Opamp Design[1]

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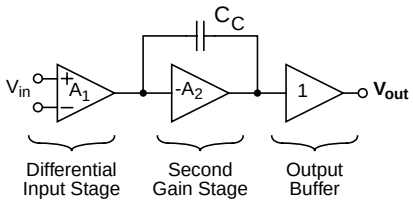
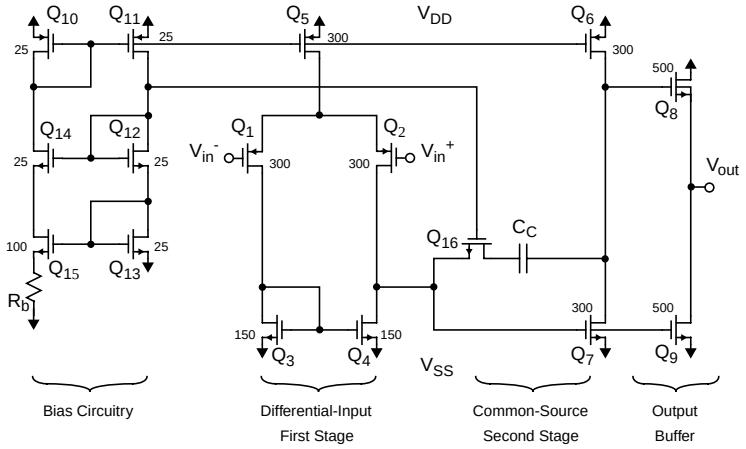
1. Much of the material presented in this section comes from the text "Analog Integrated Circuit Design," by D. Johns and K. Martin, ISBN 0-471-14448-7, Wiley, 1997.

Two-Stage CMOS Op-Amp



- Capacitor, C_C, is used to ensure stability during feedback applications.
- Example design for a 1μm process is shown below.



All transistor lengths equal 1.6 μm.

Note: Q_{16} is in triode region and realizes a small resistor used to obtain lead compensation.

Op-Amp Gain

- First stage differential-to-single ended gain is given by

$$A_{v1} = g_{m1}(r_{ds2} \| r_{ds4}) \quad (1)$$

where

- Second stage gain is given by

$$A_{v2} = -g_{m7}(r_{ds6} \| r_{ds7}) \quad (2)$$

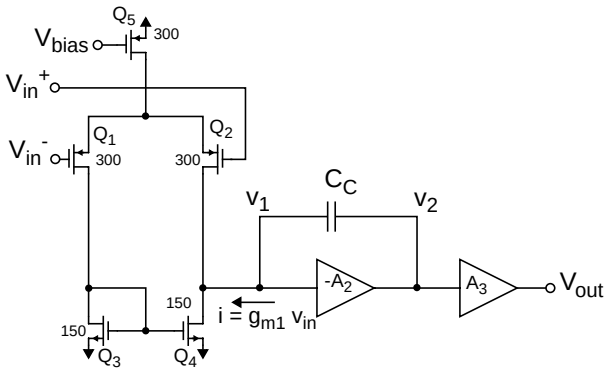
- Third stage is a source-follower and is usually only included if resistive loads need to be driven. If the load is purely capacitive, as is usually the case for integrated op-amps, it is seldom included.

$$A_{v3} \cong \frac{g_{m8}}{G_L + g_{m8} + g_{ds8} + g_{ds9}} \quad (3)$$

where G_L is the load conductance being driven by the buffer stage.

Frequency Response

- Ignore all capacitors except for C_C (to find response up to unity-gain freq).
- Also ignore Q_{16} for now as it is used for lead compensation (discussed later).



- Using Miller's Theorem, one can show that the equivalent load capacitance, C_{eq}, at node v_1 is given by,

$$C_{eq} = C_C(1 + A_2) \approx C_C A_2 \quad (4)$$

- The gain in the first stage can now be found resulting in

$$A_1 = \frac{v_1}{v_{in}} = -g_{m1} Z_{out1} \quad (5)$$

where

$$Z_{out1} = r_{ds2} \| r_{ds4} \| \frac{1}{sC_{eq}} \quad (6)$$

For mid-band frequencies, the impedance of C_{eq} dominates, and we can write

$$Z_{out1} \cong \frac{1}{sC_{eq}} \cong \frac{1}{sC_C A_2} \quad (7)$$

- Now, for the overall gain, we have

$$A_v(s) \equiv \frac{v_{out}}{v_{in}} = A_3 A_2 A_1 \approx A_3 A_2 \frac{g_{m1}}{sC_C A_2} \quad (8)$$

and assuming $A_3 \cong 1$, then the overall gain simplifies to

$$A_v(s) = \frac{g_{m1}}{sC_C} \quad (9)$$

- This simple equation can be used to find the approximate unity gain frequency. Specifically, to find the unity-gain frequency, ω_t, we set $|A_v(j\omega_t)| = 1$, and solve for ω_t. Performing such a procedure results in,

$$\omega_{ta} = \frac{g_{m1}}{C_C} \quad (10)$$

- Note here that the unity-gain frequency is directly proportional to g_{m1} and inversely proportional to C_C.

Slew Rate

- Slew-rate is the maximum rate at which the output changes when there are large input signals.
- For the op-amp above, when it slew-rate limits due to a large input signal present, all of the bias current of Q_5 goes into either Q_1 or Q_2, depending on whether v_{in} is negative or positive. In either case, the maximum current going into or out of C_C is simply the total bias current, I_{D5}.
- Defining the slew-rate, SR, to be the maximum rate that v_2 can change (and hence v_{out}), we have

$$SR \equiv \left.\frac{dv_{out}}{dt}\right|_{max} = \frac{I_{C_C}|_{max}}{C_C} = \frac{I_{D5}}{C_C} \tag{11}$$

where we made use of the charge equation $q = CV$ which leads to $I = dq/dt = C(dV/dt)$.

- Now since $I_{D5} = 2I_{D1}$, we can also write

$$SR = \frac{2I_{D1}}{C_C} \tag{12}$$

As well, from (10), we have $C_C = g_{m1}/\omega_{ta}$, and substituting into (12), we have

$$SR = \frac{2I_{D1}\omega_{ta}}{g_{m1}} \tag{13}$$

Recalling that

$$g_{m1} = \sqrt{2\mu_p C_{ox}\frac{W}{L}_1 I_{D1}} \tag{14}$$

we finally have another relationship for the slew-rate value.

$$SR = 2\frac{I_{D1}}{\sqrt{2\mu_p C_{ox}\frac{W}{L}_1 I_{D1}}}\omega_{ta} = V_{eff1}\omega_{ta} \tag{15}$$

where

$$V_{eff1} = |V_{GS}| - |V_t| = \sqrt{\frac{2I_{D1}}{\mu_p C_{ox}(W/L)_1}} \tag{16}$$

- As a result, ***the only way of improving the slew rate for the two-stage CMOS op-amp (besides maximizing ω_t) is to choose V_{eff1} to be as large as possible***. This is one of the major reasons for choosing p-channel input transistors rather than n-channel input transistors. Other reasons are less 1/f noise and higher unity-gain frequency (as it is limited by the transconductance of the second stage).

Systematic Offset Voltage

- To guarantee that no systematic offset voltage occurs, one need ensure that for a differential input voltage of zero, the gate voltage of Q_7 results in $I_{D7} = I_{D6}$.

  Due to the symmetry of the circuit, for zero differential input voltage, the drain of Q_4 follows that of Q_3 and one can easily show that the following relationship must hold for zero systematic offset voltage.

$$\frac{(W/L)_7}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5} \tag{17}$$

- Random variations result in offset-voltages on the order of 5 mV (or less).

Feedback and Op-Amp Compensation

• This section discusses using op-amps in closed-loop configurations and how to compensate an op-amp to ensure the closed-loop configuration is not only stable, but also has good settling characteristics.

First-Order Model of Closed-Loop Amplifier

• A simple first-order model for the transfer-function of a dominant-pole compensated op-amp, $A(s)$, is given by

$$A(s) = \frac{A_o}{(1 + s/\omega_{p1})} = \frac{A_o}{(1 + s\tau_1)} \tag{18}$$

where A_o is the dc gain of the op-amp and $\omega_{p1} = 1/\tau_1$ is the (real-axis) dominant pole.

• Since the unity-gain frequency of the op-amp, ω_{ta}, is much higher than ω_{p1}, we have,

$$\left|A(j\omega_{ta})\right| = 1 \approx \frac{A_o}{\omega_{ta}/\omega_{p1}} \tag{19}$$

and thus the following important relationship for this first-order model.

$$\omega_{ta} \approx A_o\omega_{p1} \tag{20}$$

• ***From here on, we define*** ω_{ta} ***to be exactly equal to*** $A_o\omega_{p1}$ ***which is approximately equal to the unity-gain frequency of the op-amp assuming a first-order model for the op-amp.***

• Substituting (20) into (18) for the case where $\omega_{p1} \ll \omega \ll \omega_{ta}$, we have at ***mid-band*** frequencies

$$A(s) \approx \frac{\omega_{ta}}{s} \tag{21}$$

where $\omega_{ta} \approx g_{m1}/C_C$ for two-stage op-amp.

• This approximate relationship is often used to analyze a closed-loop circuit for the effects of the op-amp's finite bandwidth at ***mid-band*** frequencies.

Second-Order Model of Closed-Loop Amplifier

• When we are interested in accurately modelling the frequency response around the unity-gain frequency of the op-amp, then (18) and (21) are inadequate. We must take into account higher-frequency poles and perhaps zeros. All of these can be approximately taken into account by adding a single high-frequency pole $\omega_{eq} = 1/\tau_{eq}$. $A(s)$ is now given by

$$A(s) = \frac{A_0}{(1 + s\tau_1)(1 + s\tau_{eq})} = \frac{A_0}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{eq}}\right)} \tag{22}$$

where $\tau_1 = 1/\omega_{p1}$ is the time constant of the first dominant pole and $\tau_{eq} = 1/\omega_{eq}$ is the time-constant modelling higher frequency poles.

In practice, τ_{eq}*, is found from simulation as the inverse of the frequency at which the transfer-function has a -135° phase shift (-90° due to the dominant pole and another -45° due to the higher frequency poles and zeros).*

• At frequencies much greater than the dominant pole frequency, $\omega \gg \omega_{p1} = 1/\tau_1$, we see that $1 + j\omega\tau_1 \approx j\omega\tau_1$ and so (22) can be accurately approximated by

$$A(s) \approx \frac{A_0}{\frac{s}{\omega_{p1}}\left(1 + \frac{s}{\omega_{eq}}\right)} = \frac{\omega_{ta}}{s\left(1 + \frac{s}{\omega_{eq}}\right)} \tag{23}$$

where again $\omega_{ta} = A_0\omega_{p1} = g_{m1}/C_c$ for the two-stage op-amp.

• Recalling that the closed-loop gain is given by

$$A_{CL}(s) = \frac{A(s)}{1 + \beta A(s)} \tag{24}$$

we have using (23)

$$A_{CL}(s) = \frac{A_{CL0}}{1 + \frac{s}{\beta\omega_{ta}} + \frac{s^2}{\beta\omega_{ta}\omega_{eq}}} \tag{25}$$

where

$$A_{CL0} = \frac{A_0}{1 + \beta A_0} \approx \frac{1}{\beta} \tag{26}$$

• The result of (25) can be equated to the general equation for a second-order all-pole transfer function written as

$$H_2(s) = \frac{K\omega_o^2}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2} = \frac{K}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{27}$$

where ω_o is called the resonant frequency and Q is called the Q-factor.

• Equating (25) with (27), and solving for ω_o and Q results in

$$\omega_0 = \sqrt{\beta\omega_{ta}\omega_{eq}} \tag{28}$$

and

$$Q = \sqrt{\frac{\beta\omega_{ta}}{\omega_{eq}}} \tag{29}$$

• For good transient response, we prefer $Q = 1/2$. Using (29), we see we need

$$\frac{\beta\omega_{ta}}{\omega_{eq}} = \frac{1}{4} \tag{30}$$

• For the two-stage op-amp, where $\omega_{ta} = g_{m1}/C_c$, we need

$$C_c = \frac{4\beta g_{m1}}{\omega_{eq}} \tag{31}$$

• In the case where $Q > 0.5$, the poles are complex conjugate and the percentage overshoot of the output voltage for a step input change is given by

$$\%\ \text{overshoot} = 100e^{-\frac{\pi}{\sqrt{4Q^2-1}}} \tag{32}$$

Op-Amp Compensation - Loop Response and Phase Margin

• Consider the transfer function for the loop-gain $LG(s) = \beta A(s)$

$$LG(s) \cong \frac{\beta A_0}{\frac{s}{\omega_{p1}}\left(1 + \frac{s}{\omega_{eq}}\right)} = \frac{\beta\omega_{ta}}{s\left(1 + \frac{s}{\omega_{eq}}\right)} \tag{33}$$

• We have

$$|LG(\omega)| = \frac{\beta\omega_{ta}}{\omega}\frac{1}{\sqrt{1 + (\omega/\omega_{eq})^2}} \tag{34}$$

• The unity-gain frequency, ω_t, of the loop-gain, LG(s), can now be found by setting $|LG(\omega_t)| = 1$. This gives

$$\beta\frac{\omega_{ta}}{\omega_{eq}} = \frac{\omega_t}{\omega_{eq}}\sqrt{1 + \left(\frac{\omega_t}{\omega_{eq}}\right)^2} \tag{35}$$

For $Q = 1/2$, and therefore from (30) $(\beta\omega_{ta})/\omega_{eq} = 1/4$, using (35) we get $\omega_t/\omega_{eq} = 0.243$ which is slightly less than $1/4$.

• The phase-margin, PM, is an often-used figure-of-merit for how far an op-amp with feedback is from becoming unstable. It is defined as the difference between the actual phase-shift and -180°. From (23), the actual phase-shift, $\angle LG(j\omega)$, is easily found as

$$\angle LG(j\omega) = -90° - \tan^{-1}(\omega/\omega_{eq}) \tag{36}$$

implying that at the unity-gain frequency, $s = j\omega_t$, we have

$$PM = \angle LG(j\omega_t) - (-180°) = 90° - \tan^{-1}(\omega_t/\omega_{eq}) \tag{37}$$

and therefore for $Q = 1/2$, and $\omega_t/\omega_{eq} = 0.243$ we get the required phase margin is

$$PM = 76° \tag{38}$$

For practical designs, we actually need more than this to account for processing and temperature variations. Prudent designers would normally design for 80° ***to*** 85° ***phase margins.***

- Note that for a specified phase marging the unity-gain frequency of the loop is independent of the the feedback factor, β, and therefore of the closed-loop gain as well, for an optimally compensated amplifier.
- It is now possible to relate a specified phase-margin to the Q-factor. Equation (37) can be used to find ω_t/ω_{eq}. This result can be substituted into (35) to find $\beta(\omega_{ta}/\omega_{eq})$, which can then be substituted into (29) to find the equivalent Q-factor. Finally, (32) can be used to find the corresponding percentage overshoot for a step input. This procedure allows the following table to be constructed.

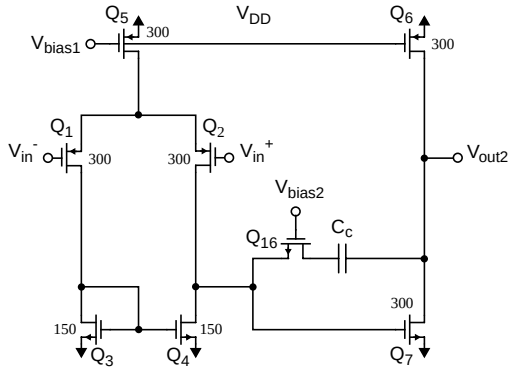
PM (Phase-Margin)	ω_t/ω_{eq}	Q-factor	%-overshoot for a step input
55°	0.700	0.925	13.3%
60°	0.580	0.817	8.7%
65°	0.470	0.717	4.7%
70°	0.360	0.622	1.4%
75°	0.270	0.527	0.008%

Soon, we shall see that when lead-compensation is used, then an ω_t/ω_{eq} ration of 0.7 can be achieved with greater than 80° phase marging. This is a substantial improvement over when lead compensation is not used and $\omega_t/\omega_{eq} < 0.25$.

- It is worth mentioning here that in the case where the feedback network is frequency independent and less than unity, (i.e. $\beta \le 1$), the worst-case phase-margin occurs for $\beta = 1$. Thus, for a general purpose op-amp where $0 < \beta \le 1$, if the op-amp is compensated for $\beta = 1$, it is guaranteed to be stable for all other β although it will not be optimally compensated and will be slower than necessary.

Compensating the Two-Stage Op-Amp

- Consider the first two stages of the two-stage op-amp as shown below.



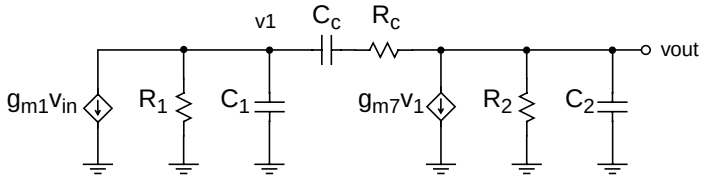
- Capacitor, C_C, realizes dominant-pole compensation. It controls the dominant first pole, (i.e. $\omega_{p1} = 1/\tau_1$), and thereby the frequency ω_{ta}, since from (20)

$$\omega_{ta} = A_o\omega_{p1} \tag{39}$$

- The transistor, Q_{16}, has $V_{DS16} = 0$ since no dc bias current flows through it and is therefore hard in the triode region. Thus, this transistor operates as a resistor, R_C, of value given by

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_{16} V_{eff16}} \tag{40}$$

- The reason for the inclusion of this transistor is to realize a left-half-plane zero at frequencies around or slightly above ω_t resulting in ***lead-compensation***.
- A simplified small-signal model for this op-amp is shown below,
- To see the need for R_C, the analysis will first be done assuming $R_C = 0$. Performing nodal analysis at the nodes designated by v_1 and v_{out}, the following transfer function is obtained.



$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}g_{m7}R_1R_2\left(1-\frac{sC_C}{g_{m7}}\right)}{1+sa+s^2b} \tag{41}$$

where

$$a = (C_2+C_C)R_2 + (C_1+C_C)R_1 + g_{m7}R_1R_2C_C \tag{42}$$

and

$$b = R_1R_2(C_1C_2 + C_1C_C + C_2C_C) \tag{43}$$

- It is possible to find approximate equations for the two poles based on the assumption that the poles are real and widely separated. This assumption allows us to express the denominator, D(s), as

$$D(s) = \left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right) \approx 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}} \tag{44}$$

- Setting the coefficients of (41) equal to the coefficients of (44) and solving for ω_{p1} and ω_{p2} results in the following relationships. The dominant pole, ω_{p1}, is given by

$$\begin{aligned}\omega_{p1} &\approx \frac{1}{R_1[C_1+C_C(1+g_{m7}R_2)]+R_2(C_2+C_C)} \\ &\approx \frac{1}{R_1C_C(1+g_{m7}R_2)} \\ &\approx \frac{1}{g_{m7}R_1R_2C_C}\end{aligned} \tag{45}$$

while the non-dominant pole, ω_{p2}, is given by

$$\begin{aligned}\omega_{p2} &\approx \frac{g_{m7}C_C}{C_1C_2 + C_2C_C + C_1C_C} \\ &\approx \frac{g_{m7}}{C_1+C_2}\end{aligned} \tag{46}$$

- Note that from (41), there is also a zero, ω_z, located in the right-half-plane given by

$$\omega_z = -\frac{g_{m7}}{C_C} \tag{47}$$

(Note that ω_z is the coefficient in the factor $(1+s/\omega_z)$ and therefor a negative sign represents a right-half-plane zero)

- Making C_C larger leaves the second pole larger unaffected but moves the first pole to a lower frequency. This 'pole-splitting' minimizes the affect of the second pole.
- A problem arises due to the right-half-plane zero, ω_z. Because the zero is in the right-half-plane, it introduces negative phase-shift (or phase-lag) in the transfer function of the op-amp. This makes achieving stability more difficult. Making C_C larger does not help because it decreases the frequencies of both the first pole and the zero without making them more widely separated.
- Fortunately, all is not lost, as introducing R_C allows adequate compensation, as will be discussed next.

Lead Compensation

- If the small-signal model is re-analyzed, but with R_C non-zero, then a third order denominator results. The first two poles are still approximately at the frequencies given by (45) and (46). The third pole is at a high frequency and has almost no effects.
- The zero is now determined by the relationship,

$$\omega_z = \frac{1}{C_C(R_C - 1/g_{m7})} \tag{48}$$

- This result allows the designer a number of possibilities. One could take

$$R_C = 1/g_{m7} \tag{49}$$

to eliminate the right-half-plane zero altogether.

- Alternatively, one could consider choosing R_C to be even larger and thus move the right-half-plane zero into the left-half-plane to cancel the non-dominant pole, ω_{p2}. Setting (48) equal to (46) and solving for R_C results in the following equation for R_C.

$$R_C = \frac{1}{g_{m7}}\left(1 + \frac{C_1 + C_2}{C_C}\right) \tag{50}$$

- Unfortunately, C_2 is often not known a priori, especially when no output stage is present.
- The third possibility is to choose R_C even larger yet to move the now left-half-plane zero to a frequency slightly greater than the unity-gain frequency that would result if the lead-resistor was not present — say, 20% larger. For this case, one should satisfy the following equation

$$\omega_z = 1.2\omega_t \tag{51}$$

and assuming $R_C \gg 1/g_{m7}$, then $\omega_z \approx 1/(R_C C_C)$ and recalling $\omega_t \approx g_{m1}/C_C$ then one should choose R_C according to

$$R_C \approx \frac{1}{1.2g_{m1}} \tag{52}$$

Compensation Pocedure

The recommended procedure for compensation is as follows:

a) Start by choosing somewhat arbitrarily $C_C' \cong 5$ pF.

b) Using SPICE, find the frequency where there is a -125° phase shift. Let the gain at this frequency be denoted A'. Also let the frequency be denoted ω_t. This is the frequency that we would like to become the unity-gain frequency of the loop gain.

c) Choose a new C_C so that ω_t becomes the unity-gain frequency of the loop-gain, thus resulting in a $55°$ phase-margin (and the reason for the choice of -125° used above). This can be achieved by taking C_C according to the equation

$$C_C = C_C'A' \tag{53}$$

It might be necessary to iterate on C_C a couple of times using SPICE.

d) Choose R_C according to

$$R_C = \frac{1}{1.2\omega_t C_C} \tag{54}$$

This choice will increase the unity-gain frequency by about 20%, leaving the zero near to the final resulting unity-gain frequency, which will end up about 15% below the the equivalent second pole frequency. The resulting phase margin is approximately $-85°$ [1]. This allows a margin of $5°$ to account for processing variations without the poles of the closed-loop response becoming real. ***This choice is also near optimum lead-compensation for almost any opamp when a resistor is placed in series with the compensation capacitor.*** It might be necessary to iterate on R_C a couple of times to optimize the phase-margin. ***However, it should be checked that the gain continues to steadily decrease at frequencies above the new unity-gain frequency, otherwise the transient response can be poor***. This situation sometimes occur when unexpected zeros at frequencies only slightly greater than ω_t are present.

e) If after d), the phase-margin is not adequate, then increase C_C while leaving R_C constant. This will move both ω_t and the lead-zero to lower frequencies, while keeping their ratio approximately constant, thus minimizing the effects of higher-frequency poles and zeros which, hopefully, do not also move to lower frequencies. In most cases, the higher-frequency poles and zeros (except for the lead zero) will not move to significantly-lower frequencies when increasing C_C.

Making Compensation Independent of Process and

1. The first pole contributes $-90°$ phase margin, the lead zero contributes approximately $45°$ phase margin, and the equivalent second pole contibutes approximately $-45°$ phase margin.

Temperature

In this section, it is shown how lead-compensation can be made process and temperature insensitive. Re-iterating equations (10), and (46), we have

$$\omega_t = \frac{g_{m1}}{C_C} \tag{55}$$

and

$$\omega_{p2} \approx \frac{g_{m7}}{C_1 + C_2} \tag{56}$$

- We see here that the second pole is proportional to the transconductance of the drive transistor of the second stage, g_{m7}. Also, the unity-gain frequency is proportional to the transconductance of the input transistor of the first stage, g_{m1}. Furthermore, the ratios of all of the transconductances remain relatively constant over process and temperature variations since the transconductances are all determined by the same biasing network. As well, most of the capacitances also track each other since they are primarily determined by gate oxides. Repeating (48), when a resistor is used to realize lead compensation, the lead zero is at a frequency given by

$$\omega_z = \frac{1}{C_C(1/g_{m7} - R_C)} \tag{57}$$

- Thus, if R_C can also be made to track the ***inverse of transconductances***, and in particular $1/g_{m7}$, then the lead zero will also be proportional to the transconductance of Q_7. As a result, the lead zero will remain at the same relative frequency with respect to ω_t and ω_{p2}, as well as all other high-frequency poles and zeros. In other words, the lead-compensation will be mostly independent of process and temperature variations.
- R_C can be made proportional to $1/g_{m7}$ as long as R_C is realized by a transistor in the triode region having an effective gate-source voltage proportional to that of Q_7. To see this result, recall that R_C is actually realized by Q_{16}, and therefore we have

$$R_C = r_{ds16} = \frac{1}{\mu_n C_{ox}(W/L)_{16} V_{eff16}} \tag{58}$$

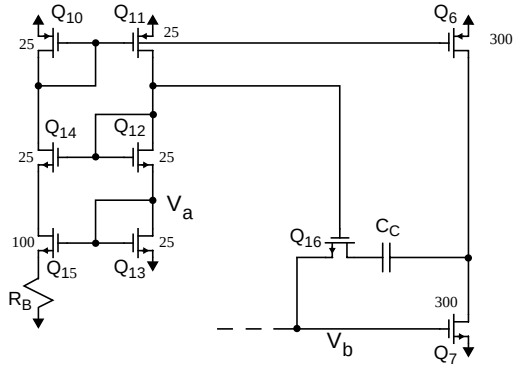
Also, g_{m7} is given by

$$g_{m7} = \mu_n C_{ox}(W/L)_7 V_{eff7} \tag{59}$$

- Thus the product $R_c g_{m7}$, which is desired to be a constant, is given by

$$R_C g_{m7} = \frac{(W/L)_7 V_{eff7}}{(W/L)_{16} V_{eff16}} \tag{60}$$

- Therefore, all that remains is to ensure that V_{eff16}/V_{eff7} is independent of process and temperature variations since clearly the remaining terms depend only on a geometric relationship. The ratio V_{eff16}/V_{eff7} can be made constant by deriving V_{GS16} from the same biasing circuit used to derive V_{GS7}. Specifically, consider the circuit shown below, It is straightforward to show that



The bias circuit, second-stage and compensation circuit of the two-stage op-amp.

$$R_C g_{m7} = \frac{(W/L)_7}{(W/L)_{16}} \sqrt{\frac{(W/L)_{12}}{(W/L)_{13}}} \tag{61}$$

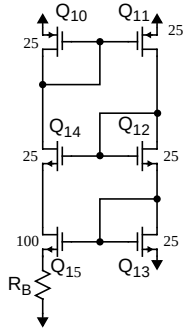
which is only dependant on geometry and not on processing or temperature variations.

- As a result, we have guaranteed that the drain-source resistance of a transistor in the triode region is inversely matched to the transconductance of a different transistor.
- This relationship can be very useful for many other applications as well. Indeed, in the next section, we will see that it's quite simple to make all of the transconductances of transistors in an IC match the conductance of a single off-

chip resistor. ***This approach results in the possibility of on-chip "resistors", realized using triode-region transistors, that are accurately ratioed with respect to a single off-chip resistor.***

Biasing an Op-Amp to Have Stable Transconductances

- This stabilization can be achieved by using a circuit approach first proposed in [Steininger, 1990] where transistor transconductances are matched to the conductance of a resistor. As a result, to a first-order effect, the transistor transconductances are independent of power-supply voltage, as well as process and temperature variations.
- For convenience, the bias-circuit above is shown again.



- First, it is assumed that $(W/L)_{10} = (W/L)_{11}$. This equality results in both sides of the circuit having the same current due to the current-mirror pair Q_{10}, Q_{11}. As a result, we also must have $I_{D15} = I_{D13}$. Now, around the loop consisting of Q_{13}, Q_{15}, and R_B, we have

$$V_{GS13} = V_{GS15} + I_{D15}R_B \tag{62}$$

and recalling that $V_{effi} = V_{GSi} - V_t$, we can subtract the threshold voltage, V_t, from both sides resulting in

$$V_{eff13} = V_{eff15} + I_{D15}R_B \tag{63}$$

This equation can also be written as

$$\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_{D15}}{\mu_n C_{ox}(W/L)_{15}}} + I_{D15}R_B \tag{64}$$

and since $I_{D13} = I_{D15}$, we can also write

$$\sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{13}}} = \sqrt{\frac{2I_{D13}}{\mu_n C_{ox}(W/L)_{15}}} + I_{D13}R_B \tag{65}$$

Re-arranging, we obtain

$$\frac{2}{\sqrt{2\mu_n C_{ox}(W/L)_{13} I_{D13}}}\left(1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right) = R_B \tag{66}$$

and recalling that $g_{m13} = \sqrt{2\mu_n C_{ox}(W/L)_{13} I_{D13}}$ results in the important relationship

$$g_{m13} = \frac{2\left(1 - \sqrt{\frac{(W/L)_{13}}{(W/L)_{15}}}\right)}{R_B} \tag{67}$$

- Thus, the transconductance of Q_{13} is determined by geometric ratios only, independent of power-supply voltages, process parameters, temperature, or any other parameters with large variability. For the special case of $(W/L)_{15} = 4(W/L)_{13}$, we have simply

$$g_{m13} = \frac{1}{R_B} \tag{68}$$

- Note that, not only is g_{m13} stabilized, but all other transconductances are also stabilized since all transistor currents are derived from the same biasing network, and, therefore, the ratios of the currents are mainly dependant on geometry. We thus have for all n-channel transistors

$$g_{mi} = \sqrt{\frac{I_{Di}}{I_{D13}}} g_{m13} \tag{69}$$

and for all p-channel transistors

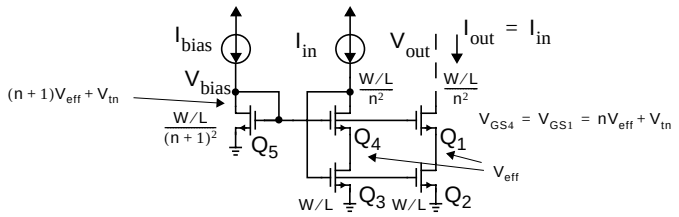
$$g_{mi} = \sqrt{\frac{\mu_p}{\mu_n}\frac{I_{Di}}{I_{D13}}} g_{m13} \tag{70}$$

- It should be noted here that the above analysis has ignored transistor output-impedance. This effect can be made of little consequence by replacing the simple current mirrors with cascode mirrors.

- Also note that the above circuit can have a second stable state where all the currents are zero. To guarantee this condition doesn't happen, it is necessary to add a "start-up circuit" which only effects the operation if all the currents are zero at start up.

Wide-Swing Current-Mirror

• The "wide-swing cascode current-mirror" is shown below [Babanezhad, 1987].



• The basic idea is to bias the transistors closest to ground to have almost the minimum possible drain-source voltages without going into the triode region.

• Before seeing how these bias voltages are created, note that the transistor pair Q_3, Q_4 act like a single diode-connected transistor in creating the gate-source voltage for Q_3. These two transistors operate very similar to how Q_3 alone would operate if its gate was connected to its source.

• To determine the bias voltages for the above circuit, let V_{eff} be the effective gate-source voltage of Q_2 and Q_3 and assume all of the drain currents are equal. We therefore have

$$V_{eff} = V_{eff2} = V_{eff3} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}(W/L)}} \tag{71}$$

• Since Q_5 has the same drain current but is $(n+1)^2$ times smaller, we have

$$V_{eff5} = (n+1)V_{eff} \tag{72}$$

• Similar reasoning results in the effective gate-source voltages of Q_1 and Q_4 being given by

$$V_{eff1} = V_{eff4} = nV_{eff} \tag{73}$$

Thus,

$$V_{G5} = V_{G4} = V_{G1} = (n+1)V_{eff} + V_{tn} \tag{74}$$

and

$$V_{DS2} = V_{DS3} = V_{G5} - V_{GS1} = V_{G5} - (nV_{eff} + V_{tn}) = V_{eff} \tag{75}$$

• This drain-source voltage puts both Q_2 and Q_3 right at the edge of the triode region. Thus, the minimum allowable output voltage is now

$$V_{out} > V_{eff1} + V_{eff2} = (n+1)V_{eff} \tag{76}$$

• A common choice for n might be simply unity, in which case the current mirror operates correctly as long as

$$V_{out} > 2V_{eff} \tag{77}$$

• With a typical value of V_{eff} between 0.2V and 0.25V, the wide-swing current-mirror can guarantee all of the transistors are in the active (i.e. saturation) region even when the voltage drop across the mirror is as small as 0.4V to 0.5V.

• There is one other requirement that must be met to ensure all transistors are in the active region. Specifically, we need

$$V_{DS4} > V_{eff4} = nV_{eff} \tag{78}$$

to guarantee that Q_4 is in the active region.

• To find V_{DS4}, we note that the gate of Q_3 is connected to the drain of Q_4 resulting in

$$V_{DS4} = V_{G3} - V_{DS3} = (V_{eff} + V_{tn}) - V_{eff} = V_{tn} \tag{79}$$

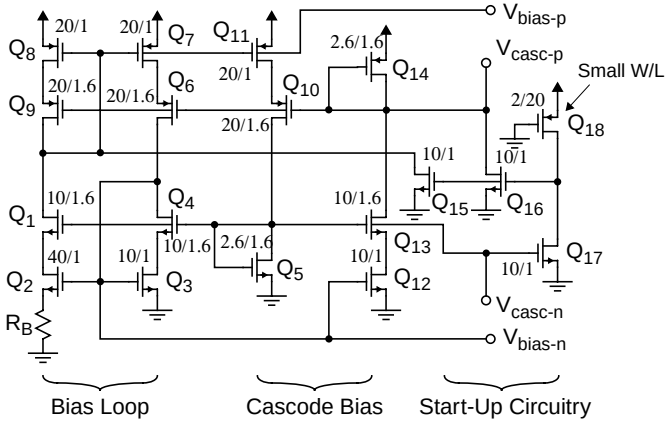
• As a result, one need only ensure that V_{tn} be greater than nV_{eff} for Q_4 to remain in the active region (not a difficult requirement).

• In most applications, an experienced designer might take $(W/L)_5$ smaller than the size shown above to bias transistors Q_2 and Q_3 with slightly larger drain-source voltages than the minimum required (perhaps 0.1V to 0.15V larger).

• Q_2 and Q_3 might be chosen to have length just a little larger than the minimum allowable gate length (as the voltage across them is quite small) but Q_1 and Q_4 might be chosen to have longer gate lengths since the output transistor (i.e. Q_1) often has larger voltages across it. Minimizing the lengths of Q_2 and Q_3 maximizes the frequency response, as their gate-source capacitances are the most significant capacitances contributing to high frequency poles.

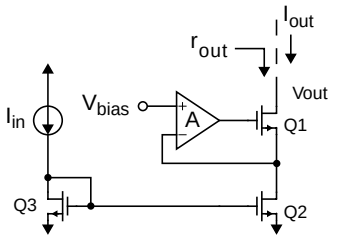
Wide-Swing Constant-Transconductance Bias Circuit

- It is possible to include the wide-swing current-mirrors into the constant-transconductance bias circuit [Martin, 1985]. This eliminates many of the second-order errors of the constant transconductance circuit and is still useable at 3V power supplies voltages.



- Notice that a start-up circuit has been included in a real implementation.
- Notice also that cascode transistors are taken as $2L_{min}$, whereas common-source transistors are $1.2L_{min}$

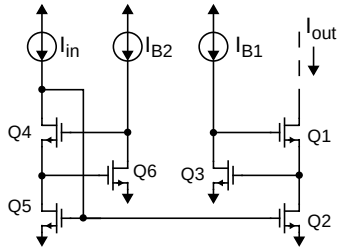
Enhanced Output-Impedance



$$r_{out} \approx g_m r_{ds}^2 (1 + A)$$

- The basic idea is to use a feedback amplifier to keep the drain-source voltage across Q_2 as stable as possible, irrespective of the output voltage. The addition of this amplifier ideally increases the output impedance by a factor equal to one plus the loop gain over that which would occur for a classical cascode current-mirror.

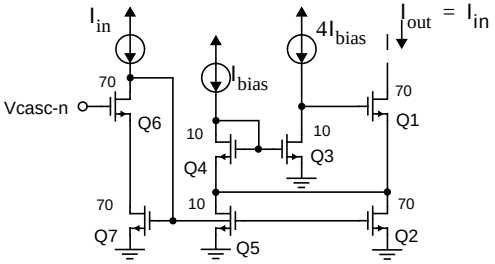
- The implementation proposed by Säckinger is shown below.



- The feedback amplifier in this case is realized by the common-source amplifier consisting of Q_3 and its current source I_{B1}. Assuming the output impedance of current-source I_{B1} is approximately equal to r_{ds3}, the loop-gain will be $(g_{m3}r_{ds3})/2$, and the final ideal output impedance will be given by

$$r_{out} \cong \frac{g_{m1}g_{m3}r_{ds1}r_{ds2}r_{ds3}}{2} \qquad (80)$$

- The circuit consisting of Q_4, Q_5, Q_6, I_{in}, and I_{B2} operates almost identically to a diode-connected transistor, but is instead used to guarantee that all transistor bias voltages are accurately matched to those of the output circuitry consisting of Q_1, Q_2, Q_3, and I_{B1}. As a result, I_{out} will very accurately match I_{in}.
- This realization has a major limitation that the signal swing is significantly reduced. This reduction is a result of Q_2 and Q_5 being biased to have drain-source voltages much larger than the minimum required.
- For a wide-swing current mirror with enhanced output-impedance [Gatti, 1990] and [Coban, 1994], [and myself after the fact]. Q_4 is used as a level-shift to bias

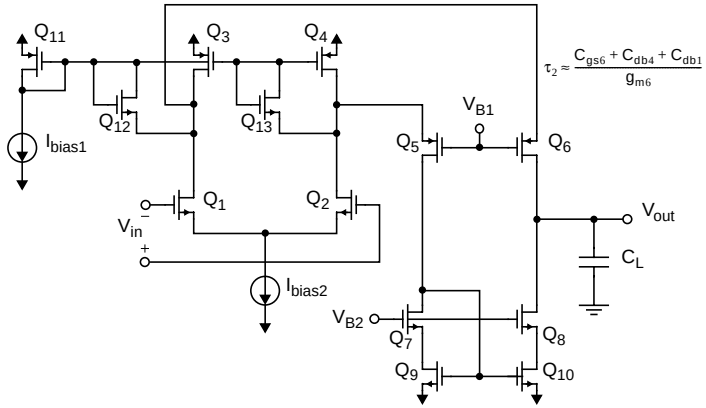


Q_2 near the edge of the active region.

- Output-impedance enhancement significantly increases the gain, has little effect on the small-signal transfer function, but significantly degrades the large-signal transient response (by about 50%) due to large voltage excursions at the gate of Q_1 during slew-rate limiting.

Folded-Cascode Op-Amp

- An example of an op-amp with a high-output impedance is the folded-cascode op-amp as shown below.



- Although a folded-cascode amplifier is basically a single gain-stage, its gain can be quite reasonable, on the order 700 to 3,000 typically. Such a high gain occurs because the gain is determined by the product of the input transconductance and the output impedance, and the output impedance is quite high due to the use of cascode techniques.
- The shown differential-to-single-ended conversion is realized by the wide-swing current-mirror composed of Q_7, Q_8, Q_9, and Q_{10}. In a differential-output design, these might be replaced by two wide-swing cascode current sinks, and common-mode feedback circuitry would be added, as is discussed later.
- Two extra transistors, Q_{12} and Q_{13}, have been included to increase the slew-rate performance of the op-amp. Also, more importantly, during times of slew-rate limiting, these transistors prevent the drain voltages of Q_1 and Q_2 having large transients where they change from their small-signal voltages to voltages very close to the negative power-supply voltage.

• The compensation is realized by the load capacitor, C_L, and realizes dominant-pole compensation.

Small-Signal Analysis

• In a small-signal analysis of the folded-cascode amplifier, it is assumed that the differential output current from the drains of the differential-pair, Q_1, Q_2, is applied to the load capacitance, C_L.

$$A_V = \frac{v_{out}(s)}{v_{in}(s)} = g_{m1} Z_L(s) \tag{81}$$

where g_{m1} is the transconductance of each of the transistors in the input differential-pair and $Z_L(s)$ is the impedance to ground seen at the output node.

$$A_V = \frac{g_{m1} r_{out}}{1 + s r_{out} C_L} \tag{82}$$

where r_{out} is the output impedance of the op-amp.

• For mid-band and high frequencies, we can ignore the unity term in the denominator and thus have,

$$A_V \cong \frac{g_{m1}}{s C_L} \tag{83}$$

from which the unity-gain frequency of the op-amp is easily found to be

$$\omega_{ta} = \frac{g_{m1}}{C_L} \tag{84}$$

• Therefore, for large load capacitances, maximizing the transconductance of the input transistors maximizes the bandwidth, assuming the load capacitance is large enough so that the unity-gain frequency is much less than the limit imposed by the second poles. The transconductance of the input transistors is maximized by using wide n-channel devices and ensuring the input-transistor-pair's bias current is substantially larger than the bias-current of the cascode transistors and current-mirror.

• Note that this approach also maximizes the dc gain (i.e. $g_{m1} r_{out}$) since not only does it maximize g_{m1}, but it also maximizes r_{out} by resulting in all transistors connected to the output node being biased at lower current levels (for a given total power dissipation).

• The second-poles of this op-amp are primarily due to the time-constants introduced by the impedance and parasitic capacitances at the sources of the p-channel cascode transistors, Q_5 and Q_6. The impedances at these nodes is one over the transconductances of the cascode transistors. Since p-channel transistors are used here, possibly biased at lower currents, these impedances are typically substantially greater than the source-impedances of most n-channel transistors in the signal path. As a consequence, when high-frequency operation is important, these impedances can be reduced by making the currents in the p-channel cascode transistors around the same level as the bias-currents of the input transistors.

• The parasitic capacitance at the sources of the cascode transistors is primarily due to the gate-source capacitances of the cascode transistors as well as the drain-to-bulk and drain-to-gate capacitances of the input transistors and the current-source transistors Q_3 and Q_4. Therefore, minimizing junction areas and peripheries at these two nodes is important.

Slew-Rate

• The diode-connected transistors, Q_{12} and Q_{13}, are turned-off during normal operation and have almost no effect on the op-amp. However, they substantially improve the operation during times of slew-rate limiting [Law, 1993].

• To appreciate their benefit, consider first what happens during times of slew-rate limiting when they are not present. Assume there is a large differential input voltage that causes Q_1 to be turned on hard and Q_2 to be turned off. Since Q_2 is off, all of the bias-current of Q_4 will be directed through the cascode transistor Q_5, through the n-channel current-mirror, and out of the load capacitance. Thus, the output voltage will decrease linearly with a slew-rate given by

$$SR = \frac{I_{D4}}{C_L} \tag{85}$$

• Also, since all of I_{bias2} is being diverted through Q_1, and since this current is usually designed to be greater than I_{D3}, both Q_1 and the current-source I_{bias2} will go into the triode region causing I_{bias2} to decrease until it is equal to I_{D3}.

• As a result, the drain voltage of Q_1 approaches that of the negative power-supply voltage. When the op-amp is coming out of slew-rate limiting, the drain voltage of Q_1 must slew back to a voltage close to the positive power-supply before the op-amp operates in its linear region again. This additional slewing time greatly increases the distortion and also increases the transient times during slew-rate

limiting (which occurs often for op-amps used in switched-capacitor applications).

- Next, consider the case where the diode-connected transistors, Q_{12} and Q_{13}, are included. One effect is to clamp the drain voltages of Q_1 or Q_2 so they don't change as much during slew-rate limiting.
- A second, more-subtle effect dynamically increases the bias currents of both Q_3 and Q_4 during times of slew rate limiting. This increased bias current results in a larger maximum current available for charging or discharging the load capacitance.
- To see this increase in bias current, consider the same case as above where a large differential input causes Q_1 to be fully on while Q_2 is off. In this case, the diode-connected transistor Q_{12} conducts where the current through it comes from the bias diode-connected transistor, Q_{11}. Thus, the current in Q_{11} increases causing the currents in bias-transistors Q_3 and Q_4 to also increase until the sum of the currents of Q_{12} and Q_3 are equal to the bias current I_{bias2}. Note that the current in Q_4 also increases since it is equal to the current in Q_3. This increase in bias-current of Q_4 results in an increase of the maximum current available for discharging C_L.
- In summary, not only are the voltage excursions less, but the maximum available current for charging or discharging the load capacitance is also greater during times of slew-rate limiting.

Equivalent Second-Pole Frequency

- There are three important internal nodes having time constants that contribute to the second-equivalent-pole-frequency: these are the source nodes of the common-source transistors Q_5 and Q_6, and the input node of the n-channel current mirror (i.e. the gate nodes of Q_9 and Q_{10}). Since Q_5 and Q_6 are p-channel transistors, the time constants at these nodes are probably dominant, although since there are two gates connected to the input node of the current mirror, the time constant there can be significant.
- Consider the time constant at the source of Q_5 and assume $C_{gs\text{-}5}$ is the dominant capacitance. *In analog circuits, the gate-source capacitances normally dominate since the transistors are often quite wide and junction capacitances can often be minimized by careful layout techniques.*.
- At the source of Q_5, the impedance is approximately given by

$$R_5 = \frac{1}{g_{m5}} = \frac{1}{\mu_p C_{ox}(W/L)_5 V_{eff\text{-}5}} \tag{86}$$

Approximating the total capacitance by the gate-source capacitance of Q_5, we have

$$C_5 = \frac{2}{3}(WL)_5 C_{ox} \tag{87}$$

and the time constant at the node is approximately given by

$$\tau_5 = \frac{2}{3}\frac{L_5^2}{\mu_p V_{eff\text{-}5}} \tag{88}$$

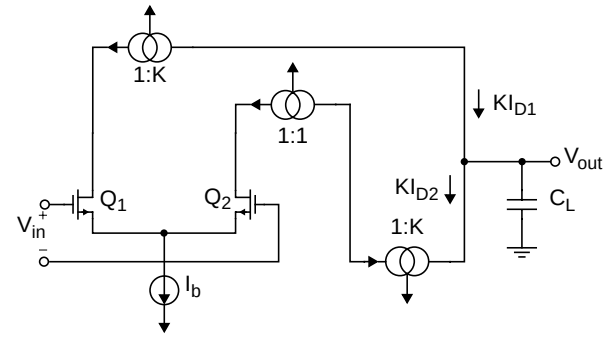
Note that for a given *effective gate-source voltage*, the time constant is relatively independent of any design parameters and primarily dependent on technology. Often the 2/3's factor is dropped to roughly take into account the junction capacitance which was ignored. For $\mu_p = 0.0175 m^2/V \cdot s$, $V_{eff\text{-}5} = 0.25V$, and $L_5 = 0.4\mu m$, this gives $\tau_5 = 36.6ps$. This corresponds to an equivalent-second-pole-frequency of $\omega_{eq} \approx 1/\tau_5 = 2.7\times 10^{10} r/s$ or $f_{eq} = 4.3GHz$. Assuming f_t is 1/4 times f_{eq}, gives $f_t = 1.1GHz$. Normally, this would be dominated by the load capacitance.

- By symmetry, the time constant at the source of Q_6 will have a similar effect in the other differential signal path. The time constant due to the n-channel current

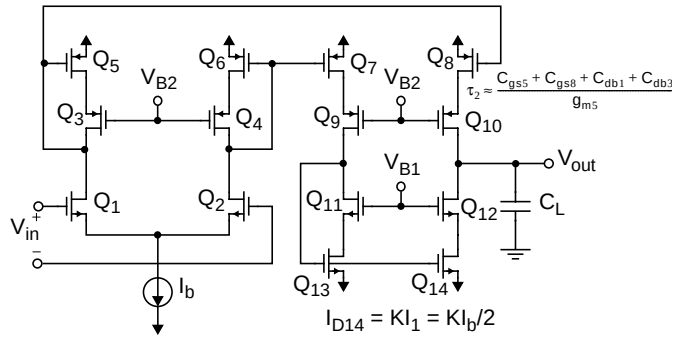
mirror may be significant but is unlikely to decrease ϖ_{eq} by more than about 1/3'rd.

- **Thus, for the folded-cascode op-amp, normally the load capacitance will be greater than is needed for stability (assuming $C_L > 2pF$) and will cause the unity-gain frequency to be significantly less than that constrained by the time constants of the internal nodes. Furthermore, there is little incentive to use p-channel transistors for the input differential-pairs (i.e. the complementary op-amp) in order to minimize the internal time constants.**

Current-Mirror Op-Amp (CMA)



- All nodes are low impedance except for the output node.
- By using good current-mirrors having high output-impedance, a reasonable over-all gain can be achieved.
- Example of an CMA with wide-swing current mirrors is shown below.



- Similar analysis to that given for the folded-cascode op-amp, we have

$$A_V = \frac{v_{out}(s)}{v_{in}(s)} = Kg_{m1}Z_L(s) = \frac{Kg_{m1}r_{out}}{1 + sr_{out}C_L} \cong \frac{Kg_{m1}}{sC_L} \tag{89}$$

- The K factor is the current-gain from the input transistors to the output sides of the current-mirrors connected to the output node. Using (89), we can solve for the unity-gain frequency resulting in

$$\omega_{ta} = \frac{Kg_{m1}}{C_L} = \frac{K\sqrt{2I_{D1}\mu_n C_{ox}(W/L)_1}}{C_L} \tag{90}$$

- If the power dissipation is specified, the total current,

$$I_{total} = (3 + K)I_{D1} \tag{91}$$

is known for a given power-supply voltage. Substituting (91) into (90), we obtain

$$\omega_{ta} = \frac{K\sqrt{2\frac{I_{total}}{3+K}\mu_n C_{ox}(W/L)_1}}{C_L} = \frac{K}{\sqrt{3+K}}\frac{\sqrt{2I_{total}\mu_n C_{ox}(W/L)_1}}{C_L} \tag{92}$$

- For larger values of K, the op-amp's transconductance is larger (i.e. Kg_{m1}), and therefore, the unity-gain frequency is also larger.
- This simple result assumes the unity-gain frequency is limited by the load capacitance rather than any high-frequency poles caused by the time-constants of the internal nodes.
- A practical upper limit on K might be around 5. The use of large K values also maximizes the gain for I_{total} fixed since r_{out} is roughly independent of K for large K. In other words, for I_{total} fixed and large K, the current through the output stage is almost equal to $I_{total}/2$.
- The important nodes for determining the non-dominant poles are the drain of Q_1, primarily, and the drains of Q_2 and Q_9, secondly. Increasing K increases the capacitances of these nodes while also increasing the impedances and thus the equivalent second pole moves to lower frequencies.
- If it is very important that speed is maximized, K might be taken as small as 1. A reasonable compromise for a general purpose op-amp might be to let $K = 2$.

Slew-Rate

- All of the bias-current of the first stage will be diverted through either Q_1 or Q_2 and amplified by the current gain of the output stage.

$$SR = \frac{KI_b}{C_L} \tag{93}$$

- For a given total power dissipation, this slew-rate is maximized by choosing a large K value.
- For example, with $K = 4$ and during slew-rate limiting, 4/5 of the total bias-current of the op-amp will be available for charging or discharging C_L.
- This result gives a CMA superior slew-rates when compared to a folded-cascode op-amp, even when the clamp transistors have been included in the folded-cascode op-amp. Also, there are no problems with large voltage transients during slew-rate limiting for the CMA.
- In summary, due primarily to the larger bandwidth and slew rate, the CMA is usually preferred over a folded-cascode op-amp.
- However, it will suffer from larger thermal noise when compared to a folded-cascode amplifier because its input transistors are biased at a lower proportion of the total bias current and therefore have a smaller transconductance.

Equivalent Second-Pole Frequency

- There are three important internal nodes having time constants that contribute to the second-equivalent-pole-frequency: these are the input nodes of the current mirrors.
- Consider the node at the gate of Q_5: the impedance is approximately given by

$$R_5 = \frac{1}{g_{m5}} = \frac{1}{\mu_p C_{ox}(W/L)_5 V_{eff\text{-}5}} \tag{94}$$

Approximating the total capacitance by the gate-source capacitances of Q_5 and Q_8, and assuming $K = 2$, and therefore $W_8 = 2W_5$, we have

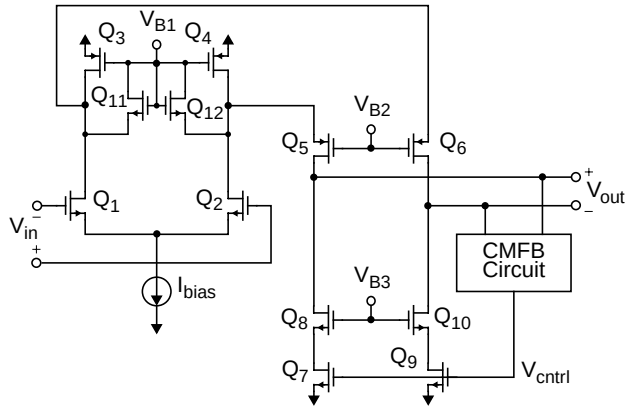
$$C_5 = \frac{2}{3}(3WL)_5 C_{ox} \tag{95}$$

and the time constant at the node is approximately given by

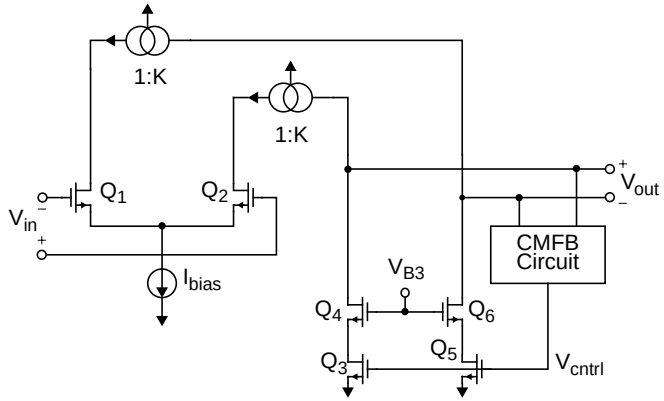
$$\tau_5 = 2\frac{L_5^2}{\mu_p V_{eff\text{-}5}} \tag{96}$$

Note that for a given *effective gate-source voltage*, the time constant is relatively independent of any design parameters and primarily dependent on technology. To roughly take into account the junction capacitance which was ignored we can replace the 2 factor by 2.5. For $\mu_p = 0.0175 m^2/V \cdot s$, $V_{eff\text{-}5} = 0.25V$, and $L_5 = 0.4\mu m$, this gives $\tau_5 = 91ps$. This corresponds to an equivalent- second-pole-frequency of $\omega_{eq} \approx 1/\tau_5 = 1.1 \times 10^{10} r/s$ or $f_{eq} = 1.7GHz$. Assuming f_t is 1/4 times f_{eq}, gives $f_t = 435MHz$. Normally, this would be dominated by the load capacitance.

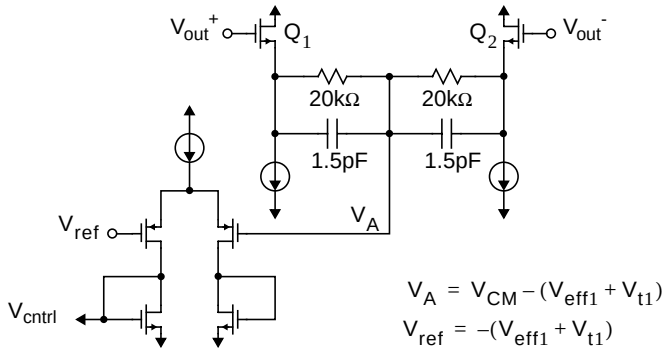
Fully-Differential Folded-Cascode Op-Amp



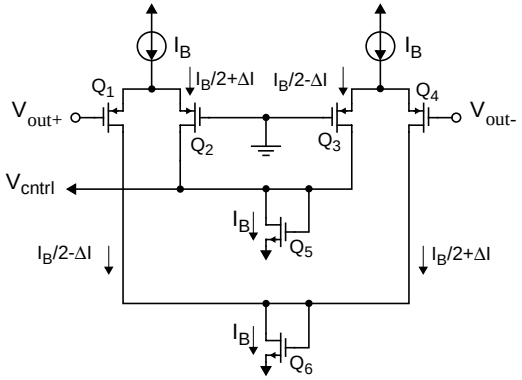
Fully-Differential CMA



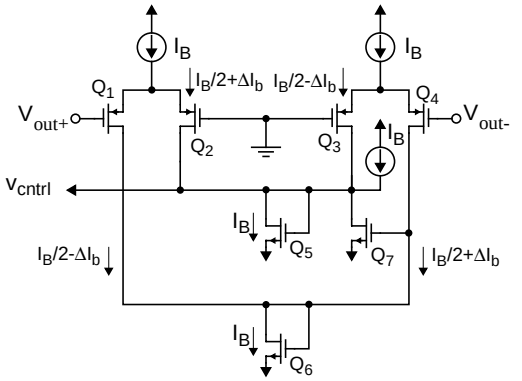
Common-Mode Feedback Circuits



- A continuous-time CMFB circuit is shown above.
- It has a major limitation in that the voltage drop across the source-follower transistors, Q_1, Q_2, severely limits the differential signals that can be processed (unless transistors with native threshold voltages, such as 0.3 volts, are available).
- The stability of the CMFB loop should be checked separately. Normally, its speed should match that of the differential loop. Since the same capacitors are used to compensate both loops, the only degree of freedom for the CMFB loop is the gain. This does not need to be large.
- Stability can be especially difficult to achieve when the differential gain is large
- A higher linearity CMFB circuit is shown below [Martin, 1985] [Gray, 1986][Whatly, 1986].
- Assuming the CMRR is perfect, this CMFB is perfectly linear irrespective of the non-linearity of the transistors.
- It should be designed so that for the maximum expected input signal, when the bias current sources are at the edge of the triode region, the transistors in the differential pair are all still conducting somewhat. This limits swings in the positive going direction to be not closer than $V_{tp} + 2V_{eff}$ within the positive power supply voltage.
- A modified version of this CMFB with more gain is shown below [Duque, 1993]
- These CMFB circuits would be greatly improved if low-threshold devices were used for the differential pairs.

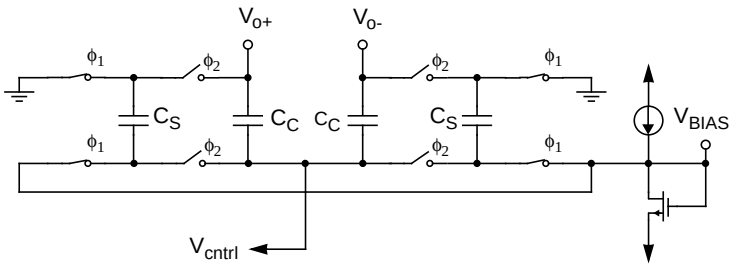


An example of a continuous-time CMFB circuit.



A modified CMFB circuit having twice the common-mode gain as compared to the previous realization.

- A switched-capacitor CMFB circuit is shown below [Senderowicz, 1982].
- In this approach, the capacitors labelled C_C generate the average of the output voltages which is used to create control voltages for the op-amp current sources. The dc voltage across C_C is determined by capacitors C_S which are switched

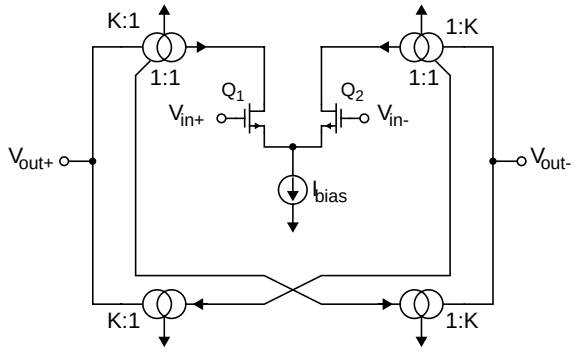


between bias voltages and between being in parallel with C_C. This circuit acts much like a simple switched-capacitor low-pass filter having a dc input signal. The bias voltages are designed to be equal to the difference between the desired common-mode voltage and the desired control voltage used for the op-amp current sources.

- In applications where the op-amp is being used to realize switched-capacitor circuits, switched-capacitor CMFB circuits are generally preferred over their continuous-time counterparts since they allow a larger output signal swing.
- When continous-time CMFB is required, the CMFB circuit is the major limitation on the signal-swing.

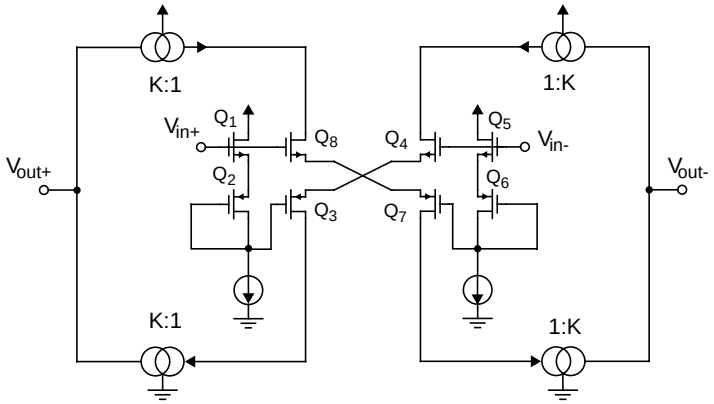
Alternative Fully-Differential Configurations

- A current-mirror op-amp with bi-directional drive capability is shown below. This has a much improved slew rate in the negative direction (for an n-channel differential pair).

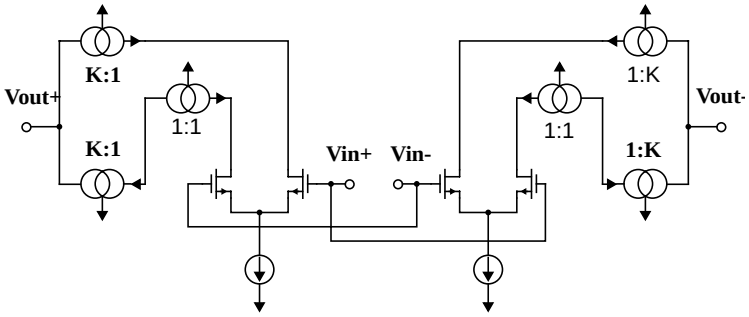


A fully-differential opamp with bi-directional output drive.

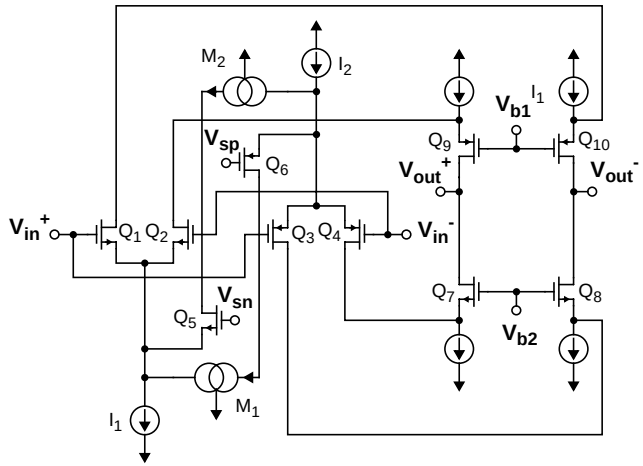
- Another alternative with bi-directional drive capability is shown below[Castello, 1989]. This configuration has a very-good slew rate but poor signal swing.
- Another alternative with bi-directional frive capability is shown below. It consists of two single-ended output op-amps connected in parallel to get a differential output op-amp.
- A low-voltage op-amp capable of handling large input common-mode voltages is shown below [Babanezhad, 1988] [Hogervorst, 1992] [Coban, 1994]. This circuit can have a transconductance and input offset voltage that are dependent on input CM voltage.



A class AB fully-differential opamp. CMFB circuit not shown.



A fully-differential opamp composed of two single-ended output current-mirror opamp's. CMFB circuit not shown.



An opamp having rail-to-rail input common-mode voltage range. CMFB circuit not shown.

Current-Feedback Amplifiers

[Comlinear, 1985], [Bowers, 1990]

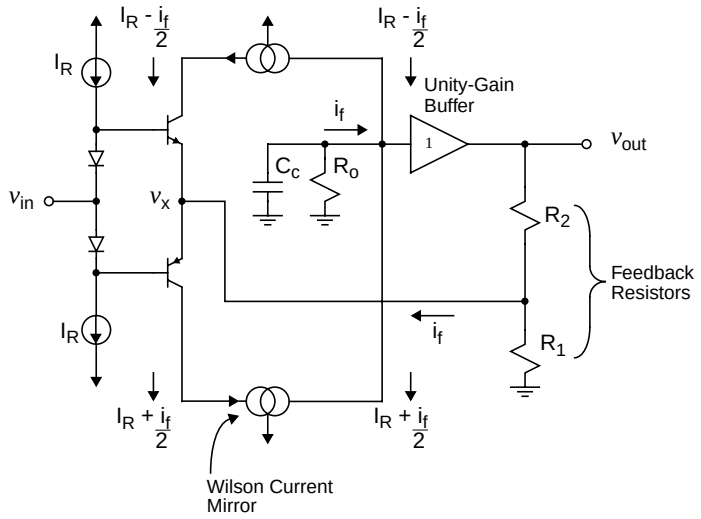
Advantages:

- Open-loop gain is independent of closed-loop gain. Thus, a single size compensation capacitor can be used irrespective of gain. Furthermore, closed-loop -3dB frequency is approximately independent of closed-loop gain.
- The amplifier almost never slew-rate limits.
- Amplifier is very fast due to all internal nodes being low impedance.

Disadvantages:

- Requires complementary process (i.e. vertical pnp's if bipolar).
- First commercially available designs have larger input referred noise and input offset voltages, as compared to voltage-mode amplifiers. These limitations may possibly be minimized in the future by careful circuit design.

Simplified Schematic



Current-mirrors would normally be Wilson current-mirrors.

Assume $1/g_{m1}$, $1/g_{m2} << R_1 \parallel R_2$.

Thus,

$$v_x \cong v_{in} \tag{97}$$

And,

$$i_f = \frac{v_{out} - v_{in}}{R_2} - \frac{v_{in}}{R_1}$$

$$\Rightarrow i_f = \frac{v_{out}}{R_2} - v_{in}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{98}$$

And

$$v_{out} = -i_f Z_L \tag{99}$$

where

$$Z_L = \frac{1}{sC_c + 1/R_c} \tag{100}$$

The open-loop gain is given by

$$LG(s) = -\frac{i_f}{v_{out}} \frac{v_{out}}{i_f} = \frac{Z_L}{R_2} = \frac{R_0/R_2}{1 + sC_cR_0} \approx \frac{1}{sC_cR_2} \tag{101}$$

Thus, LG(s) is independent of R_1! Therefore, R_1 can be changed as desired to realize any closed-loop gain without affecting the stability.

Setting

$$|LG(s)|_{s = j\omega_t} = 1 \Rightarrow \omega_t = \frac{1}{R_2C_c} \tag{102}$$

For the closed-loop gain, substitute (3), (4) into (2) and simplify to get.

$$\frac{v_{out}}{v_{in}} = \frac{1/R_1 + 1/R_2}{1/R_0 + 1/R_2 + sC_c} \tag{103}$$

$$= \frac{R_0(R_1 + R_2)}{(R_0 + R_2)R_1} \frac{1}{1 + sC_c(R_0 \| R_2)} \tag{104}$$

For $R_0 >> R_2$, we have

$$A_{cl}(s) = \frac{v_{out}}{v_{in}} = \frac{R_1 + R_2}{R_1} \frac{1}{1 + sR_2C_c} \tag{105}$$

- Thus, the -3dB frequency of $A_{cl}(s)$ is approximately equal to the unity-gain frequency of the open-loop gain, independent of R_1 and the closed-loop gain.
- This approach is becoming quite popular recently despite some problems with noise and input-offset voltages (compared to voltage-mode amplifiers). Examples are op amps from Comlinear, Harris, and Analog-Devices.

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