Programmable Current Bias Generator

Principle:

As shown in Figure 1, the main PTAT (proportional to absolute temperature) current circuit is composed of 4 MOS transistors (M_1~M_4) and 1 resistor R_x. Off-chip resistor is used for R_x for on-chip resistors usually have value variation around ±20%. M_3 and M_4 are sized to work in strong/moderate inversion for accurate current copying, and the current ratio is usually set as 1:1. M_1 and M_2 either work in moderate inversion or weak inversion. All transistors are in saturation. The generated current corresponding to different operation region of M_1 and M_2 is formulated as follows, assuming square law, perfect device matching, and secondary effects such as back-gate modulation and channel length modulation are neglected:

$$I_0 = \frac{2(\sqrt{(L/W)_2} - \sqrt{(L/W)_1})^2}{\mu C_{ox} R_x^2}$$ (Strong/Moderate Inversion),

$$I_0 = \frac{mV_T}{R_x} \ln \frac{(W/L)_1}{(W/L)_2}$$ (Weak Inversion),

where W and L are transistor's width and length, μ is carrier mobility, C_{ox} is gate capacitance, m is the subthreshold slope parameter, V_T is the thermal voltage.

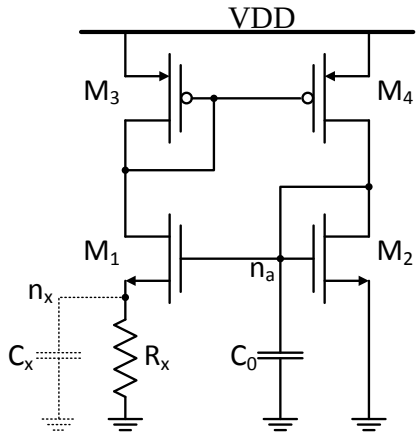


Figure 1. Main PTAT Current Circuit

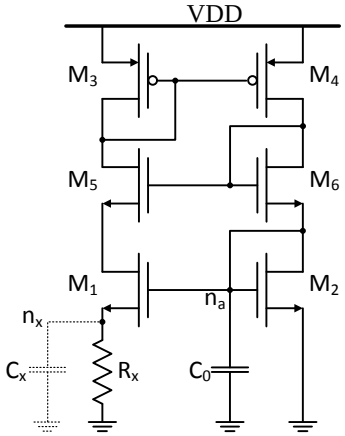


Figure 2. Cascaded PTAT Current Circuit

μ is proportional to temperature T^m, where m is usually in the range of 1~2. Thus the circuit with M_1 and M_2 working in strong/moderate inversion generates current that deviates from PTAT to some extent. V_T, however, is strictly proportional to T, thus the subthreshold mode guarantees more ideal PTAT current.

Transistors with long L are used to approximate square law and reduce channel length modulation effect. Large transistors are employed to improve matching. Particularly, the same lengths for M_1 and M_2, and also for M_3 and M_4 are used to avoid threshold voltage difference caused by short channel length effect or reverse short channel length effect in deep sub-micron process. To further alleviate the current

dependence on supply voltage, cascaded structure could be exploited as shown in figure2. Transistors M_5 and M_6 don't necessarily have the same sizes as M_1 and M_2. Actually they could be much smaller as the matching between M_5 and M_6 has little effect on the circuit performance.

If threshold voltage difference caused by back-gate modulation effect is taken into account, the generated current (weak inversion mode) is derived as:

$$I_0 = \frac{mV_T}{R_x}\ln\frac{(W/L)_1}{(W/L)_2} + \frac{V_{TH2} - V_{TH1}}{R_x},$$

where V_{TH1} and V_{TH2} are the threshold voltages of M_1 and M_2, respectively. The error is dependent on the voltage at node n_x, which varies with temperature and is also process dependent due to variation of back-gate effect coefficient.

There are two stable working mode for the PTAT current circuit, zero-current mode and normal mode. In zero-current mode, the currents in all transistors are close to zero; therefore it's not the proper working mode for correct function. To force the circuit to enter normal mode after power up, additional start-up circuit is needed. Main bias circuit with start-up circuit is illustrated in figure 3. When power up, initially, the voltages at nodes n_a, n_b and n_d are close to ground, and the voltage at node n_c is close to VDD. Thus M_8 is on, and n_a and n_b are gradually charged up, and simultaneously n_c is pulled low. Then M_7 is turned on and n_d is charged close to VDD. Consequently M_8 is turned off, and the start-up circuit doesn't inject or pull currents into the main PTAT circuit anymore. In this way, proper currents injection into the main PTAT circuit is accomplished by the start-up circuit when power up, which avoids the zero-current mode.

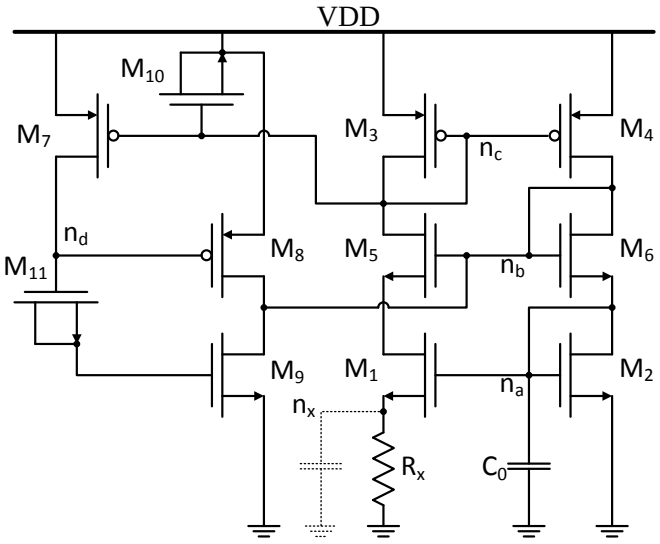


Figure 3. PTAT Current Circuit with Start-Up

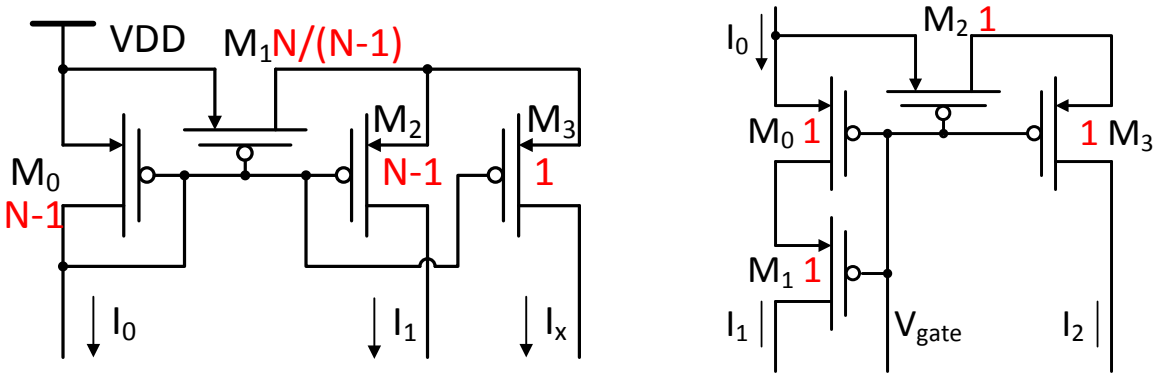
It is easy to notice that the loop formed by M_1~M_4 is a positive feedback. To make sure stable operation, the loop gain should be always less than 1. However, this is not guaranteed in all frequency range,

especially when large parasitic capacitance exists at node n_x. The loop gain of the PTAT circuit in figure 1 can be approximately calculated as:

$$A_{loop} = \frac{g_{m1}}{g_{m2}} \bullet \frac{1}{(1+\frac{g_{m1}R_x}{1+sC_xR_x})(1+\frac{sC_0}{g_{m2}})}.$$

If C_0=0, the limit of A_{loop} at high frequency is 1, providing g_{m1}=g_{m2} for idea subthreshold operation of M_1 and M_2. This could lead to instability as g_{m1} is larger than g_{m2} when non-idealities such as channel length modulation are considered. If $C_0 \neq 0$, the limit is $g_{m1}/(sC_0)$, which is always much less than 1.

To digitally program the final output current, configurable current divider is used. The circuit topologies are sketched in figure 4. The red expressions in the figure are the dimension ratios among all the transistors in two topologies, respectively. The comparison between the two topologies is shown in table 1. Current multiplying with flexible current ratio could be implemented by some modifications based on topology A.



(A) Current Divider A (B) Current Divider B

Figure 4. Current Dividers

Table 1. Comparison of Two Current Dividers

	Current Divider A	Current Divider B
Current Ratio	$I_0=N\times I_1=N^2\times I_x$	$I_0=2\times I_1=2\times I_x$
Pro	flexible current ratio	more accurate current dividing
Con	only accurate current dividing when all transistors obey square law; accuracy compromised in subthreshold	fixed current ratio; less voltage headroom for certain supply; additional bias voltage V_{gate}

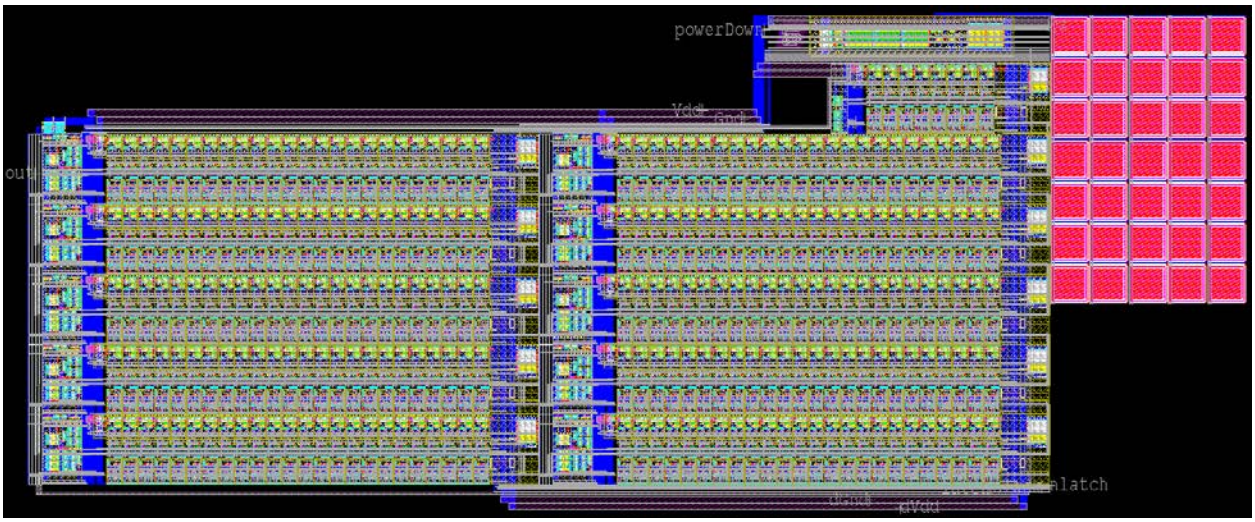
The current branches which are connected to the output buffer are selected by MOS switches, and the selection digital bits are input by shift-registers and stored in latches.

Simulation and Layout:

The generated current during shifting in configuration bits period is shown in figure 5.

Figure 5. Generated current during configuration bits shifted in

The layout is shown in Figure 6.



Some attentions need to be paid on main PTAT current circuit layout for less current variation among fabricated chips: 1. Wide connection metal wires for small voltage drops, especially between M_1 and R_x pad, and M_2 and ground; 2. Dummy transistors to improve matching besides large area and symmetry, specifically between M_1 and M_2, and M_3 and M_4.