

Why analog microelectronics?



- Digital is taking over?
 - Yes, but electrical signals are fundamentally analog!
 - Analog design has proven fundamental for high-quality design of complex systems
- Mixed-mode systems
 - Natural signals are analog
 - Sound in microphone
 - Photocells in cameras
 - Temperature sensors
 - All real world systems require interfacing to analog

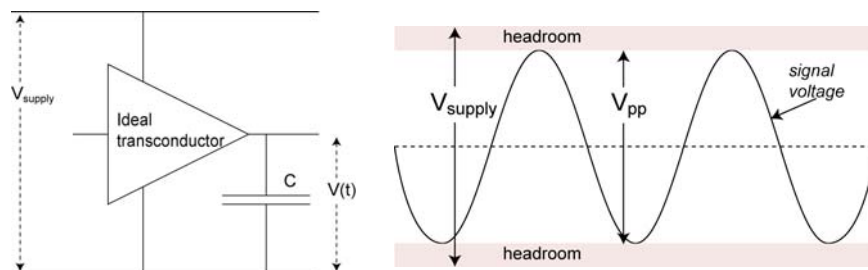
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Limitations of analog design



- Supply voltage limitations
 - Lower limit: noise
 - Upper limit: headroom < supply
 - Aiming for active region



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Upper signal limit

- Active region requirements

- weak inversion:

$$V_{DS} > V_{eff} = 4 - 5 U_T$$

$$U_T \approx 26mV \text{ at roomtemperature}$$

- strong inversion:

$$V_{DS} > V_{eff} = V_{GS} - V_{m(p)}$$

- Available headroom

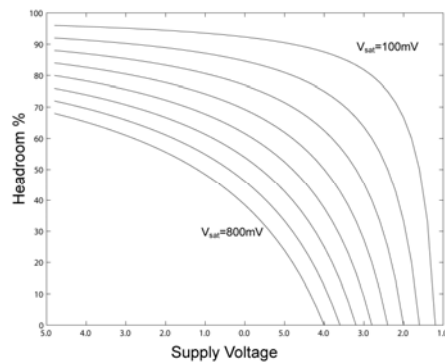
$$V_{eff} = 100mV - 800mV$$

Upper signal limit V_{eff} from rail voltage

$$V_{max} = V_{supply} - V_{eff}$$

Weak inversion lower saturation voltage

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Upper signal limit

- Active region requirements

- weak inversion:

$$V_{DS} > V_{eff} = 4 - 5 U_T$$

$$U_T \approx 26mV \text{ at roomtemperature}$$

- strong inversion:

$$V_{DS} > V_{eff} = V_{GS} - V_{m(p)}$$

- Available headroom

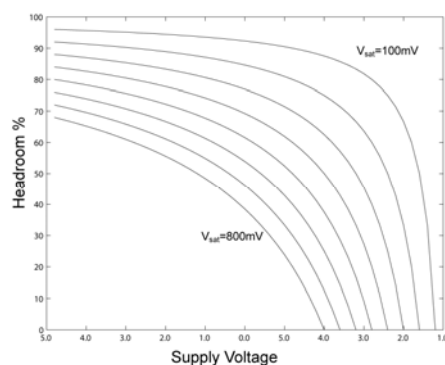
$$V_{eff} = 100mV - 800mV$$

Upper signal limit V_{eff} from rail voltage

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Weak inversion lower saturation voltage

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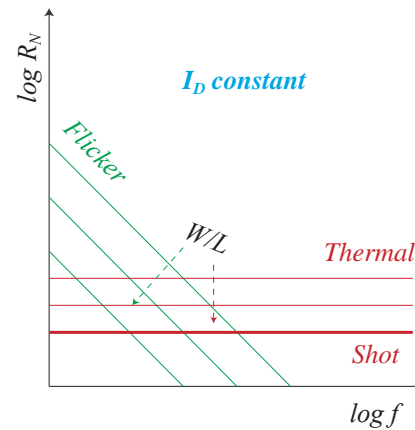


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Lower signal limit

- Noise vs. Frequency
 - Weak inversion → shot noise
 - Strong inversion → thermal noise
- Lower signal limit
 - Noise
 - Frequency dependant
 - Thermal noise
 - Flicker noise (LF)



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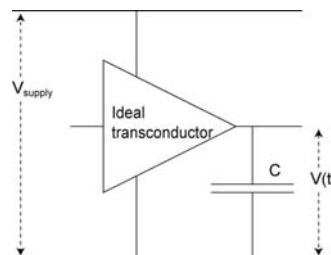
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Limitations

- Ratio between largest and smallest signal
- Signal-to-noise ratio

$$SNR = \frac{\text{max amplitude}^2}{\text{noise amplitude}^2} = \frac{V_{PP}^2}{4kTR_N} C$$

- assuming only thermal noise



*SNR improves with the square of signal amplitude.
–Maximize signal swing*

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CMOS technology



- Basic element in microelectronics
 - Digital microelectronics
 - MOS device used as switch
 - Crude and simple understanding
 - Analog microelectronics
 - MOS device used as computational element
 - Current/voltage relationship of different terminals
 - Limitations
 - Loads
 - Design parameters
 - Exploring passive devices
 - Capacitors
 - Resistors

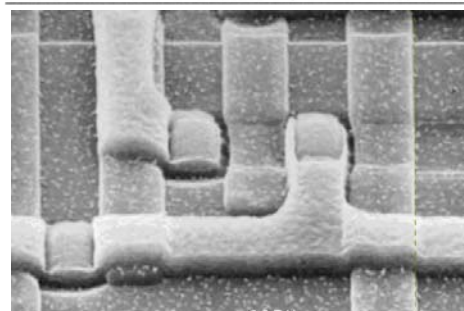
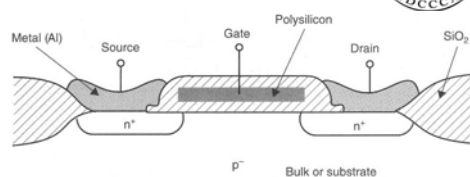
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CMOS technology



- Layered structure
 - Planar
 - Plates → capacitance
 - Wires → resistance
 - No “pure” device
 - Always added parasitics
 - Passive
 - » Resistance
 - » Capacitance
 - Active
 - » Diodes
 - » Bipolars
 - Mismatch



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Analog microelectronics



- Mastering devices and parasitics

- Explore continuous time behavior

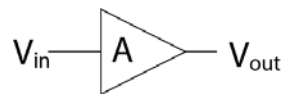
- Example: amplifier

- Output voltage A time larger than input voltage

$$V_{out} = A \cdot V_{in}$$

- Determine functional limits

- Input voltage range
 - Output voltage range
 - Maximum error
 - Frequency range



- Explore physics

- Available in CMOS microelectronics

- Developed for digital

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MOS transistor



- Most important element

- 3-4 terminal device

- Depletion region

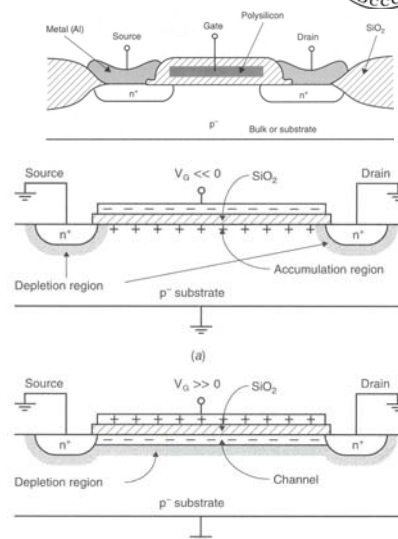
- Principal of operation

- Negative gate voltage
 - Accumulated channel
 - capacitor
 - Positive gate potential
 - channel between source and drain
 - Inversion
 - Gate voltage for making an inverted channel
 - Threshold voltage V_{th}

V_{in} - nMOS

V_{tp} - pMOS

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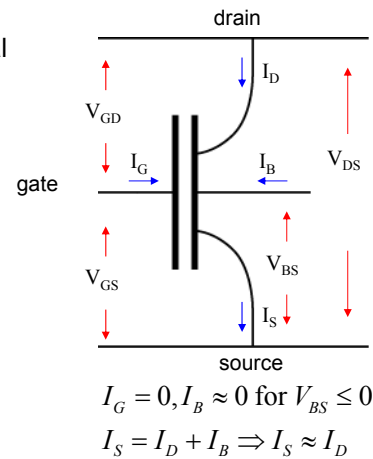
nMOS transistor



- Source referred potentials

- Source terminal:
The one closest to bulk potential
 - Substrate voltage for nMOS
- Primary characteristics
 - V_{GS} – Gate-source voltage
 - V_{DS} – Drain-source voltage
 - I_D – drain current
 - I_S – source current
- Secondary characteristics
 - V_{GD} – gate-drain voltage
 - V_{BS} – bulk-source voltage
 - I_B – bulk current
 - I_G – gate current

Source and drain
completely symmetric



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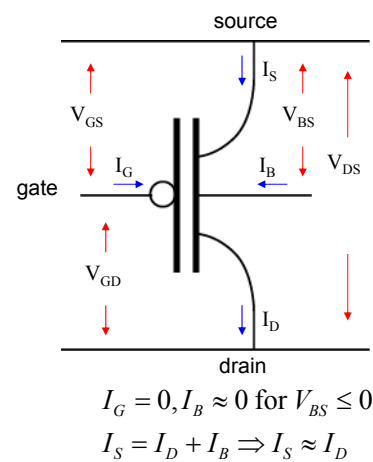
pMOS transistor



- Source referred potentials

- Source terminal:
The one closest to bulk potential
 - Well voltage for pMOS
- Primary characteristics
 - V_{GS} – Gate-source voltage
 - V_{DS} – Drain-source voltage
 - I_D – drain current
 - I_S – source current
- Secondary characteristics
 - V_{GD} – gate-drain voltage
 - V_{BS} – bulk-source voltage
 - I_B – bulk current
 - I_G – gate current

Source and drain
completely symmetric



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MOS transistor



- Definitions

- Threshold voltage
 - Reduced with
 - feature size
 - Supply voltage
 - V_{tn} - nMOS threshold voltage
 - Typical $\approx 0.7V$
 - V_{tp} - pMOS threshold voltage
 - Typical ≈ -0.9
- Effective gate voltage
- Channel charge density
 - K_{ox} - relative permittivity of silicon dioxide (≈ 3.9)
 - t_{ox} - thin oxide thickness
 - ϵ_0 - permittivity of free space

The gates voltage, for which the concentration of electrons under the gate is equal to the concentration of holes in the substrate far from the gate.

$$V_{eff} = V_{GS} - V_{tn(p)}$$

$$Q_{n(p)} = C_{ox}(V_{GS} - V_{tn(p)}) = C_{ox}V_{eff}$$

$$C_{ox} = \frac{K_{ox}\epsilon_0}{t_{ox}}$$

$$8.854 \times 10^{-12} F/m$$

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MOS transistor

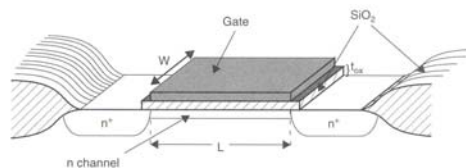


- Gate capacitance

$$C_{gs} = WLC_{ox}$$

$$Q_{T-n(p)} = WLC_{ox}(V_{GS} - V_{tn(p)})$$

$$= WLC_{ox}V_{eff}$$



- Linear channel current

- Impose drain-source voltage difference ($V_{DS} \neq 0$)
- Resistive, current increase with voltage difference

$$I_D = \mu_n Q_n \frac{W}{L} V_{DS}$$

$$\mu_n \approx 0.06 m^2/Vs - \text{mobility}$$

$$Q_n = \text{charge pr. unit area}$$

$$I_D = \mu_n \frac{W}{L} C_{ox} (V_{GS} - V_{tn}) V_{DS}$$

$$= \mu_n \frac{W}{L} C_{ox} V_{eff} V_{DS}$$

Only for V_{DS} close to zero
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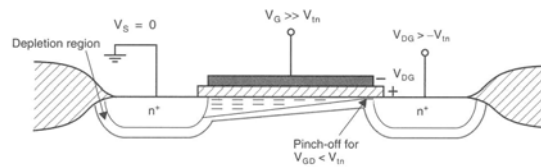
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MOS transistor



• Pinch-off

$$V_{DS} > V_{DS-sat} = V_{GS} - V_{th} = V_{eff}$$



– Channel current *independent* of drain-source voltage

- Active region
- MOS-transistor saturated
- Often desirable in analog circuits

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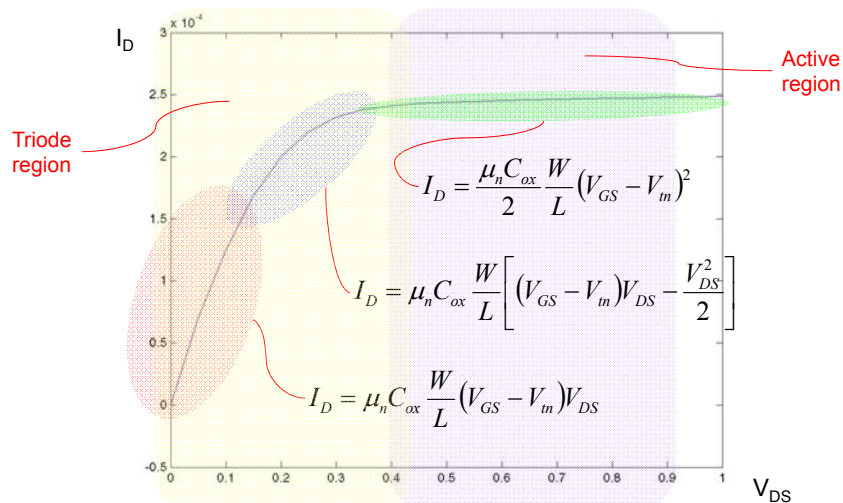
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MOS transistor



• Strong inversion behavior

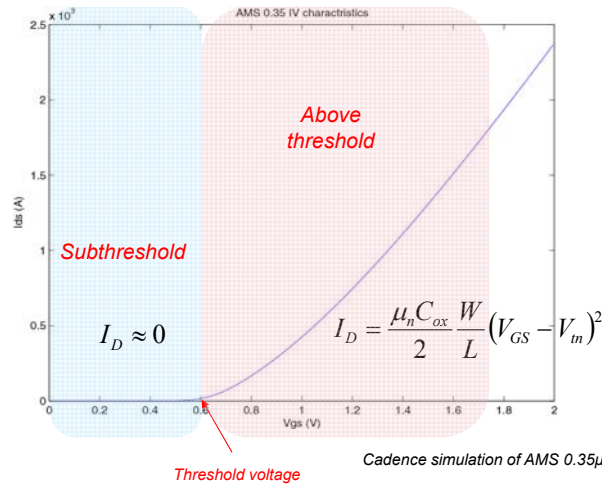
First order approximation



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MOS transistor

- Drain current vs. gate voltage

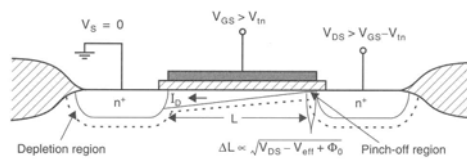
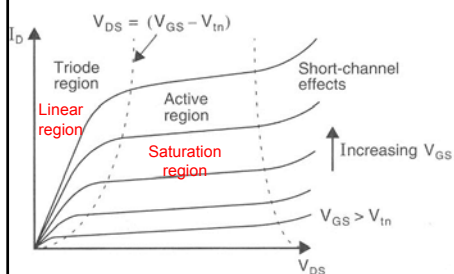


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MOS transistor deviations

- Channel shortening
 - Channel length modulation coefficient λ



$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{tn})^2 (1 + \lambda(V_{DS} - V_{eff}))$$

$$\lambda = \frac{k_{ds}}{2L\sqrt{V_{DS} - V_{eff} + \Phi_0}}$$

$$k_{ds} = \sqrt{\frac{2K_s \epsilon_0}{qN_A}}$$

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MOS transistor deviations



- Body effect
 - Back-gate effect, substrate effect
 - Current change as V_{SB} is different from zero
 - Modeled as change in threshold voltage

$$V_{th} = V_{th0} + \gamma \left(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|} \right)$$

- V_{th0} – zero biased threshold voltage

$$\gamma = \sqrt{\frac{2qN_A K_s \epsilon_0}{C_{ox}}}$$

ϕ_F - Fermi potential

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General purpose analytical model



- Models presented in book
 - Aimed for strong inversion
 - Above threshold
 - Unusable in moderate and weak inversion
 - Subthreshold
- EKV model (not in book)
 - Enz-Krummenacher-Vittoz model <http://legwww.epfl.ch/ekv/index.html>
 - Handles moderate and weak inversion
 - Continuous transition
 - Simple
 - Few parameters
 - (BSIM parameters >65)
 - Important for understanding micropower design

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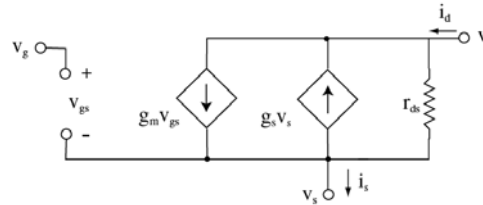
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MOS transistor models



- Active region

- Low frequency model
- Voltage controlled current source $g_m v_{gs}$
- Transconductance



$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{tn})^2 \Rightarrow$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{tn}) = \mu_n C_{ox} \frac{W}{L} V_{eff}$$

- Relation to drain current

$$V_{GS} - V_{tn} = \sqrt{\frac{2I_D}{\mu_n C_{ox} (W/L)}}$$

$$g_m = \mu_n C_{ox} \frac{W}{L} \sqrt{\frac{2I_D}{\mu_n C_{ox} (W/L)}} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \Rightarrow g_m \text{ proportional to } \sqrt{I_D}$$

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MOS transistor models



- Active region (cont.)

- Body effect

$$g_s = \frac{\partial I_D}{\partial V_{SB}} = \frac{\partial I_D}{\partial V_{tn}} \frac{\partial V_{tn}}{\partial V_{SB}} = \frac{g_m}{2\sqrt{V_{SB} + |2\phi_F|}}$$

- Ignored for

$$V_{SB} = 0$$

- Output impedance

$$\frac{1}{r_{ds}} = g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \lambda I_D$$

- Assuming λ is small

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MOSCAPs

- Gate capacitance

$$C_{gs} = \frac{2}{3} WLC_{ox}$$

- Fringing capacitances
 - Overlap

$$C_{ov} = WL_{ov}C_{ox} \Rightarrow$$

$$C_{gs} = WC_{ox} \left(\frac{2}{3}L + L_{ov} \right)$$

- Source-bulk capacitance (+channel cap when present)

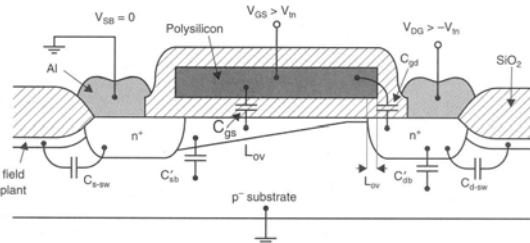
$$C'_{sb} = (A_s + A_{ch}) \frac{C_{j0}}{\sqrt{1 + V_{SB}/\Phi_0}}$$

A_s – source area

A_{ch} – channel area

C_{j0} – unit depletion capacitance at 0V

Φ_0 – build in junction potential



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MOSCAPs cont'd

- Drain-bulk capacitance

$$C'_{sb} = A_D \frac{C_{j0}}{\sqrt{1 + V_{DB}/\Phi_0}}$$

- Gate-drain overlap
 - Miller capacitance

$$C_{gd} = C_{ox}WL_{ov}$$

- Sidewall capacitances

$$C_{s-sw} = P_S \frac{C_{j-sw0}}{\sqrt{1 + V_{DB}/\Phi_0}}$$

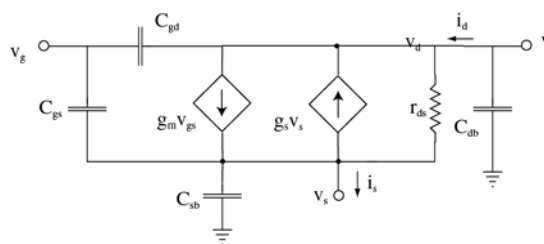
$$C_{D-sw} = P_D \frac{C_{j-sw0}}{\sqrt{1 + V_{SB}/\Phi_0}}$$

$P_{S(D)}$ – source (drain) perimeter

C_{j-sw0} – unit sidewall capacitance at 0V

- Bulk capacitances

$$C_{sb} = C'_{sb} + C_{s-sw} \quad C_{db} = C'_{db} + C_{d-sw}$$



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MOS transistor model



- Triode region

- Gain give as slope

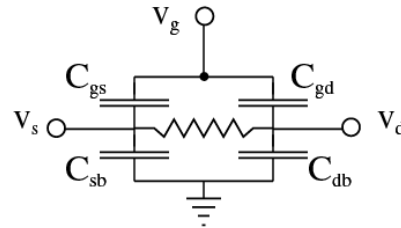
$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{tn}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- Output conductance

$$\frac{1}{r_{ds}} = g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{tn} - V_{DS})$$

- V_{DS} is small and sometimes dropped

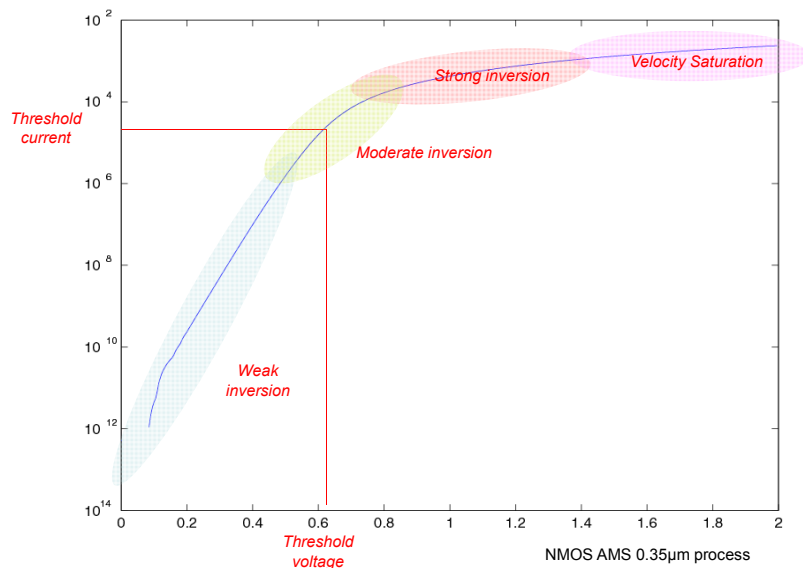
$$g_{ds} \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{tn})$$



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Channel inversion



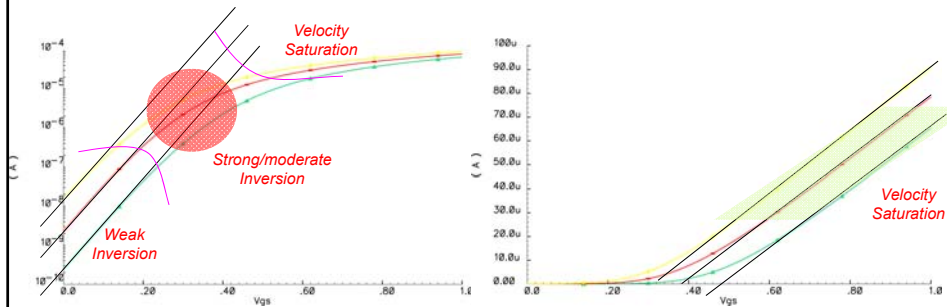
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Nanoelectronics



- 90nm technology (ST Microelectronics)
 - Minimum transistor simulated with CADENCE
 - Three different threshold voltages



ALMOST NO STRONG INVERSION LEFT!!!!

Velocity saturation in advanced technology squeeze strong inversion operation region

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Velocity saturation



- Active region
 - Strong inversion

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{tn})^2 \Rightarrow$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{tn}) = \mu_n C_{ox} \frac{W}{L} V_{eff}$$

- Velocity saturation
 - Short and small devices
 - Transconductance does not increase with smaller L!
- Maximum frequency

$$I_D = v_{sat} C_{ox} W (V_{GS} - V_{tn})$$

$$v_{sat} = 10^7 \text{ cm/s} \Rightarrow$$

$$g_m = v_{sat} C_{ox} W$$

Reduced from square to linear

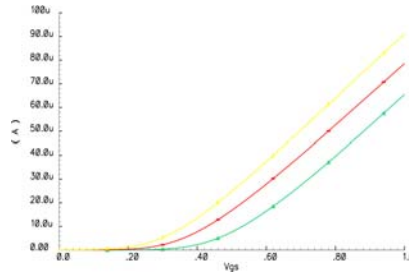
$$f_T = \frac{1}{2\pi} \frac{3}{2n} \frac{\mu}{L^2} (V_{GS} - V_{tn}) \rightarrow \frac{v_{sat}}{2\pi L}$$

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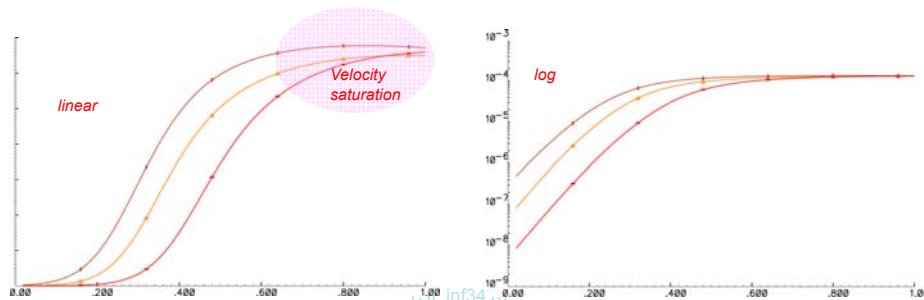
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- ST Microelectronics 90 nm

- Minimum transistor
- Drain current



- Transconductance



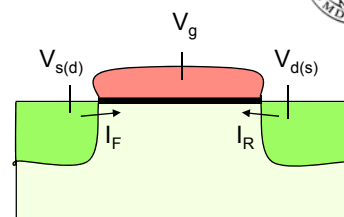
The EKV MOS model

- 3 parameters (simplest version)

- V_{T0}
Zero biased threshold voltage

- $\beta = \mu C_{ox} \frac{W}{L}$
Gain factor

- n
Slope factor $n = [1 \dots 2]$



All potentials referred to bulk

- Specific current

$$I_S = 2n\beta U_T^2 \quad U_T = \frac{kT}{q} \approx 26mV \text{ at room temperature}$$

- Channel current

$$I_{DS} = I_F - I_R = I_S(i_F - i_R) \quad i_{F(R)} = \ln^2 \left[1 + \exp \left(\frac{V_g - V_{T0} - nV_{S(D)}}{2nU_T} \right) \right]$$

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EKV MOS model

- Weak inversion

– If $V_g < V_{T0} - nV_{S(D)}$

$$i_{F(R)} \approx \exp\left(\frac{V_g - V_{T0} - nV_{S(D)}}{nU_T}\right)$$

$$y = \ln^2(1 + e^{x/2})$$

$$f = \begin{cases} \left(\frac{x}{2}\right)^2 & \text{for } x \gg 0 \\ e^x & \text{for } x \ll 0 \end{cases}$$

- Strong inversion

– If $V_g > V_{T0} - nV_{S(D)}$

$$I_{F(R)} \approx \frac{\beta}{2n} (V_g - V_{T0} - nV_{S(D)})^2$$

A continuous smoothing function proposed by Oguey (swiss math-guy)

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MOS saturation

- Weak inversion expressions

$$I_D = I_F - I_R = I_S e^{\frac{V_G - V_{T0}}{nU_T}} \left(e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}} \right)$$

$$V_D \gg 0 \Rightarrow I_R \rightarrow 0$$

$$I_D = I_S e^{\frac{V_G - V_{T0}}{nU_T}} \left(e^{\frac{-V_S}{U_T}} \right) = I_S e^{\frac{V_G - V_{T0} - nV_S}{nU_T}}$$

$$V_g < V_{T0} - nV_{S(D)}$$

$$V_{DS} > V_{eff} = 4.5 U_T$$

$$V_S < V_g - V_{T0}$$

$$V_D > V_g - V_{T0}$$

– Transconductance

$$I_D \approx I_S \exp\left[\frac{V_G - V_{T0} - nV_S}{nU_T}\right], \text{ let } I_{D0} = I_S \exp\left[\frac{-V_{T0}}{nU_T}\right] \text{ will give}$$

$$I_D = I_{D0} \exp\left[\frac{V_G - nV_S}{nU_T}\right], V_S = 0 \Rightarrow I_D = I_{D0} \exp\left[\frac{V_G}{nU_T}\right] \Rightarrow$$

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{1}{nU_T} I_D$$

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MOS saturation

- Strong inversion

$$I_D = \frac{\beta}{2n} (V_g - V_{T0} - nV_{S(D)})^2$$

$$V_g > V_{T0} - nV_{S(D)}$$

$$V_S < V_g - V_{T0}$$

$$V_D > V_g - V_{T0}$$

- Transconductance

$$I_D = \frac{\beta}{2n} (V_g - V_{T0} - nV_{S(D)})^2$$

$$g_m = \frac{\partial I_D}{\partial V_g} = \frac{\beta}{n} (V_g - V_{T0} - nV_{S(D)})$$

$$= \sqrt{\frac{2\beta}{n}} I_D$$

$$= \frac{2I_D}{V_g - V_{T0} - nV_{S(D)}}$$

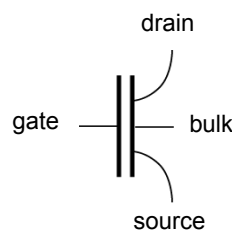
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Body effect

- MOS-transistor
 - 4-terminal device
 - Back-gate



$$I_{ds} = I_{D0} \exp \left[\frac{V_{gb} - nV_{sb}}{nU_T} \right]$$

$$V_{gb} = V_{gs} + V_{sb}$$

$$I_{ds} = I_{D0} \exp \left[\frac{V_{gs} + V_{sb} - nV_{sb}}{nU_T} \right] = I_{D0} \exp \left[\frac{V_{gs} - (n-1)V_{sb}}{nU_T} \right]$$

Body effect natural part of model

• n (slope factor) denotes gate efficiency

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Technology implications



- Finer pitch - submicron
 - Lower supply voltage
 - Reduced headroom
 - Less power
- Analog circuit design
 - Often mixed with digital
 - Limited SNR
 - Added noise
- *Weak inversion unavoidable*
 - *Even for digital circuits*
 - *No strong inversion left!*

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Example: CD4007



- Lab transistors
 - Datasheet → [MC14007.pdf](#)
 - Exact specifications not available
 - Estimated parameters nMOS:
 - $U_t=0.026$
 - $V_{T0}=1.6$
 - $\mu_n=0.067$
 - $\epsilon_0=8.854e-12$
 - $K_{ox}=3.9$
 - $L=10$
 - $W=350$
 - $t_{ox}=350e-10$ (high voltage indicated thick dioxide)

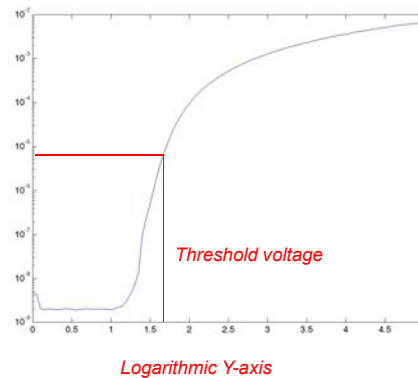
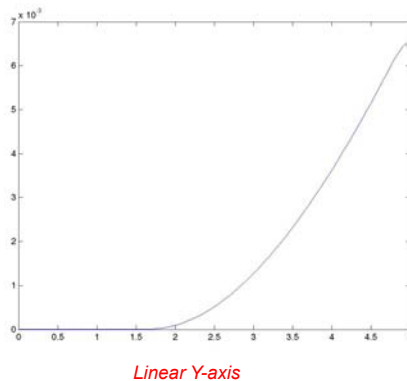
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Measured nMOS



- CD4007 nMOS transistor
- drain-current ↔ gate-voltage
- Active region
- $V_{ds} = 5V$



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Keypoints



- The source terminal of nMOS → lowest voltage
- The source terminal of pMOS → highest voltage
- MOS transistors are close to linear for $V_{ds} \ll V_{eff}$ (triode region)
- MOS transistors with $V_{ds} > V_{eff}$ have square-law current vs. voltage
- Small signal r_{ds} proportional to L/I_{ds}
- For high gain, transistors should be long and biased with low V_{eff}
- Transistors are operation with exponential current vs voltage relationship for low gate voltages. Current is flowing even for $V_{ds} = 0$
- For large V_{eff} transistor go into velocity saturation with linear current-voltage relation
- Transconductance is highest in weak inversion (linear), degrading to square root in strong inversion, fading to '1' in velocity saturation

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Layout

- Chapter 2: self-study or assumed known
- Keypoints:
 - ALL transistors are different!
 - Even with exactly the same layout, next to each other on the same die
 - Systematics process variation
 - Random production variations
 - Increase with reduced device area
 - Assume 20% random variations in modern processes for small devices
 - Other effects
 - Temperature, aging