

Silicon-on-insulator (SOI) Technology

Manufacture and Applications

Edited by Oleg Kononchuk and Bich-yen Nguyen

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Bich-Yen Nguyen



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After starting as a niche market, silicon-on-insulator (SOI) complementary metal oxide semiconductor (CMOS) technology has now reached maturity. The technology first developed in the early 1980s with rad-hard (military) and power applications. Wider SOI adoption began with high-performance computing applications within the integrated device manufacturer (IDM) community in the late 1990s. Currently SOI technology is challenging traditional CMOS technology based on bulk silicon wafers in all sectors of the market, including RF, analog, general purpose and ultra low power computing, photonics, memory, and MEMS. As an example, more than 60% of mobile devices and more than 80% of game consoles produced in 2012 have SOI chips. A complete CMOS ecosystem has developed during the last few years. It is based on a multisource wafer supply chain where three major SOI wafer companies (SOITEC, SEH, SunEdison) have a total capacity of 2.5 million wafers per year (which could easily double within 1–2 years). The ecosystem includes foundries with SOI processing (IBM, UMC, Global Foundry, ST Microelectronics), as well as providers of intellectual property (IP) core libraries (ARM, IBM) as well as electronic design automation (EDA) tools (Synopsys, Cadence, Mentor Graphics). The ITRS roadmap increasing adoption of SOI technology in the IT industry and provides SOI-specific roadmaps for different applications. Most of the major CMOS manufacturers have included SOI solutions in their R&D programs for future products.

What are the advantages of SOI? We can briefly summarize the major advantages as:

- SOI provides significant performance gains, both in speed and power, compared to corresponding bulk solutions;
- SOI allows better scaling, resulting in a smaller chip area;
- SOI simplifies the CMOS process; and
- SOI provides an easy way to co-integrate different materials at the wafer level.

What is slowing down the wider adoption of SOI by the industry? In 2008 the Global Semiconductor Alliance (GSA) and the SOI Industry Consortium conducted an online survey to study perceptions of SOI technology in the

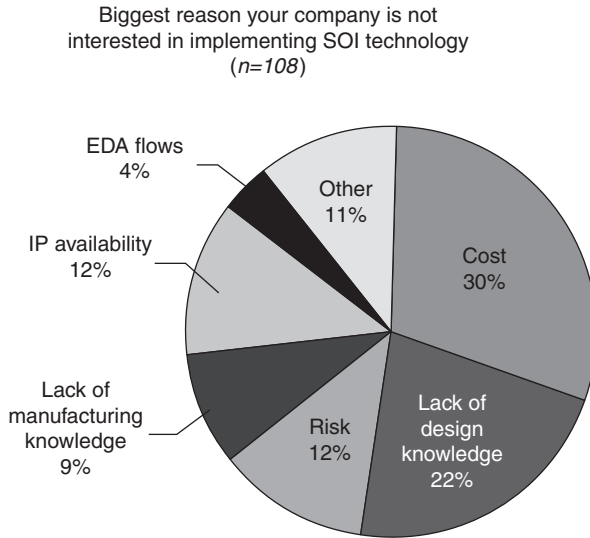


Fig. 1 Results of semiconductor industry survey (GSA report 2008 published on collaboration with the SOI Industry Consortium http://www.soiconsortium.org/pdf/2008_SOI_Report_24June.pdf).

industry (Fig. 1). The cost of SOI wafers was named as the primary reason restricting SOI growth followed by lack of specific SOI design knowledge.

However, these problems are being addressed. Historically the price of SOI wafers has been approximately five times higher than that of silicon bulk wafers. However, high volume manufacturing has reduced prices of SOI wafers significantly. In addition, the cost of the SOI wafer is a small proportion of the total cost of a processed and packaged device. The potential of SOI to simplify the manufacturing process offsets the higher substrate cost.

This book is intended to give an overview of the latest developments of SOI CMOS technology. It has two parts. The first deals with SOI wafer manufacturing, characterization and SOI device physics. The second part covers different SOI applications. It covers both more established technologies, like partially depleted SOI technology, as well as those introduced more recently, like fully depleted planar SOI technology, FinFETs, RF, photonic, MEMS, and ultralow power applications. Both transistor level and circuit level solutions are covered. We have deliberately limited the scope of the book to solutions for 32–14 nm technology nodes as well as applications where SOI technology is mature enough to reach volume production.

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O. Kononchuk and B-Y. Nguyen

Part I

Silicon-on-insulator (SOI) materials
and manufacture

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Materials and manufacturing techniques for silicon-on-insulator (SOI) wafer technology

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Abstract: This chapter reviews various processes for manufacturing SOI wafers. There is a specific focus on Separation by IMplantation of OXYgen (SIMOX) and on technologies based on direct bonding (bonded silicon-on-insulator (BSOI), epitaxial layer transfer process (Eltran[®]), Smart Cut[™]). For the latter, the physical and chemical properties of both starting wafers and SOI structures are mainly discussed. These analyses help in developing models for direct bonding and splitting. Recent fabrication process improvements and trends towards innovative engineered structures are also described.

Key words: SOI, ion implantation, direct bonding, thinning down processes, wafer manufacturing.

1.1 Introduction

SOI structures consist of a top single-crystal silicon layer, either separated from the bulk substrate by an insulating layer (for instance SiO₂) or directly supported by an insulating substrate.¹⁻⁵

Technologies based on the use of a buried oxide layer, SiO₂, as an insulator in SOI wafers have been widely developed in microelectronics because of their advantages compared to silicon bulk substrates. Among other benefits, SOI wafers allow:

- lower parasitic device capacitances due to isolation from the bulk silicon substrate, which results in lower power consumption
- higher speed devices, avoiding latchup effects due to a complete isolation of the n- and p-well devices
- radiation-hardening for sensitive applications.

SOI wafers are used in microelectronics, the fabrication of microelectro-mechanical systems (MEMS), photonics and biotechnological chips. As an example, the mechanical properties of single-crystal Si films are superior to

those of polycrystalline films. This makes them a better choice for the fabrication of MEMS components. The buried oxide layers in SOI structures also facilitate fabrication of MEMS devices. In photonic applications, the high contrast of refractive indices between Si and SiO₂ in SOI wafers allows efficient photon confinement in small waveguides with sharp bends.

From an industrial point of view, SOI substrates are compatible with most conventional device fabrication processes in microelectronics. This means that most SOI-based processes may be carried out in an existing factory built for conventional Si device fabrication. Devices made using SOI structures differ from conventional devices using bulk silicon. SOI structures are built above electrical insulators, typically using silicon dioxide, silicon nitride, diamond or sapphire.⁶ Such electrical insulators may be either buried layers or bulk wafers. The choice of insulator material depends largely on the application. As an example, one might choose:

- silicon dioxide to obtain decreased short channel effects in microelectronics devices;
- diamond to allow thermal dissipation if needed to deal with the self-heating effect; or
- sapphire for high-performance radio frequency applications.

1.2 SOI wafer fabrication technologies: an overview

This section provides an overview of the diverse technologies developed to fabricate SOI wafers. It will concentrate on SIMOX, BSOI, Eltran[®] and Smart Cut[™] technologies, which have allowed industrial-volume production of SOI structures, including buried insulating SiO₂ layers.

Since the 1970s, several novel techniques for fabricating SOI wafers have been explored and developed.⁵ These have included silicon epitaxial growth onto single-crystal substrates such as sapphire,⁷ zirconia⁸ or seeded silicon wafers. Silicon-on-sapphire (SOS) structures are still made by this technique, although the quality of the silicon layers remains one of the main concerns. Silicon epitaxial lateral overgrowth (ELO) techniques⁹ were developed as alternatives, in which growth occurs from holes in the oxide layer of an oxidized Si wafer and expands laterally over that layer. These approaches were limited because they did not allow very large areas of overgrowth.

At the same time, techniques were explored that were based on the rapid melting by laser or hot wire heating of a polysilicon layer deposited onto SiO₂ layers followed by controlled crystallization.¹⁰⁻¹² These techniques were unsuccessful because of the poor quality of the crystallized silicon.

In the early 1980s, the full isolation with porous oxidized silicon (FIPOS) method was developed. This involved the oxidation of porous regions below non-porous islands of Si, in order to form local SOI.¹³⁻¹⁵ However, the

wafer patterning required was a problem, and FIPOS was abandoned when SIMOX and direct bonding processes became available.

SIMOX technologies emerged at the end of the 1970s.^{16,17} These were strongly motivated by, for instance, the need to make microelectronics devices with sufficient radiation hardness for military and space applications. SIMOX processes can induce isolated buried oxide (BOX) layers across the full area of Si wafers. The buried oxide layers are formed through oxygen implantation in silicon wafers and high-temperature annealing.¹⁸ SIMOX processes can make top Si and BOX layers of various thicknesses for SOI wafers that are fully compatible with most of the bulk silicon device processes. This technology has reached a mature level of development, which has allowed industrial SOI production.^{19–21} SIMOX technology will be described in more detail below.

Direct wafer bonding is the basis of three other successful processes for the fabrication of SOI structures. It mainly involves transferring a single-crystal silicon layer from a ‘donor’ wafer to a final handling wafer. The three processes are:

- Bonded silicon-on-insulator (BSOI) technology: this covers several processes developed in the 1980s, based on direct bonding and the thinning down of one of the two wafers. BSOI structures have been used widely in microelectronics, microtechnologies, microelectromechanical structures (MEMS), biotechnologies and optronics.
- Epitaxial layer transfer process (Eltran[®]): this alternative technique for SOI fabrication was developed at Canon.^{22,23} It uses the mechanical (weak) and structural (single-crystal) properties of porous Si layers and requires both epitaxy and direct wafer bonding technologies. Epitaxial layers are used in order to obtain SOI layers with low threading-defect densities, which is one of the key advantages of the Eltran[®] process.^{22,23}
- Smart Cut[™] technology: this third approach, based on ion implantation, direct bonding and splitting, was proposed by Bruel²⁴ and has been promoted since 1991. It was jointly developed by CEA and SOITEC and is now used by SOITEC and other Si wafer manufacturing companies in high-volume production of bonded SOI structures.

These three technologies, based on direct bonding, are described in more detail in the next section. It might also be noted that novel tools and methods of metrology have been specifically developed to characterize the bonding quality and strength and the physical and structural properties of top silicon and buried insulating layers in SOI structures.

1.3 SOI volume-fabrication process

Only a few methods for SOI wafer fabrication have become mature enough to allow industrial-scale production. Among these, SIMOX and direct

bonding technologies (BSOI, Eltran[®], Smart Cut[™]) are well suited to obtaining thin, single-crystal top silicon layers.

1.3.1 Separation by IMplantation of OXYgen (SIMOX) technology

The first of these methods to be developed was based on a Separation by IMplantation of OXYgen (SIMOX) process. It consists of the direct synthesis of a buried SiO₂ oxide layer by oxygen ion beam implantation and very high-temperature annealing ($T > 1300^{\circ}\text{C}$).

Watanabe *et al.* pioneered attempts to form BOX layers by oxygen implantation in silicon wafers.¹⁶ Later, Izumi *et al.* demonstrated that device-quality SIMOX SOI structures were attainable in which the buried oxide was so formed.¹⁷ In the early generations of SIMOX wafers, oxygen implantation at 200 keV was necessary to obtain SOI wafers with a 200 nm-thick Si top layer above a 400 nm-thick BOX layer. Fluences of about 2×10^{18} ions cm^{-2} were required to achieve a continuous stoichiometric BOX layer, but such a high dose led to a high density of defects in the crystalline lattice. To overcome this issue, a method of annealing at 600°C during oxygen ion implantation was developed which preserved single-crystal silicon near the wafer surface, where the ion energy was highest and thus displacement damage was least.^{18,25} Annealing at very high temperatures (typically above 1300°C)¹⁸ was shown to be necessary after implantation in order to form the BOX layer, through oxygen ions reacting with Si, and in order to repair the crystal damage in the Si layer above and in the Si substrate below the BOX layer.

In SIMOX technologies, wafer cost strongly depends upon oxygen ion implant dose. A fluence of about 2×10^{18} ions cm^{-2} leads to a high wafer cost, so several approaches were explored to reduce wafer cost by reducing this ion fluence. For instance, reducing the fluence to about 4×10^{17} ions cm^{-2} and modifying the implantation and annealing conditions allowed a high-quality continuous planar BOX layer to be obtained with a thickness reduced to about 80 nm.^{19,26} It is worth noting that a lower implantation dose also reduces implantation damage density and thus a 'low dose SIMOX process' leads to fewer defects in the final annealed SOI wafers.

Several improvements have been introduced to obtain high-quality SIMOX SOI wafers. One concern with thinner BOX layers is that there might be a higher density of silicon micro-pipes, allowing electrical conduction between the Si top layer and the Si substrate. An additional 1350°C oxidation of SOI wafers, referred as ITOX, has therefore been developed which leads to both an oxidation of the top Si layer and to a complementary oxidation at the buried top Si–BOX interface, because of oxygen diffusion through the Si layer.²⁷

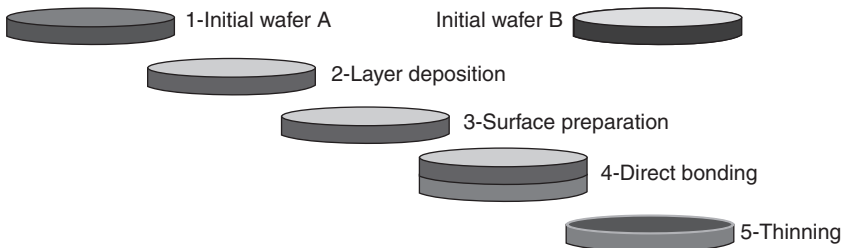
Such additional treatment improves BOX stoichiometry and oxidizes silicon micro-pipes. It also slightly increases BOX layer thickness.

1.3.2 BSOI and BESOI processes

In the 1980s, several processes were developed for the direct bonding of silicon wafers prepared with hydrophilic oxide surfaces (native, chemical, deposited or thermally grown oxides) in order to fabricate silicon-on-insulator (SOI) structures.^{24–26} High-temperature annealing processes were tuned to strengthen adhesion after the direct bonding.

Figure 1.1 shows a typical scheme for a SOI fabrication process consisting of silicon surface preparation before direct bonding of the two silicon wafers. The process starts with conditioning and cleaning of the wafer surfaces. An oxide layer is either thermally grown or deposited on at least one wafer (wafer A and/or wafer B). This will become the BOX layer. Smoothing and additional cleaning can be performed to prepare the surfaces for direct bonding. Then the direct bonding process is induced and the bonded structures are annealed in order to strengthen the stack. Finally, thinning can be performed by, for example, grinding,^{26–28} chemical processes (wet or dry etching) or lift-off techniques.²⁹ Within a few years of these techniques being introduced, SOI layers were comparable in quality to single-crystal bulk silicon wafers.

Specific techniques have been developed to achieve very thin layers through bonding and thinning processes. First developed in order to obtain SOI wafers with very thin top silicon layers, these techniques are referred to as bond and etch-back silicon-on-insulator processes (BESOI).³⁰ A thin sacrificial layer, for example, a SiGe layer, is grown epitaxially on the initial ‘donor’ wafer, for example, wafer A in Fig. 1.1. A thin silicon layer is



1.1 Typical steps used in BSOI process: (1) initial wafer preparation; (2) and (3) for oxide layer formation, smoothing and surface cleaning; (4) direct bonding of the two Si wafers with an oxide layer between them and (5) thinning down of one wafer to obtain a silicon layer on insulator.

then grown by epitaxy on the sacrificial layer prior to direct bonding. After thermal treatment to strengthen the bonding, the initial donor substrate is removed down to the sacrificial layer, which is then also removed by some method that selects strongly between the sacrificial layer and the thin layer to be transferred, for instance chemical etching. SOI wafers produced by either BSOI or BESOI processes can now be manufactured with single-crystal quality in large diameters and high, industrial-scale volumes.

1.3.3 Eltran[®] process

The epitaxial layer transfer process (Eltran[®]) was developed at Canon for SOI fabrication.^{22,23} It uses both the mechanical (weak) and structural (single-crystal) properties of porous Si layers and requires epitaxy and direct wafer bonding technologies. Growth and surface preparation of bulk Si wafers for microelectronics applications have been improving for several decades. It is now possible to obtain very high-quality wafers in large diameters (routinely 300 mm). However, defects remain, even if in very low densities. For instance, small crystal voids referred to as crystal originated particles (COPs) can be generated during the pulling of the silicon in the bulk growth process, and small pits can be created on the wafer surface during its conditioning and preparation. The sizes of such defects are typically about 0.1 μm .

When the thickness of the top silicon layer is reduced to 0.1 μm , defects in the initial bulk wafer may induce threading void defects through the active SOI layer. Such threading defects are referred to as HF defects because Si voids allow BOX etching by hydrofluoric acid (HF) penetration. These can be killer defects. For advanced SOI device applications, HF defect densities need to be below 0.1 cm^{-2} . Because COPs or pits are not propagated through epitaxially grown layers, one way to obtain SOI layers with low threading-defect densities is to use epitaxial layers. This is one of the key points in the epitaxial layer transfer process.^{22,23}

The main steps of the Eltran[®] process for epitaxial SOI wafer fabrication are as follows:^{22,23}

- Porous Si layers are first formed in the surface of initial ‘donor’ wafers.
- High-quality epitaxial layers – future active SOI layers – are then grown on top of these porous layers.
- The epitaxial layers are partially oxidized by thermal oxidation to form the future BOX layers, which makes possible a low defect density and high-quality SOI–BOX interface.
- Donor wafers are bonded to the final handling Si wafers.
- Separation is induced through the porous Si layers by mechanical stress.

- The remaining porous Si layers are removed from the SOI wafers, which are then smoothed by hydrogen annealing to produce the epitaxial SOI wafers. The remaining donor wafers can be reclaimed and reused.

The thickness of Eltran[®] SOI layers is highly controllable, ranging from a few nanometers, for instance for advanced MOSFET designs, to several micrometers, for instance for MEMS applications, mainly by tuning the growth conditions. BOX layer thickness can also be controlled over a wide range, whatever the SOI layer thickness.

Besides the epitaxial layer thickness control, a process is required that smoothes the surface of thin SOI layers without inducing unacceptable variation in their thickness.³¹ A hydrogen annealing batch process has been developed specifically to obtain atomically flat surfaces while consuming as little as 1 nm thickness of SOI.³² This hydrogen annealing is another key step in the Eltran[®] process, which means that uniformity in thickness is much greater than can be obtained by conventional chemical mechanical polishing (CMP) processes.

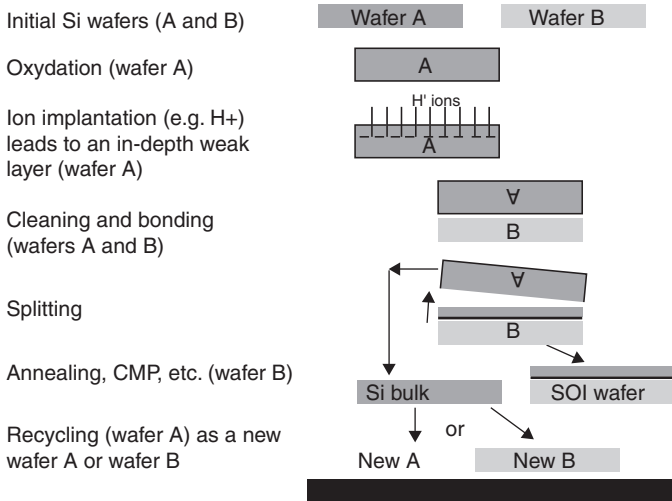
In the past decade, SOI wafer quality and process capabilities have been greatly improved. They were very promising both for advanced integrated devices and MEMS applications, and to meet the growing demand, Canon invested two billion yen in the early 2000s in order to increase its manufacturing capacity fivefold, and its output reached 10 000 wafers per month.³² One may note that this level of SOI wafer production seems to have fallen short of the targeted volume, which could be related to difficulties in satisfying application specifications or to production capacity and cost efficiency. At present, the industrial production of SOI wafers by Eltran[®] process has been discontinued.

1.3.4 Smart Cut[™] technology

Smart Cut[™] technology is a technique which has been developed since 1993. It is based on the direct bonding of two wafers, one of which has first been implanted by light gas ions, with splitting induced in the implanted zone.^{33,37}

Implantation of ions, such as hydrogen or helium, leads to the formation of a weakened buried zone, located at the mean depth of ion penetration. After the implanted wafer is bonded to a second wafer, splitting may occur, in which a thin layer is transferred from the implanted wafer onto the second wafer. Comparable scenarios occur when the second wafer is replaced by a thick layer stiff enough to allow splitting.

Smart Cut[™] technology was first developed in order to obtain SOI materials. It is now mature enough to allow industrial-volume production of high-quality SOI wafers. The Smart Cut[™] process for producing SOI wafers consists of the following steps (Fig. 1.2):^{4,37,38}



1.2 Smart Cut™ process as described to produce SOI wafers.

- A first Si wafer is thermally oxidized.
- Ions (H, He, etc.) are implanted in this first oxidized wafer to induce a buried weak zone.
- The first implanted wafer is then cleaned and directly bonded to a second support wafer.
- Splitting is induced in the weakened zone, transferring a thin layer from the first implanted wafer to the second support wafer.
- A final stage of treatment removes the roughness left at the surfaces after splitting, leading to the final SOI structure. This allows the remaining part of the donor wafer to be reclaimed.

There are several advantages to the Smart Cut™ process, such as good homogeneity in thickness and the high quality of the transferred layer, also the remainder of the first wafer may be reused as a new first or second wafer. Additionally, it is a very generic and adaptable process because it can be used to obtain a wide variety of single-crystal layers on top of many different supports. Research continues in numerous studies to develop innovative bonded structures and to better understand the basic mechanisms that are involved in bonding, implanting and splitting. These basic mechanisms are illustrated below for the case of SOI structures.

1.4 SOI wafer structures and characterization

The specific characteristics of SOI structures are determined by several parameters, such as the wide range of Si or BOX layer thickness, multiple Si–SiO₂ interfaces, specific film defects and stress effects. Depending

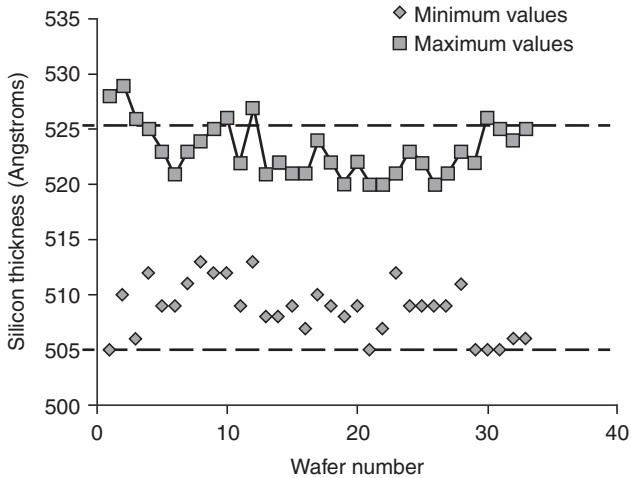
on the manufacturing process, SOI layer thicknesses may range from several micrometers, as for MEMS applications, to a few nanometers, as for advanced CMOS. It is worth noting that whatever the SOI layer thickness and process (except for SIMOX processes), BOX layer thickness can also be tuned over a wide range, from a few nanometers to several micrometers.

The manufacturing processes generally have to include final surface preparation steps in order to obtain smoothed top SOI layers. Usually this involves a very slight thinning of top SOI layers, which must not, however, reduce the uniformity of thickness of those layers. During conventional CMP processes, the thickness of removed material is noticeable, for example, a few tens of nanometers. This may lead to a marked non-uniformity of thickness, depending on the manufacturing process. By contrast, in the Eltran[®] process, specific hydrogen annealing has been developed that allows atomically flat surfaces to be obtained with a thinning of the top SOI layers limited to less than 1 nm.³¹

Whatever the manufacturing process used, surface microroughness values below 0.15 nm rms are routinely obtained, as checked by atomic force microscopy (AFM) scanning on 1 μm^2 areas. In addition, specifically designed thinning processes have been developed for local correction of variations in SOI layer thickness. For instance, the dry chemical planarization (DCP) process proposed by the Japanese Company SpeedFam³⁹ is a non-contact and non-damaging localized method based on dry chemical reactions in downstream plasmas. It achieves excellent uniformity of thickness with increased throughput.

Because of the ever-increasing demand for larger diameter wafers, SOI structures have regularly been expanded in size with the aim of meeting or exceeding specifications. During the 1990s, production supplied 100, 150 and 200 mm SOI wafers. Wafers of 300 mm are now routinely manufactured in volume and production of 450 mm wafers has been demonstrated successfully using Smart CutTM technology. For instance, in the case of 300 mm SOI wafers (e.g. with a 50 nm Si layer and 150 nm BOX layer), Smart CutTM technology enables on-wafer thickness uniformity with ± 1 nm overall distribution, on all wafers and at all sites (Fig. 1.3).⁴⁰ Recently,⁴¹ Si layer thickness control ± 0.5 nm has been demonstrated in high volume production for leading edge fully depleted SOI technology. It is worth noting that the metrology has had to be refined to achieve repeatability and accuracy at the level of a tenth of a nanometer.

The characterization of SOI structures requires traditional, tuned and innovative techniques. Physical–chemical characterization techniques such as ellipsometry, X-ray diffraction and reflection, Rutherford's backscattering spectrometry (RBS), secondary ion mass spectroscopy (SIMS), Fourier transform infrared spectroscopy (FTIR), transmission electron microscopy (TEM) and atomic force microscopy (AFM) are all well suited and are routinely used for in- and off-line production characterization. In addition,



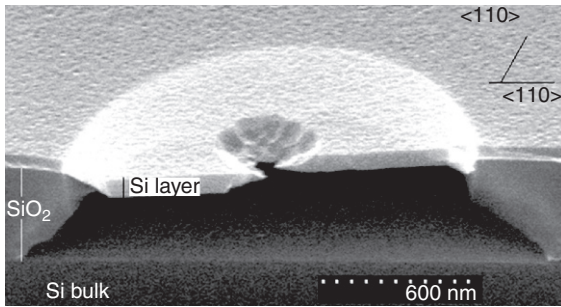
1.3 300 mm SOI thickness map (51.5 nm Si layer/145 nm BOX layer, 3 mm edge exclusion). It shows ± 1 nm overall Si layer thickness control for all sites on all wafers.

because the integrity of both the Si and SiO₂ films is a key requirement for CMOS applications, novel characterization techniques have been developed specifically for SOI structures.

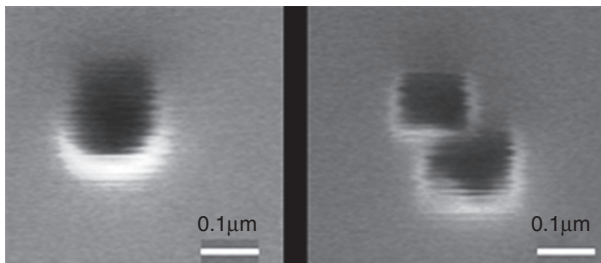
The top silicon layer has to be checked for defects in or through its full thickness. Defects can result, for instance, from dislocations and generation of stacking faults, which is strongly dependent on the fabrication process and high-temperature treatments. In the SIMOX process, annealing at very high temperature ($T > 1300^{\circ}\text{C}$), in order to form the BOX layer, can induce defects, as can badly tuned thermal treatments needed for oxidation, strengthening of bonding or thinning of the top silicon layer in bonding processes.

To investigate Si top layer qualities, a diluted Secco etch technique ($\text{K}_2\text{Cr}_2\text{O}_7:\text{H}_2\text{O}:\text{HF}$) is often used.⁴² Stress induced by defects in the Si network facilitates preferential etching around the defects, leading to etch pits. The etch pits enlarge as the etching time increases, threading through the remaining thickness of the Si layer. Figure 1.4 shows an example of a defect revealed by the Secco etch process. In this case, the sides of the threading pit exhibit crystalline orientation.⁴² Subsequent HF etching through the pit has led to underlying decoration in the buried oxide. Such pit decorations allow optical measurements of ‘Secco defect’ density on the whole wafer.

Defects in the Si top layer may also be voids created by condensation of Si vacancies (Fig. 1.5). The typical sizes of such voids are a few tenths of a micrometer and they may thus thread through the whole thickness of the Si layer. Again, single HF etching through such threading voids creates



1.4 Secco defects observed by SEM in SOI structure. Remaining silicon thickness is about 50 nm after Secco etching. (Source: Reprinted with permission from *Electrochemical Society Proceedings* 99-3, 173. Copyright (1999), The Electrochemical Society.)

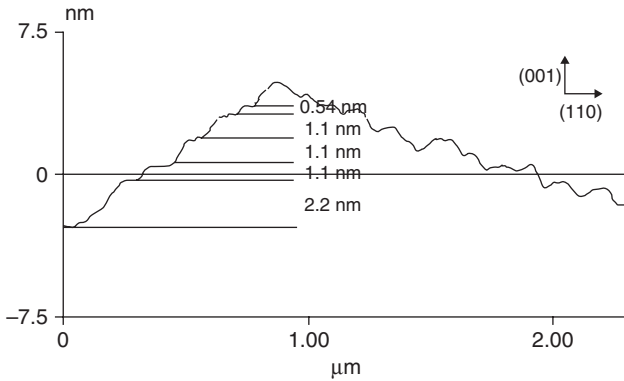


1.5 Single and twinned void defects observed by SEM. (Source: Reprinted with permission from *Electrochemical Society Proceedings* 99-3, 173. Copyright (1999), The Electrochemical Society.)

decoration in the underlying buried oxide. Measurement of these ‘HF defects’ is required because they have detrimental effect for many applications.

In order to locate defects and evaluate their density more accurately, surface-quality inspection systems can be used that scan HF decorated wafers over their whole surface, such as the Surfscan® Surface Profilometer- Dual Laser Scan (SP-DLS) tools from KLA-Tencor Corp.⁴³ Subsequent observations (e.g. by SEM) can then assess whether detected defects thread through the Si top layers. Improvements in fabrication processes have reduced the densities of HF and Secco defects to levels that are acceptable for applications. For instance, 300 mm SOI wafers with HF decorated defect densities lower than 0.05 cm^{-2} have been obtained by Smart Cut™ technology.⁴⁰

In addition to the crystal quality of the Si and BOX layers, the quality of the SOI interface also needs to be characterized. For instance, Guilhalmenc *et al.* showed by AFM observations that the top Si layer–BOX interface of low-dose SIMOX (100) wafers has a rough, square-mosaic morphology after annealing at 1320°C for 6 h.⁴⁴ This morphology results from the combination



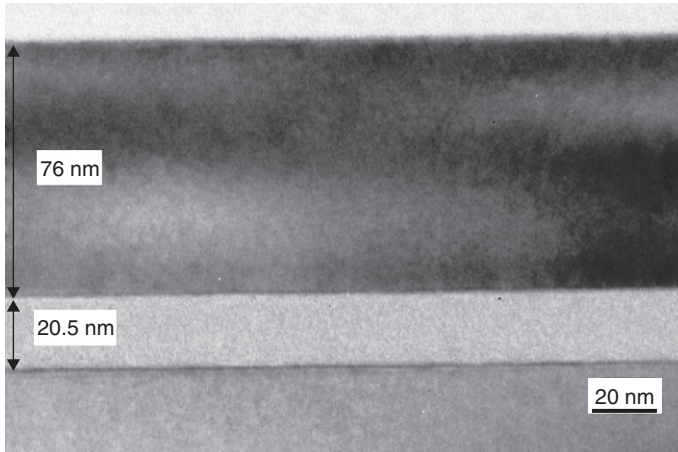
1.6 AFM cross-sectional profile of the Si top layer–buried oxide interface after annealing at 1320°C for 18 h. (Source: Reprinted from *Materials Science and Engineering B* **46**, Guilhalmenc *et al.*, ‘Characterization by atomic force microscopy of the SOI layer topography in low-dose SIMOX materials’, p 29, Copyright (1997), with permission from Elsevier.)

of the Si layers recrystallizing due to damage from oxygen implantation and the formation of the buried oxide. They also showed that the resulting Si top layer–BOX interface becomes increasingly smooth with greater annealing time at 1320°C. A spiral step and terrace morphology was demonstrated, and the heights of the terraces have been found to be multiples of the Si lattice parameter (Fig. 1.6).

In the case of bonded SOI wafers, the BOX layers can be thermally grown on the ‘donor’ wafer, from which the top Si layer derives, prior to direct bonding. This has led to Si top layer–BOX interfaces of a high thermal quality after annealing at 1100°C, as can be demonstrated by TEM (Fig. 1.7). At the same time, there are issues with closure of the bonding interface, which will be detailed later in the chapter (see Sections 1.6 and 1.7), in terms of surface preparation parameters and bonding process conditions.

Electrical properties of SOI wafers are another key concern for many applications. The pseudo-MOS transistor (ψ -MOSFET) technique was specifically developed for SOI characterization,^{45,46} and complements the standard measurements by Hall effect, spreading resistance, photoconductivity, etc., by measuring such properties as Si top layer doping type and level, carrier mobility, interface trap density and carrier recombination lifetime.

Cristoloveanu *et al.* showed that in SOI wafers obtained by the Smart Cut™ process via hydrogen implantation, hydrogen completely diffuses away from the Si wafer during high-temperature annealing, leaving the electrical properties of the single crystal unchanged.⁴⁷ In-depth homogeneity and



1.7 TEM observation of 75 nm Si/20 nm BOX layers after 1100°C annealing for 2 h. Upper interface (top Si layer–BOX) relates to the thermal oxide interface, lower interface (BOX–Si bulk wafer) relates to the bonding interface.

high carrier mobility have been demonstrated in SOI wafers, whether the SIMOX or Smart Cut™ processes have been used. For 300 mm SOI wafers, electron mobilities ($\mu_n \sim 650 \text{ cm}^2/\text{Vs}$) and hole mobilities ($\mu_p \sim 240 \text{ cm}^2/\text{Vs}$) are among the best measured in SOI wafers.^{48,49}

In the case of SOI wafers made by Smart Cut™, the interface quality is not degraded by hydrogen implantation or thermal annealing: the density of traps at the Si layer–BOX interface is less than $3 \times 10^{11} \text{ eV}^{-1}\text{cm}^{-2}$.⁴⁹ Moreover, Ionescu *et al.*, measuring carrier lifetimes by photoconductivity decay in the Si substrate and the transient ψ -MOSFET technique,⁵⁰ reported that carrier lifetimes in the top Si layer may be higher than 100 μs in SOI made by Smart Cut™, which outperforms the value measured in SIMOX SOI.

Comparisons of 300 mm SIMOX and Smart Cut™ SOI wafers show that these SOI materials are now reliable and reproducible, enabling integrated circuit fabrication. The top silicon film is high-quality single crystal with excellent electrical properties. The buried oxide and the top Si layer–BOX interface are of acceptable quality,⁴⁹ and high-performance transistors and test devices have been fabricated.⁵¹

1.5 Direct wafer bonding: wet surface cleaning techniques

Since Shimbo's experiments on silicon-to-silicon direct bonding in order to form diodes⁵² and Lasky's experiments on SOI structures obtained by

direct bonding,⁵³ there has been increasing interest in processes that can fabricate innovative structures by direct bonding. Such processes can create not only SOI structures but also many varied combinations of single-crystal layers bonded onto diverse buried layers and substrates, depending on the application.

This section describes direct bonding of Si and SiO₂ (the technique should be adaptable to other materials). The focus will be on direct bonding of two hydrophilic surfaces or of two hydrophobic surfaces, obtained via physical and chemical surface preparation. It will then be shown why smooth surfaces and suitable surface bonds are required for high-quality bonding. Fine surface preparation is needed for the proper addressing of key issues such as low particle and metallic contamination levels, in order to achieve high-yield, strong-bonding and defect-free structures. The following sections will briefly present several of the methods that are routinely used to evaluate both the surface preparation efficiency and the bonding quality and will emphasize how they aid an understanding of bonding mechanisms. Then improvements enabled by alternative surface preparations will be detailed, leading for instance to low-temperature bonding or to stronger bonding.

Direct bonding of Si and SiO₂ has been widely studied and used. Many conditioning processes have been developed for Si and SiO₂ surfaces (both film and bulk) to improve the quality of direct bonding. For most surfaces, conditioning processes result in hydrophilic surfaces that are well suited to spontaneous direct adhesion at room temperature (RT). Hydrophobic surfaces, though less commonly used, can also be suitable for direct bonding.

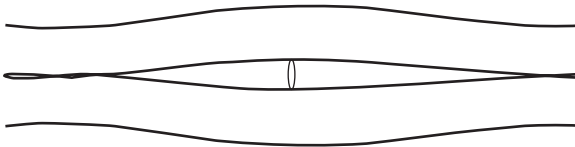
In the cases of hydrophilic Si and SiO₂ bonding, Si surfaces consist of thin native or chemically modified oxide, and SiO₂ surfaces consist of deposited or thermally grown oxide. Hydrogen bonds form between the two wafers, either from Si–OH groups present on each surface or from water molecules adsorbed on the Si–OH groups,⁵⁴ which increase the RT bonding energy. In order to strengthen the bonding, or during subsequent device processes, bonded structures are often submitted to thermal treatments. During these treatments, outgassing species, trapped particles and areas of weak bonding, if present, can cause bonding defects. In order to avoid these potential issues, surface conditioning processes must be finely tuned prior to bonding.^{55–57}

Contamination by organic species, particles and metallic species affects bonding quality. Organic compounds, from the environment or from storage materials, can inhibit the formation of chemical bonds between the two wafers. Particles will locally affect chemical bond formation and increase the cost in elastic energy of bonding the two surfaces; a relationship between sizes of particle and bonding defect has been observed for SOI bonding interfaces.⁵⁸ Metallic contaminants, from process tools or consumables, can affect the electrical properties of the bonded materials.

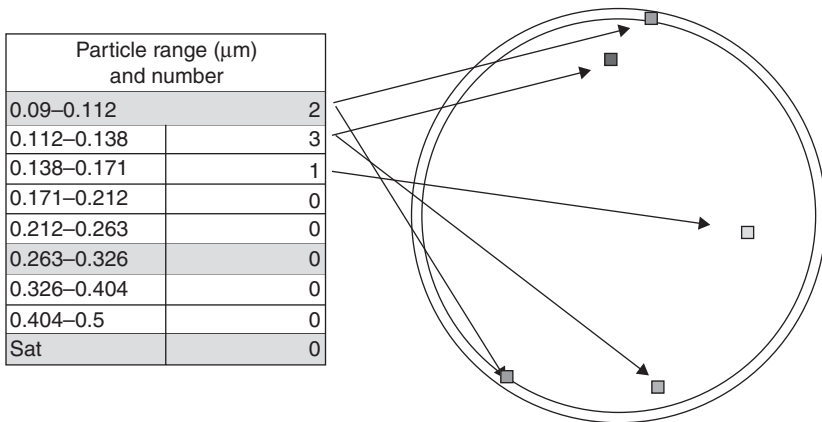
Two approaches are commonly used to remove organic contaminants, based either on a mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) (SPM) or on ozone diluted in deionized water (DIO_3). SPM and DIO_3 are very strong oxidizing agents that efficiently remove hydrocarbon contamination. SPM etching is very slight and does not affect surface microroughness. DIO_3 cleaning has the advantages of simplicity, lower temperature and reduced chemical waste. However, the low solubility of ozone limits the number of available reactive species, which limits potential oxidation. DIO_3 cleaning is thus more suited to the removal of airborne contaminants.^{3,59}

For the removal of particles, following the removal of organic contaminants, surfaces are usually cleaned by a mixture of ammonium hydroxide and hydrogen peroxide. This renders them highly hydrophilic.^{3,59,60} For instance, this basic solution oxidizes and lightly etches Si and SiO_2 surfaces simultaneously, leading to an undercut and removal of particles from the surfaces. In the case of Si surfaces, it creates a chemical oxide with a thickness in the 0.6–1.2 nm range. Note that it can also lead to surface roughening. At the same time, the high pH of the solution induces a zeta potential of the same sign on both the particles and the surface, which avoids any particle attraction. Control of surface particle contamination is crucial for high-quality direct bonding, since particles as small as 0.5 μm in height can induce bonding defects a few millimeters in diameter (Fig. 1.8).³ Particle densities can be monitored by a surface analyzer such as the KLA-Tencor SP2 Surfscan, using a particle detection threshold of 90 nm or less.⁴³ If cleaning conditions are properly specified to optimize particle removal, hydrophilic surface properties and surface roughening together, then it is possible to obtain very clean surfaces, as shown in Fig. 1.9.

Although the resulting surface is covered by Si–OH groups on which water molecules can adsorb, this cleaning can induce metal contamination, which is enhanced by its elevated pH. For this reason it is generally followed by cleaning in an acidic solution, for example, a mixture of hydrochloric acid and hydrogen peroxide.^{3,59,60} Given the low pH, the positive zeta potential induces particle attraction that can lead to light surface contamination. Solution concentration and temperature must therefore be tuned to



1.8 Bonding defect formation due to a particle contamination.

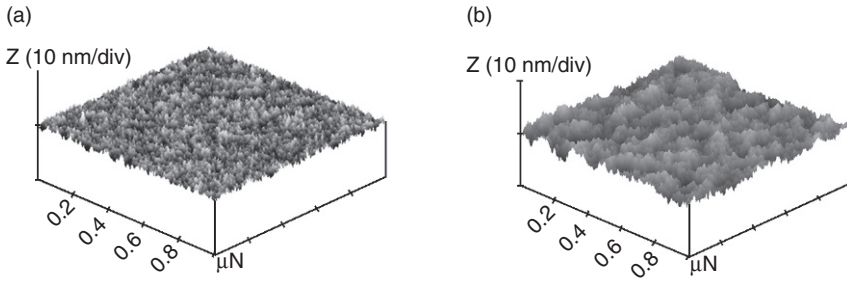


1.9 Particle contamination measurement using a KLA-Tencor SP2 Surfscan, using a detection threshold of 90 nm.

optimize metal removal efficiency while minimizing both the degradation of surface hydrophilicity and particle contamination.

Surface roughness plays a key role in the energy required for direct bonding. The key point is that covalent bonds between the two surfaces can only form if the two chemical species from each wafer are close enough to react together. Thus for wafer conditioning and to insure bonding strength and quality, one has to check that these treatments preserve the surface microroughness. For example, preparations prior to bonding can induce microroughness on hydrophilic SiO_2 surfaces. Figure 1.10 illustrates this for two different types of surface conditioning, where small (0.25 nm rms) and high (0.63 nm rms) roughness values were measured by AFM on $(1 \times 1) \mu\text{m}^2$ scans. When such surfaces are bonded onto identically rough SiO_2 surfaces, it can be observed that rougher surfaces lead to weaker bonding. In the case of SiO_2 surfaces, an upper limit of microroughness at which direct bonding is still possible has been determined at about 0.65 nm rms.⁶¹

For hydrophobic surfaces, interfacial bonding at RT occurs purely due to van der Waals forces. Several surface preparations lead to hydrophobic Si surfaces: for instance, annealing at high temperature (e.g. 1000°C under specific atmosphere) or oxide etching in hydrofluoric acid (HF solution). In these cases, bonding energy at RT is quite low and is very sensitive to surface roughness. A microroughness threshold for direct bonding of Si surfaces has been found at about 0.3 nm rms. Note that these roughness thresholds are given as practical limits for SOI fabrication process. Higher roughness values may be compatible with bonding when very weak bonding energies are acceptable, such as when there are no competing energies that need compensating (e.g. wafer bow or warp).



1.10 Typical AFM measurements on $(1 \times 1) \mu\text{m}^2$ scans for SiO_2 surfaces whose rms microroughness values are (a) 0.25 nm and (b) 0.63 nm.

1.6 Characterization of direct bonding mechanisms

Most characterization of surfaces prior to bonding and on bonded structures is done to evaluate both the strength and the quality of the bonded structures. It also helps in developing an understanding of bonding mechanisms, as described below for silicon and silicon oxide bonding.

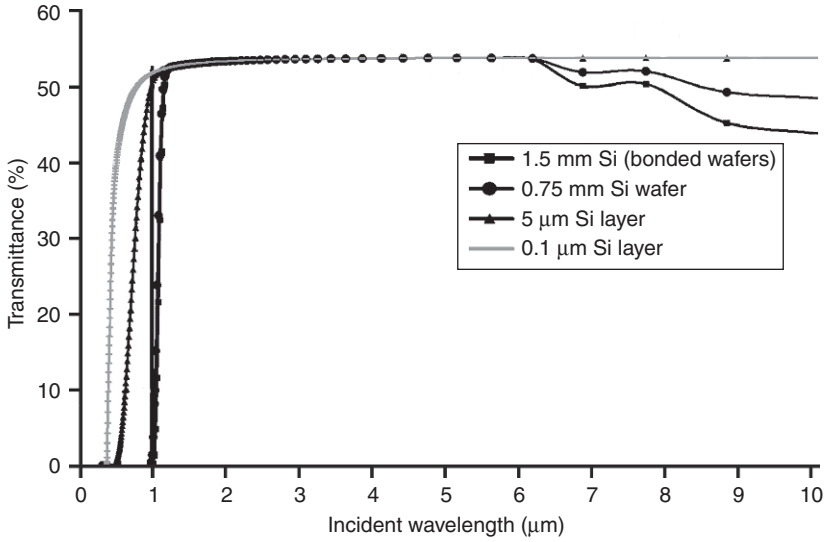
1.6.1 Bonding defect characterization

Silicon bonding defect characterization is usually performed using infrared cameras, because silicon is transparent at wavelengths of $\lambda > 1 \mu\text{m}$ (Fig. 1.11) when it is therefore possible to observe the bonding defects. Air gap induced by bonding defect creates an optical contrast that can be observed on wafer surface over bonding defect, depending on its height (Fig. 1.12).

Scanning acoustic microscopy (SAM) can be also used to characterize bonding defects. An acoustic wave is sent via a piezoelectric transducer through a water film and into the silicon wafers. The frequency is usually between 10 and 400 MHz. At each change in acoustic impedance, an echo returns to the transducer, which then functions as a microphone. By analyzing only those echoes reflected at the bonding interface, a bonding defect can be detected, whatever its thickness, as soon as a change in acoustic impedance occurs (for instance because of air or vacuum in the defect between the bonded surfaces). In the absence of bonding defects, no acoustic echo signal is detected (Fig. 1.13a). SAM routinely achieves a lateral resolution lower than $30 \mu\text{m}$ and a vertical resolution of a few nanometers, as shown in Fig. 1.13b and 1.13c.

1.6.2 Bonding energy measurements

In order to evaluate bonding strength, mode I delamination of a bonded structure can be induced by a double cantilever beam test method.⁶² Thus Maszara *et al.* proposed a method to measure the bonding strength of two

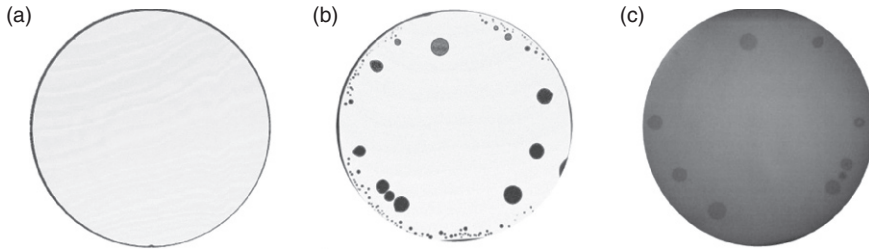


1.11 Transmittance curve versus incident wavelength depending on the silicon thickness.

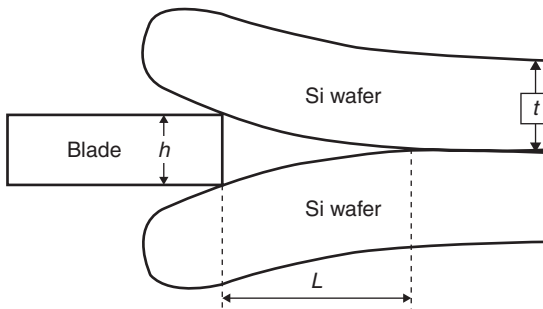


1.12 Defect located at the bonding interface observed through the top Si wafer by infrared camera. Fringes observed relate to the air gap inside the bonding defect.

wafers by inserting a blade between them, as shown in Fig. 1.14.⁶³ After Si or SiO₂ surfaces bond at room temperature, bonding energy (2γ) is relatively weak. Figure 1.15 shows typical variations in surface energy (γ) as a function of post-bonding anneal temperatures for hydrophobic Si-Si bonding and



1.13 SAM direct bonding characterization: (a) bonding interface without bonding defect; (b) bonding defect examples and (c) same bonded wafer pair as in (b) but characterized by an infrared camera. The last observation reveals that some bonding defects are not detected.



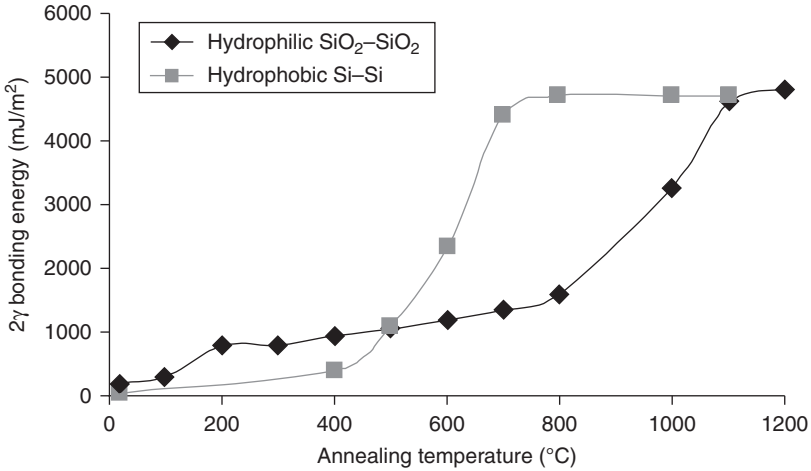
1.14 The crack-opening method by inserting a blade with thickness h in between the two t thick wafers for measuring delamination (debonding) length, L , which can be related to bonding energy.

for hydrophilic SiO_2 - SiO_2 bonding, where the oxides were thermally grown and did not need any CMP surface preparation. Room temperature bonding energy values, 2γ , are in the range 0.2 – 0.3 Jm^{-2} for bonding of hydrophilic Si or SiO_2 surfaces and a few tens of mJm^{-2} for bonding of hydrophobic, H-terminated Si surfaces.

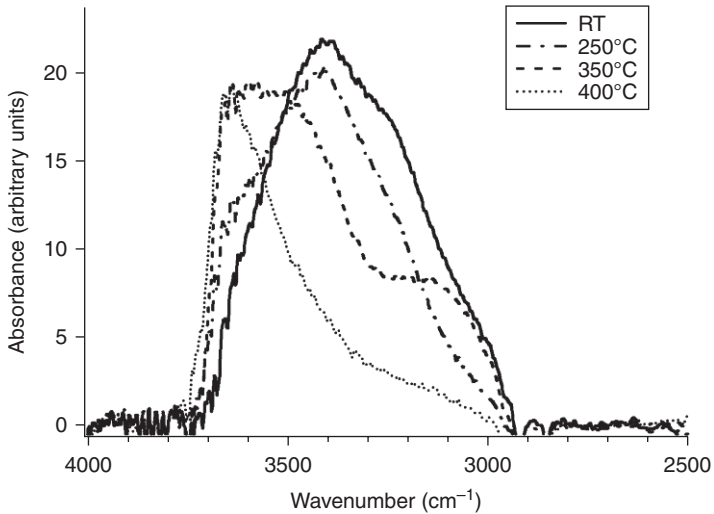
Thermal annealing is typically used to enhance adhesion by transforming weak physico-chemical interactions (due to van der Waals forces or hydrogen bonds) into covalent bonds between the two surfaces. This occurs in the hydrophilic case through modifying silanol bonds (Si-OH) into covalent siloxane bonds (Si-O-Si), and in the hydrophobic case through creating covalent silicon-silicon bonds.⁶⁴

1.6.3 Chemical bonds

Fourier transform infrared spectroscopy operated in a multiple internal reflection mode, FTIR-MIR, enables the nature of bonds and their densities



1.15 Variation of bonding energies as a function of thermal annealing temperatures for the bonding of two hydrophobic silicon wafers and two hydrophilic thermally oxidized Si wafers. (Source: Reprinted from Moriceau *et al.*, *Solid State Phenomena* **121-123**, 29-32, copyright (2007), with permission from Trans. Tech. Publications Ltd.)



1.16 Evolution of the -OH absorption band peaks in FTIR-MIR experiments measured after post-bonding anneal at different temperatures for hydrophilic SiO₂-SiO₂ bonding. (Source: Reprinted with permission from *Electrochemical and Solid-State Letters* **12**(10), H373. Copyright (2009), The Electrochemical Society.)

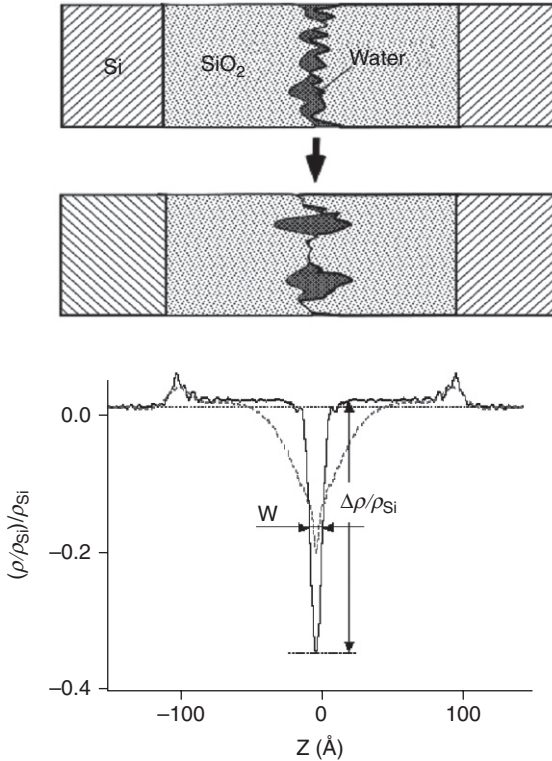
at the bonding interface to be measured. Figure 1.16 illustrates the case of hydrophilic SiO_2 – SiO_2 bonding. Thermally grown oxide layers are 10 nm thick.⁶⁵ Figure 1.16 shows clearly that –OH band peaks, in the 3000–3700 cm^{-1} wave number range, are strongly modified at annealing temperatures over 250°C. Water peaks, located in the 3200–3500 cm^{-1} range, decrease continuously. Si–OH peaks in the 3500–3700 cm^{-1} range first increase with temperature, up to 350°C, and then decrease for higher temperatures.

1.6.4 Bonding mechanisms

Hard X-ray reflectivity (XRR) measurements performed at the European Synchrotron Radiation Facility (ESRF) were used to characterize the physical and morphological evolution of the bonding interface by measuring electron density at the bonding gap.⁶⁶ For SiO_2 – SiO_2 bonding, a ziplock-type sealing mechanism has been proposed, which agrees well with both FTIR-MIR and XRR measurements (Fig. 1.17, top and middle).⁶⁶

One can observe that the bonding gap is filled during low-temperature annealing, comparing relative electron density values for $z=0$ at RT and after 400°C annealing for 2 h (Fig. 1.17, bottom). At this temperature, small unbonded zones are vertically enlarged to accommodate both a fixed amount of water and the tighter closure that exists everywhere else at the bonding interface, due to an increasing number of covalent bonds. During annealing at higher temperatures, the bonding interface gap tends to fill up and to disappear, and so any outgassing or by-product species that formed must leave the structure.

Additionally, it has been clearly demonstrated that surface roughness is a key parameter for direct bonding. For instance, Fig. 1.18 shows surface energy (γ) values versus microroughness rms values, characterized by AFM, in the case of the hydrophilic bonding of SiO_2 surfaces. At RT and in this microroughness range, we can assume that direct bonding is dominated by hydrogen bonds present at the bonding interface. Hydrogen bond density depends on the nature, the smoothness and the hydrophilic character of the surfaces. Figure 1.18 shows that surface energy values decrease when surface microroughness increases in the 0.45–0.65 nm rms range. Direct bonding seems to be dominated by asperity contacts and a continuous film of water may not be present everywhere at bonding interface. One can also observe that surface energies are quite constant at RT for microroughness values below 0.45 nm. Such behavior could be due to the water at the bonding interface. It is worth remembering that two or three single layers of water molecules are trapped at the bonding interface, as measured by FTIR or XRR.⁶⁷

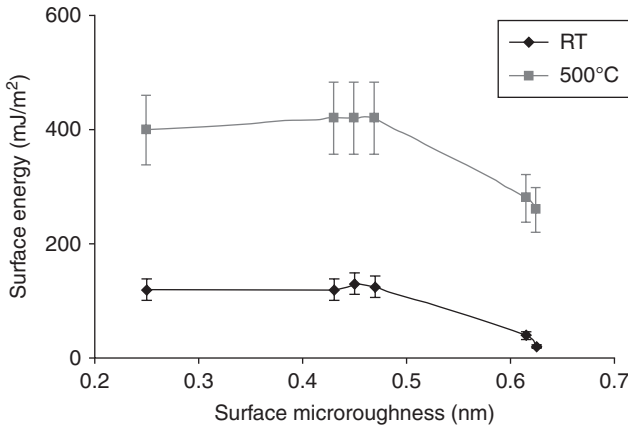


1.17 Sealing mechanism of the oxide–oxide bonding at RT (top) and after annealing at 400°C for 2 h (middle). The electron density profiles are shown on the bottom curve, at room temperature (solid line) and after annealing at 400°C for 2 h (dashed line). (Source: Reprinted with permission from *Electrochemical and Solid-State Letters* 12(10), H373. Copyright (2009), The Electrochemical Society.)

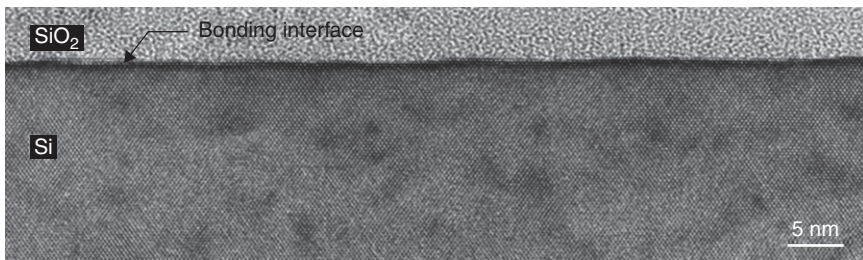
1.6.5 Bonding interface closure

It has been also suggested that high-temperature annealing could be performed in order to strengthen and close the bonding interface. The higher the annealing temperature, the more complete is the closure, as illustrated in Fig. 1.19 for Si–SiO₂ bonding after annealing at 1100°C. Nevertheless, for SiO₂ bonded structures of 0.6 nm rms roughness, cross-section TEM observations reveal many small cavities remaining at the bonding interface (Fig. 1.20),⁶¹ even after annealing at temperatures as high as 1100°C. This demonstrates weak closure of the bonding interface and low bonding energy.

In order to increase bonding energy and/or to decrease cavity density at the bonding interface, annealing at higher temperature can be used, as



1.18 Surface energies versus roughness rms values for SiO₂ bonded surfaces. Measurements are done using a blade insertion technique (◆) after RT contact and (■) after 500°C anneals. (Source: Reprinted with permission from *Electrochem Soc. PV 2003-19*, 49. Copyright (2003), The Electrochemical Society.)

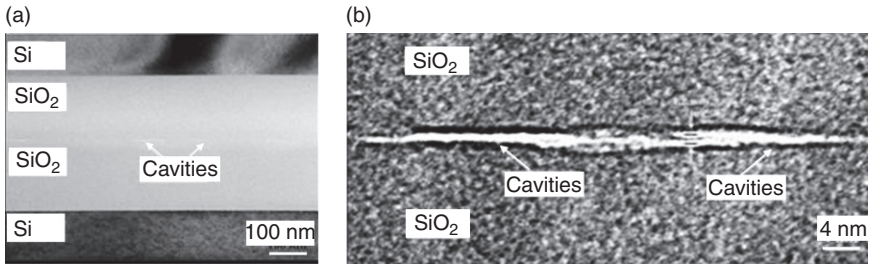


1.19 Efficient closure of Si-SiO₂ bonding interface after 1100°C annealing for 2 h as observed by HR-TEM cross-section.

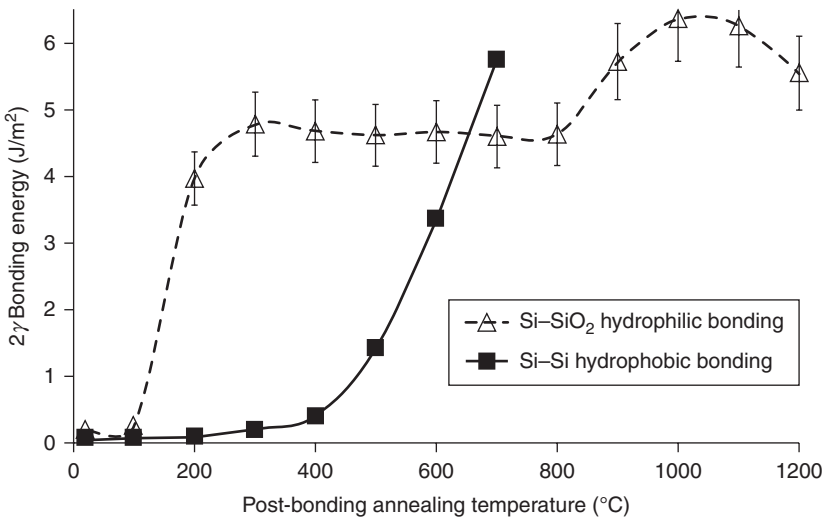
it allows oxide reflow. However, it should also be noted that annealing at high temperatures in order to strengthen bonding can be limited or even avoided and efficiently replaced by use of the alternative processes detailed below.

1.6.6 Water stress corrosion impact on bonding energy

Recently it has been shown that water stress corrosion of the siloxane bond Si-O-Si can greatly influence the measurement of bonding energy.⁶⁸ One way to avoid this phenomenon is to measure the bonding energy in an anhydrous atmosphere using, for instance, a glove box under nitrogen with less than 0.1 ppm of water. As shown in Fig. 1.21, hydrophilic bonding energy



1.20 Cross section TEM images of two bonded SiO₂ surfaces with rms roughness of 0.6 nm. (a) Small cavities at bonding interface remain observable even after annealing at 1100°C and (b) high magnification observation of such cavities.



1.21 Variation of bonding energies as a function of thermal annealing temperatures for the bonding of: (■) two hydrophobic silicon wafers and (Δ) hydrophilic silicon and thermally oxidized Si wafers. The measurements were made in an anhydrous atmosphere (0.1 ppm H₂O). The values over 900°C for hydrophilic bonding (linked to the dotted curve part) relate to the cases where the crack did not propagate at the bonding interface. (Source: Reprinted with permission from Fournel *et al.* (2012) *J. Appl. Phys.* **111**, 104907. Copyright (2002), AIP Publishing LLC.)

values are much more important for post-bonding annealing above 100°C than are the values shown in Fig. 1.15. Removing stress corrosion from the direct bonding energy measurement is then very important in order to recover the real bonding energy value and to be able to compare different bonding types.

Measurements of hydrophobic Si–Si bonding energy are not affected by water stress corrosion. This is because hydrophobic bonding induces Si–Si covalent bonds instead of Si–O–Si siloxane bonds.

Nevertheless, when instances of hydrophilic bonding performed under different conditions need to be compared, bonding energy measurements can be performed in controlled humidity atmosphere and then the comparisons will remain valid, although the absolute values of bonding energy will be underestimated. It is mainly such controlled-humidity bonding-energy values that are used in this chapter.

1.7 Alternative surface preparation processes for Si and SiO₂ direct bonding

Various surface preparation processes have been studied to substitute or complement wet surface cleaning, in order to obtain high bonding strength even after annealing at low temperatures. For instance, CMP steps, thermal treatments and plasma activations are very efficient processes for organic-contamination removal and for modifying both the surface and the near-subsurface, resulting in high bonding energies and defect-free bonding.

1.7.1 Chemical and mechanical polishing (CMP)

Direct bonding, which occurs at the nanometer scale, is induced by hydrogen bonds either via water molecules adsorbed on silanol groups (Si–OH) or between silanols from the two surfaces. So, a first approach is to increase silanol density and, specifically, water diffusion in the oxide subsurface. A surface preparation process such as CMP in a basic solution (pH in the range of 9–11) is well suited to induce these changes.⁶⁹

Superficial oxide film surfaces must not be too rough, in order to avoid issues in direct bonding. To ensure strong bonding, the surface of the oxide can be CMP-treated so that it is flat, smooth and defect-free. As silanol density is closely linked to surface roughness, this roughness will have a significant impact on the subsequent formation of strong covalent bonds.⁶¹ For instance, bonding energies for CMP-treated hydrophilic SiO₂ surfaces are measured at over 1.5 Jm⁻² after annealing for 2 h at 200°C. This should be compared with the 0.6 Jm⁻² routinely obtained for bonded structures without CMP treatment prior to bonding. However, special care must be taken to avoid any surface asperities which could be left by CMP processes, such as particles or scratches that could prevent tight closure and lead to bonding defects.

An additional benefit of surface CMP treatment is that it can allow a significant reduction in the thermal energy budget of the annealing used to strengthen the bonding. This is due to the reduction of surface microroughness and the increase of bond densities. It has thus been possible to develop

successful low-temperature bonding processes ($T < 500^\circ\text{C}$) for diverse applications.⁷⁰

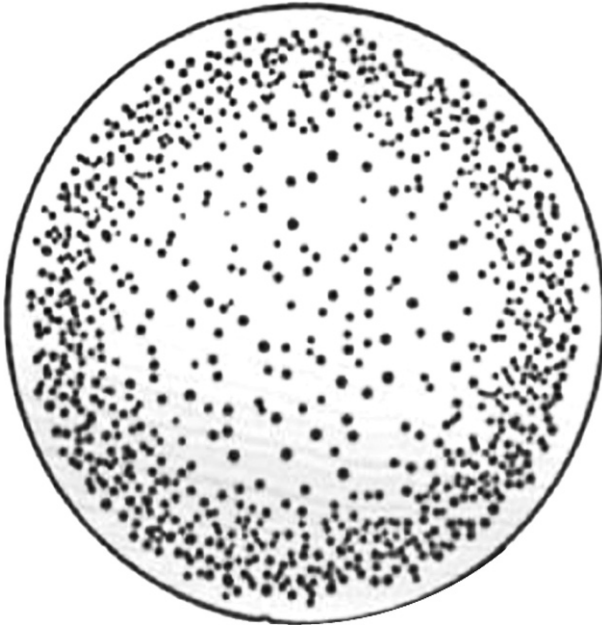
Another advantage for the CMP process is that it permits the preparation of patterned surfaces prior to direct bonding. This applies to wafers with different materials at their surface, for example, Si mesas in SiO_2 layers.⁷¹ Performing standard CMP on such mixed surfaces leads to local variations in removal rate. Specific CMP processes are thus needed, for instance based on monitoring the removal rates for each material. Nevertheless, one can conclude that bonding processes based on CMP treatments enable the manufacture of innovative bonded substrates and, consequently, new applications.

1.7.2 Surface preparation by thermal treatment

Another type of defect in the bonding of hydrophilic surfaces has its origin in outgassing at the bonding interface, which can be caused by the presence of water (as a direct effect) or hydrogen (as an indirect effect). This is, for example, the case when a hydrophilic silicon surface is bonded to either a Si or SiO_2 surface. These defects are all the more visible when buried oxide layers are thin and standard surface preparations are performed. Such a defect in Si–Si hydrophilic bonding, as detected by SAM, is illustrated in Fig. 1.22. Understanding the origin of these defects and how to avoid them are thus of special importance when defect-free bonding processes need to be developed.

Water is adsorbed at each hydrophilic surface and is thus trapped at the interface after bonding. This water allows bonding by hydrogen bonds at RT. The amount of water is typically two molecular layers. Unfortunately, during annealing (used for instance to strengthen the bonding) water may react with silicon to produce additional SiO_2 and H_2 gas as a by-product.⁷² H_2 is confined in the narrow bonding interface as long as its solubility in silicon and its ability to diffuse through silicon are small, which is typically the case at temperatures below a few hundred degrees Celsius. The solubility and diffusion of hydrogen are higher in SiO_2 but the small volume of thin BOX layers may limit its absorption capability. As a consequence, H_2 pressure increases with the annealing temperature, and when the pressure exceeds the mechanical strength of the bonding interface, a bonding defect will form.⁷³

At higher annealing temperatures, hydrogen solubility in silicon allows pressure in the bonding interface to drop. However, while small defects collapse, larger ones remain stable against dissolution. This has been explained elsewhere.^{72,75} To overcome such issues, methods have been widely developed for annealing Si wafers prior to bonding under specific atmospheres and at temperatures high enough to reduce the hydrophilic character of the surfaces. For example, 200 mm Si–Si bonded structures, with surfaces annealed under nitrogen at 500°C prior to bonding, have been observed by SAM.⁵⁶ Figure 1.23 clearly shows a decrease of defect density following

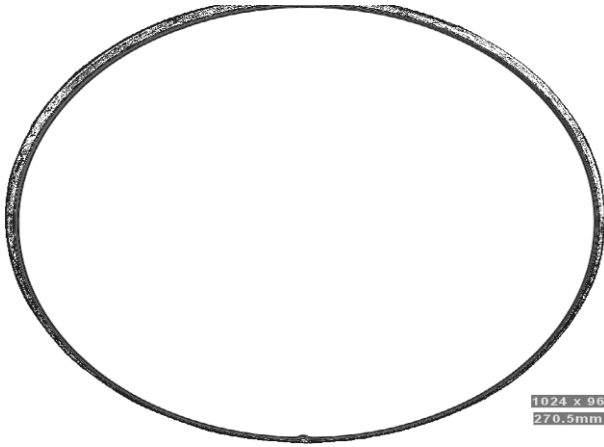


1.22 SAM image of defects formed at a Si-Si hydrophilic bonding after annealing at 400°C for 2 h. (Si wafer diameter 300 mm.)

annealing at 400°C after bonding. This demonstrates that annealing prior to bonding is an efficient method for water desorption and subsequently obtaining defect-free, bonded structures.^{56,57,72} Furthermore, Fournel *et al.* reported that low-temperature and long post-bonding annealing facilitated the lateral diffusion of degassing species⁷⁶ and enabled defect-free bonded structures to be obtained over the whole range of post-bonding annealing.

1.7.3 Surface activation by plasma processes

Surface activation by plasma processes, prior to bonding, has appreciable effects, since plasma-assisted wafer bonding is an efficient method for removing contaminants, such as hydrocarbons or undesired species adsorbed at a surface,⁷⁷ and also reduces surface roughness and creates a subsurface disordered layer.⁷⁸ Through these chemical and physical mechanisms, plasma treatments increase the surface density of silanol Si-OH groups and create surfaces with a highly hydrophilic character and a high number of available bonding sites. This allows significant increases in bonding strength by polymerization of surface Si-OH groups between the two contacted wafers.^{3,79,80} Furthermore, because plasma treatments can lead to smoother surfaces, they may also increase bonding energies.



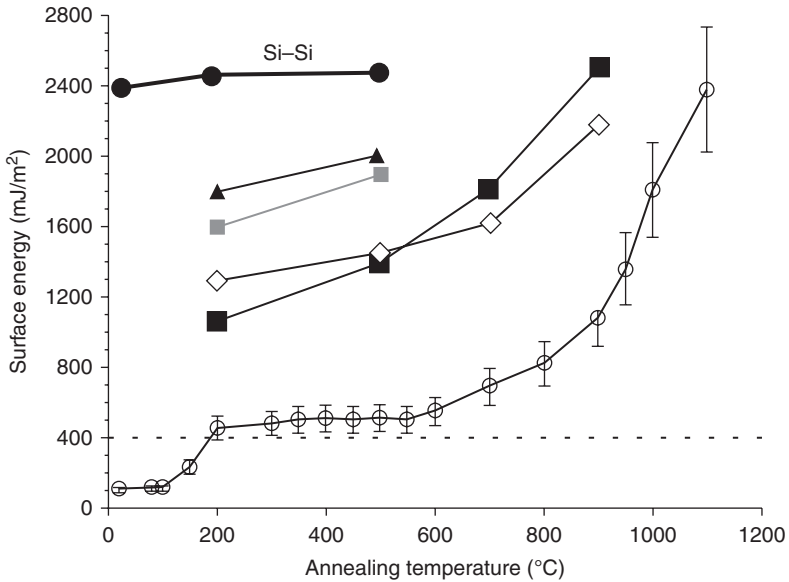
1.23 SAM observation of 200 mm Si-Si bonded structure after 400°C anneal. Bonding is achieved after a pre-bonding surface annealing at 500°C. No defects are observed here.

Figure 1.24 shows typical bonding energies for Si-SiO₂ bonded structures, obtained after surface activation by various plasma treatments, and their variation against post-bonding annealing temperature. These energy values can be compared to values obtained with surfaces prepared by RCA (Radio Corporation of America) cleaning as described by Kern.^{60,79} Moreover, comparison is made in Fig. 1.24 with the case of Si-Si bonding after plasma activation as reported by Wang *et al.*,⁸¹ which shows that bonding energy values are higher even after low-temperature annealing.⁷⁹⁻⁸³ The mechanisms responsible for the increase in bonding energy after plasma activation are still not completely understood, but they may involve both an enhancement of water diffusion away from the bonding interface and a formation of siloxane bonds, promoted by the subsurface disordered layer that plasma treatment induces.⁷⁸

Plasma treatments yield high bonding strengths at moderate temperature (<500°C), which make them very attractive methods for obtaining bonded heterostructures made of different materials, for example, wafers with different thermal expansion coefficients, such as silicon-on-glass (SOG),⁸⁴ and strained silicon-on-insulator (sSOI) and silicon-germanium-on-insulator (SiGeOI) structures.⁸⁵ This provides benefits for Smart Cut™ technology because low-temperature processes can allow thin single-crystal layers to be transferred onto substrates in spite of very different coefficients of thermal expansion.

1.7.4 Bonding under vacuum

Bonding under vacuum, instead of bonding at atmospheric pressure, offers interesting possibilities for some applications. For instance, bonding

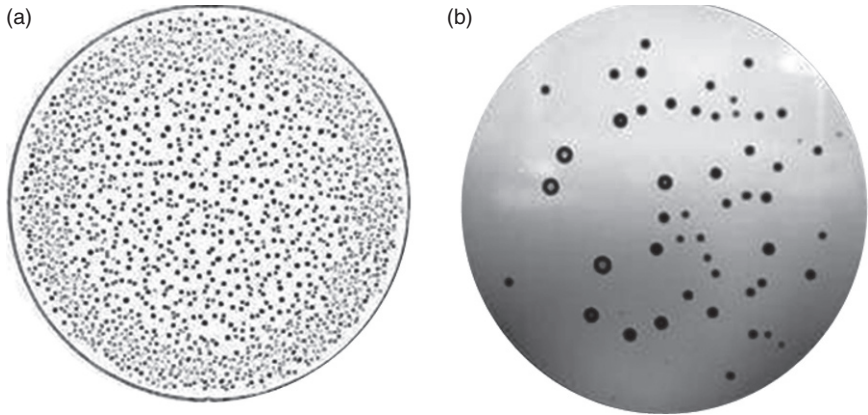


1.24 Typical Si-SiO₂ bonding energies, obtained after surface activations by various plasma treatments: (▲,■) activations by reactive ion etching (RIE) plasma and (◇,■) by microwave (MW) and induction coupled plasma (ICP) and their variations vs annealing temperatures, compared to values (○) obtained with RCA cleaned surfaces. (●) For comparison, dots correspond to bonding energy values obtained by Wang *et al.* in the case of Si-Si bonding after plasma activation.⁸¹

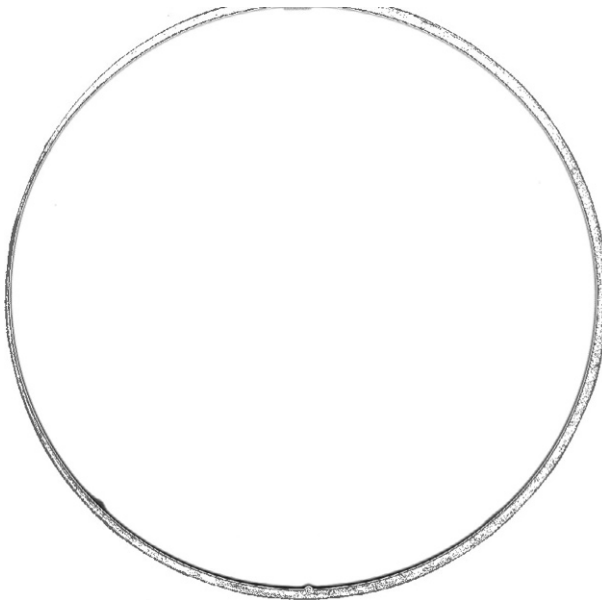
around cavities is often required for MEMS applications. Even if a vacuum is not required inside the cavity, vacuum bonding is usually performed in order to prevent overpressure during post-bonding annealing, which could induce debonding or cracks. Vacuum bonding can also be used for surface preparation, since direct hydrophilic silicon bonding creates numerous bonding voids even after low-temperature annealing (Fig. 1.25a). A combination of bonding under vacuum and long anneals post-bonding greatly reduces interfacial bonding defect density (Fig. 1.25b).⁷⁶ Moreover, still better bonding results from heating wafers under vacuum pre-bonding and using long anneals post-bonding. In these cases, no bonding defects can be detected at 400°C (Fig. 1.26) or even up to 700°C.

1.8 Mass production of SOI substrates by ion implantation, bonding and splitting: Smart Cut™ technology

Among the different techniques used for SOI fabrication, Smart Cut™ technology, based on implantation of light ions and followed by layer



1.25 SAM observations of (a) hydrophilic Si-Si surfaces bonded and annealed at 400°C and (b) Si-Si hydrophilic bonding under vacuum combined with long annealing step up to 400°C (ramp up of 0.25°C/min and annealing step each 100°C for 10 h).



1.26 SAM characterization of hot (250°C, 15 min) vacuum bonding (10^{-2} mbar) combined with post-bonding long anneal treatment up to 400°C.

transfer using wafer bonding and splitting after annealing, has become the most prominent technology for high-quality mass production of SOI substrates. Since the publication by Bruel,^{33,37} the process has been continuously improved to answer the constant demand for ever better quality substrates.

We shall focus here on describing the physical processes that make this technology effective, from atomic-scale ion implantation to the final wafer-scale splitting.

The blistering of materials by ion irradiation has been observed for a long time in a nuclear context, where the aging of materials under a high flux of particles has been an issue. Three parameters must be considered when dealing with the effects of ion implantation: dose, energy and dose rate. We shall restrict ourselves here to a parameter set with doses around 10^{16} cm⁻², energies in the 10 keV range and small dose rates to prevent implantation annealing (i.e. room temperature implantation).

1.8.1 As-implanted silicon

When implanted in these conditions, hydrogen ions are incorporated individually in the silicon matrix, and so the question of their location and effect on the crystal immediately arises. Several studies have been performed using a variety of nanometer-scale characterization tools. The first effect of ion implantation is to produce a strained layer roughly corresponding to the distribution profile of the implanted hydrogen.⁸⁶ Incorporation of the hydrogen induces a volume expansion of the silicon crystal located around the projected range of the ions. Due to the underlying bulk silicon crystal, this expansion is restricted to the normal direction, but the in-plane stress induced by implantation is visible, for example, through wafer bending.

In this ‘as-implanted’ state, the hydrogen atoms are located in preferential sites of the crystal between the silicon atoms. The preferred locations (minimal energy locations) have been explored using, for example, *ab initio* calculations, and the findings have been experimentally investigated using different spectroscopic methods (IR spectroscopy of Si–H bonds, Raman spectroscopy).⁸⁷ There is an agreement that one preferred location for hydrogen in silicon is the so-called bond-center position, where H is located midway between two Si atoms. However, a difficulty with the characterization is that immediately after implantation, a large variety of species is formed due to interaction of the hydrogen with point defects formed during implantation (vacancies and interstitials). Stable species can form that involve several hydrogen atoms or vacancies. This is the natural evolution of the system upon annealing.

1.8.2 Platelet formation

After implantation the silicon crystal is supersaturated with hydrogen, and upon annealing it will naturally tend to evolve into a phase-separated

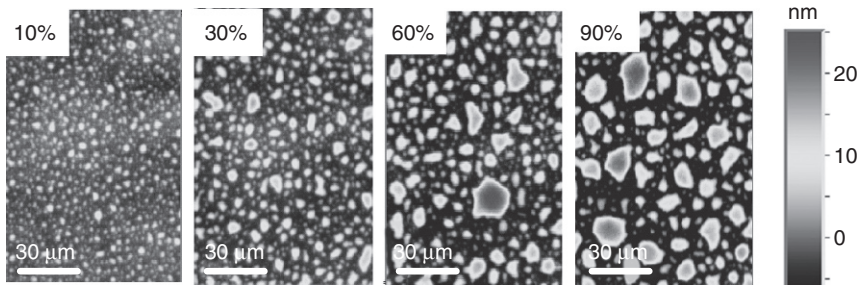
situation with hydrogen gas on one side and hydrogen-free silicon on the other (we neglect the (very slight) solubility of hydrogen in silicon). This evolution proceeds through classical nucleation, growth and coarsening, during which, especially at the early nucleation stage, some species may be more stable and play a larger role than others (according to cluster dynamics). This stage is difficult to characterize experimentally or numerically.

On longer timescales the hydrogen forms platelets. These are flat, ellipsoidal objects whose diameters vary typically between 1 and 50 nm. They are filled with hydrogen gas and their walls are covered by H-terminated Si surfaces. They have preferred orientation depending on the orientation of the crystal and its stress state. When a crystal is annealed below a free surface, the platelets tend to be parallel to the free surface. Platelet formation has been observed *in extenso* through the work of various groups, especially that of Claverie.⁸⁸ Study of the growth and coarsening stage at this nanometer-size range has been performed mainly using electron microscopy techniques.⁸⁸ Platelet distribution has been shown to evolve along a process of Ostwald ripening, that is, an exchange of material (gas) between platelets of different sizes, the larger platelets growing at the expense of the highly pressurized smaller ones. The growth of platelets does not extend forever and platelets have been observed to remain under split surfaces. It is admitted that the growth of platelets occurs only during the first percent of the total split thermal budget. Evidence for platelet formation has also been provided by techniques such as small-angle X-ray scattering.⁸⁹

1.8.3 Microcrack development

During the annealing process, the platelet stage is followed by the microcrack evolution stage.^{90,91} Microcracks are initially formed by the coalescence of platelets generally close to the middle of the implantation distribution. The evolution of microcracks during annealing can be followed using IR optical microscopy (Fig. 1.27) as the microcracks have a typical diameter of several micrometers.⁹²

Several scenarios have been put forward for microcrack development. It has been proposed that cracks interact in the same way as platelets do and that the exchange of gas between differently sized cracks is the driver for their evolution. Recent measurements, including the total amount of gas released when opening the interface at different stages of annealing up to the moment of thermal splitting, have shown that the amount of hydrogen and the total area covered by cracks increases. It is believed that platelets play a role in the last stage of microcrack development and that they may be the source of hydrogen to feed the cracks. When no stiffening wafer is bonded to



1.27 Interferometry microscopy observations of microcrack growth upon isothermal annealing. The percentage refers to split time.

the surface, the thin silicon film located above any microcracks may deform, resulting in blisters that are readily visible using microscopy. It is the development of microcracks that represent the main driver for substrate weakening along the implanted layer. When the development of microcracks has proceeded far enough, the wafer may experience macroscopic crack propagation that will travel at high speed through the cracked region. The post-split roughness of wafers show the clear signature of microcrack distribution with flat areas (the microcrack regions) separated by cracked walls.

During the development of platelets and microcracks, the system is driven by constant minimization of the total energy, including surface terms (the energy required to open an interface in the silicon) and volume terms (the elastic energy associated with the deformation of silicon by pressurized cavities). The balance between these two contributions, with continuous exchange between them by diffusion of gas, drives the evolution of the distribution of cracks up to the final split. In this respect, hydrogen has two effects. It acts both on the volume term through an increase of gas pressure in the cavities and also on the surface term by passivating dangling bonds when opening cracks in silicon, hence reducing the energetic cost of crack development.

Advantageously, when helium is used together with hydrogen, the total dose can be reduced while using a minimum amount of hydrogen in order to passivate surfaces (but limiting the amount 'lost' in stable point-defects) and using helium to exert a mechanical pressure only, given the weak affinity between helium and silicon. This process is currently used in production.

The observed roughness of the as-split wafers (a few nanometers rms up to 10 nm peak-to-valley) calls for techniques to reduce the level of post-split surface treatment (Fig. 1.28).⁹³ One possibility is to use confinement layers to try to force nucleation and microcrack development into a height range that is more restricted than the implantation range, for example by depositing

boron and re-epitaxy silicon on top of the layer. When the implanted hydrogen layer is superimposed (with implant-energy tuning) on the boron-rich layer, strong boron–hydrogen affinity will allow the rapid development of cavities located exclusively in the confinement layer. This technique is effective at reducing post-split roughness and has interesting potential for applications where very thin layers are to be transferred or where aggressive smoothing or post-split polishing techniques are not allowable.

1.8.4 Trends in SOI fabrication using the Smart Cut™ process

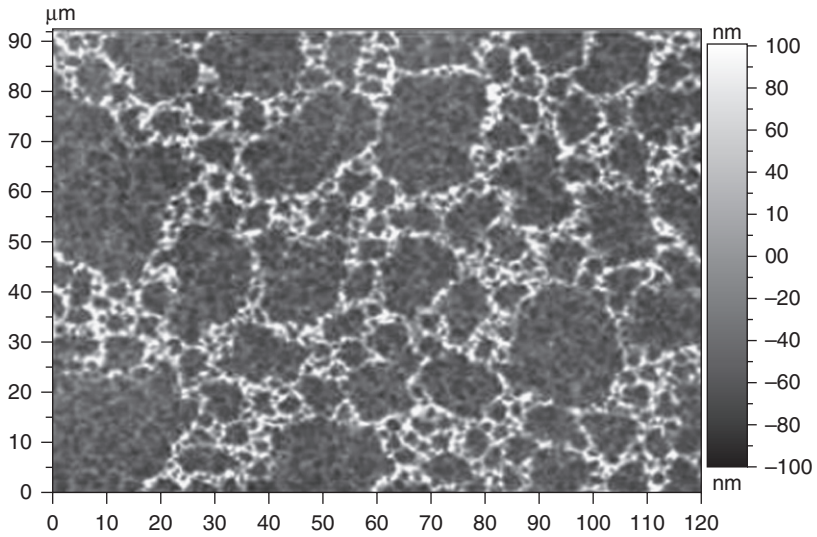
Many different SOI structures can be built using Smart Cut™ technology. The thickness of the top silicon film is typically in the range of a few tens of nanometers to a few micrometers. This is limited by implantation energy, which is below 200 keV using most of the standard implantation equipment. Furthermore, in many cases, to keep a thermal SiO₂–Si interface below a thin, top silicon film, the oxide film is thermally grown prior to the implantation. Thus BOX thickness can be also limited by implantation energy. In order to deal with a greater range of BOX thickness, SiO₂–SiO₂ bonding can be used but this requires higher annealing temperatures in order to achieve complete closure of the bonding interface.

Uniformity of thickness is a crucial SOI parameter. This is especially the case for SOI structures that are designed to enable fully depleted complementary metal oxide semiconductor (CMOS) devices.⁹⁴ At present, the uniformity of a 300 mm SOI wafer is better than ± 0.5 nm (min–max range) at any point, where the top silicon thickness is as thin as 10 nm and BOX thickness is around 10 ± 1 nm. Surfaces are now also of very high quality in that defect density is less than 0.05 def cm⁻² detected with a low threshold value for sizes around 50 nm.

It is worth noting that future advanced SOI structures may use strained sSOI wafers, described below, which enable greater electron mobility and lower power consumptions.^{95–97} Strain as high as 1.3 GPa can routinely be reached, as measured either by XRD⁹⁶ or by Raman spectroscopy.⁹⁷

1.9 Fabrication of more complex SOI structures

The different techniques developed in mainstream SOI fabrication are now applicable to more complex SOI-type structures and heterostructures, where the higher level of complexity can be taken into account, as described in this section. Thanks to its generic character, the Smart Cut™ process allows fabrication of many and varied innovative engineered structures and retains its potential for future technologies.



1.28 Optical profilometry image of the split surfaces. The pattern due to microcracks at the final stage is clearly visible.

1.9.1 Strained silicon-on-insulator wafers (sSOI)

It is very desirable to increase carrier mobility in microelectronics devices such as MOSFETs for high-frequency applications. One possibility is to use the silicon strain effect. This can be implemented in SOI structures by using strained silicon layers as top layers, leading to strained silicon-on-insulator (sSOI) structures. Two processes have been developed to obtain such sSOI structures, both of which use the ability to grow thin epitaxial, strained silicon layers on top of relaxed $\text{Si}_{(1-x)}\text{Ge}_x$ layers.

In one process, a relaxed $\text{Si}_{(1-x)}\text{Ge}_x$ layer is first grown on a silicon wafer and is implanted by light gas ions. The implanted wafer is directly bonded via the buried oxide to the final SOI-type substrate. Splitting is induced and part of the $\text{Si}_{(1-x)}\text{Ge}_x$ layer is transferred by the Smart Cut™ process, leading to a $\text{Si}_{(1-x)}\text{Ge}_x$ -on-insulator structure. Finally, a thin, epitaxial, strained silicon layer is grown on the transferred $\text{Si}_{(1-x)}\text{Ge}_x$ layer. This approach leads to a bilayer-on-insulator structure, the bilayer composed of thin, strained silicon on the top and $\text{Si}_{(1-x)}\text{Ge}_x$ on the bottom.⁹⁷⁹⁸

In the other process, a thin epitaxial strained Si layer is first grown on a relaxed epitaxial $\text{Si}_{(1-x)}\text{Ge}_x$ layer. Then light gas ion implantation is performed at depth within the $\text{Si}_{(1-x)}\text{Ge}_x$ layer. After bonding and splitting, the bilayer (thin $\text{Si}_{(1-x)}\text{Ge}_x$ as upper layer, strained silicon as bottom layer) is transferred onto the buried oxide. The superficial $\text{Si}_{(1-x)}\text{Ge}_x$ layer is then

removed in order to leave the unique, thin strained silicon layer as the top layer of the sSOI structure.^{97,98}

1.9.2 SOI type with various buried dielectric layers

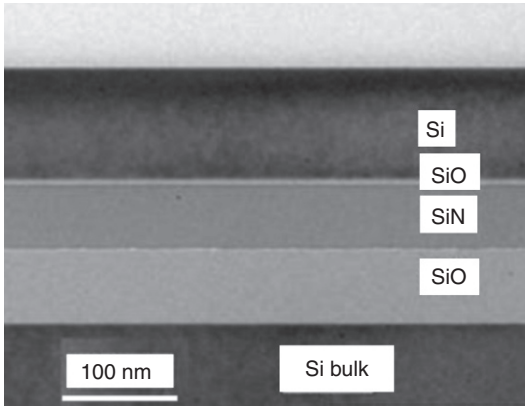
It is advantageous to change the nature of the buried insulator to give it properties better suited to the intended application of the specific SOI-type structure. For instance, SOI with a buried SiO_2 layer benefits applications that require very efficient electrical insulation between the top silicon layer and the final substrates; SiO_2 layers routinely grown by thermal oxidizing treatment have breakdown voltages higher than 5 MVcm^{-1} . Other applications may require thermal conduction between the top silicon layer and the substrate, and in those cases Si_3N_4 buried layers are preferred because their thermal conductivity is roughly 30 times higher than it is for SiO_2 .

In some more specific cases, high thermal dissipation may be needed through the buried insulating layer while a high electrical quality is required at the two buried interfaces, that is, between the top Si layer or the base and the buried insulating layer. A combination of SiO_2 and Si_3N_4 thin films can address this requirement, as demonstrated by multilayered SOI (SOIM) structures.⁹⁹ For instance, Fig. 1.29 shows a TEM observation of a SOIM structure in which the buried insulating multilayer is a stack of 2.5 nm-thick SiO_2 , 70 nm-thick Si_3N_4 and 70 nm-thick SiO_2 layers, respectively.

1.10 Fabrication of heterogeneous structures

Heterostructures made of materials with different properties could lead to very interesting and innovative applications. For instance, bonding a silicon wafer onto a fused silica wafer could lead to structures that would be attractive for use in displays. The layer transfer technique allows one material to be replaced by another, which could be cheaper or more compatible with future applications.

Nevertheless, the bonding of materials with different physical characteristics could generate problems in stacking processes and limitations in applications. For instance, if the materials have different thermal expansion coefficients (CTE), stress will be induced during post-bonding annealing.¹⁰⁰ If stacked materials are directly bonded, then there can be no gliding at the bonding interface and therefore no release of in-plane stress. Thermal stress of that type could disturb post-processing and even break the heterostructure. Using the thin layer transfer technique based on ion implantation and thermal splitting, limits at temperatures lower than for non-implanted bulk materials could require more complex processes for the fabrication of heterostructures.¹⁰¹ Different techniques, based on



1.29 TEM observation of a SOIM structure. The buried multilayered insulator is a stack of 2.5 nm SiO_2 , 70 nm Si_3N_4 and 70 nm SiO_2 layers, respectively.

analytical stress models, have been developed to minimize thermal stress in heterostructures.

1.10.1 Analytical stress model for heterostructures

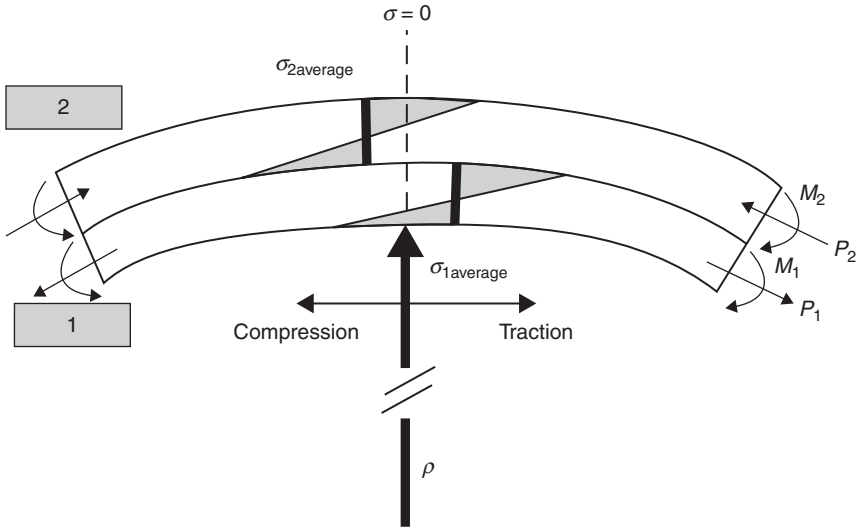
The analytical simulations addressed here are based on Timoshenko's plate theory,¹⁰² with infinite elastic plates and the assumption of small deformations. Two wafers are bonded at T_i and annealed up to T_f . Young's modulus (E_1, E_2) and Poisson's coefficients (ν_1, ν_2) are considered constants, as are thermal expansion coefficients (α_1, α_2). The wafer thicknesses are d_1 and d_2 , wafer 1 is placed below wafer 2 and $\alpha_1 < \alpha_2$. Considering a bonded portion, the internal forces (P) and the moments (M) which maintain the structure in equilibrium are represented in Fig. 1.30 (ρ is the curvature radius).

Following Timoshenko's theory, with $m = d_1/d_2$ and $n = E_1(1 - \nu_2)/E_2(1 - \nu_1) = E'_1/E'_2$, we obtain for two wafers:

$$\frac{1}{\rho} = \frac{6(1+m)^2(\alpha_1 - \alpha_2)(T_f - T_i)}{(d_1 + d_2)\left(3(m+1)^2 + (m^2 + (1/mn))(mn+1)\right)} \quad [1.1]$$

$$\sigma_1(z) = \frac{1}{\rho} \left[E'_1 \left(z - \frac{d_1}{2} \right) + \frac{1}{d_1} \left(\frac{E'_1 d_1^3 + E'_2 d_2^3}{6(d_1 + d_2)} \right) \right] \quad [1.2]$$

$$\sigma_2(z) = \frac{1}{\rho} \left[E'_2 \left(z - d_1 - \frac{d_2}{2} \right) - \frac{1}{d_2} \left(\frac{E'_1 d_1^3 + E'_2 d_2^3}{6(d_1 + d_2)} \right) \right] \quad [1.3]$$



1.30 Heterostructure stress model at a temperature $T_f > T_i$ with $\alpha_1 < \alpha_2$. P_1 and P_2 are the axial tensile forces and M_1 and M_2 are the bending moments relative to wafer 1 and wafer 2.

where σ_i is the plane stress inside each material.

For several wafers or layers bonded to each other with imposed ρ_0 during bonding,¹⁰³ one can write:

$$\frac{1}{\rho} = \frac{\left\{ \begin{aligned} & \sum_j E'_j x_j * \left[\sum_{k < i} (\alpha_k - \alpha_{k+1}) \Delta T - \sum_{k < j} (\alpha_k - \alpha_{k+1}) \Delta T \right] + \\ & -6 * \sum_i E'_i x_i * \left(2 \sum_{j < i} x_j + x_i \right) * \left\{ \sum_j E'_j x_j * \left[\sum_{k < j} \left(\frac{d_k + d_{k+1}}{2\rho_0} \right) - \sum_{k < i} \left(\frac{d_k + d_{k+1}}{2\rho_0} \right) \right] + \right. \\ & \left. \sum_j E'_j x_j * \left[\frac{P_{0i}}{E'_i d_i} - \frac{P_{0j}}{E'_j d_j} \right] \right\} \end{aligned} \right\}}{\sum_i E'_i x_i * \left[\sum_j E'_j x_j^3 + 3 * \left(2 \sum_{j < i} x_j + x_i \right) * \left\{ \sum_j E'_j x_j * \left[x_i - x_j + \sum_{k < i} 2x_k - \sum_{k < j} 2x_k \right] \right\} \right]} \quad [1.4]$$

and

$$\sigma_i = \frac{P_i}{d_i} + \frac{E_i}{\rho} \left(z - \sum_{j < i} d_j - \frac{d_i}{2} \right) \quad [1.5]$$

It is also possible to take into account that thermal coefficients are not constant between T_i and T_f by replacing

$$(\alpha_k - \alpha_{k+1})\Delta T \quad [1.6]$$

with

$$\int_{T_i}^{T_f} (\alpha_k(T) - \alpha_{k+1}(T)) dT \quad [1.7]$$

For the stored elastic energy, one can write:

$$\left[\frac{U}{S} \right] = \int_0^d \frac{(\sigma_x^2 + \sigma_y^2 - 2\nu\sigma_x\sigma_y)}{2E} dt = \int_0^d \frac{\sigma^2}{E'} dt \quad [1.8]$$

$$\left[\frac{U}{S} \right]_i = \frac{1}{E'_i} \left[a^2 \sum_{j<i+1} d_j + ab \left(\sum_{j<i+1} d_j \right)^2 + \frac{b^2 \left(\sum_{j<i+1} d_j \right)^3}{3} \right] - \frac{1}{E'_i} \left[a^2 \sum_{j<i} d_j + ab \left(\sum_{j<i} d_j \right)^2 + \frac{b^2 \left(\sum_{j<i} d_j \right)^3}{3} \right] \quad [1.9]$$

with

$$a = \frac{P_i}{d_i} - \frac{E'_i}{\rho} \left(\sum_{j<i} d_j + \frac{d_i}{2} \right) \quad [1.10]$$

and

$$b = \frac{E'_i}{\rho} \quad [1.11]$$

1.10.2 Thermal stress decrease for heterostructures

These mathematical developments can be applied, for instance, to a heterostructure built of a 720 μm -thick silicon wafer bonded onto a 1 mm-thick fused silica wafer. Wafer diameters are 200 mm in these simulations. One can calculate the stress on each side of the wafers, the global bow and the stored elastic energy as shown in Fig. 1.31a. Thermal dependency of the Si thermal expansion coefficient has been reported elsewhere by Okada

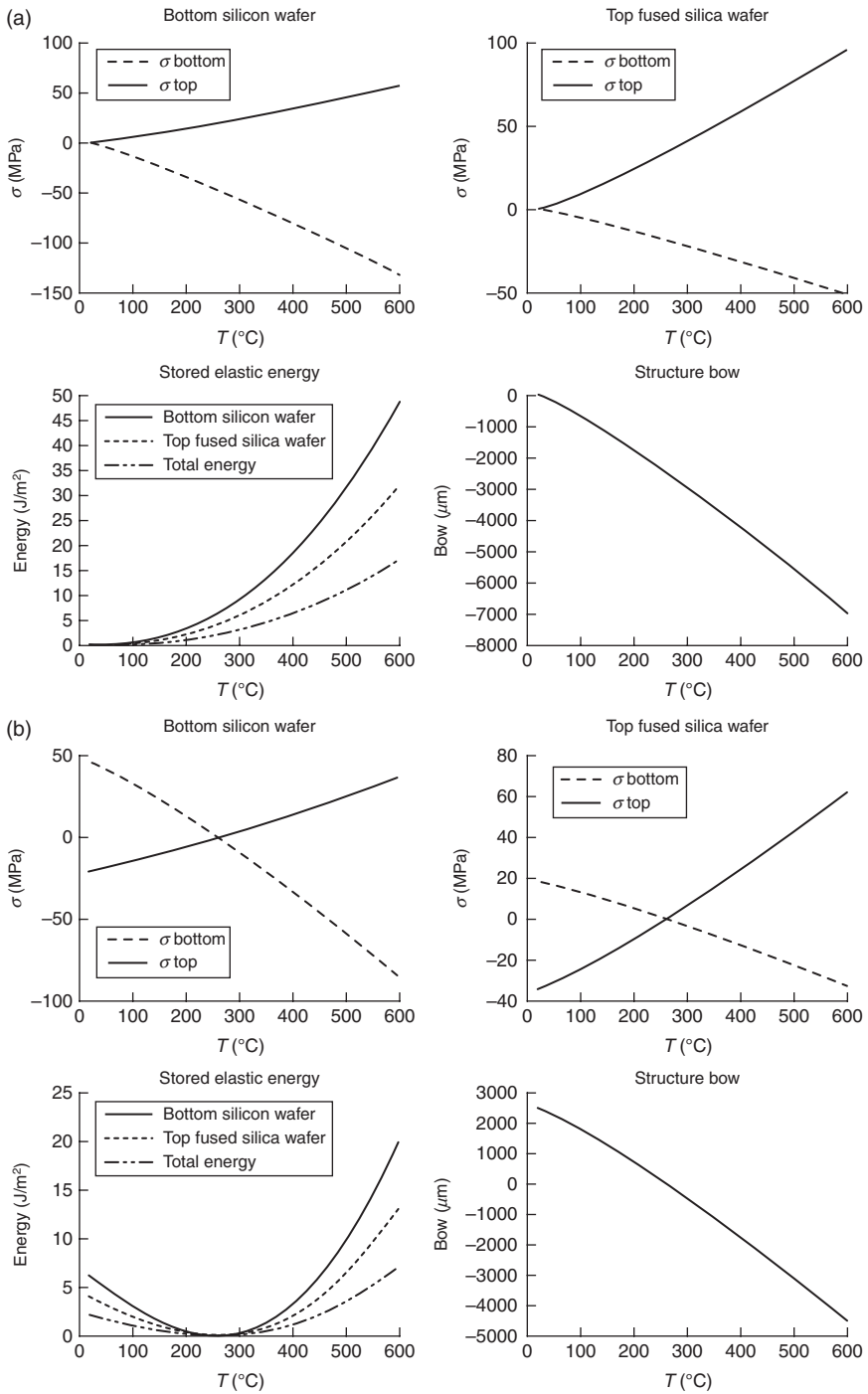
*et al.*¹⁰⁴ In order to minimize the thermal stress at a certain temperature it is possible to impose a pre-stress by bonding curved wafers. With such 'curved bonding' the unstressed temperature is no longer at RT, as shown in Fig. 1.31b.

It is possible to obtain comparable results by bonding at a specific temperature, referred to as 'hot bonding' (Fig. 1.32a), because such techniques will lead to a stressed structure at RT. For instance, Fig. 1.32b shows a bent structure at RT from 350°C hot bonding between a silicon wafer and a fused silica wafer. It is worth noting that the bow of the heterostructure shown in Fig. 1.32b is around 2.4 mm. Analytical simulation would suggest it should be around 4 mm. The difference is due to the small-deformation assumption in the previous theoretical model. If the heterostructure bow is calculated using finite elements with an assumption of large mechanical deformations (as required especially with 200 mm diameter wafers), a value of 2.5 mm is obtained, very close to the experimental observation.

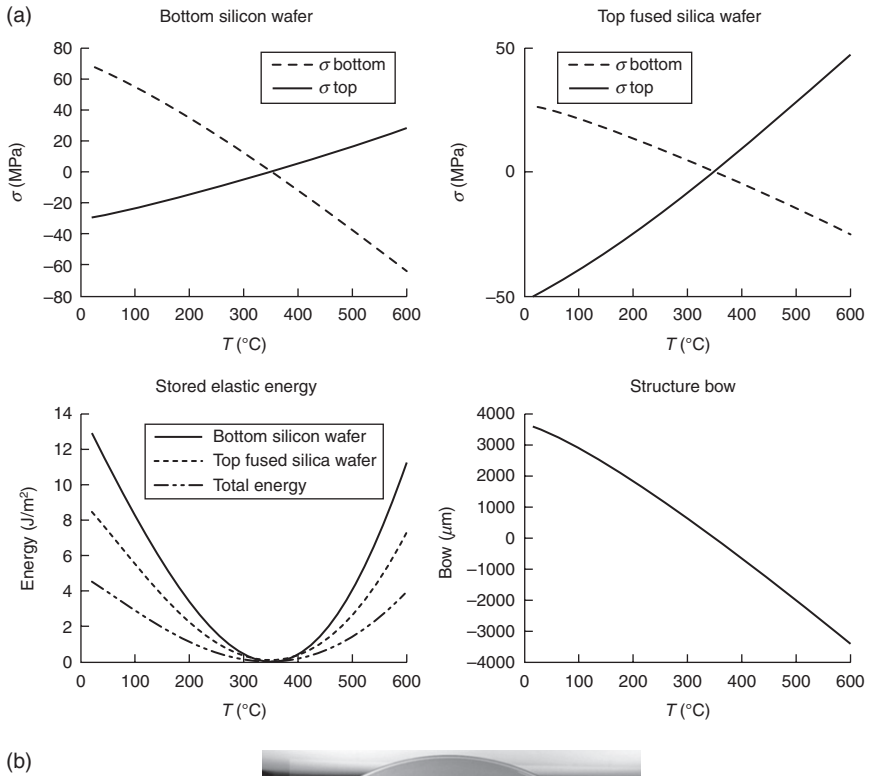
1.10.3 Application to layer transfer technique

The methods described above, for minimizing heterostructure stress and deformation and avoiding breakage of heterostructures during thermal treatment, should be considered in layer transfer processes based on ion implantation and thermal splitting and in subsequent application processes. Indeed, without thermal stress minimization, such layer transfer techniques could not be applied to any heterostructures. For example, silicon-fused silica heterostructures can withstand annealing at 600°C, but if the silicon wafer is implanted prior to bonding, annealing at 400°C in order to induce splitting leads to heterostructure breakage. As shown in Fig. 1.33a, this is due to the sudden energy release at the splitting temperature. One way to limit this energy relaxation is to perform a hot bonding at a temperature close to the splitting temperature (Fig. 1.33b), or to perform a curved bonding. It is thus possible to obtain a thin silicon layer on top of a fused silica wafer either after bonding using curvature radius of about 2 m and thermal splitting at 350°C (Fig. 1.34a) or 350°C hot bonding and splitting at 400°C (Fig. 1.34b). The hot-bonded heterostructure exhibits more transfer defects due to reduced bonding strength. Nevertheless, such a process is easier to implement in industrial equipment. Other types of heterostructures can also be obtained. For example, thin silicon layers on sapphire substrates (SOS) can be elaborated following similar processes, as can thin silicon carbide layers on silicon substrates.

Co-integration of III-V materials onto silicon is also very attractive for microelectronics and optoelectronics. Different approaches can lead to such co-integration. For instance, a thin single-crystal germanium layer can be

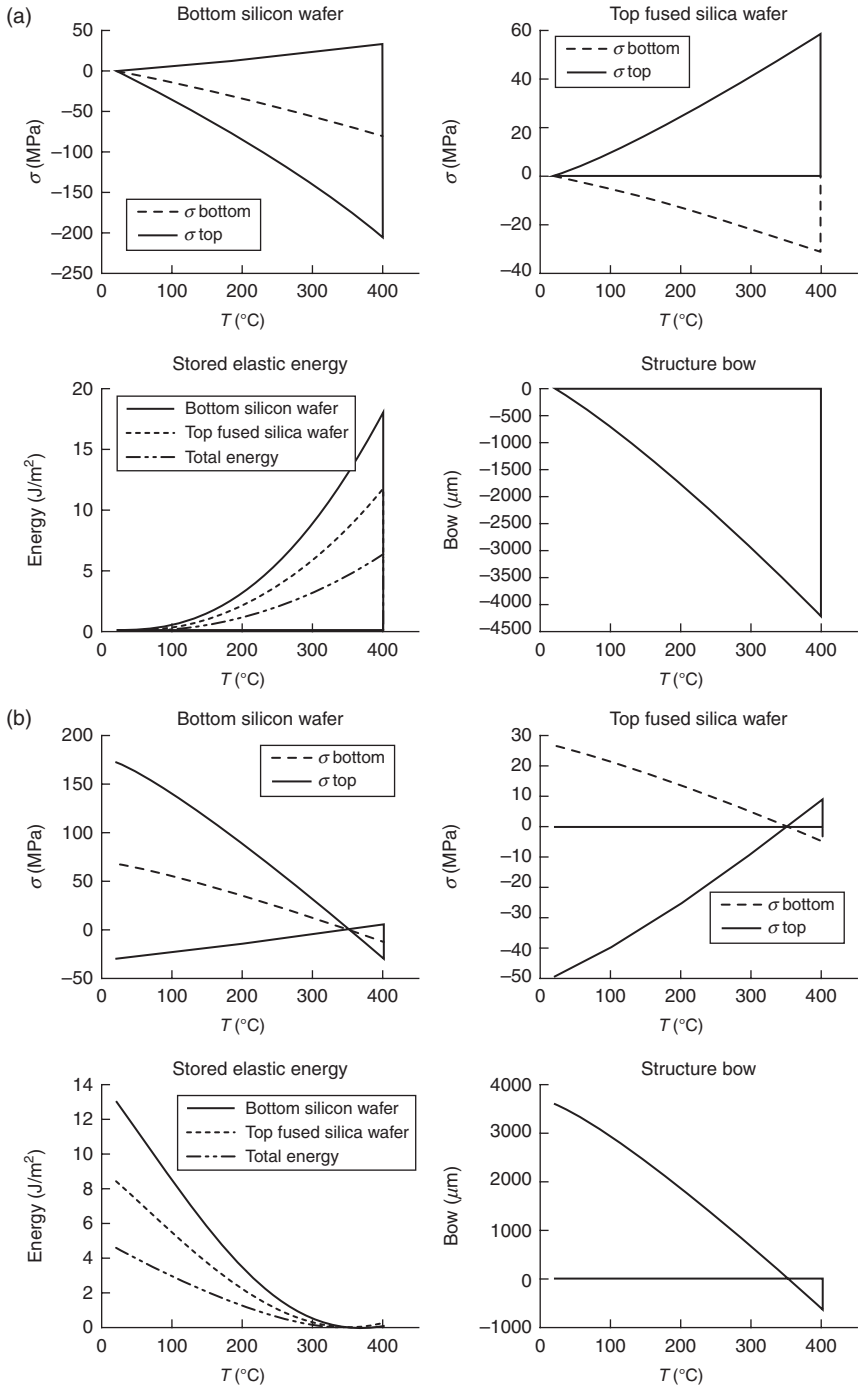


1.31 (a) Simulation of stress evolution from RT to 600°C for a silicon wafer bonded onto a fused silica wafer. (b) The same simulation for bonding of curved wafers, whose curvature radius is about 2 m.

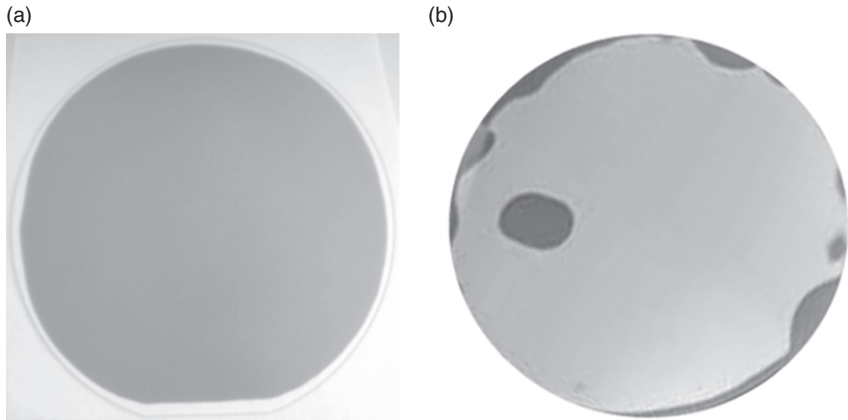


1.32 (a) Simulation of hot bonding at 350°C between a silicon wafer and a fused silica wafer. (b) Bonded heterostructure at room temperature with a bow around 2.4 mm.

elaborated onto a silicon substrate and serve as a seed layer for GaAs epitaxial growth. In order to co-integrate silicon and III–V technologies more easily, an additional silicon layer can be transferred onto the germanium layer and partially engraved to allow III–V epitaxial growth.



1.33 (a) Simulation of splitting at 400°C in a silicon wafer bonded at room temperature onto a fused silica wafer. (b) Identical splitting simulation after hot bonding at 350°C.



1.34 Thermal splitting of a silicon wafer onto a fused silica wafer (a) at 350°C after bonding using curvature radius of about 2 m and (b) at 400°C after 350°C hot bonding.

III–V co-integration can also be obtained through bonding and thinning processes. III–V epitaxial layers grown onto III–V matched substrates are thus bonded onto silicon substrates. After removing the initial III–V back-side substrate, all the surface of the III–V layer lies down onto the silicon substrate. This layer is locally engraved in order to build optical devices, for instance. Obviously, such a co-integration would be made even more attractive by bonding small III–V dies, located only where they are needed, instead of bonding a full wafer surface, so as to save most of the initial donor substrate, which can be very expensive.

1.11 Conclusion

The fabrication of SOI materials is a domain where a very broad scope of material fabrication techniques has been attempted. Techniques ranging from direct implantation of oxygen to epitaxy and direct bonding have been used. The most competitive has proven to be the light ion implantation and transfer technique, so-called Smart Cut™ technology. The bonding stage in this technology is one of the most crucial. The physics and chemistry of bonding also relate to areas ranging from interface chemical reactions to contact mechanics. The need to obtain strong adhesion calls for control of all the physico-chemical parameters of bonding and thus leads to a variety of characterization techniques.

Access to the buried interface is a difficulty for most techniques, often requiring long stages of sample preparation. Techniques like IR spectroscopy or X-ray interfacial reflection for the measurement of the interface

gap need less preparation and are well suited for the study of interfacial chemistry and physics, respectively. The light ion implantation and the splitting subsequently induced in order to transfer thin single-crystal layers are also critical steps of Smart Cut™ technology. The physical mechanisms that make splitting effective derive from the location of implanted ions, platelet formation and microcrack development, according to the total thermal budgets used for splitting.

The different techniques and knowledge developed in the mainstream of SOI fabrication are applicable to more complex heterostructures, where stress management adds a level of complexity that can now be taken into account. Thanks to its generic character, the Smart Cut™ process is adaptable to the fabrication of many and varied innovative engineered structures and it should remain open to future technologies. SOI wafers will continue to be very attractive for developing advanced microelectronics and microtechnological devices as long as they can enhance device performance. Moreover development of more effective fabrication techniques has been a constant driver of technology over the past 30 years.

1.12 Acknowledgments

Acknowledgements are due to the CEA and SOITEC teams involved in the development of SOI technology.

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Characterization of the electrical properties of advanced silicon-on-insulator (SOI) materials and transistors

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Abstract: The characterization of nanosize silicon-on-insulator (SOI) materials and devices demands special attention. This chapter shows that conventional measurement techniques need to be replaced, or at least updated. The accurate interpretation of experimental results is based on new models, able to account for multiple interfaces and channels. Informative examples are selected from various structures including ultrathin SOI wafers, fully depleted metal-oxide-semiconductor field-effect transistor (MOSFETs), and multiple-gate and nanowire transistors.

Key words: characterization, complementary metal-oxide-semiconductor (CMOS) scaling, silicon-on-insulator (SOI) wafer, buried oxide (BOX), ultrathin, metal-oxide-semiconductor field-effect transistor (MOSFET), pseudo-MOSFET, nanoscale.

2.1 Introduction

Complementary metal-oxide-semiconductor (CMOS) scaling uses nanosize layers and multiple-gate transistors operating in full depletion (FD) mode to improve electrostatic control. Enhanced transport properties are needed for higher speed and decreased power consumption. Current Si films and buried SiO₂ (BOX) are ultrathin, reaching the sub-10 nm range. Alternative semiconductor films (strained Si, Ge, SiGe, GaN, III-Vs) and buried dielectrics (ONO, diamond, glass, AlN, etc.) are also being adopted. As a result, the term silicon-on-insulator (SOI) has now come to mean 'semiconductor on insulator'. Metal-oxide-semiconductor field-effect transistor (MOSFET) technology is changing dramatically. SOI metal-oxide-semiconductor (MOS) transistors combine an ultrathin body, thin BOX, short high-K/metal gates, and strain. Future devices using this technology include the multiple-gate MOSFET,¹ tunnel field-effect transistor (FET),² junctionless transistor,³ 3D circuits,⁴ and nanowire FETs.⁵ Even bulk transistors now use a FinFET configuration and operate in FD mode.⁶

In these new structures, the evaluation of simple parameters, such as carrier mobility and lifetime, threshold voltage, or interface traps, is no longer straightforward. Multi-channel coupling and nanosize effects modify not only the measurement value, but also the meaning of classical parameters. Nevertheless, materials specialists, process engineers, and circuit designers are increasingly demanding accurate electrical parameters needed for wafer optimization, process development, and compact models. In this chapter, recent developments are reviewed by suggesting guidelines for appropriate characterization strategies and accurate interpretation of the experimental data.

2.2 Conventional characterization techniques

The evaluation of electrical properties in semiconductor films with nanometer thickness is impossible with conventional methods, as the layers are fully depleted. No current can flow between two probes on the wafer surface, so making sheet resistance, spreading resistance, and Hall measurement techniques unusable. The application of a substrate bias makes electrical evaluation possible though and this is the basis for the techniques reviewed in this chapter.

Conventional techniques are more or less efficient for the characterization of SOI wafers with relatively thick Si and BOX layers:⁷

- In relatively thick films, *Hall* and *Van der Pauw* experiments give independent values of carrier mobility and concentration.
- *Four-probe* measurements indicate the sheet resistance and film resistivity.
- *Spreading resistance* in beveled samples shows the in-depth resistivity profiles in film and substrate.
- The *surface photo-voltage* technique is used to determine the diffusion length of minority carriers.
- *Photo-conductivity* serves to extract the carrier recombination lifetime.
- *Deep-level transient spectroscopy (DLTS)* and *photo-induced current transient spectroscopy (PICTS)* enable the detailed investigation of deep-level traps.

In ultrathin, fully depleted films, the accommodation of these techniques needs substrate biasing and corresponding models.

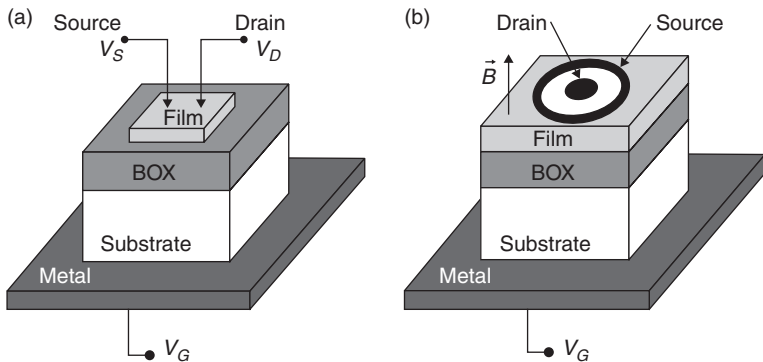
Although the MOS capacitance and conductance can be measured in SOI wafers, the interpretation of the data is rendered difficult by a number of additional parameters: full film depletion, contributions of the two BOX interfaces, and different doping levels in film and substrate. For example, when the film is biased through a top metal contact while the substrate is

grounded, depletion regions form on either side of the BOX.⁷ Plain MOS–SOI capacitors, where two oxides and three interfaces coexist, present even greater challenges to characterization. In principle, an additional contact to the film allows independent probing of the front and back interfaces. However, the large series resistance of the film makes the data inaccurate. C–V measurements are thus not recommended in thin SOI.

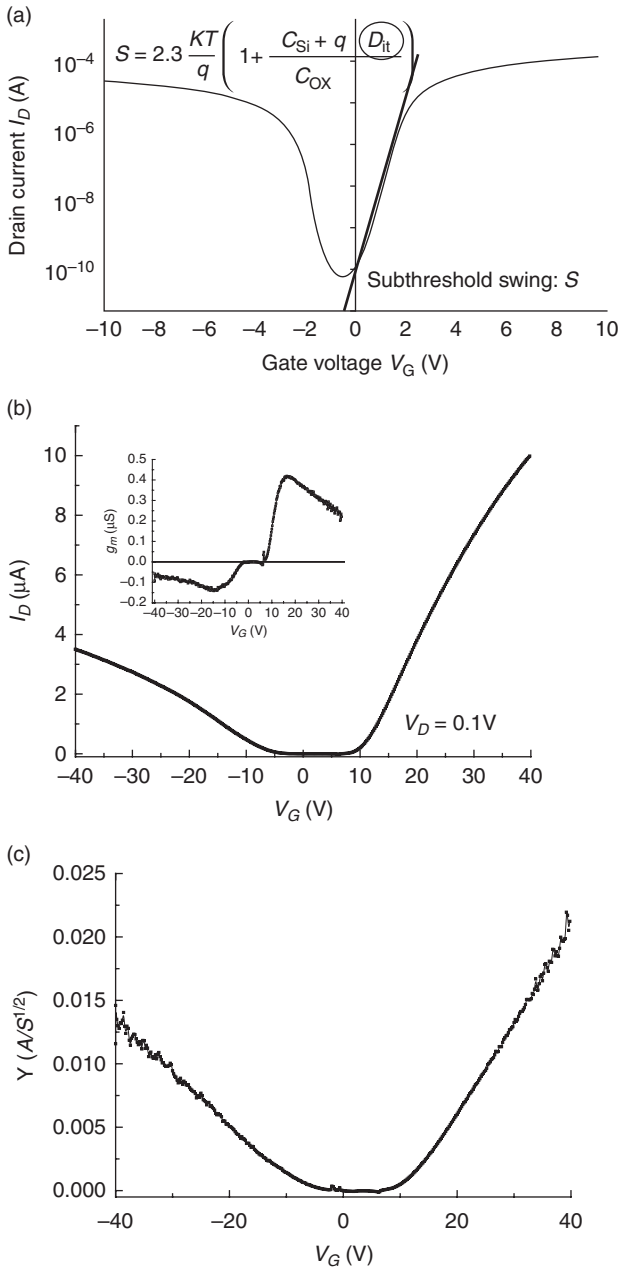
2.3 Characterization of SOI wafers using the pseudo-metal oxide semiconductor field effect transistor (MOSFET) technique

The pseudo-MOSFET (Ψ -MOSFET) technique enables *in situ* wafer inspection before CMOS device processing.^{7,8} It uses the intrinsic upside-down MOS structure in SOI: the substrate plays the role of gate, the BOX is promoted as gate oxide, and two pressure probes serve as source and drain (Fig. 2.1a). Electron or hole channels are activated at the film–BOX interface according to the positive or negative gate bias V_G . Two different Ψ -MOSFET configurations have been tested: point-contact transistor (Fig. 2.1a) and Corbino disk (Fig. 2.1b) with mercury contacts or evaporated metals. Pressure-adjustable probes are preferred, because the contacts are always ohmic.

The $I_D(V_G, V_D)$ characteristics are similar to those in fully-processed MOSFETs. The off-current region in Fig. 2.2a and 2.2b indicates a fully depleted film. Standard MOSFET models and extraction methods are available for parameter extraction. The subthreshold slope yields the density of interface traps D_{it} (Fig. 2.2a), reflecting the quality of the film–BOX interface.



2.1 (a) Point-contact and (b) Corbino Ψ -MOSFET configurations. The current at the film–BOX interface is modulated by the bias applied on the substrate.



2.2 Drain current versus back-gate voltage characteristics in SOI wafer with 20 nm film and 145 nm BOX. (a) Weak inversion; (b) strong inversion. The inset shows the transconductance curve. (c) Corresponding Y-function dependence on V_G for electron ($V_G > 0$) and hole ($V_G < 0$) channels, as predicted by Equation [2.3].

Drain current and transconductance in the ohmic region (at low drain bias V_D) are given by:

$$I_D = f_g C_{OX} V_D \frac{\mu_0}{1 + \theta(V_G - V_T)} (V_G - V_T) \quad [2.1]$$

$$g_m = \frac{dI_D}{dV_G} = f_g C_{OX} V_D \frac{\mu_0}{[1 + \theta(V_G - V_T)]^2} \quad [2.2]$$

where C_{OX} is the BOX capacitance, μ_0 is the low-field mobility, and θ is the mobility reduction factor. In p-type films, V_T stands for either the threshold voltage (electron channel) or the flat-band voltage (hole channel). The geometrical factor, f_g , accounts for non-parallel current lines. Calibration with 4-point probe measurements and numerical simulations give $f_g = 0.75$.⁸ The parameter extraction proceeds from the Y-function,⁹

$$Y = \frac{I_D}{\sqrt{g_m}} = \sqrt{f_g C_{OX} \mu_0 V_D} (V_G - V_T) \quad [2.3]$$

that has a linear variation for $V_G > V_T$ (Fig. 2.2c). The intercept of $Y(V_G)$ with the V_G axis yields V_T (or V_{FB}), and the low-field mobility for electrons or holes is extracted from the slope. The degradation factor, θ , can be obtained from the linear slope of $1/\sqrt{g_m}$ versus V_G curve (Equation [2.2]).

The pressure applied on the probes (10–100 g in Jandel equipment) is adjusted for each material, to lower the series resistance while avoiding probe penetration through the BOX. The conversion from Schottky to ohmic contacts is caused by crystal defects generated by the probes. The probes induce small craters (~100 nm deep and ~10 μm wide) and lower the Schottky barrier. A clear correlation exists between probe pressure, crater size, and series resistance.¹⁰ Probe-generated defects do not influence the extracted parameters, as the inter-probe distance is large (1 mm).

In industry, the Ψ -MOSFET is of utmost importance for monitoring the quality and stability of the wafer fabrication process. In research, it is a very fast method for detecting defects and optimizing new materials. The Ψ -MOSFET also serves for on-wafer measurement of the BOX charges induced by radiation effects, and for detecting charges intentionally deposited on the wafer surface (for bio-sensor applications).

Recent measurements have been dedicated to the evaluation of ultrathin SOI wafers. In films thinner than 50 nm, the threshold voltage increases significantly because the coupling between the buried channel and the surface

defects is amplified. Once the wafer surface is passivated, the threshold voltage recovers the expected values.¹¹ A similar effect leads to apparent mobility degradation with decreasing film thickness.¹² The vertical field increases in thinner films, induced by the potential difference between the free surface charge and channel. This extra field is not included in Equations [2.1]–[2.3]: the Y-function only describes the gate-induced field. As a consequence, the low-field mobility is no longer measured at ‘low-field’. The mobility decrease with thickness is an artifact, simply explained by the ‘universal’ mobility curve, and does not indicate any degradation of the film–BOX interface in ultrathin SOI. The Ψ -MOSFET models have been revised to include the surface and thickness effects.¹³

In SOI with thin BOX (10–20 nm), the potential drop at the substrate–BOX interface cannot be ignored without generating characterization errors. The quality of the BOX–substrate interface and its biasing state (inversion, depletion, accumulation) modify, via electrostatic coupling, the properties of the channel above the BOX. Appropriate three-interface models have been formulated using analytical derivations and equivalent capacitance circuits.¹⁴

Ψ -MOSFET measurements in germanium on insulator (GeOI) wafers have demonstrated an outstanding improvement in hole mobility with increased germanium content. However, electron mobility decreases proportionally, which inspired the co-integration of p-type Ge and n-type Si devices.¹⁵ In strained SOI, the data demonstrated the beneficial effect of biaxial stress for the enhanced mobility of both electrons and holes. Even silicon on sapphire (SOS) wafers can be probed after thinning the sapphire substrate to 50 μm or less in order to limit the gate voltage to around 1 kV. Well-behaved Ψ -MOSFET characteristics were obtained, and used to benchmark the impact of film growth conditions on SOS wafers.¹⁶

Heavily doped (10^{19} – 10^{20} cm^{-3}) films are important for achieving low-resistance source/drain terminals, adjusting the threshold voltage, and fabricating junctionless MOSFETs. The Ψ -MOSFET is still effective although the $I_D(V_G)$ curves are qualitatively different from those in Fig. 2.2b. There is no off-current region, because the film cannot be fully depleted. Most of the current flows through the film volume. The gate controls the depletion region that forms at the film–BOX interface. The extrapolation of the linear current variation to zero current yields a hypothetical threshold voltage, from which the doping level and the carrier mobility in the film can be extracted.¹⁷ Unlike the Hall effect, the Ψ -MOSFET yields carrier concentration and mobility without applying a magnetic field. The gate can also induce an accumulation channel at the interface, increasing the total current. A revisited Y-function accounts only for the excess current in accumulation. The extracted ‘surface’ mobility differs from the ‘volume’ mobility.

2.4 Developments in the pseudo-MOSFET technique

Since its discovery 20 years ago, the Ψ -MOSFET has been considerably enriched by adopting MOSFET techniques.

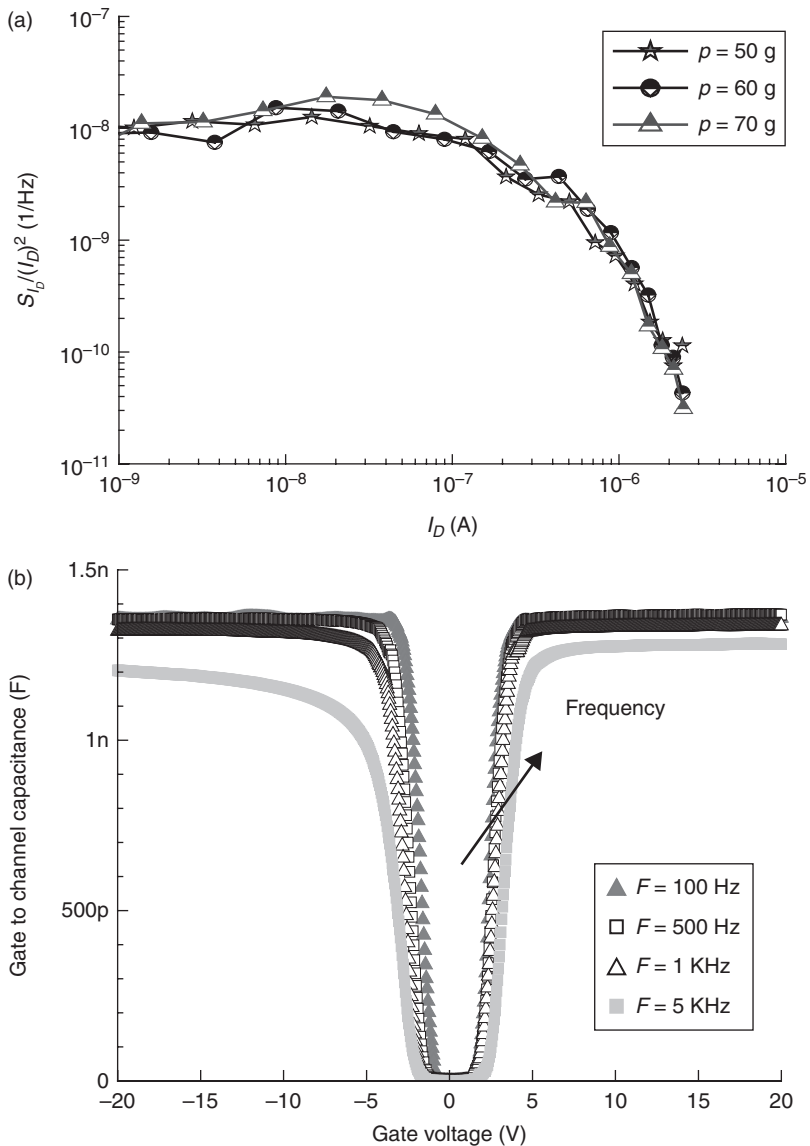
Geometrical magnetoresistance – Ψ -MOSFETs with Corbino configuration (Fig. 2.1b) have been tested under high magnetic fields, B , perpendicular to the wafer surface. Due to circular symmetry, the Hall effect is suppressed, leading to a ‘geometric’ magnetoresistance (MR): $R_B/R_0 = 1 + \mu_{MR}^2 B^2$. The channel resistance, $R_B = V_D/I_D$, is plotted as a function of B .² The slope of the resulting line yields the MR mobility, μ_{MR} , for each gate voltage.¹⁸ While strong magnetic fields are needed (>10 T), the MR method is exceptionally accurate. The extracted μ_{MR} value excludes assumptions regarding the device size, geometrical factor, f_g , or film/BOX thickness. The comparison between the MR mobility and effective mobility (determined at $B = 0$) illustrates the scattering mechanisms at variable electric field, temperature, and film thickness.¹⁸

Low-frequency noise is a more evolved method to assess the density of interface and border traps.¹⁹ The noise spectra, $S_i(f)$, indicate $1/f$ noise. The normalized current spectral density, S_i/I_D^2 , versus drain current (Fig. 2.3a) shows a plateau in weak inversion and a decrease in strong inversion, which is the signature of carrier number fluctuations.²⁰ Noise magnitude is independent of probe pressure, suggesting the prevalence of interface quality rather than series resistance or probe-induced damage localized around the contacts.

Split C-V measurements, frequently used to determine the effective carrier mobility in MOSFETs, are also feasible in Ψ -MOSFETs.²¹ Capacitance is measured between the gate and interconnected source/drain contacts. The capacitance plateau in Fig. 2.3b corresponds to BOX capacitance. The asymmetry on the electron and hole sides is due to the lateral spreading of carriers (beyond the Ψ -MOSFET contacts) and the time constants needed to build up the accumulation and inversion layers. The integral of the C-V curve between 0 V and V_G yields the inversion charge. Effective mobility is calculated as a function of V_G from the corresponding drain current value. Mobility, measured by the low-frequency split C-V method, shows excellent agreement with the Y-function results.

Transient current monitoring, after the gate is pulsed in inversion, is useful in evaluating carrier lifetime.⁸

In summary, the Ψ -MOSFET is the method of choice for characterizing the electrical properties of SOI wafers. It is fast, simple, inexpensive, and reliable. The range of materials that can be probed is vast: semiconductor film thickness from 5 μm down to at least 10 nm and dielectric thickness between 50 μm and below 10 nm. The method is adaptable to any SOI-like structure including nanowires and graphene on insulator.



2.3 (a) Normalized noise power spectral density versus drain current in Ψ -MOSFET for various probe pressures. (Source: Adapted from Diab *et al.*²⁰) (b) Split C-V capacitance curves at different frequencies (88 nm film and 145 nm BOX). (Source: Adapted from Reference 21: *Solid-State Electronics*, **90**, Diab *et al.* 'A New Characterization Technique for SOI Wafers: Split C(V) in Pseudo-MOSFET Configuration' 127-133, copyright (2013), with permission from Elsevier.)

2.5 Conventional methods for the characterization of FD MOSFETs

The material configuration of SOI MOSFETs presents significant technical challenges to their characterization: ultrathin FD film, intermediate BOX, three stacked interfaces (high-K/film, film–BOX, and BOX–substrate), floating body, etc. While conventional characterization methods are either no longer applicable or need specific tailoring, novel techniques can be implemented. The properties of SOI transistors are inferred from static/dynamic current measurements. Mobility, threshold voltage, swing, and lifetime are determined for the front and back channels, separately or in coupled mode (depletion at opposite interface).

The subthreshold slope notionally provides the density of interface traps. However, in modern MOSFETs, with 1 nm equivalent oxide thickness, the resolution is poor because gate capacitance exceeds interface trap capacitance ($C_{ox} \gg qD_{it}$), leading to a nearly ideal subthreshold swing (~ 60 mV/decade at 300 K). A promising solution is to measure the *back channel* swing that may be more affected, via coupling mechanism, by the density of *front-interface* traps.²²

Threshold voltage and carrier mobility are determined with the Y-function (Equation [2.3]), that can be updated to include a non-linear mobility degradation factor.⁷ Alternatively, the double-derivative method can be used: the threshold voltage is defined as the gate voltage for which the second derivative of drain current reaches a peak.²³ To accurately determine the double derivative, measurements should be conducted with very small V_G steps. Other popular methods are less precise in SOI. For example, threshold voltage extraction by linear extrapolation of the $I_D(V_G)$ curve is affected by strong series resistance effects. Definition of V_T by a constant current criterion (~ 0.1 $\mu\text{A}/\mu\text{m}$ for $V_D = 50$ mV) is not better, particularly when a parasitic current flows at the opposite interface.⁷

A unique advantage of SOI MOSFETs is the possibility to compare *in situ* the properties of high-K and SiO_2 dielectrics without processing dedicated lots. Such a comparison simply consists of probing the front and the back channels of the same transistor.²⁴ The electron and hole mobilities are found to be systematically lower ($\sim 50\%$) at the front interface (Si/high-K) than at the back interface (Si/ SiO_2). As usual, low-temperature measurements are very helpful in providing details and identifying the physical mechanism: carrier scattering by remote Coulomb centers, located in the high-K stack.²⁵

Effective channel length and width are normally evaluated by comparing devices with variable geometry. Several issues have to be considered:

- Effective length can be slightly different at front and back channels.
- The two channels do not have the same series resistance.

- While varying the channel length, the transistor mode of operation can change from partial to FD and *vice versa*. For example, a long MOSFET is partially depleted if the vertical depletion region, controlled by the gate, is thinner than the film. In very short devices, the lateral depletion regions of the source and drain junctions enhance the overall depletion, unexpectedly turning the device into FD mode.²⁶ However, the opposite effect is observed in FD MOSFETs with pockets: long devices are indeed FD, whereas short devices become partially depleted due to the encroachment of the two highly doped pocket regions.²⁷

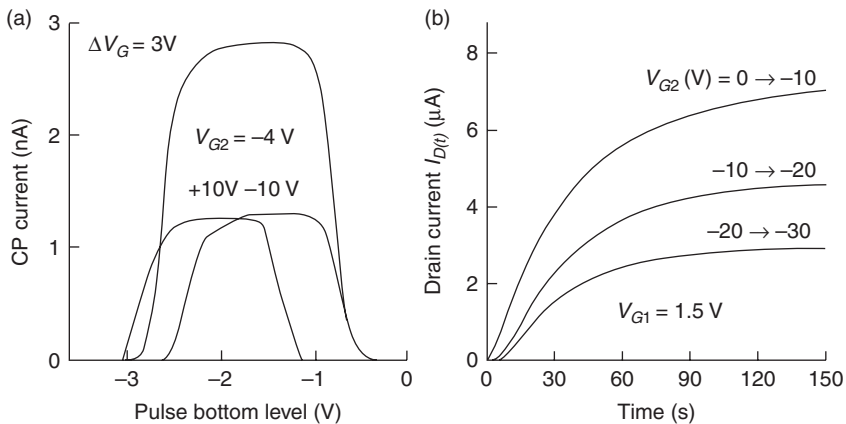
2.6 Advanced methods for the characterization of FD MOSFETs

Charge pumping (CP) is a very sensitive characterization method of interface traps. The gate is repeatedly pulsed from inversion (where the minority carriers are trapped on the interface states) to accumulation (where the trapped carriers recombine with majority carriers). The carrier recombination results in CP current in the body terminal, proportional to the trap density and frequency. The adaptation of CP to SOI transistors requires a body contact or gate-controlled p-i-n diodes, where electrons and holes are promptly supplied by the n and p contacts, respectively.²⁸ Measurement is usually performed by varying the bottom level of the pulse while keeping both the pulse magnitude $|\Delta V_G|$ and frequency fixed. Figure 2.4a reproduces a typical rectangle-like CP curve: the left- and right-hand edges correspond to $(V_T - |\Delta V_G|)$ and V_{FB} , respectively, whereas the plateau level yields the trap concentration. This CP signature is modified according to the back-gate bias. In depletion, the back interface traps are pumped simultaneously with the front traps and lead to an excess CP current from which their density can be extracted.

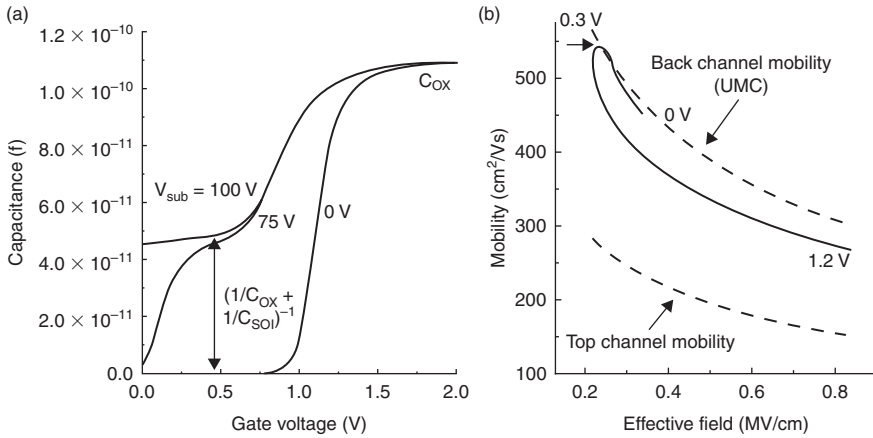
In MOSFETs, $1/f$ noise originates from fluctuations in carrier number (via trapping) and/or mobility. Interface coupling alters the noise spectra, primarily by adding the noise generated at the back interface.⁷ In small-area transistors, there are only very few traps, and single-carrier trapping is detectable in the time domain: small pulses appear superimposed on the average drain current. The duration of such *random telegraph signals* (RTS) reflects the trapping/emission time constants of the trap.¹⁹ For a complete view of trapping mechanisms, back channel and front channel measurements are compared. RTS also served to prove the prevalence of tunneling current in SOI tunneling field-effect transistors (TFETs) by showing that only a discrete number of traps are active in a large device.² The tunneling rate is indeed affected by the trapping process at the Si/SiO₂ interface just above the tunneling junction that is very narrow (~10 nm) and experiences few trapping events.

Transient current monitoring is conducted by inducing a temporary deficit or excess of majority carriers in the isolated body. Equilibrium is reached by carrier generation-recombination mechanisms. When the transistor is switched from depletion to strong inversion, the depletion depth extends, and the released majority carriers accumulate at the bottom of the film. The body potential increases, the threshold voltage decreases, and excess current (overshoot) occurs. Subsequent carrier recombination brings the current to equilibrium. The duration of the transient is processed with Zerbst-like techniques and provides the recombination carrier lifetime and surface recombination velocity.⁷ The reciprocal effect (deficit of majority carriers and current undershoot triggering carrier generation) happens when the gate is switched from strong to weak inversion. In FD MOSFETs, two gates are operated (Fig. 2.4b): one gate is biased in inversion, whereas the opposite gate is pulsed into accumulation. The body potential instantly drops, lowering the inversion charge and current. Current relaxation back to equilibrium (undershoot) involves carrier generation. In very short MOSFETs, the junctions govern the extraction/supply of majority carriers, thus reducing the transient time.

Split C-V measurements provide data on effective carrier mobility as a function of electric field, gate bias, or inversion charge. The capacitance between gate and source/drain terminals is nearly zero when the front interface is depleted. The capacitance increases with V_G as the inversion charge builds up (Fig. 2.5a). A plateau corresponding to C_{OX} is reached when inversion



2.4 (a) Front-gate charge pumping current versus base level of the gate pulse for various back-gate voltages; the film–BOX interface is in accumulation, depletion or inversion. MOS p-i-n diode with 2 μm gate length, 150 nm thick film, and 380 nm thick BOX. $V_{DS} = 0$ V. (b) Front channel drain current transients after pulsing the back gate into accumulation. N-channel SOI MOSFET with 150 nm thick film and 380 nm thick BOX. $V_{DS} = 0.1$ V.



2.5 (a) Split C-V curves in FD n-channel SOI MOSFET for various back-gate voltages. The transistor features 16 nm thick film and 400 nm thick BOX. (Source: Adapted from Ohata *et al.*²⁹) (b) Unusual electron mobility variation with effective field in FD SOI MOSFET. The bottom gate is set in inversion ($V_{G2} = +25$ V for 150 nm BOX) and the front gate increases from depletion to strong inversion. Back channel mobility is assumed to be ideal (Si-SiO₂ interface), matching the universal mobility curve (UMC), whereas the mobility at the top high-K/Si interface is half. 20 nm thick SOI film and 1 nm thick gate dielectric. (Source: Adapted from Rodriguez *et al.*³⁶)

capacitance exceeds oxide capacitance. Knowing the inversion charge (from the integral of the $C(V_G)$ curve) and the related drain current, the carrier speed (i.e., their effective mobility) is deduced. In order to determine film thickness, the substrate is biased such as to form a strongly inverted back channel (100 V in Fig. 2.5a): the minimum capacitance is no longer zero, as it corresponds to the series combination of gate oxide and FD film capacitances. Even more informative is the case of intermediate back-gate voltage (75 V in Fig. 2.5a). A double C-V curve is obtained where the left region reflects the formation of the back channel before the front channel. This curve gives, in one measurement, carrier mobility at both channels.²⁹

Geometric magnetoresistance is the most pristine method for measuring carrier mobility in short MOSFETs, as accurate values of effective channel length or oxide thickness are not needed. A strong magnetic field is applied perpendicular to the wafer. If the transistor aspect ratio is large enough ($W/L \geq 10$), the Hall field is short-circuited as in a Corbino disk (Section 2.4) and the MR reaches $R_B/R_0 = 1 + \mu_{MR}^2 B^2$. The slope of the channel resistance versus squared magnetic field yields the effective mobility from weak to strong inversion.³⁰

Self-heating in SOI MOSFETs is caused by the poor thermal conductivity of the BOX. The increase in body temperature is evaluated by comparing

$I_D(V_D)$ characteristics measured in static and pulsed modes. For better resolution, special MOSFETs with two independent body (or gate) contacts are utilized.³¹ Variation in body resistance is monitored as a function of dissipated power. Prior calibration of the body (or gate) resistance on a hot-chuck enables determination of body temperature.

2.7 Characterization of ultrathin SOI MOSFETs

State-of-the-art MOSFETs feature an ultrathin (5–10 nm) and undoped body, thin BOX (10 nm), and decananometer channel length. *Drain-induced barrier lowering* (DIBL) is a notorious short-channel effect that decreases the threshold voltage at higher V_D by reducing the source-to-body injection barrier. In FD MOSFETs, an additional and more prominent cause of V_T shift is *drain-induced virtual substrate biasing* (DIVSB). DIVSB accounts for the penetration of the electric field from drain through BOX and substrate. This fringing field increases the potential at the film–BOX interface and, via coupling, lowers V_T .³² DIBL and DIVSB effects are hard to separate experimentally in a single device. However, comparing transistors with different architectures shows that DIBL is strongly reduced by film thinning, whereas DIVSB decreases in MOSFETs with thinner BOX and ground plane. Detailed measurements demonstrate that no mobility degradation occurs in thinner films ($t_{\text{si}} = 6\text{--}20$ nm).³³ Earlier contradictory reports were probably polluted by series resistance, which does increase in ultrathin films ($R_{\text{SD}} \sim 1/t_{\text{si}}$).

In ultrathin films, ‘as-measured’ front channel properties actually include contributions from the front interface, back interface, BOX and substrate, which are not easy to isolate. It is known that the threshold voltage decreases linearly with back-gate bias from a saturated value in accumulation.³⁴ In sub-10-nm-thick MOSFETs, the plateau value in accumulation disappears due to the *supercoupling* effect;³⁵ when the front channel reaches strong inversion, the back channel is also dragged into inversion. Supercoupling results from the quasi-flat potential distribution between the two interfaces. In other words, inversion and accumulation layers that face each other cannot be accommodated in ultrathin SOI. The routine characterization strategy – that consists in keeping one interface accumulated while evaluating the other one – is no longer applicable.

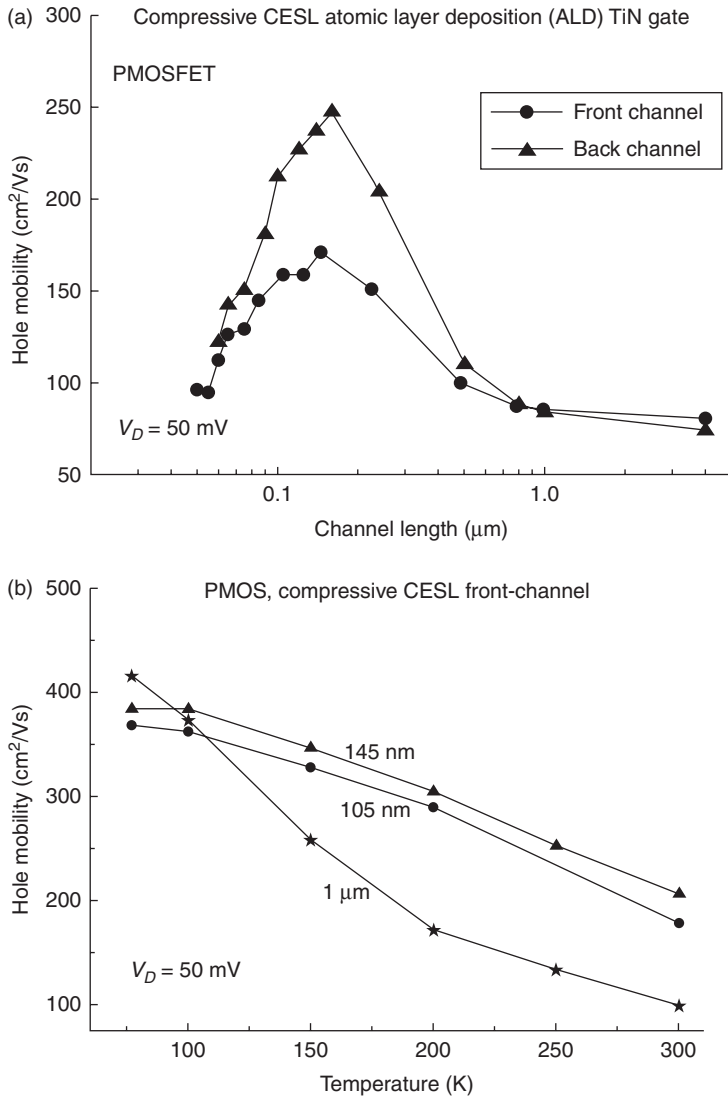
Transconductance now integrates the mobility profile across the film, as carriers flow in the entire body rather than only at the interface. This *volume inversion* makes obsolete the notions of ‘front mobility’ and ‘back channel mobility’; ‘mobility viewed from the front- or back-gate’ now encompasses both. At the experimental level, geometric MR measurements on transistors operated in double-gate and single-gate modes have irrevocably demonstrated that volume inversion brings a clear gain in mobility.³⁰

As a consequence of interface coupling and volume inversion, the ‘universal mobility’ concept (UMC) fails in SOI, because the average electric field can decrease as the inversion charge increases.³⁶ If the back-gate is biased in inversion, the vertical field decreases when the front-gate voltage increases from accumulation to inversion. The effective mobility accounts for the coexistence of two channels, their degree of activation, and the corresponding interface quality. Two distinct carrier distribution profiles – and hence two mobility values – correspond to the same effective field. Figure 2.5b shows the case of SOI MOSFET with higher mobility at the back channel, where the mobility behavior negates the UMC curve.

Strain is an efficient booster of carrier mobility that deserves careful characterization. Figure 2.6a shows a gain in hole mobility of 80% induced by the contact etch stop layer (CESL) in 100 nm long p-channel MOSFETs.²⁵ The mobility dependence on channel length indicates the localization of strain at the channel extremities, as confirmed by mechanical simulations.³⁷ In a long MOSFET, there is no mobility gain because most of the channel remains unstressed. On the other hand, the mobility degradation for devices shorter than 100 nm is attributed to neutral defects, generated during the source/drain implantation or the gate stack processing and concentrated near the source/drain junctions.³⁸ In short transistors, the defective ‘edge’ regions overlap, leading to an increased effective density of defects.

Low-temperature measurements provide additional inputs (Fig. 2.6b). Carrier mobility usually increases at reduced temperature, due to attenuated phonon scattering. This variation is observed only in long channels, whereas in short MOSFETs the mobility saturates and the benefit of strain totally disappears at 77 K. The mobility dependence on gate length and temperature results from competing effects of strain, neutral defects, and Coulomb scattering in the source/drain depletion regions, which are all inhomogeneous along the channel. The combination of these scattering mechanisms with the Matthiessen rule reproduces the experimental data.²⁹

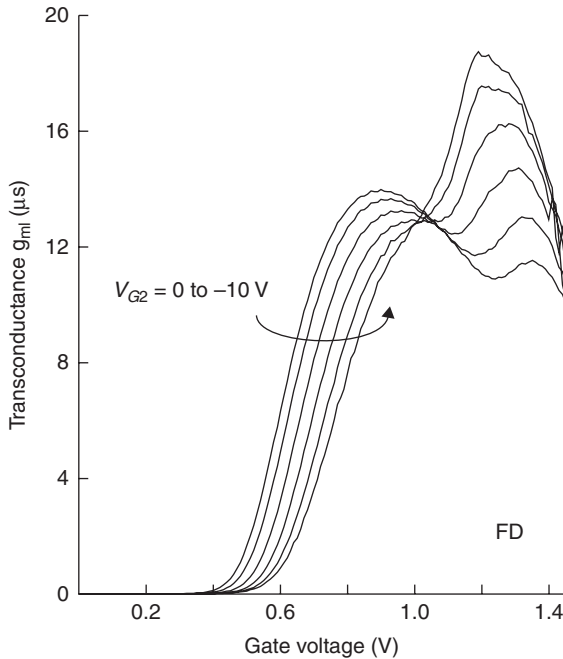
An interesting *gate-induced floating-body effect* (GIFBE) takes place in MOSFETs with ultrathin (<2 nm) oxide. The body potential is defined by the balance between the incoming gate tunneling current (body charging with majority carriers) and the outgoing current (body discharging via junction leakage and carrier recombination). In FD MOSFETs (Fig. 2.7), GIFBE increases the potential at the film–BOX interface, lowering the front channel threshold voltage.³⁹ A second peak in transconductance is observed for $V_G \approx 1.2$ V. When the back interface is driven towards accumulation, the GIFBE peak gradually increases and offsets the mobility-related first peak. It now appears that the transconductance maximum is no longer governed by the carrier mobility, but by the body potential; the mobility extracted from such a curve is overestimated and totally meaningless.



2.6 Hole mobility versus (a) channel length and (b) temperature in fully depleted p-channel SOI MOSFETs with compressive CESL strain and variable gate length. High- k /metal gate stack, 8 nm thick Si film and 20 nm thick Unibond BOX. (Source: Adapted from Pham-Nguyen *et al.*²⁵)

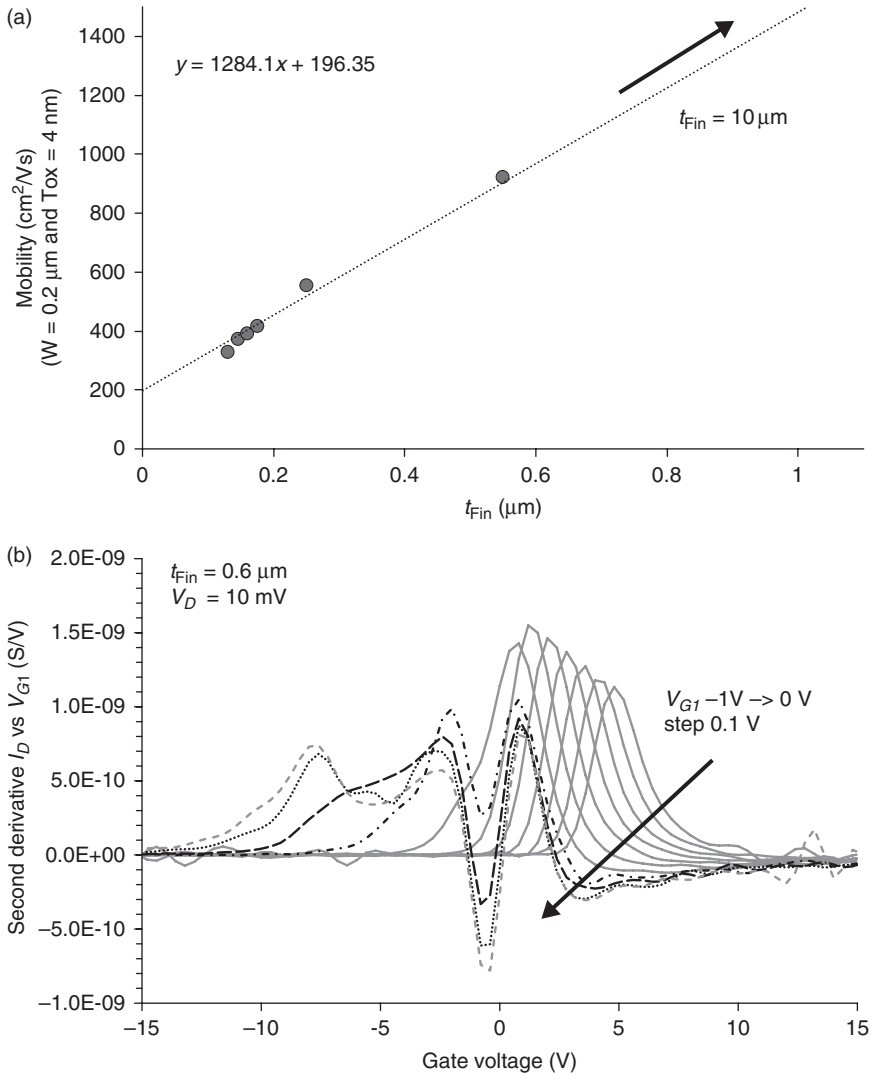
2.8 Characterization of multiple-gate MOSFETs

In a triple-gate FinFET,⁴⁰ a single gate controls three sections of the channel. The discrimination of these channels is possible by probing devices with

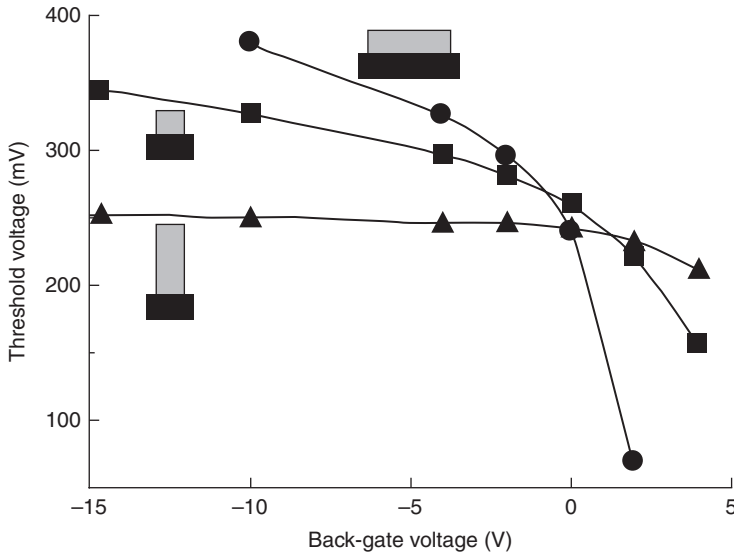


2.7 Transconductance versus gate voltage in FD n-channel SOI MOSFET showing the impact of GIFBE. A more negative substrate bias transforms the double-peak curve into a single-peak curve which no longer defines the low-field mobility. The thicknesses of gate oxide, Si film, and BOX were 1.6, 17, and 145 nm, respectively. $V_D = 0.1$ V and $L = 10$ μm . (Source: Adapted from Reference 39: *Solid-State Electronics*, **48**(7), Cassé *et al.*, 'Gate-induced floating-body effect in fully-depleted SOI MOSFETs with tunneling oxide and back-gate biasing', 1243–1247, copyright (2004), with permission from Elsevier.)

variable fin width, W_F , and constant fin height, H_F . A given parameter A – transconductance peak, mobility, CP current, or noise – includes the contributions of the two lateral channels A_L and of the top channel A_F : $A = 2A_L H_f + A_F W_F$. The experimental curve $A(W_F)$ is linear and yields A_F from the slope and A_L from the intercept at $W_F = 0$. Figure 2.8a exemplifies the mobility extraction. The same procedure can be used to determine the contribution of the back channel activated by the substrate voltage. This technique has revealed that lateral channels which feature different crystal orientation and surface roughness show lower mobility and higher density of traps than top and bottom (Si–BOX) interfaces.⁴¹ Where multiple V_T values are suspected, the second derivative of current (dg_m/dV_G , Section 2.5 and Fig. 2.8b) may efficiently verify the existence of a single peak or several peaks. Note that the Y-function does not work if two or more channels with *different* V_T values operate in parallel.



2.8 (a) Normalized transconductance peak versus fin width in triple-gate SOI FinFETs. The intercept and slope, respectively, indicate the low-field mobility values on the sidewalls and at the top surface of the fin. (b) Second derivative of drain current versus gate voltage in n-channel FinFET. Different peaks correspond to distinct channels, the activation of which depends on substrate bias. $L = 10 \mu\text{m}$, 50-nm-thick Si film, 200-nm-thick BOX. (Source: Adapted from Reference 41: *Solid-State Electronics*, **48**(4), Dauge *et al.*, 'Coupling effects and channels separation in FinFETs', 535–542, copyright (2004), with permission from Elsevier.)



2.9 Threshold voltage as a function of substrate bias in n-channel triple-gate FinFETs with wide, square, and tall fin configurations (height/width aspect ratios in nm: $H_f/W_f = 20/80, 20/20, 80/20$). 100 nm BOX thickness and long channel. (Source: Adapted from Ritzenthaler *et al.*⁴²)

Truly three-dimensional coupling effects are observed in triple-gate or double-gate FinFETs (where the top channel is inhibited by a thicker oxide):

- *lateral* coupling between the side gates
- *vertical* coupling between the top gate and the bottom gate (substrate)
- *longitudinal* coupling between the drain and the body via the fringing fields penetrating in the BOX and substrate.⁴²

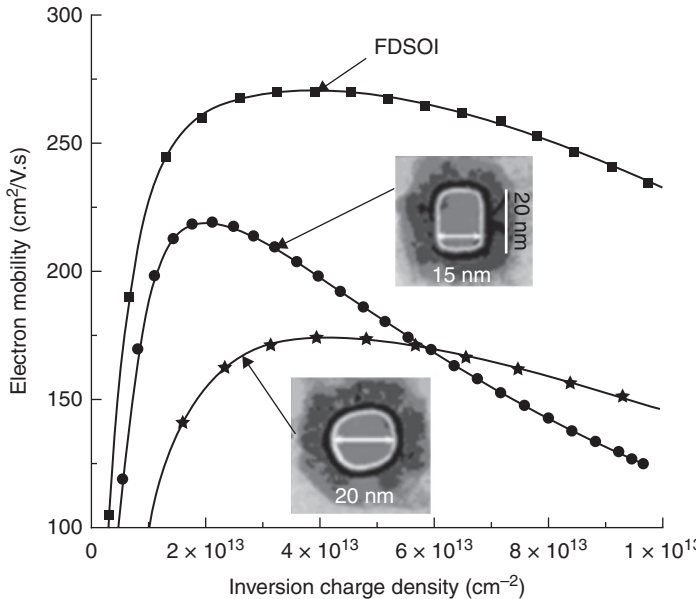
Figure 2.9 shows that wide fins behave as FD MOSFETs, with strong vertical coupling and little impact from the lateral gates. In tall and narrow fins, the electrostatics is dominated by the coupling of the lateral gates, which tends to suppress the vertical coupling to the bottom gate. The surface potential at the fin–BOX interface is massively controlled by the fringing field between the lateral gates.⁴² As a result, the defects generated in the BOX (during CMOS processing, radiations, or hot carrier injection⁴³) have no impact on device performance. Narrow triple-gate FinFETs are intrinsically radiation-hard⁴⁴ and tolerant to short-channel effects because the longitudinal drain-to-body coupling is equally screened.⁴² Conversely, narrow FinFETs cannot benefit from the back-gate effect (substrate biasing) as an option for threshold voltage tuning.

2.9 Characterization of nanowire FETs

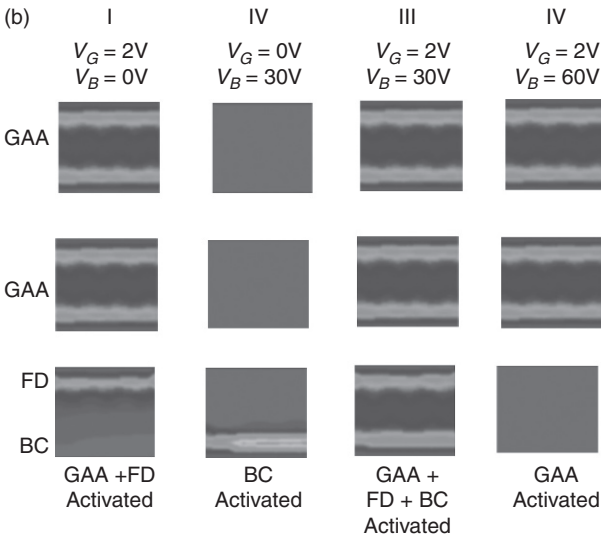
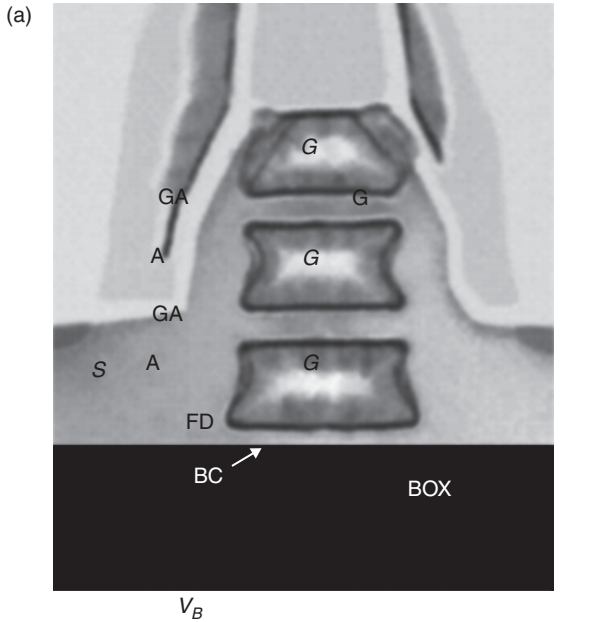
The gate-all-around (GAA) MOSFET features four channel sections, unless the body is cylindrical. GAA nanowire combines channel coupling and quantum effects¹ and is the ideal device in terms of electrostatic control and short-channel effects. Characterization-wise, there is less flexibility than in FD MOSFETs where back-gate biasing is available.

Mobility can be measured by split C-V or Y-function methods.⁴⁵ Favorable mobility values have been reported in relatively wide nanowires (20 nm), in particular when strain was used as a booster. Carrier mobility is systematically lower than in planar FD MOSFETs with equivalent thickness. In general, an acceptable mobility reduction is observed as the wire size decreases from 20 to 10 nm, while 5 nm nanowires feature rather poor mobility.⁵ Several factors may influence mobility: sub-band splitting modifying the effective mass, spatial confinement of carriers and phonons, or even insufficiently optimized production processes. For example, the fabrication of tiny nanowires by self-limited oxidation generates strain and defects.

In Fig. 2.10 rectangular and circular nanowires with similar size are compared. This puzzling mobility behavior was clarified only after complementary characterization. Nanowires with circular shape exhibit marked



2.10 Effective mobility versus charge in n-channel Si nanowire FETs with circular and rectangular cross-section. $L = 200$ nm. (Source: Adapted from Tachi *et al.*⁴⁵)



2.11 (a) Three-level nanowire transistor with 10 nm thick channels and 400 nm thick BOX. (b) Bias combinations for front (V_G) and back (V_B) gates enabling the activation and separation of different channels. (Source: Adapted from Reference 47: *Solid-State Electronics*, 53(7), Dupré *et al.*, 'Method for 3D electrical parameters dissociation and extraction in multichannel MOSFET (MCFET)', 746–752, copyright (2009) with permission from Elsevier.)

mobility degradation at low inversion charge. In this region, the mobility is limited by Coulomb scattering involving oxide charges, high-K dipoles, and interface traps. For verification, trap density was measured independently by CP; the results indicate a threefold increase of trap density in circular nanowires,⁴⁶ also confirmed by $1/f$ noise and low-temperature experiments. The difference in surface orientation may explain this; in rectangular nanowire, the sidewalls are oriented along crystal planes with low trap density, whereas in circular wires the surface orientation is continuously varying.

Why, then, do the mobility curves cross each other in very strong inversion? It is well documented that in strong inversion surface roughness scattering prevails, masking the effect of Coulomb scattering. A higher mobility reflects less surface scattering in circular nanowires. It is arguable that the surface roughness has been improved during the hydrogen annealing used to achieve the circular shape.

In order to increase the output current, the nanowires are organized in three-dimensional arrays. Advanced 3D-stacked nanowires feature a Si or SiGe body, surrounded by high-K/metal gate. Figure 2.11 shows three superposed nanowire FETs controlled by three interconnected gates. The upper two levels are plain GAA nanowires whereas the bottom device is different: it shares the top gate but has a BOX interface like a normal FD MOSFET. This configuration offers more flexibility for detailed characterization and channel separation. As shown in Fig. 2.11b, the gate controls five channels out of six, whereas the back gate governs the bottom channel. If both gates are active, all channels conduct. When the back gate is strongly accumulated, the two channels of the FD transistor are suppressed. By combining the various currents measured in these dispositions, it is possible to differentiate the conduction properties in the GAA nanowires from those in the front and back channels of the bottom FD FET.⁴⁷

2.10 Conclusions

SOI materials and devices are rapidly evolving with important modifications in size and structure. Their characterization is more challenging than ever. We have presented the issues and, when possible, proposed solutions. We also introduced updated techniques in order to characterize novel SOI structures, and illustrated them with experimental findings. While the pseudo-MOSFET is an undisputable tool for evaluation of SOI materials, there are more options for device characterization. Multiple gates are cumbersome, but their skillful manipulation provides advantages in testing.

2.11 Acknowledgments

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Modeling the performance of short-channel fully depleted silicon-on-insulator (SOI) metal oxide semiconductor field effect transistors (MOSFETs)

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Abstract: This chapter discusses different aspects in analytical modeling of silicon-on-insulator (SOI) MOSFETs which have emerged amongst the prime candidates for mobile communication and computation in the ‘Beyond Moore’s’ era. The chapter discusses two primary approaches in modeling of such devices. First, a one-dimensional model is analyzed which, by appropriate substitutions, is converted into a pseudo two-dimensional model. Later an exact two-dimensional model is described which is much more accurate than the first approach.

Key words: analytical model, silicon-on-insulator, silicon-on-nothing, Poisson’s equation, buried oxide, surface potential, threshold voltage.

3.1 Introduction

Moore’s (1995) law projects the shrinking dimensions of computer chips on an exponential curve with the number of transistors inside an integrated circuit (IC) doubling every two years. At this rate, current chips should have more than a billion transistors and a channel length less than 10 nm by 2014. Since conventional complementary metal oxide semiconductor (CMOS) technology is reaching its physical limit, the search for smaller, high efficiency chips has led to the exploration of nanometer scale CMOS alternatives. Silicon-on-insulator (SOI) technology has grown steadily with the first commercial SOI microprocessors now on the market. It is predicted that SOI technology will take over as an alternative to bulk CMOS in terms of scalability, material flexibility and minimum feature size of transistors.

Interface state characterization in small geometry MOSFETs with novel gate dielectrics is the subject of intensive research. It has been proven time and again that SOI MOSFETs are far more resistant to ‘short-channel effects’ (SCEs) than bulk MOSFETs. However, most of the modeling techniques developed for bulk silicon technology (Haddara and Cristoloveanu, 1986;

Haddara and Ghibaudo, 1988; Heremars *et al.*, 1989; Chen and Li, 1991) are not directly applicable to SOI devices for a number of reasons: the most significant being the lack of substrate contact in addition to the complex multi-interface nature of these devices. Most of the approaches so far have been unable to incorporate the SCEs and are only accurate if a number of assumptions are made. As the SOI MOSFETs in the nanoscale domain experience large vertical as well as lateral fields, the gradual channel approximation (GCA) is no longer valid and models based on a one-dimensional solution of Poisson's equation give erroneous results. Two-dimensional device modeling of SOI is a nascent field with intensive research work still being carried out.

The main objective of this chapter is to establish a detailed, physics-based framework for precise modeling of short-channel, fully depleted (FD) SOIs. This chapter does not claim to be exhaustive or complete. To date, many research groups have carried out and are continuing excellent research work in physics-based modeling and simulation of SOI MOSFETs. Most of the work presented in this chapter is the result of research from the 'Advance Computing and Low Power VLSI Design Lab' in Jadavpur University, India.

Modeling is always assumed to be the ultimate guide in gaining an insight into the operational principle of a certain device structure. But within its limits, 'device modeling' can be broadly categorized in to four different but related phases:

- The first phase, physics-based analytical simulations, are essential for the basic modeling of device operation. The charge distribution, carrier density, potential variation, electric field (both direction and magnitude) and current density in different places of the transistor are very important in identifying and facilitating subsequent improvements of the weaker aspects in a device and the conceptualization of a new structure with greater functionality.
- The second phase makes use of small signal equivalent circuit models and requires practical measurements of fabricated devices. This technique is semi empirical and acts as a bridge between the theoretical and practical aspects of a device. Limited knowledge about all material parameters can be overcome by using appropriate parameters unlike analytical modeling which is more inflexible.
- The third phase, large signal modeling, requires real time current voltage measurements and rigorous extraction of a number of intrinsic and extrinsic elements. A carefully constructed large signal circuit model can predict power levels, efficiency, linearity and stability, precisely in terms of circuit level performance.
- The fourth and final phase concentrates on evaluating device noise performance. Obviously a large number of probe station-based RF measurements are involved and the final model can be used extensively in CAD-based simulators.

Though MOSFET modeling is well covered, resulting in compact BSIM (Berkeley Short-channel IGFET Model), EKV (Enz *et al.*, 1995) and PSP (Gildenblat *et al.*, 2005) models, the field of SOI modeling is comparatively smaller. In contrast to numerical analysis, physics-based analytical models show greater compatibility with simulators and do not hinder the design procedure of circuits involving many elements. This chapter will provide a generalized theory about physics-based modeling and simulation of SOI MOSFETs. Interested readers are advised to study the additional material in the references to gain a deeper understanding.

3.2 The development of SOI MOSFET modeling

Historically SOI MOSFET modeling has followed two trends namely:

1. surface potential-based modeling
2. charge-based modeling

In both types of modeling, compact analytical formulations have always been preferred to iteration-based formulations. As the name suggests, in surface potential-based modeling the surface potential (i.e., the position of intrinsic energy level at the surface with respect to the bulk) is used to calculate the drain current, whereas in charge-based models, the current is calculated by developing the interrelations among the charges, namely gate charge, oxide charge, depletion charge and inversion charge. Taur *et al.* (2004) and Ortiz-Conde *et al.* (2005) have provided accurate surface potential-based models based on transformation of the double integration for drain current which was initially given by Sah and Pao (1966) for inversion charge in bulk MOS transistors.

Simultaneously, charge-based models which avoid the numerical solution methodology of the transcendental equations in surface potential-based models have been suggested by He *et al.* (2004) and Sallesea *et al.* (2005). A compact model was suggested by Jayadeva and Das Gupta (2009) to incorporate quantum mechanical effects. Here they took the interdependence of the charge density and the Fermi level to account for the charge formation in the well at the oxide–silicon interface. The charge and hence the current could then be accurately predicted in the weak, moderate and strong inversion region. Wu *et al.* (2010) presented a model which could predict the transport characteristics independent of whether the device works as partially depleted SOI (PD-SOI) or fully depleted SOI (FD-SOI). Their model could accommodate transition from one to another. Apart from these, various models have been presented and validated over time which analyze substrate space charge effect (Burignat *et al.*, 2010), optimize for the best dielectric (Darbandy *et al.*, 2011), treat undesirable effects such as trapped charges or defects in the front and back oxides (Husseini *et al.*, 2011) or

propose novel approaches such as work function engineering to mitigate threshold voltage roll-off (Deb *et al.*, 2012). In short, over the years, numerous researchers have helped produce a more and more detailed picture of the modeling aspect of SOI MOSFET.

3.3 A 1-D compact capacitive model for a SOI MOSFET

With each passing day microelectronics is moving towards nanoelectronics. Devices are being scaled more and more aggressively to keep up with the ever-growing demand for improved performance in terms of gain, linearity and reliability. All the device dimensions of a MOSFET are being shortened, namely:

- source drain junction depth,
- gate length,
- thickness of dielectric layers and
- thickness of active channel layers.

The present standards for gate lengths are 22 and 12 nm for industry and R&D, respectively. With the miniaturization of field effect transistors (FETs), a number of degrading effects termed short-channel effects (SCEs) modify their electrical characteristics. Just like a normal bulk MOSFET, SOI MOSFETs are affected by SCEs, though to a lesser extent. Consequently, proper inclusion of these SCEs is essential for a SOI MOSFET model to accurately predict the performance of all the dimensions of a device. SCEs can be attributed to the event when the drain along with the gate starts controlling the channel charge, major field gradients and the channel potential, current and conductance. This mode of control can be stated as ‘two-dimensional charge control’. Another phenomenon which is crucial in short-gated MOSFET modeling is termed as coupling of the field profiles. This is where coupling of the source-channel and drain-channel potential takes place through the buried insulator layer in the form of lateral electric fields (fringing fields.) This acts as an additional component to the SCEs degrading the device performance towards unpredictability. Consequently it is also very important to take these effects into account in any compact SOI MOSFET model used by circuit simulators.

To get an estimate of the charge formation in the channel, a two-dimensional Poisson’s equation has to be solved both in the active and the buried layer, but often the boundary conditions are hard to estimate and the solution procedure is quite cumbersome. In contrast, solving the 1-D Poisson’s equation perpendicular to the gate and transforming the 1-D analysis to effective 2-D analysis by voltage doping transformation (VDT) is less complex. For small drain to source voltages this method converges easily and is almost as accurate as 2-D analysis. With this method the surface potential and threshold voltage of the

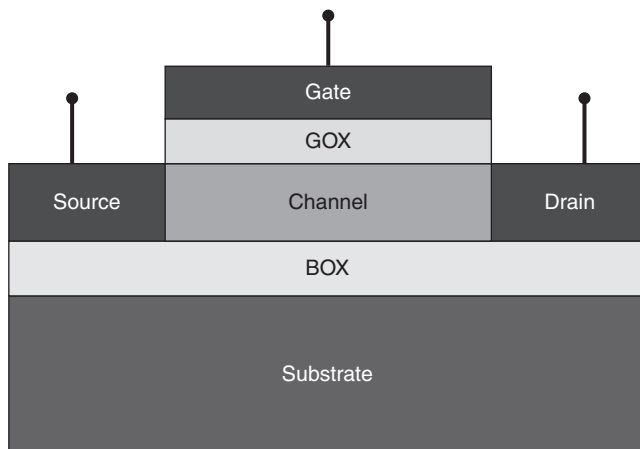
model are first calculated from an equivalent capacitance model of the device (hence the use of the term compact capacitive model) and from these the current and the conductance are calculated in the manner that follows.

3.3.1 Representative capacitance model

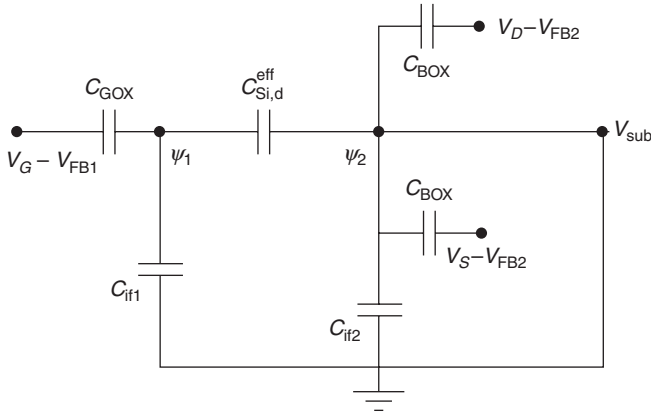
The device considered here is an ideal model structure with regular configuration. The various capacitances acting between different points are as shown in Fig. 3.1. In Fig. 3.2, an equivalent circuit model is presented. We consider the model and abbreviations as per Deb *et al.* (2011b), taking t_{GOX} , t_{Si} , t_{BOX} and t_{sub} to be the thicknesses of the gate oxide, sandwiched Si layer, buried oxide (i.e., insulator) and substrate layer, respectively. Here three oxide capacitances are present. C_{GOX} acts between the polysilicon gate and the channel whereas C_{BOX} acts between source/drain and channel. The latter can also be termed as fringing field capacitance as its origin remains in the fringing field lines through the BOX layer. Also $C_{\text{Si,d}}^{\text{eff}}$ is the depletion region capacitance in the silicon layer, C_{BOX} is the substrate bias capacitance and C_{if} are the capacitances due to interface states. In all the terminals the effective bias is reduced by an amount equal to the flatband voltage for that respective interface.

3.3.2 Modeling of the fringing field

The degree of lateral field penetration from the source/drain to the channel through the BOX layer is what differentiates a SOI MOSFET from a



3.1 A layered structure of SOI MOSFET. (Source: Printed with permission from Deb *et al.*, 2011b. <http://www.tandfonline.com/doi/abs/10.1080/00207217.2011.593140>.)



3.2 Representative capacitive model of SOI MOSFET. (Source: Printed with permission from Deb *et al.*, 2011b. <http://www.tandfonline.com/doi/abs/10.1080/00207217.2011.593140>.)

bulk Si MOSFET. A proper qualitative and quantitative analysis of the field requires complete knowledge of the potential profile in the back oxide layer for various substrate and drain biases. Though 1-D modeling is not accurate enough for this task it still gives a reasonable measure at low drain biases. When V_{DS} is small, the potential profile in the BOX profile can be assumed to be horizontally symmetrical about the channel centre. This approximation implies that both the source to channel (C_{SC}) and the drain to channel (C_{DC}) fringing field capacitances can be represented as:

$$C_{SC}(x) = \frac{K_{BOX}}{t_{BOX} \left[\exp\left(\pi/t_{BOX} \left(x + (L_{eff}/2)\right)\right) - 1 \right]} \tag{3.1}$$

$$C_{DC}(x) = \frac{K_{BOX}}{t_{BOX} \left[\exp\left(\pi/t_{BOX} \left(x - (L_{eff}/2)\right)\right) - 1 \right]} \tag{3.2}$$

where K_{BOX} and L_{eff} are the dielectric constant of the insulator and effective channel length of the device, respectively.

3.3.3 Transformation of 2-D field into effective 1-D

In the channel area both the longitudinal and lateral field control the charge formation. As a 1-D model is incapable of directly taking this into account, other possible ways need to be considered. A solution may come in the form of ‘voltage doping transformation’ or VDT approach where the lateral drain to source field supposedly reduces the effective doping concentration of

the channel. As a result of this, the depletion capacitance becomes not only a function of the gate to source potential but also of the drain to source bias and substrate bias (or effectively the back channel potential.) Thus the effective bias and doping can be written as:

$$V_{DS}^* = V_{DS} + 2(V_{bi} + \Psi_{S2} - \Psi_{S1}) + 2\sqrt{(V_{bi} + \Psi_{S2} - \Psi_{S1})(V_{DS} + V_{bi} + \Psi_{S2} - \Psi_{S1})} \quad [3.3]$$

$$N_A^* = N_A - \frac{2\varepsilon_{Si}V_{DS}^*}{qL_{eff}^2} \quad [3.4]$$

where V_{bi} is the built-in potential of the respective junction, and Ψ_{S1} and Ψ_{S2} are the front and back surface potentials, respectively.

From these the effective depletion capacitance is calculated by differentiating the depletion charge with respect to the potential:

$$C_{Si,d}^{eff} = \frac{dQ_d}{d\Psi} = \frac{qN_A^*t_{Si}L_{eff}}{\Psi_{S1} - \Psi_{S2}} \quad [3.5]$$

3.3.4 Charge control model

For a basic analytical charge control model we consider the charge equilibrium in each node as per Fig. 3.2. From the model one can write:

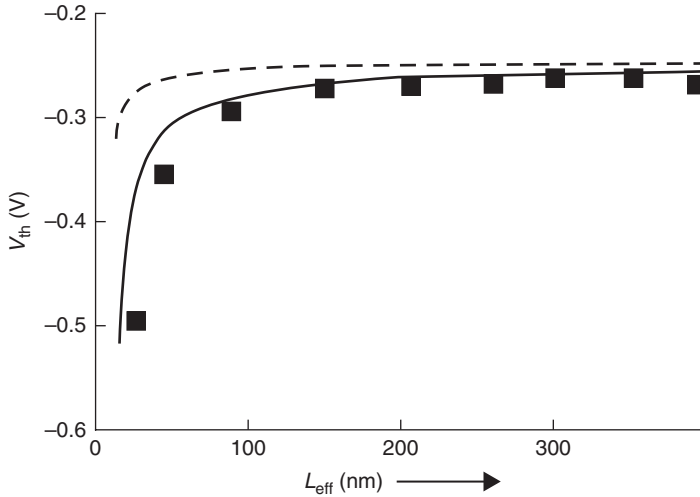
$$\psi_1(C_{GOX} + C_{Si,d}^{eff} + 2C_{if1}) = C_{GOX}(V_{G1} - V_{FB1}) + C_{Si,d}^{eff}\psi_2 \quad [3.6]$$

$$\psi_2(C_{Si,d}^{eff} + C_{if2} + 2C_{BOX}) = C_{BOX}\{(V_{DG} - V_{FB2}) + (V_{SG} - V_{FB2})\} + C_{Si,d}^{eff}\psi_1 \quad [3.7]$$

Now, as bias is applied at both the front gate and the substrate contact, there is a possibility of the formation of a charge layer at both the front and back interface. If we assume that the channel formation takes place at the front interface, then the surface potential is calculated in terms of the front gate voltage. By definition, threshold voltage is the gating voltage at which the band bending at the surface exceeds by an amount equal to $2\psi_F$ at the bulk, that is, at threshold condition, $\psi_1 = 2\psi_F + \psi_2$.

Hence the threshold voltage V_{th} is given by:

$$V_{th} = V_{FB1} + (2\psi_F + \psi_2) \left[1 + \frac{2C_{Si,d}^{eff}C_{BOX}}{C_{GOX}(C_{Si,d}^{eff} + 2C_{BOX})} \right] - (V_{DS} - 2V_{FB2}) \frac{C_{Si,d}^{eff}C_{BOX}}{C_{GOX}(C_{Si,d}^{eff} + 2C_{BOX})} \quad [3.8]$$



3.3 Variation of threshold voltage with effective channel length. Solid curve is for SOI; dashed curve represents a special situation where the insulator is vacuum and dots are simulated results for SOI with MEDICI. (Source: Printed with permission from Deb *et al.*, 2011b. <http://www.tandfonline.com/doi/abs/10.1080/00207217.2011.593140>.)

It can be clearly seen that the threshold voltage contains a factor involving V_{DS} . By plotting the threshold voltage against the channel length, the decrease in threshold voltage as the channel length diminishes can be shown. This is evident from Fig. 3.3 which shows that, for channel length up to 100 nm, the threshold voltage remains fairly constant but for channels with lesser dimensions there is a significant amount of threshold voltage roll-off. This is undesirable as it may turn on a short-channel device at the same bias which keeps the channel pinched off for a relatively longer channel length.

3.3.5 I–V characteristics

When the MOS functions as a capacitor then the charge formation is controlled simply by the gate bias, but in MOSFET both the gate and the drain bias affect the charge density. In a SOI MOSFET the same theory is involved. In an enhancement mode SOI MOSFET charge density is increased as the gate voltage increases (above threshold limit) but, when drain voltage is applied alongside, the channel potential increases linearly from source to drain. As a result charge decreases from source to drain and the pinch-off point is first observed at the drain end. Qualitatively at each point (x) in the channel the inversion must now be stronger than $2\psi_F + \psi_2 + V_c(x)$, where $V_c(x)$ is the channel potential at that particular point.

Taking a small section, dx , at any arbitrary point, x , in the channel where the channel potential and current remains constant throughout the section given by $V_c(x)$ and I_D we can formulate:

$$I_D = \mu_n C_{OX} W_g (V_{GS} - V_{th} - V_c(x)) \frac{dV_c(x)}{dx} \quad [3.9]$$

where W_g and C_{OX} are the width of the gate and permittivity of the gate oxide, respectively. Now considering the continuity of channel current in the channel itself we integrate Equation [3.9] along the channel by putting in the value of V_{th} from Equation [3.8] and we get:

$$\int_0^{L_{eff}} I_D dx = \mu_n C_{GOX} W_g \int_0^{V_{DS}} (V_{GS} - V_{th} - V_c) dV_c \quad [3.10]$$

After simplifying and rearranging we get the drain current in the non-saturation regime,

$$\begin{aligned} I_D = \mu_n C_{OX} \frac{W}{L} & [V_{GS} V_{DS} - V_{FB1} V_{DS} - 2V_T \ln\left(\frac{N_A}{n_i}\right) V_{DS} \\ & - \frac{4V_T \ln(N_A/n_i) C_{BOX} V_{DS}}{C_{GOX}} + \frac{4V_T \ln(N_A/n_i) C_{BOX} K_1 (-K_2 C_{GOX})}{(DC_{GOX})^2} \\ & \frac{\ln(K_3 C_{GOX} + K_2 C_{GOX} - K_1 C_{GOX} V_{DS})}{K_1 C_{GOX}} - \frac{(K_3 C_{GOX} + K_2 C_{GOX}) K_3 C_{BOX}}{(DC_{GOX})^2} \\ & \frac{\ln(K_3 C_{GOX} + K_2 C_{GOX} - K_1 C_{GOX} V_{DS})}{2(K_1 C_{GOX})^2} + \frac{(K_3 C_{GOX} + K_2 C_{GOX} - K_1 C_{GOX} V_{DS})^2 K_1 C_{BOX}}{(K_1 C_{GOX})^2} \\ & - \frac{2(K_3 C_{GOX} + K_2 C_{GOX} - K_1 C_{GOX} V_{DS}) K_1 C_{BOX}}{(K_1 C_{GOX})^2} \\ & + \frac{(K_3 C_{GOX} + K_2 C_{GOX})^2 K_1 C_{BOX}}{(K_1 C_{GOX})^3} \ln(K_3 C_{GOX} + K_2 C_{GOX} - K_1 C_{GOX} V_{DS}) \\ & - \frac{2V_{FB2} C_{BOX} K_1 V_{DS}}{K_1 C_{GOX}} \\ & + \frac{\{2V_{FB2} K_3 C_{BOX} K_1 C_{GOX} - 2V_{FB2} C_{BOX} K_1 (K_3 C_{GOX} + K_2 C_{GOX})\}}{(K_1 C_{GOX})^2} \\ & \ln(K_3 C_{GOX} + K_2 C_{GOX} - K_1 C_{GOX} V_{DS}) \end{aligned} \quad [3.11]$$

where K_1 , K_2 and K_3 are constants involving material dimensions, intrinsic and extrinsic properties such as temperature, doping, residual impurities, etc.

Modeling the drain current in the saturation mode presents us with two different scenarios for long- and short-channel MOSFETs. In long-channel MOSFETs it is accepted that the carrier traverses the whole channel under the gate with constant low field mobility, that is, the velocity is never saturated and is linearly proportional to the electric field (whose value never exceeds the critical electric field limit). Thus for a long-channel SOI MOSFET the saturation first sets in at the drain end where the potential just equals the gate overdrive.

$$V_{\text{DSsat}} = V_{\text{GS}} - V_{\text{th}} \quad [3.12]$$

As a result the channel first pinches off at the drain end. If the V_{DS} is increased from this particular value the pinch-off point moves into the channel and the current remains saturated. In the process to find V_{DSsat} it is noted that Equation [3.11] is a quadratic in V_{DS} . Thus it can be written that,

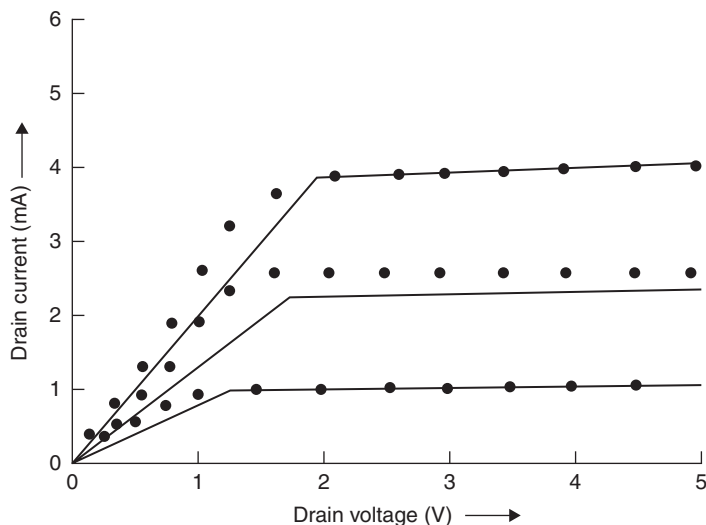
$$M_1 V_{\text{DS}}^2 + M_2 V_{\text{DS}} + M_3 = I_{\text{DS}} \quad [3.13]$$

where M_1, M_2, M_3 are constant for a particular device. At the point of saturation, I_{DS} observes a maximum, that is, $\partial I_{\text{DS}} / \partial V_{\text{DS}} = 0$ which implies

$$2M_1 V_{\text{DSsat}} + M_2 = 0 \quad [3.14]$$

From Equation [3.14] the value of V_{DSsat} is calculated and from Equation [3.8] the particular V_{thsat} is found. Finally, by putting these two particular voltages in Equation [3.11], saturated drain current can be found for a long-channel SOI MOSFET. Drain characteristics of a long-channel SOI MOSFET (280 nm) are plotted in Fig. 3.4. This shows that the transition is pretty abrupt accounting for the two asymptotic regions dictated by the extrinsic drain to source potential. Consequently it can be predicted that this modeling approach would result in a discontinuous drain conductance. Apart from this fact, the model mimics the behaviour of SOI MOSFET much better as it incorporates all the relevant capacitances into the formulation and, as will be seen over the following sections, this shortcoming is avoided in the two-dimensional model.

In the case of a short-channel SOI MOSFET, pinch-off never really occurs. Instead velocity saturation initiates the current saturation mechanism. In a short-channel FET the electric field is quite high throughout the channel and at a maximum at the drain end. As the applied drain bias increases



3.4 Variation of channel current with V_{DS} for different V_{GS} values of 1 (bottom line), 2 (middle line), and 3 volts (top line). In this case $W = 783 \mu\text{m}$, $L = 0.28 \mu\text{m}$, $t_{GOX} = 10 \mu\text{m}$, $t_{Si} = 94 \mu\text{m}$, $t_{BOX} = 347 \text{nm}$, $N_A = 10^{16} \text{cm}^{-3}$. Solid line is for SOI and dots are experimental data. (Source: Printed with permission from Deb *et al.*, 2011b. <http://www.tandfonline.com/doi/abs/10.1080/00207217.2011.593140>.)

so does the field, and as soon as it crosses the critical field limit the velocity becomes saturated. Like the long-channel SOI MOSFET, as drain bias increases, the point of saturation shifts further into the channel. For a short-channel SOI MOSFET we consider the simple mobility model,

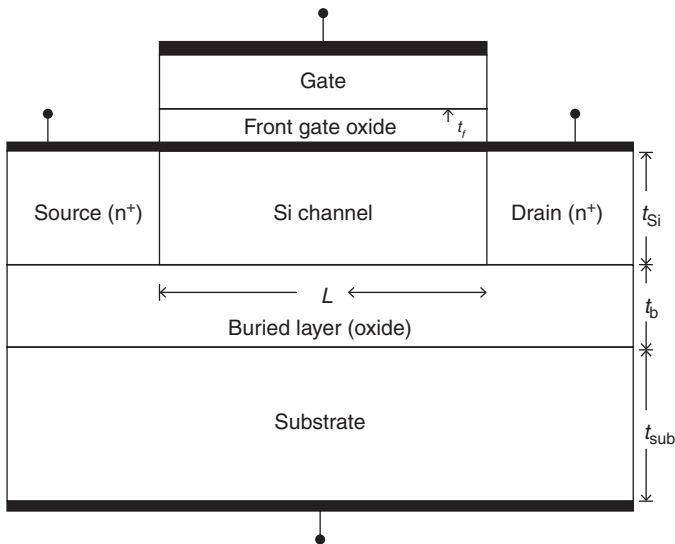
$$\mu_n = \frac{\mu_0}{1 + (\mu_0 V_{DS} / v_{sat} L_{eff})} \quad [3.15]$$

where μ_0 is the low field mobility. This gives a smoother transition from the velocity unsaturated region to saturated region. Here V_{DSsat} is given by that voltage at which the field at the drain reaches critical field, but in a short-channel MOSFET the field under the gate is essentially two-dimensional and a 1-D analysis cannot give a proper measure of the same. Hence for short-channel SOI MOSFET modeling, a two-dimensional compact model is described below.

3.4 A 2-D analytical model for a SOI MOSFET

As an extension to the above discussions, it is evident that modeling a short-channel, FD-SOI MOSFET requires a complete knowledge of the field and

potential profile. The back bias along with the coupling of the source/drain and channel through the insulator layer modifies the surface potential of the front interface. It is very important to incorporate these effects to be able to accurately describe the drain induced barrier lowering (DIBL), the SCEs and the 2-D charge sharing. In earlier MOSFET models (Grebene and Gandhi, 1969) the entire channel was divided into two distinct regions. In the region closer to the source, gradual channel approximation (GCA) is taken to be valid, in other words, the rate of change of the vertical field is much higher than for the lateral field and the field may be assumed to be one-dimensional. In contrast, near the drain, the GCA theory is no longer valid and the cumulative field effectively becomes two-dimensional. For that region a two-dimensional potential profile was assumed. The two potentials were asserted so that they are continuous at the point where the two regions converge, that is, where 1-D region ends and the 2-D region begins. However, this requires the boundary conditions inside the channels to be determined with utmost precision at all bias points. So, instead of that approach and dividing the channel under the gate into separate regions, it shall be assumed that the whole channel possesses a two-dimensional potential profile. In addition to the silicon region under the gate, the potential profile of the buried oxide layer will be taken into consideration and will also be assumed to be two-dimensional. The idealized structure that we are going to use is shown in Fig. 3.5 and the abbreviations are taken to be the same as before. Let t_f , t_{Si} , t_{BL} , t_{sub} and L be the thicknesses of gate oxide, source/drain, silicon, buried oxide and substrate respectively.



3.5 Generalized layer structure for SOI MOSFET. (Source: Printed with permission from Deb *et al.*, 2011a.)

silicon channel layer, buried (insulator) layer, substrate layer and metallurgical channel length of the device, respectively.

3.4.1 Surface potential

First, we consider the depleted channel region as per Deb *et al.* (2011a). If the potential is $\varphi(x, y)$, then Poisson's equation can be written as:

$$\frac{\partial^2 \varphi(x, y)}{\partial x^2} + \frac{\partial^2 \varphi(x, y)}{\partial y^2} = \frac{qN_A}{\epsilon_{Si}} \quad [3.16]$$

where N_A is the acceptor concentration in the p-type substrate and ϵ_{Si} is the permittivity of silicon. Now as a probable solution of $\varphi(x, y)$ we might consider a polynomial where

$$\varphi(x, y) = A_1(x) + A_2(x)y + A_3(x)y^2 \quad [3.17]$$

Thus the two-dimensional nature of the potential is accounted for. At the front and back channel interfaces the field is assumed to be uniform and the surface potentials are designated as $\varphi_{sf}(x)$ and $\varphi_{sb}(x)$, respectively. Now we can write the four boundary conditions in the channel in accordance with the continuity of electric flux,

$$\varphi(x, y)|_{y=0} = \varphi_{sf}(x) \quad [3.18]$$

$$\varphi(x, y)|_{y=t_{Si}} = \varphi_{sb}(x) \quad [3.19]$$

At $y = 0$,

$$\frac{\partial \varphi(x, y)}{\partial y} = -E_{sf}(x) = -\frac{\epsilon_{OX}}{\epsilon_{Si}} \frac{V'_{gs} - \varphi_{sf}(x)}{t_f} \quad [3.20]$$

At $y = t_{Si}$

$$\frac{\partial \varphi(x, y)}{\partial y} = -E_{sb}(x) = -\frac{\epsilon_{BL}}{\epsilon_{Si}} \frac{V'_{ss} - \varphi_{sb}(x)}{t_{BL}} \quad [3.21]$$

where ϵ_{BL} is the dielectric permittivity of silicon dioxide, and V'_{gs} and V'_{ss} are the effective applied front and back channel voltages (after correction for flatband voltages).

The front and back channel voltages are expressed as:

$$V'_{gs} = V_{gs} - V_{ffb} \quad \text{and} \quad V'_{ss} = V_{ss} - V_{bfb},$$

where V_{ffb} and V_{bfb} are the front and back channel flat band voltages, respectively. From Equations [3.17] to [3.21] the values of the coefficients $A_1(x)$, $A_2(x)$ and $A_3(x)$ are derived as:

$$A_1(x) = \varphi_{sf}(x) \quad [3.22]$$

$$A_2(x) = -\frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{V'_{gs} - \varphi_{sf}(x)}{t_f} = -\frac{C_f}{\epsilon_{Si}} [V'_{gs} - \varphi_{sf}(x)] \quad [3.23]$$

$$A_3(x) = \frac{V'_{ss} + V'_{gs} [(C_f/C_{BL}) + (C_f/C_{BL})] - \varphi_{sf}(x) [1 + (C_f/C_{BL}) + (C_f/C_{BL})]}{t_{Si}^2 [1 + 2(C_f/C_{BL})]} \quad [3.24]$$

where, C_f and C_{BL} are front and back insulator capacitances per unit area, respectively. By double differentiation of Equation [3.17] and putting the values of the $A_i(x)$ for the front surface boundary conditions we get a differential equation of $\varphi_{sf}(x)$ given by,

$$\begin{aligned} & \frac{t_{Si}^2 [1 + 2(C_{Si}/C_{BL})]}{[1 + (C_f/C_{BL}) + (C_f/C_{Si})]} \frac{d^2 \varphi_{sf}(x)}{dx^2} - \varphi_{sf}(x) \\ & + \frac{[(C_f/C_{BL}) + (C_f/C_{Si})]}{[1 + (C_f/C_{BL}) + (C_f/C_{Si})]} (V_{gs} - V_{th}) + 2\varphi_F = 0 \end{aligned} \quad [3.25]$$

Now for long-channel threshold voltage we solve the above equation for $\varphi_{sf}(x)$ and equate to $2\varphi_F$ (given by $(K_B T/q) \ln(N_A/N_i)$). Then one obtains, for long channels,

$$V_{th}^{long} = V_{ffb} + \frac{[1 + (C_f/C_{BL}) + (C_f/C_{Si})](2\varphi_F)}{[(C_f/C_{BL}) + (C_f/C_{Si})]} + \frac{qN_A t_{Si} [1 + 2(C_{Si}/C_{BL})]}{2C_{Si} [(C_f/C_{BL}) + (C_f/C_{Si})]} - \frac{V'_{ss}}{[(C_f/C_{BL}) + (C_f/C_{Si})]} \quad [3.26]$$

For the purposes of calculation we will assume:

$$\frac{\left[\left(C_f / C_{BL} \right) + \left(C_f / C_{Si} \right) \right]}{\left[1 + \left(C_f / C_{BL} \right) + \left(C_f / C_{Si} \right) \right]} \left(V_{gs} - V_{th} \right) + 2\varphi_F = v' \quad [3.27]$$

and

$$\frac{t_{Si}^2 \left[1 + 2 \left(C_{Si} / C_{BL} \right) \right]}{\left[1 + \left(C_f / C_{BL} \right) + \left(C_f / C_{Si} \right) \right]} = \lambda^2 \quad [3.28]$$

Thus Equation [3.25] is reduced to

$$\lambda^2 \frac{d^2 \varphi_{sf}(x)}{dx^2} - \varphi_{sf}(x) + v' = 0 \quad [3.29]$$

Now let us introduce another variable designated as $\zeta(x)$, where $\zeta(x) = \varphi_{sf}(x) - v'$. Thus,

$$\frac{d^2 \zeta(x)}{dx^2} - \frac{\zeta(x)}{\lambda^2} = 0 \quad [3.30]$$

Now in the buried insulator layer Equations [3.20–3.21] are no longer valid, because the vertical field there is not caused by only substrate bias but also by the field arising from the source/drain coupling with the channel. To take account of this effect it is assumed that V_{ss} will be modified to V_{ss}^{eff} . If one considers that there are no charge carriers in the insulator layer and we ignore the effect of immobile ions, then Laplace's equation for the layer is given by:

$$\frac{\partial^2 \varphi(x, y)}{\partial x^2} + \frac{\partial^2 \varphi(x, y)}{\partial y^2} = 0 \quad (0 \leq x \leq L, t_{Si} \leq y \leq t_{Si} + t_{in}) \quad [3.31]$$

Now the boundary conditions for the above equation are,

$$\varphi(0, t_{Si}) = V_{bi} \quad [3.32]$$

$$\varphi(L, t_{Si}) = V_{bi} + V_{ds} \quad [3.33]$$

$$\varphi(x, t_{Si}) = \varphi_{sb}(x) \quad [3.34]$$

$$\varphi(x, t_{\text{Si}} + t_{\text{BOX}}) = V_{ss} - V_{bfb} \quad [3.35]$$

In the buried layer the two derivatives of Equation [3.31] are weakly coupled,

$$\frac{\partial^2 \varphi(x, y)}{\partial x^2} \approx -\frac{\partial^2 \varphi(x, y)}{\partial y^2} \approx \chi_{(\text{say})} \quad [3.36]$$

Though for a long-channel SOI MOSFET it can be assumed to be zero, but it possesses a finite value as channel length reduces. Thus integrating Equation [3.36] over the entire channel we get

$$\begin{aligned} \chi &= \frac{2}{L^2} \left[\varphi(L, y) - \varphi(0, L) - \left(\frac{\partial \varphi(x, y)}{\partial x} \Big|_{x=0} \right) L \right] \\ &= \frac{2}{L^2} [kV_{ds} + rE_0L] \end{aligned} \quad [3.37]$$

where the value of r and k (both ≤ 1) are to be fitted as per experimental data. They are both process dependent parameters as their values are dependent upon the thickness and length involved in a particular fabrication process. Also we define the source of the fringing field as:

$$E_0, \quad \text{where } E_0 = -\frac{\partial \varphi(x, y)}{\partial x} \Big|_{x=0}$$

Now we again integrate Equation [3.36] but this time along the y axis from $y = t_{\text{Si}}$ to $y = t_{\text{Si}} + t_{\text{BL}}$. Also in the final integrand we put the value of χ from Equation [3.37]. Thus,

$$\frac{\partial \varphi(x, y)}{\partial y} \Big|_{x=0, y=t_{\text{Si}}} = \frac{1}{t_{\text{BL}}} \left[\frac{kV_{ds} + rE_0L}{L^2} t_{\text{BL}}^2 + V_{ss} - V_{bfb} - \varphi_{sb}(x) \right] \quad [3.38]$$

If we take a closer look at Equations [3.21] and [3.38] it is possible to assert the effective back substrate bias by comparing two equations.

$$V_{ss}^{\text{eff}} = V_{ss} + \frac{t_{\text{BL}}^2}{L^2} (kV_{ds} + rE_0L) \quad [3.39]$$

Also from Equations [3.20], [3.21] and [3.14] we can write that

$$\varphi_{sb}(x) = \frac{2C_{Si} + C_f}{2C_{Si} + C_{BL}} \varphi_{sf}(x) - \frac{C_f}{2C_{Si} + C_{BL}} V'_{gs} + \frac{C_{BL}}{2C_{Si} + C_{BL}} V'_{ss} \quad [3.40]$$

From Equation [3.40], E_0 can be determined as:

$$\begin{aligned} E_0 &= - \left. \frac{d\varphi_{sb}(x)}{dx} \right|_{x=0} \\ &= - \frac{2C_{Si} + C_f}{2C_{Si} + C_{BL}} \left\{ \left. \frac{d\varphi_{sf}(x)}{dx} \right|_{x=0} \right\} \\ &= - \frac{2C_{Si} + C_f}{2C_{Si} + C_{BL}} \left\{ \frac{(V_{bi} + V_{ds} - v') - (V_{bi} - v') \cosh(L/\lambda)}{\lambda \sinh(L/\lambda)} \right\} \end{aligned} \quad [3.41]$$

From Equations [3.39] and [3.41] we can write,

$$V_{ss}^{\text{eff}} = V_{ss} + \frac{t_{BL}^2}{L^2} \left[kV_{ds} - rL \left(- \frac{2C_{Si} + C_f}{2C_{Si} + C_{BL}} \left\{ \frac{(V_{bi} + V_{ds} - v') - (V_{bi} - v') \cosh(L/\lambda)}{\lambda \sinh(L/\lambda)} \right\} \right) \right] \quad [3.42]$$

Evidently this effective substrate bias reduces to the conventional substrate bias for long channels and/or thin buried layers. This effective substrate bias in turn modifies the threshold voltage which can be written in the form of Equation [3.26] as:

$$V_{th}^{\text{eff}} = V_{fbb} + \frac{\left[1 + (C_f/C_{BL}) + (C_f/C_{Si}) \right]}{\left[(C_f/C_{BL}) + (C_f/C_{Si}) \right]} (2\varphi_F) + \frac{qN_A t_{Si} (1 + 2(C_{Si}/C_{BL}))}{2C_{Si} \left[(C_f/C_{BL}) + (C_f/C_{Si}) \right]} \frac{V_{ss}^{\text{eff}}}{\left[(C_f/C_{BL}) + (C_f/C_{Si}) \right]} \quad [3.43]$$

Accordingly, Equation [3.30] is modified as:

$$\frac{d^2 \zeta_{\text{eff}}(x)}{dx^2} - \frac{\zeta_{\text{eff}}(x)}{\lambda^2} = 0 \quad [3.44]$$

Now the boundary conditions to this equation are:

$$\zeta_{\text{eff}}(x) \Big|_{x=0} = V_{bi} - v'_{\text{eff}} = V'_1$$

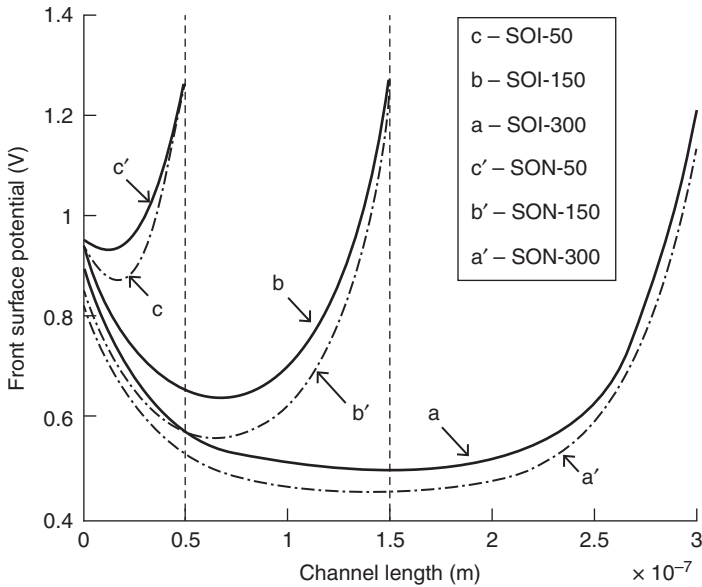
$$\zeta_{\text{eff}}(x)|_{x=L} = V_{bi} + V_{ds} - v'_{\text{eff}} = V'_2 \tag{3.45}$$

We now have enough conditions to calculate the effective surface potential for the device. As a solution to the second order differential equation it can be written as,

$$\begin{aligned} \varphi_{sf}(x) &= \zeta_{\text{eff}}(x) + v'_{\text{eff}} \\ &= \frac{V'_1 \sinh((L-x)/\lambda) + V'_2 \sinh(x/\lambda)}{\sinh(L/\lambda)} + v'_{\text{eff}} \end{aligned} \tag{3.46}$$

Clearly, the surface potential has a hyperbolic dependence upon the applied drain bias. Figure 3.6 plots the surface potential along the channel showing two cases: one where the insulator used in the buried layer is silicon dioxide, the other comprising air (vacuum). The latter is a special case where the device is known as silicon-on-nothing (SON).

It is seen that up to 300 nm of channel length, short-channel effects are minimal and the potential distribution is symmetric, that is, the point of minimum surface potential is also the midpoint of the channel. As the channel length



3.6 Variation of surface potential along the channel. Solid line is for SOI, dashed line is for SON. Here $V_{DS} = 0.5 \text{ V}$, $t_{\text{GOX}} = 7 \text{ nm}$, $t_{\text{Si}} = 100 \text{ nm}$, $t_{\text{BL/air}} = 200 \text{ nm}$, $N_A = 2 \times 10^{23} \text{ m}^{-3}$, $V_{ss} = 1 \text{ V}$. (Source: Printed with permission from Deb *et al.*, 2011a.)

is further reduced the device enters into nanometer regime from submicrometer regime. Hence the SCEs play a pivotal role, especially the drain induced barrier lowering of the source potential, shifting the point of minimum surface potential towards the source. It is also apparent that, as the permittivity of the buried layer decreases ($\text{SiO}_2 \rightarrow \text{vacuum}$), so does the minimum value of the potential, therefore restraining the SCEs to a greater degree.

3.4.2 Threshold voltage and current

The threshold voltage of the device is defined as the potential at which the surface faces an inversion at the source point. However, the point of minimum surface potential is not the source but somewhere around the midpoint of the channel, so we define the threshold voltage of our device for that point of minimum surface potential. In this way, we use the condition for minimum surface potential $d\varphi_{sf}(x)/dx = 0$. Thus the minimum point is found to be:

$$x_{\min} = 0.5 \left[L - \lambda \log \frac{\tanh(L/2\lambda) - M}{\tanh(L/2\lambda) + M} \right]$$

where

$$M = \frac{V'_2 - V'_1}{V'_2 + V'_1} \quad [3.47]$$

and the particular value of surface potential is given by

$$\varphi_{sf} \Big|_{x=x_{\min}} = \frac{V'_1 \sinh((L - x_{\min})/\lambda) + V'_2 \sinh(x_{\min}/\lambda)}{\sinh(L/\lambda)} + V'_{\text{eff}} \quad [3.48]$$

Finally we equate this surface potential with the condition of surface potential being equal to twice the value of bulk potential. Thus the threshold voltage of the SOI MOSFET is, according to our definition,

$$V_{\text{th}}^{\text{short}} = V_{\text{th}}^{\text{eff}} + \frac{1}{C_{\text{Si}}} \left[\frac{2\varphi_F}{C_2} - \frac{C_1}{C_3} - 2\varphi_F \right] \quad [3.49]$$

where the constants are given by,

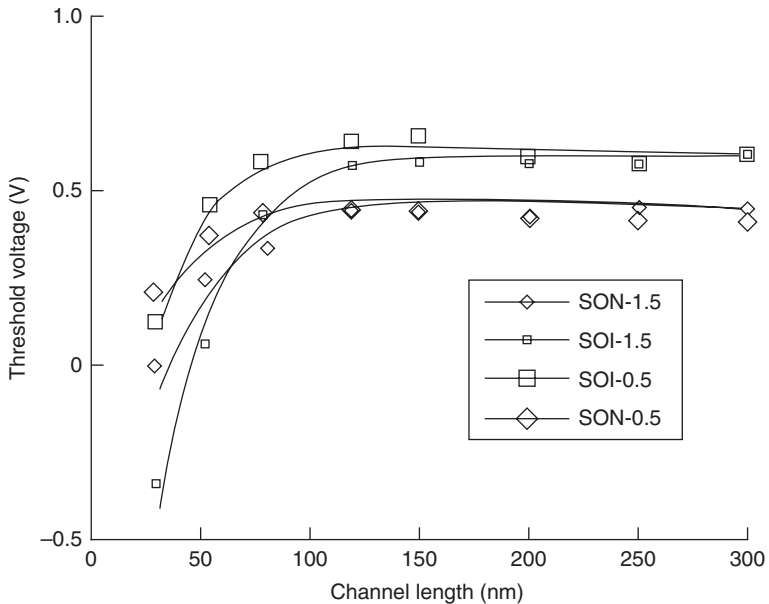
$$C_1 = \frac{V_{\text{bi}} \left[\sinh((L - x_{\min})/\lambda) + \sinh(x_{\min}/\lambda) \right] + V_{ds} \sinh(x_{\min}/\lambda)}{\sinh(L/\lambda)}$$

$$C_2 = \frac{[(C_f/C_{BL}) + (C_f/C_{Si})]}{[1 + (C_f/C_{BL}) + (C_f/C_{Si})]}$$

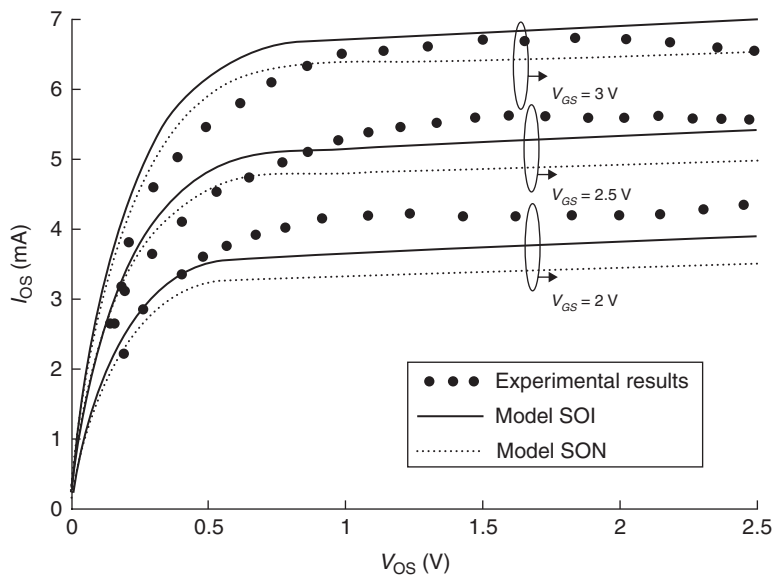
$$C_3 = 1 - \frac{[\sinh((L - x_{\min})/\lambda) + \sinh(x_{\min}/\lambda)]}{\sinh(L/\lambda)}$$

Thus the threshold voltage of a short-channel device is no longer independent of channel length as in long-channel SOI MOSFETs but decreases as the channel length diminishes. Figure 3.7 shows this threshold voltage roll-off for SOI devices which takes effect as soon as the channel length decreases below 100 nm. Two things are apparent. First, when the device is biased at higher V_{DS} , the roll-off is greater signifying the effect of drain bias on threshold voltage. Secondly, as the permittivity of the buried layer decreases, the roll-off is less, a condition similar to variation of surface potential with material dielectric constant.

To formulate drain current for an n-channel SOI MOSFET we take a simple model given by:



3.7 Variation of threshold voltage with effective channel length for SOI/SON MOSFETs for $V_{DS} = 0.5$ and $V_{DS} = 1.5$ V. The other experimental conditions are the same as Fig. 3.6 and dots indicate simulated data. (Source: Printed with permission from Deb *et al.*, 2011a.)



3.8 Variation of channel current with V_{DS} for different V_{GS} values (2, 2.5, 3V).

$$I_{DS} = \frac{W\mu_{\text{eff}}C_f}{L_{\text{eff}}(1+(V_{DS}/LE_c))} \left[(V_{GS}-V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2 \right] \quad [3.50]$$

in the linear region and

$$I_{DS,\text{sat}} = \frac{W\mu_{\text{eff}}C_f}{L_{\text{eff}}(1+(V_{DS,\text{sat}}/LE_c))} \left[(V_{GS}-V_{Th})V_{DS,\text{sat}} - \frac{1}{2}V_{DS,\text{sat}}^2 \right] \quad [3.51]$$

in the saturation region.

It is worth mentioning that μ_{eff} is different from low field mobility and has to be found out experimentally. Figure 3.8 shows the plot of drain current with drain bias. Here E_c is the critical electric field at which electron velocity (v_e) saturates and $V_{DS,\text{sat}}$ is the saturation voltage. Both are given by:

$$E_c = \frac{v_e}{\mu}, \quad V_{DS,\text{sat}} = \frac{V_{GS} - V_{Th}}{1 + ((V_{GS} - V_{Th})/LE_c)}$$

From this it is evident that the 2-D model overcomes the discontinuous drain conductance limitation of the 1-D model. The 1-D model is essentially

a charge control model whereas the 2-D model is a surface potential-based one. Even though there was no gradual transition from the former to the latter, both were presented to provide a comparative viewpoint. From a mathematical point of view the two-dimensional field assumptions are much more appropriate for all short-channel unipolar FET devices (such as MESFET, MOSFET, MISFET, HFET, TEGFET, HEMT, MISHFET, etc.). The above discussion ignored quantum effects and other second order effects as it was intended to present simplistic compact models. This is appropriate up to approximately 50 nm of channel length and about 5 nm of insulator thickness. However, in the ‘Beyond Moore’ era the channel lengths of present day FETs are approaching 22 nm and effective gate oxide thickness in terms of SiO₂ is around 0.5 nm; hence these effects cannot be ignored. In such ultrashort dimensions to ensure accurate modeling, various effects must be considered such as:

- leakage through the dielectric,
- band to band (BTB) tunneling in the channel,
- gate induced drain leakage (GIDL) and
- hot carrier effects.

Also, in the presented models, the channel region was rather thick with a certain amount of doping present in the channels. The same device can function as a partially depleted SOI (PD-SOI) when it operates near the flatband voltages and as a FD-SOI when the applied gate bias approaches supply voltage, V_{DD} . It is well documented that undoped channels with ultra-thin body SOI MOSFETs (so that they operate as FD-SOI minimizing the floating body effect) are most efficient in resisting SCEs. A number of extensive models for such devices can be found in Majumdar *et al.* (2009), Lime *et al.* (2011) and Fenouillet-Beranger *et al.* (2012). Readers are encouraged to study these to extend their understanding.

3.5 Modeling of dual gate and other types of SOI MOSFET architecture

Other than single gate SOI MOSFETs, structures such as dual gate and cylindrical/nanowire SOI MOSFETs have also been modeled quite accurately. In the case of double gated structures (Reddy and Kumar, 2004) the only difference is the presence of another fully formed gate below the buried oxide layer. In these structures both gates can create and modulate the charge at the respective insulator/silicon interfaces, but often the structure is asymmetric (the back gate oxide is much thicker than the front gate oxide) so that the inversion channel is formed at the front interface. Here a polynomial of the same form may be assumed for the back surface

potential as well as the front surface potential. The actual forms of these are worked out from the boundary conditions, Poisson's equation and continuity of electric flux. An improvised version of dual gate (DG) SOI MOSFET is dual material dual gate (DMDG.) Here, the front gate contains two different gate materials with different work functions. The step in the surface potential in this special case is accounted for by the sudden difference in flatband voltages of the two gates as shown by Reddy and Kumar (2005). Gate all around (GAA) SOI MOSFETs, which are quite different from rectangular planar structure have also been proposed and modeled (Ray and Mahapatra, 2008). A transformation of rectangular co-ordinates to cylindrical co-ordinates and analytical solution procedure with respect to appropriate boundary conditions produces favourable results to those predicted by numerical 3-D solutions.

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Partially depleted (PD) silicon-on-insulator (SOI) technology: circuit solutions

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Abstract: Partially depleted SOI (PDSOI) technology can provide a significant performance boost over bulk technology. This chapter first reviews the main device aspects of PDSOI technology including the basic benefits and issues with the floating body inherent to a PDSOI device. Next, some of the digital circuit design issues faced with PDSOI are described along with solutions. Then, the chapter addresses the SRAM design issues that are unique to PDSOI highlighting the advantage of body contacted devices in the sense amp and concludes with an example of bitcell margining that was used for a PDSOI technology.

Key words: partially depleted SOI, SRAM, floating body, circuit solutions, sense amp.

4.1 Introduction

Partially depleted SOI (PDSOI) has been successfully employed on many high performance designs by several different companies over the past 15 years. IBM successfully produced RISC based microprocessors in 0.18 μm SOI technologies in 1999 (Allen *et al.*, 1999; Canada *et al.*, 1999), and since then there have been many more products across different PDSOI technology nodes including several generations of Power PC microprocessors from IBM (Warnock 2003; Stolt *et al.*, 2008; Wendel *et al.*, 2011); the CELL broadband processor from the joint project between IBM, Sony, and Toshiba (Pham *et al.*, 2006; Pille *et al.*, 2007); PowerPC processors from Motorola (Bearden, 2002); and several different cores and processors from AMD with the most recent utilizing a 32 nm PDSOI technology (Fischer *et al.*, 2011).

PDSOI has several benefits over bulk devices that make it attractive especially for high performance applications. The PDSOI advantages include lower junction capacitance that results in higher performance at a given dynamic power; floating body effects that result in dynamic threshold voltage changes that improve the performance and body effect; reduced susceptibility to radiation induced errors; and lower substrate-coupled noise (Bernstein

and Rohrer, 2002). These advantages have resulted in performance enhancements of 20% or more on some PDSOI circuits relative to bulk.

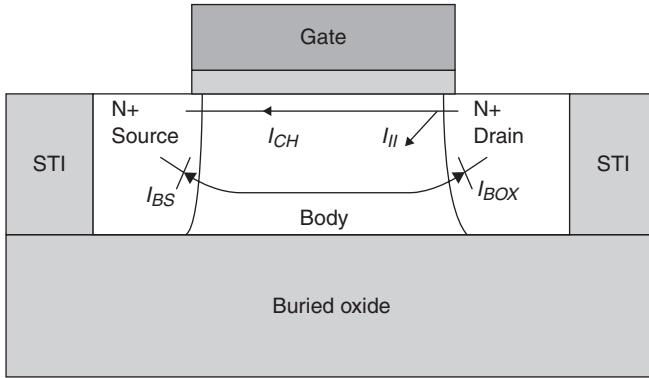
While the PDSOI floating body can provide improved performance, it does result in several undesirable effects. These include bipolar currents that can dynamically discharge high nodes that are supposed to remain high; time varying threshold voltage (V_t) that depends on the history of the device resulting in timing variations that must be accounted for; increased drain induced barrier lowering (DIBL) which requires more doping in the device to provide a similar V_t as bulk; and the lack of being able to supply a back-bias unless using a body contacted device which takes up much more area.

This chapter will next look at some basic aspects of the PDSOI devices in Section 4.2. Sections 4.3 and 4.4 will describe some of the circuit solutions that have been employed in digital and SRAM circuits, respectively. An example of SRAM cell margining from a PDSOI technology will then be detailed in Section 4.5. The chapter concludes with a few thoughts on future trends discussed in Section 4.6.

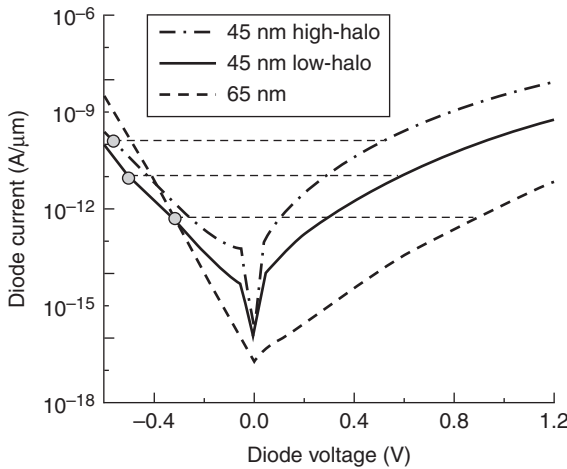
4.2 PDSOI technology and devices

In a partially depleted SOI device, the body is thick enough such that only part of the body region is depleted across the bias range of operation. Figure 4.1 shows a simple cross-section view of an NMOS PDSOI device. The body thickness and buried oxide (BOX) thickness have typically varied for different technologies with the general trend of thinner silicon thickness with scaling. For example, a 0.35 μm technology (Mistry *et al.*, 1997) used $T_{\text{Si}} = T_{\text{BOX}} = 200$ nm, while a 0.1 μm technology (Celik *et al.*, 2002) scaled the T_{Si} to 100 nm in conjunction with a 200 nm T_{BOX} . The BOX layer results in a very low capacitance for the bottom of the source and drain junctions, thus reducing the junction capacitance significantly which improves the speed-power capability of the device. The BOX does cause a parasitic FET to form along the bottom of the body with the ‘back-gate’ being the silicon substrate. Conduction along this back channel frequently caused leakage issues in early SOI work due to the defects at the BOX–substrate interface.

In addition to the benefits from the reduced junction capacitance, the floating body of the PDSOI device can provide improved performance. As shown in Fig. 4.1, the floating body forms diodes to the source and drain regions. For an NMOS device, if the device is off with the gate and source at 0 V and the drain at V_{dd} , the body will float up to an equilibrium point set by the diodes with the body-drain diode being reverse biased and the body-source diode being forward biased. Figure 4.2 shows diode characteristics from a 65 nm PDSOI as well as two 45 nm PDSOI options (Cai *et al.*, 2008).



4.1 Schematic of an NMOS PDSOI device including body-source and body-drain diodes, impact ionization current, and channel current.



4.2 Forward and reverse bias diode leakage characteristics from 65 nm PDSOI technology and 45 nm PDSOI experiments. (Source: © 2008 IEEE. Reprinted, with permission, from Cai *et al.* (2008), 'Will SOI have a life for the low-power market?', in *2008 IEEE Int. SOI Conf. Dig. Tech. Papers*, 15–16.)

The diode characteristics depend on the doping at the junction as well as the recombination centers at the junction that can be intentionally introduced by implantation (Ohno *et al.*, 1995). For the 65 nm technology in Fig. 4.2 with $V_{dd} = 1.2$ V, the diode characteristics show the body should reach equilibrium at ~ 0.35 V for the NMOS device with $V_g = V_s = 0$ V and $V_{dd} = 1.2$ V. The positive bias on the body results in a lower V_t for a given body doping relative to bulk, albeit at the expense of higher leakage. As the device is turned on, the

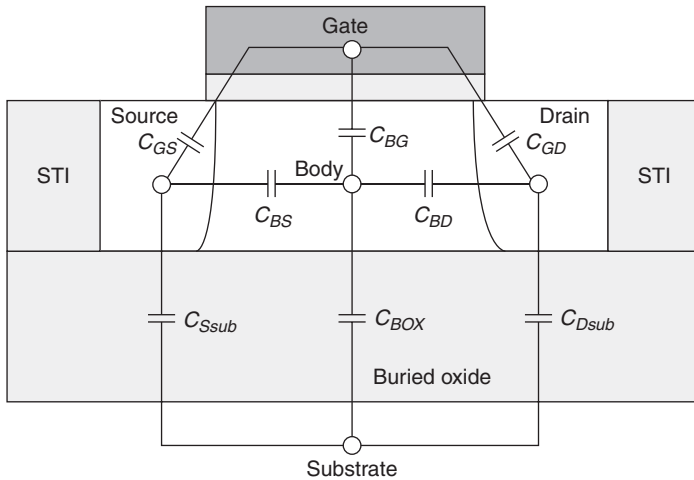
lower initial V_t provides higher transient drain current and faster switching than a comparable bulk device with the same doping. Further enhancements to the speed can come from impact ionization that builds up holes in the body, as illustrated in Fig. 4.1, thus further increasing the dynamic body voltage and lowering the dynamic V_t .

The floating body also provides significant enhancement for stacked devices as the body is not tied to the supply. For example, for an NMOS stack used in a NAND gate, the source node of the top NMOS device will rise above ground thus creating a back-bias on the top NMOS device in bulk CMOS. In SOI, the body of the top device will float up resulting in a reduced body effect (Bernstein and Rohrer, 2002, p. 44).

Overall, performance enhancements of ~20% were reported for many bulk designs that were ported over to SOI, including Mistry *et al.* (1997), Canada *et al.* (1999), Allen *et al.* (1999), and Bearden (2002). These correlate well with the composite results from the speed-up observed for different types of inverter chains in the study by Mistry *et al.* (1997). The delays for SOI vs bulk were 11% lower for the fixed capacitance loaded case, 17% lower for the unloaded case (FO1), and 35% lower for the junction capacitance loaded case. In another study (Aipperspach *et al.*, 1999), the inverter (FO1) improvement was 15% while a 4-input NAND improvement was 28% due to the reduced body effect relative to bulk.

It is important to note that when the PDSOI device I_{off} is matched to that of bulk, the device performance advantage is decreased somewhat. This occurs because the PDSOI device requires higher doping and higher linear V_t to achieve the same I_{off} due to the floating body which will end up between the source and drain voltages. One study shows that this effect results in a 2–3% drop in the SOI relative performance increase (Mistry *et al.*, 2000). An additional factor in the SOI vs bulk performance comparisons is the status of the bulk technology. When comparing the PDSOI performance against devices from a production 0.18 μm technology with optimized junction capacitance, the performance improvement was 16% and 8% for inverter chains with fanout = 1 and 4, respectively, when using consistent I_{off} assumptions (Mistry *et al.*, 2000). A Han–Carlson adder core made with these 0.18 μm technologies showed a 16% speed improvement for SOI over bulk (Mathew *et al.* 2001). As additional stress elements to improve performance are added to bulk and to SOI, these types of comparisons become more and more difficult as the elements that improve performance as well as their integration can be significantly different between the two types of technologies.

One significant factor that must be included in an evaluation of PDSOI vs bulk performance is the variation in the SOI delay due to the history effect. The body voltage of the PDSOI device depends on the history of the device as the body voltage, after remaining at a given state for a long time,



4.3 Capacitor coupling network of a PDSOI device that affects the body voltage.

will be set by the DC sources of current but, when the device is switched, the body voltage is modulated by changes in the gate, drain, and source signals that are capacitively coupled to the body, as seen in Fig. 4.3. For the NMOS device in the off state for a long time, the initial body voltage from the 65 nm example earlier was ~ 0.35 V. For a simple inverter, then as the input voltage goes high, the capacitive coupling of the NMOS gate to the body initially boosts the body voltage even higher, further enhancing the dynamic switching. As the output goes low, the body is then pulled down due to the capacitive coupling of the drain to the body such that the body voltage can drop below 0 V (Bernstein and Rohrer, 2002). If the NMOS device then remains in this state with $V_g = V_{dd}$ and $V_d = V_s = 0$ V, then the body potential will go to 0 V over time. As the NMOS device is turned off with V_g dropping back to 0 V, the body potential will rise as the output of the inverter switches high due to the drain to body coupling capacitance. The body potential that is reached after the output completes switching will depend on the starting value of the body together with the voltage changes that capacitively couple to the body. If the initial body voltage was below 0 V, then at the end of switching the body potential will be lower than if the body voltage had started at 0 V initially. As the device remains off, the body potential will adjust over time to the DC level equilibrium determined by the diodes to the body as described earlier. In one example by Bernstein and Rohrer (2002, p. 75), simulations showed ~ 150 mV range in the body voltage for a given state depending on the switching history.

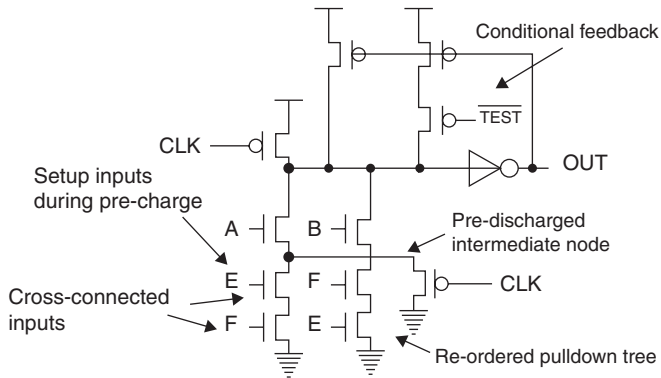
Typical delay variations for PDSOI technologies are in the range of 5–8% due to the history effect (Aipperspach *et al.*, 1999; Shahidi *et al.*, 1999; Mistry

et al., 2000; Celik *et al.*, 2002; Cai *et al.*, 2007). Mathew *et al.* (2001) had a breakout of the history effect between different types of inverter chains with data showing 7% delay variation for a simple inverter chain, 11% delay variation for 3-input NAND gates, and a 5% delay variation for a transmission gate chain. The history effect can be simulated on critical portions of the circuit to try and precisely bound for it, or a general bounding is often applied for the design or portions of the design. For example, Mathew *et al.* (2001) applied a 10% margin to all max-delay paths on their 0.18 μm PDSOI design which then made the advantage of the SOI technology over bulk be effectively 6%, although they were able to improve the performance by another 5% with an enhanced design utilizing the SOI devices.

4.3 Circuit solutions: digital circuits

One issue in some digital circuits due to the floating body is the high current that can flow in a NMOS PDSOI device when the gate is off and the source is switched from high to low while the drain has remained high. When the device is biased with the drain and source high and gate off for a long time, for example, in pass gates and dynamic circuits, the body accumulates charge and will rise up to the high level. Then, if the source is switched low, the body-to-source is forward biased and a significant bipolar current can flow. This effect caused the failure of some dynamic circuits in an initial attempt at a simple bulk to SOI design migration (Canada *et al.*, 1999).

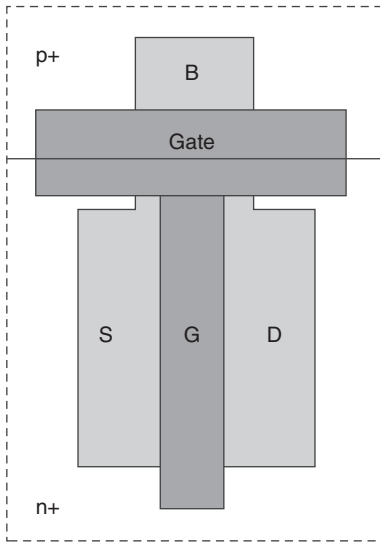
Figure 4.4 illustrates several techniques that have been used to make dynamic logic more robust against the PDSOI floating body effects (Aipperspach *et al.*, 1999; Allen *et al.*, 1999; Bernstein and Rohrer, 2002). One way to eliminate the bipolar turn-on is to pre-charge the intermediate nodes to a low or intermediate level. A PMOS pre-discharge device enables the CLK signal to be used for its gate signal. The modified pre-charge technique does require additional checking of charge sharing to ensure robustness. Also, pass-gate logic can be made robust to the bipolar effect by using similar discharge techniques, but at the expense of adding multiple devices to the logic gate (Kuang *et al.*, 1999; Redman-White and Bernstein, 2000). A second way to improve the dynamic logic robustness is to reorder the NMOS devices to place the widest group of devices at the bottom of the stack to reduce the overall bipolar current from the devices higher in the stack. A third improvement is to set up the inputs while the pre-charge is active. Another improvement can be made by rearranging the inputs in a cross-connected fashion where the gate of an upper device is connected to the gate of a lower device in a different leg. Then the worst-case bipolar current can be reduced in half. The domino design can also be modified such that any one output node has a fewer number of legs thus reducing the



4.4 Commonly used dynamic circuit techniques for PDSOI circuits. (Source: ©1999 IEEE. Reprinted, with permission, from Aipperspach *et al.* (1999), 'A 0.2- μm , 1.8-V, SOI, 550-MHz, 64-b PowerPC microprocessor with copper interconnects', *IEEE J. Solid-State Circuits*, **34**, 1430–1435.)

worst-case discharge. Also shown in Fig. 4.4 is the use of a half-latch gated by a test signal to provide additional feedback during special test modes at elevated temperature and voltage. Basic improvements to the dynamic logic robustness can be made by increasing the size of keeper PMOS device and by using longer gate lengths and/or higher V_i devices on the critical devices in the stack to reduce the bipolar current, although these changes can cause a trade-off with performance. Overall, extensive simulations are needed to guarantee that the design meets the performance requirements while being adequately robust. But, as V_{dd} drops with scaling, the bipolar current issues become much less problematic.

One way to eliminate most of the floating body effects is to use a body tie device to connect the body to a fixed potential or another signal. Figure 4.5 shows a simplified layout of a T-gate device. The active region is extended underneath and past the end of the gate contacted region (the head of the gate) to allow a connection to the body of the device. This type of device grows the area of the device significantly as well as adding much additional capacitance, so these devices are only used as necessary, typically in analog types of applications such as SRAM sense amps as discussed in Section 4.4. Even though the body is contacted, there can still be some partial floating body effects due to the large resistance of the body. The body resistance can be reduced by using an H-gate device in which the body tie construct is made on both sides of the device, but this ends up with even more area cost and higher capacitance. A source-body tie device can also be constructed by having n+ and p+ regions along the source side of the device and then shorting them together. But this type of device is not symmetrical and can have greater variation due to the



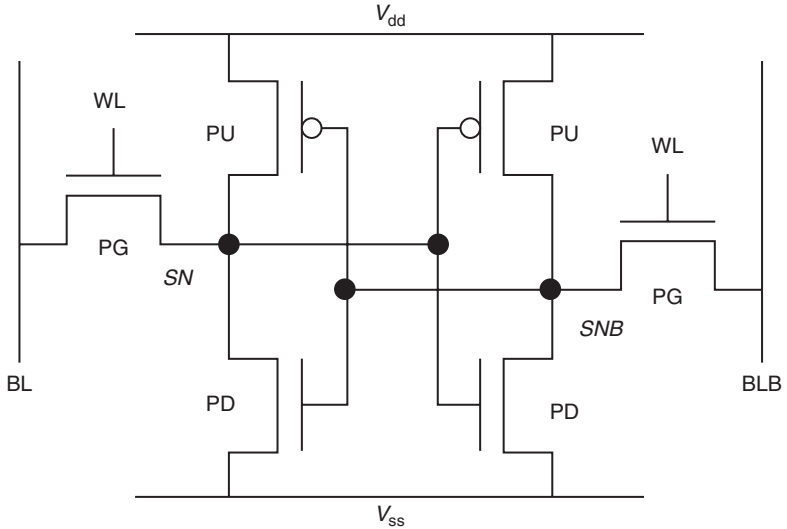
4.5 Top-down schematic of a body tie T-gate device used to provide a body connection to a PDSOI device where B, S, D, and G denote the body, source, drain, and gate regions, respectively (Burnett, 2006).

implant region variation, thus making the device undesirable for many applications.

4.4 Circuit solutions: static random access memory (SRAM) circuits

The amount of SRAM needed to support high performance processors continues to grow rapidly and drive technology scaling. The floating body effects can negatively impact the SRAM in many ways including degradations of the read stability of the cell, the ability of the write driver to successfully drive the bitline, and the functionality of the sense amp (Bearden, 2002; Joshi *et al.*, 2002; Pilo *et al.*, 2007; Ramadurai *et al.*, 2009).

As seen in the SRAM cell schematic in Fig. 4.6, the bitcell comprises six transistors consisting of matched pairs of NMOS pull-down (PD), NMOS pass-gate (PG), and PMOS pull-up (PU) transistors. The PD–PU inverters are cross coupled such that when one of the storage nodes is low, the other storage node is high. During the read operation, the wordline (WL) is turned on and the cell current (I_{cell}) flows through the PG and PD devices on the low side. Note that the bitlines are pre-charged high prior to starting the read operation. The storage node on the low side will rise up during the read due to the resistive divider formed with the series connected PD and PG devices. If the storage node voltage rises too high during the read, it will turn on the PD device on the high side of the cell and flip the state of the cell



4.6 Circuit schematic of a six transistor SRAM bitcell.

resulting in an error. For the write operation, the WL is turned on and one BL is pulled low while the other BL remains high.

At the beginning of the read operation, the body voltage and dynamic V_t of the PG on the low side being read will depend on the history of the bitcell. For example, at the completion of the write operation, the body voltage of the PG on the low side will be low. If the bitcell is then immediately read following the write, the body voltage will be at its lowest relative value for the read operation. During the next read operation, however, the body voltage will typically be higher as the BL voltage usually only falls 150–200 mV during the read operation or can remain at V_{dd} during a read disturb if the pre-charge is left on. The higher body voltage lowers the V_t of the PG device thus making it stronger and resulting in a higher storage node voltage during the read that can then flip the state of the cell. Thus, the transient operation of the bitcell must be considered carefully when optimizing the SRAM on PDSOI.

Several design techniques can be used to help mitigate the floating body effects during the read operation. The basic idea is to minimize the amount of the time the PG on the low side is exposed to a high BL level while the wordline is on. One effective technique is to float the unselected columns during the read and write operations (Joshi *et al.*, 2006). Traditionally, the pre-charge is left on for the unselected columns to minimize noise and dynamic power. By having the pre-charge turned off during the read and write operations, the bitcell will lower the BL voltage on the low side of the cell when the WL is turned on, thus reducing the body voltage on the

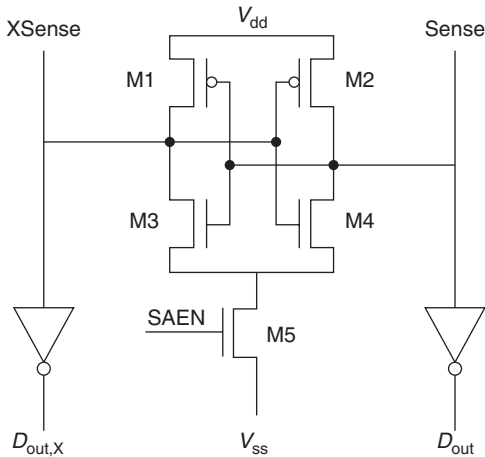
PG and the storage node voltage and making the cell less vulnerable to flipping.

Other effective techniques are available, but usually at the expense of area and architecture trade-offs. These include amplifying the BL signals with sense amps on every column (Pilo *et al.*, 2007), reducing the number of bits on the BL (Dorsey *et al.*, 2007; Pille *et al.*, 2007), and utilizing 8T cells that have a read port separate from the write port (Chang *et al.*, 2008; Jotwani *et al.*, 2011). In the 8T cell, the read port does not suffer from the resistive divider effects as the intermediate node in the PG–PD read stack is not connected to anything else. For the very high-speed L1 cache applications requiring a read followed by a write, Jotwani *et al.* (2011) found a substantial benefit in using the 8T cell as the write operation can be simultaneously performed with the pre-charge following the read operation thus resulting in more robust operation given the speed requirements.

For the write operation, the parasitic bipolar effect of the off PG devices connected to the BL can impact the write time needed. The worst case occurs when all the PG devices connected to a given bitline are from bits with a high state on the same side. Then, after the bitline has been pre-charged high for a long time, the bodies of all the PG devices will be at a high level. If a write operation to the opposite state is performed to one of these bits, then, as the bitline falls, the parasitic bipolar on all the off PG devices can turn on. This current can be large enough to swamp out the write driver device that needs to pull the BL sufficiently low for the write operation. Aipperspach *et al.* (1999) showed that this effect resulted in a 10% increase in the write time. Joshi *et al.* (2002) used a body contact device in the column bit select circuit to reduce the bipolar effect.

Another major concern in the SRAM design on PDSOI is the proper margining of the sense amp for the history effect. Figure 4.7 shows a schematic of a basic sense amp that comprises transistors M1–M5. The inverter formed by M1 and M3 are cross coupled with the inverter formed by M2 and M4. The enable transistor M5 is driven by the sense amp enable signal SAEN that activates the sense latch by pulling down the sources of M3 and M4. The NMOS devices, M3 and M4, form a matched pair and are the critical devices as they respond to the differential signal from the BLs that is applied to their gates. For the sense amp to function properly, the bitline differential at the time the sense amp turns on should be larger than the V_t mismatch of the matched pair M3 and M4. Note that the PMOS devices M1 and M2 act as loads and only have a second order effect on the latching operation. In general, M3 and M4 need to be sized appropriately to provide adequate mismatch and speed while consuming an acceptable amount of area.

During the sensing operation, a body voltage differential can develop between M3 and M4 if there are repeated reads of the same data state. If



4.7 Schematic of a latch style sense amp (Burnett, 2006).

there are repeated reads with a low on the Sense side and a high on the XSense side, then the body of M4 will be driven lower than the body of M3. This makes the V_i of M4 become higher than the V_i of M3, thus adding to whatever mismatch might already exist on the pair. Several studies have shown that if the bodies of M3 and M4 are left floating, a large body voltage differential can build up with values of 120–200 mV being reported resulting in additional V_i mismatches of 70–100 mV that must be accounted for (Aipperspach *et al.*, 1999; Canada *et al.*, 1999; Redman-White and Bernstein, 2000; Ramadurai *et al.*, 2009).

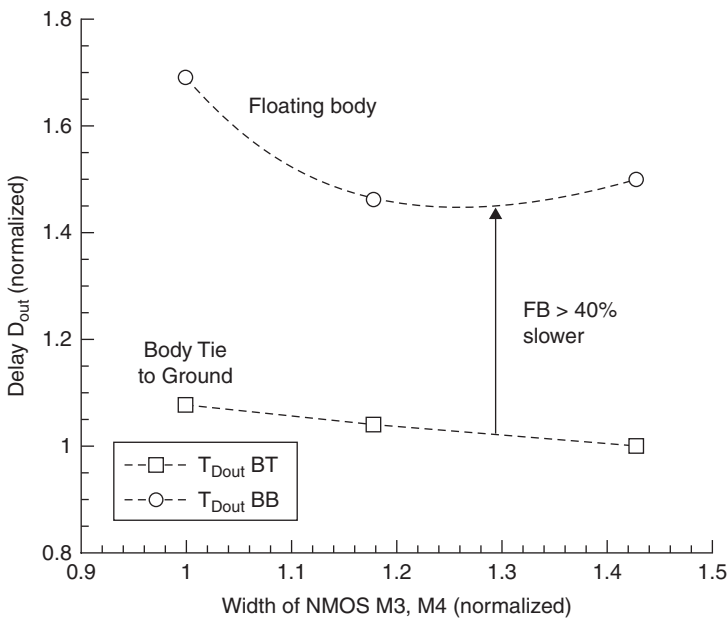
A V_i mismatch on the sense amp that is this large is very detrimental as a significant component to the SRAM access time which is the time needed to build up enough BL differential for worst-case bits to overcome the total V_i mismatch of the sense amp. If the body is left floating, then every sense amp can have these large mismatches to which the statistical V_i mismatches from random dopant effects and other sources then add. Thus, a body tie is usually added to the critical NMOS pair of devices in the sense amp where the bodies can be tied to ground (Ramadurai *et al.*, 2009) or cross-coupled to each other (Aipperspach *et al.*, 1999; Golden *et al.*, 2005).

A very useful study comparing the effect of the body tie on the sense amp NMOS matched pair was reported by Golden *et al.* (2005). The number of sense amp failures was recorded for 1 MB SRAM arrays with 20 224 sense amps with many arrays placed with different sense amp designs. The circuits then were tested under conditions to produce some failures on all the designs. The results showed more than a ten times reduction in failures when using a sense amp with body ties as compared to floating body devices

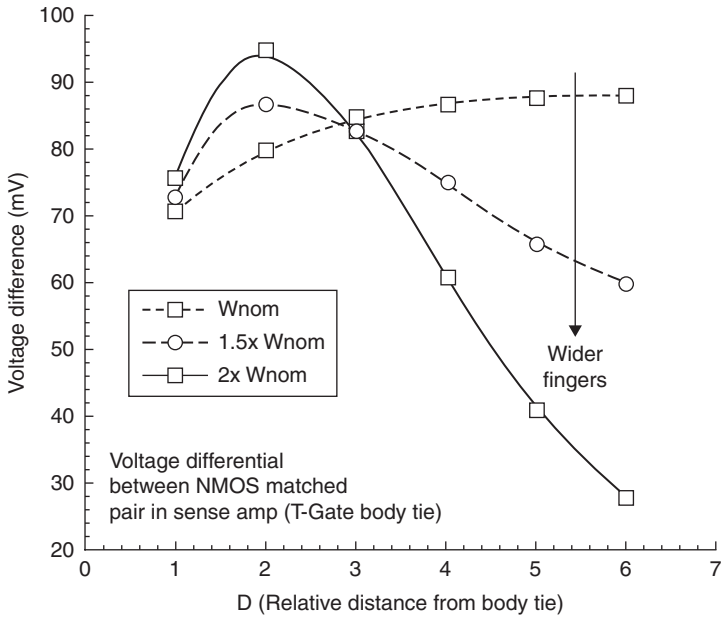
with a similar improvement independent of whether the bodies were tied to each other or tied to ground. They also demonstrated that the number of failures increases with the number of pre-reads as expected.

Although the body tied devices are not preferred for speed in logic relative to the floating body devices, the sense amp with body tied devices produces better SRAM delay results when comparing the time required for valid data. Figure 4.8 shows that the delay output from the sense amp is 40% slower when using floating body devices relative to the NMOS matched pair with their bodies tied to ground (Burnett, 2006). The effective V_t mismatch for the floating body devices in the sense amp application for the worst-case history is so large that the sense amp enable time must be pushed out significantly in order to obtain valid data.

Even when using body ties, though, a body differential can still build up in the matched pair of devices in the sense amp. Figure 4.9 shows the simulation results of the body voltage differential from a matched pair of devices in the sense amp that have their bodies tied to ground utilizing a T-gate device as shown in Fig. 4.5 (Burnett, 2006). The simulations use a model that segments the transistor along the width of the device in order to account for the resistive and capacitive effects of the body across the entire width. A body differential of up to 90 mV can still build up in the sense amp devices



4.8 Body tied sense amp devices require less time for valid data relative to floating body sense amp devices (Burnett, 2006).



4.9 Simulations of body voltage differential across the width of a matched pair of T-gate devices with bodies tied to ground in a sense amp application (Burnett, 2006).

even with the body ties. This is a result from the body tie not being completely effective in eliminating the floating body effects especially in fast switching transients as in high performance sense amps.

For the overall margining of the sense amp, the additional V_t mismatch in the case with body ties should be included as well. For example, in large SRAM arrays with 20 000 sense amps, a worst-case mismatch corresponding to a $5.3 \times$ sigma mismatch should be considered. If the sense amp NMOS transistor mismatch without any history effects is 8 mV for one sigma, then the expected worst-case V_t mismatch is 42 mV. The body differential as seen in Fig. 4.8 results in 16 mV additional effective V_t mismatch that needs to be added giving a total worst-case V_t mismatch of 58 mV. As seen in this example, the history effect even on body tied devices required an additional margining of almost 40% for the sense amp.

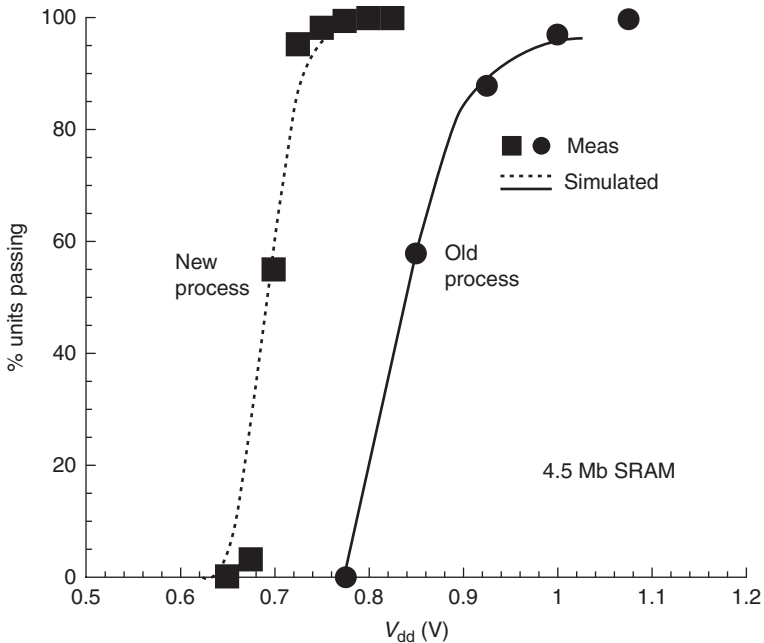
4.5 SRAM margining: PDSOI example

It is well-known that the minimum V_{dd} operation of large SRAM arrays is limited due to the V_t variations in SRAM cells (Burnett *et al.*, 1994; Bhavnagarwala *et al.*, 2001; Takeuchi *et al.*, 2001). As device dimensions

reduce with scaling and as L_{gate} is reduced to increase performance, the V_i variation worsens and degrades the low V_{dd} capability of the SRAM and ultimately limits the low power capability of products that utilize large SRAM arrays. This section looks at the local and systematic variation effects on a 130 nm SOI technology with 55 nm L_{gate} . By properly modeling the components of the static noise margin (SNM) variation, it is possible to accurately model the yield distribution of large SRAM arrays (4.5 Mb) across V_{dd} . Over 150 mV improvement in the $V_{dd,min}$ of this technology was realized by improving both the SNM and its variation (Burnett, 2006).

Figure 4.10 shows the low $V_{dd,min}$ yield distributions of 4.5 Mb SRAM arrays from a 130 nm PDSOI technology with a nominal L_{gate} of 55 nm (Celik *et al.*, 2002). The cell was optimized for high performance applications and has a PD to PG ratio of 3 with all gates drawn at the nominal L_{gate} . For the old process, the 107 samples of die shown in Fig. 4.10 all passed functionality at 1.2 V and have a median $V_{dd,min}$ of 0.85 V. From extensive testing, it was found that the first failing bits were due to read disturbs of the bit. Thus, the $V_{dd,min}$ of these arrays was limited by the SNM of the failing bits.

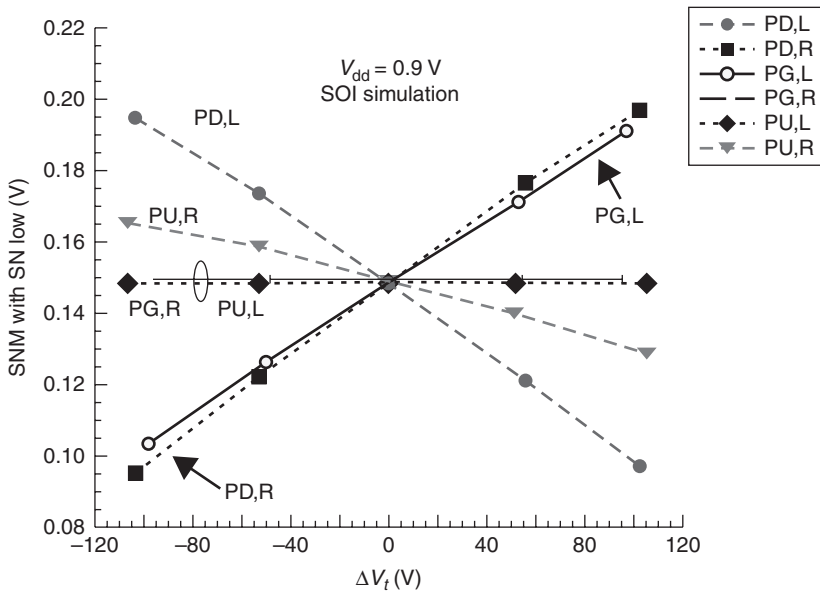
For the 6T SRAM cell, the SNM is expected to follow a normal distribution due to local variations in V_i of the bitcell devices (Bhavnagarwala



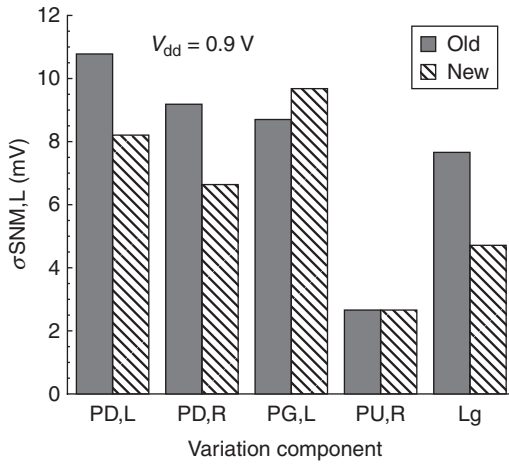
4.10 $V_{dd,min}$ yield distributions of 4.5 Mb SRAM arrays from a 130 nm PDSOI technology. Reduced variation in the SRAM devices improved the $V_{dd,min}$ distribution by ~ 200 mV (Burnett, 2006).

et al., 2001; Takeuchi *et al.*, 2001). This occurs because the SNM of the bitcell varies in a linear fashion with the V_t variation of each device and because the random V_t variation of each device is approximately normal. Thus, σ_{SNM} can be calculated as $\text{sqrt}(\sum(S_i \cdot \sigma_{V_{t,i}})^2)$ where $S_i = \Delta\text{SNM}/\Delta V_{t,i}$ is the sensitivity of SNM to the V_t variation of each of the six bitcell devices, i , and $V_{t,i}$ is the random V_t variation of each bitcell device and can be estimated from the mismatch statistics of each device pair as $\sigma_{V_t} = \sigma(\Delta V_t)/\sqrt{2}$. Simulations of the SNM show a good linear behavior with the V_t variation of the bitcell devices as expected (Fig. 4.11). The σ_{SNM} is then calculated from the S_i of each component together with the σ_{V_t} values of 21.2, 29.3, and 18.4 mV for the pull-down, pass gate, and pull-up devices, respectively, that are measured for the old process. As seen in Fig. 4.12, the pull-down device on the side being read (left) is the largest component of SNM variation with significant SNM variation also coming from the pass gate device on the same side (left) as well as the pull-down device on the other side (right).

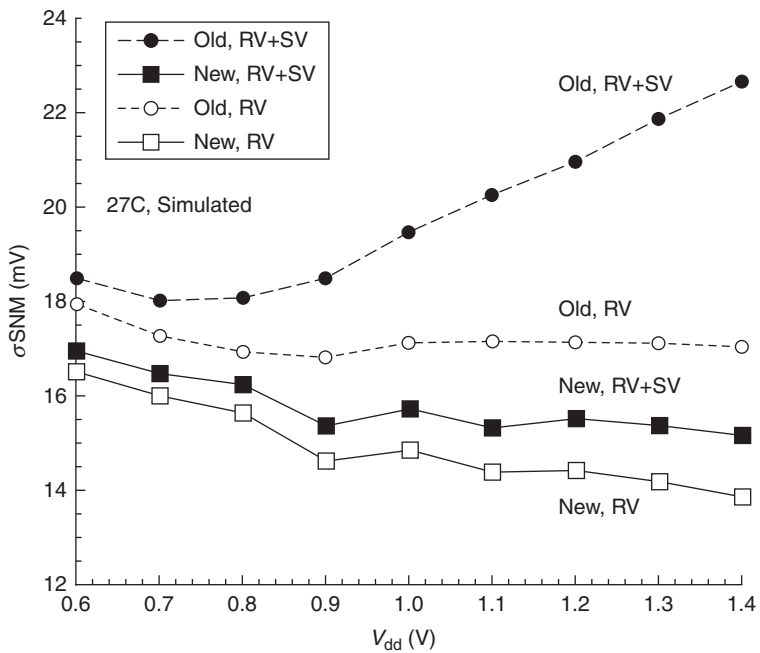
In order to account for systematic variations in SNM that will be reflected in a large sample size of die, simulations of the SNM as a function of L_{gate} were utilized to provide an estimate of the SNM variation with systematic variations in L_{gate} across the die, wafer, and lot. With S_L defined as the slope of the SNM vs L_{gate} curve at the nominal L_{gate} (55 nm), a systematic variation



4.11 Simulated static noise margin (SNM) dependence on the V_t of each device in a 6T SRAM cell from a PDSOI technology (Burnett, 2006).



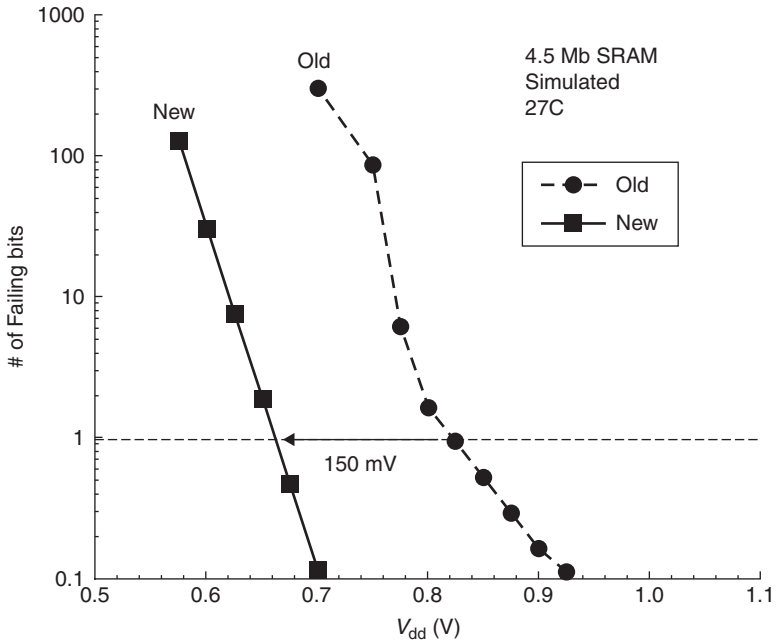
4.12 Simulated SNM variation by device component for a 130 nm PDSOI technology before and after optimization (Burnett, 2006).



4.13 Simulated SNM variation components due to random variation (RV) and systematic variation (SV) across V_{dd} for a 130 nm PDSOI technology (Burnett, 2006).

component of the SNM, $\sigma\text{SNM}_{\text{SV}}$, is calculated as $S_L \cdot \sigma L_G$ where σL_G is the one sigma estimate for the systematic L_{gate} variation (2.5 nm). With the random variation in SNM as defined previously, $(\sigma\text{SNM}_{\text{RV}})^2 = \sum(S_i \cdot \sigma V_{i,i})^2$, the total σSNM is calculated as $(\sigma\text{SNM})^2 = (\sigma\text{SNM}_{\text{SV}})^2 + (\sigma\text{SNM}_{\text{RV}})^2$.

Through optimization of the halo and extension implants and the spacer module, the short channel roll-off of the transistors was improved which resulted in less SNM sensitivity to L_{gate} variations. The SNM was improved in general by 10–20% through a 25 mV reduction in PU V_i and a 25 mV higher PG V_i with process maturity. Additional improvements in SNM by increasing the PG L_{gate} were not desirable due to the cell current requirements of the bitcell. To address the large SNM variation components due to the PD devices, the L_{gate} of the PD devices was increased to 80 nm in order to reduce the random V_i variation. With the 25 nm increase in L_{gate} , the V_i variation of the PD device improved by 25%, in good agreement with that expected from $\sigma V_i \propto (L_{\text{eff}})^{-0.5}$ (Bhavnagarwala *et al.*, 2001). With these changes, substantial improvements in the two PD components and the L_{gate} component are observed (Fig. 4.12), resulting in a 20% reduction in σSNM at 0.9 V as seen in Fig. 4.13.



4.14 Simulated bit fail count distribution showing a 150–200 mV lower minimum V_{dd} after optimization (Burnett, 2006).

The statistical distribution of bit failure was calculated using normal distribution statistics with the SNM mean and σ together with a minimum value of the SNM needed to function, SNM_{min}. The simulated bit fail distribution indicated an improvement in $V_{dd,min}$ of 150 mV for the optimized process with the upsized PD L_{gate} as compared to the old process, as shown in Fig. 4.14, and an improvement of 200 mV for the typical first failing bit in 10 units. With the SNM_{min} defined as 3% of V_{dd} , an excellent agreement in the low V_{dd} yield distribution of the 4.5 Mb units is observed for both processes (Fig. 4.10), in which the units with the new process consist of a sample size of 745 units and are tested at the worst-case ambient temperature of 90°C. With the SNM and σ SNM improvements, robust $V_{dd,min}$ below 0.85 V is observed for the new process.

4.6 Future trends

With scaling, there are several factors that make it difficult for PDSOI to maintain its advantages over bulk. As noted in the scaling study by Pelella and Fossum (2002), the dynamic capacitive coupling effects on PDSOI are reduced as the power supply voltage is scaled lower. Additionally, as V_{dd} is lowered, the delay variation percentage due to the history effect increases thus translating to additional margin that must be accounted for in the design with scaling (Mistry *et al.*, 2000). Another factor is the standby leakage of PDSOI relative to bulk especially given the ever increasing amount of memory required. As seen in Fig. 4.2, an order of magnitude increase in diode leakage occurred when scaling from 65 to 45 nm due to the heavier doping to manage the short channel effects (Cai *et al.*, 2008). Bulk has the advantage of having the well-to-source bias that can be adjusted to minimize the leakage, especially in memory arrays. Other factors that reduce the PDSOI advantage are the increasing relative impact of interconnect delay and the continued advances in bulk technology such as reduced junction capacitance (Mistry *et al.*, 2000) and stress elements that increase the performance, some of which may not translate as effectively to PDSOI. Despite these obstacles, a 22 nm PDSOI technology has been demonstrated with ~15% performance improvement over the previous 32 nm PDSOI technology by utilizing dual embedded source/drain stressors as well as dual-stress liners (Narasimha *et al.*, 2012).

In order to scale effectively, the industry is quickly moving to fully depleted (FD) devices, either on bulk or SOI. The bulk FinFET technology reported by Jan *et al.* (2012) utilizes doped fins that are thin enough at around 10 nm to be fully depleted, while planar FDSOI technology, researched for example by Weber *et al.* (2010) and Grenouillet *et al.* (2012), use a very thin, undoped silicon layer. In both cases, much improved subthreshold slope and short channel effects are realized that enable lower V_{dd} operation. While

the doped FinFET technology currently has better drive current capability, the undoped FDSOI planar technology realizes better matching. Additional details on FDSOI can be found in Chapter 5 of this book. Over time, many improvements to these technologies and advancements beyond these structures will be made that will enable Moore's Law to continue into the future (Kuhn, 2012).

4.7 References

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Planar fully depleted (FD) silicon-on-insulator (SOI) complementary metal oxide semiconductor (CMOS) technology

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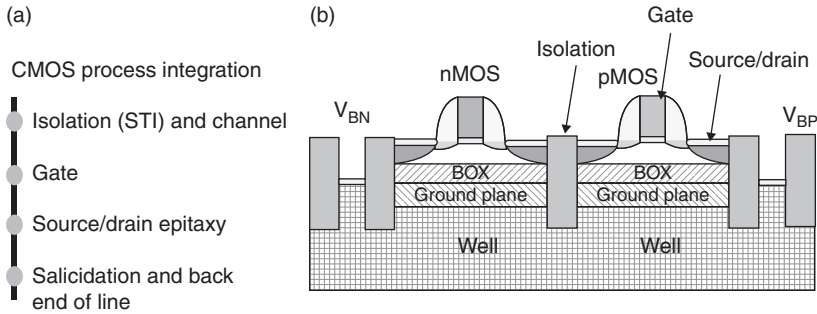
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Abstract: This chapter reviews the key features of complementary metal oxide semiconductor field effect transistor (CMOSFET) devices using planar fully depleted silicon-on-insulator (FDSOI) technology. First, it presents the FDSOI technology and then focuses on the impact of key integration steps on device performance and variability: channel thickness and doping, buried oxide (BOX) thickness, ground (or back-) planes, gate stack and mechanical booster (SiGe channel and source/drain, sSOI).

Key words: complementary metal oxide semiconductor field effect transistor (CMOSFET), planar fully depleted silicon-on-insulator (FDSOI), ultra-thin body and buried oxide (UTBB or UTB²), strain/stress, variability.

5.1 Introduction

This chapter reviews the key features of complementary metal oxide semiconductor field effect transistor (CMOSFET) devices using planar fully depleted silicon-on-insulator (FDSOI) technology. ‘Fully depleted’ means that the depletion region reaches the buried oxide (BOX) during the switch of the transistor from the OFF to the ON state. The depletion region is thus sandwiched between two oxides and limited by the SOI film thickness itself (see cross-section scheme of FDSOI nMOS and pMOS in Fig. 5.1). This confinement of the depletion zone does not exist for conventional planar architecture on bulk silicon substrates. FinFET or trigate architecture (Auth *et al.*, 2012) is also fully depleted. In trigate architecture the depletion region is restricted by the width of the active film, which is the minimum dimension of the device (and sometimes of the whole front-end and back-end technology). Conversely, in ‘planar’ architectures, the height of the active film is lower than its length and width (in-plane dimensions).



5.1 (a) Typical CMOS process integration and (b) schematic cross-section of an n- and pMOS on planar FDSOI. (STI – shallow trench isolation.)

This chapter explains the advantages of fully depleted devices, especially in terms of performance at low supply voltages (V_{DD}), which makes them the best solution for low-power applications. Not only low-power but also high-performance applications can be targeted by planar FDSOI. Indeed, planar FDSOI can be combined with other performance boosters such as mechanical stressors and high- k metal gate stacks (Ghani *et al.*, 2003; Auth *et al.*, 2008). These combinations can provide both the low power and high performance that are now required for mobile applications. Before presenting the performance of planar FDSOI, its main properties will be described. Section 5.2 provides a brief description of the technology and the main process modules of CMOS integration in planar FDSOI.

Threshold voltage (V_T or V_{th}) adjustment is critical when considering devices. Whereas threshold voltages are mainly adjusted by channel doping in bulk, this solution presents more drawbacks than advantages for FD devices. That is why V_T adjustment in FDSOI was previously considered an insurmountable problem for this technology. Solutions now actually exist. Section 5.3 details the technological solutions to centering n- and pFETs and adjusting the threshold voltage, V_T : channel doping, gate stack engineering and ground plane implantation.

Section 5.4 focuses on the substrate requirements in terms of silicon and buried oxide thicknesses. It is shown that scaling of these components is the main key to pursuing the overall scaling of this technology. The technological solutions to achieve high-performance pMOSFETs are then described: SiGe channel and SiGe source/drain integration are crucial (Section 5.5). One of the most efficient ways to boost nMOSFETs is the use of strained SOI (sSOI) substrates. Hence, Section 5.5.2 is dedicated to CMOS technology and devices on sSOI. Finally, Section 5.6 discusses the performance of planar FDSOI and makes comparisons with devices on bulk silicon.

5.2 Planar FDSOI technology

The technology of planar FDSOI and its associated challenges have been well described in the literature (see Raynaud *et al.*, 1994; Chau *et al.*, 2001; Doris *et al.*, 2002; Krivokapic *et al.*, 2002; Vandooren *et al.*, 2005). The process integration of CMOS on FDSOI does not differ substantially from that of bulk devices (see a typical process flow in Fig. 5.1). It starts with the isolation module. FDSOI does not require a particularly high depth of shallow trench isolation (STI) because of the electrical isolation provided by the BOX. However, to guarantee a similar sheet resistance of the well, plus ground plane and the co-integration of devices on bulk and FDSOI, it is possible for planar FDSOI to make use of similar STI and wells as those used on planar bulk technologies.

The ground plane or back plane, as mentioned earlier, is a highly doped region below the buried oxide. It can be obtained by ion implantation of classical dopants after the STI formation through the top silicon and the BOX. The doping level is typically in the order of a few 10^{18} at/cm³. This implantation is carried out just after the STI fabrication.

Before gate formation, the n and p channel must be completed. In particular, the importance of the SiGe channel for pFETs is explained in the following section. This can be done by epitaxy of the SiGe layer on top of the SOI (Andrieu *et al.*, 2006; Leroyer *et al.*, 2011) or by epitaxy and condensation or mixing, so that the complete region below the gate of the pFET is SiGe. The SiGe channel can be formed before or after the isolation module (Chen *et al.*, 2012). sSOI can be used as a channel material, in a similar way to SiGe. The advantages and challenges related to its integration are described below.

The gate stack is then formed. Since the advent of 45–32 nm technology nodes, the gate-first stacks include oxides of high permittivity, metal gates and poly capping. The sources/drains integrate *in situ* P-doped Si or SiC (with 1–2% C) for nMOS and *in situ* B-doped SiGe for pMOS. The *in situ* doping leads to a high level of dopants; C slows down the diffusion of P and both SiGe and SiC induce strain in the channel of the CMOSFETs (if the strain is well conserved during the entire CMOS process flow).

The rest of the process integration is very similar to that used in planar bulk technologies. The key process steps of planar FDSOI technology are discussed in the next section, highlighting their main features and challenges in respect of CMOS devices, especially the threshold voltage adjustment in FDSOI.

5.3 V_T adjustment on FDSOI: channel doping, gate stack engineering and ground planes

The threshold voltage (V_T) can be defined by several methods including: gate voltage corresponding to a given potential at the interface between

the channel and the gate oxide of the MOS, or by capacitive considerations (Poiroux *et al.*, 2011). When considering the drain current (I_D) vs gate voltage (V_G) characteristics, V_T is the limit between the exponential part (described by the subthreshold slope) and the linear or power part. In order to adjust the OFF state current (I_{OFF}) of a transistor, V_T must be adjusted. Moreover, for some applications, such as system-on-chip (SoC), transistors with different V_T values (i.e., a ‘multiple- V_T ’ or ‘multi- V_T ’ platform) are required. High-speed (low V_T (LVT) or super-low V_T (SLVT)) transistors provide I_{OFF} values in the range of tens to hundreds of nanoamperes per micron (nA/ μm) of transistor width. Low-leakage (so-called regular or standard V_T (RVT or SVT)) transistors, on the other hand, provide I_{OFF} of a few nA/ μm . A multi- V_T solution is useful in order to adjust the trade-off between speed and energy consumption in a circuit. Finally, static random access memories (SRAMs) need a higher threshold voltage (HVT) and I_{OFF} of a few tens of picoamperes per micron.

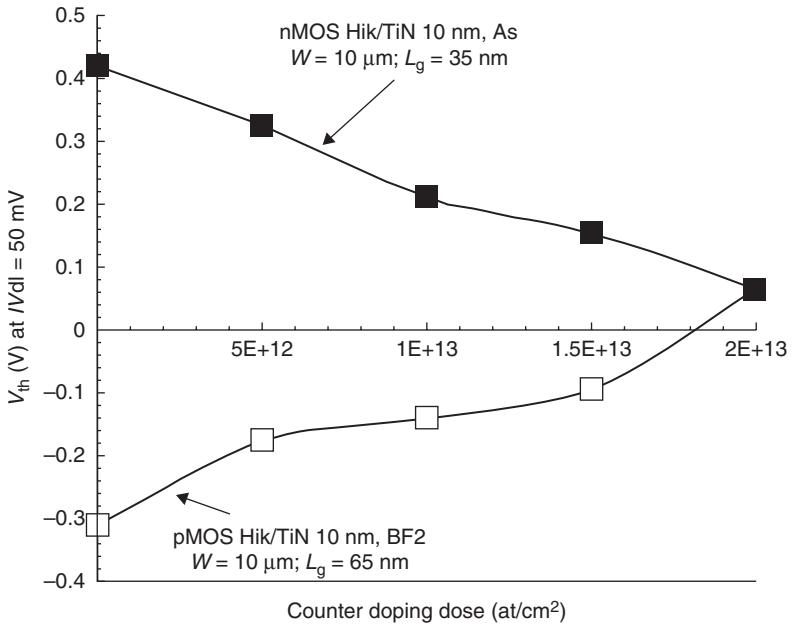
The ability to adjust the threshold voltages in a CMOS technology is therefore very important. In addition, not only the nominal V_T value of a device, but also its distribution must be finely controlled. The V_T variability is probably one of the most significant challenges of the sub-32 nm nodes. It is often characterized by V_T matching, that is, the standard deviation of the difference in V_T between two close transistors (Mazurier *et al.*, 2012).

In this section, the classical ways to adjust the threshold voltage in bulk silicon are discussed, with a view to their efficiency and drawbacks in planar FDSOI. Particular attention is paid to V_T variability. A solution is also proposed in order to adjust the threshold voltages in FDSOI.

5.3.1 Channel doping

The threshold voltage of n- and pMOSFETs is almost equal to 0.45 V with an undoped channel and a single gate of a workfunction close to the midgap (see Shimada *et al.*, 1997; Poiroux *et al.*, 2011). This value may be suitable for low-leakage transistors and SRAMs, but not for high-speed transistors. In order to lower V_T , channel doping can be used, as conventionally employed in bulk silicon. However, in order to lower the threshold voltage, a channel counter-doping (i.e., channel doping of the same type as that used for the source/drain) is necessary. The higher the channel counter-doping (e.g., Arsenic for nMOS and Boron for pMOS), the lower the V_T .

The method described above can be used in FDSOI, as illustrated by Fig. 5.2. Its sensibility is around 42 mV per 10^{18} at/cm³ doping concentration for both nMOS and pMOS with short channels (Buj-Dufournet *et al.*, 2009; Fenouillet Béranger *et al.*, 2009). This can be directly attributed to the



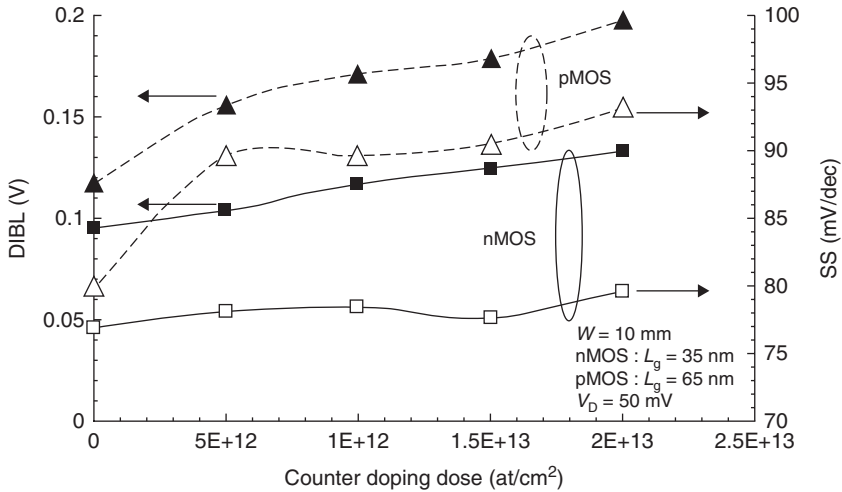
5.2 Effect of a counter-doping dose on nMOS and pMOS FDSOI devices on the short-channel threshold voltage in planar FDSOI. Each 5×10^{12} at/cm² implanted dose corresponds to 2×10^{18} at/cm³ doping concentration. SOI thickness, t_{Si} is 10 nm; BOX thickness is 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO₂/TiN gate stack) and drain induced barrier lowering (DIBL) around 100 mV/V for both n- and pMOS. (Source: Buj *et al.*, 2009. Copyright 2009, The Japan Society of Applied Physics.)

change of depletion charge (and depletion capacitance) in the channel of the MOS. The drawbacks of this method, however, are the degradations of:

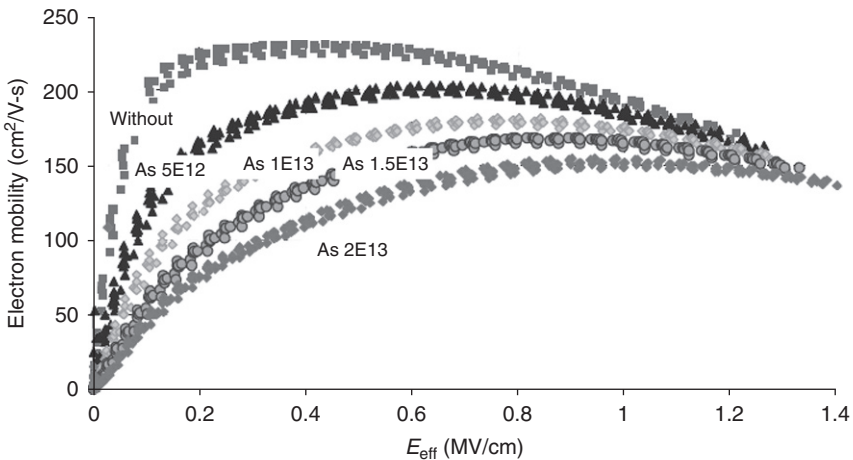
- short-channel effects (characterized by V_T vs gate length curve at low drain voltage, V_D , the drain induced barrier lowering (DIBL) and most of all the subthreshold slope);
- carrier mobility in the channel of the transistor; and
- V_T variability (Buj-Dufournet *et al.*, 2009; Fenouillet Béranger *et al.*, 2009).

Figure 5.3 depicts the evolution of DIBL against the counter-doping dose for the same devices as in Fig. 5.2. A DIBL degradation is revealed in the range of 2–8 mV/V per 10^{18} at/cm³ doping concentration, compared to undoped-channel transistors with DIBL equal to 100 mV/V.

Actually, both the electrostatics and the carrier transport are degraded. Figure 5.4 presents the effective mobility of electrons in long-channel



5.3 Drain induced barrier lowering (DIBL) and subthreshold slope of short n- and pMOSFETs as a function of the counter-doping dose. Each $5 \times 10^{12} \text{ at/cm}^2$ implanted dose corresponds to $2 \times 10^{18} \text{ at/cm}^3$ doping concentration. SOI thickness, t_{Si} , is 10 nm; BOX thickness is 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO_2/TiN gate stack) for both n- and pMOS. (Source: Buj *et al.*, 2009. Copyright 2009, The Japan Society of Applied Physics.)



5.4 Long-channel electron mobility as a function of the effective field for various implanted doses. Each $5 \times 10^{12} \text{ at/cm}^2$ implanted dose corresponds to $2 \times 10^{18} \text{ at/cm}^3$ doping concentration. SOI thickness, t_{Si} , is 10 nm; BOX thickness = 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO_2/TiN gate stack) for both n- and pMOS. (Source: Buj *et al.*, 2009. Copyright 2009, The Japan Society of Applied Physics.)

devices *vs* the inversion charge for the different counter-doping doses. It is worth noting that the electron mobility is lowered, mainly at low inversion charge. This is caused by Coulomb scattering. The hole mobility follows the same trend. Finally, the V_T variability is also degraded by the channel doping. Indeed, the contribution of the random dopant fluctuation in the V_T standard deviation is proportional to

$$\sigma V_T \sim T_{\text{inv}} \cdot \frac{\sqrt[4]{N_{\text{dop}}}}{\sqrt{W \cdot L}}$$

where T_{inv} is the electrical gate oxide thickness in inversion; N_{dop} is the channel doping concentration; and W and L are the gate width and length, respectively. The suppression of the random dopant fluctuation is one of the major advantages of undoped-channel FDSOI (see Faynot *et al.*, 2010 and references therein). The addition of counter-doping in the channel of the transistor strongly degrades its V_T variability.

To summarize, there are many drawbacks related to channel counter-doping. Incidentally, similar conclusions related to carrier mobility and V_T variability can be drawn for channel doping (i.e., when the channel is p-doped for nMOS and n-doped for pMOS, respectively). As a consequence, in FDSOI, undoped channels are not only possible, but also advantageous for carrier mobility and V_T variability. However, this means that other solutions are needed in order to adjust V_T values in FDSOI. One of the main levers is gate stack engineering, as used in bulk Si technology.

5.3.2 Gate stack engineering

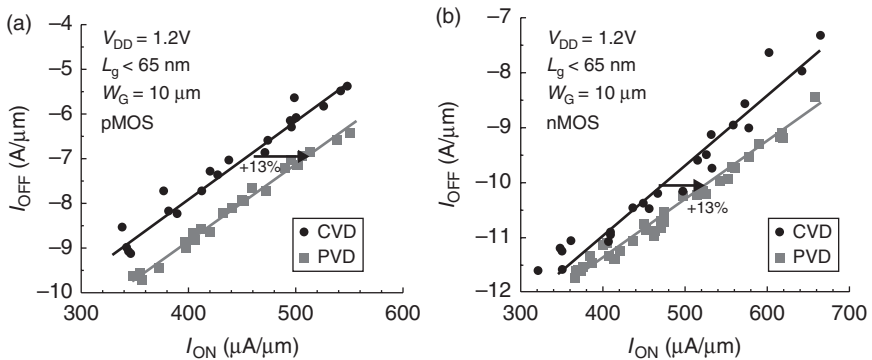
The effective gate workfunction that is required for FDSOI, depends on channel doping, as illustrated by Shimada *et al.* (1997). In FDSOI, a band-edge gate (n+ for nMOS and p+ for pMOS) and a highly doped channel (as illustrated by Gallon *et al.*, 2005) can be used or, alternatively, an ‘undoped’ channel and a gate, whose workfunction is close to the midgap. Clearly, the latter solution is preferred (as discussed previously), even if acceptable compromises might be found with a reasonable channel doping level.

TiN material, when integrated in a gate first, is a good candidate for use as a midgap gate. Its workfunction (and the gate stack properties: gate current, carrier mobility, reliability, equivalent oxide thickness (EOT)) varies with its thickness, mainly when integrated on hafnium-rich dielectrics (Fenouillet *et al.*, 2009; Brunet *et al.*, 2010). Its deposition process is also a key parameter defining transistor electrical performance. For example, TiN carried out by physical vapour deposition (PVD) and chemical vapour deposition (CVD) have been compared in a gate-first approach in FDSOI

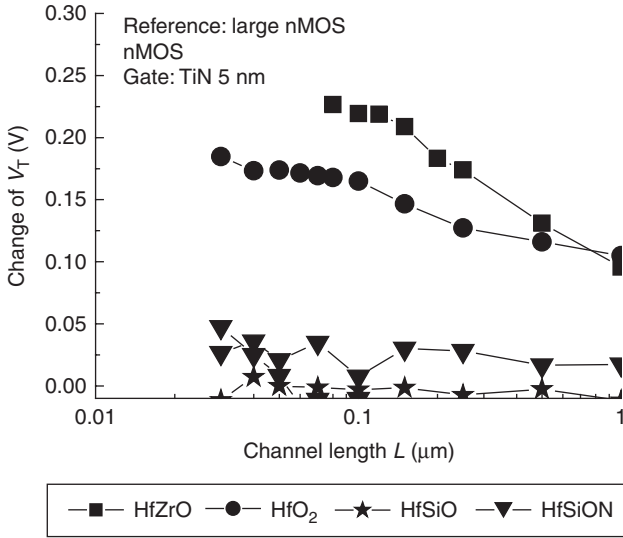
with 3 nm atomic layer deposited (ALD) HfO_2 gate oxide (Andrieu *et al.*, 2006). The principal findings are that CVD TiN yields better long-channel characteristics in terms of carrier mobility, time-dependent dielectric breakdown (TDDDB) and negative bias temperature instability (NBTI). However, ultimately, the scalability down to 25 nm gate length FDSOI CMOSFETs is found to be better with PVD than with CVD TiN (Fig. 5.5). This can be attributed to an interfacial layer regrowth with CVD TiN by oxygen diffusion from the edges of the gate. This indicates that the gate and spacer deposition/patterning are critical steps, which must be optimized so as to avoid degrading the physical and electrical characteristics of short-channel transistors.

Oxygen diffusion can also occur in the gate width direction, inducing narrow-channel effects up to about 200 mV with some gate stacks (Brunet *et al.*, 2010). Figure 5.6 shows this narrow-channel effect and its dependence on the high-k material in ALD TiN. The V_T shift is about 200 mV for both HfO_2 and HfZrO oxides, which are crystallized, whereas it is limited to 30 mV for amorphous HfSiO(N) oxides. This V_T instability appears on both nMOS and pMOS with the same sign and magnitude, indicating that it is related to a change of the metal workfunction, resulting from uncontrolled lateral diffusion of oxygen through the spacers (in agreement with in-depth physical characterizations). Amorphous HfSiON oxides offer better resilience against this effect, even when dopants such as Al are incorporated in the gate stack.

To summarize, TiN material is a good candidate metal for use in a FDSOI gate-first approach (workfunction close to the midgap or n-type). Careful



5.5 ON state current/OFF state current (I_{ON}/I_{OFF}) trade-off for PVD and CVD gated (a) pMOSFETs and (b) nMOSFETs. Devices have been integrated with 3 nm ALD HfO_2 (post-annealed at 600°C during 15 min) + 10 nm TiN + 50 nm n+-doped poly-silicon layers. Either a PVD TiN (100°C , 6 kW) or a CVD TiN (680°C with NH_3 and TiCl_4 as precursors) was deposited. SOI thickness, t_{Si} , is 10 nm; BOX thickness = 145 nm; equivalent oxide thickness is around 1.6 nm for both nMOS and pMOS.

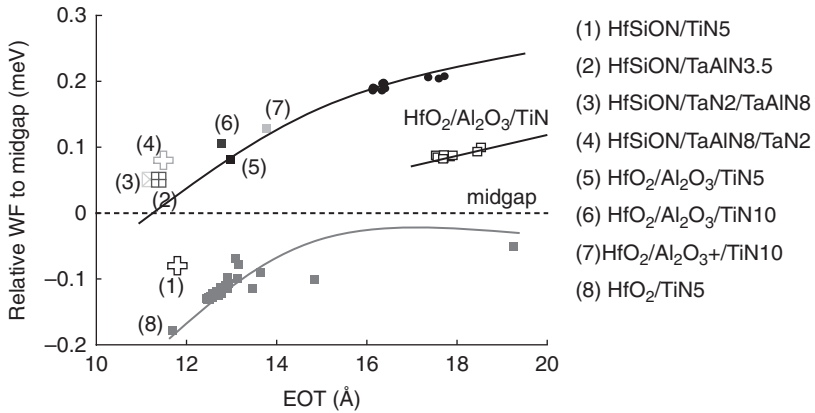


5.6 Threshold voltage (V_T) difference between large and narrow nMOS transistors ($\Delta V_T = V_T(W = 80 \text{ nm}) - V_T(W = 10 \mu\text{m})$) vs channel length L for various high-k oxides with 5 nm TiN gate. ΔV_T is drastically reduced for HfSiO(N) compared to HfO₂ and HfZrO. SOI thickness, t_{SiO_2} is around 7 nm; BOX thickness is 25 nm; equivalent oxide thickness is around 1.2 nm.

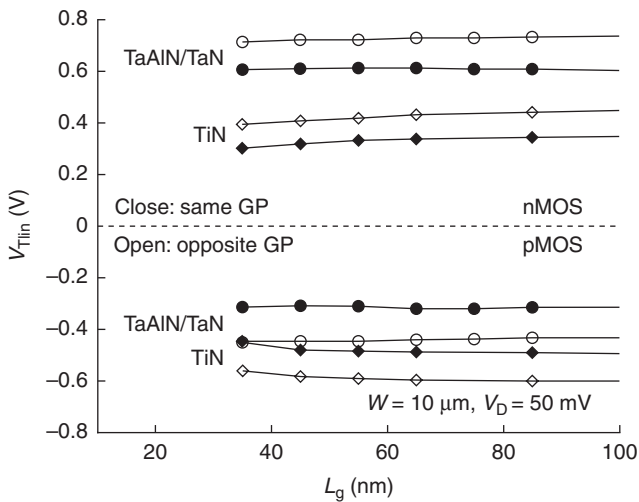
attention should be paid to its integration (gate and spacer deposition and patterning) in order to maintain good stability of this material vs the transistor dimension.

On the other hand, it is challenging to find a p-type gate in a gate-first integration scheme. This problem also exists for devices on bulk silicon. It is even more severe because p+ gates (workfunction of about 5.1 eV) are required in planar bulk silicon. This problem has been solved by the use of the gate-last integration scheme for transistors in bulk silicon (Auth *et al.*, 2008) or FDSOI (Morvan *et al.*, 2013). Indeed, in the gate-last approach, the junction anneal is completed before the metal gate deposition. This prevents (or reduces) the instability of the metal workfunction induced by the thermal budget (mainly observed on pMOS for small EOTs), as generally evidenced in the literature and termed ‘flat-band voltage (VFB) roll-off’.

The detrimental trend obtained for different gate stacks integrated using the gate-first approach is shown in Fig. 5.7 for gate stacks containing aluminium (Al) species. Al creates a dipole in the gate stack that shifts the workfunction towards a positive value. However, Fig. 5.7 shows a large roll-off of the flat-band voltage with Al₂O₃ or TaAlN gates, depending on TiN thickness (5 or 10 nm) and the high-k used. This is a general trend for p-gate material integrated in a gate-first process flow. Workfunctions



5.7 Effective workfunction (WF) relative to the midgap of silicon vs equivalent oxide thickness (EOT) for different gate stacks with or without Al atoms. This is measured on long/large devices. (Source: © 2010 IEEE. Reprinted with permission from Weber *et al.*, 2010.)



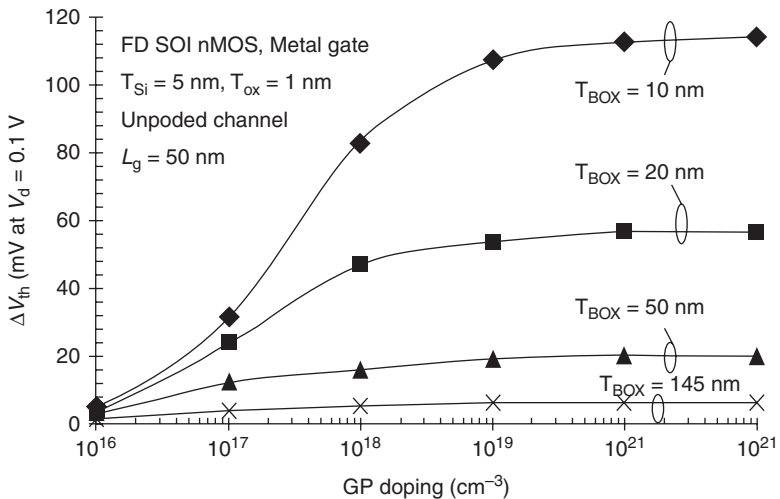
5.8 Threshold voltage vs gate length for nMOS and pMOS with N-type (TiN) and P-type (TaAlN/TaN) metal gates and N-type or P-type ground planes (GP). SOI thickness, t_{Si} , is around 7 nm; BOX thickness is 10 nm; equivalent oxide thickness is around 1.2 nm (Source: © 2010 IEEE. Reprinted with permission from Weber *et al.*, 2010.)

of 80 mV above the midgap are demonstrated with TaAlN gates (Weber *et al.*, 2010). This is sufficient for FDSOI, leading to a threshold voltage of 0.32 V for pMOSFETs (Fig. 5.8) with good NBTI and hole mobility. A workfunction difference of about 70–100 mV between two different gates is enough to induce a one decade I_{OFF} difference in the device, and thus to build a multi- V_T offer.

5.3.3 Ground planes

Finally, there is another mean to adjust V_T values, namely, the ground planes (or back planes). Indeed, ground planes play the same role as a biased back gate. Owing to the vertical coupling (caused by the fully depleted film), the workfunction of the ground plane is as important as that of the front gate. This effect is described below.

The ground plane (GP) doping changes the threshold voltage of the front gate, as illustrated in Figs 5.8 (type of doping) and 5.9 (level of doping) (see also Gallon *et al.*, 2006; Weber *et al.*, 2010). Moreover, Fig. 5.9 shows that for a 20 nm BOX thickness and a ground plane doping around a few 10^{18} cm^{-3} , there is a plateau of the V_T against GP doping curve. This explains the low impact on variability (lower than the impact of the channel doping concentration on the V_T in bulk silicon). Indeed, measurements show a negligible



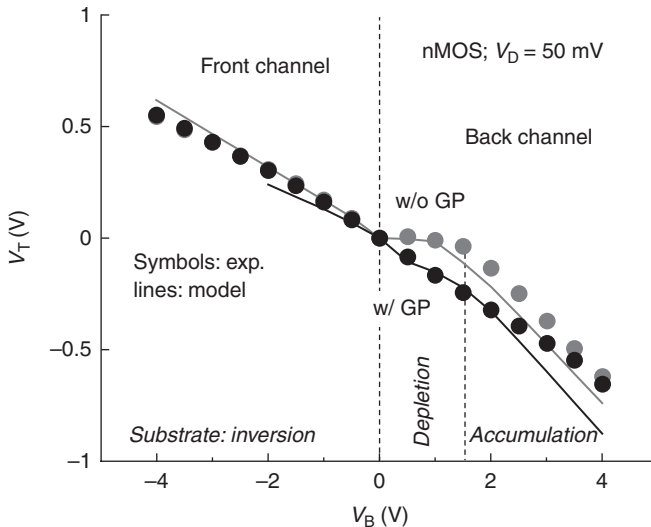
5.9 Simulated variation of the threshold voltage vs the ground plane doping. Gate length, L , is 50 nm; SOI thickness, t_{Si} , is 5 nm; equivalent oxide thickness is 1 nm (Source: © 2006 IEEE. Reprinted with permission from Gallon *et al.*, 2006.).

impact of the ground plane on the carrier mobility in the channel and on the V_T variability (Andrieu *et al.*, 2012; Mazurier *et al.*, 2012).

The ground plane could therefore be used to adjust the threshold voltage, but its main feature (and justification) is probably its capability to ensure a good back bias effect (similar to the ‘body’ bias sometimes used on planar bulk technologies). In order to maximize this sensibility of the back bias to the front gate threshold voltage, the ground plane is important. Indeed, a high level of ground plane doping makes it possible to suppress the depletion of the substrate in the forward regime (i.e., for a positive back bias of the nFETs $V_{BN} > 0$ (as shown in Fig. 5.10 and modelled by Mazellier *et al.*, 2008).

It is important to note that if the applied static back bias is the same as that used classically in bulk Si (back bias polarization of $V_{BP} = V_{DD}$ on pMOS and $V_{BN} = \text{GND}$ on nMOS, with V_{DD} and GND being the supply voltage and the ground), as can be seen on Fig. 5.1, an n-doped well (namely nwell) is required for pMOS (and a p-doped well (pwell) for nMOS, respectively) to avoid putting the nwell/pwell diode in a forward regime (Noel *et al.*, 2011).

Incidentally, also in Fig. 5.1, it can be seen that a front-side contact is needed, as well as a silicon and BOX opening, in order to create a ‘NO-SOI’



5.10 Long-channel threshold voltage vs back bias from experiments and model with and without ground plane doping. SOI thickness, t_{Si} , is 7 nm, BOX thickness is 10nm; equivalent oxide thickness is 1.3 nm (Source: © 2010 IEEE. Reprinted with permission from Andrieu *et al.*, 2010.)

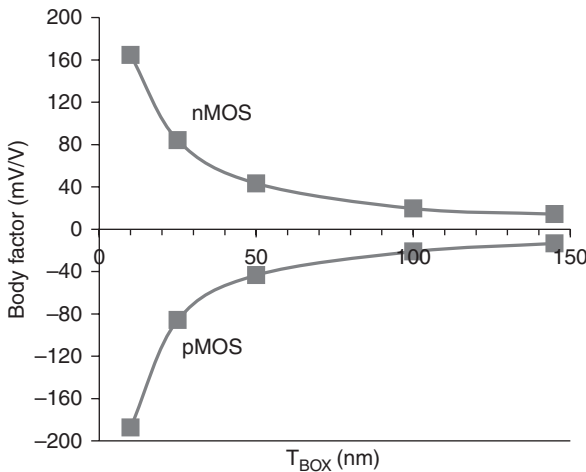
or ('NOSO') window and polarize the substrate. This is an additional step compared to the technology in bulk. Besides this well tap, the NO-SOI module enables the co-integration of FDSOI and bulk devices in a so-called hybrid platform. A part of the bulk designs could be thus directly transferred from bulk to a hybrid FDSOI/bulk platform (Golanski *et al.*, 2013). In particular, electrostatic discharge ESD protection can be done on the bulk silicon substrate in order to benefit from a large diode surface and reduced self-heating effect (Benoist *et al.*, 2010).

5.4 Substrate requirements for FDSOI CMOS devices: BOX and channel thicknesses

The main SOI substrate features are the BOX and channel thicknesses. This section will describe what are the requirements relative to these parameters in order to optimize CMOS devices.

5.4.1 Impact of BOX thickness on back bias efficiency

The BOX thickness is mainly selected according to the back bias (V_B) efficiency requirement. From Fig. 5.10, it is possible to extract a slope of the V_T vs V_B curve called the γ -factor. With ground planes, γ does not depend particularly on the back bias, but principally on BOX thickness, T_{BOX} . This is



5.11 Body factor (γ) vs the BOX thickness in the forward body bias (FBB) regime ($V_{\text{BN}} = +450$ mV for nMOS and $V_{\text{BP}} = -450$ mV for pMOS) at $L = 1$ μm gate length. Results obtained by technology computed-aided-design (TCAD) simulations performed on an undoped FDSOI nMOS with a physical gate oxide thickness of 1 nm and $t_{\text{Si}} = 8$ nm.

illustrated in Fig. 5.11. These characteristics are probably the most important in the choice of BOX thickness for a planar FDSOI technology. Indeed, it will be seen in the final section of this chapter that this body effect makes it possible to dynamically improve the performance and optimize the energy \times delay product of a circuit. From such a circuit specification, and using Fig. 5.11, it is possible to determine the required BOX thickness for a given technology node.

Furthermore, a thinner BOX, on an ultra-thin buried oxide and body (UTBB or UTB²) with ground plane, results in a smaller DIBL because of the suppression of fringing fields from the drain to the body through the BOX (Ernst *et al.*, 1999). From this point of view, a BOX with a low dielectric permittivity (low- k) is beneficial. However, this effect is second order, compared to the strong influence of the channel thickness on the electrostatics of the transistor.

5.4.2 Impact of channel thickness on short-channel effects, V_T variability, access resistance and carrier mobility

In bulk technologies, the channel doping ensures good electrostatics of short-channel devices. On the other hand, for undoped-channel FDSOI, film thickness is the principal parameter to govern the short-channel effect. Indeed, classical models predict that DIBL is given by:

$$\left. \frac{dV_{th}}{dV_{DS}} \right|_{V_{DS}=0V} = -\frac{1/2}{\cosh(L/2\lambda) - 1} \quad [5.1]$$

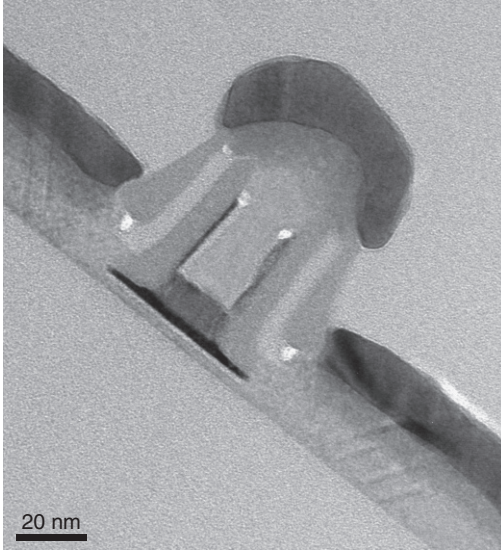
where λ is the scaling characteristic length of the technology (Suzuki *et al.*, 1993), for single gate transistor given by:

$$\lambda = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}} t_{Si} \left(t_{ox} + \frac{\epsilon_{ox}}{\epsilon_{Si}} \frac{t_{Si}}{2} \right)} \quad [5.2]$$

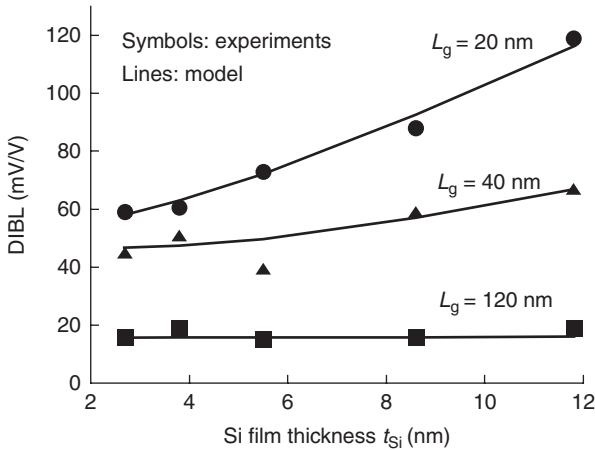
where t_{Si} is the channel thickness.

These expressions show that the DIBL decreases when t_{Si} (i.e. the channel thickness) decreases, and that a ratio of about 4 between the minimum channel length and the silicon film thickness is required to ensure DIBL values below 100 mV/V.

This trend of DIBL(t_{Si}) was clearly confirmed by experimental measurements conducted on planar FDSOI for different channel thicknesses down

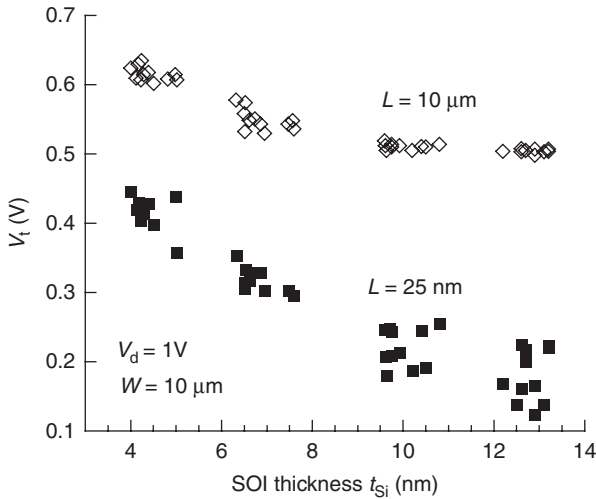


5.12 Transmission electron microscope (TEM) cross-section figure of 18 nm gate length strained SOI (sSOI) nMOSFET with 2.5 nm channel thickness.



5.13 DIBL as a function of the Si film thickness for various gate lengths. Comparison between experimental and modelling results. BOX thickness is 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO_2/TiN gate stack).

to $t_{Si} = 2.5$ nm (Figs 5.12 and 5.13). However, for very small film thicknesses, a plateau of $\text{DIBL}(t_{Si})$ exists, where DIBL is mainly controlled by the fringing fields through the BOX (Barral *et al.*, 2007). This component represents

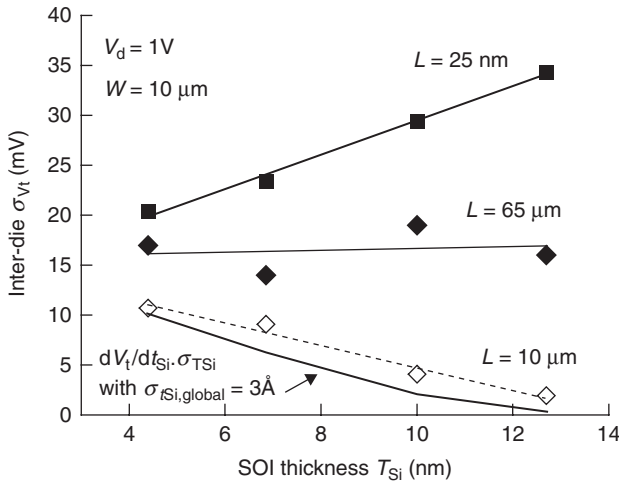


5.14 Threshold voltage (V_T) vs channel thickness (t_{Si}) at $L = 10 \mu m$ and 25 nm gate length for four t_{Si} thicknesses (four different wafers). For each wafer, t_{Si} is measured precisely by ellipsometry. BOX thickness is 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO_2 /TiN gate stack). (Source: © 2008 IEEE. Reprinted with permission from Weber *et al.*, 2008.)

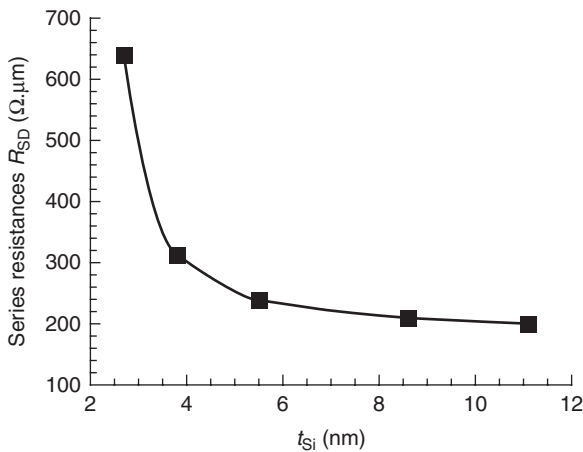
about 18% of the total DIBL at 18 nm gate length but overall, reducing t_{Si} generally makes it possible to improve the short-channel effect and lower the OFF state current of the device. Significant improvements of roll-off, subthreshold swing and DIBL are possible with t_{Si} reduction, reaching values as low as 67 mV/dec (subthreshold swing) and 75 mV/V (DIBL) for 18 nm short transistors and $t_{Si} = 4$ nm.

This improvement of the short-channel effect explains why V_T increases when t_{Si} is scaled down on short-channel devices (Fig. 5.14). Similar behaviour is observed on long-channel devices in the same figure, but this time attributable to the quantum confinement. These different causes between short and long devices result in a different response in terms of V_T variability (Fig. 5.15). On the one hand, the improvement of short-channel effects for small t_{Si} improves the variability in short channels thanks to a reduction of the $V_T(L)$ sensibility; on the other hand, the quantum confinement increases the sensibility of $V_T(t_{Si})$ and, in turn, the variability in long-channel devices (Weber *et al.*, 2008).

This behaviour was confirmed recently and extended to the local variation of t_{Si} (surface roughness) (Hook *et al.*, 2011; Mazurier *et al.*, 2012). Indeed, all the variations of t_{Si} (both local and global) play an important role in V_T variability. If the long-channel V_T variability is governed by the



5.15 Standard deviation of the inter-die threshold voltage as a function of channel thickness, t_{Si} , and gate length, L . Supply voltage is 1 V. BOX thickness is 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO_2/TiN gate stack). (Source: © 2008 IEEE. Reprinted with permission from Weber *et al.* (2008).



5.16 Series resistance evolution as a function of SOI film thickness (t_{Si}) under the gate for nMOSFETs on FDSOI.

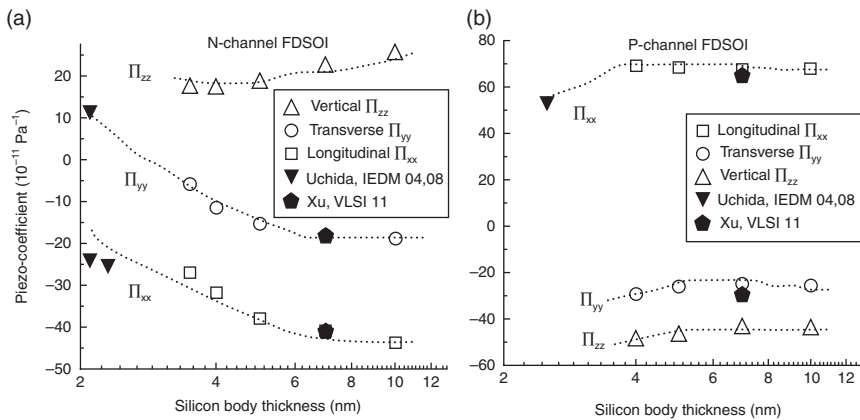
t_{Si} fluctuation (and not that of the gate stack, for example), the solution to improve V_T variability in long and large devices is to reduce the t_{Si} variation at the different scales (roughness and thickness).

An important issue related to ultra-thin (low t_{Si}) FDSOI MOSFETs is the parasitic series resistance R_{SD} . Figure 5.16 shows that series resistance is not

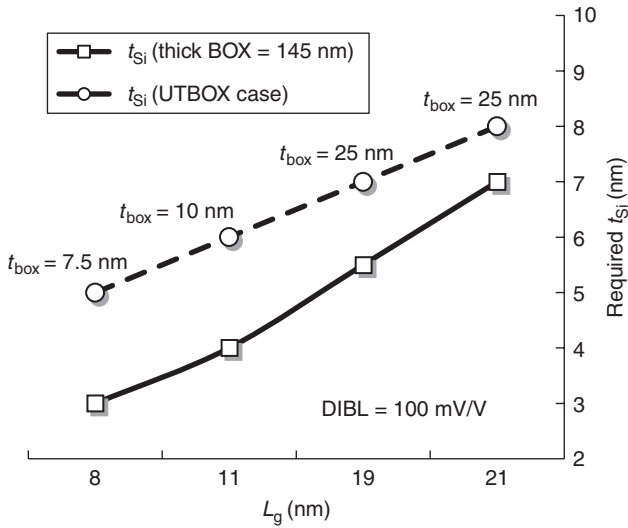
significantly degraded with R_{SD} values as low as $320 \Omega \cdot \mu\text{m}$ for a film thickness of 4 nm (Barral *et al.*, 2007). Similarly, in the literature, a degradation of 40Ω of the parasitic resistance (and no change in performance) is reported when t_{Si} is scaled down from 6 to 3.5 nm (Khakifirooz *et al.*, 2012). Even though it remains a hot topic in terms of process integration, the parasitic series resistance on thin film is thus not a barrier to the development of planar FDSOI technology.

Channel thickness (t_{Si}) scaling can also change the carrier mobility, particularly in the case of highly stressed transistor channels. The electron mobility for unstrained Si increases slightly as t_{Si} is reduced below 4.5 nm, due to quantum confinement-induced subband splitting, which results in carrier reoccupation among the Δ_2 and Δ_4 valleys (Xu *et al.*, 2011). As a consequence, the benefit of the stress for enhancing the electron mobility is diminished in this regime. This explains the reduction of the nMOS piezoelectric coefficient for $t_{Si} < 5$ nm (Fig. 5.17). In contrast, the hole mobility for unstrained Si monotonously decreases as t_{Si} is reduced below 5 nm. Simultaneously, the benefit of stress for enhancing the hole mobility is maintained for $t_{Si} < 5$ nm owing to the large reduction in hole transport mass under shear stress. This is why pMOS piezoelectric coefficients are quite constant, whatever the value of t_{Si} (Fig. 5.17 and Xu *et al.*, 2012).

To summarize, the channel thickness (below the gate stack) value (t_{Si}) in FDSOI logic MOSFETs is chosen in order to reach a given short-channel control (and DIBL). But t_{Si} also alters the V_T variability and affects the



5.17 (a) Simulated nMOS and (b) pMOS piezoelectric coefficients (vertical, longitudinal and transverse to the carrier transport) vs silicon film thickness (t_{Si}). Comparison with experimental results from Xu *et al.* (2011) and Uchida *et al.* (2008). (Source: Xu *et al.*, 2012. Copyright 2012 IEEE.)



5.18 Possible scaling rules of FDSOI devices down to 8 nm gate length (simulations) based on electrostatic considerations (DIBL = 100 mV/V): required t_{Si} vs gate length, L_g .

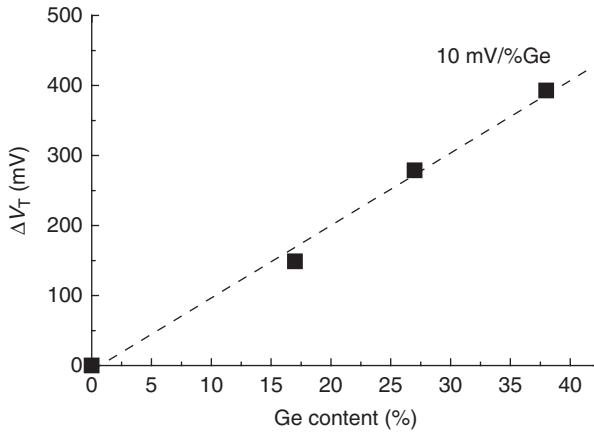
device performance through parasitic series resistance (R_{SD}) and carrier mobility.

5.4.3 Scalability of planar FDSOI transistors

Scalability of the planar FDSOI architecture can be analyzed through experimental data and technology computed-aided-design (TCAD) projection. If DIBL control at 100 mV/V is considered as the electrostatic criterion, Fig. 5.18 shows that the scalability can be demonstrated down to 8 nm gate length, through the reduction of both the SOI and BOX thicknesses. It is reported that the scaling of ultra-thin BOX thickness can help the device downscaling. Without BOX scaling, a 3 nm SOI film is required for the 8 nm gate length, whereas the film can be kept around 5 nm if the BOX is scaled down below 10 nm. Below 8 nm gate length, it is predicted that nanowire-type transistors will be required to ensure good electrostatic control (Faynot *et al.*, 2010).

5.5 Strain options on FDSOI

Planar FDSOI has been considered for long time as an excellent architecture for low-power architecture. Moreover, when mechanical strain is embedded in this technology, it can really address both low-power and high-performance markets.

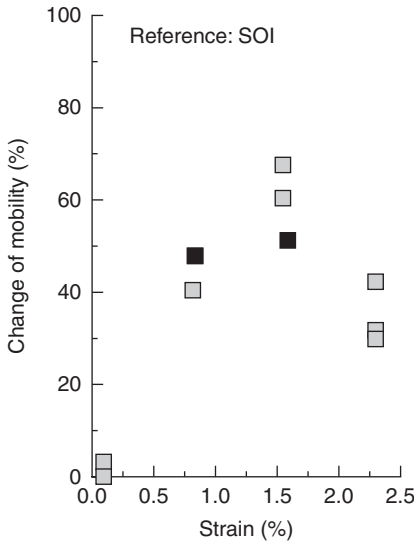


5.19 Change of the threshold voltage induced by a SiGe channel, measured on pMOS as a function of Ge content in the channel on long and large channels. Equivalent oxide thickness is 1.0 nm.

5.5.1 Strained pMOS: SiGe channel and SiGe source/drain

As previously mentioned, it is challenging to obtain p+ effective workfunction using only gate engineering. SiGe channels have been used in the channel of pMOSFETs on bulk Si in order to adjust the threshold voltage in the gate-first approach. This is achieved through strain-induced bands shifting and probably Ge-related dipole variation in the gate stack. The same solution can be effectively applied to planar FDSOI (Fig. 5.19). Experimentally, a lowering of 10 mV flat-band voltage (or V_T) per percentage content of Ge in the SiGe channel is demonstrated. However, up to 15 mV/% had already been reported (see a benchmark in Cassé *et al.*, 2012). The large dispersion of V_T sensibility (ΔV_T) to Ge content in the channel could be attributed to the gate stack difference.

SiGe provides not only this interesting capability to modulate V_T , but also hole mobility enhancement (Fig. 5.20). For SiGe/SOI pFETs, the mobility gain increases with the Ge content and the strain up to 68% for 1.4% strain (corresponding to $\text{Si}_{0.6}\text{Ge}_{0.4}$). Yet for a higher than 60% Ge content, the gain is lowered; this is likely to be attributable to formation of dislocations during the epitaxial growth. This hypothesis is confirmed by the fact that similar results are obtained in the case of $\text{Si}_{0.4}\text{Ge}_{0.6}/\text{sSOI}$ and $\text{Si}_{0.6}\text{Ge}_{0.4}/\text{SOI}$, sSOI being a strained SOI substrate built from relaxed $\text{Si}_{0.8}\text{Ge}_{0.2}$. Actually, the hole mobility is more related to the strain than the amount of Ge in the SiGe channel. This clearly demonstrates that an optimum exists in terms of mobility vs strain or Ge percentage in SiGe channels (Cassé *et al.*, 2012).



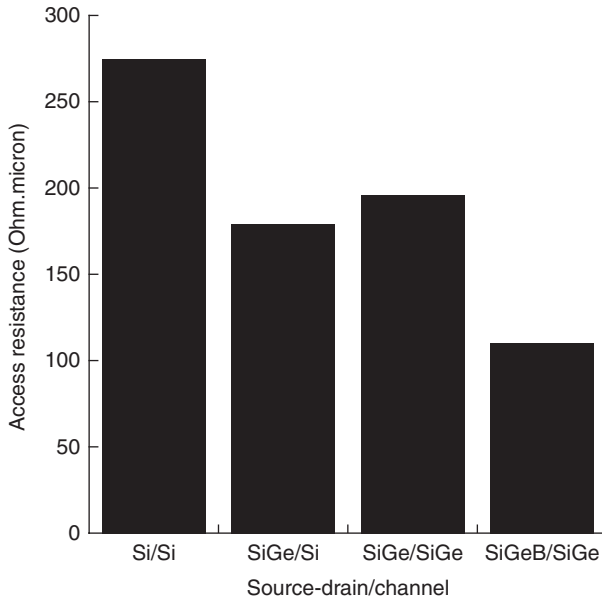
5.20 Hole mobility enhancement measured with a SiGe channel on SOI (grey) or sSOI (black) extracted at the maximum of mobility as a function of strain level in the channel ($\epsilon_{//}$). Equivalent oxide thickness is 1.3 nm.

SiGe could also be advantageous in the source/drain of pMOSFETs. In this instance, *in situ* boron doping could increase the incorporation and activation of dopants in this region. The parasitic access resistance benefits from $\text{Si}_{0.7}\text{Ge}_{0.3}$ and $\text{Si}_{0.7}\text{Ge}_{0.3}\text{:B}$ raised source/drain (with a series resistance reduction of 30% and 60%, respectively) (Fig. 5.21). Furthermore, the hole mobility is improved by the SiGe source/drain (Fig. 5.22). The short-channel hole mobility gains obtained on Si and $\text{Si}_{0.8}\text{Ge}_{0.2}$ channels are in agreement with calculations based on the strain level (~ 500 MPa) generated by $\text{Si}_{0.7}\text{Ge}_{0.3}$ raised source/drain (Le Royer *et al.*, 2011).

SiGe channels and source/drain are thus excellent solutions for high-performance pMOSFETs in FDSOI.

5.5.2 CMOS on sSOI substrates

The main mobility booster solution for an nMOSFET is the use of strained SOI substrate (sSOI). It consists of silicon under biaxial strain, directly on top of the BOX. Such a substrate can be formed from a SiGe pseudo-substrate and by a smart-cut process (Ghyselen *et al.*, 2004). Strained SOI channel changes the V_T for nMOSFETs, in the same way as SiGe does for pMOS. Given the V_T formula for SOI (see Equation [5.3] and Poiroux *et al.*, 2005) and the deformation potential theory (Herring *et al.*, 1956), the V_T shift between sSOI and SOI ($\Delta V_T = V_{T(\text{sSOI})} - V_{T(\text{SOI})}$) can be approximated



5.21 Access resistance extracted with the Y function method for four FDSOI pMOSFET configurations: Si raised source/drain on Si channel (Si/Si), Si_{0.7}Ge_{0.3} raised source/drain on Si channel (SiGe/Si) or on compressive Si_{0.8}Ge_{0.2} channel (SiGe/SiGe) and *in situ* boron-doped Si_{0.7}Ge_{0.3} raised source/drain on compressive Si_{0.8}Ge_{0.2} channel (SiGeB/SiGe). Equivalent oxide thickness is 1.3 nm.

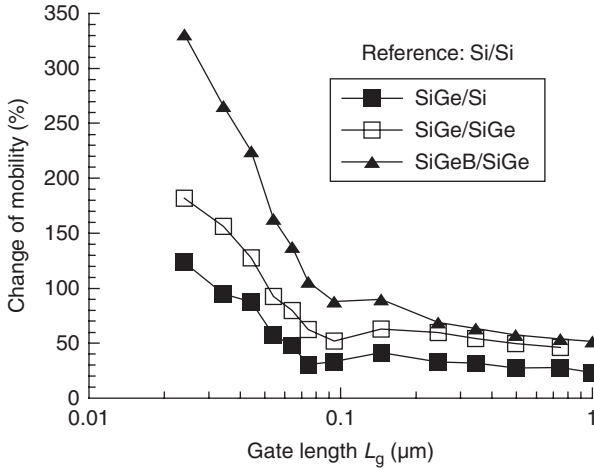
by Equation [5.4], where C_{11} and C_{12} are the elastic stiffness of silicon; $\Xi_d = -5.20$ eV and $\Xi_u = 8.50$ eV represent the deformation potentials (Baslev, 1966; Kanda, 1991); and ϵ_{xx} and ϵ_{yy} are the mean in-plane strain components in the lattice axis system, with ϵ_{zz} representing the out-of-plane strain component; the other parameters have their usual meaning.

$$V_T = \varphi_m - \chi_{Si} + \frac{kT}{q} \ln \left[\frac{C_{ox} (kT/q)}{q T_{Si} \sqrt{N_C N_V}} \right] \quad [5.3]$$

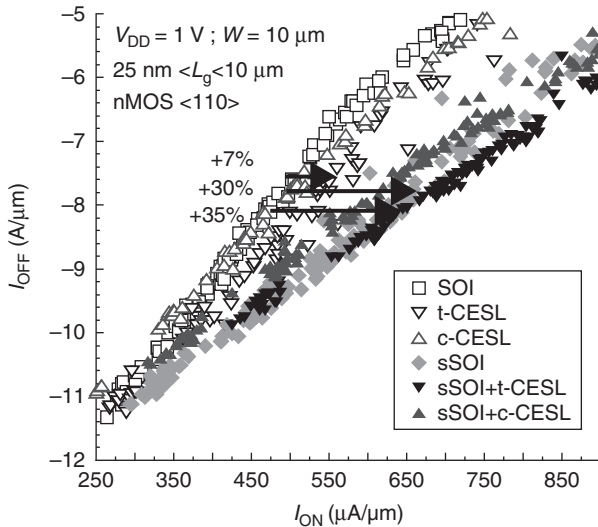
$$\Delta V_T \approx \Delta E_C \approx \Xi_d (\epsilon_{xx} + \epsilon_{yy} + \epsilon_{zz}) + \Xi_u \epsilon_{zz}$$

$$\Delta V_T \approx \left[\Xi_d - (\Xi_d + \Xi_u) \frac{C_{12}}{C_{11}} \right] (\epsilon_{xx} + \epsilon_{yy}) \quad [5.4]$$

The threshold voltage V_T is strongly lowered by strain, by 0.15 V for so-called sSOI (around 0.8% initial strain) and by 0.22 V for so-called eXtremely



5.22 Change of the hole mobility values (extracted at low field by the Y function method) vs gate length for the SOI and compressive $\text{Si}_{0.8}\text{Ge}_{0.2}$ /SOI FDSOI pMOSFETs with the following configurations: $\text{Si}_{0.7}\text{Ge}_{0.3}$ raised source/drain on Si channel (SiGe/Si) or on compressive $\text{Si}_{0.8}\text{Ge}_{0.2}$ channel (SiGe/SiGe) and *in situ* boron-doped $\text{Si}_{0.7}\text{Ge}_{0.3}$ raised source/drain on compressive $\text{Si}_{0.8}\text{Ge}_{0.2}$ channel (SiGeB/SiGe). The reference is Si raised source/drain on Si channel. $W = 10 \mu\text{m}$ active width. Equivalent oxide thickness is 1.3 nm.

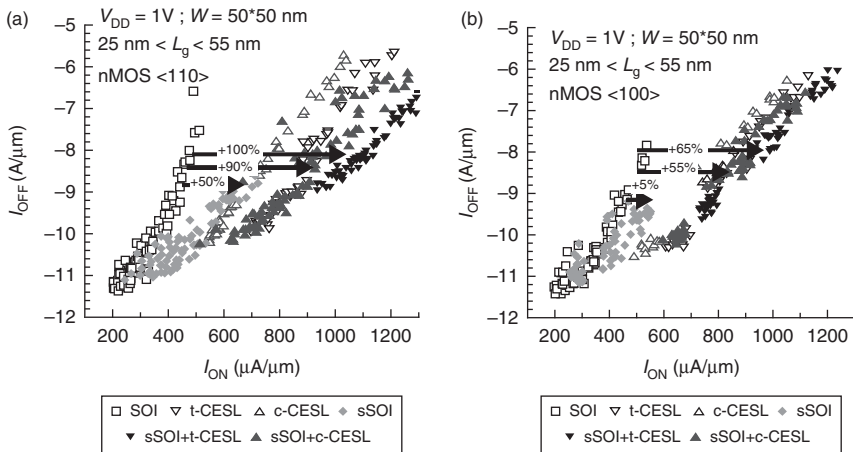


5.23 $I_{\text{ON}}-I_{\text{OFF}}$ for nMOS on SOI or strained SOI with compressive or tensile contact etch stop layers (c- or t-CESL, respectively). Supply voltage is 1 V. BOX thickness is 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO_2/TiN gate stack). (Source: Andrieu *et al.*, 2007. Copyright 2006, The Japan Society of Applied Physics.)

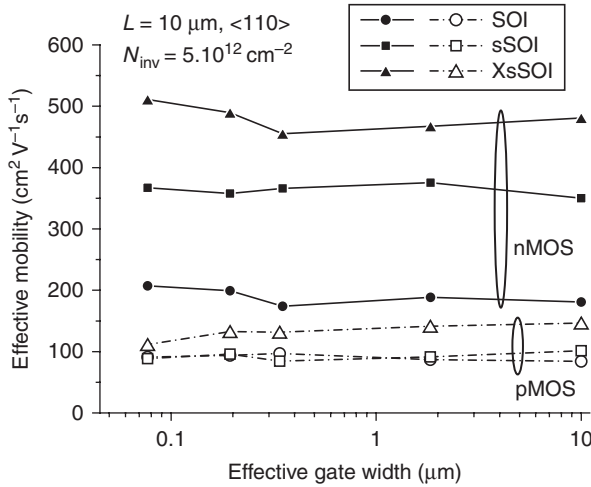
Strained Silicon-on-Insulator (XsSOI) (around 1.2% initial strain) with respect to unstrained SOI. This is generally attributed to lifting of the conduction band degeneracy and lowering of unprimed Δ_2 valleys.

As regards carrier transport and device performance, sSOI yields a 30% improvement of the I_{ON} at a given I_{OFF} for nMOSFETs at $I_{OFF} = 10 \text{ nA}/\mu\text{m}$ for a (100) substrate and $\langle 110 \rangle$ channel direction (Fig. 5.23 and Andrieu *et al.*, 2007). This can be attributed to an 80% enhancement of electron mobility measured at low- V_D in short channels.

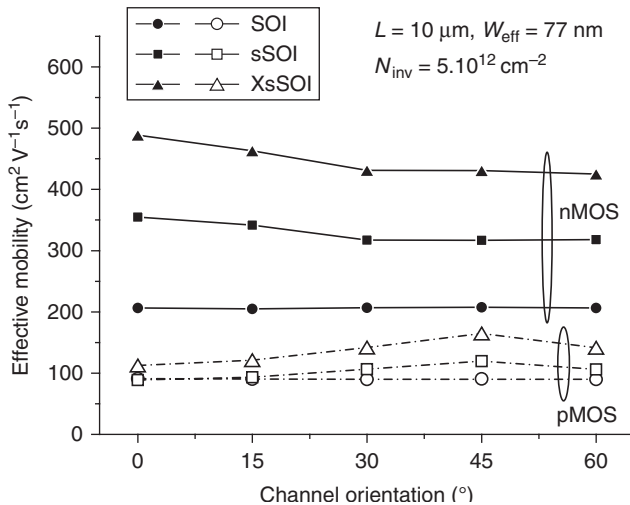
Narrow devices show greater I_{ON} improvement *vs* unstrained SOI than wide devices (+50% improvement measured at $W = 80 \text{ nm}$ channel width as opposed to +30% at $W = 10 \mu\text{m}$) and the $\langle 110 \rangle$ channel direction improvement greatly exceeds that of the $\langle 100 \rangle$ (+50% improvement measured along the $\langle 110 \rangle$ channel as opposed to +5% along the $\langle 100 \rangle$ channel, see Fig. 5.24). This excellent, anisotropic performance obtained on a narrow sSOI channel had already been well demonstrated in planar FDSOI (see Andrieu *et al.*, 2007; Fenouillet *et al.*, 2012) and even in FinFETs (Xiong *et al.*, 2006). This behaviour in respect of channel width can be captured well (even if to a lower extent) by the mobility in long, narrow nMOSFETs (Figs 5.25 and 5.26). For $\langle 110 \rangle$ -oriented channels, mobility enhancements of 135% and 72% are obtained, respectively, for 1.2% initial strain (so-called XsSOI substrates) and 0.8% initial strain (so-called sSOI substrates) compared to SOI; whereas they reach only 106% and 53%, respectively, for the $\langle 100 \rangle$ orientation (Baudot *et al.*, 2010).



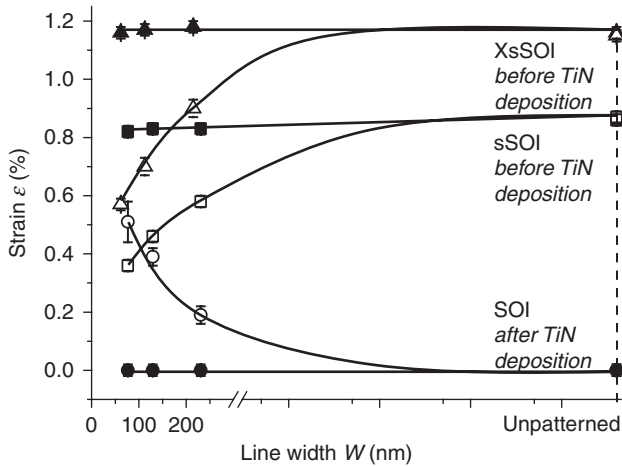
5.24 I_{ON} - I_{OFF} for short and narrow nMOSFETs (50 multi-fingers of 50 nm width each) along $\langle 110 \rangle$ (a) or $\langle 100 \rangle$ (b). Supply voltage is 1 V. BOX thickness is 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO_2/TiN gate stack). (Source: Andrieu *et al.*, 2007. Copyright 2006, The Japan Society of Applied Physics.)



5.25 Effective mobility as a function of the effective gate width for long nMOS and pMOS on SOI and strained SOI of 0.8% (sSOI) or 1.2% (XsSOI) strain. The gate length, L , is $10 \mu\text{m}$ and the channel orientation is $\langle 110 \rangle$. The effective mobility is extracted at the $N_{\text{inv}} = 5 \times 10^{12} \text{ cm}^{-2}$ fixed inversion charge density. (Source: Baudot *et al.*, 2010. Copyright 2010, with permission from Elsevier.)

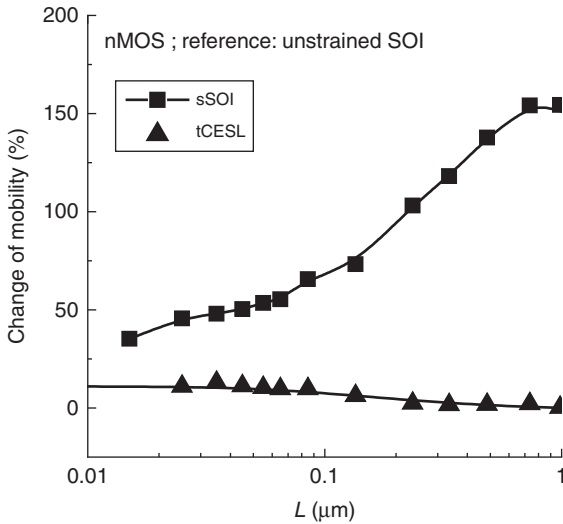


5.26 Effective mobility as a function of the channel orientation for long and narrow nMOS and pMOS on SOI and strained SOI of 0.8% (sSOI) or 1.2% (XsSOI) strain. The gate length, L , is $10 \mu\text{m}$ and the effective gate width, W_{eff} , is 77 nm . The effective mobility is extracted at the $N_{\text{inv}} = 5 \times 10^{12} \text{ cm}^{-2}$ fixed inversion charge density. 0° (45°) corresponds to the $\langle 110 \rangle$ ($\langle 100 \rangle$, respectively) orientation in the (100) plane. (Source: Baudot *et al.*, 2010. Copyright 2010, with permission from Elsevier.)



5.27 In-plane strain measured by grazing incident X-ray diffraction (GIXRD) as a function of the line width, W , along the lines (full symbols) and perpendicular to the lines (open symbols) for 0.8% (sSOI) and 1.2% (XsSOI) strained SOI lines without TiN gate and for SOI lines with TiN gate around the mesa isolation. For narrow lines, the TiN gate induces tensile strain in the SOI layer along the line width. This tensile strain increases when the line width decreases, from 0.19% for $W = 230$ nm narrow devices up to 0.51% for $W = 77$ nm narrow devices. (Source: Baudot *et al.*, 2010. Copyright 2010, with permission from Elsevier.)

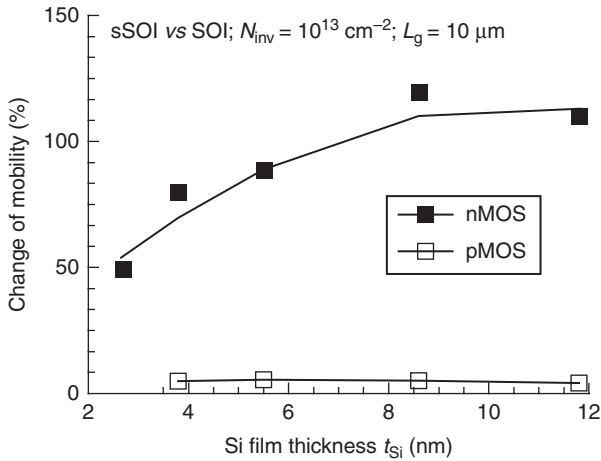
On such a design, grazing incidence X-ray diffraction (GIXRD) characterizations reveal that the strain in sSOI is no longer biaxial, but rather uniaxial in the gate length direction (Fig. 5.27). During the process integration, the strain indeed relaxes from the edges of the active area (due to patterning and thermal budget) and can be also altered by the gate stack (as illustrated by the impact of the TiN metal gate in Fig. 5.27). The strain relaxation in the device width direction transforms the strain into a longitudinal, uniaxial strain in the $\langle 110 \rangle$ direction, which is the best configuration for highly stressed nMOS (Uchida *et al.*, 2005). However, some studies have also shown that narrow devices can suffer from other integration issues, such as detrimental (compressive) stress from the STI (Morvan *et al.*, 2012) or a strong over-etching of the isolation (or divot of the STI) (Andrieu *et al.*, 2006). To conclude on these experiments, the best configuration of strain for nMOS (as for pMOS) is uniaxial strain in the gate length direction (tensile for nMOS but compressive for pMOS), and in the $\langle 110 \rangle$ channel direction. This strain must be as high as possible; consequently the relaxation of the longitudinal strain must be minimized (with special attention paid to isolation and gate/spacer patterning).



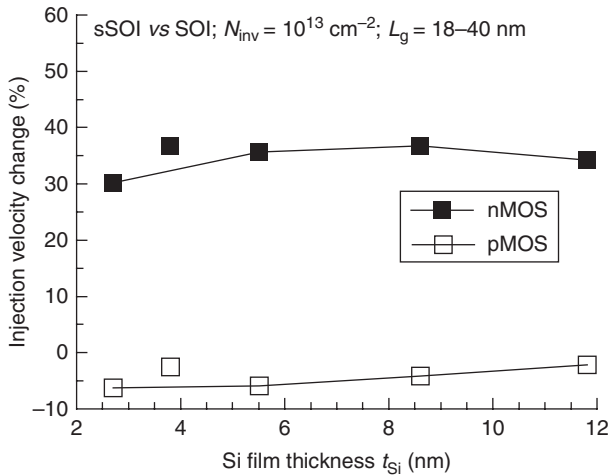
5.28 Experimental change of mobility (extracted at low field) induced by sSOI wafers and a tensile contact etch stop layer (CESL) on SOI vs gate length for large devices along $\langle 110 \rangle$ (0°). The reference is unstrained SOI.

Another classical stressor is the contact etch stop layer (CESL), which could be either compressive or tensile, to boost either pMOS or nMOS, respectively. For nMOS, for example, the CESL makes it possible to boost the mobility of short-channel electrons by about 15% (Fig. 5.28). Moreover, the performance improvement provided by CESL and sSOI can be cumulative, at least for low stress levels (Figs 5.23 and 5.24). However, for very higher stress levels, the performance improvement saturates at about 150% for mobility – and 100% for I_{ON} (Andrieu *et al.*, 2007).

The impact of the scaling of film thickness for sSOI has been also studied. While the hole mobility is not changed by sSOI in the strong inversion regime, nFETs on sSOI reveal larger electron mobility than SOI, with a mobility gain ranging from 110% for the thickest films (11 nm) to 50% for the thinnest (< 3 nm) (Fig. 5.29). The sSOI induced mobility gain decreases for thin bodies. In order to check whether this conclusion regarding electron transport can be extended to short-channel devices, ballisticity rates and injection velocities have been extracted in short-channel SOI and sSOI devices in the saturation regime, using an experimental methodology that takes into account carrier degeneracy and multi-subband population (Barral *et al.*, 2007). Ballisticity is improved with gate length reduction even for the thinnest films. Ballisticity rate is impacted by the t_{Si} reduction for both SOI and sSOI n- and pMOSFETs, without significant difference between SOI and sSOI values. Ultimately,

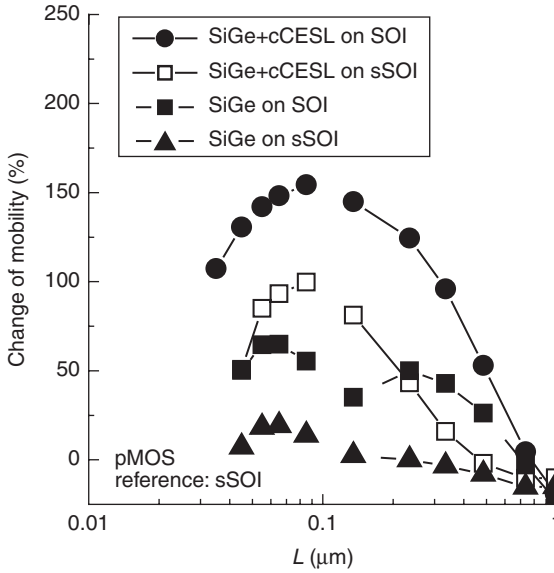


5.29 Experimental change of the long-channel electron and hole effective mobilities (sSOI vs SOI) in high inversion regime ($N_{inv} = 10^{13} \text{ cm}^{-2}$ inversion charge density) vs channel thickness (t_{Si}) for $10 \mu\text{m}$ long n and pMOS on SOI or sSOI. BOX thickness is 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO_2/TiN gate stack).



5.30 Experimental change of the electron and hole injection velocities (sSOI vs SOI) in short-channel devices ($L = 18\text{--}40 \text{ nm}$) as a function of the Si film for n and pMOS on SOI or sSOI. BOX thickness is 145 nm; equivalent oxide thickness is around 1.6 nm (with HfO_2/TiN gate stack).

however, even for ultra-thin films (2.5 nm), strain still induces a significant injection velocity enhancement (+35%) (Fig. 5.30). This means that the scalability of sSOI for planar FDSOI can be ensured, as in the case of

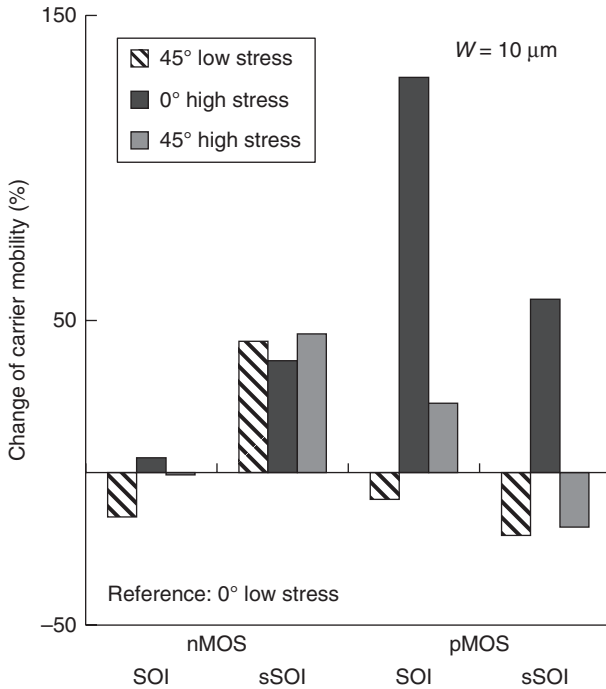


5.31 Change of the hole mobility (extracted at low field) vs gate length, L , for pMOSFETs on SOI or sSOI with $\text{Si}_{0.7}\text{Ge}_{0.3}$ source/drain (or not) and with compressive contact etch stop layer (cCESL) (or not) at $W = 10 \mu\text{m}$ active width. The reference is a sSOI pMOS. SOI thickness, t_{Si} , is around 7 nm and equivalent oxide thickness is 1.3 nm.

SOI, by film thickness reduction, while retaining the advantages of sSOI in terms of performance.

For pMOS, Fig. 5.29 shows that the hole mobility is not significantly changed by sSOI. In the worst case, a few percent performance reduction in short channels was reported on pMOS on sSOI compared to SOI. In order to improve the pMOS performance in sSOI, the SiGe channel can be locally integrated (Andrieu *et al.*, 2005). The SiGe channel in sSOI is less effective than in SOI in terms of V_T and mobility (Fig. 5.20) because of a lower strain than in SOI for a given amount of Ge. Actually, a shift of 20% Ge can be applied in sSOI compared to SOI: $\text{Si}_{1-x-0.2}\text{Ge}_{x+0.2}$ on sSOI is more or less as effective as $\text{Si}_{1-x}\text{Ge}_x$ on SOI in terms of both hole mobility enhancement and pMOS V_T lowering vs the Si channel. This is linked to the initial lattice parameter of sSOI, close to the one of relaxed $\text{Si}_{0.8}\text{Ge}_{0.2}$. This is certainly the major drawback of sSOI: it requires a high amount of Ge in the pMOS channel, which is challenging to integrate. Similarly, sSOI pMOSFETs require a high amount of Ge in the source/drain because SiGe sources/drains are less effective on sSOI than on SOI (see Fig. 5.31) (Baudot *et al.*, 2010; Morvan *et al.*, 2012).

In any case, local stressors are needed to obtain the maximum performance: SiGe channel and source/drain for pMOS. Also, the $\langle 110 \rangle$ channel



5.32 Change of the mobility (extracted at low field) in nMOS or pMOS in short channels for different substrates (SOI or sSOI) at $W = 10 \mu\text{m}$. High stress refers to the use of tensile contact etch stop layer (t-CESL) for nMOS and compressive contact etch stop layer (cCESL) plus SiGe source/drain for pMOS. 0° is the $\langle 110 \rangle$ and 45° the $\langle 100 \rangle$ orientation. SOI thickness, t_{Si} , is around 7 nm and equivalent oxide thickness of 1.3 nm.

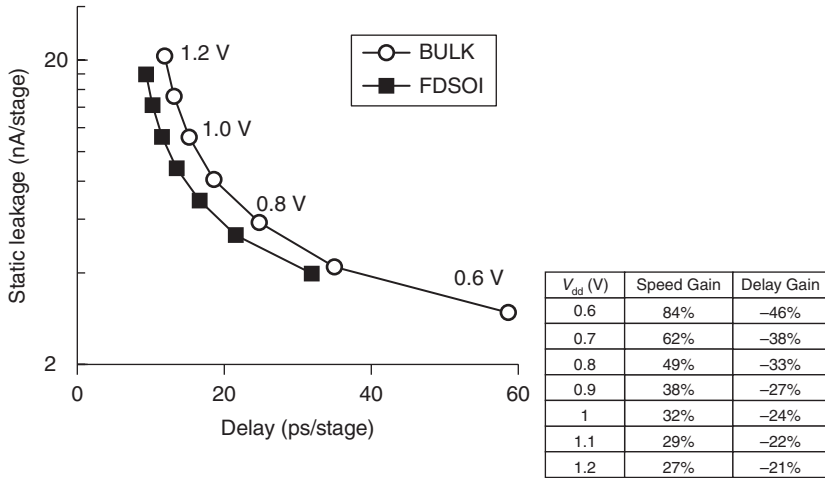
orientation is best (on (100) substrates) for CMOSFETs with high stress, as summarized in Fig. 5.32.

5.6 Performance without and with back bias

When FDSOI technology is carefully optimized in terms of threshold voltages, channel and BOX thicknesses, as well as mechanical stressors in FDSOI, this technology is of high performance, as detailed in this section.

5.6.1 Performance without back bias

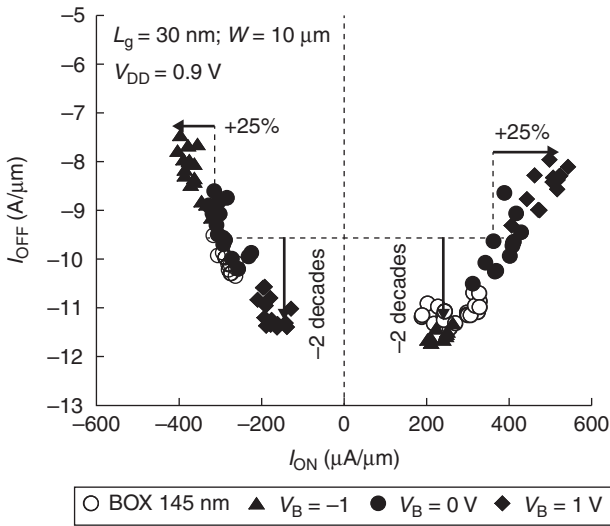
First, silicon data have already highlighted the excellent $I_{\text{ON}}-I_{\text{OFF}}$ characteristics in FDSOI (Cheng *et al.*, 2012). Moreover, good DIBL values have been obtained compared to regular planar bulk devices. Only FinFETs



5.33 Static leakage vs delay of high performance ring oscillators (left) on 28 nm FDSOI or bulk and speed gain or delay gain vs bulk for different supply voltages (from 0.6 to 1.2 V).

with aggressive Fin dimensions (typically 13 nm wide FinFETs for $L = 25$ nm) or nanowires can reach lower DIBL values (see a benchmark in Faynot *et al.*, 2010). The improved DIBL of planar FDSOI compared to planar bulk devices is correlated with a subthreshold swing below 80 mV/decade.

In comparing FDSOI with planar bulk devices at a given OFF state current (I_{OFF}), the better DIBL and subthreshold swing in FDSOI are directly responsible for a boost of the effective current (I_{EFF}) and dynamic performance. It is important to point out that electrostatics is even more efficient than mobility in boosting the I_{EFF} (Faynot *et al.*, 2010). A second advantage of FDSOI is the reduction of different capacitances, including the junction capacitance, compared to planar bulk devices. Both effects lead to a 22% improvement in the delay time of a ring oscillator at a given dynamic energy (i.e., delay time and dynamic power product) at the 45 nm node (Fenouillet *et al.*, 2009). Another experimental demonstration of the interesting features of FDSOI was conducted by Cheng *et al.* (2011). They showed a 25% improvement of the delay from a 28 nm planar bulk to a 22 nm FDSOI technology at a given static power and 1 V supply voltage (or a 20% V_{DD} reduction at a given speed). The comparison between 28 nm bulk and FDSOI presented in Fig. 5.33 gets similar results (27% delay gain at 0.9 V). In comparison with devices in planar bulk, planar FDSOI



5.34 I_{ON}/I_{OFF} characteristics of n&pMOSFETs at 30 nm gate length and 0.9V supply voltage for different back biases. Comparison with 145 nm thick BOX devices. SOI thickness, t_{Si} is 7 nm; BOX thickness is 10 nm; equivalent oxide thickness is 1.3 nm. No ground plane doping. (Source: Andrieu *et al.*, 2010. © 2010 IEEE.)

can appear even more advantageous when the gate length is reduced at a given node because planar FDSOI offers excellent (gate length) scalability, owing to its electrostatics.

The major advantage of FDSOI is indeed its electrostatics; the dynamic performance is impressive at low supply voltage. In other words, the gain over planar bulk devices in terms of delay *vs* power trade-off is greater at low V_{DD} , as shown by Fig. 5.33 and reported by Planes *et al.* (2012). This property is linked to the fully depleted behaviour (and also shown in FinFETs by Auth *et al.*, 2012), which improves the electrostatics and especially the subthreshold slope, making fully depleted devices the optimum solution for low- V_{DD} operation. This proves that the technology is very well suited to a large range of applications, from ultra-low voltage to high performance.

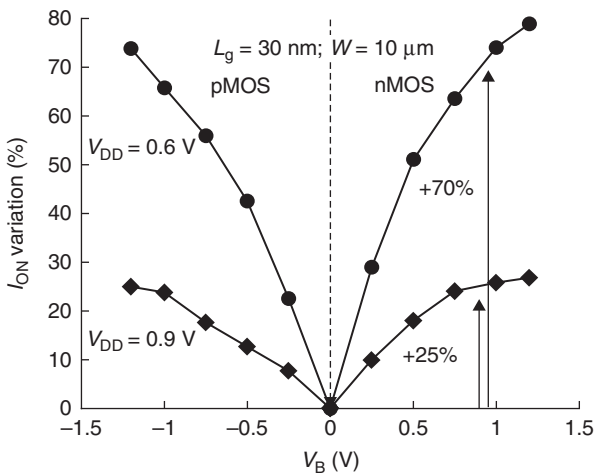
Another possible boost can be obtained by appropriate circuit design. Planar FDSOI exhibits excellent variability (mainly due to the suppression of the random dopant fluctuation). This makes it possible to reduce the minimum operating voltage of the memory (by about 100 mV) (see Planes *et al.*, 2012; Ranica *et al.*, 2013) and might reduce the corners of the

device characteristics, thereby improving the circuit performance when the designers consider worst-case scenarios.

5.6.2 Performance with back bias

One of the most interesting features of UTBB is its efficient back bias (V_B) capability. The coupling between the back bias and the channel through a 25 nm (and 10 nm, respectively) thin BOX is quite similar to (or larger than, respectively) that in planar bulk for the 32 nm node. Even FinFETs yield lower back bias efficiency because of the complete gate control over the channel. The γ -factor in planar FDSOI is between 70 and 170 mV/V, depending on the back plane doping and bias (Figs 5.10 and 5.11).

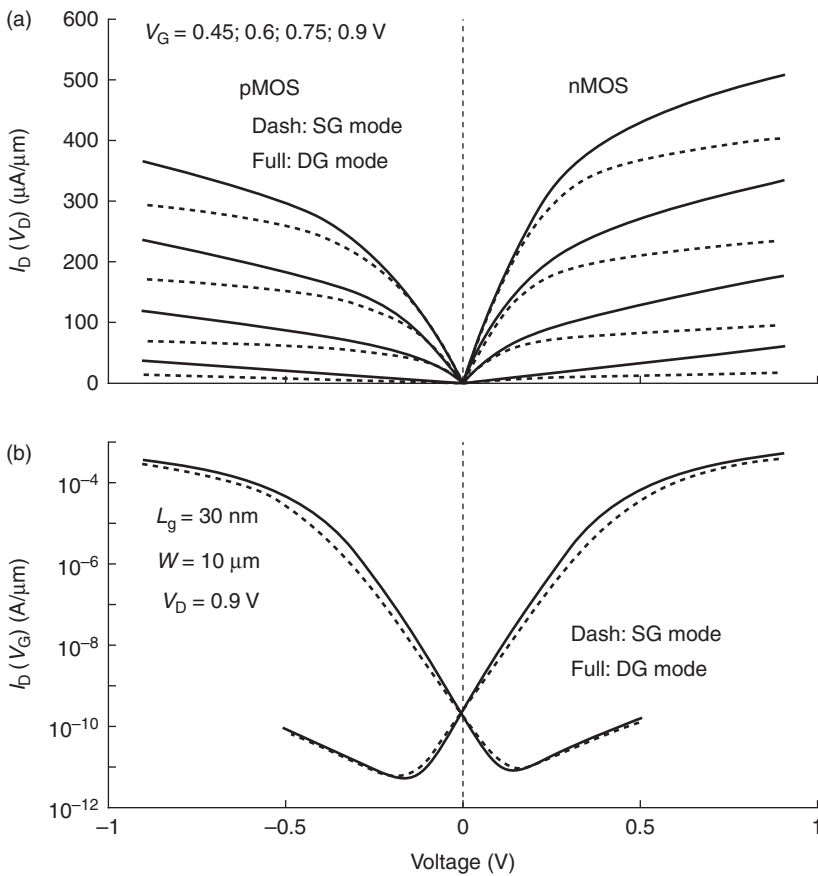
In the worst case (without back plane) and with 10 nm buried oxide thickness, forward and reverse body bias (FBB and RBB) techniques induce half a decade I_{OFF} reduction and a 10–15% I_{ON} increase at $|V_B| = 0.3$ V for $V_{\text{DD}} = 0.9$ V (Andrieu *et al.*, 2010). It should be noted that this back bias value of 0.3 V is typically used for bulk circuits. However, unlike in bulk, the presence of the BOX in FDSOI prevents junction leakages (except the possible junction leakage between back planes). Consequently, a back bias over 0.3 V is possible in FDSOI, and would lead to a wider $I_{\text{ON}}-I_{\text{OFF}}$ tuning capability and a wider speed/power window at the circuit level. For example, the use of 1 V back bias on FDSOI enables a frequency boost



5.35 I_{ON} variations by forward body bias for 30 nm n&pMOS at various supply voltages, V_{DD} . SOI thickness, t_{Si} , is 7 nm; BOX thickness is 10 nm; equivalent oxide thickness is 1.3 nm. No ground plane doping. (Source: Andrieu *et al.*, 2010. © 2010 IEEE. Reprinted with permission from Andrieu *et al.*, 2010.)

of 35% vs bulk with 0.3 V back bias at a given total power (see Flatresse *et al.*, 2013). Moreover, it is worth noting that the forward back bias effect is even higher at low- V_{DD} values (Andrieu *et al.*, 2010). This technique is thus highly effective in FDSOI to dynamically boost the FDSOI technology in the critical paths of a circuit.

This body bias is often used by designers for power management and circuit compensation in so-called reverse source biasing (RSB) or RBB. The OFF state leakage in the RBB regime can be limited by gate-induced drain leakage (GIDL < 2 pA/ μm). In the RSB regime (because of the drain voltage (V_{DS}) reduction), the off-leakage is governed by the gate



5.36 Drive current (vs drain voltage (above) or vs gate voltage (below)) in double gate (DG) mode (where $V_G = V_B$) or single gate (SG) ($V_B = 0$ V). SOI thickness is 7 nm; BOX thickness is 10 nm; equivalent oxide thickness is 1.3 nm. No ground plane doping. (Source: Andrieu *et al.*, 2010. © 2010 IEEE.)

current ($<0.5 \text{ pA}/\mu\text{m}$ at $T_{\text{inv}} = 1.3 \text{ nm}$ and $L = 30 \text{ nm}$ gate length). These characteristics for both n- and pMOS highlight some great advantages of the FDSOI technology, compared with planar bulk: very low GIDL capability and reduced junction leakage.

In terms of speed, applying $V_B = 0.9 \text{ V}$ induces a +25% I_{ON} at $V_{\text{DD}} = 0.9 \text{ V}$ (Figs 5.35 and 5.36). This V_B -sensitivity by FBB is even more efficient at $V_{\text{DD}} = 0.6 \text{ V}$ (80% boost) because of the lower gate voltage overdrive at low supply voltage. Another application of the FBB is the use of a specific design where the gate and the substrate are connected together. In this so-called dissymmetrical ‘double gate mode’ ($V_B = V_G$), a 25% I_{ON} enhancement is demonstrated at $V_{\text{DD}} = 0.9 \text{ V}$ for both n- and pMOS compared to the single top-gated mode. This gain is the same as for the aforementioned FBB, but with no I_{OFF} increase (Fig. 5.36, Andrieu *et al.*, 2010; Kilchytska *et al.*, 2013).

5.7 Conclusion

Planar FDSOI CMOS devices are fabricated on SOI wafers, either with a thick BOX (typically 145 nm) or, advantageously, a thin BOX (below 25 nm, so-called ultra-thin body and buried oxide (UTBB or UTB²) wafers). In terms of process integration, this technology can be built from a bulk CMOS technology with some extra developments/optimizations, the principal ones being:

- the NO-SOI (or ‘NOSO’) brick (in order to create a tap in the substrate);
- the ground plane implantation; and
- channel and source/drain thickness management.

In terms of device, planar FDSOI FETs represent a breakthrough compared with bulk ones. The paradigm is changed because the channel benefits from being undoped. The first consequence is that the (long-channel) threshold voltage must be tuned by the ground plane and the gate stack (no longer by the channel doping). The second consequence is great improvements in performance (25–35% at the supply voltage and even better at low supply voltage) and in variability ($\sim 100 \text{ mV } V_{\text{DDmin}}$ in SRAMs).

Fully depleted devices represent the new wave in CMOS booster development (after strain and high-k/metal gate), and can be combined with the two previous waves. They are electrostatic boosters and enable the scaling of this technology to be pursued. Starting from planar bulk technology, the electrostatics are improved as a result of planar FDSOI and even further improvements are possible with trigate/FinFET.

A fair and complete comparison between these two technologies has not been presented, because this is difficult to address. FinFET yields high-drive current but high capacitance (because of 3D devices), whereas FDSOI brings flexibility for designers (owing to the back bias efficiency and the ‘planar’ design rules), low capacitance and low variability. Only a circuit (and not only a device) comparison would be relevant (see a first trial in Flatresse *et al.* (2013)).

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Silicon-on-insulator (SOI) junctionless transistors

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Abstract: Unipolar junctionless transistors are thin-film, heavily doped (typically in the 10^{19} cm^{-3} range) semiconductor resistors with a gate electrode that controls the flow of current between source and drain. Device design is extremely simple as there are no PN junctions. Device operation relies on fully depleting the semiconductor using the workfunction of the gate material to turn the device off. When the device is turned on, current flows through the bulk of the thin film, and can be augmented by an accumulation current contribution. Junctionless transistors are characterized by reduced short-channel effects and present excellent subthreshold slope and low DIBL.

Key words: nanowire field-effect transistor (FET), multigate FET, FinFET, trigate FET, gate-all-around device, metal-oxide semiconductor FET (MOSFET), silicon-on-insulator.

6.1 Introduction

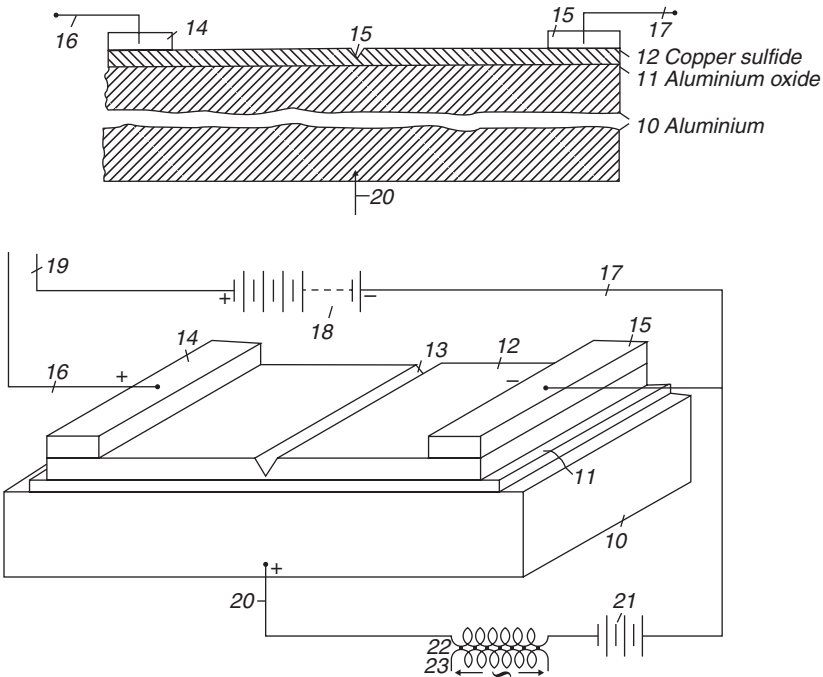
A transistor without junctions may seem to be a heresy. Yet, the very first transistor device ever conceived was junctionless: the first patent for the transistor principle was filed in Canada by Austro-Hungarian physicist Julius Edgar Lilienfeld on 22 October 1925 (Lilienfeld, 1925). The Lilienfeld transistor was a field-effect device, much like modern metal-oxide semiconductor (MOS) devices. Figure 6.1 shows a copy of Lilienfeld's US Patent 1 900 018 'Device for controlling Electric Current' (Lilienfeld, 1928). It consists of a thin semiconductor film '12' deposited on a thin insulator layer '11', itself deposited on a metal electrode '10' which acts as the gate of the device. The current flows in the resistor between contact electrodes '14' and '15', in much the same way as drain current flows between source and drain in a modern metal oxide semiconductor field-effect transistor (MOSFET). The initial semiconductor material proposed in Lilienfeld's patent was copper sulfide and the gate insulator was alumina. The device is a simple resistor, and the application of a gate voltage allows one to deplete the semiconductor film

7 March 1933

1 900 018

J.E. LILIENFELD
 DEVICE FOR CONTROLLING ELECTRIC CURRENT
 Filed 28 March 1928

3 Sheets-sheet 1



6.1 Copy of Figures 1 and 3 from Lilienfeld's US Patent 1 900 018 'Device for controlling Electric Current'. The device contains a metal gate electrode '10', a gate insulator layer '11', a semiconductor resistive film '12' with two contacts '14' and '15', and a notch in the semiconductor film to locally reduce the semiconductor layer thickness '13'. Contacts '15' and '16' are the equivalent of the source and drain contacts in a modern MOSFET.

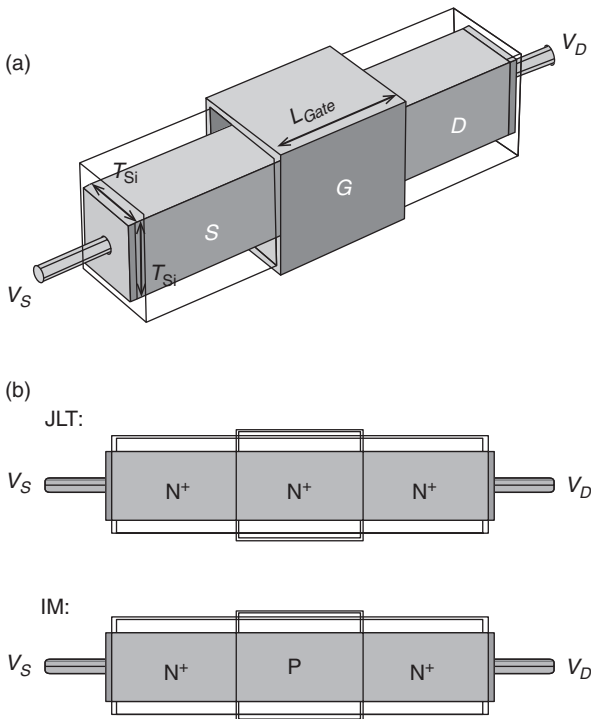
of carriers, thereby modulating its conductivity. Ideally, one should be able to completely deplete the semiconductor film of carriers, in which case the resistance of the device becomes quasi-infinite and the device can be turned off. This is why Lilienfeld introduced a notch '13' in the semiconductor film. This allows one to induce full depletion of the copper sulfide in the notch area, where the film is very thin, to turn the device off. Having a larger semiconductor thickness everywhere else helps in reducing the overall resistance of the device when it is turned on.

In 2007, an accumulation-mode silicon nanowire MOSFET without junctions was proposed (Shan *et al.*, 2007). The device received a relatively light doping concentration and, as a result, had a low current drive (a few nA for $L = 2 \mu\text{m}$) and poor subthreshold characteristics (130 mV/dec). Numerical

simulations show that this type of device can reach drain current values of only a few $\mu\text{A}/\mu\text{m}$ for $L = 50$ nm, which is far too low for CMOS applications (Iqbal *et al.*, 2008). Improved performance was demonstrated by another junctionless device, the vertical-slit field-effect transistor (VESFET), which has a double gate and allows for the fabrication of compact AND or OR gates (Weis *et al.*, 2008; Weis and Schmitt-Landsiedel, 2010). The physics of cylindrical nanowire semiconductor resistors was first explored theoretically in 2008 in a device called the surrounding gate MOS nanowire operated in junction gate FET (JFET) mode or the pinch-off FET (POFET) (Sorée *et al.*, 2008).

6.2 Device physics

The key for making a junctionless transistor with reasonable current drive is to increase the channel doping concentration above traditional values. Conventional wisdom prohibits the use of doping levels much above 10^{18} cm^{-3} , mostly because bulk electron mobility drops to values below $100 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ when the doping concentration exceeds 10^{19} cm^{-3} (Jacoboni *et al.*, 1977).



6.2 Schematics of nanowire transistors. (a) 3D view of a gate-all-around (GAA) nanowire transistor. (b) Doping polarities in an n-channel junctionless transistor (JLT) FET and an inversion-mode (IM) FET.

Doping concentrations in the range 10^{19} – 10^{20} cm^{-3} are routinely used in source and drain, as well as in source and drain extensions, but not in device channels. Instead of using the traditional N⁺-P-N⁺ sandwich found in inversion-mode (IM) MOSFETs, an n-channel junctionless transistor is composed of a single piece of N⁺ material. A schematic view of IM and junctionless field-effect transistors is presented in Fig. 6.2.

6.2.1 Current drive

The current in a resistor with given length L , width W_{Si} , and thickness T_{Si} , can readily be calculated using Ohm's law. Example numerical values are given in Table 6.1.

$$I_D = RV_D \quad \text{with} \quad R = \frac{L}{qN_D\mu_n T_{\text{Si}} W_{\text{Si}}} \quad [6.1]$$

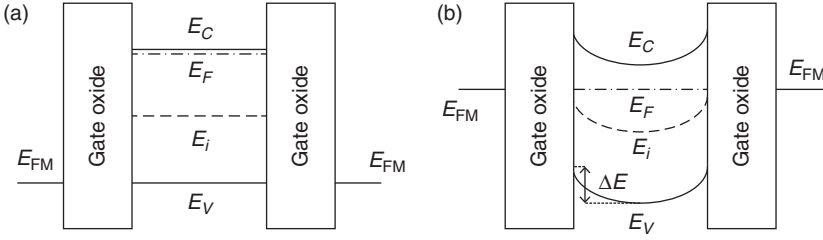
Table 6.1 shows the current in an N-type silicon resistor with a length of 25 nm calculated using Equation [6.1], assuming a mobility of $50 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for the electrons. The voltage applied across the resistor is 1 V. The current in $\mu\text{A}/\mu\text{m}$ is normalized to a device width of $W_{\text{Si}} + 2T_{\text{Si}}$ based on the assumption of a trigate configuration. The current in the resistors, I_R , is only indicative of the current levels that can be reached in junctionless transistors, $I_{D\text{BulkSat}}$: in a first approximation, pinch-off of the bulk channel limits $I_{D\text{BulkSat}}$ to approximately 50% the value of I_R but, on the other hand, the formation of an accumulation channel increases drain current to values significantly higher than those predicted in a simple resistor, which accounts only for bulk current (Berthomé *et al.*, 2011).

The key to fabricating a high performance junctionless transistor (JLT) is the formation of a semiconductor layer that is thin and narrow enough to allow for full depletion of carriers when the device is turned off. The

Table 6.1 Bulk current in pinched-off resistors

Doping concentration (cm^{-3})	$W_{\text{Si}} = T_{\text{Si}}$ (nm)	I_R (μA)	$I_{D\text{BulkSat}}$ (μA)	$I_{D\text{BulkSat}}$ ($\mu\text{A}/\mu\text{m}$)
1×10^{19}	10	32	16	533
2×10^{19}	8	41	20	853
3×10^{19}	7	47	24	1120
4×10^{19}	6	46	23	1280
5×10^{19}	5	40	20	1333

Note: $L = 25$ nm

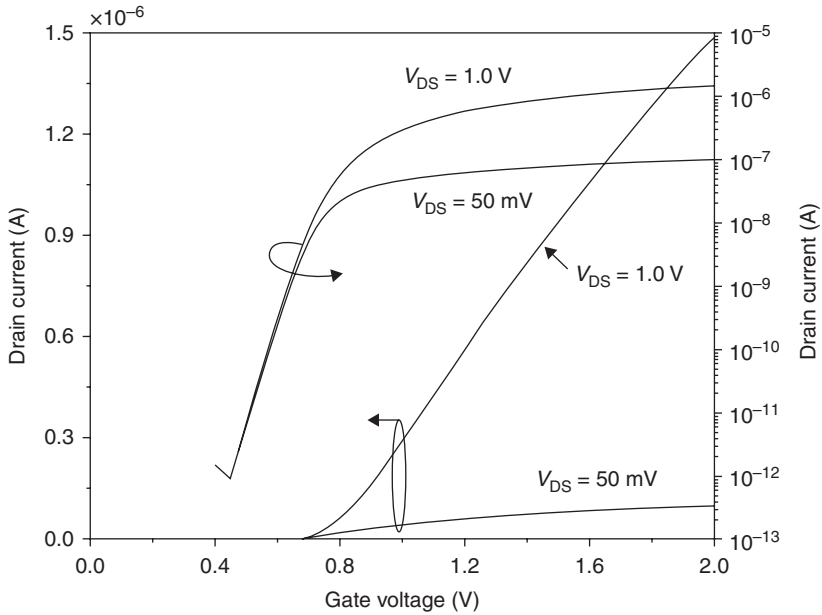


6.3 Energy-band diagram for an n-channel JLT in (a) flat-band condition (the device is turned on) and (b) in the off state (the channel region is fully depleted).

semiconductor also needs to be heavily doped to allow for a decent amount of current flow when the device is turned on. Putting these two constraints together imposes the use of nanoscale dimensions and high doping concentrations. The device is turned off not by a reverse-biased junction, as in the case of a conventional IM MOSFET, but by full depletion of the channel region. This depletion is caused by the workfunction difference between the gate material and the doped silicon in the nanowire. Figure 6.3 shows the energy-band diagram for an n-channel JLT, with a P^+ polysilicon gate electrode. Flat-band condition is achieved when a positive gate bias equal to the workfunction difference between the nanowire and the gate material is applied to the gate (Fig. 6.3a) (Colinge *et al.*, 2011). In that case the device is turned on. A gate voltage larger than V_{FB} will increase current drive by creating surface accumulation channels. When a zero gate bias is applied, the channel region is fully depleted (Fig. 6.3b). The band curvature in the nanowire (ΔE in Fig. 6.3b) can be estimated assuming a gate-all-around (GAA) configuration and a square cross section where the width of the nanowire, W_{Si} , is equal to its thickness, T_{Si} . Using the Poisson equation with the depletion approximation we find:

$$\frac{d^2\Phi}{dx^2} + \frac{d^2\Phi}{dx^2} = 2 \frac{d^2\Phi}{dx^2} = -\frac{qN_D}{\epsilon_{Si}} \Rightarrow \Delta E = \frac{q^2 N_D}{\epsilon_{Si}} \frac{T_{Si}^2}{16} \quad [6.2]$$

The value of ΔE is typically around 100 meV, which means that in full depletion the electron concentration at the Si–SiO₂ interfaces is approximately 50 times lower than in the center of the channel region. Assuming a doping concentration of 10^{19} cm^{-3} in the channel, the drain current can thus be decreased by approximately $10^{19}/50n_i = 7.5$ orders of magnitude before the hole concentration at the Si–SiO₂ interfaces becomes equal to the electron concentration. It is thus safe to assume that the device operates with one



6.4 Measured $I_D(V_G)$ characteristics of an n-channel device with $W_{\text{Si}} = 25 \text{ nm}$ and $L = 1 \text{ }\mu\text{m}$, plotted on either a linear scale (left) or a logarithmic scale (right).

type of carrier only (electrons). It is, however, possible to form inversion layers, particularly in the device corners, by applying very large negative gate voltages (Duarte *et al.*, 2012).

The electrical characteristics of the JLT are remarkably identical to those of regular trigate MOSFETs. Figure 6.4 shows the $I_D(V_G)$ characteristics of an n-channel JLT. The device has an effective width of 25 nm and a gate length, L , of 1 μm . Extrapolating using $V_{\text{DS}} = 1 \text{ V}$, the threshold voltage ($V_{\text{TH}} = 0.3 \text{ V}$, $L = 20 \text{ nm}$, $W_{\text{Si}} = 25 \text{ nm}$, and $T_{\text{Si}} = 10 \text{ nm}$, one finds that the device is capable of I_{OFF} and I_{ON} values of 0.1 nA/ μm and 1000 $\mu\text{A}/\mu\text{m}$, respectively, without using any mobility-enhancing technique such as strain.

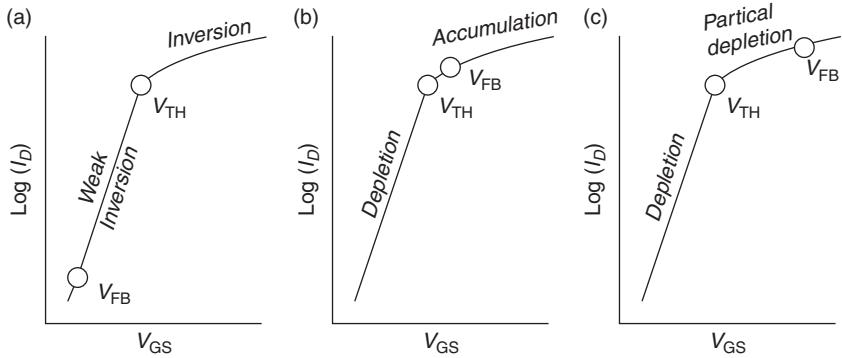
6.2.2 Conduction mechanisms

The physics of the JLT is quite different from that of standard inversion-mode multigate FETs. We will here consider an n-channel device. Depletion of the heavily doped nanowire creates a large electric field perpendicular to current flow below threshold. Under flatband bias conditions ($V_{\text{FB}} \cong 0.5 \text{ V}$ for a midgap metal gate and $V_{\text{FB}} \cong 1 \text{ V}$ for a P⁺ polysilicon gate) the electric field in the channel region is equal to zero, if one neglects quantum-mechanical

confinement effects (Colinge *et al.*, 2010). At higher gate voltages, a surface accumulation layer eventually forms, with an associated electric field. In standard IM devices the electric field in the channel perpendicular to the current flow direction is responsible for a reduction of channel carrier mobility. In the absence of strain-based mobility enhancement, the electron mobility in the channel of an IM MOSFET can fall to values below $20 \text{ cm}^2/\text{Vs}$, assuming an equivalent gate oxide thickness (EOT) of 1 nm and $V_G = 1 \text{ V}$.

In a JLT, the electric field in the channel perpendicular to the current flow is essentially equal to zero in the bulk of the nanowire, which ensures values equal to bulk mobility or higher owing to the screening effect. Furthermore, the device can be used in a weak accumulation regime. It is experimentally observed that the resulting mobility (bulk + accumulation) can exceed textbook bulk mobility due to screening of Coulomb scattering centers by majority carriers (Ohno and Okuto, 1982; Klaassen, 1992; Mundanai *et al.*, 1999). The screening effect has been evidenced in n-channel junctionless SOI MOSFETs with a channel doping concentration of 10^{17} cm^{-3} and an SOI body thickness of 48 nm (Kadotani *et al.*, 2011). The mobility, obtained from conductance and carrier concentration (capacitance) measurements, was found to be larger than the universal mobility in bulk MOSFETs. The mobility improvement is not due to a higher mobility in the accumulation layer but to an increase of the mobility in the SOI body above bulk mobility values, due to the screening effect. Screening effects have been calculated in GAA silicon nanowire transistors using a tight-binding method and the transport properties with a Landauer-Büttiker/Green's functions approach and the linearized Boltzmann transport equation in the first Born approximation for n- and p-type doping concentrations of 10^{18} cm^{-3} . These calculations reveal that electron mobility in accumulation-mode nanowires is much higher than that in inversion-mode devices. In IM nanowires acceptors behave as tunnel barriers for the electrons, while in accumulation-mode devices the carriers see the impurities as quantum wells, which results in Fano resonances (a resonant scattering phenomenon) in the transmission. As a consequence, electron mobility is much larger in phosphorus-doped than in boron-doped nanowires at low carrier density but can be larger in boron-doped nanowires at high carrier density (Persson *et al.*, 2010). Such calculations also reveal that mobility increases when the diameter of the nanowire is decreased, while it stays constant or decreases in IM devices (Niquet *et al.*, 2012).

Figure 6.5 compares the operation of inversion-mode, accumulation-mode, and JLT devices. In an n-channel IM device, the substrate is p-type and the flatband voltage, V_{FB} is located well below the threshold voltage, V_{TH} . In subthreshold operation, between V_{FB} and V_{TH} , the silicon is depleted.



6.5 Current in (a) inversion-mode (IM), (b) accumulation-mode (AM) and (c) junctionless (JLESS) nanowire multigate field-effect transistors (MuGFETs). Note the very different positions of the flatband voltage, V_{FB} .

For $V_G > V_{TH}$ the silicon surface is in strong inversion. Note that, due to quantum confinement effects, bulk (volume) inversion can also occur if the silicon film is thin enough. In an n-channel accumulation-mode device, the substrate is lightly doped n-type. In subthreshold operation, the silicon is depleted. Threshold voltage is reached when a portion of the silicon becomes neutral (i.e., no longer depleted). A small bulk current then flows in this neutral channel. Flatband voltage is reached at a slightly higher gate voltage, when the entirety of the silicon film is neutral. Between V_{TH} and V_{FB} , the device is partially depleted. Any further increase of gate voltage creates a surface accumulation layer.

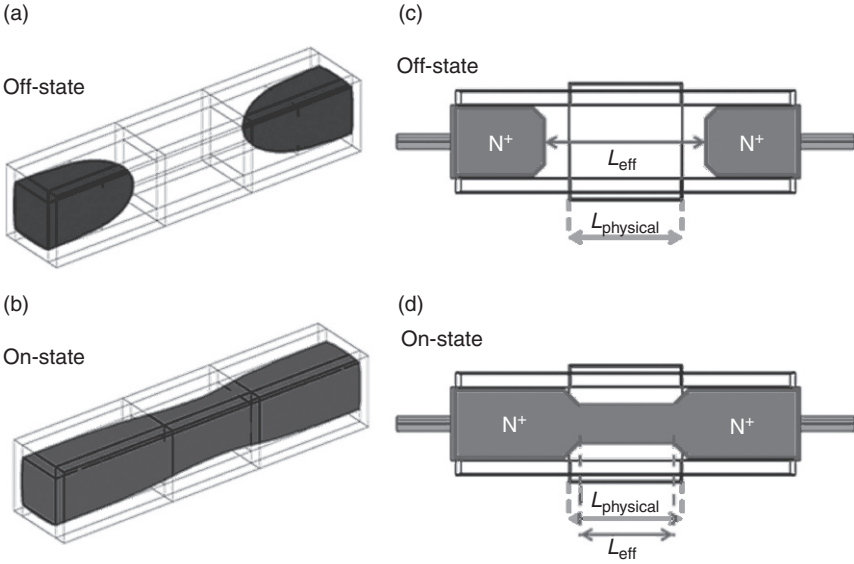
In an n-channel junctionless device, the substrate is heavily doped n-type. In subthreshold operation, the silicon is fully depleted. Threshold voltage is reached when a portion of the silicon becomes neutral. At that point the device is partially depleted. The bulk current that flows in this neutral channel is much larger than the bulk current of the accumulation-mode device because the doping concentration in the channel region is much higher. As gate voltage increases, depletion decreases and the diameter of the neutral channel increases. When the gate voltage reaches flatband voltage the entire channel region becomes neutral (assuming low V_{DS}). Further increasing the gate voltage brings about the formation of an accumulation layer. Flatband voltage is difficult to extract from current–voltage characteristics in heavily doped accumulation-mode and junctionless transistors since the transition from bulk conduction to accumulation conduction is smooth in the $I_D(V_G)$ curve and its derivatives. Instead, one can use the gate capacitance to detect flatband, since there is a clearer transition between depletion and accumulation at flatband. A curve of d^2C_G/dV_G^2 plotted as a function of V_G presents a maximum at $V_G = V_{FB}$, which can easily be used to measure flatband experimentally (Rudenko *et al.*, 2013a).

6.2.3 Short-channel effects

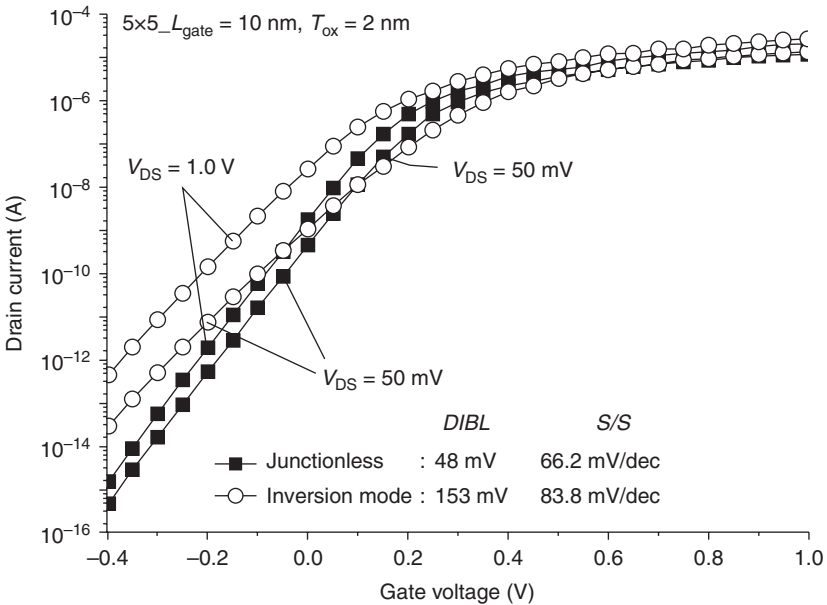
Traditional (planar SOI) accumulation-mode SOI transistors have worse short-channel characteristics than IM devices. It has, however, been demonstrated that short-channel effects in accumulation-mode double-gate (DG) MOSFETs dramatically improve and reach the same values as the IM devices when the silicon film is decreased to 10 nm and below. This observation opens the door to the design of thin and narrow accumulation-mode and junctionless nanowire FETs (Raully *et al.*, 2001; Masahara *et al.*, 2006).

In an IM MOSFET the source and drain usually overlap with the gate, and the extension of the source/drain (S/D) depletion charges due to the source and drain PN junctions in the channel region are causing short-channel effects. These effects are due to the loss of electrostatic control of the channel region by the gate. The term ‘short-channel effect’ encompasses the drain-induced barrier lowering (DIBL), the threshold voltage dependence on gate length (threshold voltage roll-off), and degradation of the subthreshold slope (SS). We will see that these effects are drastically reduced in the JLT structure.

DIBL is a key parameter for low-voltage CMOS, as it plays an important role in determining the I_{on}/I_{off} ratio of a device. Achieving a low DIBL has become as important as increasing carrier mobility for improving circuit performance (Skotnicki and Boeuf, 2010). In an IM device DIBL is caused by the increased control of the charge in the channel by the drain depletion region as drain voltage is increased. In the JLT, current blocking is not achieved by reverse-biased junctions, but rather by ‘squeezing’ the carriers out of the channel region. In practice, most of the current blocking effect occurs in the drain, outside the region covered by the gate, which increases the effective gate length, L_{eff} , above the value of the physical gate length, $L_{physical}$, when the device is turned off (Fig. 6.6). This is at the root of the short-channel effect reduction in junctionless transistors. This effect is somewhat similar to the reduction of DIBL in IM devices with gate underlap (Kranti *et al.*, 2008). The variation of effective gate length, L_{eff} , in a junctionless transistor is illustrated in Fig. 6.6. In the off mode, the effective distance between the source and drain ‘junctions’ is longer than the physical gate length (i.e., the channel depletion extends inside the source and drain), unlike in a junctioned device where there is some S/D overlap with the gate. When the device is turned on, the effective gate length becomes smaller than the physical gate length. Figure 6.6a shows the neutral (undepleted) regions in the source and drain in the off mode while Fig. 6.6b shows the neutral (undepleted) region in the source, channel, and drain in the on mode (low V_{DD} case). Figure 6.6c is a 2D representation of the increase of L_{eff} in the off state, L_{eff} being defined as the distance between the undepleted portions of the source and drain. L_{eff} becomes smaller than $L_{physical}$ when the device is turned on (Fig. 6.6d).



6.6 Illustration of the variation of effective gate length, L_{eff} in a junctionless transistor. (a) Neutral (undepleted) regions in the off mode, (b) neutral (undepleted) semiconductor when the device is turned on (low V_{DD} case), (c) $L_{eff} > L_{physical}$ in the off state, (d) $L_{eff} < L_{physical}$ when the device is turned on.



6.7 Simulated $I_D(V_G)$ characteristics of a JLT and an inversion-mode II-gate FET. $L = 10$ nm, $W_{Si} = 5$ nm, $T_{Si} = 5$ nm (squares: junctionless; circles: inversion mode).

Table 6.2 Experimental values for the subthreshold slope (SS) and drain-induced barrier lowering (DIBL) in short-channel SOI junctionless transistors

L (nm)	SS (mV/dec)	DIBL (mV/V)	Reference
50	64	7	Lee <i>et al.</i> , 2010
20	75	10	Park <i>et al.</i> , 2011a
100	62	13	Chen <i>et al.</i> , 2012
18	–	17	Jeon <i>et al.</i> , 2012
20	79	10	Park <i>et al.</i> , 2012
20	68	38	Barraud <i>et al.</i> , 2012
13	68	130	Barraud <i>et al.</i> , 2012
3	95	189	Migita <i>et al.</i> , 2012

The benefits of the junctionless source and drain configuration can be seen in Fig. 6.7 where the simulated $I_D(V_G)$ characteristics of a JLT and an IM Π -gate FET are compared. The gate length is 10 nm and the cross section of the silicon nanowire is 5 nm \times 5 nm. One can see that both the DIBL and the subthreshold slope are significantly lower in the JLT than in the IM device (Lee *et al.*, 2009). The measured subthreshold slope and DIBL in short-channel SOI junctionless transistors from different sources are listed in Table 6.2. Both DIBL and SS values are better than what is usually reported for IM devices. It is worth noting that further improvement of the short-channel effects can be obtained by increasing the extension of the gate control deeper in the source and drain regions using high- κ spacers (Gundapaneni *et al.*, 2011b). An analytical model for the dependence of the subthreshold slope in DG junctionless transistors can be found in Lin *et al.* (2012).

Transport simulations of junctionless GAA silicon nanowire FET devices with a radius of 0.6 nm and a gate length of 3.1 nm were carried out using *ab initio* simulation techniques (within a density functional theory (DFT) framework). These simulations predict that the junctionless transistor continues to work well at this scale, turning off with an I_{ON}/I_{OFF} current ratio of 10^6 , good electrostatic control of the channel by the gate, and good subthreshold characteristics. By contrast, standard junctioned MOSFET designs are very difficult to fabricate at this scale. More importantly, the distribution of charge carriers around the doping atoms blurs the boundaries of a junction over a distance comparable to the channel length, so junctions at these scales would likely fail to keep carriers out of the channel and devices cannot be turned off. Even at such small length scales, the self-consistent calculations indicate that subthreshold slopes of 74 and 80 mV/decade can be obtained for p-channel and n-channel devices, respectively (Ansari *et al.*, 2010, 2012). Recently, n-channel junctionless transistors with a gate length of 3 nm have been reported. These devices bear a remarkable resemblance to the original device patented by Lilienfeld in 1925 and exhibit an I_{ON}/I_{OFF} ratio larger than 10^6 for a drain voltage of 1 volt and a subthreshold slope of 95 mV/decade (Migita *et al.*, 2012).

6.3 Models for the junctionless transistor

A simple but useful physically based model that encompasses both the bulk current described in Equation [6.1] and the accumulation current of a JLT can be found in Tables 6.3 and 6.4. It is derived from an earlier model developed for the accumulation-mode transistors (Colinge, 1990). It is valid only above threshold but accounts for saturation of either the bulk or the accumulation current, or both. It allows one to use different mobility values for the bulk current and the accumulation current (Berthomé *et al.*, 2011).

A number of more sophisticated models based on solving Poisson's equation for either a double-gate architecture or a cylindrical geometry are available in the literature. A drain current model covering sub- and super-threshold operation long-channel DG junctionless transistors can be found in Duarte *et al.* (2011a, b). This model is a continuous 1D charge model derived by extending the concept of parabolic potential approximation for the subthreshold and the linear regions. Based on this continuous charge model, the Pao-Sah integral is analytically carried out to obtain a continuous expression for the drain current model. The proposed model captures the phenomenon of bulk conduction mechanism in all regions of device operation, including the subthreshold, linear, and saturation regions.

Another charge-based, DG model is available to calculate the charge density and the current in the junctionless FETs (Sallese *et al.*, 2011). The model is valid in all regions of operation, from deep depletion to accumulation and from linear to saturated regimes. The model is physically based and no empirical parameters or approximations are used. The model predicts the occurrence of two distinct slopes in the charge-voltage dependence, which constitutes a major difference with junction-based DG MOSFETs.

Another analytical model that assumes a cylindrical nanowire geometry can be found in Gnani *et al.* (2011). It is meant to provide a physical understanding of the device behavior. Most notably, it aims to clarify the reasons behind its nearly ideal subthreshold slope and its excellent on-state current while being a depletion device with lower electron mobility due to impurity scattering. At the same time, the model clarifies a constraint binding the allowable value of the doping density per unit length and its impact on the overall device performance. The model assumes a constant carrier mobility value and Boltzmann statistics and neglects quantum-confinement effects because it considers nanowires with sufficiently large cross sections. Since there is no closed-form solution for Poisson's equation in this case, simplifying assumptions are taken under both depletion and accumulation conditions. The model is validated by comparison with numerical results both in subthreshold and in the on-state, and very good agreement is generally achieved. The physical insight gained by this model can be used to understand and clarify the strengths and weaknesses of the junctionless transistor, such as the nearly ideal SS, the small DIBL, and the relatively large

Table 6.3 Expressions for the drain current in a JLT

Bias conditions	Drain current	Equation
$V_{GS} > V_{po}$ $V_{GS} < V_{FB}$ $V_{DS} < V_{DSat1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}} \left\{ \frac{1}{n+1} \frac{S_{max} - S_{min}}{(V_{FB} - V_{po})^n} \left((V_{GS} - V_{po})^{n+1} - (V_{GS} - V_{DS} - V_{po})^{n+1} \right) + S_{min} V_{DS} \right\}$	[6.3]
$V_{GS} > V_{po}$ $V_{GS} < V_{FB}$ $V_{DS} > V_{DSat1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}} \left\{ \frac{1}{n+1} \frac{S_{max} - S_{min}}{(V_{FB} - V_{po})^n} (V_{GS} - V_{po})^{n+1} + S_{min} V_{DS} \right\}$	[6.4]
$V_{GS} > V_{FB}$ $V_{DS} < V_{DSat2}$	$I_D = \frac{q\mu_b N_D}{L_{effb}} S_{max} C_{ox} + \frac{\mu_{acc} C_{ox} W_{eff}}{L_{affacc}} \left(V_{DS} (V_{GS} - V_{FB}) - \frac{1}{2} V_{DS}^2 \right)$	[6.5]
$V_{GS} > V_{FB}$ $V_{DS} < V_{DSat1}$ $V_{DS} > V_{DSat2}$	$I_D = \frac{q\mu_b N_D}{L_{effb}} \left\{ (S_{max} - S_{min})(V_{GS} - V_{FB}) + S_{min} V_{DS} + \frac{S_{max} - S_{min}}{n+1} \frac{\left((V_{FB} - V_{po})^{n+1} - (V_{GS} - V_{DS} - V_{po})^{n+1} \right)}{(V_{FB} - V_{po})^n} \right\}$ $+ \frac{1}{2} \frac{\mu_{acc} C_{ox} W_{eff}}{L_e}$	[6.6]
$V_{GS} > V_{FB}$ $V_{DS} > V_{DSat1}$	$I_D = \frac{q\mu_b N_D}{L_{effb}} \left(S_{max(V_{GS} - V_{FB})} + \frac{S_{max} + nS_{min}}{n+1} (V_{FB} - V_{po}) \right) + \frac{1}{2} \frac{\mu_{acc} C_{ox} W_{eff}}{L_{effacc}} (V_{GS} - V_{FB})^2$	[6.7]

Notes: These expressions include both bulk channel and accumulation channel currents. The different symbols used in the equations are defined in Table 6.4 (Berthomé *et al.*, 2011).

Table 6.4 Definition of the symbols used in Table 6.3

Symbol	Value
V_{DS}	Drain voltage
V_{GS}	Gate voltage
V_{FB}	Flat-band voltage
V_{po0}	Linear pinch-off voltage at $V_D = 0$ V
V_{po}	Pinch-off voltage $V_{po} = V_{po0} - V_{DS}$
η	DIBL coefficient
C_{ox}	Gate oxide capacitance normalized by the channel perimeter
W_{eff}	Channel perimeter
S	Neutral (non-depleted) cross section of the channel; $S = S_{min}$ when the surface is inverted and $S = S_{max}$ when the surface is accumulated
V_{DSat1}	Drain saturation voltage for the neutral bulk channel $V_{DSat1} = \frac{V_{GS} - V_{po0}}{1 - \eta}$
V_{DSat2}	Drain saturation voltage for the accumulation channel $V_{DSat2} = V_{GS} - V_{FB}$
$L_{effaccr}$ L_{effb}	Effective length of the accumulation channel and the neutral bulk channel
μ_{accr} μ_b	Effective carrier mobility in the accumulation channel and the neutral bulk channel

electron mobility. Another model for the cylindrical nanowire junctionless transistor that includes quantization effects can be found in Sorée *et al.* (2008).

A number of simulation tools and techniques have recently been applied to junctionless transistors yielding, among others, a continuous model for cylindrical junctionless transistor (Jin *et al.*, 2013); a multi-scale model that features a combination of the first-principles atomistic calculation, semi-classical semiconductor device simulation, compact model generation and circuit simulation (Yam *et al.*, 2013); a charge-based continuous model for long-channel DG junctionless transistors (Cerdeira *et al.*, 2013); and a model based on multiband quantum simulations (Huang *et al.*, 2013).

6.4 Performance comparison with trigate field effect transistors (FETs)

In this section we compare the electrical characteristics and performance of junctionless and inversion-mode multigate FETs.

6.4.1 Current–voltage characteristics

There is a trade-off between the optimization of the short-channel characteristics of junctionless transistors and their current drive. Increasing the

Table 6.5 Comparison of experimental values for the I_{ON} , I_{ON}/I_{OFF} ratio, subthreshold slope (SS), and drain-induced barrier lowering (DIBL) in short-channel SOI junctionless and IM nanowire transistors

Device type	I_{ON} (mA/mm)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)
JLT	1000	5×10^6	75	10
IM	1000	5×10^6	92	78

Notes: Gate length is 20 nm. $V_{DD} = 1$ V.

Source: Park *et al.*, 2011a.

current drive requires an increase in the doping concentration in the source and drain, including the regions that are very close to the channel. Improving short-channel effects, on the other hand, requires depleting a portion of the source and drain by the gate when the device is off, which limits the doping concentration in the parts of the source and drain that are very close to the gate (Yan *et al.*, 2011). On-current and on-off current ratio similar to those of inversion trigate MOSFETs have been reported in early publications (Rios *et al.*, 2011).

An interesting side-effect of the junctionless transistor physics is that the bulk conduction channel is located near the center of the nanowire. As a result, the gate capacitance for bulk conduction is equal to the series association of the gate oxide capacitance, C_{ox} , and the depletion capacitance in the nanowire. As a result, the gate capacitance of junctionless transistors is lower than that of either accumulation- or inversion-mode devices. Furthermore, the gate capacitance decreases when the channel doping is increased (Rios *et al.*, 2011). Table 6.5 presents a one-to-one comparison of junctionless and IM SOI nanowire transistors, revealing similar current drive and I_{ON}/I_{OFF} ratios. Both the SS and the DIBL are significantly better in the junctionless device than in the IM transistor (Park *et al.*, 2011a, b).

6.4.2 RF and analog performance

There is no experimental data available on the RF performance of junctionless transistors yet but simulation studies suggest that the cut-off frequency, f_T , of JLTs is lower than that of IM devices ($L = 30$ nm), based on the assumption of a lower carrier mobility and, therefore, a lower transconductance in the JLT. The maximum oscillation frequency, f_{max} , of the JLT, on the other hand, is higher than that of a conventional IM nanowire MOSFET because the JLT has a lower output conductance, g_{ds} , than the IM nanowire MOSFET. This study suggests that JLTs can be used in applications requiring high power gain in RF regions (Cho *et al.*, 2011a). The low output conductance of junctionless FETs also has a favorable impact on the use of the device for analog applications (Doria *et al.*, 2010, 2011a, b).

6.4.3 Noise

The $1/f$ noise in junctionless transistors is related to carrier number fluctuations. These are due to the trapping/release of charge carriers not only at the oxide–semiconductor interface but also in the depleted channel, which induce time-dependent variations of the cross-section of the neutral (undepleted) bulk conduction channel. Overall, trigate JLTs achieve noise levels similar to those in IM devices with high-quality gate oxide interfaces (Jang *et al.*, 2011). In GAA junctionless FETs, all transport below flatband is due to carriers in the center of the nanowire, far from any interface. In these devices, extremely low values of low-frequency noise are observed (Singh *et al.*, 2011).

Concerning random telegraph noise (RTN), it has been reported that a smaller relative RTN amplitude in the drain current is measured in junctionless transistors than in IM MOSFETs. This is due to the absence of an electric field attracting majority carriers (electrons in this case) toward the gate oxide/silicon interface. The average capture time of electrons into traps located in the gate oxide is considerably longer in case of the JLT devices than for the IM transistors (Nazarov *et al.*, 2011).

6.4.4 Variability and screening effect

Since junctionless transistors are heavily doped, it is of interest to study Coulomb scattering by ionized impurities, random doping fluctuations, and other variability issues that may affect device performance and reproducibility. There are basically two schools of thought regarding the issue of variability.

- The first one claims that all variability issues are directly related to the doping concentration. The higher the doping concentration, the larger the variability of device parameters with fabrication parameters such as nanowire width and thickness, and the higher the random doping fluctuation variability. An example illustrating this point of view can be found in Choi *et al.* (2011a). In this work the sensitivity of threshold voltage on the variation of silicon nanowire width was studied in GAA junctionless transistors by comparison with IM transistors with the same geometric parameters. Due to their heavily doped channel, junctionless transistors show significantly larger V_{TH} fluctuations caused by nanowire width variations than those of IM transistors with a nearly intrinsic channel. In these devices the channel doping concentration, width, thickness, and length were equal to 10^{19} cm^{-3} , 10, 20, and 50 nm, respectively. The equivalent gate oxide thickness (EOT) of the devices was equal to 13 nm, which is probably why the measured variations were so large. Another paper by Aldegunde *et al.* (2012) investigates the impact of discrete doping atoms in junctionless gate-all-around n-type silicon nanowire transistors using

3D non-equilibrium Green's functions simulations. The average doping concentration used in this example is very high (10^{20} cm^{-3}). The dopant distributions are randomly generated and modeled in a fully atomistic way. Phonon scattering, elastic and inelastic, is also included in the simulations. The results of these simulations show that junctionless nanowire transistors have a much higher subthreshold variability than their IM counterparts for the equivalent geometry and doping level (Aldegunde *et al.*, 2012). Finally, an analytical study of DG junctionless FETs is used to assess the impact of dopant number fluctuations in minimum width junctionless MOSFETs. A first-order analytic expression shows that the one-sigma threshold fluctuation is proportional to the square root of doping concentration, which places heavily doped junctionless devices at a disadvantage when compared to undoped IM devices (Taur *et al.*, 2012).

- The second school of thought claims that dopant fluctuations can be kept under control if one uses proper EOT, doping concentrations, and simulation methods. 1D and 2D simulations tend to overestimate the fluctuations by underestimating the efficiency of gate control on the channel (assuming a trigate or GAA device). Concentrations in the upper 10^{18} to lower 10^{19} cm^{-3} must be used, and low EOT values compatible with modern FET processing must be used. In addition, one must take into account the 3D nature of the device by including variability due to short-channel effects. Recent work suggests that the threshold voltage of junctionless nanowire FETs becomes less sensitive to changes in channel doping as the nanowire geometry is scaled down, which is a consequence of improved electrostatic control of the channel in the center of the nanowire from the gate (Trevioli *et al.*, 2011; Leung and Chui, 2012). It is important to note that the magnitude variability introduced by an acceptor atom in an IM device is different from that introduced by a donor atom in the equivalent accumulation-mode device. Positively charged donor ions are effectively shielded from their surroundings when surrounded by electrons. This is known as the 'screening effect' (Sun and Plummer, 1980; McKeon *et al.*, 1997; Chindalore *et al.*, 1999; Mundanai *et al.*, 1999; Ohno *et al.*, 1982; Goto *et al.*, 2012; Rudenko *et al.*, 2013b). Screening increases mobility in accumulation layers above bulk values by reducing Coulomb scattering by the dopants. It also reduces the diameter of the 'zone of electrostatic influence' of doping atoms. As a result, taking the example of n-channel devices, the presence, absence, or fluctuation of a single donor atom causes less V_{TH} variation in an accumulation-mode or junctionless transistor than an acceptor atom does in an IM device of same dimensions (Yan *et al.*, 2008; Moon *et al.*, 2010). Using a small EOT value is essential to reduce V_{TH} fluctuations in junctionless FETs. For instance, reducing EOT from 5 to 1 nm decreases $dV_{\text{TH}}/dW_{\text{Si}}$ from 25 to 6 mV/nm for $T_{\text{Si}} = 5 \text{ nm}$ and $N_D = 10^{19} \text{ cm}^{-3}$ (Colinge *et al.*, 2011; Yan *et al.*, 2011). Finally,

it is worth noting that the electrical characteristics of junctionless and accumulation-mode FETs are less sensitive to source and drain overlap/underlap variations than IM devices (Lee *et al.*, 2008). At the nanoscale, the scattering of doping atoms from source and/or drain in the channel can induce significant effective channel length variation, which greatly influences subthreshold and leakage characteristics. Facing this issue, the junctionless architecture presents less variability than IM devices in the on state (Dehdashti Akhavan *et al.*, 2011; Han *et al.*, 2013).

Because the junctionless transistor is a novel device there is little published experimental data on variability. One source of data conducted on a limited number of samples shows equivalent variations of I_{Dsat} in IM and junctionless transistors with gate lengths down to 20 nm (Park *et al.*, 2011a).

6.5 Beyond the classical SOI nanowire architecture

Due to its simplicity, the junctionless architecture can readily be applied to a number of semiconductor materials such as germanium, III–V and polycrystalline semiconductors. It is also possible to make devices having no junctions between source and drain on bulk substrates.

6.5.1 Bulk silicon versions of the junctionless transistor

Gate-all-around nanowire junctionless transistors with a width of 10 nm and a length of 50 nm have been made from bulk silicon substrates using a combination of isotropic and anisotropic etching steps. The nanowires are suspended beams above the silicon substrate. Using oxidation and polysilicon deposition the silicon nanowire channel is completely surrounded by the gate stack. Using an oxide/nitride/oxide gate dielectric the junctionless transistor can operate as a flash memory cell. Non-volatile memory characteristics have been demonstrated and parameters such as endurance, data retention, and *dc* performance show acceptable levels of performance. It can be expected that the inherent advantages of the junctionless transistor can overcome the current scaling limitations of flash memory device scaling and the junctionless transistor could become a strong candidate for the scaling of NAND flash memory devices below the 20 nm node (Choi *et al.*, 2011b).

The feasibility of a bulk silicon version of the junctionless nanowire transistor has been demonstrated using 3D simulations. Due to the N⁺N⁺N⁺ design of the device no lateral S/D junction (along the current flow path) is formed, but a vertical PN junction is required for device isolation from the substrate. The device is still ‘junctionless’ in the direction of current flow, even though a PN junction is used to insulate it from the substrate. Although the N⁺ region is heavily doped to allow for high current flow in the on state,

the small cross-section of bulk-JLMOS ensures full depletion resulting in low leakage current down to 10 nm devices (leakage currents of ~ 10 pA can be achieved in 25 nm bulk JLMOSFETs and full device functionality is observed even in the absence of reversed biased lateral PN junctions (in the direction of current flow)). The subthreshold slope and DIBL can be limited to less than 80 mV/decade and 100 mV/V, respectively, in bulk JLT devices for gate lengths down to 12 nm. The DIBL performance of the bulk JLT is similar to that of the SOI JLT. The subthreshold slope of the bulk JLT, on the other hand, is more degraded at short gate length than in the case of SOI devices (Colinge *et al.*, 2011). It is worth mentioning that a planar version of the bulk junctionless transistor has been proposed as well, in which case the nanowire structure is not required for the channel and the use of a thin n-type silicon layer on a P-type substrate can provide a functional device (Gundapaneni *et al.*, 2011a).

6.5.2 Germanium-on-insulator devices

Junctionless field-effect transistors made on a Ge-on-insulator (GeOI) substrate have been demonstrated experimentally. These devices have the potential of combining the higher mobility in Ge than in Si with all the advantages of a junctionless FET. P-channel devices were made in an 11 nm-thick GeOI layer doped at a concentration of 10^{19} cm $^{-3}$. The devices show similar current–voltage (I–V) characteristics to conventional FETs, and their on/off current ratio is larger than 10^4 . The field-effect mobility is equal to 120 cm 2 /Vs and is independent of the channel carrier density (Zhao *et al.*, 2011, 2012). N-channel germanium MOSFETs are notoriously difficult to fabricate and show poor performance despite the high mobility of electrons in bulk germanium. This is due to the difficulty of introducing high S/D doping concentrations and to the relatively poor quality of the Ge/gate oxide interface. The use of the junctionless architecture can help alleviate these problems since only moderately high doping levels can be used and since a good deal of channel carriers flow in the bulk of the device. Back-gated N-channel transistors made in GeOI films with a thickness of 15–32 nm and doping concentrations between 1×10^{18} and 5×10^{18} cm $^{-3}$ have been reported to achieve an electron channel mobility of 1000 cm 2 V $^{-1}$ s $^{-1}$ and an on/off drain current ratio of 10^5 at $V_{DS} = 1$ V (Kabuyanagi *et al.*, 2013).

6.5.3 III–V junctionless transistors

A fabrication process for making junctionless transistors on gallium arsenide (GaAs) has been proposed, and the associated device simulations have been

reported. The channel material is a 20 nm-thick N^+ GaAs layer epitaxially grown on a Si substrate with a thick enough buffer layer of P^+ germanium between the silicon and the GaAs. GaAs and Ge have a large energy band-gap offset, which enables self-isolation by effectively blocking leakage paths between the GaAs channel and substrate under any practical bias conditions. The Ge buffer layer and GaAs channel doping concentrations are $3 \times 10^{17} \text{ cm}^{-3}$ and $1 \times 10^{18} \text{ cm}^{-3}$, respectively. An on/off current ratio of 3×10^7 was demonstrated by simulation (Cho *et al.*, 2011b).

Junctionless transistors made in sub-10 nm extremely thin body (ETB) InGaAs-on-insulator (InGaAs-OI) were demonstrated on Si wafers. The devices were made using a direct wafer bonding process and have an ultra-thin Al_2O_3 buried oxide (UTBOX). Devices with a channel thickness of 9 and 3.5 nm were made. The 9 nm-thick ETB InGaAs-OI n-channel junctionless MOSFETs with a doping concentration (N_D) of 10^{19} cm^{-3} exhibit a peak electron mobility of $912 \text{ cm}^2/\text{Vs}$ and a mobility enhancement factor of 1.7 times compared to a Si n-channel MOSFET at a surface carrier density (N_s) of $3 \times 10^{12} \text{ cm}^{-2}$. In addition, it has been found that, owing to the use of a thin Al_2O_3 UTBOX layer, the devices have excellent cut-off properties. As a result, an $I_{\text{ON}}/I_{\text{OFF}}$ ratio of approximately 10^7 has been obtained in the 3.5 nm-thick ETB InGaAs-OI JLTs. These results indicate that the high mobility III–V nMOSFETs can be realized even in sub-10 nm-thick channels (Yokoyama *et al.*, 2011).

Junctionless transistors were made in GaN/sapphire nanowires with a width of 60–200 nm and a thickness of 120 nm. The devices were N-type doped with silicon atoms to a concentration of $4 \times 10^{18} \text{ cm}^{-3}$. These junctionless GaN nanowires exhibit excellent OFF-state performance such as a subthreshold slope of 68–137 mV/decade and an extremely low leakage current of 10^{-8} mA/mm , yielding an $I_{\text{ON}}/I_{\text{OFF}}$ ratio of 10^9 . A subthreshold slope of 68 mV/decade is obtained for devices with a width of 60 nm and a gate length of 1 μm . Most remarkably, these devices have a drain breakdown voltage of 500 V (Im *et al.*, 2013).

6.5.4 Polysilicon junctionless transistors

Gate-all-around polycrystalline silicon (poly-Si) nanowire transistors with junctionless configuration have been fabricated by utilizing only one heavily doped poly-Si layer to serve as source, channel, and drain regions. *In situ* doped poly-Si material features high and uniform doping concentration, facilitating the fabrication process. The developed JLT device exhibits desirable electrostatic performance in terms of higher $I_{\text{ON}}/I_{\text{OFF}}$ ratio and lower source/drain series resistance as compared with the IM counterpart. Such

a scheme appears of great potential for future system-on-panel and 3D IC applications (Su *et al.*, 2011).

Planar n-type junctionless poly-Si thin-film transistors (TFTs) with an ultrathin and heavily phosphorous-doped channel have been successfully fabricated. The devices show excellent performance with a subthreshold swing of 240 mV/dec and an on/off current ratio larger than 10^7 . Moreover, the junctionless devices show a 23-fold increase of on-state current at a gate overdrive of 4 V as compared to conventional IM control devices with an undoped channel. The significant improvement in the current drive is ascribed to the inherently high carrier concentration contained in the channel of the JL device. These results provide evidence of the great potential of the JL poly-Si TFTs for manufacturing future 3D and flat-panel electronic products (Lin *et al.*, 2012; Chen *et al.*, 2013).

P-type junctionless transistors made in polycrystalline germanium have an advantage over poly-Si transistors because of higher carrier mobility, and thus higher current drive. Poly-Ge junctionless trigate p-FETs with gate lengths down to 40 nm were made in poly-Ge nanowires with a width of 7 nm. An I_{ON}/I_{OFF} ratio larger than 10^5 was obtained at $V_D = -1$ V, with a subthreshold slope of 158 mV/decade and a DIBL as small as 74 mV/V. These values are comparable to those obtained in monocrystalline Ge devices. Devices with $L_G = 80$ nm exhibit a current drive of $100 \mu\text{A}/\mu\text{m}$ at $V_D = -1$ V (Kamata *et al.*, 2013).

6.5.5 Indium tin oxide (ITO) junctionless transistors

Junctionless, transparent, electric-double-layer thin-film transistors with an in-plane gate figure were fabricated on glass substrates at room temperature. In these junctionless transistors the channel and source/drain electrodes are made of the same thin indium tin oxide (ITO) film without any extra source/drain junction doping. Effective field-effect modulation of drain current can be obtained when the ITO thickness is reduced to 20 nm. Such junctionless, transparent TFTs exhibit a good electrical performance with a small subthreshold swing (<0.2 V/decade), a high mobility (~ 20 cm²/Vs), and a large I_{ON}/I_{OFF} ratio ($>10^6$), respectively (Jiang *et al.*, 2011a). The concept was further extended to the fabrication of junctionless, flexible thin-film transistors made on paper substrates using a room temperature process. Channel and source/drain electrodes are made in an ITO film without any source/drain junctions. Effective field-effect modulation of the drain current can be obtained if the thickness of the ITO film is thin enough (20 nm). These junctionless paper TFTs show good device performance with a subthreshold slope of 210 mV/decade and an I_{ON}/I_{OFF} ratio of 2×10^6 . Such junctionless

TFTs on paper can provide a new opportunity for flexible paper electronics and low-cost, portable-sensor applications (Jiang *et al.*, 2011b).

6.6 Conclusion

Junctionless transistors are unipolar, thin-film, heavily doped (typically in the 10^{19} cm^{-3} range) MOS transistors. Because of its simple design, the junctionless transistor architecture has been adapted to semiconductor materials other than silicon. In the off-state the channel is fully depleted owing to the workfunction difference between the semiconductor and the gate material. When the device is turned on, a substantial part of the current is carried in the bulk of the thin film, and is usually augmented by an accumulation current contribution. Junctionless transistors are characterized by reduced short channel effects and present excellent subthreshold slope and low DIBL. As a result, CMOS junctionless devices with outstanding short-channel characteristics have been demonstrated for gate lengths down to 13 nm. The junctionless transistor is probably the most scalable of all FET structures, as demonstrated by both *ab initio* simulations and experimental devices with gate lengths as small as 3 nm.

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Silicon-on-insulator (SOI) fin-on-oxide field effect transistors (FinFETs)

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Abstract: New device architectures, such as FinFETs, are required at the nanometer regime for the continuity of complementary metal-oxide semiconductor (CMOS) scaling. Using bulk FinFETs as a reference technology, this chapter evaluates the performance and variability aspects of SOI FinFETs. The results indicate that due to the BOX isolation instead of the junction isolation, SOI FinFETs can have a considerable advantage over bulk FinFETs regarding device leakage and drive current performance. SOI FinFETs have much lower process-induced variability thanks to the better fin definition in SOI technology. With matching factors of A_{VT} of around 1.2 mV.μm, SOI FinFETs are resilient to statistical variability as well.

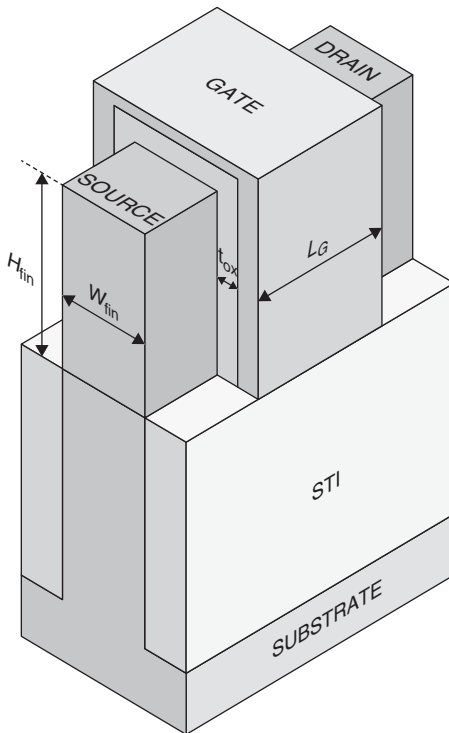
Key words: SOI, FinFET, CMOS, statistical variability, process variation, leakage current, drive current.

7.1 Introduction

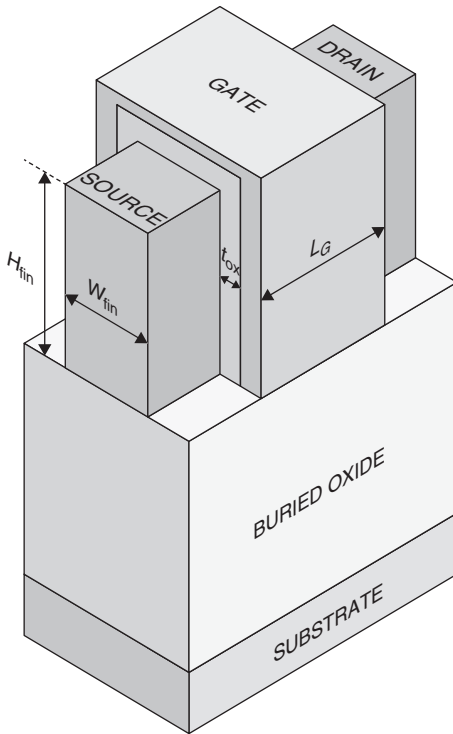
With the traditional bulk-MOSFET architecture reaching scaling limits due to performance limitations and excessive random discrete dopant fluctuations,¹ new, better performing and variability-resilient device architectures, such as FinFETs and ultra-thin body (UTB) silicon-on-insulator (SOI) devices, are required in order to maintain the benefits of technology scaling at the 22 nm node and beyond.²⁻⁷ Indeed, Intel introduced FinFETs in their 22 nm CMOS technology offering⁸ and UTB fully depleted (FD) SOI is now available from a selection of the Common Platform partners.⁹ FinFETs can offer significant improvements in performance, leakage and variability at the expense of complex 3D structure and manufacturing process. The FinFETs introduced by Intel at 22 nm, and promised by key foundries at 16/14 nm CMOS technology generations, are ‘bulk’ FinFETs due to the

abundance of ‘bulk’ silicon wafer. In bulk FinFET, the fin extends from the silicon substrate above the shallow trench insulation (STI), as illustrated in Fig. 7.1. The etching of the STI trenches after fin definition affects the resultant fin shape and introduces fin shape variability.^{10–12} Moreover, a high dose angled implantation at the base of fin is needed to create junction isolation between fins. A neater way to fabricate FinFET devices is to use a SOI substrate. In SOI FinFETs, as illustrated in Fig. 7.2, the etching of the fin stops at the buried oxide (BOX). It allows better fin shape definition and control,^{13,14} and fins are naturally isolated by the BOX. The difference between junction isolation and BOX isolation can also have an impact on parasitic capacitance. A recent study¹⁰ indicates that the BOX layer helps to minimize capacitance for SOI FinFET, while junction-isolated bulk FinFETs suffer from additional capacitance due to the junction isolation. It also concludes that although SOI-based FinFETs suffer a modest cost penalty due to the increased substrate cost, at high volumes, this can be largely offset by the cost of the more complex bulk process.¹⁰

Although it is now well recognized that using SOI wafer not only simplifies the FinFET fabrication process, but can also improve the quality



7.1 Bulk trigate FinFET.



7.2 SOI trigate FinFET.

of fin definition, there are still some remaining questions that need to be answered. One of these questions is: is there any performance penalty of using the SOI FinFET architecture compared to bulk FinFET architecture? Using bulk FinFETs as the reference technology, a comprehensive simulation study is carried out to evaluate and benchmark SOI FinFET technology from both normal performance aspect and variability aspect. This study is targeted at sub-20 nm technology nodes, using ‘optimal’ devices designed for 14 and 16 nm technology nodes as the test bed devices. The simulations are carried out with the Gold Standard Simulations Ltd (GSS) statistical ‘atomistic’ simulator GARAND,¹⁵ which is a drift-diffusion simulator that includes density gradient quantum corrections,¹⁶ that are essential for the simulation of thin body devices such as FinFETs.

In the following section, based on a wide range of device configurations and using the 14 nm technology node as an example, we present the evaluation study of SOI FinFET performance against its bulk counterpart with both trigate and double gate (DG) architectures. In Section 7.3 the impact of the SOI substrate on device short channel effects is discussed with a typical device configuration from a trigate 16 nm technology node. Section 7.4 is

dedicated to the process and statistical variability aspect of FinFET devices where we use the bulk FinFET as the control device, and we analyse the impact of variability on the electrical characteristics of SOI FinFET at a 16 nm technology node. The conclusions are drawn in Section 7.5.

7.2 SOI FinFET device performance

Before the detailed discussion of the SOI FinFET device performance, some generic aspects of the operation of the SOI and bulk FinFETs are illustrated to provide differentiation between the two architectures despite the identical fin dimensions. The structures of the simulated trigate FinFETs are schematically illustrated in Figs 7.1 and 7.2. Plate I (see colour section between pages 202 and 203) shows the electrostatic potential distribution through the middle of the fin. It is clear that for bulk FinFETs the high level of stopper layer doping can effectively suppress the penetration of the drain field into the channel, which is expected to have a beneficial effect on drain induced barrier lowering (DIBL). In the SOI FinFET the channel penetration of the drain field is determined by the BOX thickness and the permittivity of BOX material. In this case, due to the thick BOX used in this study, the bulk FinFET will have better subthreshold performance than the SOI FinFET transistor (it is worth mentioning that by introducing a thin BOX, the electrostatic performance of SOI FinFET can be improved, as demonstrated in Section 7.3).

However, previous studies indicated that for thin body devices, due to the increasing influence of source/drain resistance on device performance,¹⁷ better subthreshold behaviour does not necessarily result in better device performance. Examining from a different perspective, we look at another possible mechanism that can affect FinFET device performance. Plate II compares the carrier density in the middle of the channel at $V_G = V_T$ (gate is biased at threshold voltage) for a typical SOI and bulk FinFET transistors at a 16 nm technology node. For the bulk FinFET the built-in potential of the stopper results in a depletion of the bottom part of the channel, somewhat reducing the effective fin height. The carriers and the current penetrate further down into the SOI fin, and the carrier distribution is centred and heavier towards the bottom of the fin. This is partially due to the drain field penetration and the corresponding drain bias control of the channel carriers. This indicates that the SOI FinFET has some intrinsic advantages over the bulk FinFET in regards to device performance through increase of effective fin height.

In the following evaluation and benchmark study, the transistors on SOI and bulk substrates have identical dimensions with fixed fin height at 25 nm, and the same channel and source/drain doping profile. In order to provide a balanced picture on device performance, a device design space, which is targeted at 14 nm technology node, is considered here with a combination of

Table 7.1 Device parameters

Parameter	Value (nm)
Gate length, L_G	18, 20, 22
Fin width, W_{Fin}	8, 10, 12
Fin height, H_{Fin}	25
Equivalent oxide thickness (EOT)	0.8
STI depth	30

three gate lengths and three fin width configurations. For the bulk FinFET a $5 \times 10^{18} \text{ cm}^{-3}$ channel stop doping is introduced below the channel. A high- κ gate dielectric is used to minimize gate leakage, with EOT at 0.8 nm. The device parameters are listed in Table 7.1, with supply voltage at 0.9 V.

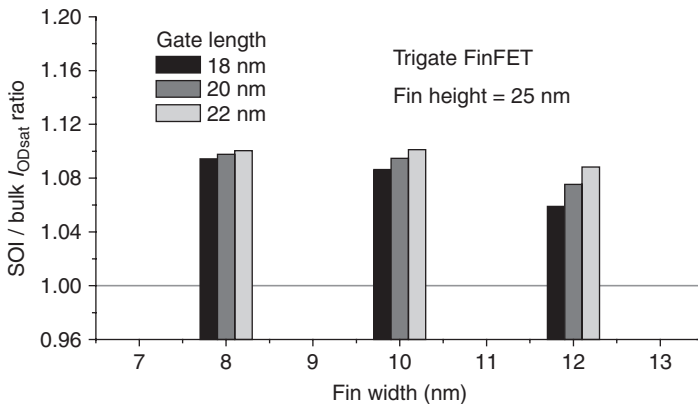
All simulations in this study are carried out with the GSS drift-diffusion (DD) simulator GARAND.¹⁵ Density gradient quantum corrections are included to capture the quantum confinement effects inherent to the narrow FinFETs. It is well known that DD simulations cannot accurately predict nanometer-scale transistor performance without the calibration of mobility models.¹⁸ Therefore the saturation velocity and strain in the DD simulations has been further adjusted to match the experimental target FinFET performance. The Masetti low-field mobility model¹⁹ is used with modification for strain, while the Lombardi²⁰ and Caughey-Thomas models²¹ account for high-field effects. The same mobility parameters are used for both the SOI and the bulk FinFETs.

Leakage current and on-current are two important device figures of merit determining circuit and system standby time, and speed performance. They are selected for the evaluation and benchmark of the SOI FinFET technology against its bulk counterpart. It is possible to employ a metal gate work function tuning technique to adjust device leakage and on-current performance according to the actual application requirement. Consequently, the gate work function (WF), which determines device threshold voltage V_T , cannot be treated as a fixed value in these devices. In order to provide a fair comparison at device architecture level (SOI vs bulk), overdrive current I_{ODsat} is used here as the on-current. This is defined as the drain current at constant overdrive gate voltage of $V_G = V_T + 0.7 \text{ V}$ with $V_D = V_{\text{DD}} = 0.9 \text{ V}$, and V_T is determined by a constant current criterion that is the same for both SOI and bulk transistors. A similar approach is employed for leakage current as well: by adjusting the metal gate work function to deliver the same drain current at $V_G = V_D = V_{\text{DD}} = 0.9 \text{ V}$ for the same fin configuration of the SOI and the bulk transistors, the leakage current I_{off} is defined as the device drain current at $V_G = 0 \text{ V}$, $V_D = V_{\text{DD}} = 0.9 \text{ V}$.

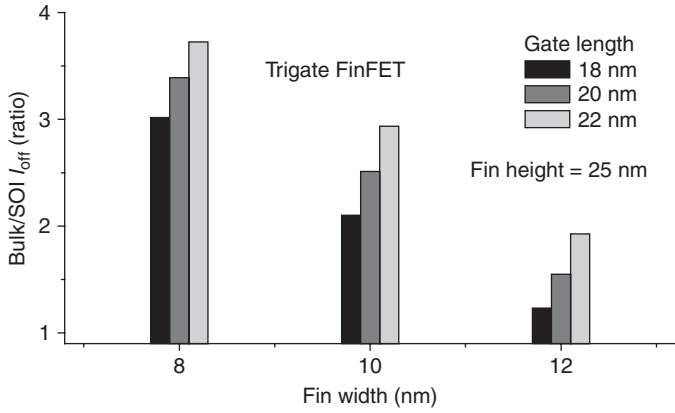
Figure 7.7 illustrates the ratio of the SOI and the bulk FinFET transistor on-currents $I_{\text{ODsatSOI}}/I_{\text{ODsatBULK}}$ against the fin geometry and gate length. The

performance advantage of SOI ranges from 6% to 10% across the design parameter space. Since in the simulation set-up both SOI and bulk FinFETs have the same level of leakage current, this indicates that there is a 6–10% improvement on I_{on}/I_{off} ratio in SOI compared to bulk. For a narrow fin, since both SOI and bulk FinFETs have excellent electrostatic control, there is a similar level of improvement for all gate lengths. However, for a wide fin there is a compromise between the intrinsic performance improvement of SOI architecture and the better electrostatic property of the bulk architecture, and device performance improvement can be gate length dependent. Based on the trend present in Fig 7.3, a further increase of fin width accompanied by a further reduction of gate length can diminish the performance advantage of a SOI FinFET. However, in a good FinFET design the fin width scaling factor should be similar to gate length scaling factor. Consequently, under normal design practice SOI FinFETs will offer better performance than bulk FinFETs.

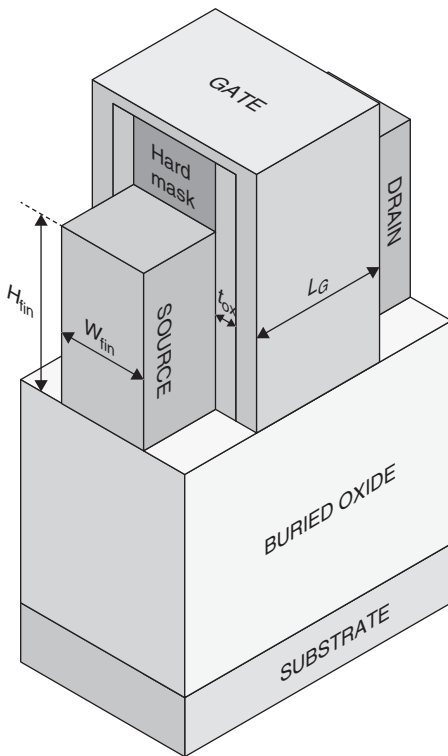
Figure 7.4 illustrates the ratio of the bulk and the SOI FinFET transistors off-currents $I_{offBULK}/I_{offSOI}$ against the fin geometry and gate length. The leakage current of SOI FinFETs can be 2~4 times smaller than bulk FinFETs where both devices have the same drive current. The general trend of leakage improvement in SOI is similar to on-current, where a narrow fin width and long gate length give SOI the biggest leakage advantage. This is a consequence of interplay between intrinsic improvement of effective fin height of the SOI FinFET and a better electrostatic behaviour of the bulk FinFET, although the SOI leakage advantage can be diminished with devices having extreme short channel lengths and very wide fin widths. Under normal design practice, the SOI FinFET will offer better leakage performance.



7.3 The ratio of the SOI and bulk FinFET on-current against fin geometry and gate length.



7.4 The ratio of the SOI and bulk FinFET off-current against fin geometry and gate length.

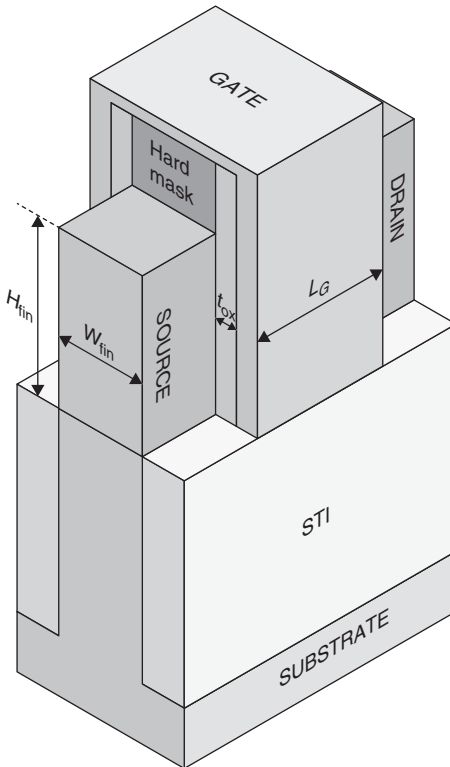


7.5 SOI double gate FinFET.

Apart from the trigate structure, double gate is another type of FinFET supported by IBM and its alliance.²² As illustrated in Figs 7.5 and 7.6, DG FinFETs can be fabricated on both SOI and bulk substrates. Using the same fin and gate length configurations as trigate FinFETs, a DG SOI FinFET is evaluated and benchmarked against its bulk counterpart.

Figure 7.7 depicts the ratio of the SOI and the bulk DG FinFET transistor on-currents $I_{ODsatSOI}/I_{ODsatBULK}$ against the fin geometry and gate length. The SOI DG FinFETs deliver in the range of 12–16% higher drive current depending on the actual design of the fin geometry, translating into a 12–16% improvement on I_{on}/I_{off} ratio. The performance advantage of SOI is more pronounced in a DG structure compared to a trigate structure, due to the fact that the relative reduction in effective device width is larger in bulk DG FinFET compared to bulk trigate FinFET.

Figure 7.8 illustrates the ratio of the bulk and the SOI DG FinFET transistor off-currents $I_{offBULK}/I_{offSOI}$ against the fin geometry and gate length. Similar to the drive current case, in a DG structure, SOI technology offers a clear advantage on leakage performance compared to bulk technology. In



7.6 Bulk double gate FinFET.

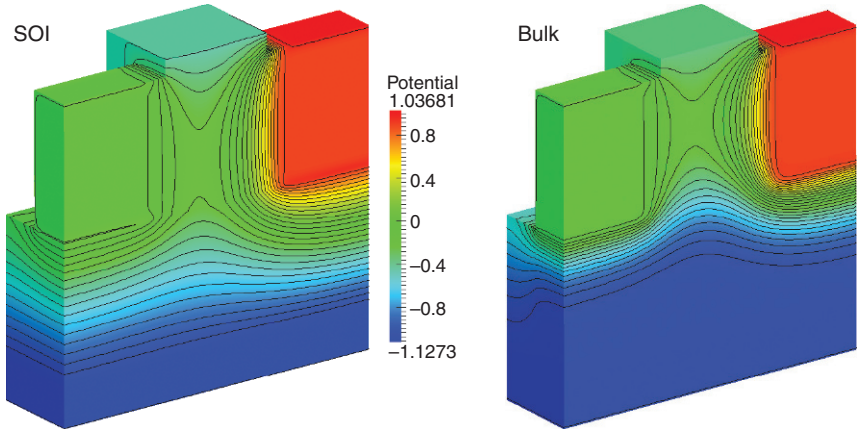


Plate I (Chapter 7) Electrostatic potential through the middle of SOI and bulk FinFETs.

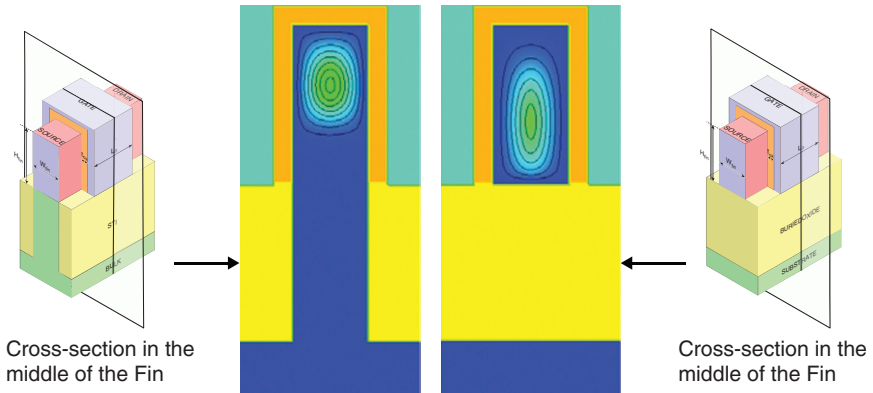


Plate II (Chapter 7) Comparison of the carrier concentration in the cross-section across the middle of the SOI and the bulk FinFETs.

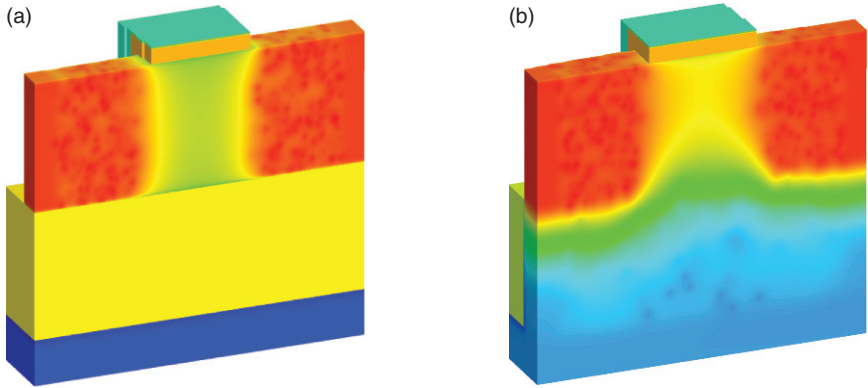


Plate III (Chapter 7) Electron concentration at threshold in one statistical instance of the (a) SOI and (b) bulk FinFETs cut down the fin middle, including all sources of statistical variability.

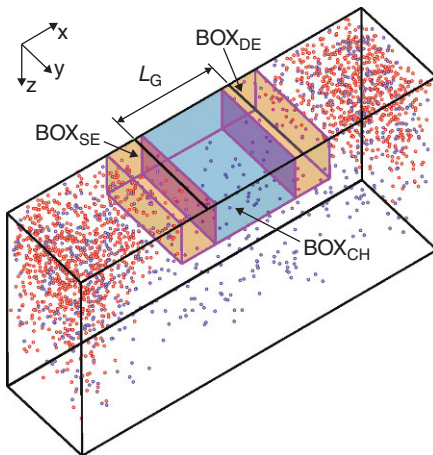


Plate IV (Chapter 8) Illustration of random dopant fluctuations in the substrate of an 18 nm n-type, bulk MOSFET. Donor and acceptor atoms are depicted as red (dark) and blue (light) spheres, respectively. L_G indicates the gate length, while the shaded regions marked as BOX_{CH} and $BOX_{SE/DE}$ delimit the critically important regions of the channel and the source/drain extensions.

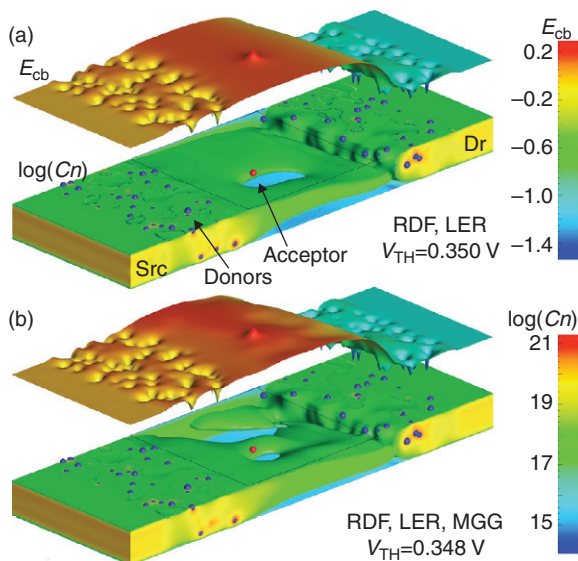


Plate V (Chapter 8) Conduction band landscape (E_{cb}) and electron density distribution (Cn); fixed dopant distribution due to RDF and LER, (a) without and (b) with MGG. Semi-transparency for low concentration reveals the shape of a Cn iso-surface at $3.2 \times 10^{17} \text{ cm}^{-3}$. $V_D = 1$ V, $V_G = 0.5$ V.

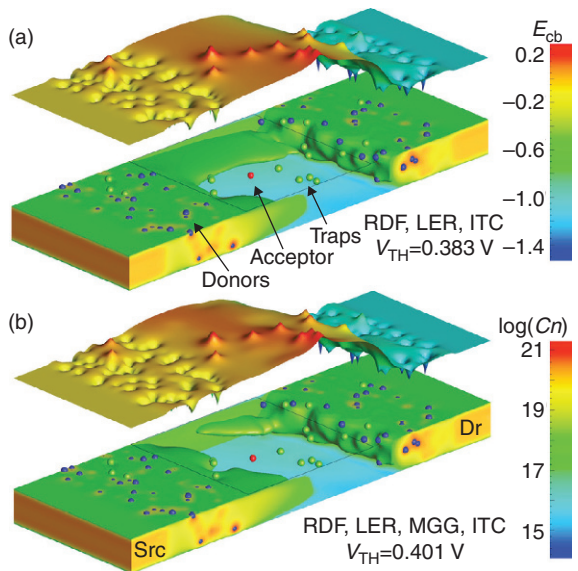


Plate VI (Chapter 8) Conduction band landscape (E_{cb}) and electron density distribution (Cn); fixed dopant distribution due to RDF, LER, and ITC, (a) without and (b) with MGG. Semi-transparency for low concentration reveals the shape of a Cn iso-surface at $3.2 \times 10^{17} \text{ cm}^{-3}$. $V_D = 1$ V, $V_G = 0.5$ V.

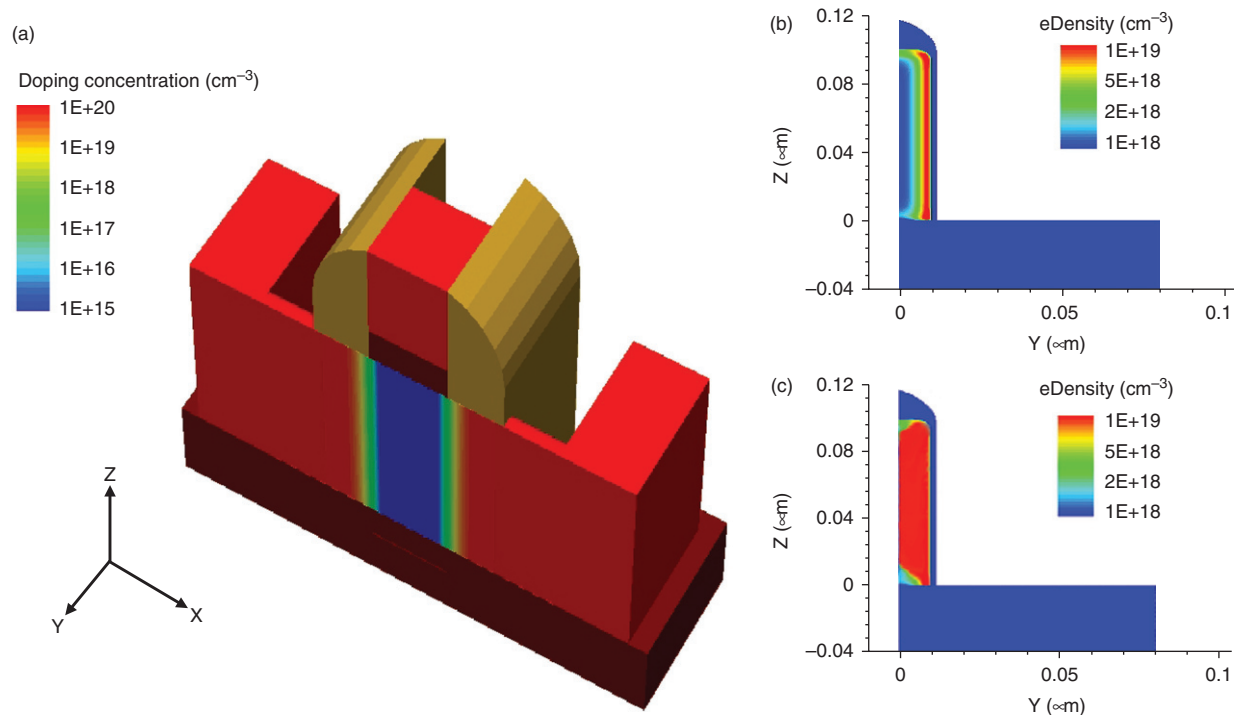
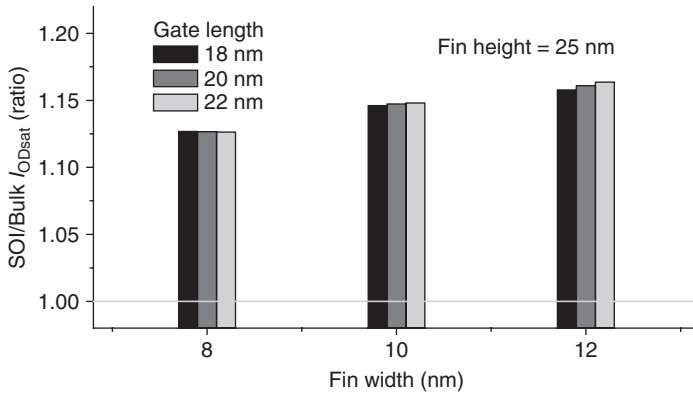
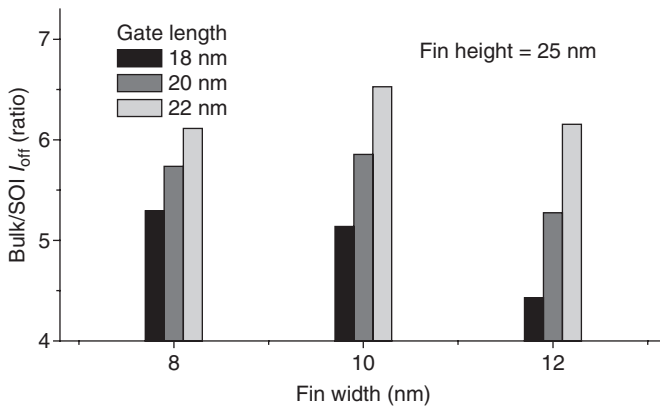


Plate VII (Chapter 9) Simulated half of undoped channel FinFET structure with $t_{Si} = 20\text{ nm}$, $h_{Si} = 100\text{ nm}$, $t_{ox} = 50\text{ \AA}$ and metal gate: (a) 3D visualization of doping concentration, (b) simulated electron distribution at $V_{ds} = 2.5\text{ V}$ and $V_{gs} = 1\text{ V}$ and (c) simulated electron distribution at 'hot gate' bias condition $V_{gs} = V_{ds} = 2.5\text{ V}$. Device cross-section is taken across the channel in the middle of the gate. (© 2008 IEEE. Reprinted, with permission, from Khazhinsky, M.G., Chowdhury, M.M., Tekleab, D., Mathew, L. and Miller, J.W. (2008) 'Study of undoped channel FinFETs in active rail clamp ESD networks', *IEEE Proceedings*.)



7.7 The ratio of the SOI and bulk DG FinFET on-current against fin geometry and gate length.



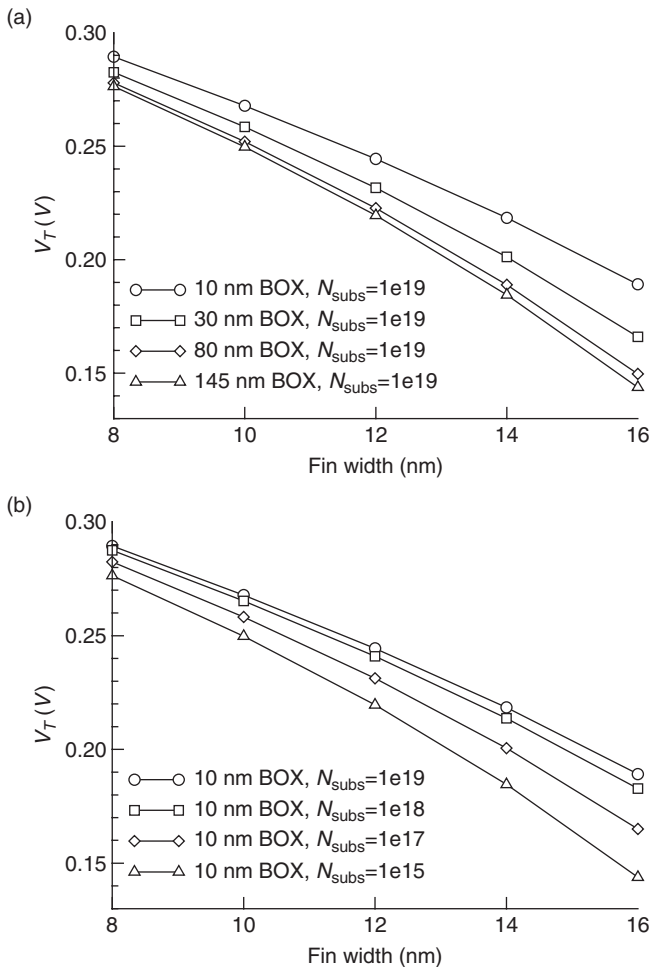
7.8 The ratio of the SOI and bulk DG FinFET off-current against fin geometry and gate length.

most cases it can deliver more than 5 times reduction of leakage current while maintaining the same drive current performance of bulk DG FinFETs.

7.3 SOI FinFET substrate optimization

For a typical design discussed in this study, the SOI FinFET architecture can have slightly worse short channel effects compared to its bulk counterpart. However, its short channel effects and the resulted process sensitivity can be improved by the optimization of the SOI substrate.²³ Similar to the case of FD-SOI MOSFETs, the reduction of the BOX thickness, in combination with the introduction of heavily doped ground plane beneath the BOX, can

reduce the drain potential coupling to the carrier concentration in the channel and can significantly reduce DIBL.²⁴ Using an SOI trigate FinFET targeted at 16 nm technology as an example, Fig. 7.9 shows V_T sensitivity of the SOI FinFETs against the fin width under different BOX thicknesses varying from 145 nm down to 10 nm, and also for different doping concentrations in the substrate below the BOX. It clearly shows that SOI FinFET processing sensitivity can be improved by using thinner BOX and implementation of a highly doped ground plane below the BOX. With the ground plane doping fixed at $1.0 \times 10^{19} \text{ cm}^{-3}$, and the BOX thickness changed from 145 to 10 nm, the sensitivity of fin width on device V_T can be reduced by 30%. With the



7.9 Sensitivity to fin width and its dependence on (a) BOX thickness and (b) substrate doping below the BOX, for the SOI trigate FinFET.

BOX thickness fixed at 10 nm, and the ground plane doping increased from 1.0×10^{15} to $1.0 \times 10^{19} \text{ cm}^{-3}$, the sensitivity of fin width on device V_T can be reduced by 30% as well.

7.4 Process and statistical variability of FinFETs

Due to the 3D nature of FinFET devices, process variation on fin definition will have a considerable impact on device performance.²³ The height of the bulk fin is determined by a number of process steps, including the etching time of the STI recess. As a result it is generally expected that there will be larger process variation in the height of the bulk FinFET compared to SOI.^{10,12} In the following analysis we assume in the bulk FinFET case a process-induced variation ($\pm 3\sigma$) of fin height ± 5 nm and width ± 2 nm. In the SOI FinFET case these variations can be reduced to ± 1 nm in fin height, since it is solely defined by SOI layer uniformity, which is well characterized and typically even lower at ± 0.5 nm,¹⁴ and ± 1.5 nm in fin width. Tables 7.2 and 7.3 summarize the calculated process corners for the nominal device at a trigate 16 nm technology node ($W_F = 12$ nm, $H_F = 30$ nm and $L_G = 25$ nm). The SOI FinFET will have a V_T corner range improved by a factor of 2. Even more spectacularly, $\Delta I_{\text{ODsat}}/I_{\text{ODsat}}$ variation is reduced from 28.7% in the bulk case down to 7.3% for the SOI.

Although FinFET devices can tolerate very low channel doping, the random discrete dopants (RDD) in the source/drain region can still play an active role in variation of device characteristics. In RDD simulation set-up, a very low channel doping level ($1 \times 10^{15} \text{ cm}^{-3}$) is assumed for both SOI and bulk FinFETs since both devices have exactly the same fin configuration. However, in reality, a much higher level of channel doping concentration can be required in bulk FinFETs. This is often applied to overcome the possible short channel effect degradation associated with the poor fin definition in the bulk technology. The RDD results presented here represent the best RDD performance that can be achieved by a bulk FinFET. Due to the 3D nature of the FinFET device, line edge roughness (LER) in FinFETs not only introduces traditional

Table 7.2 Figures of merit for the SOI and bulk FinFETs under the influence of process variation

	H control (nm)	W control (nm)	V_T min (V)	V_T max (V)	V_T range (V)	SS min (mV/ Dec)	SS max (mV/ Dec)	SS range (mV/ Dec)
Bulk fin	± 5	± 2	0.147	0.212	0.065	69.5	77.6	8.1
SOI fin	± 2	± 2	0.167	0.229	0.062	71.9	80.3	8.5
SOI fin	± 1	± 1.5	0.175	0.221	0.046	72.8	79.2	6.33

Note: Nominal device geometry: $W_F = 12$ nm, $H_F = 30$ nm and $L_G = 25$ nm.

Table 7.3 Performance variation for the SOI and bulk FinFETs under the influence of process variation

	H control (nm)	W control (nm)	I_{ODsat} min (μA)	I_{ODsat} max (μA)	I_{ODsat} range (μA)
Bulk fin	± 5	± 2	69.8	95.5	25.6
SOI fin	± 2	± 2	82.0	93.1	11.1
SOI fin	± 1	± 1.5	84.9	90.7	5.8

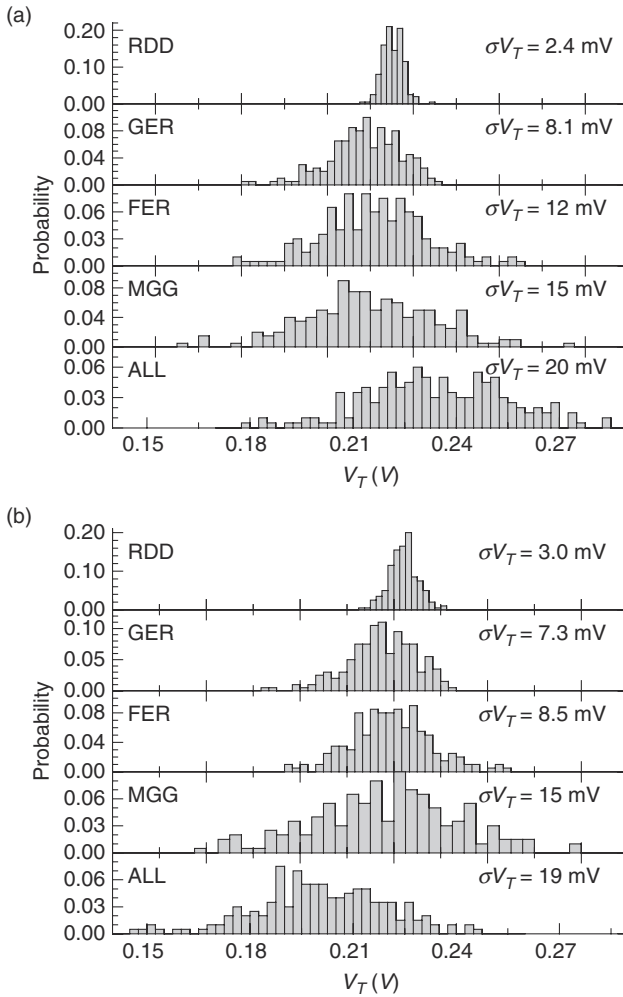
Note: Nominal device geometry: $W_F = 12$ nm, $H_F = 30$ nm and $L_G = 25$ nm.

gate edge roughness (GER) variation, but also introduces fin edge roughness (FER) variation. Depending on the high- κ /metal gate stack technology employed in the manufacturing process, metal gate granularity (MGG) can be a major variability source²⁵ in FinFET devices. Here we present the statistical variability simulation results of SOI trigate FinFETs targeted for a 16 nm technology node. To put the results in context, a bulk FinFET transistor with the same fin configuration is used as the control device, and it is subjected to the impacts of the same statistical variability sources with identical variability parameters as the SOI FinFET. The statistical variability simulations are carried out with GARAND. RDD, GER, FER and MGG are introduced individually and in combination in the simulations.

The resolution of the individual discrete dopants in the RDD simulations employs fine meshing in conjunction with density gradient quantum corrections. This prevents artificial charge trapping in the sharply resolved Coulomb wells of the ionized dopants, avoids acute mesh-spacing sensitivity¹⁶ which is particularly important when resolving random discrete dopants in the source/drain regions where artificial charge trapping can introduce an unphysical increase in the access resistance.

LER is modelled with the assumption that it follows a Gaussian autocorrelation function²⁶ with three times root-mean-square deviation of the gate edge position of $LER = 3\Delta = 2$ nm and a correlation length of $\Lambda = 30$ nm. This is used to model both GER and FER. The modelling of MGG assumes a TiN metal gate with two major grain orientations leading to a work function difference of 0.2 V, with a probability of 0.4/0.6 for the lower/higher WF, respectively, and an average grain diameter of 5 nm.^{27–29} For each individual source, and for their combinations, ensembles of 1000 microscopically different devices were simulated using the automated GSS cluster simulation technology.

Plate III illustrates the electron concentration in one statistical instance of the SOI FinFET cut down the fin middle, including all sources of statistical variability, the results from the bulk control device are also presented here. This not only provides visual understanding of the physical type of statistical variability simulations and the impact of the variability sources on the electron concentration distribution in the transistors, but also highlights



7.10 Histograms of threshold voltage for the nominal ($W_F = 12$ nm, $H_F = 30$ nm and $L_G = 25$ nm) (a) SOI and (b) bulk trigate FinFETs subject to the following sources of statistical variability: RDD, GER, FER, MGG and all of these sources combined (ALL). σV_T is calculated for each source, plus A_{V_T} for the combined case.

the differences between the SOI and the bulk FinFETs in terms of impact of the variability sources.

Figure 7.10 presents the histograms of threshold voltage for the SOI FinFETs subject to the individual and combined influence of RDD, GER, FER and MGG. The results of the control bulk device are also presented here for comparison. The SOI FinFET has less RDD induced statistical variability compared to bulk counterpart since, in bulk FinFET, random

dopants associated with the stopper doping concentration and its influence on the current flow in the fin introduce additional variability. However, the SOI FinFET is more susceptible to GER and particularly to FER due to the slightly worse short channel effects than its bulk counterpart. As expected, the impacts of MGG on both architectures are the same, and it can be the major source of statistical variability in high- κ /metal gate devices. In respect of the MGG, reducing the grain size or achieving an amorphous gate will be very beneficial.

In respect of the combined sources of statistical variability the two FinFETs have very similar standard deviations of the threshold voltage of 20 and 19 mV for the SOI and the bulk FinFETs, respectively. This translates in matching factors of $A_{VT} = 1.22$ and 1.14 mV. μm , respectively, where $A_{VT} = \sigma_{\Delta V_T} \sqrt{WL} = \sqrt{2} \sigma_{V_T} \sqrt{WL}$ and where W in this case is the effective fin width, $W = 2H_F + W_F$. The SOI A_{VT} factor performance agrees well with the value reported in References 12 and 30. The very similar A_{VT} factors of the SOI FinFET compared to its bulk counterpart indicate that the introduction of SOI architecture would not bring an additional statistical variability penalty compared to the bulk FinFET with the best possible RDD performance. In reality, the bulk FinFET can have larger process variation associated with the fin formation that will require higher channel doping to counteract the short channel effect degradation. Under these circumstances the A_{VT} factor can be around 1.8 mV. μm^{30} in the bulk FinFET, and the SOI FinFET will have a much better overall variability performance.

7.5 Summary

In this chapter we evaluate the normal and statistical performance of SOI FinFET through 3D ‘atomistic’ simulation for sub-20 nm technology nodes. The bulk devices with the same fin configurations are used as the control devices in this study. Our study indicates that for a trigate FinFET, following the normal design practice, the SOI FinFET can introduce more than 6% performance and $I_{\text{on}}/I_{\text{off}}$ ratio advantage compared to bulk FinFET, or can provide more than two times reduction in leakage current at the same drive current. This is thanks to the BOX isolation compared to the junction isolation depleting the bottom part of the bulk fin. For a DG FinFET, the advantage of SOI FinFET over its bulk counterpart will be more pronounced: over 10% improvement on drive current and $I_{\text{on}}/I_{\text{off}}$ ratio can be expected in SOI architecture for devices with the same leakage current, and more than five times reduction of leakage current in SOI can be achieved if both devices have the same drive current. Although SOI FinFETs have slightly worse short channel effects compared to bulk FinFETs, to some extent it can be mitigated by BOX and substrate doping optimization. SOI technology can efficiently help to reduce the process-induced FinFET variability.

In SOI FinFETs, there is no obvious degradation on statistical variability performance compared to bulk FinFETs that have the best possible RDD performance. Considering the larger process variation associated with the fin formation in bulk technology, the SOI FinFETs can have better overall variability performance compared to bulk FinFETs.

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Understanding variability in complementary metal oxide semiconductor (CMOS) devices manufactured using silicon-on-insulator (SOI) technology

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Abstract: Statistical variability in ultra-scaled CMOS devices is a major challenge faced by the semiconductor industry today. It has critical impact on functionality and yield, particularly of static random access memory (SRAM) circuits. This chapter focuses on the physical origins of statistical variability and their manifestation in fully depleted (FD) thin-body silicon-on-insulator (TB-SOI) transistors. We first review the major sources of statistical variability in CMOS devices. Then, the unique impact of statistical variability on TB-SOI technology is presented, drawing comparisons with conventional, bulk metal oxide semiconductor field effect transistor (MOSFET). Finally, based on a comparison study between TB-SOI and double gate technologies, the statistical aspects of reliability are discussed.

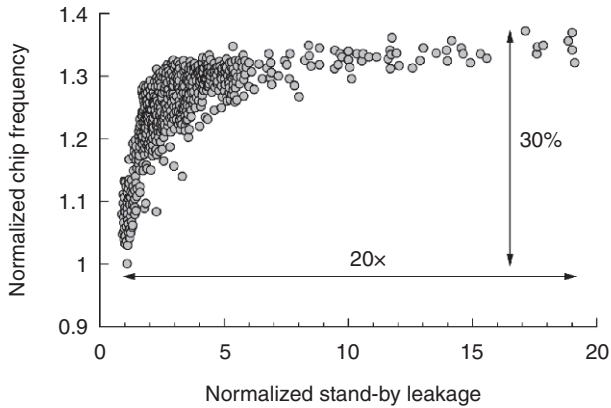
Key words: statistical variability, random dopant fluctuations, metal gate granularity, line edge roughness, CMOS.

8.1 Introduction

This section presents a background overview on device variability, statistical variability sources and measurement of device statistical variability.

8.1.1 Overview of device variability

Device variability is the dispersion of the electrical characteristics of identically designed transistors. It has emerged as one of the most significant challenges to continuous device scaling, because the tolerance in the electrical characteristics of devices cannot be easily scaled in proportion to the



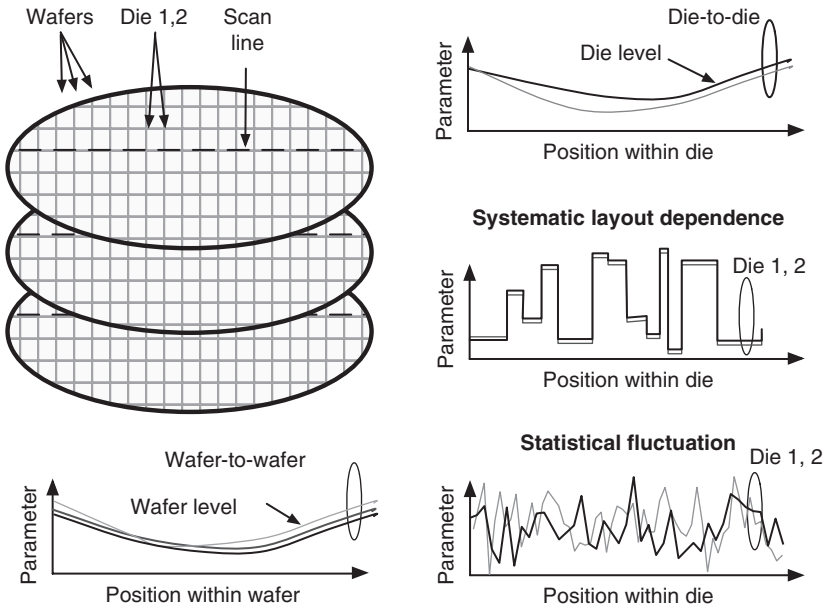
8.1 Scatter plot between chip frequency and stand-by leakage based on data from Reference 1.

nominal values of the electrical parameters, which implies variability in the delay and leakage power of circuits and systems, as seen in Fig. 8.1.¹

Variability stems from two simple facts. First, the fast approach of critical device and interconnect dimensions at the nanometre scale requires atomic level precision in their processing, and that is extremely challenging to maintain, if possible at all, by mass production fabrication facilities. Second, certain aspects of silicon technology and metal oxide semiconductor field effect transistor (MOSFET) design imply the existence of uncontrollable, intrinsic fluctuations in a number of microscopic features in devices with otherwise equivalent macroscopic parameters (i.e., geometry and layout).

Device variability can be classified according to the causes that affect parameter fluctuations. A clear illustration and differentiation between the different components of CMOS variability is presented in Fig. 8.2.² The old fashioned, 'slow' wafer to wafer, within wafer and within die process variability has been with the semiconductor industry since its beginning. It is related to inaccuracy in the control of process parameters and non-uniformity of equipment and results in slow variation of device dimensions, layer thicknesses and doping concentrations (and the corresponding electrical parameters) across the wafer, from wafer to wafer, and from lot to lot.

The systematic layout-dependent variability grew in importance somewhere around the 90 nm technology generations. It is partially related to the fact that 193 nm lithography is still surprisingly used to print sub-50 nm features today. Even with phase shift and optical proximity corrections (OPC), deviations of the real device geometry from the ideal rectangular



8.2 Schematic illustration of different types of variability according to the classification in Reference 2.

shapes that the designers have in their minds when laying out their transistors are still introduced. The introduction of strain to enhance the device performance for the 90 nm technology generation made things worse from a variability point of view. The performance of devices with identical geometry now varies not only because of the lithography-related geometry variations but also because of layout-determined strain variation. This variation in strain can be due to different spacing between the devices, different distances to the shallow trench isolation and different numbers and position of contacts. However, both the shape of the individual devices after the OPC and the impact of layout induced strain variations can be simulated and accurately predicted and therefore they belong to the type of deterministic, or systematic, variability.

However, in addition to the systematic variability there is a rapidly increasing statistical variability, arising from the fundamental atomicity of charge and matter in the transistors, and the only way to tackle statistical variability is to widen the design margins. In this chapter we focus on statistical variability, since SOI technology exhibits some very different properties in this respect, compared to standard bulk technology. In particular, the good electrostatic control – even at very low channel

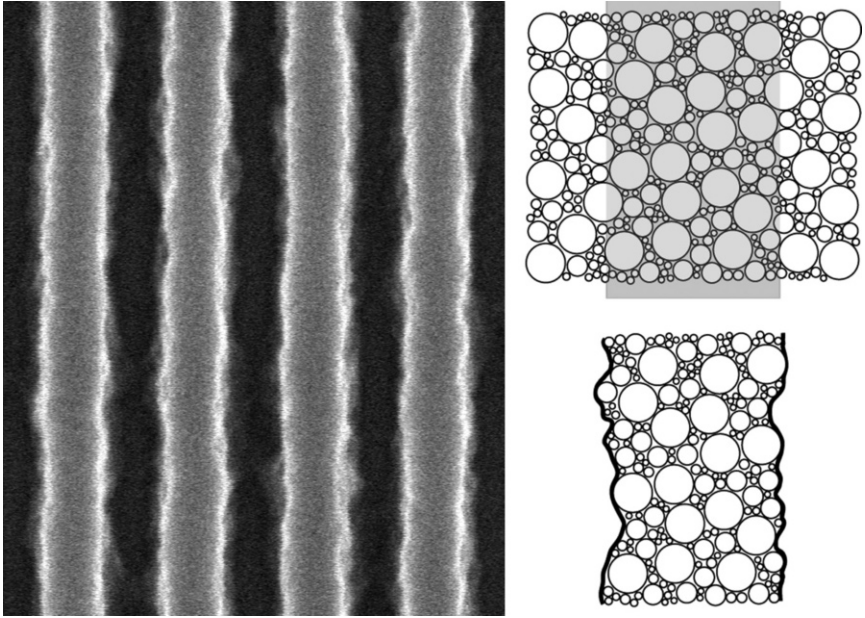
doping – successfully mitigates the variations induced by random dopant fluctuations.

8.1.2 Sources of statistical variability

The statistical variability in modern CMOS transistors is introduced by the inevitable discreteness of charge and matter, the atomic scale non-uniformity of the interfaces and the granularity of the materials used in the fabrication of integrated circuits. The granularity introduces significant variability when the characteristic size of the grains and irregularities become comparable to the transistor dimensions. Random dopant fluctuation (RDF)³ is one of the principle sources of intrinsic variability, which are the different number and spatial configuration of discrete doping atoms introduced by ion implantation and redistribution during high temperature annealing. Plate IV (see colour section between pages 202 and 203) illustrates an example dopant distribution in bulk-type MOSFET of 18 nm gate length, obtained with the help of an atomistic process simulator. The deviation of the gate edge from straight line during lithography process introduces line edge roughness (LER), as shown in Fig. 8.3. The LER limit of 193 nm lithography is of approximately 5 nm,⁴ which is mainly determined by the polymer chemistry, as schematically illustrated in Fig. 8.3. The introduction of high- κ /metal gate technology improves the random discrete dopants (RDD)-induced variability, which is inversely proportional to the equivalent oxide thickness (EOT). However, as schematically illustrated in Fig. 8.4, metal gate granularity (MGG) introduced by crystallization of metal gate material during high temperature annealing leads to variation in the work-function of the crystal grains in the metal gate,⁵ which becomes one of the major variability sources in metal-gate-first technology.

These three sources of variability are the principle ones responsible for the large fluctuation of threshold voltage in scaled bulk-MOSFETs. They act in SOI MOSFETs as well. However, the fluctuation in Si thickness is a SOI-specific source of variability. In extremely scaled transistors, atomic scale body thickness variations can become an important source of statistical variability.⁶

On top of statistical variability, problems related to statistical aspects of reliability are looming that will reduce the life-span of contemporary circuits from tens of years to 1–2 years or even less, in the near future. The statistical nature of discrete trapped charges on defect states at the interface or in the gate oxide associated with hot electron degradation and negative/positive bias temperature instability (NBTI/PBTI) and hot carrier injection (HCI) can result in relatively rare but anomalously large transistor parameter changes, leading to loss of performance or circuit failure.⁷ The statistical aspect of reliability is discussed in detail in Section 8.3.



8.3 Top-down scanning electron microscope image of narrow lithographic lines with the white traces indicating fluctuations in the line edge. The inset to the right illustrates conceptually how line edge roughness arises from the polymer aggregates in the negative photoresist after removing the unexposed (unshaded) part.

8.1.3 A note on methodology

Experimental studies of statistical variability typically involve measurements done on ensembles of paired transistors, each pair consisting of macroscopically identical transistors located next to each other. Thus, if one measures threshold voltage (V_{TH}) of each transistor in a pair, $V_{\text{TH},a}$ and $V_{\text{TH},b}$, one can obtain the statistical component of the variation, reflected in the difference $\Delta V_{\text{TH}} = V_{\text{TH},a} - V_{\text{TH},b}$, assuming that the systematic component is common to both devices, and therefore cancels out.⁸ An alternative way to isolate the statistical aspect of V_{TH} variation is to perform two consecutive measurements on the same transistor but reversing the source and drain contacts (e.g., by source/drain commutation) after the first measurement.⁹ Experiments without source/drain commutation, done on very large ensembles of specially designed transistor arrays with circuits that allow individual transistors to be accessed are also possible.¹⁰ Special care must be taken to minimize systematic variations (i.e., mature technology and a special layout are used) in such studies.¹¹

Regardless of the measurement approach, experimental observations reflect the simultaneous impact of all sources of statistical variability.

Simulations, on the other hand, enable the study of individual sources of variability, as well as combinations thereof. Thus, it is possible to trace the fluctuations of a given electrical parameter directly to the physical origins, and to establish the relevance of each source of variability.

The exposition in this chapter is centred around the three-dimensional, physical level device simulations with the commercial simulator GARAND, based on the drift-diffusion approach.¹² Quantum effects are accounted for through the density gradient approximation applied for holes and electrons.¹³ This is a computationally very efficient yet accurate framework for investigating large ensembles of nanoscale MOSFETs, providing a consistent treatment of confinement effects in the inversion layer, and in the Coulomb potential of the ionized impurities.¹⁴

The investigated FD-SOI device is a low-power n-channel template MOSFET designed by the PULLNANO consortium, with a 32 nm physical gate length (L_G) and a TiN/HfO₂/SiO₂ gate stack with an effective oxide thickness (EOT) of 1.2 nm.¹⁵ The thicknesses of the silicon body, buried oxide (BOX) and spacers are 7, 20 and 10 nm, respectively. Unless explicitly stated, V_{TH} is defined via 1 $\mu\text{A}/\mu\text{m}$ current criterion, hence saturation V_{TH} is ~ 0.3 V and $W_G/L_G = 32$ nm/32 nm.

8.2 Statistical variability in planar fully depleted SOI devices

In this section, using 32 nm gate length thin-body silicon-on-insulator (TB-SOI) device as an example, the unique impact of statistical variability on TB-SOI technology are presented, drawing where necessary comparison with conventional bulk-MOSFETs.

8.2.1 Qualitative insight from modelling and simulation

In this section we systematically compare the impact of RDF, LER and MGG on V_{TH} , I_{ON} and drain induced barrier lowering (DIBL). In order to anticipate and understand that impact, we first look at the microscopic effects inside a device, due to each source of variability. In Plate V we illustrate the conduction band landscape and the electron distribution in the body of an FD-SOI transistor with a fixed dopant configuration owing to RDF and LER. The two images differ with respect to the presence of MGG, only in Plate Vb. Transparency below $3.2 \times 10^{17} \text{ cm}^{-3}$ reveals the shape of an iso-electron surface at this density in the channel, which helps explain the interplay of the different sources of variability.

First, looking at the RDF-induced local fluctuations in the electron potential, for example Plate Va, it is clear that the potential barrier in the channel is smooth, except for a single peak caused by a spurious acceptor. At

an acceptor concentration in the order of 10^{15} cm^{-3} , as used in the simulations, a spurious acceptor in the channel occurs once every few hundred devices. Therefore, RDF-induced V_{TH} fluctuations are well suppressed.¹⁶ However, the potential fluctuations due to donors in the source and drain extensions (S/D-RDF) lead to large fluctuations in the source/drain access resistance and translate to an increase in the on-current variability, as has been recently shown theoretically and experimentally.^{17,18} Additionally, the S/D-RDF implies a local modulation of the channel length, and therefore one may expect RDF to impact DIBL fluctuations too.

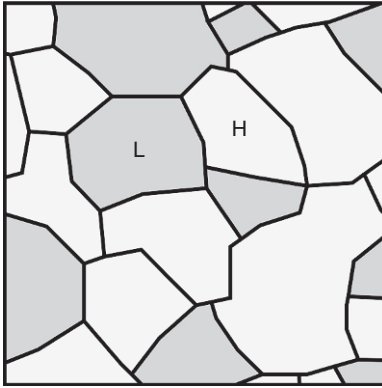
Next, we consider LER: still in Plate Va, the smoothness of the potential landscape is not affected but there is a variation in the height of the barrier across the width of the transistor. Therefore, LER principally affects the DIBL of the device, through a local variation in the channel length. It is worth noting that the variation of the gate edge position induced by LER has a much larger length scale compared to the local modulation in the effective channel length due to the distribution of S/D-RDF. Therefore the impact of LER on DIBL should be much more pronounced.

In the presence of MGG (see Plate Vb) the particular grain pattern can readily be discerned via its imprint on the potential landscape in the channel of the transistor. In particular, a grain with a higher work-function blocks the formation of a channel under the gate, whereas a grain with a lower work-function leads to the formation of a channel underneath, well before the nominal threshold condition for a uniform device (compare Plate Va and Vb). Although in the simulations the average grain area is ~ 25 times smaller than the gate area, the statistical distribution in size and arrangement of the grains implies that a relatively large area of the gate is influenced by one or the other value of gate work-function. We also observe that the potential fluctuations affect the free carrier distribution in the entire depth of the Si-body of the transistor, due to the body being so thin (7 nm). Note that in the given metal grain configuration, the effect of the spurious acceptor is reduced since grains with the lower work-function surround it inducing more electrons relative to the case with uniform gate (Plate Va). Therefore, it is reasonable to expect both V_{TH} and I_{on} to be strongly affected by MGG.

8.2.2 Evidence of high immunity to statistical variability

The most common metrics for the evaluation of statistical variability in a technology are the standard deviation of the threshold voltage, σV_{TH} , and the mismatch coefficient, A_{VT} ,^{8,19} with the following relationship between them:

$$A_{\text{VT}} = (\sigma V_{\text{TH}} \sqrt{2})(WL)^{0.5} [\text{mV} \cdot \mu\text{m}].$$



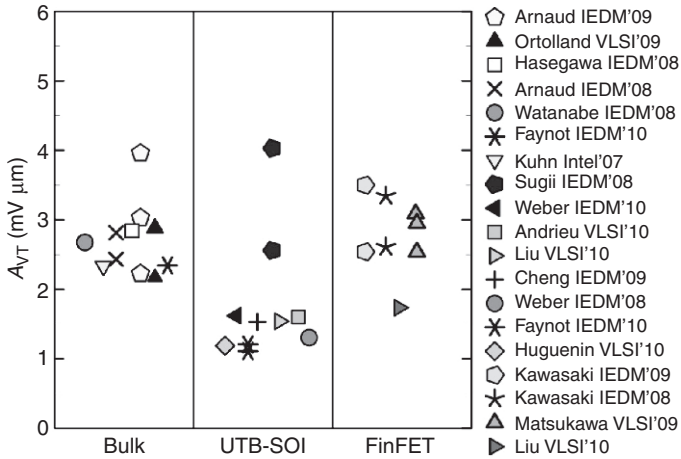
8.4 Illustration of metal gate granularity for a metal with two predominant grain orientations, depicted by colour (shade of grey). The H and L labels mean high and low work-function, respectively.

where W and L are the effective width and length of the gate, respectively. Although another mismatch coefficient, B_{VT} , has been introduced to more objectively compare different bulk-MOSFET technologies,²⁰ A_{VT} remains the principle metric for comparing the variability between different device architectures, for example, planar bulk devices *vs* fully depleted SOI *vs* FinFETs.

Figure 8.5 compiles published A_{VT} factors and provides evidence of superior transistor matching in FD-SOI technology, delivering the smallest A_{VT} in the order of $1.1 \text{ mV } \mu\text{m}$. All reported values are obtained from measurements of paired transistors with high- κ /metal gate stack and aggressively scaled effective oxide thickness.^{21–24,38} The smallest A_{VT} reflects the lowest sensitivity of V_{TH} to the different sources of statistical variability. The clear separation of the ranges of V_{TH} corresponding to planar bulk, ultra-thin body (UTB) FD-SOI and FinFETs indicates strong dependence of the V_{TH} -sensitivity on device architecture.

It is well established now that the superior V_{TH} -matching characteristics of planar FD-SOI devices with respect to planar bulk-MOSFETs are caused by the very low doping in the channel,¹⁶ translating into low RDF-induced fluctuations in V_{TH} . Due to the ultra-thin body and relatively thin BOX of the reported FD-SOI devices, they show good V_{TH} -roll-off characteristics, so that the LER-induced variability does not offset the advantage of low body doping.^{23,25} Minimizing DIBL is of crucial importance in this respect, and it has been demonstrated that the specific design and implantation techniques used in ultra-thin body transistors directly influence both DIBL and V_{TH} variability.^{23,25,39}

It should be noted that all SOI device data in Fig. 8.5 relates to transistors manufactured using gate first technology, meaning there were conditions



8.5 Comparison of published mismatch coefficients A_{VT} for planar bulk, planar SOI and FinFETs, with high- κ /metal gate stack. Data, in the order of appearance in the legend, is from References 21–37.

favouring crystallization of the metal gate during the high temperature anneal for implant activation.⁴⁰ Therefore the associated work-function variability affects V_{TH} in both architectures – bulk and FD-SOI. A relatively small difference in A_{VT} between FD-SOI devices with high- κ /metal gate and SiON/poly-Si gate has been observed.²⁵ However the residual variability is higher than that which can be expected from RDF and LER, and is attributed mainly to metal gate work-function variability after analysis of the temperature dependence of σV_{TH} .²³ Three-dimensional physical level device modelling and simulations corroborate the latter results, showing an A_{VT} around 1.15 mV.μm in the presence of MGG.¹⁷ Simulations are based on a device similar to experiment,²¹ with a 32 nm physical gate length and a TiN metal gate, assuming 5 nm average grain-size as experimentally observed for a TiN gate.⁴¹ On the other hand, the simulated variability due to RDF and LER on their own amounts to an A_{VT} below 0.7. Thus, the entire benefits of fully depleted devices can be realized only by adopting a technology that eliminates gate work-function variability.^{26,41–43}

Presently, sources of variability, stemming from microscopic non-uniformities in the gate dielectric stack, for example, oxide interface roughness, fluctuations in the dielectric constant of high- κ dielectrics, etc., are believed to have a relatively small impact and have not been systematically studied for SOI technology.^{5,14,16,23,44}

However, the variation in the thickness of the body T_{Si} has been a prime concern, specific to UTB FD-SOI transistors. A very tight criterion of ± 5 Å has been established for the maximum tolerable peak-to-peak fluctuation in T_{Si} , to maintain low V_{TH} variability.⁴⁵ Present day SOI wafer manufacturing

technologies already demonstrate the route to an excellent control of T_{Si} within this desired range.⁴⁶ Still, it should be kept in mind that the SOI wafer is subsequently thinned during the device processing steps, to obtain the target sub-10 nm body thickness. This may, in principle, change the T_{Si} -fluctuation patterns and their correlation, introducing a statistical component on a smaller length scale, leading to enhanced statistical variability in devices. Recently, it was experimentally established that σT_{Si} -induced V_{TH} variation is not random and does not scale down with area appreciably, yet it is amenable to process optimization.⁴⁷ Importantly, the resulting contribution to σV_{TH} appears to strongly depend on transistor spacing, and does not affect SRAM transistor matching (the smallest and most densely laid out transistors).

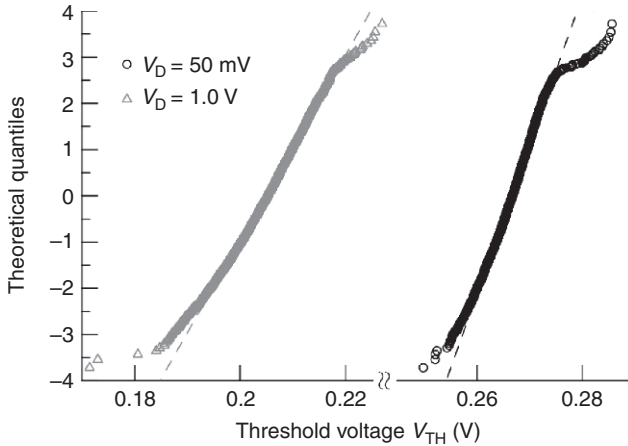
It is also important to mention that A_{VT} factors reported for FD-SOI devices appear to be independent of the level of strain induced on the channel,²³ implying that strain can be used as a performance booster in SOI, without impacting its variability performance.

Finally, it is worthwhile remembering that the usefulness of A_{VT} for comparing transistor matching properties between technologies relies on the assumption that local perturbations self-average in a way that leads to a σV_{TH} being inversely proportional to the square root of the effective gate area $(\text{WL})^{-1/2}$. Such a relation is known to hold true for bulk-MOSFET technology at fixed gate length in the presence of halo doping, on account of the dominant influence of RDF in the channel.^{48,49} Its validity may be questionable in the case of fully depleted SOI transistors, where line edge roughness and work-function variability are the main sources of V_{TH} fluctuation, but there are no detailed systematic studies to elucidate. Moreover, Pelgrom plots (i.e., $\sigma \Delta V_{\text{TH}}$ vs $(\text{WL})^{-1/2}$) are commonly reported, and the fact that the line-fit over the experimental points typically intercepts the origin for FD-SOI transistors as well as for bulk (which it should, if in the limit of very large area the statistical fluctuations self-average completely) supports the above assumption.

8.2.3 Threshold voltage distribution

The comparison of σV_{TH} and A_{VT} made so far illustrates the principle advantage of FD-SOI devices over their bulk-technology counterparts. However, σV_{TH} and A_{VT} on their own do not give a complete picture of the variability-related phenomena in FD-SOI devices. The distributions of V_{TH} in large ensembles provide additional information about the significance of different sources of variability. Such information is also necessary for the extraction and generation of parameters for statistical compact models and the subsequent statistical circuit simulations.¹⁸

Figure 8.6 shows the distributions of linear and saturation threshold voltages, effected by RDF, in an ensemble of 10 000 transistors based on the FD-SOI macroscopic template described in the previous section. Note the



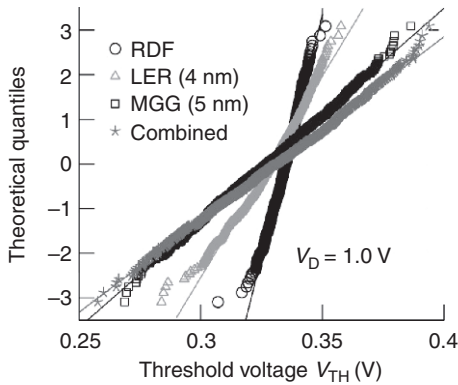
8.6 Normal probability quantiles to quantiles plot (QQ-plot) of the linear and saturation threshold voltage distributions, in an ensemble of 10 000 FD-SOI transistors. Here, the current criterion of V_{TH} is defined as ~ 30 nA/ μm to guarantee sub- V_{TH} operation for all devices.

marked departure from Gaussian distribution for a deviation beyond 2.5σ . Such tails will affect SRAM design, where devices whose parameters fall outside the $\pm 3\sigma$ range constitute a very significant fraction of chips with transistor integration density of $\sim 10^9$.

The upper tail in the distribution (positive σ), showing a higher probability of large V_{TH} values than that corresponding to a Gaussian distribution, is due to a spurious acceptor atom appearing in the channel of the transistor, as illustrated earlier in Plate Va. The tailing is less pronounced at high drain bias ($V_D = 1.0$ V) since, for devices with an acceptor atom near the drain, the effect of this atom on the electron density, and on the electrostatic potential, is mitigated by the drain depletion region. Hence, the upper tail in the distribution at high V_D is populated with devices with an acceptor nearer to the source. The lower tail (negative σ), also with a relatively higher probability than a Gaussian distribution, is due to DIBL in devices with smaller effective gate length as defined by source/drain-RDF (SD-RDF). Recall that DIBL is exponentially magnified in the electron density, hence in the sub- V_{TH} current.

Although σV_{TH} is small (3 mV/5 mV linear/saturation), it does not describe well the RDF-induced V_{TH} fluctuations because of the sharp departure from normality, and may be misleading. In particular, the observed V_{TH} span corresponds to a 40% larger σV_{TH} in both cases (4.4 mV/7 mV linear/saturation). This is not negligible in comparison to the σV_{TH} of 26 mV (A_{VT} of 1.1), discussed in relation to Fig. 8.5.

Figure 8.7 compares the isolated effect of RDF, LER and MGG on the distribution of saturation, V_{TH} , as well as their combined effect, in the absence of



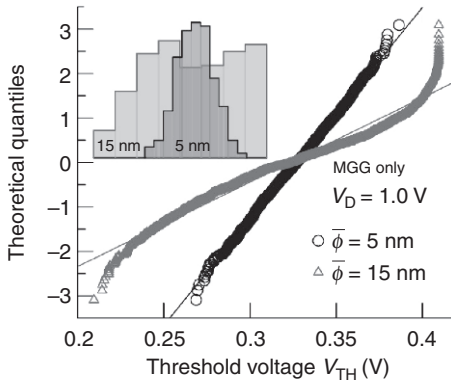
8.7 Normal probability QQ-plot of V_{TH} distribution due to the combined effect of RDF, LER and MGG density, as indicated.

interface-trapped charges (i.e., fresh devices). Ensemble size is 1000 in this case. It is clear from Fig. 8.7 that, overall, the variability in FD-SOI device is determined by the work-function fluctuations due to MGG ($\sigma V_{TH} = 24$ mV). In the absence of MGG, the dominant factor is LER ($\sigma V_{TH} = 11$ mV). In comparison, the RDF distribution appears compressed owing to the smallest σV_{TH} .

Considering the tails of the distributions in Fig. 8.7, note that due to the smaller ensemble size, these are less elaborated than in Fig. 8.6. However, all distributions indicate some tailing, albeit in opposing directions, which requires some consideration. The lower tail in the ensemble with LER has a very similar character to the RDF-induced distribution, owing to DIBL effects. The higher tail of the LER-induced dispersion is of lower probability than a Gaussian distribution, suggesting that the shortest percolation path dominates the sub- V_{TH} current. MGG on the other hand leads to a bound distribution of V_{TH} .^{44,50} This is best understood from Fig. 8.8, showing the V_{TH} dispersion arising from MGG only, but for two different average grain-size diameters: 5 and 15 nm. The upper tail is more pronounced, corresponding to the higher occurrence probability of the grain with larger work-function (WF). The lower tails of the MGG-induced distribution are in the opposite direction, compared to RDF and LER. Not surprisingly, the combined effect of the three sources brings the V_{TH} distribution closer to normality, as seen in Fig. 8.6, except for the upper tail, where the combined effect of MGG and LER appears stronger than that of RDF.

8.2.4 Influence of RDF beyond V_{TH} variability

To elucidate on the difference between bulk and FD-SOI in terms of statistical variability, here we perform a comparison between an FD-SOI device and a controlled case study in bulk technology, featuring the same physical

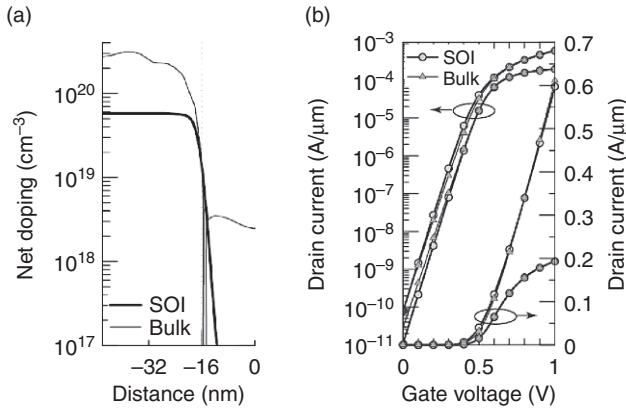


8.8 Normal probability QQ-plot of V_{TH} distributions due to MGG for two average grain diameters, with histograms in inset.

gate length, L_G , and effective oxide thickness (EOT) and nearly identical performance.

The donor-concentration profile of the FD-SOI template transistor is compared to the net-doping concentration of the bulk-technology MOSFET in Fig. 8.9a. The nominal transfer characteristics of the devices are compared in Fig. 8.9b. Note that the simulations of the bulk-MOSFET are subject to the following approximations: (1) in order to achieve transconductance similar to that of the SOI transistor, mobility degradation due to acceptors in the channel is not considered, and the dependence of mobility on perpendicular field is normalized to give the same degradation as in the SOI transistor (which exhibits roughly three-times lower perpendicular field); (2) to achieve the same source/drain resistance (R_{SD}), bulk mobility in the S/D regions is explicitly lowered, compensating for the higher donor concentration.

There is an additional problem in using σV_{TH} as a sole metric to predict the impact of RDF on FD-SOI-based circuits. The problem is caused by the increased I_{ON} variability due to S/D-RDF. This is most clearly suggested by the shape of the transfer characteristics of 1000 FD-SOI devices, shown in Fig. 8.10. There is a well pronounced flaring of the set of I–V curves as the gate voltage (V_G) approaches 1.0 V, despite the tight packing of the set for V_G below the point of maximum linear transconductance (G_m) (around 0.6 V). This effect may appear unexpected at first glance, since simulations within the draft-diffusion (DD) framework do not capture transport variability, and the dispersion of the I–V curves is typically the same for V_G above V_{TH} . Figure 8.10 also shows the transfer characteristics of the 1000-device ensemble of bulk-MOSFETs, simulated under the specific assumptions stated in the above paragraph. The notable curve-crossing, most evident at low V_D , and the broad I–V dispersion suggest strong decorrelation between I_{ON} and V_{TH} in this case, as confirmed in Fig. 8.11a. A meaningful figure of merit for

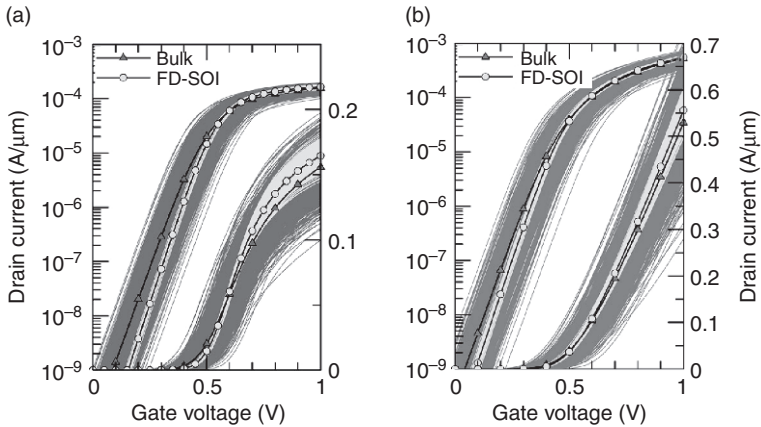


8.9 (a) Net-doping profile and (b) transfer characteristics (at 50 mV and 1 V drain biases) of the FD-SOI and bulk template devices simulated in this work.

comparison between the FD-SOI and the controlled bulk scenarios is the ratio of normalized variability, defined as $\alpha = (\sigma I_{ON}/\langle I_{ON} \rangle)/(\sigma V_{TH}/\langle V_{TH} \rangle)$. For linear/saturation bias α is 5.4/2.2 for FD-SOI and 0.9/1.0 for bulk ensemble.

Following Reference 10, the I_{ON} variability has only three components arising from the corresponding fluctuations in V_{TH} , current-onset voltage and G_m . However, variability in transport is not captured in the present simulations and therefore G_m is expected to have a limited contribution from the variation in effective channel length (due to random distribution of donors under the physical gate edge). Current-onset voltage in the simulations with RDF has negligible variability in agreement with experiments.¹¹ Therefore, the enhanced I_{ON} variability, compared to V_{TH} variability of the FD-SOI ensemble must be due to variation in the access resistance, R_{SD} , (as effected by the random number and distribution of donors under the spacers). This is understandable since at low drain voltage the resistance of the transistor is determined by the source, channel and drain resistances connected in series. The I-V flaring and I_{ON} variability in saturation are weaker, compared to the linear regime, and are mainly due to variations in the source access resistance, causing variations in the effective (intrinsic) gate-source voltage.

For the FD-SOI device our estimate of the access resistance, R_{SD} , (following Reference 51) correlates very strongly to the linear I_{ON} , as shown in Fig. 8.11b. For the bulk-MOSFET the correlation is less clear, since both channel and access resistances vary independently due to channel-RDF and SD-RDF, and affect the I_{ON} at the same time. Therefore, in FD-SOI devices, R_{SD} variation due to SD-RDF is an additional contributor to the I_{ON} variability that has not been previously revealed.



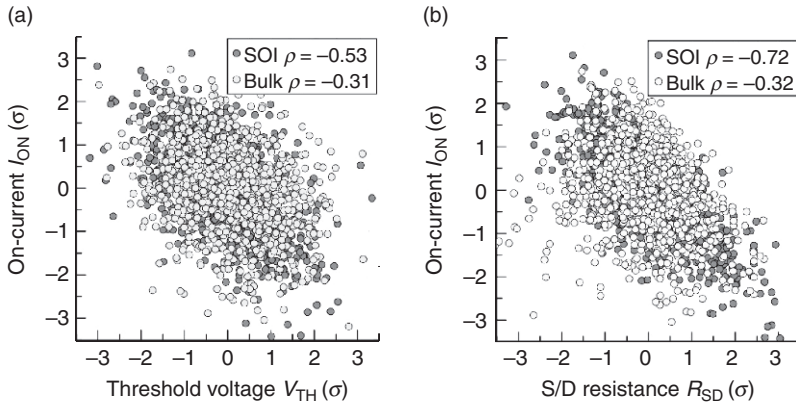
8.10 Linear ($V_D = 50$ mV) (a) and saturation ($V_D = 1$ V) (b) transfer characteristics of an ensemble of 1000 FD-SOI (light) and bulk (dark) devices, subject to RDF.

8.2.5 Architectural vs technological aspects

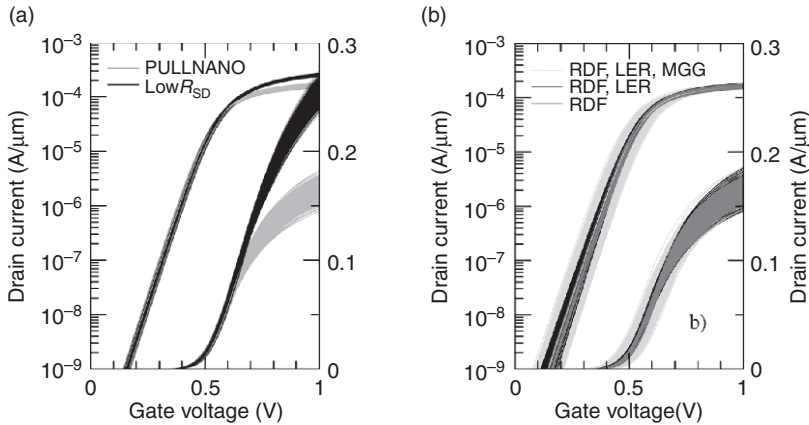
The comparison between FD-SOI and the controlled bulk device suggests the enhanced contribution of R_{SD} variability to the I_{ON} variability is partly architectural. In an FD-SOI MOSFET lacking channel impurities, the RDF-induced V_{TH} fluctuations are minimized, allowing the R_{SD} fluctuations to dominate the I_{ON} variability, especially at low V_D . Indeed, if the acceptor doping in the ‘atomistic’ simulations of a bulk-MOSFET is assumed continuous while donors are discretely resolved, the transfer characteristics of the ensemble (not shown for brevity) are like those of the FD-SOI ensemble. When channel acceptors are discretely resolved, there is a competition between the contributions from σV_{TH} and σR_{SD} to the I_{ON} variability, which is most clearly seen in Fig. 8.11b.

The enhanced contribution of σR_{SD} to σI_{ON} is partly technological too, owing to the difficulties in realizing low access resistance in ultra-thin body devices. Figure 8.12a compares the linear transfer characteristics of the FD-SOI device ensemble discussed earlier (PULLNANO), against an alternative design (Low R_{SD}) with an idealized donor concentration of $2 \times 10^{20} \text{cm}^{-3}$ under the spacer and two times lower R_{SD} ($\sim 100 \Omega \mu\text{m}$). Note that unlike σV_{TH} due to channel-RDF, which grows with the increase of doping concentration, σI_{ON} due to SD-RDF decreases with the increase of concentration.

Figure 8.12b demonstrates that while work-function variation (WFV) remains by far the dominant factor for σV_{TH} , SD-RDF retains its critical influence on the I_{ON} variability even if LER and WFV are also considered. Simulations with WFV assume 5 nm average grain diameter; TiN-type



8.11 Scatter plots of linear I_{ON} vs linear V_{TH} (a) and R_{SD} (b), normalized to standard score $(X-\mu)/\sigma$. I_{ON} - V_{TH} correlation in saturation (not shown) is 0.77/0.69 for FD-SOI/bulk. $\langle R_{SD} \rangle$ is 200 $\Omega\mu\text{m}$. ρ is the Spearman correlation coefficient, which is less sensitive to outliers in the distributions.



8.12 Technological aspects of the impact of SD-RDF on I_{ON} variability. Effect of R_{SD} reduction by a factor of two (a), and effect of additional sources of variability (b). V_D is 50 mV in both cases.

granularity with 0.2 V WF difference between two possible grains; and 60% occurrence probability for the grain with higher WF.⁴¹ LER assumes 3σ of 4 nm.²³ As mentioned, σV_{TH} in the combined case is 26 mV but only 3 mV for the RDF-ensemble. However, I_{ON} variability is due almost entirely to SD-RDF in all cases shown in Fig. 8.12b. For the RDF-ensemble and for the ensemble of RDF, LER and MGG, σI_{ON} is 5.6 and 6.0 A/ μm , respectively. V_{TH} and I_{ON} at low V_D are strongly decorrelated ($\rho = 0.2$) due to the

large influence of WFV on V_{TH} . In contrast, correlation is high ($\rho = 0.82$) in saturation. Finally, the figure of merit, α , is greatly reduced, from 5.4(2.2) to 0.6(0.7) for linear(saturation) bias, when the combined effect of variability sources is considered.

8.3 Statistical aspects of reliability

In this section, using 32 nm gate length TB-SOI device as an example, the statistical aspects of impact of bias temperature instability (BTI) on TB-SOI technology are presented, followed by a comparison study between TB-SOI and double gate (DG) technologies on BTI reliability.

8.3.1 Impact of bias temperature instability on statistical variability

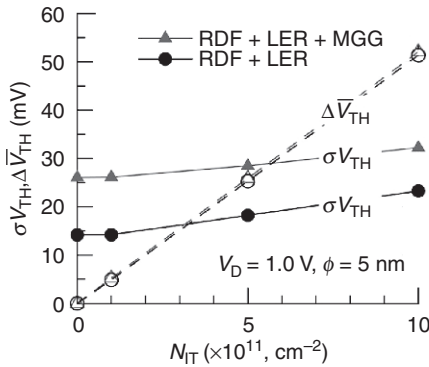
Device reliability is a major concern in ultra-scaled technologies. The degradation of gate oxide has the greatest impact, manifested in the time-dependent drift of the electrical parameters. This drift, for example the increase in V_{TH} along the device lifetime, originates from the increase of the number of charges trapped in the gate oxide.^{52–57} The gradual degradation of the oxide worsens the statistical variability as it augments the device mismatch in a time-dependent fashion.^{58–61} Moreover, statistical variability itself affects the oxide degradation phenomenon, making the projection of reliability and the establishment of appropriate design margins at circuit/system level ever more difficult.^{58–60} Unfortunately, the interplay between statistical variability (SV) and reliability is not yet well understood, nor comprehensively studied, especially for FD-SOI devices.^{60,62,63}

In this section, we consider the impact of positive-bias temperature instability (PBTI) degradation, known to be one of the dominant mechanisms inducing time-dependent variability in n-channel transistors with high- κ /metal gate technologies.⁶⁴ Here, the modelling assumes only interface traps to be involved, with an energy range at or below the Fermi level in the channel, hence all interface trap states will be filled. The sheet density of PBTI-induced interface-trapped charge density, N_{IT} , is determined by the electric/thermal stress pattern and the ageing conditions of the device, as well as by the processing and the material properties of the high- κ /metal gate stack. However, our simulations are frozen in time and consider the variability associated with different levels of N_{IT} . Three levels of N_{IT} equal to 10^{11} , 5×10^{11} , and $1 \times 10^{12} \text{ cm}^{-2}$ are selected to represent the early, intermediate and late degradation stages. For the corresponding ensemble of devices, the actual number of discrete traps in each device differs, enhancing the variability at a given stage of degradation as discussed in the following.

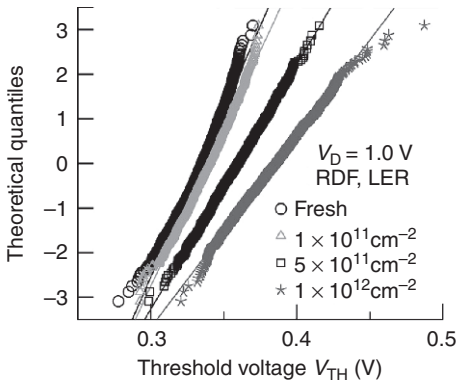
Plate VI shows the effect of interface-trapped charge (ITC) on the conduction band landscape and electron distribution in the channel of the transistor, in the presence of RDF and LER, both (a) without and (b) with MGG. Notably, the electrons trapped at the interface between the Si-body and the gate oxide act in the same way as the spurious ionized acceptor in the channel, repelling inversion electrons and reducing the current – recall Plate Va and Vb. Despite being a surface phenomenon, the interface-trapped charge extends its influence over the depth of the ultra-thin body. Plate VIb illustrates the effect of all four sources of variability. The RDF, LER, MGG patterns used in Plate VI are the same as those in Plate V; also, the same interface traps are modelled in Plate VIa and VIb. Note however, that the addition of interface charges renders substantially different potential landscape and carrier distribution, and in this particular case, completely blocks the channel conductance path. Therefore the combination of sources could markedly enhance (or possibly reduce) the effect of an individual source of variability.

Figure 8.13 reports the standard deviation and mean shift of V_{TH} vs interface-trapped charge density N_{IT} that corresponds to slight, moderate and heavy PBTI degradation. For the simulations including RDF, LER and MGG simultaneously, σV_{TH} is 26 mV for the fresh device (absence of traps), which translates to an A_{VT} of 1.18 mV.µm. Heavy PBTI degradation increases σV_{TH} to 33 mV (A_{VT} of 1.49 mV.µm), and introduces a shift in the mean V_{TH} of 55 mV. These results are in excellent agreement with measurement of similar device structures, showing record low A_{VT} of about 1.1 mV.µm and a PBTI-induced mean shift of approximately 60 mV.^{21,22}

Figure 8.14 shows the normal probability plots of the V_{TH} distribution of the FD-SOI device subject to RDF and LER only, at different levels of degradation, as indicated. The increase of the standard deviation is nearly linear



8.13 Standard deviation, and mean shift of V_{TH} vs interface-trapped charge density N_{IT} for the cases with and without MGG.

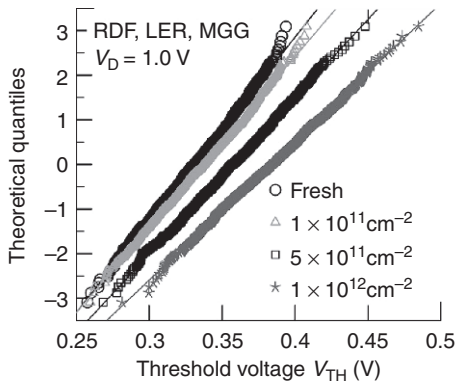


8.14 Normal probability QQ-plot of V_{TH} distributions due to the combined effect of RDF, LER and ITC, at different stages of degradation, as indicated.

with the increase of N_{IT} (refer to Fig. 8.13), and is reflected in the slope of the QQ-plots. There is more than 50% increase in σV_{TH} for a ten-fold increase in N_{IT} . Further, the shape of the distribution is also changing as suggested by the variation in the tails. It is seen that interface-trapped charge exaggerates the random-acceptor-induced upper tail of the V_{TH} distribution, in the limiting case of an amorphous metal. This is anticipated from the discussion in Section 8.2.

Figure 8.15 shows the cumulative V_{TH} distributions of the FD-SOI ensembles with RDF, LER and MGG, at different levels of ITC degradation. Although σV_{TH} is larger, its increase over a ten-fold increase of N_{IT} is only about 25%, since the MGG-induced variability is much larger than that due to trapped charges. Recall from Plate V that MGG affects the potential barrier over a relatively large area, while interface-trapped charges induce relatively localized perturbations in the potential. Additionally, by including the contribution of MGG, we see in Fig. 8.15 that V_{TH} distribution is reasonably close to normal, up to $\pm 3\sigma$, especially for greater N_{IT} , since the tailing of the V_{TH} distribution is in opposing directions for interface traps and for MGG.

The results presented in Figs 8.14 and 8.15 correspond to simulations that include traps only at the gate oxide interface with the Si-body. It could be expected that in a planar, thin body FD-SOI case the PBTI will happen predominantly at the top interface. However, the BOX interface usually does not have the same quality as gate oxide, and a higher intrinsic defect density can be expected at the back interface. Moreover, devices with ultra-thin BOX and back gate control for leakage/performance optimization may suffer additional degradation of the BOX too. Due to a lack of experimental data for the trapped charge density at the BOX interface during the ageing



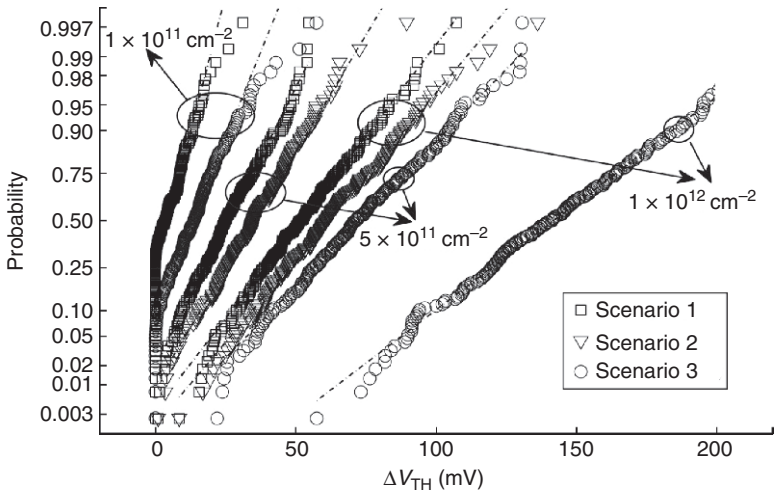
8.15 Normal probability QQ-plot of V_{TH} distribution due to the combined effect of RDF, LER, MGG and ITC, at different stages of degradation as indicated.

process, three scenarios are compared below: scenario 1 assumes that there is no trapped charge at the BOX interface; scenario 2 assumes that during the ageing process, the $N_{IT,BOX}$ (trapped charge density at the body/BOX interface) is 10^{11} cm^{-2} and does not change over time; scenario 3 assumes that $N_{IT,BOX}$ is identical to N_{IT} at the top interface. Figure 8.16 illustrates the distribution of the fractional threshold voltage changes ΔV_{TH} due to trapped charge in the simultaneous presence of RDF and LER for the three scenarios. Although scenario 3 is an extreme setting that may not occur under real operational conditions, Fig. 8.16 illustrates that, for a thin BOX structure, the quality of the BOX interface has a first-order impact on device characteristics due to the charge-coupling.⁴⁸

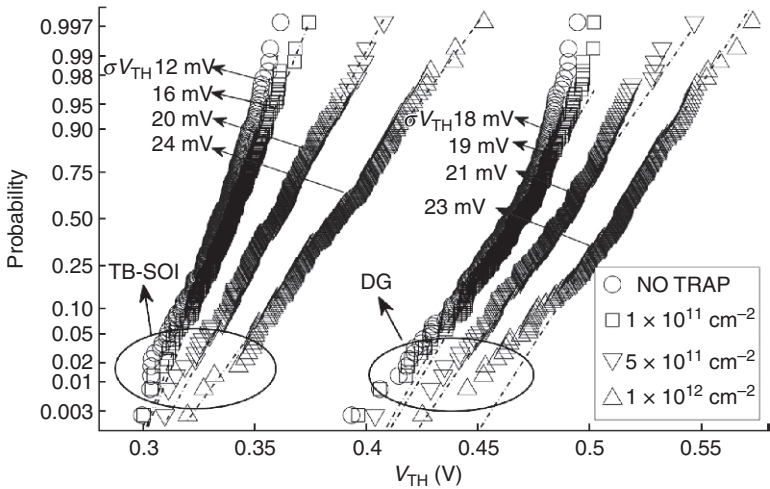
8.3.2 Single gate vs double gate devices

In the rest of this section, we compare the planar FD-SOI device discussed so far, with a fully depleted double gate device, featuring 22 nm physical gate length and 1.1 nm effective oxide thickness. The planar FD-SOI is modelled according to scenario 2 above, that is, $N_{IT,BOX} = 10^{11} \text{ cm}^{-2}$ regardless of N_{IT} , while the DG device has identical average trap density on each interface.

Figure 8.17 illustrates the impact of interface-trapped charge on the threshold voltage distributions of the two templates at V_{DS} of 1 V and different levels of degradation (average N_{IT}). Features of the distribution appear very similar in both technologies, however, it is evident that the dispersion for the TB-SOI device broadens faster than that of the DG device, at the same rate of increase in N_{IT} . This may be somewhat surprising, given that the TB-SOI device should be subject to a larger degree of



8.16 A normal probability plot of the fractional threshold voltage change due to PBTI under three scenarios of charge trapping at the body/BOX interface for the TB-SOI device with RDF, LER and different levels of ITC at the gate oxide-body interface.

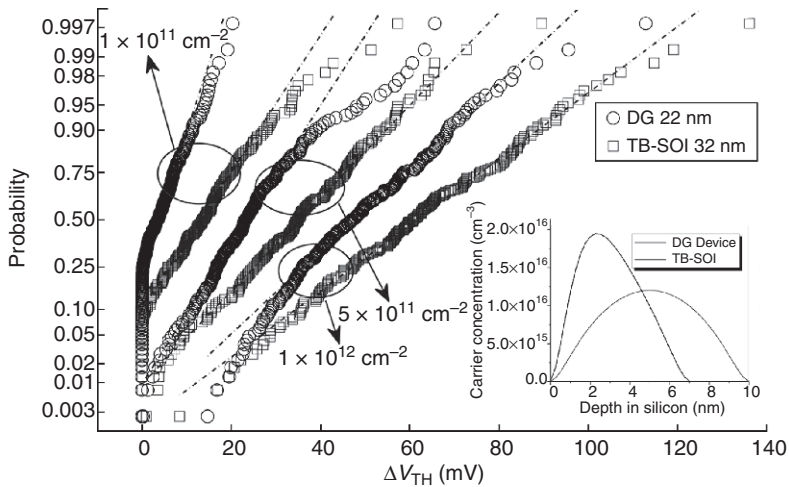


8.17 Normal probability plots of threshold voltage distribution under the influence of combined static sources of statistical variability (RDF and LER), at different levels of degradation, as indicated by the trapped charge density. Comparison is made between TB-SOI and DG MOSFETs.

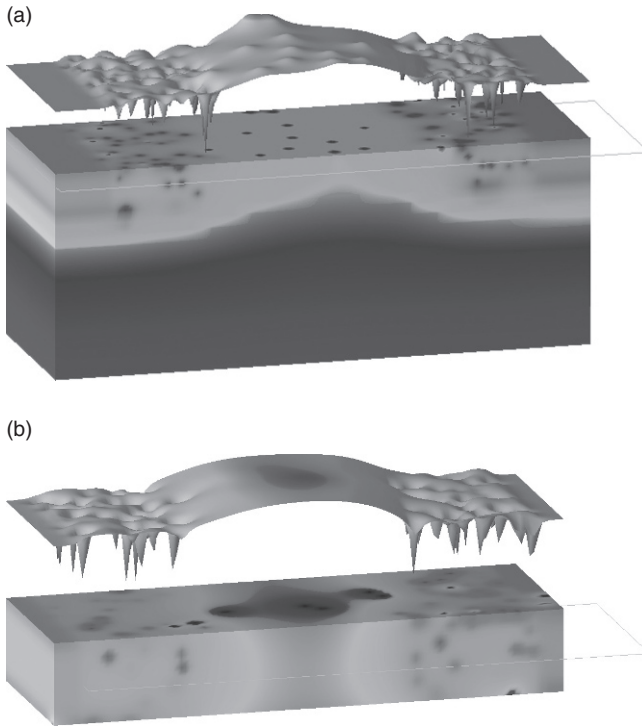
self-averaging, due to the larger gate area. The issue is further emphasized in Fig. 8.18, showing the probability plot of the fractional change of threshold voltage, ΔV_{TH} , corresponding to the cases of Fig. 8.17. Although the single gate transistor has a larger gate area, at each level of degradation the corresponding fractional changes are larger and more widely distributed compared to the DG case. Despite the 60% smaller effective gate area of the DG MOSFET it is clearly less susceptible to PBTI-induced variability.

This phenomenon is understood with the help of the inset in Fig. 8.18, showing the inversion charge distribution between the top and bottom interfaces of the TB-SOI MOSFET and the DG MOSFET. In the DG case, volume inversion occurs and the carriers flow close to the centre of the device where the potential fluctuations introduced by the trapped charges are relatively small. This leads to lower variability compared to the single gate TB-SOI, where the transport occurs close to the top interface. It means, however, that in the DG case the current flow is equally influenced by the trapped charges at both interfaces (effectively doubling the N_{IT}), so there is no reduction in variability due to averaging, as may be the case with two independent channels.

The different magnitude of the potential fluctuations at the position of the dominant current flow for the DG and TB-SOI transistors is illustrated further in Fig. 8.19. The channel potential landscape (the top plot in each device) is visibly smoother in the DG case compared to the TB-SOI case.



8.18 Normal probability plot of the increase of threshold voltage due to PBTI for 32 nm TB-SOI and 22 nm DG devices. Inset: carrier density distribution at threshold voltage.



8.19 Potential profiles of (a) TB-SOI and (b) DG devices with combined RDF and LER at ITC level of $1 \times 10^{12} \text{ cm}^{-2}$. The potential profile slices are cut at a location where maximum carrier density occurs.

8.4 Fin-on-oxide field effect transistors (FinFETs) on SOI

A final word is due in consideration of the recently commercialized FinFET architecture,⁶⁵ which is effectively a trigate transistor and offers a further improvement of the electrostatic integrity over TB-SOI and even DG devices. Although at the point of writing commercial FinFETs utilize junction-isolation technology to isolate the fin-channel from the substrate of the device, FinFETs on SOI substrates are actively being pursued for commercialization by IBM.⁶⁶

Similarly to TB-FD-SOI transistors, the channel of FinFETs on SOI is not intentionally doped. Therefore the V_{TH} values of FinFETs exhibit similar responses to random dopant fluctuations and work-function variations as planar single SOI devices. However, the fluctuation of the width of the fin is a new source of statistical variability, unique to FinFETs (bulk as well as SOI FinFETs). It imparts a V_{TH} variability of similar magnitude to that of the work-function variability.^{27,67} The fin-width directly affects carrier confinement and hence the charge density at a particular cross-section along

the channel of the transistor. Additionally, the quality of the fin-formation, which strongly depends on the type of etching process involved, is of great importance to the on-current variability too. It has been experimentally established that in addition to fluctuations in V_{TH} and R_{SD} , I_{ON} variability in FinFETs on SOI is augmented by transconductance fluctuations arising from non-uniformities of the fin and its surfaces.⁶⁸

Reliability-wise, the volume-inversion effect in the sub-threshold regime makes the FinFET devices exhibit similar responses to BTI degradation as DG MOSFETs with ultra-thin bodies. Therefore, although the quantitative evaluation of variability in FinFETs merits a chapter of its own, the quantitative trends in the statistical variability of FinFETs on SOI can largely be understood from the analysis of planar and double gate UTB-SOI.

8.5 Summary and future trends

In this chapter we focused on the statistical variability in planar FD-SOI transistors, and discussed their similarities and differences from conventional bulk-MOSFETs. Specifically we demonstrated that in FD-SOI the standard deviation of threshold voltage is mostly affected by work-function variability and, in the limiting case of amorphous metal gate, by the line edge roughness of the gate. However the source/drain-RDF has critical impact on the SV of FD-SOI transistors through (1) variation in the short-channel effects affecting the tails of V_{TH} distribution, and (2) variations in the access resistance and increase in σI_{ON} beyond what may be induced from σV_{TH} . SD-RDF dominates I_{ON} variability at low V_D even if WFV and LER are considered, eliminating I_{ON} - V_{TH} correlation. Therefore, the use of σV_{TH} as a sole metric of variability in FD-SOI devices could be grossly misleading and underestimate the impact of RDF on circuits.

In consideration of reliability, the results of the analysis presented thus far indicate that in TB-SOI and DG MOSFETs, PBTI/NBTI degradation can significantly increase the initial ‘virgin’ variability coming from RDD and LER. The effect is much stronger in the 32 nm TB-SOI case with lower initial variability where sheet density of the trapped charge of $1 \times 10^{12} \text{ cm}^{-2}$ results in almost two-fold increase in σV_{TH} . The same amount of trapped charge in the DG case results in less than 30% increase in σV_{TH} . The improvement is related to volume inversion in the DG case, thus highlighting a benefit in the pursuit of architecture with symmetric gates.

While the overall variability performance of SOI devices is better than that of the bulk counterpart transistors, the influence of the different sources of variability must be considered carefully throughout circuit and system design, in view that the variability in the device characteristics can have a direct impact on circuit and system performance and yield. Specifically, the I_{ON} variation at transistor level will introduce timing and performance

variations in digital circuits, while V_{TH} variation will cause an overall increase in leakage power dissipation. Moreover, for SRAM circuits, which deploy the narrowest transistors, statistical variability in V_{TH} and DIBL may lead to a serious degradation of the noise margins of the cell.⁶⁹

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Protecting against electrostatic discharge (ESD) in complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) manufactured using silicon-on-insulator (SOI) technology

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Abstract: This chapter describes key differences of ESD protection in SOI technologies as compared to bulk. It presents active rail clamp based SOI ESD protection network and design methodology including both device and circuit level characterization data. A compact model is introduced to describe the gated diode in the ESD regime. ESD characteristics of FinFETs, FinDiodes and FDSOI devices as likely device candidates for advanced SOI technologies are studied. A response surface method to conveniently optimize ESD device sizes depending on the output buffer configuration is presented. It is demonstrated that distributed and boosted rail clamp SOI ESD networks are very compact and provide an effective ESD protection solution.

Key words: ESD, electrostatic discharge, active rail clamp, response surface, compact model, characterization.

9.1 Introduction

Electrostatic discharge (ESD) has always been an important issue in the semiconductor industry as the source of unexpected destruction of semiconductor devices. ESD is the transfer of electrostatic charge between bodies or surfaces at different electrostatic potential. ESD is a high-current event (1–15 A) with a short duration (1–100 ns). ESD damage to integrated circuits (ICs) can be caused by:

- human handling of chips (human body model – HBM),
- robotic handling in assemblies (machine model – MM) and
- charging of IC packages during automated assemblies and testing followed by discharge to ground (charged device model – CDM).

ESD is a subset of electrical overstress (EOS), which is defined as the exposure of an object to a current or voltage beyond its maximum ratings.

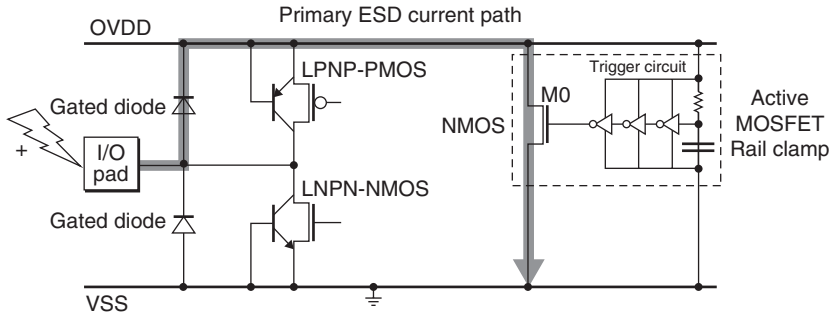
EOS/ESD has been a predominant failure mechanism across all products in many semiconductor companies. Losses due to ESD can occur anywhere from fabrication and test to field. It is estimated (Duvvury, 2003) that ESD causes millions of dollars in real losses each year and an unknown amount of hidden losses each year. It is estimated that 25% of all component failures are due to electrostatic discharge (ESD) and electrical overstress (EOS).

Downscaling of CMOS technologies in the deep sub-micron range made ESD protection an important reliability matter. In order to protect ICs from damage, ESD protection is implemented on-chip together with other input/output (I/O) and core circuits. Building ESD protection circuits within limited space and with minimum impact on normal IC operation is a challenging design task.

ESD protection of CMOS SOI ICs is especially difficult for a number of reasons (Kuo and Lin, 2001; Khazhinsky, 2007). First, since devices are built on the silicon thin film, the ESD techniques based on thick-field oxide devices are not feasible. Second, due to the existence of the buried oxide in SOI, the ESD power consumed by the device cannot dissipate easily, and the ESD SOI devices at a high current have poor performance. Also, because of the buried oxide, large area parasitic diodes, bipolar devices and silicon controlled rectifiers (SCRs) frequently adopted in bulk technology cannot be easily implemented in a standard SOI process. There are a number of other key changes from bulk to SOI that need to be considered when implementing ESD protection (Raha *et al.*, 1997a; Voldman *et al.*, 2000; Juliano and Anderson, 2003; Khazhinsky *et al.*, 2005). Bulk shallow trench isolation (STI) diodes are replaced with gated diodes. All diodes are two terminal devices only – no bipolar junction transistors (BJTs). Parasitic diodes are either very poor or non-existent. Output buffer and clamp MOSFETs may be either body-tied or floating body. Device failure voltage levels are overall lower in SOI compared to bulk.

In this chapter we will follow CMOS ESD protection philosophy that avoids use of traditional avalanche junction triggered ‘snapback’ ESD devices; builds ESD networks using active devices for which the process technology was designed (i.e., MOSFETs, diodes); treats ESD primarily as a circuit design rather than a process/device problem; designs and optimizes all ESD networks just like one designs the rest of the IC, using SPICE (Simulation Program with Integrated Circuit Emphasis); develops and utilizes simple, scalable ESD-specific compact models to describe active devices and interconnects in the short duration, high-current ESD regime.

While some designs rely on bulk-specific ESD devices and have limited use in SOI, there are ESD protection schemes that can be implemented in both bulk and SOI technologies. In particular, ESD protection networks



9.1 Rail-based ESD protection.

comprising forward biased diodes and transient triggered active MOSFET rail clamps have proven effective on advanced CMOS bulk (Worley *et al.*, 1995; Torres *et al.*, 2001; Stockinger *et al.*, 2003, 2005) and SOI (Palumbo and Dugan, 1986; Raha *et al.*, 1997a; Voldman *et al.*, 1999, 2000; Juliano and Anderson, 2003) products (Fig. 9.1).

Key advantages of rail-based ESD protection include:

- the absence of avalanching junctions in primary ESD current path;
- protection is highly process portable, scalable, and easy to simulate with SPICE; ESD risks are for the most part independent of foundry processes;
- it is the most layout area efficient ESD solution (Stockinger *et al.*, 2003);
- ballast resistance is not needed in the output buffers;
- it has least added I/O capacitance of available ESD options (Richier *et al.*, 2000).

Another advantage of these networks is that they can easily be ported from bulk to SOI technologies.

This chapter will describe the ESD protection developed for products in dual gate oxide, partially depleted (PD) SOI technology. This approach is based on the distributed and boosted ESD network design methodology introduced by Stockinger *et al.* (2003, 2005), for bulk technologies. It will be shown how this approach can be extended to SOI, focusing on the SOI-specific device and network implications.

It is known that floating body SOI MOSFETs are prone to body charging effects both during normal operation and ESD. Body-tied SOI MOSFETs are less susceptible to body charging but are very sensitive to the device body resistance (Colinge, 1991; Chan *et al.*, 1994). This chapter compares breakdown voltage data (V_{b1} and V_{b2}) of both floating body and body-tied SOI transistors along with data from a corresponding bulk technology. It shows that, for ESD purposes, the SOI transistors are much more fragile

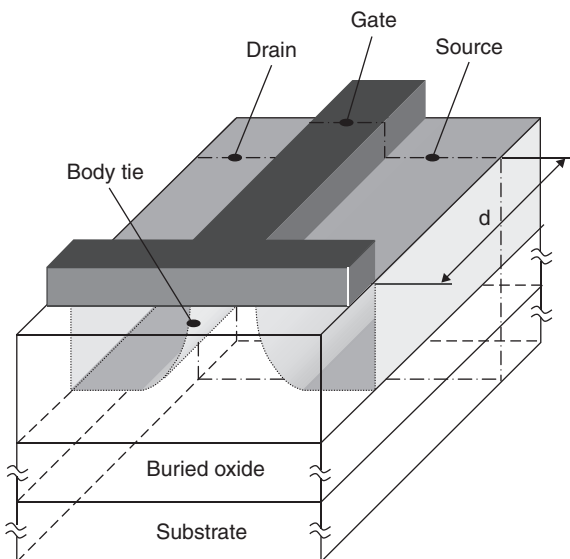
than the bulk ones, and that, contrary to common belief, the body-tied SOI device does not provide much ESD benefit over the floating body device.

The chapter also demonstrates that, while the SOI gated diode has a higher conductance than the traditional bulk trench-isolated diode, it does exhibit a lower ESD failure current. A SPICE compact model to describe the gated diode in the high-current ESD regime will be introduced. ESD characteristics of advanced technology node SOI devices, such as FinFETs, FinDiodes and fully depleted SOI (FDSOI) devices will be discussed. A response surface method to conveniently optimize ESD device sizes depending on the output buffer configuration will be presented.

9.2 ESD characterization in SOI devices: SOI transistors

Let us first study fully silicided thin oxide partially depleted OD1 ($18\text{ \AA}/1.2\text{ V}$) and thick oxide OD2 ($50\text{ \AA}/2.5\text{ V}$) NMOS and PMOS devices. The OD1 transistors are of floating body type only, while the OD2 transistors are available in either floating body or body-tied configurations. A schematic diagram of a body-tied SOI transistor is shown in Fig. 9.2. The breakdown characteristics of this transistor depend on the body resistance. Consider a transistor cross-section at a distance d from the body tie, as shown in Fig. 9.2. With the stress voltage, V_{ds} , applied to the drain and all other electrodes (source, gate and body tie) grounded, the collector-base (drain) junction becomes reverse biased, leading to the production of avalanche current. The avalanche generated hole current, drifting through the effective body tie resistance to ground, gives rise to an increase in body potential local to the avalanching junction. With the local body potential high enough to forward bias the emitter-base (source) junction, the bipolar turns on. Since the body resistance and the local body potential increase with distance d , for the transistor with channel width w , the first breakdown voltage, V_{d1} , is defined by the cross-section at $d = w$. To ensure consistent body resistance values, a fixed maximum channel width for individual body-tied devices is assumed here. Thus large transistors such as the ESD rail clamp must be laid out in an array of smaller segments. A similar layout was used for individually tested devices.

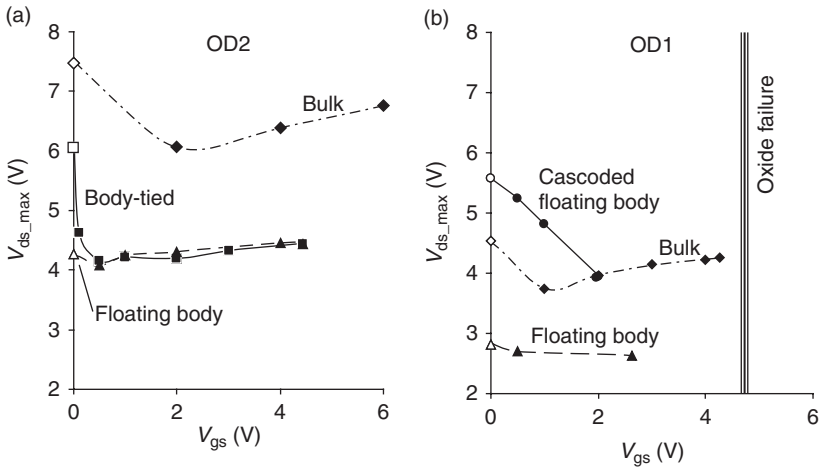
ESD device characterization involves pulsed high-current testing with pulse duration typical for ESD events in the range from 1 to 100 ns. This characterization is typically performed using a transmission line pulse (TLP) system. The system allows exploring ESD device operating limits and setting realistic network optimization targets. To study transistor characteristics under different gate biases the system needs to allow changing the gate bias of the tested structures either by providing gate voltage directly during the drain stress or by using a resistive voltage divider.



9.2 Schematic diagram of a body-tied SOI transistor.

Let us investigate how the maximum drain-to-source voltage before failure, V_{ds_max} , depends on device type (OD1 vs OD2, floating body vs body-tied, single vs cascoded), on the applied gate bias, V_{gs} , and on the applied pulse width, t_{pulse} . The measured second breakdown current (It_2) of all devices was very low (2 mA/ μm or less), which is typical for SOI devices. Therefore, the It_2 engineering approach widely used in bulk technologies and relying on significant ESD discharge current to flow through NMOS and PMOS buffers cannot be easily applied in SOI (Polgreen and Chatterjee, 1989; Amerasekera and Seitchik, 1994; Amerasekera and Duvvury, 1995). Instead an alternative approach, similar to the one described for bulk technologies by Khazhinsky *et al.* (2004), can be used. Where possible, SOI devices were compared to a corresponding bulk counterpart. While this comparison is not ideal due to non-matching transistor performance targets, it provides interesting qualitative information.

Figure 9.3a shows V_{ds_max} measurements as a function of gate bias (V_{gs}) for floating body and body-tied OD2 SOI NMOS transistors. For comparison, data from an OD2 (50 Å/2.5 V) bulk device are also shown. The transistor gate bias is changed from 0 V to the maximum voltage of $V_{gs} = V_{ds}$ ('hot gate'), which is well below the oxide failure limit of about 10 V for OD2 transistors. It should be pointed out that the term V_{ds_max} corresponds to the greater of V_{t1} or V_{t2} . For $V_{gs} = 0$ V all devices exhibited a pronounced snapback in the $I_d(V_{ds})$ curve with $V_{t1} > V_{t2}$, therefore $V_{ds_max} = V_{t1}$ at $V_{gs} = 0$ V (unfilled symbols). For $V_{gs} > 0$ V, none of the devices exhibited snapback ($V_{t2} > V_{t1}$), therefore $V_{ds_max} = V_{t2}$ (filled symbols). Note that V_{ds_max} of



9.3 V_{ds_max} measurements ($t_{pulse} = 120$ ns) of (a) OD2 and (b) OD1 NMOS transistors as a function of V_{gs} for various transistor configurations. V_{t1} , unfilled symbols, V_{t2} , filled symbols. (Source: Reproduced Fig 2, p 71 from 2005 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.)

both the floating body and body-tied SOI devices is significantly reduced by ~ 2 V compared to the bulk device. While the floating body greatly accelerates bipolar turn-on (Colinge, 1991; Verhaege *et al.*, 1993; Chan *et al.*, 1994; Ramaswamy *et al.*, 1995; Raha *et al.*, 1997b, c, 1999), it can be seen that little ESD benefit is gained with the body-tied device. The V_{ds_max} values of the OD2 body-tied and floating body devices are almost identical at each point except at $V_{gs} = 0$ V, where the body-tied device exhibits a 1.8 V higher V_{ds_max} . Only with the low impact ionization rate at $V_{gs} = 0$ V was the body tie able to hold down the body potential, postponing NPN turn-on and allowing V_{ds} to exceed 5 V without damage. For higher gate biases the body tie was too resistive and therefore ineffective.

Figure 9.3b shows V_{ds_max} as a function of V_{gs} for single and cascoded floating body OD1 NMOS transistors and data from a single OD1 (20 Å, 1.2 V) bulk device for comparison. During pulse testing the gate bias of single transistors was changed from 0 V to the maximum voltage of $V_{gs} = V_{ds}$ ('hot gate'). For the cascoded devices special care was taken to reproduce the correct upper gate (tied to VDD) bias condition V_{gs1} during pulse testing, as present in an actual cascoded output buffer I/O design, while applying varying bias V_{gs2} on the lower gate in the range from 0 V to VDD. The worst case stress on the cascoded NMOS output buffer occurs during positive ESD events on the corresponding I/O pad with respect to another grounded I/O pad. The intended ESD current path for this event includes a diode up to VDD and an active MOSFET rail clamp to VSS.

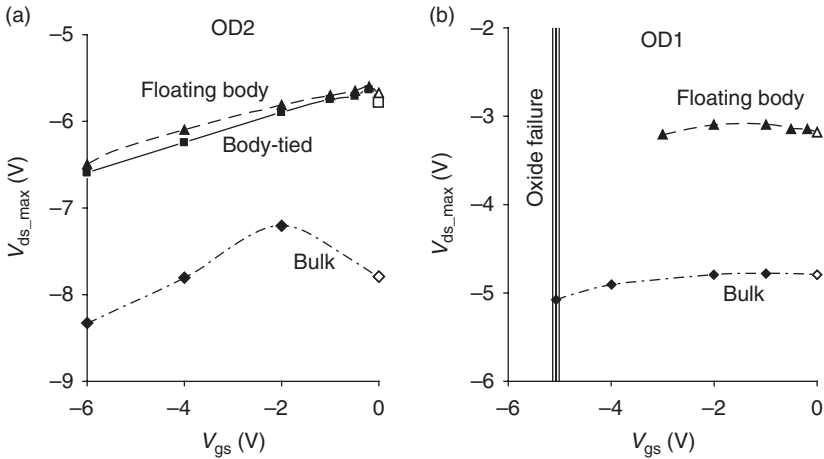
VDD is at the midpoint in this ESD path and is typically held near one-half of the I/O pad voltage ($V_{ds}/2$). Therefore a resistive voltage divider was utilized during pulse testing of the cascoded structures to ensure an upper gate bias of $V_{gs1} = V_{ds}/2$ (Khazhinsky, 2005). The lower gate voltage was varied from 0 V to $V_{gs2} = V_{ds}/2$ ('hot gate'). The gate bias corresponding to the oxide failure limit of the OD1 transistors is about 5 V. This limit is shown with a vertical line in Fig. 9.3b. Note, that the device robustness is limited by lateral first or second breakdown (V_{ds_max}) rather than vertical oxide failure.

Comparing the single floating body SOI to the bulk device a significant reduction (~ 1.8 V) in V_{ds_max} (V_{gs}) can be seen again. The V_{ds_max} values of the single floating body NMOS transistor are quite low (2.6–2.8 V). This leads to the conclusion that, when used as an output buffer, this device is extremely difficult to protect. However, as shown in Fig. 9.3b, by cascoding two OD1 floating body devices, V_{ds_max} measured across the cascoded pair can be greatly increased (Miller *et al.*, 2000). Another option for ESD-hardening the single OD1 NMOS output buffer is to add a series output resistor and secondary ESD diodes as described by Khazhinsky *et al.* (2004).

Figure 9.4 shows V_{ds_max} as a function of V_{gs} for floating body and body-tied OD2 and OD1 SOI PMOS transistors. For comparison, data from corresponding bulk devices are shown as well. Note that $|V_{ds_max}|$ of SOI devices is again significantly reduced (~ 2 V) compared to the bulk devices. For OD2 PMOS transistors (Fig. 9.4a) the body tie gives a slight improvement in V_{ds_max} compared to floating body. However, the largest V_{ds_max} improvement is observed when the gate of the transistor is biased during an ESD event such that $V_{gs} = V_{ds}$ ('hot gate'). The smallest $|V_{ds_max}|$ values are observed at V_{gs} ranging from -0.5 to -2 V.

For OD1 PMOS transistors shown in Fig. 9.4b the absolute values of V_{ds_max} are quite low. However, they are higher than those for the NMOS transistor. For example the worst case V_{ds_max} for the single floating body OD1 PMOS is -3.2 V, while it was only 2.6 V for OD1 NMOS. Note that again both OD1 and OD2 transistor failure limits are determined by V_{ds_max} rather than oxide robustness.

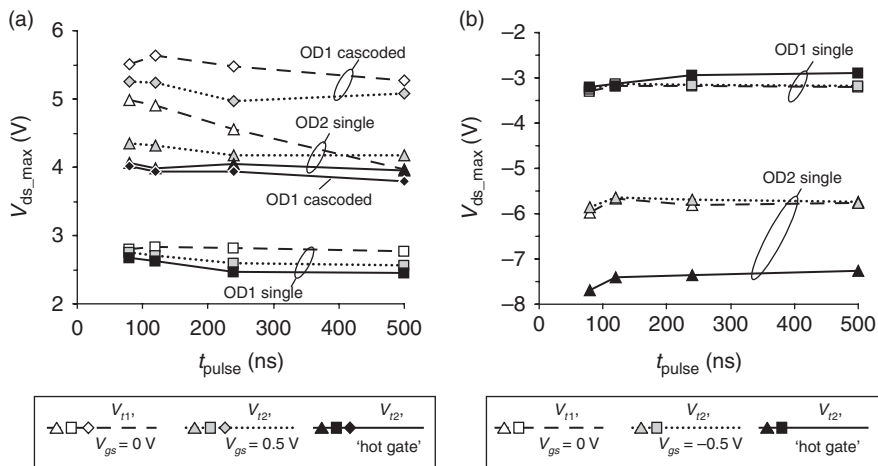
An important ESD phenomenon peculiar to floating body devices is that V_{ds_max} is sensitive to the pulse width, t_{pulse} . As has been described for grounded gate devices by Raha *et al.* (1997b), this t_{pulse} sensitivity can be explained with a capacitive charging model. The parasitic bipolar turn-on time in SOI technology varies from 100 ps to a few microseconds depending in part on the presence of the body tie and the amplitude of the applied voltage stress pulse (Raha *et al.*, 1997b). If the body resistance is small (body-tied SOI devices), the RC time constant for charging up the source-body junction during pulse test is negligible (~ 1 ps) in comparison to the stress pulse widths (~ 100 ns). Impact ionization at the collector-base junction produces holes that charge the body. Once it is charged to a point where the emitter-



9.4 V_{ds_max} measurements ($t_{pulse} = 120$ ns) of (a) OD2 and (b) OD1 PMOS transistors as a function of V_{gs} for various transistor configurations. V_{I1} , unfilled symbols, V_{I2} , filled symbols. (Source: Reproduced Fig 3, p 72 from 2005 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.)

base junction forward biases, the lateral bipolar turns on (V_{I1}). Therefore the bipolar snapback in body-tied SOI devices occurs immediately during pulse rise. If the body resistance is infinite, like in floating body SOI transistors, the body potential is raised due to both impact ionization at the drain junction and the capacitive charging current. Initially, during fast pulse ramp up (~ 1 ns), the capacitive charging current dominates. However it may not be sufficient for the bipolar to fire. In that case the impact ionization current further elevates the body potential during the pulse steady phase. If both V_{ds} and t_{pulse} are sufficient to elevate the body potential, the bipolar fires.

Figure 9.5 shows measurements for NMOS and PMOS OD1 and OD2 floating body transistors revealing the influence of both t_{pulse} (80–500 ns) and V_{gs} (for three bias conditions) on V_{ds_max} . While a slight decrease in V_{ds_max} with increasing t_{pulse} is seen for all devices and all V_{gs} voltages, the OD2 NMOS device (Fig. 9.5a) at $V_{gs} = 0$ V shows the greatest decrease (~ 1 V). This is because for a given V_{ds} , the OD2 device exhibits the lowest impact ionization current at $V_{gs} = 0$ V. Therefore only here the floating body charging current is low enough to see a significant V_{I1} dependence on t_{pulse} . For the PMOS the V_{ds_max} variation with pulse width is less pronounced (see Fig. 9.5b). However, a change of up to 0.5 V in V_{ds_max} can be seen for the shortest pulses. These pulse durations require a higher voltage amplitude to fully charge the transistor body to turn on the parasitic bipolar. Due to the dependence on t_{pulse} , V_{ds_max} data can be conservatively considered up to $t_{pulse} = 500$ ns for defining the transistor operating limits.



9.5 V_{ds_max} measurements as a function of t_{pulse} for floating body (a) NMOS and (b) PMOS transistors. 'Hot gate' refers to $V_{gs} = V_{ds}$ (single), $V_{gs2} = V_{ds}/2$ (cascoded). Upper gate of the cascoded OD1 NMOS transistor is kept at $V_{gs1} = V_{ds}/2$. (Source: Reproduced Fig 4, p 73 from 2005 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.)

Table 9.1 Worst case V_{ds_max} values and protection targets for the SOI transistors

	Transistor option	Worst case V_{ds_max} (V)	Protection target (V)
NMOS	Single floating body OD1	2.6	2.0
	Cascoded floating body OD1	3.8	2.9
	Single body-tied OD2	4.2	3.2
PMOS	Single floating body OD1	-3.2	-2.5
	Single body-tied OD2	-5.7	-4.3

Source: Reproduced Table 1, p 74, from 2005 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.

From the data presented in Figs 9.3–9.5 it is clear that SOI devices, whether floating body or body-tied, are much more fragile in terms of V_{ds_max} than their bulk counterparts. Therefore, it can be expected that SOI ESD networks need to be significantly upsized from bulk designs in order to compensate for the reduced V_{ds_max} network performance targets. While not giving much ESD benefit, the body tie is used extensively in the I/O design. For consistency with the rest of the I/O design, only body-tied OD2 devices were used in building the ESD networks.

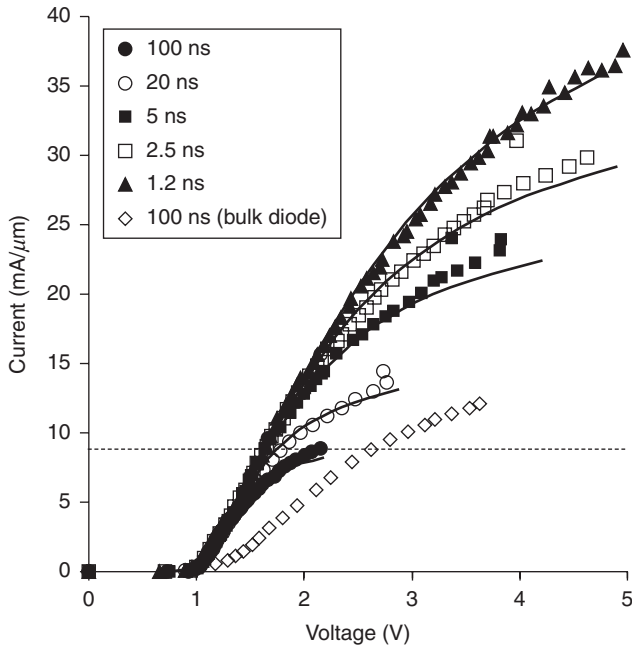
Table 9.1 summarizes the worst case $V_{ds_max}(V_{gs}, t_{pulse})$ values of the OD1 floating body (single and cascoded) and OD2 body-tied configurations. It also lists the protection targets used in the network simulations. Note that the targets are 25% below the actual measured worst case V_{ds_max} values to provide extra margin to failure for the ESD network design. The rail clamp networks are designed so that, during ESD, all clamp transistors operate under only slightly elevated bias conditions compared to normal power supply levels. With these limits, the standard transistor compact models available in an SOI technology are still accurate for ESD network simulations.

9.3 ESD characterization in SOI devices: SOI diodes

Diodes are used extensively in ESD protection networks to provide an ESD discharge path from an I/O pad and to couple different power/ground domains. Gated diodes are most commonly used in SOI due to the difficulties in implementing a trench-isolated (STI bound) diode (Voldman *et al.*, 1998; Richier *et al.*, 2000; Salman *et al.*, 2004). Also, often thick (OD2) diodes are used exclusively for oxide reliability reasons. Further, only the p+/Nwell diode type is utilized since it has a slightly smaller parasitic capacitance than the n+/Pwell type. The gated diodes are laid out with a single row of contacts to optimize the device for maximum conductance per unit layout area rather than for maximum It^2 per unit periphery.

Let us review the results of SOI diode characterization which was performed using a 50 Ω automated very fast transmission line pulse (VF-TLP) system (Grund, 2003, 2005; Grund and Gauthier, 2004). In order to explore time dependent self-heating and breakdown effects, the pulses in the range from 1.2 to 100 ns were used. The pulse rise time was measured at 175 ps. For the 100 ns pulse length, the system was configured as a standard TLP in time domain reflection (TDR)-O mode (overlapping incoming and reflected pulses); for all shorter pulses, a VF-TLP configuration in TDR-S mode (separate incoming and reflected pulses) was used. Four-point Kelvin measurements were consistently utilized to eliminate inaccuracies due to system noise and variability of the parasitic needle-to-pad resistance (Stockinger and Miller, 2006).

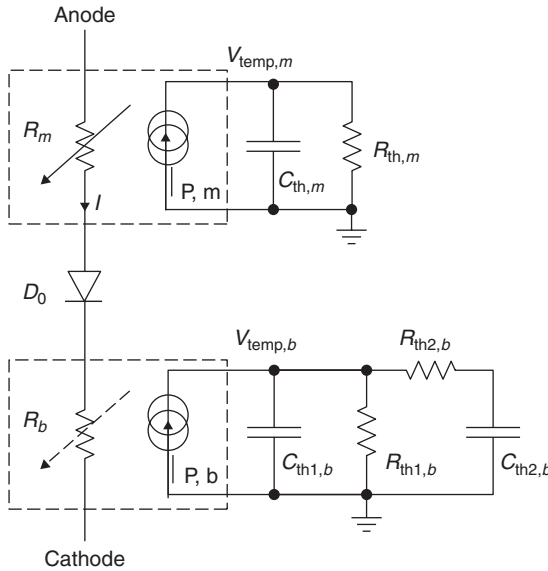
Figure 9.6 shows the high-current I-V curves for this device, with t_{pulse} varying from 1.2 to 100 ns. Self-heating causes current saturation and determines the failure point, which is the last datapoint shown for each curve. Note that the failure points are t_{pulse} dependent. In the designs the diode current limit is chosen at 8.5 mA/ μ m (horizontal line in Fig. 9.6), which corresponds to the failure point at $t_{pulse} = 100$ ns. A typical charged device model waveform has ~ 1 ns pulse width, while a typical machine model waveform has ~ 30 ns pulse width and a typical human body model waveform corresponds to ~ 100 ns TLP pulses. Therefore the chosen current limit of 8.5 mA/ μ m should provide adequate margin for CDM, MM and HBM events.



9.6 High-current diode measurements (symbols) vs ESD model (lines). Diode current is scaled to junction perimeter. (Source: Reprinted from Khazhinsky *et al.* 2007, Copyright 2007, with permission from Elsevier.)

Also shown in Fig. 9.6 is the curve for a typical bulk STI bound diode (Torres *et al.*, 2001). It can be seen that the gated SOI diode exhibits a higher on-conductance than the bulk diode before the self-heating effect causes current saturation. However, the gated SOI diode suffers from a lower failure threshold due to the limited conductive layer thickness and poor thermal conductivity of the buried oxide. Therefore, when porting an ESD network design from bulk to SOI, one can sometimes place smaller ESD diodes and meet the ESD performance targets, but, as will be demonstrated below, there is often a limit in diode scaling due to the lower failure current.

The standard gated diode compact model available as part of technology process design kit (PDK) is typically not adequate to describe the device in the pulsed high-current ESD regime. Therefore a special diode compact model which captures this regime is required. An implementation of such a model following Khazhinsky *et al.* (2005) is shown in Fig. 9.7. The diode junction is modeled by the standard gated SOI diode model D0 available in the design kit of this technology with one modification: the base resistance of D0 is set to zero and modeled by a separate temperature dependent resistor, R_b :



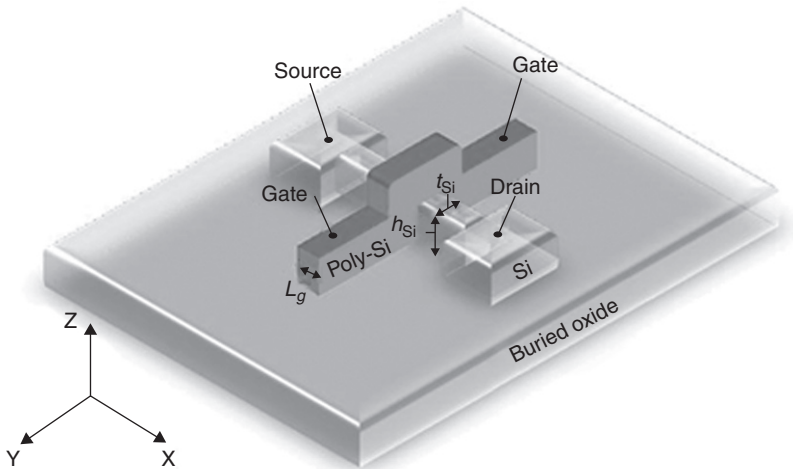
9.7 Sub-circuit of the ESD diode compact model with transient self-heating. (Source: Reprinted from Khazhinsky *et al.* 2007, Copyright 2007, with permission from Elsevier.)

$$R_b = \frac{l_b}{w_b} \cdot \rho_{0,b} \cdot \left(1 + \alpha_b \cdot V_{temp,b} \cdot 1 \frac{K}{V} \right). \tag{9.1}$$

The resistance of the metallization of the diode fingers R_m is implemented likewise. Both resistors are described by a transient self-heating model implemented in Verilog-A, which accounts for a linear temperature dependence. The parameters l_b and w_b define the length and width of the interconnect structure, respectively, $\rho_{0,b}$ denotes the sheet resistance at ambient temperature, α_b the linear temperature coefficient and $V_{temp,b}$ the equivalent voltage for the temperature increase. To obtain the time dependent temperature of the resistor, an equivalent thermal RC network ($R_{th1,b}$, $R_{th2,b}$, $C_{th1,b}$, and $C_{th2,b}$) is included in the model sub-circuit. The dissipated power per unit area in the resistor R_b is provided by the Verilog-A model as a current source output $I_{P,b}$ that drives the RC network (I is the current through resistor R_b):

$$I_{P,b} = \frac{R_b \cdot I^2}{w_b \cdot l_b} \cdot 1 \frac{\mu m^2}{V}. \tag{9.2}$$

The temperature increase appears as an equivalent voltage $V_{temp,b}$ across the RC network, and is used in Equation [9.1] to calculate the R_b increase due to self-heating. This compact model has been calibrated to diode and metal



9.8 3D Visualization of a FinFET, the gate wraps around a thin fin.
 (Source: © 2008 IEEE. Reprinted with permission from Khazhinsky *et al.* (2008) 'Study of undoped channel FinFETs in active rail clamp ESD networks', IEEE Proceedings.)

line high-current pulse data with varying t_{pulse} . The data *vs* model fit is shown in Fig. 9.6.

9.4 ESD characterization in SOI devices: fin-on-oxide field effect transistors (FinFETs) and FinDiodes

Another SOI-based device that requires ESD characterization is the FinFET (Fig. 9.8). Like its planar MOSFET counterparts, FinFET must be protected from external ESD stress events. This is particularly true for FinFETs which connect directly to external pads, as is the case when a FinFET is configured for use in an output driver. Thus there is a need for providing effective ESD protection for FinFETs.

Recently a number of papers have been published studying ESD characteristics of FinFETs for use in I/O and ESD circuits. FinFET ESD studies by Russ *et al.* (2005) and Gossner *et al.* (2006) were focused on doped channel thick fin (~50 nm) poly-Si gate devices. These FinFETs were fabricated using a conventional SOI CMOS flow with the fin formation replacing the STI module. Tremouilles *et al.* (2007) studied ESD performance of undoped channel FinFETs operating in the high-current parasitic bipolar transistor mode for various layout and process options. Khazhinsky *et al.* (2008) took a different tack, studying undoped channel FinFETs with a focus on their use as both output buffer devices to be protected during ESD and as MOSFET-only mode (not bipolar) clamp devices in active rail clamp networks. In this

chapter let us review both thin and thick oxide SOI FinFET ESD reliability at different gate bias operating conditions.

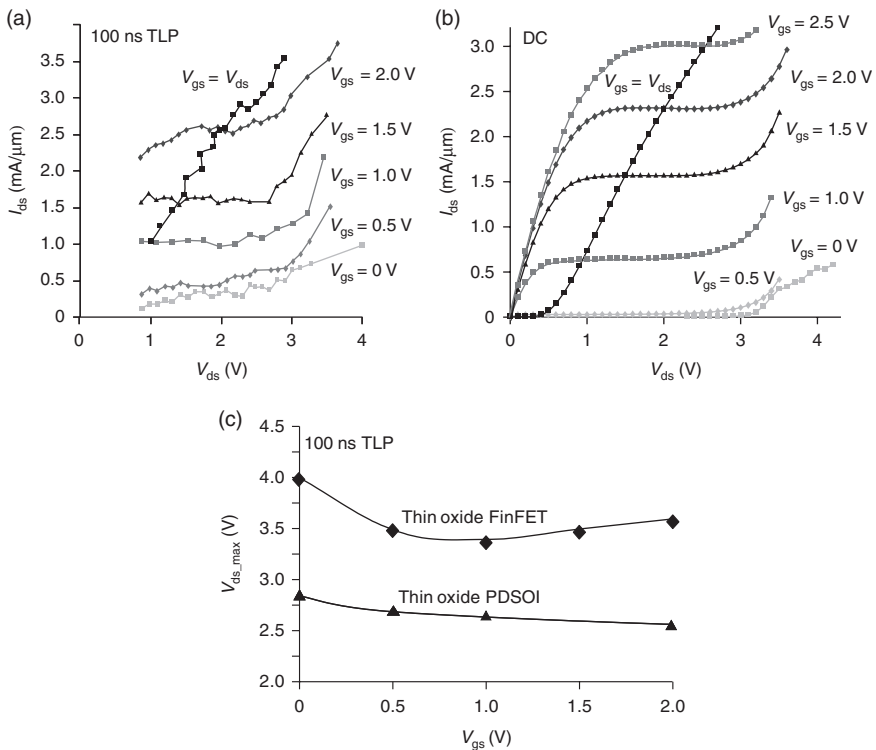
To assess FinFET electrical performance following Khazhinsky *et al.* (2008) both DC and TLP characterization with 100 ns pulses has been carried out. In addition, Technology CAD (TCAD) has been used to simulate the physical mechanisms originating in the FinFET during both normal operation and ESD. In the 3D device simulation the drift-diffusion model coupled with the continuity and Poisson's equations including quantum correction using density gradient have been solved for the device structure shown in Plate VIIa (see color section between pages 202 and 203). The device has $t_{\text{Si}} = 20$ nm, $h_{\text{Si}} = 100$ nm, $t_{\text{ox}} = 50$ Å and metal gate.

In contrast with conventional planar devices the current flow in FinFETs exhibits strong non-uniformity in the horizontal direction perpendicular to the current flow (Y-axis) for small gate biases. This can be seen in Plate VIIb showing the electron distribution in the device cross-section taken across the channel in the middle of the gate when $V_{\text{ds}} = 2.5$ V and $V_{\text{gs}} = 1$ V. However, as the FinFET approaches the 'hot gate' regime resembling ESD clamp operation ($V_{\text{gs}} = V_{\text{ds}} = 2.5$ V) the current becomes distributed uniformly across full FinFET channel cross-section (Plate VIIc), thus ensuring high current carrying capabilities and robust breakdown characteristics of the device.

Figure 9.9a shows I_{ds} vs V_{ds} pulse measurement data for the 17 Å oxide NMOS FinFET with metal gate. Data were gathered with a 50 Ω TLP system (Oryx/Thermo Celestron-I) using 100 ns pulses. The pulse rise time was measured at 175 ps. The system was configured as a standard TLP in TDR-O mode (overlapping incoming and reflected pulses). Curves are shown for various V_{gs} bias conditions. The last point on these curves corresponds to the transistor failure point, where leakage measured at $V_{\text{ds}} = 1.2$ V and $V_{\text{gs}} = 0$ V increases by more than 50%. As expected, for the grounded gate case ($V_{\text{gs}} = 0$ V), there is very little current through the device up to the first breakdown voltage (V_{t1}) threshold at $V_{\text{ds}} = 4.0$ V. For $V_{\text{gs}} = 0$ V, we could not resolve a distinct bipolar conduction region. Any transition beyond V_{t1} results in immediate second breakdown (V_{t2}) and permanent physical damage. Therefore, for $V_{\text{gs}} = 0$ V, $V_{\text{t2}} = V_{\text{t1}}$. As V_{gs} is increased, the device first conducts as a MOSFET and then fires as parasitic bipolar junction transistor at V_{t1} . This can be seen clearly, for example, in the $V_{\text{gs}} = 1.5$ V curve of Fig. 9.6a. Note that the device exhibits only MOSFET current up to $V_{\text{ds}} = 2.8$ V. The parasitic lateral NPN BJT fires at $V_{\text{t1}} = 2.8$ V and conducts in parallel with the NMOSFET for $V_{\text{ds}} > V_{\text{t1}}$, producing a distinct increase in the slope of the I–V curve. The BJT and NMOSFET continue to conduct in parallel, with the BJT dominating, up to the second breakdown threshold at $V_{\text{t2}} = 3.5$ V. Note that, for higher V_{gs} bias conditions, it becomes difficult to accurately pinpoint the exact V_{t1} threshold on the I–V curves due to the more gradual

transition in slope between the MOSFET dominated regime and the BJT dominated regime. The V_{I2} threshold, on the other hand, is easily extracted from the I–V curves. Also note that, for all non-zero gate biases, the transition into the BJT dominated regime is entered without any undesirable negative resistance ‘snapback’ transitions. For comparison, Fig. 9.9b shows the well-behaved quasi-static I_{ds} vs V_{ds} measurement data for this device.

In Fig. 9.9c we provide the TLP summary data which shows how $V_{ds,max}$ (maximum of V_{I1} or V_{I2} , as defined by Khazhinsky *et al.* (2005)) varies as a function of V_{gs} . As V_{gs} is increased from 0 V, $V_{ds,max}$ falls from an initial value of 4.0 V at $V_{gs} = 0$ V to a minimum value of 3.4 V at $V_{gs} = 1$ V, then rises again. The minimum $V_{ds,max}$ value is reached when gate bias conditions favor both high electric field and high seed current resulting in increased impact ionization rates. This worst case $V_{ds,max}$ value is used as a protection target



9.9 (a) Experimental TLP I–V characteristics; (b) quasi-static I–V characteristics; (c) $V_{ds,max}$ dependence on V_{gs} for thin oxide undoped channel NMOS FinFET (17 Å oxide, $L_g = 70$ nm). (Source: © 2008 IEEE. Reprinted with permission from Khazhinsky *et al.* (2008) ‘Study of undoped channel FinFETs in active rail clamp ESD networks’, IEEE Proceedings.)

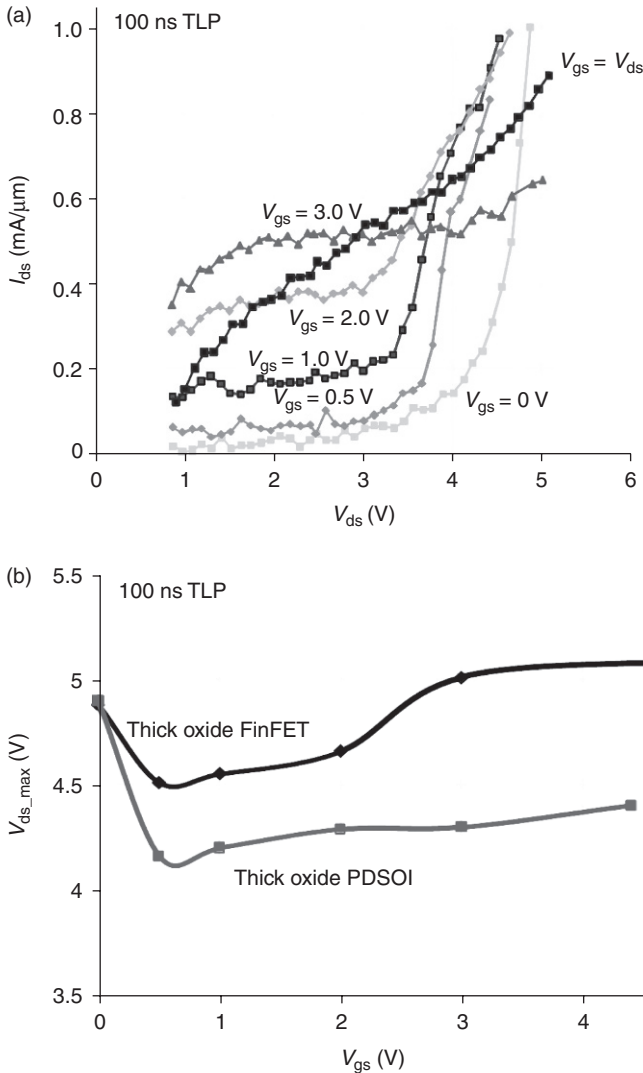
for a FinFET when it is configured as an output buffer device, since it is assumed that V_{gs} can vary during ESD. It can be seen from Fig. 9.9c that the worst case V_{ds_max} value in the thin oxide FinFET (3.4 V) is higher than the analogous V_{ds_max} value of 2.8 V in the corresponding planar PDSOI NMOS transistors as reported by Khazhinsky *et al.* (2005).

Next we consider the thicker (50 Å) oxide FinFET with metal gate. It also reveals a pronounced dependence of breakdown characteristics on gate bias. Figure 9.10a shows 100 ns TLP I_{ds} vs V_{ds} measurement data for the 50 Å oxide NMOS FinFET under various V_{gs} bias conditions. At $V_{gs} = 0$ V, the V_{t1} and V_{t2} threshold is reached at $V_{ds} = 4.8$ V. In Fig. 9.11b we show how V_{ds_max} voltage varies as a function of V_{gs} . As V_{gs} is increased from 0 V, V_{ds_max} falls from an initial value of 4.8 V at $V_{gs} = 0$ V to a minimum value of 4.5 V at $V_{gs} = 0.5$ V, then rises again. This worst case V_{ds_max} value is used as a protection target for a FinFET when it is configured as an output buffer device. It can be seen from Fig. 9.10b that the worst case V_{ds_max} value in the thick oxide FinFET (4.5 V) is higher than the analogous V_{ds_max} value of 4.2 V in the corresponding planar PDSOI NMOS transistors as reported by Khazhinsky *et al.* (2005). Therefore, breakdown characteristics of measured thicker (50 Å) oxide FinFETs are superior to similar devices in the planar PDSOI technology.

The advantages of FinFETs become more apparent with decreasing fin thickness. Figure 9.11 compares the breakdown characteristics of thin (22 nm) and thick (32 nm) fin devices at 0.5 V gate bias, corresponding to the worst case breakdown condition described above. As the fin thickness is reduced from 32 to 22 nm, the worst case breakdown voltage V_{ds_max} of 4.5 V (measured at $V_{gs} = 0.5$ V) increases to 5.4 V. The higher breakdown of the thinner fin transistors (which is observed at other gate biases as well) is partly due to the higher threshold voltage of the thinner fin devices, but is also aided by a more uniform distribution of the current in thinner fin transistors due to bulk-inversion (Kim *et al.*, 2005) and better heat dissipation due to an increased thermal conducting surface.

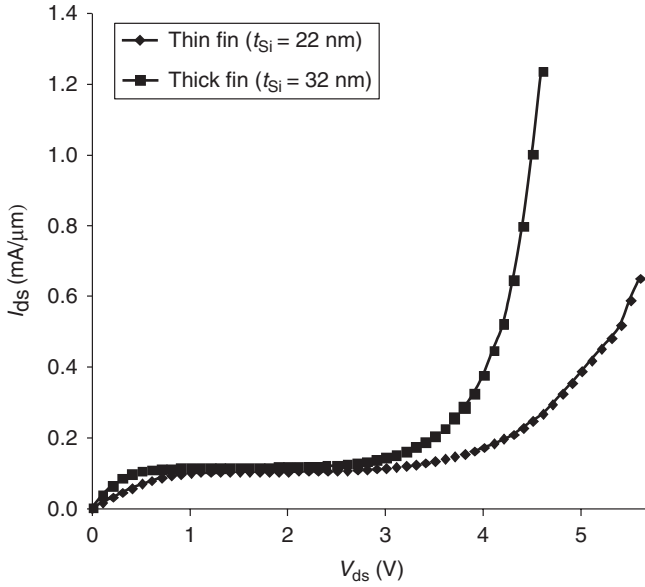
In summary, when compared to their planar PDSOI counterparts, the thin and thick oxide FinFETs exhibit a higher breakdown voltage at all gate biases. These data indicate that the FinFET may serve well as both the output buffer device and as the clamp device in an RC-triggered active clamp circuit.

In addition to FinFETs, this technology allows the creation of FinDiodes. These devices can be manufactured by doping two sections of the fin separated by the gate with the implants of the opposite type (Fig. 9.12). In this technology we exclusively use thick oxide (50 Å) diodes for oxide reliability reasons. Since the entire FinDiode cross-section conducts current, FinDiodes show superior ESD current carrying capability in forward mode, uniform current flow and reduced capacitive coupling compared to a conventional gated diode.

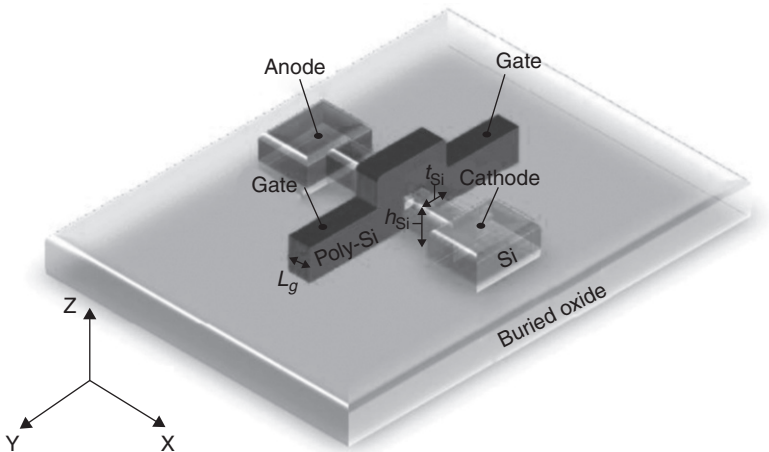


9.10 Experimental TLP I-V characteristics (a) and $V_{ds,max}$ dependence on V_{gs} (b) for thick oxide undoped channel NMOS FinFET (50 Å oxide, $L_g = 280\text{ nm}$). (Source: © 2008 IEEE. Reprinted with permission from Khazhinsky *et al.* (2008) 'Study of undoped channel FinFETs in active rail clamp ESD networks', IEEE Proceedings.)

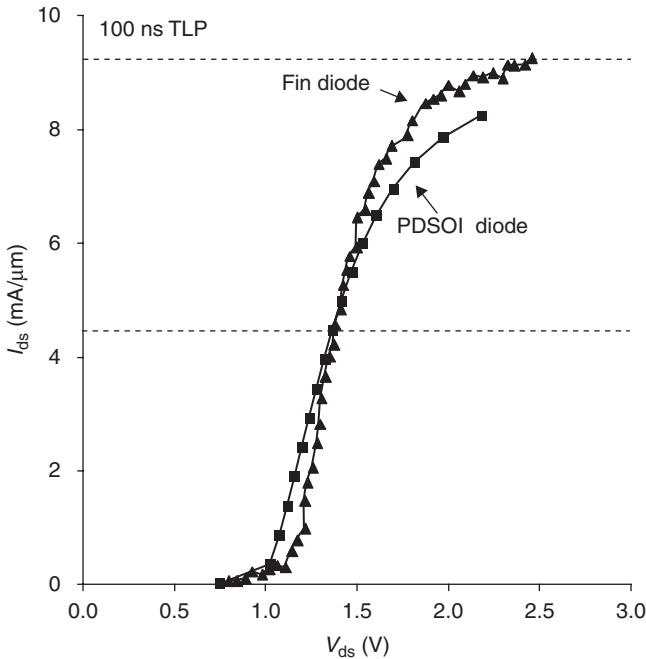
Figure 9.13 shows the 100 ns TLP I-V characteristics of a FinDiode. For normalization of current, the diode perimeter is assumed to be double the height of the Si (h_{Si}). Self-heating causes current saturation at $V_{ds} > 1.5\text{ V}$ and determines the failure point, which is the last datapoint shown on the



9.11 Effects of fin thickness reduction on the breakdown characteristics of double gate devices, $L_g = 280$ nm. (Source: © 2008 IEEE. Reprinted with permission from Khazhinsky *et al.* (2008) 'Study of undoped channel FinFETs in active rail clamp ESD networks', IEEE Proceedings.)



9.12 3D visualization of a FinDiode. (Source: © 2008 IEEE. Reprinted with permission from Khazhinsky *et al.* (2008) 'Study of undoped channel FinFETs in active rail clamp ESD networks', IEEE Proceedings.)



9.13 Comparison of FinDiode and 65 nm PDSOI diode I-V characteristics. (Source: © 2008 IEEE. Reprinted with permission from Khazhinsky *et al.* (2008) 'Study of undoped channel FinFETs in active rail clamp ESD networks', IEEE Proceedings.)

curve ($V_{ds} = 2.5$ V, $I_{ds} = 9.2$ mA/ μ m). In the ESD network designs we would choose to operate the diode in the high-current regime but limit the diode current to 9.2 mA/ μ m.

Also shown in Fig. 9.13 is the curve for a conventional PDSOI diode, as reported by Khazhinsky *et al.* (2005). It can be seen that the FinDiode exhibits a higher on-conductance than the PDSOI diode in the high ESD current regime ($I_{ds} > 4.5$ mA/ μ m) before the self-heating effect causes current saturation. Also, the FinDiode shows a higher failure threshold compared to the conventional PDSOI diode. This makes the FinDiode an attractive device in rail clamp based ESD protection networks.

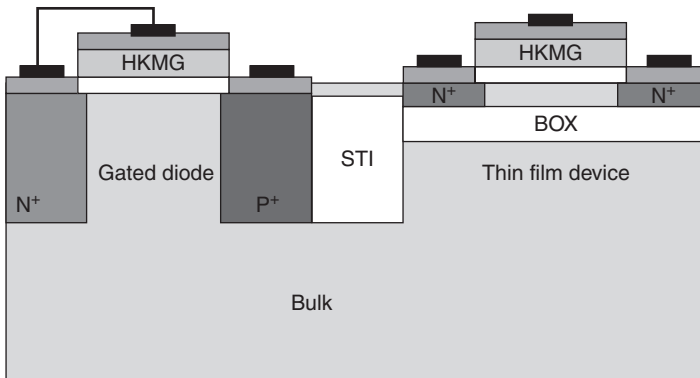
9.5 ESD characterization in SOI devices: fully depleted SOI (FDSOI) devices

Recently there were significant efforts in the development of planar FDSOI technology based on ultra-thin SOI and buried oxide (BOX) layers. The adoption of this technology for 28 nm process shows that planar FDSOI is a viable alternative to FinFET technology in the advanced nodes, especially for

System on Chip (SOC) and low power applications. Several papers have been published on ESD aspects of this technology – see, for example, Benoist *et al.*, 2010a, b and Dray *et al.*, 2012.

The beneficial properties of FDSOI technology include leakage current reduction, good control of short-channel effects, no latch-up, high immunity to the V_t variability, etc. However, in ultra-thin SOI technologies, the reduction of the active silicon layer thickness (T_{Si}), which is necessary for controlling the short-channel effect, also influences device performance in the strong injection regime, such as during ESD events. The inclusion of the high- k metal gate (HKMG) stack also affects device behavior in the ESD regime. Moreover, SOI BOX has inherently limited thermal dissipation during ESD. The above factors make FDSOI a challenging technology for enabling robust ESD protection.

The comparison of gated ESD diode performances in bulk, PDSOI and FDSOI technologies shows systematic degradation of ESD diode characteristics (I_{t2} , R_{on}) (Benoist *et al.*, 2010a). The reduction of BOX thickness in FDSOI improves ESD performance thanks to a better thermal dissipation. For example, a gain of 1.6 on the ESD diode robustness was shown by Benoist *et al.* (2010b), when comparing 10 and 145 nm BOX thickness. Further improvement can be achieved by using a hybrid bulk/FDSOI co-integration, via Silicon-on-nothing (SON) technology, where FDSOI devices are protected using ESD diodes built in the co-integrated bulk part, as shown in Fig. 9.14 (Benoist *et al.*, 2010a). The approach of hybrid bulk/FDSOI co-integration to enable robust ESD protection was further developed for 28 nm technology by Dray *et al.* (2012). Given very low BOX thickness (10–20 nm), the co-integration is achieved by local BOX etching to form ESD diodes in bulk substrate.



9.14 Cross-section of hybrid co-integration FDSOI and bulk devices. (Source: Reproduced Fig 8, p 5 from 2010 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.)

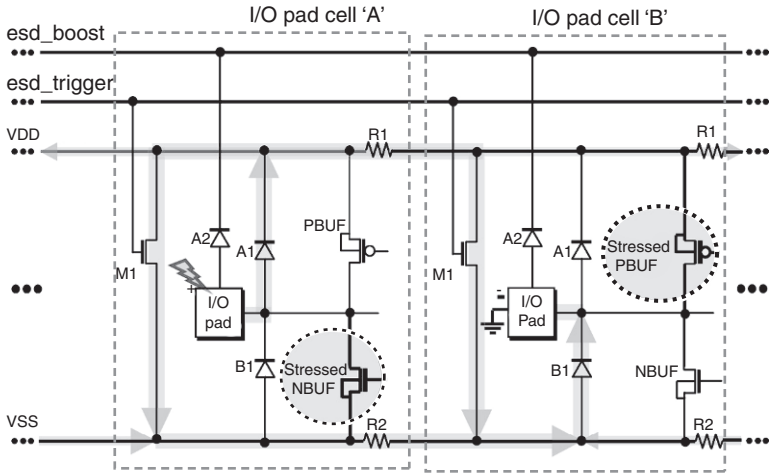
In contrast to ESD diodes, dynamically triggered ESD clamps do not suffer from reduced silicon volume available above the BOX in FDSOI technology. ESD clamps are sized to operate far from the avalanche region and therefore can be formed in FDSOI. Moreover, as demonstrated by Dray *et al.* (2012), the intrinsic superiority of ultra-thin BOX FDSOI technology improves the ESD clamping performance with respect to a similar bulk technology, when taking advantage of FDSOI back-biasing. This makes the implementation of a robust ESD protection in FDSOI technology feasible.

9.6 ESD network optimization in SOI devices

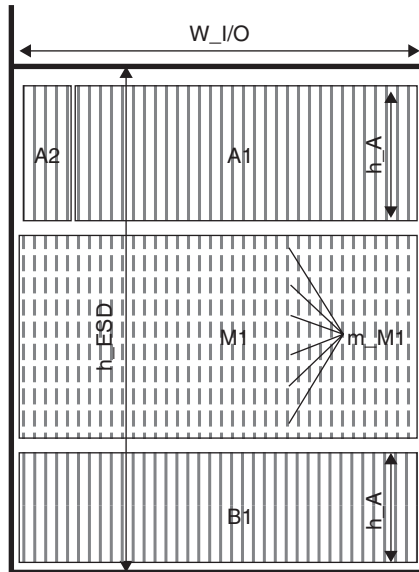
With the individual SOI device protection targets and compact models defined as described above, one can proceed with the ESD network design. This section follows very closely the distributed and boosted ESD network simulation methodology described by Stockinger *et al.* (2003, 2005) and focuses on the SOI-specific changes required. Following Khazhinsky (2007), the task is to design the ESD protection for an I/O library to be used on a wide range of SOI products. A typical product is configured with one or more banks of both 1.2 V OD1 I/O cells and 2.5 V OD2 I/O cells. Therefore two independent ESD networks were implemented to protect both 1.2 V and 2.5 V I/O banks. It is important to note that only OD2 diodes and MOSFETs were used as ESD devices, even to protect the fragile 1.2 V OD1 output buffers. The two networks differ only in the ESD device sizes.

Figure 9.15 shows the ESD devices and the output buffers to be protected in two adjacent I/O pad cells. It is assumed that additional I/O cells, forming an I/O bank, are placed on both sides of the cells shown. In addition to the output buffer, each I/O cell contains three diodes (A1, A2 and B1) and a rail clamp transistor, M1. A1 and B1 are the large ESD diodes for coupling the I/O pad to VDD and VSS, respectively. The much smaller A2 diode is a key element of the boosted clamp design as described by Stockinger *et al.* (2003, 2005). Note that in this distributed network, multiple clamps M1 operate in parallel to safely dissipate the ESD current between VDD and VSS. ESD trigger circuits (not shown) are placed remotely. Large clamps are placed at both ends of each I/O bank in order to terminate the network of smaller M1 clamps distributed in the I/O cells. Terminating clamps have been described by Torres *et al.* (2001) and Stockinger *et al.* (2003, 2005) and are not shown in Fig. 9.15.

Figure 9.16 is an illustration of the physical layout of the ESD portion of the I/O cell. I/O devices are placed above the ESD devices shown in the figure. In this project the width of the I/O cell ($w_{I/O}$) was fixed at 40 μm . Note that the ESD devices were drawn with banks of short vertical fingers across the full width of the I/O cell. The numbers of vertical fingers were fixed at 52, 4 and 58 for diodes A1, A2 and B1, respectively, and 55 for M1. Recall



9.15 NMOS and PMOS buffer ESD worst case scenario. (Source: Reproduced Fig 7, p 76, from 2005 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.)



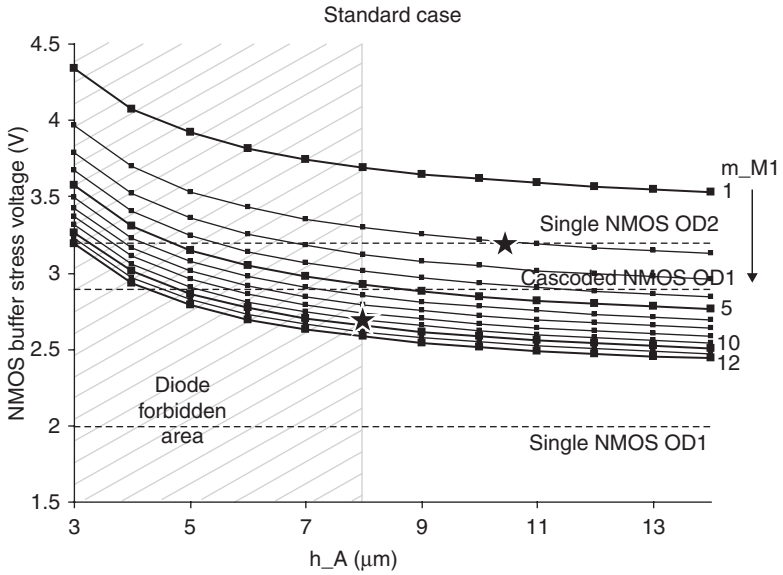
9.16 Conceptual ESD device floor plan of the I/O cell (I/O devices are not shown). (Source: Reproduced Fig 8, p 76, from 2005 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.)

that the body-tied clamp transistor M1 must be implemented in an array of $2\ \mu\text{m}$ segments. Figure 9.16 shows 6 rows of M1 fingers. For layout efficiency, it was decided to require an integer number (m_{M1}) of $2\ \mu\text{m}$ rows. The active heights of A1 and A2 (h_A) and B1 (h_B), as well as the number of M1 rows (m_{M1}) were the optimization variables.

The simulation goal was to determine the ESD device sizes in the I/O pad cell represented by h_A , h_B and m_{M1} , such that one could meet the output buffer protection targets defined in Table 9.1, while utilizing a minimum combined ESD layout area. For all simulations the peak ESD current was set to 3.8 A, corresponding to a worst case 200 V ESD MM event. To reach this goal, SPICE simulations were performed with a closed ring of 100 identical I/O cells using techniques described by Torres *et al.* (2001) and Stockinger *et al.* (2003, 2005). An I/O pad cell ‘A’ was positively stressed while an adjacent pad cell ‘B’ was grounded, as shown in Fig. 9.15. This adjacent pad stress configuration simultaneously produces the worst case voltage across the NMOS transistor in the stressed I/O pad and across the PMOS transistor in the grounded I/O pad. In the simulated circuit the parasitic incremental VDD and VSS metal bus resistances between adjacent I/O cells ($R1$ and $R2$ in Fig. 9.15) were extracted from layout and set to $0.2\ \Omega$. The incremental *esd_boost* and *esd_trigger* bus resistances (not shown) were 1.7 and $4.3\ \Omega$, respectively.

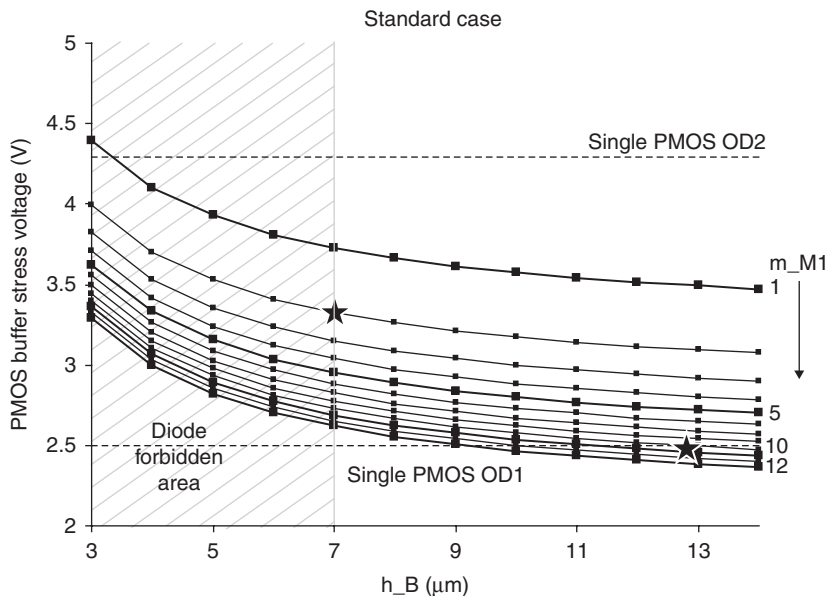
With the M1 clamp device limited to an integer number of rows, it was possible to take great advantage of response surface plots to accomplish the ESD network optimization. In contrast to other reported techniques (Torres *et al.*, 2001; Stockinger *et al.*, 2003, 2005), this response surface method (RSM) gave a full map of ESD network solutions for all various output buffer configurations (single OD2, single OD1, cascoded OD1) at once. It also allowed an analysis of trade-offs in ESD performance and relative ESD device layout area without further simulations. Two RSM plots were sufficient for the entire optimization task. The first plot (Fig. 9.17) shows the dependence of the NMOS buffer stress voltage in the stressed pad on h_A and m_{M1} while the second plot (Fig. 9.18) shows the dependence of the PMOS buffer stress voltage in the grounded pad on h_B and m_{M1} . The two plots are linked together by the common variable m_{M1} , which defines a family of curves in discrete steps from $m_{M1} = 1$ to $m_{M1} = 12$. The maximum diode current constraint of $8.5\ \text{mA}/\mu\text{m}$ and the peak current level of 3.8 A dictate a lower limit for the sizes of the ESD diodes h_A and h_B , as indicated by the shaded ‘forbidden’ areas on the left sides of Figs 9.17 and 9.18. The thick horizontal lines in these figures correspond to the buffer stress voltage targets for the various buffer configuration options of Table 9.1.

Each intersection of an RSM curve with one of these voltage target lines provides one $\{m_{M1}, h_A\}$ pair in Fig. 9.17 and another $\{m_{M1}, h_B\}$ pair in

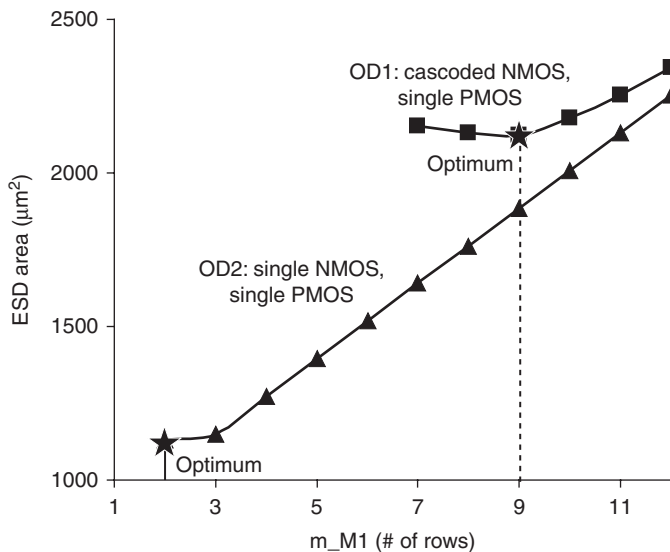


9.17 RSM for NMOS buffer stress voltage. (Source: Reproduced Fig 9, p 76, from 2005 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.)

Fig. 9.18. All of these pairs represent solutions that precisely meet the buffer stress targets of Table 9.1. If an intersection is located in the forbidden area where the diode would fail, one moves along the curve to the right until the boundary of the forbidden area is reached. In such cases the respective buffer stress voltage will then be slightly below target. By combining solution pairs of Figs 9.17 and 9.18 that have the same m_{M1} , one can calculate the total required ESD area and plot it over the variable m_{M1} (Fig. 9.19) to find the optimum m_{M1} for a given buffer configuration. The total ESD area ($h_{ESD} \cdot w_{I/O}$) includes the active device areas as well as the required inter-device spacing and area for metal routing. As can be seen in Table 9.1 and Fig. 9.17, the single OD1 NMOS buffer has such a low protection target that it cannot be protected with reasonably sized ESD devices. Therefore it is required to cascode OD1 NMOS and single OD1 PMOS output buffer transistors for 1.2 V I/O banks. According to Fig. 9.19, the total ESD area in the 1.2 V I/O pad cell was $2100 \mu\text{m}^2$ and the individual device sizes were $m_{M1} = 9$, $h_A = 8 \mu\text{m}$ and $h_B = 12.7 \mu\text{m}$. For the 2.5 V I/O banks, it is possible to easily protect single OD2 NMOS and PMOS output buffers. The total ESD area in the 2.5 V I/O pad cell was only $1100 \mu\text{m}^2$ and was achieved with $m_{M1} = 2$, $h_A = 10.5 \mu\text{m}$ and $h_B = 7 \mu\text{m}$. The optimum variable values for both the 1.2 V and 2.5 V I/O banks are highlighted using the star symbols in the RSM plots of Figs 9.17 and 9.18, as well as the ESD area plot



9.18 RSM for PMOS buffer stress voltage. (Source: Reproduced Fig 10, p 76, from 2005 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.)



9.19 ESD area as a function of clamp size for realistic OD1 and OD2 output buffer configurations. (Source: Reproduced Fig 11, p 77, from 2005 EOS/ESD Symp. Proc., by permission from EOS/ESD Association Inc.)

of Fig. 9.19. While it is difficult to make direct comparisons, this area is about 50% more than the area required for ESD devices in similarly configured bulk 2.5 V networks (Stockinger *et al.*, 2003, 2005). Nevertheless, this 2.5 V ESD network is very area efficient. Assuming ESD failure will occur at 3.8 A, the 1100 μm^2 area translates into an ESD layout area HBM efficiency of 5 V/ μm^2 , which is very high for SOI technologies. This network design has been implemented in a number of advanced SOI products and has shown exemplary ESD performance.

9.7 Conclusion

This chapter described key differences of ESD protection in SOI technologies as compared to bulk. It presented active rail clamp based SOI ESD protection network and design methodology including both device and circuit level characterization data. A compact model was introduced to describe the gated diode in the ESD regime. ESD characteristics of FinFETs, FinDiodes and FDSOI devices as likely device candidates for advanced SOI technologies were studied. A response surface method to conveniently optimize ESD device sizes depending on the output buffer configuration was presented. It was shown that, while slightly less area efficient than comparable bulk designs, distributed and boosted rail clamp SOI ESD networks are very compact and provide an effective ESD protection solution.

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Part II

Silicon-on-insulator (SOI) devices
and applications

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Silicon-on-insulator (SOI) metal oxide semiconductor field effect transistors (MOSFETs) for radio frequency (RF) and analogue applications

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Abstract: During the last decade, silicon-on-insulator (SOI) metal oxide semiconductor field effect transistor (MOSFET) technology has demonstrated its high frequency potential, reaching cut-off frequencies close to 500 GHz, and its suitability for commercial applications in harsh environments. For high-speed and radio frequency (RF) applications, strained Si and high-resistivity Si can be considered, respectively, to enhance carrier mobility and thus current and operation speed, and to minimize the RF substrate losses. Nowadays, substrate resistivity values higher than 5 k Ω .cm can easily be achieved and high-resistivity silicon is widely seen as a promising substrate for radio frequency integrated circuits and mixed-signal applications.

Key words: SOI, MOSFET, RF, Schottky barrier MOSFETs, ultra-thin body ultra-thin BOX (UTBB) MOSFETs, FinFETs, high-resistivity substrate, substrate effects, crosstalk, RF linearity, trap-rich high-resistivity SOI substrate.

10.1 Introduction

In the early 1970s, Dennard and co-workers¹ suggested a method for reducing the dimensions of metal oxide semiconductor field effect transistors (MOSFETs) to increase operating speed and the integration density of complex digital integrated circuits (ICs). Since then a key objective of the semiconductor industry has been the optimization of this scaling-down procedure.² The communication industry has been both a very challenging and profitable market for the semiconductor companies. Current communication systems are very demanding. Key requirements include:

- high frequency;
- a high degree of integration;
- the need to meet a range of standards;
- high linearity;
- low power consumption; and
- good performance even in harsh environments such as high temperature and/or radiation.

Modern transceivers often consist of three or four chip-set solutions combined with several external components. A reduction of the external components is essential to reduce cost, power consumption and weight. The analogue front-end requires high-performance technology, such as III–V compounds or silicon bipolar, for devices that can easily achieve operating frequencies in the gigahertz range. For the digital signal processor a small device size is essential for the implementation of complex algorithms. To satisfy both the digital and analogue/RF requirements of future communication systems, advanced submicron complementary MOS (CMOS) technology appears to be both a feasible and a cost-effective solution.

During the last decade, thanks to transistor and back-end downscaling, as well as the introduction of strained Si channels, MOS transistors have reached amazingly high operating speeds. Today the semiconductor industry considers Si-based CMOS as a mainstream technology for RF applications. In particular, silicon-on-insulator (SOI) MOSFET technology has demonstrated its potential for high frequencies (reaching cut-off frequencies close to 500 and 350 GHz, respectively, for n- and p-type MOSFETs³) and for commercial applications in harsh environments (high temperature, radiation). From its early development phase, SOI has grown from a mere scientific curiosity into a mature technology. Partially depleted (PD) SOI is now serving the 45 nm digital market on a massive scale, where it provides a high performance, low power alternative to bulk silicon. Fully depleted (FD) devices are also widespread, as they outperform existing semiconductor technologies for extremely low power analogue applications.⁴ For RF and system-on-chip (SoC) applications, SOI also presents the major advantage of providing high-resistivity substrate capabilities, leading to substantially reduced substrate losses and crosstalk between ICs implemented on the same chip. Substrate resistivity values higher than 5 k Ω .cm are on the market, and high-resistivity silicon (HRS) is commonly foreseen as a promising substrate for radio frequency integrated circuits (RFIC) and mixed-signal applications.⁵

In this chapter, based on experimental and simulation results, the applications and limitations – and also possible future improvements – of SOI MOS technology for microwave and millimetre-wave applications are presented.

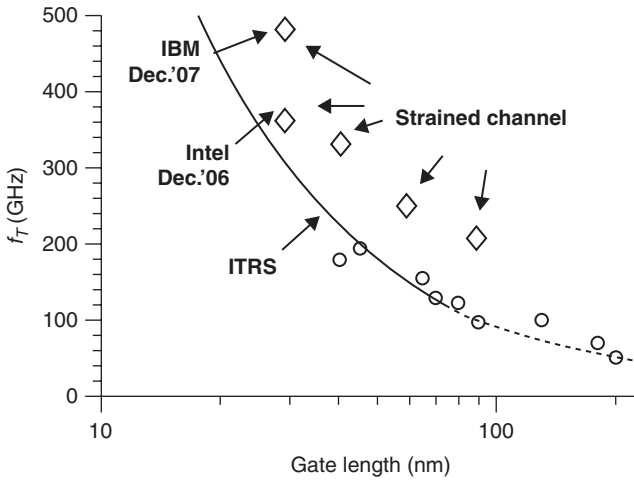
10.2 Current performance of RF devices

In 1958, a cut-off frequency in the gigahertz range was reached with a germanium bipolar transistor.⁶ In 1965, a gallium arsenide (GaAs) metal semiconductor field effect transistor (MESFET) was proposed in the literature⁷ and a maximum oscillation frequency (f_{\max}) of 100 GHz was measured for a FET⁸ in 1973. In 1980, a new FET architecture with high electron mobility (HEMT) was proposed and fabricated.⁹ f_{\max} higher than 500 GHz was achieved for a HEMT¹⁰ in 1995. In 2000, the limit of 1 terahertz was reached with a III–V heterostructure bipolar transistor (HBT),¹¹ and this was exceeded by a HEMT in 2007.¹²

The increase in the market of consumer electronics that employs RF circuits demands an optimized solution, not only from the point of view of performance, but also from the point of view of power consumption, cost and size. Handheld devices – smart phones, for instance – make it very important to integrate both the digital core and the high frequency core on one chip. This is where the interest in bipolar CMOS (BiCMOS) technology emerges. The low cost of SiGe BiCMOS compared with GaAs HBT technology is a key driver of the growing use of SiGe bipolar transistors in portable wireless systems requiring high-speed data transmission and small size. This has led to the system-on-chip (SoC) approach,¹³ and BiCMOS technology is the best candidate to satisfy this need. Today, BiCMOS technology using SiGe HBTs is the most widely used technology for ultra-high speed applications. BiCMOS devices provide continuously enhanced RF performance, with recent SiGe HBTs demonstrating a maximum oscillation frequency of 500 GHz.¹⁴ They are currently integrated into a 300 mm BiCMOS foundry for the 55 nm node.¹⁴ However, the need for low power consumption and low cost continues to drive debate on the use of pure CMOS technology for RF applications,¹⁵ justified by the continuous enhancement in the RF performance of MOSFET technology.

In 1996, thanks to the successful downscaling of the silicon MOSFET gate, cut-off frequencies higher than 200 GHz were demonstrated.¹⁶ Since that date, the interest in MOSFETs for low voltage, low power, high integration mixed-mode ICs in the field of microwave and millimetre-wave applications has grown constantly. MOSFET is a mature and cost-effective technology, ideal for mass production. Starting from the 90 nm technology node, CMOS has shown comparable cut-off frequencies and RF noise performance to state-of-the-art SiGe technology.¹⁵ Nowadays, thanks to the introduction of mobility boosters such as strained silicon channels, cut-off frequencies close to 500 and 350 GHz are achieved, respectively, for 30 nm gate-length n- and p-MOSFETs.³

Figure 10.1 presents the state-of-the-art current gain cut-off frequency (f_T) for n-type MOSFETs as a function of gate length, with the continuous

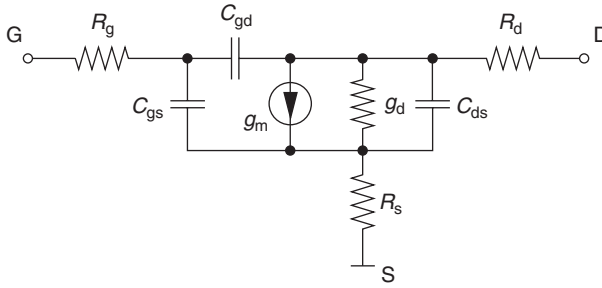


10.1 State-of-the-art current gain cut-off frequency (f_T) as a function of gate length for unstrained and strained Si and SOI nMOSFETs.

line being the prediction from the International Technology Roadmap for Semiconductors (ITRS) published in 2006.¹⁷ Despite the lower carrier mobility of electrons in silicon compared with III–V materials, silicon MOSFETs can be considered as a competitive technology for high frequency applications. As shown in Fig. 10.1, strained channel silicon MOSFETs can even exceed ITRS roadmap values, giving quite good prospects for silicon technology beyond the next 15 years.

10.3 Limiting factors in MOSFET performance

Historically, device scaling has been the primary path to improve productivity and performance of CMOS as well as to decrease the die cost. From the 100 nm node, CMOS technologies have been facing many significant technological challenges. In this context, the most critical issue is in the so-called short channel effects (SCE), which tend to degrade the subthreshold characteristic, increase the leakage current and lead to a threshold voltage roll-off with respect to channel length shrinkage. SCEs have been reported both theoretically and experimentally in the literature, and solutions have been proposed. However, only a few publications have dealt with the limitations or degradation of the high frequency characteristics of CMOS devices in relation to the downscaling of their channel length. Considering a classic small-signal equivalent circuit for MOSFET, as presented in Fig. 10.2, we can define the cut-off frequencies f_o , f_T and f_{max} , corresponding to the intrinsic (related to the useful MOSFET effect), the current gain and the available power gain cut-off frequencies, as



10.2 Small-signal lumped equivalent circuit of MOSFET.

$$f_c = \frac{g_m}{2\pi C_{gs}}, \quad [10.1]$$

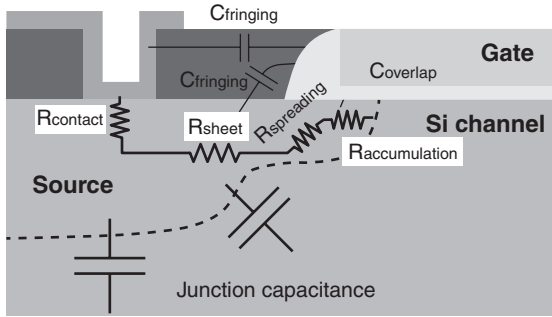
$$f_T \approx \frac{f_c}{\left(1 + (C_{gd}/C_{gs})\right) + (R_s + R_d)\left((C_{gd}/C_{gs})(g_m + g_d) + g_d\right)}, \quad [10.2]$$

$$f_{\max} \approx \frac{f_c}{2 \cdot \left(1 + (C_{gd}/C_{gs})\right) \sqrt{g_d (R_g + R_s) + (1/2)(C_{gd}/C_{gs})\left((R_s g_m) + (C_{gd}/C_{gs})\right)}}, \quad [10.3]$$

where g_m is the gate transconductance, g_d is the output conductance, C_{gs} , C_{gd} and C_{ds} are the gate-to-source, gate-to-drain and drain-to-source capacitances, respectively, and R_g , R_d and R_s are the gate, drain and source access resistances, respectively.

Figure 10.3 presents a schematic cross-section of a Si MOSFET where the different components of source and drain resistances and capacitances are illustrated.

The intrinsic cut-off frequency (f_c) measures the intrinsic ability of a field effect transistor to amplify high frequency signals. As reported by Dambrine *et al.*,¹⁸ the f_c values for HEMTs are approximately twice as high as for silicon MOSFETs with comparable gate length. That difference is mainly related to the low carrier mobility for Si compared to III–V semiconductors. In order to enhance the carrier mobility in the silicon channel and the current drive and high frequency characteristics³ of MOSFETs, strained n- and p-MOSFETs have been investigated in recent years. Beside the carrier mobility difference between Si and III–V materials, it has been demonstrated that the f_{\max}/f_T ratio is lower for Si devices. As explained by Dambrine *et al.*,¹⁸ besides the well-known degradation of high frequency



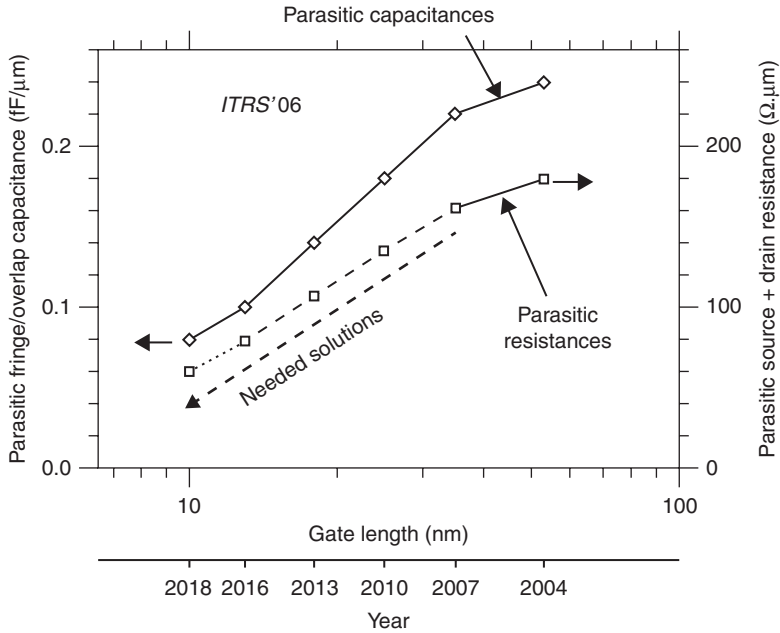
$$R_{\text{source}} = R_{\text{contact}} + R_{\text{sheet}} + R_{\text{spreading}} + R_{\text{accumulation}}$$

10.3 Schematic cross-section of a Si MOSFET illustrating the different access resistances to the channel and the surrounding overlap and fringing capacitances.

characteristics due to access resistances (R_g , R_d and R_s), the decrease of the ratios g_m/g_d and C_{gs}/C_{gd} in CMOS technology strongly contributes to the saturation of f_T and f_{max} with the reduction of the transistor channel length. The increase of the output conductance (g_d), with the reduction of gate channel length is one of the well-known short channel effects of FET devices. The degradation of the C_{gs}/C_{gd} ratio translates to loss of channel charge control by the gate and increases the direct coupling capacitance between the gate (input) and drain (output) terminals. Self-alignment of the source and drain regions, which is one of the main advantages of MOSFET architecture, also applies to the parasitic capacitances between source and gate and, more importantly, drain and gate. As demonstrated by Dambrine *et al.*,¹⁸ the C_{gs}/C_{gd} ratio is equal to 7.8 for the HEMT, but only 1.5–1.6 for a 90 nm MOSFET.

The impact of a lightly doped drain (LDD) dose and energy implant, as well as the effect of annealing temperature and time, on C_{gs}/C_{gd} ratio, g_m and g_d and hence on f_{max} , has been investigated.¹⁹ The results demonstrate that an LDD implant can be optimized to improve f_{max} and, especially, the $G_{\text{ass}}/\text{NF}_{\text{min}}$ ratio (G_{ass} and NF_{min} being, respectively, the associated power gain and the minimum RF noise figure), which is most important for low noise microwave applications. However, the optimization window is quite narrow and it seems to be difficult for a given technological node to achieve C_{gs}/C_{gd} and g_m/g_d ratios higher than 2 and 6, respectively, for a classical sub-100 nm gate-length MOSFET structure. To further improve the microwave performance of deep sub-micrometre MOSFETs, it is crucial to minimize the parasitic resistances and capacitances, as illustrated in Fig. 10.4.¹²

Several technological options have been presented in the literature in recent years to push further the digital and analogue performance limits of single gate Si MOSFETs, such as:



10.4 Parasitic capacitances and source and drain resistances as a function of the gate length published in ITRS'06.¹⁷

- Moving from bulk Si MOSFETs to partially depleted²⁰ or fully depleted²¹ SOI MOSFETs to enhance the electrostatic coupling between the gate electrode and the channel carriers, and thus minimize the SCE. Nowadays, ultra-thin body (UTB) MOSFETs in SOI technology with a silicon body thickness less than 10 nm have been proposed.^{22,23} Thanks to the buried oxide layer (BOX) beneath the SOI transistors, their junction capacitances to the Si substrate (see Fig. 10.3) are drastically reduced.
- Strained MOSFETs have been much investigated to improve the carrier mobility. The mechanical stress in the channel originates from specific process steps of the standard CMOS process flow.²⁴ Strained SOI wafers are now available on the market, with values ranging from 1 to 2 GPa, where the top silicon layer is under biaxial tensile stress.^{25,26}
- Low Schottky barrier contacts^{27–31} are seen as a very interesting candidate for lowering source/drain (S/D) contact resistances, and to form abrupt junctions (with no overlap capacitance) and drastically reduce the thermal budget of the CMOS process.
- Metal gates removes the loss of electrostatic gate control related to the polysilicon (poly-Si) gate depletion,^{32,33} as well as reducing the gate sheet resistance (lower R_g).

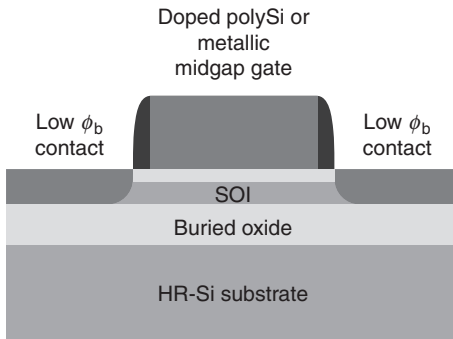
- Low-k dielectrics and air gaps^{34,35} can be introduced to reduce fringing capacitances between gate-to-source and gate-to-drain electrodes (lower parasitic gate capacitances) and to minimize the distributed capacitance and thus the delay time associated with the interconnection lines (back-end).
- SOI wafers with thin BOX have been proposed in recent years to reduce SCE (for instance, drain induced barrier lowering – DIBL) but also to lower self-heating issues.^{22,23,36,37}
- High-resistivity silicon substrate has demonstrated superior characteristics for the integration of high quality passive elements, such as transmission lines³⁸ and inductors,³⁹ as well as for the reduction of the crosstalk between circuit blocks integrated on the same silicon chip.⁵

This last point will be developed in detail in Section 10.7 Sections 10.4–10.6 present the static and high frequency characteristics of three advanced MOSFET architectures, respectively: low Schottky barrier (SB) ultra-thin SOI MOSFETs, ultra-thin body and BOX (UTBB) MOSFETs and FinFETs.

10.4 Schottky barrier (SB) MOSFETs

Schottky barrier MOSFETs with metal source/drain combine low extrinsic resistances with superior scalability.⁴⁰ However, the SB formed at the metal/channel interfaces results in an electrical performance inferior to conventional MOSFETs. Indeed, SB-MOSFETs suffer from low ON current, an ambipolar switching behaviour and a poor subthreshold swing. Simulations have demonstrated that SB-MOSFETs presenting a SB lower than 0.1 eV can outperform conventional MOSFETs.^{41,42} In addition to the use of specific silicides, which presents a low SB height to either holes or electrons,^{43,44} dopant segregation (DS) is a promising solution to lower the effective SB (eSB).^{45,46} A thin, highly doped layer, formed at the silicide/silicon interface during silicidation, causes strong band bending at the interface. As a consequence, the probability of carriers tunnelling through the effectively lowered SB is significantly increased. This technique can thus facilitate a reduction of the eSB at the NiSi/Si interface from 0.65 to <0.1 eV, depending on the implantation dose.⁴⁷

An f_T of 280 GHz has been obtained for 22 nm devices using PtSi⁴⁸ and 180 GHz for 30 nm MOSFETs when combining PtSi with DS.^{30,49} The gate-length dependence of the drain current and the RF characteristics of p- and n-type SB-MOSFETs with DS are studied by Urban *et al.*⁵⁰ The impact of the SB height on the electrical performance of n-type NiSi SB-MOSFETs with DS using different As implantation doses, presented by Urban *et al.*,⁵¹ is summarized below. The key device parameters are extracted from scattering-parameter (S-parameter) measurements using a



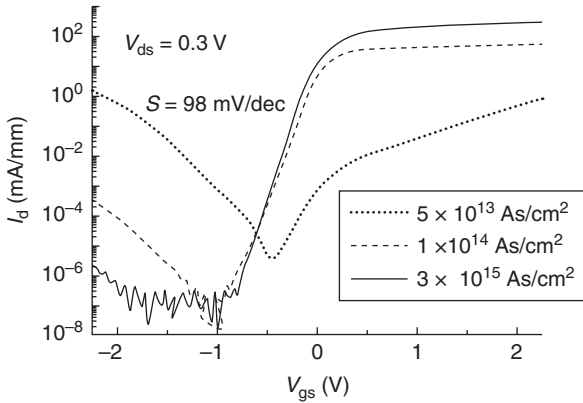
10.5 Schematic cross-section view of an ultra-thin SB SOI MOSFET on a high-resistivity Si substrate.

small-signal equivalent circuit, and are compared with SB-MOSFETs with different SB heights.

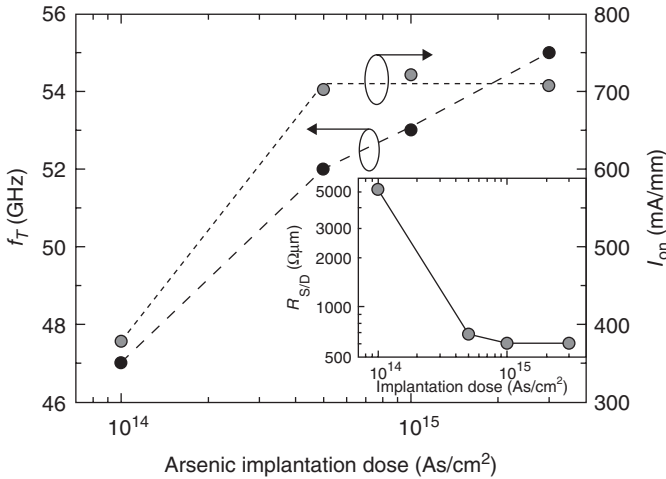
SB-MOSFETs with channel lengths (L_g) from 80 to 380 nm are fabricated on 20 nm thick, undoped SOI substrate (intrinsic channel doping of $5 \times 10^{14} \text{ cm}^{-3}$). A 3.5 nm thick SiO_2 gate oxide is grown, followed by deposition of 160 nm thick n+ poly-Si. For S/D implantation, doses ranging from 5×10^{13} to $3 \times 10^{15} \text{ As/cm}^2$ are used at an energy of 5 keV. The initial Si layer is fully silicided at 450°C for 30 s, and the NiSi encroaches under the spacer to the edge of the gate stack during the silicidation step. The unreacted Ni is selectively removed in an SPM solution ($\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2 = 4:1$). A schematic of the SOI SB-MOSFET is shown in Fig. 10.5. SB-MOSFETs consisting of two parallel gate fingers with a total gate width of $W_G = 2 \times 40 \mu\text{m}$ are embedded in coplanar waveguide (CPW) transmission lines for on-wafer microwave measurements.

Figure 10.6 shows the transfer characteristics of SB-MOSFETs ($L_g = 180 \text{ nm}$) with DS for different As doses. The devices exhibit typical ambipolar switching.⁵² For negative gate voltage (V_{gs}), holes tunnel through the drain-side (as defined for an nFET) barrier into the channel, resulting in the p-branch, whereas for positive V_{gs} , electrons are injected through the source-side barrier for the n-branch. In the case of the SB-MOSFET with the lowest dose of $5 \times 10^{13} \text{ As/cm}^2$, we observe almost equal ON currents for the p- and n-branches, indicating that the eSB for electrons is still close to the original value, whereas a significantly reduced p-branch is observed for devices with higher dose. Moreover, the n-branch ON current is drastically improved, by more than two orders of magnitude, between the lowest and the highest dose, and the inverse subthreshold slope gets steeper with higher As concentration.

This improved gate control is related to the higher tunnelling probability through the effectively lowered SB for higher implantation doses. Whereas the current flow of SB-MOSFETs with a high SB is limited by the carrier injection through the source SB, which is modulated by V_{gs} , it is mainly controlled



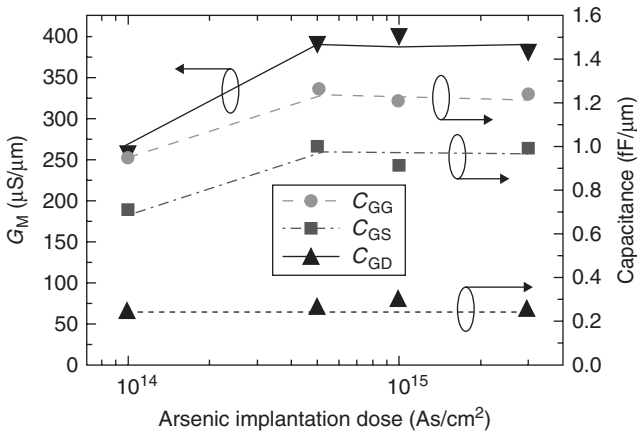
10.6 Transfer characteristics of SB-MOSFETs with DS using different As doses from 5×10^{13} to 3×10^{15} As/cm² ($L_g = 180$ nm).⁵¹



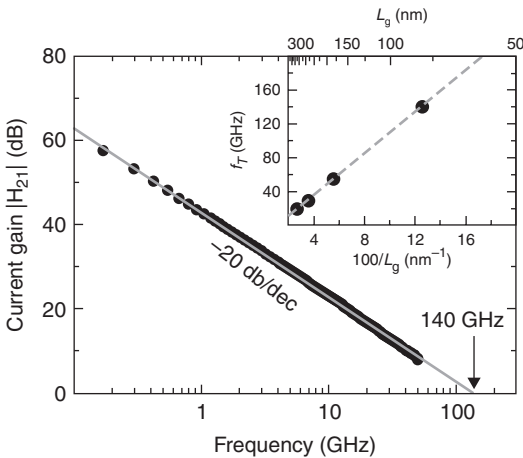
10.7 Unity-gain cut-off frequency, f_T and saturation current, I_{on} ($V_{gs} - V_{th} = 1.5$ V, $V_{ds} = 1.5$ V), of the 180 nm channel devices vs As implantation dose.⁵¹

by the potential barrier in the channel if the SB is lowered, and the tunneling probability approaches unity.^{52,53} Using dedicated on-wafer open test-structures to de-embed the CPW pads and feed lines, Cold-FET S-parameter measurements,⁵⁴ i.e. when the transistor is biased in off-state, show a strong decrease of the extrinsic resistance, $R_{S/D}$, from 5.2 k $\Omega \cdot \mu\text{m}$ down to 600 $\Omega \cdot \mu\text{m}$ as As dose increases from 1×10^{14} to 3×10^{15} As/cm² (i.e., with decreasing eSB (inset Fig. 10.7)).

Figure 10.7 shows f_T and the saturation currents, I_{on} ($V_{gs} - V_{th} = 1.5$ V, $V_{ds} = 1.5$ V), of 180 nm channel devices. Note that, although I_{on} varies by a factor of approximately two between the lowest and the highest dose, a change of only 17% is evident for f_T . Figure 10.8 shows extrinsic gate transconductance, G_M , and the total gate-to-source, C_{GS} , gate-to-drain, C_{GD} , and channel capacitance, $C_{GG} (= C_{GS} + C_{GD})$, which are extracted for the same 180 nm channel devices at peak f_T bias (see Fig. 10.7^{31,55}). G_M , as well as C_{GS} and C_{GG} , improve when the



10.8 Maximum extrinsic transconductance, G_M , as well as C_{GS} and C_{GG} extracted at peak f_T biases.⁵¹



10.9 Current gain vs frequency for n-type SB-MOSFETs with $L_g = 80$ nm (3×10^{15} As/cm²) showing a cut-off frequency of 140 GHz at $V_{gs} - V_{th} = 0.34$ V and $V_{ds} = 1.2$ V. The inset shows the linear dependence of peak f_T vs $1000/L_g$.⁵¹

implantation dose is increased from 1×10^{14} to 5×10^{14} As/cm², whereas C_{GD} remains constant at a value of 0.25 fF/ μ m. The increase of G_M with the As dose is explained by the drastic reduction of S/D resistances thanks to the decreasing eSB. At the same time we get a higher value of C_{GG} , due to the probability of carriers tunnelling through the lower eSB being significantly enhanced, resulting in an increased amount of charge being injected into the channel. Since the cut-off frequency is given by $f_T \approx G_M / (2\pi C_{GG})$, it varies only slightly for different As doses due to the similar dependence of G_M and C_{GG} on the SB. As a result, although the SB strongly deteriorates the DC performance, it has only limited impact on the RF performance of SB-MOSFETs.

A cut-off frequency of 140 GHz is extracted at $V_{gs} - V_{th} = 0.34$ V and $V_{ds} = 1.2$ V for n-type SB-MOSFETs, which is the highest value reported so far (Fig. 10.9). The inset shows a perfect $1/L_g$ dependence of f_T for L_g from 380 to 80 nm, suggesting an impressive RF performance increase when the device is further scaled down.

10.5 Ultra-thin body ultra-thin BOX (UTBB) MOSFETs

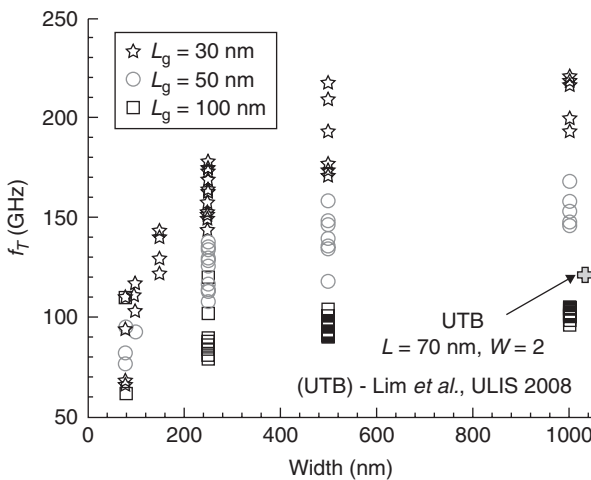
Ultra-thin body (UTB) ultra-thin BOX (UTBB, UTBOX or UTB2) SOI MOSFETs are widely considered to be amongst the most promising candidates for the ultimate device scaling required by ITRS,⁵⁶ thanks to their immunity to short channel effects.^{57–66} Employment of ultra-thin buried oxide (BOX) allows the suppression of fringing electric fields, thus further improving SCE control, reducing drain induced barrier lowering and sub-threshold slope.^{63–65,67} Simulations predict a reduction of the self-heating effect (SHE) in MOSFETs with thin BOX.^{68–70} Additionally, ultra-thin BOX enables the use of back-gate control schemes.^{59,61} Different back (or ground) planes (BP/GP) and substrate biasing have been shown to have the capability of multi-threshold voltage (V_{th}) and dynamic- V_{th} options within the same process.⁵⁹

However, the drawback of ultra-thin BOX is enhanced coupling through the substrate. Such coupling may degrade both the static behaviour^{63–65} and the frequency response of these devices,^{70,71} depending on the substrate–BOX interface space charge conditions.^{63–65,70–72} This provides additional motivation for the use of a ground plane, which helps to suppress fringing fields through the substrate.^{67,70,73}

Kilchytska *et al.*⁷⁴ presented a first assessment of UTBB technology for analogue applications. This paid particular attention to drive current, maximum transconductance, early voltage and intrinsic gain, as well as their variation with substrate bias, channel width and temperature (range up to 250°C). Measured UTBBs have been benchmarked with other devices and technologies, such as FD SOIs, UTBs and different FinFETs. We summarize below the measured RF performance of those UTBBs.

The devices are processed at CEA-Leti on the UNIBOND (100) SOI wafers with 10 nm thick BOX.⁶¹ In the channel region, the Si body is thinned down to about 7 nm. Elevated source/drain structures are employed to reduce parasitic resistance. There is no channel doping, and there is no ground plane underneath the BOX. The gate stack consists of HfSiON with an equivalent oxide thickness (EOT) of 1.3 nm and a TiN gate electrode. More process details can be found in Andrieu *et al.*⁶¹ The measured devices are n-channel MOSFETs with a gate length, L_g , from 30 nm to 10 μm and a channel width, W , from 80 nm to 10 μm .

Figure 10.10 presents current gain cut-off frequencies (f_T), for n-type UTBB MOSFETs with different values of L_g and W . It is worth pointing out that this process is not specially optimized for RF applications. Nevertheless, f_T values as high as 170 and 220 GHz, respectively, are achievable with 50 nm and 30 nm long UTBB devices. These numbers are in excess of previously reported f_T values of ~ 120 GHz with a 70 nm long UTB MOSFET,^{66,75} but are in line with them, taking into account the shorter L_g in the UTBB devices studied here. The f_T values of UTBB devices are also a bit higher than those previously reported for FinFETs with similar L_g .^{76,77} Nevertheless, these values, while being close to, are still lower than ITRS requirements and certainly lower than the best reported f_T values (>450 GHz) for 30 nm long PD SOIs⁷⁸). However, it should be noted that the highest reported f_T numbers were obtained with targeted high-performance (HP) processes and designs. On the other hand, the UTBB devices presented here are able to provide not only relatively high f_T , but also low V_{th} and excellent DIBL, I_{off} and I_{on}/I_{off}



10.10 f_T for n-type UTBB devices with different widths and lengths. The cross shows the value previously reported⁶⁶ for UTB MOSFET with $L_g = 70$ nm, $W = 2$ μm .⁷⁴

values, thus showing great promise for applications requiring low operation voltage (LOP) and/or low standby power (LSTP).

The decrease of f_T with channel width is related to the increased effect of parasitics (especially fringing capacitances) which appear with channel narrowing in multi-channel, multi-finger devices (as required for RF).⁷⁹ Complete equivalent circuit extractions confirm this hypothesis.

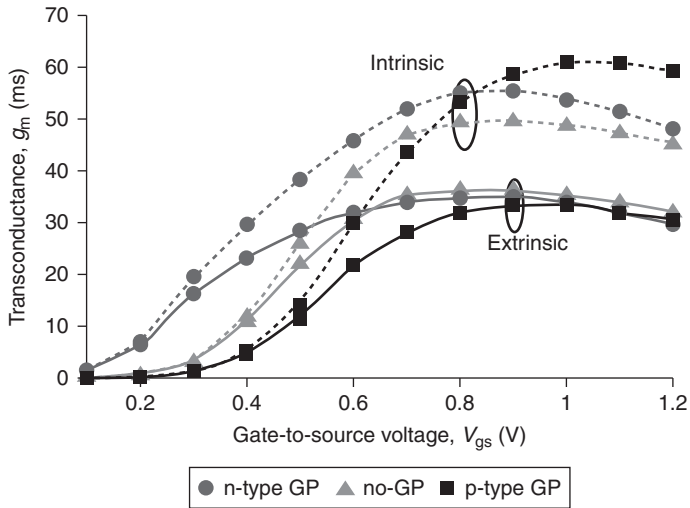
Kilchytska *et al.*,⁷⁴ in their comparison with other technologies, including both FD SOIs and different FinFETs, revealed that UTBB devices approach (and can even outperform, in the case of narrow UTBB channels) ‘optimized FinFETs’ in terms of both maximum transconductance and intrinsic gain, thus making them particularly attractive for high-precision analogue applications. Very limited degradation of both digital and analogue figures-of-merit was observed in temperatures up to 250°C.

For UTBBs without a ground plane, both self-heating and substrate-related degradations (with the latter possibly exceeding the former) have been shown experimentally to appear in output conductance with frequency. Thus, in considering wide-frequency range applications, it is important to note that performance prediction based on DC data alone may result in inaccurate evaluation. While the process is not specially optimized for RF applications, cut-off frequencies as high as 170 and 220 GHz are achievable for 50 nm and 30 nm long UTBB MOSFETs, respectively, making them a good contender for mobile/wireless applications requiring LOP/LSTP options.

As demonstrated by Arshad *et al.*,⁶⁵ ground-plane implementation below the BOX suppresses the effect of substrate depletion which prevents the thin BOX from losing its advantage. Thus, the applications of GP and substrate are important in providing optimum electrostatic control of UTBB devices. RF performance comparison for UTBB devices with and without substrate ground planes (n- and p-type GPs) was investigated in Arshad *et al.*⁸⁰

Figure 10.11 shows the extrinsic and intrinsic (removal of access resistances) gate transconductance (g_m) extracted from measured S-parameters. A significant increase of maximum intrinsic g_m compared to extrinsic g_m is observed for the devices with GP. The increase is almost 50% for UTBB devices on substrate with GP compared to about 25% for the device without GP. As previously explained, this indicates that if parasitic resistances are reduced, significant improvement of g_m can be achieved, especially for short gate lengths (Tables 10.1 and 10.2) that later directly translate to higher f_T and f_{max} (Fig. 10.12), since GP has no significant impact on the UTBB capacitances.

Different doping profiles underneath the BOX have been experimentally tested⁸⁰ and no increase in high-frequency parasitic capacitance to the substrate has been recorded. Significant improvement of intrinsic f_T can be achieved for UTBB devices with GP substrate.



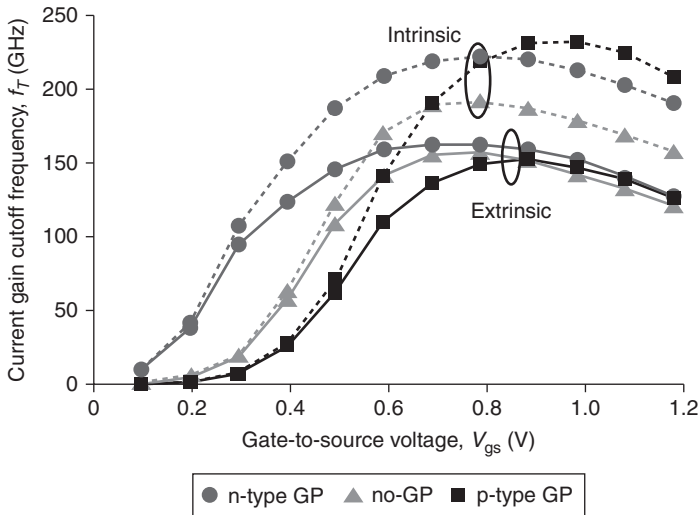
10.11 Intrinsic and extrinsic g_m for $L_g = 30$ nm extracted from measured S-parameters. The intrinsic and extrinsic g_m correspond to the real part of the gate-to-drain admittance of the transistor electrical equivalent circuit when parasitic resistances, that is, R_g and R_{sdr} , are removed or not, respectively.⁸⁰

Table 10.1 Extracted small-signal equivalent circuit lumped parameters for $W_f = 500$ nm (transistor width for one gate finger) and $N_f = 80$ (number of gate fingers) for UTBB built on top of a p-type GP substrate at $V_{ds} = 1.0$ V and V_{gs} value at the maximum gate transconductance⁸⁰

nm	Ω		fF		mS			
L_g	R_g	R_{sd}	C_{ds}	C_{gg}	g_m	g_d	g_m/g_d	C_{gs}/C_{gd}
30	47.8	25.2	32.6	41.0	61.3	9.0	6.8	2.1
50	23.1	21.9	23.3	54.4	56.4	6.0	9.4	2.3
100	8.6	21.5	16.1	79.0	46.0	4.1	11.3	3.4

Table 10.2 Extracted small-signal equivalent circuit lumped parameters for $W_f = 500$ nm (transistor width for one gate finger) and $N_f = 80$ (number of gate fingers) for UTBB built on top of an n-type GP substrate at $V_{ds} = 1.0$ V and V_{gs} value at the maximum gate transconductance⁸⁰

nm	Ω		fF		mS			
L_g	R_g	R_{sd}	C_{ds}	C_{gg}	g_m	g_d	g_m/g_d	C_{gs}/C_{gd}
30	37.1	15.5	43.9	40.3	55.4	10.1	5.5	2.2
50	24.0	12.5	22.0	51.6	55.3	6.5	8.6	2.6
100	9.9	11.7	17.2	77.6	48.4	5.1	9.6	3.6



10.12 Intrinsic and extrinsic f_T for $L_g = 30$ nm extracted from measured S-parameters and when the parasitic resistances, that is, R_g and R_{sd} , are withdrawn or not, respectively.⁸⁰

10.6 RF performance of a multi-gate MOSFET: fin-on-oxide field effect transistor (FinFET)

Thanks to the simultaneous control of the channel by more than one gate, multiple-gate architectures emerge as one of the most promising novel device structures to reduce the SCE in nanometre scale MOSFETs.⁸¹ Besides the FinFET architecture,⁸² there are a myriad of other multiple-gate MOSFET structures,⁸³ such as triple-gate (TG), pi-gate (PG), quadruple-gate (QG), omega-gate (Ω -G), and so on. Several published articles have demonstrated the great potential of multiple-gate devices to comply with the I_{on}/I_{off} requirements of the ITRS for logic operation^{83,84} due to their high immunity to SCE and excellent compatibility with planar CMOS processes. Most of the investigations performed on FinFETs have focused on their technological aspects and perspectives for digital applications,^{85,86} while only a few have assessed their analogue values.^{87,88} In this section, the RF performance of FinFETs with various geometries is presented.

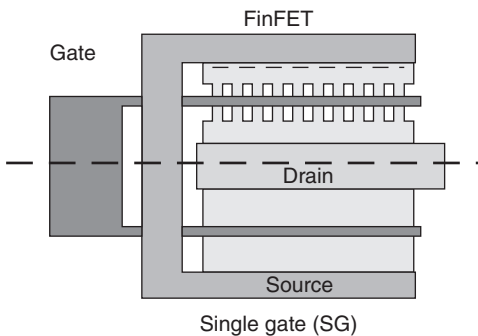
FinFETs with gate length (L_g) of 40, 60 and 120 nm are fabricated on a SOI wafer with a 60 nm thick Si film on 145 nm of buried oxide, with (100) and (110) Si planes for top and lateral channels, respectively. The silicon active area is patterned using 193 nm lithography with aggressive resist and oxide hard mask trimming to define narrow silicon fins. A hydrogen anneal with sidewall oxidation is used for surface smoothing and corner rounding. The fin patterning results in a fin height (H_{fin}) of 60 nm, fin widths (W_{fin}) of

22, 32 and 42 nm and fin spacing (S_{fin}) of 328 nm. The gate stack consists of a plasma nitrated oxide with EOT equal to 1.8 and 100 nm of polysilicon. High angle As/BF₂ extensions are then implanted, and a 40 nm thick selective epitaxial growth (SEG) is performed on the source and drain regions. After heavily doped drain (HDD) implantations and rapid thermal annealing (RTA), NiSi is used as silicide, and only one metal layer is deposited to define the contacts.

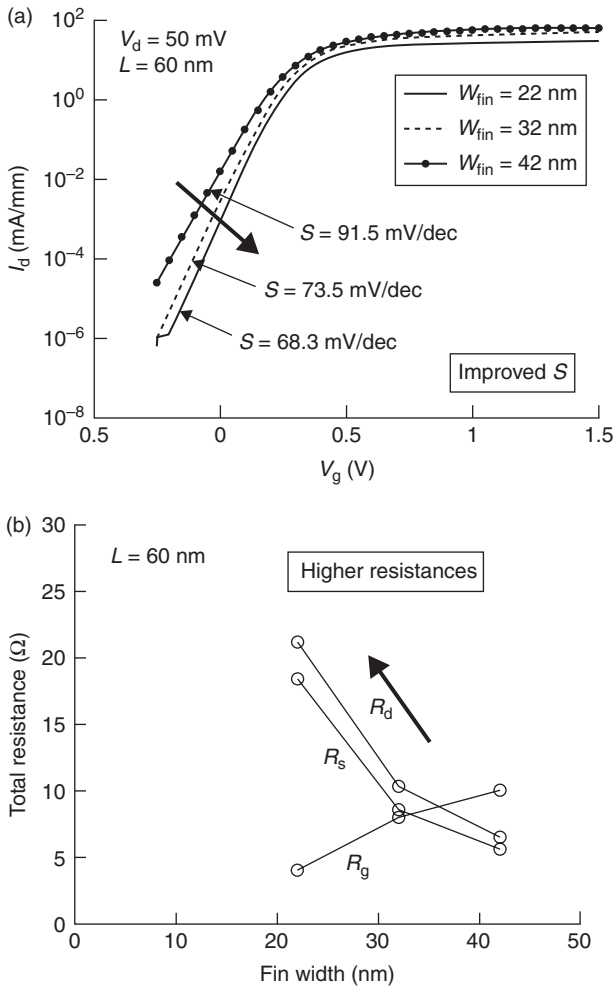
The DC and RF measurements are performed on FinFETs (Fig. 10.13) composed of 50 gate fingers (N_{finger}) each controlling 6 fins (N_{fin}). As shown in Fig. 10.14a, the 60 nm technology investigated here shows good control over SCE, with a subthreshold slope (S) close to 73.5 mV/dec. No threshold voltage (V_{th}) roll-off is observed with respect to L_g ($V_{\text{th}} \sim 260$ mV) and only small V_{th} variations (within 30 mV) are recorded as a function of W_{fin} . As expected, the devices also exhibit reduced SCE; for instance, lower S (Fig. 10.14a) as the fin width is reduced. However, an increase of the source (R_s) and drain (R_d) resistances⁸⁹ is associated with the narrowing of the fin width W_{fin} , as shown in Fig. 10.14b, which leads to a reduction of the normalized drain current, as well as the effective gate transconductance (Fig. 10.14c).

The current gain ($|H_{21}|$) as a function of frequency, which yields the device transition frequency (f_T), is presented in Fig. 10.14d for FinFETs of different fin widths. A reduction of the cut-off frequency with the shrinkage of W_{fin} is clearly observed. This degradation is mainly related to the increase of the source and drain resistances with the thinning down of the fin width (Fig. 10.14b).

The DC and RF performances of planar partially depleted SOI MOSFETs with similar dimensions built on the same wafer (Fig. 10.13) have been measured for comparison purposes. Figure 10.15 presents the extracted cut-off frequencies of planar and FinFET devices as a function of channel length.

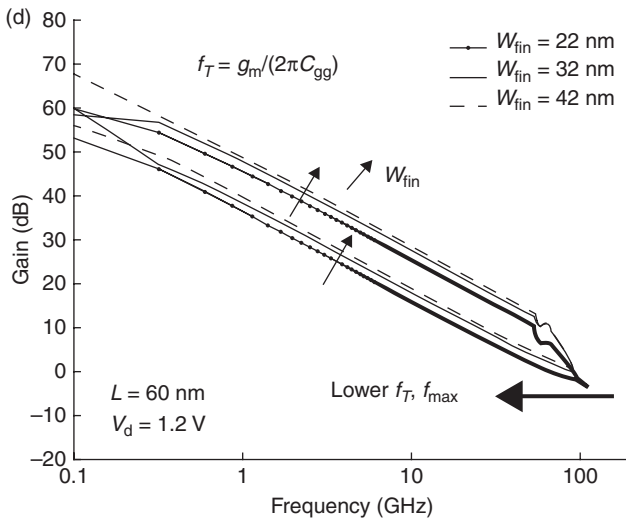
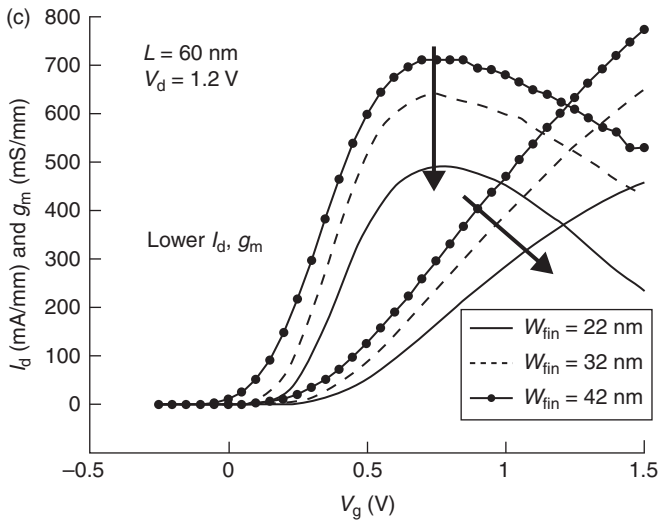


10.13 Schematic top view of a FinFET composed of 10 fins (upper) and planar (single gate (SG)) partially depleted SOI MOSFET (lower) occupying the same active silicon foot print.



10.14 DC and RF characteristics of 60 nm gate-length FinFET for various fin widths (W_{fin}): (a) transfer characteristic in log scale; (b) extracted access resistances; (c) transfer characteristic in linear scale and gate transconductance; (d) current gain and maximum available power gain vs frequency (the three bottom curves correspond to current gain and the three top curves correspond to maximum available power gain). Data are normalized by considering the total gate width $W_{tot} = N_{finger} N_{fin} (W_{fin} + 2H_{fin})$.

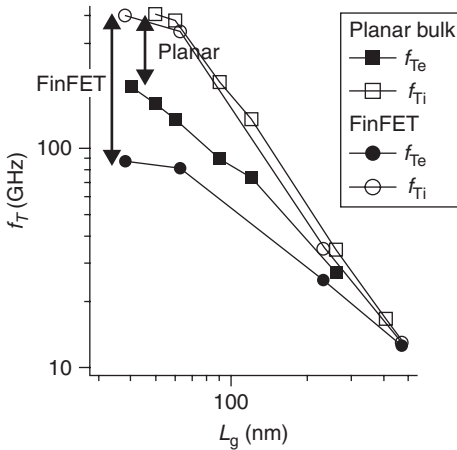
The so-called intrinsic (f_{Ti}) cut-off frequencies are the current gain cut-off frequency related only to the intrinsic lumped parameter elements (g_m , g_d , C_{gsi} and C_{gdi}). The extrinsic (f_{Te}) cut-off frequencies relate to the complete small-signal equivalent circuit presented in Fig. 10.2, including the parasitic capacitances, C_{gsc} and C_{gde} , as well as the access resistances R_s , R_d and R_g . It is



10.14 (Continued)

worth noting that both devices present similar intrinsic cut-off frequencies (around 400 GHz for a channel length of 60 nm) but the extrinsic cut-off frequency (f_{Te}) of the FinFET (90 GHz) is nearly half that of the planar MOSFET (180 GHz).

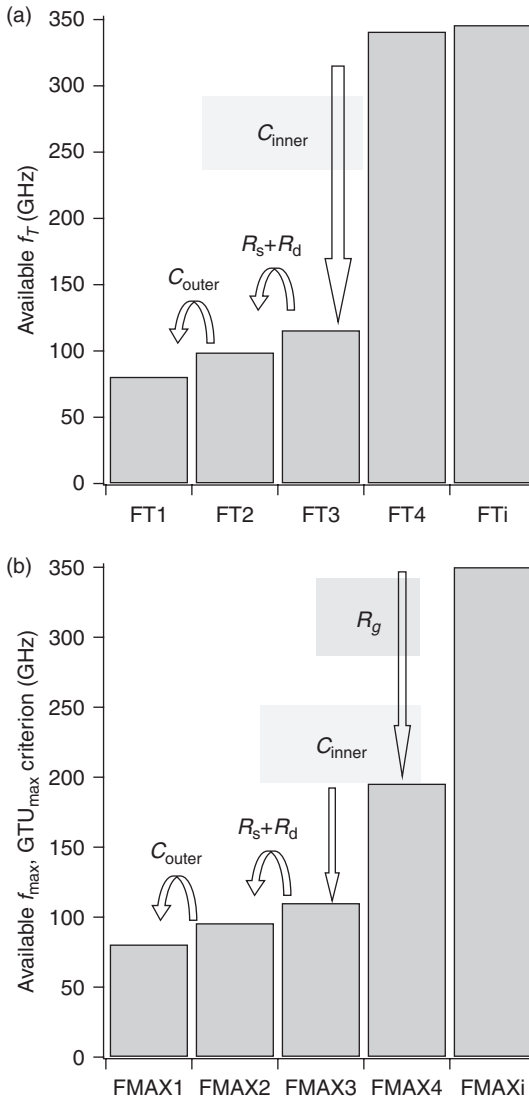
Based on a wideband analysis, the lumped small-signal equivalent circuit parameters (Fig. 10.2) are extracted from the measured S-parameters according to the methods described elsewhere.^{54,90} Figure 10.16 shows the relative impact of each parasitic parameter on current gain (f_T , Fig. 10.16a)



10.15 Extracted intrinsic (f_{Ti}) and extrinsic (f_{Te}) current gain cut-off frequencies for a SG PD SOI MOSFET and FinFET as a function of the channel length.

and maximum available power gain (f_{max} , Fig. 10.16b) cut-off frequencies of a 60 nm long FinFET. As expected from expressions [10.1]–[10.3] and the published results for single gate (SG) PD SOI MOSFETs,⁹¹ gate resistance has an important impact on f_{max} , whereas f_T is unchanged. The sum of fringing capacitances, C_{inner} , directly linked to the FinFET three-dimensional (3-D) architecture has a huge impact on both cut-off and maximum frequencies. In fact, f_T and f_{max} reduce by factors of 3 and 2 respectively. Finally, the source and drain resistances, as well as the parasitic capacitances related to the interconnection lines outside the active area of the transistor, slightly decrease both cut-off frequencies. Based on this analysis, it is quite clear that the fringing capacitances inside the active area of the FinFET are the most important limiting factor for this type of non-planar multiple-gate transistor.

In Reference 92, Wu and Chan analyse the geometry-dependent parasitic capacitances in multifin FinFETs. Parasitic fringing capacitance and overlap capacitance are physically modelled as a function of gate geometry parameters using the conformal mapping method. The relative contribution from each part of the 3-D geometry of the FinFET is calculated. They demonstrate the importance of the fringing capacitance which originates from the capacitive coupling between the source and drain regions of the fins (side walls) and the gate electrode located between the fins which assures the electrical connection between the gates, wrapping the different fins connected in parallel through the source and drain contacts. In References 93 and 94, using finite-element numerical simulations, the authors have demonstrated the possibility of reducing C_{inner} and its impact on the FinFET cut-off frequencies by reducing the fin spacing or by increasing the aspect ratio of the fin (higher H_{fin}/W_{fin}).



10.16 Relative impact of each lumped extrinsic parameters on (a) the current gain cut-off frequency (f_T) and on (b) the maximum available gain cut-off frequency (f_{max}) for a 60 nm long FinFET.

To summarize, simulation and experimental results indicate that a FinFET is a multiple-gate structure of interest in reducing digital short channel effects and assuring a lower threshold voltage roll-off, a better subthreshold slope and a higher I_{on}/I_{off} ratio. However, the high-frequency performance, such as the cut-off frequencies, and the RF noise figure, as presented by Raskin

et al.,⁹⁵ are degraded compared to its planar PD SOI MOSFET counterpart. This is due to the increased fringing capacitance linked to its complex 3-D non-planar architecture. Consequently, a trade-off exists between high f_T and f_{\max} (large W_{fin}) and good control of SCE (small W_{fin}).

10.7 High-resistivity silicon (HR-Si) substrate for SOI technology

After presenting the evolution of the SOI MOSFET technology, this section focuses on the high-frequency properties of the SOI substrate on top of which all the transistors previously described are implemented. The small- and large-signal behaviour of the SOI substrate is investigated by measuring the insertion loss and the generated harmonics along a CPW transmission line, and two metallic pads spaced by few tens of micrometres are designed to measure the parasitic coupling, named crosstalk, between devices and circuits implemented on the same chip.

10.7.1 CPW transmission lines

High-resistivity silicon (HR-Si) substrate is essential to reduce as far as possible the high-frequency losses associated with substrate conductivity. However, due to the problems related to latch-up between devices, HR-Si cannot be easily introduced into bulk Si MOSFETs. In SOI technology the thin top silicon layer, in which the transistors are implemented, is electrically isolated from the Si substrate by the BOX. HR-Si can, therefore, be introduced without impacting the good behaviour of the MOS ICs. Recently, high quality coplanar waveguides showing insertion losses of less than 2 dB/mm at 200 GHz, as well as low- and high-pass filters at millimetre-wavelength, have been successfully built in an industrial SOI CMOS process environment.⁹⁶

The insertion loss of a CPW line lying on a lossy silicon substrate depends on the conductor loss (α_{cond}) and the substrate loss (α_{sub}), which is inversely proportional to its effective resistivity. The effective resistivity represents the value of the substrate resistivity that is actually seen by the coplanar devices. This parameter accounts for wafer inhomogeneities (i.e., oxide covering and space charge effects) and corresponds to the resistivity that a uniform (without oxide or space charge effects) silicon wafer should have in order to sustain identical RF substrate losses. The effective resistivity is extracted from the measured S-parameters of the CPW line using the method described by Lederer and Raskin.⁹⁷ In the works by Lederer and Raskin^{97,99} and Lederer *et al.*⁹⁸ the authors demonstrated that HR-Si with an effective resistivity (ρ_{eff}) higher than 3 k Ω .cm can be considered as a quasi-lossless substrate. HR-Si substrates with a resistivity of 5–10 k Ω .

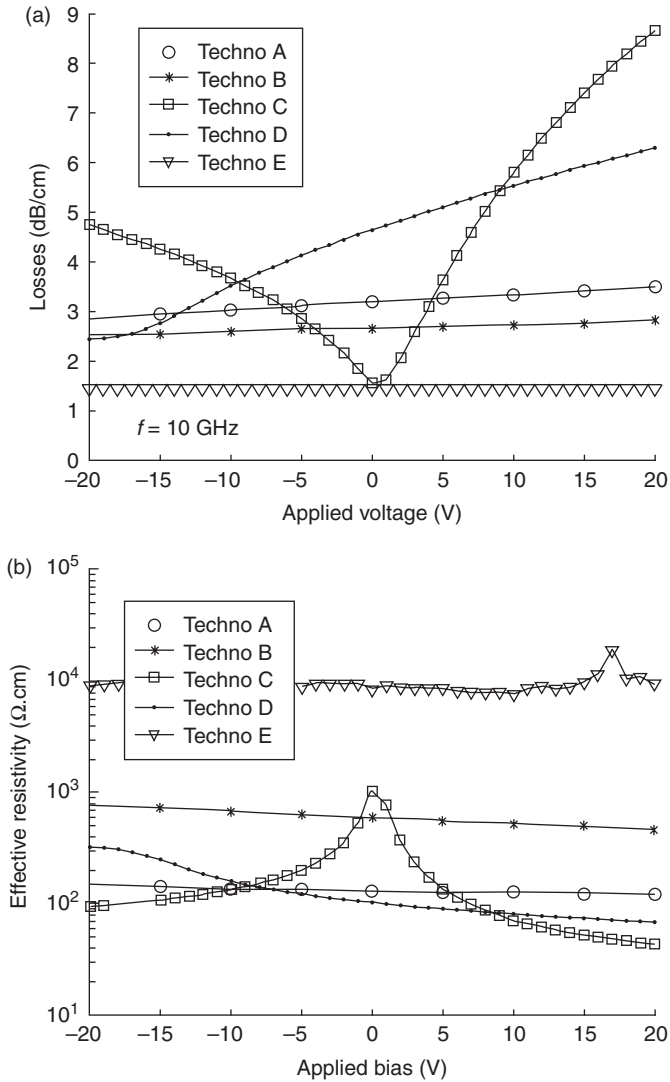
cm are today available on the market, and are the substrates of choice for RFICs¹⁰⁰ and mixed-signal applications.¹⁰¹ However, oxide passivated high-resistivity wafers are known to suffer from parasitic surface conduction (PSC) due to fixed charges (Q_{ox}) in the oxide.¹⁰² Indeed, charges within the oxide attract free carriers near the substrate surface, reducing the effective resistivity (ρ_{eff}) seen by coplanar devices and increasing substrate losses. It has been shown⁹⁸ that values as low as $Q_{ox} = 10^{10} \text{ cm}^{-2}$ could lower the value of resistivity by more than one order of magnitude in the case of a 50 Ω CPW transmission line. Parasitic surface conduction can also be formed underneath metallic lines with the application of a DC bias (V_a).¹⁰³ The extracted line loss and effective substrate resistivity as a function of the DC bias applied to the central conductor of a CPW line are presented in Fig. 10.17a and 10.17b, respectively, for different substrates, oxide layers and metallic lines, as summarized in Table 10.3. Techno A and B are industrial wafers, while the other three wafers – C, D and E – are home processed, with one metal layer. In all cases, the metallic structures are patterned on either oxidized p-type HR Unibond SOI (techno A, B, C) or oxidized p-type HR bulk Si (techno D and E) substrates.

The total RF losses (α_{tot}) of the CPW lines are extracted from the measured S-parameters with a Thru-Line-Reflect method.¹⁰⁴ They are reported at 10 GHz in Fig. 10.17a as a function of V_a . Logically, α_{tot} is more significantly affected by V_a when the oxide thickness (t_{ox}) is thinner (techno C). The V_a value for which losses are minimum ($V_{a,min}$) corresponds to a state of deep depletion underneath the oxide. As shown in Fig. 10.17, V_a depends on the flatband voltage of the structure and is, therefore, dependent on t_{ox} as well as the oxide charge density (Q_{ox}).

Table 10.3 Additional information on the different technologies investigated in Fig. 10.17

Techno	Starting wafer	Metal layers	Oxide thickness (μm)	Si passivation	Oxide type
A	HR SOI	M3	3	No	BOX + oxidized SOI + interlayer dielectrics
B	HR SOI	M5–M6	4.1	No	BOX + oxidized SOI + interlayer dielectrics
C	HR SOI	M1	0.3	No	BOX + oxidized SOI
D	HR-Si bulk	M1	1	No	PECVD
E	HR-Si bulk	M1	1	Polysilicon	PECVD

Note: The data in columns 3 and 4, respectively, indicate the metal levels that were used and the total equivalent oxide thickness for CPW lines.



10.17 (a) CPW losses and (b) effective substrate resistivity measured for different technologies described in Table 10.3 as a function of DC bias applied to the CPW central conductor.

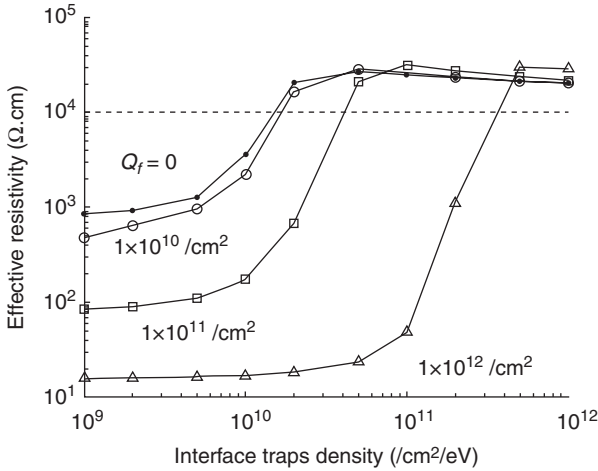
Parasitic surface conduction can be reduced or even suppressed if the silicon substrate is passivated before oxidation with a trap-rich layer. Figure 10.18 illustrates the impact of trap density (D_{it}) at the HR-Si substrate/ SiO_2 interface on ρ_{eff} at 0 V for several Q_{ox} densities. Obviously, the minimum D_{it} level that is required to obtain lossless substrates (i.e., $\rho_{\text{eff}} = 10$ $\text{k}\Omega \cdot \text{cm}$) is an increasing function of the fixed charge density in the oxide.

The introduction of a high density of traps at the Si/SiO₂ interface has been successfully achieved using low-pressure chemical vapour-deposited (LPCVD) poly-Si¹⁰⁵ and amorphous silicon (α -Si).¹⁰⁶ In the case of a HR SOI wafer fabrication process, the passivation layer should be included within the SOI structure by bonding an oxidized silicon wafer to a passivated HR substrate. In Reference 99, the proposed method consists of the LPCVD-deposition of amorphous silicon followed by Si-crystallization at 900°C with RTA. This new passivation method has also been shown to present better rms surface roughness ($\sigma = 0.37$ nm) and to remain effective after long thermal anneals (4 h at 900°C). A successful bonding of this layer with an oxidized substrate has been achieved, showing that this new passivation technique could be introduced at reduced cost inside a Smartcut or bond and etch-back SOI (BESOI) process in order to fabricate SOI wafers with enhanced resistivity, that is, higher than 10 k Ω .cm.

Figure 10.17a indicates that substrate passivation with poly-Si (techno E) significantly reduces RF losses while getting rid of the V_a influence. This is because traps present inside the poly-Si layer can absorb free carriers and pin the surface potential to a value independent of V_a .¹⁰⁵ Figure 10.17b presents the effective resistivity (ρ_{eff}) extracted according to a method depicted by Lederer and Raskin.⁹⁷ Not surprisingly, the highest ρ_{eff} value is observed for the passivated substrate, while at 0 V, the lowest value is obtained for the low quality (Q_{ox} -rich) plasma-enhanced chemical vapour deposition (PECVD) oxide. It should also be noted that, due to the inverted layer underneath the BOX in techno A and techno B, the extracted values of ρ_{eff} do not exceed 130 and 580 Ω .cm, respectively. These values are both more than one order of magnitude lower than the nominal substrate resistivity.

Very recently, SOITEC launched the so-called trap-rich HR SOI substrate onto the market. Ben Ali *et al.*¹⁰⁷ demonstrated the quality of this novel substrate, exhibiting an effective resistivity higher than 3 k Ω .cm, so providing low insertion loss along interconnection lines and extremely reduced crosstalk. Additionally, the excellent matching between the experimental static and RF characteristics of measured FD SOI MOSFETs on top of both HR SOI and trap-rich HR SOI wafers clearly demonstrates that the presence of traps underneath the BOX does not alter the DC and RF behaviours of SOI MOS transistors.

In Botula *et al.*,¹⁰⁸ IBM also proposes the introduction of traps at the BOX–Si handle wafer interface to recover the high-resistivity feature of the HR SOI substrate. The introduction of the traps between active devices is made before the back-end metallization by high dose implantation through the BOX. Trenches are etched through the shallow trench isolation (STI) and BOX to the substrate in areas where substrate effects are to be suppressed. These are either trench line features between devices, or a high-density lattice pattern in larger areas. Heavy dose implants are performed, using the etch resist as a



10.18 Simulated effective resistivity values (ρ_{eff}) as a function of the trap density (D_{it}) for several fixed charges densities (Q_{ox}) at an applied bias value of 0 V.

mask. Trenches are then filled with oxide and planarized for the contacts. Using this technology IBM demonstrated the drastic reduction of the harmonic generation issue in the HR SOI substrate, and designed a 180 nm CMOS thin film SOI RF switch with power handling, linearity and $R_{\text{on}} \times C_{\text{off}}$ competitive with GaAs pHEMT and silicon-on-sapphire (SOS) technologies.¹⁰⁸ Compared to the trap-rich HR SOI substrate proposed by SOITEC, here one additional mask and a high dose implantation step are used to suppress the PSC effects.

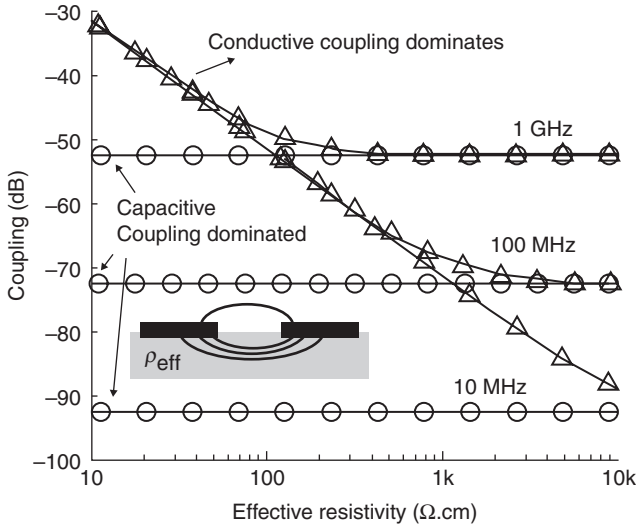
10.7.2 Crosstalk

In recent years, rapid progress of IC technology has enabled the co-integration of the analogue front-end and digital baseband processing circuits of communication systems onto the same chip. Such mixed-signal system-on-chips allow more functionality, higher performance, lower power consumption and higher reliability than non-integrated solutions. Moreover, thanks to CMOS technology scaling and its associated increasing integration level, SoCs have become the way to achieve cost effectiveness in demanding applications such as home entertainment and graphics, mobile consumer devices, networking and storage equipment. Such a rising integration level of mixed-signal ICs raises new issues, such as the substrate noise generated by switching digital circuits, called digital substrate noise (DSN), which may degrade the behaviour of adjacent analogue circuits.^{109,110} DSN issues become more and more important with IC evolution as: (i) digital parts get more noisy due to increasing complexity and clock frequencies, (ii) digital and analogue parts

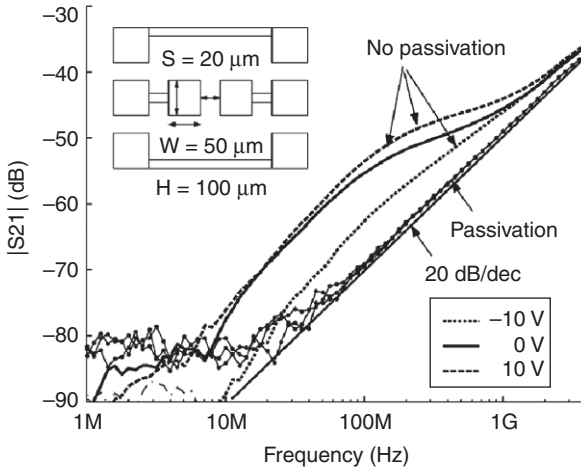
get closer together, and (iii) analogue parts get more sensitive because of supply voltage, V_{dd} , scaling for power consumption issues.

In general, substrate noise can be separated into three different mechanisms: noise generation, injection/propagation into the substrate and reception by the analogue part.¹¹¹ Improvement in the reduction of any of these three mechanisms, or in all of them, will lead to a reduction of the DSN and in a relaxation of the design requirements. Typically, guard rings and oversized structures are adopted to limit the effect of substrate noise, thereby reducing the advantages of the introduction of new technologies. It is thus a major issue for the semiconductor industry to find size-efficient design/technology solutions to reduce the impact of substrate noise in mixed-signal ICs.

In the last decade several publications have demonstrated both theoretically and experimentally the possibility of using the HR SOI substrate to greatly reduce the crosstalk level between ICs.⁵ Simulation results presented in Fig. 10.19 show how the crosstalk between two 50 μm -spaced metallic pads is directly related to ρ_{eff} . These results indicate that ρ_{eff} must be at least in the $\text{k}\Omega\cdot\text{cm}$ range to get rid of conductive coupling inside the substrate for frequencies around 100 MHz and lower. Figure 10.20 shows the measured crosstalk $|S_{21}|$ vs frequency for two 50 $\mu\text{m} \times 50 \mu\text{m}$ metallic pads spaced 20 μm apart and lying on HR-Si substrate with and without a trap-rich layer. The measurements are performed by using low-frequency vectorial network analyzer (VNA) up to 4 GHz and by applying various bias conditions to the coupling pads. The figure shows a significantly higher (~ 13 dB at 0 V) crosstalk level below 1 GHz for the standard HR SOI wafer, due to conductive effects in the substrate associated with parasitic surface conduction.¹¹² It also highlights a significant dependence with respect to the applied bias. The crosstalk level is strongly reduced for negative bias when deep depletion is formed below the BOX whereas it is increased and exhibits higher cut-off frequencies for positive bias because of the stronger inversion below the oxide. On the other hand, the trap-rich wafer exhibits: (i) no effect of the applied bias due to the presence of the trap-rich polysilicon layer below the BOX⁹⁷ and (ii) a perfect 20 dB/dec $|S_{21}|$ slope, which demonstrates that purely capacitive coupling occurs in the measurement frequency range (i.e., above the VNA noise floor). A reduction of crosstalk below 1 GHz is of particular interest for mixed-signal applications, since it is known from previous studies that the frequency spectrum of the noise generated by digital logic typically expands to several hundreds of megahertz, corresponding to multiples of the clock signal^{113,114} or circuit internal resonance frequencies.¹¹⁵ The generation of noise in that frequency range has also been shown to strongly increase the jitter in phase-locked loops (PLLs), which seem to be particularly sensitive to substrate noise injected at the PLL reference frequency – that is, in the few hundreds of megahertz range.¹¹⁶ It is further believed that, in terms of crosstalk, the benefits gained by trap-rich HR SOI will even be more



10.19 Simulated crosstalk level at 10 MHz, 100 MHz and 1 GHz as a function of ρ_{eff} according to model presented by Raskin *et al.*⁵



10.20 Crosstalk measured as a function of frequency and under distinct bias conditions on unpassivated and passivated HR Si wafers.

significant in the future. Indeed, a reduction of the BOX thickness for the next generations of SOI CMOS devices will be required to reduce short channel effects and self-heating.¹¹⁷

Substrate crosstalk into standard and trap-rich HR-Si substrates over a wide-frequency range, from ultra-low (ULF) to extremely high-frequency

(EHF) bands, has been investigated using finite-element numerical simulations and experiments.¹¹⁸ It has been demonstrated that low-frequency substrate crosstalk is strongly impacted by the presence of free carriers at the interface between the HR-Si substrate and the interconnection passivation layers. The efficiency of a trap-rich layer, a poly-Si layer thicker than 300 nm, placed at that interface to recover the nominal high-resistivity characteristic of the Si substrate has been theoretically and experimentally demonstrated. Wideband crosstalk behaviour of the HR-Si substrate with and without a trap-rich layer was modelled by means of a simple equivalent lumped element circuit. The proposed model shows excellent agreement with finite-element numerical simulations and experimental data for frequencies above 100 kHz. Thanks to the introduction of a trap-rich layer, the HR-Si substrate behaves as a lossless dielectric substrate, so a purely capacitive electrical equivalent circuit is sufficient to properly describe the substrate crosstalk characteristics.

Further decrease of crosstalk will come from the reduction of the effective permittivity of the substrate. Sapphire and quartz, but especially porous silicon, for which effective permittivity as low as 2¹¹⁹ can be reached, are handle substrates of great interest for high RF performance SOI technology.

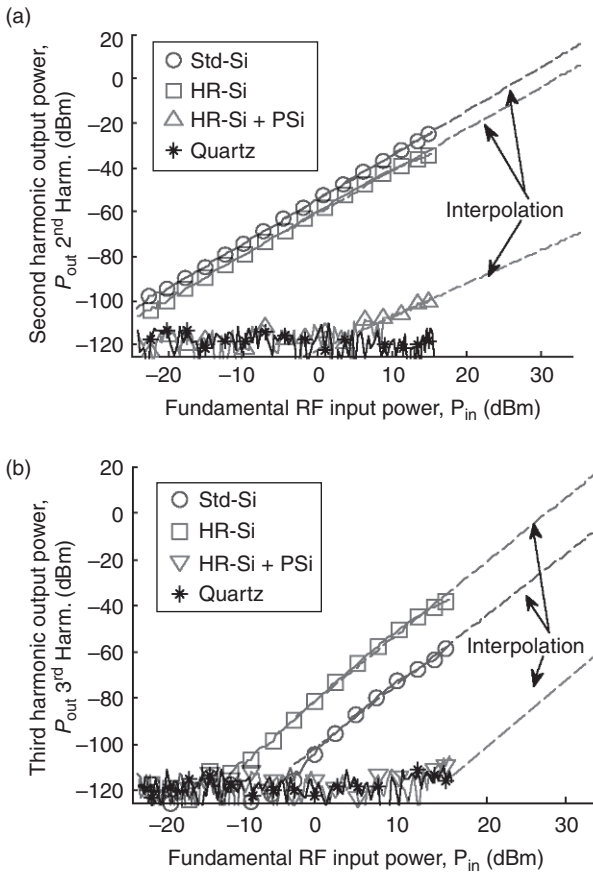
10.7.3 Non-linearities along CPW lines

Thanks to the reduced substrate loss and coupling into the HR SOI substrate, as presented in the two previous paragraphs, SOI technology is considered by more and more companies for the integration of RF cellular transmit switches.^{120,121} Radio frequency switches have high linearity requirements. A recent III–V RF switch product specifies less than –45 and –40 dBm for 2nd and 3rd harmonic powers (H2 and H3), respectively, at +35 dBm input power.¹²² As requirements become even more stringent for advanced multi-mode phones and 3G standards, it is important to investigate the non-linear behaviour of the RF switch itself, but also all other possible sources of non-linearity, such as the harmonic distortion (HD) originating from the lossy Si substrate handle onto which the RF switch is integrated.

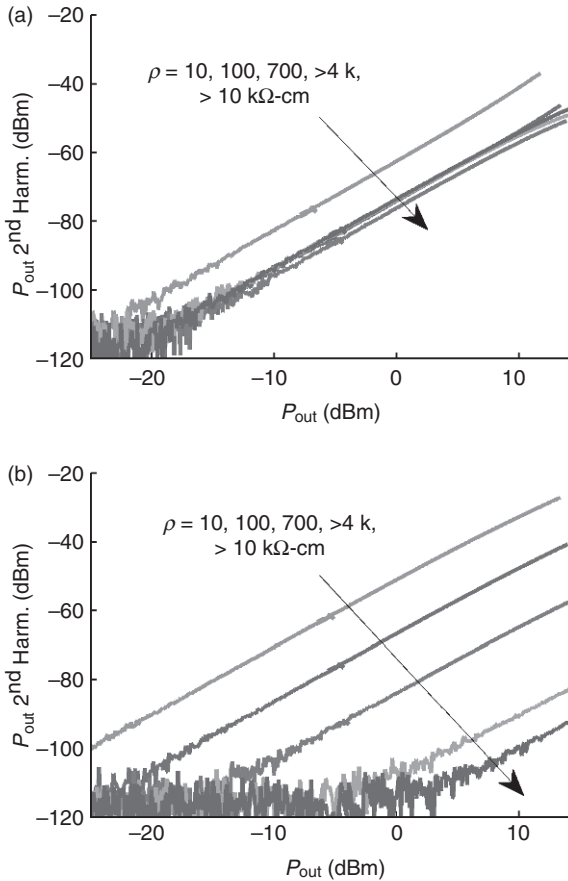
As explained in Section 10.7.1, when the CPW line is biased the distribution of potential and free carriers inside the Si substrate changes, as in the case of a classical MOS capacitor. The variation of carrier distribution in the Si substrate with applied bias or large RF signal will lead to the existence of non-linear capacitance (C) and conductance (G) associated with the Si substrate. Those variables, C and G , are at the origin of harmonics formation inside the Si substrate.

Figure 10.21 shows the harmonics distortion at the output of CPW lines lying on p-type Si substrates characterized by different resistivities and

covered by 50 nm thick SiO_2 . The HR-Si substrate presents lower HD than the 20 $\Omega\cdot\text{cm}$ (standard Si resistivity, std-Si) substrate over most of the power sweep. Measurements are made up to 15 dBm input power, and linearly interpolated up to +35 dBm. It can be observed that non-passivated Si substrates have HD levels higher than 45 dBc at +15 dBm, already 25 dB higher than the switch specifications at +35 dBm. The introduction of a 300 nm poly-Si layer reduces HD levels by more than 60 dB, compared to non-passivated HR-Si. As explained above, thanks to the high density of traps in the polycrystalline silicon or as-deposited amorphous silicon layer located at the Si– SiO_2 interface, the surface potential at this interface is nearly *fixed*, and the external DC bias or large amplitude RF signal applied to the line does not impact the distribution of carriers inside the Si substrate.



10.21 (a) 2nd and (b) 3rd harmonic power of a 3385 μm -long CPW line lying on different substrates.



10.22 Measured 2nd harmonic output power of a 2146 μm -long CPW line on n-type Si with different resistivities (a) without, and (b) with a trap-rich poly-Si layer.¹²³

In order to check the influence of the substrate nominal resistivity on the harmonic distortion, CPW lines fabricated on Si substrates with different resistivities, with and without a poly-Si layer, were measured.¹²³ Figure 10.22 clearly shows that the presence of a trap-rich layer has almost no impact on the measured distortion levels for low resistivity substrates ($\rho = 10$ and $100 \Omega\text{-cm}$). On the other hand, for substrates with higher resistivities, it considerably reduces the non-linearities. Measurements made for substrates with identical high resistivity but different oxides, not presented here, show that the minimum distortion is obtained when a poly-Si layer is introduced, and it is only limited by the final effective resistivity. The introduction of a thin poly-Si layer helps in the reduction of PSC effects but cannot totally reduce the harmonic levels. Only the combination of both the Si substrate

characterized by a high resistivity ($> 3 \text{ k}\Omega\cdot\text{cm}$) and a trap-rich layer provides a viable solution to obtain a quasi-linear Si substrate.

The correlation between the substrate effective resistivity and the generated harmonic distortion along a CPW line has been demonstrated, using both simulations and experimental measurements, on a large variety of commercial Si substrates with nominal resistivities from $10 \text{ }\Omega\cdot\text{cm}$ up to values above $10 \text{ k}\Omega\cdot\text{cm}$. Thus, the effective resistivity is really a powerful figure, of value in determining not only the substrate RF losses but also its linearity.¹²³

A trap-rich layer, such as polysilicon, placed at the Si/SiO₂ interface is an efficient technological solution for recovering the high-resistivity properties of HR-Si and thus reducing harmonic distortion due to the substrate. Moreover, it has been demonstrated that the harmonic distortion of trap-rich HR-Si is not impacted by the quality or thickness of the oxide layer. From our experimental results we can conclude that only Si handle substrates with ρ_{eff} of more than $3 \text{ k}\Omega\cdot\text{cm}$, combined with a trap-rich layer, will present equivalent harmonic levels below 70 dBc for +35 dBm input power.

10.8 Conclusions

Nowadays, the strained SOI n-MOSFET which exhibits a cut-off frequency close to 500 GHz is really competing with the III–V technologies. Thanks to the introduction of high-resistivity SOI substrates, the integration of high quality passives is a reality, and the reduction of the substrate crosstalk is a real advantage compared to Si bulk for the development of high integration low voltage mixed-mode applications. Major semiconductor companies such as ST-Microelectronics, IBM, RFMD, Honeywell, TowerJazz, and so on, have already produced several products for the telecommunications market based on SOI RF technologies.

As demonstrated in this chapter, by the introduction of a trap-rich layer underneath the BOX, HR SOI substrates can still be improved. Having a polysilicon-based layer with a thickness of approximately 300 nm sandwiched between the BOX and the HR-Si substrate, CPW insertion loss, crosstalk, DSN and harmonic distortion are greatly reduced, without affecting the good DC and RF behaviours of SOI CMOS transistors. To summarize, present and future HR SOI MOSFET technologies are very good candidates for mixed-mode low voltage low power RF and even millimetre-wavelength applications.

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Silicon-on-insulator (SOI) complementary metal oxide semiconductor (CMOS) circuits for ultralow power (ULP) applications

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Abstract: SOI CMOS device and circuit technologies operating at low voltages dedicated for ultralow power applications are reviewed. It is important to improve energy efficiency while maintaining an acceptable speed performance in ultralow power applications for long-life battery operation, or using harvested power. Major obstacles for the low voltage operation of CMOS are large characteristic variability and small on–off ratio of transistors. The solution to this issue involves using a fully depleted silicon-on-insulator (FDSOI) transistor with back bias control. The current status of the device, and circuit technology development of FDSOI with back bias, is presented.

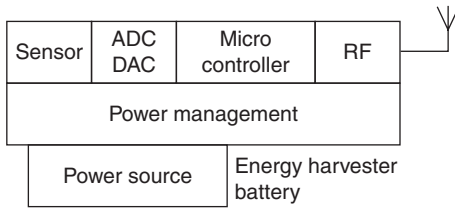
Key words: CMOS, ultralow power, ultralow voltage, variability, back bias, fully-depleted SOI, thin BOX.

11.1 Introduction: the importance of ultralow power devices

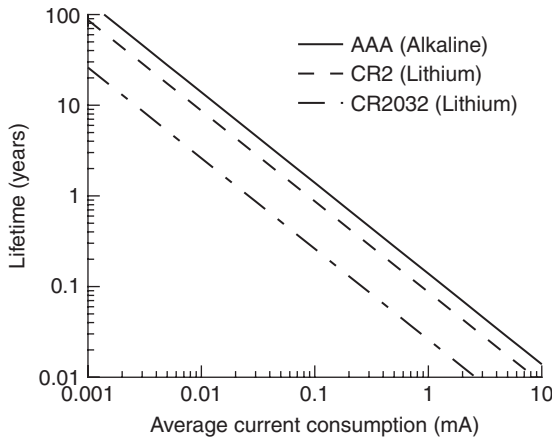
Low power technology is commonly required in electronic devices, such as cellular and smart phones, gaming devices, personal computers, and home and car electronics. This chapter focuses on ways to reduce power consumption to achieve ultralow power (ULP) electronic devices. There are many potential applications of ULP microelectronic systems, including:

- industrial sensing/monitoring systems;
- sensing systems for fatigue/fracture monitoring of infrastructure; and
- implantable or portable health monitoring systems.

These systems often need to be operated for long periods without being connected to an external power source. Figure 11.1 shows a diagram of a sensor node as an example. This system consists of:



11.1 Typical block diagram of sensor node.



11.2 Battery lifetime as a function of average current consumption.

- sensors;
- data processing unit (microcontroller);
- communication unit radio frequency (RF); and
- power supply.

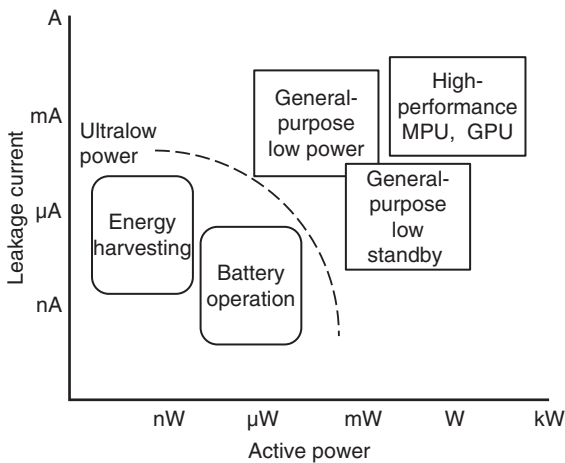
Most of the components comprise CMOS circuits. A key requirement is to reduce power consumption in these circuits.

Firstly, we need to establish the duration of the battery life, and how low power consumption must be reduced to in order to use the device over a long time period, such as ten years, with a conventional battery. Figure 11.2 shows battery lifetime as a function of average current consumption. Note that self-discharge and degradation are not taken into account. If we require a lifetime of approximately ten years, the current consumption should be less than 10 μ A. Assuming the output voltage is 3 V (lithium battery), the average power is 30 μ W. Using an energy harvester is another option for a long-term operation. Table 11.1 compares power densities of typical harvesting sources. The values are cited from Tan (2010). The power consumption of several tens of microwatts will be applicable for a system using an energy harvester.

Table 11.1 Comparison of energy harvesting sources

Energy source	Power density	Notes
Solar	100 $\mu\text{W}/\text{cm}^3$	Illuminated office assumed
Thermoelectric	60 $\mu\text{W}/\text{cm}^3$	5°C gradient assumed
Blood pressure	0.93 W	100 mmHg, order of μW (continuous load)
Ambient airflow	177 $\mu\text{W}/\text{cm}^3$	Average wind speed of 3 m/s assumed
Vibrational	4 $\mu\text{W}/\text{cm}^3$	Human motion, highly dependent on excitation
Piezoelectric push buttons	50 $\mu\text{J}/\text{N}$	At 3 V dc

Source: Tan, 2010.



11.3 Schematic map of active power versus leakage current.

In many (currently envisioned) sensor-node applications, generally speaking, the required operation speed is not too high. For example, pulse oximetry, single-lead electrocardiogram (ECG), and 12-lead ECG require operating frequencies of 331 kHz, 1 and 25.7 MHz, respectively (Chandrakasan, 2010). The latter case (25.7 MHz) is only activated in rare circumstances. The level of power consumption mentioned above is therefore affordable for many applications. However, if we further improve the level of energy efficiency, more functional and more intelligent operations in each sensor node will be possible, leading to improvements in the sensor-network system performance, leading to increased opportunity for its application. Figure 11.3 schematically shows a map of applications of CMOS circuits as functions of operational power and standby leakage power after Tani (2007). This chapter focuses on the ULP areas in which small and long-life batteries or energy harvesters can be used, and shows that SOI devices

are suitable to improve performance under restricted power supply in these areas.

11.2 Minimizing power consumption of CMOS circuits

Power consumption of CMOS circuits is the sum of operation power and leakage power, and is expressed in its simplest form as

$$P = n (aC V_{dd}^2 f + I_{leak} V_{dd}), \quad [11.1]$$

where n is the number of transistors; a is the activity of the circuit; C is the load capacitance; V_{dd} = operation voltage or supply voltage; I_{leak} is the leakage current of a transistor; and f is the operation frequency. The parameter a is introduced in order to account for the time-averaged operation power, because not all circuits are operating continuously.

The power depends on f . In this respect, energy per operation E is important and is written, simply divided by af , as

$$E = n \left(CV_{dd}^2 + I_{leak} \frac{V_{dd}}{af} \right). \quad [11.2]$$

The first term of the right-hand side (RHS) of Equation [11.2] corresponds to active energy and depends on V_{dd} assuming C is constant for the same circuit or the same CMOS technology. The second term corresponds to leakage energy that is rather complex depending on all parameters: I_{leak} , V_{dd} , a , and f . Frequency, f , of CMOS circuit and drain current, I_{ds} , of transistor are simply formulated as follows:

$$f \propto \frac{I_{ds}}{CV_{dd}} \quad [11.3]$$

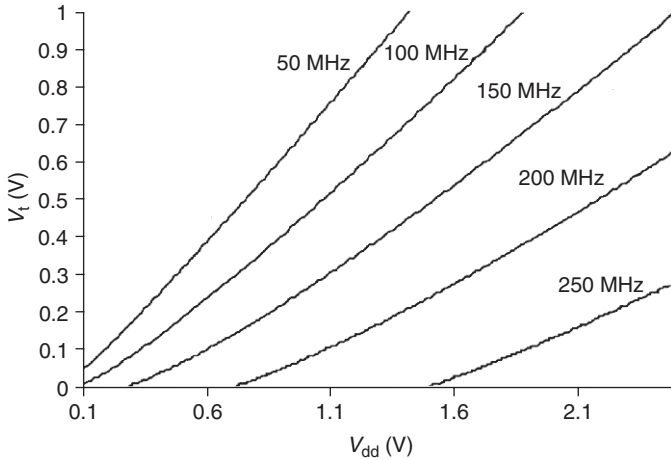
and

$$I_{ds} = C_{ox} W (V_{gs} - V_{th}) v_s \propto V_{gs} - V_{th}, \quad [11.4]$$

where C_{ox} is the gate capacitance, W is the transistor width, V_{gs} is the gate voltage, V_{th} is the threshold voltage, and v_s is the average velocity of carriers in the channel of transistor.

For example, Fig. 11.4 (Kao, 2002¹) shows f as a function of V_{dd} and V_{th} . The appropriate combination of V_{dd} and V_{th} should thus be designed to operate

¹ The curves in Figs 11.4 and 11.5 were drawn based on the theoretical formulation and electrical data of the SH4 microprocessor chip of a 0.14 μm technology. The data in Fig. 11.8 were collected from the digital signal processing (DSP) test chip of the same technology.



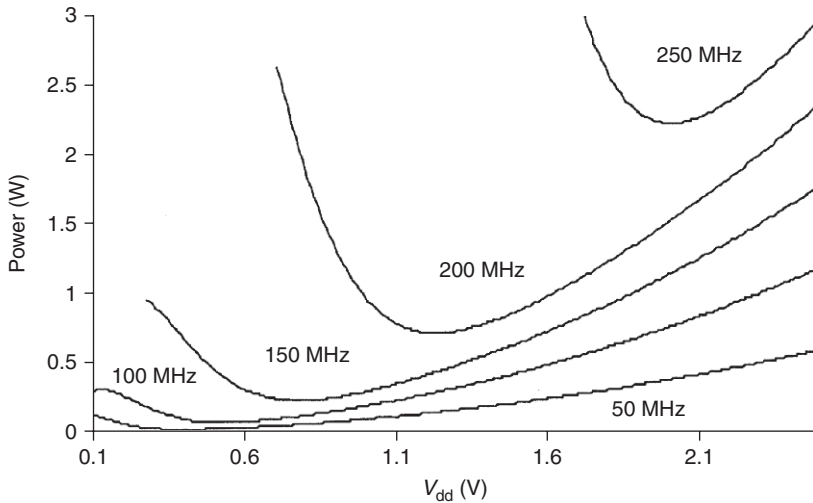
11.4 f as a function of V_{dd} and V_{th} (Kao, 2002).

at frequencies to satisfy the processing speed requirement. With decreasing V_{dd} , f significantly decreases if V_{th} is constant. V_{th} should be decreased if f is kept constant with decreasing V_{dd} . In both cases, the leakage power in Equation [11.1] increases relatively. Figure 11.5 shows P (sum of active and leakage power) as functions of various V_{dd} and f under the same conditions as in Fig. 11.4 (Kao, 2002). The best V_{dd} to minimise power thus varies with f . To compare energy for different frequencies, the values of P on this graph should be simply divided by f . It is clear that the minimum E point lies on the curve of lowest frequency (50 MHz). The minimum energy tends to decrease with decreasing f . More clearly, Fig. 11.6 shows a contour map of energy, supply voltage, and frequency (Wang, 2005²). Note that the numbers on the contours are relative energy normalised to the minimum point. At this minimum point, V_{dd} and V_{th} are 0.38 and 0.48 V, respectively, and f is only 13 kHz. Therefore, if we wish to operate the circuits with minimum energy, we should accept a slower operating speed. In short, the main requirements for minimum energy are:

- f tends to slow down, and
- there is an optimum V_{dd} and V_{th} combination for a specific f .

The minimum energy case in Fig. 11.6 has a very poor performance at $f = 13$ kHz. Looking at V_{dd} and V_{th} in this case, V_{th} is higher than V_{dd} . This means the transistors are not turned on (below the threshold) in

² The data in Fig. 11.6 were based on the standard logic cell library fabricated on a 0.18 μm standard CMOS process.

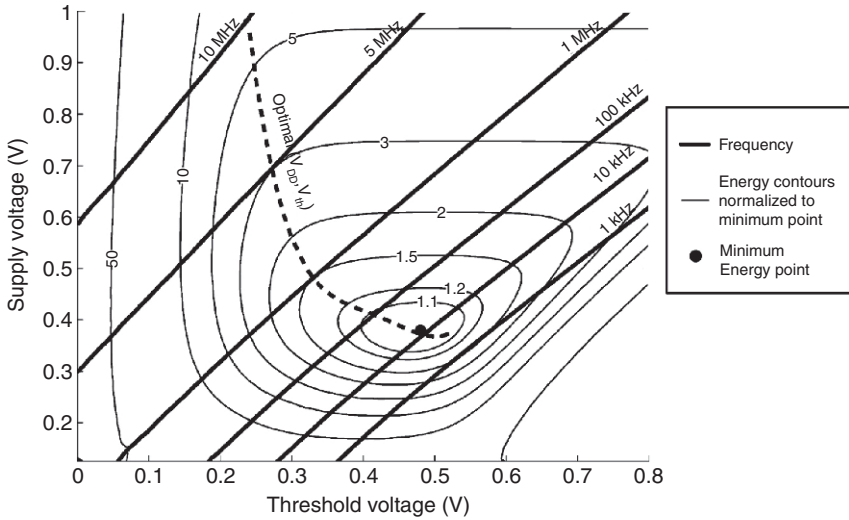


11.5 P as functions of V_{dd} and f (Kao, 2002).

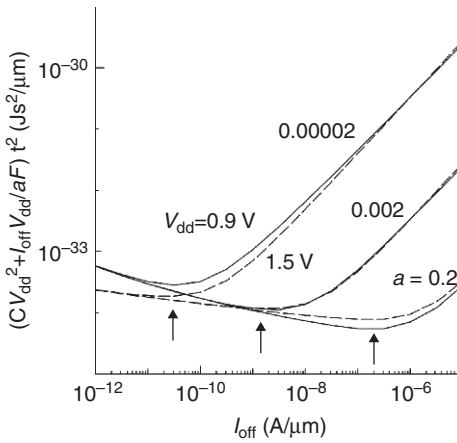
this condition. A circuit of this type is called a sub-threshold logic circuit. Although the sub-threshold operation might be better in terms of energy efficiency, its low clock frequency has hindered an implementation in its practical application. This problem should be overcome by massively parallel circuit operation. Another difficulty is large variation in the operation speed (Kwong, 2008) because I_{ds} under the sub-threshold regime exponentially changes with V_{th} variation. This results in a rapid increase in the logic error rate with decreasing V_{dd} in the sub-threshold regime (Kwong, 2006).

Practically, a preferable solution to the ultralow voltage logic circuit is staying on the conventional super-threshold operation regime, that is, optimise V_{dd} and V_{th} under the required f and the condition $V_{dd} > V_{th}$. Figure 11.6, however, shows energy under a continuous operation. In a real application, the situation is different. The circuits do not operate continuously, but rather intermittently. In Equation [11.1], the parameter a is introduced. The minimum energy condition can vary with a . Figure 11.7 shows energy as functions of a and I_{off} ($= I_{leak}$) (Takeuchi, 2001³). Note that I_{leak} is exponentially determined by $-V_{th}$. The floor level of this graph is determined by the leakage (second) term of Equation [11.2]. On this bottom line, from left to right, the operation speed increases with increasing I_{off} (decreasing V_{th}) under the same energy. The best point thus lies at the inflection point (right endpoint of the bottom line). Apparently the best point moves with a . In general, a varies according to the situation, even in the same circuit.

³ Theoretical calculation not based on the specific CMOS process.

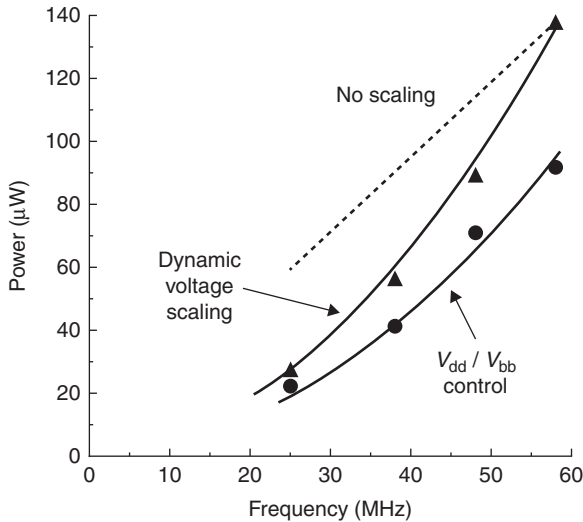


11.6 Contour map of E , V_{dd} , and f (Wang, 2005).



11.7 E as a function of a and I_{off} (Takeuchi, 2001).

This means that V_{th} (I_{off}) should be varied to minimise energy when the activity varies. The substrate bias voltage, V_{bb} , can control the V_{th} of MOSFETs. The circuit with V_{th} control by V_{bb} is known as the adaptive back (or body) bias (ABB) control (Miyazaki, 2002). The ABB control can significantly reduce power under various frequencies, as shown in Fig. 11.8 (Miyazaki, 2002). With neither V_{dd} nor V_{bb} control (no scaling), the power proportionally changes with frequency (behaviour of the first term of Equation [11.1]).

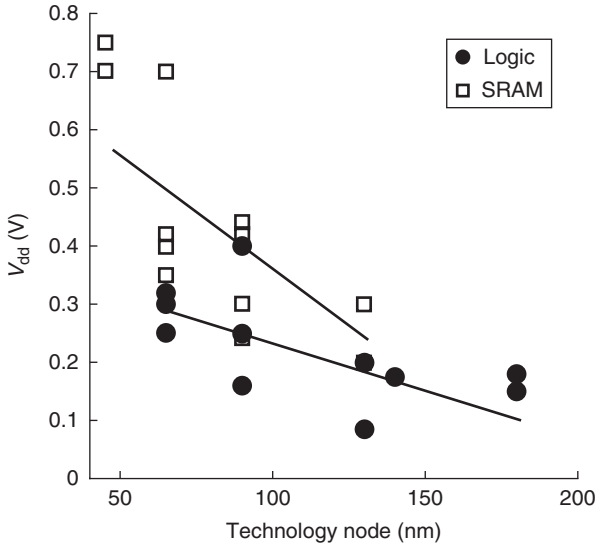


11.8 Power as a function of frequency (Miyazaki, 2002).

The dynamic voltage scaling means that V_{dd} is controlled to the minimum value that can be operated at specific frequencies; in general, V_{dd} can be decreased with decreasing f (Equations [11.3] and [11.4]), and the power is decreased. The ABB control further reduces the power by adding the V_{th} control. The ABB control is thus the best solution for optimising power that is applicable to differing frequencies and activities. However, the usability of this scheme has been limited to date in conventional bulk CMOS circuits. In the next section, issues regarding the V_{dd} scaling and the ABB will be discussed.

11.3 Issues on V_{dd} scaling to improve the energy efficiency of CMOS circuits

As discussed in the previous section, the optimisation of V_{dd} and V_{th} is important for maximizing energy efficiency in the CMOS circuit. In the four decade-long history of CMOS circuits, continuous scaling of CMOS transistors has improved circuit performance, functionality, power efficiency, and economic value. From the viewpoint of power efficiency, continuous reduction of V_{dd} obeying the ideal scaling rule (Dennard, 1974) has been effective and successful to date. If we had been able to continue V_{dd} scaling, that is, extrapolating the past V_{dd} scaling trend (Bult, 2000), V_{dd} would be less than 0.6 V at the minimum feature size of 28–40 nm. However, V_{dd} scaling in current CMOS technology is very difficult and the minimum V_{dd} still stays at a level a little less than 1.0 V.



11.9 Minimum V_{dd} trend (Chandrakasan, 2010). Data are collected from various literatures.

As shown in Fig. 11.9 (Chandrakasan, 2010), the minimum V_{dd} (V_{min}) has actually been increasing, contrary to the scaling rule (note that the technology node in the figure is roughly the same as the minimum feature size). The figure shows that the V_{min} for static random access memory (SRAM) is very difficult to reduce and exhibits higher V_{min} values than the logic circuit. In the recent technology nodes, the V_{min} values have still been high though improving slightly at the technology nodes less than 40 nm (Sinangil, 2012). This improvement might be due to progress in assist-circuit technology, which controls operation voltage during the read and write cycles.

The main cause of the difficulty in the V_{dd} scaling is an increase in V_{th} variability in the miniaturised transistors. It is well-known that the V_{th} variability can be expressed as follows (Pelgrom, 1989):

$$\sigma V_{th} = \frac{A_{VT}}{\sqrt{LW}}, \quad [11.5]$$

and in the conventional bulk transistor, it can be written as

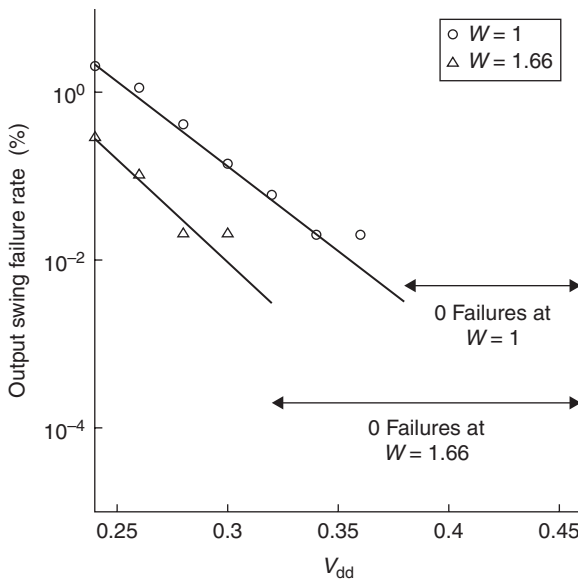
$$\sigma V_{th} \propto \frac{t_{ox} N_{imp} 1/4}{\sqrt{LW}}, \quad [11.6]$$

where σV_{th} is the standard deviation of V_{th} , A_{VT} is the Pelgrom coefficient, L the gate length, W the transistor width, t_{ox} the gate oxide thickness, and N_{imp} the impurity density of the channel region.

In the ideal scaling rule, t_{ox} , L , and W decrease at the same rate and N_{imp} increases similarly. This results in a slight increase of σV_{th} generation by generation. Moreover, in the last two or three generations, the scaling of t_{ox} has been retarded. This accelerates the increase in σV_{th} . The increase in σV_{th} with the scaling is thus very difficult to avoid if we stay on the conventional bulk transistor. The solution is moving on to different transistor structures that can reduce N_{imp} . Possible structures to reduce this variability are described later.

In the logic circuits, the output voltage of the specific stage drives the input nodes of the next stage. The output voltage of each stage should be sufficiently higher than the noise amplitude to avoid any errors. It is easily understood that the output voltages increase with increasing V_{dd} . An example is shown in Fig. 11.10 (Kwong, 2006). The failure rate of the inverter is plotted as a function of V_{dd} . The rate exponentially increases with decreasing V_{dd} . Note that the error rate is also affected by the transistor width, W , reflecting the current driving ability to charge the capacitance of the input nodes of the next stage.

The minimum V_{dd} (V_{min}) is determined both by the random-variation and systematic-variation components. The V_{min} is described as (Yasufuku, 2011)



11.10 Failure rate of inverter as a function of V_{dd} (Kwong, 2006).

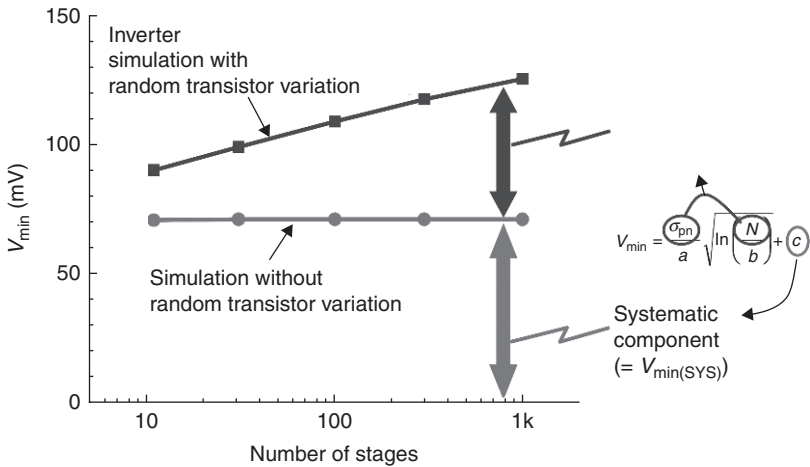
$$V_{\min} = \frac{\sigma_{pn}}{a} \sqrt{\ln\left(\frac{N}{b}\right)} + V_{\min(\text{sys})} \tag{11.7}$$

where σ_{pn} is the root sum square of $\sigma_{V_{th}}$ of N- and PMOS transistors, N is the number of stages, a is a constant determined by DIBL, and b is a constant determined by yield.

Note that the operation speed is excluded in this description, due to its ridiculously slow speed at V_{dd} near V_{\min} . Figure 11.11 shows simulated V_{\min} of inverter as a function of number of stages N (Yasufuku, 2011). V_{\min} increases with N due to the random-variation factor, as indicated in the first term of the RHS of Equation [11.7]. The systematic component $V_{\min(\text{sys})}$ is determined by the logic threshold voltage. The output amplitude of the CMOS logic circuits is determined by competition between pull-up PMOS and pull-down NMOS transistors. The $V_{\min(\text{sys})}$ reverts to a minimum when the driving ability of both transistors is balanced, that is, the logic threshold voltage is just half of V_{dd} .

The $V_{\min(\text{sys})}$ is determined predominantly by two factors. The on-off ratio is the first. In the sub-threshold regime, the drain current exponentially changes. The slope of the exponential change is known as the sub-threshold swing (or slope) S , and is written as,

$$S = \ln(10) \frac{k_B T}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right) \approx 59.5 \left(1 + \frac{C_{dm}}{C_{ox}} \right) \text{ (mV/decade at } T = 300 \text{ K)} \tag{11.8}$$

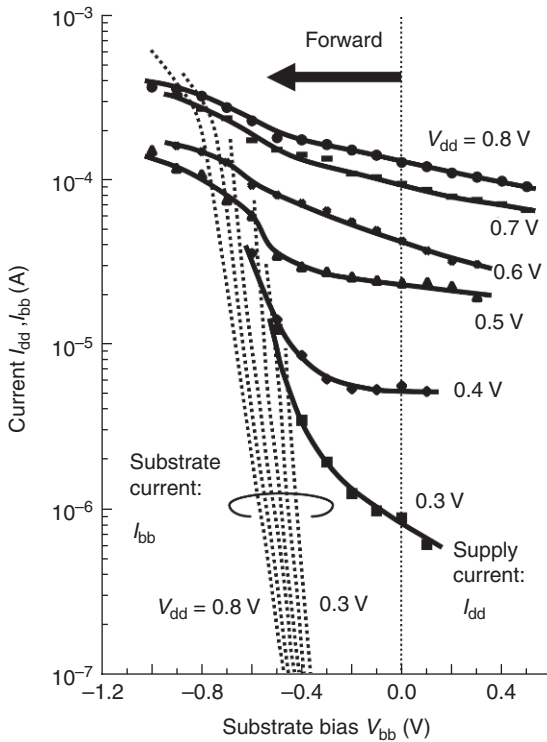


11.11 Simulated V_{\min} of inverter as a function of number of stages (Yasufuku, 2011).

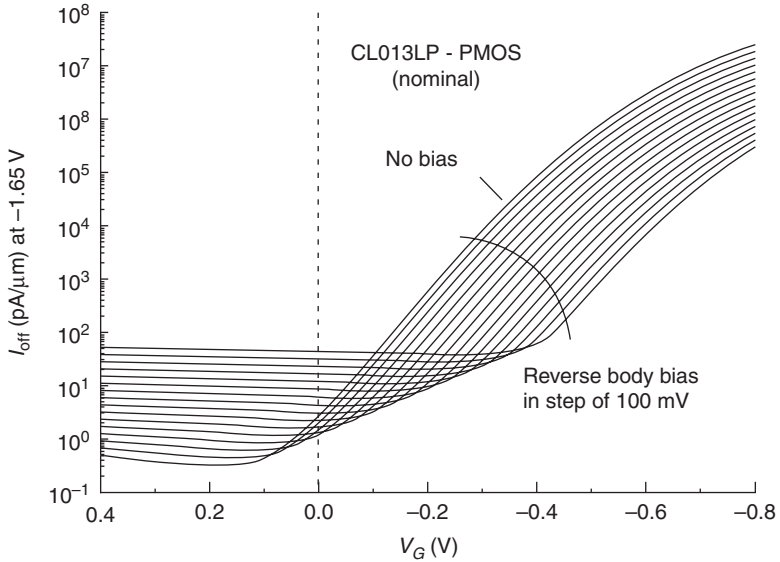
where k_B is the Boltzmann constant, T is absolute temperature, Q is the elementary charge, C_{dm} the maximum depletion capacitance at the channel region, and C_{ox} the gate oxide capacitance.

If we want to ensure the on-off ratio of six orders of magnitude, a gate voltage change of roughly 0.36 V is required where $S = 60$ mV/decade, the minimum value at room temperature, is assumed. Secondly, the turn-on voltage is another finite factor. This value is roughly the same as the gate overdrive voltage $V_{gs} - V_{th}$ in Equation [11.4] and is determined by the required I_{ds} value at the on state. In the case shown in Fig. 11.11, the sub-threshold operation is assumed. Thus the former value is very small and the latter value is zero.

As mentioned before, the operation with minimum energy, E , tends to significantly decrease the operation speed. Some compromise should be attempted to enhance speed performance to match the requirement from the applications. In other words, the task is maximising the gate overdrive voltage in Equation [11.4] for the proper speed while also securing the proper on-off ratio for the small leakage. The ABB technique, combined



11.12 Supply current and substrate current dependence on body bias voltage, V_{bb} (Miyazaki, 2002).



11.13 Drain current versus gate voltage in sub-threshold region (Lin, 2002).

with V_{dd} control is the best option for this compromise, as already shown in Fig. 11.8 (Miyazaki, 2002). This ABB scheme, however, is not always effective for the bulk CMOS circuits because of the increase in the substrate leakage current.

Under the strong forward bias condition, the operation speed increases. However, the leakage current rapidly increases through the pn junction between drain and body, as shown in Fig. 11.12 (Miyazaki, 2002). On the contrary, in the reverse bias condition as shown in Fig. 11.13 (Lin, 2002), the leakage current increases by increasing the reverse bias voltage due to the gate induced drain leakage (GIDL) and/or band-to-band tunnelling (BTBT) current at the drain junction.

11.4 Developing SOI devices with small variability and adaptive bias control

In this section, the device structure that solves the above problems is shown. The main requirements are:

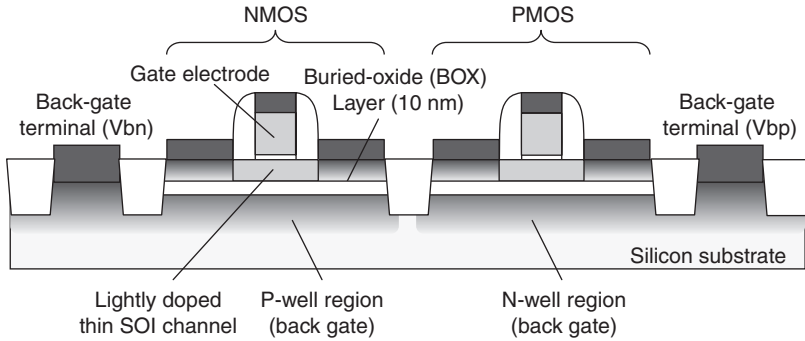
- small local variability that ensures low voltage operation with a small error rate and
- adaptive back bias controllability that enables optimisation between high operation speed (on state) and low leakage (off state).

The primary cause of local variation of the conventional bulk transistor is the random dopant fluctuation (RDF) in the channel region (described in Section 11.5). The structure to achieve a small RDF was proposed long before the intrinsic-channel (retrograde-channel) structure of the bulk MOSFETs (Aoki, 1990). This transistor structure is formed by using the epitaxial silicon growth in the channel region. However, the out-diffusion of impurities during the thermal process takes away the advantage of the intrinsic channel to some extent. In addition, the problem of drain leakage current is the same as for the conventional bulk transistors.

Around the same time, the novel SOI structure, known as the ultimate transistor structure, was proposed (Fukuma, 1988). This structure has a very thin silicon channel surrounded by insulator films and is also capable of back gate bias control. This was the first prototype of the planar FDSOI structure with back bias controllability. A revised form of this prototype structure and concept, involving process compatibility with the current CMOS technology and the V_{th} controllability for the low power application, was proposed (Tsuchiya, 2004), and named silicon on thin buried oxide (SOTB). Similar structures were reported after that (Chen, 2005; Fujiwara, 2005; Fenouillet-Beranger, 2007; Monfray, 2007; Cheng, 2009); named as ultra-thin buried oxide (UTBOX) FDSOI or ultra-thin body and BOX (UTBB), they are basically the same as SOTB.

The typical transistor cross-section and its features are shown in Fig. 11.14. The thicknesses of the SOI and BOX layers are both very thin (~ 10 nm) to improve short-channel-effect immunity and back gate bias sensitivity. Channel impurities are implanted into the silicon substrate (well region) through the SOI and BOX layers to control V_{th} while the impurity density in the SOI layer is kept low. This impurity profile is essential for reducing the RDF variability (see Section 11.5). In addition to the substrate doping, V_{th} is also controlled by the back gate bias voltage via the back gate terminal. Another important feature is hybrid integration of SOTB transistors with bulk transistors on the same wafer. Thanks to the thin SOI and BOX layers, the conventional bulk transistors can easily be fabricated removing only these layers. This feature is essential for the circuit design because the conventional circuits that use bulk CMOS can be ported with minimal change. Peripheral circuits, operating at higher voltages than the maximum voltage of the SOTB (~ 1.5 V), and electrostatic discharge (ESD) protection circuits can both be fabricated on the bulk region.

There are other types of intrinsic-channel structures with small local variability. The typical structure is the FinFET (Huang, 1999), which was invented 10 years before it was given the name, originally being called DELTA (Hisamoto, 1989). The derived structure from the FinFET, the tri-gate structure, was proposed (Doyle, 2003) and commercialised. In these structures, two or three gate electrodes surround the silicon body, shaped



Features:

1. Small local variability (RDF) due to lightly doped channel
2. Excellent short-channel-effect immunity due to thin SOI and BOX
3. Multiple V_{th} control by changing well impurity density
4. Back-gate bias control to minimise global variability and power consumption
5. Bulk transistors can be fabricated on the same wafer by removing SOI and BOX

11.14 Schematic cross-section and features of silicon on thin buried oxide (SOTB) transistor.

like a fin. The gate voltage is commonly applied to these gate electrodes (connected to each other). In general, the back bias control is not applied to this structure because the electrical potential of the thin silicon body is strongly controlled by these two or three gate electrodes.

In the case of utilising the very thin BOX layer below the thin body and the limited height of the fin, back bias control is possible, though the control coefficient is small (Nagumo, 2006). Another structure capable of the back bias control is the split gate type FinFET, named 4T (terminal) FinFET (Masahara, 2005). The electrical behaviour of the 4T FinFET is very similar to the SOTB-like planar structures. The one side of the gate electrodes acts as a front gate to turn on the transistor, and the other side acts as a back gate to control V_{th} . In the ordinary FinFET, the gate oxide thicknesses of front and back gates are the same. In the 4T FinFET, this significantly increases the S factor unless the back gate oxide is thicker than the front gate oxide by using a specific process.

11.5 Modelling variability

The local V_{th} variation mainly consists of a fluctuating number and position of discrete dopant atoms, known as random dopant fluctuation. There are many works discussing the effect of RDF on the V_{th} variability by simulation (Asenov, 1998). The analytical formulation of the RDF will be shown

to easily establish the effect of RDF as a guide to understand the FDSOI like structures.

In order to estimate the effect of discrete charge by dopants on V_{th} , the increment of the surface potential (just below the gate oxide interface) caused by placing the charge in a small volume in the depletion region is integrated in the depth direction. The dopant number fluctuation of each small region is presumed to be completely random. In classical bulk transistors with a uniformly doped channel (body) region, the V_{th} variation can be written as

$$\sigma V_{th} = \frac{q}{C_{ox}} \sqrt{\frac{N_{body} W_{dm}}{3LW}} \quad [11.9]$$

where N_{body} and W_{dm} denote the impurity density of the body region and maximum depletion width, respectively (Takeuchi, 1997; Taur, 1998).

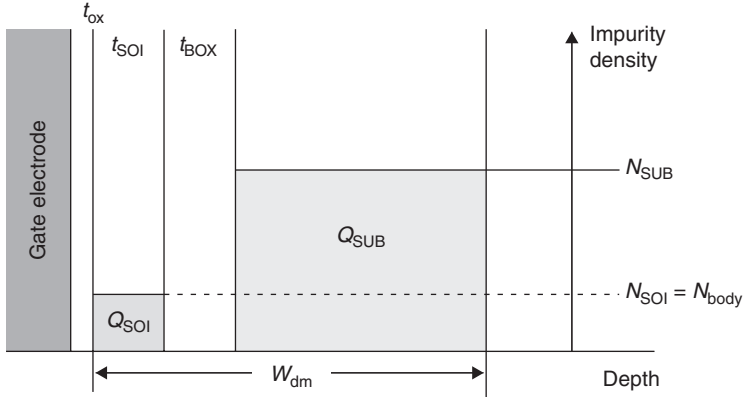
In the FDSOI structures, the effect of channel dopants only in the SOI body should be considered. The distribution is uniform in general. The V_{th} variation can simply replace W_{dm} by the SOI thickness t_{SOI} ,

$$\sigma V_{th} = \frac{q}{C_{ox}} \sqrt{\frac{N_{body} t_{SOI}}{3LW}}, \quad [11.10]$$

If the BOX layer is thin, the contribution from the dopants below the BOX layer should be considered. The equation is similar to the retrograde-channel case (Taur, 1998):

$$\sigma V_{th} = \frac{q}{C_{ox}} \sqrt{\frac{N_{sub} W_{dm}}{3LW}} \left(1 - \frac{x_s}{W_{dm}}\right)^{3/2}, \quad [11.11]$$

where N_{sub} and x_s denote impurity concentration below the BOX layer (assumed to be uniform) and the depth of the intrinsic region near the surface, respectively. If the x_s is large, that is, the intrinsic layer is thick and the doped layer below is thin, the V_{th} variation in Equation [11.11] becomes very small. This is the reason why the V_{th} variation of the intrinsic-channel (retrograde-channel) structure is small. In the SOTB-like structure, the intrinsic region consists of the SOI and BOX layers. The depth profile is schematically shown in Fig. 11.15. Because the dielectric constant of the BOX layer is smaller than that of silicon, the thickness is effectively greater than the physical BOX thickness t_{BOX} . The V_{th} variation can thus be written as (Sugii, 2010)



11.15 Depth profile of impurity density in SOTB.

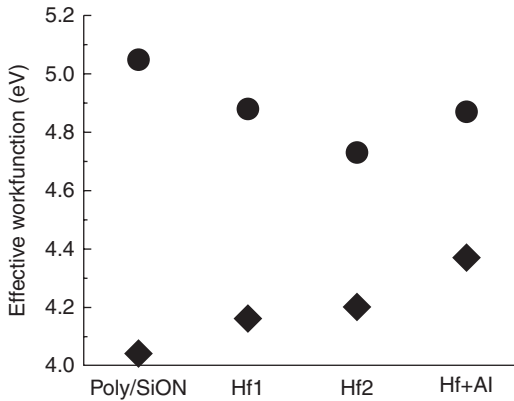
$$\sigma V_{th} = \frac{q}{C_{ox}} \sqrt{\frac{N_{sub} W_{dm}}{3LW}} \left(1 - \frac{t_{SOI} + (\epsilon_{Si}/\epsilon_{ox}) t_{BOX}}{W_{dm}} \right)^{3/2}. \quad [11.12]$$

The overall V_{th} variability of this structure can be calculated as the root sum squares of σV_{th} s in the formulas of Equations [11.10] and [11.12]. In this structure, the small V_{th} variability is achieved both by the small N_{body} in Equation [11.10] and the remoteness of the impurity doping region in Equation [11.12]. In many simulation studies, small variability due to reduced RDF for FDSOI devices has been predicted, and also many results of actual devices show very small variability in the FDSOI devices, as is shown later (Section 11.7).

11.6 Device design for ultralow-voltage operation

Controlling V_{th} is of utmost importance in the transistor design. In order to obtain a sufficient speed performance, lower V_{th} is preferred. However, higher V_{th} is preferred for low leakage. Without the ABB control, this trade-off is hard to rectify, especially for the ultralow voltage operation because the voltage margin is limited. For the transistor design with ABB, there are two methods. One is a low V_{th} with zero back bias (ZBB), applying reverse back bias (RBB) under the standby state (RBB standby mode). The other is a high V_{th} with ZBB, applying FBB under the active state (FBB boost mode).

The V_{th} value of a MOS transistor is determined by the flat-band voltage, V_{FB} , and the depletion-layer charge. The appropriate value of work function of the gate electrode is selected to control the V_{FB} . The depletion-layer charge is controlled by the impurity doping of the well region. In general, the depletion-layer charge in FDSOI is lower than in conventional bulk



11.16 Effective work function control of high-k/SiON gate dielectric.

transistors because of low impurity density of the SOI layer and remote doping below the BOX layer. The V_{th} value of the FDSOI transistor with the conventional polysilicon gate electrode of the band-edge work function is roughly 0 V. By using the midgap metal gate electrode, the V_{th} value is about 0.4 V and is suitable for low leakage applications. For the ultralow voltage operation, however, this V_{th} level is rather high, and the FBB boost mode is thus preferred. On the other hand, for the RBB standby mode, the intermediate V_{th} value (about 0.2 V) is preferred. This V_{th} level can also be achieved by the work function control of the gate electrode. Various metal electrodes can be used (Faynot, 2010). The cost effective way is to use the high-k dielectric combined with the conventional polysilicon gate electrode (Yamamoto, 2012). As shown in Fig. 11.16, by introducing a suitable amount of Hf and Al to the conventional SiON dielectric film, the effective work function can be tuned to quarter-gap values (about 4.4 and 4.8 eV for N- and PMOS, respectively).

11.6.1 Device design for back bias control: BOX thickness

As described earlier, the back bias control is essential to optimise energy consumption of the CMOS circuits, especially for ultralow voltage circuits. Regarding the transistor design, the substrate (back) bias coefficient is an important parameter because the higher coefficient lowers the required back bias voltage to sufficiently change the V_{th} . The substrate bias coefficient, m , of the bulk transistor relates to the Equation [11.8], and is written as

$$m = \left(1 + \frac{C_{dm}}{C_{ox}} \right). \quad [11.13]$$

The coefficient of V_{th} change by the substrate bias voltage, V_b , that is, $\partial V_{th}/\partial V_b$, is $m - 1$ at around $V_b = 0$. It is easy to see that $m - 1$ and S are in a trade-off relationship. One wants to decrease S as little as possible to increase the on-off ratio with a small change in the gate voltage; however, $m - 1$ decreases corresponding to the S decrease. In the FDSOI structure, the maximum depletion capacitance, C_{dm} , is a series capacitance composed of the SOI body capacitance, C_{SOI} , the BOX layer capacitance, C_{BOX} , and the depletion-layer capacitance below the BOX, C_{sub} , and is written as

$$m = 1 + \frac{1}{C_{ox}} \left(\frac{1}{C_{SOI}} + \frac{1}{C_{BOX}} + \frac{1}{C_{sub}} \right). \quad [11.14]$$

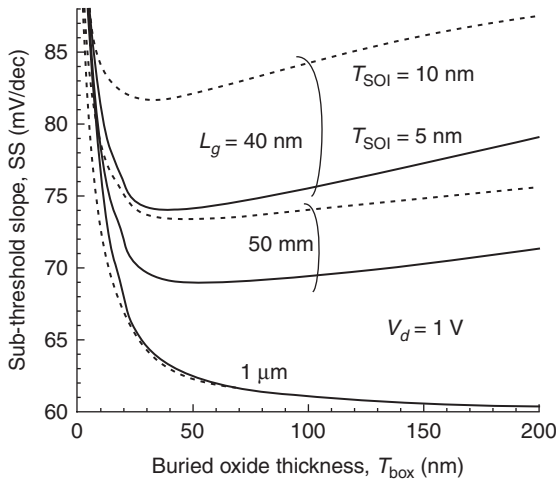
Simply replacing the term $(1 + (C_{dm}/C_{ox}))$ in Equation [11.8] to the corresponding term in Equation [11.14], obtains S of this structure. The m and S increase with decreasing SOI thickness, decreasing BOX thickness, or increasing substrate impurity density.

The above discussion only applies to the long-channel case. In the short-channel transistor, the short-channel effect (SCE) such as drain induced barrier lowering (DIBL) and charge sharing should be considered. Figure 11.17 shows S (sub-threshold slope, SS in the figure) as a function of t_{BOX} (Numata, 2004). In the long-channel case ($L_g = 1 \mu\text{m}$), S (at room temperature) steadily increases with decreasing t_{BOX} . This behaviour can be described by Equation [11.14]. For the short-channel transistors ($L_g = 50$ or 40 nm), on the contrary, S decreases with decreasing t_{BOX} and minimises at around $t_{BOX} = 30 \text{ nm}$. This is because S is mainly determined by DIBL at $t_{BOX} > 30 \text{ nm}$. With decreasing t_{BOX} or t_{SOI} , S decreases because the SCE immunity improves. With decreasing L_g , S increases for the same reason. Note that the back bias coefficient, m , also changes due to the SCE effect. This phenomenon can be explained by charge sharing (Yau, 1974). The design of t_{SOI} and t_{BOX} should thus be considered to compromise the trade-off between m and S by taking the SCE into account.

On the circuit design, the back bias coefficient poses another trade-off. Transistor stacking is widely used in the circuits. The substrate bias coefficient has a strong influence on the characteristic of the stacked transistor, especially for low voltage operations. The advantage of the FDSOI with thick BOX is nearly zero bias coefficient. The back bias controllability of the thin BOX structure is thus obtained at the expense of the stacked transistor characteristics.

11.6.2 Device design for back bias control: well structure

In FDSOI, there is no leakage path to the substrate from either the source or drain regions due to the BOX insulating layer. In applying the back bias,



11.17 Sub-threshold swing as a function of BOX thickness, t_{BOX} (Numata, 2004).

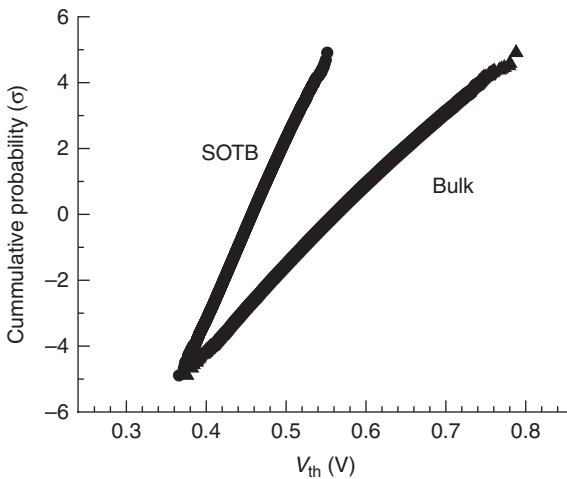
however, the leakage path between the well regions below the BOX layer should be considered. In the structure shown in Fig. 11.14, p- and n-wells are below the active regions of N- and PMOS transistors, respectively. In the reverse body biasing, the voltages at the p- and n-wells are negative and positive, respectively. The pn junction between the wells is negatively biased, and thus, the diode leakage is negligibly small. In the forward body biasing, the reverse is true. If the forward bias voltage exceeds ~ 0.4 V, a significant amount of leakage current flows from the p-well to the n-well. In this structure, maximum forward bias voltage is limited at less than ~ 0.4 V. This is suitable for the RBB standby mode. On the other hand, the flip-well structure is proposed (Weber, 2010), where simply the doping type is changed. This significantly lowers V_{th} , like a normally on-type bulk transistor. The V_{th} control is carried out by selecting the gate electrode material that exhibits larger V_{FB} than usual. In this structure, the maximum forward bias voltage is unlimited but the minimum reverse bias voltage is limited at higher than -0.4 V. This is suitable for the FBB boost mode.

If one wants to use a wide back bias voltage range from reverse to forward, other structures should be introduced, such as the dual shallow trench isolation (STI) structure (Grenouillet, 2012). In this structure, the leakage current between the wells is prevented by deep STIs. Note that the leakage between the wells can be prevented without the deep STIs if there is plenty of space for isolation. In the analogue circuits using larger transistors, this approach can be possible. Another structure is the double-BOX structure (Horiuchi, 2003; Khater, 2010). In this structure, another BOX layer is placed below the well region and each well is completely isolated by STI regions and sandwiching BOX layers.

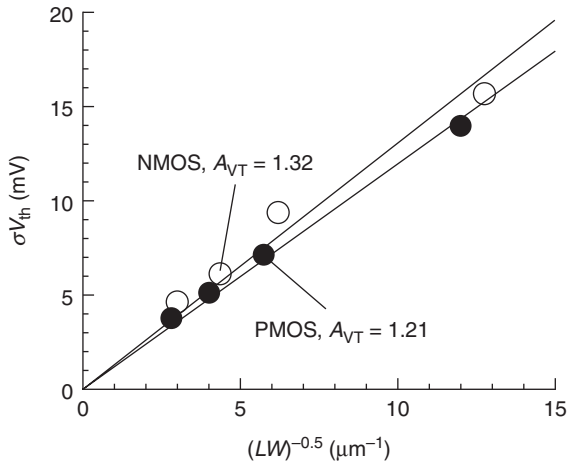
11.7 Assessing variability in fully depleted silicon-on-insulator (FDSOI) devices

There are many studies on the V_{th} variability of FDSOI devices, and some studies on the variability data based on large-scale integration. For conventional bulk transistors, the V_{th} variability is mainly caused by RDF and exhibits the normal distribution behaviour for one million transistors (\pm five sigmas) (Tsunomura, 2008). There is interest in how the V_{th} variation of FDSOI behaves with less RDF. The recent result of measuring the V_{th} variation of one million SOTB transistors (Yamamoto, 2013) shows a similar normal behaviour and σV_{th} of less than half of the bulk transistors of the same size, as shown in Fig. 11.18. This is useful information for circuit designers because the local variation of the FDSOI can still be described in the same framework as that in the bulk transistors based on the normal distribution of variability. Moreover, it was shown that the local variation of the FDSOI with very small RDF also obeys Pelgrom's law, as shown in Fig. 11.19 (Yamamoto, 2013). It can be seen that the FDSOI's local variation components behaves even more randomly: linearity of the plot of SOTB is better than that of bulk, as shown in Fig. 11.18, and it is natural to obey Pelgrom's law. Note that the A_{VT} value is the slope of the plot in Fig. 11.19. Figure 11.20 compares the A_{VT} values of transistors of various structures as a function of gate oxide thickness, t_{ox} , because A_{VT} is proportional to t_{ox} (Equation [11.6]). Data in the figure except for SOTB are collected from studies published in the last 3 years. Three lines denote linear regression of bulk, FinFET, and FDSOI data. The SOTB and FDSOI transistors exhibit very small A_{VT} values among them.

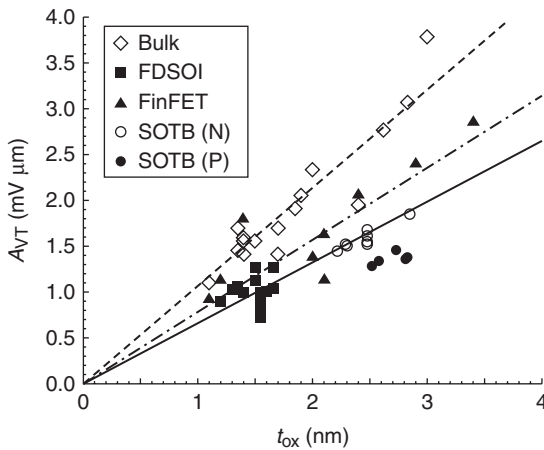
For the circuit performance, the variability of on-state current is important because it directly reflects the variation in speed (Equation [11.3]). Smaller



11.18 Five-sigma V_{th} variation of SOTB and bulk transistor.

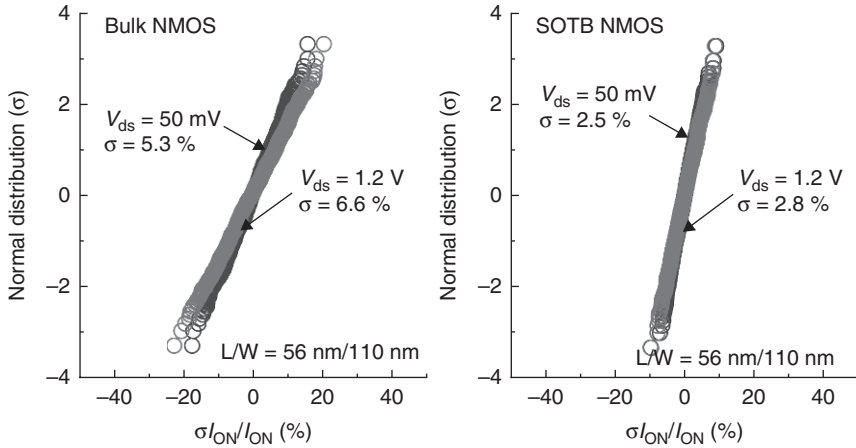


11.19 Pelgrom plots of SOTB N- and PMOS transistors.

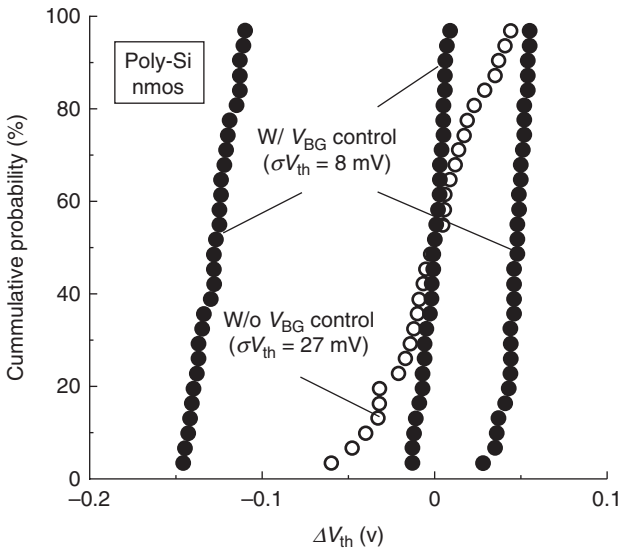


11.20 Comparison of A_{VT} values for various transistor structures (t_{ox} corresponds to the equivalent thickness under the inversion state in this figure.)

on-current variation than of the bulk devices was demonstrated (Mizutani, 2012). As shown in Fig. 11.21, the on-current variation also shows a normal behaviour both for the bulk and the SOTB. The variation for the SOTB is less than half of the bulk transistors. It is shown that this improvement is also attributed to the reduction of RDF due to the small amount of impurities in the channel region. Both reduction of current-onset voltage (COV) variation (Tsunomura, 2009) and S factor (Mizutani, 2013) contribute to decrease the on-current variability.



11.21 On-current variability of SOTB and bulk transistor (Mizutani, 2012).



11.22 Reduction of die-to-die variation with back bias control (Ishigaki, 2008).

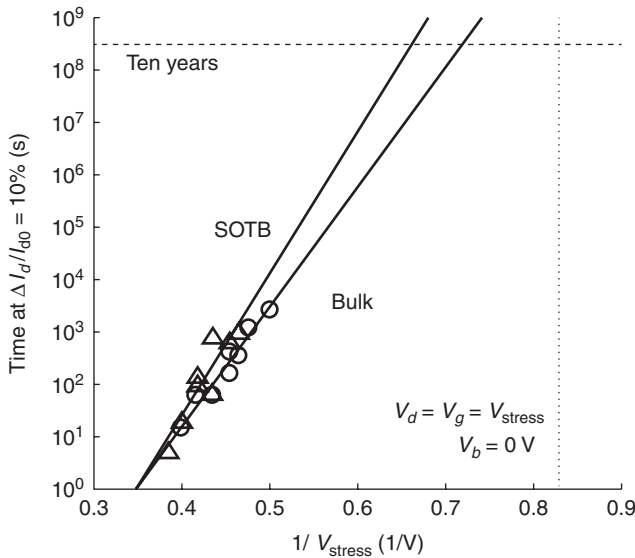
The above results are on the local variation reduction of the FDSOI. Decreasing the global (systematic) variation, such as die-to-die variation, is also of practical importance. The back gate biasing can reduce the global variation, as shown in Fig. 11.22 (Ishigaki, 2008). Without the control, the range of V_{th} values of the representative transistor of each chip exceeds 0.1 V (open symbols). The back bias control with voltage step of 0.2 V reduces the range to one third. If the voltage step is smaller, the variation can further

be reduced. Another interesting feature is that the median V_{th} value can be widely controlled by the back gate bias, as shown in the same figure (three sets of closed symbols). Corresponding to the reduction of V_{th} variation, the variation of off-current also reduces from two orders (range of max–min) to less than half order of magnitude (not shown).

11.8 Assessing the reliability of FDSOI devices

In order to commercialise a new device, it is mandatory to secure reliability. Although the reduction of operating voltage can ease a reliability requirement, it is important to evaluate the reliability of the new FDSOI transistors. In particular, the FBB operation increases the energy of carriers, and its reliability should be carefully evaluated.

The hot-carrier injection (HCI) and negative bias temperature instability (NBTI) for the SOTB was evaluated (Ishigaki, 2011). The HCI degradation is due to the channel hot-electron injection and its lifetime of the SOTB is longer than that of the bulk transistor, as shown in Fig. 11.23. This is because the lateral electric field at the drain edge is weaker for the SOTB without the halo implantation that is usual for bulk transistors. For the effect of back biasing, the RBB can increase the longitudinal electric field, but on the other hand, the FBB can increase the channel electron energy. The results show that, for both cases, the HCI lifetime of the SOTB exceeds ten years at 1.2 V operation. The NBTI degradation for the SOTB can be



11.23 Hot-carrier injection lifetime of SOTB and bulk transistors (Ishigaki, 2011).

explained by the conventional reaction/diffusion model. The lifetime of the SOTB is also longer than that of the bulk, and exceeds 10 years due to the existence of the BOX layer and the weaker longitudinal electric field of the SOTB.

Another important point is the reliability of bulk transistors integrated with the thin BOX FDSOI (SOTB) transistors on the same wafer. The bulk transistors can be fabricated simply by removing both the SOI and the BOX layers. In other words, the hybrid bulk transistors are fabricated on the surface of the support wafer below the BOX layer. The quality of the surface depends on the bonding process of the SOI wafer. Experimental results (Ishigaki, 2008) indicate there is no particular problem. Mobility of the hybrid bulk transistor is the same as that of the conventional bulk transistor. Time-dependent dielectric breakdown (TDDB) lifetime is more than ten years for the 3.3 V operation that is a typical use for the hybrid bulk transistor in the input/output (I/O) circuits.

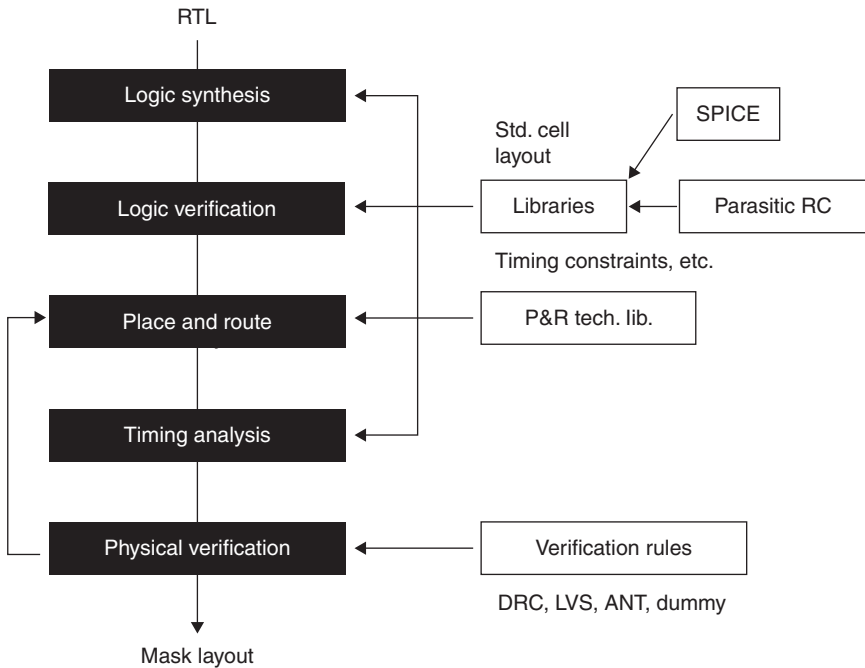
11.9 Circuit design of FDSOI devices

This section describes design environment that is necessary for the FDSOI integrated circuits, FDSOI's advantages in analog and RF circuits, and ultralow voltage circuit results.

11.9.1 Digital integrated circuit (IC) design flow

The modern CMOS integrated circuit (IC) design is built entirely using a series of electronic design automation (EDA) tools. Compatibility with the existing design flow and reusability of the existing circuit intellectual properties are important for designing circuits or macros with a new device architecture without increasing the design cost. The design flow for the FDSOI (with back biasing), as shown in Fig. 11.24, is very compatible with the existing design flow. The EDA tools and their file formats are completely the same as the existing ones from the register transfer level (RTL) to the layout (graphic database system: GDS). In many cases, the ICs include both the FDSOI and bulk transistors (the hybrid integration as mentioned in Section 11.4).

The design (mask) layer, layout rules, and their verification files (including the antenna effect) should be revised to match the transistor portfolio. The technology files, such as delay libraries and timing constraints, should be prepared with the Simulation Program with Integrated Circuit Emphasis (SPICE) parameters and the parasitic resistance and capacitance (RC) components of the new transistors. These technology files are used in each stage of the design: logic synthesis, logic verification, placement and routing, and timing analysis. The wiring architecture will be the same in many cases,



11.24 Logic IC design flow for FDSOI.

but special care for the back bias power lines should be given. The overall change in the design flow will not, however, be large.

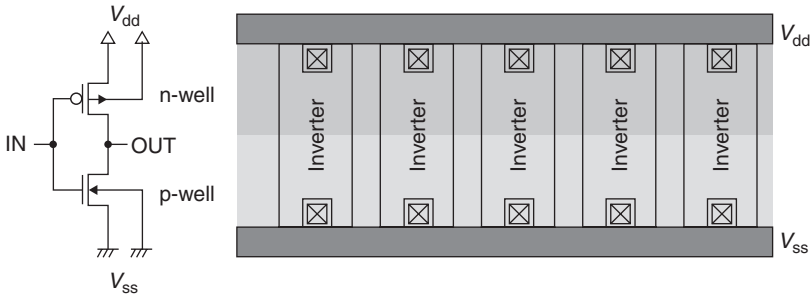
11.9.2 SPICE modelling

The well-matched SPICE parameters for new transistors are indispensable to the circuit design. The existing transistor model for the bulk transistor cannot be used accurately because the transistor characteristics when varying the back bias voltage are difficult to reproduce. New SPICE models that are fully compatible with the FDSOI with back biasing have been developed, such as HiSIM-SOTB (Miura-Mattausch, 2012) and BSIM-IMG (Khandelwal, 2012). Both models are based on the surface potential expression and can represent the back bias behaviour more accurately than conventional models. The model verification is currently still underway but will be used for commercial circuit design in the near future.

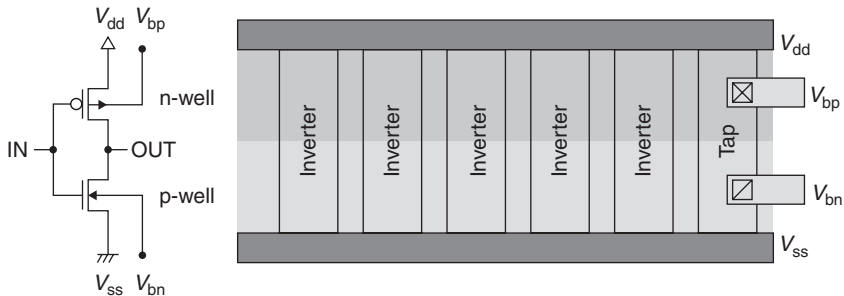
11.9.3 Building standard cell libraries

In the logic IC design, a number of standard cells that have various logic functions are prepared. Basic cell layout for the FDSOI is common with

Without body bias (well connection inside)



With body bias (well connection with tap cell)



11.25 Standard cell design for back biasing.

that of the bulk transistor because the structure of the active and the isolation regions of the FDSOI is generally the same as the bulk transistor of the same feature size. Since the driving ability of the transistor is different, the transistor widths of N- and PMOS might be changed.

The substrate biasing can change the structure and the placement of standard cells because the substrate bias voltages (of N- and PMOS) should be supplied to the well regions in each standard cell. In general, without back biasing, the p- and n-well regions are connected to the ground (V_{ss}) and the V_{dd} lines, respectively. The well connection is carried out in two ways: connection inside the cell, or using a specific cell for the connection, known as a tap cell. Figure 11.25 schematically shows an example. In the former case, only by placing the standard cells, all the well regions are automatically connected to the V_{ss} or V_{dd} . However, in order to apply back bias voltages, the standard cell layout should be modified to disconnect the well taps from V_{dd} and V_{ss} and the well taps should be connected to the substrate bias power lines: V_{bn} and V_{bp} . In the latter case, the cell layout and the placement are the same regardless of the back biasing. The tap cells are placed with appropriate spacing, then connected to the V_{bn} or V_{bp} lines in order to apply

back bias. These cells and wiring architectures are designed by taking many trade-off relationships into account: standard cell area penalty, well voltage stability, robustness against the substrate noise, packing density of standard cell placement, wiring resource, and so on.

The characterisation of the FDSOI cells is carried out in the same way as the bulk cells. The delay characteristics of the cells are evaluated by the SPICE simulation and the parasitic RC extraction with a calibration by using the real silicon hardware data. The cell library is completed by consolidating the delay information as well as logic, layout (size), and terminal information.

11.9.4 Peripheral circuits and ESD protection

The logic IC should handle several levels of voltages. Although the supply voltage can decrease less than 1 V in the core logic circuits and the embedded memory such as SRAM, the supply voltage of the peripheral circuits cannot be lowered because it is determined by the signal level of I/O terminals of the IC chip. In addition, the electrostatic discharge (ESD) protection circuits should be implemented near these external terminals. The hybrid integration (Section 11.4) enables the FDSOI devices to handle high voltage such as 1.8 or 3.3 V for the peripheral circuits and to implement the ESD circuits. Conventional bulk structures are generally used in these circuits. The ESD protection circuit on SOI can be fabricated by using the gated-diode architecture, although the robustness against an ESD event is weaker than that with bulk technology. Robustness is improved by thinning the BOX layer due to improved thermal dissipation through the BOX layer of poor thermal conductivity (Benoist, 2010).

The important circuit blocks are the level shifter and the power supply. In general, the signal level of the peripheral circuits does not scale down, unlike the core logic circuits. The signal level difference can increase with decreasing V_{dd} of the core circuits. It is therefore important to design the level shifter circuit with low power consumption. Likewise, the voltage difference between the V_{dd} of the core circuits and the power line tends to increase with decreasing the V_{dd} . Moreover, current consumption can increase at low V_{dd} . A highly efficient power regulator is needed to decrease the total power consumption of the low voltage operation chip. The back bias voltage generator is also important. Decreasing the current consumption of this circuit is especially significant for the circuits that use the RBB in standby mode. In the FDSOI circuits, the current consumption of the back bias voltage generator can be decreased because the load current of the FDSOI back bias line is substantially smaller than that of the bulk circuit due to the lack of the leakage path between drain and substrate regions. Regarding the power supply for ULP applications, the highly efficient dc–dc converter is strongly

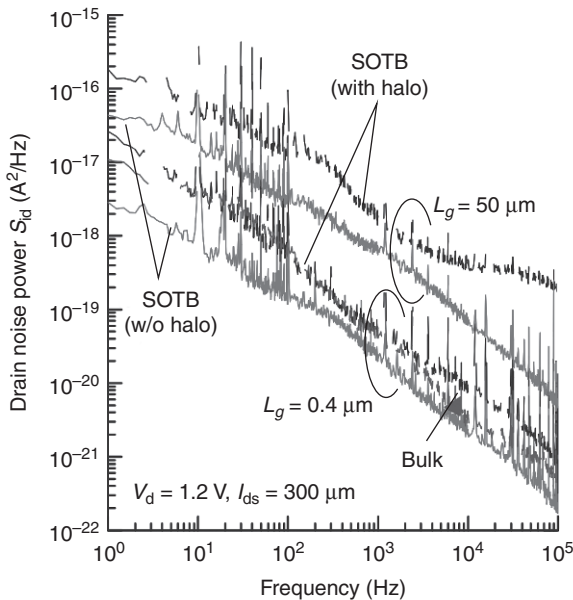
needed as it can extend the usage of various energy harvesters and significantly increase battery life.

11.9.5 Analogue and RF circuits

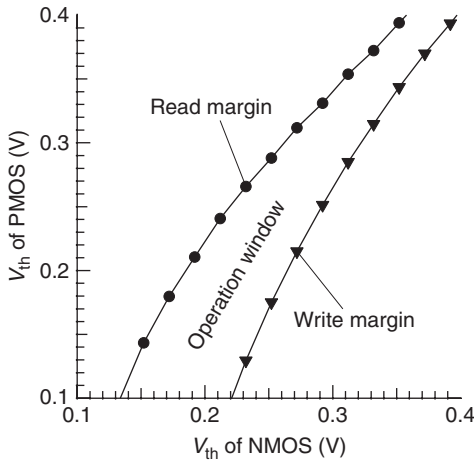
The FDSOI has several advantages over bulk transistors for analogue and RF circuits. The reduced local V_{th} variability (smaller A_{VT}) improves the matching characteristics of the differential amplifiers and reduces offset voltage. The drain conductance of the saturation region is smaller for the FDSOI than the bulk due to the improved SCE immunity (smaller DIBL and reduced channel-length modulation). This can increase the gain of the amplifiers. The structure without halo implantation increases the gain by about six times (Hartmann, 2012) and reduces the $1/f$ noise as shown in Fig. 11.26 (Tsuchiya, 2009) as well as improving reliability (Section 11.8). These advantages arise due to the reduction in the vertical electric field and the implantation damage.

11.9.6 SRAM verification

The SRAM circuit is the greatest obstacle to reducing the operating voltage of the logic ICs, as shown in Fig. 11.9 (Chandrakasan, 2010). Owing



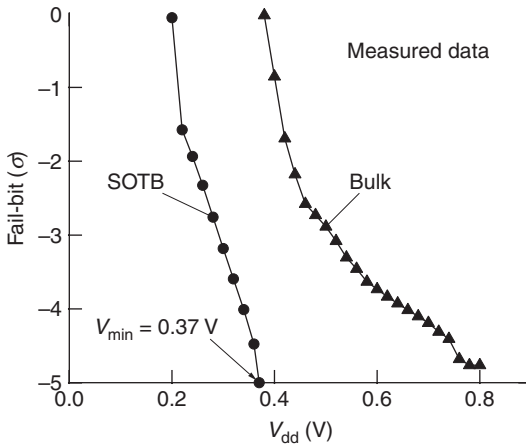
11.26 Drain noise power of SOTB and bulk transistors (Tsuchiya, 2009).



11.27 V_{th} operation window of 2Mbit SOTB SRAM at $V_{dd} = 0.4$ V.

to a significant reduction in local V_{th} variability for the large number of transistors, as shown in Fig. 11.18, the 2 Mbit SRAM operation at less than 0.4 V was demonstrated (Yamamoto, 2013). Through the SPICE characterisation of the SRAM cell transistors and the SRAM stability simulation that is proposed by (Yamaoka, 2004), the operation at 0.4 V is estimated to be possible if the A_{VT} value is ~ 1.3 mV μ m, as shown in Fig. 11.27. The safe operation window at 0.4 V is the area between the two curves (read margin and write margin). The V_{th} values of N- and PMOS SRAM cell transistors should be set in this area. A fail-bit count characteristic is shown in Fig. 11.28 for the SOTB and bulk SRAM of the same layout. The distribution of the fail-bit characteristic is smaller for the SOTB than for the bulk and the minimum operating voltage, V_{min} , is 0.37 V, that is about half of that of the bulk SRAM. It is shown that small cell-current variability, mainly due to the small V_{th} variability, contributes to improving SRAM cell stability at low voltages such as 0.4 V (Mizutani, 2013).

Moreover, the back bias operation offers a strong feature for the operation stability against temperature variation. Without the back bias, the SRAM that operates at less than 0.4 V operates neither at 80°C nor -30°C without increasing the voltage. By applying appropriate bias voltages independently for N- and P-type transistors in the SRAM cell, the V_{min} again reduces to less than 0.4 V at both temperatures (Yamamoto, 2013). Moreover, the V_{th} of SRAM designed for the low voltage operation should be lower than that for the higher operation voltage (such as 1.2 V). This leads to higher cell leakage current under operation. The RBB control also enables leakage current to be reduced under the standby state, while maintaining cell retention.



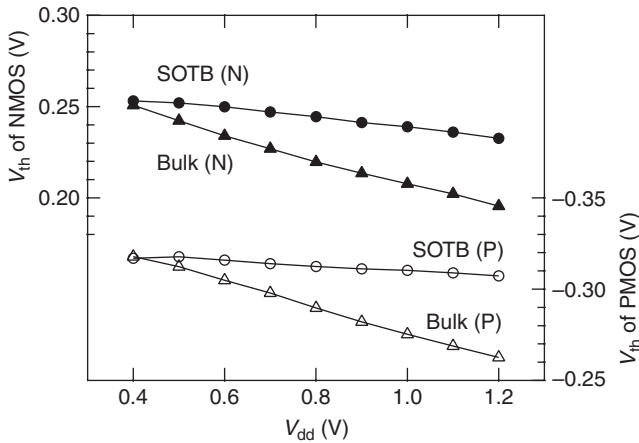
11.28 Fail-bit count as a function of V_{dd} for 2Mbit SOTB SRAM.

11.9.7 Ring oscillator and logic circuit verification

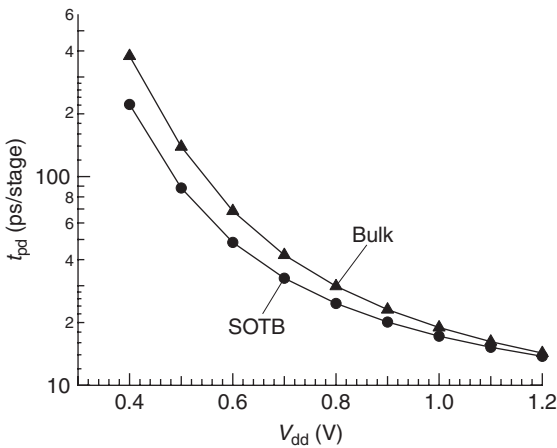
Improved electrical characteristics, such as smaller DIBL, S factor, and local variability, enhance the speed performance of circuits, especially at lower voltages. The data comparing the ring-oscillator delay of the 28 nm bulk and FDSOI (Hartmann, 2012) shows that the speed of the FDSOI is 33% and 400% higher than that of bulk at 1.3 and 0.5 V, respectively. In general, V_{th} of both transistors at different voltages can change because the DIBL values are different. The interest lies in how much faster the FDSOI is than the bulk under conditions of the same V_{th} . As shown in Fig. 11.29 (Makiyama, 2013), V_{th} of FDSOI (SOTB) and bulk at 0.4 V are the same, but at higher V_{dd} , the V_{th} of SOTB has been always higher because of smaller DIBL. The ring-oscillator delay at various V_{dd} is shown in Fig. 11.30 (Makiyama, 2013). At 0.4 V, the SOTB is roughly twice as fast as the bulk device at the same V_{th} . At V_{dd} higher than 0.4 V, the delay of the SOTB is always smaller than or equal to the bulk; nonetheless the V_{th} of the SOTB is always higher. These data verify the speed advantage at low voltage for the FDSOI.

Another advantage is speed variability. It was shown that the local delay variability of the SOTB is smaller than bulk because of weak dependence of the delay on the number of stages in the ring oscillators (Makiyama, 2013) because of the smaller local V_{th} variability. Moreover, the die-to-die back bias control can significantly reduce the global variability, that is, die-to-die variability of the delay.

Improvements in energy efficiency by the FDSOI have been demonstrated. The results of the low-density parity-check (LDPC) decoder comparing the



11.29 V_{dd} dependence of V_{th} for SOTB and bulk transistors.



11.30 Ring-oscillator delay for SOTB and bulk as a function of V_{dd} .

28 nm bulk and FDSOI (Flatresse, 2013) show that the total power consumption at the same frequency (207 MHz) reduces to 51% of the bulk power consumption with the FDSOI by reducing the V_{dd} from 1.0 to 0.7 V and by applying FBB of 1.0 V. Another significant power reduction was demonstrated by the post-layout timing and power analysis of the reconfigurable accelerator known as cool mega array (CMA). The bulk CMA operates at 1.2 V and 200 MHz, and the SOTB version operates at 0.4 V and 50 MHz (Su, 2012). The active power of the SOTB CMA is roughly one tenth of the bulk CMA. The total energy, considering both the operation power and the leakage power of the SOTB CMA, is 40% of the bulk CMA.

11.10 Future trends

This section briefly mentions a system level power optimization and a future transistor technology that can further reduce energy consumption.

11.10.1 Total power optimisation in sensor nodes

The main application of ULP electronic devices is considered to be the sensor-network system, as described in Section 11.1. Further reduction in power consumption can extend the opportunities to apply this technology and improve the function of the system. In the sensor-network nodes, the power consumption of the wireless communication (both the receiver and the transmitter) is the issue. Intermittent operation can reduce the power consumption. The appropriate procedure or algorithm of the watch-dog operation can reduce the power of the receiver. Increasing the interval of the data transmission and decreasing the data amount (data rate) can reduce that of the transmitter. In order to reduce the data amount, it is important to increase the on-site data processing or data compression by taking advantage of improved energy efficiencies of the logic circuit blocks.

11.10.2 Further E reduction: super-steep transistors

The fundamental limitation of conventional CMOS (including FDSOI) for improving energy efficiency is the switching characteristics of the transistor, as mentioned in Section 11.4. The super-steep transistors with very small S factor such as I-MOS (Gopalakrishnan, 2005), TFET (Aydin, 2004), and mechanical relay device (Kam, 2009) have the possibility of significantly reducing the energy per operation. The minimum energy per operation can be reduced to less than 10^{-17} J by the relay device, whereas that of the conventional CMOS exceeds 10^{-16} J. In the post-scaling era, it will be especially important to progress energy-aware research and development in designing the electronic system from various aspects such as system, architecture, circuit, device, and material.

11.11 Acknowledgment

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3D integration of silicon-on-insulator (SOI) integrated circuits (ICs) for improved performance

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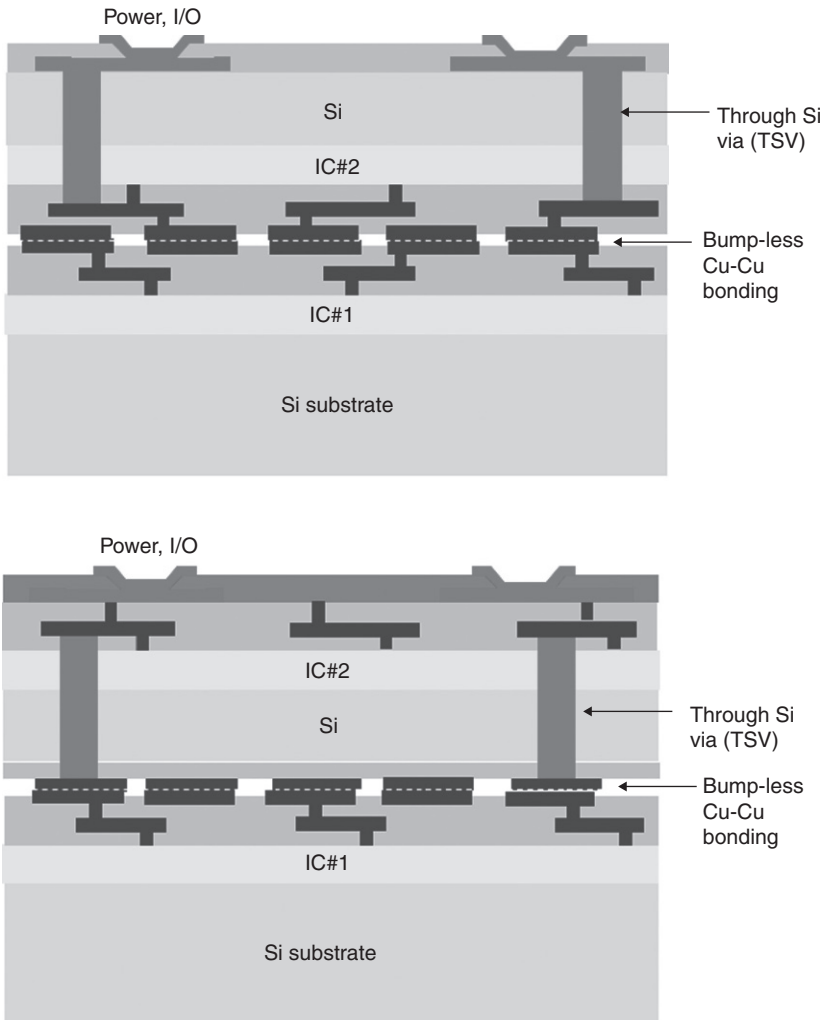
Abstract: Three-dimensional integrated circuit, 3D IC, integration is currently being investigated for continuous performance enhancement and functional diversification in future circuits and systems. SOI wafers uniquely allow ultra-thin Si layer transfer and stacking without the need for high aspect ratio TSV, usually needed in bulk Si 3D IC. This platform promises extremely high density of vertical interconnects between the active layers in 3D IC as technology scales. This chapter outlines material and process requirements of SOI-based 3D IC. Generic and customized process flows are presented. Wafer bonding technology is a key enabler in this technology and it is covered from the perspective of SOI-based 3D IC.

Key words: 3D IC, wafer bonding, thinning, through silicon via (TSV), plasma activation, handle wafer.

12.1 Introduction

Three-dimensional (3D) integration has emerged as a critical performance enabler for integrated circuits, at a time when the microelectronics industry is faced with unprecedented scaling barriers, which have arisen due to fundamental physics and economic constraints. Three-dimensional integration provides a mechanism for space transformation of the traditional planar implementation of integrated circuits into three-dimensional space. It therefore provides a pathway to augment geometrical scaling for further performance enhancement ('More Moore'), as well as enables functional diversification ('More than Moore') to improve higher-level system operation. Three-dimensional integration, in the form of a vertically stacked and electrically connected 3D stack consists of a few layers of integrated circuits, has a long list of technical merits in terms of form factor, density, performance, power, functional diversification, and cost.

At its core, 3D integration is simply the process of vertically stacking circuits and forming electrical connections between them. Mainstream 3D IC



12.1 (Top) Face-to-face or face-down stacking; (bottom) back-to-face or face-up stacking.

is usually accomplished in bulk silicon that is thinned down to a thickness that can be handled effectively and reliably. The thinned chips or wafers are connected with through silicon via (TSV) and bonded with copper/tin (Cu/Sn) Cu/Sn micro-bumps or potentially with fine pitch Cu–Cu in the future. Figure 12.1 contains schematics of 3D IC in the face-to-face and back-to-face stacking orientations conceptually.

With the emergence of 3D integration, TSV is an essential enabler that almost all major semiconductor companies have on their technology

Table 12.1 Global interconnect level 3D-SIC/3D-SOC roadmap (2010 update)

Global level 3D-stacking	2009–2012	2013–2015
Min TSV diameter (μm)	4–8	2–4
Min TSV pitch (μm)	8–16	4–8
Max TSV depth (μm)	20–50	20–50
Max TSV aspect ratio	5:1–10:1	10:1–20:1

roadmaps. There is a large variation in TSV size and density, and Table 12.1 is a summary modified from Table INTC3 of the 2009 International Technology Roadmap for Semiconductors (ITRS) on Interconnect (2010 Update).¹

The implementation of 3D IC on bulk Si wafers with TSV technology, which is seemingly a straightforward process, poses several challenges as discussed below:

- The thinning process on bulk Si wafers, particularly those with larger diameter, is a challenging step as requirements on final thickness uniformity and warpage control are stringent. At the same time, handling of thin wafers is always a concern as they are mechanically weaker. Therefore, the industry has called for final Si thickness in the vicinity of 20–50 μm for future 3D IC application. This has inevitably resulted in a TSV aspect ratio in the range of 10:1 to 20:1 in the 2013–2015 time frame as can be seen from Table 12.1. TSV with high aspect ratio is not favourable from the process point of view since conformal deposition of liner, barrier, and seed layers becomes limited. Cu plating in high aspect ratio TSV, especially when a super-conformal process is not available, can lead to incomplete filling (i.e., formation of voids due to premature pinch off) which is undesirable. At the same time, long process time and high cost of ownership are incurred.
- In TSV technology, the deep via is often filled with Cu as the conductor of choice. Since Cu has a larger coefficient of thermal expansion (CTE) than that of Si, large thermo-mechanical stress is induced in the surrounding Si. This leads to a number of reliability concerns such as Cu–TSV delamination from Si, Cu protrusion (which results in deformation of planar Cu interconnect on top) and Si cracking. At the same time, large strain in the adjacent Si causes carrier mobility changes which in turn result in spatial variation of transistor performance. In order to minimize the variability, a keep-out-zone (KOZ) must be introduced causing wastage of premium Si real estate.

The challenges described above can be overcome if one is able to handle ultra-thin (<1 μm) Si layers reliably and this process is scalable to large wafer

size. Silicon-on-insulator (SOI) offers the potential to achieve ultra-thin silicon layers that is not possible in bulk silicon. This ability to achieve ultra-thin silicon layers is based on the possibility of selectively removing the substrate and etch-stop on the buried oxide (BOX) layer. Three-dimensional ICs based on SOI wafer are often accomplished with low temperature bonding. With an ultra-thin silicon layer, it is possible to do away with high aspect TSV. Instead, interlayer vias with much lower aspect ratio can be used and the formation method is largely similar to the via formation in the back-end Cu interconnect processes. This technology has been pioneered by researchers at MIT, IBM, and a few others in the past for a range of application areas such as image sensing, high performance computing, etc. A summary of the technical merits of 3D IC realized in the SOI platform are compared with those in the bulk Si platform in Table 12.2.

Given the outstanding technical merits afforded by SOI wafer for 3D IC implementation, this chapter serves to discuss and provide references for this promising technology. In the subsequent sections, discussion is focused on material and process requirements, generic and customized process flows, and specific examples reported in the literature. Since the key supporting technology for SOI-based 3D IC is wafer bonding, one section covers discussion on advanced wafer bonding in direct Cu–Cu and dielectric–dielectric bonding.

Table 12.2 Comparison between bulk Si-based and SOI-based 3D IC

	(a)	(b)	(c)
Bonding medium	Cu–Cu	Cu–Cu	Fusion or adhesive
Distance between device layers	Largest	Middle	Smallest
Handle wafer needed	Yes	No	Yes
Alignment required	More relaxed	Few μm	Aggressive (sub- μm)
Minimum via pitch	20–50 μm	~10 μm	Very tight (~0.4 μm)
Interlayer via density	Lower	High (~ $10^6/\text{cm}^2$)	Very high (~ $10^8/\text{cm}^2$)
Suitability for SOI vs bulk wafers	Either	Either	SOI
Chip vs wafer bonding	Either	Either	Wafer/wafer only
Directly extendable to >2 layers	Yes	No	Yes
Connection to package	Standard	Deep via	Standard

Source: IBM.

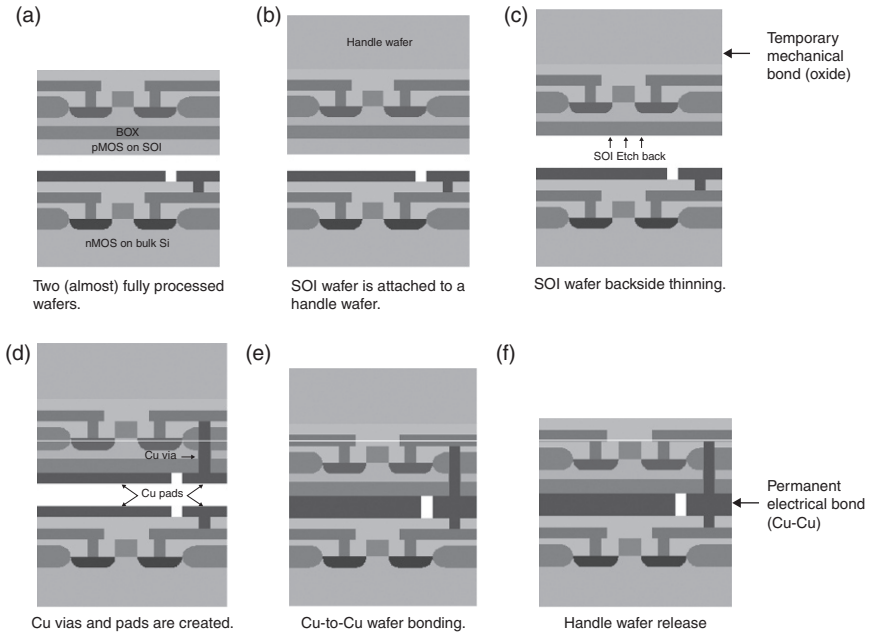
12.2 3D integration using Cu–Cu bonding: generic flow techniques

In a nutshell, a SOI-based 3D IC consists of a series of parallel device fabrication, alignment, bonding, thinning, vertical via formation and top metallization. One has a choice of face-to-face (face down) or back-to-face (face up) stacking orientations. In the case of back-to-face stacking, there is a need for a handle wafer which temporarily holds the donor wafer during thinning and is released upon successfully layer transfer. Depending on the final application and cost consideration, bulk Si wafer can be used as the substrate/base wafer as needed. The remains of the wafers must be SOI wafer. As highlighted in the above section, wafer bonding, particularly low temperature wafer bonding (below 400°C), is desired since the mating wafers have completed the front-end-of-line processes and in certain cases partial back-end-of-line processes. The SOI-based 3D IC flows are classified based on the bonding medium, that is, Cu–Cu bonding or dielectric bonding in the following discussion. This section presents several generic and specific process flows that are enabled by Cu–Cu bonding. Sections 12.5 to 12.7 present process flows that are enabled by dielectric bonding. Methods and requirements for advanced wafer bonding are studied in detail in Sections 12.8 to 12.9.

This section describes a 3D integration process based on work on Cu thermo-compression bonding originally proposed by researchers at MIT. In this scheme, two front-end-of-line (FEOL) active device wafers are stacked in a back-to-face fashion and bonded by means of low temperature Cu-to-Cu thermo compression. Interlayer vias electrically interconnect the device layers. Low temperature wafer bonding is necessary since the pre-bonding device layers already have Al or Cu metal interconnect lines. This is an attractive scheme because it allows lower aspect ratio interlayer vertical via and thinner bonding layer. Process sequence in this proposed 3D integration scheme is illustrated in Fig. 12.2a–12.2f.

12.2.1 Handle wafer attachment

Figure 12.2a–12.2f depicts the process sequence to fabricate a 3D CMOS inverter. The bottom device layer is an n-MOS device fabricated on bulk Si while the top device layer is a p-MOS device fabricated on SOI wafer independently prior to stacking. To start with, the front side of the top layer is attached to a handle wafer as shown in Fig. 12.2b to provide mechanical support for ease of wafer handling. Therefore, the bonding has to be strong enough to hold the SOI wafer during subsequent processes. Note that this bonding is a temporary one, as the handle wafer will be released from the final 3D stack. This dictates the ease of handle wafer release at the end. Low temperature oxide wafer bonding² is used in this proposal. Note that there



12.2 (a-f) Process flow for 3D integration scheme using Cu wafer bonding.

have recent advances in temporary bonding and additional discussion can be found in Reference 3.

12.2.2 SOI thin-back

In Fig. 12.2c, the SOI substrate is thinned back after bonding to a handle wafer. A combination of mechanical grinding, plasma dry etch, and chemical wet etch can be used for this thinning step. In order to achieve good etch stop behavior, it is typical to etch the final 50–100 μm of Si using wet chemical etch. The buried oxide (BOX) serves as the etch stop layer as there is an excellent selectivity between Si and oxide in wet etchant. The handle wafer has to be protected against chemical attack by SiO_2 coating.

12.2.3 Backside vias and bonding pad formation

Backside interlayer vertical vias and Cu pads are created on the thinned SOI wafer. Note that in this 3D integration scheme, the requirement for via aspect ratio is relaxed as vias are formed on both wafers and connected. There are two sets of Cu pads. The first set comprises the via landing pads to form electrical connection between both device layers and the second set

comprises the dummy pads to increase the bonding area hence increase the bonding strength. This is schematically shown in Fig. 12.2d.

12.2.4 Cu thermo-compression bonding

Figure 12.2e shows that the top device layer is aligned to the bottom device layer, presumably with Cu pads already created on it, and bonded at low temperature with a constant down force in an inert ambient environment. A final post-bonding annealing step allows interdiffusion at the Cu–Cu interface and promotes grain growth.

12.2.5 Handle wafer release

The top donor wafer is bonded to the silicon handle wafer using oxide fusion bonding. Handle wafer can be removed from the final 3D stack by a combination of mechanical grinding and wet etch. Alternatively, a less abusive method such as hydrogen-induced wafer splitting can be used. Hydrogen is implanted into the handle wafer prior to bonding. The handle wafer can be released by annealing at a temperature higher than the temperature used during Cu thermo-compression bonding to form the permanent bond.

Using metal as the bonding interface between active layers is an attractive choice because metal is a good heat conductor and this will help circumvent the heat dissipation problem encountered in 3D ICs. At the same time, a metal interface allows additional wiring and routing. Cu is a metal of choice because it is a mainstream CMOS material and it has good electrical ($\rho_{\text{Cu}} = 1.7 \text{ m}\Omega\cdot\text{cm}$ vs $\rho_{\text{Al}} = 2.65 \text{ m}\Omega\cdot\text{cm}$) and thermal ($K_{\text{Cu}} = 400 \text{ W}\cdot\text{m}^{-1}\text{K}^{-1}$ vs $K_{\text{Al}} = 235 \text{ W}\cdot\text{m}^{-1}\text{K}^{-1}$) conductivities and longer electro-migration lifetime. Another advantage offered by metal bonding interface is that the metal layer can act as a ground shield if properly grounded hence better noise isolation between device layers on the stack. Note that we have used a back-to-face bonding fashion in which the SOI wafer is thinned and bonded to the substrate wafer, hence eliminating the potential damage from the SOI thinning step to the whole 3D stack.

12.3 3D integration using Cu–Cu bonding: face-to-face silicon layer stacking

In this section, silicon layer stacking (blanket and non-functional) in a face-to-face fashion is demonstrated. Stacking is accomplished by means of direct Cu-to-Cu thermo-compression bonding and silicon substrate thinning. The advantages of this orientation include the absence of an extra handle wafer leading to a much simpler and straightforward process. A silicon bilayer

stack is successfully fabricated and a progression to a quadruple-layer stack is shown. This opens up opportunities for vertical integration of ultra-thin silicon device layers.

12.3.1 Face-to-face silicon bilayer stack

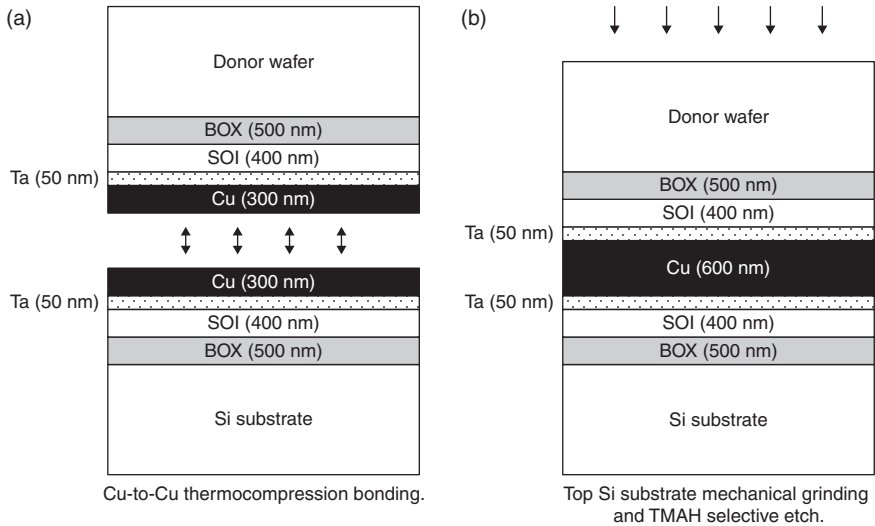
One approach to stacking thin silicon device layers is by wafer bonding and etch-back. Thin layers can be arranged either in a face-to-face or back-to-face fashion. In this section, a face-to-face silicon layer stack that is enabled by low temperature copper thermo-compression bonding is described. This stacking method is the most direct way to stack thin layers. In this face-to-face stacking method, a SOI donor wafer is bonded to a substrate wafer in a face-to-face manner using Cu as the bonding medium and etched back to the BOX layer. A silicon bilayer stack, with SOI layers that are as thin as 400 nm, is demonstrated.

Wafer preparation

The process flow to fabricate a silicon bilayer stack in a face-to-face arrangement is shown in Fig. 12.3. The experiment was performed on blanket silicon wafers. All wafers used in this experiment were n-type 150 mm Si(100) wafers. SOI wafers are an attractive choice because the BOX layer serves as an excellent etch stop layer during substrate thinning in silicon etchants such as tetraethyl-ammonium hydroxide (TMAH) as previously shown in earlier chapters. Since manufacturing grade SOI wafers are prohibitively expensive, SOI dummy wafers were prepared and used as both donor and substrate wafers in our experiment. SOI dummy structures were prepared by growing 5000 Å of thermal oxide as buried oxide on silicon wafers followed by the deposition of 4000 Å of undoped poly-silicon at 620°C. Since the donor wafers already have devices and interconnect fabricated on them in actual process, process temperatures in all subsequent steps were kept at 400°C or below to be compatible with back-end-of-line (BEOL) processes.

Cu-to-Cu bonding

All donor and substrate wafers were cleaned in piranha ($\text{H}_2\text{O}_2:\text{H}_2\text{SO}_4 = 1:3$, by volume) followed by metals deposition. In an e-beam system, 50 nm Ta and 300 nm Cu were deposited on both the donor and the substrate wafers, respectively. Ta was used as a diffusion barrier to prevent Cu diffusion into the device layer which might degrade the electrical integrity of the device layer in actual process. The donor wafer was then aligned to the substrate wafer in an EV Group aligner and the pair was clamped on a bonding chuck.



12.3 (a, b) Face-to-face silicon layer transfer and stacking based on Cu thermo-compression and wafer etch-back.

Wafers were separated by three metal flaps each about $30\ \mu\text{m}$ thick at the edge. Aligned wafers were transferred to an EV Group bonding chamber. After three cycles of N_2 purge and pump-down, the metal flaps were pulled out and thermo-compression bonding was performed at 400°C under a contact force of $4\ \text{kN}$ for 1 h in vacuum. This is schematically shown in Fig. 12.3a. The bonded pair was then annealed in atmospheric N_2 at 400°C for 1 h to allow Cu inter-diffusion and grain growth in order to achieve higher bonding strength.

The next step in the flow is donor wafer thin-back as schematically shown in Fig. 12.3b. Two methods will be described.

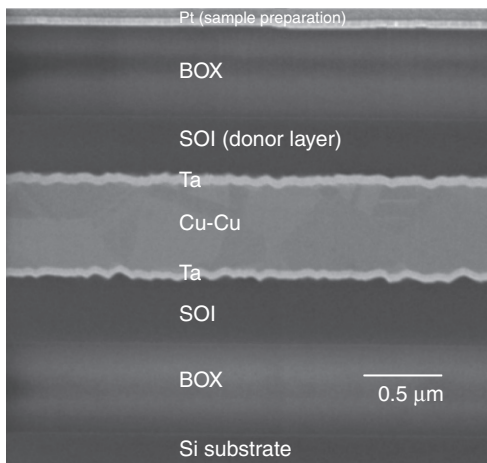
SOI donor wafer etch-back: grinding and TMAH

The substrate of the bonded donor wafer can be thinned back using a combination of mechanical grinding and TMAH strip. This is a destructive method since the substrate of the donor wafer will be completely ground and etched away. Mechanical grinding was outsourced to a vendor. This is a two-step grinding process. There is a coarse grind where most of the removal is done. This is followed by a fine grind that removes the last $15\text{--}20\ \mu\text{m}$ and removes any damage. When the grinding is finished, using a 2000 grit type grind wheel, the finished wafer surface exhibits a roughness of $0.13\ \mu\text{m}$. In addition, DI water is used for process cooling and cleaning; no chemicals or slurries are used during grinding. Process parameters including force and speed are proprietary information of the vendor that cannot be disclosed.

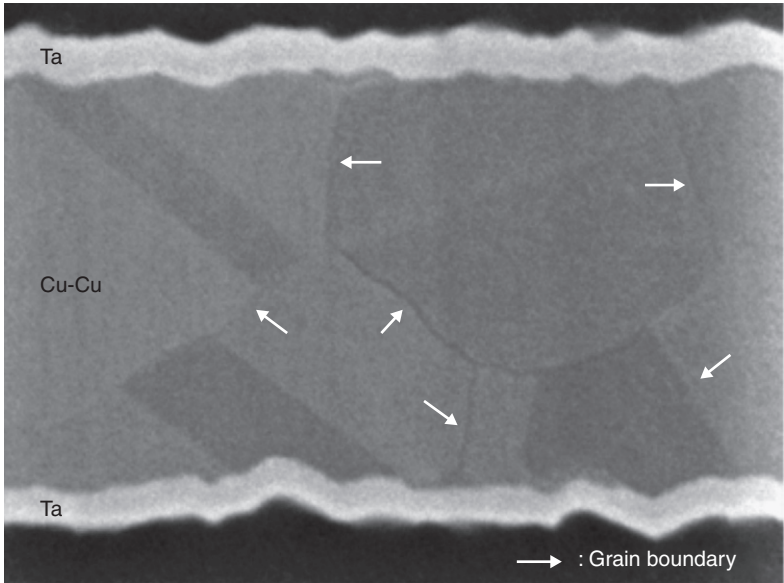
Since mechanical grinding has no selectivity between silicon and oxide, the grind-back was stopped at about 75 μm away from the BOX layer. This remaining 75 μm thickness of silicon layer was stripped easily using 12.5 wt % TMAH solution at 85°C for about 100 min. Since TMAH has excellent (more than three orders of magnitude) selectivity towards oxide, the etching stopped at the BOX layer.

Figure 12.4 is a cross-sectional scanning electron microscope (SEM) image showing the final silicon bilayer stack after donor wafer substrate removal. Note that all thin film layers are held together reliably by the bonded Cu layer. This SEM micrograph therefore confirms the layer stacking method described above. The resulting wiggling interface between the poly-Si layers and the Ta layers was caused by the surface roughness of the unpolished poly-Si layers. Figure 12.5 shows the close-up view of grain microstructures in the bonded Cu layer. Substantial inter-diffusion and grain growth in the bonded Cu layer can be observed in the close-up SEM image as evidenced by Cu grains that extend beyond the original bonding interface. The original Cu layers have merged and a homogeneous bonded Cu layer is obtained. Grain boundaries of the Cu grains are marked with arrows.

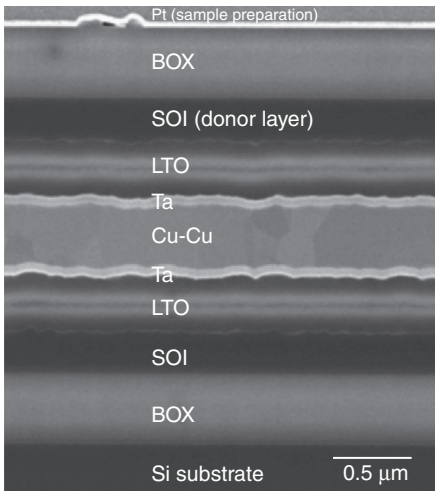
In actual process, devices in the SOI layer are interconnected by metal wires and interconnects are embedded in the interlayer dielectric (ILD). To make the above stacking process as close to the real process as possible, the donor and the substrate wafers were coated with 0.5 μm of low temperature oxide (LTO) from a silane source at 400°C. LTO is an attractive choice for ILDs and for the passivation layer because of its high deposition rate and low process temperature. We repeated the stacking process described in



12.4 SEM shows a silicon bilayer stack obtained after donor wafer thin-back.



12.5 Cu grain structures in the bonded layer. Note that the original Cu layers have merged and a homogeneous layer is obtained.



12.6 SEM image shows a silicon bilayer stack with the insertion of low temperature oxide (LTO) between the SOI and the Cu layers.

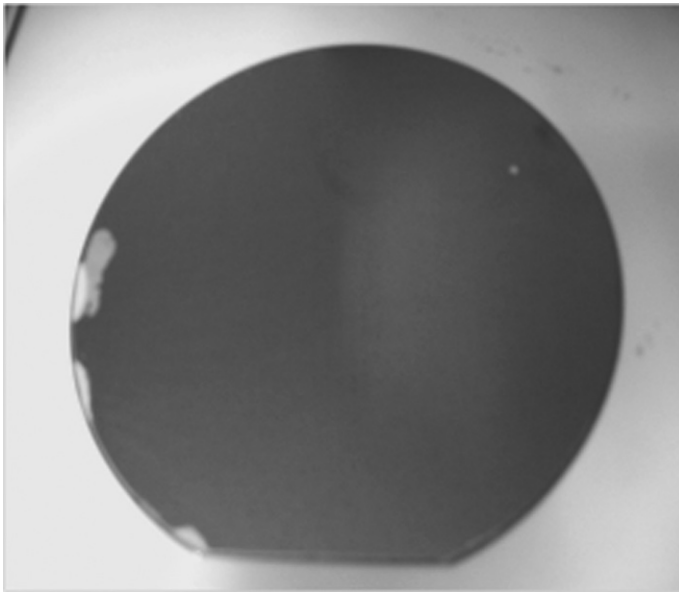
Fig. 12.3. Figure 12.6 is the SEM image of the silicon bilayer stack with the insertion of LTO layers between the SOI and Cu layers. All layers are held together with good integrity by the bonded Cu layer. In the above process, SOI dummy structures are used as both donor and substrate wafers. Note

that the substrate wafer can be either SOI wafer or bulk Si wafer for this layer stacking experiment. The selection of substrate wafer is depending on specific application needs.

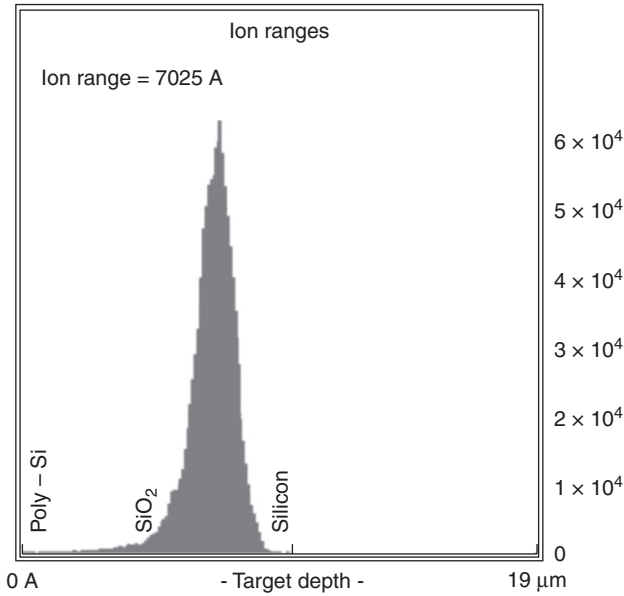
In wafer level silicon layer stacking, bonding uniformity across the wafer is essential to obtain a high yield of the final transferred films. It is therefore important to evaluate the uniformity of the transferred thin films on the substrate wafer. Shown in Fig. 12.7 is an image of transferred thin films on the substrate wafer after donor wafer etch-back. Except at the wafer edge, complete thin film transfer is obtained across the whole wafer. Thin films delaminate at the wafer edge due to wafer thickness non-uniformity and possibly the presence of particles due to wafer handling. Note that blanket Cu–Cu bonding is used in this demonstration and this has no practical application as Cu is a conductive medium. In actual application, patterned Cu structures are bonded to allow electrical isolation. These requirements, as well as methods of formation, are re-visited in Section 12.8.

SOI donor wafer etch-back: hydrogen-induced wafer splitting

To minimize potential process damage to the bonded Cu layer arising from mechanical grinding, hydrogen-induced wafer splitting⁴ can be used to release the substrate of the donor wafer. H_2^+ ions at a dose of $5 \times 10^{16} \text{ cm}^{-2}$ were implanted at an energy of 150 keV into the donor wafer prior to



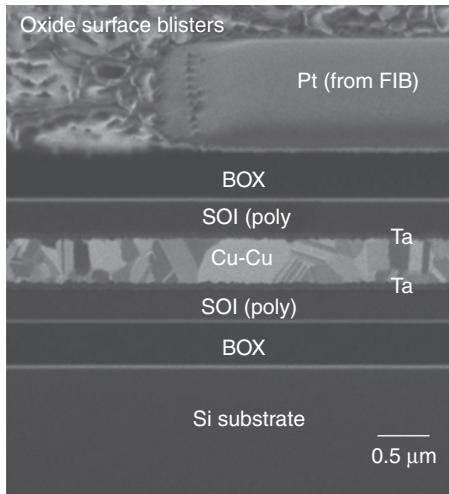
12.7 Image of transferred thin films on the substrate wafer after donor wafer etch-back. Delamination is observed at the edge of the wafer.



12.8 Simulated hydrogen profile using TRIM program.

wafer bonding. To estimate the penetration depth of the hydrogen ions, the Transport of Ions in Matter (TRIM) program was used.⁵ Since TRIM does not allow molecular ions as the doping species, hydrogen ions (H^+) were used at an energy of 150 keV. A total of 10 000 ions were simulated. The simulated hydrogen profile is shown in Fig. 12.8. A penetration depth of 7025 Å is estimated.

Upon heating at the appropriate temperature after Cu thermo-compression bonding of donor wafer to substrate wafer, lateral microcracking induced by hydrogen will release the substrate of the donor wafer at the peak of hydrogen implant. Since this process is temperature dependent, all heat treatment prior to layer splitting was kept at 300°C or below. Therefore, Cu wafer bonding was done at 300°C instead of 400°C to prevent premature wafer de-bonding. All other bonding parameters were unchanged. After the donor wafer was bonded to the substrate wafer, a final annealing step was performed at 400°C for 1 h to initiate wafer splitting and to further enhance Cu layer bonding strength. Figure 12.9 is the focus ion beam (FIB) image of the silicon bilayer stack after wafer separation. Note that the oxide surface contains surface blisters as a result of microcracks created by hydrogen ion cutting. The two wafers separated close to the interface of the BOX layer and silicon substrate of the donor wafer. A homogeneous Cu layer with grains that extend from one end to the other can be observed in the bonded Cu layer. This suggests that



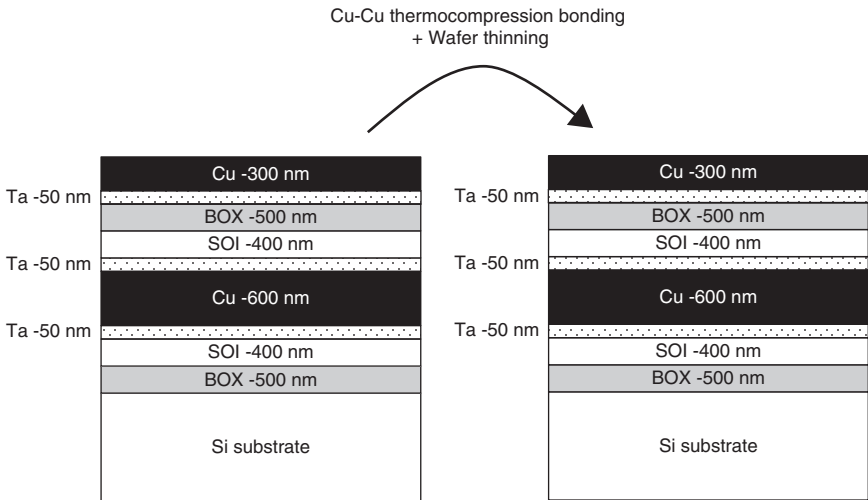
12.9 FIB image shows a silicon bilayer stack. The substrate of top donor wafer was separated using hydrogen induced wafer splitting.

significant grain growth has taken place even though the thermal budget was reduced to provide a temperature window for Cu wafer bonding and hydrogen induced layer splitting.

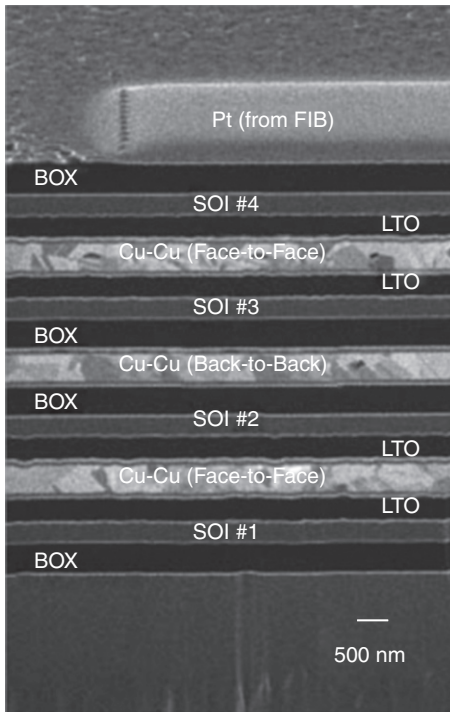
12.3.2 Silicon multilayer stack

Process flow

In applications such as system-on-a-chip (SoC) or high density memory where a higher level of integration and device density is required, a silicon multilayer stack is of great promise. It is possible to expand the silicon layer stacking developed above beyond a bilayer stack. In this section, we demonstrate a quadruple-layer stack by stacking two bilayer stacks as obtained in Fig. 12.3. Except for the starting wafers, all process steps remained the same. In an e-beam system, 50 nm Ta and 300 nm Cu were deposited on two bilayer stacks as shown in Fig. 12.10. The two wafers containing silicon bilayer stack were aligned and transferred to the bonding chamber. Thermo-compression bonding was done at 400°C under the contact force of 4 kN for 1 h in vacuum. The bonded pair was then annealed in atmospheric N₂ at 400°C for 1 h to allow inter-diffusion and grain growth in the Cu layer for higher bonding strength. The top silicon substrate was subsequently thinned back using a combination of mechanical grinding and TMAH strip as before.



12.10 Schematic showing a possible way to fabricate a silicon quadruple-layer stack by stacking two silicon bilayer stacks.



12.11 FIB image clearly shows a silicon quadruple-layer stack achieved by stacking two silicon bilayer stacks. This paves a promising path to multilayer and multifunctionality silicon stacks.

Demonstration of quadruple-layer stack

Figure 12.11 is a FIB image of a silicon quadruple-layer stack obtained by stacking two bilayer stacks together. It clearly shows that all layers are bonded and stacked accordingly. All three bonded Cu layers show stable grain structure after substantial Cu inter-diffusion and grain growth as evidenced from Cu grains that extend from one end to the other in the homogeneous layers. The same steps can be repeated to build a silicon multilayer stack.

12.4 3D integration using Cu–Cu bonding: back-to-face silicon layer stacking

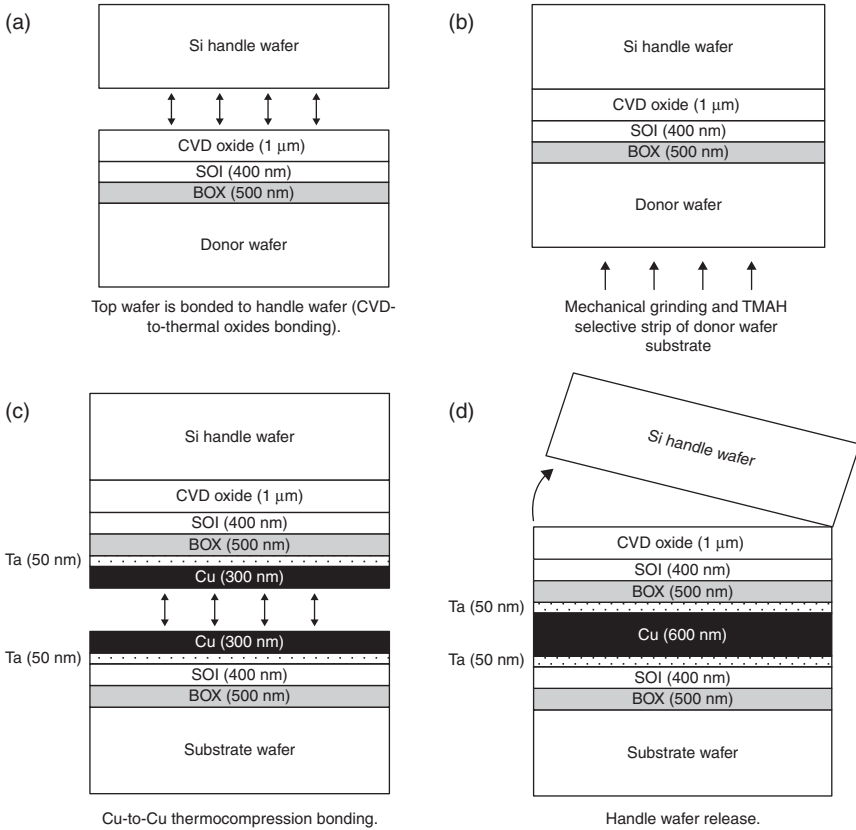
Besides face-to-face stacking, some research groups are working on face-to-back stacking. This stacking method is described in this section.

12.4.1 Back-to-face stacking

Silicon layers can also be stacked in a back-to-face fashion. In back-to-face silicon layer stacking, a donor wafer is bonded to a temporary handle wafer for mechanical support and etched back to the required thickness. Stacking is completed by bonding the thinned silicon device layer (that is attached to the handle wafer) to a substrate wafer in a back-to-face manner and followed by handle wafer release. In this chapter, we describe a back-to-face silicon layer stacking method using a combination of low temperature oxide wafer bonding (as a temporary bond between the donor wafer and the handle wafer) and Cu wafer bonding (as a permanent bond between the thinned silicon layer and the substrate wafer). The process flow is summarized in Fig. 12.12.

12.4.2 Wafer preparation

The experiment was performed on blanket silicon wafers. All wafers used in this experiment were n-type 150 mm Si-(100) wafers. Two sets of wafers were prepared: one group was the handle wafers and the other was the SOI dummy wafers (as donor and substrate wafers). The handle wafers were covered with 5000 Å of thermal oxide for protection against chemical attack during donor wafer etch-back. Wet silicon etchants such as TMAH, known to have excellent selectivity towards thermal oxide, were used. SOI dummy structures were prepared by growing 5000 Å of thermal oxide as buried oxide on silicon wafers followed by the deposition of 4000 Å of undoped poly-silicon at 620°C. Since the donor and substrate wafers already have devices and interconnects fabricated on them in actual process, all subsequent process temperatures were limited to 400°C and below. The donor



12.12 (a–d) Schematics of back-to-face silicon layer transfer and stacking for three-dimensional integration.

wafers were coated with 1 μm of tetraethyl-orthosilicate (TEOS) source plasma-enhanced chemical vapor deposition (PECVD) oxide at 350°C. This so-called PE-TEOS oxide is an attractive choice for interlayer dielectrics and the passivation layer because of its high deposition rate and low process temperature.

12.4.3 Oxide wafer bonding

To begin the silicon layer transfer and stacking process, the donor wafers were bonded to the handle wafers for mechanical support and ease of wafer handling. While epoxy⁶ or adhesive material⁷ can be used for this type of bonding, we have avoided process complexity as a result of the use of new materials and resorted to direct oxide to oxide wafer bonding which is more CMOS friendly. While the protective thermal oxide on the

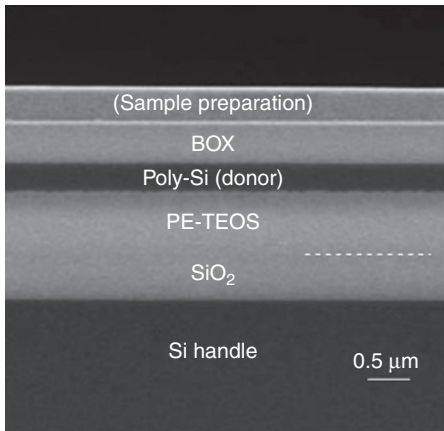
handle wafers possesses suitable properties for wafer bonding, PE-TEOS oxide on the SOI dummy wafers prepared at low temperature requires additional surface preparations before wafer bonding can be initiated. PE-TEOS oxide on SOI dummy wafers were densified in atmospheric N_2 at $350^\circ C$ for 5 h to drive away all trapped gas molecules. This step allowed degassing from the porous SiO_2 , which was detrimental to the bonding, to take place prior to bonding. Surface smoothness is a very critical factor that determines successful wafer bonding. It is well known that PE-TEOS oxide has a very rough surface. To reduce the roughness, the surfaces were chemical- mechanically polished (CMP) for 3 min after densification. The surface roughness improved from 8.53 to 0.48 nm. All handle wafers and donor wafers were activated by oxygen plasma followed by a 10 min piranha ($H_2O_2:H_2SO_4 = 1:3$) clean. This cleaning was necessary to terminate the wafer surfaces with hydroxyl (OH) groups to initiate hydrogen bonds during wafer bonding. Activated handle wafers were aligned to donor wafers in an EV Group aligner and the pairs were bonded as schematically shown in Fig. 12.12a. Bonding was performed at room temperature under a contact force of 1 kN for 2 min. After bonding, the bonded wafer pairs were annealed at $300^\circ C$ in atmospheric N_2 for 3 h to enhance the bonding strength. The bonding strength is estimated to be about 1400 mJ/m^2 using the Maszara crack opening method.

12.4.4 Donor wafer etch-back

The next step in the flow was donor wafer thin-back as described in Fig. 12.12b. The substrate of the bonded donor wafer can be thinned back using a combination of mechanical grinding and TMAH strip. Since mechanical grinding has no selectivity between silicon and oxide, the grind back was stopped at about $75 \mu\text{m}$ away from the BOX layer. The remaining $75 \mu\text{m}$ thick of silicon layer can be stripped easily using 12.5 wt % TMAH at $85^\circ C$ for about 100 min. Since TMAH has excellent selectivity towards oxide, the silicon etching stops at the BOX layer. Therefore SOI wafers are an attractive choice in this type of silicon layer stacking as the BOX layer serves as an excellent etch-stop layer. Figure 12.13 shows an SEM image of thin films attached to the handle wafer after etch-back.

12.4.5 Cu wafer bonding

The thinned silicon layer on the handle wafer was then bonded to a substrate wafer using Cu as the bonding medium as shown in Fig. 12.12c. Fifty nanometers of Ta and 300 nm of Cu were deposited on the thinned layer and the substrate wafer in an e-beam system. Ta acted as diffusion barrier.



12.13 SEM image of thin films attached to the handle wafer after etch-back.

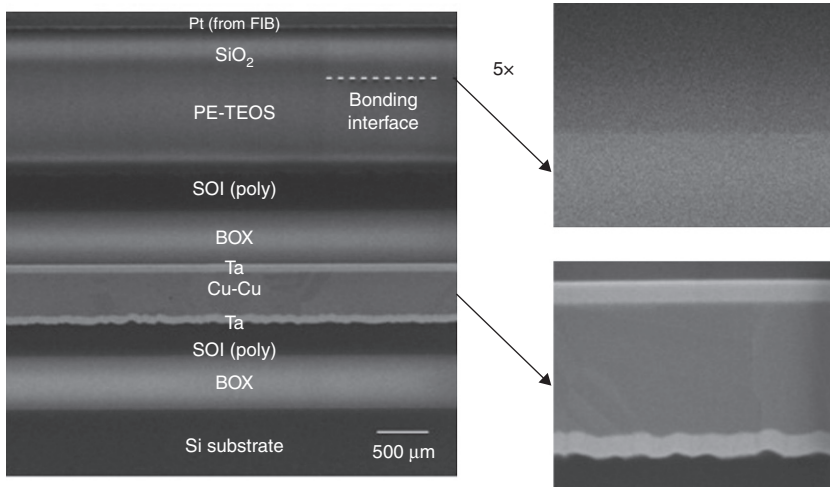
Thermo-compression bonding was carried out at 400°C under a contact force of 4 kN for 1 h in vacuum. The bonded pair was then annealed in atmospheric N₂ at 400°C for 1 h to promote Cu inter-diffusion and grain growth for higher bonding strength.

12.4.6 Handle wafer release

Figure 12.14d shows the final step in the flow, that is, the handle wafer release. This can be done in the following two ways:

Grinding and TMAH

The most direct way to remove the handle wafer is by mechanical grinding and TMAH strip. The handle wafer was ground to about 75 μm from the bonding interface. The remaining 75 μm of silicon layer was stripped in 12.5 wt % TMAH solution that stopped at the protective oxide layer. Figure 12.14 is a cross-sectional SEM image showing all of the final layers on the stack. The close-up views of the bonding interfaces are also shown. This SEM image confirms the layer stacking described above. The resulting undulating interface between the bottom poly-Si and the Ta layer was caused by the surface roughness of the unpolished poly-Si layer. No interfacial void is observed at the bonding interface between the PE-TEOS and thermal oxides. Substantial inter-diffusion and grain growth in the Cu can be observed in the close-up SEM image at the bottom right. Note that the original Cu-bonding interface has disappeared and a homogeneously bonded Cu layer is obtained.



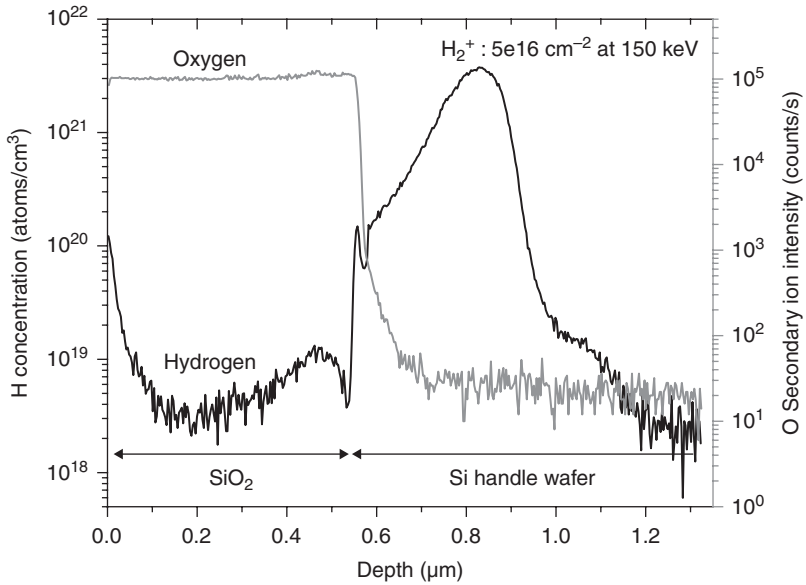
12.14 SEM shows back-to-face silicon layers stack obtained after handle wafer grinding and TMAH strip.

Hydrogen-induced wafer splitting

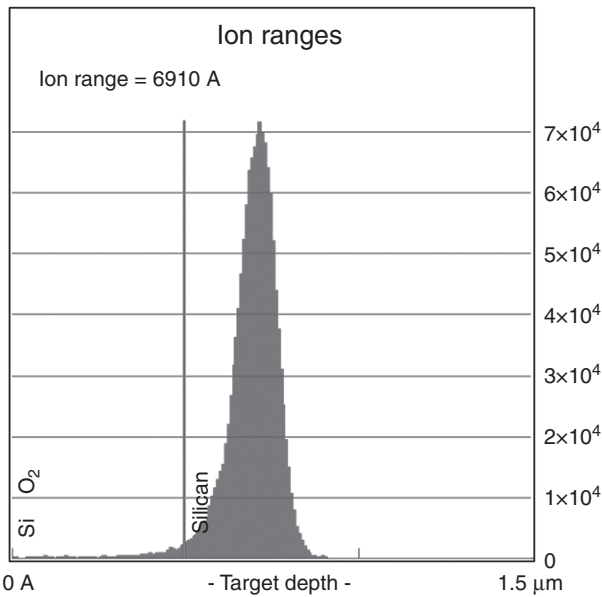
To minimize process damage to the Cu bonding interface as a result of mechanical grinding, hydrogen-induced wafer splitting can be used to release the handle wafer. H_2^+ ions at a dose of $5 \times 10^{16} \text{ cm}^{-2}$ were implanted at an energy of 150 keV into the handle wafer prior to wafer bonding. Upon heating at the appropriate temperature, lateral microcracks induced by hydrogen will release the handle wafer at the location around the peak of hydrogen implant profile. Figure 12.15 is the SIMS profile of the implanted hydrogen with a peak at about 300 nm into the silicon handle wafer from the oxide–silicon interface. The hydrogen profile simulated using the TRIM program is also shown in Fig. 12.16.

To ensure successful bonding, it is important to ensure that hydrogen implant does not increase the surface roughness of the oxide handle wafer excessively. The surface roughness of the oxide handle wafer is estimated with atomic force microscopy (AFM) to be 0.273 nm. This value increases to 0.344 nm upon hydrogen implantation. Note that this value is below the roughness requirement of <1.0 nm and hence CMP is not required for successful wafer bonding for oxide handle wafers that have gone through hydrogen implant.

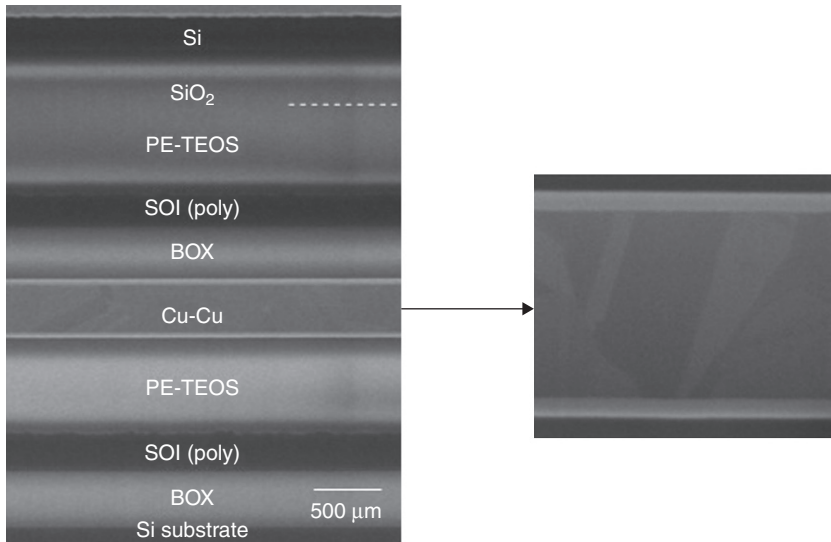
Since this process is temperature sensitive, all heat treatments prior to layer splitting were kept at 300°C or below. Therefore, Cu–wafer bonding was done at 300°C for 1 h to prevent premature wafer de-bonding. Hydrogen-induced wafer splitting was achieved with an anneal at 400°C for 1 h. This step also enhanced the Cu layer bonding strength. Figure 12.17 is



12.15 SIMS profile of implanted hydrogen into the handle wafer. The hydrogen peak is situated at about 300 nm from the oxide-silicon interface into the silicon handle wafer.



12.16 The hydrogen profile simulated using TRIM.

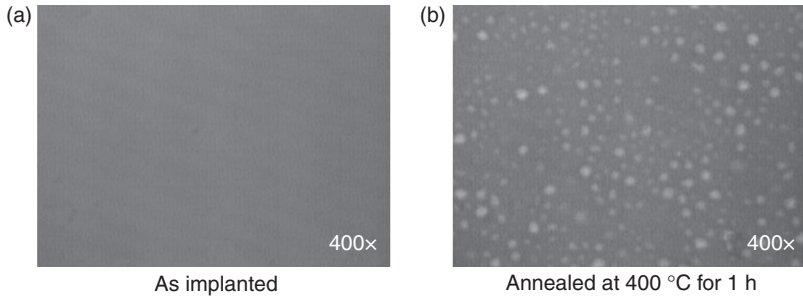


12.17 SEM shows the silicon layers stack obtained after handle wafer release. Handle wafer released at the peak of the implanted hydrogen profile.

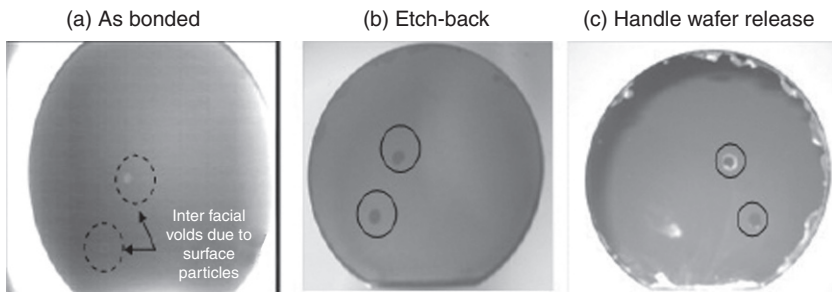
an SEM image of the stack after the handle wafer separation. We have used substrate wafer with 1 μm of PE-TEOS oxide on top. The remaining 300 nm of Si left over by handle wafer on the top of the stack can be stripped using a short TMAH dip. The close-up view shows a homogeneous Cu layer with grains that extend from one end to the other end suggesting that significant grain growth has taken place even though the thermal budget was reduced to provide a temperature window for Cu wafer bonding and hydrogen induced layer splitting.

Figure 12.18 shows optical microscope images of hydrogen implanted wafer before and after anneal at 400°C for 1 h. Note that surface blisters form on oxide wafers after anneal. These blisters originate from microcracks caused by gathering of hydrogen molecules and the force pushes upward to the free surface to force a blister. In the case of a well-bonded wafer pair, the force will cause lateral propagation of the cracks and release the wafer close to the location of the implanted hydrogen peak.

Surface cleanliness is one of the essential requirements to obtain reliable wafer bonding. The presence of surface particles at the bonding interface of protective thermal oxide on the handle wafer and the PE-TEOS oxide on the SOI donor wafer can have detrimental consequences on the final thin film integrity and/or bonding interface. This is highlighted in Fig. 12.19. The infrared (IR) image in Fig. 12.19a reveals large voids at the bonding interface of an oxide wafer pair due to unwanted surface particles



12.18 Hydrogen-implanted handle wafer surface under optical microscope showing (a) as-implanted wafer and (b) wafer which had undergone 400°C anneal for 1 h.



12.19 Thin film delamination due to the presence of surface particles at the bonding interface: (a) IR image reveals large void at the oxide bonding interface due to surface particles; (b) photo of thin films on the handle wafer after etch-back; and (c) photo of final thin films stack after handle wafer release.

that are incorporated during wafer handling. These particles prevent bonding at areas surrounding the particles. As a result, thin films detach from the handle wafer in these areas as shown in Fig. 12.19b because there is no mechanical support to hold them to the handle wafer. The same delamination is also observed after the handle wafer is released from the thin film stack in Fig. 12.19c and this will degrade the final yield. Except at the wafer edge, thin films are transferred reliably onto the substrate wafer at locations where no interfacial voids were observed at the oxide bonding interface. Therefore, surface particle control during wafer bonding is an important aspect to achieve high yield in thin film transfer.

12.5 3D integration using oxide bonding: the MIT Lincoln Laboratory's 'face down' stacking technique

MIT Lincoln Laboratory has developed a wafer-scale three-dimensional (3D) integrated circuit technology whereby 3D chips are constructed by

transferring, bonding together, and electrically connecting the active sections of integrated circuits that were fabricated on silicon-on-insulator (SOI) substrates.⁸ This technology led to the first demonstration of a ‘true’ 3D circuit with the successful operation of a 3D 64×64 visible imager.⁹ At the same time, numerous institutions have also used a variety of layer-transfer techniques to develop 3D integration technologies.^{10–15}

12.5.1 3D fabrication process

3D circuits are fabricated on 150 mm SOI substrates using a 180 nm fully depleted SOI process that includes mesa isolation of transistors and three levels of metal interconnect. A new term, ‘tier’, was adopted to distinguish among design layers, physical layers, and transferred layers of a 3D IC and is the functional section of a wafer that consists of the active silicon, the interconnect, and, for an SOI wafer, the buried oxide. A tier is approximately 10 μm thick. The 3D assembly process and a 3D chip consisting of three tiers are illustrated in Reference 8. The process begins by transferring tier 2 to the base tier (tier 1) after face-to-face infrared alignment, oxide–oxide bonding at 275°C, and a wet etch of the handle silicon to expose the BOX of tier 2. The BOX is used as an etch stop for the silicon etch to produce a uniformly thin active layer and is an essential step in the 3D assembly technology. For this reason all circuits to be transferred must be fabricated with SOI substrates. The handle silicon of a transferred tier is removed by grinding the silicon to a thickness of about 70 μm followed by a silicon etch in a 10% TMAH solution at 90°C. Since the ratio of silicon to BOX etch rates in TMAH is 1000:1, the handle silicon is removed without attacking the BOX and without introducing a thickness variation in the transferred tier, a factor that is essential when forming the vertical connections between tiers, the 3D vias. In both etches the edge is protected to ensure that the wafer can be handled by cassette-to-cassette equipment and that the silicon removal process does not attack the oxide–oxide bond. Three-dimensional vias are designed to lie in the mesa-isolated regions of the tiers so that lining the vias with a deposited dielectric is not required to achieve insulation between the vertical connections.

The 3D vias are patterned and etched through the BOX and deposited oxides to expose metal contacts in both tiers. The 3D vias are then filled with tungsten that is planarized by CMP to electrically connect the two tiers. The metal contact in the upper tier is an annulus with a 1.5 μm opening that also functions as a self-aligned hard mask during the plasma etch of the oxide beneath it to reach the metal land in the lower tier. In order to fully land the 3D via, the size of the metal pad, and thus the pitch of the vertical interconnect, are proportional to twice the wafer–wafer misalignment.

A third tier (tier 3) can then be added to the tier 1–2 assembly using the same processes, except that the front side of tier 3 is bonded to the BOX of tier 2, and 3D vias connect the top-level metal of tier 3 to metal pads on the BOX of tier 2. The 3D chip is shown after bond pads are etched to expose the back of the first-level metal for probing and wire bonding. If the 3D chip is a digital circuit, the bond pads are etched through the BOX and deposited oxides of tier 3. If it is a back-side-illuminated imager, tier 1 is a bulk silicon detector wafer in which photodiodes were fabricated. An additional transfer to a carrier wafer is then required, and bond pads are etched after thinning the back side of the detector wafer to tune the silicon to the required optical absorption. The cross-sectional scanning electron micrograph of a three-tier ring oscillator shown in Reference 8 illustrates interconnections between tiers and the compactness possible with the 3D technology.

The unrestricted placement of 3D vias is an integral part of the 3D technology. A 3D via consists of a metal annulus in the upper tier, a metal land in the lower tier, and a tungsten plug that electrically connects the two features.⁸ The plug is formed in an oxide hole that is plasma etched with a resist mask that is aligned to the metal annulus with a mean and 3σ overlay error less than 100 and 300 nm, respectively. The annulus is a unique feature of the design since it forms the top electrical contact and masks the oxide etch to the metal land. After resist removal, tungsten is deposited and planarized by CMP leaving approximately 8 μm of tungsten in the hole. The present 3D via design consists of a 3 μm square landing pad, a 1.5 μm square annulus opening, and a 1.75 μm square resist window called the 3D cut. The design of these inter-tier connections significantly reduces the pitch of 3D vias to 6 μm from 26 μm used in the 3D imager first reported.⁹

12.5.2 3D circuit and device results

The ‘low-hanging fruit’ of 3D technology is focal plane design and fabrication because the imaging tier has a 100% fill factor, and the analog and digital processing tiers are below the imaging tier. Using Lincoln Laboratory’s 3D technology discussed above, the researchers were successful in the design, fabrication and operation of avalanche photodiode (APD) imagers and 3D visible imagers.

A two-tier 1024×1024 visible imager with 8 μm pixels was demonstrated.¹⁶ Tier 1 is a p^+n photodiode, and tier 2 is a fully depleted (FD)SOI tier operated at 3.3 V. This is the most dense 3D imager circuit developed using this 3D circuit technology and illustrates the realization of a 100% imager fill factor by 3D technology. Each pixel of the 1024×1024 array includes a reverse-biased p^+n diode (in tier 1), a reset transistor, a source follower transistor, and a select transistor (in tier 2).⁸ Measured responsivity from the PMOS reset imager with added in-pixel capacitance was

$\sim 2.7 \mu\text{V}/e^-$ and from the NMOS reset imager was $\sim 9.4 \mu\text{V}/e^-$, corresponding to a charge-handling capacity of 350 000 e^- and 85 000 e^- , respectively. Measured pixel operability is in excess of 99.9%; the principal yield detractor was column or row dropouts and was not due to defective 3D vias. The high degree of pixel functionality is seen in Reference 8, an image acquired by projecting a 35 mm slide onto the CMOS circuit side of the 3D integrated imager.

12.6 3D integration using oxide bonding: IBM's 'face up' stacking technique

Researchers at IBM have developed an SOI-based 3D integration method for ultra-high density and device-level stacking. It is a back-to-face (or face up) stacking approach. Detailed process flow and related descriptions can be found in Reference 15 and related references therein. There are several differentiations from the stacking approach described in Section 12.4. The bonding step is accomplished with blanket oxide-oxide bonding, hence eliminating the design and process issues facing Cu-Cu bonding. The device layers are vertically interconnected after bonding by the formation of inter-layer via and metallization. Another specific difference is the use of glass handle instead of Si wafer and it is a low cost handle. Since the glass handle is optically transparent, alignment between the two layers can be performed directly using live images without the need for alternatives such as IR or back-side alignments. The temporary bond between the top donor wafer and the glass handle is achieved with adhesive and released upon successful layer transfer using laser ablation since the glass handle is transparent. The technical challenges associated with this method are the thermal mismatch between glass and Si wafers, as well as handling of glass in a standard Si process line.

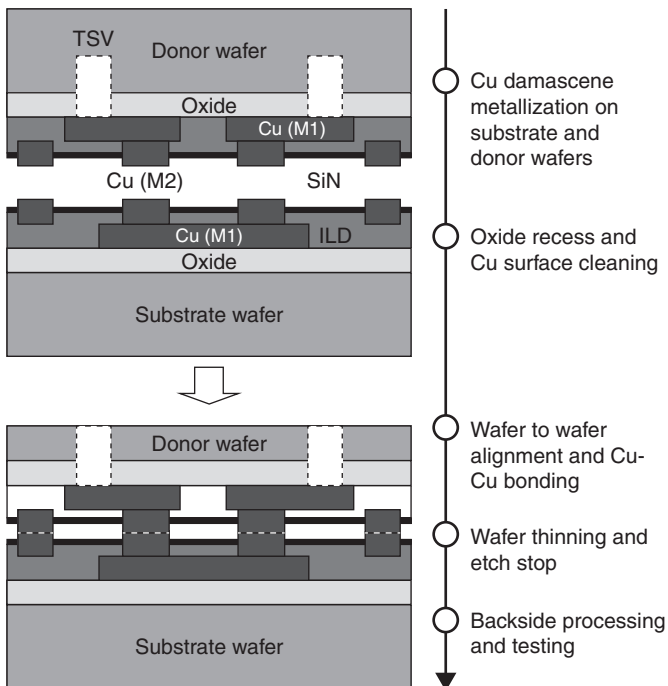
12.7 3D integration using oxide bonding: the sequential 3D process

In the SOI-based 3D IC processes discussed in the above sections, the starting wafers usually have already completed the front-end device fabrication and partial back-end metallization. This allows for independent and parallel device layer formation for performance optimization of each layer. There have also been reports on sequential 3D processes in which the donor wafers are not processed prior to layer transfer.¹⁷⁻¹⁹ Using this method, a high quality Si thin layer is transferred on a processed substrate wafer. The top layer is subsequently processed and electrically connected to the bottom layer. Due to the extremely flat and topology-free wafer surface, seamless oxide bonding can be accomplished without the need for surface polishing. In addition,

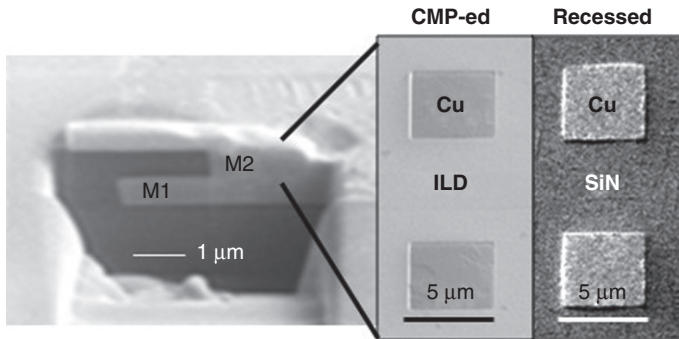
precision alignment between the wafers is not required during bonding. The down side of this approach is that the top layer needs to be processed at low temperature after bonding and transfer to avoid unwanted damage to the bottom device layer. This usually results in poorer quality devices in the top layer. Since the 3D stack is processed in a sequential manner, its throughput is expected to be lower.

12.8 Advanced bonding technology: Cu–Cu bonding

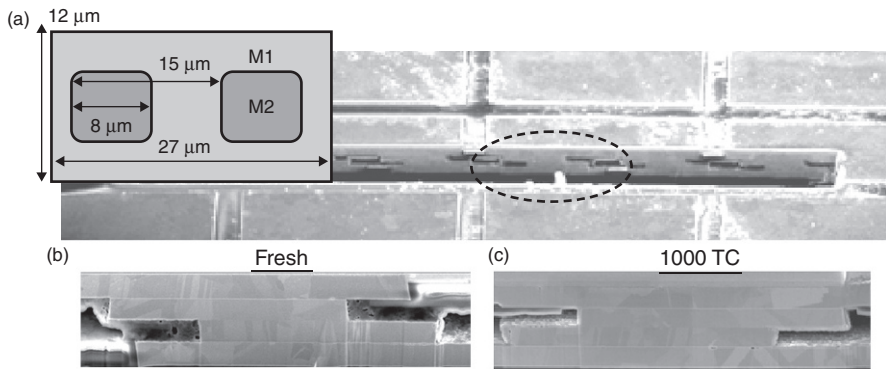
The process flow of 3D IC stacking using SOI wafers based on Cu–Cu bonding is discussed in detail in Section 12.2. In the Si layer stacking demonstrations, a continuous Cu bonding layer is used and this has no practical application since Cu is a conductive medium. In real applications, patterned Cu with isolation must be used. Besides electrical isolation, the bonded Cu structures must also be protected from environmental corrosion and be mechanically robust. There are detailed reports on Cu/dielectric hybrid bonding technology in References 20 and 21 and the references therein. Since the stacked layers are



12.20 Process flow of wafer-on-wafer stacking using bumpless Cu–Cu bonding with SAM passivation. Face-to-face bonding eliminates the need for handle wafer. (TSV is excluded from this work to simplify the fabrication process.)



12.21 Cross-sectional view of the Cu metal layers used for bonding. The plan views show the Cu surface after CMP and wet recess.



12.22 (a) The cross-sectional view of the daisy chain showing properly formed 3D connections. ILD is unintentionally removed due to extreme chemical wet etching. Each node consists of one Cu line (M1) and Cu–Cu contact (M2–M2). The contact pad (M2) is designed at $8\ \mu\text{m} \times 8\ \mu\text{m}$ and the pitch is at $15\ \mu\text{m}$ giving a density of $4.4 \times 10^5\ \text{cm}^{-2}$. Misalignment is $\sim 2\ \mu\text{m}$. (b) Freshly bonded contact node. (c) The contact node sustains thermal cycling (-40°C to 125°C) for 1000 cycles and it is intact with no defect.

usually ultra-thin, there is a very stringent requirement on the stand-off gap and co-planarity of the Cu structures. To meet the above requirement, bumpless Cu layers, such as those prepared in the back-end of line damascene processes, are preferred as opposed to Cu bumps, such as those prepared during redistribution layer (RDL) process. Ideally, a completely planar Cu/dielectric surface is needed for seamless bonding. However, CMP has always been a challenge due to the dishing effect.

In the author's research group, fine pitch Cu–Cu bonding at low temperature is extensively studied. Bumpless Cu–Cu structures are formed using the

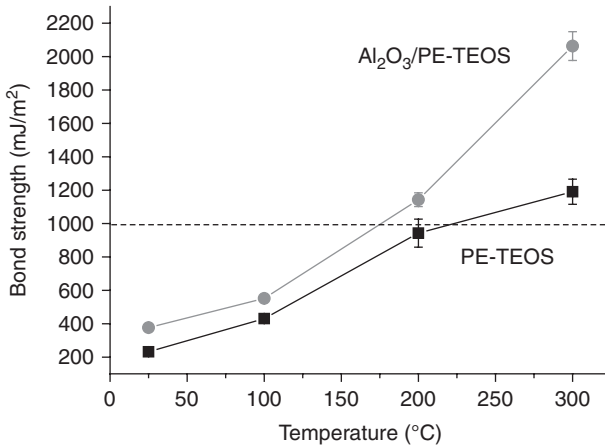
standard back-end processes and bonded to allow simultaneous formation of electrical and mechanical,^{22,23} as well as hermetic, bond^{24,25} as described in Fig. 12.20. The bumpless Cu layer needs to be recessed in order to expose the Cu layer prior to bonding as shown in Fig. 12.21. This will promote greater contact between the mating Cu layers and reduce the effect of CMP dishing. After bonding, the top wafer is removed to reveal the bonded Cu structure for testing as shown in Fig. 12.22 (as no TSV is used for ease of test structure fabrication). Note that in this demonstration, no SOI wafer is used. A similar process is applicable to SOI wafer when the CMP dishing can be precisely controlled such that the recess depth is kept as small as possible. For robust mechanical consideration, thicker SOI wafer may be required when Cu–Cu bonding is used. Experiments with bonding temperatures below 300°C has shown some success using a temporary passivation layer from self-assembled monolayer (SAM) of alkane-thiol.^{26–28}

12.9 Advanced bonding technology: dielectric bonding

As can be seen from the above discussion, oxide bonding plays an important and enabling role for SOI wafer 3D integration. There are very stringent requirements in terms of surface roughness and particle control in this technology. Surface activation, usually a combination of plasma exposure and wet cleaning, is applied to transform the oxide surface into a high energy surface for ease of bonding at low temperature. There have been substantial reports in this area.²⁹ This section discusses recent advances in oxide wafer bonding based on high- κ ^{30,31} and low- κ ^{32,33} dielectrics.

12.9.1 High- κ dielectric bonding

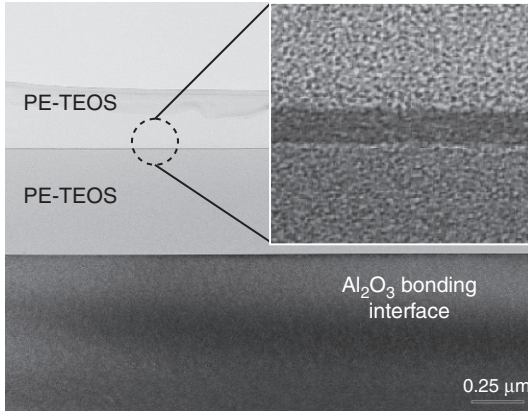
An approach based on capping the PE-TEOS oxide with a thin layer of high- κ dielectric prior to bonding is presented. A high- κ layer, such as Al_2O_3 , has been shown to be an efficient barrier material towards oxygen, water vapor, and aromas,³⁴ as well as copper.³⁵ This is useful for application in 3D integration because wafers are fabricated from various process technologies at various sites. Having a diffusion barrier at the bonding interface can control and prevent cross contamination between the disparate device layers on 3D IC. Surface activated bonding (SAB) has been previously performed on oxide (SiO_2) wafers capped with a thin Al_2O_3 intermediate bonding layer and higher bond strength compared to SiO_2 – SiO_2 bonding is observed.³⁶ In this method, energetic Argon ions are used to clean the surface and bonding is performed under high vacuum conditions. However, the need for high vacuum conditions has made this method less worthy for manufacturing. Our approach is based on conventional plasma surface activation and ambient bonding without the need for high vacuum.



12.23 The variation in bond strength of PE-TEOS and Al₂O₃/PE-TEOS samples at various annealing temperatures. Wafers bonded with Al₂O₃ thin layer consistently outperform wafers bonded with bare PE-TEOS oxide.

In Fig. 12.23, all bonded wafers exhibit bonding strength <400 mJ/m² after bonding at room temperature. During heat treatment, the bond strength of all bonded wafers improves with anneal temperature. Bond strength enhancement is insignificant for anneal temperatures below 100°C on all samples. As annealing temperature is increased to 200°C, bond strength improves rapidly with an Al₂O₃/PE-TEOS sample showing bond strength >1 J/m². Bond strength of PE-TEOS oxide shows signs of saturation beyond 200°C heat treatment. With a 300°C anneal, an Al₂O₃/PE-TEOS sample showed bond strength higher than that of PE-TEOS by as much as 73.3% (i.e., 2064 J/m² vs 1191 J/m²). This is an improvement over reported values using a thin Al₂O₃ intermediate bonding layer in which bond energy of ~ 2 J/m² is achieved with annealing at 400°C³⁶ and 1100°C.³⁷ As previously demonstrated, bond strength must be at least 1 J/m² or higher to sustain post-bonding processes such as mechanical grinding and TMAH etch. The enhancement in bond strength value with the insertion of an Al₂O₃ layer requires further study for complete understanding, but it is most likely related to the nature of the ionic bond in Al₂O₃ as compared with the covalent bond in SiO₂. One possible explanation can be drawn from the comparison of the bond dissociation energy of both types of bonds. Since the Si–O bond has lower bond dissociation energy (~ 316 kJ/mol³⁸) compared with that of the Al–O bond (~ 511 kJ/mol³⁹) at 298K, higher energy is required to debond wafers that are bonded with Al₂O₃.

Figure 12.24 is the transmission electron micrograph image at the bonding interface of bonded Al₂O₃/PE-TEOS wafers. A distinct thin layer that is



12.24 Cross-sectional TEM image shows a seamless bonding interface in the Al₂O₃/PE-TEOS wafers.

sandwiched between the PE-TEOS oxide layers is clearly seen. This layer is believed to be the bonded Al₂O₃ layer. As can be seen, the Al₂O₃ layer is uniformly bonded with no sign of micro-void. This confirms that a seamless bond at the micro-scale has been successfully achieved.

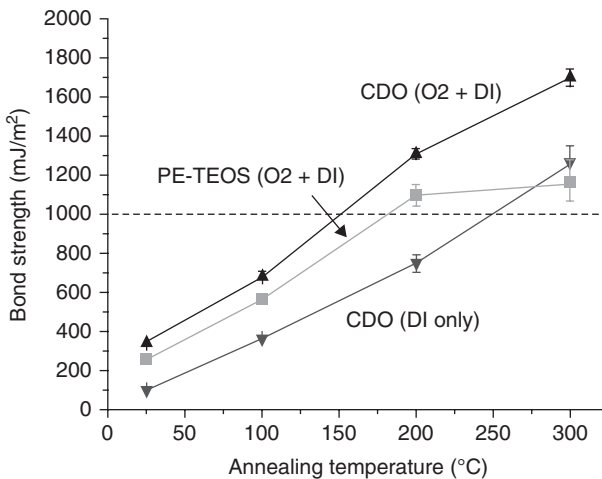
12.9.2 Low- κ dielectric bonding

In order to resolve issues related to signal propagation delay, cross talk, and power consumption in ultra large scale integrated (ULSI) applications, low permittivity dielectrics such as carbon-doped oxide (CDO) are widely used by the semiconductor industry as the interlayer dielectric (ILD) as a replacement of the conventional PE-TEOS.^{40,41} The deposition of low- κ CDO film can be carried out in a PECVD system by incorporating carbon in the form of methyl ($-\text{CH}_3$) group into a silicon oxide film. With carbon doping, bridging Si-O bonds are replaced by non-bridging Si-CH₃ bonds resulting in a lower density. This increases the film porosity of the film to around 7% and reduces the dipole density in the film, yielding a lower effective dielectric constant value ($\kappa < 3.9$).⁴² Even though CDO film is widely used in the CMOS process as interlayer dielectric in the back-end processes in recent technology nodes, there is very limited study on its bonding properties. Therefore, it is worthwhile studying its fusion bonding property for 3D integration applications as one can reuse the existing low- κ CDO film and reduce the dielectric capacitance to improve the overall performance of 3D ICs.

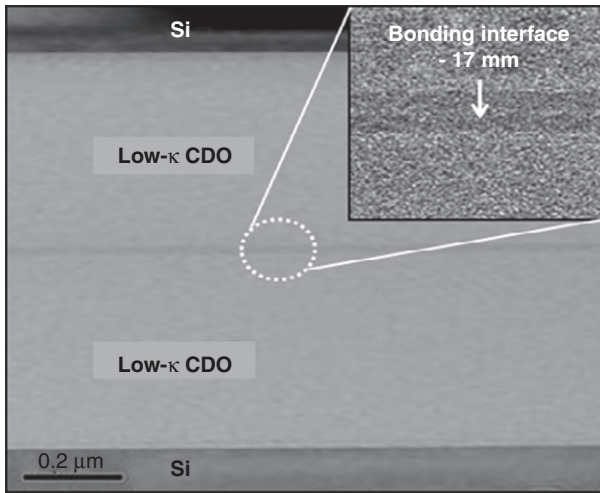
Oxygen plasma activation is commonly used to remove carbon-based contaminant from the oxide surface in order to enhance oxide-to-oxide bond strength at low temperatures. Since CDO film contains a larger amount of

carbon on top of possible surface contamination, the application of oxygen surface activation becomes necessary. This activation method is applied on low- κ CDO samples prior to wafer bonding to modify the dielectric surface to be more hydrophilic. Upon the oxygen plasma treatment, the methyl (Si-CH₃) groups near to the low- κ CDO film surface are oxidized and subsequently the silanol (Si-OH) groups are formed resulting in a sharp decrease in the contact angle (CA) value from 43.9° to 2.5°. The reduction in the CA value of PE-TEOS film is attributed to the removal of carbon containing contaminant.

Figure 12.25 presents a summary of the bond strength evolution during post-bonding annealing in an inert N₂ ambient for the temperature range 100–300°C for a duration of 3 h. The bonded wafers with low- κ CDO film are compared in terms of bond strength as a result of plasma exposure. All bonded low- κ CDO and PE-TEOS wafers exhibit a bonding strength of < 400 mJ/m² after bonding at room temperature. During heat treatment, the figure shows an improvement of the bonding strength for all bonded low- κ CDO and PE-TEOS wafers with the annealing temperature. The bonded low- κ CDO wafers demonstrate a higher bonding strength as compared to the control PE-TEOS wafers. This discrepancy is attributed to a higher porosity in the low- κ CDO film that provides a path for water molecules (by-products) to diffuse easily out of the bonding interface and leaves behind strong siloxane (Si-O-Si) bonds in the low- κ bonded CDO wafers. In the bonded PE-TEOS wafers, signs of saturation beyond 200°C are shown that are not observed in the bonded low- κ CDO wafers. With a 300°C annealing temperature, bonded low- κ CDO wafers (1700 mJ/m²)



12.25 Variation in bonding strength for O₂ plasma treated low- κ CDO and PE-TEOS films at various annealing temperatures.



12.26 Cross-sectional TEM image shows a seamless bonding interface of low- κ CDO films. No microvoid is observed at the bonding interface.

show a bonding strength exceeding that of PE-TEOS wafers (1160 mJ/m^2) by as much as 46.2%. Since the plasma-activated CDO surface contains less carbon and hence presents higher surface energy, the bond strength of the bonded wafer pair is enhanced by 33.8% from 1270 to 1700 mJ/m^2 with oxygen plasma surface activation after annealing at 300°C . With plasma activation, the bonded CDO wafers demonstrate bond strength of 1300 mJ/m^2 (which meets the requirement of 1000 mJ/m^2 for subsequent processing) after annealing at 200°C for 3 h. Without plasma activation, however, the required strength is unattainable and the bonded CDO wafer pair only demonstrates a bond strength of 750 mJ/m^2 .

Figure 12.26 is the TEM image of the bonding interface of low- κ CDO wafers. A distinct, thin layer of approximately 17 nm in thickness sandwiched between the low- κ CDO layers at the bonding interface is clearly observed in the inset of the high resolution image. This layer is uniformly bonded without any sign of microvoid and it is believed to be originated from the thin oxygen-rich layer that is formed on top of the CDO film as a result of oxygen plasma activation. This TEM image confirms that a seamless bond at the micro-scale level has been successfully achieved on the low- κ CDO wafers.

12.10 Summary

SOI wafers are very attractive for wafer-to-wafer ultra-thin Si layer transfer and 3D IC stacking without the need for high aspect ratio TSV. This platform promises an extremely high density of vertical interconnect between

the active layers in 3D IC and hence paves the way for specific applications in imaging and high performance computing. Building on this promise, this chapter outlined the material and process requirements of SOI-based 3D IC. Generic and customized process flows were presented in a systematic manner. Two major types of wafer bonding technology based on Cu–Cu bonding and oxide–oxide bonding were examined specifically for SOI-based 3D IC realization.

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Silicon-on-insulator (SOI) technology for photonic integrated circuits (PICs)

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Abstract: In this chapter we will discuss the potential and challenges for silicon-on-insulator (SOI) as a substrate for photonic integrated circuits (PICs). Silicon photonics has attracted a lot of attention in recent past years and has grown quickly from a niche research field to a technology with considerable industrial traction. It is now regarded as one of the most promising routes towards large-scale deployment of photonic ICs.

Key words: CMOS-photonics, silicon waveguides, silicon modulators, wavelength filters, grating fiber-chip couplers.

13.1 Introduction

In this chapter we will discuss the potential and challenges for silicon-on-insulator (SOI) as a substrate for photonic integrated circuits (PICs). Silicon photonics has attracted a lot of attention in recent years and has grown quickly from a niche research field to a technology with considerable industrial traction. It is now regarded as one of the most promising routes towards large-scale deployment of PICs.

Photonic integrated circuits are chips that combine many optical functions. These typically consist of the generation, transport, filtering and detection of light. PICs find their applications mainly in telecom and datacom solutions, where they provide information processing for optical fiber links. The use of optics for communication, and fiber in particular, has become widespread because of the enormous data capacity: optical signals can be modulated at bitrates of 10-40-160 Gbps, and many such signals can be transported in parallel over the same physical fiber by using different carrier wavelengths. Such wavelength-division multiplexing (WDM) boosts the capacity to multiple terabits per second (Tbps) (Onaka *et al.* 2006). The multiplexing/demultiplexing of these wavelengths is done on photonic ICs. On-chip, light is transported in waveguides, and similar data capacities are possible: in combination with the increasing bandwidth demands for on-chip, inter-chip and

board-level interconnects, photonics is being considered as a viable solution for short-distance interconnects.

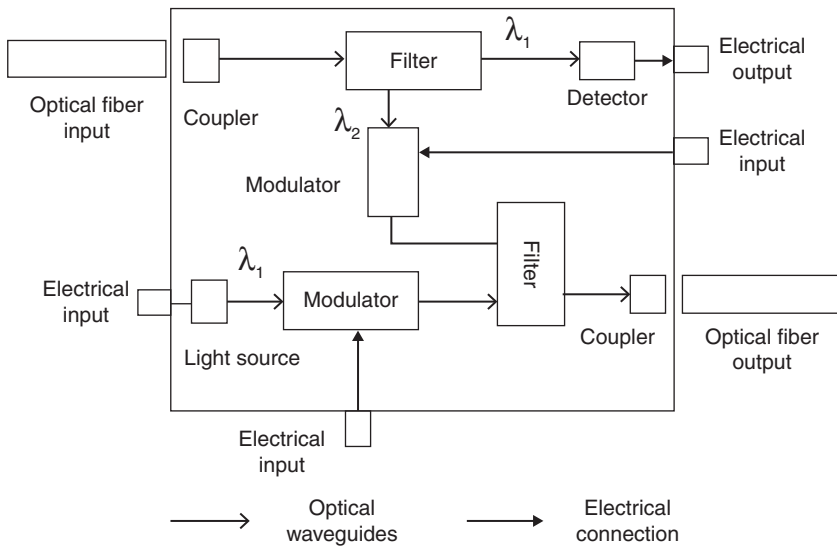
This will require the development of densely integrated electronic-photonic circuits. The prospects of this integration are immense. The essential components, such as the laser, modulators and detectors all can have a large bandwidth. However, the optical devices being used currently in classical communication systems are large, discrete and expensive. In order to use these components in an integrated form, they should be engineered to various specifications, such as material, size, bandwidth, power and process compatibility. Integration of photonic and electronic circuits will also enable communication networks with higher complexity and unique functionality. Similar to electronic integrated circuits, photonic integrated circuits should exhibit lower cost, higher reliability, and increased functionality compared to discrete components.

But interconnects are not the only application of photonic integrated circuits. A potentially huge market exists in sensors, spectroscopy and metrology applications, where light is used as a probe, rather than as a carrier of information.

13.1.1 Photonic integrated circuits

The main concept behind a photonic integrated circuit is to monolithically integrate all required optical functions on a single chip, preferably in a single material platform. These components include light sources, waveguides, light-chip couplers, splitters and combiners, wavelength-selective devices such as filters, electro-optic devices and photodetectors. Figure 13.1 shows a generalized example of a photonic integrated circuit. Unlike electronics, the range of photonic building blocks is very diverse, and a very heterogeneous set of materials is being used for the different functions. Functional building blocks include the following:

- **Waveguides:** to guide light from one point on a chip to another. Key performance metrics are a low propagation loss, a small cross-section and a compact bend radius.
- **Light sources:** lasers or light-emitting diodes are typically used. These can be either on-chip, or piped in with an optical fiber as an external power supply. Lasers typically tend to generate a lot of heat.
- **Photodetectors:** to convert optical signals into electrical ones, photodetectors are used. Performance is measured by responsivity (photocurrent produced for a given optical power), dark current and operation speed (which is largely determined by the size).
- **Modulators:** to imprint an electrical signal onto an optical carrier, an electro-optic modulator is needed. This requires an efficient way to change the optical properties of the materials. Modulator efficiency is



13.1 Schematic view of functions to be integrated on a PIC.

measured in the electrical voltage or current that is needed to induce a certain optical phase shift, and the operating speed is limited by the electrical parameters and the optical effect that is being used.

- **Wavelength filters:** to combine and split wavelength channels in a WDM system, optical filters are needed. These typically consist of an on-chip optical delay line. Control of these delay lines (both in fabrication as in post-fabrication trimming or tuning) is essential, and the wavelengths need to be well-controlled.

The functionality of a photonic circuit can be just passive, where light is passively transported or filtered, or active, where an electrical signal is embedded on or read from light. The choice of the material platform to realize such a photonic integrated circuit depends on its desired functionality. Typical material systems in use include the following:

- **III–V semiconductors:** are the most-used materials for semiconductor lasers, and also suitable for optical waveguides and efficient modulators and integrated photodetectors. Depending on the choice of wavelengths, InP-based or GaAs-based materials are used.
- **Silica on silicon:** glass is a very good waveguide material. It provides a mature technology for passive waveguide circuits, but the building blocks are quite large and thus the integration density on a single chip is very low.

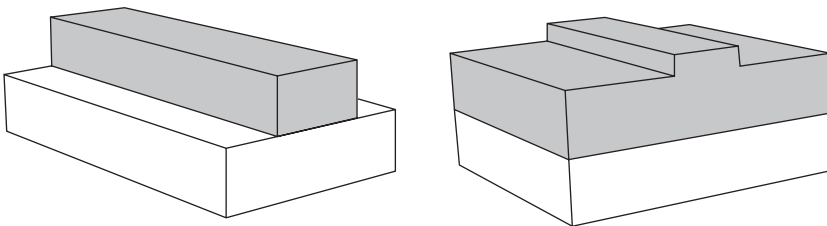
- Lithium niobate: has very strong electro-optic effects, and therefore a material of choice for efficient modulators.
- Silicon: is transparent for telecom wavelengths, and supports very compact waveguide structures. Good modulators and integrated germanium detectors have been demonstrated, but light sources pose a considerable challenge.

13.1.2 On-chip optical waveguides

The main purpose of a photonic waveguide circuit is to transport light through a medium between two designated points. To accomplish this, light can be confined in an optical waveguide: a line consisting of a core of high refractive index surrounded by a cladding of lower refractive index. This is the principle on which optical fibers are based: a cylindrical core of high refractive index glass surrounded by low index glass. On a chip, waveguides are typically defined as high-index lines in a layer of high refractive index. Two possible geometries are shown in Fig. 13.2.

The refractive index contrast between the core and the cladding is a very important determining factor in the choice of waveguides. A higher contrast will have the following effects on the waveguide behavior:

- Core size: high contrast can confine the light in a smaller cross-section. Glass waveguides (contrast 1.45 to 1.44) have a core of 10 μm . Semiconductor strip waveguides surrounded by glass (contrast 3.48 to 1.44) can confine light in a submicron strip.
- Bend radius: the tighter the confinement, the shorter the waveguide can be bent. Light cannot be guided around sharp angles, and while low-contrast waveguides need bend radii of 1 mm–1 cm, semiconductor strip waveguides can support bends as small as 2 μm .
- Dispersion: a higher index contrast and smaller core implies that the waveguide dimensions are much closer than the wavelength of the light. This makes the behavior of the waveguide (effective index) more wavelength dependent. This can have significant functional implications if



13.2 Two different on-chip waveguide geometries etched in a high-index layer.

signals on different carrier wavelengths need to be transported through the same waveguide.

- Sensitivity: as discussed further in much more detail, geometric variations will have an effect on waveguide behavior. The higher the index contrast, the larger the sensitivity, to the extent where high-contrast waveguides need to be fabricated with nanometer-scale accuracy.

Light is an electromagnetic wave: its propagation is governed by its electric and magnetic field distribution in the waveguides. These field distributions are called optical modes. Depending on their dimensions waveguides can support one or more propagating modes. Each mode is characterized by its propagation constant or effective refractive index (n_{eff}), which incorporates both refractive index of the wavelength of light, core (n_{core}), cladding (n_{clad}) and dimension of the waveguide (width and height).

Single-mode operation is, in most cases, preferred over multi-mode operation for many reasons. The higher order modes travel with a different propagation constant (speed) compared to the lowest order mode and are less confined in the waveguides. This can give rise to timing errors and additional (and unpredictable) losses. Single-mode operation therefore allows for simpler circuit design. Waveguides can be made single-mode by keeping their cross-section sufficiently small. This is illustrated further for silicon waveguides. Taking all these aspects of on-chip optical waveguides into account, we will see in the next section that silicon photonics, based on silicon-on-insulator (SOI) substrates, provides a compelling technology for large-scale photonic integrated circuits.

13.2 Silicon (on insulator) photonics

In the last decade, silicon-on-insulator (SOI) has become an attractive material for compact photonic devices. There are three key reasons for this. First of all, crystalline silicon is an exceptionally good optical material, with very low absorption at wavelengths longer than 1200 nm. This region contains the very commonly used telecom wavelength ranges around 1310 and 1550 nm. Secondly, the refractive index contrast between silicon and silicon dioxide is higher than any other material system for integrated photonics. As already mentioned, a high refractive index contrast allows light confinement in a sub-wavelength waveguide cross-section, and it enables larger scale integration of photonic components on a chip. The third reason why SOI is becoming an important photonic substrate is its compatibility with CMOS manufacturing processes: Silicon photonics can be fabricated with the same technology, which opens up avenues to mass-manufacturable photonics.

13.2.1 SOI waveguides

Two common types of SOI waveguides are shown in Fig. 13.3. In both cases a silicon waveguide core is resting on top of the SOI buried oxide (BOX) layer. The lower-index BOX optically separates the waveguide core from the silicon substrate: optical waveguide modes are never fully confined in the silicon core, and exponentially decaying ‘tails’ extend into the silicon dioxide cladding. If the cladding is too thin, the mode will ‘feel’ the underlying silicon substrate, which also has a high refractive index. The result will be a radiative leakage of the light into the substrate.

Large-core SOI waveguides

The large-core silicon waveguide is typically between 1 and 3 μm thick, and 2–5 μm wide. Such large cores with a high-index contrast of SOI are multi-mode, unless they are etched in such a way that they support only one guided mode: this is done using a rib geometry where the sides are only partially etched. The resulting waveguide has therefore a high-index contrast in the vertical direction, but in the plane of the chip the refractive index contrast is actually quite low (unetched *vs* partially etched silicon). Therefore, such waveguides are considered to be low-contrast waveguides, and they have bend radii in the order of millimeters.

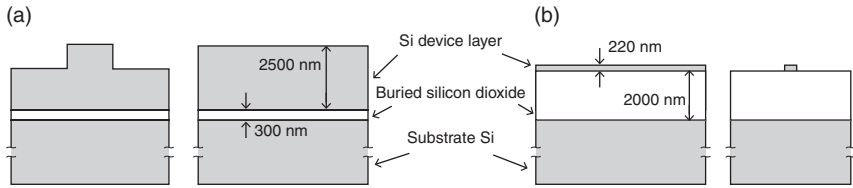
The large index contrast and thickness in the vertical direction do give a good vertical confinement, and a relatively thin BOX layer is sufficient to insulate the optical mode from the substrate. BOX thicknesses are typically in the order of 300–600 nm (Kurdi and Hall, 1988; Rickman *et al.*, 1992; Liu *et al.*, 2004; Lousteau *et al.*, 2004; Ling Liao *et al.*, 2005).

Large-core SOI waveguides typically have a relative low loss, in the order of 0.1–1 dB/cm. The large core also makes them relatively insensitive to geometric variations. However, it has proven difficult to directly integrate many optical functions in this technology. The integration density is rather small, and active functions are difficult to achieve. Still, the technology has found an active use in simple photonic circuits and individual components (Bestwick 1999; Feng *et al.*, 2010) and as an ‘optical bench’ technology, where individual optical components are positioned with pick-and-place techniques onto the SOI waveguide circuit (Kopp *et al.*, 2010).

For the remainder of this chapter we will not discuss further such large-core waveguides, instead focusing on the silicon nanophotonic waveguide technology.

Silicon photonic wires

Figure 13.3b shows a nanophotonic silicon waveguide, also called a photonic wire. In contrast with the large-core waveguides, a photonic wire has a



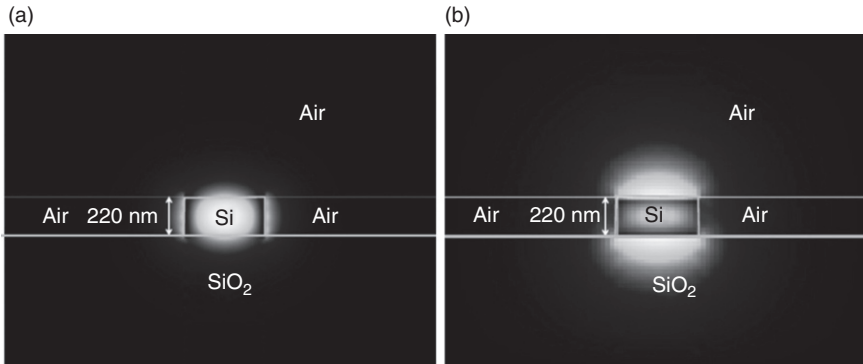
13.3 Silicon in insulator waveguides (cross-sections): (a) large-core silicon waveguide and (b) small-core silicon waveguide ('photonic wire'). Schematic drawn to comparative scale.

high refractive index contrast in all directions. With this high contrast (3.48 to 1.44), the single-mode condition is met when the core width/height is of the order of 300–400 nm. A common choice of SOI layer thickness is 220 nm, because at this thickness the core layer itself only supports one mode (a so-called slab mode) for each polarization at a wavelength of 1550 nm. The corresponding maximum waveguide width for single-mode behavior is around 520 nm. Other thicknesses have been used as well, and in general a choice of thicker silicon will need a narrower core to maintain single-mode behavior.

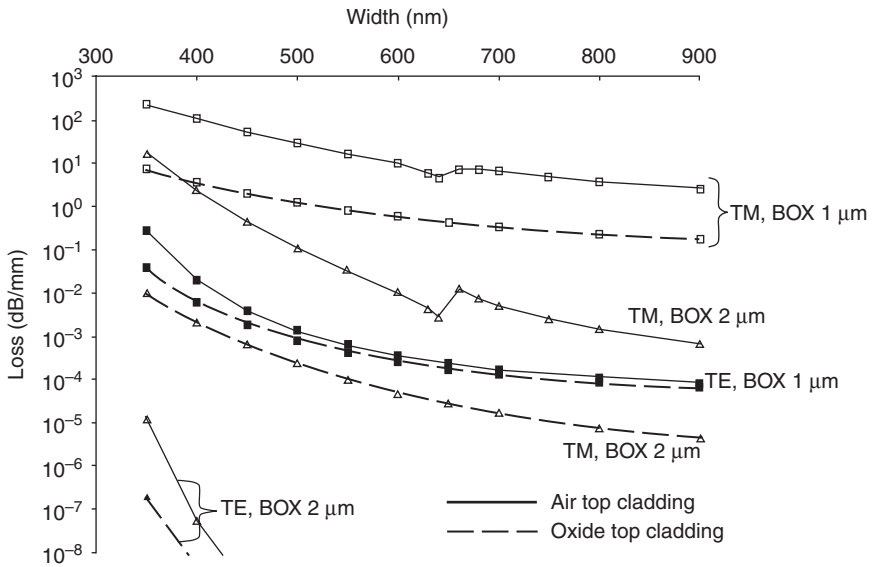
It needs to be noted that single-mode behavior is not an entirely accurate description. Even at these dimensions, a photonic wire will support two fundamental modes: one for the transverse electric (TE) polarization, and one for the transverse magnetic (TM) polarization. The intensity profile is plotted in Fig. 13.4. These modes behave very differently, because they will exhibit different field discontinuities at the top/bottom or left/right interfaces. In general the TE mode tends to be better confined, and it is considered the true fundamental mode. It has its dominant electric field vector in the plane of the SOI, and therefore field discontinuities at the waveguide sidewalls.

While both the TE and the TM optical mode are much smaller than with the large-core waveguides, they are less confined to the core and extend further into the oxide cladding. This imposes a requirement for a much thicker buried oxide. Figure 13.5 shows the propagation loss as a function of BOX thickness for TE and TM polarized light. For TE polarized light at least 1000 nm of BOX is required to avoid leakage, while for the less confined TM mode a much thicker BOX is required.

Each waveguide mode is characterized by its propagation constant, or more commonly by an *effective refractive index*, indicated by n_{eff} . Like an ordinary refractive index, the effective index describes the reduction in phase velocity of the light as it propagates through the medium. A higher refractive index will result in a slower propagation. The effective index is a weighted average between the refractive index of the core and the cladding: the more the optical mode is confined in the core, the higher its effective



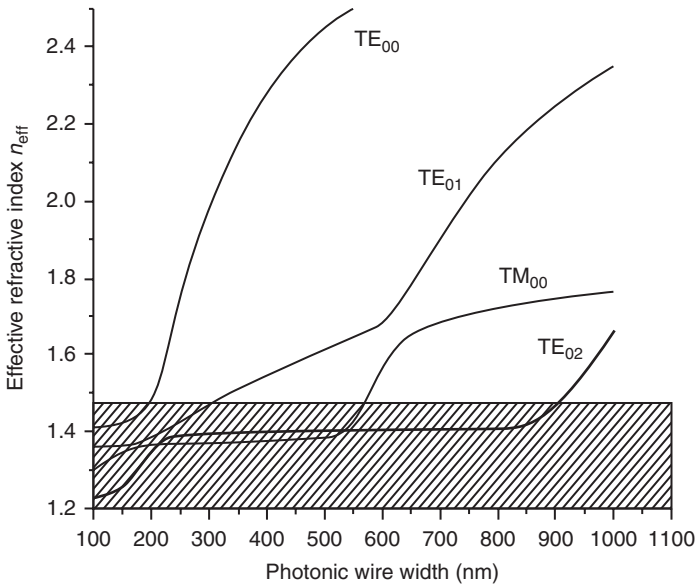
13.4 Mode intensity plots for the fundamental TE (a) and TM (b) mode of a photonic wire waveguide.



13.5 Waveguide propagation losses for photonic wires and different BOX thicknesses. Reproduced from Dumon (2007).

index. For a 450×220 nm waveguide, the effective index at 1550 nm is around 2.37.

Optical waveguides are *dispersive*, which means their effective index is wavelength dependent. One cause for this is the wavelength-dependence of the materials. But in a photonic wire, the main cause of dispersion is the geometry itself: because the dimensions of the core are on the same scale as the wavelength, a small change in wavelength will cause a change in confinement, and therefore effective index. The dispersion is described in the *group*



13.6 Effective refractive index, n_{eff} , for the TE and TM mode of a 220 nm thick photonic wire as function of core width.

index, n_g , (Chuang, 1995), linked to the *group velocity*, $v_g = c/n_g$. The group velocity is the propagation speed of a wave packet, and this is the relevant quantity for the transport of information (i.e., a modulated signal). Because of the dispersion, the group index in a silicon wire is, at $n_g = 4.3$, considerably higher than the effective index.

Figure 13.6 shows the effective refractive index, n_{eff} , of various modes in Si photonic wire waveguides as a function of waveguide width at 1550 nm for the TE and TM polarization. When n_{eff} is less than the index of the cladding n_{clad} the modes will start to leak into the cladding material. The width-dependence of n_{eff} is important for the performance of silicon photonic circuits, as we will discuss further.

Table 13.1 shows some of the SOI wafer stacks used in silicon photonics by different research groups. In addition to the thickness specification, other important requirements are thickness uniformity, doping concentration, surface roughness and defects, and sidewall roughness on the waveguides.

13.2.2 Fabrication of silicon waveguides

Fabrication of passive devices

Even though silicon is the base material for both microelectronics and silicon photonics, fabrication process flow and specifications can be very different. Most nanophotonic waveguide circuits are made by high

Table 13.1 Commonly used SOI stacks for optical waveguides

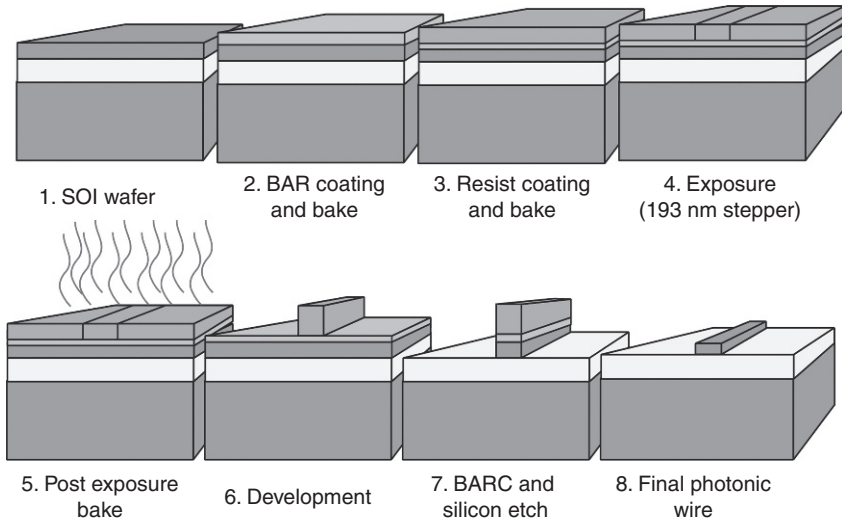
Research group	Si device layer thickness	BOX thickness	References
Univ. of California, LA	3000	1000	Yegnandarayanan <i>et al.</i> , 1997
Yokohama National Univ.	320	1000	Fukazawa <i>et al.</i> , 2004
IBM	220	2000	Vlasov <i>et al.</i> 2004; Xia <i>et al.</i> , 2007
Kyoto Univ.	250	–	Song <i>et al.</i> , 2005
MIT	220	1000	Sparacin <i>et al.</i> , 2005
NTT	200, 300	3000	Tsuchizawa <i>et al.</i> , 2005
Univ. of St. Andrews	220	1000	O’Faolain <i>et al.</i> , 2006
Univ. of Surrey	1000–1500	–	Reed <i>et al.</i> , 2006
Univ. of Glasgow	260	1000	Gnan <i>et al.</i> , 2007
CEA-LETI	400, 220	1000, 2000	Fedeli <i>et al.</i> , 2008
Intel	500	1000	Barkai <i>et al.</i> , 2008
Alcatel-Lucent, Bell Labs	200	3000	Rasras <i>et al.</i> , 2009
IMEC	220	2000	Selvaraja <i>et al.</i> , 2009a
Cornell Univ.	240	3000	Guha <i>et al.</i> , 2010

resolution lithography and dry etching. This flow is schematically represented in Fig. 13.7. Because of the submicron dimensions, the most commonly used lithography technologies are electron beam (Song *et al.*, 2005; Jacobsen *et al.*, 2005; Gnan *et al.*, 2007) and 248 nm (Bogaerts *et al.*, 2002; Tao *et al.*, 2010) and 193 nm optical projection lithography (Fedeli *et al.*, 2008; Selvaraja *et al.*, 2009b).

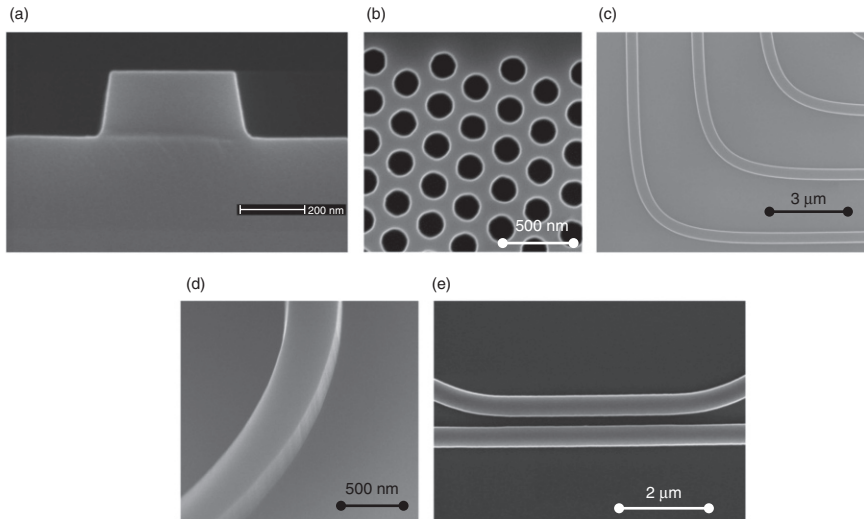
The patterning requirements for passive photonic waveguides, that is, optical circuits that do not actively change the optical properties of the waveguides, are quite different from electronics. For instance, photonic circuits can contain anything from isolated lines of different widths, dense trenches and holes in one patterning layer. Lithography needs to be done in a single step as alignment accuracy between on-chip features is very important. This requires careful lithography optimization as well as biasing and proximity corrections. A variety of photonic waveguide structures is shown in Fig. 13.8.

As the effective index of the photonic wires is very dependent on the core width, good control of critical dimensions (CDs) is especially important. In CMOS patterning processes the process window is generally defined as a 5–10% variation on the nominal CDs. In photonics, CD control of the order of 1 nm is generally required. In Section 13.4 provide more detail about the need for this CD control, and possible ways to handle or compensate CD variations.

Another important aspect of the photonic waveguide fabrication process is the quality at the core/cladding interface. Roughness at the interface will



13.7 Fabrication flow for SOI nanophotonic waveguides (Selvaraja *et al.*, 2009b). (BARC refers to bottom-anti-reflective coating.)

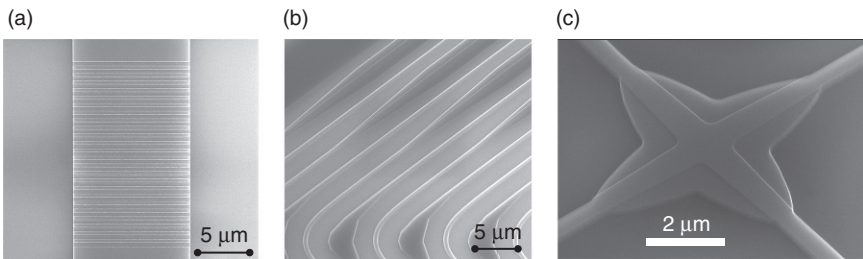


13.8 Examples of photonic waveguide structures. (a) Cross-section of a photonic crystal, (b) photonic crystal consisting of a triangular lattice of holes, (c) bend waveguide, (d) waveguide with smooth sidewall, and (e) a directional coupler.

Table 13.2 Photonic wire performance from different groups

Research group		Lithography	Si etch	Losses (dB/cm)	
Univ. of Glasgow	2008	e-beam	ICP-RIE	0.92	Gnan <i>et al.</i> , 2008
IMEC	2011	193 nm optical	ICP-RIE	1.36	Bogaerts and Selvaraja, 2011
IBM	2007	e-beam	-	1.7	Xia <i>et al.</i> , 2007
MIT-BAE	2006	248 nm optical	ICP-RIE	5.7	Sparacin, 2006
NTT	2005	e-beam	RIE + ECRPE	2.8	Tsuchizawa <i>et al.</i> , 2005
Yokohama National Univ.	2005	e-beam	ICP	120	Fukazawa <i>et al.</i> , 2004

Notes: ICP, inductively coupled plasma; RIE, reactive ion etching; ECRPE, electron cyclotron resonance plasma etch.

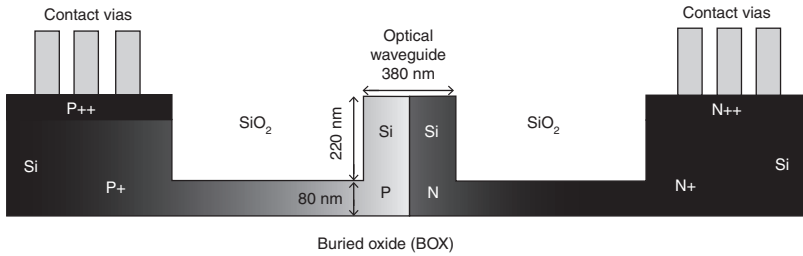


13.9 Photonic structures defined by a deep and shallow etch process: (a) a diffractive grating, (b) hybrid rib/strip waveguides, (c) a waveguide crossing.

cause scattering and back reflection in the waveguide, which is considered to be the prime cause of propagation loss. Also, surface states at the interfaces could lead to absorption.

The top and bottom surfaces of the core layer in commercial SOI substrates is typically smooth to a sub-nanometer level. Etched sidewalls, however, can exhibit significant roughness, typically of a curtain type, as shown in Fig. 13.8. Improved surface quality results in lower propagation losses. Table 13.2 gives an overview of published photonic wire losses of different groups with different technology. State-of-the-art photonic wires perform between 1 and 2 dB/cm.

More complex waveguide geometries, such as the rib waveguide from Fig. 13.2, can be defined by introducing additional etch layers. Rib waveguides have the disadvantage of a lower confinement (like the large-core SOI



13.10 Cross-section diagram of a silicon modulator (Li *et al.*, 2011)

waveguides), but have a smaller sidewall surface and therefore lower losses (Dong *et al.*, 2010; Bogaerts and Selvaraja, 2011). Also, the shallow etch can be used to define diffractive gratings that can be used for coupling to optical fibers (Taillaert *et al.*, 2006), as will be discussed in Section 13.3 (see also Fig. 13.9).

Integrating active devices

Apart from passive circuits, active electro-optic functions can be incorporated in the silicon circuit. The two most common functions are electro-optic modulation and photodetection.

Electro-optic modulation in silicon is possible in various ways. Although silicon is not an intrinsic electro-optic material, its refractive index changes with temperature (Della Corte *et al.*, 2000) and the concentration of free carriers (Soref and Bennett, 1987). Thermal effects are slower but more efficient and are generally used for tuning.

To change the effective index through carriers, the most common way is to embed a p-n junction inside the core of the waveguide. Forward or reverse biasing the junction will then change the carrier density in the optical mode. The realization of such junctions is rather straightforward, using standard CMOS implantation steps, followed by annealing. The optimal implantation pattern, energy and dose might be significantly different than those for CMOS devices (Yu *et al.*, 2010). The requirements for a significant change in carriers (for a strong modulation) has to be weighed against the need for a low propagation loss (absorption by carriers).

Metal contacting can be performed through similar standard CMOS steps, with silicidation, contact plugs and Al or Cu metal back-ends (Liao *et al.*, 2005). A typical cross-section of a silicon photonic modulator with metallization is shown in Fig. 13.10.

For thermal modulation, several materials in this stack could be used to build heaters: doped silicon (Zheng *et al.*, 2010), silicide (Van Campenhout *et al.*, 2010) or the metal back-end (Atabaki *et al.*, 2010). Alternatively, additional metal layers could be added (Thourhout *et al.*, 2010).

The requirements on the back-end are relatively relaxed. The main requirements are that the back-end stack does not induce excessive optical losses, either through diffusion of unwanted materials, or through close proximity of the absorbing metal to the waveguide.

To incorporate photodetectors, silicon in itself is not sufficient: it is transparent at these specific wavelengths. Therefore, the common approach is to incorporate epitaxial germanium. Different epitaxial strategies exist (Osmond *et al.*, 2009; Michel *et al.*, 2010), but most of them will seed on the SOI layer. Therefore, the orientation, content and stress of the SOI layer is important to guarantee high-quality epitaxial layers.

Integration with electronics

The processes described here mostly relate to silicon photonic circuits fabricated on their own. However, one of the main attractions of silicon photonics is the potential for integration with electronics, especially because the technologies share the material and manufacturing infrastructure. Moreover, the combination of photonics and electronics can yield the best of both worlds: information transport with light and logic/memory with electronics.

One of the important obstacles for monolithic integration of photonics and electronics on one SOI substrate is the vast difference in requirements for the layers. While the tendency for SOI electronics is to reduce the thickness of both buried oxide and top silicon layer, photonics needs a minimal BOX thickness, as well as a critical thickness of the silicon core for proper optical confinement.

Still, a successful example of the integration of photonics and electronics in the same process is Luxtera (Gunn, 2007; Masini *et al.*, 2008): incorporating waveguides, modulators and germanium photodetectors in a modified 130 nm SOI process. While the choice of layers is largely dictated by the existing electronics process, the SOI stack was engineered for best photonics performance, for example to achieve good fiber-chip coupling (see Section 13.3). Even so, the choice of stack makes it difficult to use photonic wires, and therefore the less confined rib waveguides are used, reducing the ultimate integration density.

Alternative integration strategies with electronics include 3D stacking, where the photonic and electronic parts are connected via the back-end metal process. Another route is to use deposited layers for the photonics. While amorphous silicon has been shown to yield decent waveguides (Liao *et al.*, 2000; Harke *et al.*, 2005; Orobtschouk *et al.*, 2005; Selvaraja *et al.*, 2009c), these still lag in performance with respect to crystalline waveguides. Also, making doped modulators without a high temperature anneal step is difficult. Lastly, while germanium epitaxy in aspect ratio-confined configurations has been demonstrated in the back-end (McComber *et al.*, 2010), it is not straightforward to implement high-efficiency photodetectors.

13.3 Photonic building blocks in SOI

A photonic circuit consists of a combination of several building blocks with very different functions. This is very different from electronics, where almost all functionality can be realized with a combination of transistors, diodes, resistors and capacitors. As already mentioned in Section 13.1.1, photonic circuits need much more functionality, incorporating waveguides, modulators, photodetectors, lasers and spectral filters. And within these categories there exists a wide variety of device concepts, each with its own merits. On top of the on-chip functionality there is a need for efficient coupling of light to optical fibers, for input and output.

The various optical functions can all be realized in silicon photonics, some more easily than others. In this section we will give a brief overview of the most common implementations, in order to make the limitations and the impact of the SOI substrate on the performance clearer in Section 13.4.

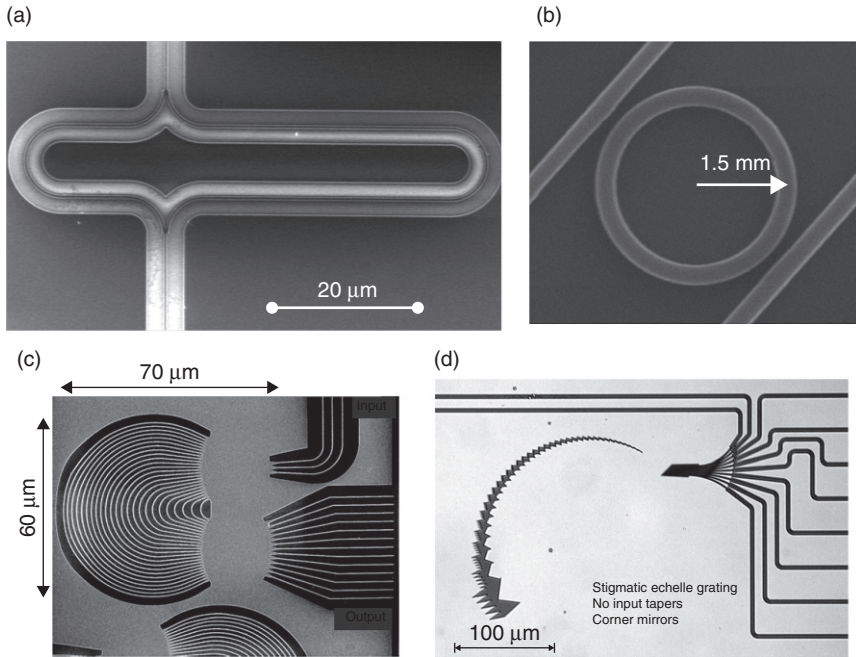
Silicon waveguides, the basic building blocks for any photonic integrated circuits, have already been introduced in Section 13.2.1. When we described the fabrication process of silicon photonics in Section 13.2.2 we also discussed their performance in terms of propagation losses.

13.3.1 Wavelength filters

Wavelength filters are the essential building block for wavelength-division multiplexing systems. They are used to combine and separate wavelength channels. The most simple wavelength filter can therefore be represented as a device with three ports: one input port and two output ports. One of the output ports will transmit a certain part of the optical spectrum, while the other port will transmit the rest. The block itself can of course introduce some loss, which might also be wavelength dependent.

Most wavelength filters are linear passive devices: their transmission is independent of the optical power, and because of reciprocity the device can be used in either direction: to split or combine wavelength channels.

Wavelength filters are based on interference: when two or more beams of light travel along a path of different length and recombine, the resulting output will depend on the phase relationship between the beams. When they arrive in phase, transmission is maximal; when in opposite phase the transmission can be reduced to zero. The phase delay is wavelength dependent: $\Delta\phi = 2\pi\Delta L \cdot n_{\text{eff}}(\lambda) / \lambda$, with ΔL the physical length difference between the paths, n_{eff} , the (wavelength-dependent) effective index of the waveguides, and λ , the wavelength. Here we see the important role of the effective index: it has a direct impact on the phase condition. As we will see in Section 13.4, this puts strong requirements on the fabrication. Or likewise, fabrication imperfections might have a severe impact on the performance of spectral filters.



13.11 Examples of silicon photonic spectral filters. (a) Mach-Zehnder interferometer, (b) ring resonator (Prabhu *et al.*, 2009), (c) arrayed waveguide grating (Sasaki *et al.*, 2005), (d) Echelle grating (Horst *et al.*, 2009).

There are several implementations of spectral filters possible. Some common examples are shown in Fig. 13.11. The simplest form is the Mach-Zehnder interferometer (MZI), where light is split in two waveguides which are later recombined. While simple, an MZI does not give a very useful filter response, and multiple devices need to be cascaded for good performance (Okayama *et al.*, 2010).

Instead of interfering two beams, a waveguide can be looped upon itself, such that the wave starts to interfere with itself in a feedback loop. When in resonance (i.e., when the wavelength of the light fits an entire time in the circumference of the ring) the light is extracted from the bus waveguide and coupled to the drop waveguide. These *ring resonators* can have very well-defined filter peaks, and they can also be cascaded for more elaborate filter configurations.

An arrayed waveguide grating (AWG) is in essence a more elaborate version of the MZI: instead of two waveguides, light is now distributed over an array of waveguides with different delay (Fukazawa *et al.*, 2004; Sasaki *et al.*, 2005; Dai and He, 2006; Dumon *et al.*, 2006). Depending on the phase delay, the light at the output is focused onto another output waveguide. As such, an

AWG can demultiplex many wavelength channels at the same time, instead of dropping just one channel. The performance of the AWG depends very much on the control of the delay between the different arms of the array: inaccuracies of the phase delay will result in increased crosstalk between the output channels.

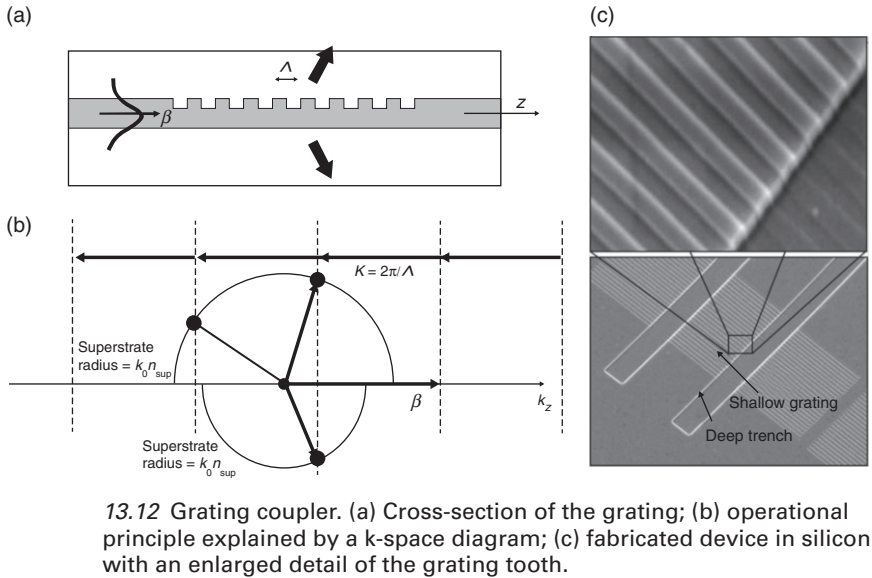
A similar device to the AWG is the echelle grating (Brouckaert *et al.*, 2007; Zhu *et al.*, 2008; Horst *et al.*, 2009; Song and Ding, 2009). Instead of using waveguides as delay lines, the light is reflected off a number of etched facets. The wavelength-dependent phase delay is caused by the offsets of the facets compared to the entrance and exit ports. The grating is curved such that light from the entrance is focused back on one of the exits. As there are no line waveguides involved, the effective index responsible for the phase delay is now that of the slab waveguide: in other words, the SOI layer which confines the light in the vertical direction. As with the AWG, variations in the effective index of the slab will result in phase errors, which can induce crosstalk between the channels.

13.3.2 Grating couplers

An important function on many photonic chips is the coupling of light to and from the chip. This is not as straightforward as it seems. The most common off-chip medium for transporting optical signals is the single-mode fiber. These have very low propagation loss, and consist of a very low-contrast cylindrical waveguide. As already mentioned in Section 13.1, the low contrast implies that the waveguide mode will be quite large. In the case of such a fiber, the mode diameter is over 10 μm . To couple such a large mode to a submicron silicon waveguide is far from trivial: when coupled directly, the efficiency is about 0.1%.

The alternative, commonly used solution to this coupling problem is a grating coupler, illustrated in Fig. 13.12. These consist of a diffraction grating etched into a broad but thin silicon waveguide. For the right wavelength band the diffraction at the grating teeth adds up, and light from a (near-) vertical fiber is coupled directly into the silicon waveguide. As with other passive devices, this works as well in the other direction: light from a waveguide is diffracted at the grating teeth, and for the right wavelength band the contributions will add up inside the optical fiber.

While this principle is simple, it has not been straightforward to make highly efficient grating couplers. A typical straightforward periodically etched grating has a coupling efficiency of about 30% (Taillaert *et al.*, 2006) although gratings with 70% efficiency have been demonstrated (Saha and Zhou 2009; Selvaraja *et al.*, 2009a, 2009d; Vermeulen *et al.*, 2010). This is in part due to the fact that each grating tooth diffracts as much downward towards the substrate as upwards towards the fiber.



However, the downward wave will be reflected at the underlying interface between the BOX and the silicon substrate. Because of the high-index contrast this reflection can be as much as 30%, and the reflected wave will then interfere with the upward-diffracted wave. Depending on the thickness of the BOX, this interference will be constructive (adding up to the upward-propagating power) or destructive (cancelling out some of the upward power). The optimum thickness is dependent on the choice of wavelength, and the performance can be further optimized by substrate engineering, as will be discussed in Section 13.5.

13.3.3 Modulators

As already introduced in Section ‘Integrating active devices’, silicon modulators can be realized by incorporating junctions in the waveguide core. There are two important types of such carrier modulators. P-i-n junctions can be forward-biased to inject carriers in the intrinsic region. In this regime, many carriers are used, which gives a very strong modulation of the effective index. However, such modulators are limited in speed because excess carriers need time to recombine. Typical operation speed of such modulators is 1–3 Gbps (Xu *et al.*, 2005), although special driving schemes can boost that to 10 Gbps (Xu *et al.*, 2007; Green *et al.*, 2007). Carrier-injection modulators are quite efficient, and a typical section of a phase modulator to obtain a phase shift of π is a few hundred micrometers.

As an alternative to carrier injection, modulators can be implemented in a reverse-biased p-n junction. As the amount of charge is much smaller, these modulators are typically longer (1–3 mm). However, because they are not limited by carrier lifetimes they can be much faster. Operation of 28 Gbps and even up to 40 Gbps has been demonstrated (Thomson *et al.*, 2011, 2012).

Junction-based modulators behave as phase modulators. That means they will change the phase of the light at their output, not the amplitude. To convert phase into amplitude, these modulators need to be combined with a spectral filter. This can either be an MZI (Thomson *et al.*, 2011, 2012) or a ring resonator (Xu *et al.*, 2005; Zheng *et al.*, 2011). The former has the advantage of being generic and quite broadband, while the latter can be quite compact but is limited in operational speed due to the bandwidth of the optical resonance.

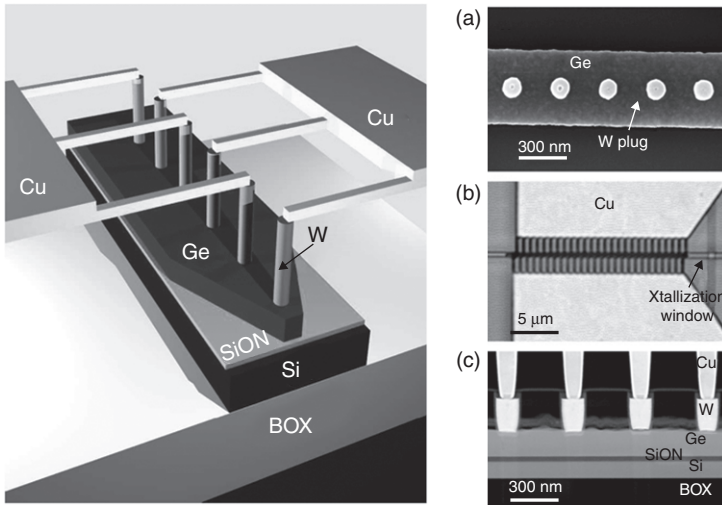
When it comes to high-speed performance of modulators, the effect of the silicon substrate starts playing a role (Raskin, 2009). High-speed modulators in an MZI configuration often use RF travelling wave electrodes implemented in the metal layers. The impedance and the losses, together with those of the junction waveguide, are affected by the thickness of the buried oxide and the conductivity of the carrier wafer. The tendency is to move to high-resistivity wafers for SOI photonics beyond 40 Gbps (Ziebell *et al.*, 2012).

13.3.4 Photodetectors

Photodetectors in a silicon photonics context are typically implemented in epitaxially grown germanium. With its bandgap around 1550 nm (up to 1600 nm when strained) it absorbs heavily in the telecom wavelength range. That means a waveguide-integrated detector can actually be quite small, in the order of 10–30 μm in length (Chen *et al.*, 2008; Masini *et al.*, 2008; Vivien *et al.*, 2009). The challenge is in designing the device such that light is travelling as little as possible in dislocation-rich layers caused by the lattice mismatch, and that generated electron-hole pairs are efficiently collected.

While germanium detectors were for long inferior to III–V InGaAs detectors, recent progress has yielded detectors with similar responsivities, around 1 A/W at 1550 nm wavelength (Vivien *et al.*, 2009). Also, the compact size of waveguide-integrated detectors allows fast performance, with 50 Gbps already demonstrated (Klinger *et al.*, 2009; Assefa *et al.*, 2010). Such an integrated waveguide detector is illustrated in Fig. 13.13.

As the performance of germanium detectors depends on the quality of the epitaxy, the properties of the underlying SOI layer can have an impact. Little research has been published on this, but strain engineering could have a major impact on this integration work.



13.13 Germanium waveguide photodetectors. Left: schematic of Ge waveguide photodetector. Right: fabricated device (a) top-down SEM image of the detector, (b) top-down microscope image showing contact and (c) cross-section of the device (Assefa *et al.*, 2010)

13.3.5 Lasers

The most difficult component to integrate on a silicon photonics chip is the optical light source. Silicon has no direct bandgap, and neither has germanium. Almost without exception all semiconductor lasers are built in III–V materials, requiring complex epitaxial stacks with (multiple) quantum wells or quantum dots layers.

The direct approach to bringing a laser to a silicon substrate is therefore to incorporate such III–V material stack on the SOI wafer. Doing this with epitaxy is considered as the 'Holy Grail', but the lattice mismatch is so significant that realizing this is not likely on a short time scale. Instead, a bonding approach is preferred: using either molecular bonding (Fang *et al.*, 2007; Ferrier *et al.*, 2008) or an adhesive (Roelkens *et al.*, 2006) a thin film of III–V material can be deposited on the silicon substrate. Moreover, because of the heterogeneous bonding, the III–V stack can already have its epitaxial layers, and the silicon wafer can already be patterned with waveguide circuits (Stanković *et al.*, 2011). This way, the subsequent patterning of the III–V material can be done at wafer scale. This technique has already yielded various types of lasers, from compact microcavity disk lasers with 100 μW optical output (Campenhout *et al.*, 2008) to stripe lasers with up to 5 mW of output (Lamponi *et al.*, 2012).

Another approach is to use effects in silicon to provide optical gain. Possibilities include parametric amplification using four-wave-mixing (Salem *et al.*, 2007; Kuyken *et al.*, 2011), or using phonons in the silicon lattice through Raman scattering (Jalali *et al.*, 2006).

A recent development throws a more hopeful light on silicon photonic lasers. In 2011, lasing was demonstrated in germanium (Liu *et al.*, 2010). This was made possible by a combination of strain to offset the direct and the indirect bandgap, and heavy doping to saturate the indirect conduction band valley (El Kurdi *et al.*, 2009; El Kurdi *et al.*, 2010). Based on this technique, an electrically pumped laser was demonstrated in 2012 (Michel *et al.*, 2012).

As with germanium photodetectors, substrate engineering might have a significant impact on the future developments on germanium lasers on silicon.

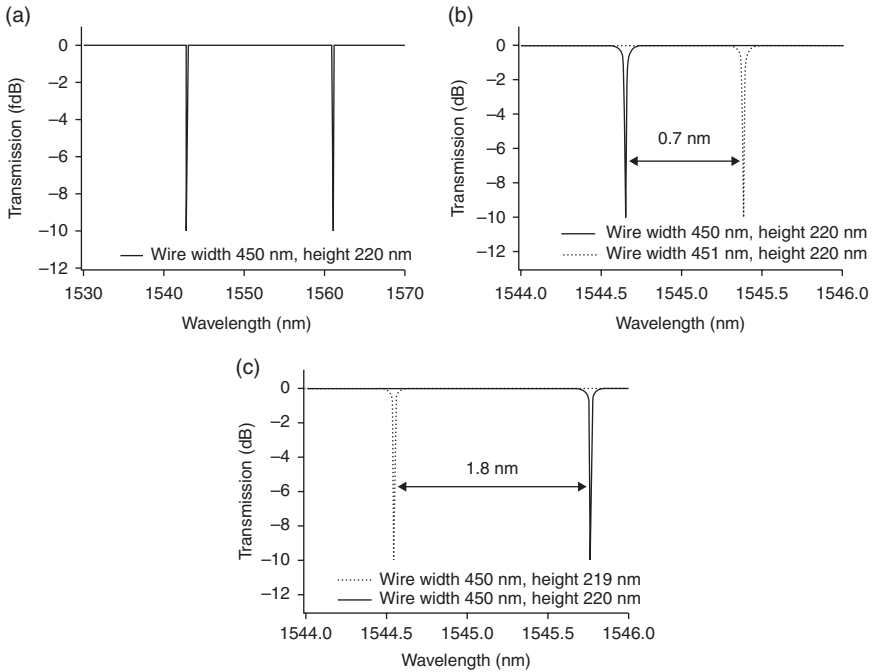
Lasers, especially electrically pumped ones, consume a lot of power, and typically run quite hot. Moreover, they tend to be less efficient or even shut down at higher temperatures. Good thermal control of lasers is therefore essential, and heat-sinking is the primary passive solution. Sitting on top of an SOI stack is not necessarily the best solution, as the thick buried oxide thermally insulates the laser from the substrate. Substrates with good thermal sinking properties, while at the same time keeping good insulation, might be required to drive a breakthrough in on-silicon lasers.

13.4 Device tolerances and compensation techniques

A lot of the photonic functions, and especially the wavelength-selective filters, are dependent on the value of the effective index, n_{eff} . The effective index can be controlled by the material parameters, the geometry, and also by operational and environmental conditions, such as temperature. As we have already seen in Section 13.2.1, the effective index of a photonic wire depends heavily on the core dimensions and the wavelength. As the optical phase delay in a wavelength filter changes linearly with n_{eff} , small changes in core dimensions could have an impact on the transmission of the filter. For instance, for a filter with a peak wavelength λ_0 , we will observe a shift $\Delta\lambda$ of the peak wavelength $\Delta\lambda/\lambda_0 = n_{\text{eff}}/n_g$. The group index, n_g , comes in when we take the wavelength-dependence of n_{eff} into account.

13.4.1 Effect of dimensional variations

To illustrate the sensitivity of n_{eff} to geometric variations, consider a ring resonator (or any other) filter with a circumference/delay length of about 35 μm , shown in Fig. 13.14. For wavelengths in the vicinity of 1550 nm, we

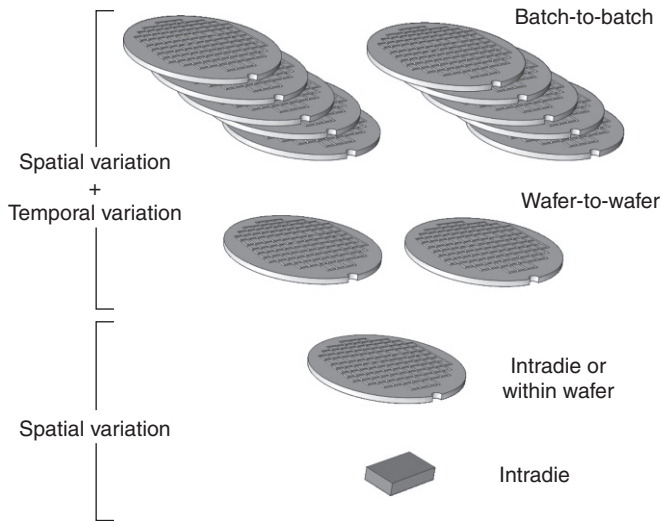


13.14 Sensitivity of a ring resonator filter. (a) Spectrum of a ring resonator with $35 \mu\text{m}$ circumference; (b) transmission spectrum of two rings with a 1 nm difference in width; (c) transmission spectrum of two rings with a 1 nm change in core thickness.

will find constructive interference in the spectrum spaced about 5 nm in wavelength. Depending on the application, wavelength channels in a WDM system can be spaced several nanometers apart, but in high-end system the spacing in the spectrum is as close together as 0.4 nm.

If we now look at the shift of the wavelength peak for small variations in geometry, we will find that a 1 nm change in waveguide width will result in about 1 nm of wavelength shift. The effect of the thickness is even stronger. A 1 nm thickness variation will yield a 2 nm shift in transmission wavelength. These variations are not measured locally. This means that nanometer-scale CD variations can easily shift the transmission over one or more channels.

Note that the local CD is not the most important metric. The important quantity is the accumulated phase shift over the delay line/round trip. This means that the average n_{eff} , or average width/thickness over the delay line should be controlled sufficiently well. This somewhat relaxes the specification on short length-scale variations, but introduces significant requirements for filters which require longer delay lines: long-scale nonuniformity might then start to dominate component performance.



13.15 Different levels of nonuniformities. Nonuniformities can be acquired within an individual die, but also within a wafer, within a batch or between batches.

13.4.2 Fabrication-induced nonuniformity

The permanent structural nonuniformity in devices is obviously influenced by the fabrication process employed in making them. The variation in the process manifests itself across time and space. Temporal process variation is often related to drift in consumables, changes in the incoming wafers, or process conditions over time. For example, the ageing of photoresist often changes the viscosity and contrast, thereby directly affecting the printed dimensions. Temporal variation is of critical concern in a mass manufacturing environment and results in nonuniformity from wafer to wafer and batch to batch. Besides temporal variation, spatial variation over the wafer also plays an important role in nonuniformity during the fabrication process. At the wafer level, we can separate sources of physical or structural variation into two categories: intra-die and inter-die (or within wafer) nonuniformity, as illustrated in Fig. 13.15. Given the generally small variation of the silicon layer thickness across the wafers, the magnitude and distribution of variations within a die can be different from those between dies (die-to-die).

- **Lithography induced nonuniformity:** this is typically caused by local proximity effects ($<1-2 \mu\text{m}$) and global stray light fluctuation. With proper characterization, the key lithography errors could be compensated by optical proximity corrections. In most high-end CMOS devices, the optical lithography is done at die-level, using a step-and-repeat process. Intra-die patterning or dimension variation caused by optical lithography can depend on the

mask-making process (e.g., writing field boundaries), and the orientation in a scanner. In addition, thickness and age of resist, antireflective coating and spinning conditions could also impact the lithography patterning variation. Using a better or more advanced lithographic tools have improved the critical dimension control. For instance, comparing nonuniformity of the same structures (using the same photomask and substrates from the same batch) the 193 nm lithography showed a dramatic improvement of the uniformity over 248 nm lithography tool (Selvaraja *et al.*, 2010).

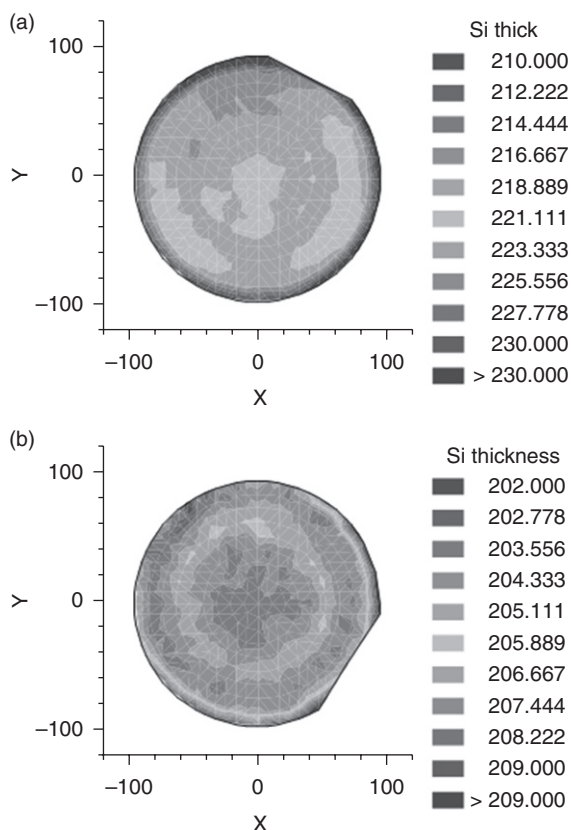
- Etch-induced nonuniformity: these can be caused by difference in local ($\sim 20\text{--}50\ \mu\text{m}$) pattern density, and by long-range variation in the plasma conditions. Local density control can be added in the form of tiling patterns. Global variations of plasma conditions (temperature, density) typically imprint a radial pattern on the wafer. Newer-generation tools provide better control and reduce this nonuniformity.
- Substrate thickness: the source of long-range nonuniformity which is the most difficult to control is the thickness variation of the base SOI substrate. Depending on the supplier, uniformity of the top silicon layer is specified to be controlled within 5–20 nm. Taking the figures above, this translates in tens of nanometers shift in wavelength.
- Other process nonuniformity: apart from lithography and etch, the main other processes which might induce nonuniformities are deposition steps (layer thickness and composition) and polishing (chemical mechanical polishing (CMP)).

Using monitoring structures, the intra-die nonuniformities can be separated from wafer-range or die-to-die nonuniformity. The intra-die uniformity can be up to 1–2 nm and short-range ($\sim 100\ \mu\text{m}$) nonuniformities can be as small as 0.5 nm (Selvaraja *et al.*, 2010), while longer ones (line width, thickness) can yield a good insight of the dominant causes of nonuniformity in a specific process flow.

The variations and nonuniformities are considered to be one of the main bottlenecks for widespread deployment of silicon photonics. While the typical CDs are quite relaxed compared to state-of-the-art transistors, the tolerances are much smaller. Also, controlling these parameters within the fabrication process is not always straightforward. The sensitivity numbers given here show that the photonic circuit is actually the most accurate measure for the CD variations, much more accurate than typical in-line measurements performed by SEM inspection or ellipsometry.

13.4.3 Nonuniformity compensation

Keeping nonuniformity of the effective index in check is one of the main challenges for silicon photonics. This can be handled at various levels, during operation or using pre- or post-fabrication steps.



13.16 Silicon thickness uniformity improvement using GCIB. (a) Before thickness correction and (b) after thickness correction.

Active tuning

Dimensional nonuniformities might introduce nonuniformities and misalignment of the wavelength peaks, but this does not necessarily render the chips useless. For instance, they can be actively tuned during operation: it is possible to use temperature (i.e., local heaters) to compensate for small variations of the effective index. Silicon has a high thermo-optic coefficient, and heating a delay line of a filter will cause the wavelength peaks to shift, with 50–100 pm/K. This means it requires a 10–20 K temperature change for a 1 nm shift, which corresponds with 1 nm of CD variation. This limits the extent of tuning, and also introduces significant power consumption. It has actually been shown that average chip power consumption scales with the CD control during fabrication (Zortman *et al.*, 2010).

Operational tuning involves more than just incorporating a heater element near the waveguide. As the technique also needs to compensate environmental temperature fluctuations (caused by external sources, but possible also by on-chip sources such as lasers or electronic hot-spots), thermal control will also require monitoring and feedback circuitry, complicating the design.

Post-fabrication trimming

An alternative to operational tuning is the use of per-chip post-fabrication trimming. After fabrication, chips can be characterized (even at wafer-scale using grating couplers) and the refractive index can be modified locally:

- **Stress:** exposing a silicon waveguide to an electron beam (Schrauwen *et al.*, 2008) or UV light will induce stress in the underlying oxide, and therefore in the waveguide itself. The stress causes a shift in the effective index of the waveguide, and this can be used to align the spectral response of a filter.
- **Overlays:** a change in the top cladding of the waveguide will also induce an effective index change. For instance, a photosensitive cladding material can be deposited (e.g., chalcogenide glasses) which can be effectively and locally tuned using exposure to visible or UV light (Naganawa *et al.*, 2005; Sparacin *et al.*, 2005).

Using these techniques, local corrections at sub-nanometer level have been demonstrated. However the time, and therefore the cost, of these trimming steps depends on the initial nonuniformity in the fabricated samples.

Pre-fabrication trimming

As the thickness of the SOI substrate is one of the main causes for non-uniformity, it makes sense to improve the thickness uniformity of the initial SOI substrate. One method to accomplish this is by local trimming of the substrate prior to the photonics fabrication. This can be done using gas cluster ion beam (GCIB) processes, milling the silicon based on a premeasured thickness map of the wafer (Kirkpatrick, 2003). Figure 13.16 and Table 13.3 show the thickness map and wafer statistics of a SOI wafer before and after

Table 13.3 Thickness uniformity improvement of SOI wafer

	Before correction	After correction
Mean	223.76 nm	204.41 nm
3σ	13.61%	2.13%
Range	19.98 nm	9.73 nm

thickness correction process. During the correction process a predetermined amount of Si is removed to flatten the wafer hence leaving a slightly thinner film of Si.

13.4.4 Conclusion

Silicon photonics devices are extremely sensitive to variations in geometry. As we have seen here, the tolerances for many devices are so low that it is almost impossible to meet the specification on uniformity with simple fabrication. Still, while active trimming and tuning can compensate the nonuniformity, good fabrication control can have a beneficial effect on the cost and power consumption.

13.5 Advanced stacks for silicon photonics

Up till now, we have discussed silicon photonics using a fairly standard configuration of silicon-on-insulator: a buried oxide of 1–3 μm , with a silicon top layer of 200–300 nm. While this has already led to good performance, optimization of the substrate could lead to significant improvements.

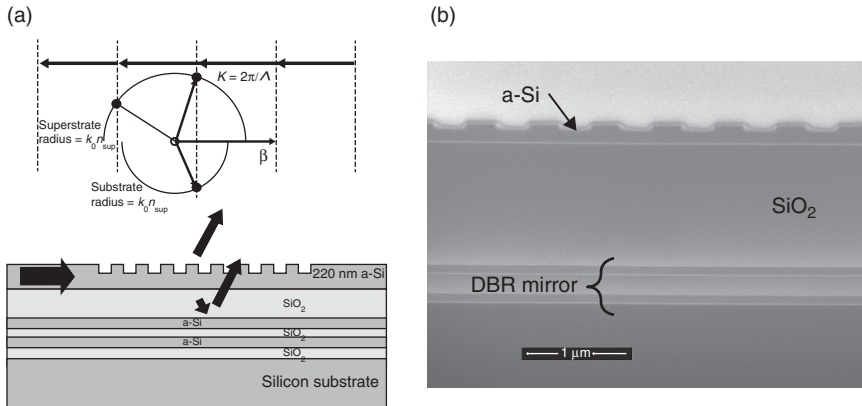
In this section we discuss a number of possible routes to engineer the SOI substrate specifically for silicon photonics. This includes:

- Stress engineering: incorporating stress in the top layer might facilitate processing or even enable novel functionality.
- Multi-layer SOI: substrates with a more elaborate stacks of silicon/oxide could improve performance of grating couplers, or enable multi-layer photonic circuits.
- Local SOI: substrates with local areas of photonic SOI could be used to combine silicon photonics with bulk CMOS.
- XOY: using another guiding layer material and another material instead of the buried oxide could enable waveguides at other wavelengths, better thermal properties or efficient active components.

We will now discuss these in some more detail.

13.5.1 Strained SOI

The guiding layers of photonic SOI are not heavily stressed, although some buckling can appear when removing the BOX layer under isolated waveguide structures. However, incorporating stress could have beneficial effects. For instance, strained silicon breaks the centrosymmetry of the crystal lattice, and therefore induces a second-order nonlinear susceptibility. In other words, the refractive index of silicon can now be changed by applying an



13.17 Grating coupler with bottom distributed Bragg reflector (DBR) mirror: (a) operating principle; (b) SEM cross-section.

external electric field. This offers opportunities for electro-optic modulation without the use of carriers, potentially improving the speed and reducing the absorption loss (Jacobsen *et al.*, 2006).

Another motivation for introducing strain is to facilitate the epitaxial growth of germanium, yielding better photodetectors and lasers.

13.5.2 Multi-layer SOI

Going beyond the single silicon layer in SOI is not a straightforward process as it requires multiple repeats of the SOI fabrication process. Still, for photonics it can have benefits.

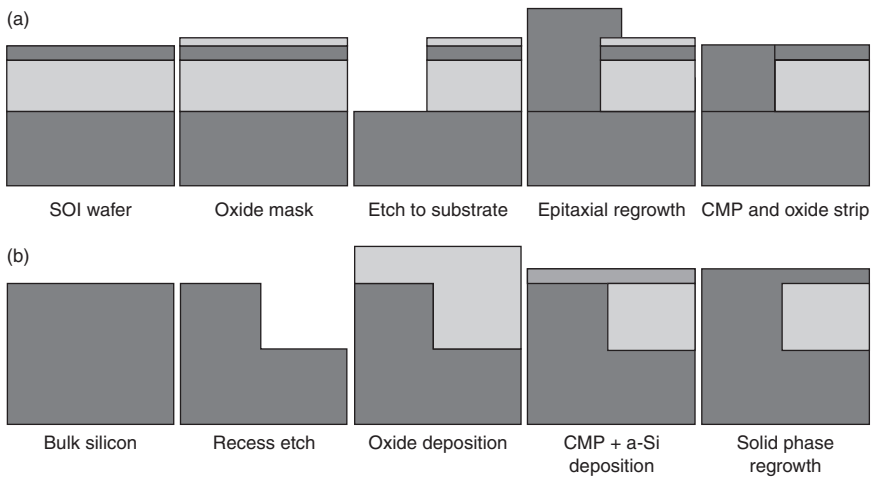
Multi-layer circuits

All photonic circuits discussed here are routed in a single plane. Having multiple guiding layers as in CMOS metal stacks would dramatically improve the scalability of photonics. However, that is not straightforward, as good waveguides require high-quality silicon layers.

A process to incorporate additional silicon-on-insulator (SOI) layers on the existing patterned SOI stack would make this possible. Using amorphous silicon, multi-layer circuits have been tried, but with limited performance (Koonath and Jalali, 2007; Selvaraja *et al.*, 2007).

High-efficiency grating couplers

As discussed in Section 13.3.2, grating couplers diffract light from a silicon waveguide upward into a fiber. But a significant fraction of the light is also



13.18 Making local SOI: (a) starting from an SOI wafer; (b) starting from a bulk wafer.

diffracted downward towards the substrate. A part of the downward light is again reflected upward at the BOX-substrate interface and interferes with the upward-travelling part.

To optimize the efficiency of the grating coupler, it would help to reflect all the downward-travelling light, and controlling the thickness of the BOX would give full constructive interference with the upward-travelling wave, maximizing the coupling efficiency.

This concept has been demonstrated by using an amorphous silicon distributed Bragg reflector (DBR), consisting of several pairs of thin oxide and amorphous silicon layers (Selvaraja *et al.*, 2009c). The structure is shown in Fig. 13.17. The multiple interfaces act as a broadband mirror, effectively reflecting all the light. On top of the mirror is a thicker oxide layer to optically insulate the mirror layers from the evanescent field in the waveguides. The waveguides are fabricated in amorphous silicon. By choosing the correct thicknesses, this grating achieved close to 70% coupling efficiency.

The main problem with this device is the fact that the bottom mirrors have to be deposited first, which means only deposited layers can be used for the waveguides. An SOI stack which already incorporates the correct mirror structure would dramatically improve the performance of the waveguides, by providing a crystalline core layer.

13.5.3 Local SOI

The requirements of SOI for photonics are very different than those for SOI electronics. In addition, a lot of electronics is made in bulk silicon, not SOI.

These conflicting requirements make it difficult to propose a generic strategy for monolithic co-integration of photonics and electronics.

One way out is the use of local SOI: only use the photonics SOI substrate where it is needed, while using a bulk substrate elsewhere. Two methods have been proposed to achieve this, illustrated in Fig. 13.18:

- Make a local bulk substrate (Zimmermann *et al.*, 2008): starting from a photonic SOI wafer, the locations for the electronics can be etched down to silicon substrate. Using epitaxy the substrate can be regrown to the level of the SOI and a subsequent planarization step then prepares the substrate for transistor and photonics processing.
- Make a local SOI substrate (Shin *et al.*, 2010): an alternative is to start from a bulk-silicon wafer. A deeply etched trench is then filled with an oxide and planarized. On top an amorphous silicon layer is deposited, which is then crystallized with solid-phase epitaxy, seeding from the original bulk substrate. While this recrystallization step will preserve lattice orientation, there will be dislocation seams near the center of the SOI areas where the regrowth phases meet up.

13.5.4 Something-on-something else

While the advantages of SOI for photonics have been discussed in detail in this chapter, silicon and silicon dioxide do have some significant drawbacks, and there might be much to gain in combinations of other materials which still provide a high-index contrast.

Other wavelength ranges

Today the focus of silicon photonics is on the wavelength band between 1300nm and 1600 nm, which is widely used for optical communication. For other applications, however, other wavelength ranges might have other material requirements. Some examples include:

- Visible wavelengths: silicon is not transparent for wavelength shorter than 1.1 μm . Incorporating a high-contrast stack that is transparent to near-IR and visible wavelengths would be exceptionally interesting for applications in spectroscopy and sensing, or even short-range communication. Possible high-contrast materials include silicon carbide ($n = 2.7$) (Liu and Prucnal, 1993; Song *et al.*, 2011) and diamond ($n = 2.4$) (Babinec *et al.*, 2011). Silicon nitride ($n = 2.1$) (Gorin *et al.*, 2008) could also be used, but the index contrast rapidly drops.
- Short-wave infrared (SWIR) and mid-infrared (MIR): towards longer wavelengths, SOI remains a useful material until 4 μm . After that, the

buried oxide starts to absorb heavily. A solution is the use of silicon-on-sapphire (Baehr-Jones *et al.*, 2010; Jackson *et al.*, 2011). For even longer wavelengths closer to 10 μm , the silicon is also no longer suitable, and germanium becomes a more interesting option (Soref, 2010). As most optical dimensions scale with the wavelength, this means that also the layers need to be thicker.

Longer wavelengths find their applications in spectroscopy, as many substances have unique ‘fingerprints’ in this wavelength range.

Thermal substrates

Photonic SOI substrates typically have a thick buried oxide. This thick oxide poses a significant thermal barrier. In particular, when considering the co-integration of lasers and electronics, efficient heat-sinking towards the substrate becomes an issue. Replacing the buried oxide with a more thermally conductive layer with similar optical properties would be required. Alternatively, etching heat pipes through the buried oxide could be considered.

In other cases the thermal conductivity of the substrate oxide is considered too high. For instance, when using local thermal tuning of a filter, the power consumption and the thermal crosstalk depend very much on the thermal leakage. One solution to this is undercutting the substrate (Dong *et al.*, 2010), effectively insulating the waveguide and its local BOX from the rest of the circuit. Depending on the choice of substrate and the widespread use of this technique on a chip, intrinsic stresses could start playing a role.

Active substrates: III–V on insulator

While silicon photonics enables most photonic functionalities, the most versatile material system for integrated photonics is still III–V semiconductors (GaAs-based up to 1300 nm, InP up to 1700 nm). In III–V materials passive waveguides, efficient modulators, detectors and efficient lasers have been demonstrated and even co-integrated on the same substrate (Schneider *et al.*, 2009; Nagarajan *et al.*, 2010).

However, to enable high-contrast photonics similar to the devices discussed here, a high vertical index contrast is required. Indium phosphide membranes on silicon use a stack similar to SOI, bonding a III–V wafer to a silicon substrate by using an adhesive BCB layer (Roelkens *et al.*, 2006). Passive circuits, as well as integration of active functions have been demonstrated using this approach. (van der Tol *et al.*, 2011).

The main limitation of this technology is that the basic III–V substrates are typically limited to 100 mm (4”) or 150 mm (6”) in diameter. Building 200 mm and 300 mm substrates based on this technology is therefore not straightforward.

13.6 Applications of silicon photonics

Historically, the main use of photonic integrated circuits is in optical communication, in transmitter/receiver circuits. In WDM systems this requires light source, wavelength multiplexers/demultiplexers, modulators, fiber-chip couplers and photodetectors.

Silicon photonics is a growing technology in this market. While the performance specifications for long-haul telecom backbones cannot yet be met with silicon PICs, shorter-range communication (metropolitan networks, fiber-to-the-home) and datacenter interconnects (rack-to-rack, board-to-board) consider silicon photonics a very attractive technology (Asghari, 2008).

Because of its shared technology base, silicon photonics is also becoming the prime candidate for on-chip optical interconnects. The dense integration of the high-contrast waveguide is an important asset, as the required footprint for a given data bandwidth is very small. Core-to-core on-chip networks could be powered with silicon photonic circuits, potentially even driven with on-chip lasers in a WDM configuration (Thourhout *et al.*, 2010).

But silicon photonics has more applications. Spectroscopy has already been mentioned in the section ‘Thermal substrates’. Wavelength demultiplexers can be used to break up a spectrum into wavelength channels. They can be combined with photodetectors and used as a spectrometer. Spectroscopy is often used to analyze the composition of substances. While communication typically used a wavelength band between 1300 nm and 1600 nm, spectroscopy could make use of much more spectral information.

But one of the most valuable future applications of silicon photonics could be in sensors. As discussed extensively in this chapter, silicon waveguides are extremely sensitive. While this is a drawback in building stable circuits, the sensitivity could also be put to use. Using an interferometer or a ring resonator, very small perturbations of the effective index can be measured. These changes can be used to measure temperature (Kim *et al.*, 2010) or strain (Taillaert *et al.*, 2007; Lee and Thillaigovindan, 2009), but the most interesting sensors can be built when there is no top cladding on the silicon waveguide. Because an exponentially decaying tail of the mode extends outside the core, changes in the top cladding will also be sensed. This can be useful for measuring refractive index variations in a watery medium (De Vos *et al.*, 2007; Washburn *et al.*, 2009). In addition, the silicon surface can be chemically modified to bind selectively to specific molecules, such as proteins or even DNA strands (Washburn *et al.*, 2010). In this way, many selective biosensors can be incorporated on the same chip for a parallel assay of multiple compounds (De Vos *et al.*, 2009; Qavi and Bailey, 2010; Washburn *et al.*, 2010).

13.7 Conclusion

In this chapter we discussed the use of silicon-on-insulator for integrated photonics. SOI provides a very attractive platform because of its high optical quality and very high refractive index contrast. It is possible to implement most optical functions in silicon, including waveguides, spectral filters, modulators and even photodetectors. Lasers remain very difficult.

Photonics poses different requirements on the substrate compared to electronics: a rather thick BOX and top silicon layer. But the most significant specification of silicon photonics is the uniformity: silicon waveguides are extremely sensitive to geometry variations and therefore need very accurate CD and thickness control.

We also covered a number of avenues to improve SOI for photonics, including multi-layer substrates, local SOI technology and even new materials made with the same technology. Silicon photonics is a technology that is rapidly gaining industrial relevance and much of its performance relies on the availability and quality of the right substrates. It could well be one of the next unique markets for silicon photonics.

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Silicon-on-insulator (SOI) technology for micro-electromechanical systems (MEMS) and nano-electromechanical systems (NEMS) sensors

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Abstract: This chapter discusses how to fabricate micro-electromechanical systems and nano-electromechanical systems (MEMS/NEMS) sensors with silicon-on-insulator (SOI) technologies. The chapter first reviews the operating principles of MEMS/NEMS sensors and how SOI wafers can help to simplify sensor design and manufacturing of the MEMS/NEMS. The chapter then discusses the design of sensor devices with detailed processing technologies, and provides some examples of the process flows for mass production of MEMS/NEMS sensors.

Key words: SOI, MEMS, NEMS, sensor, process flow.

14.1 Introduction

Micro-electromechanical systems (MEMS) and nano-electromechanical systems (NEMS) technologies are growing rapidly with a great potential to reshape our lives. MEMS/NEMS devices are fabricated using techniques such as:

- thin film deposition;
- photolithography;
- reactive ion etching (RIE);
- deep reactive ion etching (DRIE);
- wet etching; and
- vapor-phase etching.

Compared with advanced complementary metal oxide semiconductor (CMOS) devices, MEMS/NEMS devices use thin films which are much thicker with potential stress-related problems. MEMS/NEMS structures also have high aspect ratios and highly complex 3D shapes resulting from DRIE or from

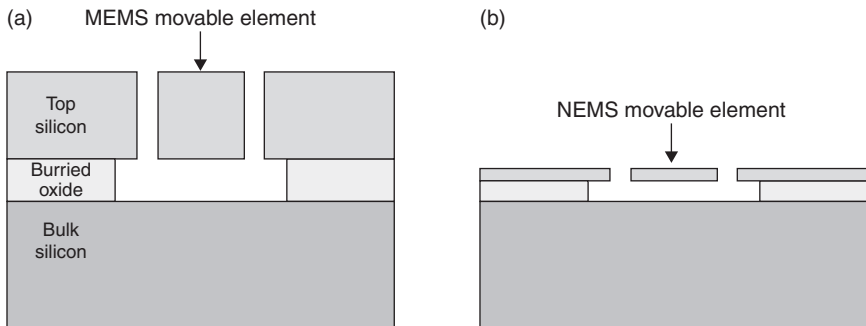
anisotropic wet etching and wafer bonding. These create new requirements for subsequent lithography, doping and thin film processes. While CMOS devices only deal with electrical signals, MEMS/NEMS devices need to convert and integrate a wide variety of signal types, such as physical (e.g., electrical, mechanical, thermal, optical), chemical and biological signals.

Silicon-on-insulator (SOI) technology was originally developed to avoid charge leakage in p/n junctions. However, due to the robustness of the single crystal device layer as a structural material for silicon microstructures,¹ SOI substrates are also attractive to MEMS and NEMS applications. With this technology, the mechanical structures of the device are formed in the upper silicon layer (Fig. 14.1a). As the SOI top layer is made from a single crystalline bulk wafer, it is a defect-free material with well-controlled doping levels for conductivity. This is a significant advantage compared to the limited thickness of polysilicon from surface micromachining of a bulk silicon wafer.²

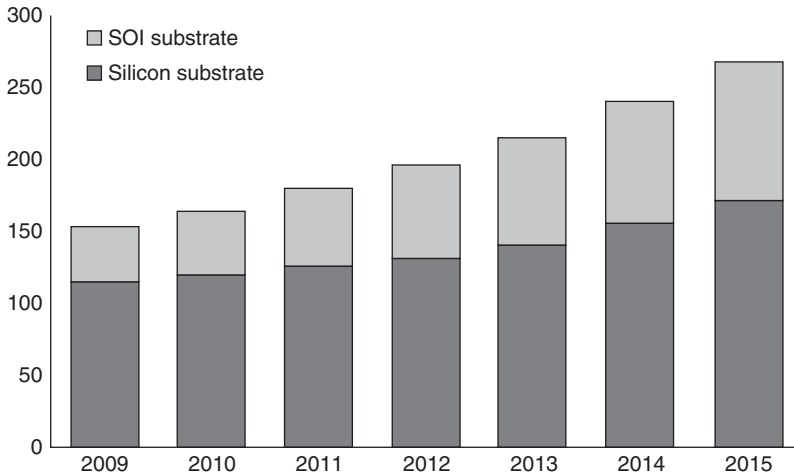
Furthermore, SOI substrates are commercially available and are becoming less expensive. More important, the features of SOI wafers can further simplify MEMS/NEMS design and manufacture. In cavity SOI, the SOI wafer has pre-etched cavities that enable MEMS manufacturers to focus on their core competencies, thus reducing development time, which in turn leads to lower production costs.³ The pre-etched SOI cavities, combined with dry etching, simplify the release of moving structures in the devices. By moving from micrometer size to nanometer size, the thin SOI substrate has helped to make the concept of producing NEMS a reality (Fig. 14.1b).

With these advantages, SOI technology has become more popular in MEMS production (Fig. 14.2). A study by Yole Development has shown that over five years the compound annual growth rate (CAGR) was 15.5% for SOI wafers compared to 8.1% for bulk silicon wafers.³

This chapter will present a brief review of the MEMS/NEMS principles of operation, the detailed design of the device, the key process technologies and some examples of fabrication process flows. With the limitation of



14.1 From (a) MEMS device to (b) NEMS device on SOI wafer.



14.2 Substrate market for MEMS. (Source: Yole Development.)

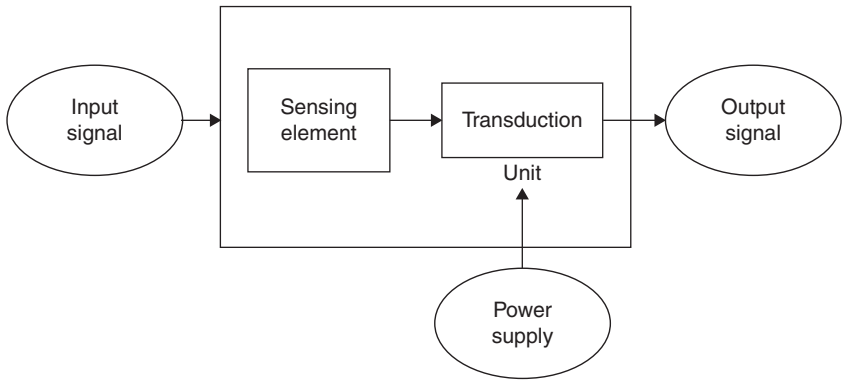
one chapter, only design and process technologies related to SOI substrates will be discussed. More details on other MEMS/NEMS technologies can be found in the articles listed in the references section.

14.2 SOI MEMS/NEMS device structures and principles of operation

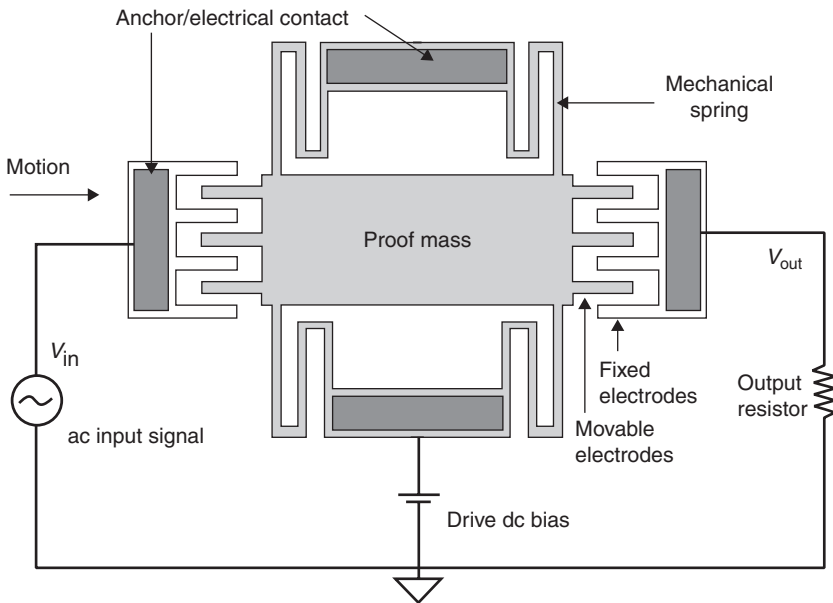
The MEMS/NEMS sensor device has two main components (see Fig. 14.3). One is the sensing element to respond to the incoming signal, the other is the transduction unit that converts the mechanical movement into the output electrical signal.

Figure 14.4 shows an example of the top view of a MEMS device. The springs allow the movable proof mass and electrodes to respond to the presence of an input signal. The movement of these movable structures changes the capacitance between movable and fixed electrodes. This capacitance change (ΔC) generates an output electrical signal.

A schematic diagram of a differential capacitive SOI accelerometer MEMS is shown in Fig. 14.5. The accelerometer consists of a proof mass that responds to any external acceleration in its sense direction. The tethers that act as mechanical springs suspend the proof mass, and the surrounding air imposes damping on the structure. The movement of the proof mass changes the capacitance between sense electrodes and proof mass fingers, and the interface circuit detects the minute changes of the capacitance. The accelerometers are designed so that mechanical stiffness is much greater than electrical stiffness. The transduction unit can either be based on a gap-change capacitance (Fig. 14.5a) or on an overlap-change capacitance (Fig. 14.5b).



14.3 Principles of operation of MEMS/NEMS devices.

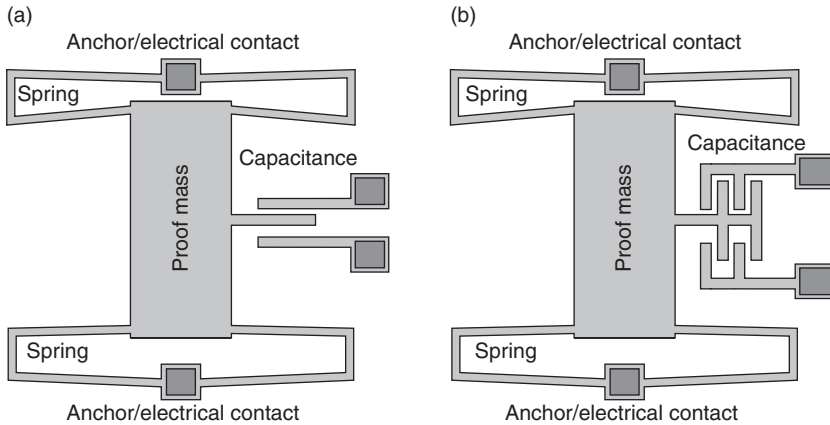


14.4 The structures and operation of a MEMS device.

In capacitive sensing devices, the capacitance between stationary and moving electrodes is:

$$C = \frac{\epsilon A}{d} \tag{14.1}$$

where ϵ is the dielectric constant, A is the area of the capacitor, and d , l , and h are the gap, length, and height of the electrode, respectively.



14.5 Basic elements of a MEMS accelerometer: (a) gap-change capacitance; (b) overlap-change capacitance.

The sensitivity of the device for a gap-change capacitance is therefore

$$\Delta C = \frac{\epsilon h}{d^2} \Delta d \tag{14.2}$$

and for an overlap-change capacitance:

$$\Delta C = \frac{\epsilon h}{d} \Delta l \tag{14.3}$$

The performance of the sensor is mainly determined by key parameters, which include the structure proof mass, spring constant, quality factor, resonant frequency, and Boltzmann noise.⁵

The relationship⁵ between resonant frequency (f_r), Boltzmann noise (B_{noise}), quality factor (Q), structure proof mass (M), and spring constant (k) is given by the following equations:

$$f_r = \frac{1}{2\pi} \sqrt{\frac{k}{M}} \tag{14.4}$$

$$B_{\text{noise}} = \sqrt{\frac{8\pi K_B T f_r B}{QM}}; \quad B < f_r \tag{14.5}$$

where K_B =Boltzmann constant, T =temperature, B =bandwidth, and Q = quality factor.

In a SOI MEMS/NEMS device, the thickness of the top silicon layer defines h , the height, in Equations [14.1]–[14.3]. The length, l , and gap, d , of

the electrodes are carefully chosen for both high operational performance and also highest possible production yield.

14.3 SOI MEMS/NEMS design

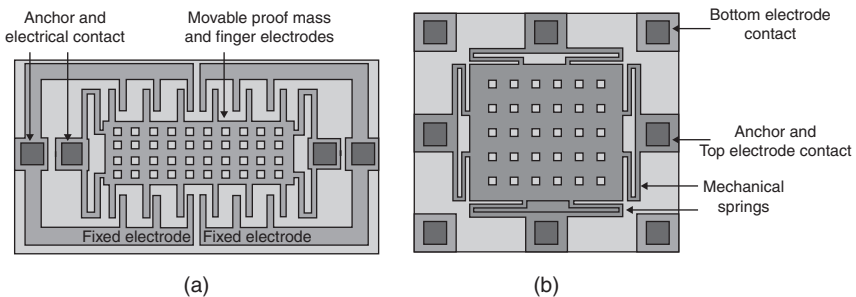
Understanding the principles of operation and the required device parameters, a designer can utilize SOI technologies to design a high performance device with the available process equipment.

Although there are many different MEMS/NEMS devices for different applications, many of them share the same process design for fabrication. An example is shown in Fig. 14.6, which shows that the same design of a capacitance sensing structure can be used in many devices.

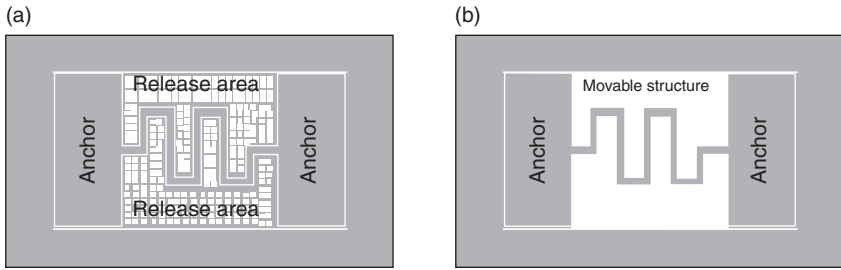
The system-determined capacitance and process-determined gap set the required mechanical spring constant. Another design consideration is that electrical current must flow through the springs to the electrodes, making the springs the dominant source of series resistance. Because of this, the geometrical dimensions of the springs can be optimized to provide the least electrical resistance for a particular spring constant.⁵ Therefore, an optimal solution is to make the spring beams short, thick, and wide, but within the constraint of the spring constant. The resistance can also be kept to a minimum by depositing a highly conductive metal on top of the highly doped silicon layer.⁵

There are two typical types of MEMS/NEMS structure: Fig. 14.6a shows an in-plane (IP) structure; an out-of-plane (OOP) structure is shown in Fig. 14.6b. The movable element in an IP structure moves in a planar direction, while that in an OOP structure moves vertically.⁶⁻⁸ The structures have a released area where the top silicon is to be removed, and anchors to hold the movable element. The surface areas of each region are carefully designed to work with the later etching processes.⁹

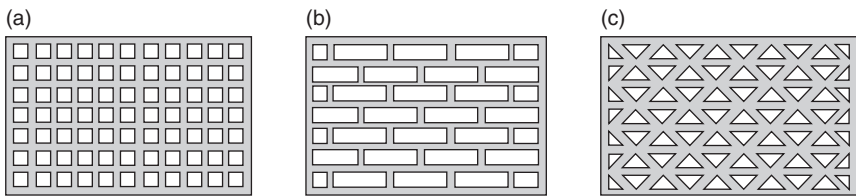
In order to release the structures via etching through the top silicon layer and buried oxide etch, the large exposed area is filled with release



14.6 Basic structure of a MEMS device: (a) in-plane (IP) and (b) out-of-plane (OOP) elements.



14.7 Device layout: (a) top view at design step and (b) final structure after releasing processes.



14.8 (a–c) Three typical layout designs of large released structures.

structure. The release structure is an area of silicon populated with a matrix of release holes and is isolated from other design features by a perimeter trench. Figure 14.7a shows the layout of a typical structure pattern, and Fig. 14.7b shows the structure after pattern processing. The released structure that connects to the anchor forms the moving element, whereas released structures that do not connect to any anchor are etched away. To form released structures, square holes (Fig. 14.8a), rectangular holes (Fig. 14.8b), triangular holes (Fig. 14.8c), or other types of layout are used.⁹

With SOI wafers, the most straightforward method is to define the structure by DRIE from the top silicon layer, followed by sacrificial wet etching of the buried oxide layer with hydrofluoric acid (HF) solutions. However, due to the stiction problem caused by wet etching, which will affect process yield, the HF vapor process is preferred and is widely used to etch the buried oxide layer to release the moving parts of the device.

14.4 SOI MEMS/NEMS processing technologies

Although most of MEMS/NEMS fabrication processes are CMOS compatible, there are many different processing challenges. Cavity forming, deep reactive ion etching, notching effect control, vapor-phase etching, and anti-

stiction coating are the key technologies that have high impact on the success of MEMS/NEMS production.

14.4.1 Cavity SOI wafer

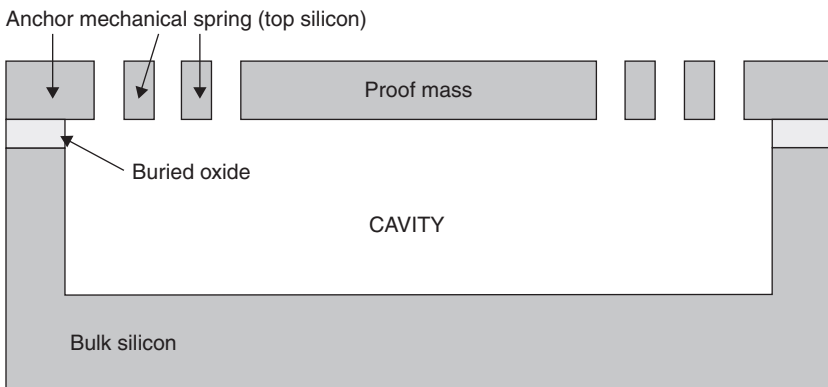
Wafers that have bonded substrates with pre-etched cavities¹² provide freedom in the design of MEMS/NEMS structures and remove some of the restrictions of using SOI for micro/nano systems (Fig. 14.9).

The fabrication of the cavity starts with a silicon wafer which is thermally oxidized. The next step is the patterning and etching of oxide on both sides (alignment marks are on the back side and cavities are on the front side). Then, this bulk silicon wafer is bonded to the cap wafer, followed by grinding and polishing down to a required top Si layer thickness.¹² The process flow of a pre-etched cavity SOI is shown in Fig. 14.10. Note that once the cavity lithography and etch processes are completed, the front side oxide layer can be removed with HF etching, and the wafer can be bonded to a cap wafer with bottom oxide layer, as shown in Fig. 14.10d.

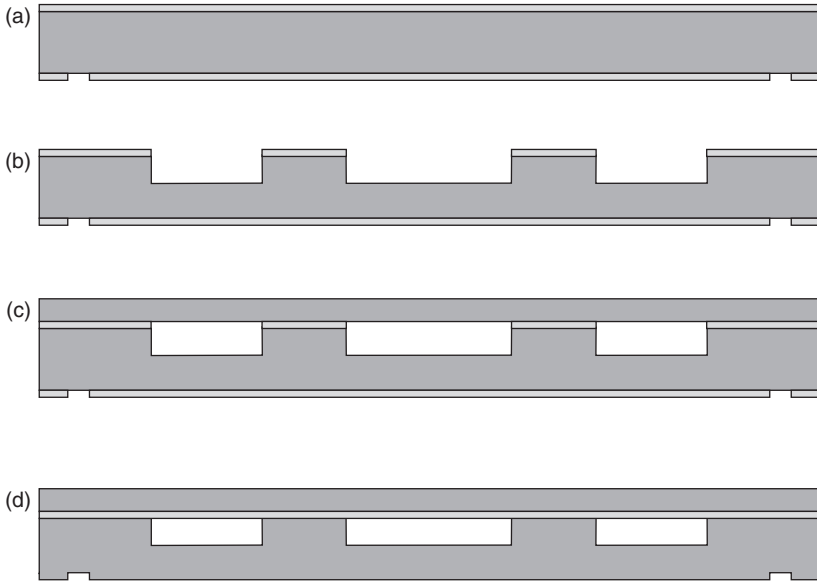
In pre-etched SOI wafers, the cavity dimensions are well-defined because they are lithographically patterned prior to bonding. Moreover, the parasitic capacitance between the device layer and the substrate can be decreased far below what is achievable with a buried oxide layer in conventional SOI wafers if deep cavities and small bonding areas are prepared on a wafer. Thus, pre-etched SOI wafers are a suitable platform for vertically and horizontally moving structures in various applications.

14.4.2 Deep reactive ion etching

The deep reactive ion etching (DRIE) technique invented by Robert Bosch (US patents #5498312 and #5501893 in 1996) is the most popular method



14.9 Cross-section view of a typical cavity SOI MEMS structure.



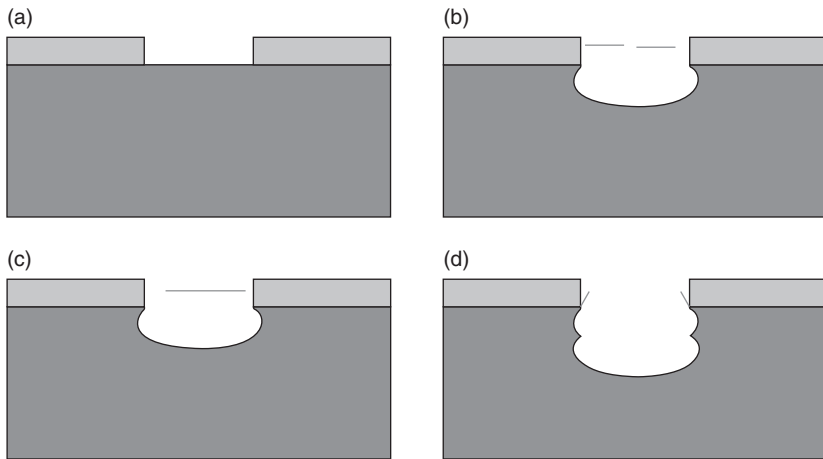
14.10 A typical process flow for SOI substrates with pre-etched cavities: (a) after oxidation and back side alignment marks patterning; (b) after front side cavity patterning; (c) after bonding to the cap wafer and thinning to the desired top silicon thickness; (d) the SOI wafer with oxide at bottom of cap wafer.

of defining the structures in present day MEMS/NEMS devices.^{13–15} The DRIE technique is the key step in etching the thick layer. In this process, the masking material and thickness are carefully selected for the required etch depth. A design of experiment (DOE) needs to be done for each item of process equipment to develop the DRIE recipe for the selected sidewall polymer deposition, etch rate uniformity, minimum loading effects, and lowest notching effects. The under-mask, lateral direction etching (under cut) must be well controlled. The DRIE process control parameters and their main effects are shown in Table 14.1.

The DRIE principle (Bosch process) is shown schematically in Fig. 14.11. First, a single short (5–15 s) etching step is applied to the patterned silicon substrate in fluorine-containing plasma, as shown in Fig. 14.11a and 14.11b, and the exposed silicon is etched in an isotropic manner. Then the process switches to a polymerization step (7–20 s) and a polymer layer is deposited on the exposed silicon surface, as shown in Fig. 14.11c. In the following etching step, the polymer layer at the bottom of the structure is rapidly removed by ion bombardment and the etchant continues to react with the exposed silicon. Conversely, as shown in Fig. 14.11d, the polymer layer on the sidewall is consumed very slowly due to lack of ion incidence, and therefore protects the sidewall silicon from being etched. By alternating between the etching step and

Table 14.1 DRIE process parameters and their effects

DRIE process parameter	Main effect
Pressure	Uniformity, etch rate, selectivity, etch profile
Platen power	Profile, etch rate, selectivity
Coil power	No effect in 500–900 W range
SF ₆ flow	Mask under cut, etch rate
C ₄ F ₈ flow	Mask under cut, etch profile
SF ₆ time	Etch profile, mask under cut, etch rate
C ₄ F ₈ time	Etch profile, mask under cut
Exposed Si area	Etch rate, etch uniformity



14.11 A schematic of the Bosch (DRIE) process: (a) patterned silicon substrate; (b) etching; (c) polymer deposition; (d) next etching.

the polymerization step, the depth of the structure increases gradually without further lateral etching underneath the mask layer. Although the single etching step is isotropic, the combination of etching and polymerization results in good anisotropy. As a result of the high chemical activity of the fluorine radicals in the plasma, low energy ion bombardment occurs under the usual configuration, and sidewall protection is provided by the deposited polymer.

Sidewall passivation

The sidewall passivation layer can be deposited via one of the following sources:¹⁶

1. Plasma polymerization can be achieved by the generation of (CF₂)_n-type radicals in the plasma starting from precursor gases like trifluoromethane (CHF₃).

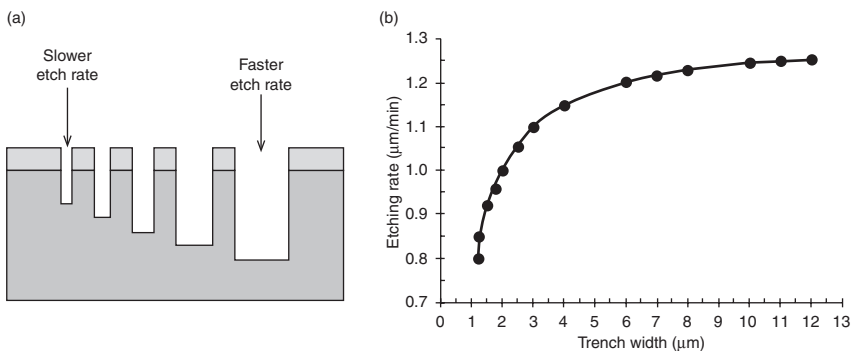
- Hexafluoropropene (C_3F_6) or octafluorocyclobutane (RC318, C_4F_8) is preferred to a nontoxic and stable dimer of tetrafluoroethylene (TFE, C_2F_4).
- Sidewall passivation can also be achieved by the addition of O_2 to the etch cycle.

The number of etch/polymer deposit cycles and the time per cycle determine the sidewall roughness of the etched structure. More cycles and a shorter time give a smoother sidewall but at the cost of slow total DRIE processing time. Also, for an etched trench width less than $10\ \mu\text{m}$, the smaller trench width has a slower DRIE etching rate, as shown in Fig. 14.12.

Sidewall roughness, as shown in Fig. 14.11d, is a concern in the DRIE process. This roughness can be reduced by decreasing passivation cycle time, reducing pressure, and reducing platen power during the passivation step.

DRIE masks

A photoresist is the primary material for etch masking. However, to form a deep trench with dry etching, the full thickness of the photoresist mask layer may be etched away before the full depth of the trench is etched. To solve this problem, an additional masking layer is deposited prior to photoresist coating and patterning. The additional materials for masking include: silicon nitride (Si_3N_4) as a mask for silicon (Si) and oxide (SiO_2) etching, and oxide as a mask for silicon and silicon nitride etching. The selective etch rate of photoresist and other masking material to the etched depends on the gas chemicals, and also on what type of DRIE equipment is used. The etch selectivity must be studied before determining the mask material and its thickness for DRIE processing.



14.12 The dependence of DRIE etching rate on the trench size: (a) etched trench depth; (b) etching rate vs trench width.

Loading effects

The loading effects of the DRIE process^{13–15} include:

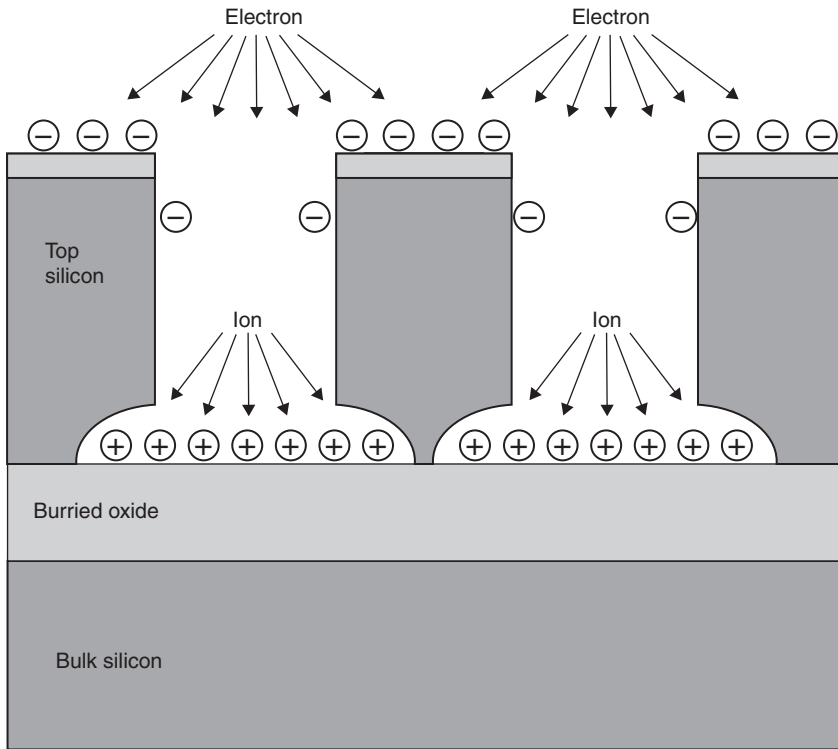
- *Macroscopic loading effect:* the DRIE etch rate throughout the reactor decreases as more area of the etchable material is added to the reactor. Higher etch gas flow to the etch chamber can help to minimize this effect.
- *Microscopic loading effect:* features of the same size etch more slowly in dense patterns than in sparse patterns. This effect is attributed to localized depletion of the etching process itself.
- *Aspect ratio dependent etch rate:* high aspect ratio features etch more slowly than low aspect ratio features. The etch rate decreases with feature size (Fig. 14.12). This is due to the difficulty faced by the etch species in traveling through smaller openings. Low pressure in the etch chamber can help to minimize this effect.

The DRIE or Bosch process and SOI wafers are well established technologies for the manufacture of high aspect ratio MEMS devices. By using only one mask, the structure can be formed by DRIE. However, the notching at the silicon and buried oxide interface must be considered and kept well under control.

Notching effect on SOI wafers

Plasma etching of the silicon over the insulator layer has long been known to cause a silicon notching problem at the silicon/insulator interface. This is because of charging on the insulator layer regardless of the geometry of the etched structures or their functionality. The poor profile contributed by the notching may result in resonant frequency variations in the microstructure, leading to degraded performance. As this undercutting is dependent on aspect ratio, the profiles and the characteristics of the final devices may further vary across the wafer, affecting repeatability and reliability, especially for thick device wafers.^{13–15}

The notching phenomenon is caused by electron charging effects. Increased electron shadowing at high aspect ratios reduces the electron current to the trench bottom. To reach a new charging steady state, the bottom potential must increase, significantly perturbing the local ion dynamics in the trench. The deflected ions bombard the sidewall with larger energies, resulting in severe notching, as can be seen in Fig. 14.13. The depth of the notching depends on many factors, such as the over-etching time, the material type, the thickness of the sidewall passivation, and the size of the feature. Other parameters include electron temperature, ion energy, and the ion/electron current at the surface.



14.13 Schematic of notching effects on SOI wafer.

The notching effect can be reduced by using a MEMS/NEMS design with minimum variation in trench width, together with a pulsed high/low frequency (HF/LF) platen power, an end-point detection system, and a two-step etch process with soft landing on the buried oxide. Although notching effects from the DRIE process can be utilized to form the released structure, a deep etch without notching followed by vapor-phase HF buried oxide etching is the better choice for uniform beam release and minimization of the stiction problem.

14.4.3 Vapor-phase etching

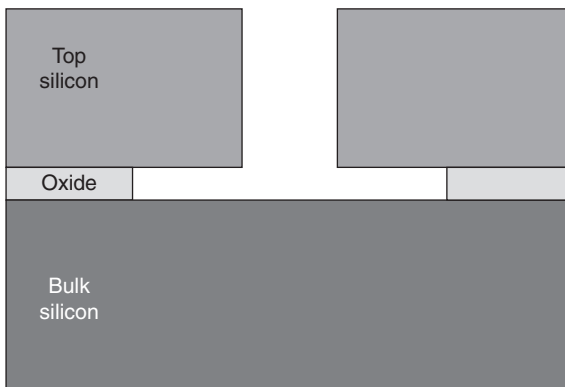
The notion of removing a sacrificial layer with vapor-phase etching (VPE) is very attractive in that it replaces the whole sequence of etching, rinsing, and an elaborate drying procedure. In addition, no meniscus is formed during the releasing procedure.¹⁷ The removal of sacrificial oxide with HF vapor has been tested by researchers for many years for the release of polysilicon structures. The best reported result has been obtained by heating the wafer during HF

vapor etching and preventing excessive water condensation.¹⁷ The advantage of this VPE process for micromachining lies in its ability to obtain free-standing compliant microstructures without stiction problems (Fig. 14.14) and in simplifying the process significantly by removing the need for repeated rinsing and drying steps. The releasing of microstructures with VPE completely removes the use of liquid throughout the release procedure.

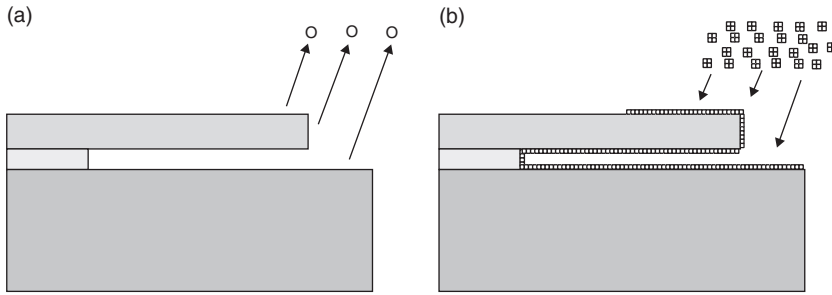
14.4.4 Anti-stiction coating

The stiction caused by a wet etch can be avoided with VPE, but during device operation stiction occurs when surface adhesion forces are higher than the mechanical restoring force of the micro/nano structures. Other factors such as surface roughness, relative humidity, and temperature also impose additional challenges in controlling surface forces.¹⁸ Although there are a wide variety of anti-stiction precursors available, the methods used to deposit them onto microstructures and other substrates follow similar steps. Typically, they include two steps: the pre-bake at 120°C for 2–3 min (Fig. 14.15a) to release the moisture trapped in small gaps between structures; and molecular vapor deposition at 120–160°C (Fig. 14.15b) to seal the structures to prevent future stiction. Fluorooctyltriethoxysilane (FOTES) and fluorooctyltrichlorosilane (FOTS) are popular anti-stiction coating materials.¹⁸ With a high temperature at the deposit step, the liquid anti-stiction material evaporates and is deposited onto all surfaces of the structures in the device.

The combination of VPE and anti-stiction coating processes provides high production yields in the manufacturing line, and also ensures that devices operate with high reliability.



14.14 Cross-section view of structure of SOI wafer after DRIE and vapor HF etching.



14.15 Schematic of anti-stiction coating: (a) pre-bake and (b) molecular vapor deposition.

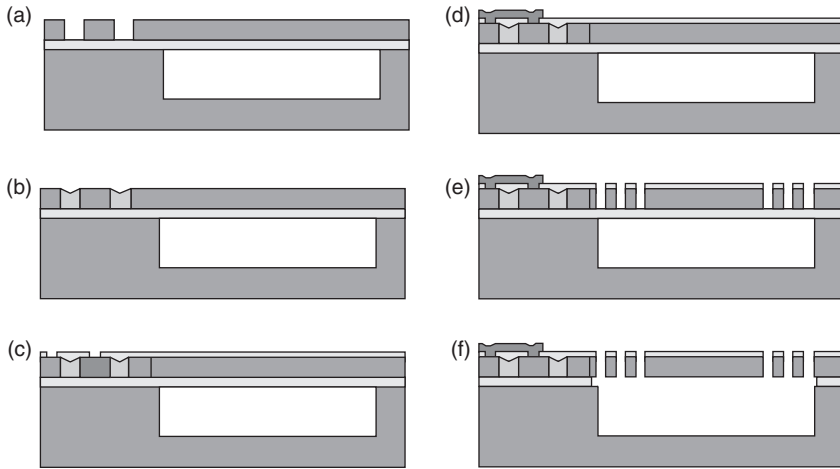
14.5 SOI MEMS/NEMS fabrication

MEMS/NEMS designers used to develop their own process flows, but MEMS/NEMS manufacturers have started to set up a standard process platform that will work with more devices, reduce manufacturing costs, and introduce new products more quickly. In this section, two typical process flows are described for the process platforms for SOI MEMS and NEMS devices.^{19–21}

14.5.1 MEMS fabricated with pre-etch cavity SOI wafer

In the fabrication flow chart shown in Fig. 14.16, the process starts with a pre-etched cavity SOI substrate. A wide range of top silicon layer thicknesses (1–50 μm) is available for different device requirements, as are those of the buried oxide depending on the choice of the designer. The key process steps are as follows:

1. Isolation trench: lithography and DRIE are used to form the isolation trench (Fig. 14.16a).
2. Isolation filling: a low-pressure chemical vapor deposition (LPCVD) process to fill the trench with silicon nitride (Si_3N_4) material, and DRIE of the wafer top to clear Si_3N_4 material from the top silicon surface (Fig. 14.16b).
3. Interlayer/contact: a sputtering process to deposit a 0.2 μm Al_2O_3 film, followed by lithography and etch to open the contact area (Fig. 14.16c).
4. Metallization: a sputtering process to deposit a 0.7 μm aluminum layer, with lithography and dry etch for metal patterning (Fig. 14.16d).
5. MEMS pattern: lithography to define the pattern and DRIE to etch through the top silicon layer (Fig. 14.16e). The gap between silicon fingers determines the sensing capacitance.



14.16 (a–f) The process flow to fabricate a SOI MEMS accelerometer.

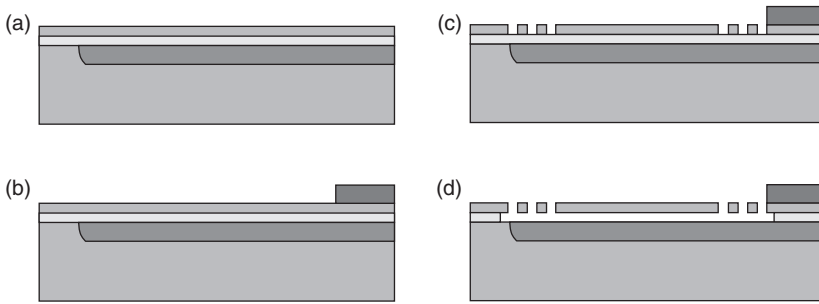
6. Structures release: a vapor-phase HF etch process to etch oxide underneath the top silicon layer in order to release the structure (Fig. 14.16f).

14.5.2 NEMS fabricated with thin SOI wafer

The main processing steps for a NEMS device are summarized in Fig. 14.17. The NEMS structure is formed in the thin top silicon layer (100–200 nm thickness) of SOI wafer, and the buried oxide is also of nanometer dimension or regime (200–400 nm thickness). The device, which in this example has the NEMS OOP capacitance structure, is fabricated through these process steps:

1. Bottom plate doping: high energy (300–400 keV) implantation followed by an annealing step to form the lower electrodes of the device (Fig. 14.17a).
2. Metallization: a sputtering process to deposit a 0.7 μm aluminum layer, with lithography and dry etch for metal patterning (Fig. 14.17b).
3. NEMS pattern: lithography and DRIE to form the structure of the device (Fig. 14.17c).
4. Structures release: vapor-phase HF etching is used to etch the buried oxide underneath the moving structures (Fig. 14.17d).

Careful extra work is required to pattern both nanostructures (spring, electrostatic combs, etc.) and large structures (proof mass, electrical pads, etc.) in a single process step. To meet this challenge, 248 nm deep ultraviolet (DUV) lithography can be used. In addition, the HF vapor technique has been improved to enable the release and protection against sticking despite



14.17 (a–d) The process flow to fabricate a SOI NEMS device.

the 500 nm diameter of the release holes and the 400 nm thickness of the sacrificial oxide.

14.6 Conclusion

The main advantage of using SOI technology enables a greater freedom of design. The technology was developed to manufacture high performance MEMS/NEMS sensors. SOI wafers can further simplify the MEMS design and the process flow for manufacturing. This shortens the time from idea to mass production. The advantages of the SOI-based solutions for MEMS/NEMS sensors include the need for the smallest possible package, very tight control and precision of the structure, the ability to withstand high pressure and temperature, a long product lifetime, and the smallest possible die size and reduced cost.

Additional features in SOI wafers include pre-etched cavity SOI, in which the SOI wafer has pre-etched cavities that enable MEMS manufacturers to focus on their core competencies by reducing development time, which in turn can even lower production costs. Some MEMS manufacturers have found that pre-etched SOI cavities combined with dry etching simplifies the release of the devices. Vapor-phase etch technology is working well with SOI wafers to replace the wet etch, creating the advantage of avoiding the stiction problem.

There has been concern regarding the high cost of SOI wafers (compared to bulk silicon wafers). However, with its advantages, SOI technology is the right choice for reducing the total device cost and saving time in new product development. Overall, SOI substrates are providing many advantages for MEMS/NEMS production, and they enable increased integration flexibility with mainstream CMOS logic devices.

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