

SRINIVAS SIRIPURAPU

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Work experience

Synopsys, India

Oct 2011 — March 2012

Intern (Technical)

Responsibilities and work:

- Trained on AMBA Verification IPs, Designware library IPs.
- Customer support for Synopsys Designware AMBA IP and VIP Library.

Education

PhD

Dec 2013 — Present

Indian Institute of Technology, Madras

Working thesis :

"Physical Design methodology and tools for NoC based SoC".

The current physical design tools are based on standard cells and/or macros design flow. As the complexity of the design increases routing congestion problem significantly delays the project by months. The problem of global wiring congestion can be avoided by using Network-on-Chip concepts for complex SoCs [Ref : "The Critical Cost of Routing Congestion" by Jonah Probell, Senior Solutions Architect, Arteris].

The individual chiplets/modules/IP cores can be synthesized by current tools and methodologies, but at top level all these modules need to be assemble within NoC framework. Thus the need for NoC aware physical design tools is inevitable.

[Ref: "21st Century Digital Design Tools" by Dally, W. J et.al]

Course Work :

- DSP Architectures and Embedded Systems (EE5030)
- Analog Integrated Circuit Design(EE5390)
- Hardware-Software Co-design(EE7030)
- Digital Integrated Circuit Design(EC5134)
- VLSI Technology(EC5133)

Projects:

- **Channel Estimation and Correction module in OFDM MODEM**
 - Implemented Channel Estimation and Correction module in verilog for Virtex-7 FPGA.
"Fixed-point C code specification to Verilog RTL". This module is part of OFDM Receiver designed for Defence Electronics Application Laboratory (DEAL), Ministry of Defence, Govt. of India as consultancy project at IIT Madras.
- **Two Stage Operational Amplifier**
 - Designed Two stage Operational Amplifier with Common mode feedback and simulated using hspice. Analog IC design course project.

Course Work:

- Digital VLSI Design
- Computer Architecture
- Introduction to software engineering for Electronic students
- Design for Testability
- Standard Cell and Memory IC Design
- Low power cmos design.

Projects:

- **NAND flash controller with AMBA-AHB interface**
 - Designed NAND flash controller with AMBA-AHB interface in Verilog HDL, final project, MS 2012.
- **8x8 SRAM**
 - Designed an 8x8 SRAM using Custom Designer, and simulated using hspice; and vcs & nanosim, mini project, MS 3rd semester, 2012.
- **Low power design techniques on an open core**
 - Incorporated low power design techniques on an open core(SDM router), using Unified Power Format (UPF) and Synopsys' MV tools, mini project, MS summer program,2011.
- **32-bit Up-Down Counter – RTL-to-GDSII**
 - 32-bit Up-Down Counter – RTL-to-GDSII (no DFT) using Synopsys tools, mini project, MS 2nd semester, 2011.
- **4-bit DAC**
 - 4-bit DAC, Charge redistribution architecture implemented and simulated using CustomDesigner and hspice, mini project, MS 2nd semester, 2011.
- **Translation LookAside buffer(TLB)**
 - Translation LookAside buffer(TLB) for 32-bit addressing in Verilog and C, mini project, MS 1st semester, 2011.
- **AMBA – AXI4 interconnect**
 - Designed AMBA – AXI4 interconnect for two masters and two slaves in SystemVerilog, mini project, MS 1st semester, 2011.

- **Demo Assembler**
 - Demo Assembler for 8051 instruction subset written in perl, mini project, MS 1st semester, 2011.

BTech (Electronics & Computers Engineering)

Course Work:

- Software engineering.
- Relational Databases Management Systems.
- Operating systems.
- Digital Systems Design.
- VLSI
- Digital Signal Processing.
- Analog Circuits.

Projects:

- 8-bit microcontroller in VHDL “Designed a 8-bit microcontroller in VHDL”, project, BTech 8th semester, 2010.
- “Most Wanted”, Small game developed in C, mini project, BTech 4th semester,2008.
- “Line Follower Robot”, mini project, BTech 6th semester, 2009.
- “Coding strategies for improving performance in FPGAs”, term paper, BTech 7th semester, 2009.

Skills & Abilities

Hardware and EDA

- Hardware languages: Verilog, Systemverilog, Bluespec SV.
- Verification: VMM
- Tools Exposed to/Working with: VCS, Design Compiler, IC Compiler, RTL Compiler, SoC Encounter.
- Custom Designer, hspice, nanosim.
- Unified Power Format (UPF) for Low power designs.
- FPGAs: Spartan3e,Virtex-5,Virtex-6

SOFTWARE

- Programming languages: C, C++, assembly - 8086, and java(Core).
- Scripting: perl,python,tcl.
- Operating systems: Windows and Linux.
- Tools Exposed to/Worked with: Rational Rose, Netbeans IDE.

Embedded Systems

- Programming languages: EmbeddedC, assembly – 8051.
- Platforms Exposed to/Worked with: Cypress PSoC (3 & 5),8051

Scholastic Achievements

- Won 2 medals for securing more than 95% marks in Math and Science in X standard.
- 1st rank holder during MS,2010-12.
- Secured 48th RANK in NET-CSIR-JRF Dec 2012 in Engineering Sciences.

References

References available upon request.