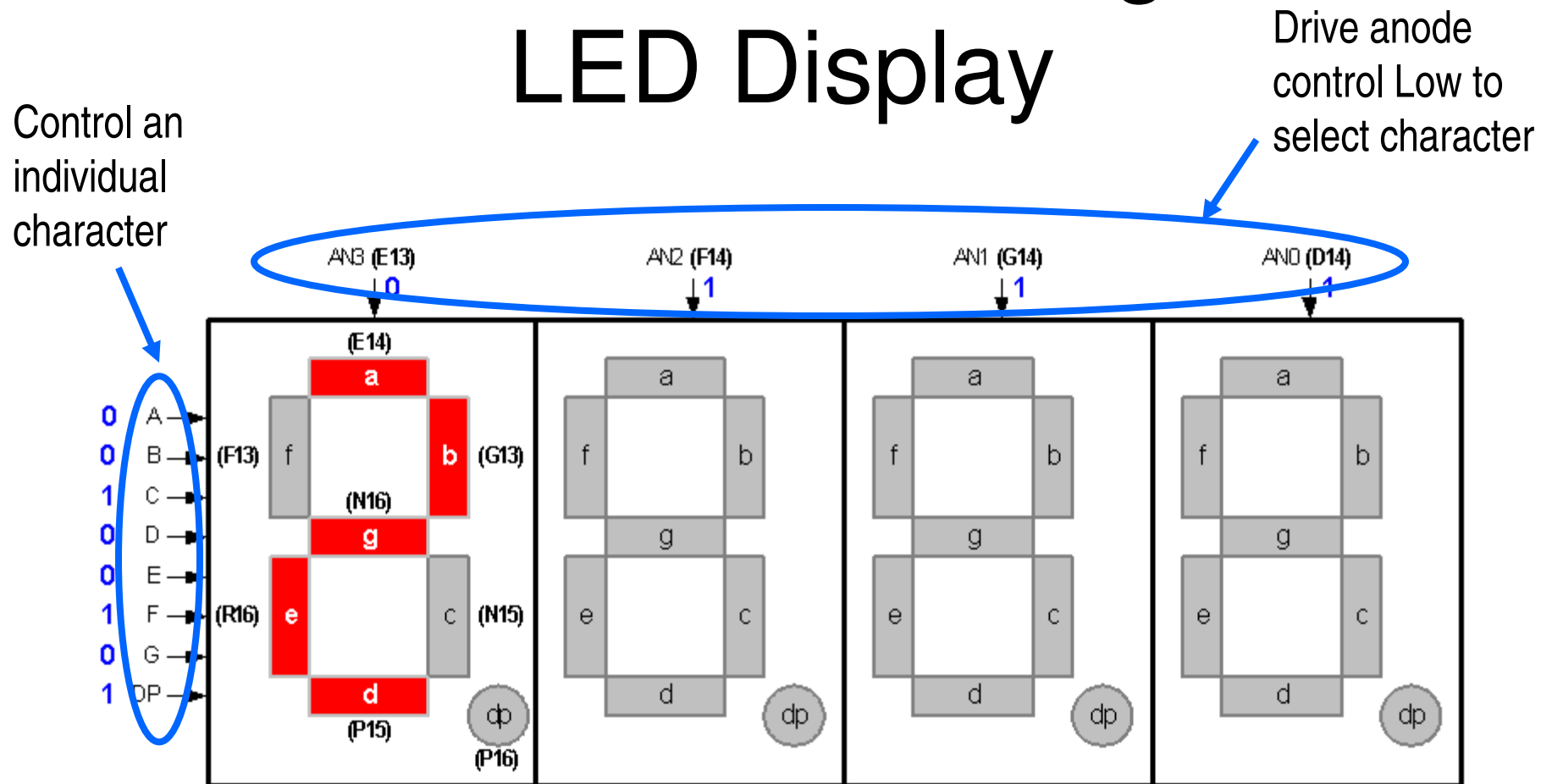


DIGITAL CLOCK for Spartan-3 Starter Board

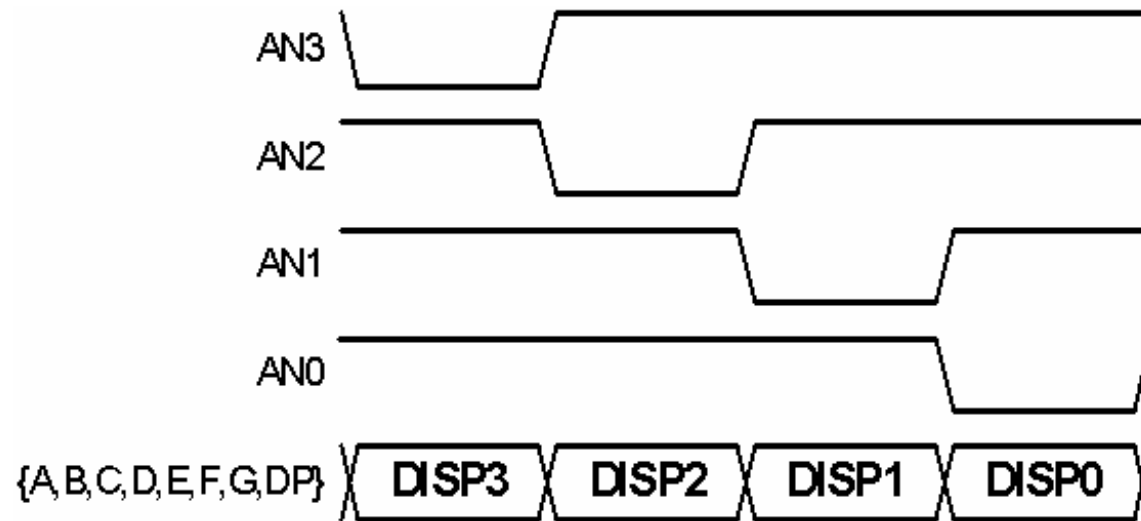
- This design shows how to generate a digital clock and display the output to the multiplexed 7-segment display in VHDL.
- Files for design.....
 - Top level design file
 - clock.vhd
 - Timing and pin out constraints file
 - clock.ucf
 - Documentation
 - readme.pdf

Four-Character, 7-Segment LED Display



- 8 control lines light a specific segment on LED
- 4 anode control lines define which character responds

Multiplexed Display



- Standard approach: 4 characters = 32 I/O pins

Advantage	Disadvantage
Saves 20 pins	Requires that FPGA logic constantly scans characters