MICROELECTRONICS CIRCUITS
Subject Code: 10EC63
VI semester ECE

References:

Text Book:
1. "Microelectronic Circuits", Adel Sedra and K.C. Smith, 5th Edition, Oxford University Press, International Version, 2009.

Reference Book:
1. "**Fundamentals of Microelectronics" , Behzad Razavi, John Wiley India** Pvt. Ltd, 2008.
2. "Microelectronics – Analysis and Design", Sundaram Natarajan, Tata McGraw-Hill, 2007

Material Prepared by

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RNSIT,
Bangalore

MODIFIED SYLLABUS

B.E. Electronics & Communication Engineering (2010-11Scheme)

Modified Syllabus (VI Semester)

MICROELECTRONICS CIRCUITS

Subject Code	: **10EC63**	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART A

UNIT – 1

MOSFETS: Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, Biasing in MOS amplifier Circuits, Small Signal Operation and Models, MOSFET as an amplifier and as a switch, biasing in MOS amplifier circuits, small signal operation modes, single stage MOS amplifiers. SPICE MOSFET Examples. **8 Hrs**

UNIT -2

Single Stage IC Amplifier: IC Design philiosophy, CoUmparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response. 5 **Hrs**

UNIT – 3

Single Stage IC amplifiers (continued): CS and CF amplifiers with loads, high frequency response of CS and CF amplifiers, CG and CB amplifiers with active loads, high frequency response of CG and CB amplifiers, Cascade amplifiers. CS and CE amplifiers with source (emitter) degeneration source and emitter followers, some useful transfer parings, current mirrors with improved performance. SPICE examples. **7 Hrs**

UNIT – 4

Differences and Multistage Amplifiers: The MOS differential pair, small signal operation of MOS differential pair, the BJT differences pair, other non-ideal characteristics and differential pair, Differential amplifier with active loads, frequency response and differential amplifiers. Multistage amplifier. SPICE examples. **8 Hrs**

PART B

UNIT – 5

Feedback. General Feedback structure. Properties of negative feedback. Four basic feedback topologies. Series-Shunt feedback. Determining the loop gain. Stability problem. Effect of feedback an amplifier poles. Stability study using Bode plots. Frequency compensation. SPICE examples. **8 Hrs**

UNIT - 6

Operational Amplifiers: Ideal Op-amp, Inverting Configuration, Non-inverting Configuration, Difference Amplifiers, Open-Loop Gain & BW on Circuit Perforamnce, Large signal peration of Op-Amps, DC Imperfections, Integratior & Differentiatiors, Non-linear Function Oprations, Sample and Hold Circuit, The SPICE Eamples. **9 Hrs**

UNIT – 7

Digital CMOS circuits. Overview. Design and performance analysis of CMOS inverter. Logic Gate Circuits. Pass-transistor logic. Dynamic Logic Circuits. SPICE examples. **7 Hrs**

Text Book:

1. **"Microelectronic Circuits",** Adel Sedra and K.C. Smith, 5th Edition, Oxford University Press, Interantional Version, 2009.

Reference Book:

1. **"Fundamentals of Microelectronics"** , Behzad Razavi, John Wiley India Pvt. Ltd, 2008.
2. **"Microelectronics – Analysis and Design"**, Sundaram Natarajan, Tata McGraw-Hill, 2007

Note : Unit1, Unit 2, Unit3 & Unit 4 - Can be of 5 questions.
Unit 5, Unit 6, & Unit 7 - Can be of 3 questions.

Unit 1 – Chapter 4
MOS Field-Effect Transistors (MOSFETs)

UNIT 1 OUTLINE

1.1 Device Structure and Physical Operation
1.2 Current – Voltage Characteristics
1.3 MOSFET Circuits at DC
1.4 Biasing in MOS amplifier circuits
1.5 Small Signal Operation and Models
1.6 The MOSFET as an Amplifier and as a Switch
1.7 Single Stage MOS amplifiers
1.8 SPICE MOSFET models and examples

LEARNING OUTCOMES:
At the end of this chapter one can clearly get to know the following:

- **Understanding Physical construction and operation of an Enhancement MOSFET**
- **Drawing the V-I characteristics of n and p channel E-MOSFET**
- **DC operation or biasing of MOSFETs**
- **AC Operation: Small signal modeling of MOSFETs**
- **Single stage MOS amplifiers : Common Source, Common Drain and Common Gate amplifiers**
- **SPICE modeling of MOSFETs**

INTRODUCTION

Along with the Junction Field Effect Transistor (JFET), there is another type of Field Effect Transistor available whose Gate input is electrically insulated from the main current carrying channel and is therefore called an **Insulated Gate Field Effect Transistor** or **IGFET**. The most common type of insulated gate FET which is used in many different types of electronic circuits is called the **Metal Oxide Semiconductor Field Effect Transistor** or **MOSFET** for short.

The **IGFET** or **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a "Metal Oxide" Gate electrode which is electrically insulated from the main semiconductor N-channel or P-channel by a thin layer of insulating material usually silicon dioxide (commonly known as glass). This insulated metal gate electrode can be thought of as one plate of a capacitor. The isolation of the controlling Gate makes the input resistance of the **MOSFET** extremely high in the Mega-ohms (MΩ) region thereby making it almost infinite.

As the Gate terminal is isolated from the main current carrying channel "NO current flows into the gate" and just like the JFET, the **MOSFET** also acts like a voltage controlled resistor were the current flowing through the main channel between the Drain and Source is proportional to the input voltage. Also like the JFET, this very high input resistance can easily accumulate large amounts of static charge resulting in the **MOSFET** becoming easily damaged unless carefully handled or protected.

MOSFETs are three terminal devices with a Gate, Drain and Source and both P-channel (PMOS) and N-channel (NMOS) MOSFETs are available. The main difference this time is that MOSFETs are available in two basic forms:

1. **Depletion Type** - the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device "OFF". The depletion mode MOSFET is equivalent to a "Normally Closed" switch.

2. **Enhancement Type** - the transistor requires a Gate-Source voltage, (V_{GS}) to switch the device "ON". The enhancement mode MOSFET is equivalent to a "Normally Open" switch.

Basic operating principle of a MOSFET:

- **Use of the voltage between two terminals to control the current flowing in the third terminal**
- **Also, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch.**

The FET differs from BJT in the following important characteristics:

1. It is a unipolar device
2. It is simpler to fabricate
3. Occupies less space in Integrated form, packaging density is high(>200 million)
4. It has higher input resistance
5. It can be used as a symmetrical Bilateral switch
6. It functions as a memory device
7. It is less noisy than a BJT
8. It exhibits no offset voltage at zero input, hence making an excellent signal chopper

THE ONLY DISADVANTAGE IS IT HAS SMALLER GAIN- BANDWIDTH PRODUCT THAN BJT

The symbols and basic construction for both configurations of MOSFETs are shown below.

DEVICE STRUCTURE AND PHYSICAL OPERATION

Device Structure:

Figure 4.1 shows the physical structure of the n-channel enhancement-type MOSFET. The transistor is fabricated on a p-type substrate. Two heavily doped n-type regions: the $n+$ source and the $n+$ drain regions, are created in the substrate.

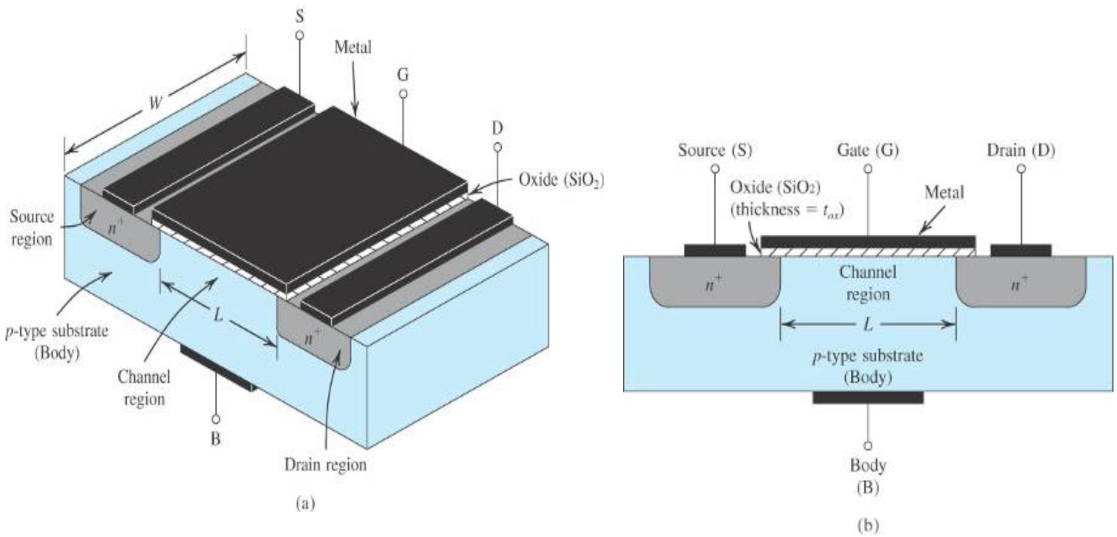


Figure 1. Physical structure of the enhancement-type NMOS transistor: (a)Perspective view; (b)Cross-section. Typically L= 0.1 to 3 μm, W= 0.2 to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

1. A thin layer of silicon dioxide (SiO2) of thickness *tox* (typically 2-50 nm) - an excellent electrical insulator, is grown on the surface of the substrate, in the area between the source and drain regions.
2. Metal is deposited on top of the oxide layer to form the **gate electrode.**
3. Metal contacts are also made to the source region, the drain region, and the substrate, also known as the **body**.

Thus four terminals are brought out: the gate terminal (G), the source terminal (S), the drain terminal (D), and the substrate or body terminal (B).

A voltage applied to the gate of the MOSFET controls current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region labelled **"channel region."**

This region has a length L in the range of 0.1 μm to 3 μm, and a width W in the range of 0.2 μm to 100 μm.

Note: The MOSFET is a symmetrical device [its source and drain can be interchanged with no change in device characteristics].

Device Operation:

(i) With No Gate Voltage

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. They prevent current conduction from drain to source when a voltage V_{DS} is applied. The path between drain and source has a very high resistance (of the order of $10^{12}\Omega$).

(ii) Creating a Channel for Current Flow

The source and the drain are grounded and a positive voltage is applied to the gate.
The positive voltage on the gate causes the free holes (which are positive charged) to be repelled from the region of the substrate under the gate. These holes are pushed downward into the substrate, leaving behind a carrier-depletion region as shown below.

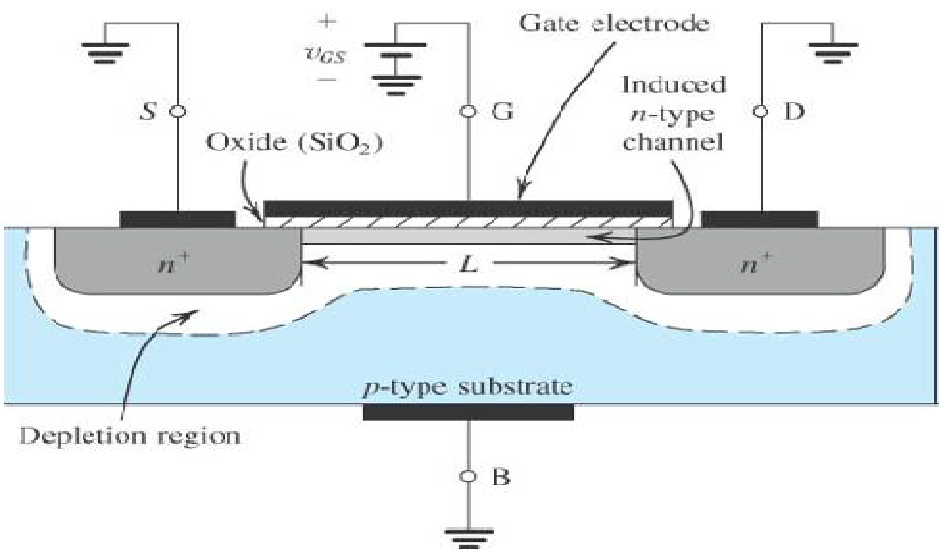


Figure 4.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

The positive gate voltage attracts electrons from the *n*+ source and drain regions into the channel region. When a sufficient number of electrons accumulate near the surface of the substrate under the gate, an n region is in effect created, connecting the source and drain regions, as indicated in Fig. 4.2. This MOSFET is called an **n-channel MOSFET** or, alternatively, an **NMOS transistor**. The induced channel is also called an **inversion layer**. The induced *n* region thus forms a **channel** for current flow from drain to source.

Note: **The value of V_{GS} at which a sufficient number of mobile electrons accumulate in the channel region to form a conducting channel is called the threshold voltage and is denoted V_t.**

The value of V_t is controlled during device fabrication and typically lies in the range of 0.5 V to 1.0V.

Now if a voltage is applied between drain and source, current flows through this induced n region.

The gate and the channel region of the MOSFET form a parallel-plate capacitor, with the oxide layer acting as the capacitor dielectric. An electric field thus develops in the vertical direction. It is this field that controls the amount of charge in the channel, and thus it determines the channel conductivity and, in turn, the current that will flow through the channel when a voltage v_{DS} is applied.

$V_{OV} \equiv v_{GS} - V_t$ (effect voltage, or overdrive voltage)

V_t : Threshold voltage,

Typically lies in the range of 0.3V to 1.0V

The magnitude of the electron charge in the channel by

$$|Q| = C_{ox} V_{OV} \underbrace{WL}_{A}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \begin{cases} C_{ox} : \text{The capacitance per unit gate area,} \\ \qquad \text{called the oxide capacitance} \\ \varepsilon_{ox} : \text{the permittivity of the silicon oxide,} \\ \qquad \varepsilon_{ox} = 3.9\varepsilon_0 = 3.45 \cdot 10^{-11}\ \text{F/m} \\ t_{ox} : \text{the thickness of the oxide} \end{cases}$$

(iii) Effect of Applying a Small V_{DS}

We now apply a small positive voltage V_{DS} between drain and source, as shown in Fig. 4.3.

- The voltage v_{DS} causes a current i_D to flow through the induced n channel. Current is carried by free electrons traveling from source to drain.
- The magnitude of i_D depends on the density of electrons in the channel, which in turn depends on the magnitude of v_{DS}
- Specifically, for $v_{GS} = V_t$, more electrons are attracted into the channel.
- The result is a channel of increased conductance or, equivalently, reduced resistance. In fact, the conductance of the channel is proportional to the excess gate voltage(v_{GS}-V_t), also known as the effective voltage or the overdrive voltage.
- Figure 4.4 shows a sketch of i_D versus v_{DS} for various values of v_{GS}. We observe that the MOSFET is operating as a linear resistance whose value is controlled by v_{GS}.

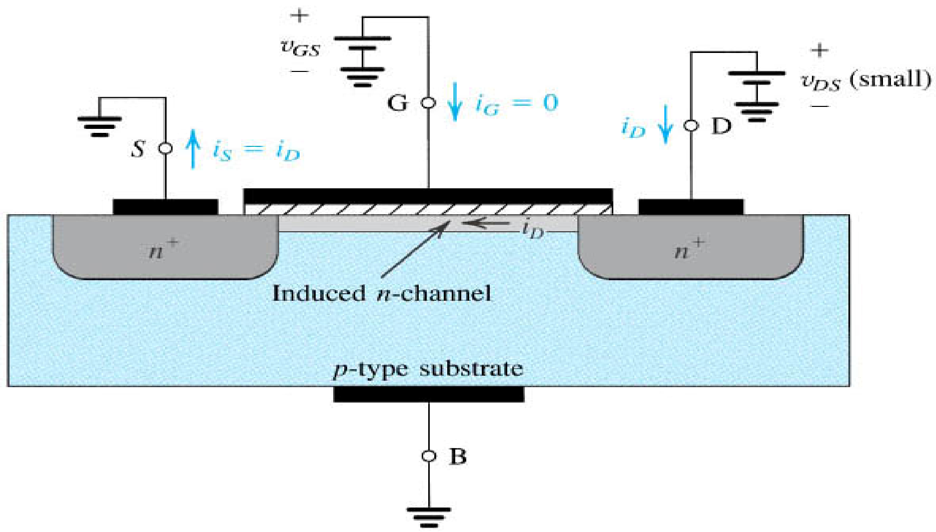


Figure 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS} (depletion region not shown).

- The resistance is infinite for $v_{GS} \leqq V_t$, and its value decreases as v_{GS} exceeds V_t.
- Specifically, the channel conductance is proportional to $v_{GS}–V_t$, and thus i_D is proportional to $(v_{GS}–V_t)\, v_{DS}$.
- Then, increasing v_{GS} above the threshold voltage V_t enhances the channel, hence the name **enhancement-mode operation** and **enhancement-type MOSFET.** Finally, we note that the current that leaves the source terminal (i_S) is equal to the current that enters the drain terminal (i_D), and the gate current $i_G = 0$.

The expression for the channel resistance can be determined as follows:

- The charge per unit channel lenth as

$$\frac{|Q|}{\text{unit channel lenth}} = \frac{C_{ox} V_{OV} WL}{L} = C_{ox} V_{OV} W$$

- The electron field E across the lenth of channel as

$$|E| = \frac{v_{DS}}{L}$$

- $\text{The electron drift velocity} = \mu_n |E| = \mu_n \dfrac{v_{DS}}{L}$

- The value of i_D can now be found by multiplying the charge per unit channel lenth by The electron drift velocity

$$i_D = C_{ox} V_{OV} W \times \mu_n \frac{v_{DS}}{L} = \left[\mu_n C_{ox} \frac{W}{L} V_{OV} \right] v_{DS}$$

$$i_D = \left[\mu_n C_{ox} \frac{W}{L} (v_{GS} - V_t) \right] v_{DS}$$

❖ The Conductance $\frac{i_D}{v_{DS}} = g_{DS} = \mu_n C_{ox} \frac{W}{L}(v_{GS} - V_t)$

❖ $k_n^{'}$: Process transconductance parameter, $k_n^{'} = \mu_n C_{ox}$

❖ k_n : MOSFET transconductance parameter,

$$k_n = k_n^{'}(W/L) = \mu_n C_{ox}(W/L)$$

❖ An NMOSFET with $v_{GS} > V_t$, and with a small v_{DS} applied, the MOSFET behaves as a linear resistance r_{DS} whose value is controlled by the gate voltage v_{GS}

$$r_{DS} = \frac{1}{g_{DS}} = \frac{1}{\mu_n C_{ox}(W/L)(v_{GS} - V_t)}$$

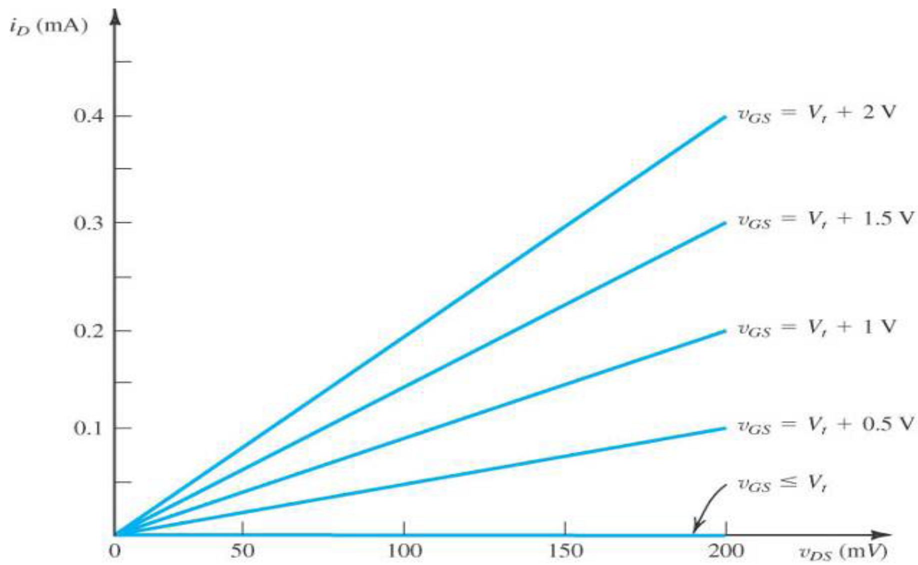


Figure 4.4 The i_D–v_{DS} characteristics of the MOSFET in Fig. 4.3 when the voltage applied between drain and source, v_{DS}, is kept small. The device operates as a linear resistor whose value is controlled by v_{GS}.

(iv) Operation as v_{DS} Is Increased

- As we travel along the channel from source to drain, the voltage (measured relative to the source) increases from 0 to v_{DS}.
- Thus the voltage between the gate and points along the channel decreases from v_{GS} at the source end to v_{GS}–v_{DS} at the drain end.

- Since the channel depth depends on this voltage, we find that the channel is no longer of uniform depth. As v_{DS} is increased, the channel becomes more tapered and its resistance increases correspondingly.
- When v_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to Vt ,

  $v_{GD}= V_t$ or $v_{GS}–v_{DS}= V_t$ or $v_{DS}= v_{GS}–V_t$

  the channel depth at the drain end decreases to almost zero, and the channel is said to be **pinched off.**
- As the value reached for $v_{DS}= v_{GS}–V_t$, the drain current **saturates**, and the MOSFET is said to have entered the saturation region of operation.

  $$v_{DSsat}= v_{GS}–V_t \tag{4.1}$$
- The region of the $i_D–v_{DS}$ characteristic obtained for $v_{DS}< v_{DSsat}$ is called the **triode region.**

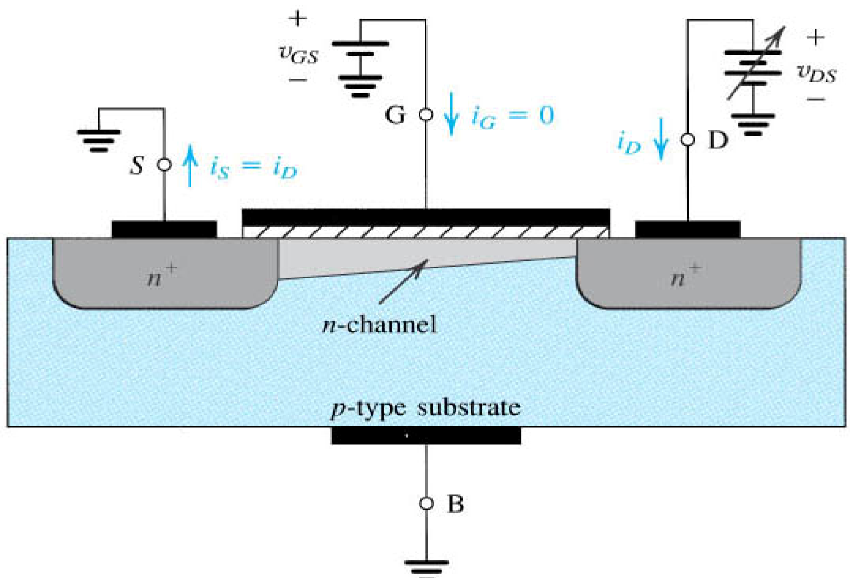
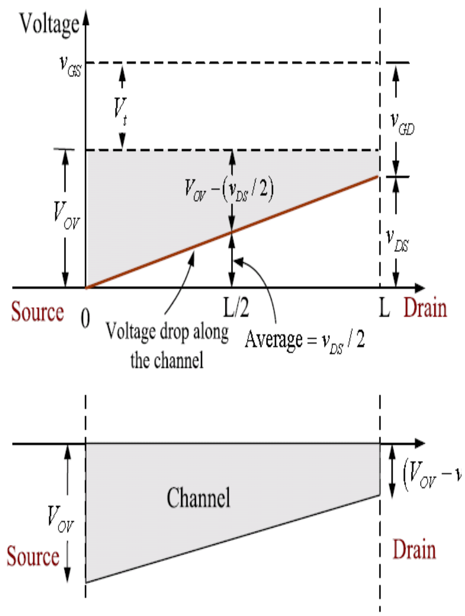


Figure 4.5 Operation of the enhancement NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t.



That the charge in the tapered channel is propotional to the channel cross section area shown in Fig. 5.6(a).

This area in turn can beseen as propotional to $(V_{OV}-v_{DS}/2)$.

The i_D can be found by replacing V_{OV} in (5.7) by $(V_{OV}-v_{DS}/2)$

i.e. $i_D = \left[\mu_n C_{ox}\frac{W}{L}V_{OV}\right]v_{DS}$

$$\Rightarrow i_D = \left[\mu_n C_{ox}\frac{W}{L}\left(V_{OV}-v_{DS}/2\right)\right]v_{DS}$$

$$i_D = k_n'\frac{W}{L}\left(V_{OV}v_{DS}-\frac{v_{DS}^2}{2}\right)$$

$$= k_n'\frac{W}{L}\left((v_{GS}-V_t)v_{DS}-\frac{v_{DS}^2}{2}\right)$$

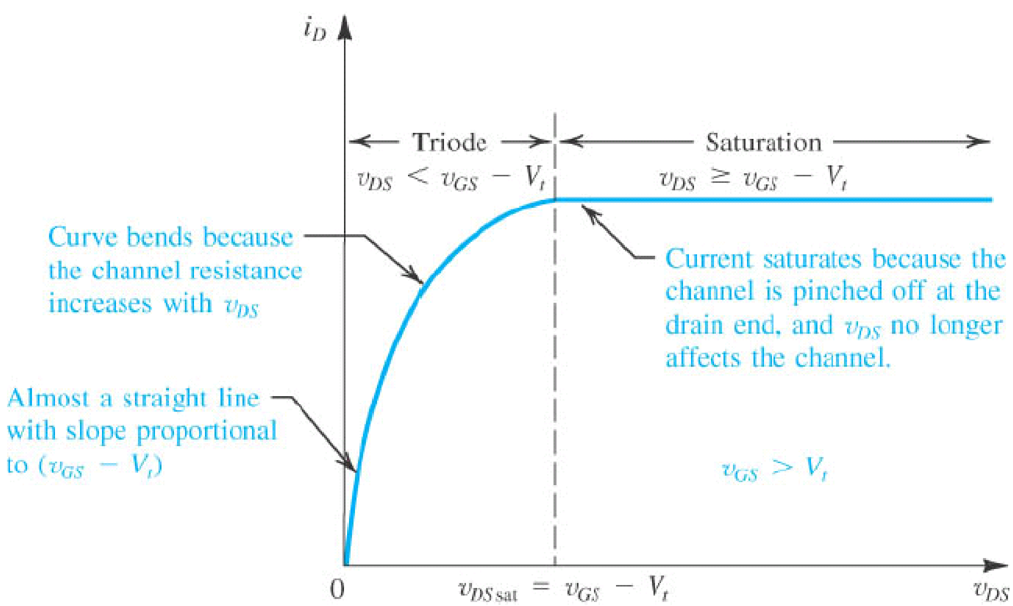
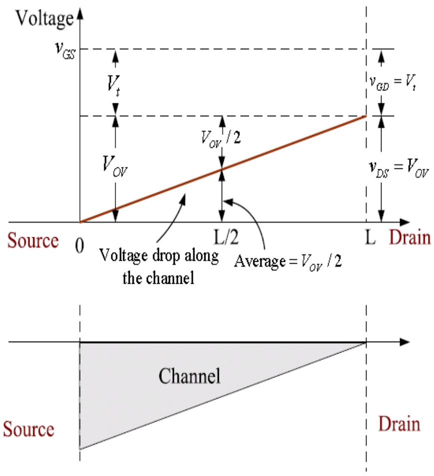


Figure 4.6 The drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} > V_t$.

Operating for $v_{DS} \geq V_{OV}$ increased



$$i_D = \left[\mu_n C_{ox} \frac{W}{L}\left(V_{OV} - V_{OV}/2\right)\right] V_{OV}$$

$$= \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2$$

$$v_{DS(sat)} = V_{OV} = v_{GS} - V_t$$

$$i_D = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2 = \frac{1}{2} k_n' \frac{W}{L}\left(v_{GS} - V_t\right)^2 \text{ (Saturation region)}$$

Derivation of the i_D-v_{DS} Relationship

In the MOSFET, the gate and the channel region form a parallel-plate capacitor for which the oxide layer serves as a dielectric.

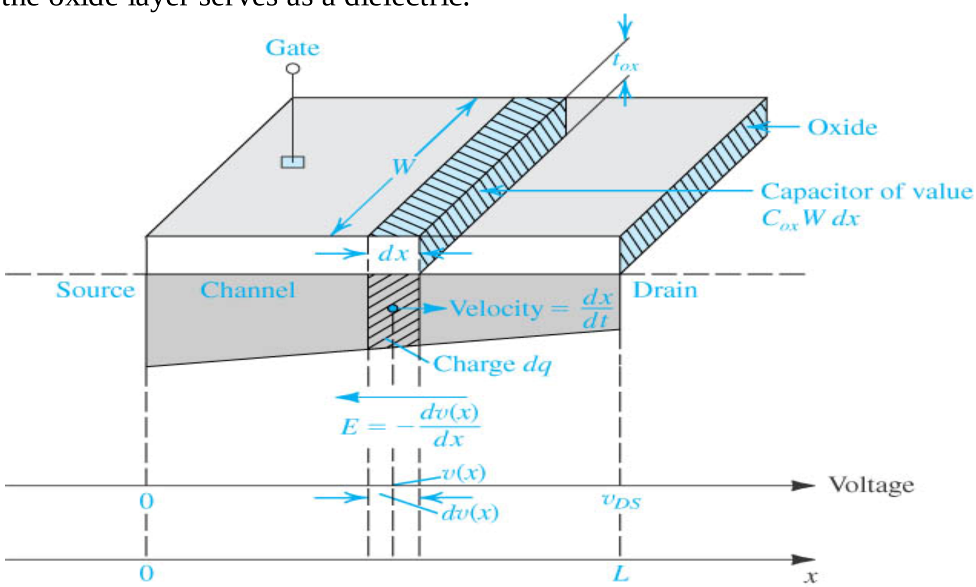


Figure 4.7 Derivation of the i_D-v_{DS} Relationship of the NMOS transistor

If the capacitance per unit gate area is denoted C_{ox} and the thickness of the oxide layer is t_{ox}, then

$$C_{ox} = \varepsilon_{ox} / t_{ox} \qquad (4.2)$$

Where ε_{ox} is the permittivity of the silicon oxide, $\varepsilon = 3.9\ \varepsilon_0 = 3.9 \times 8.854 \times 10^{-12} = 3.45 \times 10^{-11}$ F/m

Initially $v_{GS} > V_t$ *to induce channel and* $v_{DS} < v_{GS} - V_t$ and triode region of operation is assumed i.e

The gate and channel region form a parallel plate capacitor with oxide layer as the dielectric. If the capacitance per unit area is C_{ox} and the thickness of the oxide layer is t_{ox}
Now consider the infinitesimal strip of the gate at distance x from the source.
The capacitance of the strip is $C_{ox}\,W\,dx$
To find the charge stored on this strip of gate capacitance, we multiply capacitance by effective voltage between Gate and the Channel at point x

$$dq = -C_{ox}\ (Wdx)[v_{GS} - v(x) - V_t]$$

The voltage v_{DS} produces an electric field along the channel in the negative x direction.
At point x this field can be expressed as

$$E(x) = -\frac{dv(x)}{dx}$$

The Electric field *E(x)* causes the electron charge *dq* to drift toward the drain with a velocity *dx/dt*

$$\frac{dx}{dt} = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx}$$

The resulting drift current 'i' can be obtained as follows:

$$i = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt}$$

Substituting the above values, the drain current *'i'* can be obtained as follows:

$$i = -\mu_n C_{ox} W[v_{GS} - v(x) - V_t]\ \frac{dv(x)}{dx}$$

Since the current *'i'* is constant at all points along the channel it must be equated to the drain current i_D

$$i_D = -i = \mu_n C_{ox} W[v_{GS} - v(x) - V_t]\ \frac{dv(x)}{dx}$$

$$i_D dx = \mu_n C_{ox} W[v_{GS} - v(x) - V_t] dv(x)$$

Integrating both sides from $x = 0\ to\ x = L\ and\ v(0) = 0\ to\ v(L) = v_{DS}$

$$\int_0^L i_D dx = \int_0^{v_{DS}} \mu_n C_{ox} W[v_{GS} - v(x) - V_t] dv(x)$$

Gives

$$i_D = \mu_n C_{ox} \frac{W}{L}[v_{GS} - V_t]v_{DS} - \frac{1}{2}v_{DS}^2]$$

In the saturation region substituting we get

$$i_D = \frac{1}{2}(\mu_n C_{ox})\frac{W}{L}(v_{GS} - V_t)^2$$

The process transconductance parameter is denoted k_n' and $k_n' = \mu_n C_{ox}$
Therefore the i_D –v_{DS} relationship can be expressed in terms of k_n' as follows:

$$i_D = k_n' \frac{W}{L}[v_{GS} - V_t]v_{DS} - \frac{1}{2}v_{DS}^2] \; \ldots .. \, triode\ region$$

$$i_D = \frac{1}{2}k_n'(v_{GS} - V_t)^2 \ldots \ldots \ldots \, saturation\ region$$

• The drain current is proportional to the ratio of the channel width W to the channel length L, known as the aspect ratio of the MOSFET.
• For a given fabrication process, however, there is a minimum channel length, Lmin.
In fact, the minimum channel length that is possible with a given fabrication process is used to characterize the process and is being continually reduced as technology advances. State of the art MOS technology is a 0.13-µm process, meaning that for this process the minimum channel length possible is 0.13 µm, corresponding to a minimum width of 0.16 µm and t_{ox}= *2nm*.

Example 1 Consider a process technology for which $L_{min} = 0.4\mu m$, $t_{ox} = 8nm$, $\mu_n = 450 cm^2/V \cdot s$, and $V_t = 0.7V$.(a) Find C_{ox} and k_n'. (b)For a MOSFET with W/L = 10, calculate the values of V_{OV}, V_{GS}, and $V_{DS min}$ needed to operate the FET in the saturation region with a dc current $I_D = 100\mu A$. (c) For the device in (b), find the values of V_{OV} and V_{GS} required to cause the device to operate as a 1000Ω resistor for very small V_{DS}.

Solution:

(a) $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45\times10^{-11}}{8\times10^{-9}} = 4.32 \times 10^{-3} F/m^2 = 4.32 fF/\mu m^2$

$$k_n' = \mu_n C_{ox} = 450\left(\frac{cm^2}{V}.s\right) \times 4.32 fF/\mu m^2$$
$$= 194 \times 10^{-6} F/V.s$$
$$= 194 \mu A/V^2$$

(b) For operation in the saturation region,

$$i_D = \frac{1}{2}k_n'(v_{GS} - V_t)^2$$

Thus, $100 = \frac{1}{2} \times 194 \times \frac{8}{0.8}(V_{GS} - 0.7\ \ )^2$

which results in $V_{GS} - 0.7\ \ = 0.32V$

Or $V_{GS}\ = 1.02V$

And $V_{DSmin}\ =\ V_{GS} - 0.7\ \ = 0.32V$

For the MOSFET in the triode region with v_{DS} very small,

$$i_D\ =\ k'_n \frac{W}{L}(v_{GS} - V_t)\ \ v_{DS}$$

From which the drain to source resistance r_{DS} can be found as

$$r_{DS}\ = \frac{v_{DS}}{i_D}|small\ v_{DS}$$
$$= \frac{1}{[k'_n \frac{W}{L}(v_{GS} - V_t)\ \ ]}$$

Thus $$1000 = \frac{1}{[194 \times 10^{-6} \times 10(v_{GS} - 0.7)\ \ ]}$$

which yields,

$$V_{GS} - 0.7\ \ = 0.52V$$

Or $V_{GS}\ = 1.22V$

4.1.7 The p-Channel MOSFET

A p-channel enhancement-type MOSFET (PMOS transistor), fabricated on an n-type substrate with p+ regions for the drain and source, has holes as charge carriers.
The device operates in the same manner as the n-channel device except that v_{GS} and v_{DS} are negative and the threshold voltage V_t is negative. Also, the current i_D enters the source terminal and leaves through the drain terminal.

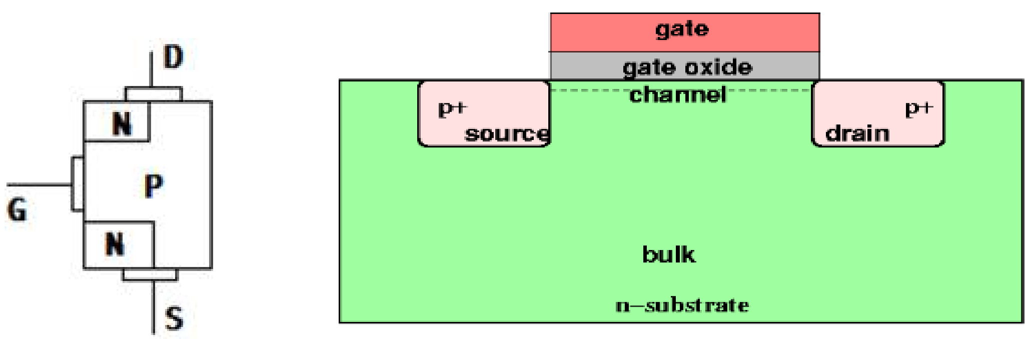


Figure 4.8 Physical construction of p channel E-MOSFET

In general, NMOS devices are normally preferred to PMOS because

- Smaller
- Operate faster and
- Requires lower supply voltages than PMOS.

4.1.8 Complementary MOS or CMOS

As the name implies, complementary MOS technology employs MOS transistors of both polarities. At present time CMOS is the most widely used of all the IC technologies. Figure 4.9 shows cross-section of a CMOS chip illustrating how the PMOS and NMOS transistors are fabricated. While the NMOS transistor is implemented directly in the p-type substrate, the PMOS transistor is fabricated in a specially created n region, known as an ***nwell.***

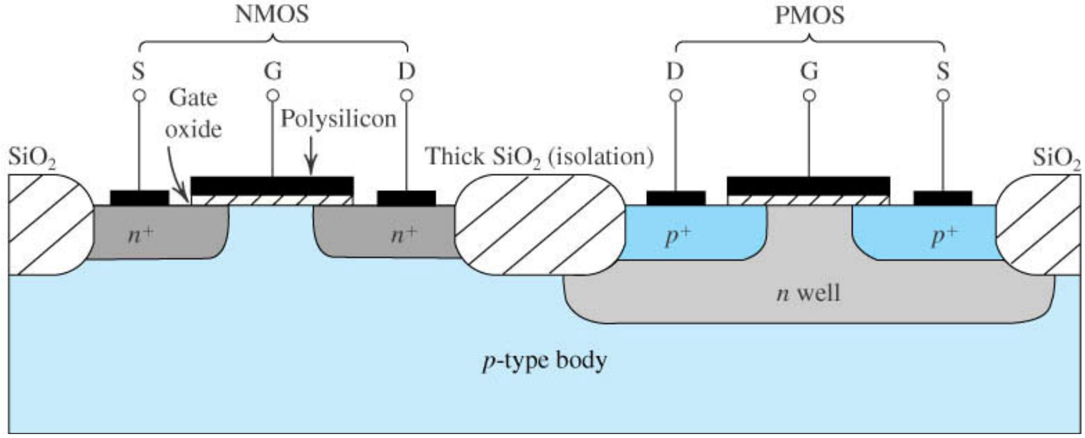


Figure 4.9 Cross-section of a CMOS integrated circuit. Not shown are the connections made to the *p*-type body and to the *n* well; the latter functions as the body terminal for the *p*-channel device.

4.2 CURRENT-VOLTAGE CHARACTERISTICS of an n-channel E-MOSFET

The drain is always positive relative to the source in an n-channel FET. The circuit Symbol for an n-channel E-MOSFET is as shown below:

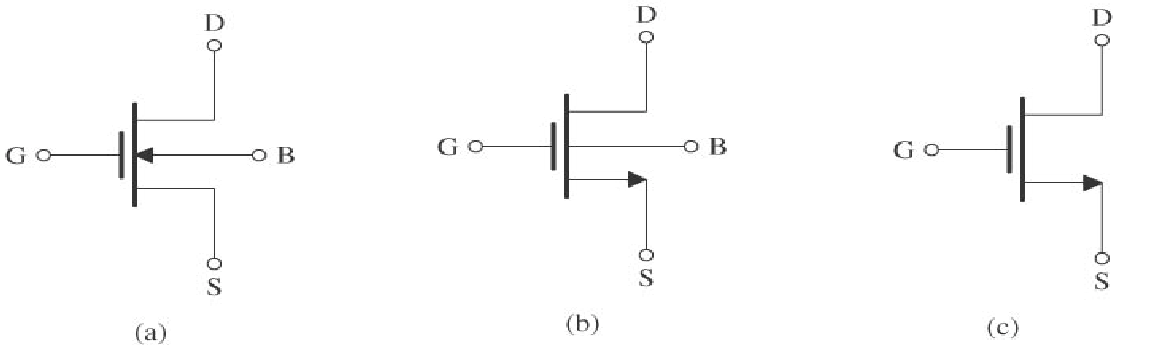


Figure 4.10 (a) Circuit symbol for the n-channel enhancement-type MOSFET.
(b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., n channel). (c) Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

Consider an n-channel enhancement-type MOSFET with voltages v_{GS} *and* v_{DS} applied and with the normal directions of current flow indicated.

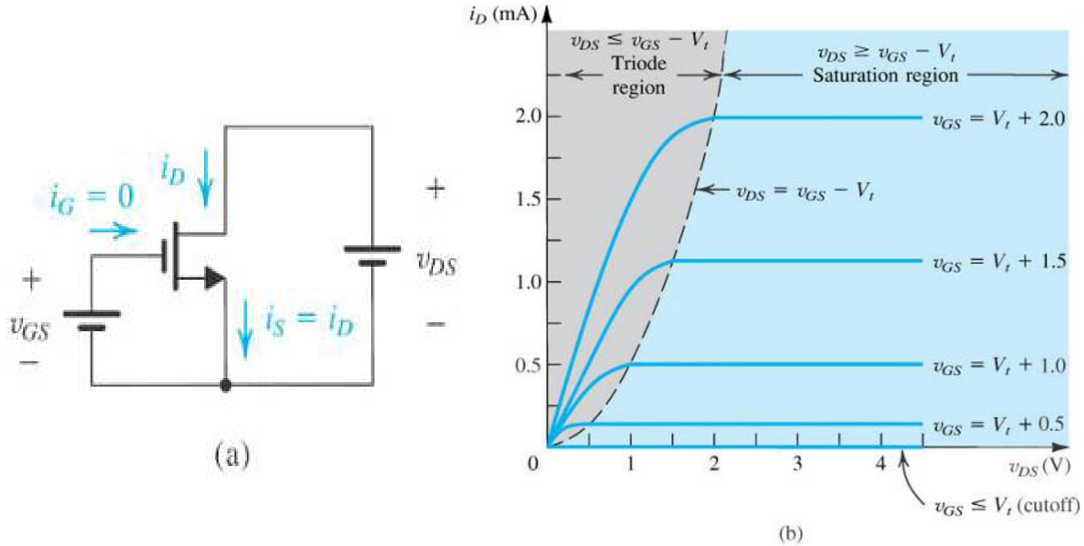


Figure 4.11 (a) An n-channel enhancement-type MOSFET with v_{GS} and v_{DS} applied and with the normal directions of current flow indicated.
(b)The i_D–v_{DS} characteristics for a device with $k'_n(W/L) = 1.0\ mA/V^2$.

There are three distinct regions of operation: the cutoff region, the **triode region, and the saturation region.**

- The saturation region is used if the FET is to operate as an amplifier.
- For operation as a switch, the cutoff and triode regions are utilized

To operate the MOSFET in the triode region we must first induce a channel,

$$v_{GS} \geq V_t \qquad \text{(Induced channel)} \qquad (4.8)$$

And then keep v_{DS} small enough so that the channel remains continuous. This is achieved by ensuring that the gate-to-drain voltage is

$$v_{GD} \geqq V_t \qquad \text{(Continuous channel)} \quad (4.9)$$

$$v_{GD} = v_{GS} + v_{SD} = v_{GS} - v_{DS};$$

$$v_{GS} - v_{DS} > V_t$$

$$v_{DS} < v_{GS} - V_t \qquad \text{(Continuous channel)} \quad (4.10)$$

The n-channel enhancement-type MOSFET operates in the triode region when v_{GS} is greater than V_t and the drain voltage is lower than the gate voltage by at least V_t volts. In the triode region, the i_D-v_{DS} characteristics can be described by

$$i_D = k_n' \frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v^2{}_{DS}] \qquad (4.11)$$

where $k_n' = \mu_n C_{ox}$ is the process transconductance parameter.
If v_{DS} is sufficiently small

$$i_D \cong k_n' \frac{W}{L}[v_{GS} - V_t]v_{DS}$$

Specifically, for v_{GS} set to a value *VGS*, r_{DS} is given by,

$$r_{DS} \equiv \frac{v_{DS}}{i_D}\Bigg|_{\substack{v_{DSsmall} \\ v_{GS} = V_{GS}}} = [k_n' \frac{W}{L}(v_{GS} - V_t)]^{-1}$$

It is also useful to express r_{DS} in terms of the **gate-to-source overdrive voltage**

$$V_{OV} = V_{GS} - V_t$$

$$r_{DS} = 1/[k_n'(\frac{W}{L})V_{OV}]$$

To operate the MOSFET in the saturation region, a channel must be induced,

$\boldsymbol{v_{GS} \geqq V_t}$ *(Induced channel)* and then the Gate-Drain and drain source voltages should be

$\boldsymbol{v_{GD} \leqq V_t}$ ***or*** $\boldsymbol{v_{DS} \geqq v_{GS} - V_t}$ *(Pinched-off channel)*

The n-channel enhancement-type MOSFET operates in the saturation region when $\boldsymbol{v_{GS} \geqq V_t}$ and $\boldsymbol{v_{DS}}$ is higher than the gate voltage by at least $\boldsymbol{V_t}$ volts.

The boundary between the triode region and the saturation region is characterized by

$$v_{DS} = v_{GS} - V_t \qquad \textit{(Boundary)}$$

Substituting this value of v_{DS} into Eq. (4.11)

$$i_D = \frac{1}{2} k'_n (v_{GS} - V_t)^2$$

Since the drain current is independent of the drain voltage, the saturated MOSFET behaves as an ideal current source whose value is controlled by v_{GS} according to the nonlinear relationship in the above Eq.

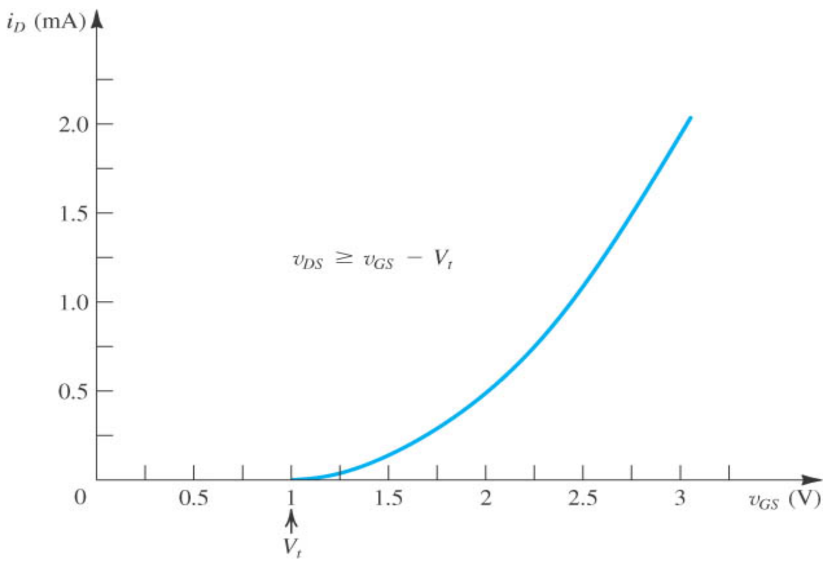


Figure 4.12 The i_D–v_{GS} characteristic for an enhancement-type NMOS transistor in saturation (V_t = 1 V, k'_n W/L = 1.0 mA/V^2).

Figure 4.13 shows a circuit representation of this view of MOSFET operation in the saturation region. Note that this is a **large-signal equivalent-circuit model.**

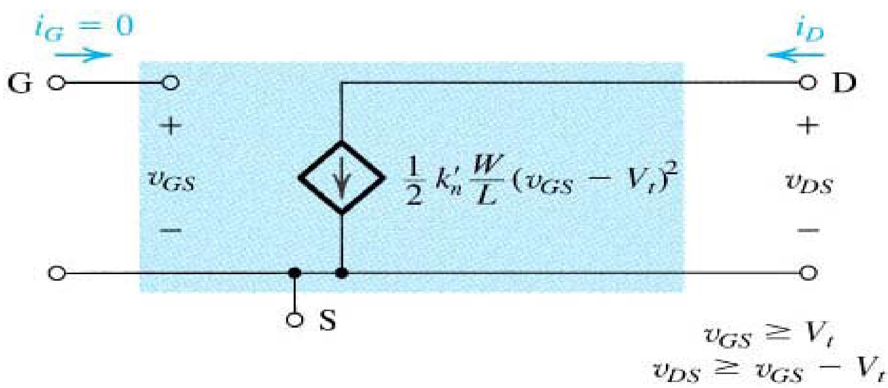


Figure 4.13 Large-signal equivalent-circuit model of an *n-channel MOSFET operating in the saturation region.*

Finite Output Resistance in Saturation

Change in v_{DS} in saturation, implies no change in corresponding i_D and hence infinite resistance in saturation. This is because of the assumption that once channel is pinched off, further increase in v_{DS} have no effect on the channel's shape. But, in practice, as v_{DS} is increased, the channel pinch-off point is moved slightly away from the drain, toward the source.

Channel Length Modulation: With an increase in v_{DS}, the channel length decreases from L to L-ΔL, but voltage drop across it remains the same, and the additional drop will appear across the depletion region between the end of the channel and the drain

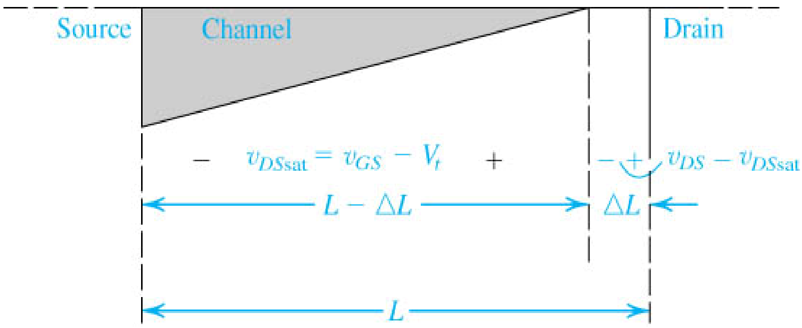


Figure 4.14
Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by D*L*).

To account for the dependence of i_D on v_{DS} in saturation, replace L with L- ΔL in the i_D Eq.

$$
\begin{aligned}
i_D &= \frac{1}{2}k_n'\frac{W}{L-\Delta L}(v_{GS}-V_t)^2 \\
&= \frac{1}{2}k_n'\frac{W}{L}\frac{1}{1-(\Delta L/L)}(v_{GS}-V_t)^2 \\
&\cong \frac{1}{2}k_n'\frac{W}{L}\left(1+\frac{\Delta L}{L}\right)(v_{GS}-V_t)^2
\end{aligned}
$$

where we have assumed that $(\Delta L/L) \ll 1$. Now, if we assume that ΔL is proportional to v_{DS},

$$\Delta L = \lambda' v_{DS}$$

where λ' is a process-technology parameter with the dimensions of μm/V, we obtain for i_D,

$$i_D = \frac{1}{2}k_n'\frac{W}{L}\left(1+\frac{\lambda'}{L}v_{DS}\right)(v_{GS}-V_t)^2$$

Usually, λ'/L is denoted λ,

$$\lambda = \frac{\lambda'}{L}$$

λ is a process technology parameter and now the expression for i_D becomes,

$$i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS})$$

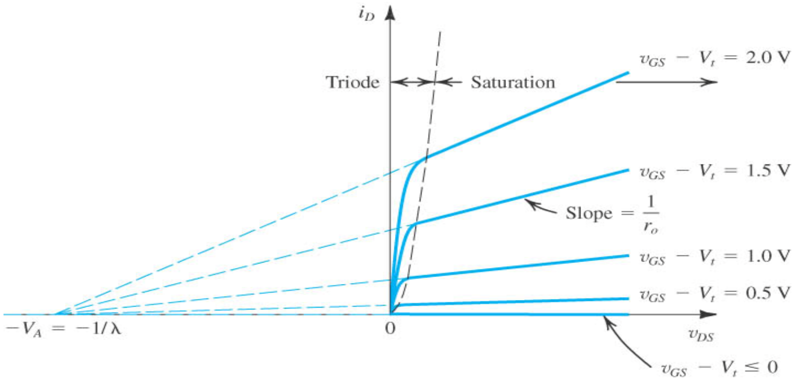


Figure 4.15 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length *L*.

The extrapolated characteristics intersect the x-axis at V_A, and the corresponding value of v_{DS} for i_D=0, from the equation will be -1/ λ
V_A = 1/ λ and $V_A = V_A'L$ V/µm where V_A is called Early Voltage
With the dependence of i_D on v_{DS}, we can now define the output resistance as follows:

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\,\text{constant}}$$

$$r_o = \left[\lambda \frac{k_n'}{2} \frac{W}{L} (V_{GS} - V_t)^2\right]^{-1}$$

$$r_o = \frac{1}{\lambda I_D}$$

$$r_o = \frac{V_A}{I_D}$$

where I_D is the drain current *without* channel-length modulation taken into account; that is,

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2$$

Thus the output resistance is inversely proportional to the drain current. Finally, we show in Fig. 4.17 the large-signal equivalent circuit model incorporating r_o.

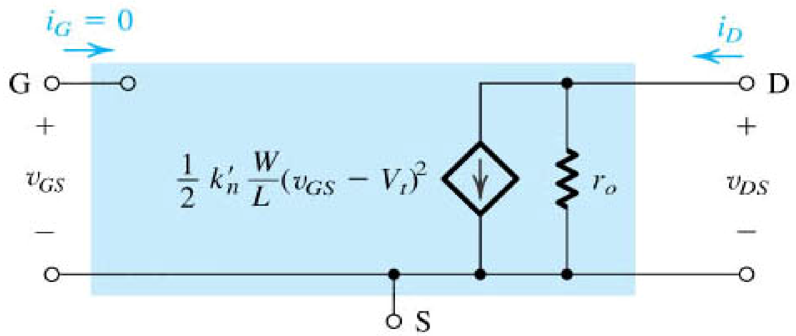


Figure 4.17 Large Signal equivalent model of n-channel E-MOSFET incorporating r_o

4.2.4 Characteristics of the *p*-Channel MOSFET

The circuit symbol for the p-channel enhancement-type MOSFET is shown in Fig. 4.18(a). Recall that for the p-channel device the threshold voltage V_t is negative. To induce a channel we apply a gate voltage that is more negative than V_t.

$$v_{GS} \leqq V_t \tag{4.27}$$

And apply a drain voltage that is more negative than the source voltage.

- To operate in the triode region V_{DS} must satisfy

$$v_{DS} \geqq v_{GS} - V_t$$

$$i_D = k_p' \frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2} v^2{}_{DS}]$$

$$k_p' = \mu_p C_{ox}$$

- To Operate in saturation, v_{DS} must satisfy the relationship,

$$v_{DS} \leqq v_{GS} - V_t$$

$$i_D = \frac{1}{2} k_p' \frac{W}{L}(v_{GS} - V_t)^2 (1 + \lambda v_{DS})$$

The symbols and Circuit diagram to measure V-I characteristics of a p-channel MOSFET are as shown below:

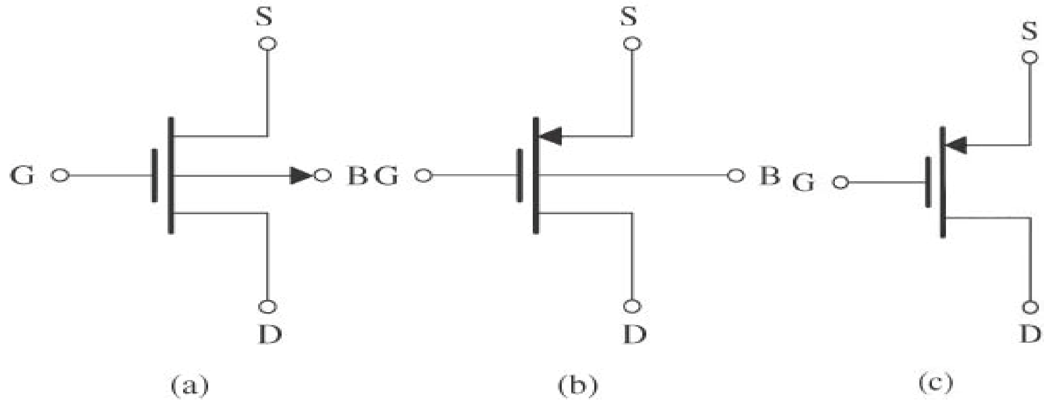


Figure 4.18 (a) Circuit symbol for the *p*-channel enhancement-type MOSFET. **(b)** Modified symbol with an arrowhead on the source lead. **(c)** Simplified circuit symbol for the case where the source is connected to the body

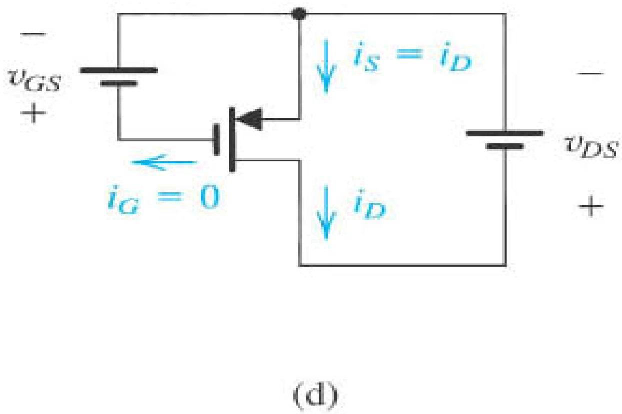


Figure 4.18 (d) The MOSFET with voltages applied and the directions of current flow indicated. Note that v_{GS} and v_{DS} are negative and i_D flows out of the drain terminal.

Comparison of NMOS and PMOS FETs

The NMOS and PMOS FETs are compared in terms of their symbol representation and large signal equivalent models as shown below:

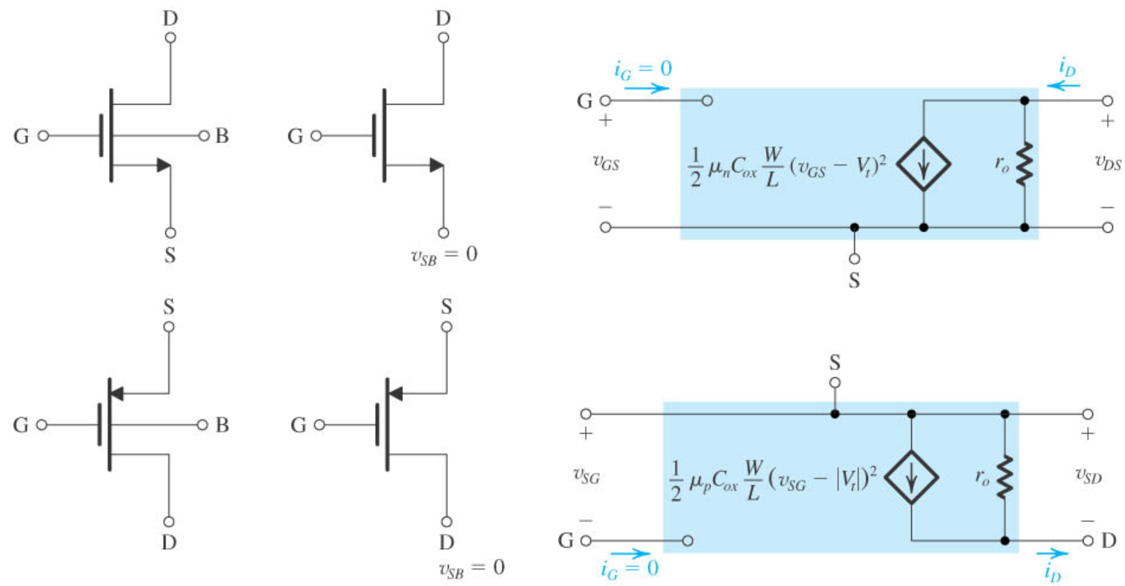


Figure 4.19 Comparison of the NMOS and PMOS transistors

4.2.5 The Role of the Substrate---The body Effect

In most of the applications the Source and Body terminals are connected and therefore V_{SB} =0 and it has no effect on the circuit operation. But, in IC's, substrate is connected to the most negative voltage, making SB junction reverse biased, hence the depletion region around the channel increases decreasing the channel depth
This decrease in channel depth should be compensated by a corresponding increase in V_t

$$V_t = V_{t0} + \gamma[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}]$$

$$\gamma = \frac{\sqrt{2qN_A\varepsilon_s}}{C_{ox}}$$

The body voltage controls i_D; thus the body acts as another gate for the MOSFET, a phenomenon known as the **body effect**. Here we note that the parameter γ is known as the **body-effect parameter**

4.2.6 Temperature Effects

1. The magnitude of V_t decreases by about 2 mV for every 1°C rise in temperature.
This decrease in $|V_t|$ gives rise to a corresponding increase in drain current as temperature is increased.
2. But, K' decreases with temperature and its effect is dominant.

Therefore, Overall effect is decrease in i_D with increase in temperature

4.2.7 Breakdown and Input Protection

There are three types of Breakdown:

- **Weak avalanche**: For V_{DS}>20V up to 150V avalanche breakdown between D and Substrate causing large drain currents
- **Punch through**: Occurs in short channel devices for smaller voltages, when depletion region of drain extends to source, through the channel
- **Permanent breakdown**: Due to high values of V_{GS} in the range of 30V which may cause the thin oxide layer to be ruptured. Therefore Input protection circuits are provided with MOSFETs

MOSFET CIRCUITS AT DC - Examples

Problem 1:

Design the circuit of Fig. 4.20 so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100\ \mu A/V^2$, $L = 1\ \mu m$, and $W = 32\ \mu m$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

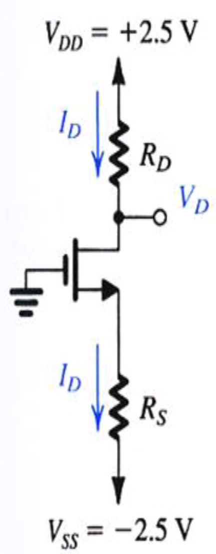


FIGURE 4.20 Circuit for Example 4.2.

Solution

Since $V_D = 0.5$ V is greater than V_G, this means the NMOS transistor is operating in the saturation region, and we use the saturation-region expression of i_D to determine the required value of V_{GS},

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2$$

Substituting $V_{GS} - V_t = V_{OV}$, $I_D = 0.4$ mA $= 400\ \mu$A, $\mu_n C_{ox} = 100\ \mu$A/V^2, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

which results in

$$V_{OV} = 0.5 \text{ V}$$

Thus, $$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 4.20, we note that the gate is at ground potential. Thus the source must be at -1.2 V, and the required value of R_S can be determined from

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega$$

To establish a dc voltage of +0.5 V at the drain, we must select R_D as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega$$

Problem 2

Analyze the circuit shown in Fig. 4.23(a) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1$ V and $k_n'(W/L) = 1$ mA/V^2. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

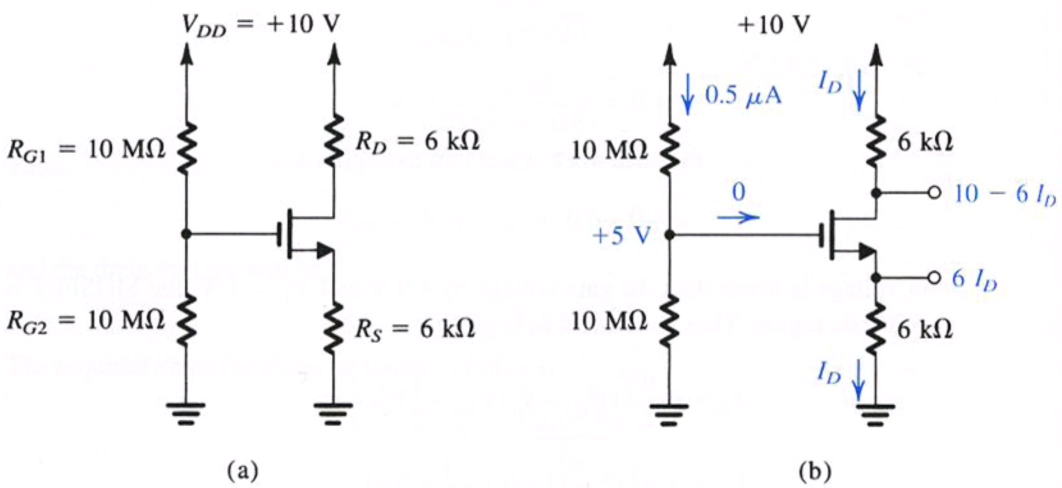


FIGURE 4.23 **(a)** Circuit for Example 4.5. **(b)** The circuit with some of the analysis details shown.

Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two 10-MΩ resistors,

$$V_G = V_{DD}\frac{R_{G2}}{R_{G2}+R_{G1}} = 10 \times \frac{10}{10+10} = +5 \text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 4.23(b). Since the voltage at the gate is 5 V and the voltage at the source is $I_D\ (\text{mA}) \times 6\ (\text{k}\Omega) = 6I_D\ (\text{V})$, we have

$$V_{GS} = 5 - 6I_D$$

Thus I_D is given by

$$\begin{aligned} I_D &= \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2 \\ &= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2 \end{aligned}$$

which results in the following quadratic equation in I_D:

$$18I_D^2 - 25I_D + 8 = 0$$

This equation yields two values for I_D: 0.89 mA and 0.5 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$\begin{aligned} I_D &= 0.5 \text{ mA} \\ V_S &= 0.5 \times 6 = +3 \text{ V} \\ V_{GS} &= 5 - 3 = 2 \text{ V} \\ V_D &= 10 - 6 \times 0.5 = +7 \text{ V} \end{aligned}$$

Since $V_D > V_G - V_t$, the transistor is operating in saturation, as initially assumed.

Problem 3:

The NMOS and PMOS transistors in the circuit of Fig. 4.25(a) are matched with $k_n'(W_n/L_n) = k_p'(W_p/L_p) = 1\ \text{mA/V}^2$ and $V_{tn} = -V_{tp} = 1$ V. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP}, as well as the voltage v_O, for $v_I = 0$ V, +2.5 V, and −2.5 V.

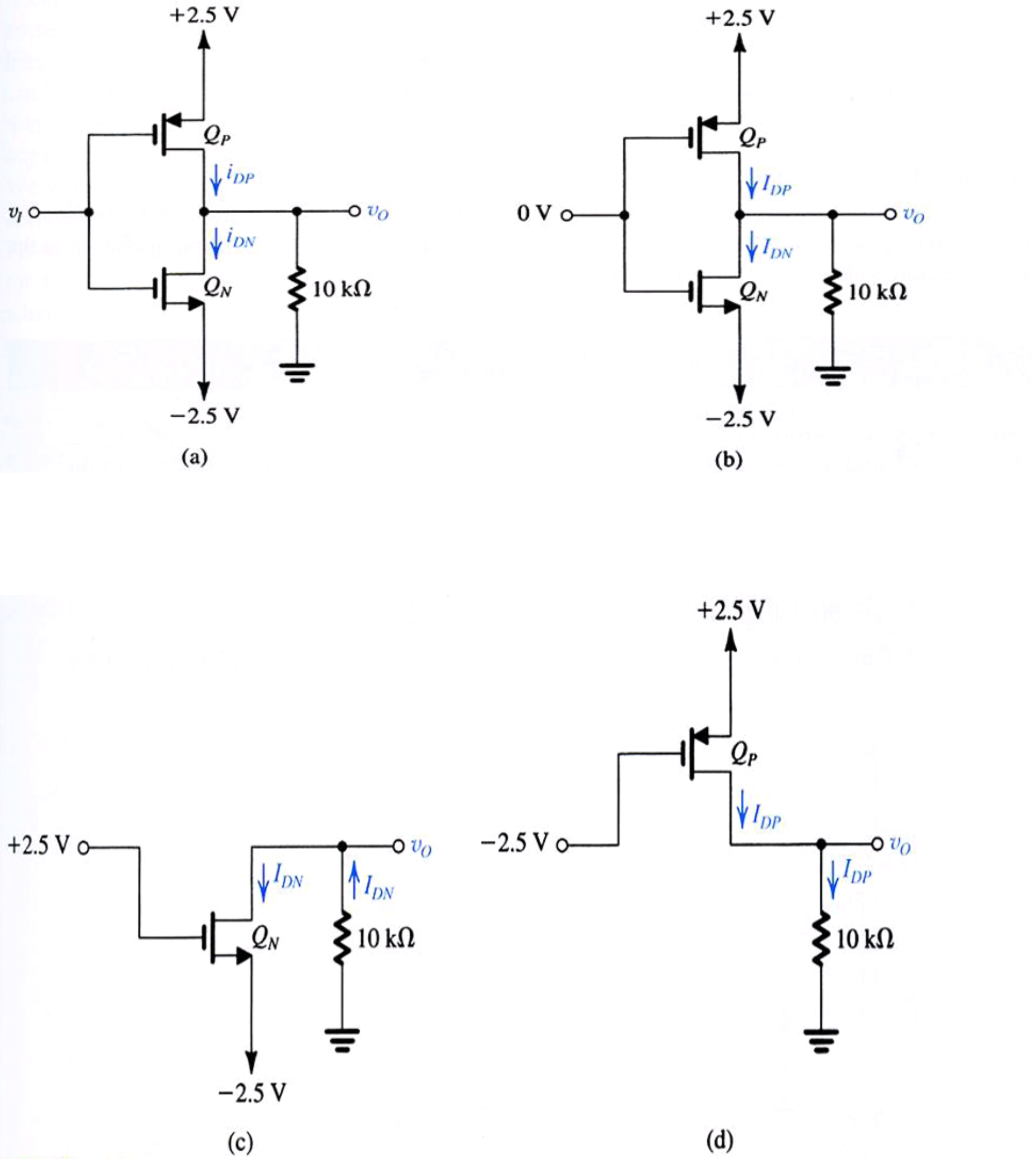


FIGURE 4.25 Circuits for Example 4.7.

Solution

Figure 4.25(b) shows the circuit for the case $v_I = 0$ V. We note that since Q_N and Q_P are perfectly matched and are operating at equal $|V_{GS}|$ (2.5 V), the circuit is symmetrical, which dictates that $v_O = 0$ V. Thus both Q_N and Q_P are operating with $|V_{DG}| = 0$ and, hence, in saturation. The drain currents can now be found from

$$I_{DP} = I_{DN} = \tfrac{1}{2} \times 1 \times (2.5 - 1)^2$$
$$= 1.125 \text{ mA}$$

Next, we consider the circuit with $v_I = +2.5$ V. Transistor Q_P will have a V_{GS} of zero and thus will be cut off, reducing the circuit to that shown in Fig. 4.25(c). We note that v_O will be negative, and thus v_{GD} will be greater than V_t, causing Q_N to operate in the triode region. For simplicity we shall assume that v_{DS} is small and thus use

$$I_{DN} \cong k_n'(W_n/L_n)(V_{GS} - V_t)V_{DS}$$
$$= 1[2.5 - (-2.5) - 1][v_O - (-2.5)]$$

From the circuit diagram shown in Fig. 4.25(c), we can also write

$$I_{DN}\,(\text{mA}) = \frac{0 - v_O}{10\,(\text{k}\Omega)}$$

These two equations can be solved simultaneously to yield

$$I_{DN} = 0.244 \text{ mA} \qquad v_O = -2.44 \text{ V}$$

Note that $V_{DS} = -2.44 - (-2.5) = 0.06$ V, which is small as assumed.

Finally, the situation for the case $v_I = -2.5$ V [Fig. 4.25(d)] will be the exact complement of the case $v_I = +2.5$ V: Transistor Q_N will be off. Thus $I_{DN} = 0$, Q_P will be operating in the triode region with $I_{DP} = 0.244$ mA and $v_O = +2.44$ V.

4.4 THE MOSFET AS AN AMPLIFIER AND AS A SWITCH

4.4.1 Large-Signal Operation-The Transfer Characteristic

Figure 4.26(a) shows the basic structure (skeleton) of the most commonly used MOSFET amplifier, the **common-source (CS) circuit or ground-source circuit.**

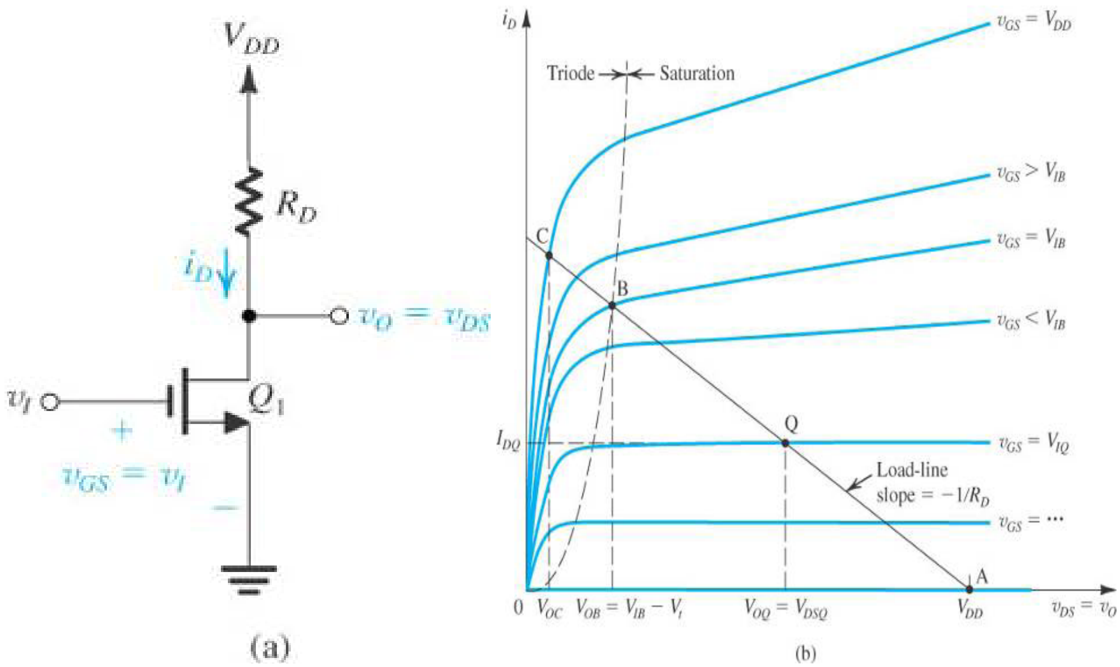


Figure 4.26(a) Basic structure of the common-source amplifier. (b)Graphical construction to determine the transfer characteristic of the amplifier in (a)

The basic control action of the MOSFET is that changes in v_{GS}(here, changes in v_I as $v_{GS}=v_I$) give rise to changes in i_D, we are using a resistor R_D to obtain an output voltage v_o

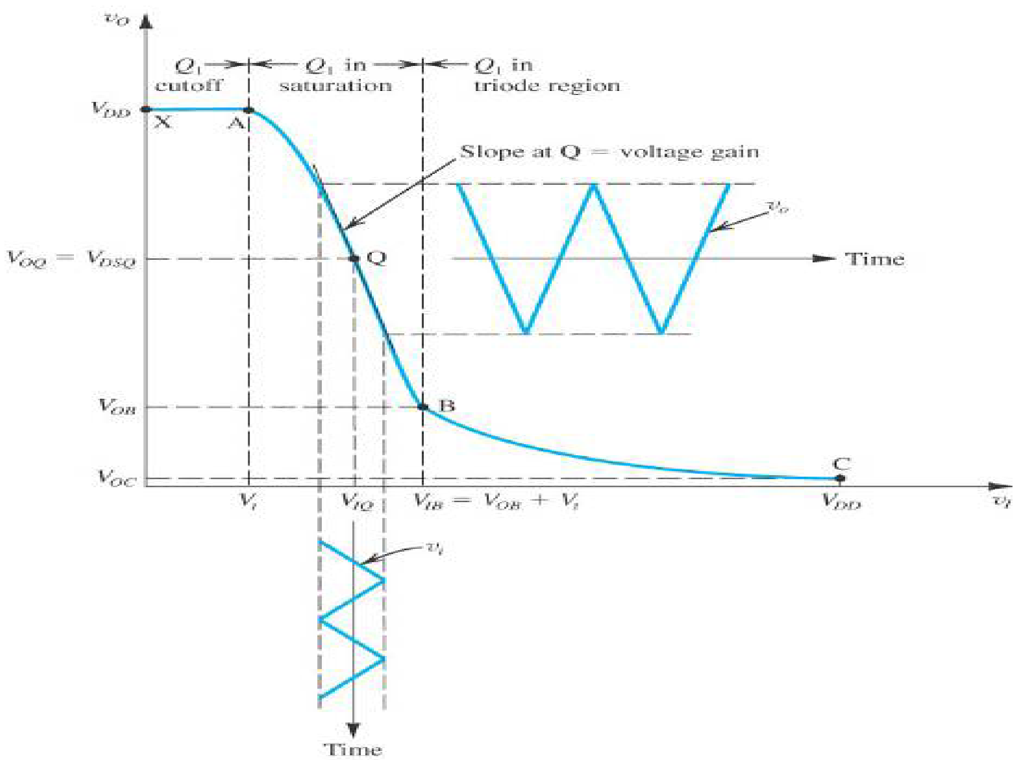
$$v_O = v_{DS} = V_{DD} - R_D i_D$$

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D} v_{DS}$$

Figure 4.26(b) shows a sketch of MOSFET's i_D-v_{DS} characteristic curves superimposed on which is a straight line representing the i_D-v_{DS} relationship of Eq.(4.37). The straight line in Fig.4.26(b) is known as the load line.

- For any given value of $v_I < V_t$, the transistor will be cut off, as shown in the i_D-v_{DS} curve and find v_o from the point of intersection of this curve with the load line.
- The circuit works as follows: Since $v_{GS}=v_I$, we see that for $v_I < V_t$, the transistor will be cut off, i_D will be zero, and $v_o=v_{GS}=V_{DD}$. Operation will be at the point labeled A.
- As v_I exceeds V_t, the transistor turns on, i_D increases, and v_o decreases. Since v_o will initially be high, the transistor will be operating in the **saturation region**. This corresponds to points along the segment of the load line from A to B.

- It is obtained for $V_{GS}=V_{IQ}$ and has the coordinates $V_{OQ}=V_{DSQ}$ and I_{DQ}.
- Saturation-region operation continues until V_o decreases to the point that it is below vi by V_t volts.
- At this point . $v_{DS}=v_{GS}-V_t$, and the MOSEFT enters its triode region of operation.This is indicate in Fig.4.26(b) by point B.
- Point B is defined by $V_{OB}=V_{IB}-V_t$
- For $V_I> V_{IB}$, the transistor is driven deeper into the triode region. The output voltage decreases slowly towards zero.
- Point C obtained for $v_I= V_{DD}$.



(c)

Figure 4.26(Continued)(c) Transfer characteristic showing operation as an amplifier biased at point Q.

4.4.3 Operation as a Switch

When the MOSFET is used as a switch, it is operated at the extreme points of the transfer curve.

• Specifically, the device is turned off by keeping $v_I< V_t$ resulting in operation somewhere on the segment ***XA*** with $\boldsymbol{v_o=V_{DD}}$.

• The switch is turned on by applying a voltage close to V_{DD}, resulting in operation close to point C with v_o very small (at C, $v_o = V_{oc}$).
The common-source MOS circuit can be used as a logic inverter with the "low" voltage level close to 0 V and the "high" level close to V_{DD}.

4.4.4 Operation as a Linear Amplifier

- To operate the MOSFET as an amplifier we make use of the saturation-mode segment of the transfer curve.
- The device is biased at a point located somewhere close to the middle of the curve; point Q called the **quiescent point.**
- The voltage signal to be amplified v_i is then superimposed on the dc voltage V_{IQ} as shown in Fig.4.26(c).It can be seen that the amplifier will be very linear, and v_o will have the same waveform as v_i except that it will be larger by a factor equal to the voltage gain of the amplifier at Q

$$A_v \equiv \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{IQ}}$$

- The voltage gain is equal to the slope of the transfer curve at the bias point Q.
- Observe that the slope is negative, and thus the basic CS amplifier is inverting.

4.4.5 Analytical Expressions for the Transfer Characteristic

The *i-v* relationships that describe the MOSFET operation in the three regions- cutoff, saturation, and triode- can be easily used to derive analytical expressions for the three segments of the transfer characteristics.

- The Cutoff-Region Segment, XA

  Here, $v_I \leqq V_t$, and $v_o \geqq V_{DD}$.
- The Saturation-Region Segment, AQB

  $v_I \geqq V_t$, and $v_o \geqq v_I - V_t$.

Substituting i_D in the expression for v_o

$$i_D = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)(v_I - V_t)^2$$

$$v_O = V_{DD} - R_D i_D$$

$$v_O = V_{DD} - \frac{1}{2} R_D \mu_n C_{OX} \frac{W}{L}(v_I - V_t)^2$$

Therefore, the expression for the incremental voltage gains Av at a bias point Q at which $V_I = V_{IQ}$ as follows:

$$A_v \equiv \frac{dv_O}{dv_I}\Big|_{v_I=V_{IQ}}$$

$$A_v = -R_D \mu_n C_{OX} \frac{W}{L}(V_{IQ} - V_t)$$

- Another simple and very useful expression for the voltage gain can be obtained by substituting $v_I=V_{IQ}$ and $v_o=V_{OQ}$ in Eq. (4.39), utilizing Eq. (4.40), and substituting V_{IQ}-V_t=V_{OV}. The result is

$$A_v = -\frac{2(V_{DD} - V_{OQ})}{V_{OV}} = -\frac{2V_{RD}}{V_{OV}} \qquad (4.41)$$

where V_{RD} is the dc voltage across the drain resistor R_D; that is, V_{RD}=V_{DD}-V_{OQ}.

- The end point of the saturation-region segment is characterized by

$$V_{OB}=V_{IB}-V_t \qquad (4.42)$$

- The Triode-Region Segment, BC

Here, $v_I \geqq V_t$, and $v_o \leqq v_I$-V_t.

$$v_O = V_{DD} - R_D \mu_n C_{OX} \frac{W}{L}[(v_I - V_t)v_O - \frac{1}{2}v_O^2]$$

$$v_O \cong V_{DD} - R_D \mu_n C_{OX} \frac{W}{L}(v_I - V_t)v_O \qquad (4.43)$$

$$v_O = V_{DD} /[1 + R_D \mu_n C_{OX} \frac{W}{L}(v_I - V_t)]$$

$$r_{DS} = 1/[\mu_n C_{OX} \frac{W}{L}(v_I - V_t)]$$

$$v_O = V_{DD} \frac{r_{DS}}{r_{DS} + R_D} \qquad (4.44)$$

Usually, r_{DS}<<R_D

$$v_O \cong V_{DD} \frac{r_{DS}}{R_D} \qquad (4.45)$$

4.5 BIASING IN MOS AMPLIFIER CIRCUITS

- An essential step in the design of a MOSFET amplifier circuit is the establishment of an appropriate dc operating point for the transistor.
- This is the step known as biasing or bias design

4.5.1 Biasing by Fixing *VGS*

The most straightforward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required to provide the desired I_D.

$$I_D = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_t)^2$$

Biasing by fixing V_{GS} is not a good technique.

1. V_t, C_{ox} and W/L vary widely among devices
2. V_t and μ_n depend on temperature

4.5.2 Biasing by Fixing V_G and Connecting a Resistance in the Source

An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, *VG*, and connecting a resistance in the source lead, as shown in Fig.4.30 (a). For this circuit we

$$V_G = V_{GS} + R_S I_D \qquad (4.46)$$

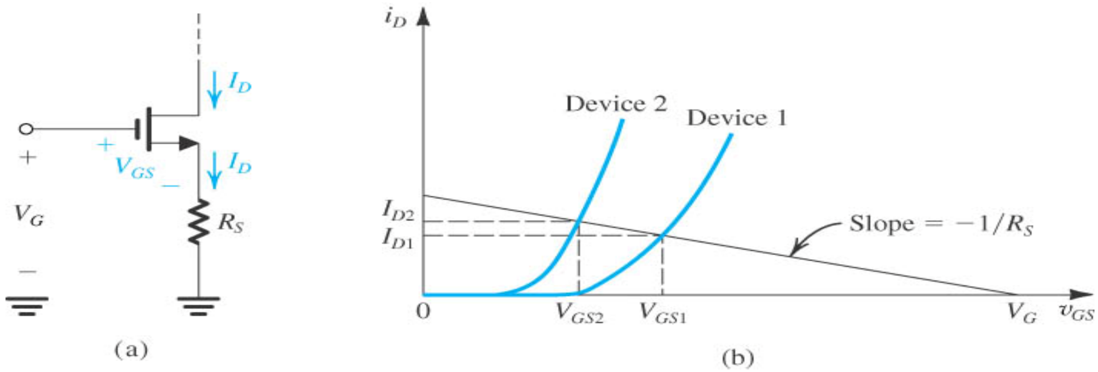


Figure 4.30 Biasing using a fixed voltage at the gate, V_G, and a resistance in the source lead, R_S: **(a)** basic arrangement; **(b)** reduced variability in I_D;

Resistor *Rs* provides *negative feedback*, which acts to stabilize the value of the bias current I_D. This gives it the name **degeneration resistance**

Figure 4.30(b) provides a graphical illustration of the effectiveness of this biasing scheme. The intersection of this straight line with the i_D-V_{GS} characteristic curve provides the coordinates (I_D and V_{GS}) of the bias point. Observe that compared to the case of fixed V_{GS}, here the variability obtained in I_D is much smaller.

Two possible practical discrete implementations of this bias scheme are shown in Fig. 4.30(c) and (e).

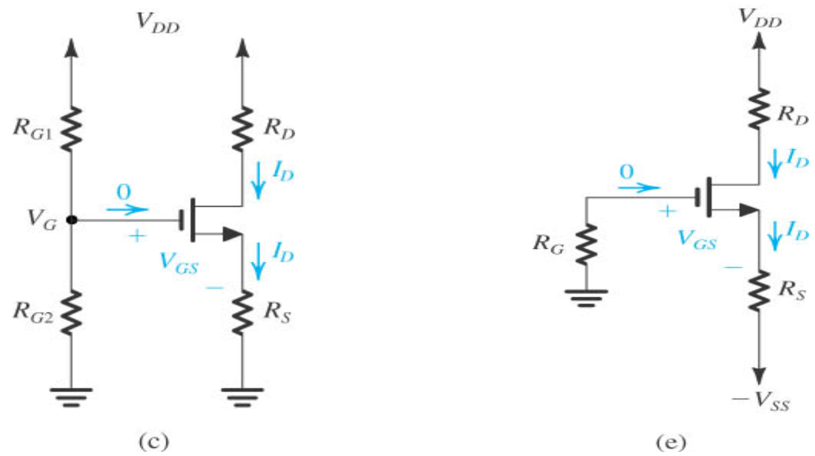


Figure 4.30 Biasing using a fixed voltage at the gate, V_G, and a resistance in the source lead, R_S: **(c)** practical implementation using a single supply; **(e)** practical implementation using two supplies

Example:

It is required to design the circuit of Fig. 4.30(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k_n'W/L = 1$ mA/V^2. For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same $k_n'W/L$ but $V_t = 1.5$ V.

Solution

As a rule of thumb for designing this classical biasing circuit, we choose R_D and R_S to provide one-third of the power-supply voltage V_{DD} as a drop across each of R_D, the transistor (i.e., V_{DS}) and R_S. For $V_{DD} = 15$ V, this choice makes $V_D = +10$ V and $V_S = +5$ V. Now, since I_D is required to be 0.5 mA, we can find the values of R_D and R_S as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5} = 10\ \text{k}\Omega$$

$$R_S = \frac{V_S}{R_S} = \frac{5}{0.5} = 10\ \text{k}\Omega$$

The required value of V_{GS} can be determined by first calculating the overdrive voltage V_{OV} from

$$I_D = \tfrac{1}{2}k_n'(W/L)V_{OV}^2$$

$$0.5 = \tfrac{1}{2} \times 1 \times V_{OV}^2$$

which yields $V_{OV} = 1$ V, and thus,

$$V_{GS} = V_t + V_{OV} = 1 + 1 = 2\ \text{V}$$

Now, since $V_S = +5$ V, V_G must be

$$V_G = V_S + V_{GS} = 5 + 2 = 7 \text{ V}$$

To establish this voltage at the gate we may select $R_{G1} = 8$ MΩ and $R_{G2} = 7$ MΩ. The final circuit is shown in Fig. 4.31. Observe that the dc voltage at the drain (+10 V) allows for a positive signal swing of +5 V (i.e., up to V_{DD}) and a negative signal swing of –4 V [i.e., down to $(V_G - V_t)$].

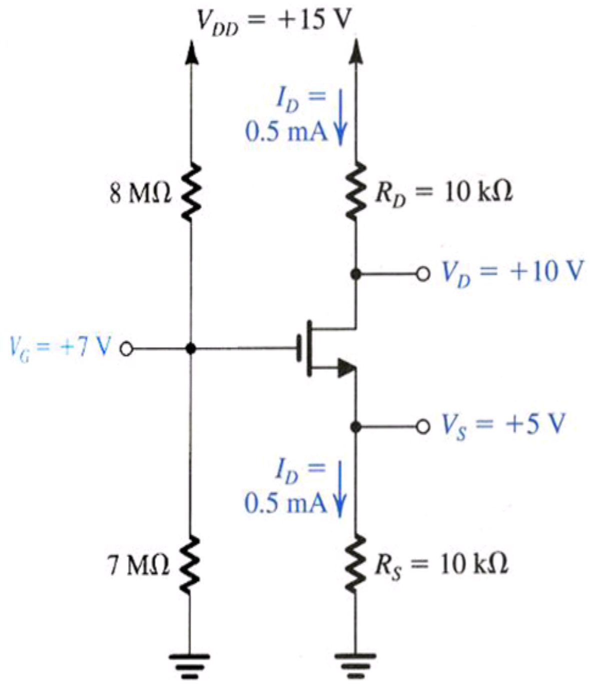


FIGURE 4.31 Circuit for Example 4.9.

If the NMOS transistor is replaced with another having $V_t = 1.5$ V, the new value of I_D can be found as follows:

$$I_D = \tfrac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \quad (4.47)$$

$$V_G = V_{GS} + I_D R_S$$

$$7 = V_{GS} + 10 I_D \quad (4.48)$$

Solving Eqs. (4.47) and (4.48) together yields

$$I_D = 0.455 \text{ mA}$$

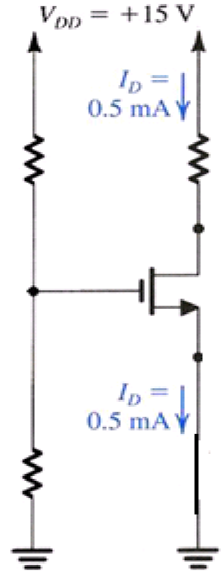
Thus the change in I_D is

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

which is $\frac{-0.045}{0.5} \times 100 = -9\%$ change.

4.19 Repeat Example 4.9 when fixed V_{GS} bias is used.

The circuit for fixed V_{GS} bias is as shown below:



Let the drop across the drain resistor RD and the drain source voltage of MOSFET V_{DS} be equal = 15/2=7.5V

Therefore the value of R_D = 7.5/0.5mA = 15kΩ

Now the value of VOV can be calculated using the equation,

$$i_D = \frac{1}{2} k_n'(v_{GS} - V_t)^2$$

$$0.5 = \frac{1}{2} \times 1 \times V_{OV}^2$$

which yields $V_{OV} = 1$ V, and thus,

$$V_{GS} = V_t + V_{OV} = 1 + 1 = 2 \text{ V}$$

Here V_G =2V.Hence the possible values for R_{G1} and R_{G2} can be 2MΩ and 13MΩ.

Now, if the value of V_t change to 1.5V, the new value of i_D would be,

$$i_D = \frac{1}{2} k_n'(v_{GS} - V_t)^2$$

$$i_D = \frac{1}{2} \times 1(2 - 1.5)^2 = 0.125mA$$

Therefore the difference/ change in the drain current is,
$\Delta i_D = (0.125 - 0.5)mA = -0.375mA$

Therefore the % change in i_D is $\frac{-0.375}{0.5} = -75\%$

4.5.3 Biasing Using a Drain-to-Gate Feedback Resistor

Here the large feedback resistance R_G (usually in the MΩ range) forces the dc voltage at the gate to be equal to that at the drain (because I_G=0) as shown in figure Fig. 4.32. Thus we can write

$$V_{GS}=V_{DS}=V_{DD}-R_D I_D$$

$$V_{DD}=V_{GS}+R_D I_D \qquad \textbf{(4.49)}$$

which is identical in form to Eq. (4.46).

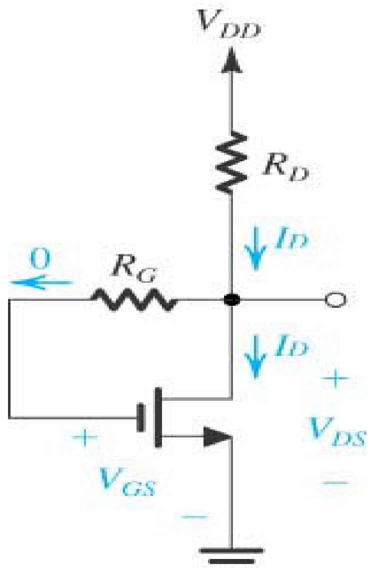


Figure 4.32 Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G.

Example: It is required to design a Gate-Drain feedback bias circuit to operate at a DC current of 0.5mA. Assume V_{DD} = +5V, K_n'W/L=1mA/V^2, V_t=1V and λ=0. Find R_D, I_D and V_D

Refer to the same circuit of Figure 4.32.

Here v_{GS} and V_D should be at the same voltage. Hence we can find v_{GS} first using the saturation expression for drain current.

$$i_D = \frac{1}{2} k_n' (v_{GS} - V_t)^2$$

$$0.5 = \frac{1}{2} \times 1(V_{OV})^2$$

$$V_{OV} = 1V \text{ and hence } v_{GS} = 2V = V_{DS}$$

$$R_D = \frac{V_{DD} - v_{GS}}{I_D} = \frac{5-2}{0.5m} = 6k\Omega$$

Allowing for 5% change in R_D, the new standard resistance that can be used is 6.2KΩ

With a 6.2kΩ resistor new value for I_D is 0.484mA

Then, the corresponding value of $\boldsymbol{V_{DS}=V_{DD}-R_D I_D}$

$$\boldsymbol{V_{DS}=5-6.2*0.484 = 1.9V}$$

4.5.4 Biasing Using a Constant-Current Source

The most effective scheme for biasing a MOSFET amplifier is that using a constant-current source. Figure 4.33(a) shows such an arrangement applied to a discrete MOSFET. A circuit for implementing the constant-current source I is shown in Fig. 4.33(b).

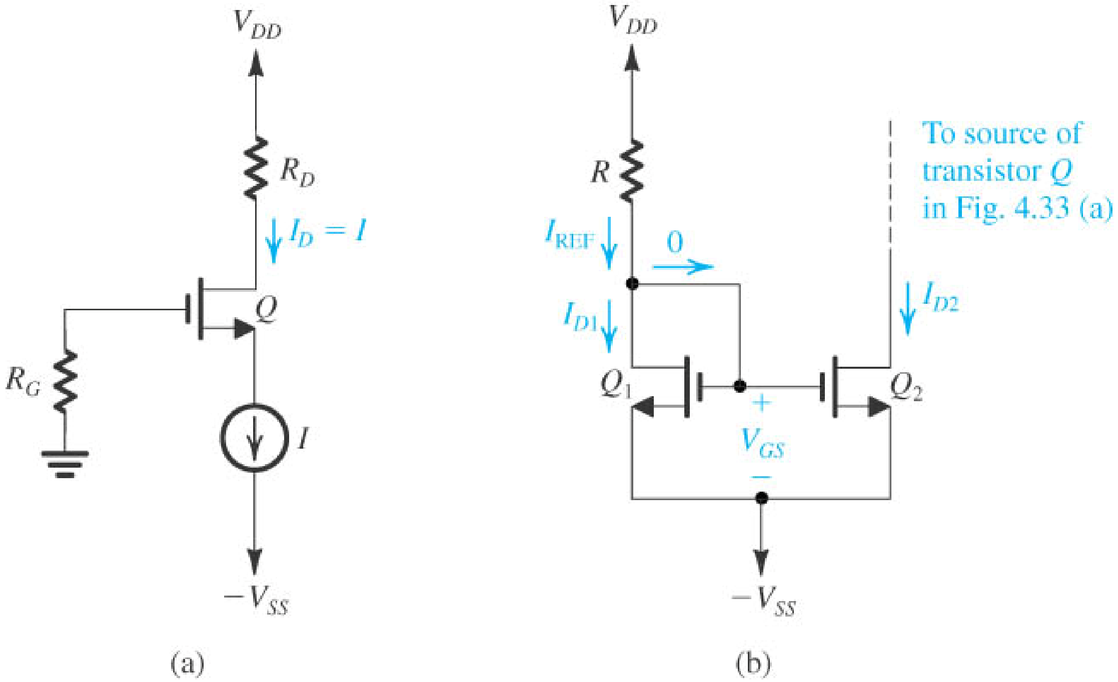


Figure 4.33 (a) Biasing the MOSFET using a constant-current source *I*. **(b)** Implementation of the constant-current source *I* using a current mirror.

Transistor Q_1, whose drain is shorted to its gate and thus is operating in the saturation region, such that

$$I_{D1} = \frac{1}{2}k'_n(\frac{W}{L})_1(V_{GS} - V_t)^2$$

Where we have neglected channel-length modulation (i.e., assumed λ=0)

• The drain current of Q_1 is supplied by V_{DD} through resistor R. Since the gate currents are zero,

$$I_{D1} = I_{REF} = \frac{V_{DD} + V_{SS} - V_{GS}}{R} \qquad (4.51)$$

R is considered to be the *reference current* of the current source and is denoted I_{REF}.

Now consider transistor Q_2: It has the same V_{GS} as Q_1; thus if we assume that it is operating in saturation, its drain current, which is the desired current I of the current source, will be

$$I = I_{D2} = \frac{1}{2}k'_n(\frac{W}{L})_2(V_{GS} - V_t)^2$$

where we have neglected channel-length modulation.
Equation (4.51) and (4.52) enable us to relate the current I to the reference current I_{REF},

$$I = I_{REF}\frac{(W/L)_2}{(W/L)_1} \qquad (4.53)$$

This circuit, known as a **current mirror**, is very popular in the design of IC MOS amplifiers.

4.6 SMALL-SIGNAL OPERATION AND MODELS

In Section 4.4 we learned that linear amplification can be obtained by biasing the MOSFET to operate in the saturation region and by keeping the input signal small.

4.6.1 The DC Bias Point

The dc bias current can be found by setting the signal v_{gs} to zero; thus,

$$I_D = \frac{1}{2}k'_n\frac{W}{L}(V_{GS} - V_t)^2 \qquad (4.54)$$

The dc voltage at the drain, V_{DS} or simply V_D (since S is ground), will be

$$V_D = V_{DD} - R_D I_D \qquad (4.55)$$

To ensure saturation-region operation, we must have

$$V_D > V_{GS} - V_t$$

Furthermore, since the total voltage at the drain will have a signal component superimposed on V_D, V_D has to be sufficiently greater than V_D -V_t to allow for the required signal swing.

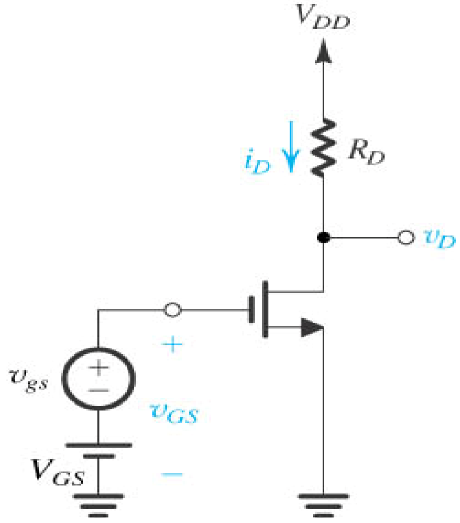


Figure 4.34 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.

4.6.2 The Signal Current in the Drain Terminal

- Next, consider the situation with the input signal v_{gs} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \qquad (4.56)$$

- resulting in a total instantaneous drain current i_D ,

$$i_D = \frac{1}{2}k'_n\frac{W}{L}(V_{GS} + v_{gs} - V_t)^2$$

$$= \frac{1}{2}k'_n\frac{W}{L}(V_{GS} - V_t)^2 + k'_n\frac{W}{L}(V_{GS} - V_t)v_{gs} + \frac{1}{2}k'_n\frac{W}{L}v_{gs}^2 \qquad (4.57)$$

- The **first term** on the right-hand side of Eq.(4.57) can be recognized as the **dc bias current I_D** (Eq. 4.54).
- The **second term** represents a **current component that is proportional to the input signal v_{gs}.**
- The **third term** is a **current component that is proportional to the square of the input signal**.

- To reduce the nonlinear distortion introduced by the MOSFET, the input signal should be kept small so that
$$\frac{1}{2}k'_n \frac{W}{L} v_{gs}^2 \ll k'_n \frac{W}{L}(V_{GS}-V_t)v_{gs}$$
- Resulting in
$$v_{gs} \ll 2(V_{GS}-V_t) \qquad (4.58)$$
- Or, equivalently,
$$v_{gs} \ll 2V_{OV} \qquad (4.59)$$

- If this **small-signal condition** is satisfied, we may neglect the last term in Eq. (4.57) and express i_D as
$$i_D \simeq I_D + i_d$$
- Where
$$i_d = k'_n \frac{W}{L}(V_{GS}-V_t)v_{gs}$$
- The parameter that relates i_d and v_{gs} is the MOSFET **transconductance** g_m ,
$$g_m \equiv \frac{i_d}{v_{gs}} = k'_n \frac{W}{L}(V_{GS}-V_t)$$

Figure 4.35 presents a graphical interpretation of the small-signal operation of the enhancement MOSFET amplifier.

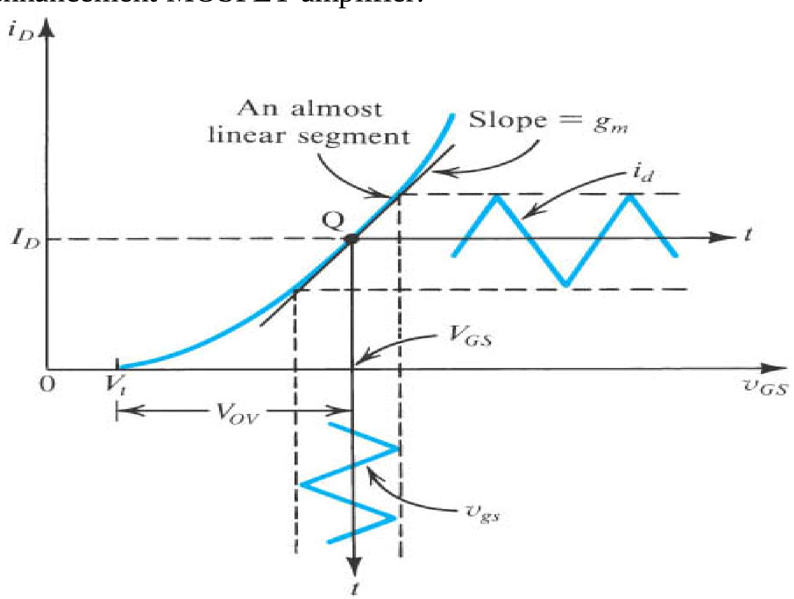
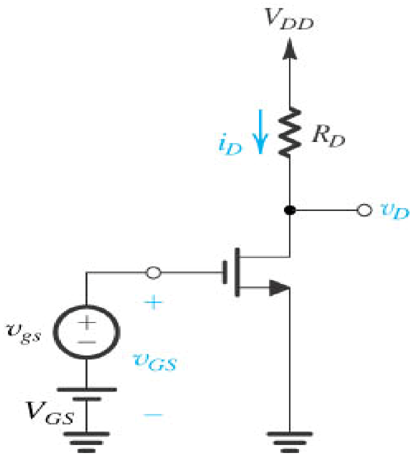


Figure 4.35 Small-signal operation of the enhancement MOSFET amplifier.

4.6.3 The Voltage Gain

Returning to the circuit of Fig. 4.34, we can express the total instantaneous drain voltage v_D as follows:



The signal component

$$v_D = V_{DD} - R_D i_D$$

$$v_D = V_{DD} - R_D(I_D + i_d)$$

$$v_D = V_D - R_D i_d - R_D I_D$$

- The signal component

$$v_d = -i_d R_D = -g_m v_{gs} R_D \qquad (4.64)$$

- Voltage gain is given by

$$A_v \equiv \frac{v_d}{v_{gs}} = -g_m R_D \qquad (4.65)$$

- This is illustrated in Fig. 4.36, which shows v_{GS} and v_D.

Note:

1. Gain is negative indicating 180^0 phase shift between input and output
2. Gain is proportional to load resistance R_D and transconductance g_m

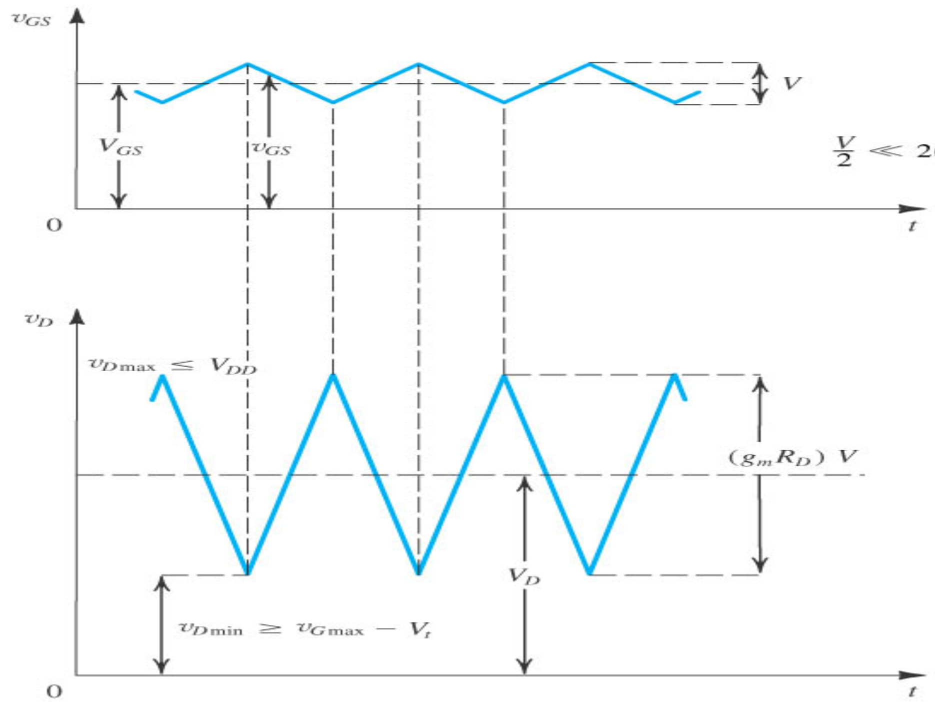
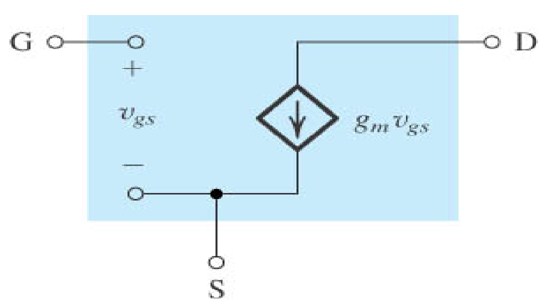


Figure 4.36 Total instantaneous voltages v_{GS} and v_D for the circuit in Fig 4.34

4.6.5 Small Signal Models for the MOSFET

FET behaves as a Voltage controlled current source – taking a signal v_{gs} between gate and source and provides a current $g_m v_{gs}$ at the drain terminal
Input and output resistances are very high ideally, infinite

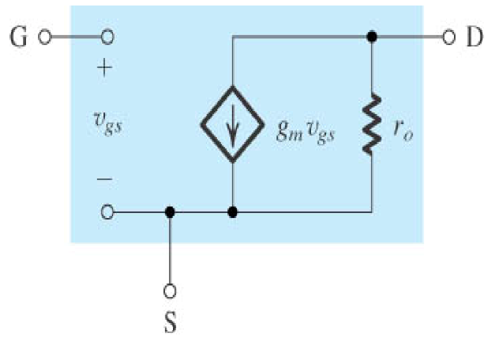


(a)

Figure 4.37 Small-signal models for the MOSFET: (a) neglecting the dependence of i_D on v_{DS} in saturation

Exact Model

- The previous model assumes i_D is independent of v_{DS} which is not true, because of the effect of channel length modulation.
- This was modeled by a finite resistance r_0 between drain and source, in parallel to the controlled current source typically of the order of 10kΩ to 100kΩ



(b)

Figure 4.37 Small-signal models for the MOSFET: **(b)** including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A| / I_D$.

The transconductance g_m

- g_m and r_0 depend on the DC bias point of the circuit
- g_m can be increased by by using a short and wide channel or by increasing the V_{GS} (which reduces the available voltage swing)
- We have the MOSFET transconductance parameter:

$$g_m = k_n'(W/L)(V_{GS} - V_t) = k_n'(W/L)V_{OV} \qquad (4.69)$$

Other useful expressions for g_m - 1

Another useful expression for g_m can be obtained by substituting for $(V_{GS} - V_t)$ in Eq. (4.69) by $\sqrt{2I_D/(k_n'(W/L))}$ [from Eq. (4.53)]:

$$g_m = \sqrt{2k_n'}\sqrt{W/L}\sqrt{I_D} \qquad (4.70)$$

This expression shows that

1. For a given MOSFET, g_m is proportional to the square root of the dc bias current.
2. At a given bias current, g_m is proportional to $\sqrt{W/L}$.

Yet another useful expression for g_m of the MOSFET can be obtained by substituting for $k_n'(W/L)$ in Eq. (4.69) by $2I_D/(V_{GS} - V_t)^2$:

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}} \qquad (4.71)$$

The T equivalent –Circuit Model

- The T model can be developed through a simple transformation of the previous hybrid –π model.
- This is very useful in many applications

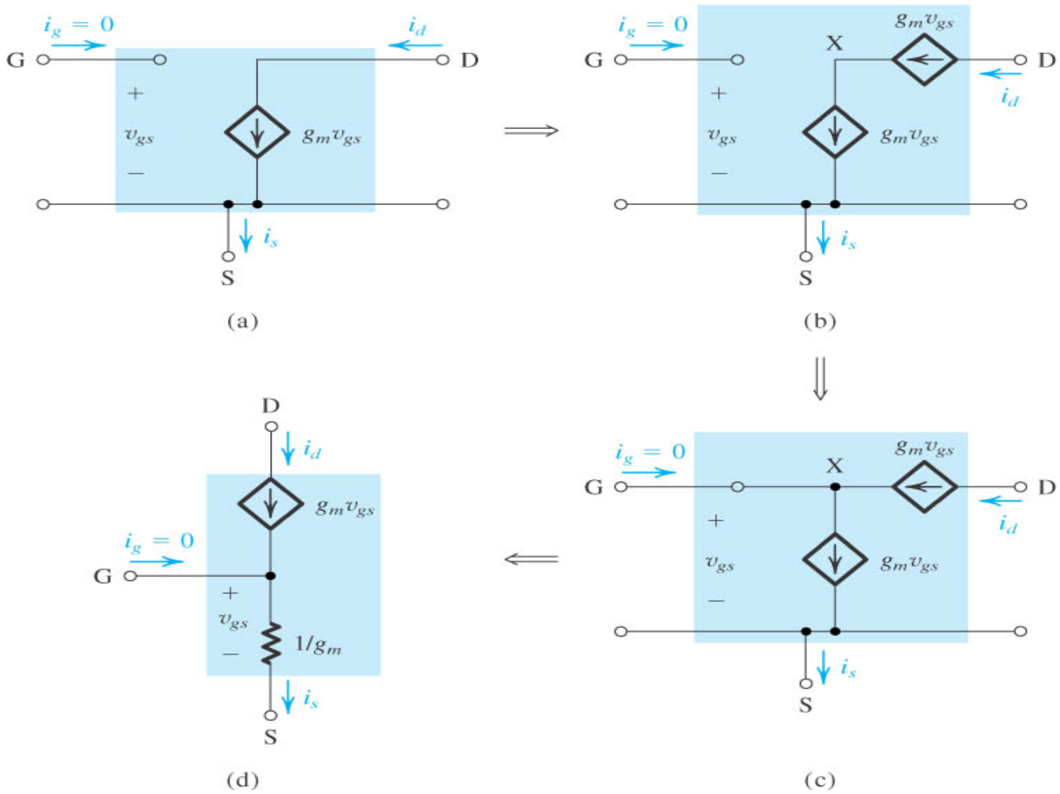


Figure 4.39 Development of the T equivalent-circuit model for the MOSFET. For simplicity, r_o has been omitted but can be added between D and S in the T model of **(d)**.

- Figure 4.39(a) shows the equivalent circuit studied above without ro.
- In figure 4.39(b) we have added a second gmvgs current source in series with the original controlled source without causing any change in circuit operation.
- This newly created circuit node, labelled X, is joined to the gate terminal G in Fig 4.39(c). The gate current does'nt change, and remains at zero.
- A controlled current source gmvgs connected across its control voltage can be represented by a resistance as long as this resistance draws an equal current as the source. This replacement is shown in fig. 4.39(d).

The resistance between gate and source looking into the source is 1/gm, and the resistance as seen from the gate is infinite.

Alternate representation- VCCS by CCCS

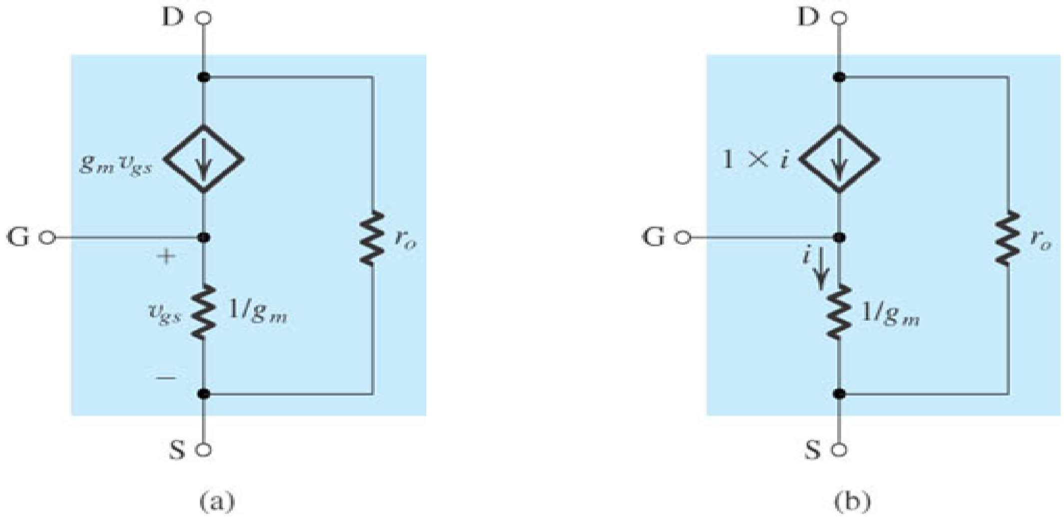


Figure 4.40 (a) The T model of the MOSFET augmented with the drain-to-source resistance r_o. (b) An alternative representation of the T model.

Modeling the Body Effect

- When source and substrate are not shorted and substrate is tied to the most negative supply in the circuit, the body effect comes into picture and the substrate acts like a second gate for the MOSFET
- The signal V_{bs} gives rise to a drain current component, written as $g_{mb}v_{bs}$, where g_{mb} is the body transconductance defined as

$$g_{mb} \equiv \left.\frac{\partial i_D}{\partial v_{BS}}\right|_{\substack{v_{GS} = \text{constant} \\ v_{DS} = \text{constant}}}$$ **where**

$$g_{mb} = \chi g_m$$ **and**

$$\chi \equiv \frac{\partial V_t}{\partial V_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}$$

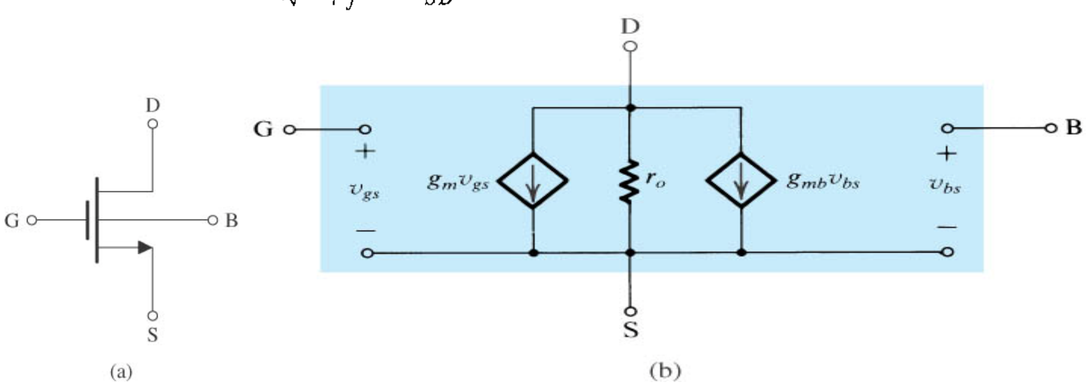


Figure 4.41 Small-signal equivalent-circuit model of a MOSFET in which the source is not connected to the body.

4.7 Single stage MOSFET Amplifiers

1. Common Source (CS) Amplifier :

A Common Source amplifier has the source terminal connected between the input and output. Input is applied between Gate –Source terminals and output is measured between the Drain-Source terminals. Any proper biasing method is used. Consider a CS amplifier with Constant current source biasing as shown below:

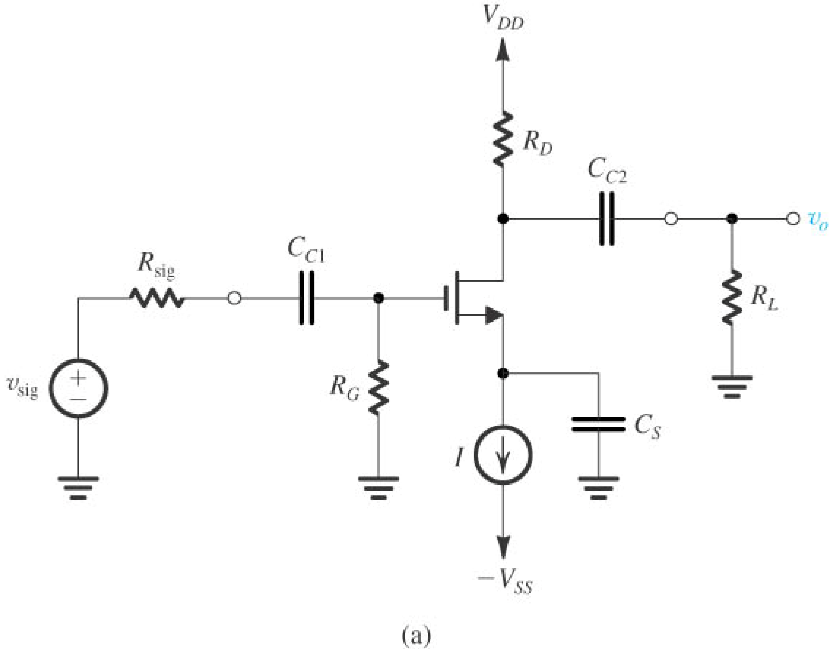


Figure 4.43 (a) Common-source amplifier

The ac equivalent circuit can be obtained by replacing the MOSFET with its small signal hybrid-π model and writing the remaining components between the respective terminals of the MOSFET in the model as shown below:

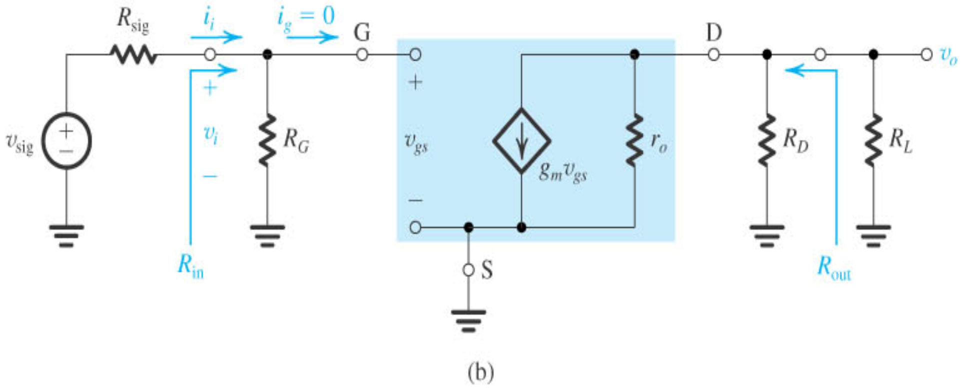


Figure 4.43 (b) Equivalent circuit of the amplifier for small-signal analysis.

Now, the electro-mathematical analysis of the CS amplifier for the voltage gain (Av), Input impedance (Zin) and Output impedance (Zout) is as shown below:

$$R_{in} = R_G$$

$$A_v = -g_m(r_o \parallel R_D \parallel R_L)$$

$$R_{out} = r_o \parallel R_D$$

$$G_v = -\frac{R_G}{R_G + R_{sig}} g_m(r_o \parallel R_D \parallel R_L)$$

Generally a Common Source amplifier will have a source resistance to improve the stability of the bias point. But this resistance also causes negative feedback and hence the voltage gain will be lesser than in a CS amplifier without source resistance.

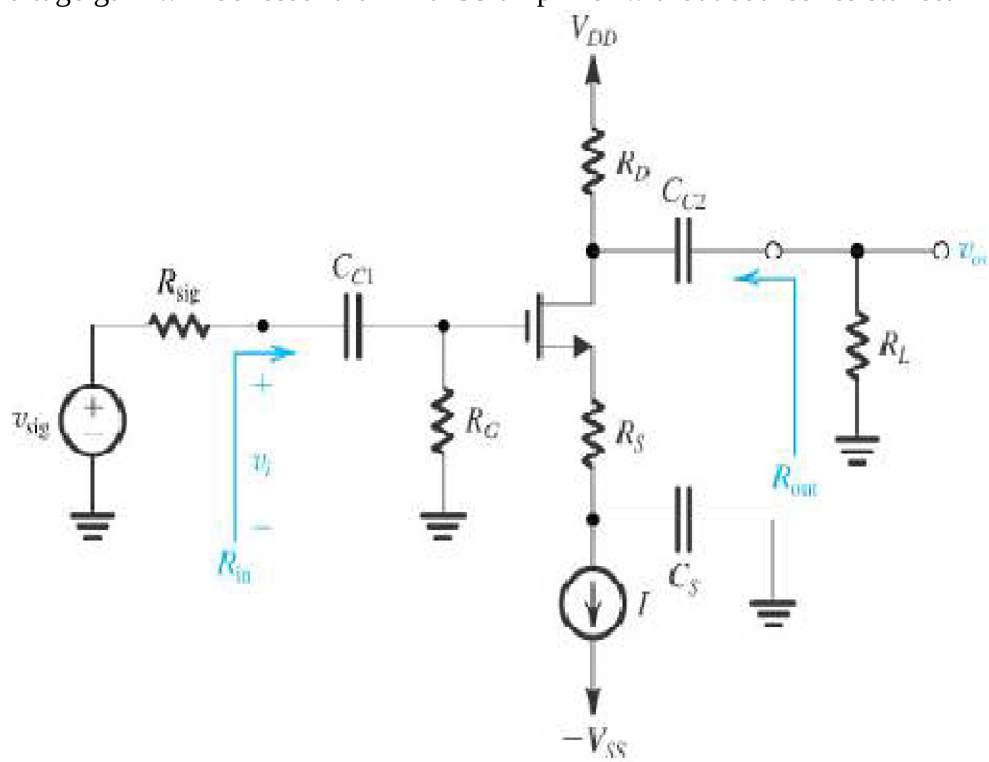


Figure 4.44 (a) Common-source amplifier with a resistance R_S in the source lead.
The small signal equivalent circuit with ro neglected is as shown below:

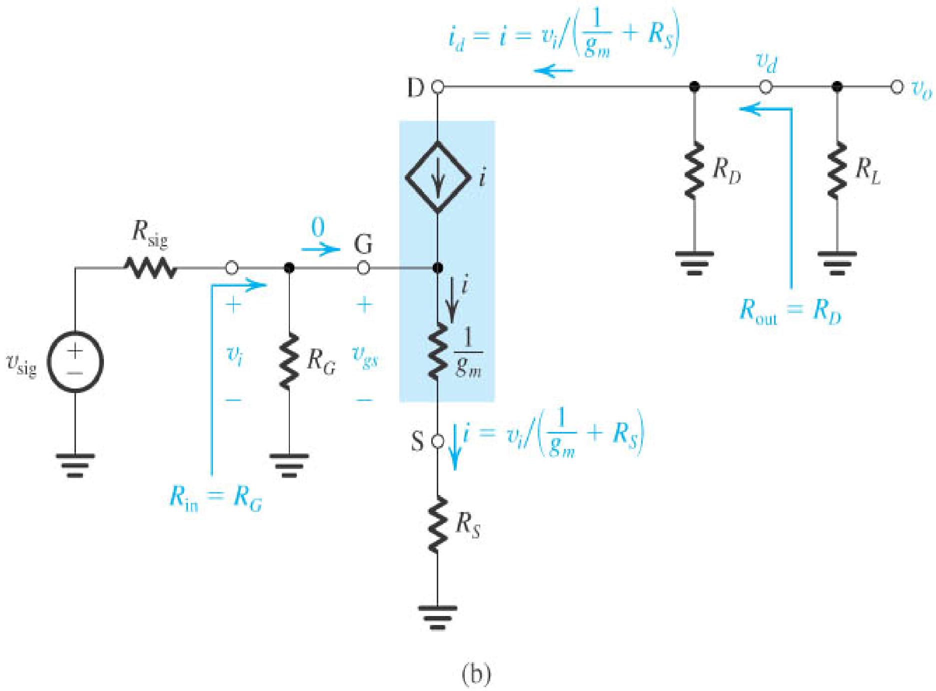


Figure 4.44 Small signal equivalent model of Common Source amplifier with R_s

From the figure we can see that as in the case of the CS amplifier,

$R_{in} = R_i = R_G$ and thus

$$V_i = V_{sig}\frac{R_G}{R_G + R_{sig}}$$

But, here unlike the previous CS circuit, v_{gs} is only a fraction of v_i .It can be determined from the voltage divider composed of $1/g_m$ and R_s that appears across the amplifier input as follows:

$$v_{gs} = v_i \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_S} = \frac{v_i}{1 + g_m R_S}$$

Hence v_{gs} can be controlled by R_S.
The current i_d is equal to the current I flowing in the source lead, thus

$$i_d = i = \frac{v_i}{\frac{1}{g_m} + R_S} = (g_m v_i)/(1 + g_m\, R_S)$$

Thus including R_S reduces i_d by the factor $(1 + g_m R_S)$.
The output is now found from

$$v_o = -i_d(R_D||R_L)$$

$$= -\frac{g_m(R_D||R_L)}{\frac{1}{g_m}+R_S} v_i$$

$$A_v = -\frac{g_m(R_D||R_L)}{\frac{1}{g_m}+R_S}$$ and setting R_L as ∞ gives

$$A_{vo} = -\frac{g_m R_D}{\frac{1}{g_m} + R_S}$$

The overall voltage gain G_v is,

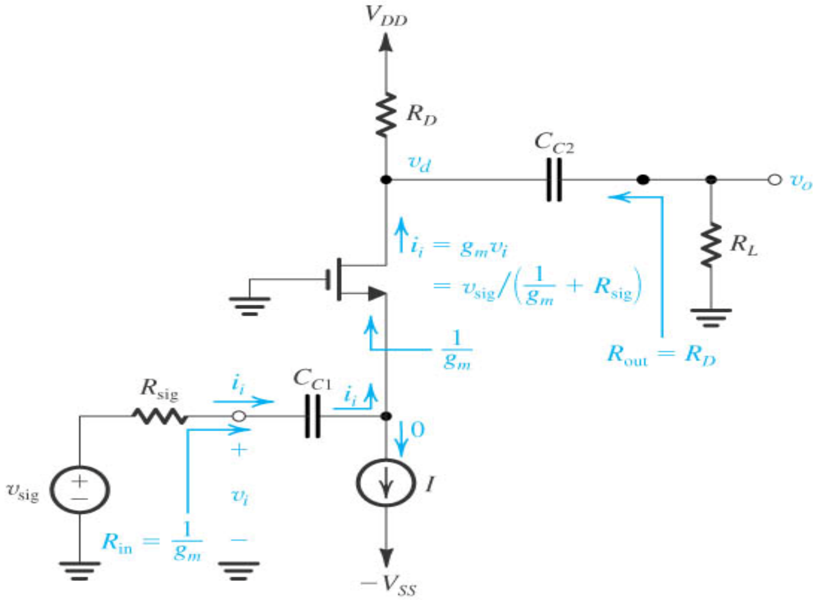
$$G_v = -\frac{R_G}{R_G + R_{sig}} \frac{g_m(R_D||R_L)}{\frac{1}{g_m} + R_S}$$

This shows that gain is reduced by a factor $(1 + g_m R_S)$ than in the previous CS amplifier without R_S.This factor is called the "amount of feedback" and that it determines both the magnitude of performance improvement and as a tradeoff, the reduction in gain. Since this R_S was used to improve the stability under dc conditions, by reducing the variability of I_D, for ac operation it has a similar action (reducing i_d), it is called "**Source degeneration resistance**".

Another useful interpretation of the gain expression is that the gain from gate to drain is simply the ratio of the total resistance in the drain, $(R_D||R_L)$ to the total resistance in the source, $[\frac{1}{g_m} + R_S]$

Common Gate Amplifier [CG amplifier]

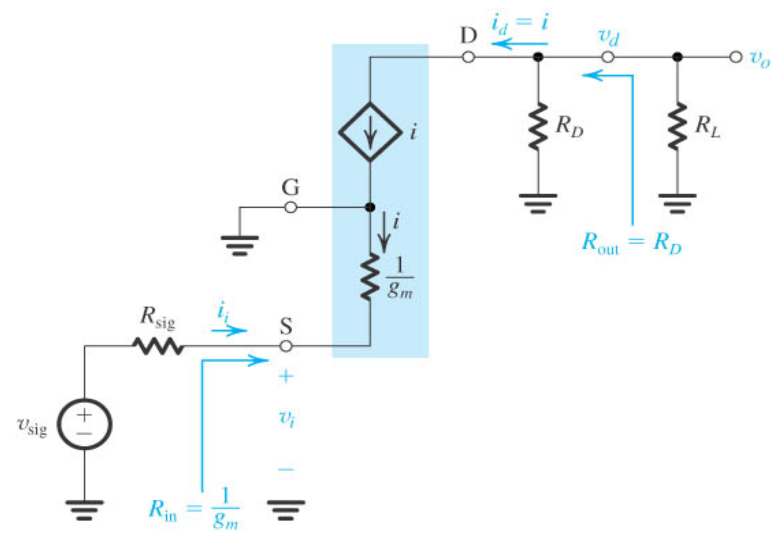
By applying a signal ground on the MOSFET gate terminal, a circuit configuration aptly named Common Gate or grounded gate amplifier is obtained. The input is applied between source and Gate and the Output is measured between the Drain and Gate. Since both the dc and ac voltages at the gate are zero, the gate terminal can be directly grounded as shown.



(a)

Figure 4.45 (a) A common-gate amplifier based on the circuit of Fig. 4.42.

The small signal equivalent circuit of the Common Gate Amplifier is as shown below. For simpler analysis we have used the T-model without considering the effect of r_o.



(b)

Figure 4.45 (b) A small-signal equivalent circuit of the amplifier in (a).

Analysis:

The input resistance is given as

$$R_{in} = \frac{1}{g_m}$$

Since g_m is of the order of 1mA/V, the input resistance of the CG amplifier is relatively low (of the order of 1kΩ) than in the CS amplifier.

$$V_i = V_{sig} \frac{R_{in}}{R_{in} + R_{sig}}$$

$$v_i = v_{sig} \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_{sig}} = \frac{v_{sig}}{1 + g_m R_{sig}}$$

The loss of signal strength in coupling the signal to input of the CG amplifier is due to the low value of R_{in}.

$$R_{sig} \ll \frac{1}{g_m}$$

The current i_i is given by,

$$i_i = \frac{v_i}{R_{in}} = \frac{v_i}{\frac{1}{g_m}} = (g_m v_i)$$

And the drain current id is

$$i_d = i = -i_i = -(g_m v_i)$$

Thus the output voltage can be found as

$$v_O = v_d - i_d(R_D||R_L) = g_m(R_D||R_L)$$

Resulting in voltage gained

$$A_v = g_m(R_D||R_L)$$

From which the open circuit voltage gain can be found as

$$A_{vo} = g_m R_D$$

The overall voltage gain can be obtained as follows:

$$G_v = \frac{R_{in}}{R_{in} + R_{sig}} A_v = A_v \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_{sig}} = \frac{A_v}{1 + g_m R_{sig}}$$

Resulting in

$$G_v = \frac{g_m (R_D || R_L)}{1 + g_m R_{sig}}$$

Finally the output resistance is found by inspection to be,

$$R_{out} = R_o = R_D$$

Note:

- The CG amplifier is non inverting
- The input resistance of CG amplifier is very low.
- Voltage gain is smaller than that of a CS amplifier by factor (1+gmRsig) which is due to low R_{in}.
- This circuit also acts like a Unity gain current amplifier or a Current follower
- This is most commonly used in the Cascode amplifier.

Common Drain Amplifier (CD amplifier)

The signal ground is established at the drain terminal, input is given between the Gate and Drain terminals and Output is measured between the Source and Drain terminals as shown below:

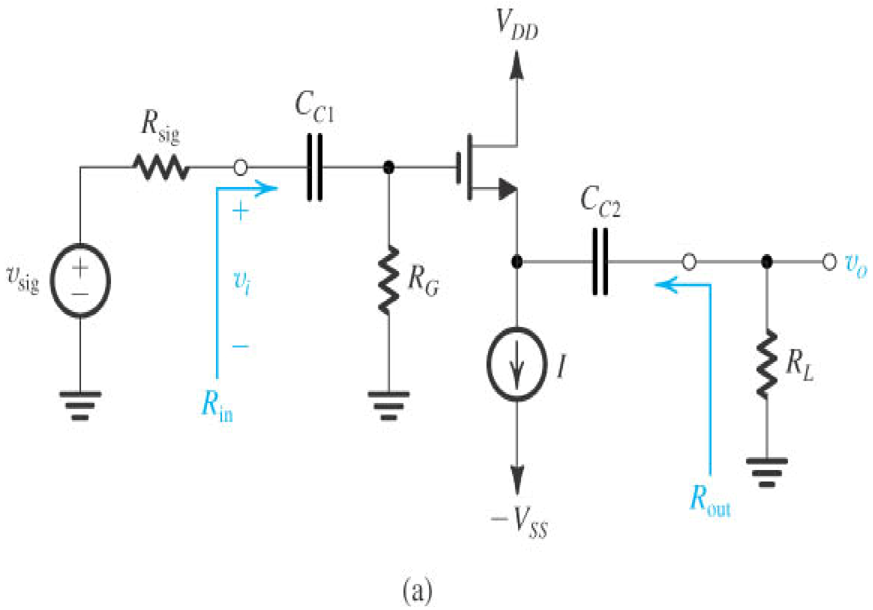


Figure 4.46 (a) A common-drain or source-follower amplifier.

Here also, it is more convenient to use the small signal T-model for analysis, but including the resistance r_o as shown below:

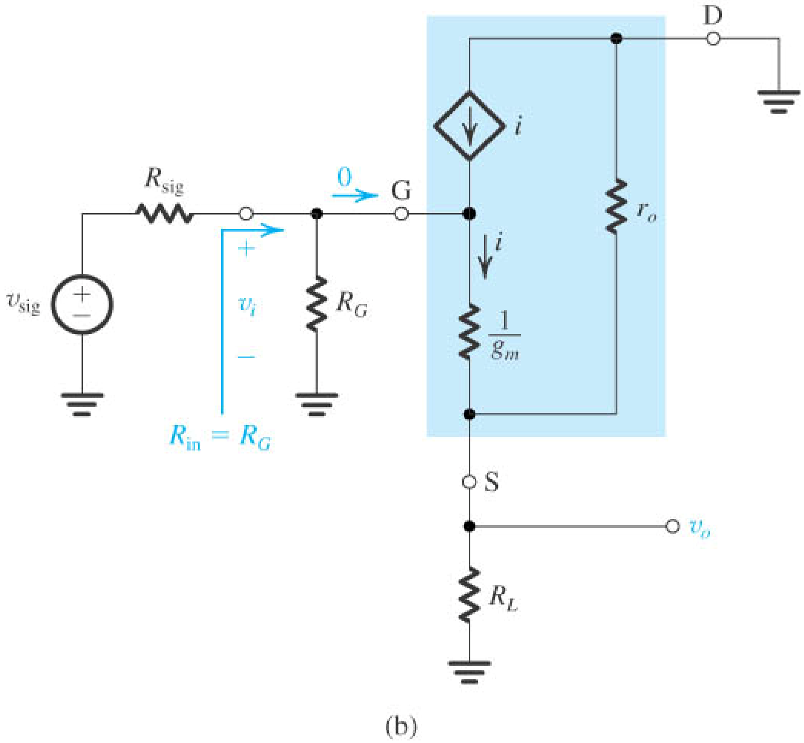


Figure 4.46 (b) Small-signal equivalent-circuit model.

Analysis:

The input resistance is given as

$R_{in} = R_G$

$V_i = V_{sig} \frac{R_{in}}{R_{in}+R_{sig}} = V_{sig} \frac{R_G}{R_G+R_{sig}}$

Usually R_G is selected to be much larger than R_{sig} with the result that

$v_i \cong v_{sig}$

$$v_O = v_i \frac{R_L \| r_o}{(R_L \| r_o) + \frac{1}{g_m}}$$

From which the voltage gain Av is obtained as

$$A_v = \frac{R_L || r_o}{(R_L || r_o) + \frac{1}{g_m}}$$

And the open circuit voltage gain A_{vo} as

$$A_{vo} = \frac{r_o}{r_o + \frac{1}{g_m}}$$

Normally $r_o \gg \frac{1}{g_m}$, causing voltage gain to become nearly unity. Thus the voltage at the source follows the voltage at the gate, giving the circuit its popular name of **source follower**. In many discrete circuits $r_o \gg R_L$ which enables the equation to be approximated by,

$$A_v \cong \frac{R_L}{R_L + \frac{1}{g_m}}$$

The overall voltage gain Gv can be found as,

$$G_v = \frac{R_G}{R_G + R_{sig}} \frac{R_L || r_o}{(R_L || r_o) + \frac{1}{g_m}}$$

Which approaches unity for $R_G \gg R_{sig}$, $r_o \gg R_L$ and $r_o \gg \frac{1}{g_m}$

The circuit for determining the output resistance R_{out} is as shown in figure. Because the gate voltage is now zero, looking back into the source, we see between the source and ground a resistance $\frac{1}{g_m}$ in parallel withr_o, thus

$$R_{out} = \frac{1}{g_m} || r_o$$

Normally$r_o \gg \frac{1}{g_m}$, reducing R_{out} to

$$R_{out} \cong \frac{1}{g_m}$$

Which indicates R_{out} will be moderately low.

Note:

- In source follower, R_{in} is independent of R_L and R_{out} is independent of R_{sig}, due to zero gate current.
- Hence, it has a very high input resistance, very low output resistance and a voltage gain that is less than or close to unity.
- It is normally used as a buffer amplifier.

Summary:

- The CS amplifier is best suited for obtaining the bulk of the gain required in an amplifier. Depending on the gain required, either a single stage or a cascade of two or three stages is used.
- Including a resistor R_S in the source terminal of the CS amplifier provides a number of improvements in its performance, as it behaves like an amplifier with negative Voltage series feedback amplifier, but at the expense of reduced gain.
- The low input resistance of the CG amplifier is used as unity gain current amplifier or current follower and also in Cascode amplifier.
- The source follower finds application as a voltage buffer for connecting a high resistance source to a low resistance load and as the output stage in a multistage amplifier.

PN: For SPICE MOSFET models and examples please refer to pages 446 to 453 in the text book Adel Sedra and K C Smith

Solutions to few selected exercise problems

Refer page 455 to 466 for the problem statements

4.1 The capacitance per unit area is

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$\varepsilon_{ox} = 3.45 * 10^{-11}\ F/m$$

$$t_{ox} = 5nm$$

$$C_{ox} = \frac{3.45*10^{-11}}{5nm} = 6.9fF/\mu m^2$$

For $t_{ox} = 5nm,\ C_{ox} = 0.56\ fF/\mu m^2$

For a capacitance of 1pF, we require an area A:

$$A = \frac{10^{-12}}{6.9\times10^{-15}} = 145\ \mu m^2\ for\ t_{ox} = 5nm$$

$$A = \frac{10^{-12}}{0.56\times10^{-15}} = 1163\ \mu m^2\ for\ t_{ox} = 20nm$$

For a square plate capacitor of 10pF,

$$A = 10 \times 145 = 1450\ \mu m^2\ for\ t_{ox} = 5nm$$
$$A = 10 \times 1163 = 11630\ \mu m^2\ for\ t_{ox} = 20nm$$

4.2 Drain current is directly proportional to the width of the channel.Therefore if width is 10 times greater, then i_D would be 10 times greater as well.

K = constant of proportionality = $\frac{1}{0.5\times0.2} = 10mA/V^2$

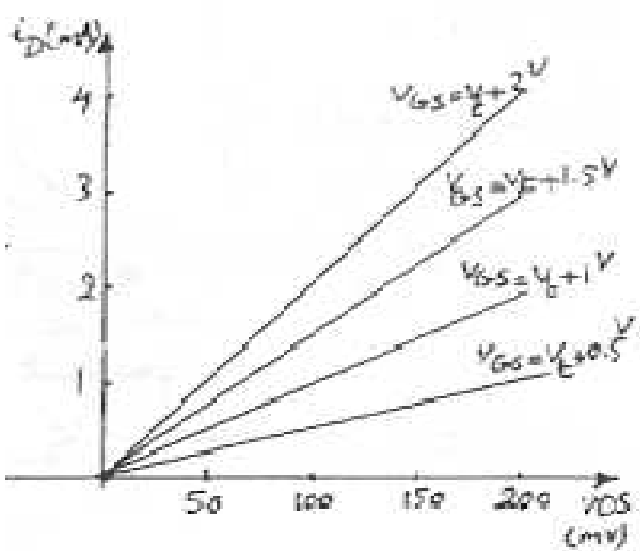
$$r_{DS} = \frac{i_D}{v_{DS}} = \frac{1}{0.2} = 5k\Omega\ for\ V_{ov} of\ 0.5V$$

$$r_{DS} = \frac{i_D}{v_{DS}} = \frac{1}{0.5} = 10k\Omega\ for\ V_{ov} of\ 1V$$

$$r_{DS} = 15k\Omega\ for\ V_{ov} of\ 1.5V$$

$$r_{DS} = 20k\Omega\ for\ V_{ov} of\ 2V$$

$$5k\Omega \le r_{DS} \le 20k\Omega\ for\ 0.5V \le V_{ov} \le 2V$$



4.3

We know that

$$i_D = \frac{1}{2}k_n'(v_{GS} - V_t)^2$$

$$k_n' = \mu_n C_{ox}$$

For equal drain currents,

$$\mu_n C_{ox}\frac{W_n}{L} = \mu_n C_{ox}\frac{W_p}{L}$$

$$\frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} = \frac{1}{0.4} = 2.5$$

4.34

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{5-0}{R_D} = 1mA$$

$$R_D = 5k\Omega$$

$$v_D = v_G \; implies \; Saturation$$

Therefore

$$i_D = \frac{1}{2}k_n'(v_{GS} - V_t)^2$$

$$1 = \frac{1}{2} \times 60 \times 10^{-3} \times \frac{100}{3}(v_{GS} - 1)^2$$

Implies $v_{GS} = 2V \; and \; V_s = -2V$

$$R_S = \frac{-2-(-5)}{1} = 3K\Omega$$

NOTE: PLEASE REFER TO ALL THE EXAMPLE PROBLEMS IN PRESCRIBED TEXT BOOK {SEDRA AND SMITH}

ALL THE BEST
