http://www.academia.edu/5272241/The_ECE_218_Analog_VLSI_Circuit_Design_CMOS_Operational_Amplifier

http://iasir.net/IJETCASpapers/IJETCAS13-335.pdf

http://www.aicdesign.org/SCNOTES/2010notes/Lect2UP250_%28100328%29.pdf

AMI C5N 0.6 µm bkabka

http://www.joace.org/uploadfile/2014/0310/20140310043126523.pdf

http://www.groupes.polymtl.ca/gbm8320/CADENCE_Manual.pdf

http://docslide.us/documents/cmos-opamp-low-power-2012.html

The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits

Nano-CMOS Circuit and Phjkljkklklklysical Design

Par Ban Wong,Anurag Mittal,Yu Cao,Greg W. Starr

Design of CMOS Operational Amplifiers (Artech House Microwave Library)

Rasoul Dehghani Author

https://books.google.fr/books?id=QRf0o477nBsC&pg=PA56&lpg=PA56&dq=cmos+op+amp+systematic+offset&source=bl&ots=aEWkM6LYWA&sig=QpEnr5AeJpi_XE1T2FgoCK4xYw8&hl=fr&sa=X&ei=PGJYVYnECouAU6v_gKAL&ved=0CCAQ6AEwADgK#v=onepage&q=cmos%20op%20amp%20systematic%20offset&f=false

Input Offset Voltage

- *Random offset*: device mismatches as random in nature
- Systematic offset: due to design technique ⇨ predictable

If the input stage is perfectly balanced, then V_{DS4} = V_{DS3} = V_{GS4}.

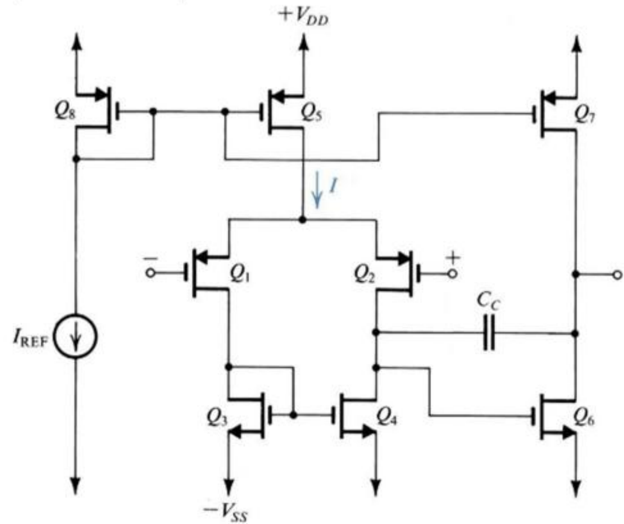
⇨ V_{GS4} = V_{GS6}, hence $I_6 = \frac{(W/L)_6}{(W/L)_4} I_4 = \frac{(W/L)_6}{(W/L)_4} \frac{I}{2}$

In order for no offset voltage to appear at the output, then I_6 = I_7.

Since $I_7 = \frac{(W/L)_7}{(W/L)_5} I$

$$\Rightarrow \quad \frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5}$$

If this condition is not met, a systematic offset will result.



Transistor	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
W/L	120/8	120/8	50/10	50/10	150/10	100/10	150/10	150/10

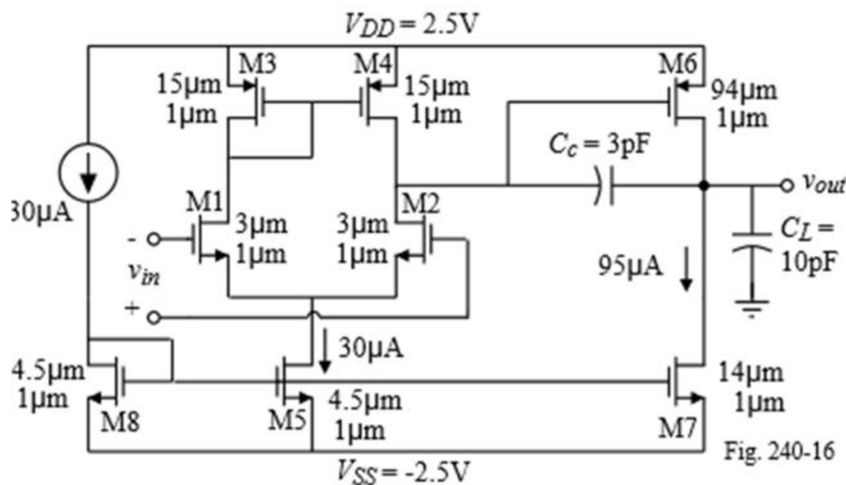


Fig. 240-16

Vt: nodal voltage (transient analysis)
It: terminal current (transient analysi
Vf: nodal voltage (AC analysis)
If: terminal current (AC analysis)
Vs: nodal voltage (DC sweep)
Is: terminal current (DC sweep)
Vdc: nodal voltage (quiescent value)

CMOS Differential Amplifiers

Page 257 to page 259,Ken Martin's book:

for the wide-swing cascode current mirror,the L of the bottom transistors are less than the top.

I have seen some design circuits, the L of the bottom transistors are larger than that of the top transistors.
I get confused.

DC Balance Conditions for the Two-Stage Op Amp

For best performance, keep all transistors in saturation.

M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages.

Therefore, we develop conditions to force M4 to be in saturation.

1.) First *assume* that $V_{SG4} = V_{SG6}$. This will cause "proper mirroring" in the M3-M4 mirror. Also, the gate and drain of M4 are at the same potential so that M4 is "guaranteed" to be in saturation.

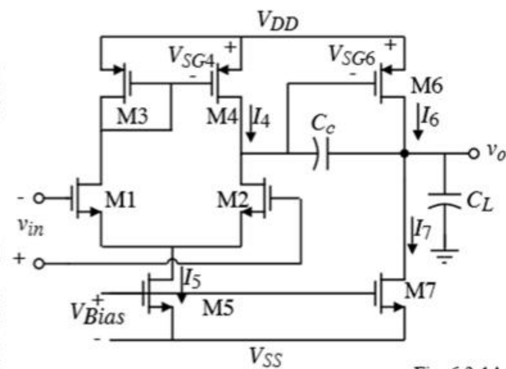


Fig. 6.3-1A

2.) *If* $V_{SG4} = V_{SG6}$, then $I_6 = \left(\frac{S_6}{S_4}\right) I_4$

3.) However, $I_7 = \left(\frac{S_7}{S_5}\right) I_5 = \left(\frac{S_7}{S_5}\right)(2I_4)$

4.) For balance, I_6 must equal I_7 $\Rightarrow$ $\boxed{\frac{S_6}{S_4} = \frac{2S_7}{S_5}}$ called the "balance conditions"

5.) So if the balance conditions are satisfied, then $V_{DG4} = 0$ and M4 is saturated.

from the model file, for nominal process corner, the specified values are as follows

parameter NMOS PMOS

tox 1.39e-8m 1.39e-8m

Cox(from tox) 2.484e-3F/m^2 2.484e-3F/m^2

un 458.43e-4m^2/Vs 212.02e-4m^2/Vs

Kn/Kp(=uncox) 113.88uA/V^2 52.66uA/V^2

You can also extract these parameters by running simulations.

You can find a very good approach in. They guide you through the process of extracting device parameters via measurements or simulation.

MOSFET Constants and Parameters

Constants for Silicon:

Constant Symbol	Constant Description	Value	Units
V_G	Silicon bandgap (27°C)	1.205	V
k	Boltzmann s constant	1.381×10^{-23}	J/K
n_i	Intrinsic carrier concentration (27°C)	1.45×10^{10}	cm^{-3}
ε_0	Permittivity of free space	8.854×10^{-14}	f/cm
ε_{si}	Permittivity of silicon	$11.7\ \varepsilon_0$	F/cm
ε_{ox}	Permittivity of SiO_2	$3.9\ \varepsilon_0$	F/cm

Model Parameters for a Typical CMOS Bulk Process (0.8 m CMOS n-well):

Parameter Symbol	Parameter Description	Typical Parameter Value N-Channel	Typical Parameter Value P-Channel	Units
V_{T0}	Threshold Voltage ($V_{BS} = 0$)	0.7 ± 0.15	-0.7 ± 0.15	V
K'	Transconductance Parameter (in saturation)	$110.0 \pm 10\%$	$50.0 \pm 10\%$	$\mu A/V^2$
γ	Bulk threshold parameter	0.4	0.57	$(V)^{1/2}$
λ	Channel length modulation parameter	0.04 (L=1 μm) 0.01 (L=2 μm)	0.05 (L = 1 μm) 0.01 (L = 2 μm)	$(V)^{-1}$
$2\lvert\phi_F\rvert$	Surface potential at strong inversion	0.7	0.8	V

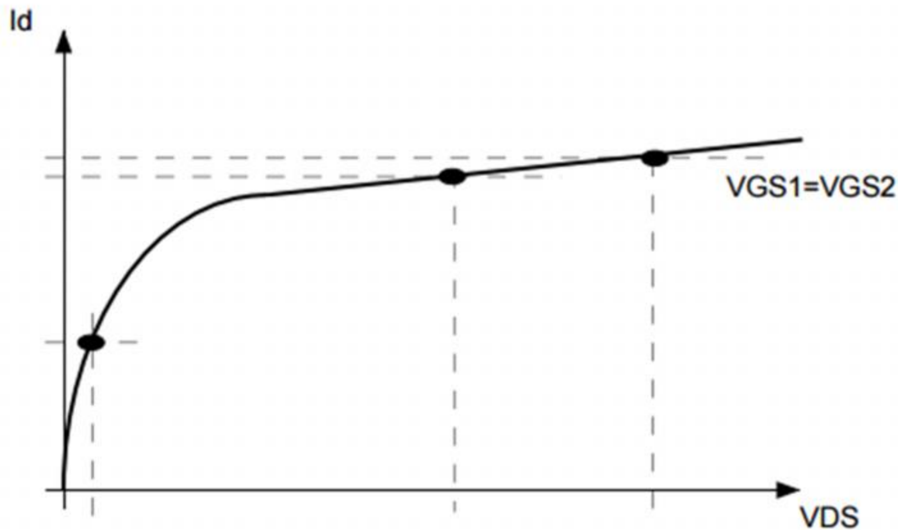
Miroir de courant simple

Voici les paramétres qui influent sur la précision

- Channel length modulation (λ)
- Threshold offset
- Parasitic resistances
- Imperfect geometrical matching and current mobility variation

- Channel length modulation (λ)

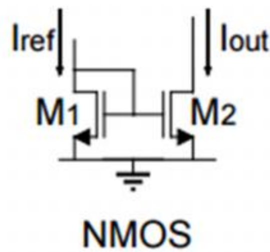
$$\frac{I_{out}}{I_{Ref}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

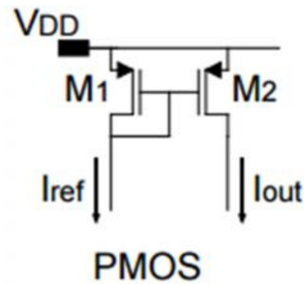


It can be improved by increasing the output resistance.

- use of large L (typically current mirrors are not realized with th eminimum technological L. This can results in a large capacitance at the output node)

Gain en courant





- M1 operates in saturation

$$I_{Ref} = I_1 = \frac{k'}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH})^2\ (1 + \lambda V_{DS1})$$

$$V_{DS1} = V_{GS1} = V_{GS2}$$

- If M2 operates in saturation

$$I_{out} = I_2 = \frac{k'}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH})^2\ (1 + \lambda V_{DS2})$$

$$I_{out} = I_{Ref}\,\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\,\frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})}$$

$Vds1 \neq Vds2$ donc le matching entre M1 et M2 est mauvais

Miroir de courant cascoded

$Vds1 = Vds2$ donc la recopie est précise

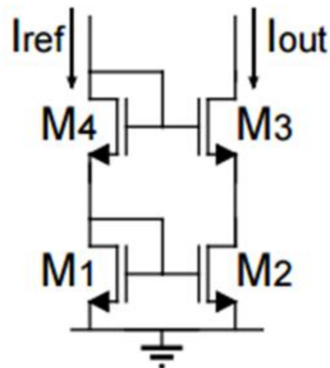
Factors affecting the mirror accuracy

Channel length modulation (λ)

Use of long device (large L) to increase rout

Use of large (VGS – VTH) for good matching (small importance of VTH mismatch)

use of large L (typically current mirrors are not realized with th eminimum technological L. This can results in a large capacitance at the output node)



$$V_{DS1} = V_{DS2} + V_{GS3} - V_{GS4}$$

$$V_{DS1} = V_{DS2} \quad \text{if} \quad V_{GS3} = V_{GS4}$$

$$\frac{I_{out}}{I_{Ref}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}$$

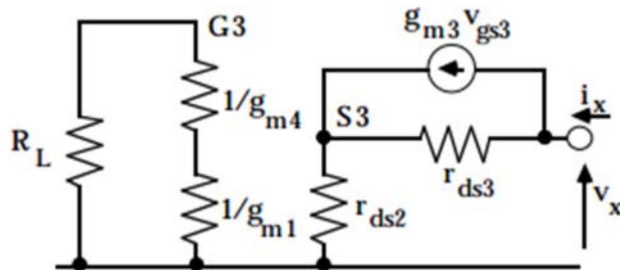
- The current gain is accurate
- For large current (i.e. with $(W/L)_{M2}$ large) it allows to decrease the output capacitance using $(W/L)_{M3}$ small.

VDS1 = VGS3 –VGS4+VDS2 =VDS2

Output impedance

- The output resistance is increased without feedback.

Small signal equivalent circuit



$$i_x = g_{m3}\, v_{GS3} + (v_x - v_{S3})/r_{ds3}$$

$$i_x = v_{S3}/r_{ds2}$$

$$i_x = g_{m3}\,(-v_{S3}) + (v_x - v_{S3})/r_{ds3}$$

$$i_x = v_{S3}/r_{ds2}$$

$$r_{out} = r_{ds2} + r_{ds3} + r_{ds3}\, g_{m3}\, r_{ds2} \cong r_{ds3}\, g_{m3}\, r_{ds2}$$

Wide Swing Cascode Current Mirror

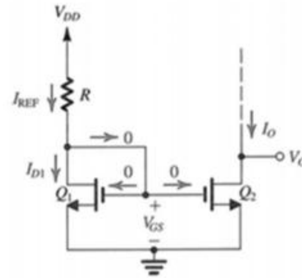
6.4 IC Biasing

Basic MOSFET current source

- MOSFET current mirror
  - Widely used for ICs with good device matching
  - Q_1 and Q_2 are identical and in saturation:

$$I_{D1} = I_{REF} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1 (V_{GS} - V_{tn})^2 = \frac{V_{DD} - V_{GS}}{R}$$

$$I_O = I_{D2} = I_{REF}$$

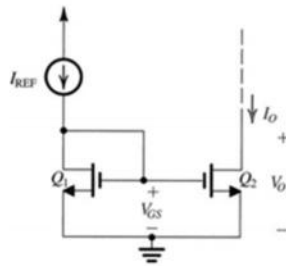


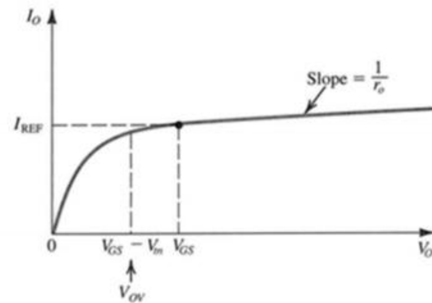
  - Current gain or **current transfer ratio**:

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

- Effect of V_O on I_O
  - Current mismatch due to channel-length modulation

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF}\left(1 + \frac{V_O - V_{GS}}{V_{A2}}\right)$$





Tradeoffs and Optimization in Analog CMOS Design

Par David Binkley

cmos differential amplifier analysis

current mirror channel length modulation

Transistor bloqué

$v_{GS} \leq 0 \quad \Rightarrow \quad i_D = 0$

Inversion faible

$V_{eff} \leq 0 \quad (v_{GS} \leq V_{tn}) \quad \Rightarrow \quad i_D \approx 0$

Inversion forte, régime triode

$V_{eff} \geq 0 \quad (v_{GS} \geq V_{tn})$ et $v_{DS} \leq V_{eff} \quad \Rightarrow \quad i_D = k'_n.(W/L).[(v_{GS} - V_{tn}).v_{DS} - v_{DS}^2/2)]$

Inversion forte, régime saturé

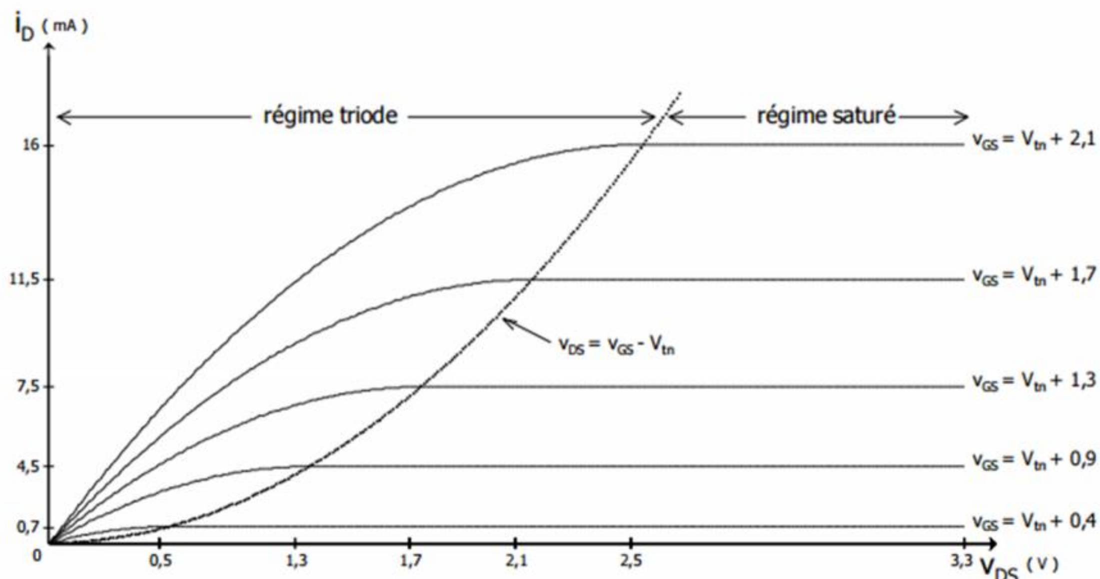
$V_{eff} \geq 0$ et $v_{DS} \geq V_{eff} \quad \Rightarrow \quad i_D = 1/2.k'_n.(W/L).(v_{GS} - V_{tn})^2$

Avec :

V_{tn}	tension de seuil du NMOS	(V)

$V_{eff} = v_{GS} - V_{tn}$	tension grille – source effective	(V)
$k'_n = \mu_n.C_{ox}$	facteur de gain du NMOS	($\mu A/V^2$)
μ_n	mobilité des électrons	(cm^2/Vs)
C_{ox}	capacité surfacique de grille	(F/cm^2)
W	largeur de grille du transistor	(μm)
L	longueur de grille du transistor	(μm)

La figure i.4 donne la caractéristique $i_D - v_{DS}$ d'un NMOS pour différents v_{GS} (L=0,35 µm W= 10µm).

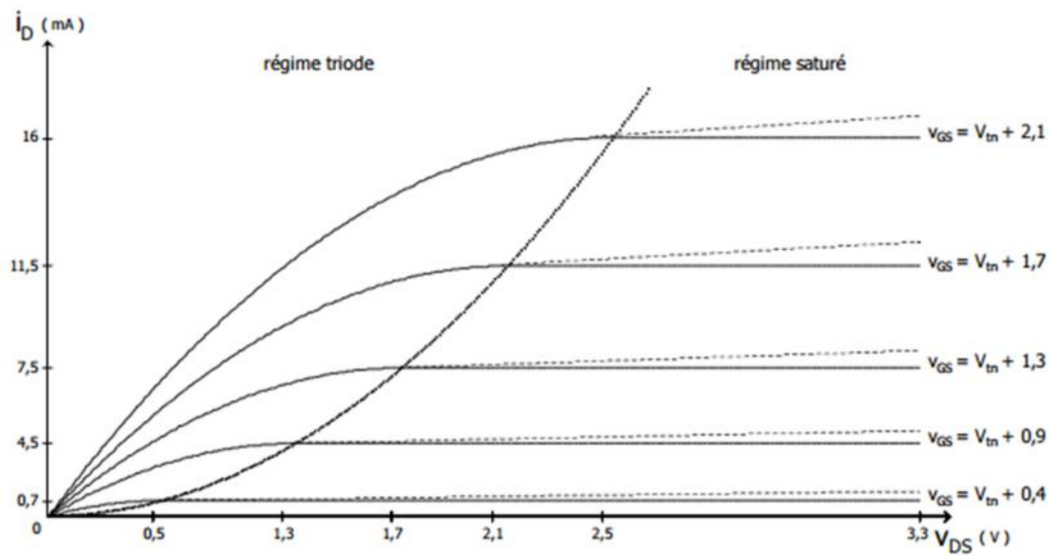


i.4. Caractéristique $i_D - v_{DS}$ d'un NMOS.

La modélisation précédente est une modélisation au premier ordre (c'est à dire grossière), elle est utilisée en première approche pour les calculs manuels simples permettant la compréhension du fonctionnement de circuits élémentaires. En particulier en régime saturé le courant i_D augmente légèrement avec v_{DS} du fait du pincement du canal et de la modulation de la longueur effective de ce dernier (cf. cours physique des semi-conducteurs), on modélise cet effet en réécrivant l'équation de i_D :

$$i_D = 1/2.k'_n.(W/L).(v_{GS} - V_{tn})^2.(1 + \lambda.v_{DS})$$

avec λ constante positive telle que $\lambda = 1/V_A$, V_A étant la "tension d'Early" du transistor (par analogie avec le bipolaire). La figure i.5 reprend la caractéristique $i_D - v_{DS}$ précédente, est représenté en pointillés les modifications apportées au régime saturé. La pente de la caractéristique en régime saturé est $1 / r_0$, r_0 étant alors la résistance de sortie du MOS (celle-ci est en effet finie).



i.5. Caractéristique $i_D - v_{DS}$ d'un NMOS intégrant la modulation de la longueur du canal en régime saturé.

http://www.mines-stetienne.fr/~dutertre/documents/1_cours_diode_final_web.pdf

modulation de la largeur du canal