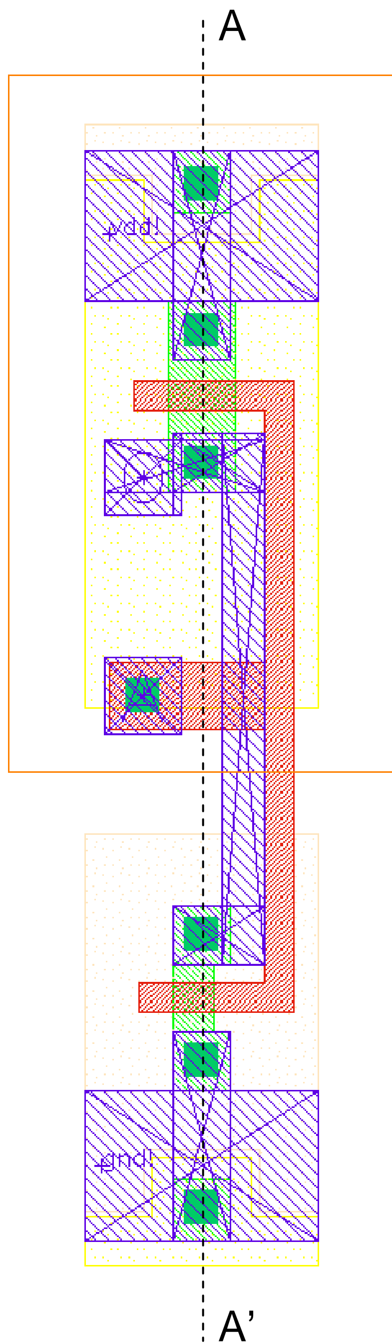
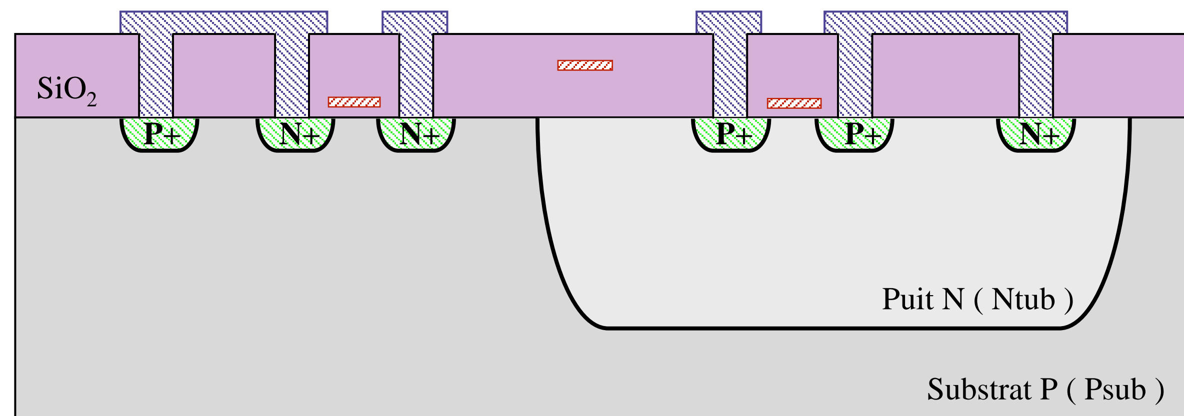
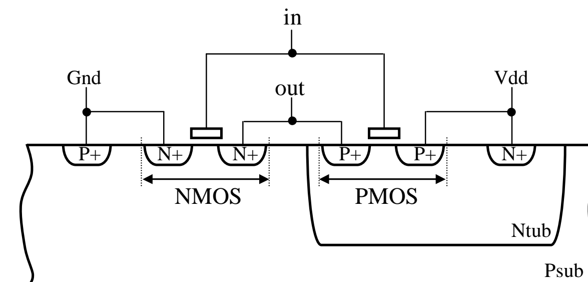
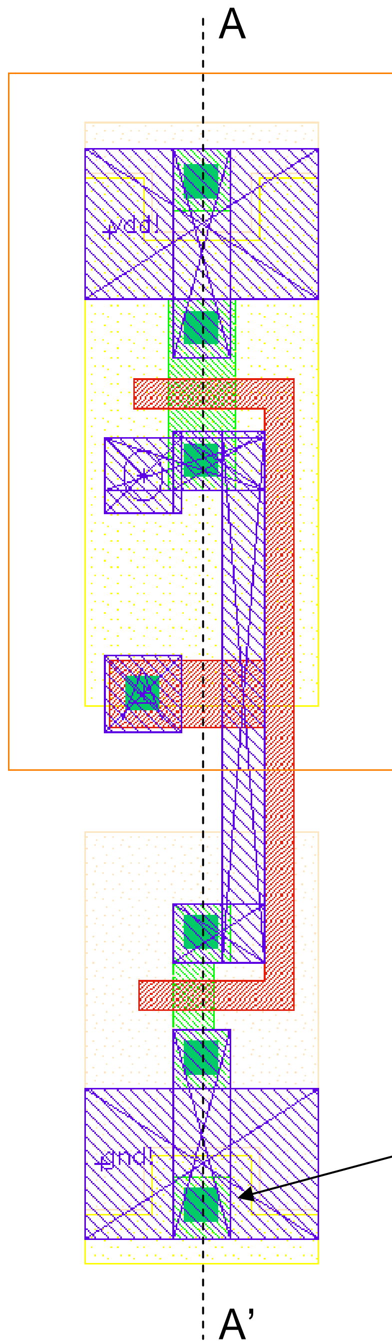
Réalisation d'un inverseur dans un process CMOS

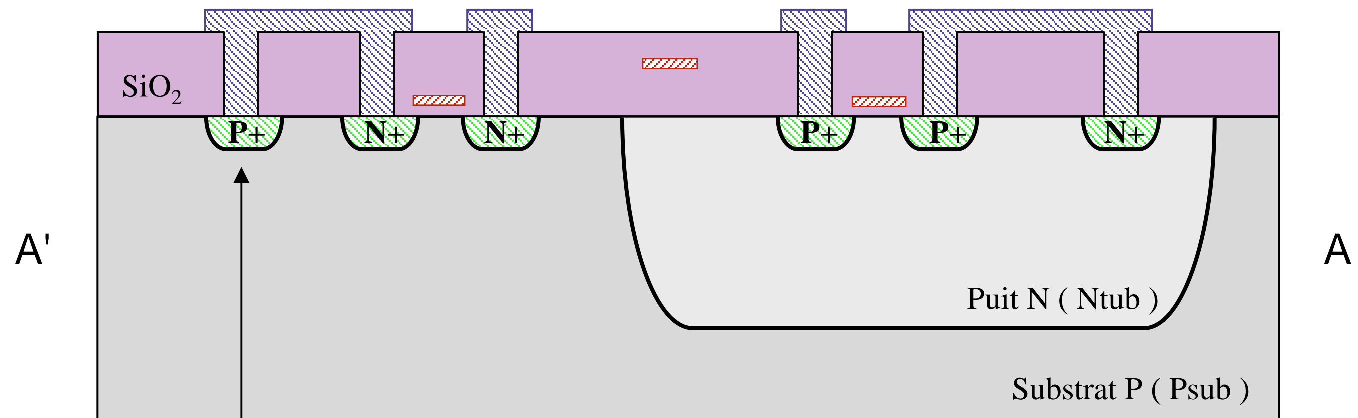






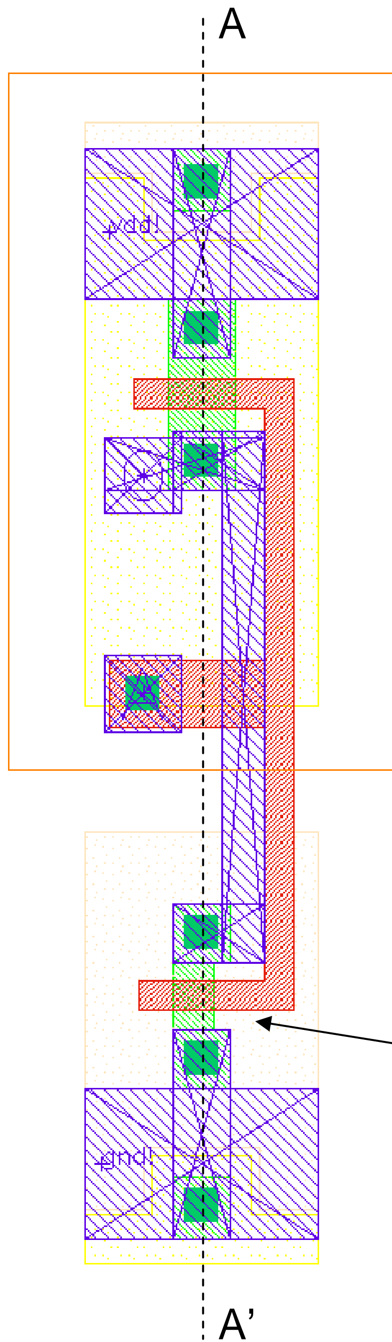
Réalisation d'un inverseur dans un process CMOS

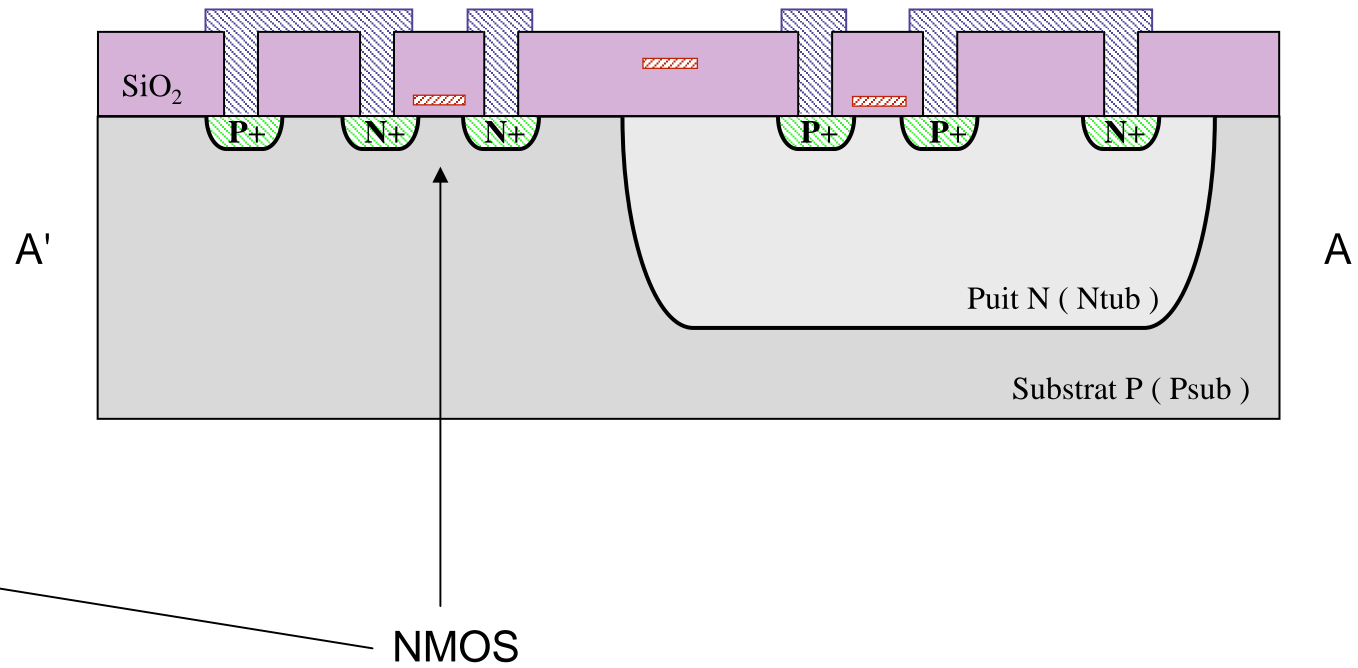


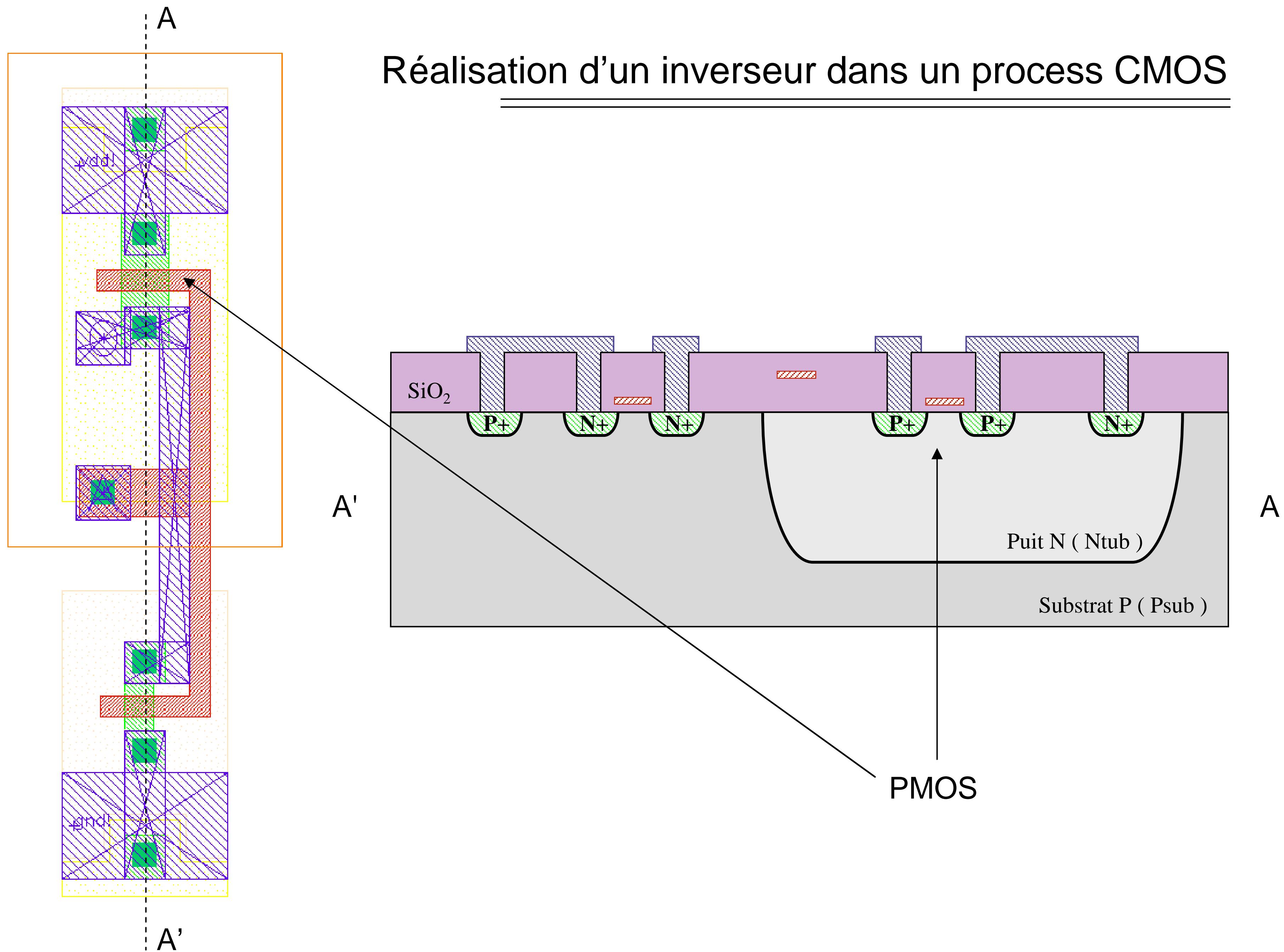


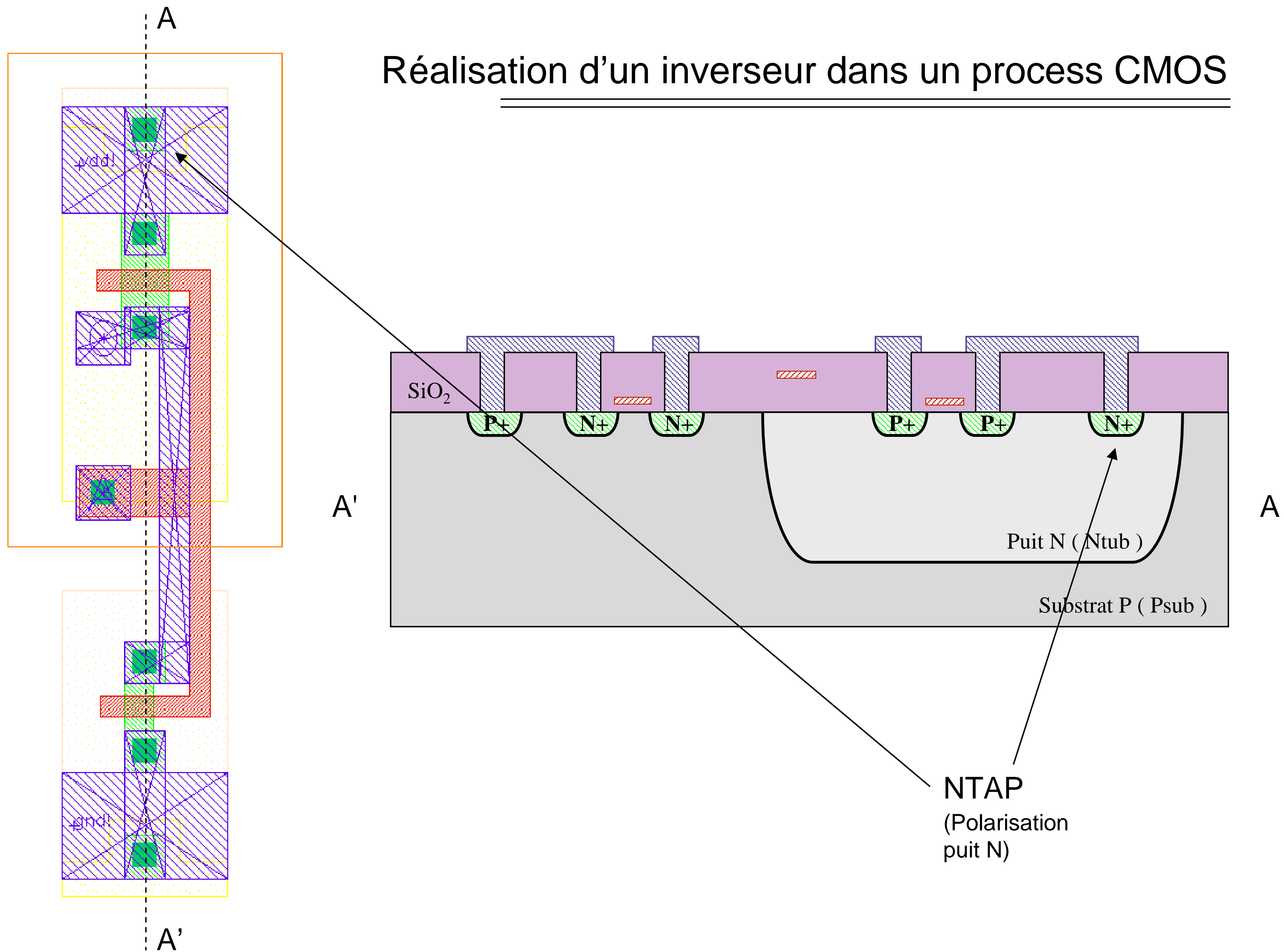
PTAP
(Polarisation substrat)

Réalisation d'un inverseur dans un process CMOS

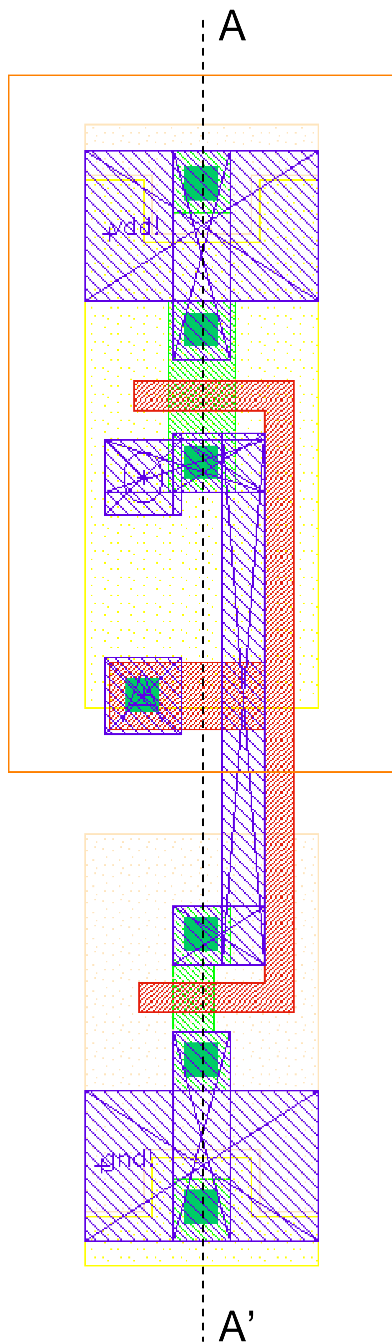


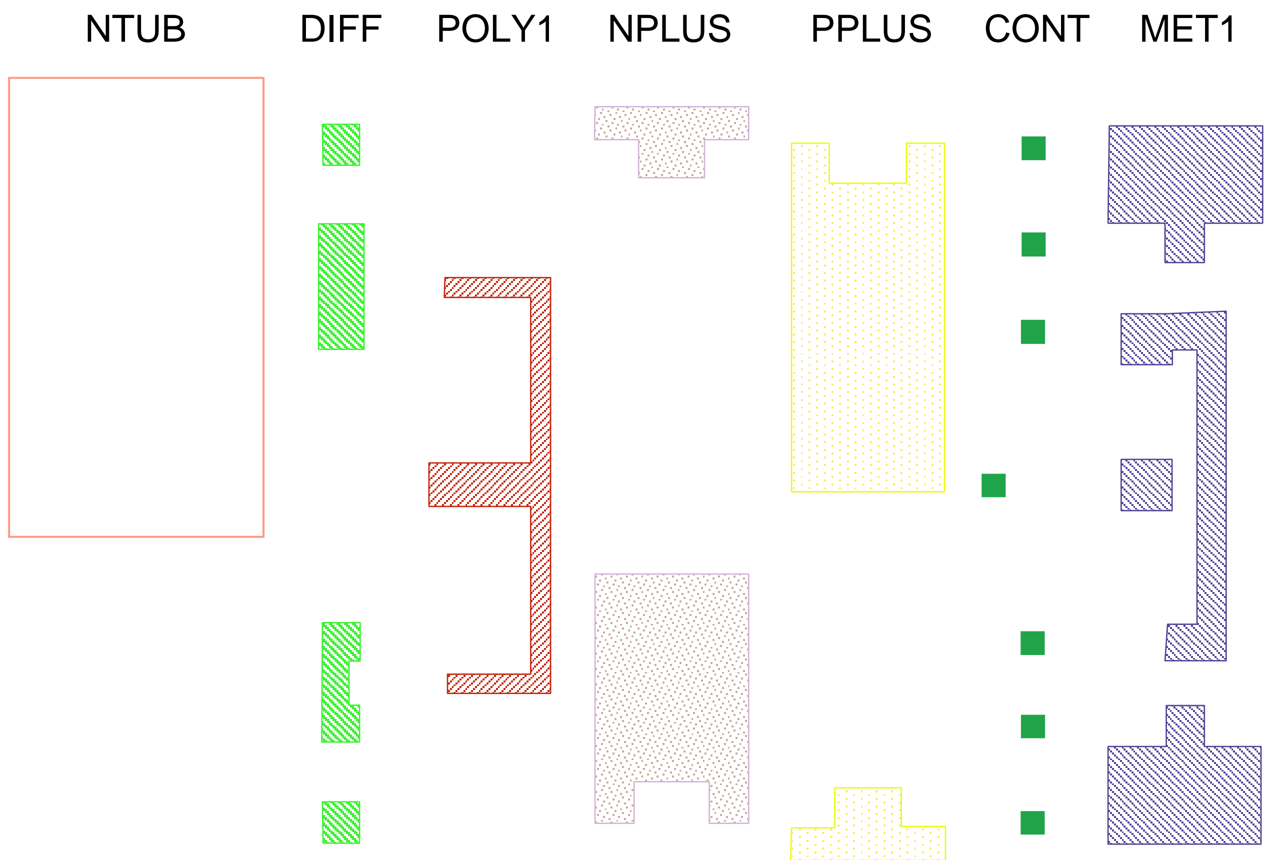


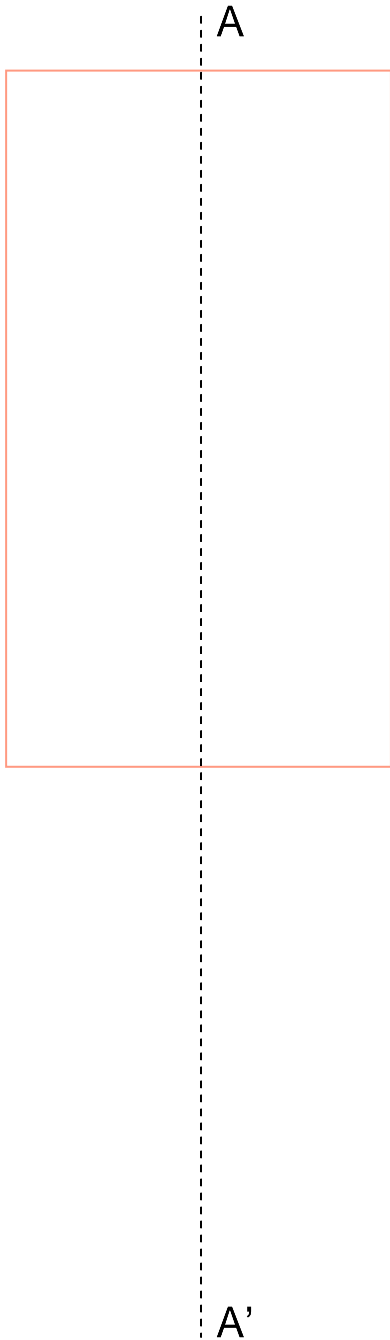

A
Réalisation d'un inverseur dans un process CMOS
vdd!
SiO$_2$
P+
N+
N+
P+
P+
N+
A'
A
Puit N (Ntub)
Substrat P (Psub)
PMOS
gnd!
A'


A
Réalisation d'un inverseur dans un process CMOS
vdd!
SiO$_2$
P+
N+
N+
P+
P+
N+
A'
A
Puit N (Ntub)
Substrat P (Psub)
gnd!
NTAP
(Polarisation
puit N)
A'

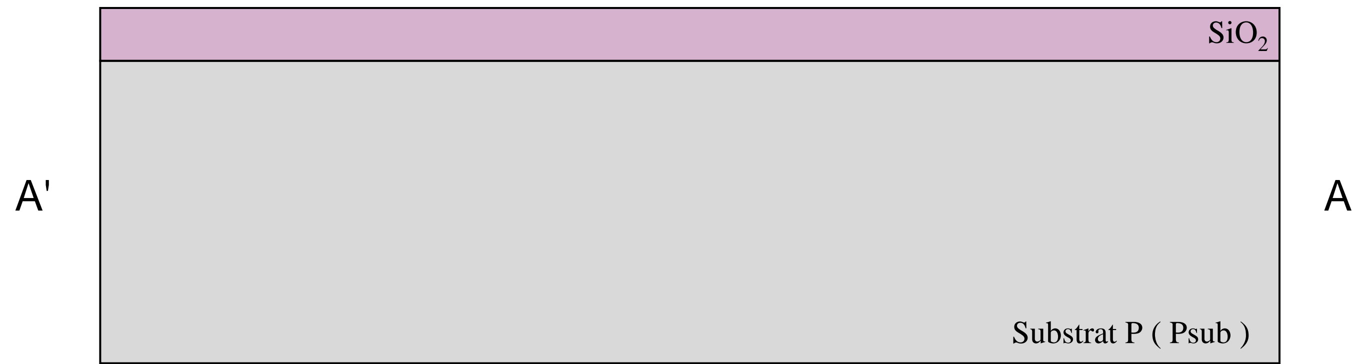
Réalisation d’un inverseur dans un process CMOS



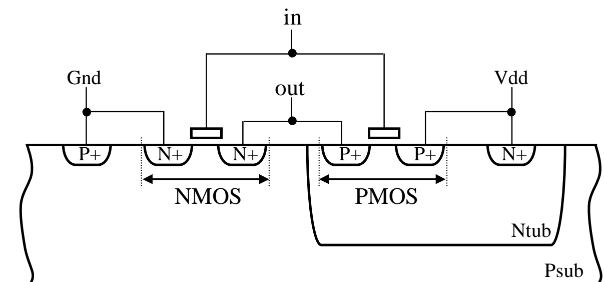


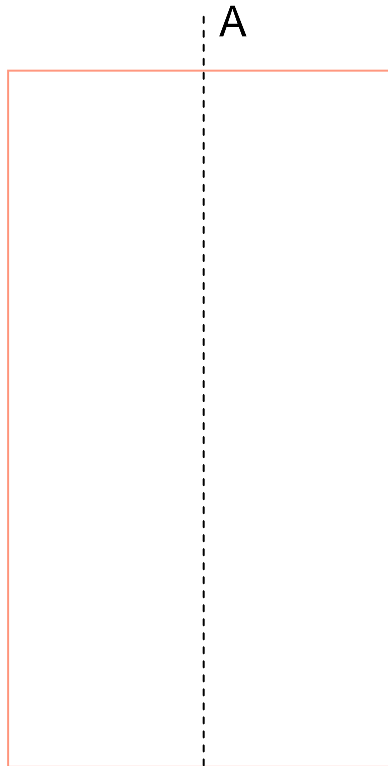


Ouverture du puit N (Ntub)

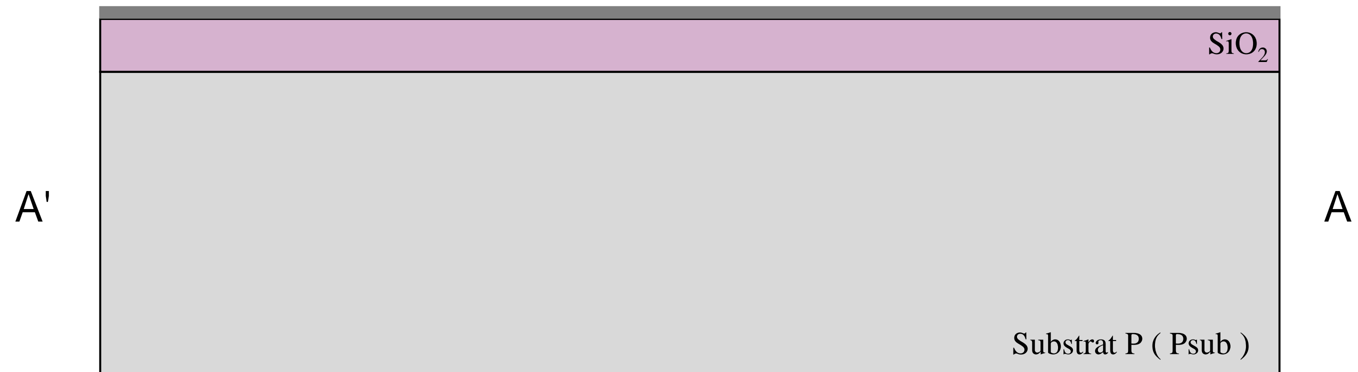


1. Dépôt d’une couche de SiO_2 protectrice.

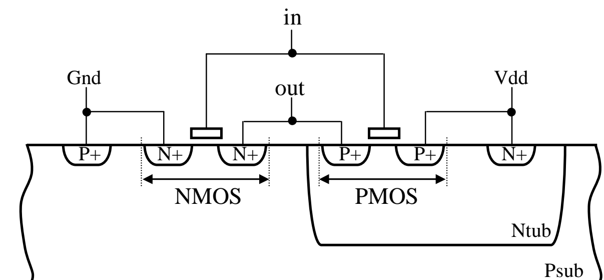


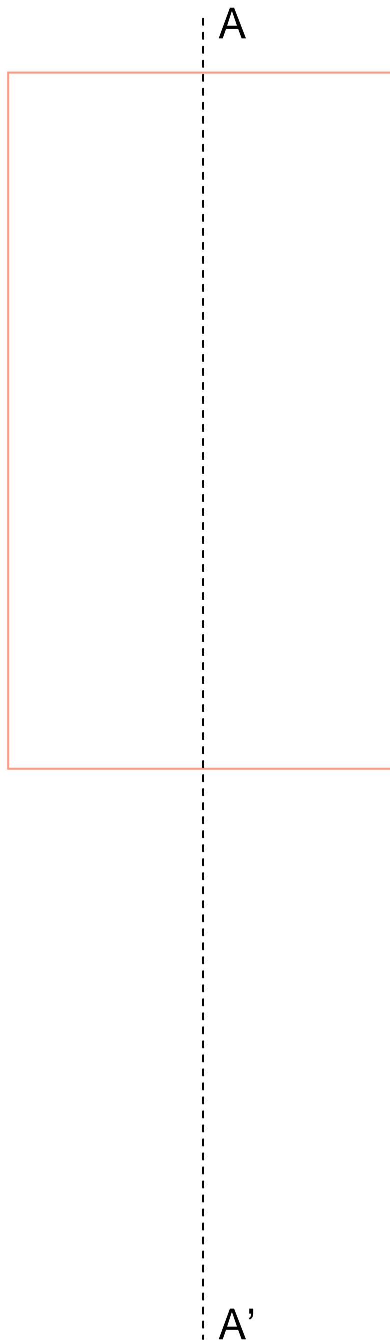


Ouverture du puit N (Ntub)

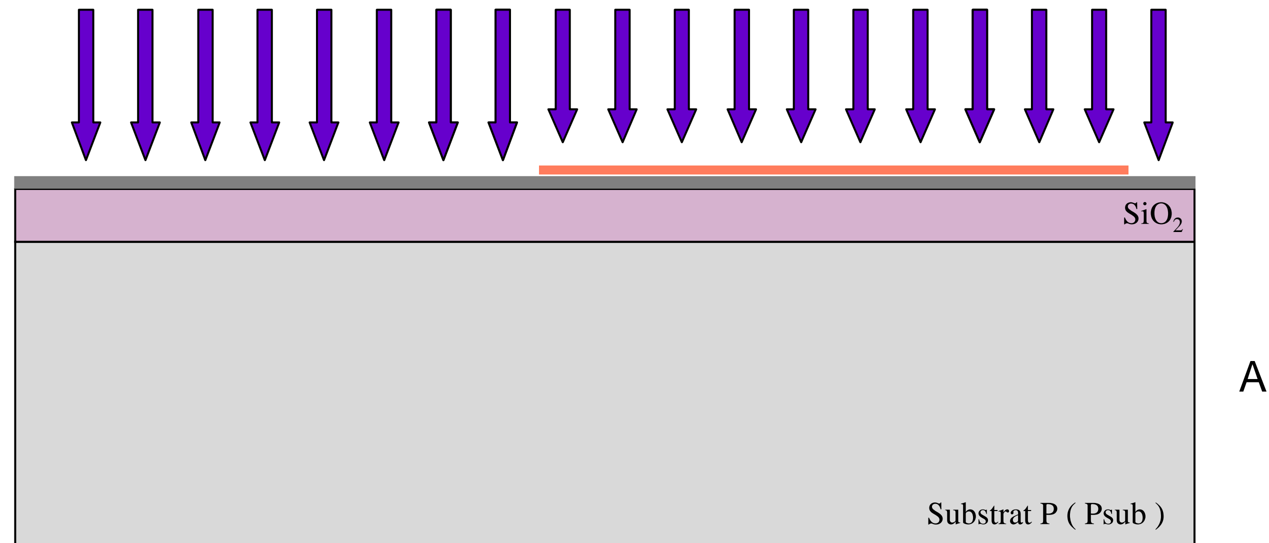


1. Dépôt d'une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
    a. Dépôt de la résine photosensible.

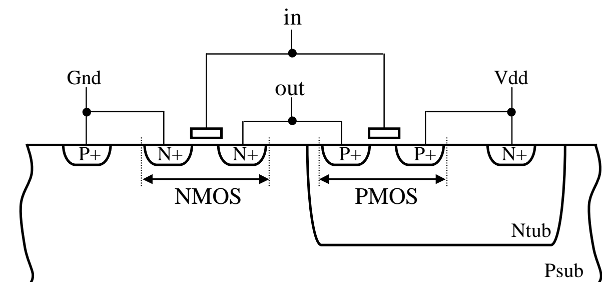


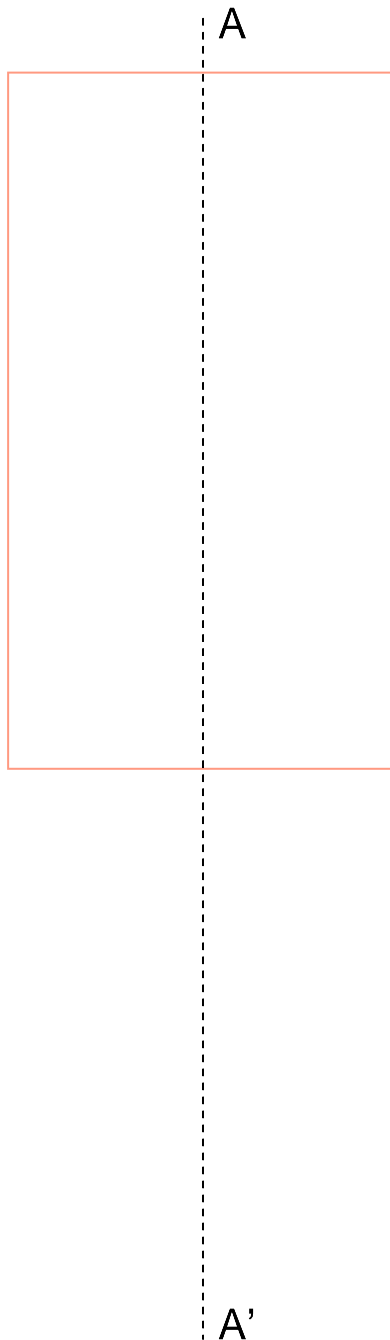


Ouverture du puit N (Ntub)

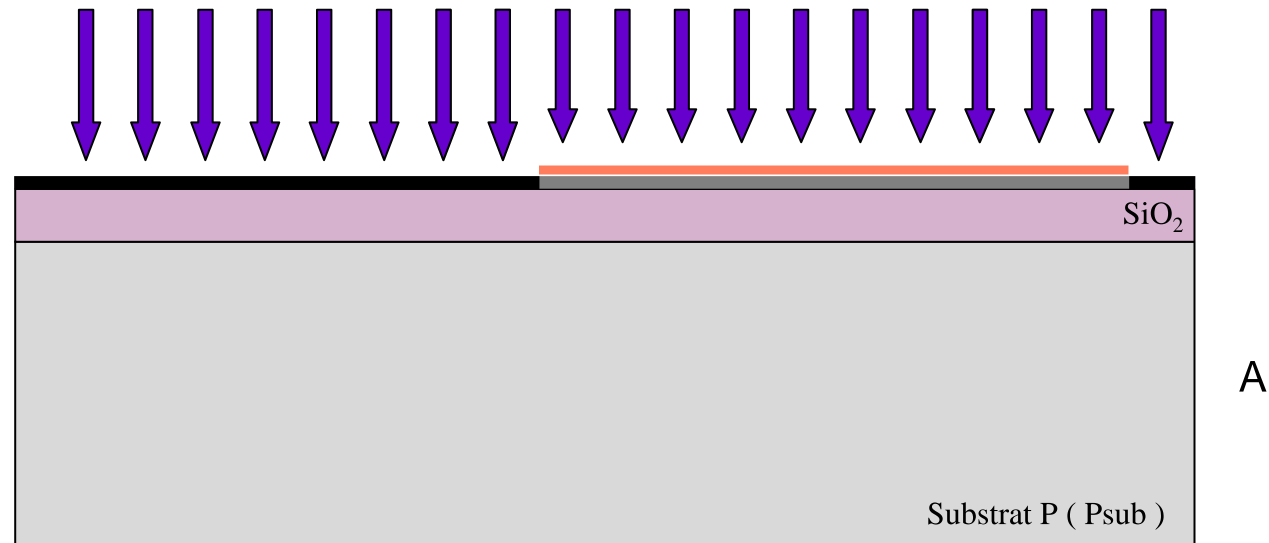


1. Dépôt d’une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
   a. Dépôt de la résine photosensible.
   b. Alignement du masque et exposition aux UV.

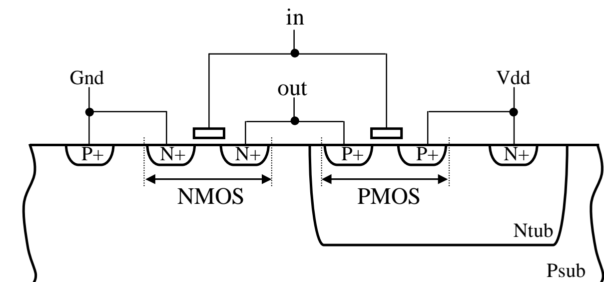


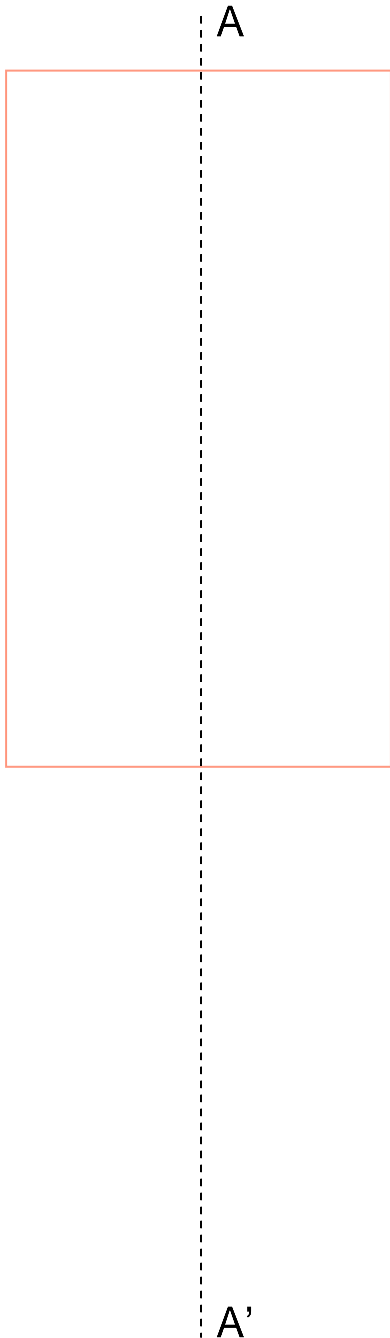


Ouverture du puit N (Ntub)

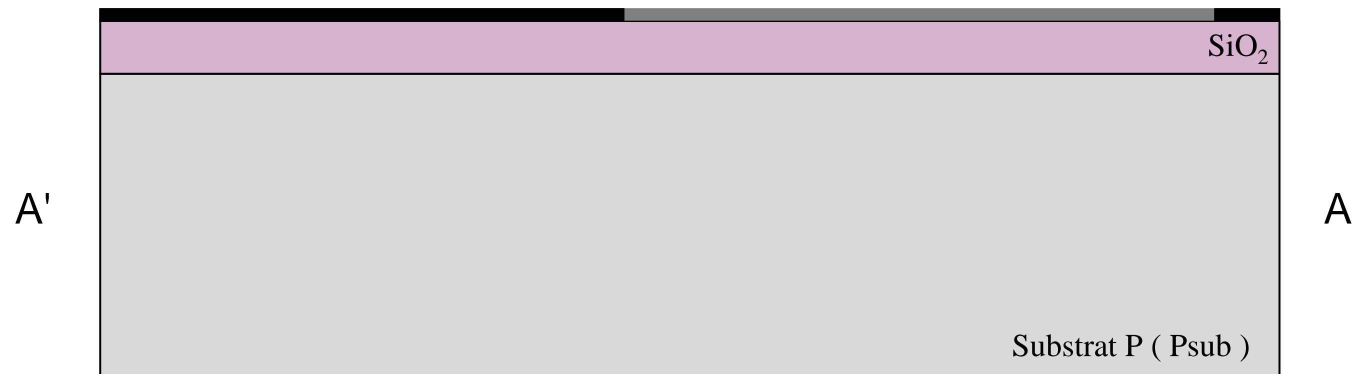


1. Dépôt d’une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
    a. Dépôt de la résine photosensible.
    b. Alignement du masque et exposition aux UV.

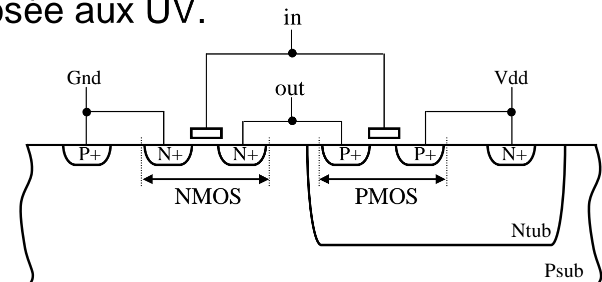


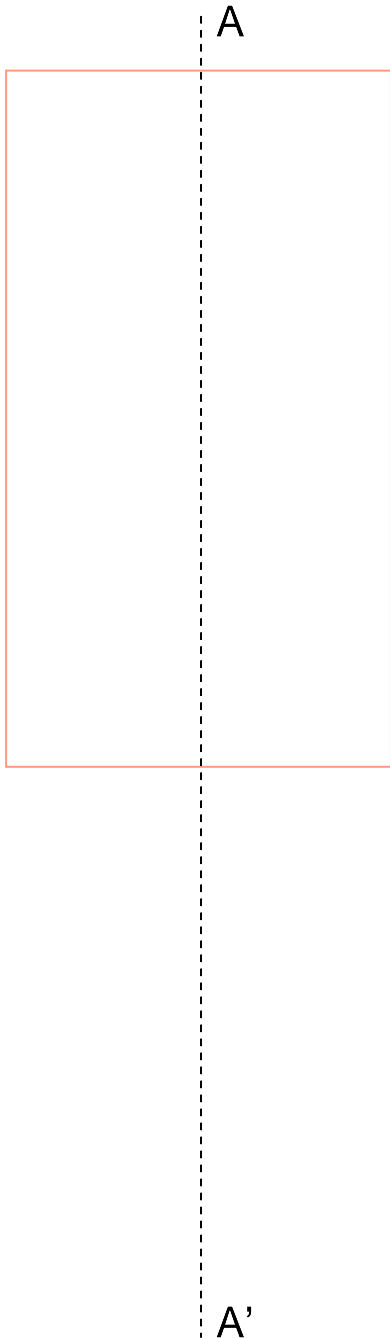


Ouverture du puit N (Ntub)



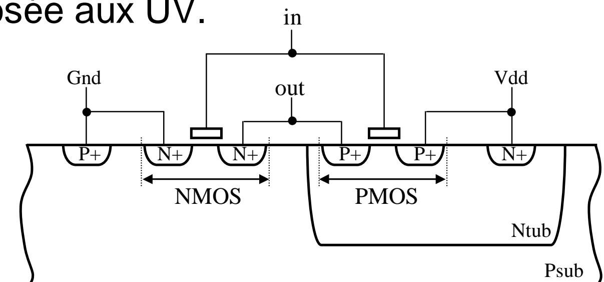
1. Dépôt d’une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
    a. Dépôt de la résine photosensible.
    b. Alignement du masque et exposition aux UV.
    c. Retrait de la résine non exposée aux UV.

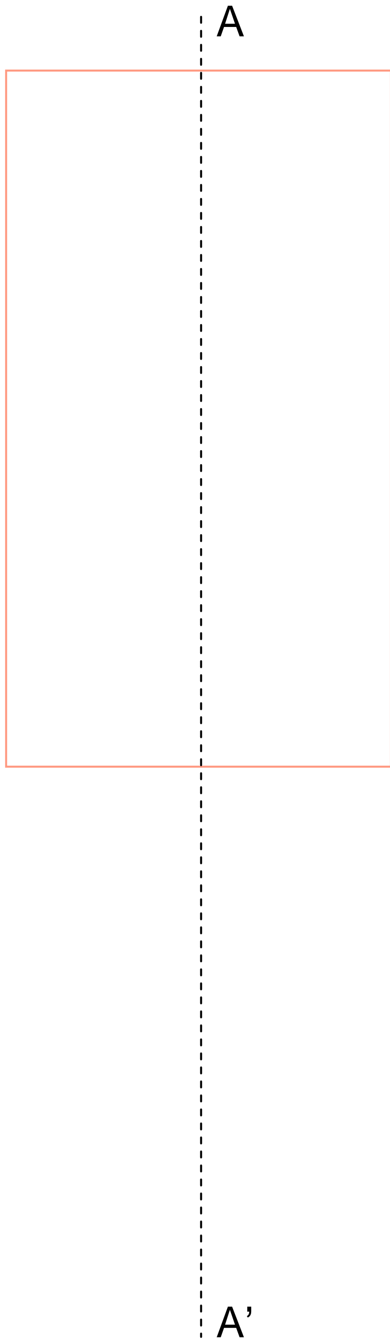




Ouverture du puit N (Ntub)

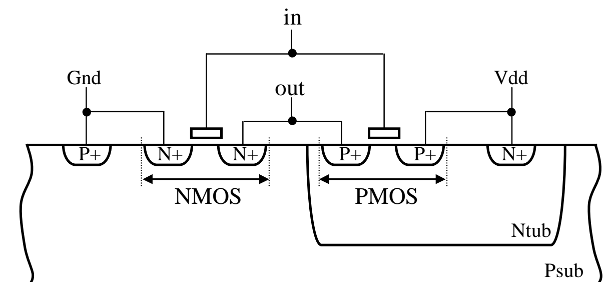
1. Dépôt d’une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
    a. Dépôt de la résine photosensible.
    b. Alignement du masque et exposition aux UV.
    c. Retrait de la résine non exposée aux UV.

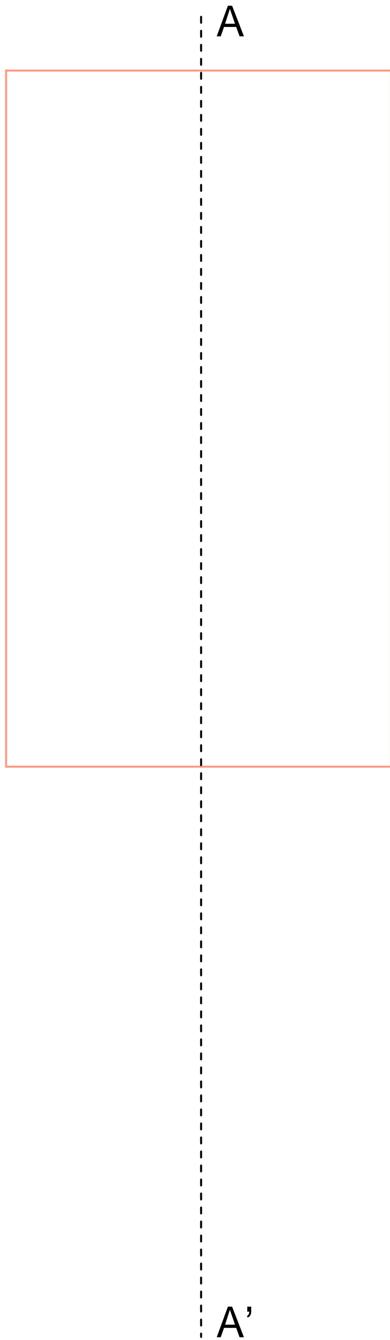




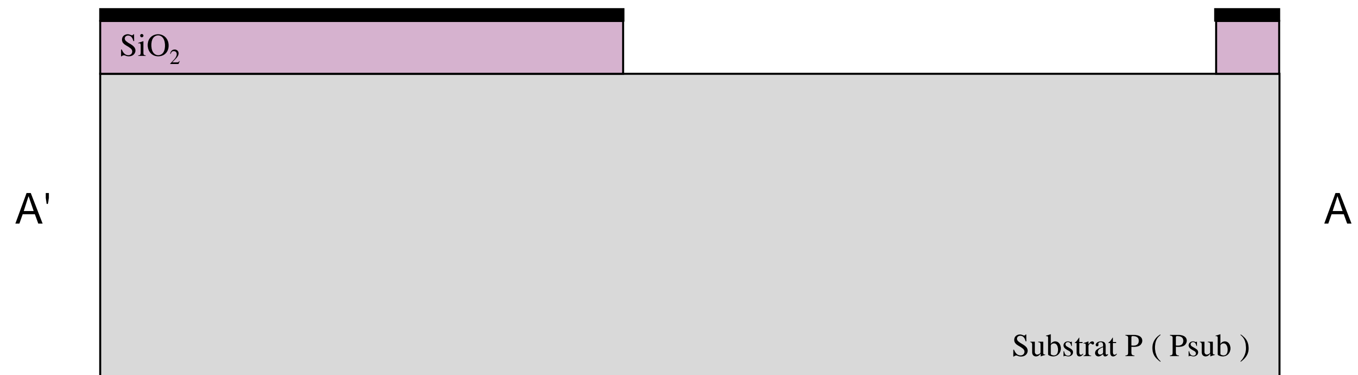
Ouverture du puit N (Ntub)

1. Dépôt d’une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
3. Retrait SiO_2 de la zone découverte.

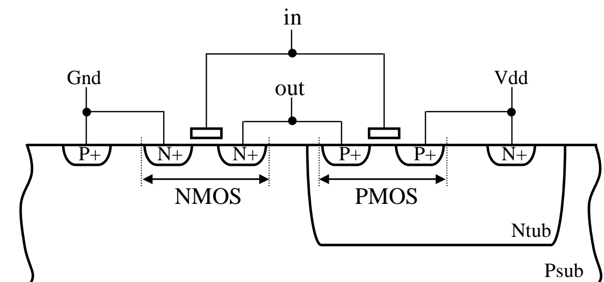


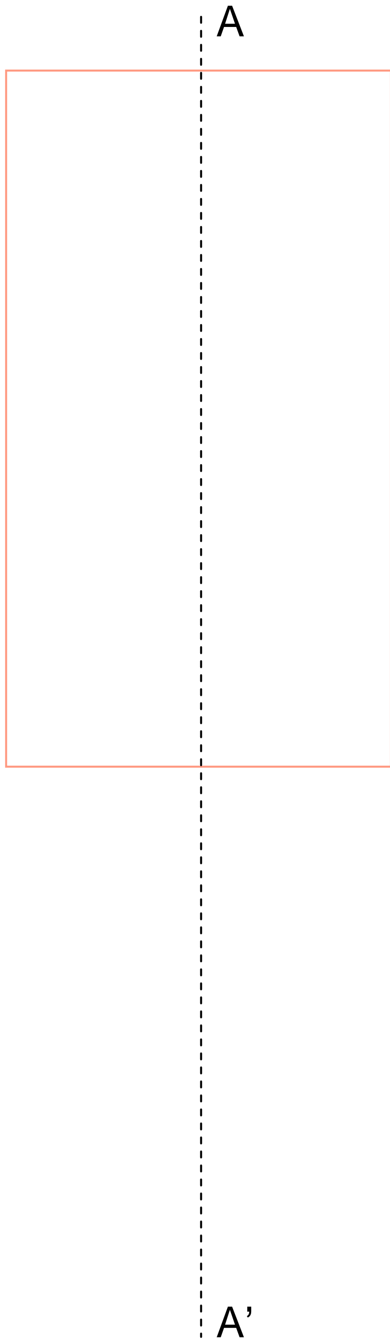


Ouverture du puit N (Ntub)

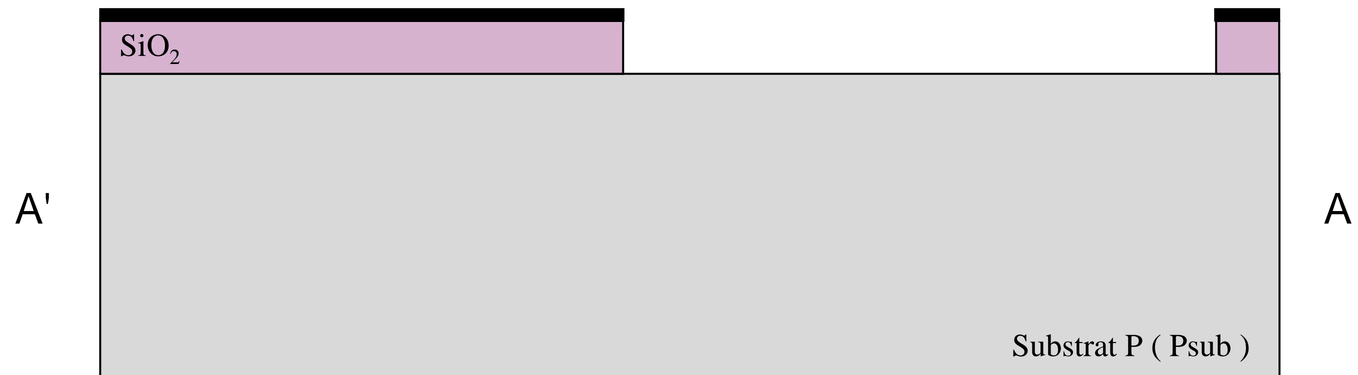


1. Dépôt d’une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
3. Retrait SiO_2 de la zone découverte.

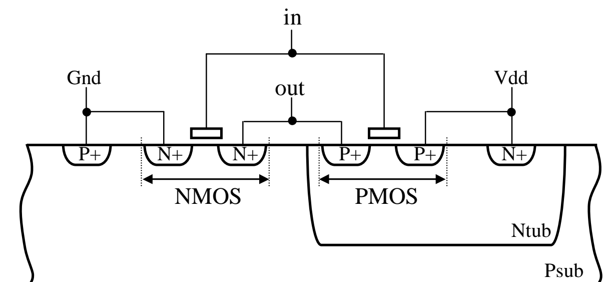


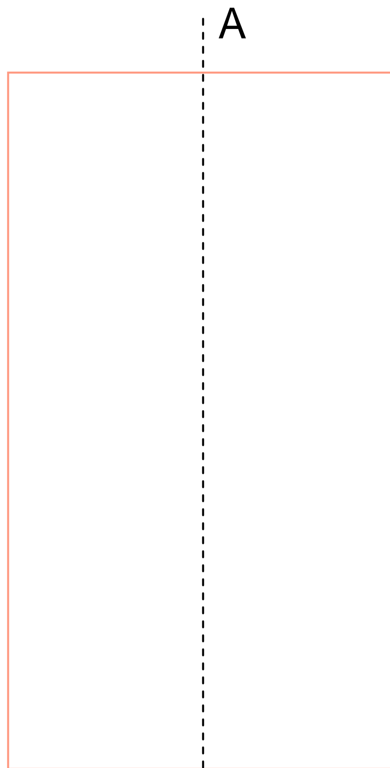


Ouverture du puit N (Ntub)

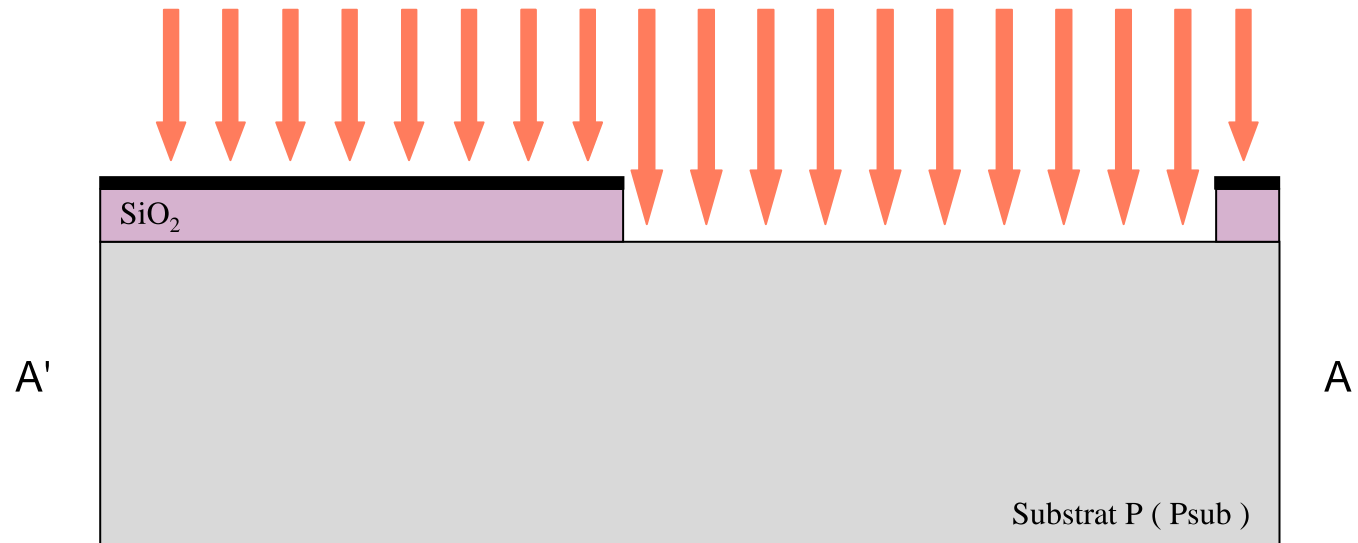


1. Dépôt d’une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
3. Retrait SiO_2 de la zone découverte.
4. Implantation dopant N.

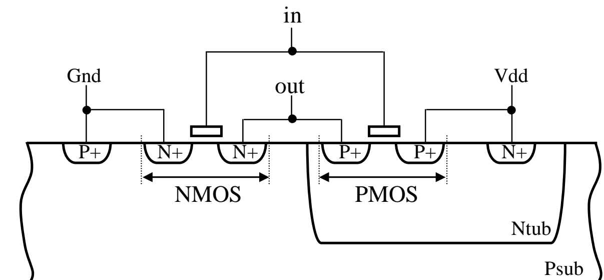


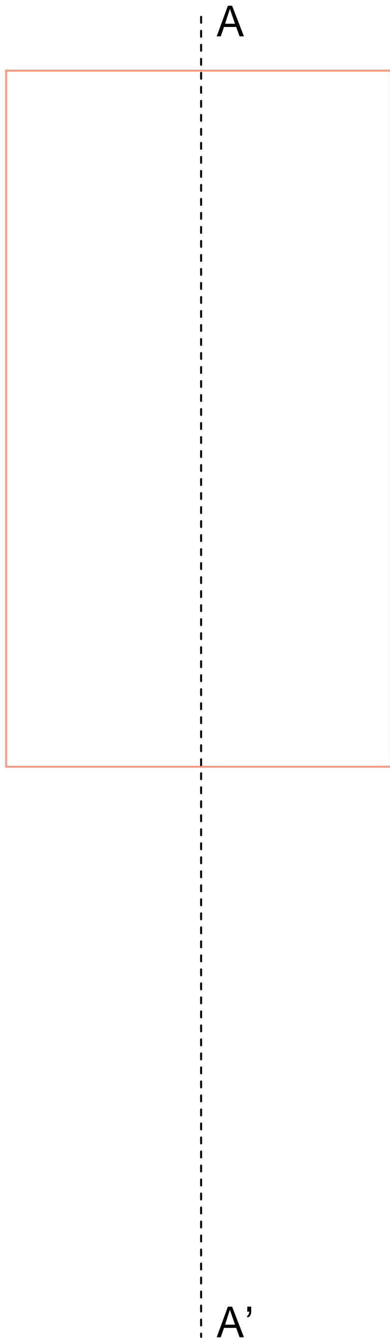


Ouverture du puit N (Ntub)

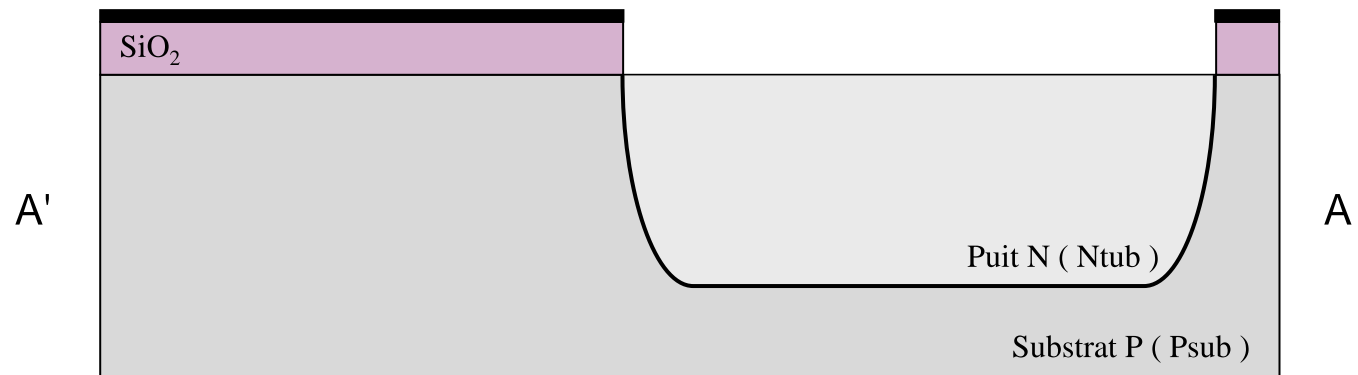


1. Dépôt d’une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
3. Retrait SiO_2 de la zone découverte.
4. Implantation dopant N.

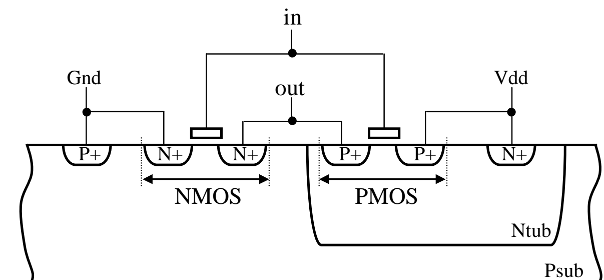




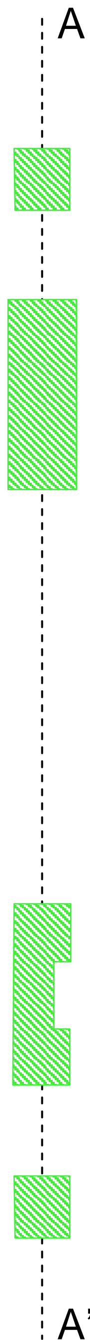
Ouverture du puit N (Ntub)

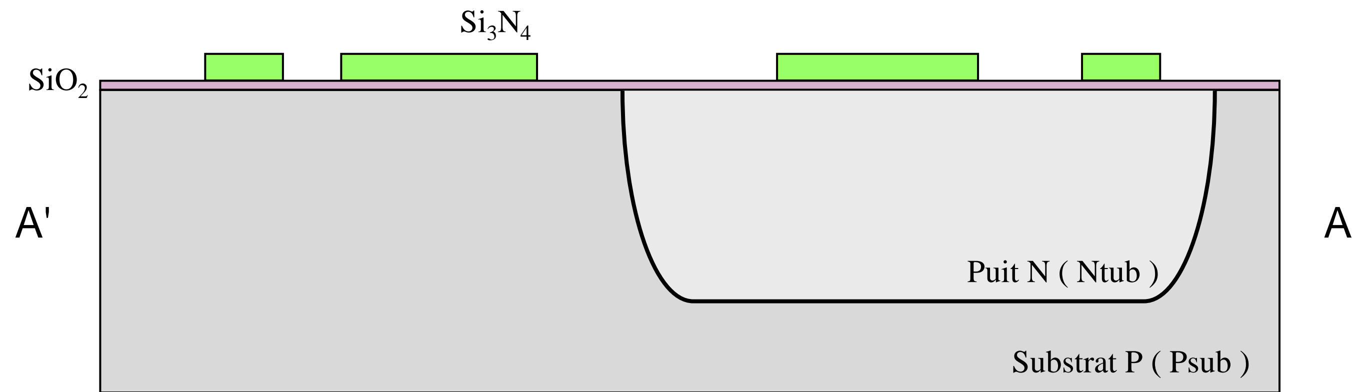


1. Dépôt d’une couche de SiO_2 protectrice.
2. Séquence de photolithographie.
3. Retrait SiO_2 de la zone découverte.
4. Implantation dopant N.

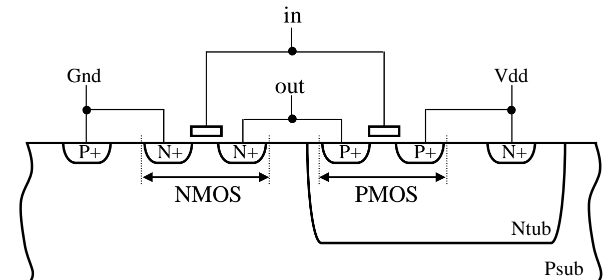


Délimitation des diffusions (zones actives)





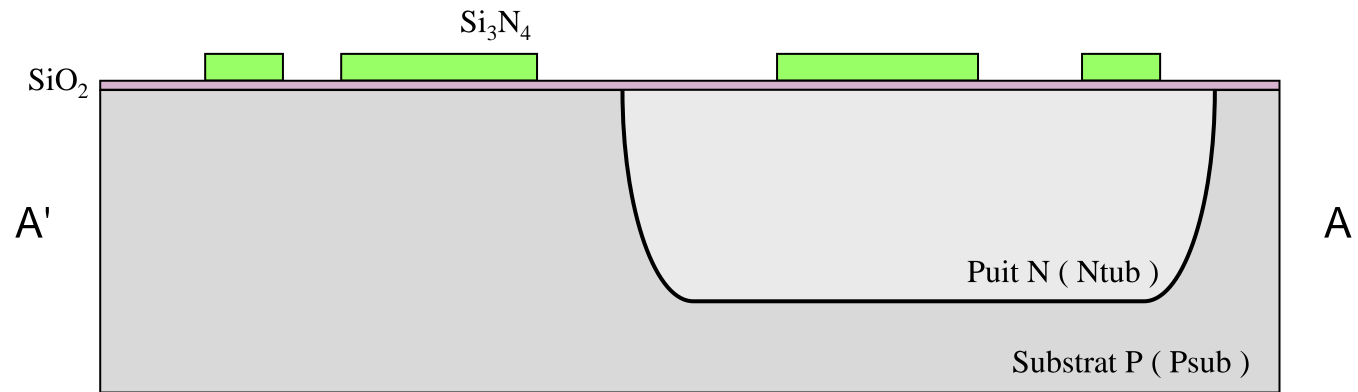
1. Dépôt d'une couche de Si_3N_4 protectrice (masque DIFF).



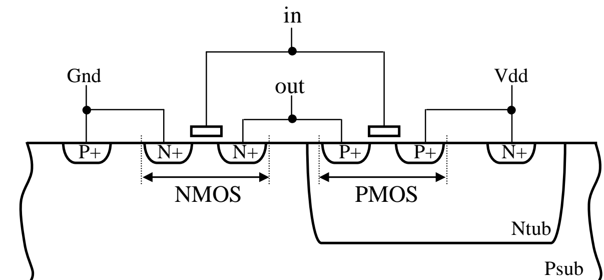
A

A'

Délimitation des diffusions (zones actives)



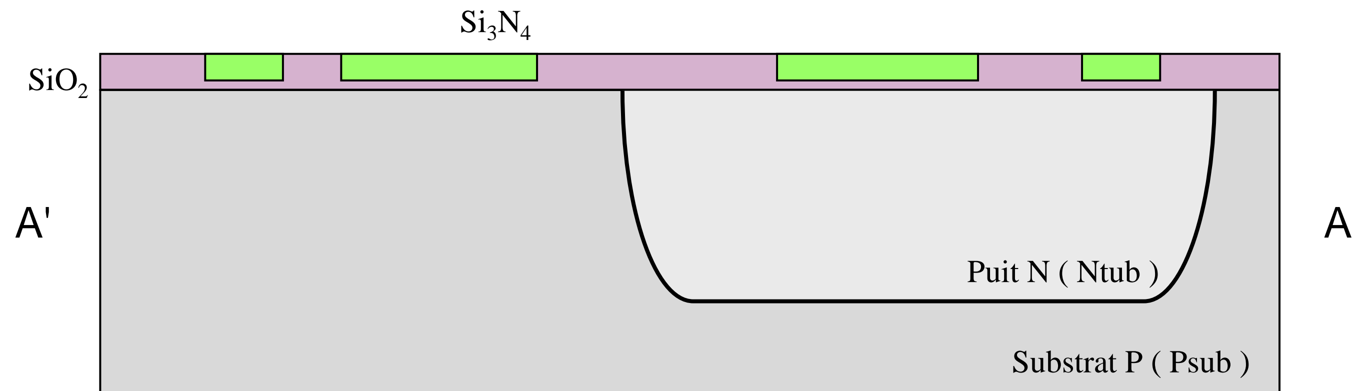
1. Dépôt d'une couche de Si_3N_4 protectrice (masque DIFF).
2. Croissance de l'oxyde local (LOCOS) hors DIFF.



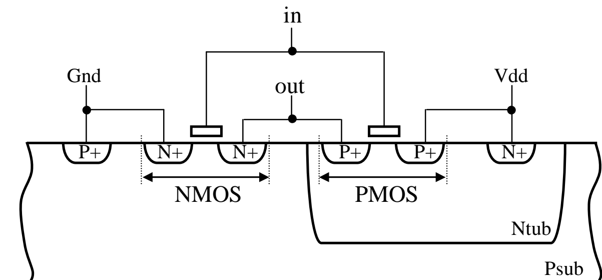
Délimitation des diffusions (zones actives)

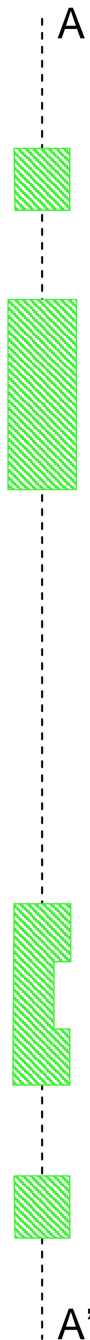
A

A'

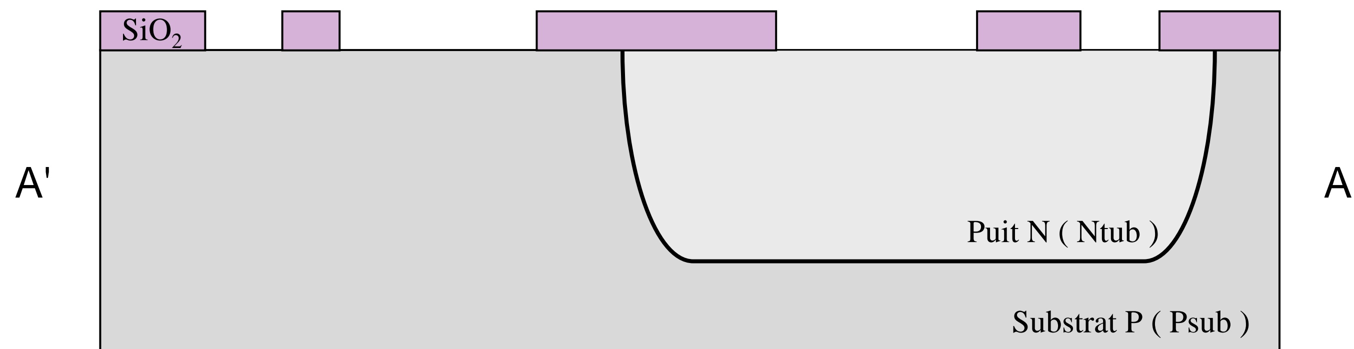


1. Dépôt d'une couche de Si_3N_4 protectrice (masque DIFF).
2. Croissance de l'oxyde local (LOCOS) hors DIFF.
3. Retrait Si_3N_4 et retrait des traces d'oxyde dans les diffusions.

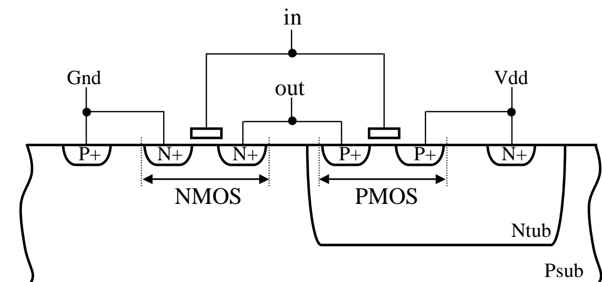




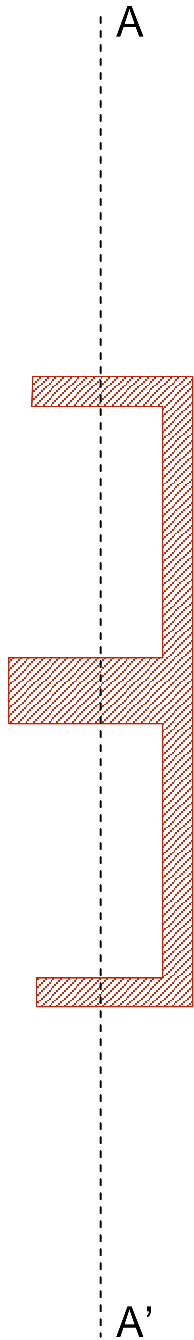
Délimitation des diffusions (zones actives)

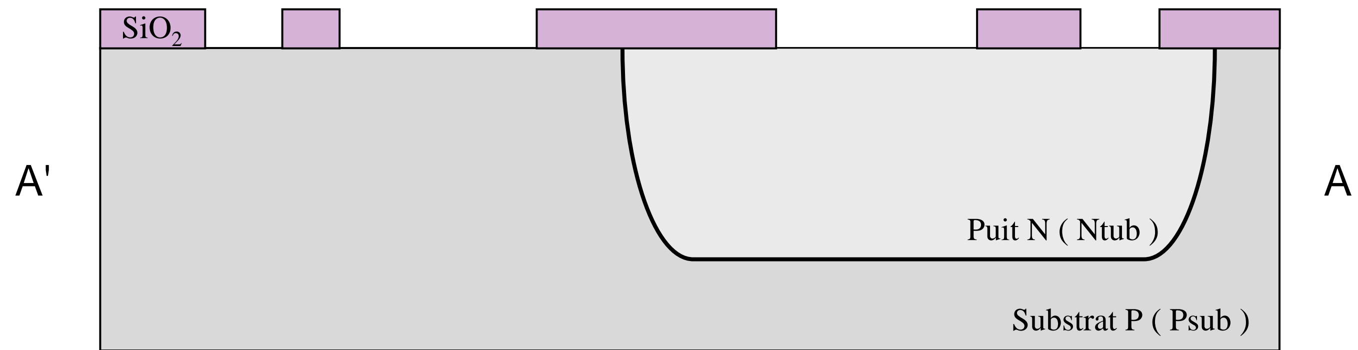


1. Dépôt d'une couche de Si_3N_4 protectrice (masque DIFF).
2. Croissance de l'oxyde local (LOCOS) hors DIFF.
3. Retrait Si_3N_4 et retrait des traces d'oxyde dans les diffusions.

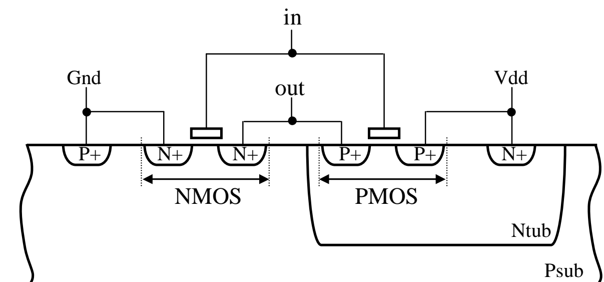


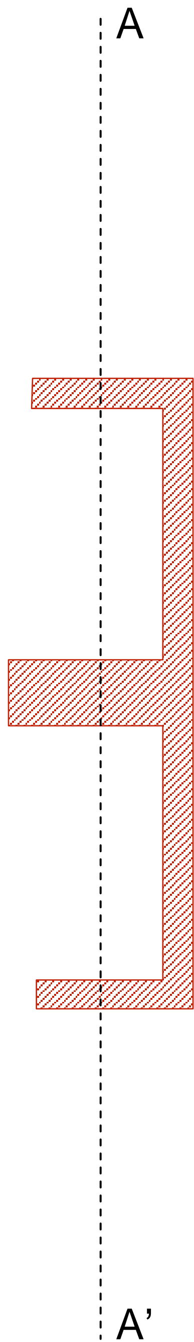
Réalisation des grilles en polysilicium



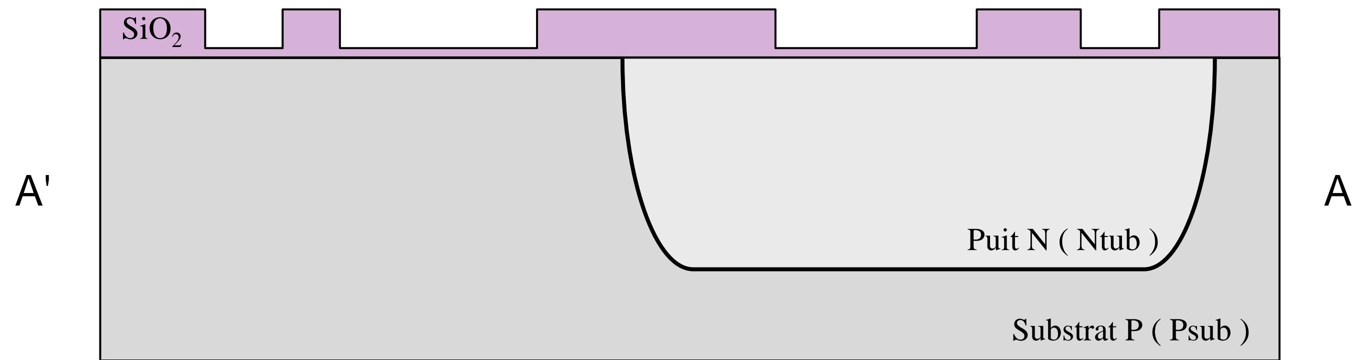


1. Croissance d’une couche d’oxyde de grille fin (SiO_2 : 7-8 nm).

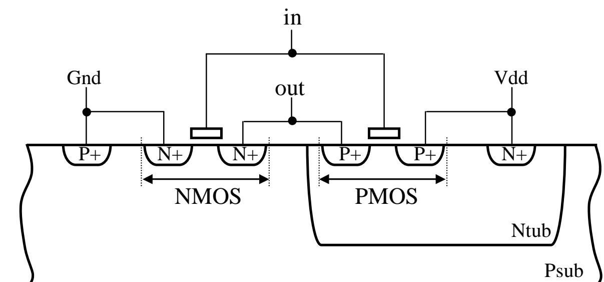


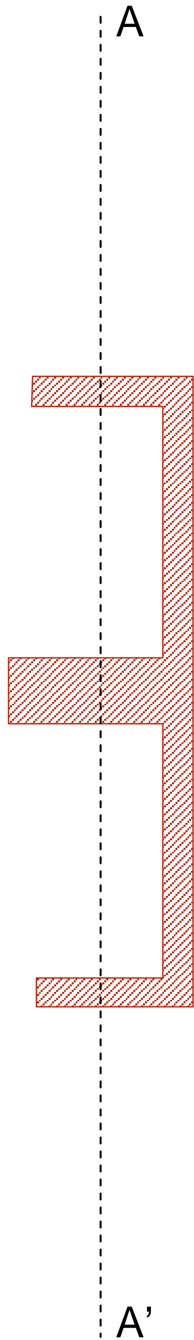


Réalisation des grilles en polysilicium

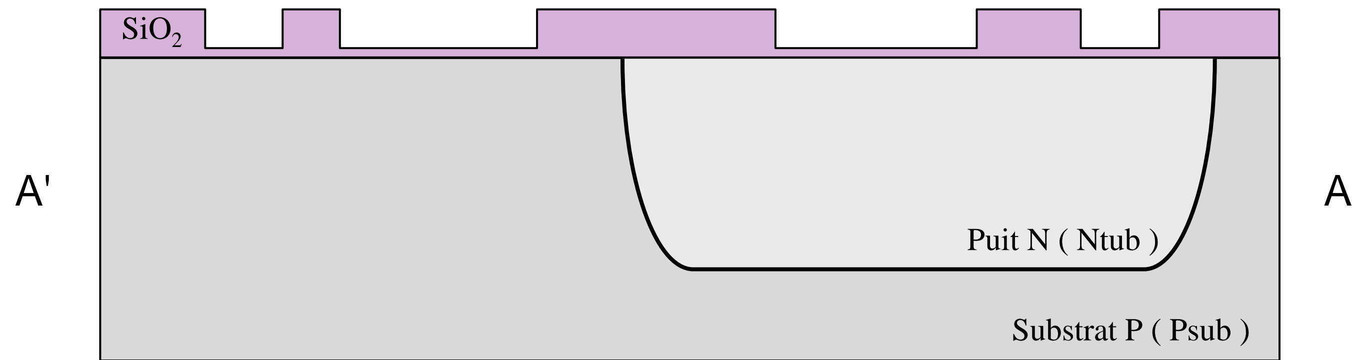


1. Croissance d'une couche d'oxyde de grille fin (SiO_2 : 7-8 nm).

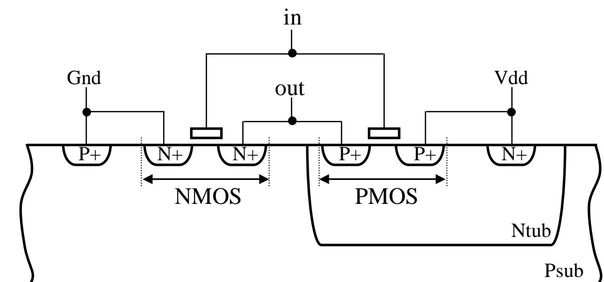


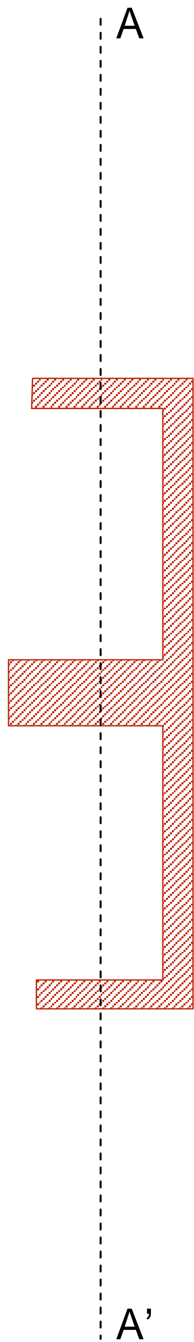


Réalisation des grilles en polysilicium

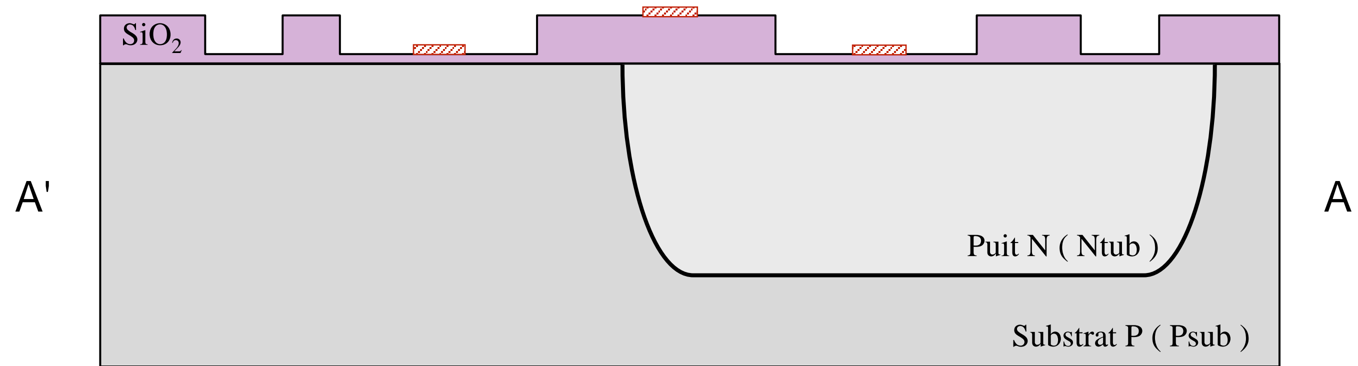


1. Croissance d'une couche d'oxyde de grille fin (SiO_2 : 7-8 nm).
2. Dépôt et gravure du polysilicium de grille.

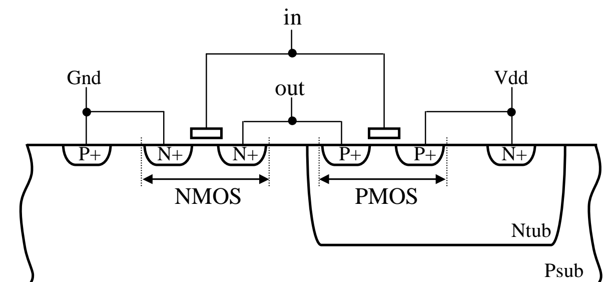


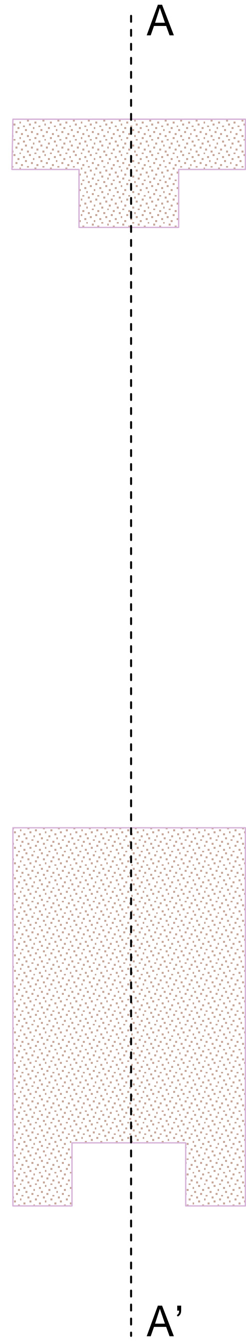


Réalisation des grilles en polysilicium



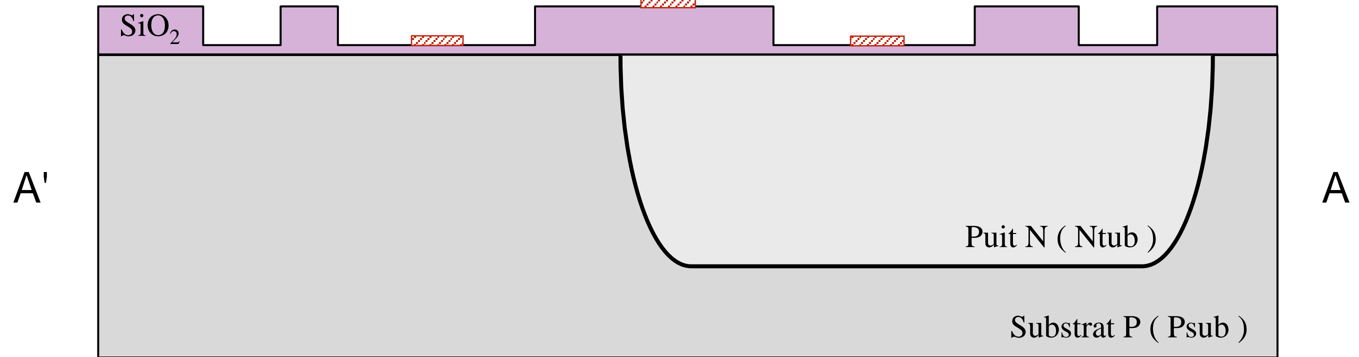
1. Croissance d'une couche d'oxyde de grille fin (SiO_2 : 7-8 nm).
2. Dépôt et gravure du polysilicium de grille.



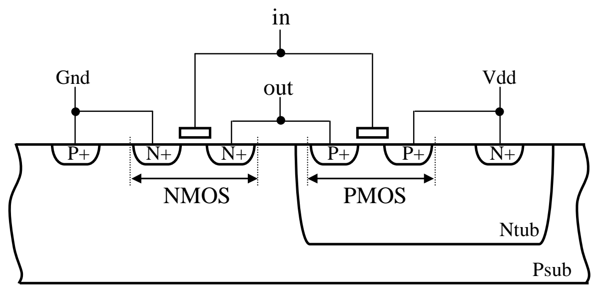


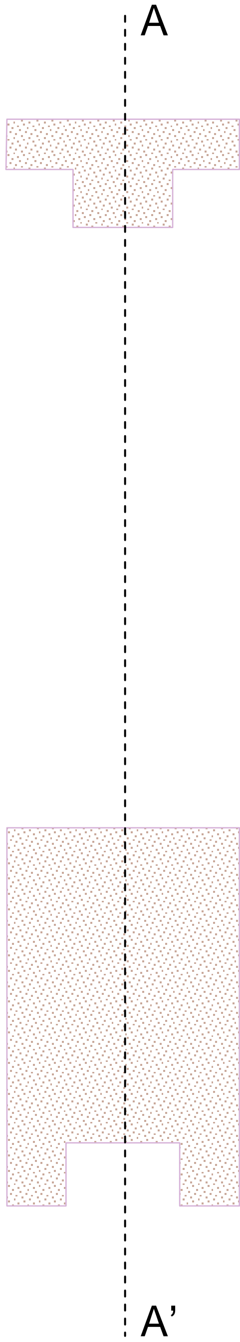
Réalisation des diffusions N+

(NMOS et NTAP)



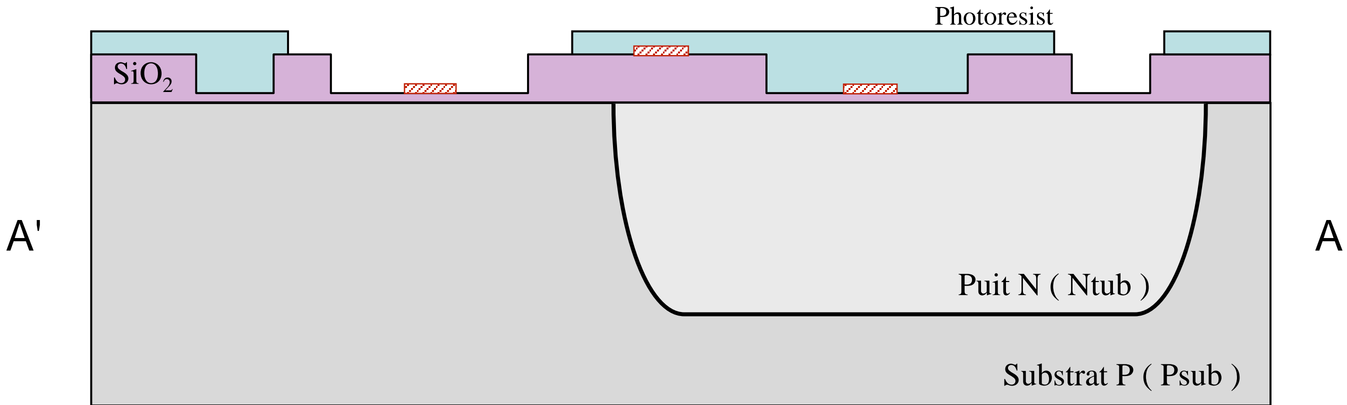
1. Dépôt et gravure (masque NPLUS) d'un photoresist protecteur.



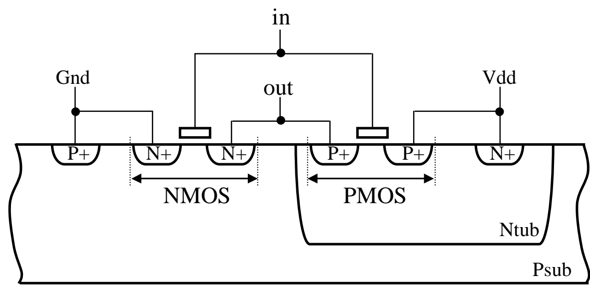


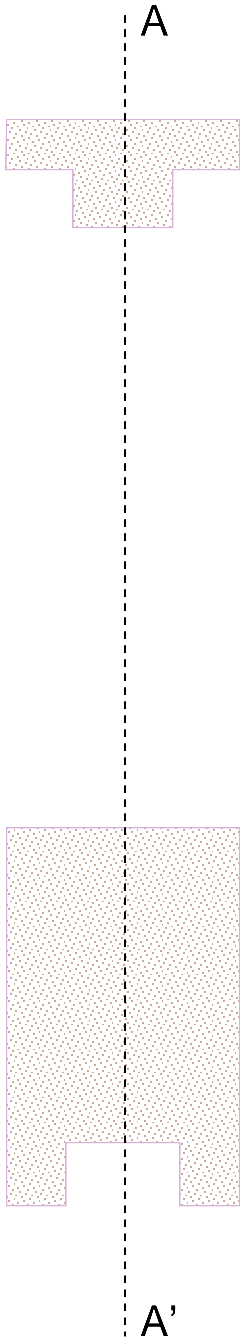
Réalisation des diffusions N+

(NMOS et NTAP)



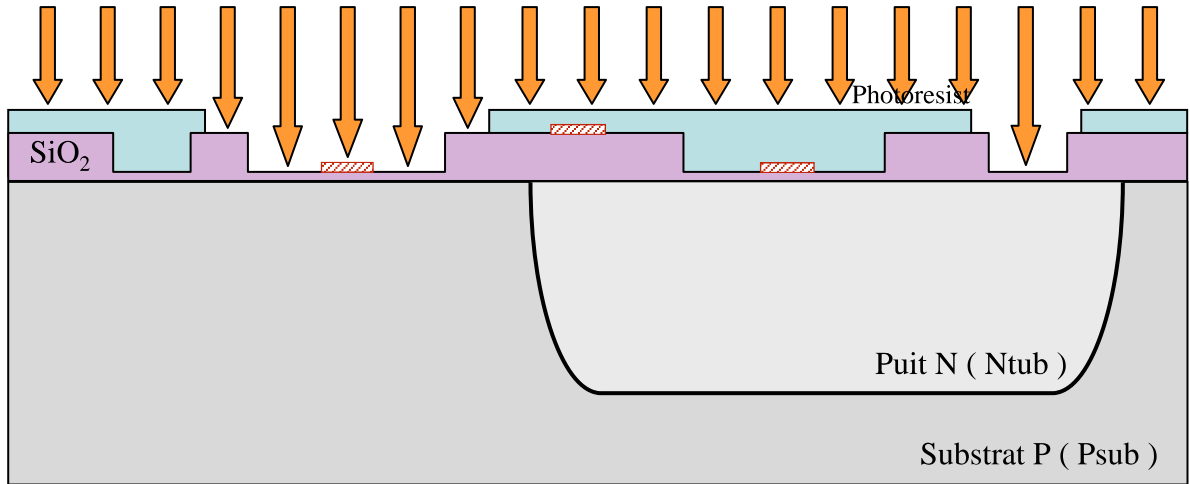
1. Dépôt et gravure (masque NPLUS) d'un photoresist protecteur.
2. Implantation ionique N+.



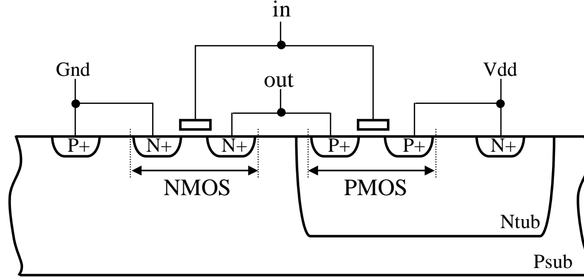


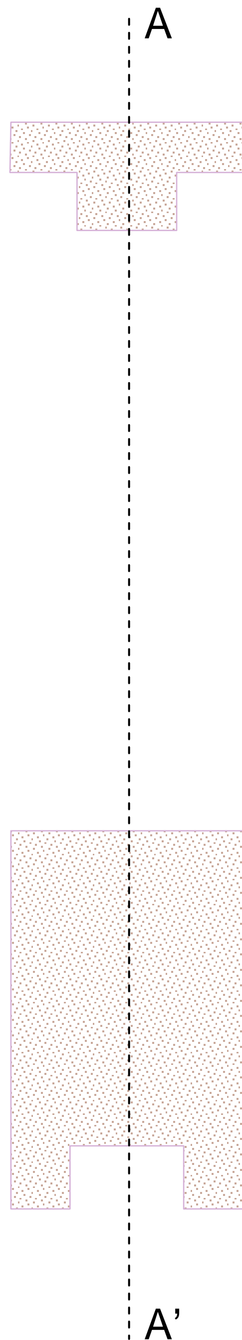
Réalisation des diffusions N+

(NMOS et NTAP)



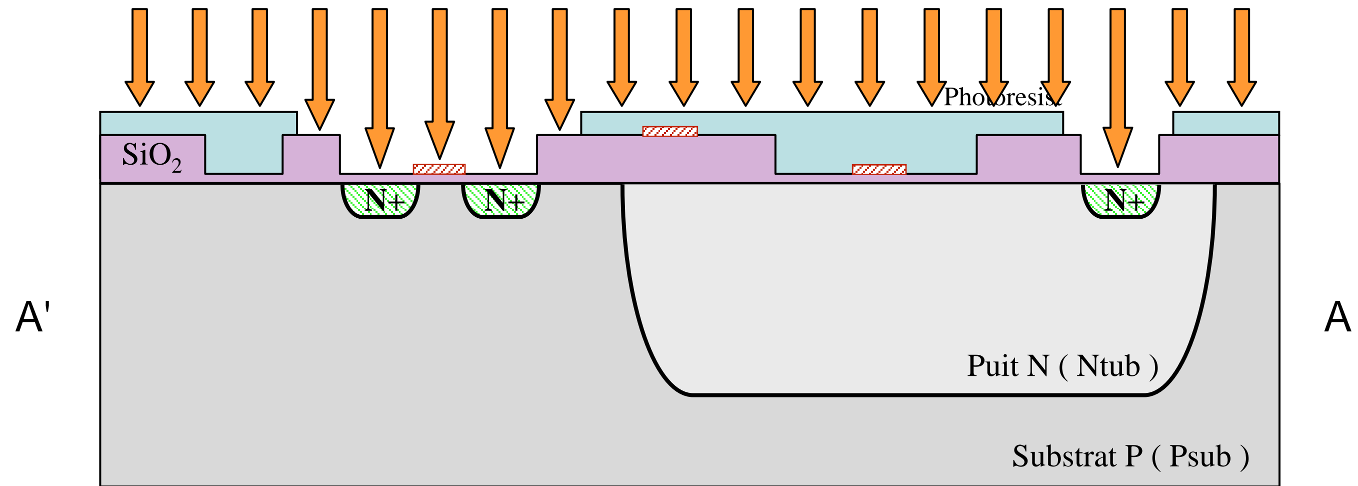
1. Dépôt et gravure (masque NPLUS) d'un photoresist protecteur.
2. Implantation ionique N+.





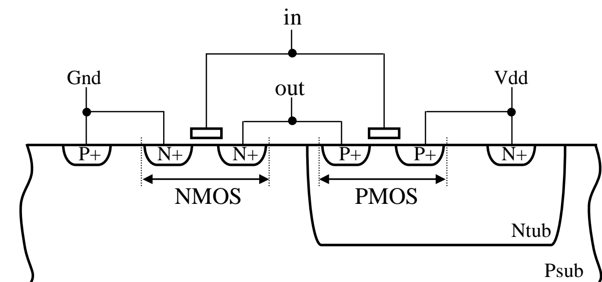
Réalisation des diffusions N+

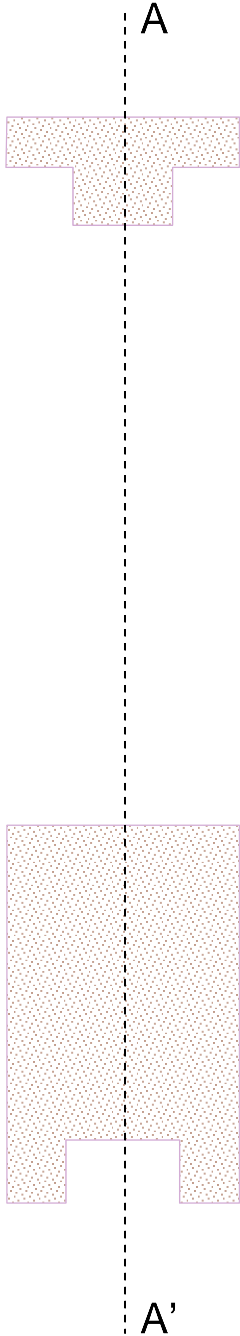
(NMOS et NTAP)



1. Dépôt et gravure (masque NPLUS) d'un photoresist protecteur.
2. Implantation ionique N+.

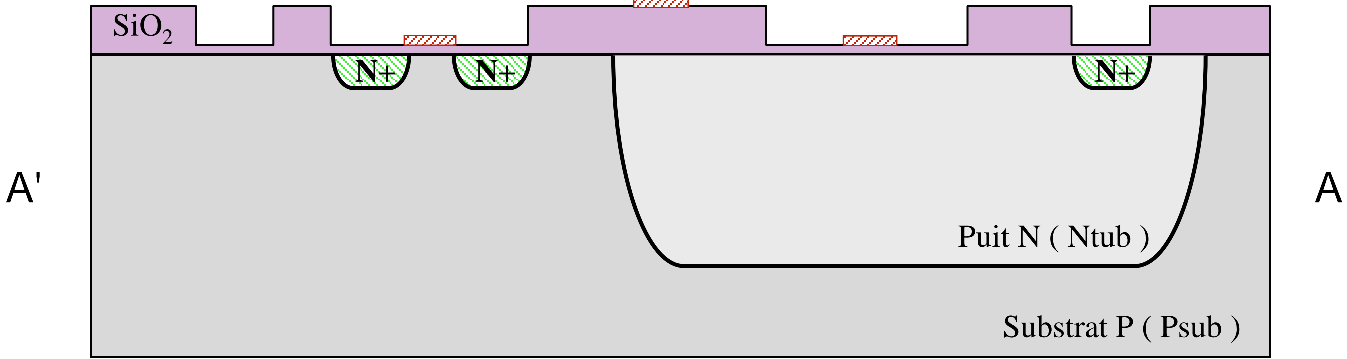
A noter le principe d'auto alignement de la grille.





Réalisation des diffusions N+

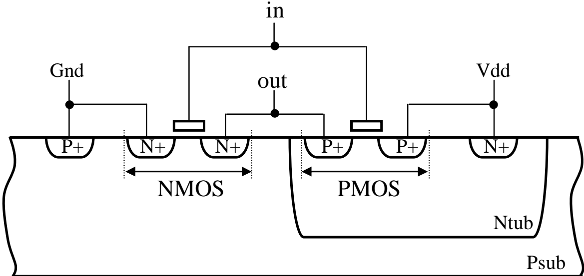
(NMOS et NTAP)

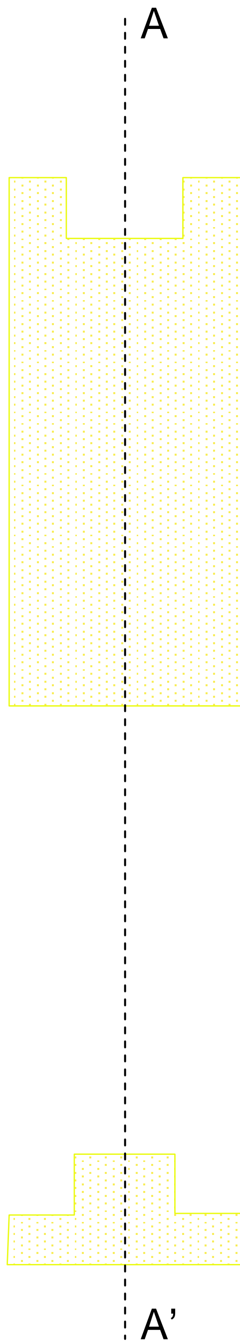


1. Dépôt et gravure (masque NPLUS) d'un photoresist protecteur.
2. Implantation ionique N+.

   A noter le principe d'auto alignement de la grille.

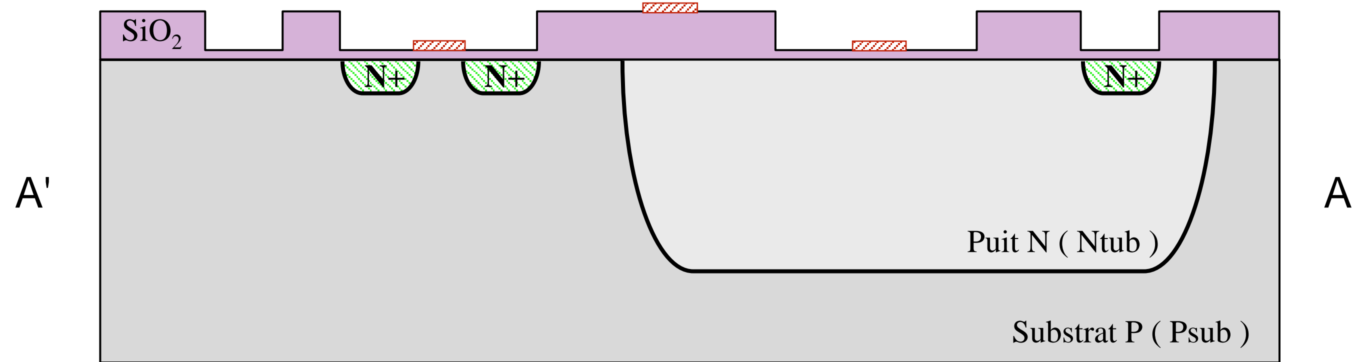
   Retrait du photoresist.



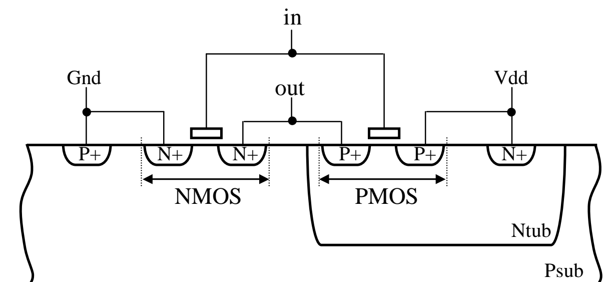


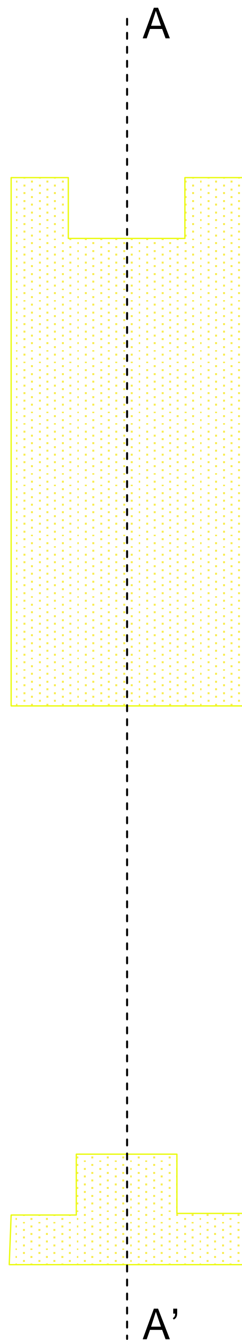
Réalisation des diffusions P+

(PMOS et PTAP)



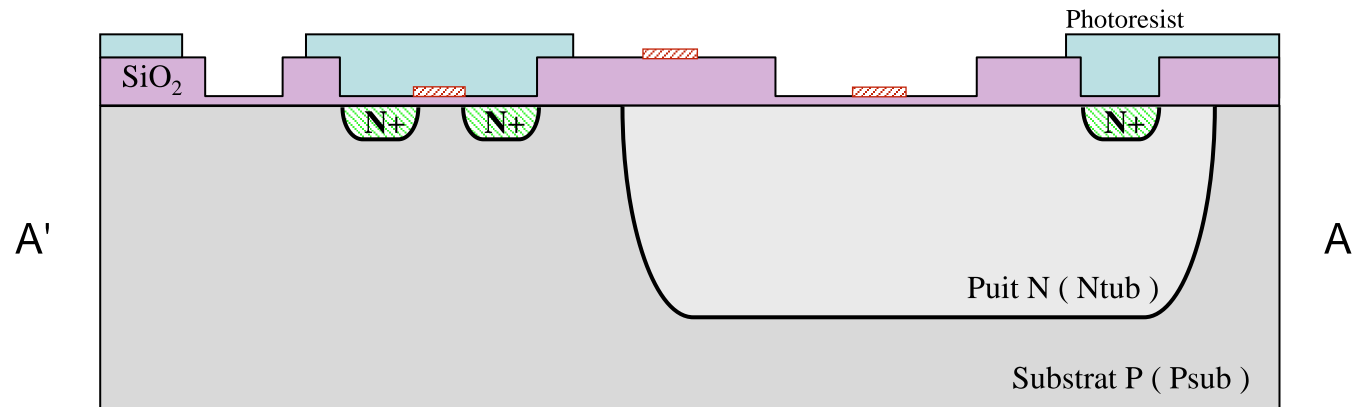
1. Dépôt et gravure (masque PPLUS) d’un photoresist protecteur.



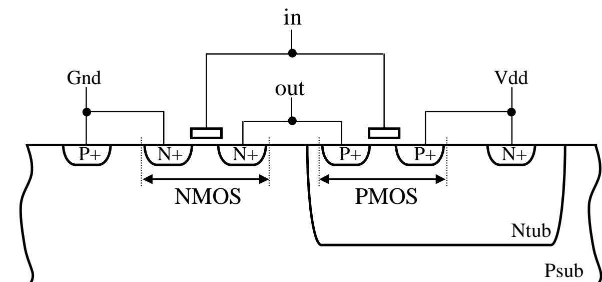


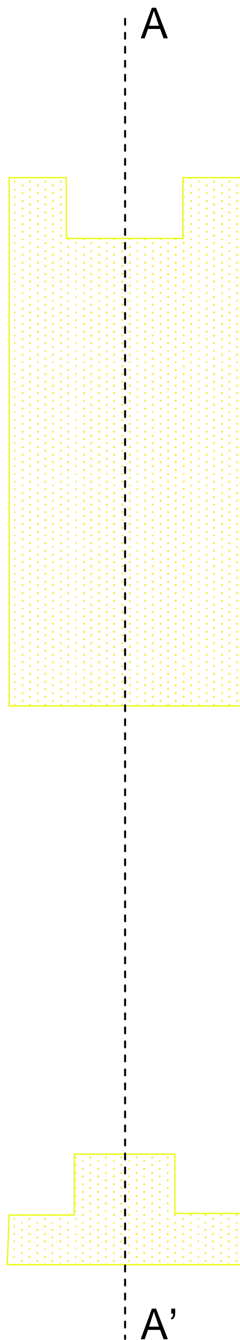
Réalisation des diffusions P+

(PMOS et PTAP)



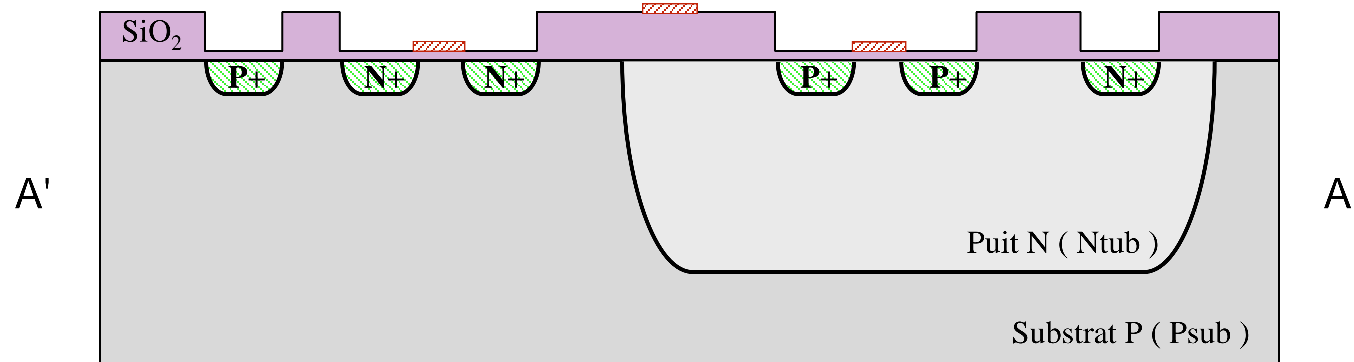
1. Dépôt et gravure (masque PPLUS) d'un photoresist protecteur.
2. Implantation ionique P+.





Réalisation des diffusions P+

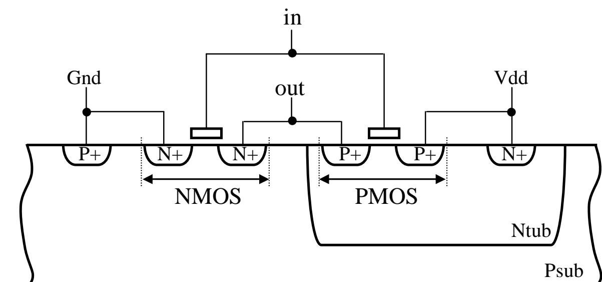
(PMOS et PTAP)



1. Dépôt et gravure (masque PPLUS) d'un photoresist protecteur.
2. Implantation ionique P+.

A noter le principe d'auto alignement de la grille.

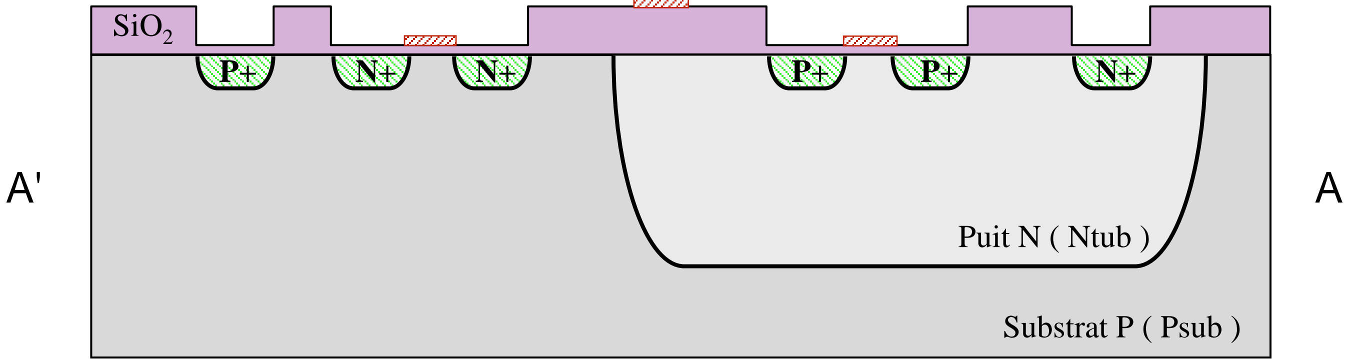
Retrait du photoresist.



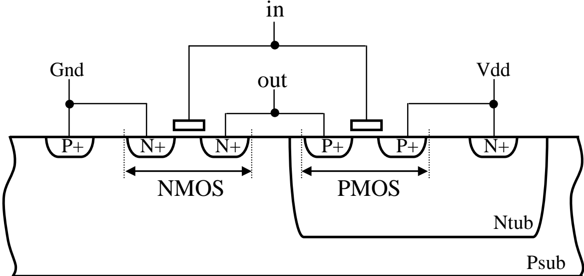
A

A'

Croissance oxyde

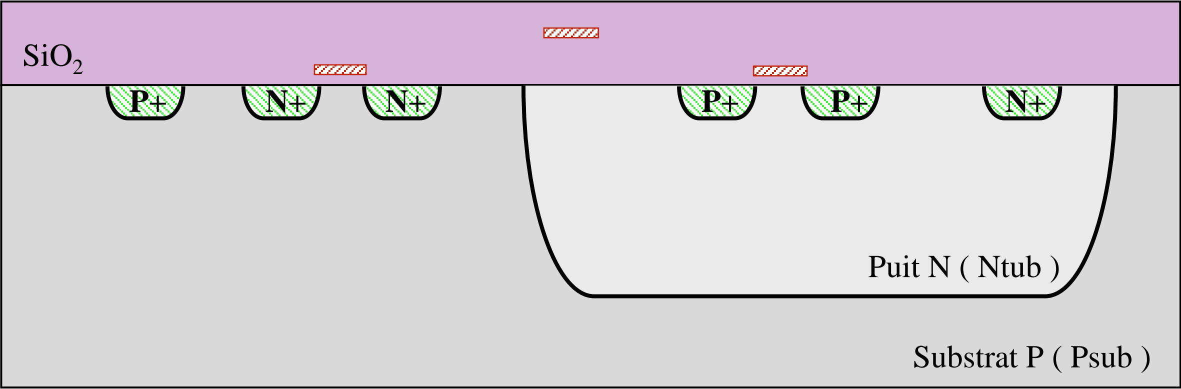


Croissance d’oxyde par Chemical Vapor Deposition (CVD).

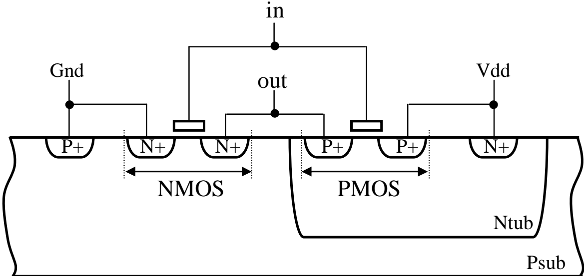


A

Croissance oxyde



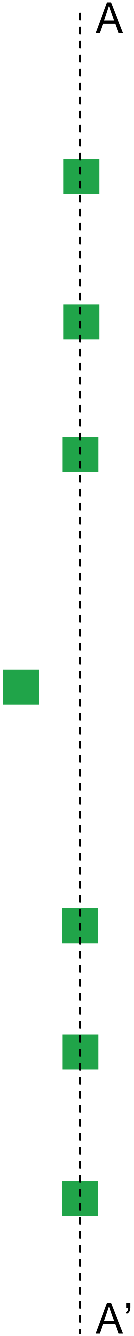
Croissance d'oxyde par Chemical Vapor Deposition (CVD).

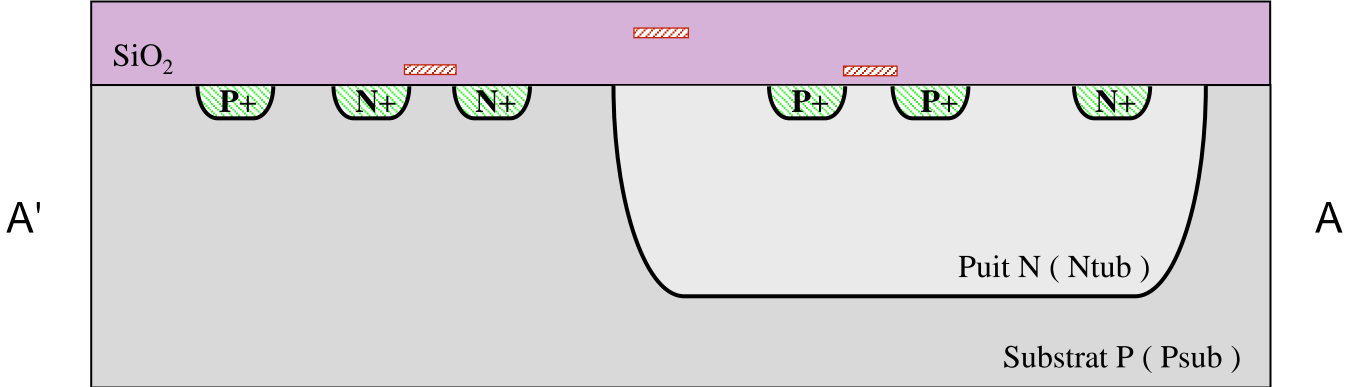


A'

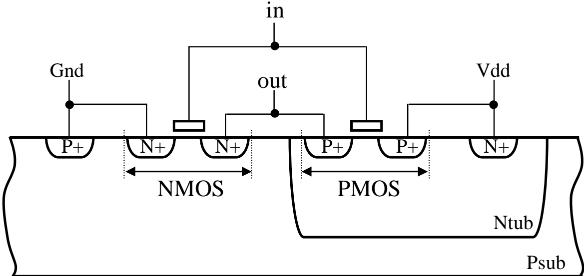
Réalisation des contacts

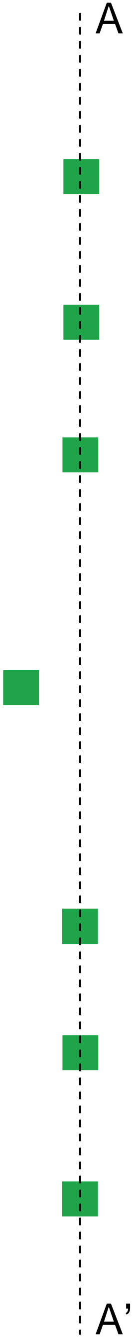
(connexion DIFF/POLY – MET1)





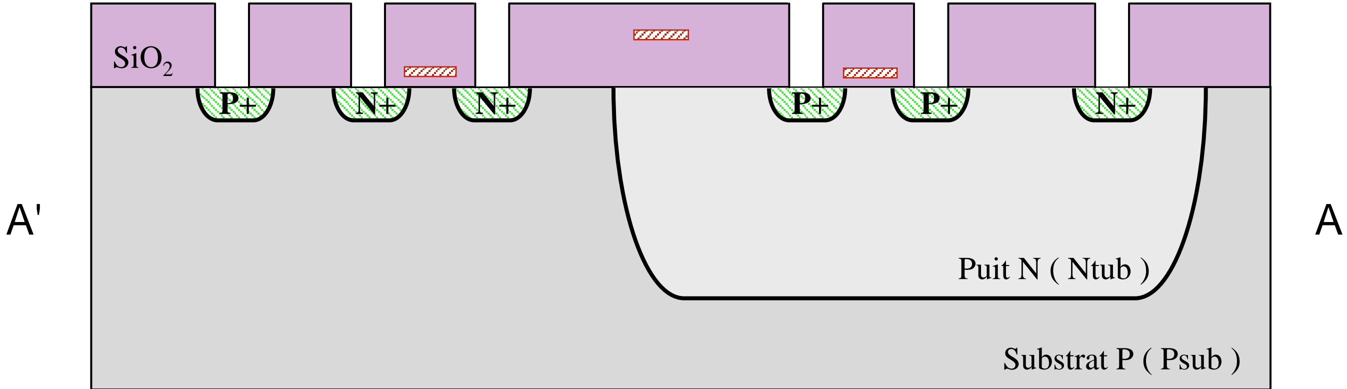
1. Ouverture des contacts (masque CONT).



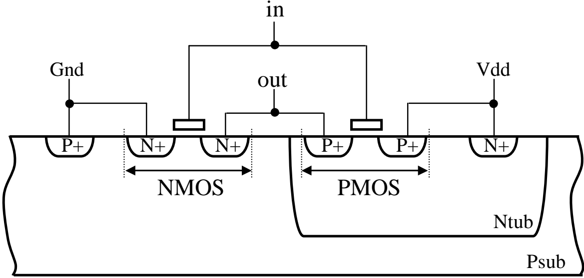


Réalisation des contacts

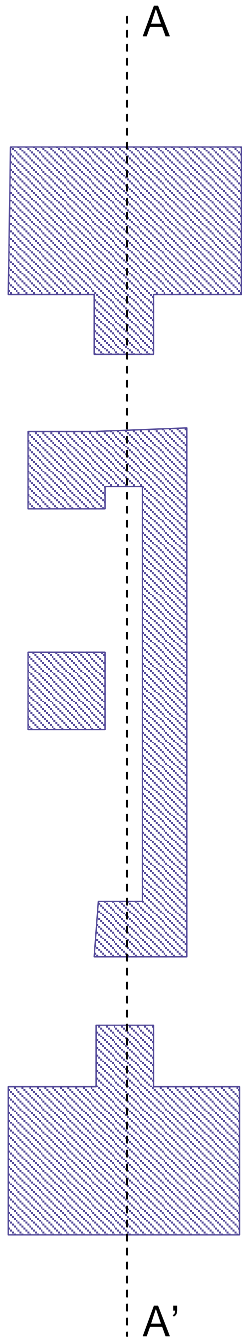
(connexion DIFF/POLY – MET1)

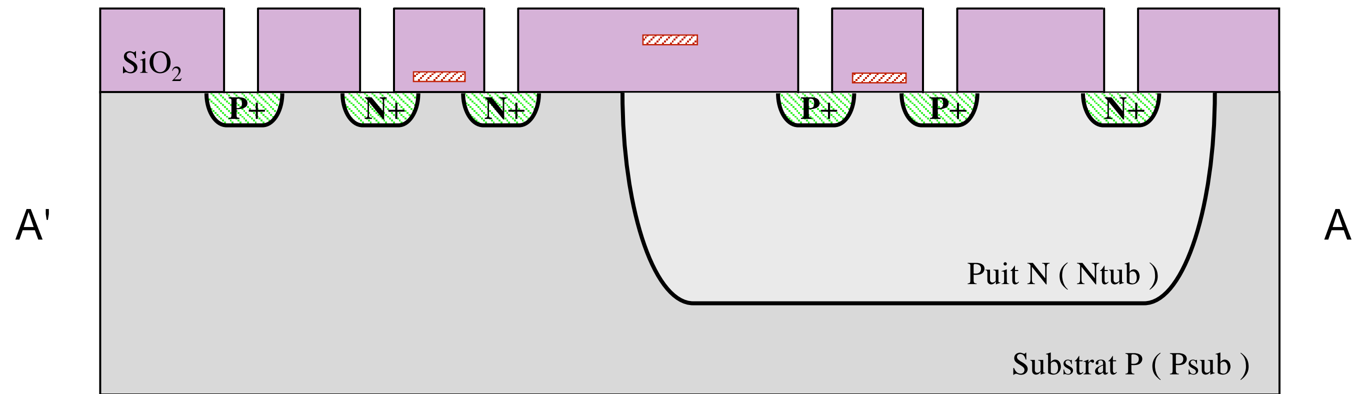


1. Ouverture des contacts (masque CONT).

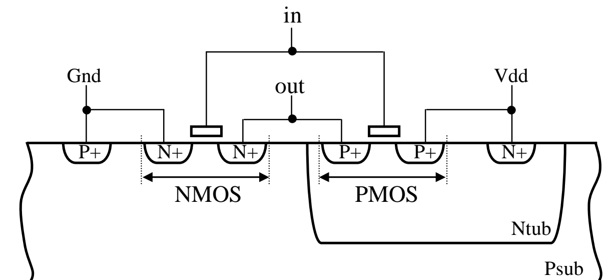


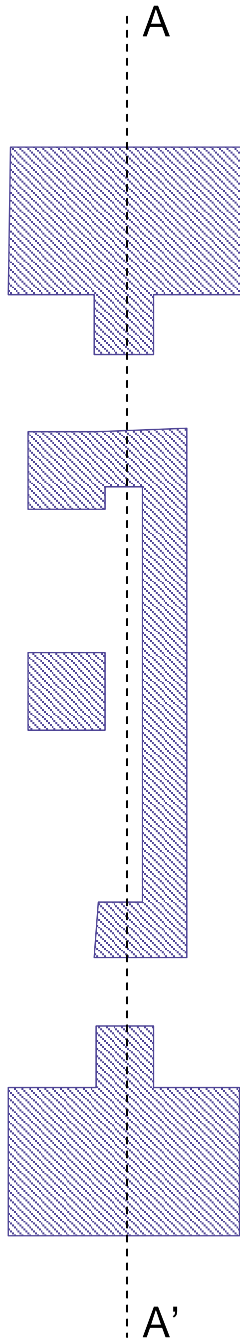
1ère métallisation – MET1



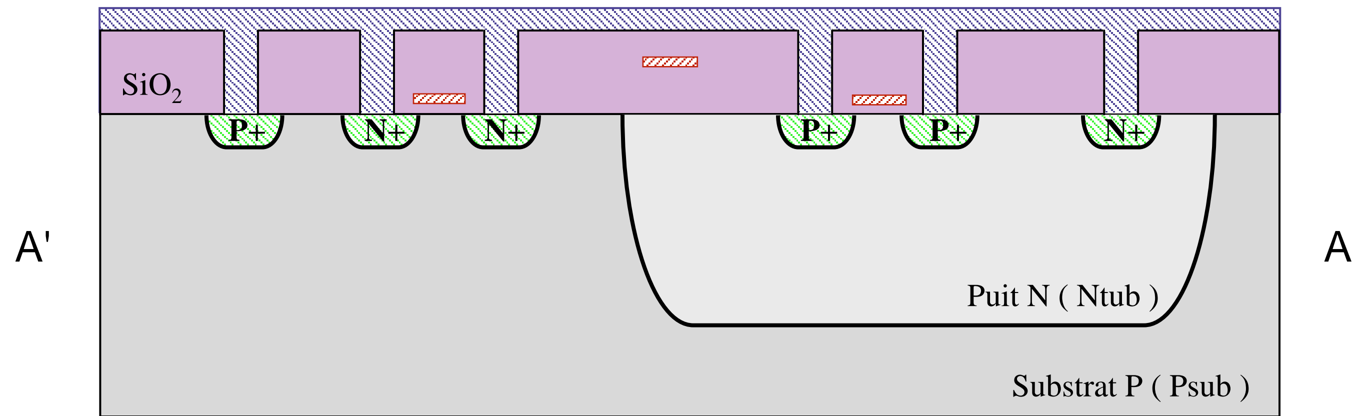


1. Métallisation uniforme.

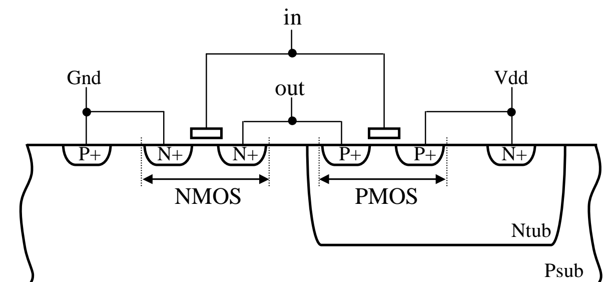


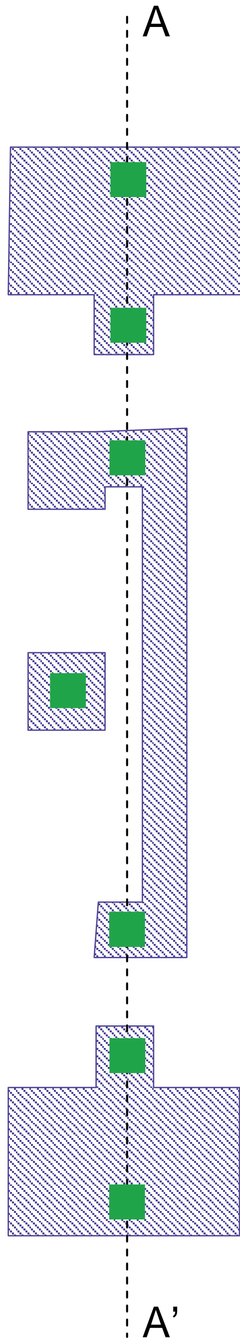


1ère métallisation – MET1

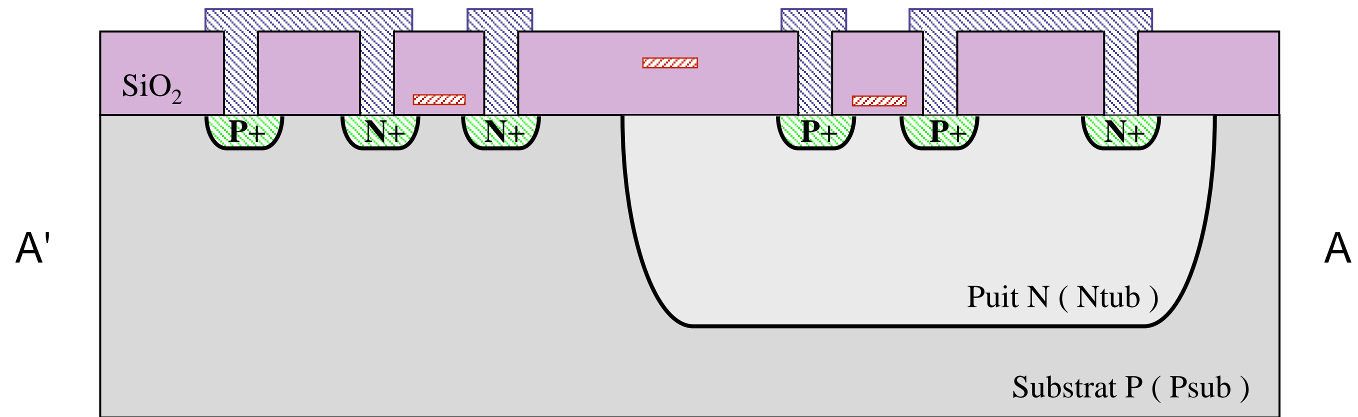


1. Métallisation uniforme.
2. Gravure du métal 1 (masque MET1).

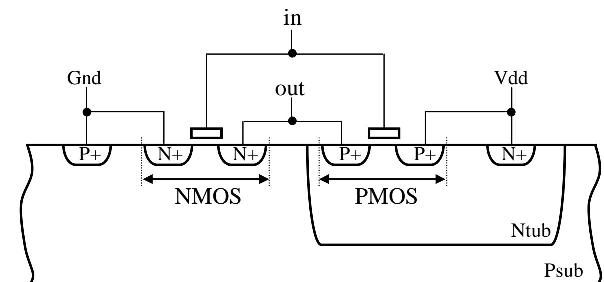




1ère métallisation – MET1



1. Métallisation uniforme.
2. Gravure du métal 1 (masque MET1).



Layout inverseur CMOS