

A  
Selected List of Resources  
on

**Verilog HDL  
&  
Xilinx FPGA**

Compiled  
By



Resource Centre

## Books available in Resource Centre

Sr. No.	Titles
1.	Arnold, Mark Gordon: Verilog digital computer design : algorithms into hardware New Jersey. Prentice Hall, 1999 621.392 ARN 017192
2.	Ashenden, Peter J. Digital design: an embedded systems approach using verilog Amsterdam. Elsevier, 2008 621.395 ASH 021341
3.	Bening, Lionel & Foster, Harry D. Principles of verifiable RTL design : a functional coding style supporting verification processes in verilog London. Kluwer Academic Publishers, 2000 621.392 BEN 002970
4.	Betz, Vaughn, Rose, Jonathan & Marquardt, Alexander Architecture and CAD for Deep-Submicron FPGAs London. Kluwer Academic Publishers, 1999 621.395 BET 002762
5.	Bhaskar, J. Verilog HDL Primer Hyderabad . BS Publications , 2001 621.382 BHA 004611
6.	Botros, Nazeih M. HDL programming fundamentals : VHDL and Verilog Hingham Da Vinci Engineering Press, 2007 621.392 BOT 016567
7.	Brown, Stephen & Vranesic, Zvonko Fundamentals of digital logic with verilog design New Delhi. Tata McGraw-Hill, 2003 621.392 BRO 004456
8.	Cavanagh, Joseph J. F. Digital design and Verilog HDL fundamentals Boca Raton. CRC Press, 2008

	621.395 CAV 023019
9.	Cavanagh, Joseph VeriIog HDL : digital design and modeling Boca Raton. CRC Press/Taylor & Francis, 2007 621.392 CAV 015513
10.	Chonnad, Shivakumar S. & Balachander, Needamangalam B. Verilog : frequently asked questions : language, applications and extensions. (Springer International Edition) New Delhi. Springer, 2004 621.392 CHO 015592
11.	Ciletti, Michael D. Advanced digital design with the verilog HDL New Delhi. Prentice Hall of India, 2005 621.395 CIL 012569
12.	Ciletti, Michael D. Modeling, synthesis, and rapid prototyping with the verilog HDL New Jersey. Prentice Hall, 1999 621.392 CIL 006522- 006523
13.	Coffman, Ken Real world FPGA design with Verilog New Jersey. Prentice Hall PTR, 1999 621.395 COF 021880
14.	Deschamps, Jean-Pierre, Bioul, Gery Jean Antoine & Sutter, Gustavo D. Synthesis of arithmetic circuits : FPGA, ASIC and embedded systems Hoboken. John Wiley & Sons, 2006 621.395 DES 017013
15.	Eccles, William J. Pragmatic logic San Rafael. Morgan & Claypool Publishers, 2007 621.395 ECC 020888
16.	FitzPatrick, Dan & Miller, Ira Analog behavioral modeling with the Verilog-A language Bolton. Kluwer Academic Publishers, 1998 621.381 FIT

	020105
17.	Foster, Harry D., Krolnik, Adam C. & Lacey, David J. Assertion-based design Boston. Kluwer Academic, 2003 621.395 FOS 008625
18.	George, Varghese & Rabaey, Jan M. Low-Energy FPGAs - architecture and design London. Kluwer Academic Publishers, 2001 621.3815 GEO 002752
19.	Ghosh, Sumit Hardware description languages : concepts and principles New Delhi. Prentice Hall of India, 2001 621.392 GH0 005111
20.	Gokhale, Maya B. & Graham, Paul S. Reconfigurable computing : accelerating computation with field-programmable gate arrays New York. Springer, 2005 621.395 GOK 013923
21.	Kundert, Kenneth S. & Zinke, Olaf Designer's guide to verilog AMS Boston. Kluwer Academic Publishers, 2004 621.392 KUN 012578
22.	Lee, James M. Verilog quickstart : a practical guide to simulation and synthesis in verilog London. Kluwer Academic Publishers, 1999 621.392 LEE 002969
23.	Lilja, David J. & Sapatnekar, Sachin S. Designing digital computer systems with Verilog Cambridge. Cambridge University Press, 2005 621.392 LIL 012819
24.	Maxfield, Clive Design warrior's guide to FPGAs : devices, tools, and flows New Delhi. Elsevier, 2004 621.395 MAX 014893
25.	Mazumder, Pinaki & Rudnick, Elizabeth M.

	Genetic algorithms for VLSI design, layout & test automation Delhi. Addison-Wesley, 1999 005.1 MAZ 000826
26.	Minns, Peter & Elliott, Ian D. FSM-based digital design using Verilog HDL Chichester. John Wiley & Sons, 2008 004.33 MIN 020404
27.	Mintz, Mike & Ekendahl, Robert Hardware verification with SystemVerilog : an object-oriented framework New York. Springer, 2007 621.392 MIN 019527
28.	Mitra, Swapnajit Principles of Verilog PLI London . Kluwer Academic Publishers , 2000 621.392 MIT 002974
29.	Murgai, Rajeev, Brayton, Robert K. & Sangiovanni-Vincentelli, Alberto Logic synthesis for field-programmable gate arrays London. Kluwer Academic Publishers, 1995 621.395 MUR 003047
30.	Navabi, Zainalabedin Embedded core design with FPGAs New York. McGraw-Hill, 2007 621.3815 NAV 016417
31.	Navabi, Zainalabedin Verilog digital system design: RT level synthesis, testbench and verification, 2 <sup>nd</sup> ed. 621.392 NAV 021814
32.	Oldfield, John V. & Dorf, Richard C. Field-programmable gate arrays : reconfigurable logic for rapid prototyping and implementation of digital systems New York. WileyJohn Wiley & Sons, 1995 621.395 OLD 017507
33.	Padmanabhan, T. R. & Sundari, B.Bala Tripura

	Design through Verilog HDL New Jersey. IEEE Press, 2003 005.74 PAD 008572
34.	Palnitkar, Samir Verilog HDL : a guide to digital design and synthesis Delhi. Pearson Education Asia, 2001 621.382 PAL 002267-02269
35.	Ramachandran, Seetharaman Digital VLSI systems design : a design manual for implementation of projects on FPGAs and ASICs using verilog Dordrecht. Springer, 2007 621.395 RAM 016719
36.	Reese, Robert B. & Thornton, Mitchell Aaron Introduction to logic synthesis using Verilog HDL San Rafael. Morgan & Claypool Publishers, 2006 621.392 REE 020883
37.	Sagdeo, Vivek Complete verilog book London. Kluwer Academic Publishers, 2000 621.392 SAG 002973
38.	Sandige, Richard S. Digital design essentials New Jersey. Prentice Hall, 2003 621.381 SAN 007300
39.	Smith, David R. Verilog styles for synthesis of digital systems New Jersey . Prentice Hall , 2000 621.392 SMI 002744
40.	Smith, Michael John Sebastian Application-specific integrated circuits Delhi. Pearson Education Asia, 2001 621.382 SMI 000779
41.	Spear, Chris SystemVerilog for verification : a guide to learning the testbench language features

	New York. Springer, 2006 621.392 SPE 014692
42.	Stine, James E. Digital computer arithmetic datapath design using verilog HDL. Boston. Kluwer Academic Publishers, 2004 621.395 STI 013461
43.	Sutherland, Stuart Verilog PLI Handbook: user's guide and comprehensive reference on the Verilog programming languages of a interface London. Kluwer Publishers, 1999 621.392 REF SUT 002971
44.	Sutherland, Stuart Verilog PLI handbook : a user's guide and comprehensive reference on the Verilog programming language interface, 2 <sup>nd</sup> ed. 621.392 SUT New Delhi. Springer, 2008 018477
45.	Sutherland, Stuart, Davidmann, Simon & Flake, Peter System Verilog for design, 2 <sup>nd</sup> ed. New York. Springer, 2006 621.392 SUT 014694
46.	Sutherland, Stuart & Mills, Don Verilog and system Verilog gotchas: 101 common coding errors and how to avoid them New York. Springer, 2007 621.392 SUT 019539
47.	Sutherland, Stuart Verilog – 2001 London. Kluwer Academic Press, 2002 621.3815 SUT 002748
48.	Thomas, Donald E. & Moorby, Philip R. Verilog hardware description language, 5 <sup>th</sup> ed. New Delhi. Kluwer Academic Publishers, 2002 621.395 THO 017680
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	Edition) New Delhi. Springer, 2007 621.395 TRI 015585
50.	Wakerly, John F. Digital design: principles and practices, 3 <sup>rd</sup> ed. New Delhi. Pearson Education Asia, 2001 621.382 WAK 010664- 010665
51.	Wolf, Wayne FPGA-based system design New Jersey. Prentice Hall, 2004 621.395 WOL 012573
52.	Zeidman, Bob Verilog designer's library New Jersey. Prentice Hall, 1999 621.392 ZEI 002239
53.	Zeidman, Bob Designing with FPCAS and CPLDS Lawrence. CMP Books, 2002 621.395 2 ZEI 005497
<b>E Books</b>	
54.	Handbook on Verilog HDL <a href="http://www.ge.infn.it/~pratolo/verilog/Handboook_Bucknell.pdf">http://www.ge.infn.it/~pratolo/verilog/Handboook_Bucknell.pdf</a>
55.	Verilog-A : Language Reference Manual - (Analog Extensions to Verilog HDL) <a href="http://www.vhdl.org/verilog-ams/htmlpages/public-docs/lrm/VerilogA/verilog-a-lrm-1-0.pdf">http://www.vhdl.org/verilog-ams/htmlpages/public-docs/lrm/VerilogA/verilog-a-lrm-1-0.pdf</a>

### CDs available in the Resource Centre

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1	Botros, Nazeih M. HDL programming fundamentals : VHDL and Verilog. Hingham. Da Vinci Engineering 621.392 BOT C01325
2	Brown, Stephen & Vranesic, Zvonko Fundamentals of digital logic with verilog design. 621.392 BRO C00498



3	Ciletti, Michael D. Advanced digital design with the verilog HDL. 621.395 CIL C00450, C00451 & C01021
4	Ciletti, Michael D. Xilinx student edition 4.2i. (ISE student ed.) 621.392 CIL C00671
5	Lee, James M. Verilog quickstart : a practical guide to simulation and synthesis in verilog. 621.392 LEE C00441
6	Minns, Peter & Elliott, Ian D. FSM-based digital design using Verilog HDL. [Synapticad : verilogger extreme] 004.33 MIN C01625
7	Navabi, Zainalabedin Verilog digital system design : RT level synthesis, testbench and verification, 2nd ed.. 621.392 NAV C01679
8	Navabi, Zainalabedin Verilog Digital System Design. 621.392 NAV C00636
9	Palnitkar, Samir Verilog HDL : a guide to digital design and synthesis. 621.382 PAL C00223 - C00237
10	Ramachandran, Seetharaman Digital VLSI systems design : a design manual for implementation of projects on FPGAs and ASICs using verilog. 621.395 RAM C01333
11	Sagdeo, Vivek Complete Verilog Book. 621.392 SAG C00446
12	Sandige, Richard S. Xilinx student edition 4.2i. 621.381 SAN C00715

13	Stine, James E. Digital computer arithmetic datapath design using verilog HDL. 621.395 STI C01119
14	Sutherland, Stuart Verilog PLI handbook : a user's guide and comprehensive reference on the Verilog programming language interface, 2nd ed.. 621.392 SUT C01449 C01449
15	Sutherland, Stuart Verilog PLI Handbook. [User`s Guide and Comprehensive Reference on the Verilog Programming Languages of a Interface] 621.392 REF SUT C00445
16	Thomas, Donald E. & Moorby, Philip R. Verilog hardware description language, 5th ed. 621.395 THO C01402
17	Thomas, Donald E. Verilog hardware description languages, 4th ed. 621.392 THO C00440
18	Zeidman, Bob Verilog Designer's Library. 621.392 ZEI C00437

### **Dissertations available in the Resource Centre**

Sr. No.	Titles
1	Choudhary, Vivek Kumar FPGA implementation of direct sequence spread spectrum techniques Gandhinagar. Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT), 2008 621.38456 CHO T00179
2	Rawat, Nitin FPGA implementation of image compression algorithm using wavelet transform Gandhinagar. Dhirubhai Ambani Institute of Information and Communication Technology (DA-IICT), 2008 621.3670151 RAW T00162

### **Other resources**

Sr. No.	Titles
1	<p data-bbox="418 279 979 317"><b>Verilog-1995 - Quick Reference Guide</b></p> <p data-bbox="418 321 1170 401"><a href="http://www.sutherland-hdl.com/online_verilog_ref_guide/vlog_ref_top.html">http://www.sutherland-hdl.com/online_verilog_ref_guide/vlog_ref_top.html</a></p> <p data-bbox="418 443 1373 522"><b>Designer's Guide to VHDL, HARDWARE DESCRIPTION LANGUAGE (HDL), FPGA (Field Programmable Gate Array)</b></p> <p data-bbox="418 527 789 564"><a href="http://www.doulos.com/">http://www.doulos.com/</a></p> <p data-bbox="418 606 1156 644"><b>A Verilog HDL Test Bench Primer : Application Note</b></p> <p data-bbox="418 648 1390 686"><a href="http://www.latticesemi.com/lit/docs/appnotes/cpld/an013_1.pdf">http://www.latticesemi.com/lit/docs/appnotes/cpld/an013_1.pdf</a></p> <p data-bbox="418 728 846 766"><b>SystemVerilog - Video Gallery</b></p> <p data-bbox="418 770 1146 808"><a href="http://www.doulos.com/knowhow/video_gallery/">http://www.doulos.com/knowhow/video_gallery/</a></p> <p data-bbox="418 850 690 888"><b>Verilog Useful links</b></p> <p data-bbox="418 892 1140 930"><a href="http://www.asic-world.com/verilog/verilinks.html">http://www.asic-world.com/verilog/verilinks.html</a></p>
2	<p data-bbox="418 972 599 1010"><b>Proceedings:</b></p> <p data-bbox="418 1052 1234 1131"><b>Verilog HDL Conference, 1996. Proceedings., 1996 IEEE International</b></p> <p data-bbox="418 1136 1328 1173"><a href="http://ieeexplore.ieee.org/xpl/RecentCon.jsp?punumber=3561">http://ieeexplore.ieee.org/xpl/RecentCon.jsp?punumber=3561</a></p> <p data-bbox="418 1215 1300 1295"><b>Verilog HDL Conference and VHDL International Users Forum, 1998. IVC/VIUF. Proceedings., 1998 International</b></p> <p data-bbox="418 1299 1330 1337"><a href="http://ieeexplore.ieee.org/xpl/RecentCon.jsp?punumber=5334">http://ieeexplore.ieee.org/xpl/RecentCon.jsp?punumber=5334</a></p>