CHAPTER 16

ANALOG INTEGRATED CIRCUITS

Chapter Outline

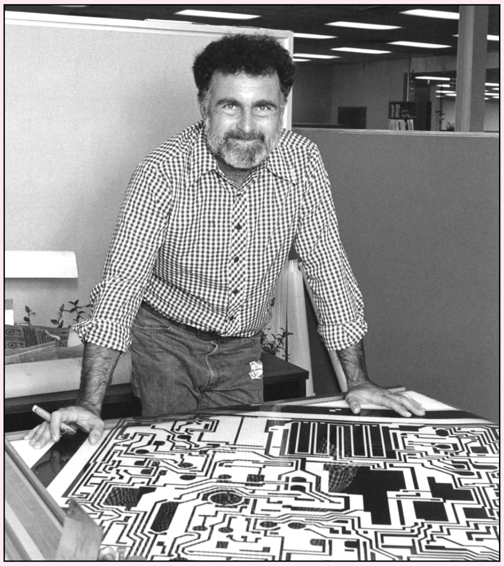
Chapter Goals

In Chapter 16 we concentrate on understanding integrated circuit design techniques that are based upon the characteristics of closely matched devices and look at a number of key building blocks of operational amplifiers and other ICs. Our goals are to:

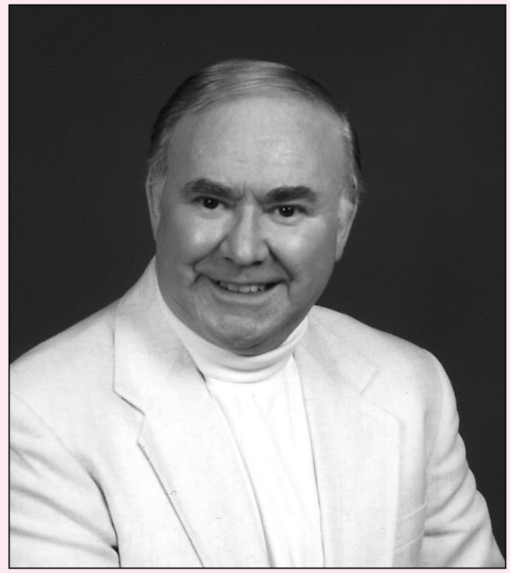
- Understand bipolar and MOS current mirror operation and mirror ratio errors
- Explore high output resistance current sources including cascode and Wilson current source circuits
- Learn to design current sources for use in both discrete and integrated circuits
- Add reference current circuit techniques to our kit of circuit building blocks. These circuits produce currents that exhibit a substantial degree of independence from power supply voltage including the V_{BE}-based reference and the Widlar current source.
- Investigate the operation and design of bandgap reference circuits, one of the most important techniques for providing an accurate reference voltage that is independent of power supply voltages and temperature
- Use current mirrors as active loads in differential amplifiers to increase the voltage gain of single-stage amplifiers to the amplification factor μ_f
- Learn how to include the effects of device mismatch in the calculation of amplifier performance measures such as CMRR
- Analyze the design of the classic μA741 operational amplifier
- Understand the techniques used to realize four-quadrant analog multipliers with large input signal range
- Continue to increase our understanding of SPICE simulation techniques

In Chapter 16, we explore several extremely clever and exciting circuits designed by two of the legends of integrated circuit design, Robert Widlar and Barrie Gilbert. Widlar developed the LM101 operational amplifier and many of the circuits that led to the design of the classic μA741 op amp. Widlar was also responsible for the bandgap reference. Gilbert invented a four-quadrant analog multiplier circuit referred to today as the Gilbert multiplier. The A741 circuit techniques spawned a broad range of follow-on designs that are still in use today. The bandgap reference forms the heart of most precision voltage references and voltage regulator circuits, and is also used as a temperature sensor in digital thermometry. Circuits related to the analog multiplier are used in RF mixers (the Gilbert mixer) and phase detectors in phase-locked loops.

Integrated circuit (IC) technology allows the realization of large numbers of virtually identical transistors. Although the absolute parameter tolerances of these devices are relatively poor, device characteristics can be matched to



(a)



(b)

Legends of Analog Design (a) Robert J. Widlar. (b) Barrie Gilbert
(a) Courtesy of National Semiconductor. (b) Courtesy of Analog Devices

within 1 percent or better. The ability to build devices with nearly identical characteristics has led to the development of special circuit techniques that take advantage of the tight matching of the device characteristics. Figures 16.1 and 16.2 show an example of the use of four matched transistors to improve the performance of the differential amplifier that we studied in the last chapter. The four devices are cross-connected to further improve the overall parameter matching and temperature tracking of the circuit.

Chapter 16 begins by exploring the use of matched transistors in the design of current sources, called **current mirrors,** in both MOS and bipolar technology. The cascode and Wilson current

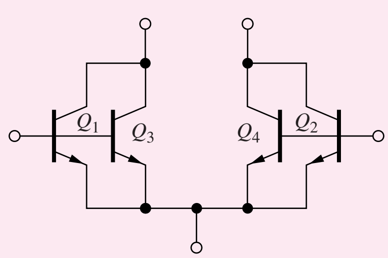


Figure 16.1 Differential amplifier formed with a cross-connected quad of identical transistors.

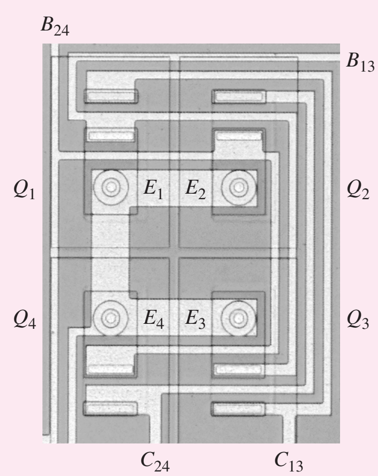


Figure 16.2 Layout of the cross-coupled transistor quad in Fig. 16.1.

sources are subsequently added to our repertoire of high-output-resistance current source circuits. Circuit techniques that can be used to achieve **power supply independent biasing** are also introduced.

We will also study the bandgap reference circuit which uses the well defined behavior of the pn junction to produce a precise output voltage that is highly independent of power supply voltage and temperature. The bandgap circuit is widely used in voltage references and voltage regulators.

The current mirror is often used to bias analog circuits and to replace load resistors in differential and operational amplifiers. This active-load circuit can substantially enhance the voltage gain capability of many amplifiers, and a number of MOS and bipolar circuit examples are presented. The chapter then discusses circuit techniques used in IC operational amplifiers, including the classic 741 amplifier. This design provides a robust, high-performance, general-purpose operational amplifier with breakdown-voltage protection of the input stage and short-circuit protection of the output stage. The final section looks at the precision four-quadrant analog multiplier design of Gilbert.

16.1 CIRCUIT ELEMENT MATCHING

Integrated circuit design is based directly on the ability to realize large numbers of transistors with nearly identical characteristics. Transistors are said to be **matched** when they have identical sets of device parameters: (I_S, β_{FO}, V_A) for the BJT, (V_{TN}, K', λ) for the MOSFET, or (I_{DSS}, V_P, λ) for the JFET. The planar geometry of the devices can easily be changed in integrated designs, and so the emitter area A_E of the BJT and the W/L ratio of the MOSFET become important circuit design parameters. (Remember from our study of MOS digital circuits in Part II that W/L represents a fundamental circuit design parameter.)

In integrated circuits, absolute parameter values may vary widely from fabrication process run to process run, with ±25 to 30 percent tolerances not uncommon (see Table 16.1). However, the matching between nearby circuit elements on a given IC chip is typically within a fraction of a percent. Thus, IC design techniques have been invented that rely heavily on **matched device** characteristics and resistor ratios rather than absolute parameter values. The circuits described in this chapter depend, for proper operation, on the tight device matching that can be realized through IC fabrication processes, and many will not operate correctly if built with mismatched discrete components. However, many of these circuits can be used in discrete circuit design if integrated transistor arrays are used in the implementation.

TABLE 16.1
IC Tolerances and Matching [1]

	ABSOLUTE TOLERANCE, %	MISMATCH, %
Diffused resistors	30	≤ 2
Ion-implanted resistors	5	≤ 1
V_{BE}	10	≤ 1
I_S, β_F, V_A	30	≤ 1
V_{TN}, V_{TP}	15	≤ 1
K', λ	30	≤ 1

EXERCISE: An IC resistor has a nominal value of 10 kΩ and a tolerance of ±30 percent. A particular process run has produced resistors with an average value 20 percent higher than the nominal value, and the resistors are found to be matched within 2 percent. What range of resistor values will occur in this process run?

ANSWER: 11.88 kΩ–12.12 kΩ

16.2 CURRENT MIRRORS

Current mirror biasing is an extremely important technique in integrated circuit design. Not only is it heavily used in analog applications, it also appears routinely in digital circuit design as well. Figure 16.3 shows the circuits for basic MOS and bipolar current mirrors. In Fig. 16.3(a), MOSFETs M_1 and M_2 are assumed to have identical characteristics (V_{TN}, K'_n, λ) and W/L ratios; in Fig. 16.3(b), the characteristics of Q_1 and Q_2 are assumed to be identical (I_S, β_{FO}, V_A). In both circuits, a **reference current** I_{REF} provides operating bias to the mirror, and the output current is represented by current I_O. These basic circuits are designed to have $I_O = I_{REF}$; that is, the output current mirrors the reference current—hence, the name "current mirror."

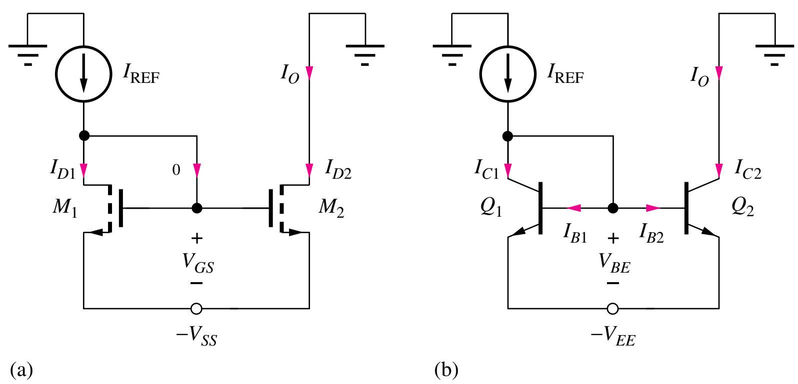


Figure 16.3 (a) MOS and (b) BJT current mirror circuits.

16.2.1 DC ANALYSIS OF THE MOS TRANSISTOR CURRENT MIRROR

Although the MOS current mirror was introduced in Chapter 4, a review of the basic analysis is repeated here so we can easily refer to the equations. Because the gate currents are zero for the MOSFETs, reference current I_{REF} must flow into the drain of M_1, which is forced to operate in pinch-off by the circuit connection because $V_{DS1} = V_{GS1} = V_{GS}$. V_{GS} must equal the value required for $I_{D1} = I_{REF}$. Assuming matched devices:[1]

$$I_{REF} = \frac{K_n}{2}(V_{GS1} - V_{TN})^2(1 + \lambda V_{DS1}) \qquad \text{or} \qquad V_{GS1} = V_{TN} + \sqrt{\frac{2I_{REF}}{K_{n1}(1 + \lambda V_{DS1})}} \tag{16.1}$$

[1] Matching between elements in the current mirror is very important; this is a case in which the $(1 + \lambda V_{DS})$ term is included in the dc, as well as ac, calculations.

Current I_O is equal to the drain current of M_2:

$$I_O = I_{D2} = \frac{K_n}{2}(V_{GS2} - V_{TN})^2(1 + \lambda V_{DS2}) \tag{16.2}$$

but the circuit connection forces $V_{GS2} = V_{GS1}$ and $V_{DS1} = V_{GS1}$. Substituting Eq. (16.1) into Eq. (16.2) yields

$$I_O = I_{\text{REF}}\frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \cong I_{\text{REF}} \tag{16.3}$$

For equal values of V_{DS}, the output current is identical to the reference current (that is, the output mirrors the reference current). Unfortunately in most circuit applications, $V_{DS2} \neq V_{DS1}$, and there is a slight mismatch between the output current and the reference current, as demonstrated in Ex. 16.1.

For convenience, we define the ratio of I_O to I_{REF} to be the **mirror ratio** MR given by

$$\text{MR} = \frac{I_O}{I_{\text{REF}}} = \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \tag{16.4}$$

EXAMPLE 16.1 OUTPUT CURRENT OF THE MOS CURRENT MIRROR

In this example, we find the output current for the standard current mirror configuration.

PROBLEM Calculate the output current I_O for the MOS current mirror in Fig. 16.3(a) if $V_{SS} = 10$ V, $K_n = 250\ \mu\text{A/V}^2$, $V_{TN} = 1$ V, $\lambda = 0.0133\ \text{V}^{-1}$, and $I_{\text{REF}} = 150\ \mu\text{A}$.

SOLUTION **Known Information and Given Data:** Current mirror circuit in Fig. 16.3(a); $V_{SS} = 10$ V; transistor parameters are given as $K_n = 250\ \mu\text{A/V}^2$, $V_{TN} = 1$ V, $\lambda = 0.0133\ \text{V}^{-1}$, and $I_{\text{REF}} = 150\ \mu\text{A}$

Unknowns: Output current I_O

Approach: Find V_{GS1} and V_{DS2} and then evaluate Eq. (16.3) to give the output current.

Assumptions: Transistors are identical and operating in the active region of operation

Analysis: We need to evaluate Eq. (16.3) and must find the value of V_{GS1} using Eq. (16.1). Since $V_{DS1} = V_{GS1}$, we can write

$$V_{DS1} = V_{TN} + \sqrt{\frac{2I_{\text{REF}}}{K_n}} = 1 + \sqrt{\frac{2(150\ \mu\text{A})}{250\dfrac{\mu\text{A}}{\text{V}^2}}} = 2.10\ \text{V}$$

in which we have neglected the $(1 + \lambda V_{DS1})$ term to simplify the dc bias calculation. Substituting this value and $V_{DS2} = 10$ V in Eq. (16.3):

$$I_O = (150\ \mu\text{A})\frac{[1 + 0.0133(10)]}{[1 + 0.0133(2.10)]} = 165\ \mu\text{A}$$

The ideal output current would be 150 μA, whereas the actual currents are mismatched by approximately 10 percent.

Check of Results: A double check shows the calculations to be correct. M_1 is pinched-off by connection, and M_2 will also be active as long as its drain-source voltage exceeds $(V_{GS1} - V_{TN})$, which is easily met in Fig. 16.3 since $V_{DS2} = 10$ V.

Discussion: We could attempt to improve the precision of our answer slightly by including the $(1 + \lambda V_{DS1})$ term in the evaluation of V_{GS1}. The solution then requires an iterative analysis that barely changes the value of I_O.

Computer-Aided Analysis: We can check our analysis directly with SPICE by setting the MOS transistor parameters to KP = 250 μA/V^2, VTO = 1 V, LEVEL = 1, and LAMBDA = 0. SPICE yields an output current of 150 μA with $V_{GS} = 2.095$ V. With nonzero λ, LAMBDA = 0.0133 V^{-1}, SPICE yields $I_O = 165$ μA with $V_{GS} = 2.081$ V. The values are in agreement with our hand calculations.

EXERCISE: Suppose we include the $(1 + \lambda V_{DS1})$ term in the evaluation of V_{GS1}. Show that the equation to be solved is

$$V_{DS1} = V_{TN} + \sqrt{\frac{2I_{REF}}{K_n(1 + \lambda V_{DS1})}}$$

Find the new value of V_{DS1} using the numbers in Ex. 16.1. What is the new value of I_O?

ANSWERS: 2.08 V; 165 μA

EXERCISE: Based on the numbers in Ex. 16.1, what is the minimum value of the drain voltage required to keep M_2 saturated in Fig. 16.3(a)?

ANSWER: −8.9 V

16.2.2 Changing the MOS Mirror Ratio

The power of the current mirror is greatly increased if the mirror ratio can be changed from unity. For the MOS current mirror, the ratio can easily be modified by changing the W/L ratios of the two transistors forming the mirror. In Fig. 16.4, for example, remembering that $K_n = K_n'(W/L)$ for the MOSFET, the K_n values of the two transistors are given by

$$K_{n1} = K_n'\left(\frac{W}{L}\right)_1 \quad \text{and} \quad K_{n2} = K_n'\left(\frac{W}{L}\right)_2 \tag{16.5}$$

Substituting these two different values of K_n in Eqs. (16.1) and (16.2) yields

$$I_O = I_{REF}\frac{K_{n2}(1 + \lambda V_{DS2})}{K_{n1}(1 + \lambda V_{DS1})} = I_{REF}\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \tag{16.6}$$

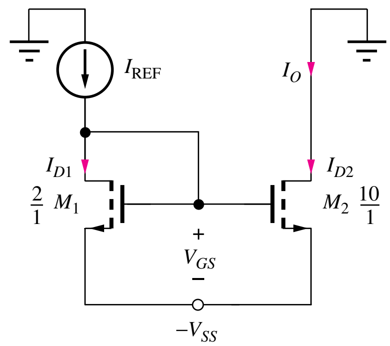


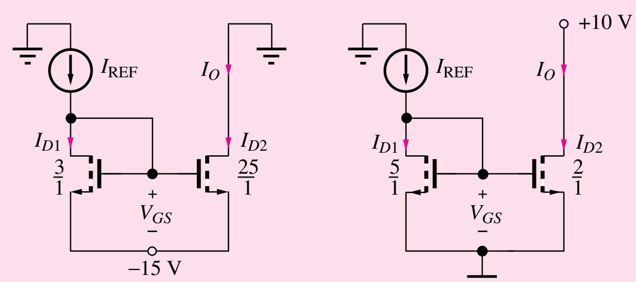
Figure 16.4 MOS current mirror with unequal (W/L) ratios.

The mirror ratio is given by

$$\text{MR} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} \tag{16.7}$$

In the ideal case ($\lambda = 0$) or for $V_{DS2} = V_{DS1}$, the mirror ratio is set by the ratio of the W/L values of the two transistors. For the particular values in Fig. 16.4, this design value of the mirror ratio would be 5, and the output current would be $I_O = 5I_{REF}$. However, the differences in V_{DS} will again create an error in the mirror ratio.

EXERCISE: (a) Calculate the mirror ratio for the MOS current mirrors in the figure here for $\lambda = 0$. (b) For $\lambda = 0.02\ \text{V}^{-1}$ if $V_{TN} = 1$ V, $K_n' = 25\ \mu\text{A/V}^2$, and $I_{REF} = 50\ \mu\text{A}$.



ANSWERS: 8.33, 0.400; 10.4, 0.462

16.2.3 DC ANALYSIS OF THE BIPOLAR TRANSISTOR CURRENT MIRROR

Analysis of the BJT current mirror in Fig. 16.3(b) is similar to that of the FET. Applying KCL at the collector of "diode-connected" transistor Q_1 yields

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} \quad \text{and} \quad I_O = I_{C2} \tag{16.8}$$

The currents needed to relate I_O to I_{REF} can be found using the transport model, noting that the circuit connection forces the two transistors to have the same base-emitter voltage V_{BE}:

$$\begin{aligned} I_{C1} &= I_S \exp\left(\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE1}}{V_A}\right) & I_{C2} &= I_S \exp\left(\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE2}}{V_A}\right) \\ \beta_{F1} &= \beta_{FO}\left(1+\frac{V_{CE1}}{V_A}\right) & \beta_{F2} &= \beta_{FO}\left(1+\frac{V_{CE2}}{V_A}\right) \\ I_{B1} &= \frac{I_S}{\beta_{FO}}\exp\left(\frac{V_{BE}}{V_T}\right) & I_{B2} &= \frac{I_S}{\beta_{FO}}\exp\left(\frac{V_{BE}}{V_T}\right) \end{aligned} \tag{16.9}$$

Substituting Eq. (16.9) into Eq. (16.7) and solving for $I_O = I_{C2}$ yields

$$I_O = I_{\text{REF}}\frac{\left(1+\dfrac{V_{CE2}}{V_A}\right)}{\left(1+\dfrac{V_{CE1}}{V_A}+\dfrac{2}{\beta_{FO}}\right)} = I_{\text{REF}}\frac{\left(1+\dfrac{V_{CE2}}{V_A}\right)}{\left(1+\dfrac{V_{BE}}{V_A}+\dfrac{2}{\beta_{FO}}\right)} \tag{16.10}$$

If the Early voltage were infinite, Eq. (16.10) would give a mirror ratio of

$$\text{MR} = \frac{I_O}{I_{\text{REF}}} = \frac{1}{1+\dfrac{2}{\beta_{FO}}} \tag{16.11}$$

and the output current would mirror the reference current, except for a small error due to the finite current gain of the BJT. For example, if $\beta_{FO} = 100$, the currents would match within 2 percent. As for the FET case, however, the collector-emitter voltage mismatch in Eq. (16.10) is generally more significant than the **current gain defect** term, as indicated in Ex. 16.2.

EXAMPLE 16.2 MIRROR RATIO CALCULATIONS

Compare the mirror ratios for MOS and BJT current mirrors operating with similar bias conditions and output resistances ($V_A = 1/\lambda$).

PROBLEM Calculate the mirror ratio for the MOS and BJT current mirrors in Fig. 16.3 for $V_{GS} = 2$ V, $V_{DS2} = 10$ V $= V_{CE2}$, $\lambda = 0.02$ V^{-1}, $V_A = 50$ V, and $\beta_{FO} = 100$. Assume $M_1 = M_2$ and $Q_1 = Q_2$.

SOLUTION **Known Information and Given Data:** Current mirror circuits in Fig. 16.3 with $M_2 = M_1$ and $Q_2 = Q_1$; $V_{SS} = 10$ V; operating voltages: $V_{GS} = 2$ V, $V_{DS2} = V_{CE2} = 10$ V and $V_{BE} = 0.7$ V; transistor parameters: $\lambda = 0.02$ V^{-1}, $V_A = 50$ V, and $\beta_{FO} = 100$

Unknowns: Mirror ratio MR for each current mirror

Approach: Use Eqs. (16.7) and (16.10) to determine the mirror ratios.

Assumptions: BJTs and MOSFETs are in the active region of operation respectively. Assume $V_{BE} = 0.7$ V for the BJTs and the MOSFETs are enhancement-mode devices.

Analysis: For the MOS current mirror,

$$\text{MR}_{\text{MOS}} = \frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} = \frac{\left[1+\dfrac{0.02}{\text{V}}(10\text{ V})\right]}{\left[1+\dfrac{0.02}{\text{V}}(2\text{ V})\right]} = 1.15$$

and for the BJT case

$$\text{MR}_{\text{BJT}} = \frac{\left(1+\dfrac{V_{CE2}}{V_A}\right)}{\left(1+\dfrac{2}{\beta_{FO}}+\dfrac{V_{CE1}}{V_A}\right)} = \frac{\left(1+\dfrac{10\text{ V}}{50\text{ V}}\right)}{\left(1+\dfrac{2}{100}+\dfrac{0.7\text{ V}}{50\text{ V}}\right)} = 1.16$$

Check of Results: A double check shows our calculations to be correct. M_1 is forced to be active by connection. M_2 has $V_{DS2} > V_{GS2}$ and will be pinched-off for $V_{TN} > 0$ (enhancement-mode transistor). Q_1 has $V_{CE} = V_{BE}$, so it is forced to be in the active region. Q_2 has $V_{CE2} > V_{BE2}$ and is also in the active region. The assumed regions of operation are valid.

Discussion: The FET and BJT mismatches are very similar — 15 percent and 16 percent, respectively. The current gain error is a small contributor to the overall error in the BJT mirror ratio.

Computer-Aided Analysis: We can easily perform an analysis of the current mirrors using SPICE, which will be done shortly as part of Ex. 16.3.

EXERCISE: What is the actual value of V_{BE} in the bipolar current mirror in Ex. 16.2 if $I_S = 0.1$ fA and $I_{REF} = 100$ μA? What is the minimum value of the collector voltage required to maintain Q_2 in the active region in Fig. 16.3(b)?

ANSWERS: 0.691 V; $-V_{EE} + 0.691$ V

16.2.4 Altering the BJT Current Mirror Ratio

In bipolar IC technology, the designer is free to modify the emitter area of the transistors, just as the W/L ratio can be chosen in MOS design. To alter the BJT mirror ratio, we use the fact that the saturation current of the bipolar transistor is proportional to its emitter area A_E and can be written as

$$I_S = I_{SO}\frac{A_E}{A} \tag{16.12}$$

I_{SO} represents the saturation current of a bipolar transistor with one unit of emitter area: $A_E = 1 \times A$. The actual dimensions associated with A are technology-dependent.

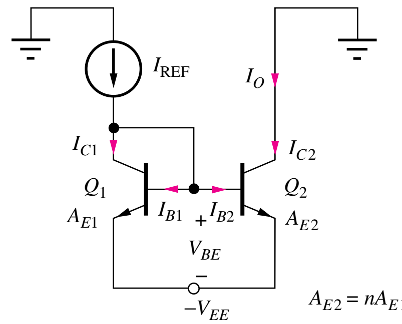


Figure 16.5 BJT current mirror with unequal emitter area.

By changing the relative sizes of the emitters (**emitter area scaling**) of the BJTs in the current mirror, the IC designer can modify the mirror ratio. For the modified mirror in Fig. 16.5,

$$I_{C1} = I_{SO}\frac{A_{E1}}{A}\exp\left(\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE1}}{V_A}\right) \qquad I_{C2} = I_{SO}\frac{A_{E2}}{A}\exp\left(\frac{V_{BE}}{V_T}\right)\left(1+\frac{V_{CE2}}{V_A}\right)$$
$$I_{B1} = \frac{I_{SO}}{\beta_{FO}}\frac{A_{E1}}{A}\exp\left(\frac{V_{BE}}{V_T}\right) \qquad I_{B2} = \frac{I_{SO}}{\beta_{FO}}\frac{A_{E2}}{A}\exp\left(\frac{V_{BE}}{V_T}\right) \tag{16.13}$$

Substituting these equations in Eq. (16.7) and then solving for I_O yields

$$I_O = nI_{REF}\frac{1+\dfrac{V_{CE2}}{V_A}}{1+\dfrac{V_{BE}}{V_A}+\dfrac{1+n}{\beta_{FO}}} \qquad \text{where } n = \frac{A_{E2}}{A_{E1}} \tag{16.14}$$

In the ideal case of infinite current gain and identical collector-emitter voltages, the mirror ratio would be determined only by the ratio of the two emitter areas:

$$\text{MR} = n \tag{16.15}$$

However, for finite current gain,

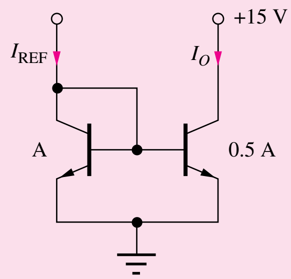
$$\text{MR} = \frac{n}{1+\dfrac{1+n}{\beta_{FO}}} \tag{16.16}$$

For example, suppose $A_{E2}/A_{E1} = 10$ and $\beta_{FO} = 100$; then the mirror ratio becomes

$$\text{MR} = 10\frac{1}{1+\dfrac{11}{100}} = 9.01 \tag{16.17}$$

A relatively large error (10 percent) is occurring even though the effect of collector-emitter voltage mismatch has been ignored. For high mirror ratios, the current gain error term can become quite important because the total number of units of base current increases directly with the mirror ratio.

EXERCISE: (a) Calculate the ideal mirror ratio for the BJT current mirrors in the figure below if $V_A = \infty$ and $\beta_{FO} = \infty$. (b) If $V_A = \infty$ and $\beta_{FO} = 75$. (c) If $V_A = 60$ V, $\beta_{FO} = 75$, and $V_{BE} = 0.7$ V.



ANSWERS: 0.500, 2.50; 0.490, 2.39; 0.606, 2.95

16.2.5 Multiple Current Sources

Analog circuits often require a number of different current sources to bias the various stages of the design. A single reference transistor, M_1 or Q_1, can be used to generate multiple output currents using the circuits in Figs. 16.6 and 16.7. In Fig. 16.6, the unusual connection of the gate terminals through the MOSFETs is being used as a "short-hand" method to indicate that all the gates are connected together. Circuit operation is similar to that of the basic current mirror. The reference current enters the **"diode-connected" transistor**—here, the MOSFET M_1—establishing gate-source voltage V_{GS}, which is then used to bias transistors M_2 through M_5, each having a different W/L ratio. Because there is no current gain defect in MOS technology, a large number of output transistors can be driven from one reference transistor.

EXERCISE: What are the four output currents in the circuit in Fig. 16.6 if $I_{REF} = 100$ μA and $\lambda = 0$ for all the FETs?

ANSWERS: 200 μA; 400 μA; 800 μA; 50.0 μA

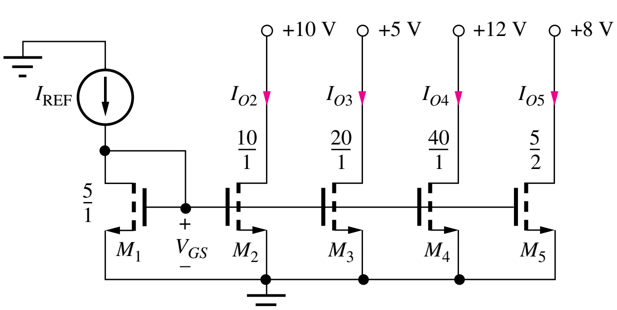


Figure 16.6 Multiple MOS current sources generated from one reference voltage.

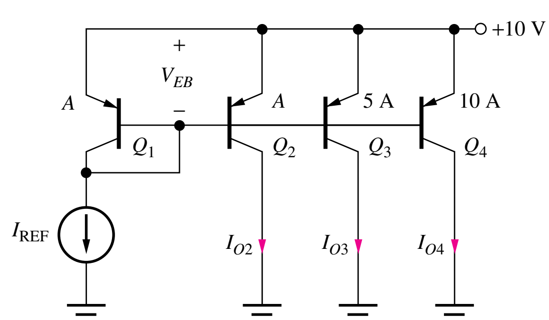


Figure 16.7 Multiple bipolar sources biased by one reference device.

EXERCISE: Recalculate the four output currents in the circuit in Fig. 16.6 if $\lambda = 0.02$ for all the FETs. Assume $V_{GS} = 2$ V.

ANSWERS: 231 μA; 423 μA; 954 μA; 55.8 μA

The situation is very similar in the *pnp* bipolar mirror in Fig. 16.7. Here again, the base terminals of the BJTs are extended through the transistors to simplify the drawing. In this circuit, reference current I_{REF} is supplied by diode-connected BJT Q_1 to establish the emitter-base reference voltage V_{EB}. V_{EB} is then used to bias transistors Q_2 to Q_4, each having a different emitter area relative to that of the reference transistor. Because the total base current increases with the addition of each output transistor, the base current error term gets worse as more transistors are added, which limits the number of outputs that can be used with the basic bipolar current mirror. The buffered current mirror in Sec. 16.2.6 was invented to solve this problem.

An expression for the output current from a given collector can be derived following the steps that led to Eq. (16.14):

$$I_{Oi} = n_i I_{REF} \frac{1 + \dfrac{V_{ECi}}{V_A}}{1 + \dfrac{V_{EB}}{V_A} + \dfrac{1 + \sum_{i=2}^{m} n_i}{\beta_{FO}}} \qquad \text{where } n_i = \frac{A_{Ei}}{A_{E1}} \tag{16.18}$$

EXERCISE: (a) What are the three output currents in the circuit in Fig. 16.5 if $I_{REF} = 10$ μA, $\beta_{FO} = 50$, and $V_A = \infty$ for all the BJTs? (b) Repeat for $V_A = 50$ V and $V_{EB} = 0.7$ V. Use Eq. (16.18).

ANSWERS: 7.46 μA, 37.3 μA, 74.6 μA; 8.86 μA, 44.3 μA, 88.6 μA

16.2.6 BUFFERED CURRENT MIRROR

The current gain defect in the bipolar current mirror can become substantial when a large mirror ratio is used or if many source currents are generated from one reference transistor. However, this error can be reduced greatly by using the circuit in Fig. 16.8, called a **buffered current mirror.** The current gain of transistor Q_3 is used to reduce the base current that is subtracted from the reference current. Applying KCL at the collector of transistor Q_1, and assuming that $V_A = \infty$

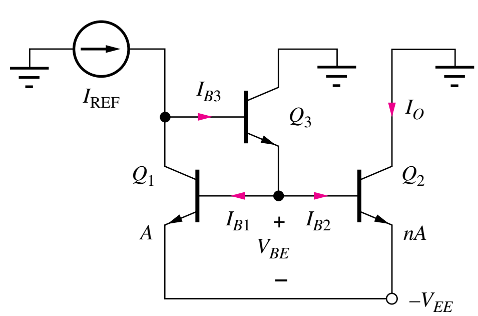


Figure 16.8 Buffered current mirror.

for simplicity, I_{C1} is expressed as

$$I_{C1} = I_{\text{REF}} - I_{B3} = I_{\text{REF}} - \frac{(1+n)\dfrac{I_{C1}}{\beta_{FO1}}}{\beta_{FO3}+1} \tag{16.19}$$

and solving for the collector current yields

$$I_O = nI_{C1} = nI_{\text{REF}} \frac{1}{1 + \dfrac{(1+n)}{\beta_{FO1}(\beta_{FO3}+1)}} \tag{16.20}$$

The error term in the denominator has been reduced by a factor of $(\beta_{FO3} + 1)$ from the error in Eq. (16.16).

EXERCISE: What is the mirror ratio and the percent error for the buffered current mirror in Fig. 16.8 if $\beta_{FO} = 50$, $n = 10$, and $V_A = \infty$ for all the BJTs? (b) What is that value of V_{CE2} required to balance the mirror if $\beta_{FO} = \infty$?

ANSWERS: 9.96, 0.430 percent; 1.4 V

16.2.7 Output Resistance of the Current Mirrors

Now that we have found the dc output current of the current mirror, we will focus on the second important parameter that characterizes the electronic current source — the output resistance. The output resistance of the basic current mirror can be found by referring to the ac model of Fig. 16.9. Diode-connected bipolar transistor Q_1 represents a simple two-terminal device, and its small-signal model is easily found using nodal analysis of Fig. 16.10:

$$\mathbf{i} = g_\pi \mathbf{v} + g_m \mathbf{v} + g_o \mathbf{v} = (g_m + g_\pi + g_o)\mathbf{v} \tag{16.21}$$

By factoring out g_m, an approximate result for the diode conductance is

$$\frac{\mathbf{i}}{\mathbf{v}} = g_m \left[1 + \frac{1}{\beta_o} + \frac{1}{\mu_f}\right] \cong g_m \qquad \text{and} \qquad R \cong \frac{1}{g_m} \tag{16.22}$$

for β_o and $\mu_f \gg 1$. The small-signal model for the diode-connected BJT is simply a resistor of value $1/g_m$. Note that this result is the same as the small-signal resistance r_d of an actual diode that was developed in Sec. 13.4.

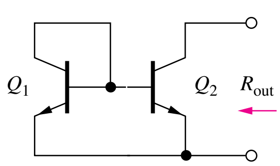


Figure 16.9 ac Model for the output resistance of the bipolar current mirror.

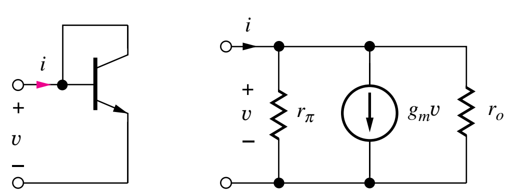


Figure 16.10 Model for "diode-connected" transistor.

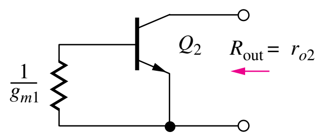


Figure 16.11 Simplified small-signal model for the bipolar current mirror.

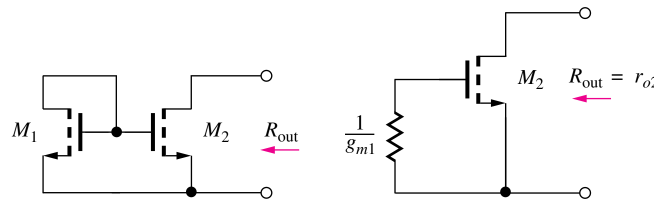


Figure 16.12 Output resistance of the MOS current mirror.

Using this diode model simplifies the ac model for the current mirror to that shown in Fig. 16.11. This circuit should be recognized as a common-emitter transistor with a Thévenin equivalent resistance $R_{th} = 1/g_m$ connected to its base; the output resistance just equals the output resistance r_{o2} of transistor Q_2.

The equation describing the small-signal model for the two-terminal "diode-connected" MOSFET is similar to that in Eq. (16.22) except that the current gain is infinite. Therefore, the two-terminal MOSFET is also represented by a resistor of value $1/g_m$, as in Fig. 16.12; the output resistance of the MOS current mirror is equal to r_{o2} of MOSFET M_2.

Thus, the output resistance and figure of merit (see Chapter 15) for the basic current mirror circuits are determined by output transistors Q_2 and M_2:

$$R_{out} = r_{o2} \qquad \text{and} \qquad V_{CS} \cong V_{A2} \qquad \text{or} \qquad \frac{1}{\lambda_2} \tag{16.23}$$

EXERCISE: What are the output resistances of sources I_{O2} and I_{O3} in Fig. 16.4 for $I_{REF} = 100\ \mu A$ and Fig. 16.5 for $I_{REF} = 10\ \mu A$ if $V_A = 1/\lambda = 50$ V?

ANSWERS: 260 kΩ, 130 kΩ; 6.77 MΩ, 1.35 MΩ

16.2.8 TWO-PORT MODEL FOR THE CURRENT MIRROR

We shall see shortly that the current mirror can be used not only as a dc current source but, in more complex circuits, as a current amplifier and active load. It will be useful to understand the small-signal behavior of the current mirror, redrawn as a two-port in Fig. 16.13. Because the current mirror has a current input and current output, the *h*-parameters represent a convenient parameter set to model the current mirror:

$$\begin{aligned} \mathbf{v_1} &= h_{11}\mathbf{i_1} + h_{12}\mathbf{v_2} \\ \mathbf{i_2} &= h_{21}\mathbf{i_1} + h_{22}\mathbf{v_2} \end{aligned} \tag{16.24}$$

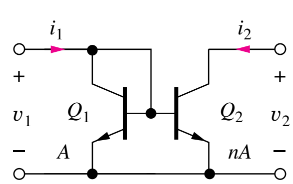


Figure 16.13 Current mirror as a two-port.

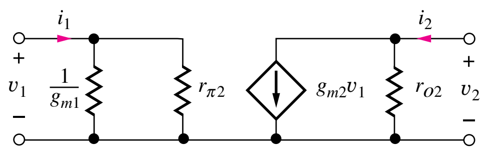


Figure 16.14 Small-signal model for the current mirror.

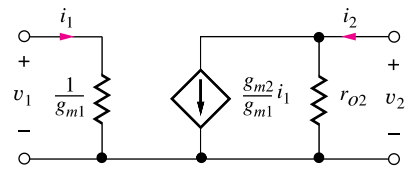


Figure 16.15 Simplified small-signal model for the current mirror.

The small-signal model for the current mirror is in Fig. 16.14, in which diode-connected transistor Q_1 is represented in its simplified form by $1/g_{m1}$.

From the circuit in Fig. 16.14,

$$h_{11} = \left.\frac{\mathbf{v_1}}{\mathbf{i_1}}\right|_{\mathbf{v_2}=0} = \frac{1}{(g_{m1}+g_{\pi 2})} = \frac{1}{g_{m1}\left(1+\dfrac{n}{\beta_{o2}}\right)} \cong \frac{1}{g_{m1}}$$

$$h_{12} = \left.\frac{\mathbf{v_1}}{\mathbf{v_2}}\right|_{\mathbf{i_1}=0} = 0 \tag{16.25}$$

$$h_{21} = \left.\frac{\mathbf{i_2}}{\mathbf{i_1}}\right|_{\mathbf{v_2}=0} = \frac{g_{m2}r_{\pi 2}}{1+g_{m1}r_{\pi 2}} = \frac{\beta_{o2}}{1+\dfrac{g_{m1}}{g_{m2}}\beta_{o2}} \cong \frac{g_{m2}}{g_{m1}} \cong \frac{I_{C2}}{I_{C1}} = n$$

$$h_{22} = \left.\frac{\mathbf{i_2}}{\mathbf{v_2}}\right|_{\mathbf{i_1}=0} = \frac{1}{r_{o2}}$$

Figure 16.15 shows the two-port model representation for these h-parameters. The bipolar current mirror has an input resistance of $1/g_{m1}$ determined by diode Q_1 and an output resistance equal to r_{o2} of Q_2. The current gain is determined approximately by the emitter-area ratio $n = A_{E2}/A_{E1}$. Be sure to remember to use the correct values of I_{C1} and I_{C2} when calculating the values of the small-signal parameters.

Analysis of the MOS current mirror yields similar results [or by simply setting $\beta_{o2} = \infty$ in Eq. (16.25)]:

$$h_{11} = \frac{1}{g_{m1}} \qquad h_{12} = 0$$

$$h_{21} = \frac{g_{m2}}{g_{m1}} \cong \frac{\left(\dfrac{W}{L}\right)_2}{\left(\dfrac{W}{L}\right)_1} \cong n \qquad h_{22} = \frac{1}{r_{o2}} \tag{16.26}$$

In this case, the current gain h_{21} is determined by the W/L ratios of the two FETs rather than by the bipolar emitter-area ratio.

EXERCISE: What are the values of I_{C1} and I_{C2} and the small-signal parameters for the current mirror in Fig. 16.5 if $I_{REF} = 100$ μA, $\beta_{FO} = 50$, $V_A = 50$ V, $V_{BE} = 0.7$ V, $V_{CE2} = 10$ V, and $n = 5$?

ANSWERS: 89.4 μA; 529 μA; 280 Ω; 0; 5.92; 113 kΩ

EXAMPLE 16.3 CALCULATING THE TWO-PORT PARAMETERS OF A CURRENT MIRROR USING SPICE

Transfer function analysis is used to find the two-port parameters of the BJT current mirror.

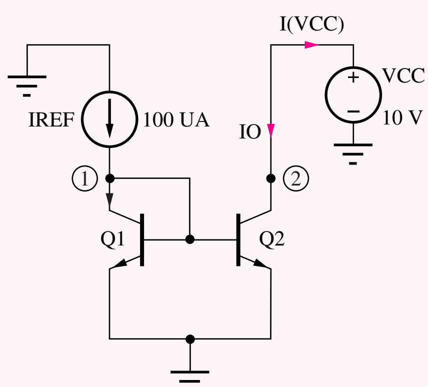
PROBLEM Use the transfer function capability of SPICE to find the two-port parameters of the BJT current mirror biased by a reference current of 100 μA and a power supply of +10 V.

SOLUTION **Known Information and Given Data:** A current mirror using bipolar transistors; $I_{REF} = 100\ \mu A$ and $V_{CC} = 10$ V

Unknowns: Output current I_O, V_{BE}, h_{11}, h_{12}, h_{21}, and h_{22} for the current mirror

Approach: Construct the circuit using the schematic editor in SPICE. Use the transfer function analysis to find the forward transfer function from I_{REF} to $I(V_{CC})$, and reverse transfer function from V_{CC} to node 1. The SPICE transfer function analysis automatically calculates three values: the requested transfer function, the resistance at the input source node, and the resistance at the output source node. However, since the output node is connected to V_{CC}, the output resistance calculated at that node will be zero, and two analyses will be required to find all the two-port parameters.

Assumptions: Use the current mirror with a single positive supply V_{CC} biased by current source I_{REF} as shown in the figure here. $V_A = 50$ V, $\beta_{FO} = 100$, and $I_S = 0.1$ fA.



Analysis: First, we must set the BJT parameters to the desired values: BF = 100, VAF = 50 V, and IS = 0.1 fA. An operating point and two transfer function analyses are used in this example. The first asks for the transfer function from input source I_{REF} to output variable $I(V_{CC})$. The operating point analysis yields $V(1) = 0.719$ V and $I_O = 116\ \mu A$. The transfer function analysis gives input resistance $h_{11} = (1/259\ \Omega)$ and current gain $h_{21} = +1.16$. The second analysis requests the transfer function from voltage source V_{CC} to node 1. SPICE analysis gives $h_{22} = 510\ k\Omega$, and $h_{12} = 2.59 \times 10^{-12}$.

Check of Results: Based on equation set (16.25) and the operating point results, we expect

$$h_{11} = (1/250\ \Omega) \qquad h_{12} = 0$$

$$h_{21} = +1.16 \qquad h_{22} = 517\ k\Omega$$

and we see that agreement with theory is very good.

Discussion: One should always try to understand and account for the differences between our theory and SPICE. In this example, the input resistance difference can be traced to the use of $V_T = 25.9$ mV. The nonzero value for h_{12} simply resulted from numerical noise in the calculation and is as close to zero as the computer could achieve in this particular case. Be careful not to make a sign error in interpreting the data for h_{21}. A negative sign appears in the SPICE output because of the assumed polarity of V_{CC} and $I(V_{CC})$. Finally, the SPICE model uses $r_o = (V_A + V_{CB})/I_C = 511$ kΩ, accounting for the small difference in the values of h_{22}.

EXERCISE: Use the transfer function capability of SPICE to find the two-port parameters for a MOS current mirror biased by a reference current of 100 μA and a power supply of +10 V. Assume $K_n = 1$ mA/V^2, $V_{TN} = 0.75$ V, and $\lambda = 0.02$/V.

ANSWERS: $I_O = 117$ μA, $V_{GS} = 1.19$ V; 4.55 mS, 0, 1.17, 512 kΩ

EXERCISE: Compare the answers in the previous exercise to hand calculations.

ANSWERS: $I_O = 117$ μA with $V_{GS} = 1.20$ V; 4.47 mS, 0, 1.17, 513 kΩ

16.2.9 The Widlar Current Source

Resistor R in the **Widlar**[2] **current source** circuit shown in the schematic in Fig. 16.16 gives the designer an additional degree of freedom in adjusting the mirror ratio of the current mirror. In this circuit, the difference in the base-emitter voltages of transistors Q_1 and Q_2 appears across resistor R and determines the output current I_O. Transistor Q_3 buffers the mirror reference transistor in Fig. 16.16(b) to minimize the effect of finite current gain.

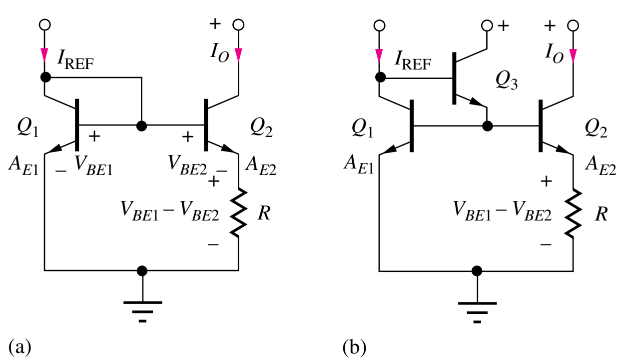


Figure 16.16 (a) Basic Widlar current source and (b) buffered Widlar source.

[2] Robert Widlar was a famous IC designer who made many lasting contributions to analog IC design. For examples, see references 2 and 3.

An expression for the output current may be determined from the standard expressions for the base-emitter voltage of the two bipolar transistors. In this analysis, we must accurately calculate the individual values of V_{BE1} and V_{BE2} because the behavior of the circuit depends on small differences in the values of these two voltages.

Assuming high current gain,

$$V_{BE1} = V_T \ln\left(1 + \frac{I_{REF}}{I_{S1}}\right) \cong V_T \ln \frac{I_{REF}}{I_{S1}}$$

and (16.27)

$$V_{BE2} = V_T \ln\left(1 + \frac{I_O}{I_{S2}}\right) \cong V_T \ln \frac{I_O}{I_{S2}}$$

The current in resistor R is equal to

$$I_{E2} = \frac{V_{BE1} - V_{BE2}}{R} = \frac{V_T}{R} \ln\left(\frac{I_{REF}}{I_O}\frac{I_{S2}}{I_{S1}}\right) \tag{16.28}$$

If the transistors are matched, then $I_{S1} = (A_{E1}/A)I_{SO}$ and $I_{S2} = (A_{E2}/A)I_{SO}$, and Eq. (16.28) can be rewritten as

$$I_O = \alpha_F I_{E2} \cong \frac{V_T}{R} \ln\left(\frac{I_{REF}}{I_O}\frac{A_{E2}}{A_{E1}}\right) \tag{16.29}$$

If I_{REF}, R, and the emitter-area ratio are all known, then Eq. (16.29) represents a transcendental equation that must be solved for I_O. The solution can be obtained by iterative trial and error or by using Newton's method.

Widlar Source Output Resistance

The ac model for the Widlar source in Fig. 16.16(a) represents a common-emitter transistor with resistor R in its emitter and a small value of R_{th} $(= 1/g_{m1})$ from diode Q_1 in its base, as indicated in Fig. 16.17. In normal operation, the voltage developed across resistor R is usually small ($\leq 10V_T$). Referring to Table 14.1, or by simplifying Eq. (15.182) for this case, we can reduce the output resistance of the source to

$$R_{out} \cong r_{o2}[1 + g_{m2}R] = r_{o2}\left[1 + \frac{I_O R}{V_T}\right] \tag{16.30}$$

in which $I_O R$ can be found from Eq. (16.28):

$$R_{out} \cong r_{o2}\left[1 + \ln \frac{I_{REF}}{I_O}\frac{A_{E2}}{A_{E1}}\right] = K r_{o2} \qquad \text{and} \qquad V_{CS} \cong K V_{A2} \tag{16.31}$$

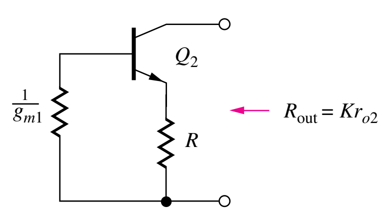


Figure 16.17 Widlar source output resistance – $K = 1 + \ln[(I_{REF}/I_{C2})(A_{E2}/A_{E1})]$

where

$$K = \left[1 + \ln \frac{I_{REF}}{I_O} \frac{A_{E2}}{A_{E1}}\right]$$

For typical values, $1 < K < 10$.

EXERCISE: What value of R is required to set $I_O = 25$ μA if $I_{REF} = 100$ μA and $A_{E2}/A_{E1} = 5$? What are the values of output resistance and K in Eq. (16.33) for this source if $V_A + V_{CE} = 75$ V?

ANSWERS: 3000 Ω; 12 MΩ, 4

EXERCISE: Find the output current in the Widlar source if $I_{REF} = 100$ μA, $R = 100$ Ω, and $A_{E2} = 10A_{E1}$. What are the values of output resistance and K in Eq. (16.31) for this source if $V_A + V_{CE} = 75$ V?

ANSWERS: 301 μA; 551 kΩ, 2.20

16.2.10 THE PTAT VOLTAGE

The voltage developed across resistor R in Fig. 16.16 represents an extremely useful quantity because it is directly **p**roportional **t**o **a**bsolute **t**emperature (referred to as PTAT). V_{PTAT} is equal to the difference in the two base-emitter voltages described by Eq. (16.27):

$$V_{PTAT} = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\frac{A_{E2}}{A_{E1}}\right) = \frac{kT}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\frac{A_{E2}}{A_{E1}}\right) \tag{16.32}$$

and the change of V_{PTAT} with temperature is

$$\frac{\partial V_{PTAT}}{\partial T} = +\frac{k}{q} \ln\left(\frac{I_{C1}}{I_{C2}}\frac{A_{E2}}{A_{E1}}\right) = +\frac{V_{PTAT}}{T} \tag{16.33}$$

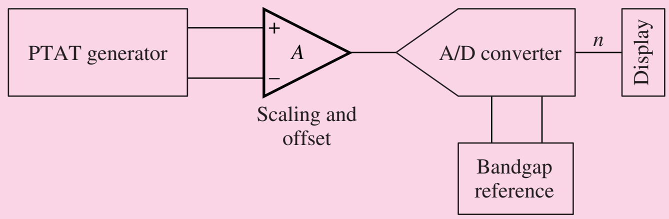
For example, suppose $T = 300$ K, $I_{C1} = I_{C2}$ and $A_{E2} = 10A_{E1}$. Then $V_{PTAT} = 59.6$ mV with a temperature coefficient of slightly less than $+0.2$ mV/K.

The PTAT voltage developed in the Widlar cell, combined with an analog-to-digital converter, forms the heart of all of today's highly accurate electronic thermometers. We will see the PTAT voltage again shortly in the form of the bandgap voltage reference, another extremely important circuit building block.

ELECTRONICS IN ACTION

PTAT Voltage Based Digital Thermometry

The PTAT generator produces a well-defined output voltage that is used in many of today's digital thermometers as in the block diagram on the next page. The output of the PTAT circuit is scaled and the offset voltage is shifted to provide an output voltage that directly represents either the Fahrenheit or Celsius temperature scales. The analog voltage is converted to a digital representation by an A/D converter and the digital output is sent to an alphanumeric display. The scaling and offset shift can also be easily done in digital form after the A/D conversion operation is performed.



Block diagram of a digital thermometer.

Wireless digital thermometer.

16.2.11 The MOS Version of the Widlar Source

Figure 16.18 is the MOS version of the Widlar source. In this circuit, the difference between the gate-source voltages of transistors M_1 and M_2 appears across resistor R, and I_O can be expressed as

$$I_O = \frac{V_{GS1} - V_{GS2}}{R} = \frac{\sqrt{\dfrac{2I_{\text{REF}}}{K_{n1}}} - \sqrt{\dfrac{2I_O}{K_{n2}}}}{R}$$

or (16.34)

$$I_O = \frac{1}{R}\sqrt{\frac{2I_{\text{REF}}}{K_{n1}}}\left(1 - \sqrt{\frac{I_O}{I_{\text{REF}}}\frac{(W/L)_1}{(W/L)_2}}\right)$$

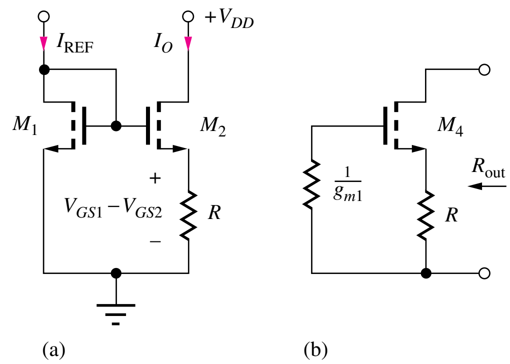


Figure 16.18 (a) MOS Widlar source and (b) small-signal model.

Dividing through by I_{REF},

$$\frac{I_O}{I_{REF}} = \frac{1}{R}\sqrt{\frac{2}{K_{n1}I_{REF}}}\left(1 - \sqrt{\frac{I_O}{I_{REF}}\frac{(W/L)_1}{(W/L)_2}}\right) \tag{16.35}$$

If I_O is known, then I_{REF} can be calculated directly from Eq. (16.34). If I_{REF}, R, and the W/L ratios are known, then Eq. (16.35) can be written as a quadratic equation in terms of $\sqrt{I_O/I_{REF}}$:

$$\left(\sqrt{\frac{I_O}{I_{REF}}}\right)^2 + \frac{1}{R}\sqrt{\frac{2}{K_{n1}I_{REF}}}\sqrt{\frac{(W/L)_1}{(W/L)_2}}\left(\sqrt{\frac{I_O}{I_{REF}}}\right) - \frac{1}{R}\sqrt{\frac{2}{K_{n1}I_{REF}}} = 0 \tag{16.36}$$

MOS Widlar Source Output Resistance

In Fig. 16.18(b), the small-signal model for the MOS Widlar source is recognized as a common-source stage with resistor R in its source. Therefore, from Table 14.1,

$$R_{out} = r_{o2}(1 + g_{m2}R) \tag{16.37}$$

EXERCISE: (a) Find the output current in Fig. 16.18(a) if $I_{REF} = 200\ \mu A$, $R = 2\ k\Omega$, and $K_{n2} = 10K_{n1} = 250\ \mu A/V^2$. (b) What is R_{out} if $\lambda = 0.02/V$ and $V_{DS} = 10\ V$?

ANSWERS: 764 μA; 176 kΩ

16.3 HIGH-OUTPUT-RESISTANCE CURRENT MIRRORS

In the discussion of differential amplifiers in Chapter 15, we found that current sources with very high output resistances are needed to achieve good CMRR. The basic current mirrors discussed in the previous sections have a figure of merit V_{CS} equal to V_A or $1/\lambda$; that for the Widlar source is only a few times higher. This section continues our introduction to current mirrors by discussing two additional circuits, the Wilson current source and the cascode current source, which enhance the value of V_{CS} to the order of $\beta_o V_A$ or μ_f/λ.

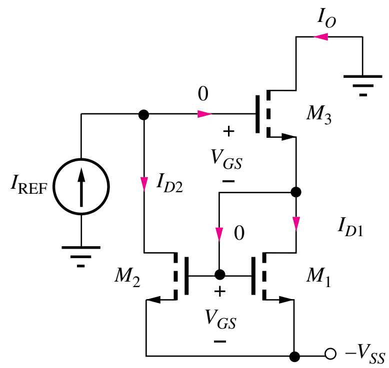


Figure 16.19 MOS Wilson current source.

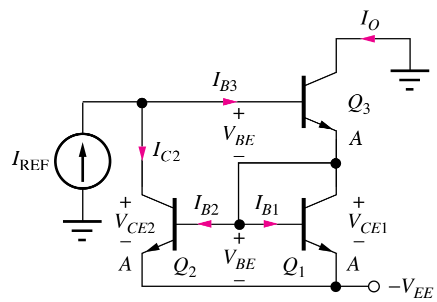


Figure 16.20 Original Wilson current source circuit using BJTs.

16.3.1 The Wilson Current Sources

The **Wilson current sources** [4] depicted in Figs. 16.19 and 16.20 use the same number of transistors as the buffered current mirror but achieve much higher output resistance; it is often used in applications requiring precisely matched current sources. In the MOS version, the output current is taken from the drain of M_3, and M_1 and M_2 form a current mirror. During circuit operation, the three transistors are all pinched-off and in the active region. Because the gate current of M_3 is zero, I_{D2} must equal reference current I_{REF}. If the transistors all have the same W/L ratios, then

$$V_{GS3} = V_{GS1} = V_{GS} \qquad \text{because } I_{D3} = I_{D1}$$

The current mirror requires

$$I_{D2} = I_{D1}\frac{1 + 2\lambda V_{GS}}{1 + \lambda V_{GS}}$$

and because $I_O = I_{D3}$ and $I_{D3} = I_{D1}$, the output current is given by

$$I_O = I_{REF}\frac{1 + \lambda V_{GS}}{1 + 2\lambda V_{GS}} \qquad \text{where } V_{GS} \cong V_{TN} + \sqrt{\frac{2I_{REF}}{K_n}} \tag{16.38}$$

For small λ, $I_O \cong I_{REF}$. For example, if $\lambda = 0.02$/V and $V_{GS} = 2$ V, then I_O and I_{REF} differ by 3.7 percent.

The Wilson source actually appeared first in bipolar form as drawn in Fig. 16.20. The circuit operates in a manner similar to the MOS source, except for the loss of current from I_{REF} to the base of Q_3 and the current gain error in the mirror formed by Q_1 and Q_2. Applying KCL at the base of Q_3,

$$I_{REF} = I_{C2} + I_{B3} \tag{16.39}$$

in which I_{C2} and I_{B3} are related through the current mirror formed by Q_1 and Q_2:

$$I_{C2} = \frac{1 + \dfrac{2V_{BE}}{V_A}}{1 + \dfrac{V_{BE}}{V_A} + \dfrac{2}{\beta_{FO}}} I_{E3} = \frac{1 + \dfrac{2V_{BE}}{V_A}}{1 + \dfrac{V_{BE}}{V_A} + \dfrac{2}{\beta_{FO}}} (\beta_{FO} + 1) I_{B3} \tag{16.40}$$

Note in Fig. 16.20 that $V_{CE1} = V_{BE}$ and $V_{CE2} = 2V_{BE}$.

Directly combining Eqs. (16.37) and (16.38) yields a messy expression that is difficult to interpret. However, if we assume the error terms are small, then we can eventually reduce (with considerable effort) the expression to the following approximate result:

$$I_O \cong I_{\text{REF}} \frac{1 + \dfrac{V_{BE}}{V_A}}{1 + \dfrac{2}{\beta_{FO}(\beta_{FO}+2)} + \dfrac{2V_{BE}}{V_A}} \tag{16.41}$$

For $\beta_{FO} = 50$, $V_A = 60$ V, and $V_{BE} = 0.7$ V, the mirror ratio is 0.988. The primary source of error results from the collector-emitter voltage mismatch between transistors Q_1 and Q_2. The base current error has been reduced to less than 0.1 percent of I_{REF}.

The errors due to drain-source voltage mismatch in Fig. 16.19, or collector-emitter voltage mismatch in Fig. 16.20, may still be too large for use in precision circuits, but this problem can be significantly reduced by adding one more transistor to balance the circuit. In Fig. 16.21, transistor Q_4 reduces the collector-emitter voltage of Q_2 by one V_{BE} drop and balances the collector-emitter voltages of Q_1 and Q_2:

$$V_{CE2} = V_{BE1} + V_{BE3} - V_{BE4} = V_{BE} + V_{BE} - V_{BE} = V_{BE}$$

All four transistors are operating at approximately the same value of collector current, and the values of V_{BE} are all the same if the devices are matched with equal emitter areas.

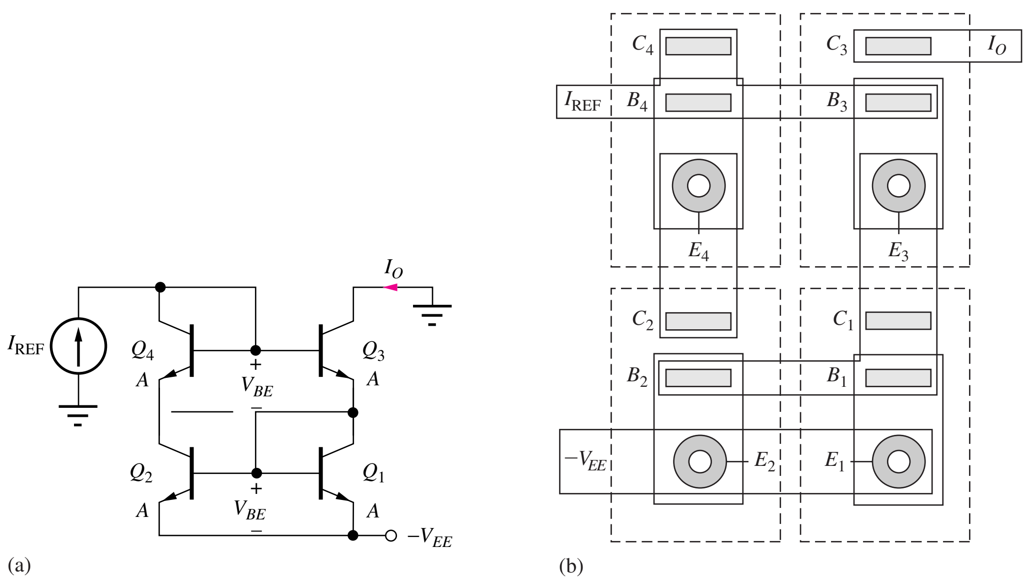


Figure 16.21 (a) Wilson source using balanced collector-emitter voltages. (b) Layout of Wilson source.

EXERCISE: Draw a voltage-balanced version of the MOS Wilson source by adding one additional transistor to the circuit in Fig. 16.19.

ANSWER: See Prob. 16.43.

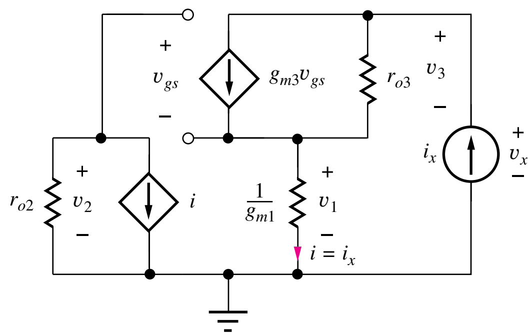


Figure 16.22 Small-signal model for the MOS version of the Wilson source.

16.3.2 Output Resistance of the Wilson Source

The primary advantage of the Wilson source over the standard current mirror is its greatly increased output resistance. The small-signal model for the MOS version of the Wilson source is given in Fig. 16.22, in which test current i_x is applied to determine the output resistance.

The current mirror formed by transistors M_1 and M_2 is represented by its simplified two-port model assuming $n = 1$. Voltage v_x is determined from

$$\mathbf{v_x} = \mathbf{v_3} + \mathbf{v_1} = [\mathbf{i_x} - g_{m3}\mathbf{v_{gs}}]r_{o3} + \mathbf{v_1} \tag{16.42}$$

where

$$\mathbf{v_{gs}} = \mathbf{v_2} - \mathbf{v_1} \qquad \text{with } \mathbf{v_1} = \frac{\mathbf{i_x}}{g_{m1}} \text{ and } \mathbf{v_2} = -\mu_{f2}\mathbf{v_1} \tag{16.43}$$

Combining these equations, and recognizing that $g_{m1} = g_{m2}$ for $n = 1$ yields

$$R_{\text{out}} = \frac{\mathbf{v_x}}{\mathbf{i_x}} = r_{o3}\left[\mu_{f2} + 2 + \frac{1}{\mu_{f2}}\right] \cong \mu_{f2}r_{o3} \tag{16.44}$$

and

$$V_{CS} = I_{D3}\mu_{f2}\frac{1 + \lambda_3 V_{DS3}}{\lambda_3 I_{D3}} \cong \frac{\mu_{f2}}{\lambda_3} \tag{16.45}$$

Analysis of the bipolar source is somewhat more complex because of the finite current gain of the BJT and yields the following result:

$$R_{\text{out}} \cong \frac{\beta_{o3}r_{o3}}{2} \qquad \text{and} \qquad V_{CS} \cong \frac{\beta_o V_A}{2} \tag{16.46}$$

Derivation of this equation is left for Prob. 16.41.

Exercise: Calculate R_{out} for the Wilson source in Fig. 16.20 if $\beta_F = 150$, $V_A = 50$ V, $V_{EE} = 15$ V, and $I_O = I_{\text{REF}} = 50$ μA. What would be the output resistance of a standard current mirror operating at the same current?

Answer: 96.6 MΩ versus 1.30 MΩ

EXERCISE: Use SPICE to find the output current and output resistance of the Wilson source in the previous exercise.

ANSWERS: $I_O = 49.5\ \mu A$; 118 MΩ

16.3.3 CASCODE CURRENT SOURCES

We learned in Chapter 15 that the output resistance of the cascode connection (C-E/C-B cascade) of two transistors is very high, approaching $\mu_f r_o$ for the FET case and $\beta_o r_o$ for the BJT circuit. Figure 16.23 shows the implementation of the MOS and BJT **cascode current sources** using current mirrors.

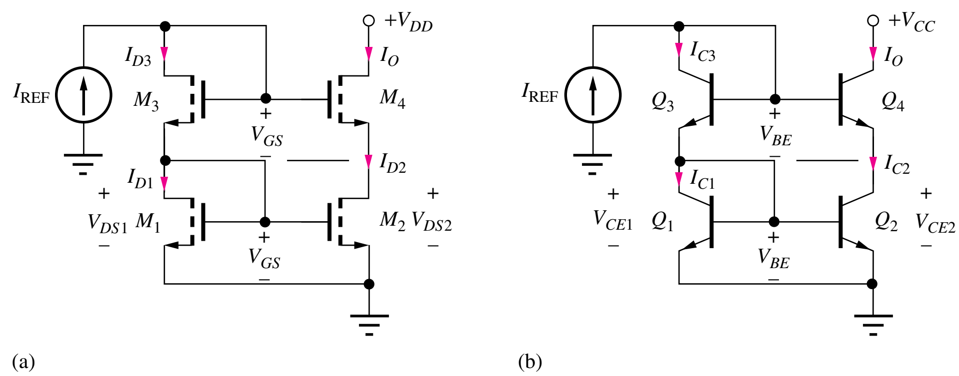


Figure 16.23 (a) MOS and (b) BJT cascode current sources.

In the MOS circuit in Fig. 16.23(a), $I_{D1} = I_{D3} = I_{\text{REF}}$. The current mirror formed by M_1 and M_2 forces the output current to be approximately equal to the reference current because $I_O = I_{D4} = I_{D2}$. Diode-connected transistor M_3 provides a dc bias voltage to the gate of M_4 and balances V_{DS1} and V_{DS2}. If all transistors are matched with the same W/L ratios, then the values of V_{GS} are all the same, and V_{DS2} equals V_{DS1}:

$$V_{DS2} = V_{GS1} + V_{GS3} - V_{GS4} = V_{GS} + V_{GS} - V_{GS} = V_{GS} = V_{DS1}$$

Thus the M_1-M_2 current mirror is precisely balanced, and $I_O = I_{\text{REF}}$.

The BJT source in Fig. 16.23(b) operates in the same manner. For $\beta_F = \infty$, $I_{\text{REF}} = I_{C3} = I_{C1}$ on the reference side of the source. Q_1 and Q_2 form a current mirror, which sets $I_O = I_{C4} = I_{C2} = I_{C1} = I_{\text{REF}}$. Diode Q_3 provides the bias voltage at the base of Q_4 needed to keep Q_2 in the active region and balances the collector-emitter voltages of the current mirror:

$$V_{CE2} = V_{BE1} + V_{BE3} - V_{BE4} = 2V_{BE} - V_{BE} = V_{BE} = V_{CE1}$$

16.3.4 OUTPUT RESISTANCE OF THE CASCODE SOURCES

Figure 16.24 shows the small-signal model for the MOS cascode source; the two-port model has been used for the current mirror formed of transistors M_1 and M_2. Because current i represents the gate current of M_4, which is zero, the circuit can be reduced to that on the right in Fig. 16.24, which should be recognized as a common-source stage with resistor r_{o2} in its source. Thus, its output

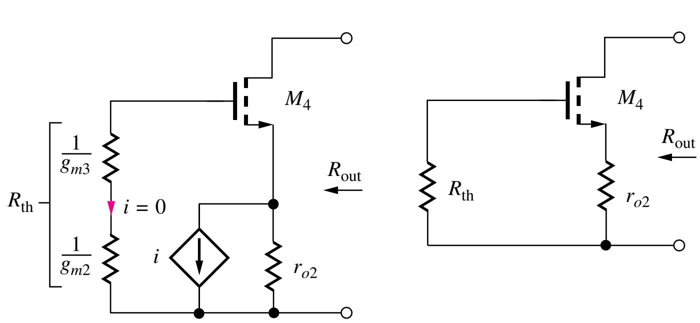


Figure 16.24 Small-signal model for the MOS cascode source.

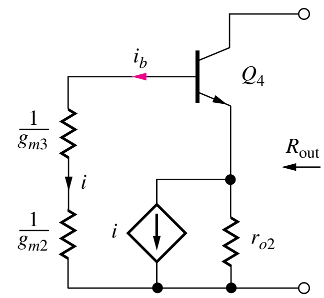


Figure 16.25 Small-signal model for the BJT cascode source.

resistance is

$$R_{\text{out}} = r_{o4}(1 + g_{m4}r_{o2}) \cong \mu_{f4}r_{o2} \qquad \text{and} \qquad V_{CS} \cong \frac{\mu_{f4}}{\lambda_2} \cong \frac{\mu_{f4}}{\lambda_4} \tag{16.47}$$

Analysis of the output resistance of the BJT source in Fig. 16.25 is again more complex because of the finite current gain of the BJT. If the base of Q_4 were grounded, then the output resistance would be just equal to that of the cascode stage, $\beta_o r_o$. However, the base current i_b of Q_4 enters the current mirror, doubles the output current, and causes the overall output resistance to be reduced by a factor of 2:

$$R_{\text{out}} \cong \frac{\beta_{o4}r_{o4}}{2} \qquad \text{and} \qquad V_{CS} \cong \frac{\beta_{o4}V_{A4}}{2} \tag{16.48}$$

Detailed calculation of this result is left as Prob. 16.67.

EXERCISE: Calculate the output resistance of the MOS cascode current source in Fig. 16.23(a) and compare it to that of a standard current mirror if $I_O = I_{\text{REF}} = 50$ μA, $V_{DD} = 15$ V, $K_n = 250$ μA/V^2, $V_{TN} = 0.8$ V, and $\lambda = 0.015$ V^{-1}.

ANSWER: 379 MΩ versus 1.63 MΩ including all λV_{DS} terms

EXERCISE: Use SPICE to find the output current and output resistance of the cascode current source in the previous exercise.

ANSWERS: $I_O = 50.0$ μA; 382 MΩ

EXERCISE: Calculate the output resistance of the BJT cascode current source in Fig. 16.23(b) and compare it to that of a standard current mirror if $I_O = I_{\text{REF}} = 50$ μA, $V_{CC} = 15$ V, $\beta_o = 100$, and $V_A = 67$ V.

ANSWER: 81.3 MΩ versus 1.63 MΩ

16.3.5 Current Mirror Summary

Table 16.2 is a summary of the current mirror circuits discussed in this chapter. The cascode and Wilson sources can achieve very high values of V_{CS} and often find use in the design of differential and operational amplifiers as well as in many other analog circuits.

TABLE 16.2
Comparison of the Basic Current Mirrors

TYPE OF SOURCE	R_{out}	V_{CS}	TYPICAL VALUES OF V_{CS}
Resistor	R	V_{EE}	15 V
Two-transistor mirror	r_o	V_A or $\frac{1}{\lambda}$	75 V
Cascode BJT	$\frac{\beta_o r_o}{2}$	$\frac{\beta_o V_A}{2}$	5000 V
Cascode FET	$\mu_f r_o$	$\frac{\mu_f}{\lambda}$	>5000 V
BJT Wilson	$\frac{\beta_o r_o}{2}$	$\frac{\beta_o V_A}{2}$	5000 V
FET Wilson	$\mu_f r_o$	$\frac{\mu_f}{\lambda}$	>5000 V

DESIGN EXAMPLE 16.4 **ELECTRONIC CURRENT SOURCE DESIGN**

Design an IC current source to meet a given set of specifications.

PROBLEM Design a 1:1 current mirror with a reference current of 25 μA and a mirror ratio error of less than 0.1 percent when the output is operating from a 20-V supply. Devices with these parameters are available: $\beta_{FO} = 100$, $V_A = 75$ V, $I_{SO} = 0.5$ fA; $K_n' = 50\ \mu A/V^2$, $V_{TN} = 0.75$ V, and $\lambda = 0.02$/V.

SOLUTION **Known Information and Given Data:** $I_{REF} = 25\ \mu A$. A mirror ratio error of less than 0.1 percent requires an output current of 25 μA ± 25 nA when the output voltage is 20 V. Either a bipolar or MOS realization is acceptable.

Unknowns: Current source configuration; transistor sizes

Approach: The specifications define the required values of R_{out} and V_{CS}. Use this information to choose a circuit topology. Complete the design by choosing device sizes based on the output resistance expressions for the selected circuit topology.

Assumptions: Room temperature operation; devices are in the active region of operation.

Analysis: The output resistance of the current source must be large enough that 20 V applied across the output does not change (increase) the current by more than 25 nA. Thus, the output resistance must satisfy $R_{out} \geq 20\ V/25\ nA = 800\ M\Omega$. Let us choose $R_{out} = 1\ G\Omega$ to provide some safety margin. The effective current source voltage is then $V_{CS} = 25\ \mu A\,(1\ G\Omega) = 25{,}000$ V! From Table 16.2 we see that either a cascode or Wilson source will be required to meet this value of V_{CS}. In fact, the source must be an MOS version, since our BJTs can at best reach $V_{CS} = 100(75\text{ V})/2 = 3750$ V.

The choice between the Wilson and cascode sources is arbitrary at this point. Let us pick the cascode source, which does not involve an internal feedback loop. In order to achieve the small mirror error, a voltage-balanced version is required. Our final circuit choice is therefore the circuit shown in Fig. 16.23(a). Now we must choose the device sizes. In this case, the W/L ratios are all the same since we require MR = 1.

Again referring to Table 16.2, the required amplification factor for the transistor is

$$\mu_f = \lambda V_{CS} = \left(\frac{0.02}{\text{V}}\right)(25{,}000\text{ V}) = 500$$

and the MOS transistor's amplification factor is given approximately by

$$\mu_f = g_m r_o \cong \sqrt{2K_n I_D}\frac{1}{\lambda I_D}$$

Using $\mu_f = 500$, $\lambda = 0.02/\text{V}$, and $I_D = 25\ \mu\text{A}$ gives a value of $K_n = 1.25$ mS. Since $K_n = K'_n(W/L)$, we need a W/L ratio of 25/1 for the given technology. (This W/L ratio is easy to achieve in integrated circuit form.) In this circuit all the transistors are operating at the same current, so that the W/L ratios should all be the same size in order to maintain the required voltage balance.

Check of Results: Let us check the calculations by directly calculating the output resistance of the source.

$$R_{\text{out}} \cong g_{m4} r_{o4} r_{o2} \qquad g_{m4} = \sqrt{2K_n I_D(1 + \lambda V_{DS4})} \qquad r_o = \frac{(1/\lambda) + V_{DS}}{I_D}$$

We can either neglect the values of V_{DS} in these expressions, or we can calculate them. In order to best compare with simulation, let us find V_{DS} and the corresponding values of g_m and r_o.

$$V_{DS2} = V_{GS2} = V_{TN} + \sqrt{\frac{2I_D}{K_n}} = 0.75 + \sqrt{\frac{50\ \mu\text{A}}{1.25\text{ mS}}} = 0.95\text{ V}$$

$$V_{DS4} = 20 - V_{DS2} = 19.0\text{ V}$$

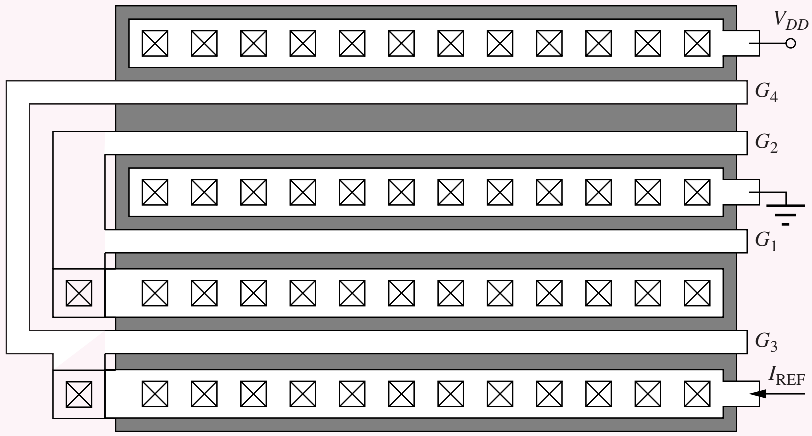
$$g_{m4} = \sqrt{2K_n I_D(1 + \lambda V_{DS4})} = \sqrt{2(1.25\text{ mA/V}^2)(25\ \mu\text{A})[1 + .02(19)]} = 0.294\text{ mS}$$

$$r_{o2} = \frac{(1/\lambda) + V_{DS2}}{I_D} = \frac{51.0\text{ V}}{25\ \mu\text{A}} = 2.04\text{ M}\Omega$$

$$r_{o4} = \frac{(1/\lambda) + V_{DS4}}{I_D} = \frac{69.0}{25\ \mu\text{A}} = 2.76\text{ M}\Omega$$

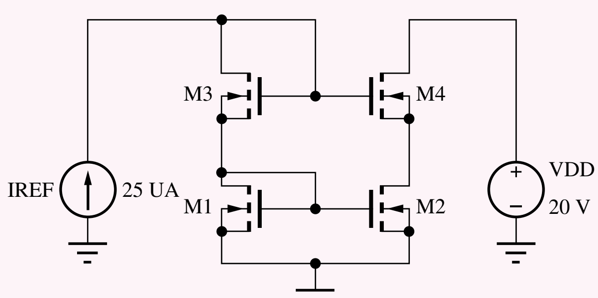
Multiplying the small-signal parameters together produces an output resistance estimate of 1.65 GΩ, which exceeds the design requirement that we originally calculated from the design specifications.

Discussion: Note that our ability to set the amplification factor of the MOS transistor was very important in achieving the design goals. In this case $\mu_{f4} = 811$. A possible layout for the cascode current source is presented in the figure. The four 25/1 NMOS transistors are stacked vertically. G_1 and G_2 are the gates of the current mirror transistors. Gates G_1 and G_3 are connected directly to their respective drains. The drain of M_1 and the source of M_3 are merged as are those of M_2 and M_4. However, there are no contacts required to the connection between the drain of M_2 and the source of M_4.



Computer-Aided Analysis: SPICE represents a good way to double check the results. First, we must set the MOS device parameters: KP = 50 μA/V^2, VTO = 0.75 V, LAMBDA = 0.02/V, W = 25 μm, and L = 1 μm. A dc simulation of the final circuit (shown next) with the given device parameters yields an output current of 25.014 μA. In addition, the voltages at the drains of M_1 and M_2 are 0.948 V and 0.976 V, respectively, indicating that the voltage balancing is working as desired.

A transfer function analysis from source V_{DD} to the output node yields an output resistance of 1.66 GΩ, easily meeting the specifications with a satisfactory safety margin. We also have good agreement with the value of R_{out} that we calculated by hand.



EXERCISE: In the SPICE results in Design Ex. 16.4, $I_O = 25.015$ μA at $V_{DD} = 20$ V. If $R_{out} = 1.66$ GΩ, what will be the output current at $V_{DD} = 10$ V?

ANSWER: 25.008 μA

EXERCISE: What is the minimum value of V_{DD} for which M_4 remains in the active region of operation?

ANSWER: 1.15 V

EXERCISE: Repeat the design in Design Ex. 16.4 for a current source with a mirror ratio of 2 ± 0.1 percent.

ANSWERS: $(W/L)_3 = (W/L)_1 = 25/1$; $(W/L)_4 = (W/L)_2 = 50/1$

16.4 REFERENCE CURRENT GENERATION

A **reference current** is required by all the current mirrors that have been discussed. The least complicated method for establishing this reference current is to use resistor R, as shown in Fig. 16.26(a).

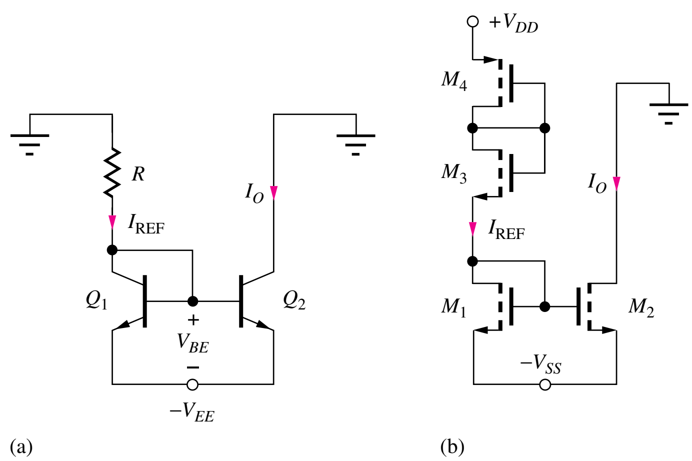


Figure 16.26 Reference current generation for current mirrors: (a) resistor reference and (b) series-connected MOSFETs.

However, the source's output current is directly proportional to the supply voltage V_{EE}:

$$I_{REF} = \frac{V_{EE} - V_{BE}}{R} \tag{16.49}$$

In MOS technology, the gate-source voltages of MOSFETs can be designed to be large, and several MOS devices can be connected in series between the power supplies to eliminate the need for large-value resistors. An example of this technique is given in Fig. 16.26(b), in which

$$V_{DD} + V_{SS} = V_{SG4} + V_{GS3} + V_{GS1}$$

and the drain currents must satisfy $I_{D1} = I_{D3} = I_{D4}$. However, any change in the supply voltages directly alters the values of the gate-source voltages of the three MOS transistors and again changes the reference current. Note that the series device technique is not usable in bipolar technology because of the small fixed voltage ($\cong 0.7$ V) developed across each diode as well as the exponential relationship between voltage and current in the diode.

EXERCISE: What is the reference current in Fig. 16.26(a) if $R = 43\ \text{k}\Omega$ and $V_{EE} = -5$ V? (b) If $V_{EE} = -7.5$ V?

ANSWERS: 100 µA; 158 µA

EXERCISE: What is the reference current in Fig. 16.26(b) if $K_n = K_p = 400\ \mu\text{A/V}^2$, $V_{TN} = -V_{TP} = 1$ V, and $V_{SS} = -5$ V? (b) If $V_{SS} = -7.5$ V?

ANSWERS: 88.9 µA; 450 µA. *Note:* the variation is worse than in the resistor bias case because of the square-law MOSFET characteristic.

16.4.1 Supply-Independent Biasing

In most cases, the supply voltage dependence of I_{REF} is undesirable. For example, we would like to fix the bias points of the devices in general-purpose op amps, even though they must operate from power supply voltages ranging from ±3 V to ±22 V. In addition, Eq. (16.47) indicates that relatively large values of resistance are required to achieve small operating currents, and these resistors use significant area in integrated circuits, as was discussed in detail in Sec. 6.6.9. Thus, a number of circuit techniques that yield currents relatively independent of the power supply voltages have been invented.

Some bipolar technologies offer the capability of fabricating *p*-channel JFETs, which can be used to set a fixed reference current, as shown in Fig. 16.27. For this circuit, the JFET is operating with $V_{SG} = 0$, and therefore $I_D = I_{DSS}$, assuming that V_{SD} is large enough to pinch off the JFET. In MOS technology, depletion-mode devices can be used in a similar manner, if available. However, because both these circuit techniques require special IC processes and therefore lack generality, other methods are preferred.

A V_{BE}-Based Reference

One possibility is the **V_{BE}-based reference,** shown in Fig. 16.28, in which the output current is determined by the base-emitter voltage of Q_1. For high current gain, the collector current of Q_1 is equal to the current through resistor R_1,

$$I_{C1} = \frac{V_{EE} - V_{BE1} - V_{BE2}}{R_1} \cong \frac{V_{EE} - 1.4\ \text{V}}{R_1} \tag{16.50}$$

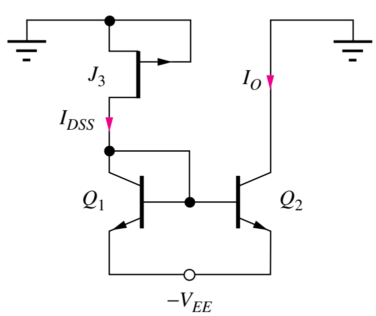


Figure 16.27 Constant reference current from a JFET.

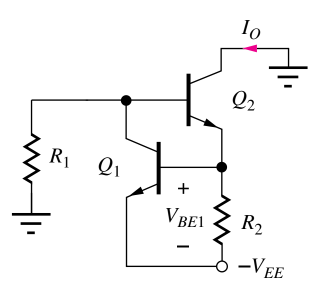


Figure 16.28 V_{BE}-based current source.

and the output current I_O is approximately equal to the current in R_2:

$$I_O = \alpha_{F2} I_{E2} = \alpha_{F2}\left(\frac{V_{BE1}}{R_2} + I_{B1}\right) \cong \frac{V_{BE1}}{R_2} \cong \frac{0.7\text{ V}}{R_2} \tag{16.51}$$

Rewriting V_{BE1} in terms of V_{EE},

$$I_O \cong \frac{V_T}{R_2} \ln \frac{V_{EE} - 1.4\text{ V}}{I_{S1} R_1} \tag{16.52}$$

A substantial degree of supply-voltage independence has been achieved because the output current is now only logarithmically dependent on changes in the supply voltage V_{EE}. However, the output current is temperature dependent due to the temperature coefficients of both V_{BE} and resistor R.

EXERCISE: (a) Calculate I_O in Fig. 16.28 for $I_S = 10^{-16}$ A, $R_1 = 39$ kΩ, $R_2 = 6.8$ kΩ, and $V_{EE} = -5$ V. Assume infinite current gains. (b) Repeat for $V_{EE} = -7.5$ V.

ANSWERS: 101 μA; 103 μA

The Widlar Source

Actually, we already discussed another source that achieves a similar independence from power supply voltage variations. The expression for the output current of the Widlar source given in Fig. 16.16 and Eq. (16.29) is

$$I_O = \alpha_F I_{E2} \cong \frac{V_T}{R} \ln\left(\frac{I_{\text{REF}}}{I_O} \frac{A_{E2}}{A_{E1}}\right) \tag{16.53}$$

Here again, the output current is only logarithmically dependent on the reference current I_{REF} (which may be proportional to V_{CC}).

Power-Supply-Independent Bias Cell

Bias circuits with an even greater degree of power supply voltage independence can be obtained by combining the Widlar source with a standard current mirror, as indicated in the circuit in Fig. 16.29. Assuming high current gain, the *pnp* current mirror forces the currents on the two

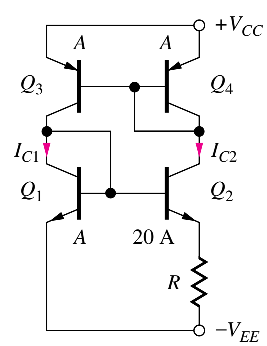


Figure 16.29 Power-supply-independent bias circuit using the Widlar source and a current mirror.

sides of the reference cell to be equal—that is, $I_{C1} = I_{C2}$. In addition, the emitter-area ratio of the Widlar source in Fig. 16.29 is equal to 20.

With these constraints, Eq. (16.53) can be satisfied by an operating point of

$$I_{C2} \cong \frac{V_T}{R}\ln(20) = \frac{0.0749\ \text{V}}{R} \tag{16.54}$$

In this example, a fixed voltage of approximately 75 mV is developed across resistor R, and this voltage is independent of the power supply voltages. Resistor R can then be chosen to yield the desired operating current.

Obviously, a wide range of mirror ratios and emitter-area ratios can be used in the design of the circuit in Fig. 16.29. Although the current, once established, is independent of supply voltage, the actual value of I_C still depends on temperature as well as the absolute value of R and varies with run-to-run process variations.

Unfortunately, $I_{C1} = I_{C2} = 0$ is also a stable operating point for the circuit in Fig. 16.29. **Start-up circuits** must be included in IC realizations of this reference to ensure that the circuit reaches the desired operating point.

Exercise: Find the output current in the current source in Fig. 16.29 if $A_{E3} = 10A_{E4}$, $A_{E2} = 10A_{E1}$, and $R = 1\ \text{k}\Omega$.

Answer: 115 μA

Exercise: What is the minimum power supply voltage for proper operation of the supply-independent bias circuit in Fig. 16.29?

Answer: $2V_{BE} \cong 1.4$ V

Once the current has been established in the reference cell consisting of Q_1–Q_4 in Fig. 16.29, the base-emitter voltages of Q_1 and Q_4 can be used as reference voltages for other current mirrors, as shown in Fig. 16.30. In this figure, buffered current mirrors have been used in the reference

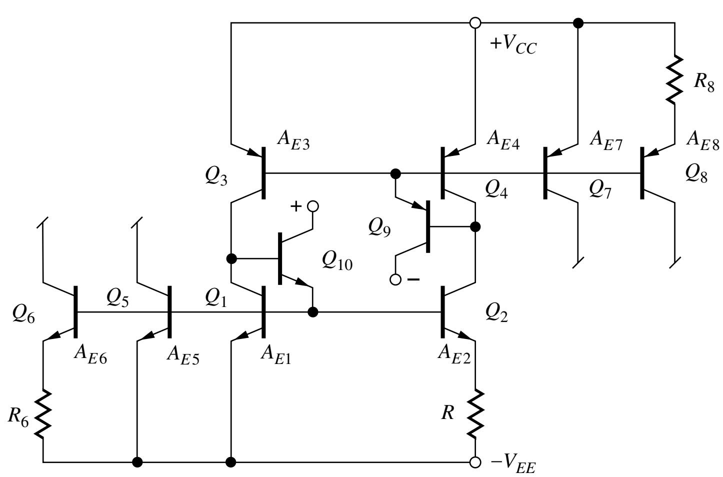


Figure 16.30 Multiple source currents generated from the supply-independent cell.

cell to minimize errors associated with finite current gains of the *npn* and *pnp* transistors. Output currents are shown generated from basic mirror transistors Q_5 and Q_7 and from Widlar sources, Q_6 and Q_8.

16.4.2 A Supply-Independent MOS Reference Cell

The MOS analog of the circuit in Fig. 16.29 appears in Fig. 16.31. In this circuit, the PMOS current mirror forces a fixed relationship between drain currents I_{D3} and I_{D4}. For the particular case in Fig. 16.31, $I_{D3} = I_{D4}$, and so $I_{D1} = I_{D2}$. Substituting this constraint into Eq. (16.35) yields an equation for the value of R required to establish a given current I_{D2}:

$$R = \sqrt{\frac{2}{K_{n1} I_{D2}}}\left(1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}}\right) \tag{16.55}$$

Based on Eq. (16.55), we see that the MOS source is independent of supply voltage but is a function of the absolute values of R and K_n'.

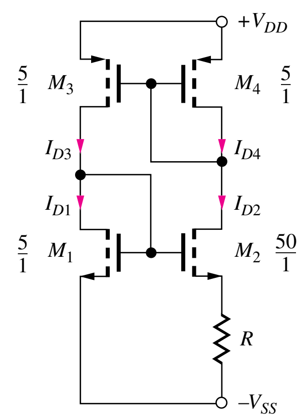


Figure 16.31 Supply-independent current source using MOS transistors.

Exercise: What value of R is required in the current source in Fig. 16.31 if I_{D2} is to be designed to be 100 μA and $K_n' = 25$ μA/V^2?

Answer: 8.65 kΩ

16.4.3 Variation of Reference Cell Current with Power Supply Variations (Advanced Topic)

Analysis of the bias circuits in this section has ignored the influence of the output resistance of the transistors, and the current is actually affected somewhat by changes in the power supply voltages. For small changes in supply voltages, the small-signal models of the circuit in Fig. 16.32(a) can be used to relate the changes in cell currents to the changes in power supply voltages. These two

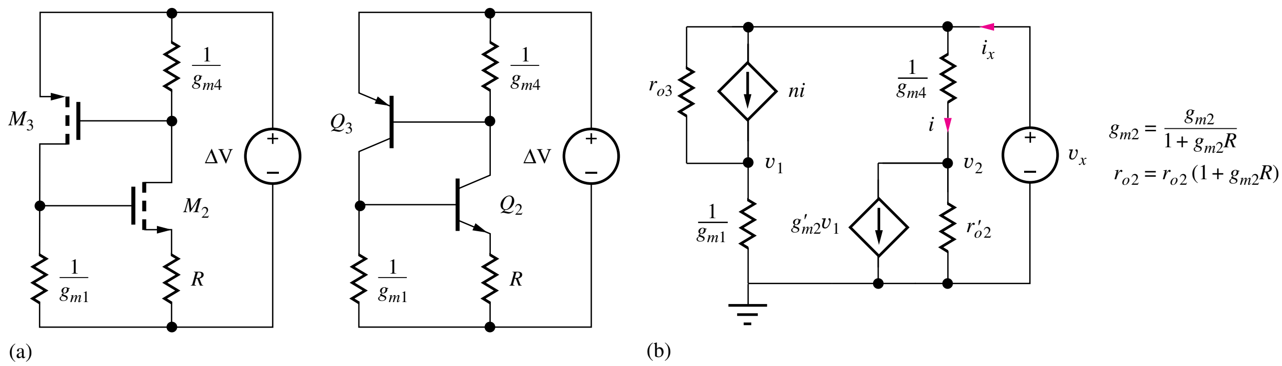


Figure 16.32 (a) Small-signal models for the reference cell current variations. (b) Simplified small-signal model.

circuits are redrawn in simplified form in Fig. 16.32(b), in which resistor R has been absorbed into the model for transistor M_2 or Q_2 (see Prob. 14.56). Source v_x represents the total change in the supply voltages

$$v_x = \Delta V_{CC} + \Delta V_{EE} \qquad \text{or} \qquad v_x = \Delta V_{DD} + \Delta V_{SS} \tag{16.56}$$

and the current i_x is expressed as

$$\mathbf{i_x} = g_{m1}\mathbf{v_1} + g'_{m2}\mathbf{v_1} + g'_{o2}\mathbf{v_2} = (g_{m1} + g'_{m2})\mathbf{v_1} + g'_{o2}\mathbf{v_2} \tag{16.57}$$

Node voltages $\mathbf{v_1}$ and $\mathbf{v_2}$ must both be found in order to determine $\mathbf{i_x}$.

Writing the nodal equations for the circuit using $\mathbf{i} = g_{m4}(\mathbf{v_x} - \mathbf{v_2})$ and collecting terms,

$$\begin{aligned}(ng_{m4} + g_{o3})\mathbf{v_x} &= (g_{m1} + g_{o3})\mathbf{v_1} + ng_{m4}\mathbf{v_2} \\ g_{m4}\mathbf{v_x} &= g'_{m2}\mathbf{v_1} + (g_{m4} + g'_{o2})\mathbf{v_2}\end{aligned} \tag{16.58}$$

Calculating the determinant of this system of equations yields

$$\Delta = g_{m1}g_{m4}\left[1 - n\frac{g'_{m2}}{g_{m1}}\right] + O\left[\frac{g_m^2}{\mu_F}\right]^3 \tag{16.59}$$

Solving Eq. (16.58) for $\mathbf{v_1}$ and $\mathbf{v_2}$ yields:

$$\begin{aligned}\mathbf{v_1} &= \left[g_{m4}(g_{o3} + ng'_{o2}) + O\left(\frac{g_m g_o}{\mu_f}\right)\right]\frac{\mathbf{v_x}}{\Delta} \\ \mathbf{v_2} &= \left[g_{m1}g_{m4}\left(1 - n\frac{g'_{m2}}{g_{m1}}\right) + O\left(\frac{g_m^2}{\mu_f}\right)\right]\frac{\mathbf{v_x}}{\Delta}\end{aligned} \tag{16.60}$$

[3] $O(x)$ = terms of the order of x.

Substituting the results from Eqs. (16.59) and (16.60) into Eq. (16.57) produces

$$\frac{\mathbf{i_x}}{\mathbf{v_x}} = \frac{g_{o3}\left(1 + \dfrac{g'_{m2}}{g_{m1}}\right) + g'_{o2}(1+n)}{1 - n\dfrac{g'_{m2}}{g_{m1}}} \tag{16.61}$$

Equation (16.61) represents the sum of two conductance terms, and therefore the output resistance can be represented as the parallel combination of two equivalent resistances:

$$R_{\text{out}} = \left(\frac{r_{o3}}{1 + \dfrac{g'_{m2}}{g_{m1}}} \,\Bigg\|\, \frac{r'_{o2}}{1+n}\right)\left(1 - n\frac{g'_{m2}}{g_{m1}}\right) \qquad \text{for } n\frac{g'_{m2}}{g_{m1}} < 1 \tag{16.62}$$

Equations (16.61) and (16.62) can be interpreted by referring to Fig. 16.32(b). In the left-hand branch of the circuit, voltage change $\mathbf{v_x}$ appears almost entirely across r_{o3}. The current in r_{o3} is amplified by the current gain of the Widlar source (g'_{m2}/g_{m1}), yielding a total current $\mathbf{i} = g_{o3}(1 + g'_{m2}/g_{m1})\mathbf{v_x}$. In the middle branch of the circuit, the voltage change appears almost entirely across r'_{o2}, and this current is amplified by the gain n of the upper current mirror, producing a total current of $\mathbf{i} = g'_{o2}(1+n)\mathbf{v_x}$.

In addition, this circuit represents a positive feedback amplifier with a loop gain $n(g'_{m2}/g_{m1})$. Because of this positive feedback, the overall output resistance is reduced by the factor $[1 - n(g'_{m2}/g_{m1})]$. Note carefully that circuit stability requires $n(g'_{m2}/g_{m1}) < 1$. Negative resistance would cause instability, and the circuit designer must be careful not to violate this condition. Further discussion of feedback circuits is postponed to Chapter 18.

EXERCISE: What is the output resistance of the source in Fig. 16.31 if $R = 8.65$ kΩ and $I_{D2} = 100$ μA? Assume $K'_n = 25$ μA/V^2, $K'_p = 10$ μA/V^2, $V_{TN} = -V_{TP} = 0.75$ V, and $1/\lambda = 80$ V.

ANSWER: 148 kΩ

EXERCISE: Simulate the circuit in Fig. 16.31 and determine I_{D2} and the output resistance of the source. (*Suggestion:* Make use of SPICE transfer function analysis.)

ANSWER: 97.8 μA, 184 kΩ

Equation (16.62) indicates that the output resistances r'_{o2} and r_{o3} of the Widlar source and current mirror determine the sensitivity to power supply variations. The supply voltage dependence can be improved by increasing these two resistance values. Figure 16.33 shows improved versions of the supply-independent reference current cells in which cascode sources have been used to improve the output resistance of the Widlar portion of the cell, and Wilson sources have been used to improve the output resistance of the current mirrors.

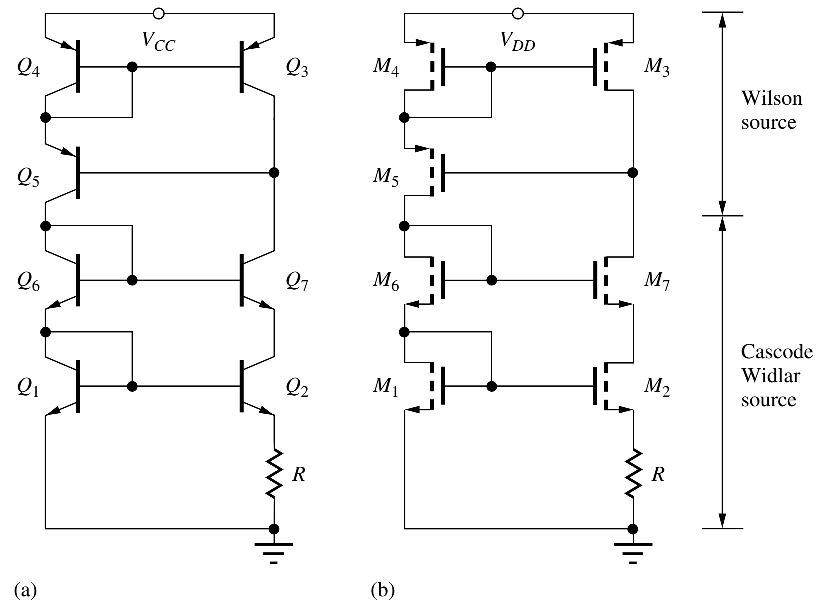


Figure 16.33 (a) Bipolar and (b) MOS reference current cells with improved power supply rejection.

DESIGN EXAMPLE 16.5 **REFERENCE CURRENT DESIGN**

Design a supply-independent current source using bipolar technology.

PROBLEM Design a supply-independent current source to provide an output current of 45 μA at $T = 300$ K using the circuit topology in Fig. 16.29 with symmetrical 5-V power supplies. The circuit should use no more than 1 kΩ of resistance or 60 μA of total current. Use SPICE to determine the sensitivity of the design current to power supply voltage variations. Assume that a unit-area BJT has the following parameters: $\beta_{FO} = 100$, $V_A = 75$ V, and $I_{SO} = 0.1$ fA for both *npn* and *pnp* transistors.

SOLUTION **Known Information and Given Data:** Circuit topology in Fig. 16.29; $\beta_{FO} = 100$, $V_A = 75$ V, $I_{SO} = 0.1$ fA. Total current ≤ 60 μA.

Unknowns: R and the area ratio between Q_1 and Q_2

Approach: The current in the circuit is described by Eq. (16.53). Use the maximum resistance values to select the area ratio. Select a current ratio in the sides of the reference to satisfy the total supply current requirement.

Assumptions: Transistors operate in the active region. $I_{C2} = 45$ μA.

Analysis: At $T = 300$ K and $V_T = 25.88$ mV, and from Eq. (16.53), we have

$$\ln\left(\frac{I_{C1}}{I_{C2}}\frac{A_{E2}}{A_{E1}}\right) = \frac{I_{C2}R}{V_T} \leq \frac{(45\ \mu\text{A})(1\ \text{k}\Omega)}{25.88\ \text{mV}} = 1.739 \qquad \text{or} \qquad \frac{I_{C1}}{I_{C2}}\frac{A_{E2}}{A_{E1}} \leq 5.69$$

In addition, the maximum current specification requires

$$\frac{I_{C2}}{I_{C1}} \geq \frac{45\ \mu\text{A}}{15\ \mu\text{A}} = \frac{3}{1}$$

Let's choose $I_{C2} = 5I_{C1}$. Then $A_{E2}/A_{E1} \leq 28.45$. Choosing $A_{E2}/A_{E1} = 20$, we obtain

$$R = \frac{25.88 \text{ mV} \ln(4)}{45 \ \mu\text{A}} = 797 \ \Omega$$

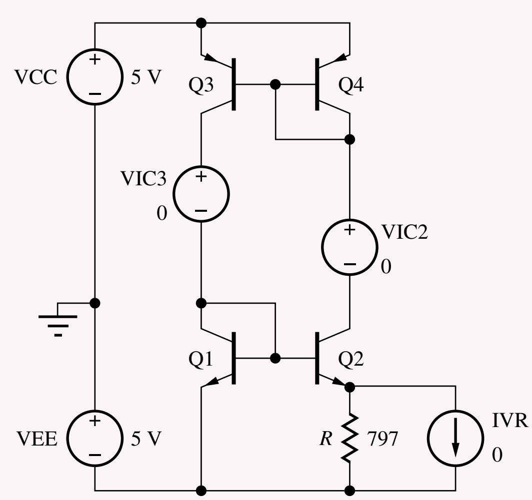
The final design is $R = 797\ \Omega$, $A_{E1} = \text{A}$, $A_{E2} = 20$ A, $A_{E3} = \text{A}$, $A_{E4} = 5$ A with 35.88 mV across resistor R.

Check of Results: Since we need to use SPICE to find the power supply sensitivity, let us use it to also check our design.

Computer-Aided Analysis: The circuit shown is drawn using the schematic editor. Zero-valued sources V_{IC2} and V_{IC3} function as ammeters to measure the collector currents of transistors Q_2 and Q_3, and I_{VR} serves as a voltmeter to measure the voltage across R. First we must remember to set the *npn* and *pnp* BJT parameters to BF = 100, VAF = 75 V, IS = 0.1 fA, and TEMP = 27 C. We must also specify AREA = 1, AREA = 20, AREA = 1 and AREA = 5 for Q_1 through Q_4, respectively. SPICE then gives $I_{C2} = 49.6\ \mu$A and $I_{C3} = 10.94\ \mu$A with 39.89 mV across R. The currents and voltage are slightly higher than predicted, and this is primarily due to having neglected the mirror ratio error due to the different values of V_{EC4} and V_{EC3}. (Try the exercise after this example.) We can correct for this error by modifying the emitter area ratio:

$$A_{E4} = 5\left(1 + \frac{V_{EC3} - V_{EC4}}{V_A}\right) = 5\left(1 + \frac{9.34 - 0.65}{75}\right) = 5.58$$

SPICE now yields $I_{C2} = 45.9\ \mu$A, $I_{C3} = 9.08\ \mu$A and $V_{E2} = 36.9$ mV. A transfer function analysis from V_{CC} to V_{IC2} gives a total output resistance of 928 kΩ for the current source, and the sensitivity of I_{C2} to changes in V_{CC} is 0.808 μA/V.



Discussion: The current source meets the specifications. If desired, the power supply sensitivity could be reduced by using the circuit in Fig. 16.33(a).

EXERCISE: Explore the errors caused by finite current gain and Early voltage by simulating the circuit with BF = 10,000 and VAF = 10,000 V. What are the new values of I_{C2}, I_{C3}, and the voltage developed across R?

ANSWERS: 45.0 μA; 9.01 μA; 35.88 mV

EXERCISE: What are the new design values if we choose $A_{E2}/A_{E1} = 25$?

ANSWERS: $R = 925\ \Omega$; $A_{E1} = A$; $A_{E2} = 25\ A$; $A_{E3} = A$; $A_{E4} = 5.57\ A$

16.5 THE BANDGAP REFERENCE

Precision **voltage references** need to not only be independent of power supply voltage, but also be independent of temperature. Although the circuits described in Sec. 16.4 can produce reference currents and voltages that are substantially independent of power supply voltage, they all still vary with temperature. Robert Widlar solved this problem with his invention of the elegant bandgap reference circuit, and today, the bandgap reference is the most common technique used to generate a precision voltage. It has supplanted Zener reference diodes in the majority of applications.

Based on his detailed understanding of bipolar transistor characteristics, Widlar realized that the negative temperature coefficient associated with the base-emitter junction could be canceled out by the positive temperature dependence of a scaled PTAT voltage as indicated conceptually in Fig. 16.34. The output voltage of the circuit in Fig. 16.34 can be written as

$$V_{BG} = V_{BE} + GV_{\text{PTAT}} \tag{16.63}$$

We desire this output voltage to have a zero temperature coefficient:

$$\frac{\partial V_{BG}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + G\frac{\partial V_{\text{PTAT}}}{\partial T} = 0 \tag{16.64}$$

The dependence of V_{BE} and V_{PTAT} on temperature were developed previously in Eqs. (3.15) and (16.33), respectively. Substituting these values into Eq. (16.64) gives

$$\frac{\partial V_{BG}}{\partial T} = \frac{V_{BE} - V_{GO} - 3V_T}{T} + G\frac{V_{\text{PTAT}}}{T} = 0$$

or (16.65)

$$GV_{\text{PTAT}} = V_{GO} + 3V_T - V_{BE}$$

where V_{GO} is the silicon bandgap voltage at 0 K (1.12 V). Substituting this result into Eq. (16.65) reduces the output voltage to

$$V_{BG} = V_{GO} + 3V_T \tag{16.66}$$

The output voltage at which zero temperature coefficient is achieved is slightly above the bandgap voltage of silicon. Hence, this circuit is referred to as a "bandgap reference." At room temperature, the output voltage is approximately 1.20 V.

A circuit realization of the bandgap reference is shown in Fig. 16.35. This circuit is attributed to another talented designer, Paul Brokaw of Analog Devices [5], and is easier to understand

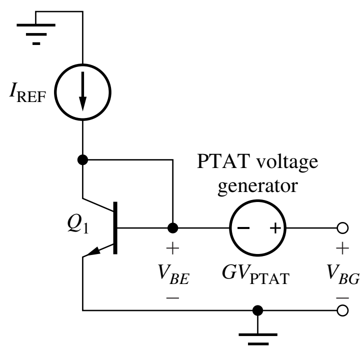


Figure 16.34 Concept for the bandgap reference.

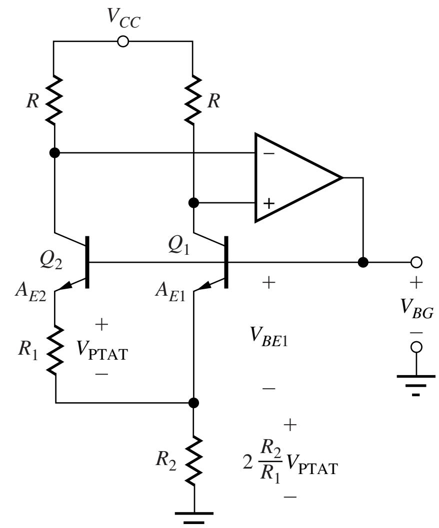


Figure 16.35 Brokaw version of the bandgap reference.

than the original circuit of Widlar. In this circuit, the output voltage is equal to the sum of the base-emitter voltage of Q_1 plus the voltage across resistor R_2, which is a scaled replica of the PTAT voltage being developed across resistor R_1. The scaling factor is controlled by the op amp and resistors R.

The ideal op amp forces the voltage across the two matched collector resistors to be the same, thereby setting $I_{C2} = I_{C1}$ and $I_{E2} = I_{E1}$. Thus the PTAT voltage is equal to $V_T \ln(A_{E2}/A_{E1})$, and the emitter current of Q_2 equals V_{PTAT}/R_1. The current in R_2 is twice that in R_1, since $I_{E2} = I_{E1}$. Combining these results yields an expression for the output voltage V_{BG}:

$$V_{BG} = V_{BE1} + 2\frac{R_2}{R_1}V_T \ln \frac{A_{E2}}{A_{E1}} \tag{16.67}$$

For this circuit, the gain $G = 2R_2/R_1$, and based on Eq. (16.65), the resistor ratio is given by

$$\frac{R_2}{R_1} = -\frac{1}{2}\frac{\dfrac{\partial V_{BE1}}{\partial T}}{\dfrac{\partial V_{PTAT}}{\partial T}} = \frac{V_{GO} + 3V_T - V_{BE1}}{2V_{PTAT}} \tag{16.68}$$

Often we want an output voltage that is not equal to 1.2 V, and other voltages are easy to achieve by adding a two-resistor voltage divider to the Brokaw circuit as in Fig. 16.36. In this case the op amp output voltage becomes

$$V_O = \left(1 + \frac{R_4}{R_3}\right) V_{BG} \tag{16.69}$$

which can be scaled up to any desired value (e.g., 2.5 or 5 V).

A word of caution is needed here. In most bandgap reference designs, zero-output voltage is a valid operating point, and some additional circuitry must be added to ensure that the circuit “starts up” and reaches the desired operating point. In many simple circuit cases, SPICE will have considerable difficulty converging to the desired operating point.

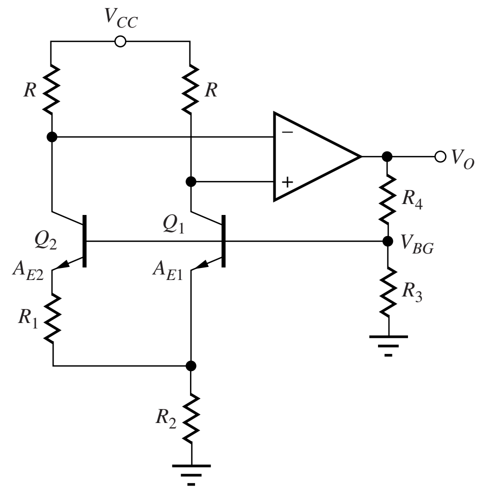


Figure 16.36 Bandgap reference with $V_O > V_{BG}$.

EXAMPLE 16.6 BANDGAP REFERENCE ANALYSIS

In this example, we determine the operating point for a specific bandgap reference circuit.

PROBLEM Find I_C, V_{PTAT}, V_{BE}, and V_{BG} for the circuit in Fig. 16.35 if $R = 30$ kΩ, $R_1 = 1$ kΩ, and $R_2 = 4.16$ kΩ. Assume $I_S = 0.1$ fA and $A_{E2} = 10A_{E2}$.

SOLUTION **Known Information and Given Data:** The circuit is the Brokaw reference in Fig. 16.35 with $R = 30$ kΩ, $R_1 = 1$ kΩ, and $R_2 = 4.16$ kΩ. Transistor parameters are specified as $I_S = 0.1$ fA and $A_{E2} = 10A_{E2}$.

Unknowns: I_C, V_{PTAT}, V_{BE}, and V_{BG}

Approach: Find V_T and V_{PTAT} which determine I_C. Use I_C to find V_{BE1}. Use V_{BE1} and V_{PTAT} to find the output voltage.

Assumptions: $T = 300$ K; BJTs are in the active region of operation; the current gain is large, say $\beta_{FO} = 10{,}000$ and $V_A = \infty$.

Analysis: Because of the precision involved, we should carry more digits in our calculations than normal. Following the sequence of calculations outlined earlier,

$$V_T = \frac{kT}{q} = \frac{1.380 \times 10^{-23}(300)}{1.602 \times 10^{-19}} = 25.84 \text{ mV}$$

$$V_{\text{PTAT}} = V_T \ln\left(\frac{A_{E2}}{A_{E1}}\right) = V_T \ln(10) = 59.50 \text{ mV}$$

$$I_C = I_E = \frac{V_{\text{PTAT}}}{R_1} = 59.50\ \mu\text{A}$$

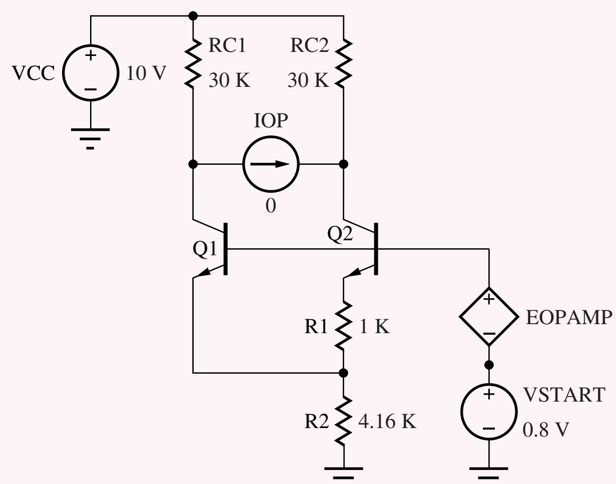
$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) = (25.84 \text{ mV}) \ln\left(\frac{59.50\ \mu\text{A}}{0.1 \text{ fA}}\right) = 0.7006 \text{ V}$$

$$V_{BG} = V_{BE1} + 2\frac{R_2}{R_1}V_{\text{PTAT}} = 0.7006 + 2\frac{4.16 \text{ k}\Omega}{1 \text{ k}\Omega}(59.50 \text{ mV}) = 1.196 \text{ V}$$

Check of Results: V_{BG} is approximately 1.20 V so our calculation appears correct. Our analysis showed that the output voltage should also be $V_{GO} + 3V_T = 1.198$ V, which also checks.

Discussion: Note that the voltage drop across the collector resistors must be enough to bring the inputs of the op amp into its common-mode operating range. In this circuit, the drop across the collector resistors is only 1.5 V.

Computer-Aided Analysis: We first set the *npn* parameters to BF = 10,000, IS = 0.1 fA, and let VAF default to infinity. Set AREA = 1 for Q_1 and AREA = 10 for Q_2. In the circuit shown here, the ideal op amp is modeled by EOPAMP, whose controlling voltage appears across zero-value current source IOP. The gain is set to 10^6. Source VSTART may be needed in certain versions of SPICE to help the circuit start up. (Remember that $V_O = 0$ is a valid operating point.) Sweeping VCC from 0 to 10 V can also help the startup problem. SPICE simulation produces $V_{BG} = 1.197$ V and $V_{\text{PTAT}} = 59.55$ mV for the default temperature of 27°C.



EXERCISE: Suppose $\beta_{FO} = 100$ and $V_A = 75$. Use SPICE to find the new output voltage of the bandgap reference in Ex. 16.6?

ANSWER: 1.194 V

DESIGN EXAMPLE 16.7

BANDGAP REFERENCE DESIGN

Design of the bandgap reference requires a slightly different sequence of calculations than the analysis in the previous example.

PROBLEM Design the bandgap reference in Fig. 16.36 to produce an output voltage of 5.000 V with zero temperature coefficient at a temperature of 47°C. Design for a collector current of 25 μA, and assume $I_S = 0.5$ fA.

SOLUTION **Known Information and Given Data:** The circuit is the Brokaw reference with amplified output given in Fig. 16.36. $V_O = 5.000$ V with a zero temperature coefficient (TC) at $T = 320$ K. Collector currents are to be 25 μA, and the transistor saturation current is 0.5 fA.

Unknowns: Values of resistors R, R_1, R_2, R_3, and R_4

Approach: Find V_T and V_{PTAT}. Then use I_C to determine R_1. Use I_C to find V_{BE1}. Determine R_2 using Eq. (16.68). Choose R_4 and R_3 to set $V_O = 5$ V. Choose R to provide operating voltage to the op amp.

Assumptions: BJTs are in the active region of operation. $\beta_{FO} = \infty$ and $V_A = \infty$. $A_{E2} = 10A_{E1}$ represents a reasonable emitter area ratio. Drop 2 V across R.

Analysis: Because of the precision involved, we will carry four digits in our calculations.

$$V_T = \frac{kT}{q} = \frac{1.380 \times 10^{-23}(320)}{1.602 \times 10^{-19}} = 27.57 \text{ mV}$$

$$V_{PTAT} = V_T \ln\left(\frac{A_{E2}}{A_{E1}}\right) = V_T \ln(10) = 63.47 \text{ mV}$$

$$R_1 = \frac{V_{PTAT}}{I_E} = \frac{63.47 \text{ mV}}{25 \text{ μA}} = 2.539 \text{ kΩ}$$

$$V_{BE1} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right) = (27.57 \text{ mV}) \ln\left(\frac{25 \text{ μA}}{0.5 \text{ fA}}\right) = 0.6792 \text{ V}$$

$$\frac{R_2}{R_1} = \frac{V_{GO} + 3V_T - V_{BE1}}{2V_{PTAT}} = \frac{1.12 + 3(0.02757) - 0.6792}{2(0.06347)} = 4.124$$

$$R_2 = 4.124R_1 = 10.47 \text{ kΩ}$$

$$V_{BG} = V_{BE1} + 2\frac{R_2}{R_1}V_{PTAT} = 0.6792 + 2(4.124)(63.47 \text{ mV}) = 1.203 \text{ V}$$

$$\frac{R_4}{R_3} = \frac{V_O}{V_{BG}} - 1 = 3.157$$

We should not waste an excessive amount of current in the output voltage divider, so let us choose $I_3 = I_4 = 50$ μA. Also, set the voltage drop across R to 2 V.

$$R_3 = \frac{V_{BG}}{I_3} = \frac{1.203 \text{ V}}{50 \text{ μA}} = 24.0 \text{ kΩ} \qquad \text{and} \qquad R_4 = \frac{V_O - V_{BG}}{I_3} = \frac{3.797 \text{ V}}{50 \text{ μA}} = 75.9 \text{ kΩ}$$

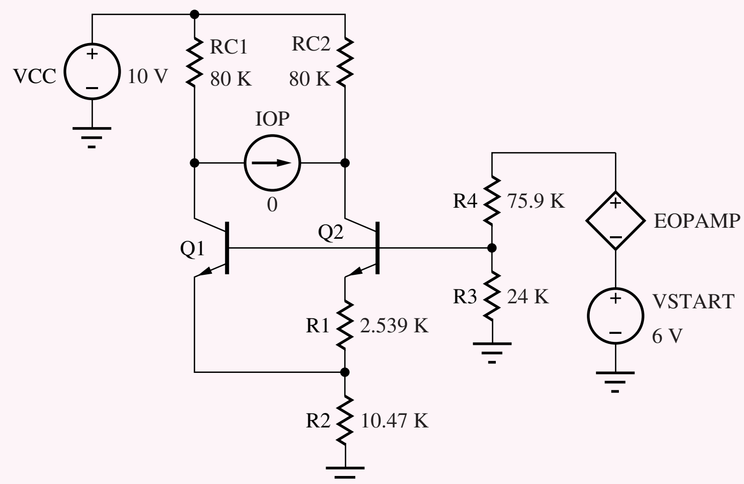
$$R = \frac{2 \text{ V}}{25 \text{ μA}} = 80 \text{ kΩ}$$

Check of Results: V_{BG} is approximately 1.20 V so our calculation appears correct. Our analysis showed that the output voltage should also be $V_{GO} + 3V_T = 1.203$ V, which also checks.

Discussion: Note that the voltage drop across the collector resistors must be enough to bring the inputs of the op amp into its common-mode operating range. In this circuit, the drop across the collector resistors is designed to be 2 V.

Computer-Aided Analysis: We first set the *npn* parameters to BF = 10,000 and IS = 0.5 fA and let VAF default to infinity. Set AREA = 1 for Q_1, AREA = 10 for Q_2, and TEMP = 47°C.

In the circuit shown here, the ideal op amp is modeled by EOPAMP whose controlling voltage appears across zero-value current source IOP. The gain is set to 10^6. Source VSTART may be needed in some versions of SPICE to help the circuit start up. Another help is to sweep VCC from 0 to 10 V. (Remember that $V_O = 0$ is a valid operating point.) SPICE simulation produces $V_{BG} = 1.204$ V and $V_{\text{PTAT}} = 63.52$ mV and $V_O = 5.01$ V. With BF = 100 and VAF = 75 V, the values are $V_{BG} = 1.201$ V and $V_{\text{PTAT}} = 63.52$ mV and $V_O = 5.03$ V.



EXERCISE: Redesign the reference in Ex. 16.7 using $A_{E2} = 20A_{E1}$.

ANSWER: 3.17 kΩ, 10.5 kΩ, 24.0 kΩ, 75.9 kΩ, 80 kΩ

16.6 THE CURRENT MIRROR AS AN ACTIVE LOAD

One of the most important applications of the current mirror[4] is as a replacement for the load resistors of differential amplifier stages in IC operational amplifiers. This elegant application of the current mirror can greatly improve amplifier voltage gain while maintaining the operating-point balance necessary for good common-mode rejection and low offset voltage. When used in this manner, the current mirror is referred to as an **active load** because the passive load resistors have been replaced with active transistor circuit elements.

16.6.1 CMOS DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

Figure 16.37 shows a CMOS differential amplifier with an active load; the load resistors have been replaced by a PMOS current mirror. Let us first study the quiescent operating point of this circuit and then look at its small-signal characteristics.

[4] In addition to its role as a current source.

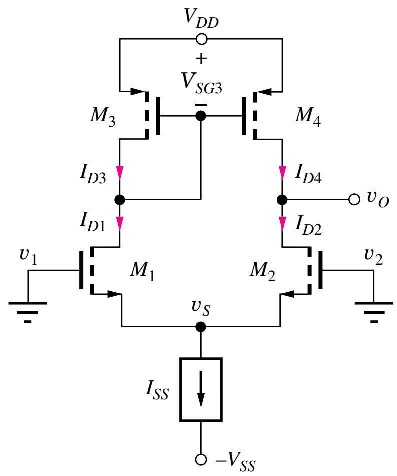


Figure 16.37 CMOS differential amplifier with PMOS active load.

dc Analysis

Assume for the moment that the amplifier is voltage balanced (in fact, it will turn out that it *is* balanced). Then bias current I_{SS} divides equally between transistors M_1 and M_2, and I_{D1} and I_{D2} are each equal to $I_{SS}/2$. Current I_{D3} must equal I_{D1} and is mirrored as I_{D4} at the output of the PMOS current mirror. Thus, I_{D3} and I_{D4} are also equal to $I_{SS}/2$, and the current in the drain of M_4 is exactly the current required to satisfy M_2.

The mirror ratio set by M_3 and M_4 is exactly unity when $V_{SD4} = V_{SD3}$ and hence $V_{DS1} = V_{DS2}$. Thus, the differential amplifier is completely balanced at dc when the quiescent output voltage is

$$V_O = V_{DD} - V_{SD4} = V_{DD} - V_{SG3} = V_{DD} - \left(\sqrt{\frac{I_{SS}}{K_p}} - V_{TP}\right) \tag{16.70}$$

Q-Points

The drain-source voltages of M_1 and M_2 are

$$V_{DS1} = V_O - V_S = V_{DD} - \left(\sqrt{\frac{I_{SS}}{K_p}} - V_{TP}\right) + \left(V_{TN} + \sqrt{\frac{I_{SS}}{K_n}}\right)$$

or

$$V_{DS1} = V_{DD} + V_{TN} + V_{TP} + \sqrt{\frac{I_{SS}}{K_n}} - \sqrt{\frac{I_{SS}}{K_p}} \cong V_{DD} \tag{16.71}$$

and those of M_3 and M_4 are

$$V_{SD3} = V_{SG3} = \sqrt{\frac{I_{SS}}{K_p}} - V_{TP} \tag{16.72}$$

(Remember that $V_{TP} < 0$ for *p*-channel enhancement-mode devices.)

The drain currents of all the transistors are equal:

$$I_{DS1} = I_{DS2} = I_{SD3} = I_{SD4} = \frac{I_{SS}}{2} \tag{16.73}$$

Small-Signal Analysis

Now that we have found the operating points of the transistors, we can proceed to analyze the small-signal characteristics of the amplifier including differential-mode gain, differential-mode input and output resistances, common-mode gain, CMRR, and common-mode input and output resistances.

Differential-Mode Signal Analysis

Analysis of the ac behavior of the differential amplifier begins with the differential-mode input applied in the ac circuit model in Fig. 16.38. Upon studying the circuit in Fig. 16.38, we realize that it is a two terminal network and can be represented by its Norton equivalent circuit consisting of the short-circuit output current and Thévenin equivalent output resistance. With the output terminals short circuited, the NMOS differential pair produces equal and opposite currents with amplitude $g_{m2}v_{id}/2$ at the drains of M_1 and M_2. Drain current i_{d1} is supplied by current mirror transistor M_3 and is replicated at the output of M_4. Thus the total short circuit output current is

$$\mathbf{i_o} = 2\frac{g_{m2}\mathbf{v_{id}}}{2} = g_{m2}\mathbf{v_{id}} \tag{16.74}$$

The current mirror provides a single-ended output but with a transconductance equal to the full value of the C-S amplifier.

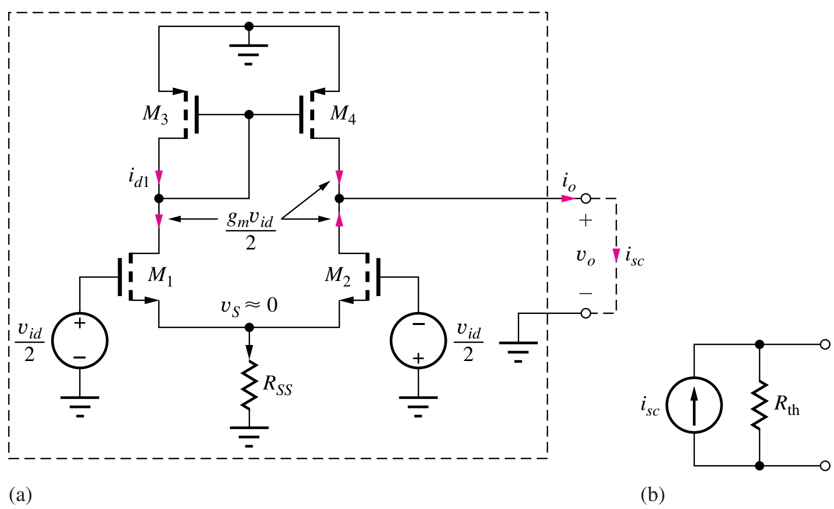


Figure 16.38 (a) CMOS differential amplifier with differential-mode input. (b) The circuit is a one port and can be represented by its Norton equivalent circuit.

The Thévenin equivalent output resistance will be found using the circuit in Fig. 16.39 in which the internal output resistances of M_2 and M_4 are shown next to their respective transistors. In the next section we will show that R_{th} is equal to the parallel combination of r_{o2} and r_{o4}:

$$R_{th} = r_{o2} \| r_{o4} \tag{16.75}$$

The differential-mode voltage gain of the open-circuited differential amplifier is simply the product of i_{sc} and R_{th}:

$$A_{dm} = g_{m2}(r_{o2} \| r_{o4}) = \frac{\mu_{f2}}{1 + \frac{r_{o2}}{r_{o4}}} \cong \frac{\mu_{f2}}{2} \tag{16.76}$$

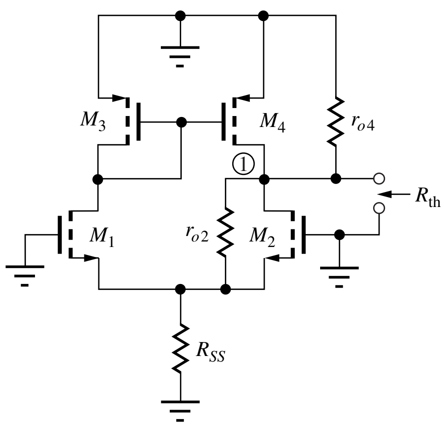


Figure 16.39 Simple CMOS op amp with active load in the first stage.

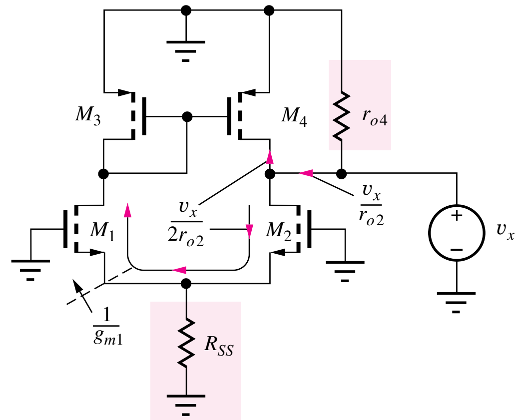


Figure 16.40 Output resistance component due to r_{o2}.

Equation (16.76) indicates that the gain of the input stage of the amplifier approaches one-half the amplification factor of the transistors forming the differential pair. We are now within a factor of 2 of the theoretical voltage gain limit for a single-transistor amplifier!

Output Resistance of the Differential Amplifier

The origin of the output resistance expression in Eq. (16.75) can be thought of conceptually in the following (although technically incorrect) manner. At node 1 in Fig. 16.39, r_{o4} is connected directly to ac ground at the positive power supply, whereas r_{o2} appears connected to virtual ground at the sources of M_2 and M_1. Thus r_{o2} and r_{o4} are effectively in parallel. Although this argument gives the correct answer, it is not precisely correct. Because the differential amplifier with active load no longer represents a symmetric circuit, the node at the sources of M_1 and M_2 *is not* truly a virtual ground.

Exact Analysis

A more precise analysis can be obtained from the circuit in Fig. 16.40. The output resistance r_{o4} of M_4 is indeed connected directly to ac ground and represents one component of the output resistance. However, the current from v_x due to r_{o2} is more complicated. The actual behavior can be determined from Fig. 16.40, in which R_{SS} is assumed to be negligible with respect to $1/g_{m1}$, $R_{SS} \gg 1/g_{m1}$.

Transistor M_2 is operating as a common-gate transistor with an effective resistance in its source of $R_S = 1/g_{m1}$. Based on the results in Table 14.1, the resistance looking into the drain of M_2 is

$$R_{o2} = r_{o2}(1 + g_{m2}R_S) = r_{o2}\left(1 + g_{m2}\frac{1}{g_{m1}}\right) = 2r_{o2} \tag{16.77}$$

Therefore, the drain current of M_2 is equal to $\mathbf{v_x}/2r_{o2}$. However, the current goes around the differential pair and into the input of the current mirror at M_3. The current is replicated by the mirror to become the drain current of M_4. The total current from source v_x becomes $2(\mathbf{v_x}/2r_{o2}) = \mathbf{v_x}/r_{o2}$.

Combining this current with the current through r_{o4} yields a total current of

$$\mathbf{i_x^T} = \frac{\mathbf{v_x}}{r_{o2}} + \frac{\mathbf{v_x}}{r_{o4}} \qquad \text{and} \qquad R_{od} = r_{o2} \| r_{o4} \tag{16.78}$$

The equivalent resistance at the output node is, in fact, exactly equal to the parallel combination of the output resistances of M_2 and M_4.

EXERCISE: Find the Q-points of the transistors in Fig. 16.34 if $I_{SS} = 250\ \mu A$, $K_n = 250\ \mu A/V^2$, $K_p = 200\ \mu A/V^2$, $V_{TN} = -V_{TP} = 0.75$ V, and $V_{DD} = V_{SS} = 5$ V. What are the transconductance, output resistance, and voltage gain of the amplifier if $\lambda = 0.0133\ V^{-1}$?

ANSWERS: (125 μA, 4.88 V), (125 μA, 1.87 V); 250 μS, 314 kΩ, 78.5

Common-Mode Input Signals

Figure 16.41 is the CMOS differential amplifier with a common-mode input signal. The common-mode input voltage causes a common-mode current i_{oc} in both sides of the differential pair consisting of M_1 and M_2. The common-mode current (i_{oc}) in M_1 is mirrored at the output of M_4 with a small error since no current can appear in r_{o4} with the output shorted. In addition, the small voltage difference developed between the drains of M_1 and M_2 causes a current in the differential output resistance ($2r_{o2}$) of the pair that is then doubled by the action of the current mirror.

An expression for the short-circuit output current can be found using the small-signal model for the circuit in Fig. 16.41(b). The differential pair with common-mode input is represented by the two-port model from Sec. 15.3.15 with

$$i_{oc} \cong \frac{v_{ic}}{2R_{SS}} \qquad R_{od} = 2r_{o2} \qquad R_{oc} = 2\mu_f R_{SS} \tag{16.79}$$

With the output short-circuited, we have a one-node problem. Solving for v_3,

$$v_3 = \frac{-i_{oc}}{g_{m3} + g_{o3} + \dfrac{g_{o2}}{2} + G_{oc}} \qquad \text{and} \qquad i_{sc} = -\left(i_{oc} + g_{m4}v_3 - \frac{g_{o2}}{2}v_3\right) \tag{16.80}$$

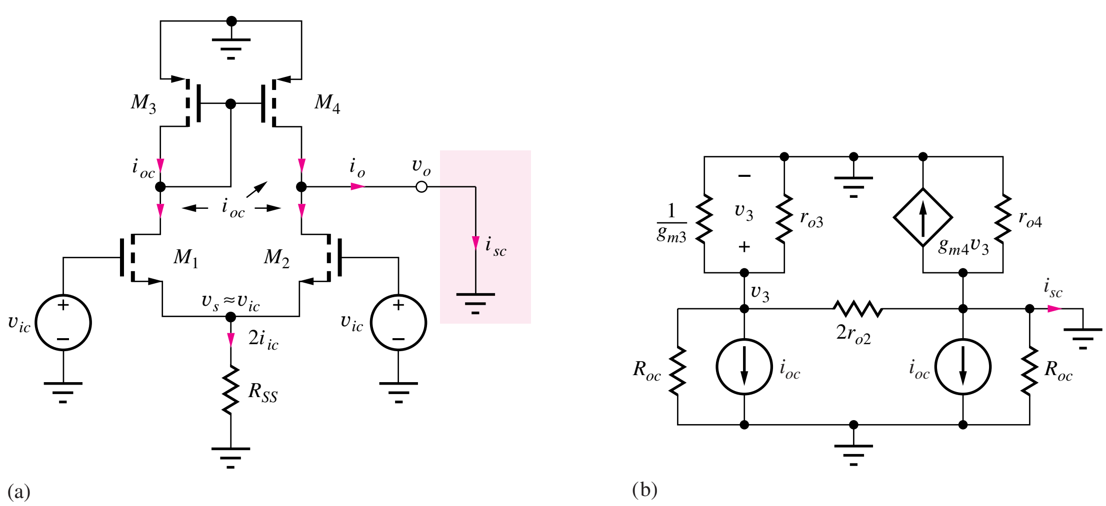


Figure 16.41 CMOS differential amplifier with common-mode input.

which together with Eq. (16.79) yield

$$i_{sc} = -\frac{g_{o3} + g_{o2}}{g_{m3} + g_{o3} + \dfrac{g_{o2}}{2} + G_{oc}} i_{oc} \cong -\frac{1 + \dfrac{r_{o3}}{r_{o2}}}{\mu_{f3}} \left(\frac{v_{ic}}{2R_{SS}}\right) \tag{16.81}$$

where it is assumed that $g_{m4} = g_{m3}$ and $G_{oc} \ll g_{m3}$. The Thévenin equivalent output resistance is exactly the same as found in the previous section, $R_{\text{th}} = r_{o2} \| r_{o4}$. Thus the common-mode gain is

$$A_{cm} = \frac{i_{sc} R_{\text{th}}}{v_{ic}} = -\frac{\left(1 + \dfrac{r_{o3}}{r_{o2}}\right)}{2\mu_{f3} R_{SS}} (r_{o2} \| r_{o4}) \tag{16.82}$$

where $\mu_{f3} \gg 1$ has been assumed. The common-mode rejection ratio is

$$\text{CMRR} = \left|\frac{A_{dm}}{A_{cm}}\right| = \frac{2\mu_{f3} g_{m2} R_{SS}}{\left(1 + \dfrac{r_{o3}}{r_{o2}}\right)} \cong \mu_{f3} g_{m2} R_{SS} \quad \text{for} \quad r_{o3} \cong r_{o2} \tag{16.83}$$

which is improved by a factor of approximately μ_{f3} over that of the pair with a resistor load!

EXERCISE: Evaluate Eq. (16.83) for $K_p = K_n = 5$ mA/V^2, $\lambda = 0.0167$ V^{-1}, $I_{SS} = 200$ μA, and $R_{SS} = 10$ MΩ.

ANSWER: 6.00×10^6 or 136 dB

In the last exercise, we find that the CMRR predicted by Eq. (16.83) is quite large, whereas typical op amp specs are 80 to 100 dB. We need to look deeper. In reality, this level will not be achieved, but will be limited by mismatches between the devices in the circuit.

Mismatch Contributions to CMRR Analysis

In this section we explore the techniques used to calculate the effects of device mismatches on CMRR. Figure 16.42 presents the small-signal model for the differential amplifier with mismatches in transistors M_1 and M_2 in which we assume

$$g_{m1} = g_m + \frac{\Delta g_m}{2} \qquad g_{m2} = g_m - \frac{\Delta g_m}{2} \qquad g_{o1} = g_o + \frac{\Delta g_o}{2} \qquad g_{o2} = g_o - \frac{\Delta g_o}{2} \tag{16.84}$$

In this analysis, M_3 and M_4 are still identical. We desire to find the short circuit output current $i_{sc} = (i_{d1} - i_{d2})$ in which i_{d1} is replicated by the current mirror. Let us use our knowledge of the gross behavior of the circuit to simplify the analysis. We have $v_{d2} = 0$, since we are finding the short-circuit output current, and based on previous common-mode analyses, we expect the signal at v_{d1} to be small. So let us assume that $v_{d1} \cong 0$. With this assumption, and noting that the two gate-source voltages are identical,

$$i_{sc} = i_{d1} - i_{d2} = (g_{m1} - g_{m2})v_{gs} - (g_{o1} - g_{o2})v_s = \Delta g_m v_{gs} - \Delta g_o v_s \tag{16.85}$$

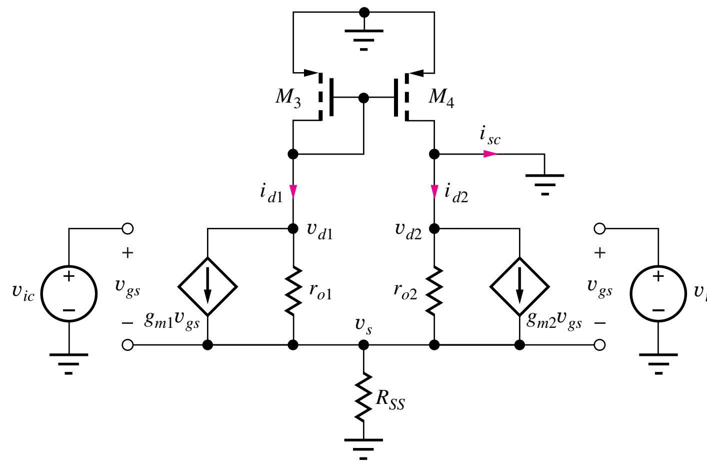


Figure 16.42 CMOS differential amplifier in which M_1 and M_2 are no longer matched.

To evaluate this expression, we need to find source voltage v_s and gate-source voltage v_{gs}. Writing a nodal equation for v_s with $v_{gs} = v_{ic} - v_s$, $v_{d1} = 0$ and $v_{d2} = 0$, yields

$$\left(g_m + \frac{\Delta g_m}{2} + g_m - \frac{\Delta g_m}{2}\right)(v_{ic} - v_s) = \left(g_o + \frac{\Delta g_o}{2} + g_o - \frac{\Delta g_o}{2} + G_{SS}\right) v_s$$

in which we may be surprised to see all the mismatch terms cancel out! Thus, for common-mode inputs, v_s and v_{gs} are not affected by the transistor mismatches[5]:

$$v_s \cong \frac{2g_m R_{SS}}{1 + 2g_m R_{SS}} v_{ic} \cong v_{ic} \qquad \text{and} \qquad v_{gs} \cong \frac{1 + 2g_o R_{SS}}{1 + 2g_m R_{SS}} v_{ic} \cong \left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right) v_{ic} \tag{16.86}$$

The short-circuit output current goes through the Thévenin output resistance $R_{\text{th}} = r_{o2} \| r_{o4}$ to produce the output voltage, and

$$A_{cm} = \frac{i_{sc} R_{\text{th}}}{v_{ic}} = \left[\Delta g_m \left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right) - \Delta g_o\right] (r_{o2} \| r_{o4}) \tag{16.87}$$

The CMRR is then

$$\text{CMRR}^{-1} = \left|\frac{A_{cm}}{A_{dm}}\right| = \left|\frac{A_{cm}}{g_m (r_{o2} \| r_{o4})}\right| = \left[\frac{\Delta g_m}{g_m}\left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right) - \frac{\Delta g_o}{g_o}\frac{1}{\mu_f}\right] \tag{16.88}$$

For very large R_{SS}, we see that CMRR is now limited by the transistor mismatches and value of the amplification factor. For example, a 1 percent mismatch with an amplification factor of 500 limits the individual terms in Eq. (16.88) to 2×10^{-5}. Since we cannot predict the signs on the $\Delta g/g$ terms, the expected CMRR is 2.5×10^4 or 88 dB. This is much more consistent with observed values of CMRR.

[5] An exact analysis without assuming that $v_{d1} = 0$ shows that a negligibly small change actually occurs.

16.6.2 Bipolar Differential Amplifier with Active Load

The bipolar differential amplifier with an active load formed from a *pnp* current mirror is depicted in Fig. 16.43 with $v_1 = 0 = v_2$. If we assume that the circuit is balanced with $\beta_{FO} = \infty$, then the bias current I_{EE} divides equally between transistors Q_1 and Q_2, and I_{C1} and I_{C2} are equal to $I_{EE}/2$. Current I_{C1} is supplied by transistor Q_3 and is mirrored as I_{C4} at the output of *pnp* transistor Q_4. Thus, I_{C3} and I_{C4} are both also equal to $I_{EE}/2$, and the dc current in the collector of Q_4 is exactly the current required to satisfy Q_2.

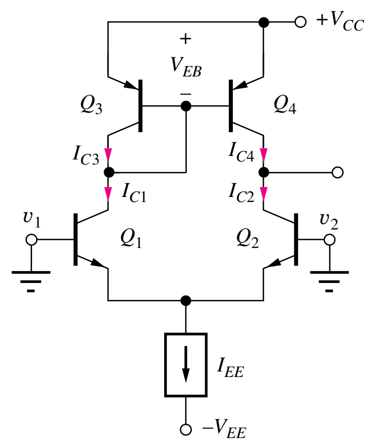


Figure 16.43 Bipolar differential amplifier with active load.

If β_{FO} is very large, then the current mirror ratio is exactly 1 when $V_{EC4} = V_{EC3} = V_{EB}$, and the differential amplifier is completely balanced when the quiescent output voltage is

$$V_O = V_{CC} - V_{EB} \tag{16.89}$$

Q-Points

The collector currents of all the transistors are equal:

$$I_{C1} = I_{C2} = I_{C3} = I_{C4} = \frac{I_{EE}}{2} \tag{16.90}$$

The collector-emitter voltages of Q_1 and Q_2 are

$$V_{CE1} = V_{CE2} = V_C - V_E = (V_{CC} - V_{EB}) - (-V_{BE}) \cong V_{CC} \tag{16.91}$$

and for Q_3 and Q_4,

$$V_{EC3} = V_{EC4} = V_{EB} \tag{16.92}$$

Finite Current Gain

The current gain defect in the current mirror upsets the dc balance of the circuit. However, as long as the transistors remain in the forward-active region, the collector current of Q_4 must equal the collector current of Q_2, and the collector-emitter voltage of Q_4 adjusts itself to make up for the current-gain defect of the current mirror. The required value of V_{EC4} can be found using the current mirror expression from Eq. (16.10):

$$I_{C4} = I_{C1} \frac{\left[1 + \dfrac{V_{EC4}}{V_A}\right]}{\left[1 + \dfrac{V_{EB}}{V_A} + \dfrac{2}{\beta_{FO4}}\right]} \tag{16.93}$$

However, because $I_{C4} = I_{C2}$ and $I_{C2} = I_{C1}$, the mirror ratio must be unity, which requires

$$V_{EC4} = V_{EB} + \frac{2V_A}{\beta_{FO4}} \tag{16.94}$$

For $\beta_{FO3} = 50$, $V_A = 60$ V, and $V_{EB} = 0.7$ V, $V_{EC4} = 3.10$ V.

This collector-emitter voltage difference represents a substantial offset at the amplifier output and translates to an equivalent input offset voltage of

$$V_{OS} = \frac{V_{EC4} - V_{EC3}}{A_{dd}} = \frac{V_{EC4} - V_{EB}}{A_{dd}} \tag{16.95}$$

V_{OS} represents the input voltage needed to force the output voltage differential to be zero. For $A_{dd} = 100$, V_{OS} would be 24.0 mV. To eliminate this error, a buffered current mirror is usually used as the active load, as shown in Fig. 16.44.

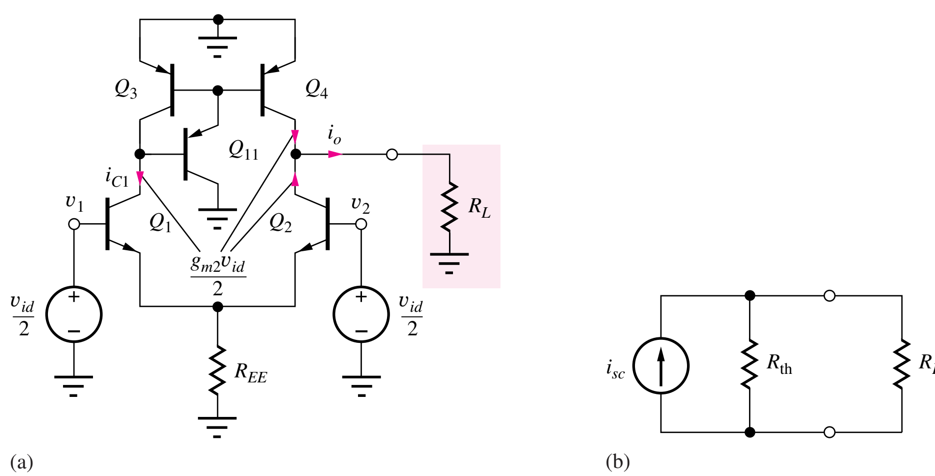


Figure 16.44 (a) BJT differential amplifier with differential-mode input. (b) Equivalent circuit.

EXERCISE: Calculate the dc value of V_{EC4} if the circuit buffered current mirror replaces the active load in Fig. 16.43. What is V_{OS} if $A_{dd} = 100$?

ANSWERS: $V_{EC4} = 1.25$ V and $\Delta V_{EC} = 47$ mV; $V_{OS} = 0.47$ mV

It should be noted that Eq. (16.94) actually overestimates the value of V_{EC4} because the increase in V_{EC4} decreases V_{CE2} and thereby reduces I_{C2}.

Differential-Mode Signal Analysis

Analysis of the ac behavior of the differential amplifier begins with the differential-mode input applied in the ac circuit model in Fig. 16.44. The differential input pair produces equal and opposite currents with amplitude $g_{m2}v_{id}/2$ at the collectors of Q_1 and Q_2. Collector current i_{c1} is supplied by Q_3 and is replicated at the output of Q_4. Thus the total short circuit output current is equal to

$$\mathbf{i_{sc}} = 2\frac{g_{m2}\mathbf{v_{id}}}{2} = g_{m2}\mathbf{v_{id}} \tag{16.96}$$

The output resistance is identical to Eq. (16.75)

$$R_{\text{th}} = r_{o2} \| r_{o4} \tag{16.97}$$

and

$$A_{dd} = \frac{i_{sc}(R_L \| R_{\text{th}})}{v_{dm}} = g_{m2}(R_L \| r_{o2} \| r_{o4}) = -g_{m2}R_L \tag{16.98}$$

The current mirror provides a single-ended output but with a voltage equal to the full gain of the C-E amplifier, just as for the FET case. Here we have included R_L which models the loading of the next stage in a multistage amplifier.

The power of the current mirror is again most apparent when additional stages are added, as in the prototype operational amplifier in Fig. 16.45. The resistance at the output of the differential input stage, node 1, is now equivalent to the parallel combination of the output resistances of transistors Q_2 and Q_4 and the input resistance of Q_5 ($R_L = r_{\pi 5}$):

$$R_{\text{eq}} = r_{o2} \| r_{o4} \| r_{\pi 5} \cong r_{\pi 5} \tag{16.99}$$

and the gain of the differential input stage becomes

$$A_{dm} = g_{m2}R_{\text{eq}} \cong g_{m2}r_{\pi 5} = \beta_{o5}\frac{I_{C2}}{I_{C5}} \tag{16.100}$$

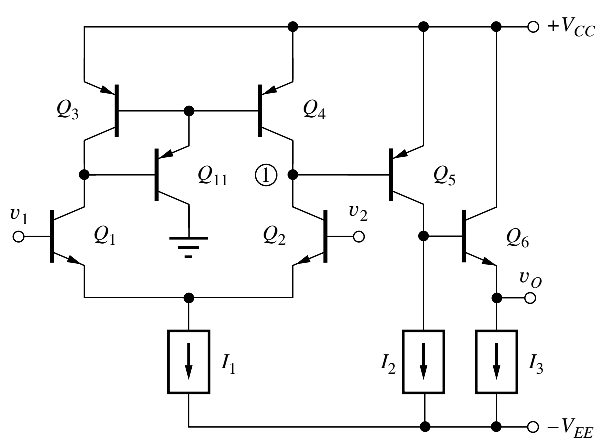


Figure 16.45 Bipolar op amp with active load in first stage.

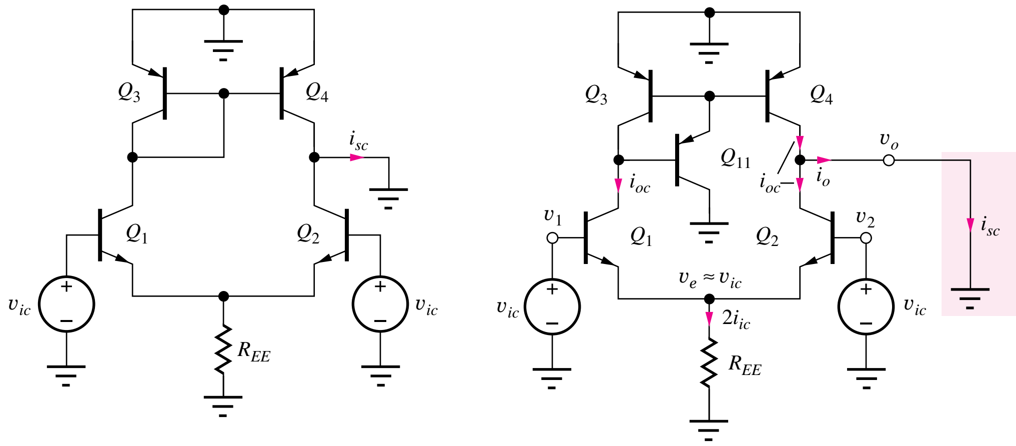


Figure 16.46 Bipolar differential amplifiers with common-mode input.

EXERCISE: What is the approximate differential-mode voltage gain of the amplifier in Fig. 16.45 if $\beta_{FO} = 150$, $V_A = 75$ V, and $I_{C5} = 3\ I_{C2}$?

ANSWER: 50

Common-Mode Input Signals

The circuits in Fig. 16.46 represent the bipolar differential amplifier with current mirror load and a buffered current mirror load. The detailed analysis is quite involved and tedious, particularly for the buffered mirror, so here we will argue the result based on earlier analyses. The common-mode current i_{oc} in Q_1 and Q_2 is found with the help of Eq. (15.87):

$$i_{oc} = \frac{A_{cc} v_{ic}}{R_C} = v_{ic}\left(\frac{1}{2R_{EE}} - \frac{1}{\beta_o r_o}\right) \tag{16.101}$$

The current from Q_1 is mirrored at the output of Q_4 with a mirror error of $2/\beta_o$. Thus the short-circuit output current is

$$i_{sc} = v_{ic}\frac{2}{\beta_o}\left(\frac{1}{\beta_o r_o} - \frac{1}{2R_{EE}}\right) \tag{16.102}$$

In a manner similar to that of the FET pair, the voltage developed at the collector of Q_1, i_{oc}/g_{m3}, forces a current in the differential output resistance of the pair $(2r_{o2})$, which is doubled by the action of the current mirror:

$$i_{sc} = 2v_{ic}\left(\frac{1}{\beta_o r_o} - \frac{1}{2R_{EE}}\right)\frac{1}{g_{m3}(2r_{o2})} \cong \frac{v_{ic}}{\mu_{f2}}\left(\frac{1}{\beta_o r_o} - \frac{1}{2R_{EE}}\right) \tag{16.103}$$

Since $\mu_f \gg \beta_o$ for the BJT, the output will be dominated by Eq. (16.102) and the CMRR is

$$\text{CMRR} = \left|\frac{g_{m2} R_{\text{th}}}{i_{sc} R_{\text{th}}/v_{ic}}\right| \cong \left[\frac{2}{\beta_{o3}}\left(\frac{1}{\beta_{o2}\mu_{f2}} - \frac{1}{2g_{m2} R_{EE}}\right)\right]^{-1} \tag{16.104}$$

EXERCISE: Evaluate Eq. (16.104) for $\beta_F = 100$, $V_A = 75$ V, $I_{EE} = 200$ μA, and $R_{EE} = 10$ MΩ.

ANSWER: 5.45×10^6 or 135 dB

The expression in Eq. (16.104) yields a very large CMRR that is almost impossible to achieve. The CMRR predicted for the buffered current mirror is even larger, since the mirror error is approximately $2/\beta_{o11}\beta_{o3}$. In both these circuits, however, the CMRR will actually be limited to much smaller levels by small mismatches between the various transistors:

$$\text{CMRR}^{-1} = \left[\left(\frac{\Delta g_m}{g_m} + \frac{\Delta g_\pi}{g_\pi}\right)\left(\frac{1}{2g_m R_{SS}} + \frac{1}{\mu_f}\right) - \frac{\Delta g_o}{g_o}\frac{1}{\mu_f}\right] \tag{16.105}$$

Equation (16.105) is similar to the results for the FET from Eq. (16.88) with the addition of the $\Delta g_\pi / g_\pi$ term. In an actual amplifier, the common-mode gain is determined by small imbalances in the bipolar transistors and overall symmetry of the amplifier.

16.7 ACTIVE LOADS IN OPERATIONAL AMPLIFIERS

Let us now explore more fully the use of active loads in MOS and bipolar operational amplifiers. Figure 16.47 shows a complete three-stage MOS operational amplifier. The input stage consists of NMOS differential pair M_1 and M_2 with PMOS current mirror load, M_3 and M_4, followed by a second common-source gain stage M_5 loaded by current source M_{10}. The output stage is a class-AB amplifier consisting of transistors M_6 and M_7. Bias currents I_1 and I_2 for the two gain stages are set by the current mirrors formed by transistors M_8, M_9, and M_{10}, and class-AB bias for the output stage is set by the voltage developed across resistor R_{GG}. At most, only two resistors are required: R_{GG} and one for the current mirror reference current.

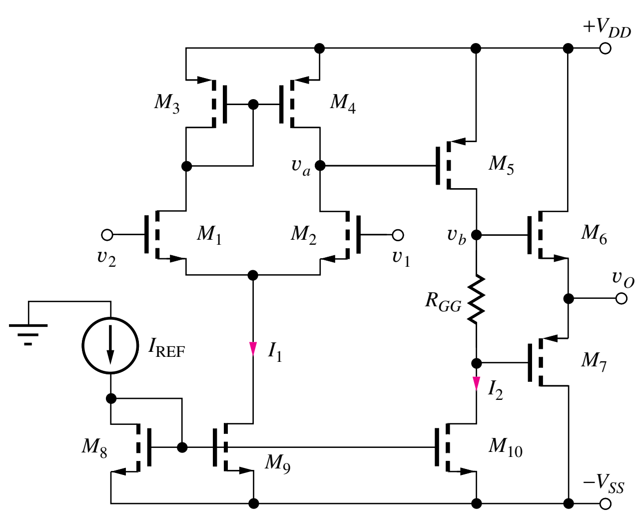


Figure 16.47 Complete CMOS op amp with current mirror bias.

16.7.1 CMOS Op Amp Voltage Gain

Assuming that the gain of the output stage is approximately 1, then the overall differential-mode gain A_{dm} of the three-stage operational amplifier is approximately equal to the product of the terminal gains of the first two stages:

$$A_{dm} = \frac{\mathbf{v_a}}{\mathbf{v_{id}}}\frac{\mathbf{v_b}}{\mathbf{v_a}}\frac{\mathbf{v_o}}{\mathbf{v_b}} = A_{vt1}A_{vt2}(1) \cong A_{vt1}A_{vt2} \quad (16.106)$$

As discussed earlier, the input stage provides a gain of

$$A_{vt1} = g_{m2}(r_{o2}\|r_{o4}) \cong \frac{\mu_{f2}}{2} \quad (16.107)$$

The terminal gain of the second stage is equal to

$$A_{vt2} = g_{m5}(r_{o5}\|(R_{GG} + r_{o10})) \cong g_{m5}(r_{o5}\|r_{o10}) \cong g_{m5}(r_{o5}\|r_{o5}) = \frac{\mu_{f5}}{2} \quad (16.108)$$

assuming that the output resistances of M_5 and M_{10} are similar in value and $R_{GG} \ll r_{o10}$. Combining the three equations above yields

$$A_{dm} \cong \frac{\mu_{f2}\mu_{f5}}{4} \quad (16.109)$$

The gain approaches one-quarter of the product of the amplification factors of the two gain stages.

The factor of 4 in the denominator of Eq. (16.109) can be eliminated by improved design. If a Wilson source is used in the first-stage active load, then the output resistance of the current mirror is much greater than r_{o2}, and A_{v1} becomes equal to μ_{f2}. The gain of the second stage can also be increased to the full amplification factor of M_5 if the current source M_{10} is replaced by a Wilson or cascode source. If both these circuit changes are used (see Prob. 16.111), then the gain of the op amp can be increased to

$$A_{dm} \cong \mu_{f2}\mu_{f5} \quad (16.110)$$

This discussion has only scratched the surface of the many techniques available for increasing the gain of the CMOS op amp. Several examples appear in the problems at the end of this chapter; further discussion can be found in the bibliography.

16.7.2 dc Design Considerations

When the circuit in Fig. 16.47 is operating in a closed-loop op amp configuration, the drain current of M_5 must be equal to the output current I_2 of current source transistor M_{10}. For the amplifier to have a minimum offset voltage, the (W/L) ratio of M_5 must be carefully selected so the source-gate bias of M_5, $V_{SG5} = V_{SD4} = V_{SG3}$, is precisely the proper voltage to set $I_{D5} = I_2$. The W/L ratio of M_5 is also usually adjusted to account for V_{DS} and λ differences between M_5 and M_{10}. R_{GG} and the (W/L) ratios of M_6 and M_7 determine the quiescent current in the class-AB output stage.

Even resistor R_{GG} has been eliminated from the op amp in Fig. 16.48 by using the gate-source voltage of FET M_{11} to bias the output stage. The current in the class-AB stage is determined by the W/L ratios of the output transistors and the matching diode-connected MOSFET M_{11}.

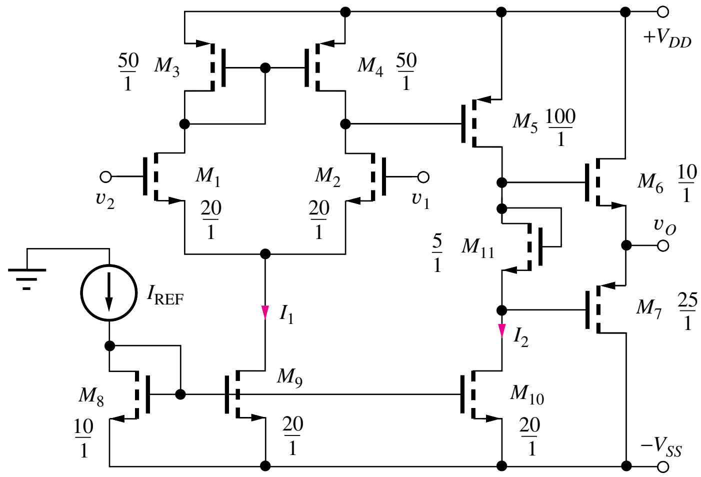


Figure 16.48 Op amp with current mirror bias of the class-AB output stage.

EXAMPLE 16.8 CMOS OP AMP ANALYSIS

Find the small-signal characteristics of a CMOS operational amplifier.

PROBLEM Find the voltage gain, input resistance, and output resistance of the amplifier in Fig. 16.48 if $K'_n = 25\ \mu A/V^2$, $K'_p = 10\ \mu A/V^2$, $V_{TN} = 0.75$ V, $V_{TP} = -0.75$ V, $\lambda = 0.0125\ V^{-1}$, $V_{DD} = V_{SS} = 5$ V, and $I_{REF} = 100\ \mu A$.

SOLUTION **Known Information and Given Data:** The schematic for the operational amplifier appears in Fig. 10.48; $V_{DD} = V_{SS} = 5$ V, and $I_{REF} = 100\ \mu A$; device parameters are given as $K'_n = 25\ \mu A/V^2$, $K'_p = 10\ \mu A/V^2$, $V_{TN} = 0.75$ V, $V_{TP} = -0.75$ V, $\lambda = 0.0125\ V^{-1}$.

Unknowns: Q-points, A_{dm}, R_{id}, and R_{out}

Approach: Find the Q-point currents and use the device parameters to evaluate Eq. (16.109) for A_{dm}. Since we have MOSFETS at the input, $R_{id} = R_{ic} = \infty$. R_{out} is set by M_6 and M_7: $R_{out} = (1/g_{m6})\|(1/g_{m7})$.

Assumptions: MOSFETs operate in the active region.

Analysis: The gain can be estimated using Eq. (16.109).

$$A_{dm} \cong \frac{\mu_{f2}\mu_{f5}}{4} = \frac{1}{4}\left(\frac{1}{\lambda_2}\sqrt{\frac{2K_{n2}}{I_{D2}}}\right)\left(\frac{1}{\lambda_5}\sqrt{\frac{2K_{p5}}{I_{D5}}}\right)$$

For the amplifier in Fig. 16.50,

$$I_{D2} = \frac{I_1}{2} = \frac{2I_{REF}}{2} = 100\ \mu A \qquad I_{D5} = I_2 = 2I_{REF} = 200\ \mu A$$

$$K_{n2} = 20K'_n = 500\frac{\mu A}{V^2} \qquad K_{p5} = 100K'_p = 1000\frac{\mu A}{V^2}$$

and

$$A_{dm} \cong \frac{\mu_{f2}\mu_{f5}}{4} = \frac{1}{4}\left(\frac{1}{0.0125}\right)^2 \mathrm{V}^2 \sqrt{\frac{2\left(500\dfrac{\mu\mathrm{A}}{\mathrm{V}^2}\right)}{100\ \mu\mathrm{A}}} \sqrt{\frac{2\left(1000\dfrac{\mu\mathrm{A}}{\mathrm{V}^2}\right)}{200\ \mu\mathrm{A}}} = 16{,}000$$

The input resistance is twice the input resistance of M_1, which is infinite: $R_{id} = \infty$. The output resistance is determined by the parallel combination of the output resistances of M_6 and M_7, which act as two source followers operating in parallel:

$$R_{\text{out}} = \frac{1}{g_{m6}} \left\| \frac{1}{g_{m7}} = \frac{1}{\sqrt{2K_{n6}I_{D6}}} \right\| \frac{1}{\sqrt{2K_{p7}I_{D7}}}$$

To evaluate this expression, the current in the output stage must be found. The gate-source voltage of M_{11} is

$$V_{GS11} = V_{TN11} + \sqrt{\frac{2I_{D11}}{K_{n11}}} = 0.75\ \mathrm{V} + \sqrt{\frac{2(200\ \mu\mathrm{A})}{125\left(\dfrac{\mu\mathrm{A}}{\mathrm{V}^2}\right)}} = 2.54\ \mathrm{V}$$

In this design, $V_{TP} = -V_{TN}$ and the W/L ratios of M_6 and M_7 have been chosen so that $K_{p7} = K_{n6}$. Because I_{D6} must equal I_{D7}, $V_{GS6} = V_{SG7}$. Thus, both V_{GS6} and V_{SG7} are equal to one-half V_{GS11}, and

$$I_{D7} = I_{D6} = \frac{250}{2}\frac{\mu\mathrm{A}}{\mathrm{V}^2}(1.27\ \mathrm{V} - 0.75\ \mathrm{V})^2 = 33.7\ \mu\mathrm{A}$$

The transconductances of M_6 and M_7 are also equal,

$$g_{m7} = g_{m6} = \sqrt{2\left(2.50 \times 10^{-4}\frac{\mu\mathrm{A}}{\mathrm{V}^2}\right)(33.7 \times 10^{-6}\ \mu\mathrm{A})} = 1.30 \times 10^{-4}\ \mathrm{S}$$

and the output resistance at the Q-point is $R_{\text{out}} = 3.85\ \mathrm{k}\Omega$.

Check of Results: A double check of our hand calculations indicates they are correct. Because of the complexity of the circuit, SPICE simulation represents an excellent check of hand calculations. The simulation results appear in the next exercise.

Discussion: Simulation of the open-loop characteristics of high-gain amplifiers in SPICE can be difficult. The open-loop gain will amplify the offset voltage of the amplifier and may saturate the output. One approach is to first determine the offset voltage and then to apply a compensating voltage to the amplifier input to bring the output near zero. The steps are outlined next. In very high gain cases, SPICE may still be unable to converge because numerical "noise" during the simulation steps is amplified just as an input voltage. The successive voltage and current injection method discussed in Chapter 18 solves this problem.

Computer-Aided Analysis: After drawing the circuit of Fig. 16.48 with the schematic editor, be sure to set the device parameters to the desired values. For the NMOS devices, KP = 25 μA/V^2, VTO = 0.75 V, and LAMBDA = 0.0125 V^{-1}. For the PMOS devices, KP = 10 μA/V^2, VTO = −0.75 V, and LAMBDA = 0.0125 V^{-1}. W and L must be specified for each individual transistor. For example, use $W = 5\ \mu$m and $L = 1\ \mu$m for a 5/1 device.

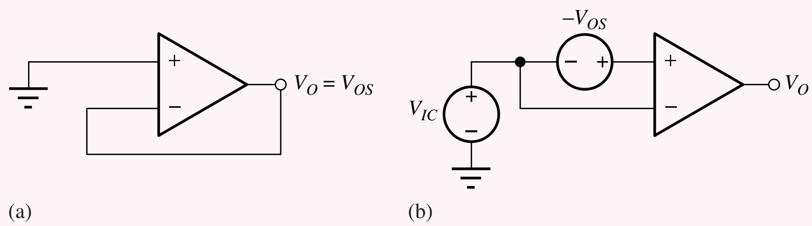


Figure 16.49 Op amp setups for SPICE simulation. (a) Offset voltage determination. (b) Circuit for open-loop analysis using SPICE transfer functions.

The first step in the simulation is to find the offset voltage by operating the op amp in a voltage-follower configuration for which $V_O = V_{OS}$, as in Fig. 16.49(a). V_{OS} is then applied as a differential input to the amplifier in Fig. 16.49(b) with a common-mode input $V_{IC} = 0$. If the value of V_{OS} is correct, an operating point analysis should yield a value of approximately 0 for V_O. A transfer function analysis from V_{OS} to the output will give values of A_{dm}, R_{id}, and R_{out}. A transfer function analysis from V_{IC} to the output will give A_{cm}, R_{ic}, and R_{out}. The SPICE results are given as the answers to the next exercise.

EXERCISE: **Simulate the amplifier in Fig. 16.48 using SPICE and compare the results to the answers in Ex. 16.6. Which terminal is the noninverting input? What are the offset voltage, common-mode and differential-mode gains, CMRR, common-mode and differential-mode input resistances, and output resistance?**

ANSWERS: **v_1; 64.164 mV; 17,800; 0.052; 90.7 dB; ∞; ∞; 3.63 kΩ**

16.7.3 Bipolar Operational Amplifiers

Active-load techniques can be applied equally well to bipolar op amps. In fact, most of the techniques discussed thus far were developed first for bipolar amplifiers and later applied to MOS circuits as NMOS and CMOS technologies matured. In the circuit in Fig. 16.50, a differential input stage with active load is formed by transistors Q_1 to Q_4. The first stage is followed by a high gain C-E amplifier formed of Q_5 and its current source load Q_8. Load resistance R_L is driven by the class-AB output stage, consisting of transistors Q_6 and Q_7 biased by current I_2 and diodes Q_{11} and Q_{12}. (The diodes will actually be implemented with BJTs, in this case with emitter areas five times those of Q_6 and Q_7.)

Based on our understanding of multistage amplifiers, the gain of this circuit is approximately $A_{dm} = A_{vt1}A_{vt2}A_{vt3}$ and

$$A_{dm} \cong [g_{m2}r_{\pi 5}][g_{m5}(r_{o5}\|r_{o8}\|(\beta_{o6}+1)R_L)][1] \cong \frac{g_{m2}}{g_{m5}} g_{m5}r_{\pi 5}g_{m5}\frac{r_{o5}}{2} = \frac{I_{C2}}{I_{C5}}\beta_{o5}\frac{\mu_{f5}}{2} \tag{16.111}$$

in which it has been assumed that the input resistance of the class-AB output stage is much larger than the parallel combination of r_{o5} and r_{o8}. Note that the upper limit to Eq. (16.111) is set by the $\beta_o V_A$ product of Q_5, because I_{C2} is typically less than or equal to I_{C5}.

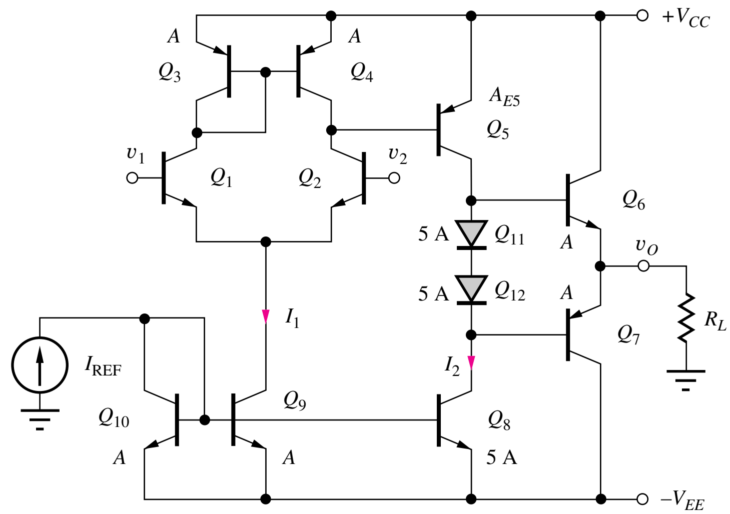


Figure 16.50 Complete bipolar operational amplifier.

EXERCISE: Estimate the voltage gain of the amplifier in Fig. 16.50 using Eq. (16.111) if $I_{REF} = 100\ \mu A$, $V_{A5} = 60$ V, $\beta_{o1} = 150$, $\beta_{o5} = 50$, $R_L = 2$ MΩ, and $V_{CC} = V_{EE} = 15$ V. What is the gain of the first stage? The second stage? What should be the emitter area of Q_5? What is R_{ID}? Which terminal is the inverting input?

ANSWERS: 7500; 5; 1500; 10 A; 150 kΩ; v_1

EXERCISE: Simulate the amplifier in the previous exercise using SPICE and determine the offset voltage, voltage gain, differential-mode input resistance, CMRR, and common-mode input resistance.

ANSWERS: 3.28 mV; 8440; 165 kΩ; 84.7 dB; 59.1 MΩ

16.7.4 A BJT AMPLIFIER WITH IMPROVED VOLTAGE GAIN

To improve the gain of the amplifier in Fig. 16.50, Eq. (16.107) indicates that we need a transistor with an improved $\beta_o V_A$ product. We also see from the exercise that the first-stage gain is low because $r_{\pi 5}$ is small (the ratio I_{C2}/I_{C5} is too low). Mentally searching through our bag of basic circuit tools, we should discover the two-transistor Darlington circuit, which has a current gain of $\beta_{o1}\beta_{o2}$, an amplification factor of $\mu_{f2}/4$, an output resistance of $r_{o2}/2$, and an input resistance of $2\beta_{o1}r_{\pi 2}$. This configuration has been used to replace Q_5 in the circuit in Fig. 16.51. The *pnp* Darlington circuit requires an emitter-base bias of $2V_{EB}$, and the buffered current mirror provides proper dc balance at the collectors of Q_3 and Q_4.

Let us now determine an expression for the voltage gain of the amplifier in Fig. 16.51. Writing the voltage gain as a product of the gains of the individual stages and assuming the output stage has unity gain,

$$A_{dm} = \frac{\mathbf{v_a}}{\mathbf{v_{id}}}\frac{\mathbf{v_b}}{\mathbf{v_a}}\frac{\mathbf{v_o}}{\mathbf{v_b}} = A_{vt1}A_{vt2}(1) \cong A_{vt1}A_{vt2} \qquad (16.112)$$

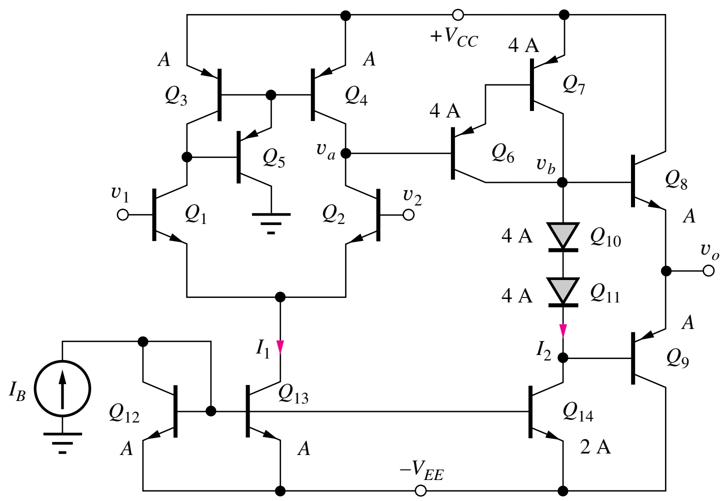


Figure 16.51 Op amp with buffered current mirror and second-stage Darlington circuit.

The input stage provides a gain of

$$A_{vt1} = g_{m2}(r_{o2} \| r_{o4} \| 2\beta_{o6} r_{\pi 7}) \cong g_{m2}\left(\frac{r_{o2}}{2} \middle\| 2\beta_{o6} r_{\pi 7}\right) \tag{16.113}$$

in which the load resistance represents the parallel combination of the output resistances of transistors Q_2 and Q_4 and the input resistance of the Darlington stage. We expect $r_{o4} \cong r_{o2}$, and comparing the input resistance of the Darlington stage to r_{o2} yields

$$\frac{2\beta_{o6} r_{\pi 7}}{r_{o2}} = \frac{2\beta_{o6}\dfrac{\beta_{o7} V_T}{I_{C7}}}{\dfrac{V_{A2} + V_{CE2}}{I_{C2}}} \cong \frac{I_1}{I_2}\frac{0.025\beta_{o6}\beta_{o7}}{V_{A2} + V_{CE2}} \tag{16.114}$$

Using $I_2 = 2I_1$, $\beta_o = 50$, $V_A = 60$ V, and $V_{CE} = 15$ V, we find that the value of Eq. (16.114) is approximately 0.42. Therefore, an estimate for the gain of the first stage is

$$A_{vt1} \cong g_{m2}(0.5r_{o2} \| 0.42r_{o2}) = 0.23\mu_{f2} \tag{16.115}$$

For large values of R_L, we can assume the resistance at node v_b is dominated by the output resistances of the Darlington stage and current source I_2. For this case, the gain of the second stage is equal to

$$A_{vt2} \cong \frac{g_{m7}}{2}\left(\frac{2r_{o7}}{3} \middle\| r_{o14}\right) \cong \frac{g_{m7}}{2}\left(\frac{2r_{o7}}{3} \middle\| r_{o7}\right) = \frac{g_{m7}}{2}\left(\frac{2r_{o7}}{5}\right) = \frac{\mu_{f7}}{5} \tag{16.116}$$

Combining Eqs. (16.112), (16.114), and (16.116) and assuming that the output stage provides a gain of unity yields a final estimate for the voltage gain of the amplifier in Fig. 16.51:

$$A_{dm} \cong \frac{\mu_{f2}\mu_{f7}}{22} = \frac{40(75)\,40(75)}{22} = 4.15 \times 10^5 \tag{16.117}$$

EXERCISE: Calculate the voltage gain of the circuit in Fig. 16.51 including the effect of a 2-kΩ load resistor on the output if the input resistance of the output stage is $(\beta_{o8} + 1)R_L$. Assume $\beta_o = 100$, $V_A + V_{CE} = 75$ V, and $I_B = 100$ μA. Which terminal is the noninverting input?

ANSWERS: 2.14×10^5; v_2

EXERCISE: Use SPICE to determine the offset voltage, voltage gain, differential-mode input resistance, output resistance, CMRR, and common-mode input resistance of the amplifier in Fig. 16.51. Assume $\beta_{on} = 150$, $\beta_{op} = 50$, $V_A = 60$ V, $R_L = 2$ kΩ, and $I_B = 100$ μA.

ANSWERS: 11.6 μV, 2.40×10^5, 128 kΩ, 822 Ω, 120 dB, 57.3 MΩ

We can come up with an almost endless array of circuit permutations to modify the various characteristics of the amplifier in Figs. 16.50 and 16.51. Cascode circuits can be used in the input stage and second stage. In BIMOS technology, FETs can be used to increase the input resistance at Q_5 as well as that of the output stages. A FET input stage will offer higher input resistance but lower voltage gain.

16.7.5 Input Stage Breakdown

Although the bipolar amplifier designs discussed thus far have provided excellent voltage gain, input resistance, and output resistance, the amplifiers all have a significant flaw. The input stage does not offer **overvoltage protection** and can easily be destroyed by the large input voltage differences that can occur, not only under fault conditions but also during unavoidable transients during normal use of the amplifier. For example, the voltage across the input of an op amp can temporarily be equal to the total supply voltage span during slew-rate limited recovery.

Consider the worst-case fault condition applied to the differential pair in Fig. 16.52. Under the conditions shown, the base-emitter junction of Q_1 will be forward-biased, and that of Q_2 reverse-biased by a voltage of $(V_{CC} + V_{EE} - V_{BE1})$. If $V_{CC} = V_{EE} = 22$ V, the reverse voltage exceeds 41 V. Because of heavy doping in the emitter, the typical Zener breakdown voltage of the base-emitter junction of an *npn* transistor is only 5 to 7 V. Thus any voltage exceeding this value by more than one diode drop may destroy at least one of the transistors in the differential input pair.

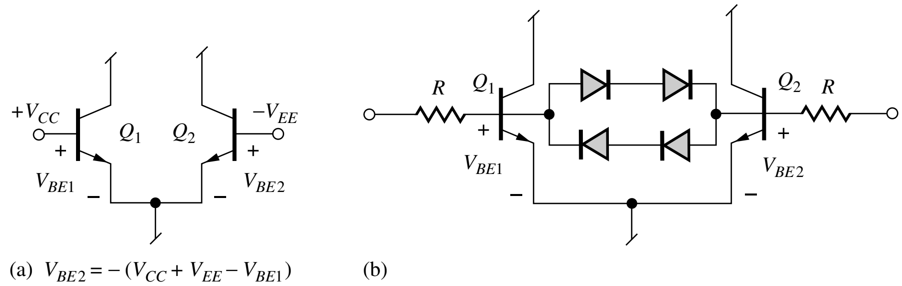


Figure 16.52 (a) Differential input stage voltages under a fault condition. (b) Simple diode input protection circuit.

Early IC op amps required circuit designers to add external diode protection across the input terminals, as shown Fig. 16.52(b). The diodes prevent the differential input voltage from exceeding approximately 1.4 V, but this technique adds extra components and cost to the design. The two resistors limit the current through the diodes. The μA741 described in the next section was the first commercial IC op amp to solve this problem by providing a fully protected input, as well as output, stage.

16.8 THE μA741 OPERATIONAL AMPLIFIER

The now classic Fairchild **μA741** operational-amplifier design was the first to provide a highly robust amplifier from the application engineer's point of view. The amplifier provides excellent overall characteristics (high gain, input resistance and CMRR, low output resistance, and good frequency response) while providing overvoltage protection for the input stage and short-circuit current limiting of the output stage. The 741 style of amplifier design quickly became the industry standard and spawned many related designs. By studying the 741 design, we will find a number of new amplifier circuit design and bias techniques.

Figure 16.53 is a simplified schematic of the μA741 operational amplifier. The three bias sources shown in symbolic form are discussed in more detail following a description of the overall circuit. The op amp has two stages of voltage gain followed by a class-AB output stage. In the first stage, transistors Q_1 to Q_4 form a differential amplifier with a buffered current mirror active load, Q_5 to Q_7. Practical operational amplifiers offer an offset voltage adjustment port, which is provided in the 741 through the addition of 1-kΩ resistors R_1 and R_2 and an external potentiometer R_{EXT}.

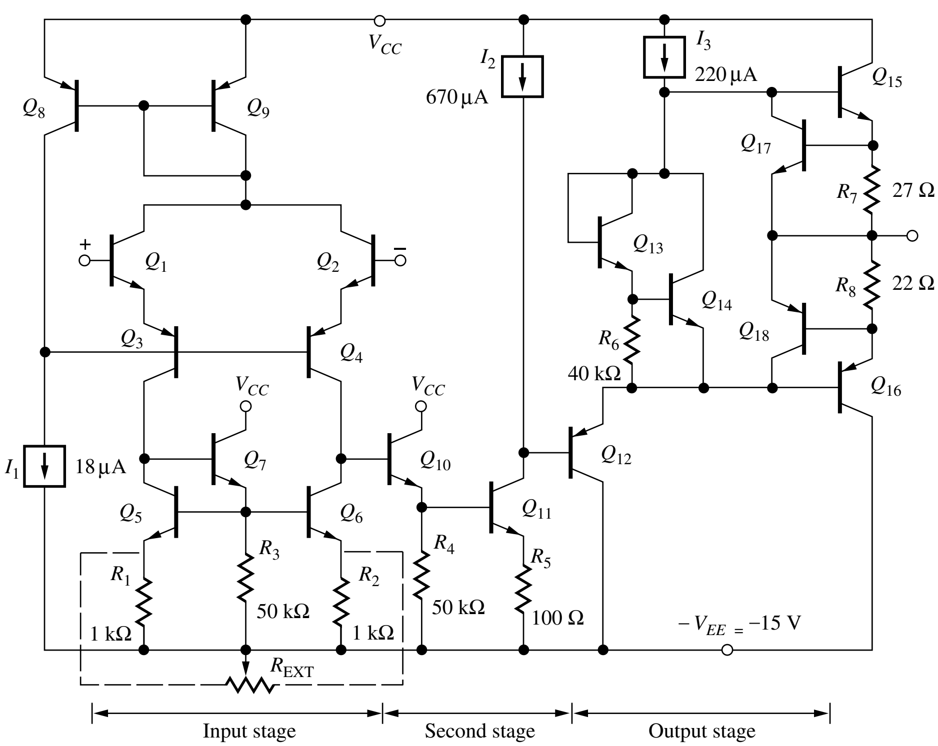


Figure 16.53 Overall schematic of the classic Fairchild μA741 operational amplifier (the bias network appears in Fig. 16.54).

The second stage consists of emitter follower Q_{10} driving common-emitter amplifier Q_{11} with current source I_2 and transistor Q_{12} as load. Transistors Q_{13} to Q_{18} form a short-circuit protected class-AB push-pull output stage that is buffered from the second gain stage by emitter follower Q_{12}.

EXERCISE: Reread this section and be sure you understand the function of each individual transistor in Fig. 16.53. Make a table listing the function of each transistor.

16.8.1 BIAS CIRCUITRY

The three current sources shown symbolically in Fig. 16.53 are generated by the bias circuitry in Fig. 16.54. The value of the current in the two diode-connected reference transistors Q_{20} and Q_{22} is determined by the power supply voltage and resistor R_5:

$$I_{\text{REF}} = \frac{V_{CC} + V_{EE} - 2V_{BE}}{R_5} = \frac{15 + 15 - 1.4}{39\ \text{k}\Omega} = 0.733\ \text{mA} \qquad (16.118)$$

assuming ±15-V supplies. Current I_1 is derived from the Widlar source formed of Q_{20} and Q_{21}. The output current for this design is

$$I_1 = \frac{V_T}{5000} \ln\left[\frac{I_{\text{REF}}}{I_1}\right] \qquad (16.119)$$

Using the reference current calculated in Eq. (16.118) and iteratively solving for I_1 in Eq. (16.119) yields $I_1 = 18.4\ \mu\text{A}$.

The currents in mirror transistors Q_{23} and Q_{24} are related to the reference current I_{REF} by their emitter areas using Eq. (16.17). Assuming $V_O = 0$ and $V_{CC} = 15$ V, and neglecting the voltage drop across R_7 and R_8 in Fig. 16.53, $V_{EC23} = 15 + 1.4 = 16.4$ V and $V_{EC24} = 15 - 0.7 = 14.3$ V.

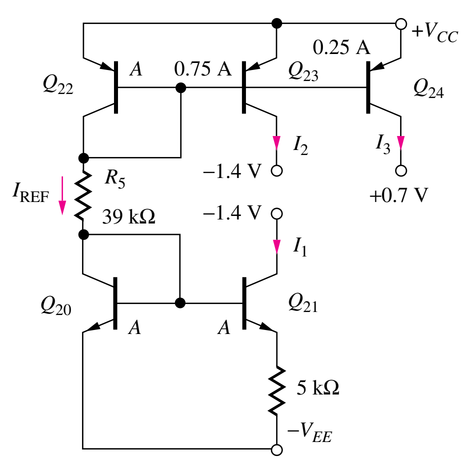


Figure 16.54 741 bias circuitry with voltages corresponding to $V_O = 0$ V.

Using these values with $\beta_F = 50$ and $V_A = 60$ V, the two source currents are

$$I_2 = 0.75(733\ \mu\text{A})\frac{1+\dfrac{16.4\text{ V}}{60\text{ V}}}{1+\dfrac{0.7\text{ V}}{60\text{ V}}+\dfrac{2}{50}} = 666\ \mu\text{A}$$
$$I_3 = 0.25(733\ \mu\text{A})\frac{1+\dfrac{14.4\text{ V}}{60\text{ V}}}{1+\dfrac{0.7\text{ V}}{60\text{ V}}+\dfrac{2}{50}} = 216\ \mu\text{A} \tag{16.120}$$

and the two output resistances are

$$R_2 = \frac{V_{A23}+V_{EC23}}{I_2} = \frac{60\text{ V}+16.4\text{ V}}{0.666\text{ mA}} = 115\text{ k}\Omega$$
$$R_3 = \frac{V_{A24}+V_{EC24}}{I_3} = \frac{60\text{ V}+14.3\text{ V}}{0.216\text{ mA}} = 344\text{ k}\Omega \tag{16.121}$$

Exercise: What are the values of I_{REF}, I_1, I_2, and I_3 in the circuit in Fig. 16.54 for $V_{CC} = V_{EE} = 22$ V?

Answers: 1.09 mA, 20.0 μA, 1.08 mA, 351 μA

Exercise: What is the output resistance of the Widlar source in Fig. 16.54 operating at 18.4 μA for $V_A = 60$ V and $V_{EE} = 15$ V?

Answer: 18.8 MΩ

16.8.2 DC Analysis of the 741 Input Stage

The input stage of the μA741 amplifier is redrawn in the schematic in Fig. 16.55. As noted earlier, Q_1, Q_2, Q_3, and Q_4 form a differential input stage with an active load consisting of the buffered current mirror formed by Q_5, Q_6, and Q_7. In this input stage there are four base-emitter junctions between inputs v_1 and v_2, two from the *npn* transistors and, more importantly, two from the *pnp* transistors, and $(v_1 - v_2) = (V_{BE1} + V_{EB3} - V_{EB4} - V_{BE2})$.

In standard bipolar IC processes, *pnp* transistors are formed from lateral structures in which both junctions exhibit breakdown voltages equal to that of the collector-base junction of the *npn* transistor. This breakdown voltage typically exceeds 50 V. Because most general-purpose op amp specifications limit the power supply voltages to less than ±22 V, the emitter-base junctions of Q_3 and Q_4 provide sufficient breakdown voltage to fully protect the input stage of the amplifier, even under a worst-case fault condition, such as that depicted in Fig. 16.52(a).

Q-Point Analysis

In the 741 input stage in Fig. 16.55, the current mirror formed by transistors Q_8 and Q_9 operates with transistors Q_1 to Q_4 to establish the bias currents for the input stage. Bias current I_1 represents the output of the Widlar source discussed previously (18 μA) and must be equal to the collector

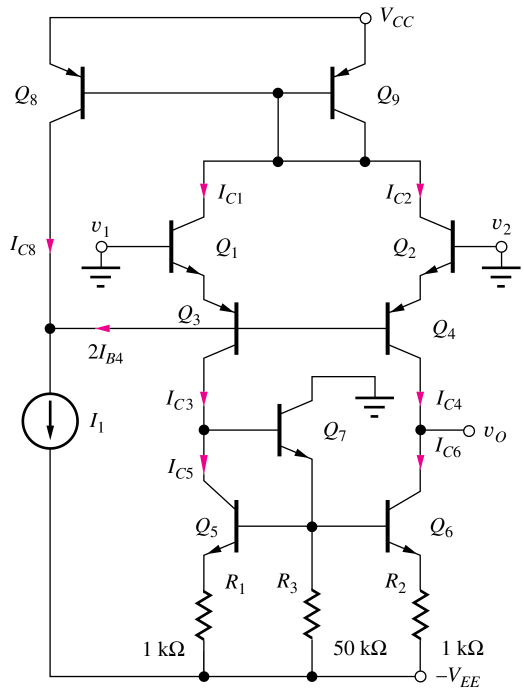


Figure 16.55 μA741 input stage.

current of Q_8 plus the base currents of matched transistors Q_3 and Q_4:

$$I_1 = I_{C8} + I_{B3} + I_{B4} = I_{C8} + 2I_{B4} \tag{16.122}$$

For high current gain, the base currents are small and $I_{C8} \cong I_1$.

The collector current of Q_8 mirrors the collector currents of Q_1 and Q_2, which are summed together in mirror reference transistor Q_9. Assuming high current gain and ignoring the collector-voltage mismatch between Q_7 and Q_8,

$$I_{C8} = I_{C1} + I_{C2} = 2I_{C2} \tag{16.123}$$

Combining Eqs. (16.122) and (16.123) yields the ideal bias relationships for the input stage

$$I_{C1} = I_{C2} \cong \frac{I_1}{2} \qquad \text{and} \qquad I_{C3} = I_{C4} \cong \frac{I_1}{2} \tag{16.124}$$

because the emitter currents of Q_1 and Q_3 and Q_2 and Q_4 must be equal. The collector current of Q_3 establishes a current equal to $I_1/2$ in current mirror transistors Q_5 and Q_6 as well. Thus, transistors Q_1 to Q_6 all operate at a nominal collector current equal to one-half the value of source I_1.

Now that we understand the basic ideas behind the input stage bias circuit, let us perform a more exact analysis. Expanding Eq. (16.122) using the current mirror expression from Eq. (16.9),

$$I_1 = 2I_{C2} \frac{1 + \dfrac{V_{EC8}}{V_{A8}}}{1 + \dfrac{2}{\beta_{FO8}} + \dfrac{V_{EB8}}{V_{A8}}} + 2I_{B4} \tag{16.125}$$

I_{C2} is related to I_{B4} through the current gains of Q_2 and Q_4:

$$I_{C2} = \alpha_{F2} I_{E2} = \alpha_{F2}(\beta_{FO4} + 1) I_{B4} = \frac{\beta_{FO2}}{\beta_{FO2} + 1}(\beta_{FO4} + 1) I_{B4} \tag{16.126}$$

Combining Eqs. (16.125) and (16.126) and solving for I_{C2} assuming small errors yields

$$I_{C2} \cong \frac{I_1}{2} \times \left[\frac{1}{1 + \dfrac{V_{EC8} - V_{EB8}}{V_{A8}} - \dfrac{2}{\beta_{FO8}} + \dfrac{1}{\beta_{FO4}}} \right] \tag{16.127}$$

which is equal to the ideal value of $I_1/2$ but reduced by the nonideal current mirror effects because of finite current gain and Early voltage.

The emitter current of Q_4 must equal the emitter current of Q_2, and so the collector current of Q_4 is

$$I_{C4} = \alpha_{F4} I_{E4} = \alpha_{F4} \frac{I_{C2}}{\alpha_{F2}} = \frac{\beta_{FO4}}{\beta_{FO4} + 1} \frac{\beta_{FO2} + 1}{\beta_{FO2}} I_{C2} \tag{16.128}$$

The use of buffer transistor Q_7 essentially eliminates the current gain defect in the current mirror. Note from the full amplifier circuit in Fig. 16.53 that the base current of transistor Q_{10}, with its 50-kΩ emitter resistor R_4, is designed to be approximately equal to the base current of Q_7, and $V_{CE6} \cong V_{CE5}$ as well. Thus, the current mirror ratio is quite accurate and

$$I_{C5} = I_{C6} = I_{C3} \cong \frac{I_1}{2} \tag{16.129}$$

If 50-kΩ resistor R_3 were omitted, then the emitter current of Q_7 would be equal only to the sum of the base currents of transistors Q_5 and Q_6 and would be quite small. Because of the Q-point dependence of β_F, the current gain of Q_7 would be poor. R_3 increases the operating current of Q_7 to improve its current gain as well as to improve the dc balance and transient response of the amplifier. The value of R_3 is chosen to approximately match I_{B7} to I_{B10}.

To complete the Q-point analysis, the various collector-emitter voltages must be determined. The collectors of Q_1 and Q_2 are $1V_{EB}$ below the positive power supply, whereas the emitters are $1V_{BE}$ below ground potential. Hence,

$$V_{CE1} = V_{CE2} = V_{CC} - V_{EB9} + V_{BE2} \cong V_{CC} \tag{16.130}$$

The collector and emitter of Q_3 are approximately $2V_{BE}$ above the negative power supply voltage and $1V_{BE}$ below ground, respectively:

$$V_{EC3} = V_{E3} - V_{C3} = -0.7 \text{ V} - (-V_{EE} + 1.4 \text{ V}) = V_{EE} - 2.1 \text{ V} \tag{16.131}$$

The buffered current mirror effectively minimizes the error due to the finite current gain of the transistors, and $V_{CE6} = V_{CE5} \cong 2V_{BE} = 1.4$ V, neglecting the small voltage drop (<10 mV) across R_1 and R_2. Finally, the collector of Q_8 is $2V_{BE}$ below zero so that

$$V_{EC8} = V_{CC} + 1.4 \text{ V} \tag{16.132}$$

and the emitter of Q_7 is $1V_{BE}$ above $-V_{EE}$:

$$V_{CE7} = V_{EE} - 0.7 \text{ V} \tag{16.133}$$

EXAMPLE 16.9 **µA741 INPUT STAGE BIAS CURRENTS**

Find the currents in the 741 input stage.

PROBLEM Calculate the bias currents in the 741 input stage if $I_1 = 18$ µA, $\beta_{FOnpn} = 150$, $V_{Anpn} = 75$ V, $\beta_{FOpnp} = 60$, $V_{Apnp} = 60$ V, and $V_{CC} = V_{EE} = 15$ V.

SOLUTION **Known Information and Given Data:** µA741 input stage depicted in Fig. 16.55. $I_1 = 18$µA, $\beta_{FOnpn} = 150$, $V_{Anpn} = 75$ V, $\beta_{FOpnp} = 60$, $V_{Apnp} = 60$ V, and $V_{CC} = V_{EE} = 15$ V.

Unknowns: I_{C1}, I_{C2}, I_{C3}, I_{C4}, I_{C5}, and I_{C6}

Approach: Use given data to evaluate Eqs. (16.127) through (16.129).

Assumptions: Transistors are in the active region; use default values of I_S.

Analysis: From Fig. 16.55, we find that the collector-emitter voltage of Q_8 is equal to $V_{CC} + V_{BE1} + V_{EB3} \cong 16.4$ V. Substituting the known values into Eq. (16.127) gives

$$I_{C2} = \frac{18\ \mu\text{A}}{2} \frac{1}{\dfrac{1 + \dfrac{16.4\text{ V}}{60\text{ V}}}{1 + \dfrac{2}{50} + \dfrac{0.7\text{ V}}{60\text{ V}}} + \dfrac{1}{\dfrac{150}{150+1}(60+1)}} = 7.32\ \mu\text{A}$$

$$I_{C1} = I_{C2} = 7.32\ \mu\text{A}$$

Equation (16.128) yields

$$I_{C3} = I_{C4} = \alpha_{F4}\frac{I_{C2}}{\alpha_{F2}} = \frac{\beta_{FO4}}{\beta_{FO4}+1}\left(\frac{\beta_{FO2}+1}{\beta_{FO2}}\right) I_{C2} = \frac{60}{61}\left(\frac{151}{150}\right) I_{C2} = 7.25\ \mu\text{A}$$

$$I_{C5} \cong I_{C3} = 7.25\ \mu\text{A} \qquad \text{and} \qquad I_{C6} = I_{C4} = 7.25\ \mu\text{A}$$

Check of Results: The basic objective of the bias circuit would be to set all currents to 18 µA/2 or 9 µA. Our calculations are close to this value and appear correct.

Discussion: The actual bias currents are slightly greater than 7 µA, whereas the ideal value would be 9 µA. The dominant source of error arises from the collector-emitter voltage mismatch of the *pnp* current mirror.

Computer-Aided Analysis: We draw the circuit using the schematic editor and set the BJT parameters. For the *npn* devices, BF = 150 and VAF = 75 V. For the *pnp* transistors, BF = 60 and VAF = 60 V. Source V_O is added to balance the circuit by forcing the output voltage to the same voltage as that which will appear at the collector of Q_5. Otherwise, the voltage at the collectors of Q_4 and Q_6 will float to a value determined by the difference in overall output resistances of transistors Q_4 and Q_6. When balance is achieved, the current in source V_O will be nearly zero. Table 16.3 summarizes the Q-points based on these calculations and Eqs. (16.124) to (16.129) and compares them with the SPICE operating point simulation results.

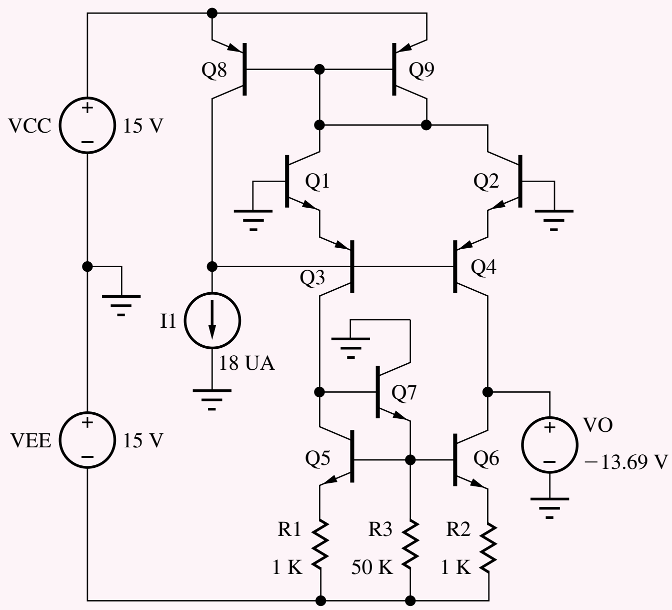


TABLE 16.3
Q-points of 741 Input Stage Transistors for $I_1 = 18\ \mu A$ and $V_{CC} = V_{EE} = 15$ V

TRANSISTORS	Q-POINT	SPICE RESULTS
Q_1 and Q_2	7.32 μA, 15 V	7.30 μA, 15.0 V
Q_3 and Q_4	7.25 μA, 12.9 V	7.24 μA, 13.0 V
Q_5 and Q_6	7.25 μA, 1.4 V	7.16 μA, 1.30 V
Q_7	12.2 μA, 14.3 V	13.1 μA, 14.3 V
Q_8	17.7 μA, 16.4 V	17.8 μA, 16.3 V
Q_9	14.0 μA, 0.7 V	14.1 μA, 0.66 V

EXERCISE: Remove V_O and simulate the 741 input stage amplifier. What are the new collector currents? What are the voltages at the collectors or Q_5 and Q_6?

ANSWERS: 7.31 μA, 7.28 μA, 7.25 μA, 7.22 μA, 7.18 μA, 7.22 μA, 13.1 μA, 17.8 μA, 14.1 μA; −13.7 V, −13.1 V

EXERCISE: Suppose buffer transistor Q_7 and resistor R_3 are eliminated from the amplifier in Fig. 16.55 and Q_5 and Q_6 were connected as a standard current mirror. What would be the collector-emitter voltage of Q_6 if $V_{BE6} = 0.7$ V, $\beta_{FO6} = 100$, and $V_{A6} = 60$ V? Use Eq. (16.89).

ANSWER: 1.90 V

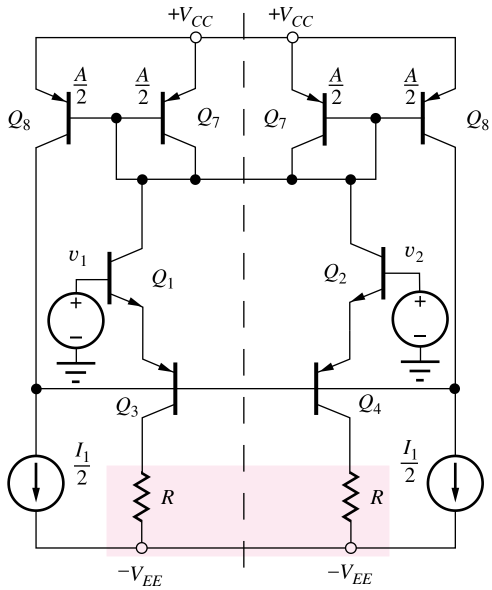


Figure 16.56 Symmetry in the 741 input stage.

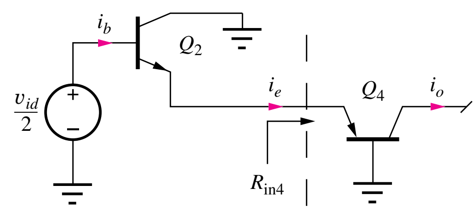


Figure 16.57 Differential-mode half-circuit for the 741 input stage.

16.8.3 AC Analysis of the 741 Input Stage

The 741 input stage is redrawn in symmetric form in Fig. 16.56, with its active load temporarily replaced by two resistors. From Fig. 16.56, we see that the collectors of Q_1 and Q_2 as well as the bases of Q_3 and Q_4 lie on the line of symmetry of the amplifier and represent virtual grounds for differential-mode input signals.

The corresponding differential-mode half-circuit shown in Fig. 16.57 is a common-collector stage followed by a common-base stage, a C-C/C-B cascade. The characteristics of the C-C/C-B cascade can be determined from Fig. 16.57 and our knowledge of single-stage amplifiers.

The emitter current of Q_2 is equal to its base current i_b multiplied by $(\beta_{o2} + 1)$, and the collector current of Q_4 is α_{o4} times the emitter current. Thus, the output current can be written as

$$\mathbf{i_o} = \alpha_{o4}\mathbf{i_e} = \alpha_{o4}(\beta_{o2} + 1)\mathbf{i_b} \cong \beta_{o2}\mathbf{i_b} \tag{16.134}$$

The base current is determined by the input resistance to Q_2:

$$\mathbf{i_b} = \frac{\dfrac{\mathbf{v_{id}}}{2}}{r_{\pi 2} + (\beta_{o2} + 1)R_{in4}} = \frac{\dfrac{\mathbf{v_{id}}}{2}}{r_{\pi 2} + (\beta_{o2} + 1)\left(\dfrac{r_{\pi 4}}{\beta_{o4} + 1}\right)} = \frac{\dfrac{\mathbf{v_{id}}}{2}}{r_{\pi 2} + r_{\pi 4}} \cong \frac{\mathbf{v_{id}}}{4r_{\pi 2}} \tag{16.135}$$

in which $R_{in4} = r_{\pi 4}/(\beta_{o4} + 1)$ represents the input resistance of the common-base stage. Combining Eqs. (16.134) and (16.135) yields

$$\mathbf{i_o} \cong \beta_{o2}\frac{\mathbf{v_{id}}}{4r_{\pi 2}} = \frac{g_{m2}}{4}\mathbf{v_{id}} \tag{16.136}$$

Each side of the C-C/C-B input stage has a transconductance equal to one-half of the transconductance of the standard differential pair. From Eq. (16.135) we can also see that the differential-mode

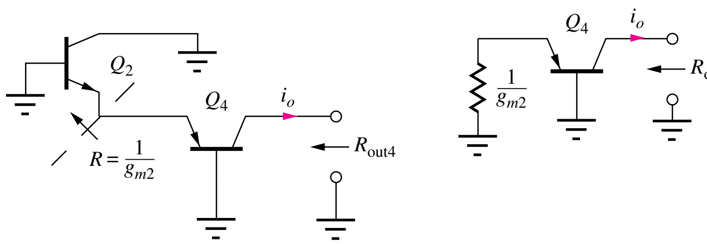


Figure 16.58 Output resistance of C-C/C-B cascade.

input resistance is twice the value of the corresponding C-E stage:

$$R_{id} = \frac{\mathbf{v_{id}}}{\mathbf{i_b}} = 4r_{\pi 2} \tag{16.137}$$

From Fig. 16.58, we can see that the output resistance is equivalent to that of a common-base stage with a resistor of value $1/g_{m2}$ in its emitter:

$$R_{\text{out}} \cong r_{o4}(1 + g_{m4}R) = r_{o4}\left(1 + g_{m4}\frac{1}{g_{m2}}\right) = 2r_{o4} \tag{16.138}$$

16.8.4 Voltage Gain of the Complete Amplifier

We now use the results from the previous section to analyze the overall ac performance of the op amp. We find a Norton equivalent circuit for the input stage and then couple it with a two-port model for the second stage.

Norton Equivalent of the Input Stage

Figure 16.59 is the simplified differential-mode ac equivalent circuit for the input stage. We use Figure 16.59(a) to find the short-circuit output current of the first stage. Based on our analysis of Fig. 16.57, the differential-mode input signal establishes equal and opposite currents in the two

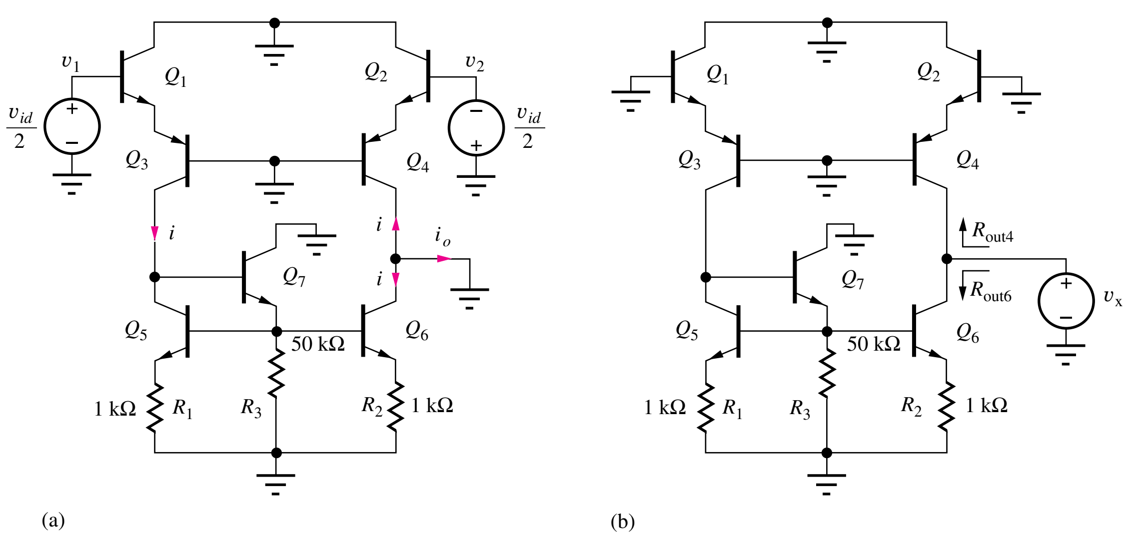


Figure 16.59 Circuits for finding the Norton equivalent of the input stage.

sides of the differential amplifier where $\mathbf{i} = (g_{m2}/4)\mathbf{v_{id}}$. Current i, exiting the collector of Q_3, is mirrored by the buffered current mirror so that a total signal current equal to $2i$ flows in the output terminal:

$$\mathbf{i_o} = -2\mathbf{i} = -\frac{g_{m2}\mathbf{v_{id}}}{2} = (-20I_{C2})\mathbf{v_{id}}$$
$$= -\left(\frac{20}{\text{V}}7.32 \times 10^{-6}\text{ A}\right)\mathbf{v_{id}} = (-1.46 \times 10^{-4}\text{ S})\mathbf{v_{id}} \tag{16.139}$$

The Thévenin equivalent resistance at the output is found using the circuit in Fig. 16.59(b) and is equal to

$$R_{\text{th}} = R_{\text{out6}} \| R_{\text{out4}} \tag{16.140}$$

Because only a small dc voltage is developed across R_2, the output resistance of Q_6 can be calculated from

$$R_{\text{out6}} \cong r_{o6}[1 + g_{m6}R_2] \cong r_{o6}\left[1 + \frac{I_{C6}R_2}{V_T}\right] = r_{o6}\left[1 + \frac{0.0073\text{ V}}{0.025\text{ V}}\right] = 1.3r_{o6} \tag{16.141}$$

The output resistance of Q_4 was already found in Eq. (16.138) to be $2r_{o4}$. Substituting the results from Eqs. (16.138) and (16.141) into Eq. (16.140),

$$R_{\text{th}} = 2r_{o4} \| 1.3r_{o6} = 0.79r_{o4} \cong 0.79\frac{60\text{ V}}{7.25 \times 10^{-6}\text{ A}} = 6.54\text{ M}\Omega \tag{16.142}$$

in which $r_{o4} = r_{o2}$ has been assumed for simplicity with $V_A + V_{CE} = 60$ V.

The resulting Norton equivalent circuit for the input stage appears in Fig. 16.60. Based on the values in this figure, the open-circuit voltage gain of the first stage is −955. SPICE simulations yield values very similar to those in Fig. 16.60: $(1.40 \times 10^{-4}\text{ S})\mathbf{v_{id}}$, 6.95 MΩ, and $A_{dm} = -973$.

EXERCISE: Improve the estimate of R_{th} using the actual values of V_{CE6} and V_{CE4} if $V_{CC} = V_{EE} = 15$ V and $V_A = 60$ V. What are the values of R_{out4} and R_{out6}?

ANSWERS: 7.12 MΩ; 20.2 MΩ, 11.0 MΩ

Model for the Second Stage

Figure 16.61 is a two-port representation for the second stage of the amplifier. Q_{10} is an emitter follower that provides high input resistance and drives a common-emitter amplifier consisting

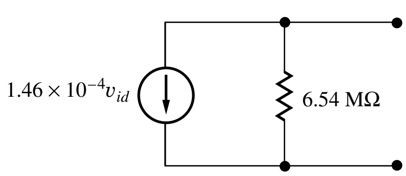


Figure 16.60 Norton equivalent of the 741 input stage.

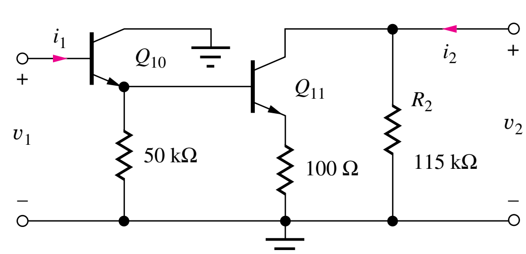


Figure 16.61 Two-port representation for the second stage.

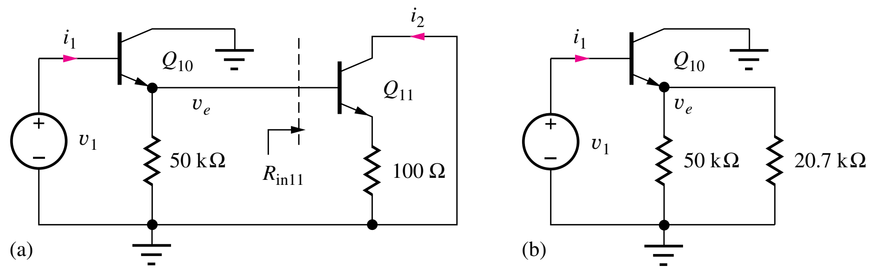


Figure 16.62 Network for finding y_{11} and y_{21}.

of Q_{11} and its current source load represented by output resistance R_2. A y-parameter model is constructed for this network.

From Fig. 16.53 and the bias current analysis, we can see that the collector current of Q_{11} is approximately equal to I_2 or 666 μA. Calculating the collector current of Q_{10} yields

$$I_{C10} \cong I_{E10} = \frac{I_{C11}}{\beta_{F11}} + \frac{V_{B11}}{50\text{ k}\Omega} = \frac{666\ \mu\text{A}}{150} + \frac{0.7 + (0.67\text{ mA})(0.1\text{ k}\Omega)}{50\text{ k}\Omega} = 19.8\ \mu\text{A} \quad (16.143)$$

Using these values to find the small-signal parameters with ($\beta_{on} = 150$) gives

$$r_{\pi 10} = \frac{\beta_{o10} V_T}{I_{C10}} = \frac{3.75\text{ V}}{19.8\ \mu\text{A}} = 189\text{ k}\Omega \qquad \text{and} \qquad \text{r}_{\pi 11} = \frac{3.75\text{ V}}{0.666\text{ mA}} = 5.63\text{ k}\Omega \quad (16.144)$$

Parameters y_{11} and y_{21} are calculated by applying a voltage v_1 to the input port and setting $v_2 = 0$, as in Fig. 16.62. The input resistance to Q_{11} is that of a common-emitter stage with a 100-Ω emitter resistor:

$$R_{in11} = r_{\pi 11} + (\beta_{o11} + 1)100 \cong 5630 + (151)100 = 20.7\text{ k}\Omega \quad (16.145)$$

This value is used to simplify the circuit, as in Fig. 16.62(b), and the input resistance to Q_{10} is

$$\begin{aligned}[y_{11}]^{-1} &= r_{\pi 10} + (\beta_{o10} + 1)(50\text{ k}\Omega \| R_{in11}) \\ &= 189\text{ k}\Omega + (151)(50\text{ k}\Omega \| 20.7\text{ k}\Omega) = 2.40\text{ M}\Omega\end{aligned} \quad (16.146)$$

The gain of emitter follower Q_{10} is:

$$\begin{aligned}\mathbf{v_e} &= \mathbf{v_1}\frac{(\beta_{o10} + 1)(50\text{ k}\Omega \| R_{in11})}{r_{\pi 10} + (\beta_{o10} + 1)(50\text{ k}\Omega \| R_{in11})} \\ &= \frac{(151)(50\text{ k}\Omega \| 20.7\text{ k}\Omega)}{189\text{ k}\Omega + (151)(50\text{ k}\Omega \| 20.7\text{ k}\Omega)} = 0.921\mathbf{v_1}\end{aligned} \quad (16.147)$$

The output current $\mathbf{i_2}$ in Fig. 16.60(a) is given by

$$\mathbf{i_2} = \frac{\mathbf{v_e}}{\dfrac{1}{g_{m11}} + 100\ \Omega} = \frac{0.921\mathbf{v_1}}{\dfrac{1}{\dfrac{40}{\text{V}}(0.666\text{ mA})} + 100\ \Omega} = 0.00670\mathbf{v_1} \quad (16.148)$$

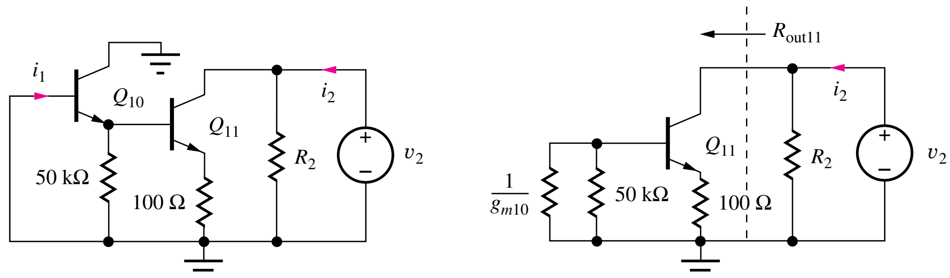


Figure 16.63 Network for finding y_{12} and y_{22}.

yielding a forward transconductance of

$$y_{21} = 6.70 \text{ mS} \tag{16.149}$$

Parameters y_{12} and y_{22} can be found from the network in Fig. 16.63. We assume that the reverse transconductance y_{12} is negligible and reserve its calculation for Prob. 16.133. The output conductance y_{22} can be determined from Fig. 16.63(b).

$$[y_{22}]^{-1} = R_2 \| R_{out11} \tag{16.150}$$

where $R_2 = 115$ kΩ was calculated during the analysis of the bias circuit.

Because the voltage drop across the 100-Ω resistor is small, the output resistance of Q_{11} is approximately

$$\begin{aligned} R_{out11} &= r_{o11}[1 + g_{m11}R_E] = \frac{V_{A11} + V_{CE11}}{I_{C11}}\left[1 + \frac{I_{C11}R_E}{V_T}\right] \\ &= \frac{60 \text{ V} + 13.6 \text{ V}}{0.666 \text{ mA}}\left[1 + \frac{0.067 \text{ V}}{0.025 \text{ V}}\right] = 407 \text{ k}\Omega \end{aligned} \tag{16.151}$$

and

$$[y_{22}]^{-1} = 115 \text{ k}\Omega \| 407 \text{ k}\Omega = 89.1 \text{ k}\Omega \tag{16.152}$$

Figure 16.64 depicts the completed two-port model for the second stage, driven by the Norton equivalent of the input stage. Using this model, the open-circuit voltage gain for the first two stages of the amplifier is

$$\begin{aligned} \mathbf{v_2} &= -0.00670(89.1 \text{ k}\Omega)\mathbf{v_1} = -597\mathbf{v_1} \\ \mathbf{v_1} &= -1.46 \times 10^{-4}(6.54 \text{ M}\Omega \| 2.40 \text{ M}\Omega)\mathbf{v_{id}} = -256\mathbf{v_{id}} \\ \mathbf{v_2} &= -597(-256\mathbf{v_{id}}) = 153{,}000\mathbf{v_{id}} \end{aligned} \tag{16.153}$$

Note from Eq. (16.152) that the 2.42-MΩ input resistance of Q_{10} reduces the voltage gain of the first stage by a factor of almost 4.

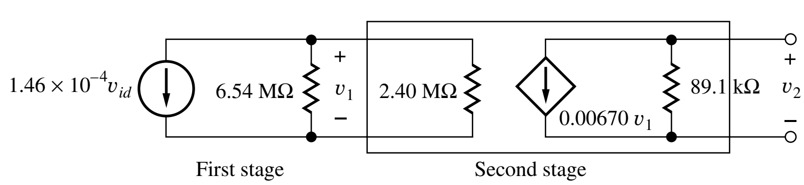


Figure 16.64 Combined model for first and second stages.

EXERCISE: What would be the voltage gain of the input stage if transistor Q_{10} and its 50-kΩ emitter resistor were omitted so that the output of the first stage would be connected directly to the base of Q_{11}? Use the small-signal element values already calculated.

ANSWER: −3.00

16.8.5 THE 741 OUTPUT STAGE

Figure 16.65 shows simplified models for the 741 output stage. Transistor Q_{12} is the emitter follower that buffers the high impedance node at the output of the second stage and drives the push-pull output stage composed of transistors Q_{15} and Q_{16}. Class-AB bias is provided by the sum of the base-emitter voltages of Q_{13} and Q_{14}, represented as diodes in Fig. 16.65(b). The 40-kΩ resistor is used to increase the value of I_{C13}. Without this resistor, I_{C13} would only be equal to the base current of Q_{14}. The short-circuit protection circuitry in Fig. 16.53 is not shown in Fig. 16.65 in order to simplify the diagram.

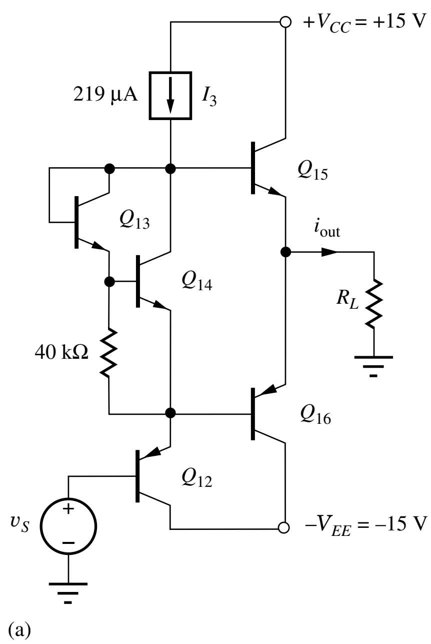


Figure 16.65 (a) 741 output stage without short-circuit protection. (b) Simplified output stage.

The input and output resistances of the class-AB output stage are actually complicated functions of the signal voltage because the operating current in Q_{15} and Q_{16} changes greatly as the output voltage changes. However, because only one transistor conducts strongly at any given time in the class-AB stage, separate circuit models can be used for positive and negative output signals. The model for positive signal voltages is shown in Fig. 16.66. (The model for negative signal swings is similar except *npn* transistor Q_{15} is replaced by *pnp* transistor Q_{16} connected to the emitter of Q_{12}.)

Let us first determine the input resistance of transistor Q_{12}. If R_{in12} is much larger than the 89-kΩ output resistance of the two-port in Fig. 16.66, then it does not significantly affect the overall voltage gain of the amplifier. Using single-stage amplifier theory,

$$R_{in12} = r_{\pi 12} + (\beta_{o12} + 1)R_{eq1} \tag{16.154}$$

where

$$R_{eq1} = r_{d14} + r_{d13} + R_3 \| R_{eq2} \tag{16.155}$$

and

$$R_{eq2} = r_{\pi 15} + (\beta_{o15} + 1)R_L \cong (\beta_{o15} + 1)R_L \tag{16.156}$$

The value of R_3 (344 kΩ) was calculated in the bias circuit section. For $I_{C12} = 216$ μA, and assuming a representative collector current in Q_{15} of 2 mA,

$$R_{eq2} = r_{\pi 15} + (\beta_{o15} + 1)R_L = \frac{3.75\text{ V}}{2\text{ mA}} + (151)2\text{ k}\Omega = 304\text{ k}\Omega \tag{16.157}$$

Note that the value of R_{eq2} is dominated by the reflected load resistance $\beta_{o15}R_L$. Resistor $r_{\pi 15}$ represents a small part of R_{eq2}, and knowing the exact value of I_{C15} is not critical.

$$R_{eq1} = r_{d14} + r_{d13} + R_3 \| R_{eq2} = 2\frac{0.025\text{ V}}{0.216\text{ mA}} + 344\text{ k}\Omega \| 304\text{ k}\Omega = 162\text{ k}\Omega \tag{16.158}$$

and

$$R_{in12} = r_{\pi 12} + (\beta_{o12} + 1)R_{eq1} = \frac{1.25\text{ V}}{0.216\text{ mA}} + (51)162\text{ k}\Omega = 8.27\text{ M}\Omega \tag{16.159}$$

Because R_{in12} is approximately 100 times the output resistance (y_{22}^{-1}) of the second stage, R_{in12} has little effect on the gain of the second stage. Although the value of R_{in12} changes for different values of load resistance, the overall op amp gain is not affected because the value of R_{in12} is so much larger than the value of y_{22}^{-1} in Fig. 16.66.

Similar results are obtained for negative signal voltages. The values are slightly different because the current gain of the *pnp* transistor Q_{16} differs from that of the *npn* transistor Q_{15}.

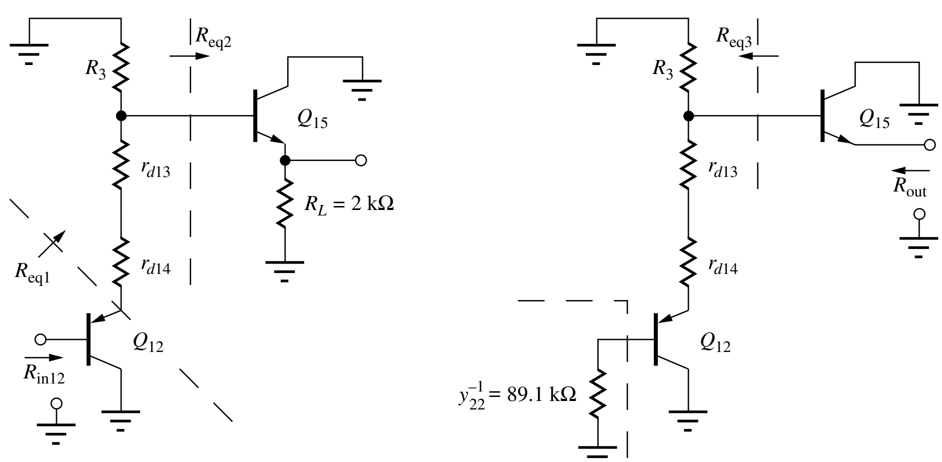


Figure 16.66 Circuits for determining input and output resistance of the output stage.

16.8.6 Output Resistance

The output resistance of the amplifier for positive output voltages is determined by transistor Q_{15}

$$R_o = \frac{r_{\pi 15} + R_{\text{eq3}}}{\beta_{o15} + 1} \tag{16.160}$$

in which

$$\begin{aligned} R_{\text{eq3}} &= R_3 \left\| \left[r_{d13} + r_{d14} + \frac{r_{\pi 12} + y_{22}^{-1}}{\beta_{o12} + 1} \right] \right. \\ &= 304\ \text{k}\Omega \left\| \left[2\frac{0.025\ \text{V}}{0.219\ \text{mA}} + \frac{5.71\ \text{k}\Omega + 89.1\ \text{k}\Omega}{51} \right] \right. = 2.08\ \text{k}\Omega \end{aligned} \tag{16.161}$$

Substituting the values from Eq. (16.161) into Eq. (16.160) yields

$$R_o = \frac{1.88\ \text{k}\Omega + 2.08\ \text{k}\Omega}{151} = 26.2\ \Omega \tag{16.162}$$

From Fig. 16.56, we can see that the 27-Ω resistor R_7, which determines the short-circuit current limit, adds directly to the overall output resistance of the amplifier so that actual op-amp output resistance is

$$R_{\text{out}} = R_o + R_7 = 53\Omega \tag{16.163}$$

EXERCISE: Repeat the calculation of R_{in12} and R_{out} if *pnp* transistor Q_{16} has a current gain of 50, $I_{C16} = 2$ mA, and $I_{C15} = 0$. Be sure to draw the new equivalent circuit of the output stage for negative output voltages.

ANSWERS: 3.94 MΩ ($\gg$ 89.1 kΩ), 53 Ω + 22 Ω = 75 Ω

16.8.7 Short Circuit Protection

For simplicity, the output short-circuit protection circuitry was not shown in Fig. 16.65. Referring back to the complete op amp schematic in Fig. 16.53, we see that **short-circuit protection** is provided by resistors R_7 and R_8 and transistors Q_{17} and Q_{18}. The circuit is identical to the one presented in the previous chapter in Fig. 15.60(a). Transistors Q_{17} and Q_{18} are normally off, but if the current in resistor R_7 becomes too high, then transistor Q_{17} turns on and steals the base current from Q_{15}. Likewise, if the current in resistor R_8 becomes too large, then transistor Q_{18} turns on and removes the base current from Q_{16}. The positive and negative short-circuit current levels will be limited to approximately V_{BE17}/R_7 and $-V_{EB18}/R_8$, respectively. As already mentioned, resistors R_7 and R_8 increase the output resistance of the amplifier since they appear directly in series with the output terminal.

EXERCISE: Estimate the positive and negative short-circuit output current in the 741 op amp in Fig. 16.53.

ANSWERS: 26 mA; −32 mA

16.8.8 Summary of the μA741 Operational Amplifier Characteristics

Table 16.4 is a summary of the characteristics of the μA741 operational amplifier. Column 2 gives our calculated values; column 3 presents values typically found in the actual commercial product. The observed values depend on the exact values of current gain and Early voltage of the *npn* and *pnp* transistors and vary from process run to process run.

TABLE 16.4
μA741 Characteristics

	CALCULATION	TYPICAL VALUES
Voltage gain	153,000	200,000
Input resistance	2.05 MΩ	2 MΩ
Output resistance	53 Ω	75 Ω
Input bias current	49 nA	80 nA
Input offset voltage	—	2 mV

16.9 THE GILBERT ANALOG MULTIPLIER

In Chapter 11 we saw how operational amplifiers could be used to perform scaling, addition, subtraction, integration, and differentiation of electronic signals. However, one of the more difficult operations to realize is accurate multiplication of two analog signals. Barrie Gilbert, another of the "legends" of integrated circuit design, discovered a solution to this problem using the characteristics of the bipolar transistor. The basic multiplier "core" in Fig. 16.67 consists of three differential pairs. The Q_1–Q_2 pair has significant emitter degeneration so that the transconductance of the pair is approximately[6] $1/R_1$. Under this assumption, the collector currents of the lower pair can

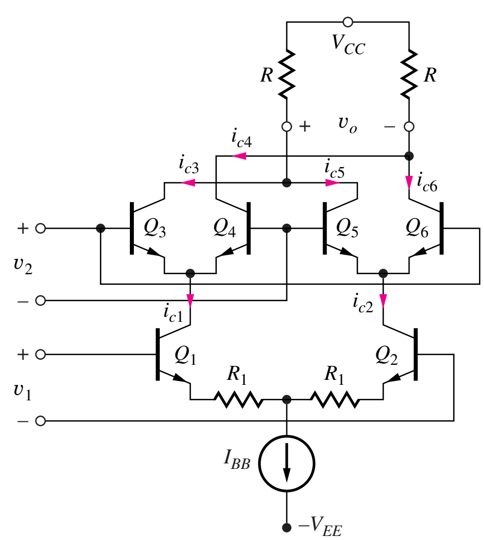


Figure 16.67 Gilbert multiplier core.

[6] More sophisticated voltage-to-current converters (transconductance amplifiers) can also be used.

be written as

$$i_{c1} \cong \frac{I_{BB}}{2} + \frac{v_1}{2R_1} \qquad i_{c2} \cong \frac{I_{BB}}{2} - \frac{v_1}{2R_1} \quad \text{for} \quad |v_1| \leq I_{BB}R_1 \tag{16.164}$$

The bound on v_1 is determined by the requirement that neither collector current can be negative.

Multiplier output current v_o is taken from the upper two differential pairs and can be written as

$$v_o = [(i_{c3} + i_{c5}) - (i_{c4} + i_{c6})]R = [(i_{c3} - i_{c4}) + (i_{c5} - i_{c6})]R \tag{16.165}$$

Using Eq. (15.63), we can write expressions for the collector current differences in this equation:

$$i_{c3} - i_{c4} = i_{c1} \tanh\left(\frac{v_2}{2V_T}\right) \quad \text{and} \quad i_{c5} - i_{c6} = -i_{c2} \tanh\left(\frac{v_2}{2V_T}\right) \tag{16.166}$$

Using these equations, the output voltage can be reduced to

$$v_o = (i_{c1} - i_{c2})R \tanh\left(\frac{v_2}{2V_T}\right) = v_1\left(\frac{R}{R_1}\right)\tanh\left(\frac{v_2}{2V_T}\right) \tag{16.167}$$

At this point, one approach to multiplication is to expand the hyperbolic tangent as a series, and then keep only the first term:

$$\tanh(x) = x - \frac{x^3}{3} + \cdots \quad \text{and} \quad v_o \cong v_1\left(\frac{R}{R_1}\right)\left(\frac{v_2}{2V_T}\right) \quad \text{for} \quad \frac{x^3}{3} \ll x \tag{16.168}$$

where $x = v_2/2V_T$. However, this approach greatly restricts the input signal range of v_2 to only a few tens of mV [see discussion following Eq. (15.64)].

The key to the full range **Gilbert multiplier** is to use another pair of *pn* junctions to "pre-distort" the input signal as in Fig. 16.68. Diode connected transistors Q_9 and Q_{10} are driven by a second transconductance stage formed by Q_7 and Q_8 for which

$$i_{c7} \cong \frac{I_{EE}}{2} + \frac{v_3}{2R_3} \qquad i_{c8} \cong \frac{I_{EE}}{2} - \frac{v_3}{2R_3} \quad \text{for} \quad |v_3| \leq I_{EE}R_3 \tag{16.169}$$

to develop voltage v_2:

$$v_2 = (V_{BB} - v_{BE10}) - (V_{BB} - v_{BE9}) = v_{BE9} - v_{BE10} \tag{16.170}$$

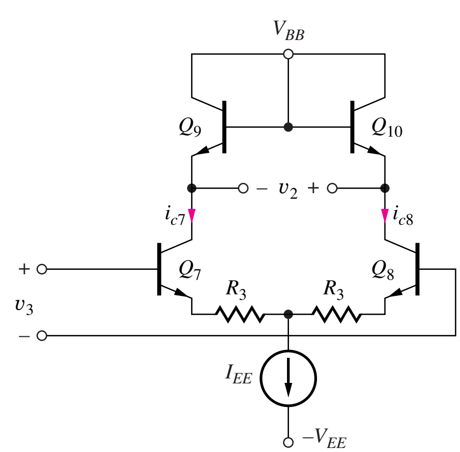


Figure 16.68 Inverse hyperbolic tangent "predistortion" circuit.

Using the standard expressions for the base-emitter voltages and assuming the two transistors are matched gives

$$v_2 = V_T \ln\left(\frac{\dfrac{I_{EE}}{2} + \dfrac{v_3}{2R_3}}{I_S}\right) - V_T \ln\left(\frac{\dfrac{I_{EE}}{2} - \dfrac{v_3}{2R_3}}{I_S}\right) = V_T \ln\left(\frac{1 + \dfrac{v_3}{I_{EE}R_3}}{1 - \dfrac{v_3}{I_{EE}R_3}}\right) \tag{16.171}$$

Searching our math tables, we might stumble on this identity:

$$\ln\left(\frac{1+x}{1-x}\right) = 2\tanh^{-1}(x)$$

which can be used to rewrite the expression for v_2 as

$$v_2 = 2V_T \tanh^{-1}\left(\frac{v_3}{I_{EE}R_3}\right) \tag{16.172}$$

Combining Eq. (16.172) with (16.167) gives the final result for the analog multiplier

$$v_o = \left(\frac{R}{I_{EE}R_1R_3}\right) v_1 v_3 \tag{16.173}$$

The circuit described by Eq. (16.173) is known as a **four-quadrant multiplier** since both input voltages are permitted to take on both positive and negative values. One common design sets the scaling constant to be 0.1 so that the input and output signals can all have a 10-V range.

An example of operation of an analog multiplier appears in Fig. 16.69. Input $v_3 = 5\sin 20000\pi t$ V. Signal v_1 is a ramp starting at -5 V at $t = 0$ and reaching $+5$ V at $t = 2$ ms. The product of the two waveforms appears in the figure. The product is zero and changes sign as v_1 crosses through 0 V at $t = 1$ ms.

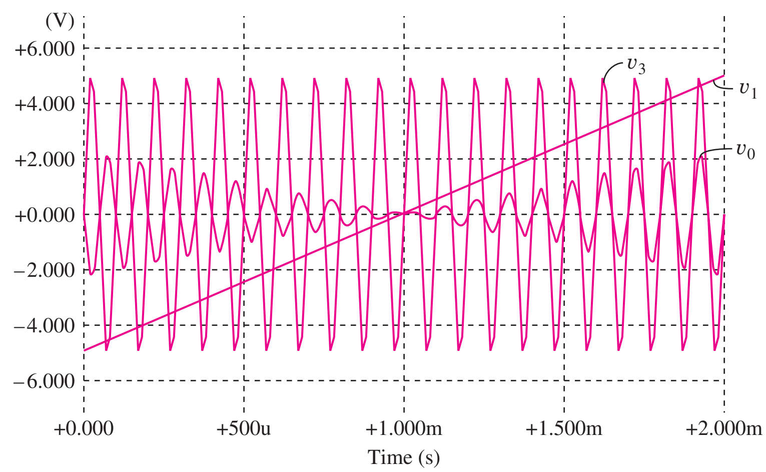


Figure 16.69 Gilbert multiplier simulation results for $v_3 = 5\sin 20000\pi t$ and v_1 ramping between -5 and $+5$ V with a scale factor of 0.1.

EXERCISE: What should the scale factor be in Eq. (16.173) if all voltages are to have a 5-V range? A 1-V range?

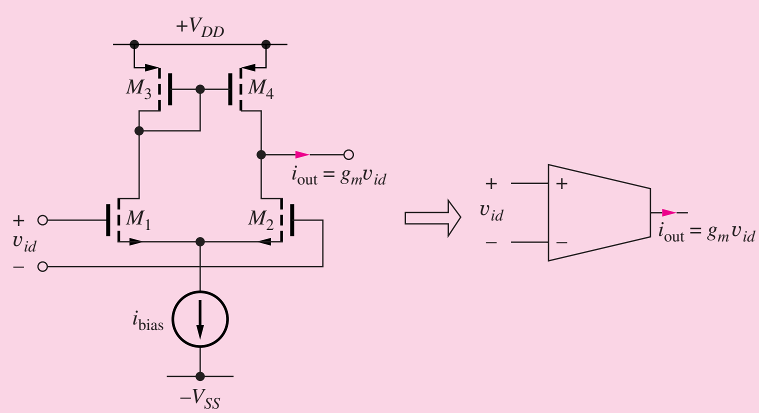
ANSWERS: 0.2; 1.0

EXERCISE: Simulate the full Gilbert multiplier with a 5-V, 1-kHz sine wave for v_1 with $v_3 = 5 \sin 20000\pi t$ V.

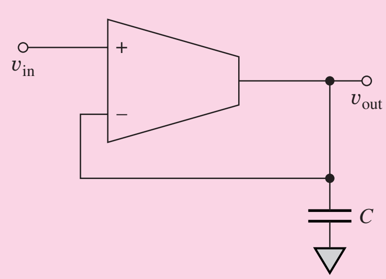
ELECTRONICS IN ACTION

G_m-C Integrated Filters

The design of integrated circuit filters is complicated by the lack of well-controlled resistive components in most mainstream CMOS processes. One approach to overcome this is the use of G_m-C filter topologies based on the operational transconductance amplifier (OTA). The OTA is characterized by both a high input and high output impedance. A simple form of an OTA is shown below. The high impedance output is a small-signal current given by the product of the differential pair g_m and the differential input voltage v_{id}. Typically, commercial OTA designs include additional devices to improve output resistance and voltage swing.



Equivalent schematic symbol for operational transconductance amplifier (OTA).



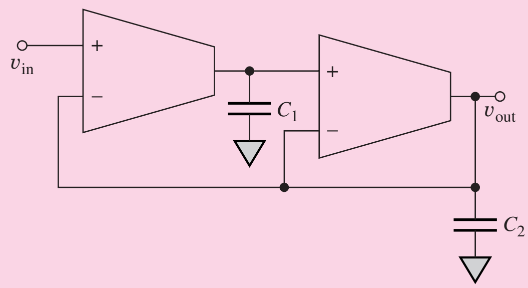
$$\mathbf{V}_{out} = \frac{\mathbf{I}_{out}}{sC} = (\mathbf{V}_{out} - \mathbf{V}_{in})\frac{g_m}{sC}$$

$$A_v(s) = \frac{\mathbf{V}_{out}(s)}{\mathbf{V}_{in}(s)} = \frac{1}{1 + s\dfrac{C}{g_m}}$$

Single pole g_m-C low-pass filter.

A simple low-pass filter formed with an OTA and a capacitor is shown above. The transfer characteristic is also included and indicates that the upper cutoff frequency occurs at $f_H = g_m/2\pi C$. One of the more useful characteristics of the g_m-C filter approach is the ease with which the characteristics can be tuned. Recalling that g_m is a function of the differential pair current, we see that the cutoff frequency of the filter is easily modified by adjusting the bias current.

A second-order version (a biquad topology) is shown below. This version allows for the adjustment of cutoff frequency with constant Q, and still requires no resistors. High-pass, band-pass, and band-reject are also readily derived from this basic form. Because of their compatibility with standard CMOS processes and excellent power efficiency, g_m-C filters have become prevalent in communication circuits, A/D converter anti-alias filters, noise shaping, and many other applications.



$$\frac{\mathbf{V_{out}}(s)}{\mathbf{V_{in}}(s)} = \frac{g_m^2}{s^2C_1C_2 + sC_1g_m + g_m^2}$$

$$\omega_o = \frac{g_m}{\sqrt{C_1C_2}} \qquad Q = \sqrt{\frac{C_2}{C_1}}$$

Two pole biquadratic g_m-C low-pass filter.

SUMMARY

Integrated circuit (IC) technology permits the realization of large numbers of virtually identical transistors. Although the absolute parameter tolerances of these devices are relatively poor, device characteristics can actually be matched to within less than 1 percent. The availability of large numbers of such closely matched devices has led to the development of special circuit techniques that depend on the similarity of device characteristics for proper operation. These matched circuit design techniques are used throughout analog circuit design and produce high-performance circuits that require very few resistors.

- One of the most important of the IC techniques is the current mirror circuit, in which the output current replicates, or mirrors, the input current. Multiple copies of the replicated current can be generated, and the gain of the current mirror can be controlled by scaling the emitter areas of bipolar transistors or the W/L ratios of FETs. Errors in the mirror ratio of current mirrors are related directly to the finite output resistance and/or current gain of the transistors through the parameters λ, V_A, and β_F.
- In bipolar current mirrors, the finite current gain of the BJT causes an error in the mirror ratio, which the buffered current mirror circuit is designed to minimize. In both FET and BJT circuits, the ideal balance of the current mirror is disturbed by the mismatch in dc voltages between the input and output sections of the mirror. The degree of mismatch is determined by the output resistance of the current sources.

- The figure of merit V_{CS} for the basic current mirror is approximately equal to V_A for the BJT or $1/\lambda$ for the MOS version. However, the value of V_{CS} can be improved by up to two orders of magnitude through the use of either the cascode or Wilson current sources.
- Current mirrors can also be used to generate currents that are independent of the power supply voltages. The V_{BE}-based reference and the Widlar reference produce currents that depend only on the logarithm of the supply voltage. By combining a Widlar source with a current mirror, a reference is realized that exhibits first-order independence of the power supply voltages. The only variation is due to the finite output resistance of the current mirror and Widlar source used in the supply-independent cell. Even this variation can be significantly reduced through the use of cascode and Wilson current mirror circuits within the reference cell. Once generated, the stabilized currents of the reference cell can be replicated using standard current mirror techniques.
- The Widlar cell produces a PTAT voltage (proportional to absolute temperature) which is used as the basic sensing element in most electronic thermometers.
- The bandgap reference combines a PTAT cell with a base-emitter voltage to produce a highly precise output voltage that is independent of temperature and supply voltage. The typical output voltage of the basic bandgap cell is 1.20 V at room temperature and is approximately equal to the silicon bandgap voltage. The 1.20-V output is easily scaled up to any desired reference voltage.
- An extremely important application of the current mirror is as a replacement for the load resistors in differential and operational amplifiers. This active-load circuit can substantially enhance the voltage gain capability of most amplifiers while maintaining the operating-point balance necessary for low offset voltage and good common-mode rejection. Amplifiers with active loads can achieve single-stage voltage gains that approach the amplification factor of the transistor. Analysis of the ac behavior of circuits employing current mirrors can often be simplified using a two-port model for the mirror.
- Active current mirror loads are used to enhance the performance of both bipolar and MOS operational amplifiers. The classic μA741 operational amplifier, introduced in the late 1960s, was the first highly robust design combining excellent overall amplifier performance with input-stage breakdown-voltage protection and short-circuit protection of the output stage. Active loads are used to achieve a voltage gain in excess of 100 dB in an amplifier with two stages of gain. This operational amplifier design immediately became the industry standard op amp and spawned many similar designs.
- Four-quadrant multiplication of analog signals can be accurately obtained using the Gilbert multiplier circuit.

KEY TERMS

Active load
Buffered current mirror
Cascode current source
Current gain defect
Current mirror
"Diode-connected" transistor
Emitter area scaling
Four-quadrant multiplier
Gilbert multiplier
Matched devices
Matched transistors
μA741
Mirror ratio
Overvoltage protection
Power-supply independent biasing
Reference current
Short-circuit protection
Start-up circuit
V_{BE}-based reference
Voltage reference
Widlar current source
Wilson current source

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PROBLEMS

16.1 Circuit Element Matching

16.1. An integrated circuit resistor has a nominal value of 4.02 kΩ. A given process run has produced resistors with a mean value 15 percent higher than the nominal value, and the resistors are found to be matched within 3 percent. What are the maximum and minimum resistor values that will occur?

16.2. (a) The emitter areas of two bipolar transistors are mismatched by 10 percent. What will be the base-emitter voltage difference between these two transistors when their collector currents are identical? (Assume $V_A = \infty$.) (b) Repeat for a 20 percent area mismatch. (c) What degree of matching is required for a base-emitter voltage difference of less than 1 mV?

16.3. The bipolar transistors in the differential pair in Fig. 15.19(a) are mismatched. (a) What will be the offset voltage if the current gains are mismatched by 5 percent? (b) If the saturation currents are mismatched by 5 percent? (c) If the Early voltages are mismatched by 5 percent? (d) If the collector resistors are mismatched by 5 percent? (Remember, the offset voltage is the input voltage required to force the differential output voltage to be zero.)

16.4. What is the worst-case fractional mismatch $\Delta I_D/I_D$ in drain currents in two MOSFETs if $K_n = 250\ \mu\text{A/V}^2 \pm 5$ percent and $V_{TN} = 1\text{ V} \pm 25\text{ mV}$ for (a) $V_{GS} = 2$ V? (b) $V_{GS} = 4$ V? Assume $I_{D1} = I_D + \Delta I_D/2$ and $I_{D2} = I_D - \Delta I_D/2$.

16.5. (a) A layout design error causes the W/L ratios of the two NMOSFETs in a differential amplifier to differ by 10 percent. What will be the gate-source voltage difference between these two transistors when their drain currents are identical if the nominal value of $(V_{GS} - V_{TN}) = 0.5$ V? (Assume $V_{TN} = 1$ V, $\lambda = 0$ and identical values of K_n'). (b) What degree of matching is required for a gate-source voltage difference of less than 3 mV? (c) For 1 mV?

*16.6. The collector currents of two BJTs are equal when the base-emitter voltages differ by 2 mV. What is the fractional mismatch $\Delta I_S/I_S$ in the saturation current of the two transistors if $I_{S1} = I_S + \Delta I_S/2$ and $I_{S2} = I_S - \Delta I_S/2$? Assume that the collector-emitter voltages and Early voltages are matched. If $\Delta\beta_{FO}/\beta_{FO} = 5$ percent, what are the values of I_{B1} and I_{B2} for the transistors at a Q-point of (100 μA, 10 V)? Assume $\beta_{FO} = 100$ and $V_A = 50$ V.

16.7. The MOS transistors in the differential pair in Fig. 15.20(b) are mismatched. The nominal value of $(V_{GS} - V_{TN}) = 0.75$ V. (a) What will be the offset voltage if the (W/L) ratios are mismatched by 5 percent? (b) If the threshold voltages are mismatched by 5 percent? (c) If the values of λ are mismatched by 5 percent? (d) If the drain resistors are mismatched by 5 percent? (Remember, the offset voltage is the input voltage required to force the differential output voltage to be zero.)

16.2 Current Mirrors

16.8. (a) What are the output currents and output resistances for the current sources in Fig. 16.70 if $I_{REF} = 30\ \mu$A, $K_n' = 25\ \mu\text{A/V}^2$, $V_{TN} = 0.75$ V and $\lambda = 0.015\ \text{V}^{-1}$? (b) What are the currents if

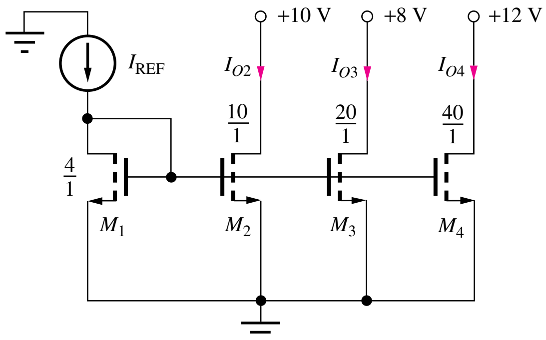

Figure 16.70

I_{REF} is changed to 50 μA? (c) What would be the values if $\lambda = 0$?

16.9. (a) What are the output currents for the circuit in Prob. 16.8 if the W/L ratio of M_1 is changed to 2.5/1? (b) If $I_{REF} = 20$ μA and $(W/L)_1 = 6/1$?

16.10. The current sources in Prob. 16.8 could represent the binary weighted currents needed for a 3-bit D/A converter. (a) What are the ideal values of the three output currents (i.e., $\lambda = 0$)? (b) Express the current errors from Prob. 16.8 in terms of LSBs.

*16.11. What are the output currents and output resistances for the current sources in Fig. 16.71 if $R = 30$ kΩ, $K'_p = 15$ μA/V^2, $V_{TP} = -0.90$ V, and $\lambda = 0.01$ V^{-1}?

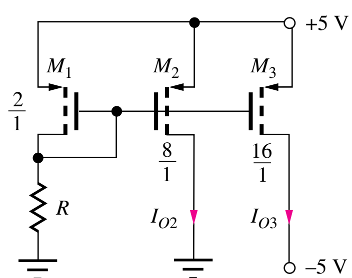

Figure 16.71

16.12. (a) What are the output currents for the circuit in Prob. 16.11 if the W/L ratio of M_1 is changed to 3.3/1? (b) $R = 50$ kΩ and $(W/L)_1 = 4/1$?

16.13. Simulate the current source array in Fig. 16.70 and compare the results to the hand calculations in Prob. 16.8.

16.14. Simulate the current source array in Fig. 16.71 and compare the results to the hand calculations in Prob. 16.11.

16.15. What value of R is required in Fig. 16.71 to have $I_{O2} = 35$ μA? Use device data from Prob. 16.11.

16.16. (a) What are the output currents and output resistances for the current sources in Fig. 16.72(a) if $R = 50$ kΩ, $\beta_{FO} = 50$, and $V_A = 60$ V? (b) Repeat part (a) if the emitter areas of all the transistors are doubled. (c) Repeat for Fig. 16.72(b).

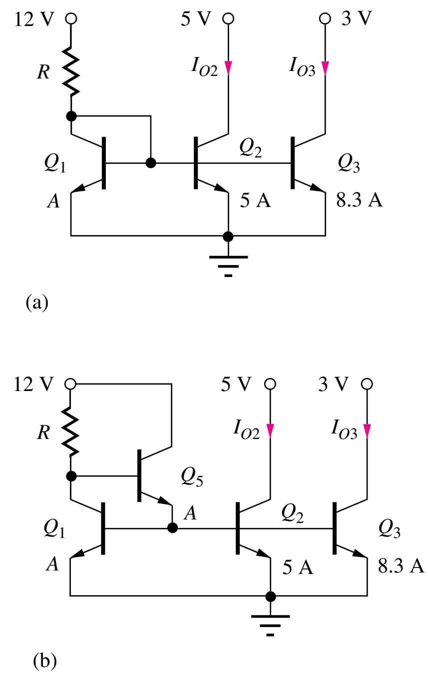

Figure 16.72

16.17. Simulate the current source array in Fig. 16.72(a) and compare the results to the hand calculations in Prob. 16.16. (b) Repeat for Fig. 16.72(b).

16.18. What value of R is required in Fig. 16.72(a) to have $I_{O3} = 166$ μA? What is the value of I_{O2}? Assume $\beta_{FO} = 50$ and $V_A = 60$ V. (b) Repeat for the circuit in Fig. 16.72(b).

16.19. (a) What are the output currents in the circuit in Fig. 16.72(a) if the area of transistor Q_1 is changed to $2A$, and $R = 75$ kΩ? Use $\beta_{FO} = 125$ and $V_A = 75$ V. (b) Repeat for Fig. 16.72(b).

16.20. What are the output currents in the circuit in Fig. 16.72(b) if the area of transistor Q_1 is changed to $3A$, and $R = 100$ kΩ? Use $\beta_{FO} = 100$ and $V_A = 75$ V.

16.21. (a) What are the output currents in the circuit in Fig. 16.72(a) if $R = 140$ kΩ? Use $\beta_{FO} = 125$ and $V_A = 75$ V. (b) What value of R is required to produce the same output currents in Fig. 16.72(b).

16.22. (a) What are the output currents in Fig. 16.72(a) if $R = 100\ \text{k}\Omega$? (b) What are the output currents if the 5-V supply increases to 6 V? (c) What are the output currents if the 12-V supply decreases to 11 V? (d) Show that the change in I_{O2} in part (b) is equal to $g_{o2}\,\Delta V$.

16.23. (a) What are the output currents in Fig. 16.72(b) if $R = 43\ \text{k}\Omega$? (b) What are the output currents if the 5-V supply increases to 6 V? (c) What are the output currents if the 12-V supply decreases to 11 V? (d) Show that the change in I_{O2} in part (b) is equal to $g_{o2}\,\Delta V$.

16.24. What are the output currents and output resistances for the current sources in Fig. 16.73 if $R = 60\ \text{k}\Omega$, $\beta_{FO} = 50$, and $V_A = 60$ V?

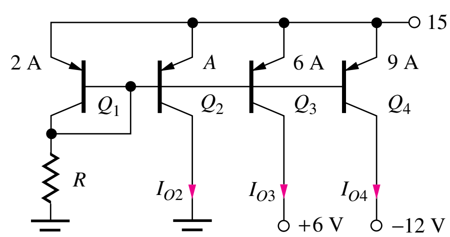

Figure 16.73

16.25. What value of R is required in the circuit in Fig. 16.73 to set $I_{O3} = 50\ \mu\text{A}$? What are the values of I_{O2} and I_{O4}?

*16.26. Draw a buffered current mirror version of the source in Fig. 16.73 and find the value of R required to set $I_{REF} = 25\ \mu\text{A}$ if $\beta_{FO} = 50$ and $V_A = 60$ V. What are the values of the three output currents? What is the collector current of the additional transistor?

16.27. In Fig. 16.74, $R_2 = 5R_3$. What value of n is required to set I_{E3} to be equal to exactly $5I_{E2}$?

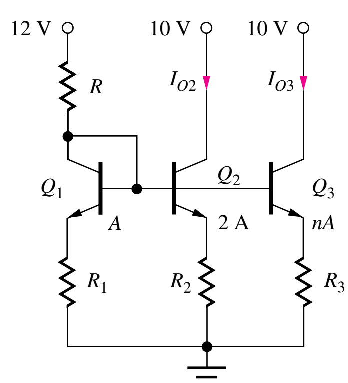

Figure 16.74

*16.28. What are the output currents and output resistances for the current sources in Fig. 16.74 if $R = 10\ \text{k}\Omega$, $R_1 = 10\ \text{k}\Omega$, $R_2 = 5\ \text{k}\Omega$, $R_3 = 2.5\ \text{k}\Omega$, $n = 4$, $\beta_{FO} = 75$, and $V_A = 60$ V?

*16.29. What values of n and R_3 would be required in Prob. 16.28 so that $I_{O2} = 3I_{O3}$?

16.30. Repeat Prob. 16.28 if the area of transistor Q_1 is changed to 0.5 A and R_1 is changed to $20\ \text{k}\Omega$?

16.31. What are the output current I_O and output resistance in the circuit in Fig. 16.75 if $-V_{EE} = -5$ V, $n = 7.2$, $K_n = 50\ \mu\text{A/V}^2$, $V_{TN} = 0.75$ V, $I_{REF} = 15\ \mu\text{A}$, $\beta_{FO} = 100$, and $V_A = 75$ V?

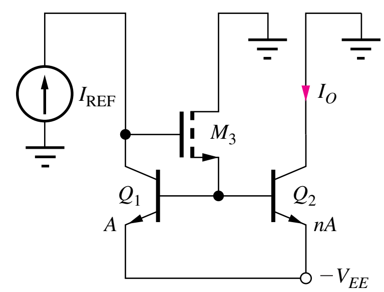

Figure 16.75

16.32. Use SPICE to simulate the circuit in Prob. 16.31 and compare the results to hand calculations.

16.33. (a) What is the input resistance presented to source I_{REF} at the gate of transistor M_3 in Fig. 16.75 if $n = 1$? Use the other parameters from Prob. 16.31? (b) Use transfer function analysis in SPICE to verify your result.

Widlar Sources

16.34. (a) What are the output current and output resistance for the Widlar current source I_{O2} in Fig. 16.76 if $R = R_2 = 10\ \text{k}\Omega$ and $V_A = 60$ V? (b) For I_{O3} if $R_3 = 5\ \text{k}\Omega$ and $n = 12$?

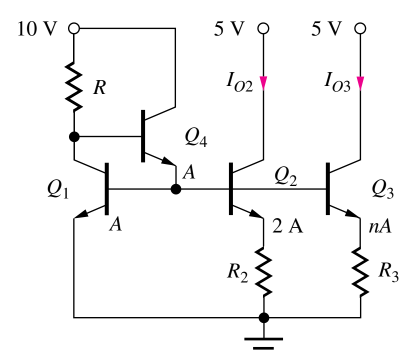

Figure 16.76

16.35. What value of R is required to set $I_{REF} = 75\ \mu A$ in Fig. 16.76? If $I_{REF} = 75\ \mu A$, what value of R_2 is needed to set $I_{O2} = 5\ \mu A$? If $R_3 = 2\ k\Omega$, what value of n is required to set $I_{O3} = 10\ \mu A$?

16.36. Simulate the source of Prob. 16.35 and compare the results to hand calculations.

16.37. (a) What are the output current and output resistance for the Widlar current source I_{O2} in Fig. 16.77 if $R = 40\ k\Omega$ and $R_2 = 5\ k\Omega$? Use $V_A = 70$ V and $\beta_F = 100$. (b) For I_{O3} if $R_3 = 2.5\ k\Omega$ and $n = 20$?

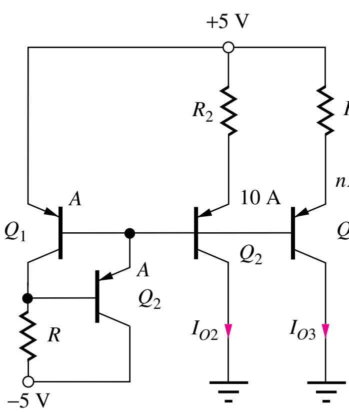

Figure 16.77

16.38. What value of R is required to set $I_{REF} = 50\ \mu A$ in Fig. 16.77. If $I_{REF} = 50\ \mu A$, what value of R_2 is needed to set $I_{O2} = 10\ \mu A$? If $R_3 = 2\ k\Omega$, what value of n is required to set $I_{O3} = 10\ \mu A$?

16.3 High-Output-Resistance Current Mirrors

Wilson Sources

16.39. $I_{REF} = 50\ \mu A$, $-V_{EE} = -5$ V, $\beta_{FO} = 125$, and $V_A = 40$ V in the Wilson source in Fig. 16.78. (a) What are the output current and output resistance for $n = 1$? (b) For $n = 3$? (c) What is the value of V_{CS} for the current source in (b)? (d) What is the minimum value of V_{EE}?

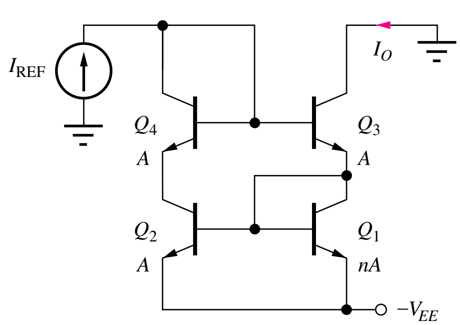

Figure 16.78

*16.40. Derive an expression for the output resistance of the Wilson source in Fig. 16.78 as a function of the area ratio n.

**16.41. Derive an expression for the output resistance of the BJT Wilson source in Fig. 16.21 and show that it can be reduced to Eq. (16.46). What assumptions were used in this simplification?

16.42. What is the minimum voltage that can be applied to the collector of Q_3 in Fig. 16.78 and have the transistor remain in the active region if $I_{REF} = 15\ \mu A$, $n = 5$, $\beta_{FO} = 125$, and $I_{SO} = 3$ fA? Calculate an exact value based on the value of I_{SO}.

16.43. $R = 30\ k\Omega$ in the Wilson source in Fig. 16.79. (a) What is the output current if $(W/L)_1 = 5/1$, $(W/L)_2 = 20/1$, $(W/L)_3 = 20/1$, $K_n' = 25\ \mu A/V^2$, $V_{TN} = 0.75$ V, $\lambda = 0\ V^{-1}$, and $V_{SS} = -5$ V. What value of $(W/L)_4$ is required to balance the drain voltages of M_1 and M_2? (*b) Repeat if $\lambda = 0.015\ V^{-1}$. (c) Check your results in (b) with SPICE simulation.

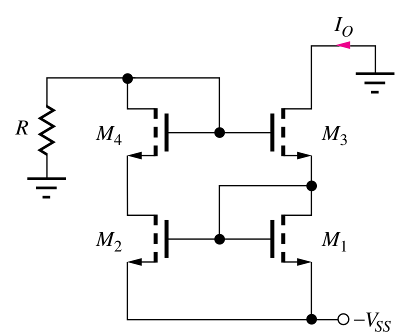

Figure 16.79

*16.44. Derive an expression for the output resistance of the Wilson source in Fig. 16.79 as a function of $(W/L)_1$, $(W/L)_2$, $(W/L)_3$, $(W/L)_4$, and the reference current I_{REF}. Assume $R = \infty$.

16.45. Derive an expression for the equivalent resistance presented to I_{REF} in the Wilson source in Fig. 16.19.

16.46. Derive an expression for the equivalent resistance presented to I_{REF} in the Wilson source in Fig. 16.20.

16.47. What is the minimum voltage required on the drain of M_3 to maintain it in pinch-off in the circuit in Fig. 16.79 if $I_{REF} = 150\ \mu A$, $(W/L)_1 = 5/1$, $(W/L)_2 = 20/1$, $(W/L)_3 = 20/1$, $K_n' =$

$25\ \mu A/V^2$, $V_{TN} = 0.75$ V, $\lambda = 0\ V^{-1}$, and $-V_{SS} = -10$ V?

16.48. In Fig. 16.79, $(W/L)_3 = 5/1$, $(W/L)_4 = 5/1$, and $I_{REF} = 50\ \mu A$. What value of $(W/L)_2$ is required for $R_{out} = 250\ M\Omega$ if $K_n' = 25\ \mu A/V^2$, $V_{TN} = 0.75$ V, $\lambda = 0.0125\ V^{-1}$. Assume $(W/L)_2 = (W/L)_1$, $R = \infty$, and $V_{SS} = 5$ V. Neglect V_{DS}.

**16.49. Redraw the equivalent circuit used to calculate the output resistance of the MOS Wilson source in Figs. 16.21 and 16.22 including a finite output resistance R_{REF} for the reference source. Based on this circuit, how large must R_{REF} be to keep from degrading the output resistance of the Wilson source? What type of current source could be used to implement I_{REF} to meet this requirement?

Cascode Current Sources

16.50. (a) What are the output current and output resistance for the cascode current source in Fig. 16.80 if $I_{REF} = 17.5\ \mu A$, $V_{DD} = 5$ V, $K_n = 75\ \mu A/V^2$, $V_{TN} = 0.75$ V, and $\lambda = 0.0125\ V^{-1}$. (b) What is the value of V_{CS} for this current source? (c) What is the minimum value of V_{DD}?

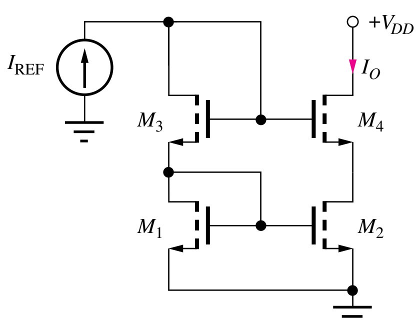

Figure 16.80

16.51. Use SPICE to simulate the current source in Prob. 16.50 and compare the results to your calculations.

16.52. (a) A layout error causes the W/L ratio of M_2 to be 5 percent larger than that of M_1 in Prob. 16.50. What is the error in the output current I_O? (a) Repeat if $M_1 = M_2$, but M_4 is 5 percent larger than that of M_3.

16.53. (a) Repeat Prob. 16.50 for $I_{REF} = 25\ \mu A$. (b) Repeat Prob. 16.50 for $I_{REF} = 50\ \mu A$.

16.54. What is the equivalent resistance presented to I_{REF} in the cascode current source in Prob. 16.50?

16.55. (a) What are the output current and output resistance for the cascode current source in Fig. 16.81 if $I_{REF} = 17.5\ \mu A$, $\beta_{FO} = 110$, and $V_A = 50$ V? (b) What is the value of V_{CS} for this current source? (c) What is the minimum value of V_{CC}?

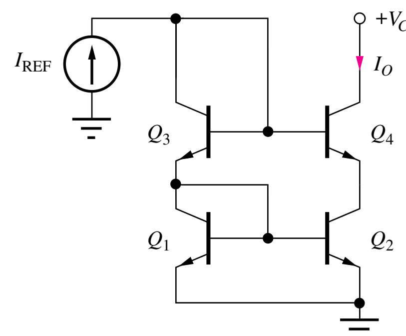

Figure 16.81

16.56. Simulate the current source in Prob. 16.81 and compare the results to hand calculations.

16.57. In Fig. 16.80, $(W/L)_1 = 5/1$, $(W/L)_2 = 5/1$, $(W/L)_3 = 5/1$, and $I_{REF} = 50\ \mu A$. What value of $(W/L)_4$ is required for $R_{out} = 250\ M\Omega$ if $K_n' = 25\ \mu A/V^2$, $V_{TN} = 0.75$ V, and $\lambda = 0.0125\ V^{-1}$?

16.58. What is the equivalent resistance presented to I_{REF} in the cascode current source in Prob. 16.55?

16.4 Reference Current Generation

16.59. What are the output current and output resistance for the Widlar source in Fig. 16.82 if $I_{REF} = 80\ \mu A$ and $R_2 = 500\ \Omega$? (b) What is the new value of the output current if a layout error causes the area of Q_2 to be 5 percent larger than desired? (c) What are the new values or output current and resistance if the emitter area of Q_2 is reduced to $14A$?

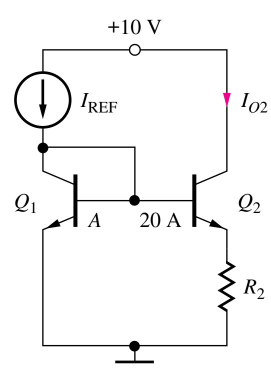

Figure 16.82

16.60. What are the output current and output resistance for the Widlar source in Fig. 16.82 if $I_{REF} = 35\ \mu A$ and $R_2 = 935\ \Omega$? (b) What are the new values if the emitter area of Q_1 is increased to $2A$?

16.61. $I_{REF} = 73\ \mu A$ in Fig. 16.82. (a) What value of R_2 is required to set $I_{O2} = 22\ \mu A$? (b) To set $I_{O2} = 5.7\ \mu A$? (c) To set $I_{O2} = 5.7\ \mu A$ if the area of Q_2 is changed to $10A$?

16.62. $I_{REF} = 62\ \mu A$ in Fig. 16.82. (a) What value of R_2 is required to set $I_{O2} = 12\ \mu A$ if the area Q_1 is changed to $2A$? (b) If the area of Q_2 is changed to $10A$?

16.63. Plot the variation of the output current vs. I_{REF} for the Widlar source in Fig. 16.82 for $50\ \mu A \le I_{REF} \le 5$ mA if $R_2 = 4\ k\Omega$ and $\beta_{FO} = 100$.

16.64. (a) Find the PTAT voltage across R_2 in Fig. 16.84 if $T = 300$ K, $I_{REF} = 75\ \mu A$, and $R_2 = 2\ k\Omega$? (b) What is the temperature coefficient of the PTAT voltage? (c) If R_2 has a temperature coefficient of 1500 ppm/°C, what is the temperature coefficient of the collector current of Q_2 at 300 K?

16.65. (a) What is the output current of the V_{BE}-based reference in Fig. 16.83(a) if $I_S = 10^{-15}$ A, $\beta_F = \infty$, $R_1 = 10\ k\Omega$, $R_2 = 2.2\ k\Omega$, and $V_{EE} = 15$ V? (b) For $V_{EE} = 3.3$ V? (c) What is the output current of the V_{BE}-based reference in Fig. 16.83(b) if $R_1 = 10\ k\Omega$, $R_2 = 10\ k\Omega$, and $V_{CC} = 5$ V?

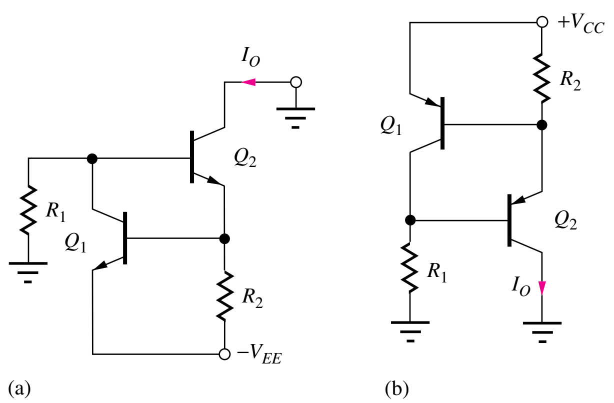

Figure 16.83

16.66. (a) Design the reference in Fig. 16.83(a) to produce an output current $I_O = 30\ \mu A$. Assume $-V_{EE} = -3.3$ V and $I_S = 0.1$ fA and $\beta_{FO} = 130$ for both transistors. (b) Repeat for the circuit in Fig. 16.83(b) if $V_{CC} = 3.3$ V.

*16.67. Derive an expression for the output resistance of the cascode current source in Fig. 16.25.

*16.68. What is the output current of the NMOS reference in Fig. 16.84 if $R_1 = 10\ k\Omega$, $R_2 = 15\ k\Omega$, $K_n = 250\ \mu A/V^2$, $V_{TN} = 0.75$ V, $\lambda = 0.017\ V^{-1}$, and $V_{DD} = 10$ V?

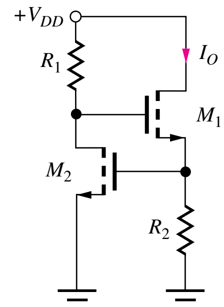

Figure 16.84

16.69. Design the reference in Fig. 16.84 to produce an output current $I_O = 75\ \mu A$. Assume $V_{DD} = 6$ V and use the transistor parameters from Prob. 16.68.

*16.70. What is the output current of the PMOS reference in Fig. 16.85 if $R_1 = 10\ k\Omega$, $R_2 = 18\ k\Omega$, $K_p = 100\ \mu A/V^2$, $V_{TP} = -0.75$ V, $\lambda = 0.02\ V^{-1}$, and $V_{DD} = 5$ V?

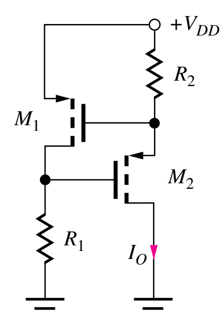

Figure 16.85

16.71. Design the reference in Fig. 16.85 to produce an output current $I_O = 125\ \mu A$. Assume $V_{DD} = 9$ V and use the transistor parameters from Prob. 16.70.

16.72. What are the collector currents in Q_1 and Q_2 in the reference in Fig. 16.86 if $V_{CC} = V_{EE} = 1.5$ V, $n = 20$, and $R = 2.2\ k\Omega$? Assume $\beta_{FO} = \infty$ and $V_A = \infty$.

16.73. Simulate the reference in Fig. 16.86 using SPICE, assuming $\beta_{FO} = 100$ and $V_A = 50$ V. Compare the currents to hand calculations and discuss the source of any discrepancies. Use SPICE to determine the sensitivity of the reference currents to power supply voltage changes.

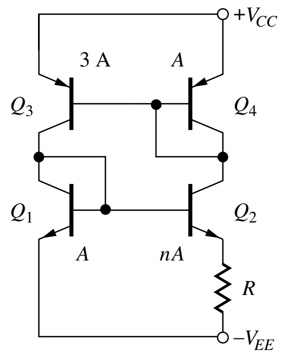

Figure 16.86

16.74. What are the collector currents in the four transistors in Fig. 16.86 if $V_{CC} = V_{EE} = 3.3$ V, $n = 8$, and $R = 4$ kΩ?

16.75. What is the smallest value of n required for the circuit in Fig. 16.86 to operate properly based on Eq. 16.32 (i.e., $V_{\text{PTAT}} > 0$)?

16.76. (a) What value of R is required to set $I_{C2} = 35$ μA in Fig. 16.86 if $n = 5$ and $T = 50$°C? (b) For $n = 10$ and $T = 0$°C?

16.77. What are the drain currents in M_1 and M_2 in the reference in Fig. 16.87 if $R = 5.1$ kΩ and $V_{DD} = V_{SS} = 5$ V? Use $K'_n = 25$ μA/V², $V_{TN} = 0.75$ V, $K'_p = 10$ μA/V², and $V_{TP} = -0.75$ V. Assume $\gamma = 0$ and $\lambda = 0$ for both transistor types.

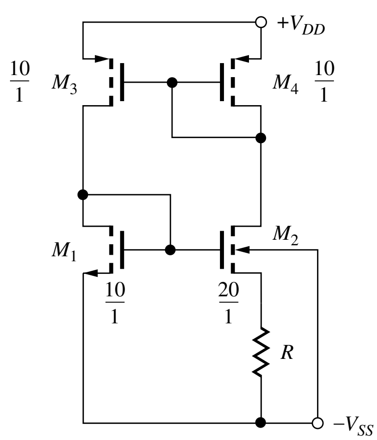

Figure 16.87

16.78. (a) Find the currents in both sides of the reference cell in Fig. 16.87 if $R = 10$ kΩ and $V_{DD} = V_{SS} = 5$ V, using $K'_n = 25$ μA/V², $V_{T\text{on}} = 0.75$ V, $K'_p = 10$ μA/V², $V_{T\text{op}} = -0.75$ V, $\gamma_n = 0$ and $\gamma_p = 0$. Use $2\phi_F = 0.6$ V and $\lambda = 0$ for both transistor types. (b) Repeat for $\gamma_n = 0.5\ \text{V}^{0.5}$ and $\gamma_p = 0.75\ \text{V}^{0.5}$ and compare the results.

16.79. Simulate the references in Prob. 16.78(a) and (b) using SPICE with $\lambda = 0.017\ \text{V}^{-1}$. Compare the currents to hand calculations (with $\gamma = 0$ and $\lambda = 0$) and discuss the source of any discrepancies. Use SPICE to determine the sensitivity of the reference currents to power supply voltage changes.

16.80. What are the collector currents in Q_1 to Q_8 in the reference in Fig. 16.88 if $V_{CC} = 0$ V, $V_{EE} = 3.3$ V, $R = 11$ kΩ, $R_6 = 3$ kΩ, $R_8 = 4$ kΩ, and $A_{E2} = 5$ A, $A_{E3} = 2$ A, $A_{E4} =$ A, $A_{E5} = 2.5$ A, $A_{E6} =$ A, $A_{E7} = 5$ A, and $A_{E8} = 3$ A?

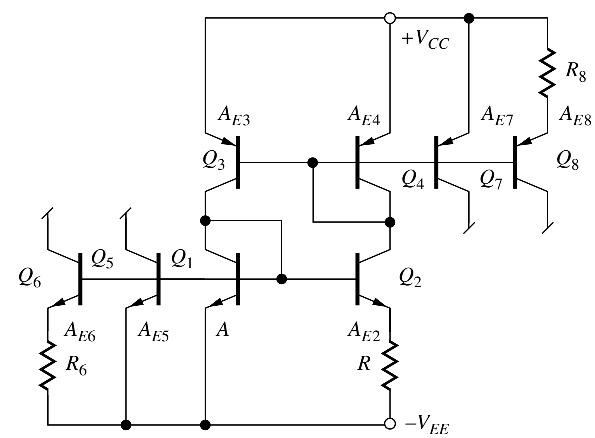

Figure 16.88

16.81. Repeat Prob. 16.80 if $A_{E2} = 10A$ and $A_{E3} = A$.

*16.82. (a) What are the collector currents in Q_1 to Q_7 in the reference in Fig. 16.89 if $V_{CC} = 5$ V and $R = 4300$ Ω? Assume $\beta_F = \infty = V_A$. (b) Repeat part (a) if the emitter areas of transistors Q_5, Q_6, and Q_7 are all changed to $2A$.

*16.83. (a) Simulate the reference in Prob. 16.82 using SPICE. Assume $\beta_{FOn} = 100$, $\beta_{FOp} = 50$, and both Early voltages = 50 V. Compare the currents to hand calculations and discuss the source of any discrepancies. Use SPICE to determine the sensitivity of the reference currents to power supply voltage changes.

16.84. Repeat Prob. 16.82 assuming the emitter area of transistor Q_3 is changed to $2A$.

*16.85. (a) What are the drain currents in M_1 and M_2 in the reference in Fig. 16.90 if $R = 3300$ Ω,

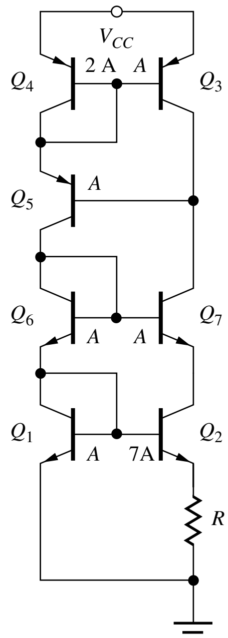

Figure 16.89

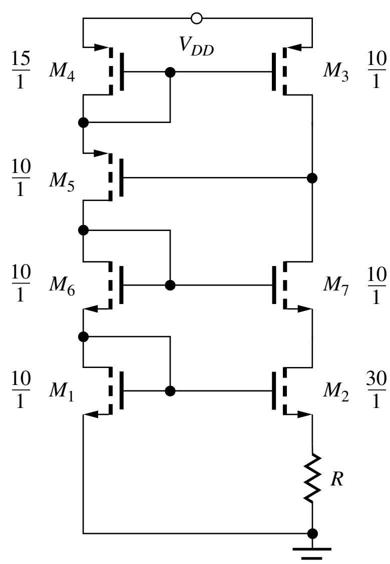

Figure 16.90

$V_{DD} = 15$ V, $K'_n = 25$ μA/V^2, $V_{TN} = 0.75$ V, $K'_p = 10$ μA/V^2, $V_{TP} = -0.75$ V, and $\lambda = 0$ for both transistor types? (b) Repeat part (a) if the W/L ratios of transistors M_5, M_6, and M_7 are all increased to 15/1.

16.86. Simulate the reference in Prob. 16.85 with SPICE using $\lambda = 0.017$ V^{-1} for both transistor types. Compare the currents to those in Prob. 16.85 and discuss the source of any discrepancies. Use SPICE to determine the sensitivity of the reference currents to power supply voltage changes.

16.87. Repeat Prob. 16.85 assuming the W/L ratio of transistor M_3 is changed to 15/1.

16.5 The Bandgap Reference

16.88. A layout error caused $A_{E2} = 9A_{E1}$ in the bandgap reference in Ex. 16.6. What is the new output voltage? What temperature corresponds to zero TC?

16.89. (a) Process variations cause the value of the two collector resistors in the circuit in Ex. 16.6 to increase to 35 kΩ. What is the new value of V_{BG}? What temperature corresponds to zero TC? (b) Repeat for $R = 25$ kΩ.

16.90. What are the bandgap reference output voltage and temperature coefficient of the reference in Ex. 16.6 if I_S changes to 0.5 fA?

16.91. What are the bandgap reference output voltage and the temperature coefficient of the reference in Design Ex. 16.7 at 320 K if I_S changes to 0.3 fA?

16.92. Process variations cause the values of the two collector resistors in the circuit in Design Ex. 16.7 to be mismatched. If $R_1 = 82$ kΩ and $R_2 = 78$ kΩ, what is the new value of V_{BG}? What temperature corresponds to zero TC?

16.93. The bandgap reference in Design Ex. 16.7 was designed to have zero temperature coefficient at 320 K. What will be the temperature coefficient at 280 K? At 320 K?

16.94. Redesign the bandgap reference in Design Ex. 16.7 to use $A_{E2} = 8A_{E1}$.

16.95. Redesign the bandgap reference in Design Ex. 16.7 to produce an output voltage of 7.500 V with zero TC at 10°C. Assume $V_{CC} = 10$ V.

16.6 The Current Mirror as an Active Load

*16.96. What are the values of A_{dd}, A_{cd}, and CMRR for the amplifier in Fig. 16.37 if $I_{SS} = 200$ μA, $R_{SS} = 25$ MΩ, $K_n = K_p = 500$ μA/V^2, $V_{TN} = 1$ V, and $V_{TP} = -1$ V and $\lambda = 0.02$ V^{-1} for both transistors?

16.97. Use SPICE to simulate the amplifier in Prob. 16.96 and compare the results to the hand calculations. Use symmetrical 12-V supplies.

16.98. What are the values of A_{dd}, A_{cd}, and CMRR for the amplifier in Fig. 16.37 if $I_{SS} = 1$ mA, $R_{SS} = 10$ MΩ, $K_n = K_p = 500$ μA/V^2,

$V_{TN} = -V_{TP} = 1$ V, and $\lambda = 0.015$/V for both transistors? What are the minimum power supply voltages if the common-mode input range must be ±5 V? Assume symmetrical supply voltages.

16.99. Use SPICE to simulate the amplifier in Prob. 16.98 and compare the results to hand calculations. Use symmetrical 12-V power supplies.

**16.100. (a) What are A_{dd} and A_{cd} for the bipolar differential amplifier in Fig. 16.43 ($R_L = \infty$) if $\beta_{op} = 70$, $\beta_{on} = 125$, $I_{EE} = 200$ μA, $R_{EE} = 25$ MΩ, and the Early voltages for both transistors are 60 V? What is the CMRR for $v_{C1} = v_{C2}$? (b) What are the minimum power supply voltages if the common-mode input range must be ±1.5 V? Assume symmetrical supply voltages.

16.101. Use SPICE to calculate A_{dd} and A_{cd} for the differential amplifier in Prob. 16.100. Compare the results to hand calculations.

16.102. (a) Repeat Prob. 16.100 if I_{EE} is changed to 50 μA, $R_{EE} = 100$ MΩ, and $V_A = 75$ V. (b) Repeat part (a) for $V_A = 100$ V.

16.103. Use SPICE to simulate the amplifier in Prob. 16.102 and compare the results to hand calculations. Use symmetrical 3-V power supplies.

*16.104. (a) Find the Q-points of the transistors in the CMOS differential amplifier in Fig. 16.91 if $V_{DD} = V_{SS} = 10$ V and $I_{SS} = 200$ μA. Assume $K'_n = 25$ μA/V², $V_{TN} = 0.75$ V, $K'_p = 10$ μA/V², $V_{TP} = -0.75$ V, and $\lambda = 0.017$ V^{-1} for both transistor types. (b) What is the voltage gain A_{dd} of the amplifier? (c) Compare this result to the gain of the amplifier in Fig. 16.37 if the Q-point and W/L ratios of M_1 to M_4 are the same.

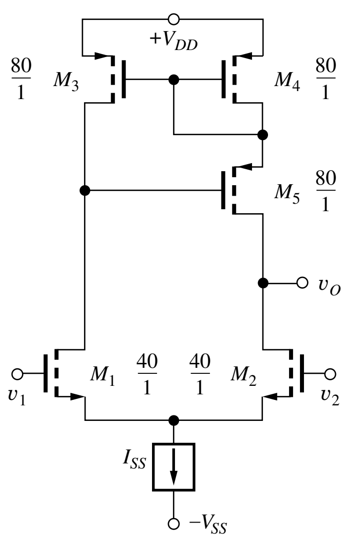

Figure 16.91

16.105. Use SPICE to simulate the amplifier in Prob. 16.104(a,b) and compare the results to hand calculations.

*16.106. Find the Q-points of the transistors in the folded-cascode CMOS differential amplifier in Fig. 16.92 if $V_{DD} = V_{SS} = 5$ V, $I_1 = 250$ μA, $I_2 = 250$ μA, $(W/L) = 40/1$ for all transistors, $K'_n = 25$ μA/V², $V_{TN} = 0.75$ V, $K'_p = 10$ μA/V², $V_{TP} = -0.75$ V, and $\lambda = 0.017$ V^{-1} for both transistor types. Draw the differential-mode half-circuit for transistors M_1 to M_4 and show that the circuit is in fact a cascode amplifier. What is the differential-mode voltage gain of the amplifier?

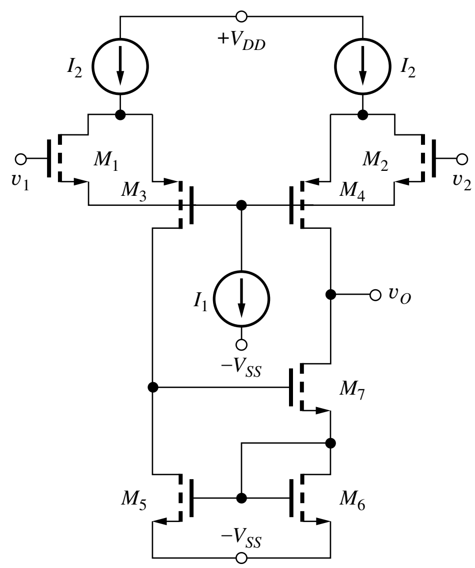

Figure 16.92

16.107. Use SPICE to simulate the amplifier in Prob. 16.106 and determine its voltage gain, output resistance, and CMRR. Compare to hand calculations.

*16.108. Design a current mirror bias network to supply the three currents needed by the amplifier in Prob 16.106.

Output Stages

16.109. What are the currents in Q_3 and Q_4 in the class-AB output stage in Fig. 16.93 if $R_1 = 20$ kΩ, $R_2 = 20$ kΩ, and $I_{S4} = I_{S3} = I_{S2} = 10^{-14}$ A. Assume $\beta_F = \infty$.

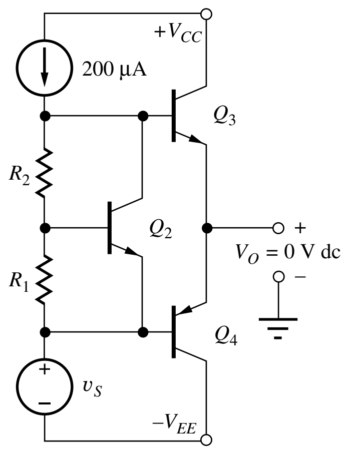

Figure 16.93

*16.110. (a) Show that the currents in Q_3 and Q_4 in the class-AB output stage in Fig. 16.94 are equal to $I_o = I_2\sqrt{(A_{E3}A_{E4})/(A_{E1}A_{E2})}$. (b) What are the currents in Q_3 and Q_4 if $A_{E1} = 3A_{E3}$, $A_{E2} = 3A_{E4}$, $I_2 = 300\ \mu\text{A}$, $I_{SOpnp} = 4$ fA, and $I_{SOnpn} = 10$ fA?

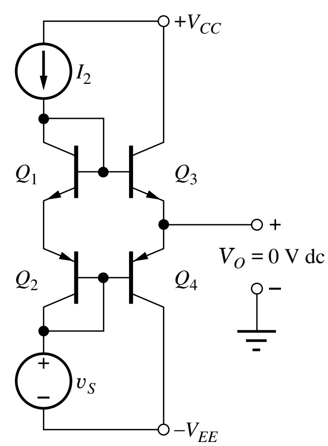

Figure 16.94

16.7 Active Loads in Operational Amplifiers

*16.111. (a) Find the Q-points of the transistors in Fig. 16.95 if $V_{DD} = V_{SS} = 10$ V, $I_{\text{REF}} = 250\ \mu\text{A}$, $K_n' = 25\ \mu\text{A/V}^2$, $V_{TN} = 0.75$ V, $K_p' = 10\ \mu\text{A/V}^2$, and $V_{TP} = -0.75$ V. (b) What is the approximate value of the W/L ratio for M_6 of the CMOS op amp in order for the offset voltage to be zero? What is the differential-mode voltage gain of the op amp if $\lambda = 0.017\ \text{V}^{-1}$ for both transistor types?

*16.112. (a) Simulate the amplifier in Prob. 16.111 and compare its differential-mode voltage gain to the hand

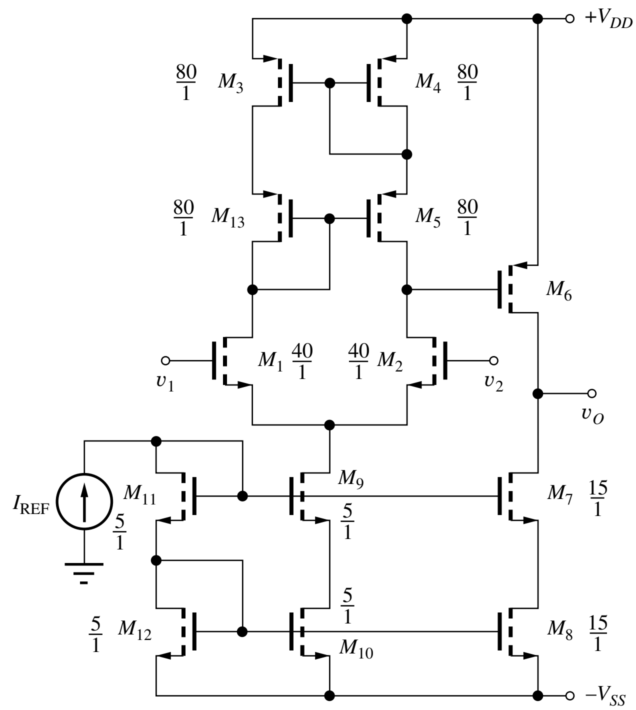

Figure 16.95

calculations in Prob. 16.111. (b) Use SPICE to calculate the offset voltage and CMRR of the amplifier.

*16.113. What is the differential-mode gain of the amplifier in Fig. 16.96 if $V_{DD} = V_{SS} = 10$ V,

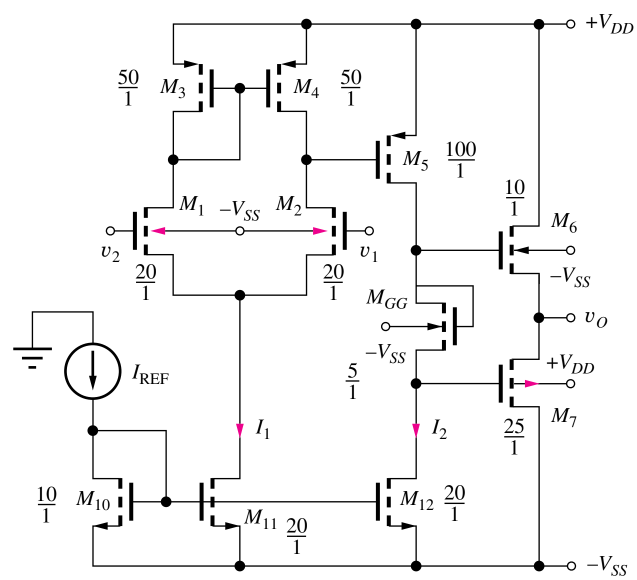

Figure 16.96

$I_{REF} = 100\ \mu A$, $K'_n = 25\ \mu A/V^2$, $V_{TON} = 0.75$ V, $K'_p = 10\ \mu A/V^2$, $V_{TOP} = -0.75$ V, $\gamma_n = 0$, and $\gamma_p = 0$. Use $\lambda = 0.017\ V^{-1}$ for both transistor types.

16.114. (a) Use SPICE to find the Q-points of the transistors of the amplifier in Prob. 16.113. (b) Repeat with $2\phi_F = 0.8$ V, $\gamma_n = 0.60\ V^{0.5}$, and $\gamma_p = 0.75\ V^{0.5}$, and compare the results to (a).

*16.115. Find the Q-points of the transistors in Fig. 16.96 if $V_{DD} = V_{SS} = 7.5$ V, $I_{REF} = 250\ \mu A$, $(W/L)_{12} = 40/1$, $K'_n = 25\ \mu A/V^2$, $V_{TN} = 0.75$ V, $K'_p = 10\ \mu A/V^2$, and $V_{TP} = -0.75$ V. What is the differential-mode voltage gain of the op amp if $\lambda = 0.017\ V^{-1}$ for both transistor types?

*16.116. (a) Estimate the minimum values of V_{DD} and V_{SS} needed for proper operation of the amplifier in Prob. 16.113. Use $K'_n = 25\ \mu A/V^2$, $V_{TN} = 0.75$ V, $K'_p = 10\ \mu A/V^2$, and $V_{TP} = -0.75$ V. (b) What are the minimum values of V_{DD} and V_{SS} needed to have at least a $\pm$5-V common-mode input range in the amplifier?

16.117. (a) Find the Q-points of the transistors in the CMOS op amp in Fig. 16.48 if $V_{DD} = V_{SS} = 5$ V, $I_{REF} = 250\ \mu A$, $K'_n = 25\ \mu A/V^2$, $V_{TN} = 0.75$ V, $K'_p = 10\ \mu A/V^2$, and $V_{TP} = -0.75$ V. (b) What is the voltage gain of the op amp assuming the output stage has unity gain and $\lambda = 0.017\ V^{-1}$ for both transistor types? (c) What is the voltage gain if I_{REF} is changed to 500 μA?

16.118. Based on the example calculations and your knowledge of MOSFET characteristics, what will be the gain of the op amp in Ex. 16.8 if the I_{REF} is set to (a) 250 μA? (b) 20 μA? (*Note:* These should be short calculations.)

16.119. Based on the exercise answers and your knowledge of BJT characteristics, what will be the gain of the op amp in Fig. 16.51 if the I_{REF} is set to (a) 250 μA? (b) 50 μA? (*Note:* These should be short calculations.)

16.120. Draw the amplifier that represents the mirror image of Fig. 16.48 by interchanging NMOS and PMOS transistors. Choose the W/L ratios of the NMOS and PMOS transistors so the voltage gain of the new amplifier is the same as the gain of the amplifier in Fig. 16.48. Maintain the operating currents the same and use the device parameter values from Ex. 16.8.

16.121. Draw the amplifier that represents the mirror image of Fig. 16.50 by interchanging *npn* and *pnp* transistors. If $\beta_{on} = 150$, $\beta_{op} = 60$, and $V_{AN} = V_{AP} = 60$ V, which of the two amplifiers will have the highest voltage gain? Why?

*16.122. What is the approximate emitter area of Q_{16} needed to achieve zero offset voltage in the amplifier in Fig. 16.97 if $I_B = 250\ \mu A$ and $V_{CC} = V_{EE} = 5$ V? What is the value of R_{BB} needed to set the quiescent current in the output stage to 75 μA? What are the voltage gain and input resistance of this amplifier? Assume $\beta_{on} = 150$, $\beta_{op} = 60$, $V_{AN} = V_{AP} = 60$ V, and $I_{SOnpn} = I_{SOpnp} = 15$ fA.

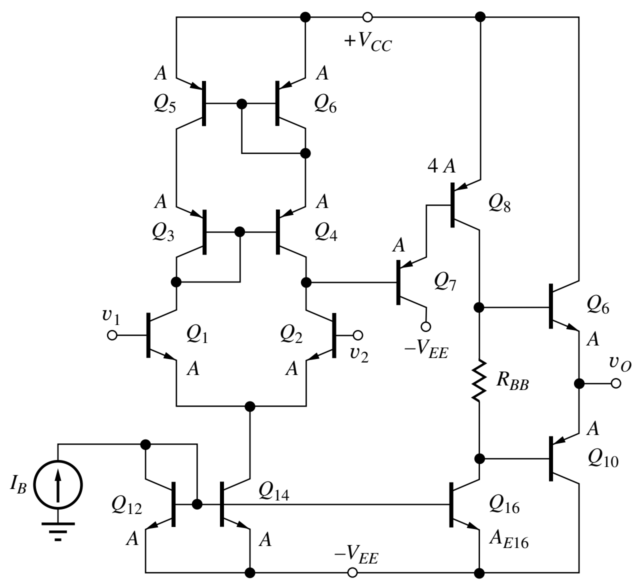

Figure 16.97

16.123. Use SPICE to simulate the characteristics of the amplifier in Prob. 16.122. Determine the offset voltage, voltage gain, input resistance, output resistance, and CMRR of the amplifier.

16.124. (a) What are the minimum values of V_{CC} and V_{EE} needed for proper operation of the amplifier in Fig. 16.97? (b) What are the minimum values of V_{CC} and V_{EE} needed to have at least a $\pm$1-V common-mode input range in the amplifier?

16.125. Find the output voltage of the bandgap reference circuit in Fig. 16.98 if $R_1 = 537\ \Omega$, $R_2 = 2.43$ kΩ, $R_L = 5$ kΩ, and $A_{E1} = 8A_{E2}$. What are the values of the five collector currents? Assume infinite current gains, $V_{CC} = 5$ V, and $I_{S2} = 10^{-16}$ A.

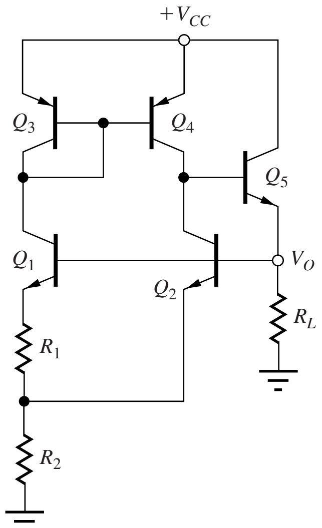

Figure 16.98

16.8 The μA741 Operational Amplifier

16.126. (a) What are the three bias currents in the source in Fig. 16.99 if $R_1 = 100\text{ k}\Omega$, $R_2 = 4\text{ k}\Omega$, and $V_{CC} = V_{EE} = 3$ V. (b) Repeat for $V_{CC} = V_{EE} = 22$ V. (c) Why is it important that I_1 in the μA741 be independent of power supply voltage but it does not matter as much for I_2 and I_3?

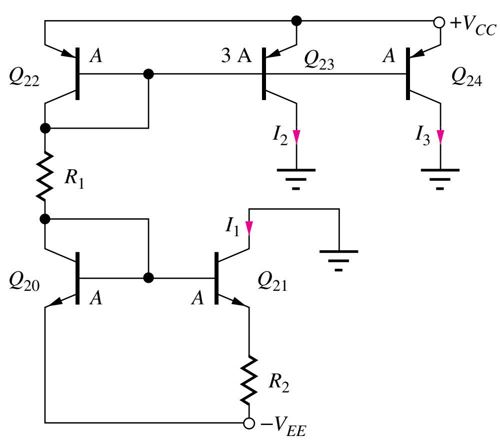

Figure 16.99

16.127. Choose the values of R_1 and R_2 in Fig. 16.99 to set $I_2 = 250$ μA and $I_1 = 50$ μA if $V_{CC} = V_{EE} = 12$ V. What is I_3?

16.128. Choose the values of R_1 and R_2 in Fig. 16.99 to set $I_3 = 300$ μA and $I_1 = 75$ μA if $V_{CC} = V_{EE} = 15$ V. What is I_2?

*16.129. (a) Based on the schematic in Fig. 16.53, what are the minimum values of V_{CC} and V_{EE} needed for proper operation of μA741 amplifier? (b) What are the minimum values of V_{CC} and V_{EE} needed to have at least a ±1-V common-mode input range in the amplifier?

16.130. What are the values of the elements in the Norton equivalent circuit in Fig. 16.60 if I_1 in Fig. 16.53 is increased to 50 μA?

16.131. Suppose Q_{23} in Fig. 16.54 is replaced by a cascode current source. (a) What is the new value of output resistance R_2? (b) What are the new values of the y-parameters of Fig. 16.61? (c) What is the new value of A_{dm} for the op amp?

16.132. Draw a schematic for the cascode current source in Prob. 16.131.

16.133. Create a small-signal SPICE model for the circuit in Fig. 16.61 and verify the values of y_{11}, y_{21}, and y_{22}. What is the value of y_{12}?

**16.134. Figure 16.100 represents an op amp input stage that was developed following the introduction of the μA741. (a) Find the Q-points for all the transistors in the differential amplifier in Fig. 16.100 if $V_{CC} = V_{EE} = 15$ V and $I_{REF} = 100$ μA. (b) Discuss how this bias network operates to establish the Q-points. (c) Label the inverting and noninverting input terminals. (d) What are the transconductance and output resistance of this amplifier? Use $V_A = 60$ V.

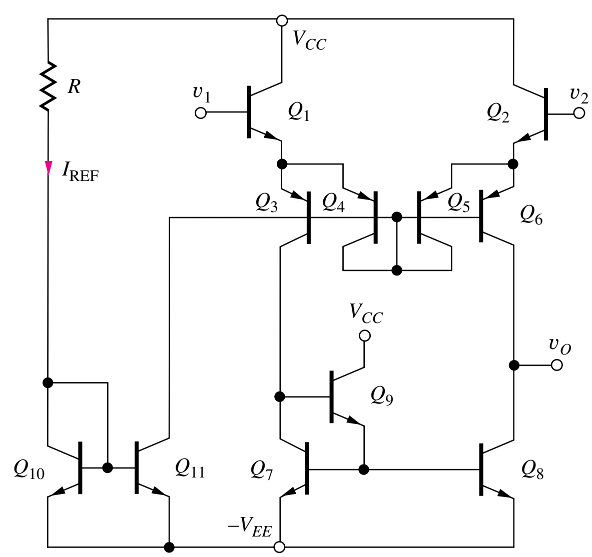

Figure 16.100

**16.135. Figure 16.101 represents an op amp input stage that was developed following the introduction of the μA741. Find the Q-points for all the transistors in the differential amplifier in Fig. 16.97 if $V_{CC} = V_{EE} = 15$ V and $I_{REF} = 100$ μA. (b) Discuss how this bias network operates to establish the Q-points. (c) Label the inverting and noninverting input terminals. (d) What are the transconductance and output resistance of this amplifier? Use $V_A = 60$ V.

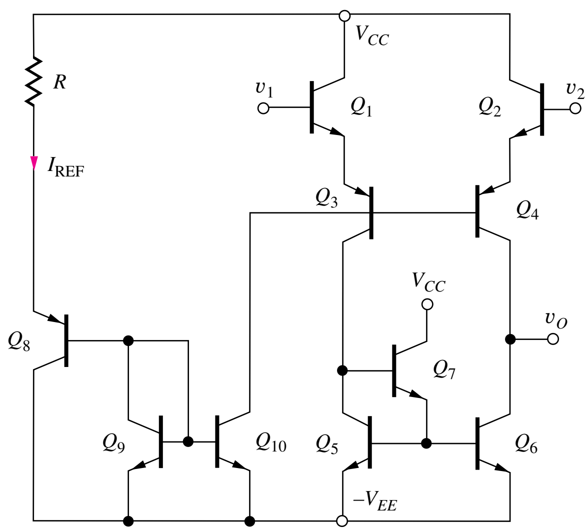

Figure 16.101

16.9 The Gilbert Analog Multiplier

16.136. Find the Q-points of the six transistors in Fig. 16.67 if $V_{CC} = -V_{EE} = 5$ V, $I_{BB} = 100$ μA, $R_1 = 10$ kΩ, and $R = 50$ kΩ. Draw the circuit assuming the bases of Q_1 and Q_2 are biased at a common-mode voltage of −2.5 V with $v_1 = 0$. Assume the bases of Q_3 through Q_6 are biased at a common-mode voltage of 0 V with $v_2 = 0$.

16.137. (a) Find the collector currents of the six transistors in Fig. 16.67 if $V_{CC} = -V_{EE} = 7.5$ V, $I_{BB} = 200$ μA, $R_1 = 10$ kΩ, and $R = 50$ kΩ. Draw the circuit assuming the bases of Q_1 and Q_2 are biased at a common-mode voltage of −3 V with $v_1 = 0.5$ V. Assume the bases of Q_3 through Q_6 are biased at a common-mode voltage of 0 V with $v_2 = 0$. (b) Repeat with $v_2 = 1$ V. (c) Repeat with $v_2 = -1$ V.

16.138. Write an expression for the output voltage for the circuit in Fig. 16.67 if $v_1 = 0.5 \sin 2000\pi t$, and v_2 is generated by the circuit in Fig. 16.68 with $v_3 = 0.5 \sin 10{,}000\pi t$? Assume $V_{CC} = -V_{EE} = 10$ V, $I_{EE} = 500$ μA, $R_1 = R_3 = 2$ kΩ, and $R = 10$ kΩ.

16.139. (a) Write expressions for the total collector currents i_{C1} and i_{C2} in Fig. 16.67 if $I_{BB} = 1$ mA, $R_1 = 2$ kΩ, and $v_1 = 0.4 \sin 5000\pi t$ V. Assume the transistors are operating in the active region. (b) What is the transconductance G_m of the voltage-to-current converter formed by Q_1 and Q_2? $[G_m = \Delta(i_{C1} - i_{C2})/\Delta v_1]$

16.140. Use SPICE to plot the VTC for the circuit in Fig. 16.68 with $V_{BB} = 3$ V, $-V_{EE} = -5$ V, $I_{EE} = 300$ μA, and $R_3 = 3.3$ kΩ.