Study and Design of Low Drop-Out Regulators

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Abstract

The motivation behind the study of low drop-out (LDO) regulators is driven by the increasing demand for higher performance power supply circuits. This paper discusses thoroughly the important issues relevant to the emergence and design of these circuits. An increasing number of low voltage applications require the use of LDOs, i.e., cellular phones, pagers, laptops, etc. Switching regulators, though similar in function, cater to different market demands. The paper further illustrates the design criteria and corresponding analysis relevant to LDOs. This is followed by a discussion on the circuit design considerations under low voltage conditions of the two major components of the regulator in existing process technologies, the pass device and the error amplifier.

I. Introduction

1.1 Definition

A series low-drop-out regulator is a circuit that provides a well-specified and stable dc voltage [1] whose input to output voltage difference is low [2]. The drop-out voltage is defined as the value of the input/output differential voltage where the control loop stops regulating. The term series comes from the fact that a power transistor [pass device] is connected in series between the input and the output terminals of the regulator [3]. The operation of the circuit is based on feeding back an amplified error signal used to control the output current flow of the power transistor driving the load. This type of regulator has two inherent characteristics: (1) the magnitude of the input voltage is greater than the respective output and (2) the output impedance is low so as to yield good performance [2]. Low drop-out (LDO) regulators can be categorized as either low power or high power. Low power LDOs are typically those with a maximum output current of less than 1 A, mostly exhibited by portable applications. On the other hand, high power LDOs can yield currents that are equal to or greater than 1 A to the output, which are commonly demanded by many automotive and industrial applications [4].

1.2 Motivation

The low drop-out nature of the regulator makes it appropriate for use in many applications, namely, automotive, portable, and industrial applications. In the automotive industry, the low drop-out voltage is necessary during cold-crank conditions where the battery voltage can be below 6 V. The increasing demand, however, is readily apparent in mobile battery operated products, such as cellular phones, pagers, camera recorders, and laptops [5]. This portable electronics market requires low voltage and low quiescent current flow for increased battery efficiency and longevity [6]. Low voltage operation is also a consequence of the direction of process technology towards higher packing densities. In particular, isolation barriers decrease as the component densities per unit area are increased thereby manifesting lower breakdown voltages [7, 8]. Consequently, low power and finer lithography drive regulators to operate at low voltages, produce precise output voltages, and require low quiescent current [8]. By the year 2004, the power supply voltage is expected to be as low as 0.9 V in 0.14 μm technologies [8, 9]. Furthermore, minimization of drop-out voltages is necessary to maximize dynamic range within a given power supply voltage. This is because the signal-to-noise ratio decreases as the power supply voltages decrease since noise typically remains constant [10].

Financial considerations also require that these circuits be realized in relatively simple processes, such as standard CMOS, bipolar, and stripped down biCMOS technologies [11].

The alternative to low drop-out regulators are dc-dc converters, switching regulators. Switching regulators are essentially mixed-mode circuits that feed back an analog error signal and digitally gate it to provide bursts of current to the output. The circuit is inherently more complex and costly than LDO realizations [8]. Furthermore, switching regulators can provide a wide range of output voltages that can be less or greater than the input voltage depending on the circuit configuration, buck or boost. The circuit, for the most part, requires a controller with an oscillator, pass elements, inductor, capacitors, and diodes. Some switched-capacitor implementations do not require an inductor [12, 13].

The worst case response time of a dc-dc converter is dependent on the oscillating frequency of the controller (approximately 20 to 200 kHz) and circuit delay. As a result, the corresponding response time is roughly between 6 and 8 μs, whereas the LDO typically requires between 1 and 2 μs [9]. Since the pass elements switch high currents through an inductor at the rate of the oscillator, the output voltage is inherently noisy. This is especially true for boost configurations where RF noise tends to be worse [14]. The high noise present is a consequence of the rectified inductor voltage behavior of the output of these converters. Furthermore, start-stop clock operation (on/off sleep-mode transitions) further aggravates the noise content of the output voltage [9].

On the other hand, switching regulators benefit from having high power efficiency and the ability to generate larger output voltages than the input. They can yield efficiencies between 80 and 95 %. The efficiency of the LDO counterpart is limited by the quiescent current and the input/output voltages, and is expressed as

$$\text{Efficiency}_{\text{Power}} = \frac{I_o V_o}{\left[I_o + I_q\right] V_i} \le \frac{V_o}{V_i}, \qquad (1)$$

where I_o and V_o correspond to the output current and voltage, V_i is the input voltage, and I_q is the quiescent current or ground current. The main power issue in LDO design is battery-life, in other words, the output current flow of the battery. When the load-current is low, which is the normal operating mode for many applications, the quiescent [ground] current becomes an intrinsic factor in determining the lifetime of the battery. Consequently, current efficiency is important during low load-current conditions. Power efficiency, on the other hand, becomes more pertinent during high load-current conditions where quiescent current is negligible relative to the output current.

If the maximum load-current is much greater than the ground current, then the maximum possible power efficiency is defined by the ratio of the output and the input voltages, as seen in equation (1). The power efficiency increases as the voltage difference between the input and the output decreases. Under these conditions, the LDO is better suited for many applications than the switching regulator because of lower cost, complexity, and output noise. The decision becomes obscure, however, if the output current increases to the point where the LDO requires a heat sink [9]. A heat sink not only increases cost by requiring an additional component but it also means more real estate area in the board, which further increases cost. Applications that require high input/output voltage differentials with high output currents greatly benefit from the efficiency of dc-dc converters. Nevertheless, there are some cases where a high input/output voltage differential regulator is required to drive noise sensitive circuits. In these situations, a switching regulator is used to bring down the voltage and an LDO is cascaded to provide a low noise output [4]. Circuits that perform analog functions tend to be more sensitive to noise originated in the supply rails than the digital counterparts [14]. Therefore, the choice between LDOs and switching regulators is driven by the application and is made during the design of the system.

1.3 Characteristics

Figure 1 illustrates the block level diagram of a generic series low drop-out regulator. The circuit is composed of a reference and associated start-up circuit, protection circuit and associated current sense element, an error amplifier, a pass element, and a feedback network. The reference provides a stable dc bias voltage with limited current driving capabilities. This is usually a zener diode or a bandgap reference. The zener diode finds its applications in high voltage circuits, greater than approximately seven volts, with relaxed temperature variation requirements [1, 3]. The bandgap, on the other hand, is better suited for low voltage and high accuracy applications. The protection circuitry ensures that the LDO operates in safe stable conditions. Some of its functions include over-current protection (typically a foldback current limiter [6]), thermal shutdown in case of self-heating (junction temperature increases beyond safety levels), and other similar functions. The error amplifier, the pass element, and the feedback network form the regulation loop. The temperature dependence of the reference and the amplifier's input offset voltage define the overall temperature coefficient of the regulator; hence, low drift references and low input offset voltage amplifiers are preferred [15].

The noise present at the output of the LDO is composed of three components, namely, noise injected from the system through the substrate and the input voltage, noise generated by the reference circuit, and noise associated with the output trace [lead] inductance and resistance [4]. Switching regulators can typically be used to provide power to LDOs and can be integrated in the same chip thereby injecting noise through the substrate and the input voltage, i.e., cellular phones. In these cases, physical layout isolation techniques and high power supply rejection ratio are intrinsic circuit characteristics for good noise performance. Transient load-current changes also affect the noise content seen by the load. This results from the parasitic resistance and inductance of the trace [lead] from the LDO's output to the load. Therefore, physical proximity of the LDO to its load must be minimized to reduce the noise seen by the load [9].

Low drop-out regulators tend to necessitate large output capacitors that occupy large board area. Furthermore, typical LDOs require that these capacitors have low electrical series resistance (ESR). Consequently, capacitors play an intrinsic role in the cost of the LDO. High power LDOs may require heat sinks further aggravating the cost issue. However, a system level design choice may circumvent the need for a heat sink by utilizing several smaller LDOs distributed throughout the board [4]. Finally, the emergence of finer lithography and the increasing demand for low power cause low voltage operation to be a necessary condition. Therefore, there are some circuit design techniques that are discouraged, which give rise to more complex and possibly more expensive circuits. Some of the discouraged techniques include frivolous cascoding, emitter followers, and Darlington configurations [10].

II. Specifications

The important aspects of the LDO can be summarized into three categories, namely, regulating performance, quiescent current, and operating voltages [16]. Some of the specifications that serve as metrics for the LDO include drop-out voltage, line regulation, load regulation, tolerance over temperature, output voltage variation resulting from a transient load-current step, output capacitor and ESR range, quiescent current, maximum load-current, and input/output voltage range. These performance characteristics often contradict each other giving rise to necessary compromises. The priority of the performance parameters is defined according to the particular application.

Drop-out voltage is the minimum input/output differential voltage where the circuit begins to stop regulation. This can be expressed in terms of switch "on" resistance [R_{on}] [6],

$$V_{drop\text{-}out} = I_{Load}\, R_{on}. \tag{2}$$

Typical drop-out voltages range from 0.1 to 1.5 V [4]. Output voltage variations arising from specific changes in input voltage is defined as line regulation. Similarly, load regulation is the change in output voltage for specific changes in load-current [2]. Load regulation is essentially the output impedance of the circuit [R_o],

$$R_o = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}, \tag{3}$$

where ΔV_{LDR} and ΔI_o are the output voltage and the load-current changes, $R_{o\text{-}pass}$ is the output impedance of the pass element, A_{ol} is the open-loop gain of the system, and β is the feedback factor [3]. Therefore, improved load regulation of the system results from higher dc open-loop gain [9]. The temperature dependence of the output voltage is a function of the temperature drift of the reference and that of the input offset voltage of the error amplifier,

$$TC = \frac{1}{V_o} \cdot \frac{\partial V_o}{\partial Temp} \approx \frac{1}{V_o} \cdot \frac{\Delta V_{TC}}{\Delta Temp} = \frac{\left[\Delta V_{TC_{ref}} + \Delta V_{TC_{Vos}}\right] \frac{V_o}{V_{ref}}}{V_o\, \Delta Temp}, \tag{4}$$

where TC is the temperature coefficient, ΔV_{TC} is the output voltage variation over the temperature range ΔTemp, ΔV_{TCref} and ΔV_{TCVos} are the voltage variations of the reference and input offset voltage of the error amplifier, and V_o/V_{ref} is the ratio of the nominal output and reference voltages. Transient output voltage variations resulting from sudden load-current changes are dominated by the closed-loop bandwidth of the system, output capacitor, and load-current. The worst case situation occurs when the load-current suddenly steps from zero to its maximum specified value. The resulting output voltage variation is described as

$$\Delta V_{tr} = \frac{I_{o-max}\Delta t}{C_o}, \tag{5}$$

where ΔV_{tr} is the output voltage variation, $I_{o\text{-}max}$ is the maximum specified load-current, C_o is the output capacitor, and Δt is the time required for the LDO to respond (approximately equal to the reciprocal of the closed-loop bandwidth [BW_{cl}] if internal slew-rate conditions are neglected). This output voltage variation must be kept low to meet the overall accuracy requirements of the system, i.e., 150 - 300 mV [8]. Thus, the circuit benefits from the use of a high bandwidth amplifier in the feedback loop. A pivotal specification is the output capacitor and associated ESR range for which the LDO is stable. This can typically prove to be a difficult task if a wide range of values is to be allowed. The value of the load-current also affects the frequency response of the circuit. Lastly, long term stability and low external component count are also pertinent factors to keep in mind when designing LDOs.

The effects of line regulation, load regulation, temperature dependence, and transient output voltage variations can be summed up into one specification, accuracy.

Accuracy refers to the total output voltage variation and can be described by the absolute minimum and maximum output voltages ($V_{o\text{-}min}$ and $V_{o\text{-}max}$), shown in the following equations:

$$V_{o-min} \le \Delta V_{LNR} + \Delta V_{LDR} + \Delta V_{TC} + \Delta V_{tr} + V_{reference}\left\langle \frac{V_o}{V_{ref}} \right\rangle \le V_{o-max}, \quad (6)$$

$$V_{reference} = V_{ref} + \Delta V_{TC_{ref}} + \Delta V_{LNR_{ref}} \pm V_{os}, \quad (7)$$

$$Accuracy_{system} = \left\langle \frac{V_{o\,max} - V_{o\,min}}{V_o} \right\rangle, \quad (8)$$

where ΔV_{LNR}, ΔV_{LDR}, ΔV_{TC}, ΔV_{tr}, ΔV_{TCref}, and ΔV_{LNRref} are voltage variations resulting from line regulation, load regulation, temperature dependence, worst case transient load-current steps, reference circuit's temperature dependence, and reference circuit's line regulation respectively while V_{os} and V_o are the input offset voltage of the error amplifier and the nominal output voltage of the regulator. In specifying accuracy, the effect of the transient load-current step and the reference circuit is sometimes excluded but they are included here for completeness. Low voltage operation often implies more stringent specifications in the form of overall accuracy. Typical implementations achieve roughly 1 % total variation resulting from load regulation, line regulation, and temperature dependence while leaving some headroom for transient load-current specifications [9].

III. AC Analysis

Figure 2 illustrates the intrinsic factors that determine the stability of the system, namely, an error amplifier, a pass element, feedback resistors, an output load-current and associated output impedance, an output capacitor and associated ESR, and a bypass capacitor. The ESR of the bypass capacitors can typically be neglected because they are usually high frequency capacitors; in other words, they have low ESR values [17].

For the purpose of analysis, the feedback loop can be broken at "A" in Figure 2. It is readily apparent that the system must be unity gain stable, considering V_{ref} and V_{fb} to be the input and the output voltages respectively. The open-loop gain can be described as

$$\frac{V_{fb}}{V_{ref}} = \left|A_v\right| = \frac{g_{ma} R_{oa} g_{mp} Z}{[1 + sR_{oa} C_{par}]} \cdot \frac{R_1}{[R_1 + R_2]}, \tag{9}$$

where g_{ma} and g_{mp} refer to the transconductance of the amplifier and the pass element, R_{oa} is the output impedance of the amplifier, C_{par} refers to the parasitic capacitance introduced by the pass element, and Z is the impedance seen at V_{out},

$$Z = R_x // \frac{sC_o R_{esr} + 1}{sC_o} // \frac{1}{sC_b} = \frac{R_x[sC_o R_{esr} + 1]}{s^2 C_o C_b R_x R_{esr} + sC_o[R_x + R_{esr}] + sC_b R_x + 1}, \tag{10}$$

where C_o and R_{esr} are the capacitance and the ESR of the output capacitor, C_b is the bypass capacitor, and R_x is the impedance seen from V_{out} back into the regulator defined as

$$R_x = R_{o\text{-}pass} // [R_1 + R_2], \tag{11}$$

where $R_{o\text{-}pass}$ is the output resistance of the pass element. The output resistance of the load [R_L] is commonly neglected because its value is significantly larger than R_x. If C_o is assumed to be reasonably larger than C_b (typical condition), then Z approximates to

$$Z \approx \frac{R_x[sC_o R_{esr} + 1]}{[1 + sC_o(R_x + R_{esr})][1 + sC_b(R_x // R_{esr})]}. \tag{12}$$

It can be observed from equations (9) - (12) that the overall transfer function of the system consists of three poles and one zero, a potentially unstable system. For the majority of the load-current range, R_x simplifies to $R_{o\text{-}pass}$ since $R_1 + R_2$ is greater in magnitude (especially at high currents). The poles and zero can thus be approximated to be the following:

$$P_1 = 1 / 2\pi C_o R_{o\text{-}pass}, \tag{13}$$

$$P_2 = 1 / 2\pi C_b R_{esr}, \tag{14}$$

$$P_3 = 1 / 2\pi R_{oa} C_{par}, \tag{15}$$

and

$$Z_1 = 1 / 2\pi C_o R_{esr}. \tag{16}$$

Figure 3 illustrates the typical frequency response of the system assuming that the output capacitor [C_o] is larger than the bypass capacitor [C_b]. The regulator yields better load regulation performance as the open-loop gain increases; however, the gain is limited by the closed-loop bandwidth of the system, equivalent to the unity gain frequency (UGF). The minimum UGF is bounded by the response time required to yield an allowable output voltage variation during a transient load-current step, which was discussed in the specifications section. Furthermore, the maximum UGF is also bounded by the parasitic poles of the system, i.e., P_3 and internal poles of the amplifier. If the parasitic poles are assumed to be at higher frequencies than 1 MHz, then the gain at 1.0 kHz has to be less than 40 - 45 dB depending on the location of Z_1 and P_2, assuming the conditions illustrated in Figure 3. Moreover, the pass element's associated input capacitance (error amplifier's load capacitance) is significantly large. This places a ceiling on the value of the amplifier's output impedance [R_{oa}]. The pass element typically needs to be a large device to yield low drop-out voltages and high output current characteristics with limited voltage [current] drive, low voltage and low power atmosphere.

The worst case stability condition, given the set of elements shown in Figure 2, arises when the phase margin is at its lowest point, which occurs when the unity gain frequency is pushed out to higher frequencies where the parasitic poles reside. This happens when the load-current is at its peak value [17]. This is because the dominant pole [P_1] usually increases at a faster rate ($R_{o\text{-}pass}$ decreases linearly with increasing current, $1/\lambda I_o$ or V_a/I_o) than the gain of the system decreases ($g_{mp}R_{o\text{-}pass}$ decreases with the square root of the increasing current for a MOS device or stays constant for a bipolar transistor). The type and value of the output capacitor determine the location of P_1, P_2, and Z_1. Therefore, the permissible range of values of ESR for a stable circuit is a function of load-current and circuit characteristics [5]. Spice simulations confirm the aforementioned tendencies.

IV. Transient Analysis

An important specification is the maximum allowable output voltage change for a full range transient load-current step. The application determines how low this value is required to be. For instance, a less stringent specification for the peak output voltage variation can be tolerated if the regulator is used to provide power to digital circuits, which inherently have high noise margins [6]. However, this is not the case for many analog applications. Figure 4 shows the characteristic nature of the stimulus and the typical respective response. The time required for the loop to respond [Δt_1] (ideally the reciprocal of the closed-loop bandwidth) is specified by the output capacitor, maximum load-current, and maximum allowable output voltage variation [equation (5)]. However, in typical implementations the time is prolonged by the internal slew-rate associated with the parasitic capacitance [C_{par}] of the pass element in Figure 2. The resulting time can be approximated to be

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par}\frac{\Delta V}{I_{sr}}, \tag{17}$$

where BW_{cl} is the closed-loop bandwidth of the system, t_{sr} is the slew-rate time associated with C_{par}, ΔV is the voltage variation at C_{par}, and I_{sr} is the slew-rate limited current. For instance, if BW_{cl} is 500 kHz, C_{par} is 200 pF, ΔV is 0.5 V, I_{sr} is 5 µA, C_o is 10 µF, and $I_{Load\text{-}max}$ is 100 mA, then the maximum output voltage variation is approximately 220 mV [equations (5) and (17)]. However, if the slew-rate current is large enough, the reciprocal of the closed-loop bandwidth starts to dominate Δt_1. This would be at the cost of quiescent current, in other words, battery lifetime. Once the slew-rate condition is terminated, the output voltage recovers and settles to its final value. The settling time [Δt_2] is dependent on the phase margin of the open-loop frequency response.

The slew-rate limitation is usually unidirectional in nature thereby creating the asymmetrical response of Figure 4. The slew-rate condition typically occurs when the load-current steps from zero to full range. The direction for which this condition occurs is dependent on the configuration of the buffer and the output pass device. A typical topology is that of a class "A" buffer driving a PMOS pass element and associated parasitic capacitance [C_{par}]. A class "A" stage yields high current in one direction and limited dc current in the other, i.e., emitter [source] follower biased with a dc current source. An example of this is illustrated in the simplified schematic of Figure 5. More complex topologies, however, could be implemented for the buffer to realize high symmetrical slew-rate currents. The portion of the time response that does not experience internal slew-rate is dominated by the bandwidth and the low pull-down current of the LDO's output, $I_{pull\text{-}down}$ in Figure 5. The output voltage variation during this condition can be described as

$$\Delta V_2 \approx \frac{I_{o-max}}{C_o}\Delta t_3 \approx \frac{I_{o-max}}{C_o}\cdot\frac{1}{BW_{cl}}, \qquad (18)$$

where the terminology of Figures 4 and 5 is adopted. At this point, the output voltage takes time,

$$\Delta t_4 \approx C_o \frac{\Delta V_2}{I_{pull-down}} = C_o \frac{\Delta V_2 R_1}{V_{ref}}, \qquad (19)$$

to discharge to its final value.

V. The Pass Device

The five basic possible configurations for the pass element are illustrated in Figure 6, namely, NPN Darlington, NPN follower, common emitter lateral PNP, NMOS follower, and common source PMOS transistor [4]. The degree of freedom for the choice of topology is dependent on the process technology and the required specifications of the LDO. Multiple transistor structures are also possible candidates for pass devices. However, the intrinsic performance characteristics of these structures center around the transistor that actually delivers the output current. The remaining devices can be grouped into the output stage of the feedback amplifier, otherwise referred to as the buffer stage.

Table 1 shows a comparison between the different pass elements with respect to their applicable LDO performance parameters. Bipolar devices are capable of delivering the highest output currents for a given supply voltage. On the other hand, the output current capabilities per unit area of MOS transistors exhibit limited performance with high dependencies on aspect ratio and gate drive. However, the voltage driven nature of MOS devices is beneficial in minimizing quiescent current. Bipolar transistors are current driven with finite forward current gains (β) that can be as low as 20 A/A over process variations. As a result, the error amplifier that drives a bipolar pass device must be able to source or sink relatively high base currents. The base current of the NPN transistor, however, flows to the output while that of the PNP counterpart is lost as ground current. Consequently, NPN structures are better suited for low quiescent current flow than PNP realizations. The fastest response, needed for transient load-current steps, is achieved by NPN structures. PNP transistors are typically created as lateral devices with inherent slow response times. Vertical PNP structures yield faster response times but their availability is limited in standard process technologies. MOS transistors are typically slower than vertical bipolar devices but faster than lateral PNP realizations.

Lowest drop-out voltages are achieved by PMOS ($V_{sd\text{-}sat}$) and PNP ($V_{ec\text{-}sat}$) transistors, approximately between 0.1 and 0.4 V. The NPN Darlington, NPN, and NMOS structures involve at least one V_{be} [V_{gs}] and one $V_{ec\text{-}sat}$ [$V_{sd\text{-}sat}$] with a minimum drop-out voltage of roughly 0.8 to 1.2 V. However, the drop-out voltage of these pass devices could be improved by utilizing a charge pump. The disadvantage of this technique lies in complexity and cost. It requires an oscillator thereby increasing quiescent current overhead, noise injection, and circuit complexity. Excluding the charge pump method, PMOS transistors exhibit the lowest drop-out voltages because of their characteristically variable resistance, V_{sd} changes with gate drive and aspect ratio. On the other hand, PNP devices have a constant saturation voltage that is approximately 200 mV. In conclusion, PMOS devices are typically the best overall choice yielding a good compromise of drop-out voltage, quiescent current flow, output current, and speed.

The circuit design of the LDO is thoroughly affected by the physical requirements of the pass device. The pass element must be physically large to yield high output currents and low drop-out voltage characteristics. This translates to a large load capacitance for the error amplifier, characterized as C_{par} in the frequency response section. Consequently, the parasitic pole at the output of the amplifier is pulled to lower frequencies thereby degrading the phase margin and compromising the stability of the system. Moreover, leakage currents increase as the device size increases, i.e., MOS sub-threshold currents. This places an upper limit on device size, a lower limit on quiescent current, and/or more stringent requirements on the error amplifier. Furthermore, drop-out voltage is increased by series parasitic resistance inherent in the layout, such as the pass device's source [emitter] and drain [collector] contacts, metal traces, and diffusion links. Lastly, the drive requirements of the pass device can generally define the minimum input voltage of the regulator, i.e., the gate drive of the PMOS transistor necessary to yield high output currents and low drop-out voltages ($V_{in} \geq V_{sg} + V_{ds}$, where V_{ds} corresponds to the voltage overhead of a current source).

VI. The Amplifier

The specifications of the amplifier that are relevant to the LDO as inferred from the previous discussions are: output impedance, gain, bandwidth, output slew-rate current, output voltage swing, and quiescent current. The output impedance must be low enough so as to place the parasitic pole P_3 [equation (15)] at a frequency greater than the unity gain frequency, thus maintaining stability. The requirement is stringent because of the large value of the load capacitance introduced by the vast pass device. This requires the use of a buffer to isolate the high output resistance of the gain stage [R_{og}] from the high load capacitance [C_{par}], as illustrated in Figure 7.

Load regulation performance is enhanced as the open-loop gain of the system is increased, as shown in equation (3). However, the gain is limited by the unity gain frequency, as discussed in the ac analysis section. Therefore, caution must be exercised in designing the gain-bandwidth product (GBW) of the amplifier. This is dependent on the location of the output poles and the zero of the system, namely, P_1, P_2, and Z_1 [equations (13), (14), and (16)]. It is further noted that the location of the dominant pole [P_1] varies with load-current, i.e., $R_{o\text{-}pass} \propto 1/I_{Load}$ for all pass elements except for the NMOS source follower, where $R_{o\text{-}NMOS} \propto 1/\sqrt{I_{Load}}$.

The topology and the biasing current of the buffer is designed according to the frequency and the transient response requirements of the system. Transient specifications tend to dominate the bias current demands of the buffer. In particular, the slew-rate current available to the output of the buffer partially determines the magnitude of the output voltage variation during transient load-current steps, as discussed in the transient analysis. The choice in topology also reflects the driving requirements of the pass device. For instance, a PMOS pass device requires a high negative voltage swing to yield maximum gate drive and thus produce large output currents and low drop-out voltages. On the other hand, a high positive swing is needed to shut off the device to the point where sub-threshold currents do not become a problem. A simple implementation of the buffer could be a source follower using a natural NMOS transistor, which is a non-threshold adjusted device exhibiting threshold voltages close to zero [DE3]. These devices are available at the possible cost of one extra mask in the process flow. The product of the input capacitance of the buffer [C_{buf}] and the output resistance of the gain stage [R_{og}] must be kept low to yield an internal frequency pole that is greater than the unity gain frequency of the system. Therefore, the ohmic resistance and line capacitance of the trace path in the layout between the output of the gain stage and the input of the buffer must be minimized.

The overall design of the amplifier must be kept as simple as the specifications will allow in order to necessitate low quiescent currents. The limiting factors for low quiescent current are amplifier bandwidth and slew-rate requirements. A tradeoff between performance and power dissipation is therefore necessary. In a low voltage environment, such as the case for battery operated applications, the number of devices connected from the input voltage to ground must be kept low [10]. The ultimate limit is one diode connected and one common source [emitter] device, V_{be} [V_{gs}] + V_{ec-sat} [V_{sd-sat}]. More flexibility may be allowed if the limiting factor lies elsewhere in the system, i.e., pass element's voltage drive requirements.

VII. Conclusion

Applications that demand the use of low drop-out (LDO) regulators include cellular phones, pagers, camera recorders, laptops, and automotive components. LDOs are characteristically simpler and yield less noise than switching regulators. On the other hand, the power efficiency of switching regulators is typically better than that of LDOs. Though these two types of circuits serve similar functions, their performance characteristics make them suitable for different applications and sometimes both are necessary in the same system.

The major components of the LDO are an error amplifier, a pass element, a reference circuit, a feedback network, and some protection circuitry. The regulating loop is formed by the amplifier, the pass element, and feedback components (typically a resistive network). These coupled with the load (output capacitor and associated electrical series resistance [ESR], load-current and associated output impedance, and bypass capacitors) determine the performance characteristics of the regulator. The metrics used to describe performance include drop-out voltage, accuracy, quiescent current, output capacitor and associated ESR range, input/output voltage range, and maximum output current.

Analysis show that the system inherently exhibits an open-loop transfer response of three poles, one zero, and parasitic poles internal to the amplifier. This frequency response behavior results in the use of large output capacitors to ensure stability. Further analysis show that the system is typically slew-rate limited at the output of the error amplifier as a result of a parasitic capacitance introduced by the pass element. Consequently, the amplifier must have a low output impedance with relatively high output current capabilities. The use of a buffer in the amplifier is encouraged to isolate the high capacitance of the pass element from the characteristically high output resistance of the amplifier. Such a buffer could be a natural NMOS (non threshold-adjusted NMOS device exhibiting low threshold voltages) source follower. The most appropriate pass elements for low drop-out voltage are PMOS and PNP transistors (preferably vertical but seldom available). However, PMOS devices are better suited for low quiescent current flow (ground current) applications because of their voltage driven nature. In conclusion, the paper has demonstrated the issues involved in designing a low drop-out regulator under existing process technologies meeting today's and tomorrow's market demands.

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Table 1. Comparison of pass element structures.

	Darlington	NPN	PNP	NMOS	PMOS
$I_{o\text{-}max}$	High	High	High	Medium	Medium
$I_{quiescent}$	Medium	Medium	Large	Low	Low
$V_{drop\text{-}out}$	$V_{sat}+2V_{be}$	$V_{sat}+V_{be}$	$V_{ec\text{-}sat}$	$V_{sat}+V_{gs}$	$V_{sd\text{-}sat}$
Speed	Fast	Fast	Slow	Medium	Medium

Figure Captions

Figure 1. Generic low drop-out series linear regulator architecture.

Figure 2. System model under loading conditions.

Figure 3. LDO frequency response under loading conditions.

Figure 4. Typical LDO transient response to a load-current step.

Figure 5. Simplified LDO schematic for the purpose of transient analysis.

Figure 6. Pass element structures.

Figure 7. LDO buffered architecture.

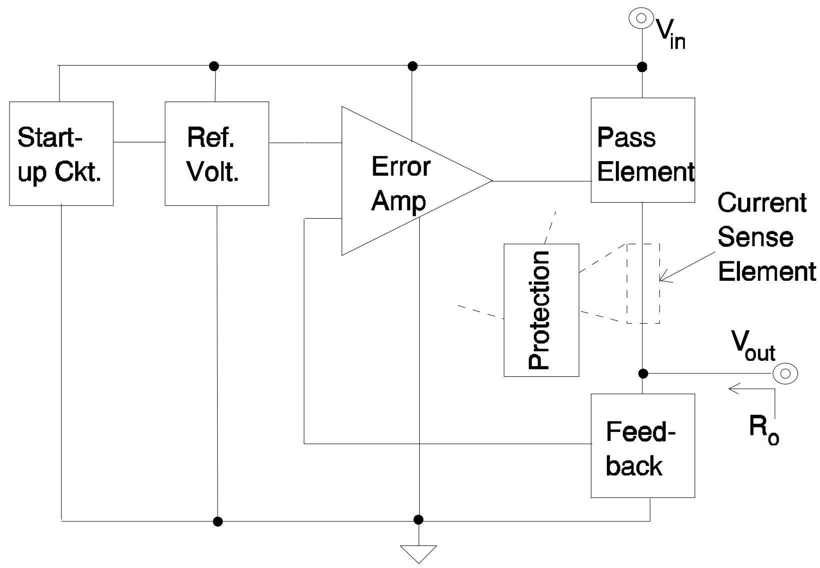

Figure 1. Generic low drop-out series linear regulator architecture.

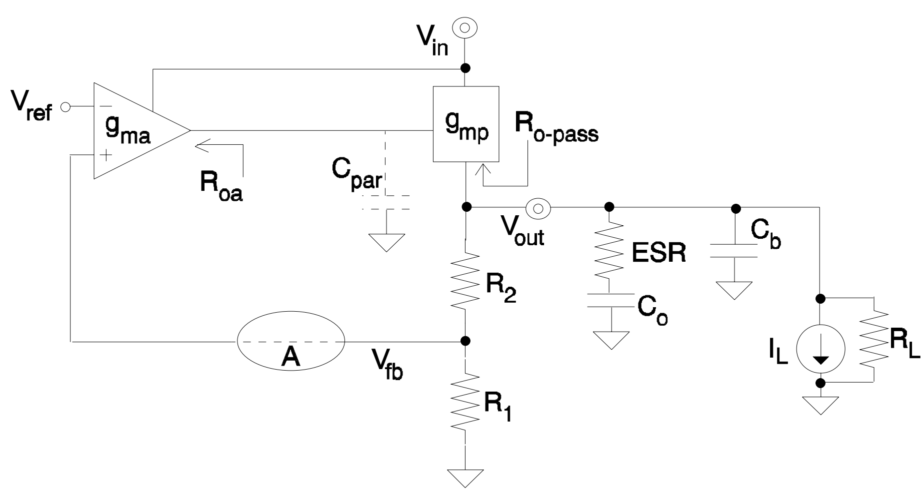

Figure 2. System model under loading conditions.

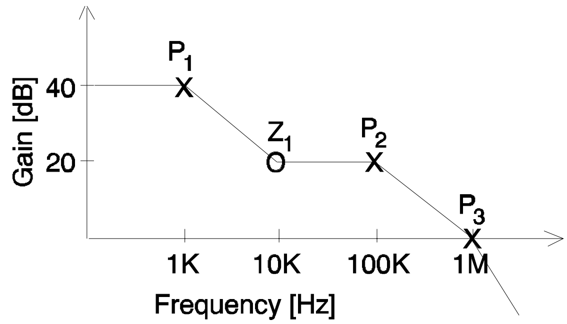

Figure 3. LDO frequency response under loading conditions.

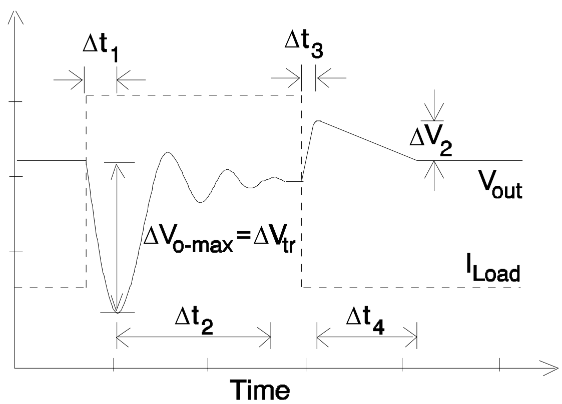

Figure 4. Typical LDO transient response to a load-current step.

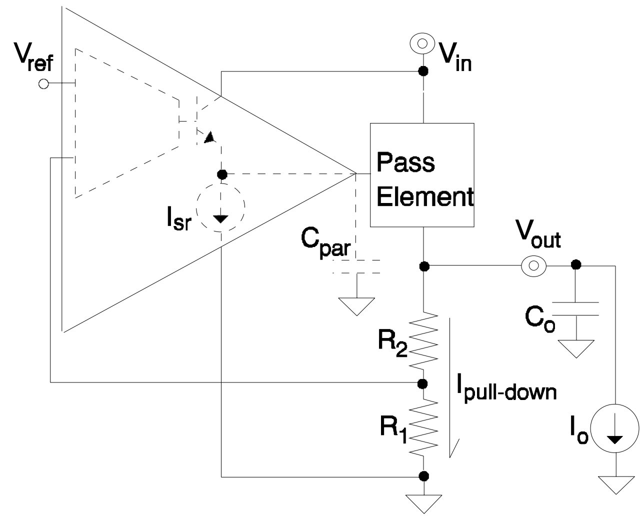

Figure 5. Simplified LDO schematic for the purpose of transient analysis.

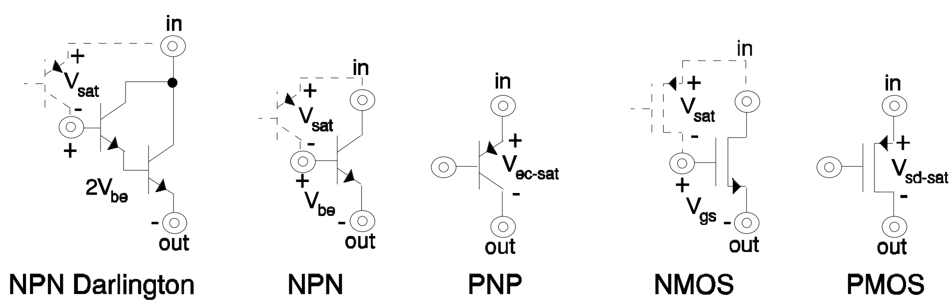

Figure 6. Pass element structures.

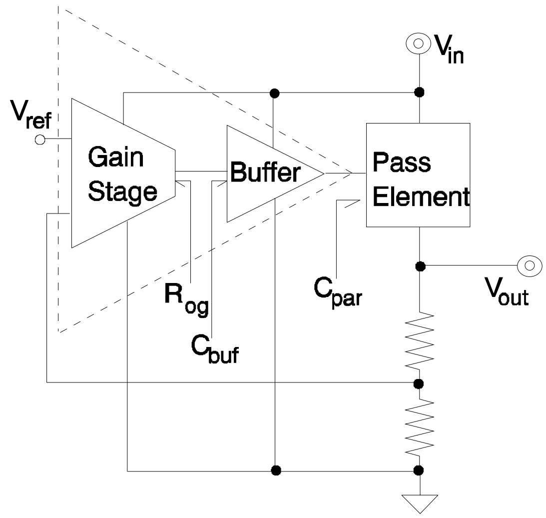

Figure 7. LDO buffered architecture.