

# Analog Integrated Circuits

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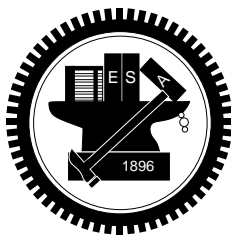
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# Analog Integrated Circuits

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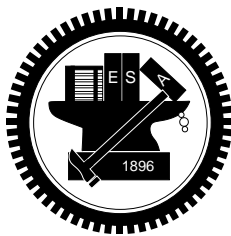
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- 20. Fundamentals of Analog Filters
- 21. Active-RC Filters
- 22. MOST-C and  $G_m$ -C Filters
- 23. Switched-Capacitor Filters
- 24. Niquist-Rate Digital-to-Analog Converters
- 25. Niquist-Rate Analog-to-Digital Converters
- 26. Oversampling Converters
- 27. Phase-Locked Loops

# Introduction

Jieh-Tsorng Wu

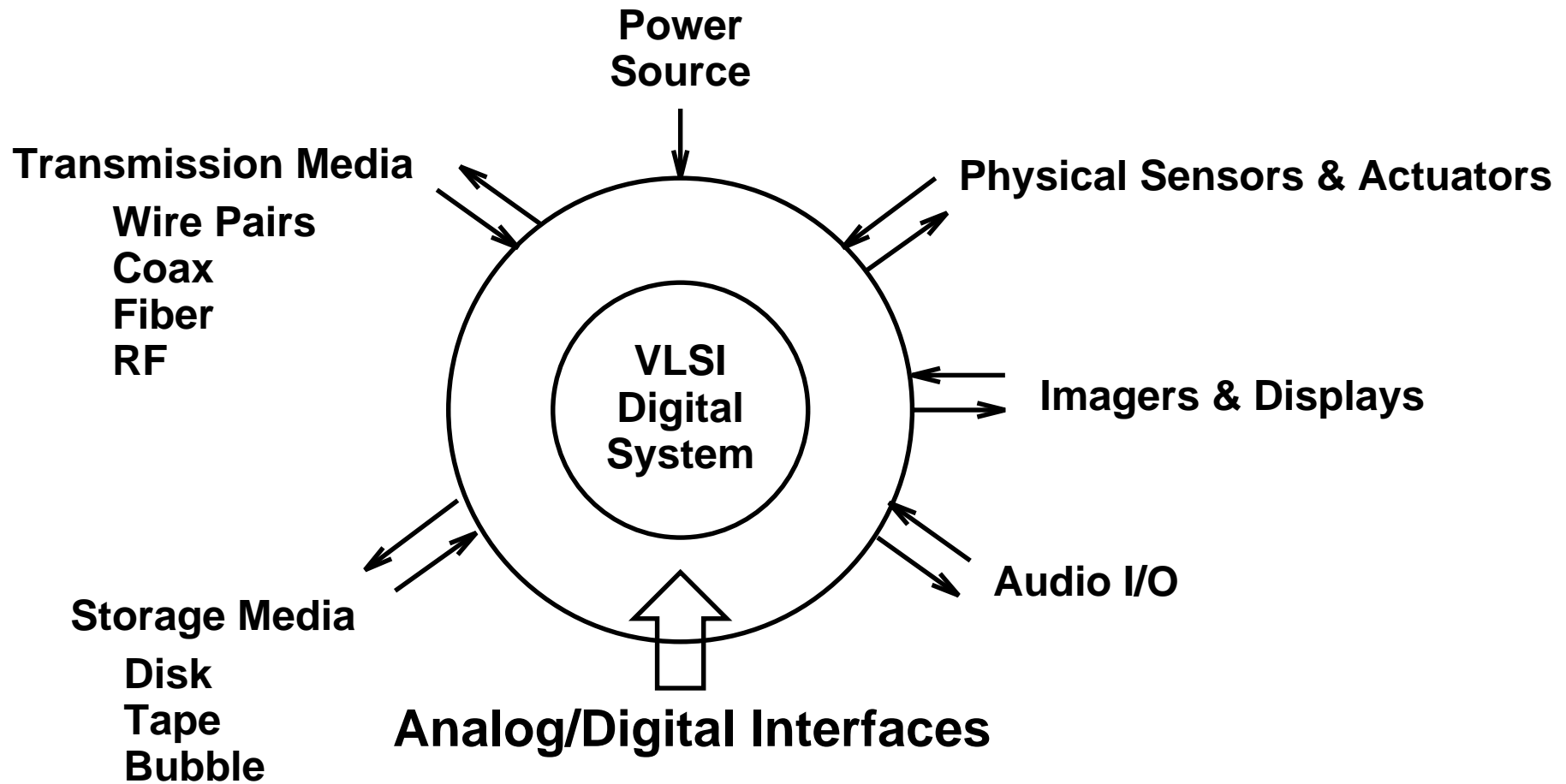
July 16, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Analog Integrated Circuits

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- Usually integrated with digital VLSI circuits monolithically (*mixed-signal integrated circuits*) for better performance and/or lower cost.

# Analog Signal Processing

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## Analog Signals

- Always continuous in amplitude.
- Either continuous in time (s-transform) or discrete in time (z-transform).

Analog circuits provide interfaces between the analog environment of the physical world and a digital environment. Major functions are

- Amplification.
- Filtering.
- Analog-to-digital conversion.
- Digital-to-analog conversion.
- Power supply conditioning.

# Design for Analog Circuits

---

## Signal path

- Small (variational) signals related by linear transfer function in the frequency domain.
- Model with linearized *small-signal* equivalent circuit.
- Analyze using Laplace transforms.

## Biasing Circuit

- Establish operating conditions of devices in signal path.
- Concern with sensitivity to variations in temperature, supply voltage, and fabrication process.
- Analyze using *large-signal* device models.

# Performance Considerations

---

- Small-signal response: gain, bandwidth, noises, . . .
- Large-signal response: settling time, distortion, . . .
- Sensitivity to device variation, temperature variation, external noises, . . .
- Cost: power dissipation, chip area, yield.

# Design Practices

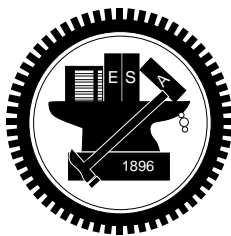
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- Make simplifying assumptions that allow hand analysis.
- Keep in mind potential consequences of the assumptions.
- Use simulations to verify the design.
- Good designs are robust; i.e., insensitive to approximations in the modeling as well as variations in temperature and fabrication process.

# PN Junctions and Bipolar Junction Transistors

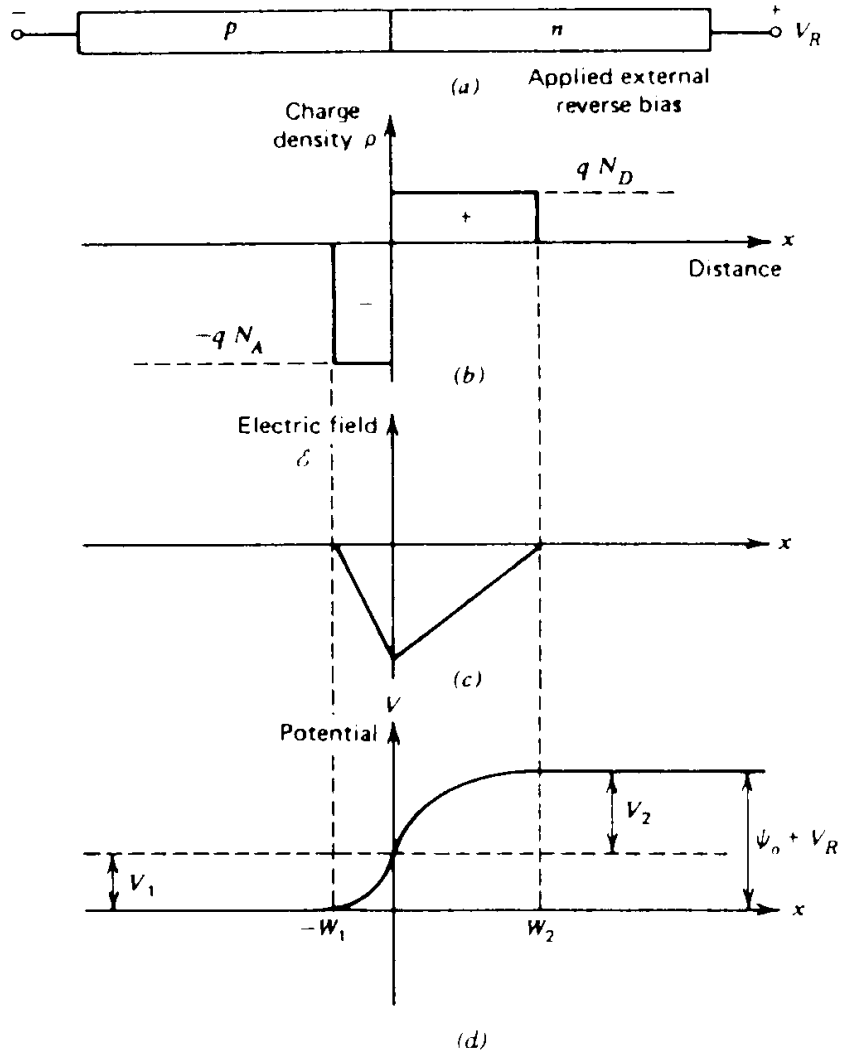
Jieh-Tsorng Wu

September 6, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# PN Junctions



$$\text{Built-in potential} = \psi_0 = U_T \ln \frac{N_A N_D}{n_i^2}$$

$$U_T = \frac{kT}{q} \approx 26 \text{ mV at } 300^\circ\text{K}$$

$$n_i \approx 1.5 \times 10^{10} \text{ cm}^{-3} \text{ at } 300^\circ\text{K for Si}$$

Solving Poisson's equation,

$$W_1 = \left[ \frac{2\epsilon(\psi_0 + V_R)}{qN_A \left(1 + \frac{N_A}{N_D}\right)} \right]^{1/2}$$

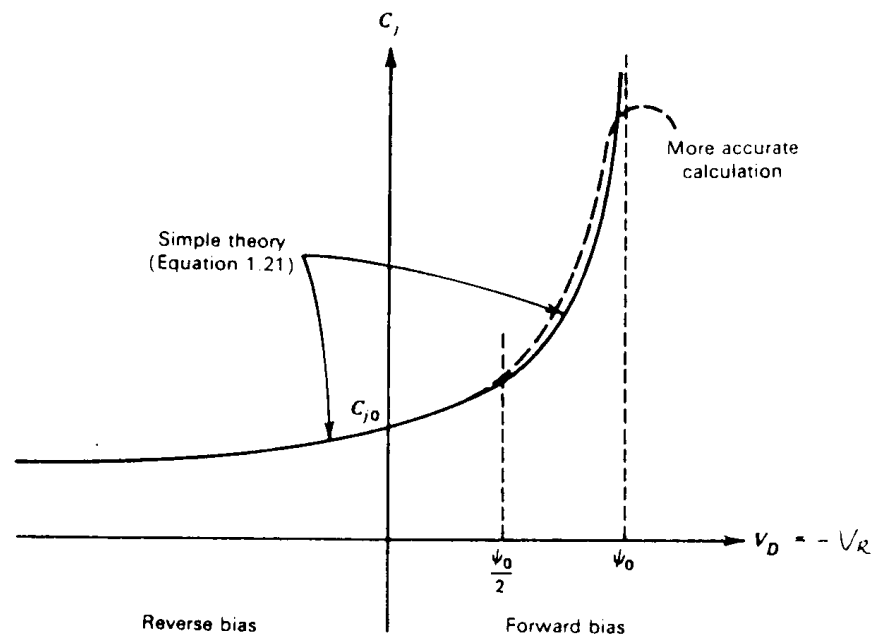
$$W_2 = \left[ \frac{2\epsilon(\psi_0 + V_R)}{qN_D \left(1 + \frac{N_D}{N_A}\right)} \right]^{1/2}$$

# Small-Signal Junction Capacitance

Depletion layer charge is  $Q_j = qN_A W_1 A = qN_D W_2 A$ , where  $A$  is the cross-sectional area.

Depletion-region capacitance

$$C_j = \frac{dQ_j}{dV_R} = A \left[ \frac{q\epsilon N_A N_D}{2\psi_0 N_A + N_D} \right]^{1/2} \cdot \frac{1}{\sqrt{1 + \frac{V_R}{\psi_0}}} = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\psi_0}}}$$



# Small-Signal Junction Capacitance

---

- $C_j$  can be expressed as

$$C_j = A \cdot \frac{\epsilon}{x_d} \quad x_d = W_1 + W_2$$

- In general

$$C_j = \frac{C_{j0}}{\left(1 + \frac{V_R}{\psi_0}\right)^m} \quad \frac{1}{3} \leq m \leq \frac{1}{2}$$

- $m = 1/2$  for abrupt junction.
  - $m = 1/3$  for graded junction.
- In forward bias, diffusion capacitance dominates.

# Large-Signal Junction Capacitance

---

Depletion layer charge can be rewritten as

$$Q_j = \frac{C_{j0}}{1-m} \cdot \psi_0 \cdot \left(1 + \frac{V_R}{\psi_0}\right)^{1-m}$$

Average capacitance is defined as

$$C_{j-av} = \frac{Q_j(V_2) - Q_j(V_1)}{V_2 - V_1}$$

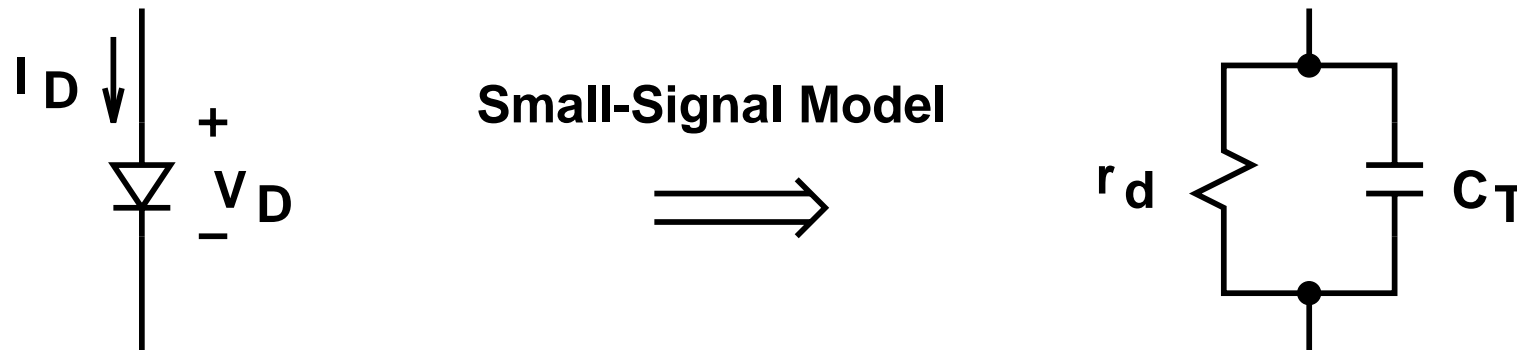
For an abrupt junction,  $m = 0.5$ ,

$$C_{j-av} = 2C_{j0}\psi_0 \cdot \frac{\sqrt{1 + \frac{V_2}{\psi_0}} - \sqrt{1 + \frac{V_1}{\psi_0}}}{V_2 - V_1}$$

- If  $V_1 = 0$  V,  $V_2 = 5$  V, and  $\psi_0 = 0.9$  V

$$C_{j-av} = 0.56 \cdot C_{j0} \approx \frac{1}{2} C_{j0}$$

# PN Junction in Forward Bias



$$I_D = I_S(e^{V_D/U_T} - 1) \approx I_S e^{V_D/U_T} \quad I_S \approx A \left( \frac{1}{N_A} + \frac{1}{N_D} \right)$$

$$\frac{1}{r_d} = \frac{dI_D}{dV_D} = \frac{I_D}{U_T} \quad C_T = C_d + C_j$$

$$C_d = \tau_T \cdot \frac{I_D}{U_T} = \frac{\tau_T}{r_d} \quad \tau_T = \text{Transit Time}$$

- For moderate forward-bias currents,  $C_d \gg C_j$ ,  $r_d C_T \approx \tau_T$ .
- For Schottky diode,  $C_d = 0$ .

# PN Junction Avalanche Breakdown

---

- The maximum electric field in the depletion region of an abrupt junction is

$$|\mathcal{E}_{max}| = \frac{qN_A W_1}{\epsilon} = \left[ \frac{2qN_A N_D (\psi_0 + V_R)}{\epsilon(N_A + N_D)} \right]^{1/2}$$

$|\mathcal{E}_{max}|$  increases with both  $V_R$  and doping density.

- As  $|\mathcal{E}_{max}| \rightarrow \mathcal{E}_{crit}$ , carriers crossing the depletion region acquire enough energy to create new electron-hole pairs when colliding with silicon atoms. The result is *avalanche breakdown*.

$$I_{RA} = M I_R \quad M = \frac{1}{1 - \left(\frac{V_R}{BV}\right)^n}$$

$BV$  is the *breakdown voltage*. And typically  $3 \leq n \leq 6$

- $\mathcal{E}_{crit}$  is a function of doping density, which can vary from  $3 \times 10^5$  V/cm to  $10^6$  V/cm as  $N_A$  (or  $N_D$ ) varying from  $10^{15}$  atoms/cm<sup>3</sup> to  $10^{18}$  atoms/cm<sup>3</sup>.

# PN Junction Breakdown

---

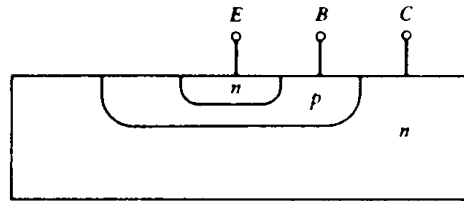
## *Zener Breakdown*

- In very heavily doped junctions where the electric field becomes large enough to strip electrons always from the valence bonds. This process is called *tunneling*.
- The Zener breakdown mechanism is important only for breakdown voltages below about 6 V.

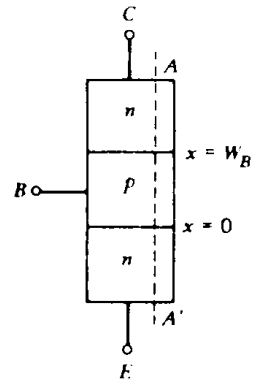
## *Punch Through*

- A form of breakdown that occurs when the depletion regions of two neighboring junctions meet.

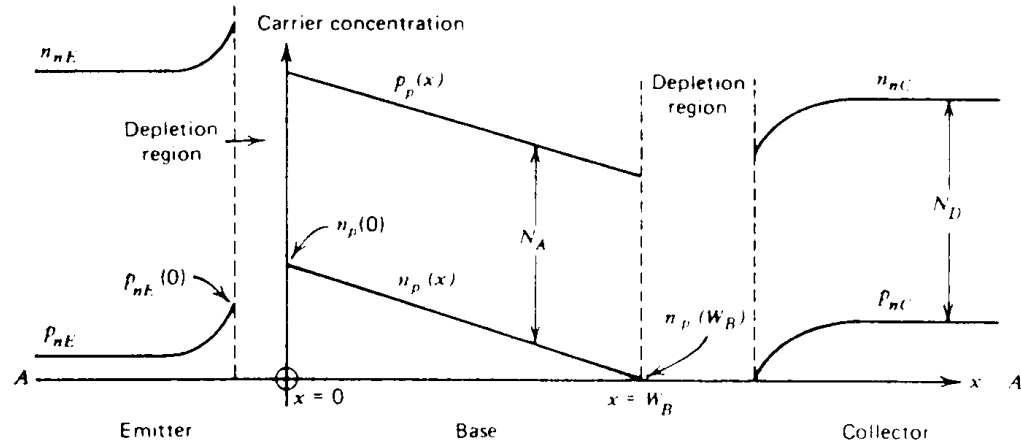
# Bipolar Junction Transistor (BJT)



(a)



(b)



(c)

## Minority Carrier Current in the Base Region

---

There is a negligible flow of holes between emitter and collector junctions because neither can supply a significant flow of holes into the base. Thus, in the neutral base region,

$$J_p = q\mu_p p_b(x)\mathcal{E}(x) - qD_p \frac{dp_b}{dx} = 0 \quad \Rightarrow \quad \mathcal{E}(x) = \frac{D_p}{\mu_p} \frac{1}{p_b} \frac{dp_b}{dx} = \frac{kT}{q} \frac{1}{p_b} \frac{dp_b}{dx}$$

- Note that for uniformly doped region  $dp_b/dx = 0 \Rightarrow \mathcal{E}(x) = 0$

For electrons in the base,

$$\begin{aligned} J_n &= q\mu_n n_b(x)\mathcal{E}(x) + qD_n \frac{dn_b}{dx} = kT\mu_n \frac{n_b}{p_b} \frac{dp_b}{dx} + qD_n \frac{dn_b}{dx} = \frac{qD_n}{p_b} \left( n_b \frac{dp_b}{dx} + p_b \frac{dn_b}{dx} \right) \\ &= \frac{qD_n}{p_b} \left[ \frac{d(n_b p_b)}{dx} \right] \end{aligned}$$

## Minority Carrier Current in the Base Region

---

Assuming negligible recombination in the base, so that  $J_n$  is constant,

$$J_n \int_0^{W_B} \frac{p_b(x)}{qD_n} dx = \int_0^{W_B} \frac{d(n_b p_b)}{dx} dx = n_b(0)p_b(0) - n_b(W_B)p_b(W_B)$$

From the Boltzman approximation at the edges of the depletion layers,

$$n_b(0)p_b(0) = n_i^2 e^{V_{BE}/U_T} \quad n_b(W_B)p_b(W_B) = n_i^2 e^{V_{BC}/U_T}$$

Thus

$$J_n = \frac{qn_i^2}{\int_0^{W_B} \frac{p_b}{D_n} dx} \left( e^{V_{BE}/U_T} - e^{V_{BC}/U_T} \right) = J_S \left( e^{V_{BE}/U_T} - e^{V_{BC}/U_T} \right)$$

where

$$J_S \equiv \frac{qn_i^2}{\int_0^{W_B} \frac{p_b}{D_n} dx}$$

## Gummel Number (G)

---

$D_n$  is a weak function of  $x$ . Then,  $J_S$  can be expressed as

$$J_S = \frac{qn_i^2}{\int_0^{W_B} \frac{p_b}{D_n} dx} = \frac{qn_i^2 \bar{D}_n}{G}$$

where

$$G \equiv \int_0^{W_B} p_b(x) dx \approx \int_0^{W_B} N_A(x) dx$$

- The *Gummel number*,  $G$ , is simply the dopant concentration per unit cross-sectional area of the base.
- For a uniform base region,  $N_A(x) = N_A$ , then  $G = W_B N_A$ .

## Base Transport Current

---

The total minority carrier *transport current* across the base is

$$I_T = J_N \times A = I_S \left[ e^{V_{BE}/U_T} - e^{V_{BC}/U_T} \right] \quad \text{where} \quad I_S = J_S \times A = \frac{qn_i^2 \bar{D}_n}{G} \times A$$

The transport current can be separated into *forward* and *reverse* components as

$$I_T = I_S \left( e^{V_{BE}/U_T} - 1 \right) - I_S \left( e^{V_{BC}/U_T} - 1 \right) = I_{CF} + I_{ER}$$

- If  $V_{BE} > 0$  and  $V_{BC} < 0$ , the device is biased in the *forward-active region*,

$$I_T = I_S e^{V_{BE}/U_T}$$

- If  $V_{BE} < 0$  and  $V_{BC} > 0$ , the device is biased in the *inverse-active region*,

$$I_T = I_S e^{V_{BC}/U_T}$$

- If  $V_{BE} > 0$  and  $V_{BC} > 0$ , the device is biased in the *saturation region*.

# Base Current

---

In the forward-active region

$$I_B = I_{BB} + I_{BE}$$

- $I_{BB}$  is due to the recombination of holes and electrons in the base.
- $I_{BE}$  is due to the injection of holes from the base into the emitter.

Define  $Q_e$  as the minority carrier charge in the base region

$$Q_e = qA \int_0^{W_B} n_b(x) dx \quad \text{or} \quad Q_e = \frac{1}{2} qAW_B n_b(0) = \frac{1}{2} qAW_B \frac{n_i^2}{N_A} e^{V_{BE}/U_T}$$

$I_{BB}$  is related to  $Q_e$  by the lifetime of minority carriers in the base,  $\tau_b$

$$I_{BB} = \frac{Q_e}{\tau_b} = \frac{1}{2} \frac{qAW_B}{\tau_b} \frac{n_i^2}{N_A} \cdot e^{V_{BE}/U_T}$$

## Base Current

---

$I_{BE}$  depends on the gradient of minority carriers (holes) in the emitter.

- For a “long-base” emitter (all minority carriers recombine in the quasi-neutral region) with a diffusion length  $L_p$

$$I_{BE} = \frac{qAD_p}{L_p} p_{e0} e^{V_{BE}/U_T} = \frac{qAD_p}{L_p} \frac{n_i^2}{N_D} e^{V_{BE}/U_T} \quad N_D = \text{Emitter Donor Density}$$

- For a “short-base” emitter (all recombination at the contact) with emitter width  $W_E$ ,  $W_E$  simply replaces  $L_p$  in the expression for  $I_{BE}$ .

The total base current in the forward-active region is

$$I_B = \left[ \frac{1}{2} \frac{qAW_B}{\tau_B} \frac{n_i^2}{N_A} + \frac{qAD_p}{L_p} \frac{n_i^2}{N_D} \right] e^{V_{BE}/U_T}$$

- In modern narrow-base transistors  $I_{BE} \gg I_{BB}$ .

## Forward Current Gain

---

In the forward-active region, the *forward current gain* is

$$\beta_F \equiv \frac{I_C}{I_B} = \frac{1}{\frac{W_B^2}{2\tau_b D_n} + \frac{D_p W_B N_A}{D_n L_P N_D}}$$

The emitter current is

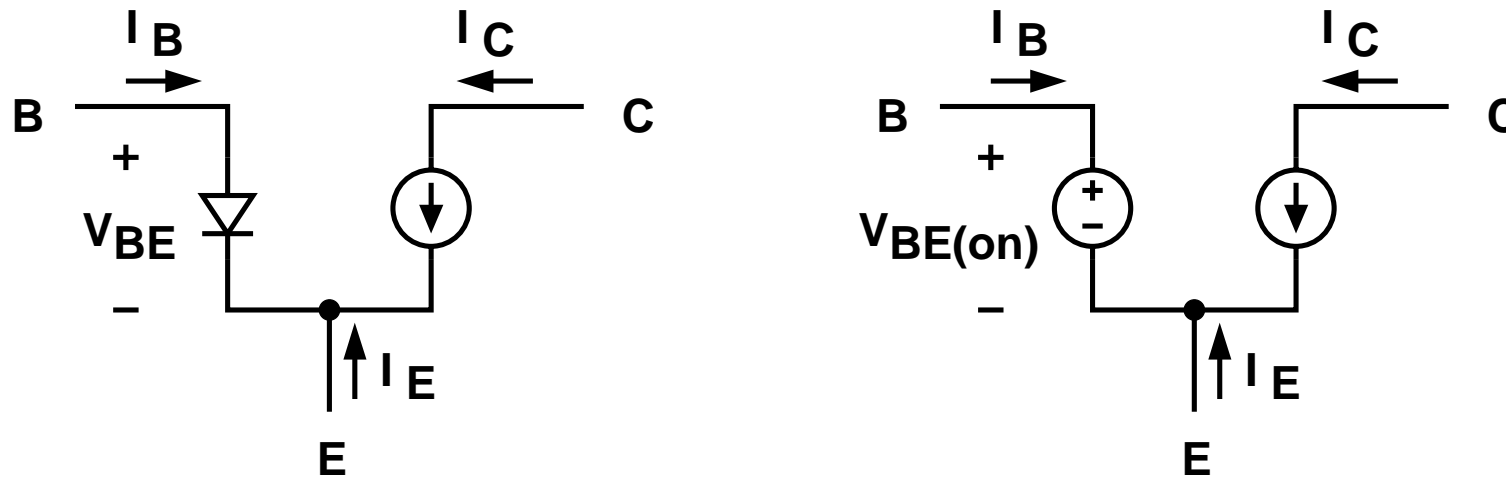
$$I_E = -(I_C + I_B) = -\left(I_C + \frac{I_C}{\beta_F}\right) = -\frac{I_C}{\alpha_F}$$

where

$$\alpha_F \equiv -\frac{I_C}{I_E} = \frac{\beta_F}{\beta_F + 1} = \frac{1}{1 + \frac{1}{\beta_F}} = \frac{1}{1 + \frac{W_B^2}{2\tau_b D_n} + \frac{D_p W_B N_A}{D_n L_P N_D}} \approx \alpha_T \cdot \gamma$$
$$\alpha_T = \frac{1}{1 + \frac{W_B^2}{2\tau_B D_n}} \quad \gamma = \frac{1}{1 + \frac{D_p W_B N_A}{D_n L_P N_D}}$$

- $\alpha_T$  is called the *base transport factor*, and  $\gamma$  is called the *emitter injection efficiency*.

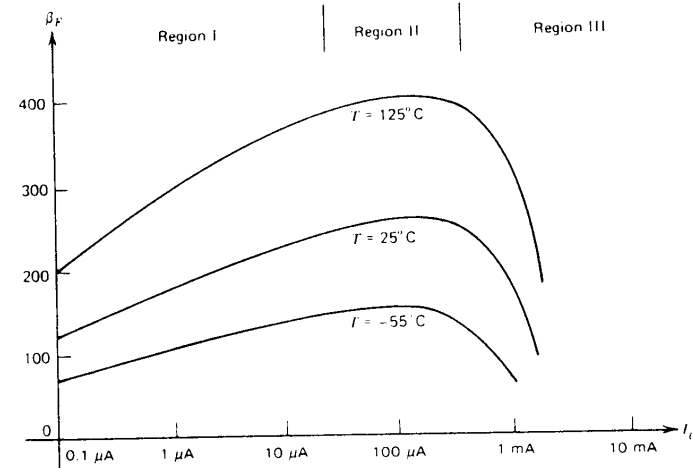
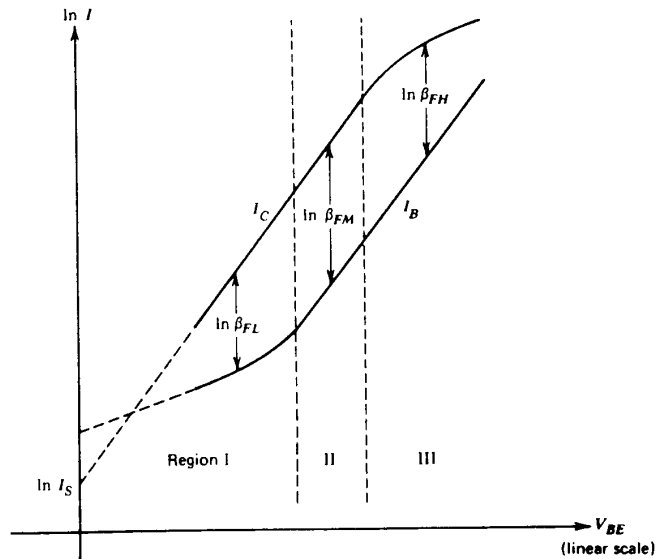
# BJT DC Large-Signal Model in Forward-Active Region



$$I_B = \frac{I_S}{\beta_F} e^{V_{BE}/U_T} \quad I_C = \beta_F I_B$$

- The voltage on the emitter junction can be approximated by a constant  $V_{BE(on)}$ .
- $V_{BE(on)}$  is usually 0.6 V to 0.8 V, and has a temperature coefficient of  $-2 \text{ mV}/^\circ\text{C}$ .

# Dependence of $\beta_F$ on Operating Condition



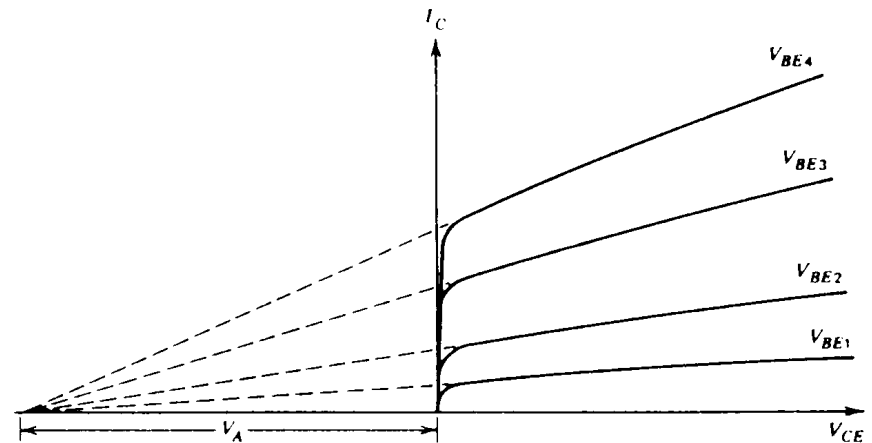
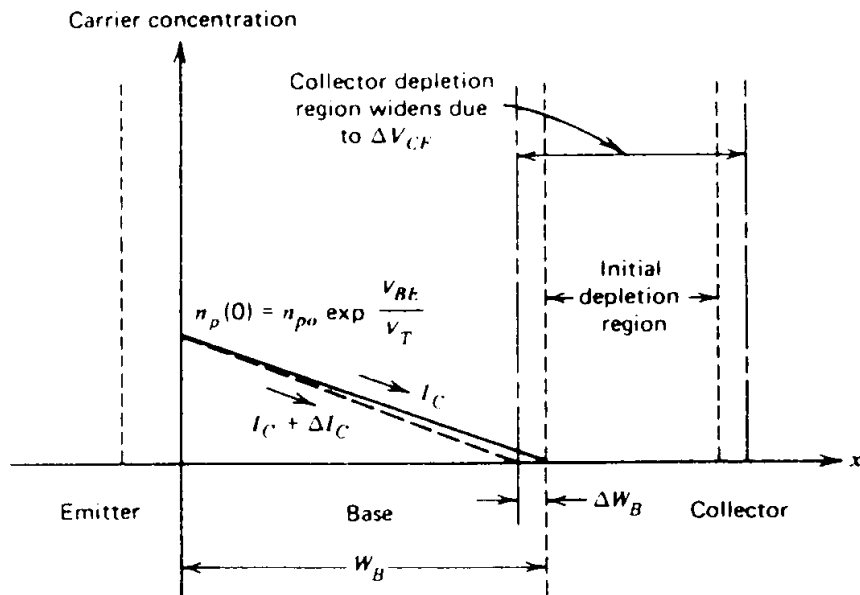
- At high currents, due to high-level injection

$$I_C \rightarrow I_S e^{V_{BE}/(2U_T)}$$

- At low currents, due to recombination in the B-E depletion region

$$I_B \rightarrow I_S e^{V_{BE}/(2U_T)}$$

# Collector Voltage Effects



In the forward-active region, an increase  $\Delta V_{CE}$  in  $V_{CE}$  results in an increase in the collector depletion layer width, thereby reducing  $W_B$  by  $\Delta W_B$ , and increasing  $I_C$ .

$$I_C = I_S e^{V_{BE}/U_T} = A \frac{qn_i^2 D_n}{G} e^{V_{BE}/U_T} \quad G = \text{Gummel number}$$

$$\frac{\partial I_C}{\partial V_{CE}} = -A \frac{qn_i^2 D_n}{G^2} e^{V_{BE}/U_T} \cdot \frac{dG}{dV_{CE}} = -\frac{I_C}{G} \cdot \frac{dG}{dV_{CE}}$$

# Collector Voltage Effects

---

For a uniform-base transistor

$$G = W_B N_A \quad \text{and} \quad \frac{\partial I_C}{\partial V_{CE}} = -\frac{I_C}{W_B} \cdot \frac{dW_B}{dV_{CE}}$$

- $dW_B/dV_{CE}$  is typically a weak function of  $V_{CE}$  for a reverse biased collector junction and is often assumed to be constant.

The *Early voltage*,  $V_A$ , is given by

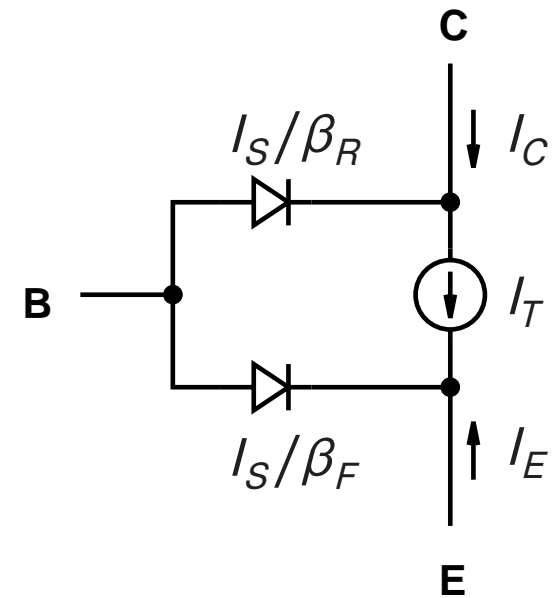
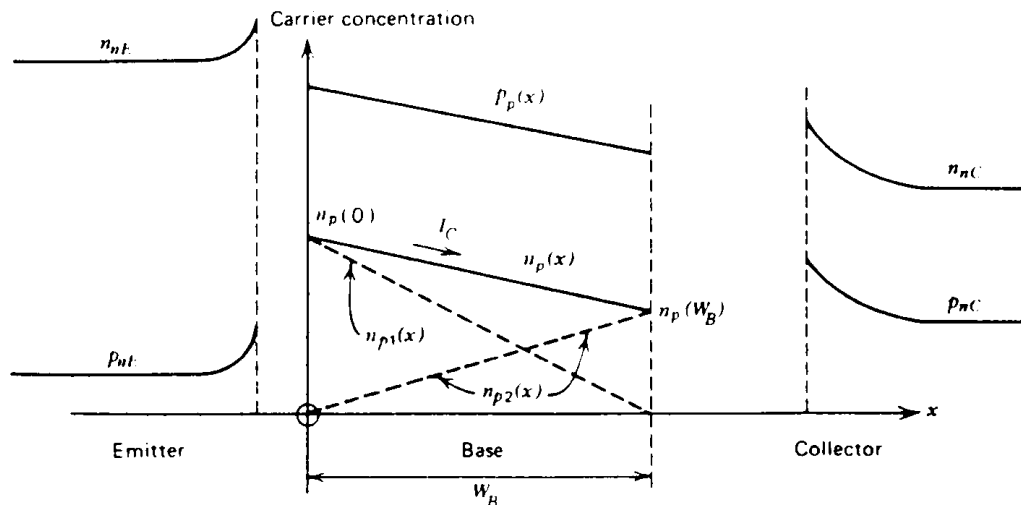
$$V_A = \frac{I_C}{\partial I_C / \partial V_{CE}} = -W_B \frac{1}{dW_B / dV_{CE}}$$

The influence of changes in  $V_{CE}$  on  $I_C$  can thus be represented as

$$I_C = I_S e^{V_{BE}/U_T} \left( 1 + \frac{V_{CE}}{V_A} \right)$$

- Typical values of  $V_A$  are 15–100 V.

# Base Transport Model



$$I_T = I_S \left( e^{V_{BE}/U_T} - e^{V_{BC}/U_T} \right)$$

$$I_C = I_T - \frac{I_S}{\beta_R} \left( e^{V_{BC}/U_T} - 1 \right) \quad I_E = -I_T - \frac{I_S}{\beta_F} \left( e^{V_{BE}/U_T} - 1 \right)$$

$$I_B = \frac{I_S}{\beta_F} \left( e^{V_{BE}/U_T} - 1 \right) + \frac{I_S}{\beta_R} \left( e^{V_{BC}/U_T} - 1 \right)$$

# Ebers-Moll Model

---

Recalling

$$I_T = I_S \left( e^{V_{BE}/U_T} - e^{V_{BC}/U_T} \right)$$
$$I_C = I_T - \frac{I_S}{\beta_R} \left( e^{V_{BC}/U_T} - 1 \right) \quad I_E = -I_T - \frac{I_S}{\beta_F} \left( e^{V_{BE}/U_T} - 1 \right)$$

SPICE uses the base transport model with the equations rewritten as:

$$I_C = I_S \left( e^{V_{BE}/U_T} - 1 \right) - I_S \left( 1 + \frac{1}{\beta_R} \right) \left( e^{V_{BC}/U_T} - 1 \right) = I_S \left( e^{V_{BE}/U_T} - 1 \right) - \frac{I_S}{\alpha_R} \left( e^{V_{BC}/U_T} - 1 \right)$$

$$I_E = -I_S \left( 1 + \frac{1}{\beta_F} \right) \left( e^{V_{BE}/U_T} - 1 \right) - I_S \left( e^{V_{BC}/U_T} - 1 \right) = -\frac{I_S}{\alpha_F} \left( e^{V_{BE}/U_T} - 1 \right) - I_S \left( e^{V_{BC}/U_T} - 1 \right)$$

- Note that, in the classical Ebers-Moll model, parameters  $I_{ES}$  and  $I_{CS}$  are defined such that

$$\alpha_F I_{ES} = \alpha_R I_{CS} = I_S$$

# Leakage Current

---

In the forward-active region,  $e^{V_{BE}/U_T} \gg 1$  and  $e^{V_{BC}/U_T} \ll 1$ , then

$$I_C \approx I_S e^{V_{BE}/U_T} + \frac{I_S}{\alpha_R} \quad I_E \approx -\frac{I_S}{\alpha_F} e^{V_{BE}/U_T} - I_S$$

thus

$$I_S e^{V_{BE}/U_T} = -\alpha_F I_E - \alpha_F I_S$$

and

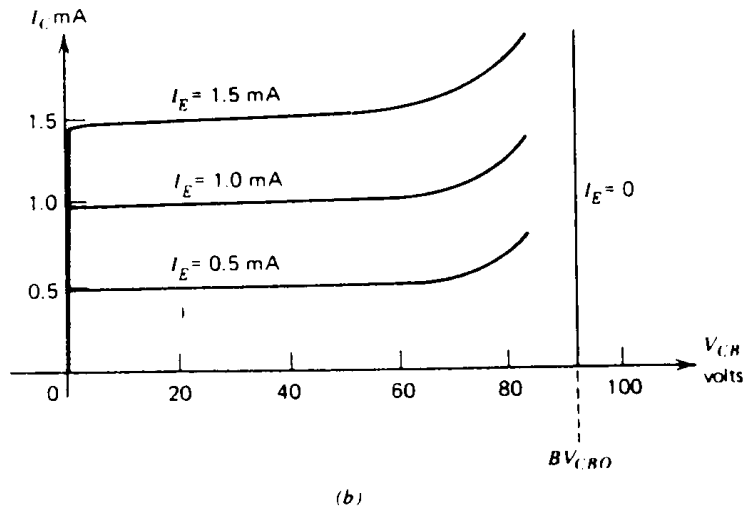
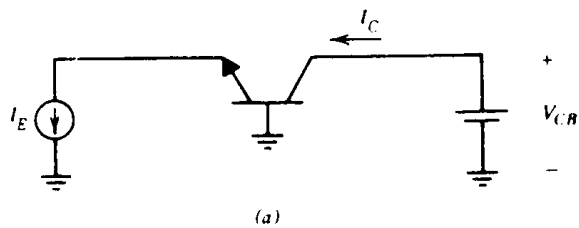
$$I_C = -\alpha_F I_E + \left( \frac{1}{\alpha_R} - \alpha_F \right) I_S = -\alpha_F I_E + I_{CO}$$

where

$$I_{CO} \equiv (1 - \alpha_F \alpha_R) \frac{I_S}{\alpha_R}$$

- $I_{CO}$  is the collector-base leakage current with the emitter open.
- In practice, because of surface leakage effects,  $I_{CO}$  is several orders of magnitude larger than the value predicted by the above definition.

# Common-Base Transistor Breakdown



- Avalanche multiplication at the junctions of a BJT limits the voltage that can be sustained.

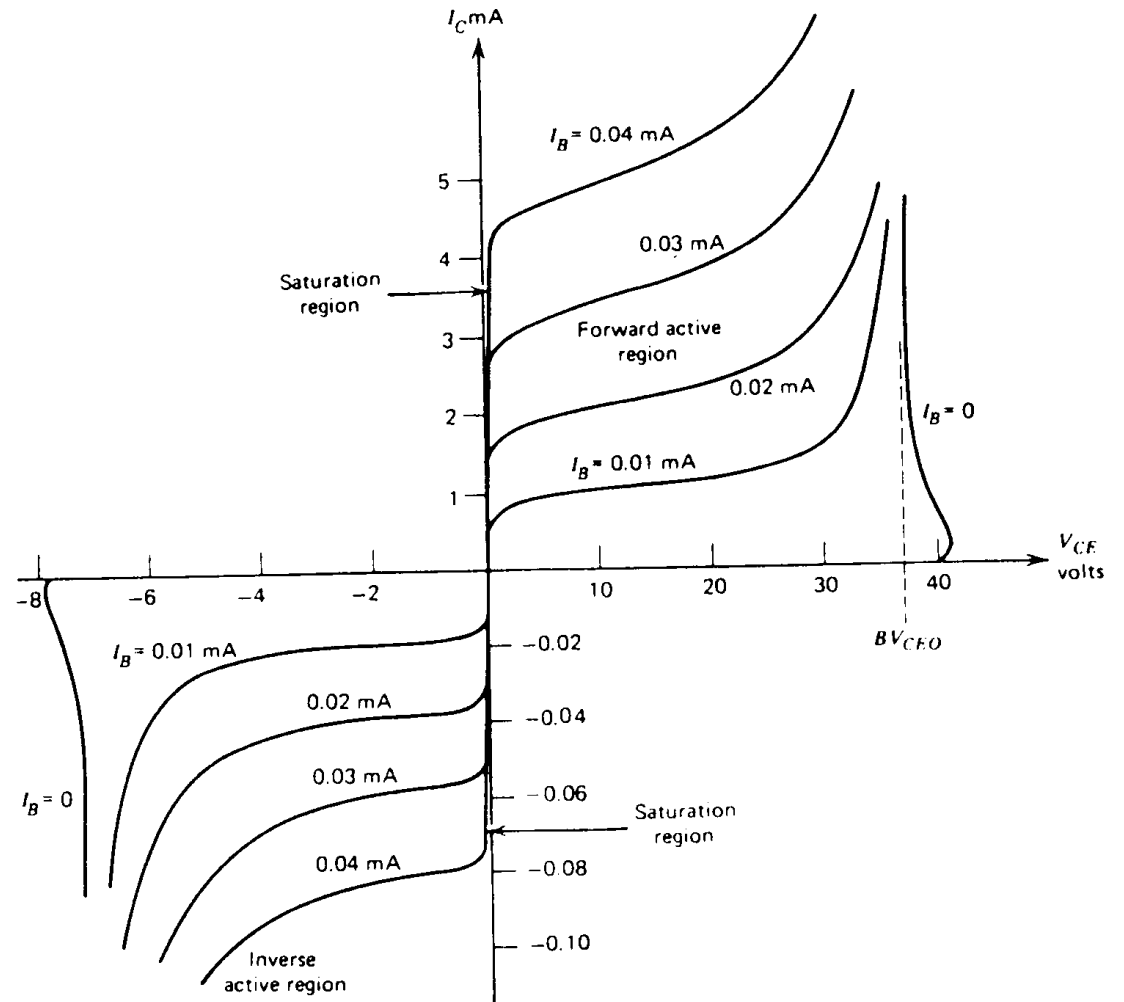
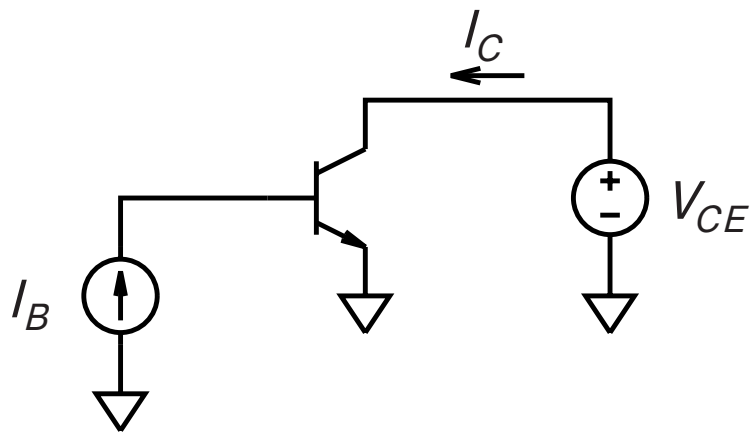
- $BV_{CBO}$  is the breakdown voltage of C-B junction with  $I_E = 0$ .

$BV_{EBO}$  is much less than  $BV_{CBO}$ .

Neglecting leakage currents

$$I_C = -\alpha_F I_E M \quad \text{where} \quad M = \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n}$$

# Common-Emitter Transistor Breakdown



## Common-Emitter Transistor Breakdown

---

In this configuration, holes generated in the avalanche process are swept into the base where they act as a supply of base current. The avalanche current is thus effectively amplified by  $\beta_F$ .

$$I_B = -(I_C + I_E) = -I_C + \frac{I_C}{M\alpha_F} \Rightarrow I_C = \left( \frac{M\alpha_F}{1 - M\alpha_F} \right) I_B$$

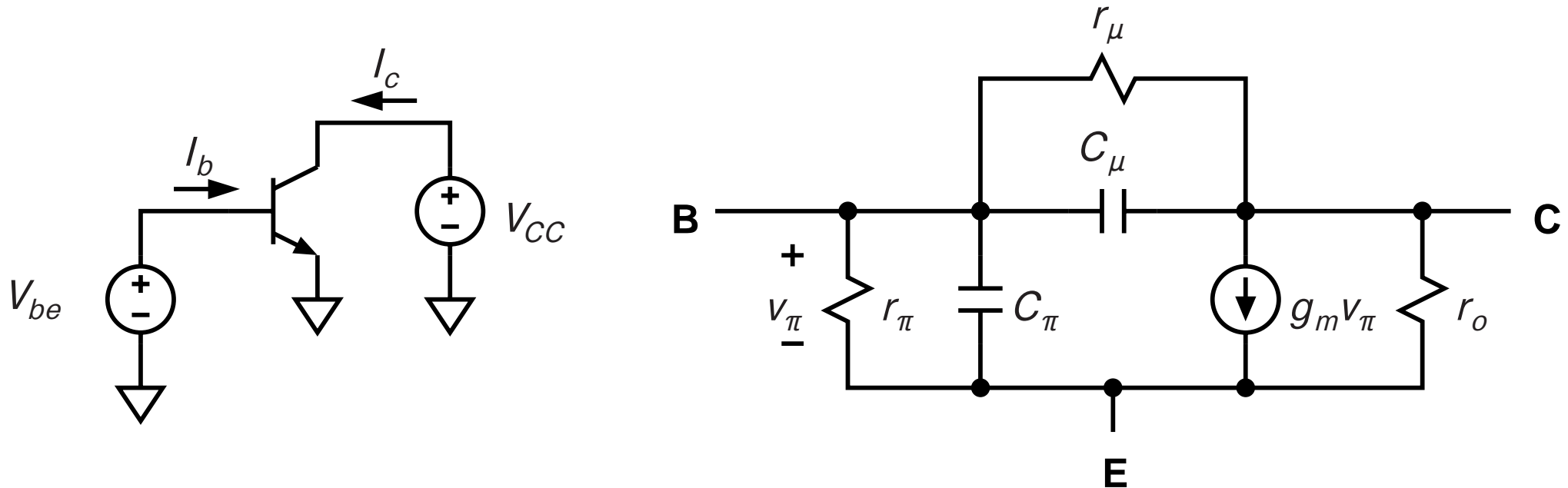
where  $M$  is as defined above for the common-base case.

$BV_{CEO}$  is defined as the value of  $V_{CE}$  for which  $I_C \rightarrow \infty$ ; that is, for which  $M\alpha_F \rightarrow 1$ . Assume  $V_{CB} \approx V_{CE}$ , then

$$M\alpha = \frac{\alpha_F}{1 - \left( \frac{BV_{CEO}}{BV_{CBO}} \right)^n} = 1 \Rightarrow \frac{BV_{CEO}}{BV_{CBO}} = (1 - \alpha_F)^{1/n} = \frac{1}{(\beta_F + 1)^{1/n}} \approx \frac{1}{\beta_F^{1/n}}$$

- Note: Here must use value of  $BV_{CBO}$  for intrinsic transistor. Actual  $BV_{CBO}$  is lower than this because of sidewall effects.

# Small-Signal Model of Forward-Biased BJT



In the forward-active region

$$I_C = I_S e^{V_{BE}/U_T} \left( 1 + \frac{V_{CE}}{V_A} \right) \quad I_B = \frac{I_C}{\beta_F}$$

Bias and small-signal variables are:

$$I_b = I_B + i_b \quad I_c = I_C + i_c \quad V_{be} = V_{BE} + v_{be}$$

# Small-Signal Model of Forward-Biased BJT

$$g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{qI_C}{kT} = \frac{I_C}{U_T}$$

$$\beta_o = \frac{\partial I_C}{\partial I_B} = \left[ \frac{\partial}{\partial I_C} \left( \frac{I_C}{\beta_F} \right) \right]^{-1}$$

$$g_\pi = \frac{\partial I_B}{\partial V_{BE}} = \frac{1}{r_\pi} = \frac{1}{\beta_o} \frac{\partial I_C}{\partial V_{BE}} = \frac{g_m}{\beta_o}$$

$$g_o = \frac{\partial I_C}{\partial V_{CE}} = \frac{I_C}{V_A} = \eta g_m$$

$$g_\mu = \frac{\partial I_{BB}}{\partial V_{CB}} = \frac{\partial I_{BB}}{\partial I_C} \frac{\partial I_C}{\partial V_{CB}} = \frac{1}{r_\mu}$$

$$C_\pi = C_b + C_{je} = \tau_F g_m + C_{je}$$

$$C_\mu = C_{jc}$$

- If  $\beta_F$  is constant, then  $\beta_o = \beta_F$ .

- $\eta \equiv \frac{U_T}{V_A}$ .

- If  $I_B = I_{BB}$

$$g_\mu \approx \frac{\partial I_B}{\partial I_C} \frac{\partial I_C}{\partial V_{CE}} = \frac{g_o}{\beta_o} \quad \text{or} \quad r_\mu = \beta_o r_o$$

- Typically,  $r_\mu > 10\beta_o r_o$ .  
For lateral pnp,  $r_\mu$  is  $2\beta_o r_o \sim 5\beta_o r_o$ .

- *Junction capacitances are*

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V}{\psi_0}\right)^n} \quad n = 0.2 \sim 0.5$$

# Charge Storage

---

In the intrinsic transistor charge is stored in the junction capacitances,  $C_{je}$  and  $C_{jc}$ , and as minority carriers in the base ( $Q_e$ ) and emitter ( $Q_p$ ).

- Both  $Q_e$  and  $Q_p$  are proportional to  $e^{V_{BE}/U_T}$ .
- $Q_e \gg Q_p$  and typically the effect of  $Q_p$  is taken into account simply by modifying  $Q_e$ .

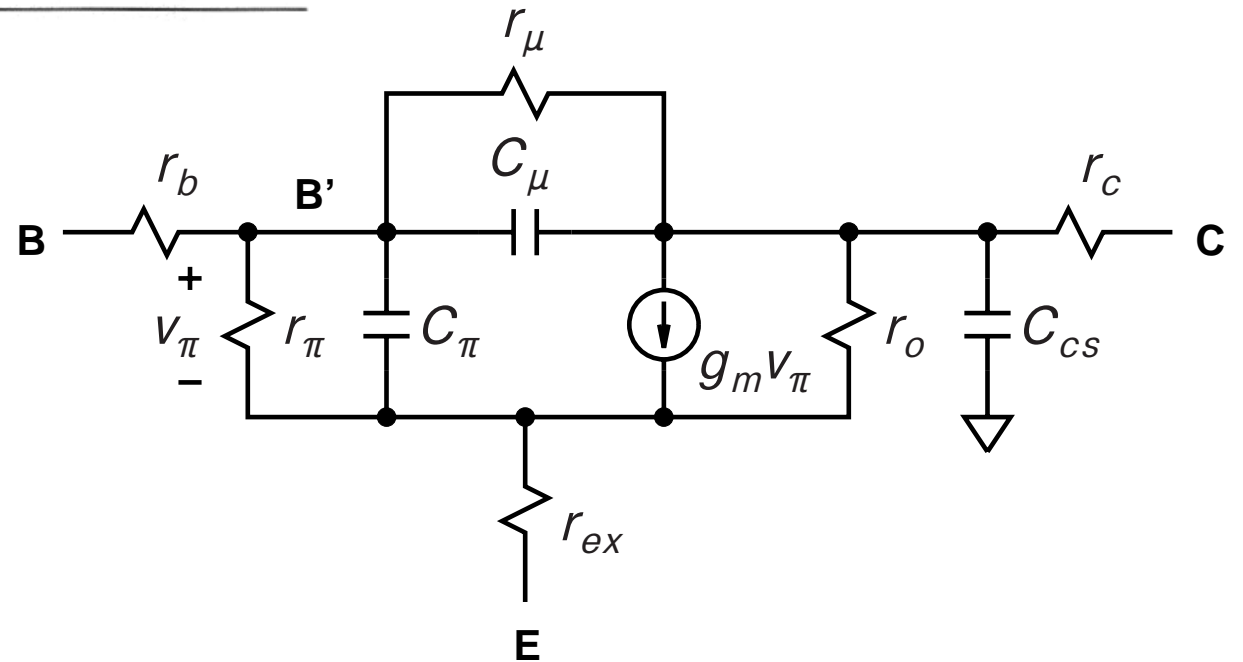
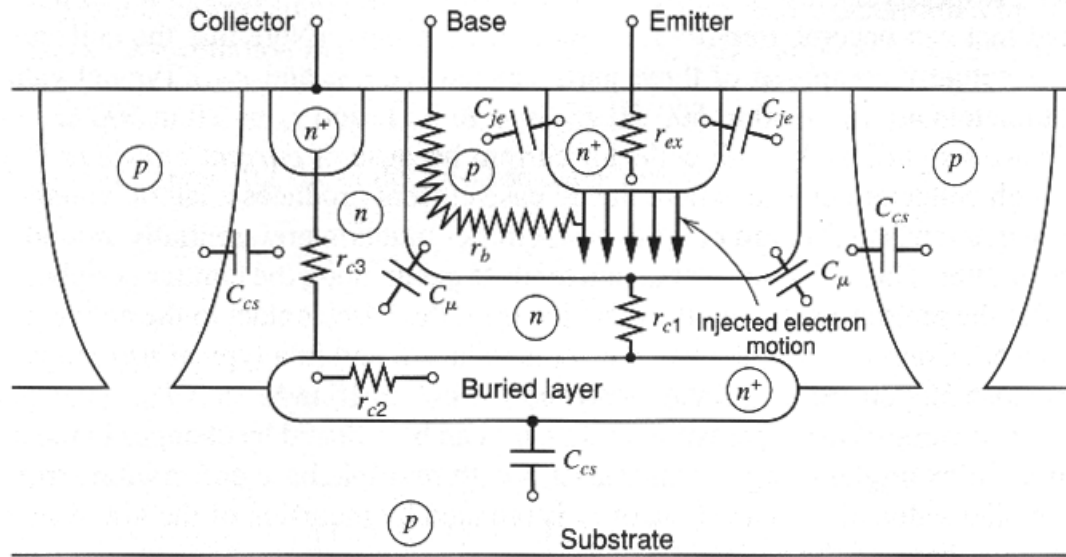
An equivalent *forward base transit time*,  $\tau_F$ , is defined as

$$\tau_F \equiv \frac{Q_e}{I_C} \quad \tau_F = \frac{W_B^2}{2D_n} \quad \text{for uniform-base transistor}$$

The *diffusion capacitance* is

$$C_b = \frac{\partial Q_e}{\partial V_{BE}} = \tau_F \frac{\partial I_C}{\partial V_{BE}} = \tau_F g_m$$

# Complete Small-Signal Model with Extrinsic Components

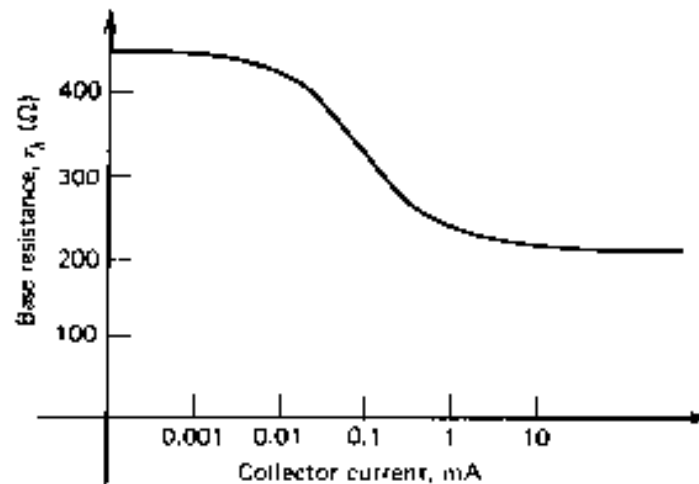


# Typical values of Extrinsic Components

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$r_b$	50–500 $\Omega$
$r_c$	20–500 $\Omega$
$r_{ex}$	1–8 $\Omega$
$C_{CS}$	0.2–3 pF

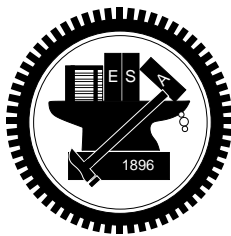
The value of  $r_b$  varies significantly with  $I_C$  because of *current crowding*.



# MOS Field-Effect Transistors

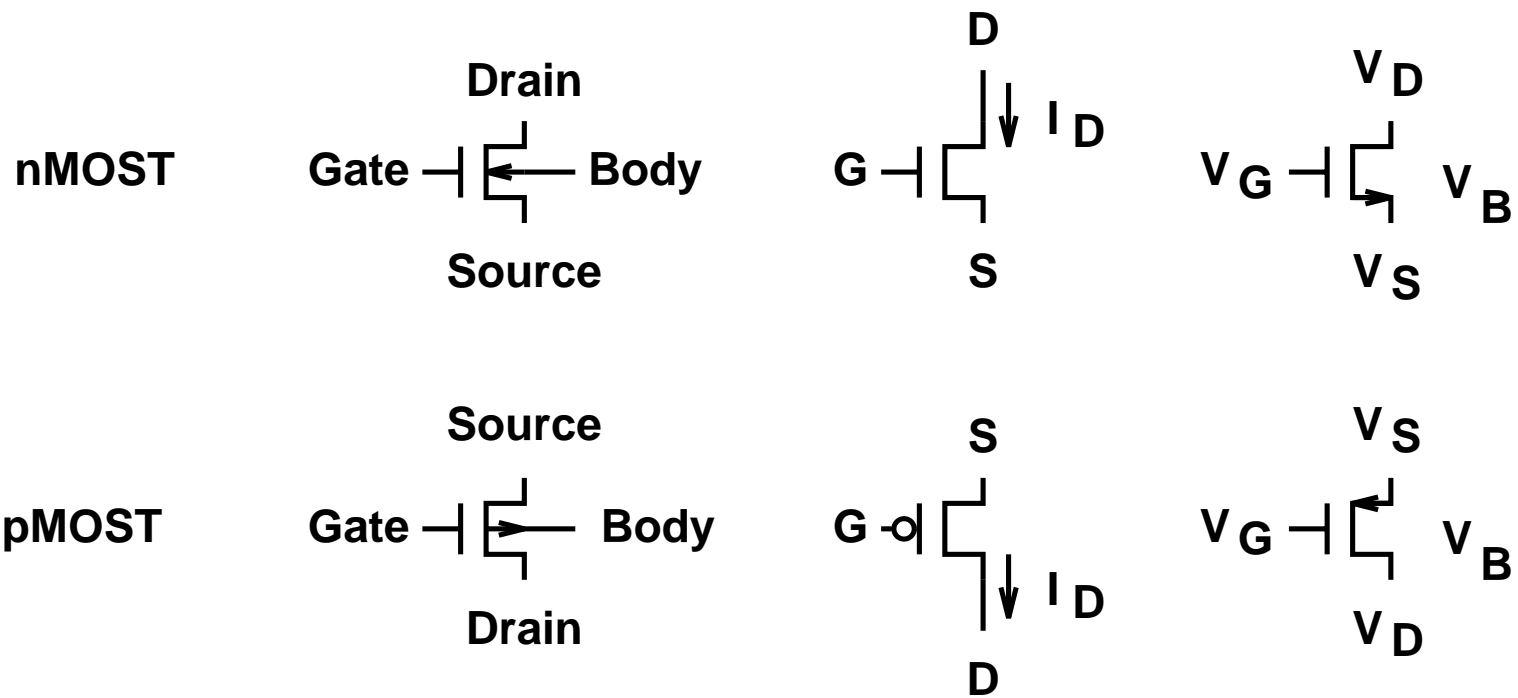
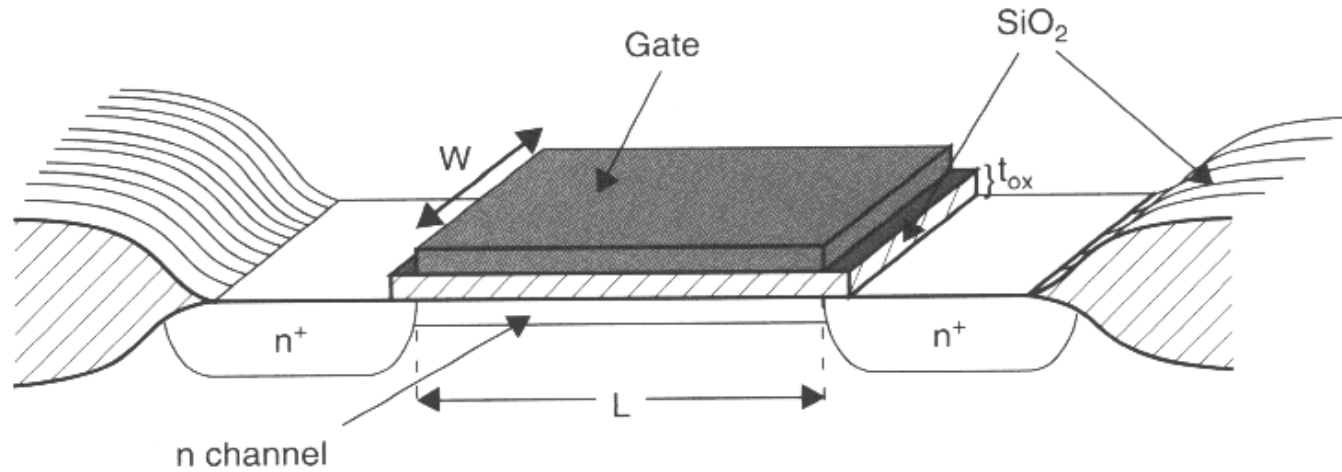
Jieh-Tsorng Wu

October 8, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# MOS Transistors

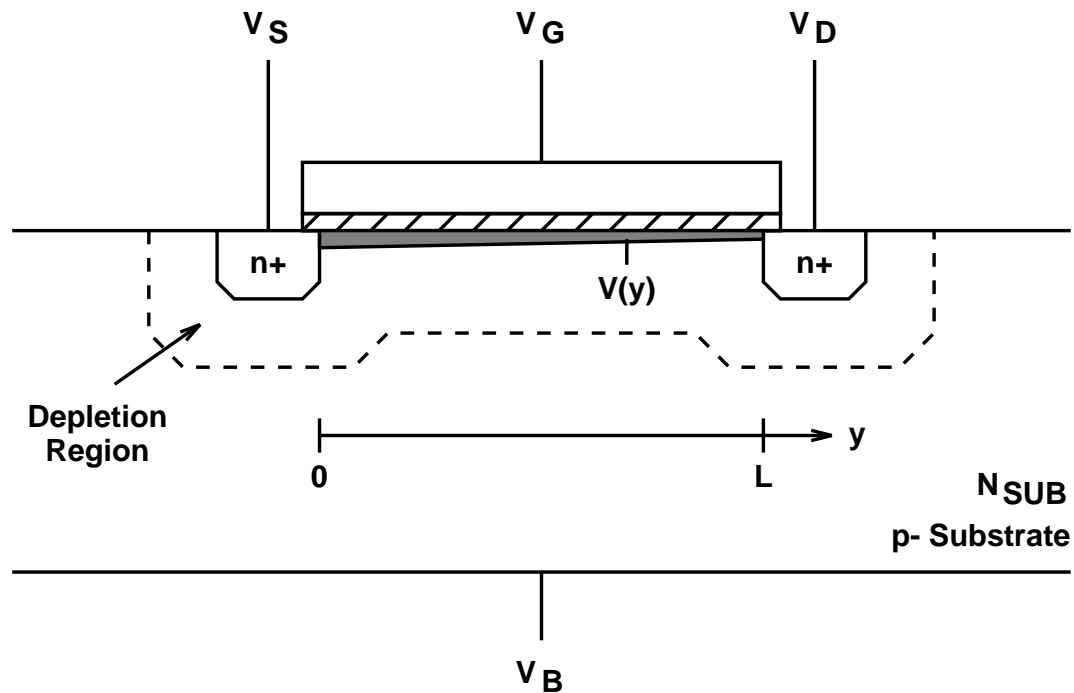


# MOS Transistors

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- $L_{electrical} = L_{gate} - 2L_D$ . In SPICE,  $L = L_{gate}$ .
- For nMOST,  $V_D > V_S > V_B$ .
- For pMOST,  $V_D < V_S < V_B$ .
- The  $I - V$  equations of nMOST are identical to those of pMOST.
- For enhancement-mode device,  $V_{tn} > 0$  and  $V_{tp} < 0$ .

# Strong Inversion



The *threshold voltage* of  $V_{GB}$  for strong inversion is

$$V_t(y) = V(y) + 2\phi_f + \gamma \sqrt{V(y) + 2\phi_f} + V_{FB}$$

$$2\phi_f = 2 \frac{kT}{q} \ln \left( \frac{N_{SUB}}{n_i} \right) \quad \gamma = \frac{\sqrt{2q\epsilon_{si}N_{SUB}}}{C_{ox}} \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

# Channel Charge Transfer Characteristics

---

The induced *channel charge* per unit area is

$$Q_I(y) = C_{ox} [V_{GB} - V_t(y)] \quad \text{when } V_{GB} > V_t(y)$$

The current along the channel is

$$I_D = W \cdot \mu Q_I(y) \cdot \mathcal{E}(y) = W \cdot \mu Q_I(y) \cdot \frac{dV}{dy} \quad \Rightarrow \quad I_D dy = W \mu Q_I(y) dV$$

Integration along the channel from 0 to  $L$  gives

$$\int_0^L I_D dy = \int_{V_{SB}}^{V_{DB}} W \mu C_{ox} [V_{GB} - V_t(y)] dV$$

$$I_D = \mu C_{ox} \frac{W}{L} \left\{ (V_{GB} - 2\phi_f - V_{FB})V(y) - \frac{1}{2}V^2(y) - \frac{2}{3}\gamma[V(y) + 2\phi_f]^{3/2} \right\} \Big|_{V_{SB}}^{V_{DB}}$$

# Simplified Channel Charge Transfer Characteristics

---

The threshold voltage of  $V_{GS}$  for strong inversion is simplified as

$$V'_t(y) + V_{SB} = V'(y) + V_{SB} + V_t(SB) \quad \Rightarrow \quad V'_t(y) = V'(y) + V_t$$

The channel charge becomes

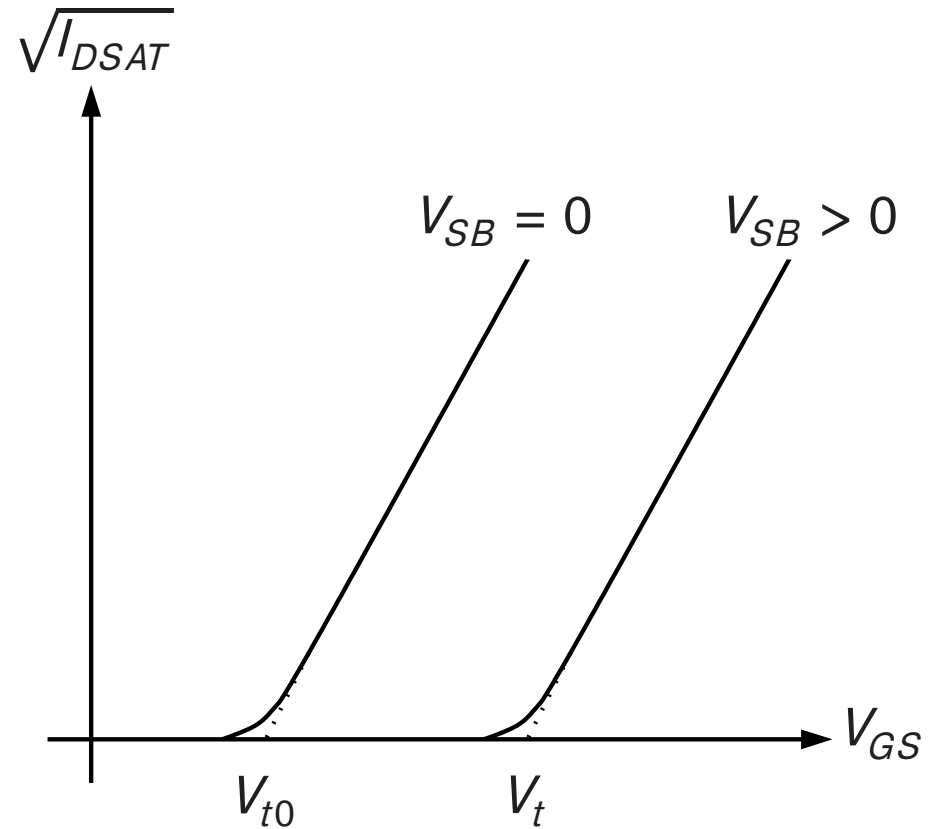
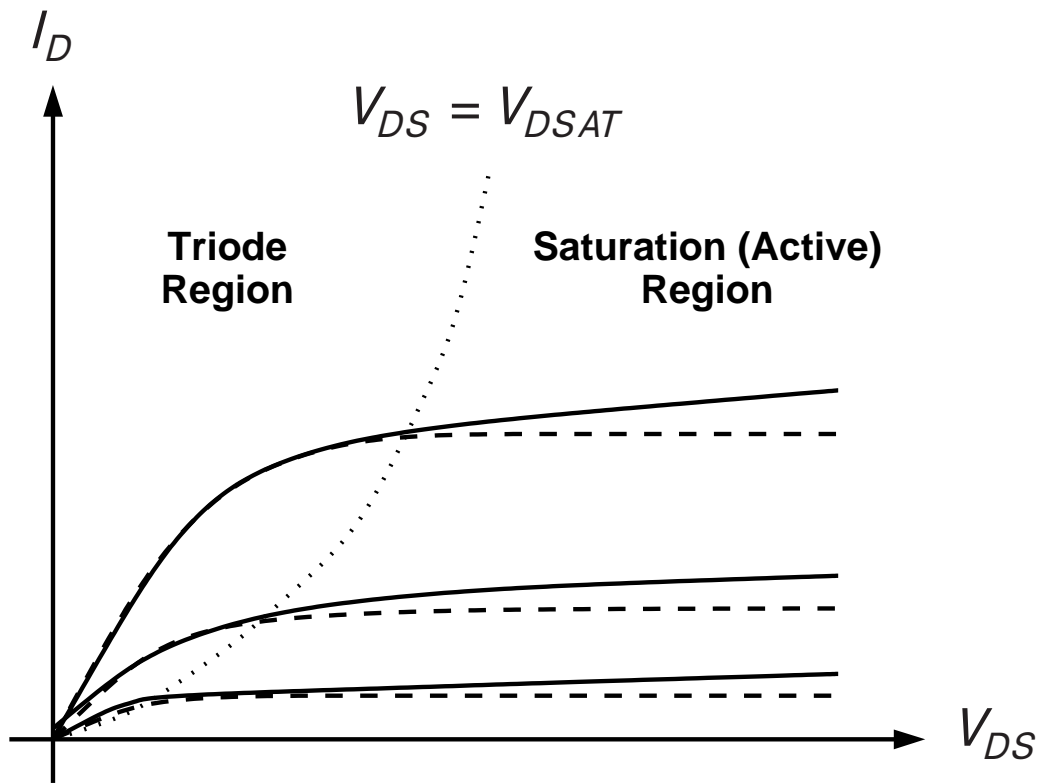
$$Q_I(y) = C_{ox} [V_{GS} - V'(y) - V_t]$$

And the drain current is

$$I_D = \mu C_{ox} \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] = k' \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

- $V_t$  is the threshold voltage of  $V_{GS}$  for strong inversion, and depends on  $V_{SB}$ .
- $k' = \mu C_{ox}$  is called the *process transconductance*.

# MOST I-V Characteristics



$$I_D = \mu C_{ox} \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad \text{for } V_{DS} \leq V_{DSAT} = V_{GS} - V_t$$

$$I_{DSAT} = I_D @ V_{DS} = V_{DSAT} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

# Threshold Voltage

---

$$V_t = V_{t0} + \gamma \left[ \sqrt{V_{SB} + 2\phi_f} - \sqrt{2\phi_f} \right] \quad \text{for } V_{SB} > 0$$

$V_{t0}$  is the threshold voltage when  $V_{SB} = 0$ .

$$V_{t0} = 2\phi_f + \gamma \sqrt{2\phi_f} + V_{FB} \quad \phi_f = \frac{kT}{q} \ln \left( \frac{N_{SUB}}{n_i} \right) \quad \gamma = \frac{\sqrt{2q\epsilon_{si}N_{SUB}}}{C_{ox}} \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

The Fermi level  $\phi_f$  is temperature dependent, i.e.,

$$\frac{d\phi_f}{dT} = -\frac{1}{T} \left[ \frac{E_{g0}}{2q} - \phi_f \right] \quad E_{g0} = \text{Silicon band gap at } T = 0^\circ\text{K}$$

The  $V_{t0}$ 's temperature coefficient is

$$\frac{dV_{t0}}{dT} = -\frac{1}{T} \left[ \frac{E_{g0}}{2q} - \phi_f \right] \left[ 2 + \frac{\gamma}{\sqrt{2\phi_f}} \right]$$

- $dV_{t0}/dT$  is usually in the range between  $-0.5 \text{ mV}/^\circ\text{C}$  to  $-4 \text{ mV}/^\circ\text{C}$ .

# Square-Law I-V Characteristics

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In triode region, 1st-order long-channel model is

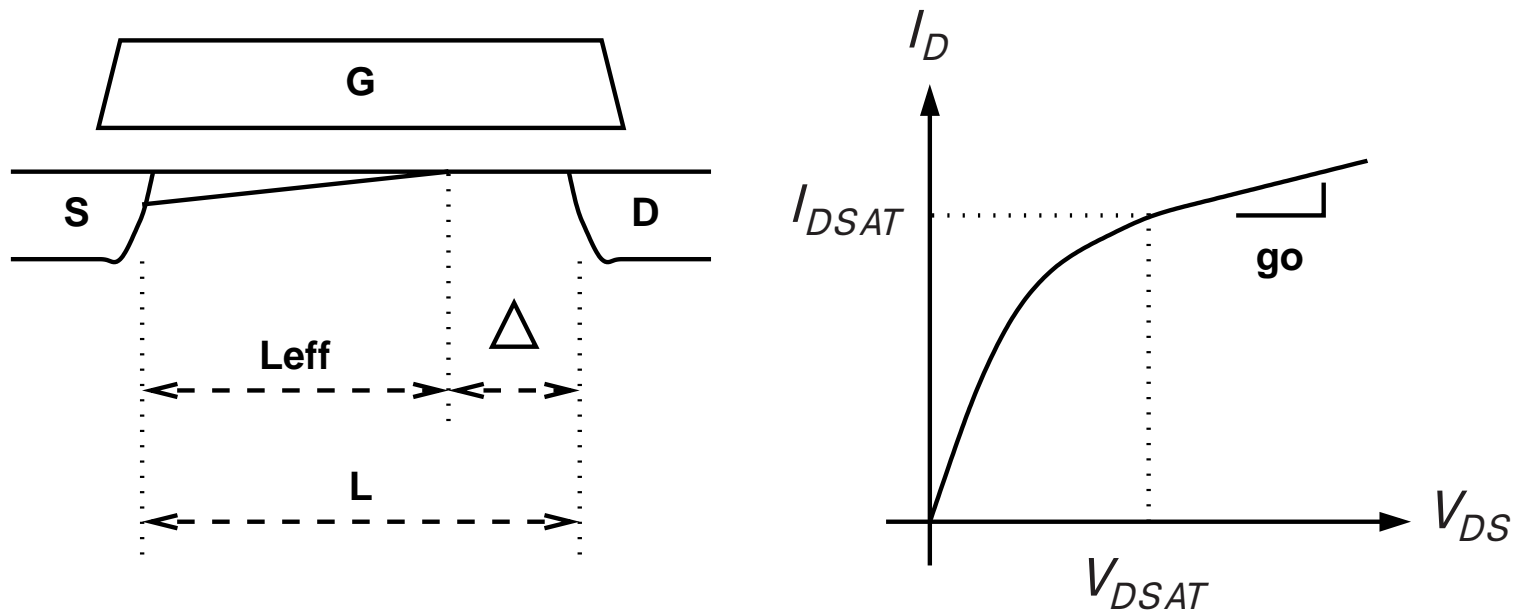
$$I_D = \mu C_{ox} \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] = k' \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

When  $V_{DS} \geq V_{DSAT} = V_{GS} - V_t$ , the MOST is in the *pinch-off* region (or *saturation* region),

$$I_{DS} = I_{DSAT} = I_D(V_{DS} = V_{GS} - V_t) = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{GS} - V_t)^2 = \frac{1}{2} k' \frac{W}{L} V_{ov}^2$$

- $k' = \mu C_{ox}$  is called the *process transconductance parameter*.
- $k = \beta = \mu C_{ox} \frac{W}{L}$  is called the *device transconductance parameter*.
- $V_{ov} = V_{GS} - V_t$  is called the *gate drive* or the *overdrive*.

# Channel-Length Modulation



$$I_{D(sat)} = \frac{1}{2} k' \frac{W}{L_{eff}} V_{ov}^2 \quad L_{eff} = L - \Delta \quad \Delta V_{DS} = V_{DS} - V_{DSAT}$$

Using one-dimensional abrupt PN junction model,

$$\Delta \approx \sqrt{\frac{2\epsilon_{si}}{qN_{SUB}}} \sqrt{V_{DS} - V_{DSAT} + \psi_0}$$

# Channel-Length Modulation

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The  $I_D$  variation due to  $V_{DS}$  can be written as:

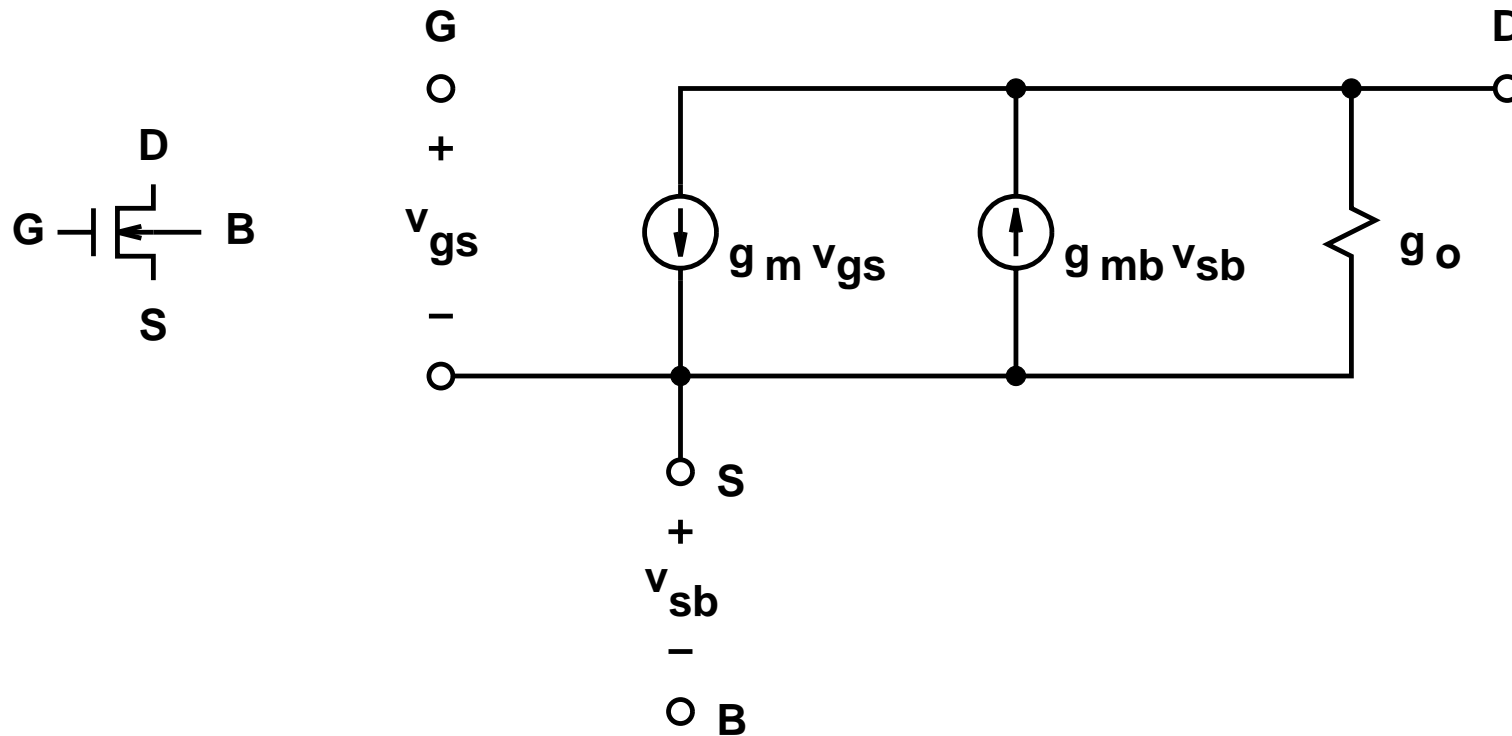
$$\frac{\partial I_D}{\partial V_{DS}} = \frac{\partial I_D}{\partial L_{eff}} \times \frac{\partial L_{eff}}{\partial V_{DS}} = -\frac{I_D}{L_{eff}} \times -\frac{1}{2} \sqrt{\frac{2\epsilon_{si}}{qN_{SUB}}} \frac{1}{\sqrt{V_{DS} - V_{DSAT} + \psi_0}} = I_D \cdot \lambda$$

The drain current in the pinch-off region can be approximated as

$$I_{D(sat)} = \frac{1}{2} k' \frac{W}{L} V_{ov}^2 (1 + \lambda V_{DS}) = \frac{1}{2} k' \frac{W}{L} V_{ov}^2 \left( 1 + \frac{V_{DS}}{V_A} \right)$$

- $\lambda$  is inversely proportional to  $L$ , i.e.,  $\lambda \propto 1/L$ .
- Typical values of  $\lambda$  are in the range  $0.05 \text{ V}^{-1}$  to  $0.005 \text{ V}^{-1}$ .
- The accurate calculation of  $\lambda$  from the device structure is quite difficult. Extraction from experimental data is usually necessary.

# MOST Small-Signal Model in Saturation Region



$$\text{Transconductance} = g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = k' \frac{W}{L} V_{ov} (1 + \lambda V_{DS}) = \sqrt{2k' \frac{W}{L} I_D (1 + \lambda V_{DS})} = \frac{I_D}{V_{ov}/2}$$

$$\text{Output Conductance} = g_o \equiv \frac{\partial I_D}{\partial V_{DS}} = \lambda I_D$$

# MOST Small-Signal Model in Saturation Region

---

$$\text{Body Transconductance} = g_{mb} \equiv -\frac{\partial I_D}{\partial V_{SB}} = -\frac{\partial I_D}{\partial V_t} \times \frac{\partial V_t}{\partial V_{SB}} = g_m \times \frac{\gamma}{2\sqrt{V_{SB} + 2\phi_f}}$$

Thus

$$g_{mb} = g_m \times \chi \quad \text{where} \quad \chi \equiv \frac{\gamma}{2\sqrt{V_{SB} + 2\phi_f}}$$

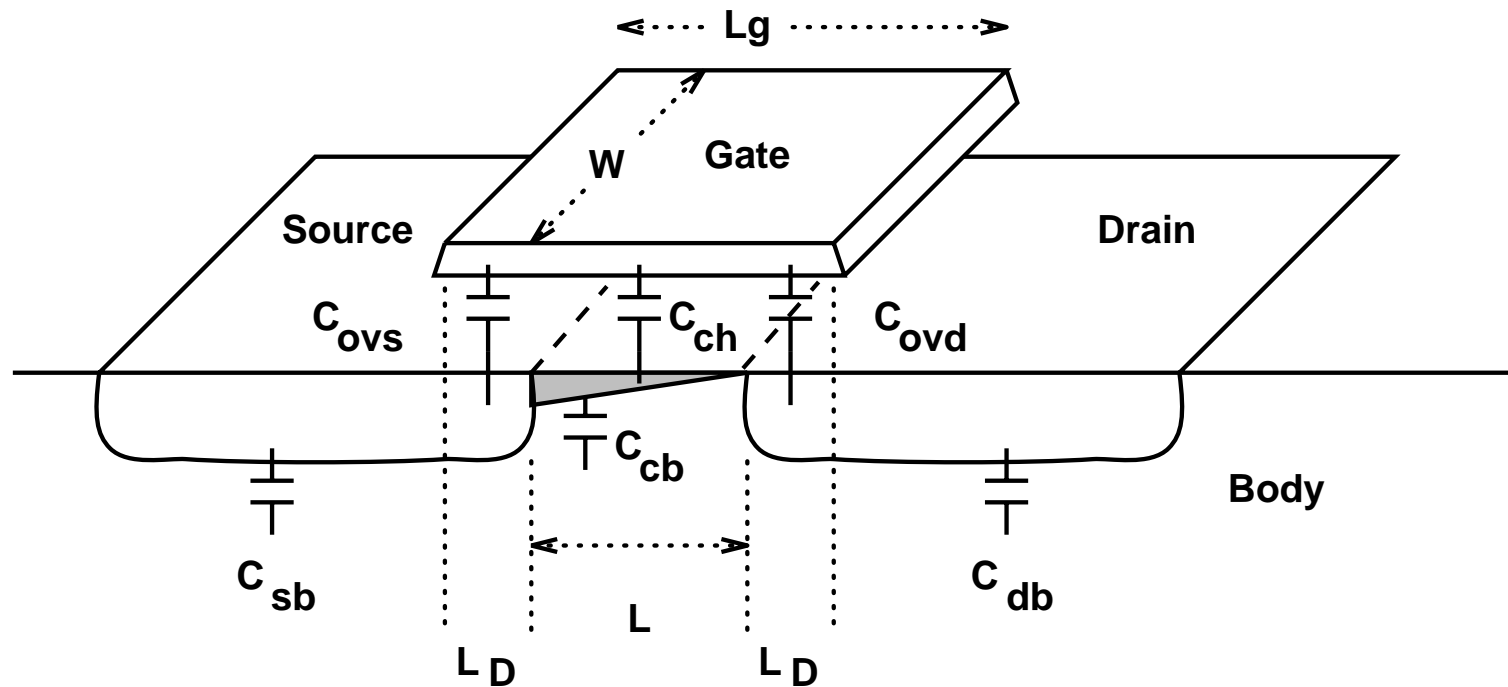
- The factor  $\chi$  is typically 0.1–0.3.
- Since  $\gamma = \sqrt{2q\epsilon_{si}N_{SUB}/C_{ox}}$

$$\chi = \left[ \epsilon_{si} / \sqrt{\frac{2\epsilon_{si}(V_{SB} + 2\phi_f)}{qN_{SUB}}} \right] \frac{1}{C_{ox}} = \frac{\epsilon_{si}/x_{dmax}}{C_{ox}} = \frac{C_{depl}}{C_{ox}}$$

$x_{dmax}$ : The width of depletion layer under channel.

$C_{depl}$ : The capacitance/area of depletion layer under channel.

# MOST Small-Signal Capacitances in Saturation Region



$$C_{sb} = AS \times C_J(V_{SB}) + PS \times C_{JSW}(V_{SB}) \quad C_{db} = AD \times C_J(V_{DB}) + PD \times C_{JSW}(V_{DB})$$

$$C'_{sb} = C_{sb} + C_{cb} \quad C_{cb} \approx WL \times C_J(V_{SB})$$

- $AS$  and  $AD$  are the areas of the source/drain junctions.
- $PS$  and  $PD$  are the source/drain perimeters excluding the sides adjacent to channel.

# MOST Small-Signal Capacitances in Saturation Region

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Junction Capacitances:

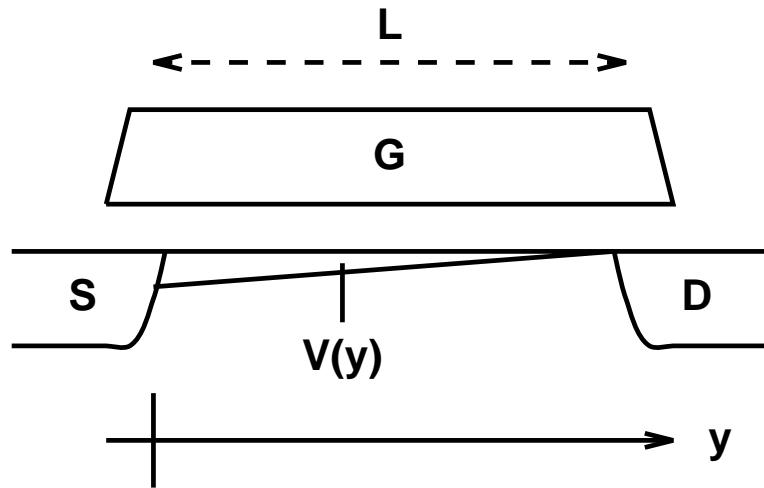
$$C_{sb} = \frac{C_{sbo}}{\left(1 + \frac{V_{SB}}{\psi_o}\right)^m} \quad C_{db} = \frac{C_{dbo}}{\left(1 + \frac{V_{DB}}{\psi_o}\right)^m} \quad m = \frac{1}{3} \sim \frac{1}{2}$$

Overlap Capacitances:

$$C_{ovs} = W \times C_{GSO} = W \times (nL_D C_{ox}) \quad C_{ovd} = W \times C_{GDO} = W \times (nL_D C_{ox})$$

$$1 \leq n \leq 2 \quad (\text{Due to fringing})$$

# Channel Capacitance in Saturation Region



$$Q_I(y) = C_{ox}[V_{GS} - V_t - V(y)] = C_{ox}[V_{ov} - V(y)]$$

$$I_D = W \cdot \mu Q_I(y) \cdot \mathcal{E}(y) = W \cdot \mu Q_I(y) \cdot \frac{dV}{dy}$$

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} V_{ov}^2$$

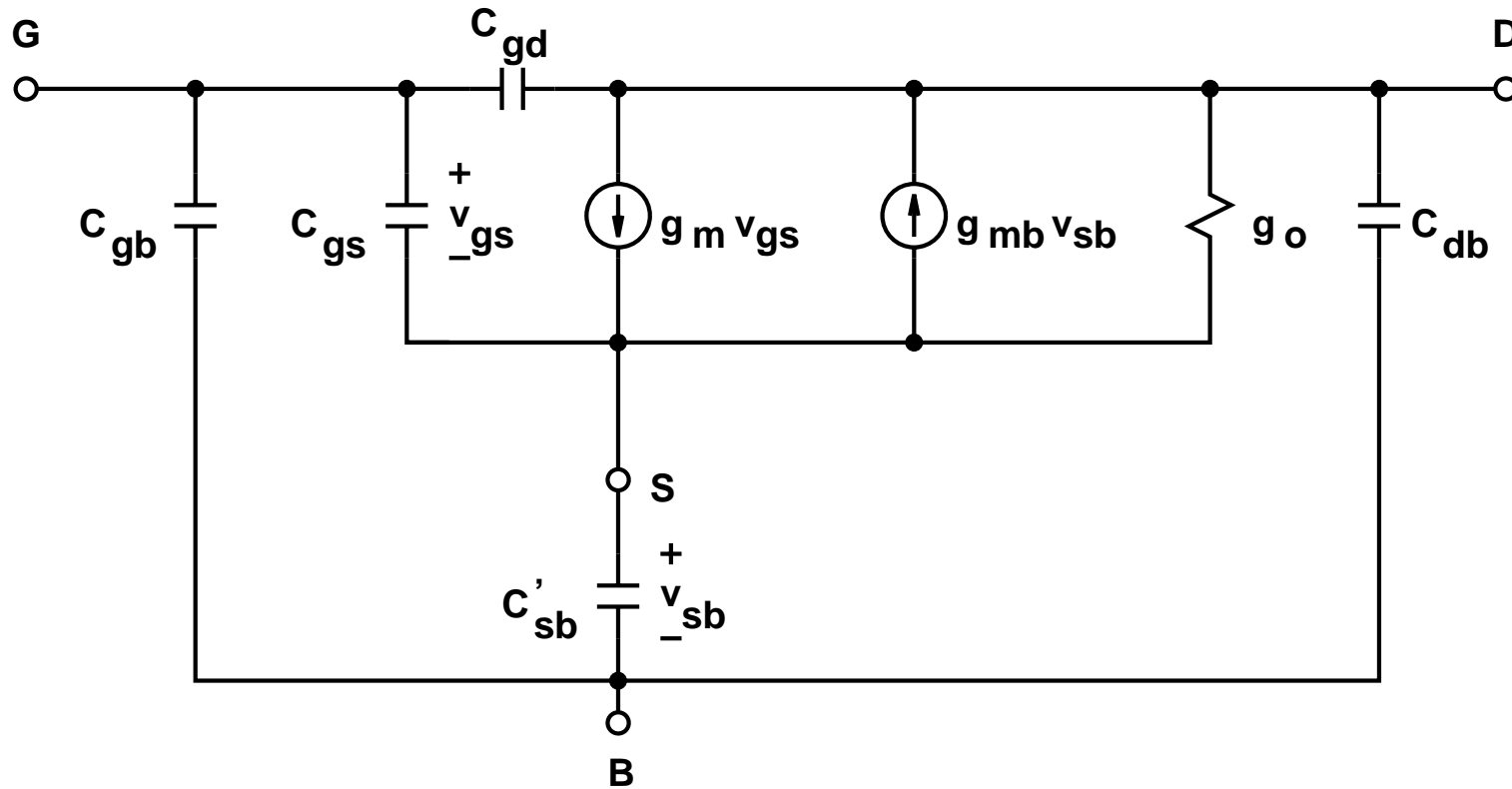
Let  $V_S = 0$  and  $\frac{I_D}{\mu C_{ox} W} \cdot dy = [(V_{GS} - V_t) - V(y)] \cdot dV$

Integration from 0 to  $y \Rightarrow \frac{1}{2} V_{ov}^2 \frac{y}{L} = V_{ov} V - \frac{1}{2} V^2(y) \Rightarrow V(y) = V_{ov} \left( 1 - \sqrt{1 - \frac{y}{L}} \right)$

Total Channel Charge =  $Q_T = \int_0^L Q_I(y) W dy = \frac{2}{3} W L C_{ox} V_{ov} = \frac{2}{3} W L C_{ox} (V_{GS} - V_t)$

Channel Capacitance =  $C_{ch} \equiv \frac{\partial Q_T}{\partial V_{GS}} = \frac{2}{3} W L C_{ox}$

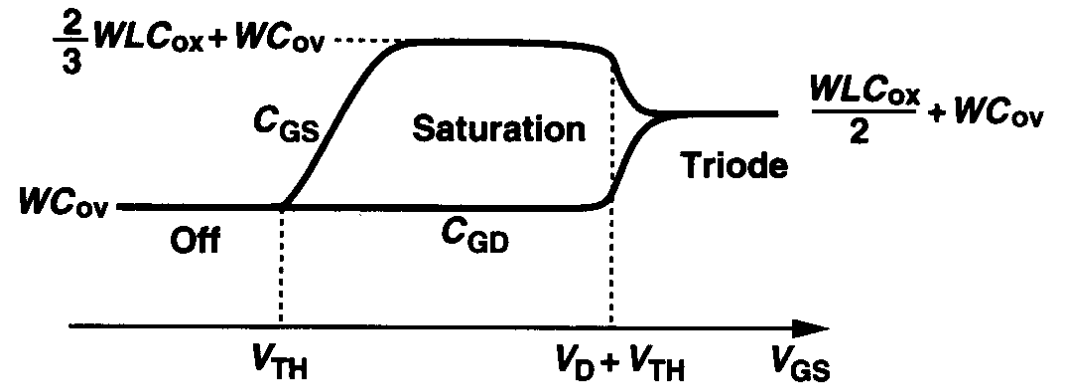
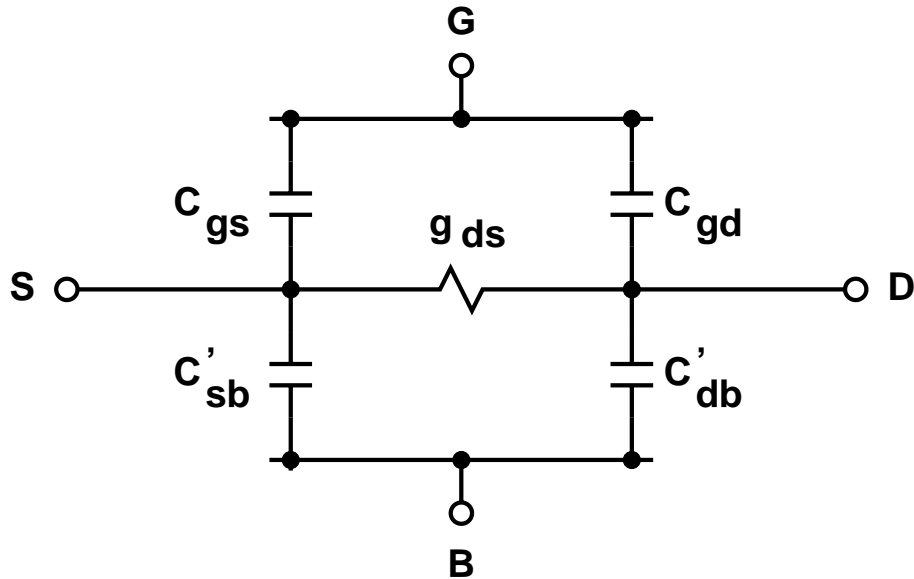
# Complete MOST Small-Signal Model in Saturation Region



$$C_{gd} = C_{ovd} \quad C_{gs} = C_{ovs} + \frac{2}{3}WLC_{ox}$$

$$C'_{sb} = C_{sb} + C_{cb} = (AS + W \cdot L) \times C_J(V_{SB}) + PS \times C_{JSW}(V_{SB})$$

# MOST Small-Signal Model in Triode Region

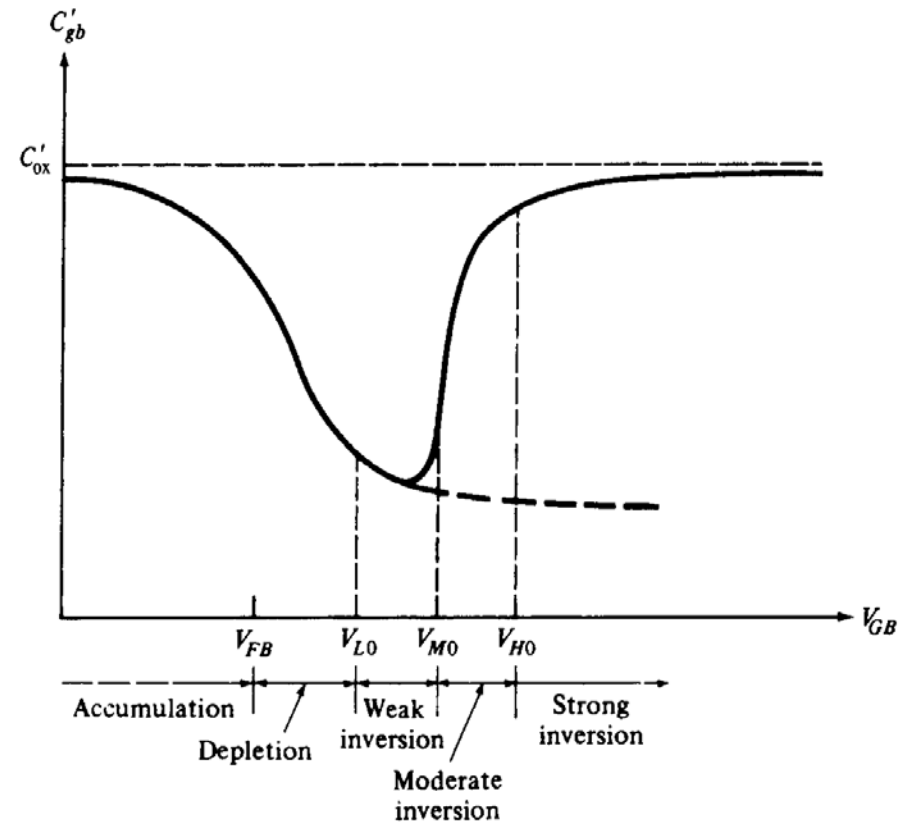
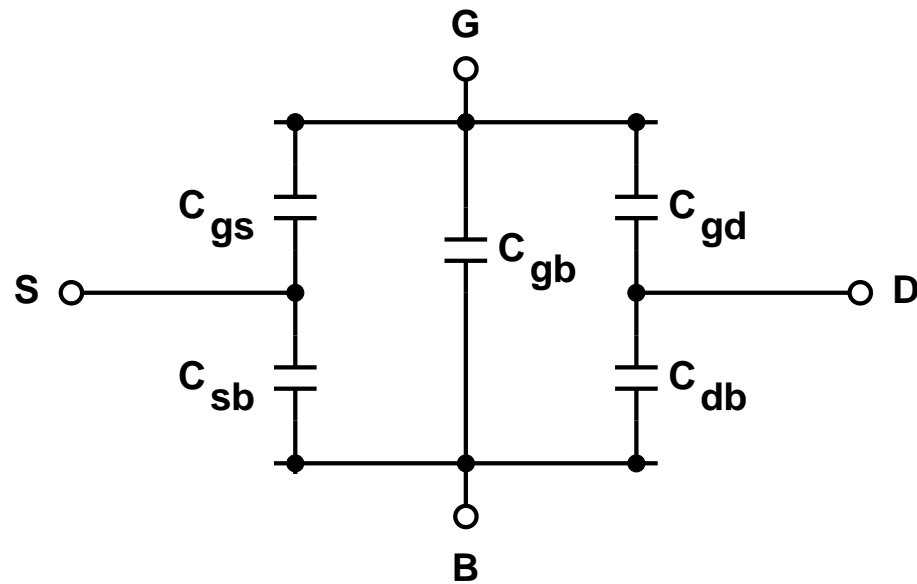


$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_t) \text{ for } V_{DS} \rightarrow 0$$

$$C_{gs} = C_{ovs} + \frac{1}{2} W L C_{ox} \quad C_{gd} = C_{ovd} + \frac{1}{2} W L C_{ox}$$

$$C'_{sb} = C_{sb} + \frac{1}{2} W L C_J (V_{SB}) \quad C'_{db} = C_{db} + \frac{1}{2} W L C_J (V_{DB})$$

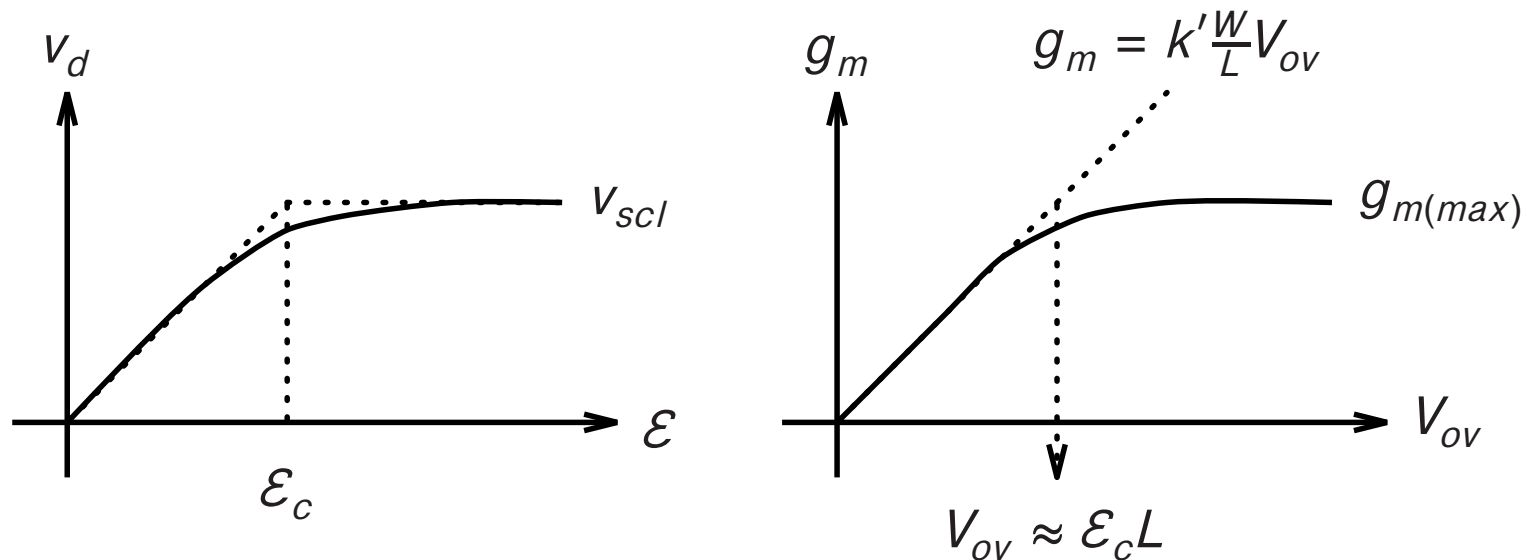
# MOST Small-Signal Model in Cutoff Region



$$C_{gs} = C_{ovs} \quad C_{gd} = C_{ovd}$$

- $C_{gb}$  is highly nonlinear and dependent on the gate voltage.

# Carrier Velocity Saturation



$$v_d = \text{Carrier Drift velocity} = \frac{\mu \mathcal{E}}{1 + \mathcal{E}/\mathcal{E}_c} \quad \mathcal{E}_c \approx 1.5 \times 10^6 \text{ V/m}$$

- $\mu$  is the low-field mobility.

In the triode region

$$I_D = W Q_I(y) \cdot v_d \quad \Rightarrow \quad I_D = \frac{\mu C_{ox}}{1 + \frac{1}{\mathcal{E}_c} \frac{V_{DS}}{L}} \cdot \frac{W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

# Carrier Velocity Saturation

---

Using  $\partial I_D / \partial V_{DS} = 0$  to find  $V_{DSAT}$ , we have

$$V_{DSAT} = \varepsilon_c L \left( \sqrt{1 + \frac{2V_{ov}}{\varepsilon_c L}} - 1 \right) = V_{ov} \left( 1 - \frac{V_{ov}}{2\varepsilon_c L} + \dots \right)$$

And the saturation current is

$$I_{DSAT} = \frac{1}{2} \mu C_{ox} \frac{W}{L} V_{DSAT}^2 = \frac{1}{2} \mu C_{ox} \frac{W}{L} V_{ov}^2 \left( 1 - \frac{V_{ov}}{2\varepsilon_c L} + \dots \right)^2$$

The transconductance is

$$g_m = W \mu C_{ox} \varepsilon_c \frac{\sqrt{1 + \frac{2V_{ov}}{\varepsilon_c L}} - 1}{\sqrt{1 + \frac{2V_{ov}}{\varepsilon_c L}}} \quad \text{or} \quad \frac{g_m}{I_D} = \frac{2}{\varepsilon_c L \sqrt{1 + \frac{2V_{ov}}{\varepsilon_c L}} \left( \sqrt{1 + \frac{2V_{ov}}{\varepsilon_c L}} - 1 \right)}$$

# Effects of Carrier Velocity Saturation

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- If  $V_{ov} \ll \mathcal{E}_c L$ ,

$$I_{DSAT} \approx \frac{1}{2} \frac{\mu C_{ox}}{1 + \frac{V_{ov}}{\mathcal{E}_c L}} \frac{W}{L} V_{ov}^2 \quad g_m \approx \mu C_{ox} \frac{W}{L} \frac{V_{ov}}{1 + \frac{V_{ov}}{\mathcal{E}_c L}} \quad \frac{g_m}{I_D} \approx \frac{2}{V_{ov}}$$

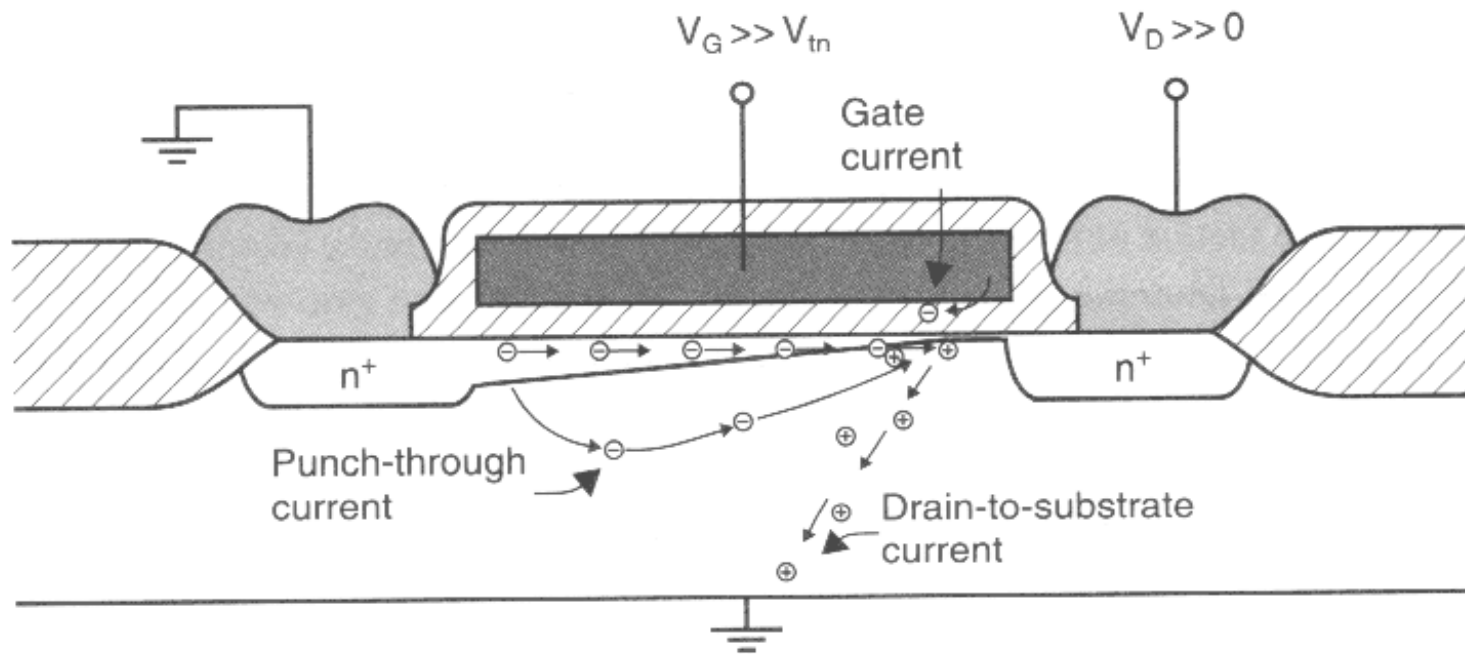
- The mobility degradation can be modeled by a resistor  $R_{SX} = \frac{1}{\mathcal{E}_c} \frac{1}{\mu C_{ox}} \frac{1}{W}$  in series with the source of an ideal square-law device.
- Velocity-saturation effects are insignificant in hand calculations if  $V_{ov} < 0.1 \mathcal{E}_c L$ .

- If  $V_{ov} \gg \mathcal{E}_c L$ ,

$$I_{DSAT} \approx \mu C_{ox} W V_{ov} \mathcal{E}_c = W C_{ox} V_{ov} v_{scl} \quad g_m \approx W C_{ox} v_{scl} \quad \frac{g_m}{I_D} \approx \frac{1}{V_{ov}}$$

- $v_{scl} = \mu \mathcal{E}_c$  is the scattering-limited velocity.
- $I_{DSAT}$  is a linear function of  $V_{ov}$ , and independent of  $L$ .

# Hot Carriers



$$I_{DB} = K_1(V_{DS} - V_{DSAT})I_D e^{-K_2/(V_{DS} - V_{DSAT})}$$

$$g_{db} \equiv \frac{\partial I_{DB}}{\partial V_D} = \frac{I_{DB}}{V_D - V_{DSAT}} \left( \frac{K_2}{V_{DS} - V_{DSAT}} + 1 \right) \approx \frac{K_2 I_{DB}}{(V_{DS} - V_{DSAT})^2}$$

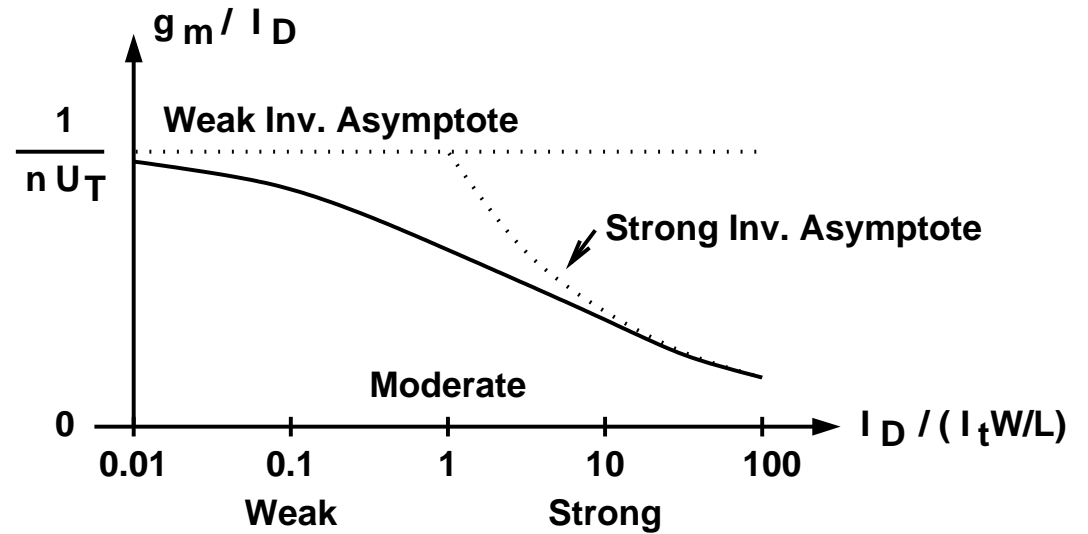
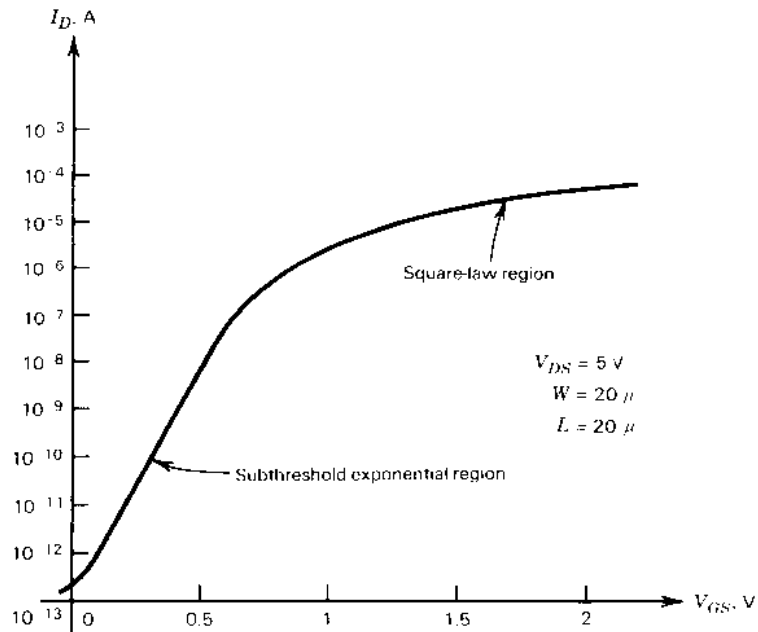
- $K_1 \sim 5 \text{ V}^{-1}$  and  $K_2 = 30 \text{ V}$  are process-dependent parameters.

# Short-Channel Effects

---

- Hot Carriers.
  - The drain-to-substrate current can be modeled by a finite drain-to-substrate resistor.
  - The punch-through current is an additional cause of lower  $r_o$  and possibly transistor breakdown.
  - Some charges in the gate current can be trapped in the gate oxide, causing a shift in  $V_t$ .
  - The hot-carrier effects are more pronounced for nMOST than for pMOST, because electrons have larger velocities than holes.
- Drain-Induced Barrier Lowering (DIBL)
  - For short-channel devices, DIBL effectively lowers  $V_t$  as  $V_{DS}$  is increased, thereby further lowering the  $r_o$ .
- Carrier Velocity Saturation.

# Subthreshold Conduction in MOST



In the weak inversion region

$$I_D = I_t \frac{W}{L} e^{V_{ov}/(nU_T)} \left(1 - e^{-V_{DS}/U_T}\right) \quad n = \frac{C_{ox} + C_{depl}}{C_{ox}} = 1 + \chi \approx 1.5$$

- $I_t \propto D_n n_{po}$  depends on process parameters (e.g., 20 nA).

# Subthreshold Conduction in MOST

---

When  $|V_{DS}| > 3U_T$ ,  $I_D$  saturates and

$$g_m \equiv \frac{\partial I_D}{\partial V_{GS}} = \frac{I_D}{nU_T} = \frac{I_D}{U_T} \frac{C_{ox}}{C_{ox} + C_{depl}} \quad \frac{g_m}{I_D} = \frac{1}{nU_T} = \frac{1}{U_T} \frac{C_{ox}}{C_{ox} + C_{depl}}$$

To find  $V_{ov}$  for strong inversion, let

$$\frac{g_m}{I_D} = \frac{1}{nU_T} = \frac{2}{V_{ov}} \quad \Rightarrow \quad V_{ov} = 2nU_T \approx 78 \text{ mV}$$

- $2nU_T < V_{ov}$  → *Strong Inversion*
- $0 < V_{ov} < 2nU_T$  → *Moderate Inversion*
- $V_{ov} < 0$  → *Weak Inversion*

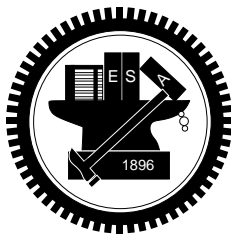
- In weak inversion,  $C_{gs} \simeq C_{gd} \simeq 0$ , and

$$C_{gb} = WL \times (C_{ox} \parallel C_{depl}) = WL \times C_{ox} C_{depl} / (C_{ox} + C_{depl})$$

# Integrated Circuit Technologies

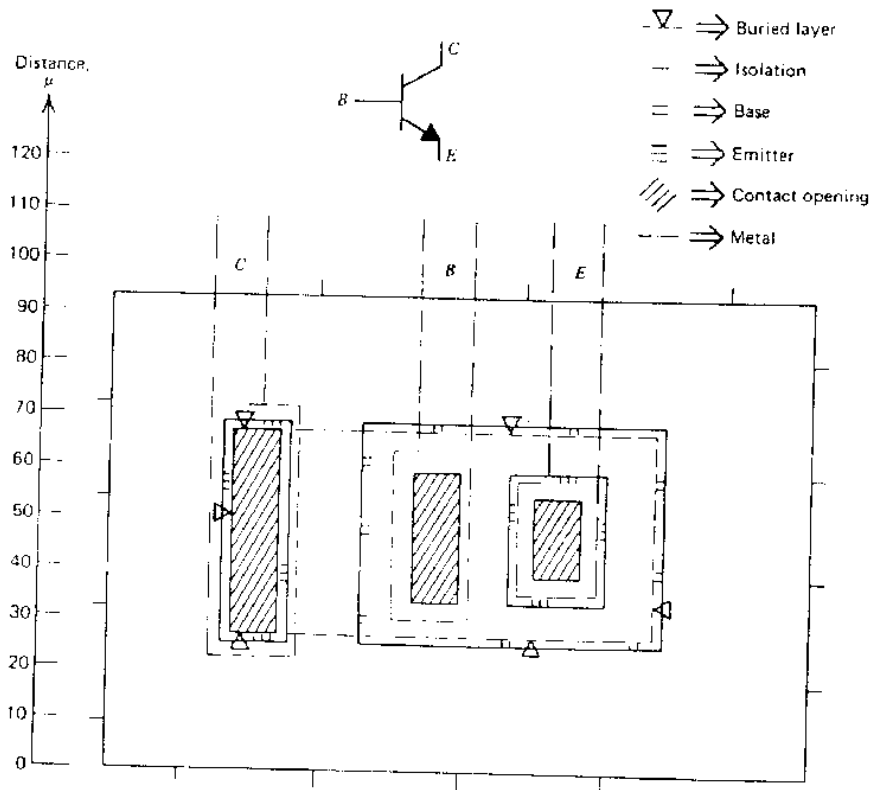
Jieh-Tsorng Wu

July 16, 2002



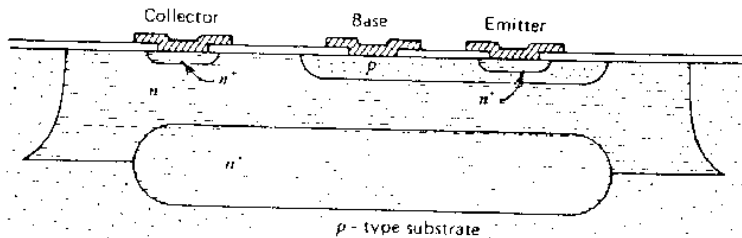
National Chiao-Tung University  
Department of Electronics Engineering

# Integrated-Circuit NPN Transistor

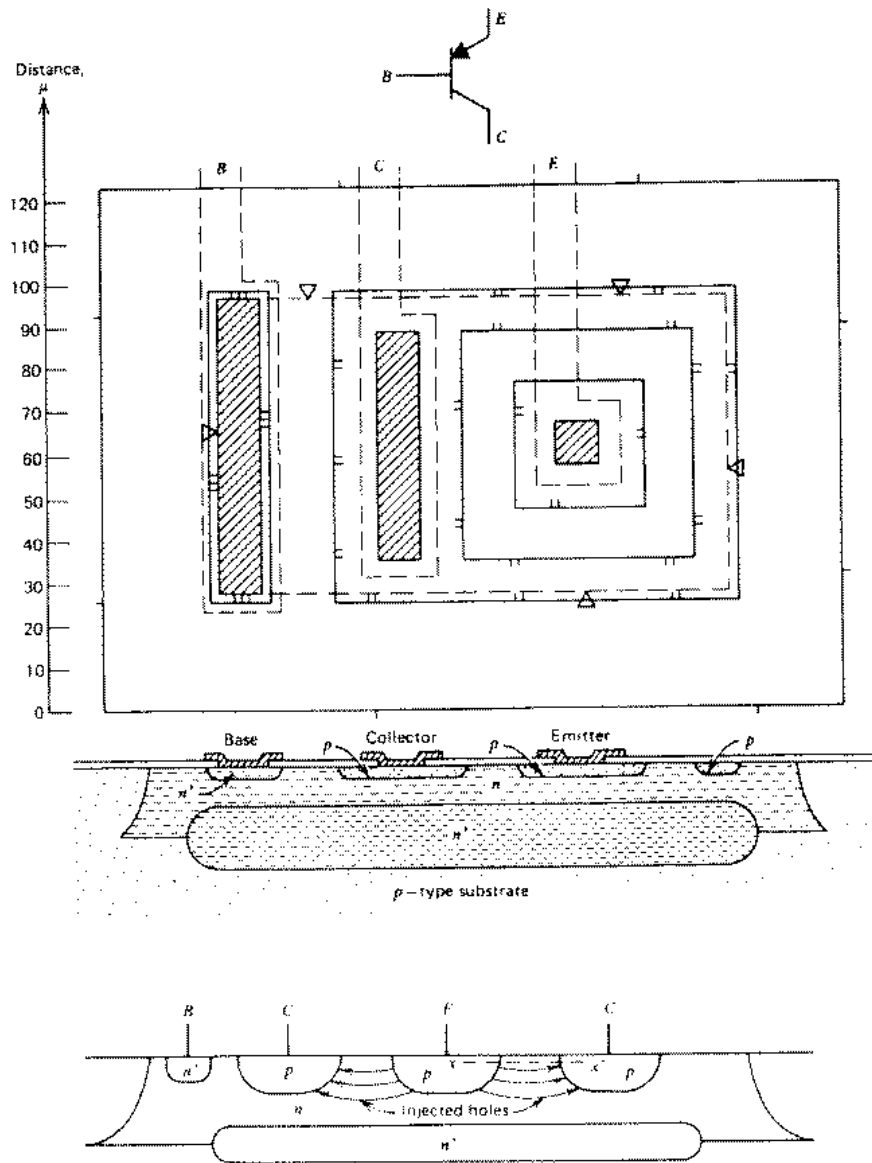


Emitter Diffusion	0.5–2.5 $\mu\text{m}$ , 2–10 $\Omega/\square$
Base Diffusion	1–3 $\mu\text{m}$ , 100–300 $\Omega/\square$
Isolation Diffusion	20–40 $\Omega/\square$
Epitaxial layer	17 $\mu\text{m}$ ( $BV_{CEO} = 36 \text{ V}$ ) $10^{15} \text{ atoms/cm}^3$ , 5 $\Omega\text{-cm}$
Buried layer	20–50 $\Omega/\square$
P-Substrate	250 $\mu\text{m}$ $10^{16} \text{ atoms/cm}^3$ 1–2 $\Omega\text{-cm}$

- Junction isolation.

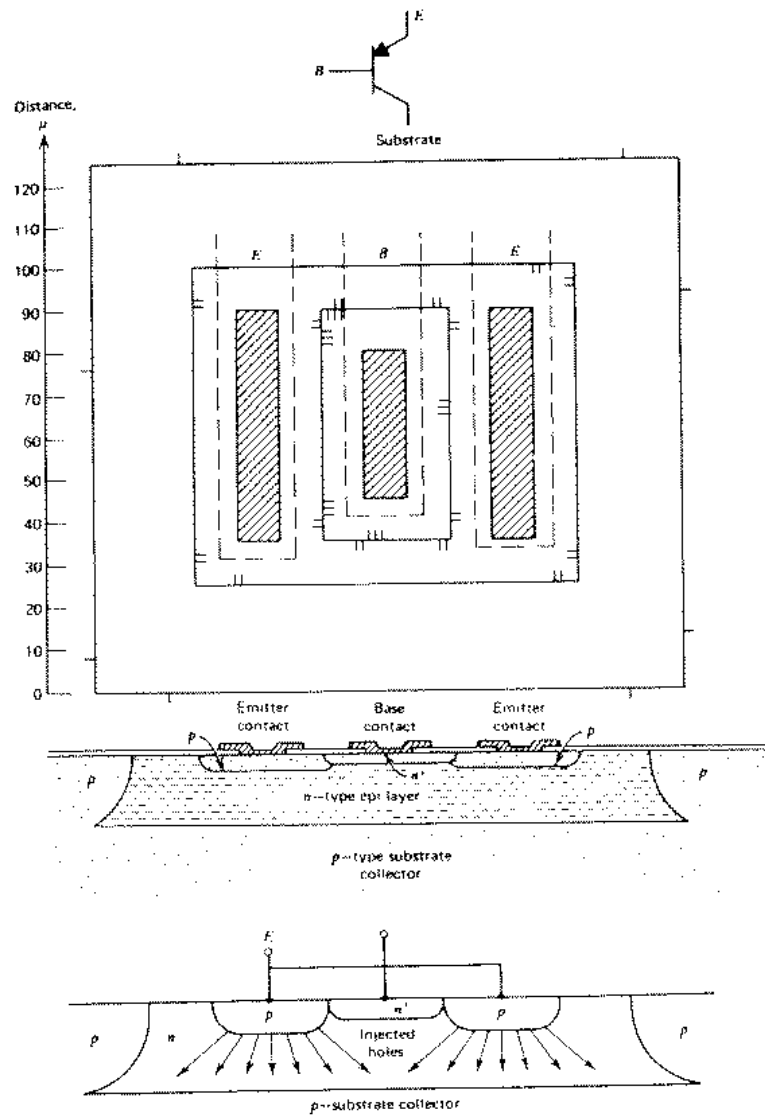


# Lateral PNP Transistor



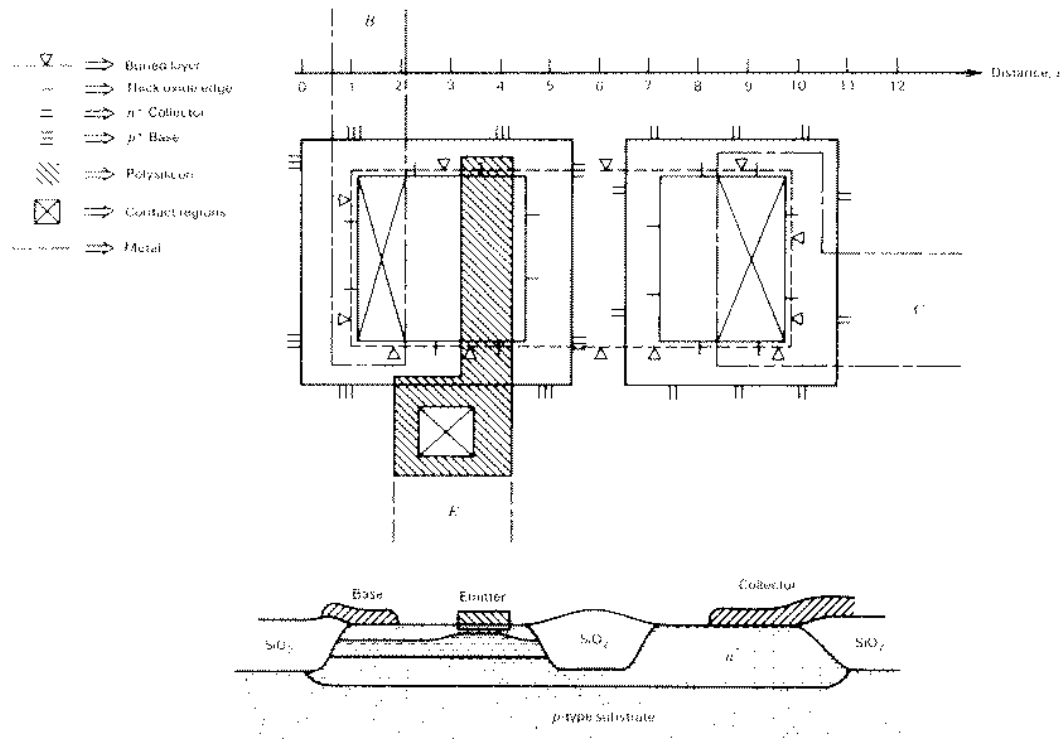
- Lightly doped base.
- Slow.
- Low current gain, especially as  $I_C \uparrow$ .

# Vertical PNP Transistors



- Low base resistance.
- Low emitter-base breakdown voltage.
- Substrate collector (no buried layer).

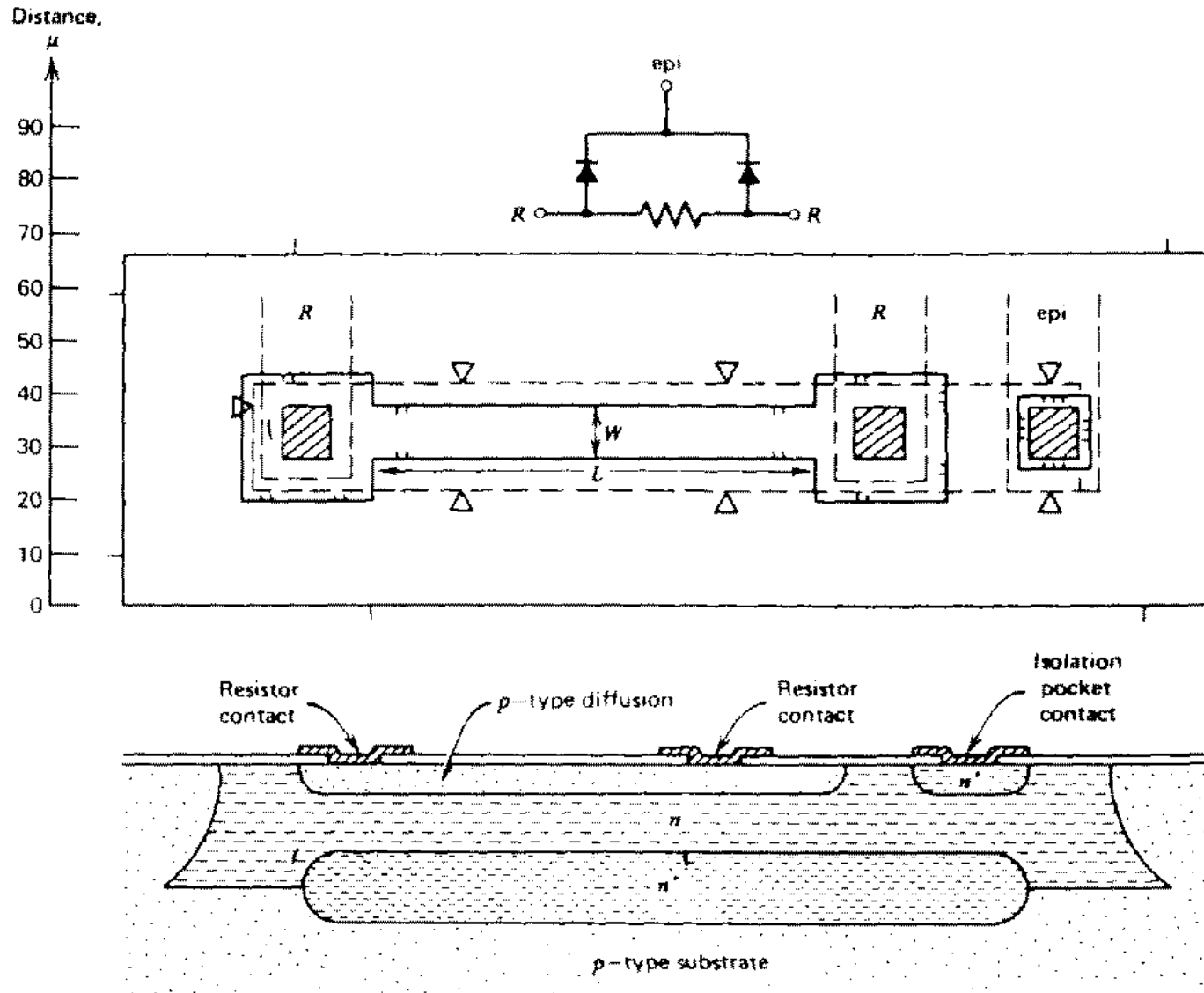
# Advanced-Technology NPN Transistor



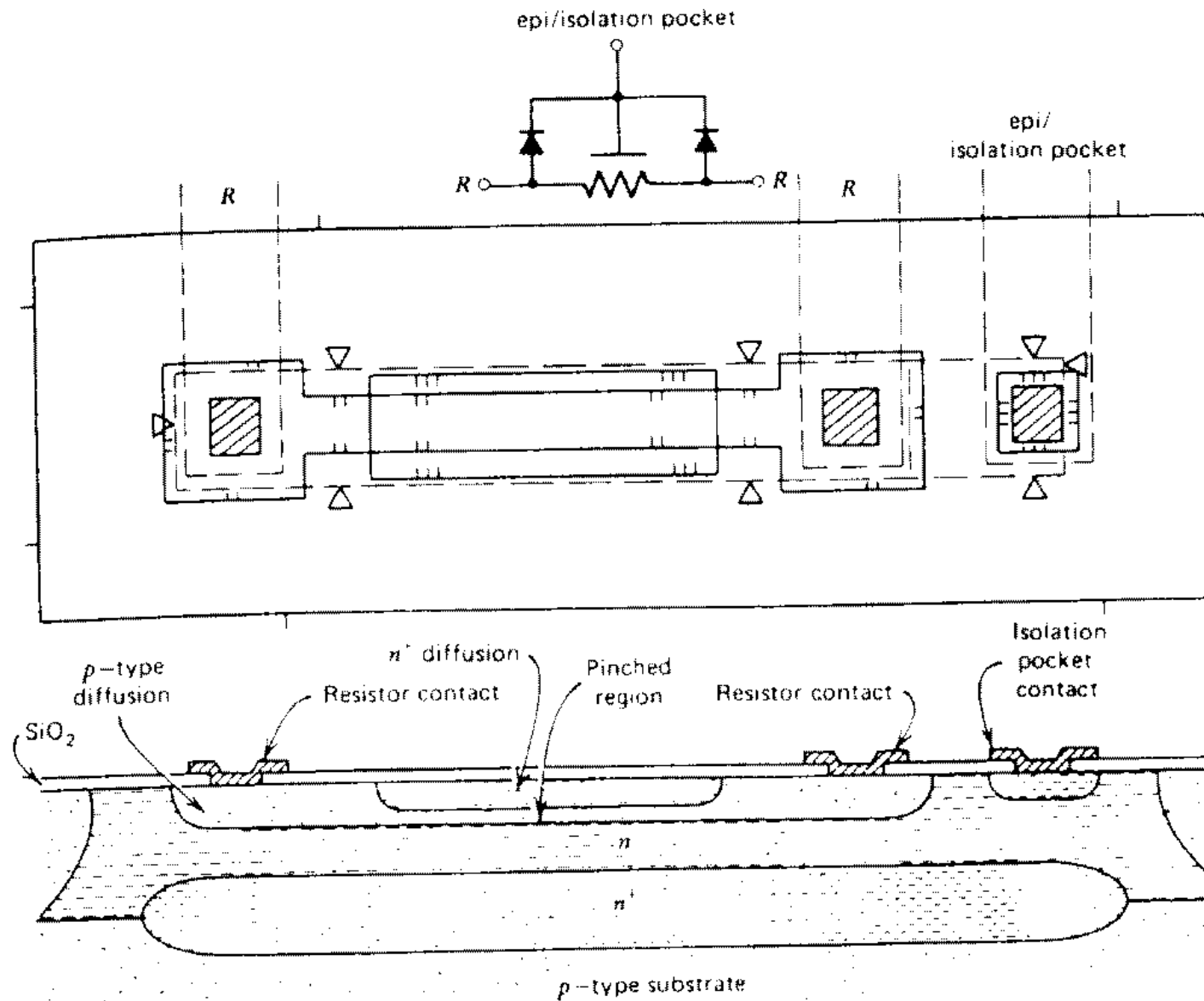
Emitter	0.1 $\mu\text{m}$
Base	0.1 $\mu\text{m}$
Epitaxial layer	1 $\mu\text{m}$ , 0.5 $\Omega\text{-cm}$
Buried layer	20–50 $\Omega/\square$
P-Substrate	250 $\mu\text{m}$
	$10^{16}$ atoms/cm <sup>3</sup>
	1–2 $\Omega\text{-cm}$

- Oxide isolation.
- Polysilicon emitter self-aligned structure.
- High  $f_T$  ( $> 10$  GHz).

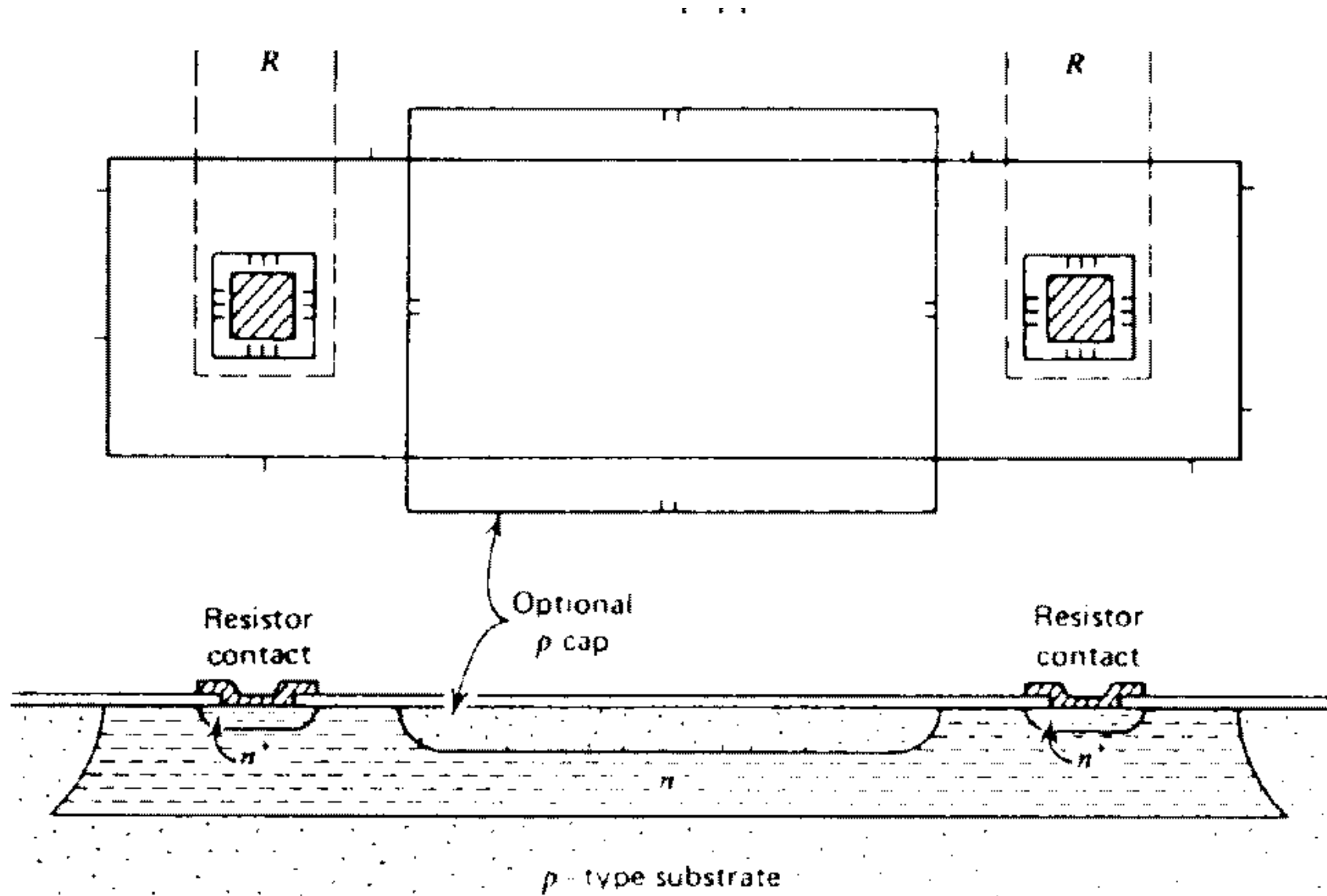
# Base and Emitter Diffused Resistors



# Base Pinch Resistor



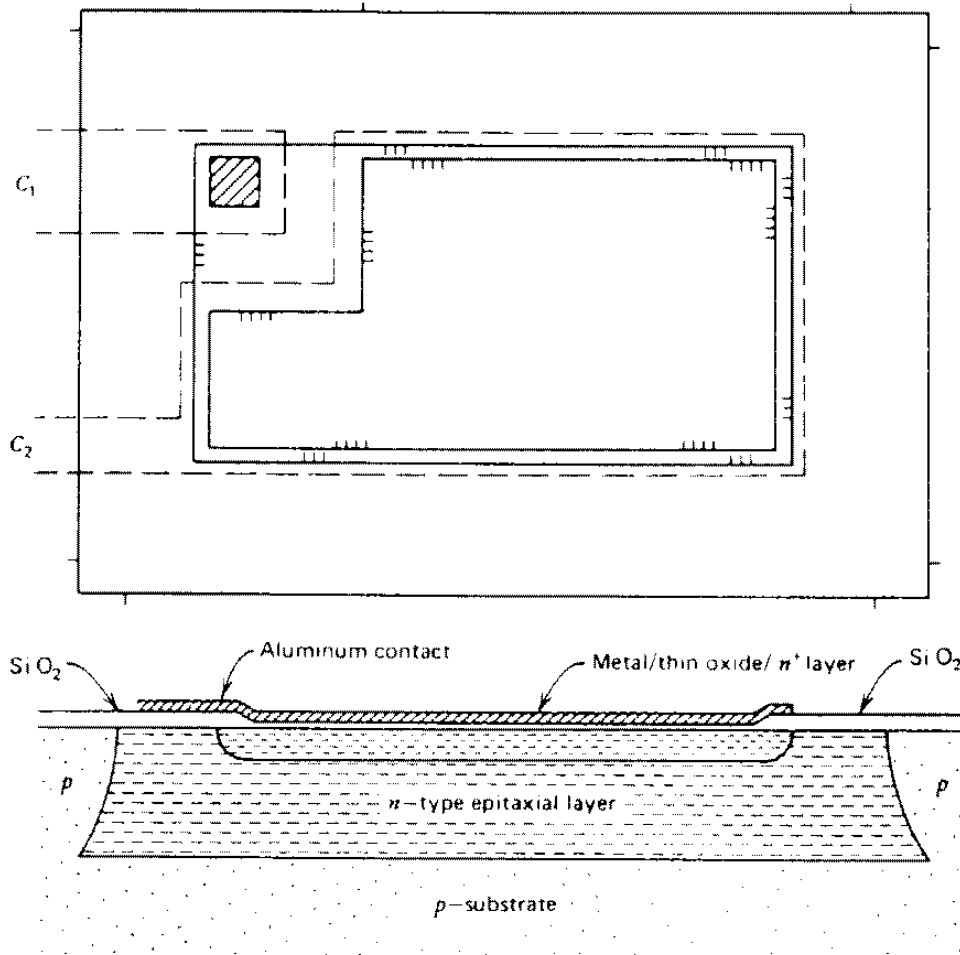
# Epitaxial Resistor



## Properties of IC Resistor

Resistor Type	Sheet $\rho$ $\Omega/\square$	Absolute Tolerance (%)	Matching Tolerance (%)	Temperature Coefficient
Base diffused	100–200	$\pm 20$	$\pm 2$ (5 $\mu$ wide) $\pm 0.2$ (50 $\mu$ wide)	+1500 to +2000 ppm/ $^{\circ}$ C
Emitter diffused	2–10	$\pm 20$	$\pm 2$	+ 600 ppm/ $^{\circ}$ C
Ion implanted	100–1000	$\pm 3$	$\pm 1$ (5 $\mu$ wide) $\pm 0.1$ (50 $\mu$ wide)	Controllable to $\pm 100$ ppm/ $^{\circ}$ C
Base pinch	2 k–10 k	$\pm 50$	$\pm 10$	+ 2500 ppm/ $^{\circ}$ C
Epitaxial	2 k–5 k	$\pm 30$	$\pm 5$	+ 3000 ppm/ $^{\circ}$ C
Epitaxial pinch	4 k–10 k	$\pm 50$	$\pm 7$	+ 3000 ppm/ $^{\circ}$ C
Thin film	0.1 k–2 k	$\pm 5$ – $\pm 20$	$\pm 0.2$ – $\pm 2$	$\pm 10$ to $\pm 200$ ppm/ $^{\circ}$ C

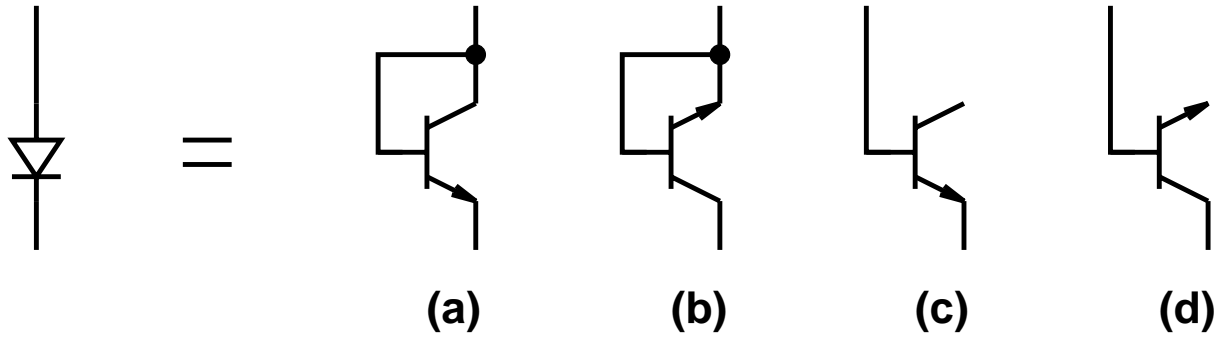
# Capacitors



- PN junctions.
- Metal or poly over thin oxide.

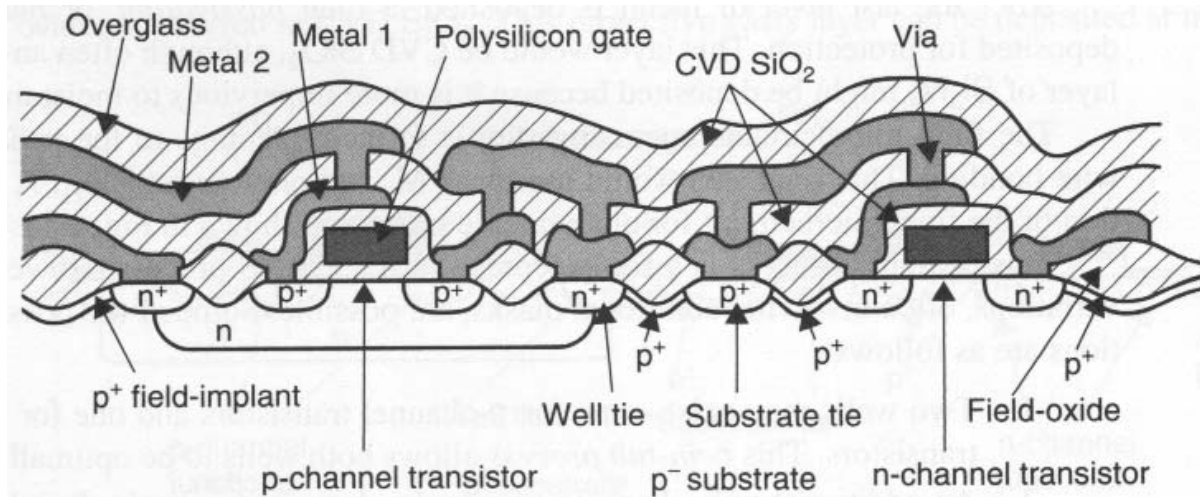
# Diodes

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- Implementation (a) is usually preferred to avoid forward biasing the C-B junction.
- C-B forward bias injects carriers into the epi, which in turn can be collected in the substrate.

# CMOS Integrated-Circuit Technologies



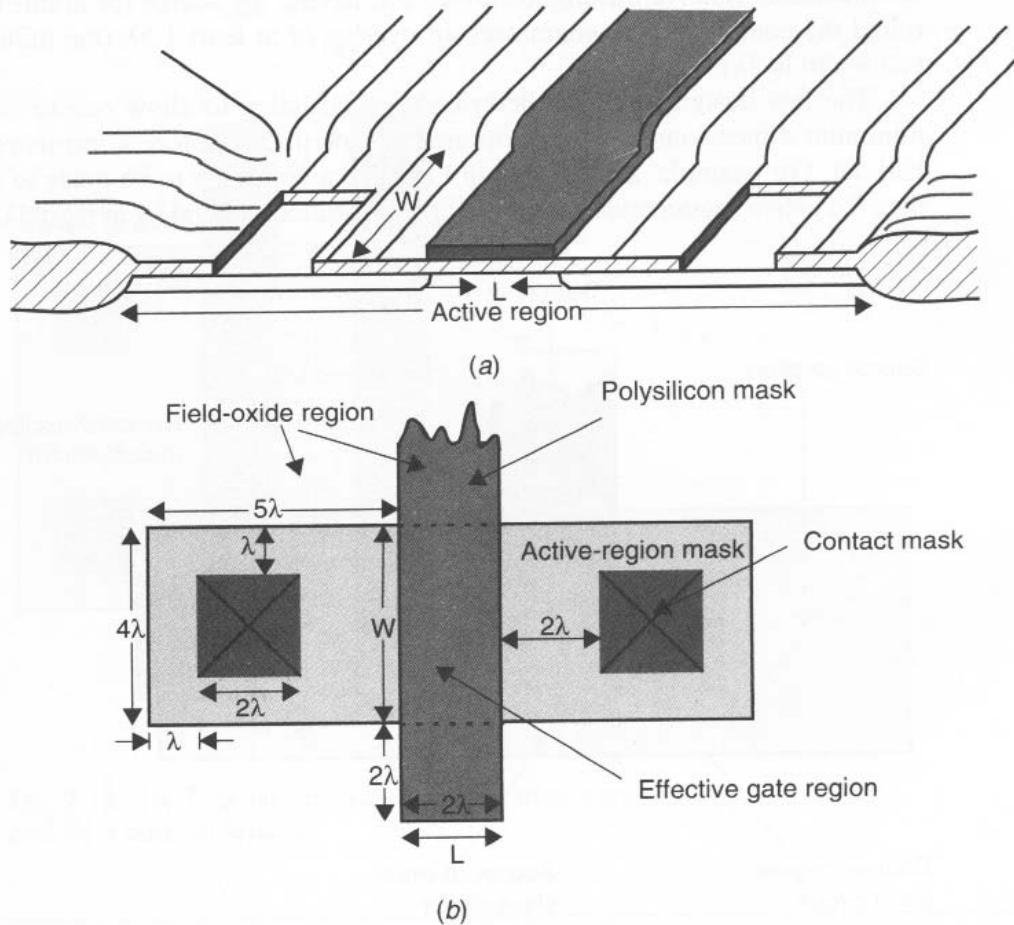
0.5  $\mu\text{m}$  CMOS

M2	1.20	$\mu\text{m}$
M1	0.60	$\mu\text{m}$
Poly	0.25	$\mu\text{m}$
Field Oxide	0.30	$\mu\text{m}$
Gate Oxide	130	$\text{\AA}$
n+ Depth	0.20	$\mu\text{m}$
p+ Depth	0.25	$\mu\text{m}$
N-well Depth	2.50	$\mu\text{m}$

- Additional polysilicon layer may exist to realize poly-to-poly capacitors.
- There are twin-tub processes that have separate and optimized wells for nMOSTs as well as pMOSTs.
- Additional processing steps may be used to fabricate vertical bipolar transistors on the same chip. This is called a BiCMOS technology.

# MOS Transistors

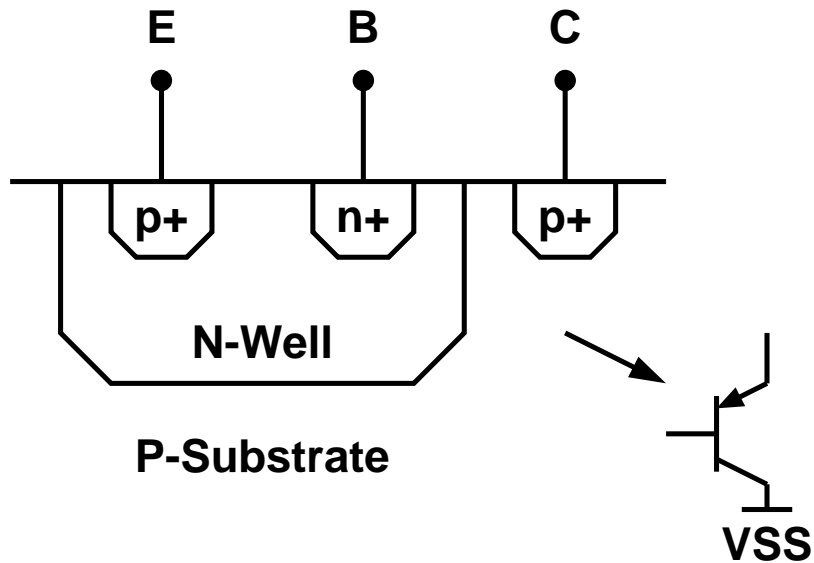
- May have devices with different  $V_t$ .



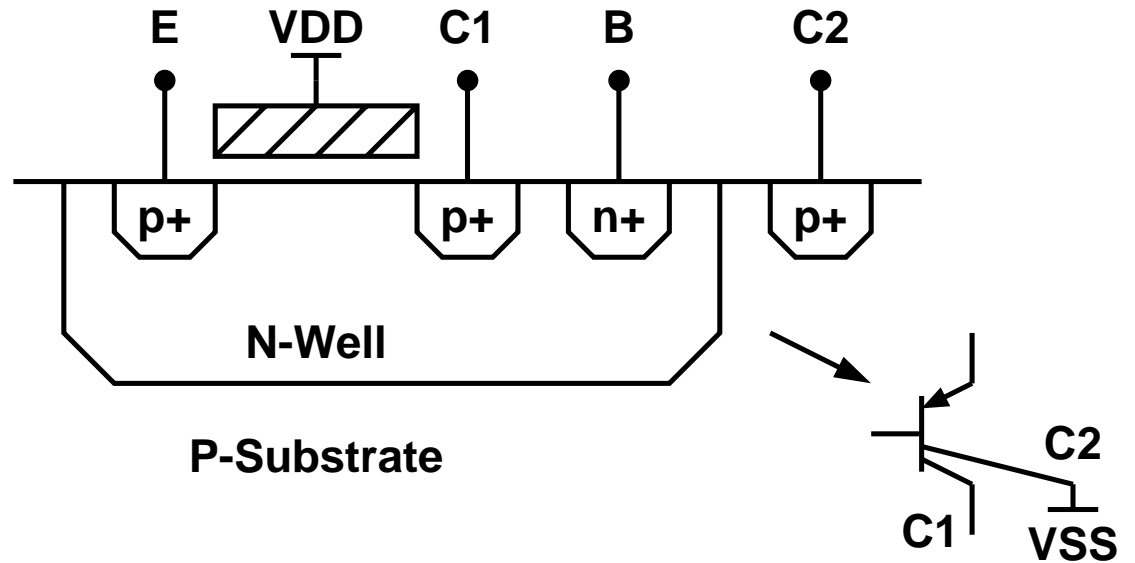
- Source/drain can be shared between two series-connected MOSTs of the same type.
- Wide devices usually employ stacked layout.

# Parasitic BJTs in CMOS Technologies

## Vertical PNP Transistor



## Lateral PNP Transistor

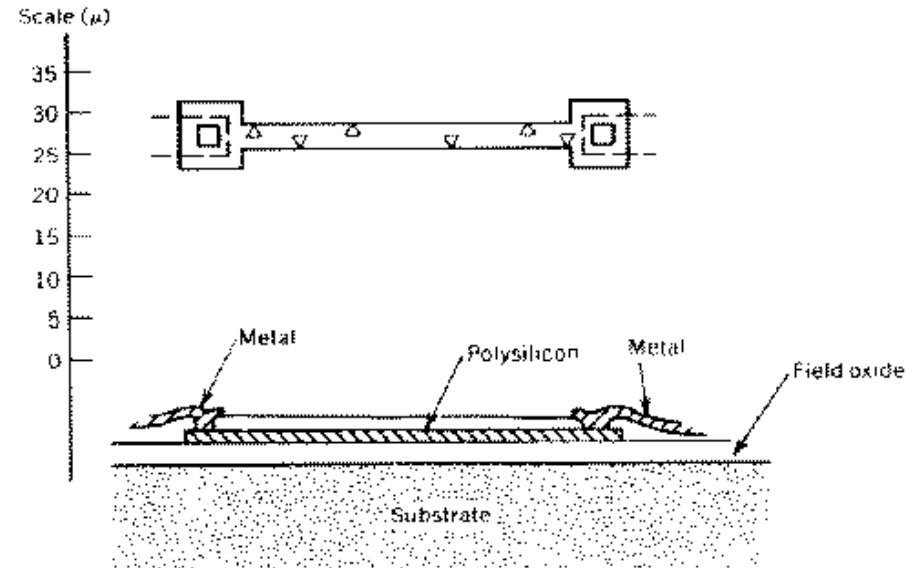


- The collector is usually in ring form surrounding the emitter.
- In the lateral devices, the MOST's  $L$  is the base width.
- The ratio of  $I_{C2}/I_{C1}$  is poorly controlled in practice.

# Resistors in CMOS Technologies

- n+ and p+ diffusion
  - 10–30  $\Omega/\square$
- Polysilicon
  - 20–80  $\Omega/\square$
- N (or P) well diffusion
  - 1k–10k  $\Omega/\square$
- MOSTs in the triode region
  - Depends on  $V_{ov}$  and  $W/L$

## Polysilicon Resistor

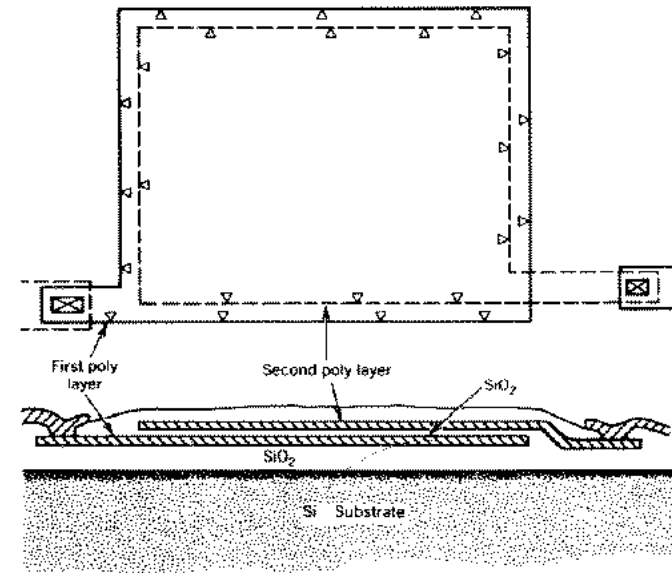


- Large  $R$  variation due to process variation.
- Matching properties is  $\sim 1\%$ .
- Small voltage coefficient.
- No parasitic pn junction.

# Capacitors in CMOS Technologies

- Poly-Poly
- Poly-Metal
- Metal-Metal (MIM)
- Multi-Layer Sandwich.
- Lateral structures.
- MOSTs in triode region
- MOS in accumulation
  - Large voltage coefficient.
  - Large  $R$  in one terminal.

## Poly-Poly Capacitor



- Bottom-plate  $C_{\text{parasitic}}$  is 10%–30% of  $C$  itself.
- Matching properties is 0.1%–1%.
- Voltage coefficient is  $< 50$  ppm/V.
- Temperature coefficient is  $< 50$  ppm/°C.

# Matching Issues

---

Mismatches between two supposedly identical devices are due to

- Localized geometric variation.
  - Resulting from the limited resolution of the photolithographic process itself
- Global material gradient variation.
  - Variations across wafer resulting from nonuniform conditions during the fabrication processes.
- Temperature gradient variation.

# Guidelines for Better Device Matching

---

## Device Considerations:

- Match devices of equal nature.
  - e.g., no JFET-MOST pair or poly-diffusion resistor pair.
- Devices to be matched should operate on the same temperature.
- Input offset voltage for a BJT pair is only  $\sim 1/10$  that for a MOST pair.
- May consider post-fabrication trimming.

# Guidelines for Better Device Matching

---

*Local Matching* Consideration:

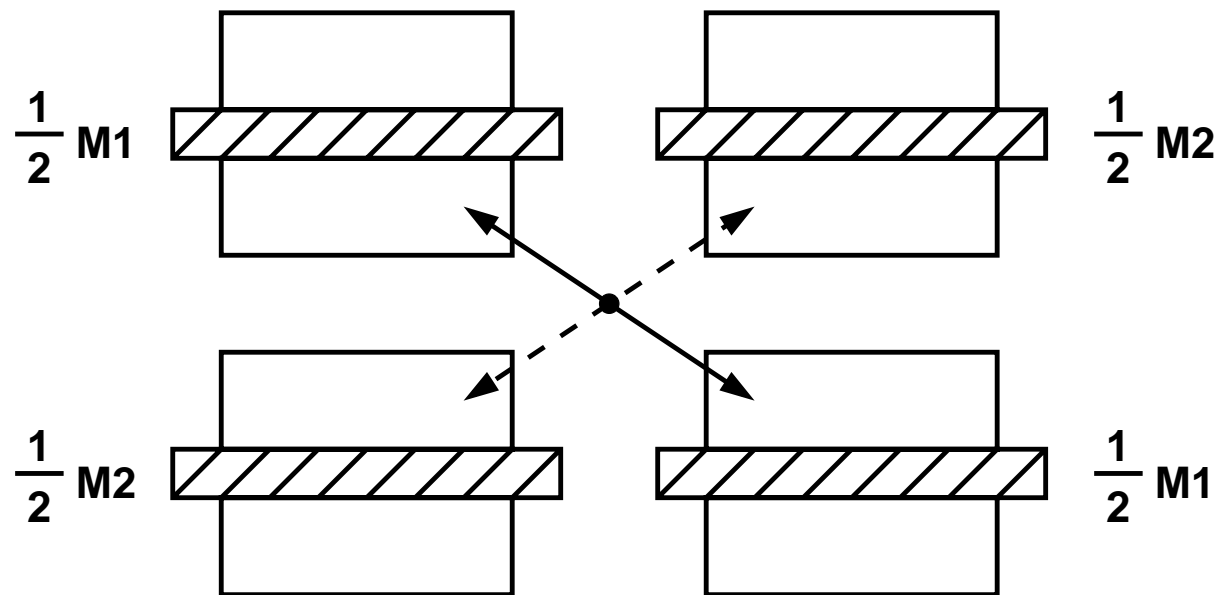
- Increase device size.
- Round devices matches better than square devices.
- Whenever possible, utilize series and/or parallel combination of *unit-sized devices* to form devices of different sizes.
- Use dummy devices to protect matching devices from different etch effects.

# Guidelines for Better Device Matching

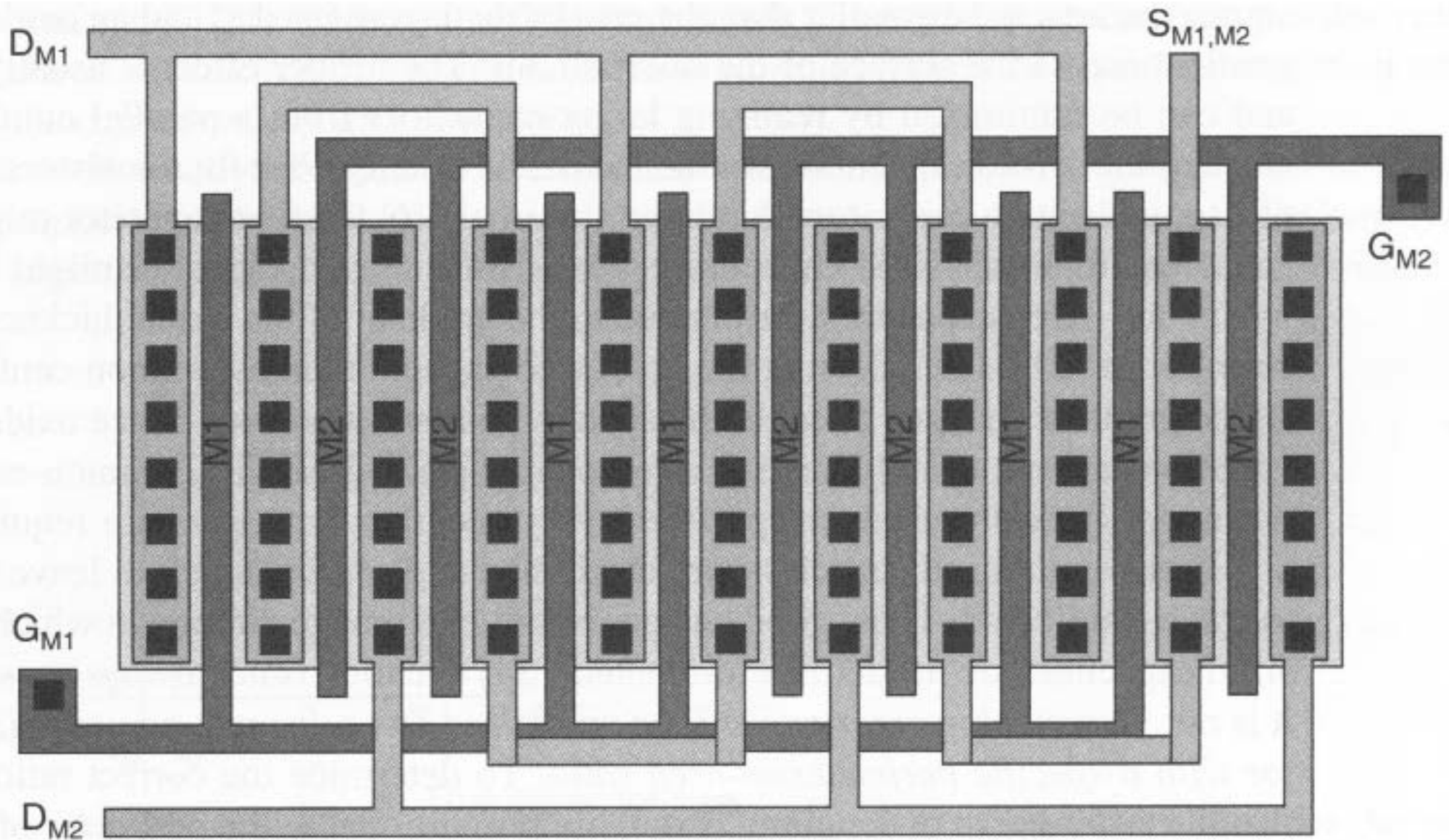
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*Global Matching* Consideration:

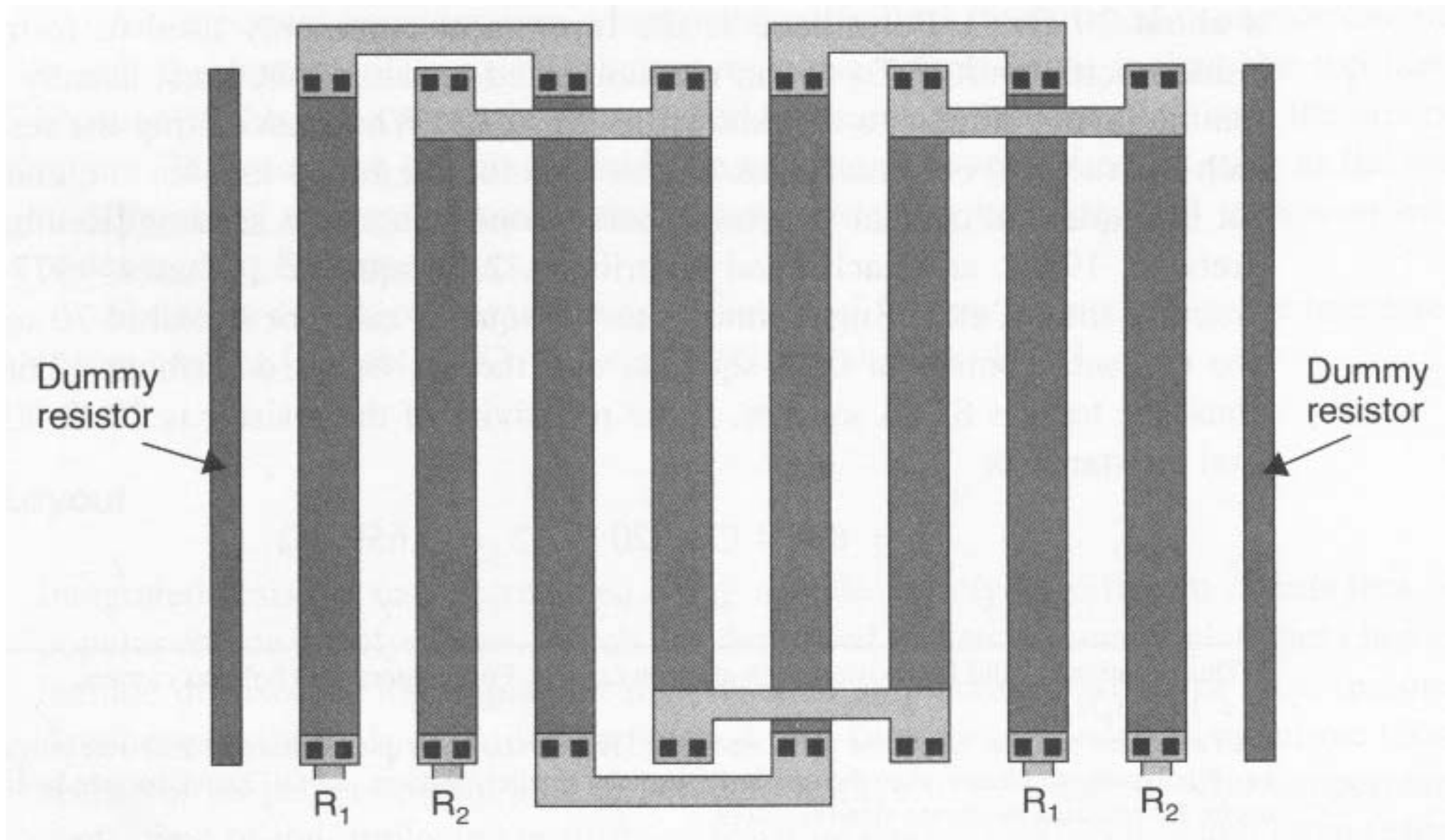
- Layout devices with the same orientation.
- Decrease device separation distance.
- Try a common-centroid layout for the devices to be matched.



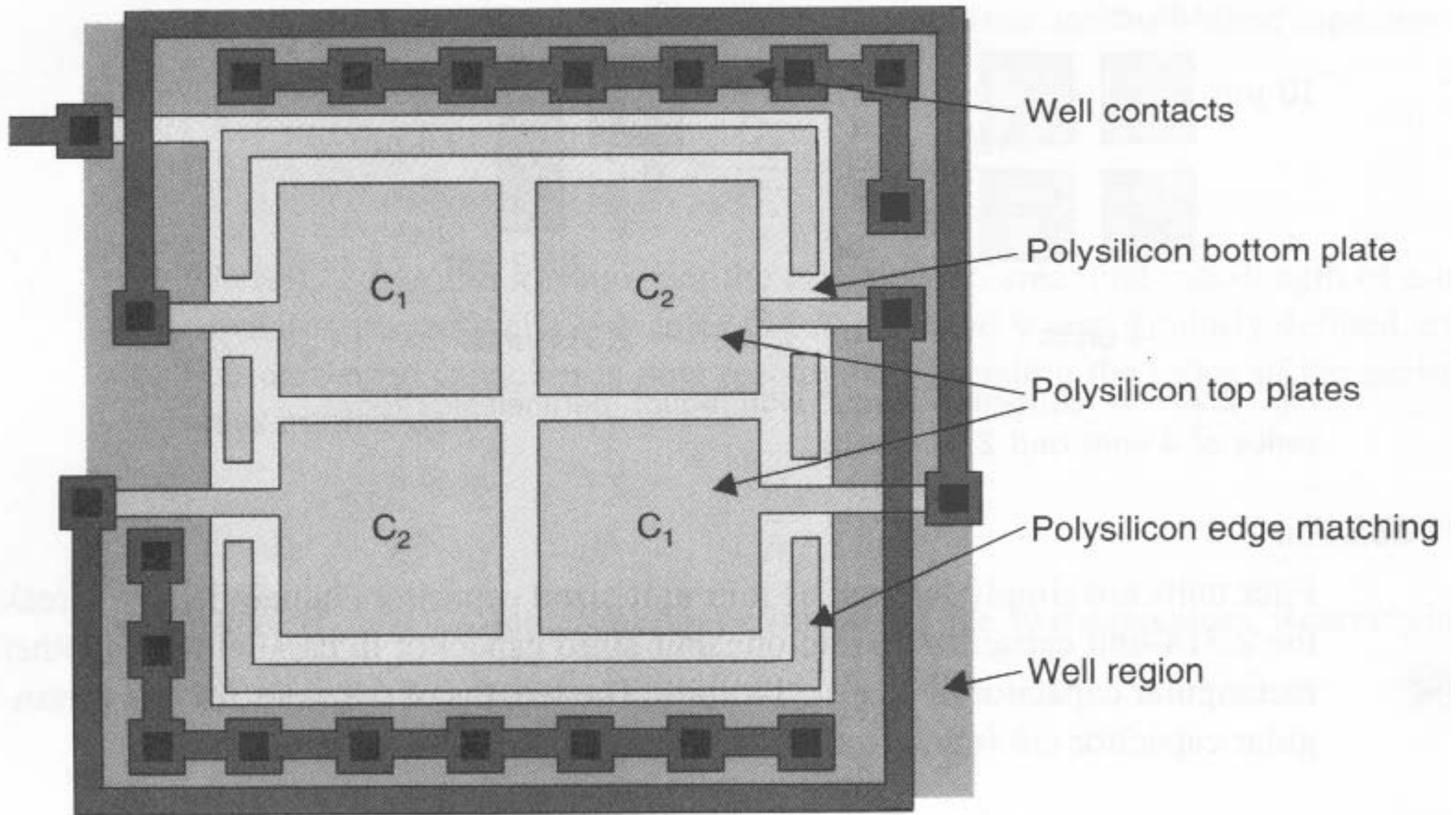
# Transistor Pair Layout Example



# Resistor Pair Layout Example

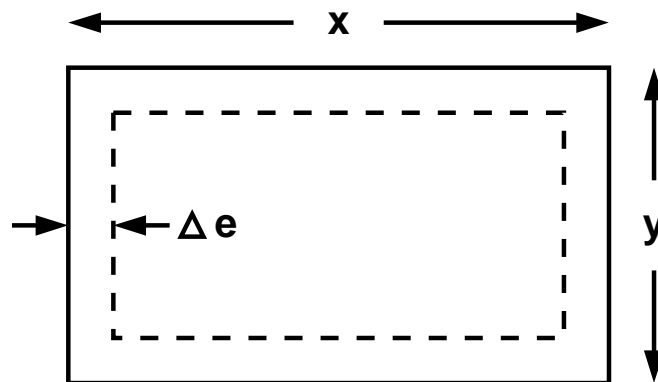


# Capacitor Pair Layout Example



# Capacitor Errors

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Assume a rectangular capacitor with dimension  $x$  and  $y$ . Then

$$C_{\text{ideal}} = C_{ox} \cdot x \cdot y$$

Due to lithography modification  $\Delta e$ , we have

$$C_{\text{true}} = C_{ox} \cdot (x - 2\Delta e) \cdot (y - 2\Delta e) \approx C_{\text{ideal}} \cdot (1 - \epsilon_r)$$

$$\epsilon_r = 2\Delta e \times \frac{x + y}{xy} = \Delta e \times \frac{\text{Perimeter}}{\text{Area}}$$

# Capacitor Layout Design

---

To minimize capacitor ratio error, want

- Capacitors of identical values should have the same shape.
- Capacitors of different values should have the same perimeter-to-area ratio.

Let unit-size capacitor  $C_u$  have a square layout with  $x_u$  on each side. Want to realize a new capacitor  $C$  with dimension  $x$  and  $y$  so that

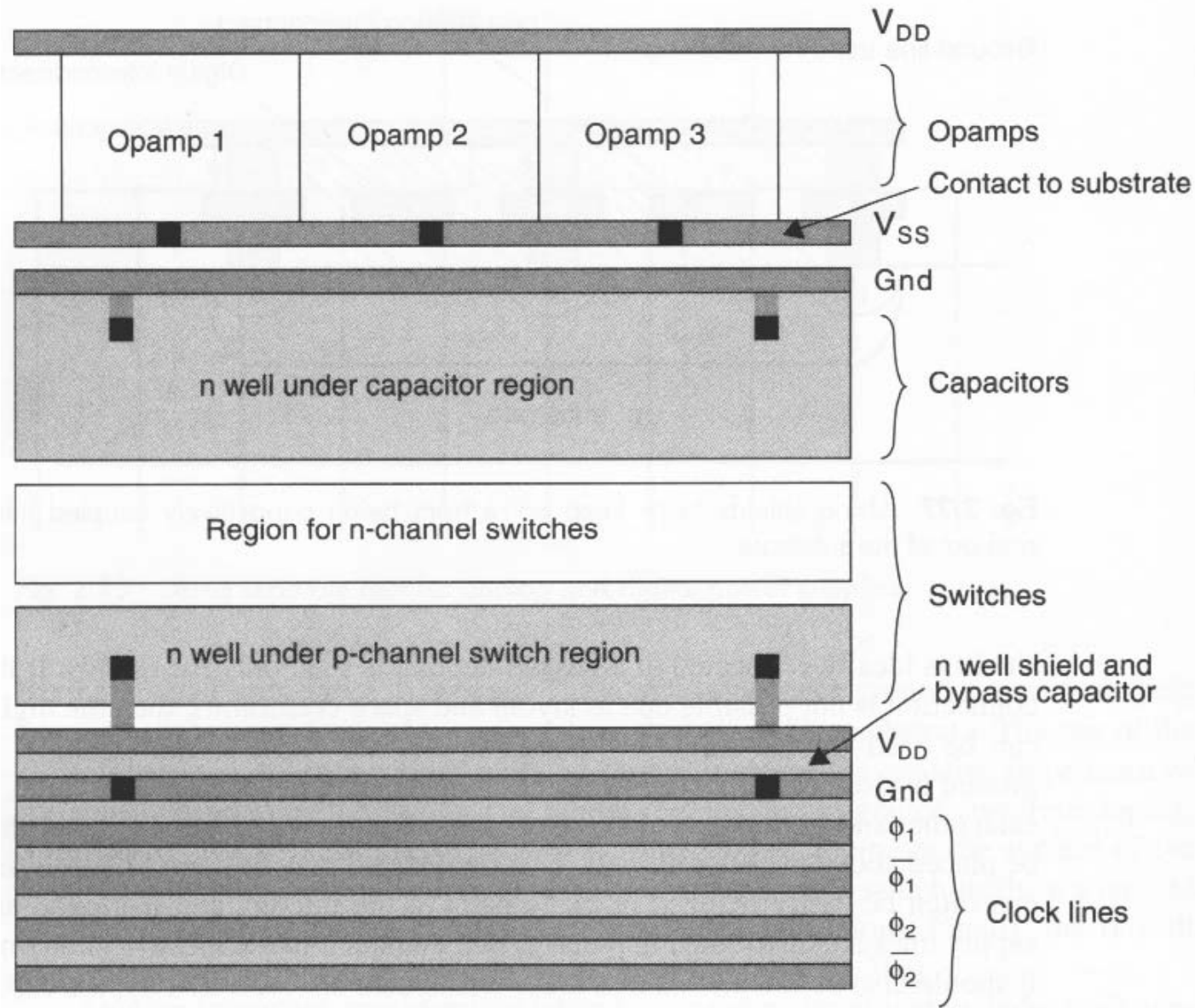
$$\frac{C}{C_u} = K \quad \text{and} \quad \frac{1}{2} \frac{\text{Perimeter}}{\text{Area}} = \frac{2x_u}{x_u^2} = \frac{x+y}{x \cdot y}$$

We have

$$\frac{x \cdot y}{x_u^2} = \frac{x+y}{2x_u} = K \quad \Rightarrow \quad y = x_u \left( K \pm \sqrt{K^2 - K} \right) \quad x = \frac{K x_u^2}{y}$$

- $K$  is usually between 1 and 2.

# Analog Section Floor Plan Example

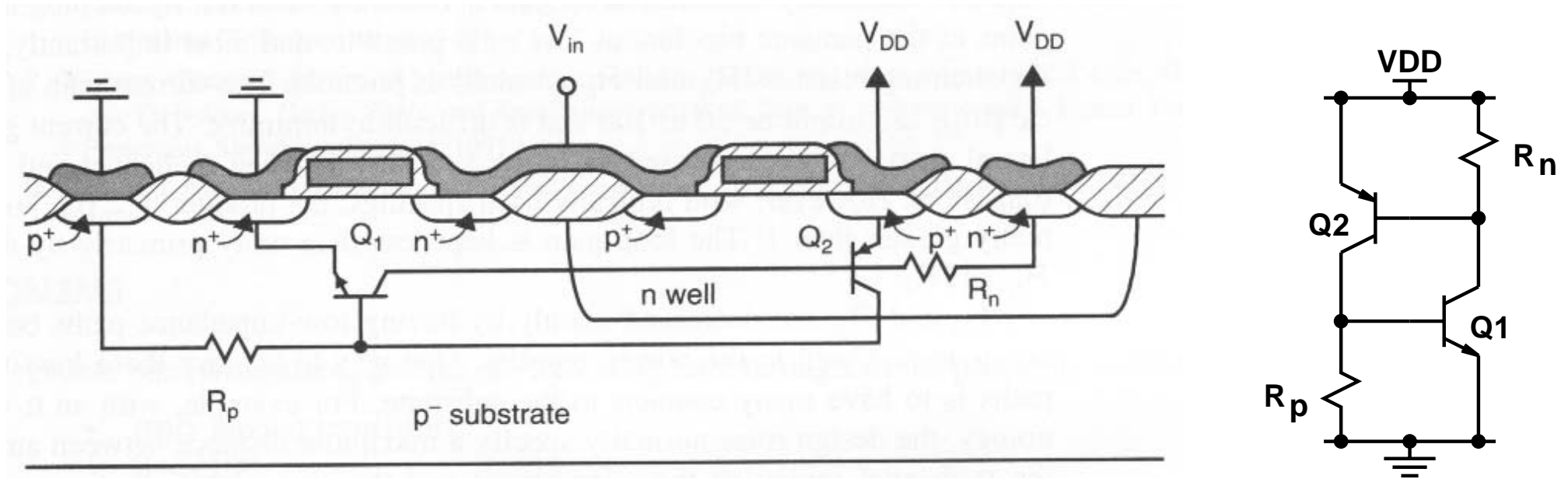


# Noise-Coupling Layout Considerations

---

- Want to minimize noise from digital circuits coupling into the substrate or analog power supplies.
- Separate power lines for analog and digital circuits.
- Different region for analog and digital circuitry, separated by guard rings and wells connected to the power supplies.
- Use metals and wells as shield to protect sensitive nodes. The shields must be connected to clean supply voltages.
- Whenever possible, bypass the power supplies with junction capacitors and/or MOSTs.

# Latch-Up in CMOS Technologies

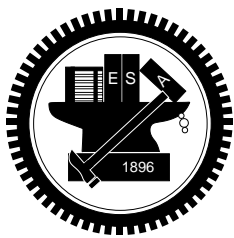


- Keep  $R_p$  and  $R_n$  small by having low-impedance paths between the substrate and well to the power supplies.
- Avoid currents flowing in substrate and wells.
- Transistors that conduct large current must be surrounded by guard rings.

# Single-Transistor Gain Stages

Jieh-Tsorng Wu

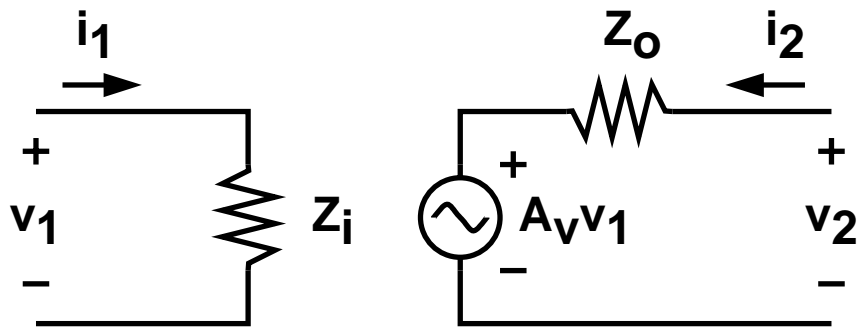
October 25, 2002



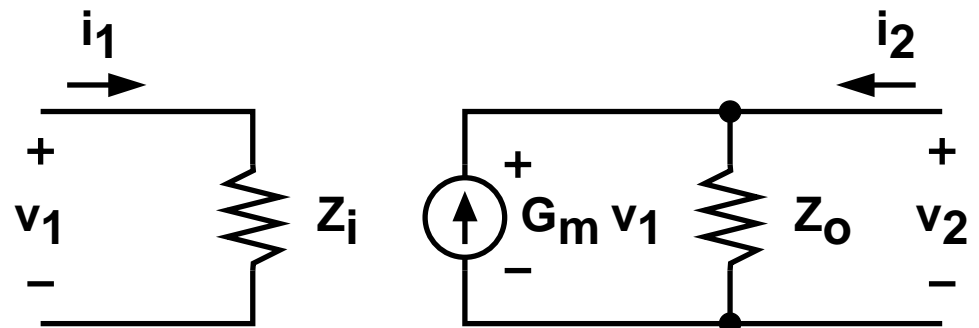
National Chiao-Tung University  
Department of Electronics Engineering

# Unilateral Two-Port Network

Thevenin Output Model



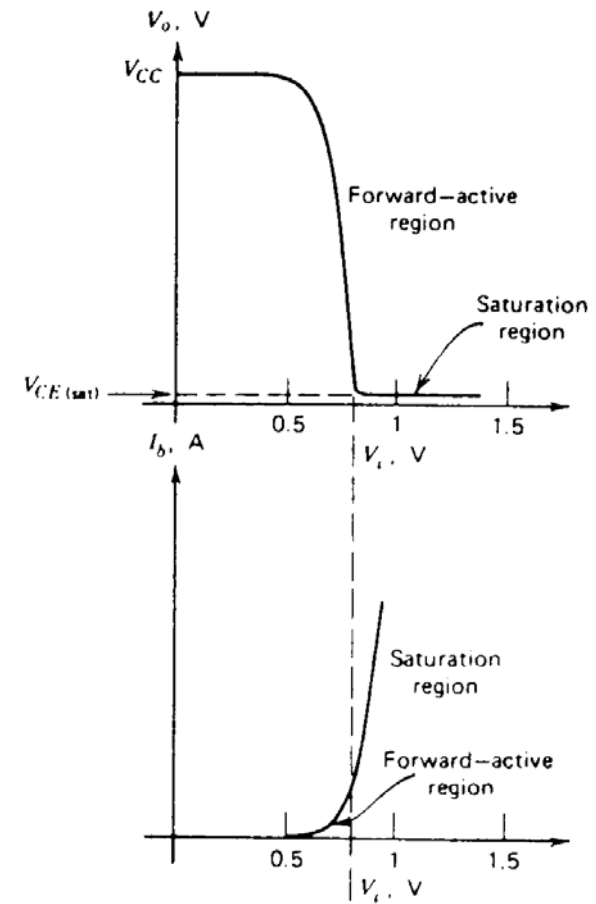
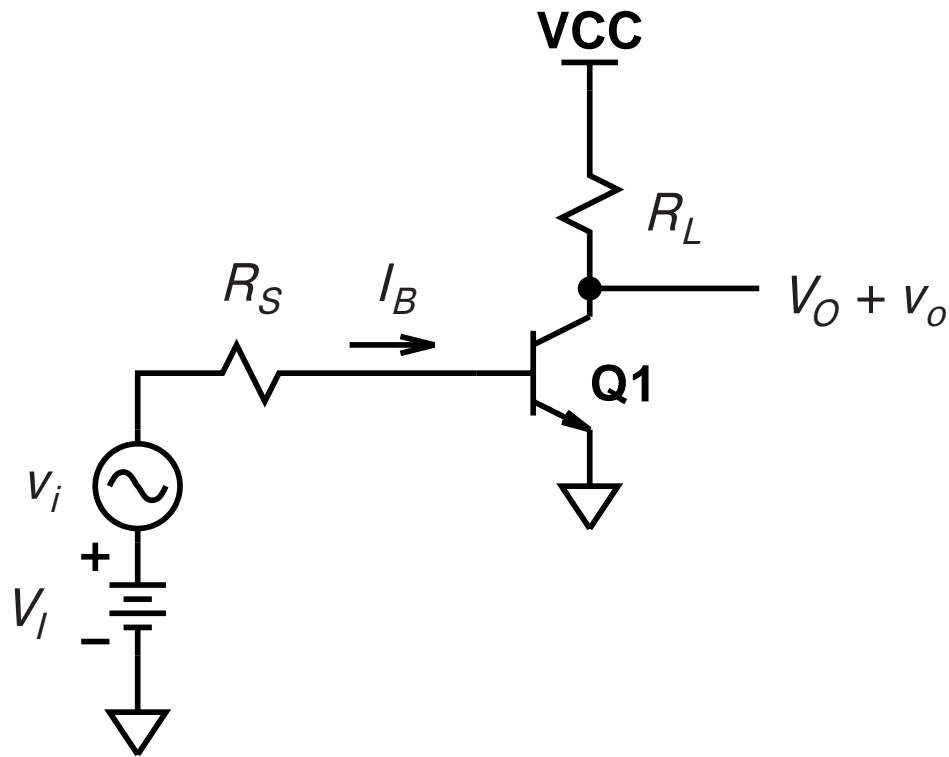
Norton Output Model



$$Z_i = \frac{V_1}{i_1} \quad Z_o = \frac{V_2}{i_2} \Big|_{v_1=0}$$

$$A_v = \frac{V_2}{V_1} \Big|_{i_2=0} \quad G_m = \frac{i_2}{V_1} \Big|_{v_2=0} \quad A_v = G_m \times Z_o$$

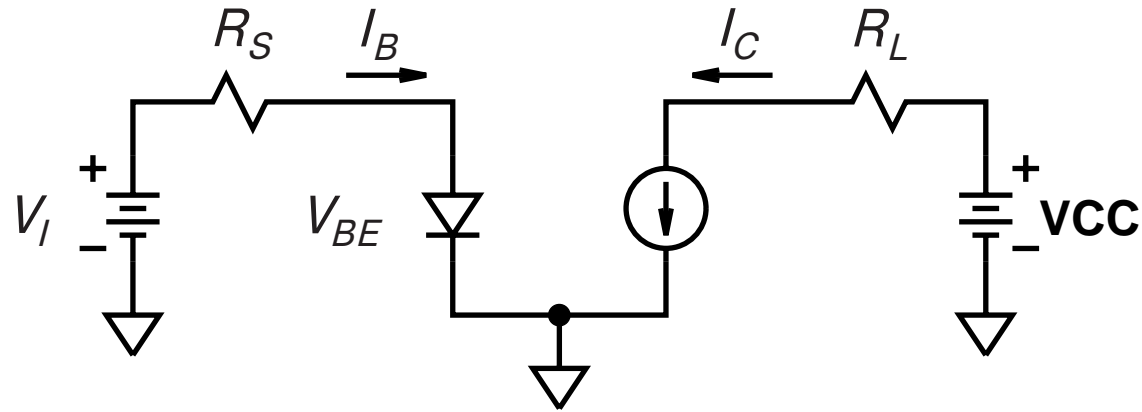
# Common-Emitter Configuration



- DC voltage  $V_I$  establishes bias of  $Q1$  so that it is on the forward-active region. Typically want  $V_O \approx V_{CC}/2$ .

# Common-Emitter Configuration — Bias Analysis

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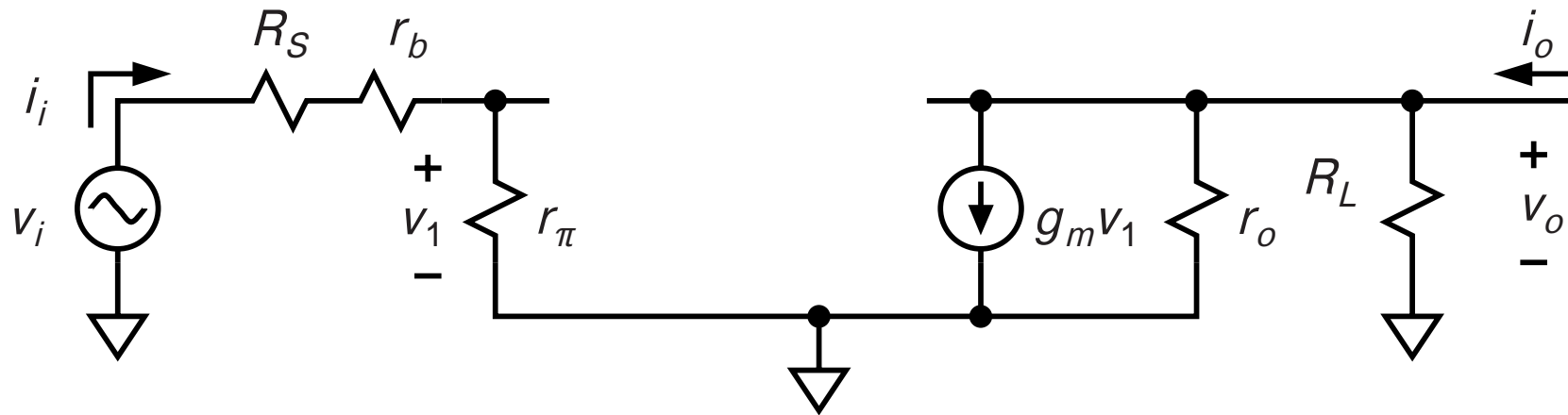
$$I_C = I_S e^{V_{BE}/U_T} = \beta_F I_B$$

If Q1 is in the forward-active region, voltage across the emitter junction can be approximated by a constant  $V_{BE(on)}$ .

$$I_B = \frac{V_I - V_{BE(on)}}{R_S} \quad V_O = V_{CC} - I_C R_L = V_{CC} - \beta_F I_B R_L = V_{CC} - \beta_F \frac{R_L}{R_S} [V_I - V_{BE(on)}]$$

- Dependence on  $\beta_F$  is a problem with this direct approach to biasing.

# Common-Emitter Configuration — Small-Signal Analysis



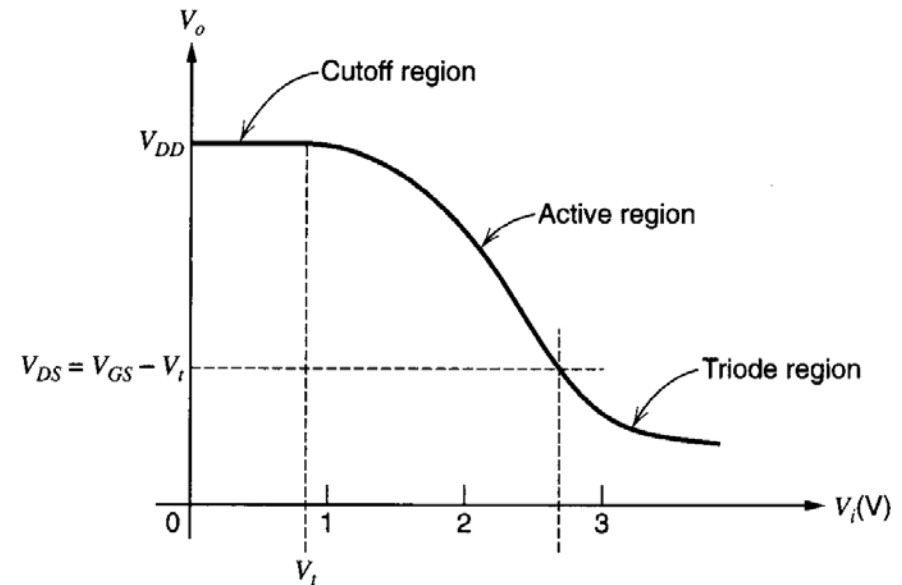
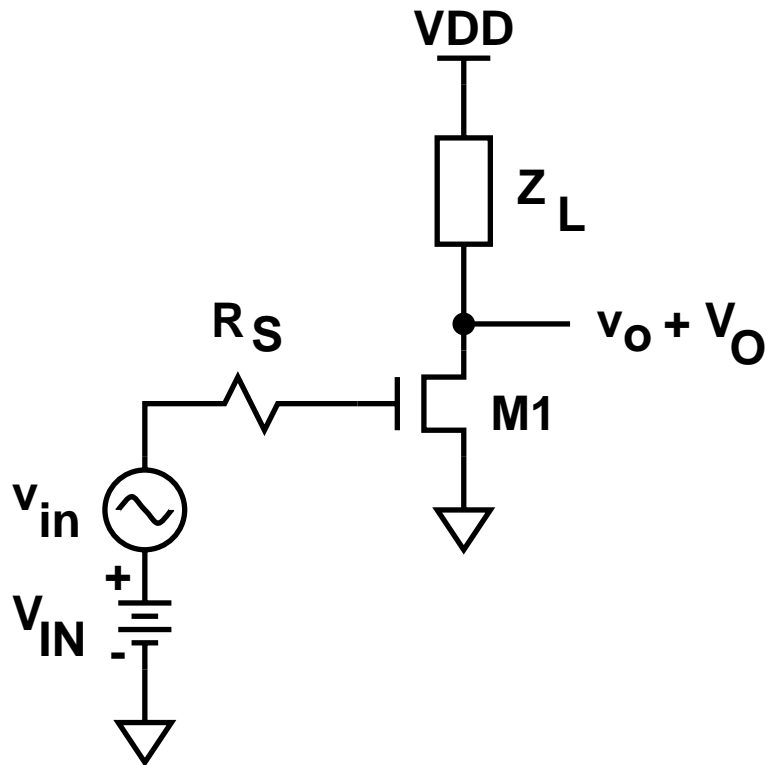
$$A_V(0) \equiv \left. \frac{V_o}{V_i} \right|_{\omega=0} = - \left( \frac{r_\pi}{R'_S + r_\pi} \right) \cdot g_m \cdot (r_o \parallel R_L) \quad \text{where } R'_S \equiv R_S + r_b$$

$$R_i \equiv \frac{V_i}{i_i} = R'_S + r_\pi \quad R_o \equiv \left. \frac{V_o}{i_o} \right|_{v_i=0} = r_o \parallel R_L = R'_L$$

- Note that for  $R'_S \rightarrow 0$  and  $R_L \rightarrow \infty$

$$A_V(0) \rightarrow -g_m r_o = -\frac{1}{\eta} = -\frac{V_A}{U_T}$$

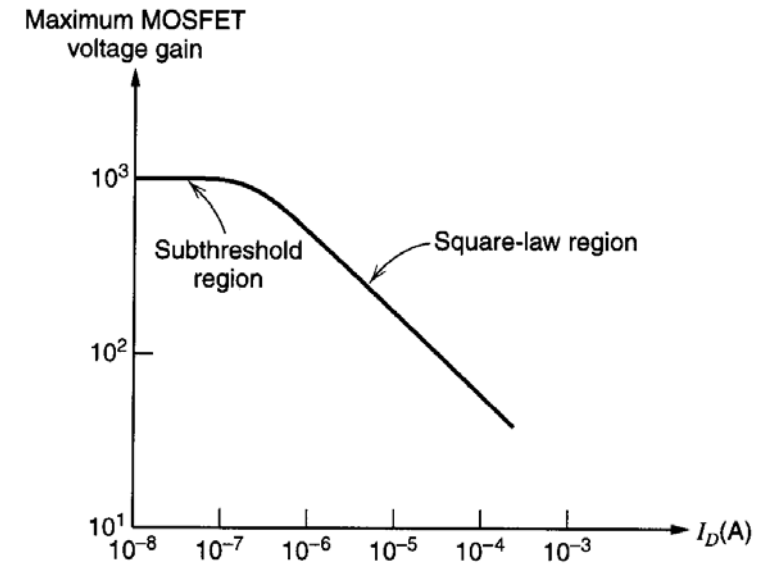
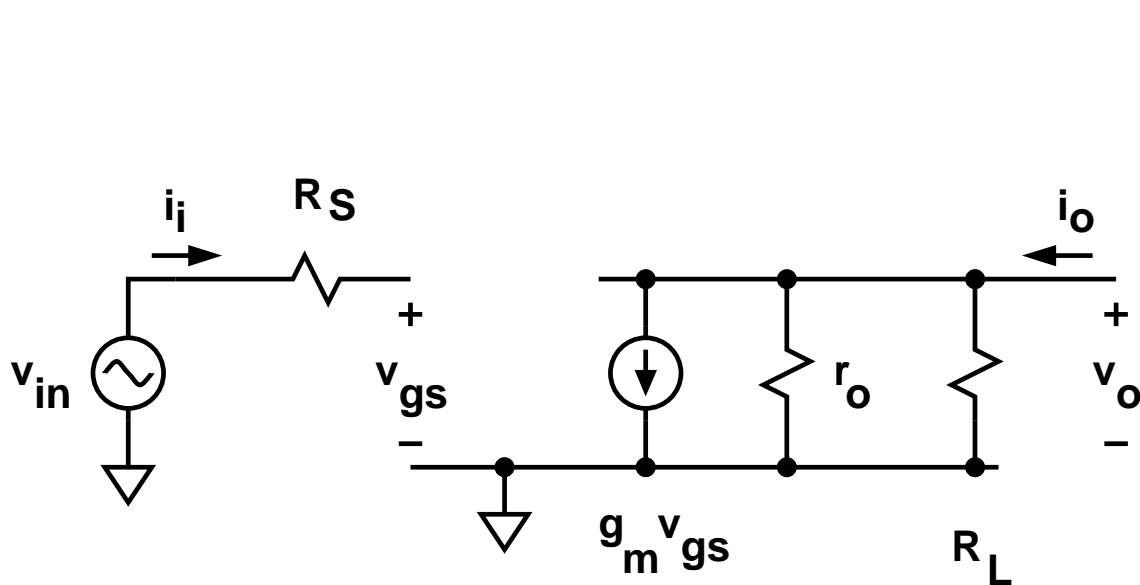
# Common-Source Amplifier



$$V_o = V_{DD} - I_d \cdot R_L = V_{DD} - \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_i - V_{tn})^2 \cdot R_L$$

- DC voltage  $V_i$  is chosen to bias M1 so that M1 is in active (saturation) region and its drain voltage is near the midpoint of the output swing ( $V_O \approx V_{DD}/2$ ).

# Common-Source Configuration — Small-Signal Analysis

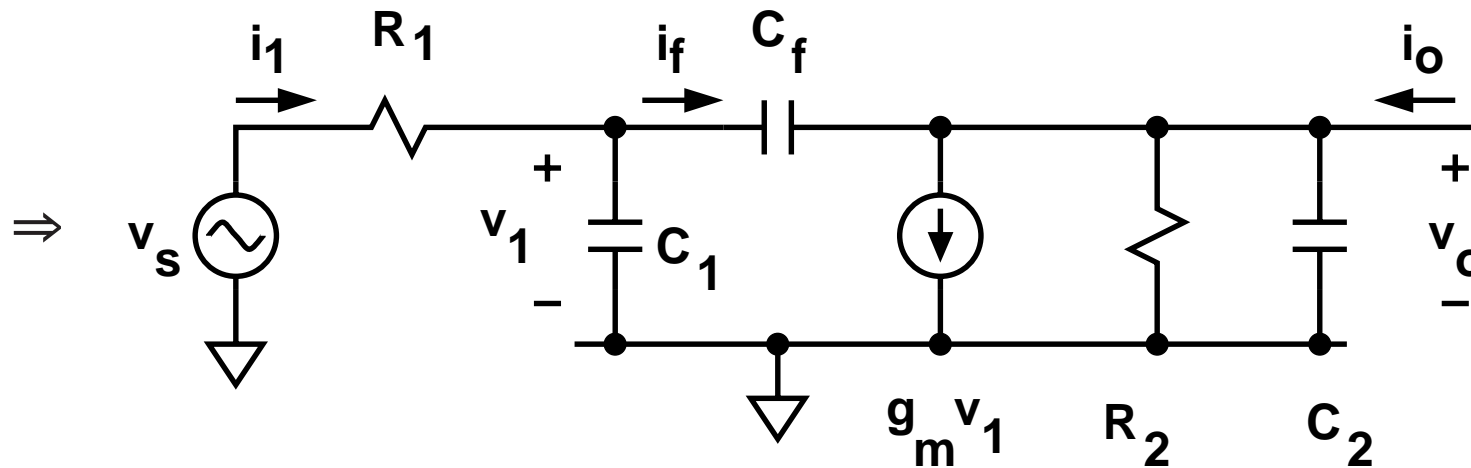
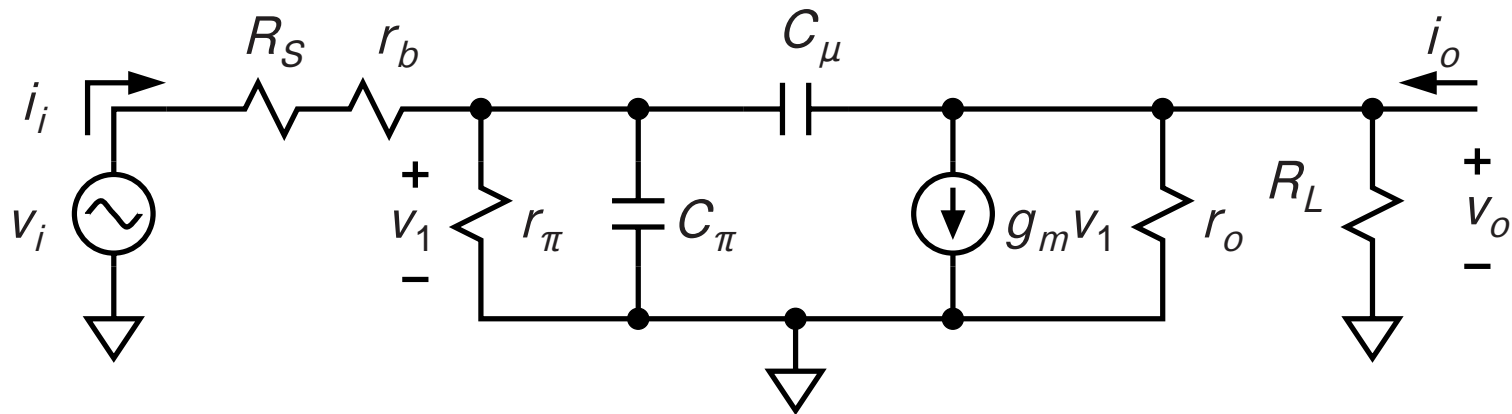


$$A_V(0) = -g_m(r_o \parallel R_L) = -g_m R'_L \quad R_i = \infty \quad R_o = r_o \parallel R_L = R'_L$$

- Note that for  $R_L \rightarrow \infty$ ,  $R'_L \rightarrow r_o$ , and

$$|A_V(0)|_{max} = g_m r_o = \frac{I_D}{V_{ov}/2} \times \frac{L_{eff}}{I_D} \left| \frac{\partial L_{eff}}{\partial V_{DS}} \right|^{-1} = \frac{2L_{eff}}{V_{ov}} \left| \frac{\partial L_{eff}}{\partial V_{DS}} \right|^{-1}$$

# Common-Emitter Configuration Small-Signal AC Analysis

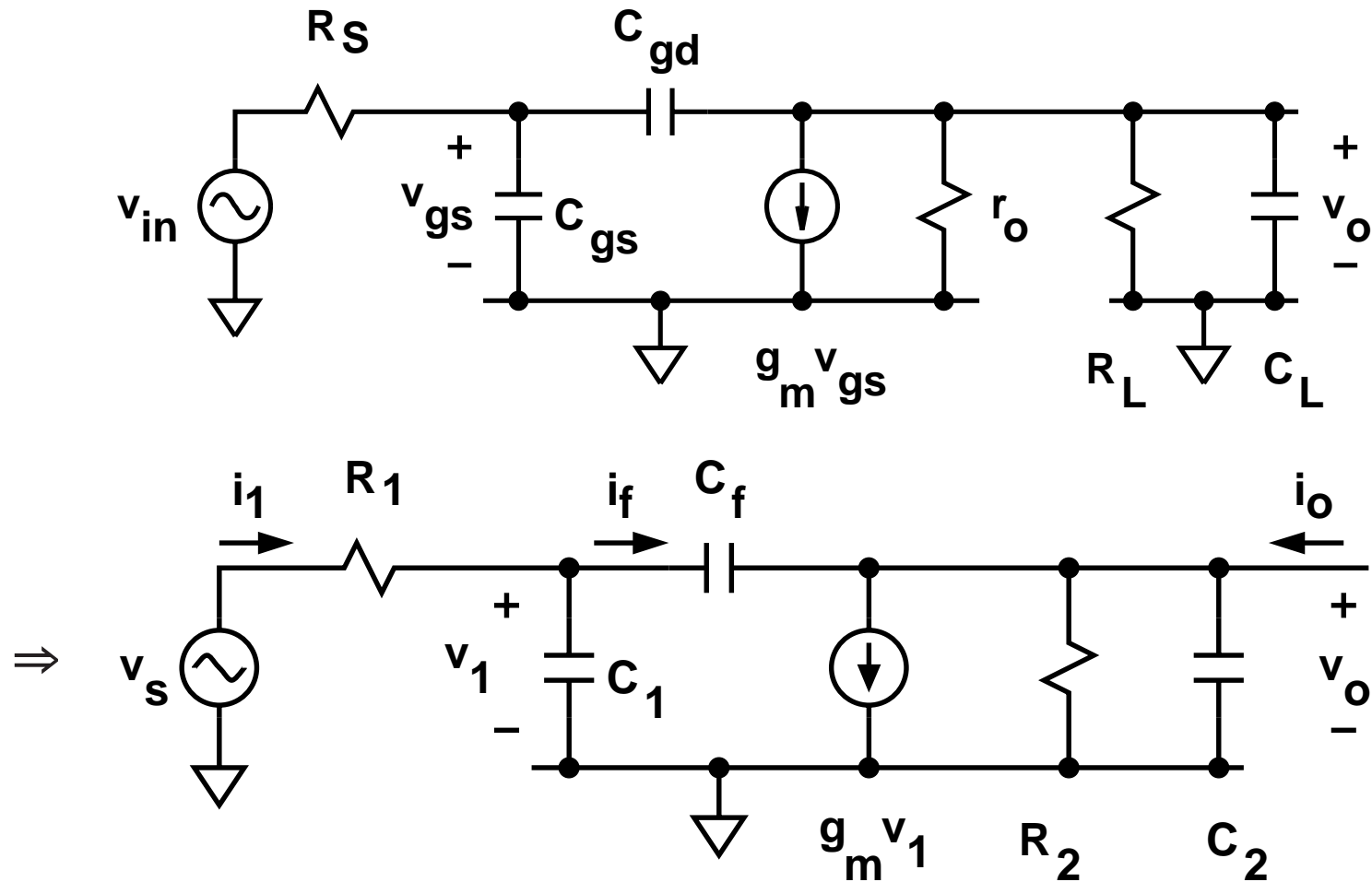


$$v_s = v_i \times \frac{(R_S + r_b) \parallel r_\pi}{R_S + r_b}$$

$$R_1 = (R_S + r_b) \parallel r_\pi \quad R_2 = r_o \parallel R_L$$

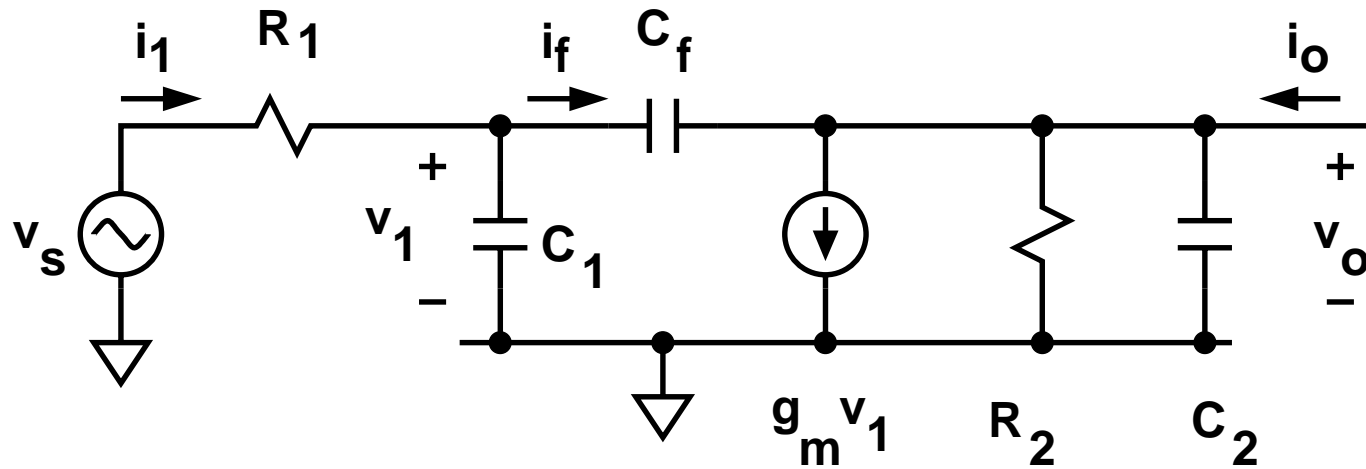
$$C_1 = C_\pi \quad C_2 = C_L + C_{cs} \quad C_f = C_\mu$$

# Common-Source Configuration Small-Signal AC Analysis



$$v_s = v_i \quad R_1 = R_S \quad R_2 = r_o \parallel R_L \quad C_1 = C_{gs} \quad C_2 = C_L \quad C_f = C_{gd}$$

# Miller Approximation



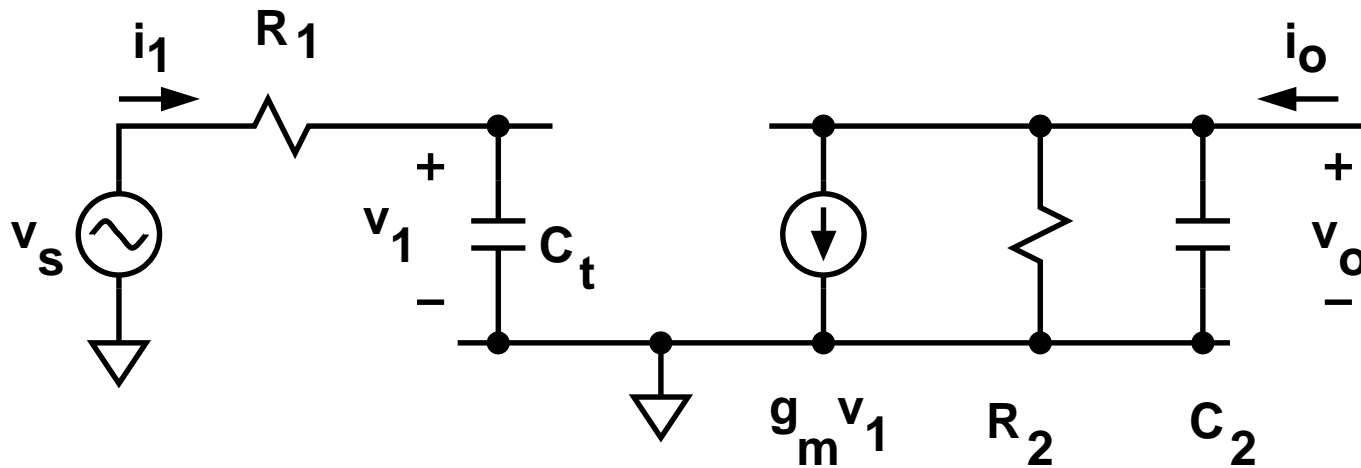
$$v_o = (-g_m v_1 + i_f) \left( R_2 \parallel \frac{1}{sC_2} \right) \quad i_f = (v_1 - v_o) s C_f$$

If  $R_2$ - $C_2$  is a non-dominant pole, then, at the frequencies of interest

$$v_o \approx -g_m R_2 v_1 \quad i_f \approx (v_1 + g_m R_2 v_1) s C_f \quad \Rightarrow \quad \frac{i_f}{v_i} = s(1 + g_m R_2) C_f = s C_M$$

$$C_M = (1 + g_m R_2) \cdot C_f = (1 + a_{v0}) \cdot C_f = \text{Miller Capacitance}$$

# Miller Approximation Equivalent Circuit

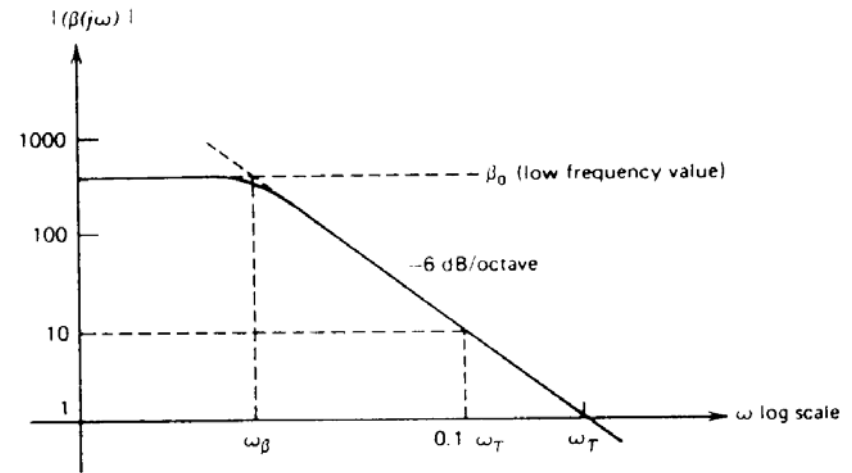
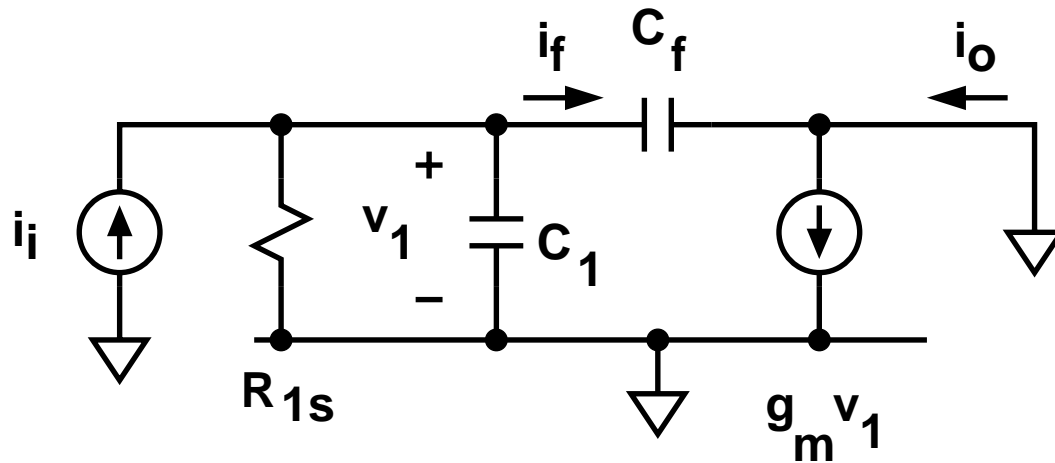


$$C_t = C_1 + C_M = C_1 + (1 + g_m R_2) C_f$$

$$A_v(s) = \frac{V_o}{V_s} = A_v(0) \frac{1}{(1 - s/p_1)(1 - s/p_2)}$$

$$A_v(0) = -g_m R_2 \quad p_1 = \frac{1}{R_1 C_t} \quad p_2 = \frac{1}{R_2 C_2}$$

# Short-Circuit Current Gain



$$i_o \approx -g_m \times v_1 = -g_m \times i_i \frac{R_{1s}}{1 + R_{1s}(C_1 + C_f)s}$$

$$\text{Short-Circuit Current Gain} = \beta(s) = -\frac{i_o}{i_i} = \frac{g_m R_{1s}}{1 + R_{1s}(C_1 + C_f)s} = \frac{\beta_0}{1 + R_{1s}(C_1 + C_f)s}$$

$$\text{Transition Frequency} = \omega_T \approx \frac{g_m}{C_1 + C_f}$$

$$\text{-3 dB Frequency} = \omega_\beta = \frac{1}{R_{1s}(C_1 + C_f)} = \frac{1}{\beta_0} \frac{g_m}{C_1 + C_f} = \frac{\omega_T}{\beta_0}$$

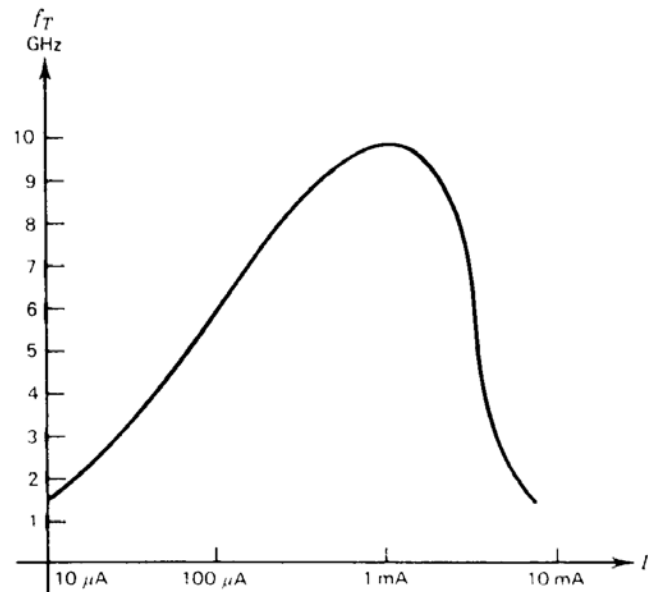
# BJT Transition Frequency

For BJTs, we have

$$R_{1s} = r_{\pi} \quad C_1 = C_{\pi} \quad C_f = C_{\mu}$$

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{\pi} + C_{\mu}}$$

$$\tau_T = \frac{1}{\omega_T} = \frac{C_{\pi}}{g_m} + \frac{C_{\mu}}{g_m} = \frac{C_b}{g_m} + \frac{C_{je}}{g_m} + \frac{C_{jc}}{g_m} = \tau_F + \frac{C_{je}}{g_m} + \frac{C_{jc}}{g_m}$$



# MOST Transition Frequency

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For MOSTs, we have

$$R_{1s} = \infty \quad C_1 = C_{gs} = \frac{2}{3}C_{ox}WL \quad C_f = C_{gd}$$

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs} + C_{gd}}$$

To calculate intrinsic device speed, let  $\omega_T \approx g_m/C_{gs}$ .

- For square-law device,

$$g_m = \mu C_{ox} \frac{W}{L} V_{ov} \quad \Rightarrow \quad \omega_T = \frac{3}{2} \cdot \frac{\mu}{L^2} \cdot V_{ov}$$

- For device with carrier velocity saturation,

$$g_m = WC_{ox}v_{scl} \quad \Rightarrow \quad \omega_T = \frac{3}{2} \cdot \frac{v_{scl}}{L}$$

# MOST Transition Frequency — Weak Inversion

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For MOSTs in the weak inversion region,

$$\omega_T = \frac{g_m}{C_{gb}} \quad g_m = \frac{I_D}{U_T} \frac{C_{ox}}{C_{ox} + C_{depl}} \quad C_{gb} = WL \times \frac{C_{ox} C_{depl}}{C_{ox} + C_{depl}}$$

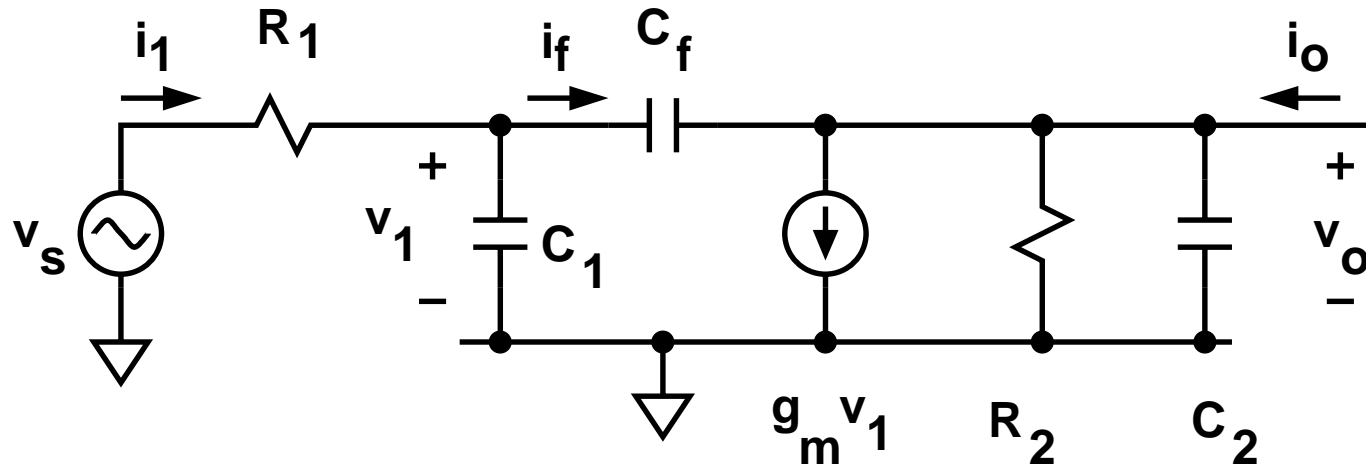
$$\omega_T = \frac{I_D}{U_T} \cdot \frac{1}{WLC_{depl}} = \frac{I_t}{U_T} \cdot \frac{1}{C_{depl}} \cdot \frac{1}{L^2} \cdot \frac{I_D}{I_M}$$

- $I_M = I_t \cdot W/L$  is the maximum  $I_D$  for device in weak inversion.

Since  $I_t \propto D_n$  and  $D_n = \mu U_T$ , we have

$$\omega_T \simeq \frac{D_n}{L^2} \cdot \frac{I_D}{I_M} \simeq \frac{\mu}{L^2} \cdot U_T \cdot \frac{I_D}{I_M}$$

# Complete AC Analysis of Common-Emitter(Source) Amplifier



$$A_V(s) = \frac{v_o(s)}{v_s(s)} = A_V(0) \frac{1 - s/z_1}{1 + b_1 s + b_2 s^2}$$

$$A_V(0) = -g_m R_2$$

$$z_1 = +\frac{g_m}{C_f}$$

$$b_1 = R_1(C_1 + C_f) + R_2(C_2 + C_f) + g_m R_1 R_2 C_f$$

$$b_2 = R_1 R_2 (C_1 C_2 + C_1 C_f + C_2 C_f)$$

# Complete AC Analysis of Common-Emitter(Source) Amplifier

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Using the *dominant-pole approximation*, let  $|p_1| \ll |p_2|$

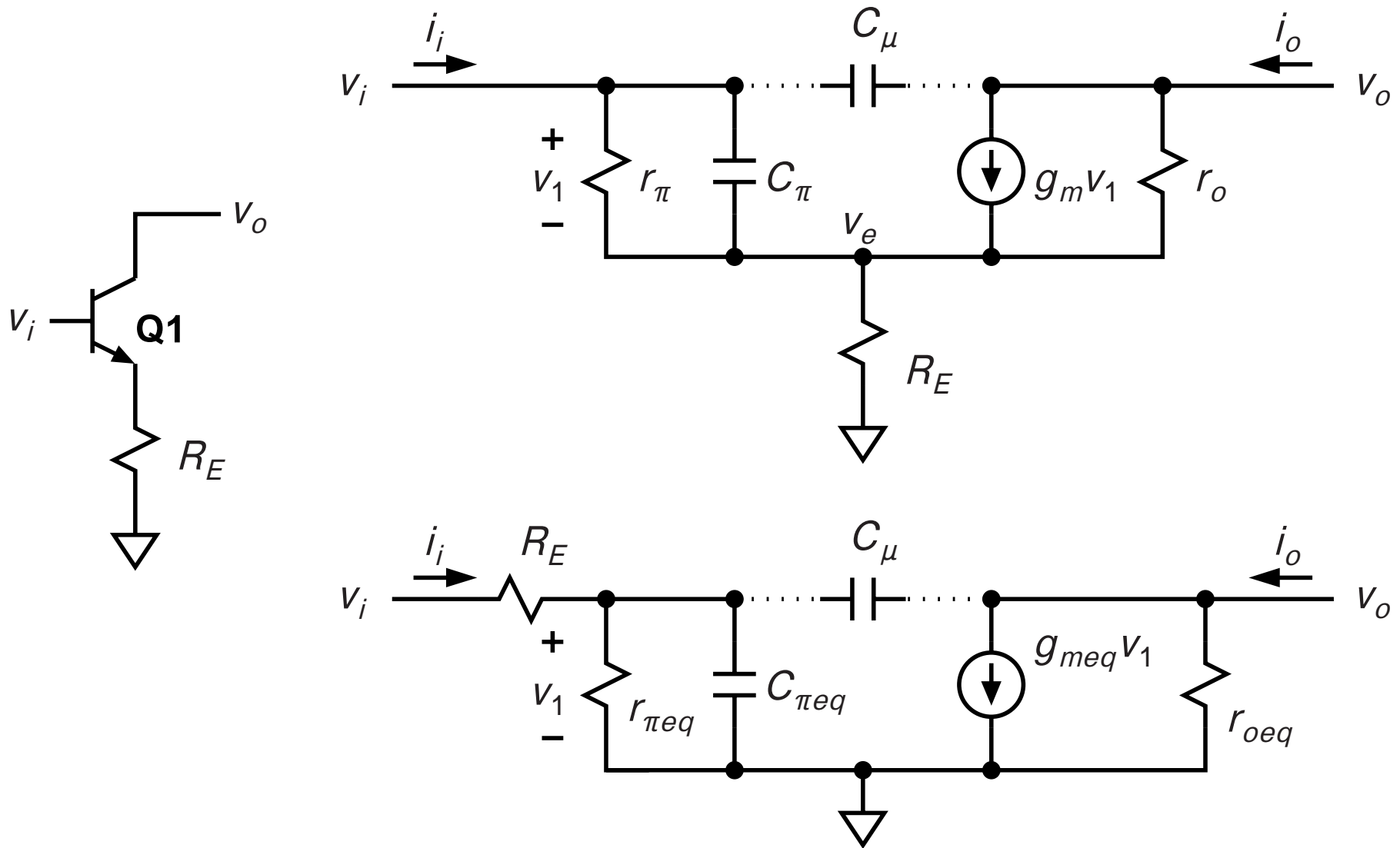
$$D(s) = 1 + b_1s + b_2s^2$$

$$= \left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right) = 1 - s \left(\frac{1}{p_1} + \frac{1}{p_2}\right) + \frac{s^2}{p_1p_2} \approx 1 - \frac{s}{p_1} + \frac{s^2}{p_1p_2}$$

$$p_1 \approx -\frac{1}{b_1} = \frac{1}{R_1[C_1 + C_f(1 + g_m R_2)] + R_2(C_2 + C_f)} \approx -\frac{1}{R_1[C_1 + C_f(1 + g_m R_2)]}$$
$$p_2 \approx -\frac{b_1}{b_2} = \frac{R_1(C_1 + C_f) + R_2(C_2 + C_f) + g_m R_1 R_2 C_f}{R_1 R_2 (C_1 C_2 + C_1 C_f + C_2 C_f)} \approx -\frac{g_m C_f}{C_1 C_2 + C_1 C_f + C_2 C_f}$$

- The Miller approximation is a simplified dominant pole approximation.
- The Miller approximation results in incorrect estimation for the second pole.

# Common-Emitter Amplifier with Emitter Degeneration



# Common-Emitter Amplifier with Emitter Degeneration

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To find  $r_{\pi eq}$ ,  $C_{\pi eq}$ , and  $g_{meq}$ , let  $v_o = 0$ , then

$$(g_m + g_\pi + sC_\pi)(v_i - v_e) = (G_E + g_o)v_e$$

At frequencies where  $\omega \ll \omega_T = g_m/(C_\pi + C_\mu)$ ,

$$\frac{v_e}{v_i} = \frac{g_m + g_\pi + sC_\pi}{g_m + g_\pi + G_E + g_o + sC_\pi} \approx \frac{g_m + g_\pi}{g_m + g_\pi + G_E + g_o}$$

$$g_{meq} = \frac{-i_o}{v_i} = g_m \left(1 - \frac{v_e}{v_i}\right) - g_o \cdot \frac{v_e}{v_i} = \frac{g_m G_E - g_o g_\pi}{g_m + g_\pi + G_E + g_o} = g_m \cdot \frac{1 - \frac{R_E}{\beta_o r_o}}{1 + g_m R_E \left(1 + \frac{1}{\beta_o} + \frac{1}{g_m r_o}\right)}$$

$$\frac{i_j}{v_i} = (g_\pi + sC_\pi) \left(1 - \frac{v_e}{v_i}\right) = (g_\pi + sC_\pi) \frac{1 + \frac{R_E}{r_o}}{1 + g_m R_E \left(1 + \frac{1}{\beta_o} + \frac{1}{g_m r_o}\right)}$$

# Common-Emitter Amplifier with Emitter Degeneration

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- If  $\beta_0 \gg 1$ ,  $r_o \gg R_E$ , and  $g_m r_o \gg 1$

$$g_{meq} \approx \frac{g_m}{1 + g_m R_E} \quad r_{\pi eq} \approx r_\pi (1 + g_m R_E) \quad C_{\pi eq} \approx \frac{C_\pi}{1 + g_m R_E}$$

To find  $r_{oeq}$ , let  $v_i = 0$ , then

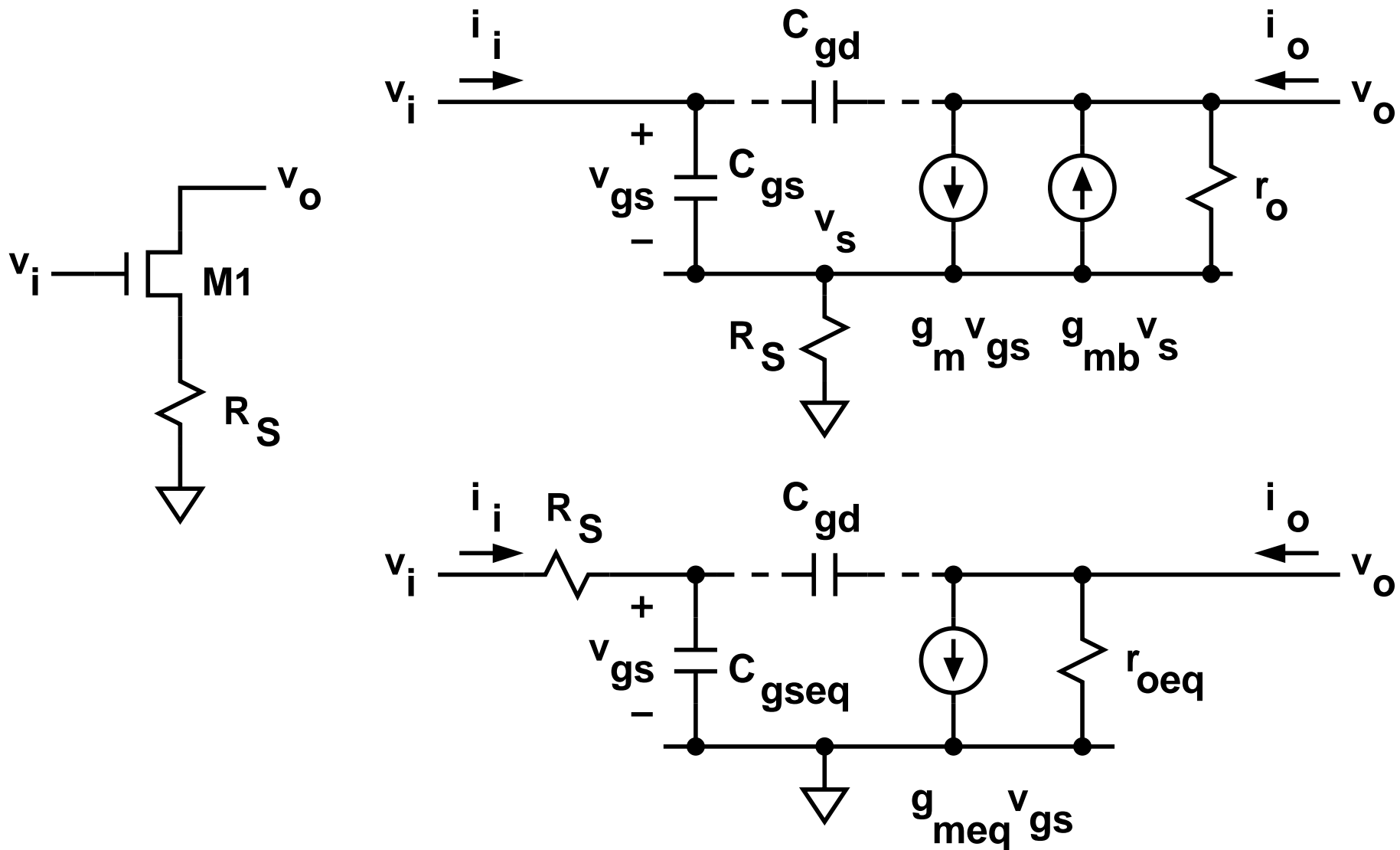
$$(g_m + g_\pi + sC_\pi + G_E)v_e = g_o(v_o - v_e)$$

$$\frac{v_e}{v_o} = \frac{g_o}{g_m + g_\pi + G_E + g_o + sC_\pi} \approx \frac{g_o}{g_m + g_\pi + G_E + g_o}$$

$$g_{oeq} = \frac{i_o}{v_o} = g_o \left(1 - \frac{v_e}{v_o}\right) - g_m \frac{v_e}{v_o} = g_o \cdot \frac{g_\pi + G_E}{g_m + g_\pi + G_E + g_o} = g_o \cdot \frac{1 + \frac{g_m R_E}{\beta_0}}{1 + g_m R_E \left(1 + \frac{1}{\beta_0} + \frac{1}{g_m r_o}\right)}$$

$$r_{oeq} \approx r_o(1 + g_m R_E) \quad \text{if } g_m R_E \ll \beta_0 \quad r_{oeq} \approx r_o(1 + \beta_0) \quad \text{if } g_m R_E \gg \beta_0$$

# Common-Source Amplifier with Source Degeneration



# Common-Source Amplifier with Source Degeneration

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To find  $C_{gseq}$  and  $g_{meq}$ , let  $v_o = 0$ , then

$$(g_m + sC_{gs})(v_i - v_s) = (G_S + g_{mb} + g_o)v_s$$

At frequencies where  $\omega \ll \omega_T = g_m/C_{gs}$ ,

$$\frac{v_s}{v_i} = \frac{g_m + sC_{gs}}{g_m + g_{mb} + G_S + g_o + sC_{gs}} \approx \frac{g_m}{g_m + g_{mb} + G_S + g_o}$$

$$g_{meq} = \frac{-i_o}{v_i} = g_m \left(1 - \frac{v_s}{v_i}\right) - (g_{mb} + g_o) \frac{v_s}{v_i} = \frac{g_m G_S}{g_m + g_{mb} + G_S + g_o} = \frac{g_m}{1 + (g_m + g_{mb})R_S + \frac{R_S}{r_o}}$$

$$\frac{i_i}{v_i} = sC_{gs} \left(1 - \frac{v_s}{v_i}\right) = sC_{gs} \cdot \frac{1 + g_{mb}R_S + \frac{R_S}{r_o}}{1 + (g_m + g_{mb})R_S + \frac{R_S}{r_o}}$$

# Common-Source Amplifier with Source Degeneration

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- If  $r_o \gg R_S$ ,

$$g_{meq} \approx \frac{g_m}{1 + (g_m + g_{mb})R_S} = \frac{g_m}{1 + (1 + \chi)g_m R_S}$$

$$C_{gseq} = C_{gs} \cdot \frac{1 + g_{mb}R_S}{1 + (g_m + g_{mb})R_S} = C_{gs} \cdot \frac{1 + \chi g_m R_S}{1 + (1 + \chi)g_m R_S}$$

To find  $r_{oeq}$ , let  $v_i = 0$ , then

$$(g_m + g_{mb} + sC_{gs} + G_S)v_s = g_o(v_o - v_s)$$

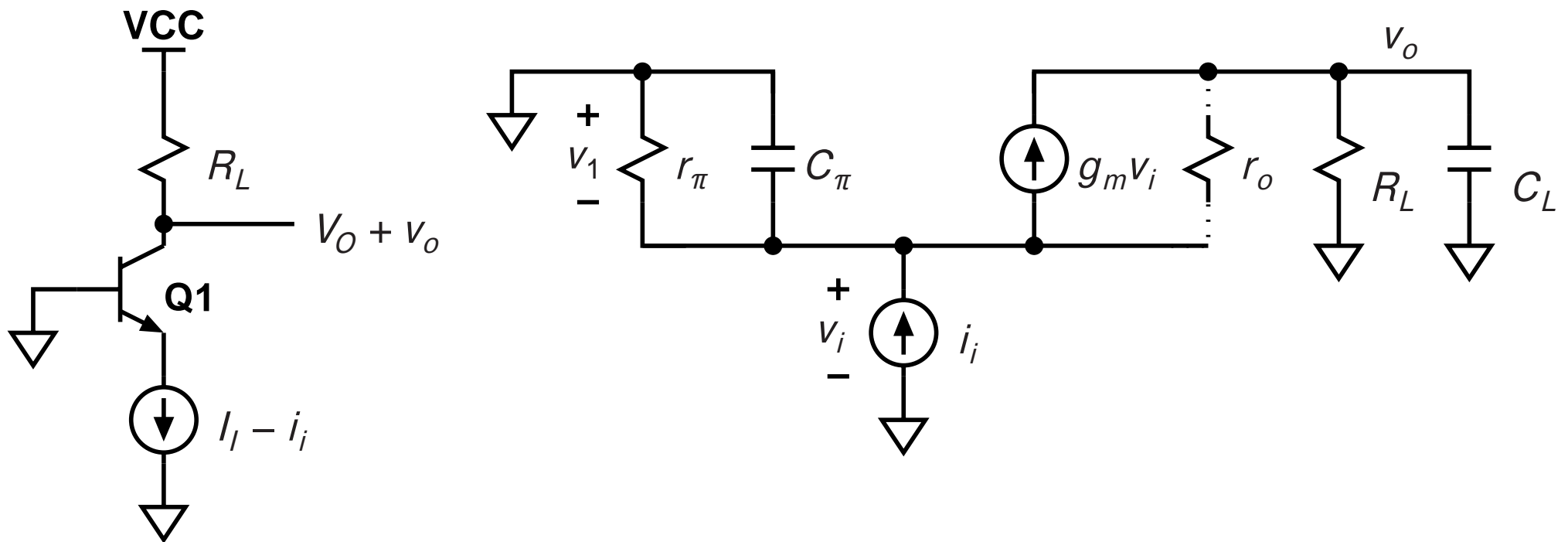
$$\frac{v_s}{v_o} = \frac{g_o}{g_m + g_{mb} + G_S + g_o + sC_{gs}} \approx \frac{g_o}{g_m + g_{mb} + G_S + g_o}$$

$$g_{oeq} = \frac{i_o}{v_o} = g_o \left(1 - \frac{v_e}{v_o}\right) - (g_m + g_{mb})\frac{v_e}{v_o} = \frac{g_o G_S}{g_m + g_{mb} + G_S + g_o}$$

$$r_{oeq} = R_S + r_o[1 + (g_m + g_{mb})R_S]$$

- $r_{oeq}$  can be made arbitrarily large by increasing  $R_S$ .

# Common-Base Configuration



- It is a current buffer, i.e., current gain  $\simeq 1$ , low  $R_{in}$ , and high  $R_{out}$ .
- Typically neglect  $r_b$ ,  $r_c$ , and  $r_e$ , so that  $v_1 = -v_i$ .
- Combine  $C_\mu$ ,  $C_{CS}$ , and load capacitance into  $C_L$ .

# Common-Base Configuration AC Analysis

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To further simplify the analysis, neglect  $r_o$ ; i.e., assume  $g_o(v_o - v_i) \ll g_m v_i$ , then

$$(g_\pi + sC_\pi)v_i + g_m v_i = i_i \quad (G_L + sC_L)v_o = g_m v_i$$

$$\Rightarrow Z_t(s) = \frac{v_o(s)}{i_i(s)} = \frac{g_m}{g_m + g_\pi + sC_\pi} \times \frac{1}{G_L + sC_L} = \frac{Z_t(0)}{(1 - s/p_1)(1 - s/p_2)}$$

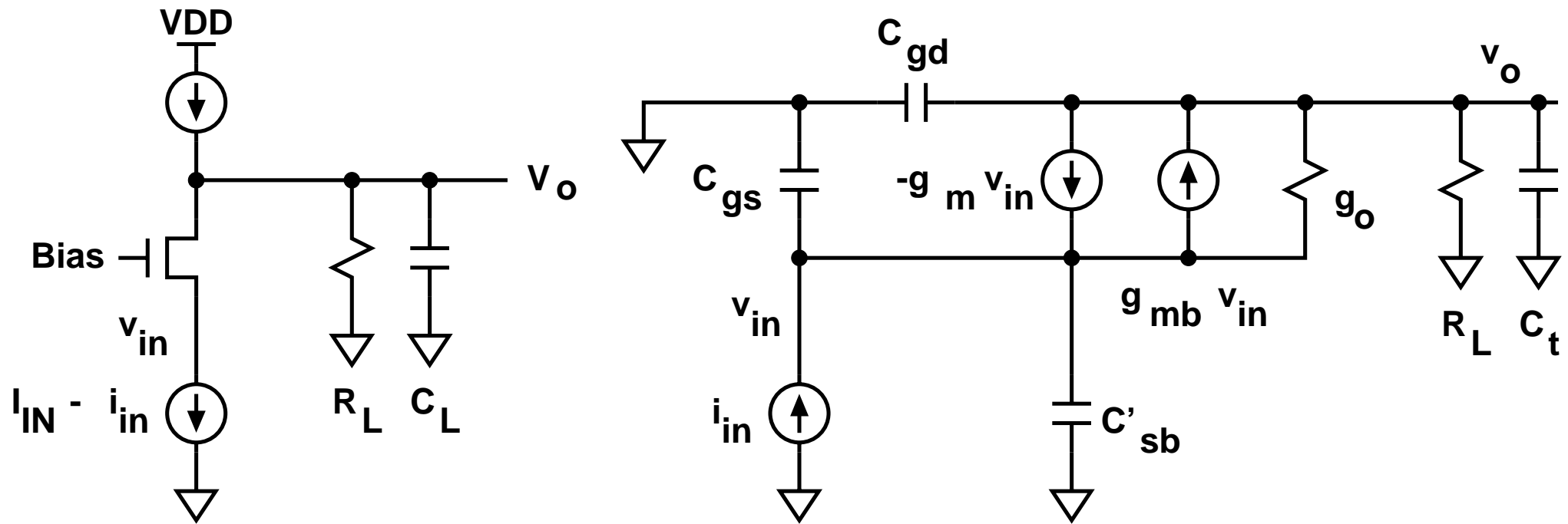
$$Z_t(0) = \frac{g_m}{g_m + g_\pi} R_L = \frac{\beta_o}{\beta_o + 1} R_L = \alpha_o R_L \quad p_1 = -\frac{g_m + g_\pi}{C_\pi} = -\frac{1}{\alpha_o} \frac{g_m}{C_\pi} \quad p_2 = -\frac{1}{R_L C_L}$$

$$\text{Input Impedance} = Z_{in}(s) = \frac{v_i(s)}{i_i(s)} = \frac{R_{in}}{1 - s/p_1} \quad R_{in} = Z_{in}(0) = r_\pi \parallel \frac{1}{g_m} = \frac{\alpha_o}{g_m}$$

$$\text{Current Gain} = \frac{i_o(s)}{i_i(s)} = \frac{g_m v_i}{i_i} = g_m Z_{in}(s) = \frac{\alpha_o}{1 - s/p_1}$$

- Note that  $|p_1| = (1/\alpha_o)(g_m/C_\pi) > \omega_T = g_m/(C_\pi + C_\mu)$ .
- Expect  $|p_2| < |p_1|$  in typical cases.

# Common-Gate Configuration



$$g'_m = g_m + g_{mb}$$

$$C'_L = C_t + C_{gd} = C_L + C_{db} + C_{gd}$$

$$C_{in} = C_{gs} + C'_{sb}$$

The nodal equations are

$$i_{in} = (g'_m + sC_{in})v_{in} - g_o(v_o - v_{in}) \quad g'_m v_{in} = (G_L + sC'_L)v_o + g_o(v_o - v_{in})$$

# Common-Gate Configuration AC Analysis

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If the  $g_o(v_o - v_{in})$  terms are neglected, then

$$\text{Transimpedance} = Z_t(s) = \frac{v_o}{i_{in}} = \frac{R_L}{(1 - s/p_1)(1 - s/p_2)}$$

$$p_1 = -\frac{g'_m}{C_{in}} = -\frac{g'_m}{C_{gs} + C'_{sb}} \quad p_2 = -\frac{1}{R_L C'_L}$$

$$\text{Input Impedance} = Z_{in}(s) = \frac{v_{in}(s)}{i_{in}(s)} = \frac{1/g'_m}{1 - s/p_1}$$

$$\text{Current Gain} = \frac{i_o(s)}{i_{in}(s)} = \frac{g'_m v_{in}}{i_{in}} = g'_m Z_{in}(s) = \frac{1}{1 - s/p_1}$$

- Note that  $p_1 \simeq \omega_T = g_m / (C_{gs} + C_{gd})$ .

# Common-Gate Configuration AC Analysis

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If  $g_o$  is considered,

$$\text{Voltage Gain} = A_V(s) = \frac{V_o}{V_{in}} = \frac{g'_m + g_o}{g_o + G_L + sC'_L}$$

$$\text{Input Impedance} = Y_{in}(s) = \frac{i_{in}}{V_{in}} = g'_m + sC_{in} - g_o(A_V - 1)$$

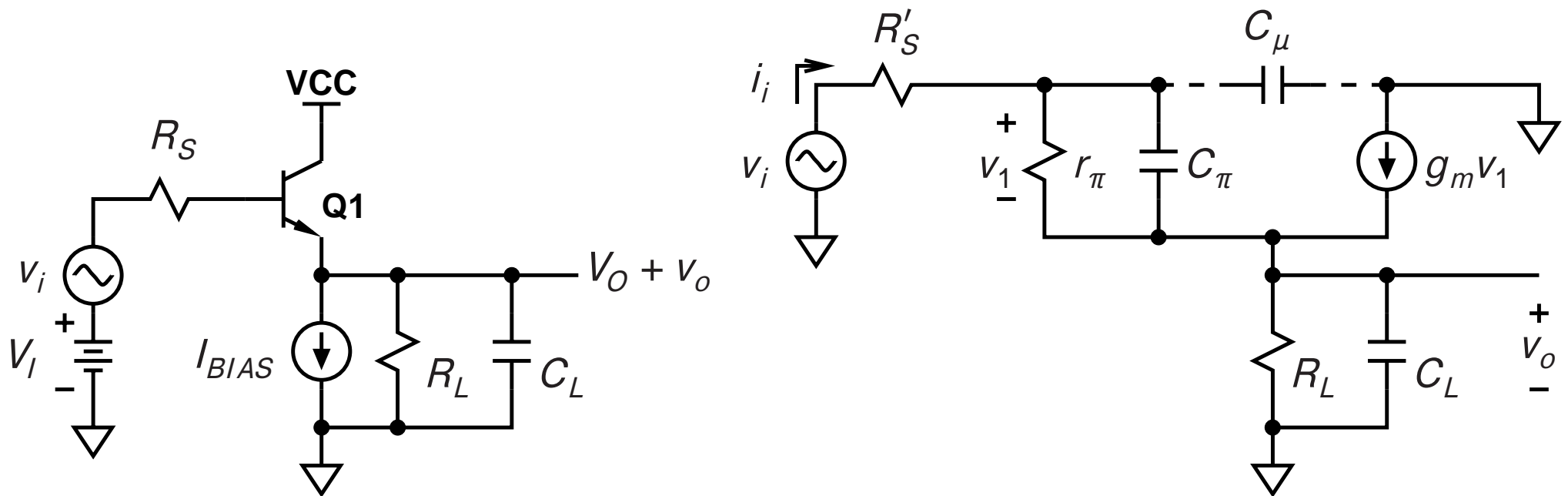
$$Z_t(s) = \frac{V_o}{i_{in}} = \frac{A_V(s)}{Y_{in}(s)}$$

- At low frequencies where  $\omega \rightarrow 0$ , assuming  $g'_m \gg g_o$ ,

$$A_V = \frac{g'_m + g_o}{g_o + G_L} \approx \frac{g'_m}{g_o + G_L}$$

$$\Rightarrow Y_{in} = g'_m - \frac{g'_m}{1 + \frac{G_L}{g_o}} + g_o \approx \frac{g'_m}{1 + \frac{R_L}{r_o}} \quad Z_t = \frac{A_V}{Y_{in}} \approx R_L$$

# Common-Collector Configuration (Emitter Follower)



$$R'_S = R_S + r_b$$

- It is a voltage buffer, i.e., voltage gain  $\simeq 1$ , high  $Z_{in}$ , and low  $Z_{out}$ .
- Neglect  $C_\mu$ ,  $r_e$ ,  $r_c$ , and  $r_o$  in the following analysis.

# Emitter Follower's Voltage Gain

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Summing currents at the output, we have

$$i_i v_1 + g_m v_1 = (G_L + sC_L)v_o \quad i_i = (g_\pi + sC_\pi)v_1 \quad v_i = R'_S i_i + v_1 + v_o$$

We have

$$A_v(s) = \frac{g_m + g_\pi + sC_\pi}{g_m + g_\pi + sC_\pi + (G_L + sC_L)[1 + R'_S(g_\pi + sC_\pi)]} = A_v(0) \frac{1 - s/z_1}{1 + b_1 s + b_2 s^2}$$

$$A_v(0) = \frac{g_m + g_\pi}{g_m + g_\pi + G_L(1 + R'_S g_\pi)} = \frac{g_m/\alpha_o}{g_m/\alpha_o + \frac{1}{R_L}(1 + g_m R'_S/\beta_o)} = \frac{g_m R_L}{g_m R_L + \alpha_o + \frac{g_m R'_S}{\beta_o + 1}}$$

$$z_1 = -\frac{g_m + g_\pi}{C_\pi} = -\frac{g_m/\alpha_o}{C_\pi} \simeq -\omega_T$$

$$b_1 = \frac{R_L[C_\pi(1 + R'_S/R_L) + C_L(1 + g_m R'_S/\beta_o)]}{1 + g_m(R_L/\alpha_o + R'_S/\beta_o)} \quad b_2 = \frac{R_L R'_S C_\pi C_L}{1 + g_m(R_L/\alpha_o + R'_S/\beta_o)}$$

# Emitter Follower's Voltage Gain

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- If  $C_L = 0$ , then  $b_2 = 0$  and

$$A_V(s) = A_V(0) \frac{1 - s/z_1}{1 - s/p_1}$$

$$p_1 = -\frac{1 + g_m(R_L/\alpha_o + R'_S/\beta_o)}{(R_L + R'_S)C_\pi} \approx -\frac{1 + g_m R_L}{(R_L + R'_S)C_\pi}$$

$A_V(0)$  &  $z_1$  are unchanged from case where  $C_L \neq 0$ .

- If  $R'_S = 0$ , again  $b_2 = 0$  and

$$A_V(s) = A_V(0) \frac{1 - s/z_1}{1 - s/p_1}$$

$$A_V(0) = \frac{g_m R_L}{\alpha_o + g_m R_L} \approx \frac{g_m R_L}{1 + g_m R_L} \quad p_1 = -\frac{1 + g_m R_L/\alpha_o}{R_L(C_\pi + C_L)} \approx -\frac{g_m}{C_\pi + C_L} \text{ if } g_m R_L \gg 1$$

$z_1$  is unchanged from case where  $R'_S \neq 0$ .

# Emitter Follower's Input Impedance

$$Z_{in}(s) = \frac{v_i(s)}{i_i(s)} = R'_S + \frac{1}{g_\pi + sC_\pi} + \frac{1 + g_m/(g_\pi + sC_\pi)}{G_L + sC_L} = R'_S + R_{in} \frac{1 - s/z_1}{(1 - s/p_1)(1 - s/p_2)}$$

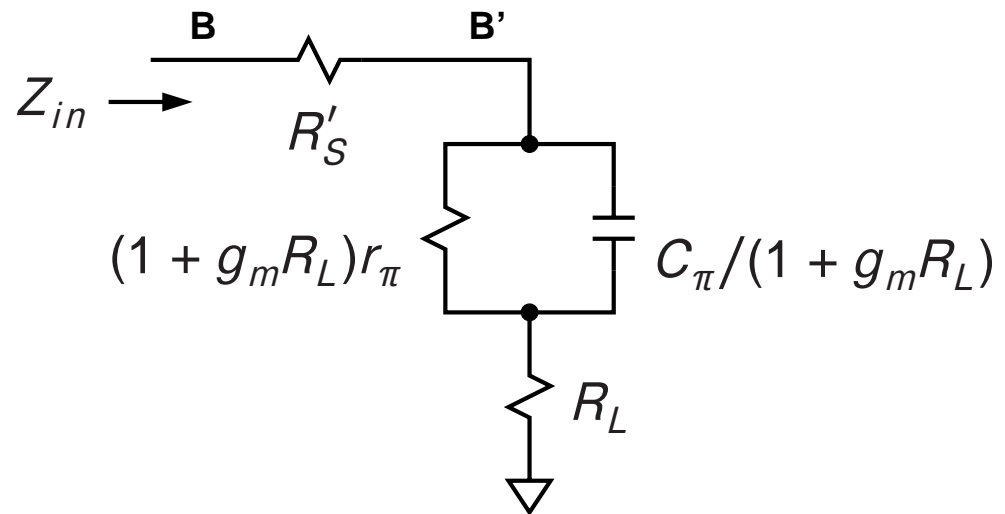
$$R_{in} = (G_L + g_m/\alpha_o)/(G_L + g_\pi) = r_\pi + (\beta_o + 1)R_L \approx r_\pi(1 + g_mR_L)$$

$$z_1 = -\frac{g_m/\alpha_o + G_L}{(\beta_o + 1)C_\pi + C_L} = -\frac{1 + g_mR_L/\alpha_o}{R_L[(\beta_o + 1)C_\pi + C_L]} \approx -\frac{g_m}{(\beta_o + 1)C_\pi + C_L} \text{ if } g_mR_L \gg 1$$

$$p_1 = -\frac{1}{r_\pi C_\pi} = -\frac{g_m}{\beta_o C_\pi} \approx -\frac{\omega_T}{\beta_o} \quad p_2 = -\frac{1}{R_L C_L}$$

If  $C_L = 0$ , then

$$Z_{in}(s) = R'_S + \frac{1 + g_mR_L}{g_\pi + sC_\pi} + R_L$$



# Emitter Follower's Output Impedance

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The output impedance looking into the transistor's emitter is

$$Z_{out}(s) = \frac{1 + R'_S(g_\pi + sC_\pi)}{g_m + g_\pi + sC_\pi} = R_{out} \frac{1 - s/z_1}{1 - s/p_1}$$

$$Z_{out}(0) = R_{out} = \frac{1 + R'_S g_\pi}{g_m + g_\pi} = \frac{r_\pi + R'_S}{g_m r_\pi + 1} = \frac{r_\pi + R'_S}{\beta_o + 1} \quad Z_{out}(\infty) = R'_S$$
$$z_1 = -\frac{1 + R'_S g_\pi}{R'_S C_\pi} = -\frac{r_\pi + R'_S}{r_\pi R'_S C_\pi} = -\frac{1}{(r_\pi \parallel R'_S) C_\pi} \quad p_1 = -\frac{g_m / \alpha_o}{C_\pi} \approx -\omega_T$$

- If  $r_\pi \parallel R'_S > \alpha_o / g_m$  (or  $R'_S > 1/g_m$  if  $\beta_o \gg 1$ ),  $|z_1| < |p_1|$ , which represents inductive behavior.
- In addition, if  $R'_S \gg r_\pi$

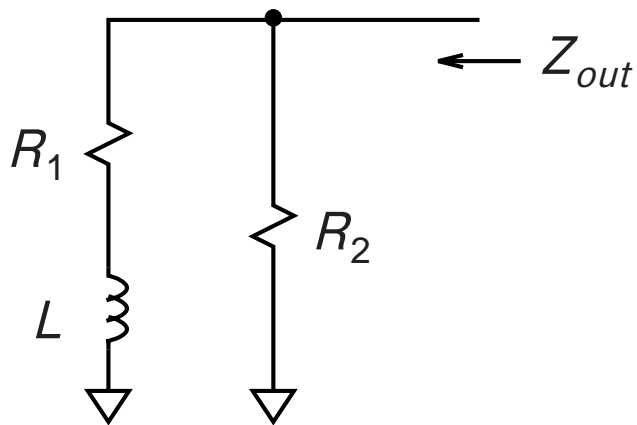
$$|z_1| \approx \frac{1}{r_\pi C_\pi} = \frac{g_m}{\beta_o C_\pi} \approx \frac{|p_1|}{\beta_o}$$

# Emitter Follower's Output Impedance

If  $\beta_o \gg 1$ ,  $Z_{out}(s)$  can be rewritten as:

$$Z_{out}(s) = \frac{r_{\pi} + R'_S + sC_{\pi}r_{\pi}R'_S}{\beta_o + 1 + sC_{\pi}r_{\pi}} \approx \frac{\left(\frac{1}{g_m} + \frac{R'_S}{\beta_o} + sC_{\pi}r_{\pi}\frac{R'_S}{\beta_o}\right) R'_S}{R'_S + sC_{\pi}r_{\pi}\frac{R'_S}{\beta_o}}$$

If  $R_2 \gg R_1$ , we have

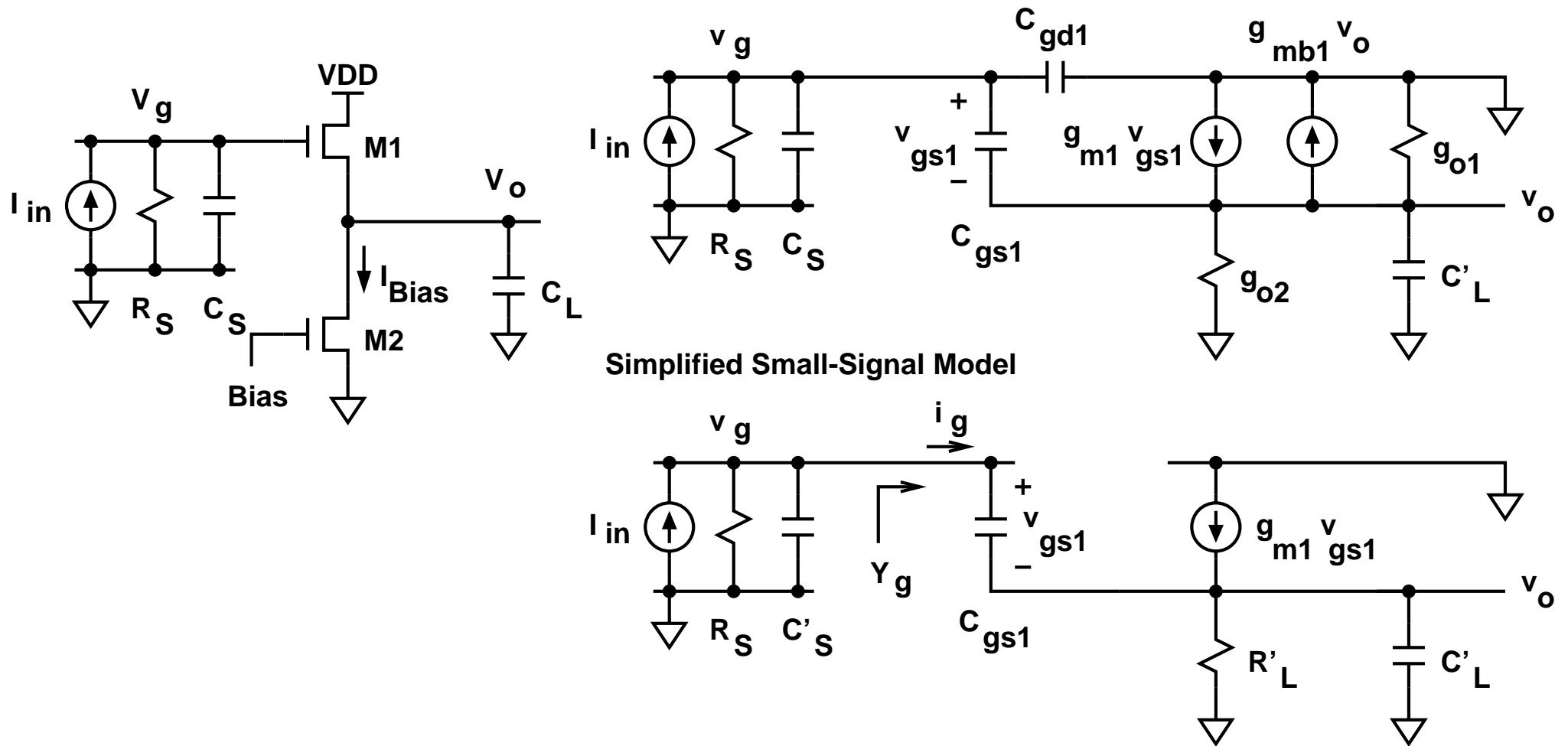


$$Z_{out}(s) = \frac{(R_1 + sL)R_2}{R_1 + R_2 + sL} \approx \frac{(R_1 + sL)R_2}{R_2 + sL}$$

Then

$$R_1 = \frac{1}{g_m} + \frac{R'_S}{\beta_o} \quad R_2 = R'_S \quad L = C_{\pi}r_{\pi}\frac{R'_S}{\beta_o}$$

# Common-Drain Configuration (Source Follower)



$$C'_S = C_S + C_{gd1} \quad C'_L = C_L + C'_{sb1} + C_{db2} + C_{gd2} \quad G'_L = g_{o1} + g_{o2} + g_{mb1} = \frac{1}{R'_L}$$

## Source Follower's Gate Voltage Gain

---

Summing the currents at the output node, we have

$$(g_{m1} + sC_{gs1})(v_g - v_o) - v_o(sC'_L + G'_L) = 0$$

The voltage gain from gate to output is

$$A_{vg}(s) \equiv \frac{v_o(s)}{v_g(s)} = \frac{g_{m1} + sC_{gs1}}{g_{m1} + G'_L + s(C_{gs1} + C'_L)} = A_{vg}(0) \frac{1 - s/z_1}{1 - s/p_1}$$

$$A_{vg}(0) = \frac{g_{m1}}{g_{m1} + G'_L} = \frac{g_{m1}}{g_{m1} + g_{mb1} + g_{o1} + g_{o2}} \quad A_{vg}(\infty) = \frac{C_{gs1}}{C_{gs1} + C'_L}$$

$$z_1 = -\frac{g_{m1}}{C_{gs1}} \approx -\omega_T \quad p_1 = -\frac{g_{m1} + G'_L}{C_{gs1} + C'_L}$$

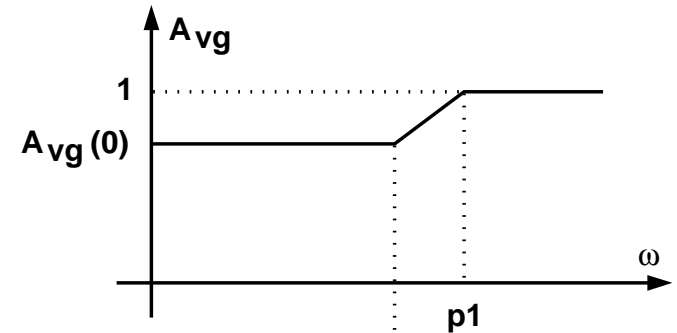
# Source Follower's Gate Voltage Gain

For most practical cases

$$g_{o1} + g_{o2} \ll g_{m1} + g_{mb1} = g_{m1}(1 + \chi)$$

$$|p1| > |z1|$$

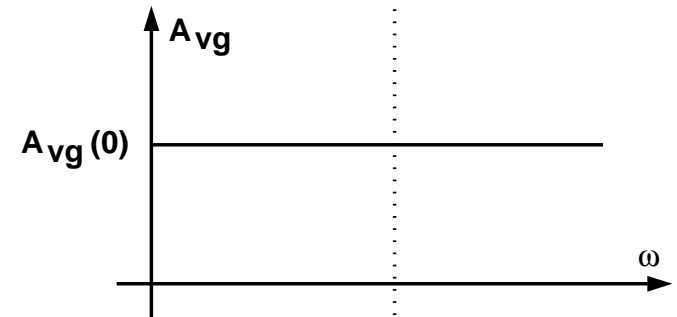
$$(C'_L = 0)$$



$$A_{vg}(0) \approx \frac{g_{m1}}{g_{m1} + g_{mb1}}$$

$$\approx \frac{1}{1 + \chi_1}$$

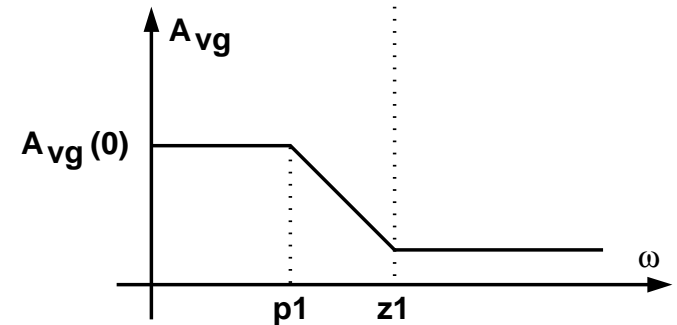
$$|p1| = |z1|$$



$$p_1 \approx -\frac{g_{m1}(1 + \chi_1)}{C_{gs1} + C'_L}$$

$$\approx (1 + \chi_1) \left( \frac{1}{1 + \frac{C'_L}{C_{gs1}}} \right) z_1$$

$$|p1| < |z1|$$



# Source Follower's Gate Input Impedance

The input admittance looking into the gate is

$$Y_g(s) = \frac{i_g}{V_g} = sC_{gs1}[1 - A_{vg}(s)] = \frac{sC_{gs1}(G'_L + sC'_L)}{g_{m1} + G'_L + s(C_{gs1} + C'_L)}$$

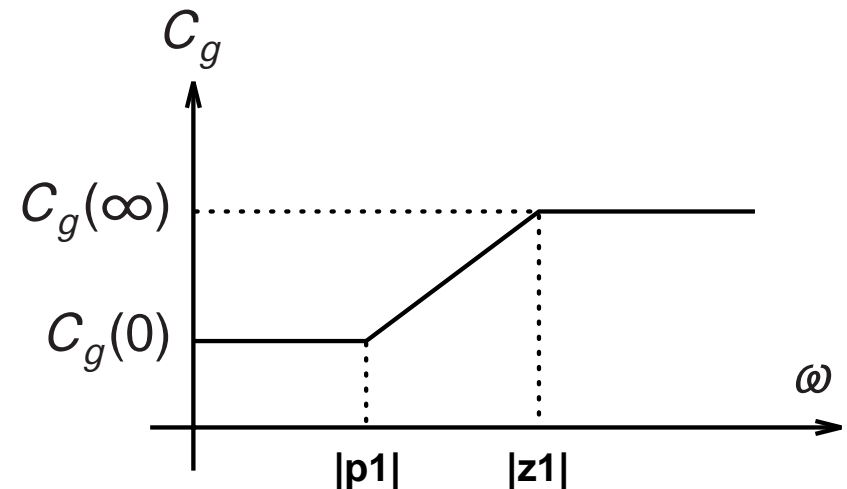
Define the capacitance looking into the gate as

$$Y_g(s) = sC_g(s)$$

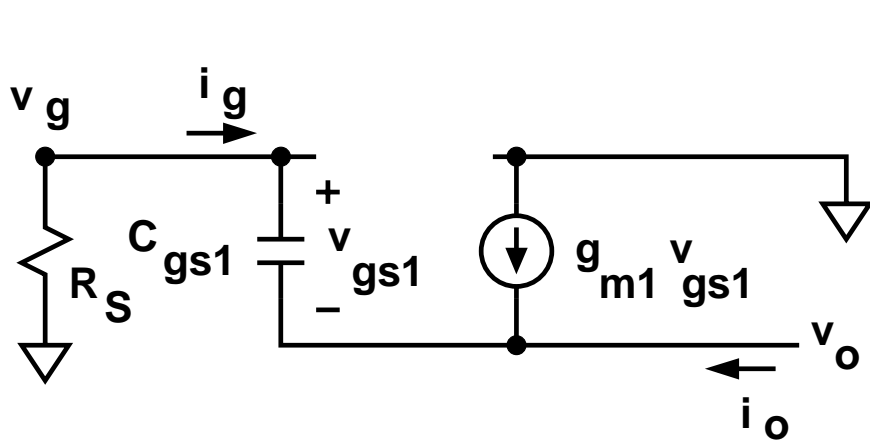
$$C_g(j\omega) = C_{gs1}[1 - A_{vg}(j\omega)]$$

$$C_g(0) = C_{gs1}[1 - A_{vg}(0)]$$

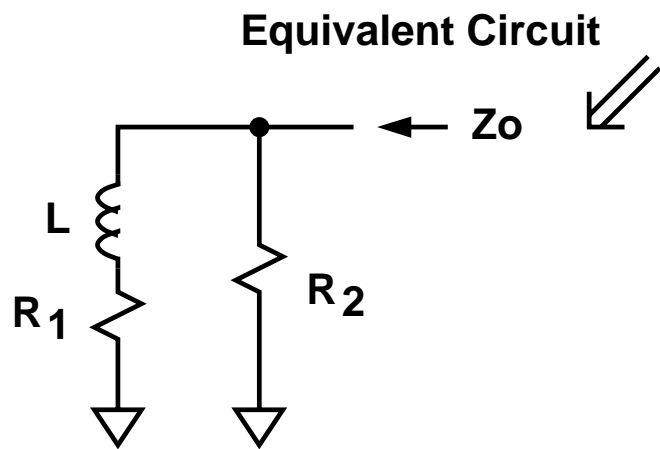
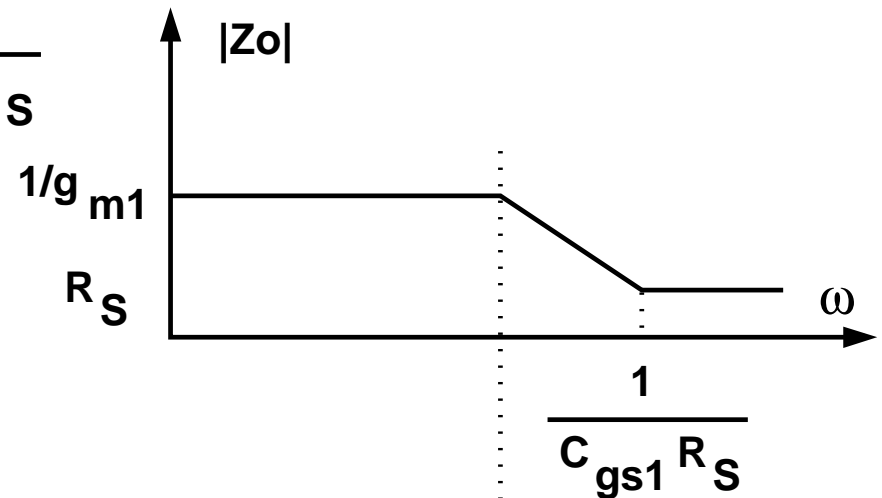
$$C_g(\infty) = C_{gs1}[1 - A_{vg}(\infty)] = \frac{C_{gs1}C'_L}{C_{gs1} + C'_L}$$



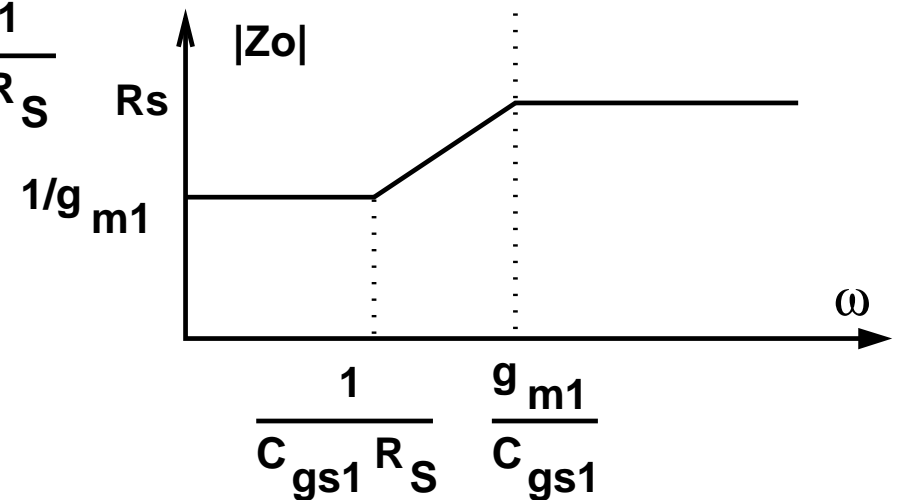
# Source Follower's Output Impedance



$$g_{m1} < \frac{1}{R_S}$$



$$g_{m1} > \frac{1}{R_S}$$



$$i_o = -(g_{m1} + sC_{gs1})(v_g - v_o)$$

$$G_S v_g + sC_{gs1}(v_g - v_o) = 0$$

# Source Follower's Output Impedance

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The output admittance is

$$Y_o(s) = \frac{1}{Z_o(s)} \equiv \frac{i_o}{v_o} = \frac{G_S(g_{m1} + sC_{gs1})}{G_S + sC_{gs1}} = G_S + \frac{G_S(g_{m1} - G_S)}{G_S + sC_{gs1}} = G_S + \frac{1}{\frac{1}{g_{m1} - G_S} + \frac{sC_{gs1}R_S}{g_{m1} - G_S}}$$

- Note that

$$Z_o(0) = \frac{1}{g_{m1}} \quad Z_o(\infty) = R_S$$

- The equivalent circuit is

$$R_1 = \frac{1}{g_{m1} - G_S} \quad R_2 = R_S \quad L = \frac{R_S C_{gs1}}{g_{m1} - G_S}$$

# Source Follower's Complete Frequency Response

$$A(s) = \frac{v_o}{i_{in}} = \frac{A_{vg}(s)}{G_S + sC'_S + Y_g} = \frac{g_{m1} + sC_{gs1}}{b_0 + b_1s + b_2s^2} = A(0) \frac{1 - s/z_1}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o^2}}$$

where

$$A(0) = R_S \cdot \frac{g_{m1}}{g_{m1} + G'_L} = R_S \cdot \frac{g_{m1}R'_L}{1 + g_{m1}R'_L} \quad z_1 = -\frac{g_{m1}}{C_{gs1}} \simeq -\omega_T$$

$$b_0 = G_S(g_{m1} + G'_L)$$

$$b_1 = G_S(C_{gs1} + C'_L) + (g_{m1} + G'_L)C'_S + G'_L C_{gs1}$$

$$b_2 = C_{gs1}C'_L + C'_S(C_{gs1} + C'_L)$$

and

$$\omega_o = \sqrt{\frac{G_S(g_{m1} + G'_L)}{C_{gs1}C'_L + C'_S(C_{gs1} + C'_L)}}$$

$$Q = \frac{\sqrt{G_S(g_{m1} + G'_L)[C_{gs1}C'_L + C'_S(C_{gs1} + C'_L)]}}{G_S C'_L + (g_{m1} + G'_L)C'_S + G'_L C_{gs1}}$$

# Source Follower's Complete Frequency Response

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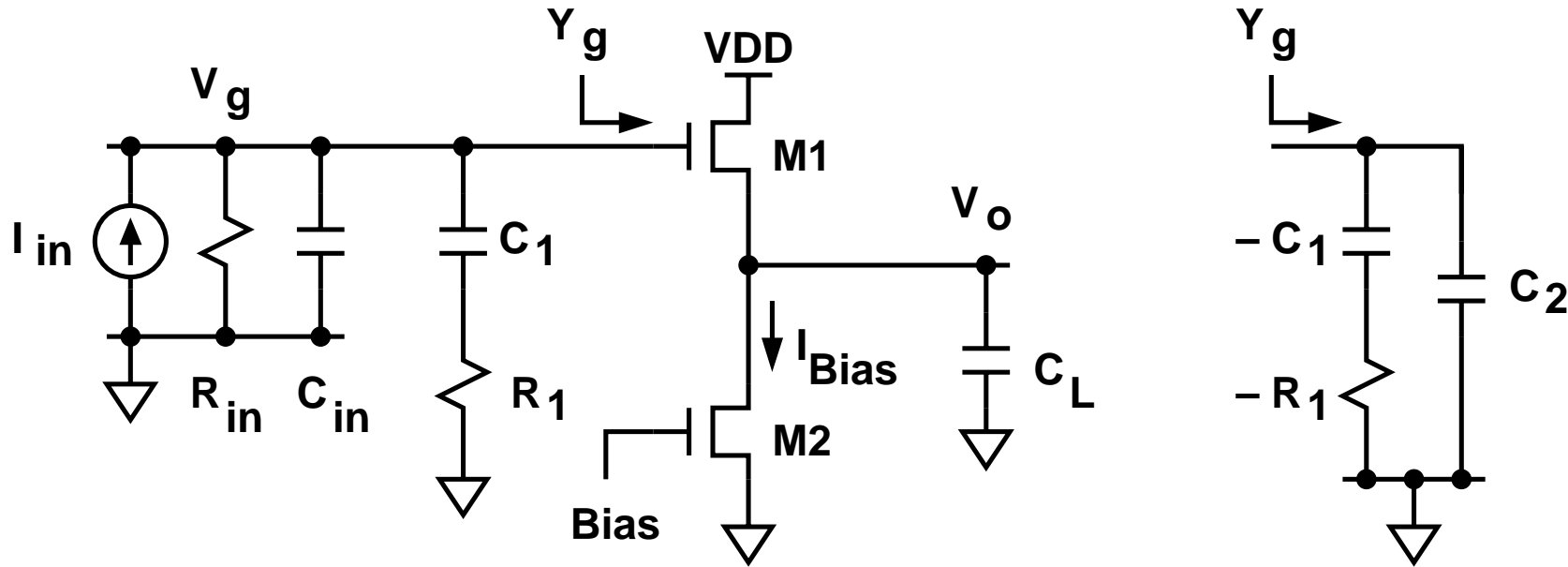
- $\omega_o$  is the *pole frequency* and  $Q$  is the *Q-factor*.
- The bandwidth can be estimated by

$$BW \approx \omega_o \approx \sqrt{\frac{1}{R_S(C'_S + C_{gs1})} \times \frac{g_{m1} + G'_L}{C'_L}} \quad \text{if } C'_L \gg C'_S$$

- If  $Q < 1/\sqrt{2} \approx 0.707$ , no peaking in  $|A(j\omega)|$ .
- If  $Q > 0.5$ , the poles are complex, and overshoot appears in the step response.  
 $\% \text{ Overshoot} = 100e^{-\pi/\sqrt{4Q^2-1}}$
- If  $g_{m1} \gg G'_L$  and  $C'_L \gg C'_S$

$$\frac{1}{Q} \approx \sqrt{\frac{G_S C'_L}{g_{m1}(C_{gs1} + C'_S)}} + \sqrt{\frac{g_{m1} C'_S}{G_S C'_L (C_{gs1}/C'_S + 1)}} + \sqrt{\frac{G'_L C_{gs1}}{G_S (g_{m1}/G'_L)(1 + C'_S/C_{gs1})}}$$

# Compensated Source Follower



$$Y_g = \frac{1}{-R_1 - \frac{1}{sC_1}} + sC_2$$

$$R_1 = \frac{(C_{gs1} + C'_L)^2}{C_{gs1}(g_{m1}C'_L - G'_L C_{gs1})} \approx \frac{(C_{gs1} + C'_L)^2}{g_{m1}C_{gs1}C'_L}$$

$$C_1 = \frac{C_{gs1}(g_{m1}C'_L - G'_L C_{gs1})}{(g_{m1} + G'_L)(C_{gs1} + C'_L)} \approx \frac{g_{m1}C_{gs1}C'_L}{(g_{m1} + G'_L)(C_{gs1} + C'_L)}$$

$$C_2 = \frac{C_{gs1}C'_L}{C_{gs1} + C'_L}$$

# Compensated Source Follower

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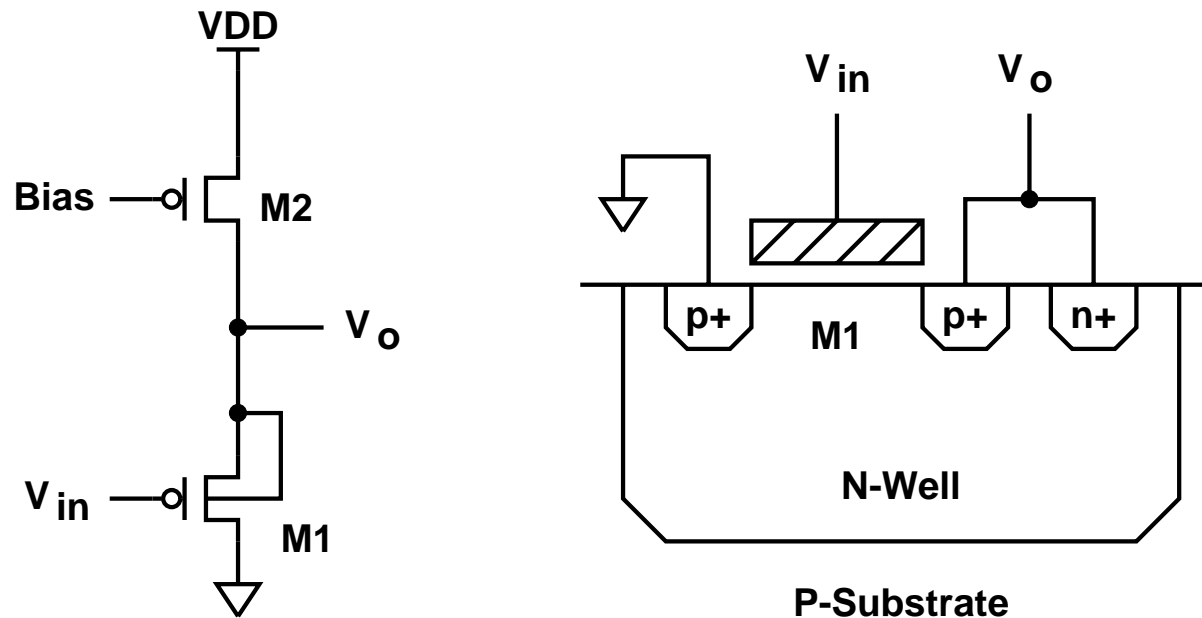
- Adding  $R_1$  and  $C_1$  to the input port can eliminate the complex poles.
- For the compensated source follower, we have

$$A(s) = [G_S + s(C'_S + C_2)] \cdot A_{vg} = R_S \frac{g_{m1} R'_L}{1 + g_{m1} R'_L} \times \frac{1 + s \frac{C_{gs1}}{g_{m1}}}{(1 - s/p_1)(1 - s/p_2)}$$

where

$$p_1 = -\frac{G_S}{C'_S + \frac{C_{gs1} C'_L}{C_{gs1} + C'_L}} \approx -\frac{G_S}{C'_S + C_{gs1}} \quad \text{if } C'_L \gg C_{gs1}$$
$$p_2 = -\frac{g_{m1} + G'_L}{C_{gs1} + C'_L} \approx -\frac{g_{m1} + G'_L}{C'_L} \quad \text{if } C'_L \gg C_{gs1}$$

# Floating-Well Source Follower



The follower is in an isolated well tied to the M1 source. Thus,  $V_{SB}(M1) = 0$ , and

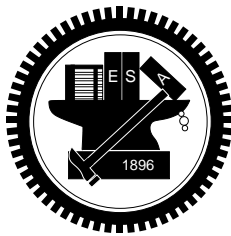
$$A_{vg}(0) = \frac{g_{m1}}{g_{m1} + g_{o1} + g_{o2}}$$

- The junction capacitance at the M1's source is now replaced by the well-substrate junction capacitor.
- $p+$  guard-ring surrounding the n-well may be required.

# Multiple-Transistor Gain Stages

Jieh-Tsorng Wu

October 24, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Dominant-Pole Approximation

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The response of an amplifier has the form of

$$A(s) = A(0) \frac{N(s)}{D(s)} = A(0) \frac{1 + a_1 s + a_2 s^2 + \dots + a_m s^m}{1 + b_1 s + b_2 s^2 + \dots + b_n s^n} \approx \frac{A(0)}{\left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right) \dots \left(1 - \frac{s}{p_n}\right)}$$

If  $|p_1| \ll |p_2|, |p_3|, \dots, |p_n|$ , then  $p_1$  is a dominant pole. We have

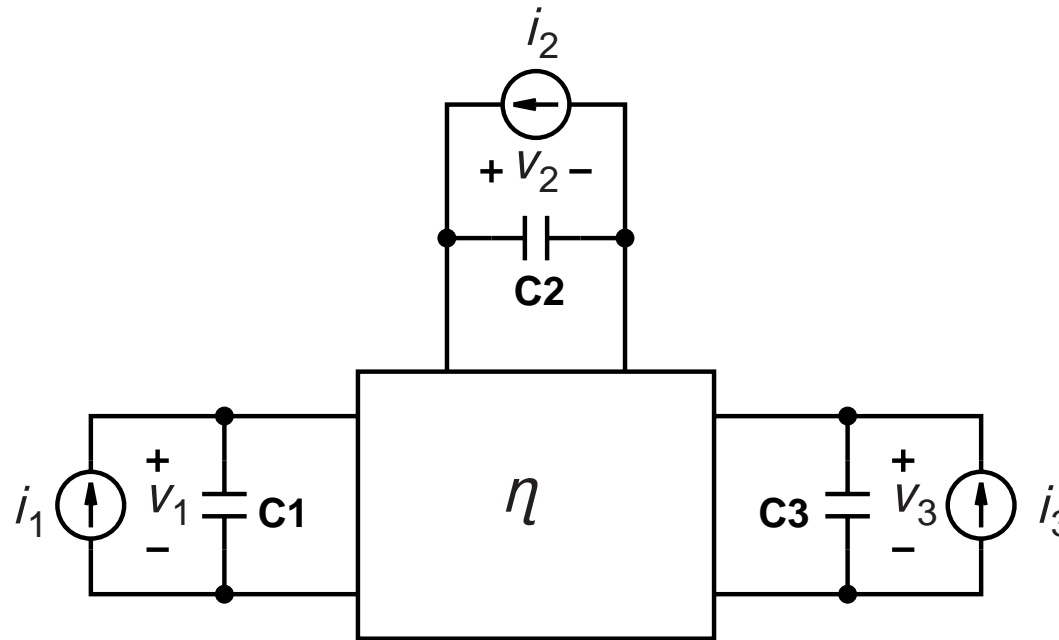
$$b_1 = -\frac{1}{p_1} - \frac{1}{p_2} - \dots - \frac{1}{p_n} \approx -\frac{1}{p_1} = \left| \frac{1}{p_1} \right|$$

$$|A(j\omega)| = \frac{A(0)}{\sqrt{\left[1 + \left(\frac{\omega}{p_1}\right)^2\right] \left[1 + \left(\frac{\omega}{p_2}\right)^2\right] \dots \left[1 + \left(\frac{\omega}{p_n}\right)^2\right]}} \approx \frac{A(0)}{\sqrt{1 + \left(\frac{\omega}{p_1}\right)^2}}$$

$$\text{-3 dB Bandwidth} = \omega_{-3\text{dB}} \approx |p_1| \approx \frac{1}{b_1}$$

# Zero-Value Time Constants

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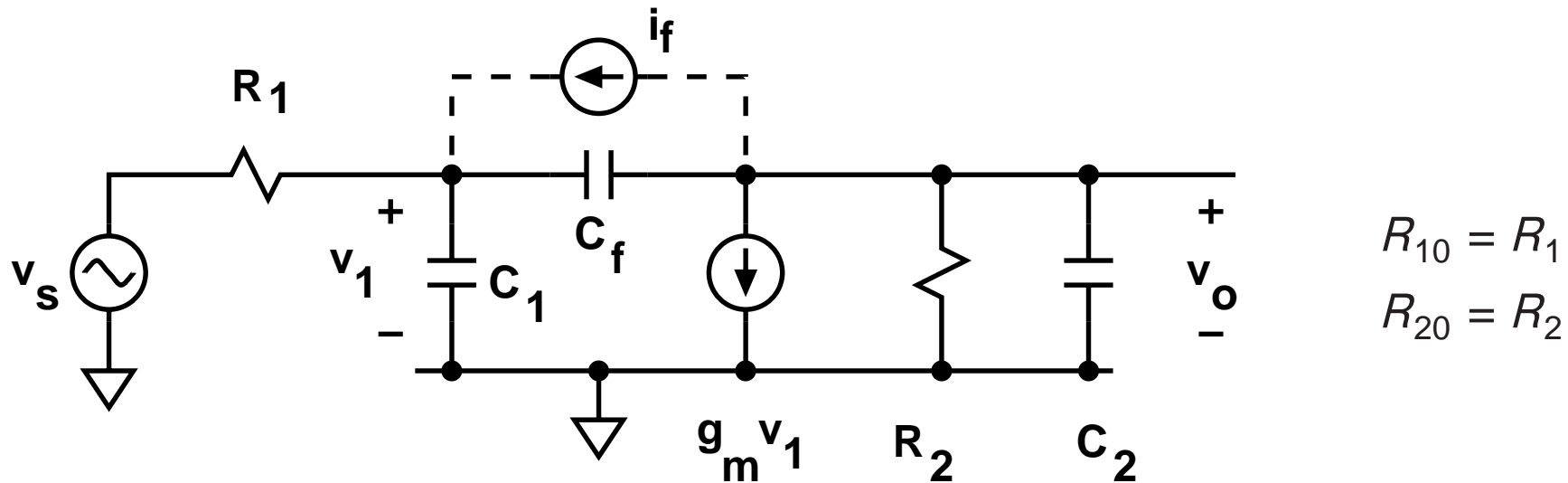


- $\eta$  is a linear active network without energy storage.
- The  $b_1$  in the denominator of the system function can be expressed as

$$b_1 = \sum T_0 = R_{10}C_1 + R_{20}C_2 + R_{30}C_3 + \dots$$

$R_{i0}$  is the driving point resistance seen by  $C_i$  with all capacitors equal to zero.

## Zero-Value Time Constant Example



To determine  $R_{f0}$ , replace  $C_f$  with a current source  $i_f$ , then

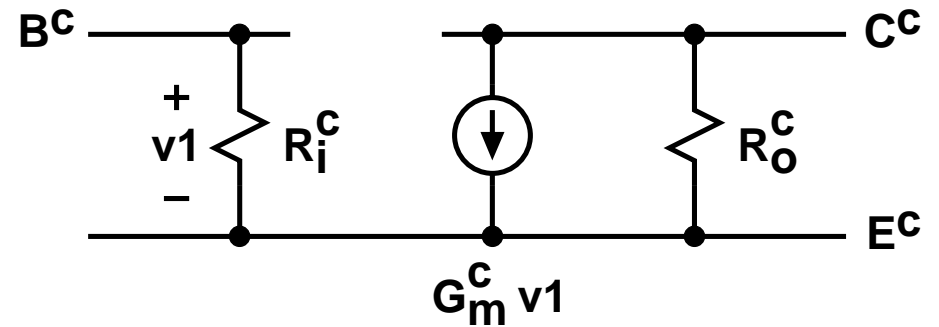
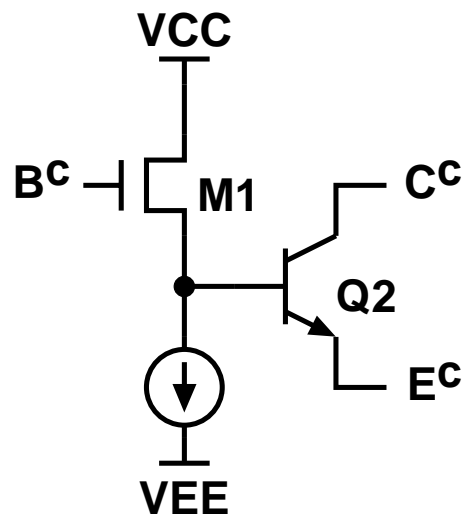
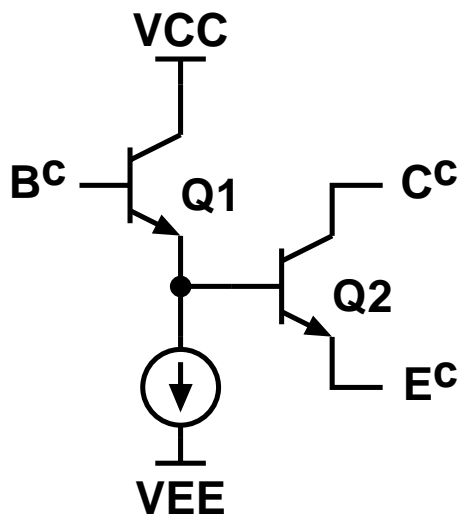
$$v_1 = i_f R_1 \quad v_o = -(i_f + g_m v_1) R_2$$

$$R_{f0} = \frac{v_1 - v_o}{i_f} = R_1 + R_2 + g_m R_1 R_2 = R_1 \left( 1 + g_m R_2 + \frac{R_2}{R_1} \right)$$

We have

$$b_1 = \sum T_0 = R_1 C_1 + R_2 C_2 + (R_1 + R_2 + g_m R_1 R_2) C_f$$

# Darlington Configuration



For the BJT-BJT Darlington configuration,

$$\beta^c = \beta_{o2}(\beta_{o1} + 1)$$

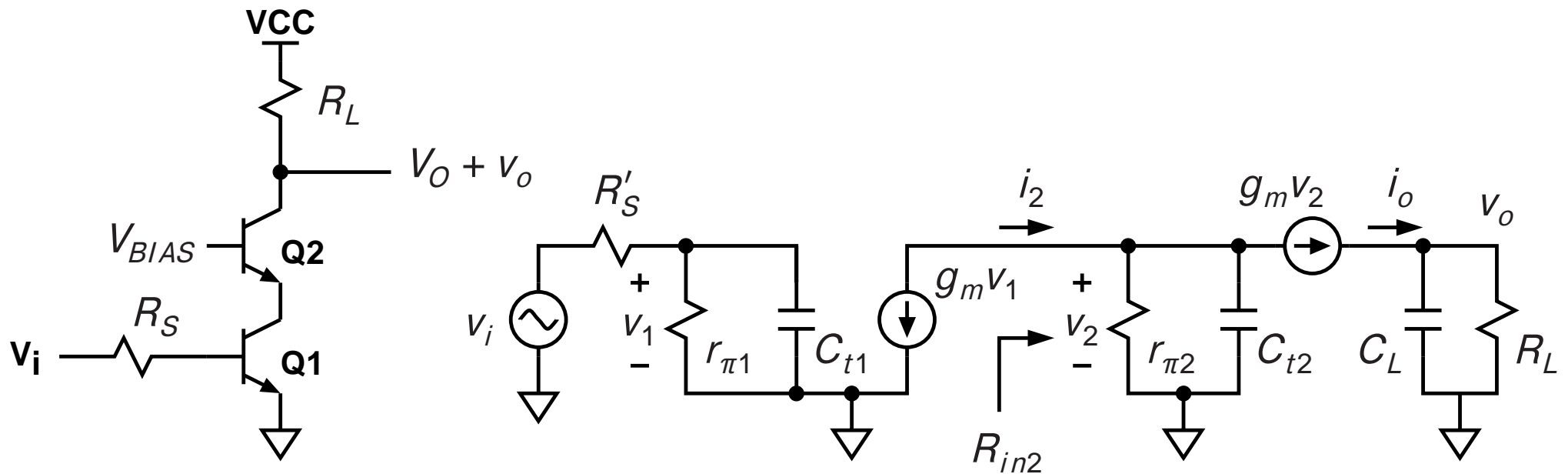
$$R_i^c = r_{\pi1} + (\beta_{o1} + 1)r_{\pi2}$$

$$G_m^c = \frac{g_{m2}}{1 + \frac{r_{\pi1}}{(\beta_{o1} + 1)r_{\pi2}}}$$

$$R_o^c = r_{o2}$$

- Use to boost the effective current gain of BJTs.
- No significant application in pure-MOS circuits.

# BJT Cascode Configuration



$$C_L = C_{\mu 2} + C_{cs2} + \text{Capacitive Load} \quad C_{t2} = C_{\pi 2} + C_{cs1}$$

$$C_{t1} = C_{\pi 1} + C_{\mu 1}(1 + g_{m1}R_{in2}) \quad R_{in2} = \frac{r_{\pi 2} + r_{b2}}{\beta_{o2} + 1} = \frac{\alpha_{o2}}{g_{m2}} + \frac{r_{b2}}{\beta_{o2} + 1} \approx \frac{1}{g_{m2}}$$

- Usually  $I_{C2} \approx I_{C1}$ , then  $g_{m2} \approx g_{m1}$  and  $C_{t1} \approx C_{\pi 1} + 2C_{\mu 1}$ .
- If  $R_L$  is large compared to  $r_{o2}$ , then  $R_{in2} \approx (1/g_{m2})(1 + R_L/r_{o2})$ .

# BJT Cascode Characteristics

We can express voltage gain  $A_v(s)$  as

$$A_v(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_1}{V_i} \frac{i_2}{V_1} \frac{i_o}{i_2} \frac{V_o}{i_o} = \left( \frac{r_{\pi 1}}{R'_S + r_{\pi 1}} \frac{1}{1 - \frac{s}{p_1}} \right) \times (-g_{m1}) \times \left( \frac{\alpha_{o2}}{1 - \frac{s}{p_2}} \right) \times \left( \frac{R_L}{1 - \frac{s}{p_3}} \right)$$

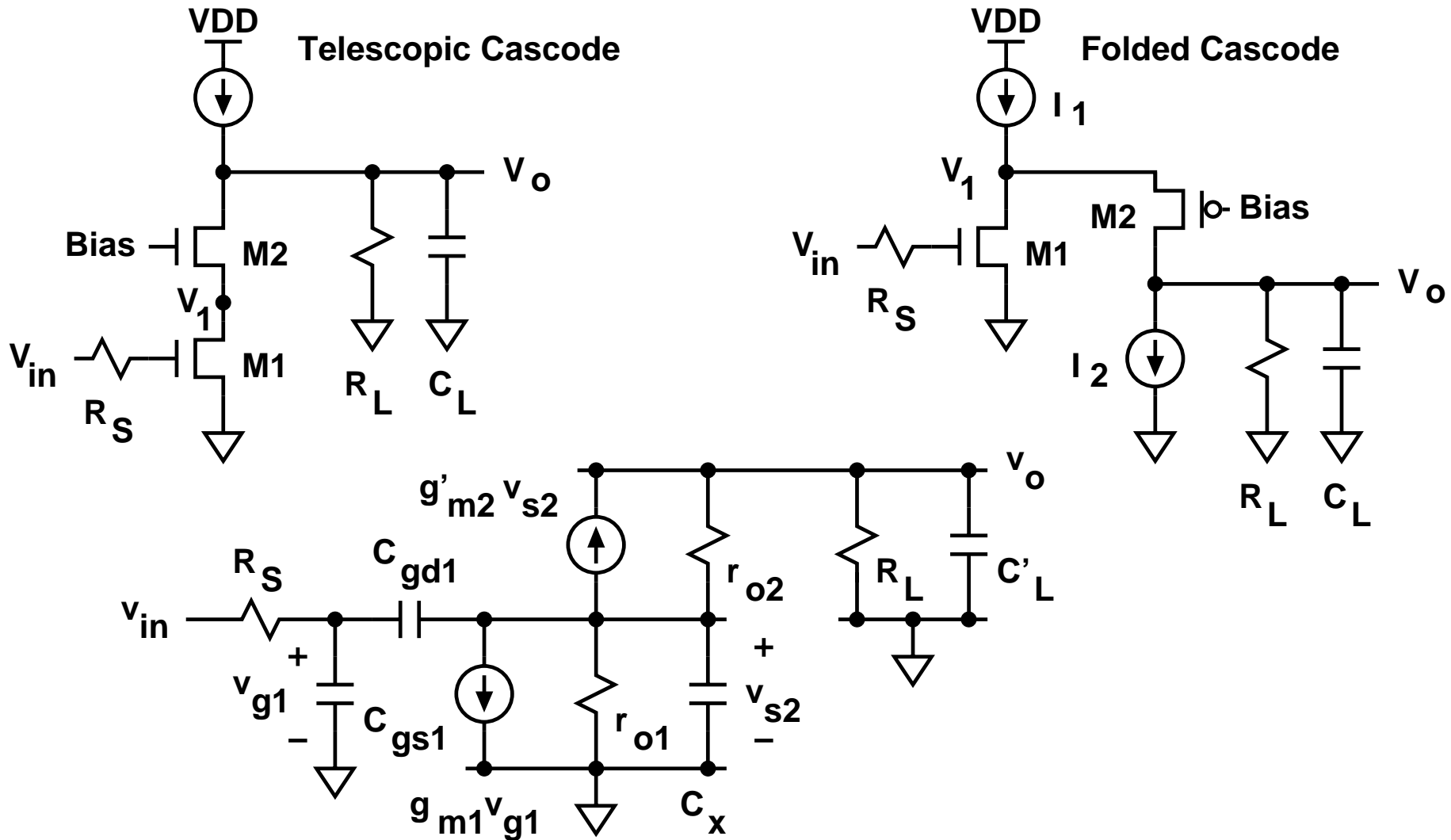
$$\Rightarrow A_v(s) = \frac{A_v(0)}{(1 - s/p_1)(1 - s/p_2)(1 - s/p_3)}$$

$$A_v(0) = -\alpha_{o2} g_{m1} R_L \frac{r_{\pi 1}}{R'_S + r_{\pi 1}} \quad p_1 = -\frac{1}{(R'_S \parallel r_{\pi 1}) C_{t1}} \quad p_2 = -\frac{1}{\alpha_{o2} C_{t2}} \quad p_3 = -\frac{1}{R_L C_L}$$

The output resistance of the cascode stage is

$$R_{out} = r_{o2} \cdot \frac{1 + g_{m2} r_{o1} \left( 1 + \frac{1}{\beta_{o2}} + \frac{1}{g_{m2} r_{o2}} \right)}{1 + \frac{g_{m2} r_{o1}}{\beta_{o2}}} = r_{o2} \left( 1 + \frac{1 + g_{m2} r_{o1}}{1 + \frac{g_{m2} r_{o1}}{\beta_{o2}}} \right) \approx \beta_{o2} r_{o2}$$

# MOST Cascode Configuration



$$g'_{m2} = g_{m2} + g_{mb2}$$

$$C_x = C_{db1} + C'_{sb2} + C_{gs2}$$

$$C'_L = C_L + C_{db2} + C_{gd2}$$

# MOST Cascode Low-Frequency Characteristics

---

The output impedance looking into M2's drain is

$$R_{ot2} = r_{o1} + (g'_{m2}r_{o1} + 1)r_{o2} \approx g'_{m2}r_{o1}r_{o2}$$

The input admittance looking into M2's source is

$$G_{in2} \approx \frac{g'_{m2}}{g_{o2}/G_L + 1}$$

The overall voltage gain is

$$A_v = \frac{V_o}{V_{in}} \approx -\frac{g_{m1}}{g_{o1} + G_{in2}} \times \frac{g'_{m2}}{g_{o2} + G_L} = g_{m1} \times \frac{g'_{m2}r_{o1}r_{o2}R_L}{r_{o2} + g'_{m2}r_{o1}r_{o2} + R_L} \approx g_{m1} \times (R_{ot2} \parallel R_L)$$

- Let  $g_m = g_{m1} = g'_{m2}$ ,  $r_o = r_{o1} = r_{o2}$ , and  $g_m \gg g_o$ . If  $R_L = R_{ot2} = g_m r_o^2$ , then

$$G_{in2} \approx \frac{g_m}{g_o R_L + 1} \approx \frac{g_m}{g_m r_o + 1} \approx g_o \quad A_v \approx -\frac{g_m}{2g_o} \frac{g_m}{g_o + G_L} \approx -\frac{1}{2} \left( \frac{g_m}{g_o} \right)^2$$

# MOST Cascode Zero-Value Time Constant Analysis

---

Using the zero-value time constant method, we have

$$R_{gs10} = R_S \quad R_{gd10} = R_S + R_{x0} + g_{m1}R_S R_{x0}$$

$$R_{x0} = r_{o1} \parallel R_{in2} \approx r_{o1} \parallel [(1/g'_{m2})(g_{o2}/G_L + 1)] \quad R_{L0} = R_L \parallel R_{ot2} \approx R_L \parallel (g'_{m2}r_{o1}r_{o2})$$

$$\sum T_0 = R_{gs10}C_{gs1} + R_{gd10}C_{gd1} + R_{x0}C_x + R_{L0}C_L \quad \omega_{-3dB} = 1 / \left( \sum T_0 \right)$$

- Let  $g_m = g_{m1} = g'_{m2}$ ,  $r_o = r_{o1} = r_{o2}$ ,  $g_m \gg g_o$ . If  $R_L = R_{ot2} = g_m r_o^2$  and  $R_S = r_o$ , then

$$R_{in2} \approx r_o \quad R_{x0} = \frac{r_o}{2} \quad R_{L0} \approx \frac{g_m r_o^2}{2} \quad R_{gd10} \approx R_S + \frac{r_o}{2} + \frac{g_m r_o R_S}{2} \approx \frac{g_m r_o^2}{2}$$

$$\Rightarrow \sum T_0 = R_S C_{gs1} + \frac{g_m r_o^2}{2} C_{gd1} + \frac{r_o}{2} C_x + \frac{g_m r_o^2}{2} C_L$$

- $R_{L0}C_L$  usually is the dominant term, unless  $R_S$  is very large.

# MOST Cascode AC Characteristics

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Let  $R_L = R_{ot2} = g'_{m2}r_{o1}r_{o2}$ , then

$$G_{in2} \approx \frac{g'_{m2}}{g_{o2}R_L + 1} \approx \frac{g'_{m2}}{g'_{m2}r_{o1} + 1} \approx g_{o1}$$

The dc gain is

$$A_V(0) \approx -\frac{g_{m1}}{g_{o1} + G_{in2}} \times \frac{g'_{m2}}{g_{o2} + G_L} \approx -\frac{1}{2} \cdot \frac{g_{m1}}{g_{o1}} \cdot \frac{g'_{m2}}{g_{o2}}$$

The dominant pole is

$$p_1 = -\frac{1}{R_{L0}C_L} \approx -\frac{2}{g'_{m2}r_{o1}r_{o2}C_L}$$

At frequencies where  $|p_1| \ll \omega \ll |p_2|$ ,

$$A_V(s) = \frac{A_V(0)}{1 - \frac{s}{p_1}} \approx \frac{A_V(0)}{-\frac{s}{p_1}} \approx -\frac{g_{m1}}{sC_L} = -\frac{\omega_u}{s} \quad \omega_u = A_V(0) \cdot p_1 = \frac{g_{m1}}{C_L}$$

# MOST Cascode AC Characteristics

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The second pole is approximately at

$$p_2 = -\frac{g_{o1} + Y_{in2}}{C_x}$$

$Y_{in2}$  is the resistance looking into the M2's source at high frequencies.

$$Y_{in2} = g'_{m2} - g_{o2} \left( \frac{V_o}{V_{s2}} - 1 \right)$$

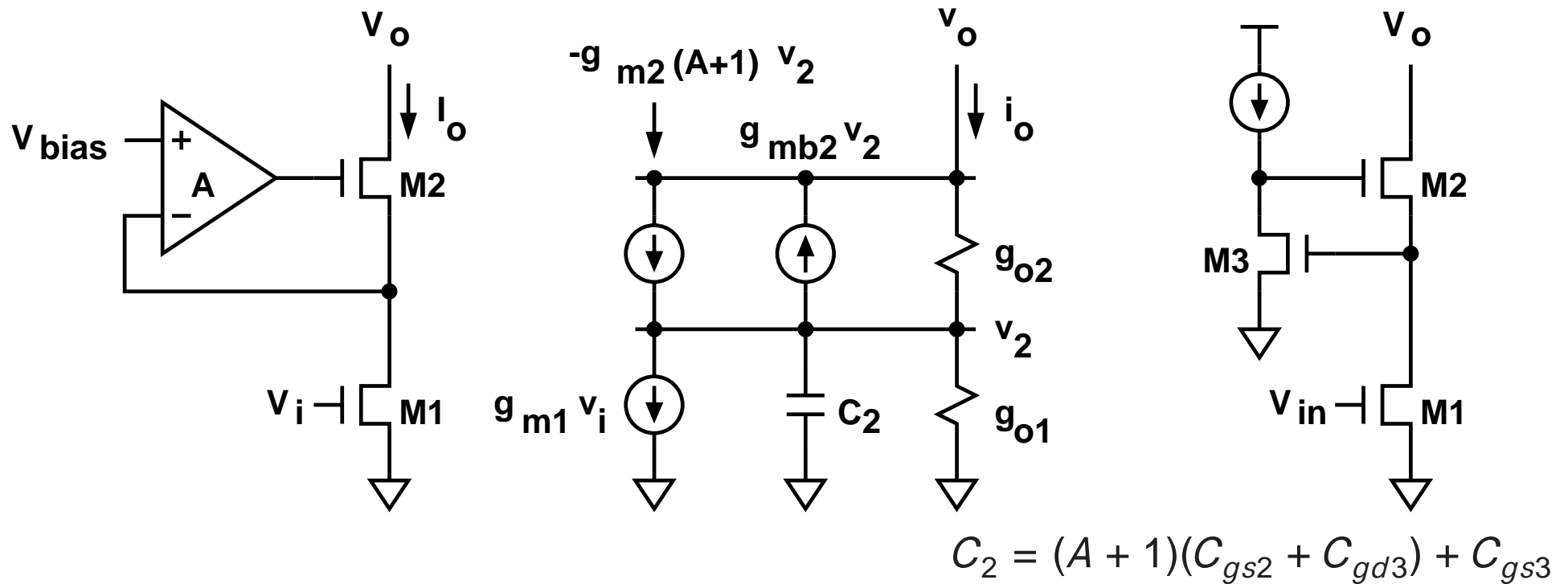
- At frequencies  $\omega \gg (g_{o2} + G_L)/C_L$ ,

$$\frac{V_o}{V_{s2}} = \frac{g'_{m2} + g_{o2}}{g_{o2} + G_L + sC_L} \approx \frac{g'_{m2}}{sC_L} \Rightarrow Y_{in2} \approx g'_{m2} \left( 1 - \frac{g_{o2}}{sC_L} \right) + g_{o2} \approx g'_{m2}$$

$$p_2 \approx -\frac{g'_{m2}}{C_x} \approx -\frac{g_{m2}}{KC_{gs2}} \approx -\frac{\omega_T}{K}$$

where  $K$  is between 1 and 2 (usually closer to 1).

# Active Cascode Configuration



The M2's transconductance is boosted as  $g'_{m2} = g_{m2}(A + 1) + g_{mb2}$ , thus

$$R_{ot2} = r_{o1} + r_{o2} + g'_{m2}r_{o1}r_{o2} \approx [g_{m2}(A + 1) + g_{mb2}]r_{o1}r_{o2}$$

$$G_{in2} \approx \frac{g_{m2}(A + 1) + g_{mb2}}{g_{o2}/G_L + 1} \quad G_{in2} = g_{m2}(A + 1) + g_{mb2} + g_{o2} \quad \text{if } R_L = 0$$

# Active Cascode Characteristics

---

The equivalent transconductance is

$$G_m = \left. \frac{i_o}{V_i} \right|_{v_o=0} = g_{m1} \times \frac{G_{in2}}{g_{o1} + G_{in2}} = g_{m1} \left( 1 - \frac{1}{1 + [g_{m2}(A + 1) + g_{mb2}]r_{o1} + r_{o1}/r_{o2}} \right)$$

- If  $A(s)$  has a dominant pole, i.e,  $A(s) = a_o/(1 - s/p_1) \approx -\omega_u/s$ ,  $\omega_u = a_o \cdot |p_1|$ . The transfer function  $V_o/V_i$  has an additional zero and pole at

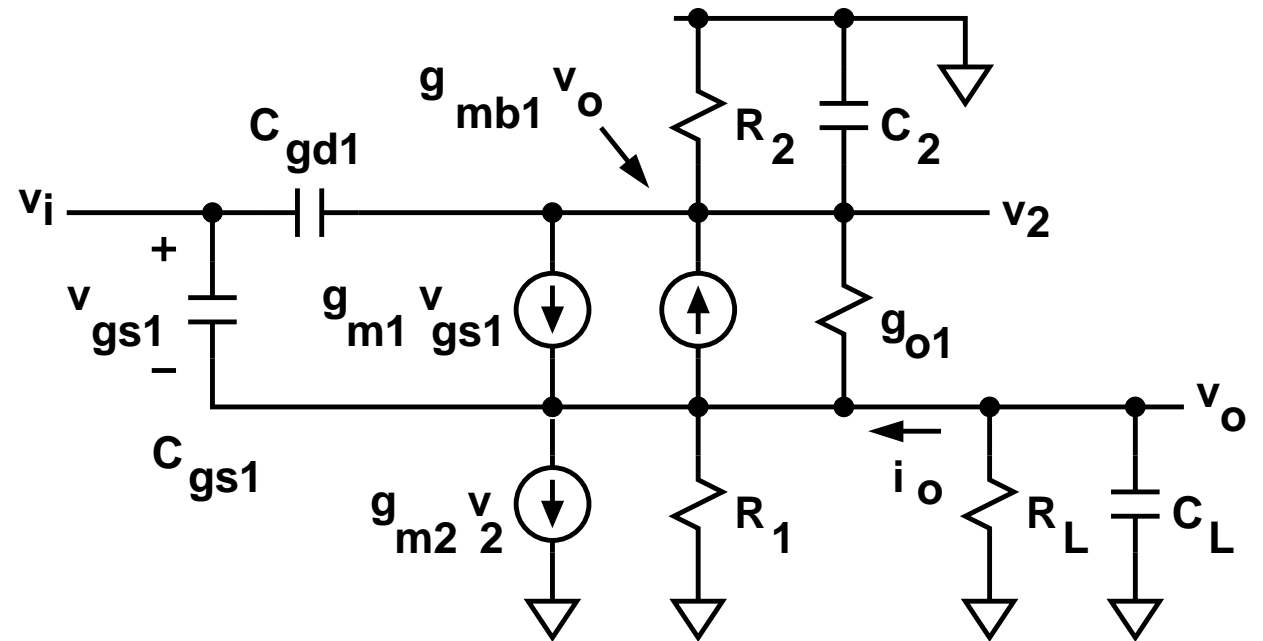
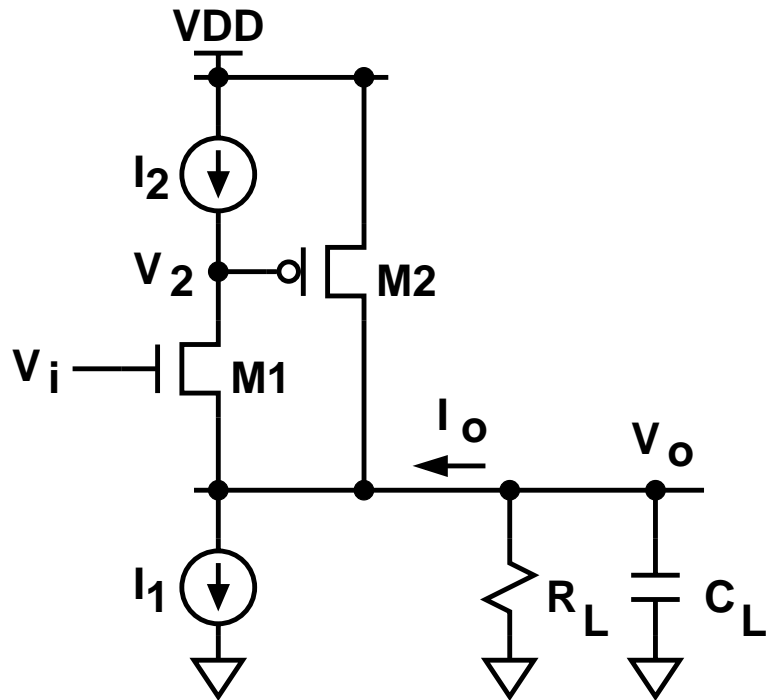
$$z' = -\omega_u \quad p' = -\omega_u - \frac{1}{g_{m2}r_{o1}r_{o2}C_L} \approx -\omega_u \quad C_L = \text{Capacitor at } V_o$$

- The non-dominant pole at the M2's source is

$$p_2 \approx \frac{g'_{m2}}{C_2} = \frac{g_{m2}(A + 1) + g_{mb2}}{(A + 1)(C_{gs2} + C_{gd3}) + C_{gs3}} \approx \frac{g_{m2}}{C_{gs2} + C_{gd3}}$$

$p_2$  is degraded slightly by the addition of amplifier  $A$ .

# Super Source Follower Configuration



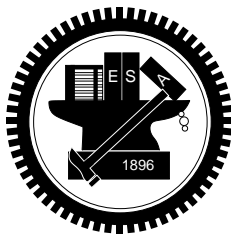
$$R_o = \left. \frac{V_o}{i_o} \right|_{v_i=0} = R_1 \parallel \left( \frac{r_{o1} + R_2}{[1 + (g_{m1} + g_{mb1})r_{o1}](1 + g_{m2}R_2)} \right) \approx \frac{1}{g_{m1} + g_{mb1}} \left( \frac{1}{g_{m2}r_{o1}} \right)$$

$$A_V(0) = \left. \frac{V_o}{V_i} \right|_{i_o=0} = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{R_2+r_{o1}}{R_1(1+g_{m2}R_2)}} \approx \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{1}{g_{m2}r_{o2}}}$$

# Differential Gain Stages

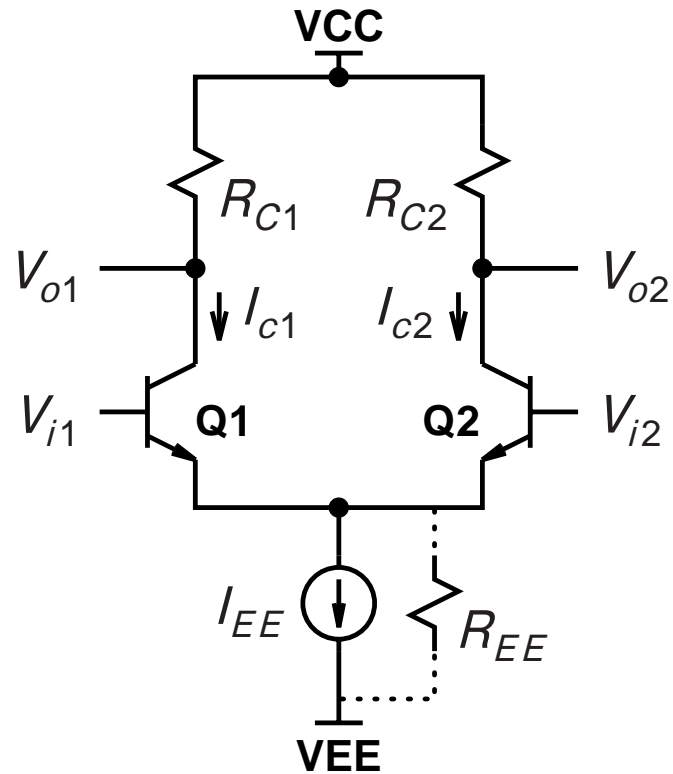
Jieh-Tsorng Wu

July 16, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Emitter-Coupled Pair



Assume

- $Q1=Q2$ .
- $R_{C1} = R_{C2} \equiv R_C$ .
- Q1 and Q2 don't saturate.
- Neglect  $r_b$ ,  $r_o$ , and  $r_\mu$ .
- Neglect  $R_{EE}$ , i.e,  $R_{EE} \rightarrow \infty$ .

$$V_{id} \equiv V_{i1} - V_{i2} \quad I_{cd} \equiv I_{c1} - I_{c2}$$

$$V_{o1} = V_{CC} - I_{c1}R_C \quad V_{o2} = V_{CC} - I_{c2}R_C \quad V_{od} = V_{o1} - V_{o2} = -(I_{c1} - I_{c2})R_C = -I_{cd}R_C$$

$$I_{c1} \approx I_{S1}e^{V_{BE1}/U_T} \quad I_{c2} \approx I_{S2}e^{V_{BE2}/U_T} \quad I_{S1} = I_{S2} \quad \Rightarrow \quad \frac{I_{c1}}{I_{c2}} = e^{(V_{BE1}-V_{BE2})/U_T} = e^{V_{id}/U_T}$$

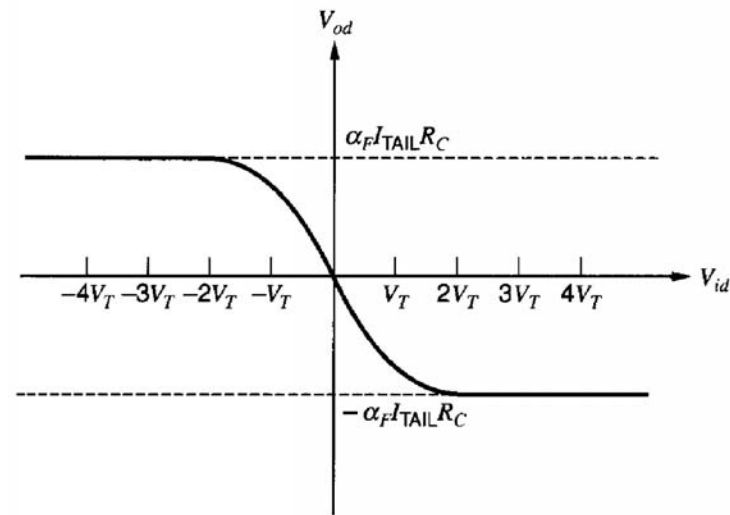
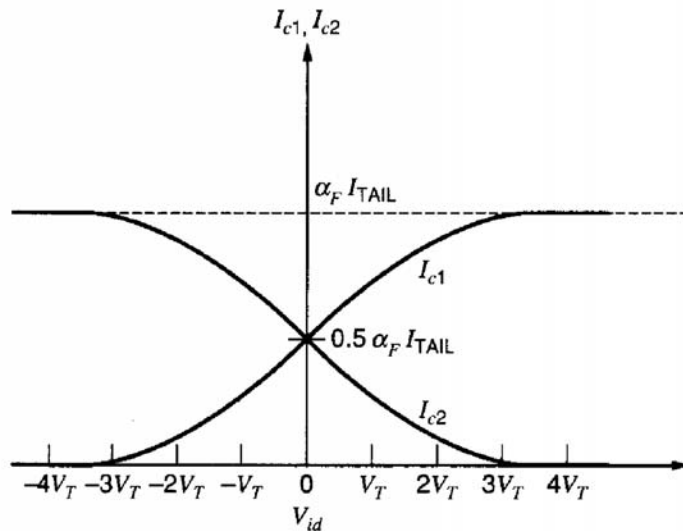
# Emitter-Coupled Pair Large-Signal Behavior

Summing currents at the common emitter node with  $\alpha_{F1} = \alpha_{F2} \equiv \alpha_F$

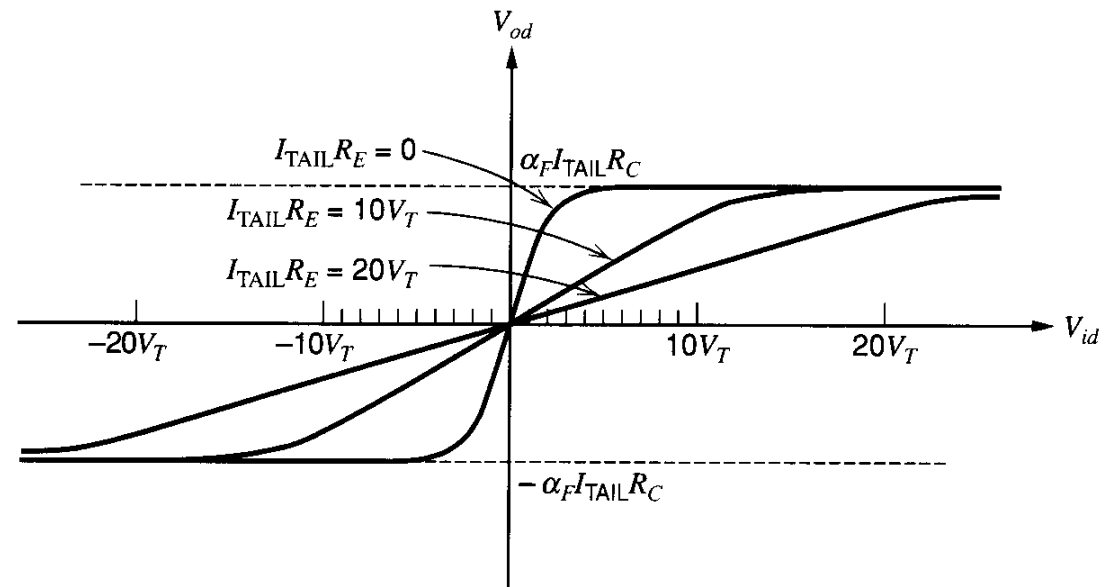
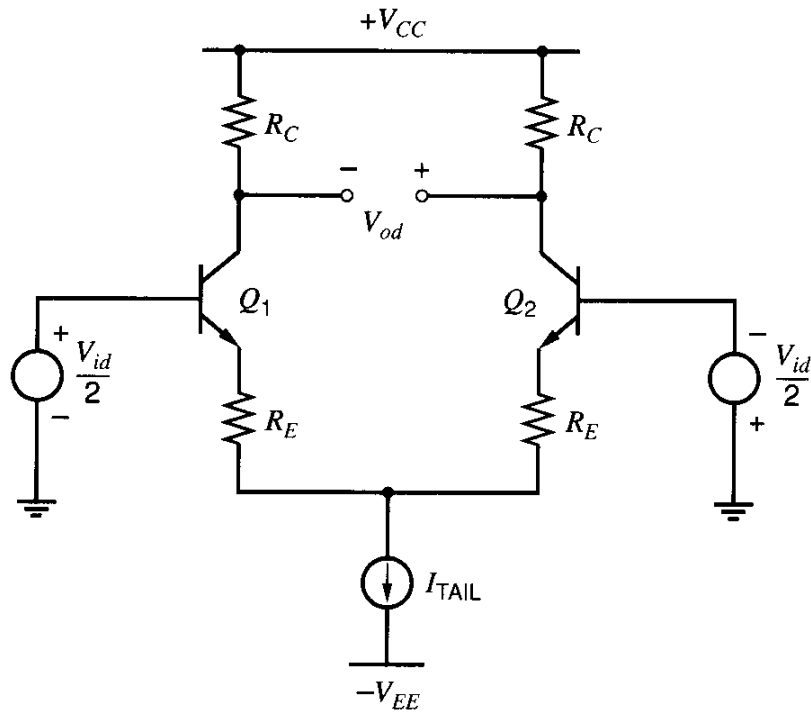
$$\alpha_F I_{EE} = I_{c1} + I_{c2} = I_{c1} \left( 1 + e^{-V_{id}/U_T} \right) \Rightarrow I_{c1} = \frac{\alpha_F I_{EE}}{1 + e^{-V_{id}/U_T}} \quad I_{c2} = \frac{\alpha_F I_{EE}}{1 + e^{+V_{id}/U_T}}$$

$$I_{cd} = I_{c1} - I_{c2} = \alpha_F I_{EE} \left( \frac{1}{1 + e^{-V_{id}/U_T}} - \frac{1}{1 + e^{+V_{id}/U_T}} \right) = \alpha_F I_{EE} \tanh \left( \frac{V_{id}}{2U_T} \right)$$

$$V_{od} = V_{o1} - V_{o2} = -I_{cd} R_C = -\alpha_F I_{EE} R_C \tanh \left( \frac{V_{id}}{2U_T} \right) = \alpha_F I_{EE} R_C \tanh \left( \frac{-V_{id}}{2U_T} \right)$$

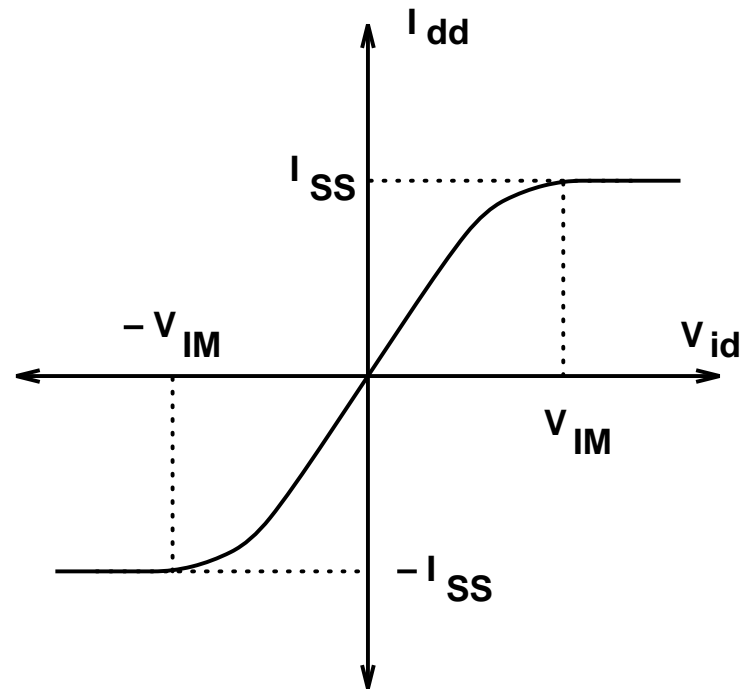
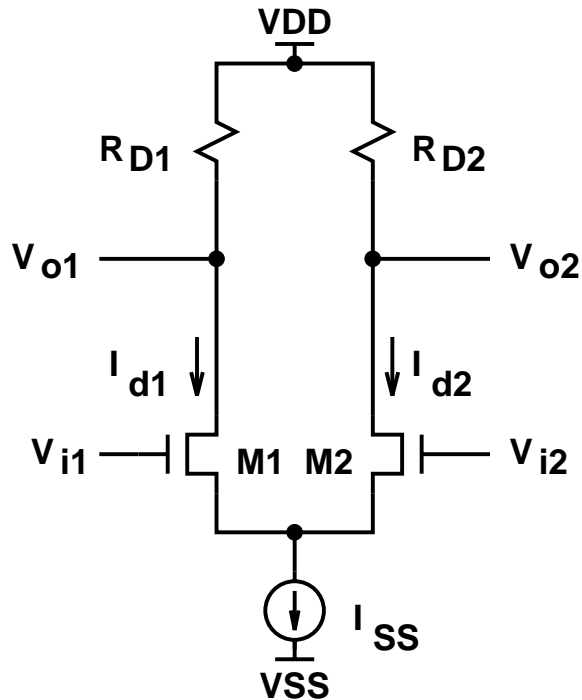


# Emitter-Coupled Pair with Emitter Degeneration



- Series feedback used to exchange gain for linearity.
- Linear input range increased by approximately same factor gain is reduced.
- Doesn't increase linear output range.

# Source-Coupled Pair



Assume

- $M1 = M2$ .
- $R_{D1} = R_{D2} \equiv R_D$ .
- Neglect  $r_o$ .
- $R_{SS} \rightarrow \infty$ .

$$V_{id} \equiv V_{i1} - V_{i2} \quad I_{dd} \equiv I_{d1} - I_{d2} \quad V_{od} \equiv V_{o1} - V_{o2} = -I_{dd}R_D$$

Assume M1 and M2 are in the saturation region,

$$I_{d1} = \frac{1}{2}k(V_{gs1} - V_t)^2 \quad I_{d2} = \frac{1}{2}k(V_{gs2} - V_t)^2 \quad k = \mu C_{ox} \frac{W}{L}$$

# Source-Coupled Pair Large-Signal Behavior

---

Summing currents at the common source node, we have

$$I_{d1} + I_{d2} = I_{SS} \quad \Rightarrow \quad I_{d1} = \frac{I_{SS}}{2} + \frac{I_{dd}}{2} \quad I_{d2} = \frac{I_{SS}}{2} - \frac{I_{dd}}{2}$$

The gate voltages can be written as

$$V_{gs1} = V_t + \sqrt{\frac{2I_{d1}}{K}} \quad V_{gs2} = V_t + \sqrt{\frac{2I_{d2}}{K}}$$

The differential input voltage is

$$V_{id} = V_{gs1} - V_{gs2} = \sqrt{\frac{2I_{d1}}{k}} - \sqrt{\frac{2I_{d2}}{k}} = \sqrt{\frac{2}{k}} \left( \sqrt{I_{d1}} - \sqrt{I_{d2}} \right)$$

Squaring

$$V_{id}^2 = \frac{2}{k} \left[ I_{d1} + I_{d2} - 2\sqrt{I_{d1}I_{d2}} \right] = \frac{2}{k} \left[ I_{SS} - \sqrt{I_{SS}^2 - I_{dd}^2} \right]$$

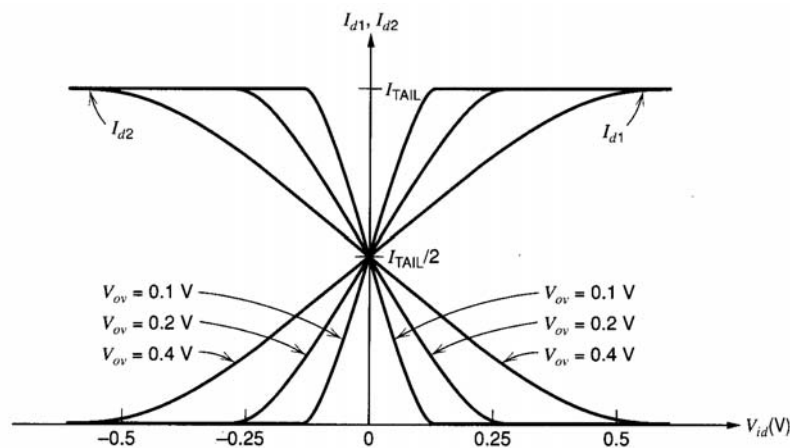
# Source-Coupled Pair Large-Signal Behavior

Rearrange, then we have

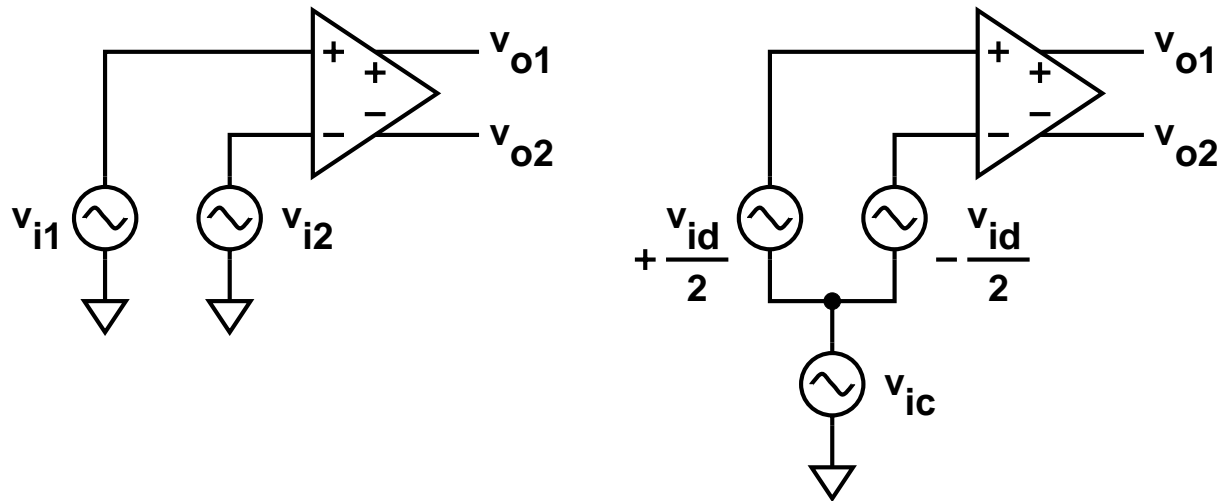
$$I_{dd} = \frac{k}{2} V_{id} \sqrt{\frac{4I_{SS}}{k} - V_{id}^2} \quad \text{and} \quad I_{d1} = \frac{I_{SS}}{2} + \frac{I_{dd}}{2} \quad I_{d2} = \frac{I_{SS}}{2} - \frac{I_{dd}}{2}$$

Define  $V_{IM}$  as the differential input voltage at which one of the MOST is turned off, i.e.,

$$I_{SS} = \frac{k}{2} V_{IM} \sqrt{\frac{4I_{SS}}{k} - V_{IM}^2} \Rightarrow V_{IM} = \sqrt{\frac{2I_{SS}}{k}} = \sqrt{2} (V_{ov1})|_{V_{id}=0} = \sqrt{2} (V_{ov2})|_{V_{id}=0}$$



# Small-Signal Analysis of Differential Amplifiers



The differential and common-mode signals are defined as

$$V_{id} \equiv V_{i1} - V_{i2} \quad V_{ic} \equiv \frac{V_{i1} + V_{i2}}{2} \quad V_{od} \equiv V_{o1} - V_{o2} \quad V_{oc} \equiv \frac{V_{o1} + V_{o2}}{2}$$

$$V_{i1} = V_{ic} + \frac{1}{2}V_{id} \quad V_{i2} = V_{ic} - \frac{1}{2}V_{id} \quad V_{o1} = V_{oc} + \frac{1}{2}V_{od} \quad V_{o2} = V_{oc} - \frac{1}{2}V_{od}$$

$$\begin{bmatrix} V_{o1} \\ V_{o2} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} V_{i1} \\ V_{i2} \end{bmatrix} \quad \begin{bmatrix} V_{od} \\ V_{oc} \end{bmatrix} = \begin{bmatrix} A_{dm} & A_{cdm} \\ A_{dcm} & A_{cm} \end{bmatrix} \begin{bmatrix} V_{id} \\ V_{ic} \end{bmatrix}$$

# Small-Signal Analysis of Differential Amplifiers

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The voltage gain are defined as

$$A_{11} = \left. \frac{V_{o1}}{V_{i1}} \right|_{v_{i2}=0} \quad A_{12} = \left. \frac{V_{o1}}{V_{i2}} \right|_{v_{i1}=0} \quad A_{21} = \left. \frac{V_{o2}}{V_{i1}} \right|_{v_{i2}=0} \quad A_{22} = \left. \frac{V_{o2}}{V_{i2}} \right|_{v_{i1}=0}$$

The differential and common-mode gains are

$$\text{Differential-Mode Gain} = A_{dm} = \left. \frac{V_{od}}{V_{id}} \right|_{v_{ic}=0} = \frac{A_{11} - A_{12} - A_{21} + A_{22}}{2}$$

$$\text{Common-Mode Gain} = A_{cm} = \left. \frac{V_{oc}}{V_{ic}} \right|_{v_{id}=0} = \frac{A_{11} + A_{12} + A_{21} + A_{22}}{2}$$

$$\text{Differential-Mode-to-Common-Mode Gain} = A_{dcm} = \left. \frac{V_{oc}}{V_{id}} \right|_{v_{ic}=0} = \frac{A_{11} - A_{12} + A_{21} - A_{22}}{4}$$

$$\text{Common-Mode-to-Differential-Mode Gain} = A_{cdm} = \left. \frac{V_{od}}{V_{ic}} \right|_{v_{id}=0} = A_{11} + A_{12} - A_{21} - A_{22}$$

# Small-Signal Analysis of Differential Amplifiers

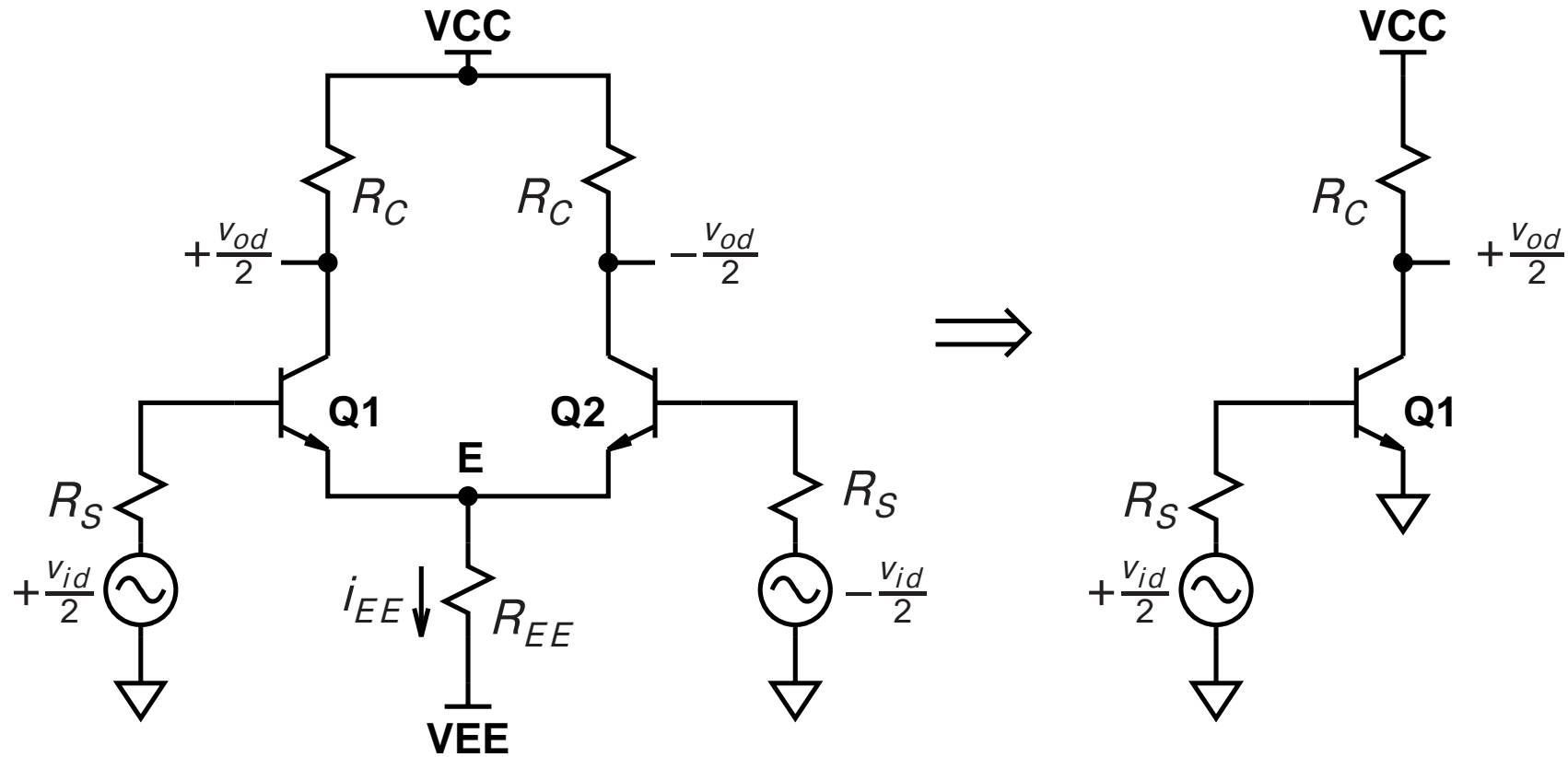
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- Usually want to sense  $v_{id}$  while rejecting  $v_{ic}$ , thus want  $A_{dm} \gg A_{cm}, A_{cdm}, A_{dcm}$ .
- The *common-mode-rejection ratio* is defined as

$$\text{CMRR} \equiv \left| \frac{A_{dm}}{A_{cm}} \right|$$

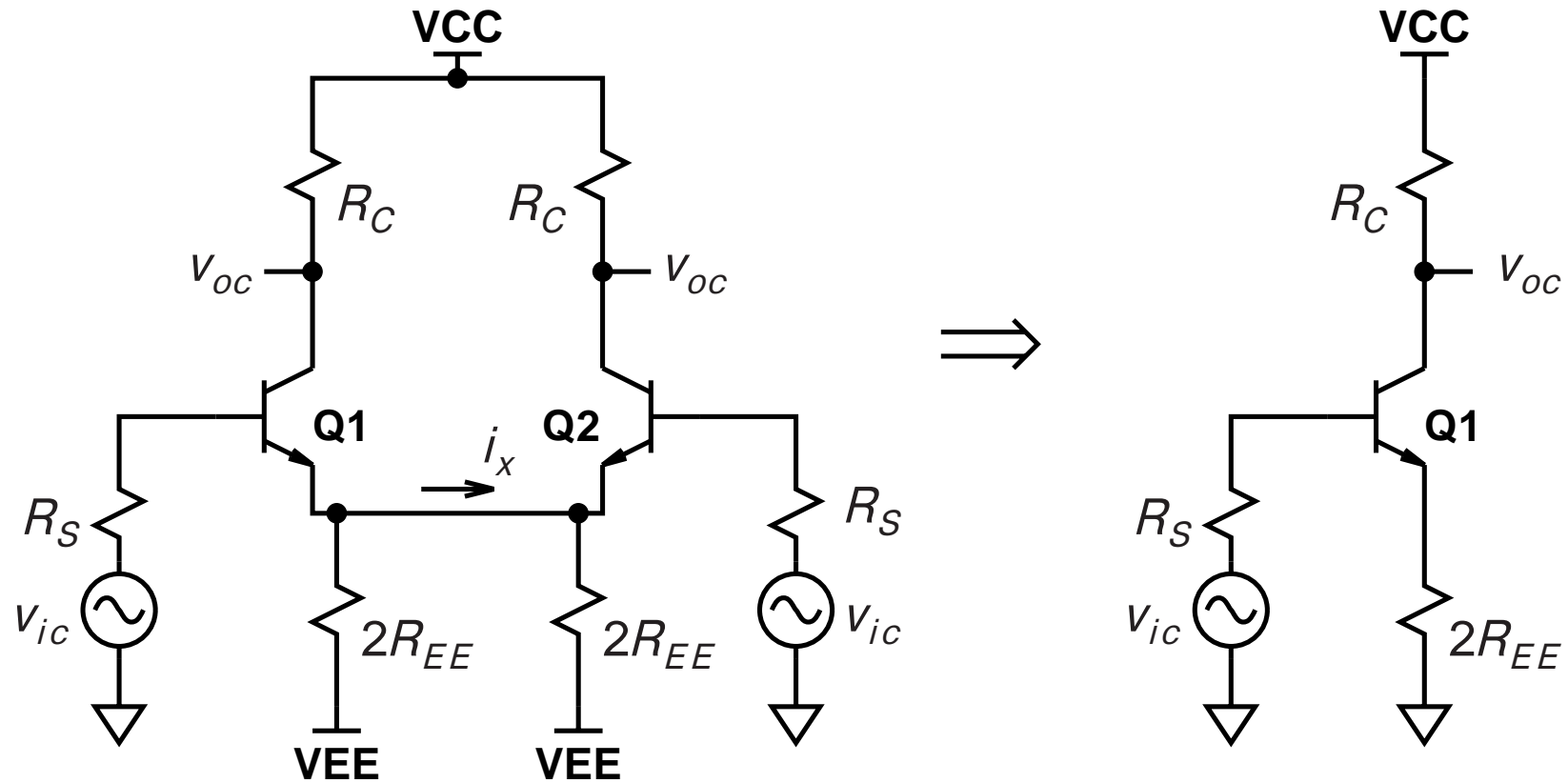
- In a perfectly balanced circuit,  $A_{cmd} = A_{dcm} = 0$ . However, in practice, these transfer functions are not zero because of component imbalances.
- The ratio  $A_{dm}/A_{cdm}$  is important because it indicates the extent to which a common-mode input corrupts the differential output.

# Emitter-Coupled Pair Differential-Mode Half Circuit



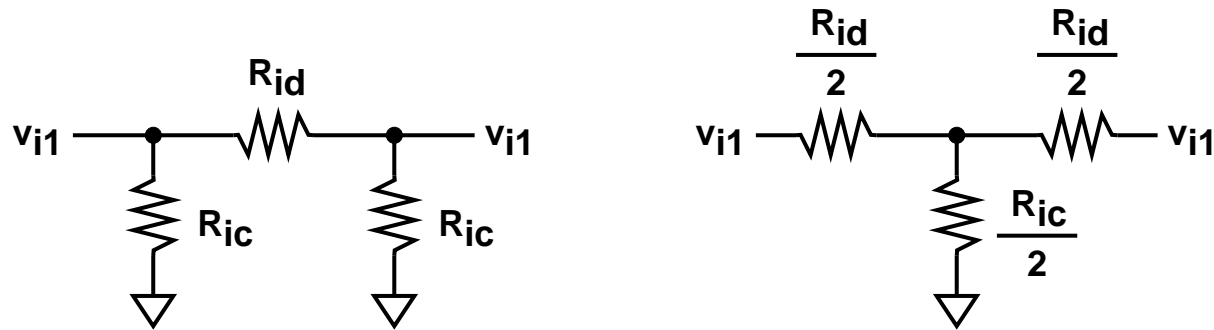
$$v_e = 0 \quad \Rightarrow \quad A_{dm} = \frac{v_{od}}{v_{id}} = \frac{v_{od}/2}{v_{id}/2} = -g_m \left( \frac{r_\pi}{r_\pi + R_S} \right) (r_o \parallel R_C)$$

# Emitter-Coupled Pair Common-Mode Half Circuit



$$i_x = 0 \quad \Rightarrow \quad A_{cm} = \frac{V_{oc}}{v_{ic}} = -\frac{g_m R_C}{1 + \frac{2g_m R_{EE}}{\alpha_o}} \approx -\frac{R_C}{2R_{EE}}$$

# Emitter-Coupled Pair Input Resistances



Assume  $R_S = 0$  and  $r_b = 0$ . When  $v_{ic} = 0$ ,  $i_{b1} = -i_{b2} \equiv i_{bd}$ ,

$$\text{Differential-Mode Input Resistance} = R_{id} \equiv \left. \frac{v_{id}}{i_{bd}} \right|_{v_{ic}=0} = 2r_{\pi}$$

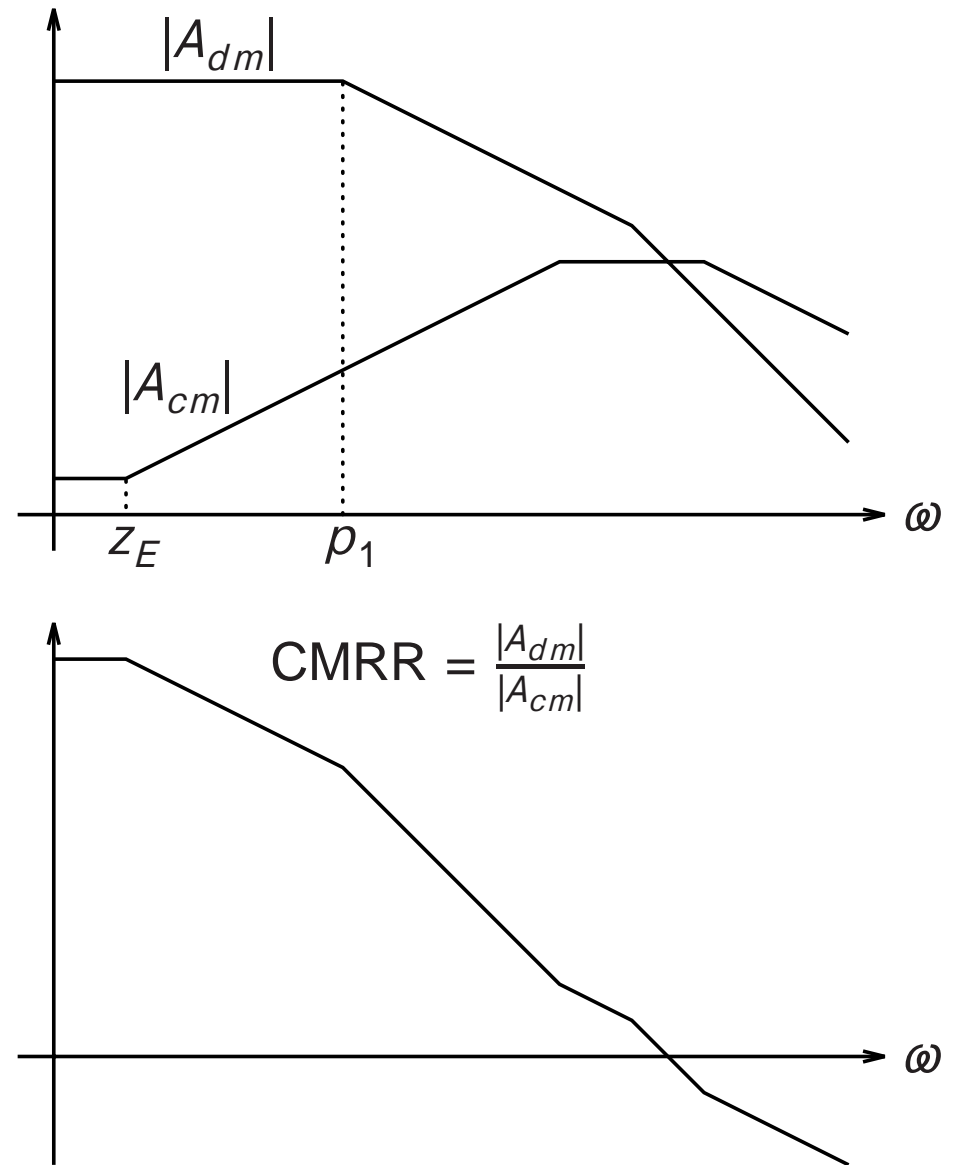
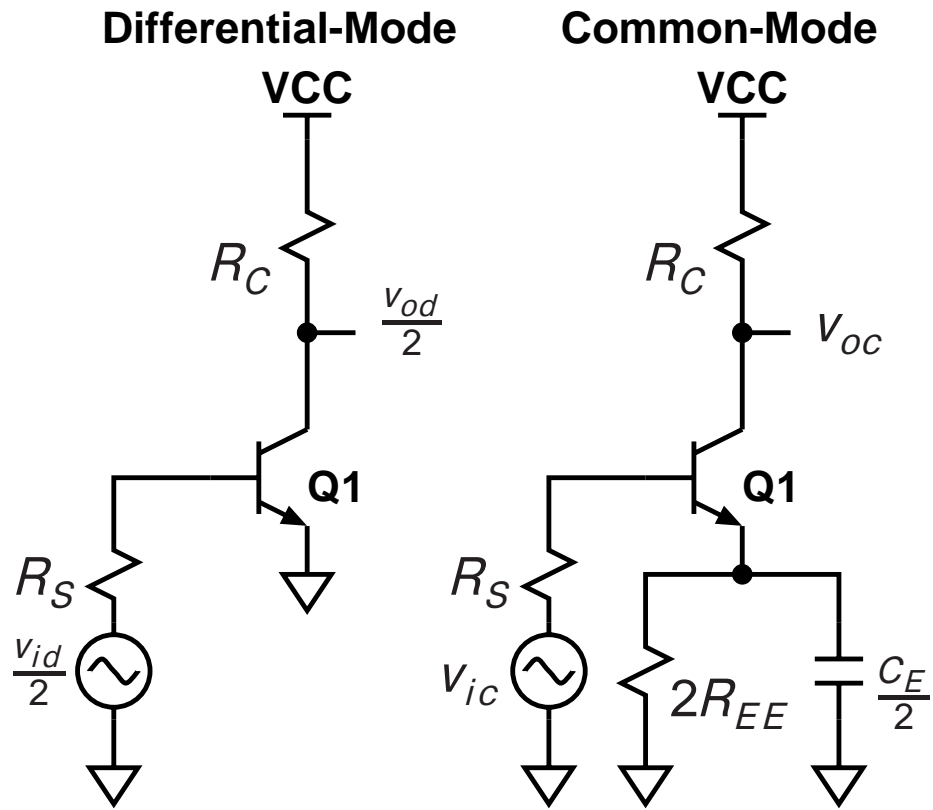
When  $v_{id} = 0$ ,  $i_{b1} = i_{b2} \equiv i_{bc}$ ,

$$\text{Common-Mode Input Resistance} = R_{ic} \equiv \left. \frac{v_{ic}}{i_{bc}} \right|_{v_{id}=0} = r_{\pi} + 2R_{EE}(\beta_o + 1) \approx 2\beta_o R_{EE}$$

In general

$$i_{b1} = +\frac{v_{id}}{R_{id}} + \frac{v_{ic}}{R_{ic}} \quad i_{b2} = -\frac{v_{id}}{R_{id}} + \frac{v_{ic}}{R_{ic}}$$

# Emitter-Coupled Pair Frequency Response



# Emitter-Coupled Pair Frequency Response

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- Using the Miller approximation, the differential Response can be written as

$$A_{dm}(s) = \frac{V_{od}}{V_{id}} \approx \frac{A_{dm}(0)}{1 - s/p_1}$$

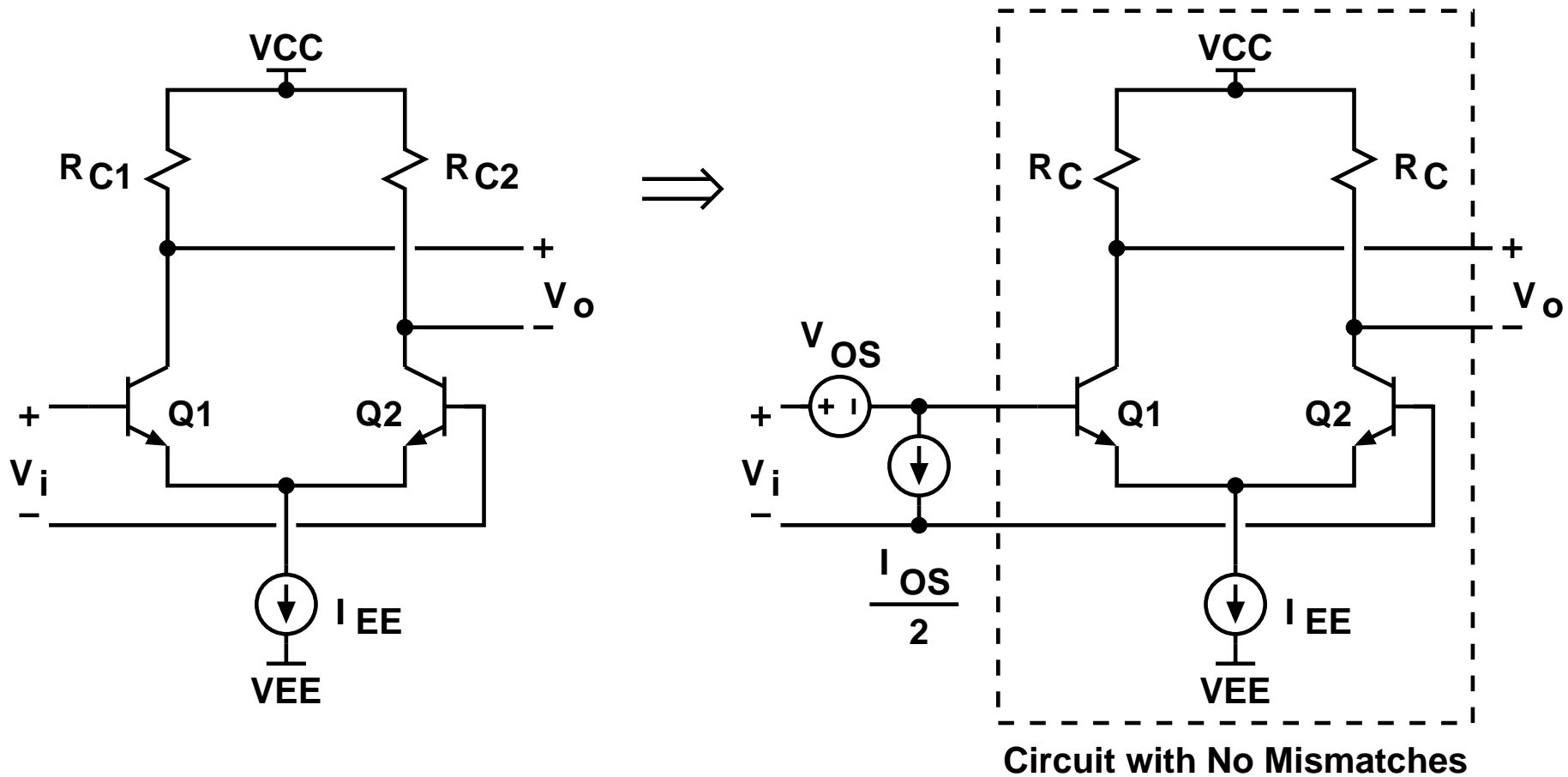
$$A_{dm}(0) = -g_m R_C \left( \frac{r_\pi}{R_S + r_b + r_\pi} \right) \quad p_1 = -\frac{1}{C_t [(R_S + r_b) \parallel r_\pi]} \quad C_t = C_\pi + C_\mu (1 + g_m R_C)$$

- Because  $R_{EE}$  is usually large, the common-mode response is typically dominated by the time constant at the tail node of the pair.

$$A_{cm}(s) = \frac{V_{oc}}{V_{ic}} \approx -\frac{R_C}{Z_E(s)} \approx A_{cm}(0) (1 - s/z_E) \quad Z_E(s) = \frac{1}{\frac{1}{2R_{EE}} + s\frac{C_E}{2}} = \frac{2R_{EE}}{1 + sC_E R_{EE}}$$

$$A_{cm}(0) = -\frac{R_C}{2R_{EE}} \quad z_E = -\frac{1}{R_{EE}C_E}$$

# Emitter-Coupled Pair Input Offset Voltage and Current



- $V_{OS}$  and  $I_{OS}$  is equal to the value of  $V_{ID} = V_{I1} - V_{I2}$  and  $I_{BD} = I_{B1} - I_{B2}$  that must be applied to the input to drive  $V_{OD} = 0$ .

# Emitter-Coupled Pair Input Offset Voltage

---

For BJTs in the forward-active region,

$$I_C = I_S e^{V_{BE}/U_T} \quad V_{BE} = U_T \ln \frac{I_C}{I_S} \quad I_S = A \frac{qn_i^2 D_n}{G(V_{CB})}$$

The output condition is

$$V_{OD} = -(I_{C1}R_{C1} - I_{C2}R_{C2}) = 0 \quad \Rightarrow \quad \frac{I_{C1}}{I_{C2}} = \frac{R_{C2}}{R_{C1}}$$

Since  $V_{OS} = V_{ID} = V_{BE1} - V_{BE2}$ , we have

$$V_{OS} = U_T \ln \frac{I_{C1}}{I_{S1}} - U_T \ln \frac{I_{C2}}{I_{S2}} = U_T \ln \left( \frac{I_{C1} I_{S2}}{I_{C2} I_{S1}} \right) = U_T \ln \left[ \frac{R_{C2}}{R_{C1}} \cdot \frac{A_2}{A_1} \cdot \frac{G_1(V_{CB1})}{G_2(V_{CB2})} \right]$$

# Emitter-Coupled Pair Input Offset Voltage

---

To describe the mismatch in the components, using

$$\Delta X = X_1 - X_2 \quad X = \frac{X_1 + X_2}{2} \quad \Rightarrow \quad X_1 = X + \frac{\Delta X}{2} \quad X_2 = X - \frac{\Delta X}{2}$$

Then

$$V_{OS} = U_T \ln \left[ \frac{R_C - \frac{\Delta R_C}{2}}{R_C + \frac{\Delta R_C}{2}} \cdot \frac{A - \frac{\Delta A}{2}}{A + \frac{\Delta A}{2}} \cdot \frac{G + \frac{\Delta G}{2}}{G - \frac{\Delta G}{2}} \right] = U_T \ln \left[ \frac{1 - \frac{1}{2} \frac{\Delta R_C}{R_C}}{1 + \frac{1}{2} \frac{\Delta R_C}{R_C}} \cdot \frac{1 - \frac{1}{2} \frac{\Delta A}{A}}{1 + \frac{1}{2} \frac{\Delta A}{A}} \cdot \frac{1 + \frac{1}{2} \frac{\Delta G}{G}}{1 - \frac{1}{2} \frac{\Delta G}{G}} \right]$$

From Taylor series, if  $y \ll 1$ ,  $\ln(1 + y) = y - \frac{y^2}{2} + \frac{y^3}{3} - \dots \approx y$ . We have

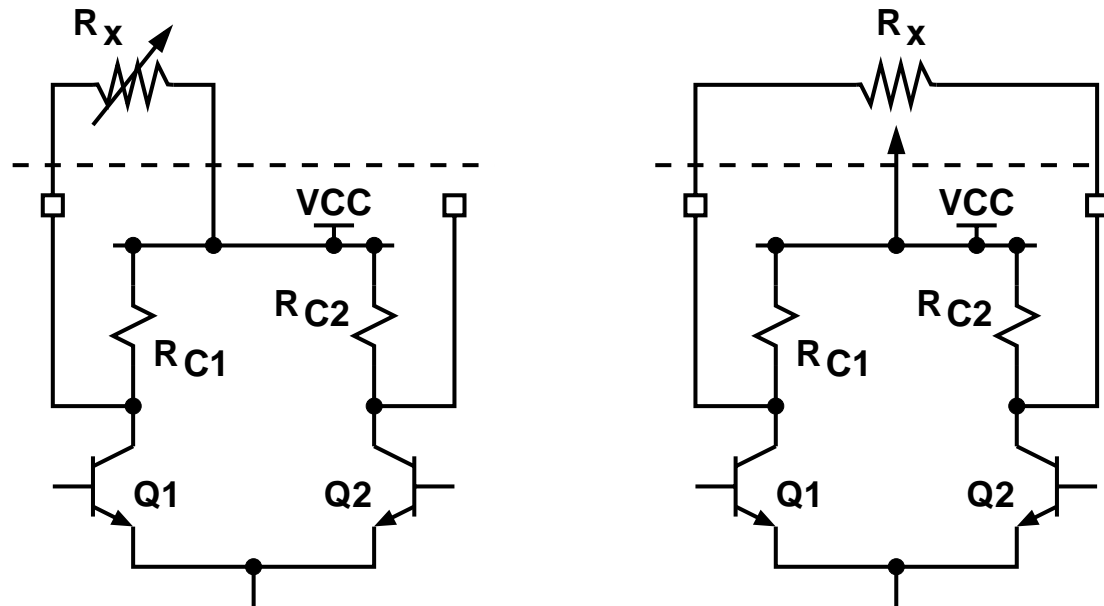
$$V_{OS} \approx U_T \left( -\frac{\Delta R_C}{R_C} - \frac{\Delta A}{A} + \frac{\Delta G}{G} \right) \quad \text{or} \quad V_{OS} = U_T \left( -\frac{\Delta R_C}{R_C} - \frac{\Delta I_S}{I_S} \right)$$

# Emitter-Coupled Pair Input Offset Voltage

- The offset voltage drift due to temperature variation is

$$\frac{dV_{OS}}{dT} = \frac{d}{dT} \left[ \frac{kT}{q} \left( -\frac{\Delta R_C}{R_C} - \frac{\Delta I_S}{I_S} \right) \right] = \frac{k}{q} \left( -\frac{\Delta R_C}{R_C} - \frac{\Delta I_S}{I_S} \right) = \frac{V_{OS}}{T}$$

- Nulling  $V_{OS}$  usually doesn't null  $dV_{OS}/dT$  because of how it is accomplished.
- $V_{OS}$  drifts in the  $1 \mu\text{V}/^\circ\text{C}$  range can be obtained with careful design.



# Emitter-Coupled Pair Input Offset Current

---

The input offset current is defined as

$$I_{OS} \equiv I_{BD}|_{V_{OD}=0} = I_{B1} - I_{B2} = \frac{I_{C1}}{\beta_{F1}} - \frac{I_{C2}}{\beta_{F2}}$$

As before, the formula can be arranged as

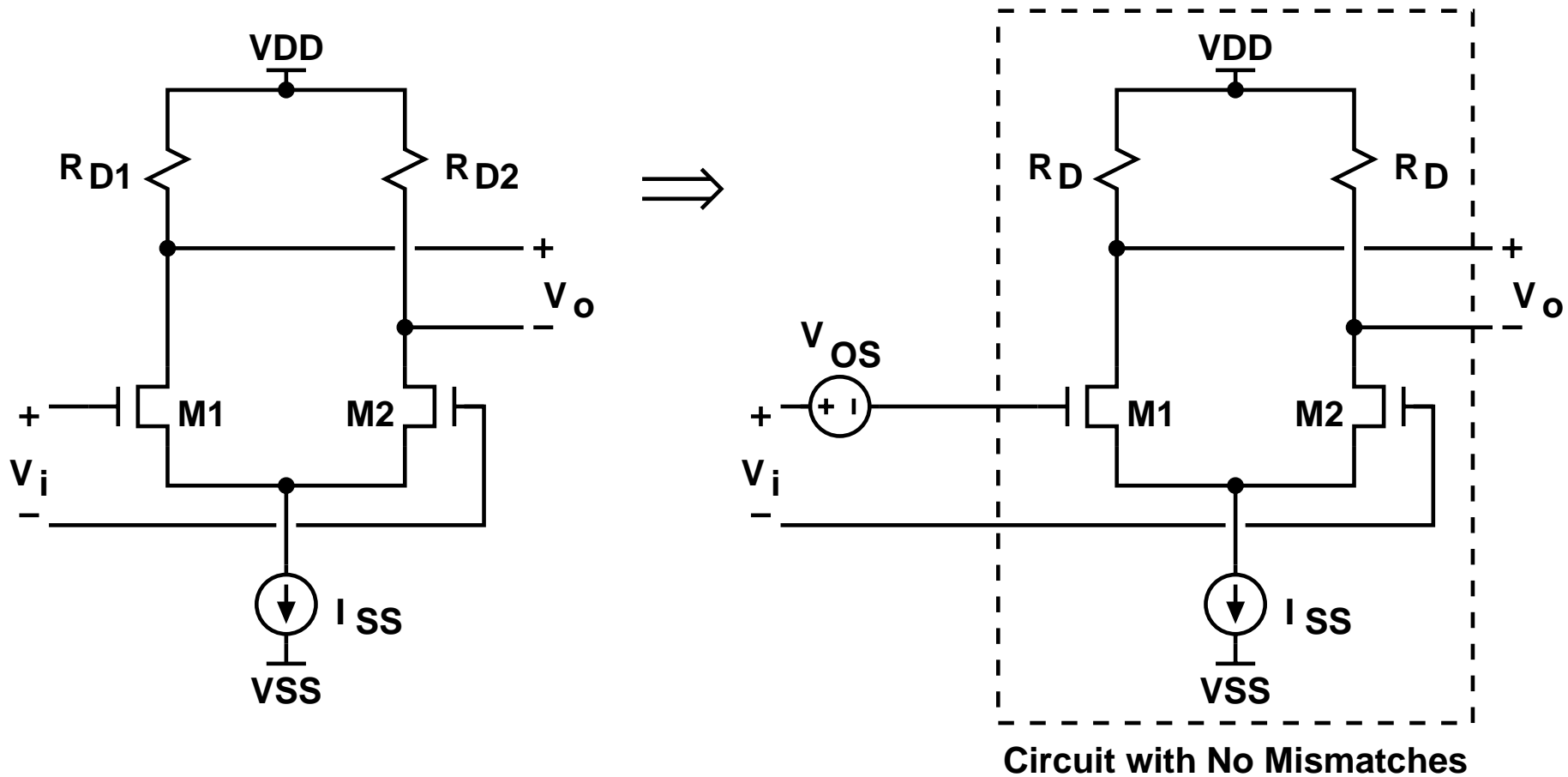
$$I_{OS} = \frac{I_C + \frac{\Delta I_C}{2}}{\beta_F + \frac{\Delta \beta_F}{2}} - \frac{I_C - \frac{\Delta I_C}{2}}{\beta_F - \frac{\Delta \beta_F}{2}} \approx \frac{I_C}{\beta_F} \left( \frac{\Delta I_C}{I_C} - \frac{\Delta \beta_F}{\beta_F} \right)$$

Since  $V_{OD} = 0$ , we have

$$I_{C1}R_{C1} = I_{C2}R_{C2} \quad \Rightarrow \quad \frac{\Delta I_C}{I_C} = -\frac{\Delta R_C}{R_C} \quad \Rightarrow \quad I_{OS} \approx -\frac{I_C}{\beta_F} \left( \frac{\Delta R_C}{R_C} + \frac{\Delta \beta_F}{\beta_F} \right)$$

- A typical  $\beta_F$  mismatch distribution displays a deviation of about 10%.

# Source-Coupled Pair Input Offset Voltage



$$V_{OS} = V_{GS1} - V_{GS2} \quad V_{GS} = V_t + \sqrt{\frac{2I_D}{k'(W/L)}} \quad k' = \mu C_{ox}$$

# Source-Coupled Pair Input Offset Voltage

---

Since  $V_{OD} = 0$ , we have

$$I_{D1}R_{D1} = I_{D2}R_{D2} \quad \Rightarrow \quad \frac{\Delta I_D}{I_D} = -\frac{\Delta R_D}{R_D}$$

The offset voltage is

$$V_{OS} = V_{GS1} - V_{GS2} = \Delta V_t + \sqrt{\frac{2I_D}{k'(W/L)}} \times \left( \sqrt{\frac{1 + \frac{1}{2} \frac{\Delta I_D}{I_D}}{1 + \frac{1}{2} \frac{\Delta(W/L)}{(W/L)}}} - \sqrt{\frac{1 - \frac{1}{2} \frac{\Delta I_D}{I_D}}{1 - \frac{1}{2} \frac{\Delta(W/L)}{(W/L)}}} \right)$$

Using Taylor series,

$$V_{OS} \approx \Delta V_t + \frac{V_{GS} - V_t}{2} \left[ \frac{\Delta I_D}{I_D} - \frac{\Delta(W/L)}{(W/L)} \right] \approx \Delta V_t + \frac{V_{GS} - V_t}{2} \left[ -\frac{\Delta R_D}{R_D} - \frac{\Delta(W/L)}{(W/L)} \right]$$

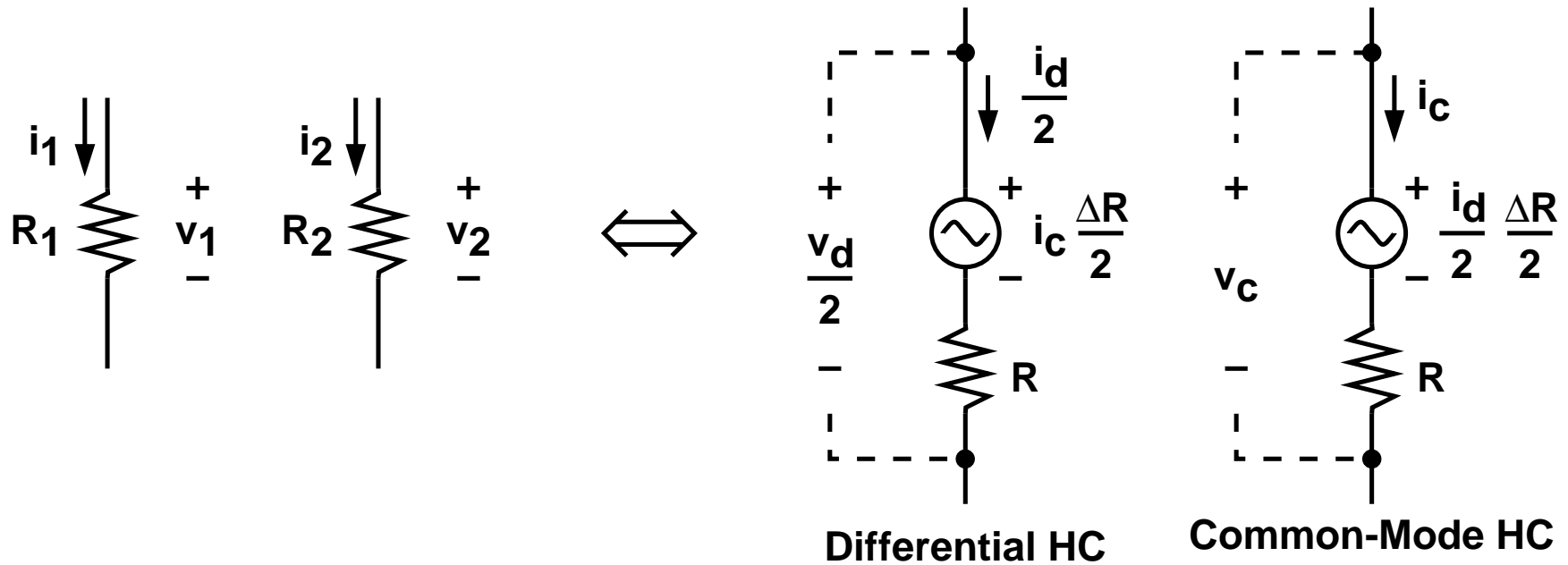
$$V_{GS} - V_t \equiv \sqrt{\frac{2I_D}{k'(W/L)}} = V_{ov} = \sqrt{\frac{2[(I_{D1} + I_{D2})/2]}{k'(W/L)}} = \sqrt{\frac{I_{SS}}{k'(W/L)}}$$

# Source-Coupled Pair Input Offset Voltage

---

- $\Delta V_t$  can be minimized by careful layout. Large-geometry structures can achieve a  $\Delta V_t$  with standard deviations on the order of 2 mV in modern MOS process.
- Due to the  $V_{GS} - V_t$  term, offset in MOST pairs is typically 10 times larger than that of BJT pairs.
- Both  $V_t$  and  $V_{ov}$  have a strong temperature dependence, affecting  $V_{GS}$  in opposite directions.
- $dV_{OS}/dT$  in MOST pairs is not well correlated with  $V_{OS}$ , unlike BJT pairs.

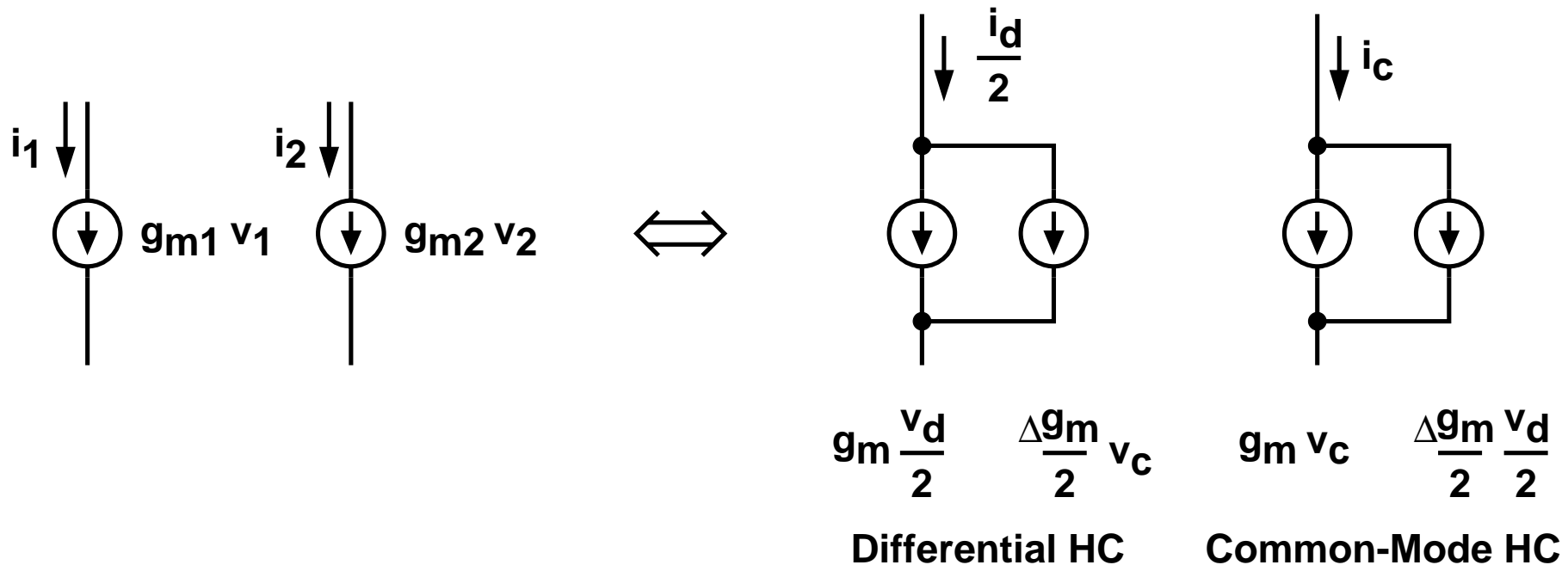
# Unbalanced Resistor Circuit Analysis



$$V_d = v_1 - v_2 = i_1 R_1 - i_2 R_2 = \left( i_c + \frac{i_d}{2} \right) \left( R + \frac{\Delta R}{2} \right) - \left( i_c - \frac{i_d}{2} \right) \left( R - \frac{\Delta R}{2} \right) = i_d R + i_c (\Delta R)$$

$$V_c = \frac{v_1 + v_2}{2} = \frac{\left( i_c + \frac{i_d}{2} \right) \left( R + \frac{\Delta R}{2} \right) + \left( i_c - \frac{i_d}{2} \right) \left( R - \frac{\Delta R}{2} \right)}{2} = i_c R + i_d \frac{\Delta R}{4}$$

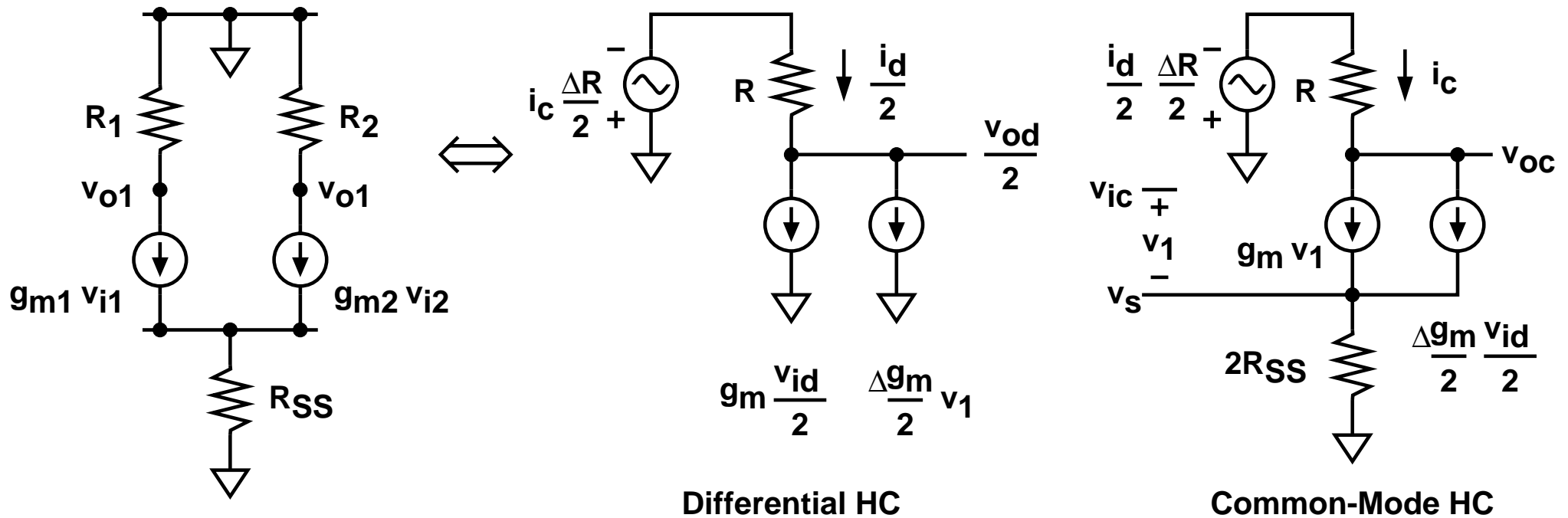
# Unbalanced $g_m$ Circuit Analysis



$$i_d = i_1 - i_2 = \left( g_m + \frac{\Delta g_m}{2} \right) \left( v_c + \frac{v_d}{2} \right) - \left( g_m - \frac{\Delta g_m}{2} \right) \left( v_c - \frac{v_d}{2} \right) = g_m v_d + \Delta g_m v_c$$

$$i_c = \frac{i_1 + i_2}{2} = \frac{\left( g_m + \frac{\Delta g_m}{2} \right) \left( v_c + \frac{v_d}{2} \right) - \left( g_m - \frac{\Delta g_m}{2} \right) \left( v_c - \frac{v_d}{2} \right)}{2} = g_m v_c + \frac{\Delta g_m v_d}{4}$$

# Unbalanced Differential Amplifier



If  $\Delta R = 0$  and  $\Delta g_m = 0$ , we have

$$A_{dm} = -g_m R \quad A_{cm} = -\frac{g_m R}{1 + 2g_m R_{SS}} \quad A_{cdm} = 0 \quad A_{dcm} = 0$$

# Unbalanced Differential Amplifier

---

Including mismatches, the voltage gains are

$$\begin{bmatrix} V_{od} \\ V_{oc} \end{bmatrix} = \begin{bmatrix} A_{dm} & A_{cdm} \\ A_{dcm} & A_{cm} \end{bmatrix} \begin{bmatrix} V_{id} \\ V_{ic} \end{bmatrix}$$

where

$$A_{dm} = \left. \frac{V_{od}}{V_{id}} \right|_{v_{ic}=0} = -g_m R + \frac{\Delta g_m R_{SS} \frac{\Delta g_m R}{2} - \frac{\Delta g_m \Delta R}{2}}{1 + 2g_m R_{SS}}$$

$$A_{cdm} = \left. \frac{V_{od}}{V_{ic}} \right|_{v_{id}=0} = -\frac{g_m \Delta R + \Delta g_m R}{1 + 2g_m R_{SS}}$$

$$A_{dcm} = \left. \frac{V_{oc}}{V_{id}} \right|_{v_{ic}=0} = -\frac{1}{4} \left[ g_m \Delta R + \frac{\Delta g_m R - g_m \Delta R \left( 2g_m R_{SS} \left( \frac{\Delta g_m}{2g_m} \right)^2 \right)}{1 + 2g_m R_{SS}} \right]$$

$$A_{cm} = \left. \frac{V_{oc}}{V_{ic}} \right|_{v_{id}=0} = -\frac{g_m R + \frac{\Delta g_m \Delta R}{2}}{1 + 2g_m R_{SS}}$$

# Simplified Analysis for Unbalanced Differential Amplifier

---

First assume no mismatches, and find  $A_{dm}$ ,  $A_{cm}$ ,  $\hat{v}_{od}$ ,  $\hat{i}_d$ ,  $\hat{v}_{oc}$ ,  $\hat{i}_c$ , and  $\hat{v}_1$ ,

$$A_{dm} = -g_m R \quad A_{cm} = -\frac{g_m R}{1 + 2g_m R_{SS}} \quad \hat{v}_{od} = A_{dm} v_{id} = -g_m R v_{id} \quad \hat{i}_d = g_m v_{id}$$

$$\hat{v}_{oc} = A_c v_{ic} = -\frac{g_m R v_{ic}}{1 + 2g_m R_{SS}} \quad \hat{v}_1 = \frac{v_{ic}}{1 + 2g_m R_{SS}} \quad \hat{i}_c = \frac{g_m v_{ic}}{1 + 2g_m R_{SS}}$$

Then consider only the mismatch terms,

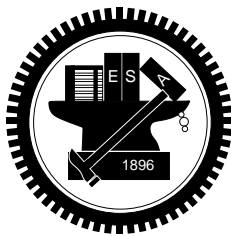
$$-\hat{i}_c \frac{\Delta R}{2} - R \frac{\Delta g_m}{2} \hat{v}_1 = \frac{v'_{od}}{2} \Rightarrow A_{cdm} = \left. \frac{v'_{od}}{v_{ic}} \right|_{v_{id}=0} = -\frac{g_m \Delta R + \Delta g_m R}{1 + 2g_m R_{SS}}$$

$$-\frac{\hat{i}_d \Delta R}{2} - R \frac{\Delta g_m}{2(1 + 2g_m R_{SS})} \frac{v_{id}}{2} = v'_{oc} \Rightarrow A_{dcm} = \left. \frac{v'_{oc}}{v_{id}} \right|_{v_{ic}=0} = -\frac{1}{4} \left( g_m \Delta R + \frac{\Delta g_m R}{1 + 2g_m R_{SS}} \right)$$

# Current Mirrors and Active Loads

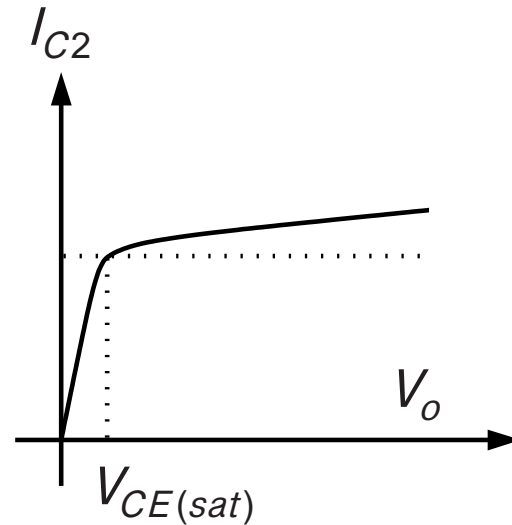
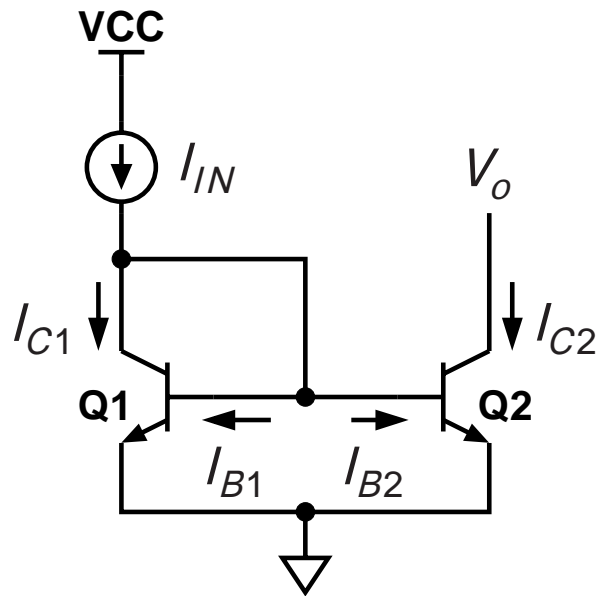
Jieh-Tsorng Wu

November 7, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Simple BJT Current Mirror



$$\beta_{F1} = \beta_{F2} = \beta_F$$

$$V_{A1} = V_{A2} = V_A$$

$$I_{C1} = I_{S1} e^{V_{BE}/U_T} \left( 1 + \frac{V_{CE1}}{V_A} \right)$$

$$I_{C2} = I_{S2} e^{V_{BE}/U_T} \left( 1 + \frac{V_{CE2}}{V_A} \right)$$

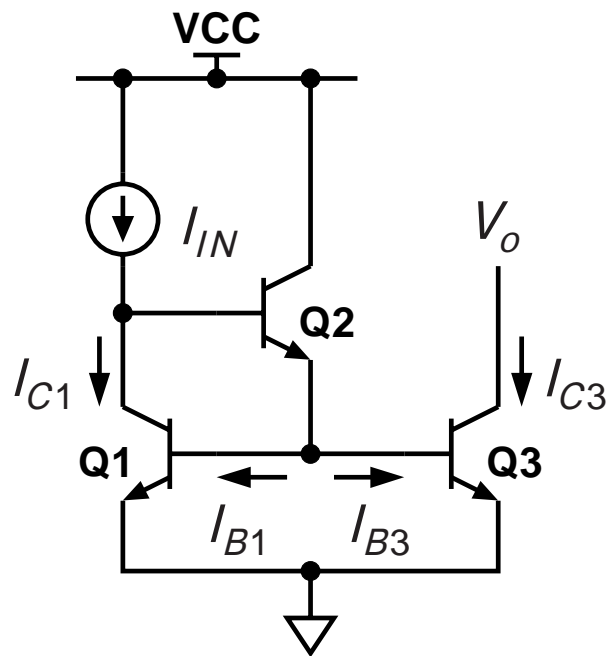
$$I_{IN} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + \frac{I_{C1}}{\beta_F} + \frac{I_{C2}}{\beta_F}$$

$$I_{C2} = I_{C1} \frac{I_{S2}}{I_{S1}} \left( 1 + \frac{V_{CE2} - V_{CE1}}{V_A + V_{CE1}} \right) = I_{IN} \cdot \frac{I_{S2}}{I_{S1}} \cdot \frac{1 + \frac{V_{CE2} - V_{CE1}}{V_A + V_{CE1}}}{1 + \frac{1}{\beta_F} + \frac{1}{\beta_F} \frac{I_{S2}}{I_{S1}} \left( 1 + \frac{V_{CE2} - V_{CE1}}{V_A + V_{CE1}} \right)}$$

$$I_{C2} = I_{IN} \cdot \frac{I_{S2}}{I_{S1}} \cdot (1 + \epsilon) \quad \epsilon = \text{Systematic Gain Error} \approx \frac{V_{CE2} - V_{CE1}}{V_A} - \frac{1}{\beta_F} \left( 1 + \frac{I_{S2}}{I_{S1}} \right)$$

$$R_{o2} = r_{o2} \quad V_{o(min)} = V_{CE2(sat)} \quad V_{CC(min)} = V_{BE1(on)}$$

# Simple BJT Current Mirror with Beta Helper



- Ignore Early effect. For Q1 and Q2, let

$$\beta_{F1} = \beta_{F3} = \beta_F \quad \frac{I_{C3}}{I_{C1}} = \frac{I_{S3}}{I_{S1}}$$

- From KCL,

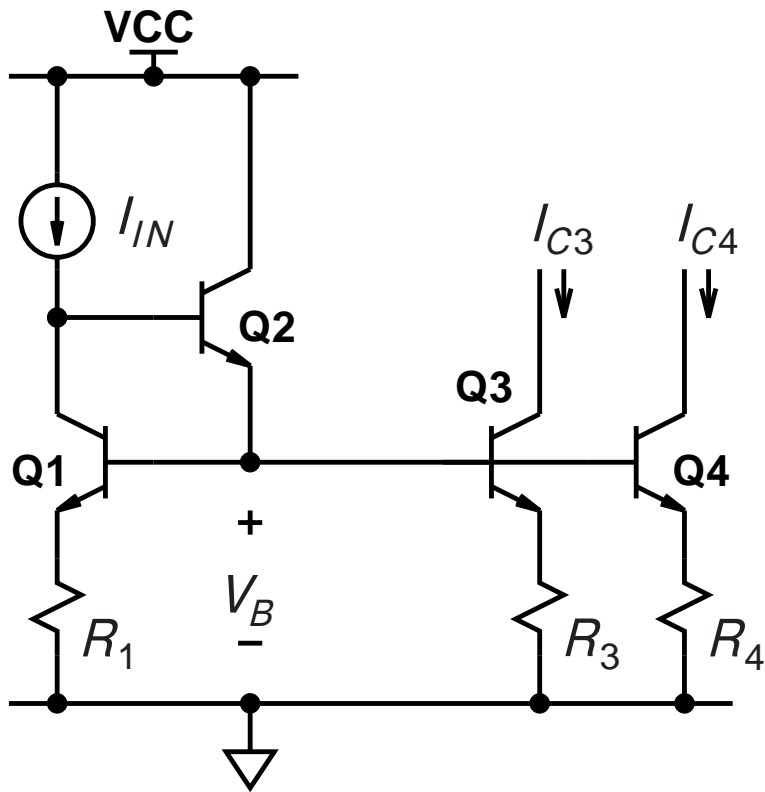
$$I_{IN} = I_{C1} + \frac{I_{B1} + I_{B3}}{\beta_{F2} + 1} = I_{C1} + \frac{1}{\beta_F(\beta_{F2} + 1)}(I_{C1} + I_{C3})$$

$$I_{C3} = I_{C1} \frac{I_{S3}}{I_{S1}} = I_{IN} \cdot \frac{I_{S3}}{I_{S1}} \cdot \frac{1}{1 + \frac{1}{\beta_F(\beta_{F2} + 1)} \left(1 + \frac{I_{S3}}{I_{S1}}\right)} = I_{IN} \cdot \frac{I_{S3}}{I_{S1}} \cdot (1 + \epsilon)$$

$$\epsilon \approx -\frac{1}{\beta_F(\beta_{F2} + 1)} \left(1 + \frac{I_{S3}}{I_{S1}}\right)$$

$$R_{o3} = r_{o3} \quad V_{o(min)} = V_{CE3(sat)} \quad V_{CC(min)} = V_{BE1(on)} + V_{BE2(on)}$$

# Simple BJT Current Mirror with Emitter Degeneration



$$V_B = I_{C1}R_1 + U_T \ln \frac{I_{C1}}{I_{S1}} = I_{C3}R_3 + U_T \ln \frac{I_{C3}}{I_{S3}}$$

$$I_{C1}R_1 \left( \frac{I_{C3}I_{S1}}{I_{C1}I_{S3}} - 1 \right) = U_T \ln \left( \frac{I_{C1}I_{S3}}{I_{C3}I_{S1}} \right)$$

$$\text{If } \frac{I_{S3}}{I_{S1}} = \frac{R_1}{R_3} \text{ then } \frac{I_{C3}}{I_{C1}} = \frac{I_{S3}}{I_{S1}}$$

- The BJT should be scaled with corresponding emitter resistor.

$$R_{o3} \approx r_{o3} \left( 1 + g_{m3}R_3 \right) = r_{o3} \left( 1 + \frac{I_{C3}R_3}{U_T} \right) \quad \epsilon|_{\beta_F=\infty} = \frac{V_{CE3} - V_{CE1}}{V_A(1 + g_{m3}R_E)} = \frac{V_{CE3} - V_{CE1}}{V_A \left( 1 + \frac{I_{C3}R_3}{U_T} \right)}$$

$$V_{o(min)} = V_{CE3(sat)} + I_{C3}R_3 \quad V_{CC(min)} = V_{BE1(on)} + V_{BE2(on)} + I_{C1}R_1$$

# Matching Consideration in BJT Current Mirrors

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Assume  $Q3 \approx Q4$ , and let

$$\Delta I_C \equiv I_{C3} - I_{C4} \quad \Delta I_S \equiv I_{S3} - I_{S4} \quad \Delta \alpha_F \equiv \alpha_{F3} - \alpha_{F4} \quad \Delta R \equiv R_3 - R_4$$

$$I_C \equiv \frac{I_{C3} + I_{C4}}{2} \quad I_S \equiv \frac{I_{S3} + I_{S4}}{2} \quad \alpha_F \equiv \frac{\alpha_{F3} + \alpha_{F4}}{2} \quad R \equiv \frac{R_3 + R_4}{2}$$

To calculate mismatch between  $I_{C3}$  and  $I_{C4}$ ,

$$V_B = V_{BE3} + I_{E3}R_3 = V_{BE4} + I_{E4}R_4 = U_T \ln \frac{I_{C3}}{I_{S3}} + \frac{I_{C3}}{\alpha_{F3}}R_3 = U_T \ln \frac{I_{C4}}{I_{S4}} + \frac{I_{C4}}{\alpha_{F4}}R_4$$

$$U_T \ln \frac{I_{C3}}{I_{C4}} - U_T \ln \frac{I_{S3}}{I_{S4}} + \frac{I_{C3}}{\alpha_{F3}}R_3 - \frac{I_{C4}}{\alpha_{F4}}R_4 = 0$$

$$U_T \ln \left( \frac{I_C + \frac{\Delta I_C}{2}}{I_C - \frac{\Delta I_C}{2}} \right) - U_T \ln \left( \frac{I_S + \frac{\Delta I_S}{2}}{I_S - \frac{\Delta I_S}{2}} \right) + \frac{\left( I_C + \frac{\Delta I_C}{2} \right) \left( R + \frac{\Delta R}{2} \right)}{\alpha_F + \frac{\Delta \alpha_F}{2}} - \frac{\left( I_C - \frac{\Delta I_C}{2} \right) \left( R - \frac{\Delta R}{2} \right)}{\alpha_F - \frac{\Delta \alpha_F}{2}} = 0$$

$$U_T \frac{\Delta I_C}{I_C} - U_T \frac{\Delta I_S}{I_S} + \frac{I_C R}{\alpha_F} \left( 1 + \frac{\Delta I_C}{2I_C} + \frac{\Delta R}{2R} - \frac{\Delta \alpha_F}{2\alpha_F} \right) - \frac{I_C R}{\alpha_F} \left( 1 - \frac{\Delta I_C}{2I_C} - \frac{\Delta R}{2R} + \frac{\Delta \alpha_F}{2\alpha_F} \right) = 0$$

# Matching Consideration in BJT Current Mirrors

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With above approximations, we obtain

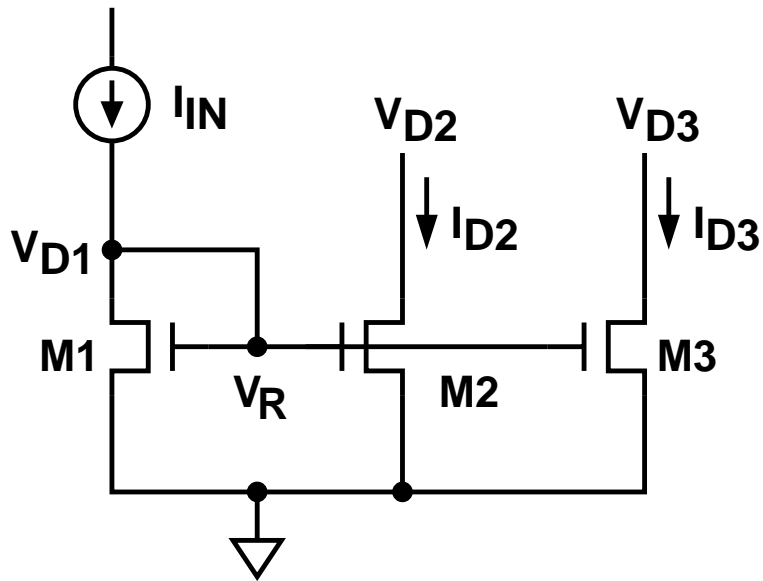
$$\frac{\Delta I_C}{I_C} \approx \left( \frac{1}{1 + \frac{g_m R}{\alpha_F}} \right) \frac{\Delta I_S}{I_S} + \frac{\frac{g_m R}{\alpha_F}}{1 + \frac{g_m R}{\alpha_F}} \left( -\frac{\Delta R}{R} + \frac{\Delta \alpha_F}{\alpha_F} \right)$$

For a typical bipolar process

$$\frac{\Delta I_S}{I_S} \simeq \pm 1\% - \pm 10\% \quad \frac{\Delta \alpha_F}{\alpha_F} \simeq \pm 0.1\%(\text{nnp}) \pm 1\%(\text{pnp}) \quad \frac{\Delta R}{R} \simeq \pm 0.1\% - \pm 2\%$$

- If  $g_m R \ll 1$ , the  $I_C$  mismatch is determined by  $I_S$  mismatch.
- If  $g_m R \gg 1$ , the  $I_C$  mismatch is determined by  $R$  and  $\alpha_F$  mismatches.

# Simple MOST Current Mirror



$$k' = \mu_n C_{ox}$$

$$I_{IN} = \frac{1}{2} k' \left( \frac{W}{L} \right)_1 (V_R - V_{t1})^2 (1 + \lambda_1 V_{D1})$$

$$I_{D2} = \frac{1}{2} k' \left( \frac{W}{L} \right)_2 (V_R - V_{t2})^2 (1 + \lambda_2 V_{D2})$$

$$I_{D3} = \frac{1}{2} k' \left( \frac{W}{L} \right)_3 (V_R - V_{t3})^2 (1 + \lambda_3 V_{D3})$$

Let  $V_{t1} = V_{t2} = V_t$  and  $\lambda_1 = \lambda_2 = \lambda$ , then

$$I_{D2} = I_{IN} \cdot \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{D2}}{1 + \lambda V_{D1}} = I_{IN} \cdot \frac{(W/L)_2}{(W/L)_1} \cdot (1 + \epsilon) \quad \epsilon \approx \lambda(V_{D2} - V_{D1}) = \frac{V_{D2} - V_{D1}}{V_A}$$

$$R_{o2} = r_{o2} = \frac{1}{\lambda_2 I_{D2}} \quad V_{o2(min)} = V_{ov2} \approx V_{ov1} \approx \sqrt{\frac{2I_{IN}}{k'(W/L)_1}} \quad V_{DD(min)} = V_{GS1} = V_t + V_{ov1}$$

# Matching Consideration in Simple MOST Current Mirror

---

Ignore  $\lambda$  effects. Assume  $M2 \simeq M3$ , and let

$$\Delta I_D \equiv I_{D2} - I_{D3} \quad \Delta(W/L) \equiv (W/L)_2 - (W/L)_3 \quad \Delta V_t \equiv V_{t2} - V_{t3}$$

$$I_D \equiv \frac{I_{D2} + I_{D3}}{2} \quad (W/L) \equiv \frac{(W/L)_2 + (W/L)_3}{2} \quad V_t \equiv \frac{V_{t2} + V_{t3}}{2}$$

$$V_R = V_{t2} + V_{ov2} = V_{t3} + V_{ov3} = V_{t2} + \sqrt{\frac{2I_{D2}}{k'(W/L)_2}} = V_{t3} + \sqrt{\frac{2I_{D3}}{k'(W/L)_3}}$$

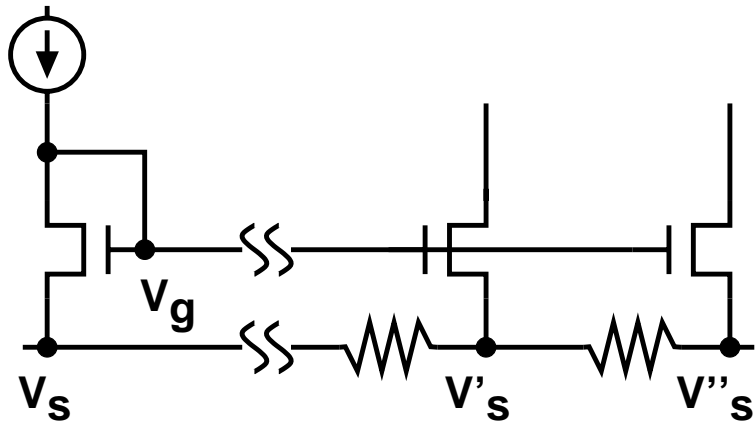
Neglecting all second order terms, we obtain

$$\frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{(W/L)} - \frac{\Delta V_t}{V_{ov}/2} \quad V_{ov} = \sqrt{\frac{2I_D}{k'(W/L)}}$$

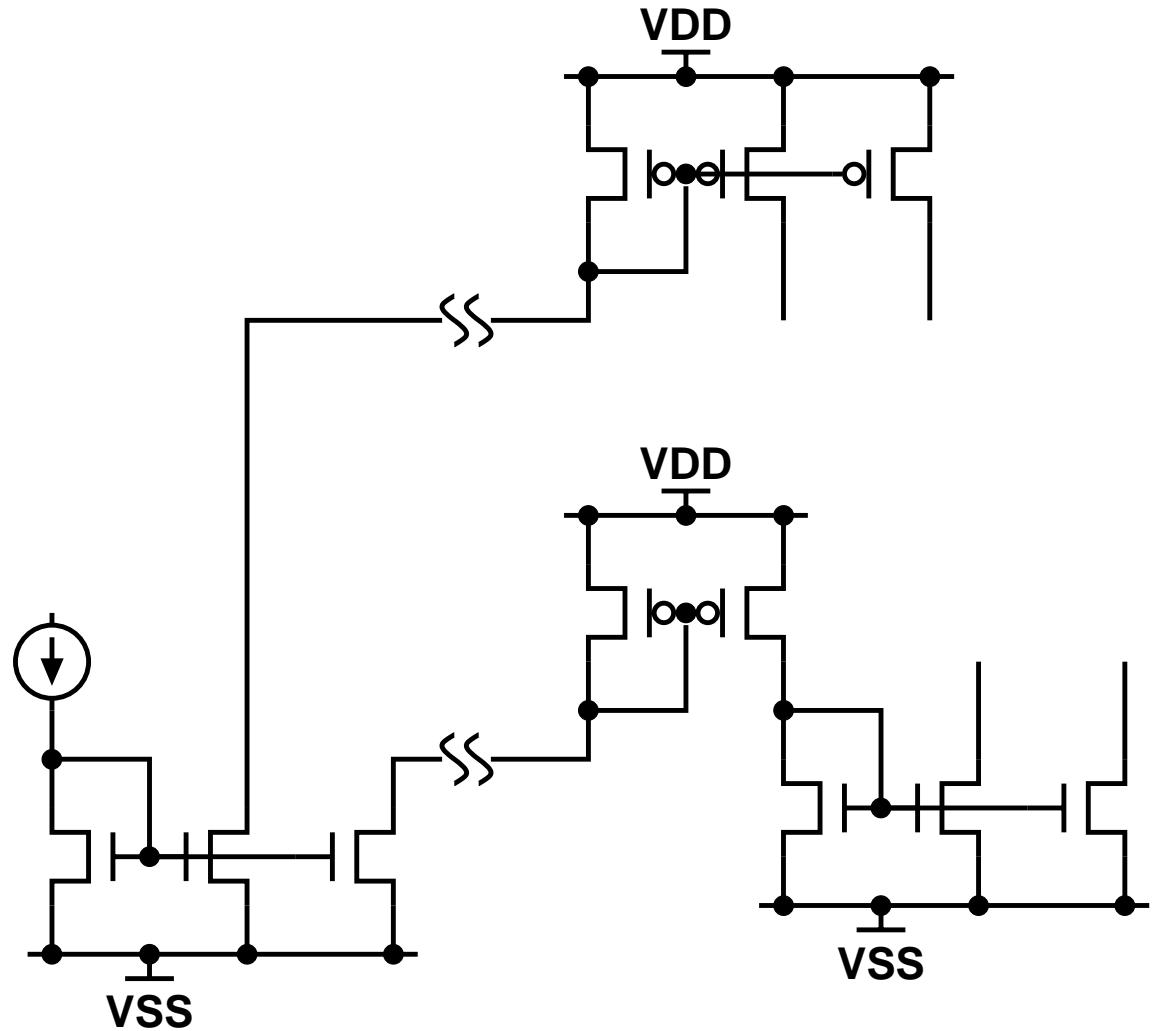
- To maximize output swing, want a small  $V_{ov}$ . But then  $\Delta I_D/I_D$  increases as  $V_{ov}$  decreases for a given  $\Delta V_t$ .

# Layout Considerations

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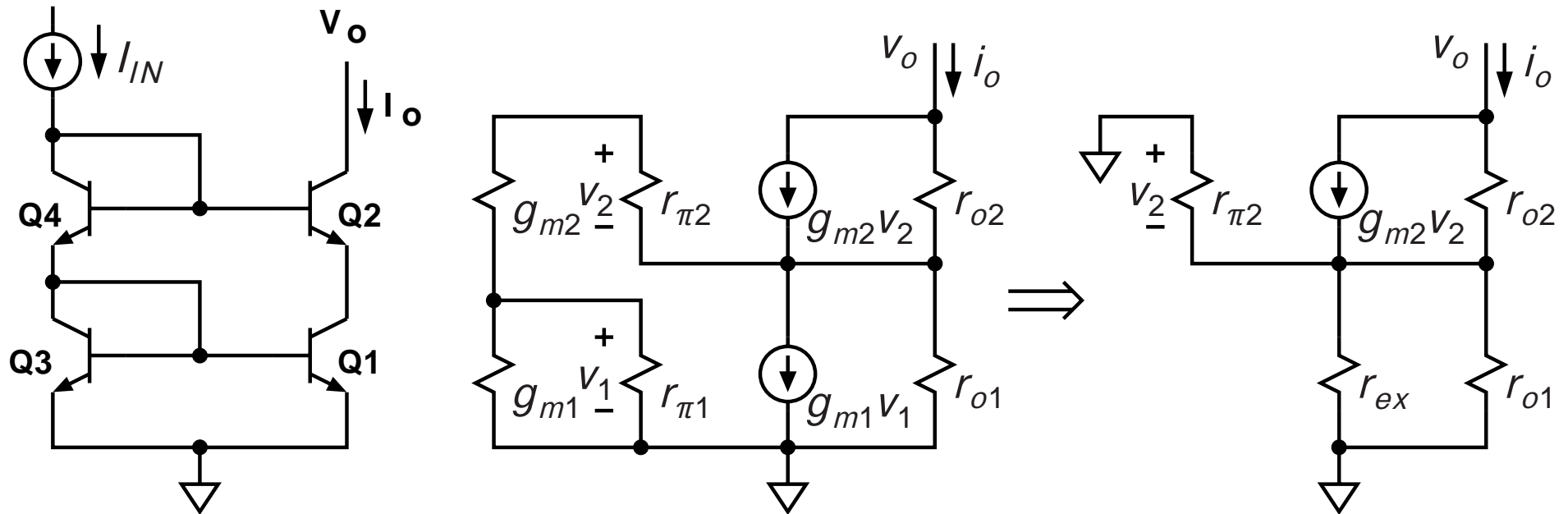


Voltage Routing



Current Routing

# BJT Cascode Current Mirror



$$g_{m1} = g_{m2} \Rightarrow \frac{1}{r_{ex}} \approx g_{m1} \frac{\frac{1}{g_{m1}}}{r_{\pi2} + \frac{1}{g_{m2}} + \frac{1}{g_{m1}}} \approx \frac{g_{m2}}{\beta_{o2} + 2} \approx \frac{1}{r_{\pi2}} \Rightarrow R_E = r_{o1} \parallel r_{ex} \approx r_{\pi2}$$

$$R_o \approx r_{o2} \left( 1 + \frac{g_{m2} R_E}{1 + \frac{g_{m2} R_E}{\beta_{o2}}} \right) \approx r_{o2} \left( 1 + \frac{\beta_{o2} r_{\pi2}}{r_{\pi2} + r_{\pi2}} \right) \approx \frac{\beta_{o2} r_{o2}}{2}$$

$$V_{o(min)} = V_{CE1} + V_{CE2(sat)} \approx V_{BE3(on)} + V_{CE2(sat)} \quad V_{CC(min)} = V_{BE3(on)} + V_{BE4(on)}$$

# BJT Cascode Current Mirror

---

Neglect Early effect. Let  $Q1=Q3$ ,

$$I_{C3} = I_{C1} \quad I_{C2} = I_{C1} \frac{\beta_F}{\beta_F + 1} = I_{C3} \frac{\beta_F}{\beta_F + 1}$$

From KCL,

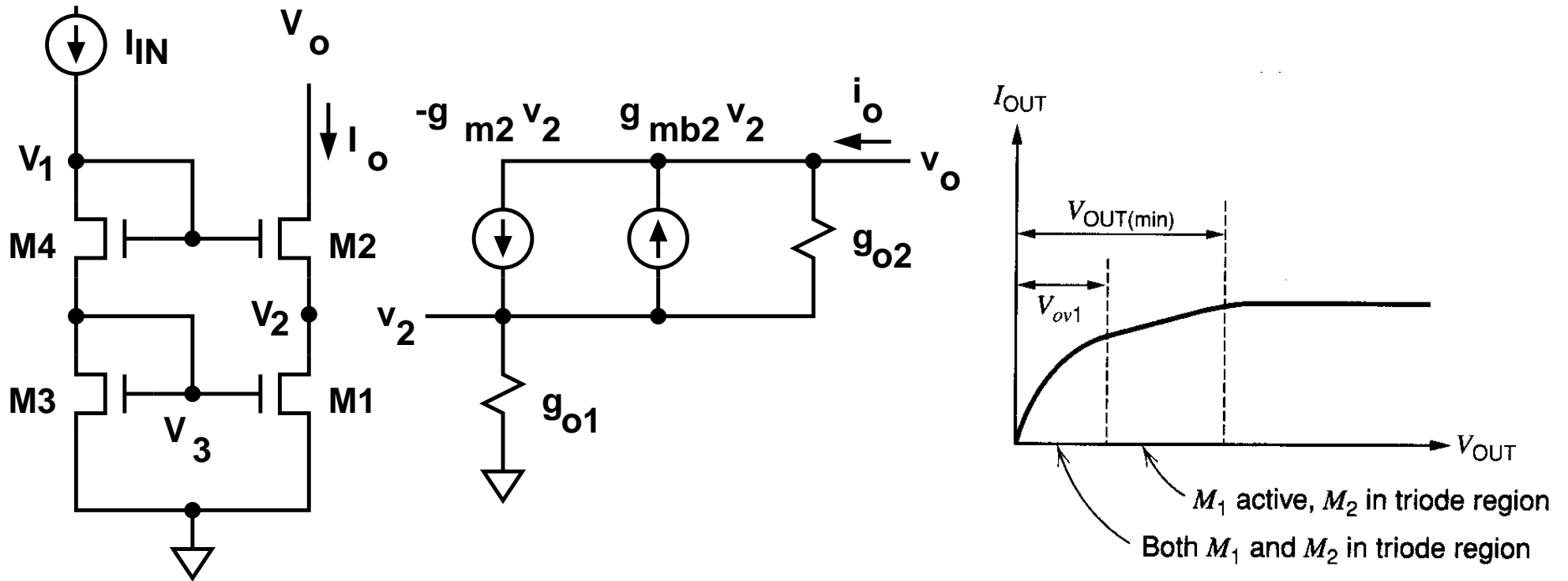
$$I_{IN} = I_{C4} + I_{B4} + I_{B2} = I_{C3} + I_{B3} + I_{B1} + I_{B2} = I_{C3} + \frac{I_{C3}}{\beta_F} + \frac{I_{C3}}{\beta_F} + \frac{I_{C3}}{\beta_F + 1}$$

Thus

$$I_{C2} = I_{C3} \frac{\beta_F}{\beta_F + 1} = I_{IN} \cdot \frac{\beta_F}{\beta_F + 1} \cdot \frac{1}{1 + \frac{2}{\beta_F} + \frac{1}{\beta_F + 1}} = I_{IN} \cdot \left( 1 - \frac{4\beta_F + 2}{\beta_F^2 + 4\beta_F + 2} \right)$$

$$I_{C2} = I_{IN}(1 + \epsilon) \quad \Rightarrow \quad \epsilon = -\frac{4\beta_F + 2}{\beta_F^2 + 4\beta_F + 2} \approx -\frac{4}{\beta_F + 4}$$

# MOST Cascode Current Mirror



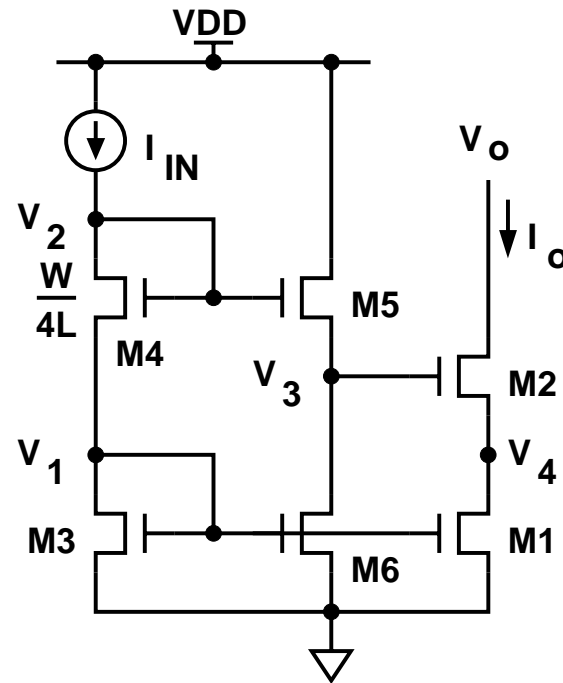
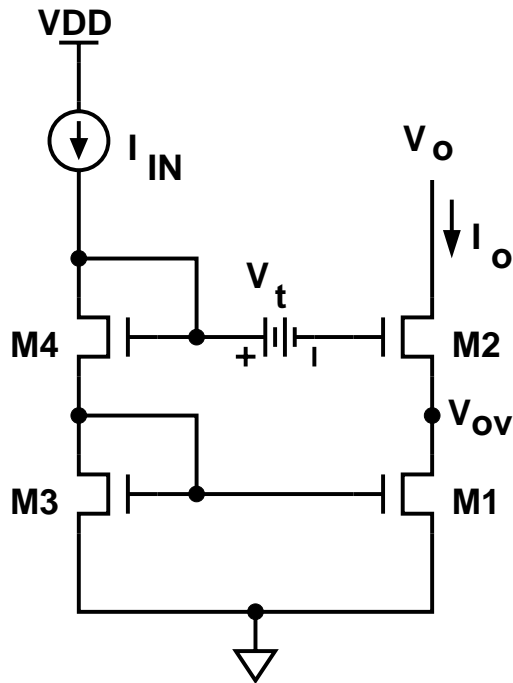
$$R_o = r_{o1}r_{o2}(g_{m2} + g_{mb2} + g_{o1} + g_{o2}) \approx r_{o1}r_{o2}g_{m2}(1 + \chi_2)$$

$$V_{o(min)} = V_{DS1} + V_{DSAT2} = V_{t3} + V_{ov3} + V_{ov2}$$

$$V_{DD(min)} = V_{GS3} + V_{GS4} = V_{t3} + V_{t4} + V_{ov3} + V_{ov4}$$

$$\epsilon \approx 0$$

# MOST High-Swing Cascode Current Mirror



$$(W/L)_4 = \frac{1}{4}(W/L)$$

$$\Rightarrow V_{GS4} = V_t + 2V_{ov}$$

$$V_1 = V_t + V_{ov}$$

$$V_2 = 2V_t + 3V_{ov}$$

$$V_3 = V_t + 2V_{ov}$$

$$V_4 = V_{ov}$$

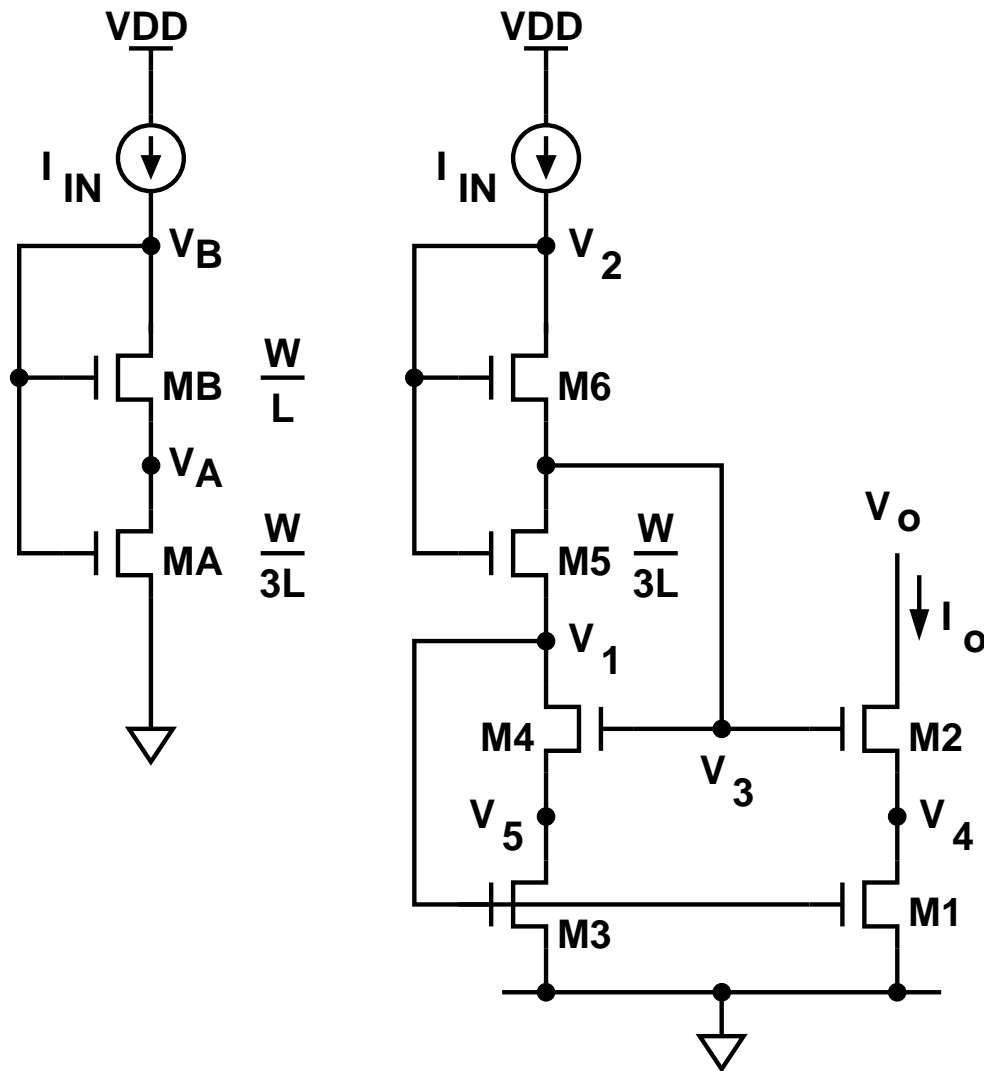
$$V_{o(min)} = V_{DS1} + V_{DSAT2} = 2V_{ov}$$

$$V_{DD(min)} = V_{GS3} + V_{GS4} = 2V_t + 3V_{ov}$$

$$\epsilon \approx \frac{V_{DS1} - V_{DS3}}{V_A} \approx \frac{V_{ov} - (V_t + V_{ov})}{V_A} = -\frac{V_t}{V_A}$$

- In practice, select  $(W/L)_4 < (1/4)(W/L)$  due to body effect and design margin.

# MOST Sooch Cascode Current Mirror



$$I_{IN} = \frac{1}{2} k' \left( \frac{1W}{4L} \right) (V_B - V_t)^2$$

$$= k' \left( \frac{1W}{3L} \right) [(V_B - V_t)V_A - 2V_A^2]$$

$$\Rightarrow V_B = V_t + 2V_{ov} \quad V_A = V_{ov}$$

$$V_1 = V_t + V_{ov}$$

$$V_2 = 2V_t + 3V_{ov}$$

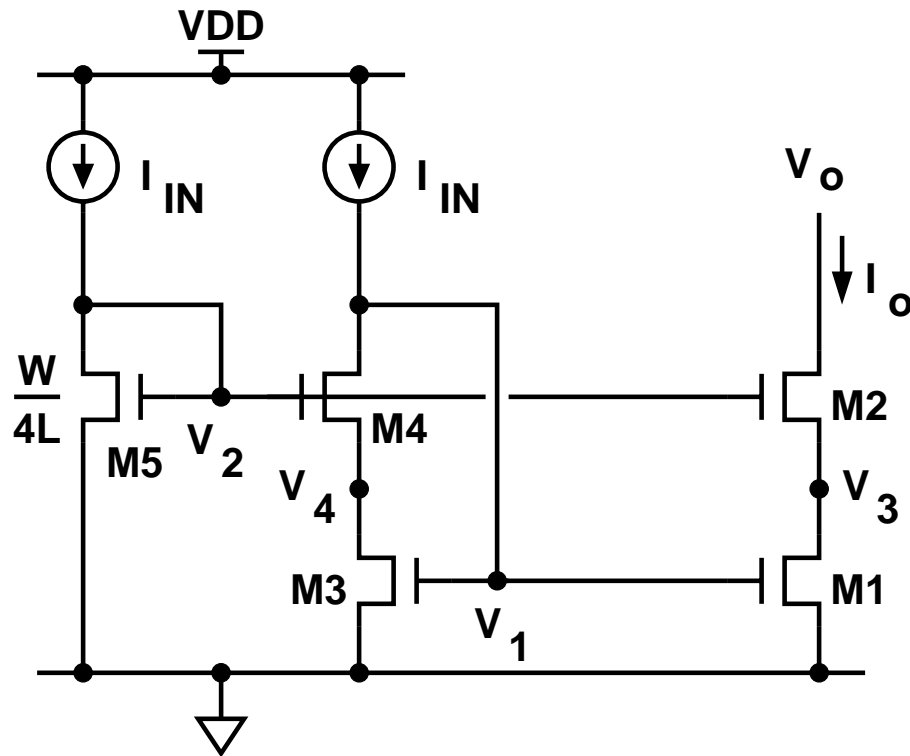
$$V_3 = V_t + 2V_{ov}$$

$$V_4 = V_{ov}$$

$$V_5 = V_{ov}$$

$$V_{o(min)} = V_{DS1} + V_{DSAT2} = 2V_{ov} \quad V_{DD(min)} = V_2 = 2V_t + 3V_{ov} \quad \epsilon = 0$$

# MOST Low-Voltage High-Swing Cascode Current Mirror



$$V_1 = V_t + V_{ov}$$

$$V_2 = V_t + 2V_{ov}$$

$$V_3 = V_{ov}$$

$$V_4 = V_{ov}$$

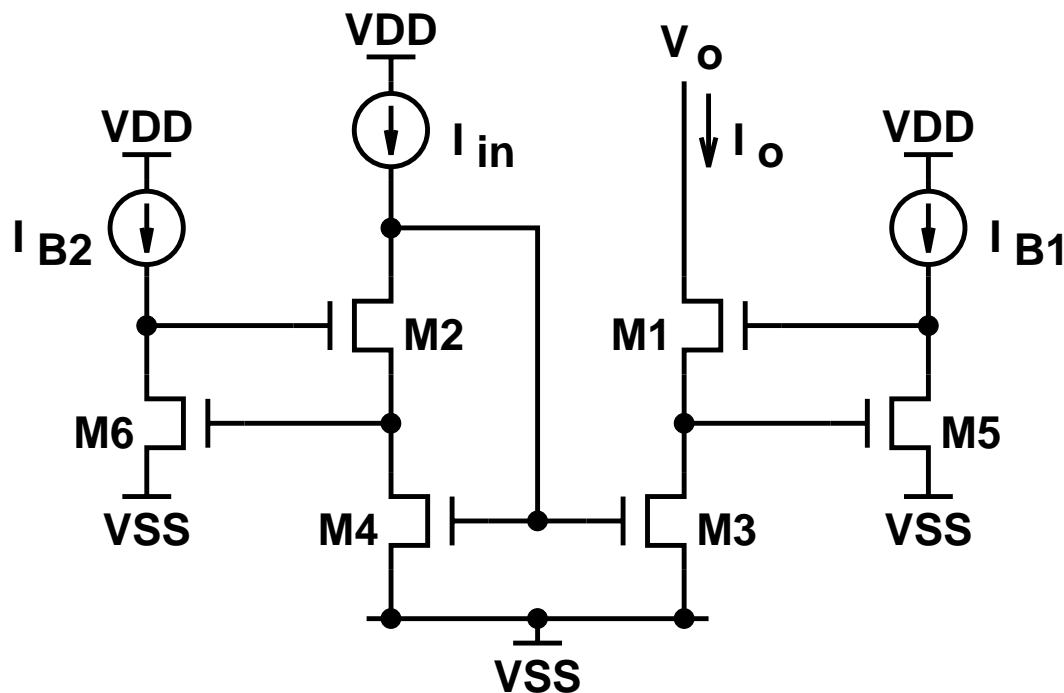
$$V_{o(min)} = V_{DS1} + V_{DSAT2} = 2V_{ov}$$

$$V_{DD(min)} = V_2 = V_t + 2V_{ov}$$

$$\epsilon = 0$$

- In practice, select  $(W/L)_5 < (1/4)(W/L)$  due to body effect and design margin.
- To bias M2 and M4 in the active region, want  $V_2 - V_1 < V_t \Rightarrow V_{ov} < V_t$ .

# Säckinger Current Mirror



$$\text{If } A = \frac{1}{2}g_{m5}r_{o5}$$

$$\Rightarrow R_o \approx \frac{1}{2}g_{m1}g_{m5}r_{o1}r_{o3}r_{o5}$$

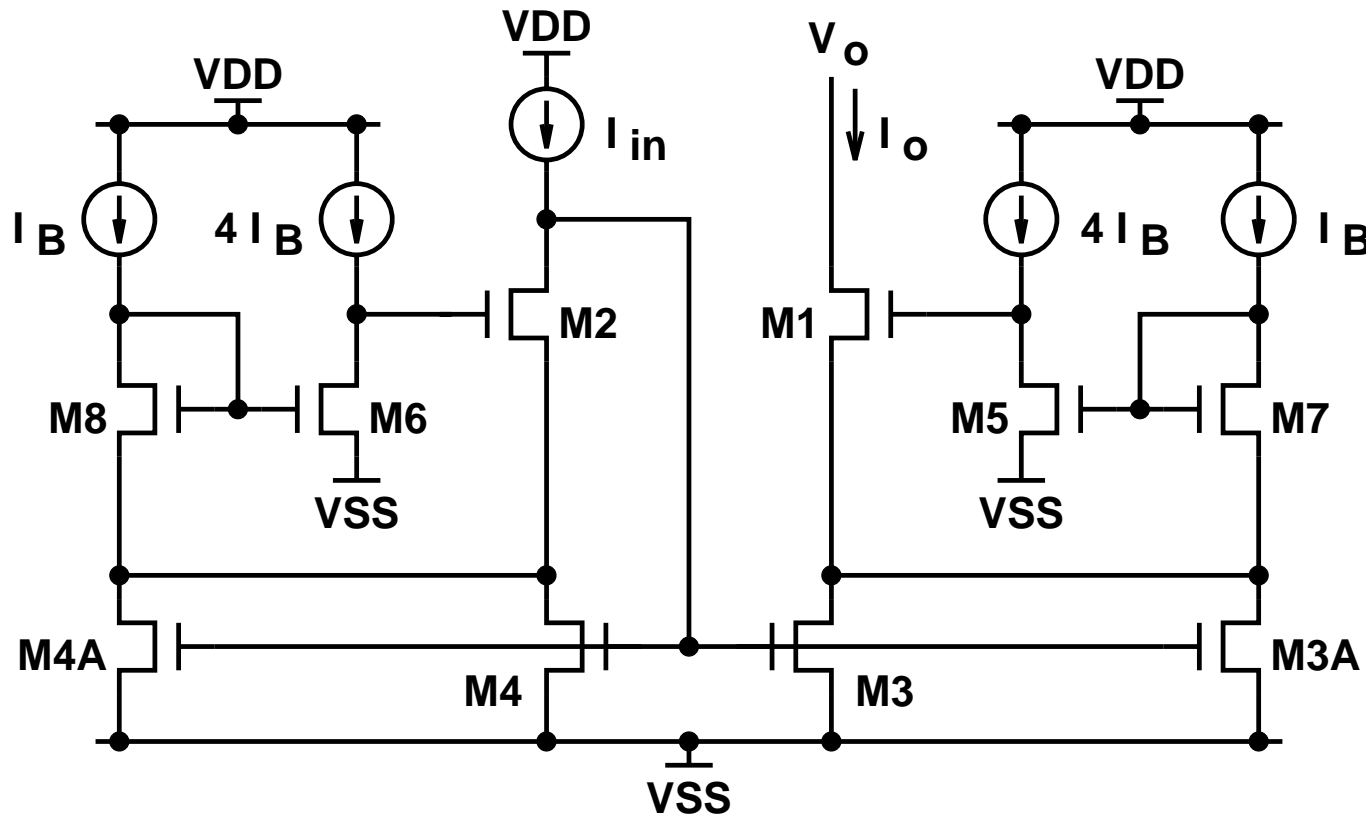
$$V_{o(min)} = V_{GS5} + V_{DSAT1} = V_{ov1} + V_{ov5} + V_t$$

$$V_{DD(min)} = V_{GS5} + V_{VGS1}$$

$$= V_{ov1} + V_{ov5} + 2V_t$$

- It may be necessary to add local compensation capacitors to the enhancement loops to prevent ringing during transients.
- The scheme can substantially slow down the settling times for large-signal transients. A typical settling-time might be increased by 50%.

# Gatti Current Mirror



$$V_{GS5} = V_{ov3} + V_{ov7} + V_t$$

$$\Rightarrow V_{DS3} = V_{ov3}$$

$$V_{o(min)} = V_{DS3} + V_{DSAT1}$$

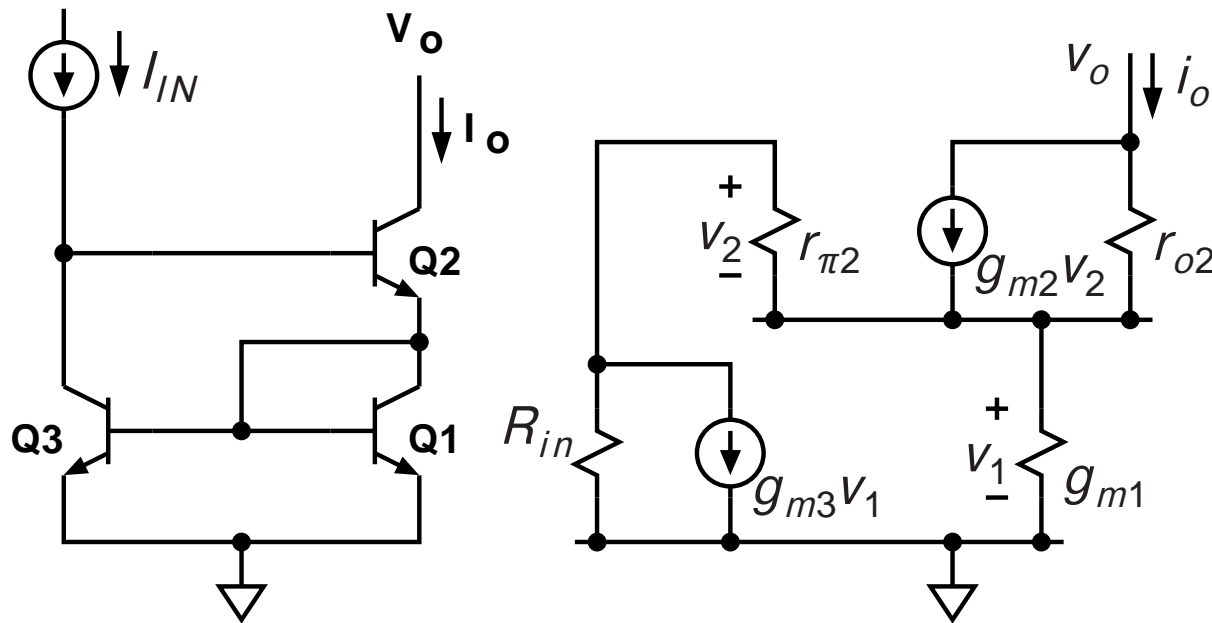
$$= V_{ov1} + V_{ov3}$$

$$V_{DD(min)} = V_{GS5}$$

$$= V_{ov3} + V_{ov7} + V_t$$

- If  $(W/L)_{1,2,3,4} = n \times (W/L)_{5,6,7,8,3A,4A}$ , keep  $I_{in} < nI_B$ .
- M2 can be a fixed-bias cascode. The resulting circuit is less prone to instability.

# BJT Wilson Current Mirror



$$R_o \approx \frac{\beta_{o2}r_{o2}}{2}$$

$$V_{o(min)} = V_{BE1(on)} + V_{CE2(sat)}$$

$$V_{DD(min)} = V_{BE1(on)} + V_{BE2(on)}$$

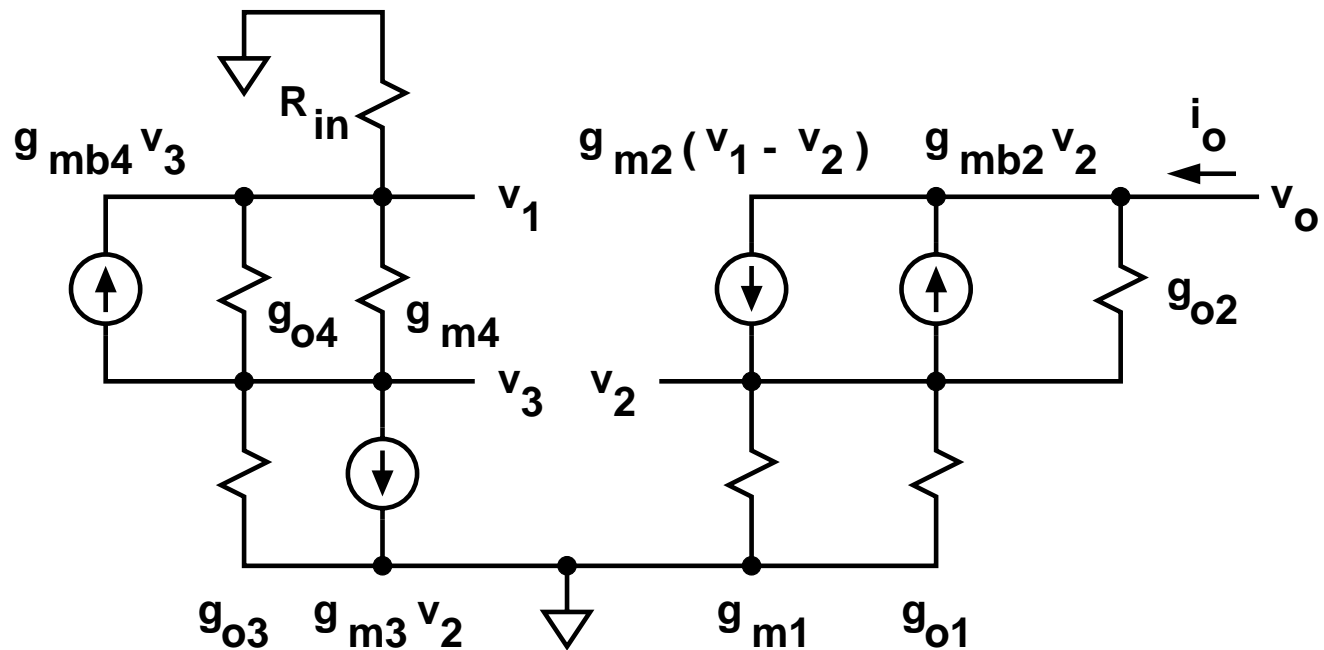
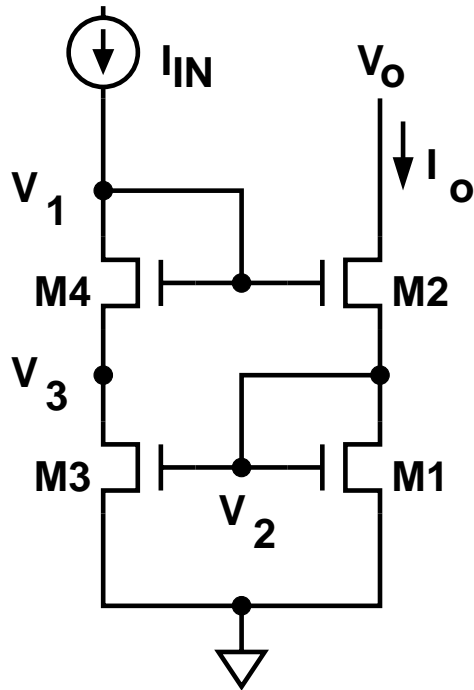
$$\epsilon \approx - \left( -\frac{2}{\beta_F^2 + 2\beta_F + 2} + \frac{V_{BE2}}{V_A} \right)$$

Assume  $Q1=Q2=Q3$ , then  $I_{C1} = I_{C3}$ , and

$$I_{IN} = I_{C3} + \frac{I_{C2}}{\beta_F} = I_{C1} + \frac{I_{C2}}{\beta_F} \quad I_{C2} = -I_{E2} \left( \frac{\beta_F}{\beta_F + 1} \right) = I_{C1} \left( 1 + \frac{2}{\beta_F} \right) \left( \frac{\beta_F}{\beta_F + 1} \right)$$

$$I_O = I_{C2} = I_{IN} \left( 1 - \frac{2}{\beta_F^2 + 2\beta_F + 2} \right) = \frac{I_{IN}}{1 + \frac{2}{\beta_F(\beta_F+2)}}$$

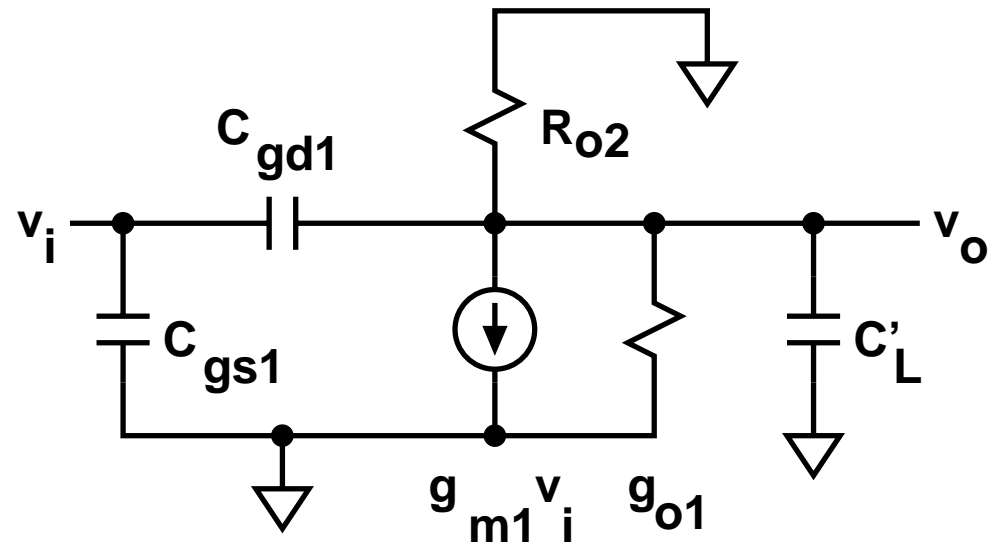
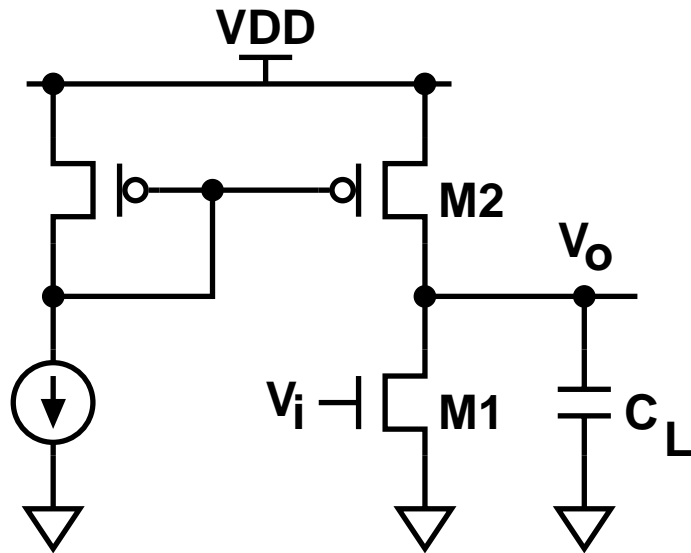
# MOST Wilson Current Mirror



$$R_o \approx r_{o2} \left[ 1 + \frac{g_{m2}}{g_{m1}}(1 + \chi_2) + \frac{g_{m2}}{g_{m1}} \cdot \frac{g_{m3}}{G_{in} + g_{o3} \cdot \frac{G_{in} + g_{m4}}{g_{m4}(1 + \chi_4)}} \right]$$

$$\epsilon \approx 0 \quad V_{o(min)} = V_{GS1} + V_{DSAT2} \quad V_{DD(min)} = V_{GS1} + V_{GS2}$$

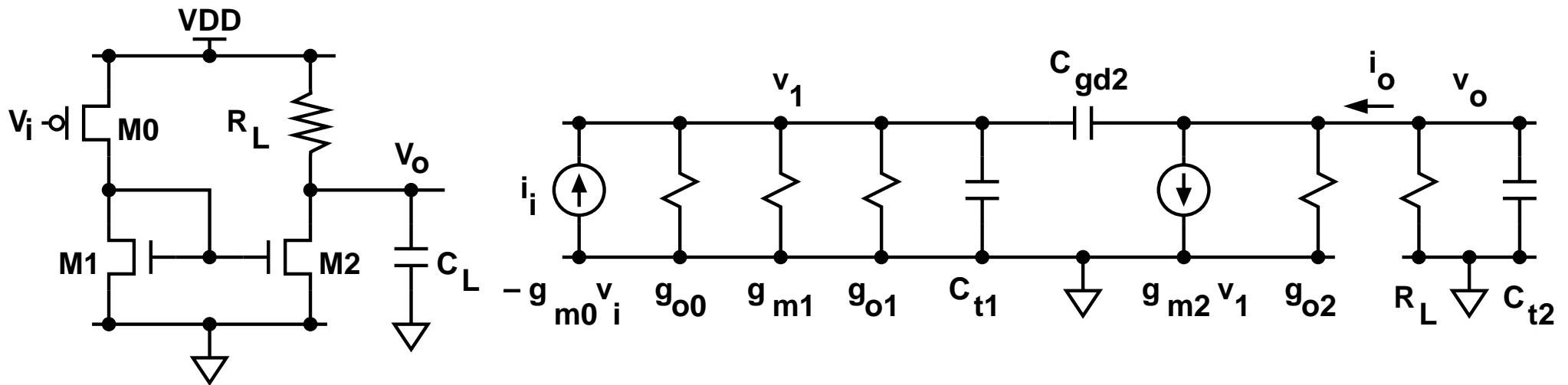
# Complementary Current Source Load



$$G'_L = g_{o1} + G_{o2} \quad C'_L = C_L + C_{o2}$$

- The  $V_o$  range in normal operation is between  $V_{DSAT1}$  and  $V_{DD} - V_{o2(min)}$ .

# Current Mirror Load



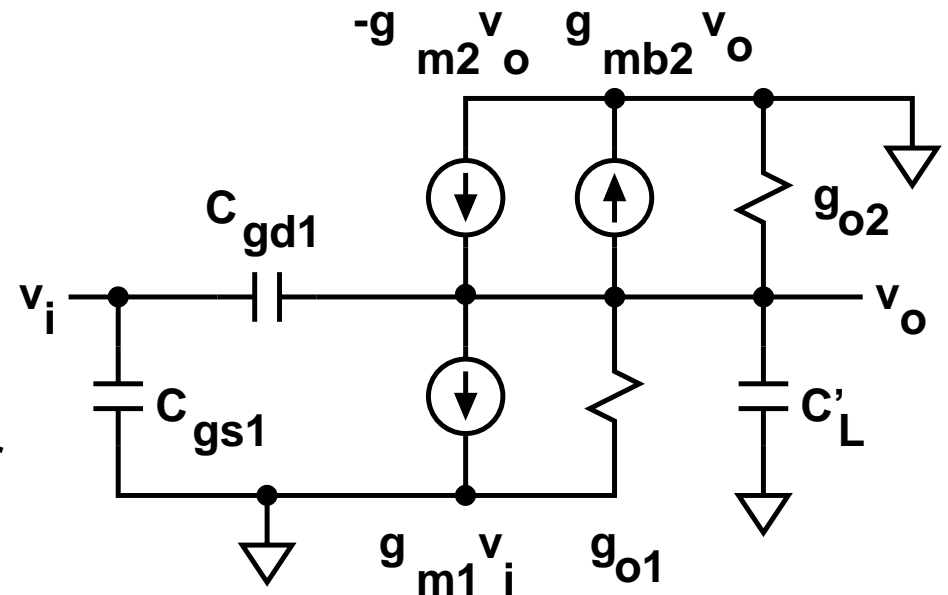
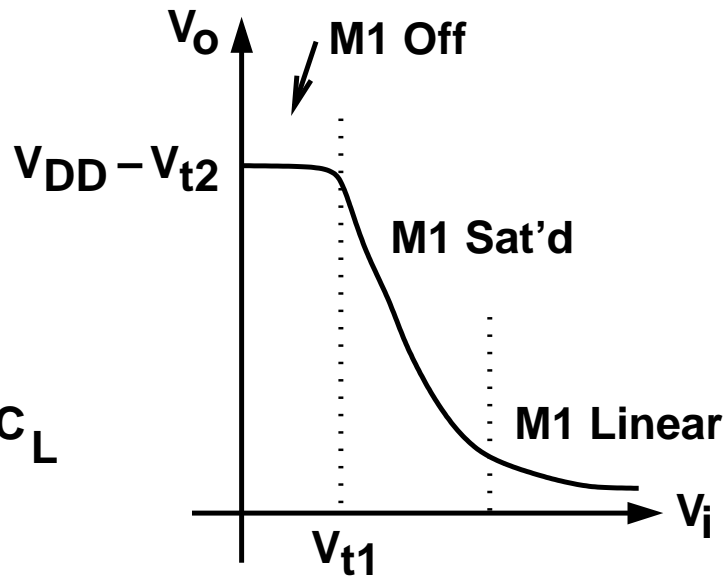
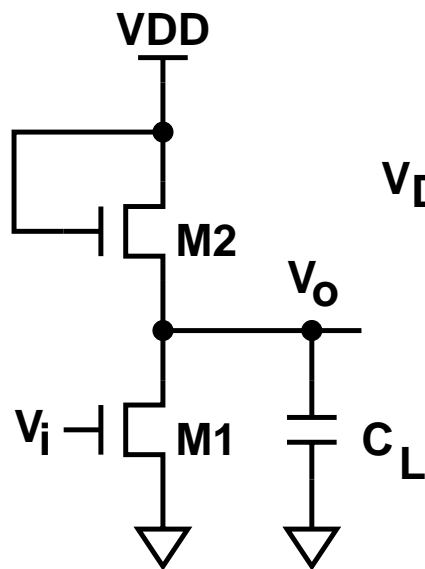
$$G_1 = g_{m1} + g_{o1} + g_{o0} \quad C_{t1} = C_{gs1} + C_{gs2} + C_{db0} + C_{db1} + \dots = KC_{gs1}$$

$$G'_L = g_{o2} + G_L \quad C_{t2} = C_L + C_{db2} + \dots$$

$$\text{Neglect } C_{gd2} \Rightarrow A_I(s) \equiv \left. \frac{i_o}{i_i} \right|_{v_o=0} = \frac{g_{m2}}{G_1 + sC_{t1}} = \frac{A_I(0)}{1 - s/p_1}$$

$$A_I(0) = \frac{g_{m2}}{G_1} = \frac{g_{m2}}{g_{m1}} \cdot \frac{1}{1 + \frac{g_{o1}}{g_{m1}} + \frac{g_{o0}}{g_{m1}}} \quad p_1 = \frac{G_1}{C_{t1}} \approx \frac{g_{m1}}{KC_{gs1}} = \frac{\omega_{T1}}{K}$$

# Diode-Connected Load



$$G'_L = g_{m2} + g_{mb2} + g_{o1} + g_{o2} \quad C'_L = C_L + C_{db1} + C_{gs2} + C'_{sb2}$$

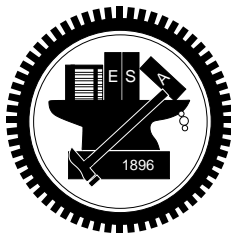
$$A_V(0) = -\frac{g_{m1}}{G'_L} = -\frac{g_{m1}}{g_{m2} + g_{mb2} + g_{o1} + g_{o2}} \approx -\frac{g_{m1}}{g_{m2} + g_{mb2}}$$

$$A_V(0) \approx -\frac{g_{m1}}{g_{m2}} \left( \frac{1}{1 + \chi_2} \right) = -\sqrt{\frac{2k_1 I_{D1}}{2k_2 I_{D2}}} \left( \frac{1}{1 + \chi_2} \right) = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \left( \frac{1}{1 + \chi_2} \right)$$

# Voltage and Current References

Jieh-Tsorng Wu

November 13, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Sensitivity and Temperature Coefficient

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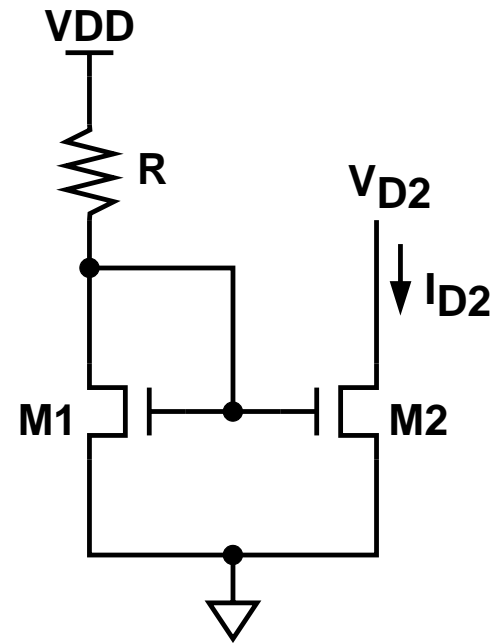
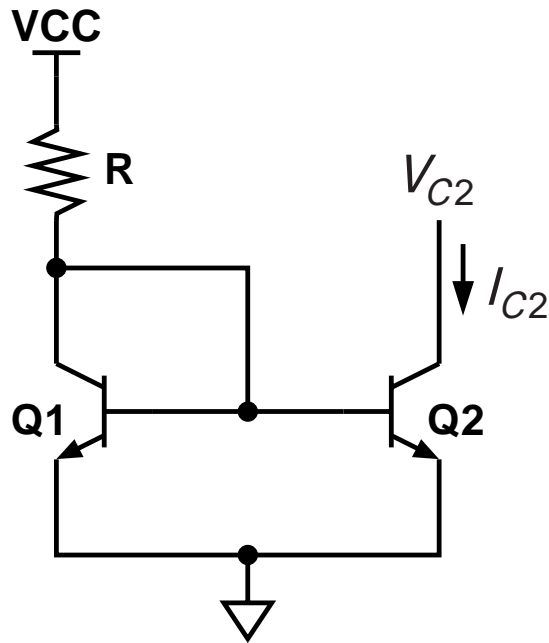
- The *sensitivity* of a parameter  $y$  to a second one  $x$  is defined as

$$S_x^y \equiv \frac{\left(\frac{\Delta y}{y}\right)}{\left(\frac{\Delta x}{x}\right)} = \frac{x}{y} \cdot \frac{\partial y}{\partial x}$$

- The variation of a parameter  $y$  that results from changes in temperature is usually characterized by its *fractional temperature coefficient*, which is defined as the fractional change per degree centigrade change in temperature.

$$TC_y \equiv \frac{\left(\frac{\Delta y}{y}\right)}{\Delta T} = \frac{1}{y} \cdot \frac{\partial y}{\partial T}$$

# Simple Current Sources

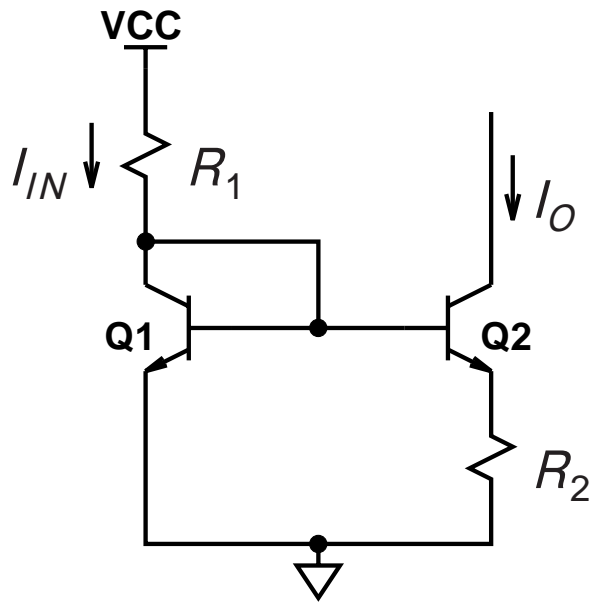


$$I_{C2} \approx I_{C1} \approx \frac{V_{CC} - V_{BE1(on)}}{R} \approx \frac{V_{CC}}{R}$$

$$S_{V_{CC}}^{I_{C2}} = \frac{V_{CC}}{I_{C2}} \cdot \frac{\partial I_{C2}}{\partial V_{CC}} = \frac{V_{CC}}{V_{CC}/R} \cdot \frac{\partial}{\partial V_{CC}} \left( \frac{V_{CC}}{R} \right) = R \cdot \left( \frac{1}{R} \right) = 1$$

$$\frac{\partial I_{C2}}{\partial T} = \frac{1}{R} \frac{\partial V_{CC}}{\partial T} - \frac{V_{CC}}{R^2} \frac{\partial R}{\partial T} = I_{C2} \left( \frac{1}{V_{CC}} \frac{\partial V_{CC}}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T} \right) \Rightarrow TC_{I_{C2}} = TC_{V_{CC}} - TC_R$$

# BJT Widlar Current Source



Let  $\beta_F \rightarrow \infty$  and  $V_A \rightarrow \infty$ ,

$$I_{IN} \approx \frac{V_{CC} - V_{BE1}}{R_1} \approx \frac{V_{CC}}{R_1} \quad S_{V_{CC}}^{I_{IN}} \approx 1$$

$$U_T \ln \frac{I_{IN}}{I_{S1}} = U_T \ln \frac{I_O}{I_{S2}} + I_O R_2 \Rightarrow U_T \ln \left( \frac{I_{IN}}{I_O} \cdot \frac{I_{S2}}{I_{S1}} \right) = I_O R_2$$

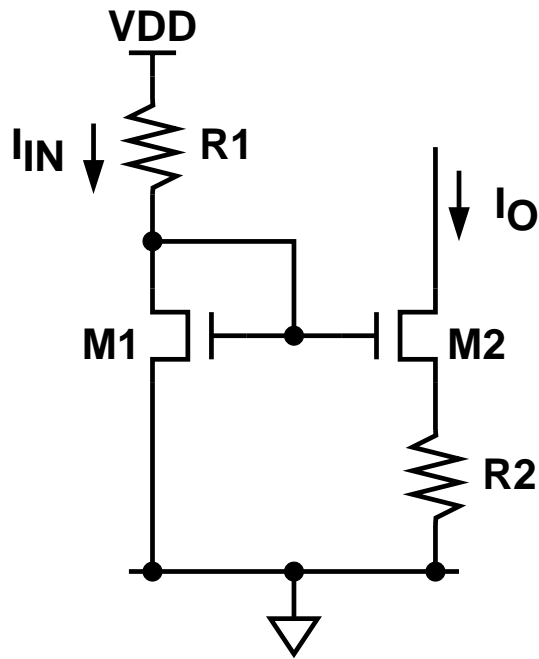
$$\text{If } I_{S1} = I_{S2} \Rightarrow U_T \ln \frac{I_{IN}}{I_O} = I_O R_2$$

Differentiating both sides of the above equation with respect to  $V_{CC}$ ,

$$U_T \frac{I_O}{I_{IN}} \left( \frac{1}{I_O} \frac{\partial I_{IN}}{\partial V_{CC}} - \frac{I_{IN}}{I_O^2} \frac{\partial I_O}{\partial V_{CC}} \right) = R_2 \frac{\partial I_O}{\partial V_{CC}} \Rightarrow \frac{\partial I_O}{\partial V_{CC}} = \left( \frac{1}{1 + \frac{I_O R_2}{U_T}} \right) \frac{I_O}{I_{IN}} \frac{\partial I_{IN}}{\partial V_{CC}}$$

$$S_{V_{CC}}^{I_O} = \frac{V_{CC}}{I_O} \frac{\partial I_O}{\partial V_{CC}} = \left( \frac{1}{1 + \frac{I_O R_2}{U_T}} \right) \frac{V_{CC}}{I_{IN}} \frac{\partial I_{IN}}{\partial V_{CC}} = \left( \frac{1}{1 + \frac{I_O R_2}{U_T}} \right) S_{V_{CC}}^{I_{IN}} \approx \frac{1}{1 + \frac{I_O R_2}{U_T}}$$

# MOST Widlar Current Source



Let  $V_A \rightarrow \infty$  and  $\gamma \rightarrow 0$ ,

$$I_{IN} = \frac{V_{DD} - V_{ov1} - V_t}{R_1} = \frac{1}{2} k' \left( \frac{W}{L} \right)_1 V_{ov1}^2 \quad V_{ov1} = \sqrt{\frac{2I_{IN}}{k'(W/L)_1}}$$

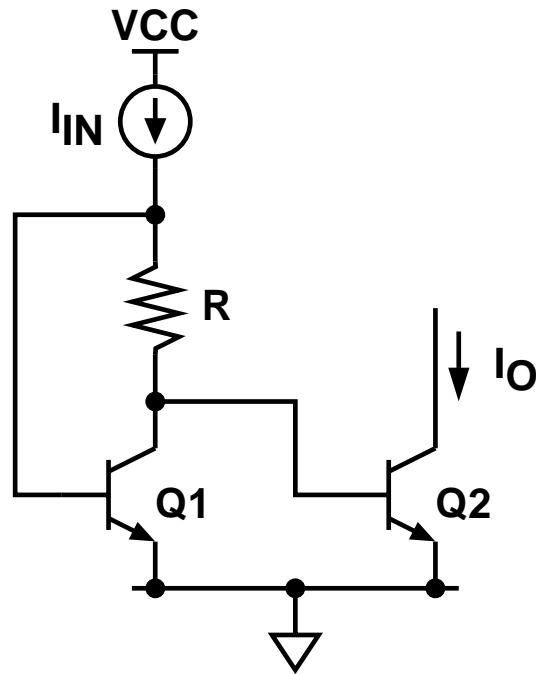
$$V_{ov1} = V_{ov2} + I_O R_2 \Rightarrow I_O R_2 + \sqrt{\frac{2I_O}{k'(W/L)_2}} - V_{ov1} = 0$$

$$\sqrt{I_O} = \frac{1}{2R_2} \left( -\sqrt{\frac{2}{k'(W/L)_2}} + \sqrt{\frac{2}{k'(W/L)_2} + 4R_2 V_{ov1}} \right)$$

$$\frac{1}{2\sqrt{I_O}} \frac{\partial I_O}{\partial V_{DD}} = \frac{1}{4R_2} \frac{1}{\sqrt{\frac{2}{k'(W/L)_2} + 4R_2 V_{ov1}}} 4R_2 \frac{\partial V_{ov1}}{\partial V_{DD}} \quad \frac{\partial V_{ov1}}{\partial V_{DD}} = \sqrt{\frac{2}{k'(W/L)_1}} \frac{1}{2\sqrt{I_{IN}}} \frac{\partial I_{IN}}{\partial V_{DD}}$$

$$S_{V_{DD}}^{I_O} = \frac{V_{ov1}}{\sqrt{V_{ov2}^2 + 4I_O R_2 V_{ov1}}} S_{V_{DD}}^{I_{IN}} \approx \frac{V_{ov1}}{\sqrt{4V_{ov1}^2}} S_{V_{DD}}^{I_{IN}} = \frac{1}{2} S_{V_{DD}}^{I_{IN}}$$

# BJT Peaking Current Source



Since

$$V_{BE1} - I_{IN}R = V_{BE2}$$

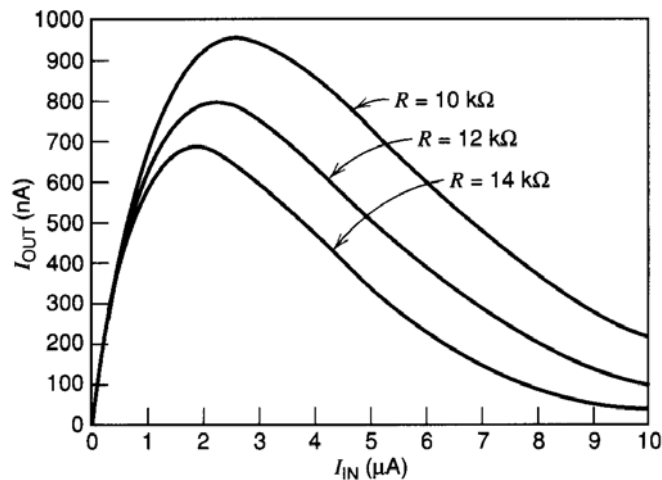
$$U_T \ln \frac{I_{IN}}{I_{S1}} - I_{IN}R = U_T \ln \frac{I_O}{I_{S2}}$$

We have

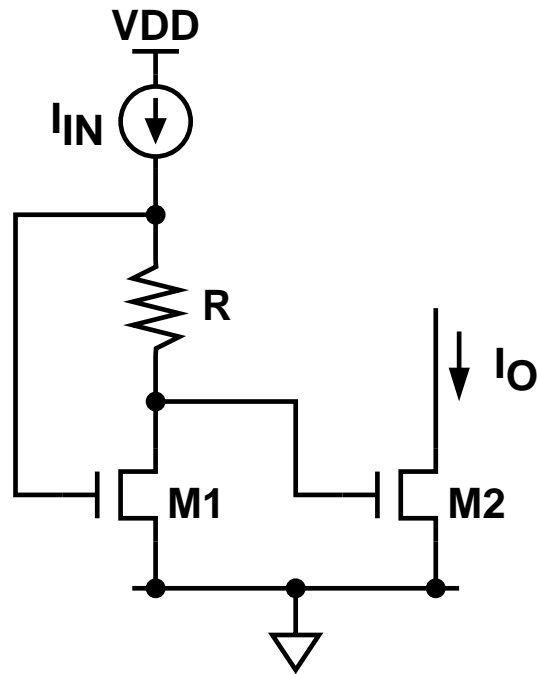
$$U_T \ln \left( \frac{I_{IN}}{I_O} \cdot \frac{I_{S2}}{I_{S1}} \right) = I_{IN}R$$

If  $Q1=Q2$ , then

$$I_O = I_{IN} e^{-I_{IN}R/U_T} \quad R = \frac{U_T}{I_{IN}} \ln \frac{I_{IN}}{I_O}$$



# MOST Peaking Current Source



For M1 and M2 in strong inversion

$$I_O = \frac{1}{2} k' \left( \frac{W}{L} \right)_2 V_{ov2}^2 = \frac{1}{2} k' \left( \frac{W}{L} \right)_2 (V_{o1} - I_{IN} R)^2$$

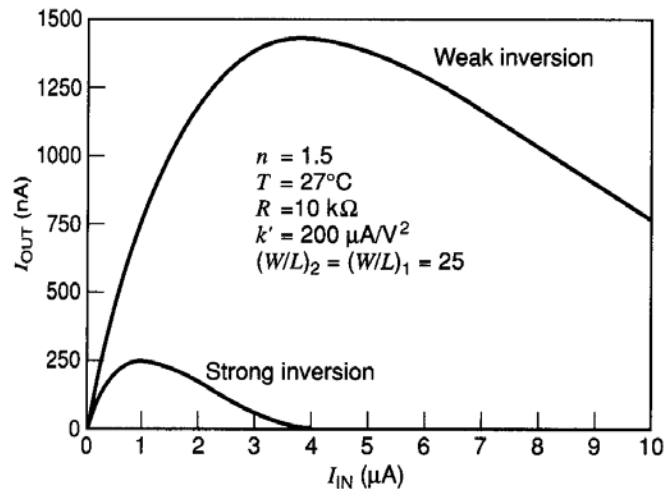
$$V_{ov1} = \sqrt{\frac{2I_{IN}}{k'(W/L)_1}}$$

For M1 and M2 in weak inversion region,

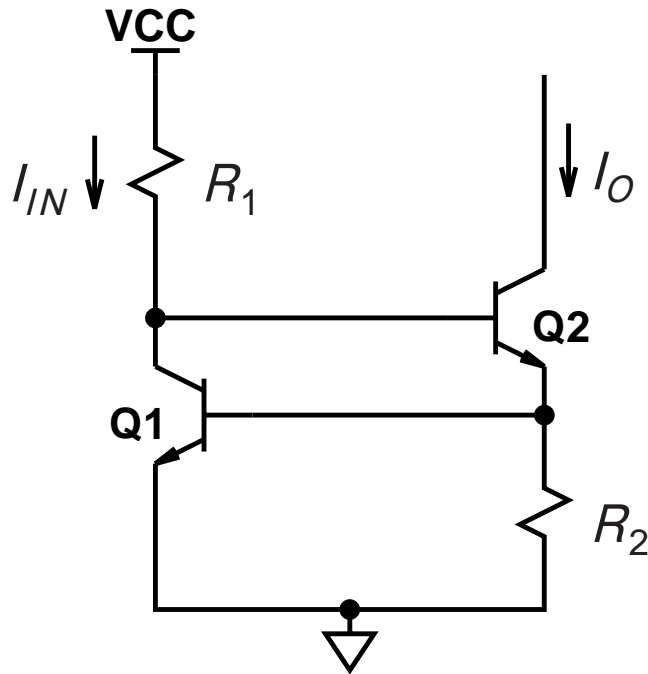
$$V_{GS2} - V_t = nU_T \ln \left( \frac{I_{IN}}{(W/L)_1 I_t} \right) - I_{IN} R$$

If M1=M2,

$$I_O \approx I_t \left( \frac{W}{L} \right)_2 e^{(V_{GS2} - V_t)/(nU_T)} \approx I_{IN} e^{-I_{IN} R / (nU_T)}$$



# BJT $V_{BE}$ Referenced Current Source



$$I_{IN} = \frac{V_{CC} - V_{BE1} - V_{BE2}}{R_1}$$

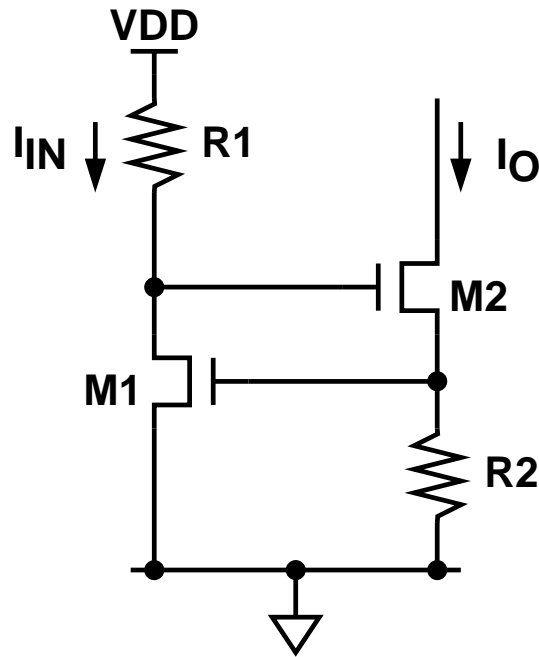
$$V_{BE1} = U_T \ln \frac{I_{IN}}{I_{S1}}$$

$$I_O = \frac{V_{BE1}}{R_2} = \frac{U_T}{R_2} \ln \frac{I_{IN}}{I_{S1}}$$

$$\frac{\partial I_O}{\partial V_{CC}} = \frac{U_T}{R_2} \left( \frac{I_{S1}}{I_{IN}} \right) \left( \frac{1}{I_{S1}} \frac{\partial I_{IN}}{\partial V_{CC}} - \frac{I_{IN}}{I_{S1}^2} \frac{\partial I_{S1}}{\partial V_{CC}} \right) = \frac{U_T}{R_2} \frac{1}{I_{IN}} \frac{\partial I_{IN}}{\partial V_{CC}}$$

$$S_{V_{CC}}^{I_O} = \left( \frac{V_{CC}}{I_O} \right) \frac{\partial I_O}{\partial V_{CC}} = \left( \frac{V_{CC}}{I_O} \right) \frac{U_T}{R_2} \frac{1}{I_{IN}} \frac{\partial I_{IN}}{\partial V_{CC}} = \frac{U_T}{I_O R_2} S_{V_{CC}}^{I_{IN}} = \frac{U_T}{V_{BE1(on)}} S_{V_{CC}}^{I_{IN}}$$

# MOST $V_t$ Referenced Current Source



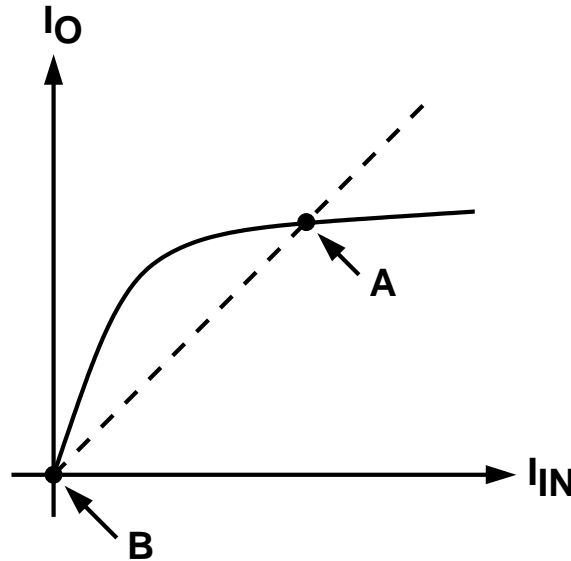
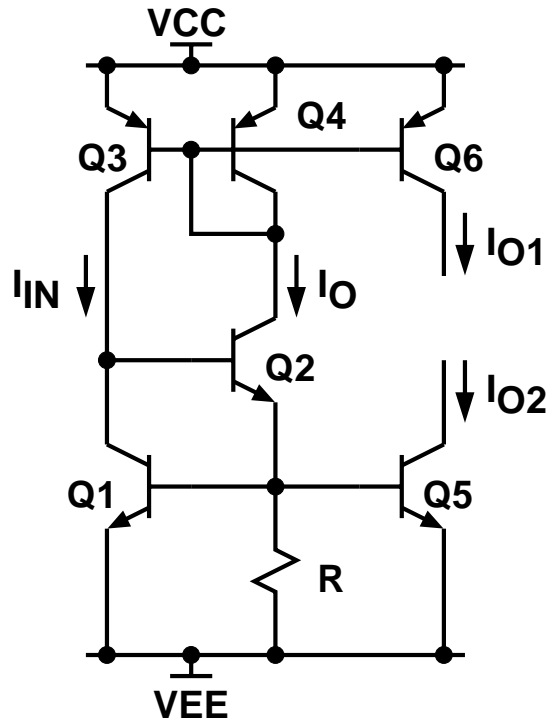
$$I_{IN} = \frac{V_{DD} - V_{GS1} - V_{GS2}}{R_1} = \frac{V_{DD} - V_{ov1} - V_{ov2} - V_{t1} - V_{t2}}{R_1}$$

$$V_{ov1} = \sqrt{\frac{2I_{IN}}{k'(W/L)_1}} \quad V_{ov2} = \sqrt{\frac{2I_O}{k'(W/L)_2}}$$

$$I_O = \frac{V_{GS1}}{R_2} = \frac{V_{t1} + V_{ov1}}{R_2} = \frac{V_{t1} + \sqrt{\frac{2I_{IN}}{k'(W/L)_1}}}{R_2}$$

$$S_{V_{DD}}^{I_O} = \frac{V_{ov1}}{2I_O R_2} S_{V_{DD}}^{I_{IN}} = \frac{V_{ov1}}{2V_{GS1}} S_{V_{DD}}^{I_{IN}}$$

# Self-Biasing BJT $V_{BE}$ Reference



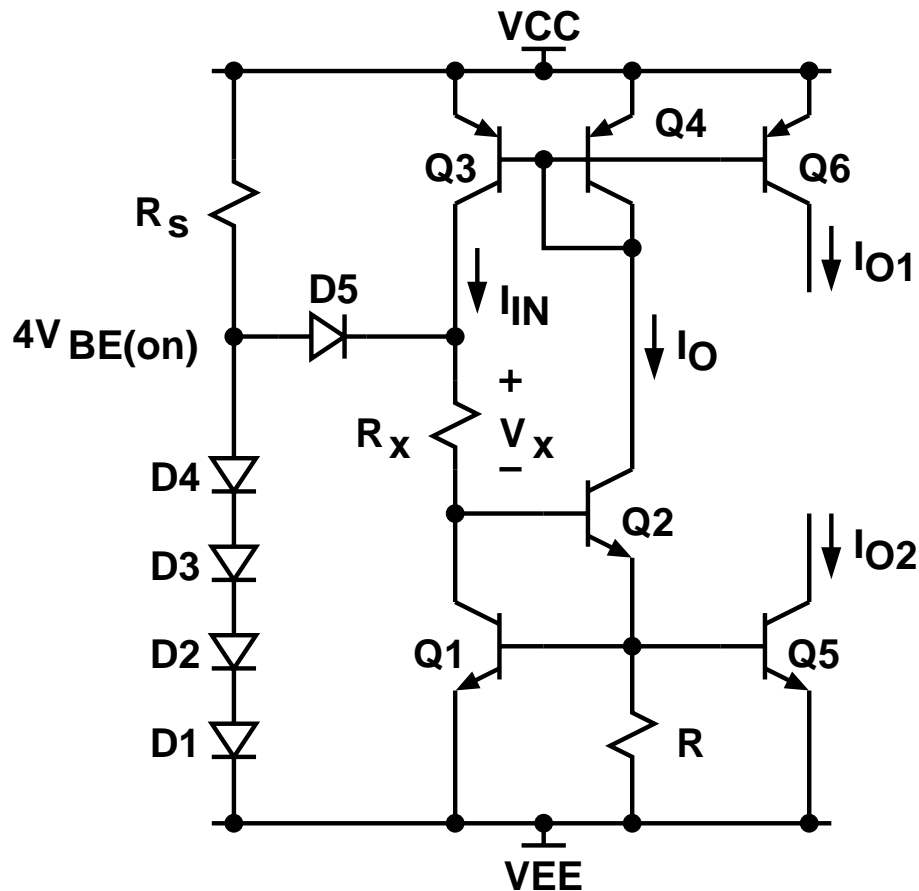
$$I_{IN} \approx I_O \cdot \frac{I_{S3}}{I_{S4}}$$

$$I_O \approx \frac{V_{BE1}}{R} = \frac{U_T}{R} \ln \left( \frac{I_{IN}}{I_{S1}} \right)$$

$$TC_{I_O} = TC_{V_{BE1}} - TC_R$$

- Two possible operating states, A and B. State A is stable and desirable.
- State B, where only leakage currents flow, would normally be unstable. However, it may become stable due to low loop gain under low-current condition.
- There may exist hidden states when the supply is ramping from 0 V.

# Self-Biasing BJT $V_{BE}$ Reference with Start-Up Circuit



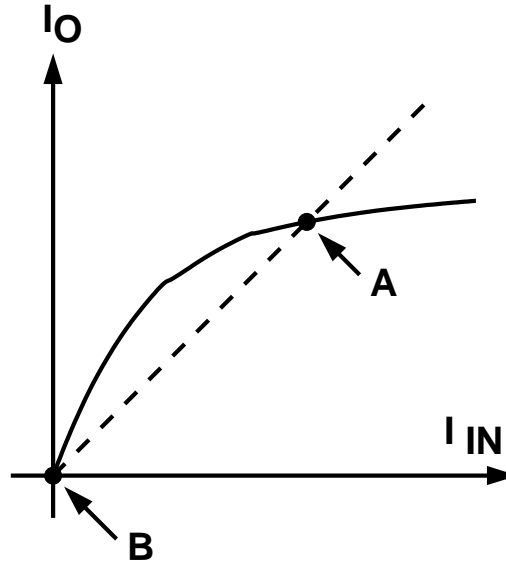
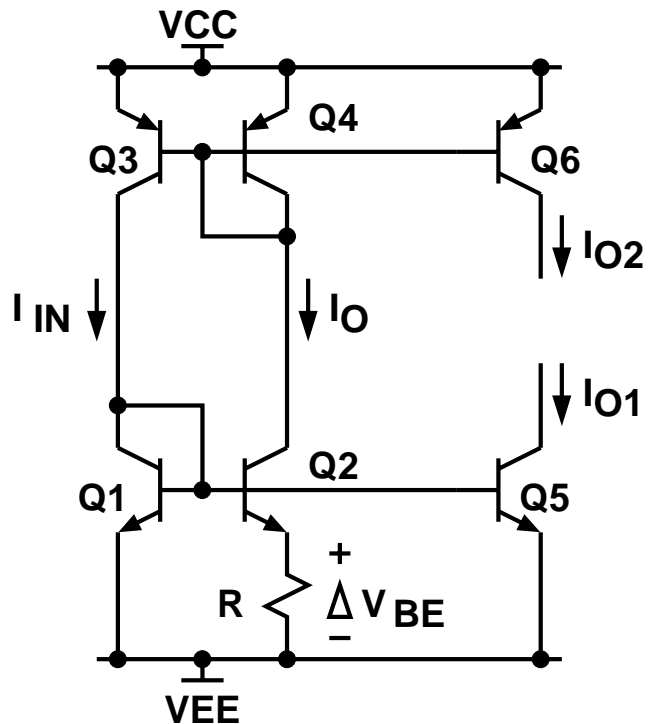
- When in zero-current state (B),  $V_x \approx 0$ , and D5 is forward biased, forcing a current flowing into the self-biasing loop.
- Choose  $R_x$  so that, in State A,

$$V_x = I_{IN} R_x \geq 2V_{BE(on)}$$

Thus, D5 is reversed biased and the start-up circuit won't disturb the self-biasing loop when in State A.

- The start-up circuit may also introduce additional bias points.

# Self-Biasing BJT $U_T$ Reference



$$I_{IN} \approx I_O \cdot \frac{I_{S3}}{I_{S4}}$$

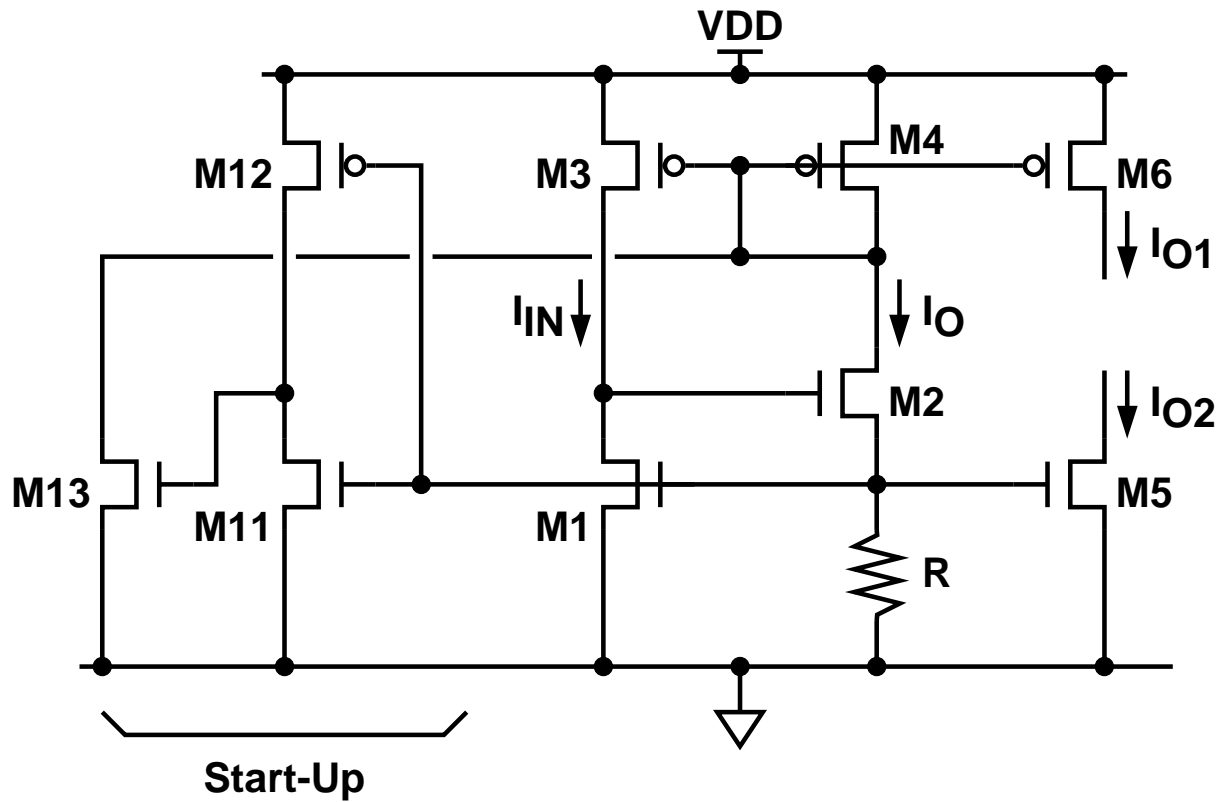
$$U_T \ln \frac{I_{IN}}{I_{S1}} = U_T \ln \frac{I_O}{I_{S2}} + I_O R$$

$$TC_{I_O} = TC_{U_T} - TC_R$$

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = U_T \ln \left( \frac{I_{IN}}{I_O} \cdot \frac{I_{S2}}{I_{S1}} \right) = U_T \ln \left( \frac{I_{S3}}{I_{S4}} \cdot \frac{I_{S2}}{I_{S1}} \right) \quad I_O = \frac{\Delta V_{BE}}{R}$$

- The  $U_T$  reference is a *proportional-to-absolute-temperature* (PTAT) circuit.
- A start-up circuit is required to avoid the “zero-current” state.

# Self-Biasing MOST $V_t$ Referenced Current Source



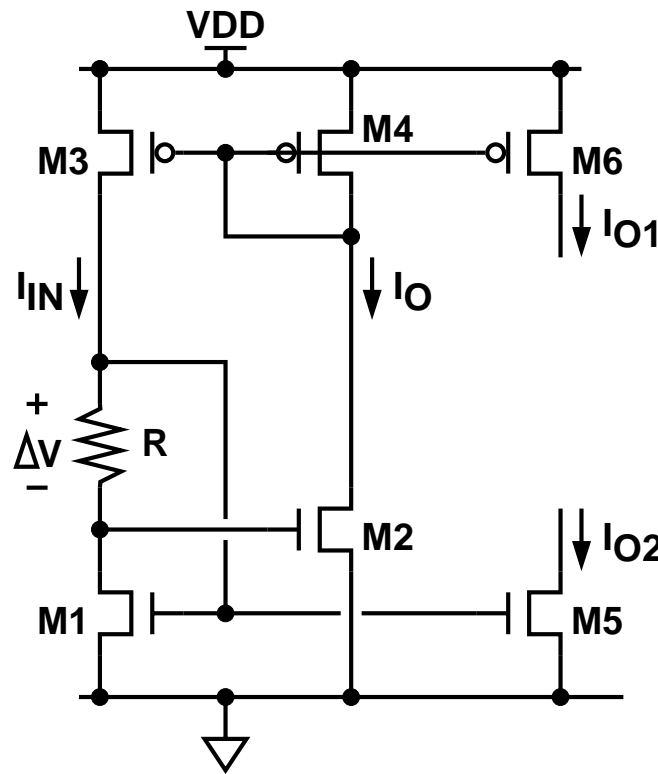
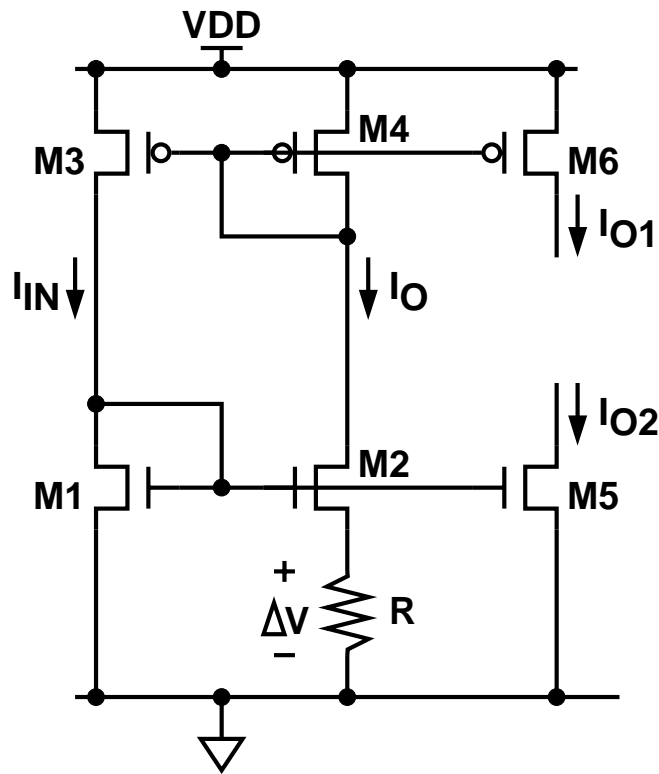
$$V_{ov1} = \sqrt{\frac{2I_{IN}}{k'(W/L)_1}}$$

$$V_{ov2} = \sqrt{\frac{2I_O}{k'(W/L)_2}}$$

$$\frac{I_{IN}}{I_O} = \frac{(W/L)_3}{(W/L)_4}$$

$$I_O = \frac{V_{GS1}}{R} = \frac{V_{t1} + V_{ov1}}{R} = \frac{V_{t1} + \sqrt{\frac{2I_{IN}}{k'(W/L)_1}}}{R} \approx \frac{V_{t1}}{R}$$

# Self-Biasing MOST $g_m$ Referenced Current Source



$$k' = \mu_n C_{ox}$$

$$\alpha \equiv \frac{(W/L)_2}{(W/L)_1} > 1$$

$$\Delta V = I \cdot R$$

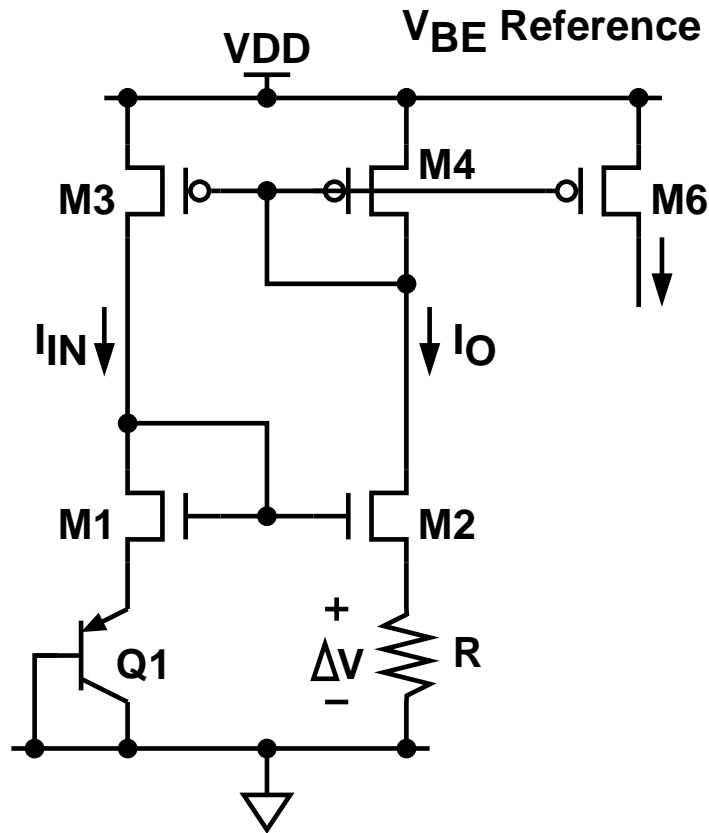
Let  $M3=M4$ , then

$$I_{IN} = I_O = I$$

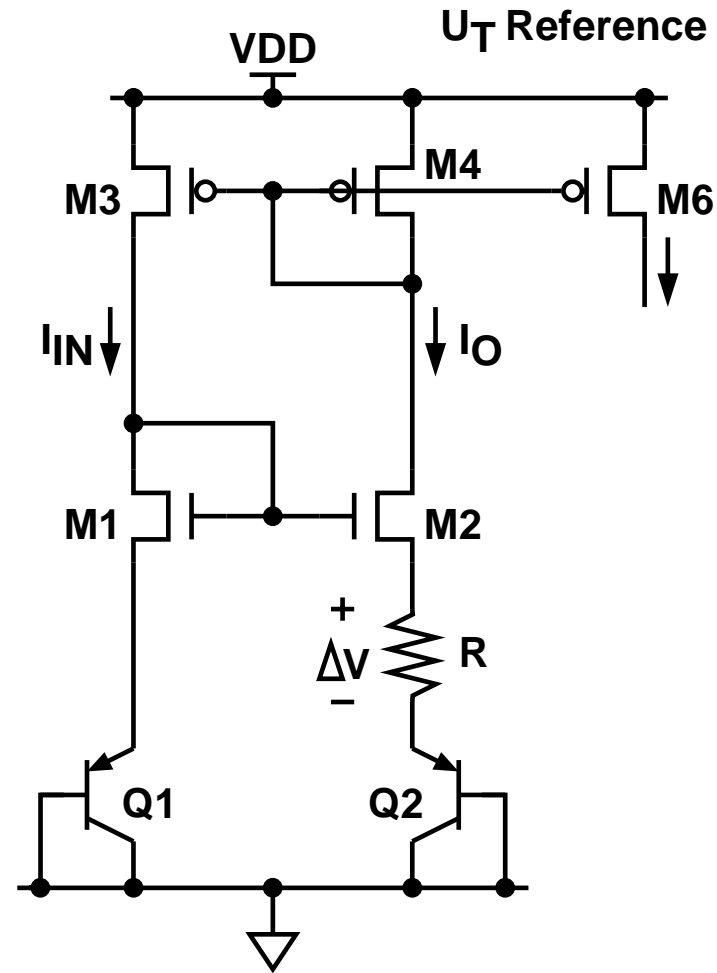
$$I = \frac{1}{2} k' \left( \frac{W}{L} \right)_1 V_{ov1}^2 = \frac{1}{2} k' \left( \frac{W}{L} \right)_2 (V_{ov1} - \Delta V)^2 \Rightarrow V_{ov1} = \frac{\sqrt{\alpha}}{\sqrt{\alpha} - 1} \cdot \Delta V$$

$$I = \frac{\Delta V}{R} = \frac{2(\sqrt{\alpha} - 1)^2}{\alpha} \frac{1}{k'(W/L)_1 R^2} \quad g_{m1} = \frac{2I}{V_{ov1}} = \frac{\Delta V}{R} \cdot \frac{2(\sqrt{\alpha} - 1)}{\sqrt{\alpha} \Delta V} = \frac{2}{R} \frac{\sqrt{\alpha} - 1}{\sqrt{\alpha}}$$

# Self-Biasing MOST $V_{BE}$ and $U_T$ Referenced Current Source

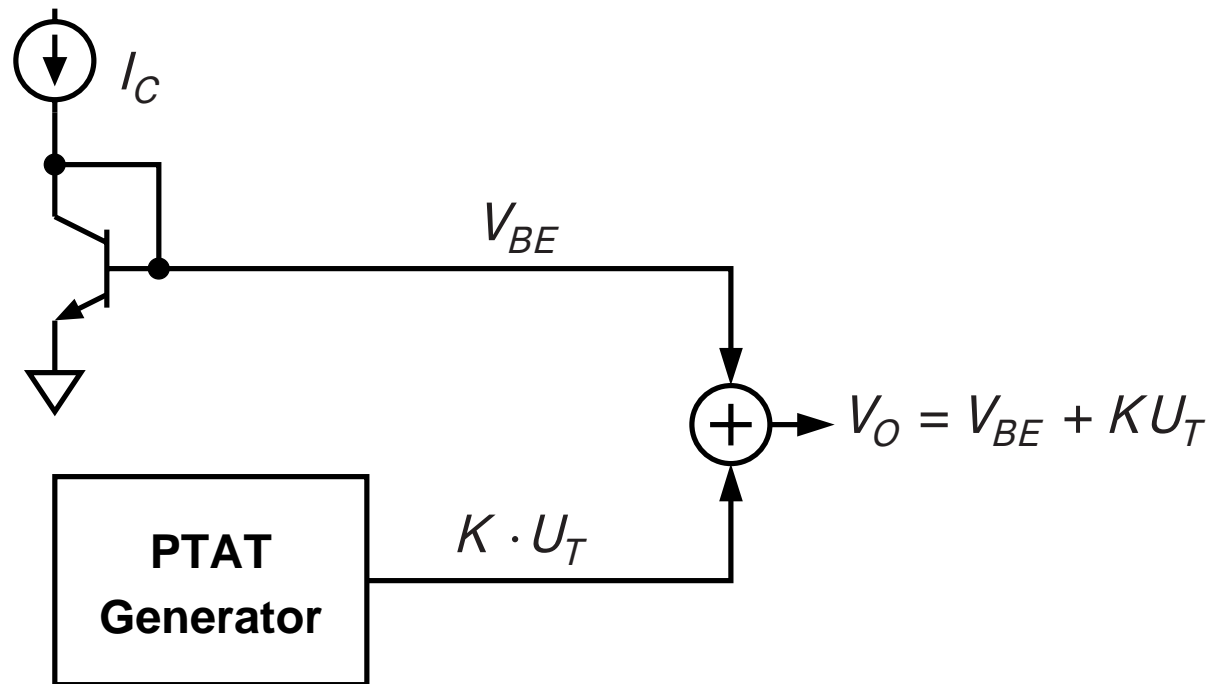


$$\Delta V = V_{BE1}$$



$$\Delta V = U_T \ln \left( \frac{I_{S2}}{I_{S1}} \cdot \frac{(W/L)_3}{(W/L)_4} \right)$$

# Band-Gap References



- $U_T = kT/q = 26 \text{ mV}$  at  $T = 300^\circ\text{K}$ .  $\partial U_T / \partial T = k/q = 0.087 \text{ mV}/^\circ\text{C}$ .
- $V_{BE} = 600 \text{ mV}$  at  $T = 300^\circ\text{K}$ .  $\partial V_{BE} / \partial T \approx -2 \text{ mV}/^\circ\text{C}$ .
- Want  $K = 23$  so that  $\partial V_O / \partial T = 0$  at  $300^\circ\text{K}$  and  $V_O \approx 1.2 \text{ V}$ .

# Band-Gap References

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For a BJT biased in the forward-active region, we have

$$V_{BE} = V_{G0} \left(1 - \frac{T}{T_0}\right) + V_{BE0} \frac{T}{T_0} + mU_T \ln \left(\frac{T_0}{T}\right) + U_T \ln \left(\frac{J_C}{J_{C0}}\right) \quad U_T = \frac{kT}{q}$$

$V_{G0}$  Bandgap voltage of Si extrapolated to 0°K ( $\approx 1.206$  V)

$k$  Boltzmann's constant

$m$  Constant ( $\approx 2.3$ )

$T_0$  Reference temperature

$J_C$  Collector current density ( $= I_C/A_E$ )

$J_{C0}$  Collector current density at  $T_0$

Let

$$V_O = V_{BE} + KU_T \quad \text{and} \quad \frac{J_C}{J_{C0}} = \left(\frac{T}{T_0}\right)^\alpha$$

We have

$$V_O = V_{G0} + \frac{T}{T_0}(V_{BE0} - V_{G0}) + (m - \alpha)U_T \ln \left(\frac{T_0}{T}\right) + K \cdot U_T$$

## Band-Gap References

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Then

$$\frac{\partial V_O}{\partial T} = \frac{1}{T_0}(V_{BE0} - V_{G0}) + (m - \alpha) \frac{k}{q} \left[ \ln \left( \frac{T_0}{T} \right) - 1 \right] + K \cdot \frac{k}{q}$$

Set  $\partial V_O / \partial T = 0$  at  $T = T_0$ , we obtain

$$K = \frac{1}{U_{T0}} \cdot [V_{G0} + (m - \alpha)U_{T0} - V_{BE0}] \quad U_{T0} = \frac{kT_0}{q}$$

$$V_O = V_{G0} + U_T(m - \alpha) \left[ 1 + \ln \left( \frac{T_0}{T} \right) \right] \quad \frac{\partial V_O}{\partial T} = \frac{k}{q}(m - \alpha) \ln \left( \frac{T_0}{T} \right)$$

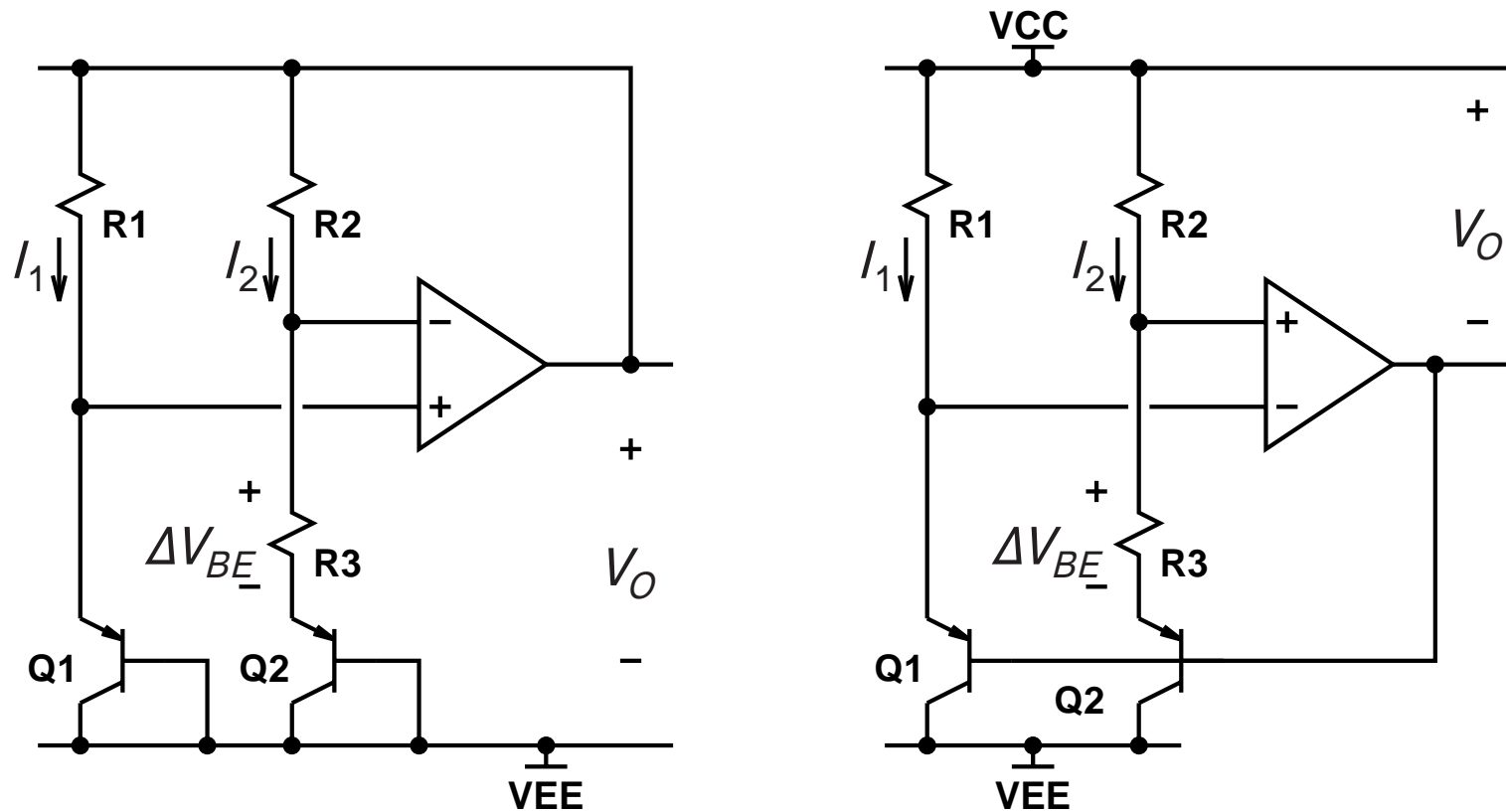
- At  $T = T_0$ ,

$$V_O = V_{G0} + U_{T0}(m - \alpha) \quad \frac{\partial V_O}{\partial T} = 0$$

- If  $T_0 = 300^\circ\text{K}$  and  $\alpha = 1$ , then,

$$K = \frac{1.24 - V_{BE0}}{0.0258} \quad \text{and} \quad V_O = 1.24 \text{ V} \quad \text{at } T = T_0$$

# Kujik Band-Gap References

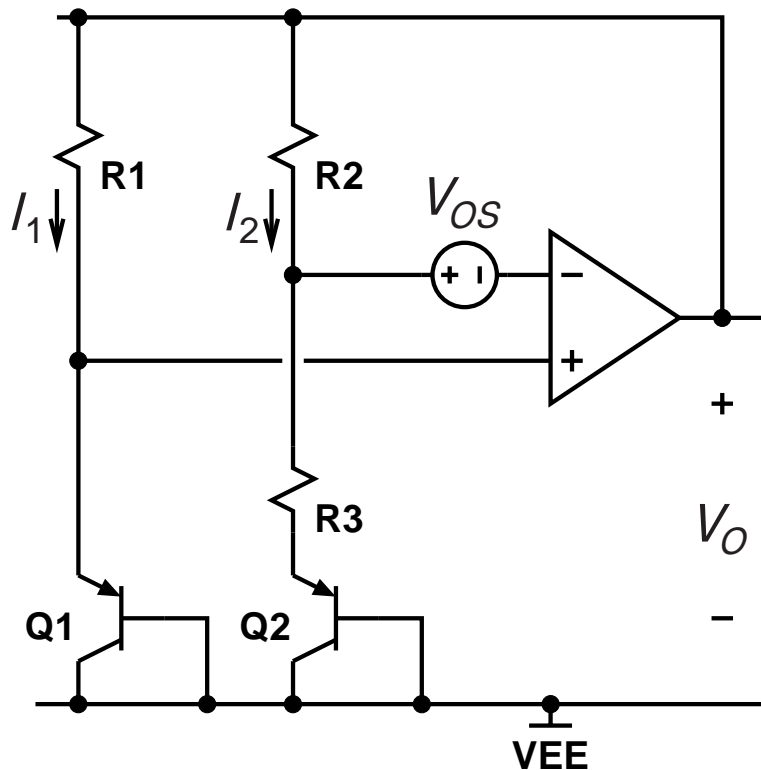


$$\frac{I_1}{I_2} = \frac{R_2}{R_1} \quad V_{R2} = \frac{R_2}{R_3} \Delta V_{BE} \quad \Delta V_{BE} = U_T \ln \left( \frac{I_1}{I_2} \cdot \frac{I_{S2}}{I_{S1}} \right) = U_T \ln \left( \frac{R_2}{R_1} \cdot \frac{I_{S2}}{I_{S1}} \right)$$

$$V_O = |V_{BE1}| + V_{R2} = |V_{BE1}| + \frac{R_2}{R_3} \Delta V_{BE} = |V_{BE1}| + U_T \times \frac{R_2}{R_3} \ln \left( \frac{R_2}{R_1} \cdot \frac{I_{S2}}{I_{S1}} \right)$$

# Kujik Band-Gap References

- Both  $I_{C1}$  and  $I_{C2}$  are proportional to  $T$ .
- In n-well CMOS technologies, use vertical pnp BJTs with with collectors tied to  $V_{SS}$ .
- Reference: Kujik, JSSC 6/73, pp. 222–226.



Let  $V_{OS}$  be the opamp's input offset voltage.

$$V_{R3} = |V_{BE1}| - |V_{BE2}| + V_{OS} = \Delta V_{BE} + V_{OS}$$

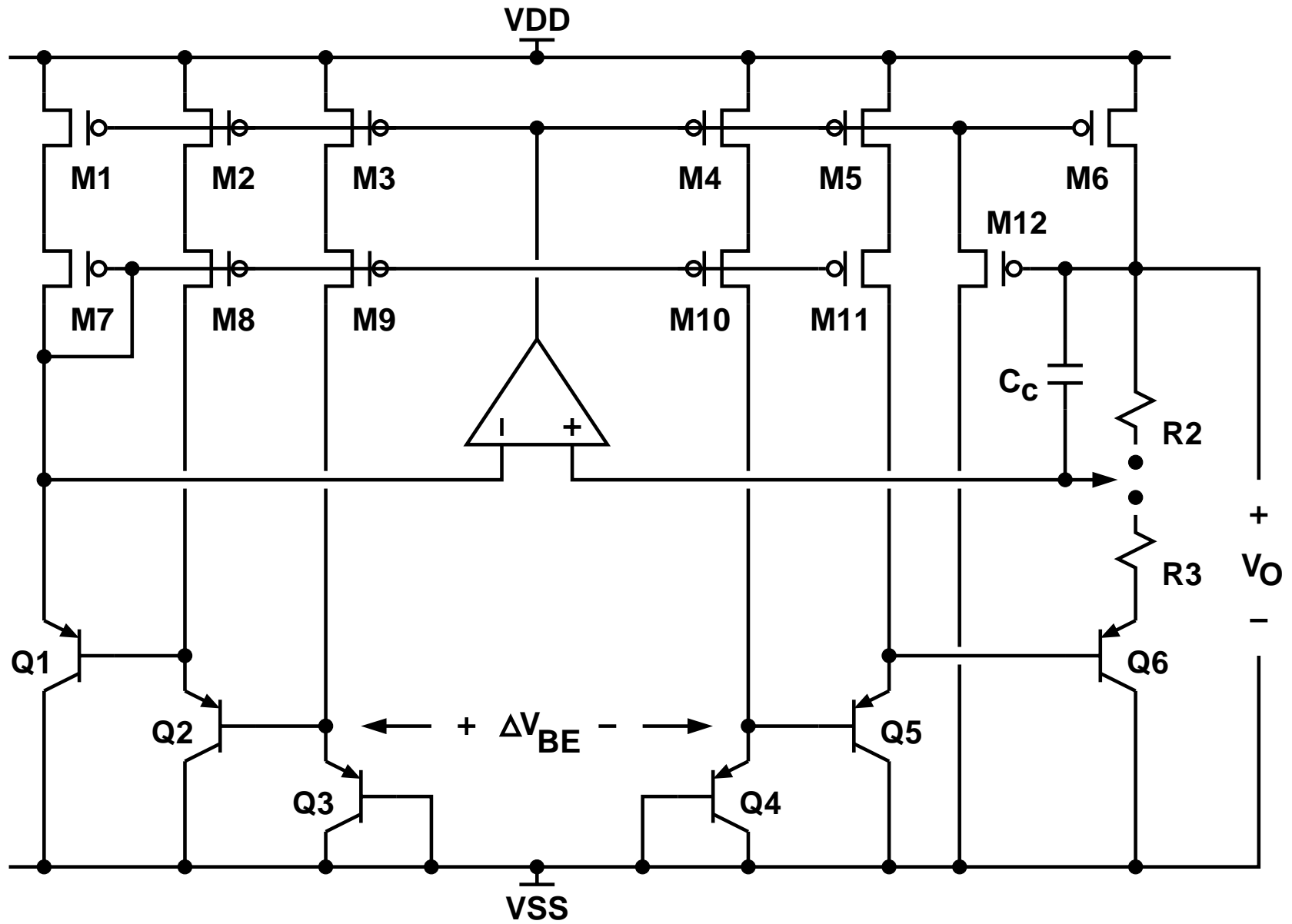
$$V_{R2} = \frac{R_2}{R_3} V_{R3} = \frac{R_2}{R_3} (\Delta V_{BE} + V_{OS})$$

$$V_O = |V_{BE1}| + V_{OS} + V_{R2}$$

$$= |V_{BE1}| + \frac{R_2}{R_3} \Delta V_{BE} + \left(1 + \frac{R_2}{R_3}\right) V_{OS}$$

- The ratio  $R_2/R_3$  is typically  $5 \sim 10$ .

# Ahuja Band-gap Reference



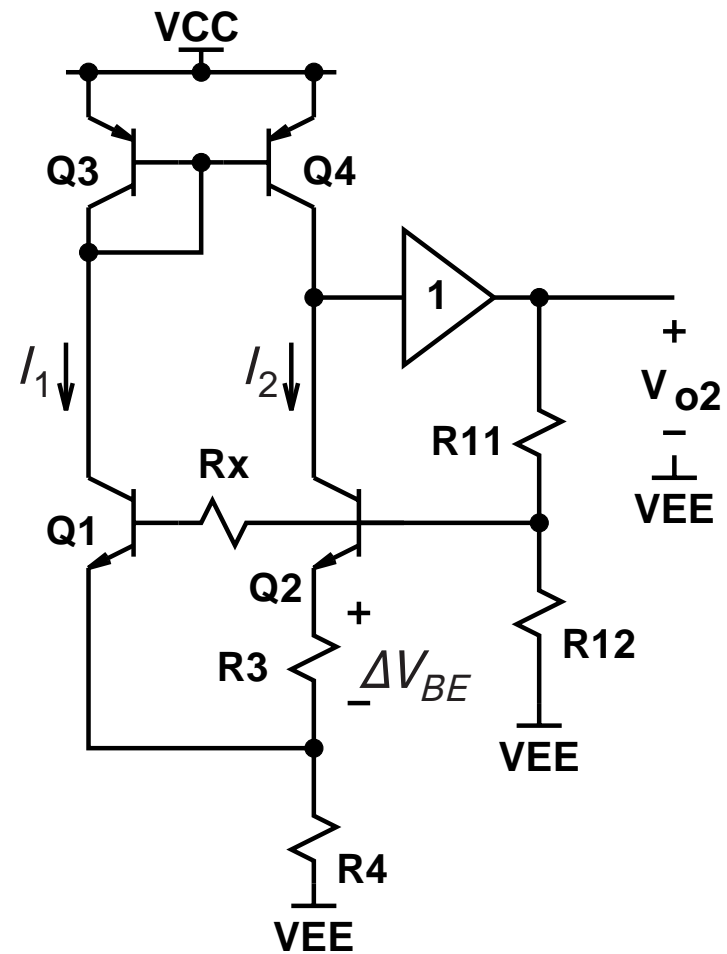
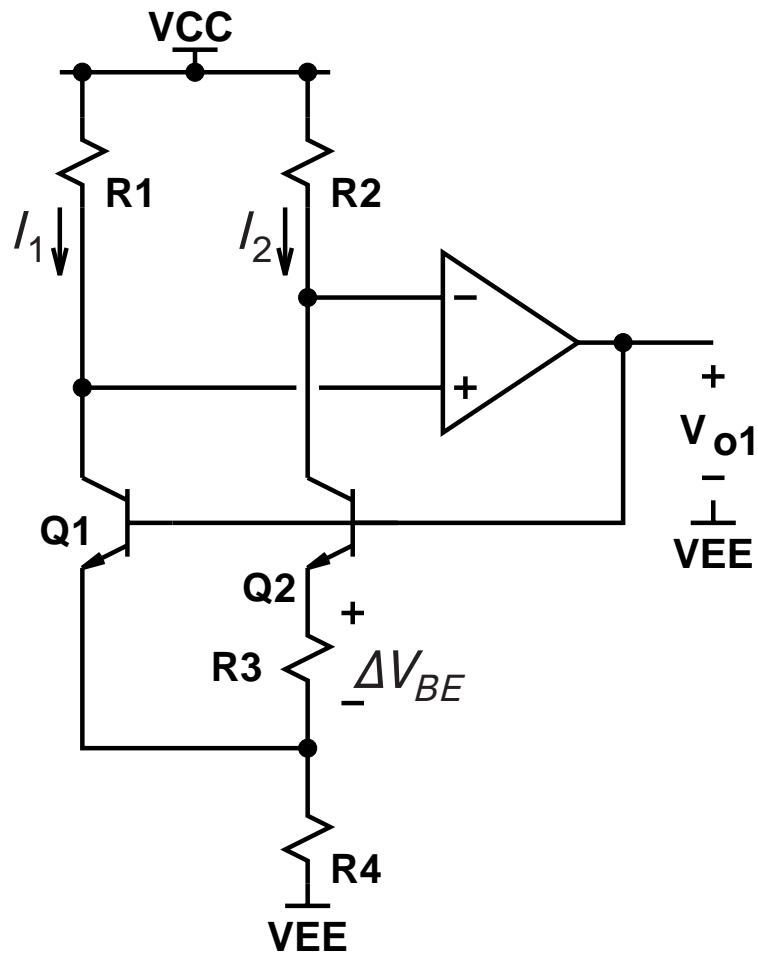
# Ahuja Band-gap Reference

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$$V_O = 3|V_{BE}| + 3\frac{R_2}{R_3}\Delta V_{BE} + \left(1 + \frac{R_2}{R_3}\right)V_{OS}$$

- Increase number of  $V_{BE}$  to suppress the contribution from  $V_{OS}$ .
- Opamp doesn't need to drive resistive load.
- $C_c$  provides a feedforward path for negative feedback to ensure stability.
- Cascode current sources for better current matching.
- M12 is added for auto start-up to avoid the zero-current state.
- Reference: Ahuja, JSSC 12/84, pp. 892–899.

# Brokaw Band-Gap References



$$\beta_F \rightarrow \infty \Rightarrow \frac{I_1}{I_2} = \frac{R_2}{R_1} \quad I_2 = \frac{\Delta V_{BE}}{R_3} \quad \Delta V_{BE} = U_T \ln \left( \frac{I_1}{I_2} \cdot \frac{I_{S2}}{I_{S1}} \right)$$

# Brokaw Band-Gap References

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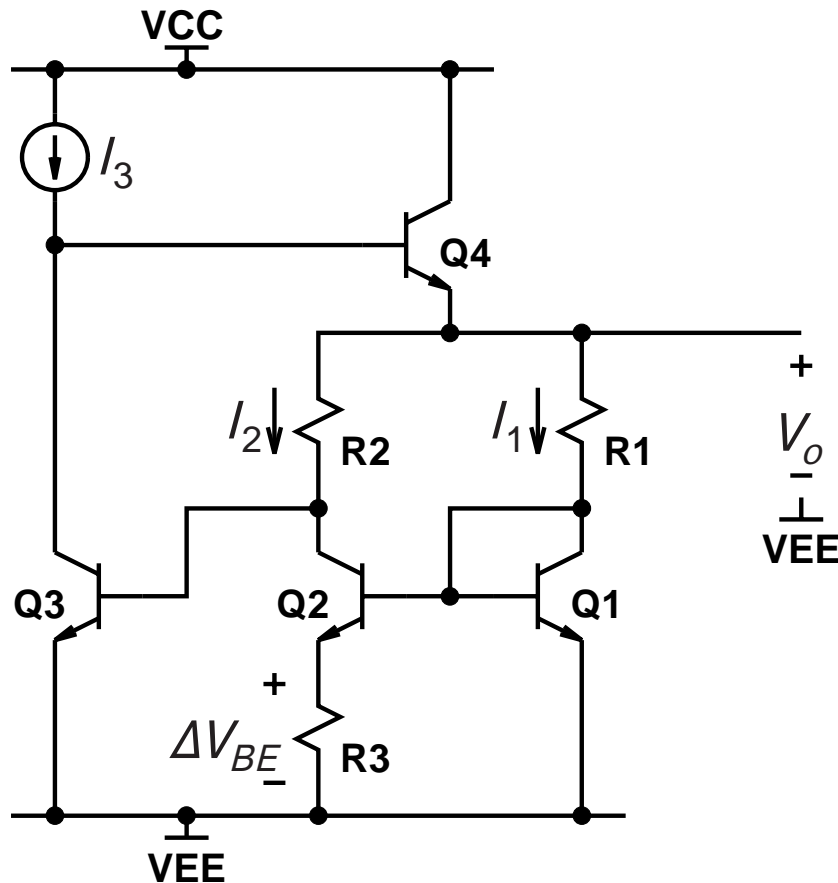
The output voltages are

$$\begin{aligned}V_{O1} &= V_{BE1} + (I_1 + I_2)R_4 = V_{BE1} + \frac{\Delta V_{BE}}{R_3} \left( \frac{I_1}{I_2} + 1 \right) R_4 \\ &= V_{BE1} + U_T \times \frac{R_4}{R_3} \left( \frac{R_2}{R_1} + 1 \right) \ln \left( \frac{R_2}{R_1} \cdot \frac{I_{S2}}{I_{S1}} \right)\end{aligned}$$

$$V_{O2} = \left( 1 + \frac{R_{11}}{R_{12}} \right) \left[ V_{BE1} + U_T \frac{R_4}{R_3} \left( \frac{I_1}{I_2} + 1 \right) \ln \left( \frac{I_1}{I_2} \cdot \frac{I_{S2}}{I_{S1}} \right) \right]$$

- Both  $I_1$  and  $I_2$  are proportional to  $T$ .
- The resistor  $R_x = \left( \frac{R_3}{R_4} R_{11} \right) \parallel R_{12}$  is added to cancel the effects of the finite base currents going through  $R_{11}$ .
- Reference: Brokaw, JSSC 12/74, pp. 388–393.

# Widlar Band-Gap Reference



$$\beta_F \rightarrow \infty \quad \frac{I_1}{I_{S1}} = \frac{I_3}{I_{S3}} \quad V_{BE1} = V_{BE3}$$

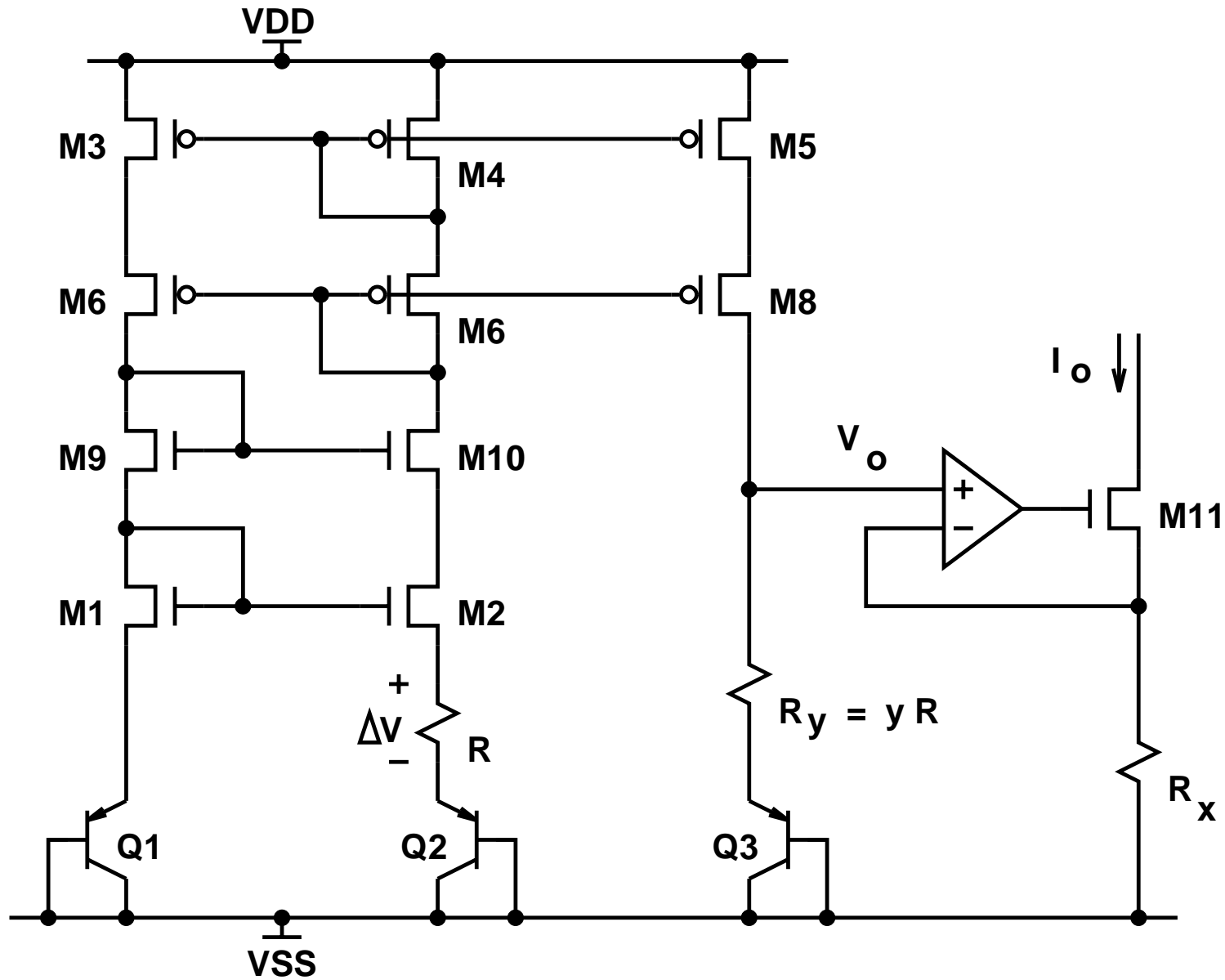
$$\frac{I_1}{I_2} = \frac{R_2}{R_1} \quad \Delta V_{BE} = U_T \ln \frac{I_1 I_{S2}}{I_2 I_{S1}} = U_T \ln \frac{R_2 I_{S2}}{R_1 I_{S1}}$$

$$V_O = V_{BE1} + \frac{R_2}{R_3} \Delta V_{BE}$$

$$= V_{BE1} + U_T \times \frac{R_2}{R_3} \ln \left( \frac{R_2}{R_1} \cdot \frac{I_{S2}}{I_{S1}} \right)$$

- Both  $I_1$  and  $I_2$  are proportional to  $T$ .  $I_3$  can be mirrored from a separate PTAT source.
- In the simplest form,  $I_3$  can be implemented with a resistor.

# Song Band-Gap Reference



# Song Band-Gap Reference

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Let  $Q_2=Q_3$ ,  $I_{S2}/I_{S1} = n$ , and  $M_3=M_4=M_5$ , then

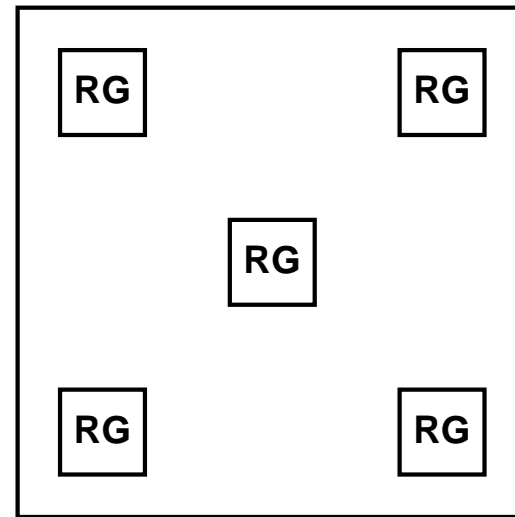
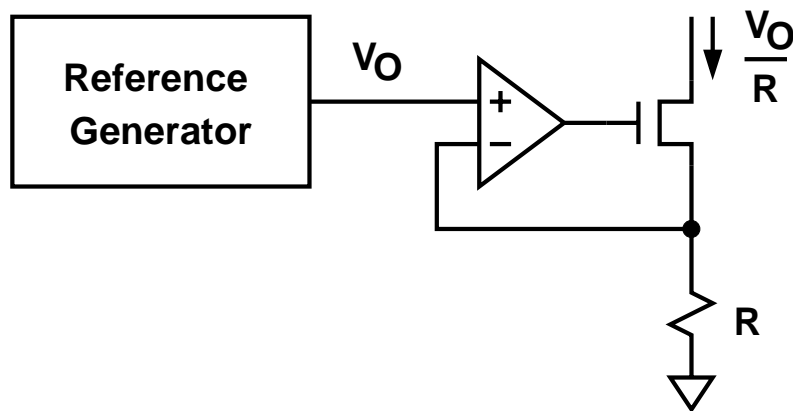
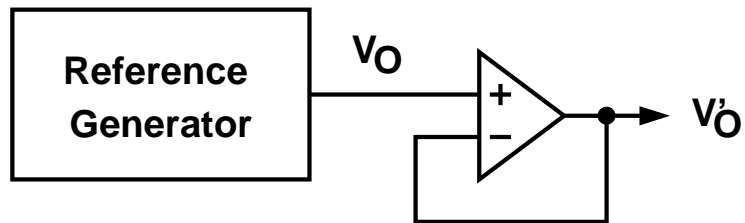
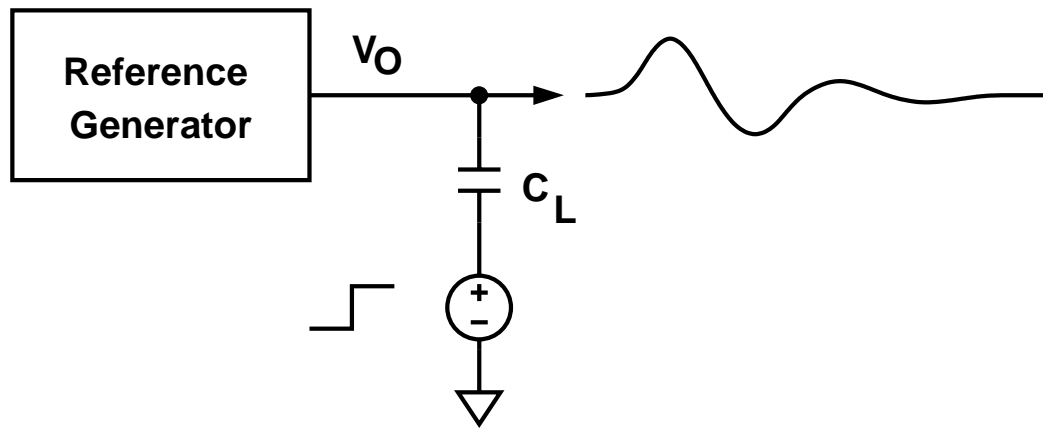
$$\Delta V = U_T \ln(n)$$

The output voltage,  $V_O$ , and current,  $I_O$ , are thus

$$V_O = V_{BE3} + U_T \cdot y \ln(n) \quad \text{and} \quad I_O = \frac{V_O}{R_x}$$

- A PTAT current from M8 develops a  $U_T$ -dependent voltage across resistor  $R_y$ . A proper choice of the ratio  $y$  can give a band-gap voltage at  $V_O$ .
- All currents are proportional to  $T$ .
- If desired, a temperature-independent output current can be realized by choosing  $y$  to give an appropriate TC to  $V_O$  to cancel the TC of resistor  $R_2$ .
- Reference: Song, et al., JSSC 12/83, pp. 634–643.

# Band-Gap Reference Output Issues



# Band-Gap Reference Output Issues

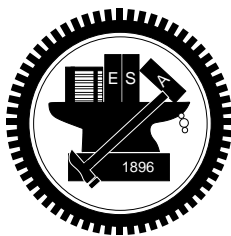
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- Feedback is employed in the reference generator. Loop stability must be ensured.
- The stability can be tested by observing the output step response.
- Capacitive loading at the output of reference generator has to be either extremely large (i.e., off-chip capacitors, undesirable because of extra pin, lead inductance, ...) or very small (not easy to accomplish).
- Can use buffers to reduce the output loading. But additional offset and drift are introduced.
- One possible scheme is using separate generators for different parts of system so as to isolate more sensitive circuits from other ones. However, mismatch among generators, area, power, and trimming cost must be considered.

# Output Stages

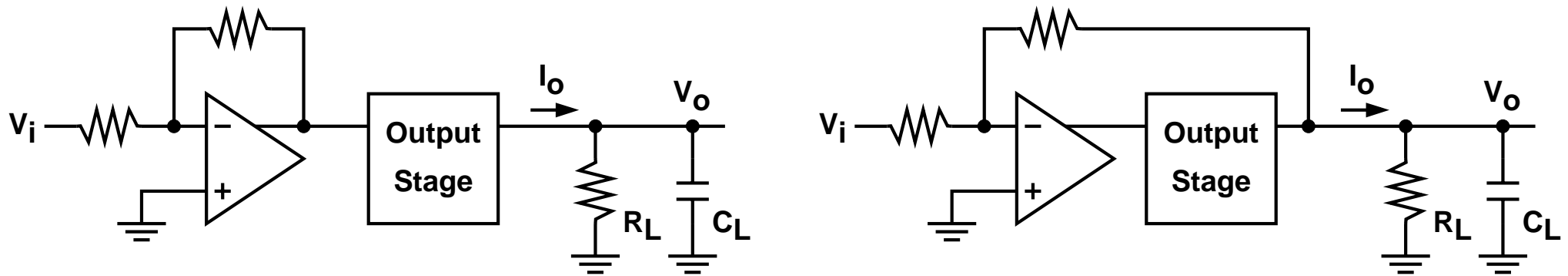
Jieh-Tsorng Wu

December 5, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Output Stage Requirements



- Deliver large output current to low-impedance loads (resistive and/or capacitive).
- Usually is a voltage buffer, i.e., low voltage gain, high  $Z_{in}$ , and low  $Z_o$ .
- High  $Z_{in}$  is to maintain voltage gain and bandwidth of previous stage.
- Wide bandwidth if in the feedback loop,
- May need protection against load shorts.

# Output Stage Design Issues

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- Frequency response.
- Output impedance.
- Output current.
- Output voltage range.
- Power efficiency.
- Distortion.

# Nonlinearity and Harmonic Distortion

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For a nonlinear system with input  $x$ , the output  $y$  can be expressed as:

$$y = a_0 + a_1x + a_2x^2 + a_3x^3 + \dots$$

With a pure sinusoidal input  $x = \hat{v} \cos \omega t$ ,

$$\begin{aligned} y &= a_0 + a_1\hat{v} \cos \omega t + a_2\hat{v}^2 \cos^2 \omega t + a_3\hat{v}^3 \sin^3 \omega t + \dots \\ &= a_0 + a_1\hat{v} \cos \omega t + \frac{a_2\hat{v}^2}{2}(1 + \cos 2\omega t) + \frac{a_3\hat{v}^3}{4}(3 \cos \omega t + \cos 3\omega t) + \dots \\ &= b_0 + b_1 \cos \omega t + b_2 \cos 2\omega t + b_3 \cos 3\omega t + \dots \end{aligned}$$

where

$$b_0 = a_0 + \frac{1}{2}a_2\hat{v}^2 + \dots$$

$$b_1 = a_1\hat{v} + \frac{3}{4}a_3\hat{v}^3 + \dots$$

$$b_2 = \frac{1}{2}a_2\hat{v}^2 + \dots$$

$$b_3 = \frac{1}{4}a_3\hat{v}^3 + \dots$$

# Nonlinearity and Harmonic Distortion

---

The harmonic distortion factors are

$$\text{HD}_2 \equiv \left| \frac{b_2}{b_1} \right| \approx \frac{1}{2} \frac{a_2}{a_1} \cdot \hat{v}$$
$$\text{HD}_3 \equiv \left| \frac{b_3}{b_1} \right| \approx \frac{1}{4} \frac{a_3}{a_1} \cdot \hat{v}^2$$

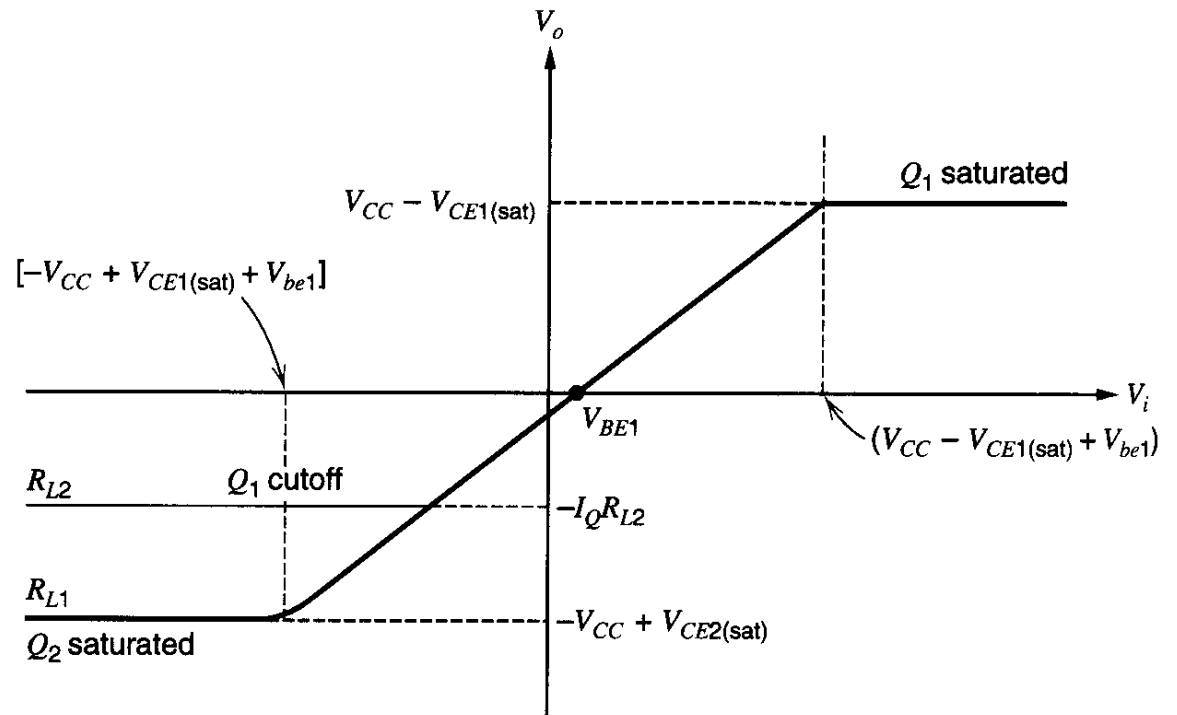
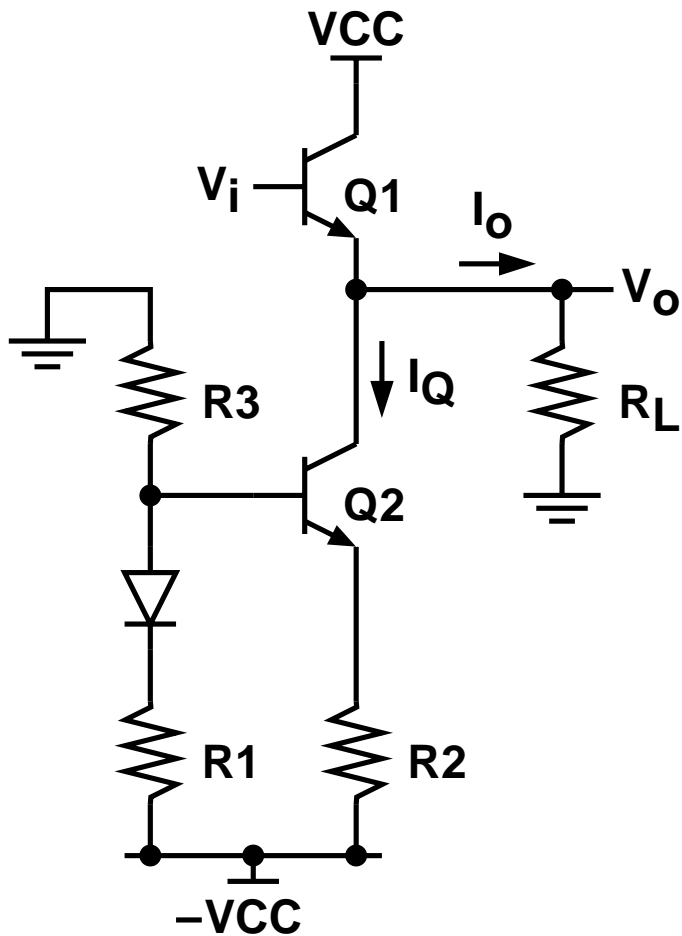
The total harmonic distortion (THD) is

$$\text{THD} = \frac{\sqrt{b_2^2 + b_3^2 + \dots}}{b_1}$$

The SINAD is the ratio of signal plus noise plus distortion powers to noise and distortion powers, i.e.,

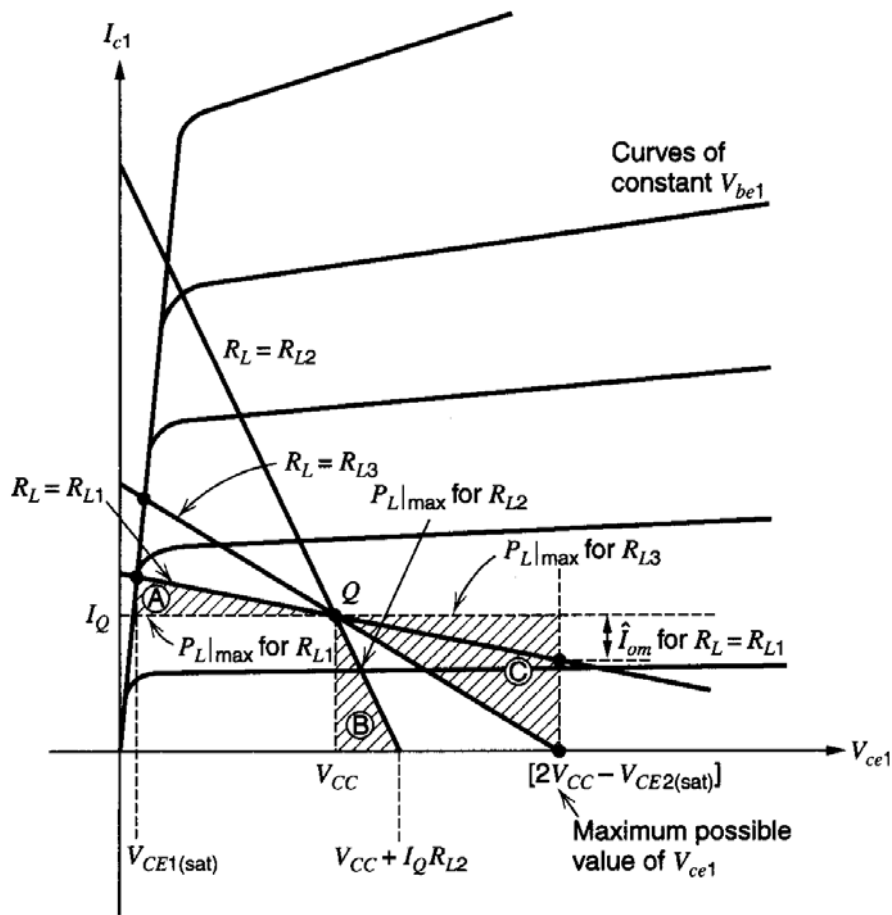
$$\text{SINAD} = \frac{S + N + D}{N + D}$$

# Class-A BJT Emitter Follower



$$V_{be1} = U_T \ln \left( \frac{I_{c1}}{I_{S1}} \right) \quad I_{c1} = I_Q + \frac{V_o}{R_L} \quad \Rightarrow \quad V_i = V_o + V_{be1} = V_o + U_T \ln \left( \frac{I_Q + V_o/R_L}{I_{S1}} \right)$$

# Class-A BJT Emitter Follower Output Power



$$V_{ce1} = V_{CC} - (I_{c1} - I_Q)R_L$$

For a sinusoidal  $V_o$  with amplitudes  $\hat{V}_o$  and  $\hat{I}_o$ ,

$$\text{Average Output Power} = P_L = \frac{1}{2} \hat{V}_o \hat{I}_o$$

$$\text{Average Supply Power} = P_{\text{supply}} = 2V_{CC}I_Q$$

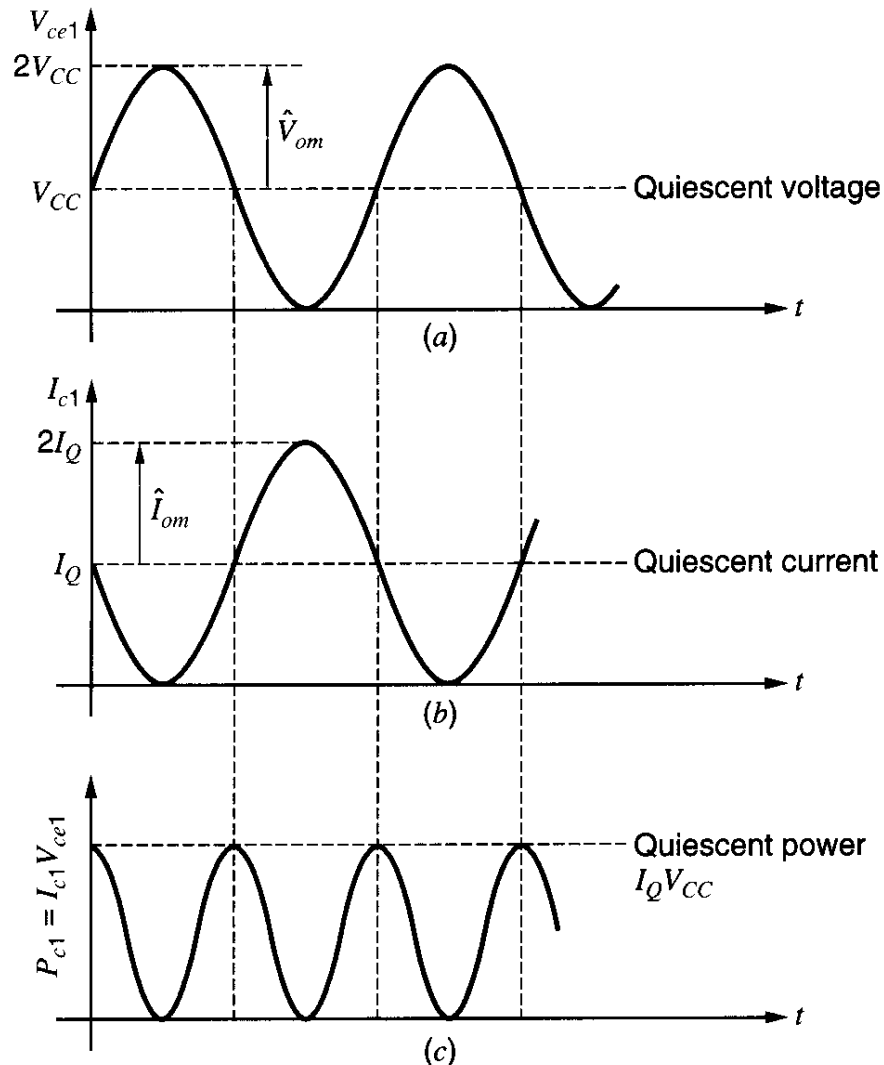
Maximum output swing and output power are

$$\hat{V}_{om} = V_{CC} - V_{CE(sat)} = I_Q \cdot R_L \quad \hat{I}_{om} = I_Q$$

$$P_{L(max)} = \frac{1}{2} \hat{V}_{om} \hat{I}_{om} = \frac{1}{2} [V_{CC} - V_{CE(sat)}] I_Q$$

$$\text{Power Conversion Efficiency} = \eta_C = \frac{P_L}{P_{\text{supply}}} \quad \eta_{C(max)} = \frac{1}{4} \left( 1 - \frac{V_{CE(sat)}}{V_{CC}} \right) \leq \frac{1}{4}$$

# Instantaneous Power Dissipation



Q1 Instantaneous Power Dissipation is

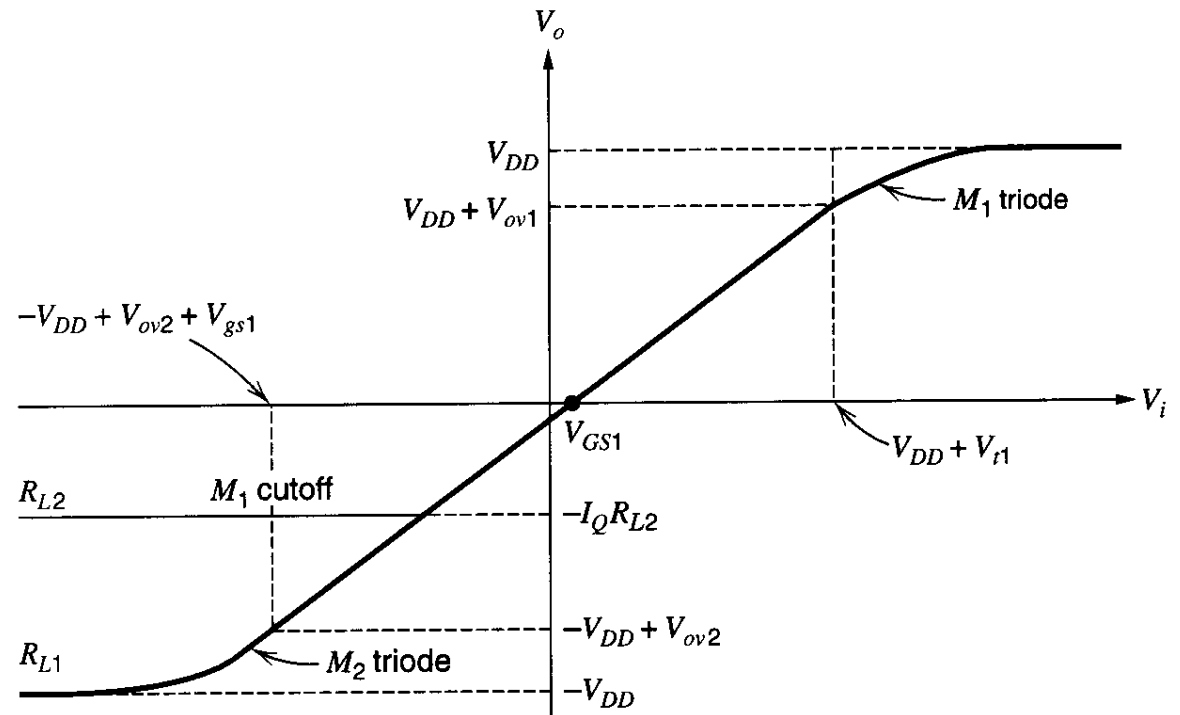
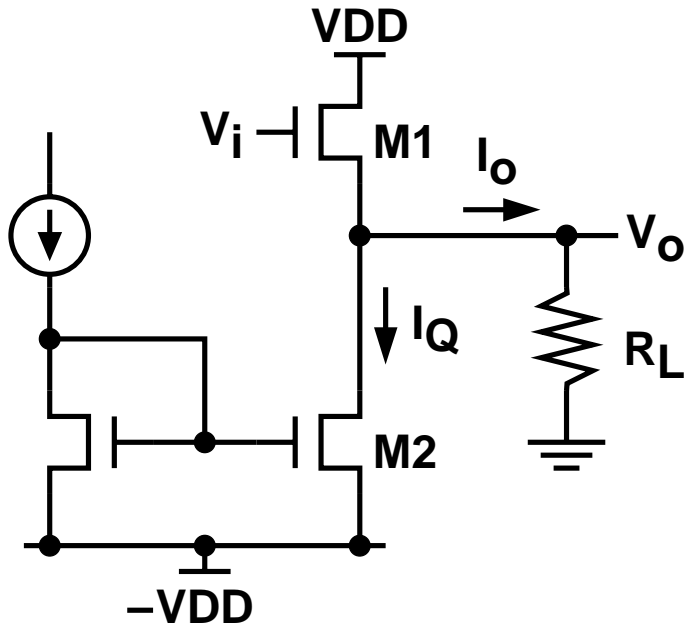
$$P_{c1} = V_{ce1} I_{c1}$$

At maximum  $\eta_C$ ,

$$\begin{aligned} P_{c1} &= V_{CC}(1 + \sin \omega t) \times I_Q(1 - \sin \omega t) \\ &= \frac{V_{CC} I_Q}{2} (1 + \cos 2\omega t) \end{aligned}$$

- The maximum  $P_{c1}$  occurs at the *midpoint* of any load line.

# Class-A MOST Source Follower



$$I_{d1} = I_Q + \frac{V_o}{R_L} \quad V_i = V_o + V_{gs1} = V_o + V_{t1} + V_{ov1}$$

$$\Rightarrow V_i = V_o + V_{t0} + \gamma \left( \sqrt{2\phi_f + V_o + V_{DD}} - \sqrt{2\phi_f} \right) + \sqrt{\frac{2(I_Q + V_o/R_L)}{k'(W/L)_1}}$$

# Distortion in the MOST Source Follower

---

Since  $V_i = f(V_o)$ , we have

$$V_i = V_i + v_i = \sum_{n=0}^{\infty} b_n (v_o)^n \quad v_o = V_o - V_O \quad b_n = \frac{1}{n!} f^{(n)}(V_O) \quad \Rightarrow \quad v_i = \sum_{n=1}^{\infty} b_n (v_o)^n$$

To find

$$v_o = \sum_{n=1}^{\infty} a_n (v_i)^n$$

use

$$\begin{aligned} v_i &= \sum_{n=1}^{\infty} b_n (v_o)^n = \sum_{n=1}^{\infty} b_n \left( \sum_{m=1}^{\infty} a_m (v_i)^m \right)^n \\ &= b_1 a_1 v_i + (b_1 a_2 + b_2 a_1^2) v_i^2 + (b_1 a_3 + 2b_2 a_1 a_2 + b_3 a_1^3) v_i^3 + \dots \end{aligned}$$

# Distortion in the MOST Source Follower

---

Matching coefficients, we obtain

$$a_1 = \frac{1}{b_1} \quad a_2 = -\frac{b_2}{b_1^3} \quad a_3 = \frac{2b_2^2}{b_1^5} - \frac{b_3}{b_1^4}$$

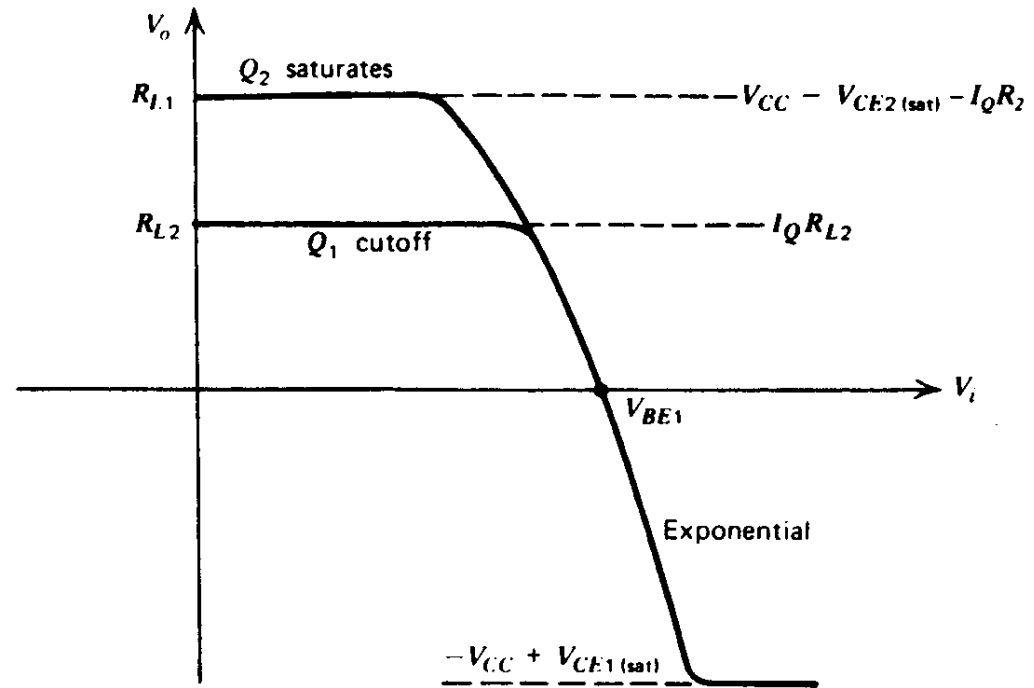
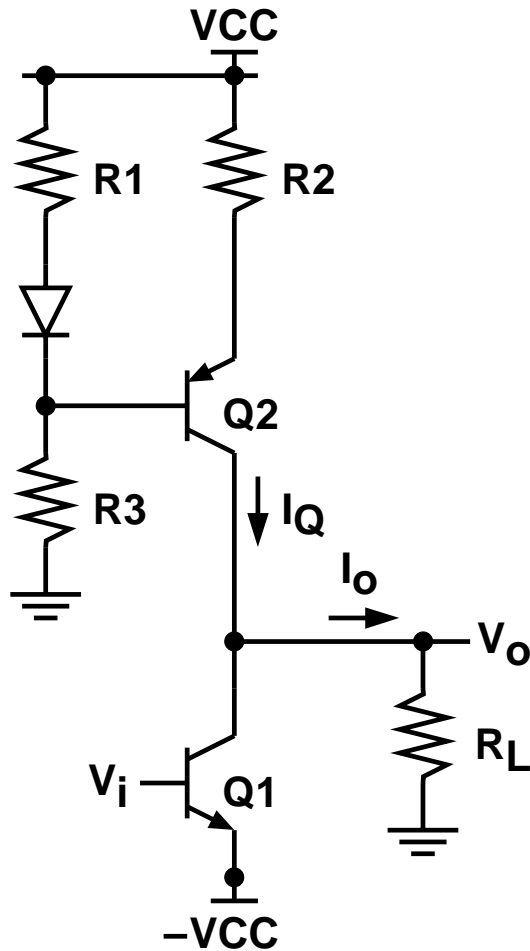
- Assume  $R_L \rightarrow \infty$ , and let  $V_M = V_O + V_{DD} + 2\phi_f$ ,  $v_i = \hat{v}_i \sin \omega t$ , then

$$a_1 = \frac{1}{1 + \frac{\gamma}{2} V_M^{-1/2}} \quad a_2 = \frac{\frac{\gamma}{8} V_M^{-3/2}}{\left(1 + \frac{\gamma}{2} V_M^{-1/2}\right)^3} \quad a_3 = -\frac{\frac{\gamma}{16} V_M^{-5/2}}{\left(1 + \frac{\gamma}{2} V_M^{-1/2}\right)^5}$$

$$\text{HD}_2 = \frac{1 a_2}{2 a_1} \cdot \hat{v}_i = \frac{\gamma}{16} \frac{V_M^{-3/2}}{\left(1 + \frac{\gamma}{2} V_M^{-1/2}\right)^2} \cdot \hat{v}_i$$

$$\text{HD}_3 = \frac{1 a_3}{4 a_1} \cdot \hat{v}_i^2 = -\frac{\gamma}{64} \frac{V_M^{-5/2}}{\left(1 + \frac{\gamma}{2} V_M^{-1/2}\right)^4} \cdot \hat{v}_i^2$$

# Class-A BJT Common-Emitter Stage



$$I_o = I_Q - I_{c1} \Rightarrow V_o = I_o R_L = (I_Q - I_S e^{V_i/U_T}) R_L$$

Same output power,  $\eta_C$ , and  $P_{c1}$  as the class-A emitter followers, since

$$V_{ce1} = V_{CC} - (I_{c1} - I_Q)R_L$$

# Distortion in Class-A BJT Common-Emitter Stage

---

Assume the input is

$$V_i = V_{BE1} + v_i \quad I_Q = I_S e^{V_{BE1}/U_T}$$

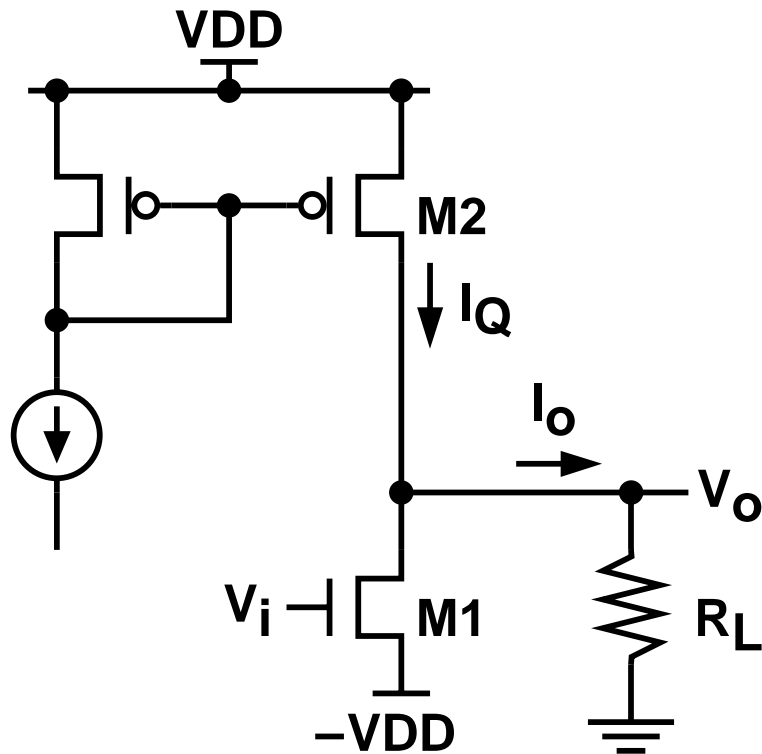
Then, the output voltage is

$$\begin{aligned} V_o &= -R_L \left[ I_S e^{(V_{BE1} + v_i)/U_T} - I_Q \right] = -R_L I_Q \left( e^{v_i/U_T} - 1 \right) \\ &= -R_L I_Q \left[ \frac{v_i}{U_T} + \frac{1}{2} \left( \frac{v_i}{U_T} \right)^2 + \frac{1}{6} \left( \frac{v_i}{U_T} \right)^3 + \dots \right] = a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \dots \end{aligned}$$

Let  $v_i = \hat{v}_i \sin \omega t$ , then the harmonic distortion factors are

$$\begin{aligned} \text{HD}_2 &= \frac{1}{2} \frac{a_2}{a_1} \cdot \hat{v}_i = \frac{1}{4} \frac{\hat{v}_i}{U_T} \\ \text{HD}_3 &= \frac{1}{4} \frac{a_3}{a_1} \cdot \hat{v}_i^2 = \frac{1}{24} \left( \frac{\hat{v}_i}{U_T} \right)^2 \end{aligned}$$

# Class-A MOST Common-Source Stage



$$V_o = I_o R_L = (I_Q - I_{d1}) R_L$$

$$I_{d1} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_i - V_t)^2 = \frac{1}{2} k (V_i - V_t)^2$$

Let  $V_i = V_I + v_i$ ,  $V_I = V_{ov} + V_t$  and  $I_Q = (1/2)kV_{ov}^2$

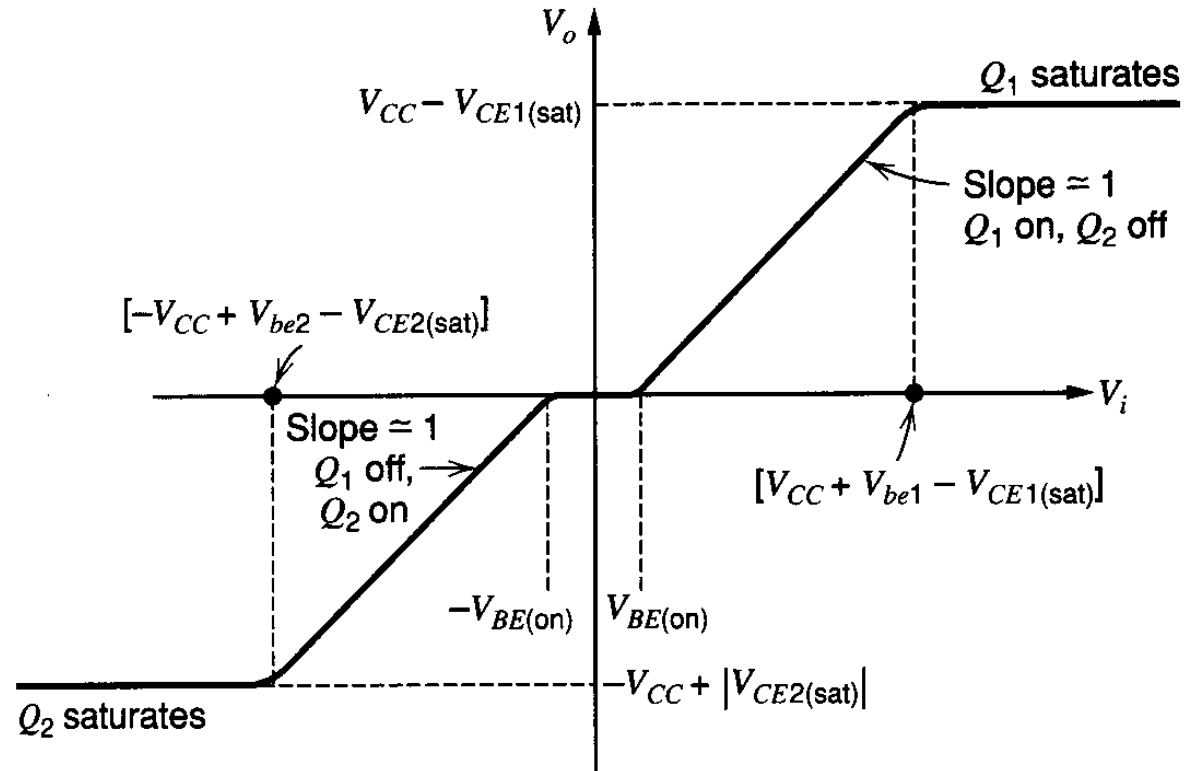
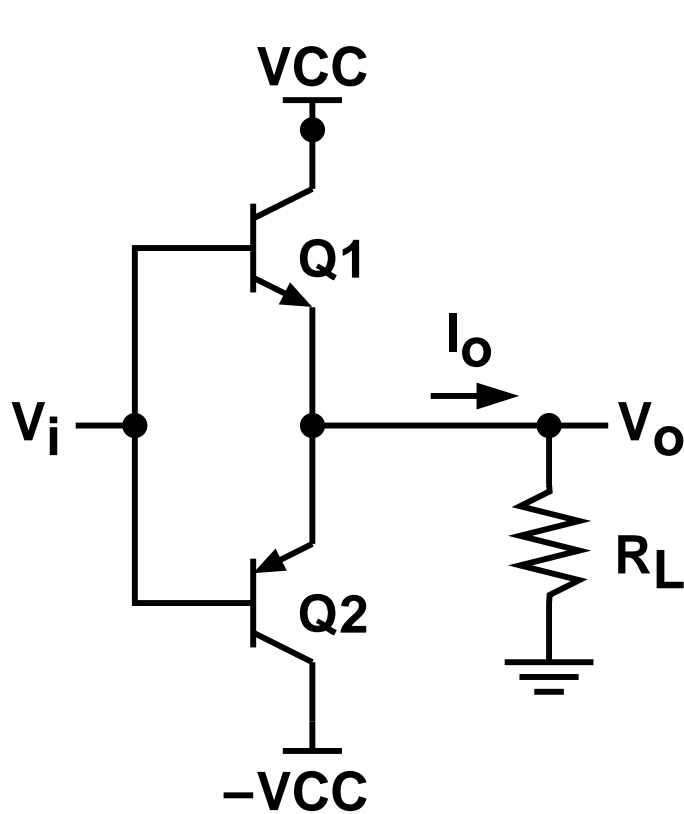
$$V_o = R_L (I_Q - I_d) = R_L \left[ I_Q - \frac{1}{2} k (V_{ov} + v_i)^2 \right]$$

$$= -R_L I_Q \left[ 2 \left( \frac{v_i}{V_{ov}} \right) + \left( \frac{v_i}{V_{ov}} \right)^2 \right]$$

Let  $v_i = \hat{v}_i \sin \omega t$ , then the harmonic distortion factors are

$$HD_2 = \frac{1 a_2}{2 a_1} \cdot \hat{v}_i = \frac{1}{4} \left( \frac{v_i}{V_{ov}} \right) \quad HD_3 = 0$$

# Class-B Push-Pull Emitter Follower



# Output Power of Class-B Push-Pull Emitter Follower

For a sinusoidal output

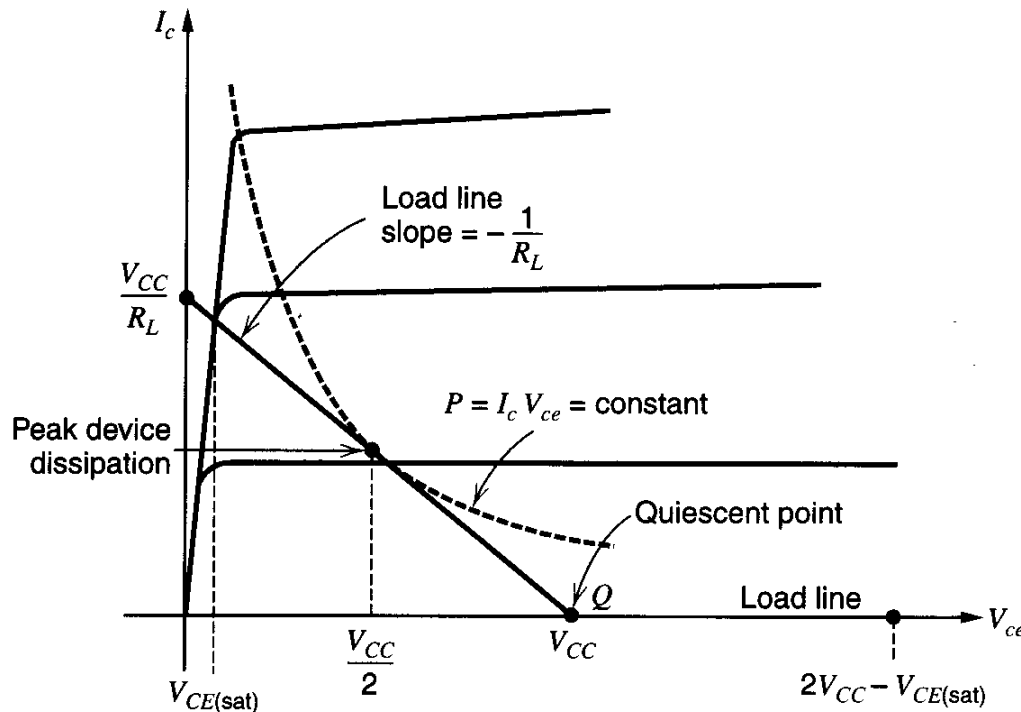
$$V_o = \hat{V}_o \sin \omega t \quad I_o = V_o/R_L = \hat{I}_o \sin \omega t$$

We have

$$P_L = \frac{1}{2} \hat{V}_o \hat{I}_o = \frac{1}{2} \frac{\hat{V}_o^2}{R_L}$$

$$I_{\text{supply}} = \frac{1}{T/2} \int_0^{T/2} I_{c1}(t) dt = \frac{2 \hat{V}_o}{\pi R_L} = \frac{2}{\pi} \hat{I}_o$$

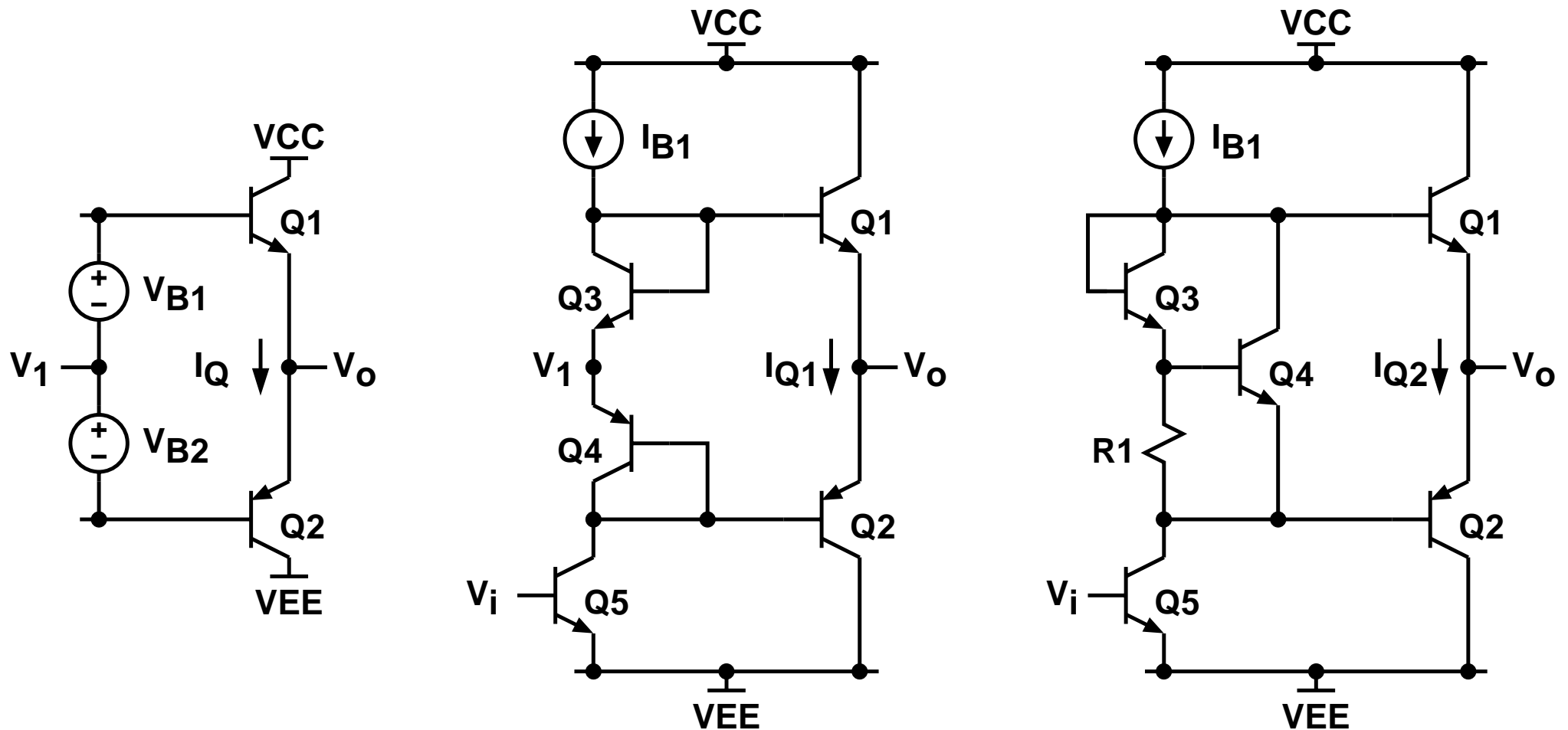
$$P_{\text{supply}} = V_{CC} I_{\text{supply}} = \frac{2 V_{CC}}{\pi R_L} \cdot \hat{V}_o$$



$$V_{ce1} = V_{CC} - I_{c1} R_L$$

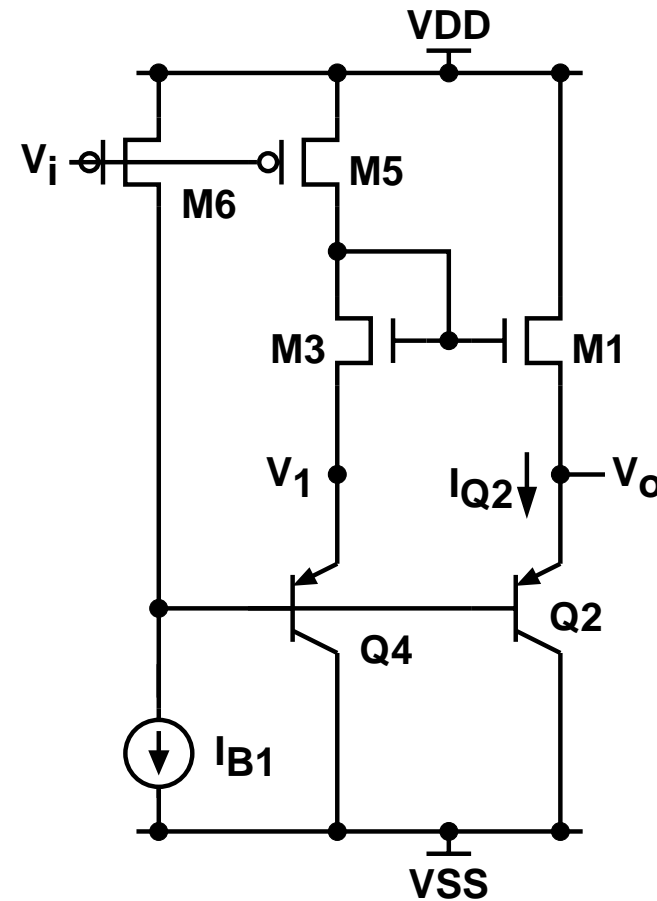
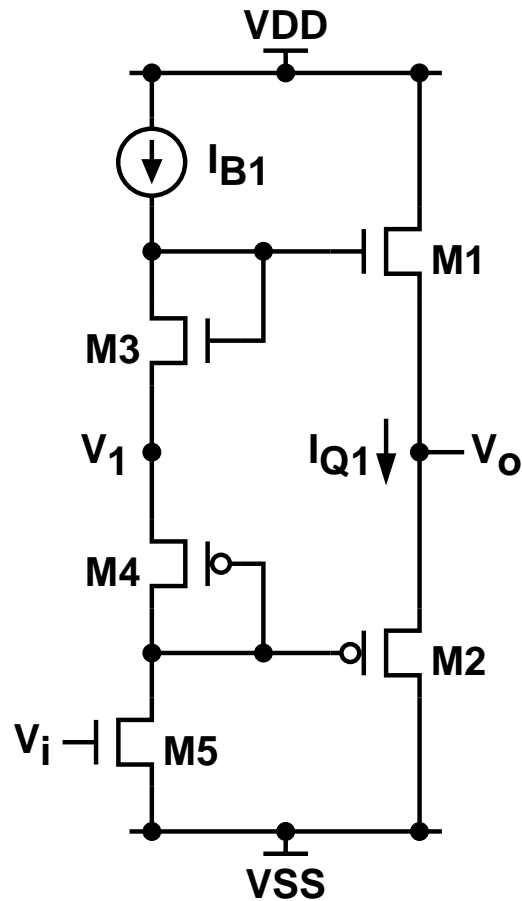
$$\text{Power Conversion Efficiency} = \eta_C = \frac{\pi \hat{V}_o}{4 V_{CC}} \leq \frac{\pi}{4}$$

# Class-AB Push-Pull Emitter Followers



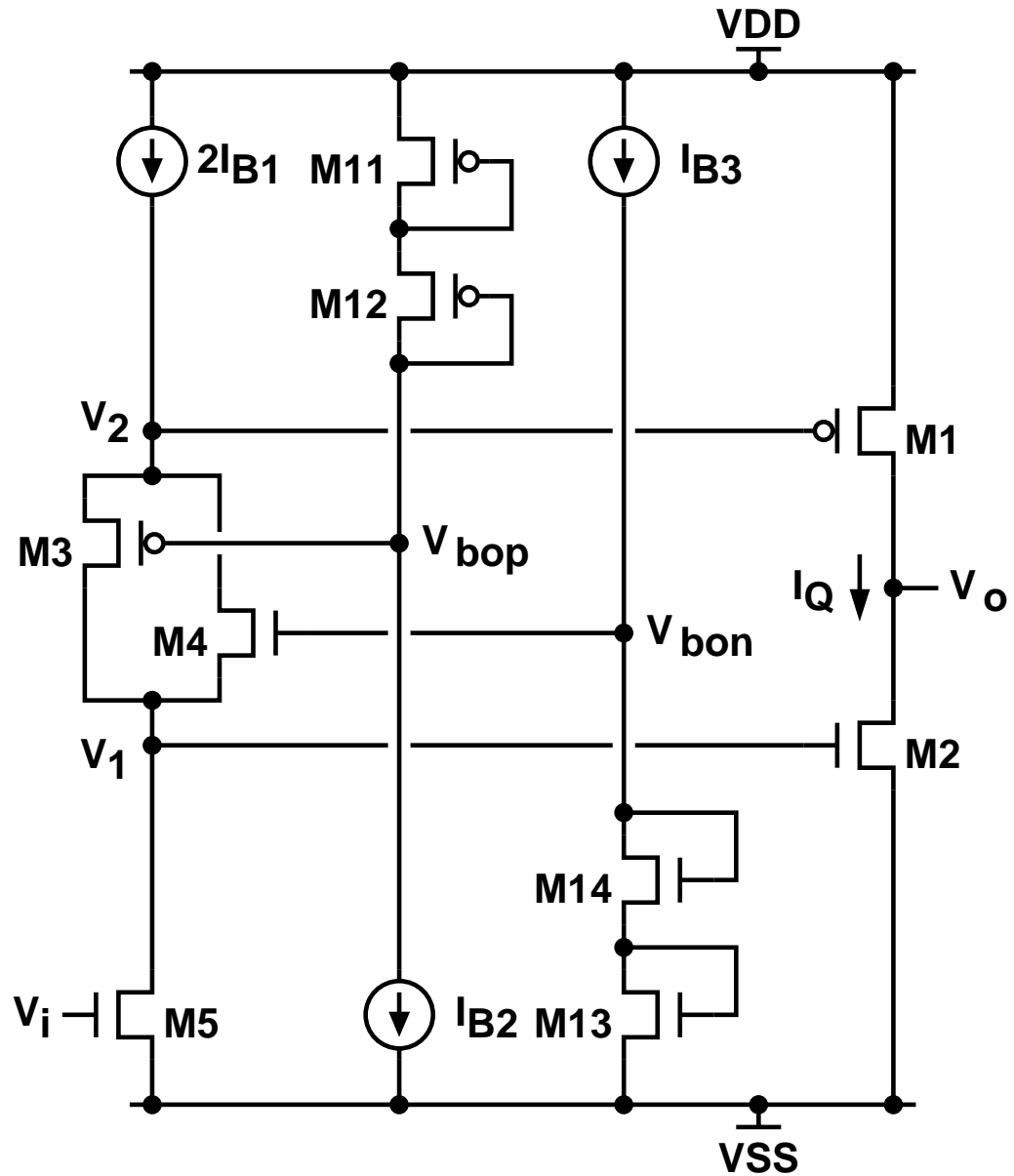
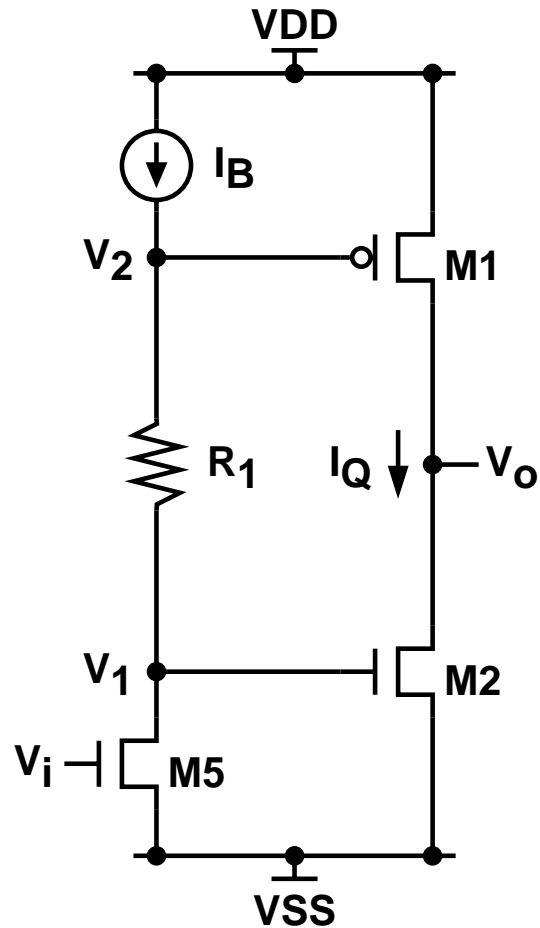
$$V_{BE1} + |V_{BE2}| = V_{BE3} + |V_{BE4}| \quad \Rightarrow \quad I_{Q1} = I_{B1} \sqrt{\frac{I_{S1} I_{S2}}{I_{S3} I_{S4}}} \quad I_{Q2} = \sqrt{I_{C3} I_{C4}} \sqrt{\frac{I_{S1} I_{S2}}{I_{S3} I_{S4}}}$$

# Class-AB Push-Pull Source Followers



$$V_{GS1} + |V_{GS2}| = V_{GS3} + |V_{GS4}| \Rightarrow I_{Q1} = I_{B1} \left( \frac{1/\sqrt{k'_n(W/L)_3} + 1/\sqrt{k'_p(W/L)_4}}{1/\sqrt{k'_n(W/L)_1} + 1/\sqrt{k'_p(W/L)_2}} \right)^2$$

# Class-AB Push-Pull Common-Source Stage



## Class-AB Push-Pull Common-Source Stage

---

Let  $I_{B1} = I_{B2} = I_{B3}$ , and

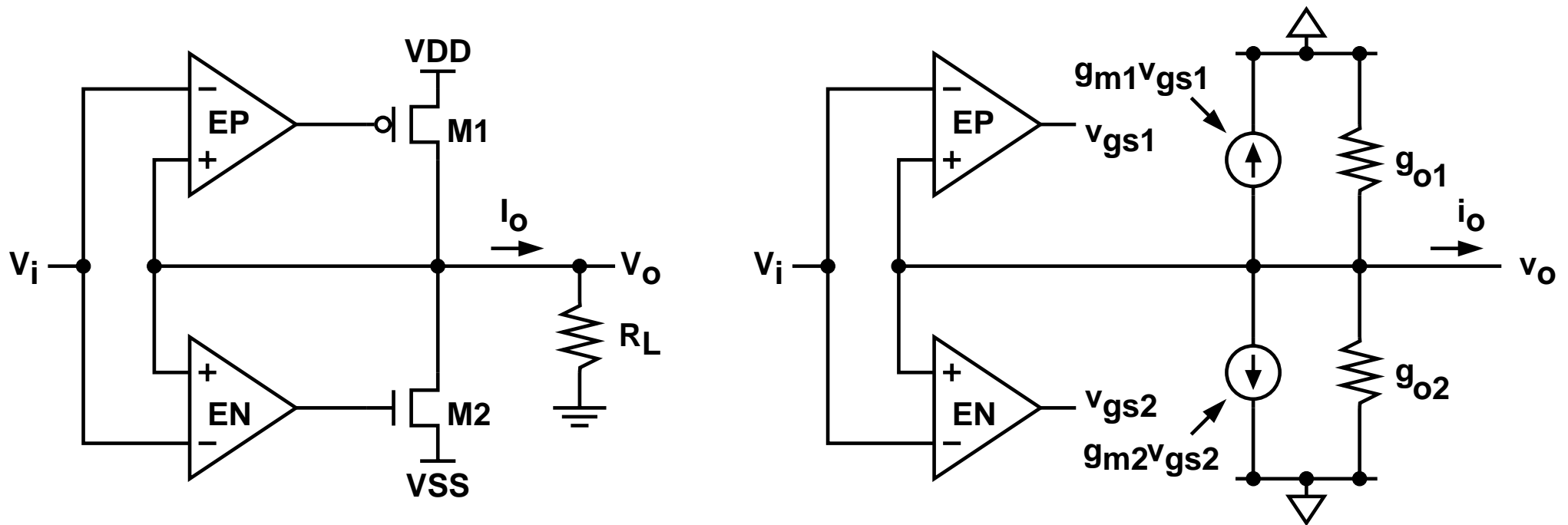
$$\frac{1}{K} \left( \frac{W}{L} \right)_1 = \left( \frac{W}{L} \right)_{11} \quad \left( \frac{W}{L} \right)_3 = \left( \frac{W}{L} \right)_{12} \quad \frac{1}{K} \left( \frac{W}{L} \right)_2 = \left( \frac{W}{L} \right)_{13} \quad \left( \frac{W}{L} \right)_4 = \left( \frac{W}{L} \right)_{14}$$

Then,  $V_{GS1} = V_{GS11}$ ,  $V_{GS3} = V_{GS12}$ ,  $V_{GS2} = V_{GS13}$ ,  $V_{GS4} = V_{GS14}$ , and

$$I_Q = I_{D1} = I_{D2} = K \cdot I_{B1}$$

- M3 and M4 form a floating resistor.
- Large output impedance. The pole at  $V_o$  can be significant.
- Large distortion. Usually this output stage is included in the feedback loop.

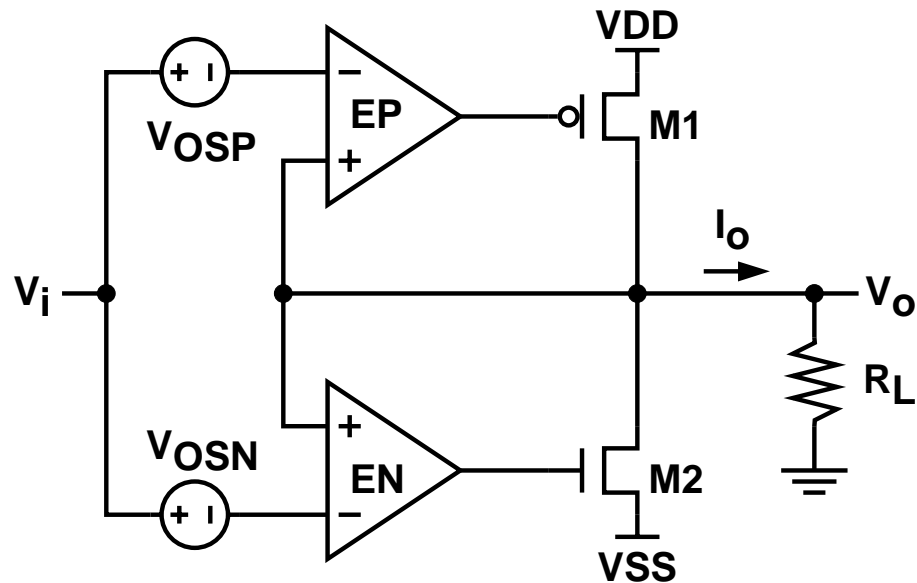
# Class-AB Quasi-Complementary Configuration



$$G_o = -\left. \frac{i_o}{V_o} \right|_{v_i=0} = g_{m1}A_{EP} + g_{m2}A_{EN} + g_{o1} + g_{o2}$$

- The distortion and output resistance are reduced by  $A_{EP}$  and  $A_{EN}$ .
- Need to control  $I_Q$ .

# Class-AB Quasi-Complementary Configuration



$$A_{EP} = A_{EN} = A$$

$$V_{tn} = -V_{tp} = V_t$$

$$k'_p \left(\frac{W}{L}\right)_1 = k'_n \left(\frac{W}{L}\right)_2 = k' \left(\frac{W}{L}\right)$$

$$I_{d1} = -\frac{1}{2} k' \frac{W}{L} (V_{gs1} + V_t)^2$$

$$I_{d2} = \frac{1}{2} k' \frac{W}{L} (V_{gs2} - V_t)^2$$

If  $V_i = 0$  and  $V_{OSP} = V_{OSN} = 0$ , let

$$-I_{D1} = I_{D2} = I_Q \quad V_{ov} = \sqrt{\frac{2I_Q}{k'(W/L)}} \quad V_{gs1} = -V_t - V_{ov} \quad V_{gs2} = V_t + V_{ov}$$

# Class-AB Quasi-Complementary Configuration

---

We have

$$V_{gs1} = -V_t - V_{ov} + A[V_o - (V_i - V_{OSP})] \quad V_{gs2} = V_t + V_{ov} + A[V_o - (V_i - V_{OSP})]$$

$$I_o = \frac{V_o}{R_L} \quad I_o + I_{d1} + I_{d2} = 0 \quad \Rightarrow \quad V_o = \frac{V_i - \frac{V_{OSP} + V_{OSN}}{2}}{1 + \frac{1}{k'(W/L)A[2V_{ov} - A(V_{OSP} - V_{OSN})]R_L}}$$

- If  $V_{OSP} = V_{OSN} = 0$ ,

$$V_o = \frac{V_i}{1 + \frac{1}{k'(W/L)A2V_{ov}R_L}} = \frac{V_i}{1 + \frac{1}{2Ag_mR_L}} \quad g_m = k' \frac{W}{L} V_{ov}$$

- If  $A(V_{OSP} - V_{OSN}) \ll 2V_{ov}$  and  $2Ag_mR_L \gg 1$ ,

$$V_o = \frac{V_i - \frac{V_{OSP} + V_{OSN}}{2}}{1 + \frac{1}{k'(W/L)A2V_{ov}R_L}} = \frac{V_i - \frac{V_{OSP} + V_{OSN}}{2}}{1 + \frac{1}{2Ag_mR_L}} \approx V_i - \frac{V_{OSP} + V_{OSN}}{2}$$

# Class-AB Quasi-Complementary Configuration

---

To find  $I_Q$  when  $V_{OSP}$  and  $V_{OSN}$  exist, let  $V_i = 0$  and

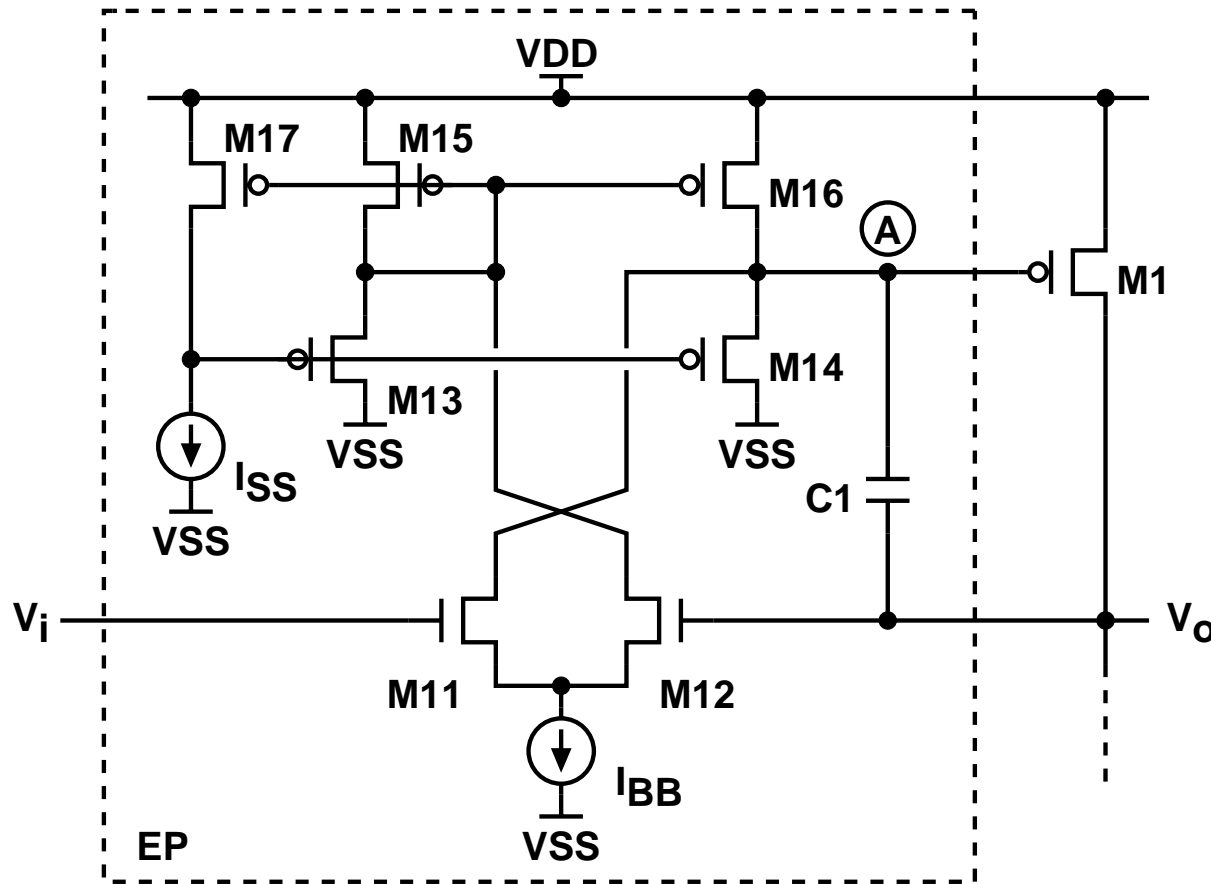
$$V_o + V_{OSP} \approx \frac{V_{OSP} - V_{OSN}}{2} \quad V_o + V_{OSN} \approx -\frac{V_{OSP} - V_{OSN}}{2}$$
$$I_Q = \frac{1}{2} k' \frac{W}{L} \left( V_{ov} - A \frac{V_{OSP} - V_{OSN}}{2} \right)^2$$

Define  $I_{Q0} = I_Q$  when  $V_{OSP} = V_{OSN} = 0$ , and  $\Delta I_Q = I_{Q0} - I_Q$ ,

$$\Delta I_Q = \frac{1}{2} k' \frac{W}{L} A (V_{OSP} - V_{OSN}) \left( V_{ov} - A \frac{V_{OSP} - V_{OSN}}{4} \right)$$
$$\frac{\Delta I_Q}{I_{Q0}} = A \left( \frac{V_{OSP} - V_{OSN}}{V_{ov}} \right) \left( 1 - A \frac{V_{OSP} - V_{OSN}}{4V_{ov}} \right) \approx A \left( \frac{V_{OSP} - V_{OSN}}{V_{ov}} \right)$$

- Must keep  $A$  small to reduce  $I_Q$  variation.

# An Error Amplifier Example



Let

$$(W/L)_{15} = (W/L)_{16} = (W/L)_{17}$$

$$(W/L)_{13} = (W/L)_{14}$$

$$\Rightarrow I_{Q(M1)} = I_{SS} \times \frac{(W/L)_1}{(W/L)_{17}}$$

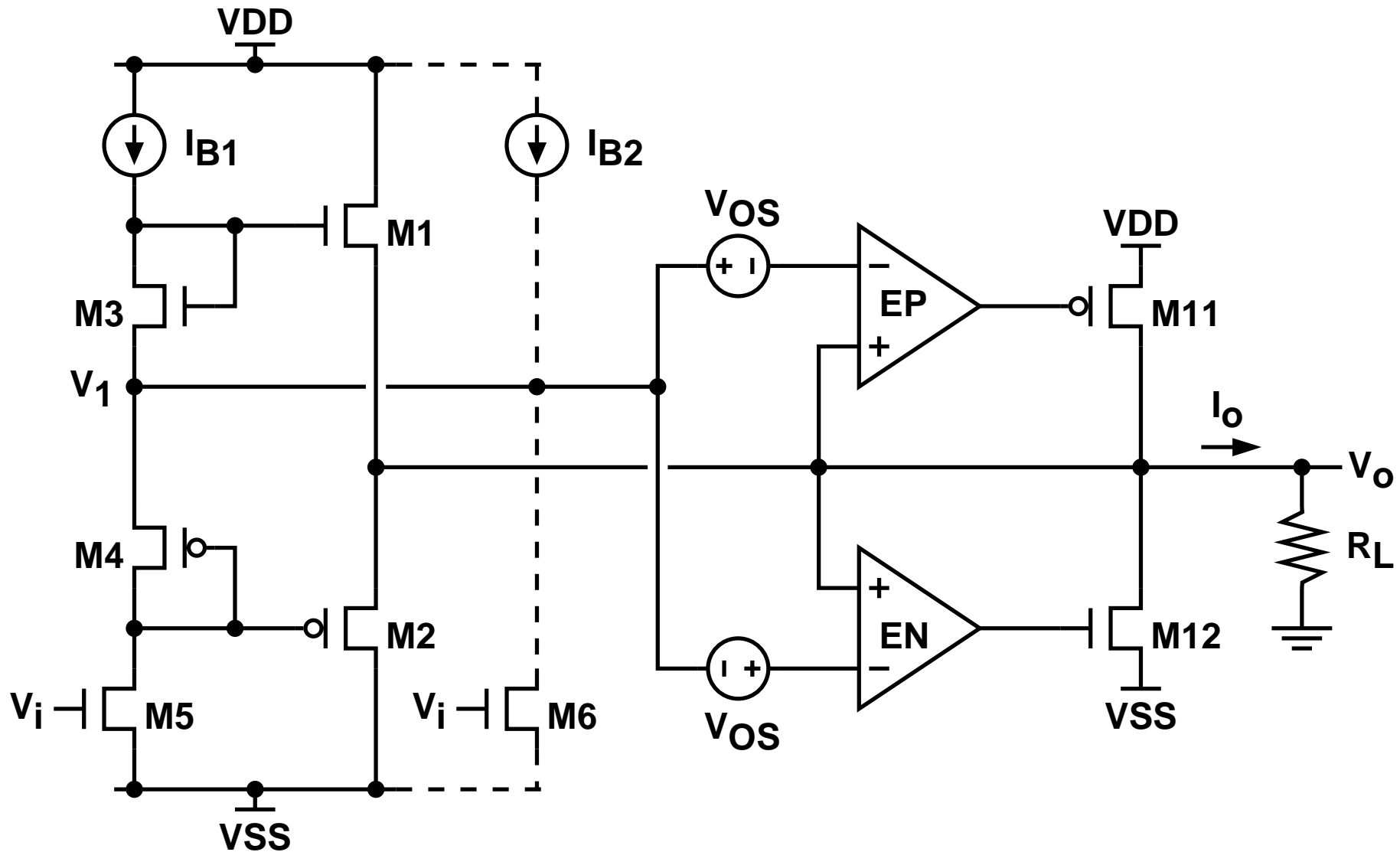
$$I_{D13} = I_{D14} = I_{SS} - I_{BB}/2$$

Voltage gain is

$$A_{EP} = \frac{g_{m11}}{g_{m14} + g_{mb14}}$$

- Want large swing at node A to provide strong gate drive for M1.
- Reference: Khorramabadi, JSSC 4/92, pp. 539–544.

# Combined Common-Drain Common-Source Configuration

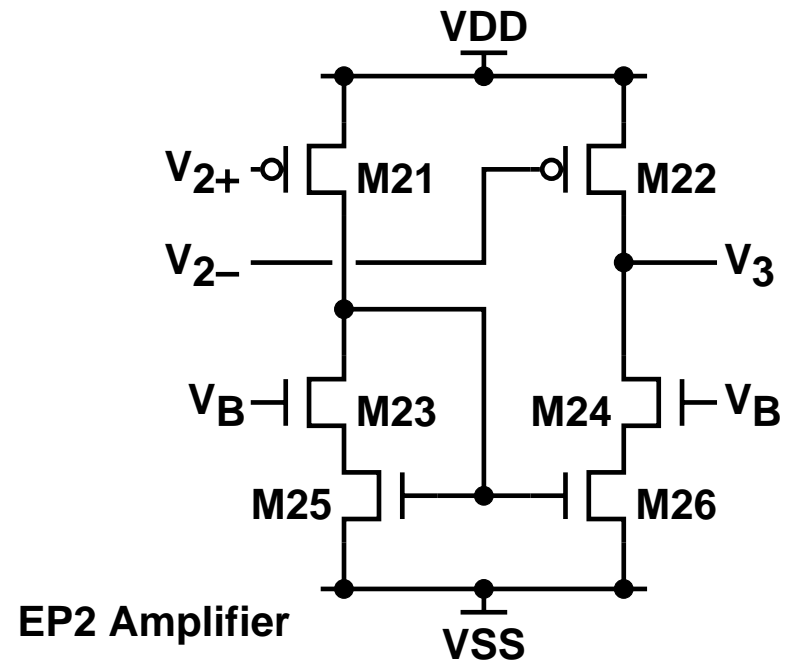
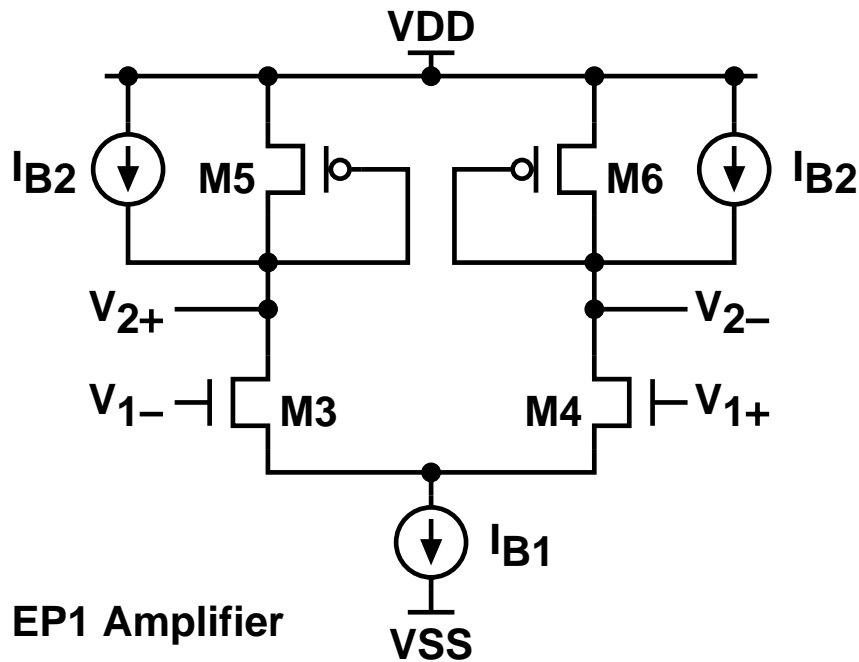
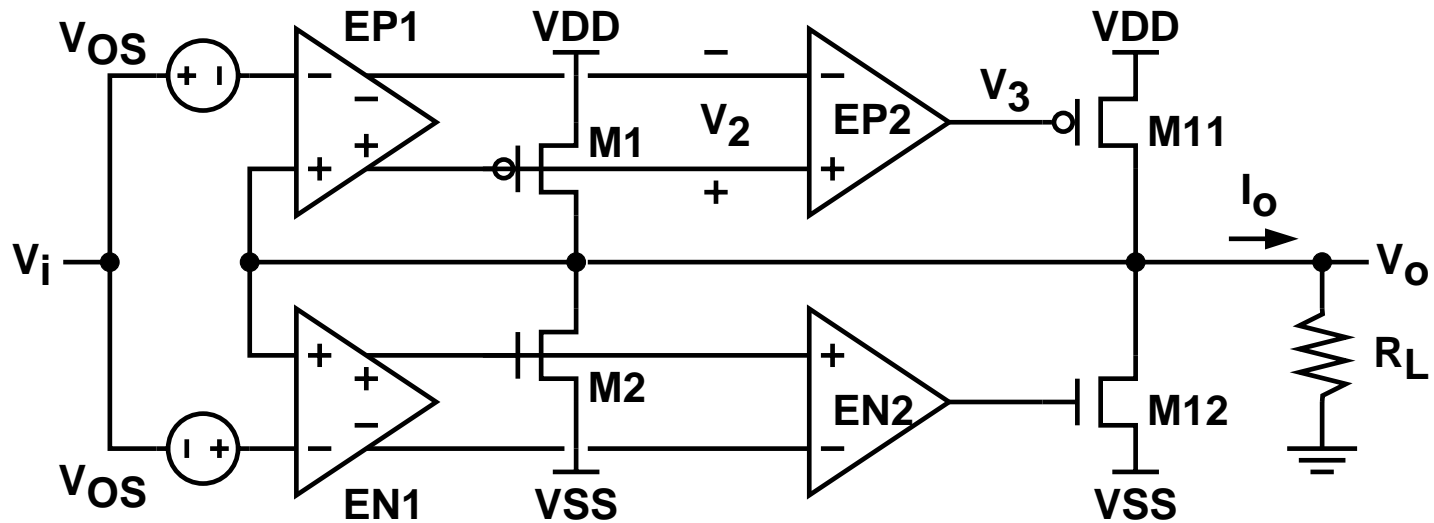


# Combined Common-Drain Common-Source Configuration

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- $V_{OS}$  can be introduced by intentionally mismatching the input differential pair in each error amplifier.
- The circuit can be designed so that, when  $V_o = V_1 = 0$ , the introduction of  $V_{OS}$  turn off M11 and M12.
- M11 is turned on only when  $V_1 - V_o - V_{OS} > |V_{tp}|/A_{EP}$ .
- Error amplifiers,  $A_{EP}$  and  $A_{EN}$ , can have high gain, and are often designed as one-stage amplifier with gain  $\approx g_m r_o$ .
- The wide bandwidth of M1 and M2 source followers simplify the design required to guarantee stability.
- The  $V_1$  voltage range, limited by  $V_{gs3}$  and  $V_{gs4}$ , can be increased by adding the M6 common-source stage.

# Parallel Common-Source Configuration



## Parallel Common-Source Configuration

---

- Want turn off M11 and M12 when  $V_o \approx V_i = 0$ , so that  $A_{EP2}$  and  $A_{EN2}$  have high gain, and  $A_{EP1}$  and  $A_{EN1}$  have low gain.
- $V_{OS}$  of EP1 is introduced by making  $(W/L)_3 \simeq 0.8(W/L)_4$ . When  $V_o \approx V_i = 0$ ,

$$I_{D3} = I_{B1} \cdot \frac{(W/L)_3}{(W/L)_3 + (W/L)_4} \quad I_{D1} = (I_{D3} - I_{B2}) \cdot \frac{(W/L)_1}{(W/L)_3}$$

$$A_{EP1} = \frac{g_{m3}}{g_{m5}} = \sqrt{\frac{k'_n \cdot (W/L)_3}{k'_p \cdot (W/L)_5} \cdot \frac{I_{D3}}{I_{D3} - I_{B2}}} \quad A_{EP2} \approx g_{m22} r_{o22}$$

- When  $|V_i|$  is small, and M11 and M12 are not turned on, the output is

$$V_o = \frac{V_i}{1 + 1/(A_1 g_{m1} R_L)}$$

## Parallel Common-Source Configuration

---

- When  $V_i$  is large, M11 can be turned on, and the output becomes

$$V_o \approx V_i - V_{OS} \quad \text{if } A_{EP2} \rightarrow \infty$$

- When  $V_{2+} = V_{2-}$  at EP2, define  $V_3 = V_{ov25} + V_{t25} + V_{SS} = V_K + V_{SS}$ . Then

$$V_3 = [V_o - (V_i - V_{OS})]A_{EP1}A_{EP2} + V_K + V_{SS}$$

Define  $V_{i(min)}$  as the minimum input to turn on M11. Let  $V_3 = V_{DD} - |V_{tp11}|$ , we have

$$V_{i(min)} = V_{OS}(1 + A_{EP1}g_{m1}R_L) - \frac{(V_{DD} - V_{SS} - V_K - |V_{tp11}|)(1 + A_{EP1}g_{m1}R_L)}{A_{EP1}A_{EP2}}$$

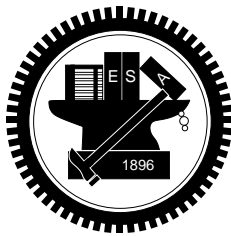
$$V_{i(min)} = V_{OS}(1 + A_{EP1}g_{m1}R_L) \quad \text{if } A_{EP2} \rightarrow \infty$$

M11 and M12 remain off for only a small range of input voltages.

# Noise Analysis and Modeling

Jieh-Tsorng Wu

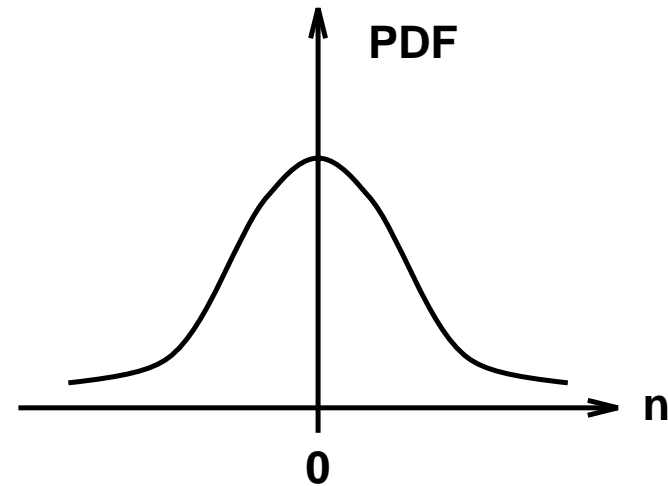
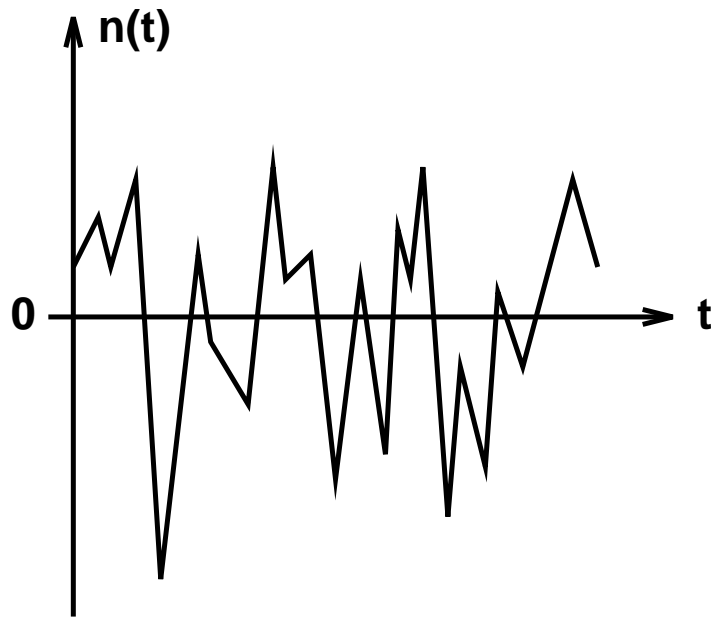
December 5, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Noise in Time Domain

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$$\text{Mean} = \bar{n} = \frac{1}{T} \int_0^T n(t) dt = 0$$

$$\text{Noise Power} = \overline{n^2} = \frac{1}{T} \int_0^T n^2(t) dt$$

$$\text{Root Mean Square} = n_{\text{rms}} = \left( \overline{n^2} \right)^{1/2}$$

- $T$  is a suitable averaging time interval. Typically, a longer  $T$  gives a more accurate measurement.

# Probability Density Function

---

- The probability that the noise lies between values  $n$  and  $n + dn$  at any time is given by  $P(n)dn$ .  $P(n)$  is the probability density function (PDF).
- The PDF of a random noise is usually Gaussian, i.e.,

$$P(n) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{n^2}{2\sigma^2}}$$

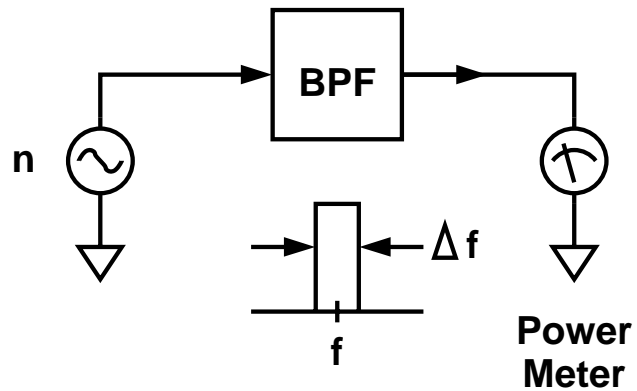
We have

$$\int_{-\infty}^{+\infty} \text{PDF}(n)dn = 1$$

and

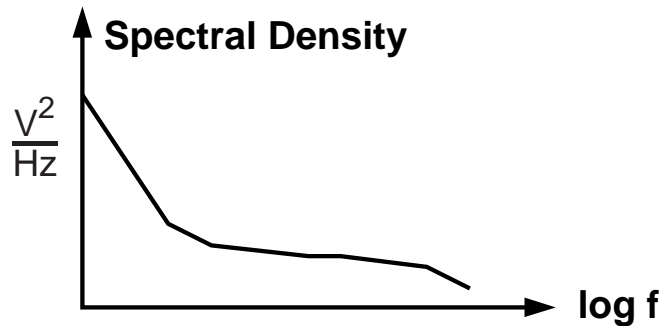
$$\text{Variance} = \int_{-\infty}^{+\infty} n^2 \cdot \text{PDF}(n)dn = \overline{n^2} = \sigma^2$$

# Noise in Frequency Domain



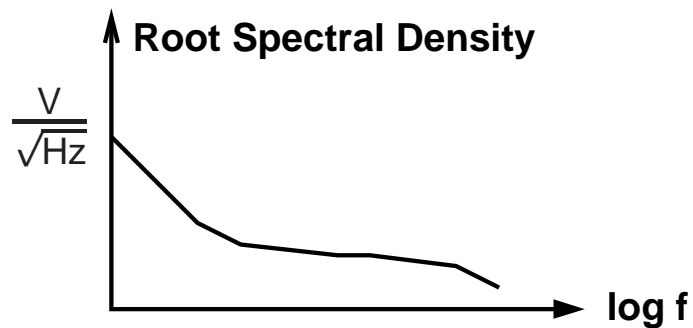
One-sided *power spectral density*

$$SD(f) = \lim_{\Delta f \rightarrow 0} \frac{\overline{n^2(f)}}{\Delta f}$$



One-sided *root spectral density*

$$RD(f) = (SD)^{1/2}$$

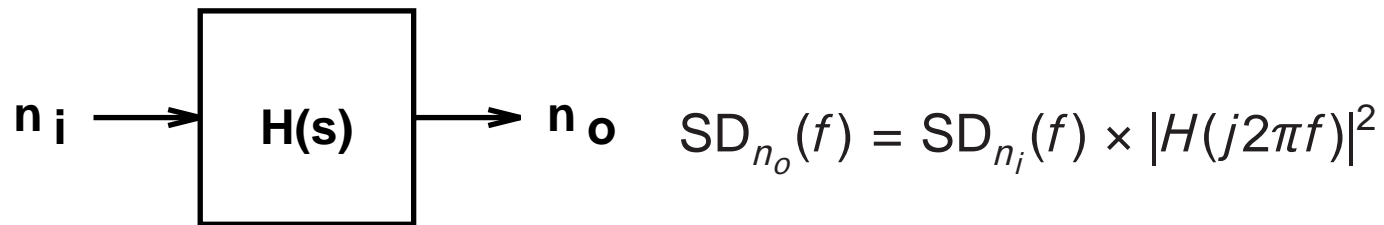


The total noise power is

$$\int_0^{\infty} SD_n(f) df = \overline{n^2}$$

## Filtered Noise

---



If  $SD_{n_i}(f) = N$  is a constant (white noise), then

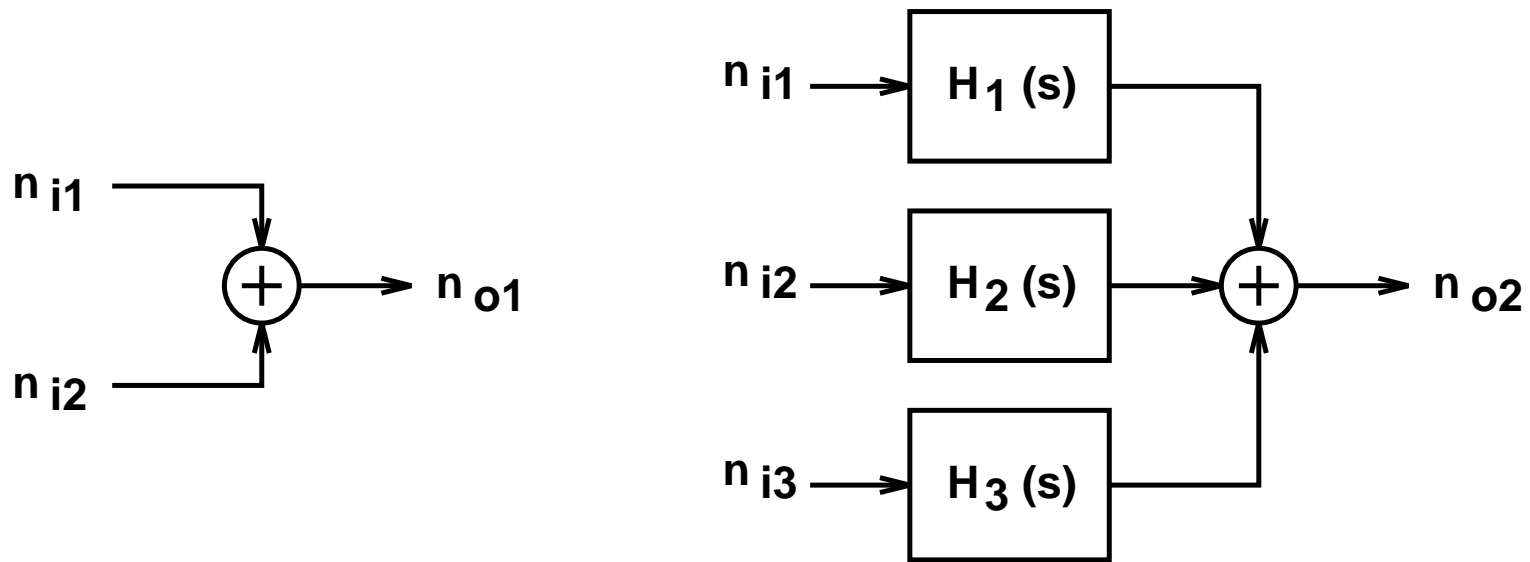
$$\overline{n_o^2} = \int_0^{\infty} SD_{n_i}(f) \cdot |H(j2\pi f)|^2 df = N \cdot \int_0^{\infty} |H(j2\pi f)|^2 df = N \cdot B_n$$

- $B_n$  is called the *noise bandwidth* of the filter.
- For a single-pole filter  $H(s) = \frac{1}{1+s/\omega_o}$ ,

$$B_n = \int_0^{\infty} |H(j2\pi f)|^2 df = \int_0^{\infty} \frac{1}{1 + \left(\frac{f}{f_o}\right)^2} df = \frac{\pi}{2} \cdot f_o$$

# Noise Summation

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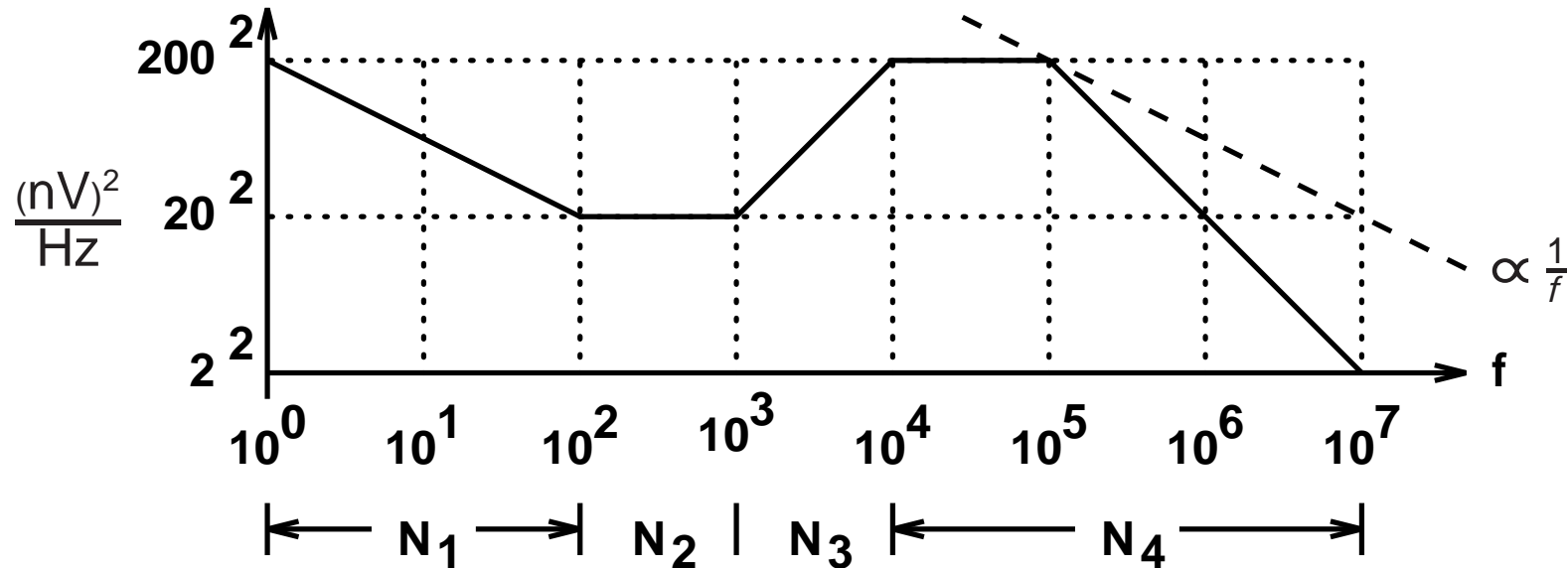


If two noises,  $n_i$  and  $n_j$ , are uncorrelated then, i.e.,  $\overline{n_i \cdot n_j} = 0$ . Then

$$\overline{n_{o1}^2} = \overline{(n_{i1} + n_{i2})^2} = \overline{n_{i1}^2} + \overline{n_{i2}^2} + 2 \cdot \overline{n_{i1}n_{i2}} = \overline{n_{i1}^2} + \overline{n_{i2}^2}$$

$$SD_{n_{o2}}(f) = |H_1(j2\pi f)|^2 SD_{n_{i1}} + |H_2(j2\pi f)|^2 SD_{n_{i2}} + |H_3(j2\pi f)|^2 SD_{n_{i3}}$$

# Piecewise Integration of Noise



The noise power in each frequency region is

$$P_{N_1} = \int_{10^0}^{10^2} \frac{200^2}{f} df = 200^2 \ln(f) \Big|_{10^0}^{10^2} = 1.84 \times 10^5 (nV)^2$$

$$P_{N_2} = \int_{10^2}^{10^3} 20^2 df = 20^2 f \Big|_{10^2}^{10^3} = 3.6 \times 10^5 (nV)^2$$

## Piecewise Integration of Noise

---

$$P_{N_3} = \int_{10^3}^{10^4} \left(\frac{20}{10^3}\right)^2 f^2 df = \left(\frac{20}{10^3}\right)^2 \frac{1}{3} f^3 \Big|_{10^3}^{10^4} = 1.33 \times 10^8 \text{ (nV)}^2$$

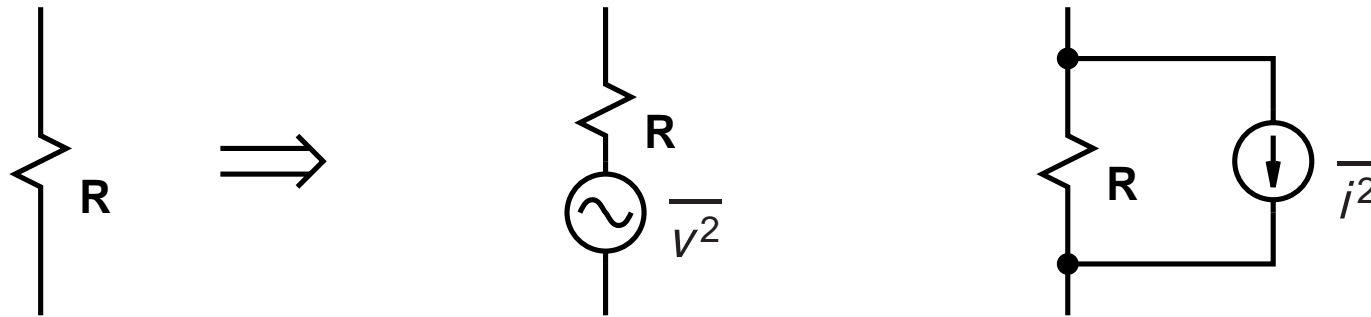
$$\begin{aligned} P_{N_4} &= \int_{10^4}^{\infty} \frac{200^2}{1 + \left(\frac{f}{10^5}\right)^2} df = \int_0^{\infty} \frac{200^2}{1 + \left(\frac{f}{10^5}\right)^2} df - \int_0^{10^4} 200^2 df \\ &= 200^2 \left(\frac{\pi}{2}\right) 10^5 - 200^2 \cdot 10^4 = 5.88 \times 10^9 \text{ (nV)}^2 \end{aligned}$$

Total rms of the noise is

$$n_{\text{rms}} = \left(P_{N_1} + P_{N_2} + P_{N_3} + P_{N_4}\right)^{1/2} = 77.5 \mu\text{V rms}$$

- $1/f$  noise tangent principle: Lower a  $1/f$  line until it touches the spectral density curve; the total noise can be approximated by the noise in the vicinity of the  $1/f$  line.

# Thermal Noise



$$\frac{\overline{v^2}}{\Delta f} = 4kTR$$

$$\frac{\overline{i^2}}{\Delta f} = 4kT \frac{1}{R}$$

$$f = 0 \sim \infty$$

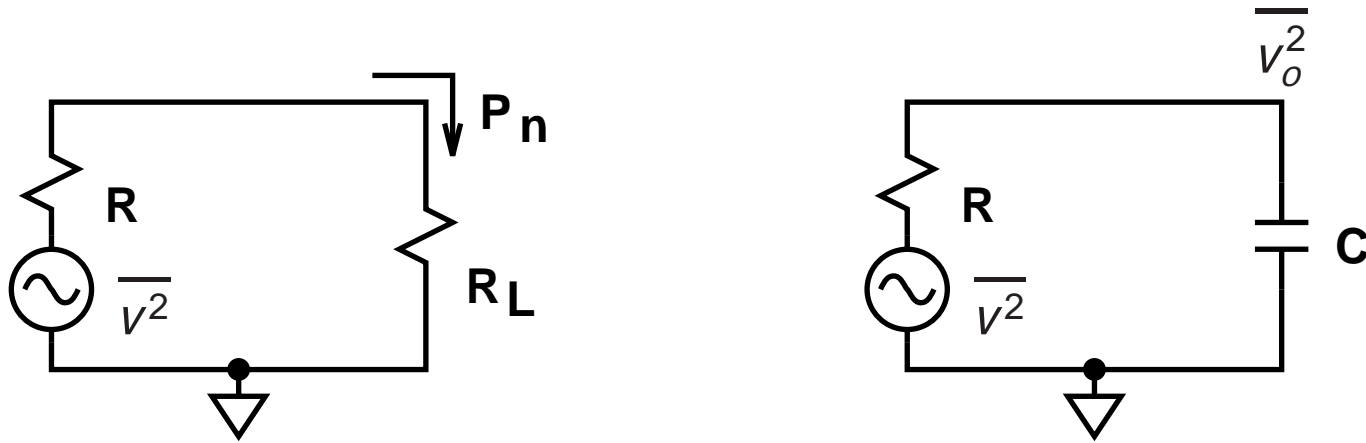
$T$  = Absolute Temperature in Kelvins

$k$  =  $1.38 \times 10^{-23}$  watt/K-Hz (Boltzmann's Constant)

$\Delta f$  = Bandwidth per Hertz

- Thermal noise is a white noise, i.e., its power spectral density  $\overline{v^2}/\Delta f$  is independent of frequency, and its amplitude distribution is Gaussian.
- For a 1 k $\Omega$  resistor at 300 $^\circ$ K,  $\overline{v^2}/\Delta f \approx (4 \text{ nV}/\sqrt{\text{Hz}})^2$ .

# Thermal Noise with Loading



- The  $R_L$  load receives the maximum power if  $R_L = R$ . Thus the available noise power for  $R_L$  is

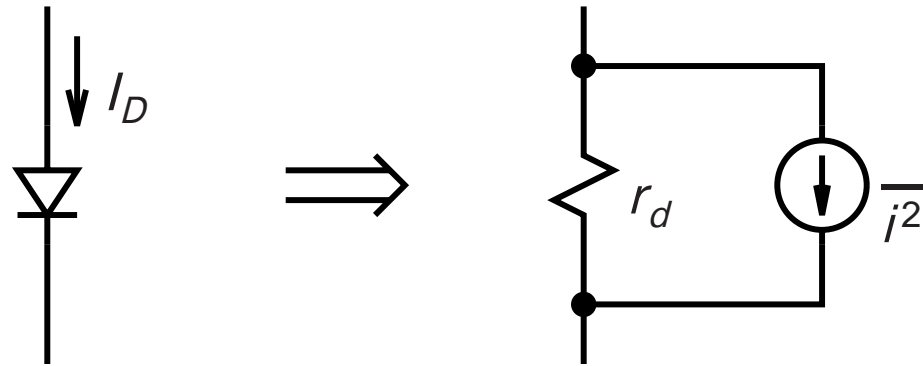
$$P_n = \frac{1}{4R} \cdot \overline{v^2} \cdot B_n = kTB_n \quad B_n = \text{Noise Bandwidth}$$

- For the RC low-pass network

$$B_n = \frac{\pi}{2} \cdot \frac{1}{2\pi RC} = \frac{1}{4RC} \quad \overline{v_o^2} = 4kTR \cdot \frac{1}{4RC} = \frac{kT}{C}$$

If  $C = 1 \text{ pF}$  and  $T = 300 \text{ }^\circ\text{K}$ ,  $\overline{v_o^2} = (64 \text{ } \mu\text{V})^2$

# Shot Noise



$$r_d = \frac{kT}{qI_D} \quad \overline{i^2} = 2qI_D \Delta f \quad f = 0 \sim \infty$$

$$q = 1.6 \times 10^{-19} \text{ C (Electronic Charge)}$$

$$kT/q = U_T \approx 26 \text{ mV at } T = 300^\circ\text{K}$$

- Shot noise is also a white noise.
- The shot noise from a diode with  $50 \mu\text{A}$  bias current is the same as the thermal noise from a  $1 \text{ k}\Omega$  resistor at room temperature.

## Flicker Noise ( $1/f$ Noise)

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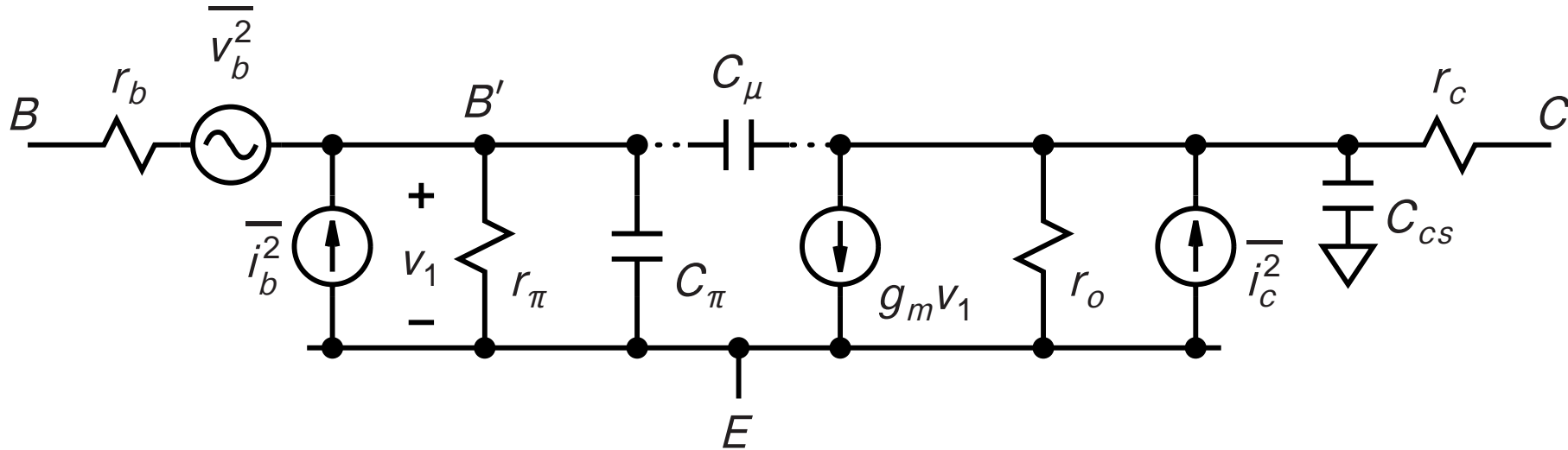
- Flicker noise, which is always associated with a flow of direct current, displays a spectral density of the form

$$\frac{\overline{i^2}}{\Delta f} = K_1 \frac{I^a}{f^b} \quad f = 0 \sim \infty$$

$$a \approx 0.5 \sim 2 \quad b \approx 1 \quad K_1 = \text{a constant for a particular device}$$

- The flicker noise's power spectral density is frequency dependent, and its amplitude distribution is non-Gaussian.
- Flicker noise is caused mainly by traps associated with contamination and crystal defects. The constant  $K_1$  can vary widely even for devices from the same wafer.

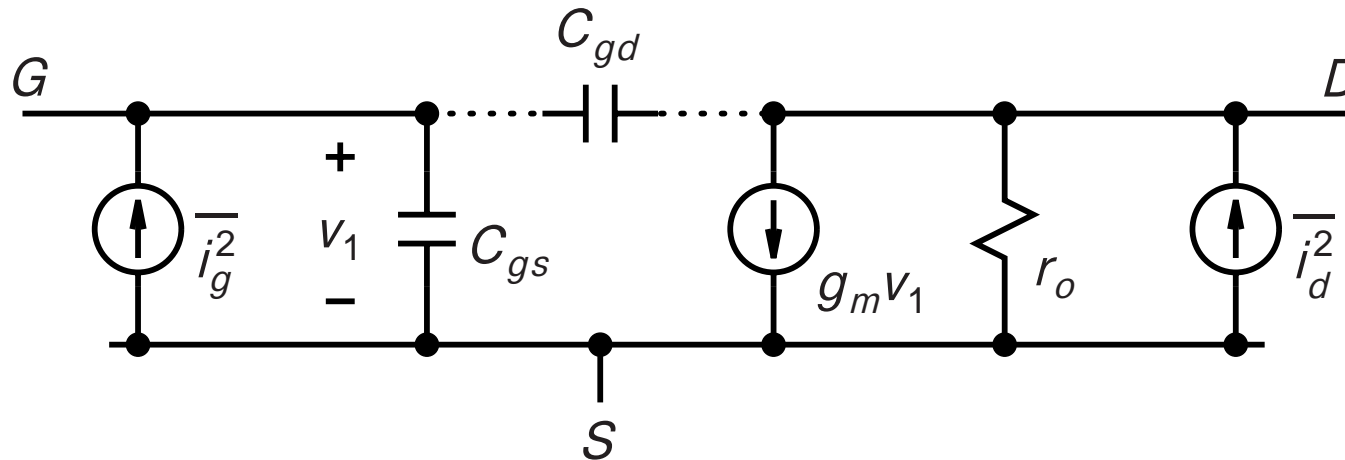
## BJT Noise Model



$$\frac{\overline{v_b^2}}{\Delta f} = 4kTr_b \quad \frac{\overline{i_c^2}}{\Delta f} = 2qI_C \quad \frac{\overline{i_b^2}}{\Delta f} = 2qI_B + K_1 \frac{I_B^a}{f}$$

- All noise sources are independent of each other.
- The thermal noise of  $r_c$  is neglected.
- Avalanche noise is found to be negligible if  $V_{CE}$  is kept at least 5 V below  $BV_{CEO}$ .
- $C_\mu$  can be neglected in noise calculation.

# FET Noise Model



$$\frac{\overline{i_g^2}}{\Delta f} = 2qI_G + \frac{16}{15}kT\omega^2 C_{gs}^2 \quad \frac{\overline{i_d^2}}{\Delta f} = 4kT(\gamma g_{d0}) + K_1 \frac{I_D^a}{f}$$

- Since the channel material is resistive, it exhibits thermal noise.  $\gamma$  is a constant,  $g_{d0}$  is the channel conductance at  $V_{DS} = 0$ .

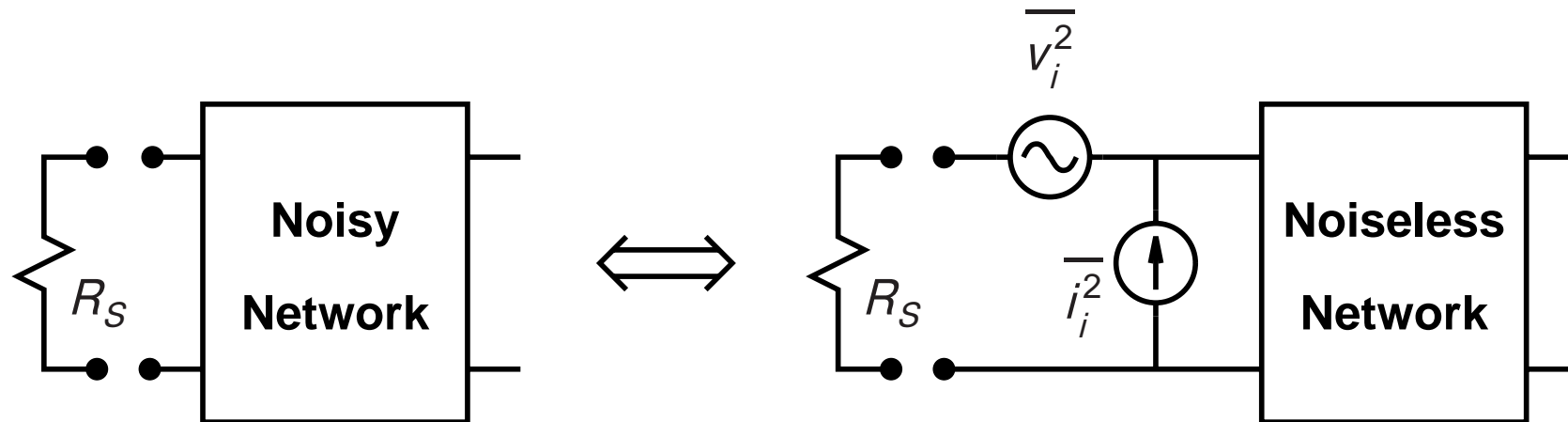
$$\gamma \approx \frac{2}{3} \quad g_{d0} \approx g_m$$

# FET Noise Model

---

- For short-channel device ( $L < 1 \mu\text{m}$ ), the thermal noise is 2 to 5 times larger than  $4kT(2/3)g_m$ .
- The gate-current noise,  $(16/15)kT\omega^2C_{gs}^2$ , is usually insignificant at low frequencies. Its correlation with the thermal noise is 0.39.
- $I_G$  is the gate leakage current.
- $C_{gd}$  can be neglected in noise calculation.
- The  $1/f$  noise in the surface devices, such as MESFETs and MOSFETs, is usually larger than that of BJTs.
- pMOSTs have less  $1/f$  noise than nMOSTs, since holes are less likely to be trapped.

# Equivalent Input Noise Generators



- The noise in network is lumped and represented by a noise voltage generator  $\overline{v_i^2}$  and a noise current generator  $\overline{i_i^2}$ . This representation is valid for any source impedance, if correlation between the noise generators is considered.
- And the total input equivalent noise can be found by

$$V_{iN} = V_s + V_i + i_i R_S \quad \text{and} \quad \overline{v_{iN}^2} = \overline{v_s^2} + \overline{v_i^2} + \overline{i_i^2} R_S^2$$

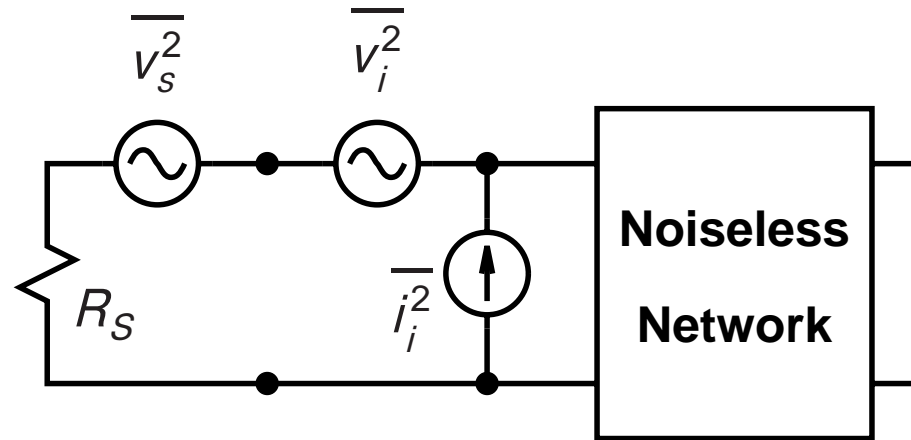
# Equivalent Input Noise Generators

---

- In most practical circuits, the correlation between  $v_i$  and  $i_i$  is small and may be neglected. If either  $\overline{v_i^2}$  or  $\overline{i_i^2}$  dominates, the correlation may be neglected in any case.
- The value of  $\overline{v_i^2}$  can be found by *shorting* the input ports and equating the output noise in each case.
- The value of  $\overline{i_i^2}$  can be found by *opening* the input ports and equating the output noise in each case.

# Noise Factor and Input Noise Generators

---



$\overline{v_s^2}$  is the thermal noise of  $R_S$ , i.e.,

$$\overline{v_s^2} = 4kTR_S\Delta f$$

Assume no correlation between  $\overline{v_i^2}$  and  $\overline{i_i^2}$ , we have

$$\frac{N_a}{N_i} = \frac{\overline{v_i^2} + \overline{i_i^2}R_S^2}{\overline{v_s^2}}$$

# Noise Factor and Input Noise Generators

---

Thus, the noise factor for the two-port network is

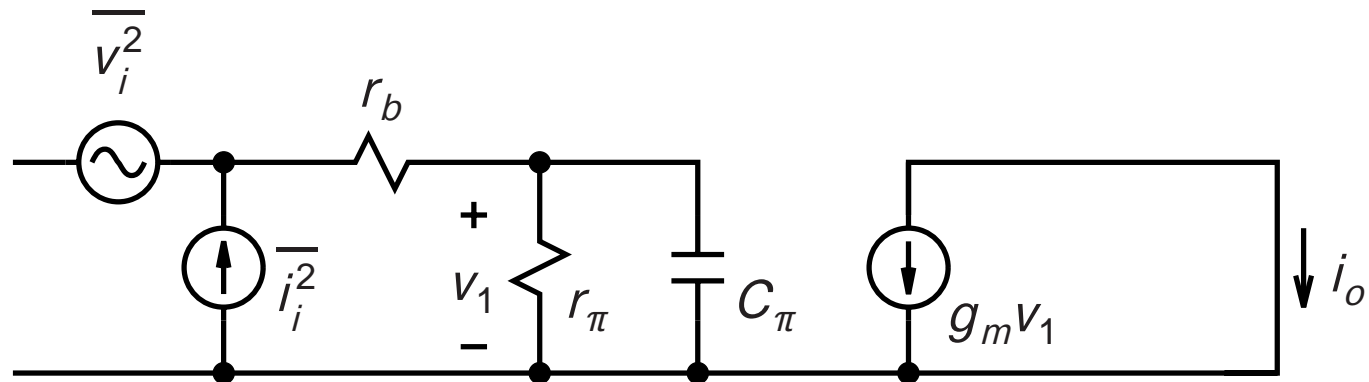
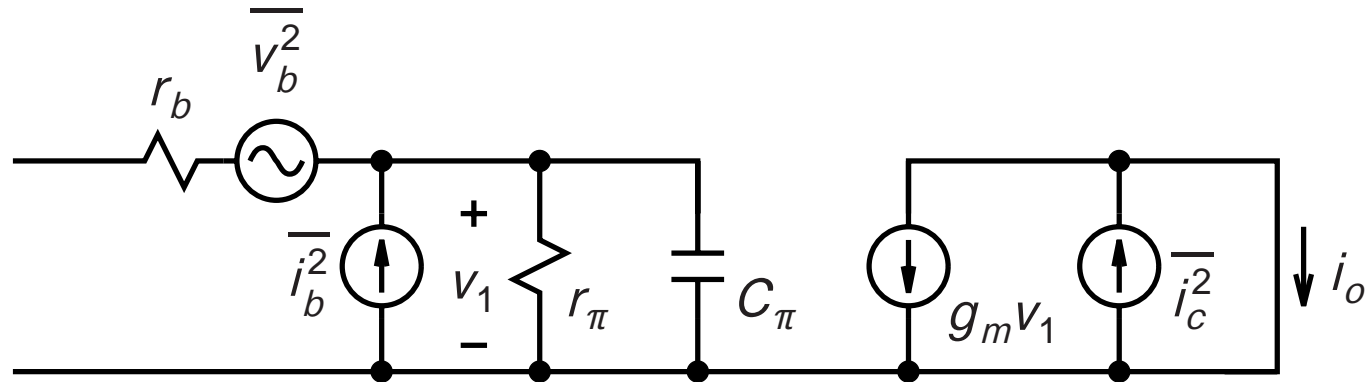
$$F = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_{\text{out}}} = \frac{S_i/N_i}{(G \cdot S_i)/[G \cdot (N_i + N_a)]} = 1 + \frac{N_a}{N_i} = 1 + \frac{\overline{v_i^2}}{4kTR_S\Delta f} + \frac{\overline{i_i^2}R_S}{4kT\Delta f}$$

- For small  $R_S$ ,  $\overline{v_i^2}$  dominates, whereas for large  $R_S$ ,  $\overline{i_i^2}$  dominates.
- There exists an optimal  $R_S$  for minimum  $F$ :

$$R_{S,opt}^2 = \frac{\overline{v_i^2}}{\overline{i_i^2}} \quad \text{and} \quad F_{opt} = 1 + \frac{\overline{i_i^2}R_S}{2kT\Delta f}$$

This is one reason for the widespread use of transformers at the input of low-noise tuned amplifiers.

# Noise Generators of a BJT Common-Emitter Stage



$$\frac{\overline{v_b^2}}{\Delta f} = 4kTr_b$$

$$\frac{\overline{i_b^2}}{\Delta f} = 2qI_B + K_1 \frac{I_B^a}{f}$$

$$\frac{\overline{i_c^2}}{\Delta f} = 2qI_C$$

# Noise Voltage Generator of a BJT Common-Emitter Stage

---

By shorting the input ports, we obtain

$$i_o = g_m v_b + i_c = g_m v_i$$

Since  $r_b$  is small,  $\overline{i_b^2}$  is neglected. We have

$$v_i = v_b + \frac{i_c}{g_m} \qquad \overline{v_i^2} = \overline{v_b^2} + \frac{\overline{i_c^2}}{g_m^2}$$

$$\frac{\overline{v_i^2}}{\Delta f} = 4kT r_b + \frac{2qI_C}{g_m^2} = 4kT \left( r_b + \frac{I_C/U_T}{2g_m^2} \right) = 4kT \left( r_b + \frac{1}{2g_m} \right) = 4kT R_{eq}$$

$$R_{eq} = \text{Equivalent Input Noise Resistance} = r_b + \frac{1}{2g_m}$$

# Noise Current Generator of a BJT Common-Emitter Stage

---

By opening the input ports, we obtain

$$i_o = \beta(j\omega)i_b + i_c = \beta(j\omega)i_i \quad \Rightarrow \quad i_i = i_b + \frac{i_c}{\beta(j\omega)} \quad \overline{i_i^2} = \overline{i_b^2} + \frac{\overline{i_c^2}}{|\beta(j\omega)|^2}$$

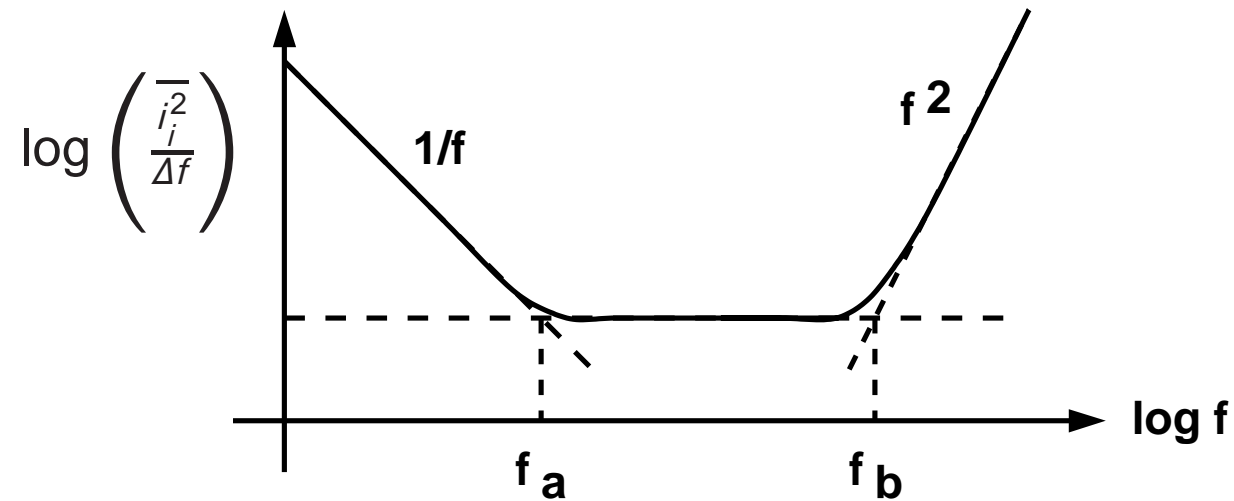
Thus

$$\frac{\overline{i_i^2}}{\Delta f} = 2q \left[ I_B + K'_1 \frac{I_B^a}{f} + \frac{I_C}{|\beta(j\omega)|^2} \right] = 2q I_{eq} \quad K'_1 = \frac{K_1}{2q}$$

$$I_{eq} = \text{Equivalent Input Shot Noise Current} = I_B + K'_1 \frac{I_B^a}{f} + \frac{I_C}{|\beta(j\omega)|^2}$$

$$\beta(j\omega) = \frac{\beta_o}{1 + j\frac{\omega}{\omega_\beta}} = \frac{\beta_o}{1 + j\frac{f}{f_T}\beta_o} = \frac{\beta_o}{1 + \beta_o \frac{C_\pi + C_\mu}{g_m} j\omega}$$

# BJT Equivalent Input Shot Noise Spectral Density



At high frequencies

$$\frac{I_C}{|\beta(j\omega)|^2} = \frac{I_C}{\beta_o^2} \left( 1 + \frac{f^2}{f_T^2} \beta_o^2 \right) \approx I_C \frac{f^2}{f_T^2}$$

$$\text{Let } I_B = I_C \frac{f_b^2}{f_T^2} \quad \Rightarrow \quad f_b = f_T \sqrt{\frac{I_B}{I_C}} = \frac{f_T}{\sqrt{\beta_F}}$$

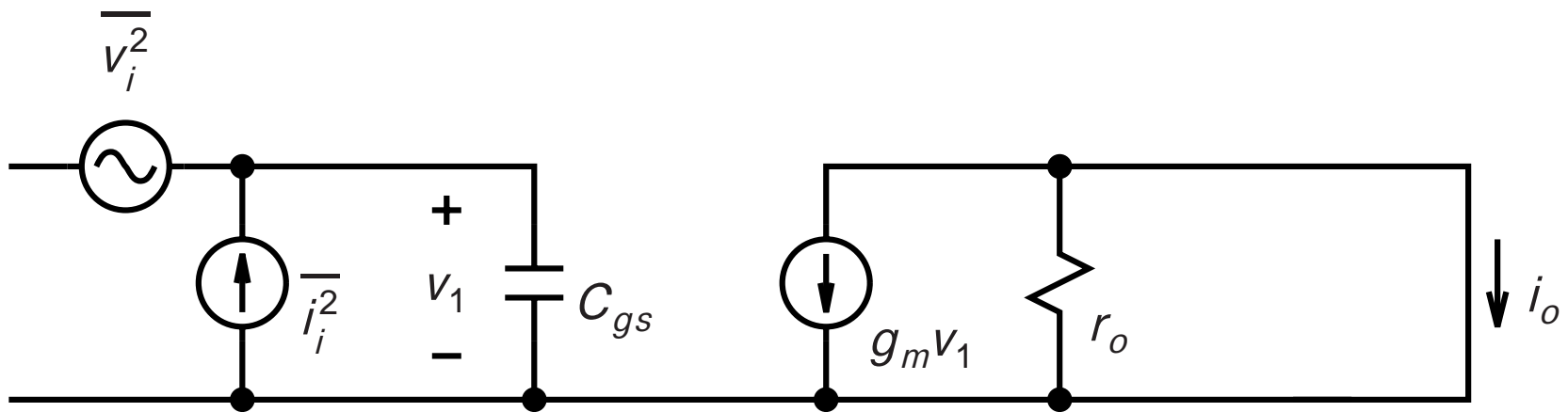
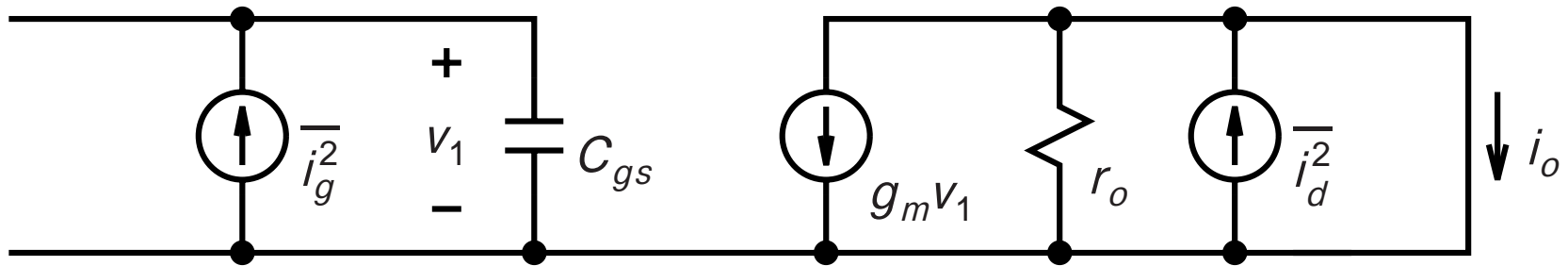
# Total Equivalent Noise Voltage of a BJT Common-Emitter Stage

---

The total equivalent noise voltage with a source resistance  $R_S$  can be found as

$$\begin{aligned}\overline{\frac{v_{iN}^2}{\Delta f}} &= \overline{\frac{v_s^2}{\Delta f}} + \overline{\frac{v_i^2}{\Delta f}} + \overline{\frac{i_i^2}{\Delta f}} R_S^2 \\ &= 4kT \left( R_S + r_b + \frac{1}{2g_m} \right) + R_S^2 \cdot 2q \left( I_B + K'_1 \frac{I_B^a}{f} + \frac{I_C}{|\beta(j\omega)|^2} \right) \\ &= 4kT \left[ \left( R_S + r_b + \frac{1}{2g_m} \right) + \frac{R_S^2}{2U_T} \left( I_B + K'_1 \frac{I_B^a}{f} + \frac{I_C}{|\beta(j\omega)|^2} \right) \right] \\ &= 2qR_S^2 \left[ \frac{2U_T}{R_S^2} \left( R_S + r_b + \frac{1}{2g_m} \right) + \left( I_B + K'_1 \frac{I_B^a}{f} + \frac{I_C}{|\beta(j\omega)|^2} \right) \right]\end{aligned}$$

# Noise Generators of a FET Common-Source Stage



$$\frac{\overline{i_g^2}}{\Delta f} = 2qI_G + \frac{16}{15}kT\omega^2 C_{gs}^2$$

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT(\gamma g_{d0}) + K_1 \frac{I_D^a}{f}$$

# Noise Voltage Generator of a FET Common-Source Stage

---

By shorting the input ports, we obtain

$$i_o = i_d = g_m v_i \quad \Rightarrow \quad \overline{v_i^2} = \frac{\overline{i_d^2}}{g_m^2}$$

$$\frac{\overline{v_i^2}}{\Delta f} = 4kT\gamma \frac{g_{d0}}{g_m^2} + K_1 \frac{I_D^a}{g_m^2 f} = 4kT R_{eq} \quad K'_1 = \frac{K_1}{4kT}$$

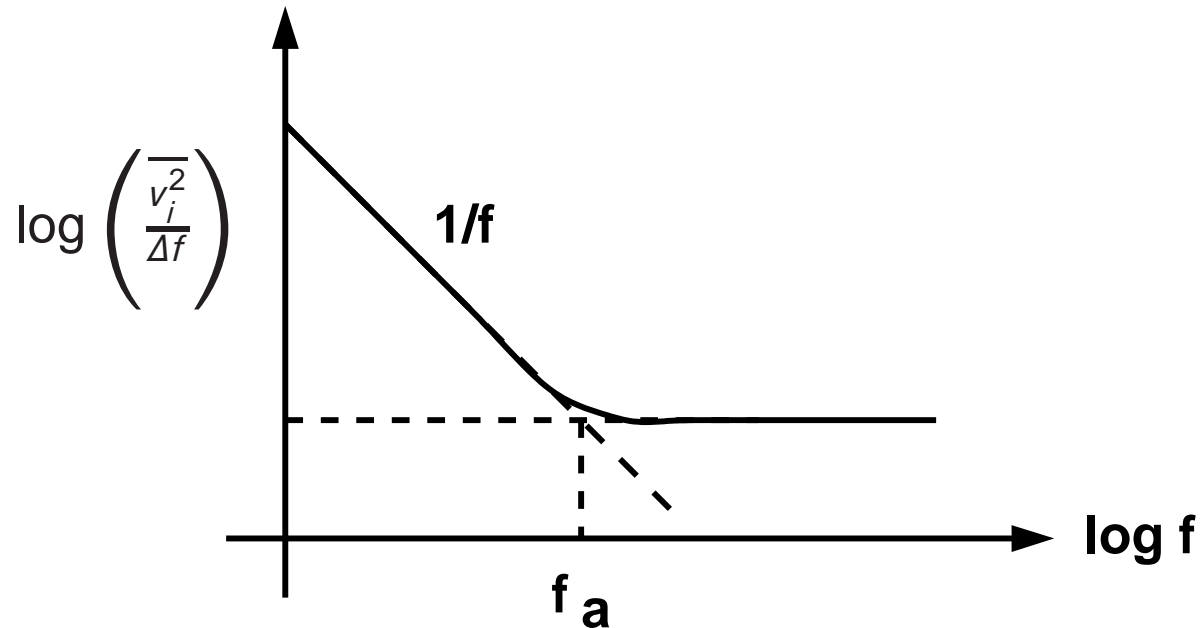
$$R_{eq} = \text{Equivalent Input Noise Resistance} = \gamma \frac{g_{d0}}{g_m^2} + K'_1 \frac{I_D^a}{g_m^2 f} \approx \frac{2}{3} \frac{1}{g_m} + K'_1 \frac{I_D^a}{g_m^2 f}$$

- For MOST, its voltage generator for flicker noise is approximately independent of bias current and voltage and is inversely proportional to the gate-oxide capacitance, i.e.,

$$\frac{\overline{v_i^2}}{\Delta f} \approx 4kT \left( \frac{2}{3} \frac{1}{g_m} \right) + \frac{K_f}{WLC_{ox}} \cdot \frac{1}{f} \quad K_f \sim 3 \times 10^{-24} \text{ V}^2\text{-F}$$

# MOST Equivalent Input Noise Voltage Spectral Density

---



- At frequencies above the flicker noise region, the  $R_{eq}$  of a FET is significantly higher than that of a BJT at a comparable bias current.
- For a MOST, it is not uncommon for the  $f_a$  to extend well into the MHz region.

# Noise Current Generator of a FET Common-Source Stage

---

By opening the input ports, we obtain

$$i_o = i_g \frac{g_m}{j\omega C_{gs}} + i_d = i_i \frac{g_m}{j\omega C_{gs}} \quad \Rightarrow \quad i_i = i_g + \frac{j\omega C_{gs}}{g_m} i_d \quad \overline{i_i^2} = \overline{i_g^2} + \frac{\omega^2 C_{gs}^2}{g_m^2} \overline{i_d^2}$$

$$\frac{\overline{i_i^2}}{\Delta f} = 2qI_G + \frac{16}{15}kT\omega^2 C_{gs}^2 + \frac{\omega^2 C_{gs}^2}{g_m^2} \left( 4kT\gamma g_{d0} + K_1 \frac{I_D^a}{f} \right) = 2qI_G + \omega^2 C_{gs}^2 (4kTR_{eq})$$

$$R_{eq} = \gamma \frac{g_{d0}}{g_m^2} + \frac{K_1}{4kT g_m^2} \cdot \frac{I_D^a}{f} + \frac{4}{15} \approx \frac{2}{3} \frac{1}{g_m} + \frac{K_1'}{g_m^2} \cdot \frac{I_D^a}{f} + \frac{4}{15}$$

- When the source impedance is large,  $\overline{i_i^2}$  dominates. Since  $I_G$  is very small, FETs have noise performance much superior to that of BJTs. However, for low source impedances where  $\overline{v_i^2}$  dominates, BJTs often have noise performance superior to that of FETs.

# Noise Factor of a BJT Common-Emitter Stage

---

Neglecting flicker noise,

$$\frac{\overline{v_i^2}}{\Delta f} = 4kT \left( r_b + \frac{1}{2g_m} \right) \quad \frac{\overline{i_i^2}}{\Delta f} = 2q \left( I_B + \frac{I_C}{|\beta(j\omega)|^2} \right) = 2q \left( \frac{I_C}{\beta_F} + \frac{I_C}{|\beta(j\omega)|^2} \right)$$

The noise factor is

$$\begin{aligned} F &= 1 + \frac{\overline{v_i^2}}{4kTR_S\Delta f} + \frac{\overline{i_i^2}}{4kT\frac{1}{R_S}\Delta f} \\ &= 1 + \frac{1}{R_S} \left( r_b + \frac{1}{2g_m} \right) + R_S \left( \frac{g_m}{2\beta_F} + \frac{g_m}{2|\beta(j\omega)|^2} \right) \\ &= 1 + \frac{1}{R_S} \left( r_b + \frac{1}{2g_m} \right) + R_S \left[ \frac{g_m}{2\beta_F} + \frac{g_m}{2\beta_o^2} \left( 1 + \beta_o^2 \left( \frac{\omega}{\omega_T} \right)^2 \right) \right] \end{aligned}$$

# Noise Factor of a BJT Common-Emitter Stage

---

For high-frequency circuits, if  $\omega/\omega_T \gg 1/\beta_o$  and  $\omega/\omega_T \gg 1/\beta_F$ ,

$$F \approx 1 + \frac{1}{R_S} \cdot \left( r_b + \frac{1}{2g_m} \right) + R_S \cdot \frac{g_m}{2} \cdot \left( \frac{\omega}{\omega_T} \right)^2$$

- For fixed  $R_S$  and  $\omega_T$ ,

$$g_{m,opt} = \frac{1}{R_S} \cdot \frac{\omega_T}{\omega} \quad F_{opt} = 1 + \frac{r_b}{R_S} + \frac{\omega}{\omega_T}$$

- For fixed  $g_m$  and  $\omega_T$ ,

$$R_{S,opt} = \sqrt{\frac{2r_b}{g_m} + \frac{1}{g_m^2}} \cdot \frac{\omega_T}{\omega} \quad F_{opt} = 1 + \sqrt{2r_b g_m + 1} \cdot \frac{\omega}{\omega_T}$$

# Noise Factor of a BJT Common-Emitter Stage

---

For low-frequency circuits, if  $\omega/\omega_T \ll 1/\beta_o$  and  $\omega/\omega_T \ll 1/\beta_F$ ,

$$\begin{aligned} F &\approx 1 + \frac{1}{R_S} \cdot \left( r_b + \frac{1}{2g_m} \right) + R_S \cdot \frac{g_m}{2} \cdot \left( \frac{1}{\beta_F} + \frac{1}{\beta_o^2} \right) \\ &\approx 1 + \frac{1}{R_S} \cdot \left( r_b + \frac{1}{2g_m} \right) + R_S \cdot \frac{g_m}{2} \cdot \frac{1}{\beta_F} \end{aligned}$$

- For fixed  $R_S$  and  $\beta_F$ ,

$$g_{m,opt} = \frac{1}{R_S} \cdot \sqrt{\beta_F} \quad F_{opt} = 1 + \frac{r_b}{R_S} + \frac{1}{\sqrt{\beta_F}}$$

- For fixed  $g_m$  and  $\beta_F$ ,

$$R_{S,opt} = \sqrt{\frac{2r_b}{g_m} + \frac{1}{g_m^2}} \cdot \sqrt{\beta_F} \quad F_{opt} = 1 + \sqrt{2r_b g_m + 1} \cdot \frac{1}{\sqrt{\beta_F}}$$

# Noise Factor of an FET Common-Source Stage

---

Neglecting flicker noise,  $I_G$ , and gate-current noise,

$$\overline{\frac{v_i^2}{\Delta f}} = 4kT\gamma g_{d0} \cdot \frac{1}{g_m^2} \quad \overline{\frac{i_i^2}{\Delta f}} = \omega^2 C_{gs}^2 \cdot 4kT\gamma g_{d0} \cdot \frac{1}{g_m^2}$$

The noise factor is

$$\begin{aligned} F &= 1 + \frac{\overline{v_i^2}}{4kTR_S\Delta f} + \frac{\overline{i_i^2}}{4kT\frac{1}{R_S}\Delta f} \\ &= 1 + \frac{1}{R_S} \cdot \frac{\gamma g_{d0}}{g_m^2} + R_S \cdot \omega^2 C_{gs}^2 \cdot \frac{\gamma g_{d0}}{g_m^2} \end{aligned}$$

# Noise Factor of an FET Common-Source Stage

---

For low-frequency circuits,  $\omega C_{gs} \ll 1/R_S$ ,

$$F \approx 1 + \frac{1}{R_S} \cdot \frac{\gamma g_{d0}}{g_m^2}$$

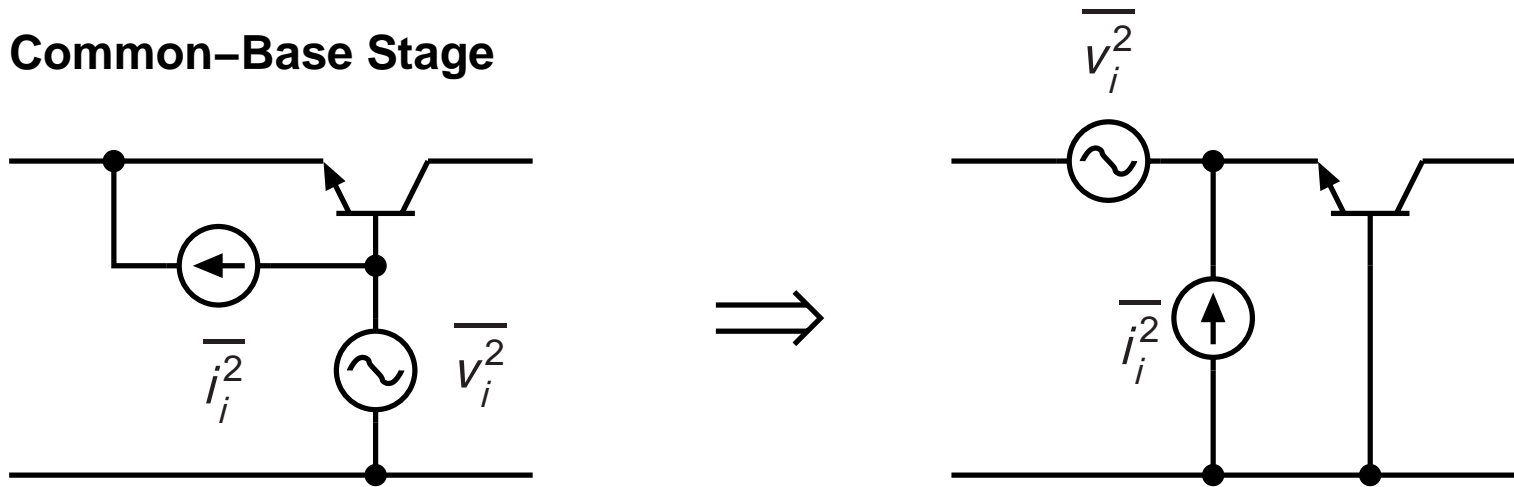
- For fixed  $R_S$ ,  $g_{m,opt} \rightarrow \infty$  and  $F_{opt} \rightarrow 1$
- For fixed  $g_m$ ,  $R_{S,opt} \rightarrow \infty$  and  $F_{opt} \rightarrow 1$
- For  $R_S$  of the order of  $M\Omega$  or higher, the FET usually has significantly lower noise figure than a BJT.

For high-frequency circuits,  $\omega C_{gs} \gg 1/R_S$ ,

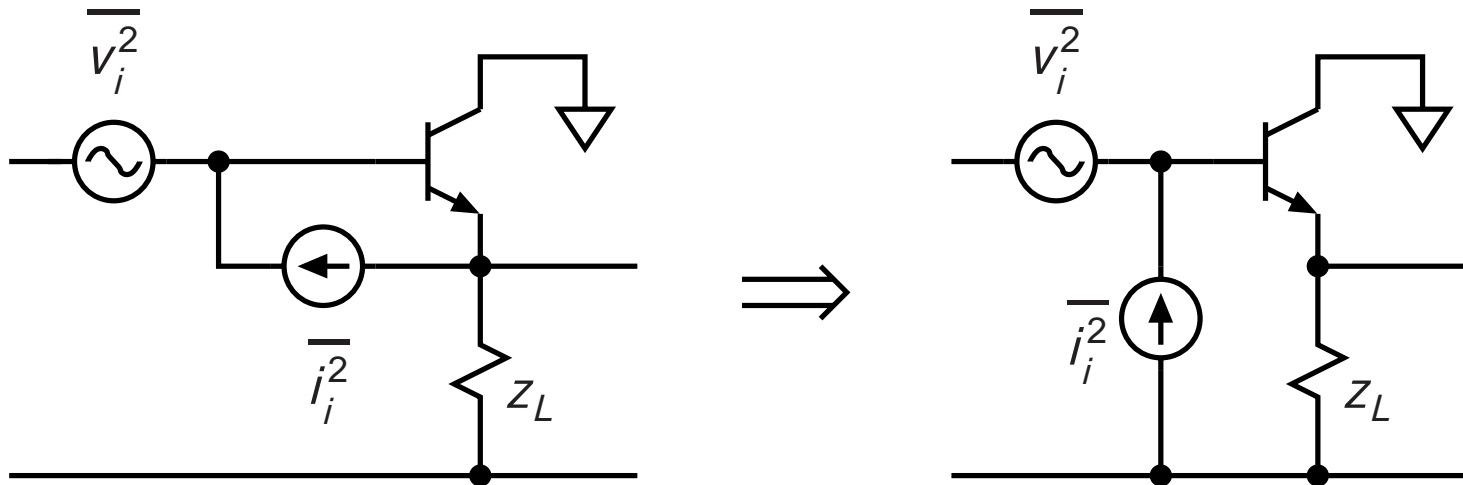
$$F \approx 1 + R_S \cdot \omega^2 C_{gs}^2 \cdot \frac{\gamma g_{d0}}{g_m^2} \approx 1 + R_S \cdot \gamma g_{d0} \cdot \left( \frac{\omega}{\omega_T} \right)^2$$

# Noise Performance of Other Configurations

## Common-Base Stage



## Emitter Follower

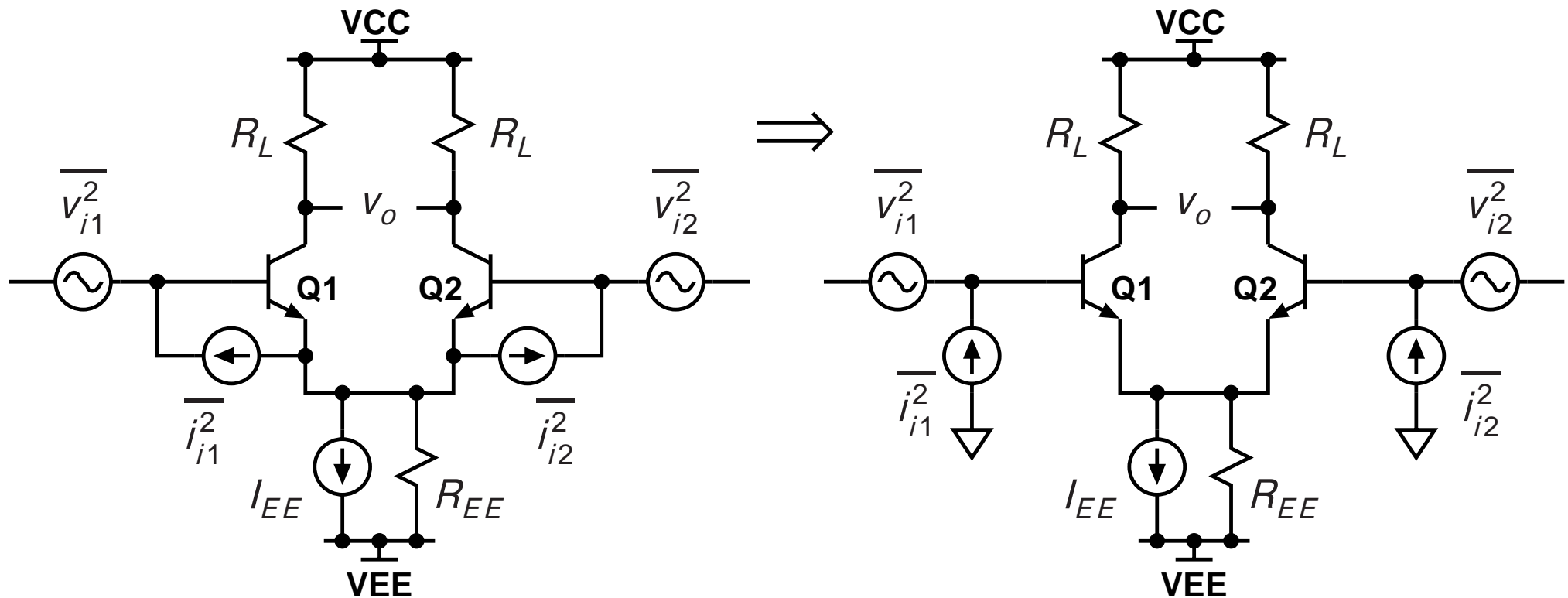


# Noise Performance of Other Configurations

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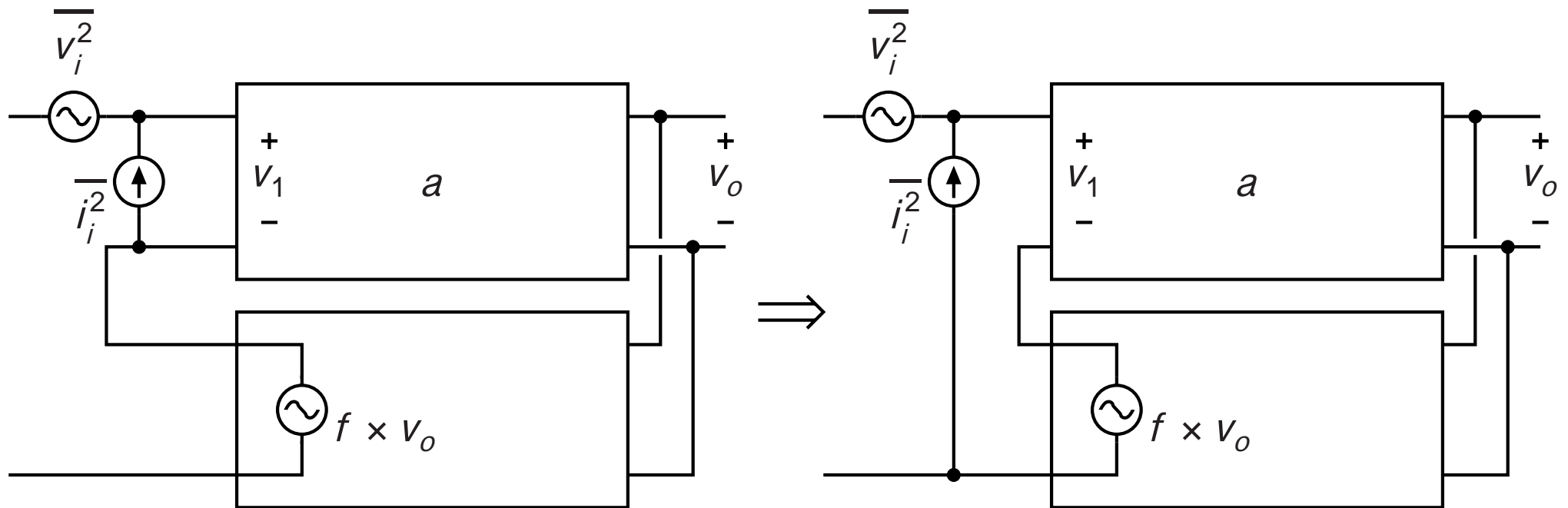
- The equivalent input noise generators of a common-base stage or emitter follower are the same as those of a common-emitter stage.
- For the common-base configuration, since its current gain  $\approx 1$ , any noise current at the output is referred directly back to the input without reduction.
- For the emitter follower, since its voltage gain  $\approx 1$ , any noise voltage at the output, including noise due to  $z_L$ , is transformed unchanged to the input.
- In most low-noise designs, common-emitter connection is used for the input stage.

# Emitter-Coupled Pair Noise Performance



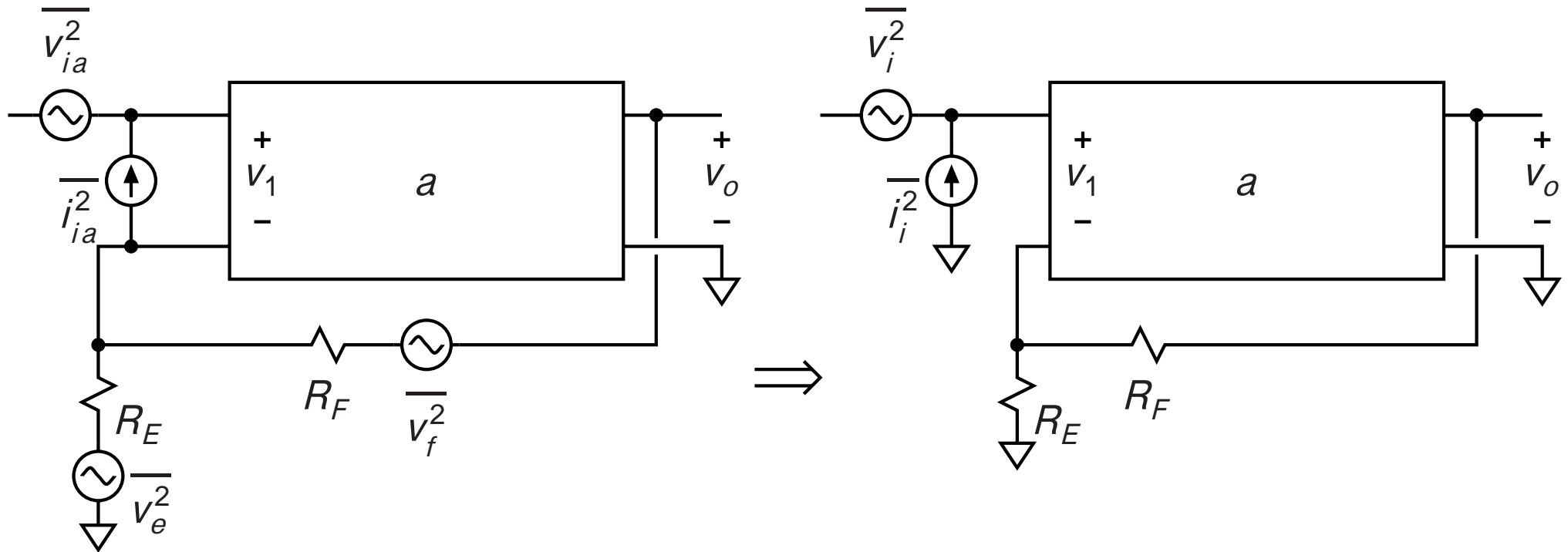
- If the circuit is balanced, the current-source noise represents a common-mode signal and will produce no differential output.

## Effect of Ideal Feedback on Noise Performance



- For ideal feedback systems, the equivalent input noise generators can be moved unchanged outside the feedback loop and the feedback has no effect on the circuit noise performance.

# Effect of Input Series Feedback on Noise Performance

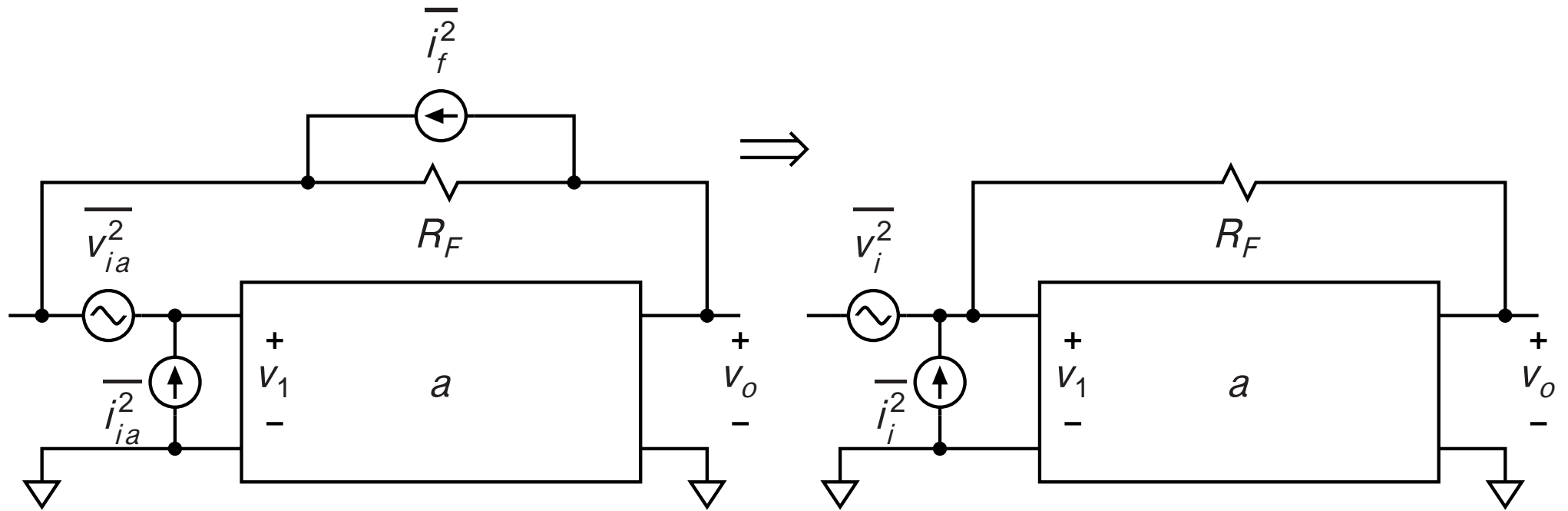


$$\overline{v_f^2} = 4kTR_F\Delta f \quad \overline{v_e^2} = 4kTR_E\Delta f \quad R = R_F || R_E$$

$$V_i = V_{ia} + i_{ia}R + \frac{R_F V_e}{R_F + R_E} + \frac{R_E V_f}{R_F + R_E} \quad i_i \approx i_{ia}$$

$$\Rightarrow \quad \overline{v_i^2} = \overline{v_{ia}^2} + \overline{i_{ia}^2} R^2 + 4kTR\Delta f \quad \overline{i_i^2} \approx \overline{i_{ia}^2}$$

# Effect of Input Shunt Feedback on Noise Performance



$$\overline{i_f^2} = 4kT \frac{1}{R_F} \Delta f$$

$$v_i \approx v_{ia} \quad i_i = i_{ia} + \frac{v_{ia}}{R_F} + i_f$$

$$\Rightarrow \quad \overline{v_i^2} \approx \overline{v_{ia}^2} \quad \overline{i_i^2} = \overline{i_{ia}^2} + \frac{\overline{v_{ia}^2}}{R_F^2} + 4kT \frac{1}{R_F} \Delta f$$

## Effect of Feedback on Noise Performance

---

To analyze the noise performance of a practical feedback system, first use *the loading approximation* according to its feedback configuration to find the loading for the input port due to the feedback network.

For series feedback at the input

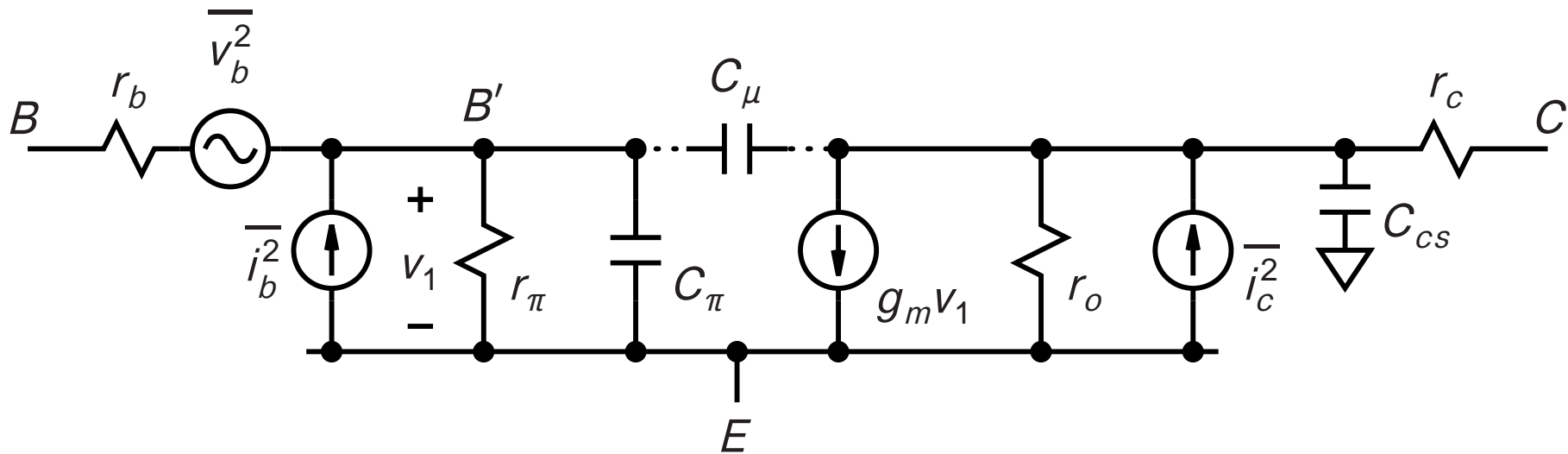
$$\overline{v_i^2} = \overline{v_{ia}^2} + \overline{i_{ia}^2} |Z_{fb}|^2 + 4kTR_{fb}\Delta f \qquad \overline{i_i^2} \approx \overline{i_{ia}^2}$$

For shunt feedback at the input

$$\overline{v_i^2} \approx \overline{v_{ia}^2} \qquad \overline{i_i^2} = \overline{i_{ia}^2} + \frac{\overline{v_{ia}^2}}{|Z_{fb}|^2} + 4kT \frac{1}{R_{fb}} \Delta f$$

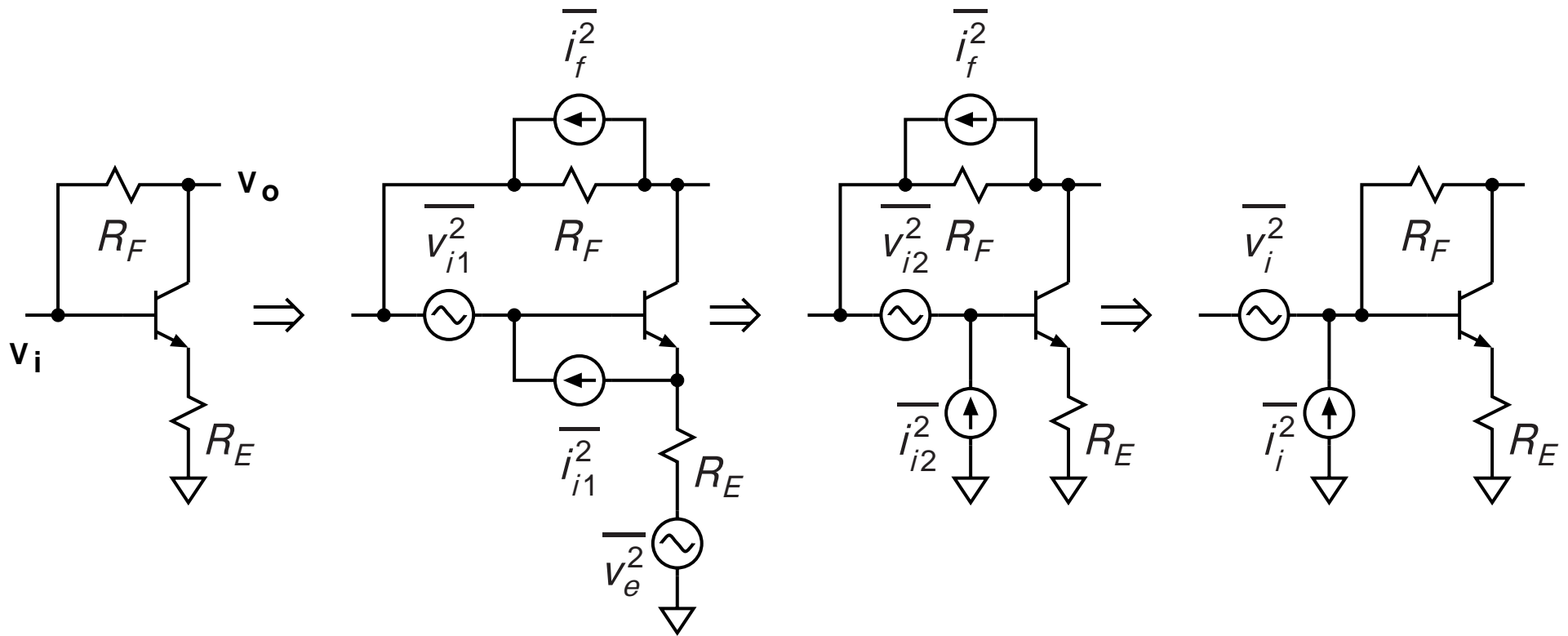
where  $Z_{fb}$  is the loading of the feedback network for the input port, and  $R_{fb}$  represents the resistive part (thermal noise) of the loading.

## Effect of $C_\mu$ on Noise Performance



- Note that the collector-base capacitor  $C_\mu$  represents single-stage shunt feedback, and thus does not significantly affect the equivalent input noise generators of a transistor, even if Miller effect is dominant. The capacitor itself contributes no noise. Also, in calculating  $\overline{i_i^2}$ , the term  $\overline{v_{ia}^2}/|Z_{fb}|^2$  can be neglected, since  $|Z_{fb}| = 1/|\omega C_\mu|$  is quite large at frequencies of interest.

# Single-Stage Amplifier with Local Feedback



$$\frac{\overline{v_{i1}^2}}{\Delta f} \approx 4kT \left( r_b + \frac{1}{2g_m} \right)$$

$$\frac{\overline{v_{i2}^2}}{\Delta f} \approx 4kT \left( r_b + \frac{1}{2g_m} + R_E \right)$$

$$\frac{\overline{v_i^2}}{\Delta f} \approx 4kT \left( r_b + \frac{1}{2g_m} + R_E \right)$$

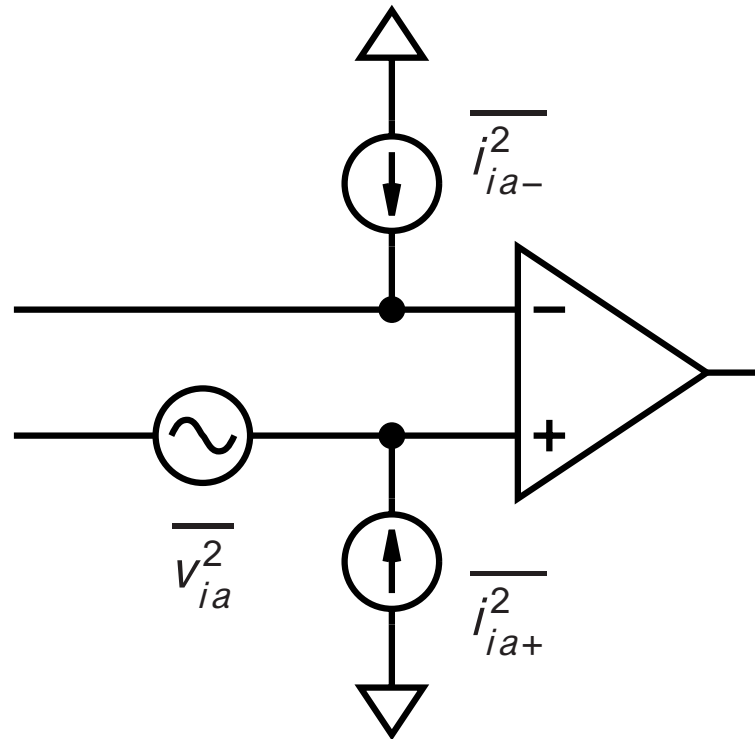
$$\frac{\overline{i_{i1}^2}}{\Delta f} \approx 2qI_B$$

$$\frac{\overline{i_{i2}^2}}{\Delta f} \approx 2qI_B$$

$$\frac{\overline{i_i^2}}{\Delta f} \approx 2qI_B + \frac{4kT}{R_F}$$

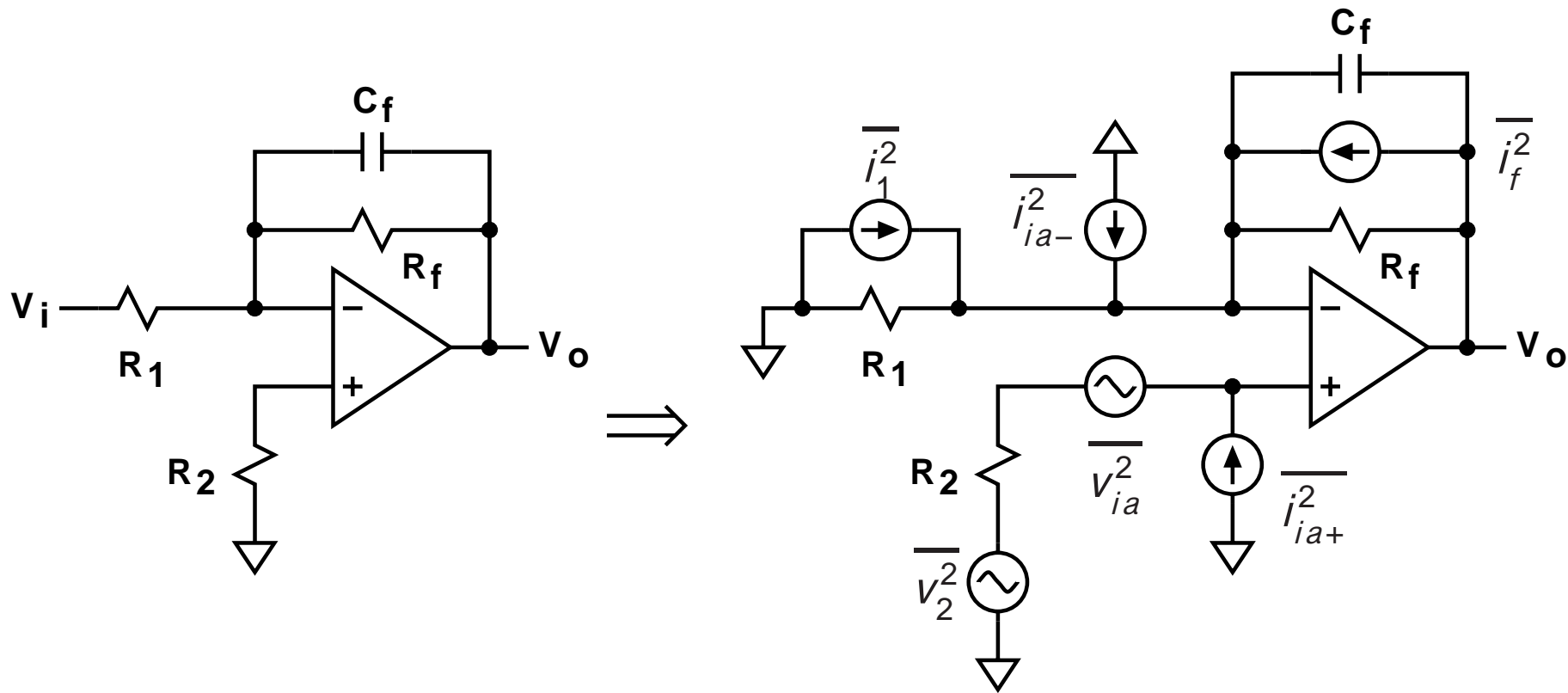
# Operational Amplifier Noise Model

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- With FET input stage, the current noises can often be ignored at low frequencies since their values are small.

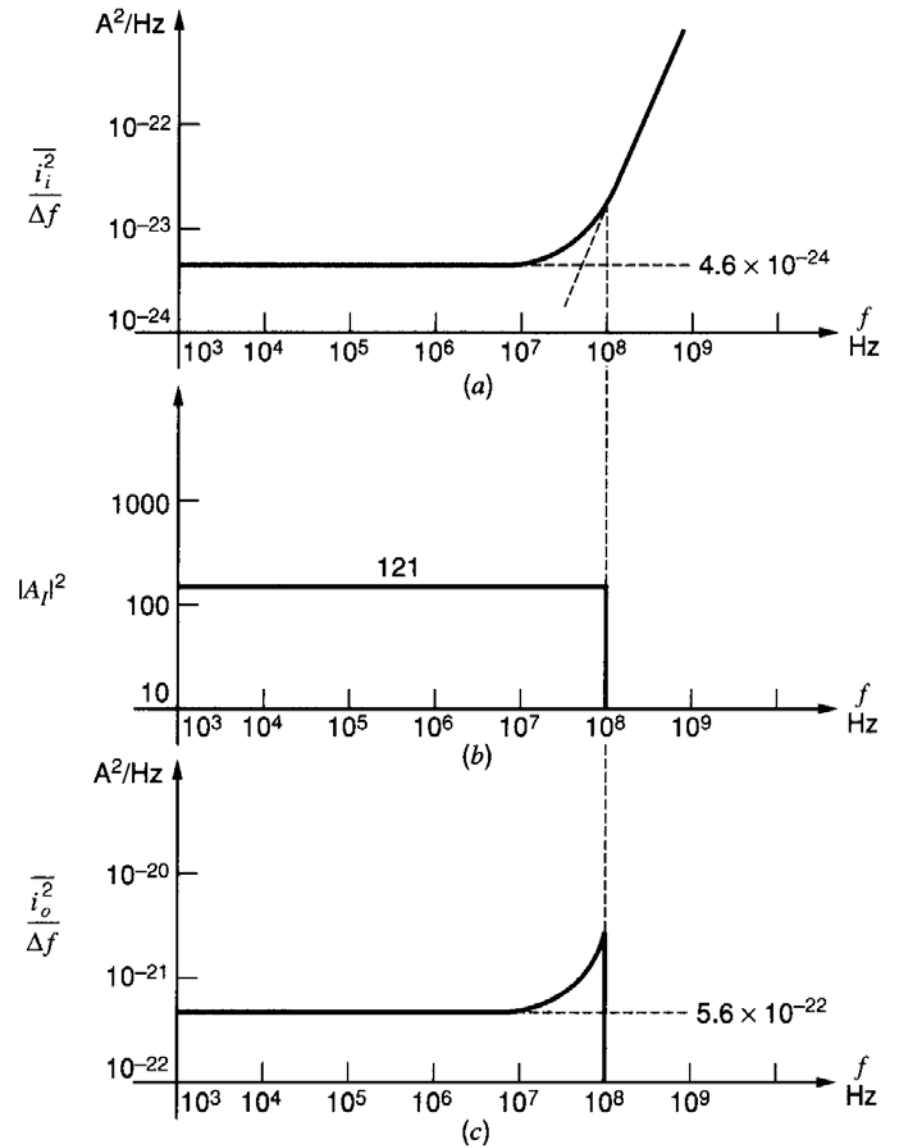
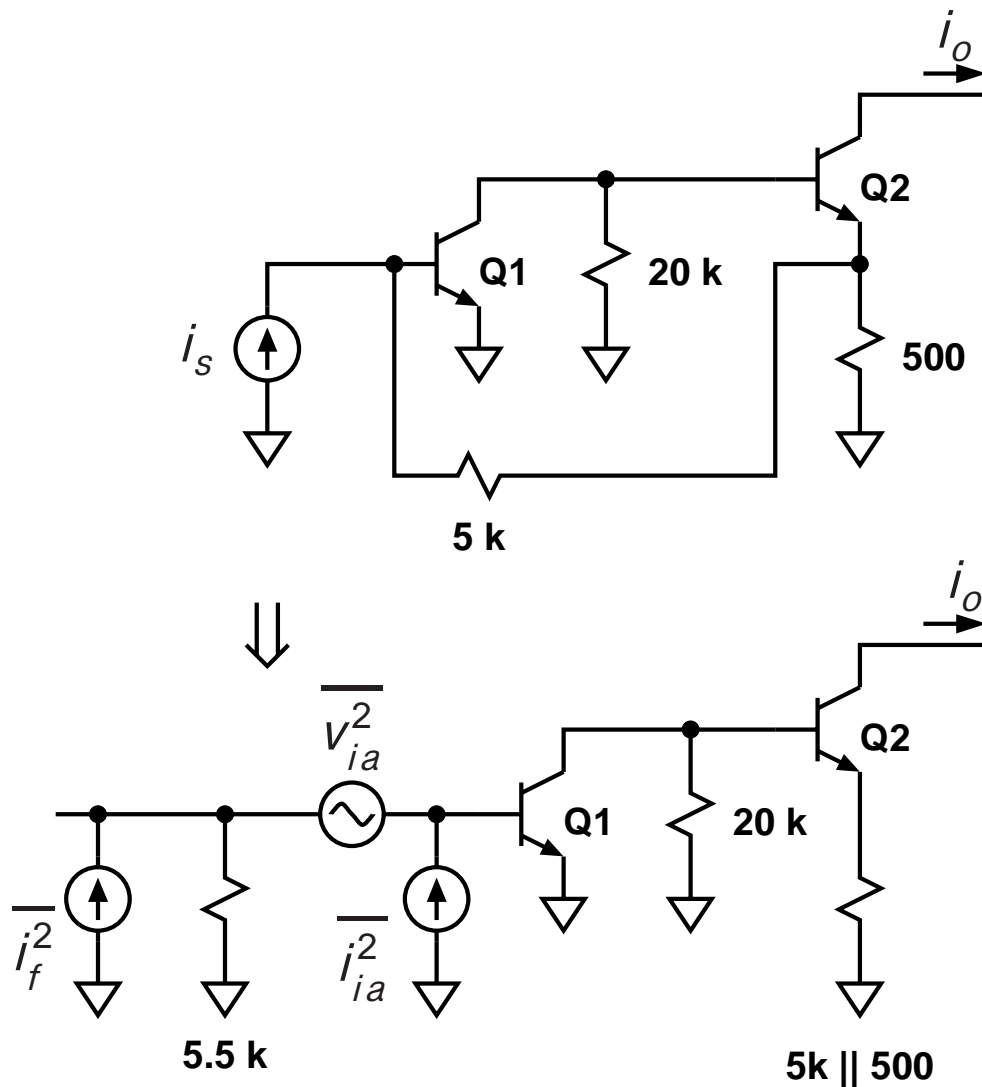
# A Low-Pass Filter Example



$$\overline{V_{o1}^2} = \left( \overline{i_{a-}^2} + \overline{i_1^2} + \overline{i_f^2} \right) \left| \frac{R_f}{1 + j2\pi f R_f C_f} \right|^2 \quad \overline{V_{o2}^2} = \left( \overline{v_{ia}^2} + \overline{i_{a+}^2 R_2^2} + \overline{v_2^2} \right) \left| 1 + \frac{R_f/R_1}{1 + j2\pi f R_f C_f} \right|^2$$

$$\overline{V_{oT}^2} = \overline{V_{o1}^2} + \overline{V_{o2}^2}$$

# A Current Amplifier Example



# A Current Amplifier Example

---

- Neglect flicker noise and assume

$$I_{C1} = 0.5 \text{ mA} \quad I_{C2} = 1 \text{ mA} \quad r_{b1} = r_{b2} = 100 \Omega \quad \beta_1 = \beta_2 = 100$$
$$f_{T1} = 300 \text{ MHz} \quad f_{T2} = 500 \text{ MHz}$$

- For both first and second stages, the driving signals are high-impedance current sources, thus we need to consider only equivalent noise current generators.
- The equivalent noise current from the 2nd stage is approximately

$$2qI_{B2} + 4kT \frac{1}{20 \text{ k}\Omega} = 2q(10 \mu\text{A} + 2.6 \mu\text{A})$$

which can be neglected when compared to  $2qI_{C1} = 2q \times 500 \mu\text{A}$ .

## A Current Amplifier Example

---

- The equivalent input noise current for the amplifier is

$$\begin{aligned}\overline{\frac{i_i^2}{\Delta f}} &= \overline{\frac{i_{ia}^2}{\Delta f}} + \frac{\overline{v_{ia}^2}}{(5.5 \text{ k}\Omega)^2 \Delta f} + \frac{4kT}{5.5 \text{ k}\Omega} \\ &= 2q \left( I_B + \frac{I_C}{|\beta_1|^2} \right) + \frac{4kT}{(5.5 \text{ k}\Omega)^2} \left( r_{b1} + \frac{1}{2g_{m1}} \right) + \frac{4kT}{5.5 \text{ k}\Omega} \\ &= 2q \left( 5 \mu\text{A} + \frac{500 \mu\text{A}}{|\beta_1|^2} \right) + 2q \times 0.2 \mu\text{A} + 2q \times 9.1 \mu\text{A} \\ &= 2q \left( 14.3 + \frac{500}{|\beta_1|^2} \right) \times 10^{-6} \text{ A}^2/\text{Hz}\end{aligned}$$

- We know that

$$\beta(jf) = \frac{\beta_o}{1 + j\frac{\beta_o f}{f_{T1}}} \quad \Rightarrow \quad \frac{1}{|\beta_1(jf)|^2} = \frac{1}{\beta_{o1}^2} \left( 1 + \frac{\beta_{o1}^2 f^2}{f_{T1}^2} \right)$$

## A Current Amplifier Example

---

- The current gain of the amplifier is  $A_i \approx 11$  and is constant up to  $B = 100 \text{ MHz} = f_{T1}/3$ . The total output noise is

$$\begin{aligned}\overline{i_{oT}^2} &= \int_0^B A_i^2 \frac{\overline{i_i^2}}{\Delta f} df = A_i^2 \times \int_0^B 2q \left( 14.3 + \frac{500}{|\beta_1|^2} \right) \times 10^{-6} df \\ &= A_i^2 \times 2q \times 10^{-6} \left[ 14.3f + \frac{500}{\beta_{o1}^2} f + \frac{500f^3}{f_{T1}^2 3} \right]_0^B \\ &= A_i^2 \times 2q \times 10^{-6} \times (14.3B + 18.6B) = A_i^2 \times 1.05 \times 10^{-15} \text{ A}^2\end{aligned}$$

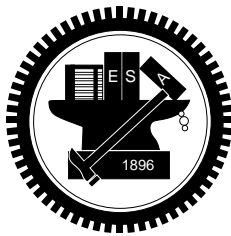
- The equivalent input noise current is

$$\overline{i_{iT}^2} = \frac{\overline{i_{oT}^2}}{A_i^2} \Rightarrow i_{iT} = 32.4 \text{ nA rms}$$

# Feedback and Frequency Compensation

Jieh-Tsorng Wu

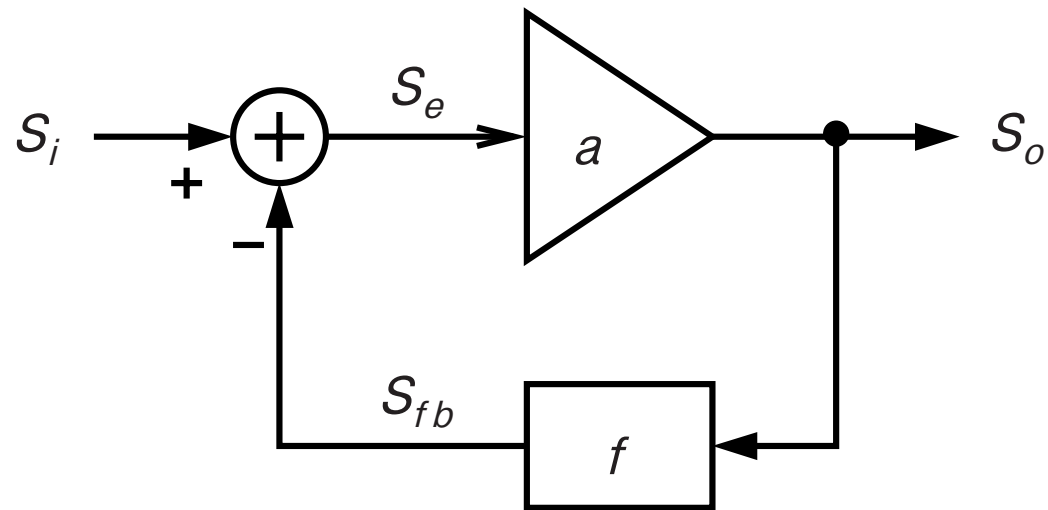
December 5, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Feedback

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$$S_o = a \cdot S_e \quad S_{fb} = f \cdot S_o \quad S_e = S_i - S_{fb}$$

$$\text{Closed-Loop Gain} = A \equiv \frac{S_o}{S_i} = \frac{a}{1 + af} = \frac{a}{1 + T} \approx \frac{1}{f} \text{ if } T \gg 1$$

$$\text{Gain Sensitivity} = \frac{\delta A}{A} = \frac{1}{1 + T} \cdot \frac{\delta a}{a}$$

$$\text{Loop Gain} = T \equiv a \times f$$

# Effect of Negative Feedback on Distortion

---

If  $a$  is a nonlinear amplifier

$$S_o = a_1 S_e + a_2 S_e^2 + a_3 S_e^3 + \dots \quad T = a_1 f$$

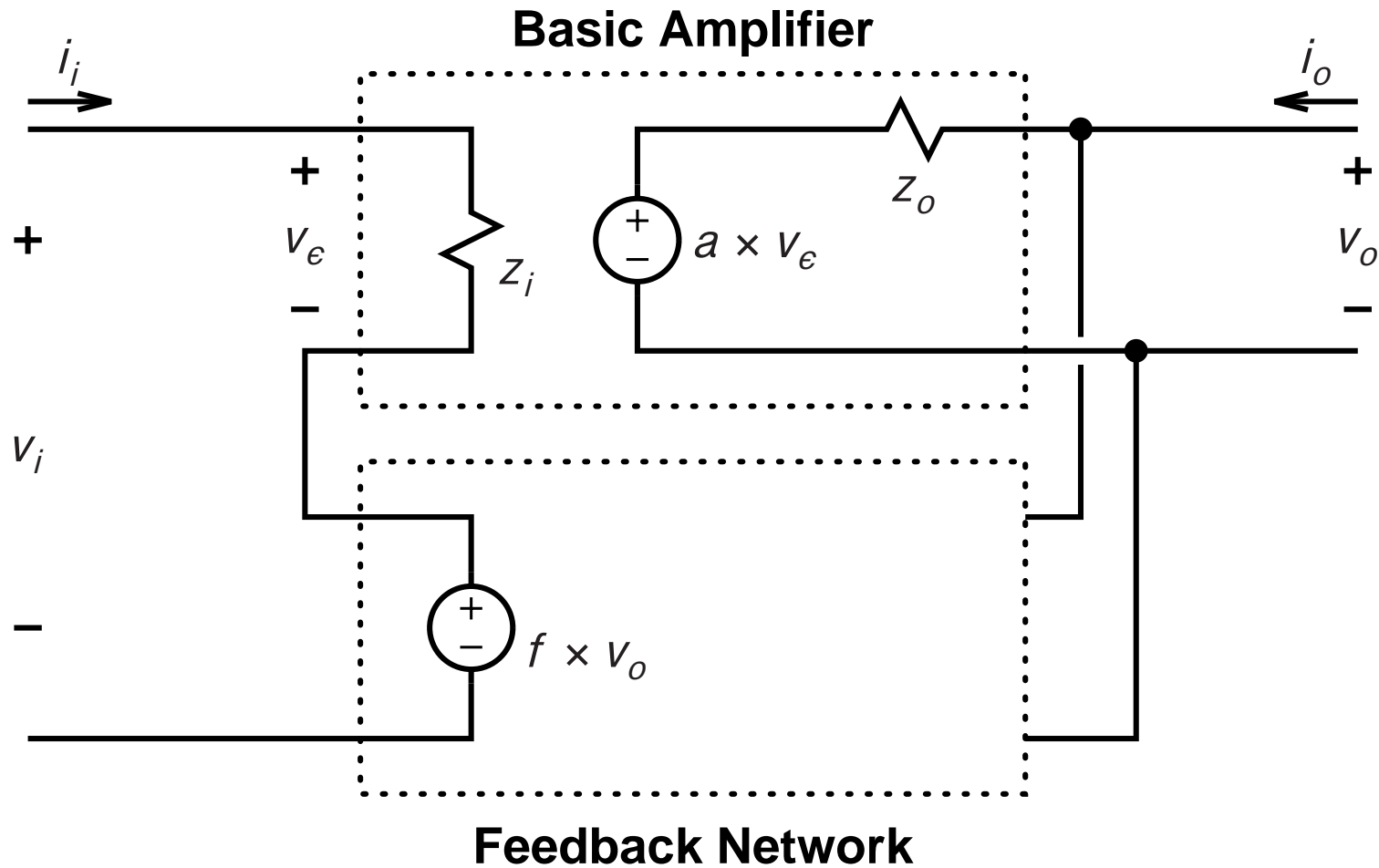
- For constant input level, the harmonic distortions are

$$\text{HD}_2 = \frac{1}{(1 + T)^2} \cdot \text{HD}_2|_{T=0} \quad \text{HD}_3 = \frac{1 - \frac{2a_2^2 f}{a_3(1+T)}}{(1 + T)^3} \cdot \text{HD}_3|_{T=0}$$

- For constant output level, the harmonic distortions are

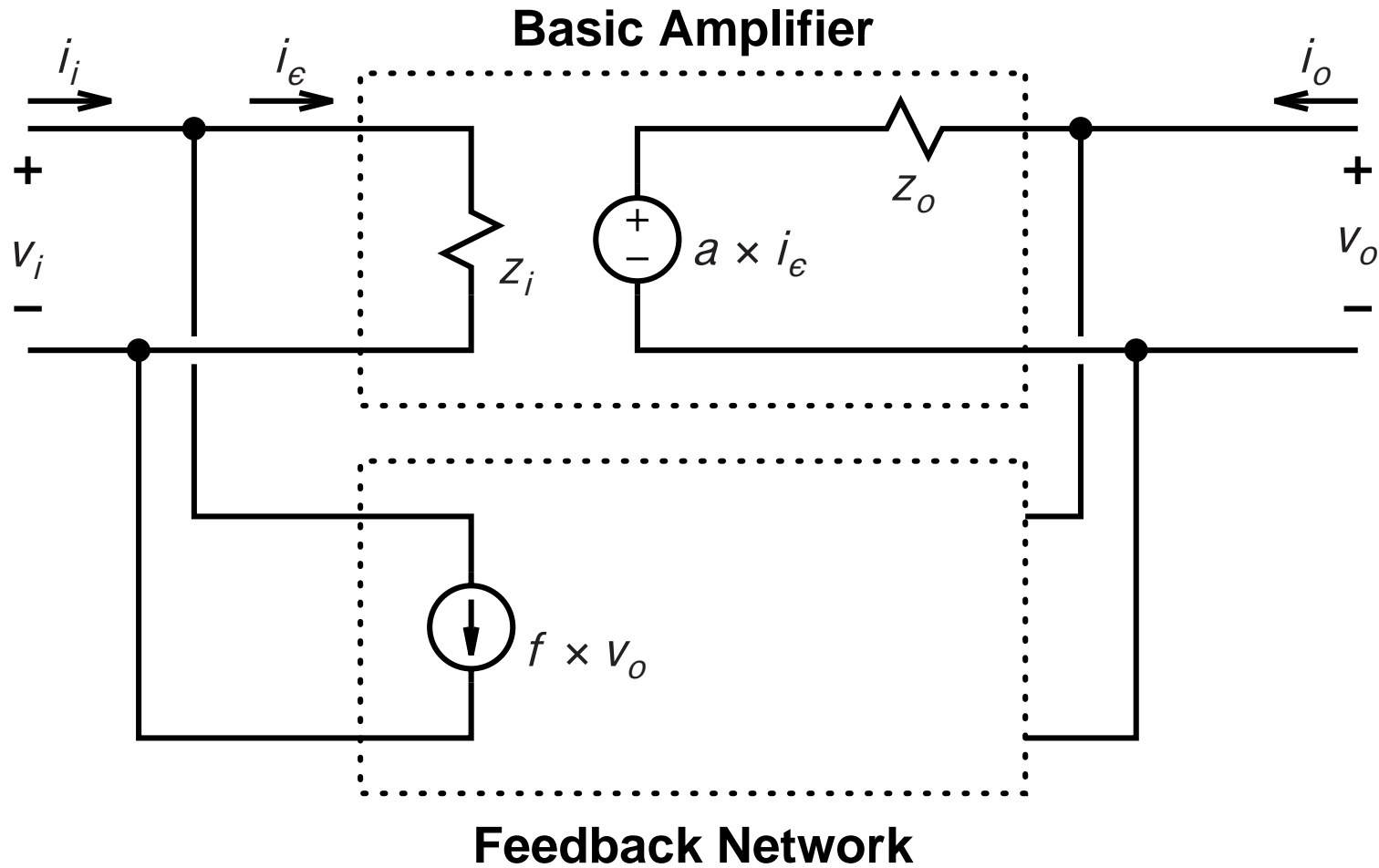
$$\text{HD}_2 = \frac{1}{(1 + T)} \cdot \text{HD}_2|_{T=0} \quad \text{HD}_3 = \frac{1 - \frac{2a_2^2 f}{a_3(1+T)}}{(1 + T)} \cdot \text{HD}_3|_{T=0}$$

# Series-Shunt Feedback Configuration



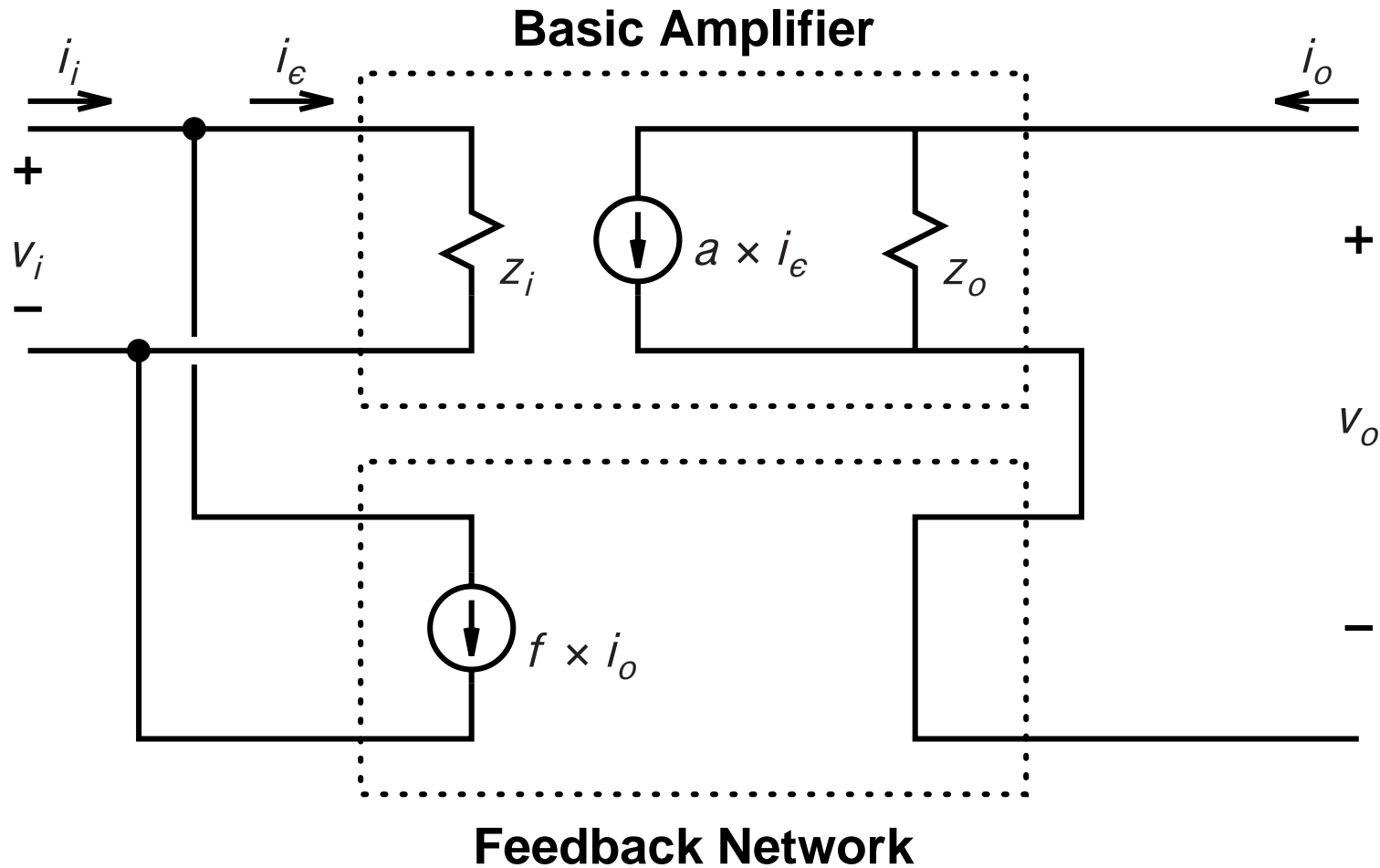
$$T = a \times f \quad \frac{v_o}{v_i} = \frac{a}{1 + T} \quad Z_i = z_i \times (1 + T) \quad Z_o = \frac{z_o}{1 + T}$$

# Shunt-Shunt Feedback Configuration



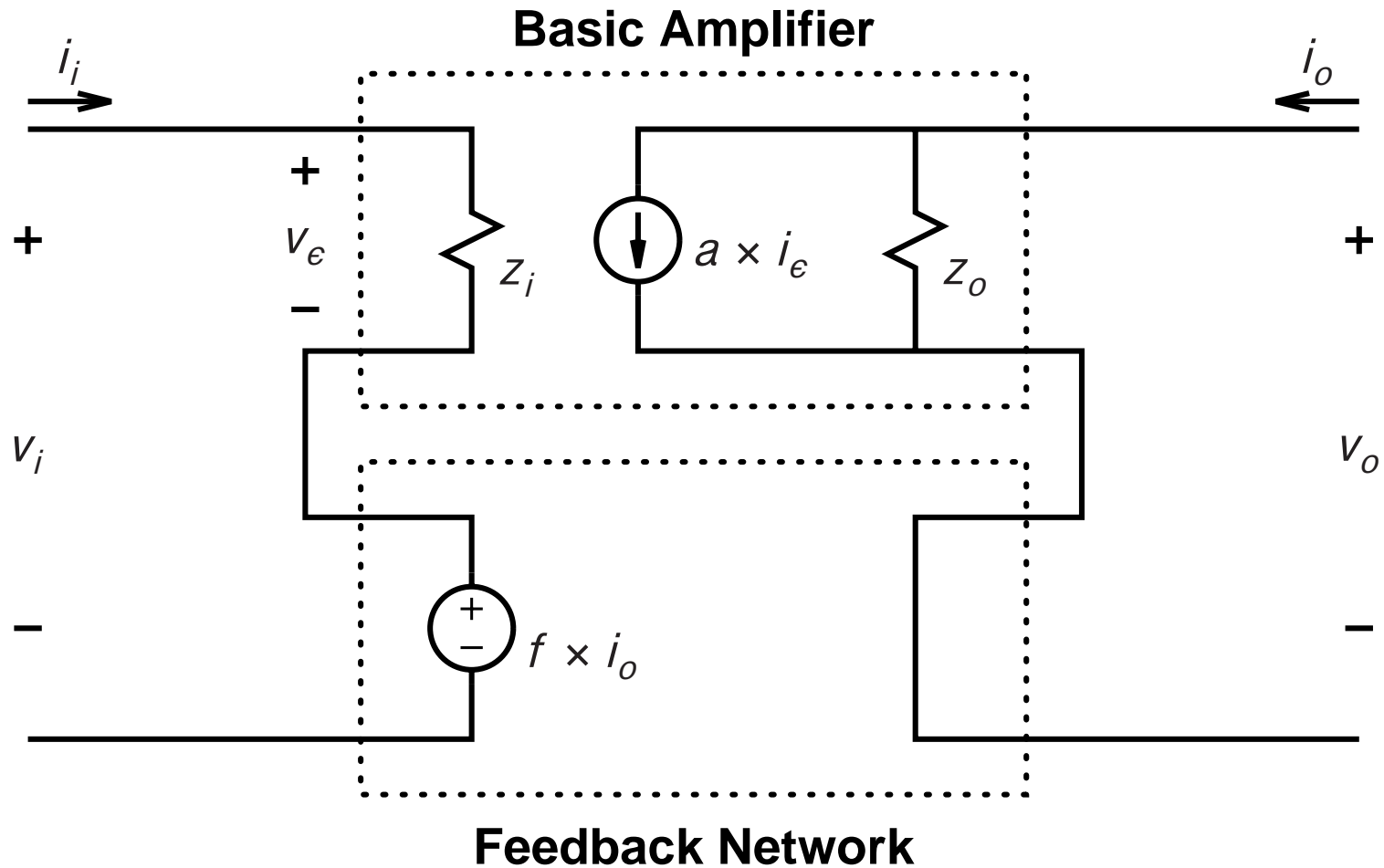
$$T = a \times f \quad \frac{V_o}{i_j} = \frac{a}{1 + T} \quad Z_i = \frac{Z_i}{1 + T} \quad Z_o = \frac{Z_o}{1 + T}$$

# Shunt-Series Feedback Configuration



$$T = a \times f \quad \frac{i_o}{i_j} = \frac{a}{1 + T} \quad Z_i = \frac{z_i}{1 + T} \quad Z_o = z_o \times (1 + T)$$

# Series-Series Feedback Configuration



$$T = a \times f \quad \frac{i_o}{V_i} = \frac{a}{1 + T} \quad Z_i = z_i \times (1 + T) \quad Z_o = z_o \times (1 + T)$$

# Two-Port Analysis of Feedback Amplifier

Topology	Series-Shunt	Series-Series	Shunt-Series	Shunt-Shunt
$S_{fb}$	V	V	I	I
$S_o$	V	I	I	V
For $L_i$ set	$v_o = 0$	$i_o = 0$	$i_o = 0$	$v_o = 0$
For $L_o$ set	$i_i = 0$	$i_i = 0$	$v_i = 0$	$v_i = 0$
Source	Thevenin	Thevenin	Norton	Norton

$S_{fb}$  = Feedback signal;  $S_o$  = Sampled Signal  
 $L_i$  = Input loop loading;  $L_o$  = Output loop loading

Fundamental Assumptions:

1. The input signal is transmitted to the output through the amplifier  $a$  and not through the  $f$  feedback network.
2. The feedback signal is transmitted from the output to the input through the  $f$  block, and not through the amplifier.
3. The feedback factor  $f$  is independent of the load and the source impedances.

# Two-Port Analysis of Feedback Amplifier

---

1. Identify the topology.
2. Draw the basic amplifier circuit without feedback using the *loading approximation* method.
3. Use a Thevenin's source if  $S_{fb}$  is a voltage and a Norton's source if  $S_{fb}$  is a current.
4. Indicate  $S_{fb}$  and  $S_o$  on the "open-loop" circuit. Evaluate  $f = S_{fb}/S_o$ .
5. Evaluate forward gain  $a = S_o/S_i$  from the open-loop circuit.
6. Calculate closed-loop characteristics.

# Loading Approximation Method

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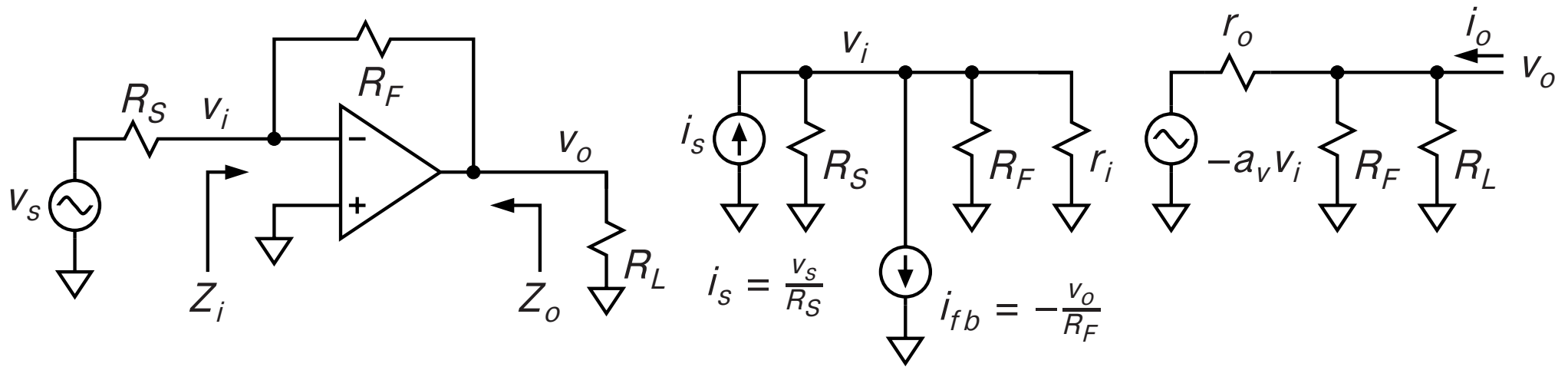
To find the input network:

1. Set  $v_o = 0$  for shunt sampling; i.e., short the output node.
2. Set  $i_o = 0$  for series sampling; i.e., open the output loop.

To find the output network:

1. Set  $v_i = 0$  for shunt comparison; i.e., short the input node.
2. Set  $i_i = 0$  for series comparison; i.e., open the input loop.

# Two-Port Analysis of a Shunt-Shunt Feedback Amplifier



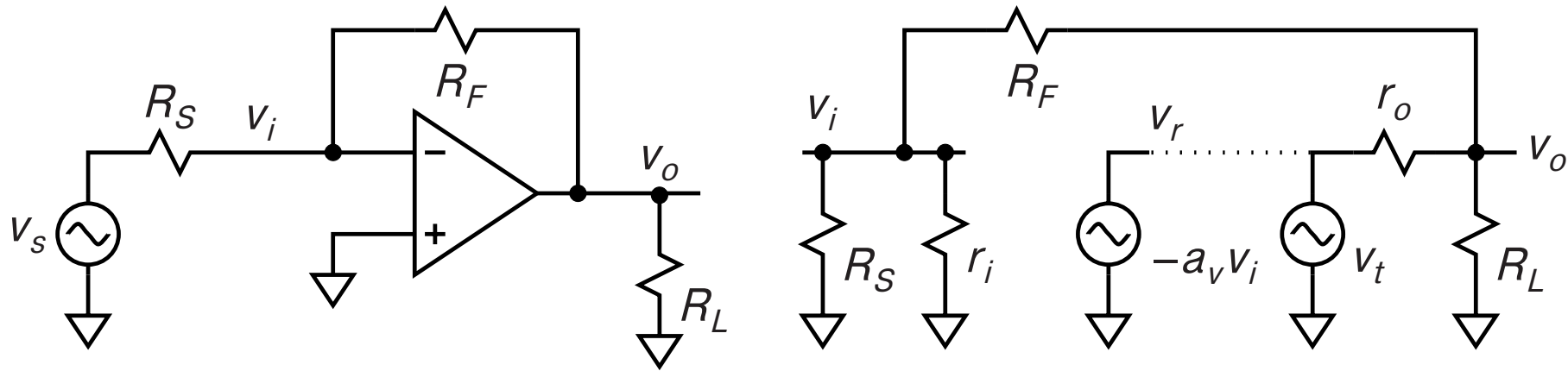
$$a = \left. \frac{v_o}{i_s} \right|_{i_{fb}=0} = (R_S \parallel R_F \parallel r_i)(-a_v) \frac{R_F \parallel R_L}{r_o + (R_F \parallel R_L)} \quad f = \frac{i_{fb}}{v_o} = -\frac{1}{R_F}$$

$$T = a \times f \approx a_v \times \frac{R_S}{R_S + R_F}$$

$$\left. \frac{v_o}{i_s} \right|_{\text{closed loop}} = \frac{a}{1 + af} \approx \frac{1}{f} \approx -R_F \quad \Rightarrow \quad \frac{v_o}{v_s} \approx -\frac{R_F}{R_S}$$

$$\frac{v_i}{i_s} = Z_i \parallel R_S = \frac{R_S \parallel R_F \parallel r_i}{1 + T} \approx \frac{R_F}{a_v} \quad \frac{v_o}{i_o} = Z_o \parallel R_L = \frac{R_F \parallel R_L \parallel r_o}{1 + T} \approx \frac{r_o}{1 + T}$$

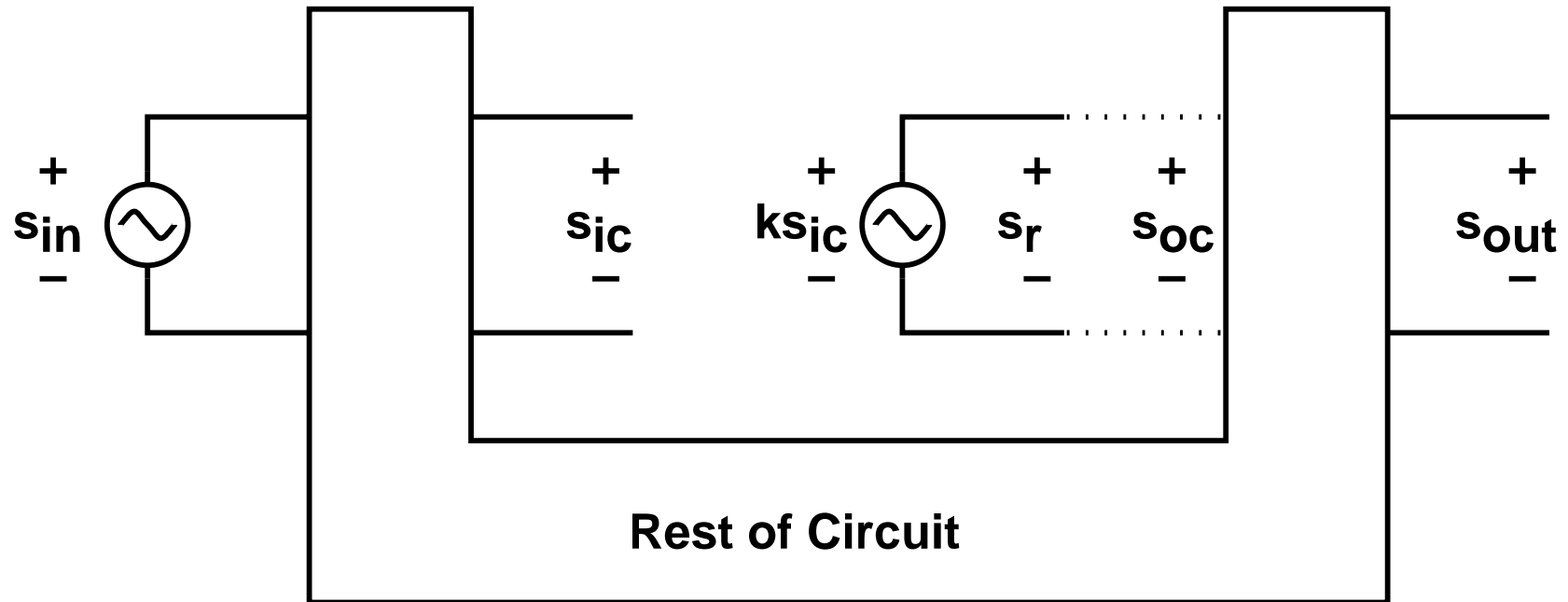
# Return Ratio



$$\begin{aligned} \text{Return Ratio} = \mathcal{R} &\equiv -\frac{v_r}{v_t} = \frac{v_o}{v_t} \cdot \frac{v_i}{v_o} \cdot -\frac{v_r}{v_i} \\ &= \frac{R_L \parallel [R_F + (R_S \parallel r_i)]}{r_o + R_L \parallel [R_F + (R_S \parallel r_i)]} \cdot \frac{R_S \parallel r_i}{R_F + (R_S \parallel r_i)} \cdot a_v \end{aligned}$$

- The loop gain  $T = a \cdot f$  in the two-port analysis is an approximation of  $\mathcal{R}$ .

# Closed-Loop Gain Using Return Ratio



$$\begin{bmatrix} s_{ic} \\ s_{out} \end{bmatrix} = \begin{bmatrix} B_1 & -H \\ d & B_2 \end{bmatrix} \begin{bmatrix} s_{in} \\ s_{oc} \end{bmatrix} \quad s_{oc} = k s_{ic} \quad \mathcal{R} \equiv -\frac{s_r}{s_{oc}} = kH$$

$$B_1 = \left. \frac{s_{ic}}{s_{in}} \right|_{s_{oc}=0} \quad B_2 = \left. \frac{s_{out}}{s_{oc}} \right|_{s_{in}=0} \quad H = -\left. \frac{s_{ic}}{s_{oc}} \right|_{s_{in}=0} \quad d = \left. \frac{s_{out}}{s_{in}} \right|_{s_{oc}=0}$$

# Closed-Loop Gain Using Return Ratio

---

We have

$$A = \frac{s_{out}}{s_{in}} = \frac{B_1 k B_2}{1 + kH} + d = \frac{g}{1 + \mathcal{R}} + d \quad g = B_1 k B_2$$

$$A = \frac{g + d(1 + \mathcal{R})}{1 + \mathcal{R}} = \frac{\left(\frac{g}{\mathcal{R}} + d\right) \mathcal{R}}{1 + \mathcal{R}} + \frac{d}{1 + \mathcal{R}} = A_\infty \cdot \frac{\mathcal{R}}{1 + \mathcal{R}} + d \cdot \frac{1}{1 + \mathcal{R}} \quad A_\infty = \frac{g}{\mathcal{R}} + d$$

- $d$  is the transfer function from the input to the output with  $k = 0$ .
- The value of  $A_\infty$  can be found readily by letting  $k \rightarrow \infty$  and  $s_{ic}$  is virtually “0”.
- Typically,  $A_\infty$  is determined by a passive feedback network and is equal to  $1/f$  from two-port analysis.

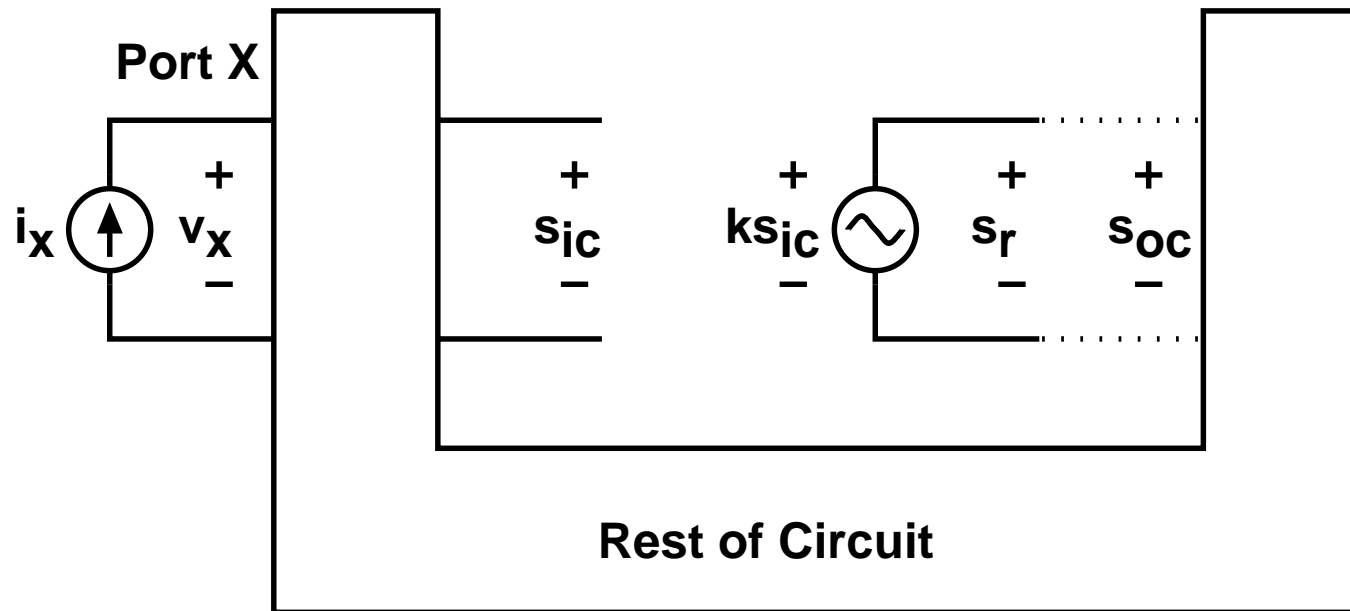
## Closed-Loop Gain Using Return Ratio

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The  $A_\infty \mathcal{R}$  term can be rewritten as

$$\begin{aligned} A_\infty \cdot \mathcal{R} &= \left( \frac{g}{\mathcal{R}} + d \right) \cdot \mathcal{R} = B_1 k B_2 + d \mathcal{R} = \left( B_1 + \frac{dH}{B_2} \right) \cdot k \cdot B_2 \\ &= \left. \frac{s_{ic}}{s_{in}} \right|_{s_{out}=0} \times k \times \left. \frac{s_{out}}{s_{oc}} \right|_{s_{in}=0} \end{aligned}$$

# Blackman's Impedance Formula

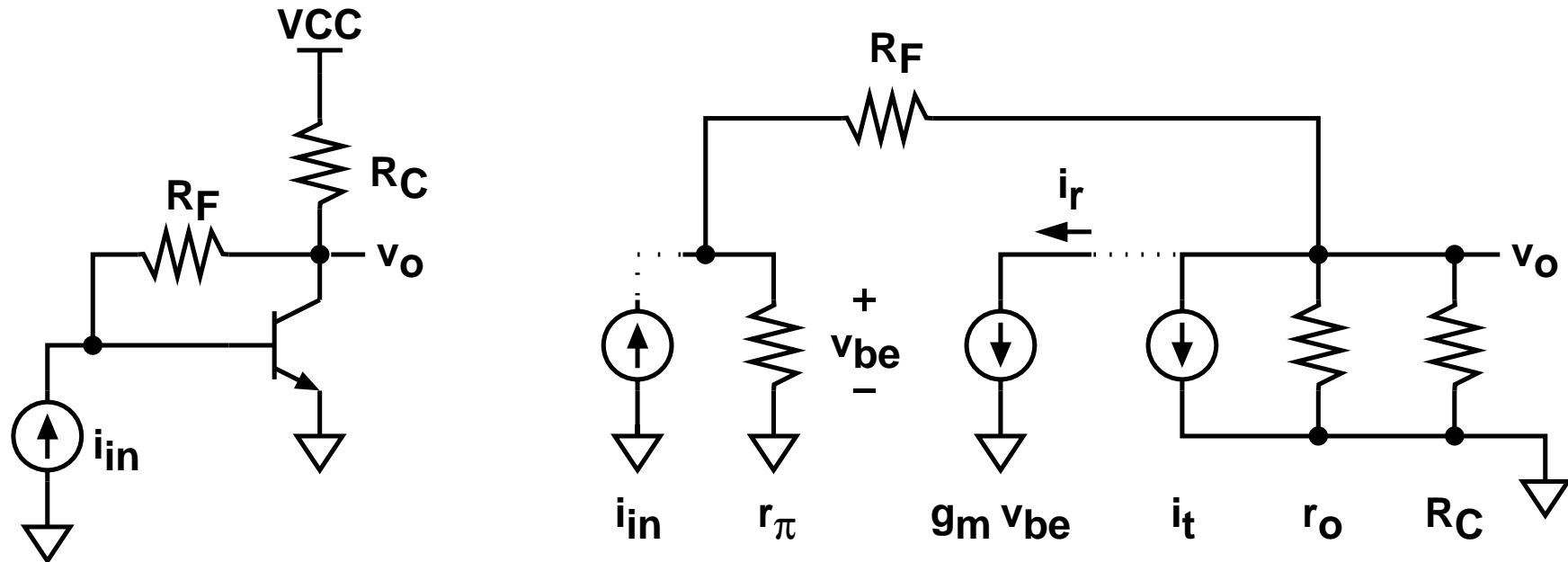


$$\begin{bmatrix} v_x \\ S_{ic} \end{bmatrix} = \begin{bmatrix} a_1 & a_2 \\ a_3 & a_4 \end{bmatrix} \begin{bmatrix} i_x \\ S_{oc} \end{bmatrix} \quad S_{oc} = kS_{ic} \quad \Rightarrow \quad Z_X(k=0) = \left. \frac{v_x}{i_x} \right|_{k=0} = a_1$$

$$\mathcal{R}(\text{port X open}) = -ka_4 \quad \mathcal{R}(\text{port X shorted}) = -k \left( a_4 - \frac{a_2 a_3}{a_1} \right)$$

$$Z_X = \frac{v_x}{i_x} = a_1 \cdot \frac{1 - k \left( a_4 - \frac{a_2 a_3}{a_1} \right)}{1 - ka_4} = Z_X(k=0) \cdot \frac{1 + \mathcal{R}(\text{port X shorted})}{1 + \mathcal{R}(\text{port X open})}$$

# A Transresistance Feedback Amplifier



$$\mathcal{R} = -\frac{i_r}{i_t} = \frac{r_o \parallel R_C}{r_o \parallel R_C + R_F + r_\pi} \cdot r_\pi \cdot g_m$$

$$A_\infty = \left. \frac{v_o}{i_{in}} \right|_{g_m=\infty} = -R_F \quad d = \left. \frac{v_o}{i_{in}} \right|_{g_m=0} = \frac{r_\pi}{r_\pi + R_F + r_o \parallel R_C} \cdot (r_o \parallel R_C)$$

$$\left. \frac{S_{ic}}{S_{in}} \right|_{s_{out}=0} = \left. \frac{v_{be}}{i_{in}} \right|_{v_o=0} = r_\pi \parallel R_F \quad \left. \frac{S_{out}}{S_{oc}} \right|_{s_{in}=0} = \left. \frac{v_o}{i_{oc}} \right|_{i_{in}=0} = -[r_o \parallel R_C \parallel (R_F + r_\pi)]$$

# A Transresistance Feedback Amplifier

---

The closed-loop gain is

$$A = A_{\infty} \frac{\mathcal{R}}{1 + \mathcal{R}} + \frac{d}{1 + \mathcal{R}} = \left. \frac{s_{ic}}{s_{in}} \right|_{s_{out}=0} \cdot k \cdot \left. \frac{s_{out}}{s_{oc}} \right|_{s_{in}=0} \cdot \frac{1}{1 + \mathcal{R}} + \frac{d}{1 + \mathcal{R}}$$

The output resistance is

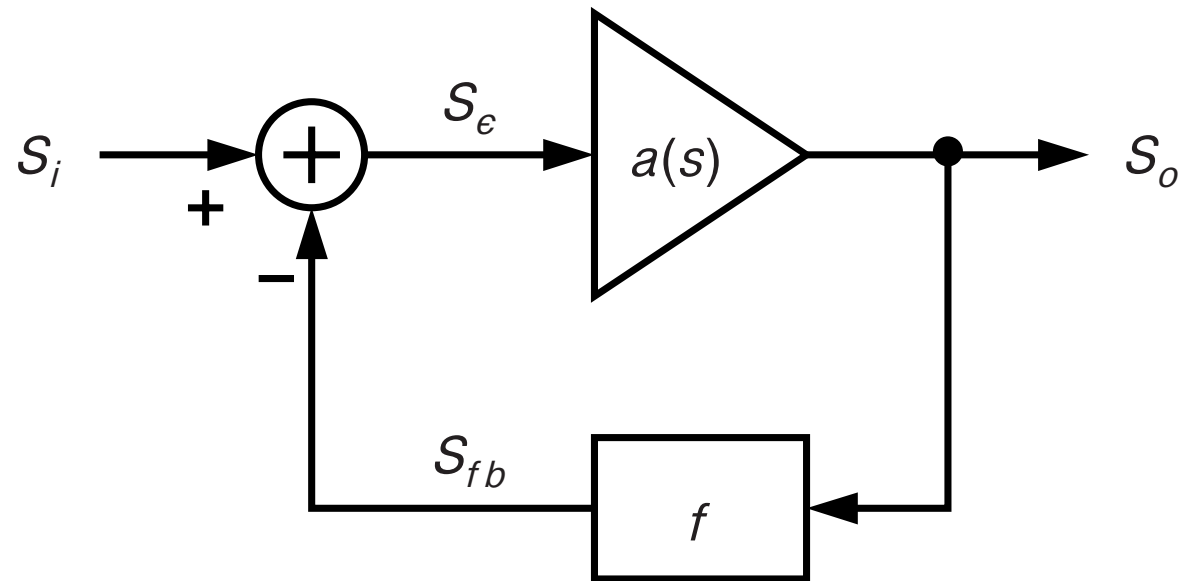
$$R_o = R_X(k = 0) \cdot \frac{1 + \mathcal{R}(\text{port X shorted})}{1 + \mathcal{R}(\text{port X open})} = R_o(g_m = 0) \cdot \frac{1 + \mathcal{R}(\text{output shorted})}{1 + \mathcal{R}(\text{output open})}$$

$$R_o(g_m = 0) = r_o \parallel R_C \parallel (R_F + r_{\pi})$$

$$\mathcal{R}(\text{output shorted}) = 0 \quad \mathcal{R}(\text{output open}) = \mathcal{R}$$

# Frequency Response of Feedback Amplifiers

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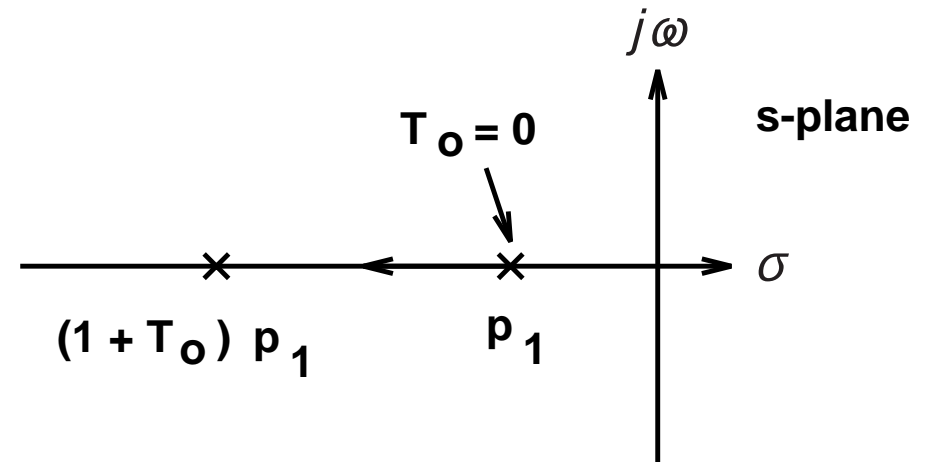
$$A(s) = \frac{S_o}{S_i} = \frac{a(s)}{1 + a(s) \times f}$$

# Single-Pole Model

$$a(s) = \frac{a_o}{1 - s/p_1} \quad T_o = a_o \cdot f$$

$$A(s) = \frac{a_o}{1 + a_o f} \times \frac{1}{1 - \frac{s}{(1+a_o f)p_1}}$$

$$= \frac{a_o}{1 + T_o} \times \frac{1}{1 - \frac{s}{(1+T_o)p_1}}$$

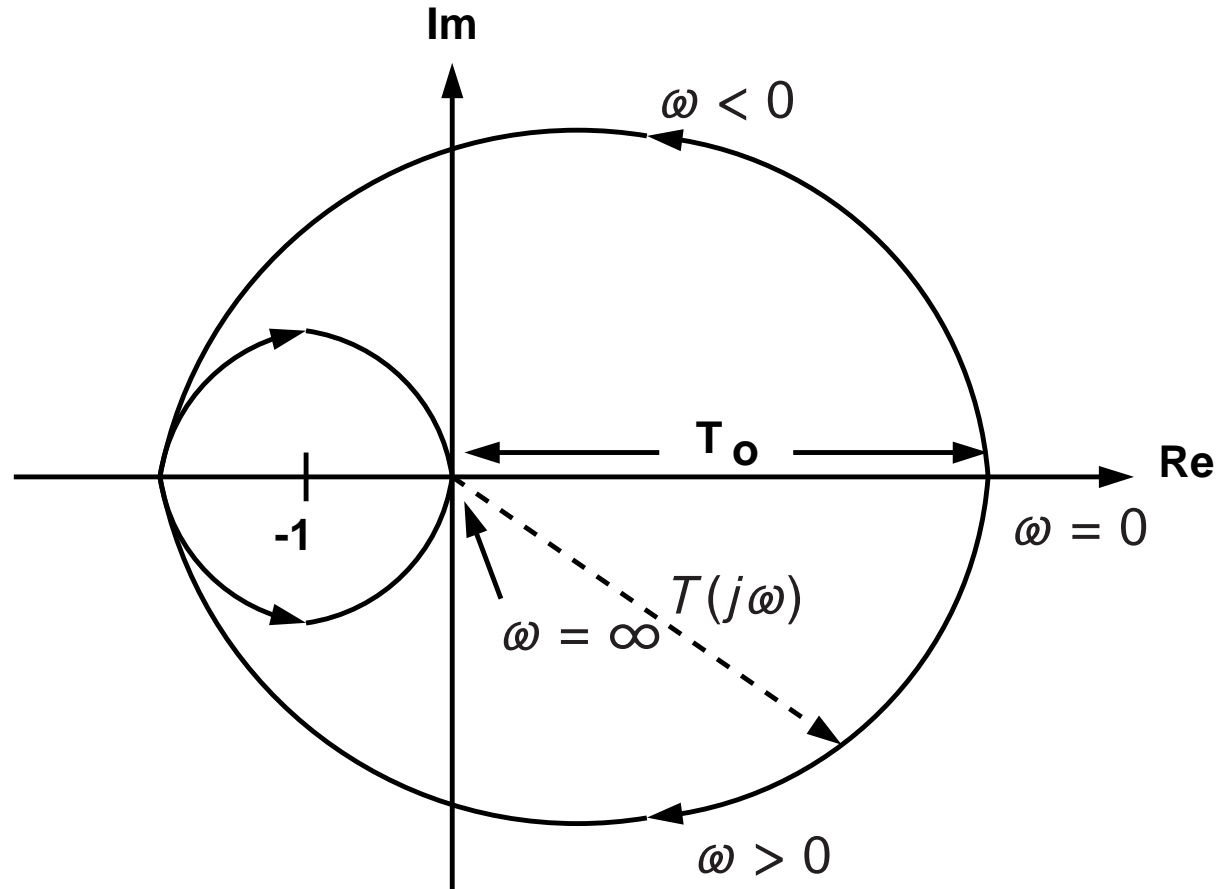


For  $\omega \gg |p_1|$ ,

$$a(s) \approx \frac{a_o}{-s/p_1} \approx \frac{\omega_u}{s} \quad A(s) \approx \frac{\omega_u}{f \cdot \omega_u + s} = \frac{1}{f} \times \frac{1}{1 + s/(f\omega_u)}$$

$$\omega_u \equiv a_o \times |p_1| = \text{Unity-Gain Frequency}$$

# Nyquist Diagram

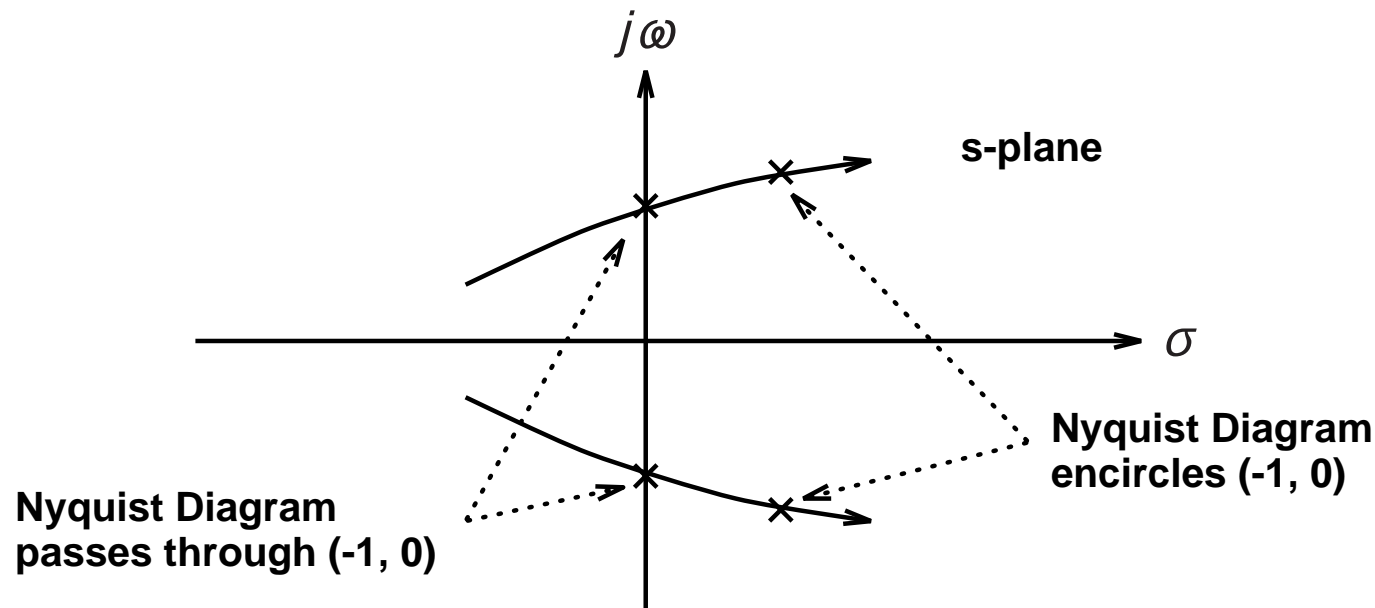


*Nyquist diagram* is the polar plot of a feedback amplifier's loop gain  $T(j\omega) = af$  for  $-\infty < \omega < \infty$ .

# Nyquist Criterion

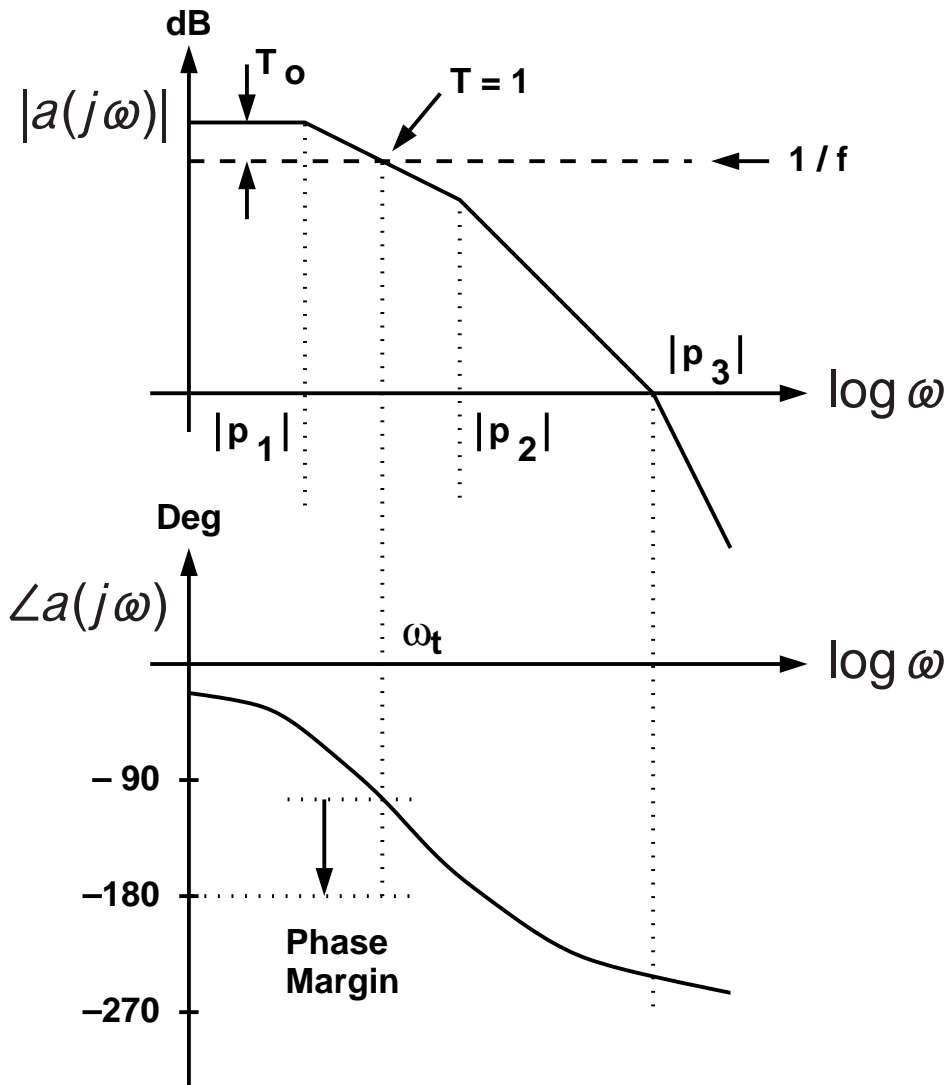
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- If the Nyquist plot encircles the point  $(-1, 0)$ , the amplifier is unstable.
- The number of encirclements of the point  $(-1, 0)$  gives the number of right-half-plane poles.



- If  $|T(j\omega)| > 1$  at the frequency where  $\angle T(j\omega) = -180^\circ$ , then the amplifier is unstable.

# Phase Margin



The phase margin is defined as

$$PM = 180^\circ + \angle T(j\omega_t)$$

$\omega_t$  is the frequency where  $|T(j\omega_t)| = 1$

- A typical lower allowable limit for the phase margin is  $45^\circ$ , with a value of  $60^\circ$  being more common.

# Pseudo Dominant-Pole Model

---

$$a(s) = \frac{a_o}{(1 + s/\omega_1)(1 + s/\omega_2)}$$

- $\omega_1 = -p_1$  is the dominant pole frequency.
- If other poles and zero are on the real axis at much higher frequencies, then

$$\frac{1}{\omega_2} \approx \sum_{i=2}^m \frac{1}{-p_i} - \sum_{i=1}^m \frac{1}{-z_i}$$

- In practice,  $\omega_2$  can be found from simulation.  $\omega_2$  is the frequency at which

$$\angle a(j\omega_2) = -135^\circ$$

# Phase Margin of the Pseudo Dominant-Pole Model

---

At frequencies  $\omega \gg \omega_1$

$$a(s) \approx \frac{a_o}{(s/\omega_1)(1 + s/\omega_2)} = \frac{\omega_u}{s(1 + s/\omega_2)} \quad \omega_u = a_o \times \omega_1$$

The loop gain becomes

$$T(s) = a(s) \cdot f = \frac{f \cdot \omega_u}{s(1 + s/\omega_2)}$$

Since  $\angle T(j\omega) = -90^\circ - \tan^{-1}(\omega/\omega_2)$

$$\text{PM} = 180^\circ + \angle T(j\omega_t) = 90^\circ - \tan^{-1}\left(\frac{\omega_t}{\omega_2}\right) \quad \frac{\omega_t}{\omega_2} = \tan(90^\circ - \text{PM})$$

- $\omega_t$  is the unity-gain frequency of  $T$ , i.e.,

$$|T(j\omega_t)| = 1$$

- $\omega_t$  is independent of the feedback factor  $f$ .

# Closed-Loop Response of the Pseudo Dominant-Pole Model

---

Since

$$a(s) = \frac{a_o}{(1 + s/\omega_1)(1 + s/\omega_2)}$$

The closed-loop gain is

$$A(s) = \frac{a(s)}{1 + a(s) \times f} = \frac{A_o}{1 + \frac{s(1/\omega_1 + 1/\omega_2)}{1 + a_o f} + \frac{s^2}{(1 + a_o f)(\omega_1 \omega_2)}} = \frac{A_o}{1 + \frac{s}{\omega_o Q} + \frac{s^2}{\omega_o^2}}$$

$$A_o = \frac{a_o}{1 + a_o f} \quad \omega_o = \sqrt{(1 + a_o f)(\omega_1 \omega_2)} \quad Q = \frac{\sqrt{(1 + a_o f)/(\omega_1 \omega_2)}}{1/\omega_1 + 1/\omega_2}$$

- If  $Q = 1/\sqrt{2} = 0.707$ ,  $|A(j\omega)|$  has the widest passband without peaking. Its  $-3$  dB frequency is  $\omega_o$ .
- If  $Q > 0.5$ , the percentage overshoot of the step response is

$$\% \text{ overshoot} = 100e^{-\pi/\sqrt{4Q^2-1}}$$

## Quality Factor ( $Q$ ) and Phase Margin

---

If  $a_o f \gg 1$  and  $\omega_2 \gg \omega_1$ , then

$$A_o \approx \frac{1}{f} \quad \omega_o \approx \sqrt{f \omega_u \omega_2} \quad Q \approx \sqrt{\frac{f a_o \omega_1}{\omega_2}} \approx \sqrt{f \frac{\omega_u}{\omega_2}}$$

Since  $|T(j\omega_t)| = 1$ , we have

$$|T(j\omega_t)| = \left| \frac{f \omega_u}{j\omega_t(1 + j\omega_t/\omega_2)} \right| = 1 \quad \Rightarrow \quad f \frac{\omega_u}{\omega_t} = \sqrt{1 + \left(\frac{\omega_t}{\omega_2}\right)^2}$$

$$Q^2 = f \frac{\omega_u}{\omega_2} = \frac{\omega_t}{\omega_2} \sqrt{1 + \left(\frac{\omega_t}{\omega_2}\right)^2}$$

- For a given phase margin,  $\omega_t/\omega_2$  is known. Then  $Q$  can be found using the above equation.

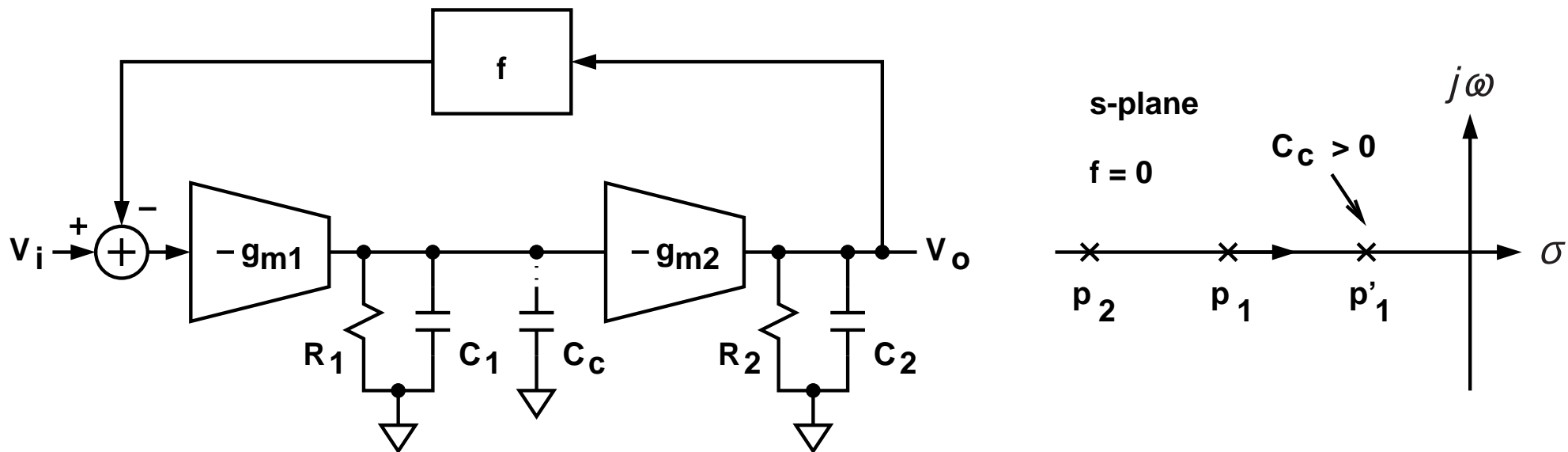
## Quality Factor ( $Q$ ) and Phase Margin

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PM	$\omega_t/\omega_2$	$f(\omega_u/\omega_2)$	$Q$	Overshoot
45°	1.000	1.414	1.189	36.8%
55°	0.700	0.854	0.924	13.3%
60°	0.577	0.666	0.816	8.7%
65°	0.466	0.514	0.717	4.7%
70°	0.364	0.387	0.622	1.4%
75°	0.268	0.277	0.527	0.008%

- Define  $\alpha_t \equiv \omega_t/\omega_2$  and  $\alpha_p \equiv f(\omega_u/\omega_2)$ . Note that  $\alpha_t \approx \alpha_p$  for PM > 65°.
- Design with PM > 65° for no peaking in frequency response.
- Design with PM > 80° for no overshoot in step response.

# Dominant-Pole Compensation



The original poles of  $a(s)$  are

$$p_1 = \frac{-1}{R_1 C_1} \quad p_2 = \frac{-1}{R_2 C_2} \quad \omega_u = |A_v(0)| \cdot |p_1| = g_{m1} R_1 g_{m2} R_2 \cdot |p_1| = \frac{g_{m1}}{C_1} \cdot g_{m2} R_2$$

By adding compensation capacitor  $C_c$

$$p'_1 = \frac{-1}{R_1(C_1 + C_c)} \quad \omega'_u = \frac{g_{m1}}{(C_1 + C_c)} \cdot g_{m2} R_2$$

# Dominant-Pole Compensation

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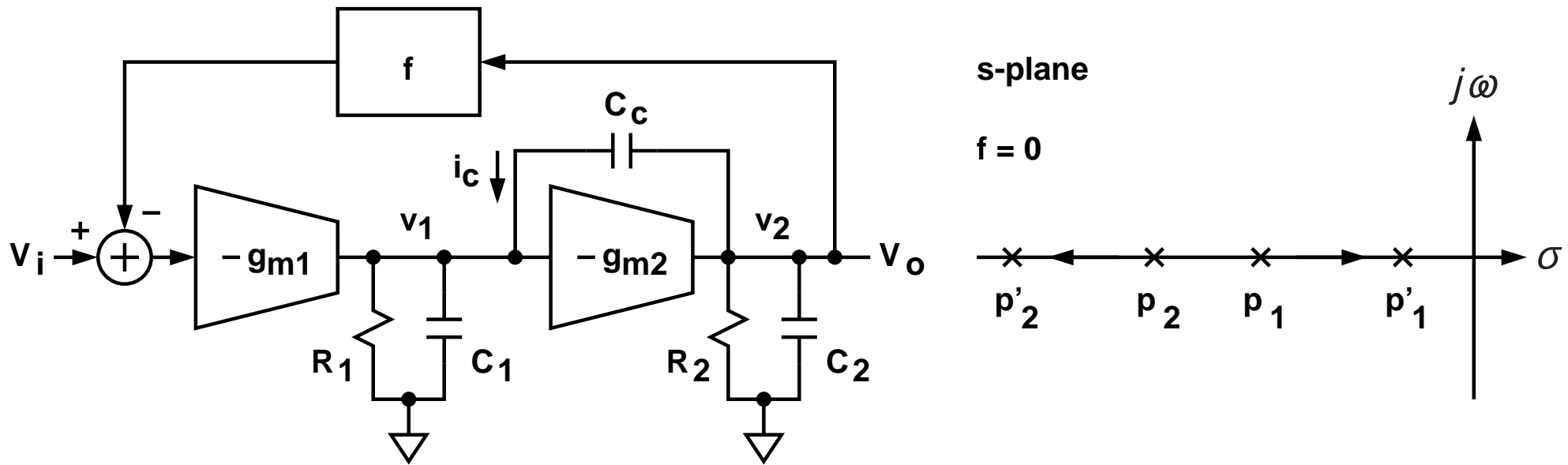
- The  $-3$  dB bandwidth of the closed loop gain is approximately

$$f \cdot \omega'_u = \alpha_p \cdot |\rho'_2| \qquad \omega_{-3\text{dB}} \approx \omega_t = \alpha_t \cdot |\rho'_2|$$

where  $\alpha_t$  and  $\alpha_p$  are determined by the required phase margin.

- $C_c$  usually is quite large (typically  $> 1000$  pF) and cannot be realized on a monolithic chip.
- For a general-purpose opamp where  $0 < f \leq 1$ , if the opamp is compensated for  $f = 1$ , it is guaranteed to be stable for all  $f$ , although it will be slower than necessary.

# Miller (Pole-Splitting) Compensation



Let  $f = 0$ , the nodal equations are

$$\begin{bmatrix} G_1 + s(C_1 + C_c) & -sC_c \\ g_{m2} - sC_c & G_2 + s(C_2 + C_c) \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} -g_{m1}V_i \\ 0 \end{bmatrix}$$

# Miller (Pole-Splitting) Compensation

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The open-loop forward gain  $a(s)$  can be solved as

$$a(s) \equiv \frac{v_2}{v_i} = a_0 \times \frac{1 - s/z'_1}{1 + b_1s + b_2s^2} = a_0 \times \frac{1 - s/z'_1}{D(s)}$$

$$a_0 = g_{m1}g_{m2}R_1R_2$$

$$z'_1 = +\frac{g_{m2}}{C_c}$$

$$b_1 = R_1(C_1 + C_c) + R_2(C_2 + C_c) + g_{m2}R_1R_2C_c \quad b_2 = R_1R_2(C_1C_2 + C_1C_c + C_2C_c)$$

Using dominant-pole approximation, i.e.,  $|p'_1| \ll |p'_2|$ ,

$$p'_1 \approx -\frac{1}{b_1} = -\frac{1}{R_1(C_1 + C_c) + R_2(C_2 + C_c) + g_{m2}R_1R_2C_c}$$

$$p'_2 \approx -\frac{b_1}{b_2} = -\frac{R_1(C_1 + C_c) + R_2(C_2 + C_c) + g_{m2}R_1R_2C_c}{R_1R_2(C_1C_2 + C_1C_c + C_2C_c)}$$

# Miller (Pole-Splitting) Compensation

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Further, if  $g_{m2}R_2 \gg 1$ ,  $R_1 \sim R_2$ , and  $C_1 \sim C_2 \sim C_c$ , then

$$p'_1 \approx -\frac{1}{g_{m2}R_1R_2C_c} = -\frac{g_{m1}}{C_c} \times \frac{1}{a_0}$$

$$p'_2 \approx -\frac{g_{m2}C_c}{C_1C_2 + C_1C_c + C_2C_c} \approx -\frac{g_{m2}}{C_1 + C_2}$$

The dominant-pole unity-gain frequency is

$$\omega'_u = |a_0| \times |p'_1| = \frac{g_{m1}}{C_c}$$

- Note that if  $C_c = 0$

$$p_1 = -\frac{1}{R_1C_1} \quad p_2 = -\frac{1}{R_2C_2}$$

- $C_c$  acts as a *pole splitting* capacitor that separate  $p_1$  and  $p_2$ .

# Miller (Pole-Splitting) Compensation

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For a given phase margin, we have

$$f \cdot \omega'_u = \alpha_p \cdot |p'_2| \qquad \omega_{-3\text{dB}} \approx \omega_t = \alpha_t \cdot |p'_2|$$

Thus

$$\frac{|p'_2|}{\omega'_u} = \frac{f}{\alpha_p} = \frac{g_{m2}}{g_{m1}} \times \frac{C_c}{C_1 + C_2}$$

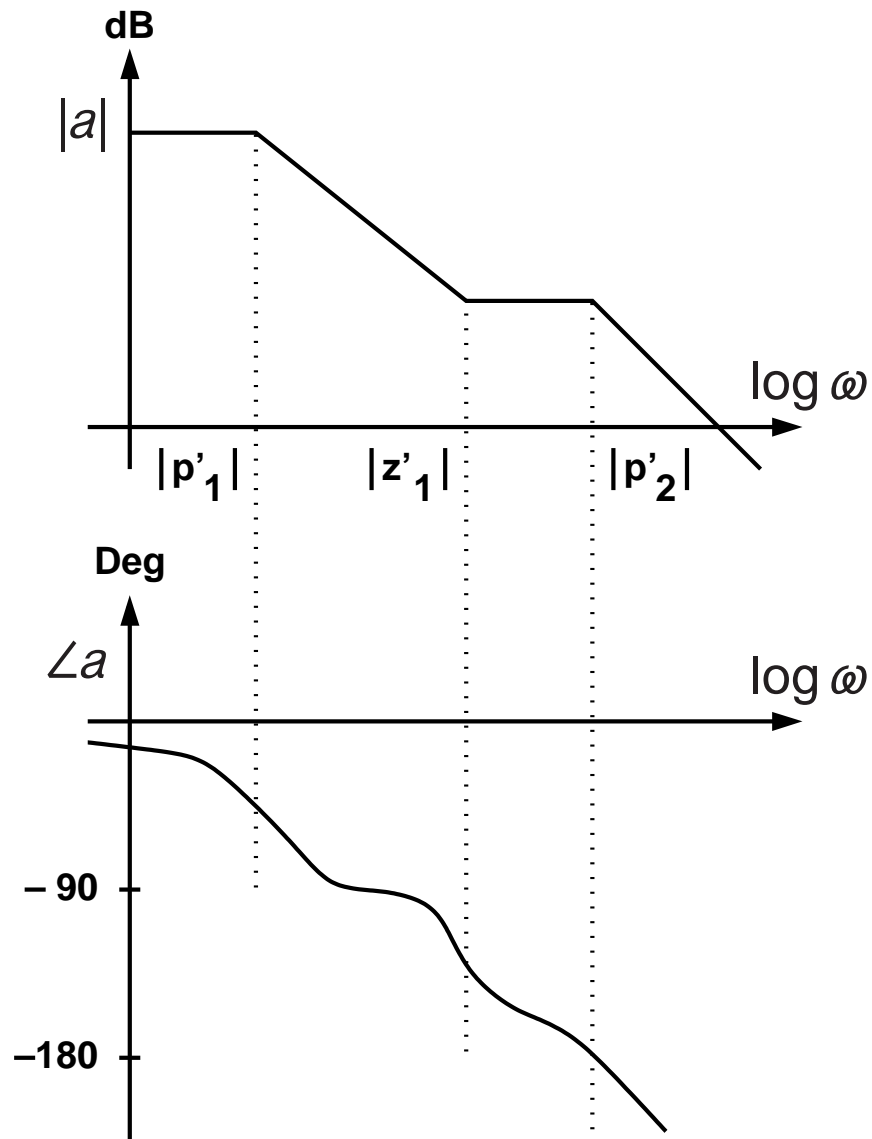
And  $C_c$  can be determined by

$$C_c = \frac{f}{\alpha_p} \times \frac{g_{m1}}{g_{m2}} \times (C_1 + C_2)$$

- For compensation of a general-purpose opamp, let  $f = 1$ , then

$$\omega'_u = \alpha_p \cdot |p'_2| \qquad C_c = \frac{1}{\alpha_p} \times \frac{g_{m1}}{g_{m2}} \times (C_1 + C_2)$$

# Feedforward Zero in Miller Compensation



- Because  $z'_1$  is in the right half-plane (RHP), it will degrade the amplifier phase margin as it approaches  $f \cdot \omega'_u$ .
- $z'_1$  is caused by the feedforward path of  $C_c$ .

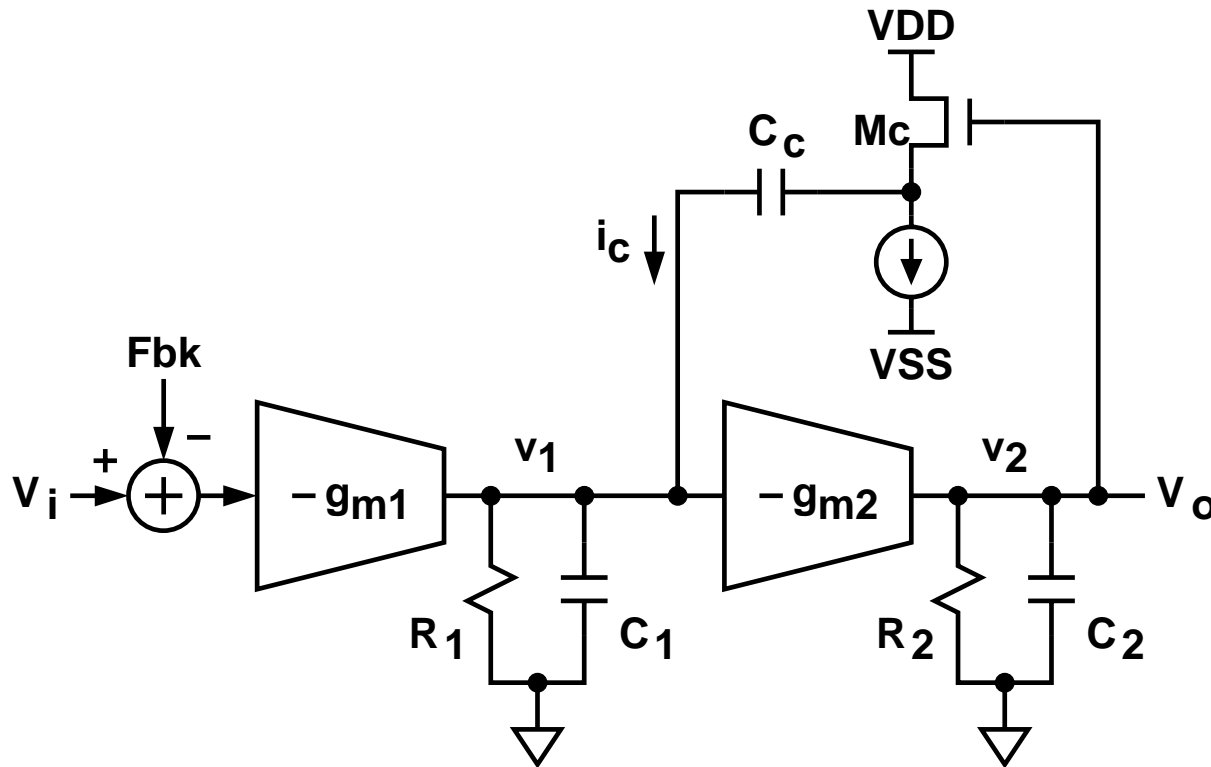
$$i_c = sC_c(v_2 - v_1) = sC_c v_2 - sC_c v_1$$

- To avoid degrading of phase margin by  $z'_1$ , want

$$z'_1 \gg f \cdot \omega'_u \Rightarrow \frac{z'_1}{\omega'_u} \approx \frac{g_{m2}}{g_{m1}} \gg f$$

- Otherwise, additional circuitry must be added to move  $z'_1$ .

# Miller Compensation With Unity-Gain Buffer



Assume the voltage gain of the  $M_c$  source follower is 1. Then

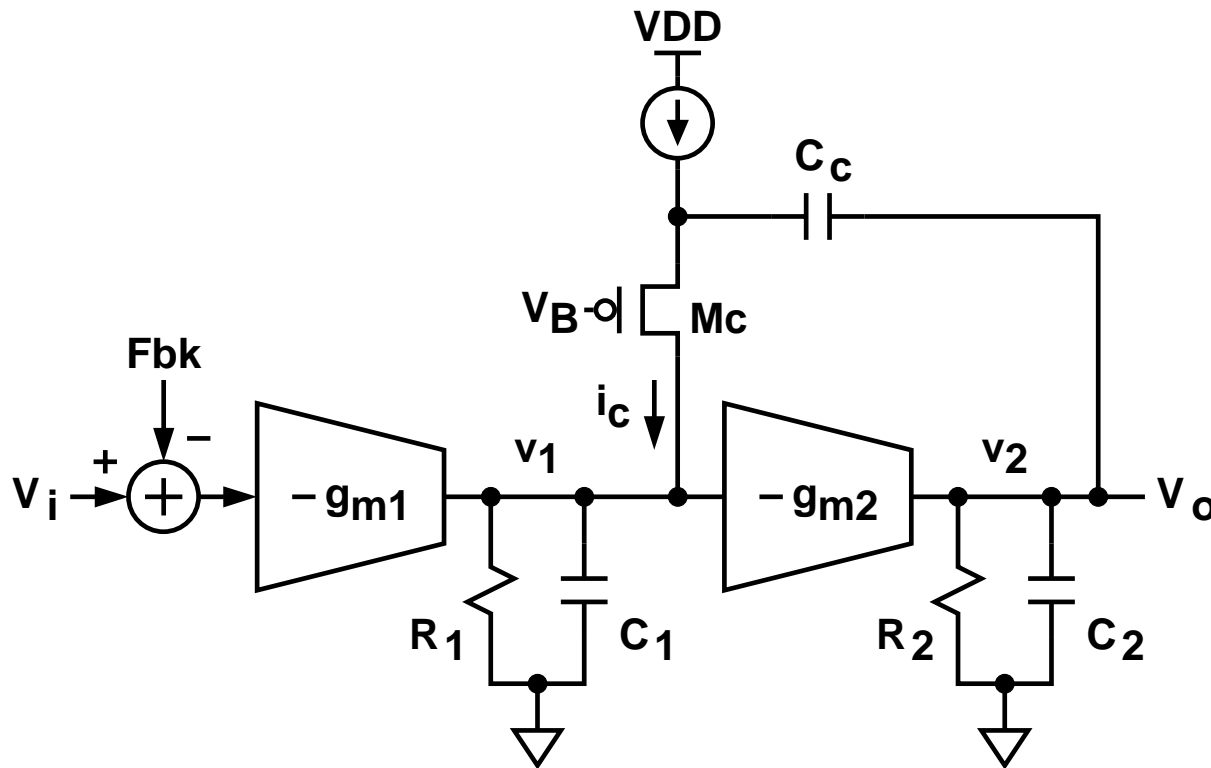
$$i_c = sC_c(v_2 - v_1)$$

$$-g_{m2}v_1 = v_2(G_2 + sC_2)$$

$$a(s) = \frac{g_{m1}g_{m2}R_1R_2}{1 + s[R_1(C_1 + C_c) + R_2C_2 + g_{m2}R_2R_1C_c] + s^2R_1R_2C_2(C_1 + C_c)}$$

$$p_1 \approx -\frac{1}{g_{m2}R_1R_2C_c} \quad p_2 \approx -\frac{g_{m2}}{C_1 + C_2}$$

# Miller Compensation With Common-Gate Stage



Assume the input impedance of the Mc common-gate stage is 0. Then

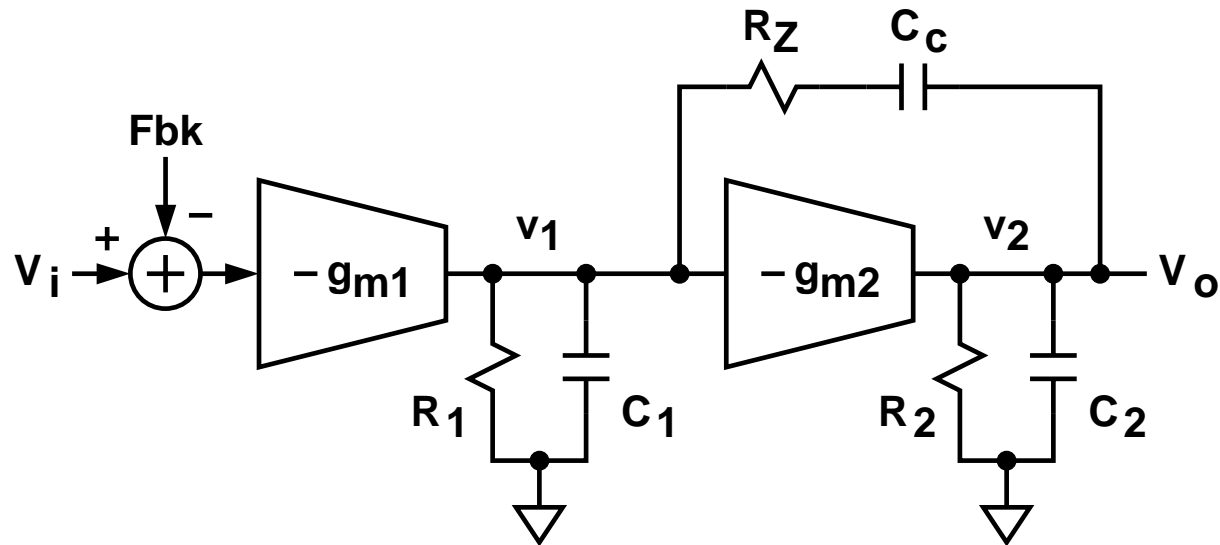
$$i_c = sC_c \cdot v_2$$

$$-g_{m2}v_1 = v_2(G_2 + sC_2 + sC_c)$$

$$a(s) = \frac{g_{m1}g_{m2}R_1R_2}{1 + s[R_1C_1 + R_2(C_2 + C_c) + g_{m2}R_2R_1C_c] + s^2R_1R_2C_1(C_2 + C_c)}$$

$$p_1 \approx -\frac{1}{g_{m2}R_1R_2C_c} \quad p_2 \approx -\frac{g_{m2}}{C_2 + C_c} \cdot \frac{C_c}{C_1}$$

# Miller Compensation With Nulling Resistor



$$a(s) = g_{m1}g_{m2}R_1R_2 \cdot \frac{1 - sC_c (1/g_{m2} - R_Z)}{1 + b_1s + b_2s^2 + b_3s^3}$$

$$b_1 = R_2(C_2 + C_c) + R_1(C_1 + C_c) + R_ZC_c + g_{m2}R_1R_2C_c$$

$$b_2 = R_1R_2(C_1C_2 + C_cC_1 + C_cC_2) + R_ZC_c(R_1C_1 + R_2C_2)$$

$$b_3 = R_1R_2R_ZC_1C_2C_c$$

# Miller Compensation With Nulling Resistor

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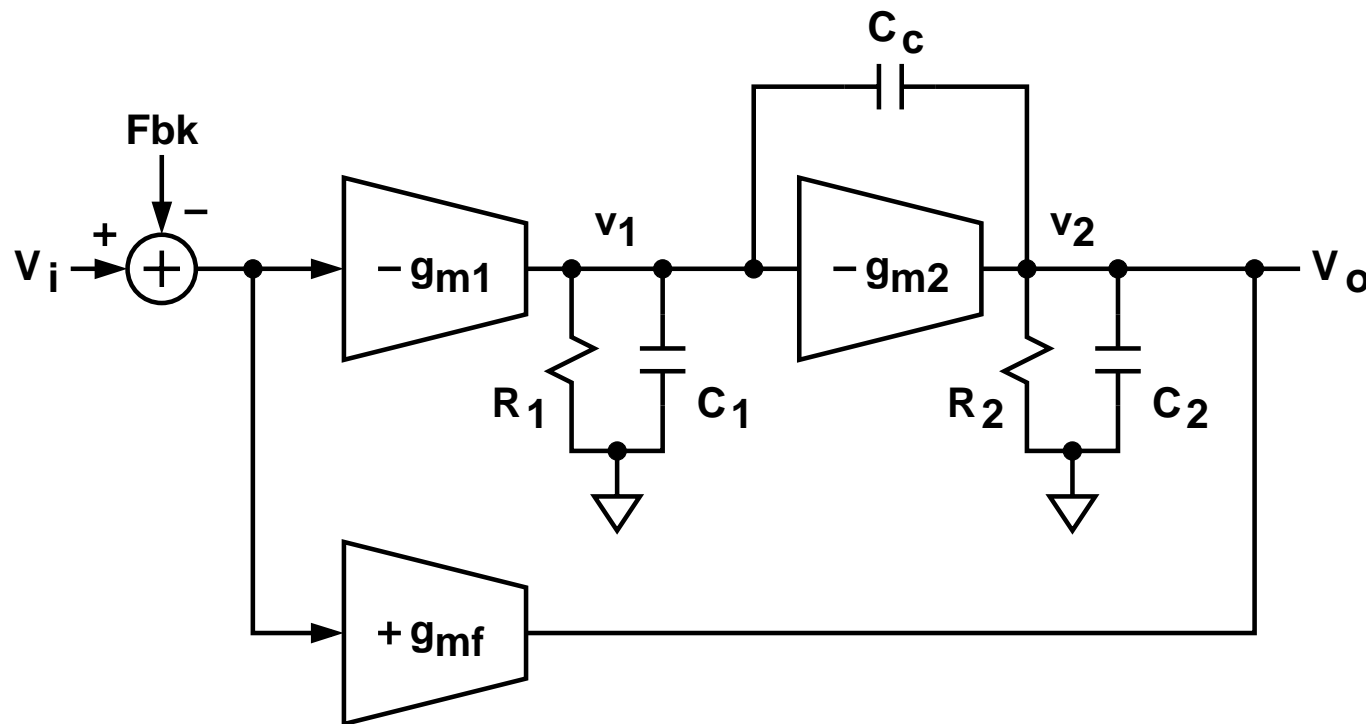
We have

$$z_1 = \frac{1}{(1/g_{m2} - R_Z)C_c}$$
$$p_1 \approx -\frac{1}{g_{m2}R_2R_1C_c} \quad p_2 \approx -\frac{g_{m2}}{C_1 + C_2} \quad p_3 \approx -\frac{1}{R_ZC_1}$$

- In most cases,  $p_3 \gg p_{1,2}$ .
- Usually want  $z_1$  becomes negative and

$$|z_1| \approx \frac{1}{R_ZC_c} = 1.2\omega_u \Rightarrow \frac{1}{R_ZC_c} = 1.2 \cdot \frac{g_{m1}}{C_c} \Rightarrow R_Z = \frac{1}{1.2g_{m1}}$$

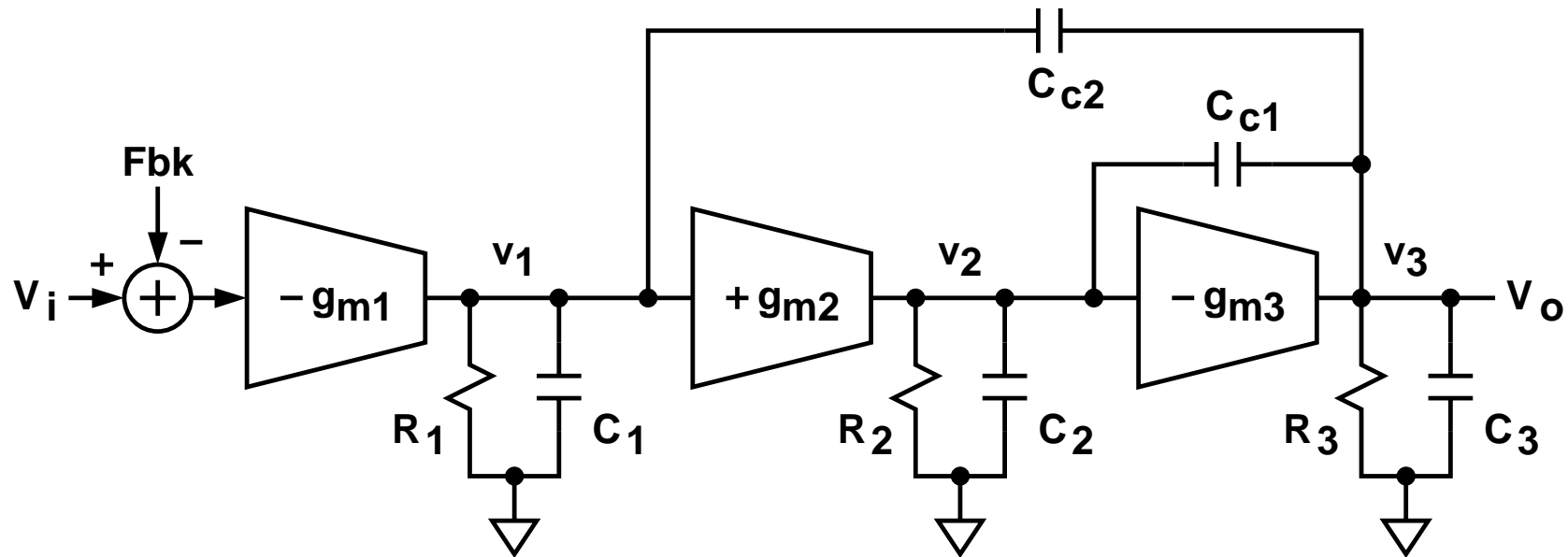
# Miller Compensation with Feedforward Transconductor



$$a(s) = \frac{g_{m1}R_1g_{m2}R_2 + g_{mf}R_2 + sR_1R_2[g_{mf}(C_1 + C_c) - g_{m1}C_c]}{1 + s[R_1(C_1 + C_c) + R_2(C_2 + C_c) + g_{m2}R_1R_2C_c] + s^2[R_1R_2(C_1C_2 + C_1C_c + C_2C_c)]}$$

$$\text{To remove zero, let } g_{mf} = g_{m1} \cdot \frac{C_c}{C_1 + C_c} = g_{m1} \cdot \frac{1}{1 + C_1/C_c}$$

# Nested-Miller Compensation



$$a(s) = \frac{N(s)}{D(s)} = \frac{a_0 + a_1s + a_2s^2}{1 + b_1s + b_2s^2 + b_3s^3}$$

$$a_0 = g_{m1}g_{m2}g_{m3}R_1R_2R_3$$

$$a_1 = -(g_{m2}R_2C_{c1} + C_{c2})g_{m1}R_1R_3$$

$$a_2 = -g_{m1}R_1R_2R_3C_{c2}(C_2 + C_{c1})$$

# Nested-Miller Compensation

---

$$b_1 = K + R_1(C_{c2} + C_1) + g_{m2}R_2g_{m3}R_3R_1C_{c2}$$

$$b_2 = R_2R_3(C_3 + C_{c1} + C_{c2})(C_2 + C_{c1}) - R_2R_3C_{c1}^2 + R_1(C_{c2} + C_1)K \\ - g_{m2}R_2C_{c1}C_{c2}R_1R_3 - R_1R_3C_{c2}^2$$

$$b_3 = R_1R_2R_3[(C_3C_{c2} + C_1C_3 + C_1C_{c2})(C_2 + C_{c1}) + C_1C_{c1}C_{c2} + C_1C_2C_{c1}]$$

$$K = R_3(C_3 + C_{c1} + C_{c2}) + R_2(C_2 + C_{c1}) + R_2C_{c1}g_{m3}R_3$$

The dominant pole is

$$p_1 \approx -\frac{1}{R_1C_{c2}(g_{m2}R_2g_{m3}R_3)}$$

If  $C_{c1} \gg C_{1,2}$ , then  $|p_2| \ll |p_3|$ , and

$$p_2 \approx -\frac{g_{m2}g_{m3}}{(g_{m3} - g_{m2})C_{c1}} \quad p_3 \approx -\frac{(g_{m3} - g_{m2})C_{c1}}{C_2C_3 + C_{c1}(C_2 + C_3)} \approx -\frac{g_{m3} - g_{m2}}{C_2 + C_3}$$

# Nested-Miller Compensation

---

- To ensure  $p_2$  and  $p_3$  are in the LHP, want  $g_{m3} > g_{m2}$ .
- If  $|p_1| \ll |p_2| \ll |p_3|$ ,

$$p_1 \propto \frac{1}{C_{c2}} \quad p_2 \propto \frac{1}{C_{c1}} \quad p_3 \approx -\frac{g_{m3} - g_{m2}}{C_2 + C_3}$$

The two-pole model can be used by making  $|p_3| \gg \omega_t$ .

- If  $C_{c1}$  is not large enough,  $p_2$  and  $p_3$  are either complex conjugates or real but closely spaced. Higher unity-gain bandwidth may be achievable when  $p_2$  and  $p_3$  are not real and widely separated.

# Zeros in the Nested-Miller Compensation

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The numerator of  $a(s)$  is

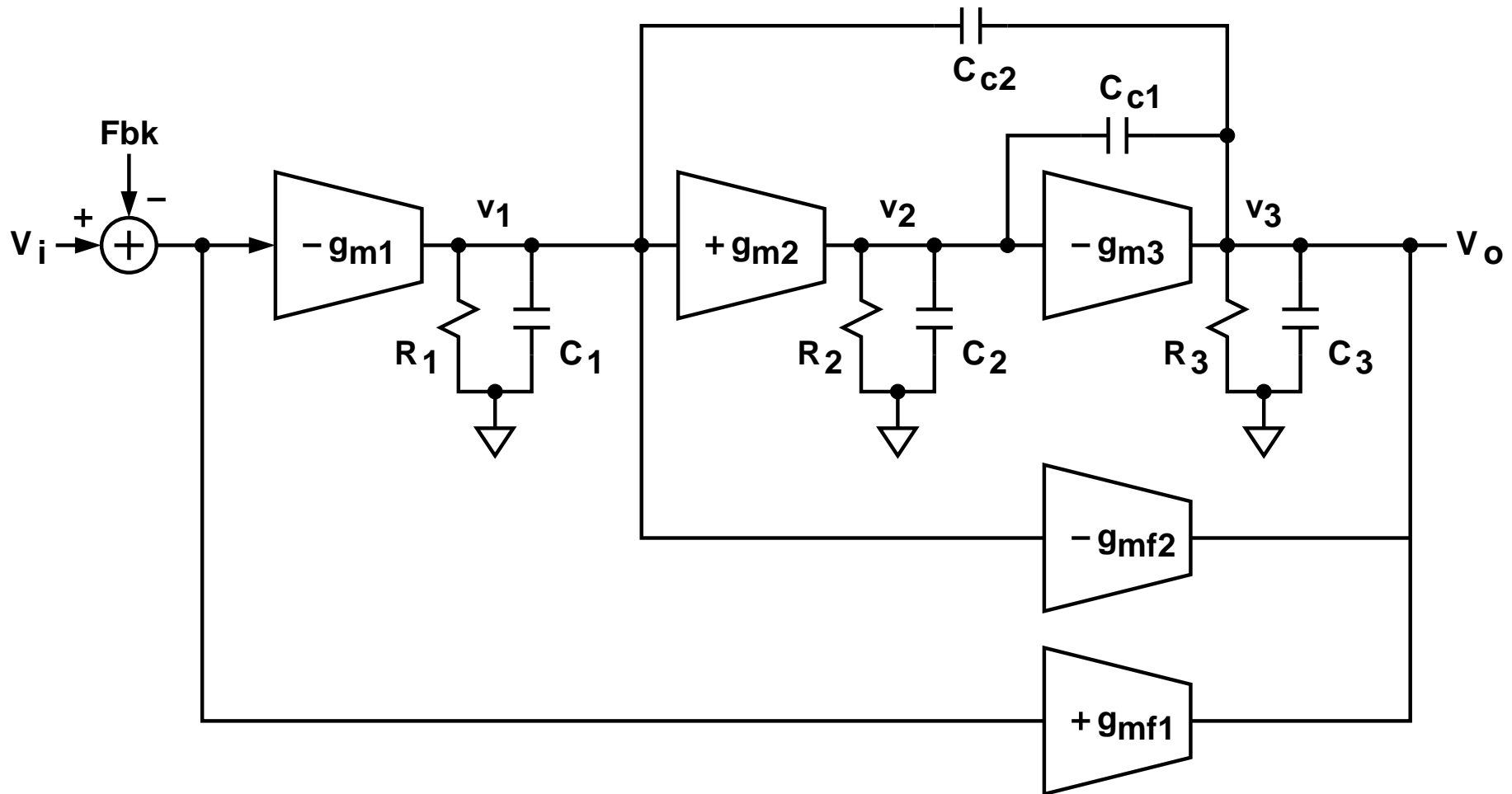
$$N(s) = g_{m1}R_1g_{m2}R_2g_{m3} \left[ 1 - s \left( \frac{C_{c1}}{g_{m3}} + \frac{C_{c2}}{g_{m2}R_2g_{m3}} \right) - s^2 \frac{C_{c2}(C_2 + C_{c1})}{g_{m2}g_{m3}} \right]$$

Assuming  $C_{c1} \gg C_2$  and  $C_{c1} \gg C_{c2}/(g_{m2}R_2)$ , then

$$N(s) \approx g_{m1}R_1g_{m2}R_2g_{m3} \left[ 1 - s \frac{C_{c1}}{g_{m3}} - s^2 \frac{C_{c2}C_{c1}}{g_{m2}g_{m3}} \right]$$
$$z_1 = -\frac{g_{m2}}{2C_{c2}} \left( 1 + \sqrt{1 + \frac{4g_{m3}C_{c2}}{g_{m2}C_{c1}}} \right) \quad z_2 = -\frac{g_{m2}}{2C_{c2}} \left( 1 - \sqrt{1 + \frac{4g_{m3}C_{c2}}{g_{m2}C_{c1}}} \right)$$

- $z_1$  is a LHP zero and  $z_2$  is a RHP zero.  $|z_1| > |z_2|$
- $|z_1|$  and/or  $|z_2|$  can be comparable to  $|\rho_2|$ , thus degrading phase margin.

# Nested-Miller Compensation with Feedforward Transconductors



$$a(s) = -\frac{R_3(n_0 + n_1s + n_2s^2)}{1 + b'_1s + b'_2s^2 + b'_3s^3}$$

# Nested-Miller Compensation with Feedforward Transconductors

---

$$b'_1 = b_1 + g_{mf2}R_1R_3C_{c2}$$

$$b'_2 = b_2 + g_{mf2}R_1R_2R_3(C_2 + C_{c1})C_{c2}$$

$$b'_3 = b_3$$

$$n_0 = -g_{m1}g_{m2}g_{m3}R_1R_2 - g_{mf1} - g_{m1}g_{mf2}R_1$$

$$n_1 = g_{m1}(g_{m2} - g_{mf2})R_1R_2C_{c1} + (g_{m1} - g_{mf1})R_1C_{c2} \\ - g_{mf1}R_2(C_2 + C_{c1}) - g_{mf1}R_1C_1 - g_{m1}g_{mf2}R_1R_2C_2$$

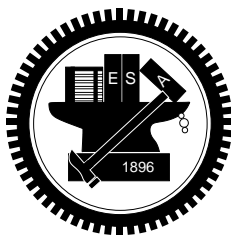
$$n_2 = (g_{m1} - g_{mf1})R_1R_2(C_2 + C_{c1})C_{c2} - g_{mf1}R_1R_2(C_2 + C_{c1})C_1$$

- To eliminate zeros, one can set  $n_1 = n_2 = 0$ .
- If  $g_{mf1} = g_{m1}$  and  $g_{mf2} = g_{m2}$ , then  $n_0$ ,  $n_1$ , and  $n_2$  are all negative, and both zeros are in the LHP.
- With  $g_{mf1} = g_{m1}$  and  $g_{mf2} = g_{m2}$ ,  $b_1 \approx a_1$  and the dominant pole  $p_1$  is not changed by  $g_{mf}$ . However,  $p_2$  and  $p_3$  will be different from the case without  $g_{mf1}$  and  $g_{mf2}$ .

# Basic Two-Stage Operational Amplifier Design

Jieh-Tsorng Wu

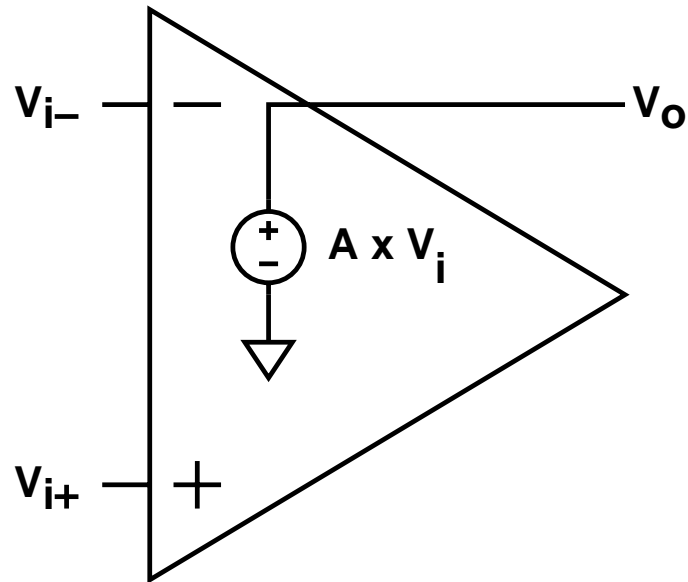
December 23, 2002



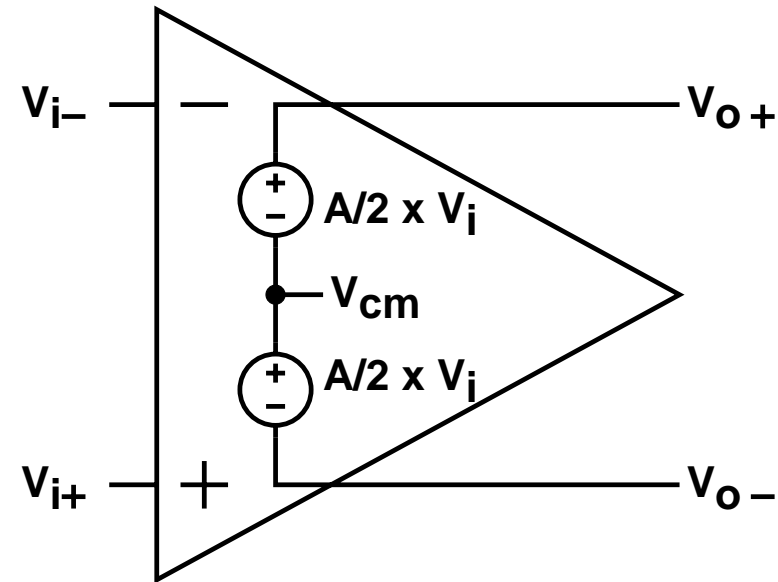
National Chiao-Tung University  
Department of Electronics Engineering

# Ideal Operational Amplifier

## Single-Ended Output

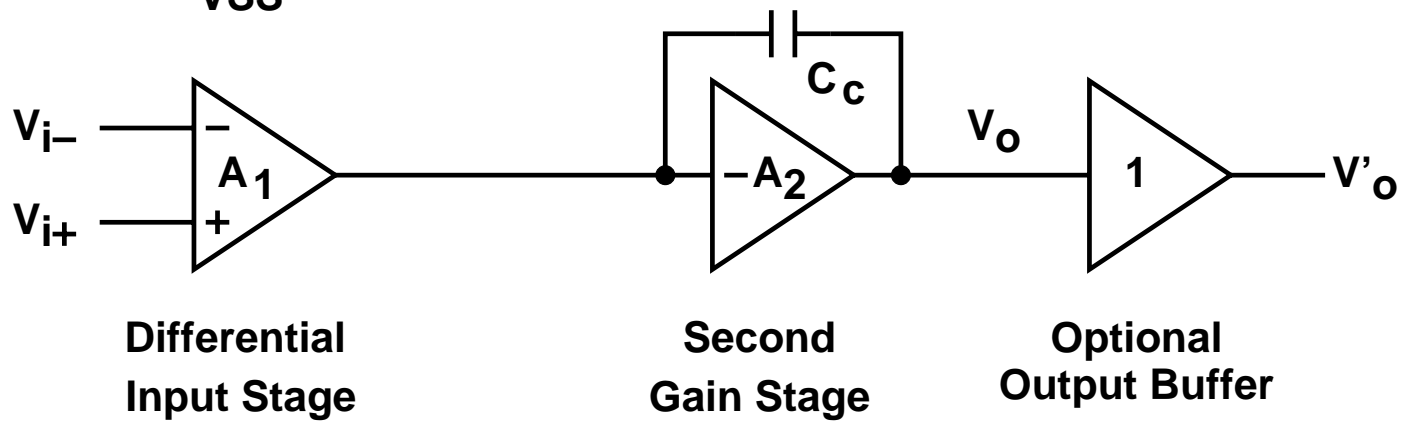
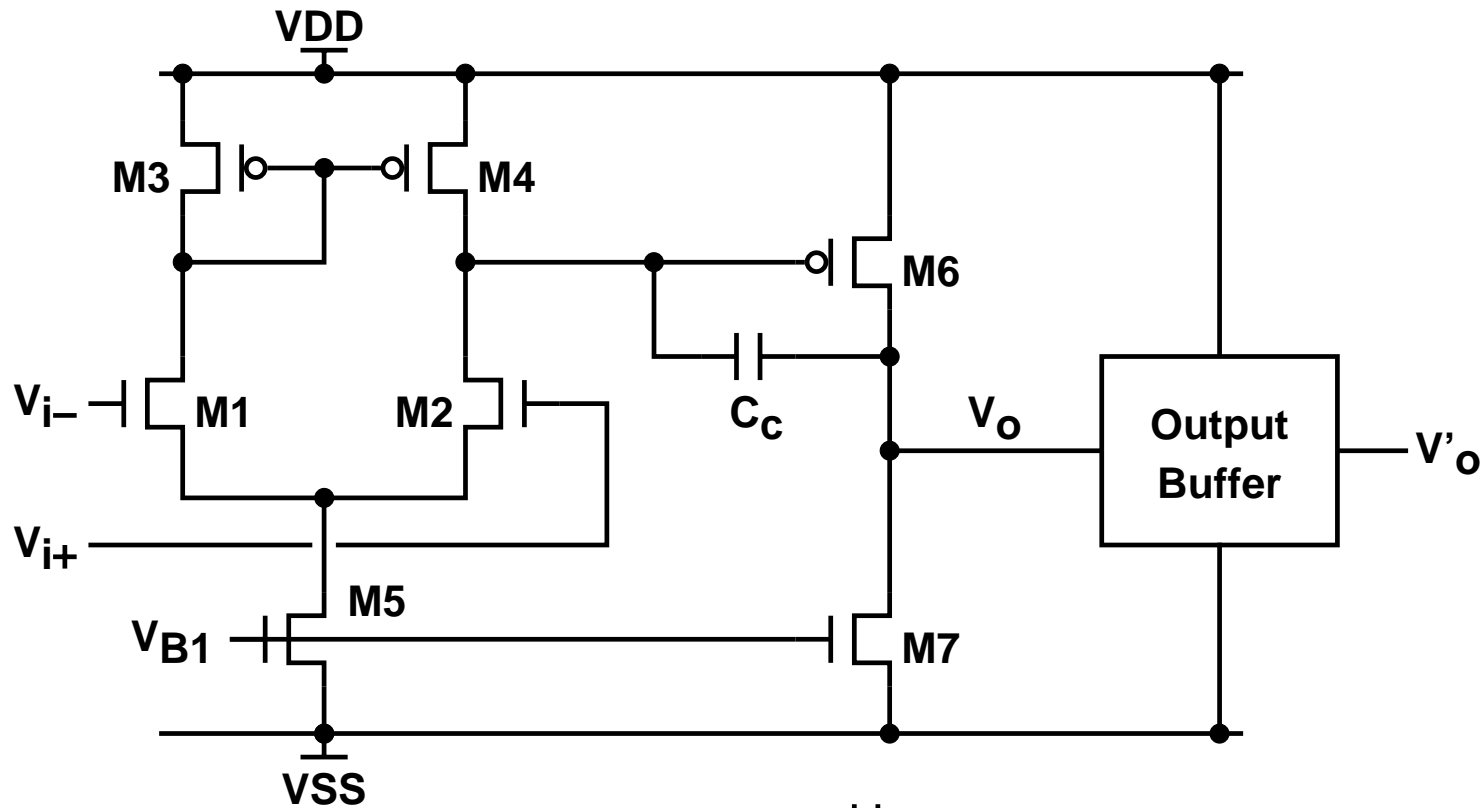


## Fully Differential

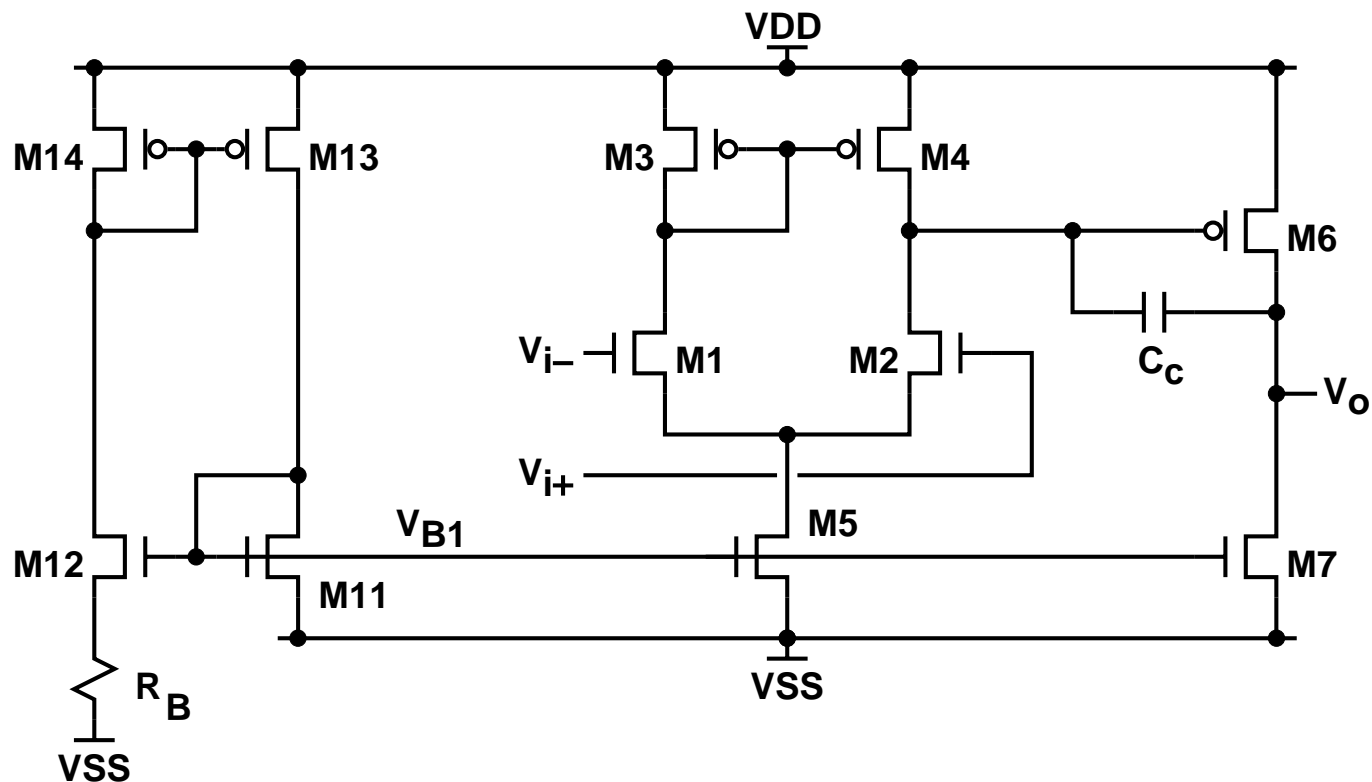


- $V_o = A \times V_i$
- Ideal opamp:
  - $A \rightarrow \infty$ ,  $Z_{in} \rightarrow \infty$ ,  $Z_{out} \rightarrow 0$ .
  - No frequency dependence.

# Basic 2-Stage CMOS Opamp



# Constant $g_m$ Bias Generator



$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$$

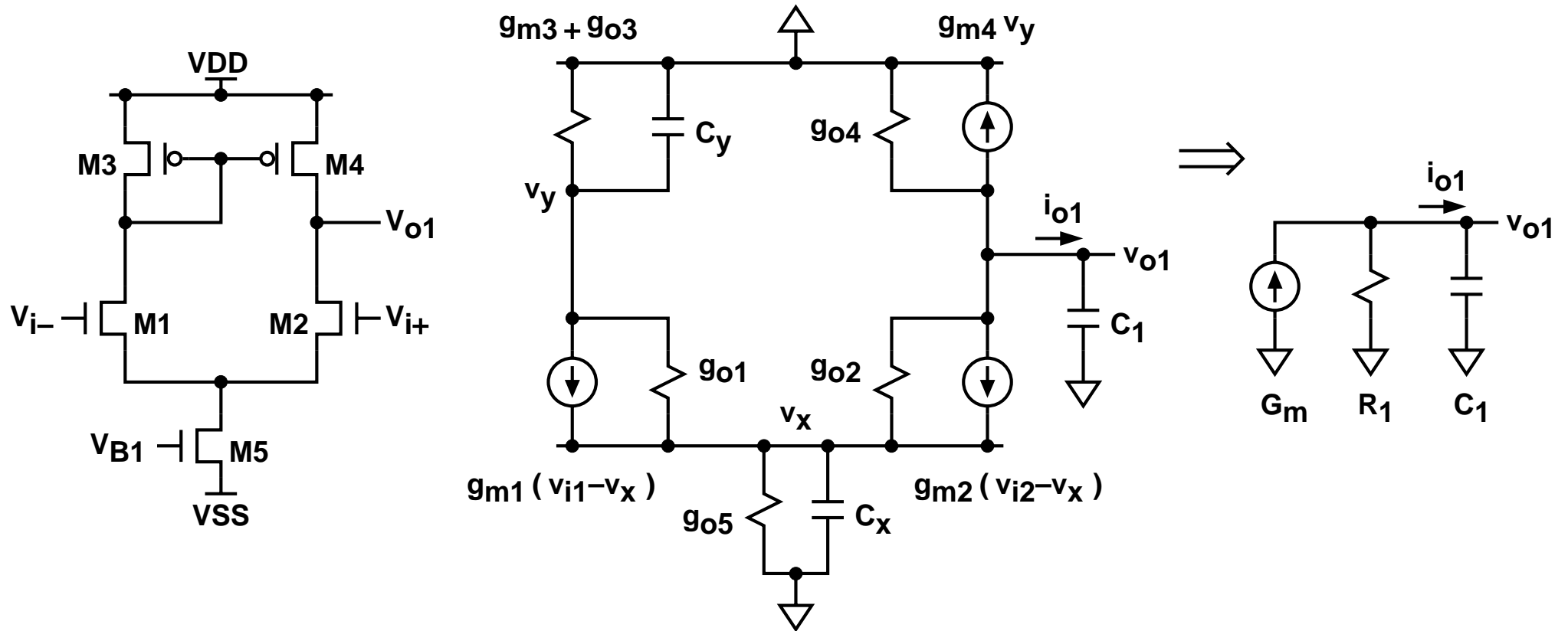
$$\left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14}$$

$$\left(\frac{W}{L}\right)_{12} = \alpha \cdot \left(\frac{W}{L}\right)_{11}$$

$$g_m = \sqrt{2\mu C_{ox}(W/L)I_D} \quad g_{m11} = \frac{2}{R_B} \frac{\sqrt{\alpha} - 1}{\sqrt{\alpha}} \quad g_{m1,m2} = g_{m11} \cdot \sqrt{\frac{(W/L)_1}{(W/L)_{11}}} \sqrt{\frac{1}{2} \frac{(W/L)_5}{(W/L)_{11}}}$$

$$g_{m3,m4} = g_{m11} \cdot \sqrt{\frac{\mu_p}{\mu_n}} \sqrt{\frac{(W/L)_3}{(W/L)_{11}}} \sqrt{\frac{1}{2} \frac{(W/L)_5}{(W/L)_{11}}} \quad g_{m6} = g_{m11} \cdot \sqrt{\frac{\mu_p}{\mu_n}} \sqrt{\frac{(W/L)_6}{(W/L)_{11}}} \sqrt{\frac{(W/L)_7}{(W/L)_{11}}}$$

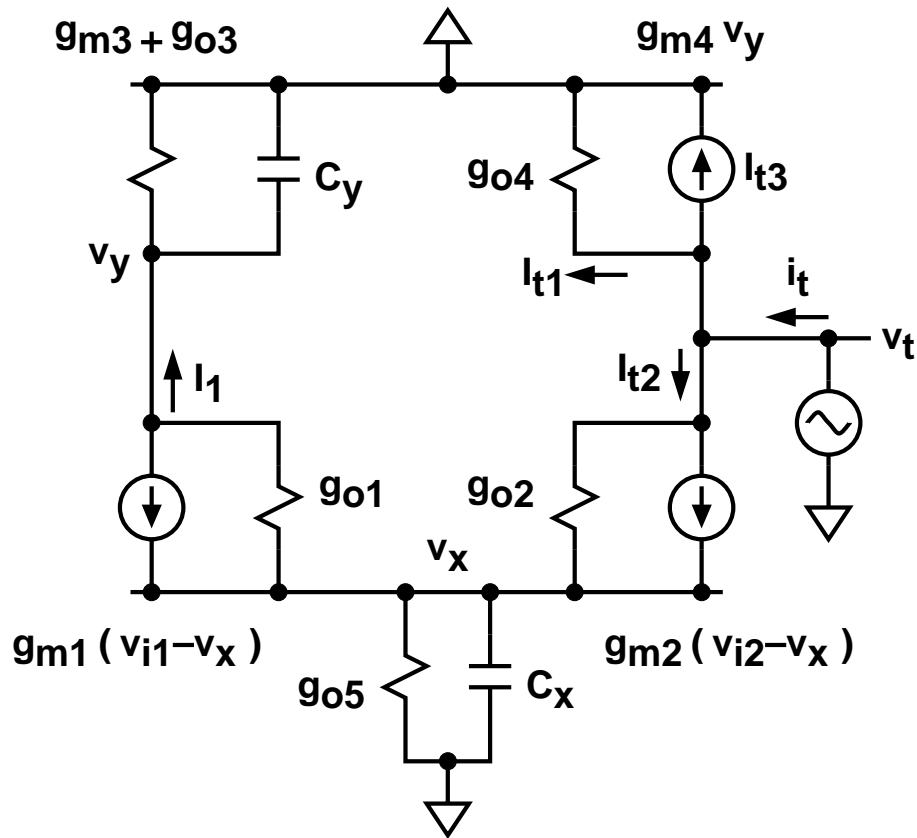
# Input Stage Small-Signal Model



$$g_{m1} = g_{m2} \quad g_{m3} = g_{m4} \quad g_{o1} = g_{o2} \quad g_{o3} = g_{o4} \quad g_m \gg g_o$$

$$C_y \approx C_{gs3} + C_{gs4} = 2C_{gs3}$$

# Input Stage Output Impedance



$$v_{i1} = v_{i2} = 0 \quad G_1 = 1/R_1 = v_t/i_t$$

$$i_t = i_{t1} + i_{t2} + i_{t3} \quad i_{t1} = v_t \cdot g_{o4}$$

$$f \rightarrow \infty$$

$$i_{t2} \approx v_t \cdot g_{o2} \quad i_{t3} \approx i_1 \approx 0$$

$$G_1 = g_{o2} + g_{o4}$$

$$f \rightarrow 0$$

$$i_{t2} \approx v_t \cdot g_{o2}/2 \quad i_{t3} \approx i_1 \approx i_{t2}$$

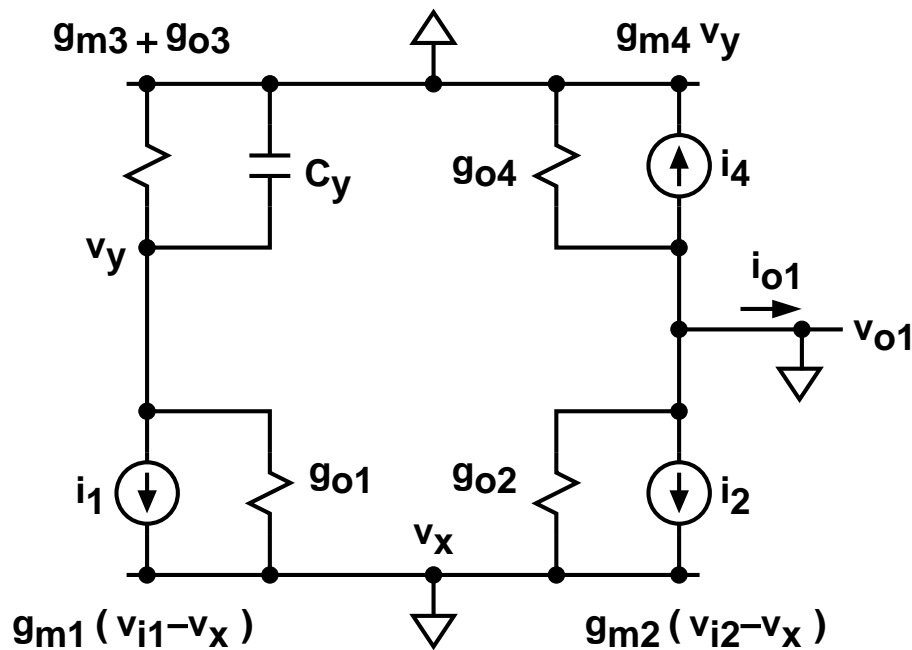
$$G_1 = g_{o2} + g_{o4}$$

$$\frac{i_{t2}}{v_t} = \frac{g_{o2}(g'_{m1} + g_{o5} + sC'_x)}{g_{m2} + g_{mb2} + g_{o2} + g'_{m1} + g_{o5} + sC'_x} \approx \frac{g_{o2}}{2} \cdot \frac{1 + sC'_x/g'_{m1}}{1 + sC'_x/(2g'_{m1})}$$

$$g'_{m1} = g_{m1} + g_{mb1}$$

$$C'_x = C_x + C_{gs1} + C_{gs2}$$

# Input Stage Differential-Mode Transconductance



$$V_{id} = V_{i2} - V_{i1} \quad V_{i1} = -\frac{1}{2}V_{id} \quad V_{i2} = +\frac{1}{2}V_{id}$$

$$i_1 = g_{m1}V_{i1} = -\frac{1}{2}g_{m1}V_{id}$$

$$i_2 = g_{m2}V_{i2} = +\frac{1}{2}g_{m1}V_{id}$$

$$\frac{-i_4}{i_1} = \frac{g_{m4}}{g_{m3} + g_{o1} + g_{o3} + sC_y} \approx \frac{g_{m3}}{g_{m3} + sC_y}$$

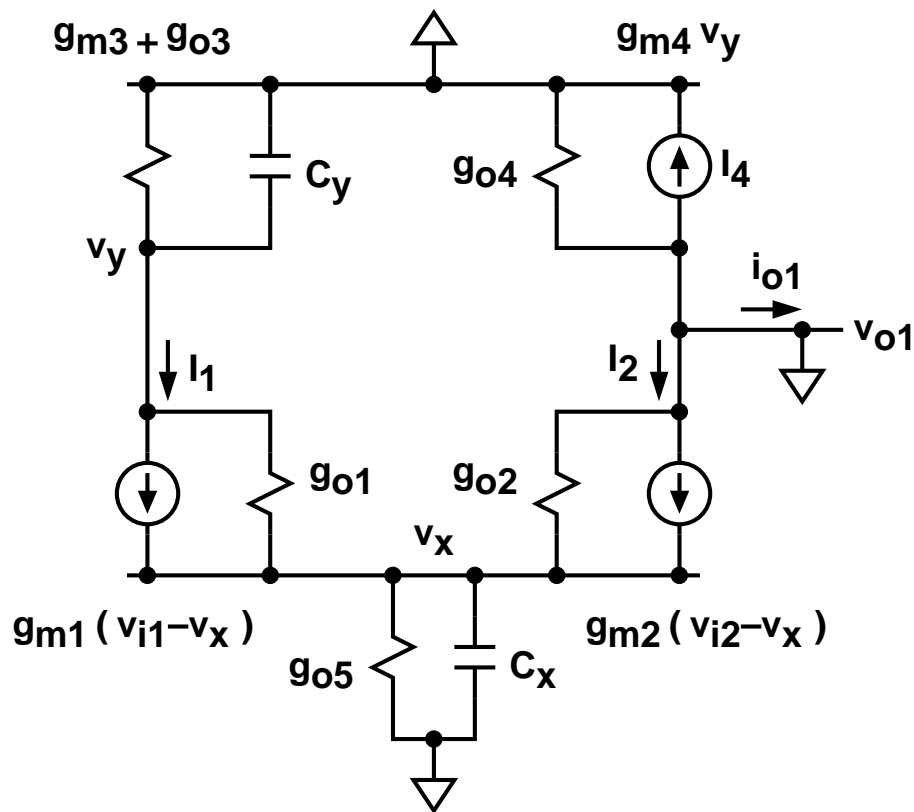
$$i_o = -i_4 - i_2$$

$$G_{md}(s) \equiv \frac{i_o}{V_{id}} = -\frac{1}{2}g_{m1} \left[ 1 + \frac{g_{m3}}{g_{m3} + sC_y} \right] = -g_{m1} \cdot \frac{1 + sC_y/(2g_{m3})}{1 + sC_y/g_{m3}} = -g_{m1} \cdot \frac{1 - s/z_m}{1 - s/p_m}$$

$$z_m = \text{Mirror Zero} = -\frac{2g_{m3}}{C_y} \approx -\omega_{t3}$$

$$p_m = \text{Mirror Pole} = -\frac{g_{m3}}{C_y} \approx -\frac{\omega_{t3}}{2}$$

# Input Stage Common-Mode Transconductance



$$V_{ic} = V_{i1} = V_{i2}$$

$$i_1 = i_2(1 - \epsilon_d)$$

$$-i_4 = i_1(1 - \epsilon_m)$$

$$i_{o1} = -i_4 - i_2 = i_1(1 - \epsilon_m) - i_2$$

$$\Rightarrow i_{o1} = -i_2(\epsilon_d + \epsilon_m - \epsilon_d\epsilon_m) \approx -i_2(\epsilon_d + \epsilon_m)$$

$$G_{mc} = \frac{i_{o1}}{V_{ic}} \approx -\frac{i_2}{V_{ic}} \cdot (\epsilon_d + \epsilon_m)$$

$$\frac{i_2}{V_{ic}} = \frac{g_{m1}}{1 + \frac{2(g_{m1} + g_{mb1})}{(g_{o5} + sC_x)}} = \frac{g_{m1}(g_{o5} + sC_x)}{2(g_{m1} + g_{mb1}) + g_{o5} + sC_x} \approx \frac{g_{o5} + sC_x}{2 + sC_x/g_{m1}} = \frac{g_{o5}}{2} \cdot \frac{1 - s/z_t}{1 - s/p_t}$$

$$z_t = \text{Tail Zero} = -\frac{g_{o5}}{C_x} \quad p_t = \text{Tail Pole} = -\frac{2g_{m1}}{C_x}$$

# Input Stage Common-Mode Transconductance

---

For the M1-M2 source-coupled pair,

$$i_1 = g_{m1}(v_{ic} - v_x) + g_{o1}(v_y - v_x)$$

$$i_2 = g_{m2}(v_{ic} - v_x) + g_{o2}(0 - v_x) = g_{m1}(v_{ic} - v_x) - g_{o1}v_x$$

$$v_y = -\frac{i_1}{g_{m3} + g_{o3} + sC_y}$$

We have

$$i_1 = i_2 + g_{o1}v_y = i_2 - i_1 \cdot \frac{g_{o1}}{g_{m3} + g_{o3} + sC_y}$$

$$i_1 = i_2 \frac{1}{1 + \frac{g_{o1}}{g_{m3} + g_{o3} + sC_y}} \approx i_2 \left( 1 - \frac{g_{o1}}{g_{m3} + g_{o3} + sC_y} \right) = i_2(1 - \epsilon_d)$$

$$\epsilon_d = \frac{g_{o1}}{g_{m3} + g_{o3} + sC_y} \approx \frac{g_{o1}}{g_{m3} + sC_y} = \frac{g_{o1}}{g_{m3}} \cdot \frac{1}{1 + sC_y/g_{m3}} = \frac{g_{o1}}{g_{m3}} \cdot \frac{1}{1 - s/p_m}$$

# Input Stage Common-Mode Transconductance

---

For the M3-M4 current mirror,

$$-\frac{i_4}{i_1} = \frac{g_{m4}}{g_{m3} + g_{o3} + sC_y} = \frac{g_{m3}}{g_{m3} + g_{o3} + sC_y} = 1 - \frac{g_{o3} + sC_y}{g_{m3} + g_{o3} + sC_y} = 1 - \epsilon_m$$

$$\epsilon_m = \frac{g_{o3} + sC_y}{g_{m3} + g_{o3} + sC_y} \approx \frac{g_{o3} + sC_y}{g_{m3} + sC_y} = \frac{g_{o3}}{g_{m3}} \cdot \frac{1 + sC_y/g_{o3}}{1 + sC_y/g_{m3}} = \frac{g_{o3}}{g_{m3}} \cdot \frac{1 + sC_y/g_{o3}}{1 - s/p_m}$$

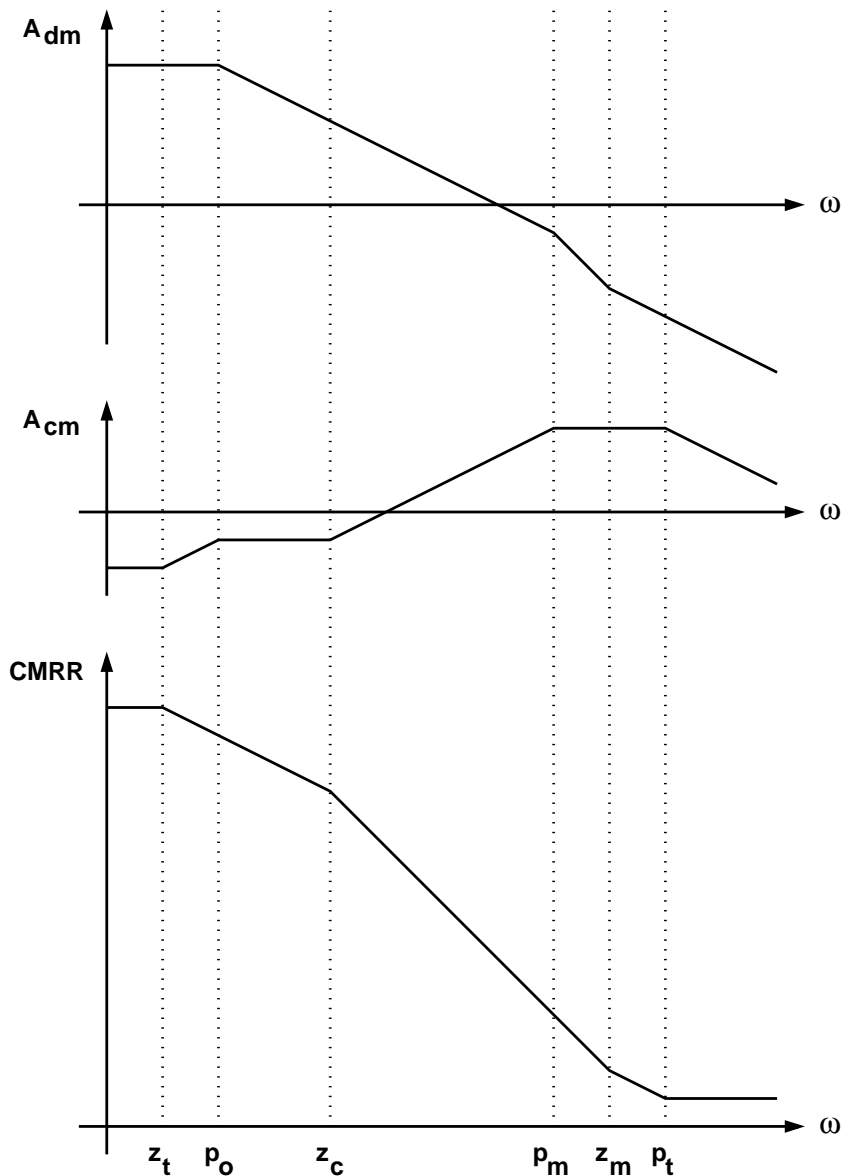
The common-mode transconductance is

$$G_{mc}(s) \approx -\frac{i_2}{V_{ic}} \cdot (\epsilon_d + \epsilon_m)$$

$$\approx -\frac{g_{o5}}{2} \cdot \frac{1 - s/z_t}{1 - s/p_t} \cdot \left( \frac{g_{o1}}{g_{m3}} \cdot \frac{1}{1 - s/p_m} + \frac{g_{o3}}{g_{m3}} \cdot \frac{1 + sC_y/g_{o3}}{1 - s/p_m} \right)$$

$$= -\frac{g_{o5}(g_{o1} + g_{o3})}{2g_{m3}} \cdot \frac{(1 - s/z_t)(1 - s/z_c)}{(1 - s/p_t)(1 - s/p_m)} \quad z_c = -\frac{g_{o1} + g_{o3}}{C_y}$$

# Input Stage Voltage Gain



$$A_{dm} = G_{dm} \cdot Z_1 \quad A_{cm} = G_{cm} \cdot Z_1$$

$$Z_1 = \frac{1}{G_1 + sC_1} = \frac{1}{g_{o2} + g_{o4}} \cdot \frac{1}{1 - s/p_o}$$

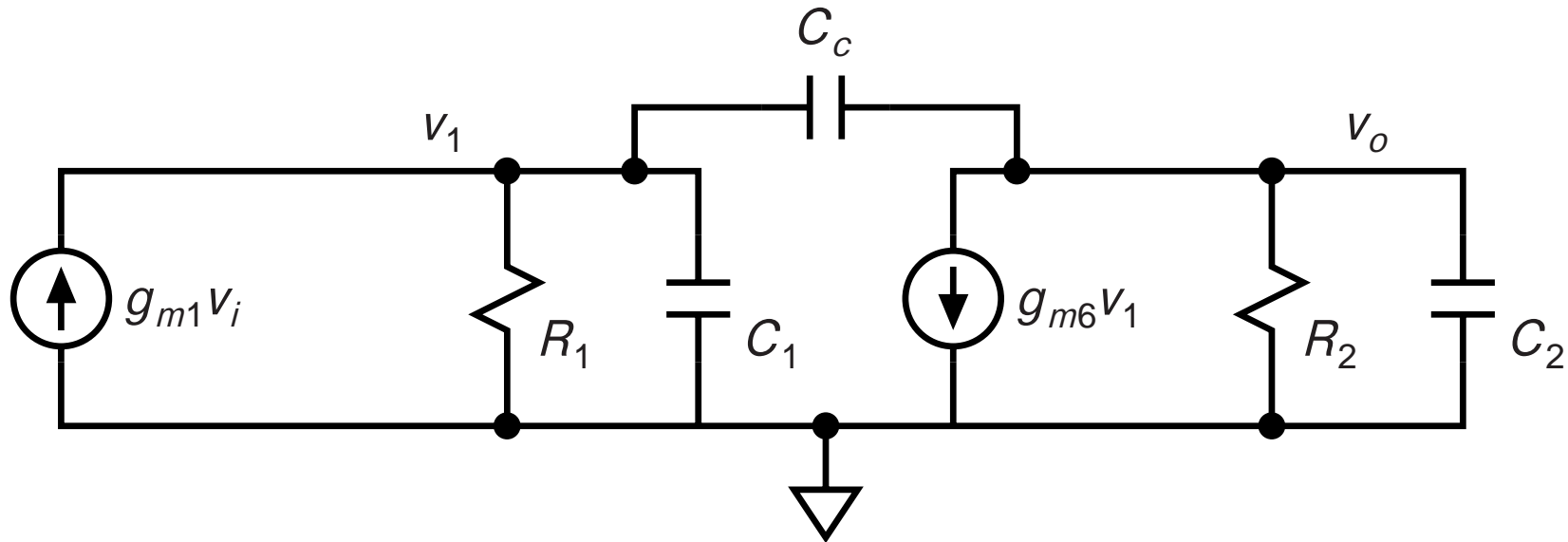
$$p_o = \text{Output Load Pole} = -\frac{g_{o2} + g_{o4}}{C_1}$$

$$\text{CMRR} = \left| \frac{G_{md}}{G_{mc}} \right|$$

$$= \frac{2g_{m1}g_{m3}}{g_{o5}(g_{o1} + g_{o3})} \cdot \frac{(1 - s/z_m)(1 - s/p_t)}{(1 - s/z_t)(1 - s/z_c)}$$

$$\text{CMRR}(\infty) = \frac{g_{m1}/2}{g_{m1}} = \frac{1}{2}$$

## Simplified Two-Stage Model



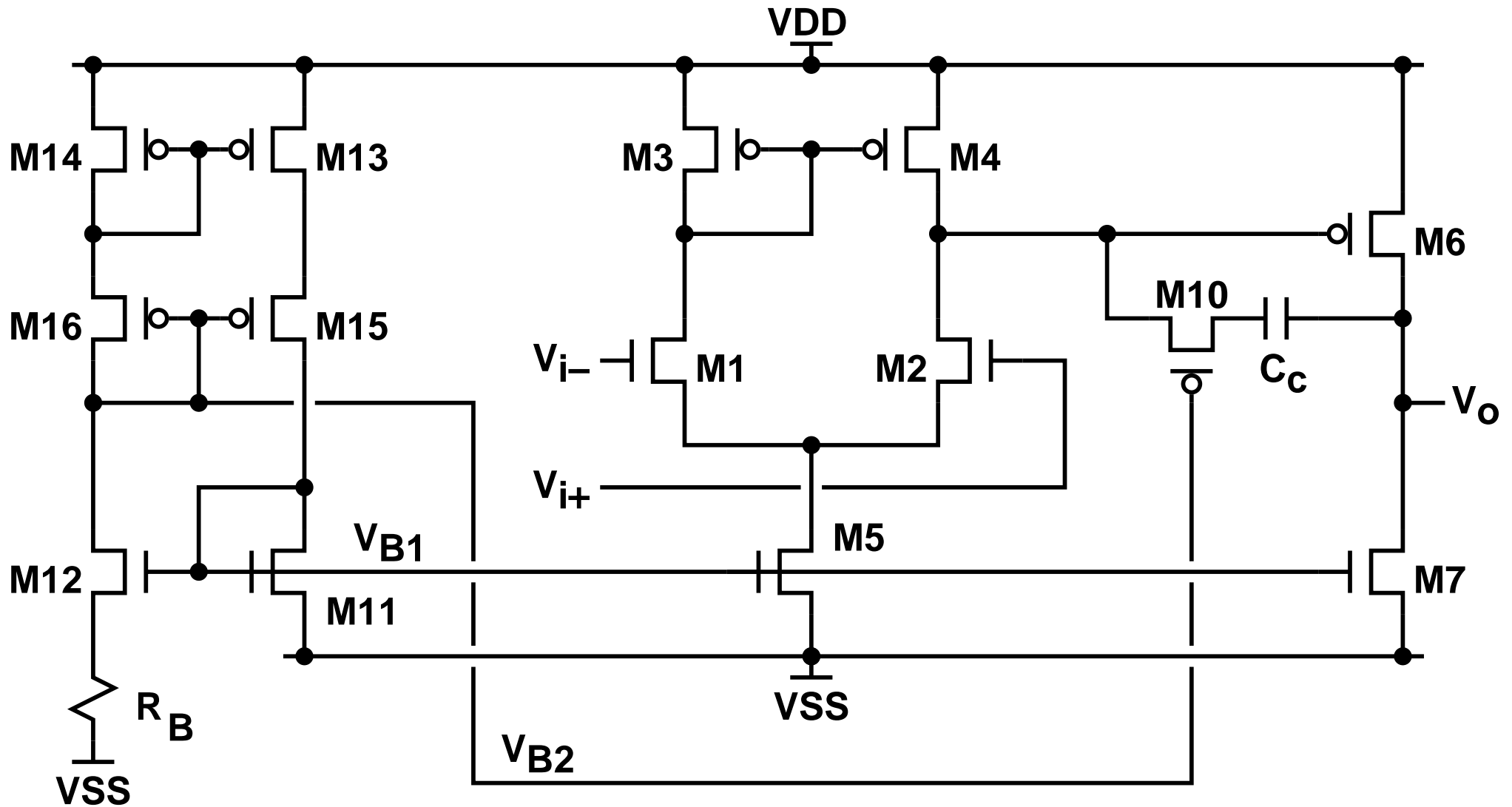
$$G_1 = g_{o2} + g_{o4} \quad G_2 = g_{o6} + g_{o7} \quad C_1 \simeq C_{gs6}$$

$$A_v \equiv \frac{V_o}{V_i} = A_v(0) \frac{1 - s/z_1}{(1 - s/p_1)(1 - s/p_2)}$$

$$A_v(0) = g_{m1}g_{m6}R_1R_2$$

$$p_1 \approx -\frac{g_{m1}}{C_c} \times \frac{1}{A_v(0)} \quad p_2 \approx -\frac{g_{m6}}{C_1 + C_2} \quad z_1 = +\frac{g_{m6}}{C_c}$$

# Frequency Compensation Using Nulling Resistor



# Frequency Compensation Using Zero-Nulling Resistor

---

- The zero-nulling resistor  $R_c$  is realized by M10 in the triode region.

$$z_1 = \frac{1}{(1/g_{m6} - R_c)C_c} = -\frac{g_{m6}}{(g_{m6}R_c - 1)C_c}$$

- Let  $\frac{(W/L)_{13}}{(W/L)_{14}} = \frac{(W/L)_{15}}{(W/L)_{16}}$  and  $\frac{(W/L)_7}{(W/L)_{11}} = \frac{(W/L)_6}{(W/L)_{13}}$ , then

$$V_{ov6} = V_{ov13} = V_{ov14} \quad V_{ov10} = V_{ov15} = V_{ov16} \quad \frac{V_{ov6}}{V_{ov10}} = \frac{V_{ov13}}{V_{ov15}} = \sqrt{\frac{(W/L)_{15}}{(W/L)_{13}}}$$

$$g_{m6}R_c = \frac{g_{m6}}{g_{m10}} = \frac{(W/L)_6}{(W/L)_{10}} \frac{V_{ov6}}{V_{ov10}} = \frac{(W/L)_6}{(W/L)_{10}} \sqrt{\frac{(W/L)_{15}}{(W/L)_{13}}}$$

- $p_2/z_1 \approx (g_{m6}R_c - 1)C_c/(C_1 + C_2)$  is independent of process and temperature variations.

# Voltage and Current Range

---

## Input Common-Mode Range

$$V_{ic(max)} = V_{DD} - V_{GS3} + V_{t1} \quad V_{ic(min)} = V_{SS} + V_{DSAT5} + V_{GS1}$$

- The range is limited to the voltage levels where any transistor goes out of saturation.

## Output Voltage Range

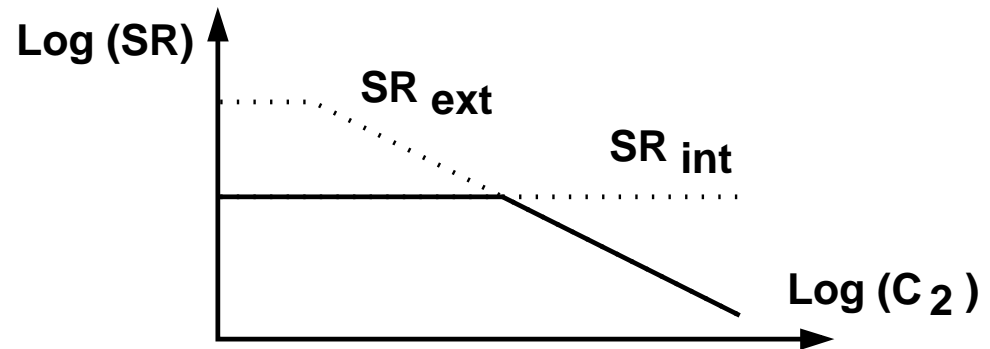
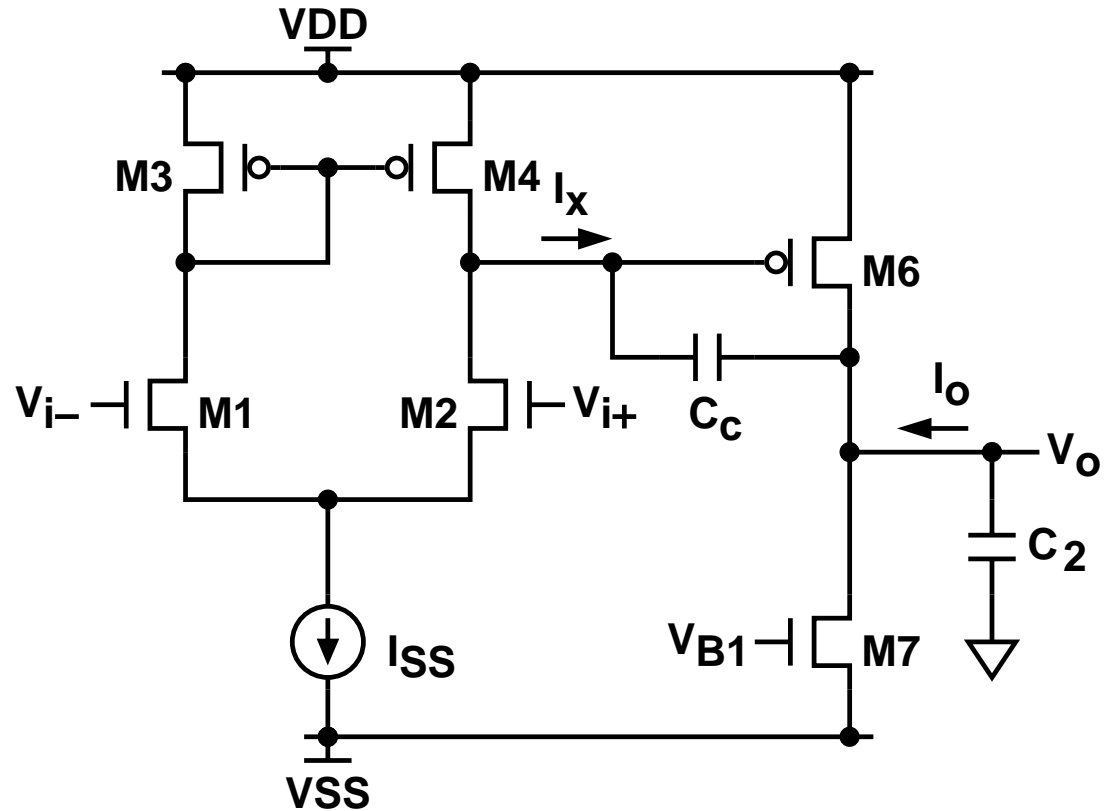
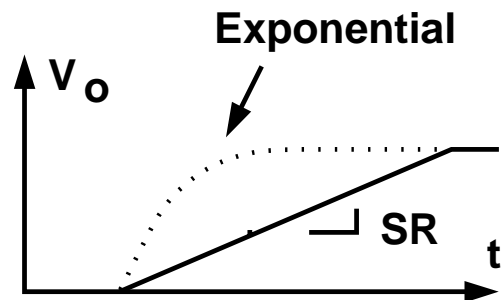
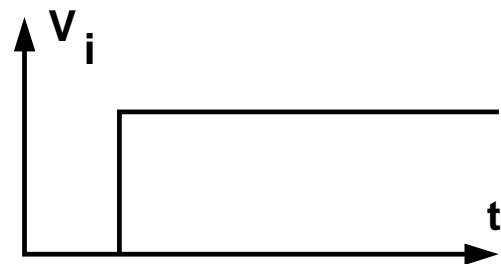
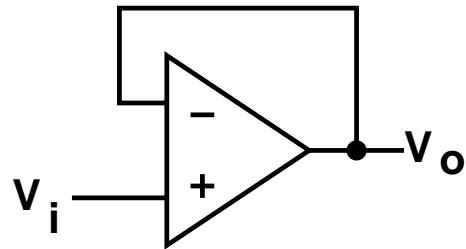
$$V_{o(max)} = V_{DD} - V_{DSAT6} \quad V_{o(min)} = V_{SS} + V_{DSAT7}$$

- Output resistive load can also limit the voltage range, if the available output current is insufficient.

## Maximum Output Current

$$I_{o(\text{sink,max})} = I_{D7} \quad I_{o(\text{source,max})} = \frac{1}{2} k'_p \left( \frac{W}{L} \right)_6 [V_{gs6(max)} - V_{t6}]^2 - I_{D7}$$
$$V_{gs6(max)} = V_{DD} - V_{i+} + V_{t2}$$

# Slew Rate



# Slew Rate

---

The *internal slew rate* is generally limited by current available to charge and discharge  $C_c$  from input stage. Therefore,

$$\begin{aligned} \text{SR}_{int} &= \left. \frac{dV_o}{dt} \right|_{max} = \frac{I_{x(max)}}{C_c} = \frac{I_{SS}}{C_c} \\ &= \frac{I_{SS}}{g_{m1}} \times \frac{g_{m1}}{C_c} = \frac{I_{SS}}{g_{m1}} \times \omega_u \\ &= (V_{GS1} - V_{t1}) \times \omega_u \\ &= V_{ov1} \times \omega_u \end{aligned}$$

The *external slew rate* is limited by the available current to charge and discharge  $C_2$ . Thus,

$$\text{SR}_{ext} = \frac{I_{D7} - I_x(max)}{C_2} = \frac{I_{D7} - I_{SS}}{C_2}$$

# Settling Time

---

The frequency response and step response of a single-pole amplifier is

$$A(s) = \frac{A_o}{1 + s/\omega_p} \quad V_o(t) = A_o (1 - e^{-\omega_p t})$$

The settling time can be written as

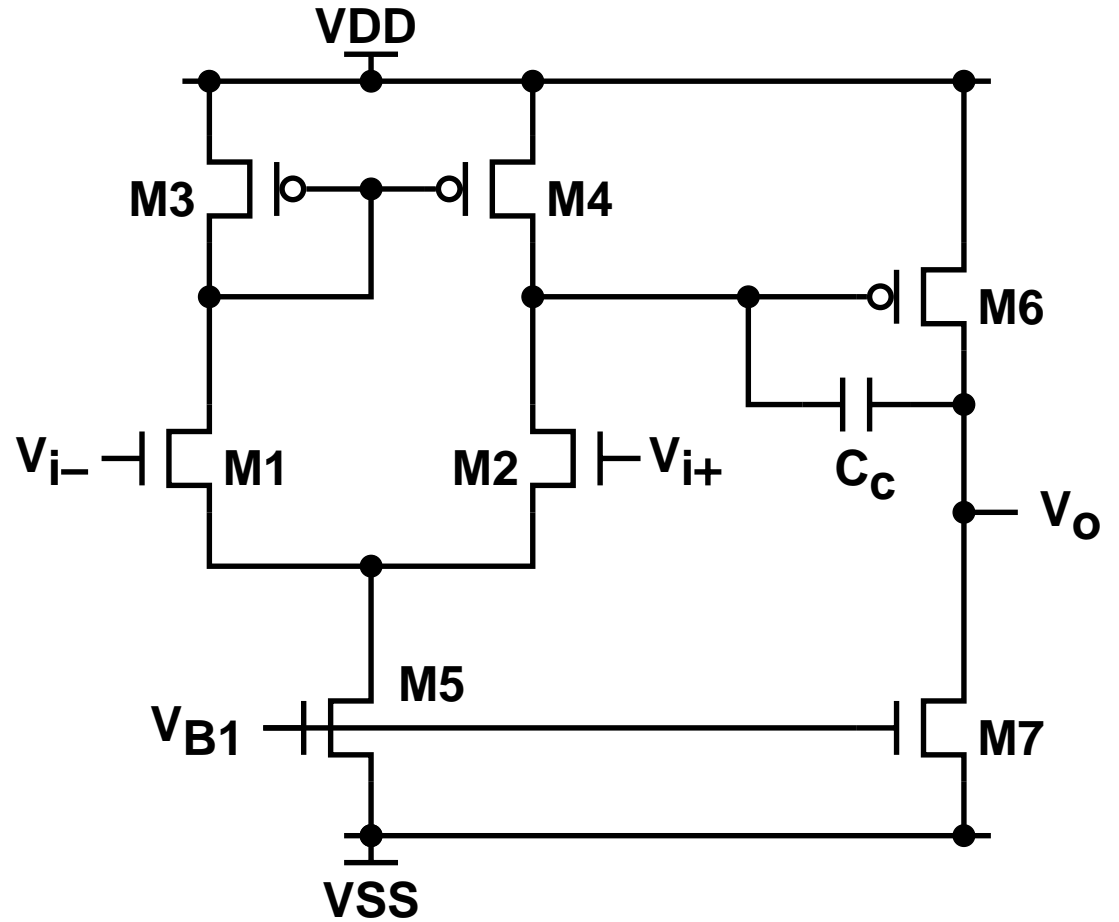
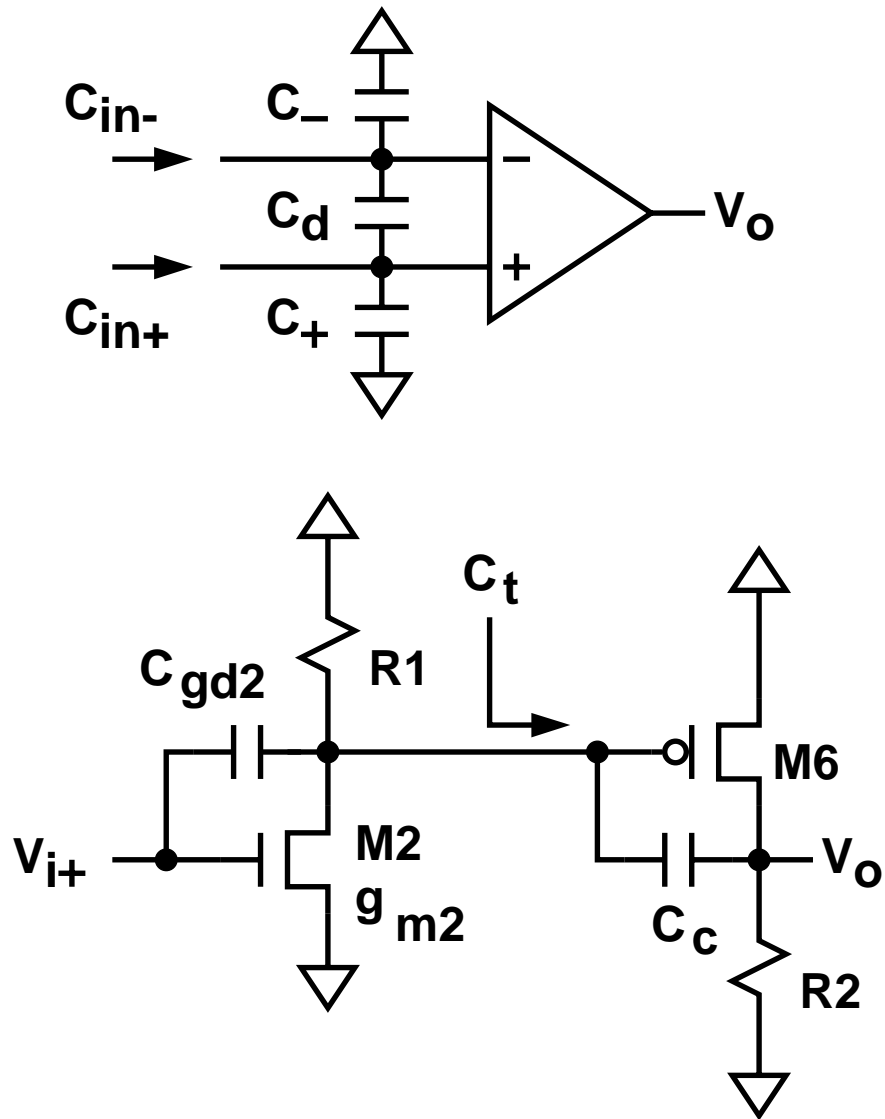
$$t_s(\epsilon) = \frac{1}{\omega_p} \ln \frac{1}{\epsilon} = \frac{A_o}{\omega_u} \ln \frac{1}{\epsilon}$$

- $\omega_u = A_o \cdot \omega_p$  is the dominant-pole unity-gain frequency.
- $\epsilon = 1 - |V_o(t_s)/A_o|$  is the error when settling occurs.

The 10% to 90% rise time is

$$t_r = \frac{1}{\omega_p} \ln(9) = \frac{2.2}{\omega_p} = \frac{0.35}{f_p} \quad \omega_p = 2\pi f_p$$

# Input Impedance



# Input Impedance

---

Shorting the noninverting input to ground,

$$C_{in-} = C_d + C_- \approx \frac{C_{gs1}}{2}$$

Shorting the inverting input to ground,

$$C_{in+} = C_d + C_+ \approx \frac{C_{gs1}}{2} + C_{gd2} \cdot (1 + A_{o1}) \quad A_{o1} = g_{m2}R_1$$

And we have

$$C_d \approx \frac{C_{gs2}}{2} \quad C_- \approx 0 \quad C_+ \approx C_{gd2} \cdot (1 + A_{o1})$$

# Input Impedance

---

The equivalent voltage gain of the M2 stage decreases with increasing frequency, due to the effect of  $C_t$ . The capacitance  $C_+$  is then modified as

$$C_+ \approx C_{gd2} \cdot A_{o1} \cdot \frac{1 + \frac{C_{gd2}}{g_{m2}}s}{1 + A_{o1} \frac{C_{gd2} + C_t}{g_{m2}}s}$$

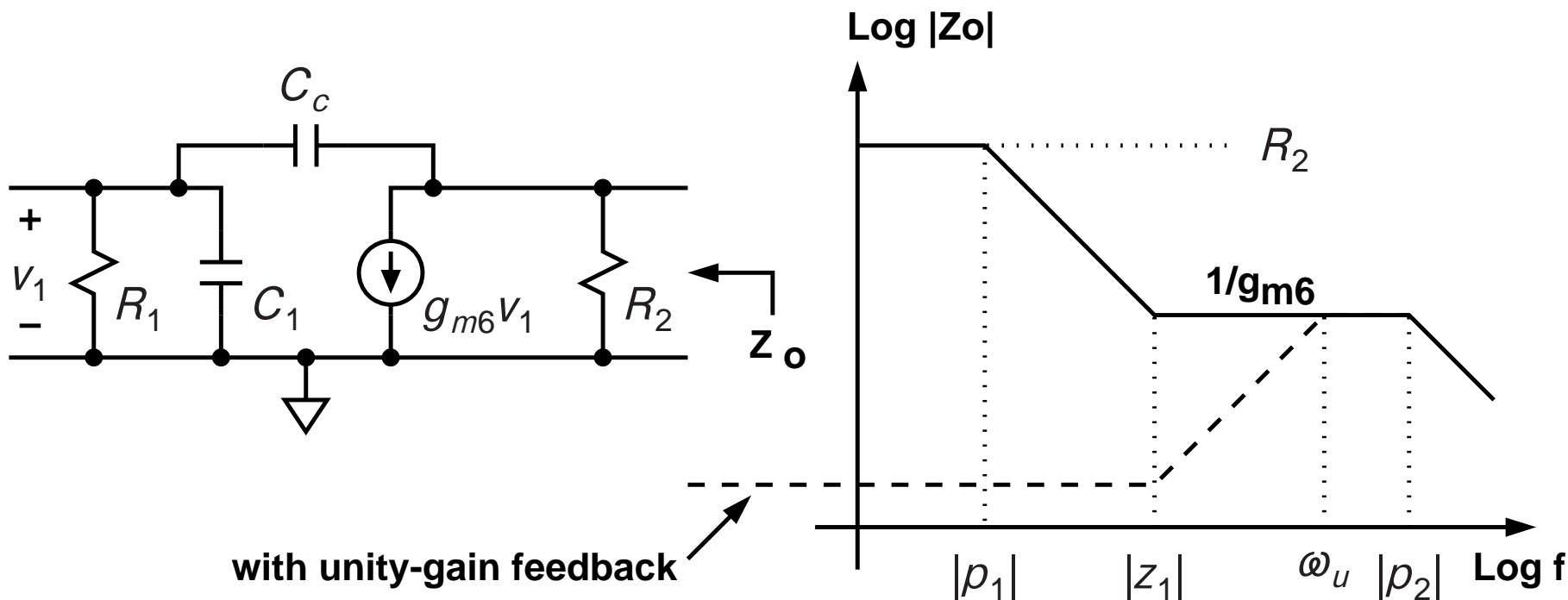
where

$$C_t = C_{gs6} + C_c \cdot (1 + A_{o2}) = C_{gs6} + C_c \cdot (1 + g_{m6}R_2)$$

- For  $g_{m2}/[A_{o1}(C_{gd2} + C_t)] < \omega < g_{m2}/C_{gd2}$ ,  $C_+$  become resistive, and

$$C_+ \rightarrow R_+ \approx \frac{1}{g_{m2}} \cdot \left( 1 + \frac{C_t}{C_{gd2}} \right)$$

# Output Impedance



Assuming  $g_{m6} \gg R_1$  and  $R_2$ , we have

$$Z_o = R_2 \cdot \frac{1 + sR_1(C_c + C_1)}{1 + sg_{m6}R_1R_2C_c + s^2R_1C_1R_2C_c}$$

$$p_1 \approx -\frac{1}{g_{m6}R_1R_2C_c} = -\frac{g_{m1}}{C_c} \cdot \frac{1}{|A_v(0)|} \quad p_2 \approx -\frac{g_{m6}}{C_1} \quad z_1 \approx -\frac{1}{R_1(C_c + C_1)}$$

# Output Impedance

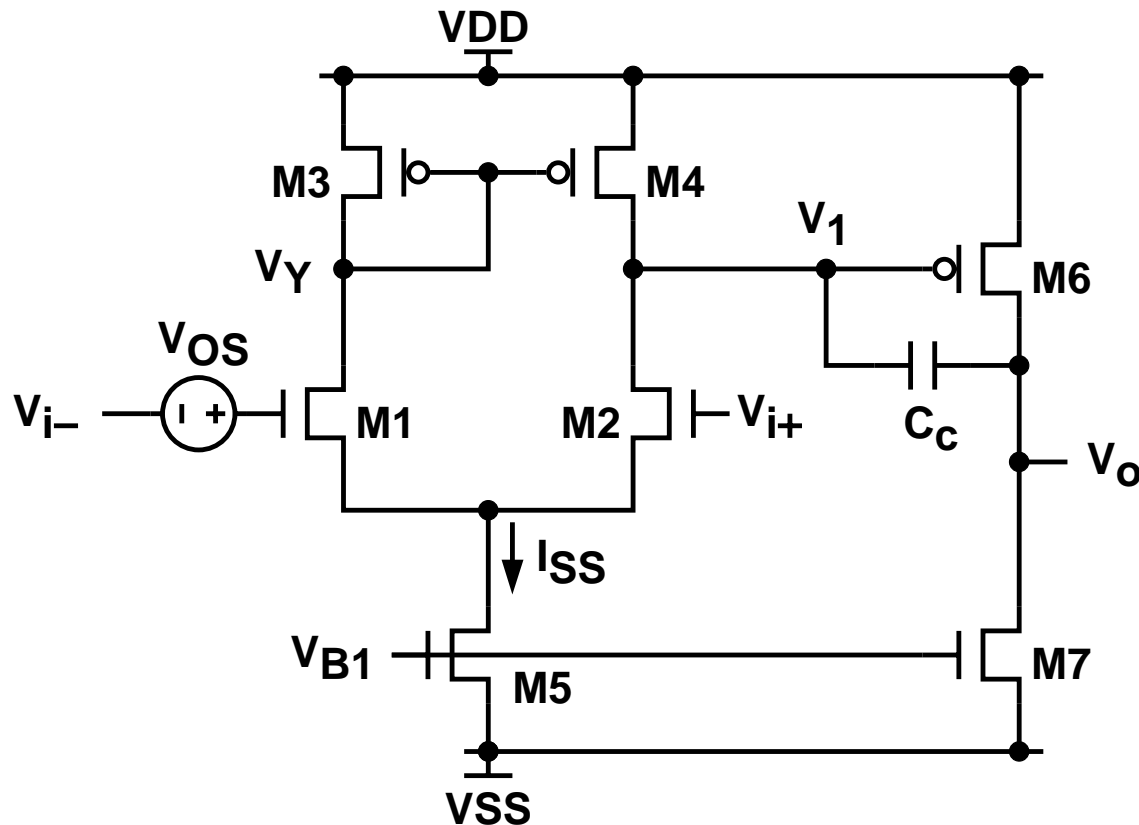
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- For frequencies larger than  $z_1$ ,  $C_c$  acts as a short, the  $Z_o$  is a resistive  $1/g_{m6}$ .
- The closed-loop  $Z_o$  of the unity-gain buffer is

$$Z_{oc} \approx \frac{Z_o}{A_v} \approx \frac{R_2}{A_v(0)} \cdot (1 - s/z_1) \quad \text{for } \omega < \omega_u$$

where  $\omega_u = g_{m1}/C_c$ .

# Systematic Input Offset Voltage



$$I_D = \frac{1}{2}kV_{ov}^2(1 + \lambda V_{DS})$$

$$\lambda_1 = \lambda_2 \quad \lambda_3 = \lambda_4$$

$$\Delta I_{1-2} = I_{D1} - I_{D2} = \frac{I_{SS}}{2}\lambda_1(V_Y - V_1)$$

$$\Delta I_{3-4} = |I_{D3}| - |I_{D4}| = \frac{I_{SS}}{2}\lambda_3(V_1 - V_Y)$$

The systematic input referred dc offset can be expressed as

$$-V_{OS,s} = \frac{1}{g_{m1}} \cdot (\Delta I_{1-2} - \Delta I_{3-4}) = \frac{V_{ov,1-2}}{2} \cdot (\lambda_1 + \lambda_3)(V_Y - V_1)$$

# Systematic Input Offset Voltage

---

- The systematic offset is caused by asymmetry in the dc biasing of  $V_Y$  and  $V_1$ .
- To minimize  $V_{OS,s}$ , want  $V_{DS3} = V_{DS4} = V_{GS6}$ , then

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{(W/L)_5}{2(W/L)_7}$$

- Further, to minimize process induced variations choose

$$L_3 = L_4 = L_6$$

However, this constraint may conflict with frequency response and noise constraints.

# Random Input Offset Voltage

$$\Delta V_{i-j} = |V_i| - |V_j| \quad V_{i-j} = \frac{|V_i| + |V_j|}{2} \quad \Delta I_{i-j} = |I_i| - |I_j| \quad I_{i-j} = \frac{|I_i| + |I_j|}{2}$$

$$\Delta \left( \frac{W}{L} \right)_{i-j} = \left( \frac{W}{L} \right)_i - \left( \frac{W}{L} \right)_j \quad \left( \frac{W}{L} \right)_{i-j} = \frac{1}{2} \left[ \left( \frac{W}{L} \right)_i + \left( \frac{W}{L} \right)_j \right]$$

$$\Rightarrow \frac{\Delta I_{D,3-4}}{I_{D,3-4}} = \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}} - 2 \frac{\Delta V_{t,3-4}}{V_{ov,3-4}} = \frac{\Delta I_{D,1-2}}{I_{D,1-2}}$$

$$-V_{OS,r} = \Delta V_{t,1-2} + \frac{V_{ov,1-2}}{2} \left[ \frac{\Delta I_{D,1-2}}{I_{D,1-2}} - \frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} \right]$$

$$= \Delta V_{t,1-2} - \frac{V_{ov,1-2}}{V_{ov,3-4}} \cdot \Delta V_{t,3-4} + \frac{V_{ov,1-2}}{2} \left[ -\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}} \right]$$

$$= \Delta V_{t,1-2} - \frac{g_{m3}}{g_{m1}} \cdot \Delta V_{t,3-4} + \frac{V_{ov,1-2}}{2} \left[ -\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}} \right]$$

# Input Offset Voltage and Common-Mode Rejection Ratio

---

The output voltage change due to common-mode input variation is

$$\Delta V_o = A_{cm} \cdot \Delta V_{ic}$$

Want to change differential input so that  $\Delta V_o = 0$ , then

$$\Delta V_{id} = -\frac{\Delta V_o}{A_{dm}} = -\frac{A_{cm}}{A_{dm}} \cdot \Delta V_{ic}$$

Therefore, we have

$$\text{CMRR} \equiv \left| \frac{A_{dm}}{A_{cm}} \right| = \left| \left( \frac{\partial V_{id}}{\partial V_{ic}} \Big|_{\Delta V_o=0} \right)^{-1} \right| = \left| \left( \frac{\partial V_{os}}{\partial V_{ic}} \right)^{-1} \right|$$

# CMRR Due to Systematic and Random Offset

---

Since

$$V_{OS} = V_{OS,s} + V_{OS,r}$$

We have

$$\frac{1}{\text{CMRR}} = \left| \frac{\partial V_{OS,s}}{\partial V_{ic}} + \frac{\partial V_{OS,r}}{\partial V_{ic}} \right|$$

$$\begin{aligned} \frac{\partial V_{OS,s}}{\partial V_{ic}} &= \frac{\partial V_{OS,s}}{\partial V_{ov1}} \cdot \frac{\partial V_{ov1}}{\partial I_{d1}} \cdot \frac{\partial I_{d1}}{\partial V_{ic}} = -\frac{1}{2}(\lambda_1 + \lambda_3)(V_Y - V_1) \cdot \frac{1}{g_{m1}} \cdot \frac{g_{m1}}{1 + 2(g_{m1} + g_{mb1})r_{o5}} \\ &= -\frac{1}{2}(\lambda_1 + \lambda_3)(V_Y - V_1) \cdot \frac{1}{1 + 2(g_{m1} + g_{mb1})r_{o5}} \approx -\frac{(\lambda_1 + \lambda_3)(V_Y - V_1)}{4(g_{m1} + g_{mb1})r_{o5}} \end{aligned}$$

$$\begin{aligned} \frac{\partial V_{OS,r}}{\partial V_{ic}} &= \frac{\partial V_{OS,r}}{\partial V_{ov1}} \cdot \frac{\partial V_{ov1}}{\partial I_{d1}} \cdot \frac{\partial I_{d1}}{\partial V_{ic}} = -\frac{1}{2} \left[ -\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}} \right] \cdot \frac{1}{1 + 2(g_{m1} + g_{mb1})r_{o5}} \\ &= -\left[ -\frac{\Delta(W/L)_{1-2}}{(W/L)_{1-2}} + \frac{\Delta(W/L)_{3-4}}{(W/L)_{3-4}} \right] \cdot \frac{1}{4(g_{m1} + g_{mb1})r_{o5}} \end{aligned}$$

# Mismatches and Input Stage Transconductance

---

Define

$$\Delta g_{m,i-j} = g_{m,i} - g_{m,j} \quad g_{m,i-j} = \frac{g_{m,i} + g_{m,j}}{2} \quad \Delta r_{o,i-j} = r_{o,i} - r_{o,j} \quad r_{o,i-j} = \frac{r_{o,i} + r_{o,j}}{2}$$

Then

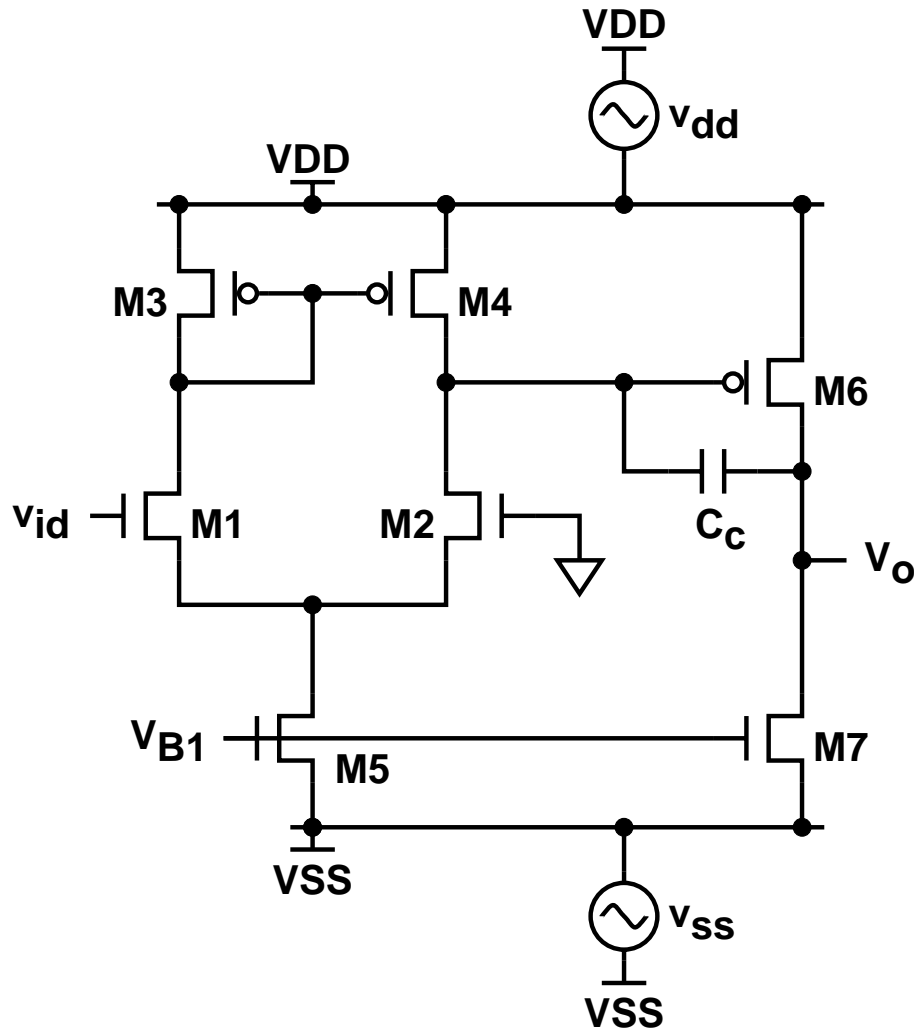
$$G_{md} \approx g_{m,1-2} \cdot \frac{1 - \left(\frac{\Delta g_{m,1-2}}{2g_{m,1-2}}\right)^2}{1 + \left(\frac{\Delta g_{m,3-4}}{2g_{m,3-4}}\right)} \quad G_{mc} \approx -\frac{g_{m,1-2}}{1 + 2g_{m,1-2}r_{o5}} \cdot (\epsilon_d + \epsilon_m)$$

where

$$\epsilon_d \approx \frac{1}{g_{m3}r_{o1}} - \frac{\Delta g_{m,1-2}}{g_{m,1-2}} \left(1 + \frac{2r_{o5}}{r_{o1}}\right) - \frac{2r_{o5}}{r_{o1}} \cdot \frac{\Delta r_{o,1-2}}{r_{o,1-2}}$$

$$\epsilon_m = \frac{1}{1 + g_{m3}r_{o3}} + \frac{(g_{m3} - g_{m4})r_{o3}}{1 + g_{m3}r_{o3}} \approx \frac{1}{g_{m3}r_{o3}} + \frac{\Delta g_{m,3-4}}{g_{m,3-4}}$$

# Power Supply Rejection Ratio (PSRR)



$$V_o = -A_v V_{id} + A_{dd} V_{dd} + A_{ss} V_{ss}$$

$$\text{PSRR}_{DD} \equiv \frac{A_v}{A_{dd}}$$

$$\text{PSRR}_{SS} \equiv \frac{A_v}{A_{ss}}$$

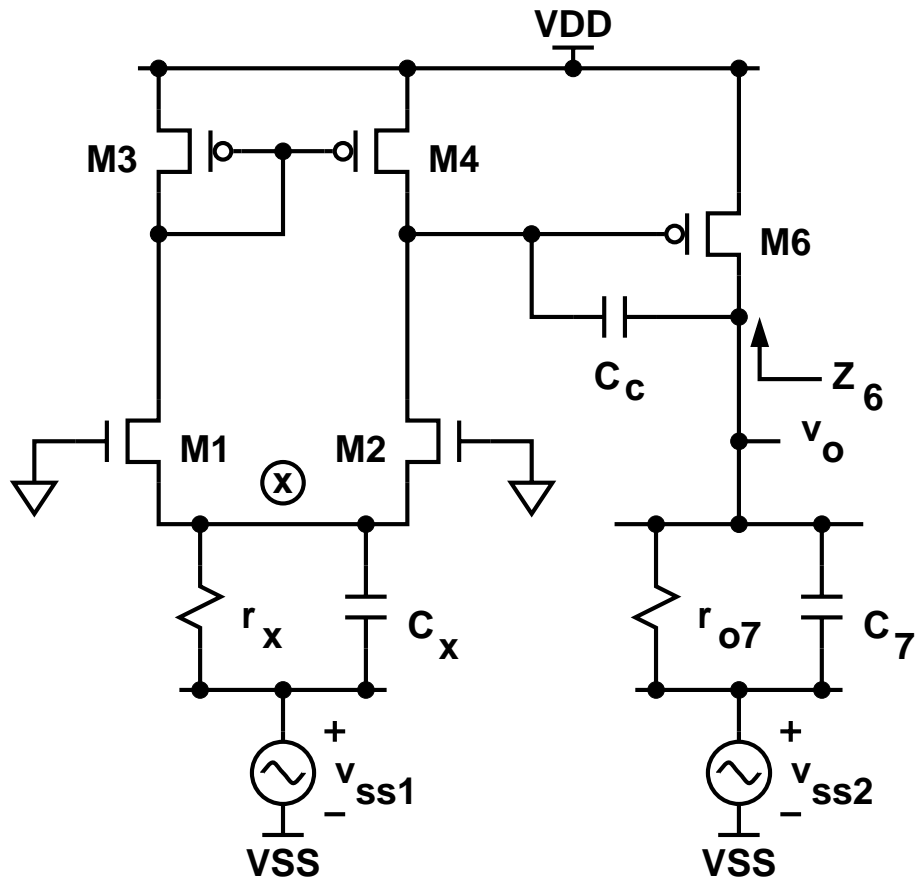
$$A_v = \frac{A_v(0)}{1 - s/p_1}$$

$$A_v(0) = g_{m1} g_{m6} R_1 R_2$$

$$A_v(0) p_1 = -\frac{g_{m1}}{C_c}$$

$$A_v \approx \frac{g_{m1}}{s C_c} \quad \text{for } \omega \gg |p_1|$$

# Power Supply Rejection Ratio (PSRR<sub>SS</sub>)



$$\frac{v_o}{v_{ss1}} = A_{v,cm} = \frac{A_v}{\text{CMRR}}$$

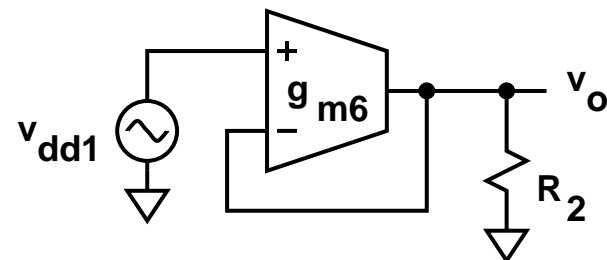
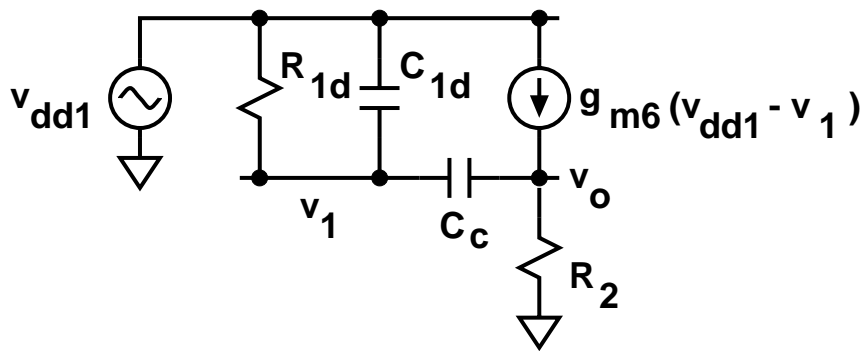
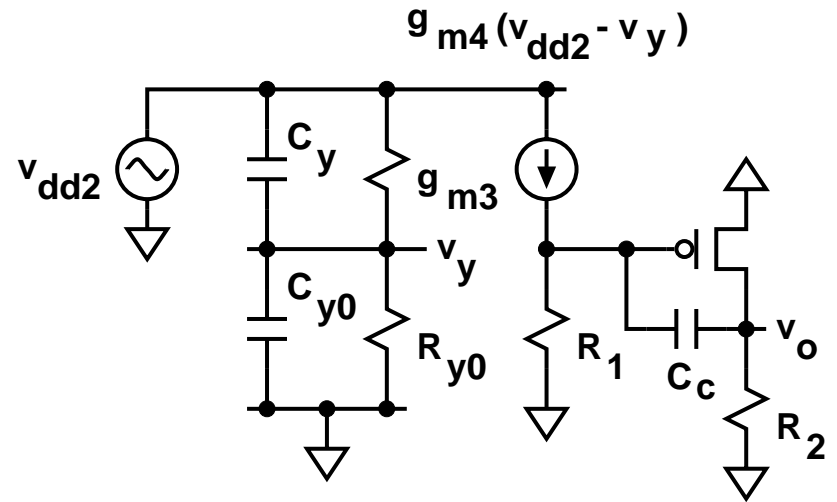
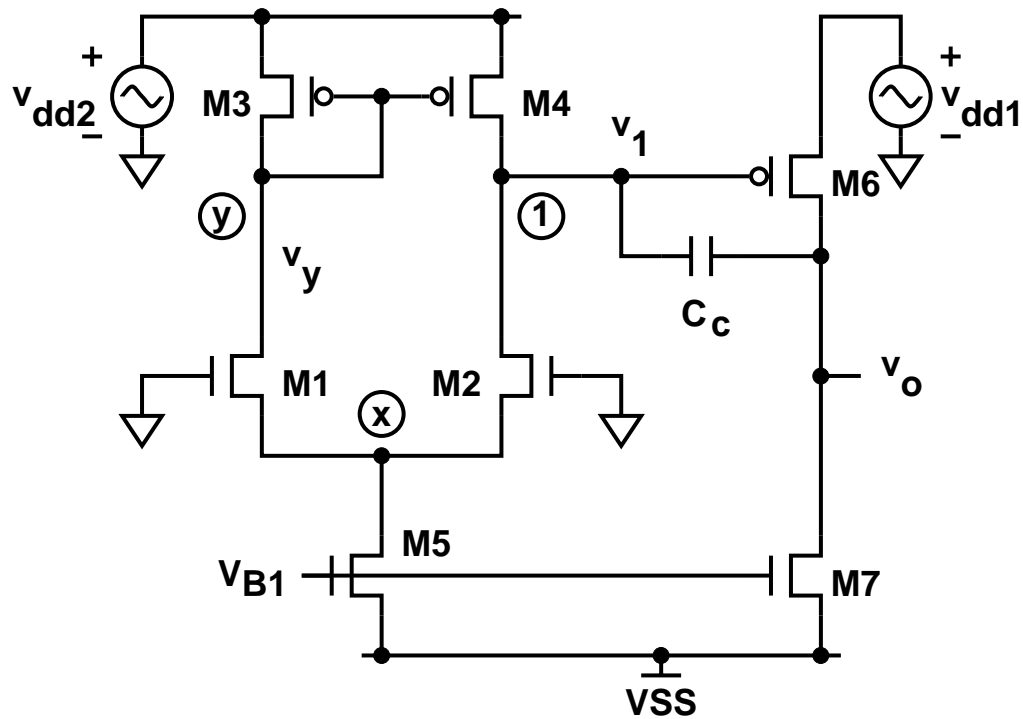
$$Z_6 \approx \frac{1}{g_{m6}}$$

$$Z_7 = \frac{1}{g_{o7} + sC_7}$$

$$\frac{v_o}{v_{ss2}} = \frac{Z_6}{Z_6 + Z_7} \approx \frac{Z_6}{Z_7} \approx \frac{g_{o7} + sC_7}{g_{m6}}$$

$$\frac{1}{\text{PSRR}_{SS}} = \frac{v_o/v_{ss1} + v_o/v_{ss2}}{A_v} = \frac{1}{\text{CMRR}} + \frac{(1 + sr_{o7}C_7)(1 - s/p_1)}{g_{m6}r_{o7}A_v(0)} \approx \frac{1}{\text{CMRR}}$$

# Power Supply Rejection Ratio (PSRR<sub>DD</sub>)



# Power Supply Rejection Ratio (PSRR<sub>DD</sub>)

---

The voltage gain from  $v_{dd1}$  to  $v_o$  is

$$\frac{V_o}{V_{dd1}} = \frac{1}{1 + \frac{1+(g_{1d}+sC_{1d})/(sC_c)}{R_2(g_{1d}+sC_{1d})+g_{m6}R_2}} \approx \frac{1}{1 + \frac{C_{1d}/C_c}{g_{m6}R_2}} \approx 1$$

For  $v_{dd2}$  input, since  $g_{m3} + sC_y \gg G_{y0} + sC_{y0}$ , the resulting current flow in M3 is approximately

$$i_{y0} \approx v_{dd2} \cdot (g_{y0} + sC_{y0})$$

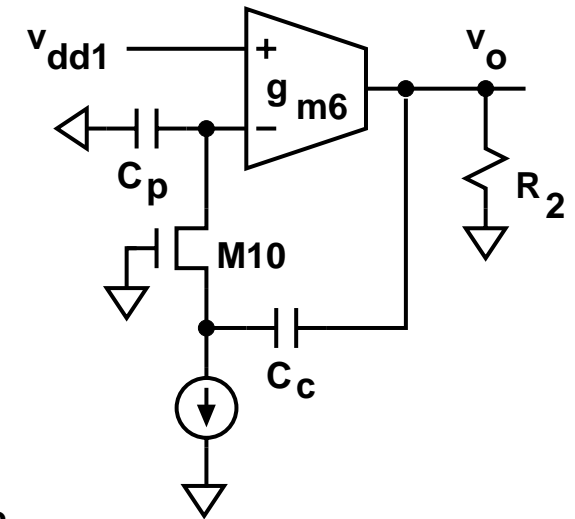
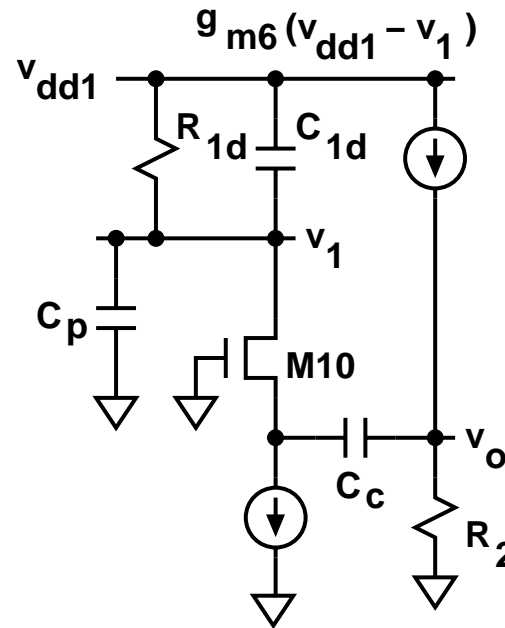
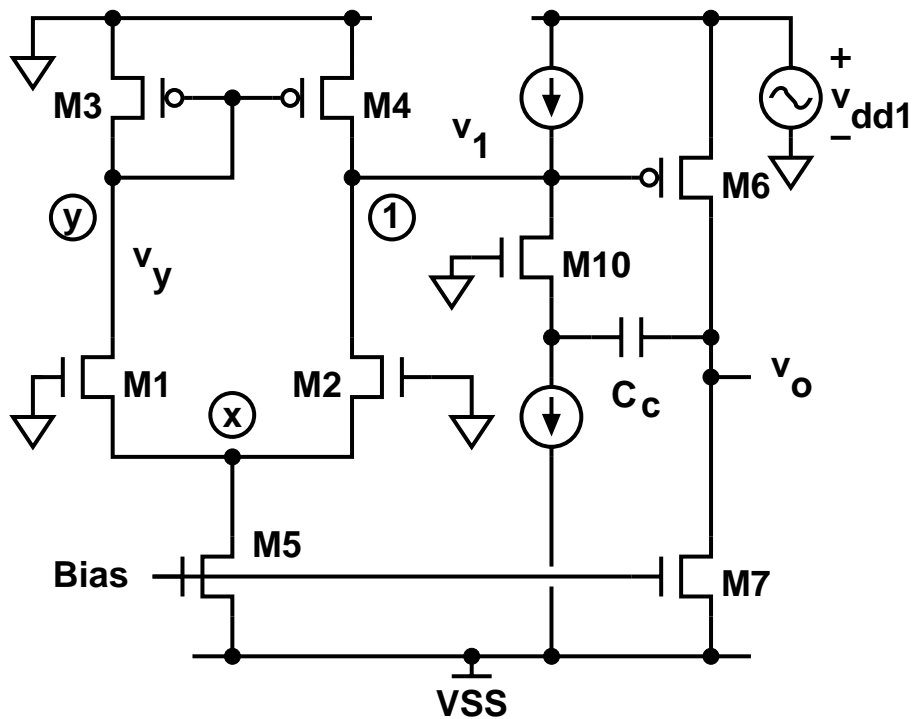
The current is mirrored in M4, and amplified by M6 and  $C_c$ . The voltage gain is

$$\frac{V_o}{V_{dd2}} = i_{y0} \cdot A_{v2} \approx -\frac{g_{y0} + sC_{y0}}{sC_c} \Rightarrow \frac{V_o}{V_{dd2}} \ll \frac{V_o}{V_{dd1}}$$

Thus

$$\text{PSRR}_{DD} \approx \frac{A_v}{V_o/V_{dd1}} \approx A_v$$

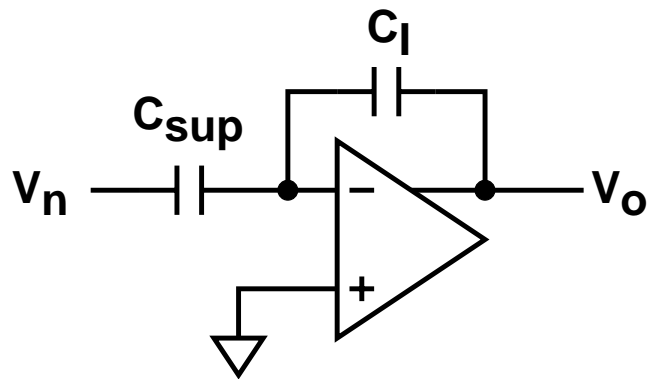
# PSRR<sub>DD</sub> with Common-Gate Miller Compensation



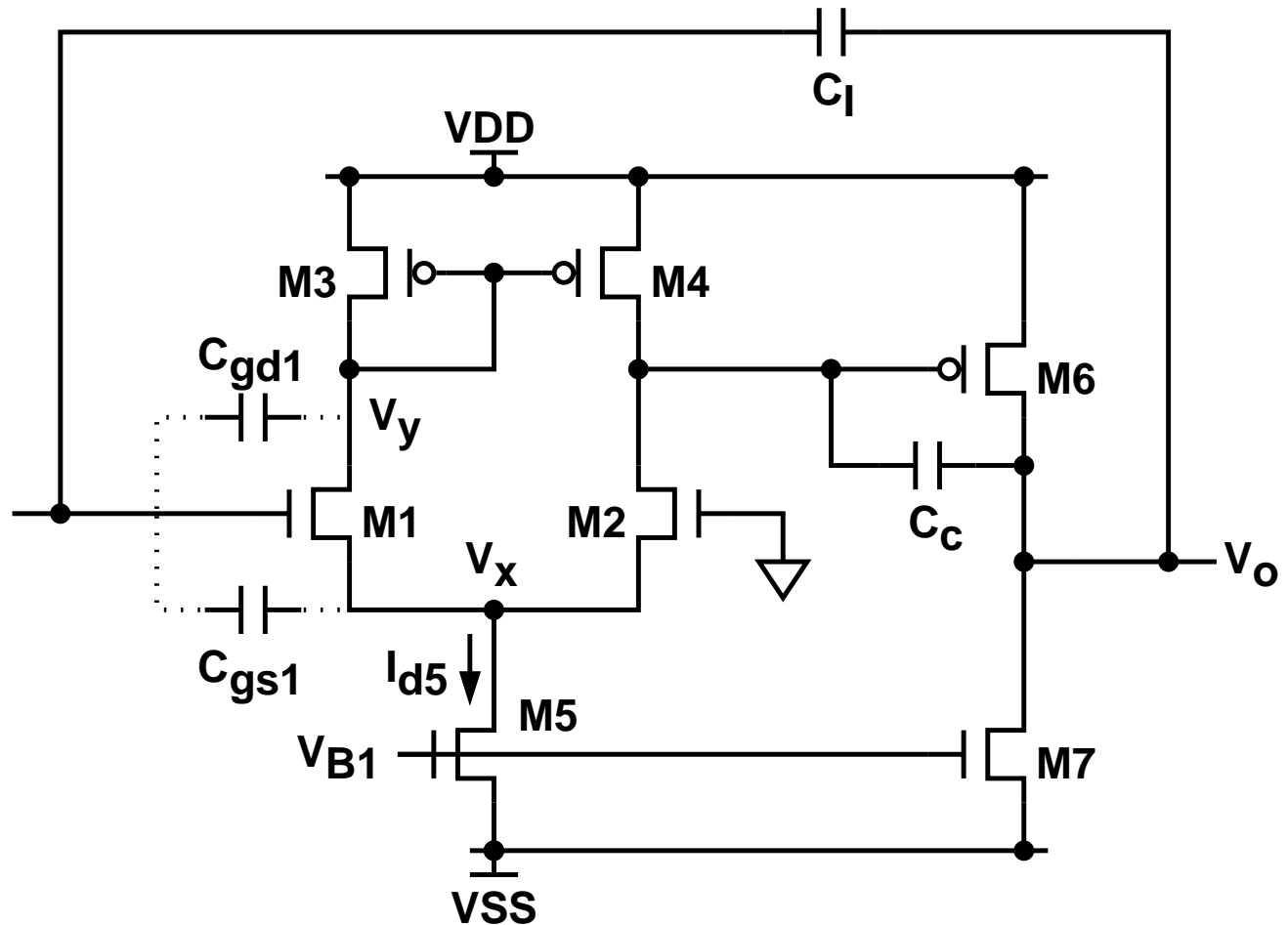
Assume the M10 stage has  $R_{in} = 1/g_{m10}$  and  $A_I = 1$ . Neglecting  $R_{1d}$  and  $C_{1d}$ , we have

$$\frac{V_o}{V_{dd1}} = \frac{1}{\frac{1}{1+sC_c/g_{m10}} \cdot \left( \frac{C_c}{C_p} + \frac{sC_c}{g_{m6}} \right) + \frac{1}{g_{m6}R_2}} \approx \frac{C_p}{C_c} \cdot \left( 1 + s \frac{C_c}{g_{m10}} \right)$$

# Supply Capacitance



$$V_o = -\frac{C_{sup}}{C_f} \cdot V_n$$



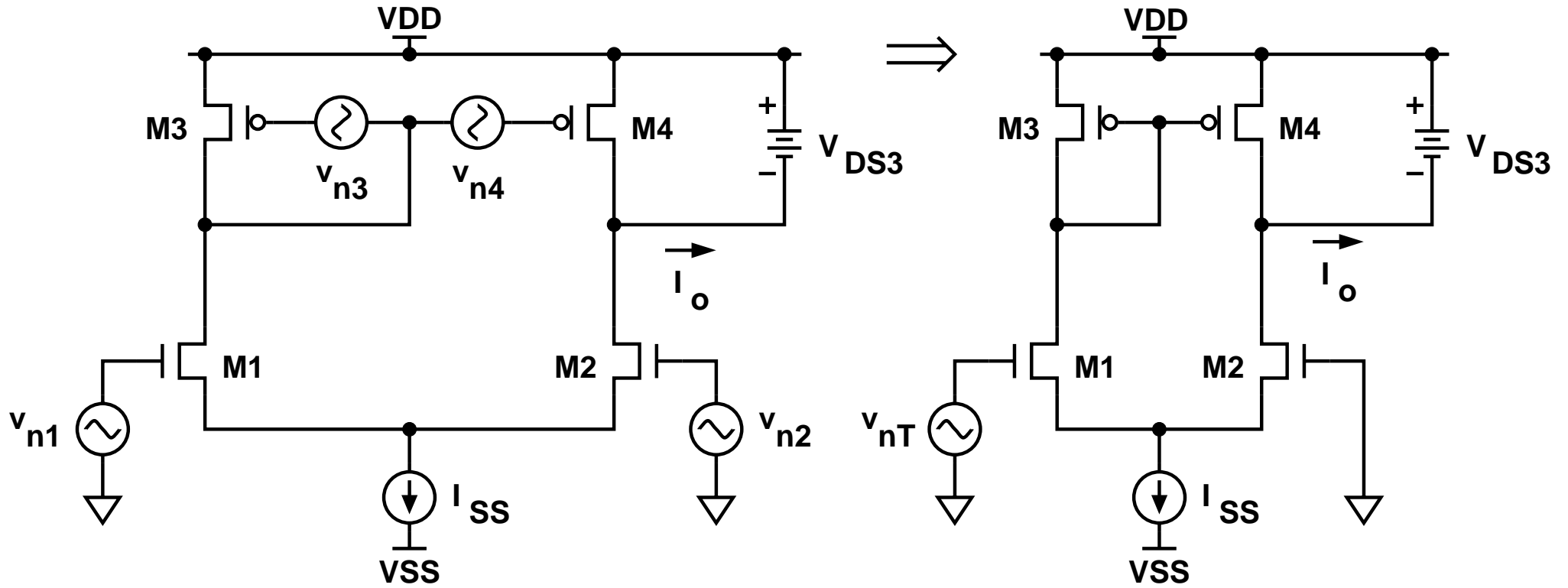
- Both  $C_{gs1}$  and  $C_{gd1}$  can function as  $C_{sup}$ , and noises at  $V_x$  and  $V_y$  can leak to the output.

# Power-Supply Rejection and Supply Capacitance

---

- The  $V_{DD}$  noise can be coupled to  $V_y$  through the diode-connected M3 device. The use of cascode input stage can overcome this problem.
- If  $i_{d5}$  is modulated by the supply voltage variation, then  $v_x \approx i_{d5}/(2g_{m1})$ . The use of supply-independent bias reference can overcome this problem.
- The noises at the substrate/well terminals of M1 and M2 can change the  $V_t$  of the devices due to body effect, and cause  $V_{gs}$  variation, introducing noises at  $V_x$ . A solution is to place both M1 and M2 in a single well, and connect well and source terminals together to eliminate body effect.
- Interconnect crossovers can introduce undesired coupling capacitors to the  $V_{i-}$  summing node. Careful layout is required.
- Fully-differential circuit topology generally has better power-supply rejection performance.

# Device Noise Analysis



$$\overline{v_n^2} \approx 4kT \left( \frac{2}{3} \cdot \frac{1}{g_m} \right) + \frac{K_f}{WLC_{ox}} \cdot \frac{1}{f} \quad \overline{i_n^2} \approx 0$$

$$\overline{v_{nT}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2} + \left( \frac{g_{m3}}{g_{m1}} \right)^2 \left( \overline{v_{n3}^2} + \overline{v_{n4}^2} \right)$$

# Thermal Noise Performance

---

Assuming  $M1=M2$  and  $M3=M4$ , and knowing  $I_{D1} = I_{D3}$  so that

$$\left(\frac{g_{m3}}{g_{m1}}\right)^2 = \frac{\mu_p C_{ox}(W/L)_3}{\mu_n C_{ox}(W/L)_1} = \frac{\mu_p (W/L)_3}{\mu_n (W/L)_1} \quad k'_n = \mu_n C_{ox} \quad k'_p = \mu_p C_{ox}$$

The input referred thermal noise is

$$\begin{aligned} \overline{v_{(\theta)T}^2} \\ \Delta f &= 4kT \left(\frac{4}{3} \frac{1}{g_{m1}}\right) + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \times 4kT \left(\frac{4}{3} \frac{1}{g_{m3}}\right) = 4kT \left(\frac{4}{3} \frac{1}{g_{m1}}\right) \times \left[1 + \frac{g_{m3}}{g_{m1}}\right] \\ &= 4kT \left(\frac{4}{3} \cdot \frac{1}{\sqrt{2k'_n(W/L)_1 I_{D1}}}\right) \times \left[1 + \sqrt{\frac{\mu_p}{\mu_n} \cdot \frac{(W/L)_3}{(W/L)_1}}\right] \end{aligned}$$

- The load contribution can be made small by making  $g_{m1} > g_{m3}$  or  $(W/L)_1 > (W/L)_3$ .
- $g_{m1}$  should be made as large as possible to minimize thermal noise contribution.

# Flicker Noise Performance

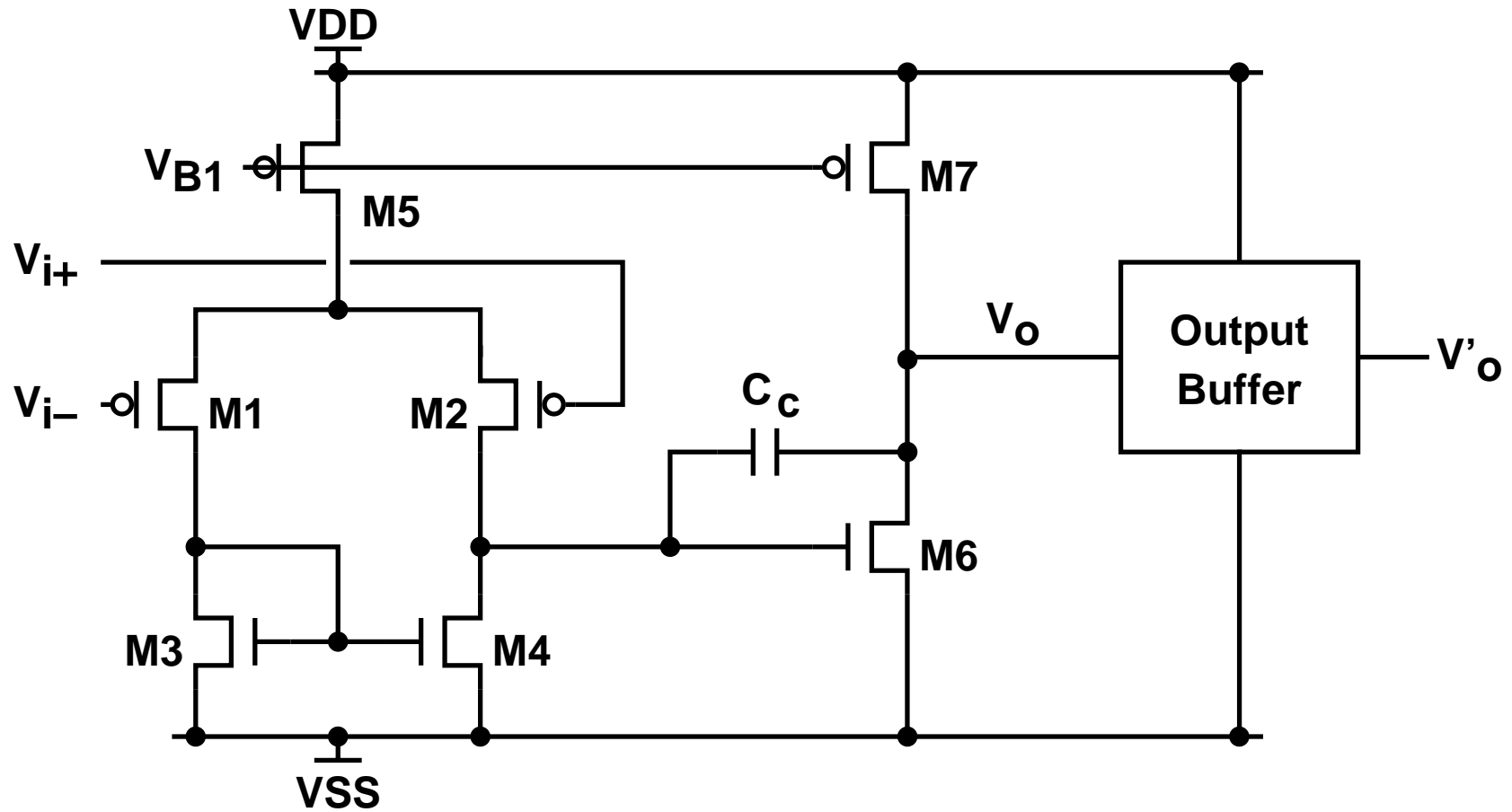
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The input referred  $1/f$  noise is

$$\begin{aligned}\frac{\overline{v^2}_{(1/f)T}}{\Delta f} &= \frac{2K_{fn}}{W_1 L_1 C_{ox} f} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \times \frac{2K_{fp}}{W_3 L_3 C_{ox} f} = \frac{2K_{fn}}{W_1 L_1 C_{ox} f} + \frac{\mu_p (W/L)_3}{\mu_n (W/L)_1} \times \frac{2K_{fp}}{W_3 L_3 C_{ox} f} \\ &= \frac{1}{f} \times \frac{2K_{fn}}{W_1 L_1 C_{ox}} \left(1 + \frac{K_{fp}}{K_{fn}} \cdot \frac{\mu_p}{\mu_n} \cdot \frac{L_1^2}{L_3^2}\right)\end{aligned}$$

- $K_{fp}$  is typically smaller than  $K_{fn}$  by a factor of two or more.
- The load contribution can be made small by making  $L_3 > L_1$ . But longer  $L_3$  can limit the signal swing somewhat.
- The width of load devices does not affect the  $1/f$  noise performance. But making it wider can maximize signal swing.
- Making  $W_1$  wider can reduce  $1/f$  noise.

## 2-Stage Opamp with pMOST Input Stage



## 2-Stage Opamp with pMOST Input Stage

---

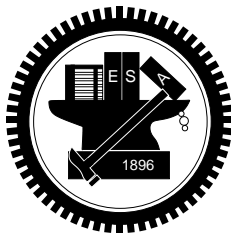
Comparing to the nMOST-input opamps, the pMOST-input opamps have

- Similar dc voltage gain.
- Smaller  $g_{m1}$  and larger  $g_{m6}$ .
- Larger unity-gain frequency since  $\omega_u \simeq |p_2|$  and  $|p_2| = g_{m6}/C_2$ .
- Better slew rate since both  $V_{ov1}$  and  $\omega_u$  are larger.
- Better 1/f noise performance.
- Poorer thermal noise performance.

# Operational Amplifiers with Single-Ended Outputs

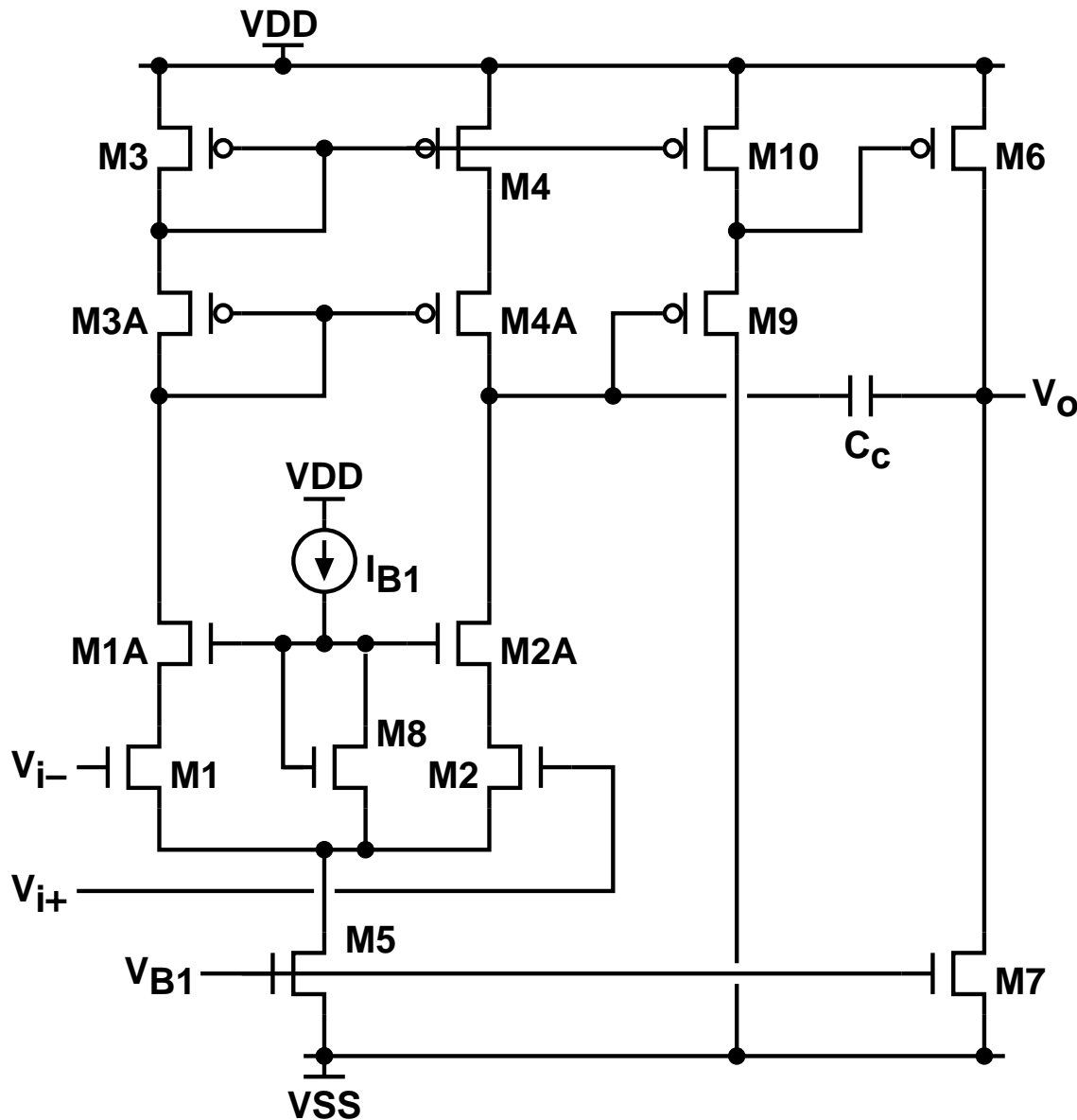
Jieh-Tsorng Wu

December 23, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Two-Stage Operational Amplifier with Cascode



- The voltage gain  $A_v \propto (g_m r_o)^3$ .

- Size M8 so that

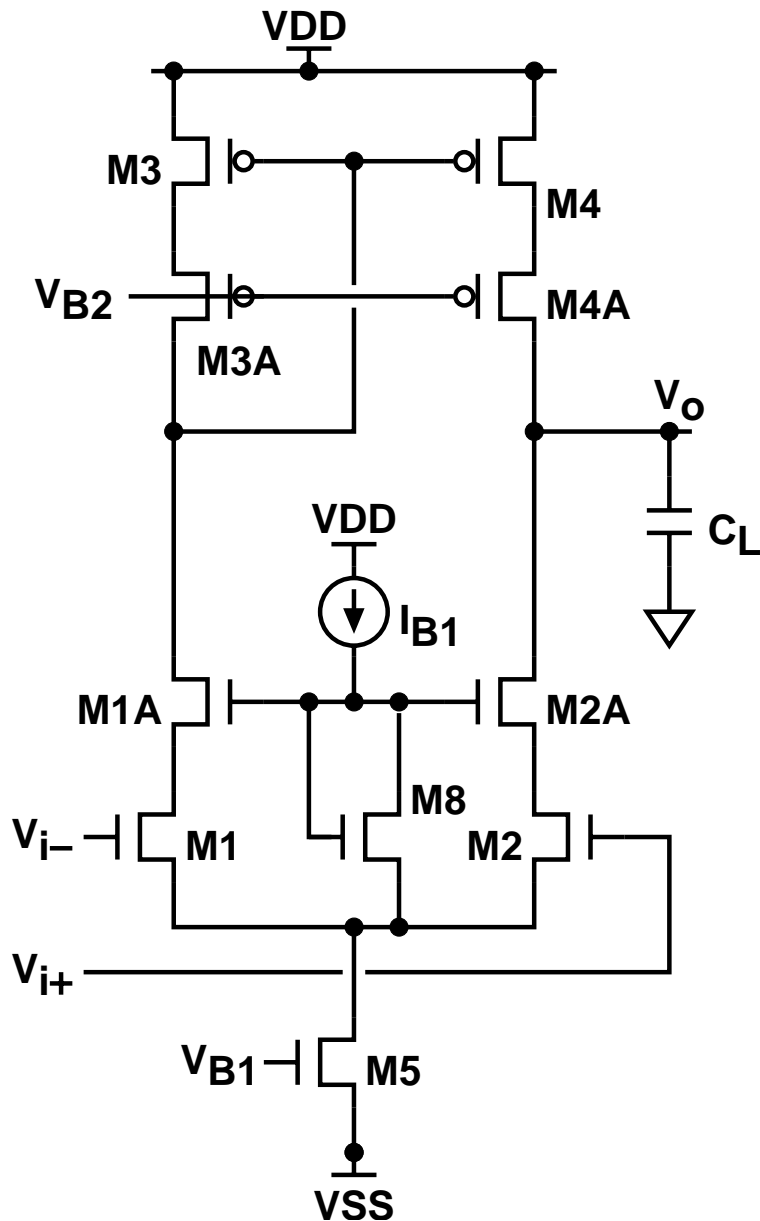
$$V_{DS1} = V_{DS2} \approx V_{DSAT}$$

- Input common-mode range is reduced by cascodes.

- The additional poles are non-dominant and located near  $\omega_T$ .

- The 2nd stage can also use cascodes.

# Telescopic-Cascode Operational Amplifier



- The voltage gain  $A_v \propto (g_m r_o)^2$ .
- Consider the output current branch,

$$V_{DD} - (V_{IC} - V_t) > \Delta V_o + 3V_{ov}$$

$$\Rightarrow V_{DD} - V_{IC} > \Delta V_o + 3V_{ov} - V_t$$

Since  $V_{IC,min} = V_t + 2V_{ov} + V_{SS}$ , we have

$$V_{DD} - V_{SS} > \Delta V_o + 5V_{ov}$$

- Consider the non-output branch,

$$V_{DD} - (V_{IC} - V_t) > V_t + 2V_{ov}$$

$$\Rightarrow V_{DD} - V_{IC} > 2V_{ov} \quad \text{or} \quad V_{DD} - V_{SS} > V_t + 4V_{ov}$$



# Folded-Cascode Operational Amplifier

---

- Consider output stage

$$V_{DD} - V_{SS} > \Delta V_o + 4V_{ov} \quad \text{or} \quad V_{DD} - V_{SS} > V_t + 3V_{ov}$$

Consider input stage

$$V_{IC,max} = V_{DD} - V_{ov} + V_t \quad V_{IC,min} = V_{SS} + V_t + V_{ov} + V_{o,min}(I_1)$$

- The differential-mode voltage gain is

$$A_v = \frac{A_v(0)}{1 - s/p_1} \quad A_v(0) = g_{m1}R_o \quad p_1 = -\frac{1}{R_o C_L} \quad R_o = \frac{1}{\frac{g_{o2}+g_{o9}}{g_{m3}r_{o3}} + \frac{g_{o7}}{g_{m5}r_{o5}}}$$

At midband frequencies where  $\omega \gg |p_1|$

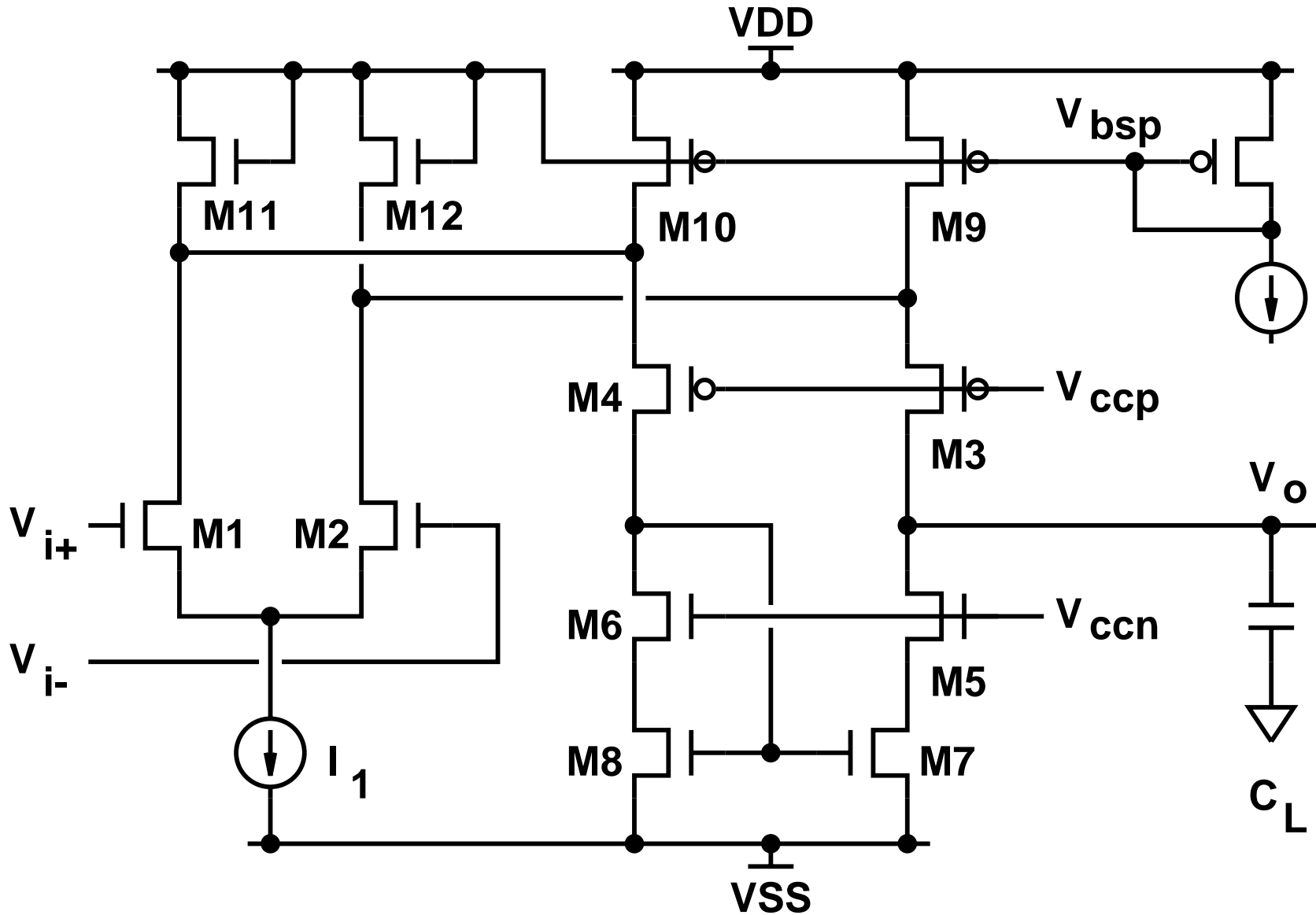
$$A_v \approx \frac{A_v(0)}{-s/p_1} = \frac{g_{m1}}{sC_L} = \frac{\omega_u}{s} \quad \omega_u = \frac{g_{m1}}{C_L}$$

# Folded-Cascode Operational Amplifier

---

- The dominant pole is associated with the only high-impedance node at  $V_o$ . All other poles are located near  $\omega_T$ , and their magnitude are normally larger than  $|p_2|$  of the two-stage opamps.
- $C_L$  provides the dominant-pole frequency compensation. Increasing  $C_L$  *improves* the phase margin.
- If lead compensation is desired, a resistor can be placed in series with  $C_L$ .
- Use nMOST input stage for larger  $g_{m1}$  and better thermal noise performance.
- Good PSRR since no pole-splitting  $C_c$ .
- Slightly higher noise due to more devices.
- Suitable for low-voltage operation.
- Active cascodes can be used to increase voltage gain.

# Folded-Cascode Operational Amplifier



# Folded-Cascode Operational Amplifier

---

If bias currents  $I_{D1,D2} > I_{D3,D4}$ , i.e.,  $I_1 > I_{D9,D10}$ ,

- Without M11 and M12, the slew rate is

$$SR = \frac{I_{D9}}{C_L} = \frac{I_{D10}}{C_L}$$

- During slew condition, M11 and M12 can be used to clamp the drain voltage of M1 and M2 to reduce bias recovery time, and increase  $I_{D9}$  and  $I_{D10}$  to improve SR.

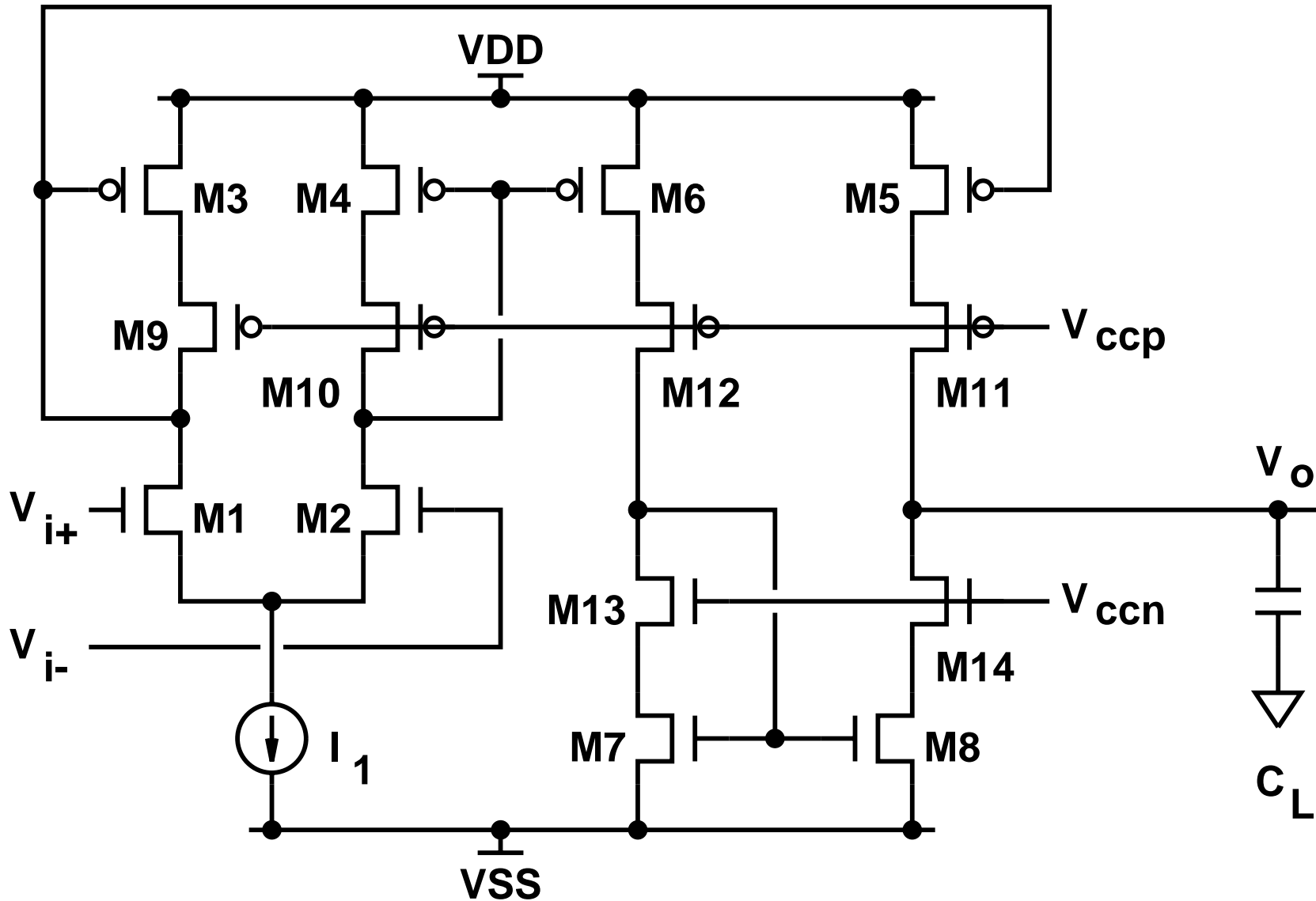
If bias currents  $I_{D1,D2} < I_{D3,D4}$ , i.e.,  $I_1 < I_{D9,D10}$ ,

- This slew rate is

$$SR = \frac{I_1}{C_L} \quad I_1 = I_{D1} + I_{D2}$$

- M11 and M12 are not required.

# Current-Mirror Operational Amplifier



# Current-Mirror Operational Amplifier

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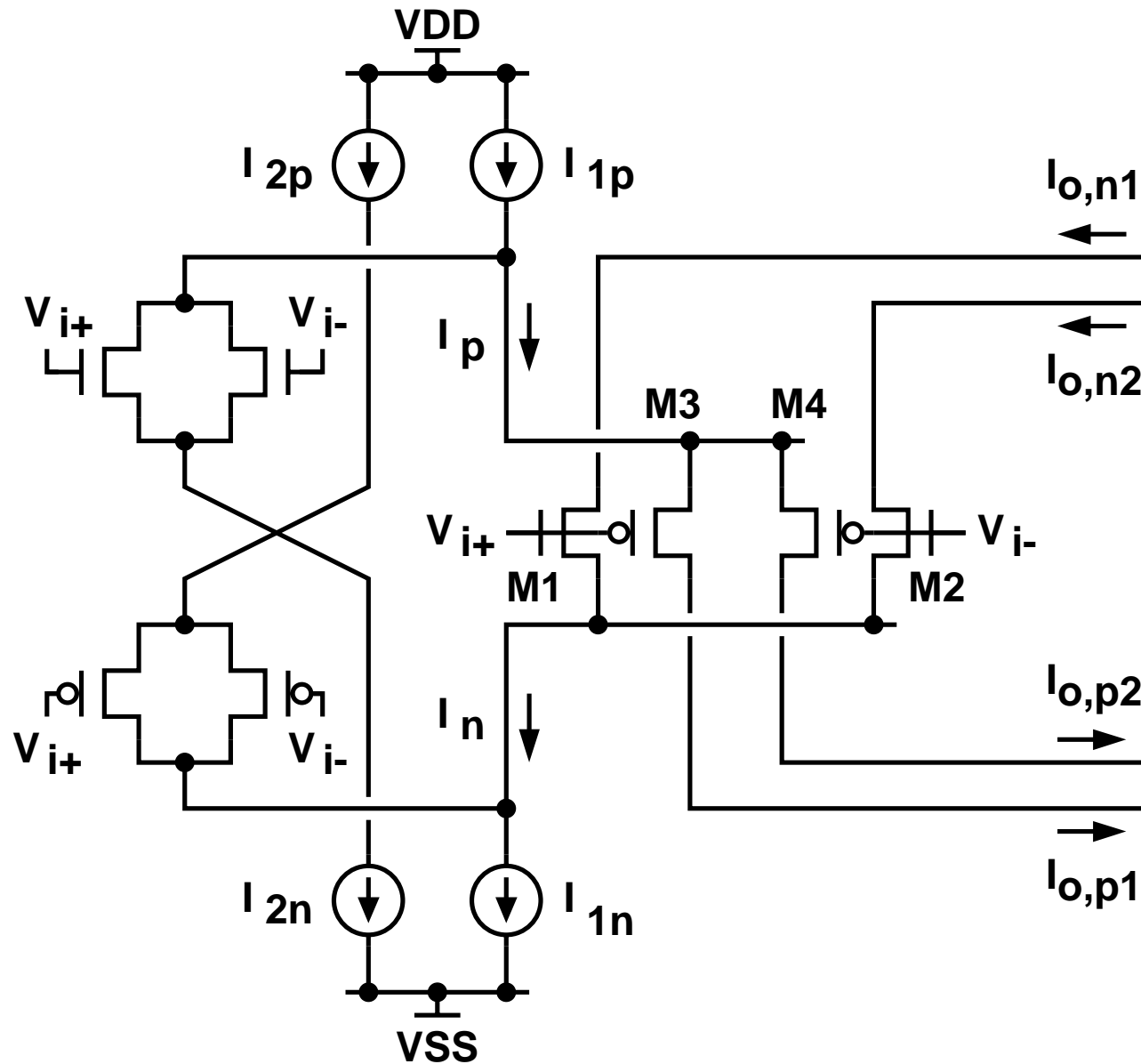
$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_6 = \frac{1}{K} \left(\frac{W}{L}\right)_5 \quad \left(\frac{W}{L}\right)_7 = \frac{1}{K} \left(\frac{W}{L}\right)_8$$

$$I_{D1,D2} = I_{D3,D4} = I_{D6} = I_{D7} = \frac{1}{K} I_{D5} = \frac{1}{K} I_{D8} = \frac{1}{2} I_1 \quad \text{SR} = \frac{K I_1}{C_L}$$

$$A_v(0) = K g_{m1} R_o \quad R_o = \frac{1}{\frac{g_{o5}}{g_{m11} r_{o11}} + \frac{g_{o8}}{g_{m14} r_{o14}}} \quad p_1 = -\frac{1}{R_o C_L} \quad \omega_u = \frac{K g_{m1}}{C_L}$$

- For a given power dissipation, the current-mirror opamps have larger bandwidth and SR than the folded-cascode opamps. But they also suffer from larger thermal noise.
- For small  $C_L$ ,  $K$  may have to be reduced to prevent the nondominant poles from degrading the phase margin.
- A practical upper limit on  $K$  is around 5. For a general-purpose opamp,  $K \simeq 2$ .

# Rail-to-Rail Complementary Input Stage



# Rail-to-Rail Complementary Input Stage

---

- Total input stage transconductance is

$$G_m = g_{m1} + g_{m3}$$

- $G_m$  variation due to  $V_{ic}$  change can degrade CMRR. Want

$$g_{m1} + g_{m3} = \sqrt{\mu_n C_{ox} (W/L)_1 I_n} + \sqrt{\mu_p C_{ox} (W/L)_3 I_p} = \text{Constant}$$

If  $\mu_n C_{ox} (W/L)_1 = \mu_p C_{ox} (W/L)_3$ , want

$$\sqrt{I_n} + \sqrt{I_p} = \sqrt{I_{1n} - I_{2p}} + \sqrt{I_{1p} - I_{2n}} = \text{Constant}$$

# Rail-to-Rail Complementary Input Stage

---

- Let

$$I_{1n} = I_{1p} = 4I \quad I_{2n} = I_{2p} = 3I$$

At  $V_{ic} \simeq (V_{DD} - V_{SS})/2$

$$\sqrt{I_n} + \sqrt{I_p} = \sqrt{1I} + \sqrt{1I} = 2\sqrt{I}$$

At  $V_{ic} \simeq V_{SS}$ ,  $I_n = 0$  and  $I_{2n} = 0$ ,

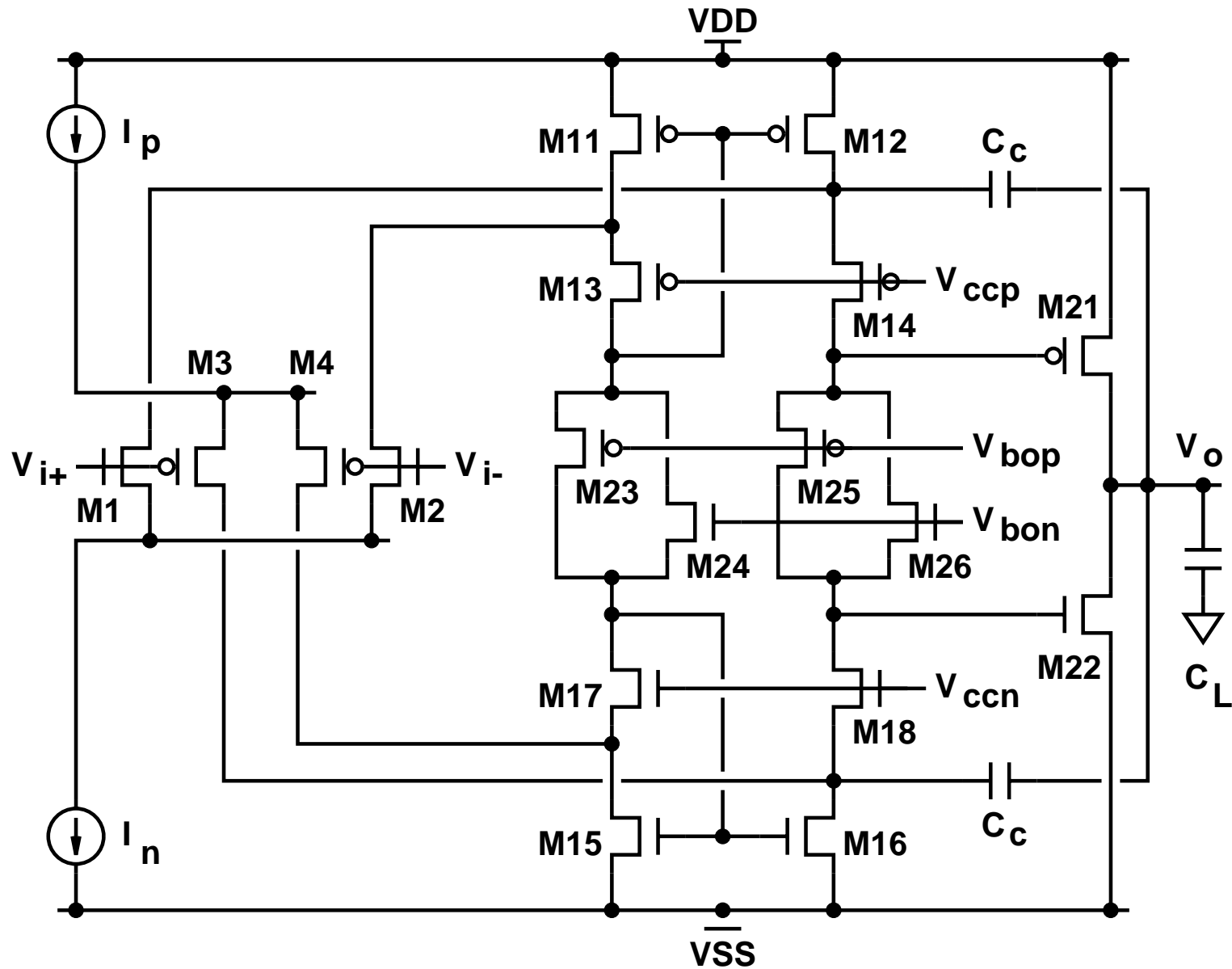
$$\sqrt{I_n} + \sqrt{I_p} = \sqrt{0I} + \sqrt{4I} = 2\sqrt{I}$$

At  $V_{ic} \simeq V_{DD}$ ,  $I_p = 0$  and  $I_{2p} = 0$ ,

$$\sqrt{I_n} + \sqrt{I_p} = \sqrt{4I} + \sqrt{0I} = 2\sqrt{I}$$

- Less than 5% change in  $G_m$  is possible.
- The variation of the input-referred dc offset  $V_{OS}$  due to  $V_{ic}$  change also degrades CMRR.

# A Rail-to-Rail Input/Output Opamp



# A Rail-to-Rail Input/Output Opamp

---

- Two cascaded gain stages.
- Noises in  $V_{bop}$  and  $V_{bon}$  are canceled at output.
- The bias of the output stage is insensitive to variations in  $I_p$ ,  $I_n$  and supply voltage.
- The two  $C_c$  are connected as Miller frequency compensation using common-gate stages.

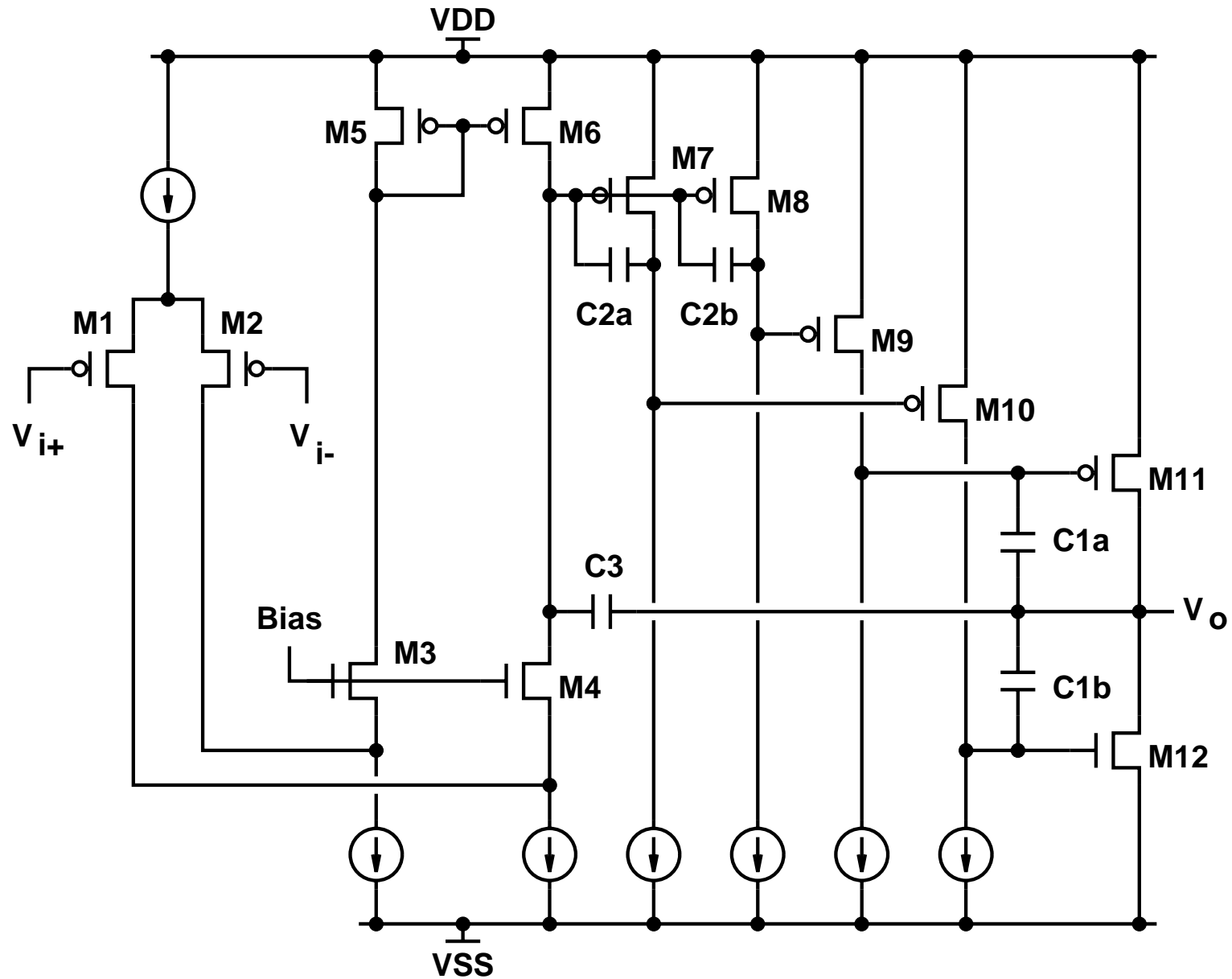
- The output pole is

$$p_2 = \frac{C_c}{C_{gso}} \times \frac{g_{mo}}{C_L}$$

where  $g_{mo}$  and  $C_{gso}$  are respectively the total  $g_m$  and  $C_{gs}$  of the output stage.

- Reference: Hogervorst, et al., JSSC 12/94, pp. 1505–1513.

# Low-Voltage Multi-Stage Opamp

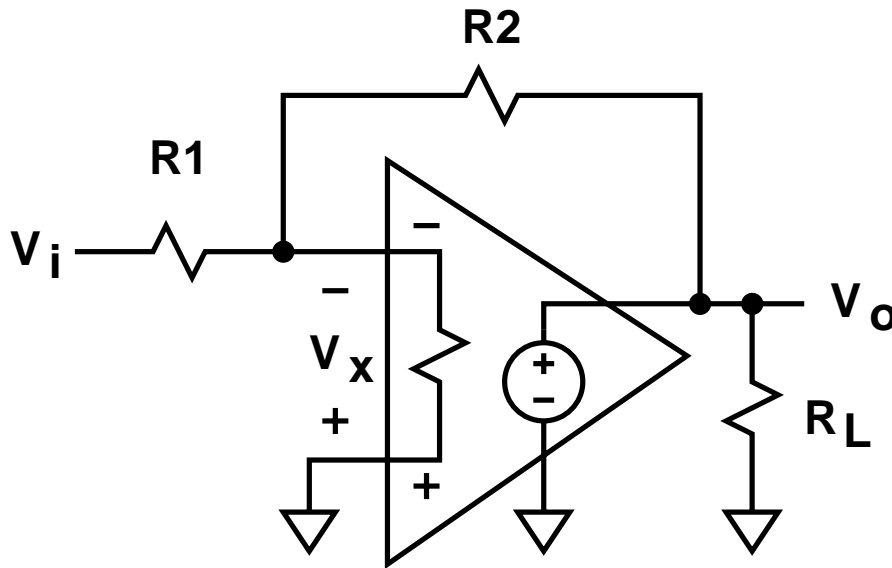


# Low-Voltage Multi-Stage Opamp

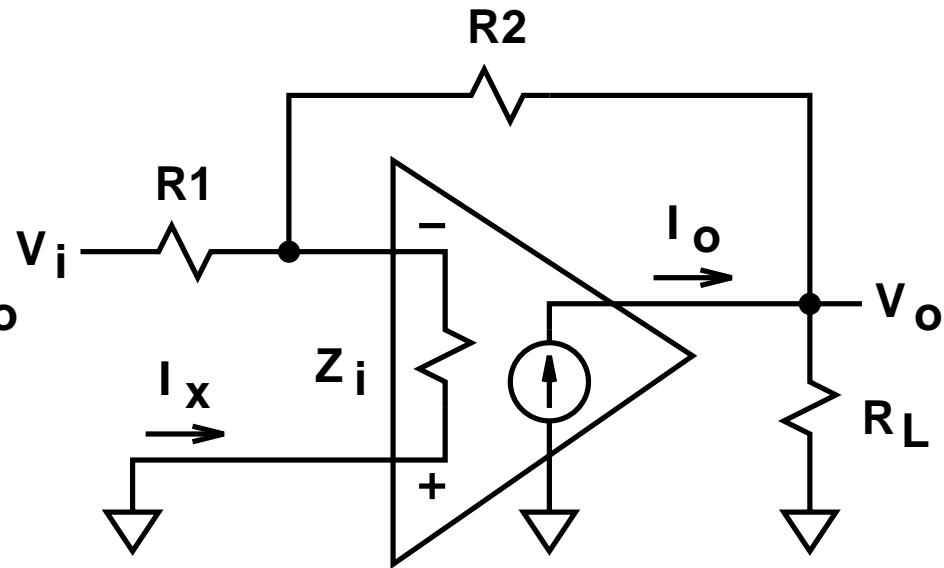
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- Four cascaded gain stages.
- Hybrid nested Miller compensation.
- Class-AB output stage.
- A supply voltage below 1.5 V is possible.
- Reference: Eschauzier, et al., JSSC 12/94, pp. 1497–1504.

# Current-Feedback Configuration



**Voltage-Feedback Opamp**



**Current-Feedback Opamp**

For the voltage-feedback opamp, let  $V_o/V_x = A \approx \omega_u/s$  and  $Z_i \rightarrow \infty$ , then

$$A_v = \frac{V_o}{V_i} = -\frac{R_2}{R_1} \cdot \frac{1}{1 + \frac{1}{A} \left(1 + \frac{R_2}{R_1}\right)} \approx -\frac{R_2}{R_1} \cdot \frac{1}{1 + \frac{s}{\omega_u} \left(1 + \frac{R_2}{R_1}\right)}$$

- Trade-off between closed-loop gain and closed-loop bandwidth.

# Current-Feedback Configuration

---

For the current-feedback opamp, let  $I_o/I_x = A \approx \omega_u/s$ , then

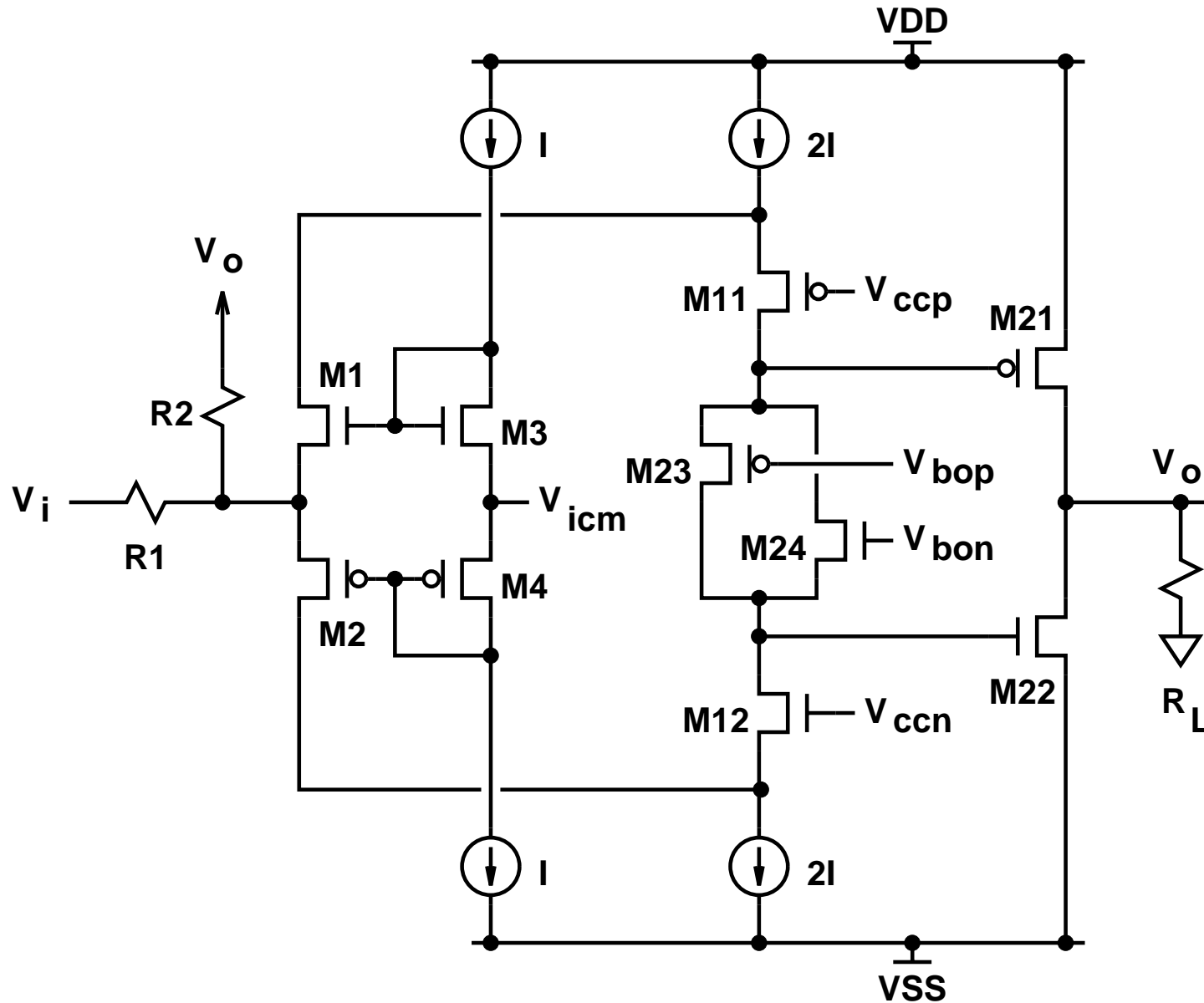
$$A_v = \frac{V_o}{V_i} = -\frac{R_2}{R_1} \cdot \frac{1 - \frac{Z_i}{AR_2}}{1 + \frac{1}{A} \left[ 1 + \frac{R_1 R_2 + Z_i (R_1 + R_2 + R_L)}{R_1 R_L} \right]} \approx -\frac{R_2}{R_1} \cdot \frac{1}{1 + \frac{s}{\omega_u} \left[ 1 + \frac{R_2 + Z_i \left( 1 + \frac{R_2 + R_L}{R_1} \right)}{R_L} \right]}$$

If  $Z_i \rightarrow 0$ ,

$$A_v \approx -\frac{R_2}{R_1} \cdot \frac{1}{1 + \frac{s}{\omega_u} \left( \frac{R_2}{R_L} \right)}$$

- The closed-loop gain can be modified by changing  $R_1$ , leaving the closed-loop bandwidth unchanged.
- For a given  $R_2$ , frequency compensation can be optimized. Suitable for high-frequency applications.

# A CMOS Current-Feedback Driver



# A CMOS Current-Feedback Driver

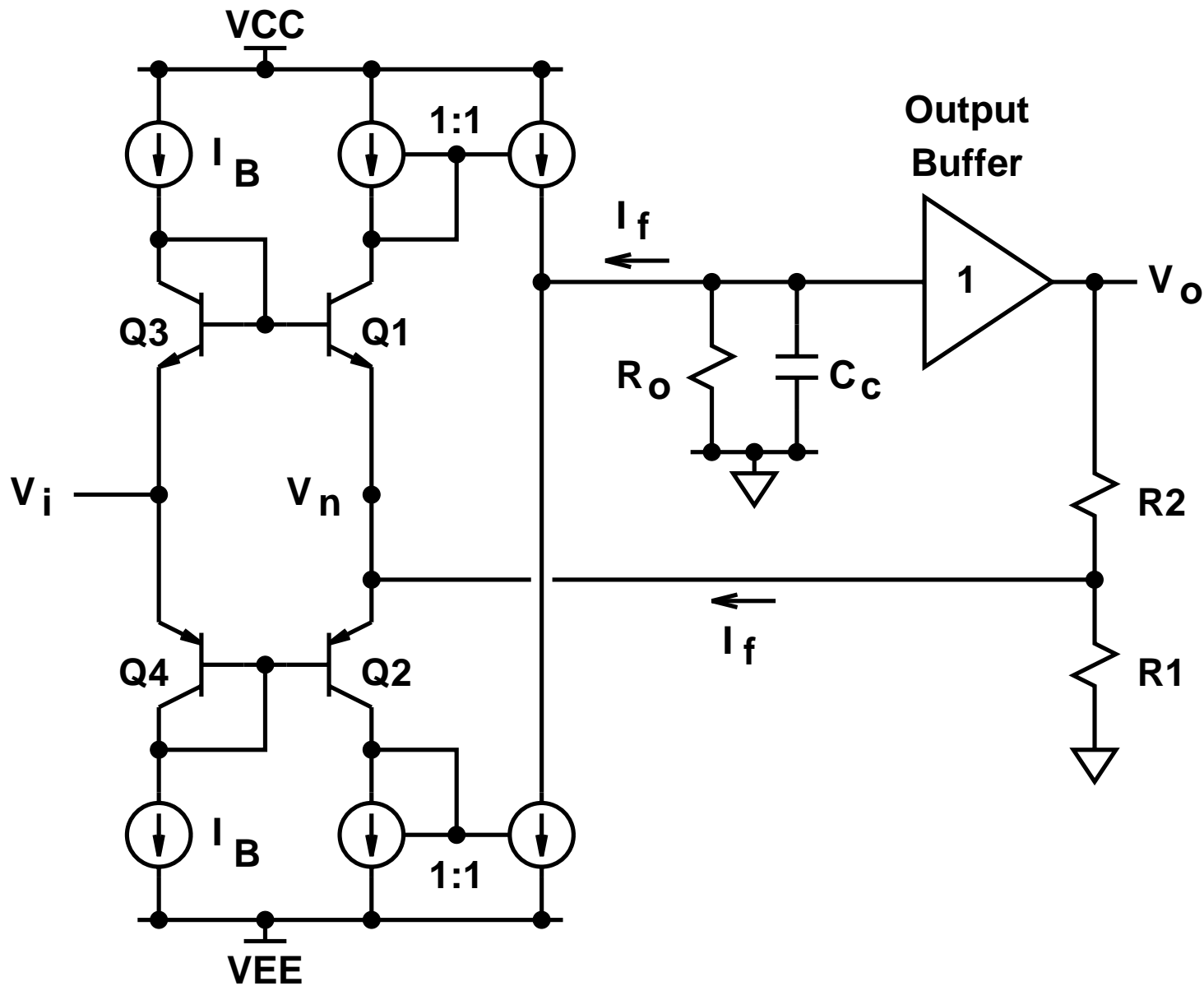
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- This opamp has been designed to drive  $R_L = 25 \Omega$  and provide 50 mA of output current.
- Two-stage opamp with only one high-impedance node.
- $C_{gs}$  and  $C_{gd}$  of M21 and M22 are large enough to provide adequate frequency compensation.
- The class-AB common-gate input stage provides large internal slew rate.
- Large voltage swing of  $V_{gs21}$  and  $V_{gs22}$  are required.
- Open-loop current gain is determined by the output stage,

$$A(s) \approx \frac{g_{mo}}{sC_{go}} = \frac{\omega_u}{s} \quad \omega_u = \frac{g_{mo}}{C_{go}}$$

- Loop gain  $T(s) \approx A(s)R_L / (R_L + R_2)$  is independent of  $R_1$ .

# A General-Purpose BJT Current-Feedback Opamps



# A General-Purpose BJT Current-Feedback Opamps

---

Due to the symmetry of the input stage, we have  $V_i = V_n$ .

If  $R_1 \parallel R_2 \gg 1/(g_{m1} + g_{m2})$ , we have

$$I_f = \frac{V_o - V_n}{R_2} - \frac{V_n}{R_1} = V_o \left( \frac{1}{R_2} \right) - V_i \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \quad V_o = -I_f \left( \frac{1}{sC_c + 1/R_o} \right)$$

$$A_v = \frac{V_o}{V_i} = \left[ \frac{R_o(R_1 + R_2)}{(R_o + R_2)R_1} \right] \left[ \frac{1}{1 + sC_c(R_o \parallel R_2)} \right]$$

If  $R_o \gg R_2$ ,

$$A_v \approx \left( 1 + \frac{R_2}{R_1} \right) \left( \frac{1}{1 + sC_c R_2} \right)$$

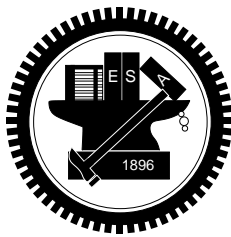
Also the loop gain is

$$T(s) = \left( \frac{1}{sC_c + 1/R_o} \right) \left( \frac{1}{R_2} \right) \approx \frac{1}{sC_c R_2}$$

# Fully Differential Operational Amplifiers

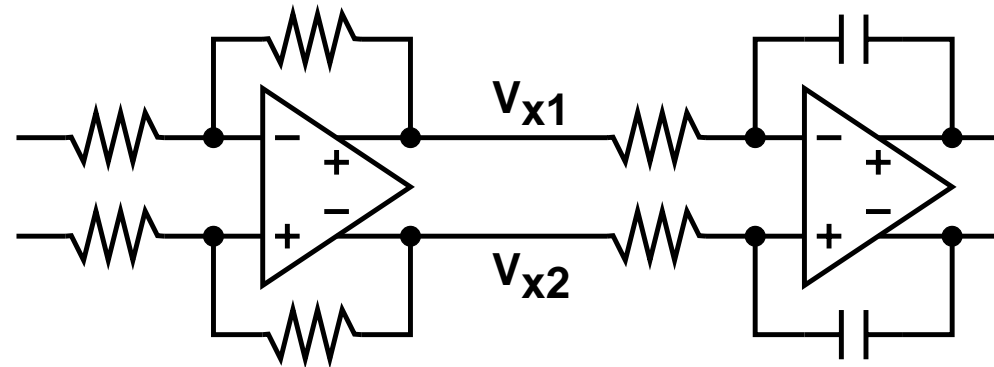
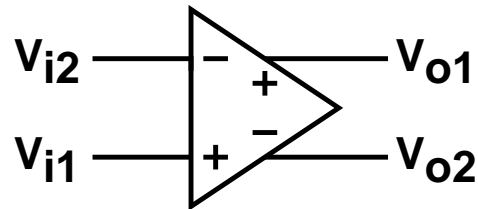
Jieh-Tsorng Wu

July 16, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Fully Balanced Circuit Topology



$$\begin{bmatrix} V_{od} \\ V_{oc} \end{bmatrix} = \begin{bmatrix} A_{dm} & A_{cdm} \\ A_{dcm} & A_{cm} \end{bmatrix} \begin{bmatrix} V_{id} \\ V_{ic} \end{bmatrix}$$

$$\begin{aligned} V_{id} &= V_{i1} - V_{i2} & V_{ic} &= (V_{i1} + V_{i2})/2 \\ V_{od} &= V_{o1} - V_{o2} & V_{oc} &= (V_{o1} + V_{o2})/2 \end{aligned}$$

- In practice, want

$$A_{dm} \gg 1 \quad A_{cm} \ll 1$$

- If the circuit is fully symmetrical,

$$A_{cdm} = 0 \quad A_{dcm} = 0$$

# Fully Balanced Circuit Topology

---

- Signal is carried in  $V_{xd} = V_{x1} - V_{x2}$ . Let

$$V_{x1} = A \sin \omega t + n_1 \quad V_{x2} = -A \sin \omega t + n_2 \quad V_{xd} = 2A \sin \omega t + n_1 - n_2$$

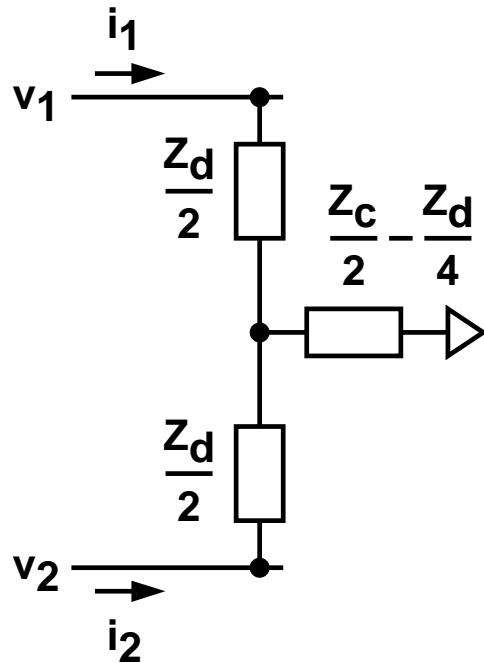
Assuming  $n_1$  and  $n_2$  are uncorrelated, then

$$\text{SNR}_{x1} = \text{SNR}_{x2} = \frac{A^2/2}{n^2} \Rightarrow \text{SNR}_{xd} = \frac{2A^2}{n_1^2 + n_2^2} = \frac{2A^2}{2n^2} = 2\text{SNR}_{x1}$$

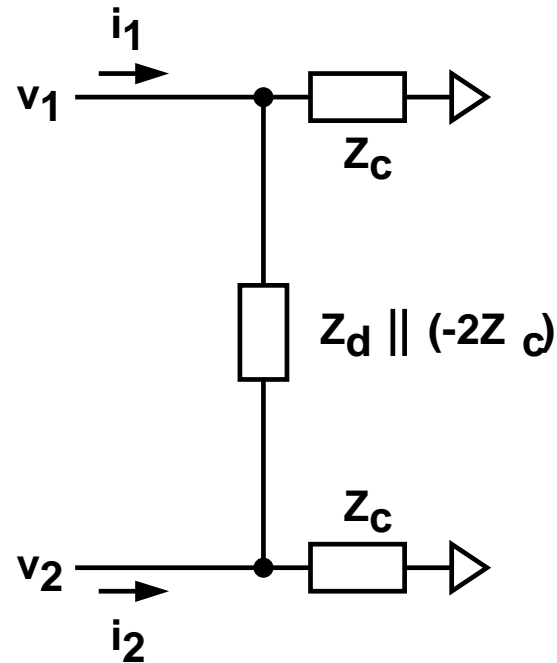
- Immune to common-mode noise, such as noises from power supplies and substrate.
- No even-order harmonic distortion in  $V_{xd}$ .
- Require additional common-mode feedback circuitry to set  $V_{xc} = (V_{x1} + V_{x2})/2$ .

# Small-Signal Models for Differential Loading

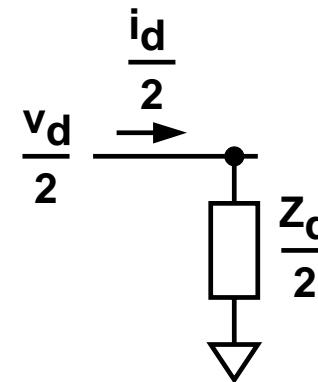
T-Network Model



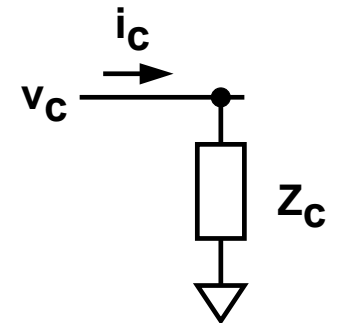
$\pi$ -Network Model



DM Half Circuit



CM Half Circuit



$$V_d = V_1 - V_2$$

$$V_c = (V_1 + V_2)/2$$

$$i_d = (i_1 - i_2)/2$$

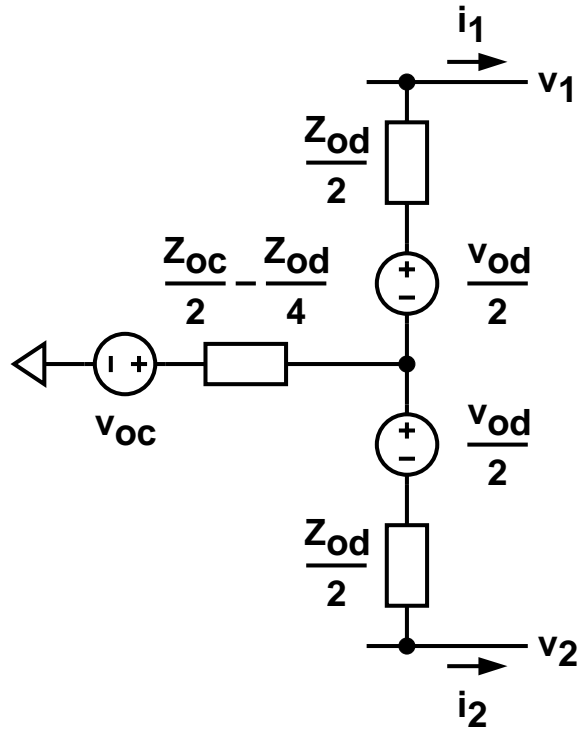
$$i_c = (i_1 + i_2)/2$$

$$Z_d = \left. \frac{V_d}{i_d} \right|_{V_c=0}$$

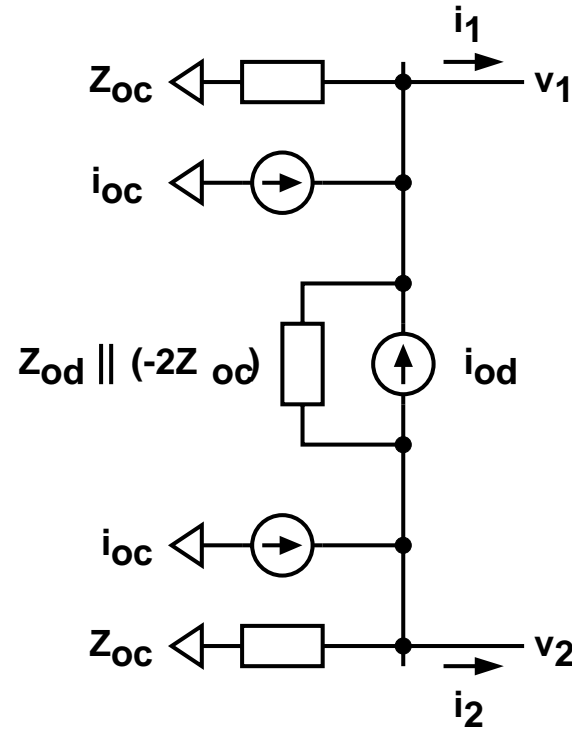
$$Z_c = \left. \frac{V_c}{i_c} \right|_{V_d=0}$$

# Small-Signal Models for Differential Signal Sources

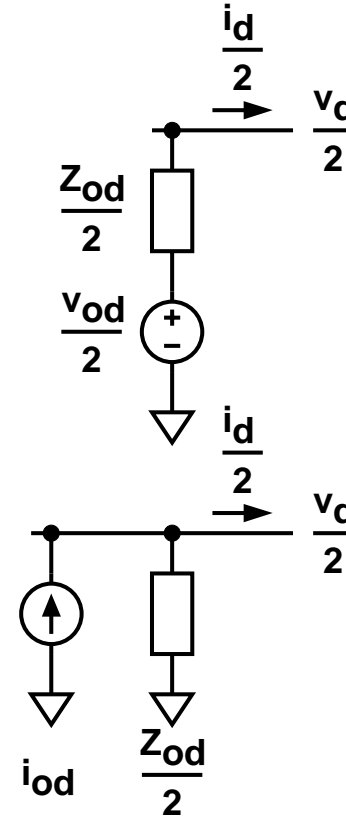
Thevenin-Network Model



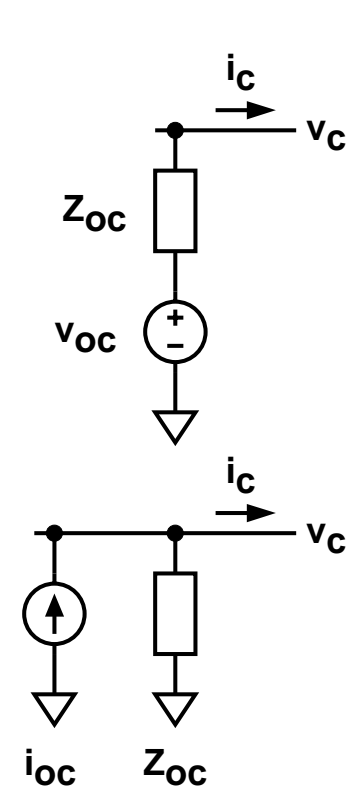
Norton-Network Model



DM Half Circuit



CM Half Circuit



$$V_{od} = A_{dm} V_{id}$$

$$V_{oc} = A_{cm} V_{ic}$$

$$i_{od} = G_{md} V_{id}$$

$$i_{oc} = G_{mc} V_{ic}$$

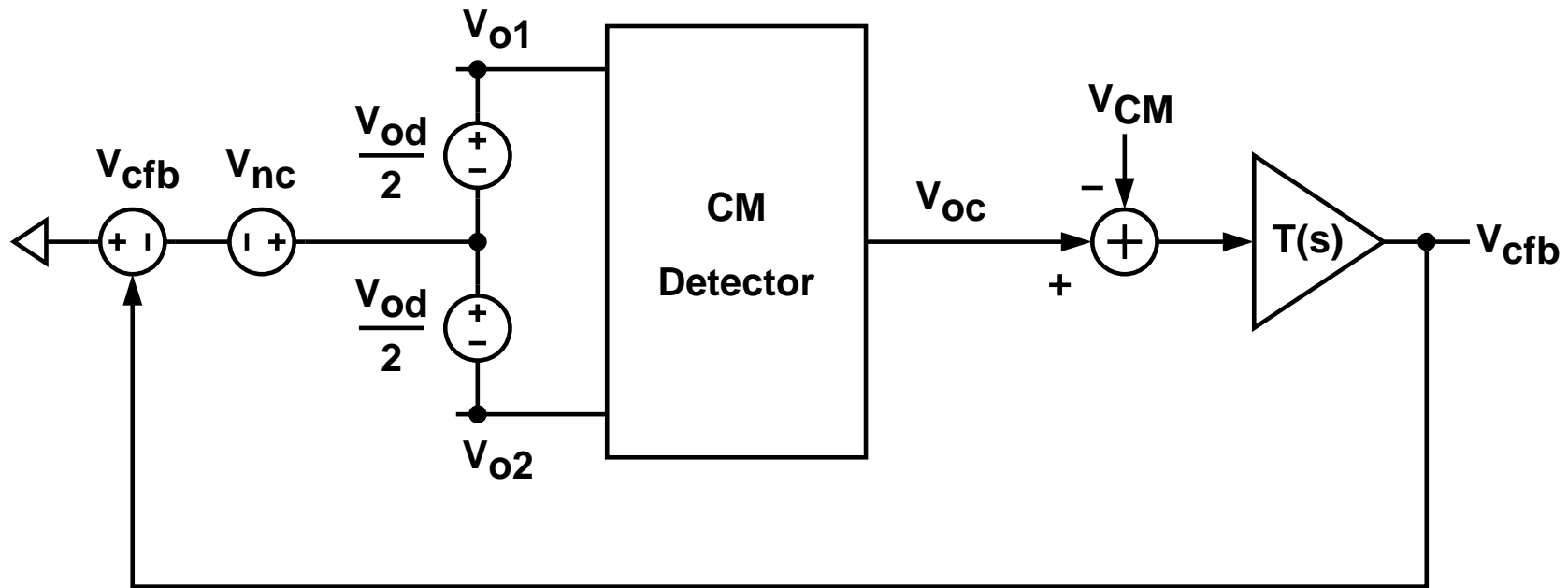
$$A_{dm} = \left. \frac{V_{od}}{V_{id}} \right|_{i_{od}=0}$$

$$A_{cm} = \left. \frac{V_{oc}}{V_{ic}} \right|_{i_{oc}=0}$$

$$G_{md} = \left. \frac{i_{od}}{V_{id}} \right|_{v_{od}=0}$$

$$G_{mc} = \left. \frac{i_{oc}}{V_{ic}} \right|_{v_{oc}=0}$$

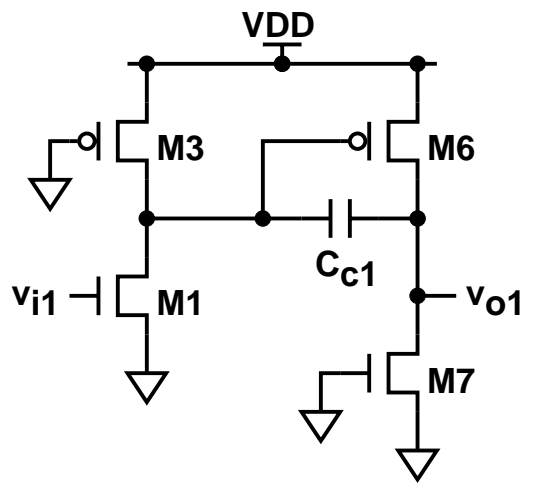
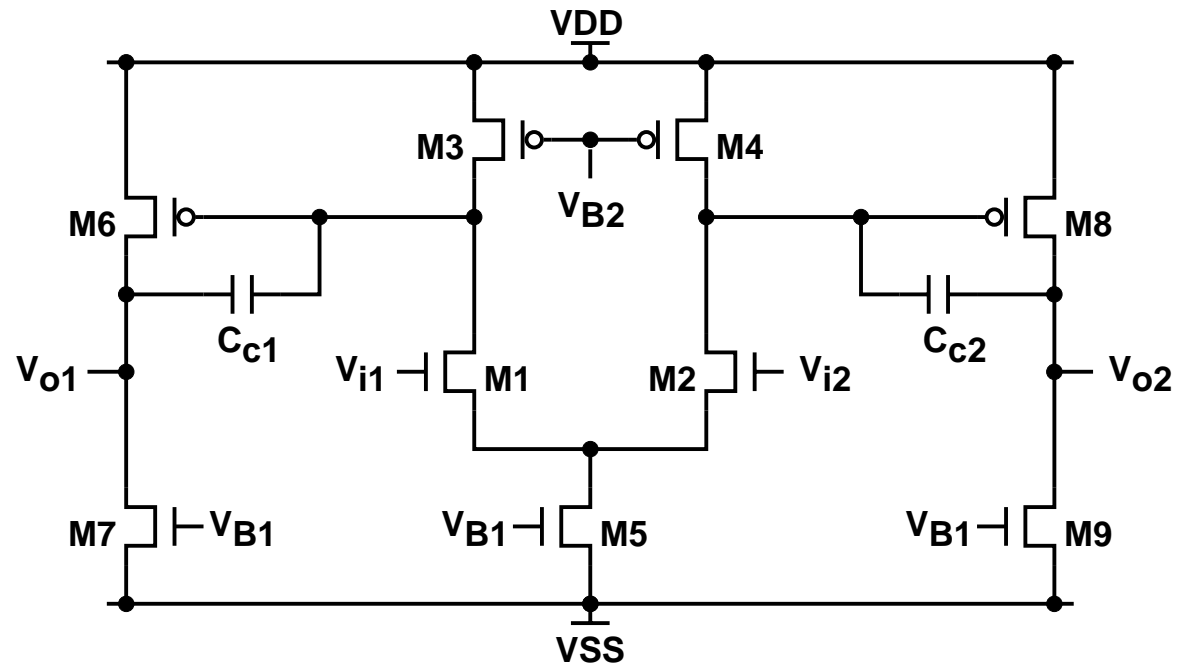
# Common-Mode Feedback (CMFB)



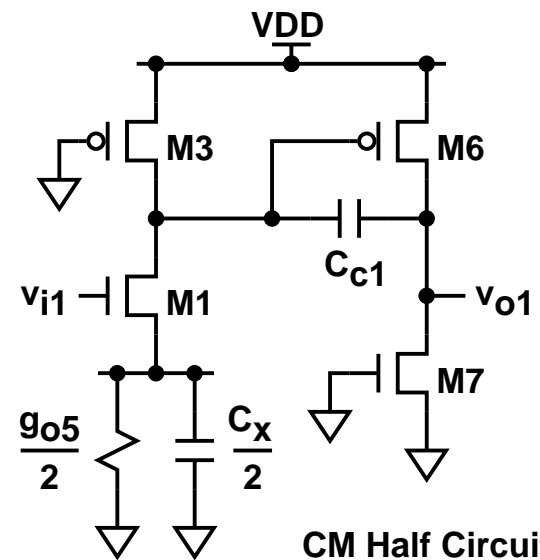
$$V_{cfb} = (V_{oc} - V_{CM}) \cdot T(s) \quad V_{oc} = V_{nc} - V_{cfb} \quad \Rightarrow \quad V_{oc} = \frac{T}{1+T} \times V_{CM} + \frac{1}{1+T} \times V_{nc}$$

- Want large CMFB loop gain,  $T$ , to stabilize  $V_{oc}$ .
- May want large  $\omega_t$  of  $T$  to suppress high-frequency components in  $V_{nc}$ .
- Must check the frequency stability of  $1/[1 + T(s)]$ .

# A Fully Differential Two-Stage Operational Amplifier

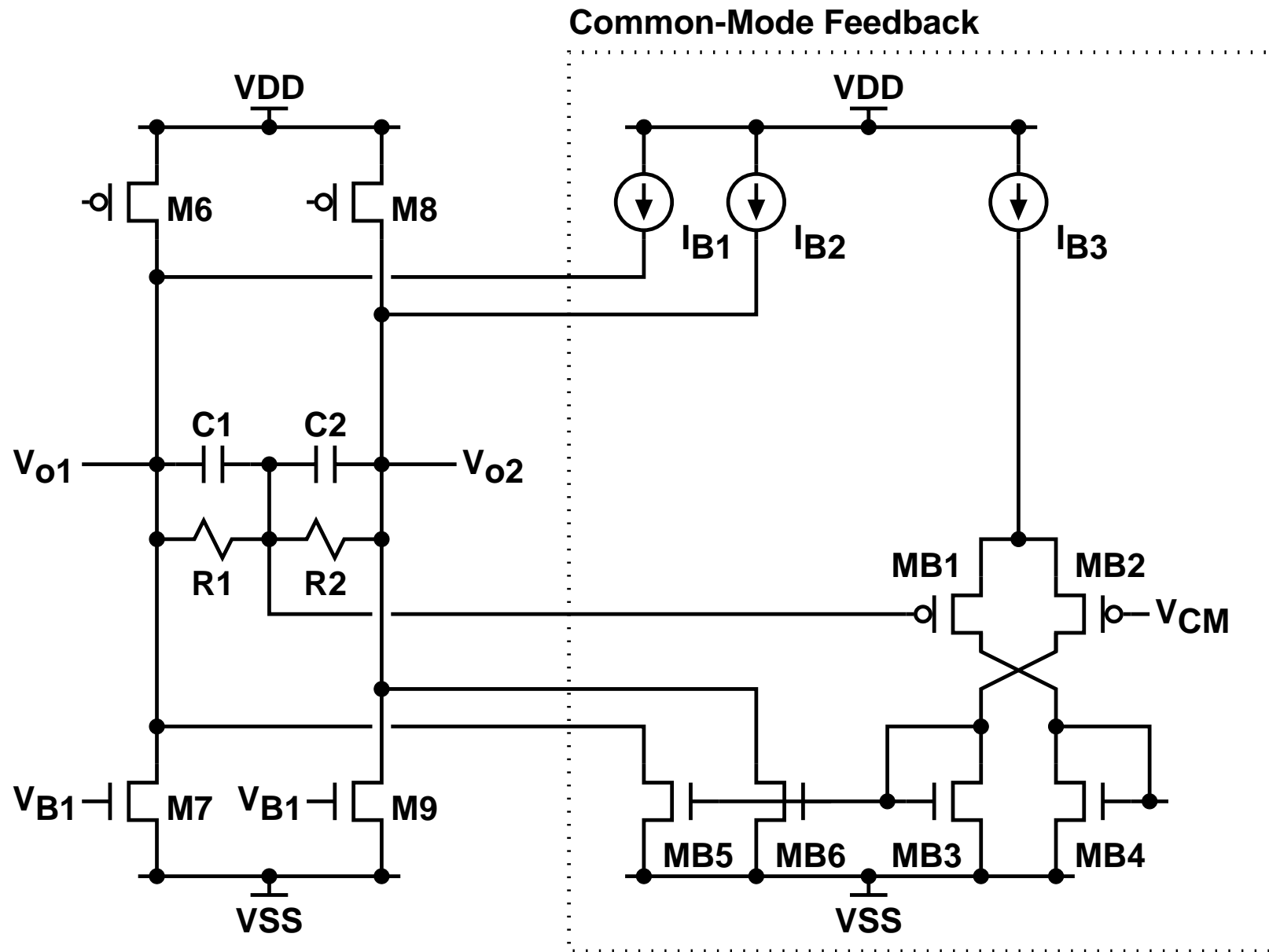


DM Half Circuit

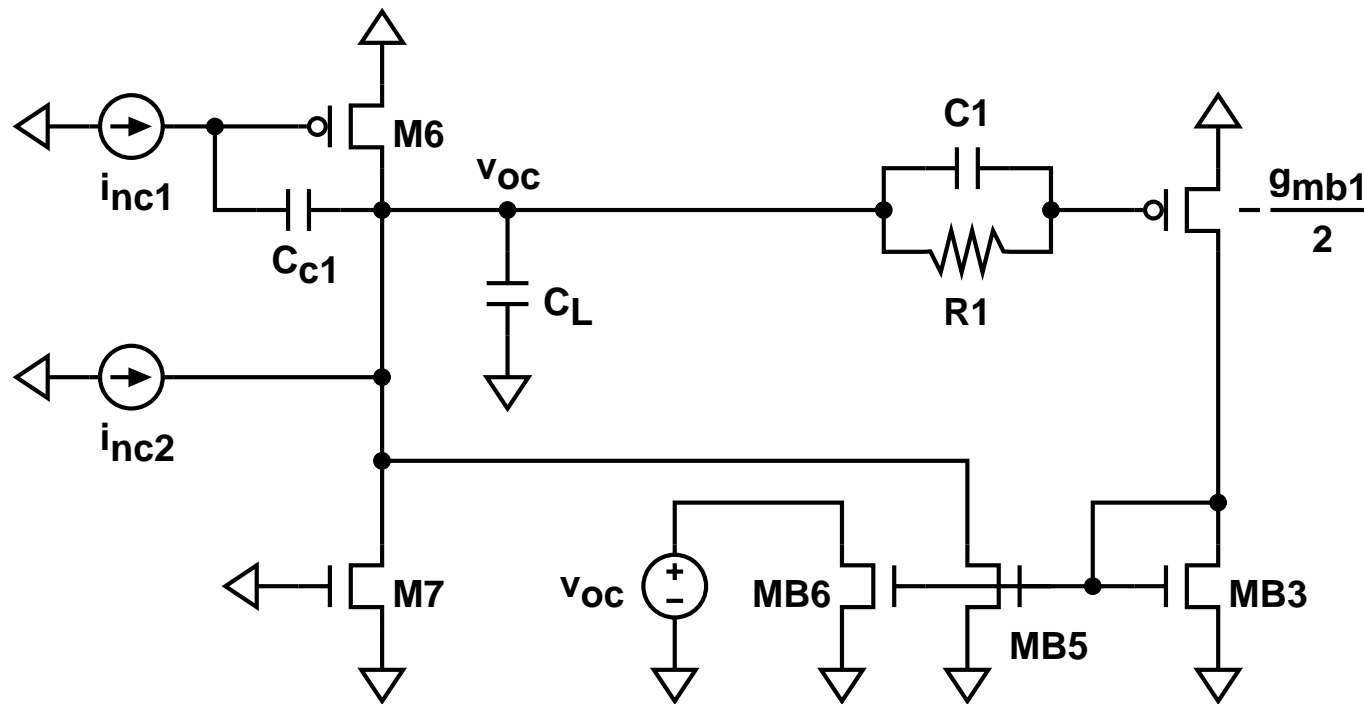


CM Half Circuit

# CMFB Using Resistive Divider and Error Amplifier

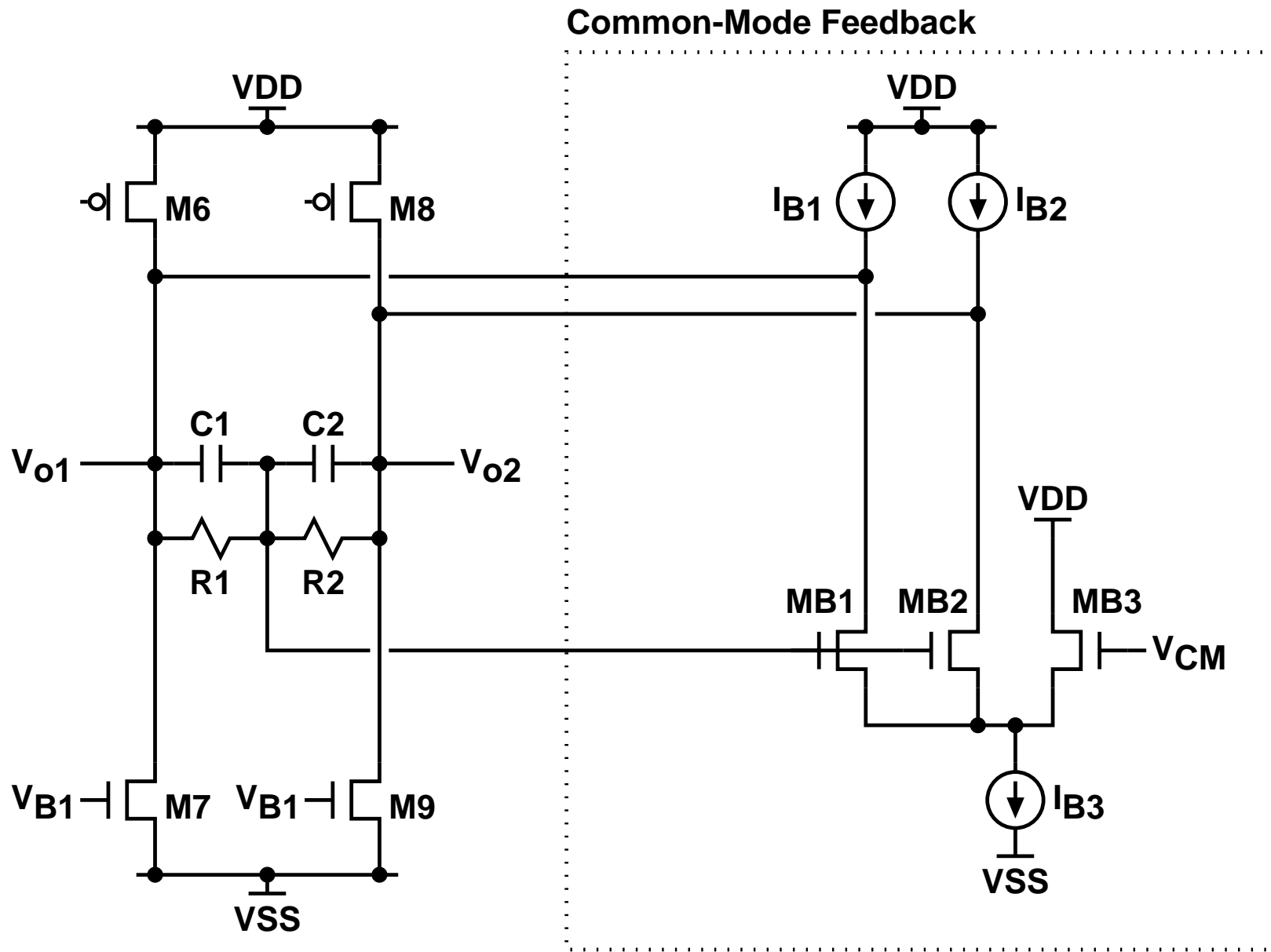


# CMFB Using Resistive Divider and Error Amplifier

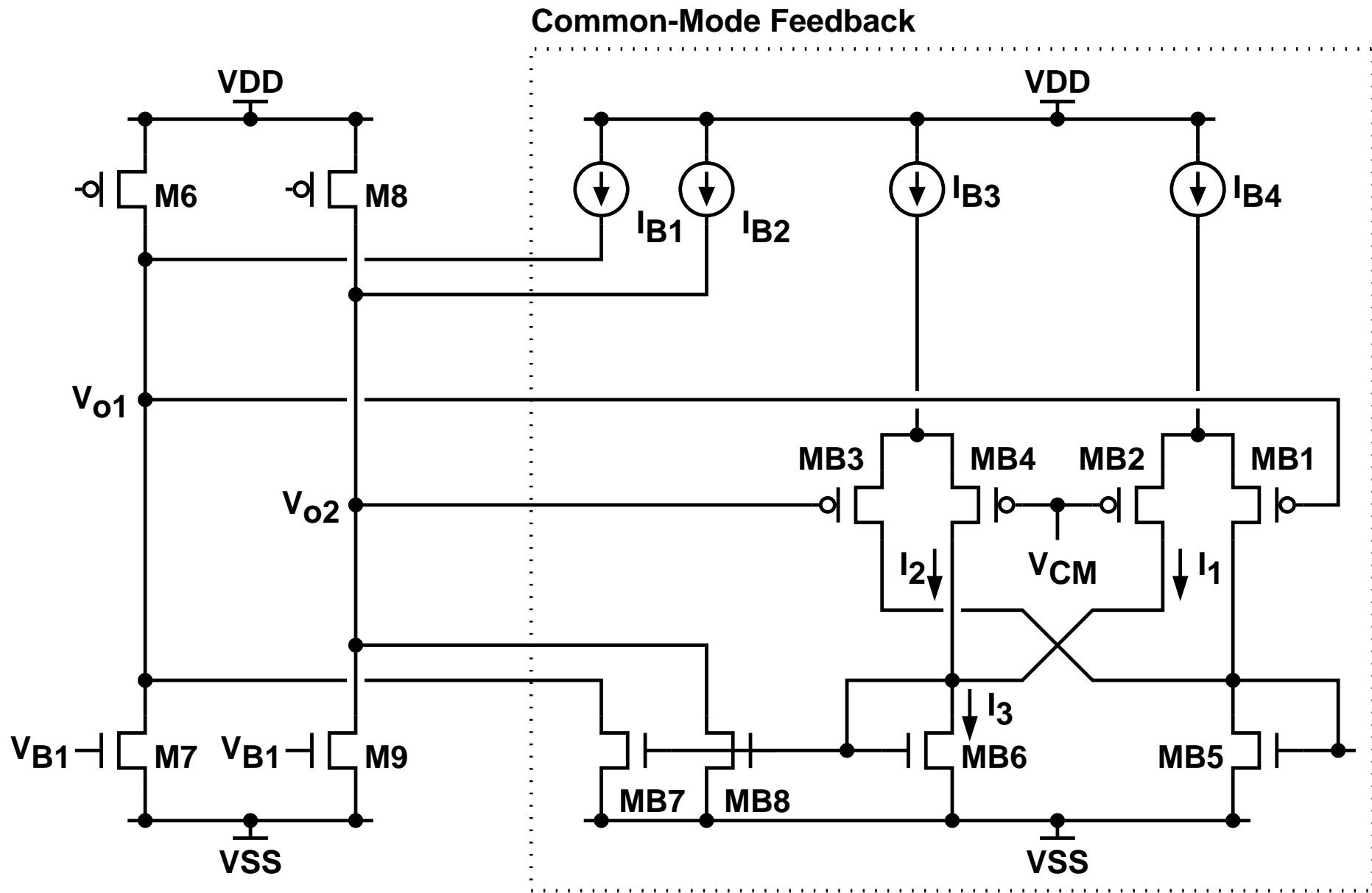


- The loop gain  $|T| \approx g_{mb5}(r_{o6} \parallel r_{o7}) \cdot g_{mb1}/(2g_{mb3})$ .
- $C_1$  and  $C_2$  are used to improve high-frequency response.
- The resistive loading of  $R_1$  and  $R_2$  can degrade  $A_{dm}$ . Voltage buffers can be added between the opamp's outputs and the resistive divider.

# CMFB Using Resistive Divider and Direct Current Injection



# CMFB Using Dual Differential Pairs



## CMFB Using Dual Differential Pairs

---

For the MB1-MB2 and MB3-MB4 source-coupled pairs,

$$I_{BB} = I_{B3} = I_{B4} = 2 \times \frac{k}{2} \cdot V_{ov}^2 \quad k = k' \left( \frac{W}{L} \right)$$

$$I_{dd} = \frac{k}{2} V_{id} \sqrt{4 \frac{I_{BB}}{k} - V_{id}^2} \quad I_{d1} = \frac{I_{BB}}{2} + \frac{I_{dd}}{2} \quad I_{d2} = \frac{I_{BB}}{2} - \frac{I_{dd}}{2}$$

$$\begin{aligned} I_1 &= \frac{I_{BB}}{2} + \frac{k}{4} (V_{oc} + V_{od}/2 - V_{CM}) \sqrt{4 \frac{I_{BB}}{k} - (V_{oc} + V_{od}/2 - V_{CM})^2} \\ &\approx \frac{I_{BB}}{2} + \frac{k}{4} (V_{oc} - V_{CM} + V_{od}/2) \sqrt{4V_{ov}^2 - (V_{od}/2)^2 - (V_{oc} - V_{CM})V_{od}} \\ &\approx \frac{I_{BB}}{2} + \frac{k}{4} (V_{oc} - V_{CM} + V_{od}/2) \sqrt{4V_{ov}^2 - (V_{od}/2)^2} \\ &\quad \times \left\{ 1 - \frac{1}{2} \left[ \frac{(V_{oc} - V_{CM})V_{od}}{4V_{ov}^2 - (V_{od}/2)^2} \right] - \frac{1}{8} \left[ \frac{(V_{oc} - V_{CM})V_{od}}{4V_{ov}^2 - (V_{od}/2)^2} \right]^2 + \dots \right\} \end{aligned}$$

## CMFB Using Dual Differential Pairs

---

$$I_2 \approx \frac{I_{BB}}{2} + \frac{k}{4}(V_{oc} - V_{CM} - V_{od}/2)\sqrt{4V_{ov}^2 - (V_{od}/2)^2}$$

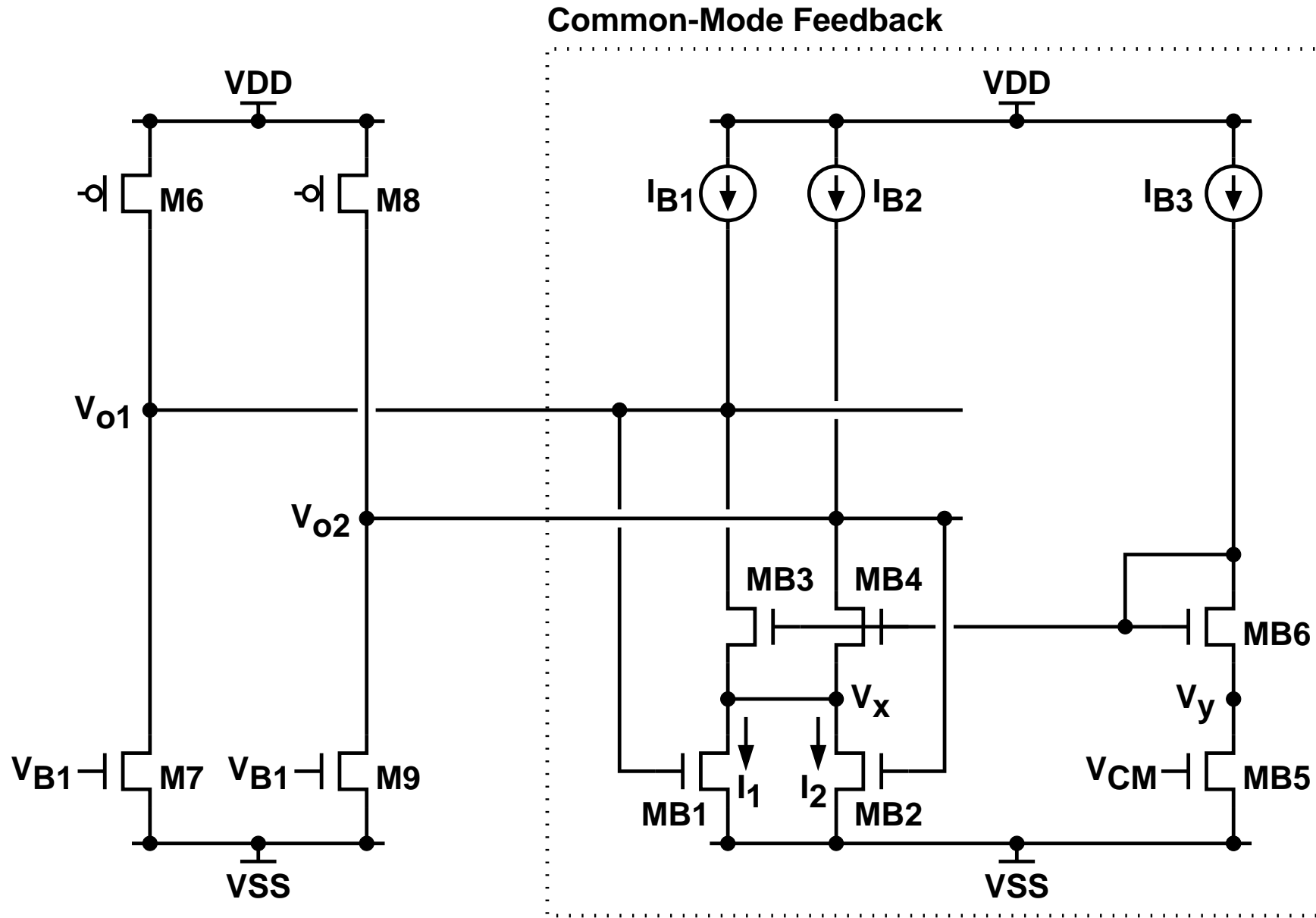
$$\times \left\{ 1 + \frac{1}{2} \left[ \frac{(V_{oc} - V_{CM})V_{od}}{4V_{ov}^2 - (V_{od}/2)^2} \right] - \frac{1}{8} \left[ \frac{(V_{oc} - V_{CM})V_{od}}{4V_{ov}^2 - (V_{od}/2)^2} \right]^2 + \dots \right\}$$

$$I_3 = I_1 + I_2 \approx I_{BB} + \frac{k}{2}(V_{oc} - V_{CM})\sqrt{4V_{ov}^2 - (V_{od}/2)^2}$$

$$\times \left\{ 1 - \frac{1}{4} \left[ \frac{V_{od}^2}{4V_{ov}^2 - (V_{od}/2)^2} \right] - \frac{1}{8} \left[ \frac{(V_{oc} - V_{CM})V_{od}}{4V_{ov}^2 - (V_{od}/2)^2} \right]^2 + \dots \right\}$$

- The input devices, MB1–MB4, must remain in the forward-active region over the voltage range of  $V_{o1}$  and  $V_{o2}$ .
- The variation in  $V_{od}$  can produce an ac component in  $I_3$  as well as  $V_{oc}$ .
- If  $V_{oc} = V_{CM}$ ,  $I_1$  and  $I_2$  are nonlinear functions of  $V_{od}$ , but  $I_3 = I_1 + I_2$  is a constant.

# CMFB Using Transistors in the Triode Region



## CMFB Using Transistors in the Triode Region

---

MB1, MB2, and MB5 are in the triode region. Let  $k_{B1} = k_{B2} = k_{B5} = k$ ,

$$I_1 = k \left( V_{o1} - V_{tn} - \frac{1}{2}V_x \right) V_x \quad I_2 = k \left( V_{o2} - V_{tn} - \frac{1}{2}V_x \right) V_x \quad I_{B3} = k \left( V_{CM} - V_{tn} - \frac{1}{2}V_y \right) V_y$$

$$\Rightarrow I_1 + I_2 = 2k \left( V_{oc} - V_{tn} - \frac{1}{2}V_x \right) V_x \quad V_x \approx V_y = \frac{I_{B3}}{k \left( V_{CM} - V_{tn} - \frac{1}{2}V_y \right)}$$

$$I_1 + I_2 = 2I_{B3} \cdot \frac{V_{oc} - V_{tn} - \frac{1}{2}V_x}{V_{CM} - V_{tn} - \frac{1}{2}V_y} = 2I_{B3} \left( 1 + \frac{V_{oc} - V_{CM}}{V_{CM} - V_{tn} - \frac{1}{2}V_y} \right)$$

- Output swing is reduced, since it is required that  $V_{o1,o2} > V_{tn} + V_x$ .
- MB1 and MB2 are in the triode region, their effective  $g_m$  can be small, thus degrading loop gain and bandwidth of the CMFB.



# Switched-Capacitor CMFB

---

- The opamp operates in two different modes. It is in the *normal* mode when  $\phi_2$  is low.
- Assuming  $\Delta Q$  charges are injected into  $C_3$  and  $C_4$  when  $\phi_1$  switches are turned off,

$$V_{oc} - V_x = V_{CM} - V_{CB} + \frac{\Delta Q}{C_3} \quad \Rightarrow \quad V_{oc} \approx V_{CM} + \frac{\Delta Q}{C_3}$$

- The loop gain of the CMFB is approximately

$$|T| \approx \frac{C_1}{C_1 + C_{gs,B1}} \times g_{m,B1} \cdot R_{o1}$$

- $C_1$  and  $C_2$  add differential-mode capacitive loading to the outputs.
- The additional common-mode capacitive loading is  $(C_1 + C_2) \parallel (C_{gs,B1} + C_{gs,B2})$ .
- The value of  $C_{3,4}$  may be between 1/4–1/10 of  $C_{1,2}$  for low-pass filter function.

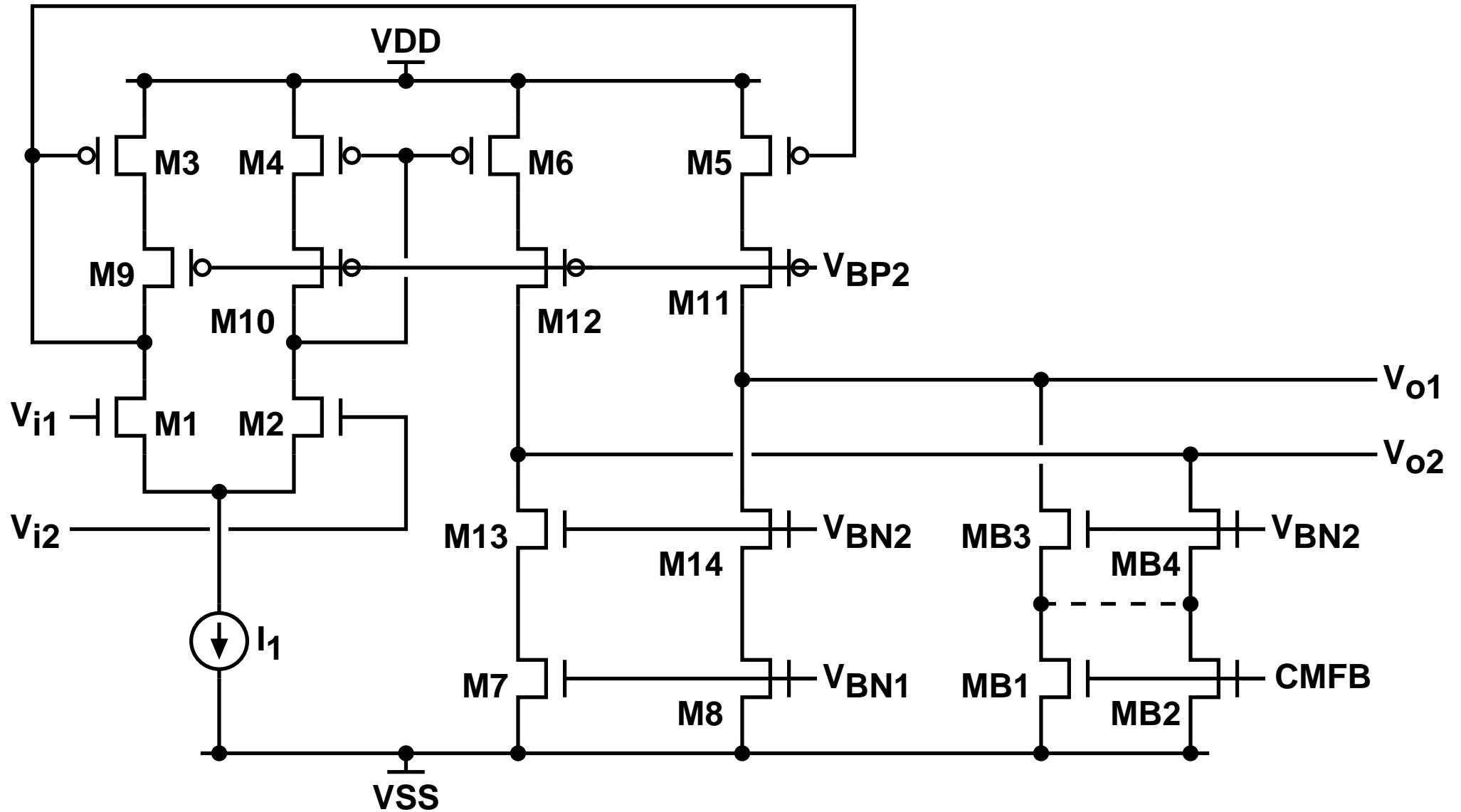


# Folded-Cascode Operational Amplifier

---

- Frequency compensation is provided by the capacitive loads at the outputs.
- Non-dominant poles are determined by M3 and M4, and  $\approx \omega_{t3}$  ( $\omega_{t4}$ ).
- It is not uncommon that  $I_{D1,D2} \simeq I_{D3,D4}$ .
- For high-speed designs, use pMOST input stage. The resulting opamps has higher non-dominant poles.
- Active cascode configuration can be applied to M3, M4, M5, and M6.

# Current-Mirror Operational Amplifier



# Current-Mirror Operational Amplifier

---

The M3-M5 and M4-M6 current mirrors have a current gain of  $K$ .

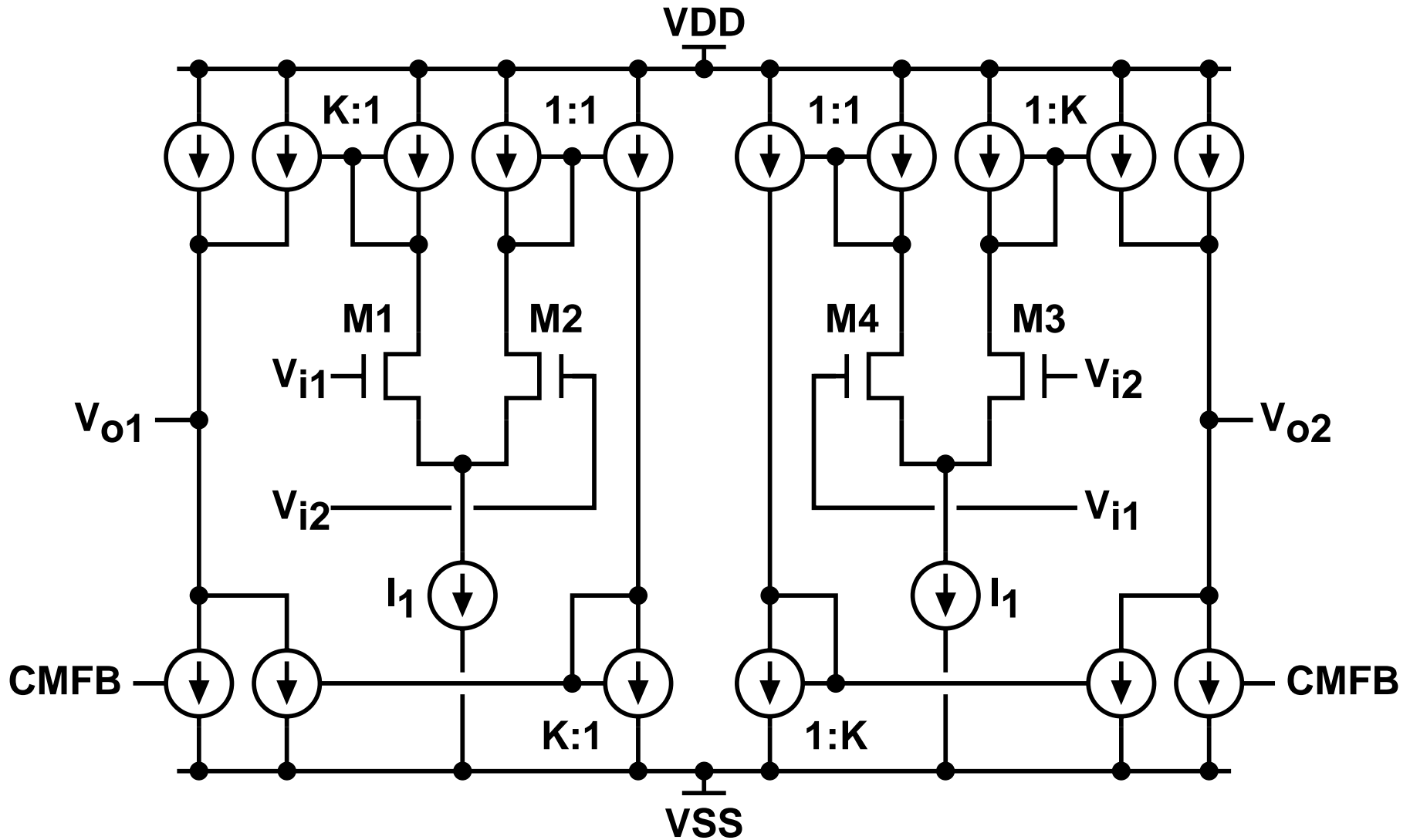
$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{1}{K} \left(\frac{W}{L}\right)_5 = \frac{1}{K} \left(\frac{W}{L}\right)_6$$
$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{1}{K} I_{D5} = \frac{1}{K} I_{D6} = \frac{1}{2} I_1$$

- The single-ended maximum output current for slewing is

$$I_{o(max)} = \frac{K}{2} I_1$$

- For a general-purpose fully differential opamp, may use large pMOST input stage,  $K=2$ , and wide-swing enhanced output-impedance cascode current mirrors.

# Current-Mirror Push-Pull Operational Amplifier



# Current-Mirror Push-Pull Operational Amplifier

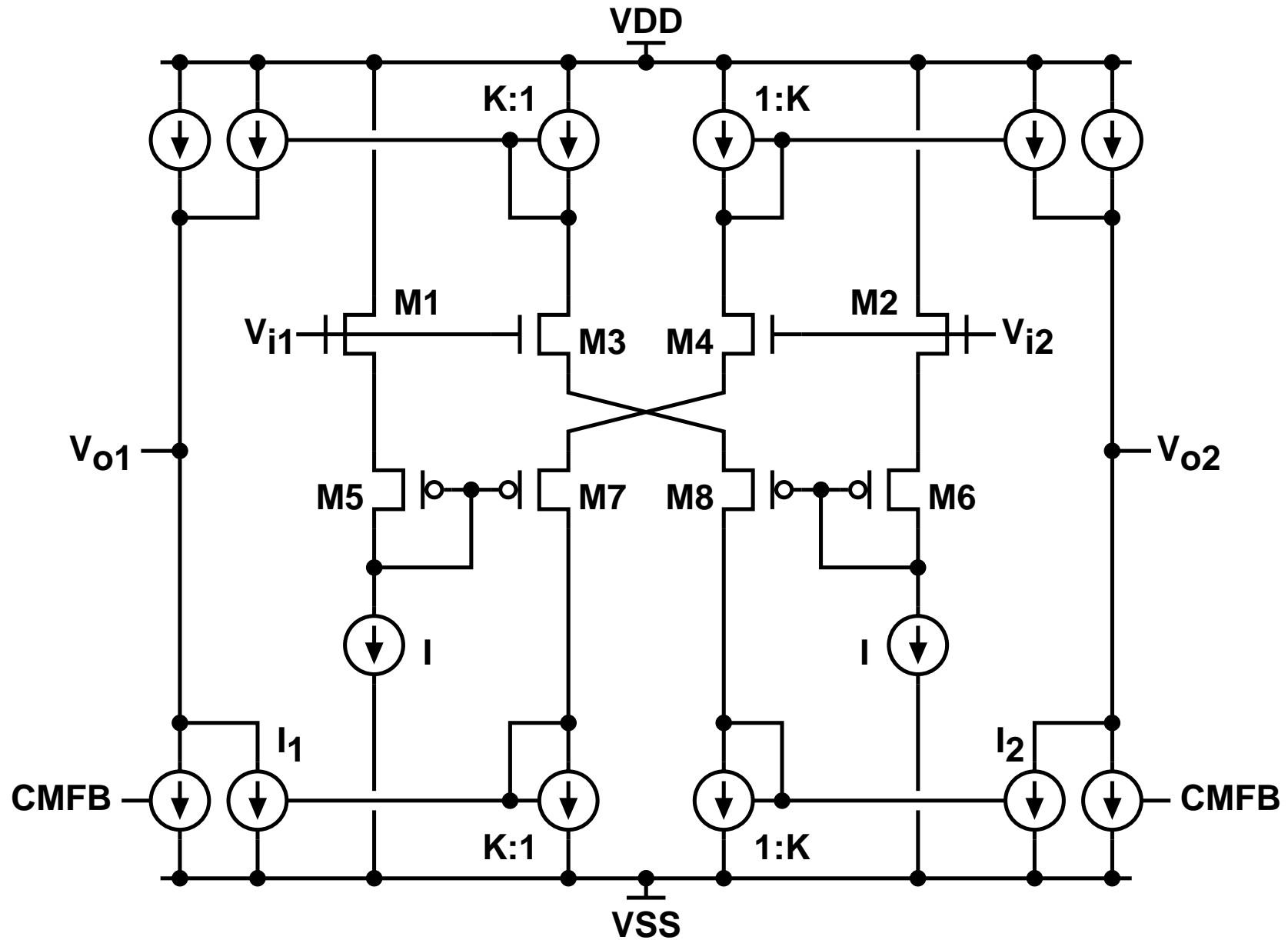
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- The single-ended maximum output current for slewing is

$$I_{o(max)} = K I_1$$

- The small-signal response is slower due to additional signal paths.

# Class-AB Operational Amplifier



# Class-AB Operational Amplifier

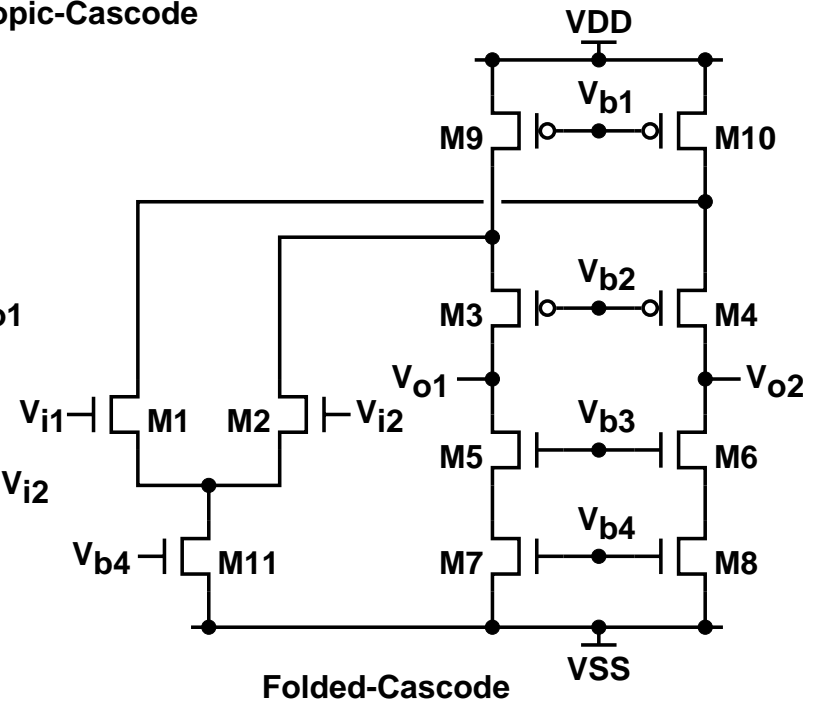
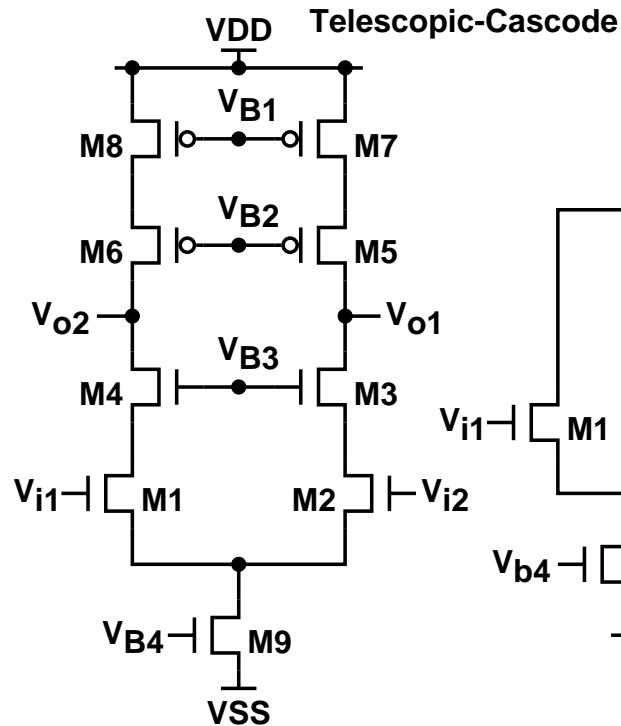
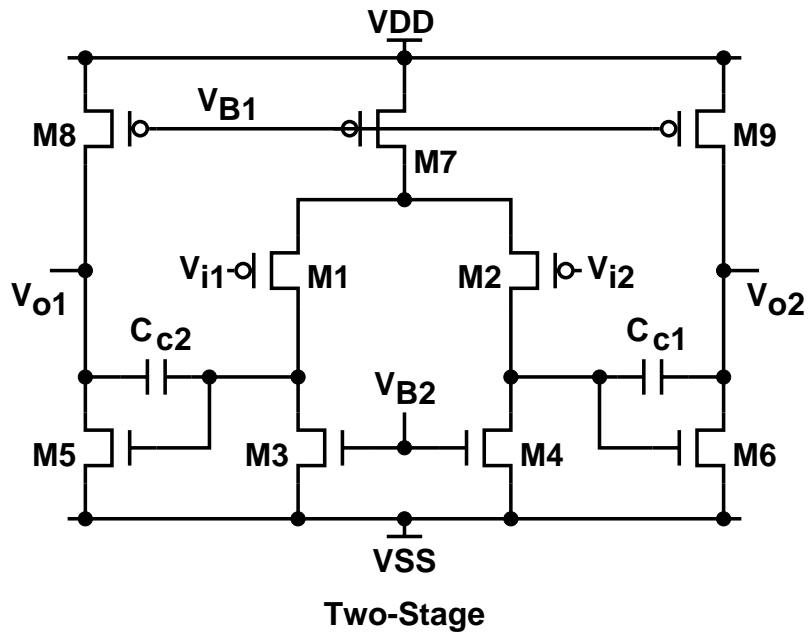
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If nMOSTs M1–M4 are identical, and pMOSTs M5–M8 are identical, and all current mirrors have a current gain of  $K$ , then the bias currents are

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = \frac{1}{K}I_1 = \frac{1}{K}I_2 = I$$

- Low quiescent power and large slew rate.
- The input level shifter increases the noise and offset, and adds additional poles.
- Not suitable for low-voltage operation.

# Fully Differential Operational Amplifiers



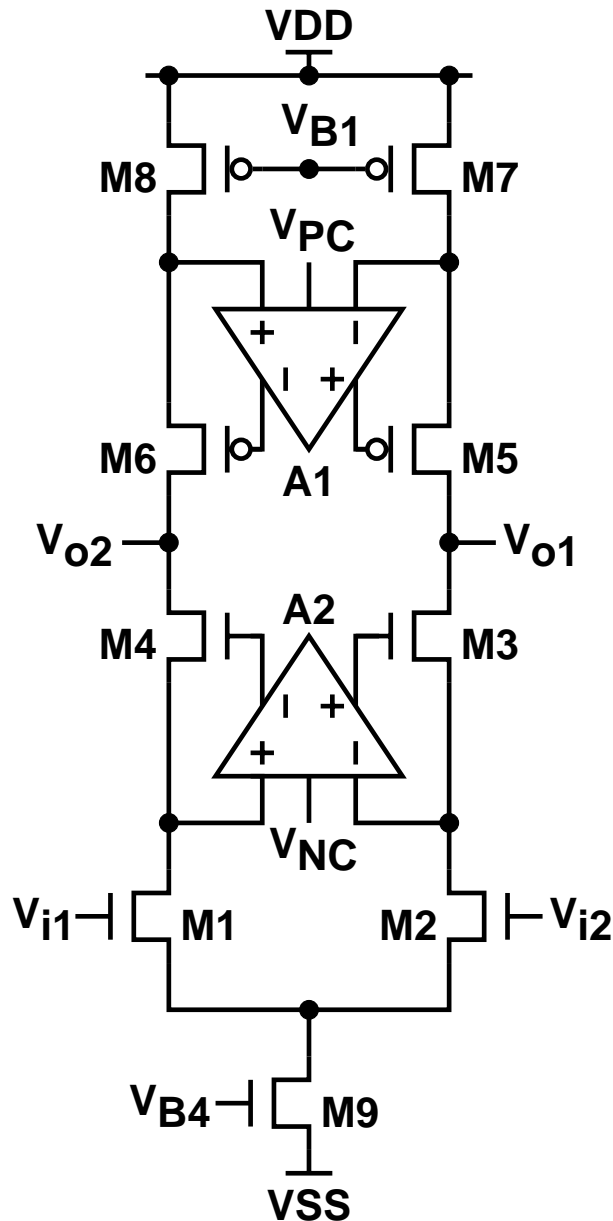
$$\Delta V_o(\text{Two Stage}) = V_{DD} - 2V_{DSAT}$$

$$\Delta V_o(\text{Telescopic}) = V_{DD} - 5V_{DSAT} - 3V_{margin}$$

$$\Delta V_o(\text{Folded-Cascode}) = V_{DD} - 4V_{DSAT} - 2V_{margin}$$

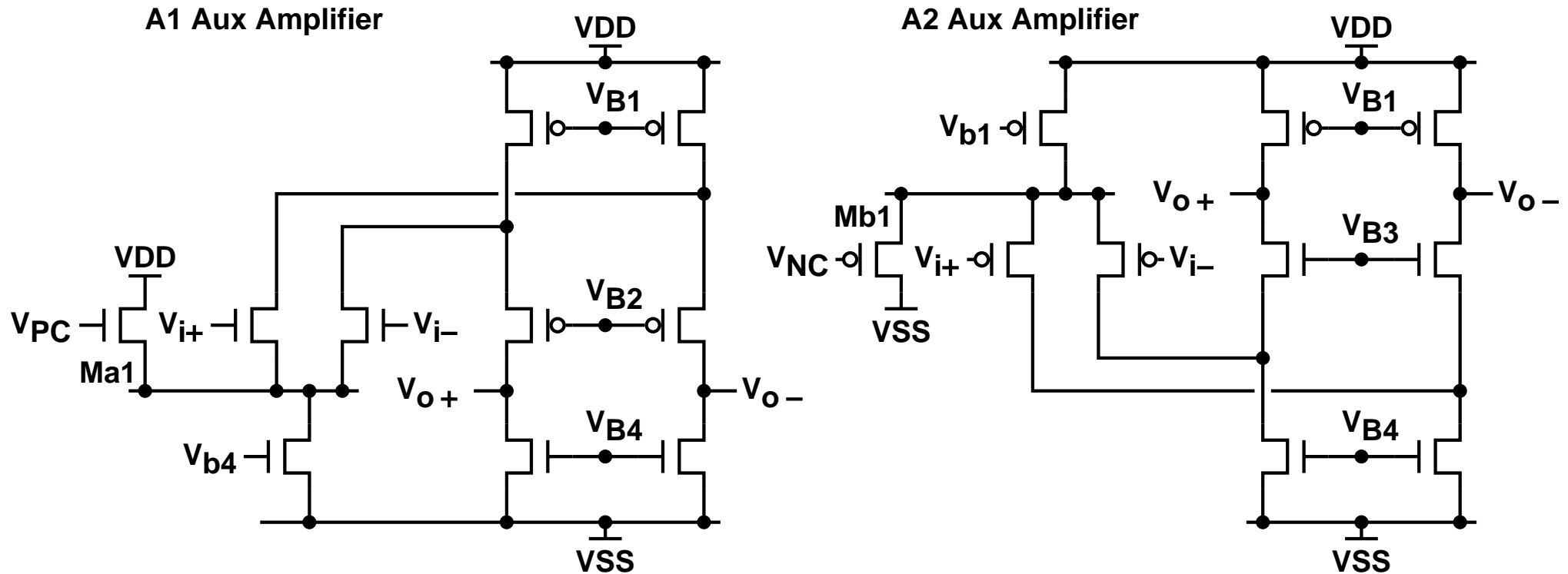
$$\text{SNR} \cdot \frac{\text{Speed}}{\text{Power}} \propto \frac{\Delta V_o^2}{kT/C} \cdot \frac{g_m/C}{V_{DD} \cdot I} \propto \frac{\Delta V_o^2}{V_{DD}}$$

# Active-Cascode Telescopic Operational Amplifier



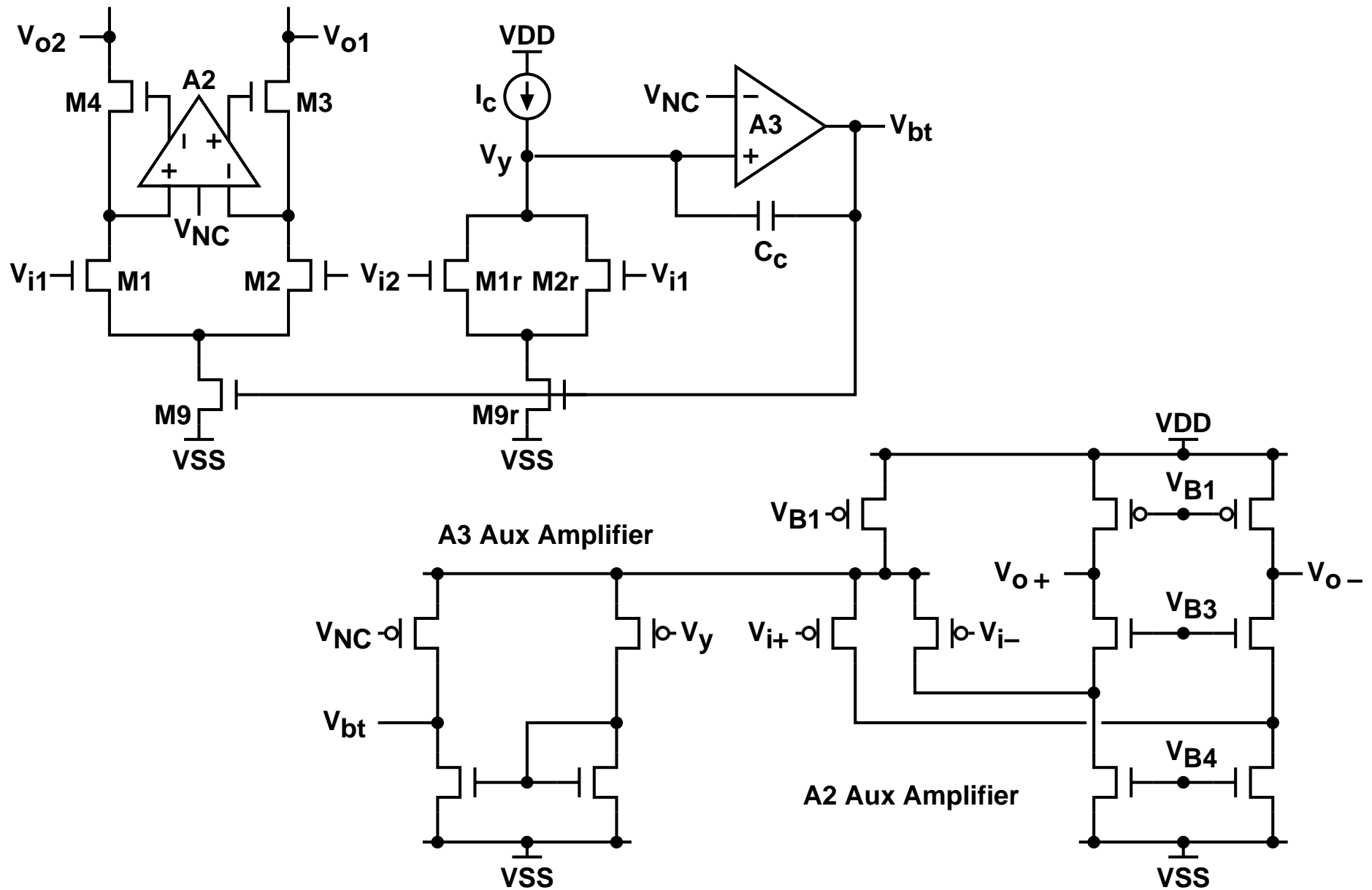
- Have the best speed/power ratio.
- A1 and A2 auxiliary amplifiers are used to increase output impedance and the dc voltage gain,  $A_v(0)$ .
- Explicit compensation capacitors may be required at the outputs of A1 and A2.
- To increase  $\Delta V_o$ , M7, M8, and M9, can be biased in the triode region. However,  $A_v(0)$  is reduced due to the reduced  $r_o$  of M7 and M8. Also, CMRR and PSRR are degraded due to the reduced  $r_o$  of M9.
- Reference: Gulati and Lee, JSSC 12/98, pp. 2010–2019.

# Fully Differential Gain-Enhancement Auxiliary Amplifiers



- $V_{S3} \approx V_{S4} \approx V_{NC}$ , due to the CMFB of M3, M4, and A2.
- $V_{S5} \approx V_{S6} \approx V_{PC}$ , due to the CMFB of M5, M6, and A1.

# Replica-Tail Feedback



# Replica-Tail Feedback

---

- The feedback loop increase M9's output resistance,  $R_{o9}$ , i.e.,

$$R_{o9} = r_{o9} [1 + A_3 \cdot (g_{m9r}r_{o9r})(g_{m1r}r_{o1r})] = r_{o9} [1 + A_{loop}]$$

- It can be shown the effective common-mode transconductance of M1-M2-M9 is

$$G_e = G_m \times \frac{1 + A_{loop} \cdot M}{1 + A_{loop}} \quad M = 1 - \frac{g_{m9}}{g_{m9r}} \cdot \frac{G_{mr}}{G_m}$$

$$G_m = \frac{g_m}{1 + g_m r_{o9}} \quad g_m = g_{m1} + g_{m2}$$

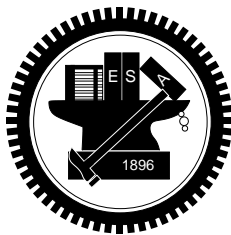
$$G_{mr} = \frac{g_{mr}}{1 + g_{mr} r_{o9r}} \quad g_{mr} = g_{m1r} = g_{m2r}$$

- The mismatch  $M$  and the bandwidth of the feedback loop limit the enhancement effect.

# Operational Amplifiers and Their Basic Configurations

Jieh-Tsorng Wu

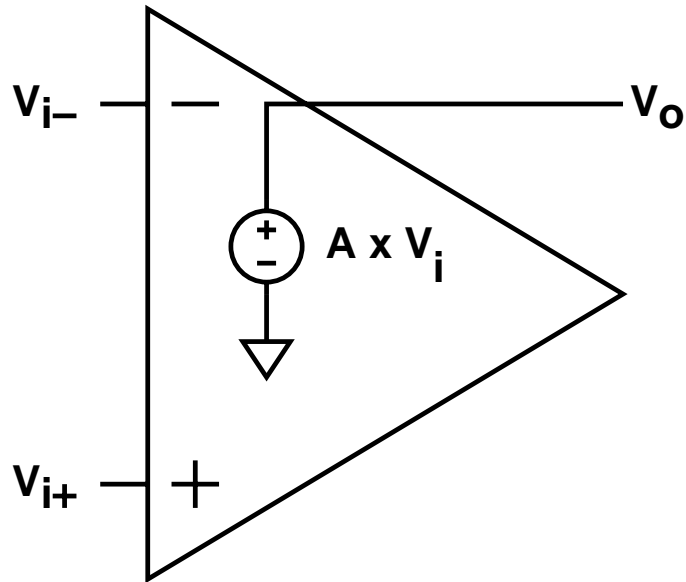
July 16, 2002



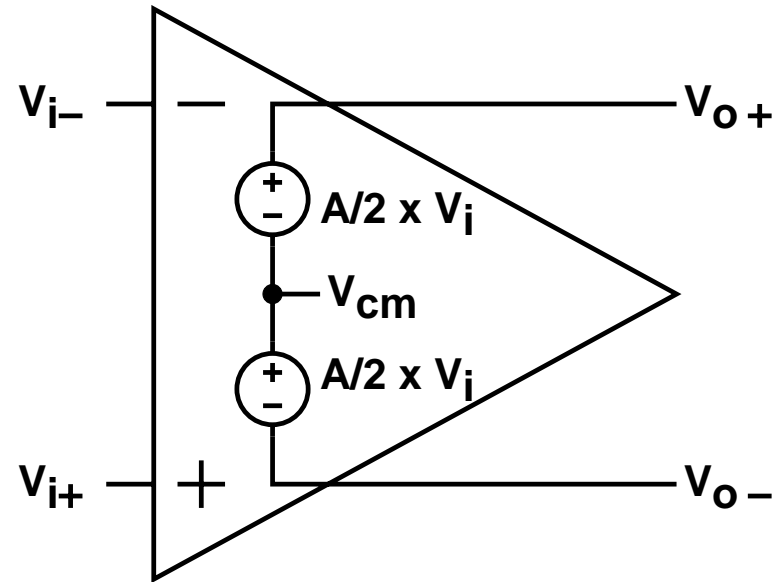
National Chiao-Tung University  
Department of Electronics Engineering

# Ideal Operational Amplifier

## Single-Ended Output

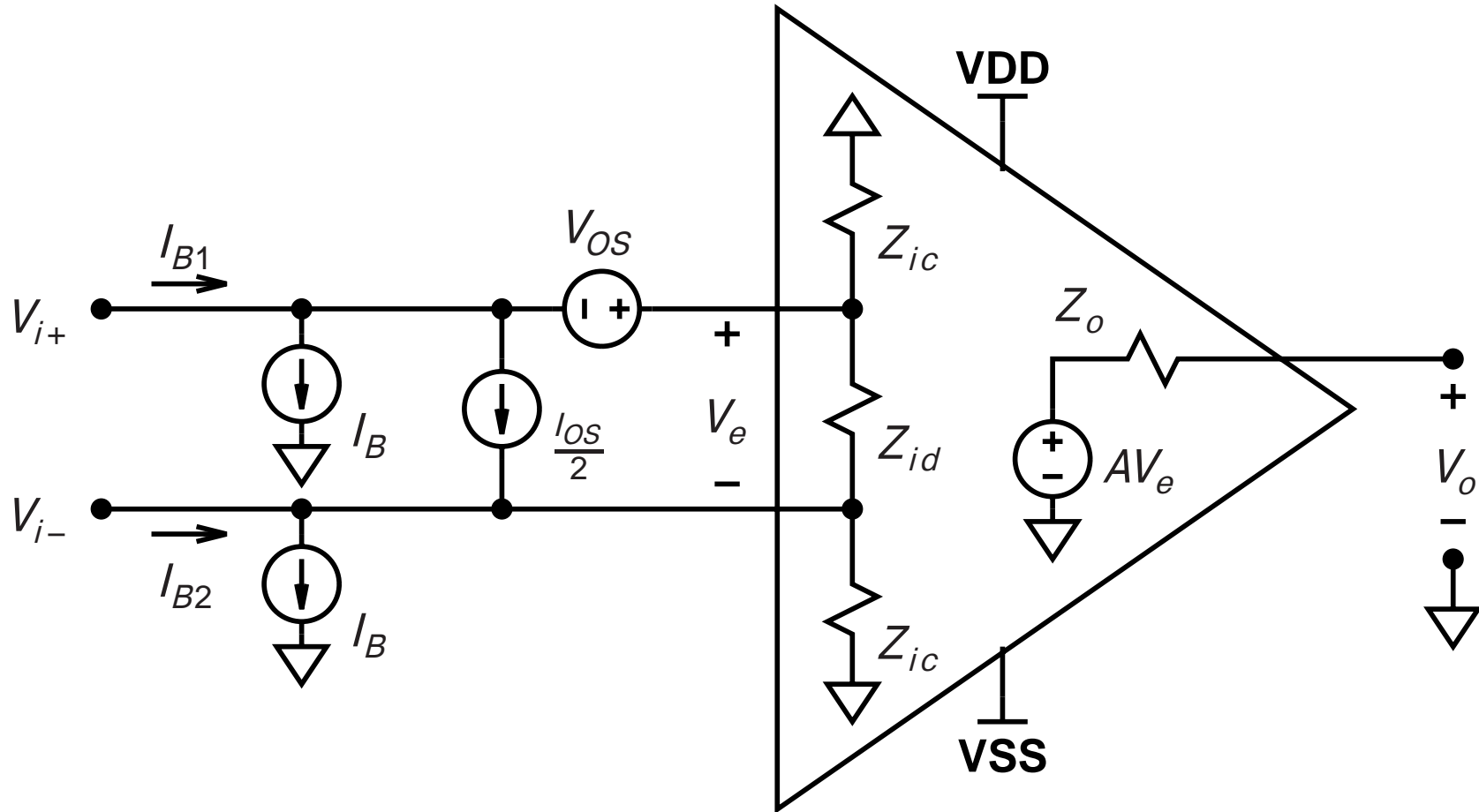


## Fully Differential



- $V_o = A \times V_i$
- Ideal opamp:
  - $A \rightarrow \infty$ ,  $Z_{in} \rightarrow \infty$ ,  $Z_{out} \rightarrow 0$ .
  - No frequency dependence.

# Operational Amplifier Imperfections (I)



Differential Input =  $V_{id} \equiv V_{i+} - V_{i-}$

Common-mode Input =  $V_{ic} \equiv \frac{V_{i+} + V_{i-}}{2}$

## Operational Amplifier Imperfections (II)

---

- Finite differential-mode gain,  $A_{dm} \equiv \left. \frac{dV_o}{dV_{id}} \right|_{V_{ic}=0}$
- Non-zero common-mode gain,  $A_{cm} \equiv \left. \frac{dV_o}{dV_{ic}} \right|_{V_{id}=0}$

$$\text{Common-Mode Rejection Ratio (CMRR)} \equiv \left| \frac{A_{dm}}{A_{cm}} \right|$$

- Frequency response:  $A_{dm}(s)$  and  $A_{cm}(s)$ .
- Input impedance:  $Z_{id}$  and  $Z_{ic}$ .
- Output impedance:  $Z_o$ .
- Power supply bias current:  $I_{DD}$ .

## Operational Amplifier Imperfections (III)

---

- Input offset voltage:  $V_{OS} \equiv (V_{i+} - V_{i-})|_{V_o=0}$
- Input bias current:  $I_B \equiv (I_{B1} + I_{B2})/2$
- Input offset current:  $I_{OS} \equiv I_{B1} - I_{B2}$
- Input common-mode range:  $V_{ic(max)}$  and  $V_{ic(min)}$ . Range of  $V_{ic}$  for which amplifier is operational.
- Output voltage range:  $V_{o(max)}$  and  $V_{o(min)}$ .
- Maximum output currents:  $I_{o(max)}^+$  and  $I_{o(max)}^-$ .
- Internal slew rate:  $SR^+$  and  $SR^-$ . Internally-limited rate of change in  $V_o$  in response to a step input.

## Operational Amplifier Imperfections (IV)

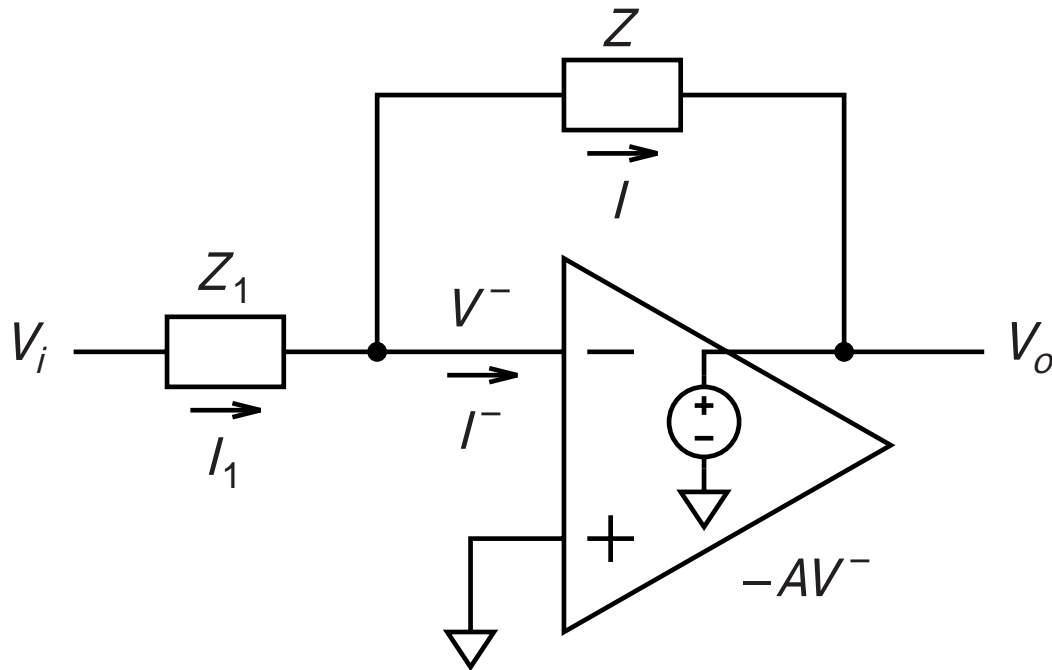
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- Power supply signal gain:  $A_{DD}(s)$  and  $A_{SS}(s)$ . Power supply rejection ratio (PSRR) are:

$$\text{PSRR}_{DD} \equiv \left| \frac{A_{dm}}{A_{DD}} \right| \quad \text{PSRR}_{SS} \equiv \left| \frac{A_{dm}}{A_{SS}} \right|$$

- Supply capacitance. Capacitive coupling between power supplies and the opamp's input leads.
- Inherent noises in active devices and resistors.

# Inverting Configuration



Let  $Z_{in} = \infty$  for the opamp, then

$$I^- = I_1 - I = \frac{V_i - V^-}{Z_1} - \frac{V^- - V_o}{Z} = 0$$

$$V_o = -A \times V^-$$

$$\text{Closed-Loop Gain} = A_{CL} = \frac{V_o}{V_i} = -\frac{Z}{Z_1} \left[ \frac{1}{1 + \frac{1}{A} \left(1 + \frac{Z}{Z_1}\right)} \right] = -\frac{Z}{Z_1} \left( \frac{1}{1 + \epsilon_{rr}} \right)$$

$$\text{Input Impedance} = Z_{ic} = \frac{V_i}{I_1} = \frac{Z_1}{1 + \frac{A_{CL}}{A}} \approx \frac{Z_1}{1 + \frac{1}{A} \cdot \left(-\frac{Z}{Z_1}\right)}$$

# Inverting Configuration

---

The error term,  $\epsilon_{rr}(s)$ , is due to the finite opamp gain.

$$\epsilon_{rr} = \frac{1}{A} \left( 1 + \frac{Z}{Z_1} \right)$$

- $\epsilon_{rr}(s)$  can be expressed in terms of magnitude and phase, i.e.,

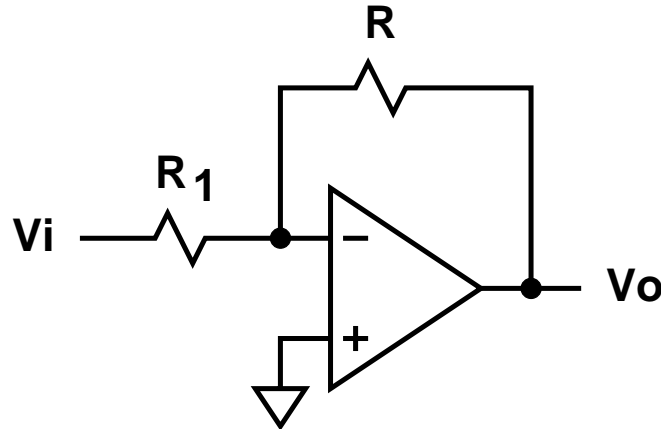
$$\epsilon_{rr}(j\omega) = m_{rr}(\omega)e^{j\varphi_{rr}(\omega)} \approx m_{rr}(\omega) + j\varphi_{rr}(\omega)$$

- If  $\epsilon_{rr} \ll 1$ ,

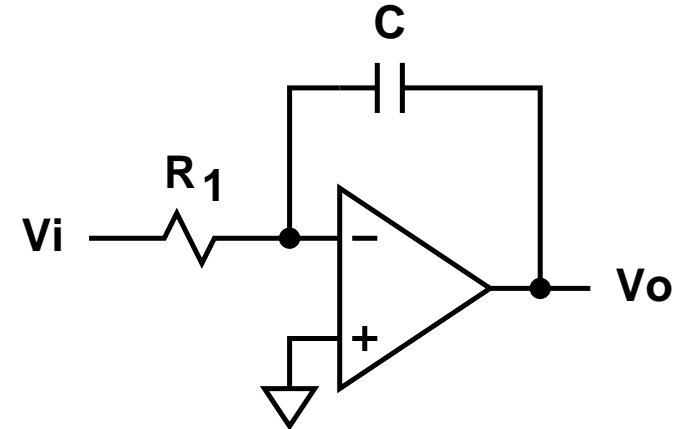
$$A_{CL} \approx -\frac{Z}{Z_1} \cdot (1 - \epsilon_{rr})$$

# Examples of Inverting Configuration

Inverting Amplifier



Inverting Integrator



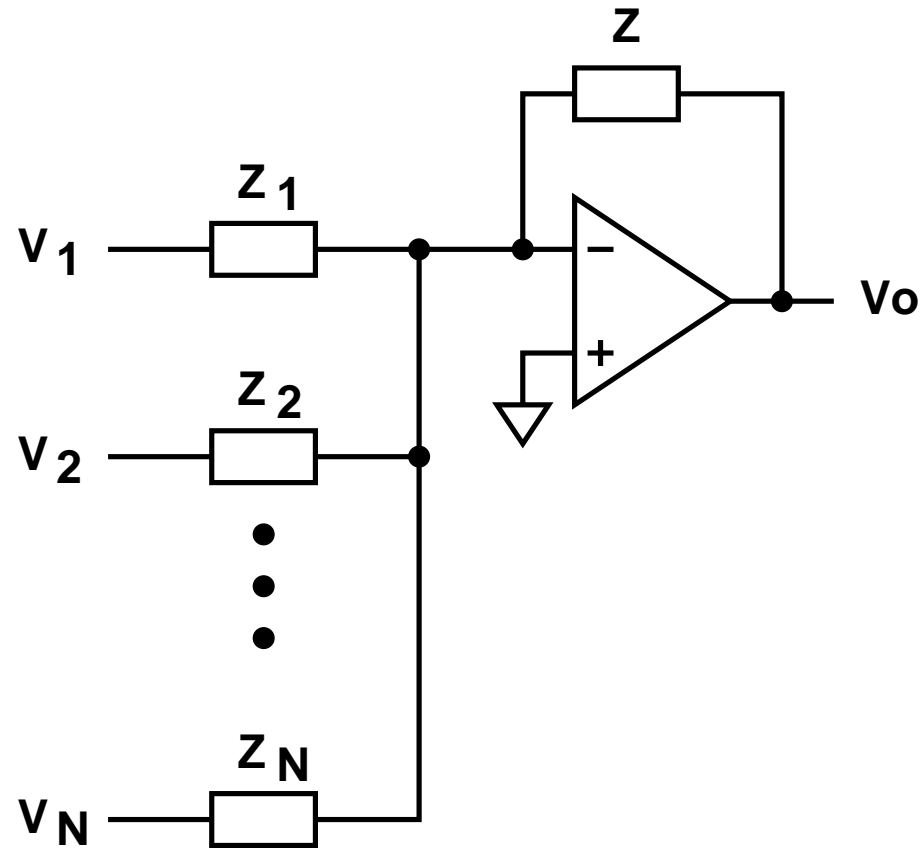
For the inverting amplifier

$$A_{CL} = -\frac{R}{R_1} \left( \frac{1}{1 + \epsilon_{rr}} \right) \quad \epsilon_{rr} = \frac{1}{A} \left( 1 + \frac{R}{R_1} \right)$$

For the inverting integrator

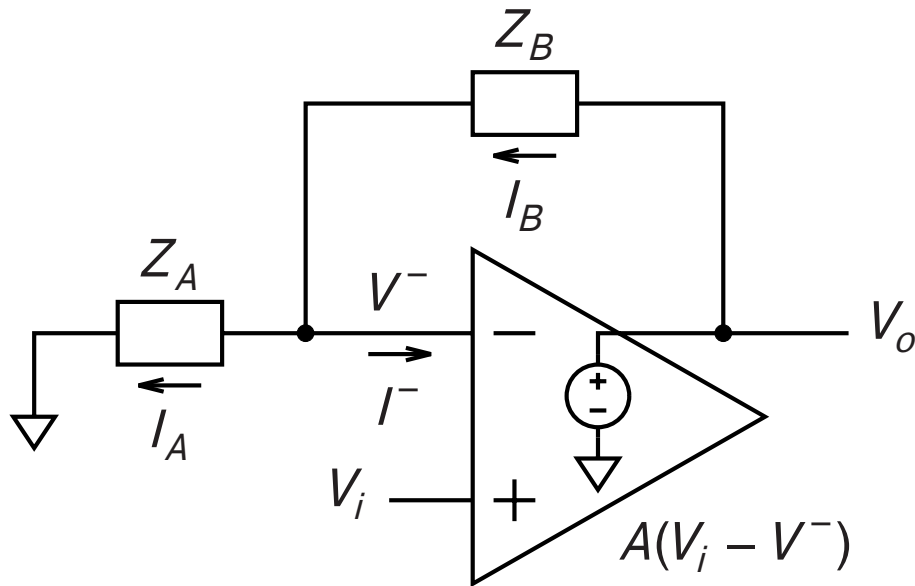
$$A_{CL} = -\frac{1}{sR_1C} \left( \frac{1}{1 + \epsilon_{rr}} \right) \quad \epsilon_{rr} = \frac{1}{A} \left( 1 + \frac{1}{sR_1C} \right)$$

# Inverting Summer Configuration



$$V_o = - \sum_{i=1}^N \left( \frac{Z}{Z_i} V_i \right) \cdot \left[ \frac{1}{1 + \frac{1}{A} \left( 1 + \sum_{i=1}^N \frac{Z}{Z_i} \right)} \right] = - \sum_{i=1}^N \left( \frac{Z}{Z_i} V_i \right) \cdot \left( \frac{1}{1 + \epsilon_{rr}} \right)$$

# Noninverting Configuration



Let  $Z_{in} = \infty$  for the opamp, then

$$I^- = I_B - I_A = \frac{V_o - V^-}{Z_B} - \frac{V^-}{Z_A} = 0$$

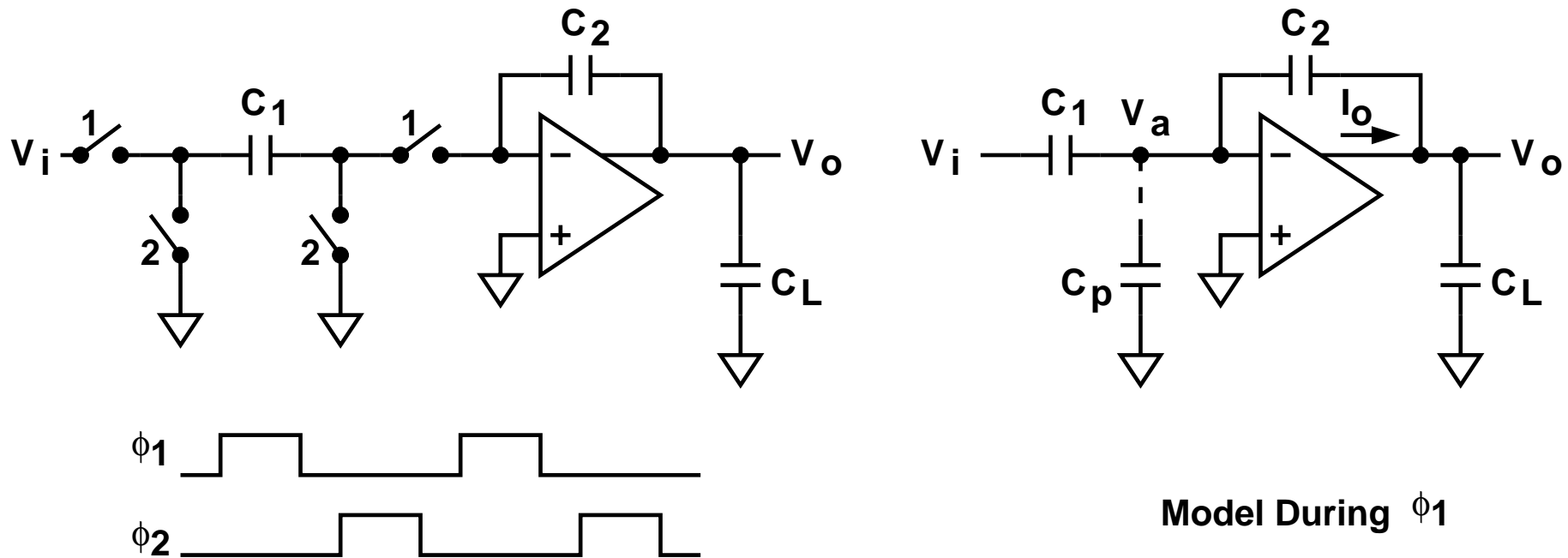
$$V_o = -A \times (V_i - V^-)$$

$$\text{Closed-Loop Gain} = A_{CL} = \frac{V_o}{V_i} = \left(1 + \frac{Z_B}{Z_A}\right) \left[ \frac{1}{1 + \frac{1}{A} \left(1 + \frac{Z_B}{Z_A}\right)} \right] = A_{CL, \infty}(s) \left( \frac{1}{1 + \epsilon_{rr}} \right)$$

$$\text{Input Impedance} = Z_{ic} = Z_i(1 + T) \quad \text{Output Impedance} = Z_{oc} = \frac{Z_o}{1 + T}$$

$$T = \text{Loop Gain} = A \times \frac{Z_A}{Z_A + Z_B}$$

# Switched-Capacitor Applications



For the opamp in closed-loop gain calculation, let  $V_o = -A \times V_a$ .

$$C_1(V_i - V_a) = C_p V_a + C_2(V_a - V_o) \Rightarrow C_1 \left( V_i + \frac{V_o}{A} \right) = -C_p \frac{V_o}{A} - C_2 V_o \left( \frac{1}{A} + 1 \right)$$

$$A_{CL} = \frac{V_o}{V_i} = -\frac{C_1}{C_2} \left[ \frac{1}{1 + \frac{1}{A} \left( \frac{C_1 + C_2 + C_p}{C_2} \right)} \right] = -\frac{C_1}{C_2} \left( \frac{1}{1 + \epsilon_{rr}} \right) \quad \epsilon_{rr} = \frac{1}{A} \left( 1 + \frac{C_1 + C_p}{C_2} \right)$$

# Switched-Capacitor Step Response

---

For the opamp in step response calculation, let  $I_o = -G_m V_a$ .

$$C_1(V_i - V_a) = C_p V_a + C_2(V_a - V_o) \quad I_o = -G_m V_a = sC_2(V_o - V_a) + sC_L V_o$$

$$\Rightarrow A_{CL} = \frac{V_o}{V_i} = -\frac{C_1}{C_2} \left[ \frac{1 - s \cdot \frac{C_2}{G_m}}{1 + s \cdot \frac{(C_1 + C_p)C_2 + (C_1 + C_2 + C_p)C_L}{C_2 G_m}} \right] = -\frac{C_1}{C_2} \left[ \frac{1 - s \cdot \frac{C_2}{G_m}}{1 + s \cdot \tau_a} \right]$$

$$\tau_a = \frac{(C_1 + C_p)C_2 + (C_1 + C_2 + C_p)C_L}{C_2 G_m} = \frac{C_1 + C_2 + C_p}{C_2} \cdot \frac{C_L + [(C_1 + C_p) \parallel C_2]}{G_m}$$

$$\text{Open-Loop Unity-Gain Frequency} = \omega_{u,OL} = \frac{G_m}{C'_L} \quad C'_L = C_L + [(C_1 + C_p) \parallel C_2]$$

$$\text{Feedback Factor} = f = \frac{C_2}{C_1 + C_2 + C_p}$$

$$\text{Closed-Loop } -3 \text{ dB Bandwidth} = \omega_{u,CL} = \omega_{u,OL} \cdot f = \frac{1}{\tau_a}$$

# Switched-Capacitor Step Response

---

The closed-loop step response is

$$V_o(t) = V_{step} \left(1 - e^{-t/\tau_a}\right) \quad \left. \frac{dV_o}{dt} \right|_{t=0} = \frac{V_{step}}{\tau_a}$$

The settling time is

$$t_{settle} = \tau_a \times \ln \left(\frac{1}{\epsilon}\right) \quad \epsilon = 1 - \frac{V_o(t_{settle})}{V_o(\infty)}$$

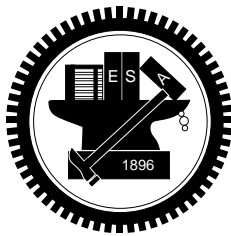
- For  $\epsilon < 0.001$ , require  $t_{settle} > 6.9 \times \tau_a$ .
- Total delay can be estimated by

$$t_d = t_{slew} + t_{settle} = \frac{V_{step}}{SR} + \tau_a \times \ln \left(\frac{1}{\epsilon}\right)$$

# Analog Switches and Sample-and-Hold Circuits

Jieh-Tsorng Wu

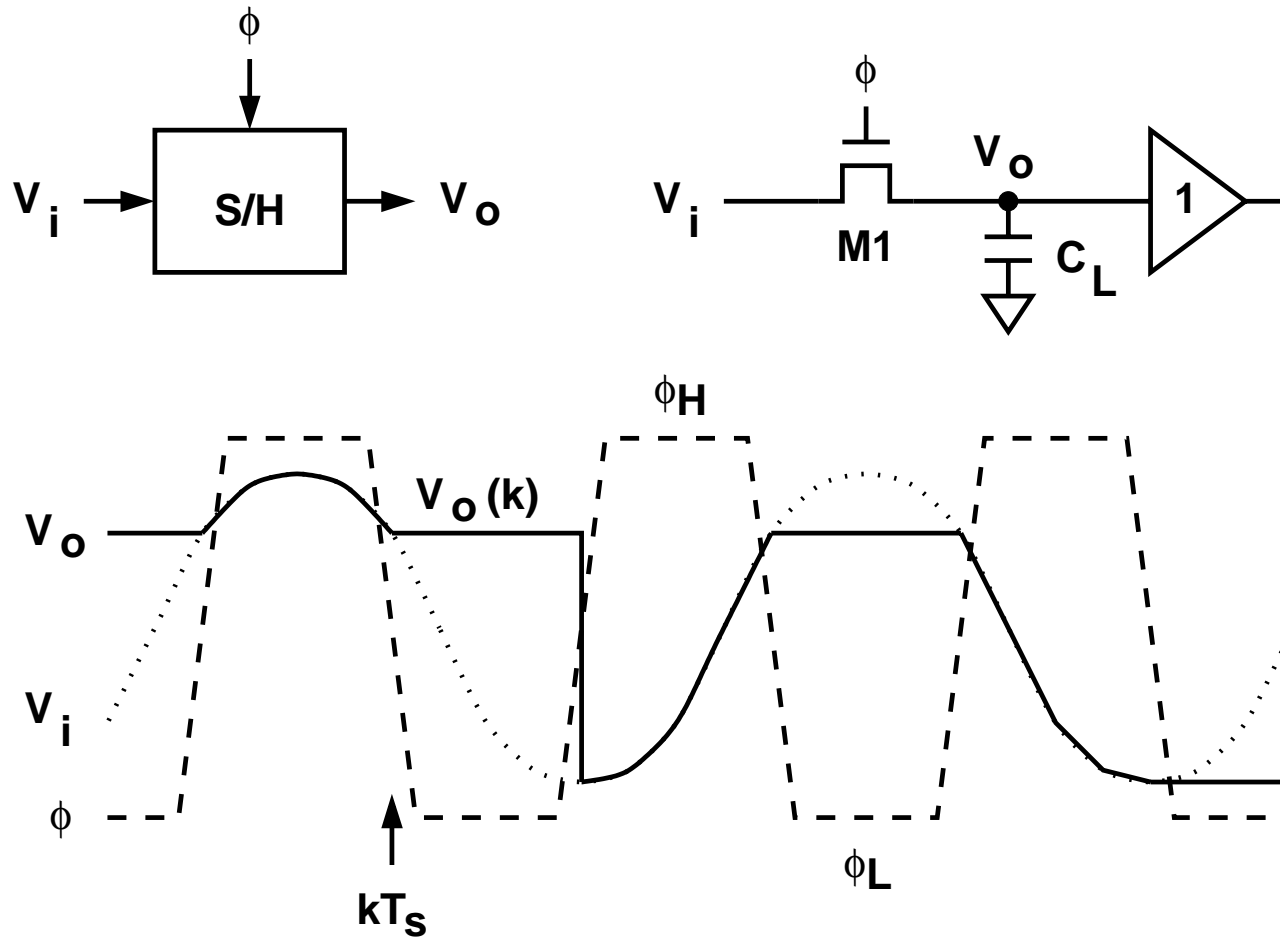
October 8, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Sample-and-Hold (Track-and-Hold) Circuits

Switched-Capacitor S/H



$$V_o(k) = (1 + \epsilon) \times V_i(kT_s + \Delta t) + V_{os}$$

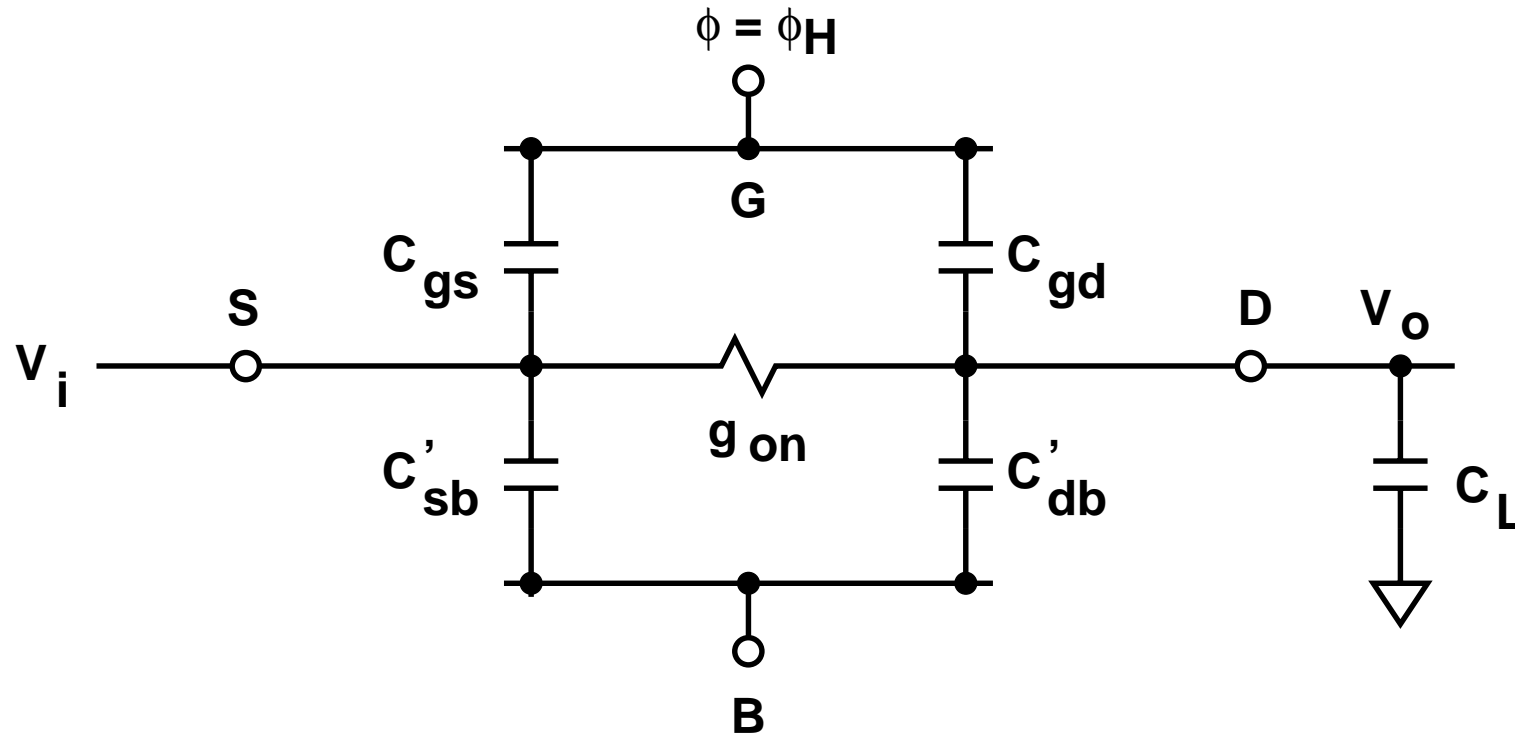
# Sample-and-Hold (Track-and-Hold) Circuits

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Impairments:

- Finite bandwidth in sample mode.
- Acquisition time and hold settling time.
- Aperture jitter  $\Delta t$ .
- Sampling pedestal (Offset  $V_{OS}$  and gain error  $\epsilon$ ).
- Droop in hold mode.
- Feedthrough.
- Thermal Noise.

# MOST Switches in Sample Mode

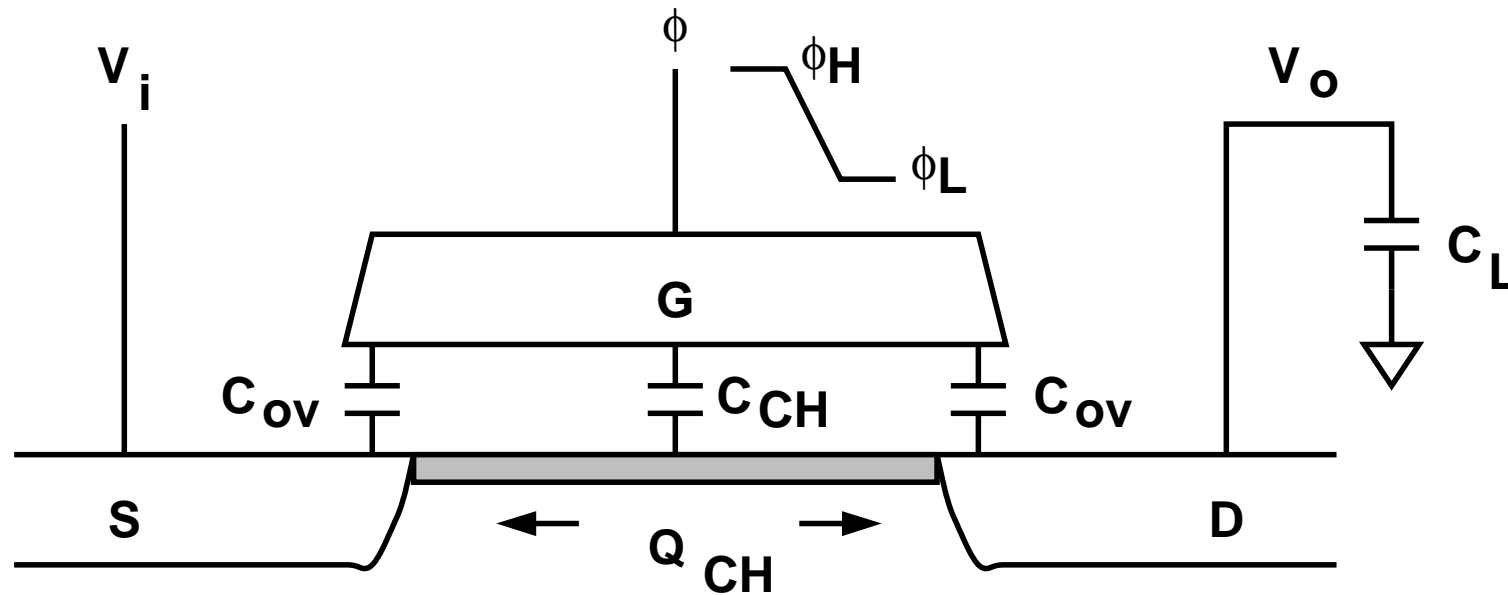


$$g_{on} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_t) = \mu C_{ox} \frac{W}{L} (\phi_H - V_i - V_t)$$

$$C_{gs} = C_{ovs} + \frac{1}{2} W L C_{ox} \quad C_{gd} = C_{ovd} + \frac{1}{2} W L C_{ox}$$

$$C'_{sb} = C_{sb} + \frac{1}{2} W L C_J (V_{SB}) \quad C'_{db} = C_{db} + \frac{1}{2} W L C_J (V_{DB})$$

# MOST Switches from Sample to Hold Mode



$$V_o = V_i + \Delta V = (1 + \epsilon)V_i + V_{OS}$$

- $\Delta V$  is due to switch's *clock feedthrough* and *charge injection*.
- $\Delta V$  depends on the waveform of  $\phi$ .
- Due to the finite slope of  $\phi$ , the exact turn-off time of the switch depends on  $V_i$ .

# Switching Errors in Slow-Gating MOST Switches

---

The body effect of MOSTs can be approximately by

$$V_t = V_{t0} + \gamma \left( \sqrt{V_S + 2\phi_f} - \sqrt{2\phi_f} \right) \approx V_{t0} + (n - 1)V_S$$

- $n$  is a constant, and  $1 < n < 2$ .

For slow gating (slow  $\phi$  fall time),  $\Delta V$  is due to the clock feedthrough *after* the switch is turned off.

$$\Delta V = -\frac{C_{ov}}{C_{ov} + C_L}(V_i + V_t - \phi_L) = -\frac{C_{ov}}{C_{ov} + C_L}(nV_i + V_{t0} - \phi_L) = \epsilon V_i + V_{OS}$$
$$\Rightarrow \quad \epsilon = -n \cdot \frac{C_{ov}}{C_{ov} + C_L} \quad V_{OS} = -(V_{t0} - \phi_L) \cdot \frac{C_{ov}}{C_{ov} + C_L}$$

# Switching Errors in Fast-Gating MOST Switches

---

For fast gating (fast  $\phi$  fall time), assuming the channel charge  $Q_{CH}$  is divided equally between input and output, then

$$\Delta V = -(\phi_H - \phi_L) \frac{C_{ov}}{C_{ov} + C_L} + \frac{1}{2} Q_{CH} \frac{1}{C_{ov} + C_L} = \epsilon V_i + V_{OS}$$

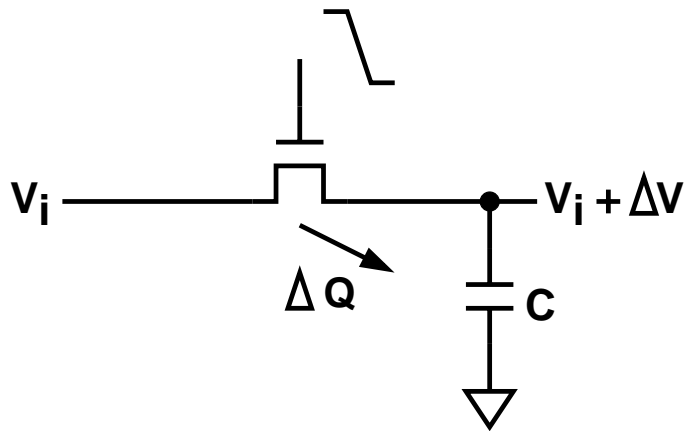
$$Q_{CH} = -C_{CH} \cdot [(\phi_H - V_i) - V_t] = -C_{CH} \cdot (-nV_i + \phi_H - V_{t0})$$

$$C_{CH} = C_{ox} \cdot W(L - 2L_D)$$

$$\Rightarrow \quad \epsilon = +\frac{n}{2} \cdot \frac{C_{CH}}{C_{ov} + C_L} \quad V_{OS} = -(\phi_H - \phi_L) \frac{C_{ov}}{C_{ov} + C_L} - \frac{1}{2} (\phi_H - V_{t0}) \frac{C_{CH}}{C_{ov} + C_L}$$

- In practice,  $\epsilon$  and  $V_{OS}$  decrease with increasing fall time of  $\phi$ .
- The body effect of  $V_t$  can cause nonlinearity.

# MOST S/H Speed-Precision Tradeoff



$$\text{On Conductance} = g_{on} = \mu C_{ox} \frac{W}{L} V_{ov}$$

$$\text{Charge Injection} = \Delta Q = \alpha \cdot Q$$

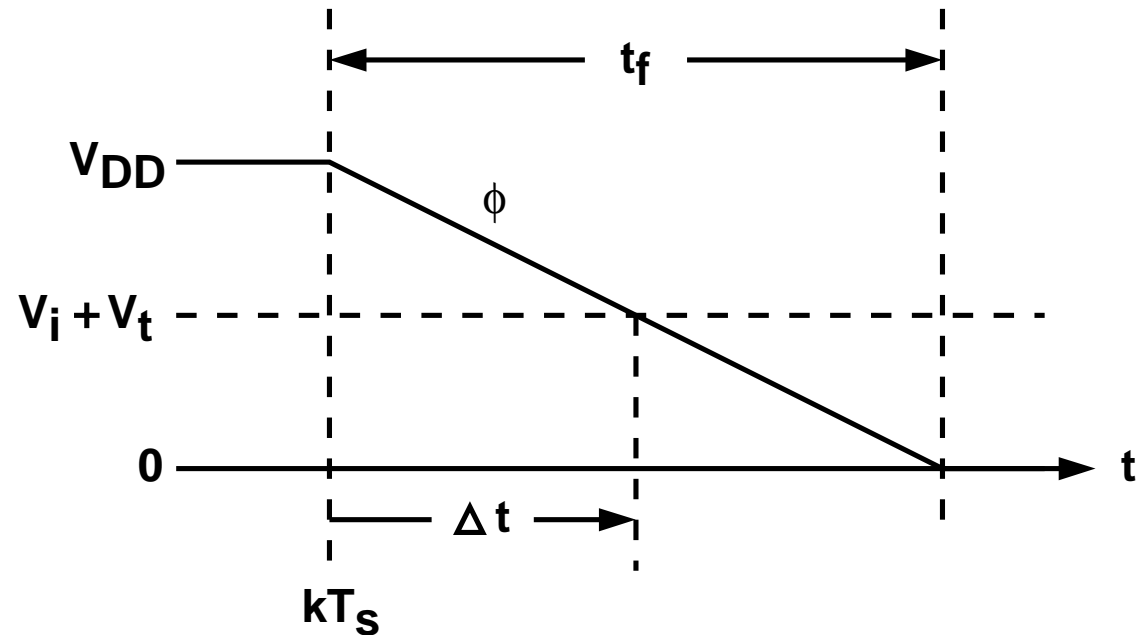
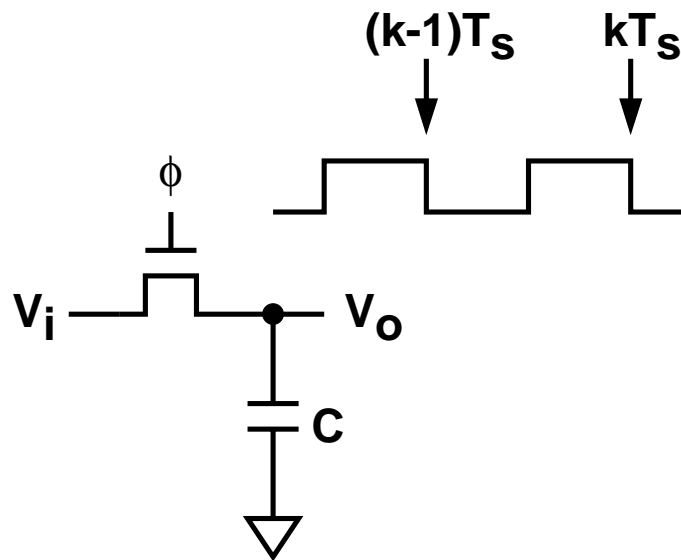
$$Q = C_{ox} W L V_{ov} = g_{on} \cdot \frac{L^2}{\mu}$$

$$\text{Time Constant in Sampling Mode} = \tau_{on} = \frac{C}{g_{on}}$$

$$\text{Absolute Voltage Error} = \Delta V = \frac{\Delta Q}{C} = \frac{\alpha L^2}{\mu \tau_{on}} \quad \text{Relative Voltage Error} = \frac{\Delta V}{V_i} = \frac{\alpha L^2}{\mu \tau_{on} V_{DD}}$$

- Want  $T_{s,on} > 7\tau_{on}$  for a 0.1% settling accuracy, where  $T_{s,on}$  is the sampling time.
- $\alpha$  can be reduced by compensation.
- Relative error  $\Delta V/V_i$  is increased when reducing  $V_{DD}$ .

# Aperture Jitter Due to the Finite Falling Time

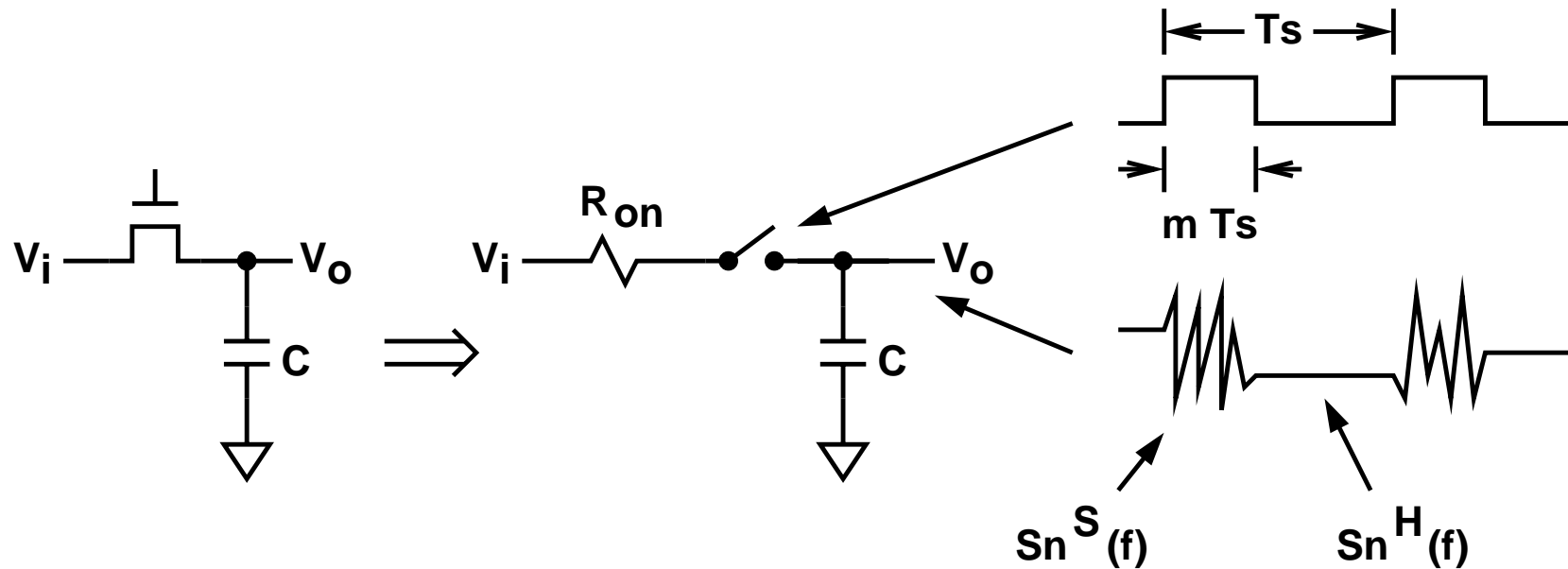


$$\Delta t = t_f \times \frac{V_{DD} - (V_i + V_t)}{V_{DD}}$$

$$0 \leq \Delta t \leq t_f \left( 1 - \frac{V_{t0}}{V_{DD}} \right)$$

- The jitter is input dependent, and introduces noise at output.

# Thermal Noise in MOST S/H



During sampling mode, the *two-sided* noise PSD at  $V_o$  is

$$S_n^S(f) = S_n(f) = \frac{1}{2} \cdot 4kTR_{on} \cdot |H(j2\pi f)|^2 = \frac{1}{2} \cdot \frac{4kTR_{on}}{1 + (2\pi f R_{on} C)^2} \quad B_n = \frac{1}{4R_{on} C}$$

- For sampling rate  $f_s = 1/T_s$ , want

$$T_{s,on} = m \cdot T_s > 7 \cdot R_{on} C \quad \Rightarrow \quad B_n > \frac{7}{4} \cdot \frac{1}{m} \cdot f_s \quad \text{or} \quad B_n \geq 5f_s$$

## Thermal Noise in MOST S/H

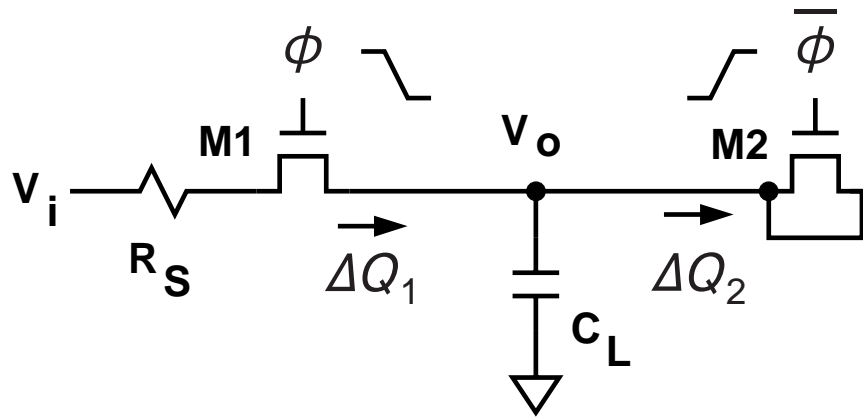
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During the hold mode, the noise is sampled and the noise PSD is

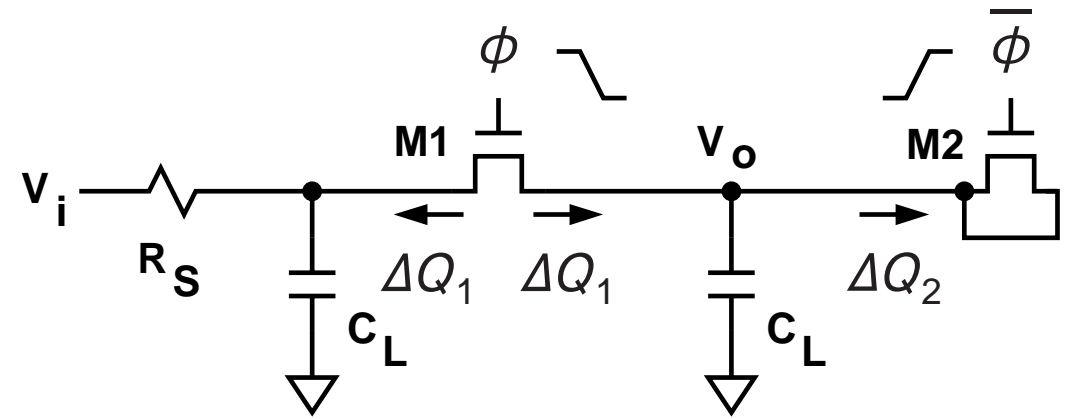
$$S_n^H(f) = \sum_{i=-\infty}^{\infty} S_n(f - i \cdot f_s) \approx \frac{2B_n}{f_s} \times S_n(f) \approx \frac{1/(2R_{on}C)}{f_s} \times 2kTR_{on} = \frac{kT}{C} \cdot \frac{1}{f_s}$$

- It is assumed that  $B_n \gg f_s$ .
- The total noise power in the baseband  $-f_s/2 \leq f \leq f_s/2$  is hence  $kT/C$ .
- Want large  $C$  for low-noise performance.
- Reference: Roubik Gregorian and Gabor Temes, “*Analog MOS Integrated Circuits for Signal Processing*,” John Wiley & Sons, Inc., 1986.

# Charge Compensation for MOST Switches



Dummy Switch



Dummy Switch with Equalizing Capacitor

Design the M2 dummy switch so that

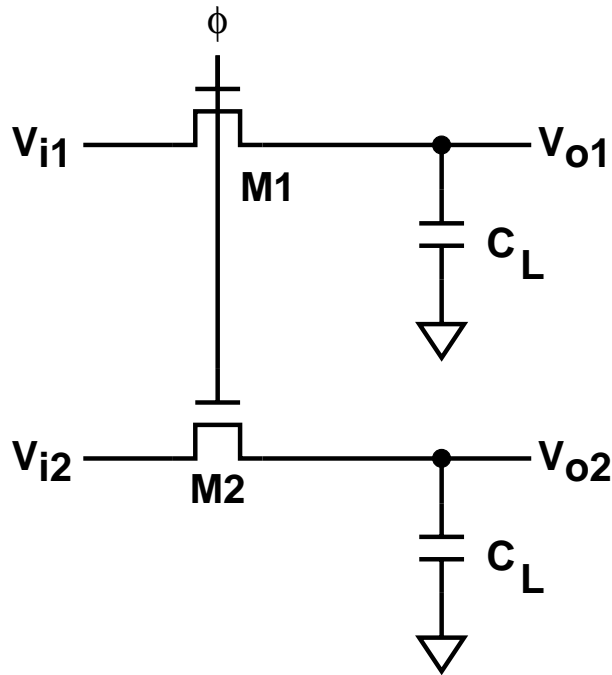
$$L_2 = L_1 \quad W_2 = \frac{1}{2}W_1$$

Then

$$\Delta Q_1 = \Delta Q_{ov1} + \alpha \Delta Q_{CH1} \quad \Delta Q_2 = \Delta Q_{ov1} + \frac{1}{2} \Delta Q_{CH1}$$

- The problem is that  $\alpha$  is not exactly 1/2.

# Differential Sampling



$$V_{o1} - V_{o2} = [V_{i1}(1 + \epsilon_1) + V_{OS1}] - [V_{i2}(1 + \epsilon_2) + V_{OS2}]$$

$$= (V_{i1} - V_{i2})[1 + \epsilon_D] + (V_{i1} + V_{i2})\epsilon_C + V_{OS}$$

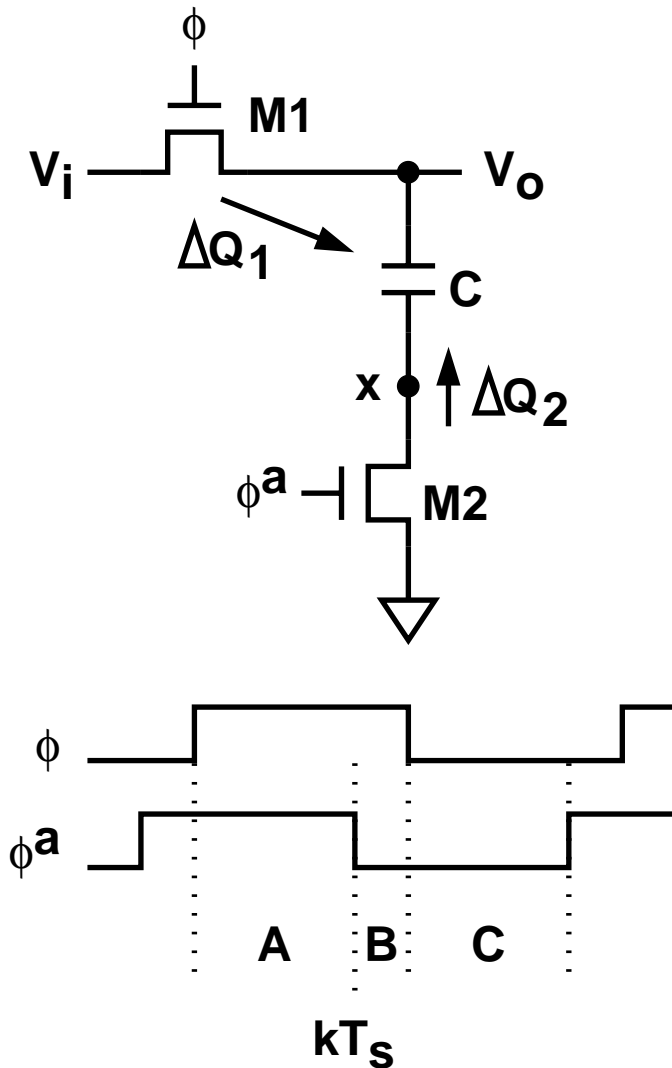
$$\epsilon_D = \frac{\epsilon_1 + \epsilon_2}{2} = \text{Differential-Mode Gain Error}$$

$$\epsilon_C = \frac{\epsilon_1 - \epsilon_2}{2} = \text{Common-Mode Gain Error}$$

$$V_{OS} = V_{OS1} - V_{OS2} = \text{Offset}$$

- The switching errors of M1 and M2 at  $V_{o1}$  and  $V_{o2}$  are to the first order equal and hence appear as a common-mode component at the output.
- Good CMRR and PSRR. Less sensitive to  $\phi$  waveform.
- The body effect can cause  $\epsilon_C \neq 0$  as well as nonlinearity.

# Bottom-Plate Sampling



The charge in  $C$  can be expressed as

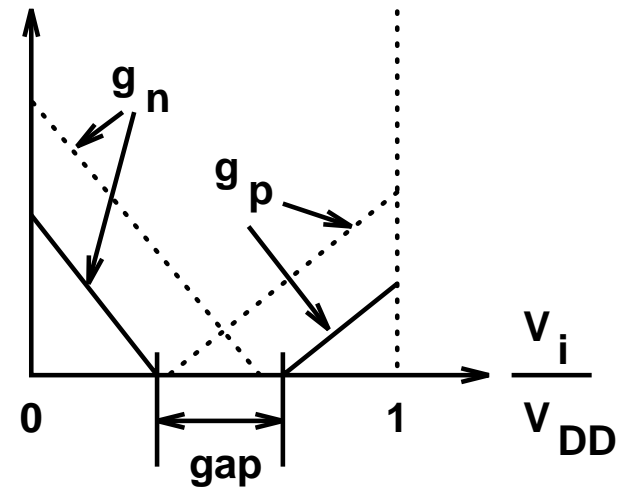
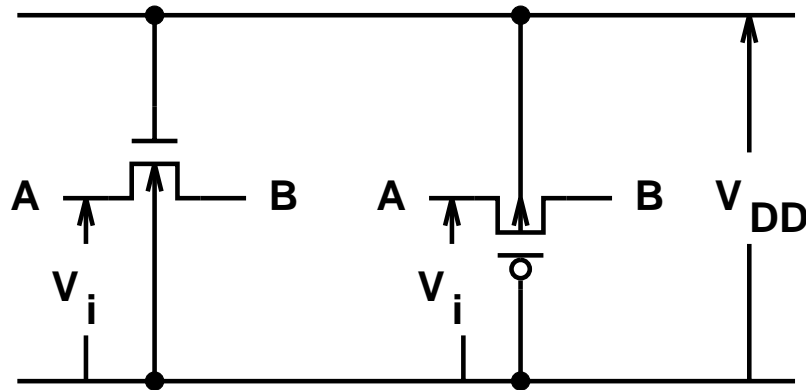
$$Q_C(A) = C \cdot V_i(t)$$

$$Q_C(B) = C \cdot V_i(kT_s) - \Delta Q_2$$

$$Q_C(C) = C \cdot V_i(kT_s) - \Delta Q_2 + \Delta Q_1 \approx C \cdot V_i(kT_s) - \Delta Q_2$$

- The switching charge  $\Delta Q_2$  is independent of  $V_i$ , and contains little noise due to aperture jitter.
- Since node  $x$  is floating during period B and C, the switching charge  $\Delta Q_1 \approx 0$ .
- Parasitic capacitance from node  $x$  to ground can enhance  $\Delta Q_1$ .

# Complementary Analog Switches



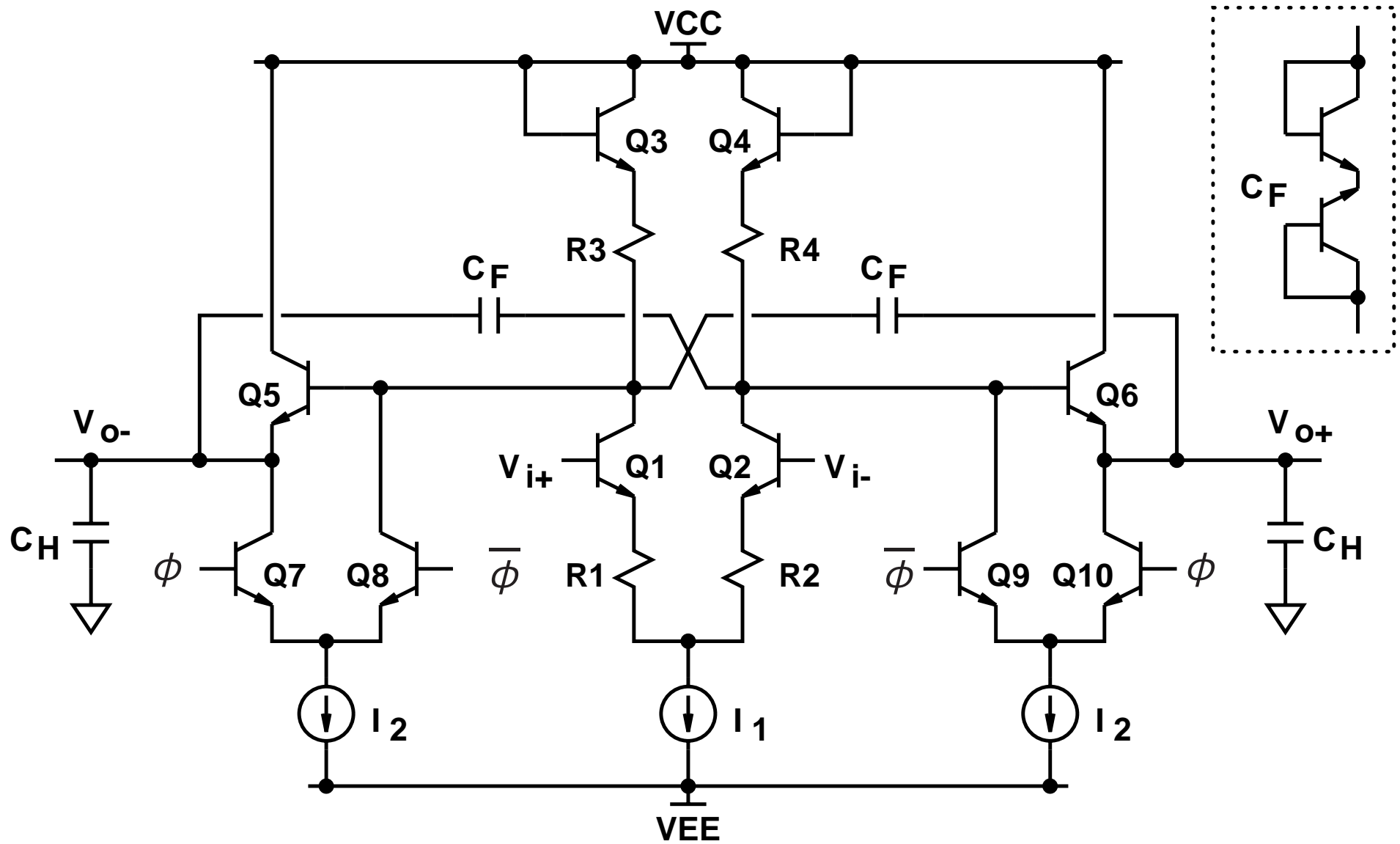
$$g_{on} = \mu C_{ox} \frac{W}{L} (V_g - V_s - V_t) = \beta (V_g - V_{t0} - nV_s) \quad \beta = \mu C_{ox} \frac{W}{L} \quad V_t = V_{t0} + (n-1)V_s$$

$$g_n = \beta_n [V_{DD} - V_{t0,n} - n_n V_i] \quad g_p = \beta_p [V_{DD} - V_{t0,p} - n_p (V_{DD} - V_i)]$$

$$V_{DD(min)} = \frac{n_n V_{t0,p} + n_p V_{t0,n}}{n_n + n_p - n_n n_p} \quad V_{DD(min)} = \frac{2V_{t0}}{2-n} \quad \text{if } n_n = n_p \text{ and } V_{t0,n} = V_{t0,p}$$

- If  $V_{DD} > V_{DD(min)}$ , no gap between  $g_n$  and  $g_p$  curves, thus conduction for any  $V_i$  is possible by parallel connection of nMOST and pMOST.

# A Differential BJT Sampling Switch



# A Differential BJT Sampling Switch

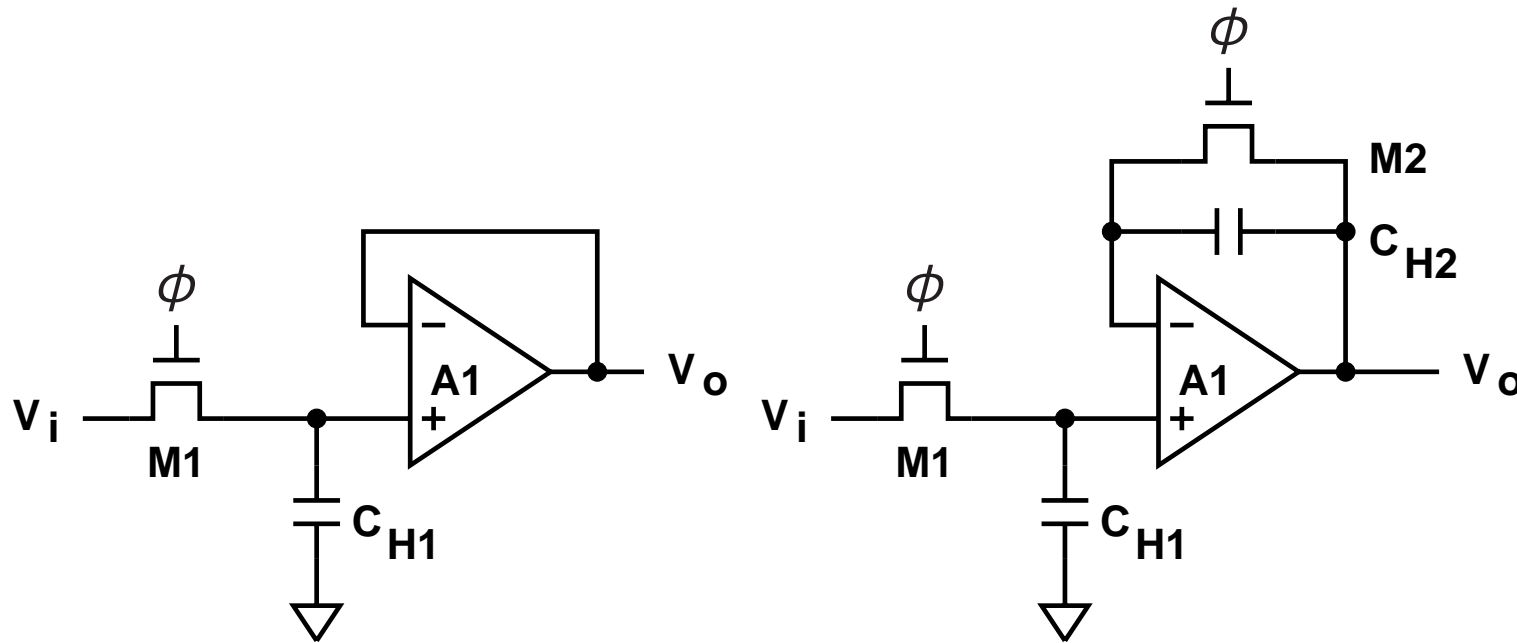
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- The nonlinearities of Q1 and Q2 are canceled by Q3 and Q4.
- The differential operation results in only odd harmonics introduced by the Q5 and Q6 followers.
- During hold mode ( $\phi = 0$ ), Q5 and Q6 are in cut-off region, the feedthrough gain is

$$A_H(\text{Without } C_F) \approx \frac{C_{je5}}{C_L + C_{je5}} \quad A_H(\text{With } C_F) \approx \frac{C_{je5}}{C_L + C_{je5}} \left( 1 - \frac{C_F}{C_{je5}} \right)$$

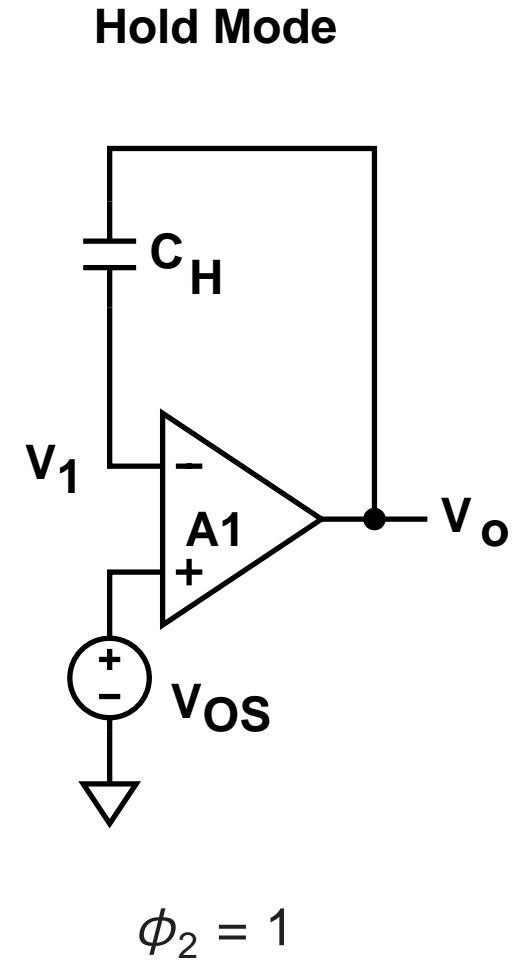
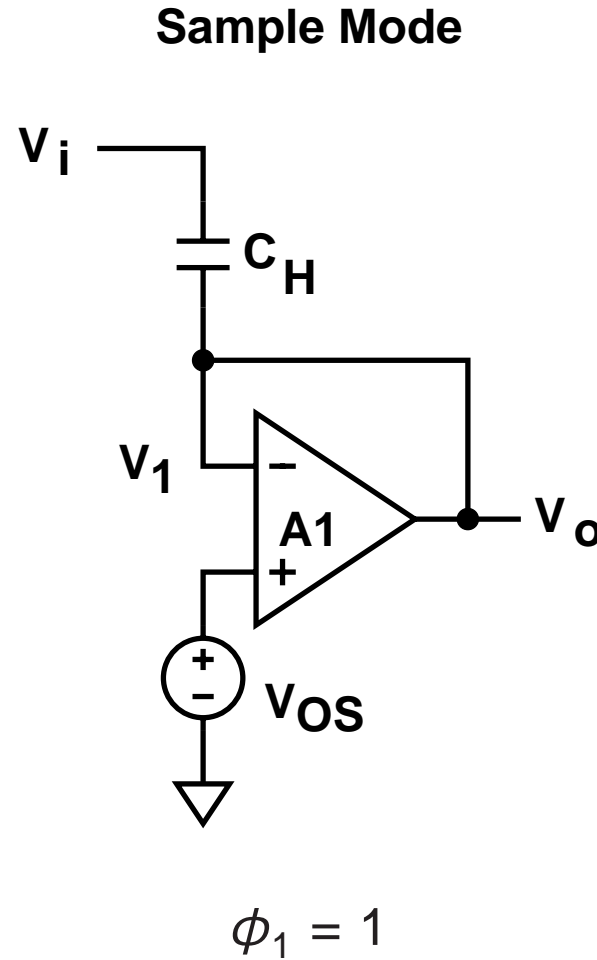
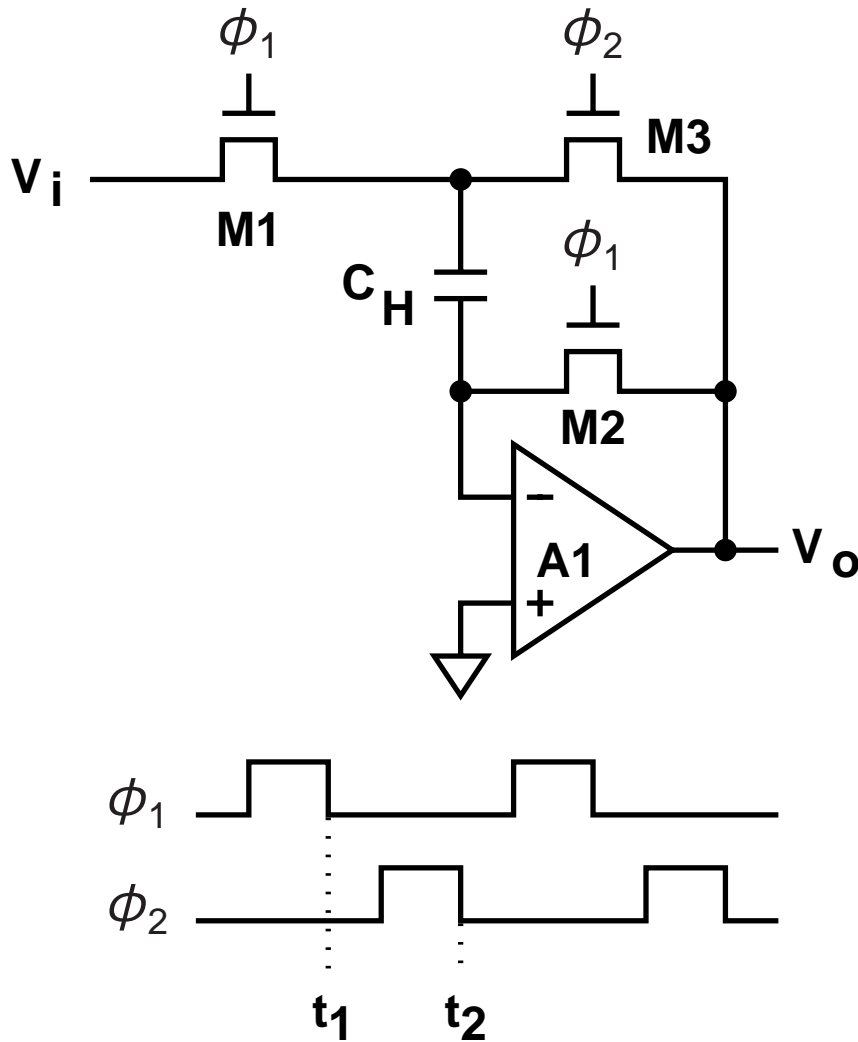
- Reference: P. Vorenkamp, et al., *Fully Bipolar 120 MS/s 10-b Track-and-Hold Circuit*, JSSC 7/92, pp. 988–992.

# Open-Loop MOST S/H



- M2 and  $C_{H2}$  are used to compensate for the switching error of M1.
- The  $V_{OS}$  of the opamp is shown in  $V_o$ .
- The aperture jitter can be reduced by having clock signals that change above and below  $V_i$  by fixed amounts.

# MOST S/H Using Miller Holding Capacitor



# MOST S/H Using Miller Holding Capacitor

---

To consider the  $V_{OS}$  effect, let  $A_1 = \infty$  and  $V_i = 0$ , then

$$V_o(t_1) = V_{OS}(t_1) \qquad V_o(t_2) = V_{OS}(t_2) - V_{OS}(t_1)$$

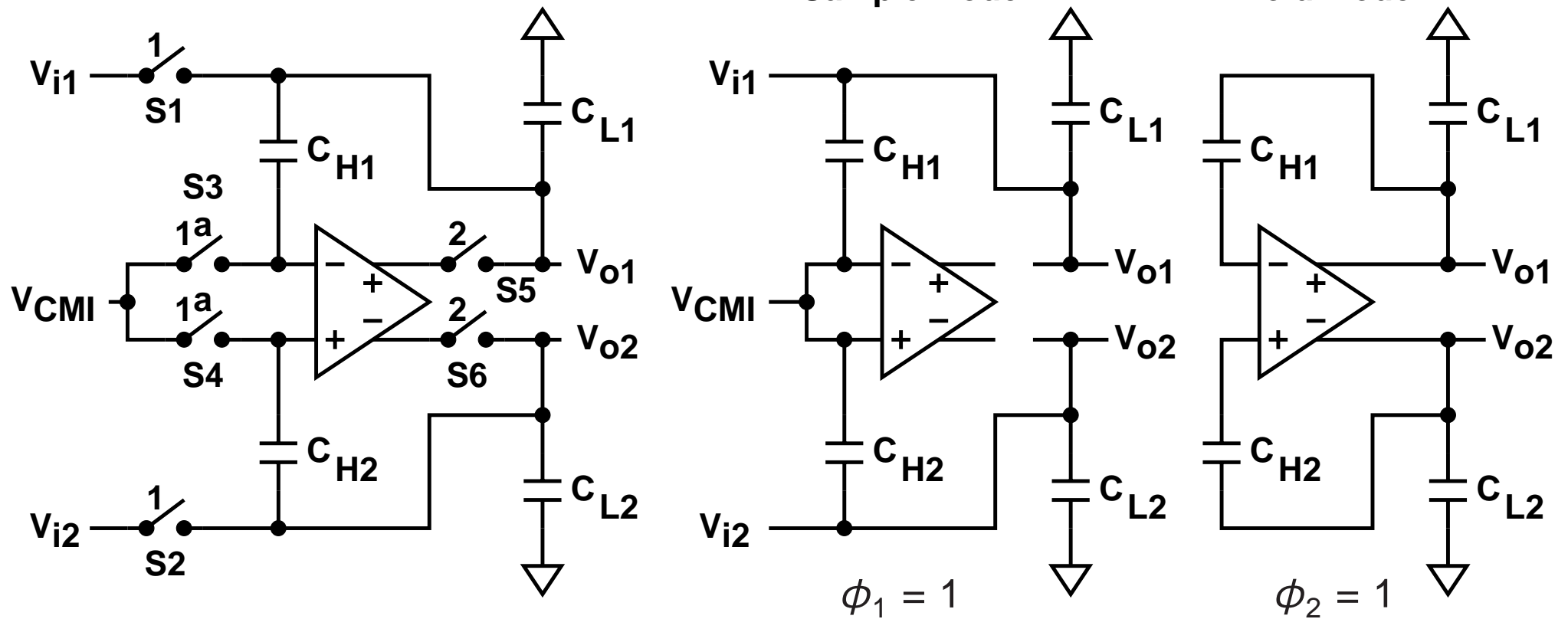
- The  $V_{OS}$  is sampled in the sample mode, and canceled in the hold mode.

To consider the finite gain effect, let  $V_{OS} = 0$ , then during the hold mode,

$$V_o - V_1 = V_i \quad V_o = -A_1 V_1 \quad \Rightarrow \quad V_o = \frac{V_i}{1 + \frac{1}{A_1}} \approx V_i \cdot \left(1 - \frac{1}{A_1}\right)$$

- The  $V_o$  is reset to ground in sample mode. High slew-rate opamp is required.
- The virtual ground is not ideal at high frequencies in the sample mode.
- The switching errors are concerns.

# MOST S/H Using Miller Capacitor and Bottom-Plate Sampling

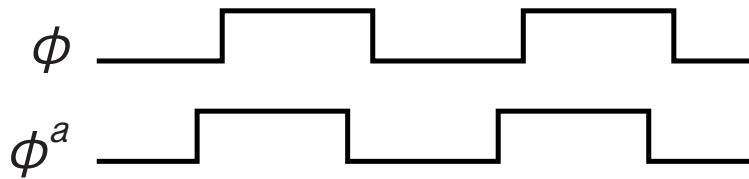
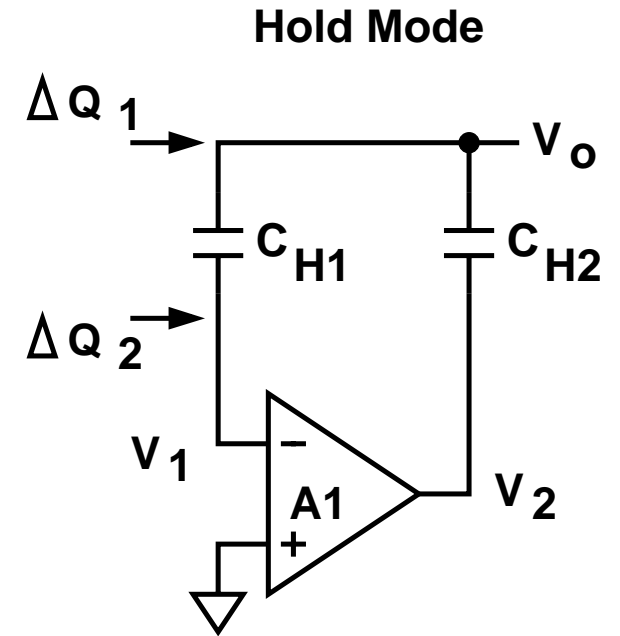
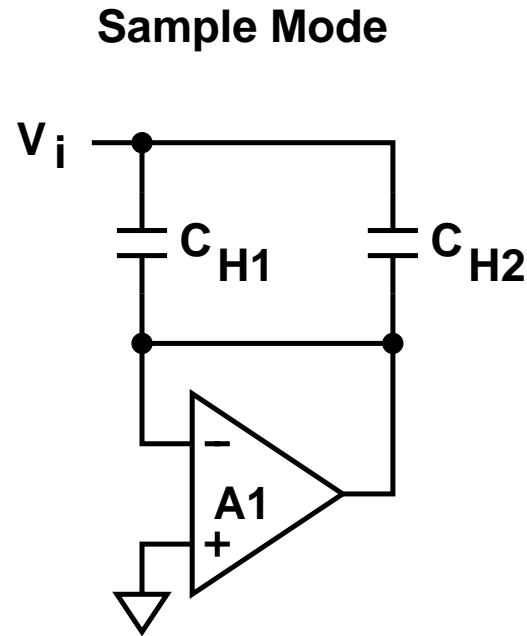
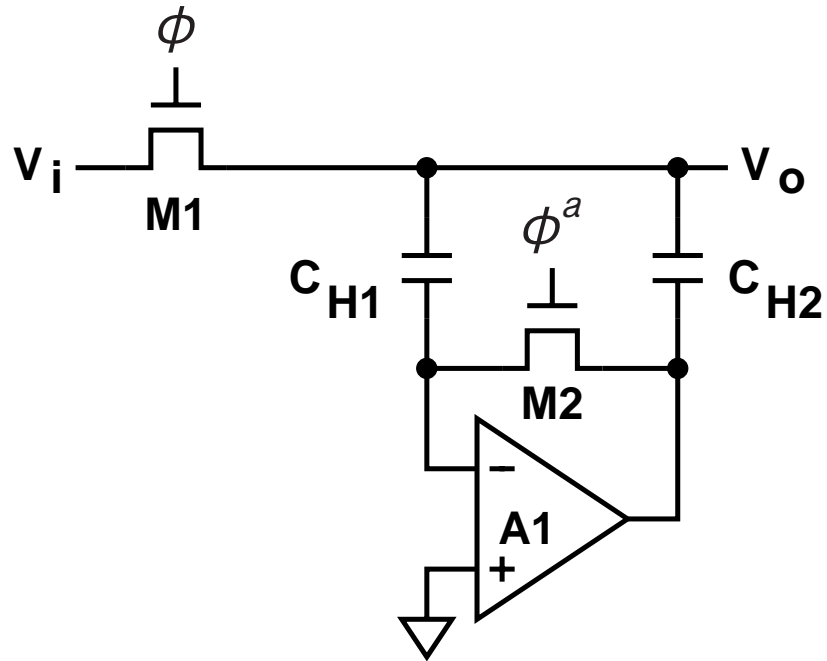


# MOST S/H Using Miller Capacitor and Bottom-Plate Sampling

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- The opamp is open-loop during the sample mode. Glitches can occur during the transition from the sample mode to the hold mode.
- $V_{OS}$  of the opamp is not canceled.
- The outputs,  $V_{o1}$  and  $V_{o2}$ , are precharged to  $V_{i1}$  and  $V_{i2}$  during the sample mode, so that the settling time in the hold mode can be reduced.
- The input common-mode voltage,  $V_{CMI}$ , can be different from the value of  $(V_{i1} + V_{i2})/2$ .
- The  $V_{CMO}$  of the opamp's CMFB should closely follow the value of  $(V_{i1} + V_{i2})/2$ .
- The mismatches of the switching errors of S3–S8 can introduce a constant offset voltage in the outputs.

# MOST S/H Using Double Miller Capacitors



$\phi = 1$

$\phi = 0$

## MOST S/H Using Double Miller Capacitors

---

Let  $\Delta Q_2$  be the charge injecting to  $V_1$  when M2 turns off. Then

$$\begin{aligned} \Delta Q_2 &= C_{H1}(\Delta V_1 - \Delta V_o) & \Delta V_o \approx \Delta V_2 &= -A_1 \Delta V_1 \\ \Rightarrow \Delta V_1 &= \frac{1}{1 + A_1} \cdot \frac{\Delta Q_2}{C_{H1}} & \Delta V_o &= -\frac{A_1}{1 + A_1} \cdot \frac{\Delta Q_2}{C_{H1}} \end{aligned}$$

- $\Delta Q_2$  is independent of  $V_i$ .

Let  $\Delta Q_1$  be the charge injecting to  $V_o$  when M1 turns off. Then

$$\begin{aligned} \Delta Q_1 &= C_{H1}(\Delta V_o - \Delta V_1) + C_{H2}(\Delta V_o - \Delta V_2) & \Delta V_1 \approx \Delta V_o & & \Delta V_2 = -A_1 \Delta V_1 \approx -A_1 \Delta V_o \\ \Rightarrow \Delta V_o &= \frac{1}{1 + A_1} \cdot \frac{\Delta Q_1}{C_{H2}} \end{aligned}$$

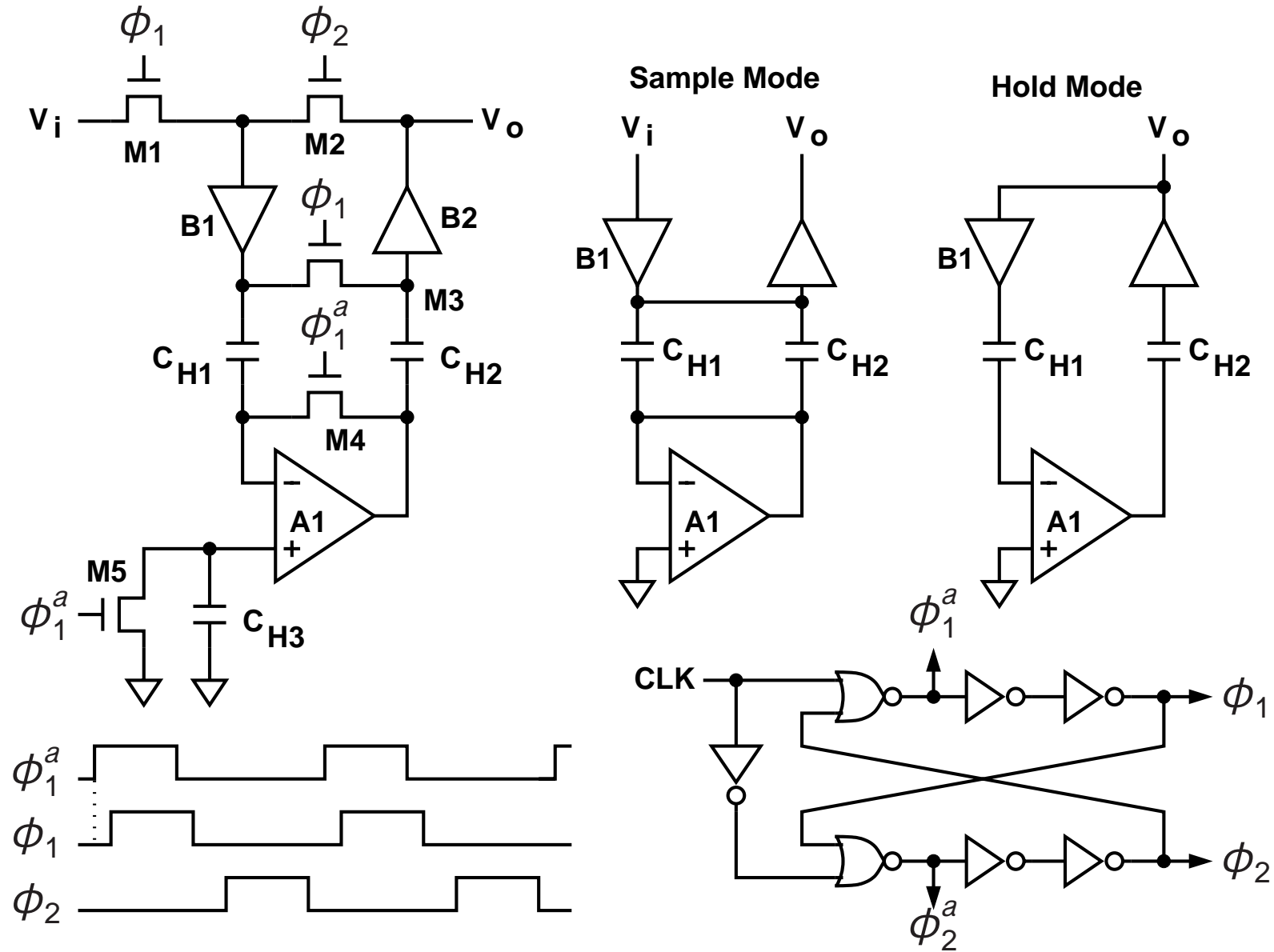
- Small  $C_{H1}$  and  $C_{H2}$  can be used.

# MOST S/H Using Double Miller Capacitors

---

- The  $V_{OS}$  is sampled in the sample mode, and canceled in the hold mode.
- The opamp's output has small voltage variation. Thus, it is easier to design the opamp for high speed.
- Suitable for high speed.

# A MOST Recycling S/H



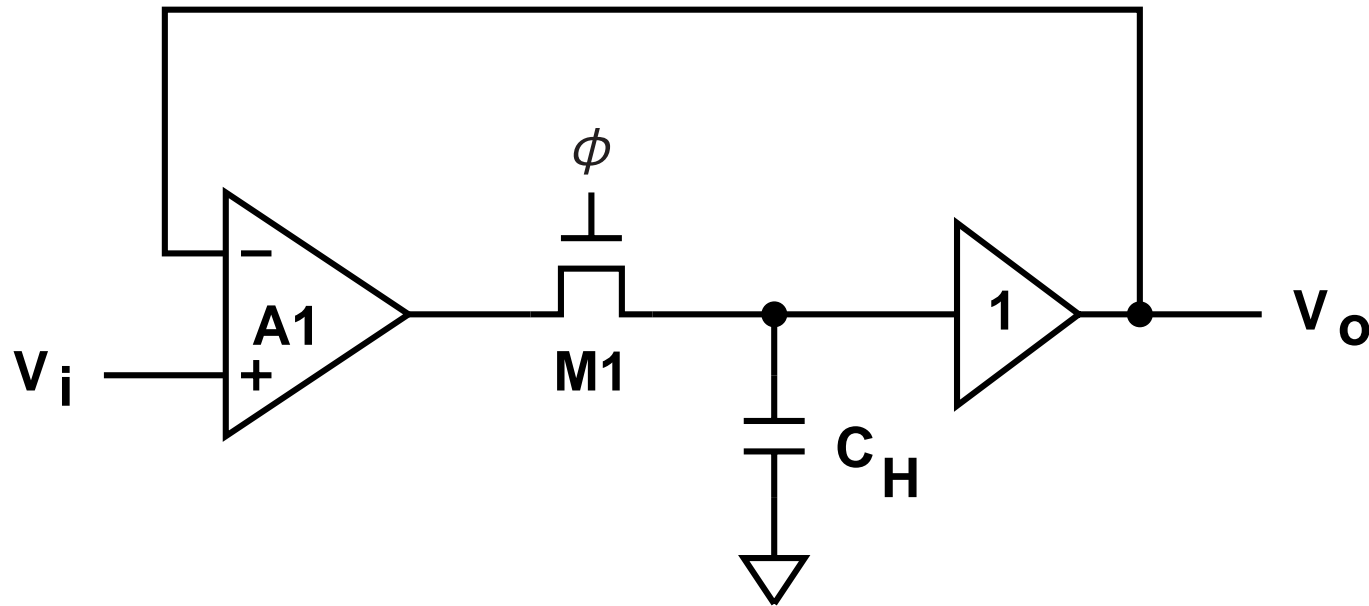
## A MOST Recycling S/H

---

- B1 and B2 are two unity-gain buffer.
- M5 and  $C_{H3}$  is to compensate for the M4's switching error.
- The switching errors of M1 and M2 does not affect  $V_o$ .
- The switching error of M3 does affect  $V_o$ . But its effect is reduced by the opamp's voltage gain.
- Mismatch between B1 and B2 can affect  $V_o$ .

# Closed-Loop S/H

---

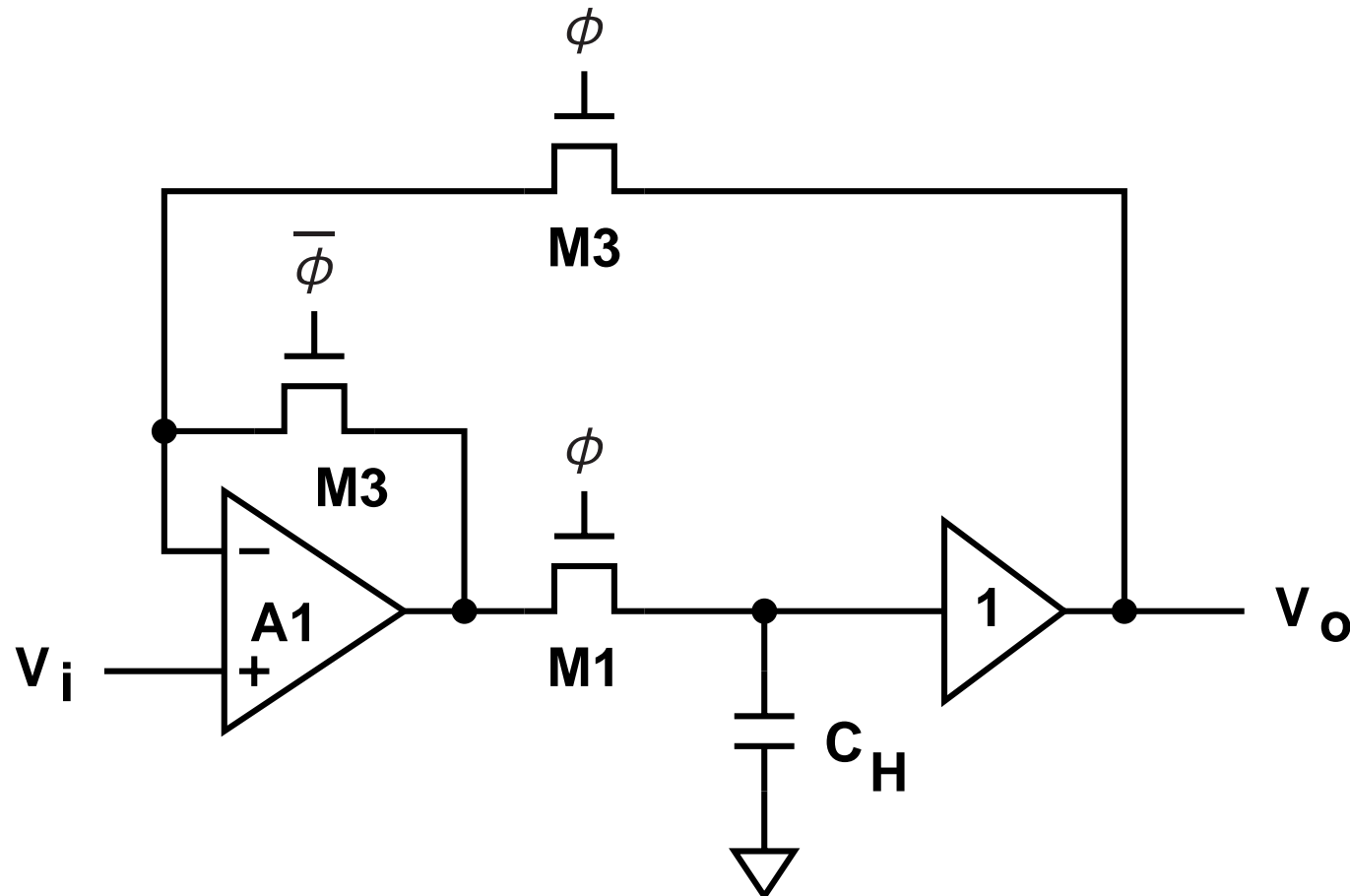


## Closed-Loop S/H

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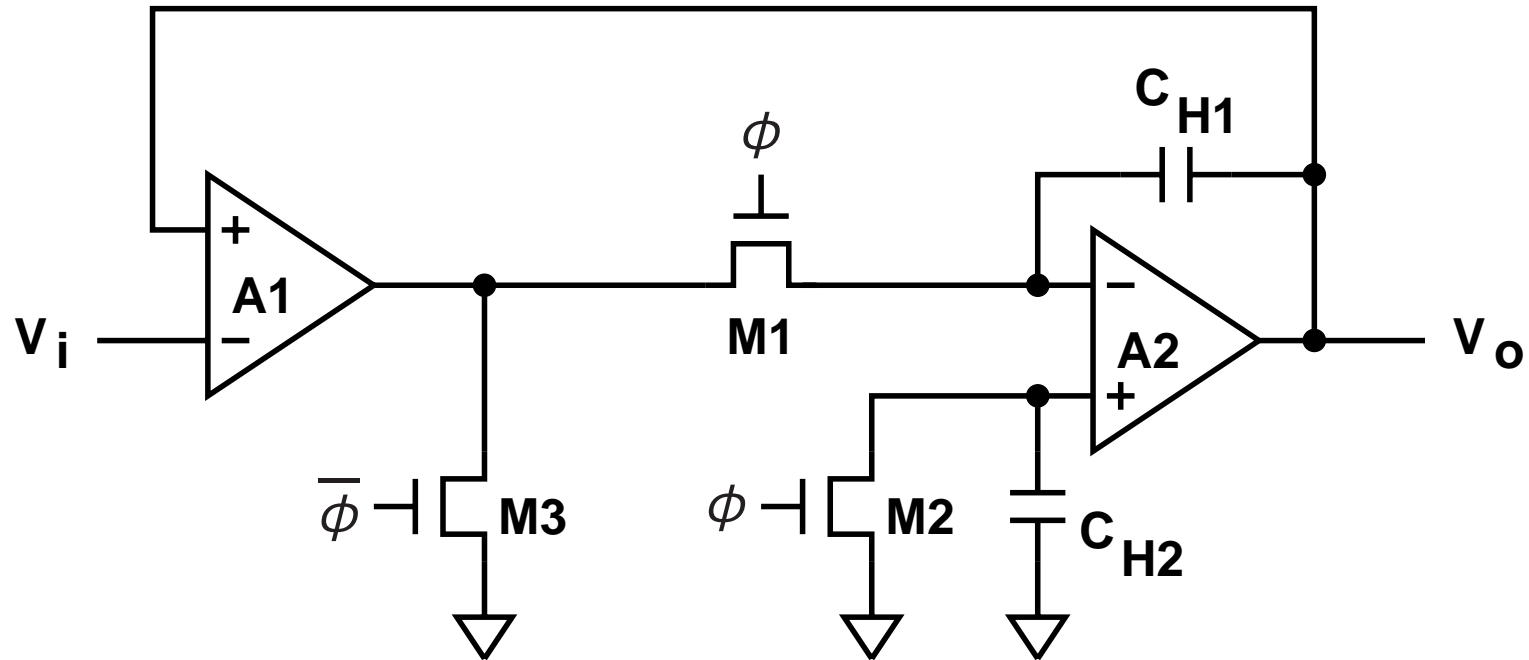
- The circuit is in the track mode when  $\phi = 1$ , and is in the hold mode when  $\phi = 0$ .
- High input impedance.
- The offset and gain of the output buffer are not critical.
- The input offset of the A1 opamp is not canceled.
- The speed can be seriously degraded due to the necessity of guaranteeing that the loop is stable in the track mode.
- The A1 opamp is open loop when in the hold mode. It takes time to recover the bias when switches to the track mode.

## Closed-Loop S/H with Improved $t_{\text{slew}}$



- During hold mode, A1 is configured as a unity-gain amplifier. Thus, the slewing time is greatly minimized.

# Closed-Loop S/H Using Active Integrator

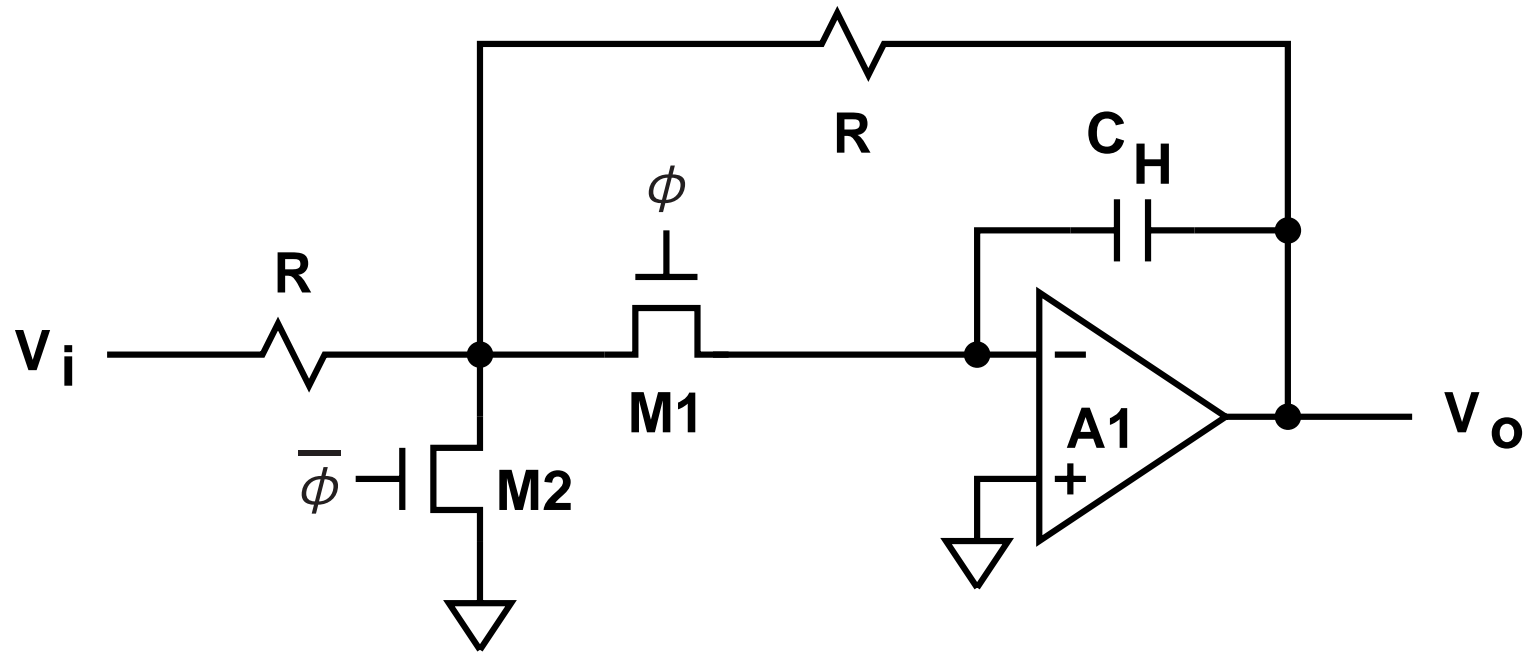


## Closed-Loop S/H Using Active Integrator

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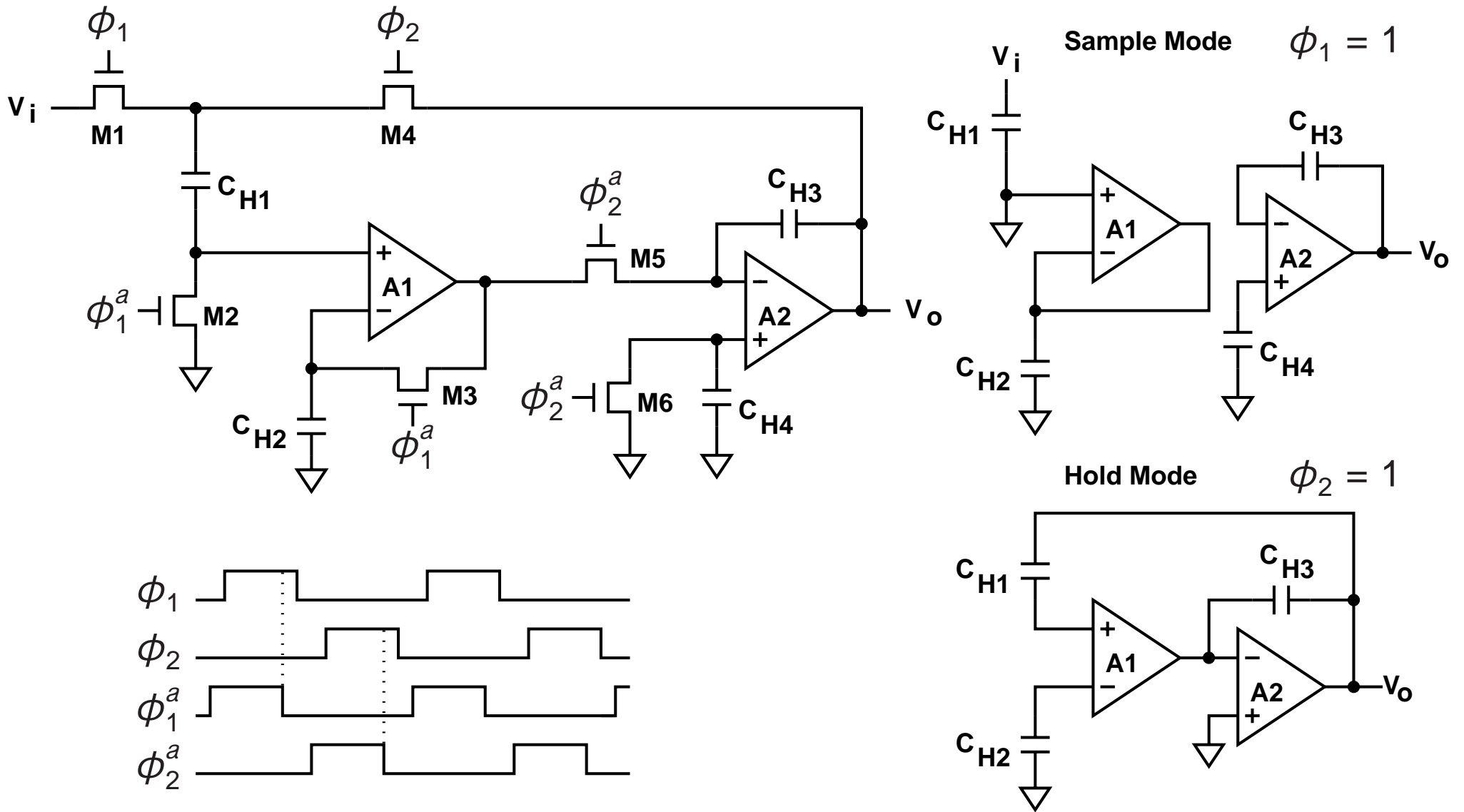
- When in the track mode, the voltage on both sides of M1 are closed to ground, and are nearly signal independent.
- Aperture jitter is minimized.
- The switching error of M1 causes a dc offset in  $V_o$ , which will be signal independent.
- M2 and  $C_{H2}$  are to compensate for the M1 switching error.
- When in the hold mode, M3 clamps the A1's output to ground, speeding up the time it takes the S/H to return to the track mode.
- M3 also reduces signal feedthrough when in the hold mode.
- The speed is degraded because of the necessity to guarantee stability in the track mode.

## An RC Closed-Loop S/H



- The A1 opamp need to have low output impedance.

# A Switched-Capacitor Closed-Loop S/H

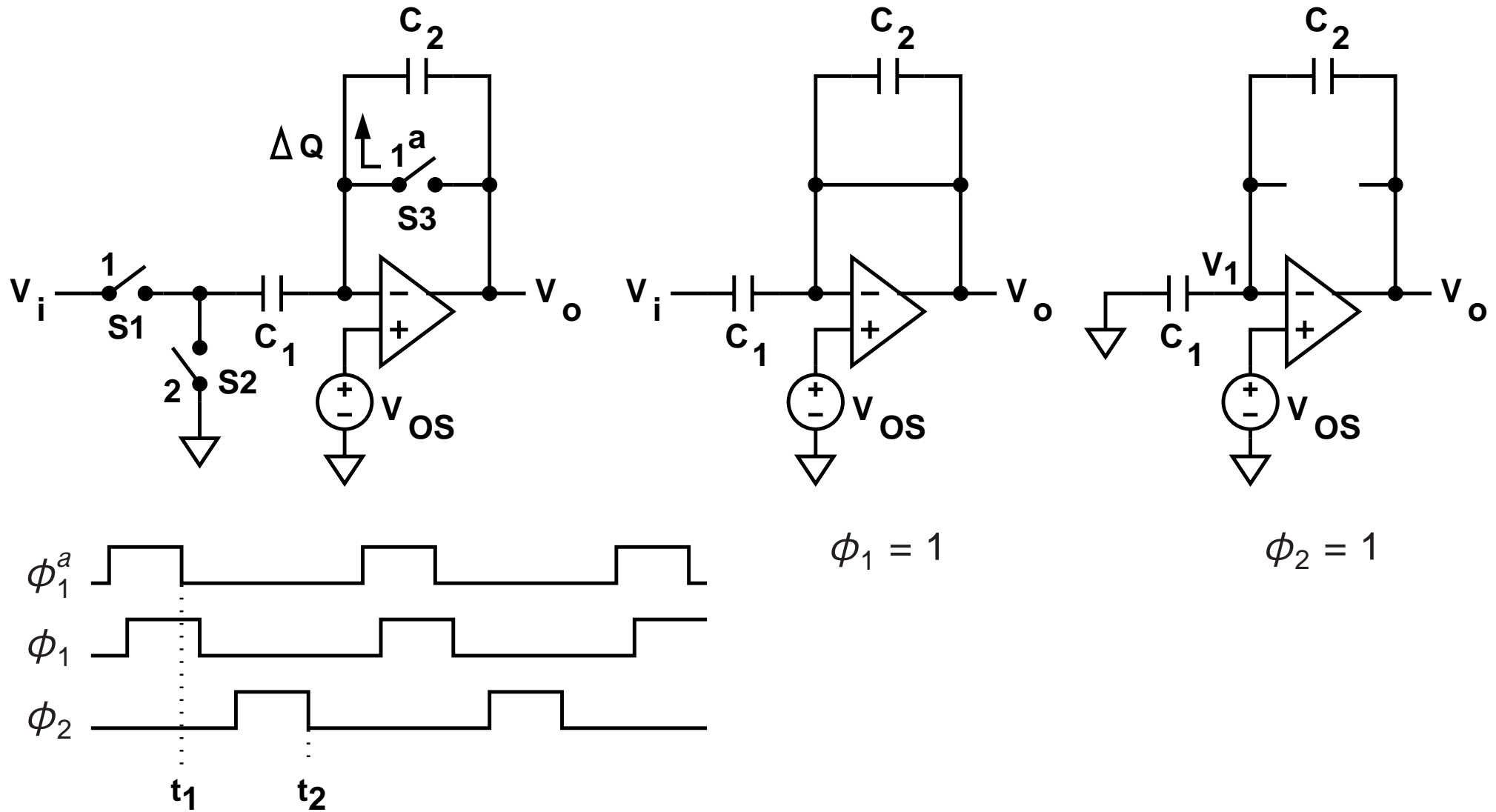


# A Switched-Capacitor Closed-Loop S/H

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- The  $V_o$  is always valid.
- The  $V_{OS1}$  of A1 is stored in  $C_{H2}$  during the sample mode.
- The M2's switching error is canceled by M3.
- The M5's switching error is canceled by M6.
- The switching error of M1 and M4 doesn't affect  $V_o$ .

# Charge Redistribution Sampled-Data Amplifier



# Charge Redistribution Sampled-Data Amplifier

---

To consider the ideal case, let  $A = \infty$  and  $V_{OS} = 0$ , then

$$V_o(t_1) = 0$$
$$C_1 V_i(t_1) = C_2 V_o(t_2) \quad \Rightarrow \quad V_o(t_2) = \frac{C_1}{C_2} \times V_i(t_1)$$

To consider the  $V_{OS}$  effect, let  $A = \infty$ , then

$$V_o(t_1) = V_{OS}(t_1)$$
$$V_o(t_2) = \frac{C_1}{C_2} \times V_i(t_1) + V_{OS}(t_1) + \left(1 + \frac{C_1}{C_2}\right) \times [V_{OS}(t_2) - V_{OS}(t_1)]$$
$$= \frac{C_1}{C_2} \times \left[ V_i(t_1) + \frac{C_2}{C_1} \cdot V_{OS}(t_1) \right] + \left(1 + \frac{C_1}{C_2}\right) \times [V_{OS}(t_2) - V_{OS}(t_1)]$$

- The input referred offset is  $V_{OS} \cdot (C_2/C_1)$ .

# Charge Redistribution Sampled-Data Amplifier

---

To consider the finite gain effect, let  $V_{OS} = 0$ , then during  $\phi_2 = 1$

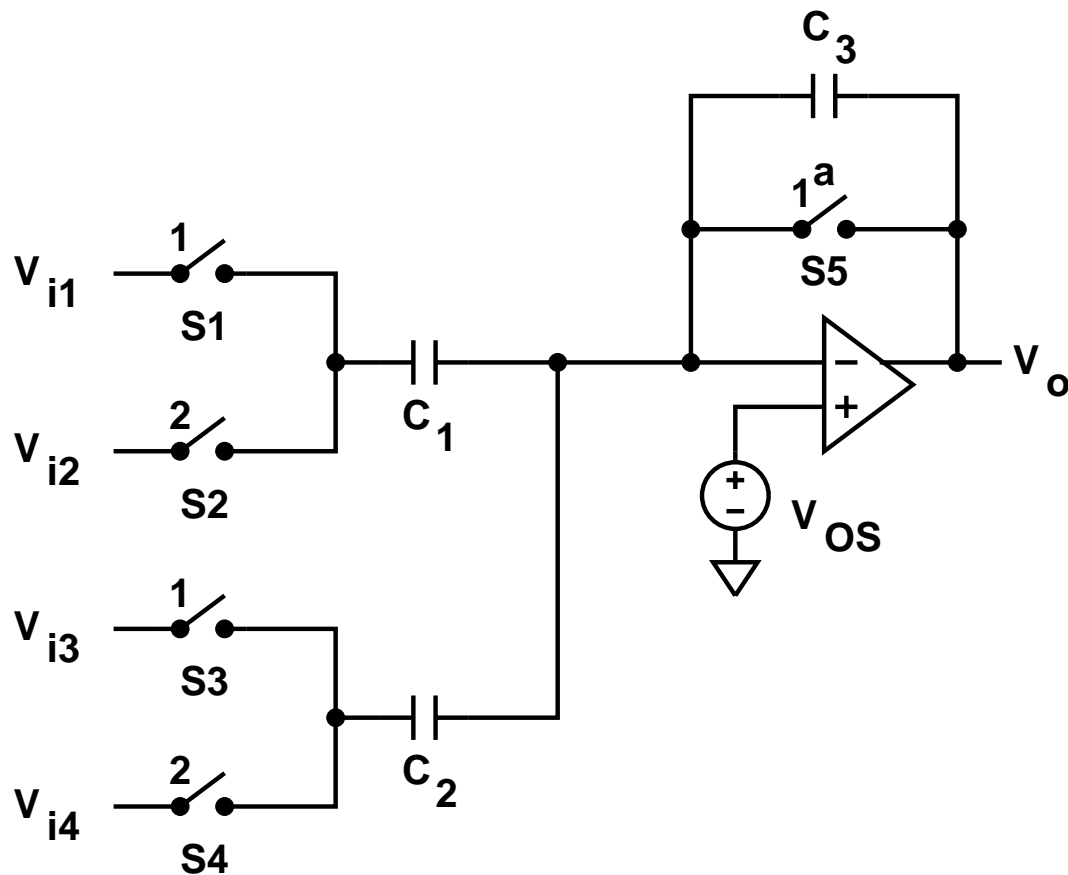
$$C_1 V_i + C_1 V_1 = C_2 (V_o - V_1) \quad V_o = -A V_1 \quad \Rightarrow \quad V_o = \frac{C_1}{C_2} \cdot \frac{1}{1 + \frac{1}{A} \left(1 + \frac{C_1}{C_2}\right)} \times V_i$$

To consider the effect S3 switching error, let  $A = \infty$ ,  $V_{OS} = 0$ , and  $V_i = 0$ , then during  $\phi_2 = 1$

$$V_o = V'_{OS} = -\frac{\Delta Q}{C_2}$$

- $V'_{OS}$  is independent of input.
- If S3 is opened before S1, the switching errors of S1 and S2 have no effect on  $V_o$ .

# Charge Redistribution Summing Amplifier



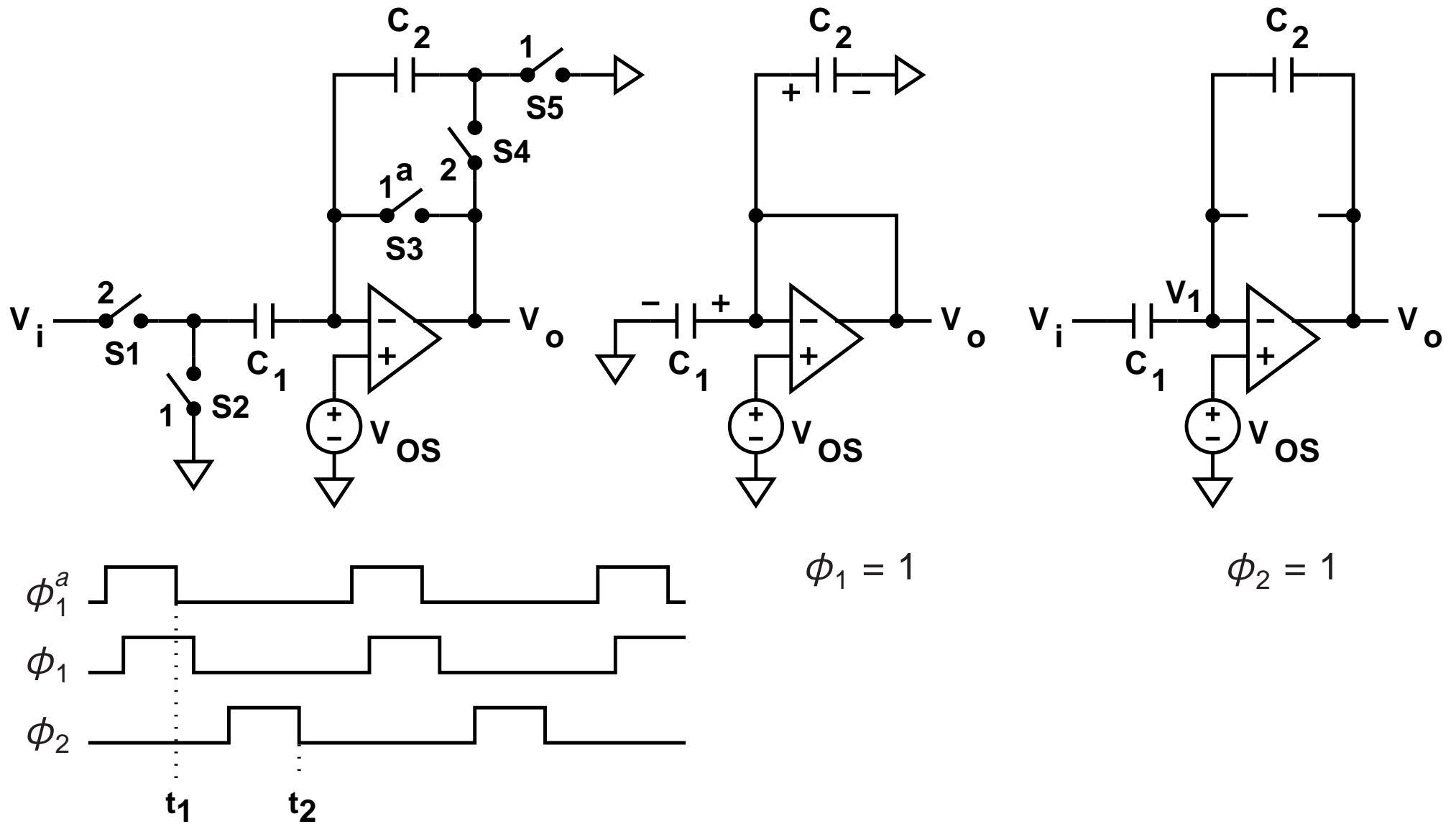
During the sample mode ( $\phi_1 = 1$ )

$$V_o = V_{OS}$$

During the hold mode ( $\phi_2 = 1$ )

$$V_o = \frac{C_1}{C_3}(V_{i1} - V_{i2}) + \frac{C_2}{C_3}(V_{i3} - V_{i4}) + V_{OS}$$

# Sampled-Data Amplifier with CDS



# Sampled-Data Amplifier with CDS

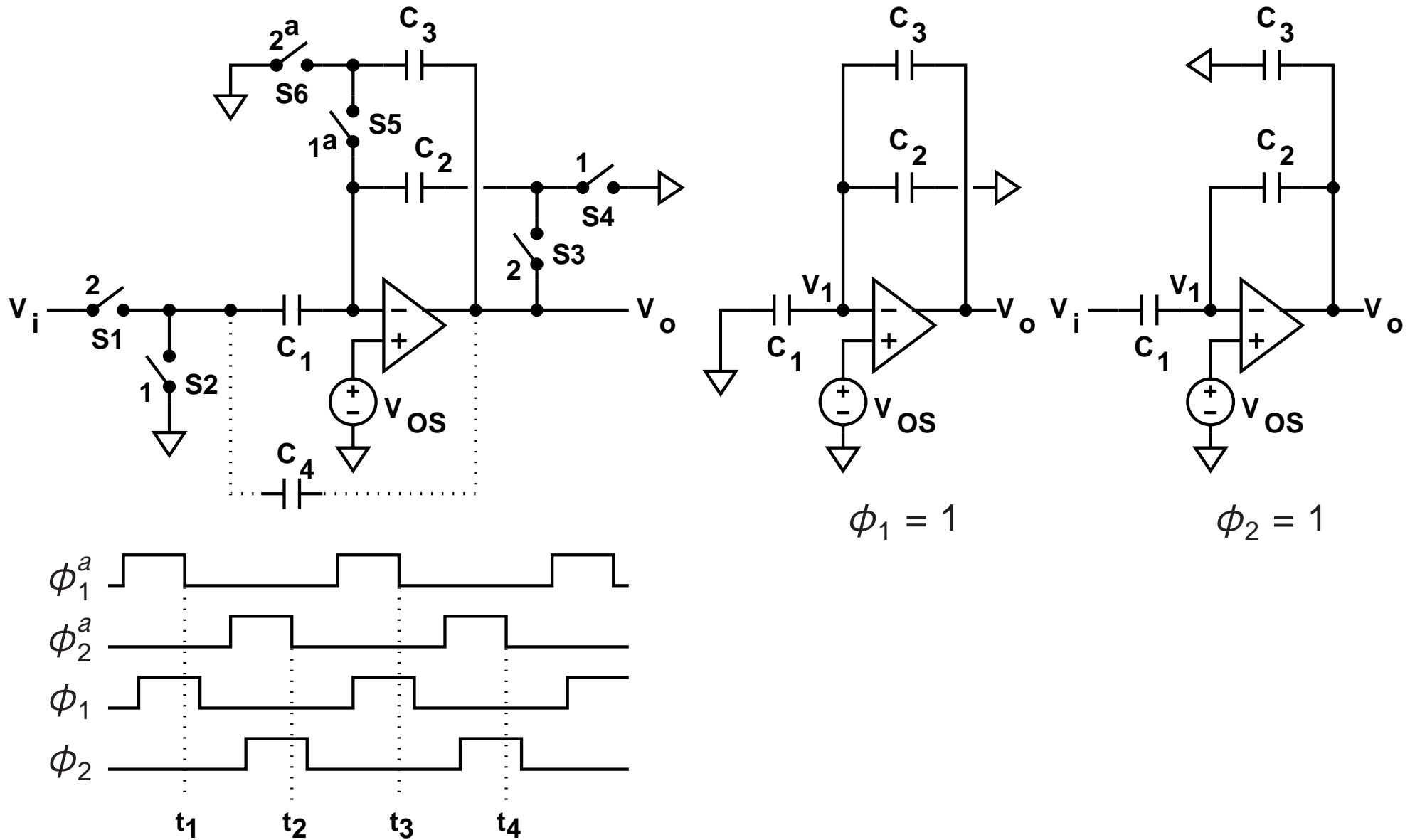
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Let  $A = \infty$ , then

$$V_o(t_1) = V_{c1} = V_{c2} = V_{OS}(t_1)$$
$$V_o(t_2) = -\frac{C_1}{C_2} \times V_i(t_2) + \left(1 + \frac{C_1}{C_2}\right) [V_{OS}(t_2) - V_{OS}(t_1)]$$

- The correlated double-sampling (CDS) technique, resulting in  $V_{OS}(nT_s) - V_{OS}(nT_s - T_s/2)$ , can reduce the effects of the opamp's input offset voltage and its 1/f noise.
- To minimize switching noises, realize switches with nMOSTs whenever possible, and turn off the switches near the virtual ground node of the opamps first.
- Reference: C. Enz and G. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," Proc. IEEE, Nov. 1996, pp. 1584–1614.

# A Capacitive-Reset Sampled-Data Amplifier



# A Capacitive-Reset Sampled-Data Amplifier

---

To consider the  $V_{OS}$  effect, let  $A = \infty$  and  $V_i = 0$ , then

$$V_1(t_1) = V_{OS}(t_1)$$

$$V_o(t_2) = \left(1 + \frac{C_1}{C_2}\right) \times [V_{OS}(t_2) - V_{OS}(t_1)]$$

$$V_o(t_3) = V_{OS}(t_3) + V_o(t_2) + \frac{C_2}{C_3} \times V_o(t_2) + \left(1 + \frac{C_1 + C_2}{C_3}\right) \times [V_{OS}(t_3) - V_{OS}(t_2)] \approx V_{OS}(t_3)$$

$$V_o(t_4) = \left(1 + \frac{C_1}{C_2}\right) \times [V_{OS}(t_4) - V_{OS}(t_3)]$$

- During  $\phi_2 = 1$ , the effects of opamp's  $V_{OS}$  and  $1/f$  noise are reduce by CDS.

# A Capacitive-Reset Sampled-Data Amplifier

---

To consider the finite gain effect, let  $V_{OS} = 0$ , then

$$-C_1V_1(t_1) - C_2V_1(t_1) = C_1[V_i(t_2) - V_1(t_2)] + C_2[V_o(t_2) - V_1(t_2)] \quad V_1 = -V_o/A$$

$$\Rightarrow V_o(t_2) = -\frac{C_1}{C_2} \cdot \frac{1}{1 + \frac{1}{A} \left(1 + \frac{C_1}{C_2}\right)} \times V_i(t_2) + \frac{1}{A} \left(1 + \frac{C_1}{C_2}\right) \cdot \frac{1}{1 + \frac{1}{A} \left(1 + \frac{C_1}{C_2}\right)} \times V_o(t_1)$$

$$\approx -\frac{C_1}{C_2}(1 - \epsilon_1) \times V_i(t_2) + \epsilon_1(1 - \epsilon_1) \times V_o(t_1)$$

$$V_o(t_3) \approx (1 - \epsilon_2)V_o(t_2) + \frac{C_1}{C_3}(1 - \epsilon_2)V_i(t_2) + \frac{C_2}{C_3}(1 - \epsilon_3)V_o(t_2) \approx V_o(t_2) \approx -\frac{C_1}{C_2}V_i(t_2)$$

$$V_o(t_4) \approx -\frac{C_1}{C_2}(1 - \epsilon_1) \times V_i(t_4) + \epsilon_1(1 - \epsilon_1) \times V_o(t_3)$$

$$\approx -\frac{C_1}{C_2} \times V_i(t_4) + \epsilon_1 \frac{C_1}{C_2} \times [V_i(t_4) - V_i(t_2)] + \epsilon_1^2 \frac{C_1}{C_2} \times V_i(t_2)$$

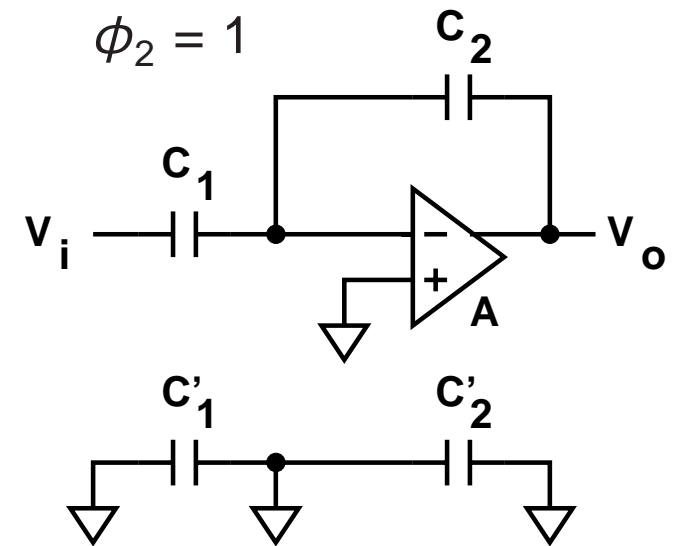
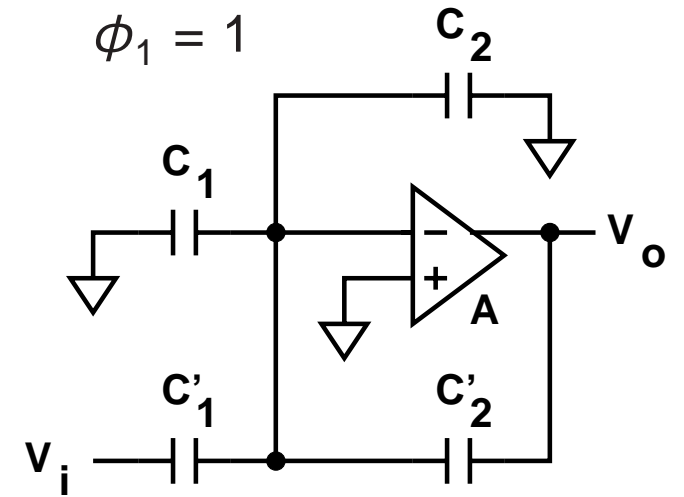
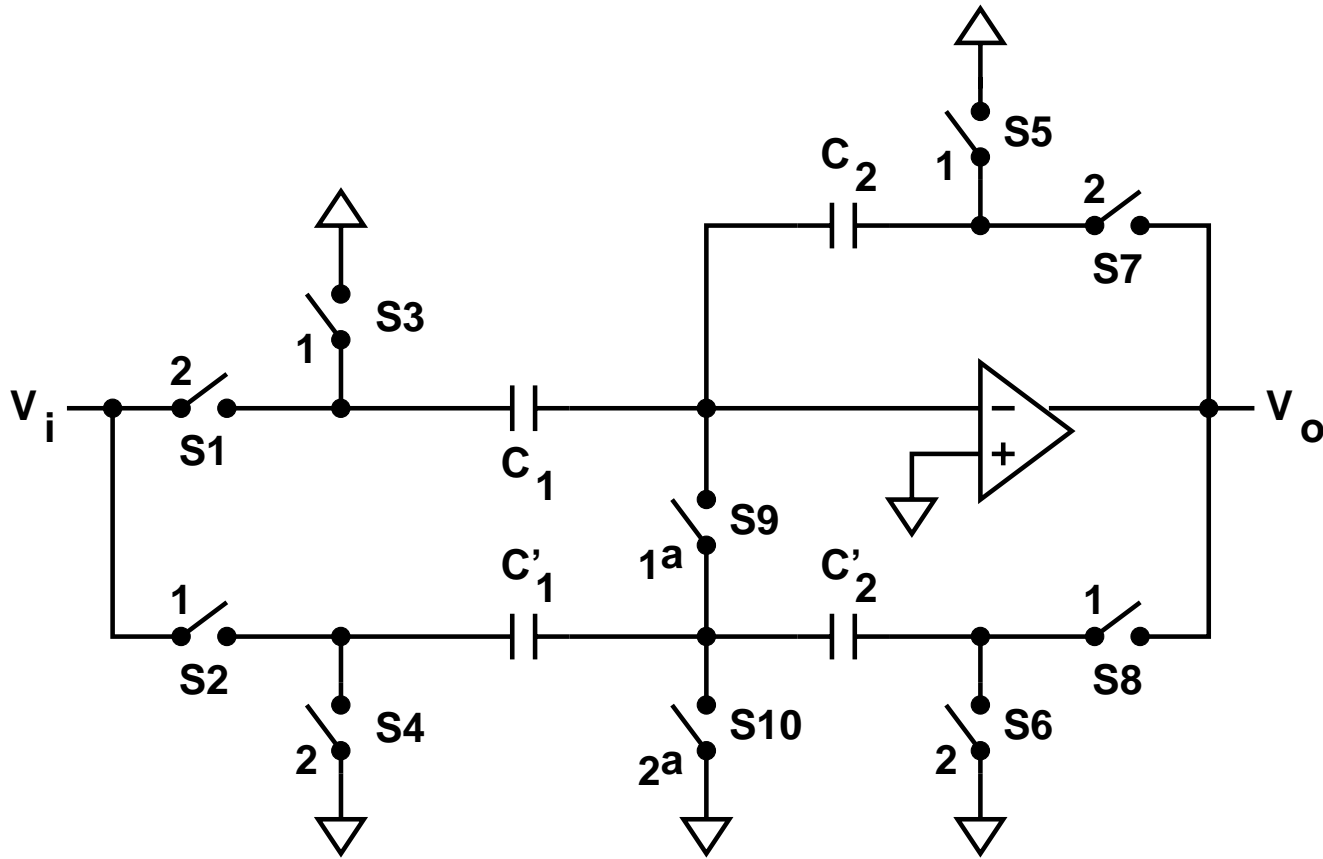
$$\epsilon_1 = \frac{1}{A} \left(1 + \frac{C_1}{C_2}\right) \quad \epsilon_2 = \frac{1}{A} \left(1 + \frac{C_1}{C_3}\right) \quad \epsilon_3 = \frac{1}{A} \left(1 + \frac{C_2}{C_3}\right)$$

# A Capacitive-Reset Sampled-Data Amplifier

---

- During  $\phi_2 = 1$ , the effects of opamp's  $V_{OS}$  and  $1/f$  noise are reduced by CDS.
- During  $\phi_2 = 1$ , the errors due to opamp's finite gain,  $A$ , are proportional to  $1/A^2$  for low-frequency input.
- During  $\phi_1 = 1$ , the output keeps the value obtained in the previous  $\phi_2 = 1$  period.
- C4 is an optional deglitching capacitor used to provide continuous-time feedback during the nonoverlap clock times. This capacitor would normally be small.
- The clock phases for S1 and S2 can be exchanged, to obtain noninverting gain.
- When CDS is used, the opamps should be designed to minimize thermal noise rather than  $1/f$  noise.

# A Capacitive-Reset CDS Amplifier



# A Capacitive-Reset CDS Amplifier

---

- During  $\phi_1 = 1$ ,  $C'_1$  and  $C'_2$  are used in the feedback network to have

$$V_o \approx -\frac{C'_1}{C'_2} \cdot V_i$$

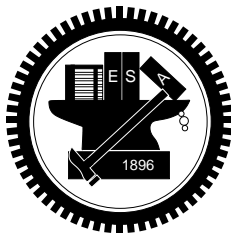
but with errors due to  $V_{OS}$ ,  $1/f$  noise, and  $A$ .

- During  $\phi_1 = 1$ , the opamp input voltage is sampled and stored in  $C_1$  and  $C_2$ .
- During  $\phi_2 = 1$ ,  $C_1$  and  $C_2$  are used in the feedback network, the output errors due to  $V_{OS}$ ,  $1/f$  noise, and  $A$  are canceled by the correlated double-sampling (CDS) operation.

# Comparators and Offset Cancellation Techniques

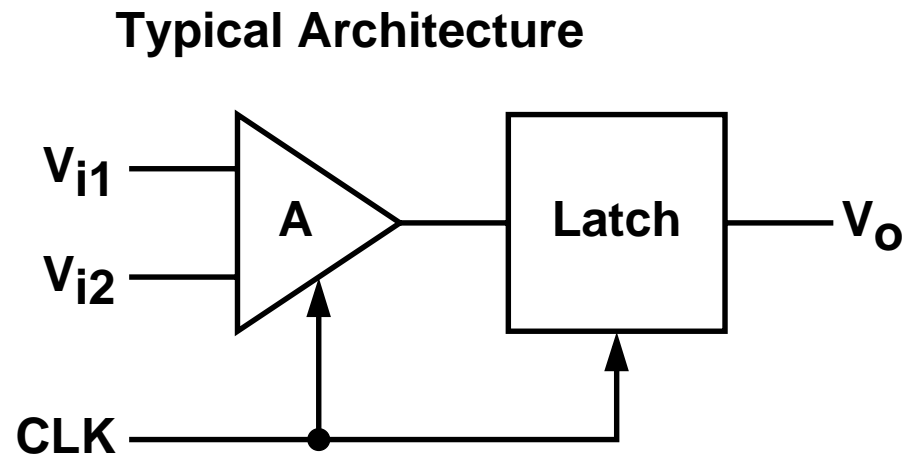
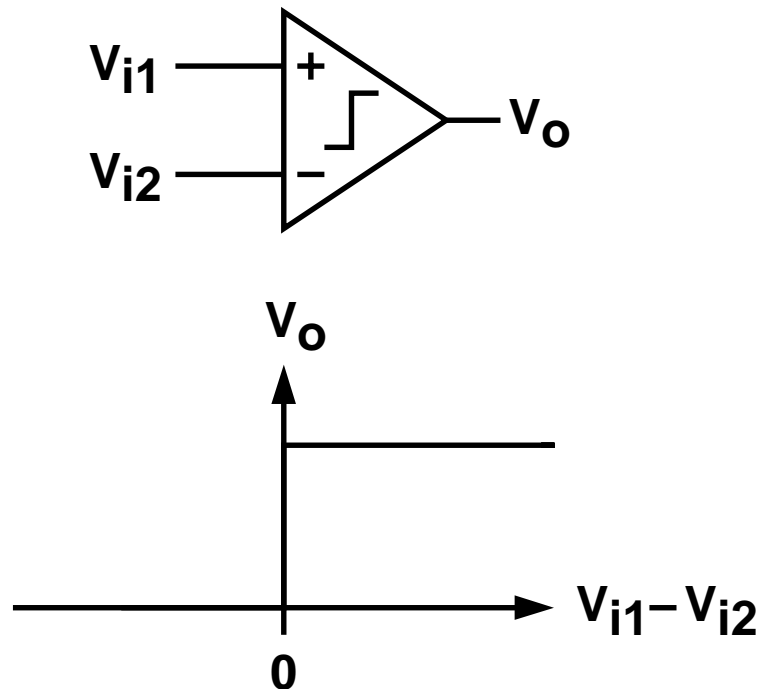
Jieh-Tsorng Wu

October 25, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Comparators



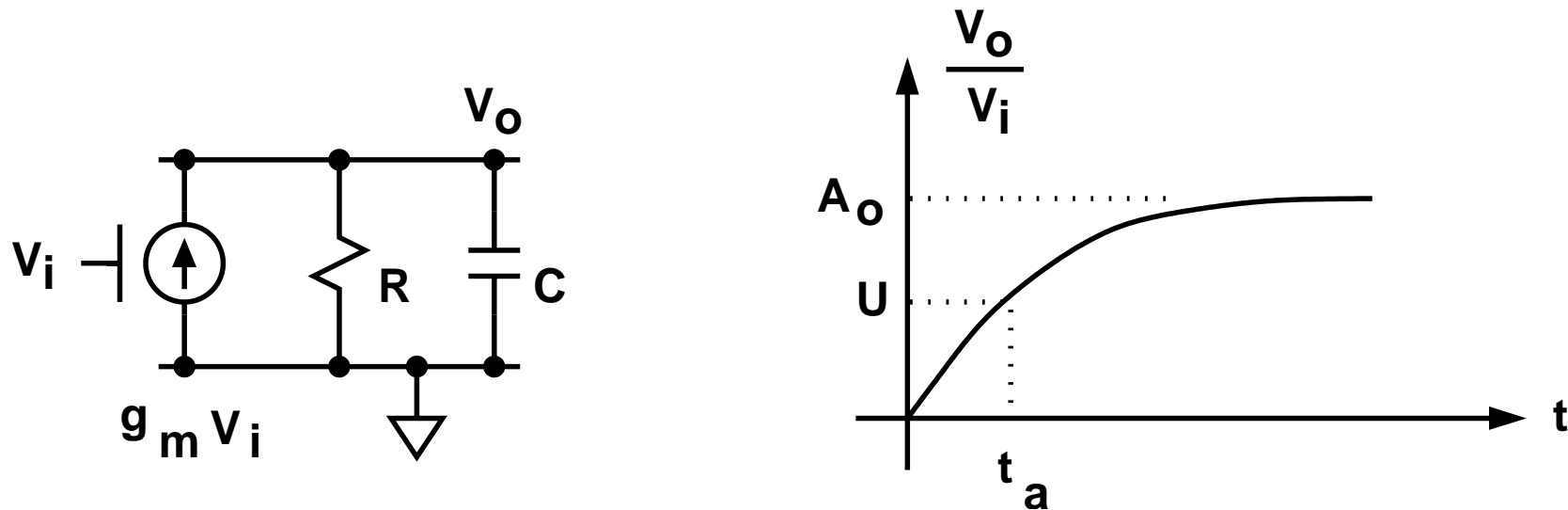
- A comparator compare the instantaneous values of two inputs generate a digital 1 or 0 level depending on the polarity of the difference.
- Usually a clock is applied to improve the performance.

# Comparator Design Considerations

---

- Resolution (gain).
- Accuracy (offset).
- Input range (dynamic range).
- Common-mode rejection.
- Speed (conversion time, over-drive recovery).
- Power dissipation.
- Input kickback noise.
- Area

# Comparison with Single-Pole Amplifier

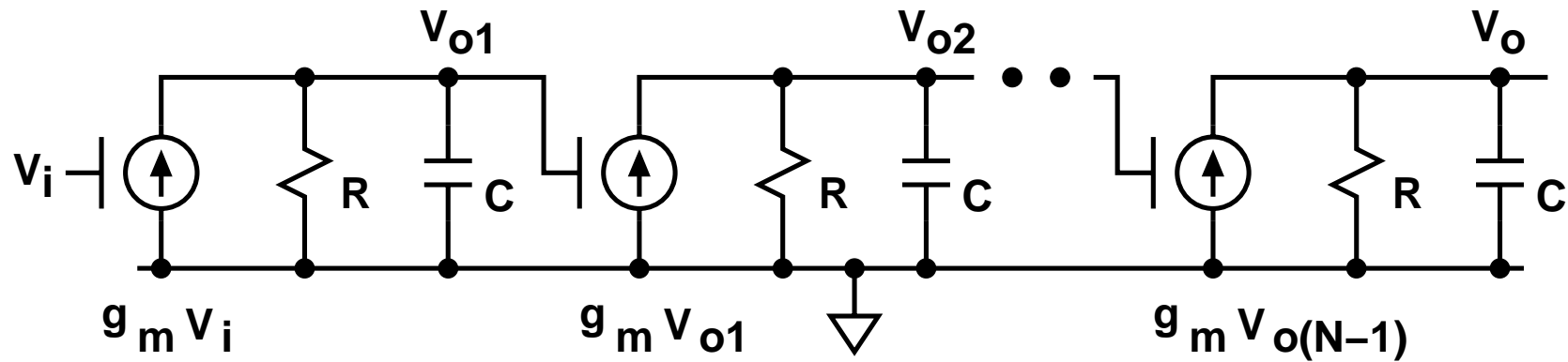


$$U = \frac{V_o}{V_i} = A_o \left[ 1 - e^{-t_a/(RC)} \right] \quad A_o = g_m R \quad \tau_m = \frac{C}{g_m}$$

$$\frac{t_a}{\tau_m} = A_o \times \ln \left( \frac{1}{1 - \frac{U}{A_o}} \right) \quad \Rightarrow \quad \frac{t_a}{\tau_m} \approx U \quad \text{if } U \ll A_o$$

- The amplification in a comparator need not be linear.

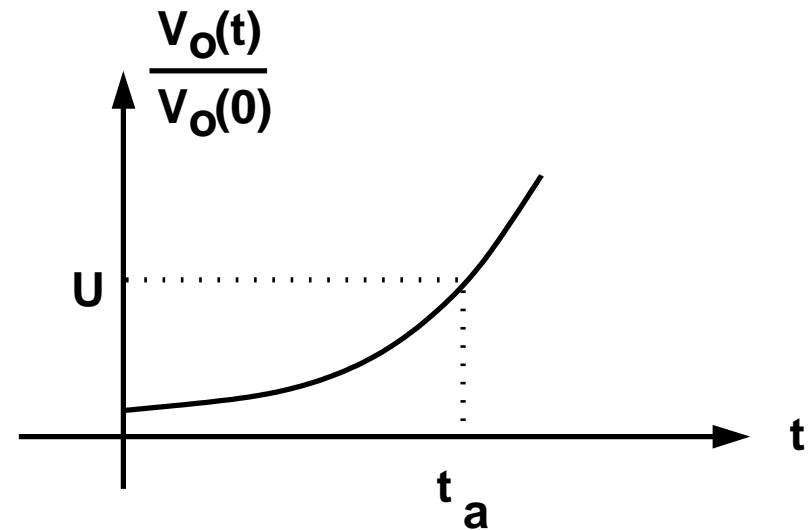
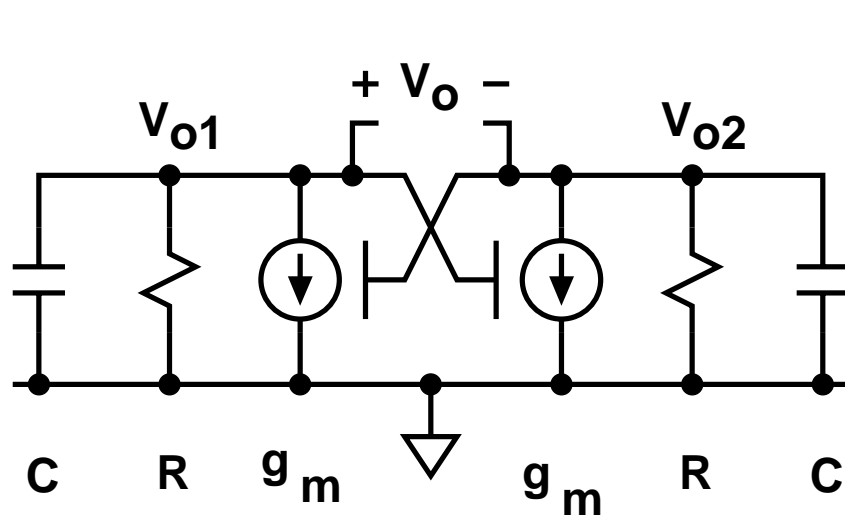
## Comparison with Multi-Stage Cascaded Amplifier



$$\frac{t_a}{\tau_m} \approx (U \times N!)^{\frac{1}{N}} \quad \text{for} \quad t_a \ll A_o \tau_m$$

- There exists an optimum number of cascaded stages for minimum  $t_a$ .
- Optimum in  $N$  is very broad.
- Gain of  $\sqrt{10}$  (i.e. 10 dB) per stage results in near optimum delay (within 10%).

# Comparison with Positive-Feedback Regeneration



$$U = \frac{V_o(t_a)}{V_o(0)} = e^{\frac{(A_o-1)t_a}{RC}}$$

$$A_o = g_m R \quad \tau_m = \frac{C}{g_m}$$

$$\frac{t_a}{\tau_m} = \frac{1}{1 - \frac{1}{A_o}} \times \ln(U)$$

$$\Rightarrow \frac{t_a}{\tau_m} \approx \ln(U) \quad \text{if } A_o \gg 1$$

# Comparison with Positive-Feedback Regeneration

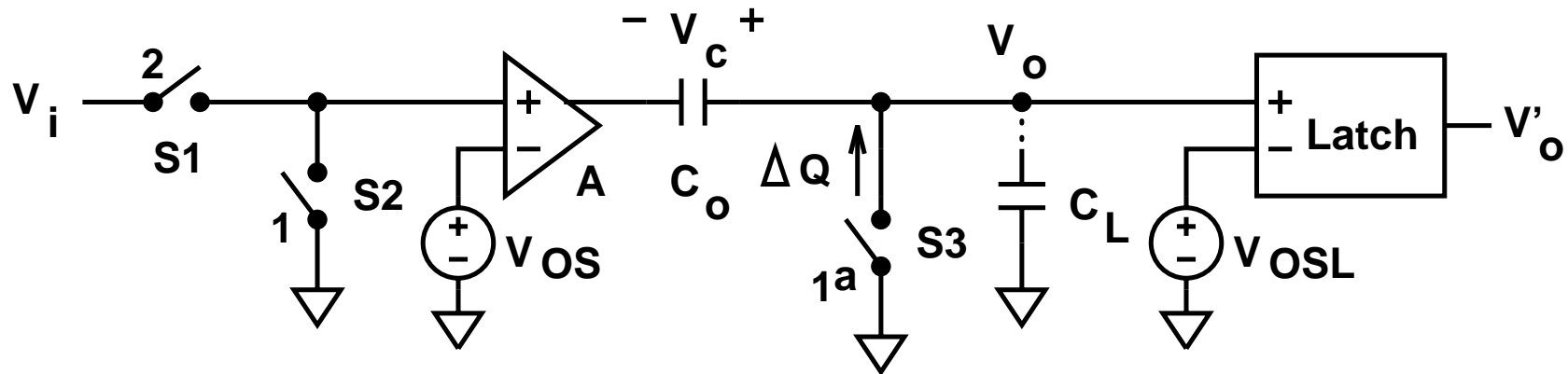
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- The *gain* is not bounded by  $A_o$ .
- It is *faster* than the multi-stage cascaded amplifier, and dissipates less power.
- Require a strobe signal (clock).
- Let  $T_c$  be the conversion time, the final output  $V_o(T_c) = V$ , and the initial sampled input  $V_o(0)$  has a uniform distribution between  $-V$  and  $+V$ . Then the probability of observing a *metastable state* is

$$P = \frac{V/U}{V} = \frac{1}{U} = e^{-\frac{(A_o-1)T_c}{RC}} \approx e^{-\frac{T_c}{C/g_m}}$$

The metastable state occurs when the sampled input is so small that the regenerated output,  $|V_o|$ , cannot reach  $|V|$  after the  $T_c$  period.

# Output Offset Storage (OOS)



During the reset mode ( $\phi_1 = 1$ )

$$V_o = 0 \quad V_c = A \times V_{OS}$$

During the amplification mode ( $\phi_2 = 1$ )

$$V'_o = V_i \times A \cdot \frac{C_o}{C_o + C_L} + \frac{\Delta Q}{C_o + C_L} - V_{OSL} = A \cdot \frac{C_o}{C_o + C_L} \left( V_i + \frac{\Delta Q}{AC_o} - \frac{V_{OSL}}{A} \cdot \frac{C_o + C_L}{C_o} \right)$$

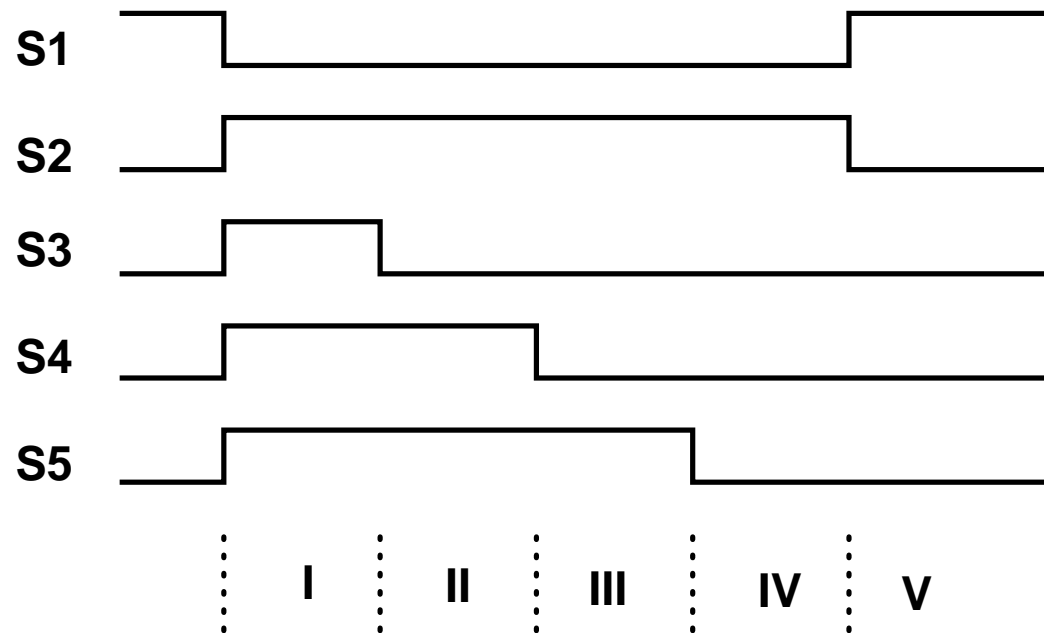
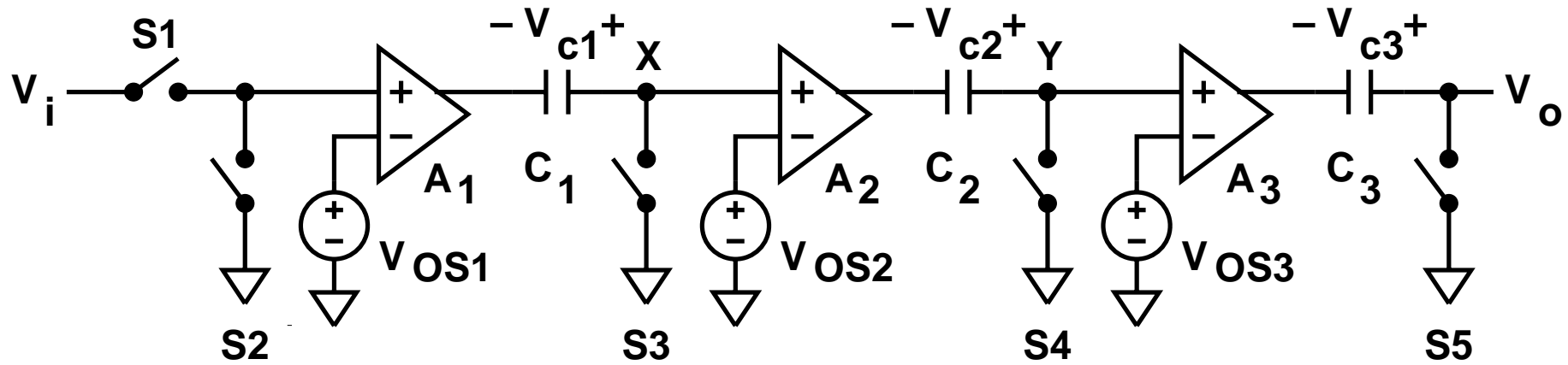
$$\text{Input-Referred Offset} = V_{OS,in} = \frac{1}{A} \cdot \frac{\Delta Q}{C_o} - \frac{V_{OSL}}{A} \cdot \frac{C_o + C_L}{C_o}$$

# Output Offset Storage (OOS)

---

- During the reset-to-amplification transition, let S3 open before S2, so that  $\Delta Q$  can be a constant.
- Amplifier  $A$  cannot employ high gain.
- Amplifier  $A$  must cover the input common-mode range.
- Want latch with high-impedance (capacitive) input so as not to discharge  $C_o$  during amplification.
- Make  $C_o \gg C_L$  to avoid attenuation.

# Multistage Output Offset Storage



# Multistage Output Offset Storage

---

During Period I, S1 open, S2–S5 closed.

$$V_{c1} = A_1 V_{OS1} \quad V_{c2} = A_2 V_{OS2} \quad V_{c3} = A_3 V_{OS3}$$

During Period II, S3 open.

$$V_X = \epsilon_2 = \text{S3 Switching Error} \quad V_{c1} = A_1 V_{OS1} + \epsilon_2 \quad V_{c2} = A_2 (V_{OS2} - \epsilon_2)$$

During Period III, S4 open.

$$V_Y = \epsilon_3 = \text{S4 Switching Error} \quad V_{c2} = A_2 (V_{OS2} - \epsilon_2) + \epsilon_3 \quad V_{c3} = A_3 (V_{OS3} - \epsilon_3)$$

During Period IV, S5 open.

$$V_O = \epsilon_4 = \text{S5 Switching Error} \quad V_{c3} = A_3 (V_{OS3} - \epsilon_3) + \epsilon_4$$

# Multistage Output Offset Storage

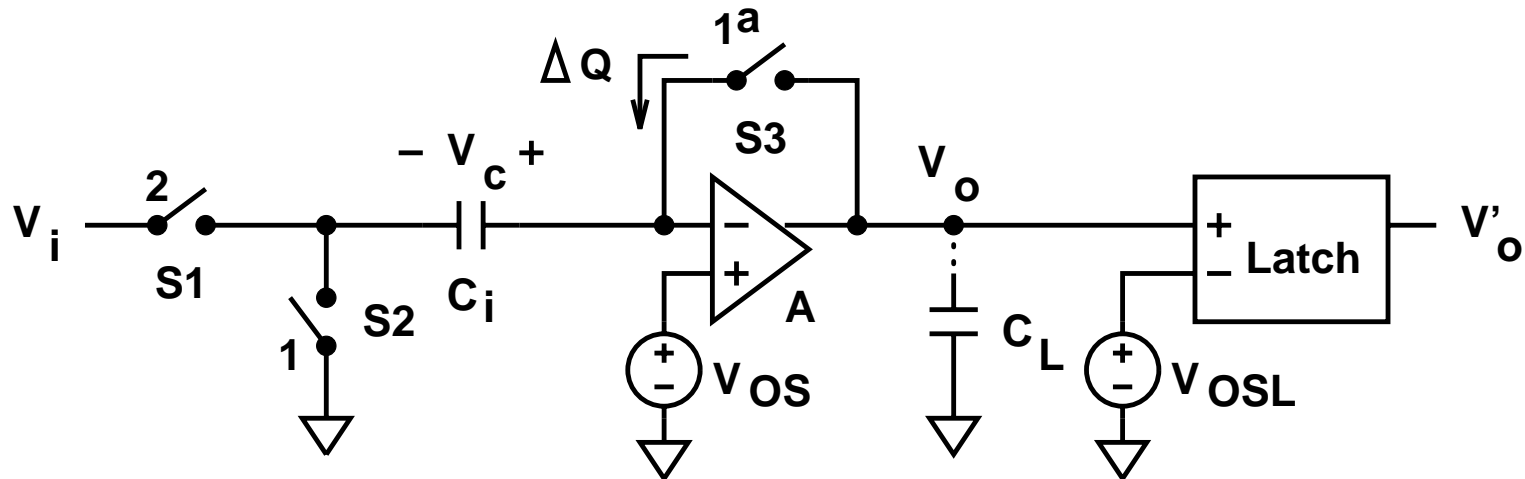
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During Period V (amplification mode), S2 closed, S1 open.

$$V_o = A_1 \cdot A_2 \cdot A_3 \cdot V_i + \epsilon_4$$

$$V_{OS,in} = \frac{\epsilon_4}{A_1 \cdot A_2 \cdot A_3}$$

# Input Offset Storage (IOS)



During the reset mode ( $\phi_1 = 1$ )

$$V_o = V_c = V_{OS} \times \frac{A}{A + 1}$$

During the amplification mode ( $\phi_2 = 1$ )

$$V'_o = -V_i \times A + V_{OS} \frac{A}{A + 1} - \frac{\Delta Q}{C_i} A - V_{OSL} = -A \left( V_i - \frac{V_{OS}}{A + 1} + \frac{\Delta Q}{C_i} + \frac{V_{OSL}}{A} \right)$$

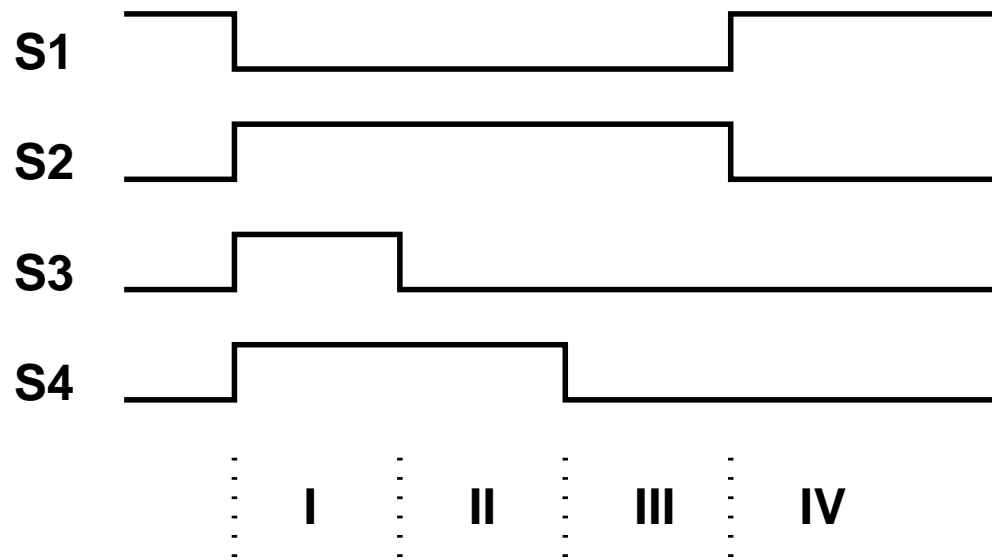
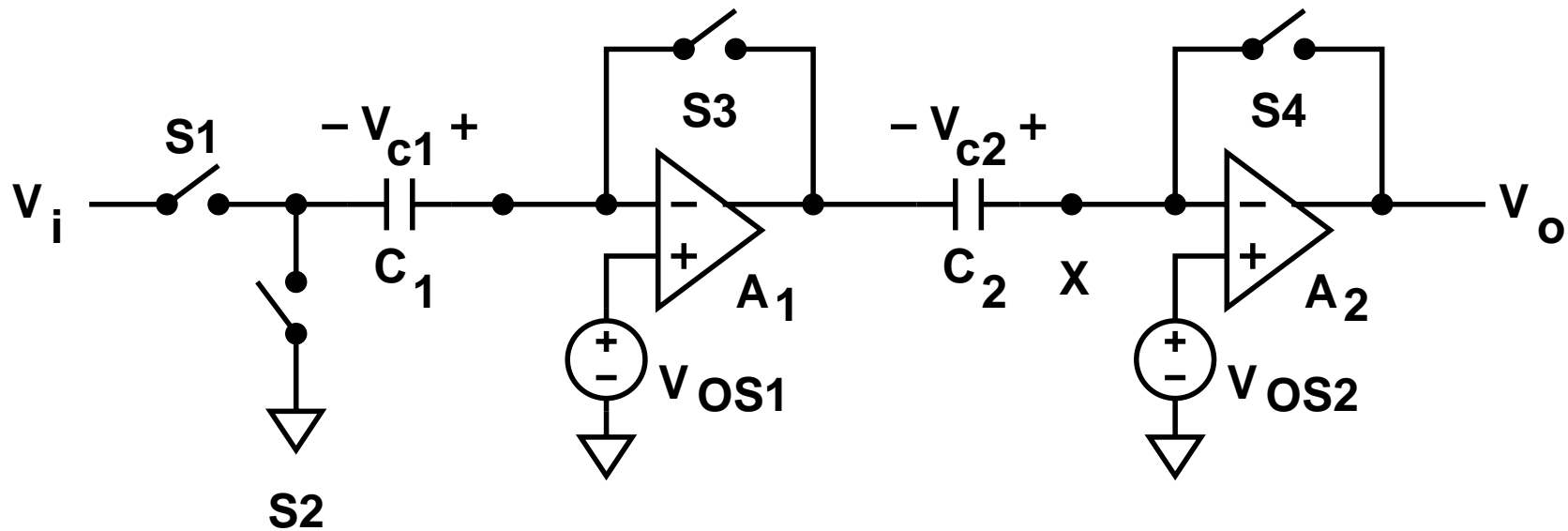
$$\text{Input-Referred Offset} = V_{OS,in} = -\frac{V_{OS}}{A + 1} + \frac{\Delta Q}{C_i} + \frac{V_{OSL}}{A}$$

# Input Offset Storage (IOS)

---

- The S3 switching error  $\Delta Q$  is input-independent.
- During the reset-to-amplification transition, let S3 open before S2.
- The IOS allows rail-to-rail input common-mode level and quick overdrive recovery.
- Amplifier  $A$  can employ high gain.
- Amplifier  $A$  may require compensation  $C_c$  to ensure closed-looped stability.  $C_c$  can be switched off during the amplification mode.

# Multistage Input Offset Storage



# Multistage Input Offset Storage

---

During Period I, S1 open, S2–S4 closed.

$$V_{c1} = \frac{A_1}{A_1 + 1} V_{OS1} \quad V_{c2} = \frac{A_2}{A_2 + 1} V_{OS2} - V_{c1} = \frac{A_2}{A_2 + 1} V_{OS2} - \frac{A_1}{A_1 + 1} V_{OS1}$$

During Period region II, S3 open. Let  $\epsilon_1$  be the 3 switching error.

$$V_{c1} = \frac{A_1}{A_1 + 1} V_{OS1} + \epsilon_1 \quad V_{c2} = \frac{A_2}{A_2 + 1} V_{OS2} - \frac{A_1}{A_1 + 1} V_{OS1} + A_1 \epsilon_1$$

During Period III, S4 open. Let  $\epsilon_2$  be the S4 switching error.

$$V_{c2} = \frac{A_2}{A_2 + 1} V_{OS2} - \frac{A_1}{A_1 + 1} V_{OS1} + A_1 \epsilon_1 + \epsilon_2 \quad V_o = \frac{A_2}{A_2 + 1} V_{OS2} - A_2 \epsilon_2$$

# Multistage Input Offset Storage

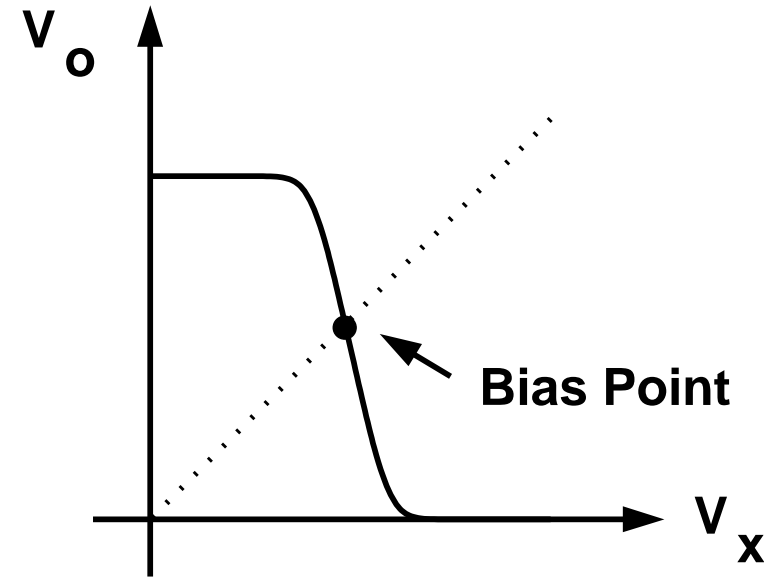
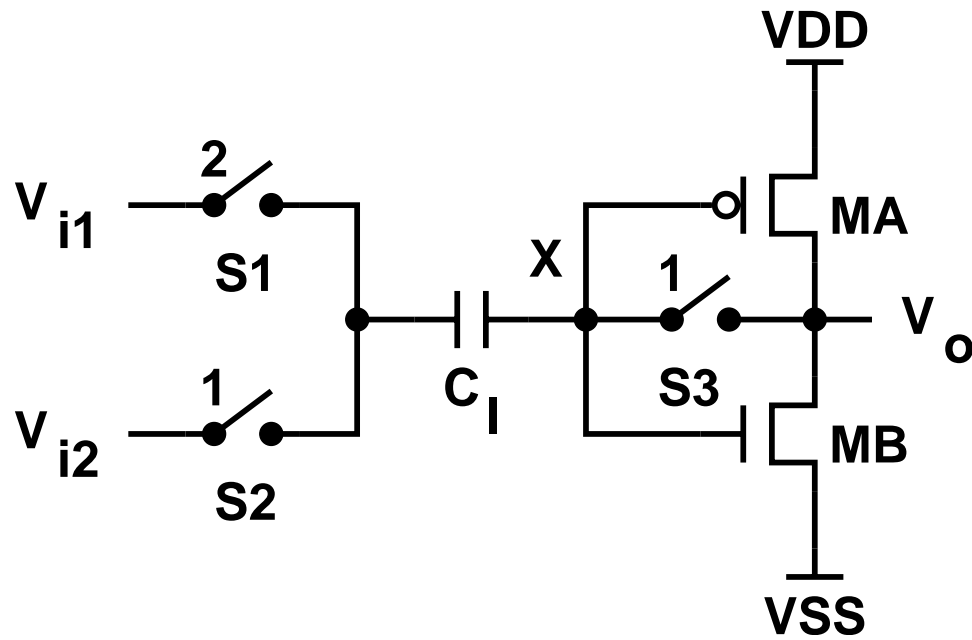
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During Period IV (amplification mode), S2 open, S1 closed.

$$V_o = A_1 A_2 V_i + \frac{A_2}{A_2 + 1} V_{OS2} - A_2 \epsilon_2 = A_1 A_2 \left[ V_i + \frac{V_{OS2}}{A_1(A_2 + 1)} - \frac{\epsilon_2}{A_1} \right]$$

$$\text{Input-Referred Offset} = V_{OS,in} = \frac{V_{OS2}}{A_1(A_2 + 1)} - \frac{\epsilon_2}{A_1}$$

# MOST Comparator: Auto-Zeroing Inverter

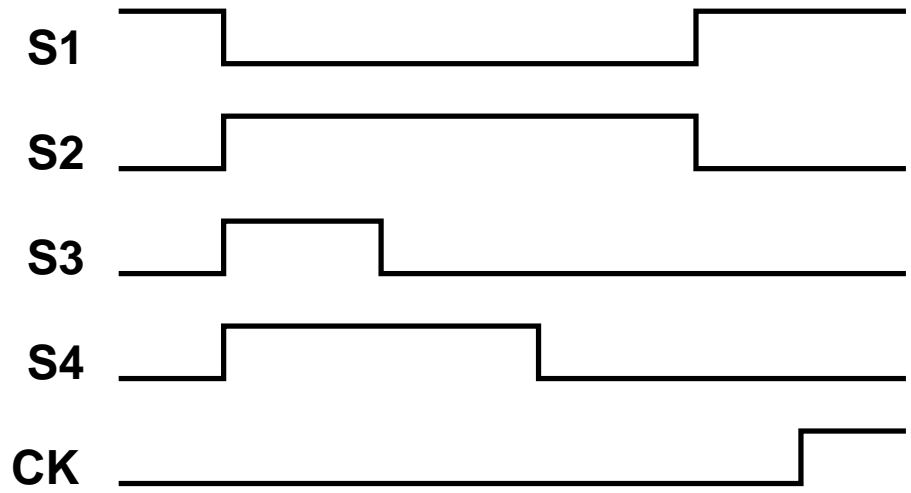
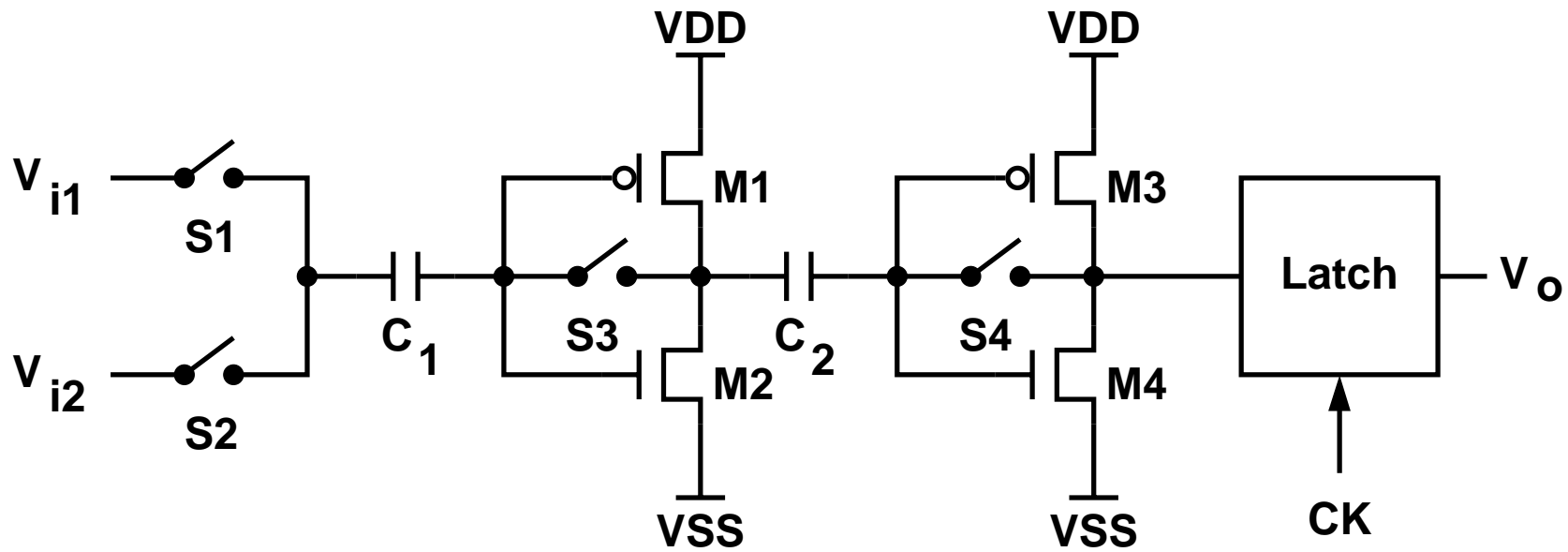


# MOST Comparator: Auto-Zeroing Inverter

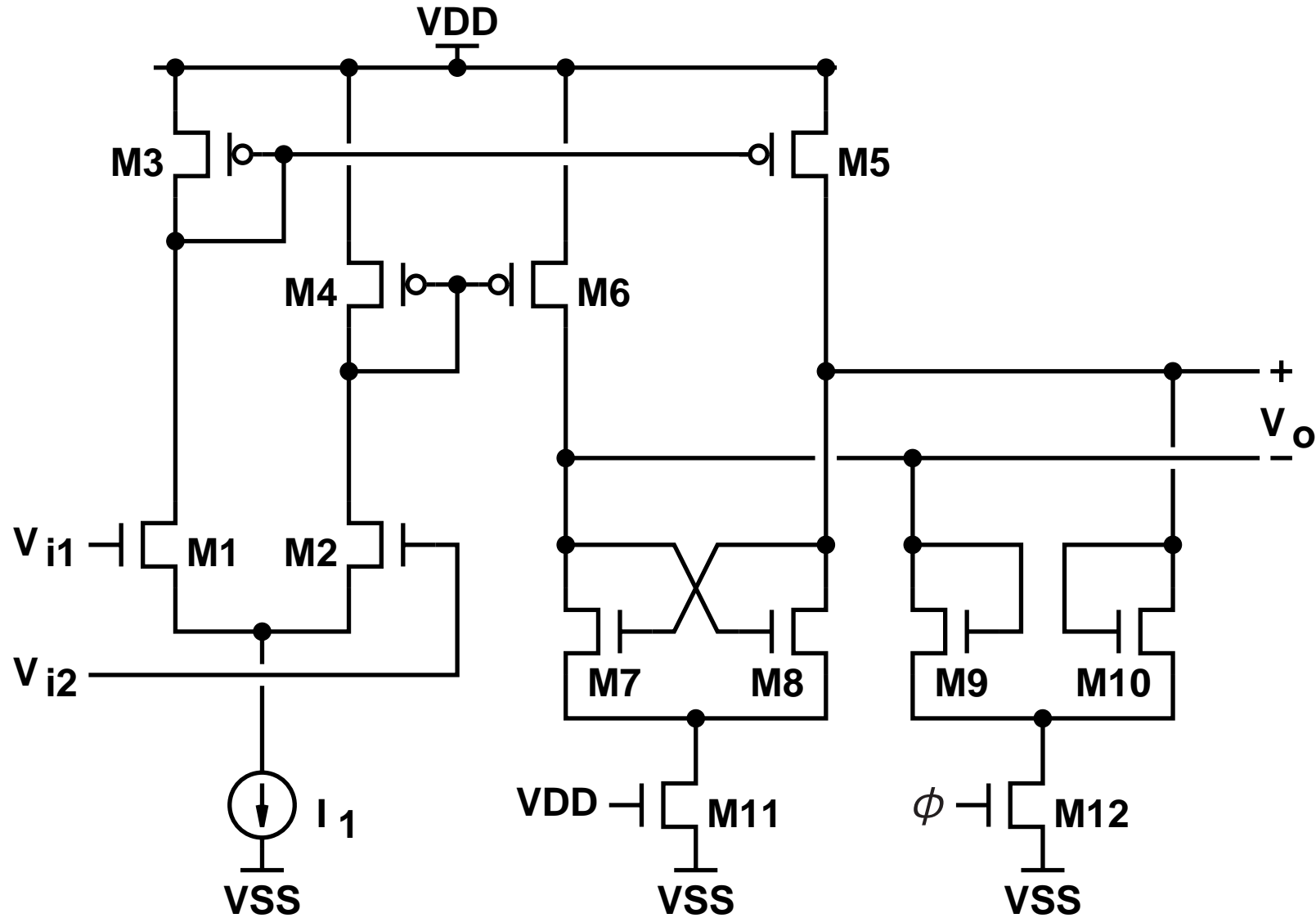
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- Trade-off between speed and resolution by selecting different value of  $C$ .
- Very sensitive to supply noises.
- Power dissipation is strongly process- and supply-dependent.
- Kickback noise presented at the inputs.
- Reference: T. Kumamoto, et. al., JSSC, 12/86, pp. 976–982.

# MOST Comparator: Cascaded Auto-Zeroing Inverters



# MOST Comparator: Preamp + Regenerative Sense Amplifier



# MOST Comparator: Preamp + Regenerative Sense Amplifier

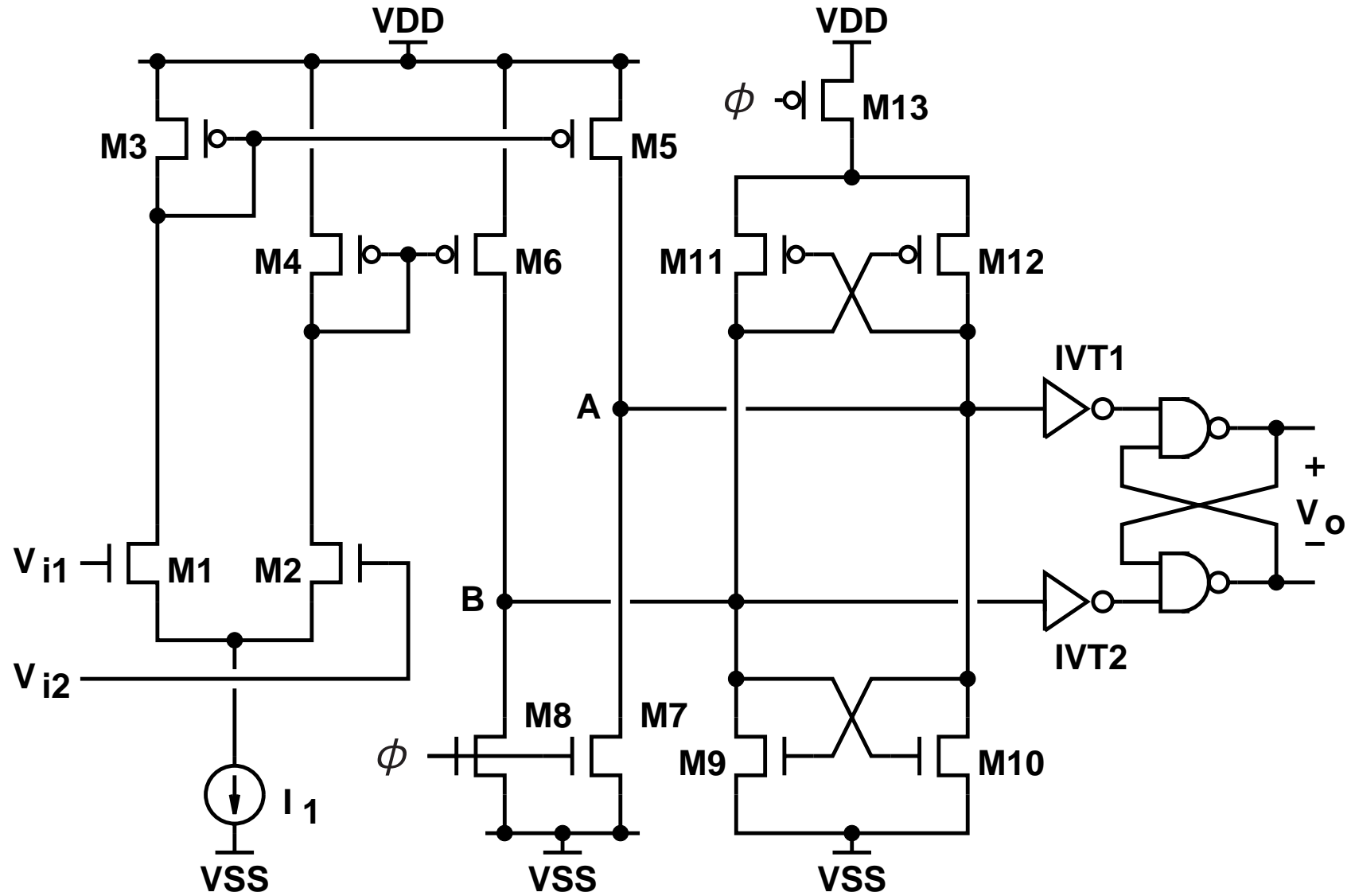
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- During the track mode ( $\phi = 1$ ), want  $g_{m7,m8} < g_{m9,m10}$  so that the combination of M7-M8 and M9-M10 pair become the resistive loads for M5 and M6. The small-signal voltage gain is

$$\frac{V_o}{V_i} \approx \frac{g_{m1}}{g_{m9} - g_{m7}} \cdot \frac{(W/L)_6}{(W/L)_4}$$

- During the latch mode ( $\phi = 0$ ), M7, M8, and M11 must be large enough to prevent the change of latched state by the  $V_i$  variation.
- All nodes are low impedance, thus giving fast operation.
- Overdrive recovery can be improved by adding an equalizing switch between the  $V_o$  nodes.
- The preamplifier buffers the kickback from the input circuitry.
- Reference: B. Song, et al., JSSC, 12/90, pp. 1328–1338.

# MOST Comparator: Preamp + Regenerative Sense Amplifier



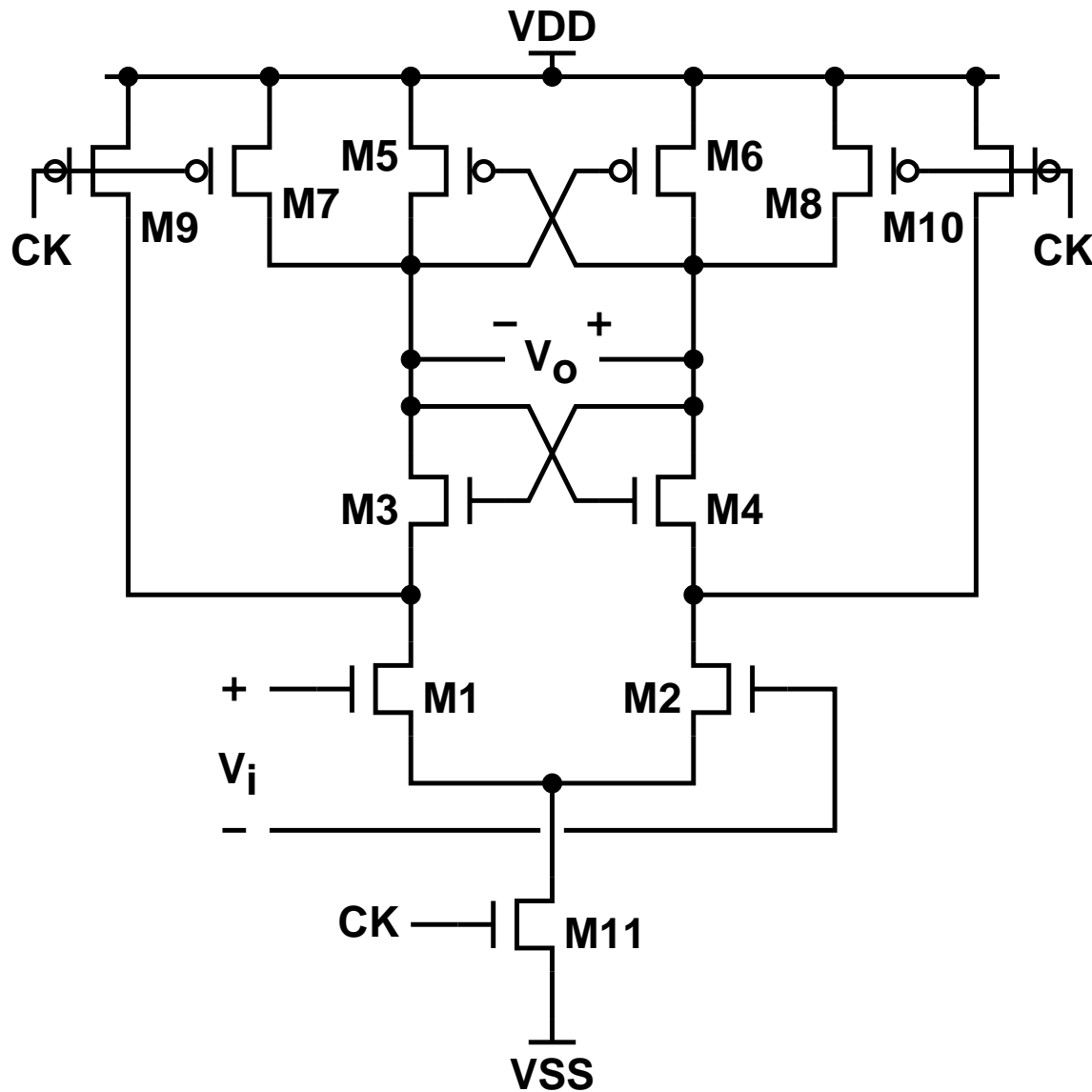
# MOST Comparator: Preamp + Regenerative Sense Amplifier

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- During the track mode ( $\phi = 1$ ), need M7 and M8 large enough to overpower the M9-M10 cross-coupled pair and pull  $V_A$  and  $V_B$  below the input threshold level of IVT1 and IVT2.
- During the latch mode ( $\phi = 0$ ), the M9-M10 and M11-M12 pairs provide regeneration. They must be large enough to prevent the change of latched state by the  $V_i$  variation.

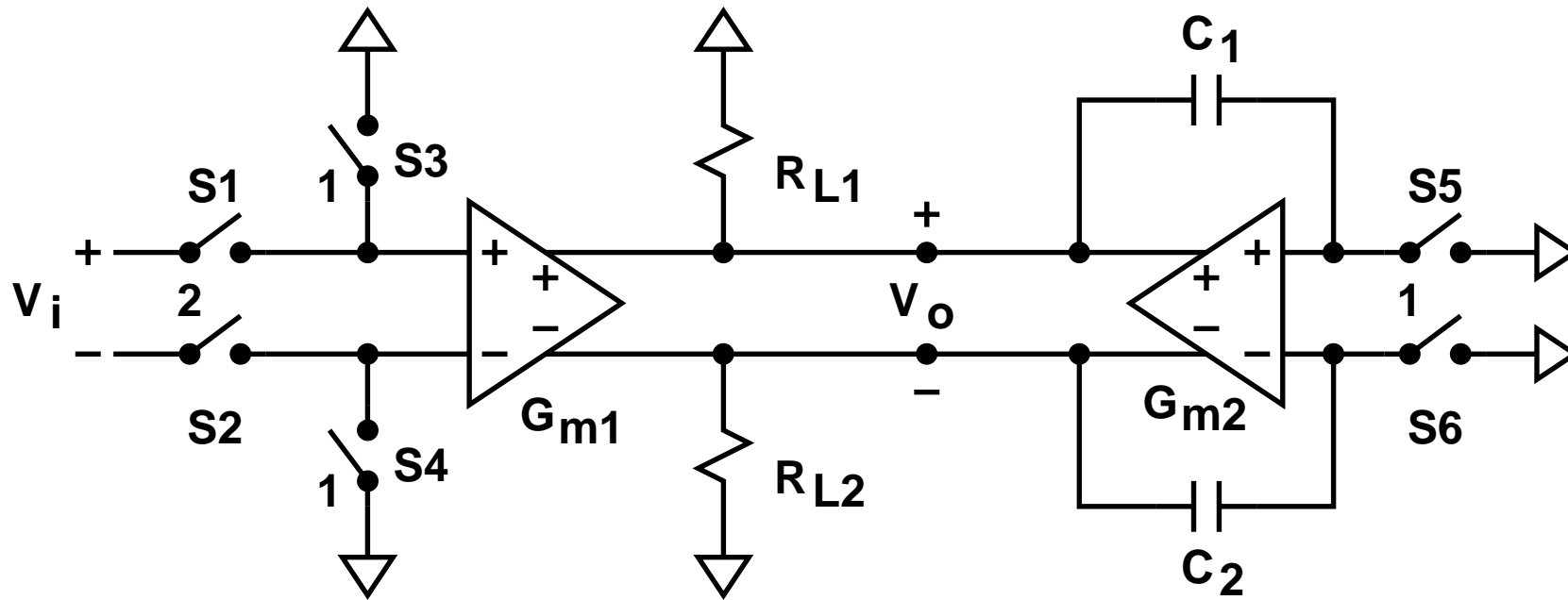
The input threshold level of IVT1 and IVT2 must be high enough to avoid false triggering.

# MOST Comparator: Merged Preamp + Sense Amplifier



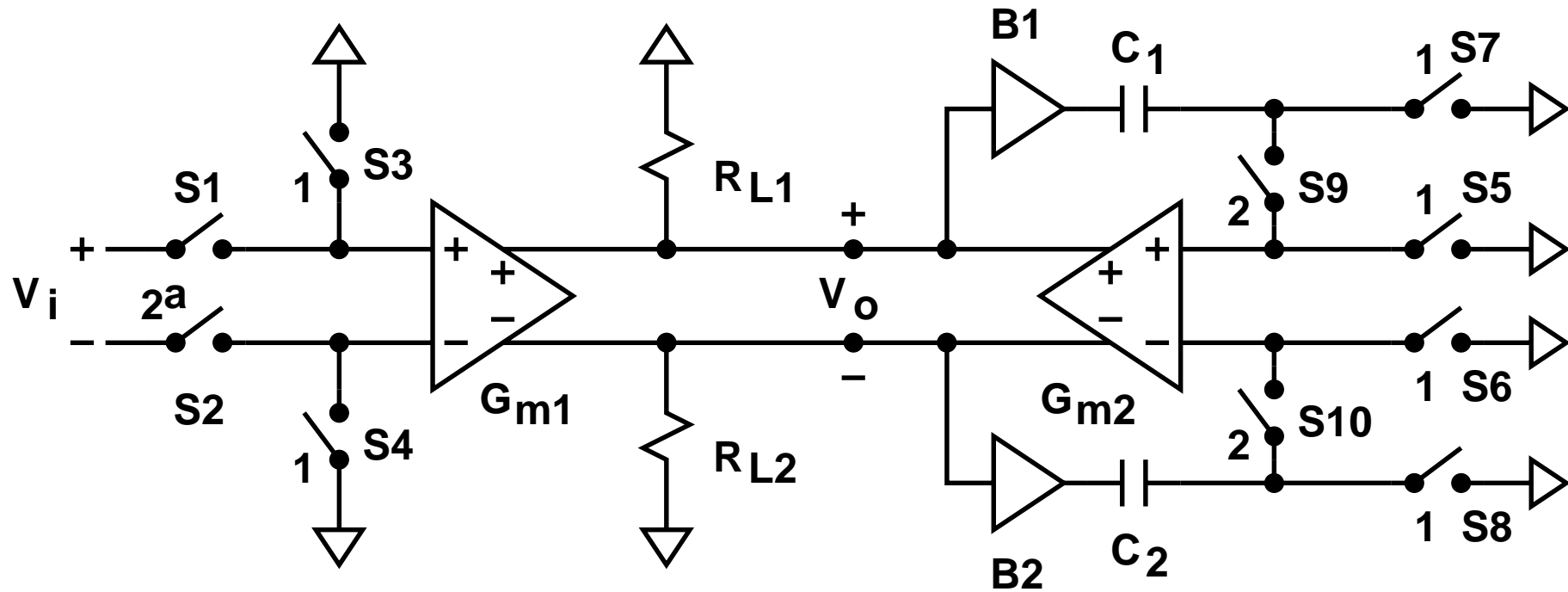
- No power dissipation when  $CK=0$ .
- When  $CK=1$ , the M1-M2 pair is activated first, the M3-M4 pair is second, and the M5-M6 pair is the last.
- Kickback noise is generated at input during the 0-to-1 transition of CK.
- Reference: B. Razavi, 1999 ISSCC Short Course.

## Offset Canceled Latches: Idea



- During reset mode ( $\phi_1 = 1$ ), the OOS is applied to both  $G_{m1}$  and  $G_{m2}$ .
- During reset mode, the finite on-resistance of S5 and S6 may cause oscillation.
- During reset-to-regeneration transition, any mismatch of the switching errors between S5 and S6 can trigger a false regeneration, yielding a large input-referred offset.

# Offset Canceled Latches: Simplified Schematic

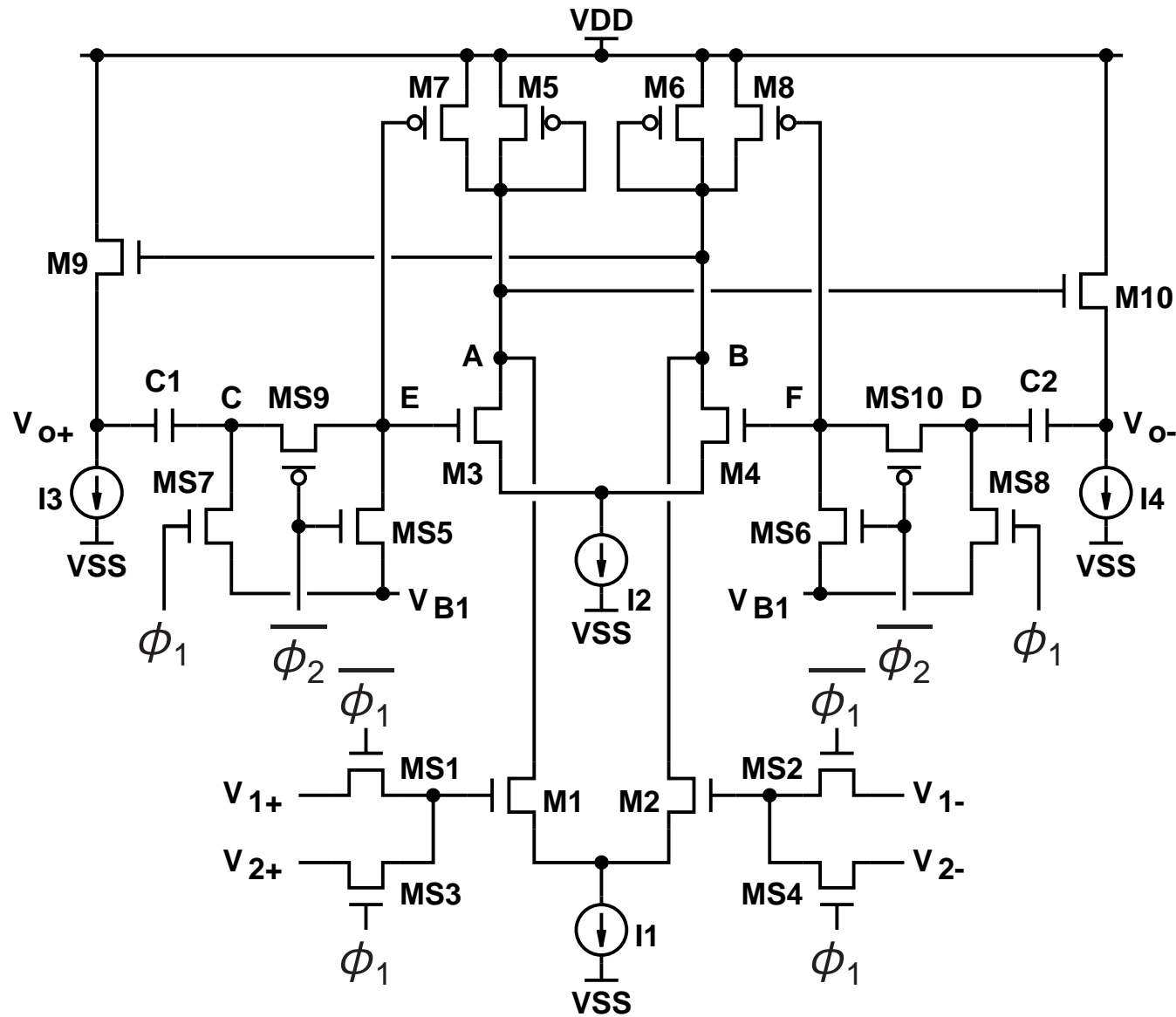


## Offset Canceled Latches: Simplified Schematic

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- During reset mode, the positive feedback loop is completely broken.
- The regeneration begins only after  $V_i$  has been sensed and amplified.
- Buffers B1 and B2 isolate output nodes from  $C_1$  and  $C_2$ , thus enhancing regeneration speed.
- The residual offset is primarily caused by the switching errors of S5–S10.
- Reference: B. Razavi, et al., “*Design Techniques for High-Speed High-Resolution Comparators*,” JSSC, 12/92, pp. 1916–1926.

# Offset Canceled Latches: MOST Implementation



# Offset Canceled Latches: MOST Implementation

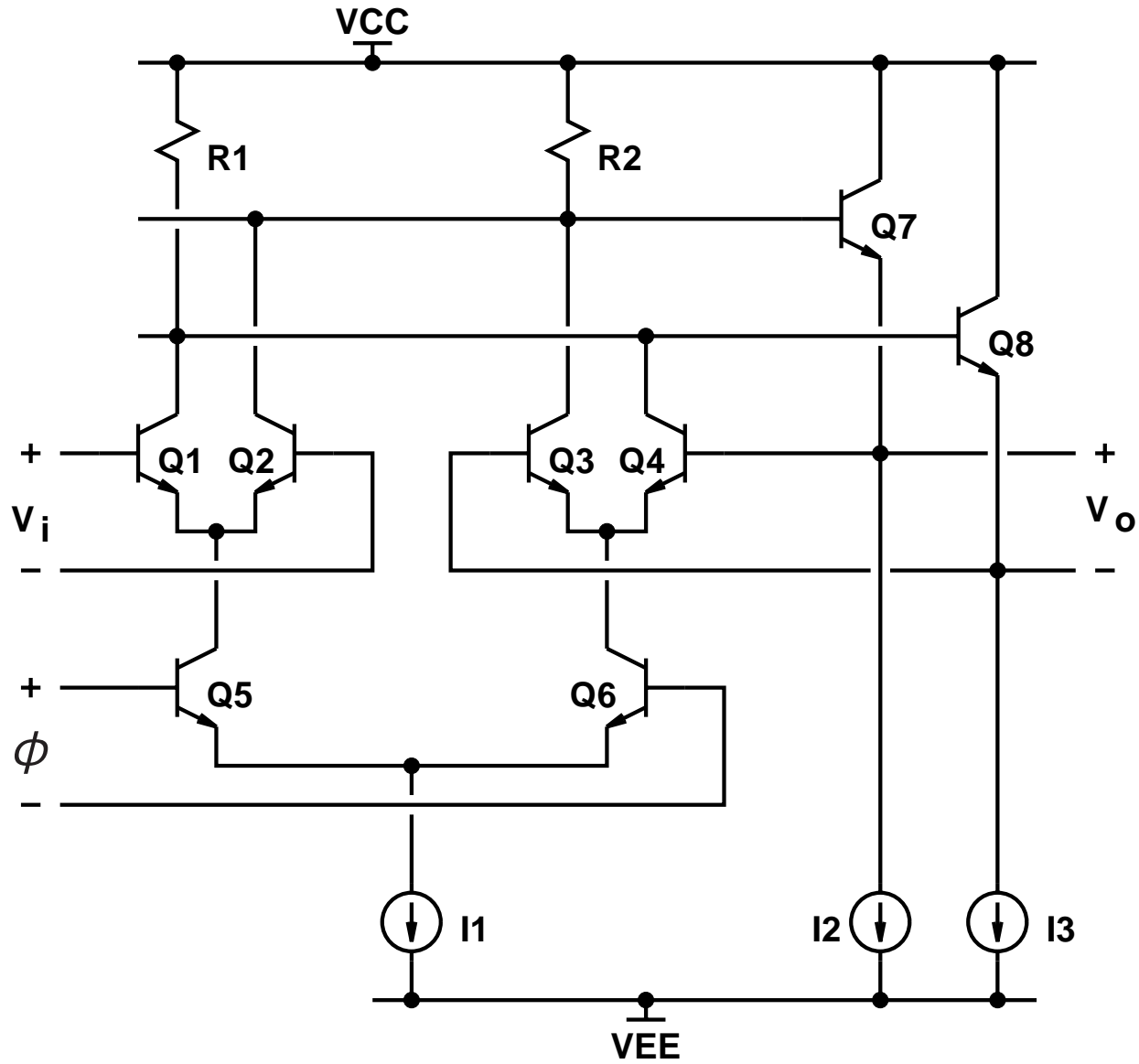
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- M7 and M8 are active loads, which both decrease the voltage drops across M5 and M6, increase available gain, increase  $V_o$  output swing, and enhance speed.
- An equalizing switch driven by  $\phi_1^d$  can be placed between node C and D to eliminate the switching error mismatch between MS7 and MS8.
- An equalizing switch driven by  $\phi_2^d$  can be placed between node E and F to eliminate the mismatch between MS5 and MS6. In this case, MS9 and MS10 are driven by  $\phi_2^{dd}$  and the charge absorption mismatch between MS9 and MS10 becomes the only significant contribution to the offset, which is

$$V_{OS(in)} = \frac{\Delta Q}{C} \cdot \frac{g_{m3} + g_{m7}}{g_{m1}}$$

- Reference: B. Razavi, JSSC, 12/92, pp. 1916–1926.

# BJT Latched Comparator

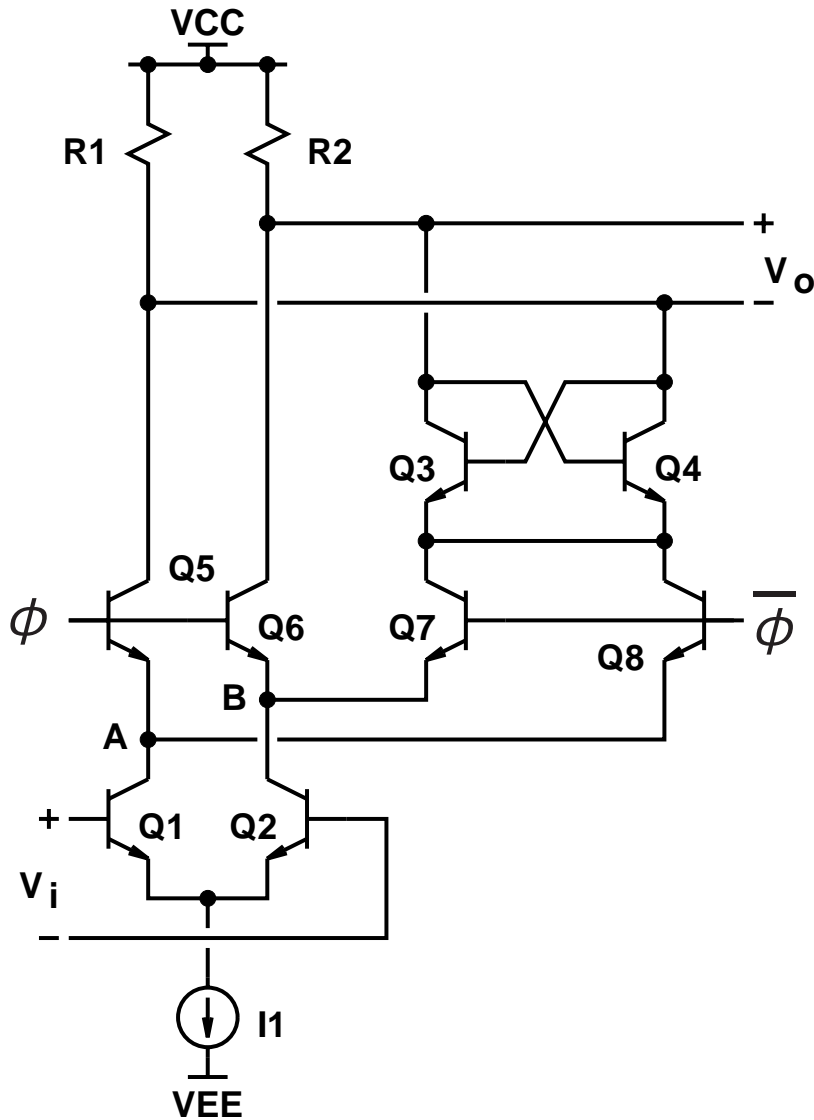


# BJT Latched Comparator

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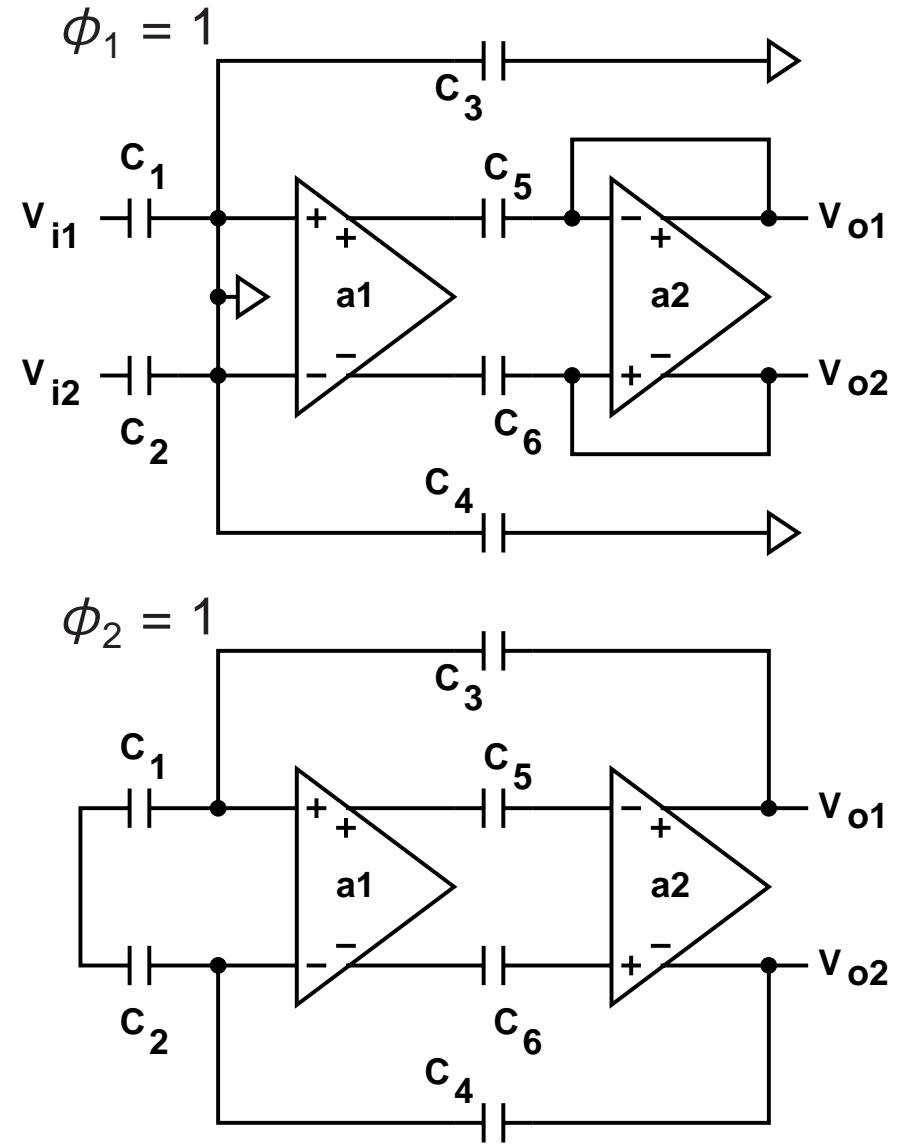
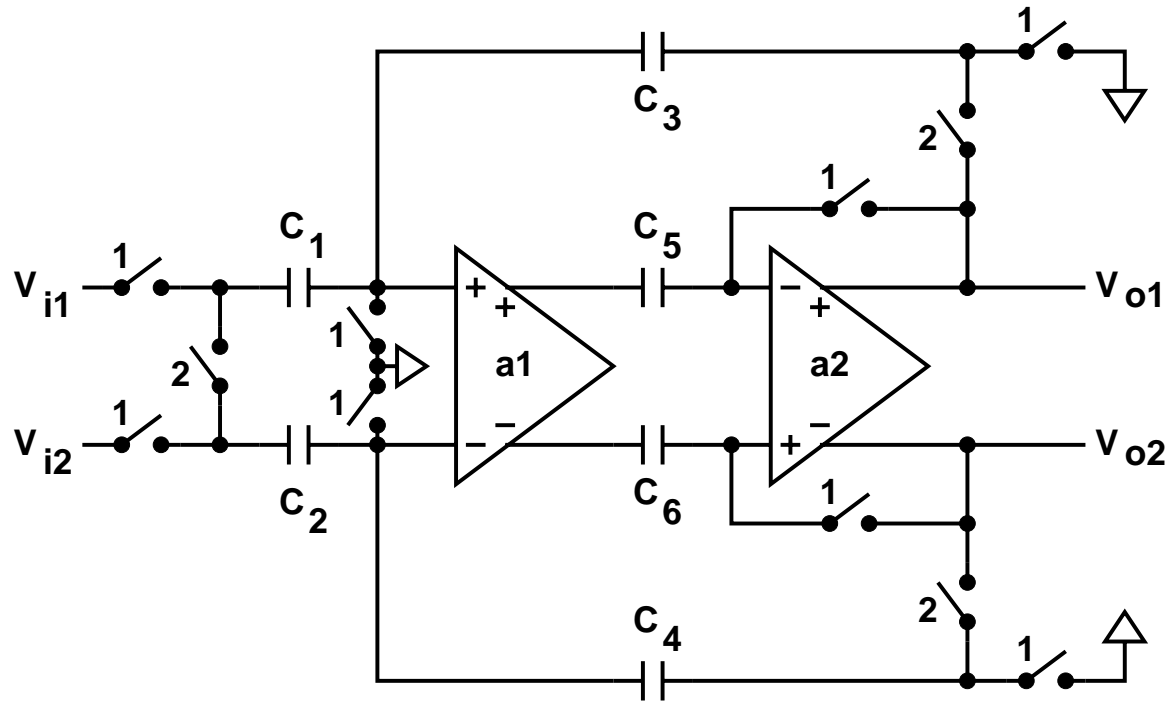
- During the track mode ( $\phi = 1$ ), the variation of input capacitance with  $V_i$  causes input-dependent delay and hence harmonic distortion.
- Speed may be limited by overdrive recovery.
- During latch-to-track transition, Q1 and Q2 are initially off, the I1 current then flows through Q5 and the emitter junctions of Q1 and Q2 to the input, creating kickback noise.
- Usually preceded by a buffer.

# BJT Comparator with High-Level Latch



- During the latch mode ( $\phi = 0$ ), the variation in  $V_i$  will not disturb the latched state.
- Q1 and Q2 are never turned off, thus reducing kickback noise.
- The kickback noise results only from the transients at nodes A and B. Adding a resistor between A and B decreases these transient and improves the recovery at these node.

# A Sampled-Data Amplifier with Internal Offset Cancellation

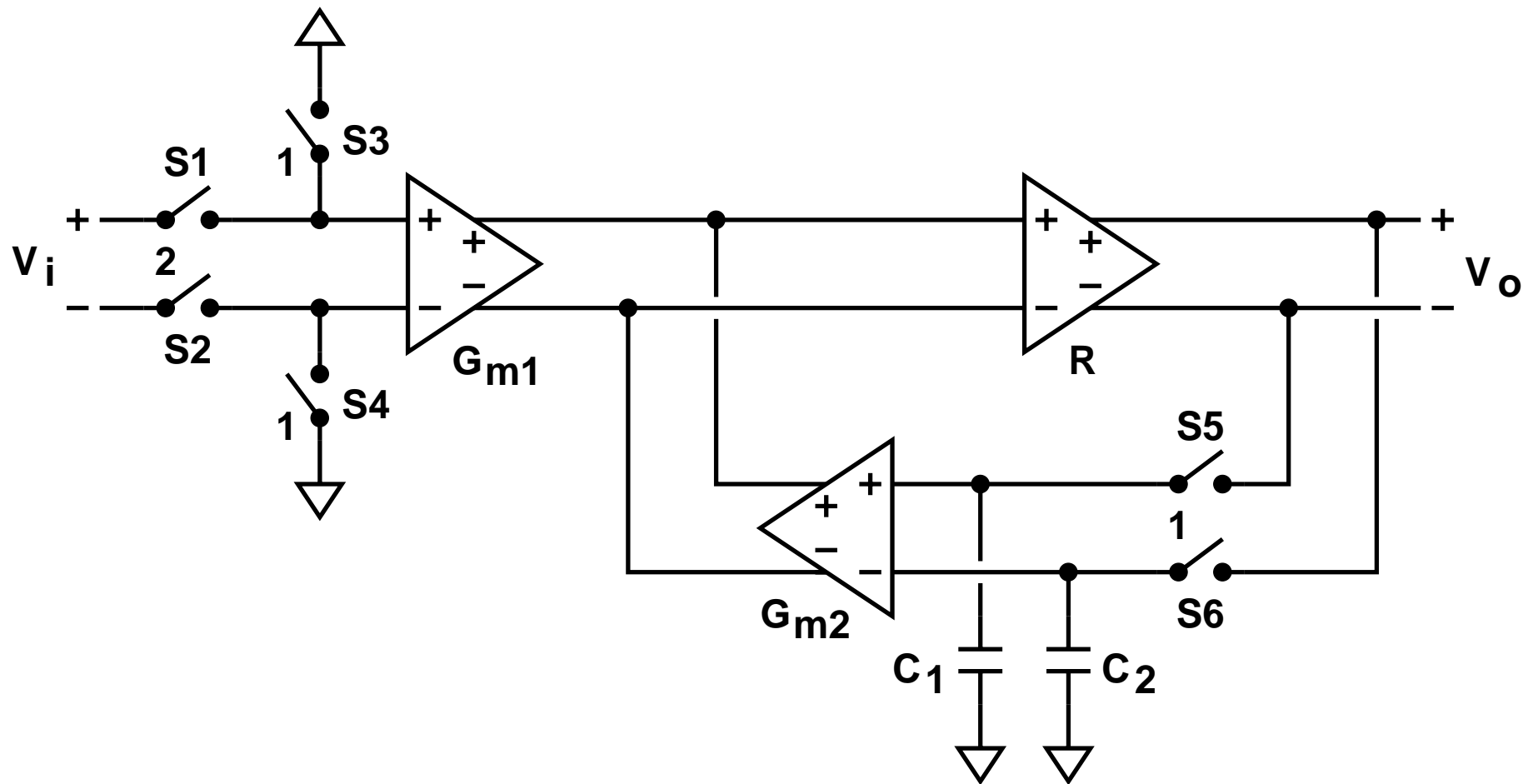


# A Sampled-Data Amplifier with Internal Offset Cancellation

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- During reset mode, OOS is applied to  $a1$  and IOS is applied to  $a2$ .  $a1$  is low gain and  $a2$  is high gain.
- The OOS and IOS perform *correlated double sampling (CDS)* so that the effect of  $1/f$  noise is also reduced.
- Additional capacitors in the signal path (i.e.,  $C_5$  and  $C_6$ ) can degrade the closed-loop settling behavior.
- Reference: Yen, JSSC, 12/82, pp. 1008–1013.

# Operational Amplifier with Offset Compensation



- The  $G_{m2}$  compensation circuit is not in the signal path. The original frequency/speed performance can be maintained.

# Operational Amplifier with Offset Compensation

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During the reset mode ( $\phi_1 = 1$ )

$$V_o = V_{OS1} \cdot G_{m1}R + (V_{OS2} - V_o) \cdot G_{m2}R$$
$$\Rightarrow V_o = \frac{V_{OS1} \cdot G_{m1}R + V_{OS2} \cdot G_{m2}R}{1 + G_{m2}R} \Rightarrow V_o \approx V_{OS1} \cdot \frac{G_{m1}}{G_{m2}} + V_{OS2} \quad \text{If } G_{m2}R \gg 1$$

- $V_{OS1}$  and  $V_{OS2}$  are the input-referred offset of the  $G_{m1}$ - $R$  and  $G_{m2}$ - $R$  pairs.

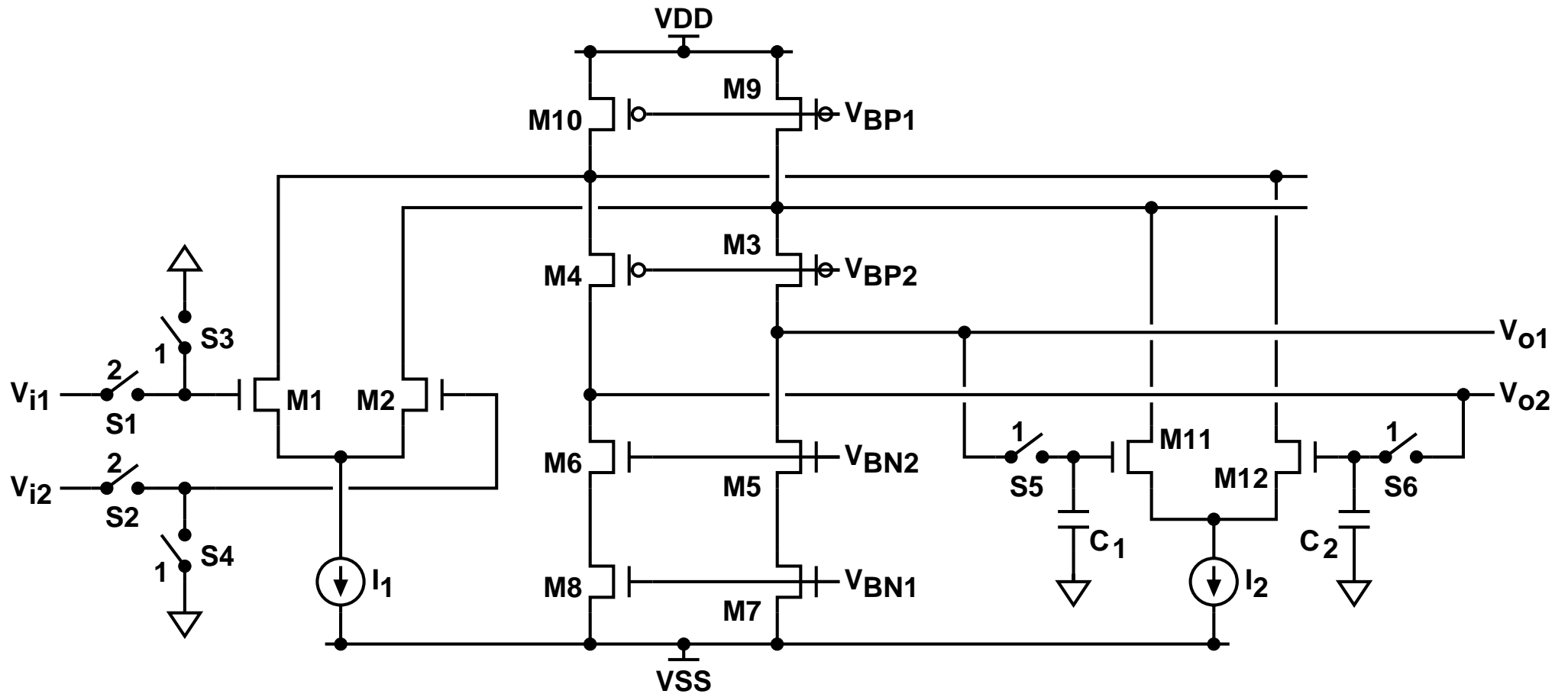
During the amplification mode ( $\phi_2 = 1$ )

$$V_o = V_i \cdot G_{m1}R + V_{OS1} \frac{G_{m1}}{G_{m2}} + V_{OS2} + \Delta V \cdot G_{m2}R = G_{m1}R \left( V_i + \frac{V_{OS1}}{G_{m2}R} + \frac{V_{OS2}}{G_{m1}R} + \Delta V \frac{G_{m2}}{G_{m1}} \right)$$

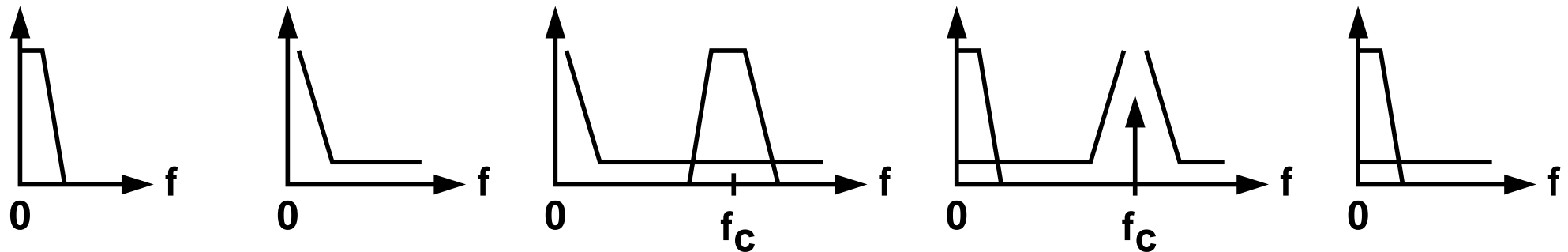
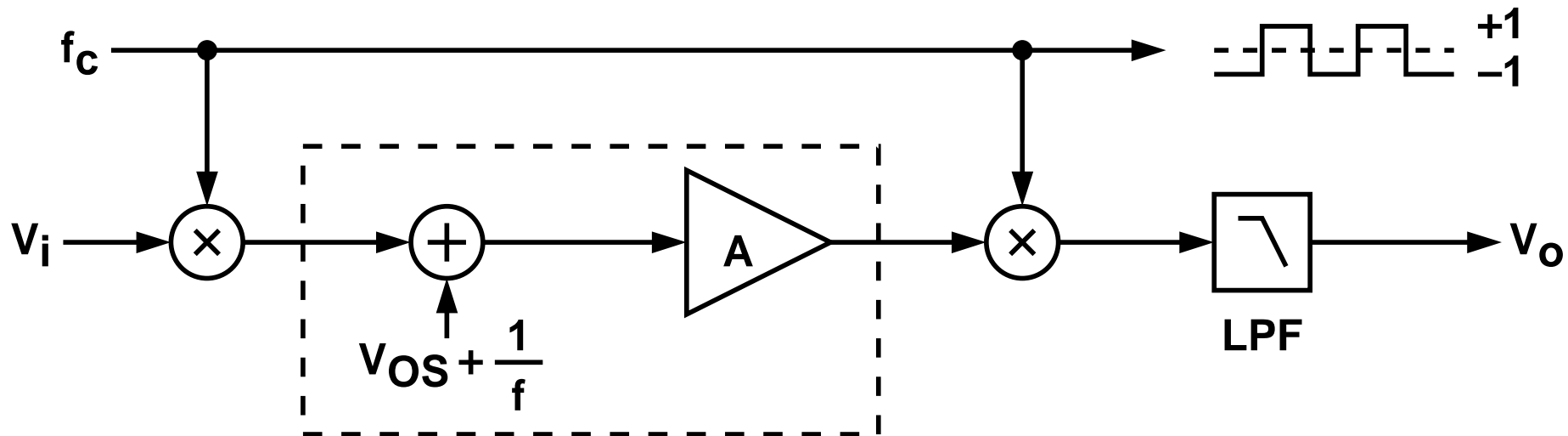
$$\text{Input-Referred Offset} = V_{OS,in} = \frac{V_{OS1}}{G_{m2}R} + \frac{V_{OS2}}{G_{m1}R} + \Delta V \cdot \frac{G_{m2}}{G_{m1}}$$

- $\Delta V$  is due to the mismatch between the switching errors of S5 and S6. Its effect on  $V_o$  can be reduced by making  $G_{m2}/G_{m1}$  small.

# Operational Amplifier with Offset Compensation

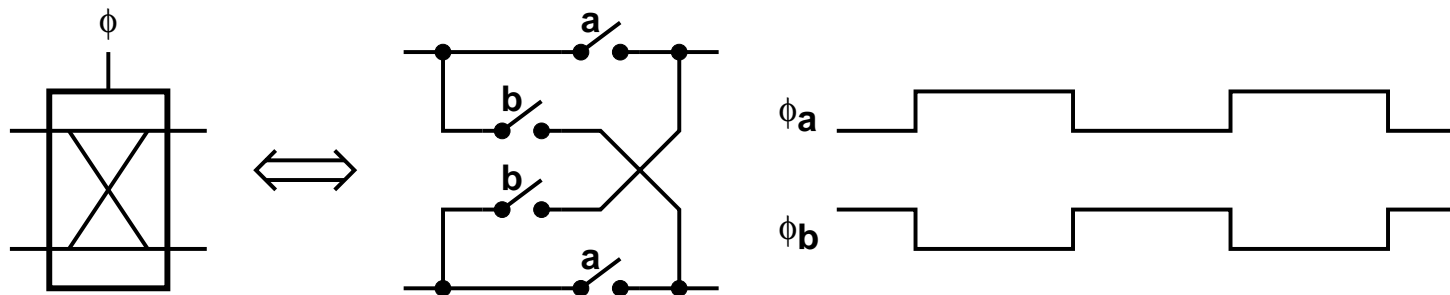
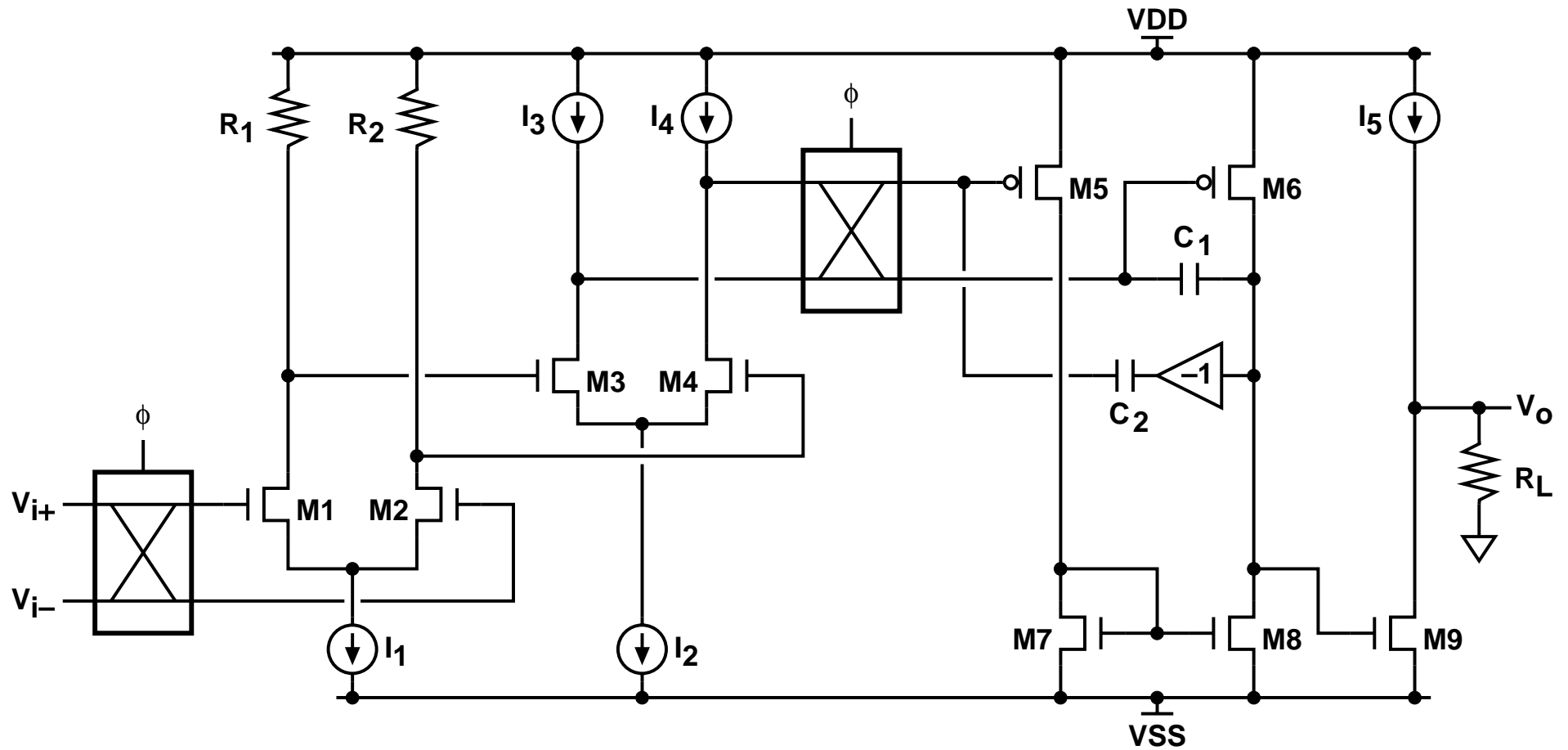


# The Chopper Stabilization Technique



- The bandwidth of the amplifier  $A$  must be wider than  $f_c$ .
- The amplifier  $A$  should employ design of minimizing thermal noise.

# A Chopper Operational Amplifier

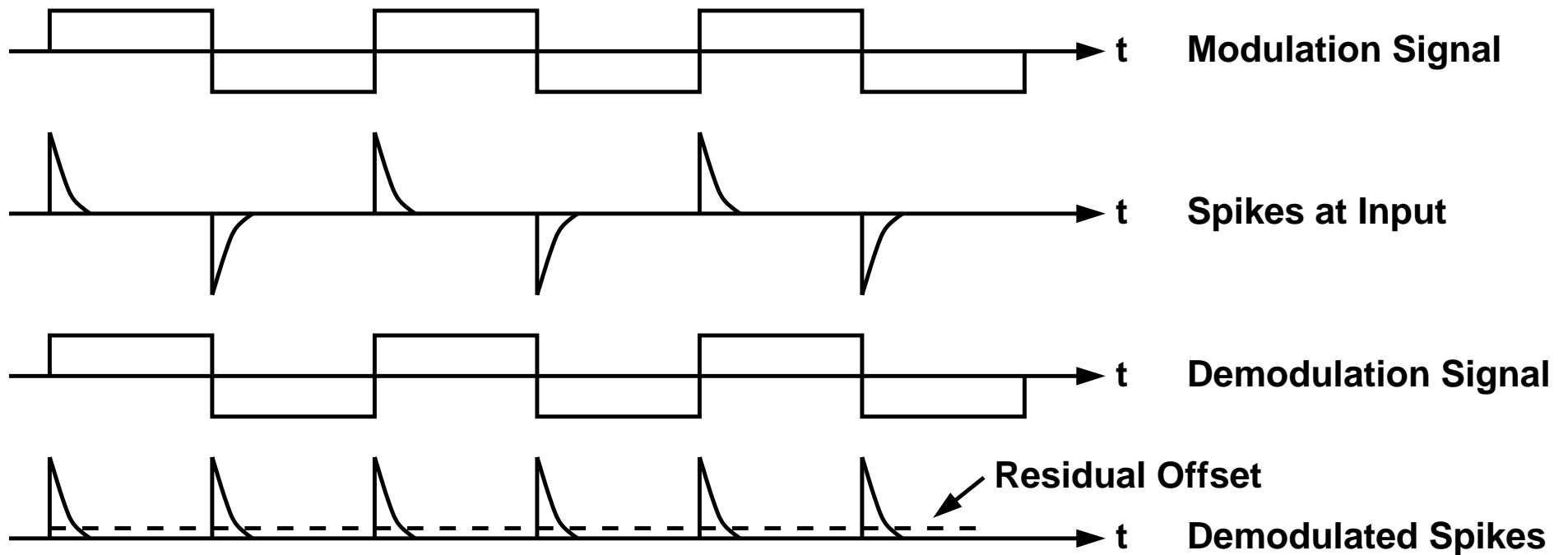
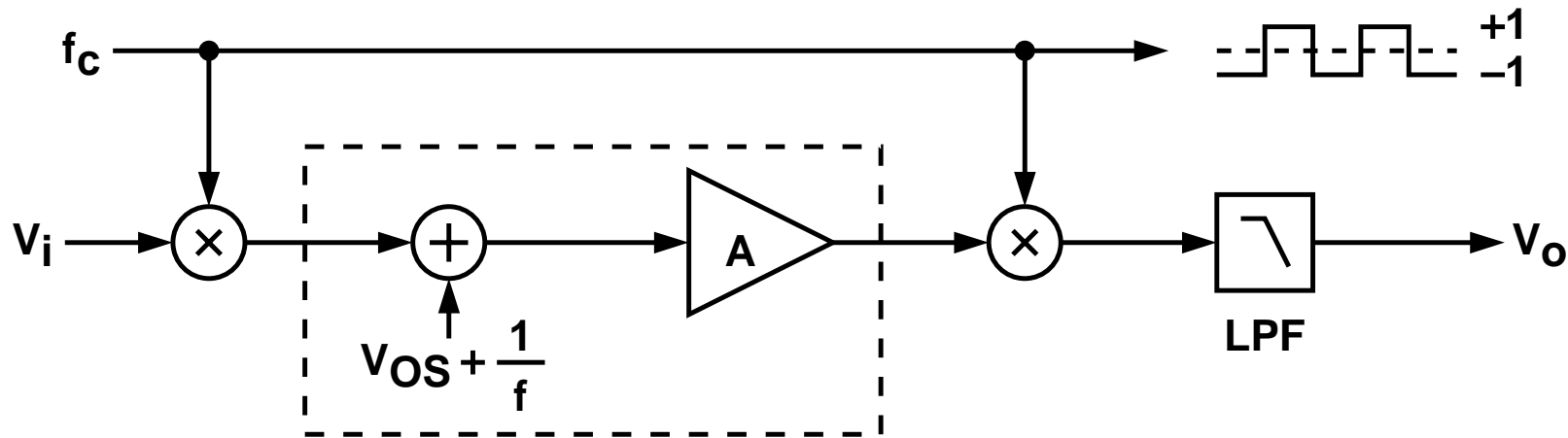


# A Chopper Operational Amplifier

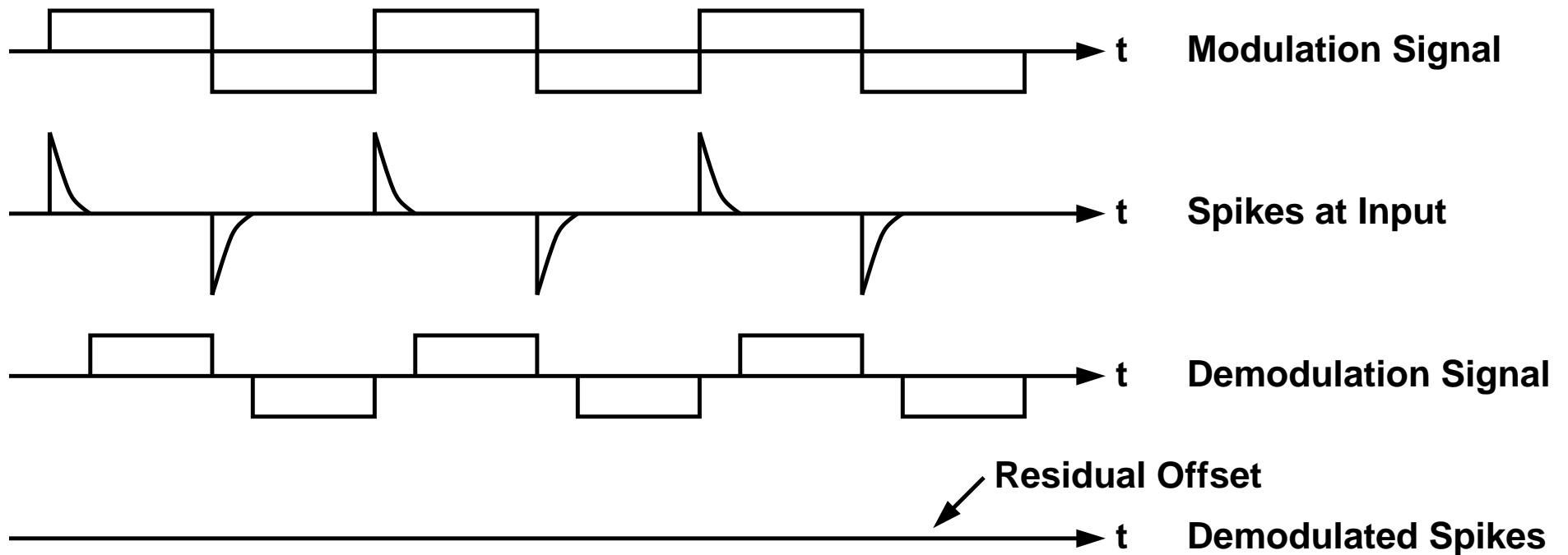
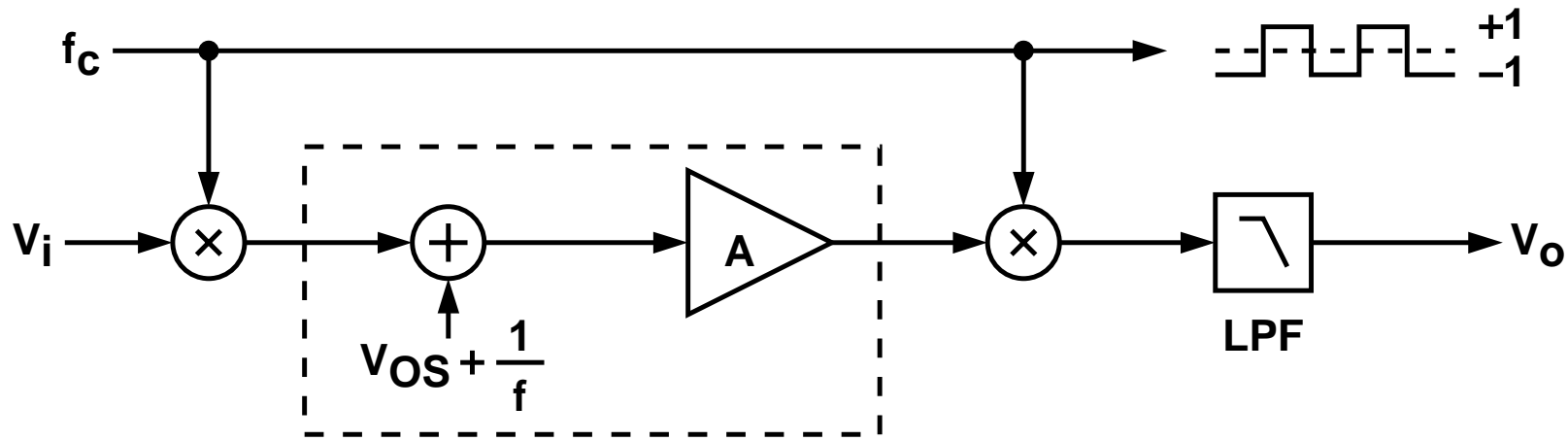
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- The M1–M2 is a low-gain low-noise stage.
- The M3–M4 is a high-gain stage with low  $G_m$ . A common-mode feedback circuit is required to stabilize the drain voltages of M3 and M4.
- The M5–M8 is a high-gain Miller stage for frequency compensation and low-pass filter.
- The M9 is a low-gain buffer stage.
- The chopper can introduce additional  $kT/C$  noise.
- Reference: A. Bakker, et al., “A CMOS Nested-Chopper Instrumentation Amplifier with 100-nV Offset,” JSSC 12/2000, pp. 1877–1883.
- Reference: C. Enz and G. Temes, “Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization,” Proc. IEEE, 11/1996, pp. 1584–1614.

# Residual Offset of Chopper Amplifier



# Chopper Modulation with Guard Time



# Chopper Modulation with Guard Time

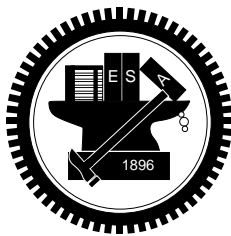
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- The spikes at the input is due to the switching error mismatch of the chopper.
- The residual offset is linear dependent on chopper frequency.
- Reference: Q. Huang and C. Menolfi, “A 200nV Offset 6.5nV/ $\sqrt{\text{Hz}}$  Noise PSD 5.6kHz Chopper Instrumentation Amplifier,” ISSCC 2002.

# Oscillators

Jieh-Tsorng Wu

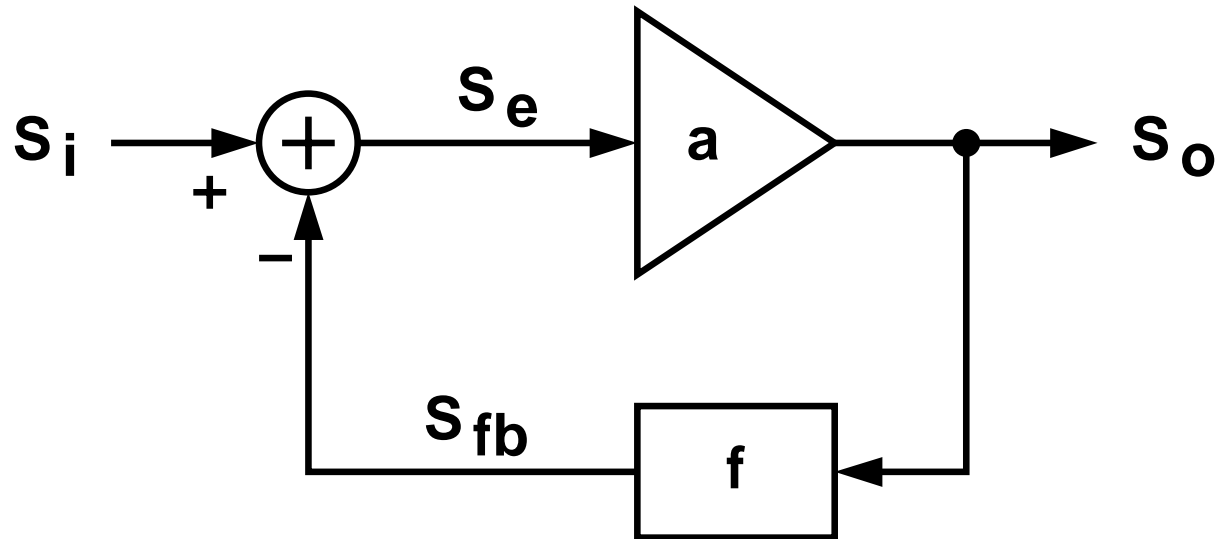
October 16, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# The Barkhausen Criteria

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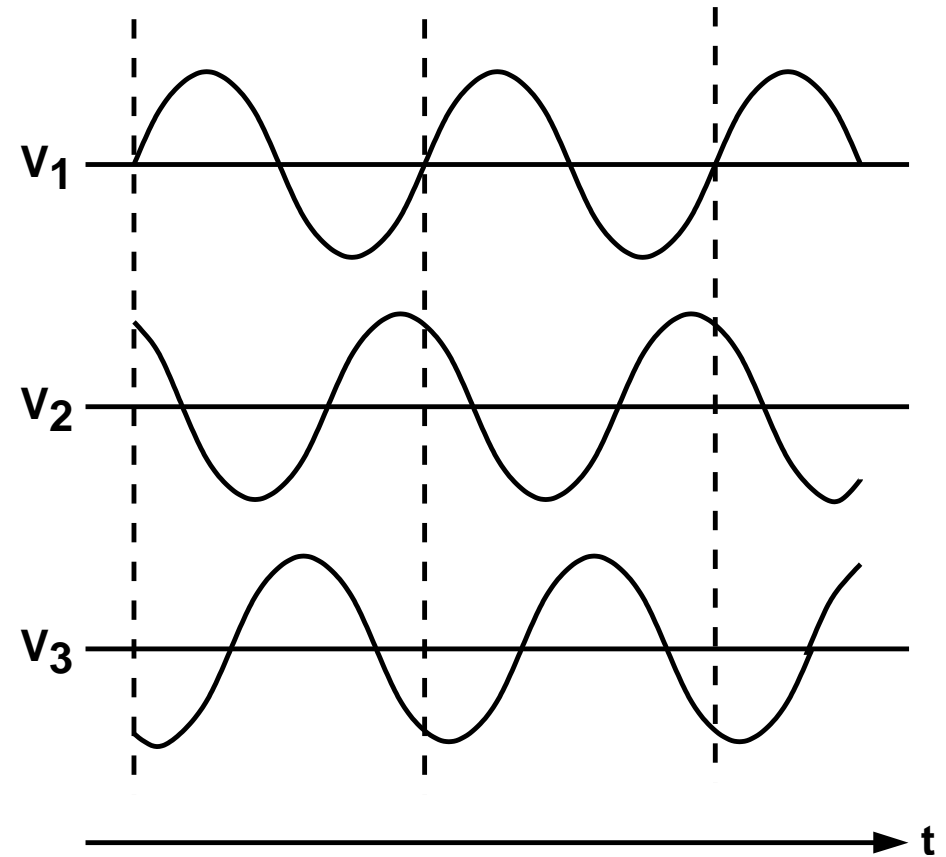
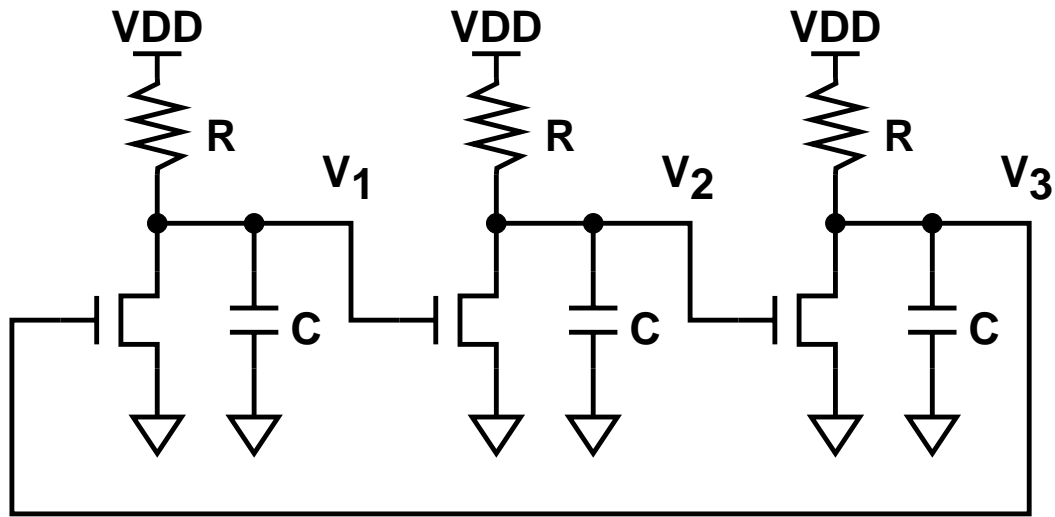
$$S_o = a \cdot S_e \quad S_{fb} = f \cdot S_o \quad S_e = S_i - S_{fb}$$

$$\text{Closed-Loop Gain} = A \equiv \frac{S_o}{S_i} = \frac{a}{1 + af} = \frac{a}{1 + T} \quad \text{Loop Gain} = T \equiv a \times f$$

The feedback system oscillates at  $\omega_o$ , if

$$|T(j\omega_o)| \geq 1 \quad \angle T(j\omega_o) = 180^\circ$$

# Three-Stage Ring Oscillator



$$-T(s) = \left[ -\frac{g_m R}{1 + sRC} \right]^3 = -\frac{A_0^3}{\left(1 + \frac{s}{\omega_p}\right)^3}$$

$$A_0 = g_m R \quad \omega_p = \frac{1}{RC}$$

# Three-Stage Ring Oscillator

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From the Barkhausen criteria,

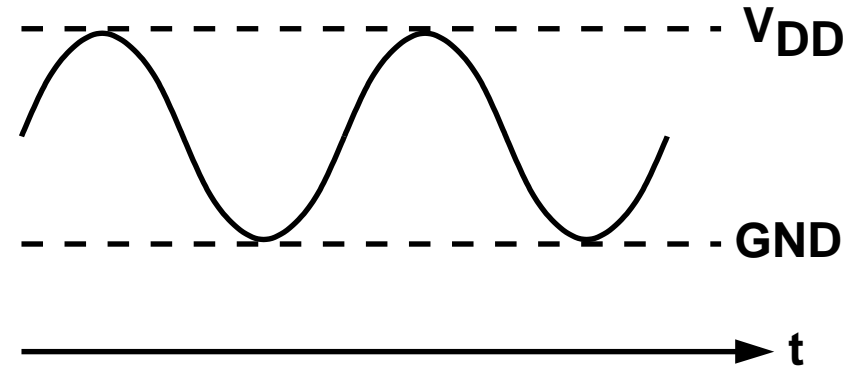
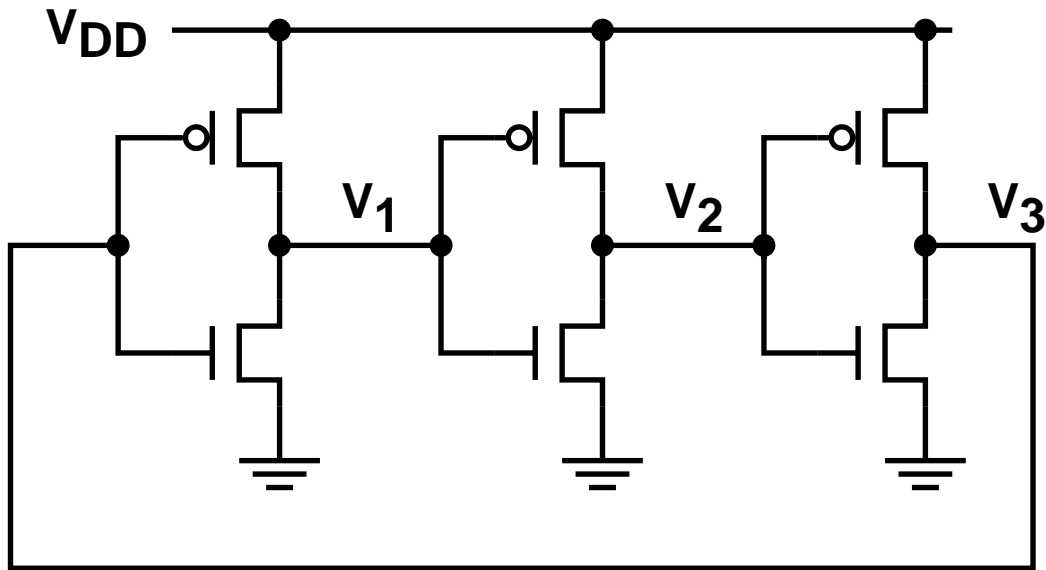
$$\tan^{-1} \left( \frac{\omega_o}{\omega_p} \right) = 60^\circ \quad \Rightarrow \quad \omega_o = \sqrt{3}\omega_p$$

$$\frac{A_0^3}{\left[ \sqrt{1 + \left( \frac{\omega_o}{\omega_p} \right)^2} \right]^3} = 1 \quad \Rightarrow \quad A_0 = g_m R = 2$$

- The phase difference between the neighboring nodes is  $180^\circ + 60^\circ = 240^\circ$ .
- If  $A_0 > 2$ , the oscillation amplitude increase exponentially until nonlinear effect limits the growth.

$$V(t) \propto \exp \left( \frac{A_0 - 2}{2} \omega_p t \right) \cos \left( \frac{A_0}{2} \omega_o t \right)$$

# Three-Stage CMOS Inverter Ring Oscillator

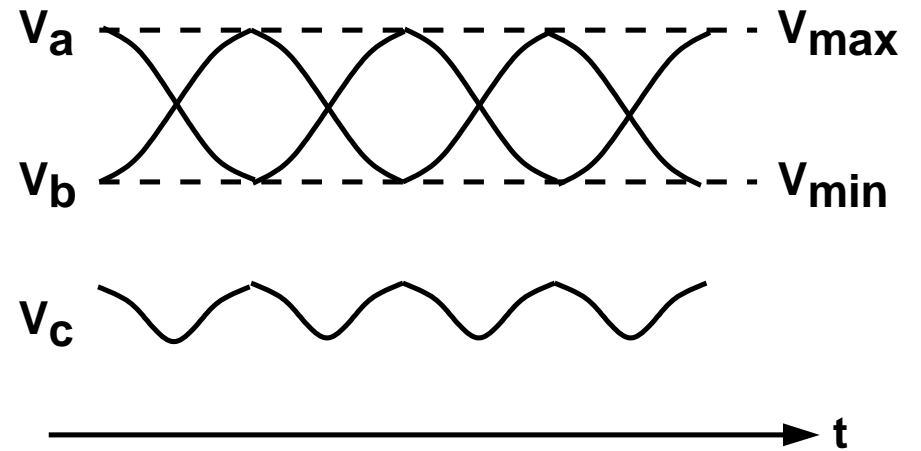
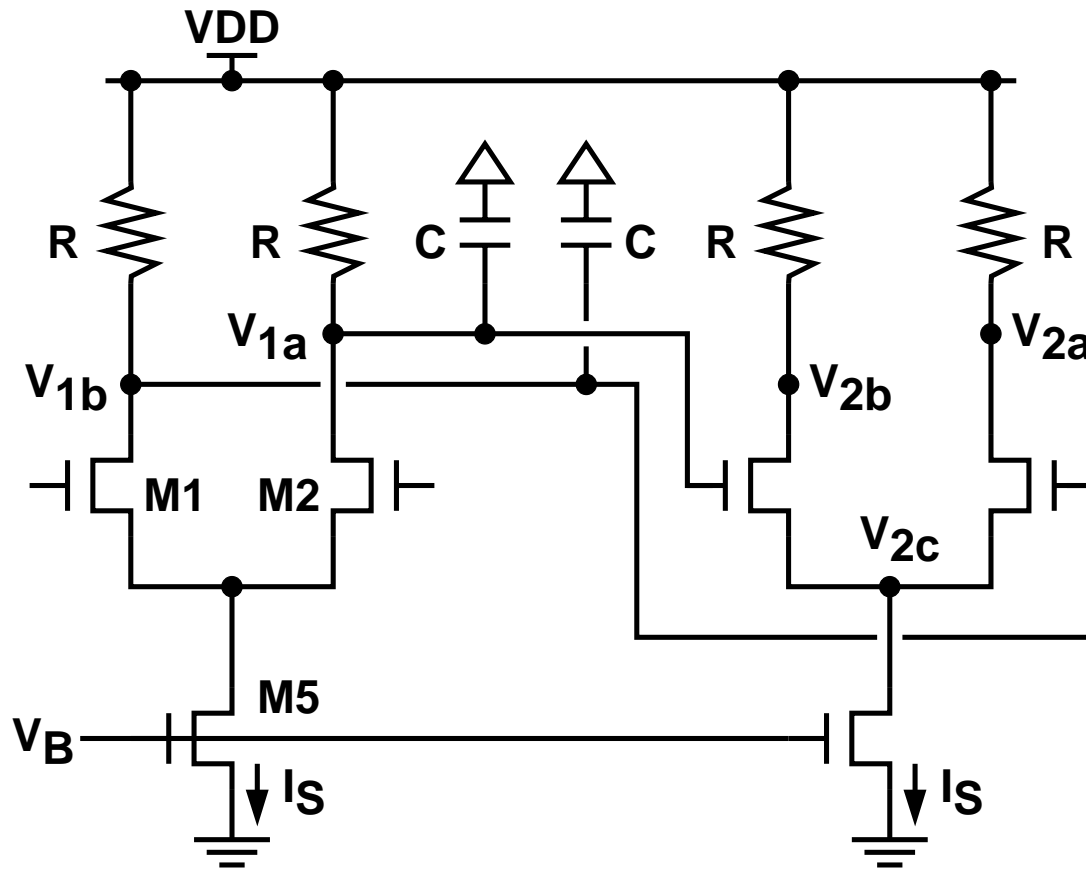
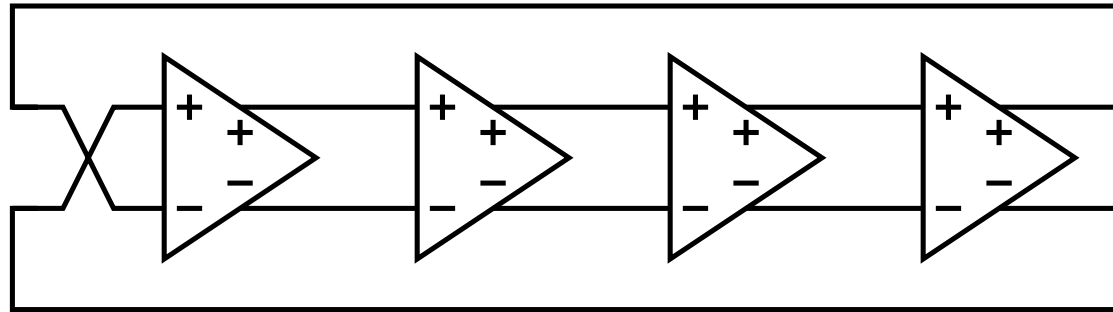


$$f_o = \frac{1}{6t_p} \quad t_p = \frac{1}{2} (t_{pHL} + t_{pLH}) = \frac{1}{2} (0.69R_{eqn}C + 0.69R_{eqp}C)$$

$$R_{eq} = \frac{-1}{V_{DD}/2} \int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}(1 + \lambda V)} dV \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{7}{9} \lambda V_{DD} \right)$$

- The oscillation frequency  $f_o$  can be varied by changing  $V_{DD}$ .

# Four-Stage Differential Ring Oscillator



# Four-Stage Differential Ring Oscillator

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From the Barkhausen criteria,

$$\tan^{-1} \left( \frac{\omega_o}{\omega_p} \right) = 45^\circ \quad \omega_p = RC \quad \Rightarrow \quad \omega_o = \omega_p$$
$$\frac{A_0^4}{\left[ \sqrt{1 + \left( \frac{\omega_o}{\omega_p} \right)^2} \right]^4} = 1 \quad \Rightarrow \quad A_0 = g_m R = \sqrt{2}$$

The delay stage is usually designed to experience complete switching, i.e.,

$$V_{max} = V_{DD} \quad V_{min} = V_{DD} - I_S R \quad \Delta V = V_{max} - V_{min} = I_S R$$

# Differential Delay Stage

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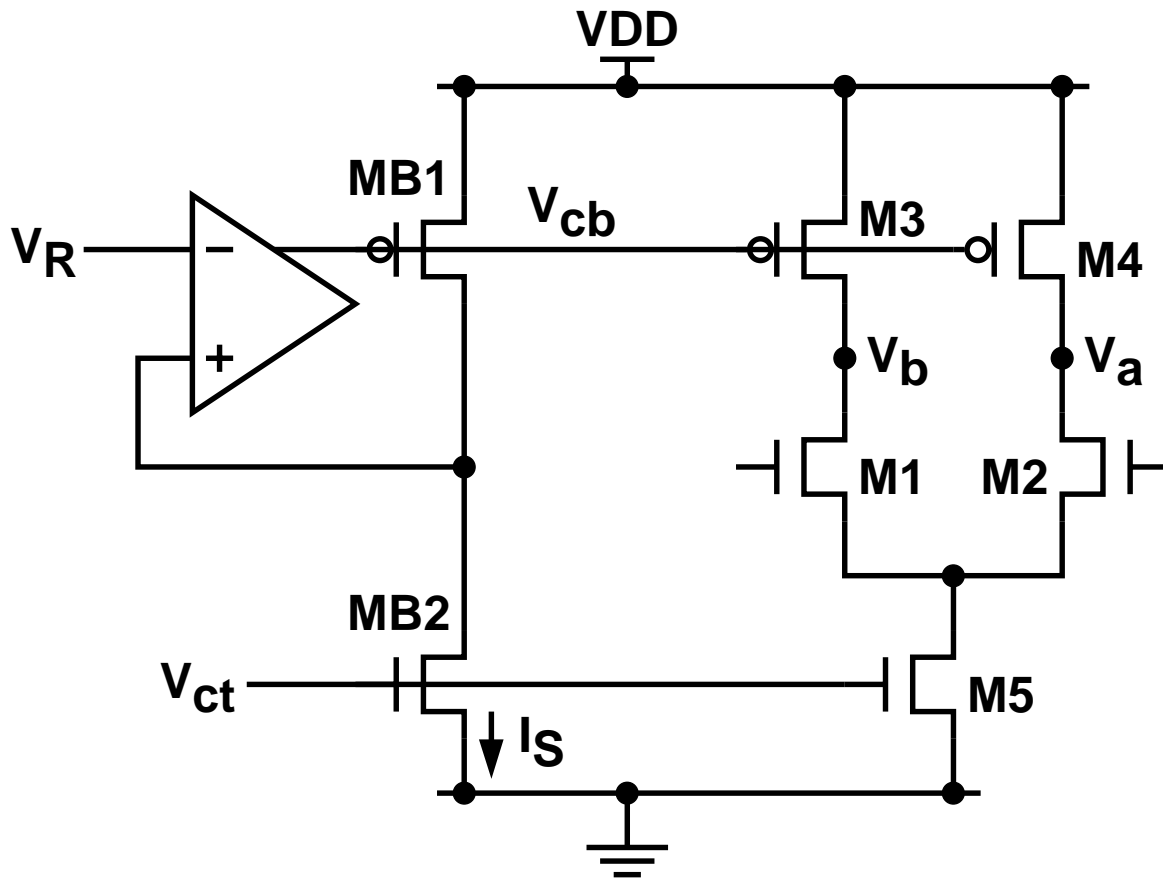
Let

$$\Delta V = I_S R \quad V_t = V_{t1} = V_{t2} \quad V_{ov} = V_{ov1} = V_{ov2} = \sqrt{\frac{2(I_S/2)}{\mu C_{ox}(W/L)_{1,2}}}$$

- To maintain M1 and M2 in the forward-active region,  $I_S R < V_{t1,2}$ .
- For complete switching, want  $\Delta V > \sqrt{2}V_{ov} \Rightarrow V_{ov} < \Delta V/\sqrt{2}$ .
- For enough loop gain, want  $g_m R = [(I_S/2)/(V_{ov}/2)] \cdot R > \sqrt{2} \Rightarrow V_{ov} < \Delta V/\sqrt{2}$ .
- The minimum  $V_{DD}$  can be approximated by

$$V_{DD,min} \approx V_{ov5} + V_t + V_{ov} + \frac{\Delta V}{2}$$

# Delay Variation Using Variable Resistors



MB1=M3=M4 and MB2=M5,

$$\Delta V = V_{DD} - V_R \approx I_S R_{on}$$

$$\omega_p = \frac{1}{R_{on} C} \approx \frac{I_S}{\Delta V \cdot C}$$

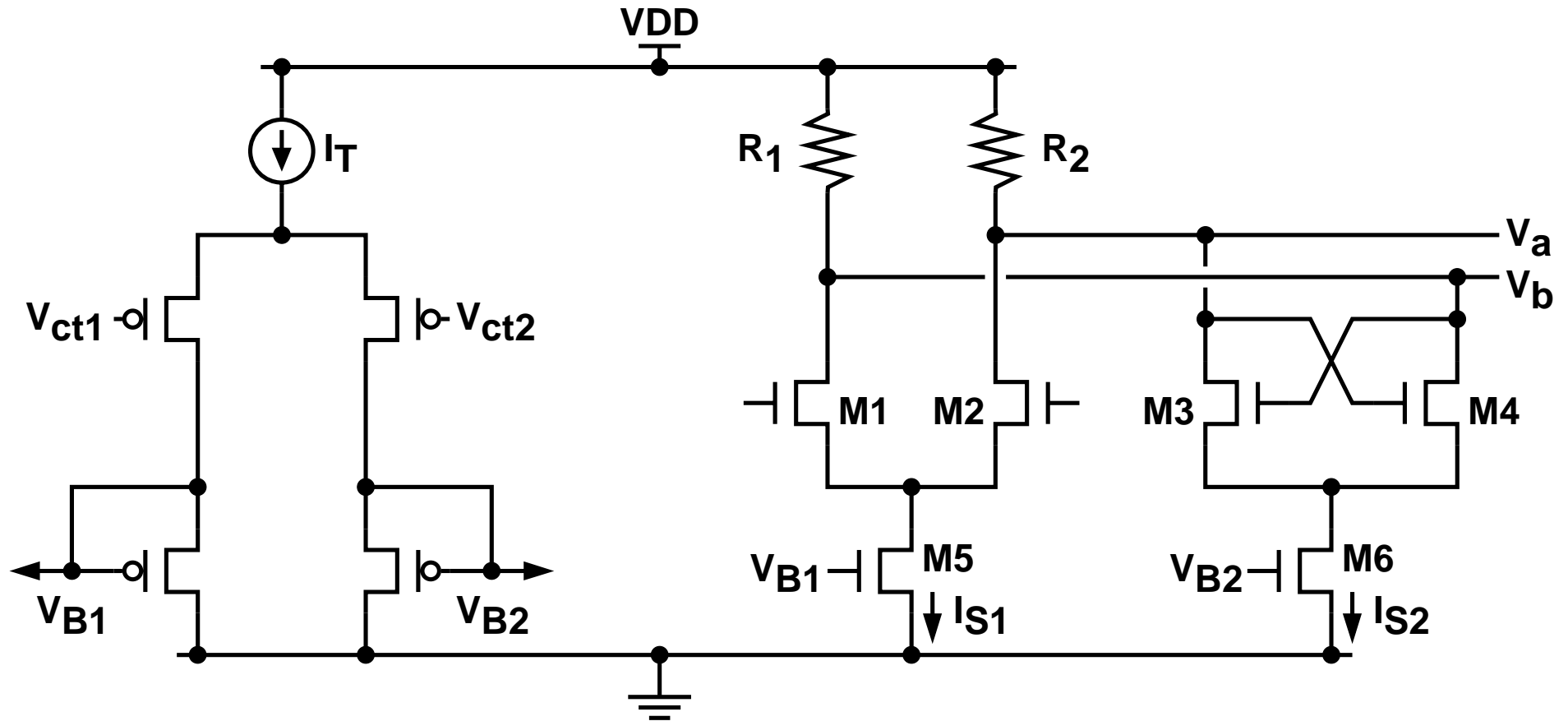
$$A_0 = g_{m1,2} R_{on}$$

$$= \frac{\Delta V}{I_S} \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2} I_S}$$

$$= \frac{\Delta V}{\sqrt{I_S}} \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right)_{1,2}}$$

- MB1, M3, and M4 are biased in the triode region.
- $A_0$  decreases at higher oscillation frequencies.

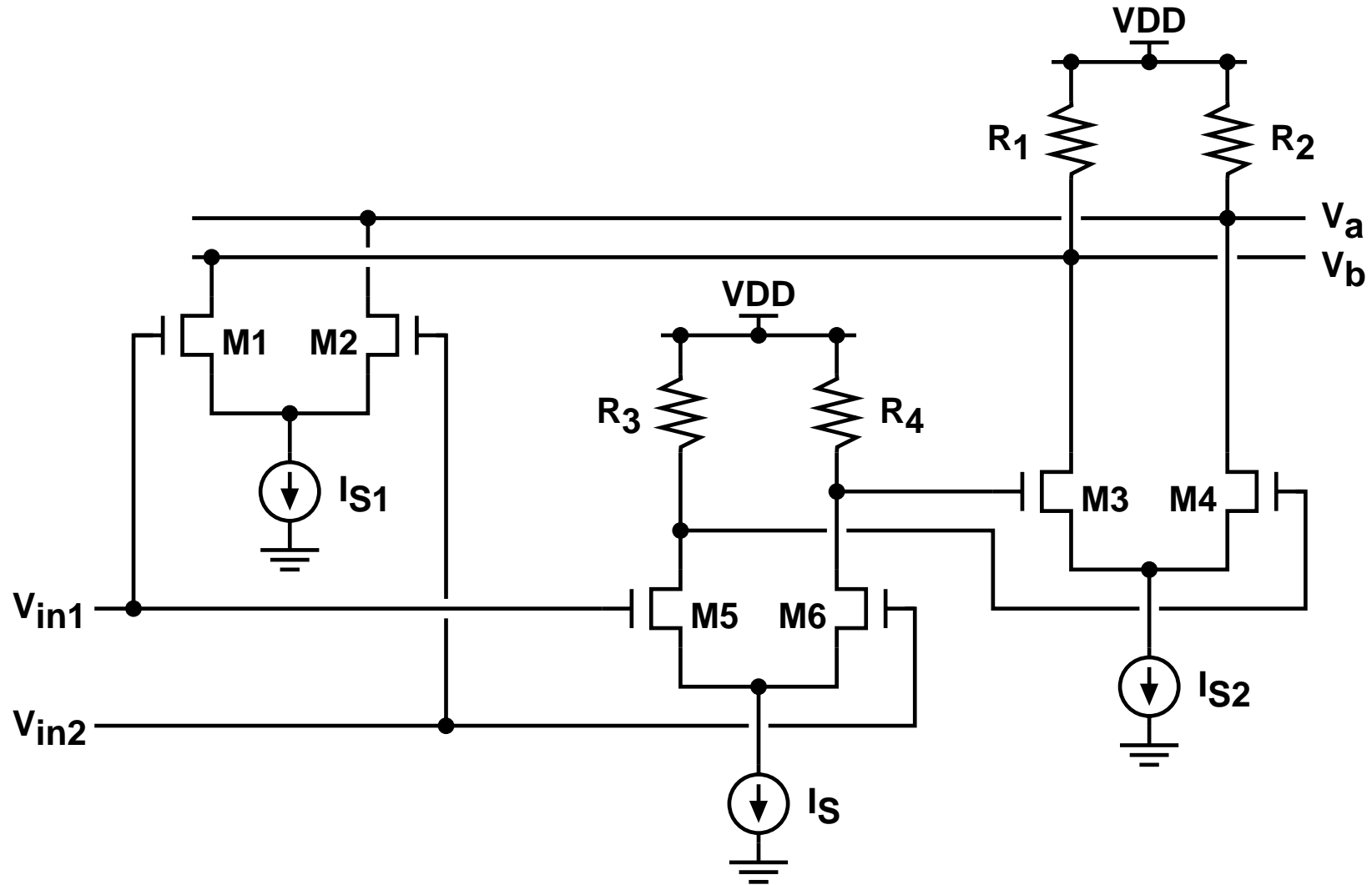
# Delay Variation Using Positive Feedback



$$I_T = I_{S1} + I_{S2} \quad \Delta V = I_T R_{1,2} \quad \omega_p \approx \frac{C}{G_{1,2} - g_{m3,4}} \quad A_0 \approx \frac{g_{m1,2}}{G_{1,2} - g_{m3,4}}$$

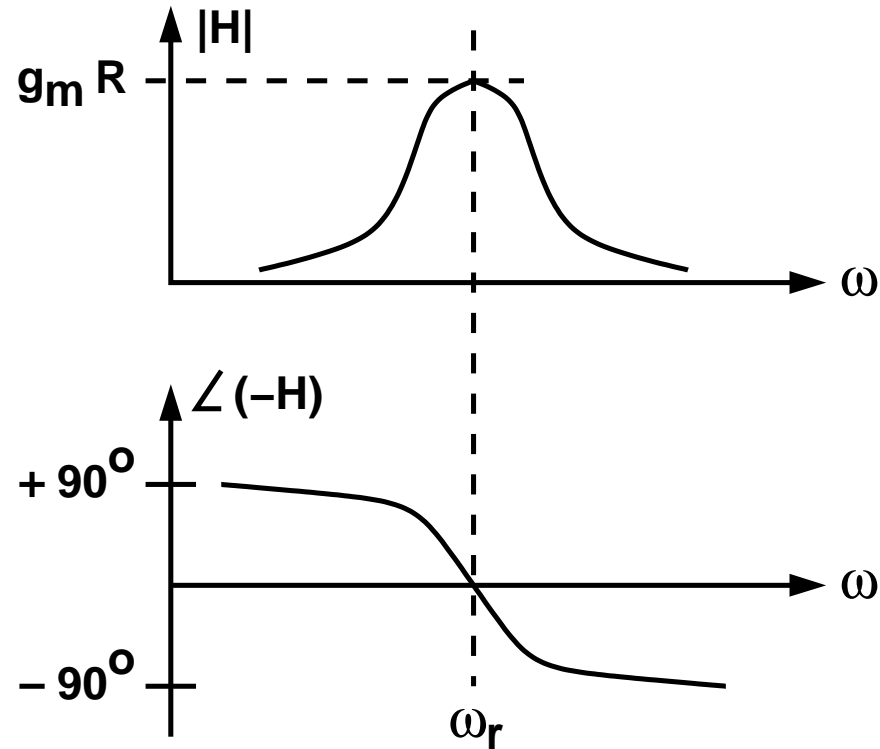
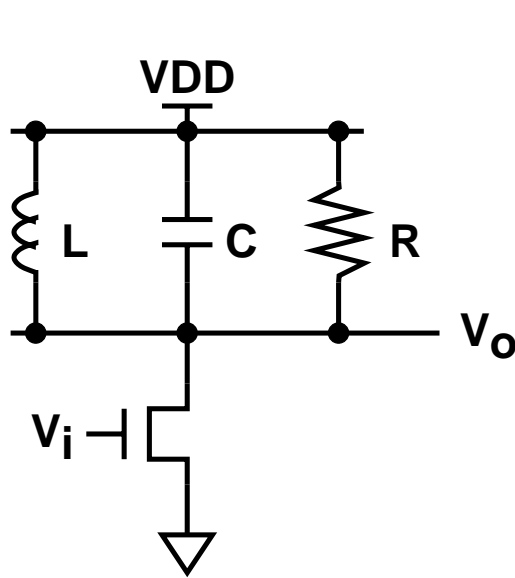
$$g_{m1,2} = \sqrt{2\mu_n C_{ox} (W/L)_{1,2} I_{S1}} \quad g_{m3,4} = \sqrt{2\mu_n C_{ox} (W/L)_{3,4} I_{S2}}$$

# Delay Variation Using Interpolation



$$I_{S1} + I_{S2} = \text{Constant}$$

# LC-Tuned Delay Stage



$$\omega_r = \frac{1}{\sqrt{LC}}$$

$$Q = \omega_r RC = \frac{R}{\omega_r L}$$

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{g_m}{(sL)^{-1} + sC + 1/R} = g_m R \cdot \frac{\frac{1}{Q} \left( \frac{s}{\omega_r} \right)}{\left( \frac{s}{\omega_r} \right)^2 + \frac{1}{Q} \left( \frac{s}{\omega_r} \right) + 1}$$

# LC-Tuned Delay Stage

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In the frequency domain

$$H(j\omega) = g_m R \cdot \frac{1}{1 + jQ \left( \frac{\omega}{\omega_r} - \frac{\omega_r}{\omega} \right)} = g_m R \cdot A(j\omega)$$

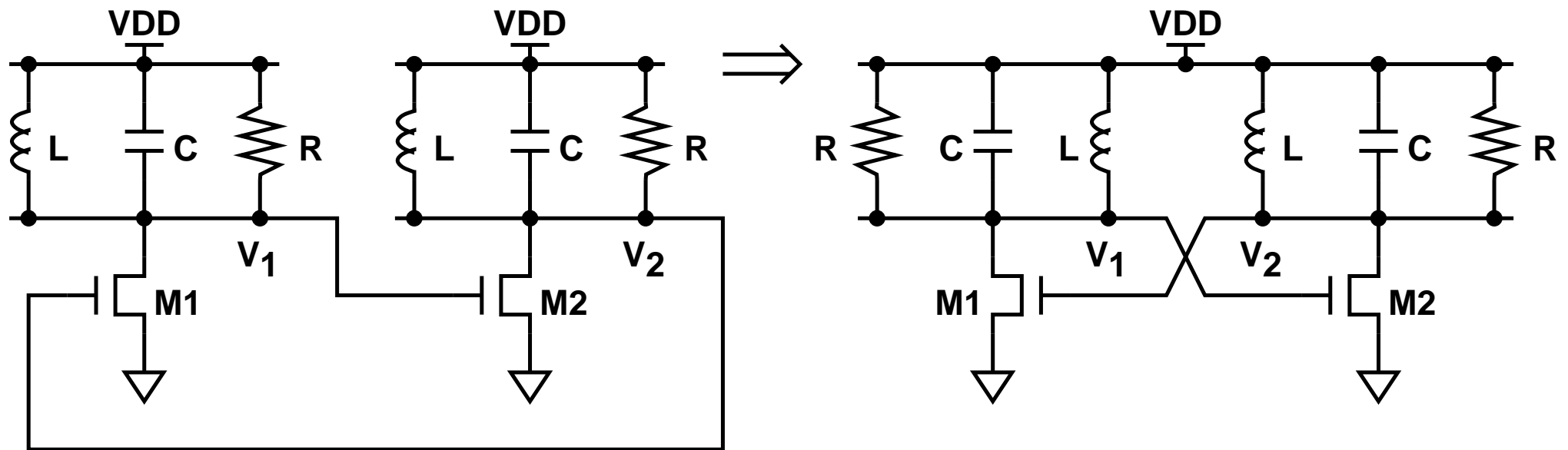
- $A(j\omega)$  is a band-pass function with  $-3$  dB frequencies at  $\omega_1$  and  $\omega_2$ , and bandwidth  $B = \omega_2 - \omega_1$ .

$$\omega_1 \cdot \omega_2 = \omega_r^2 \qquad B = \frac{\omega_r}{Q} = \omega_r^2 RC = \frac{R}{L}$$

- If  $\Delta\omega = \omega - \omega_r \ll \omega_r$ , we have

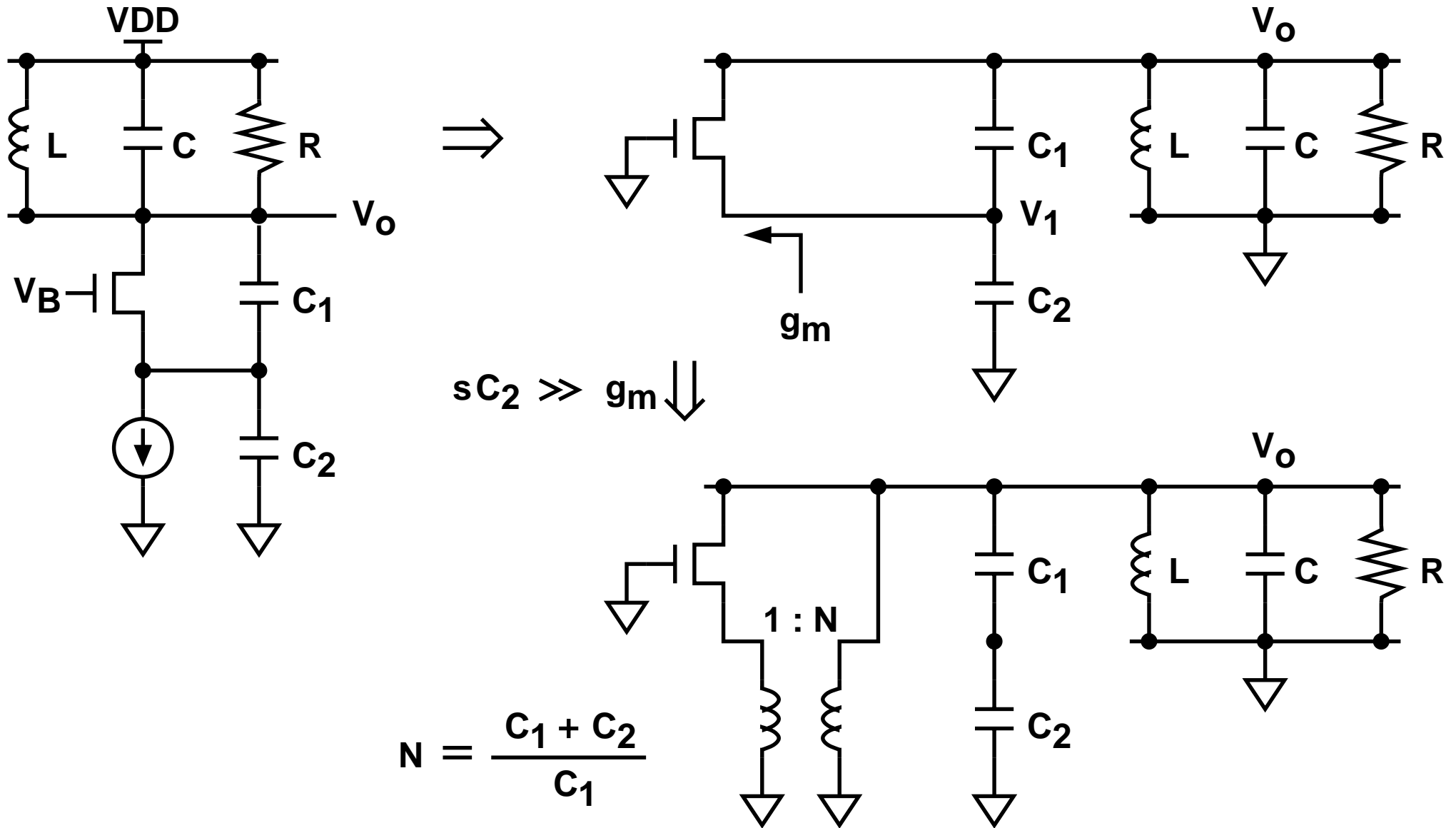
$$A(j\omega) \approx \frac{1}{1 + j2Q \cdot \frac{\Delta\omega}{\omega_r}}$$

# LC-Tuned Ring Oscillators



- Oscillation frequency is  $\omega_o = \omega_r = 1/\sqrt{LC}$ .
- $V_1$  and  $V_2$  are  $180^\circ$  out of phase.
- Need  $g_m R > 1$  to start oscillation.
- Varactors, such as pn junctions with reverse bias or MOSTs in the accumulation mode, are used for  $\omega_o$  variation.

# Colpitts Oscillator



# Colpitts Oscillator

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- The oscillation frequency is

$$\omega_o \approx \omega_r = \sqrt{\frac{1}{LC_p}} \quad C_p = C + (C_1 \parallel C_2) = C + \frac{C_1 C_2}{C_1 + C_2}$$

- The loop gain at  $\omega_r$  is

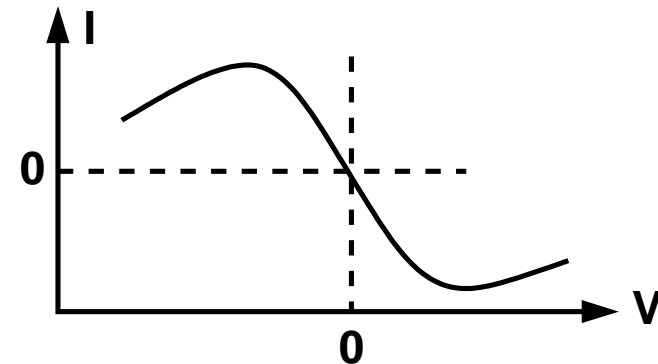
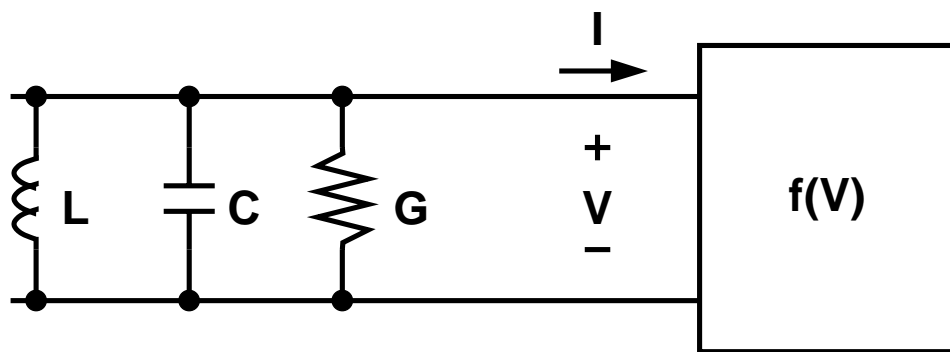
$$|T(j\omega_r)| = \frac{g_m}{G + \frac{g_m}{N^2}} \cdot \frac{1}{N} = \frac{g_m}{G \cdot N + \frac{g_m}{N}}$$

Want

$$|T(j\omega_r)| > 1 \quad \Rightarrow \quad g_m R > N + \frac{g_m R}{N}$$

- If  $C_1 \gg C_2$ , i.e.,  $N \sim 1$ , oscillation cannot occur.

# One-Port Oscillators



$$\frac{1}{L} \int V dt + C \frac{dV}{dt} + G \cdot V + f(V) = 0 \quad \Rightarrow \quad LC \frac{dV^2}{dt} + L \frac{d}{dt} [G \cdot V + f(V)] + V = 0$$

- For small-signal analysis, let  $f(V) = -a \cdot V$  with  $a = -df(V)/dV|_{V=0}$ . Then, we have

$$LCs^2 + L(G - a)s + 1 = 0$$

$$s_1, s_2 = -\left(\frac{G - a}{2C}\right) \pm j \sqrt{\frac{1}{LC} - \left(\frac{G - a}{2C}\right)^2} = \alpha \pm j\beta \quad \Rightarrow \quad V(t) \approx Ae^{\alpha} \cos \beta t$$

Need  $a > G$  to start oscillation.

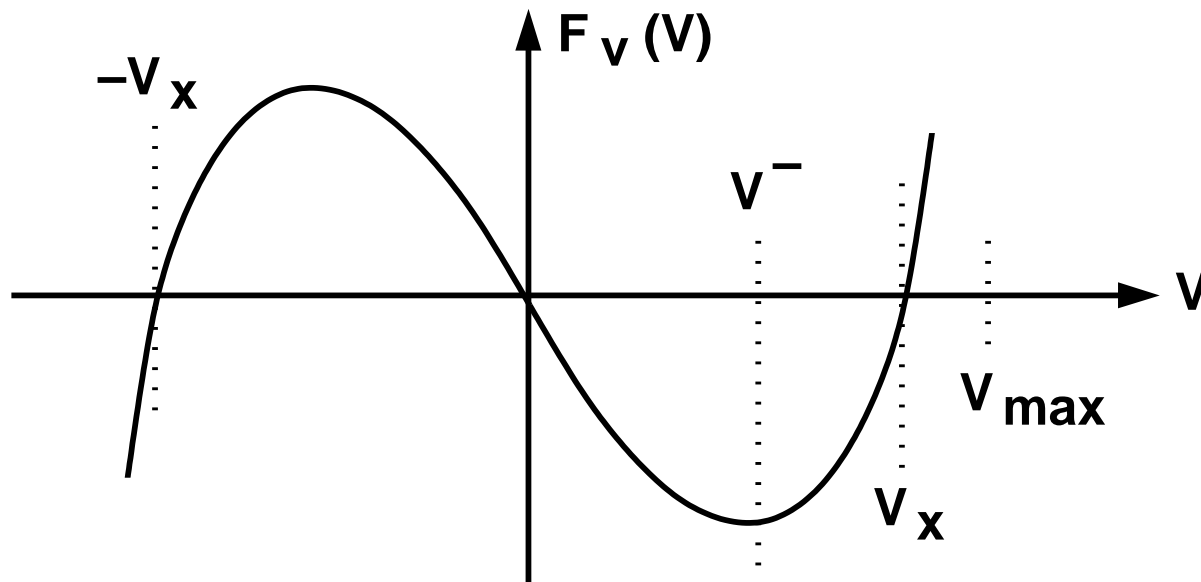
# The van der Pol Approximation

Let  $T = t/\sqrt{LC}$ , we have

$$\frac{d^2V}{dT^2} + \sqrt{\frac{L}{C}} \cdot \frac{d}{dT}[F(V)] + V = 0 \quad F(V) = G \cdot V + f(V)$$

The van der Pol approximation for  $F(V)$  is

$$F_V(V) = -a_1 \cdot V + b_1 \cdot V^3 \quad a_1 = a - G$$



$$\pm V_x = \pm \sqrt{\frac{a_1}{b_1}}$$

$$V^- = \sqrt{\frac{1}{3} \cdot \frac{a_1}{b_1}}$$

$$\epsilon = \sqrt{\frac{L}{C}} \cdot a_1 = \sqrt{\frac{L}{C}} \cdot (a - G)$$

# The van der Pol Approximation

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For near-sinusoidal oscillations,  $\epsilon > 0$  and  $\epsilon \rightarrow 0$ .

$$v(t) = \sqrt{\frac{4a_1}{3b_1}} \cdot \frac{1}{\sqrt{1 + e^{-(t-t_0)\epsilon/\sqrt{LC}}}} \cos\left(\frac{t}{\sqrt{LC}}\right)$$

- At the start of oscillation,  $e^{-(t-t_0)\epsilon/\sqrt{LC}} \gg 1$ , we have

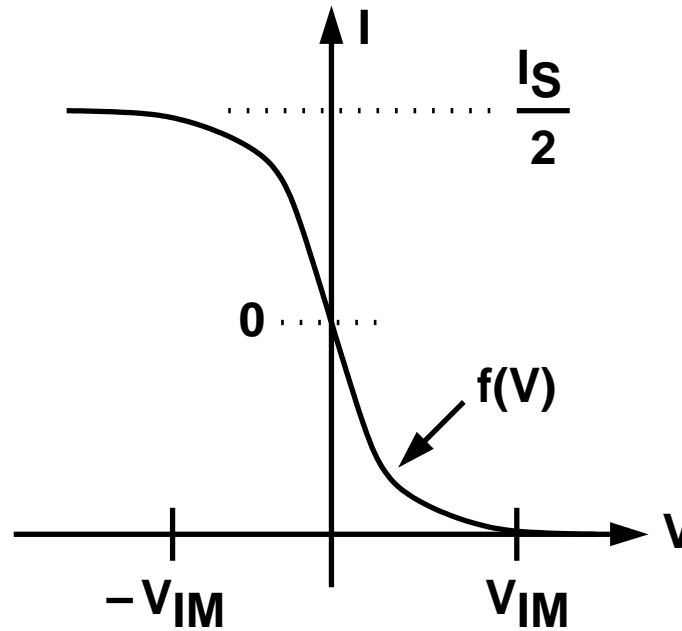
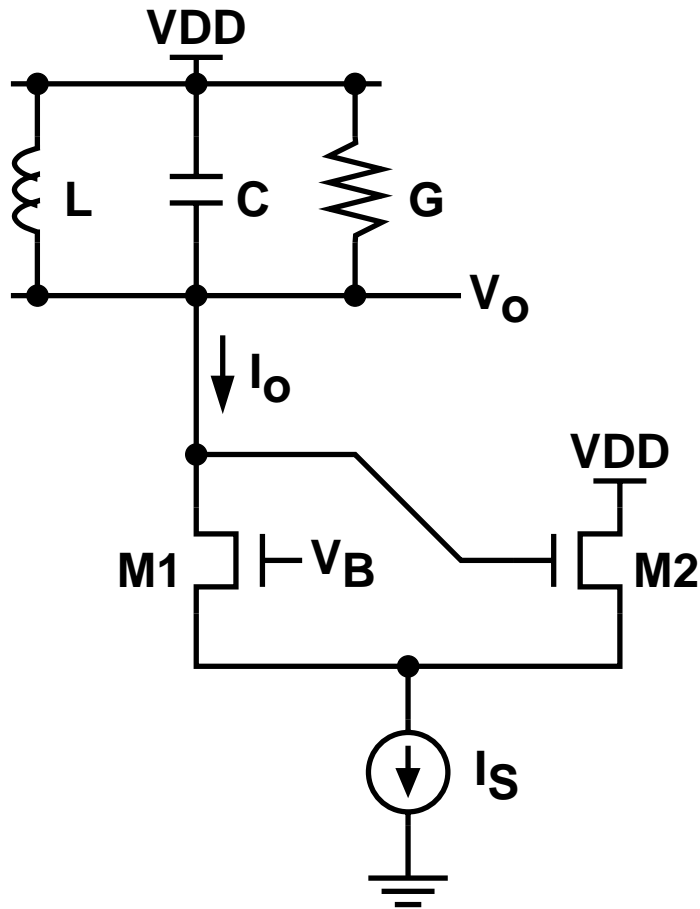
$$V(t) = Ae^{et/(2\sqrt{LC})} \cos\left(\frac{t}{\sqrt{LC}}\right) = Ae^{\epsilon T/2} \cos T \quad A = \sqrt{\frac{4a_1}{3b_1}} \cdot e^{-\epsilon t_0/(2\sqrt{LC})}$$

- In steady state,  $t \rightarrow \infty$ ,

$$V(t) = \sqrt{\frac{4a_1}{3b_1}} \cos\left(\frac{t}{\sqrt{LC}}\right) = V_{max} \cos T$$

$$V_{max} = \sqrt{\frac{4a_1}{3b_1}} = \sqrt{\frac{4}{3}} \cdot V_x = 1.15V_x = 2V^-$$

# A CMOS SONY Oscillator



$$V = V_o - V_B$$

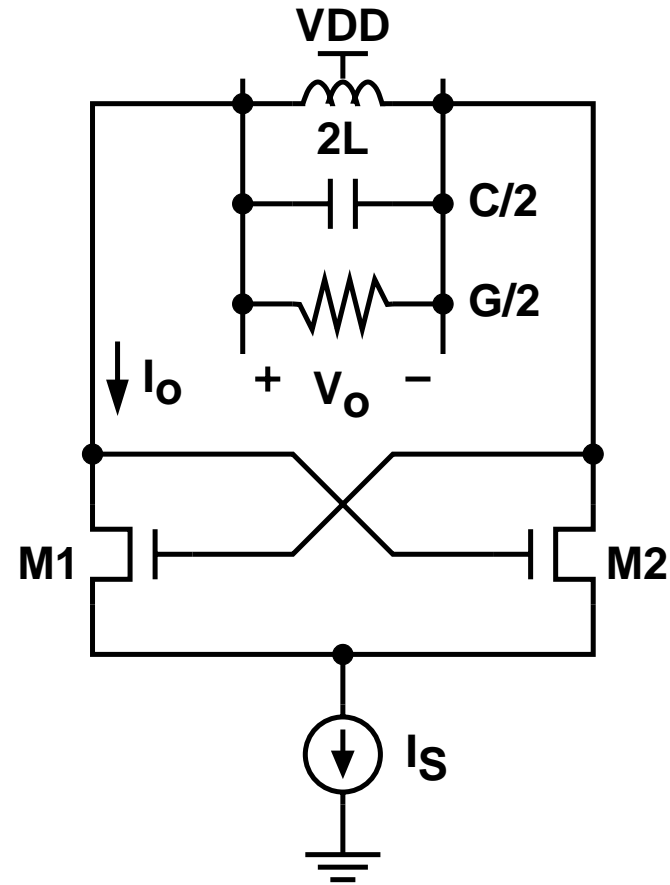
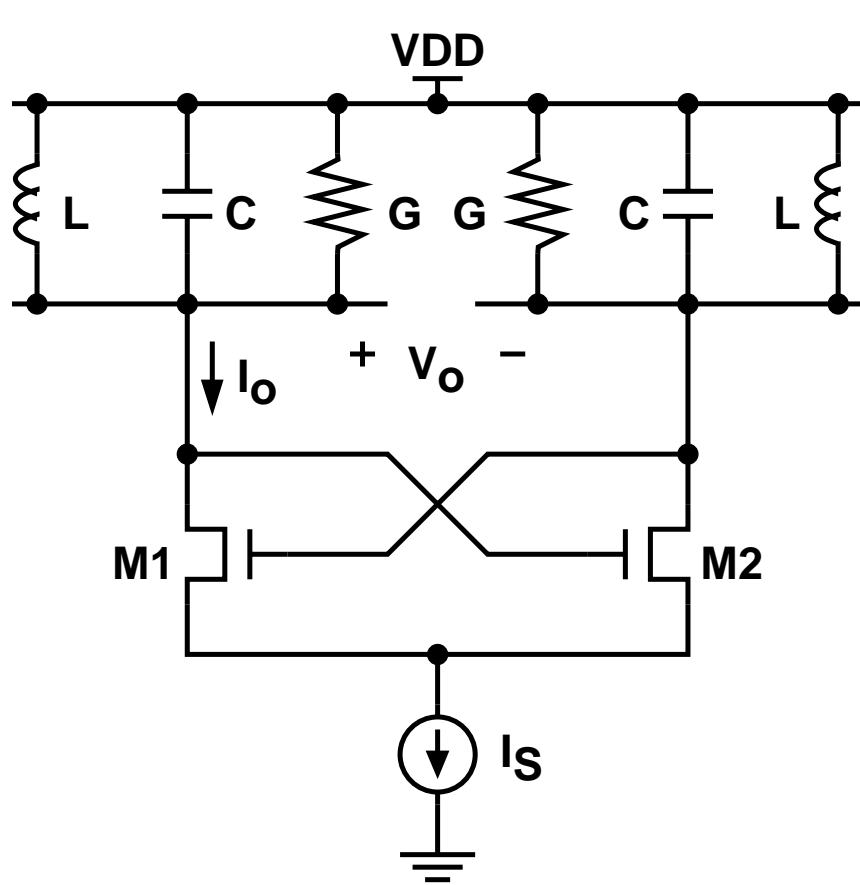
$$I = I_o - \frac{I_S}{2}$$

$$I = f(V) = \frac{k}{4} V \sqrt{\frac{4I_S}{k} - V^2}$$

$$V_{IM} = \sqrt{\frac{2I_S}{k}}$$

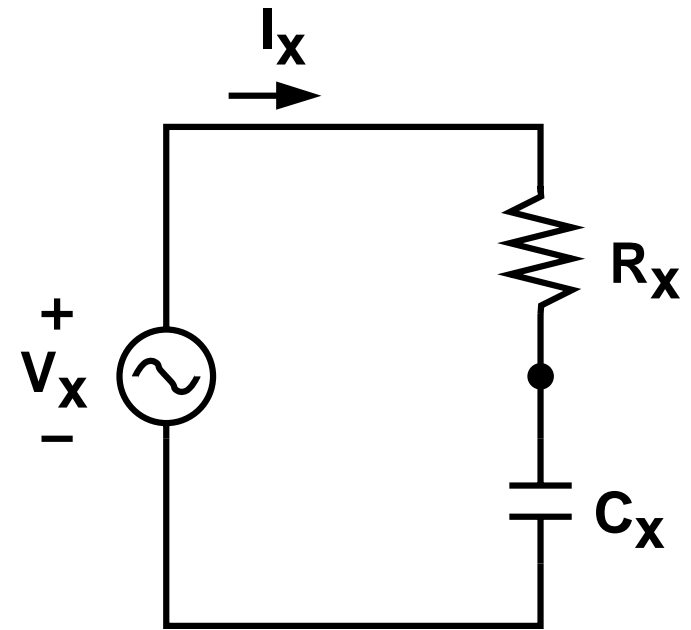
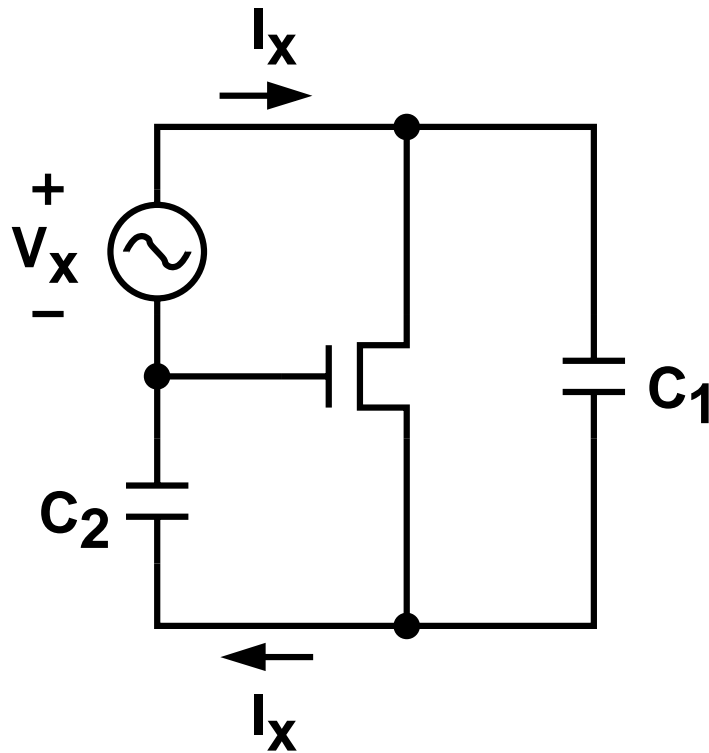
$$k = \mu C_{ox} \left( \frac{W}{L} \right)_{1,2}$$

# Differential CMOS SONY Oscillators



$$V = V_o \quad I = I_o \quad I = f(V) = \frac{k}{4} V \sqrt{\frac{4I_S}{k} - V^2} \quad k = \mu C_{ox} \left( \frac{W}{L} \right)_{1,2}$$

# Single-Transistor Negative Resistance Generator



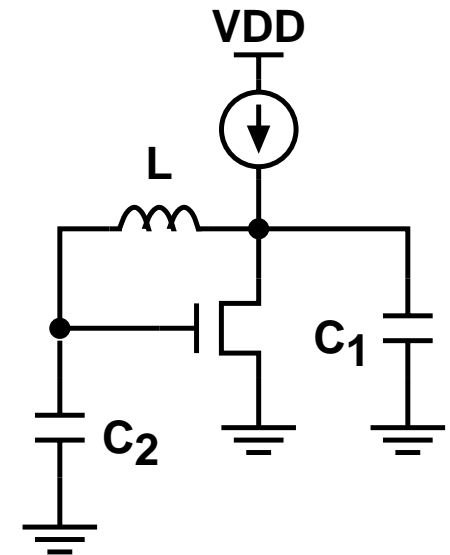
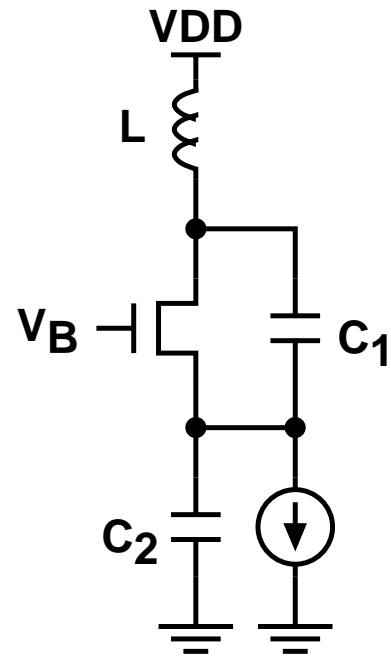
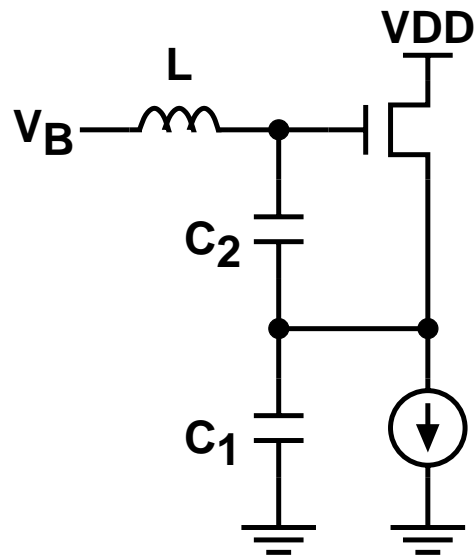
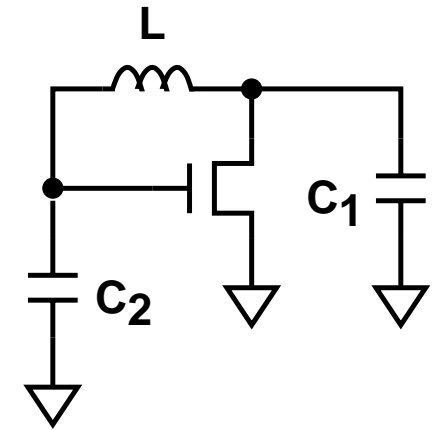
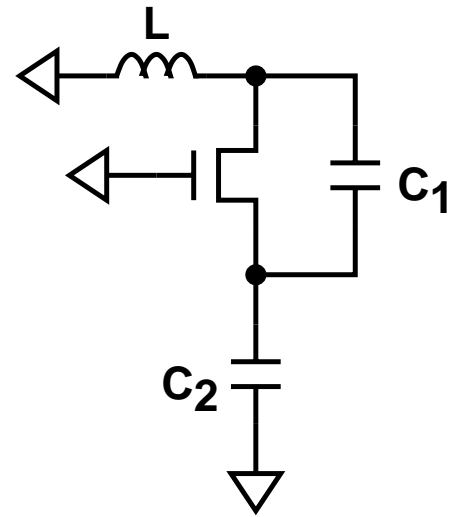
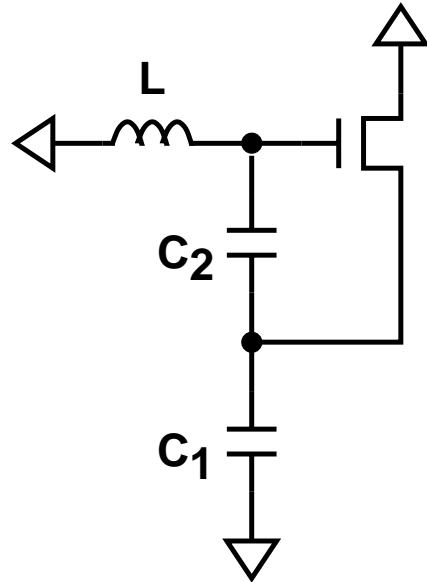
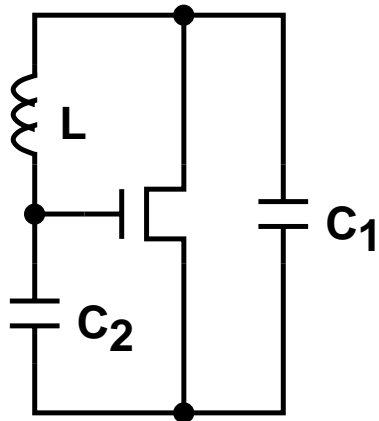
$$V_x = \left( I_x - \frac{-I_x \cdot g_m}{sC_2} \right) \frac{1}{sC_1} + \frac{I_x}{sC_2}$$

$$\Rightarrow \frac{V_x}{I_x} = \frac{g_m}{s^2 C_1 C_2} + \frac{1}{sC_1} + \frac{1}{sC_2}$$

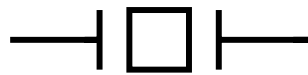
$$R_x = -\frac{g_m}{\omega^2 C_1 C_2}$$

$$C_x = C_1 \parallel C_2 = \frac{C_1 C_2}{C_1 + C_2}$$

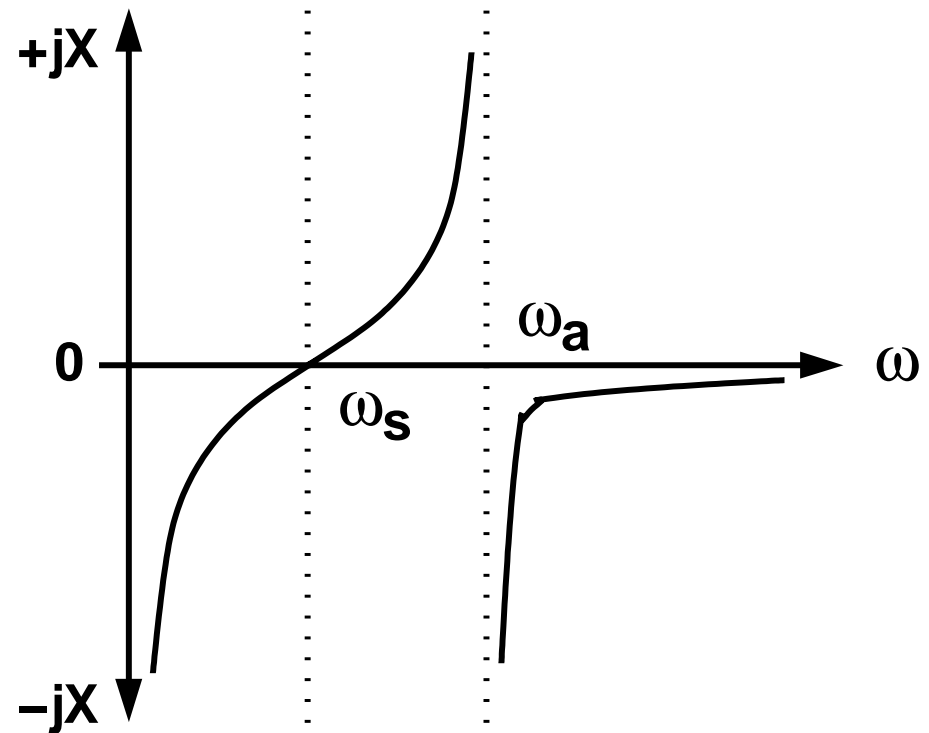
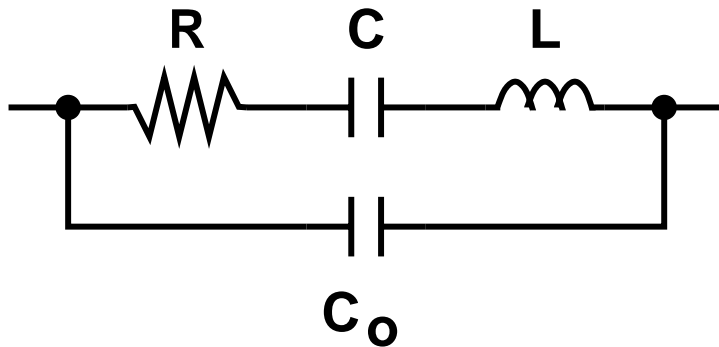
# Single-Transistor Negative-Resistance Oscillators



# Piezoelectric Crystals



Circuit Model



$$Z(j\omega) = \frac{[R + (j\omega C)^{-1} + j\omega L](j\omega C_o)^{-1}}{R + (j\omega C)^{-1} + j\omega L + (j\omega C_o)^{-1}}$$

$$\omega_s = \frac{1}{\sqrt{LC}}$$

$$\omega_a = \frac{1}{\sqrt{L(C \parallel C_o)}}$$

$$\frac{\omega_a}{\omega_s} = \sqrt{1 + \frac{C}{C_o}}$$

$$Q = \frac{1}{\omega_s RC} = \frac{\omega_s L}{R}$$

# Piezoelectric Crystals

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- Example:  $R = 16.3 \Omega$ ,  $C = 0.009 \text{ pF}$ ,  $L = 7.036 \text{ nH}$ ,  $C_o = 2.3 \text{ pF}$ ; thus  $f_o = 20 \text{ MHz}$ ,  $Q = 54245$ .
- The serial RLC can be transformed into a parallel circuit

$$R_p = R (1 + Q_s^2) \quad X_p = X_s \left( 1 + \frac{1}{Q_s^2} \right) \quad \text{where} \quad X_s = \omega L - \frac{1}{\omega C} \quad Q_s = \frac{X_s}{R}$$

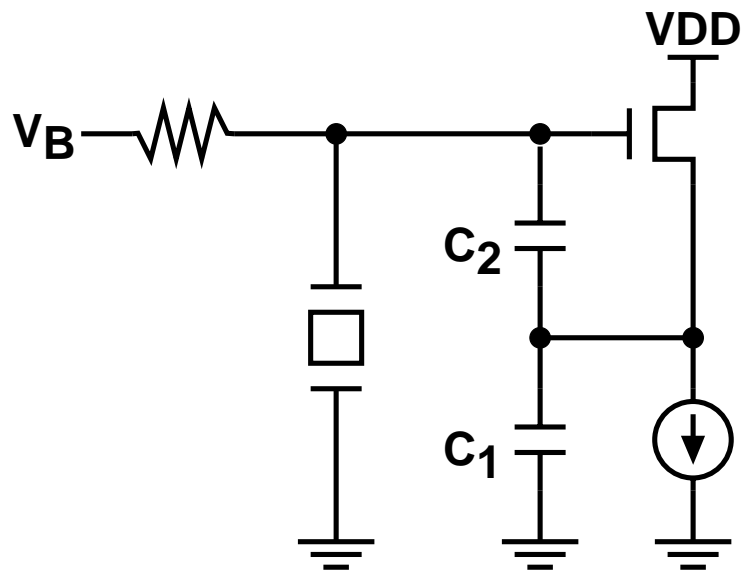
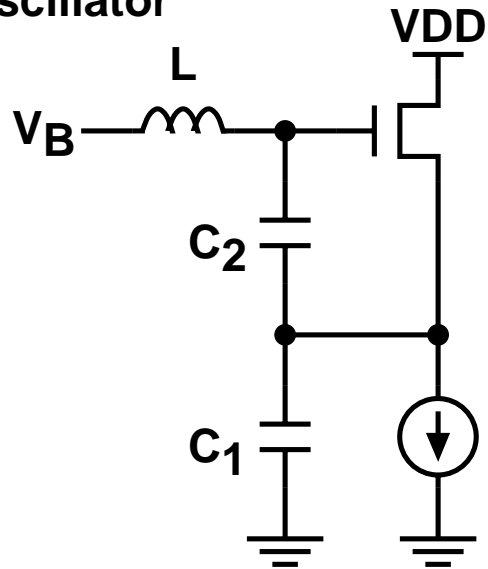
At  $\omega = \omega_a$ , with  $Q_s \gg 1$ , we have

$$X_p = \frac{1}{\omega_a C_o} \quad R_p \approx \frac{X_s^2}{R} \approx \frac{X_p^2}{R} = \frac{1}{R(\omega_a C_o)^2}$$

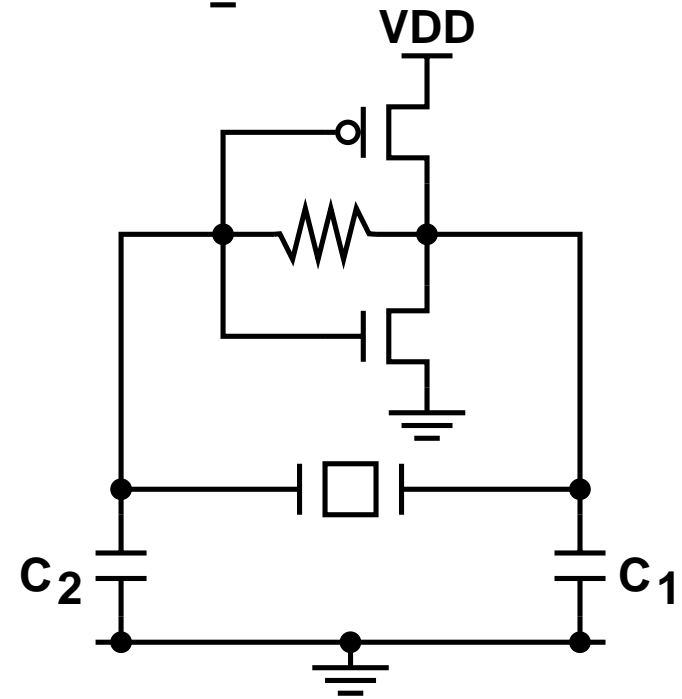
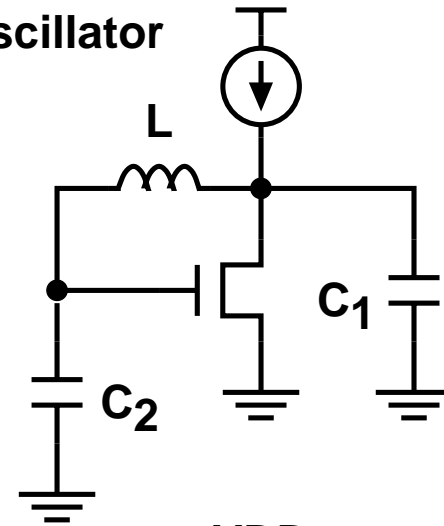
- Circuits containing crystals are designed so that the frequency range of interest is between  $\omega_s$  and  $\omega_a$ .

# Crystal Oscillators

## Colpitts Oscillator

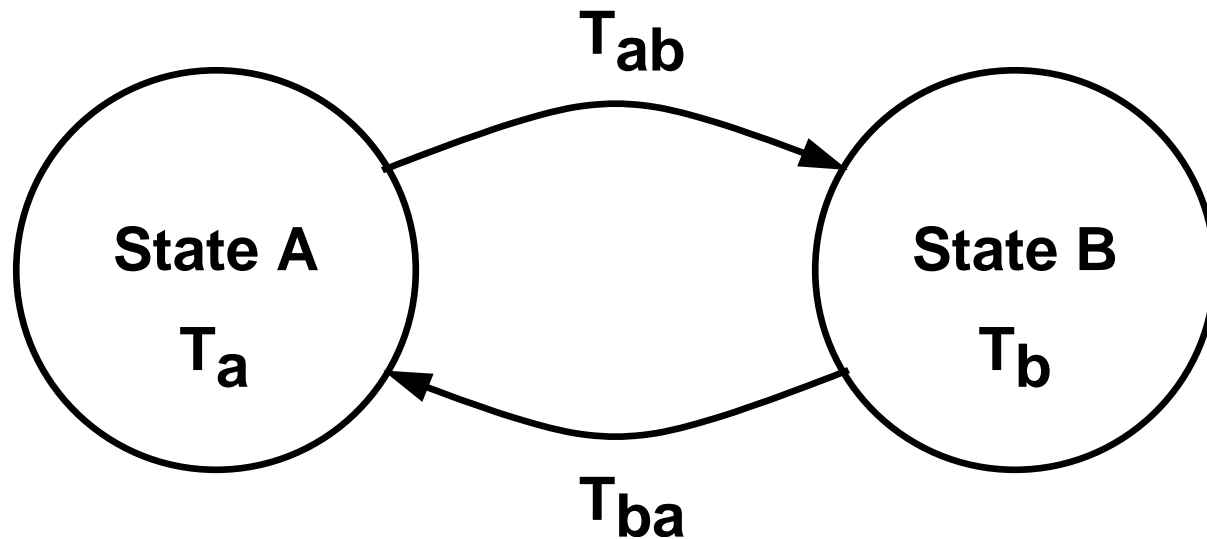


## Pierce Oscillator



# Relaxation Oscillators (Multivibrators)

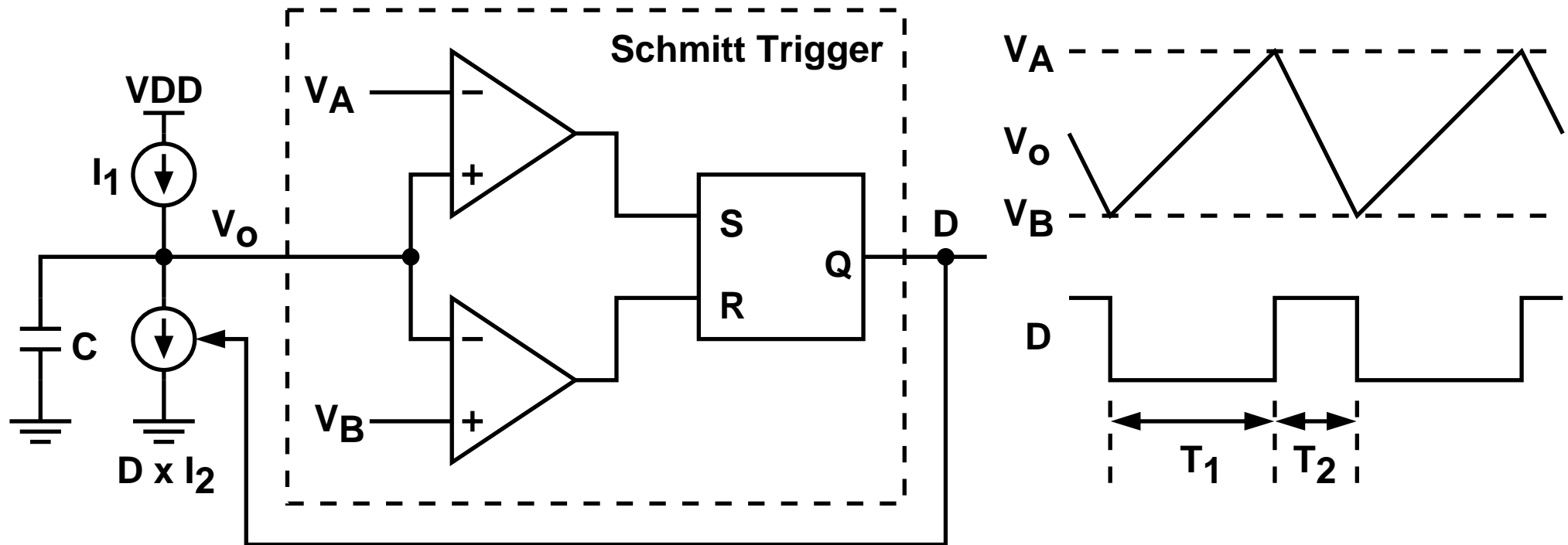
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$$f_o = \frac{1}{T_a + T_b + T_{ab} + T_{ba}}$$
$$f_{o,max} \approx \frac{1}{T_{ab} + T_{ba}}$$

- The two states are created by positive feedback.
- $T_a$  and  $T_b$  are usually determined by the charging and discharging of timing capacitors, while  $T_{ab}$  and  $T_{ba}$  are the transient response of the circuit.
- Comparing with the frequency-tuned oscillators, the relaxation oscillators have wider tuning range, predictable waveforms, but poorer spectral purity.

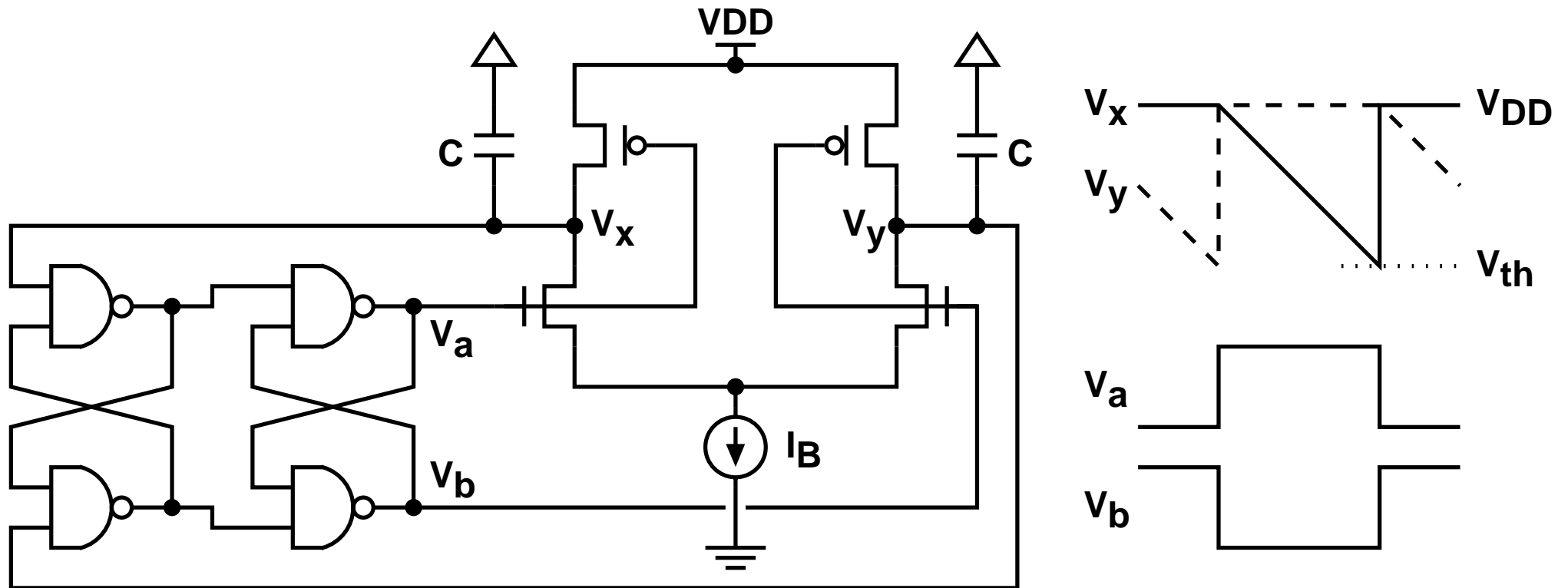
# Constant-Current Charge/Discharge Oscillators



$$T_1 = \frac{C \cdot (V_A - V_B)}{I_1} \quad T_2 = \frac{C \cdot (V_A - V_B)}{I_2 - I_1}$$

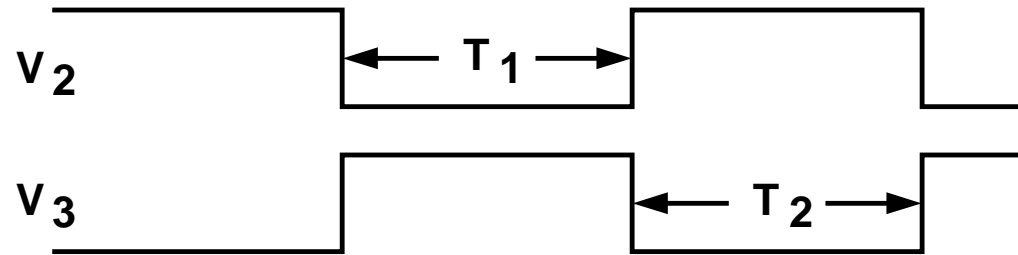
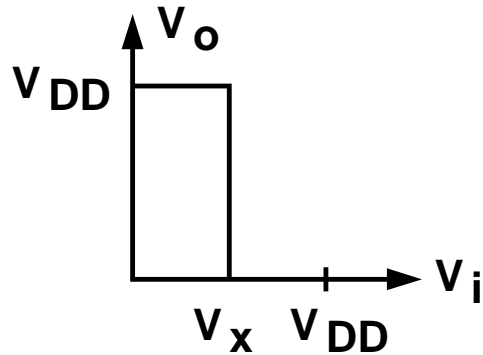
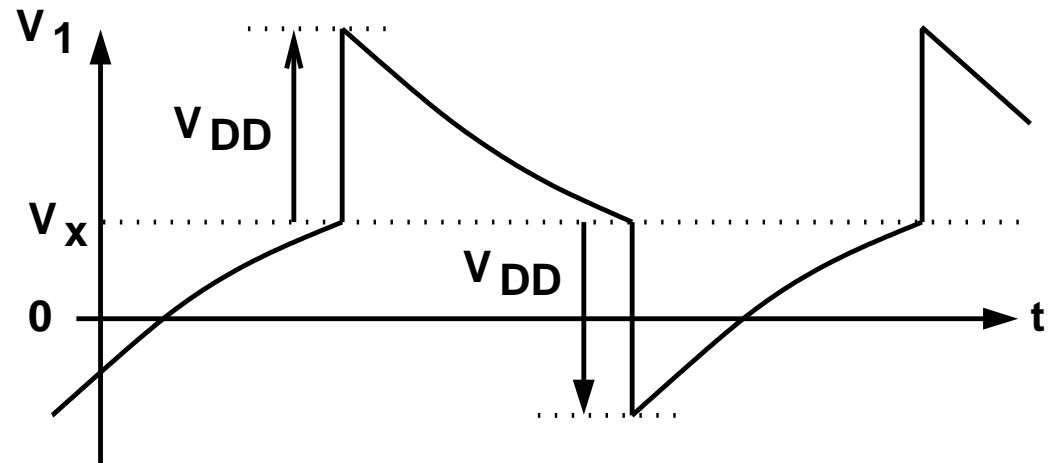
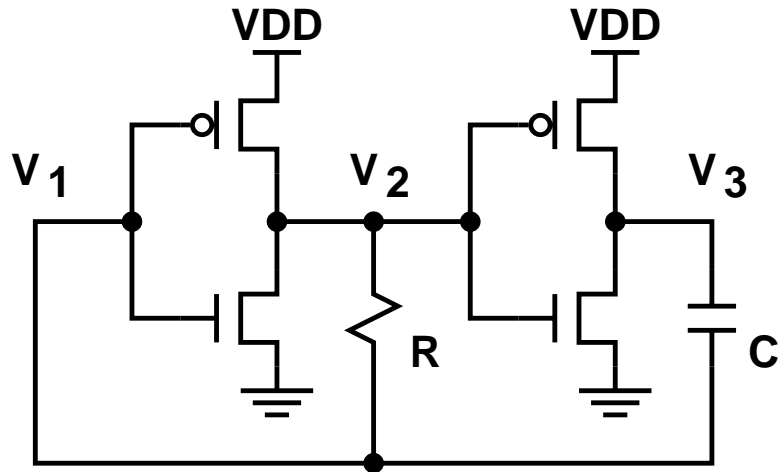
$$f_o = \frac{1}{T_1 + T_2} = \frac{I_1}{C \cdot (V_A - V_B)} \left( 1 - \frac{I_1}{I_2} \right)$$

# The Banu Oscillator



- Oscillation frequency is  $f_o = 1/(2T)$  where  $T = C \cdot (V_{DD} - V_{th})/I_B$ .
- Reference: Banu, M., "MOS Oscillators with Multi-Decade Tuning Range and GHz Maximum Speed," JSSC, 12/1998, pp. 1386–1393.

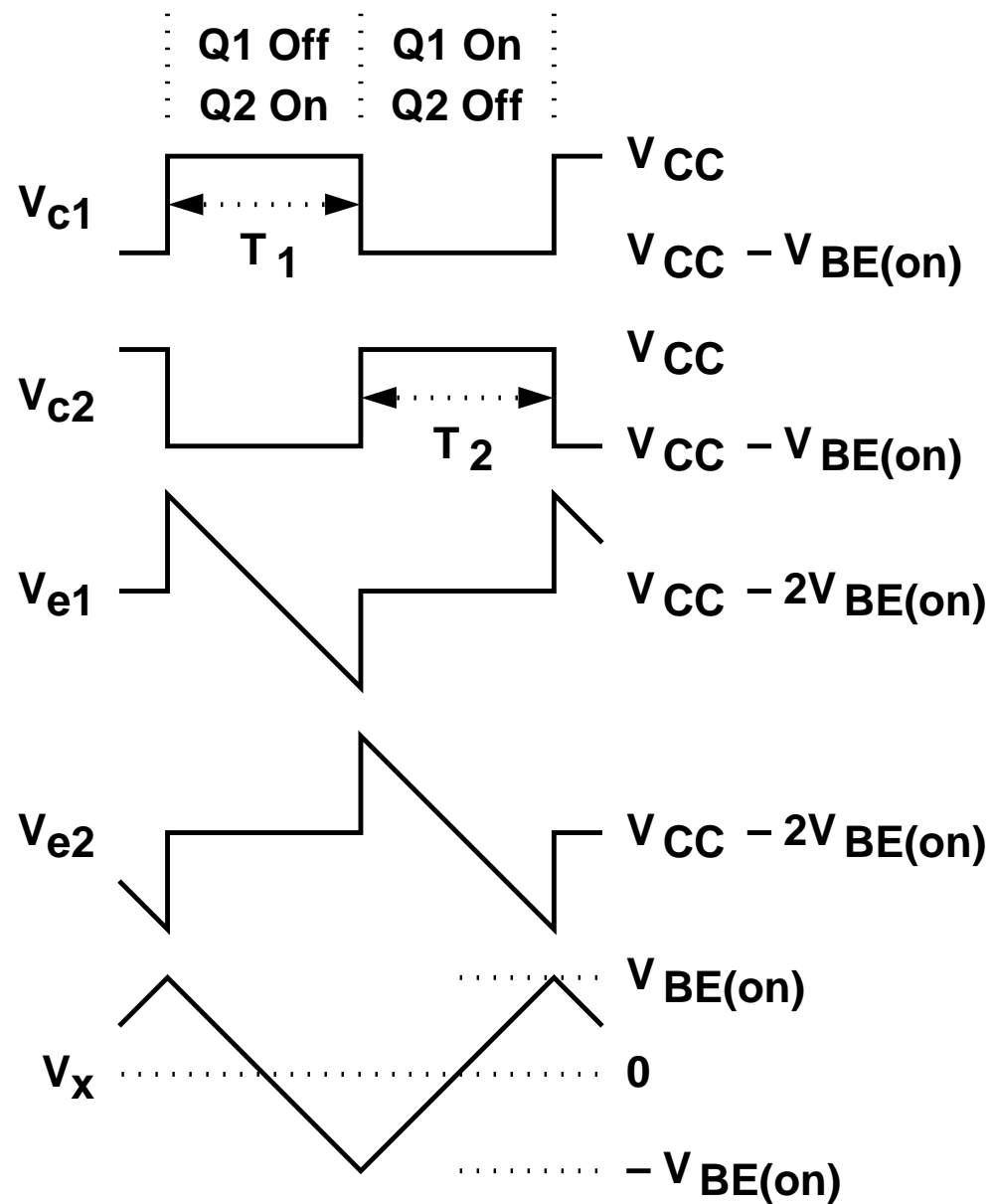
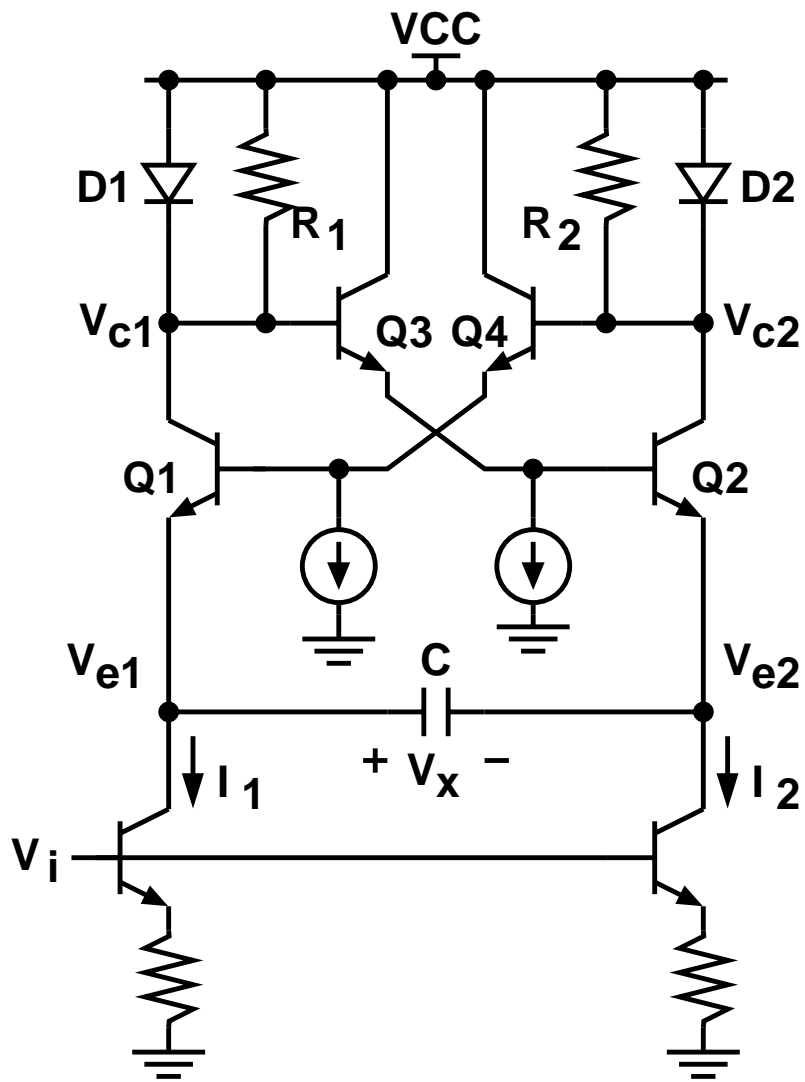
# A CMOS Relaxation Oscillator



$$V_1(t) = 0 + (V_x + V_{DD} - 0)e^{-t/(RC)} \quad \Rightarrow \quad T_1 = RC \ln \frac{V_x + V_{DD}}{V_x}$$

$$V_1(t) = V_{DD} + (V_x - V_{DD} - V_{DD})e^{-t/(RC)} \quad \Rightarrow \quad T_2 = RC \ln \frac{2V_{DD} - V_x}{V_{DD} - V_x}$$

# A Emitter-Coupled Multivibrator



# A Emitter-Coupled Multivibrator

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- Q1, Q2, Q3, and Q4 are never saturated.
- D1 and D2 act as voltage clamps. Thus the maximum voltage across R1 and R2 are  $V_{BE(on)}$ .
- The relaxation times are

$$T_1 = \frac{C \cdot 2V_{BE(on)}}{I_1} \qquad T_2 = \frac{C \cdot 2V_{BE(on)}}{I_2}$$

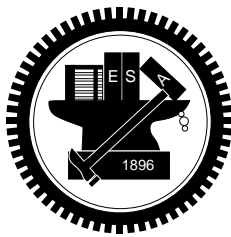
- If  $I_1 = I_2 = I$ , the frequency of oscillation is

$$f_o = \frac{1}{T_1 + T_2} = \frac{1}{4} \cdot \frac{I}{C \cdot V_{BE(on)}}$$

# Fundamentals of Analog Filters

Jieh-Tsorng Wu

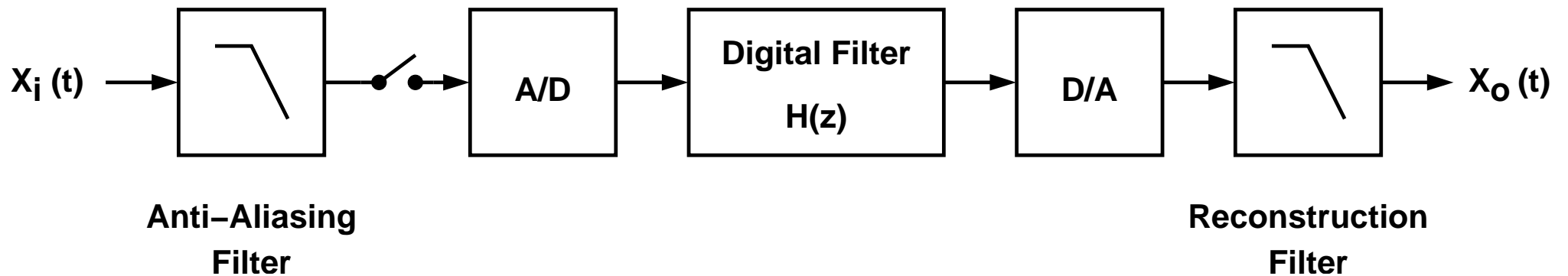
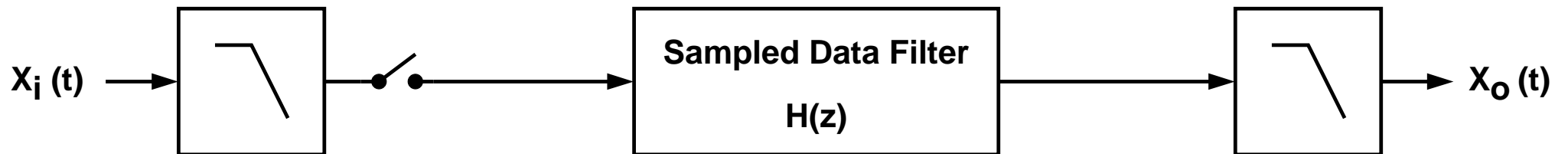
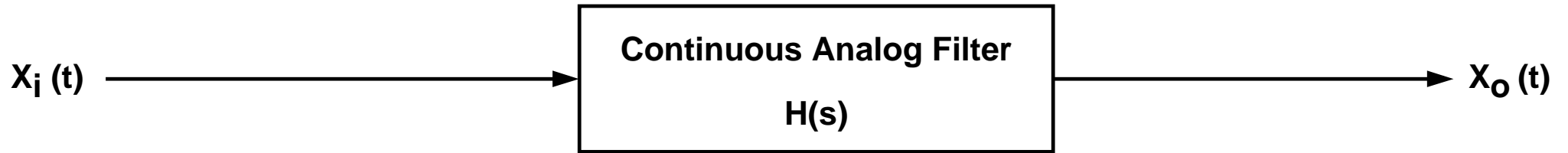
July 16, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Filters

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# Filters

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## Continuous-Time Analog Filters

- Differential equations.
- Laplace transforms.  $s = j\omega$

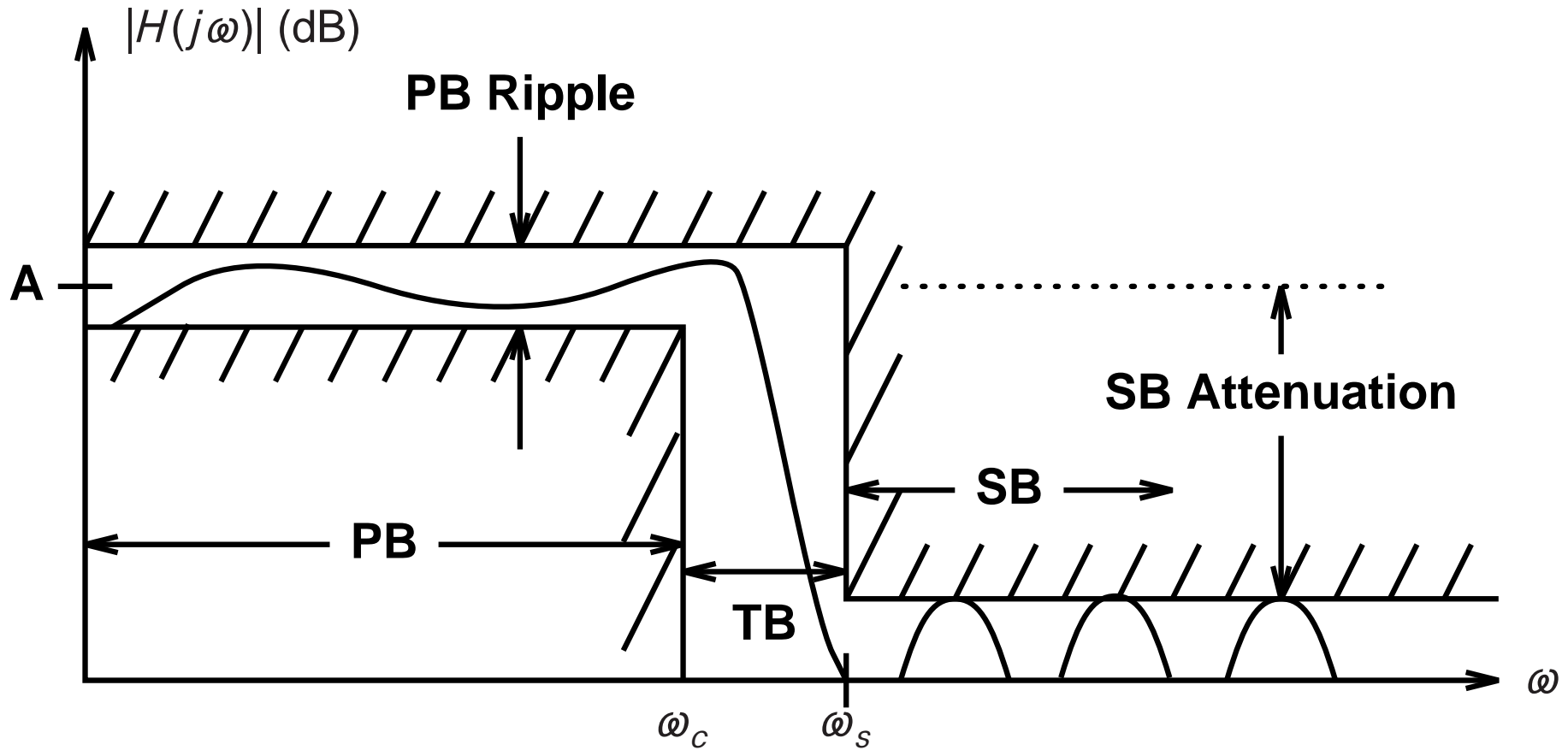
## Discrete-Time (Sampled-Data) Analog Filters

- Difference equations.
- Z-transform;  $z^{-1}$  is unit delay operator.  $z = e^{j\omega T_s}$ ;  $T_s$  is sampling period.

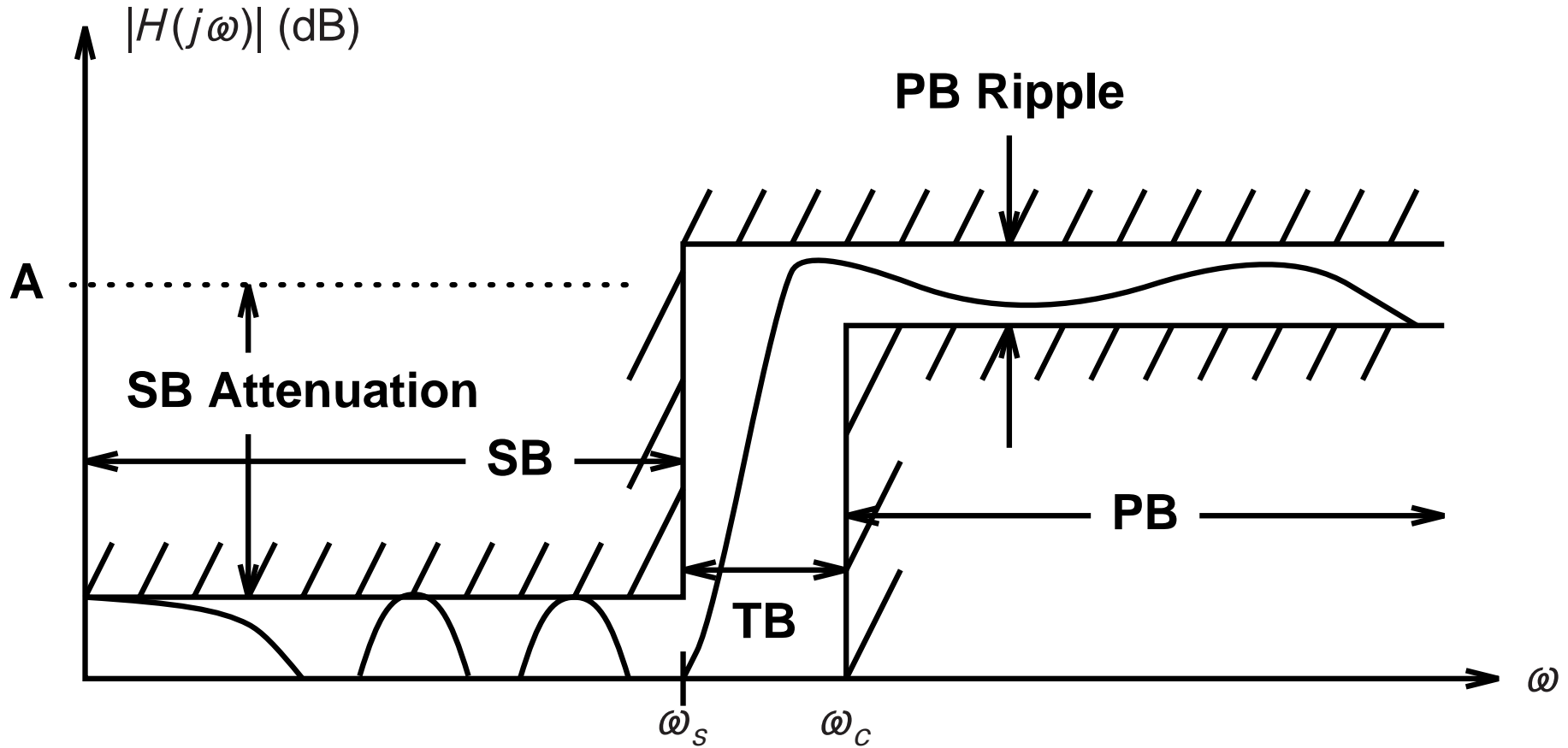
## Discrete-Time (Sampled-Data) Digital Filters

- Discrete-time systems.
- A/D introduces quantization noise.

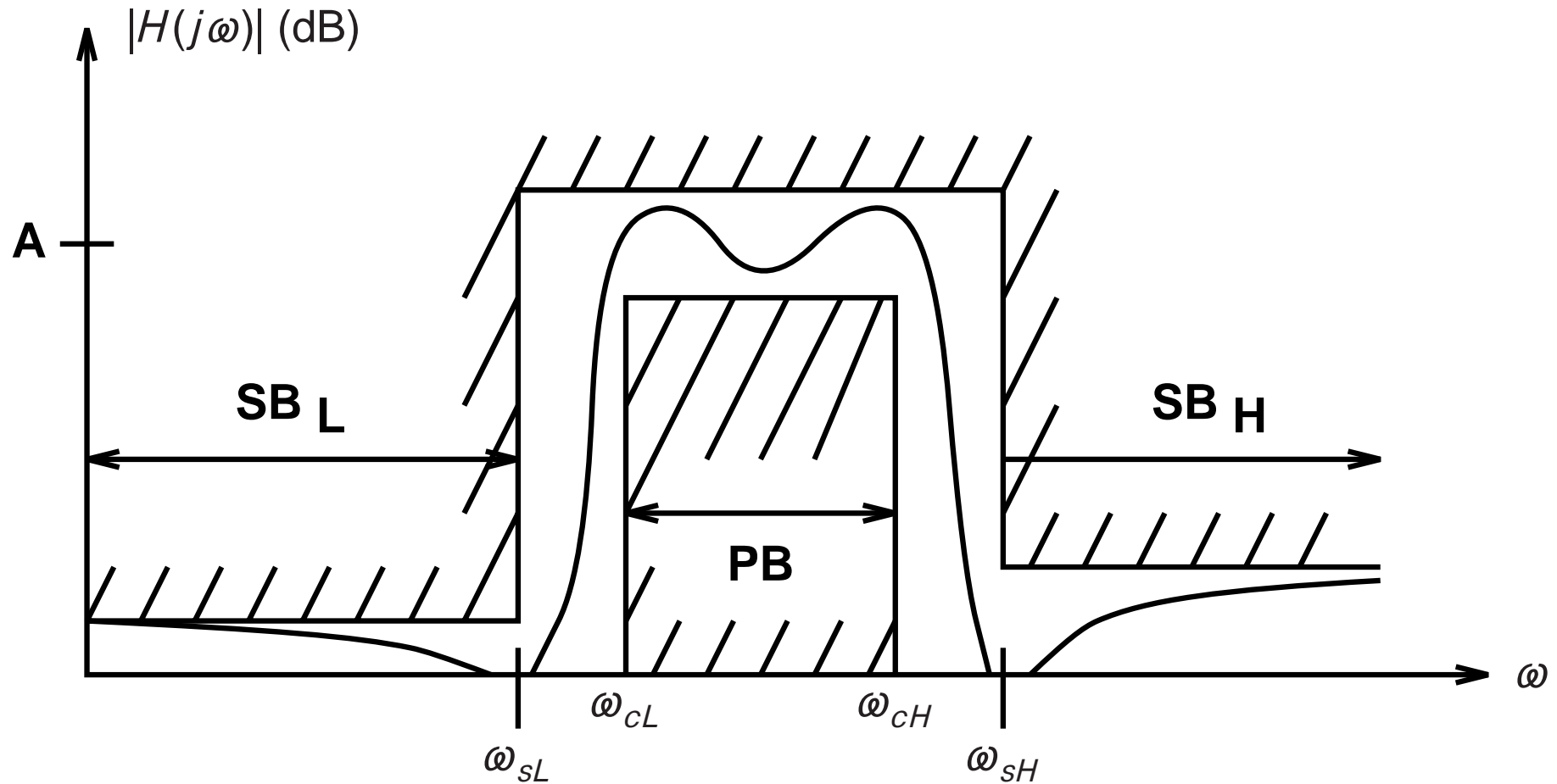
# Low-Pass Filter Specifications



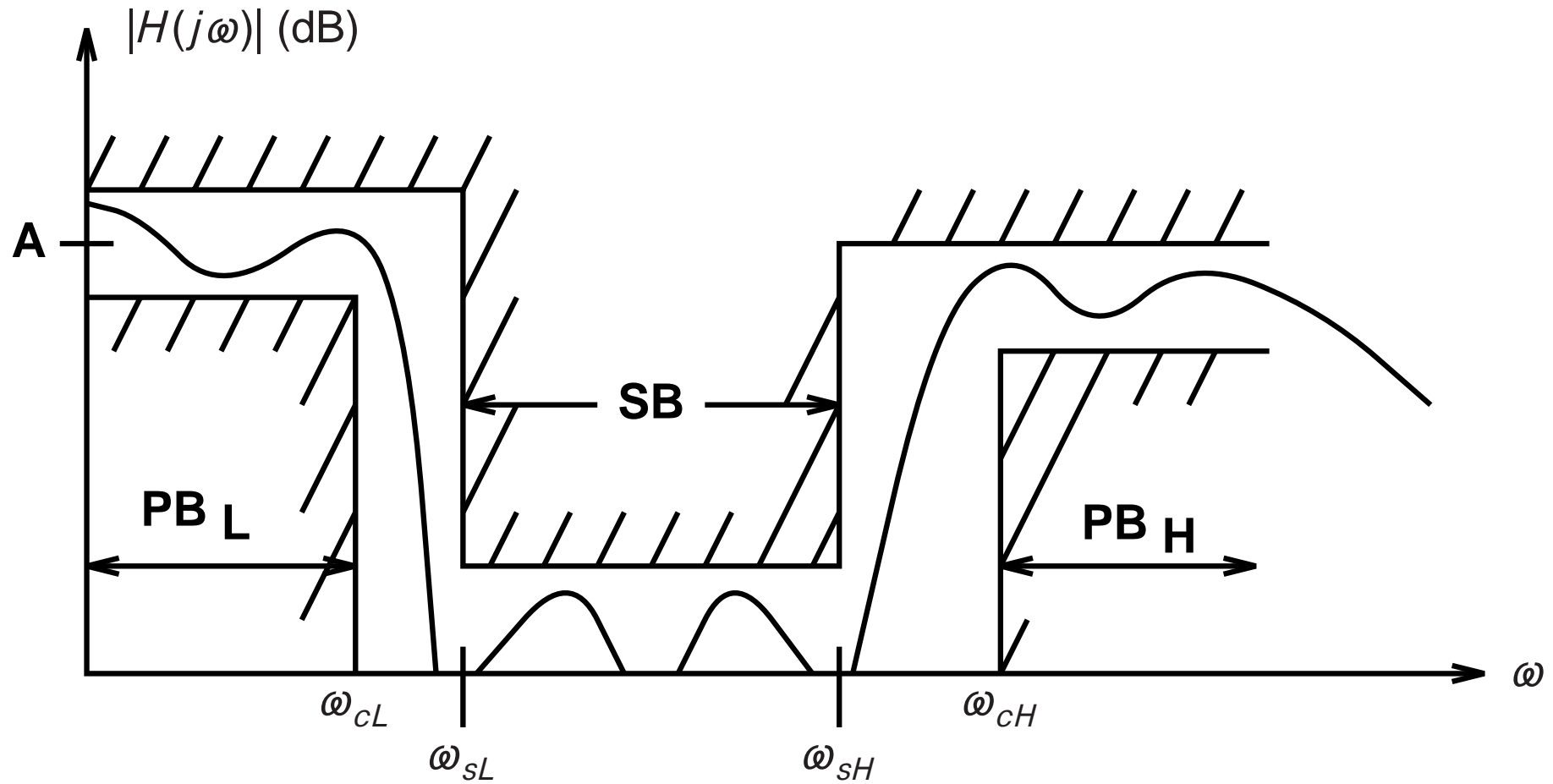
# High-Pass Filter Specifications



# Band-Pass Filter Specifications

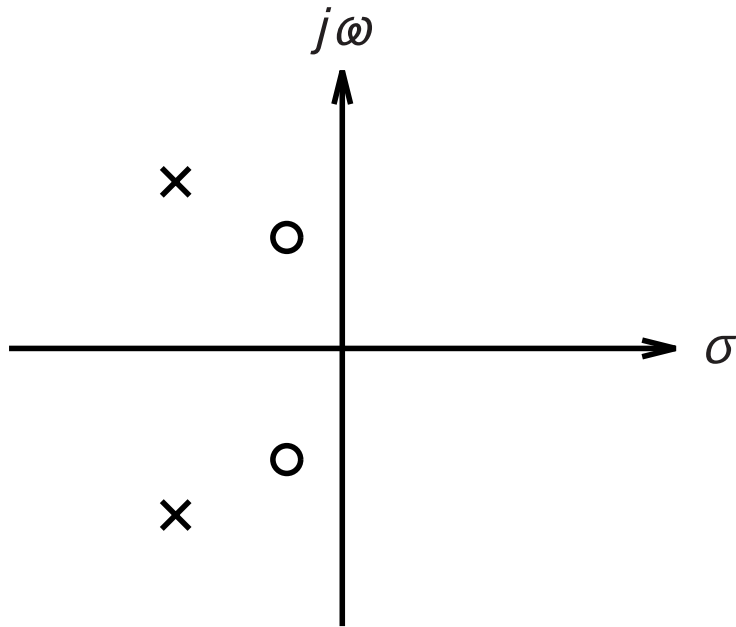


# Band-Reject Filter Specifications



## Second-Order Filter (Biquadratic Function)

---



$$\begin{aligned} H(s) &= \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0} \\ &= \frac{a_2 (s - z_1)(s - z_2)}{(s - p_1)(s - p_2)} \\ &= K \cdot \frac{s^2 + (\omega_z/Q_z)s + \omega_z^2}{s^2 + (\omega_p/Q_p)s + \omega_p^2} \end{aligned}$$

$$\omega_p = \text{Pole Frequency} = |p_1| = |p_2|$$

$$\omega_z = \text{Zero Frequency} = |z_1| = |z_2|$$

$$Q_p = \text{Pole Quality Factor} = \frac{\omega_p}{2\text{Re}(p_1)}$$

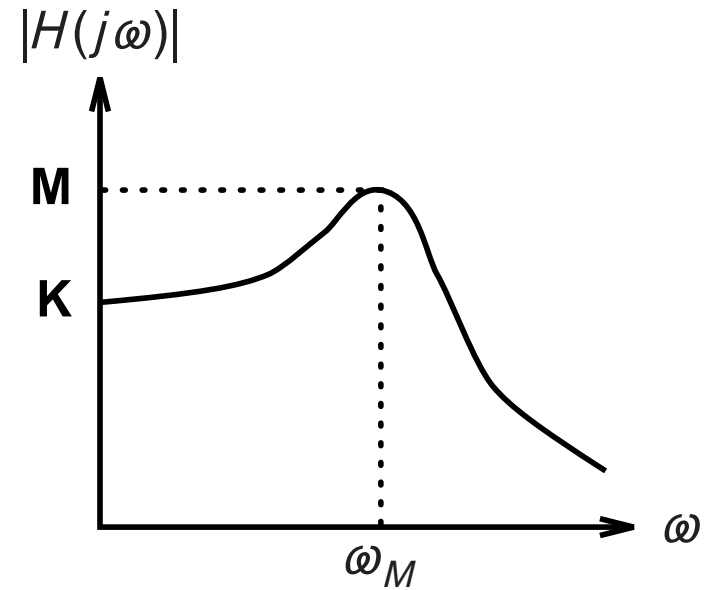
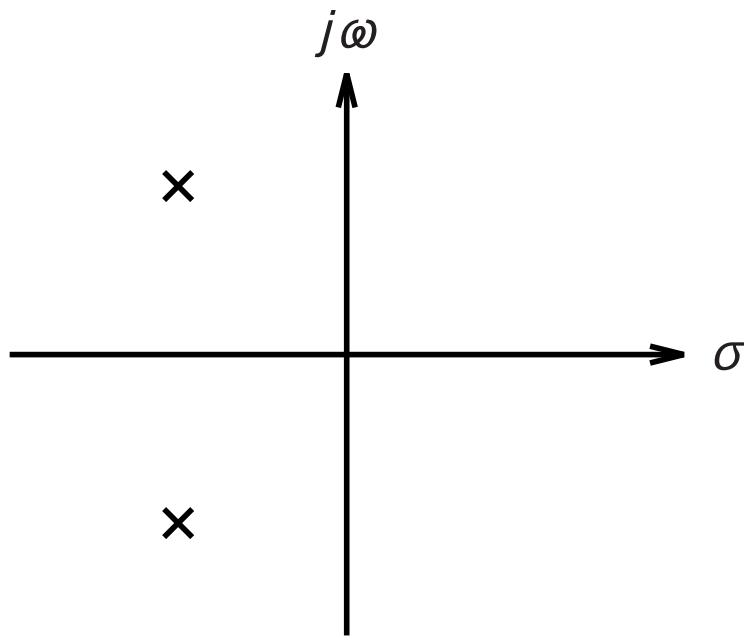
$$Q_z = \text{Zero Quality Factor} = \frac{\omega_z}{2\text{Re}(z_1)}$$

## Second-Order Filter (Biquadratic Function)

---

- For complex poles and zeros,  $z_2 = z_1^*$  and  $p_2 = p_1^*$ .
- $H(0) = K \omega_z^2 / \omega_p^2$  and  $H(\infty) = K$ .
- $|H(j\omega)|$  is maximum, at  $\omega \approx \omega_p$ .
- The sharpness of the maximum is determined by  $Q_p$ .
- $|H(j\omega)|$  is minimum, at  $\omega \approx \omega_z$ .
- The depth of the minimum is determined by  $Q_z$ .

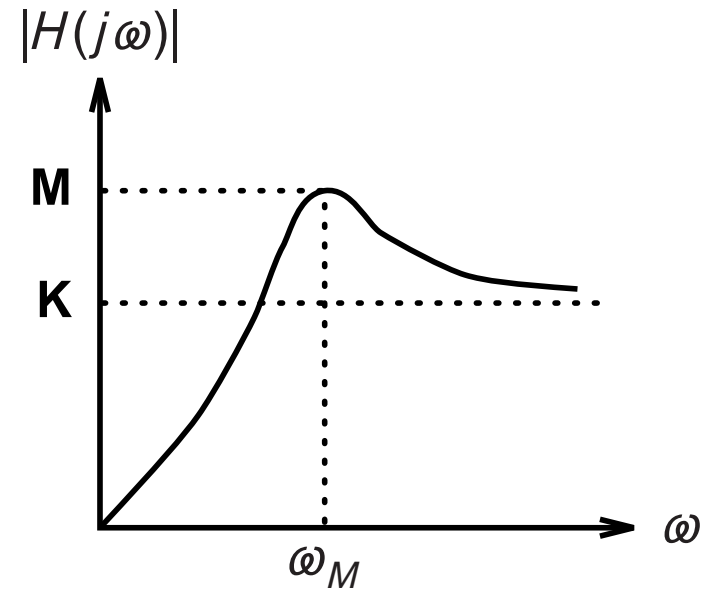
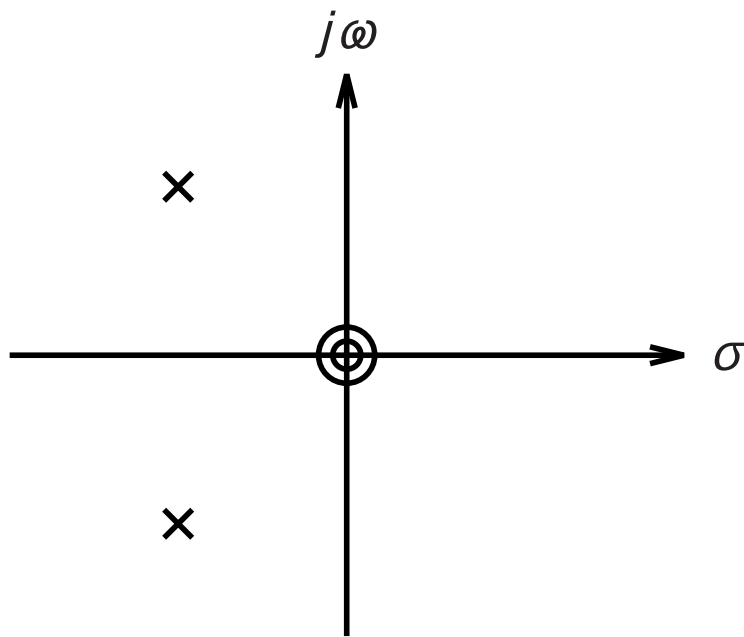
# Second-Order Low-Pass (LP) Filter



$$H(s) = \frac{K \omega_p^2}{s^2 + (\omega_p/Q_p)s + \omega_p^2}$$

$$\omega_M = \omega_p \cdot \sqrt{1 - 1/(2Q^2)} \quad M = \frac{KQ}{\sqrt{1 - 1/(4Q^2)}}$$

# Second-Order High-Pass (HP) Filter

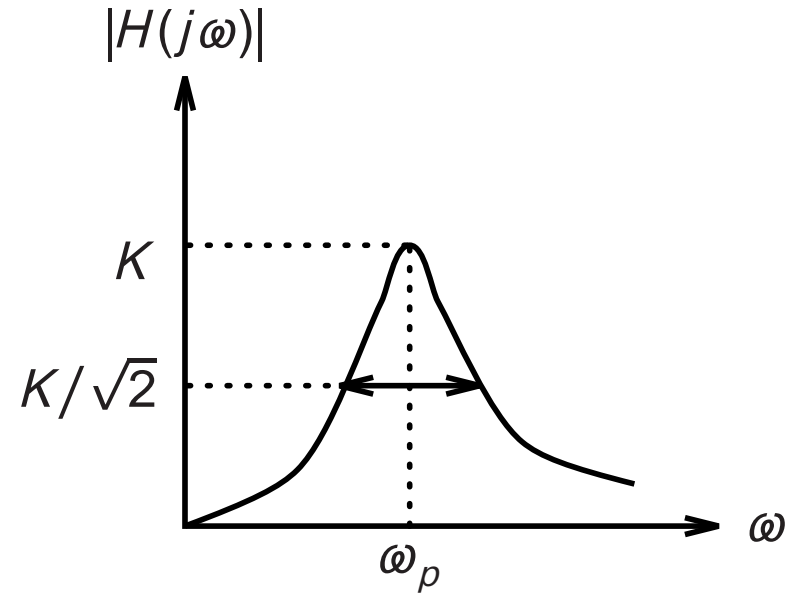
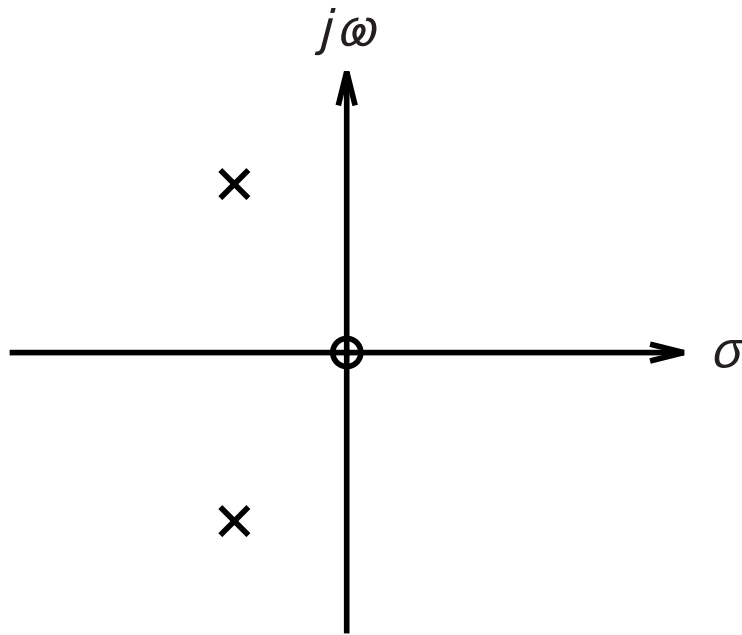


$$H(s) = \frac{Ks^2}{s^2 + (\omega_p/Q_p)s + \omega_p^2}$$

$$\omega_M = \frac{\omega_p}{\sqrt{1 - 1/(2Q^2)}}$$

$$M = \frac{KQ}{\sqrt{1 - 1/(4Q^2)}}$$

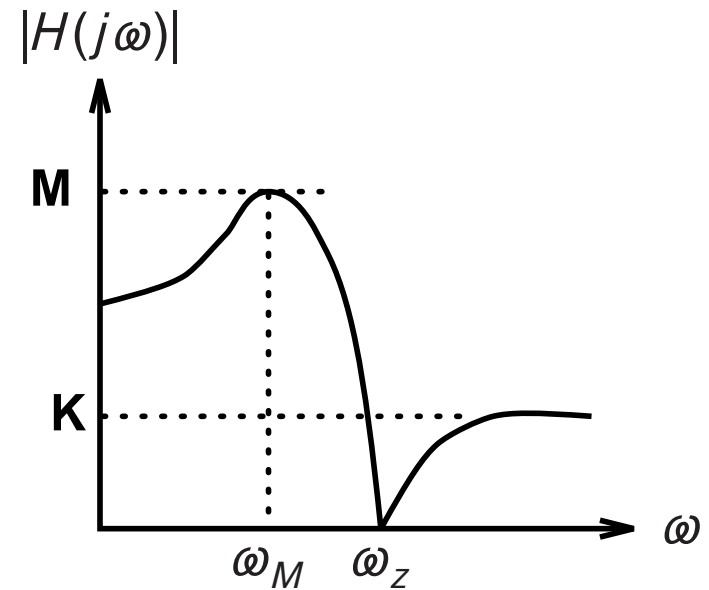
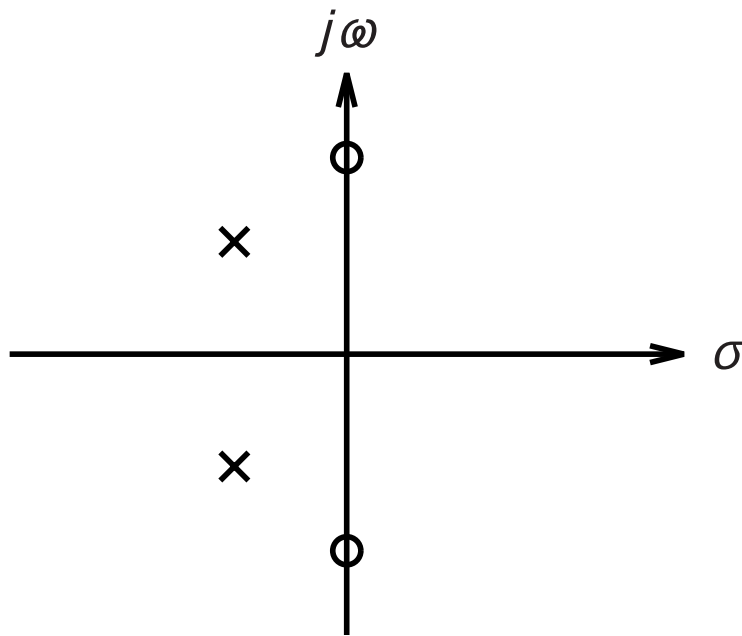
# Second-Order Band-Pass (BP) Filter



$$H(s) = \frac{K(\omega_p/Q_p)s}{s^2 + (\omega_p/Q_p)s + \omega_p^2}$$

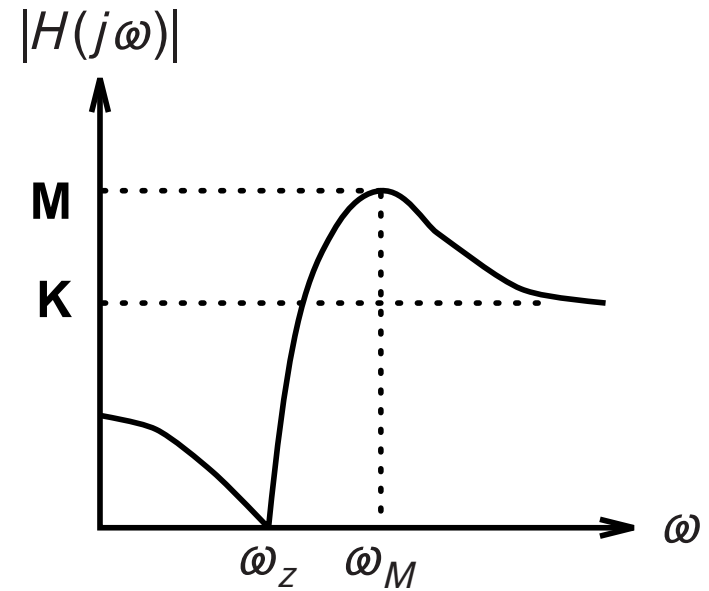
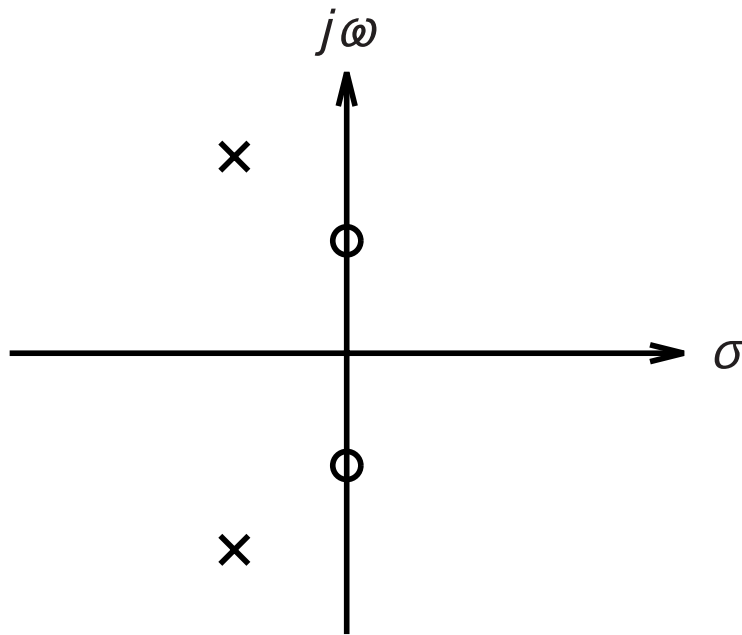
$$3 \text{ dB Bandwidth} = \frac{\omega_p}{Q_p}$$

# Second-Order Band-Reject (BR) Filter — Low-Pass Notch (LPN)



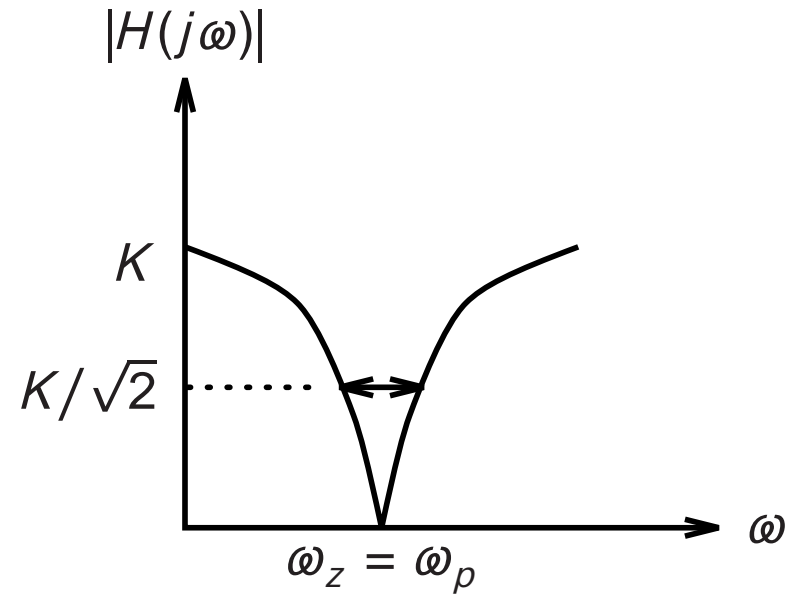
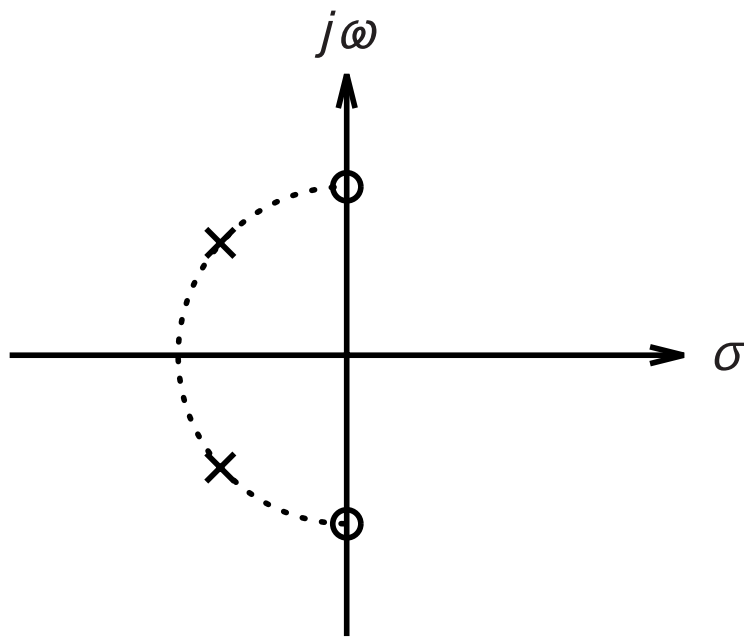
$$H(s) = \frac{K(s^2 + \omega_z^2)}{s^2 + (\omega_p/Q_p)s + \omega_p^2} \quad \omega_z > \omega_p$$

# Second-Order Band-Reject (BR) Filter — High-Pass Notch (HPN)



$$H(s) = \frac{K(s^2 + \omega_z^2)}{s^2 + (\omega_p/Q_p)s + \omega_p^2} \quad \omega_z < \omega_p$$

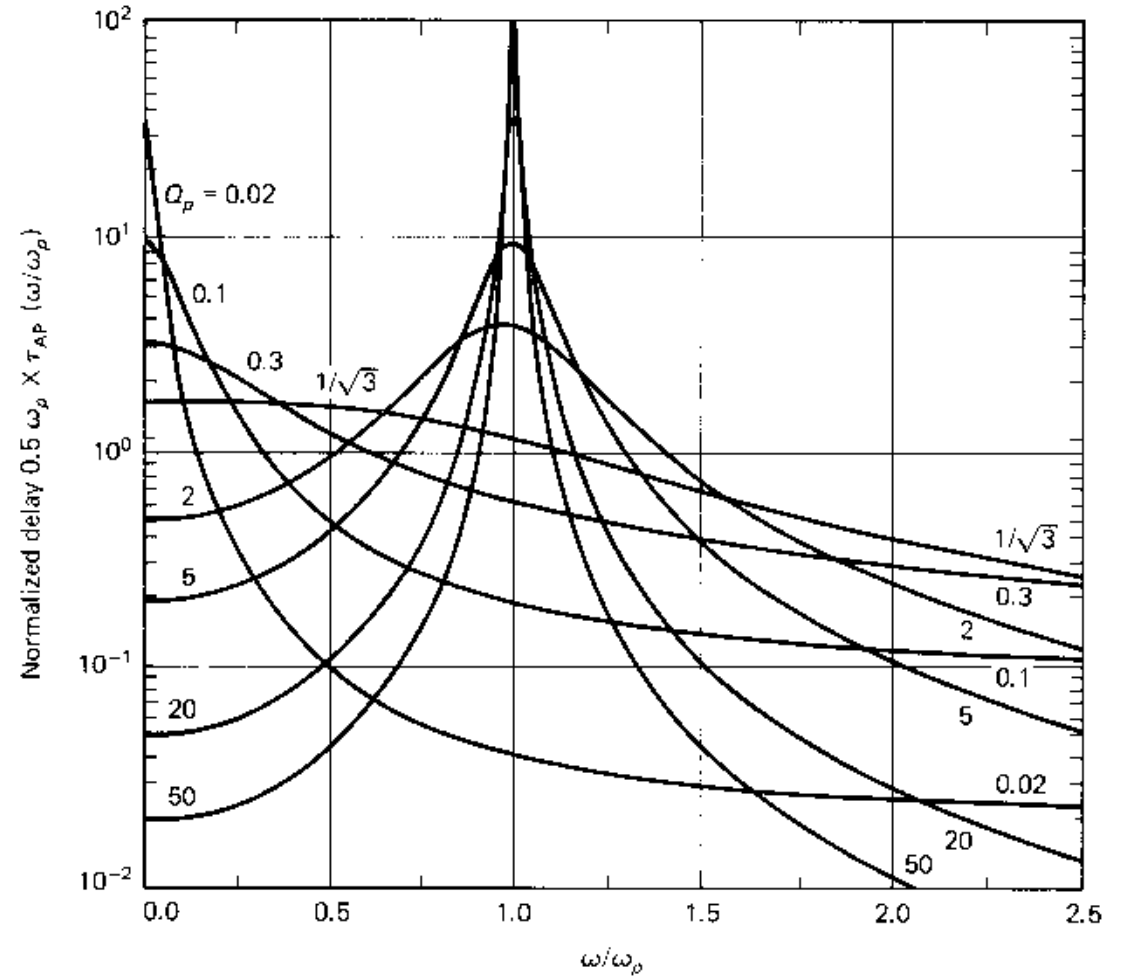
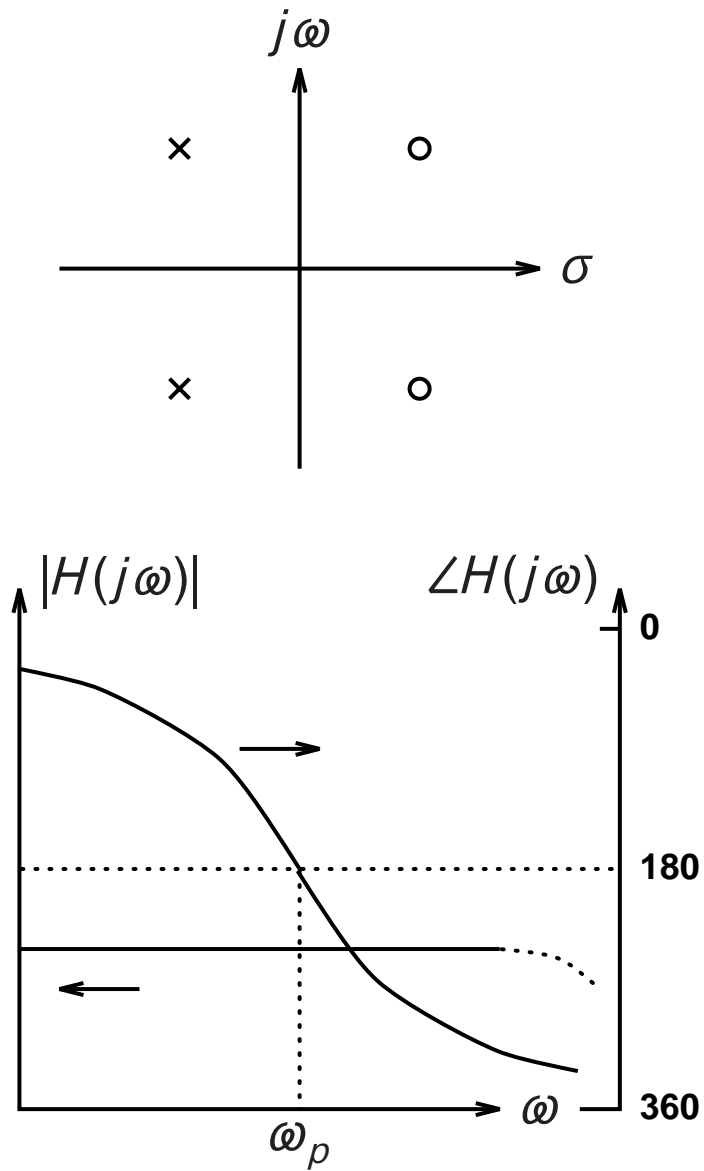
# Second-Order Band-Reject (BR) Filter — Symmetrical Notch



$$H(s) = \frac{K(s^2 + \omega_z^2)}{s^2 + (\omega_p/Q_p)s + \omega_p^2} \quad \omega_z = \omega_p$$

$$3 \text{ dB Notch Width} = \frac{\omega_p}{Q_p}$$

# Second-Order All-Pass (AP) Filter



## Second-Order All-Pass (AP) Filter

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$$H(s) = K \cdot \frac{s^2 - (\omega_p/Q_p)s + \omega_p^2}{s^2 + (\omega_p/Q_p)s + \omega_p^2} \quad |H(j\omega)| = K$$

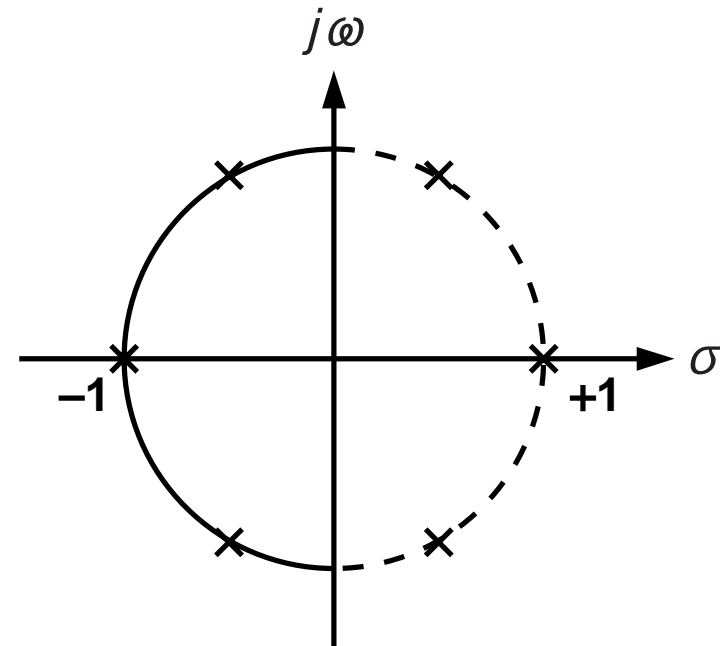
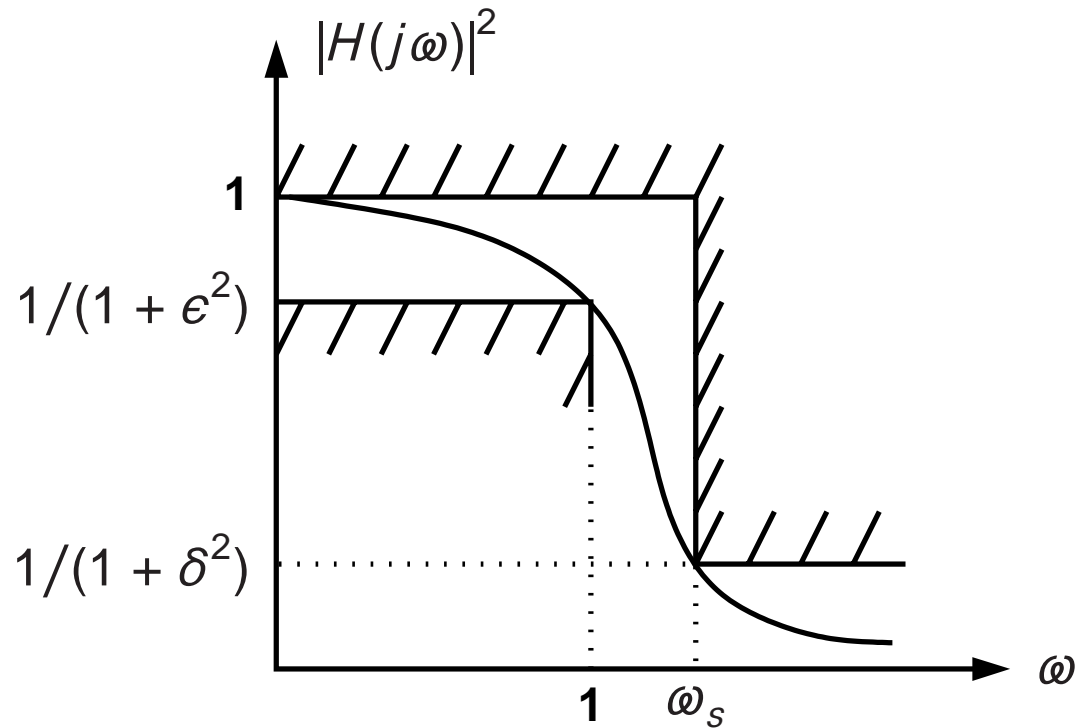
$$\phi(\omega_n) = -2 \tan^{-1} \frac{\omega_n/Q_p}{1 - \omega_n^2} \quad \omega_n = \frac{\omega}{\omega_p}$$

$$\text{Group Delay} = \tau = -\frac{d\phi(\omega)}{d\omega} \quad \tau_n(\omega_n) = \omega_p \tau(\omega_n) = \frac{2}{Q_p} \cdot \frac{1 + \omega_n^2}{(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2}$$

- For  $Q_p = 1/\sqrt{3}$ , the delay curve is maximally flat.
- For  $Q_p > 1/\sqrt{3}$ ,  $\tau$  has a peaking,  $\tau_{n,max} \approx 4Q_p/\omega_p$  at  $\omega_n \approx \sqrt{1 - 1/(4Q_p^2)}$ .
- For 2nd-order filters,

$$\tau_{n,(LP,HP,BP,BR)}(\omega_n) = \frac{1}{2} \tau_{n,AP}(\omega_n)$$

# Maximally Flat (Butterworth) Filters



$$|H(j\omega)|^2 = \frac{1}{1 + \epsilon^2 \omega^{2N}}$$

$$\text{Poles} = s_k = e^{-1/N} \cdot \exp\left(j \frac{2k + N - 1}{2N} \pi\right) \quad k = 1, 2, \dots, N$$

# Maximally Flat (Butterworth) Filters

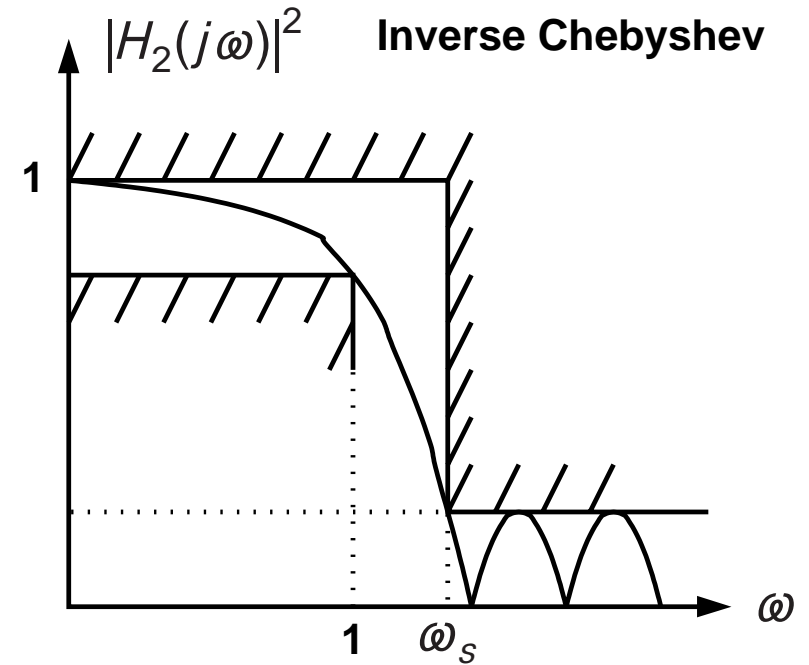
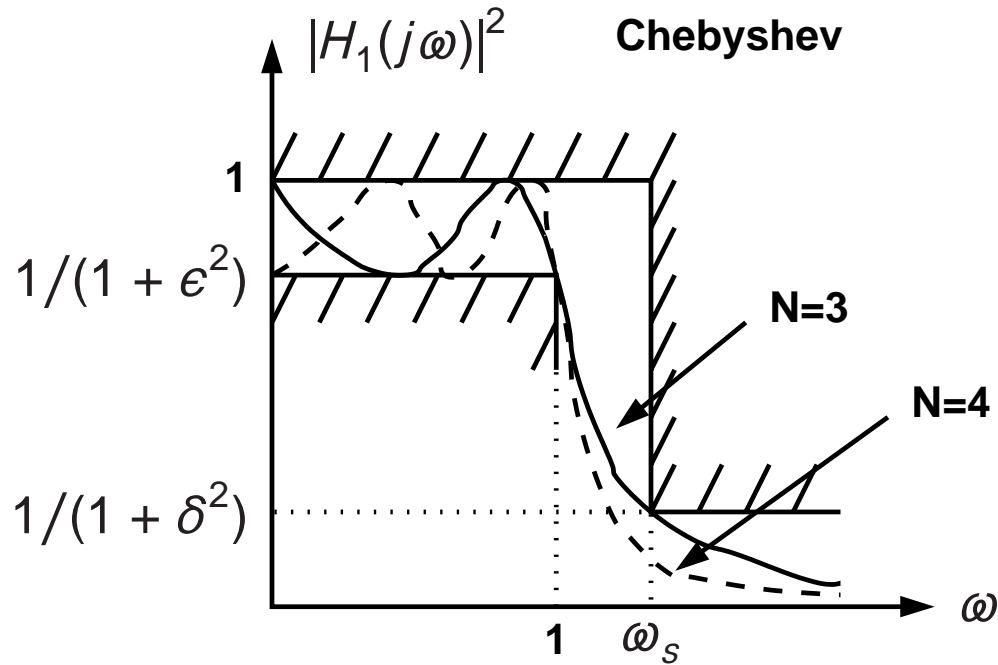
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The relationship between the filter order,  $N$ , and the steepness of the magnitude response is

$$N \geq \frac{\log \delta - \log \epsilon}{\log \omega_s}$$

- Good flatness in passband.
- Poor phase linearity.
- Moderate attenuation slope steepness.

# Equi-Ripple (Chebyshev) Filters



$$\text{Chebyshev} = |H_1(j\omega)|^2 = \frac{1}{1 + \epsilon^2 C_N^2(\omega)}$$

$$\text{Inverse Chebyshev} = |H_2(j\omega)|^2 = \frac{\epsilon^2 C_N^2(1/\omega)}{1 + \epsilon^2 C_N^2(1/\omega)}$$

# Equi-Ripple (Chebyshev) Filters

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The function  $C_N$  is

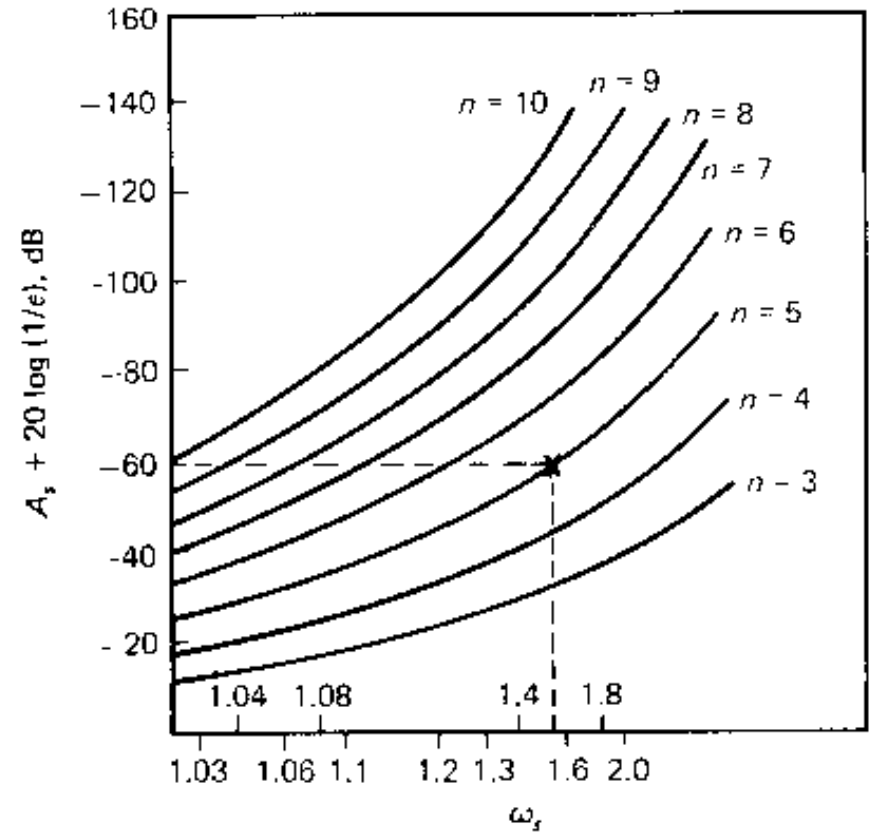
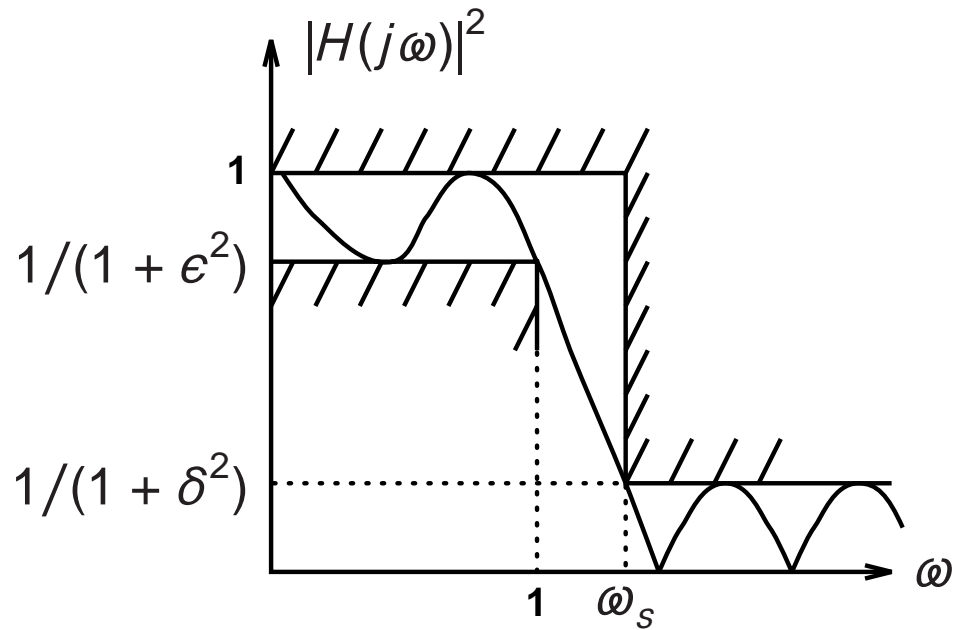
$$\begin{aligned}C_N(\omega) &= \cos[N \cos^{-1}(\omega)] \text{ for } \omega \leq 1 \\ &= \cosh[N \cosh^{-1}(\omega)] \text{ for } \omega > 1 \\ &= 2\omega C_{N-1}(\omega) - C_{N-2}(\omega)\end{aligned}$$

The relationship between the filter order,  $N$ , and the steepness of the magnitude response is

$$N \geq \frac{\cosh^{-1}(\delta/\epsilon)}{\cosh^{-1} \omega_s} \approx \frac{\ln(2\delta/\epsilon)}{\ln\left(\omega_s + \sqrt{\omega_s^2 - 1}\right)}$$

- Good steepness of the attenuation slope.
- Poorer phase linearity and passband flatness than the Butterworth filters.
- Inverse Chebyshev filters have better phase and delay performance.

# Elliptic (Cauer) Filters



$$|H(j\omega)|^2 = \frac{1}{1 + \epsilon^2 R_N^2(\omega)}$$

# Elliptic (Cauer) Filters

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The function  $R_N$  is

$$\begin{aligned} R_N(\omega) &= k \prod_{i=1}^{N/2} \frac{\omega^2 - (\omega_s/\omega_{zi})^2}{\omega^2 - \omega_{zi}^2} \quad \text{for } N \text{ even} \\ &= k\omega \prod_{i=1}^{(N-1)/2} \frac{\omega^2 - (\omega_s/\omega_{zi})^2}{\omega^2 - \omega_{zi}^2} \quad \text{for } N \text{ odd} \end{aligned}$$

In the stopband, if  $\epsilon^2 R_N^2(\omega) \gg 1$ ,

$$20 \log \frac{\delta}{\epsilon} \approx 20 \log |R_N(\omega_s)|$$

- Best steepness of the attenuation slope.
- Poor phase linearity.

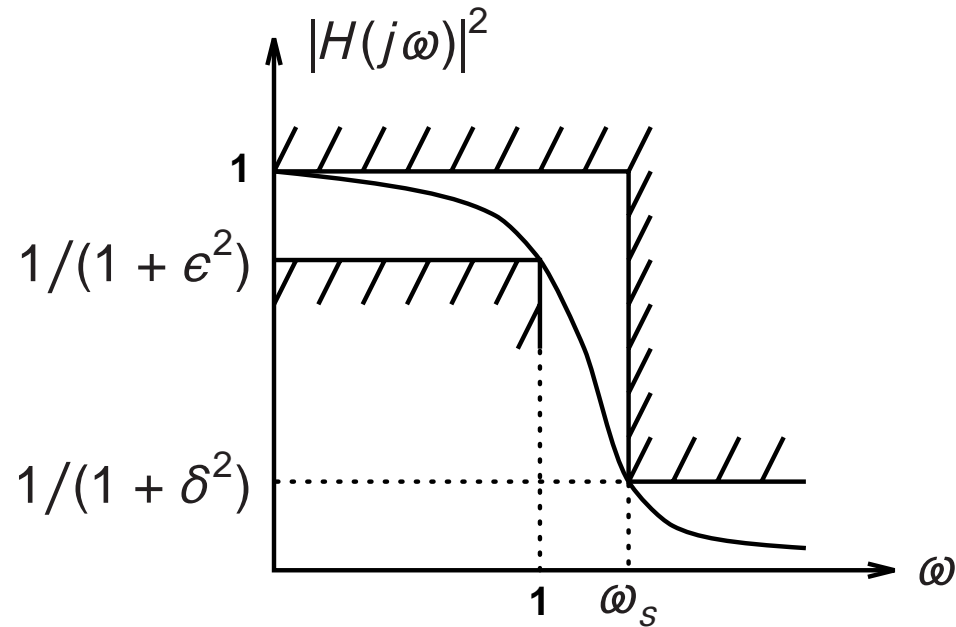
# Comparison of the Classical Filter Responses

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Comparing filters that satisfy the same  $\delta$  and  $\epsilon$  requirements:

- The Cauer filter has the lowest order, while the Butterworth filter has the highest order.
- The Butterworth filter has the best passband performance, and the inverse Chebyshev filter is a close second.
- The Cauer filter has the largest pole quality factor; next is the Chebyshev filter, followed by the inverse Chebyshev and the Butterworth filters.
- The Chebyshev filter has the worst group delay variation; next is the inverse Chebyshev filter, followed by the Butterworth and the Cauer filters.
- The Butterworth and the Chebyshev are all-pole filter, while the inverse Chebyshev and Cauer filters have finite transmission zeros.
- The inverse Chebyshev filters have low order, modest Q values, good delay performance, and minimal passband attenuation, making them most attractive.

# Linear-Phase (Bessel-Thomson) Filters



$$H(s) = \frac{b_0}{D(s)} \quad D(s) = \sum_{i=0}^N b_i s^i \quad b_i = \frac{(2N - i)!}{2^{N-i} i! (N - i)!} \quad i = 0, 1, \dots, N - 1$$

$D(s)$  is related to Bessel polynomials.

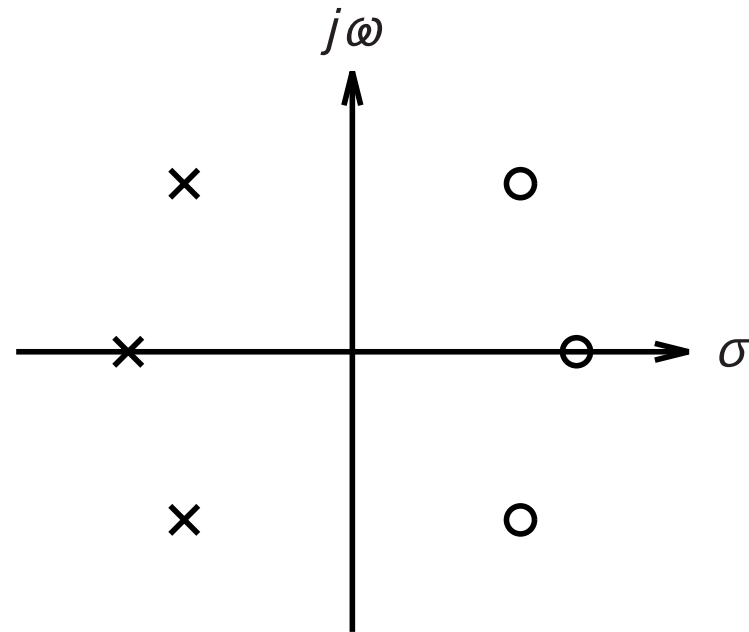
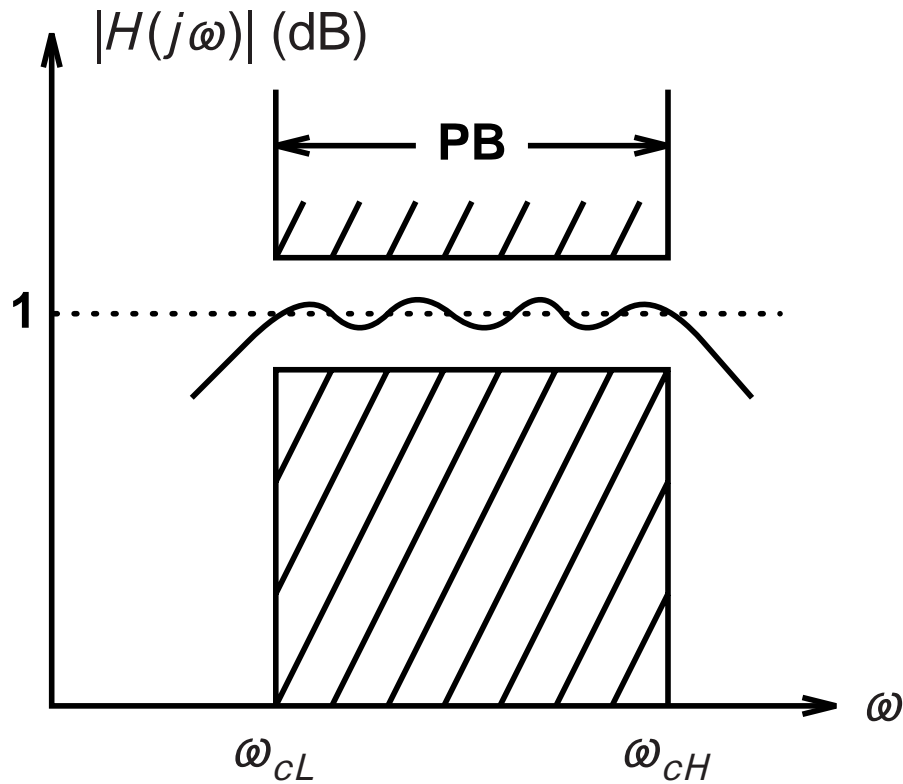
$$D(s) = (2N - 1)D_{N-1} + s^2 D_{N-2}$$

# Linear-Phase (Bessel or Thomson) Filters

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- Approximate the linear-phase response.
- Poor steepness of the attenuation slope.
- It is usually more efficient to use a Butterworth, Chebyshev or a Cauer filter cascaded with an all-pass filter to achieve required gain and linear-phase response.

# All-Pass Filter (Delay Equalizer) Specifications



$$H(j\omega) = |H(j\omega)|e^{j\phi(\omega)}$$

$$\text{Group Delay} = \tau(\omega) = -\frac{d\phi(\omega)}{d\omega}$$

# Frequency Transformations

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## Low-Pass to High-Pass Transformation

$$H_{\text{HP}}(s) = H_{\text{LP}}\left(\frac{1}{s}\right)$$

- For RC active filters, it is an RC-CR transformation.

## Low-Pass to Band-Pass Transformation

$$H_{\text{BP}}(s) = H_{\text{LP}}\left(Q \cdot \frac{s^2 + 1}{s}\right)$$

- $Q = \omega_o/B$  is the quality factor, where  $\omega_o$  is the center frequency,  $B = \omega_{cH} - \omega_{cL}$  is the passband bandwidth.
- Transformation always results in symmetrical band-pass filters.

# Frequency Transformations

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## Low-Pass to Band-Reject Transformation

$$H_{BR}(s) = H_{LP} \left( \frac{1}{Q} \cdot \frac{s}{s^2 + 1} \right)$$

- $Q = \omega_o/B$  is the quality factor, where  $\omega_o$  is the center frequency,  $B = \omega_{sH} - \omega_{sL}$  is the passband bandwidth.
- Transformation always results in symmetrical band-reject filters.

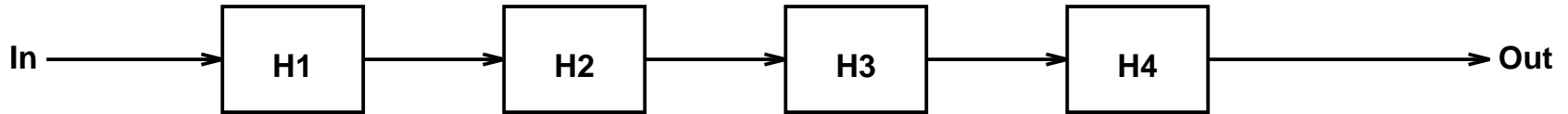
## Frequency Scaling

$$H'(s) = H\left(\frac{s}{a}\right)$$

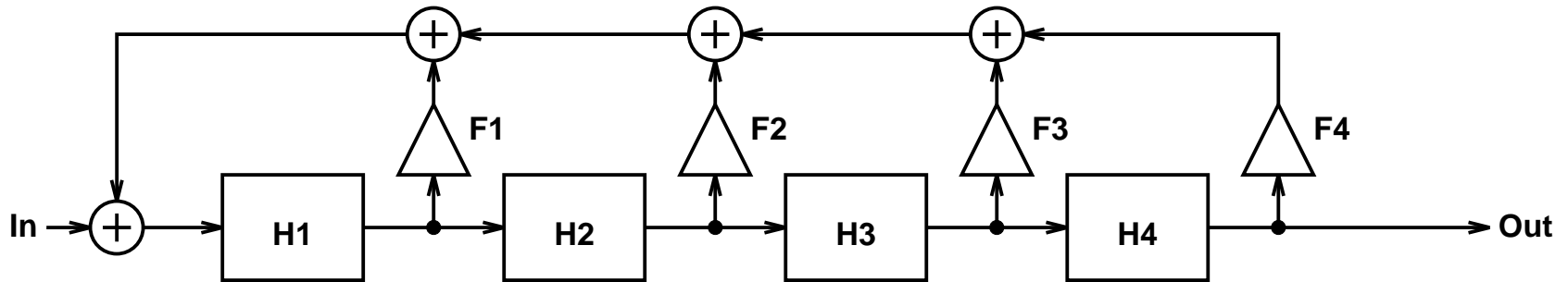
- So that  $\omega'_c = a \cdot \omega_c$ ,  $\omega'_s = a \cdot \omega_s$ ,  $\omega'_o = a \cdot \omega_o$

# High-Order Filters

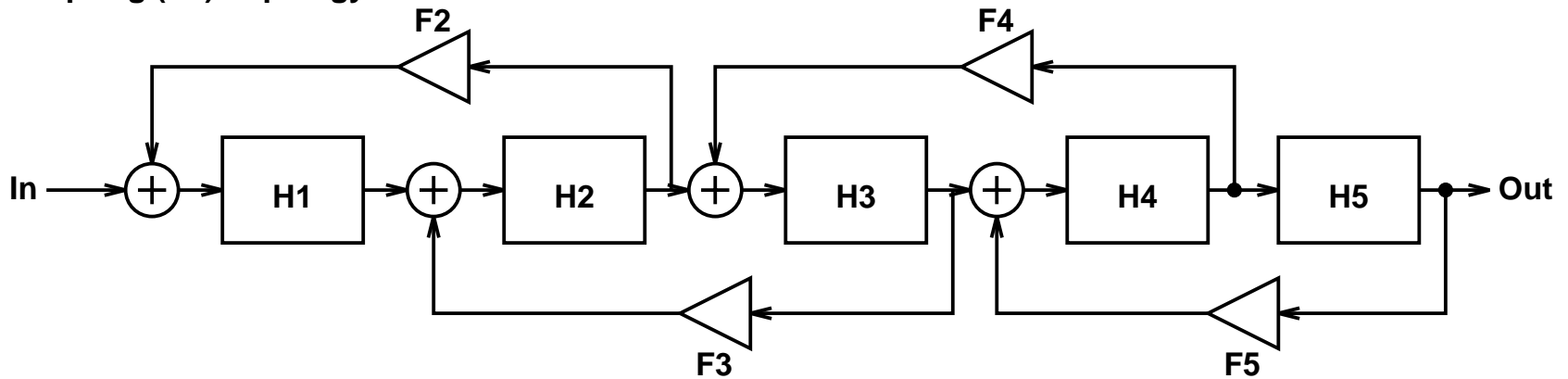
Cascade Topology



Follow-the-Leader Feedback (FLF) Topology



Leapfrog (LF) Topology



# High-Order Filters

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Cascade Topology:

$$H(s) = H_1 \cdot H_2 \cdot H_3 \cdot H_4$$

Follow-the-Leader Feedback (FLF) Topology:

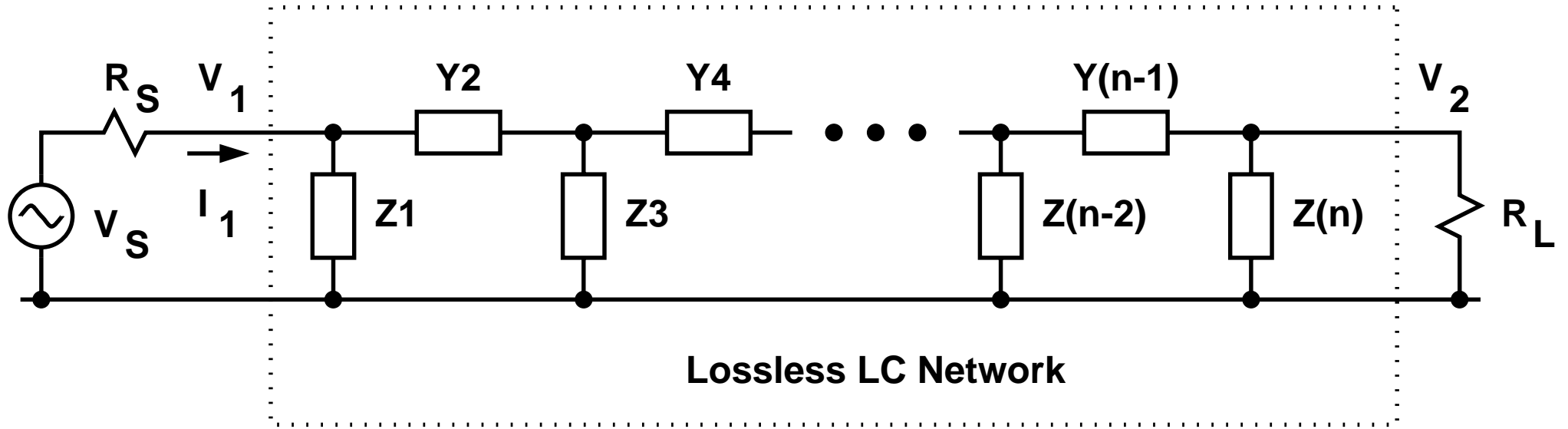
$$H(s) = \frac{H_1 H_2 H_3 H_4}{1 + F_1 H_1 + F_2 H_1 H_2 + F_3 H_1 H_2 H_3 + F_4 H_1 H_2 H_3 H_4}$$

Leapfrog Topology:

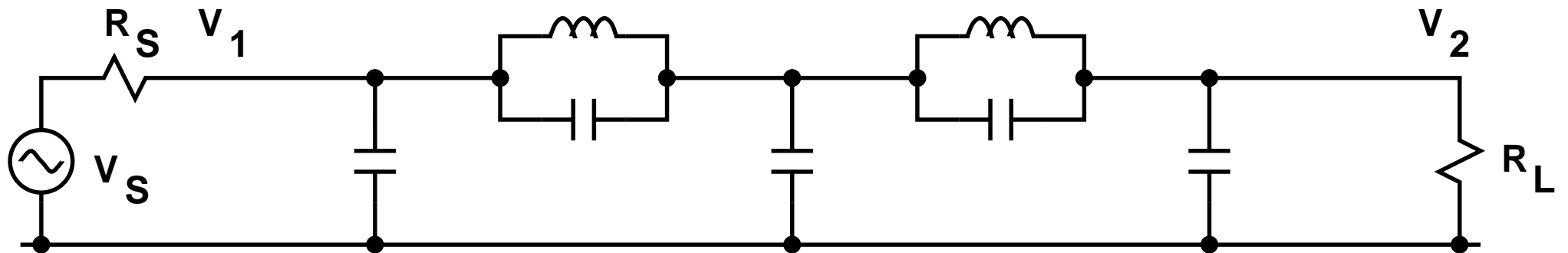
$$H(s) = \frac{H_1 H_2 H_3 H_4 H_5}{D(s)}$$

$$D(s) = 1 + F_2 H_1 H_2 + F_3 H_2 H_3 + F_4 H_4 H_4 + F_5 H_4 H_5 \\ + F_2 F_4 H_1 H_2 H_3 H_4 + F_2 F_5 H_1 H_2 H_4 H_5 + F_3 F_5 H_2 H_3 H_4 H_5$$

# LC Ladder Filters



## A Fifth-Order Elliptic Low-Pass Filter



## LC Ladder Filters

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When designed for maximum power transfer, the LC ladder filters are inherently insensitive to component variations, particularly in their passband.

$$\text{Input Power} = P_1 = |I_1(j\omega)|^2 \text{Re}\{Z_{in}(j\omega)\} = \frac{|V_S|^2}{|R_S + Z_{in}(j\omega)|^2} \text{Re}\{Z_{in}(j\omega)\}$$

$$\text{Maximum Input Power} = P_{1,max} = \frac{1}{4} \frac{|V_S|^2}{R_S} \quad \text{Output Power} = P_2 = \frac{|V_2|^2}{R_L}$$

$$H(s) = \sqrt{\frac{4R_S}{R_L}} \cdot \frac{V_2}{V_S} = \frac{N(s)}{D(s)} \quad |H(j\omega)|^2 = \frac{4R_S}{R_L} \cdot \left| \frac{V_2}{V_S} \right|^2 \leq 1$$

$$|H(j\omega)|^2 = 1 - \left| \frac{R_S - Z_{in}(j\omega)}{R_S + Z_{in}(j\omega)} \right|^2 = 1 - |\rho(j\omega)|^2 \quad \rho(s) = \pm \frac{R_S - Z_{in}(s)}{(R_S + Z_{in}(s))}$$

- $\rho(s)$  is the reflection coefficient.

# Sensitivity

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Let  $P$  is a function of  $x$ . The *sensitivity* of  $P$  with respect to  $x$  is defined as:

$$S_x^P = \frac{\partial P/P}{dx/x} = \frac{x}{P} \cdot \frac{\partial P}{\partial x} = \frac{\partial(\ln P)}{\partial(\ln x)}$$

The *semirelative sensitivity* is defined as

$$Q_x^P = \frac{\partial P}{\partial x/x} = x \cdot \frac{\partial P}{\partial x}$$

- Some useful relationships:

$$S_x^{P_1 P_2} = S_x^{P_1} + S_x^{P_2} \quad S_x^{P_1/P_2} = S_x^{P_1} - S_x^{P_2} \quad S_x^P = S_y^P \cdot S_x^y$$

# Sensitivity

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- Let  $Y$  is a function of  $x_1, x_2, \dots, x_n$ .

$$dY = \frac{\partial Y}{\partial x_1} \cdot dx_1 + \frac{\partial Y}{\partial x_2} \cdot dx_2 + \dots + \frac{\partial Y}{\partial x_n} \cdot dx_n$$

$$\frac{dY}{Y} = S_{x_1}^Y \cdot \frac{dx_1}{x_1} + S_{x_2}^Y \cdot \frac{dx_2}{x_2} + \dots + S_{x_n}^Y \cdot \frac{dx_n}{x_n}$$

- Let the forward gain  $T = T_1 \cdot T_2$ , we have

$$S_{T_2}^T = \frac{T_2}{T} \cdot \frac{\partial T}{\partial T_2} = 1$$

With negative feedback factor  $H$ , we have

$$T = \frac{T_1 T_2}{1 + H T_1 T_2} \quad \Rightarrow \quad S_{T_2}^T = \frac{T_2}{T} \cdot \frac{\partial T}{\partial T_2} = \frac{1}{1 + H T_1 T_2}$$

The  $T$  sensitivity is reduced by the loop gain  $H T_1 T_2$

# Transfer Function Sensitivity

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Let the transfer function be

$$H(s) = \frac{N(s)}{D(s)} = \frac{a_m s^m + \dots + a_1 s + a_0}{b_n s^n + \dots + b_1 s + b_0} = K \cdot \frac{(s - z_1)(s - z_2) \dots (s - z_m)}{(s - p_1)(s - p_2) \dots (s - p_n)}$$

The sensitivity is

$$\begin{aligned} S_x^H &= S_x^N - S_x^D = \frac{\partial \ln N}{\partial \ln x} - \frac{\partial \ln D}{\partial \ln x} \\ &= S_x^K + x \frac{\partial}{\partial x} \{ [\ln(s - z_1) + \dots + \ln(s - z_m)] - [\ln(s - p_1) + \dots + \ln(s - p_n)] \} \\ &= S_x^K - \left[ \frac{x \frac{\partial z_1}{\partial x}}{s - z_1} + \dots + \frac{x \frac{\partial z_m}{\partial x}}{s - z_m} \right] + \left[ \frac{x \frac{\partial p_1}{\partial x}}{s - p_1} + \dots + \frac{x \frac{\partial p_n}{\partial x}}{s - p_n} \right] \\ &= S_x^K - \left[ \frac{z_1 S_x^{z_1}}{s - z_1} + \dots + \frac{z_m S_x^{z_m}}{s - z_m} \right] + \left[ \frac{p_1 S_x^{p_1}}{s - p_1} + \dots + \frac{p_n S_x^{p_n}}{s - p_n} \right] \end{aligned}$$

# Transfer Function Sensitivity

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- Any pole or zero shift influences  $H(s)$  most strongly in the neighborhood of that pole or zero.
- $S_x^H \rightarrow \infty$  at a  $j\omega$ -axis transmission zero  $z_i = j\omega_{z_i}$ .
- For frequencies  $s = j\omega$  in the neighborhood of pole with large quality factor, high sensitivities are expected.
- Sensitivities are normally largest at the passband corner.

# Second-Order Filter Sensitivity

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The Biquadratic function is

$$H(s) = \frac{N(s)}{D(s)} = \frac{a_2(s - z_1)(s - z_2)}{(s - p_1)(s - p_2)} = \frac{a_2s^2 + a_1s + a_0}{s^2 + (\omega_p/Q_p)s + \omega_p^2}$$

$$p_1 = -\omega_p \left( \frac{1}{2Q_p} - j\sqrt{1 - \frac{1}{4Q_p^2}} \right) \quad p_2 = p_1^* = -\omega_p \left( \frac{1}{2Q_p} + j\sqrt{1 - \frac{1}{4Q_p^2}} \right)$$

The sensitivity of the poles are

$$S_x^{p_1} = S_x^{\omega_p} - j \frac{S_x^{Q_p}}{\sqrt{4Q_p^2 - 1}} \quad S_x^{p_2} = (S_x^{p_1})^* = S_x^{\omega_p} + j \frac{S_x^{Q_p}}{\sqrt{4Q_p^2 - 1}}$$

- The pole is  $\sqrt{4Q_p^2 - 1} \approx 2Q_p$  times more sensitive to variations in  $\omega_p$  than to variations in  $Q_p$ .

## Second-Order Filter Sensitivity

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The transfer function can be expressed as  $H(j\omega) = |H(j\omega)|e^{j\theta(\omega)}$ , then

$$S_x^{H(j\omega)} = \frac{\partial \ln H(j\omega)}{\partial \ln x} = \frac{\partial \ln |H(j\omega)|}{\partial \ln x} + jx \frac{\partial \theta(\omega)}{\partial x} = S_x^{|H(j\omega)|} + j\theta(\omega) S_x^{\theta(\omega)}$$

Consider only the effects of poles on the passband of  $H(s)$

$$S^{H(s)}_x = -\frac{x}{D(s)} \frac{\partial D(s)}{\partial x} = -\frac{\left(\frac{s\omega_p}{Q_p} + 2\omega_p^2\right) S_x^{\omega_p} - \frac{s\omega_p}{Q_p} S_x^{Q_p}}{s^2 + (\omega_p/Q_p)s + \omega_p^2} = -\frac{\left(\frac{s_n}{Q_p} + 2\right) S_x^{\omega_p} - \frac{s_n}{Q_p} S_x^{Q_p}}{s_n^2 + s_n/Q_p + 1}$$

$$S_x^{H(j\omega)} = -\frac{\left[\left(\frac{\omega_n}{Q_p}\right)^2 + 2(1 - \omega_n^2)\right] S_x^{\omega_p} - \left(\frac{\omega_n}{Q_p}\right)^2 S_x^{Q_p}}{(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2} + j\frac{\omega_n}{Q_p} \frac{(1 + \omega_n^2) S_x^{\omega_p} + (1 - \omega_n^2) S_x^{Q_p}}{(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2}$$

$$s_n = \frac{s}{\omega_p} \quad \omega_n = \frac{\omega}{\omega_p}$$

## Second-Order Filter Sensitivity

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We have

$$S_x^{|H(j\omega)|} = -\frac{2(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2}{(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2} \cdot S_x^{\omega_p} + \frac{(\omega_n/Q_p)^2}{(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2} \cdot S_x^{Q_p}$$

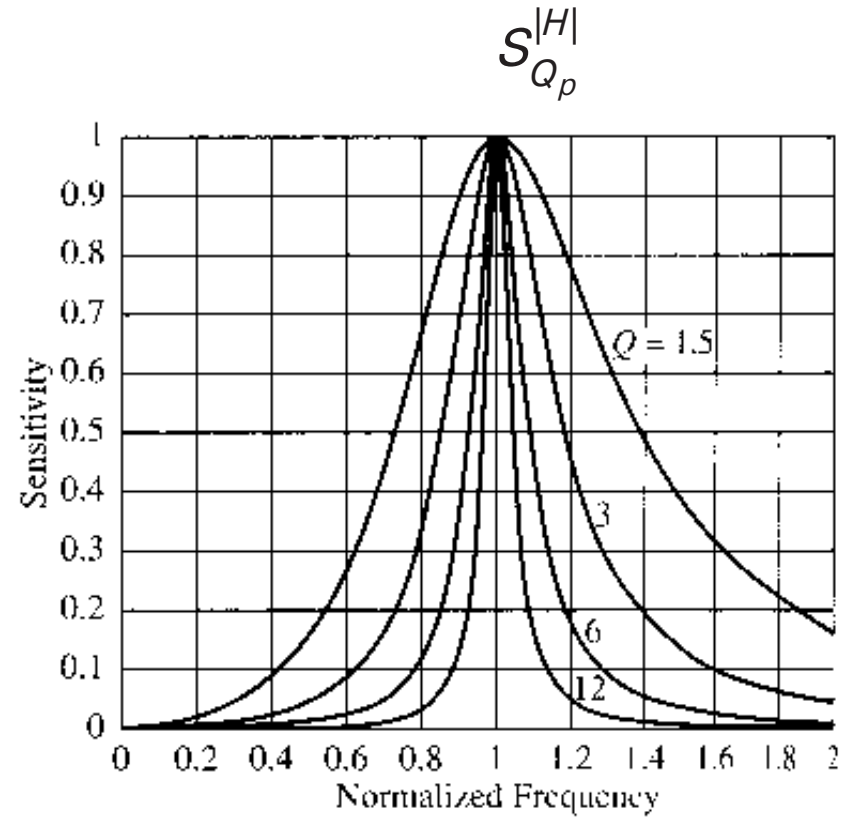
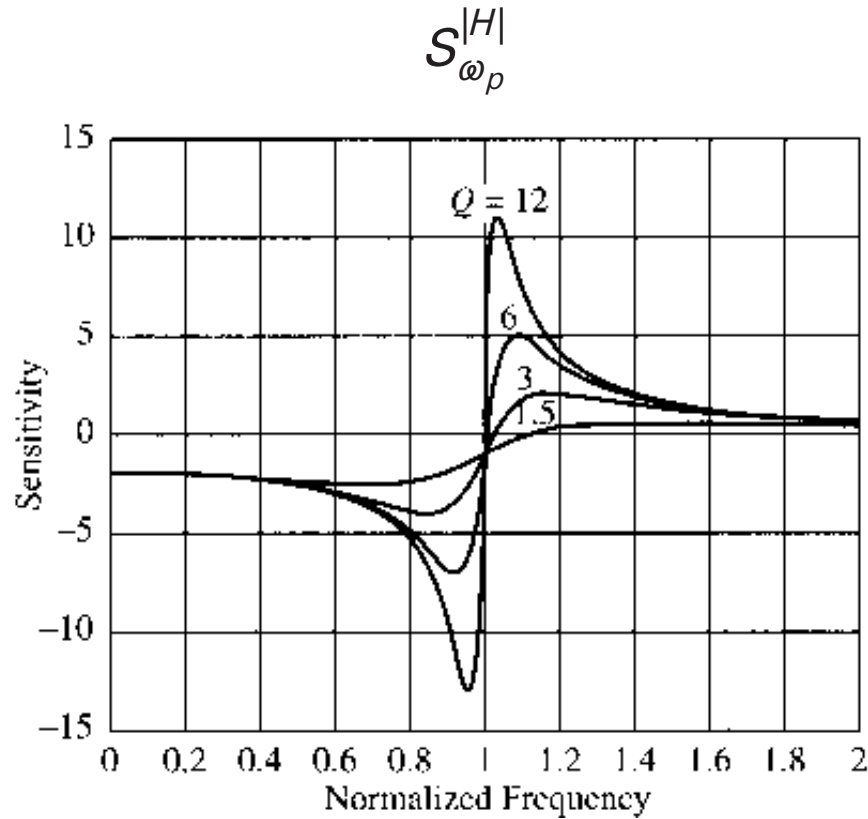
$$\theta(\omega) S_x^{\theta(\omega)} = x \frac{\partial \theta(\omega)}{\partial x} = \frac{(1 + \omega_n^2)^2 (\omega_n/Q_p)}{(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2} \cdot S_x^{\omega_p} + \frac{(1 - \omega_n^2)^2 (\omega_n/Q_p)}{(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2} \cdot S_x^{Q_p}$$

And

$$S_x^{|H(j\omega)|} = S_{\omega_p}^{|H|} \cdot S_x^{\omega_p} + S_{Q_p}^{|H|} \cdot S_x^{Q_p}$$

$$\Rightarrow S_{\omega_p}^{|H|} = -\frac{2(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2}{(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2} \quad S_{Q_p}^{|H|} = \frac{(\omega_n/Q_p)^2}{(1 - \omega_n^2)^2 + (\omega_n/Q_p)^2}$$

# Second-Order Filter Sensitivity



$$\max\{S_{\omega_p}^{|H|}\} \approx \frac{Q_p}{1 + 1/Q_p} \quad \text{at} \quad \omega_n \approx 1 + \frac{1}{2Q_p}$$

$$\max\{S_{Q_p}^{|H|}\} = 1 \quad \text{at} \quad \omega_n = 1$$

$$\min\{S_{\omega_p}^{|H|}\} \approx -\frac{Q_p}{1 - 1/Q_p} \quad \text{at} \quad \omega_n \approx 1 - \frac{1}{2Q_p}$$

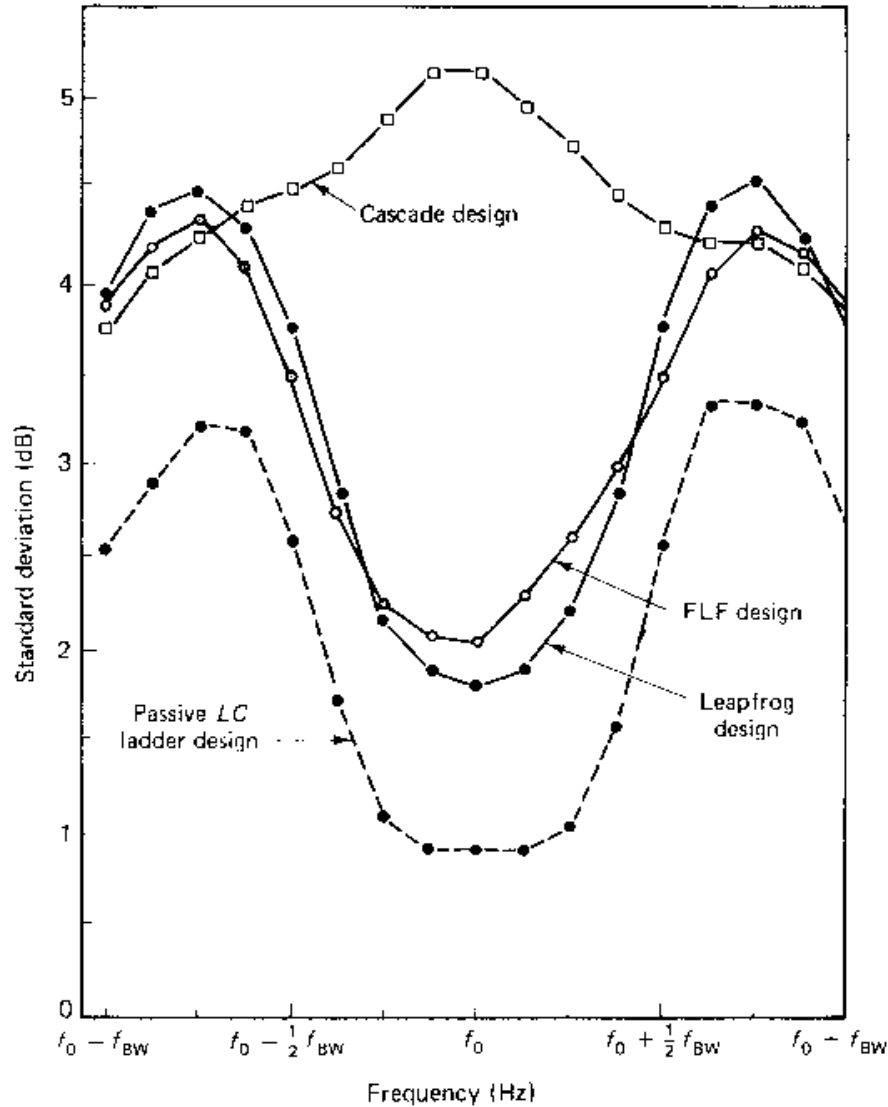
## Second-Order Filter Sensitivity

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- Small variations of  $\omega_p$  are far more important than small change in  $Q_p$ .
- Since the errors increase with  $Q$ , low- $Q$  filters are easier to design with less accurate components than high- $Q$  filters.
- Sensitivities are strong functions of frequency, and the passband edges are very critical.

# High-Order Filter Sensitivity

A 6th-order Butterworth bandpass filter



- For cascade design,

$$H(s) = H_1(s)H_2(s) \cdots H_n(s)$$

$$S_{H_j(s)}^{H(s)} = 1 \quad \text{and} \quad S_x^{H(s)} = S_x^{H_j(s)}$$

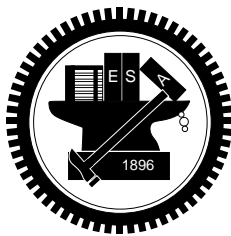
The sensitivity of  $H(s)$  to  $x$  is as large as sensitivity of sub-block  $H_j(s)$  to  $x$ .

- Feedback paths around low-order sections in a multiple-feedback (MF) filter topology can reduce sensitivities in the passband. In the stopbands, where feedback paths lose their effectiveness, MF and cascade sensitivities are approximately the same.

# Active-RC Filters

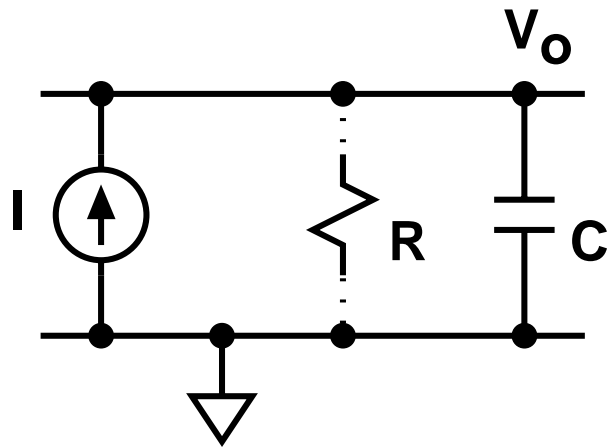
Jieh-Tsorng Wu

October 17, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Capacitor Integrators



$$\frac{V_o}{I} = \frac{1}{j\omega C + G} = \frac{1}{j\omega C \left[1 - j\frac{G}{\omega C}\right]} = \frac{1}{j\omega C \left[1 - j\frac{1}{Q_I(\omega)}\right]}$$

$$Q_I(\omega) = \frac{\omega C}{G}$$

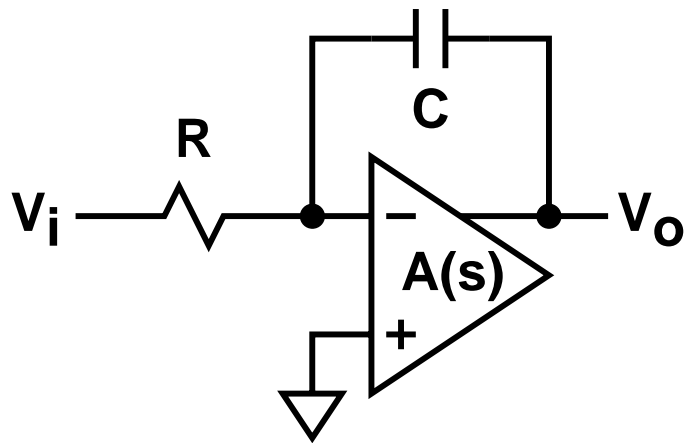
The transfer function of an integrator can be expressed as

$$H(j\omega) = \frac{1}{F(j\omega)} = \frac{1}{j\text{Im}[F(j\omega)] + \text{Re}[F(j\omega)]} = \frac{1}{j\omega\tau + q} = \frac{1}{j\omega\tau \left[1 - j\frac{1}{Q_I(\omega)}\right]}$$

$$Q_I(\omega) = \frac{\text{Im}[F(j\omega)]}{\text{Re}[F(j\omega)]} = \frac{\omega\tau}{q}$$

- $Q_I$  is the *quality factor* of the integrator.
- For an ideal integrator,  $Q_I \rightarrow \infty$  and  $q \rightarrow 0$ .

# Active-RC Inverting Integrators



$$\frac{V_o}{V_i}(s) = -\frac{1}{sRC} \cdot \frac{1}{1 + \frac{1}{A(s)} \left[1 + \frac{1}{sRC}\right]}$$

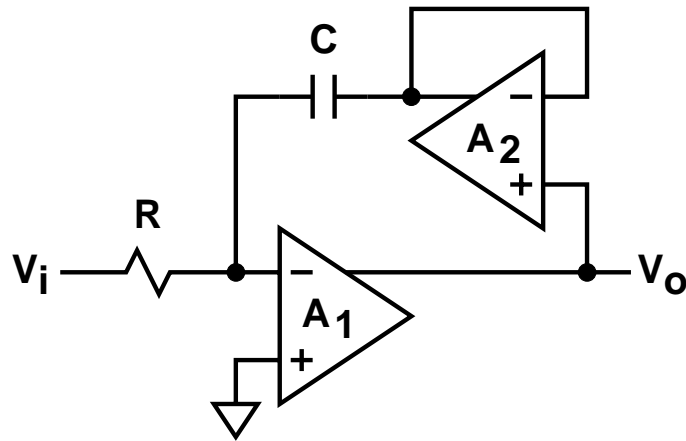
Let  $A(s) = \omega_u/s$ , then

$$\frac{V_o}{V_i}(s) = -\frac{1}{sRC} \cdot \frac{1}{1 + s/\omega_u + 1/(\omega_u RC)} \approx -\frac{1}{sRC} \cdot \frac{1}{1 + s/\omega_u} \quad \text{if } \omega_u \gg \frac{1}{RC}$$

$$\frac{V_o}{V_i}(j\omega) = -\frac{1}{j\omega RC - \omega^2 RC/\omega_u} = -\frac{1}{j\omega\tau + q}$$

$$\tau = RC \quad q = -\frac{\omega^2 RC}{\omega_u} = -\frac{\omega RC}{|A(j\omega)|} \quad Q_I = \frac{\omega\tau}{q} = -\frac{\omega_u}{\omega} = -|A(j\omega)|$$

# Actively Compensated Inverting Integrator



$$\frac{V_o}{V_i}(s) = -\frac{1}{\frac{sRC}{1+1/A_2(s)} + \frac{1+sRC}{A_1(s)}}$$

$$\approx -\frac{1}{sRC \left(1 - \frac{1}{A_2(s)} + \frac{1}{A_2^2(s)} - \frac{1}{A_2^3(s)} + \dots\right) + \frac{1+sRC}{A_1(s)}}$$

Let  $A_1(s) = \omega_{u1}/s$ , and  $A_2(s) = \omega_{u2}/s$ ,

$$\frac{V_o}{V_i}(j\omega) \approx -\frac{1}{j\omega RC \left(1 - \frac{j\omega}{\omega_{u2}} - \frac{\omega^2}{\omega_{u2}^2} + \frac{j\omega^3}{\omega_{u2}^3} + \dots\right) - \frac{\omega^2 RC - j\omega}{\omega_{u1}}}$$

$$\approx -\frac{1}{j\omega RC \left(1 + \frac{1}{\omega_{u1} RC} - \frac{\omega^2}{\omega_{u2}^2}\right) + \frac{\omega^2 RC}{\omega_{u2}} \left(1 - \frac{\omega^2}{\omega_{u2}^2} - \frac{\omega_{u2}}{\omega_{u1}}\right)}$$

# Actively Compensated Inverting Integrator

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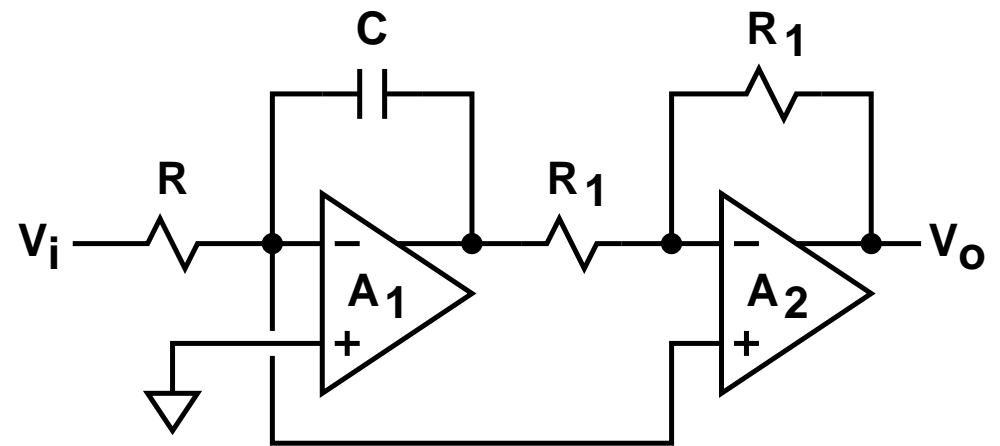
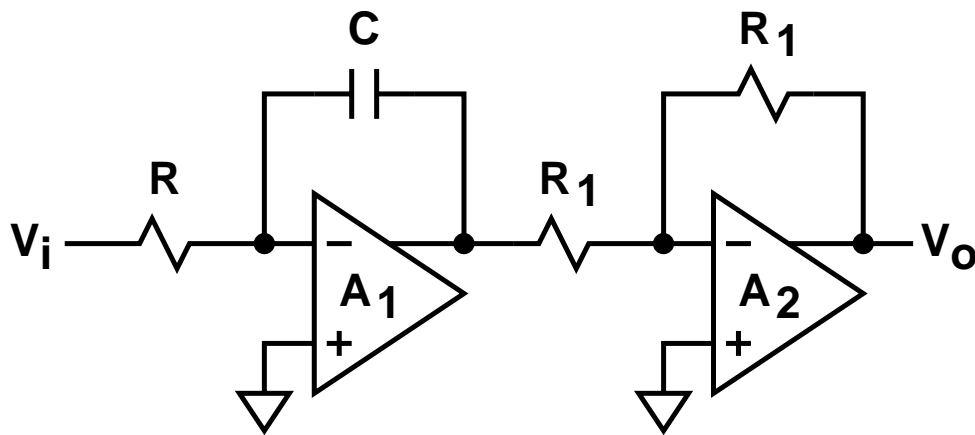
Thus

$$\tau \approx RC \quad q = \frac{\omega^2 RC}{\omega_{u2}} \left( 1 - \frac{\omega^2}{\omega_{u2}^2} - \frac{\omega_{u2}}{\omega_{u1}} \right) \approx \frac{\omega RC}{|A_2(j\omega)|} \left( 1 - \frac{\omega_{u2}}{\omega_{u1}} \right)$$
$$\Rightarrow Q_I = \frac{\omega\tau}{q} = \frac{|A_2(j\omega)|}{1 - \frac{\omega_{u2}}{\omega_{u1}}}$$

If  $A_1(s) = A_2(s) = A(s) = \omega_u/s$ , then

$$\tau \approx RC \quad q = -\frac{\omega^4 RC}{\omega_u^3} = -\frac{\omega RC}{|A(j\omega)|^3}$$
$$\Rightarrow Q_I = -\left(\frac{\omega}{\omega_u}\right)^3 = -|A(j\omega)|^3$$

# Noninverting Integrator



Let  $A_1 = A_2 = A$

$$\frac{V_o}{V_i} = \frac{1}{sRC} \cdot \frac{1}{1 + \frac{3}{A} + \frac{1}{sRCA} + \frac{2}{A^2} + \frac{2}{sRCA^2}}$$

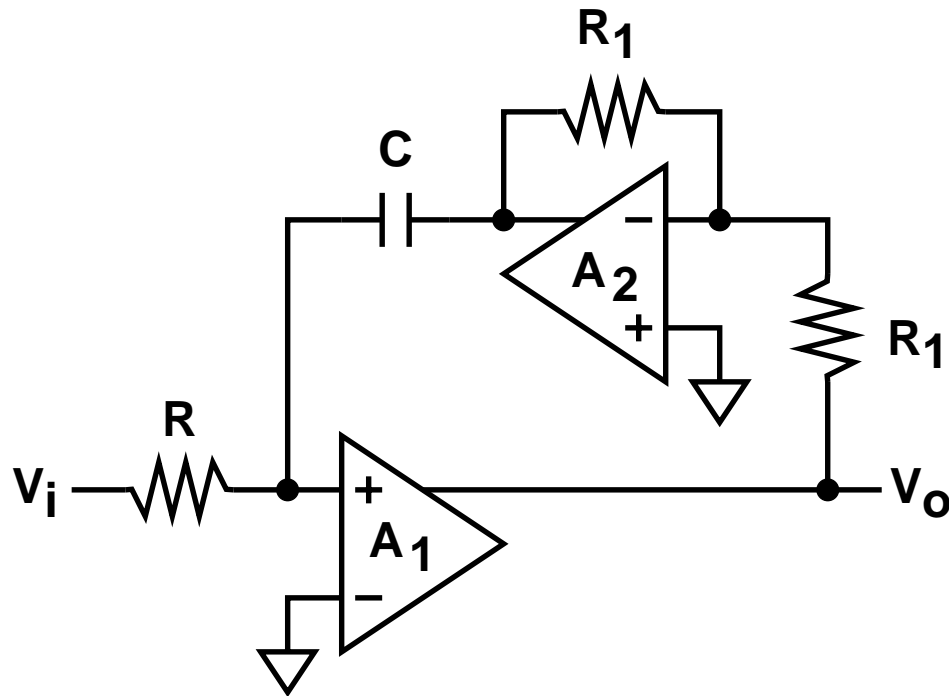
$$Q_I = -\frac{1}{3}|A(j\omega)|$$

Let  $A_1 = A_2 = A$

$$\frac{V_o}{V_i} = \frac{1}{sRC} \cdot \frac{1}{1 + \frac{1}{A} + \frac{1}{sRCA}}$$

$$Q_I = -|A(j\omega)|$$

# Phase-Lead Noninverting Integrator



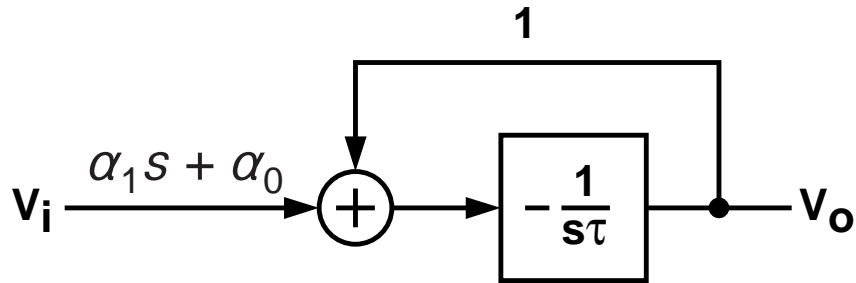
$$\frac{V_o}{V_i}(s) = \frac{1}{sRC \left[ \frac{1}{1+2/A_2(s)} + \frac{1}{A_1(s)} + \frac{1}{sR_1CA_1(s)} \right]}$$

If  $A_1(s) = A_2(s) = A(s) = \omega_u/s$ , then

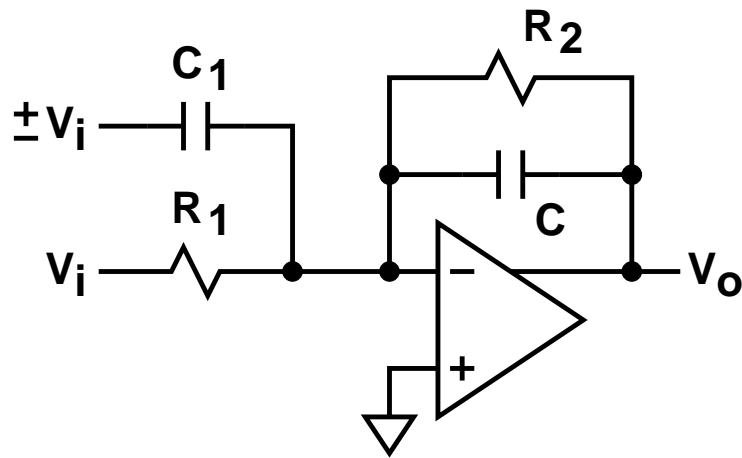
$$Q_I \approx +\frac{\omega_u}{\omega} = +|A(j\omega)|$$

# First-Order Filters

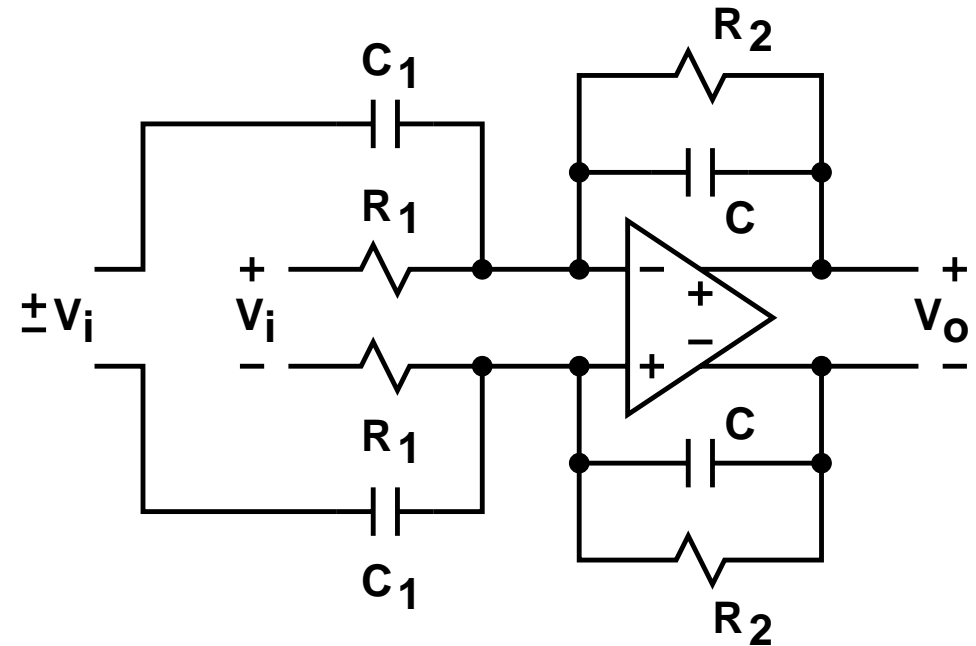
## State-Variable Topology



## Active-RC Filter

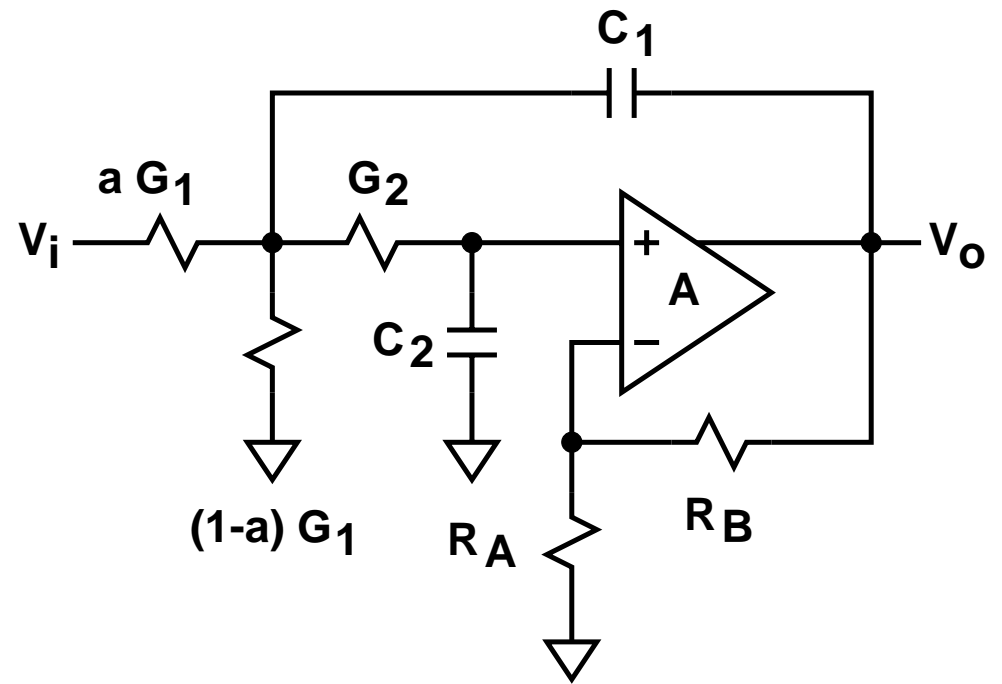
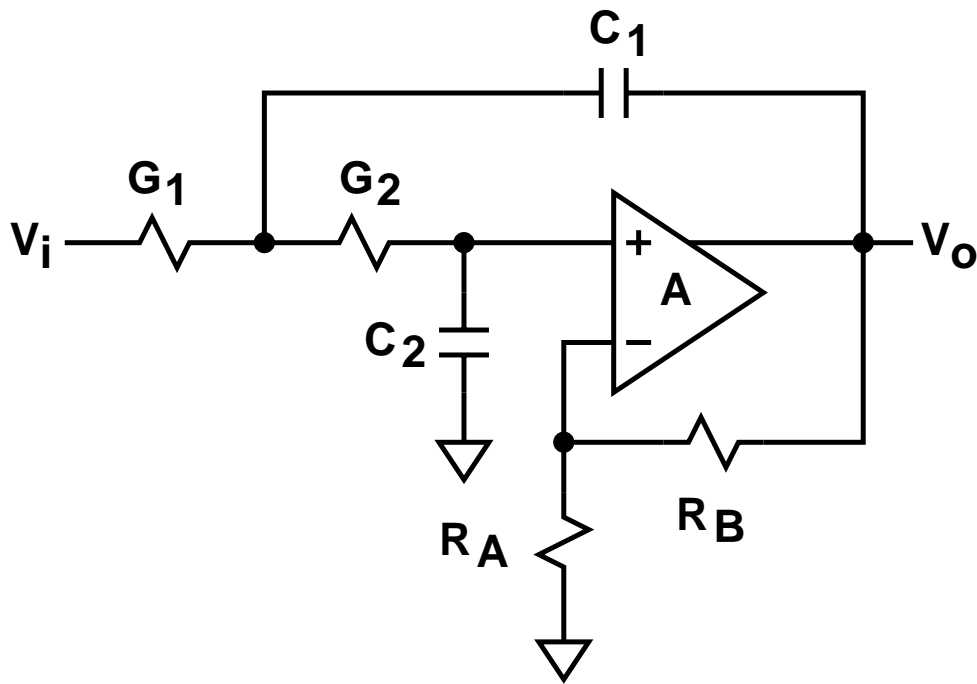


## Fully-Differential Active-RC Filter



$$\frac{V_o}{V_i} = -\frac{\alpha_1 s + \alpha_0}{s\tau + 1} = -\frac{\pm sC_1 + G_1}{sC + G_2} = -\frac{R_2}{R_1} \cdot \frac{\pm sR_1C_1 + 1}{sR_2C + 1}$$

# Single-Amplifier 2nd-Order Filters — Sallen-Key LP Biquad



$$H(s) = \frac{V_o}{V_i} = \frac{KG_1G_2 \frac{1}{1+K/A}}{s^2C_1C_2 + s \left[ C_2(G_1 + G_2) + C_1C_2 \left( 1 - K \frac{1}{1+K/A} \right) \right] + G_1G_2}$$

$$K = a \cdot \left( 1 + \frac{R_B}{R_A} \right) \quad a \leq 1$$

# Single-Amplifier 2nd-Order Filters —Sallen-Key LP Biquad

---

Let  $A = \infty$  and  $C_1 = C_2 = C$ , then

$$H(s) = \frac{KG_1G_2/C^2}{s^2 + s[G_1 + G_2(2 - k)]/C + G_1G_2/C^2} = K \cdot \frac{\omega_p^2}{s^2 + s\omega_p/Q + \omega_p^2}$$
$$\omega_p^2 = \frac{G_1G_2}{C^2} \quad Q = \frac{\sqrt{G_1G_2}}{G_1 + G_2(2 - K)} \quad K = a \cdot \left(1 + \frac{R_B}{R_A}\right)$$

If  $a = 1$ ,  $R_1 = R_2 = R$ , we have

$$\omega_p = \frac{1}{RC} \quad Q = \frac{1}{3 - K} \quad S_K^Q = 3Q - 1$$

- Minimal use of opamp, at the expense of more passive components.
- Sensitive to parasitic capacitors.
- Widely used to realize the on-chip anti-aliasing and reconstruction filters.

# Single-Amplifier 2nd-Order Filters —Sallen-Key LP Biquad

---

Let  $a = 1$ ,  $R_1 = R_2 = R$ ,  $C_1 = C_2 = C$ ,  $A = \omega_u/s$ ,

$$H'(s) = K \cdot \frac{\omega_p^2 \frac{1}{1+K/A}}{s^2 + s\omega_p \left(3 - K \frac{1}{1+K/A}\right) + \omega_p^2} \approx K \cdot \frac{\omega_p^2(1 - K/A)}{s^2 + s\omega_p [3 - K(1 - K/A)] + \omega_p^2}$$

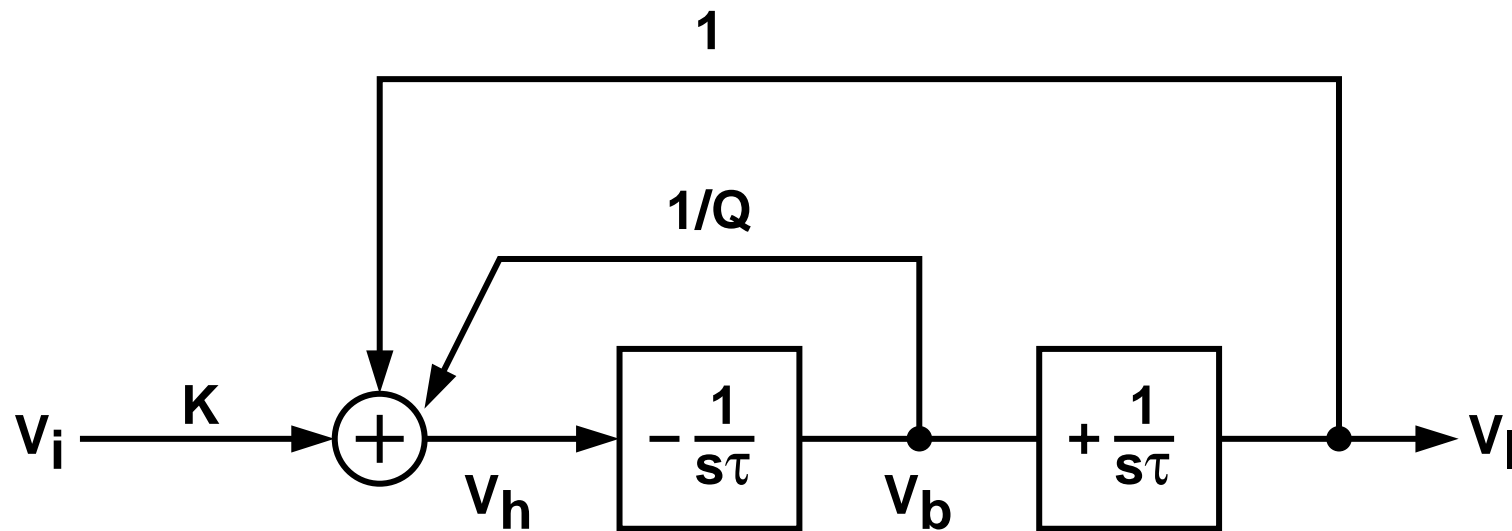
$$\Rightarrow H'(s) \approx K \cdot \frac{\omega_p^2(1 - sK/\omega_u)}{s^2(1 + \epsilon) + s\omega_p(3 - K) + \omega_p^2} = K \cdot \frac{\omega_p'^2(1 - K/\omega_u)}{s^2 + s\omega_p'/Q' + \omega_p'^2}$$

$$\omega_p' = \frac{\omega_p}{\sqrt{1 + \epsilon}} \approx \omega_p \left(1 - \frac{\epsilon}{2}\right) = \omega_p - \Delta\omega_p \quad Q' = Q\sqrt{1 + \epsilon} \approx Q \left(1 + \frac{\epsilon}{2}\right) = Q + \Delta Q$$

$$\epsilon = \frac{\omega_p}{\omega_u} K^2 = \frac{K^2}{|A(j\omega_p)|}$$

- $H'(s)$  has an additional positive zero at  $\omega_u/K$ .
- The Sallen-Key biquad is a good low- $Q$  LP filter with small  $\omega_u$ -caused deviations.

# State-Variable Second-Order Filters



$$\frac{V_h}{V_i} = +K \cdot \frac{s^2}{s^2 + s/(Q\tau) + 1/\tau^2} = K \cdot \frac{s^2}{s^2 + s\omega_p/Q + \omega_p^2}$$

$$\frac{V_b}{V_i} = -K \cdot \frac{s/\tau}{s^2 + s/(Q\tau) + 1/\tau^2} = -K \cdot \frac{s\omega_p}{s^2 + s\omega_p/Q + \omega_p^2}$$

$$\omega_p = \frac{1}{\sqrt{\tau_1\tau_2}} = \frac{1}{\tau}$$

$$\frac{V_o}{V_i} = -K \cdot \frac{1/\tau^2}{s^2 + s/(Q\tau) + 1/\tau^2} = -K \cdot \frac{\omega_p^2}{s^2 + s\omega_p/Q + \omega_p^2}$$

# State-Variable Second-Order Filters

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For integrators with finite quality factors, let

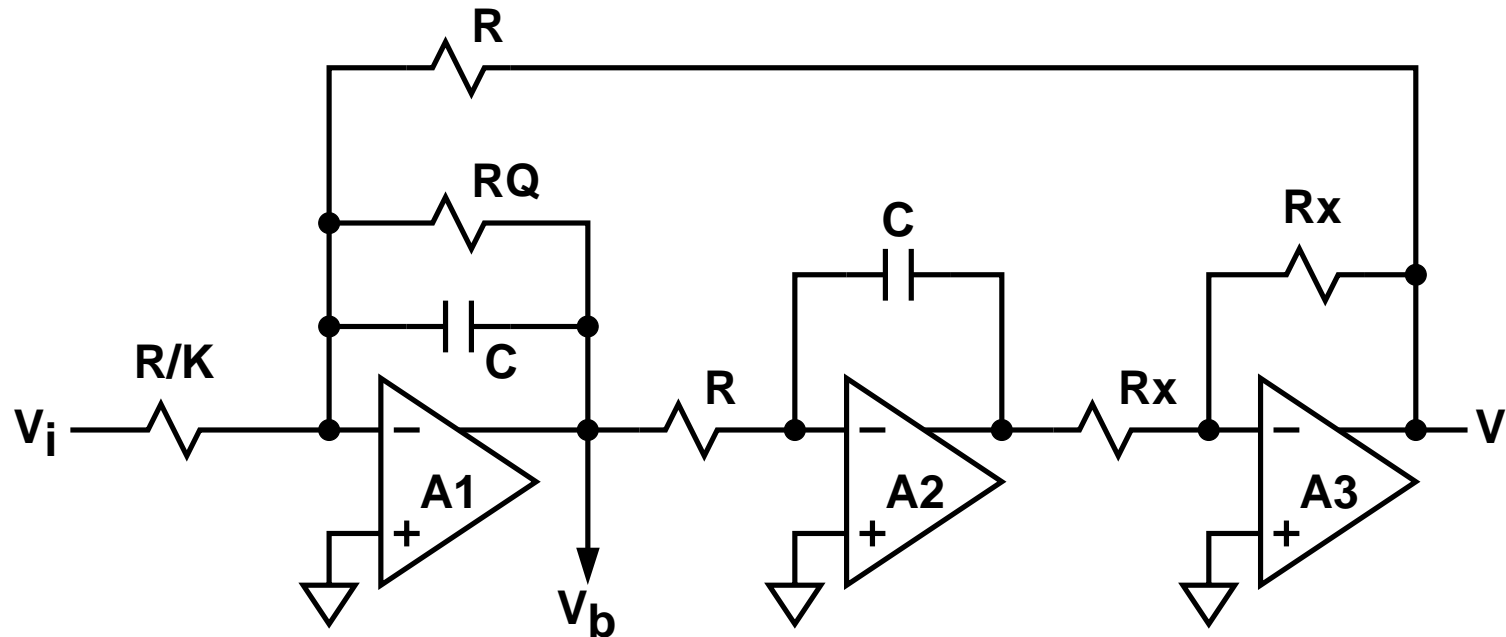
$$-\frac{1}{s\tau} \rightarrow -\frac{1}{\tau(s\alpha_1 + \sigma_1)} \quad + \frac{1}{s\tau} \rightarrow +\frac{1}{\tau(s\alpha_2 + \sigma_2)}$$

The new  $\omega_p$  and  $Q$  are

$$\omega_p'^2 = \frac{\omega_p^2}{\alpha_1\alpha_2} \left( 1 + \frac{1}{Q} \cdot \frac{\sigma_2}{\omega_p} + \frac{\sigma_1\sigma_2}{\omega_p^2} \right)$$

$$Q' = \frac{\omega_p'}{\omega_p} \cdot \frac{Q}{\alpha_2 + Q \cdot \frac{\alpha_2\sigma_1 + \alpha_1\sigma_2}{\omega_p}}$$

# Tow-Thomas (TT) Biquad



$$\frac{V_b}{V_i} = -K \cdot \frac{\omega_p s}{s^2 + s\omega_p/Q + \omega_p^2} \quad \frac{V_1}{V_i} = -K \cdot \frac{\omega_p^2}{s^2 + s\omega_p/Q + \omega_p^2} \quad \omega = \frac{1}{RC}$$

The sensitivities for any passive component  $x$  are

$$S_x^{\omega_p} = -1/2 \quad |S_x^Q| \leq 1$$

## Tow-Thomas (TT) Biquad

---

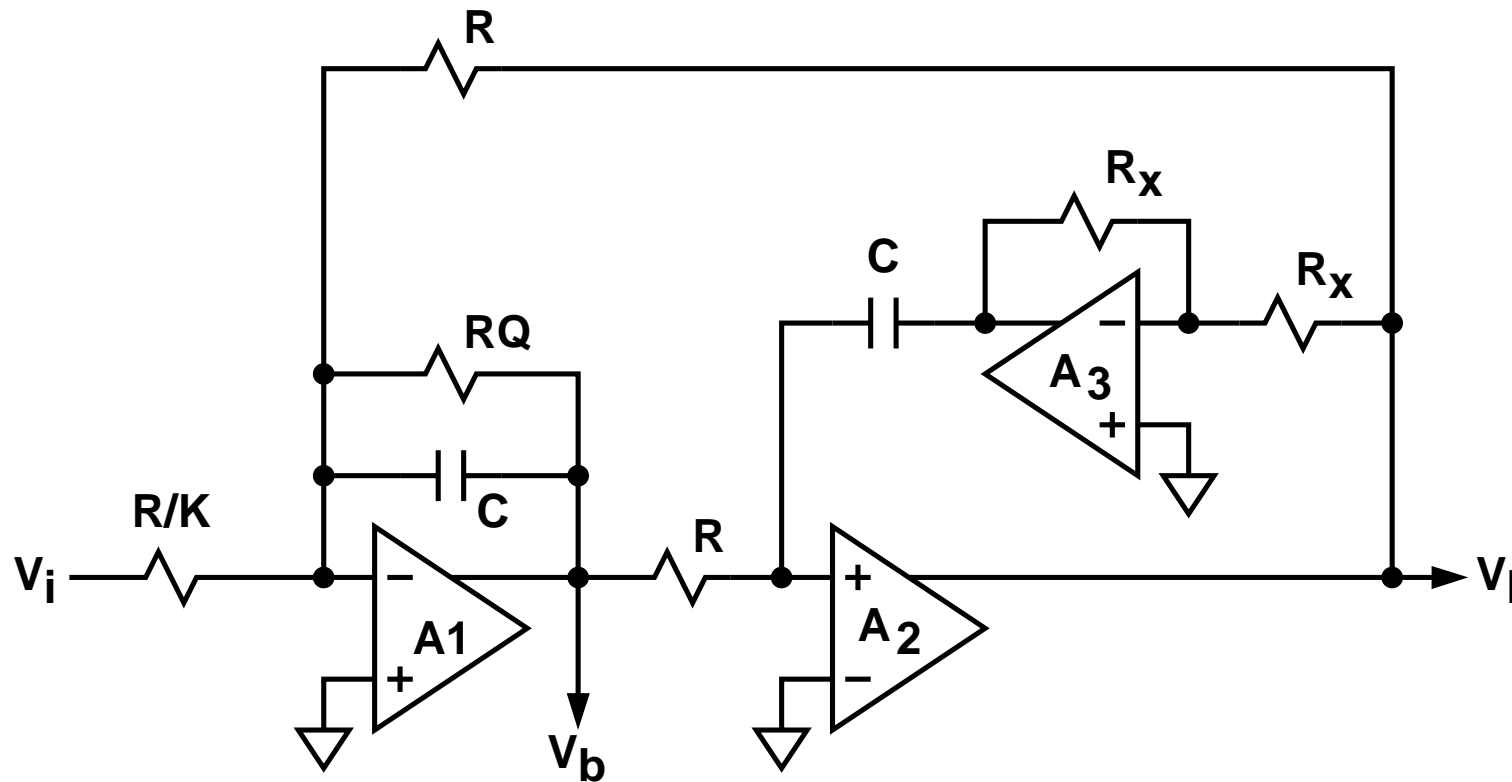
Let  $A_1 = \omega_{u1}/s$ ,  $A_2 = \omega_{u2}/s$ , and  $A_3 = \omega_{u3}/s$ , then

$$\begin{aligned}
 -\frac{1}{s\tau} &\rightarrow -\frac{1}{\tau(s\alpha_1 + \sigma_1)} & \alpha_1 &= 1 + \frac{\omega_p}{\omega_{u1}} \left(1 + K + \frac{1}{Q}\right) & \sigma_1 &= -\frac{\omega^2}{\omega_{u1}} \\
 +\frac{1}{s\tau} &\rightarrow +\frac{1}{\tau(s\alpha_2 + \sigma_2)} & \alpha_2 &= 1 + \frac{\omega_p}{\omega_{u2}} & \sigma_2 &= -\frac{\omega^2}{\omega_{u2}} - 2\frac{\omega^2}{\omega_{u3}}
 \end{aligned}$$

Assuming matched opamps and  $\omega_p \ll \omega_u$ , we have

$$\begin{aligned}
 \frac{\omega'_p - \omega_p}{\omega_p} &= \frac{\Delta\omega_p}{\omega_p} \approx -\frac{2+K}{2} \cdot \frac{\omega_p}{\omega_u} = -\frac{2+K}{2} \cdot \frac{1}{|A(j\omega_p)|} \\
 \frac{Q'}{Q} &\approx \frac{1}{1 - 4Q \cdot \frac{\omega_p}{\omega_u}} \quad \leftarrow \text{Q Enhancement}
 \end{aligned}$$

# Ackerberg-Mossberg (AM) Biquad



Let  $A_1 = \omega_{u1}/s$ ,  $A_2 = \omega_{u2}/s$ , and  $A_3 = \omega_{u3}/s$ , then

$$-\frac{1}{s\tau} \rightarrow -\frac{1}{\tau(s\alpha_1 + \sigma_1)} \quad +\frac{1}{s\tau} \rightarrow +\frac{1}{\tau(s\alpha_2 + \sigma_2)}$$

# Ackerberg-Mossberg (AM) Biquad

---

where

$$\alpha_1 = 1 + \frac{\omega_p}{\omega_{u1}} \left( 1 + K + \frac{1}{Q} \right) \quad \sigma_1 = -\frac{\omega^2}{\omega_{u1}} \quad \alpha_2 = 1 + \frac{\omega_p}{\omega_{u2}} \quad \sigma_2 = + \left( \frac{2\omega^2}{\omega_{u3}} - \frac{\omega^2}{\omega_{u2}} \right)$$

If  $Q \gg 1$ , we have

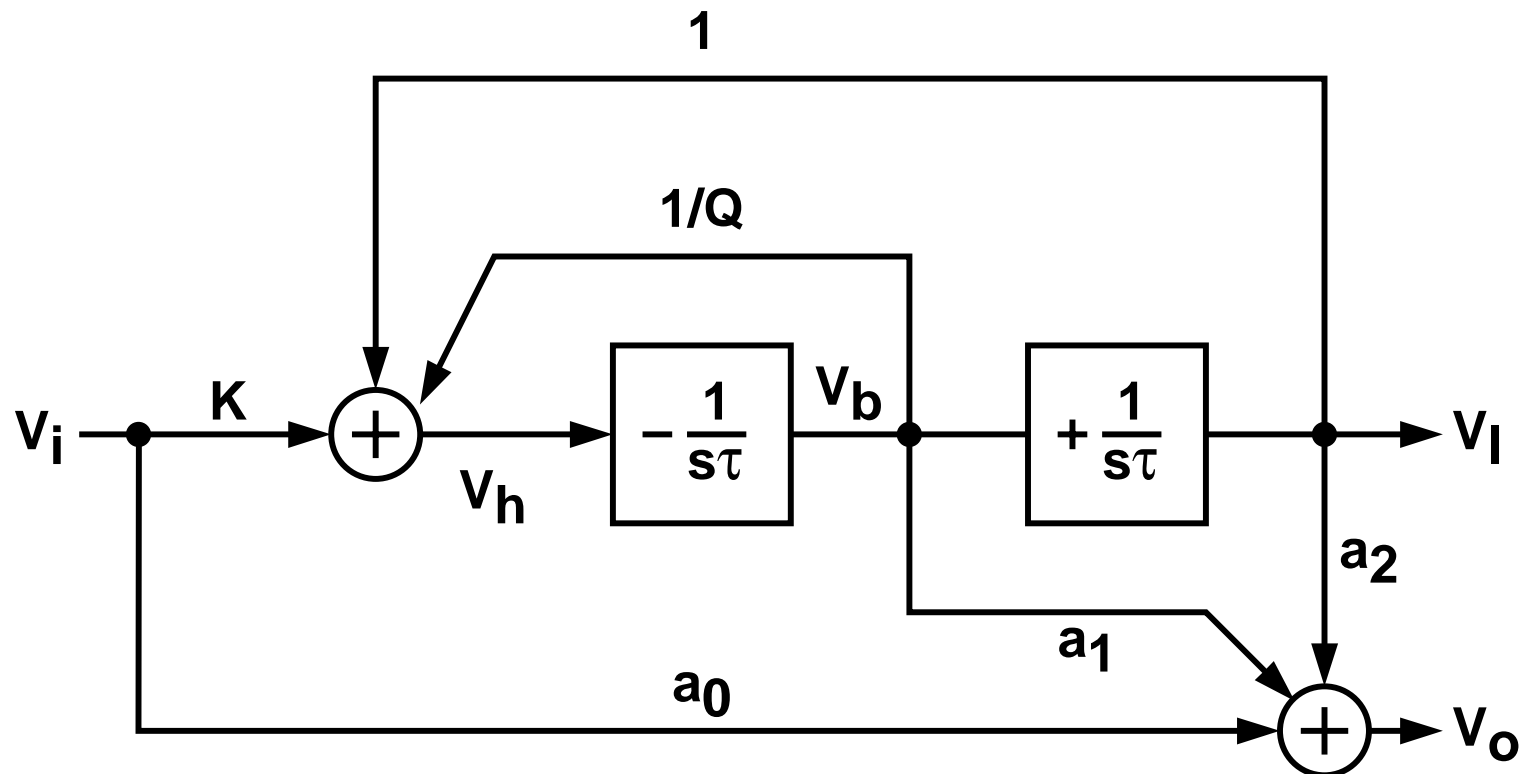
$$\frac{\omega'_p - \omega_p}{\omega_p} = \frac{\Delta\omega_p}{\omega_p} \approx -\frac{1}{2} \left[ (1 + K) \frac{\omega_p}{\omega_{u1}} + \frac{\omega_p}{\omega_{u2}} \right] \quad \frac{Q'}{Q} \approx \frac{1 + \Delta\omega_p/\omega_p}{1 + \frac{\omega_p}{\omega_{u2}} + Q \cdot D}$$

$$D = \frac{2\omega_p}{\omega_{u3}} - \frac{\omega_p}{\omega_{u1}} - \frac{\omega_p}{\omega_{u2}} - \frac{\omega_p^2}{\omega_{u1}\omega_{u2}} + \frac{\omega_p^2(1 + K)}{\omega_{u1}} \left( \frac{2}{\omega_{u3}} - \frac{1}{\omega_{u2}} \right)$$

For matched opamps, we have

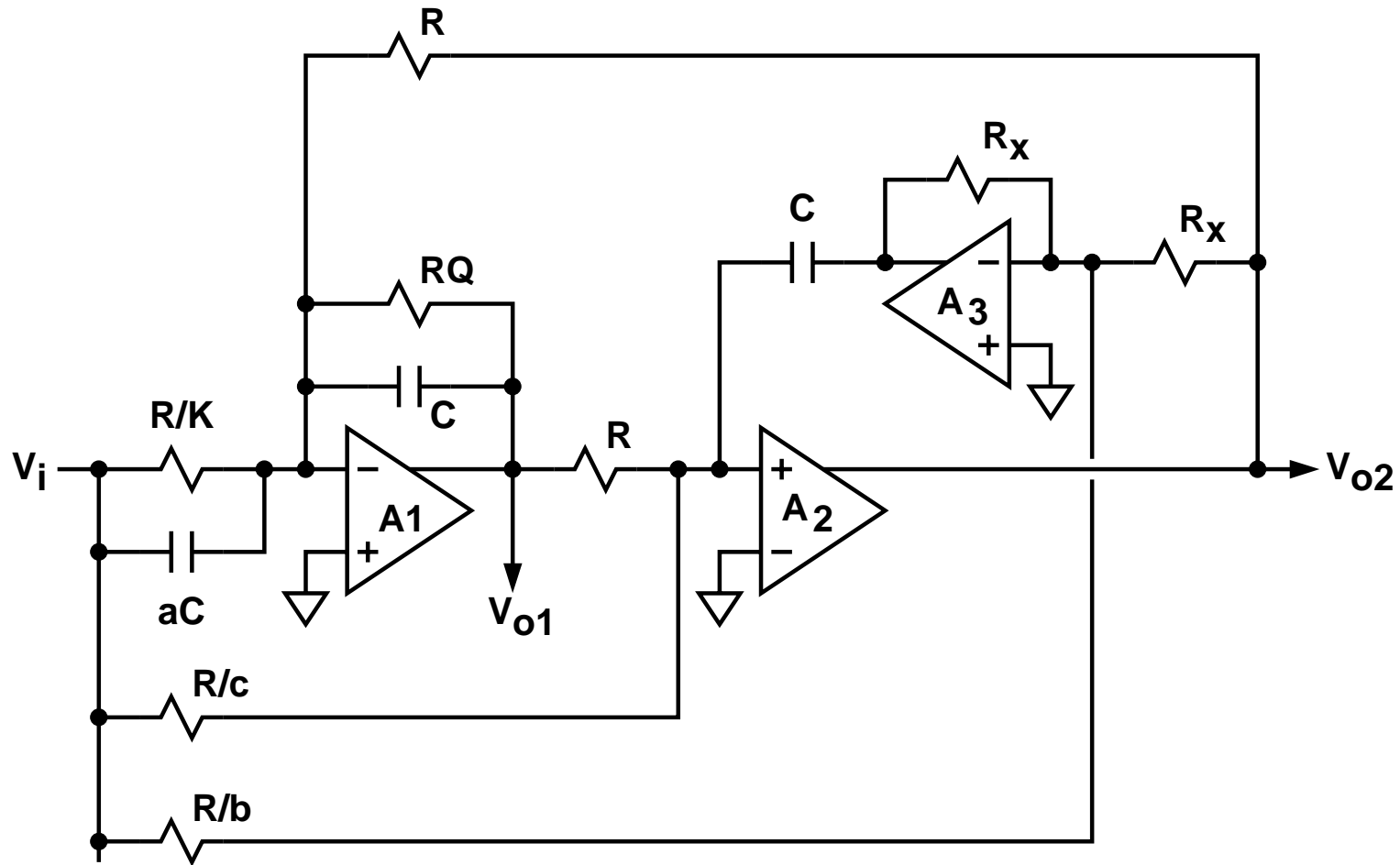
$$\frac{Q'}{Q} \approx \frac{1 - \left(1 + \frac{K}{2}\right) \frac{\omega_p}{\omega_u}}{1 + \frac{\omega_p}{\omega_u} + QK \left(\frac{\omega_p}{\omega_u}\right)^2}$$

# Arbitrary Transmission Zeros by Summing



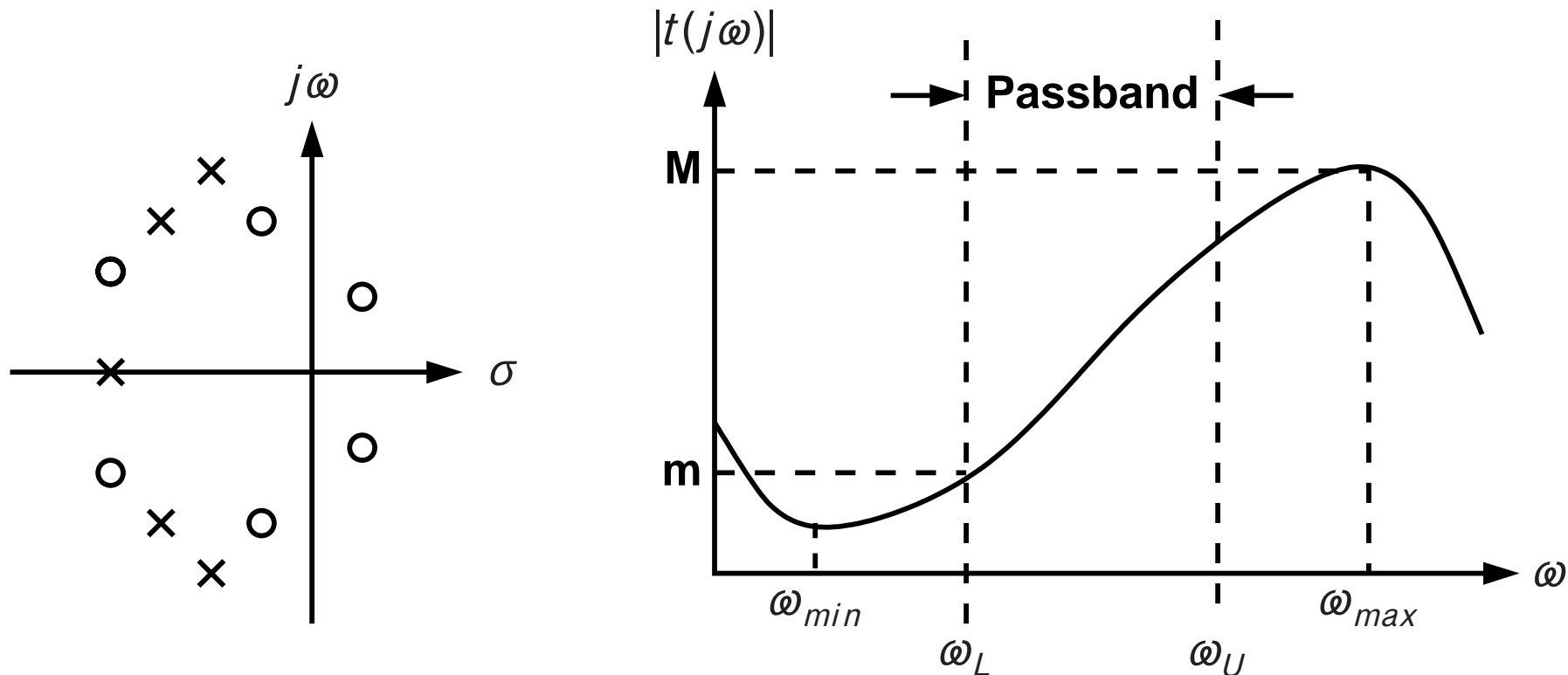
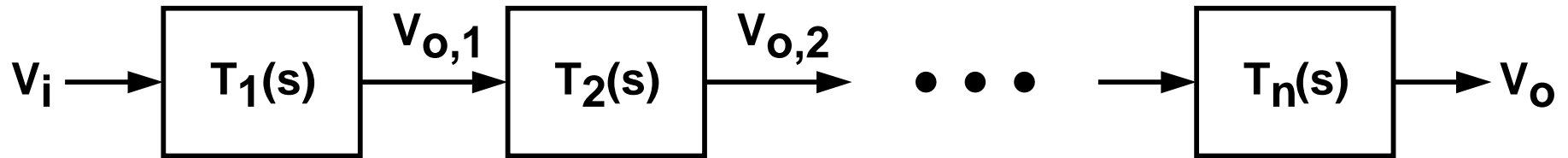
$$\frac{V_o}{V_i} = a_0 + \frac{-a_1 \cdot K s \omega_p - a_2 \cdot K \omega_p^2}{s^2 + s \omega_p / Q + \omega_p^2} = \frac{a_0 s^2 + s(\omega_p / Q)[a_0 - a_1(KQ)] + \omega_p^2[a_0 - a_2 K]}{s^2 + s \omega_p / Q + \omega_p^2}$$

# Arbitrary Transmission Zeros by Voltage Feedforward



$$\frac{V_{o1}}{V_i} = -\frac{as^2 + s\omega_p(K - b) + c\omega_p^2}{s^2 + s\omega_p/Q + \omega_p^2}$$

# High-Order Filter Using Cascade Topology



# High-Order Filter Using Cascade Topology

---

- Each stage is a biquad, i.e.,

$$T_i(s) = k_i \cdot \frac{a_{2,i}s^2 + a_{1,i}s + a_{0,i}}{s^2 + s\omega_{p,i}/Q_{p,i} + \omega_{p,i}^2} = k_i \cdot t_i(s) \quad |t_i(j\omega_{p,i})| = 1$$

$k_i$  is defined as gain constant, such that  $|t_i(j\omega_{p,i})| = 1$ .

- No interaction between stages, therefore

$$H(s) = \frac{V_o(s)}{V_i(s)} = T_1(s) \cdot T_2(s) \cdot T_3(s) \cdots = \prod_{i=1}^n T_i(s) = \prod_{i=1}^n k_i t_i(s)$$

- Easy to tune.
- Sensitive to component variation in the passband for high-order filter, e.g., order > 8.

# High-Order Filter Using Cascade Topology

---

To maximize dynamic range want

$$\max|V_{o,i}| < V_{o,max} \quad 0 \leq \omega < \infty \quad \text{and} \quad \min|V_{o,i}| \rightarrow \max \quad \omega_L \leq \omega \leq \omega_U$$

$$V_{o,i}(s) = V_i(s) \cdot \prod_{j=1}^i T_j(s) = V_i(s) \cdot H_i(s) \quad H_i(s) = \prod_{j=1}^i T_j(s) \quad i = 1, \dots, n$$

- $V_{o,max}$  is the maximum undistorted signal level, which is limited by power supply or by the slew rate of the opamps.
- Large signal even outside the passband must not overload the opamps.
- Signal-to-noise ratio is of no interest in the stopband.

# Cascaded Filter Design Procedures

---

1. *Pole-Zero Pairing*. Every  $|t_i(j\omega)|$  should be as flat as possible in the  $\omega$  of interest, i.e.,

$$\max \left\{ \log \frac{M(t_i)}{m(t_i)} \right\} \leftarrow \text{Minimize} \quad i = 1, \dots, n$$

- A good suboptimal solution is assigning each zero or zero pair to the closest pole.

2. *Section Ordering*. Every  $|V_{o,i}(j\omega)|$  or  $|H_i(j\omega)|$  should be as flat as possible in the  $\omega$  of interest, i.e.,

$$\max \left\{ \log \frac{M(H_i)}{m(H_i)} \right\} \leftarrow \text{Minimize} \quad i = 1, \dots, n$$

- The section sequence in the order of increasing  $Q_p$  is often close to the optimum.
- It is often desirable to have a low-pass or bandpass biquad as the first section to minimize slew-rate problem.
- If possible, employ a high-pass or band-pass biquad as the last section to eliminate low-frequency noise and dc offset.

# Cascaded Filter Design Procedures

---

3. *Gain Assignment.* Every  $V_{o,j}$  should be as large as possible, i.e.,

$$M(V_{o,1}) = M(V_{o,2}) = \cdots = M(V_o)$$

Since

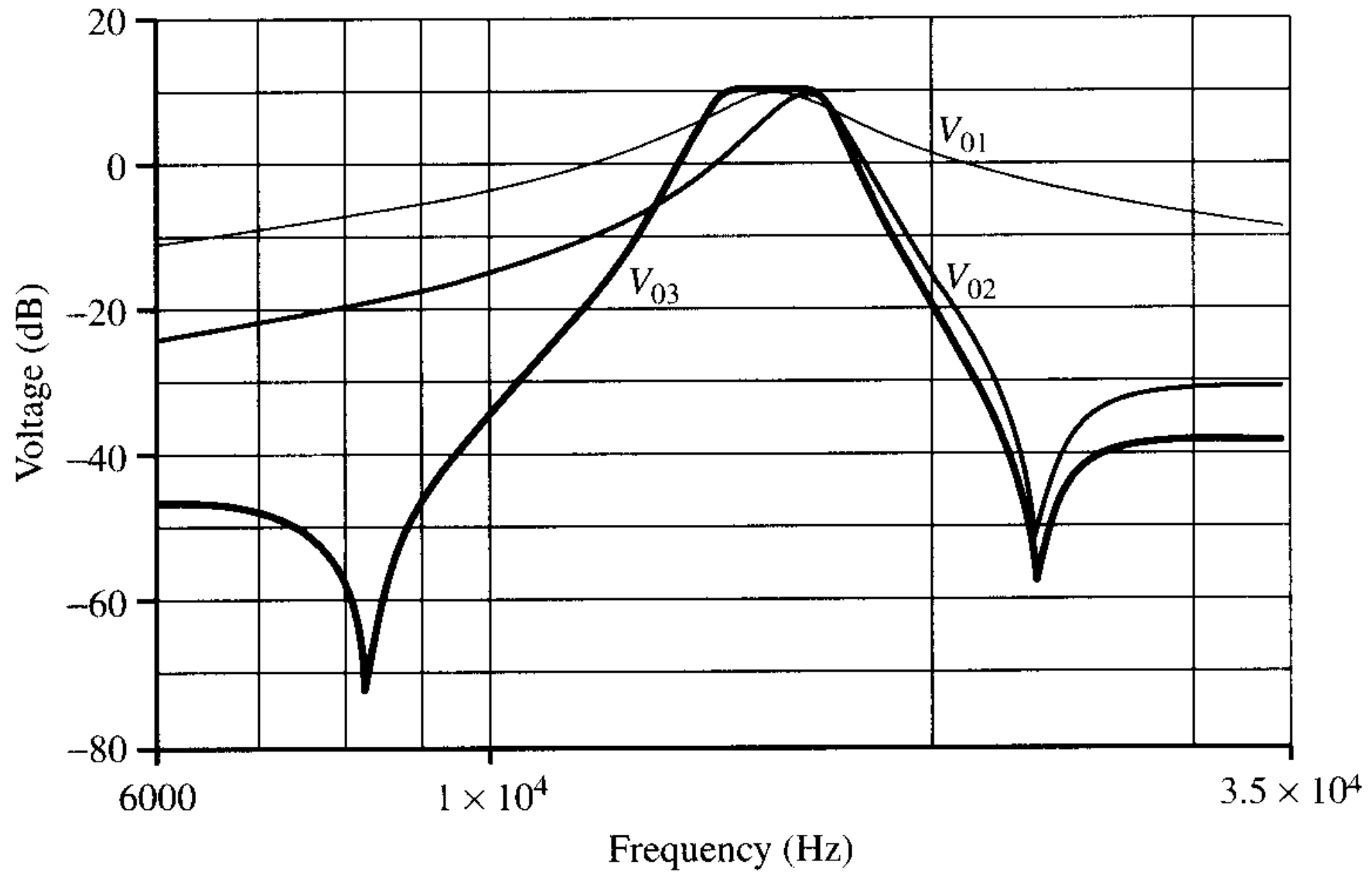
$$H_i(s) = \prod_{j=1}^i k_j t_j(s) = \prod_{j=1}^i k_j \prod_{j=1}^i t_j(s) \quad K_i = \prod_{j=1}^i k_j \quad M_i = \max \left| \prod_{j=1}^i t_j(j\omega) \right|$$

Filter Specification  $\rightarrow H(s) = H_n(s) \rightarrow K = K_n \quad M = M_n$

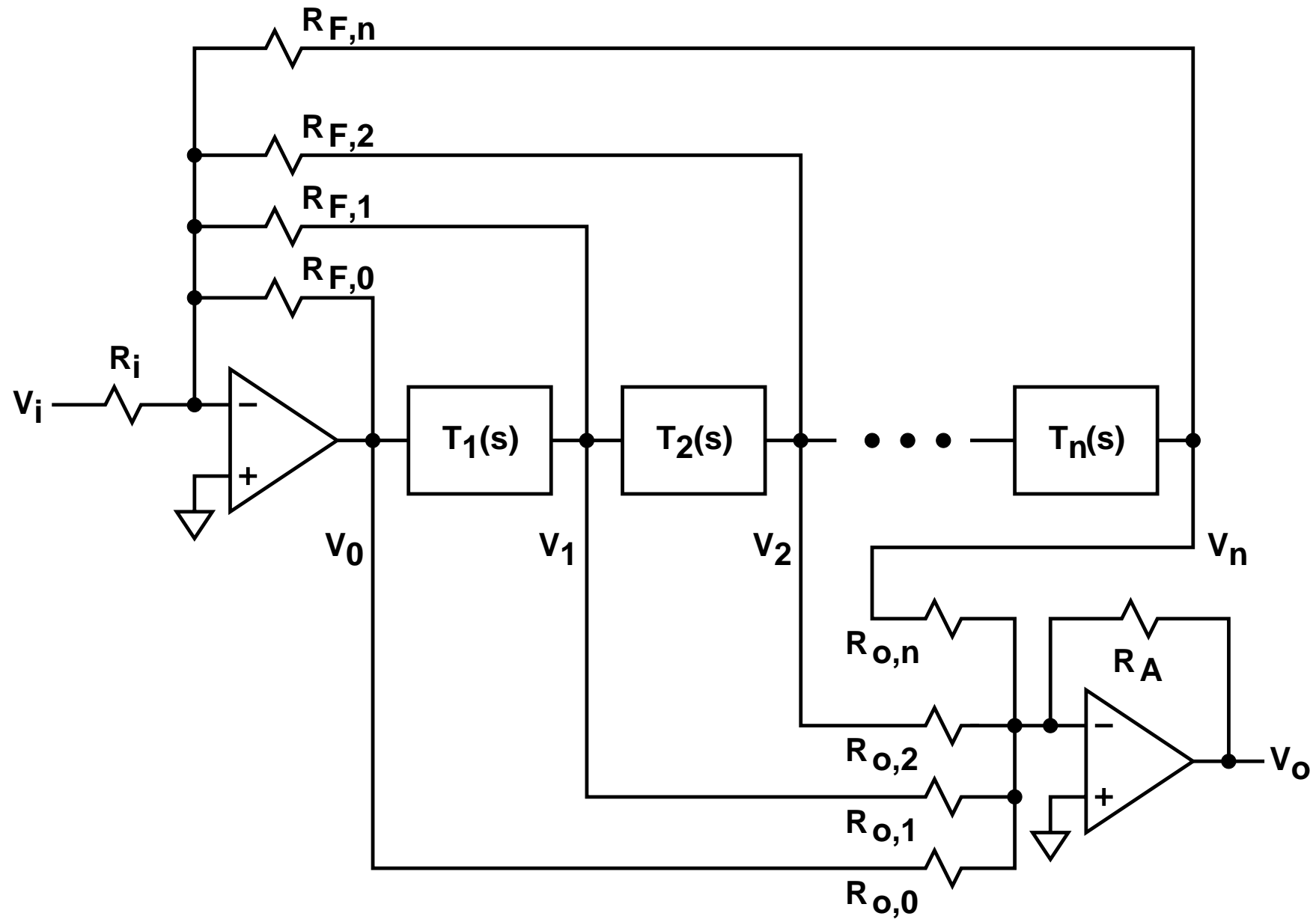
We have

$$K_i \cdot M_i = K_n \cdot M_n = K \cdot M \quad i = 1, \dots, n-1$$
$$\Rightarrow k_1 = K \cdot \frac{M}{M_1} \quad \text{and} \quad k_i = \frac{M_{i-1}}{M_i} \quad i = 2, \dots, n-1$$

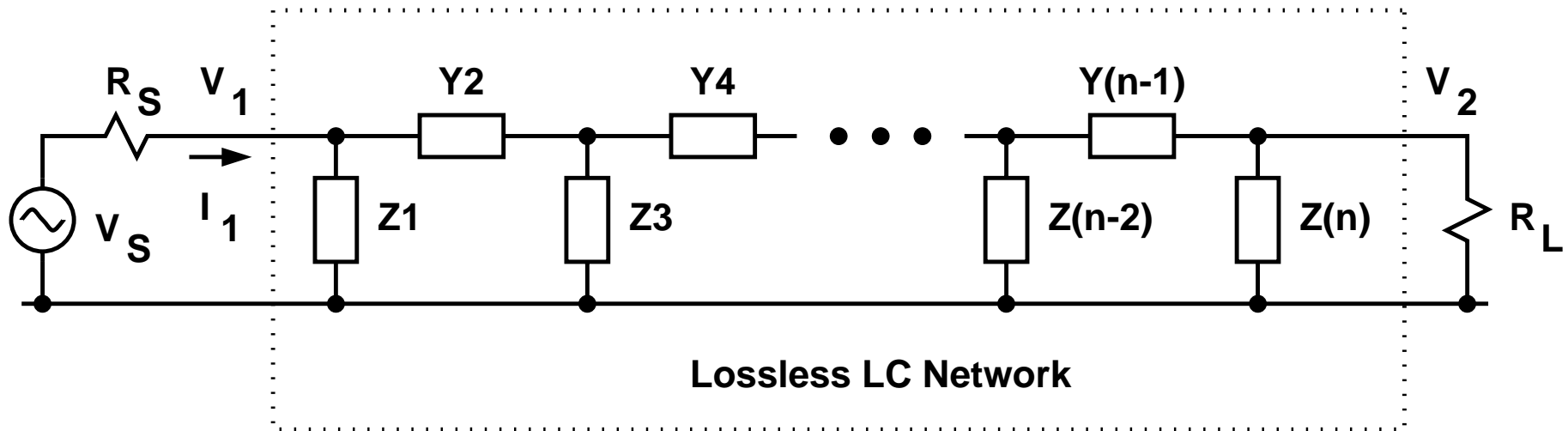
# Cascaded Filter Design Procedures



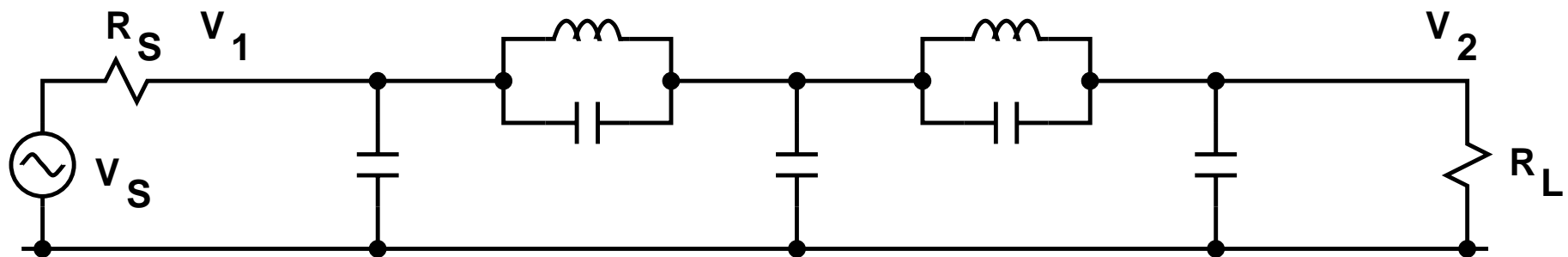
# High-Order Filter Using the Follow-the-Leader Feedback Topology



# High-Order Filter LC Ladder Simulation



A Fifth-Order Elliptic Low-Pass Filter

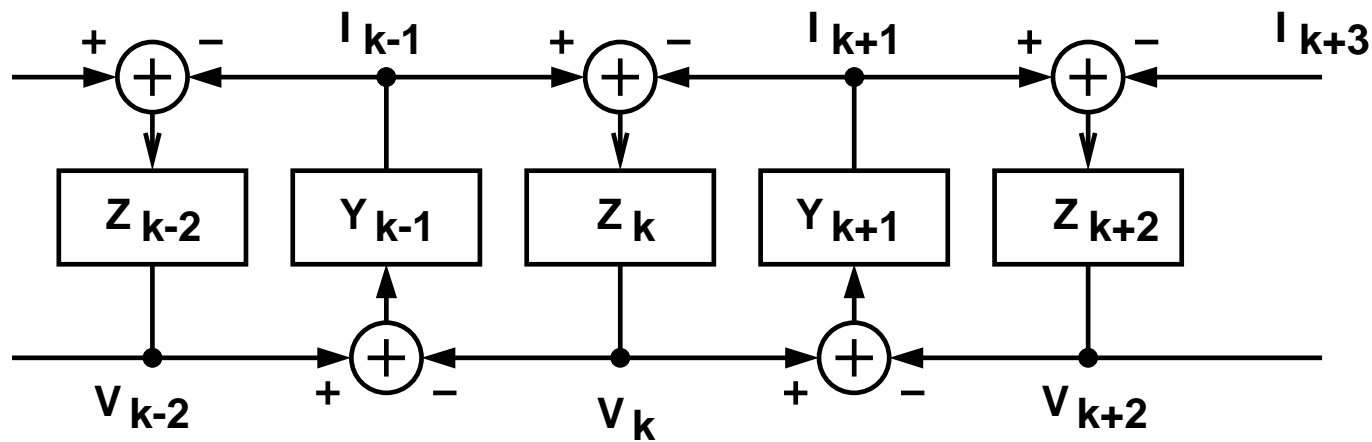
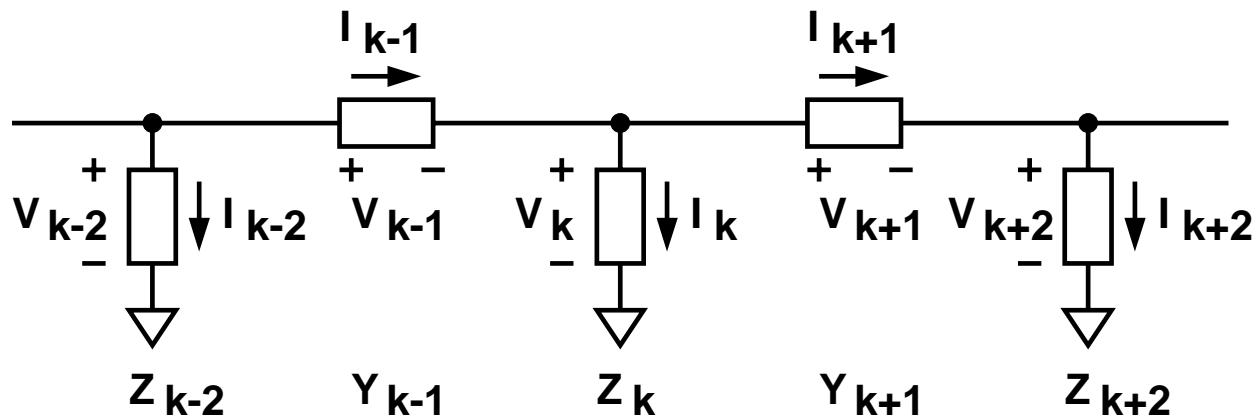
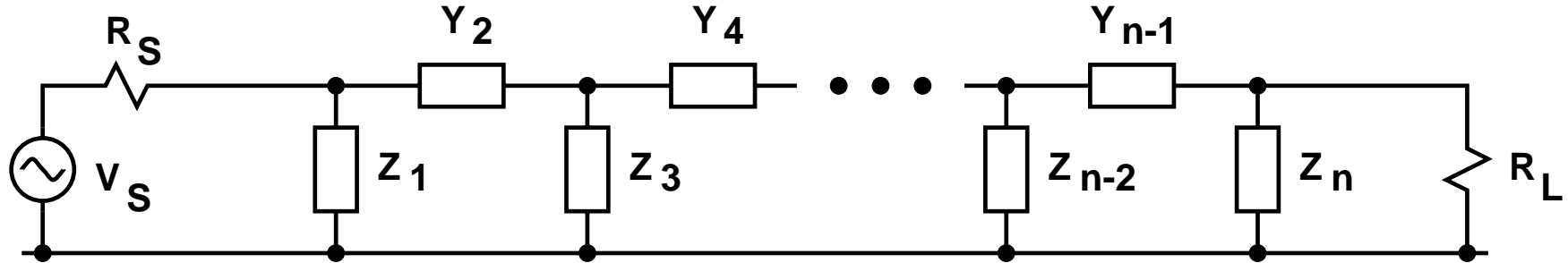


# High-Order Filter LC Ladder Simulation

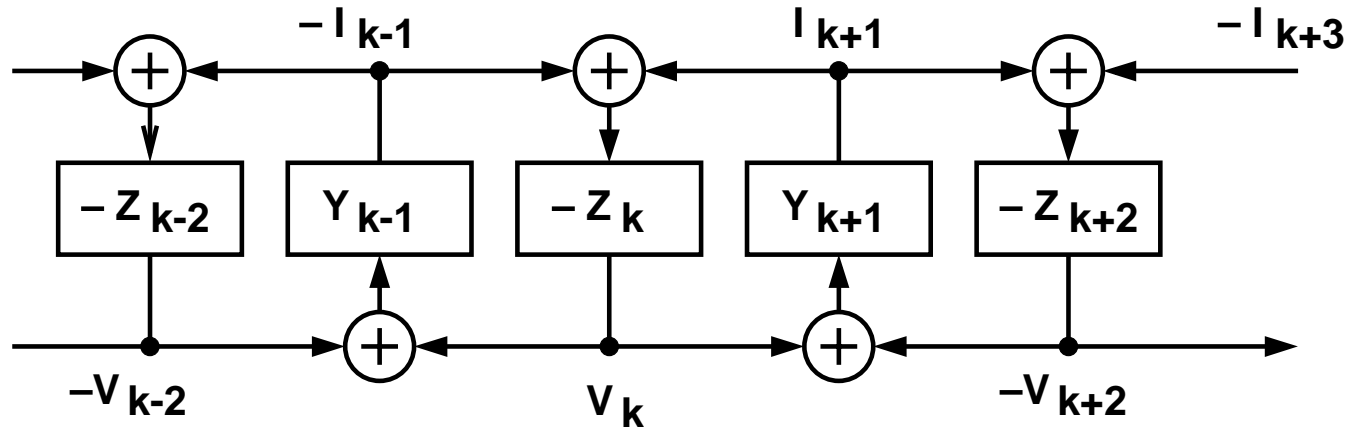
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- Minimum passband sensitivity to component tolerances.
- Can be implemented with
  - Element substitution.
  - Operational simulation with signal-flow graph.
- Requires more opamps than the cascade and MF methods.

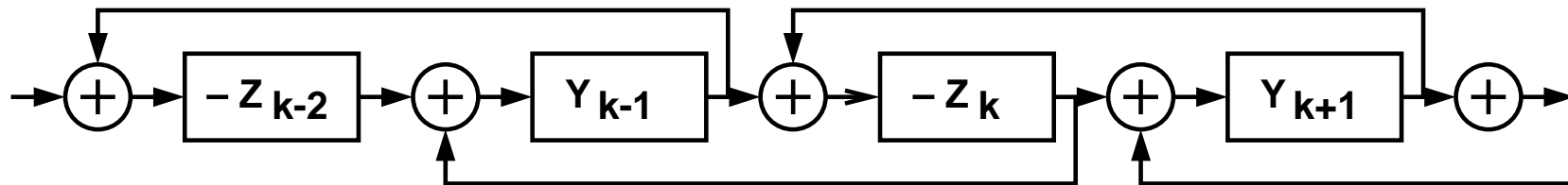
# LC Ladder Simulation



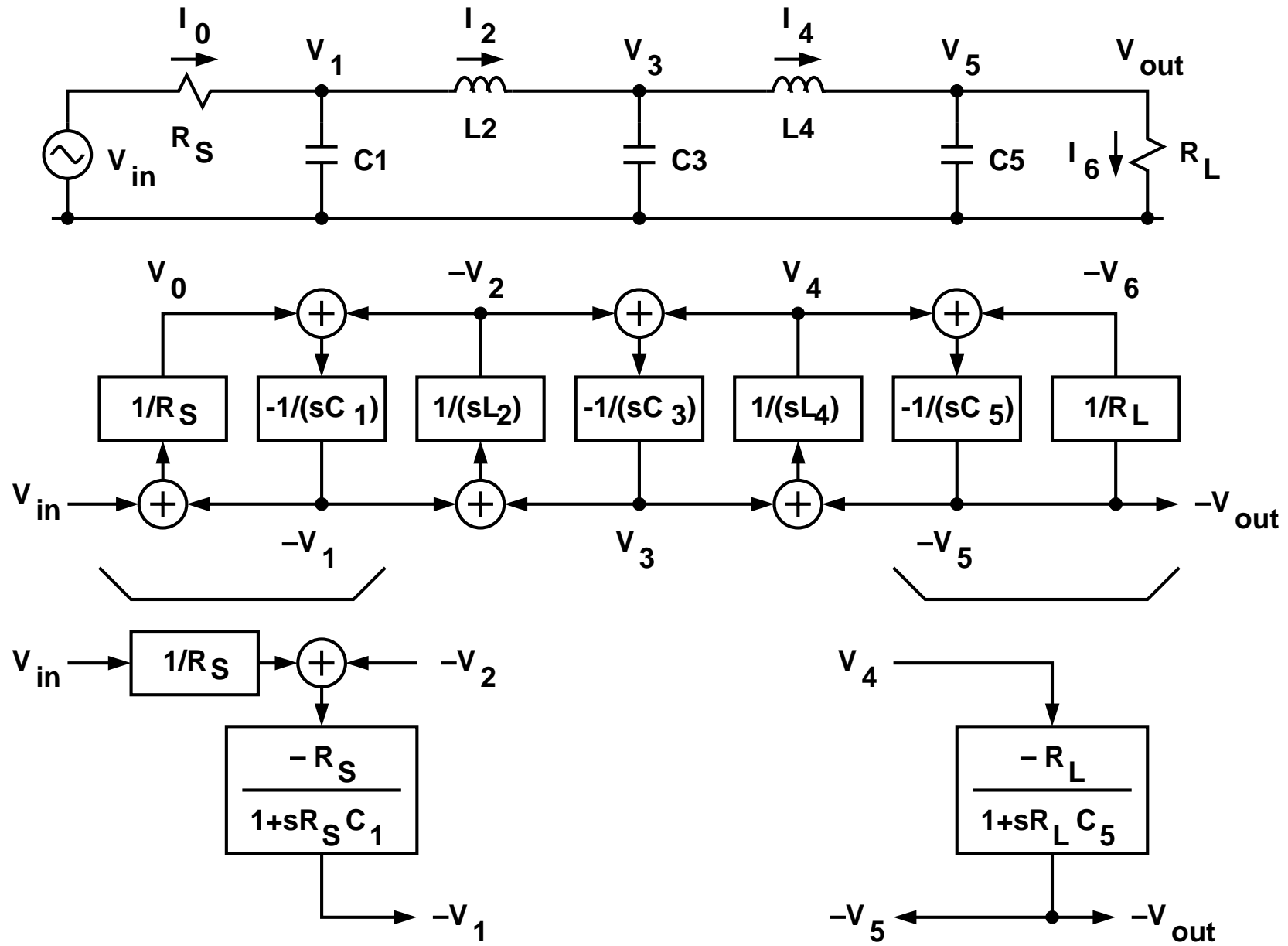
# LC Ladder Simulation



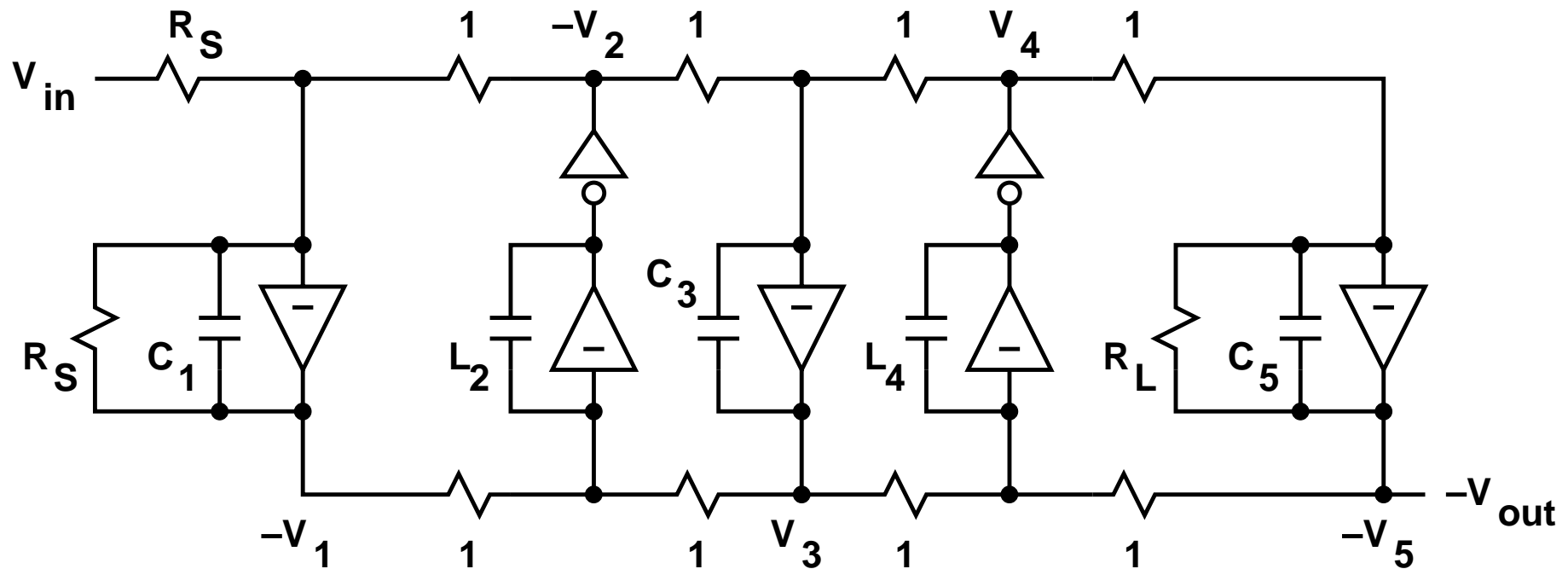
## Leapfrog (LF) Topology



# An All-Pole Low-Pass Ladder Filter

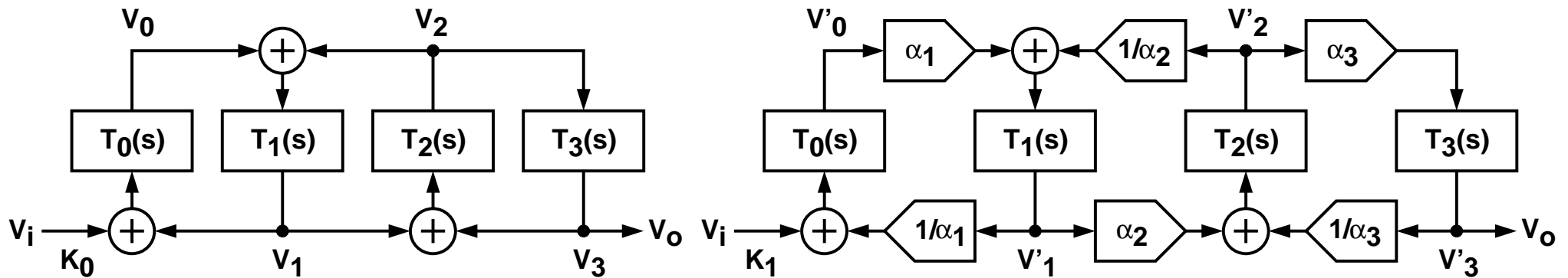


## An All-Pole Low-Pass Ladder Filter



- Component scaling can be done by maintaining the  $RC$  values.
- Use both lossless and lossy integrators.
- Combining the phase-lag Miller inverting integrator with the phase-lead noninverting integrator can reduce phase errors.

# Signal-Level Scaling in Ladder Filters



$$V_j = H_j(s) \cdot V_{j-1} \quad V'_j = \alpha_j H_j(s) \cdot V'_{j-1} \quad \Rightarrow \quad V'_j = V_j \cdot \alpha_j \cdot \frac{V'_{j-1}}{V_{j-1}}$$

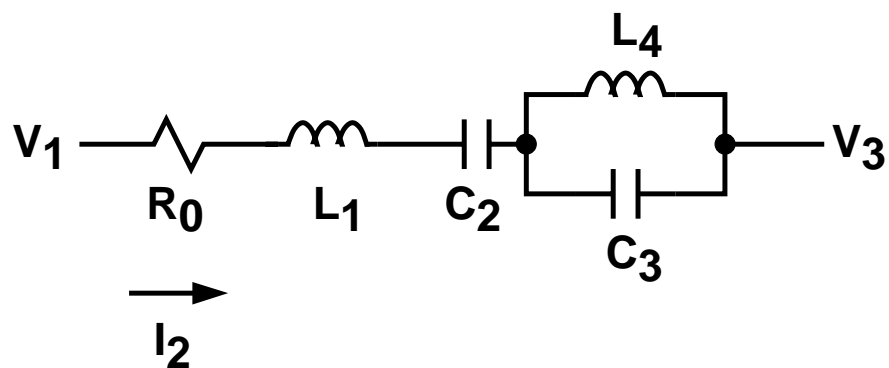
- The signal level of  $V_j$  can be scaled by  $\alpha_j$ .
- Signal-level scaling is to maximize dynamic range. Want

$$\max |V_j(j\omega)| = V_{o,max} \quad \text{for} \quad j = 0, \dots, n \quad 0 < \omega < \infty$$

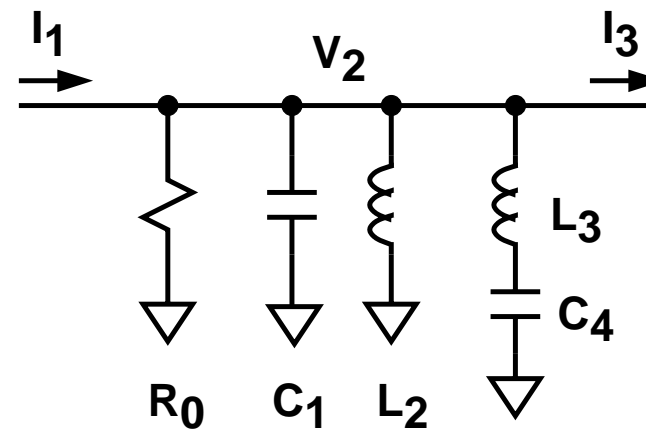
- Scale  $V_j$  sequentially from  $j = 1$  to  $j = n$ .

# General Ladder Branches

Series Branch



Shunt Branch



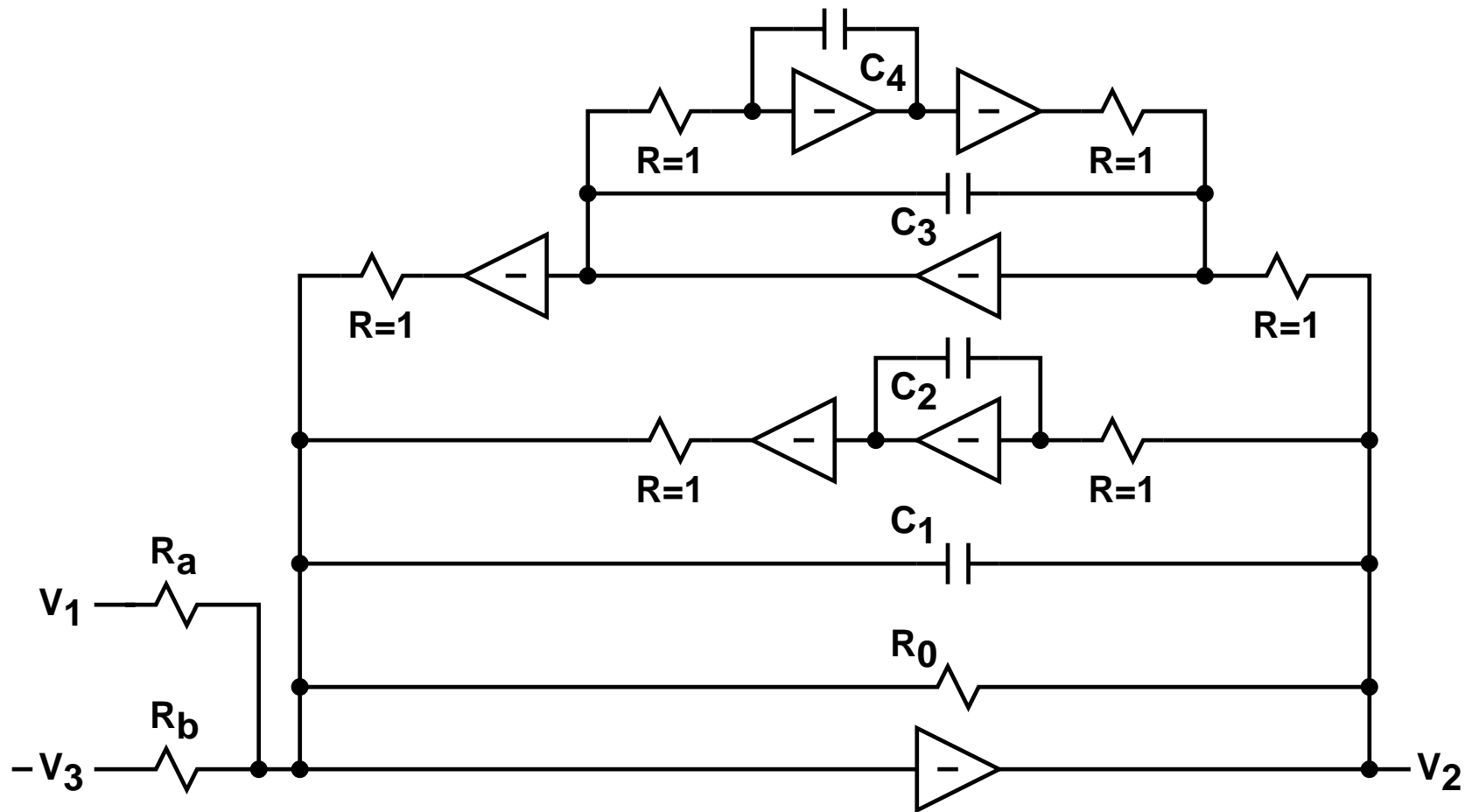
For the series branch

$$I_2 = (V_1 - V_3) \cdot Y(s) = (V_1 - V_3) \cdot \frac{1}{R_0 + sL_1 + \frac{1}{sC_2} + \frac{1}{sC_3 + \frac{1}{sL_4}}}$$

For the shunt branch

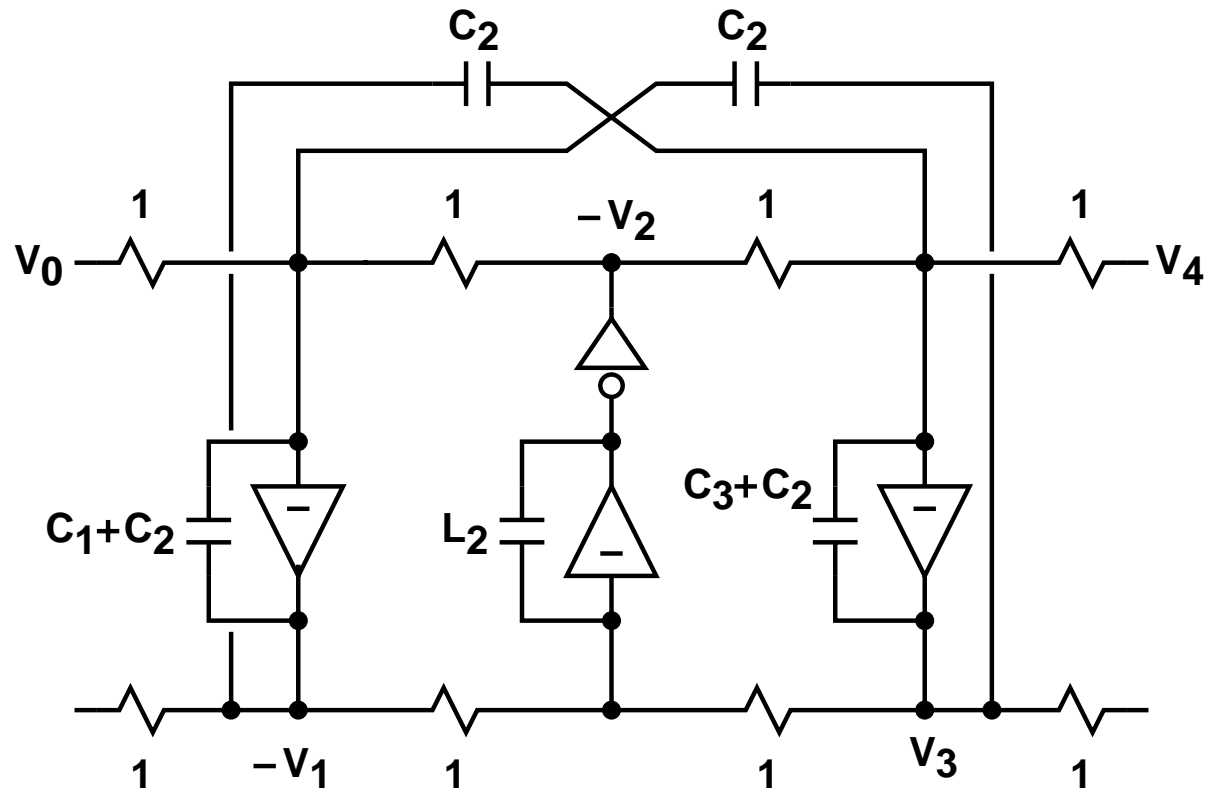
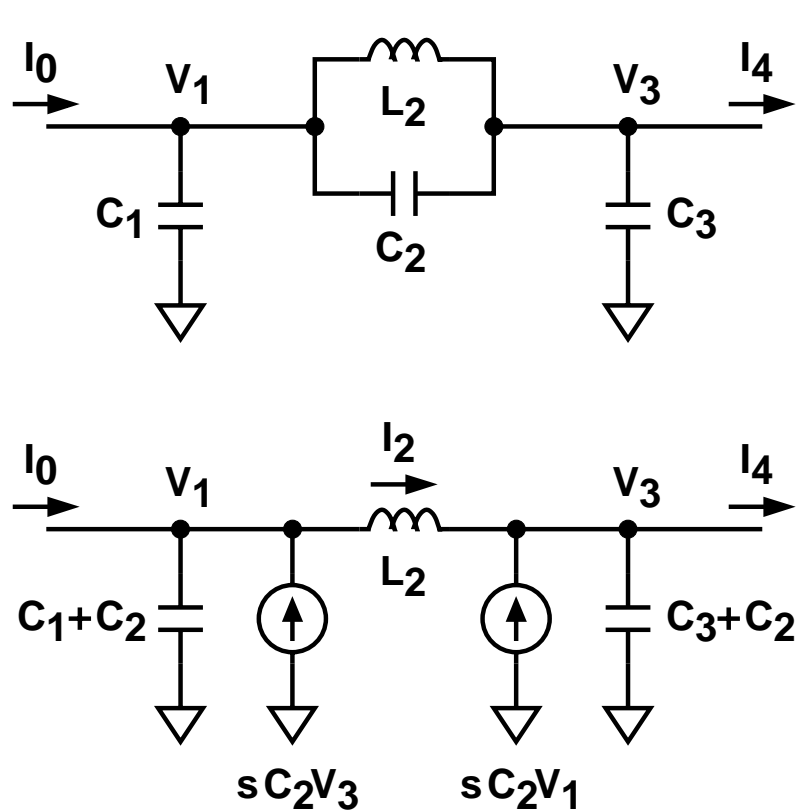
$$V_2 = (I_1 - I_3) \cdot Z(s) = (I_1 - I_3) \cdot \frac{1}{G_0 + sC_1 + \frac{1}{sL_2} + \frac{1}{sL_3 + \frac{1}{sC_4}}}$$

# General Ladder Branches by Active-RC Implementation



$$V_2 = - \left( \frac{V_1}{R_a} - \frac{V_3}{R_b} \right) \cdot \frac{1}{G_0 + sC_1 + \frac{1}{sC_2} + \frac{1}{sC_3 + \frac{1}{sC_4}}}$$

# Finite Transmission Zeros in the Series Branches



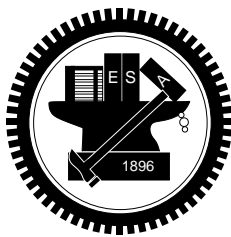
$$I_0 = sC_1V_1 + (sC_2 + Y_2)(V_1 - V_3) = s(C_1 + C_2)V_1 - sC_2V_3 - Y_2(V_1 - V_3)$$

$$I_4 = (sC_2 + Y_2)(V_1 - V_3) - sC_3V_3 = Y_2(V_1 - V_3) + sC_2V_1 - s(C_2 + C_3)V_3$$

# MOST-C and $G_m$ -C Filters

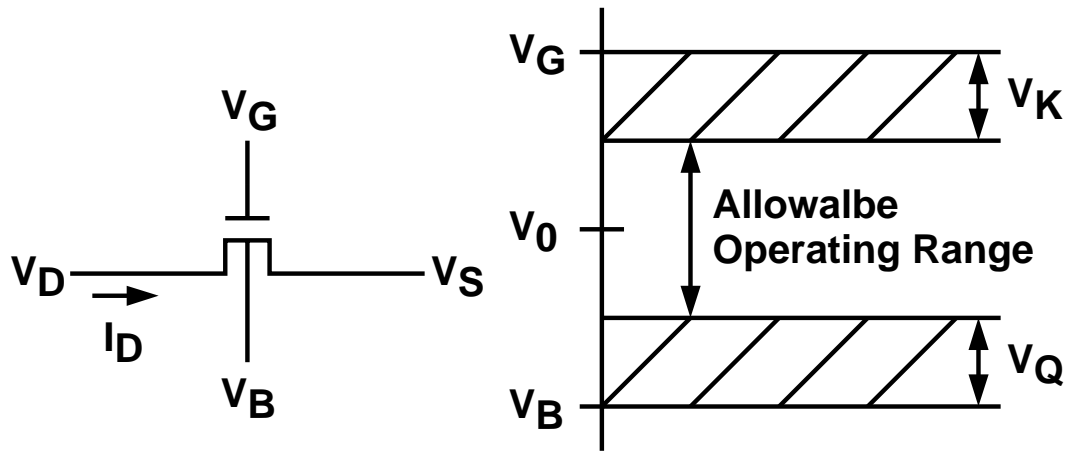
Jieh-Tsorng Wu

July 16, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# MOSTs in the Triode Region



$V_{FB}$  = Flat-Band Voltage

$\phi_0$  = Surface Band Bending  $\approx 2\phi_f$

$\gamma$  = Body Effect Coefficient

$$k = \mu C_{ox} \frac{W}{L}$$

$$V_K = V_{FB} + \phi_0 - \frac{\gamma^2}{2} + \gamma \sqrt{V_{GB} - V_{FB} + \frac{\gamma^2}{4}} \quad V_Q \leftarrow \text{Model Accuracy Consideration}$$

$$\frac{I_D}{k} = (V_{GB} - V_{FB} - \phi_0)(V_{DB} - V_{SB}) - \frac{1}{2} (V_{DB}^2 - V_{SB}^2) - \frac{2}{3} \gamma \left[ (V_{DB} + \phi_0)^{\frac{3}{2}} - (V_{SB} + \phi_0)^{\frac{3}{2}} \right]$$

$$= (V_{GB} - V_{FB} - \phi_0)V_{DS} - [f(V_{DB}) - f(V_{SB})]$$

$$f(V_{XB}) = \frac{1}{2} V_{XB}^2 + \frac{2}{3} \gamma (V_{XB} + \phi_0)^{\frac{3}{2}} = \frac{1}{2} (V_{X0} + V_{0B})^2 + \frac{2}{3} \gamma (V_{X0} + V_{0B} + \phi_0)^{\frac{3}{2}}$$

# MOSTs in the Triode Region

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Using Taylor's series

$$f(V_{XB}) \approx \left( \frac{1}{2}V_{0B}^2 + V_{0B} \cdot V_{X0} + \frac{1}{2}V_{X0}^2 \right) + \frac{2}{3}\gamma(V_{0B} + \phi_0)^{\frac{3}{2}} + \gamma(V_{0B} + \phi_0)^{\frac{1}{2}} \cdot V_{X0} \\ + \frac{1}{4}\gamma(V_{0B} + \phi_0)^{-\frac{1}{2}} \cdot V_{X0}^2 - \frac{1}{24}\gamma(V_{0B} + \phi_0)^{-\frac{3}{2}} \cdot V_{X0}^3 + \dots$$

We have

$$\frac{I_D}{k} = (V_{G0} - V_T)V_{DS} - [g(V_{D0}) - g(V_{S0})] \quad V_T = V_{FB} + \phi_0 + \gamma(V_{0B} + \phi_0)^{\frac{1}{2}}$$

$$g(V_{X0}) = g_e(V_{X0}) + g_o(V_{X0}) \quad g_e(-V_{X0}) = g_e(V_{X0}) \quad g_o(-V_{X0}) = -g_e(V_{X0})$$

$$g_e(V_{X0}) = \frac{1}{2} \cdot V_{X0}^2 + \frac{1}{4}\gamma(V_{0B} + \phi_0)^{-\frac{1}{2}} \cdot V_{X0}^2 + \dots$$

$$g_o(V_{X0}) = -\frac{1}{24}\gamma(V_{0B} + \phi_0)^{-\frac{3}{2}} \cdot V_{X0}^3 + \dots$$

# MOSTs in the Triode Region

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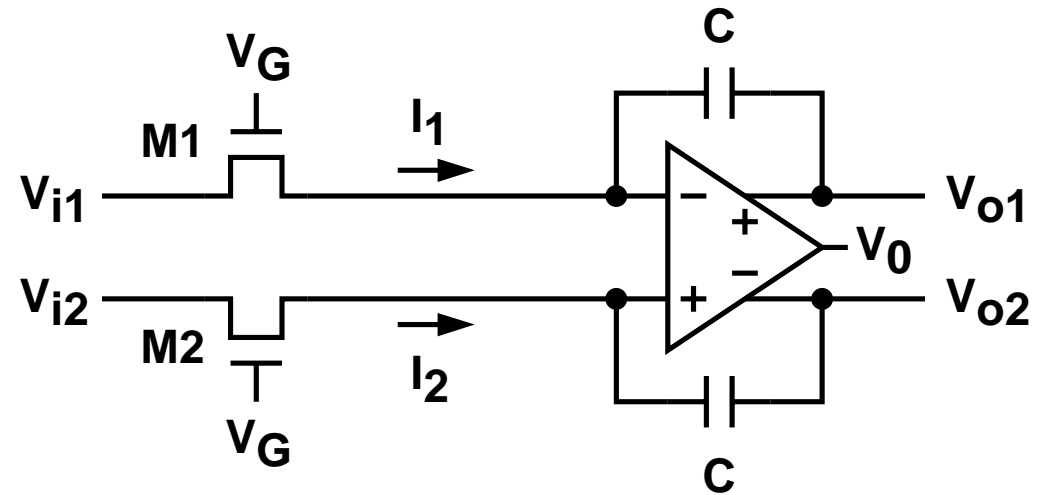
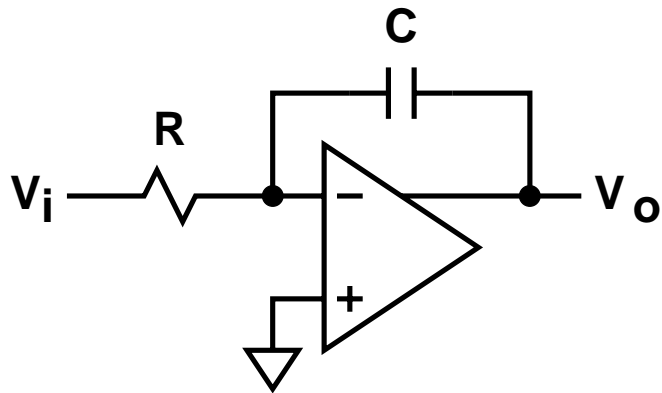
Thus

$$I_D = I_L - I_N \quad I_L = k(V_{G0} - V_T) \times V_{DS} = G \times V_{DS} \quad I_N = k [g(V_{D0}) - g(V_{S0})]$$

- Both  $g_e$  and  $g_o$  are independent of  $V_G$ .
- $g_o(V_{D0}) - g_o(V_{S0})$  is very small comparing to  $I_L$  (e.g., 0.1 percent of it or less).
- $g_e(V_{D0}) - g_e(V_{S0})$  can be large and its effect must be eliminated to obtain a linear resistor.
- If only  $I_L$  is considered, the resistance between  $V_D$  and  $V_S$  is

$$G = \frac{I_D}{V_{DS}} = k(V_{G0} - V_T) = \mu C_{ox} \frac{W}{L} (V_{G0} - V_T)$$

# MOST-C Fully-Balanced Integrators



$$V_{i1} = +\frac{V_i}{2} + V_0 \quad V_{i2} = -\frac{V_i}{2} + V_0 \quad V_{o1} = +\frac{V_o}{2} + V_0 \quad V_{o2} = -\frac{V_o}{2} + V_0$$

$$I_1 = G \times \left( +\frac{V_i}{2} \right) - \left[ g_e \left( +\frac{V_i}{2} \right) - g_e(0) \right] - \left[ g_o \left( +\frac{V_i}{2} \right) - g_o(0) \right]$$

$$I_2 = G \times \left( -\frac{V_i}{2} \right) - \left[ g_e \left( -\frac{V_i}{2} \right) - g_e(0) \right] - \left[ g_o \left( -\frac{V_i}{2} \right) - g_o(0) \right]$$

$$I_1 - I_2 = G \times V_i - 2g_o \left( \frac{V_i}{2} \right) \approx G \times V_i \quad G = k(V_G - V_0 - V_T)$$

# MOST-C Fully-Balanced Integrators

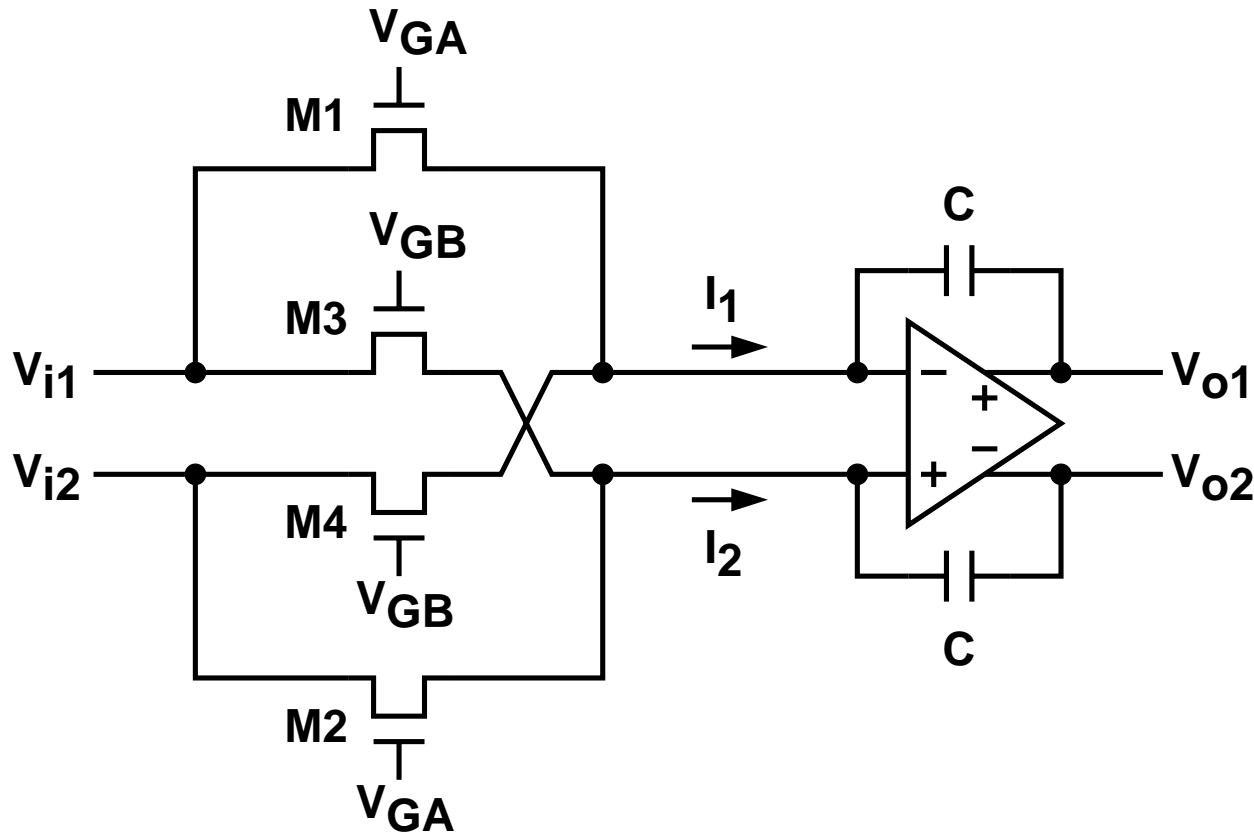
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Therefore

$$\frac{V_o(s)}{V_i(s)} = \frac{I_1(s) - I_2(s)}{V_i(s)} \cdot \left( -\frac{1}{sC} \right) = -\frac{G}{sC}$$

- Even-order nonlinearities are eliminated.
- The common-mode voltage along the differential signal path must be maintained at  $V_0$ .
- Linearities around 50 dB have been achieved.

# Double MOST-C Differential Integrators



$$V_{i1} = +\frac{V_i}{2} + V_0$$

$$V_{i2} = -\frac{V_i}{2} + V_0$$

$$V_{o1} = +\frac{V_o}{2} + V_0$$

$$V_{o2} = -\frac{V_o}{2} + V_0$$

$$G_A = k_{1,2} (V_{GA} - V_0 - V_T)$$

$$G_B = k_{3,4} (V_{GB} - V_0 - V_T)$$

$$I_1 = G_A \times \left( +\frac{V_i}{2} \right) - \left[ g \left( +\frac{V_i}{2} \right) - g(0) \right] + G_B \times \left( -\frac{V_i}{2} \right) - \left[ g \left( -\frac{V_i}{2} \right) - g(0) \right]$$

$$I_2 = G_A \times \left( -\frac{V_i}{2} \right) - \left[ g \left( -\frac{V_i}{2} \right) - g(0) \right] + G_B \times \left( +\frac{V_i}{2} \right) - \left[ g \left( +\frac{V_i}{2} \right) - g(0) \right]$$

# Double MOST-C Differential Integrators

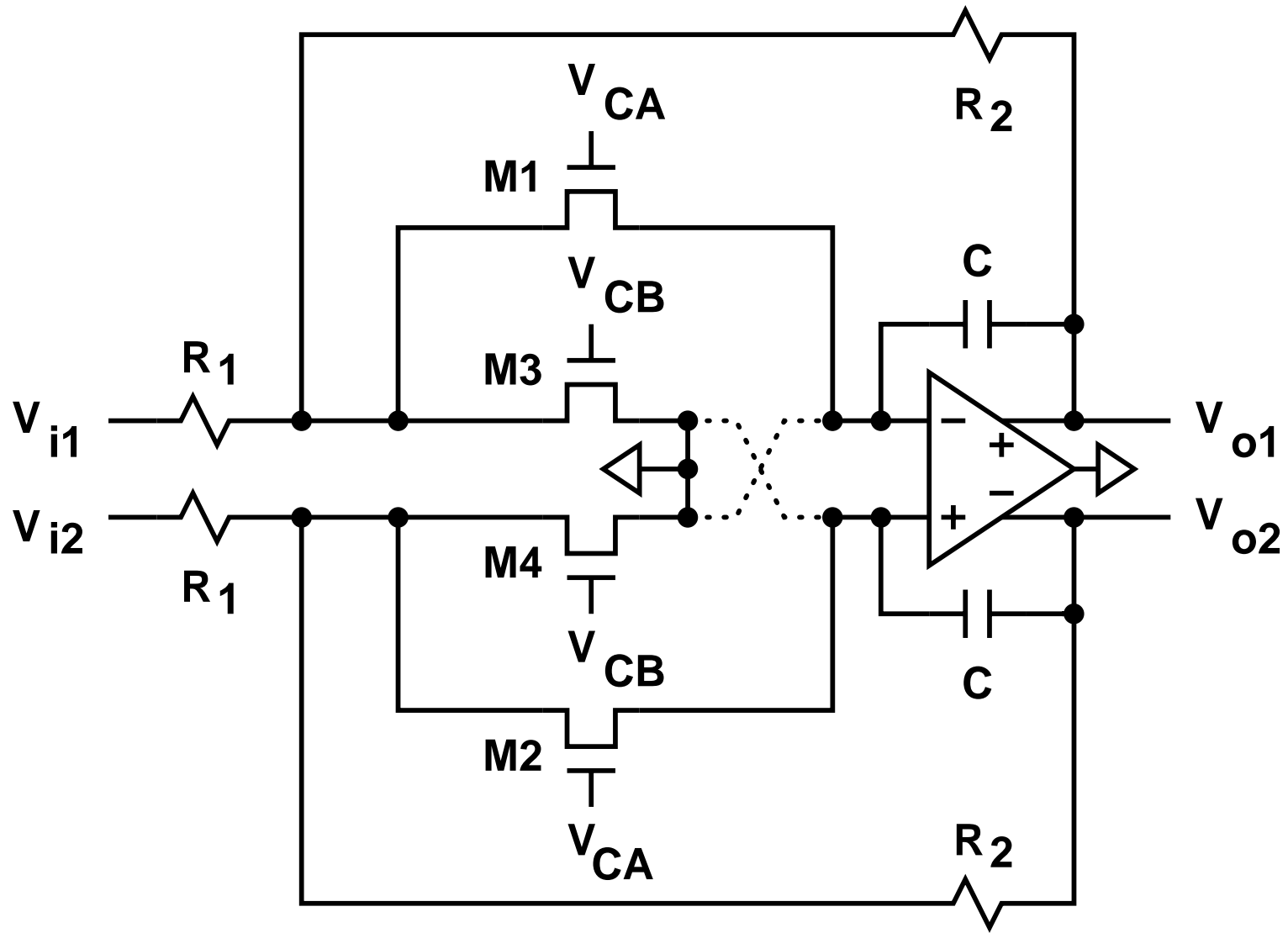
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We have

$$I_1 - I_2 = (G_A - G_B) \times V_i \quad \frac{V_o(s)}{V_i(s)} = \frac{I_1(s) - I_2(s)}{V_i(s)} \cdot \left( -\frac{1}{sC} \right) = -\frac{G_A - G_B}{sC}$$

- Both even-order and odd-order nonlinearities are eliminated.
- Differential signals are not required to be fully balanced.
- Around 10 dB linearity improvement over the two-transistor MOST-C integrators.
- Linearity performance is limited by the deviation of the above device model and mismatches among the MOSTs.
- Reference: Ismail, JSSC 2/88, pp. 183–194.

# R-MOST-C Differential Integrators



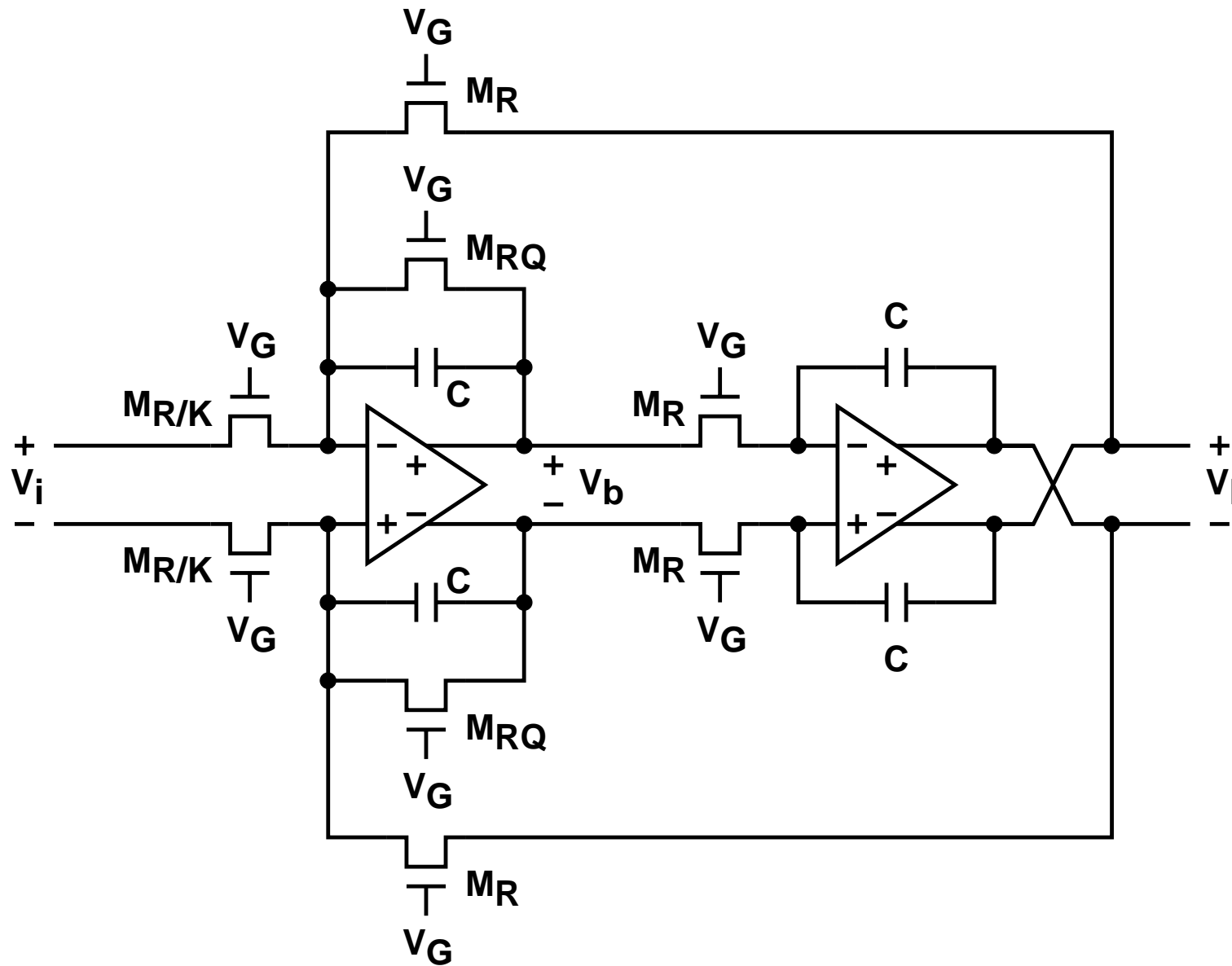
# R-MOST-C Differential Integrators

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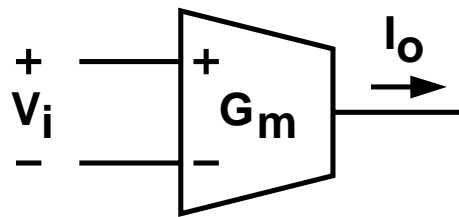
$$\frac{V_o}{V_i} = -\frac{R_2/R_1}{sC \left[ R_2 \left( 1 + \frac{R_{M1}}{R_1 \parallel R_2 \parallel R_{M2}} \right) \right] + 1}$$

- The dc gain is not adjustable.
- The integrator's time constant can be varied by changing  $R_{M1}$  and  $R_{M2}$
- At low-frequencies, the linear resistors,  $R_1$  and  $R_2$ , dominate the transfer function, thus reducing distortion. A linearity of 90  $dB$  has been achieved.
- In the criss-cross version, M3 and M4 reduce the effective dc gain and bandwidth of the integrator, enhance the unity-gain frequency sensitivity to component mismatches, and increase noises.
- Reference: U-K Moon, et al., JSSC 12/93, pp. 1254–1264.

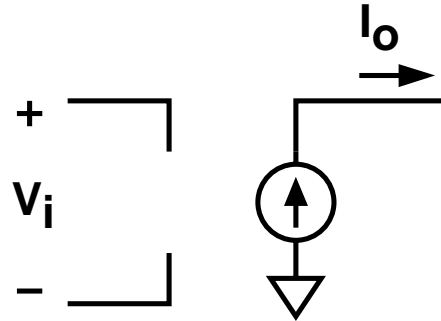
# A MOST-C Tow-Thomas Biquad



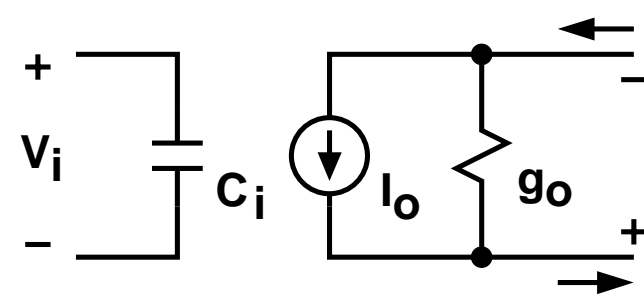
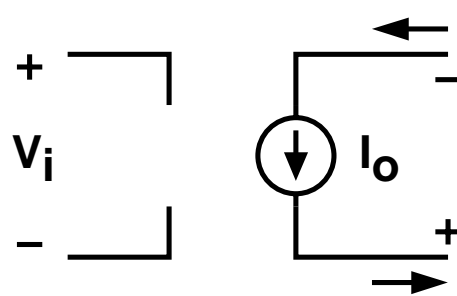
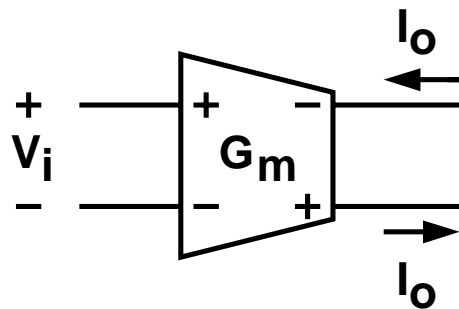
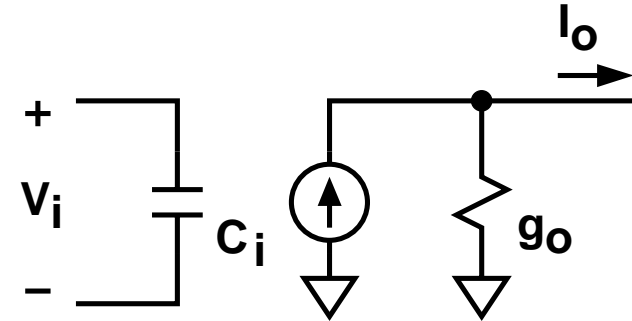
# Transconductors



Ideal Model



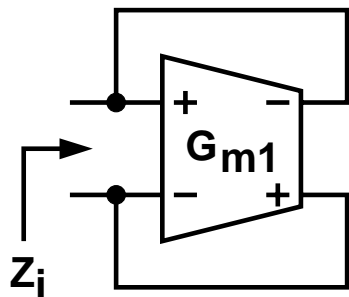
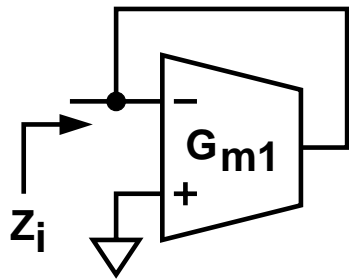
Nonideal Model



$$I_o = G_m \times V_i$$

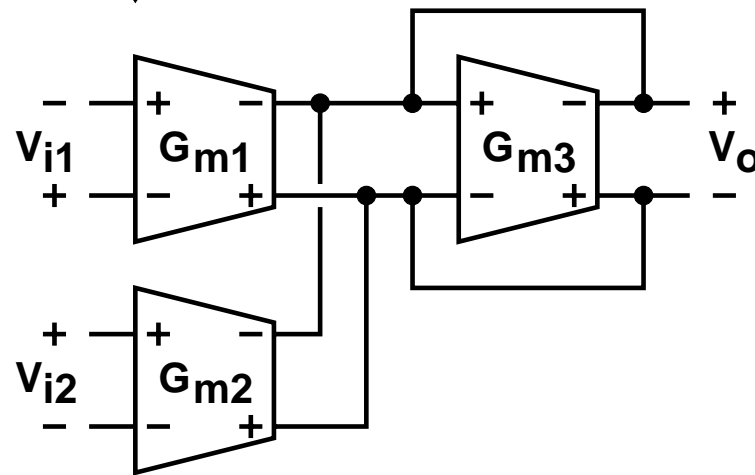
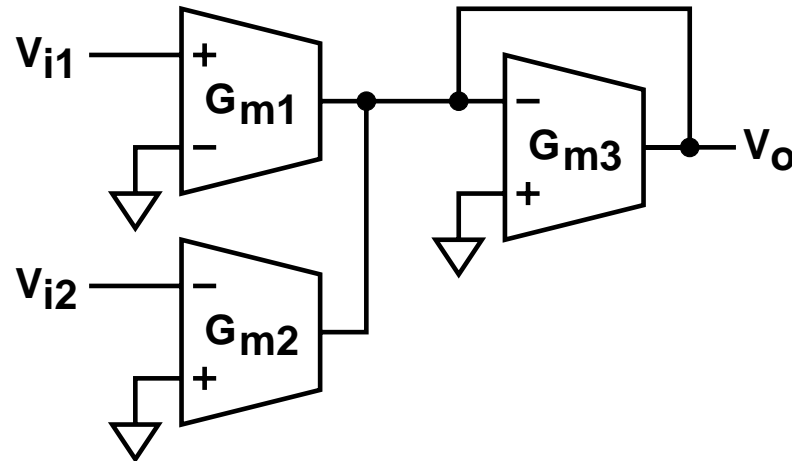
# Transconductor Basic Circuits

Controlled Resistance



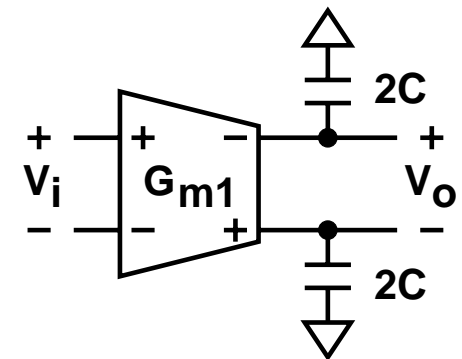
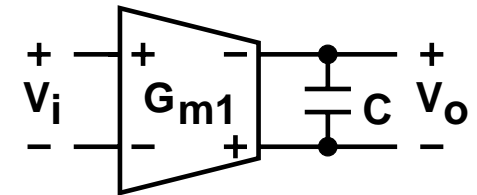
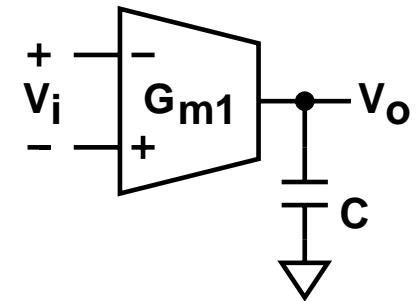
$$Z_i = \frac{1}{G_{m1}}$$

Voltage Amplifier



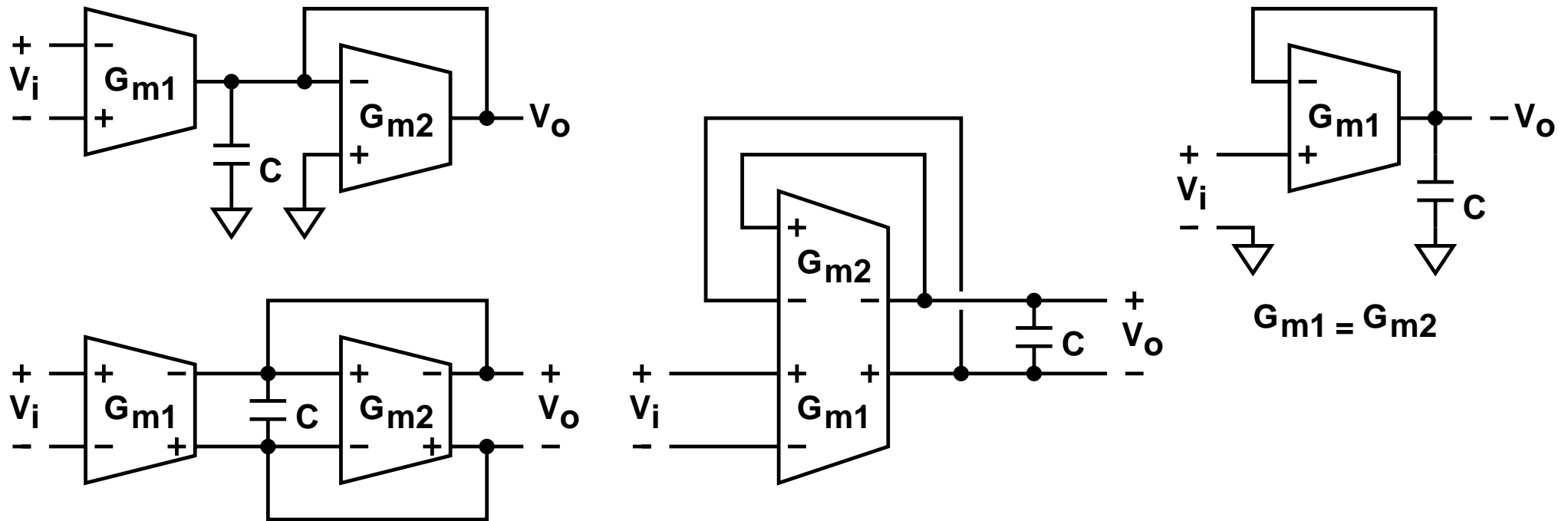
$$V_o = \frac{1}{G_{m3}} \cdot (G_{m1}V_{i1} - G_{m2}V_{i2})$$

Lossless Integrator



$$\frac{V_o(s)}{V_i(s)} = -\frac{G_m}{sC}$$

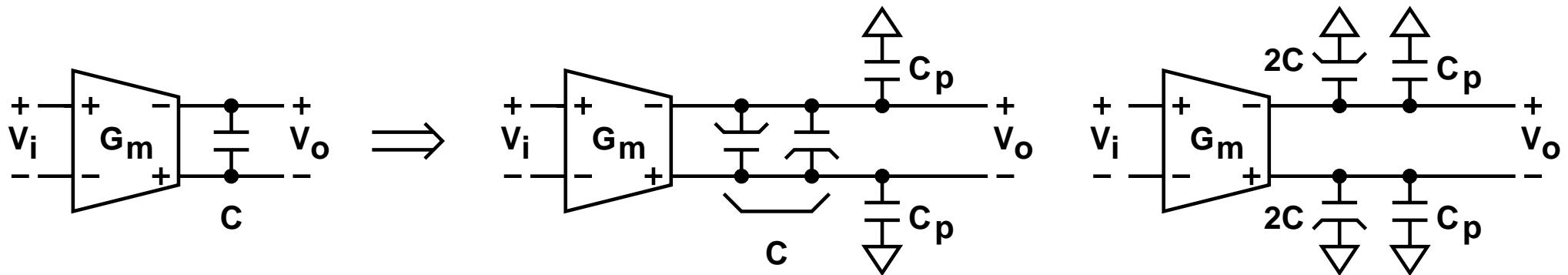
# $G_m$ -C Lossy Integrator



$$\frac{V_o(s)}{V_i(s)} = -\frac{G_{m1}}{sC + G_{m2}}$$

- Since no feedback for the integrators, they can be wide-band.
- A transconductor's output current should be linearly related to the input over the entire input voltage range.

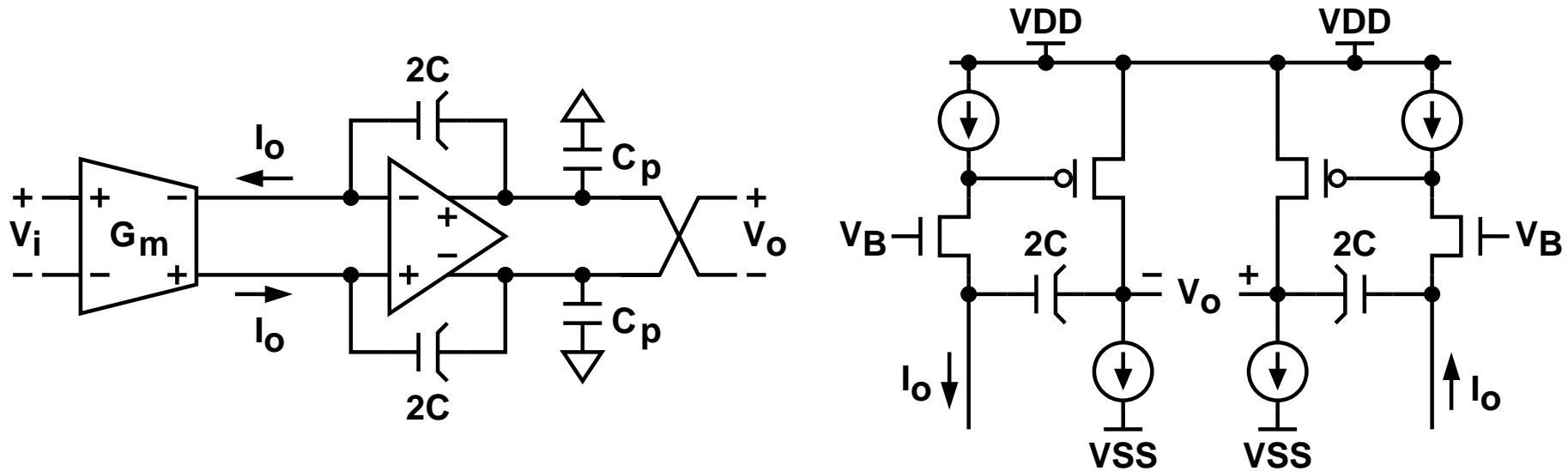
# Fully-Differential $G_m$ -C Integrators



$$\frac{V_o(s)}{V_i(s)} = -\frac{G_m}{s(C + C_p/2)}$$

- Can use only grounded capacitors.
- The  $C_p$  can affect the integration time constant.
- Partially nonlinear  $C_p$  can also cause linearity problems.

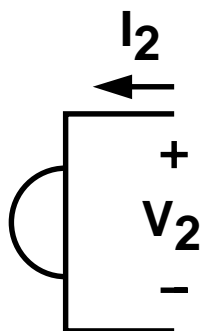
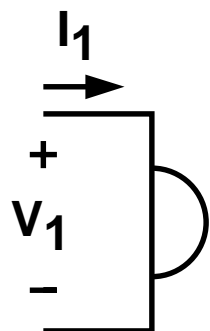
# $G_m$ -C Opamp Integrators (Miller Integrators)



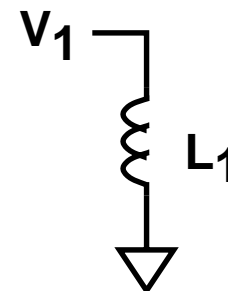
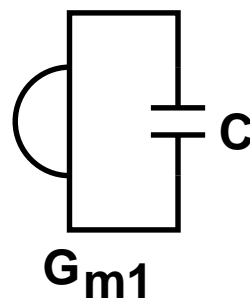
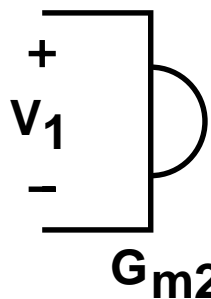
$$\frac{V_o(s)}{V_i(s)} = -\frac{G_m}{sC}$$

- The effects of parasitic capacitances are reduced.
- The  $G_m$ 's output stage can be simplified, since no large voltage swing is required.
- The lower impedances at the  $G_m$ 's output nodes make those nodes less sensitive to capacitive coupling of noise.

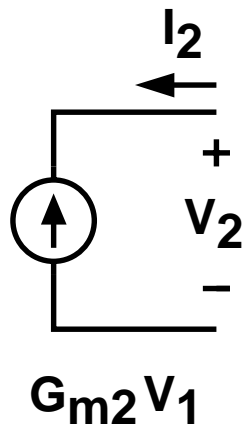
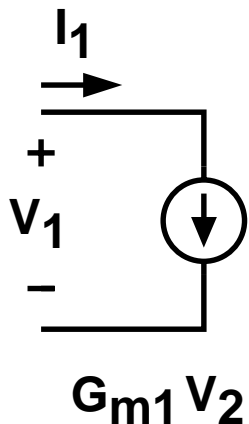
# Gyrators



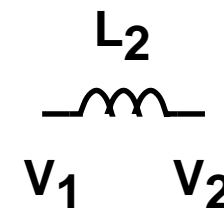
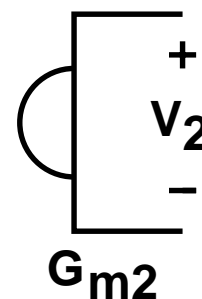
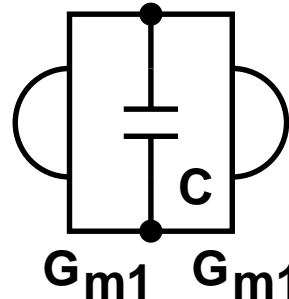
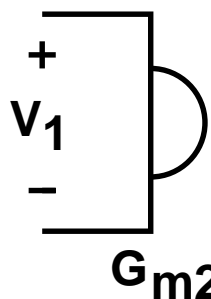
Grounded Inductor



Model



Floating Inductor

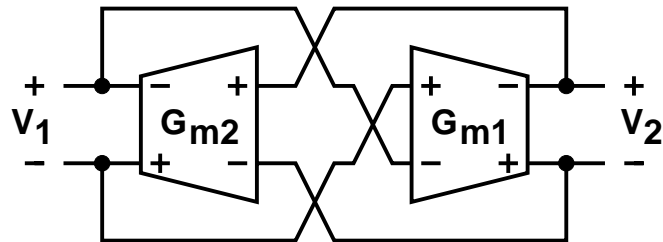
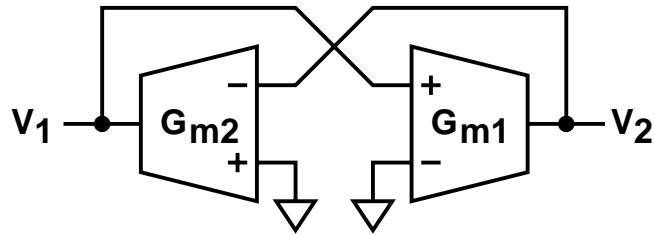


$$L_1 = \frac{C}{G_{m1} \cdot G_{m2}}$$

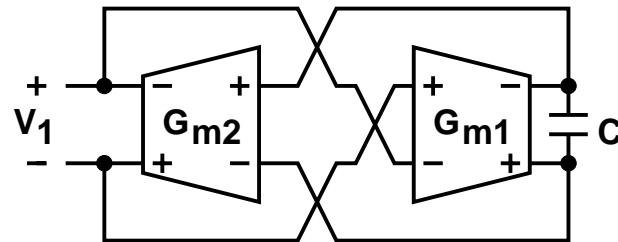
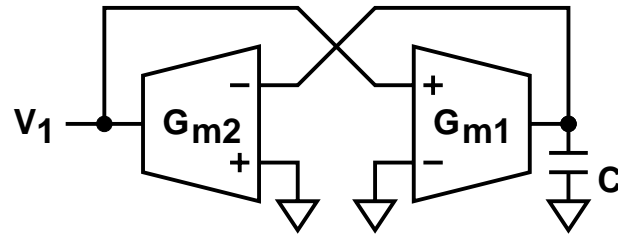
$$L_2 = \frac{C}{G_{m1} \cdot G_{m2}}$$

# $G_m$ -C Simulated Gyration

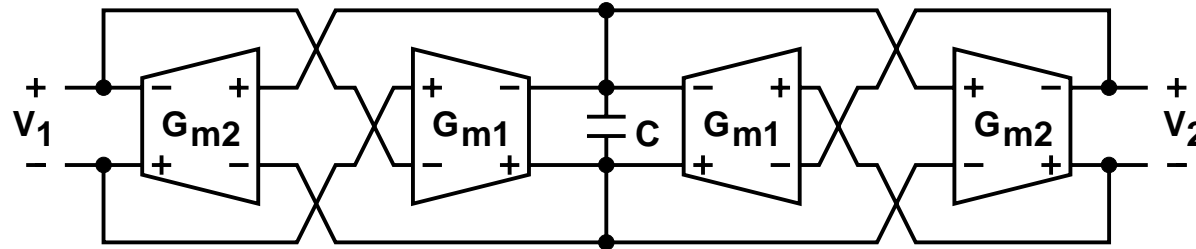
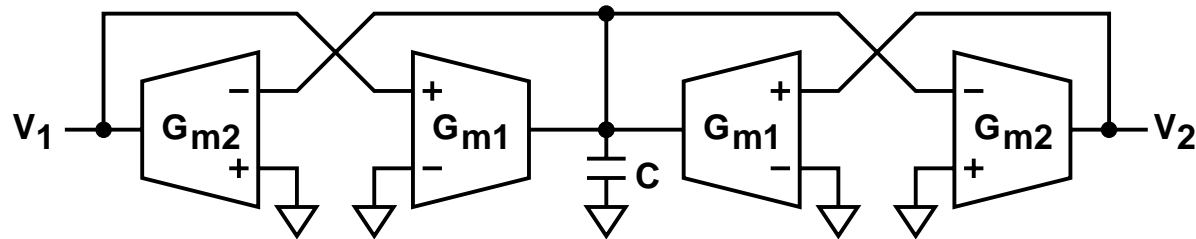
Gyrator



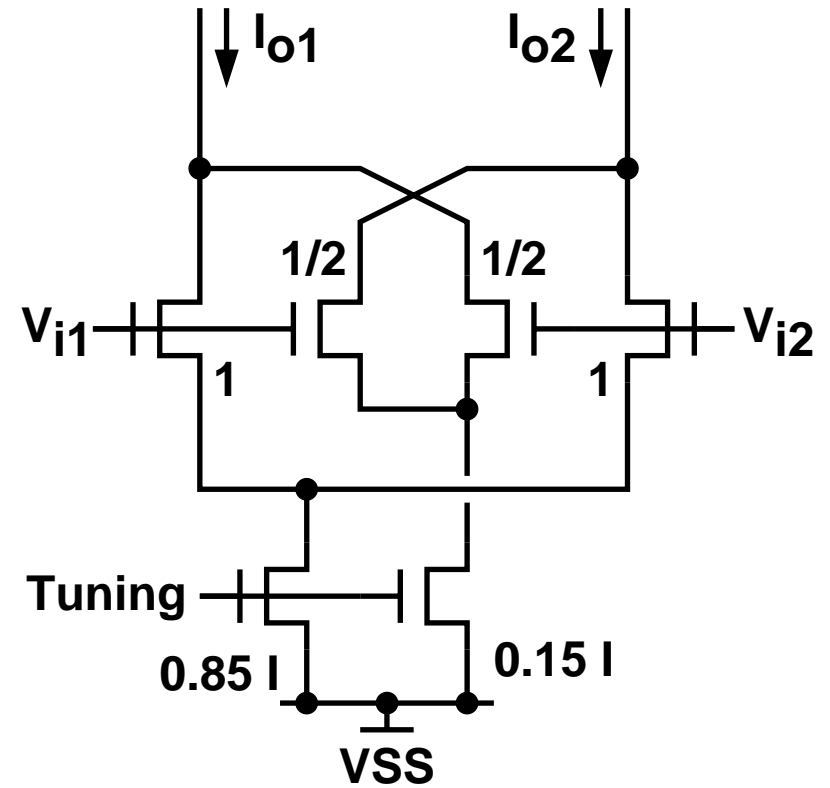
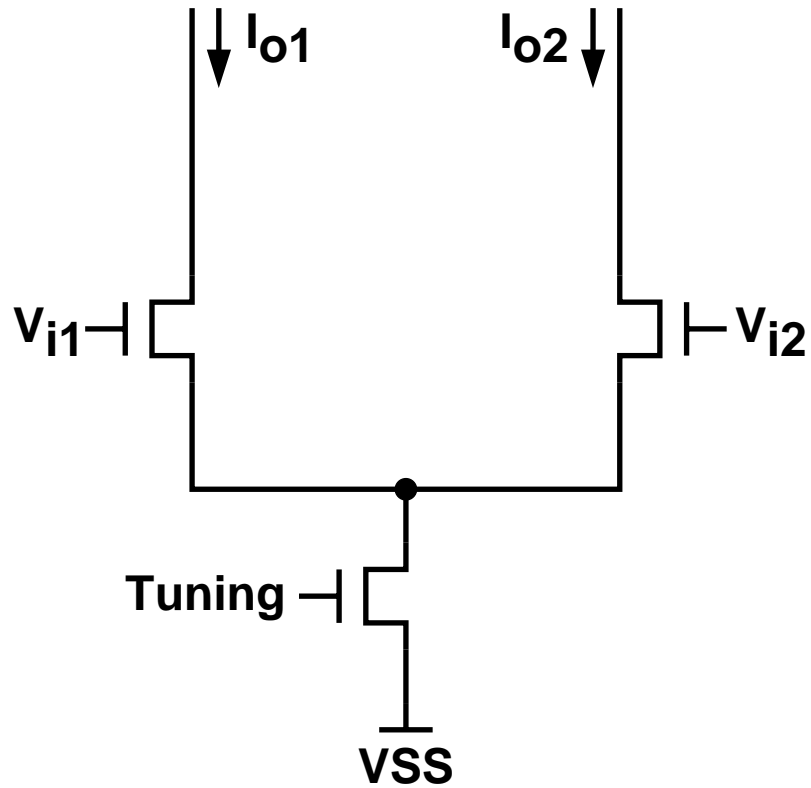
Simulated Grounded Inductor



Simulated Floating Inductor

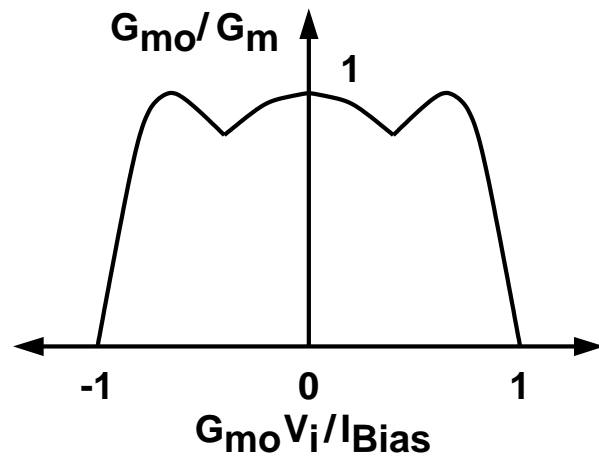
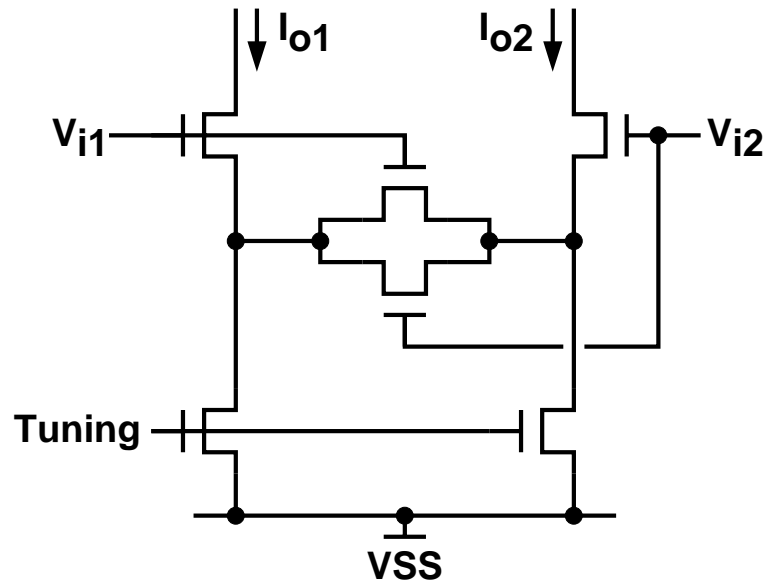


# MOST Transconductors

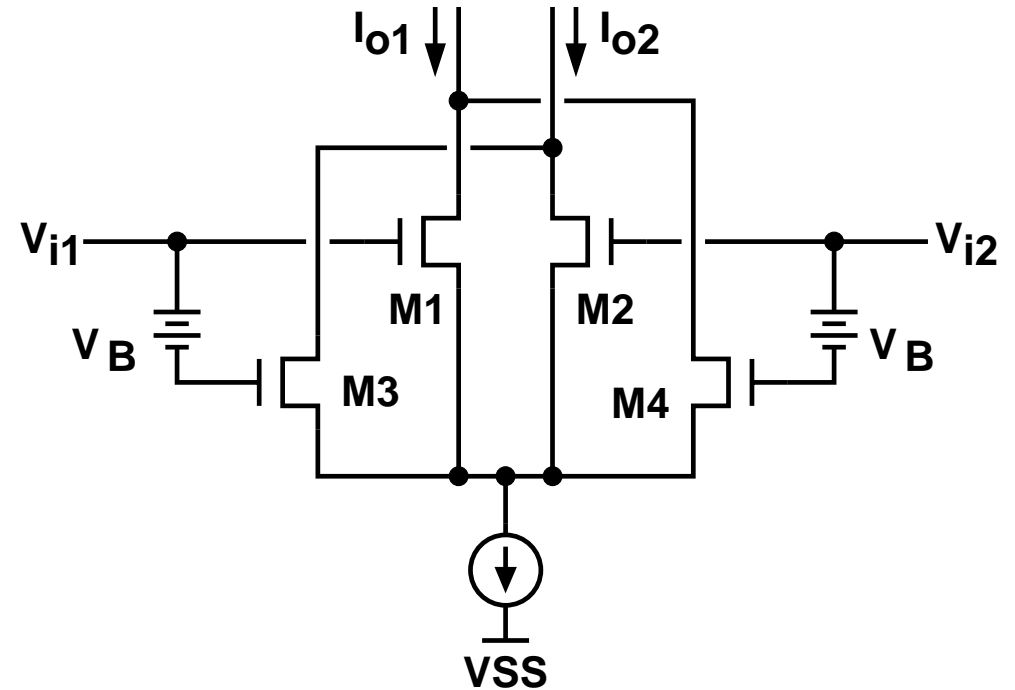


# MOST Transconductors

## Adaptive Source Degeneration



## Bias Offset Linearization

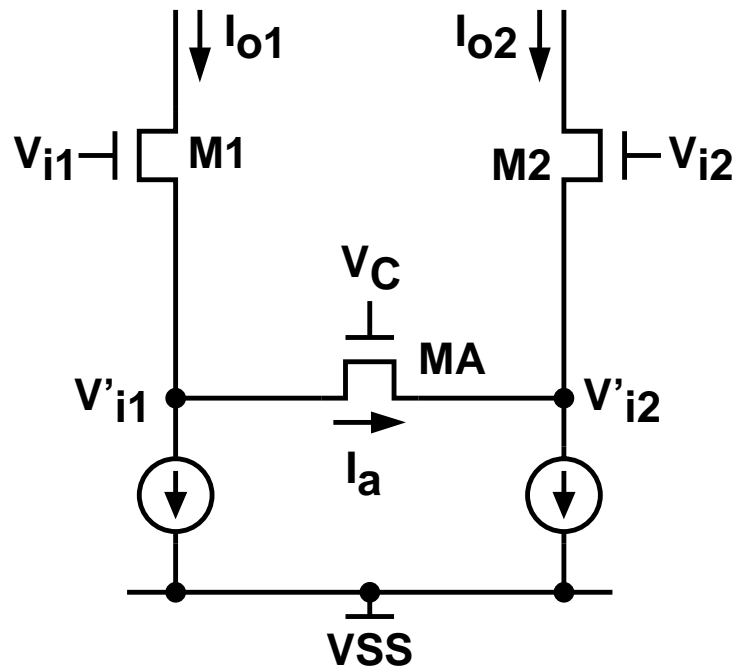


Let  $M1 = M2 = M3 = M4$ ,

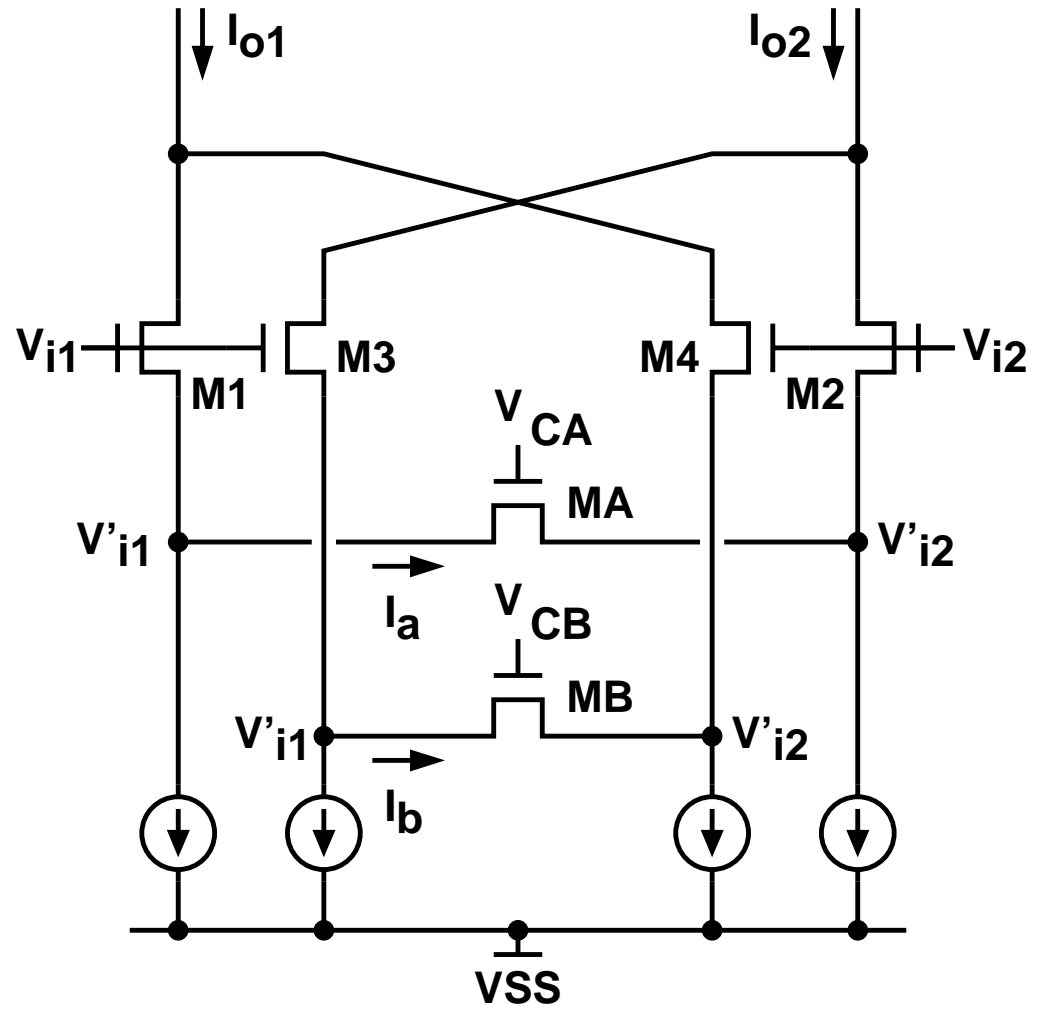
$$I_D = \frac{1}{2}k(V_{GS} - V_T)^2$$

$$I_{o1} = I_{o2} = kV_B(V_{i1} - V_{i2})$$

# MOST Transconductors with Source Degeneration



Fully Balanced Type



Double-MOST Type

# MOST Transconductors with Source Degeneration

---

Let

$$V'_{i1} = +\frac{V_i}{2} + V_0 \quad V'_{i2} = -\frac{V_i}{2} + V_0 \quad G = k(V_C - V_0 - V_t)$$

For the fully balanced differential transconductor

$$I_a = G \times V_i - \left[ g_e \left( +\frac{V_i}{2} \right) - g_e \left( -\frac{V_i}{2} \right) \right] - \left[ g_o \left( +\frac{V_i}{2} \right) - g_o \left( -\frac{V_i}{2} \right) \right]$$

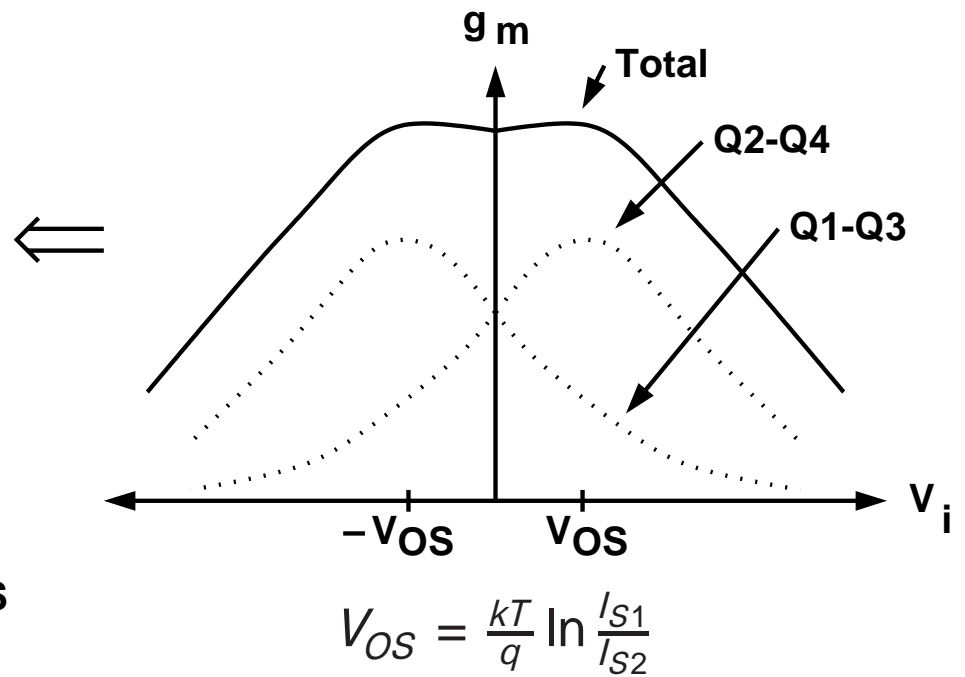
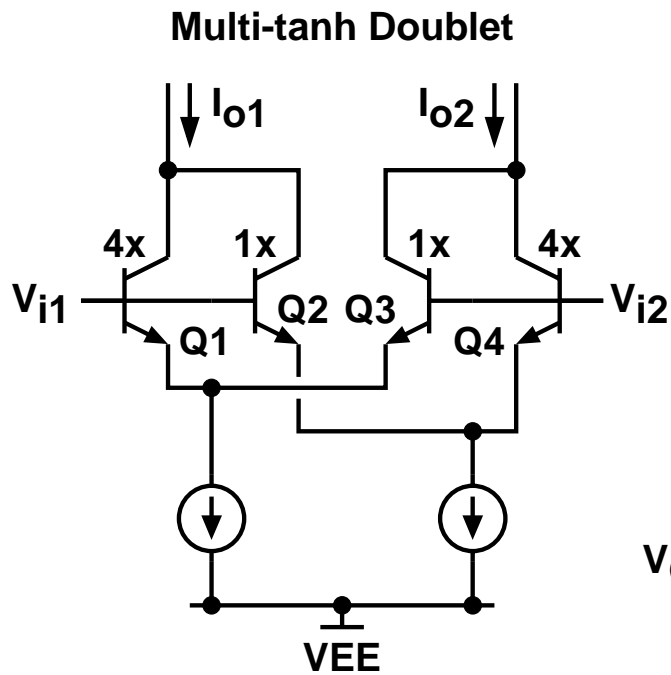
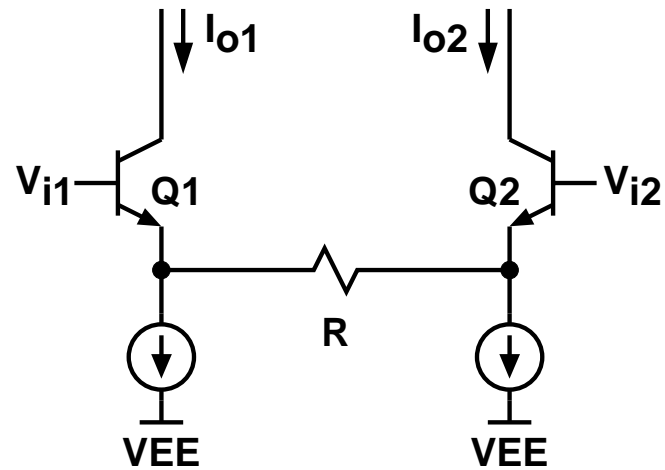
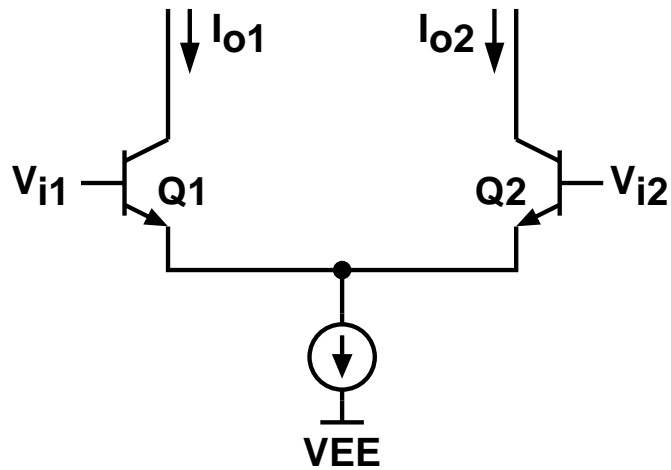
$$I_{o1} - I_{o2} = 2I_a \approx 2G \times V_i - 2g_o \left( +\frac{V_i}{2} \right) \approx 2G \times V_i$$

For the double-MOSFET differential transconductor

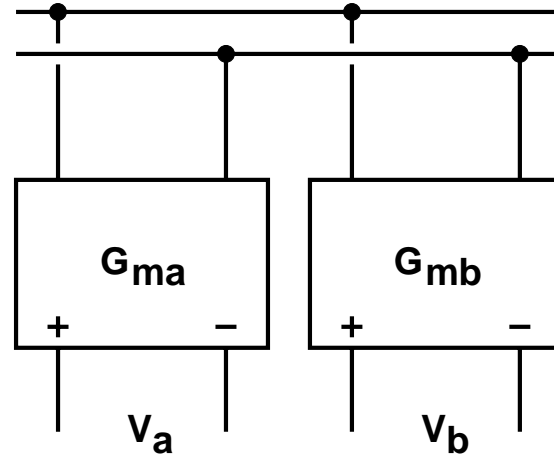
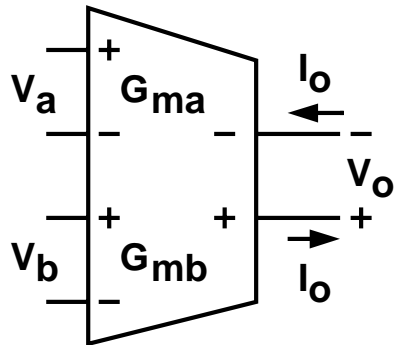
$$I_a = G_A \times V_i - \left[ g \left( +\frac{V_i}{2} \right) - g \left( -\frac{V_i}{2} \right) \right] \quad I_b = G_B \times V_i - \left[ g \left( +\frac{V_i}{2} \right) - g \left( -\frac{V_i}{2} \right) \right]$$

$$I_{o1} - I_{o2} = 2(I_a - I_b) = 2(G_A - G_B) \times V_i$$

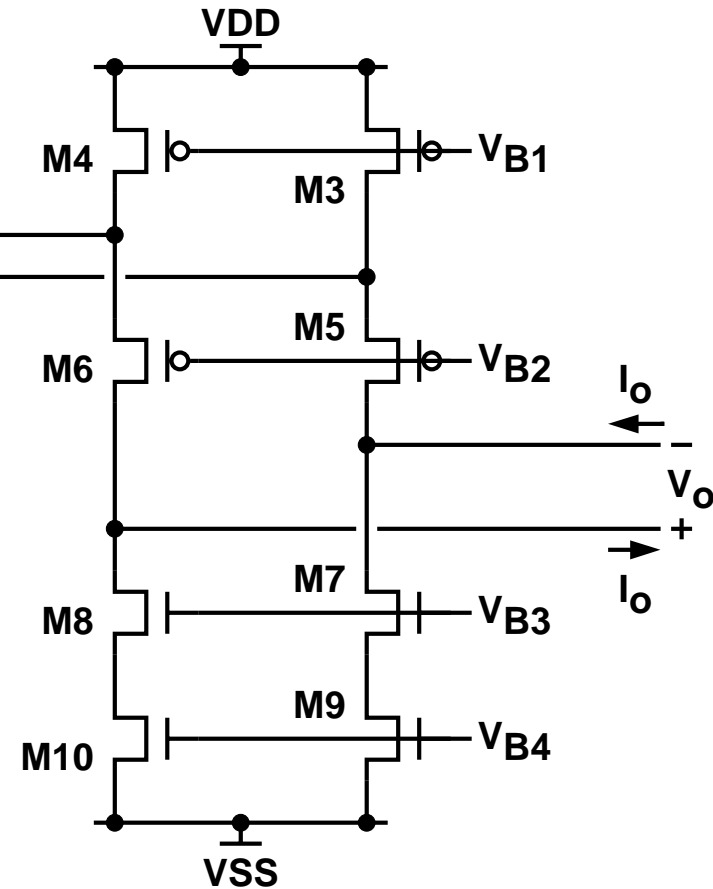
# BJT Transconductors



# Multi-Input Transconductors



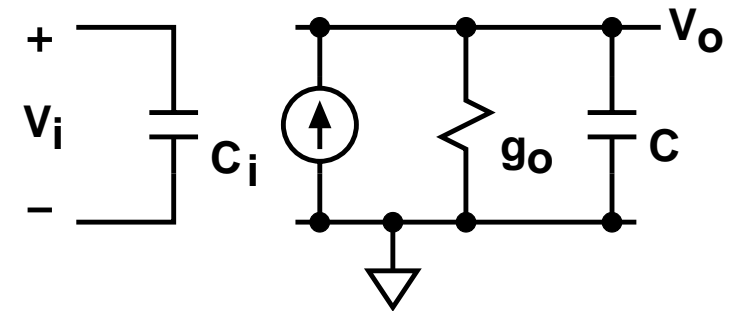
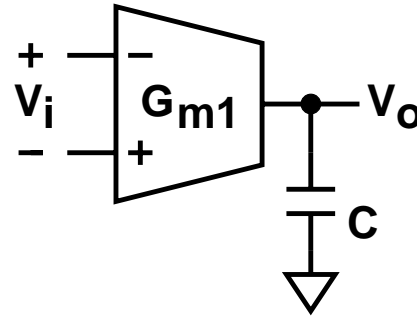
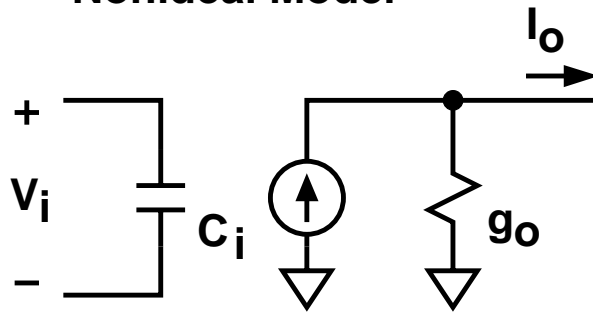
$$I_o = G_{ma} \cdot V_a + G_{mb} \cdot V_b$$



- Need only one output common-mode feedback.
- Reference: Edited by Y.P. Tsividis and J.O. Voorman, *“Integrated Continuous-Time Filters”*, IEEE Press, 1993.

# Transconductor's Imperfections

## Nonideal Model

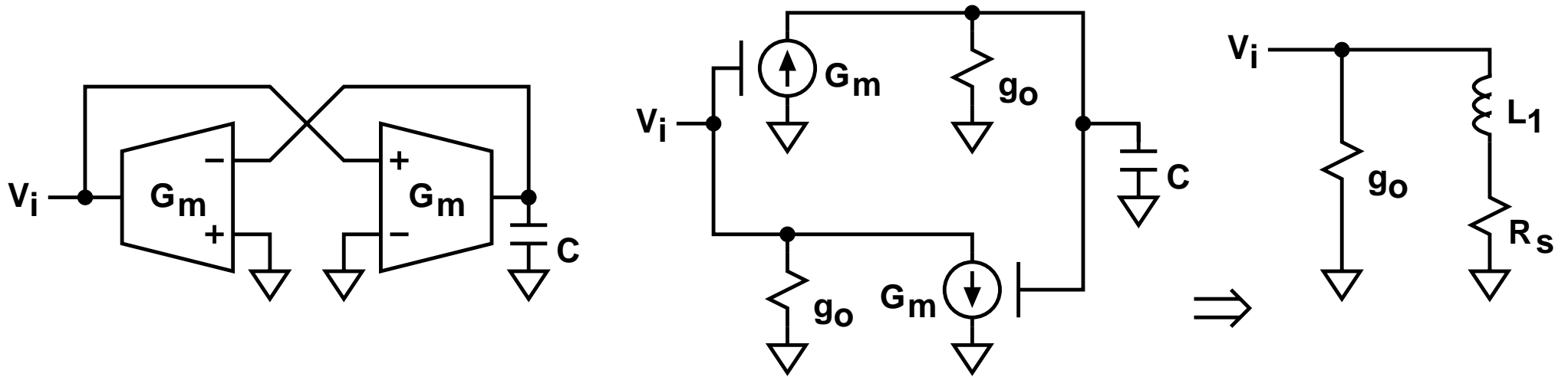


$$I_o = G_m(s) \times V_i \quad G_m(j\omega) = \frac{G_m}{1 + j\omega/\omega_2} \approx G_m e^{-j\phi} \quad \phi = \tan^{-1} \frac{\omega}{\omega_2}$$

For the  $G_m$ -C integrator

$$\frac{V_o}{V_i} = \frac{G_m}{1 + s/\omega_2} \times \frac{1}{sC + g_o} = \frac{G_m}{sC \left(1 + \frac{\omega_o}{\omega_2}\right) + g_o \left(1 + \frac{s^2}{\omega_o\omega_2}\right)} \quad \omega_o = \frac{g_o}{C}$$

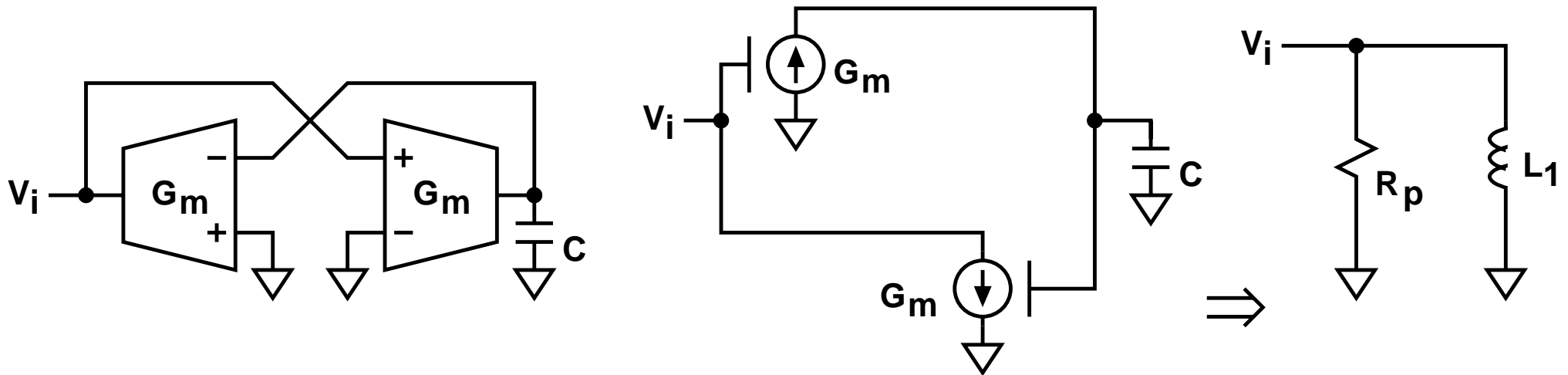
# The Effect of Non-Zero $g_o$ on Gyration



$$L = \frac{C}{G_m^2}$$

$$R_s = \frac{g_o}{G_m^2}$$

# The Effect of Phase Shift on Gyration



If

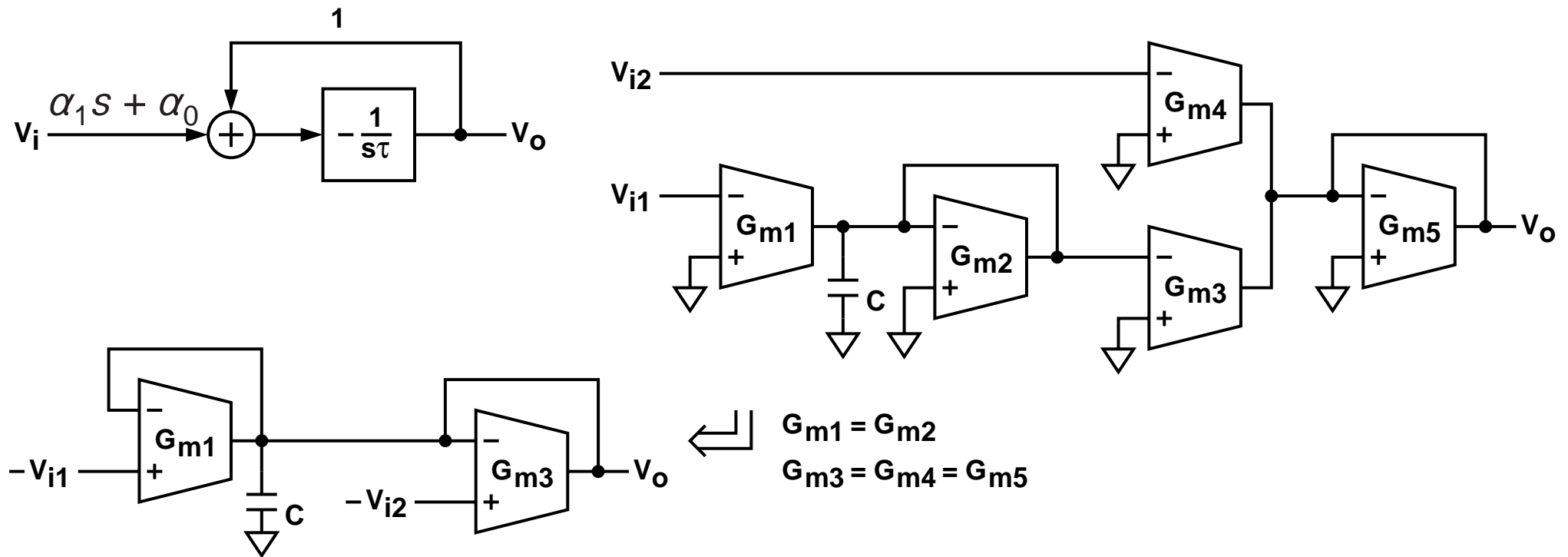
$$G_m(j\omega) = G_m e^{-j\phi}$$

$$\phi = \tan^{-1} \left( \frac{\omega}{\omega_2} \right) \approx \frac{\omega}{\omega_2} \ll 1$$

We have

$$L = \frac{C}{G_m^2} \quad \frac{1}{R_p} \approx -\frac{2G_m^2}{\omega C} \cdot \phi \approx -\frac{2G_m^2}{\omega_2 C} = -\frac{2}{\omega_2 L}$$

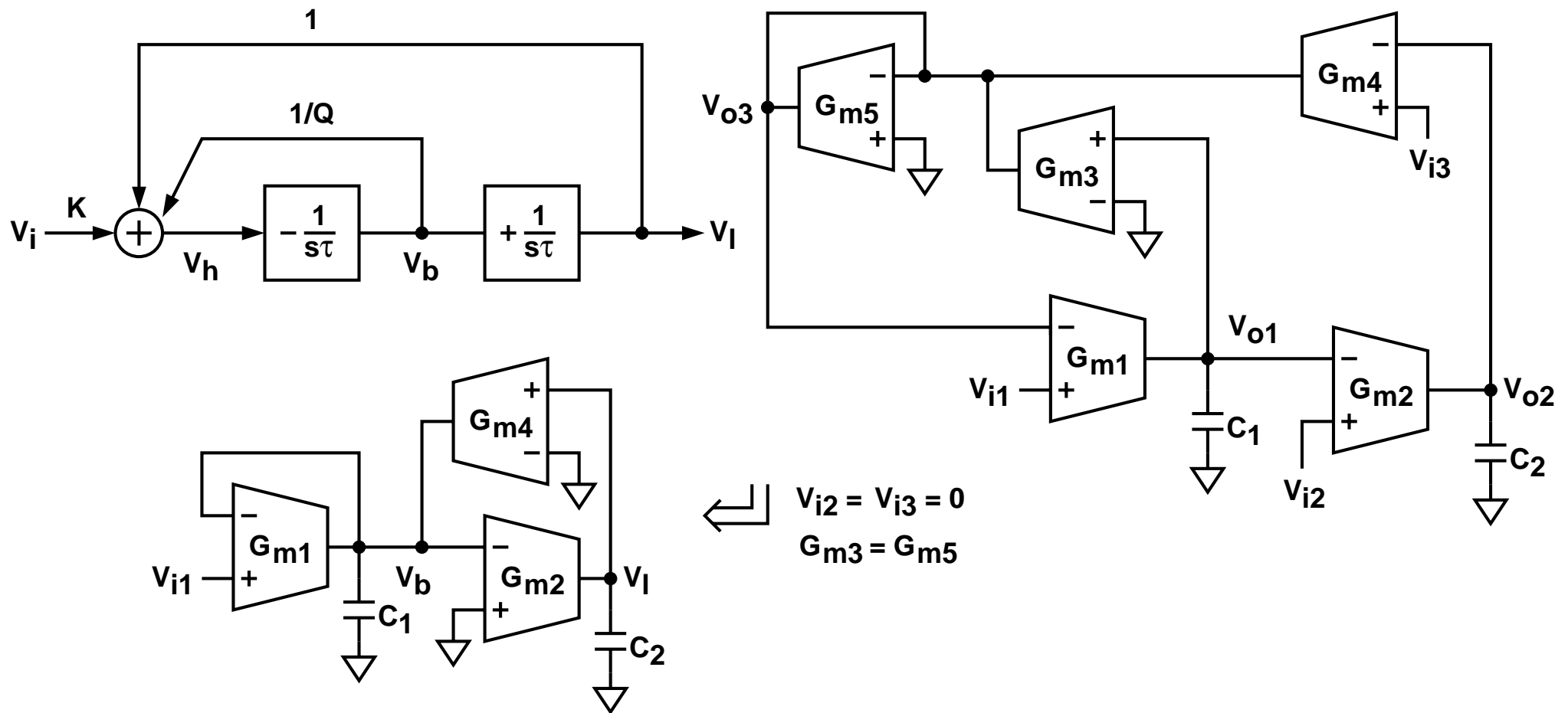
# $G_m$ -C First-Order Filters



$$H(s) = - \left( \frac{G_{m1} V_{i1}}{sC + G_{m2}} \cdot G_{m3} + G_{m4} V_{i2} \right) \cdot \frac{1}{G_{m5}} = - \frac{sCG_{m4} V_{i2} + (G_{m1} G_{m3} V_{i1} + G_{m2} G_{m4} V_{i2})}{(sC + G_{m2}) \cdot G_{m5}}$$

- The output requires another buffer to prevent loading effects.
- Use only grounded capacitors.

# $G_m$ -C Second-Order Filters



$$V_b = \frac{sC_2G_{m1}}{s^2C_1C_2 + sC_2G_{m1} + G_{m2}G_{m4}}$$

$$V_1 = -\frac{G_{m1}G_{m2}}{s^2C_1C_2 + sC_2G_{m1} + G_{m2}G_{m4}}$$

## $G_m$ -C Second-Order Filters

---

The transfer functions are

$$V_{o1} = [1/D(s)] \cdot [sC_2G_{m1}(G_{m5}V_{i1} - G_{m4}V_{i3}) + G_{m1}G_{m2}G_{m4}V_{i2}]$$

$$V_{o2} = [1/D(s)] \cdot [(sC_1G_{m2}G_{m5} + G_{m1}G_{m2}G_{m3})V_{i2}G_{m1}G_{m2}(G_{m4}V_{i3} - G_{m5}V_{i1})]$$

$$V_{o3} = [1/D(s)] \cdot [s^2C_1C_2G_{m4}V_{i3} + s(C_2G_{m1}G_{m3}V_{i1} - C_1G_{m2}G_{m4}V_{i2}) + G_{m1}G_{m2}G_{m4}V_{i1}]$$

$$D(s) = C_1C_2G_{m5} \left( s^2 + s \frac{1}{C_1} \frac{G_{m1}G_{m3}}{G_{m5}} + \frac{G_{m1}G_{m2}G_{m4}}{C_1C_2G_{m5}} \right)$$

If  $V_{i1} = V_{i2} = 0$ , then

$$\frac{V_{o1}}{V_{i3}} = H_{BP}(s) = -\frac{sC_2G_{m1}G_{m4}}{D(s)}$$

$$\frac{V_{o2}}{V_{i3}} = H_{LP}(s) = \frac{G_{m1}G_{m2}G_{m4}}{D(s)}$$

$$\frac{V_{o3}}{V_{i3}} = H_{HP}(s) = \frac{s^2C_1C_2G_{m4}}{D(s)}$$

## $G_m$ -C Second-Order Filters

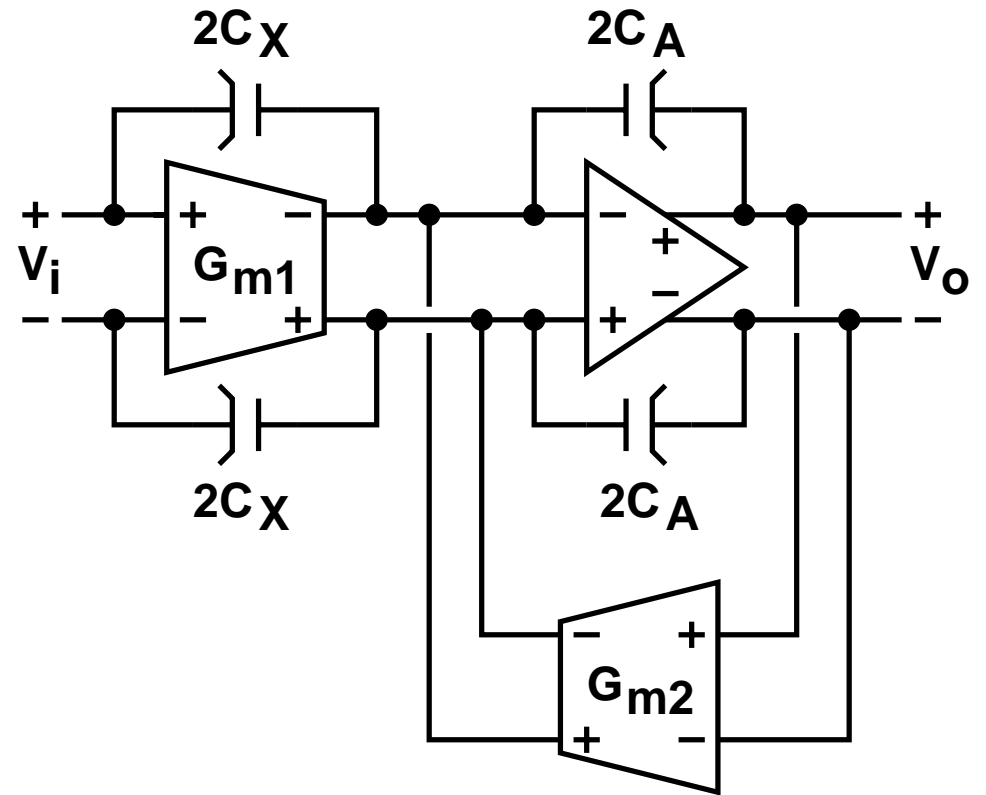
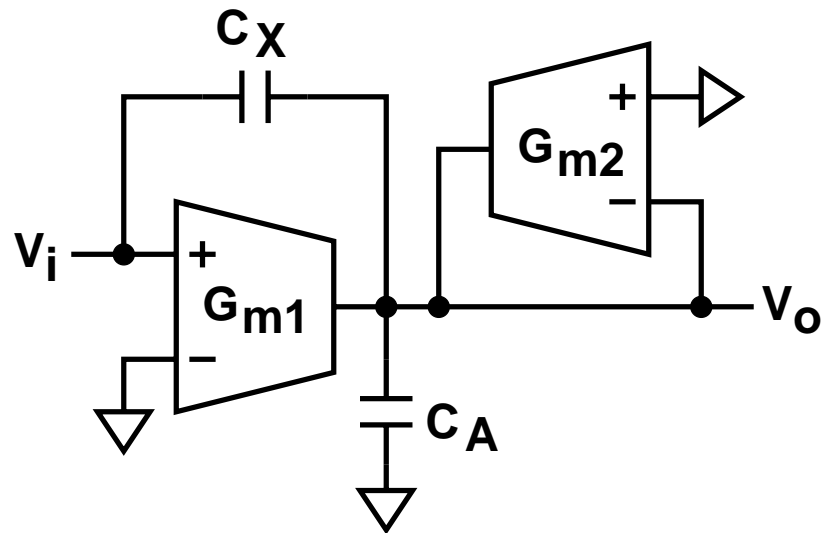
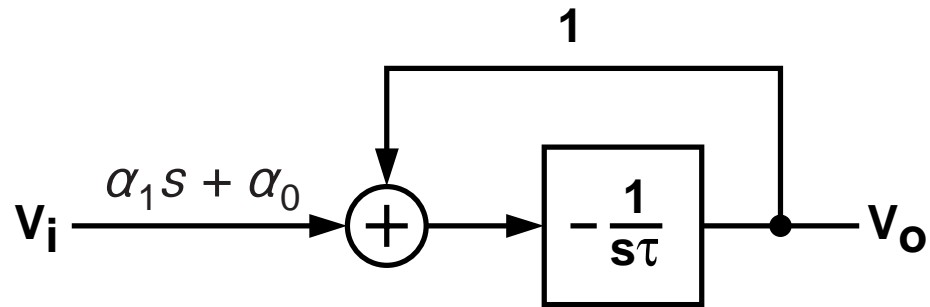
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If  $V_{i1} = V_{i2} = V_{i3} = V_i$ , then

$$\frac{V_{o3}}{V_i} = \frac{s^2 C_1 C_2 G_{m4} + s(C_2 G_{m1} G_{m3} - C_1 G_{m2} G_{m4}) + G_{m1} G_{m2} G_{m4}}{D(s)}$$

- If  $C_2 G_{m1} G_{m3} = C_1 G_{m2} G_{m4}$ , it is a band-reject biquad.
- If  $C_1 G_{m2} G_{m4} = 2C_2 G_{m1} G_{m3}$  and  $G_{m4} = G_{m5}$ , it is an allpass biquad.
- There is one parasitic pole in the biquad.

# $G_m$ -C First-Order Filters Using Miller Integrators



# $G_m$ -C First-Order Filters Using Miller Integrators

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Without the Miller Integrator

$$\frac{V_o}{V_i} = \frac{\alpha_1 s + \alpha_0}{s + \omega_o} = \frac{s \left( \frac{C_X}{C_A + C_X} \right) + \left( \frac{G_{m1}}{C_A + C_X} \right)}{s + \left( \frac{G_{m2}}{C_A + C_X} \right)}$$

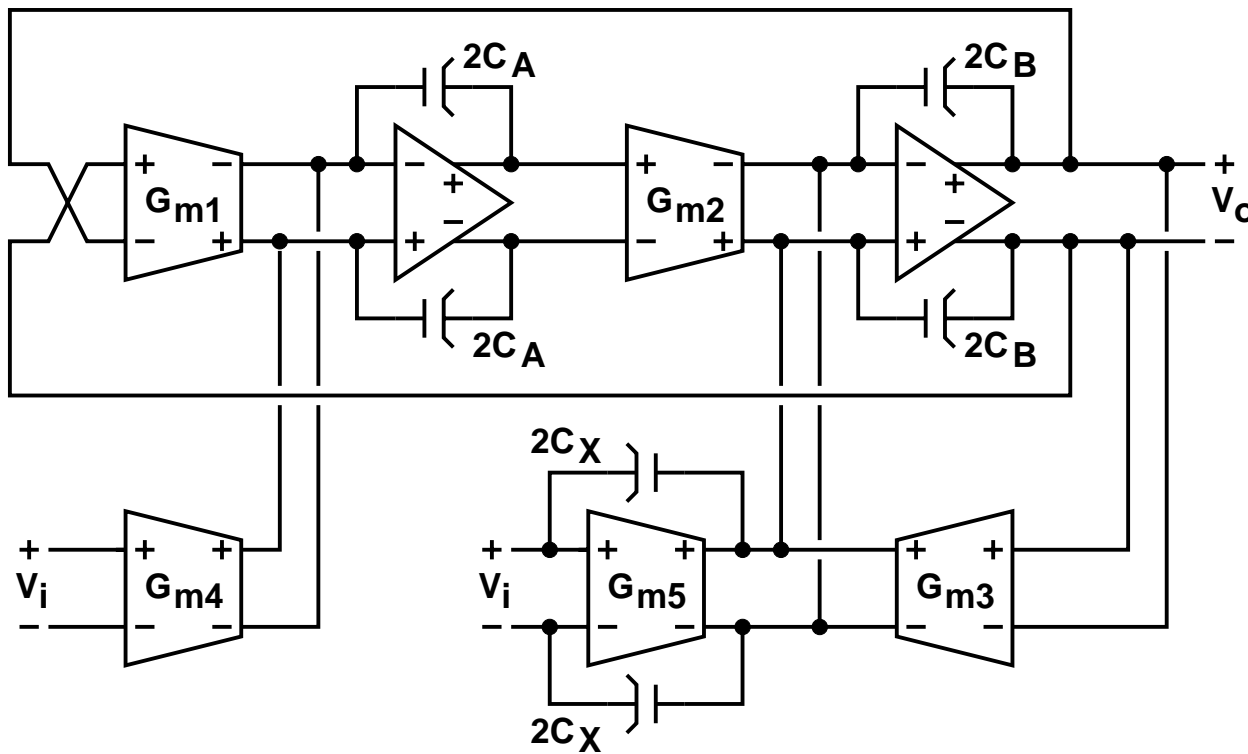
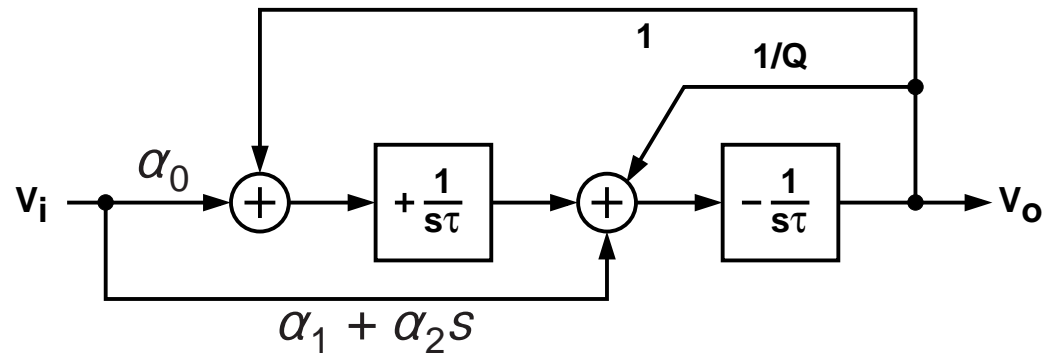
$$G_{m1} = \alpha_0(C_A + C_X) \quad G_{m2} = \omega_o(C_A + C_X) \quad C_X = C_A \frac{\alpha_1}{1 - \alpha_1} \quad \text{where } 0 \leq \alpha_1 < 1$$

With the Miller Integrator

$$\frac{V_o}{V_i} = \frac{\alpha_1 s + \alpha_0}{s + \omega_o} = \frac{s \left( \frac{C_X}{C_A} \right) + \left( \frac{G_{m1}}{C_A} \right)}{s + \left( \frac{G_{m2}}{C_A} \right)}$$

- The use of feed-in capacitors can simplify design, but requires inputs of low source impedance.

# $G_m$ -C Second-Order Filters Using Miller Integrators



# $G_m$ -C Second-Order Filters Using Miller Integrators

---

The transfer function is

$$\frac{V_o}{V_i} = \frac{\alpha_2 s^2 + \alpha_1 s + \alpha_0}{s^2 + \left(\frac{\omega_p}{Q}\right) s + \omega_p^2} = \frac{s^2 \left(\frac{C_X}{C_B}\right) + s \left(\frac{G_{m5}}{C_B}\right) + \left(\frac{G_{m2}G_{m4}}{C_A C_B}\right)}{s^2 + s \left(\frac{G_{m3}}{C_B}\right) + \left(\frac{G_{m1}G_{m2}}{C_A C_B}\right)}$$

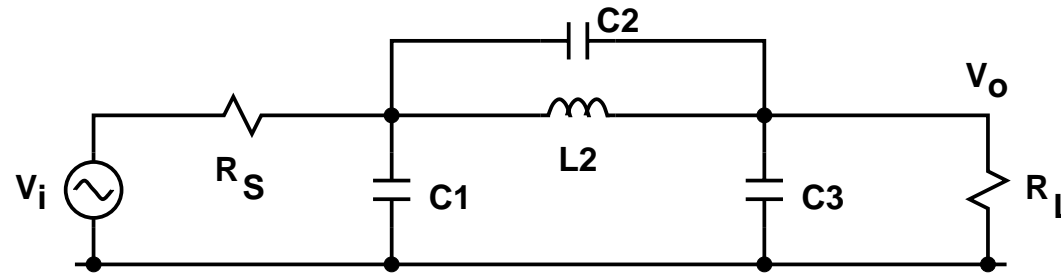
Thus

$$C_X = \alpha_2 C_B$$

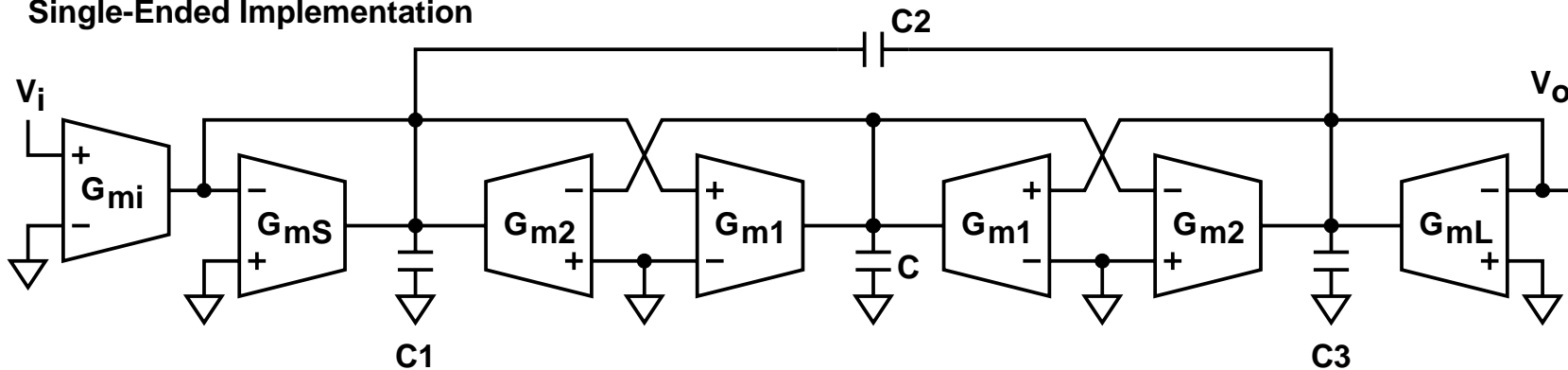
and

$$G_{m1} = \omega_p C_A \quad G_{m2} = \omega_p C_B \quad G_{m3} = \frac{\omega_p C_B}{Q} \quad G_{m4} = \frac{\alpha_0 C_A}{\omega_p} \quad G_{m5} = \alpha_1 C_B$$

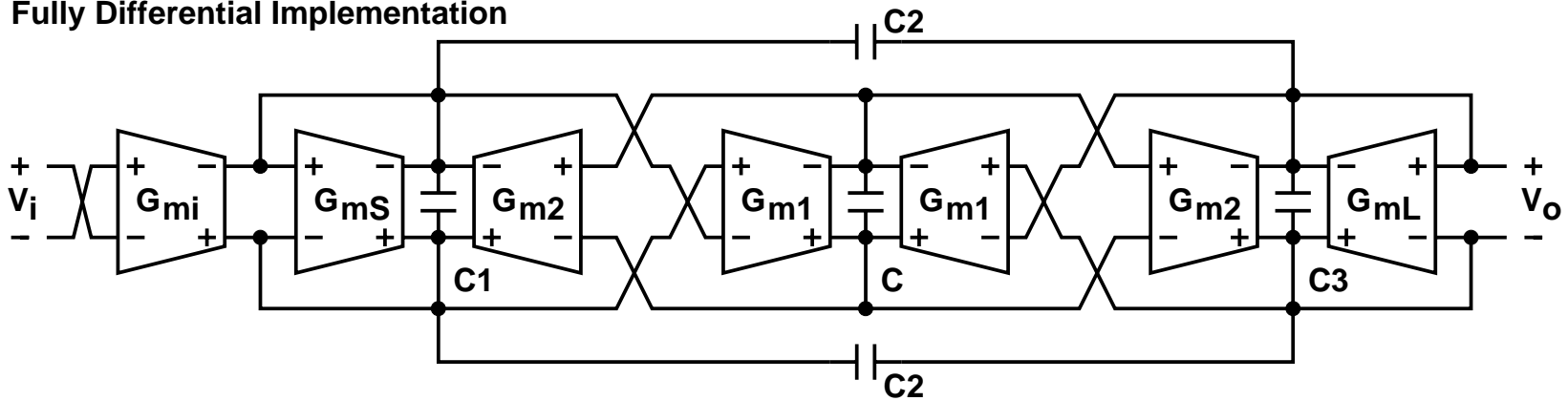
# Ladder Filter Using Simulated Gytrators



Single-Ended Implementation



Fully Differential Implementation

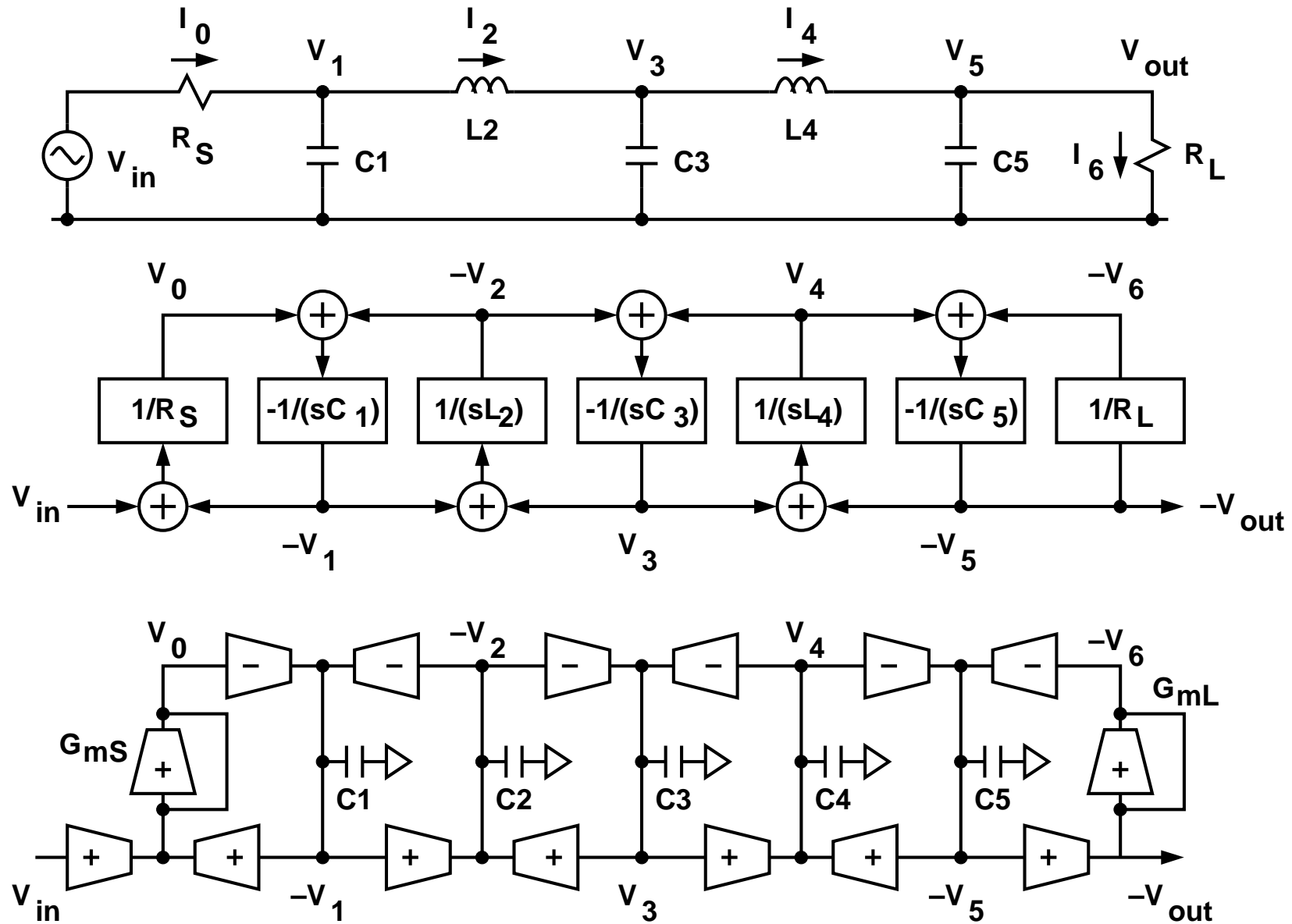


# Ladder Filter Using Simulated Gytrators

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- Inductors are replaced with  $G_m$ -C gytrators.
- Floating capacitors are required.
- Finite  $g_o$  of the transconductors results in lossy inductors and capacitor, i.e., Q degradation; while phase shift causes Q enhancement.
- The Q-control automatic tuning circuits may be required.

# Ladder Filter Using Signal-Flow Graph



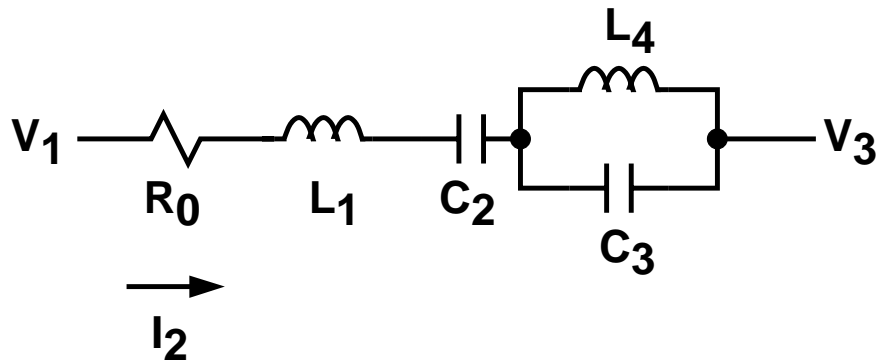
# Ladder Filter Using Signal-Flow Graph

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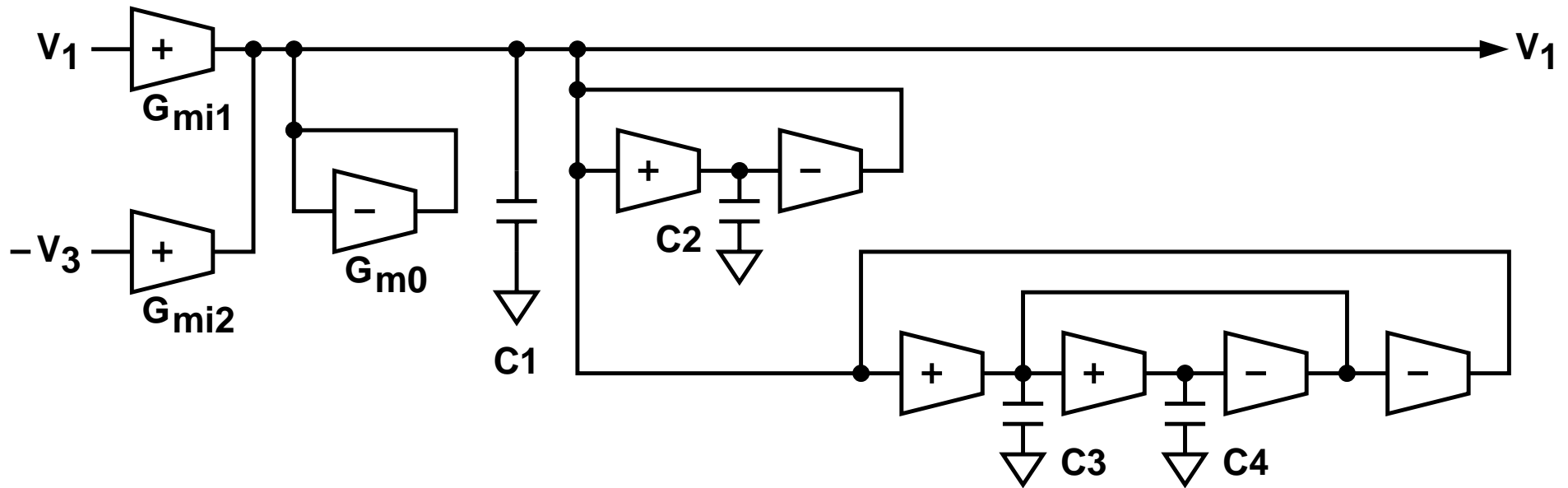
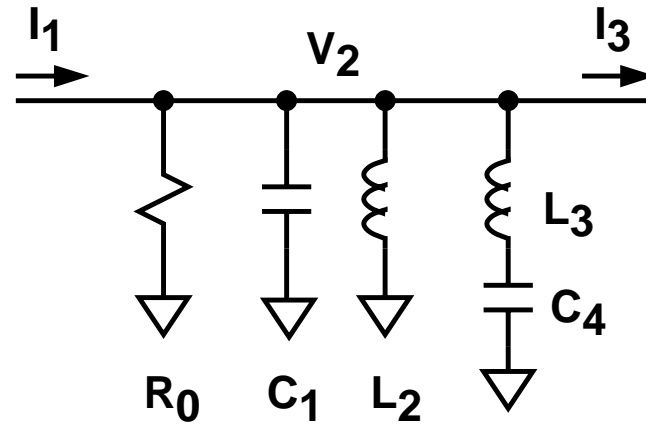
- Floating capacitors are not necessary.
- Finite  $g_o$  of the transconductors results in lossy inductors and capacitor, i.e., Q degradation; while phase shift causes Q enhancement.
- Signal-level scaling is possible.

# $G_m$ -C Simulation of Ladder Branches (I)

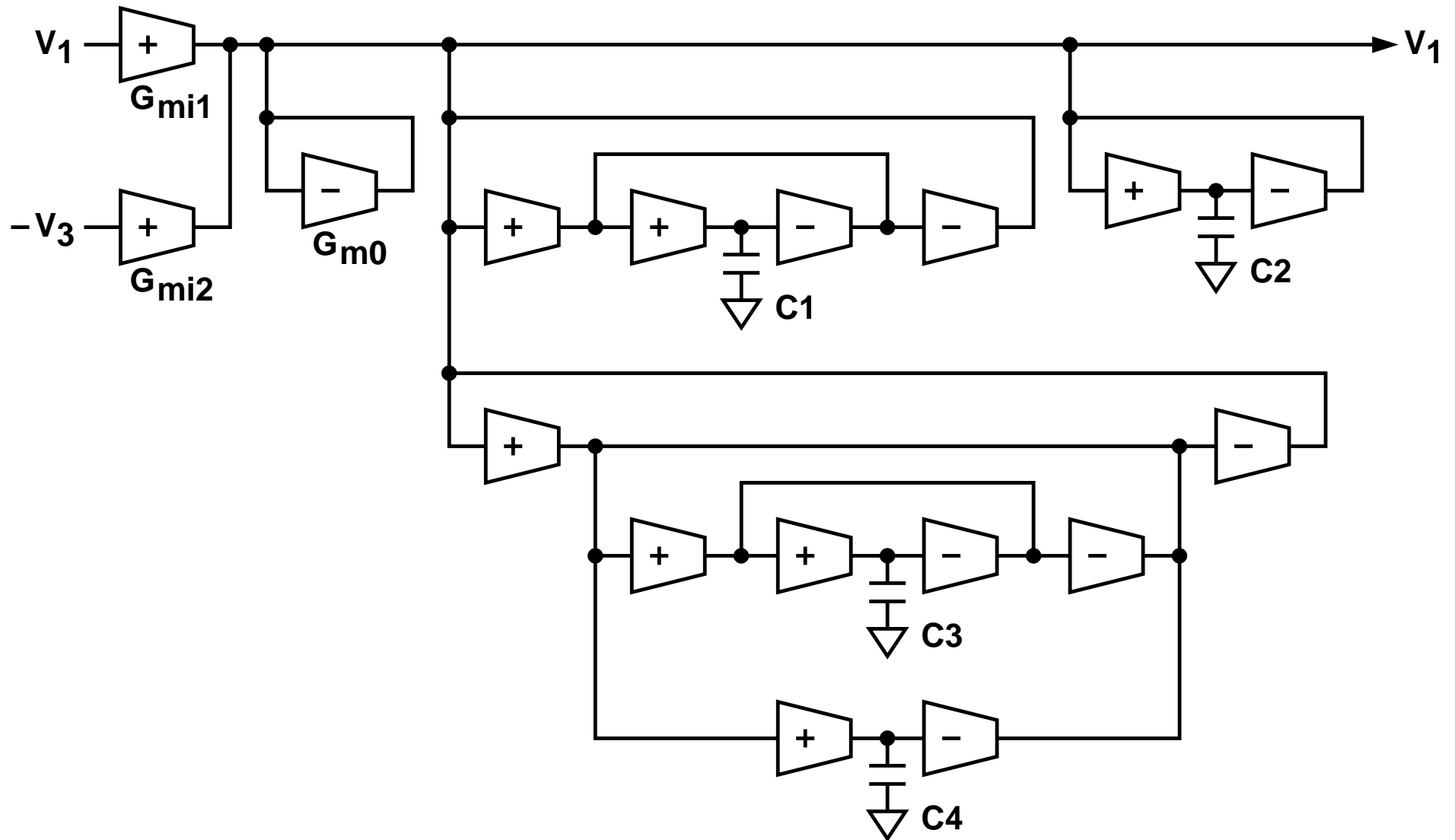
Series Branch



Shunt Branch



# $G_m$ -C Simulation of Ladder Branches (II)



## $G_m$ -C Simulation of Ladder Branches

---

The branch characteristics are

$$I_2 = (V_1 - V_3) \cdot Y(s) = (V_1 - V_3) \cdot \frac{1}{R_0 + sL_1 + \frac{1}{sC_2} + \frac{1}{sC_3 + \frac{1}{sL_4}}}$$

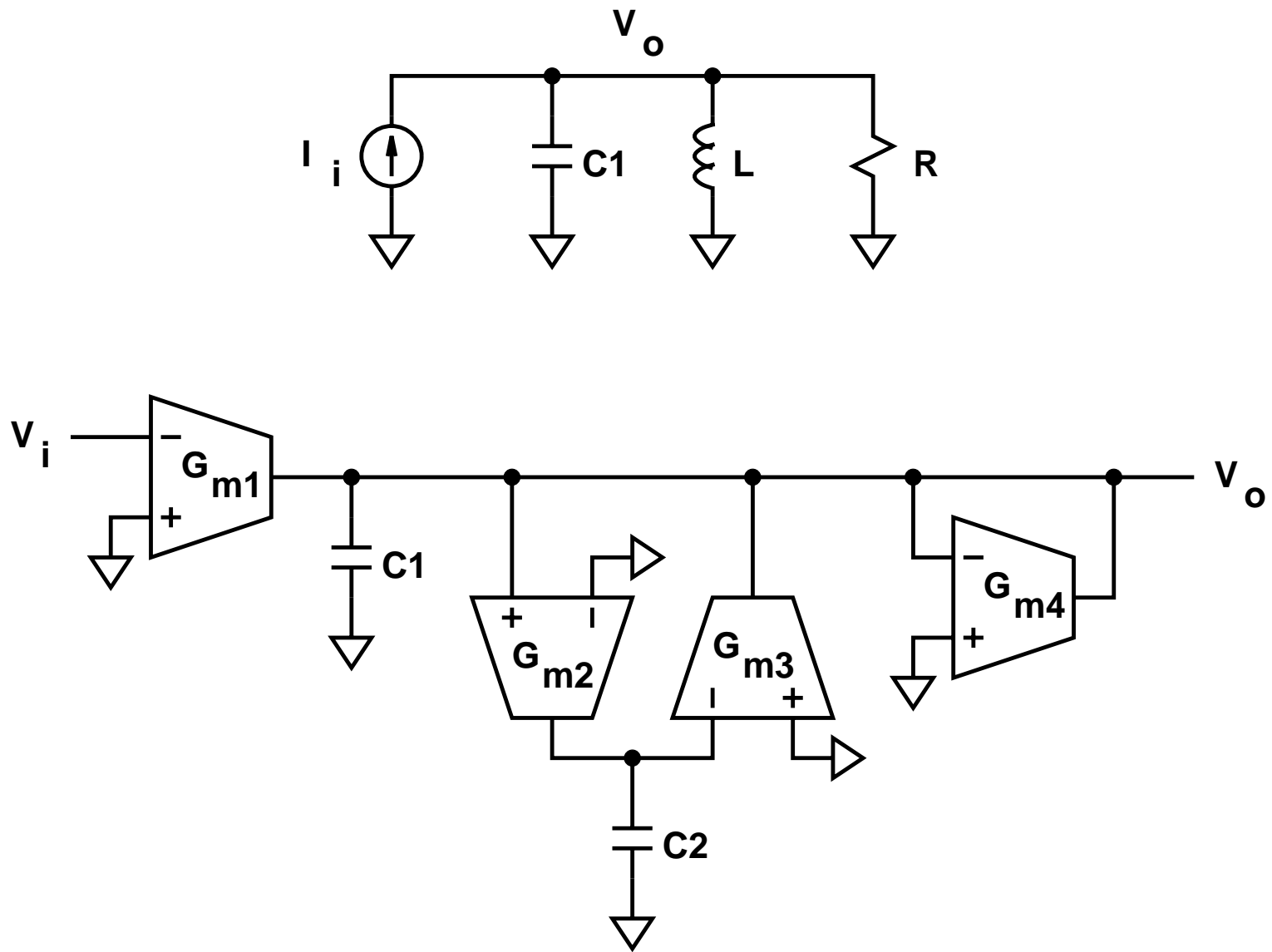
$$V_2 = (I_1 - I_3) \cdot Z(s) = (I_1 - I_3) \cdot \frac{1}{G_0 + sC_1 + \frac{1}{sL_2} + \frac{1}{sL_3 + \frac{1}{sC_4}}}$$

The  $G_m$ -C circuit's transfer function is

$$V_2 = (G_{mi1} \cdot V_1 - G_{mi2} \cdot V_3) \cdot \frac{1}{G_{m0} + sC_1 + \frac{1}{sC_2} + \frac{1}{sC_3 + \frac{1}{sC_4}}}$$

- Method 2 usually uses more transconductors than method 1, but may have advantages in terms of sensitivity to and compensation for parasitic effects.
- For better matching, use identical transconductors whenever possible.

# $G_m$ -C Resonators



# $G_m$ -C Resonators

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- The inductor  $L$  is simulated by  $G_{m2}$ ,  $G_{m3}$ , and  $C_2$ . The resistor  $R$  is simulated by  $G_{m4}$ .
- The resonant frequency and the quality factor are

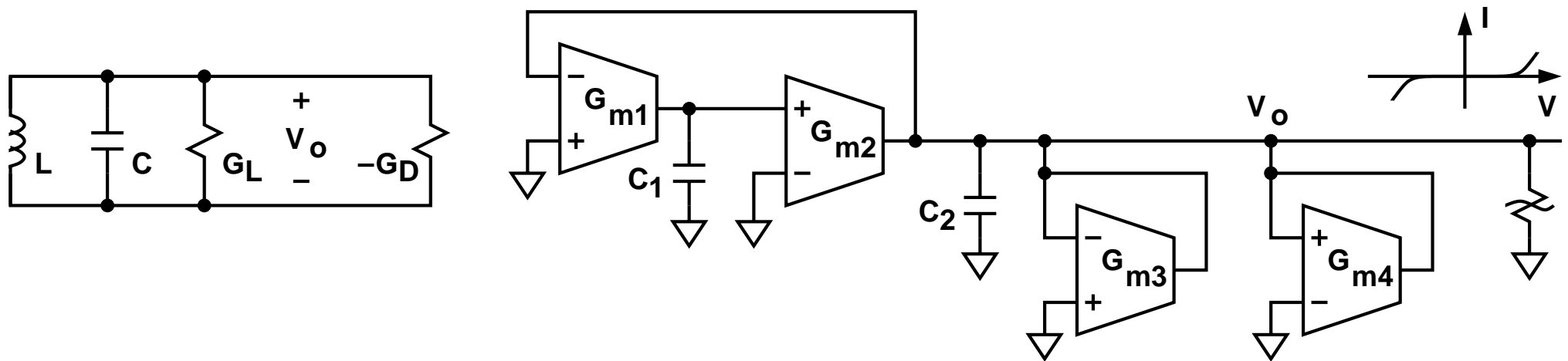
$$\omega_o = \sqrt{\frac{1}{LC_1}} = \sqrt{\frac{G_{m2}G_{m3}}{C_1C_2}} \quad Q = \omega_o RC_1 = \sqrt{\frac{C_1}{C_2}} \times \sqrt{\frac{G_{m2}G_{m3}}{G_{m4}^2}}$$

The voltage gain at the resonant frequency is

$$A_{vo} = \frac{V_o}{V_i} = G_{m1}R = \frac{G_{m1}}{G_{m4}}$$

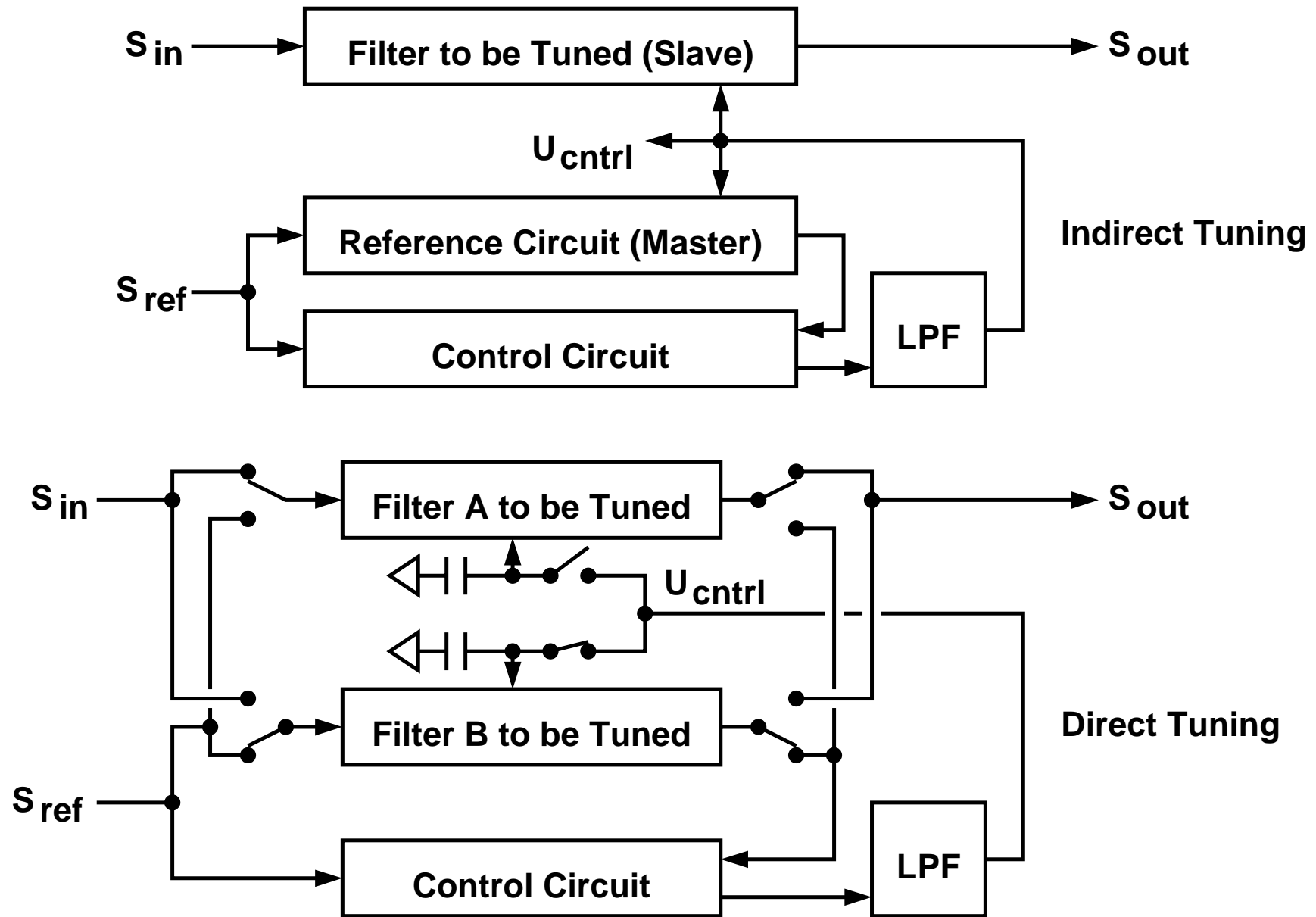
- Reference: Silva-Martinez, et al., JSSC 12/92, pp. 1843–1853.

## $G_m$ -C Quadrature Oscillators

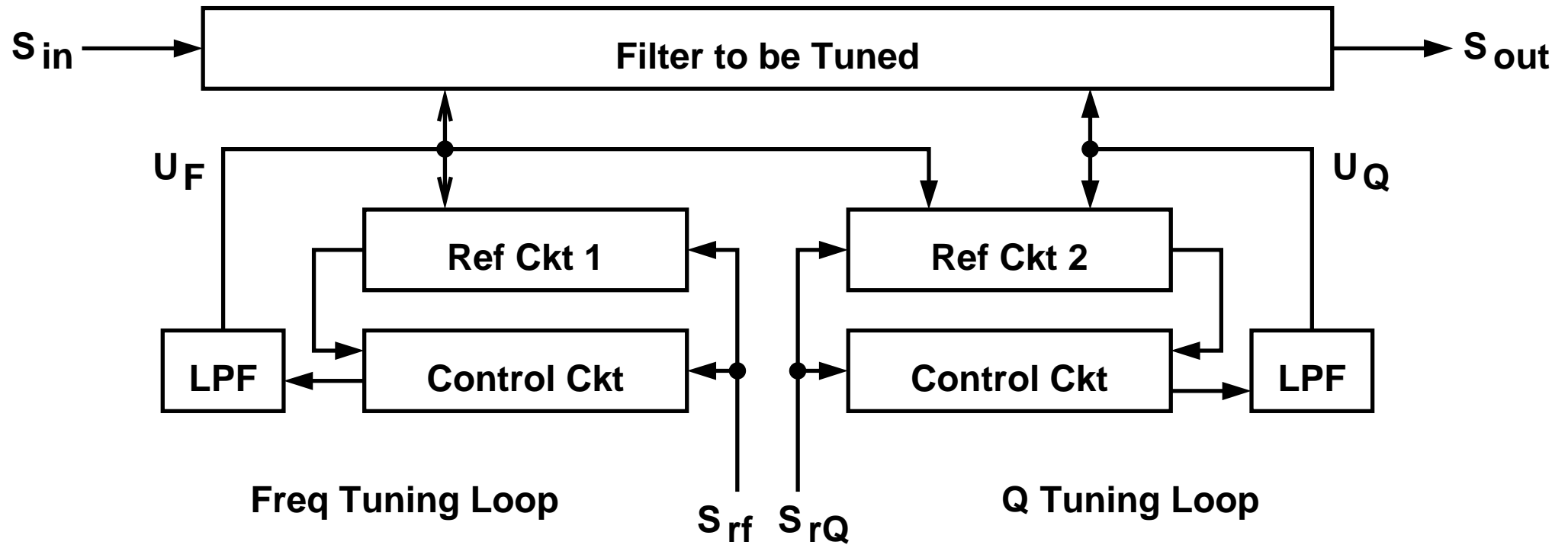


- The combination of  $G_{m1}$ ,  $G_{m2}$  and  $C_1$  simulates an inductor.
- The oscillation frequency is  $\omega_o = \sqrt{G_{m1}G_{m2}/(C_1C_2)}$ .
- The oscillation condition is  $G_{m4} = G_{m3}$ . In many cases,  $G_{m3}$  and  $G_{m4}$  are not required.
- The nonlinear resistor is used to control the output amplitude.
- Reference: Rodriguez-Vazquez, Transactions on Circuits and Systems, 2/90, pp. 198–211.

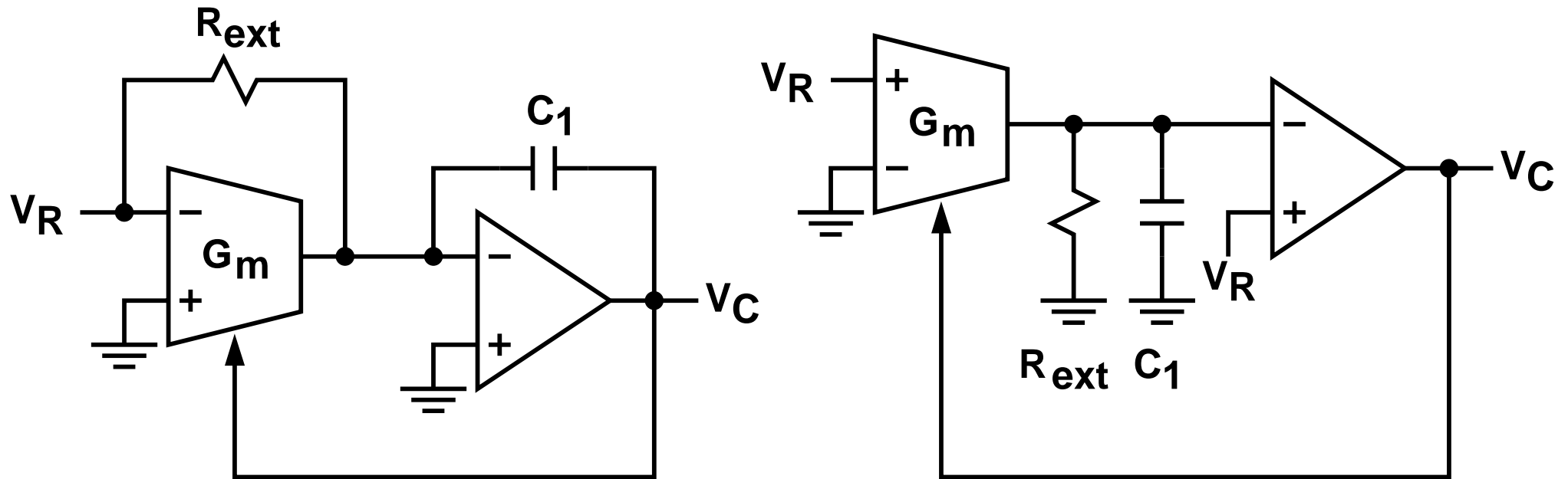
# On-Chip Tuning Strategies



# Separate Frequency and Q Control



# $G_m$ Tuning

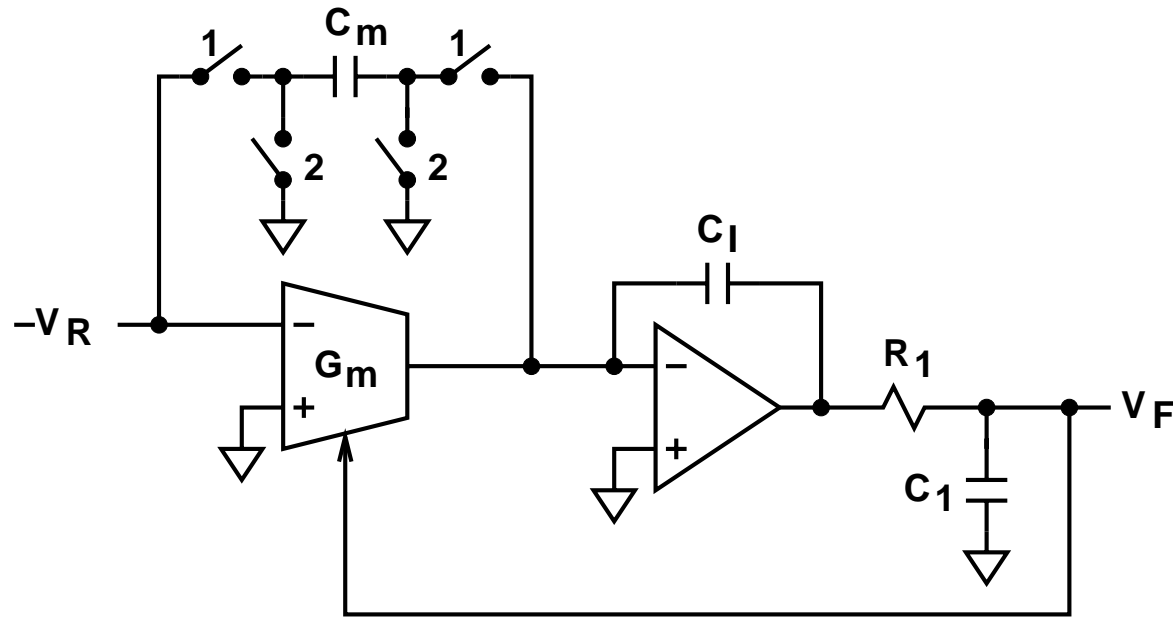


- $V_C$  is automatically adjusted so that

$$G_m = \frac{1}{R_{ext}}$$

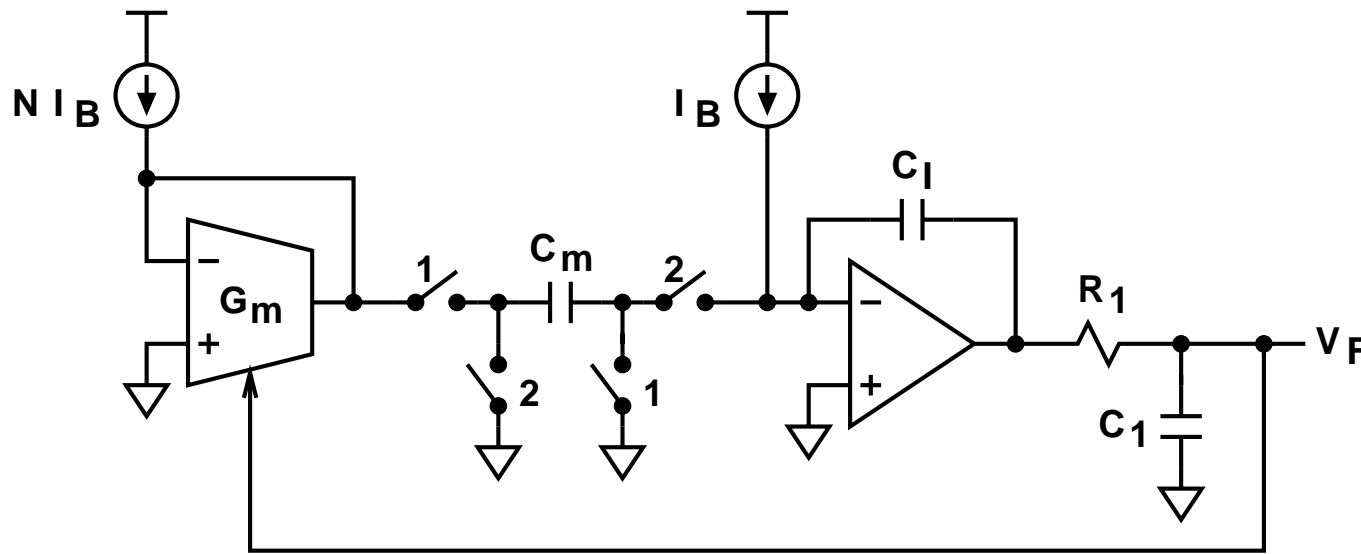
- $C_1$  is an integrating capacitor used to maintain loop stability.

# Frequency Tuning Using Switched Capacitors



$$G_m = \frac{1}{R_{eq}} = f_s C_m$$

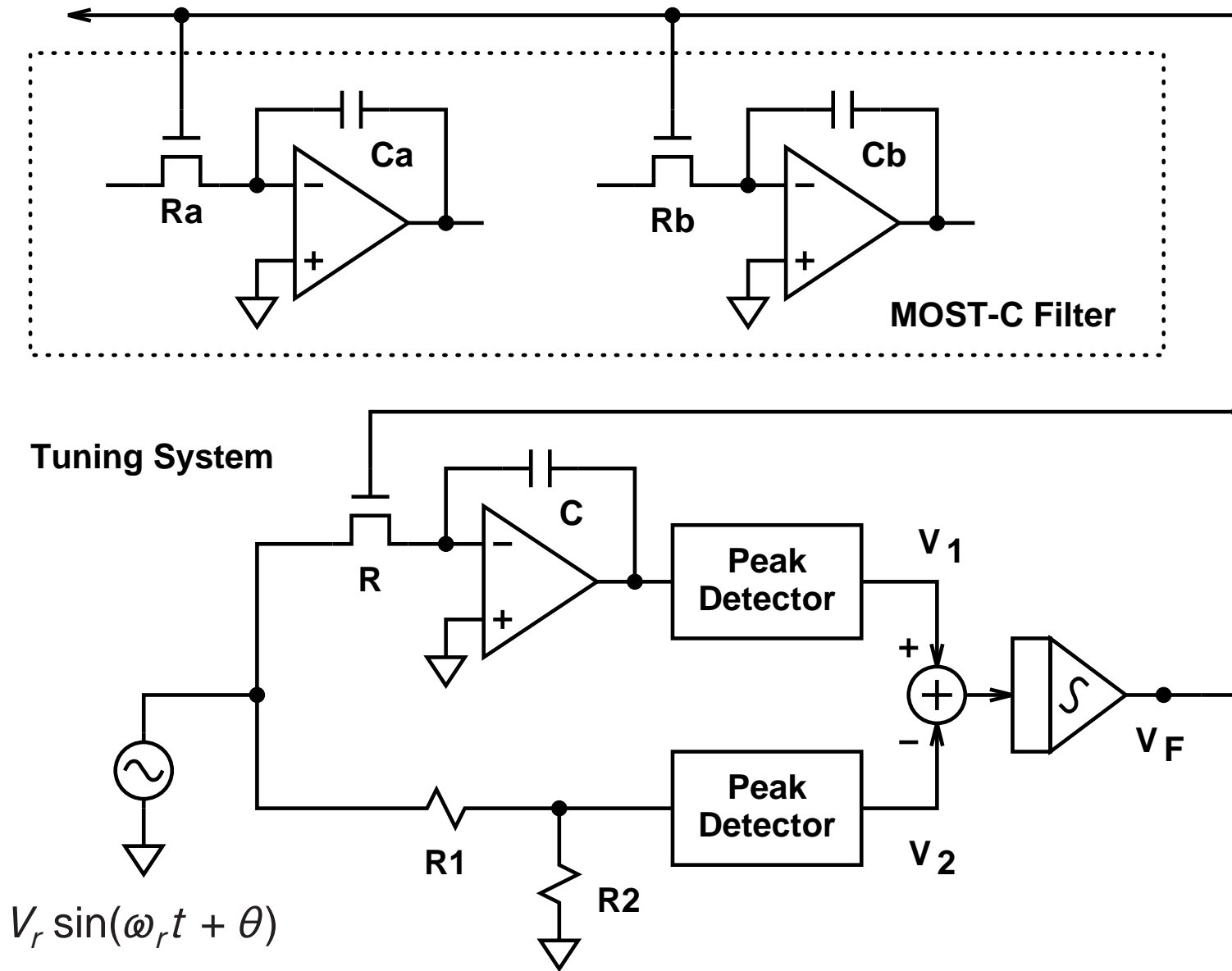
$$\Rightarrow \frac{G_m}{C_m} = f_s$$



$$N I_B \cdot \frac{1}{G_m} \cdot \frac{1}{R_{eq}} = I_B$$

$$\Rightarrow \frac{G_m}{C_m} = N f_s$$

# Frequency Tuning Using Response Detection



# Frequency Tuning Using Response Detection

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For this amplitude-response detection scheme

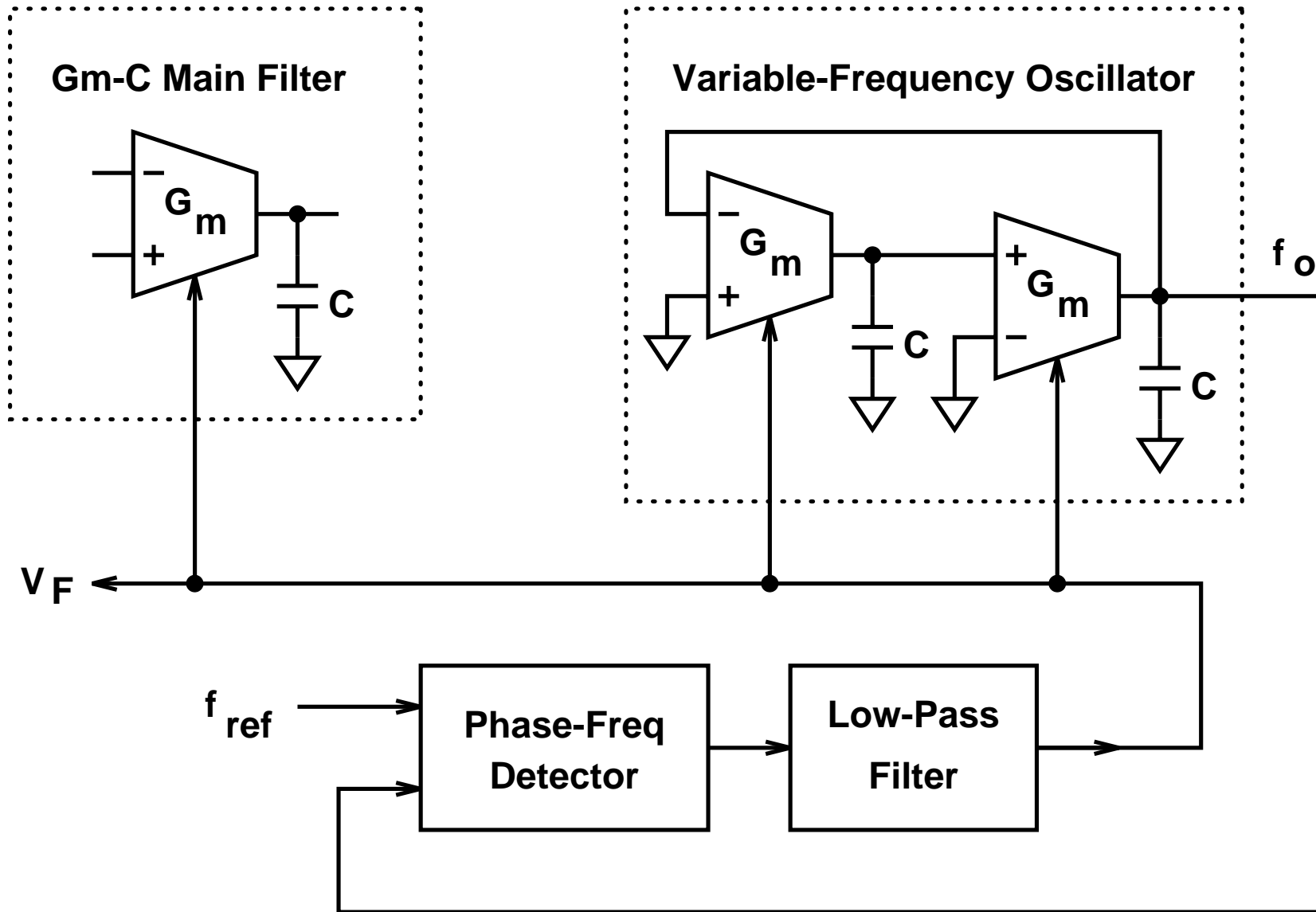
$$V_1 = V_r \cdot \frac{1}{\omega_r RC} \quad V_2 = V_r \cdot \frac{R_2}{R_1 + R_2}$$

The feedback adjusts  $V_F$  so that  $V_1 = V_2$ , thus

$$R \cdot C = \frac{1}{\omega_r} \cdot \left( 1 + \frac{R_1}{R_2} \right)$$

- The above tuning system is a magnitude locked loop (MLL).
- Usually use  $\omega_r RC \gg 1$  to place  $\omega_r$  in the filter stopband.
- Phase-response detection scheme can also be used.
- The reference circuit can be any filter.

# Frequency Tuning Using Phase-Locked Loop



# Frequency Tuning Using Phase-Locked Loop

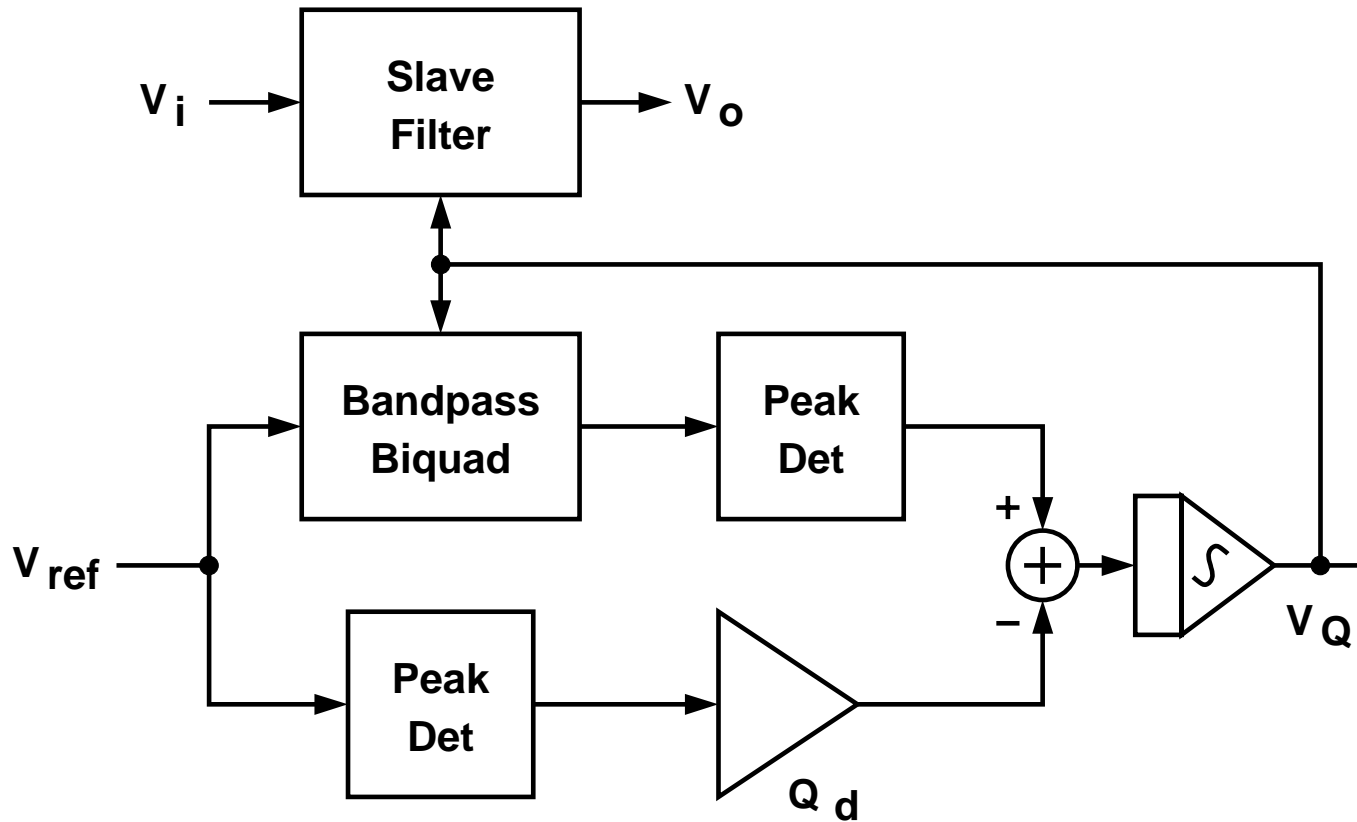
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The phase-locked loop (PLL) forces

$$f_{\text{ref}} = f_o = \frac{1}{2\pi} \cdot \frac{G_m}{C} \quad \Rightarrow \quad \frac{G_m}{C} = 2\pi f_{\text{ref}}$$

- For best matching between the reference VFO and the main filter, it is best to choose  $f_{\text{ref}}$  at the upper passband edge. However, the reference signal may leak into the main filter's output.
- If  $f_{\text{ref}}$  moves away from the upper passband edge, the matching will be poorer, but an improved immunity to the reference signal results.
- If the VFO is sensitive to supply variation, any power-supply noise can inject jitter into  $V_F$ .

# Q-Factor Tuning Using MLL

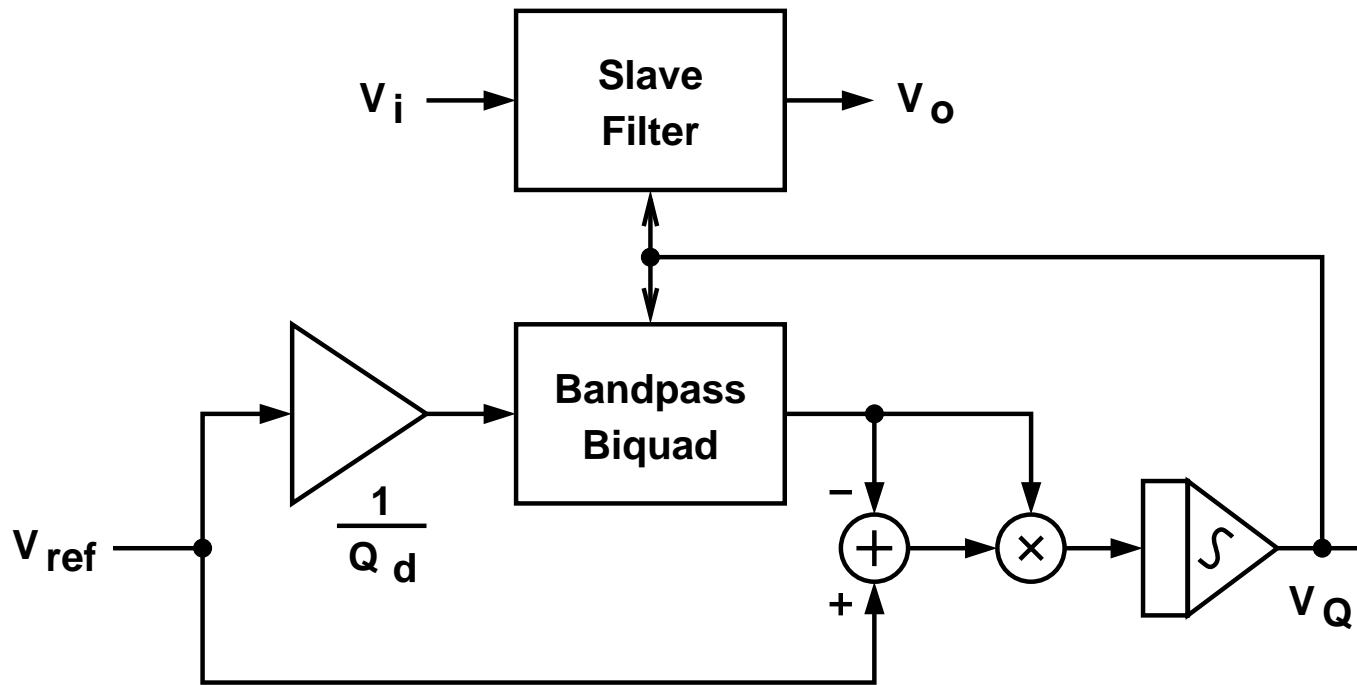


$$H_{bq}(s) = \frac{\omega_p s}{s^2 + \frac{\omega_p}{Q_p} s + \omega_p^2}$$

$$V_{\text{ref}} = A \sin \omega_r t$$

- At  $s = j\omega_r = j\omega_p$ , the MLL forces  $H_{bq}(j\omega_p) = Q_p = Q_d$ .
- For high  $Q$  biquad, mismatch between  $\omega_r$  and  $\omega_p$  results in large Q-tuning error.
- Distortion in  $V_{\text{ref}}$  can also cause error.

# Q-Factor Tuning Using LMS



$$H_{bq}(s) = \frac{\omega_p s}{s^2 + \frac{\omega_p}{Q_p} s + \omega_p^2}$$

$$V_{\text{ref}} = A \sin \omega_r t$$

$$\frac{dV_Q(t)}{dt} = \mu \cdot [V_{\text{ref}}(t) - V_{bq}(t)] \cdot V_{bq}(t)$$

The modified continuous-time least-mean-squares (LMS) algorithm will force

$$\overline{[V_{\text{ref}}(t) - V_{bq}(t)] \cdot V_{bq}(t)} = \overline{V_{\text{ref}}(t) \cdot V_{bq}(t) - V_{bq}^2(t)} = 0$$

# Q-Factor Tuning Using LMS

---

If  $\omega_r = \omega_p$ ,

$$V_{bq}(t) = \frac{Q_p}{Q_d} \cdot A \sin \omega_r t = B \cdot \sin \omega_r t \quad B = \frac{Q_p}{Q_d} \cdot A$$

$$\text{LMS} \Rightarrow \frac{A \cdot B}{2} = \frac{B \cdot B}{2} \Rightarrow A = B \Rightarrow Q_p = Q_d$$

If  $\omega_r \neq \omega_p$ ,

$$V_{bq}(t) = \frac{Q_p}{Q_d} \cos \phi \cdot A \sin (\omega_r t + \phi) = B \cdot \sin (\omega_r t + \phi) \quad B = \frac{Q_p}{Q_d} \cos \phi \cdot A$$

$$\text{LMS} \Rightarrow \frac{A \cdot B \cdot \cos \phi}{2} = \frac{B \cdot B}{2} \Rightarrow A \cos \phi = B \Rightarrow Q_p = Q_d$$

- Insensitive to mismatch between  $\omega_r$  and  $\omega_p$ .

# Q-Factor Tuning Using LMS

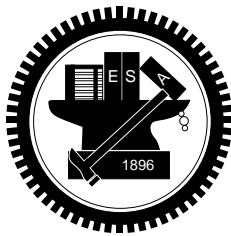
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- Require no peak detector.
- The scheme is also insensitive to  $V_{\text{ref}}$  waveform shape.
- Square wave can be used for  $V_{\text{ref}}(t)$ .
- Reference: J.-M. Stevenson, et al., *An Accurate Quality Factor Tuning Scheme for IF and High-Q Continuous-Time Filters*, JSSC 12/1998, pp. 1970–1978.

# Switched-Capacitor Filters

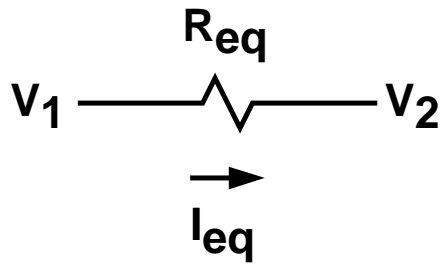
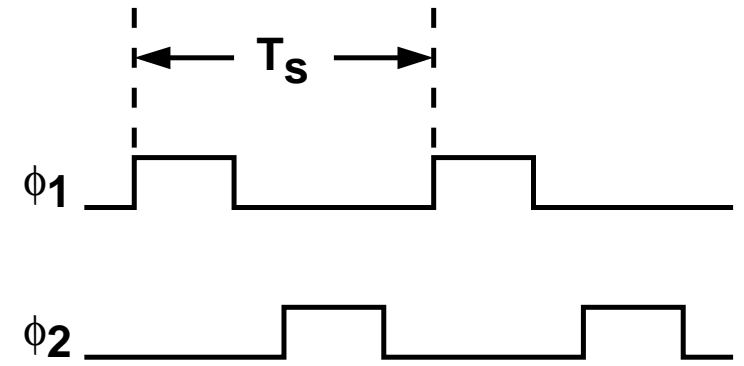
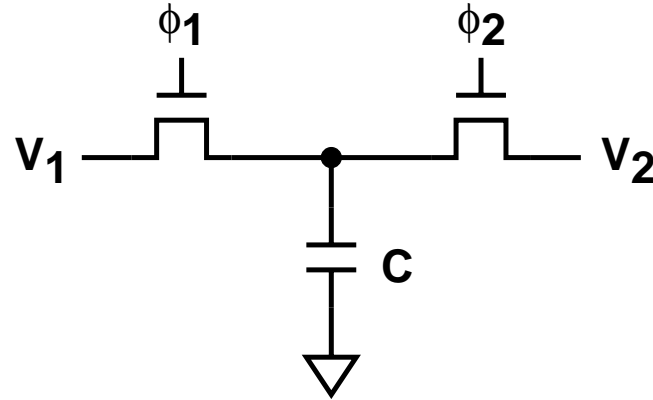
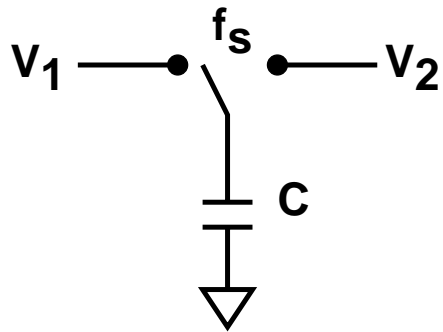
Jieh-Tsorng Wu

October 23, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Switched-Capacitor Equivalent Resistor

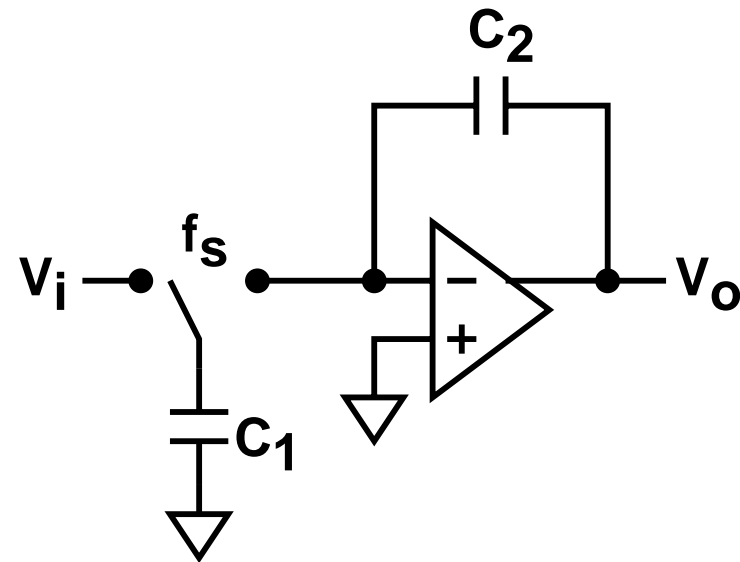
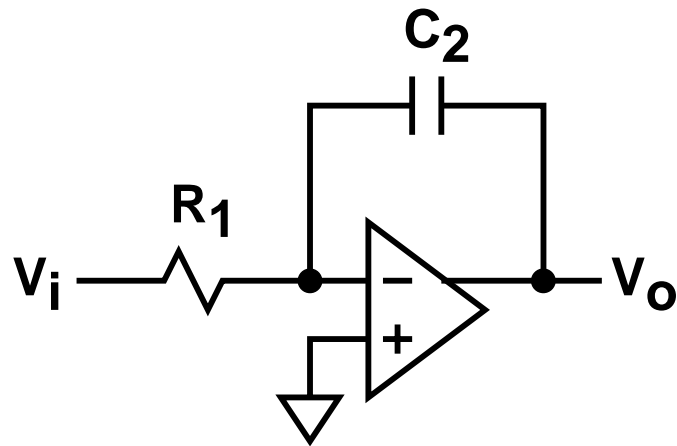


$$I_{eq} = \overline{\left(\frac{\Delta Q}{\Delta t}\right)} = \frac{C \cdot V_1 - C \cdot V_2}{T_s} = C \cdot (V_1 - V_2) \cdot f_s$$

$$T_s = \frac{1}{f_s}$$

$$G_{eq} = \frac{1}{R_{eq}} = \frac{I_{eq}}{V_1 - V_2} = C \cdot f_s$$

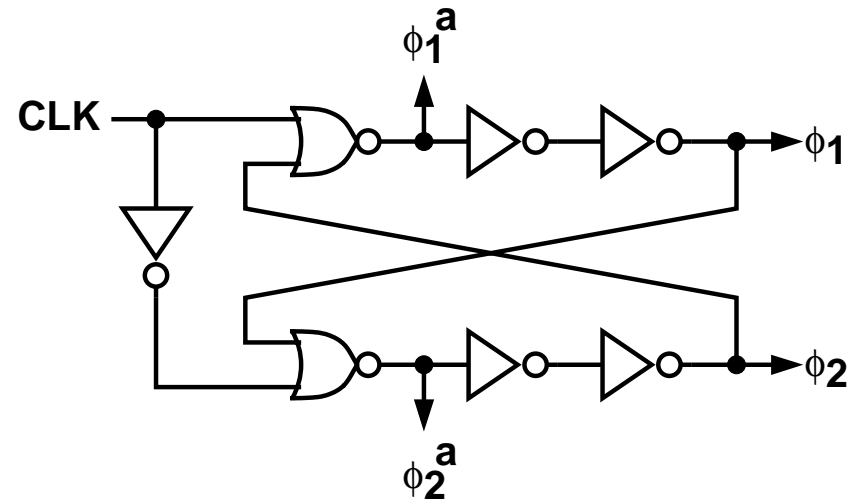
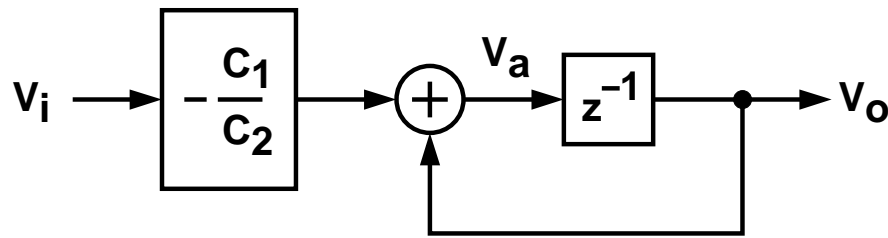
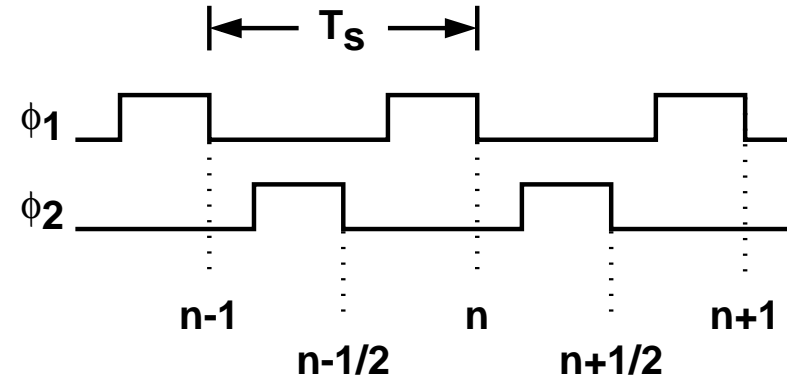
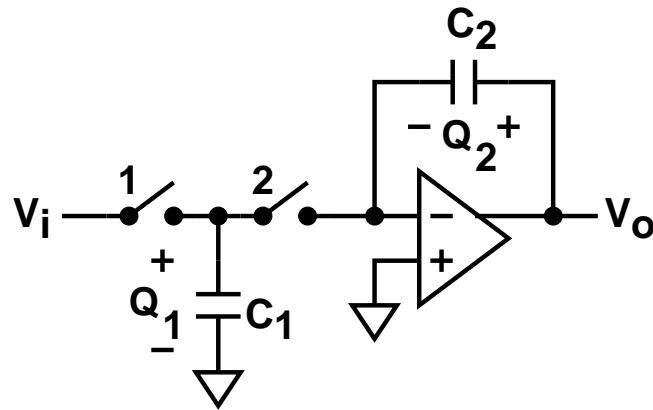
# Switched-Capacitor Integrators



$$\frac{V_o}{V_i} = -\frac{1}{sR_1C_2} = -\frac{1}{s} \cdot \frac{G_{eq1}}{C_2} = -\frac{1}{s} \cdot \left( f_s \cdot \frac{C_1}{C_2} \right)$$

- Consist of analog switches, capacitors and opamps.
- Discrete-time (or sampled-data) analog filters.
- Time constant is determined by capacitance ratio and switching frequency.

# SC Integrator Analysis



$$\frac{V_o(z)}{V_i(z)} = -\frac{C_1}{C_2} \times \frac{z^{-1}}{1 - z^{-1}}$$

## SC Integrator Analysis

---

At cycle  $n$ , i.e.,  $t = nT_s$ , we have  $Q_1(n) = C_1V_i(n)$  and  $Q_2(n) = C_2V_o(n)$

At cycle  $n + 1/2$ , i.e.,  $t = (n + 1/2)T_s$ ,

$$Q_1(n + 1/2) = 0 \quad Q_2(n + 1/2) = Q_2(n) - Q_1(n) = C_2V_o(n) - C_1V_i(n)$$

At cycle  $n + 1$ , i.e.,  $t = (n + 1)T_s$ ,

$$Q_1(n + 1) = C_1V_i(n + 1) \quad Q_2(n + 1) = C_2V_o(n + 1) = Q_2(n + 1/2) = C_2V_o(n) - C_1V_i(n)$$

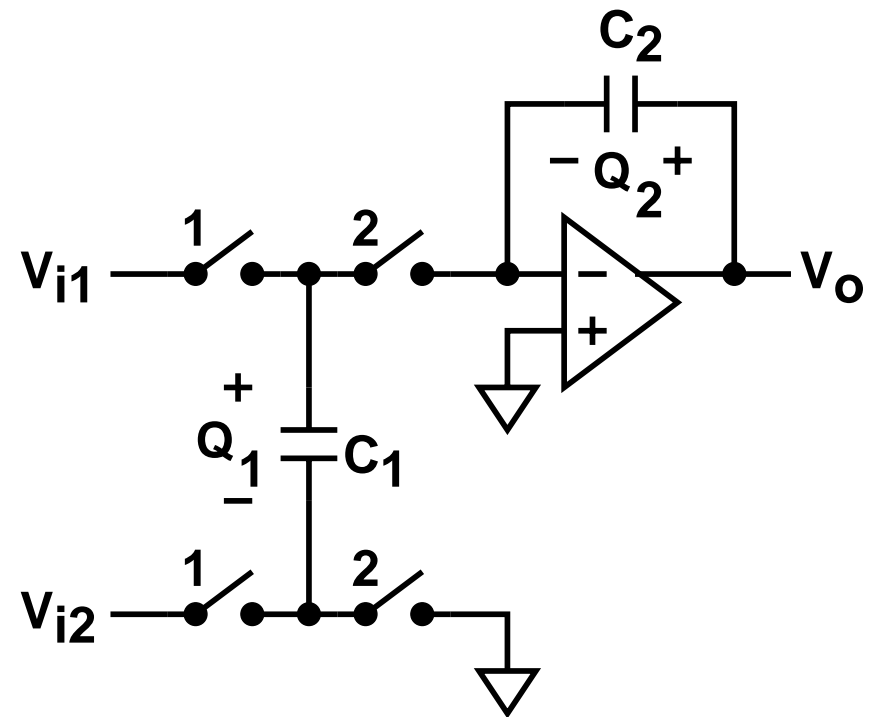
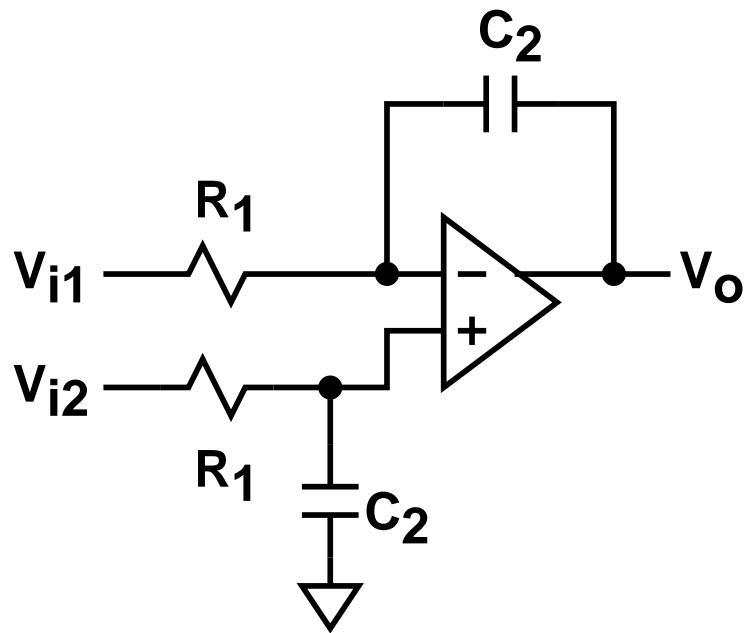
Thus, the time-domain difference equation is

$$C_2V_o(n + 1) = C_2V_o(n) - C_1V_i(n)$$

In the z-domain

$$zC_2V_o(z) = C_2V_o(z) - C_1V_i(z) \quad \Rightarrow \quad \frac{V_o(z)}{V_i(z)} = -\frac{C_1}{C_2} \times \frac{1}{z - 1} = -\frac{C_1}{C_2} \times \frac{z^{-1}}{1 - z^{-1}}$$

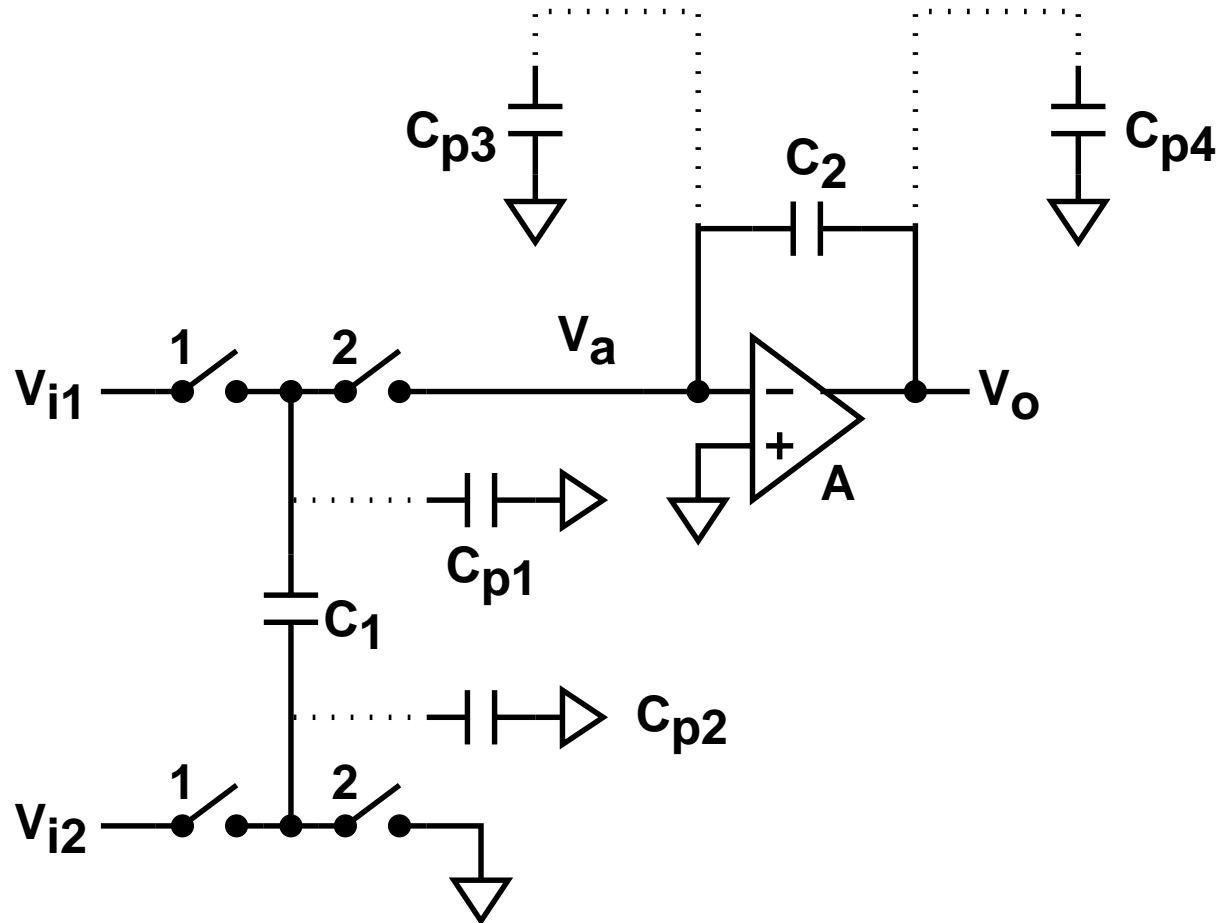
# SC Differential Integrators



RC Integrator  $\rightarrow V_o(s) = -\frac{1}{sR_1C_2} (V_{i1} - V_{i2})$

SC Integrator  $\rightarrow V_o(z) = -\frac{C_1}{C_2} \times \frac{z^{-1}}{1 - z^{-1}} \times [V_{i1}(z) - V_{i2}(z)]$

# Effects of Parasitic Capacitances



$$V_o(z) = \left[ -\frac{C_1}{C_2} [V_{i1}(z) - V_{i2}(z)] - \frac{C_{p1}}{C_2} V_{i1}(z) \right] \times \frac{z^{-1}}{1 - z^{-1}}$$

# Effects of Parasitic Capacitances

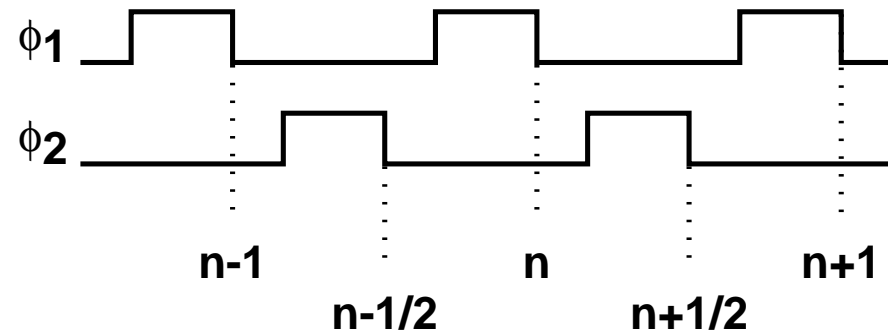
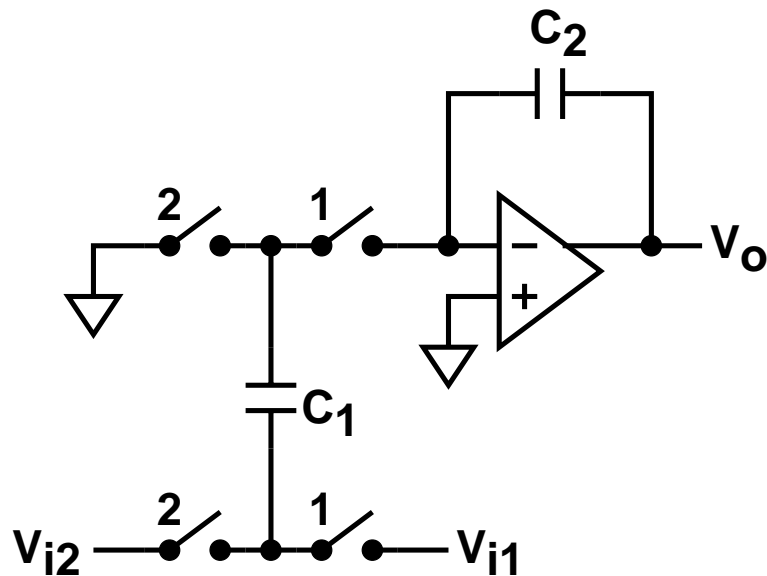
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- Among the parasitic capacitors, only  $C_{p1}$  contribute charge to  $C_2$  if  $A = \infty$ .
- Consider a finite value of  $A$ , then  $V_o = -A \cdot V_a$ , and

$$\begin{aligned} & C_1[V_{i1}(n) - V_{i2}(n)] + C_2[V_a(n) - V_o(n)] + C_{p1}V_{i1} + C_{p3}V_a(n) \\ &= (C_1 + C_{p1} + C_{p3})V_a(n+1) + C_2[V_a(n+1) - V_o(n+1)] \\ \Rightarrow V_o(z) &= \frac{\left[-\frac{C_1}{C_2}[V_{i1}(z) - V_{i2}(z)] - \frac{C_{p1}}{C_2}V_{i1}(z)\right] \times z^{-1}}{1 + \frac{1}{A} \left(1 + \frac{C_1}{C_2} + \frac{C_{p1}}{C_2} + \frac{C_{p3}}{C_2}\right) - z^{-1} \left[1 + \frac{1}{A} \left(1 + \frac{C_{p3}}{C_2}\right)\right]} \end{aligned}$$

- Must keep  $C_{p1} \ll C_1$  and  $C_{p1,p3} \ll C_2$ .
  - Connect the top plates of the capacitors to the opamp's input.
  - Let the bottom plates of the capacitors always be driven.

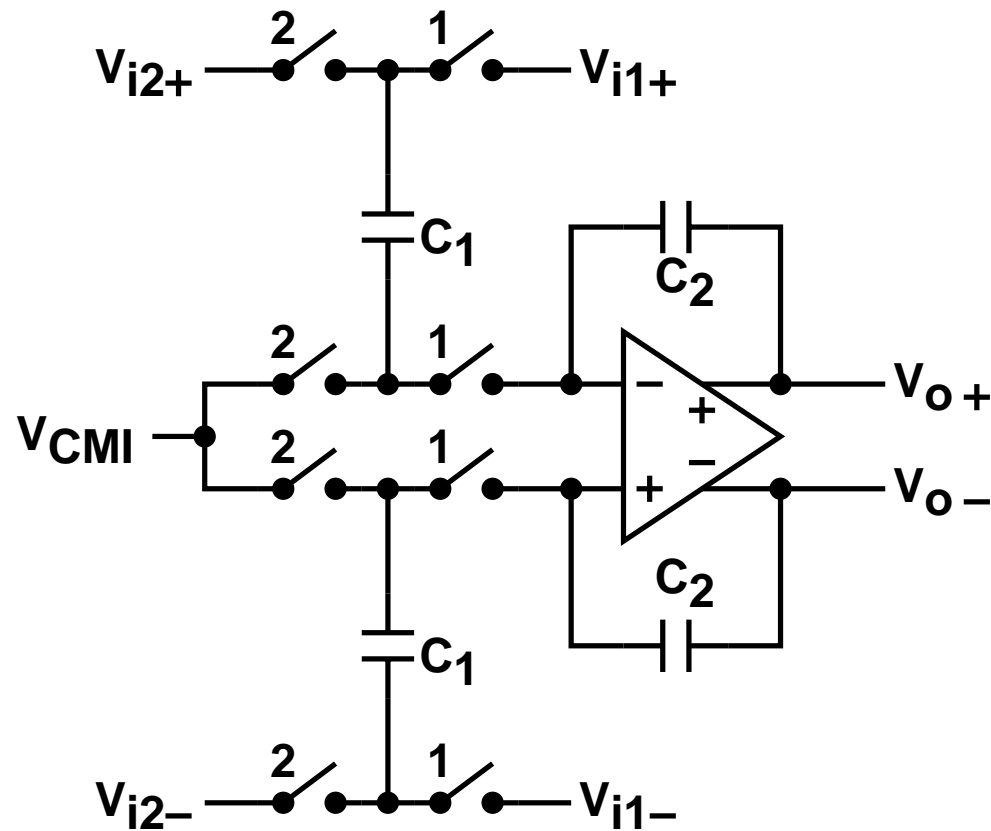
# Parasitics-Insensitive SC Integrators



$$V_o(z) = \frac{\frac{C_1}{C_2} [-V_{i1} + z^{-1}V_{i2}]}{1 + \frac{1}{A} \left( 1 + \frac{C_1}{C_2} + \frac{C_{p1}}{C_2} + \frac{C_{p3}}{C_2} \right) - z^{-1} \left[ 1 + \frac{1}{A} \left( 1 + \frac{C_{p3}}{C_2} \right) \right]}$$

- Insensitive to parasitics if  $A \rightarrow \infty$ .
- The two inputs have different delays.

# Fully Differential SC Integrators



$$V_{i1} = V_{i1+} - V_{i1-}$$

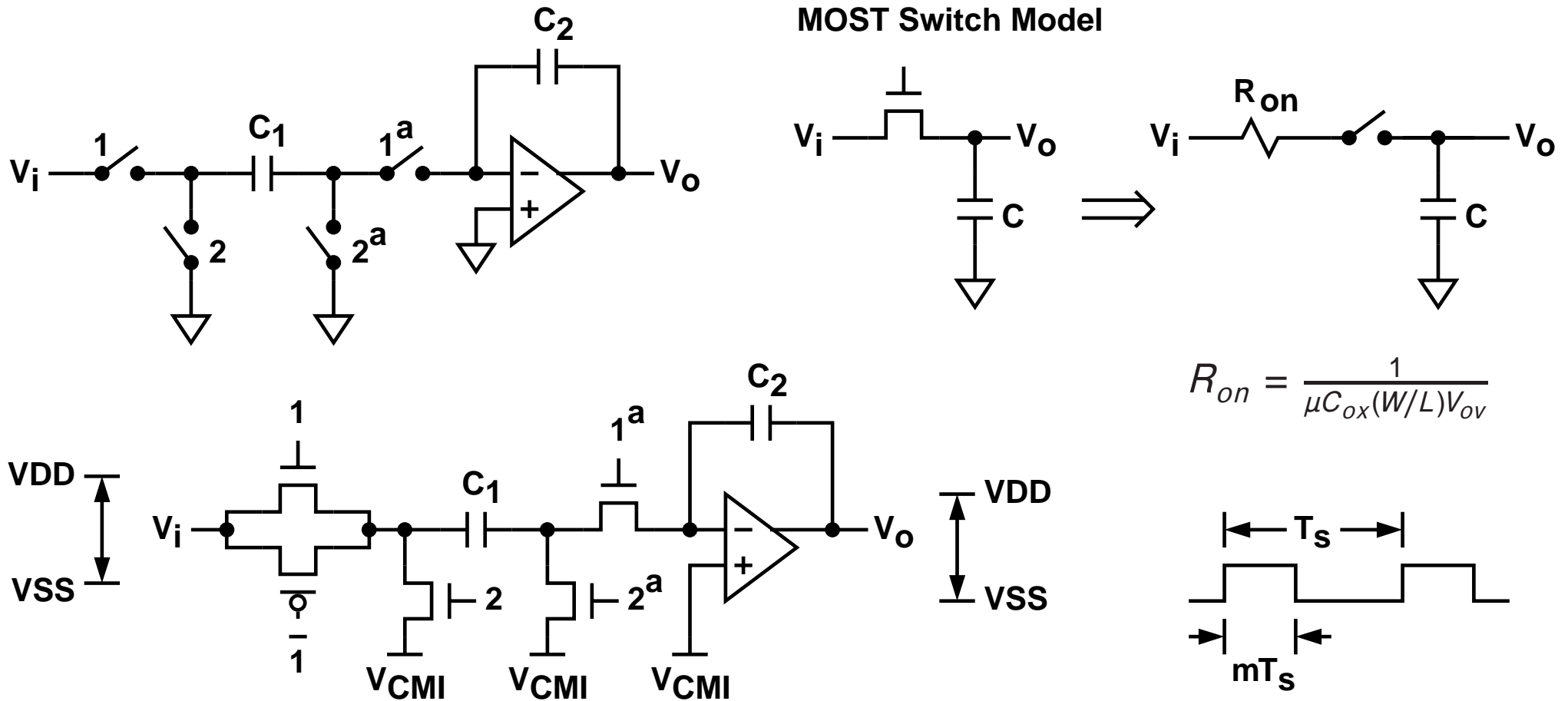
$$V_{i2} = V_{i2+} - V_{i2-}$$

$$V_o = V_{o+} - V_{o-}$$

$$V_o(z) = \frac{C_1}{C_2} \times \left[ -\frac{1}{1 - z^{-1}} \cdot V_{i1} + \frac{z^{-1}}{1 - z^{-1}} \cdot V_{i2} \right]$$

- $V_{CMI}$  and  $V_{CMO}$  can be different.

# MOST Analog Switches



For good settling, want

$$mT_s > 5R_{on}C = \frac{5C}{\mu C_{ox}(W/L)V_{ov}}$$

# MOST Analog Switches

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- When turning off the switch, the switching error is

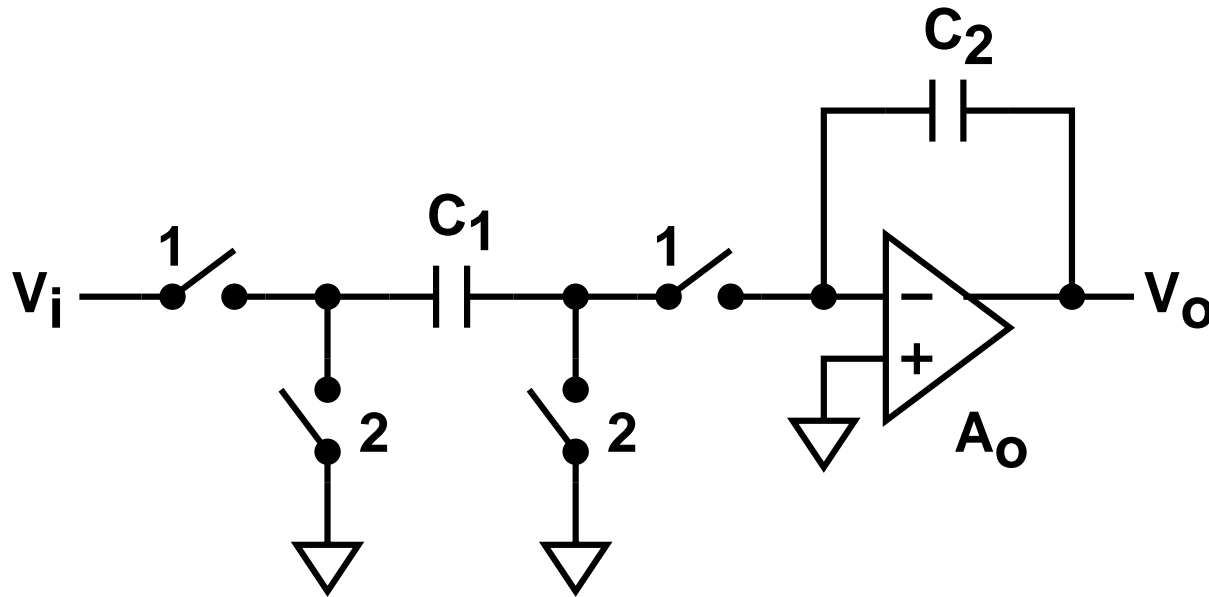
$$\Delta V = \frac{\alpha Q_{CH}}{C} = \frac{\alpha W L C_{ox} V_{ov}}{C}$$

The maximum clock rate is

$$f_s < \frac{m}{\alpha} \cdot \frac{\mu \Delta V}{5L^2}$$

- Realize switches connected to  $V_{SS}$  or near  $V_{SS}$  with nMOSTs.
- Realize switches connected to  $V_{DD}$  or near  $V_{DD}$  with pMOSTs.
- Turn off the switches near the virtual ground node of the opamps first.
- The thermal noise is proportional to  $kT/C$ .
- There are also noises from the power supplies.

# Effects of Opamp's Finite DC Gain



If  $A_o = \infty$ , then

$$V_o(n) = -kV_i(n) + V_o(n-1)$$

$$H(z) = -\frac{k}{1-z^{-1}}$$

$$k = \frac{C_1}{C_2}$$

If  $A_o = 1/\mu$  is finite, then

$$V_o(n) = -k\alpha V_i(n) + \beta V_o(n-1) \quad H(z) = -\frac{k\alpha}{1-\beta z^{-1}}$$

$$\alpha = \frac{1}{1+(1+k)\mu} \approx 1 - (1+k)\mu = 1 + \Delta\alpha \quad \Delta\alpha = -(1+k)\mu \ll 1$$

$$\beta = \frac{1+\mu}{1+(1+k)\mu} \approx 1 - k\mu = 1 + \Delta\beta \quad \Delta\beta = -k\mu \ll 1$$

## Effects of Opamp's Finite DC Gain

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The transfer function  $H(z)$  in s-domain is

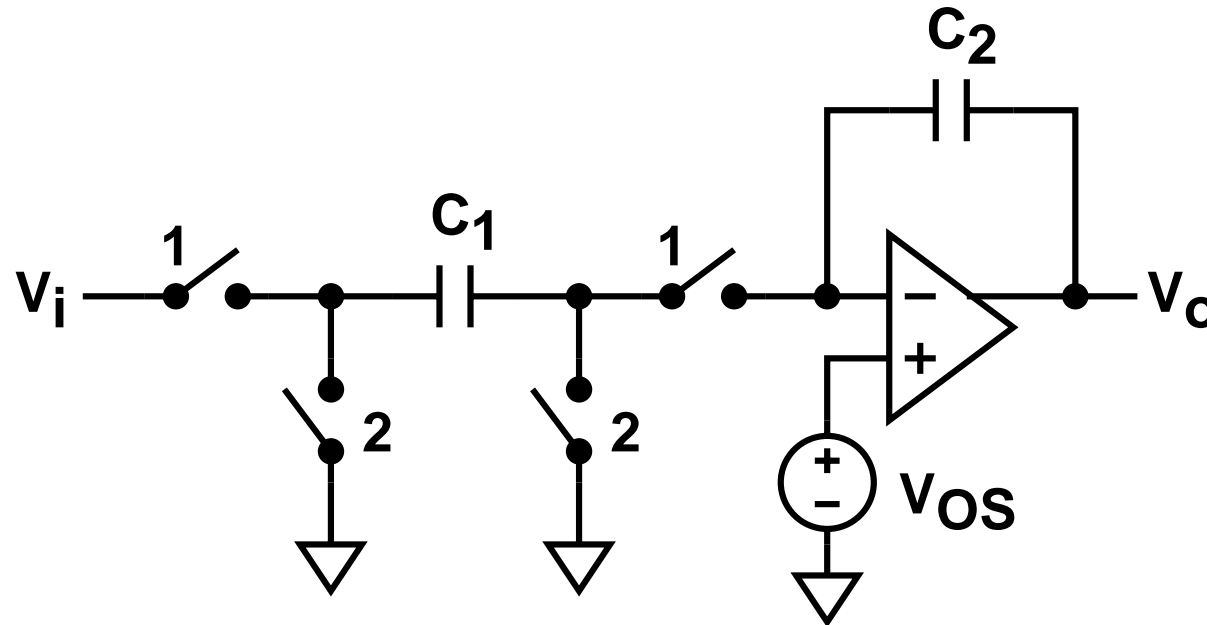
$$H(e^{j\omega T_s}) \approx -\frac{k}{1-z^{-1}} \Big|_{z=e^{j\omega T_s}} \times [1 + m(\omega)] e^{j\theta(\omega)}$$
$$m(\omega) \approx \Delta\alpha - \frac{\Delta\beta}{2} \approx -\left(1 + \frac{1C_1}{2C_2}\right) \cdot \frac{1}{A_o}$$
$$\theta(\omega) \approx -\frac{\Delta\beta}{2} \cdot \frac{1}{\tan(\omega T_s/2)} \approx \frac{1}{2} \cdot \frac{C_1}{C_2} \cdot \frac{1}{A_o} \cdot \frac{1}{\tan(\omega T_s/2)} \approx \frac{C_1}{C_2} \cdot \frac{1}{A_o} \cdot \frac{1}{\omega T_s}$$

- At the unit-gain frequency  $\omega_i$ , where  $\left|H(e^{j\omega_i T_s})\right| = 1$ , we have

$$-m(\omega_i) \approx \theta(\omega_i) \approx 1/A_o \quad \text{if} \quad \omega_i T_s/2 \ll 1$$

- In most applications, the magnitude error  $m(\omega)$  has negligible effect, but the phase error  $\theta(\omega)$  can be detrimental in narrowband (high-Q) filters.

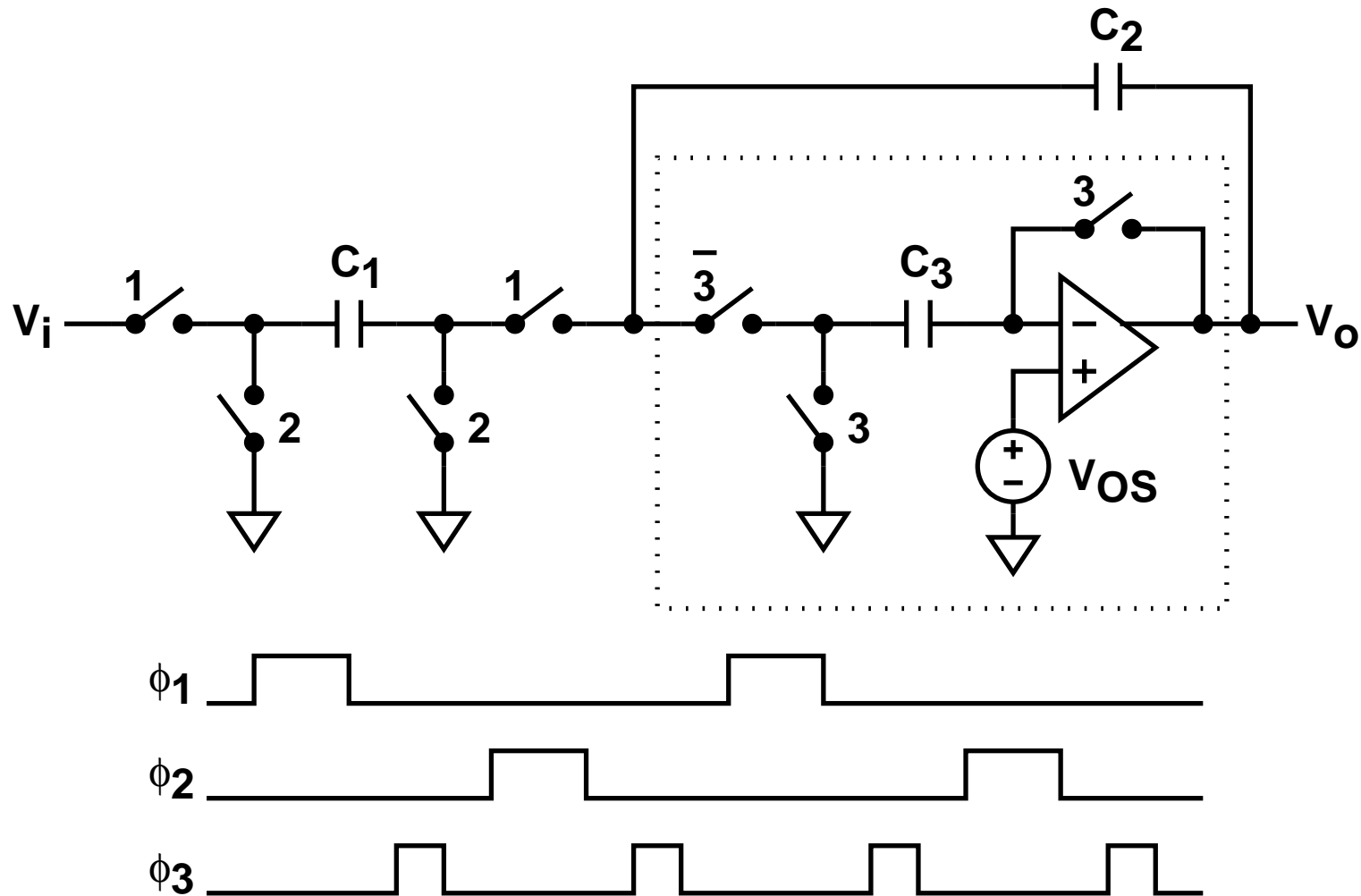
# Effects of Opamp's DC Offset



$$V_o(z) = -\frac{C_1}{C_2} \frac{1}{1 - z^{-1}} \cdot V_i(z) + \frac{C_1}{C_2} \frac{1}{1 - z^{-1}} \cdot V_{OS} + V_{OS}$$

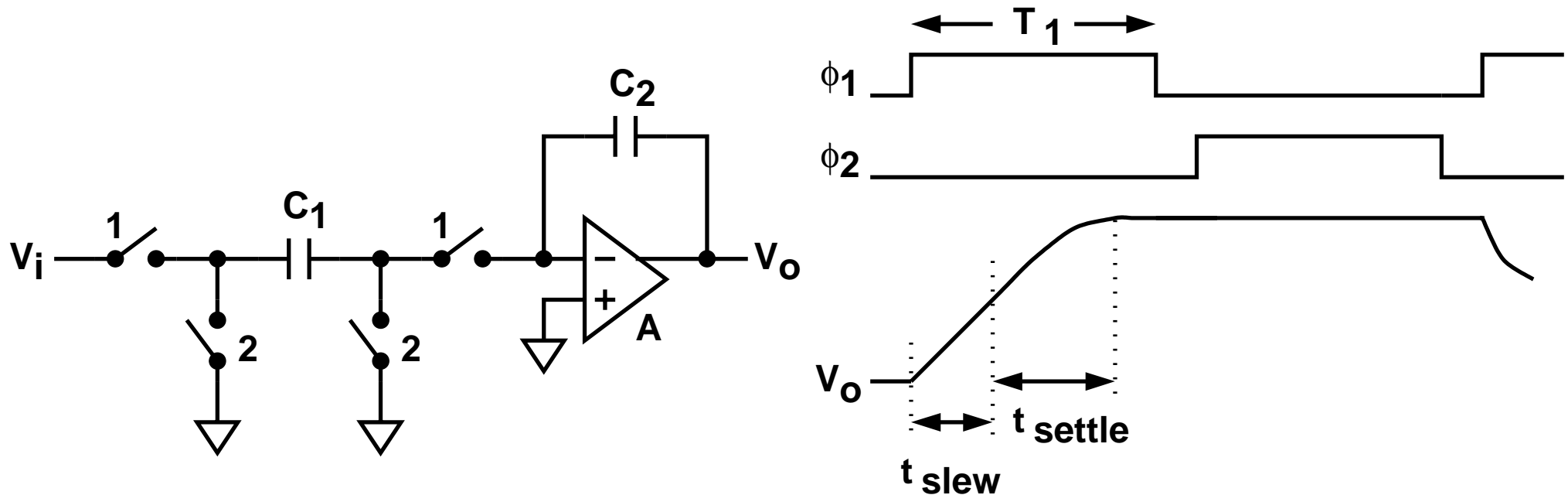
- The  $V_{OS}$  to  $V_o$  transfer function is also an integration.
- When the entire filter is considered, the  $V_{OS}$  may cause finite dc level shift in this and other integrators.

# An Offset Auto-Zeroing Scheme



- During the  $\phi_3$  auto-zeroing mode, opamp's offset voltage is stored in  $C_3$ .

# Effects of Opamp's Finite Settling Time

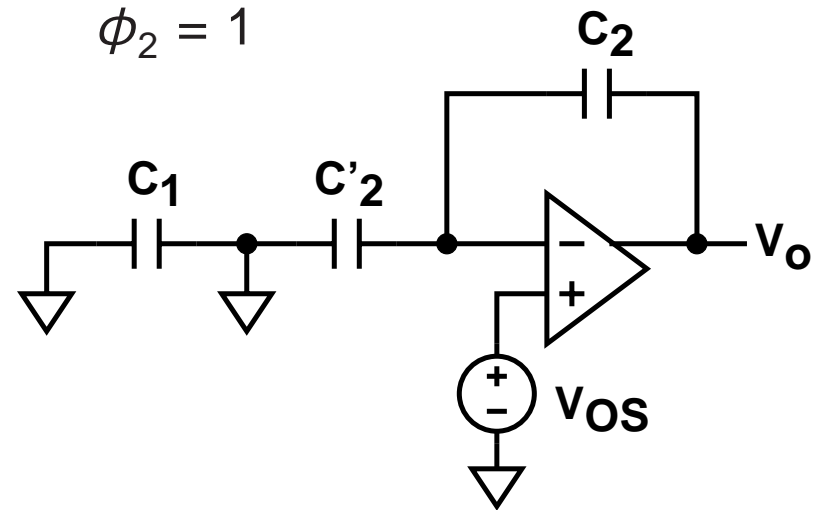
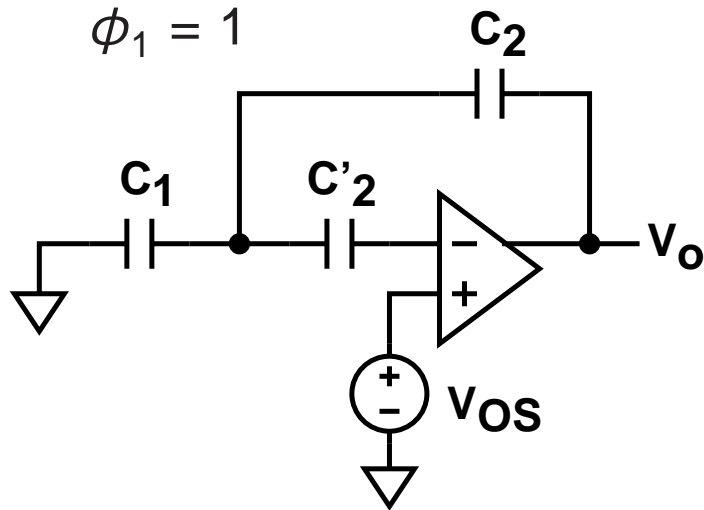
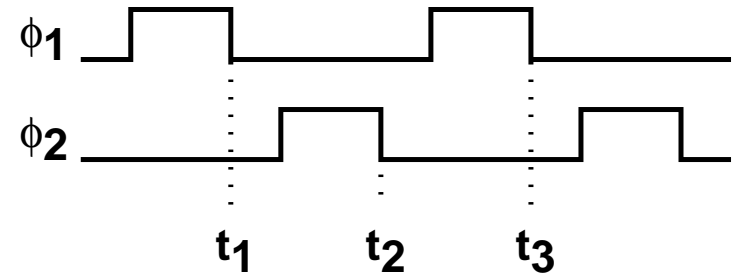
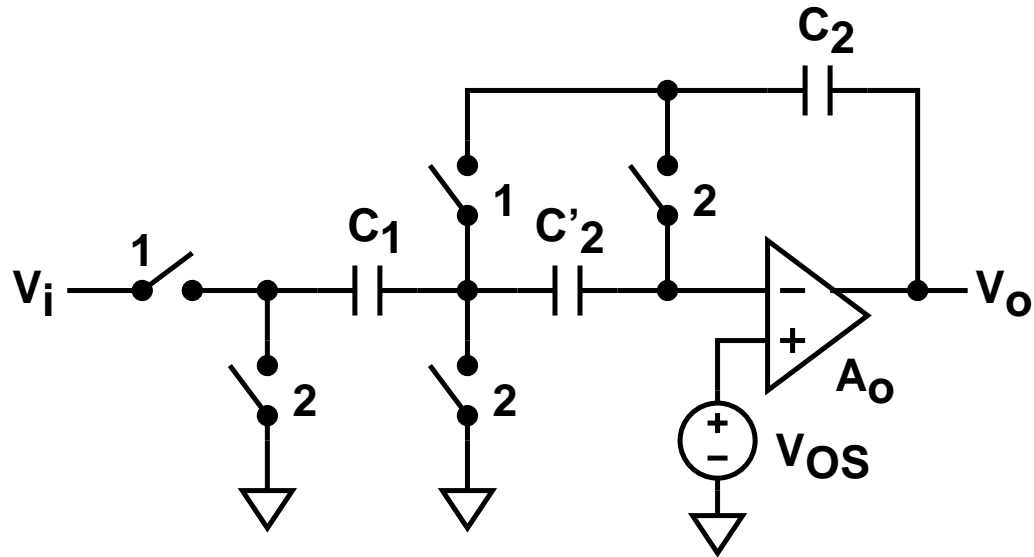


- Let  $t_{\text{slew}} = 0$ ,  $A(s) = \omega_u/s$ ,  $T_1 = T_s/2$ ,  $\omega_i$  is the unit-gain frequency of the integrator, and  $\omega_i T_s \ll 1$ . At  $\omega = \omega_i$ , the magnitude error and phase error of the integrator are

$$m(\omega_i) \approx \theta(\omega_i) \approx -\omega_i T_s e^{-\omega_u T_s / 2}$$

- Want  $\omega_u \geq 5 \cdot \omega_s$ . However, to avoid unnecessary noise aliasing,  $\omega_u$  should not be too much larger than necessary.

# An SC Integrator with CDS



## An SC Integrator with CDS

---

Consider the  $V_{OS}$  effect only. Let

$$V_i = 0 \quad A_o = \infty \quad \text{and} \quad \Delta V_{OS}(t) = V_{OS}(t) - V_{OS}(t - T_s/2)$$

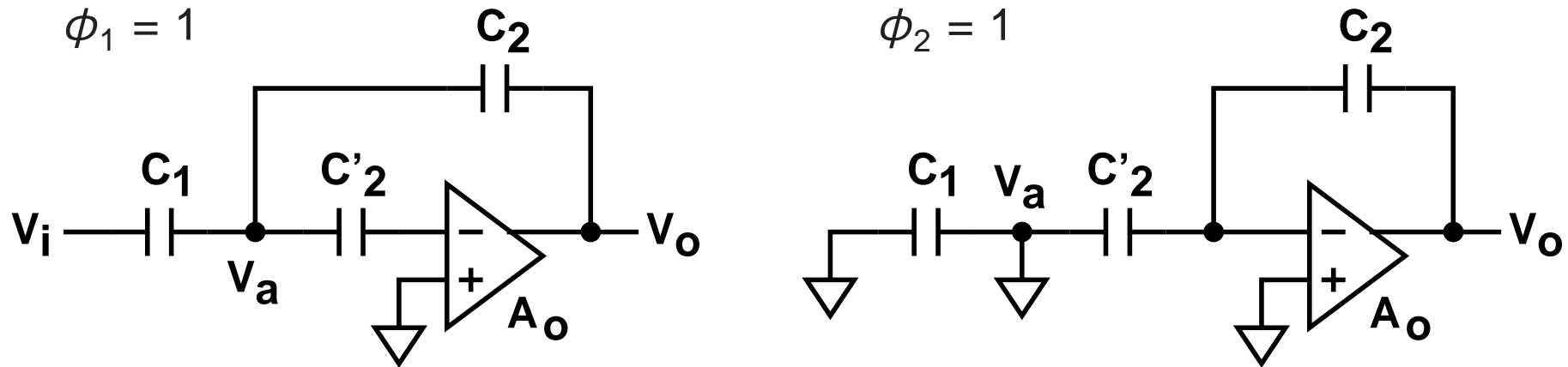
At  $t = t_2$

$$V_o(t_2) = V_o(t_1) + V_{OS}(t_2) + \left(1 + \frac{C'_2}{C_2}\right) \Delta V_{OS}(t_2)$$

At  $t = t_3$

$$\begin{aligned} V_o(t_3) &= V_o(t_2) - V_{OS}(t_2) + \left(1 + \frac{C_1}{C_2}\right) \Delta V_{OS}(t_3) \\ &= V_o(t_1) + \Delta V_{OS}(t_2) + \left(1 + \frac{C_1}{C_2}\right) \Delta V_{OS}(t_3) \end{aligned}$$

# An SC Integrator with CDS



Consider the finite dc gain effect only. Let  $V_{OS} = 0$ , and

$$A_o = \frac{1}{\mu} \quad k = \frac{C_1}{C_2} \quad j = \frac{C'_2}{C_2} \quad \epsilon_1 = (1 + k)\mu \quad \epsilon_2 = (1 + j)\mu$$

At  $t = t_2$

$$V_o(t_2) \approx V_o(t_1) - j(1 - \epsilon_2)V_o(t_1) = [1 - j\mu + (1 + j)\mu^2] V_o(t_1)$$

- Note that  $V_a$  is reset from  $-\mu V_o(t_1)$  to 0.

## An SC Integrator with CDS

---

At  $t = t_3$ , assuming  $V_i = 0$ , then

$$V_o(t_3) = V_o(t_2) + [\mu V_o(t_2) + V_a] + kV_a = -A_o[V_a - \mu V_o(t_2)]$$
$$\Rightarrow V_o(t_3) = \left(1 + \frac{1}{1 + k + A_o}\right) V_o(t_2) \approx [1 + \mu - (1 + k)\mu^2] V_o(t_2)$$

Including  $V_i$ , we have

$$V_o(t_3) \approx -k(1 - \epsilon_1)V_i(t_3) + [1 + \mu - (1 + k)\mu^2] V_o(t_2)$$
$$\approx -k(1 - \epsilon_1)V_i(t_3) + [1 + (1 - j)\mu - k\mu^2] V_o(t_1)$$

## An SC Integrator with CDS

---

If  $j = C'_2/C_2 = 1$ , the output difference equation becomes

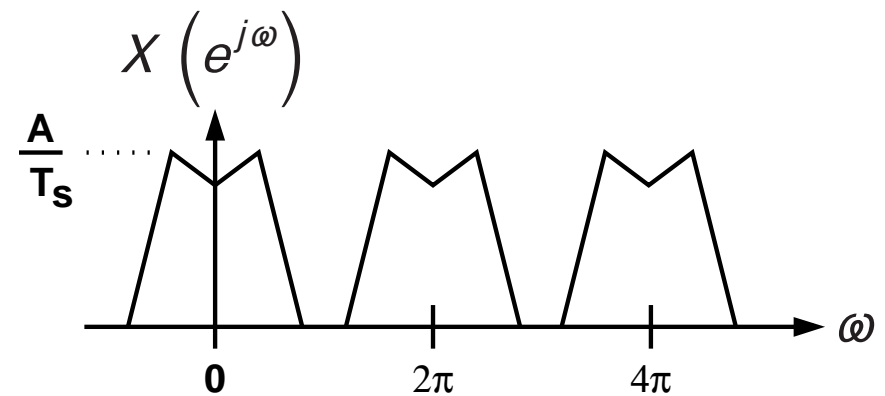
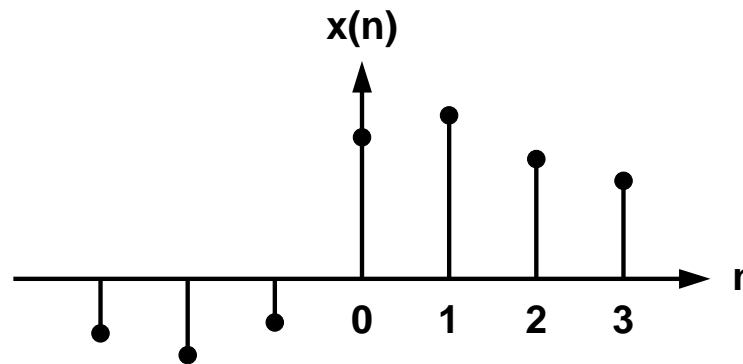
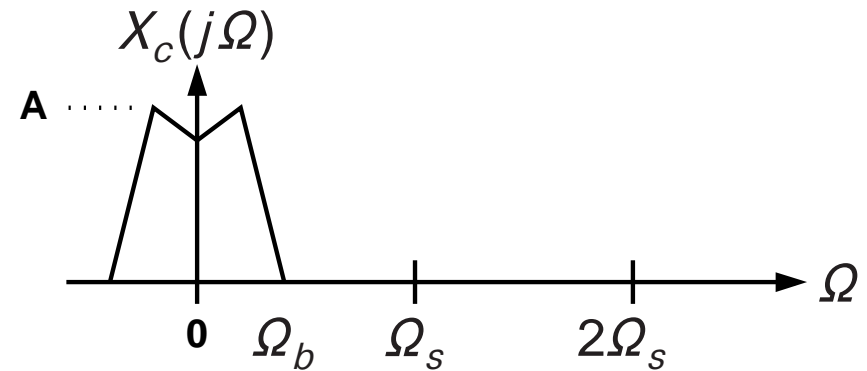
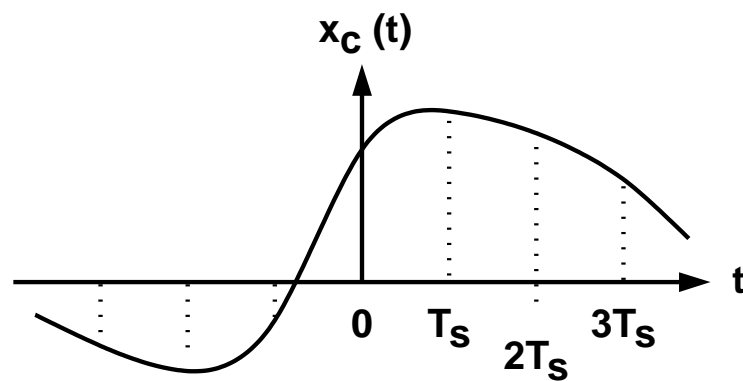
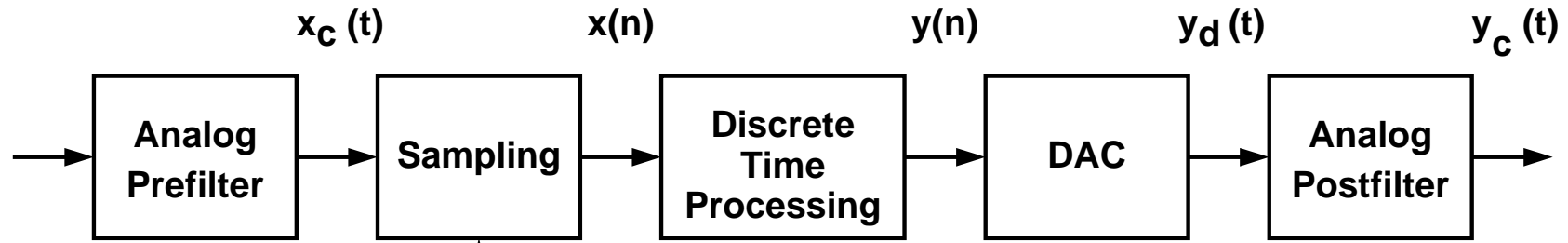
$$V_o(n) = -k(1 + \Delta\alpha)V_i(n) + (1 + \Delta\beta)V_o(n - 1)$$

$$\Delta\alpha = -(1 + k)\mu = -\left(1 + \frac{C_1}{C_2}\right) \cdot \frac{1}{A_o}$$

$$\Delta\beta = -k\mu^2 = -\frac{C_1}{C_2} \cdot \frac{1}{A_o^2}$$

- Reference: W. Ki, et. al., “Offset-Compensated Switched-Capacitor Integrators,” ISCAS, 1990, pp. 2829–2832.

# Discrete-Time Signal Processing



# Continuous-Time Signals

---

The Laplace transform and the continuous-time Fourier transform (CTFT) are

$$X_c(s) = \int_{-\infty}^{\infty} x_c(t) e^{-st} dt \qquad X_c(j\Omega) = \int_{-\infty}^{\infty} x_c(t) e^{-j\Omega t} dt$$

If the region of convergence of  $X_c(s)$  includes the imaginary axis, then

$$X_c(j\Omega) = X_c(s)|_{s=j\Omega}$$

**Sampling Theorem:** To avoid aliasing, want

$$\Omega_s > 2\Omega_b \qquad \Omega_s = 2\pi f_s = \frac{2\pi}{T_s}$$

- $\Omega_b$  is the bandwidth of  $x_c(t)$ ,  $\Omega_s$  is the sampling frequency, and  $2\Omega_b$  is called the *Nyquist rate*.

# Discrete-Time Signals

---

In discrete-time domain, the z transform is

$$X(z) = \sum_{n=-\infty}^{\infty} x(n)z^{-n}$$

The discrete-time Fourier transform (DTFT) is

$$X(e^{j\omega}) = \sum_{n=-\infty}^{\infty} x(n)e^{-j\omega n}$$

If the region of convergence of  $X(z)$  includes the unit circle, then

$$X(e^{j\omega}) = X(z)|_{z=e^{j\omega}}$$

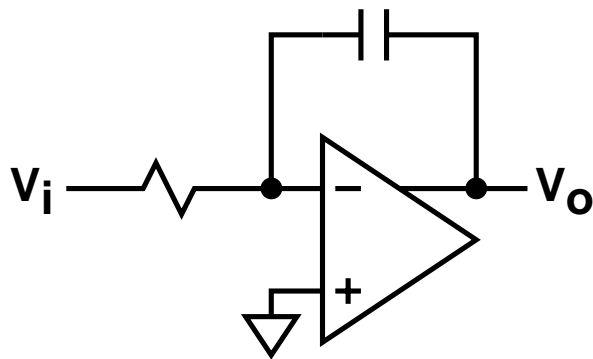
# s-to-z Transformation

Want to approximate  $H_c(s)$  with  $H(z)$ .

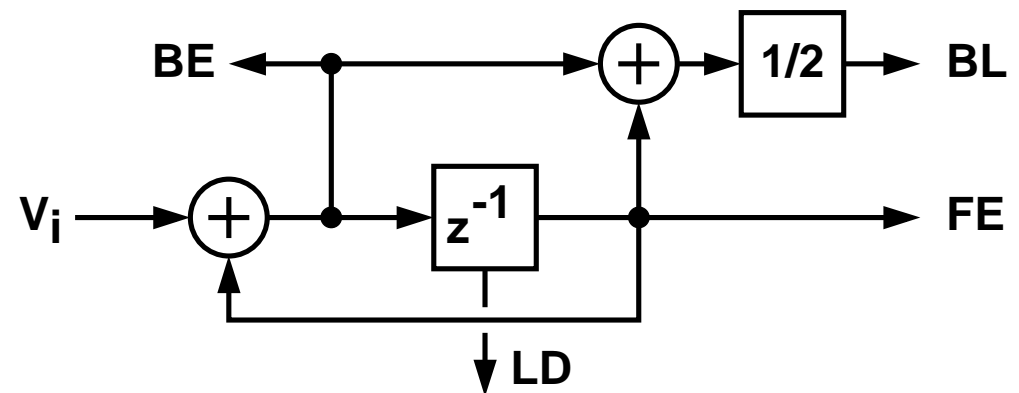
$$z = e^{sT_s} \quad s = \frac{1}{T_s} \cdot \ln z \quad \Rightarrow \quad H(z) = H_c(s)|_{s=(1/T_s)\ln z} \approx H_c(s)|_{s=T(z)}$$

Transformation error of an Integrator can be written as

$$H_c(s) = \frac{1}{s} = \frac{1}{j\Omega} \quad \Rightarrow \quad H(z)|_{e^{j\Omega T_s}} = \frac{1}{j\Omega} \cdot [1 - e^{-j\Omega T_s}] \cdot e^{j\phi(\Omega)}$$



s to z  
 $\Rightarrow$



# s-to-z Transformation

---

Backward Euler (BE) Transformation

$$s = \frac{1}{T_s} \cdot (1 - z^{-1}) \quad \Rightarrow \quad \frac{1}{s} = T_s \cdot \frac{1}{1 - z^{-1}} \quad \epsilon = 1 - \frac{\Omega T_s/2}{\sin(\Omega T_s/2)} \quad \phi = +\frac{\Omega T_s}{2}$$

Forward Euler (FE) Transformation

$$s = \frac{1}{T_s} \cdot \frac{1 - z^{-1}}{z^{-1}} \quad \Rightarrow \quad \frac{1}{s} = T_s \cdot \frac{z^{-1}}{1 - z^{-1}} \quad \epsilon = 1 - \frac{\Omega T_s/2}{\sin(\Omega T_s/2)} \quad \phi = -\frac{\Omega T_s}{2}$$

Lossless Discrete (LD) Transformation

$$s = \frac{1}{T_s} \cdot \frac{1 - z^{-1}}{z^{-1/2}} \quad \Rightarrow \quad \frac{1}{s} = T_s \cdot \frac{z^{-1/2}}{1 - z^{-1}} \quad \epsilon = 1 - \frac{\Omega T_s/2}{\sin(\Omega T_s/2)} \quad \phi = 0$$

## Bilinear s-to-z Transformation

---

The transformation is

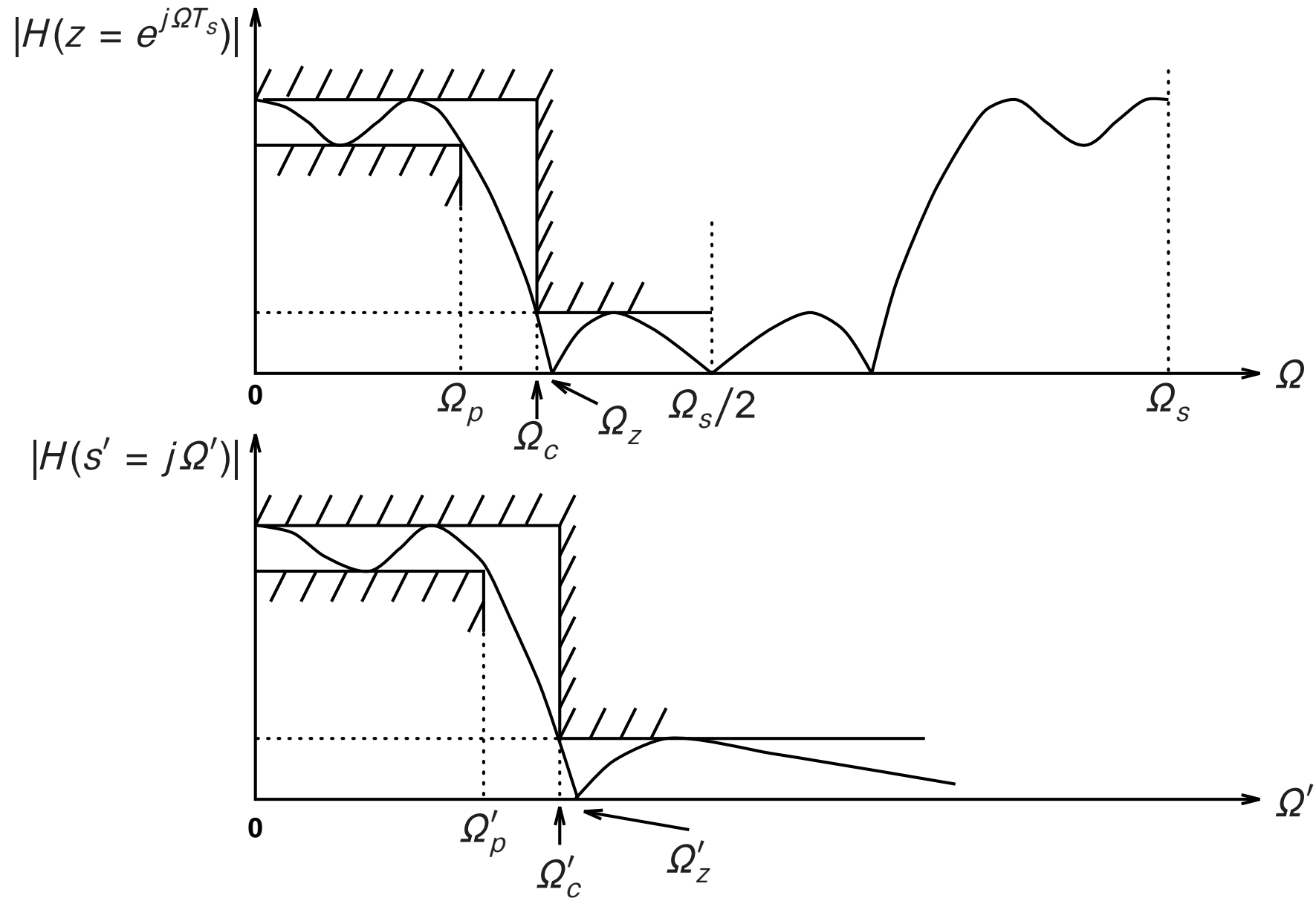
$$s = \frac{2}{T_s} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \quad \Rightarrow \quad \frac{1}{s} = \frac{T_s}{2} \cdot \frac{1 + z^{-1}}{1 - z^{-1}} \quad \epsilon = 1 - \frac{\Omega T_s / 2}{\tan(\Omega T_s / 2)} \quad \phi = 0$$

let  $z = e^{j\omega}$ , then

$$s = \frac{2}{T_s} \cdot \frac{e^{j\omega} - 1}{e^{j\omega} + 1} = \frac{2}{T_s} \cdot j \tan\left(\frac{\omega}{2}\right) = j\Omega \quad \Omega = \frac{2}{T_s} \tan\left(\frac{\omega}{2}\right)$$

- The unit circle in the z-plane is mapped to the  $j\Omega$  axis in the s-plane.

# $H_c(s)$ to $H(z)$ Design Procedures for Bilinear Transformation



# $H_c(s)$ to $H(z)$ Design Procedures for Bilinear Transformation

---

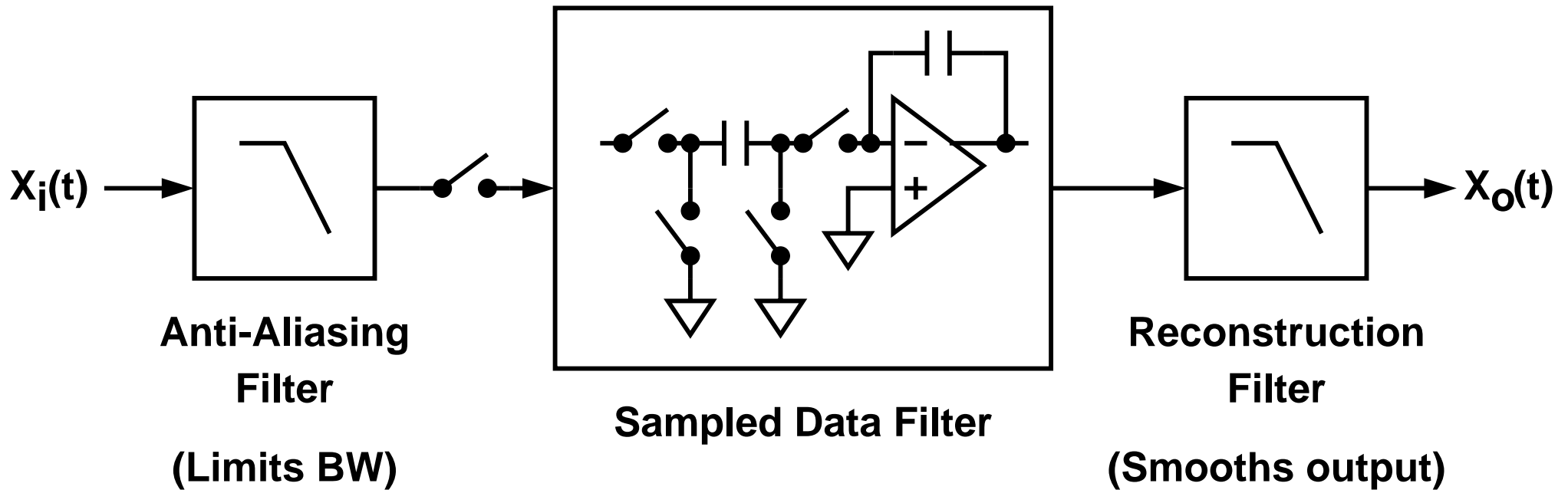
- Prewarp the filter specifications from  $\Omega$  to  $\Omega'$ .

$$\Omega'_p = \frac{2}{T_s} \tan \frac{\Omega_p T_s}{2} \quad \Omega'_c = \frac{2}{T_s} \tan \frac{\Omega_c T_s}{2} \quad \Omega'_z = \frac{2}{T_s} \tan \frac{\Omega_z T_s}{2}$$

- Find  $H_c(s')$ .
- The  $H(z)$  is obtained by

$$H(z) = H_c \left( s' = \frac{2}{T_s} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \right)$$

# Switched-Capacitor Filter Systems



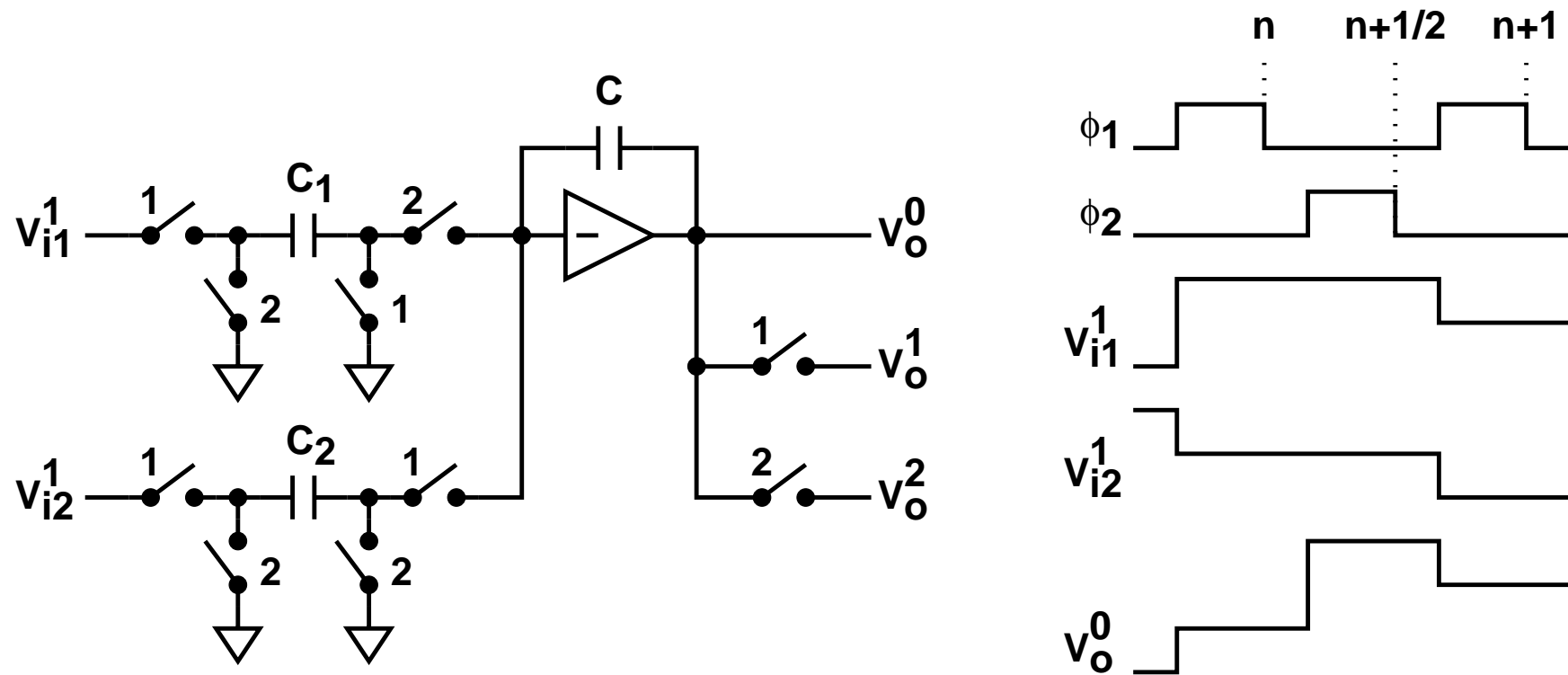
- Discrete-time (or sampled-data) analog filters.
- Filters consist of analog switches, capacitors and opamps.
- Filter response is determined by ratios of capacitance.

# Design Constraints

---

- Switched-C “resistor” cannot be the only feedback around an opamp. Since the path is not continuous, it won’t stabilize the opamp.
- No floating node. Otherwise charge can accumulate.
- Capacitor bottom plate must always be driven from a low impedance (voltage sources or ground).
- Connect non-inverting opamp input to a dc bias. Otherwise response is sensitive to parasitic capacitances.

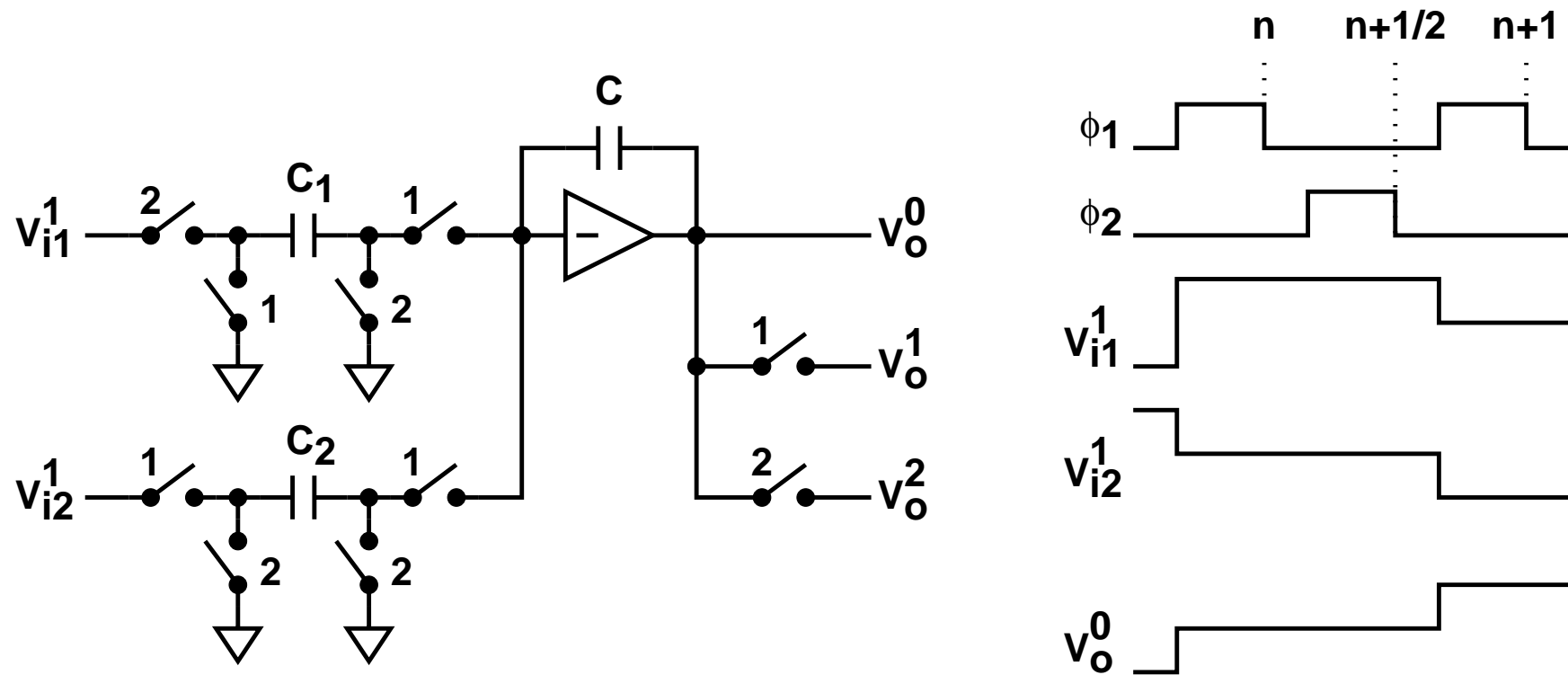
# Periodic Time-Variance in Biphase SC Filters



The circuit is *periodic time-variant* if

$$V_o^1[n \cdot T_s] \neq V_o^2 \left[ \left( n + \frac{1}{2} \right) \cdot T_s \right]$$

# Periodic Time-Invariance in Biphase SC Filters

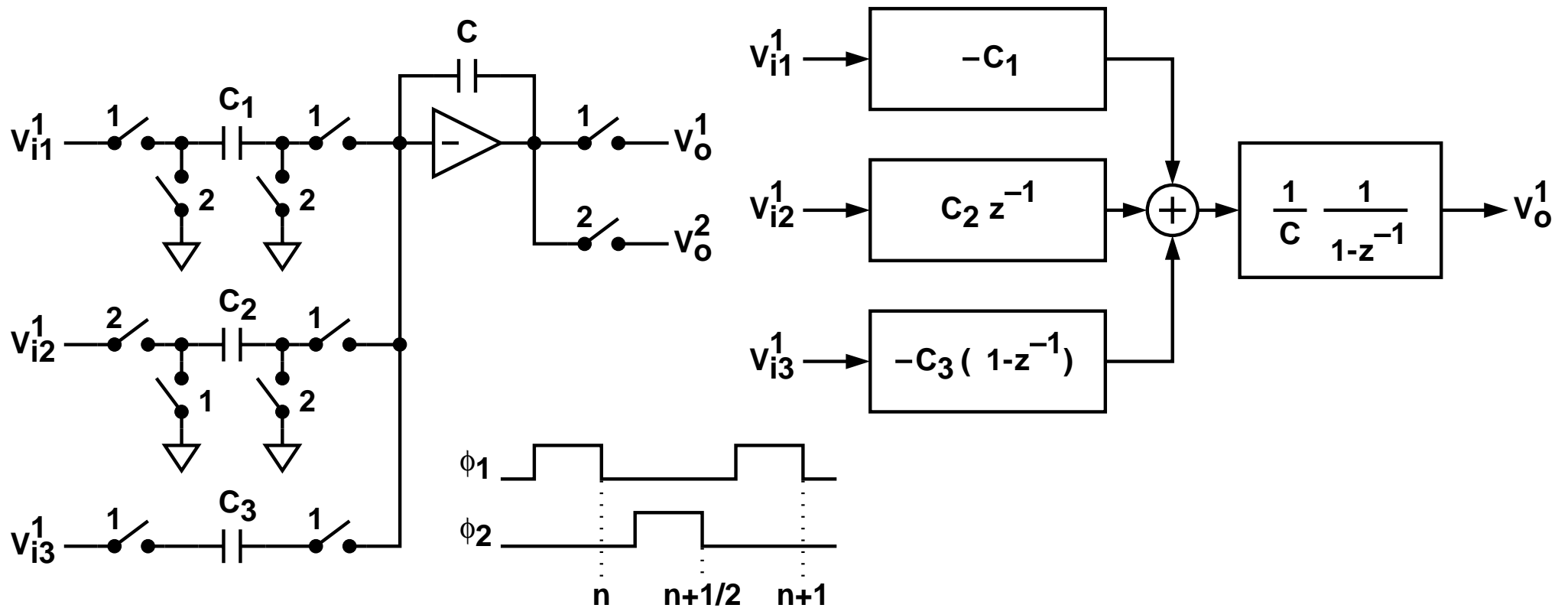


The circuit is *periodic time-invariant* if

$$V_o^1[n \cdot T_s] = V_o^2 \left[ \left( n + \frac{1}{2} \right) \cdot T_s \right]$$

- SC filters are more robust when designed to be time-invariant.

# Active Switched-Capacitor Integrators



$$V_o^1 = \frac{1}{C(1-z^{-1})} \cdot [-C_1 V_{i1}^1 + C_2 z^{-1} V_{i2}^1 - C_3 (1-z^{-1}) V_{i3}^1]$$

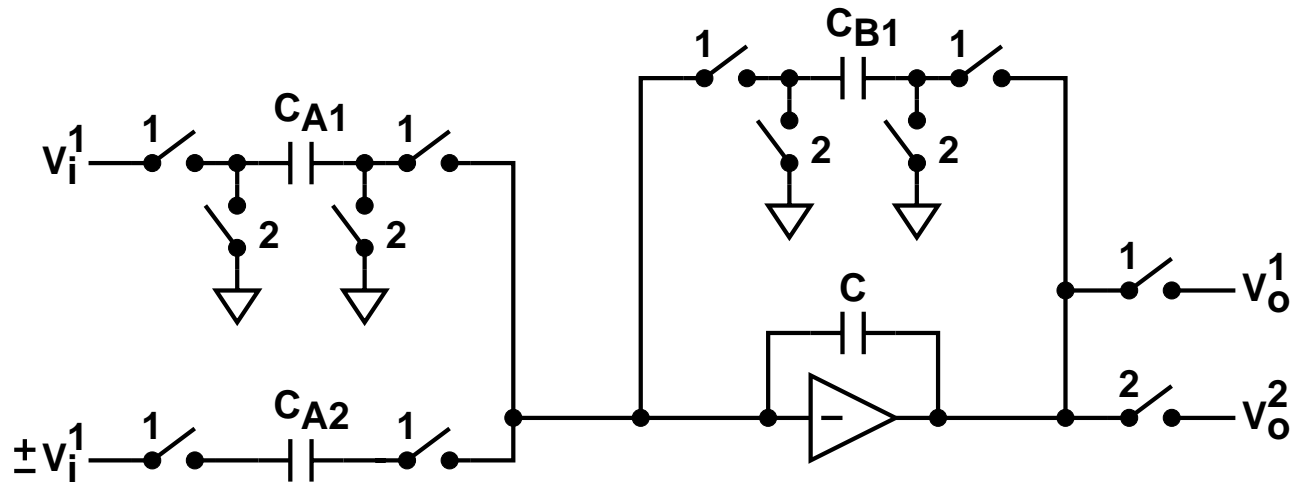
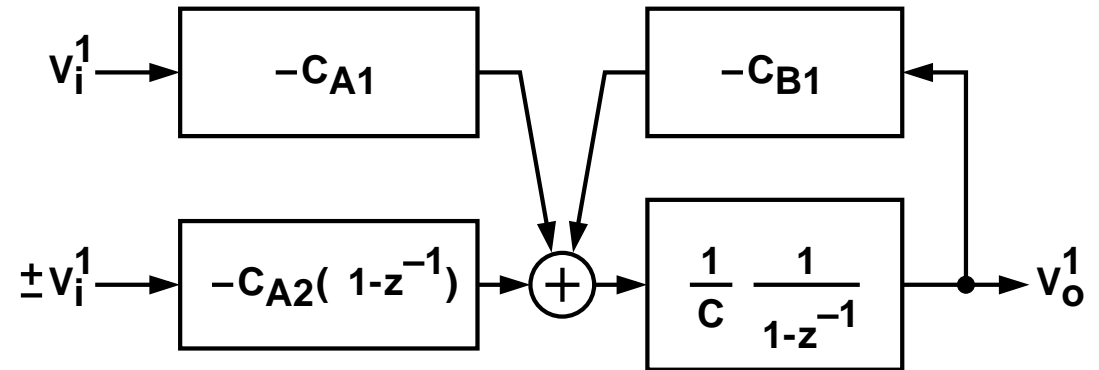
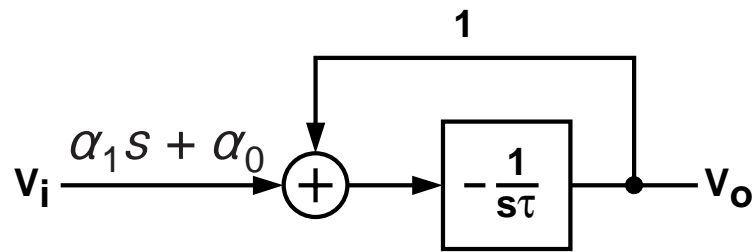
$$V_o^2 = V_o^1 \cdot z^{-1/2}$$

# Active Switched-Capacitor Integrators

---

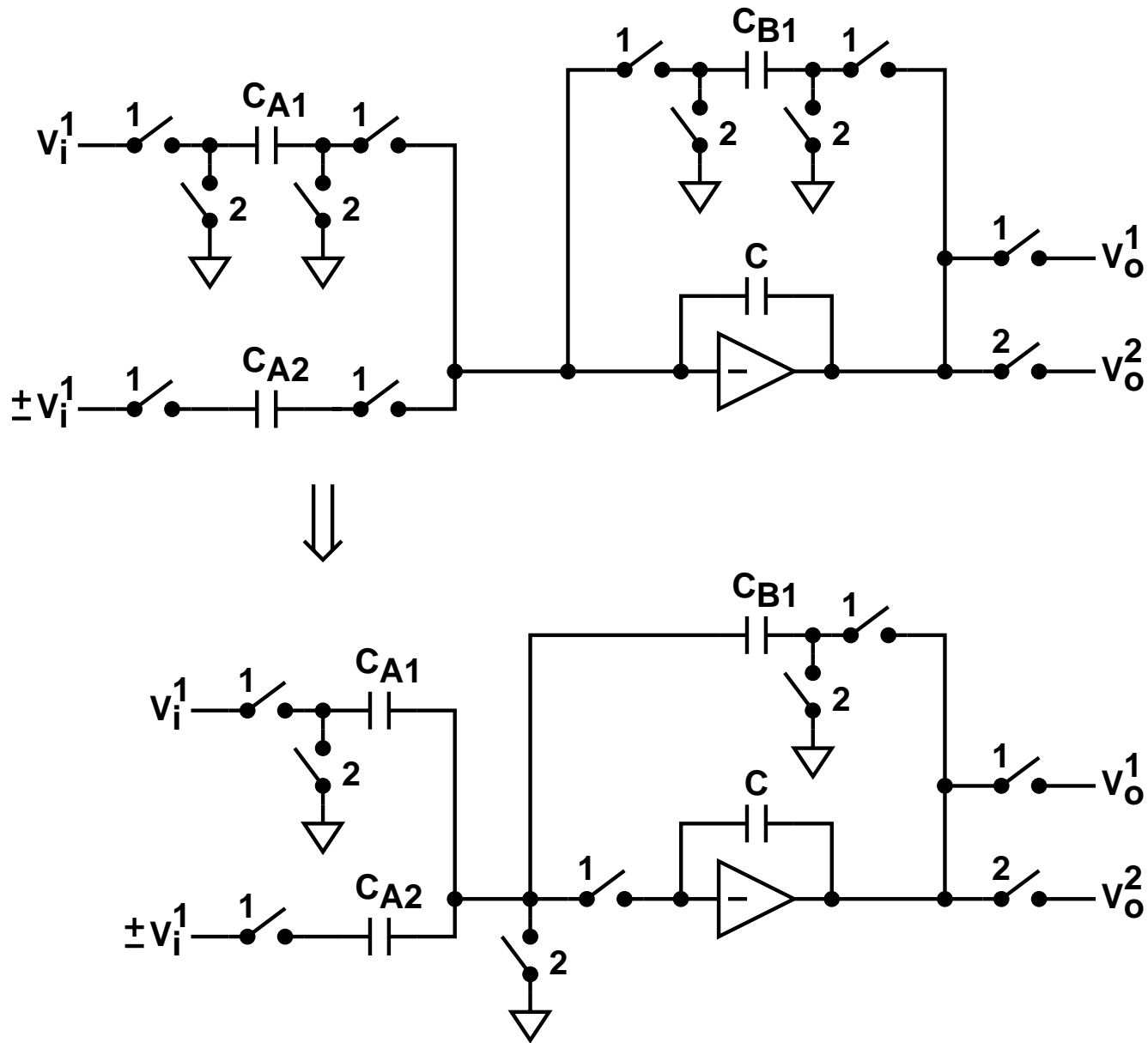
- $V_{i1}^1$  to  $V_o^1$  is a Backward Euler (–BE) integrator.
- $V_{i1}^1$  to  $V_o^2$  is a Lossless Discrete (–LD) integrator.
- $V_{i2}^1$  to  $V_o^1$  is a Forward Euler (+FE) integrator.
- $V_{i2}^2$  to  $V_o^1$  is a Lossless Discrete (+LD) integrator.

# SC First-Order Filters

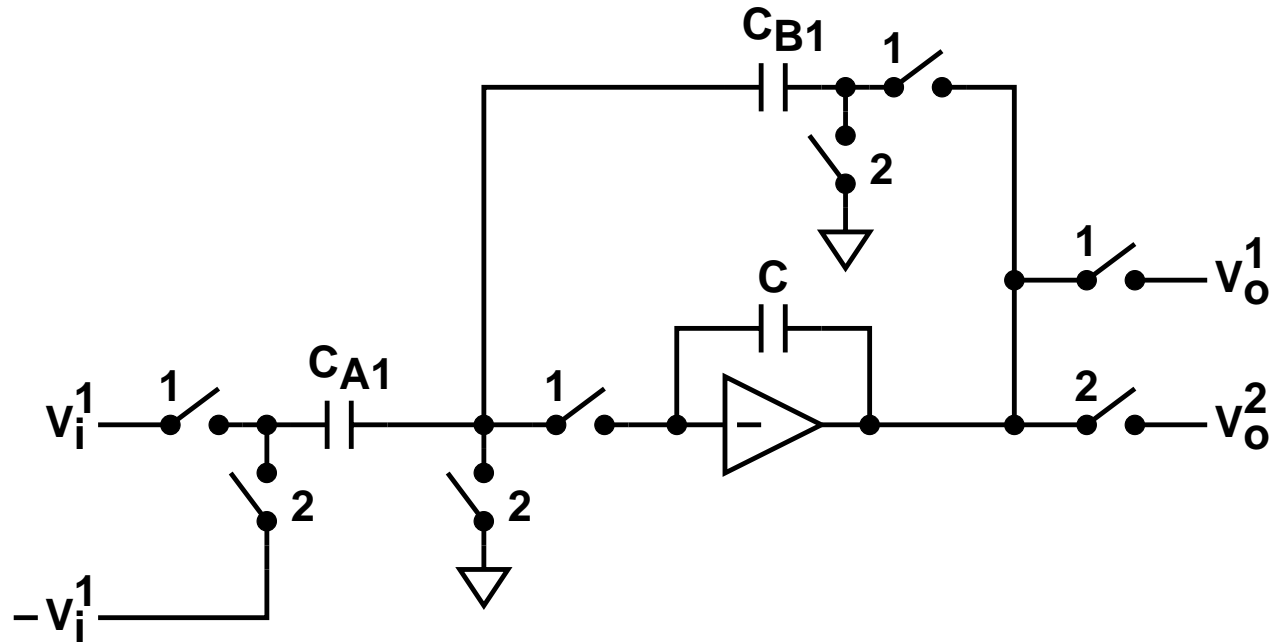


$$\frac{V_o(s)}{V_i(s)} = -\frac{\alpha_1 s + \alpha_0}{s\tau + 1} \quad \frac{V_o^1}{V_i^1} = -\frac{C_{A1} \pm C_{A2}(1 - z^{-1})}{C_{B1} + C(1 - z^{-1})} = -\frac{\left(\frac{C_{A1}}{C} \pm \frac{C_{A2}}{C}\right) \mp \frac{C_{A2}}{C} z^{-1}}{\left(\frac{C_{B1}}{C} + 1\right) - z^{-1}}$$

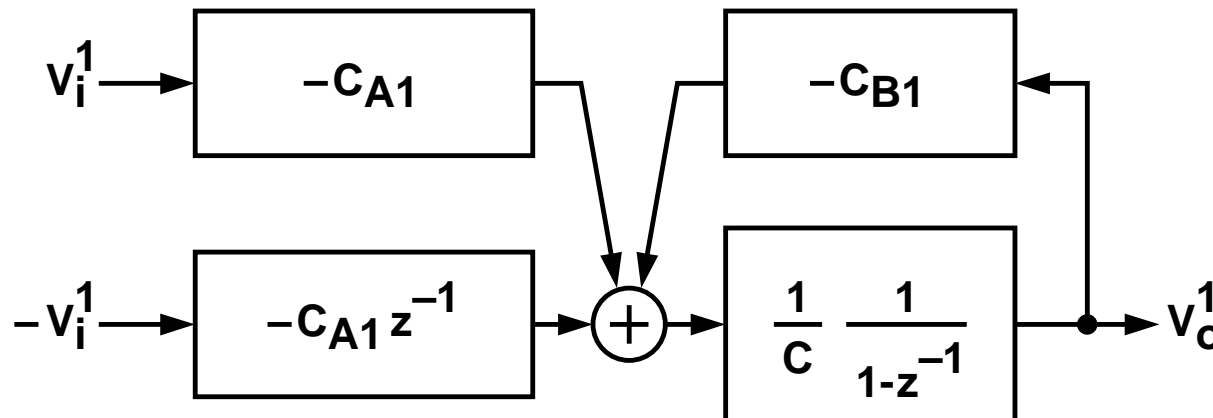
# Switch Sharing



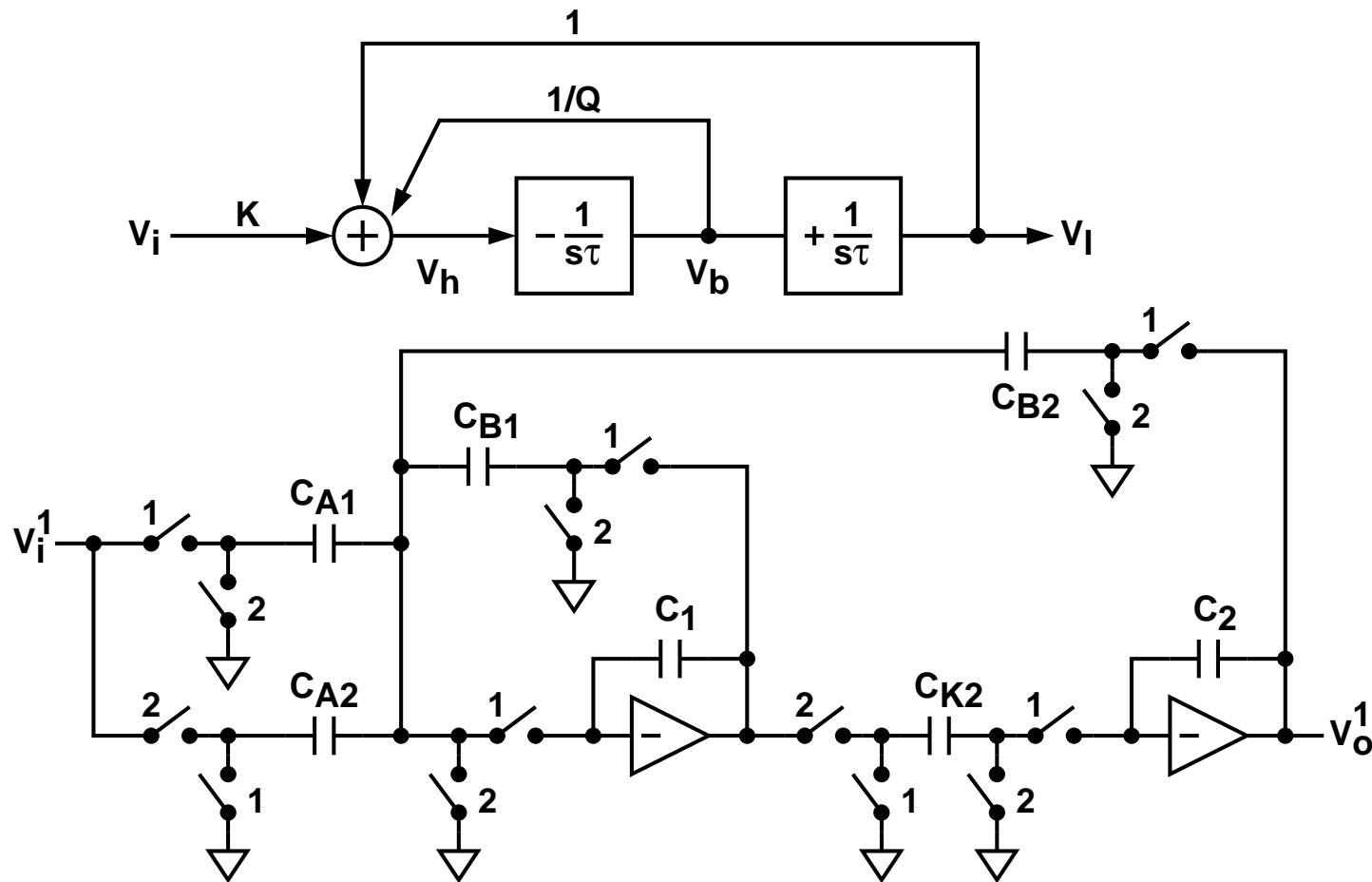
# Bilinear SC First-Order Filters



$$\begin{aligned} \frac{V_o^1}{V_i^1} &= -\frac{C_{A1} + C_{A1}z^{-1}}{C_{B1} + C(1 - z^{-1})} \\ &= -\frac{\frac{C_{A1}}{C} + \frac{C_{A1}}{C}z^{-1}}{\left(\frac{C_{B1}}{C} + 1\right) - z^{-1}} \end{aligned}$$

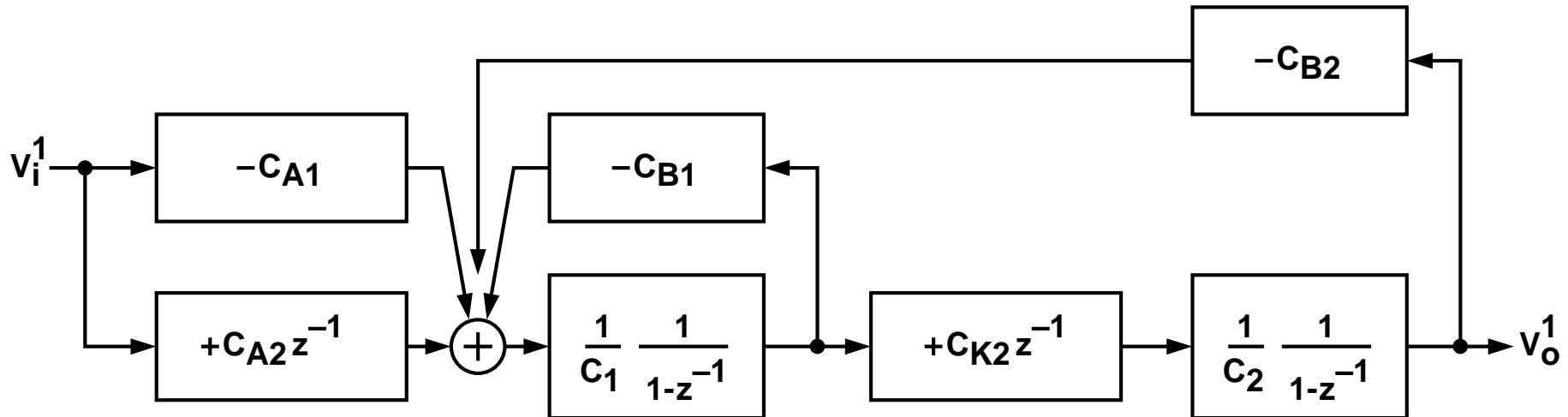
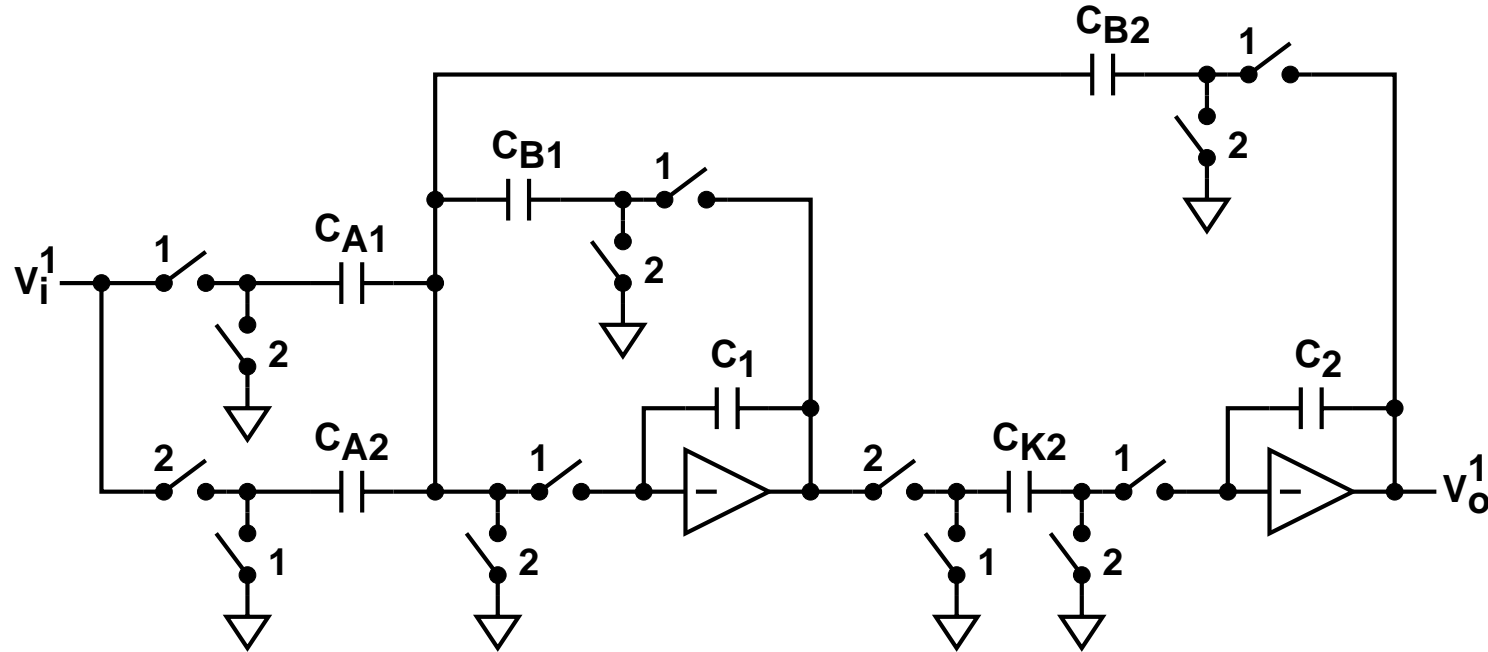


# SC Second-Order Filters

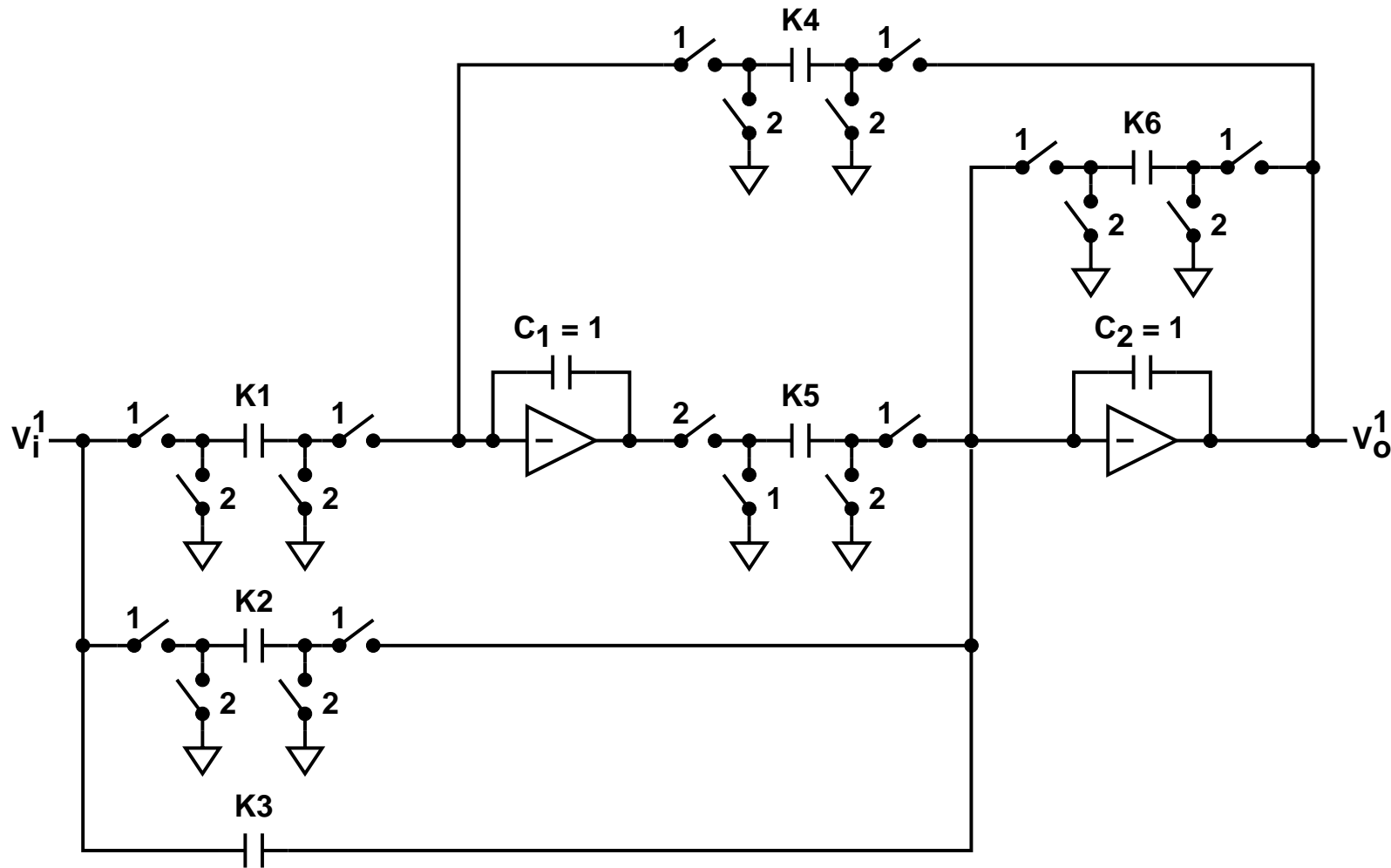


$$\frac{V_o^1}{V_i^1} = \frac{\left(\frac{C_{A1} C_{K2}}{C_1 C_2}\right) z^{-1} - \left(\frac{C_{A2} C_{K2}}{C_1 C_2}\right) z^{-2}}{\left(\frac{C_{B1}}{C_1} + 1\right) + \left(\frac{C_{B2}}{C_1} \cdot \frac{C_{K2}}{C_2} - \frac{C_{B1}}{C_1} - 2\right) z^{-1} + z^{-2}}$$

# SC Second-Order Filters



# A Low-Q SC Biquad



$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{(K_2 + K_3)z^2 + (K_1K_5 - K_2 - 2K_3)z + K_3}{(1 + K_6)z^2 + (K_4K_5 - K_6 - 2)z + 1} = -\frac{a_2z^2 + a_1z^1 + a_0}{b_2z^2 + b_1z + 1}$$

## A Low-Q SC Biquad

---

We have

$$K_3 = a_0 \quad K_2 = a_2 - a_0 \quad K_1 K_5 = a_0 + a_1 + a_2 \quad K_6 = b_2 - 1 \quad K_4 K_5 = b_2 + b_1 + 1$$

- Additional constraint can be made by

$$K_5 = 1 \quad \text{or} \quad K_4 = K_5 = \sqrt{b_2 + b_1 + 1}$$

Let  $z = e^{j\Omega T_s} = \cos(\Omega T_s) + j \sin(\Omega T_s)$ , and

$$z^{1/2} = \cos\left(\frac{\Omega T_s}{2}\right) + j \sin\left(\frac{\Omega T_s}{2}\right) \quad z^{-1/2} = \cos\left(\frac{\Omega T_s}{2}\right) - j \sin\left(\frac{\Omega T_s}{2}\right)$$

Then

$$H(e^{j\Omega T_s}) = \frac{K_1 K_5 + j K_2 \sin(\Omega T_s) + (4K_3 + 2K_2) \sin^2(\Omega T_s/2)}{K_4 K_5 + j K_6 \sin(\Omega T_s) + (4 + 2K_6) \sin^2(\Omega T_s/2)}$$

## A Low-Q SC Biquad

---

Assume  $\Omega T_s \ll 1$ , we have

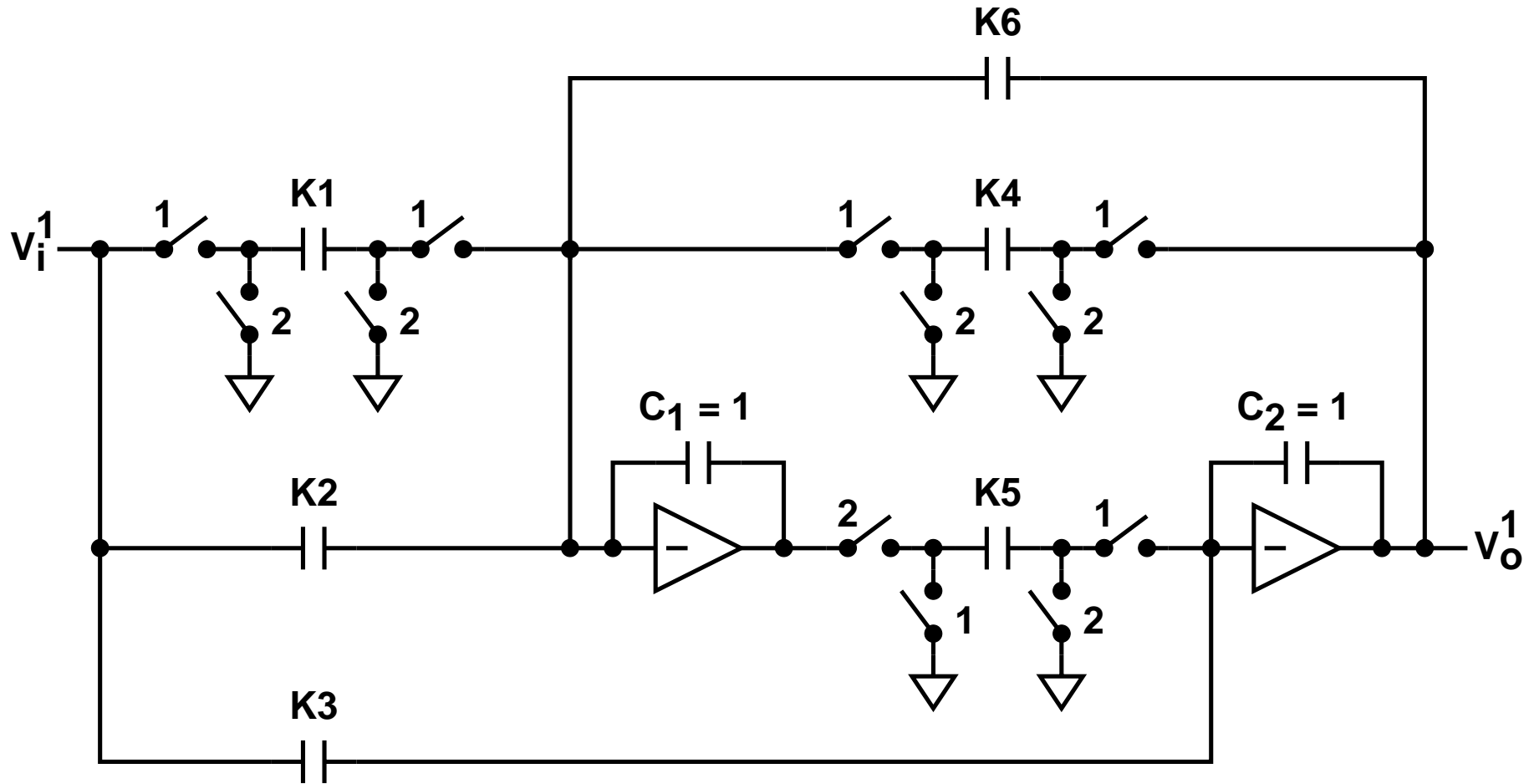
$$H(e^{j\Omega T_s}) \approx \frac{K_1 K_5 + jK_2(\Omega T_s) + (K_3 + K_2/2)(\Omega T_s)^2}{K_4 K_5 + jK_6(\Omega T_s) + (1 + K_6/2)(\Omega T_s)^2} = \frac{\alpha_2 s^2 + \alpha_1 s + \alpha_0}{s^2 + \frac{\omega_p}{Q_p} \cdot s + \omega_p^2}$$

Let  $K_4 = K_5$ , then

$$K_4 = K_5 \approx \omega_p T_s \quad K_6 \approx \frac{\omega_p T_s}{Q_p}$$

- Usually,  $\omega_p T_s \ll 1$ .
- The largest capacitors are the integrating capacitors,  $C_1$  and  $C_2$ .
- If  $Q_p < 1$ , the smallest capacitors are  $K_4$  and  $K_5$ .
- If  $Q_p > 1$ , the smallest capacitors is  $K_6$ .

# A High-Q SC Biquad



$$H(z) = \frac{V_o(z)}{V_i(z)} = -\frac{K_3 z^2 + (K_1 K_5 + K_2 K_5 - 2K_3)z + (K_3 - K_2 K_5)}{z^2 + (K_4 K_5 + K_5 K_6 - 2)z + (1 - K_5 K_6)} = -\frac{a_2 z^2 + a_1 z^1 + a_0}{z^2 + b_1 z + b_0}$$

# A High-Q SC Biquad

---

We have

$$K_1K_5 = a_0 + a_1 + a_2 \quad K_2K_5 = a_2 - a_0 \quad K_3 = a_2 \quad K_4K_5 = 1 + b_1 + b_0 \quad K_5K_6 = 1 - b_0$$

- Additional constraint can be made by

$$K_4 = K_5 = \sqrt{1 + b_1 + b_0}$$

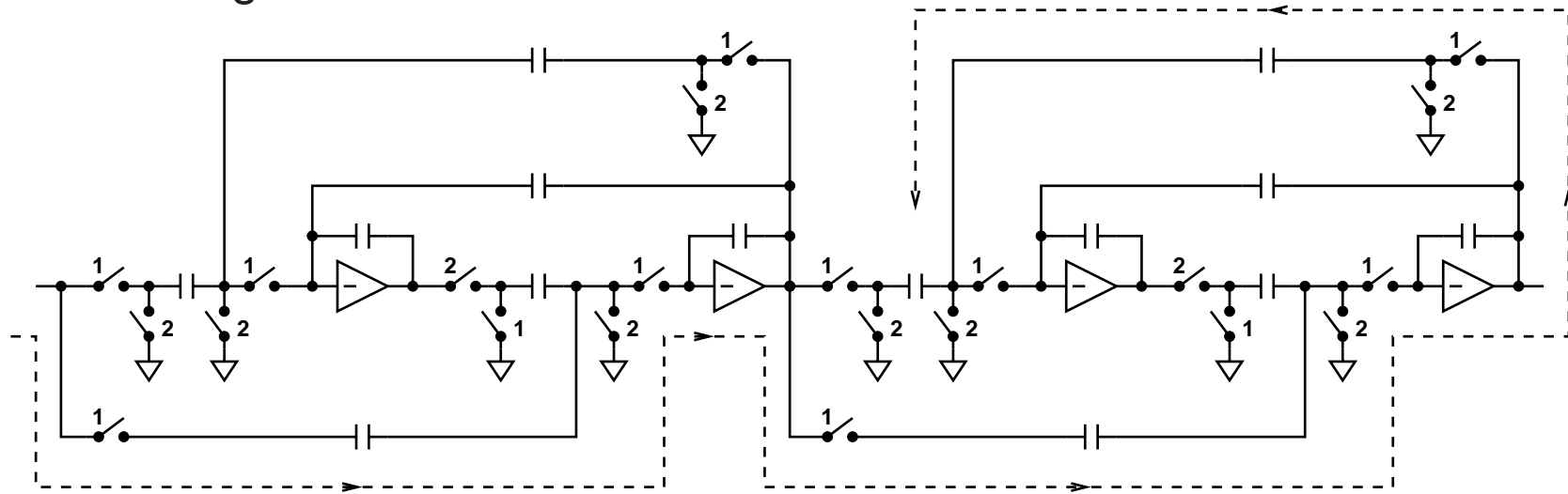
- Less capacitance spread.

In general,

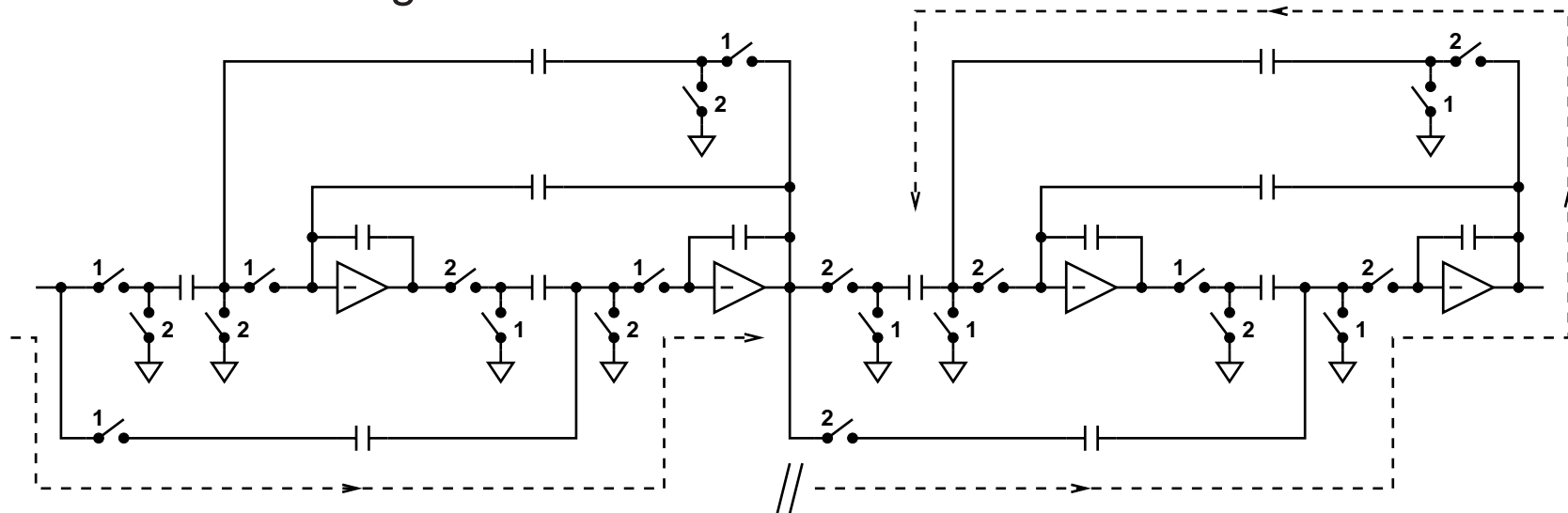
- For the SC biquad, it is important that the two-integrator loop have a single delay around the loop. A delay-free loop may have an excessive settling time behavior, while two delays around the loop cause difficulties in designing high-Q circuit.

# Time-Staggered SC Stages

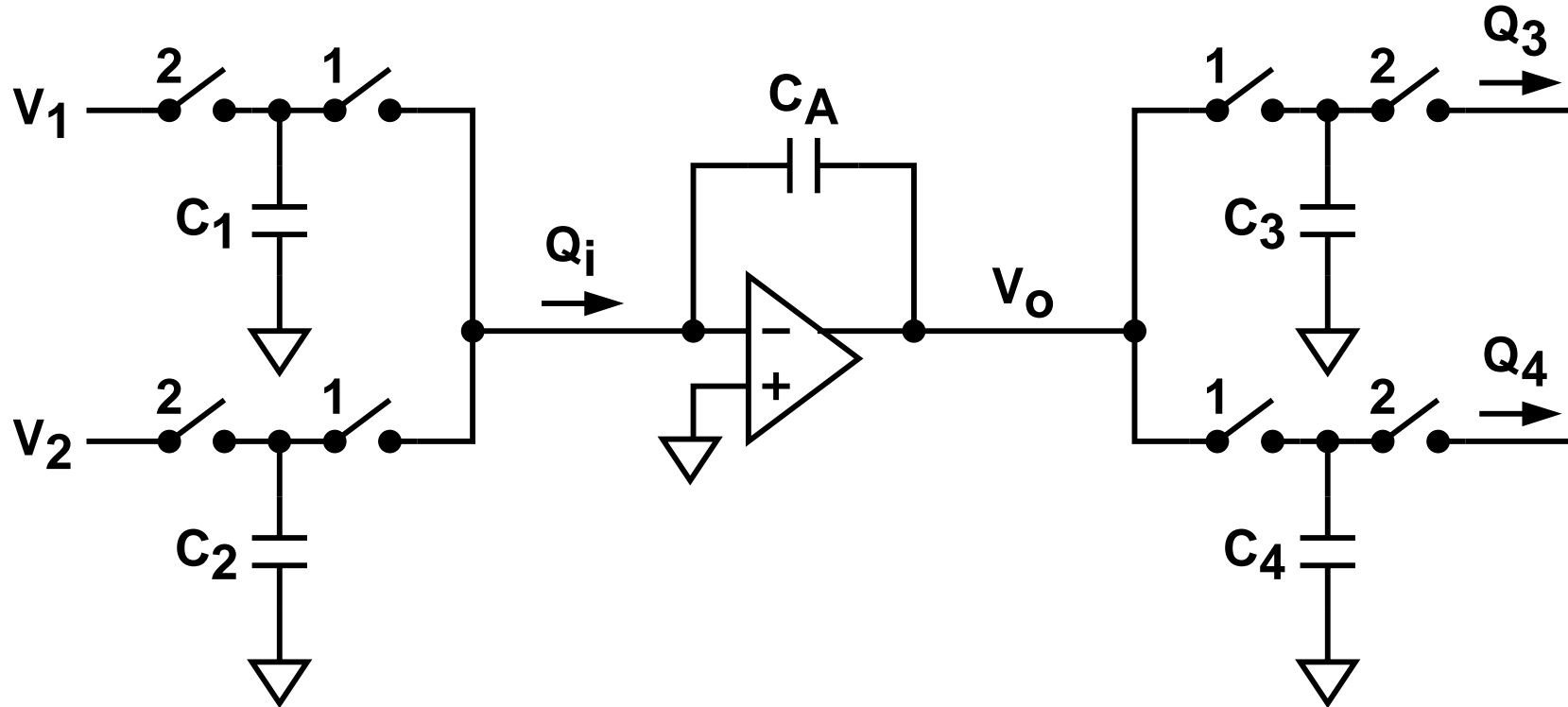
## Cascaded SC Stages



## Staggered Cascaded Stages



# Capacitor Scaling



For each switching cycle

$$Q_i = C_1 V_1 + C_2 V_2$$

$$\Delta V_o = -\frac{Q_i}{C_A}$$

$$Q_3 = C_3 V_o \quad Q_4 = C_4 V_o$$

## Output Capacitor Scaling

---

If  $C'_A = kC_A$ ,  $C'_3 = kC_3$ ,  $C'_4 = kC_4$ ,  $C_1$  and  $C_2$  unchanged, then

$$Q'_i = C_1V_1 + C_2V_2 = Q_i$$

$$\Delta V'_o = -\frac{Q'_i}{C'_A} = -\frac{Q_i}{kC_A} = \frac{\Delta V_o}{k}$$

$$Q'_3 = C'_3V'_o = kC_3\frac{V_o}{k} = Q_3 \quad Q'_4 = Q_4$$

- If the values of all capacitors (including feedback capacitors) connected or switched to the *output* terminal of an opamp in an SCF are multiplied by the same constant  $k$ , then the output voltage of this opamp will be divided by  $k$ ; all other opamp output voltages remain unchanged. This follows since the described changes leave all charges flowing to and from the affected opamp unchanged.
- The output capacitor scaling technique can be used to achieve optimum *scaling for maximum dynamic range*.

# Input Capacitor Scaling

---

If  $C'_A = kC_A$ ,  $C'_1 = kC_1$ ,  $C'_2 = kC_2$ ,  $C_3$  and  $C_4$  unchanged, then

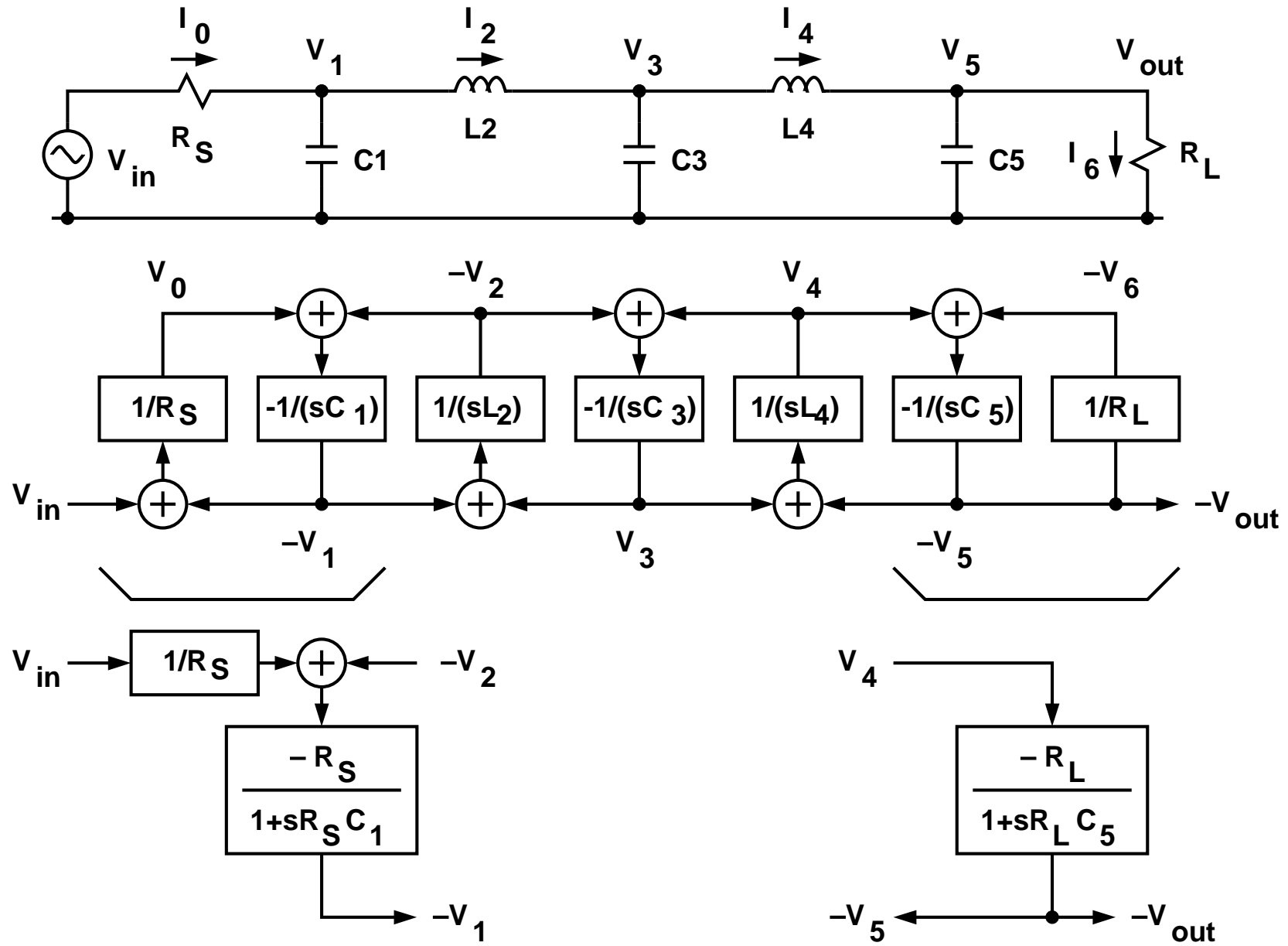
$$Q'_i = C'_1V_1 + C'_2V_2 = kC_1V_1 + kC_2V_2 = kQ_i$$

$$\Delta V'_o = -\frac{Q'_i}{C'_A} = -\frac{kQ_i}{kC_A} = \Delta V_o$$

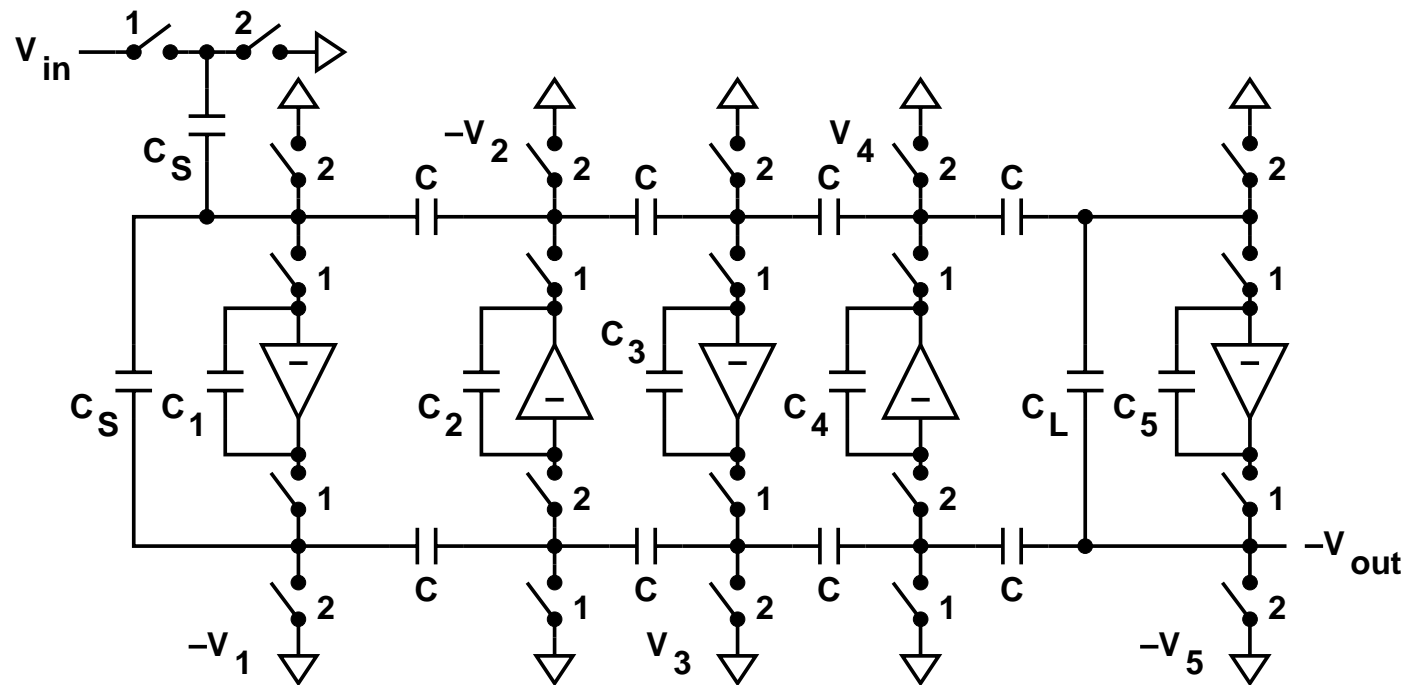
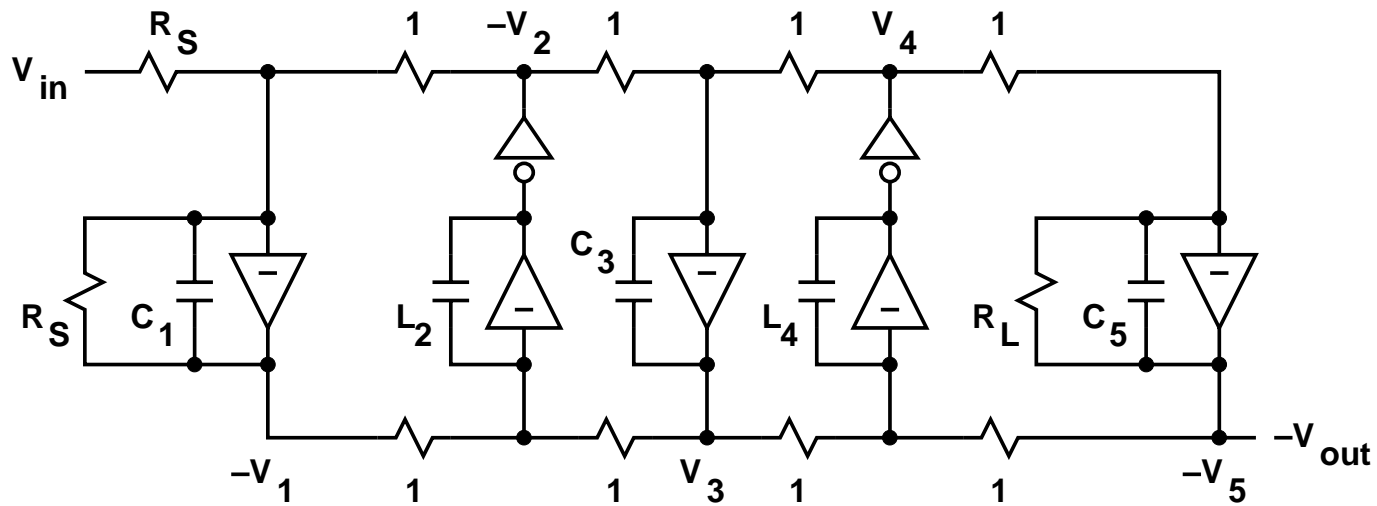
$$Q'_3 = C_3V'_o = C_3V_o = Q_3 \quad Q'_4 = Q_4$$

- If the values of all capacitors (including feedback capacitors) connected or switched to the inverting *input* terminal of an opamp are multiplied by the same constant, then all voltages in the SCF remain unchanged. This is true since all voltages are affected only by the ratios of these capacitances.
- The input capacitor scaling technique can be used to achieve optimum *scaling for minimum capacitance*.

# An All-Pole Low-Pass Ladder Filter

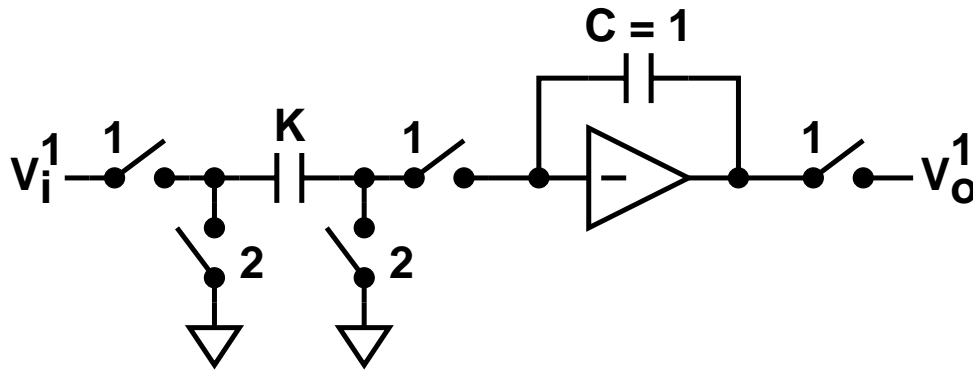


# An All-Pole Low-Pass SC Ladder Filter



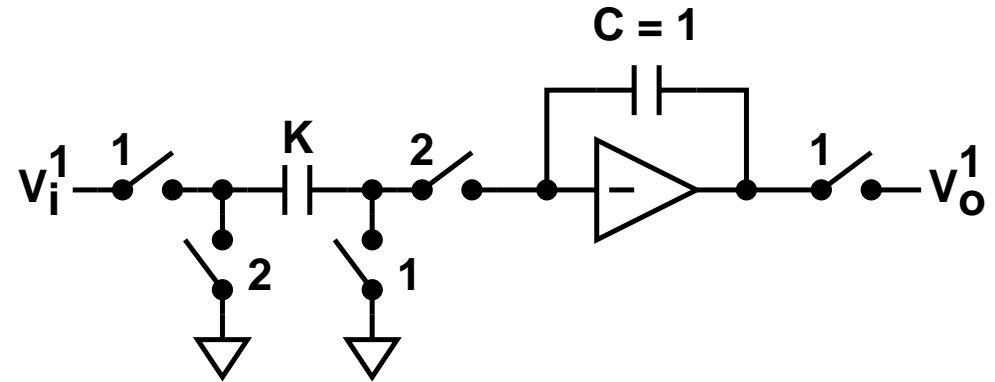
# SC Ladder Filter Using Signal-Flow Graph

Inverting BE Integrator



$$H_{BE}(z) = -K \cdot \frac{1}{1 - z^{-1}}$$

Noninverting FE Integrator



$$H_{FE}(z) = +K \cdot \frac{z^{-1}}{1 - z^{-1}}$$

- $H_{BE}(z)$  is a Backward-Euler (BE) integrator.  $H_{FE}(z)$  is a Forward-Euler (FE) integrator.
- The phase errors of the integrators are cancelled in the ladder topology, while the magnitude errors can cause deviations in the frequency response when  $\omega T_s \ll 1$  is no longer true.
- The SC ladder filters are inherently time-staggering.

# SC Ladder Filters Design Methodology

---

It is possible to realize the SC ladder filters with exact frequency response, using only the BE and FE integrators. The design procedures involves bilinear transformation prewarping and frequency-dependent impedance scaling.

$$\lambda = \frac{s'T_s}{2} = \frac{z^{1/2} - z^{-1/2}}{z^{1/2} + z^{-1/2}} = \tanh \frac{sT_s}{2}$$
$$\gamma = \frac{1}{2} \left( z^{1/2} - z^{-1/2} \right) = \sinh \frac{sT_s}{2} \quad \mu = \frac{1}{2} \left( z^{1/2} + z^{-1/2} \right) = \cosh \frac{sT_s}{2}$$
$$\Rightarrow \quad \lambda = \frac{\gamma}{\mu} \quad \mu^2 - \gamma^2 = 1 \quad z^{1/2} = \mu + \gamma$$

- $\lambda \leftrightarrow z$  is the bilinear (BL) transformation.
- $\gamma \leftrightarrow z$  is the lossless discrete (LD) transformation.
- The design goal is to implement  $H(z = e^{sT_s})$  with  $H(\gamma)$ .  $H(\gamma)$  can then be realized with SC integrators.

# SC Ladder Filters Design Procedures

---

1. Prewarp the filter specifications from  $\omega$  to  $\omega'$  with bilinear transformation.

$$\omega' = \frac{2}{T_s} \tan \frac{\omega T_s}{2}$$

2. Find  $H(s')$ . Renormalize  $H(s')$  into  $H(\lambda)$  by setting  $s'T_s/2 = \lambda$ .

3. Realized  $H(\lambda)$  as an LC ladder filter in  $\lambda$  domain.

4. Scale the impedance level,

$$Y(\gamma) = \mu Y(\lambda) \quad Z(\gamma) = Z(\lambda)/\mu$$

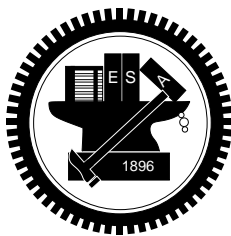
to obtain the  $\gamma$ -domain LC ladder circuit.

5. Implement the  $\gamma$ -domain circuit with SC circuits.

# Nyquist-Rate Digital-to-Analog Converters

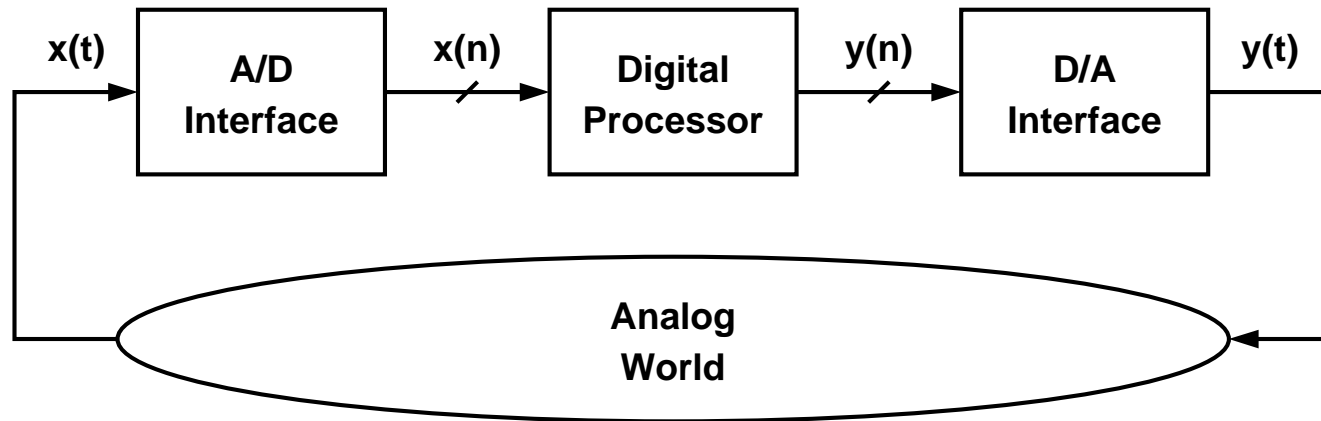
Jieh-Tsorng Wu

July 16, 2002

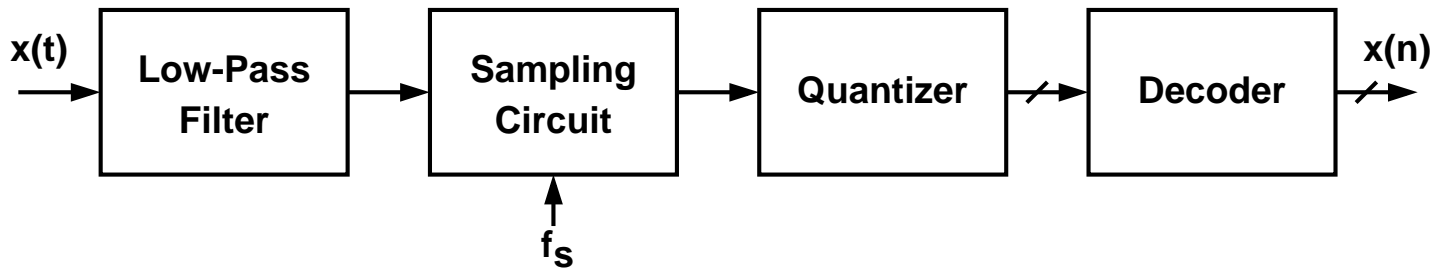


National Chiao-Tung University  
Department of Electronics Engineering

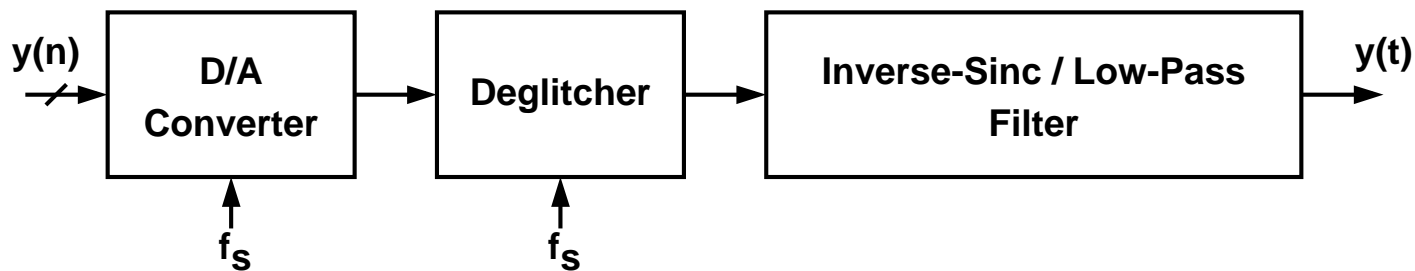
# A/D and D/A Interfaces



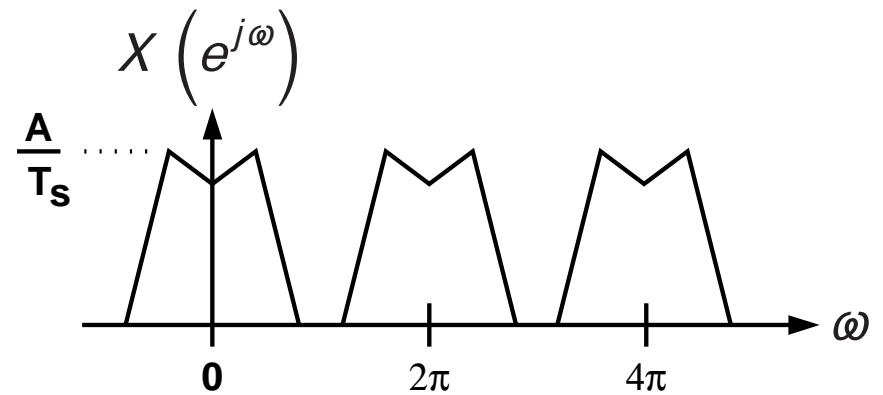
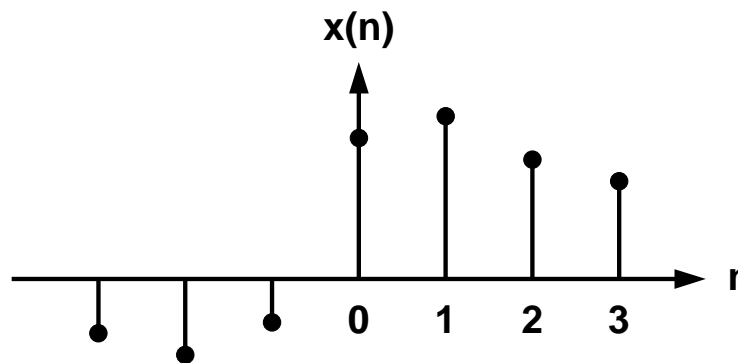
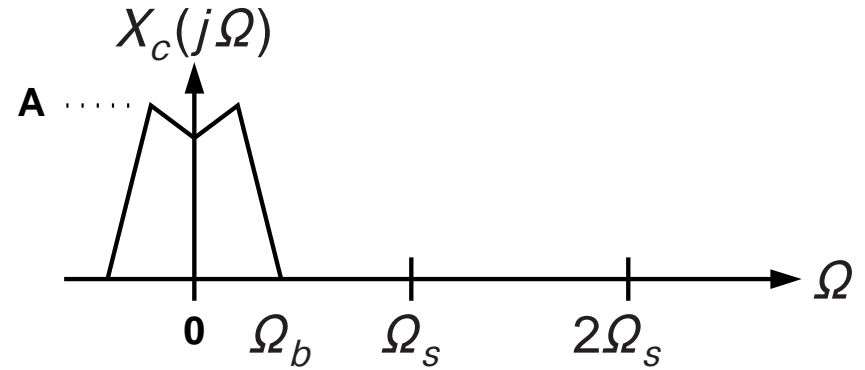
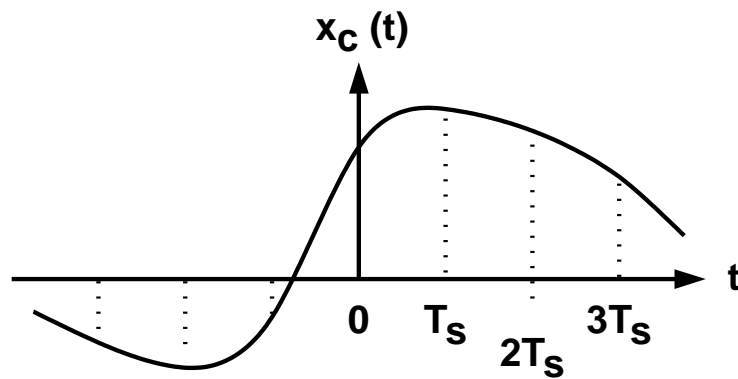
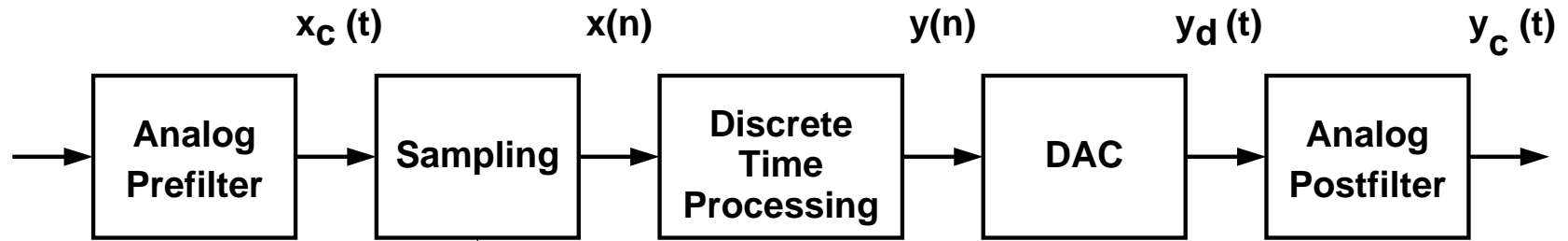
## Analog-to-Digital Interface



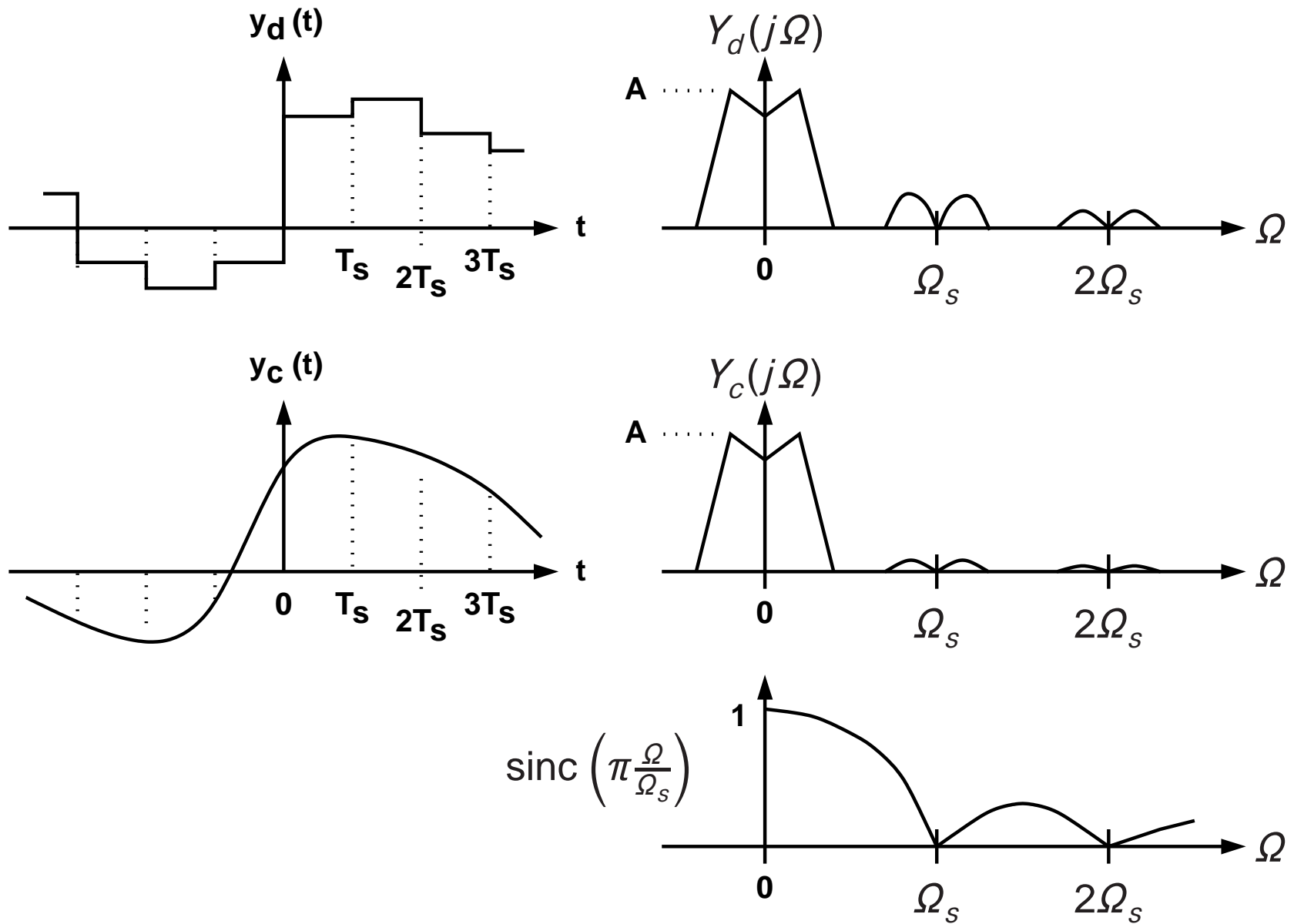
## Digital-to-Analog Interface



# Continuous-to-Discrete Conversion



# Discrete-to-Continuous Conversion



# Discrete-to-Continuous Conversion

---

The digital-to-analog converter (DAC) usually performs the discrete-to-continuous sample-and-hold translation, i.e.,

$$y_d(t) = \sum_{n=-\infty}^{\infty} y(n) \cdot \Pi(t - nT_s) \quad \text{where} \quad \Pi(t) = \begin{cases} 1 & \text{if } 0 < t < T_s \\ 0 & \text{otherwise} \end{cases}$$

The continuous-time Fourier transform (CTFT) of  $y_d(t)$  can be expressed as

$$Y_d(j\Omega) = Y_d(z)|_{z=e^{j\Omega T_s}} \times H_{da}(j\Omega) = Y_d(e^{j\omega})|_{\omega=\Omega T_s} \times H_{da}(j\Omega)$$

The discrete-to-continuous sample-and-hold transfer function is

$$H_{da}(s) = \frac{1 - e^{-sT_s}}{s} \quad H_{da}(j\Omega) = e^{-j\pi\Omega/\Omega_s} \cdot T_s \cdot \text{sinc}\left(\pi\frac{\Omega}{\Omega_s}\right)$$

$$\Omega_s = 2\pi f_s = \frac{2\pi}{T_s} \quad \text{sinc}(x) = \frac{\sin x}{x}$$

# Imperfections in Discrete-to-Continuous Conversion

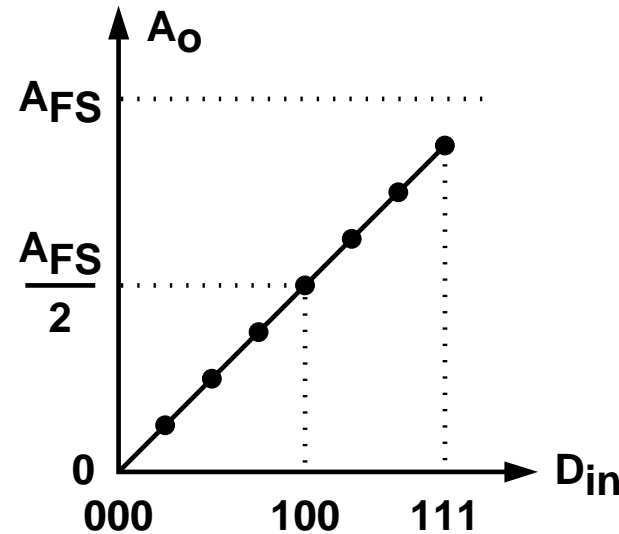
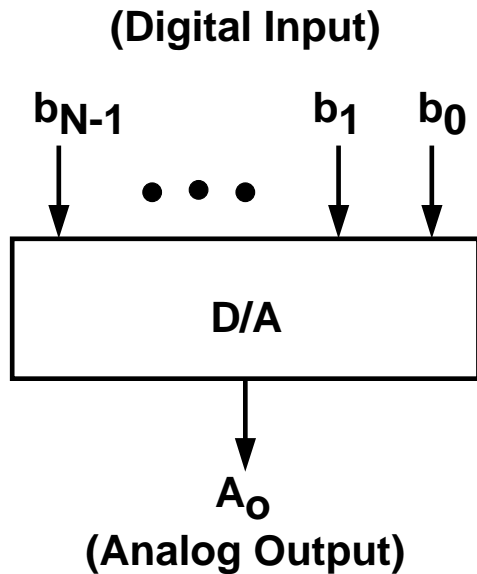
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The D/A conversion of  $y(n)$  can be expressed as:

$$y_d(t) = \sum_{n=-\infty}^{\infty} \hat{y}(n) \cdot C[t - nT_s + \epsilon]$$

- The  $y(n) \rightarrow \hat{y}(n)$  conversion may contain gain error, offset, and nonlinearity.
- $C(t)$  has transient behavior. Its pulse width can be larger than  $T_s$ .
- $C(t)$  may contain  $y(n)$  dependency.
  - A return-to-zero  $C(t)$  can reduce the  $y(n)$  dependency.
- The timing jitter  $\epsilon$  can be random or deterministic.

# D/A Transfer Characteristic



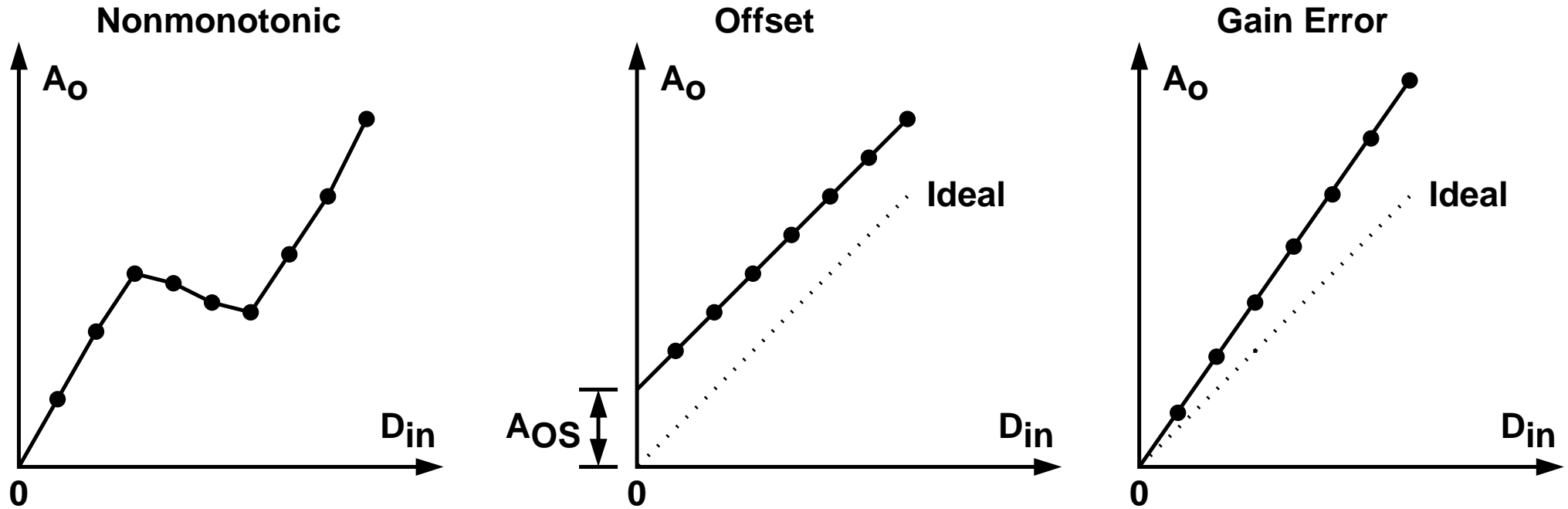
$A_{FS}$  = Full-Scale Output

$$\Delta = \text{LSB} = \text{Step Size} = \frac{A_{FS}}{2^N}$$

$$\begin{aligned} A_o &= \Delta \times D_{in} \\ &= \Delta \times [b_{N-1}2^{N-1} + \dots + b_12^1 + b_02^0] \\ &= A_{FS} \times [b_{N-1}2^{-1} + \dots + b_12^{-(N-1)} + b_02^{-N}] \end{aligned}$$

- In some applications, relationship between  $D_{in}$  and  $A_o$  can be nonlinear.
- $D_{in}$  may use other coding scheme such as offset binary or 2's complement.

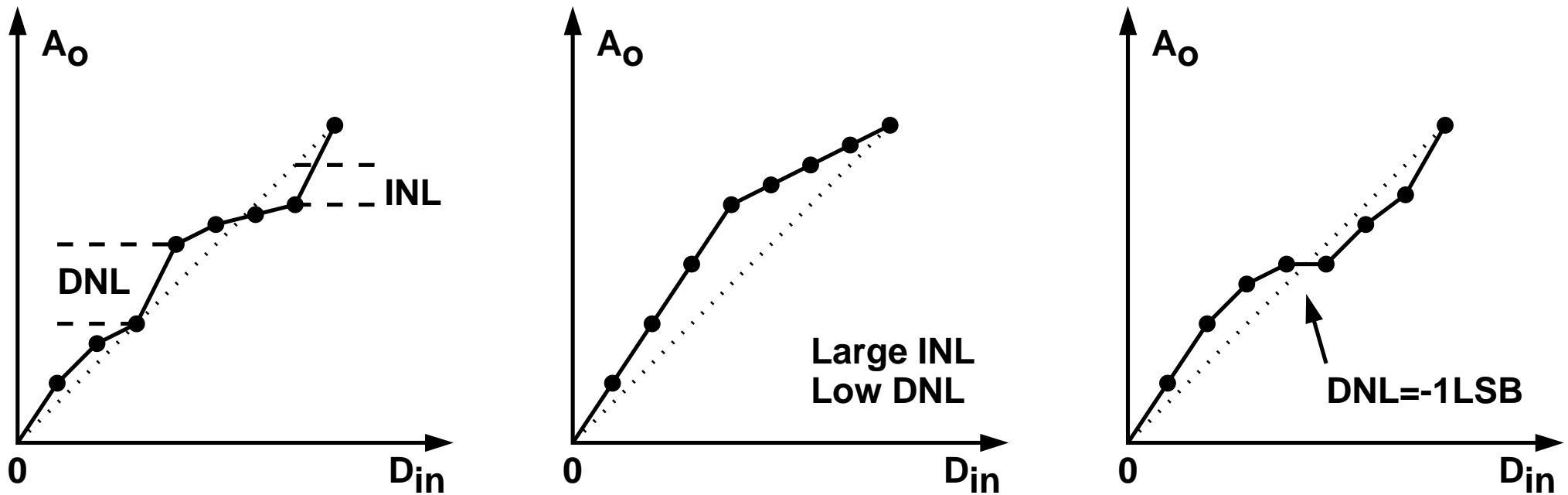
# D/A Transfer Characteristic



$$\text{Offset Error} = \frac{A_{OS}}{\Delta} \quad A_{OS} = A_o|_{D_{in}=0}$$

$$\text{Gain Error} = \frac{A_{o,max} - A_{OS}}{\Delta \cdot (2^N - 1)} = \frac{A_{o,max} - A_{OS}}{A_{FS} \cdot (1 - 2^{-N})}$$

## D/A Nonlinearity



- Measure of deviation from straight line with offset and gain error corrected.
- **Differential nonlinearity (DNL):** Maximum deviation of the analog output *step* from the ideal value of 1 LSB ( $= \Delta$ ).
- **Integral nonlinearity (INL):** Maximum deviation of the analog output from the ideal value.

# D/A Performance Metrics — Static Characteristics

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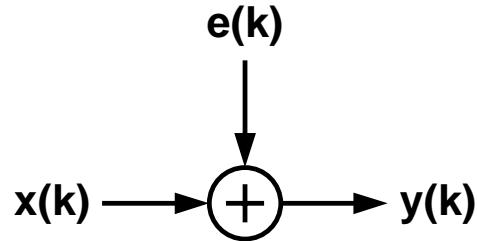
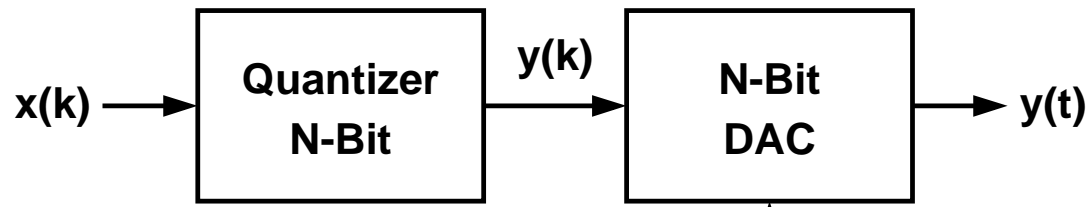
- Resolution: number of bits (N), analog 1 LSB step ( $\Delta$ ).
- Offset error.
- Gain error.
- Integral nonlinearity (INL).
- Differential nonlinearity (DNL).
- Monotonicity.
  - Monotonicity can be assumed if the  $DNL > -1$  LSB.
- Stability.
  - Variation with time, temperature, and supply voltage.

# D/A Performance Metrics — Dynamic Characteristics

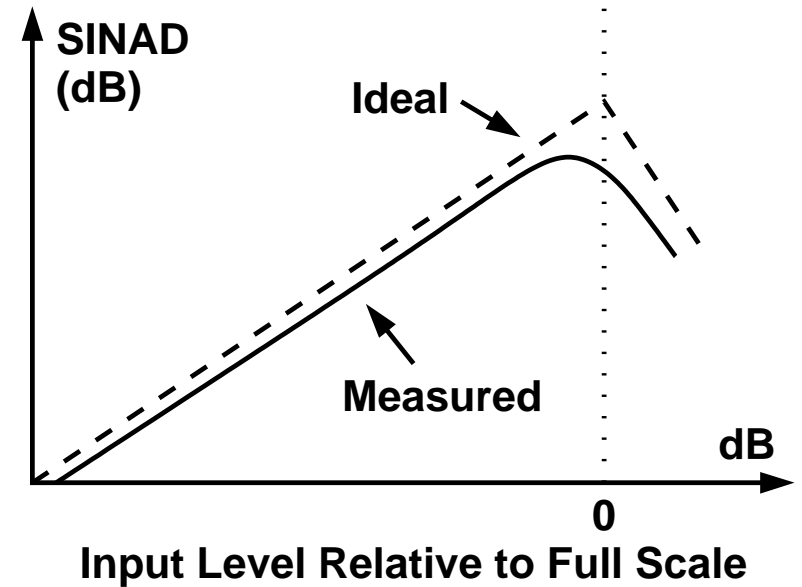
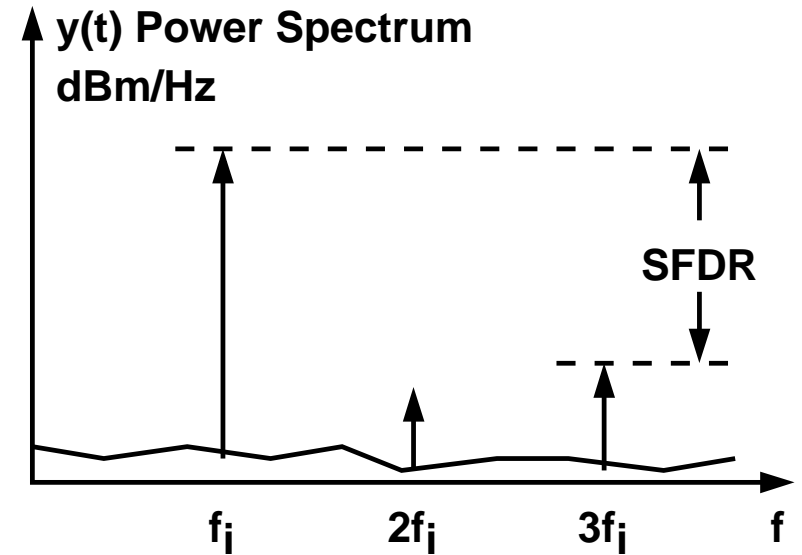
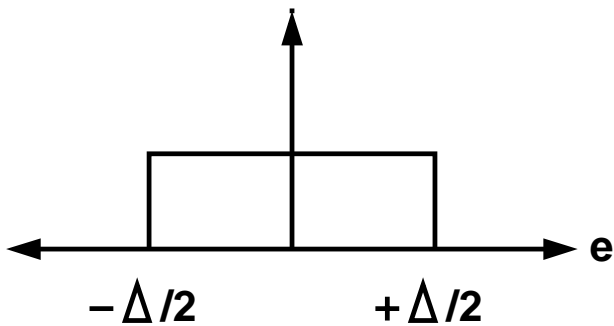
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- Sampling rate.
- Settling time.
  - Settling time is the time taken by the D/A output to settle within some specified error band (typically  $\pm\frac{1}{2}$  LSB).
  - The settling time is primarily dominated by the settling of the MSB contribution.
- Glitch impulse area (glitch energy).
  - Glitches is the output transient spikes during the conversion process.
  - Glitches are caused by the unequal delays in switching various signal sources within the converter.
- Dynamic range:  $\text{SNR}_{max}$ , SFDR, SINAD.

# Dynamic Range



Probability Density Function (pdf)



# Dynamic Range

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$e(k)$  is a *quantization noise* due to the quantization process.

$$e(k) \equiv y(k) - x(k) \quad \text{Noise Power} = P_n = \int e^2 \text{pdf}(e) de = \frac{1}{12} \Delta^2$$

Let the input  $x(k)$  be a sinusoidal waveform

$$x(k) = A \sin(2\pi f_i \cdot kT_s) \quad \text{Signal Power} = P_s = \frac{1}{2} A^2$$

The signal-to-noise ratio of  $y(k)$  is

$$\text{SNR} \equiv \frac{P_s}{P_n} = 6 \cdot \frac{A^2}{\Delta^2}$$

When the input's amplitude  $A = A_{FS}/2$ , the SNR reaches its maximum value.

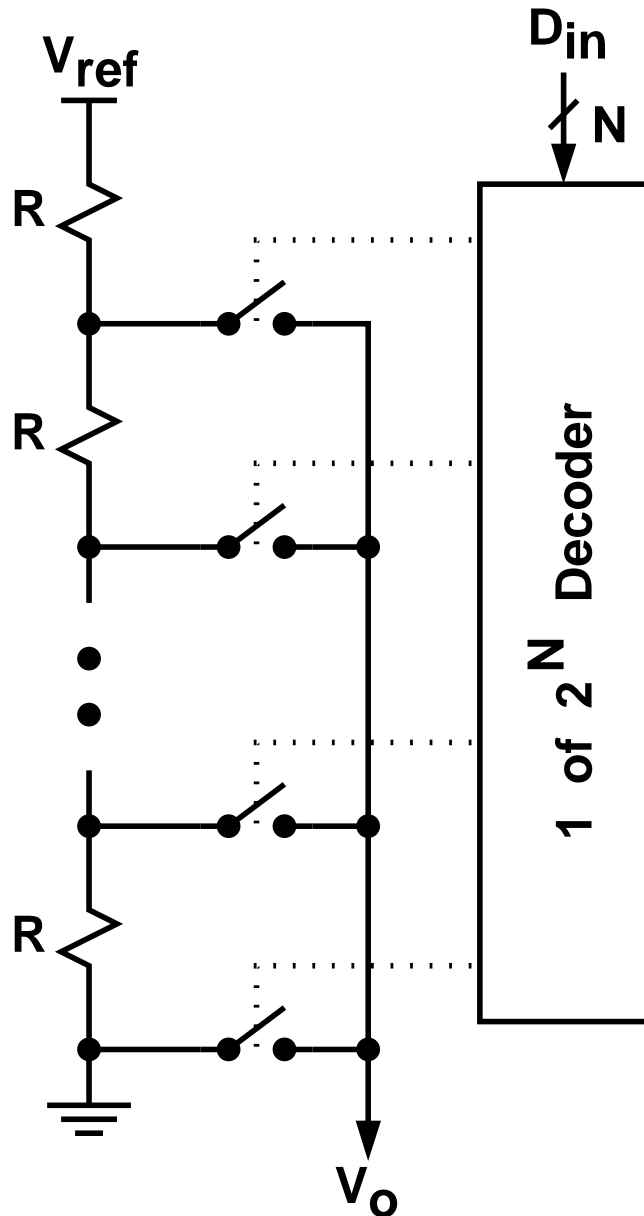
$$A_{FS} = 2^N \Delta \quad P_s = \frac{1}{8} \cdot 2^{2N} \Delta^2 \quad \text{SNR}_{max} = 2^{2N} \times \frac{3}{2} = N \times 6.02 \text{ dB} + 1.76 \text{ dB}$$

# Dynamic Range

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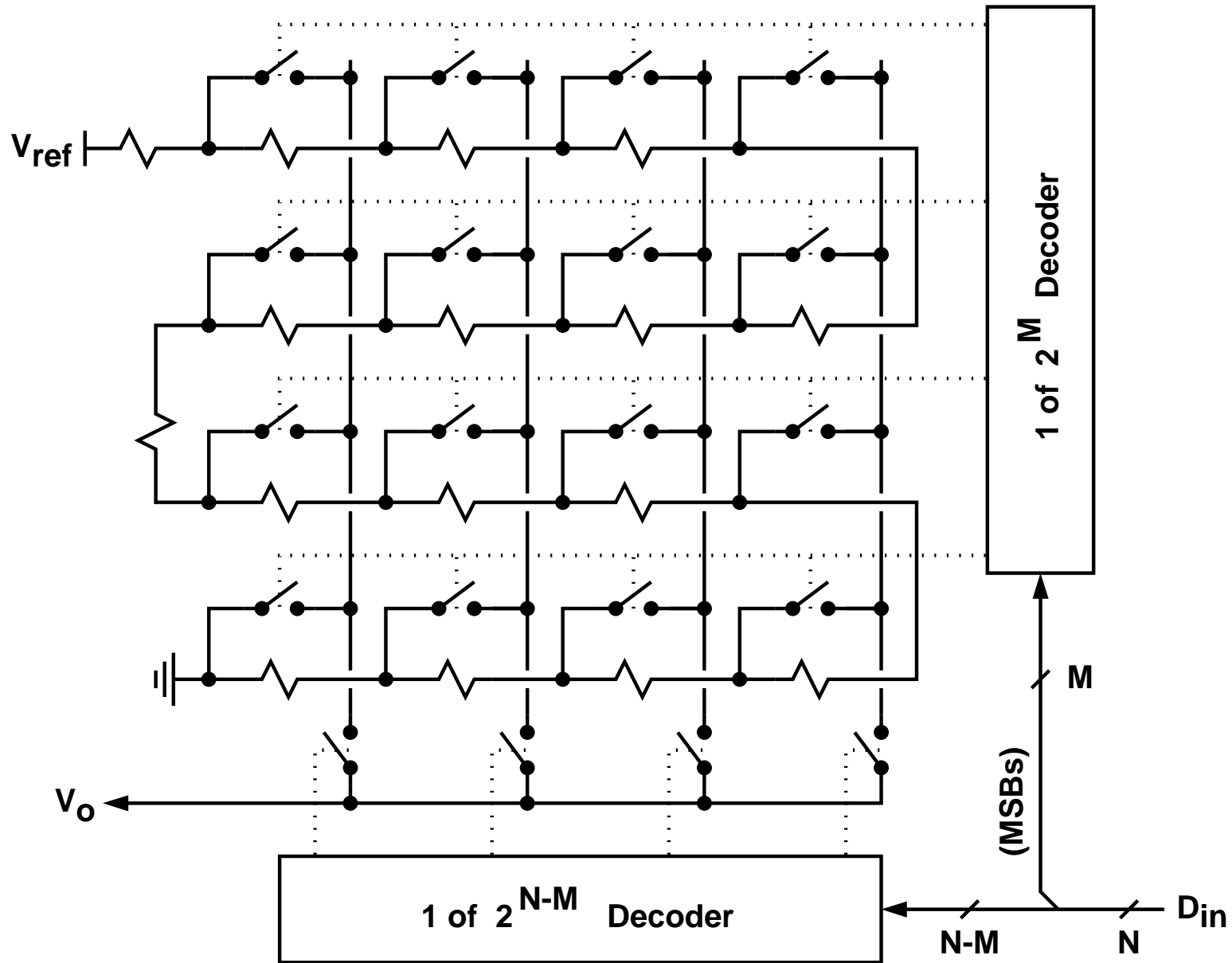
- The ratio between  $f_s$  and  $f_j$  should be irrational.
- In the discrete-time domain, noise power of  $e(k)$  is assumed to be uniformly distributed between  $-\Omega_s/2$  and  $+\Omega_s/2$ . The power density is  $\Delta^2/(12\Omega_s)$ .
- The *spurious free dynamic range* (SFDR) is the ratio of the fundamental signal component to the largest distortion component when  $A = A_{FS}/2$ .
- The *signal-to-noise plus distortion ratio* (SINAD) is the ratio of power of the fundamental signal to the total power of noise and distortion when  $A = A_{FS}/2$ .
- The *total harmonic distortion* (THD) is the ratio of the total power of the 2nd and higher harmonic components to the power of the fundamental signal.
- In finding the total noise power, the noise bandwidth need to be specified.

# Resistor-String DACs with Digital Decoding

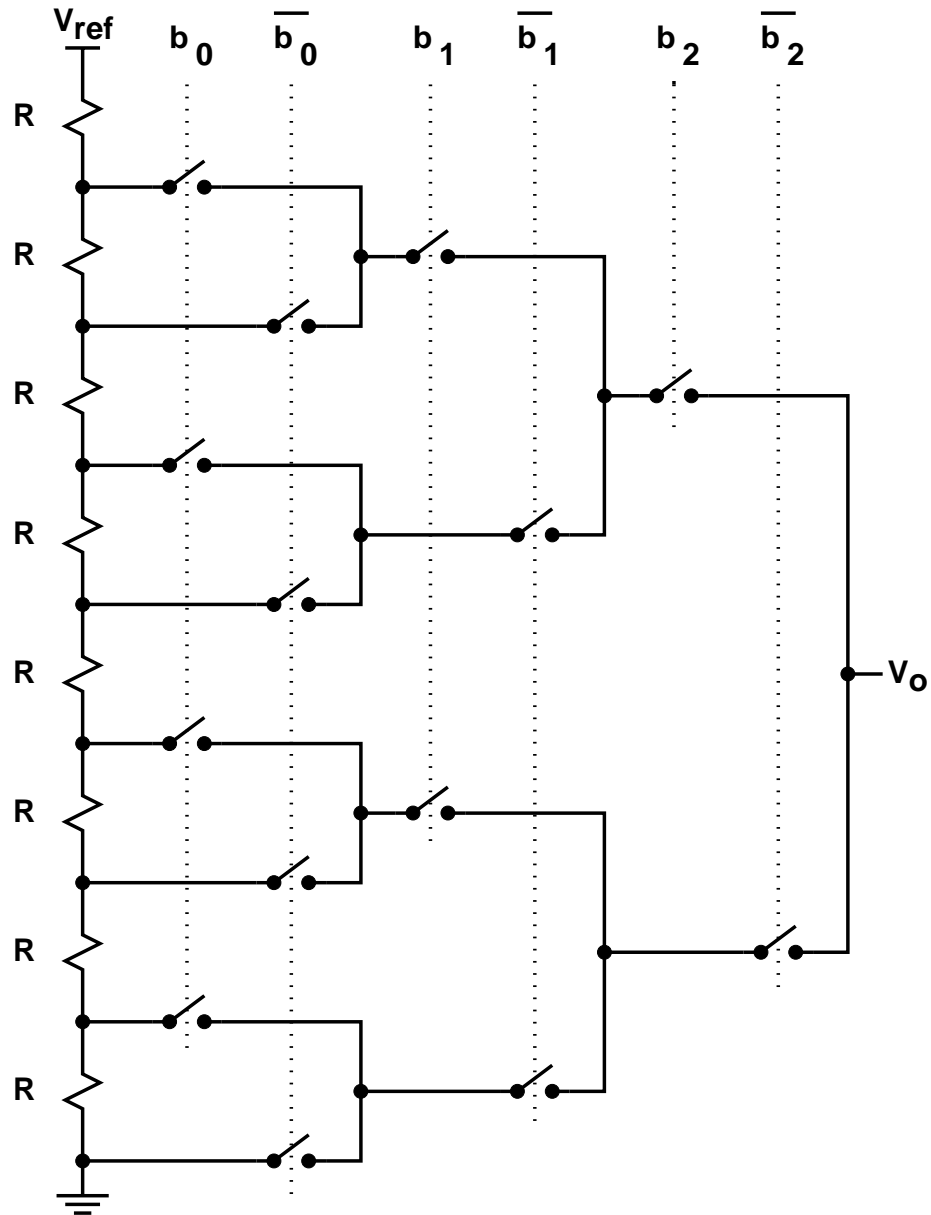


- Inherently monotonic.
- DNL depend on local matching of neighboring R's.
- INL depends on global matching of the R-string.
- No resistive load at  $V_o$ .
- The worst-case time constant occurs a the midpoint of the R-string.
- Large capacitive loading at  $V_o$ .

# Folded R-String DACs with Digital Decoding

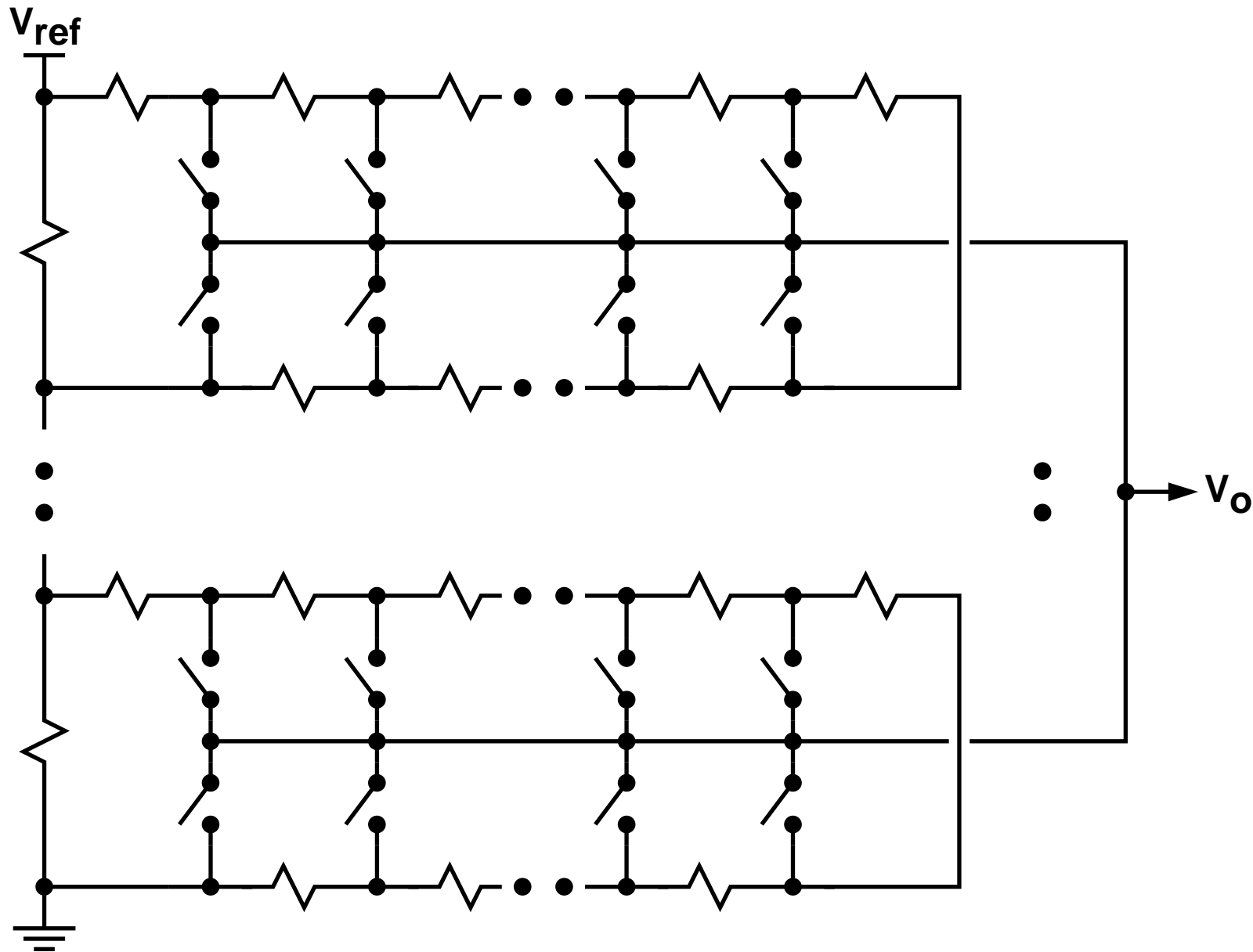


# R-String DACs with Binary-Tree Decoding

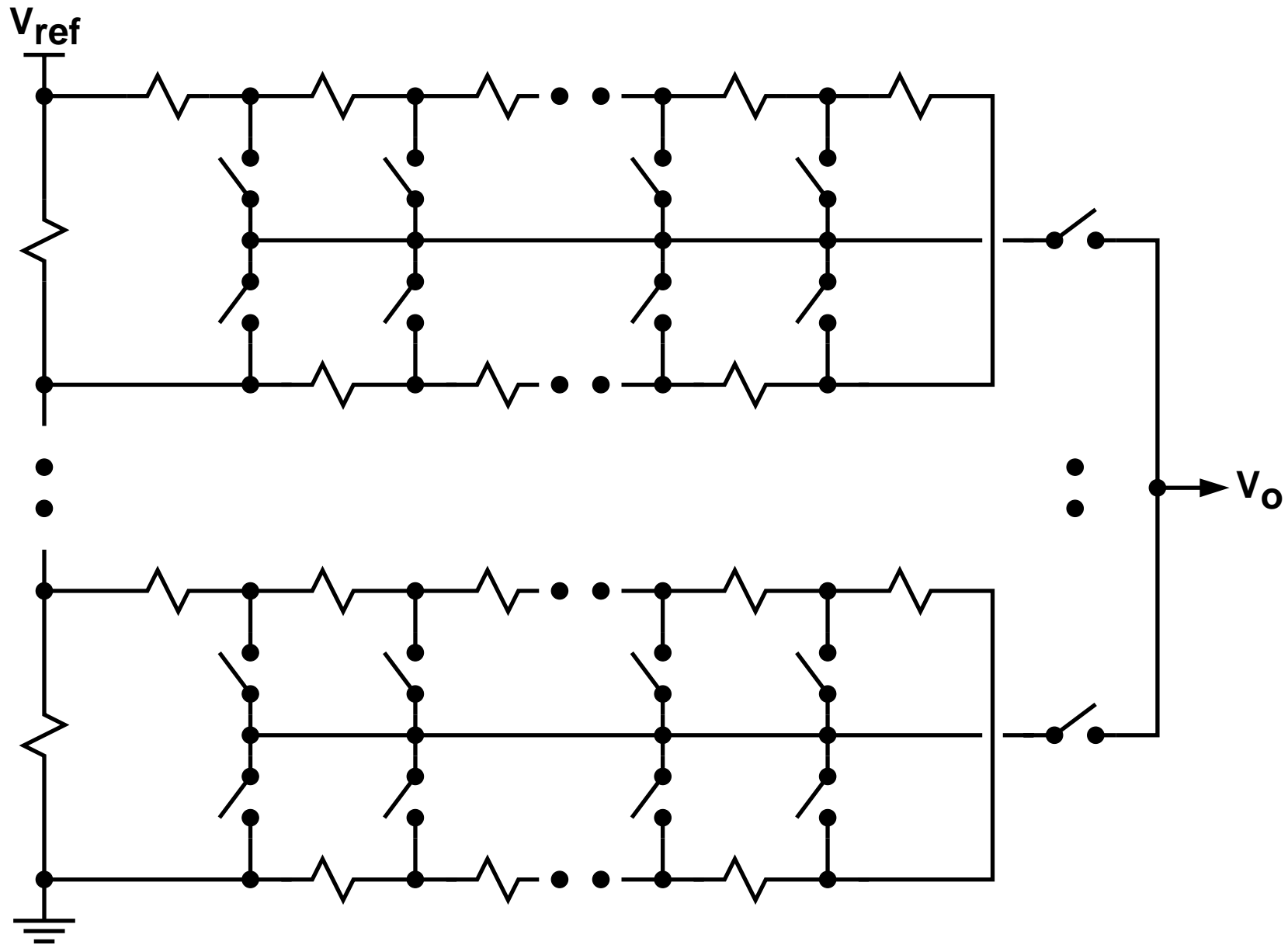


- Require no digital decoder.
- Speed is limited by the delay through the resistor string as well as the delay through the switch network.

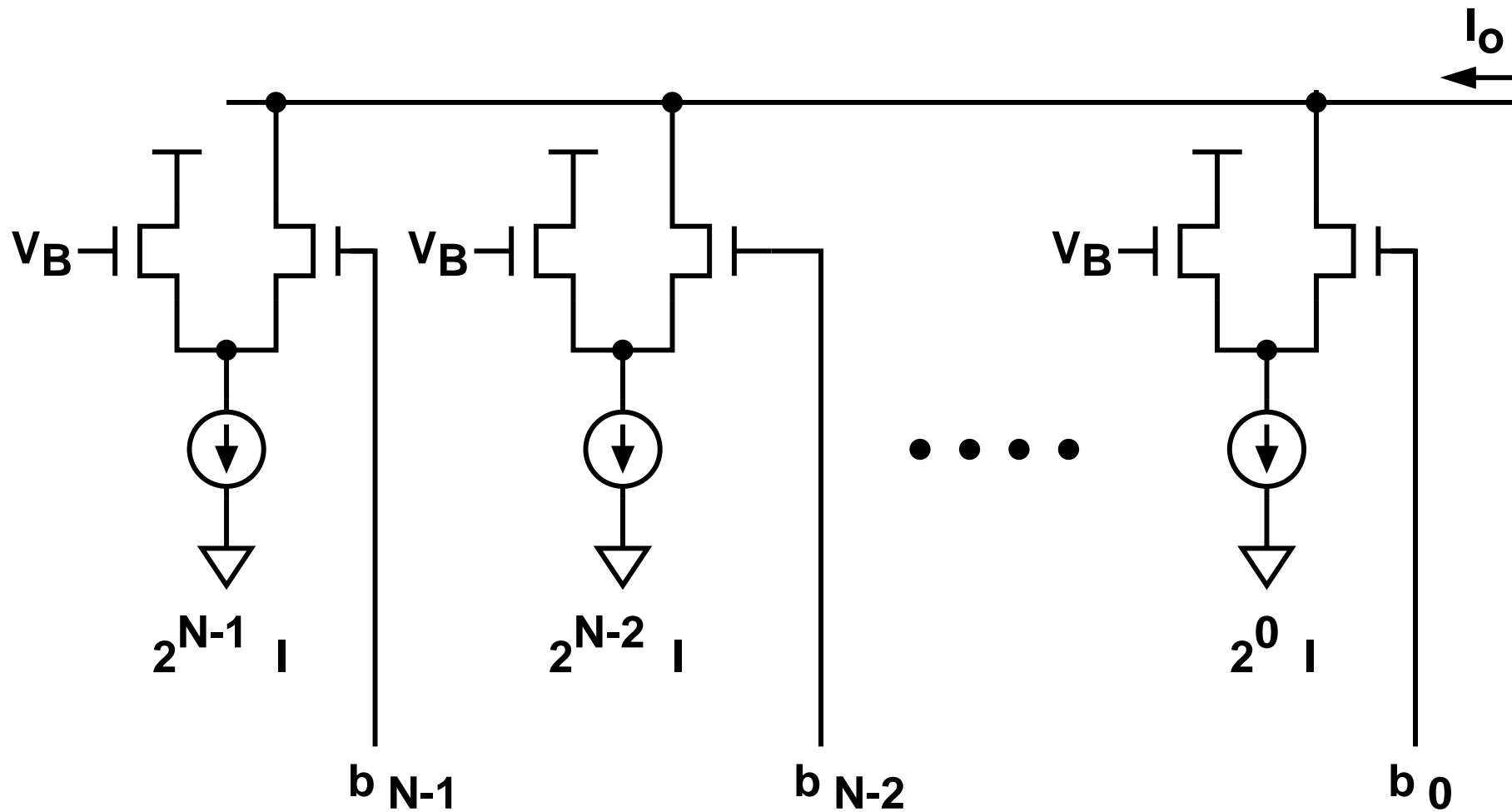
# Intermeshed Resistor-String DACs (One-Level Multiplexing)



# Intermeshed Resistor-String DACs (Two-Level Multiplexing)



# Binary-Weighted Current-Steering DACs

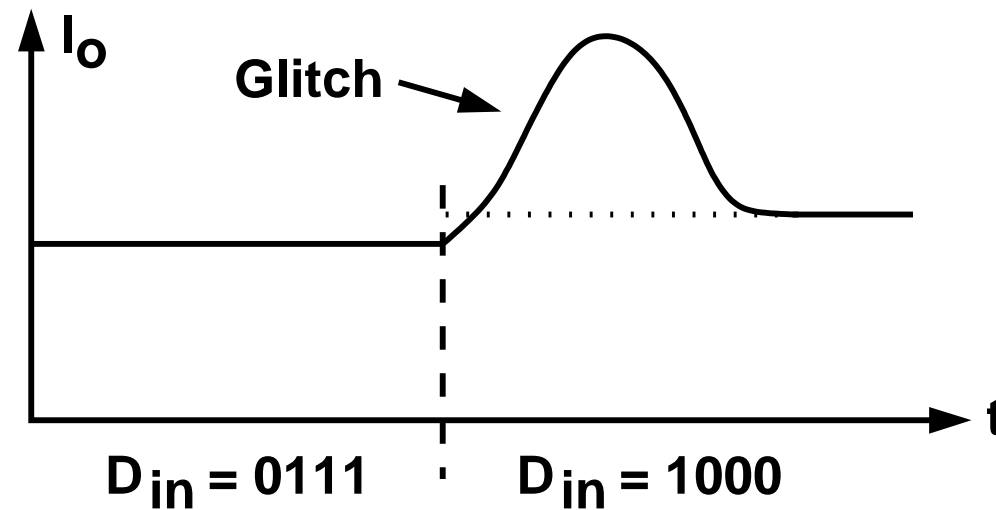


$$I_o = I \cdot (b_{N-1} \cdot 2^{N-1} + b_{N-2} \cdot 2^{N-2} + \dots + b_1 \cdot 2^1 + b_0 \cdot 2^0)$$

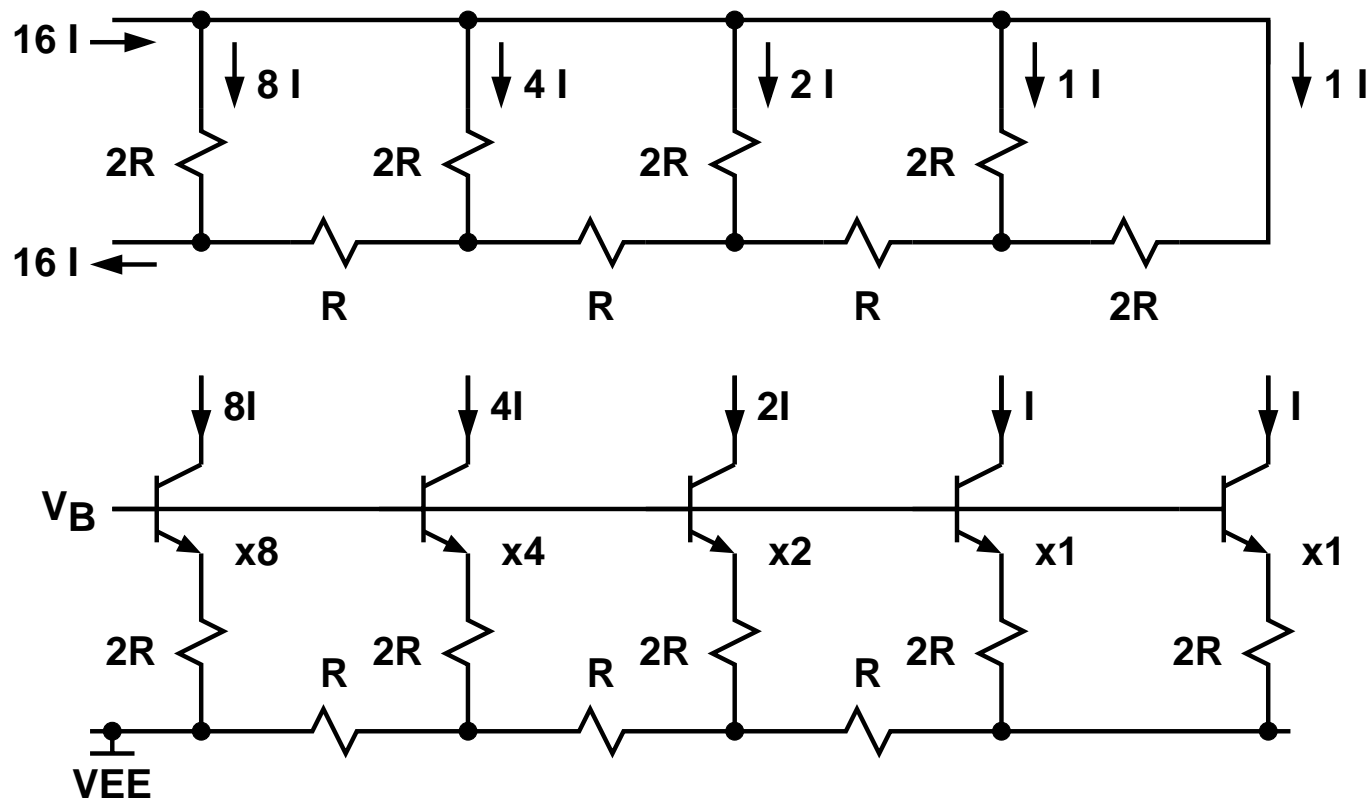
# Binary-Weighted Current-Steering DACs

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- Fast.
- Monotonicity is not guaranteed.
- Potentially large glitches due to timing skews.
- Latches are often used to synchronize  $b_{N-1}, b_{N-2}, \dots$
- $R_o$  of the current sources can cause nonlinearity.

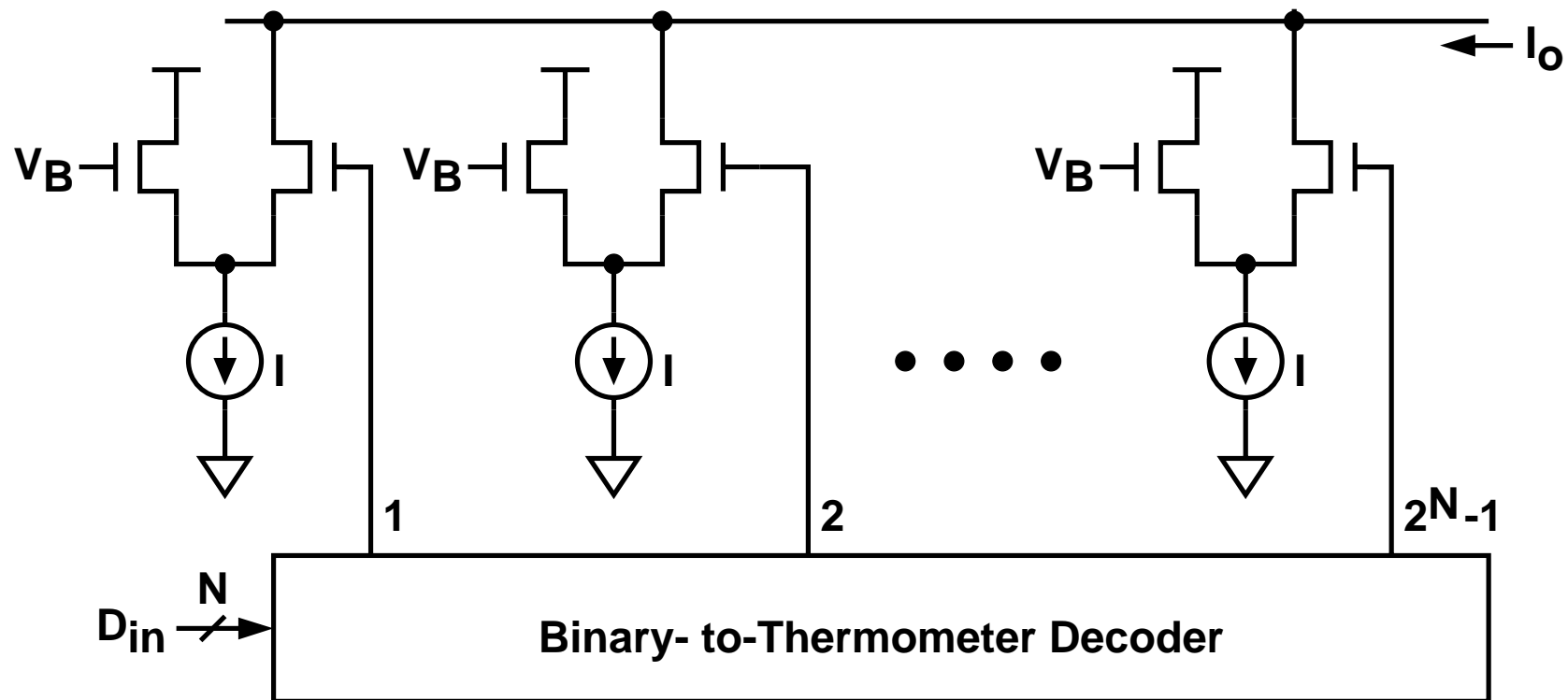


# Binary-Weighted R-2R Networks



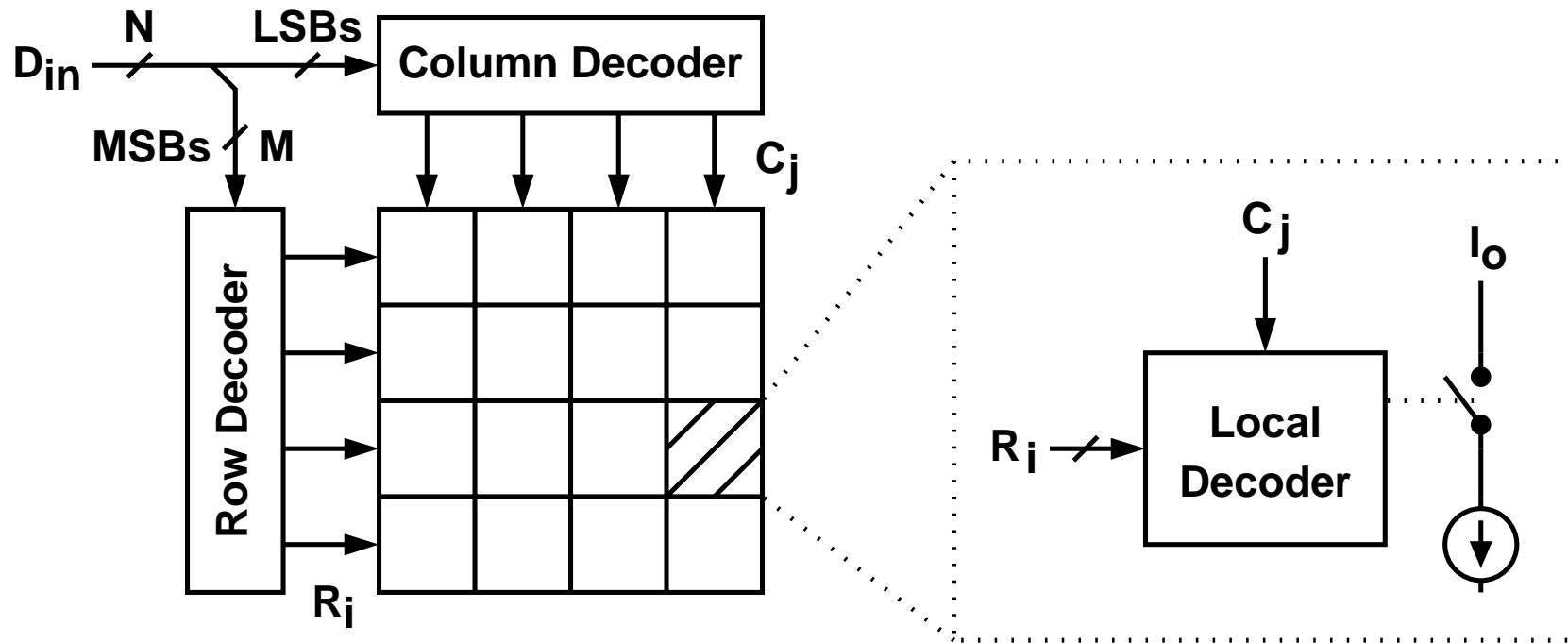
- No wide-range scaling of resistors.
- BJT emitter-area scaling can be confined to the first few MSBs; and the voltage drops in the emitter resistors should dominate the  $V_{BE(on)}$  mismatches of the less significant bits.

# Equally-Weighted Current-Steering DACs



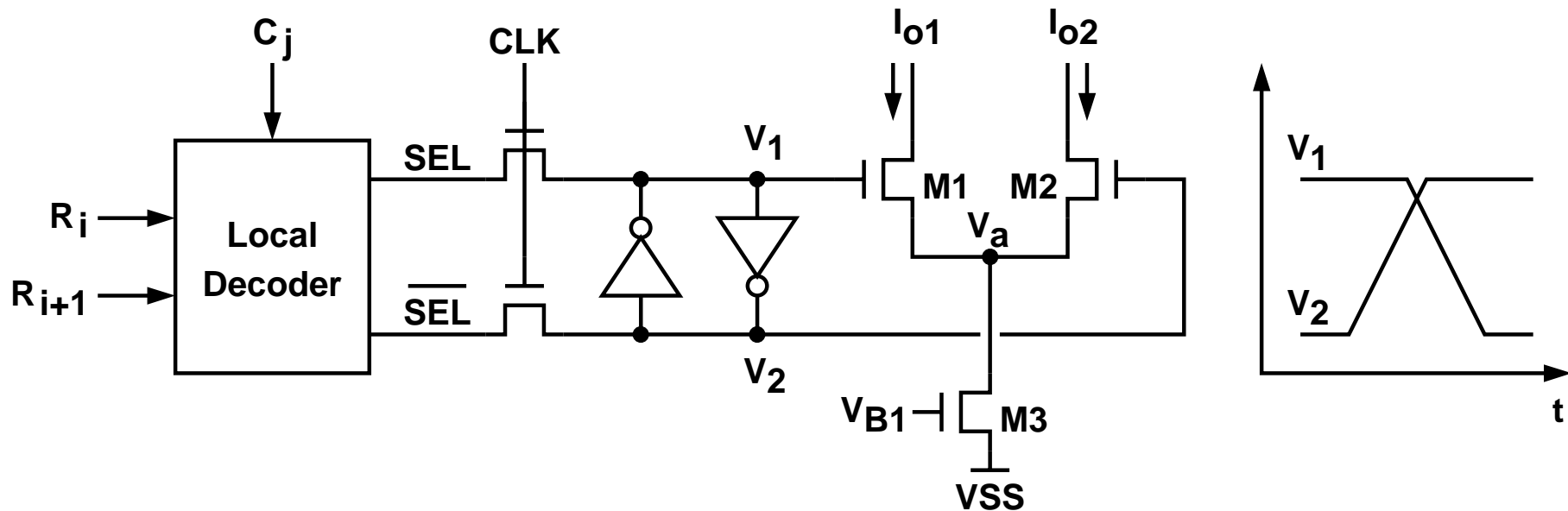
- Inherently monotonic.
- Glitches are reduced. Synchronizing latches may be still required.

# The Matrix Floorplan



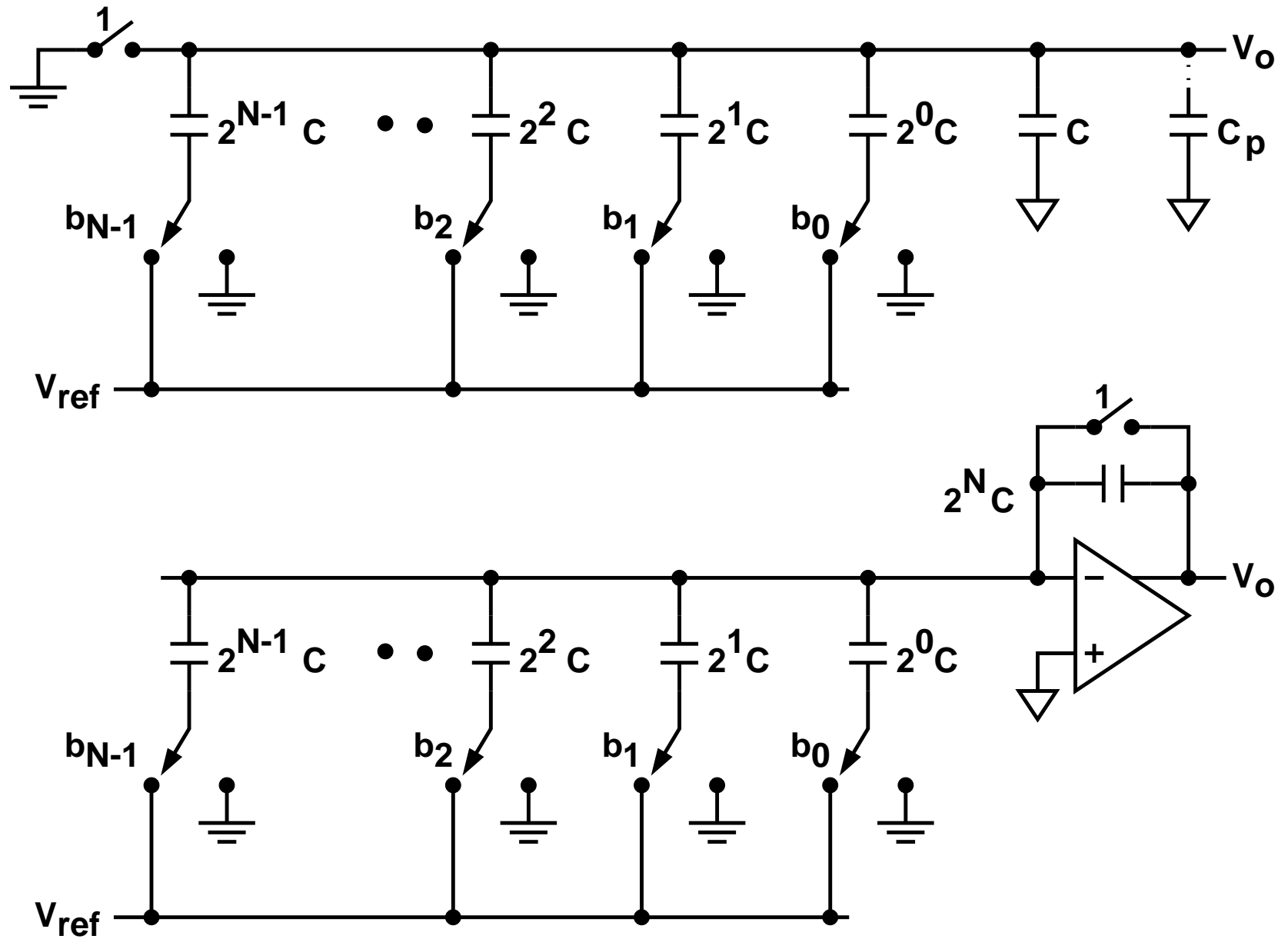
- $R_j$  is a  $2^M - 1$  thermometer code, and  $C_j$  is a  $2^{N-M} - 1$  thermometer code.
- One example of the local decoding is  $S = R_{i+1} + R_i \cdot C_j$ .
- INL may exhibit the gradient of the unit cell's variations.
- INL can be *dithered* by jumping selection of unit cells.

# A Current Cell Example



- The current switch MOSTs,  $M1$  and  $M2$ , are in the triode region when fully turned on.
- To minimize voltage fluctuation at  $V_a$ , the inverters are sized so that the cross-over voltage of the  $V_1$  and  $V_2$  transient waveforms can turn on both  $M1$  and  $M2$ .
- Reference: C-H Lin and K Bult, "A 10-b, 500-MSample/s CMOS DAC in  $0.6 \text{ mm}^2$ ," JSSC, 12/1998, pp. 1948–1958.

# Charge-Redistribution DACs



# Charge-Redistribution DACs

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During  $\phi_1 = 1$ ,

Cap Bottom Plate @ GND

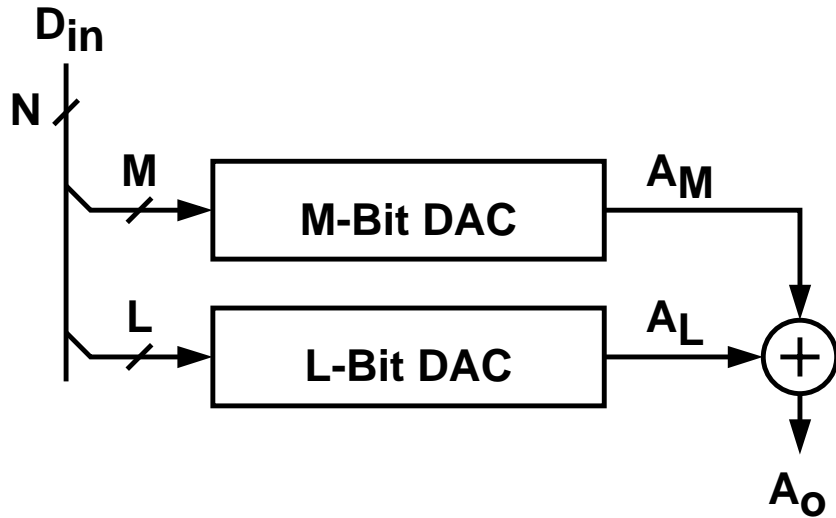
$$V_o = 0$$

During  $\phi_2 = 1$ ,

$$b_i = \begin{cases} 1 & \rightarrow \text{Cap Bottom Plate @ } V_{ref} \\ 0 & \rightarrow \text{Cap Bottom Plate @ GND} \end{cases} \quad V_o = V_{ref} \times \frac{C}{2^N C + C_p} \times \sum_{i=0}^{N-1} b_i 2^i$$

- Binary-weighted or equally-weighted capacitor array.
- $C_p$  is top plate parasitic capacitance, and introduces a gain error.
- Opamp can be used to provide voltage gain and mitigate the effects of  $C_p$ .
- DACs at resolutions of 10 bits or above usually requires some kind of trimming or calibration.

# Segmented DAC Architecture



$$D_{in} = \sum_{i=0}^{N-1} b_i 2^i = \sum_{i=0}^{M-1} b_{i+L} 2^{i+L} + \sum_{j=0}^{L-1} b_j 2^j$$

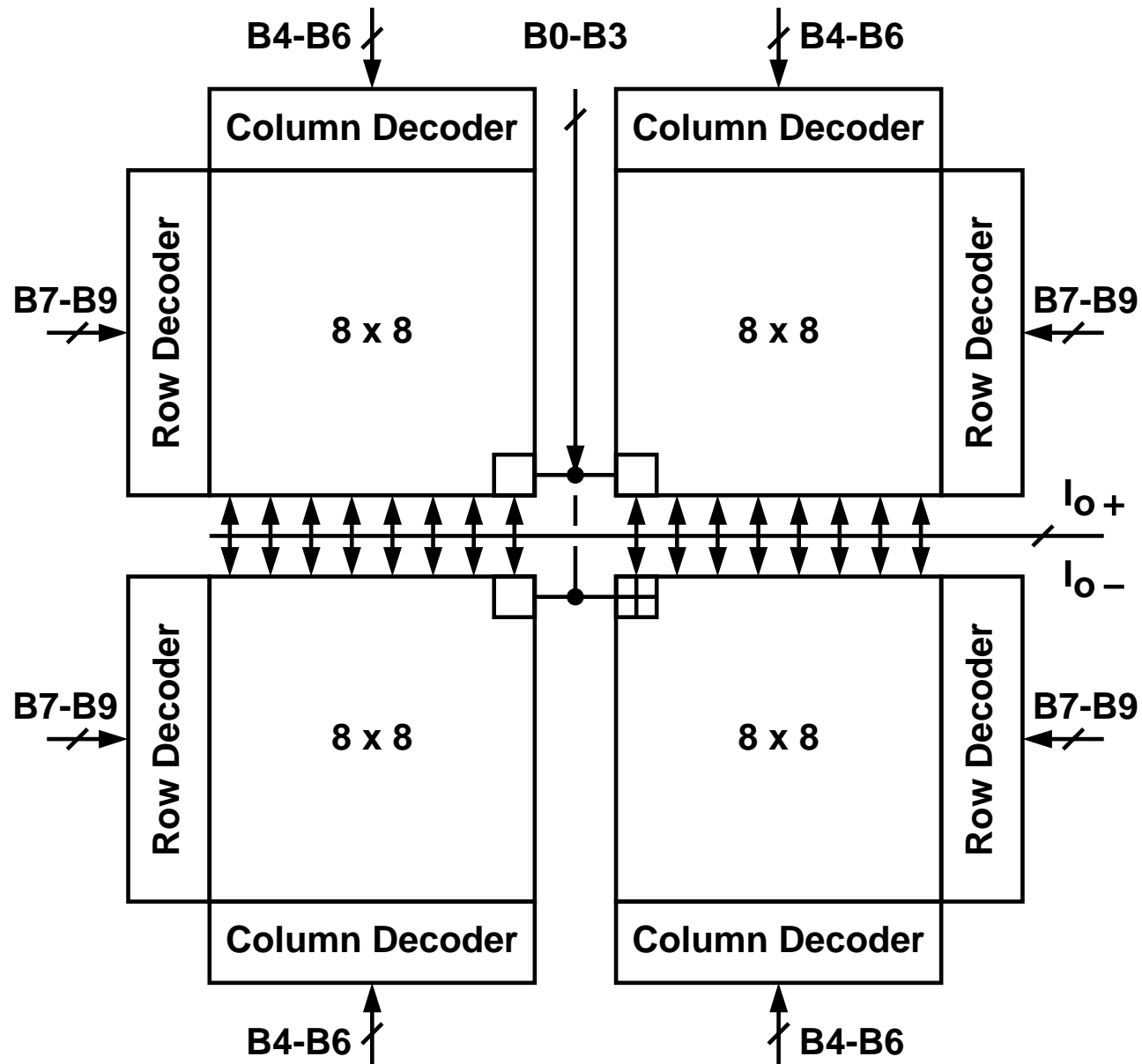
$$A_M = \Delta_M \times \sum_{i=0}^{M-1} b_{i+L} 2^i \quad A_L = \Delta_L \times \sum_{j=0}^{L-1} b_j 2^j$$

$$N = M + L \quad \Delta_M = 2^L \times \Delta_L$$

$$A_o = A_M + A_L = \Delta_L \times \sum_{i=0}^{M-1} b_{i+L} 2^{i+L} + \Delta_L \times \sum_{j=0}^{L-1} b_j 2^j = \Delta_L \times \sum_{i=0}^{N-1} b_i 2^i$$

- The M-DAC need to have  $\pm\Delta_L/2$  accuracy.
- Signal path delay mismatch between the M-DAC and the L-DAC can cause glitch.
- Can have more than two segments.

# A 10-Bit Segmented Current-Steering DAC

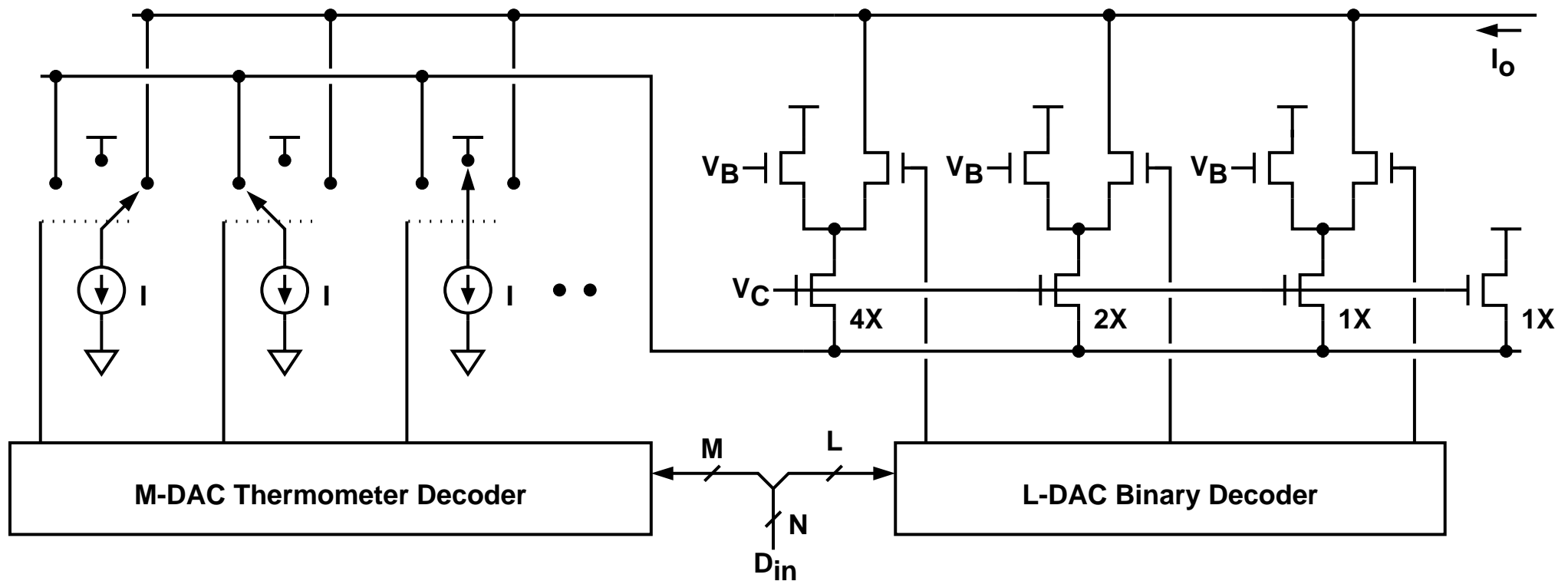


# A 10-Bit Segmented Current-Steering DAC

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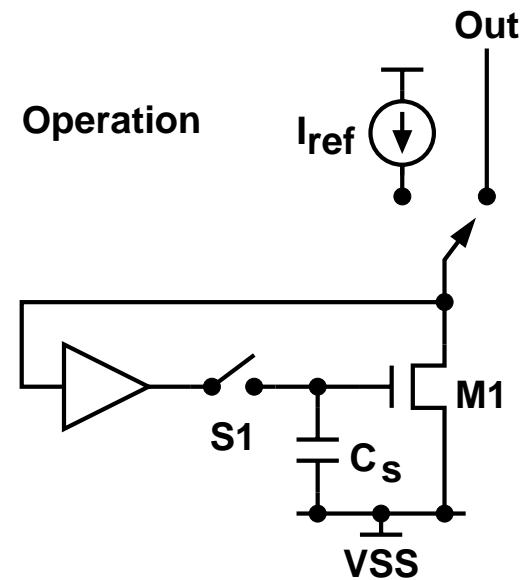
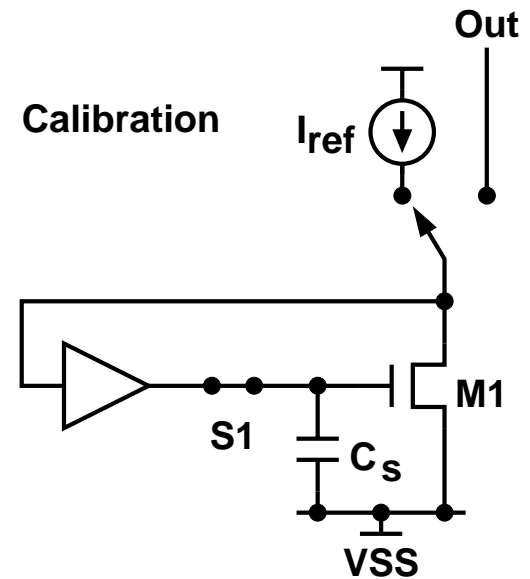
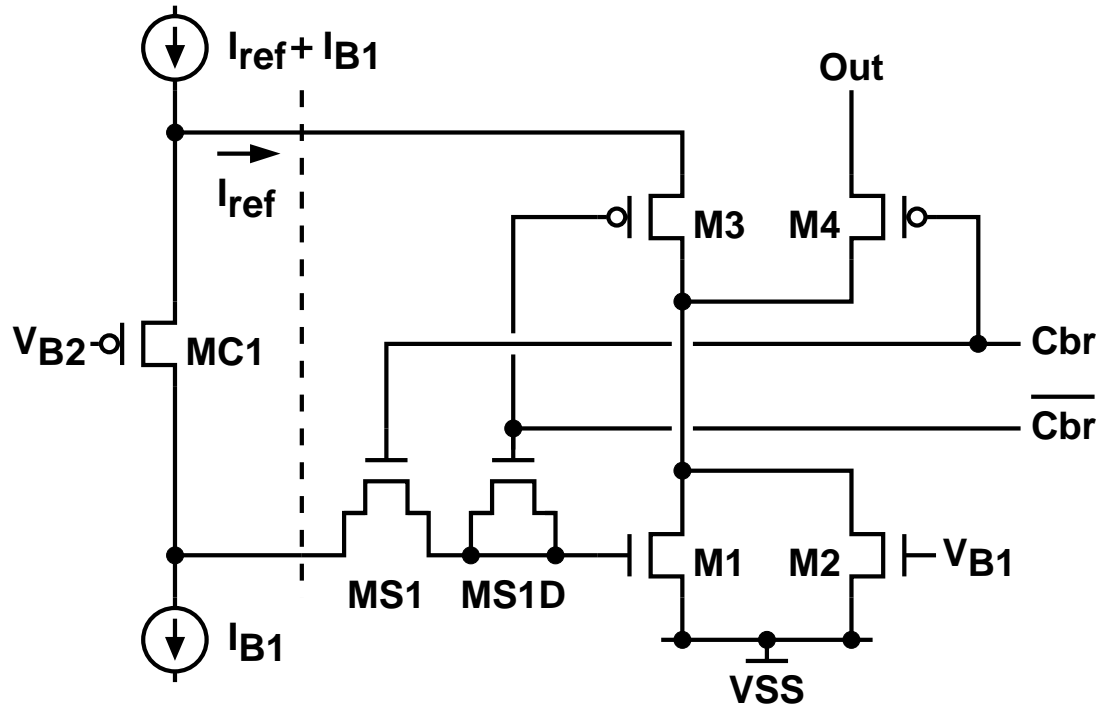
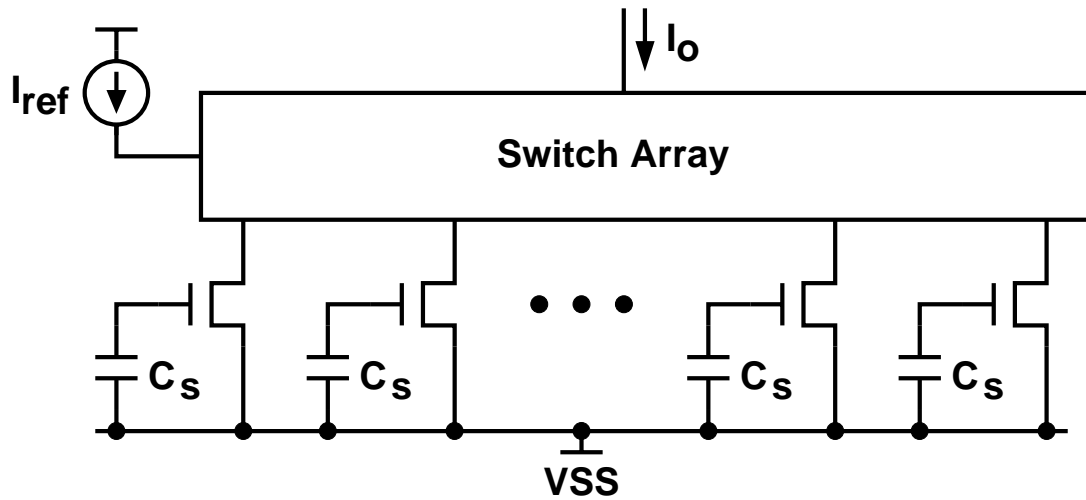
- Segmented 6-2-2 architecture with common-centroid layout.
- Each current cell in the matrix contains 4 LSB current.
- Reference: J. Bastos, et. al., “A 12-Bit Intrinsic Accuracy High-Speed CMOS DAC,” JSSC 12/1998, pp. 1959–1969.

# A Segmented Current-Steering DAC



- Greatly reduces area for large  $N$  while ensuring monotonicity (at least for MSBs).
- The L-DAC can be a binary-weighted DAC if its glitches can be tolerated.
- Reference: H. Schouwenaar, et al., JSSC 12/88, pp. 1290–1297.

# Dynamically-Matched Current Sources

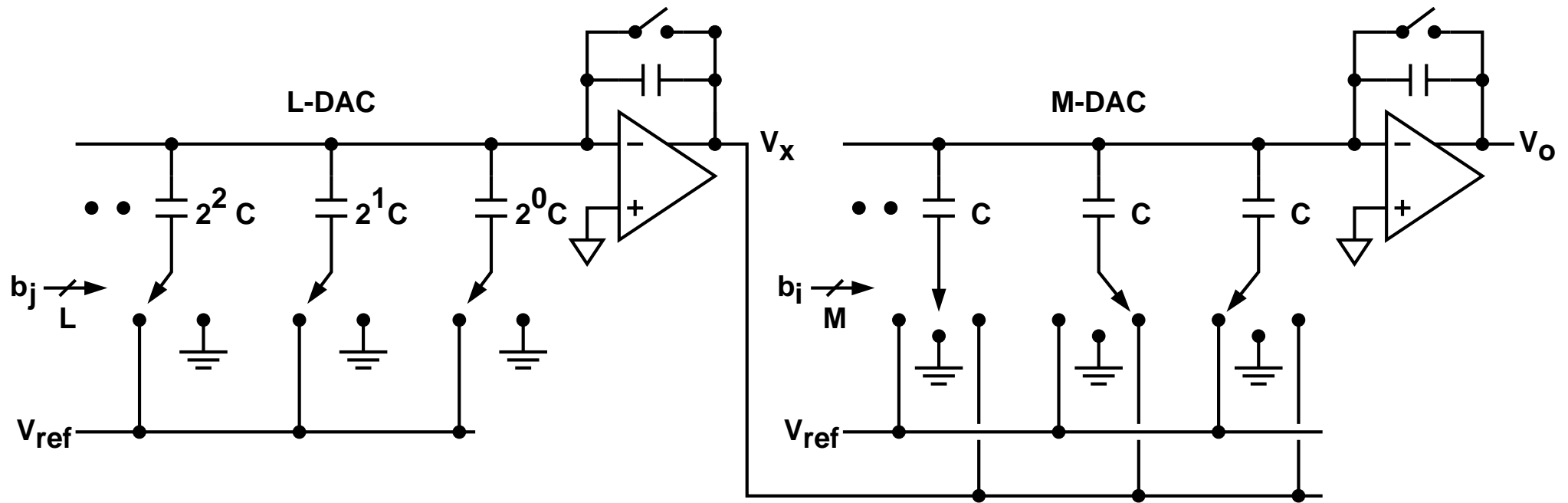


# Dynamically-Matched Current Sources

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- The bias voltage for the current sources is stored in each individual  $C_s$ . The voltage on  $C_s$  is refreshed periodically by means of calibration.
- A spare current source can be added to facilitate uninterrupted operation.
- $C_s$  can be just the  $C_{gs}$  of M1.
- The switching error of MS1 as well as  $g_{m1}$  must be minimized.
- By adding M2 with a constant current,  $g_{m1}$  can be reduced.
- 16-bit resolution can be achieved using this technique.
- Reference: D. Groeneveld, et al., JSSC 12/89, pp. 1517–1522.

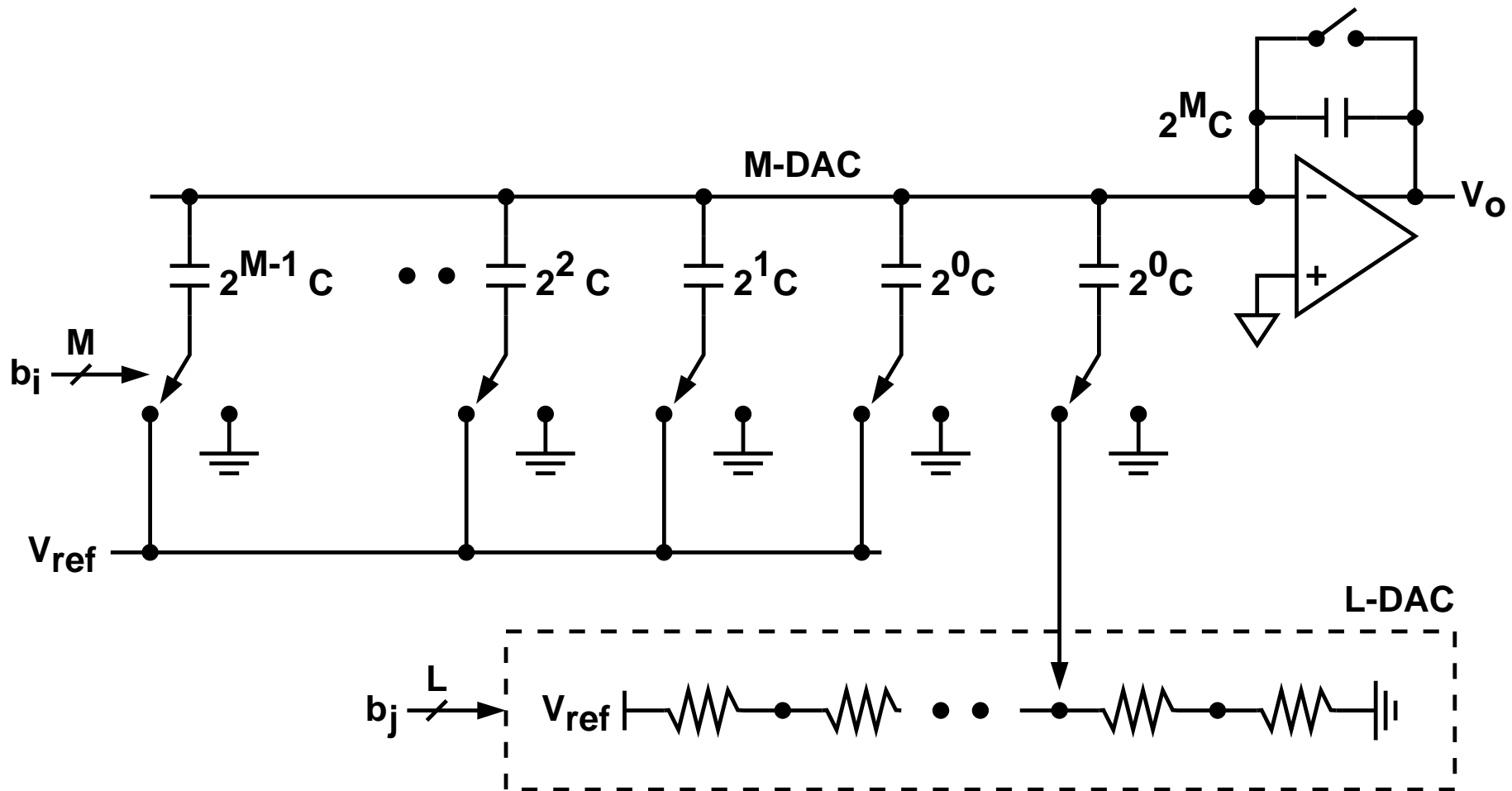
# A Segmented Charge-Redistribution DAC



$$D_{in} = \sum_{i=0}^{N-1} b_i 2^i \quad N = M + L \quad V_x = \frac{V_{ref}}{2^L} \cdot \sum_{j=0}^{L-1} b_j 2^j$$

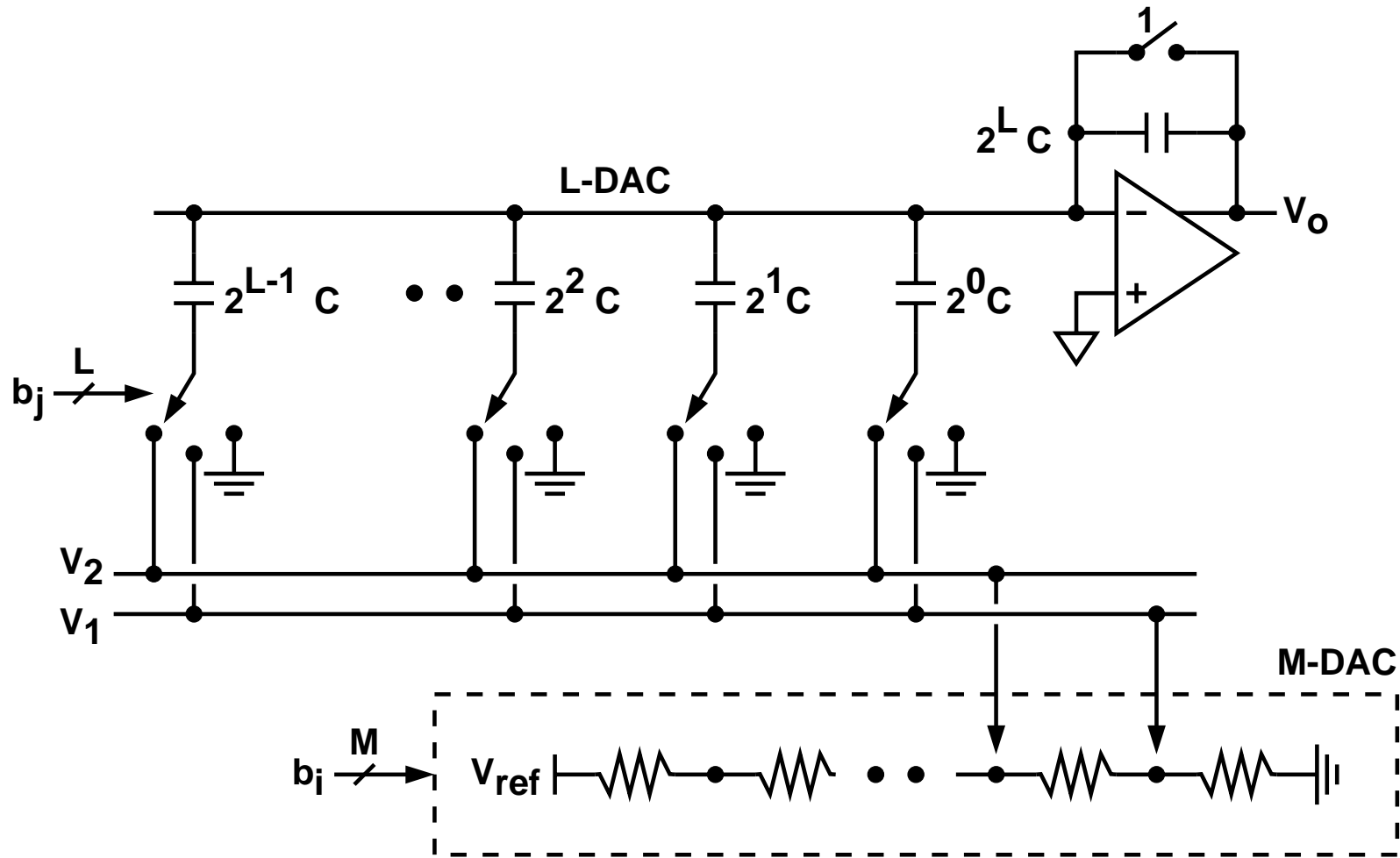
$$V_o = \frac{V_{ref}}{2^M} \cdot \sum_{i=0}^{M-1} b_{i+L} 2^i + \frac{1}{2^M} \cdot V_x = \frac{V_{ref}}{2^{M+L}} \cdot \left[ \sum_{i=0}^{M-1} b_{i+L} 2^{i+L} + \sum_{j=0}^{L-1} b_j 2^j \right] = \frac{V_{ref}}{2^N} \cdot \sum_{i=0}^{N-1} b_i 2^i$$

# A Capacitor-Resistor Hybrid DAC



$$V_o = \frac{V_{ref}}{2^M} \times \sum_{i=0}^{M-1} b_{i+L} 2^i + \frac{1}{2^M} \times \frac{V_{ref}}{2^L} \times \sum_{j=0}^{L-1} b_j 2^j = \frac{V_{ref}}{2^N} \times \sum_{i=0}^{N-1} b_i 2^i \quad N = M + L$$

# A Resistor-Capacitor Hybrid DAC



$$V_1 = \Delta_M \times \sum_{i=0}^{M-1} b_{i+L} 2^i \quad V_2 = V_1 + \Delta_M \quad \Delta_M = \frac{V_{ref}}{2^M} \quad N = M + L$$

# A Resistor-Capacitor Hybrid DAC

---

During  $\phi_1 = 1$ ,

Cap Bottom Plate @ GND

$$V_o = 0$$

During  $\phi_2 = 1$ ,

$$b_i = \begin{cases} 1 & \rightarrow \text{Cap Bottom Plate @ } V_2 \\ 0 & \rightarrow \text{Cap Bottom Plate @ } V_1 \end{cases}$$

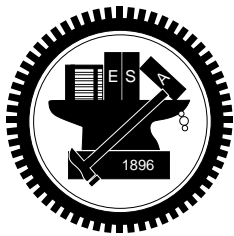
$$V_o = V_1 + \frac{\Delta_M}{2^L} \times \sum_{j=0}^{L-1} b_j 2^j = \frac{V_{ref}}{2^M} \times \sum_{i=0}^{M-1} b_{i+L} 2^i + \frac{V_{ref}}{2^{M+L}} \times \sum_{j=0}^{L-1} b_j 2^j = \frac{V_{ref}}{2^N} \times \sum_{i=0}^{N-1} b_i 2^i$$

- The capacitor array interpolates the voltages between  $V_1$  and  $V_2$ .
- Reference: J.-W. Yang, et al., JSSC 10/89, pp. 1458–1461.

# Nyquist-Rate Analog-to-Digital Converters

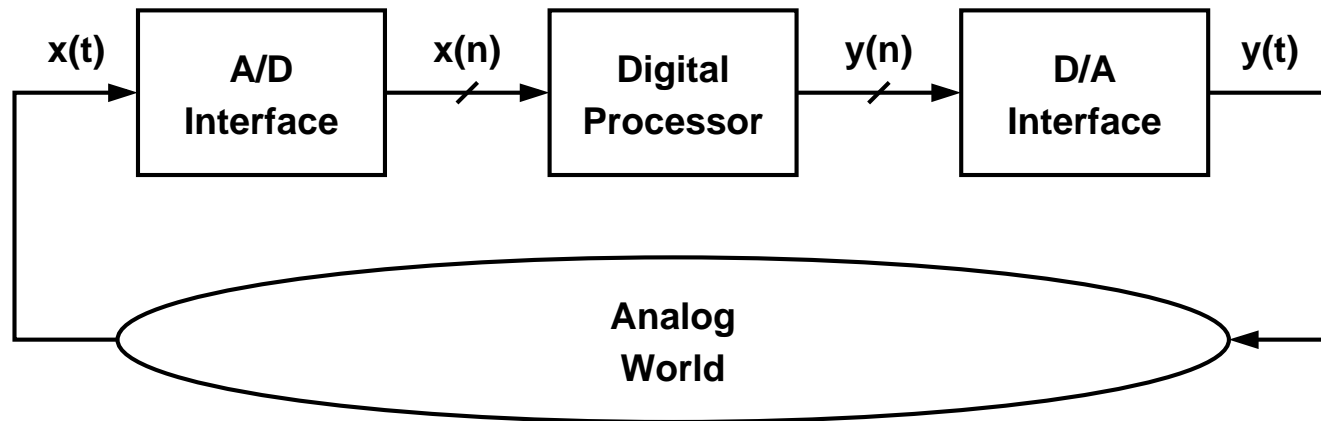
Jieh-Tsorng Wu

November 13, 2002

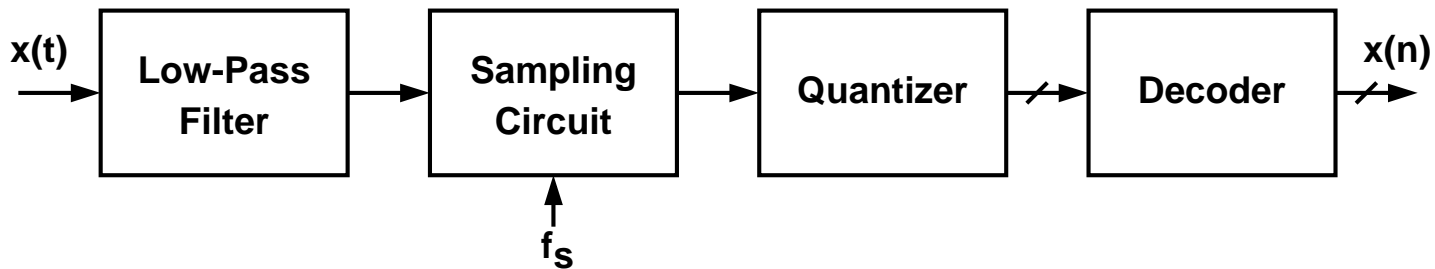


National Chiao-Tung University  
Department of Electronics Engineering

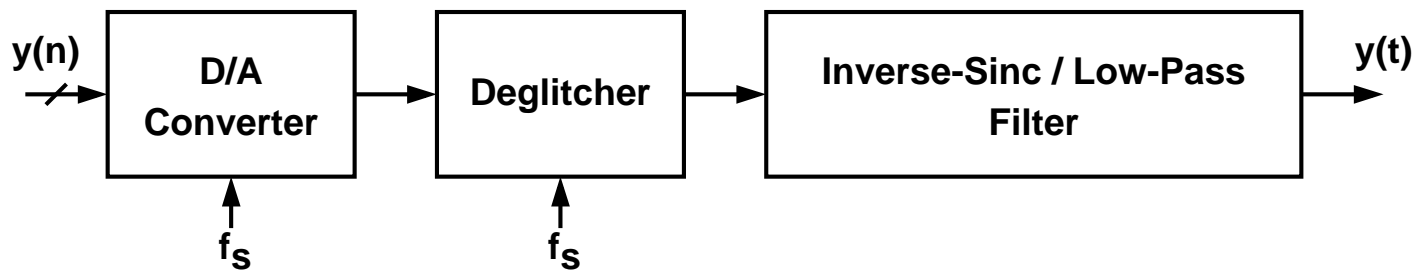
# A/D and D/A Interfaces



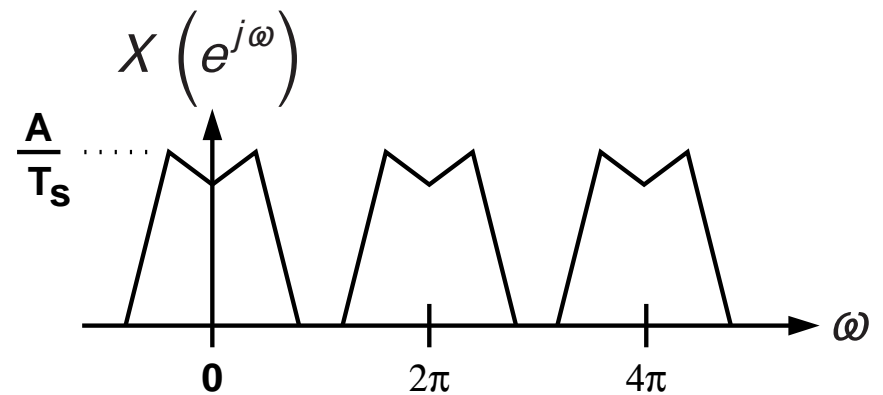
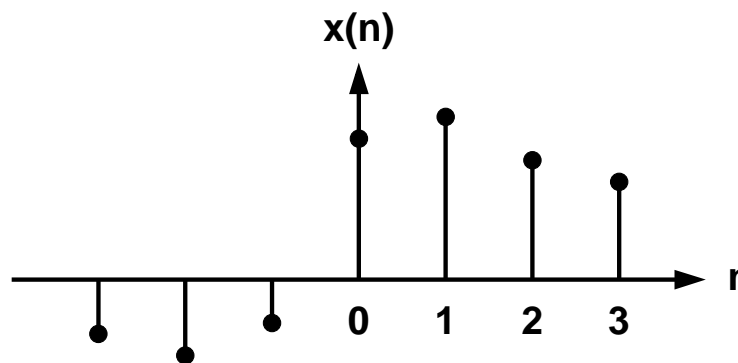
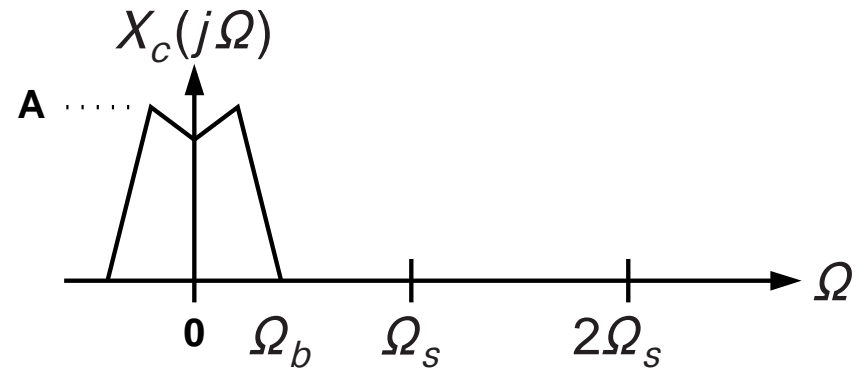
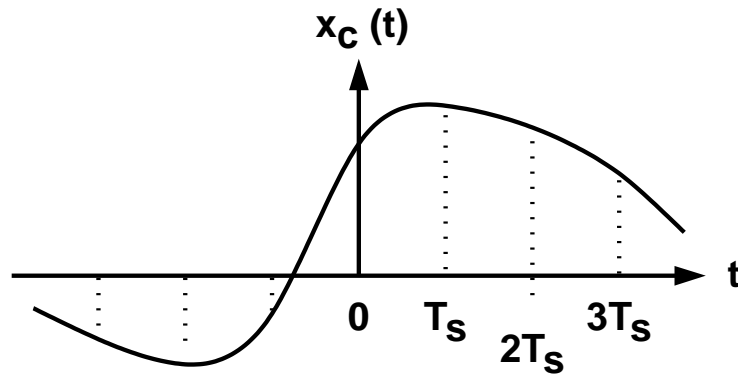
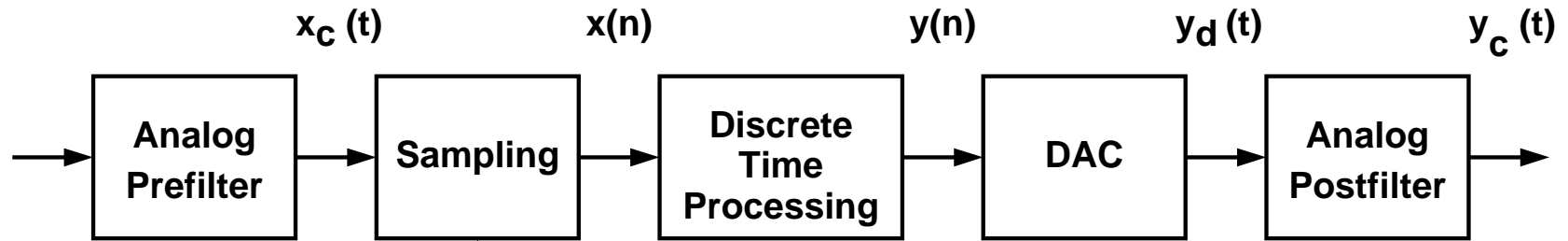
## Analog-to-Digital Interface



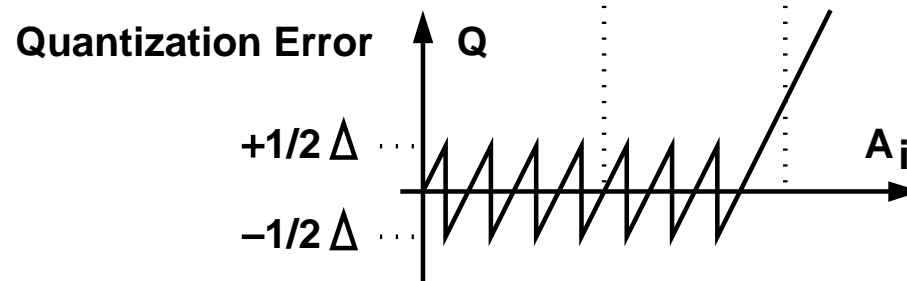
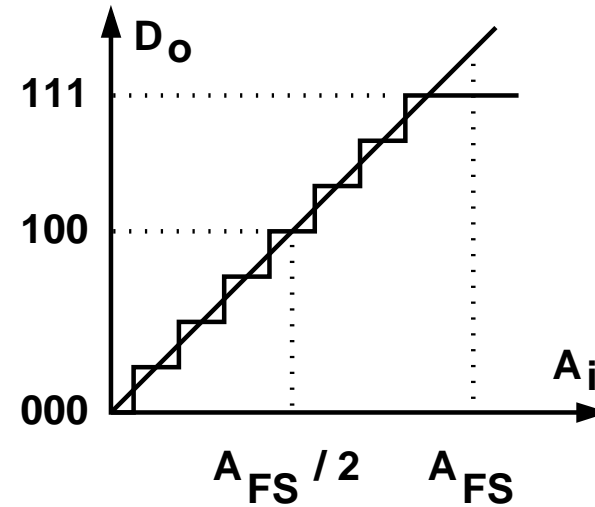
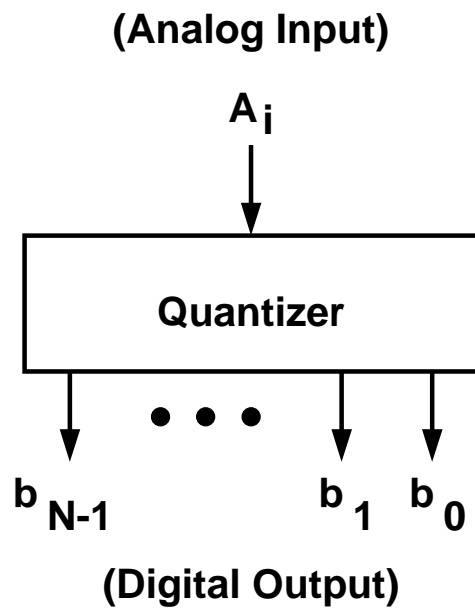
## Digital-to-Analog Interface



# Continuous-to-Discrete Conversion



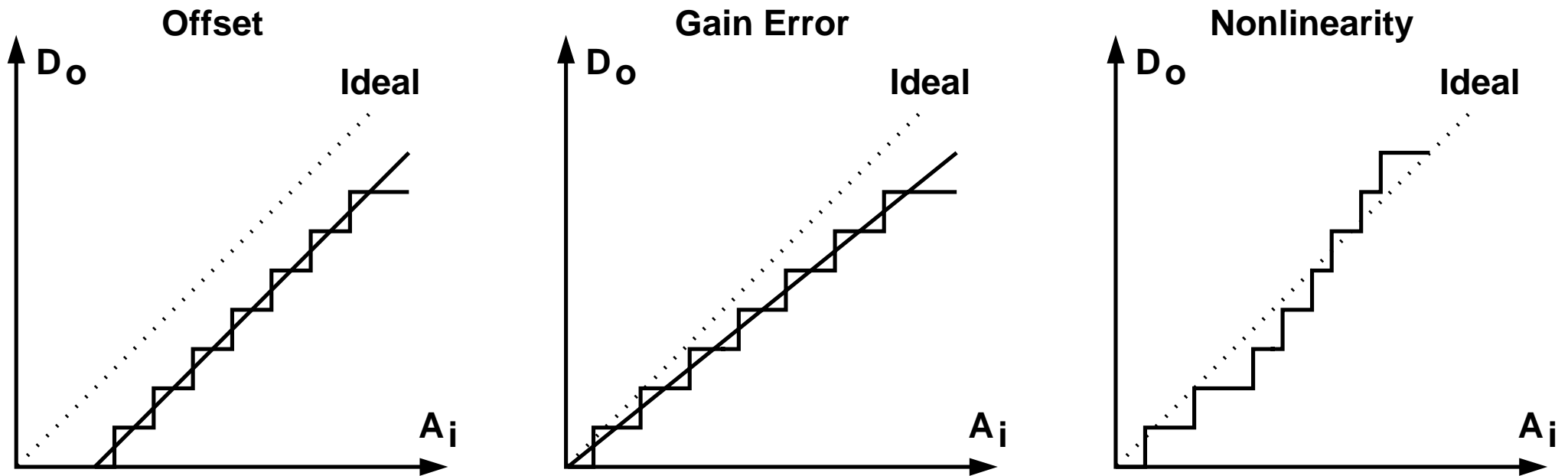
# A/D Quantization Characteristic



$$A_{i,tran} = \Delta \times \sum_{i=0}^{N-1} b_i 2^i - \frac{1}{2} \Delta$$

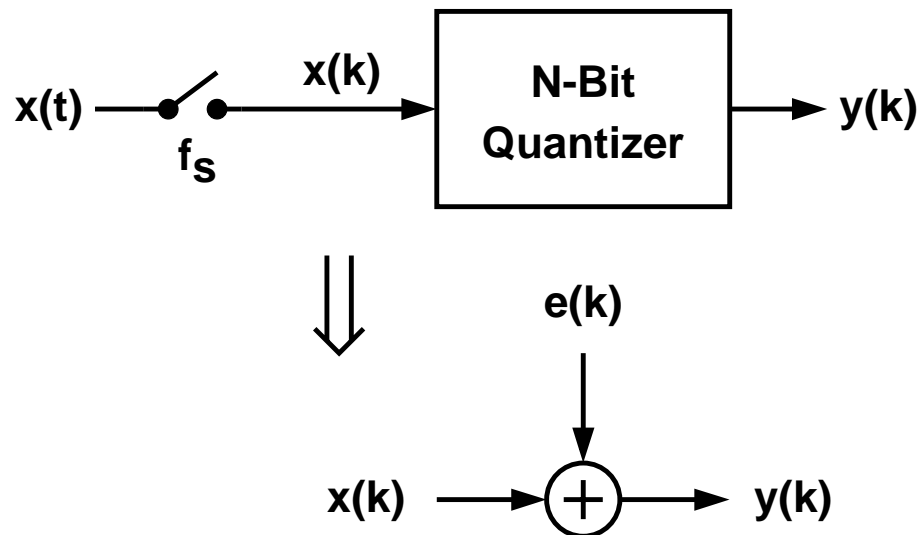
$$A_{FS} = \text{Full-Scale Output} \quad \Delta = \text{LSB} = \text{Step Size} = \frac{A_{FS}}{2^N}$$

# Imperfections in A/D Quantization Characteristic

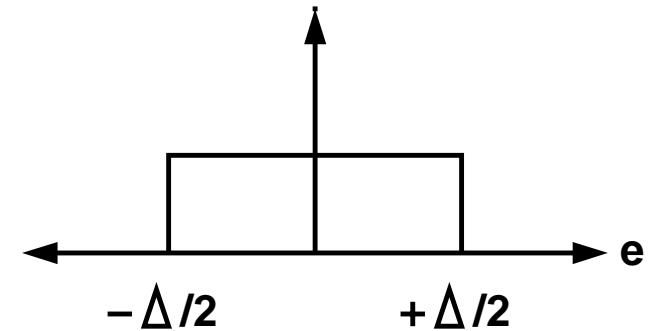


- **Differential nonlinearity (DNL):** Maximum deviation in step width (width between transitions) from the ideal value of 1 LSB ( $= \Delta$ ).
- **Integral nonlinearity (INL):** Maximum deviation of the step midpoints from the ideal step midpoints. Or the maximum deviation of the transition points from ideal.
- If  $DNL = -1$  LSB  $\Rightarrow$  missing code.

# Quantization Noise



Probability Density Function (pdf)



$e(k)$  is a *quantization noise* due to the quantization process.

$$e(k) \equiv y(k) - x(k) \quad \text{Noise Power} = P_n = \int e^2 \text{pdf}(e) de = \frac{1}{12} \Delta^2$$

# Quantization Noise

---

Let the input  $x(k)$  be a sinusoidal waveform

$$x(k) = A \sin(2\pi f_i \cdot kT_s) \quad \text{Signal Power} = P_s = \frac{1}{2}A^2$$

The signal-to-noise ratio of  $y(k)$  is

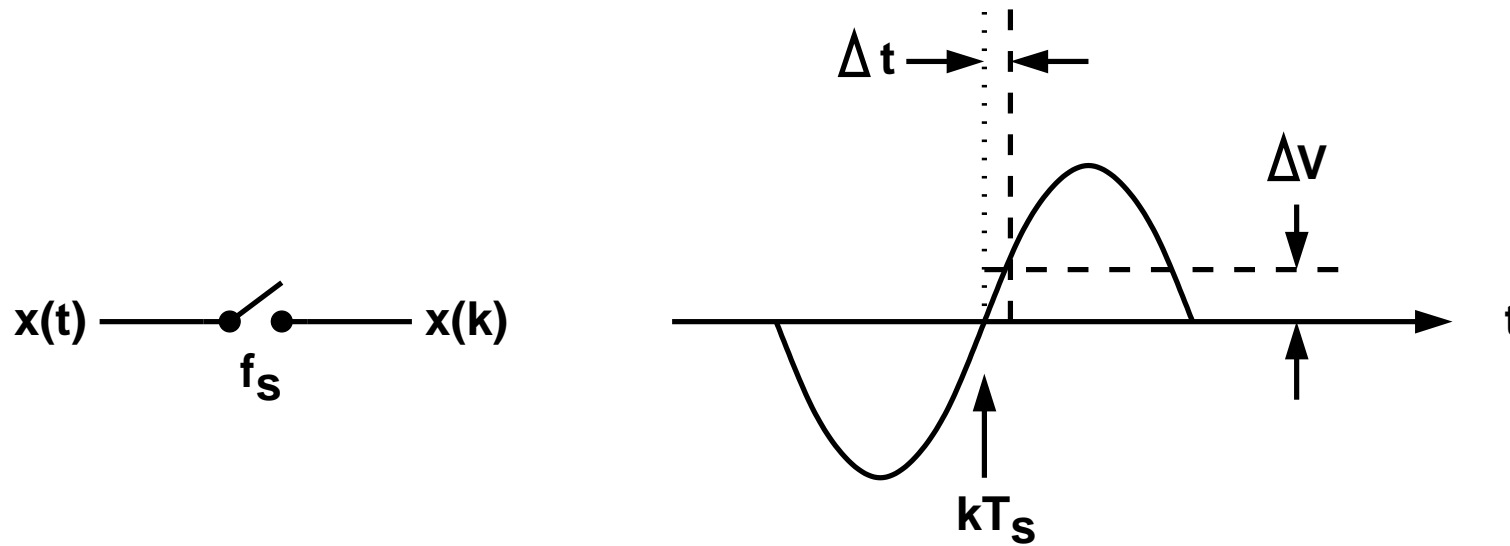
$$\text{SNR} \equiv \frac{P_s}{P_n} = 6 \cdot \frac{A^2}{\Delta^2}$$

When the input's amplitude  $A = A_{FS}/2$ , the SNR reaches its maximum value.

$$A_{FS} = 2^N \Delta \quad P_s = \frac{1}{8} \cdot 2^{2N} \Delta^2 \quad \text{SNR}_{max} = 2^{2N} \times \frac{3}{2} = N \times 6.02 \text{ dB} + 1.76 \text{ dB}$$

- The ratio between  $f_s$  and  $f_i$  should be irrational.
- In the discrete-time domain, noise power of  $e(k)$  is assumed to be uniformly distributed between  $-\Omega_s/2$  and  $+\Omega_s/2$ . The power density is  $\Delta^2/(12\Omega_s)$ .

# Sampling-Time Uncertainty (Aperture Jitter)



$$x(k) = x(kT_s + \Delta t) \quad T_s = \frac{1}{f_s}$$

For a full-scale sinusoidal input

$$x(t) = \frac{1}{2} A_{FS} \sin(2\pi f_i t) \quad A_{FS} = 2^N \Delta$$

$$\Delta V \approx \frac{dx}{dt} \times \Delta t < A_{FS} \cdot \pi f_i \times \Delta t < \frac{1}{2} \Delta \quad \Rightarrow \quad \Delta t < \frac{1}{2^N} \cdot \frac{1}{2\pi f_i}$$

# Sampling-Time Uncertainty (Aperture Jitter)

---

Let  $x(t) = \frac{1}{2}A_{FS} \sin(2\pi f_i t)$  and  $\Delta t$  be a random variable, then

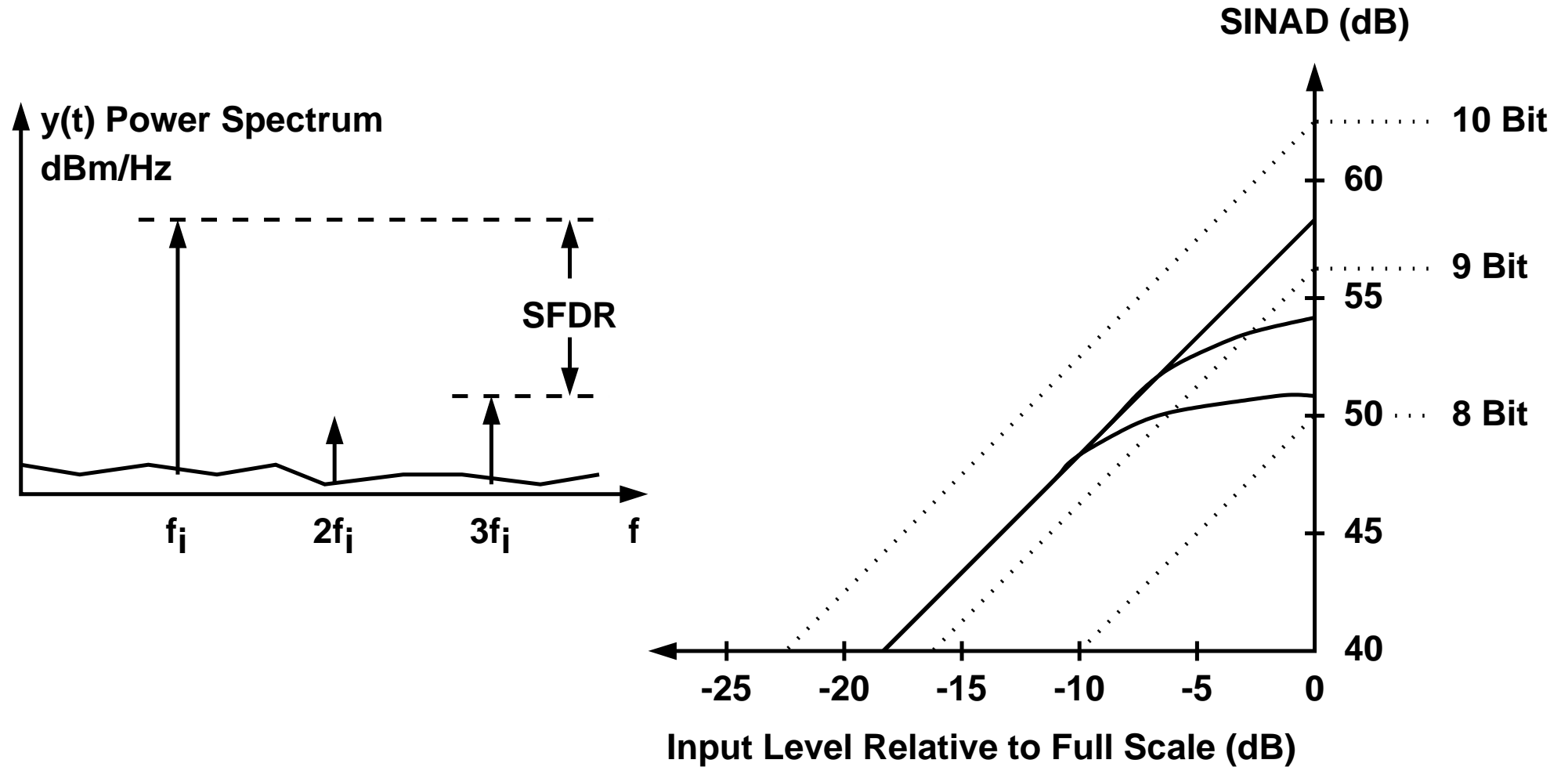
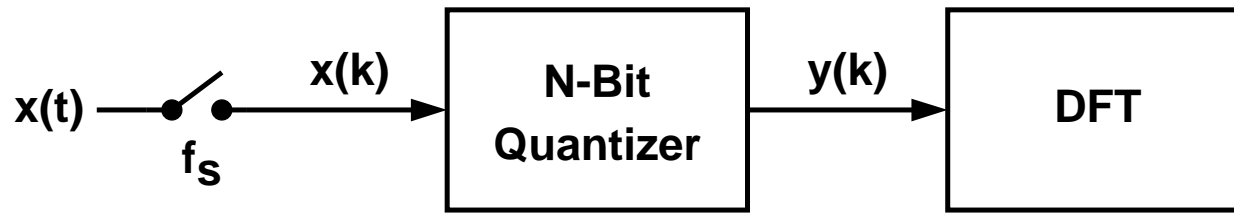
$$\begin{aligned}x(k) &= x(kT_s + \Delta t) \approx \frac{1}{2}A_{FS} \sin(2\pi f_i kT_s) + \left. \frac{dx(t)}{dt} \right|_{t=kT_s} \times \Delta t \\ &\approx \frac{1}{2}A_{FS} \sin(2\pi f_i kT_s) + A_{FS} \pi f_i \cos(2\pi f_i kT_s) \times \Delta t \\ \overline{x^2(k)} &= \frac{1}{8}A_{FS}^2 + \frac{1}{2}A_{FS}^2 \pi^2 f_i^2 \times \overline{\Delta t^2} = P_s + P_n\end{aligned}$$

The signal-to-noise ratio of  $x(k)$  is

$$\text{SNR} = \frac{P_s}{P_n} = \frac{1}{4\pi^2 f_i^2 \cdot \overline{\Delta t^2}} = -20 \log(2\pi f_i \cdot \Delta t_{\text{rms}}) \text{ dB}$$

- If  $f_i = 1$  MHz,  $N = 14$ , SNR = 86 dB, want  $\Delta t_{\text{rms}} < 8.0$  psec.
- If  $f_i = 100$  MHz,  $N = 10$ , SNR = 62 dB, want  $\Delta t_{\text{rms}} < 1.26$  psec.

# DFT Nonlinearity Test of ADCs

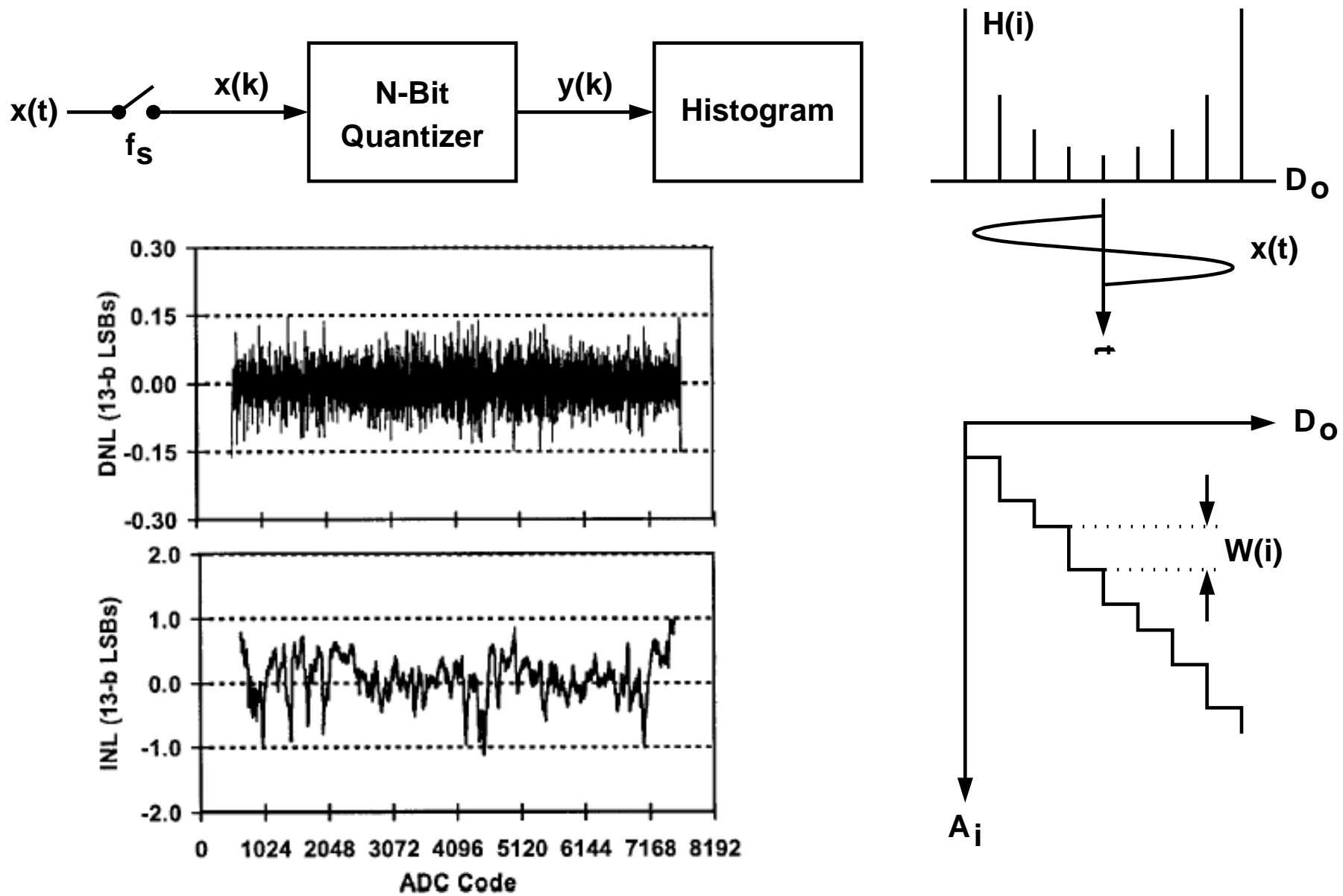


# DFT Nonlinearity Test of ADCs

---

- The ratio between  $f_s$  and  $f_j$  should be irrational.
- In the discrete-time domain, noise power of  $e(k)$  is assumed to be uniformly distributed between  $-\Omega_s/2$  and  $+\Omega_s/2$ . The power density is  $\Delta^2/(12\Omega_s)$ .
- The *spurious free dynamic range* (SFDR) is the ratio of the fundamental signal component to the largest distortion component when  $A = A_{FS}/2$ .
- The *signal-to-noise plus distortion ratio* (SINAD) is the ratio of power of the fundamental signal to the total power of noise and distortion when  $A = A_{FS}/2$ .
- In finding the total noise power, the noise bandwidth need to be specified.

# Code Density Test of ADCs



# Code Density Test of ADCs

---

Let  $N_t$  be the total number of samples,  $H(i)$  the number of counts in the  $i$ -th  $D_o$ , and  $P(i)$  the ideal probability for the  $i$ -th  $D_o$ . We have

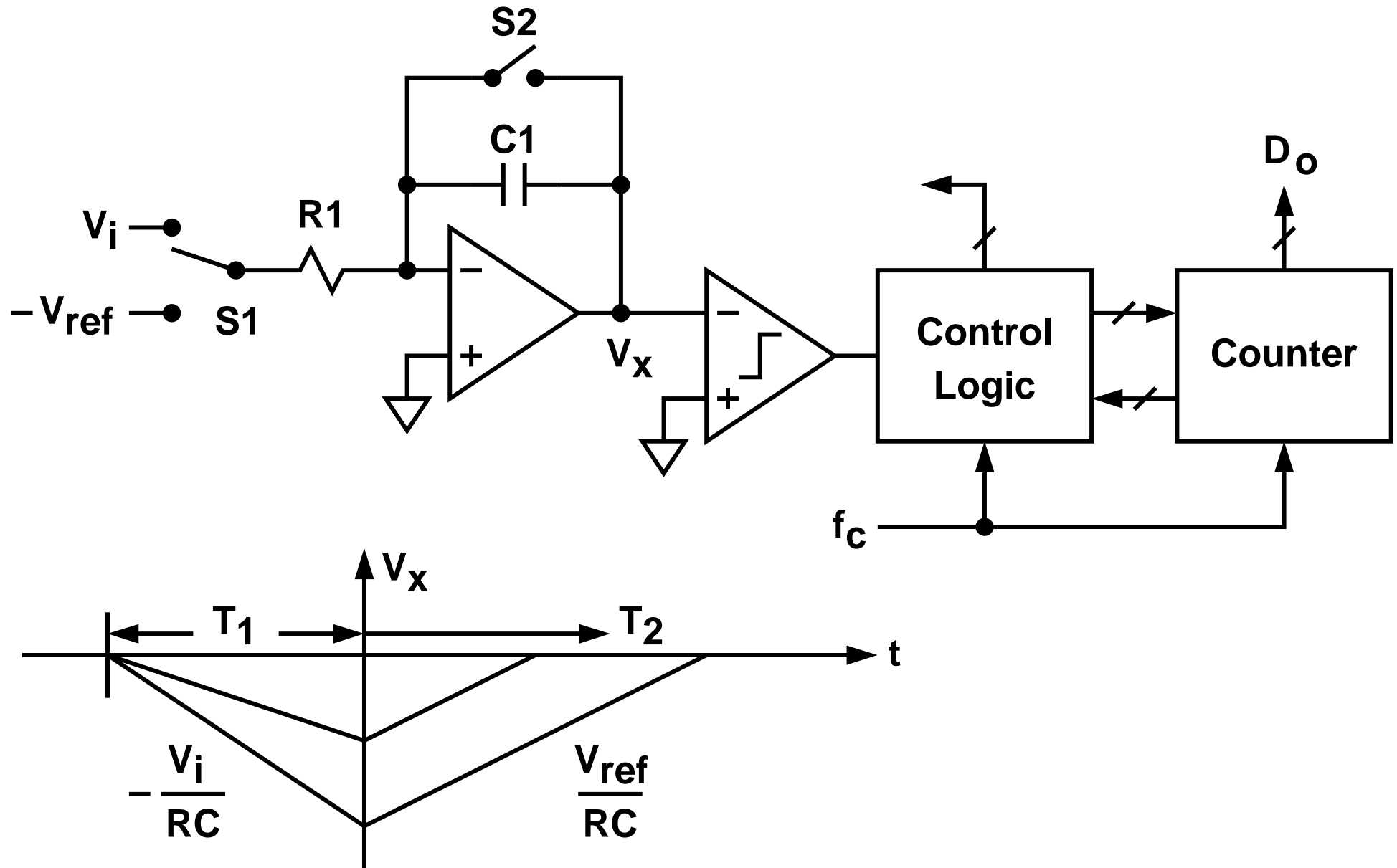
$$\frac{W(i)}{\Delta} = (A_{i+1,tran} - A_{i,tran}) \cdot \frac{1}{\Delta} = \frac{H(i)}{N_t} \cdot \frac{1}{P(i)}$$

- For high precision, sinusoidal waveform is usually for the input. The probability density  $p(V)$  for  $A \sin(\omega t)$  is

$$p(V) = \frac{1}{\pi \sqrt{A^2 - V^2}}$$

- To test a 12-bit ADC, for 99 percent confidence and 0.10 bit precision, 4.2 million samples are needed.
- Reference: Doernberg, JSSC 12/84, pp. 820–827.

# Serial (Integrating) Architectures



# Serial (Integrating) Architectures

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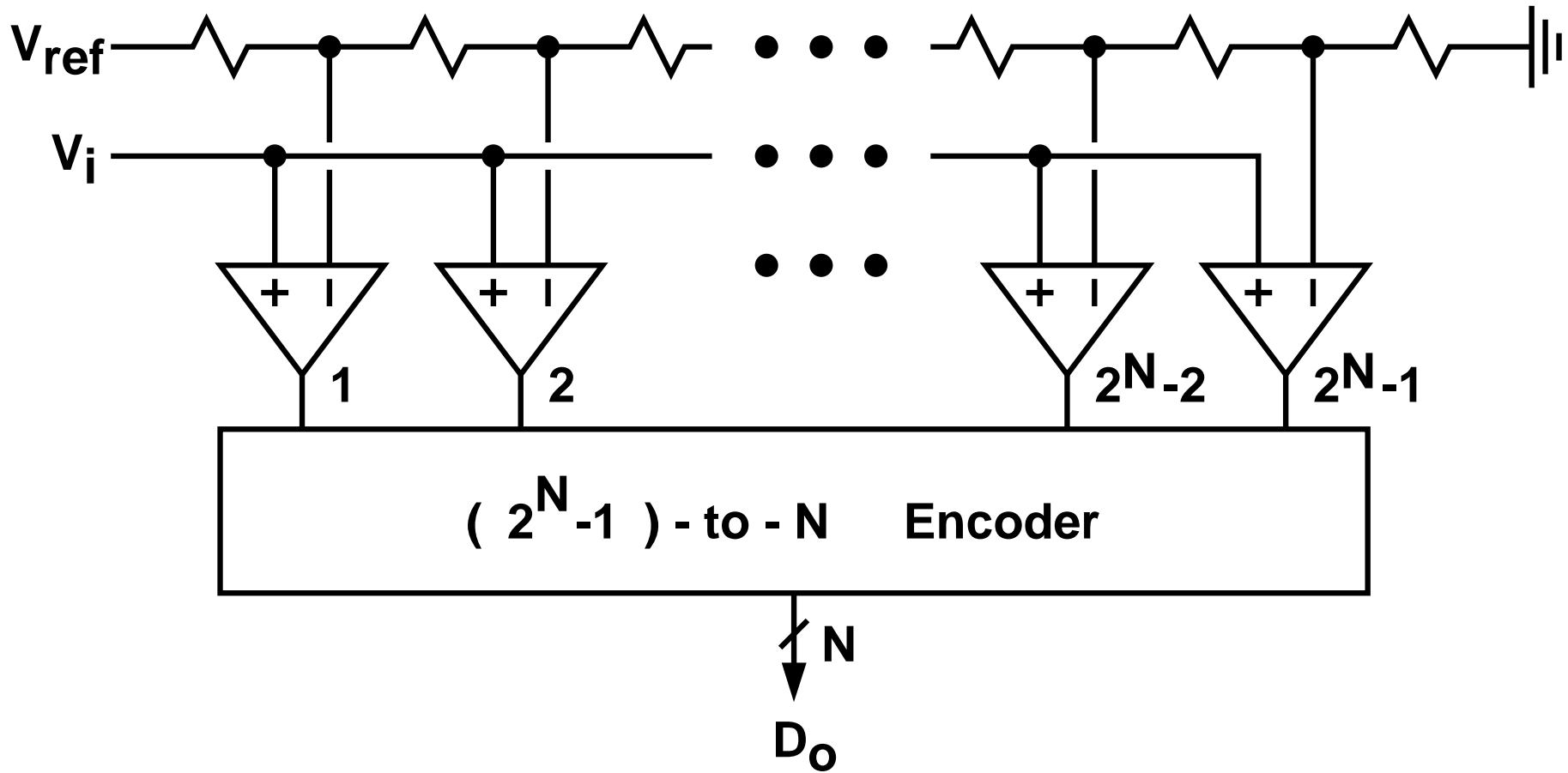
The output is

$$\frac{D_o}{f_c} = T_2 = T_1 \cdot \frac{V_i}{V_{ref}}$$

- Linear search of possible subregions.
- Integrating types: single slope, dual slope, quad-slope.
- Low conversion rate. Requires  $2 \times 2^N$  clock cycles for a full-scale conversion.
- The input is integrated in the  $T_1$  period, resulting in a filter transfer function of

$$|H(f)| = \left| \frac{\sin(\pi T_1 f)}{\pi T_1 f} \right|$$

# Parallel (Flash) Architectures

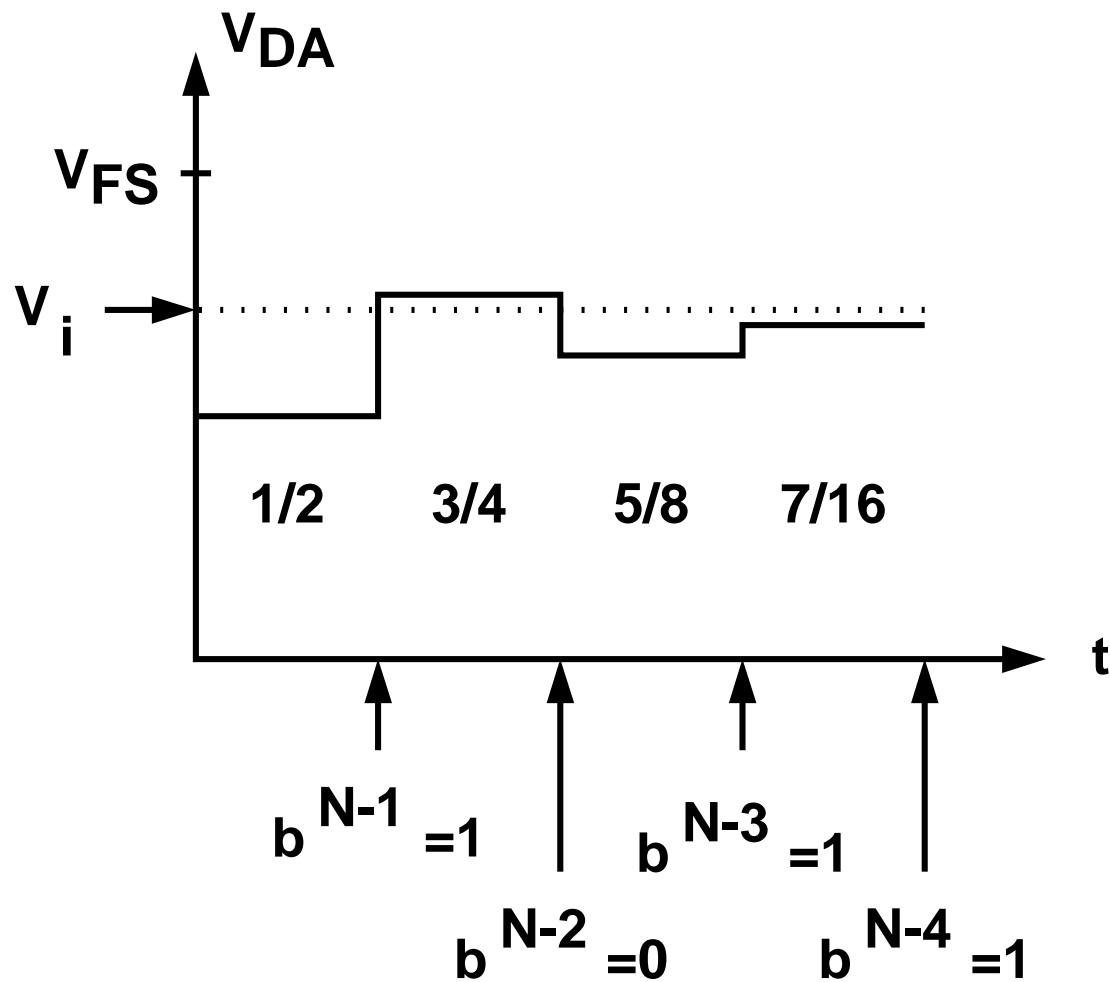
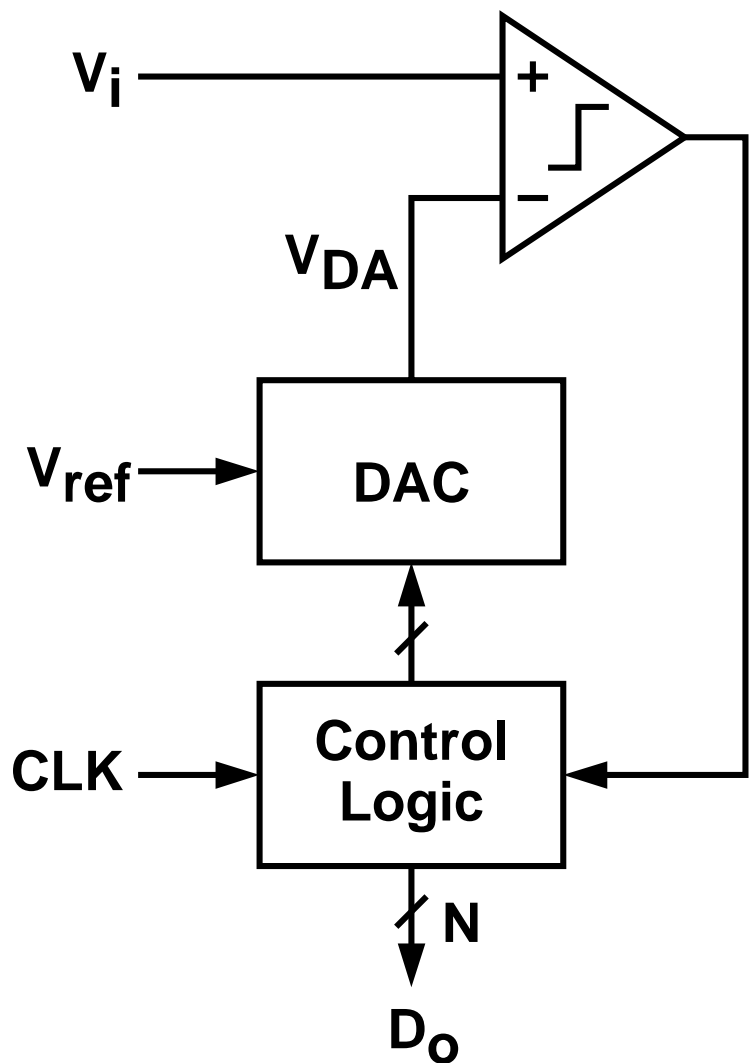


# Parallel (Flash) Architectures

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- All subregions are examined simultaneously. One comparator per subregion.
- Using  $2^N - 1$  comparators, the input is simultaneously compared with  $2^N - 1$  reference voltages derived from resistor string.
- High speed. Requires only one comparison cycle per conversion.
- Large size and power dissipation for large  $N$ .
- Design issues: input capacitive loading, clock jitter and dispersion, slew-dependent sampling point, nonlinear input capacitance, resistor-string dc and ac bowing, substrate and power-supply noises, kickback noises, sparkles in thermometer code.
- Gray encoding is often used as an intermediate step between thermometer and binary codes.

# Successive Approximation Architectures

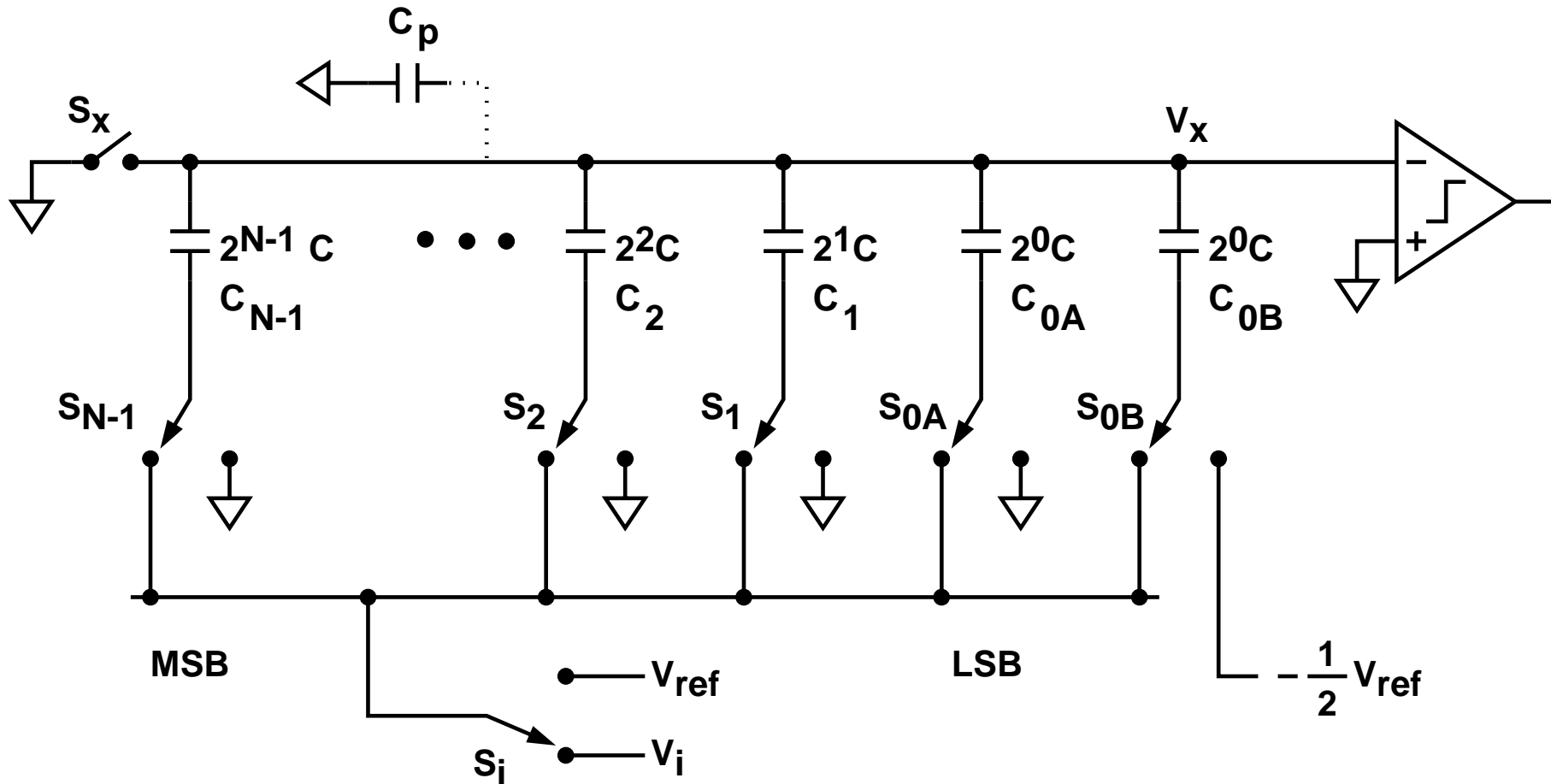


# Successive Approximation Architectures

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- Binary search of possible subregions.
- Fraction of  $V_{FS}$  corresponding to each bit is successively (starting with MSB) added to fraction corresponding to already determined bits and sum is compared to input.
- $N$  comparisons per conversion.
- Requires a high-speed DAC with precision on the order of the converter itself.
- Excellent trade-off between accuracy and speed.

# Charge-Redistribution ADC



$$C_{tot} = \sum_{i=1}^{N-1} 2^i C_i + C_{0A} + C_{0B} = 2^N C$$

# Charge-Redistribution ADCs

---

## Sample Mode

- $S_x \rightarrow \text{GND}$ .  $V_x = 0$ .
- $S_{0A}, S_{0B}, S_1, S_2, \dots, S_{N-1}, S_i \rightarrow V_i$ .

## Hold Mode

- $S_x$  open.
- $S_{0A}, S_1, S_2, \dots, S_{N-1} \rightarrow \text{GND}$ .
- $S_{0B} \rightarrow -\frac{1}{2}V_{ref}$ , sets transition offset to  $\frac{1}{2}\Delta$ .

$$V_x = -V_i - \frac{C_{0B}}{C_{tot}} \cdot \frac{V_{ref}}{2} = -V_i - \frac{1}{2} \cdot \frac{V_{ref}}{2^N} \quad \Delta = \frac{V_{ref}}{2^N}$$

# Charge-Redistribution ADCs

---

## Redistribution Mode

- $S_i \rightarrow V_{ref}$ .
- Test bits one at a time in succession, beginning with  $b_{N-1}$ .

## Bit $b_{N-1}$ Test

- $S_{N-1} \rightarrow V_{ref}$

$$V_x = -V_i - \frac{1}{2} \frac{V_{ref}}{2^N} + \frac{C_{N-1}}{C_{tot}} \cdot V_{ref} = -V_i - \frac{1}{2} \cdot \frac{V_{ref}}{2^N} + \frac{V_{ref}}{2}$$

- If  $V_x < 0$ ,  $b_{N-1} = 1$ ,  $S_{N-1} \rightarrow V_{ref}$ .  
If  $V_x > 0$ ,  $b_{N-1} = 0$ ,  $S_{N-1} \rightarrow \text{GND}$ .

# Charge-Redistribution ADCs

---

Bit  $b_i$  Test,  $i = N - 2, N - 3, \dots, 0$

- $S_i \rightarrow V_{ref}$

$$V_x = -V_i - \frac{1}{2} \frac{V_{ref}}{2^N} + \frac{V_{ref}}{2^N} \sum_{j=i+1}^{N-1} b_j 2^j + \frac{C_i}{C_{tot}} \cdot V_{ref} = -V_i - \frac{1}{2} \cdot \frac{V_{ref}}{2^N} + \frac{V_{ref}}{2^N} \left( \sum_{j=i+1}^{N-1} b_j 2^j + 2^i \right)$$

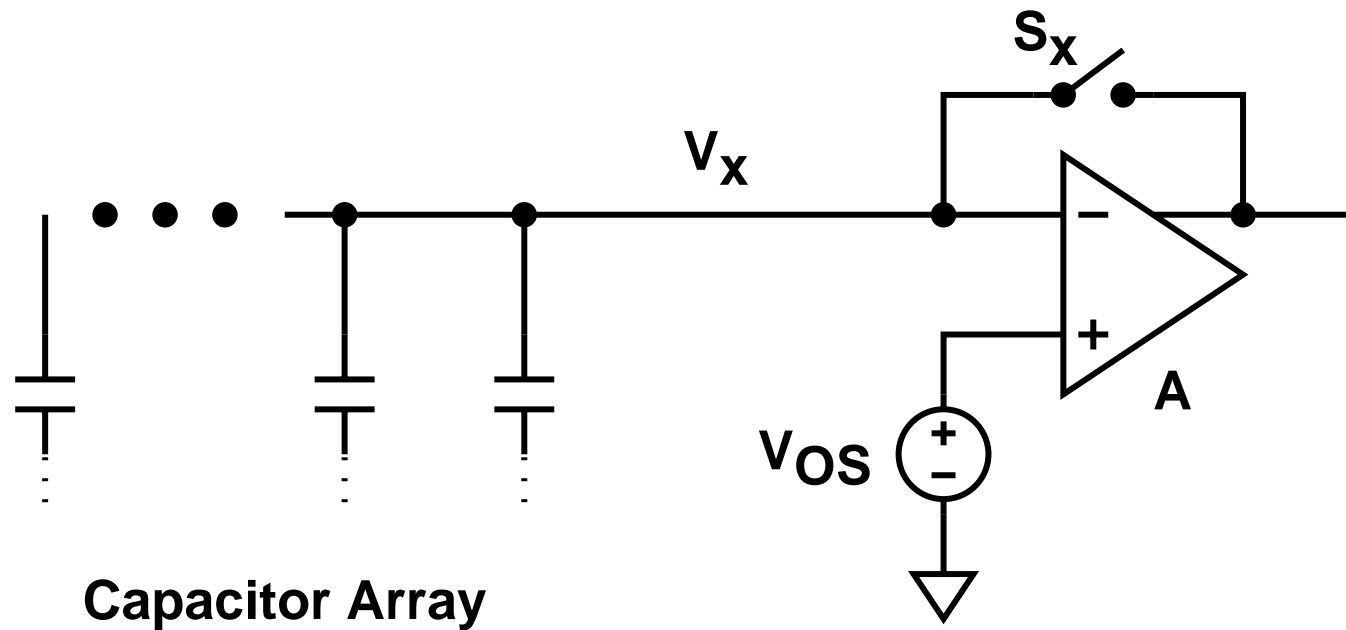
- If  $V_x < 0$ ,  $b_i = 1$ ,  $S_i \rightarrow V_{ref}$ .  
If  $V_x > 0$ ,  $b_i = 0$ ,  $S_i \rightarrow \text{GND}$ .

The effect of parasitic capacitance,  $C_p$

- The voltage on the summing node becomes  $V'_x = V_x \cdot \frac{C_{tot}}{C_{tot} + C_p}$ .
- $C_p$  has no effect on the A/D quantization characteristic, if the comparator is ideal.
- $C_p$  does attenuate  $V_x$ , thus requiring higher comparator gain.

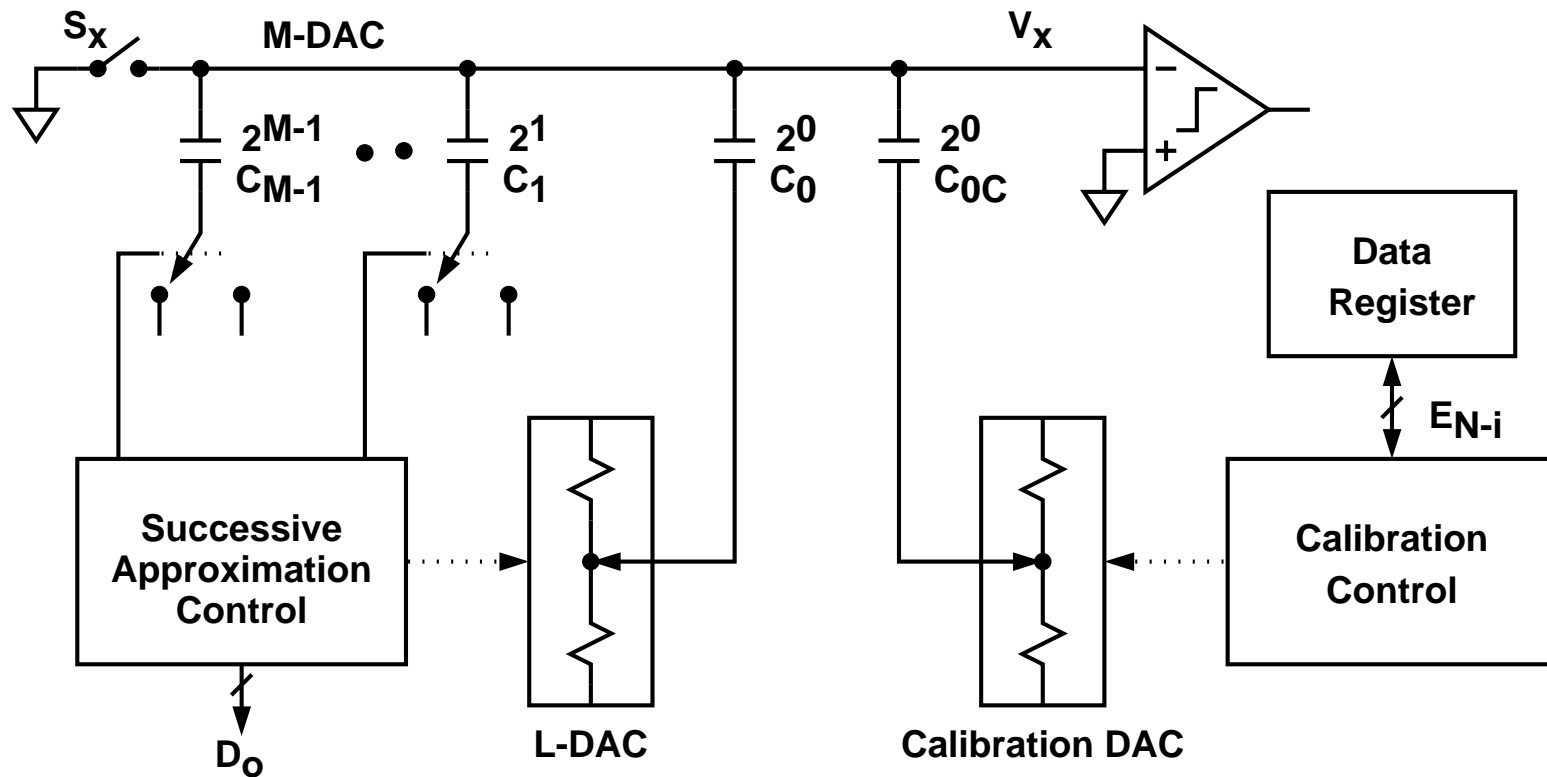
# C-R ADCs Using Input Offset Storage Technique

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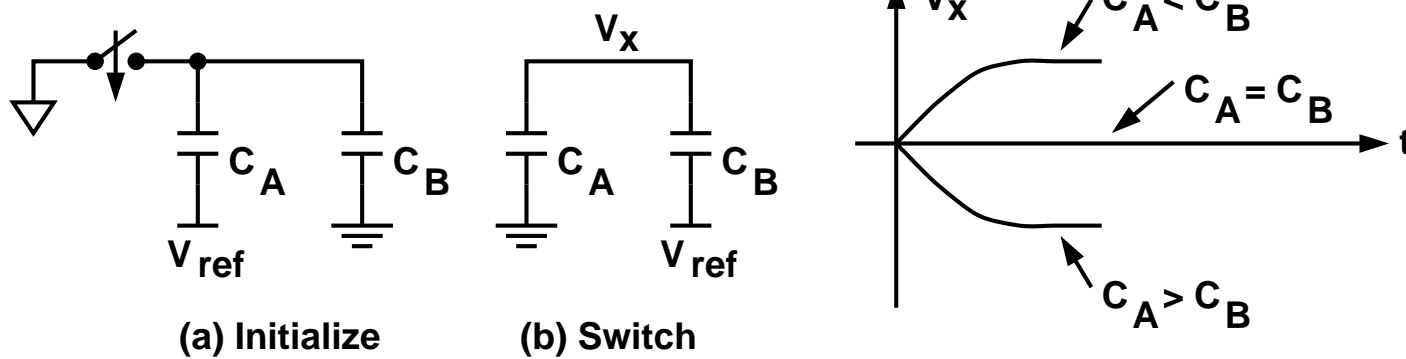


- Non-zero comparator offset can be cancelled by referencing  $V_x$  to the offset, rather than GND during sampling.

# Self-Calibrating Charge-Redistribution ADCs



## Calibration Basic Concept



# Self-Calibrating Charge-Redistribution ADCs

---

- The error voltage  $V_x$ , thus the capacitor mismatch, can be digitized by the Calibration DAC.
- During the calibration, the capacitor mismatches in  $C_{M-1}, C_{M-2}, \dots, C_0$  are measured sequentially, and stored in the data register.
- During the normal operation, the calibration DAC generate a correction voltage that compensates the error voltage caused by the mismatches in the capacitor array
- The binary-weighted capacitor array has an accuracy of about 10 bits. With self-calibration, 16-bit resolution is possible.
- Reference: H-S Lee, JSSC 12/84, pp. 813–819.

# Self-Calibrating Charge-Redistribution ADCs

---

Let

$$C_{tot} = C_{M-1} + C_{M-2} + \cdots + C_1 + C_0 + C_{0C} + C_p$$

Capacitor  $C_{M-1}$  calibration

$$C_A = C_{M-1} \equiv \frac{1}{2}C_{tot} + \Delta C_{M-1}$$

$$C_B = C_{M-2} + \cdots + C_1 + C_0 + C_{0C} = \frac{1}{2}C_{tot} - \Delta C_{M-1}$$

$$V_x = -V_{ref} \cdot \frac{C_A - C_B}{C_{tot}} = -V_{ref} \cdot \frac{2\Delta C_{M-1}}{C_{tot}}$$

- Using the C-DAC to digitize  $V_x$ , we obtain  $D_x$ .
- Store  $E_{M-1}$  in the data register as

$$E_{M-1} = \frac{1}{2}D_x = -V_{ref} \cdot \frac{\Delta C_{M-1}}{C_{tot}}$$

# Self-Calibrating Charge-Redistribution ADCs

---

Capacitor  $C_{M-2}$  calibration

$$C_A = C_{M-2} \equiv \frac{1}{4}C_{tot} + \Delta C_{M-2}$$

$$C_B = C_{M-3} + \cdots + C_1 + C_0 + C_{0C} = \frac{1}{4}C_{tot} - \Delta C_{M-1} - \Delta C_{M-2}$$

$$V_x = -V_{ref} \cdot \frac{C_A - C_B}{C_{tot}} = -V_{ref} \cdot \frac{\Delta C_{M-1} + 2\Delta C_{M-2}}{C_{tot}}$$

- Using the C-DAC to digitize  $V_x$ , we obtain  $D_x$ .
- Store  $E_{M-2}$  in the data register as

$$E_{M-2} = \frac{1}{2} (D_x - E_{M-1}) = -V_{ref} \cdot \frac{\Delta C_{M-2}}{C_{tot}}$$

# Self-Calibrating Charge-Redistribution ADCs

---

Capacitor  $C_i$  calibration,  $i = M - 2, M - 3, \dots$

$$C_A \equiv \frac{1}{2^{M-i}} C_{tot} + \Delta C_i$$

$$C_B = \frac{1}{2^{M-i}} C_{tot} - \sum_{j=i+1}^{M-1} \Delta C_j - \Delta C_i$$

$$V_x = -V_{ref} \cdot \frac{\sum_{j=i+1}^{M-1} \Delta C_j + 2\Delta C_i}{C_{tot}}$$

- Using the C-DAC to digitize  $V_x$ , we obtain  $D_x$ .
- Store  $E_i$  in the data register as

$$E_i = \frac{1}{2} \left[ D_x - \sum_{j=i+1}^{M-1} E_j \right] = -V_{ref} \cdot \frac{\Delta C_i}{C_{tot}}$$

# Self-Calibrating Charge-Redistribution ADCs

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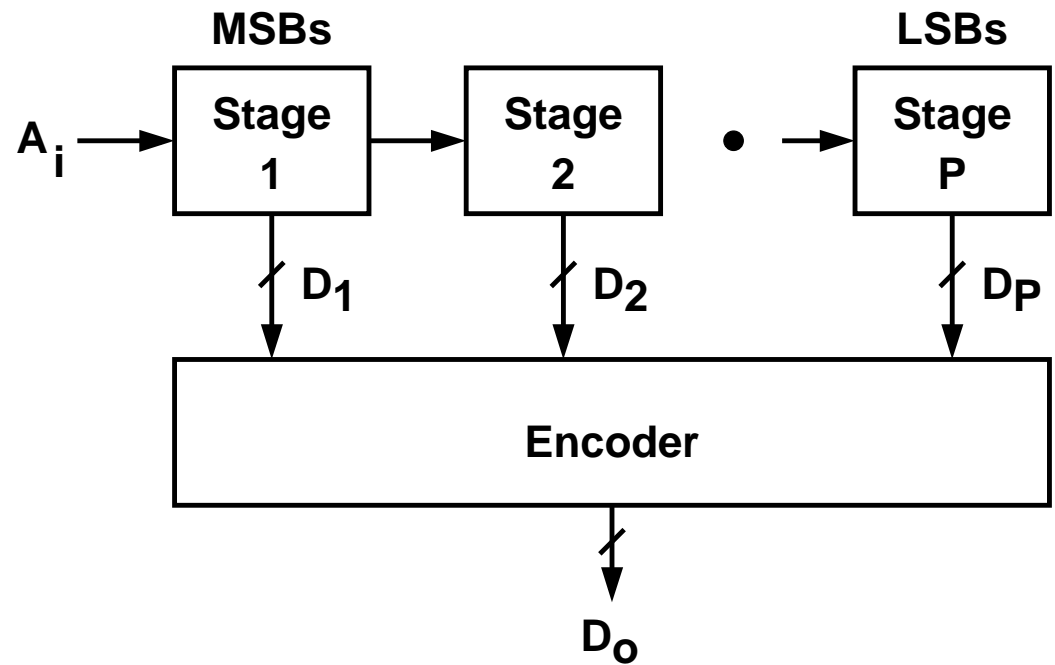
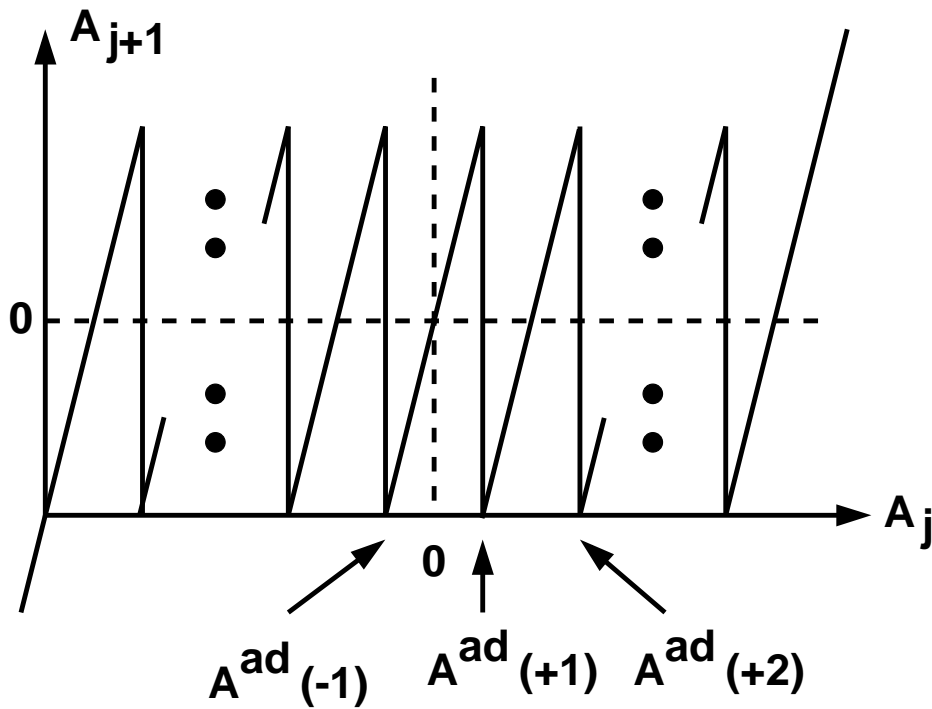
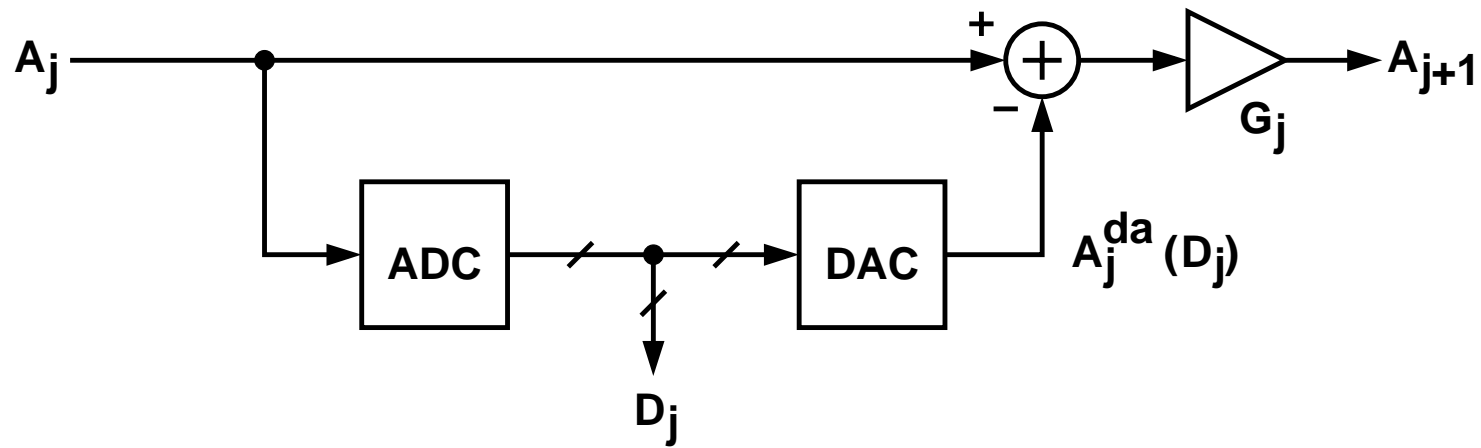
During normal operation, the  $V_x$  generated by the M-DAC is

$$V_x = V_{ref} \sum_0^{M-1} \left( b_{i+L} \cdot \frac{C_i}{C_{tot}} \right)$$

The  $V_x$  is corrected by the C-DAC as

$$\begin{aligned} V_x^c &= V_x + \sum_{i=0}^{M-1} (b_{i+L} \cdot E_i) = V_{ref} \sum_0^{M-1} \left( b_{i+L} \cdot \frac{C_i}{C_{tot}} \right) - V_{ref} \sum_{i=0}^{M-1} \left( b_{i+L} \cdot \frac{\Delta C_i}{C_{tot}} \right) \\ &= V_{ref} \sum_{i=0}^{M-1} \left( b_{i+L} \cdot \frac{C_i - \Delta C_i}{C_{tot}} \right) \\ &= \frac{V_{ref}}{2^M} \sum_{i=0}^{M-1} (b_{i+L} \cdot 2^i) \end{aligned}$$

# Quantized-Feedforward (Subranging) Architectures



# Quantized-Feedforward (Subranging) Architectures

---

The relationship between  $A_j$  and  $A_{j+1}$  is

$$A_{j+1} = \left[ A_j - A_j^{\text{da}}(D_j) \right] \cdot G_j \quad \Rightarrow \quad A_j = A_j^{\text{da}}(D_j) + \frac{A_{j+1}}{G_j}$$

The input  $A_j$  can be expressed as

$$A_j = A_1^{\text{da}} + \frac{A_2^{\text{da}}}{G_1} + \frac{A_3^{\text{da}}}{G_1 G_2} + \dots + \frac{A_P^{\text{da}}}{G_1 G_2 \dots G_{P-1}} + \frac{A_{P+1}}{G_1 G_2 \dots G_P}$$

- If  $A_j^{\text{da}}(D_j)$  and  $G_j$  are known,  $A_j$  can be computed from  $D_1, D_2, \dots, D_P$ .
- The term,  $Q = A_{P+1}/(G_1 G_2 \dots G_P)$ , is the conversion error (quantization error).
- $A_j^{\text{ad}}$  has no effect on the A/D result.
- $G_j$  may include sample-and-hold function for pipeline or cyclic operation.

# Quantized-Feedforward (Subranging) Architectures

---

If the  $G_j$  amplifier has dc offset, i.e.,

$$A_{j+1} = \left[ A_j - A_j^{\text{da}}(D_j) - A_j^{\text{os}} \right] \cdot G_j \quad \Rightarrow \quad A_j = A_j^{\text{da}}(D_j) + A_j^{\text{os}} + \frac{A_{j+1}}{G_j}$$

The input  $A_j$  can be expressed as

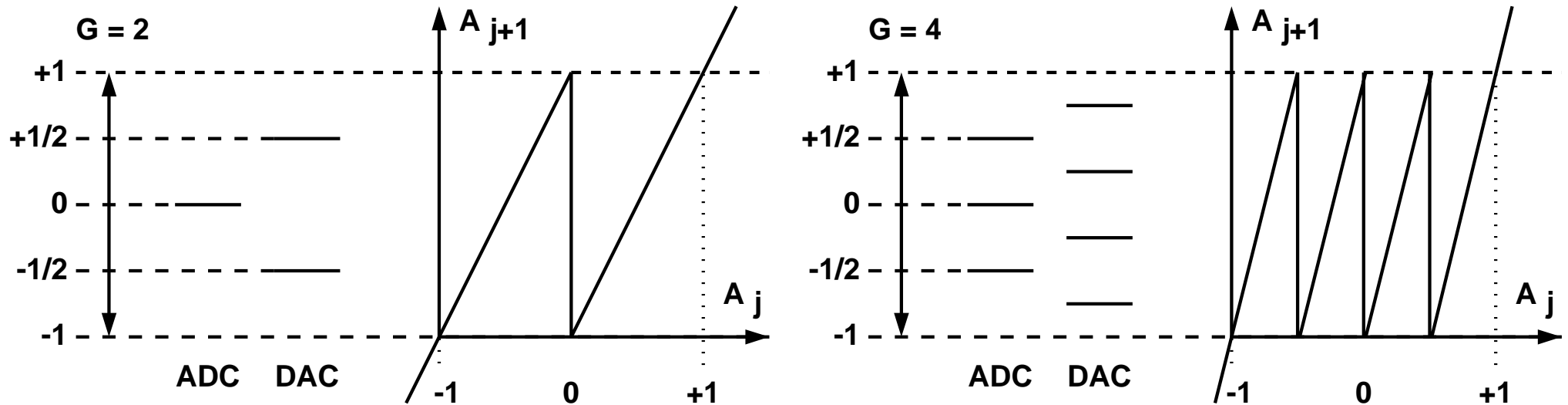
$$A_j = A_1^{\text{da}} + \frac{A_2^{\text{da}}}{G_1} + \frac{A_3^{\text{da}}}{G_1 G_2} + \dots + \frac{A_P^{\text{da}}}{G_1 G_2 \dots G_{P-1}} + \frac{A_{P+1}}{G_1 G_2 \dots G_P} + A^{\text{os}}$$

The entire system has an dc offset of

$$A^{\text{os}} = A_1^{\text{os}} + \frac{A_2^{\text{os}}}{G_1} + \frac{A_3^{\text{os}}}{G_1 G_2} + \dots + \frac{A_P^{\text{os}}}{G_1 G_2 \dots G_{P-1}}$$

- Ref: E. Soenen and R. Geiger, "An Architecture and An Algorithm for Fully Digital Correction of Monolithic Pipelined ADC's," IEEE CAS II, pp. 143–153, March 1995.

# Quantized-Feedforward Minimal Design



$$G = G_1 = G_2 = \dots = G_P = \text{integer} \quad \Delta A = \frac{2}{G} \quad Q = \frac{A_{P+1}}{G_1 G_2 \dots G_P} < \frac{1}{G^P}$$

$$\text{Effective Number of Bit} = N = \log_2 \frac{1}{Q_{max}} = P \times \log_2 G$$

- There are  $M = G - 1$  comparators in the ADC.  $G$  is preferred to be power of 2.
- $D_j$  has  $M + 1$  different values, and the DAC has corresponding  $M + 1$  different output values.

# Over-Range in the Minimal Design

---

Assume nonideal ADC, DAC, and G, as

$$\hat{A}_j^{\text{ad}} = A_j^{\text{ad}} + \epsilon_j^{\text{ad}} \quad \hat{A}_j^{\text{da}} = A_j^{\text{da}} + \epsilon_j^{\text{da}} \quad \hat{G}_j = G_j \times (1 + \epsilon_j^{\text{g}})$$

Then we have

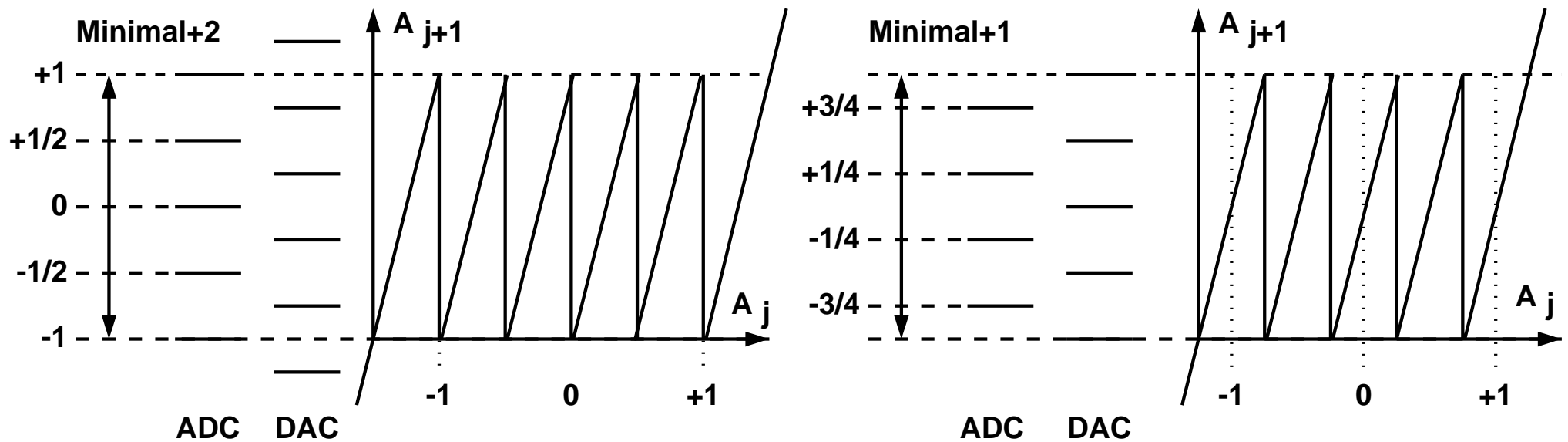
$$A_{j+1} = \left[ A_j - A_j^{\text{da}}(D_j) + (\epsilon_j^{\text{ad}} - \epsilon_j^{\text{da}}) \right] \cdot \hat{G}_j = \left[ A_j - A_j^{\text{da}}(D_j) \right] \cdot G_j + \text{OR}$$

The over range, OR, is

$$\text{OR} = \left[ A_j - A_j^{\text{da}}(D_j) \right] \epsilon_j^{\text{g}} G_j + (\epsilon_j^{\text{ad}} - \epsilon_j^{\text{da}}) \cdot \hat{G}_j \leq \epsilon_j^{\text{g}} + (\epsilon_j^{\text{ad}} - \epsilon_j^{\text{da}}) \cdot \hat{G}_j$$

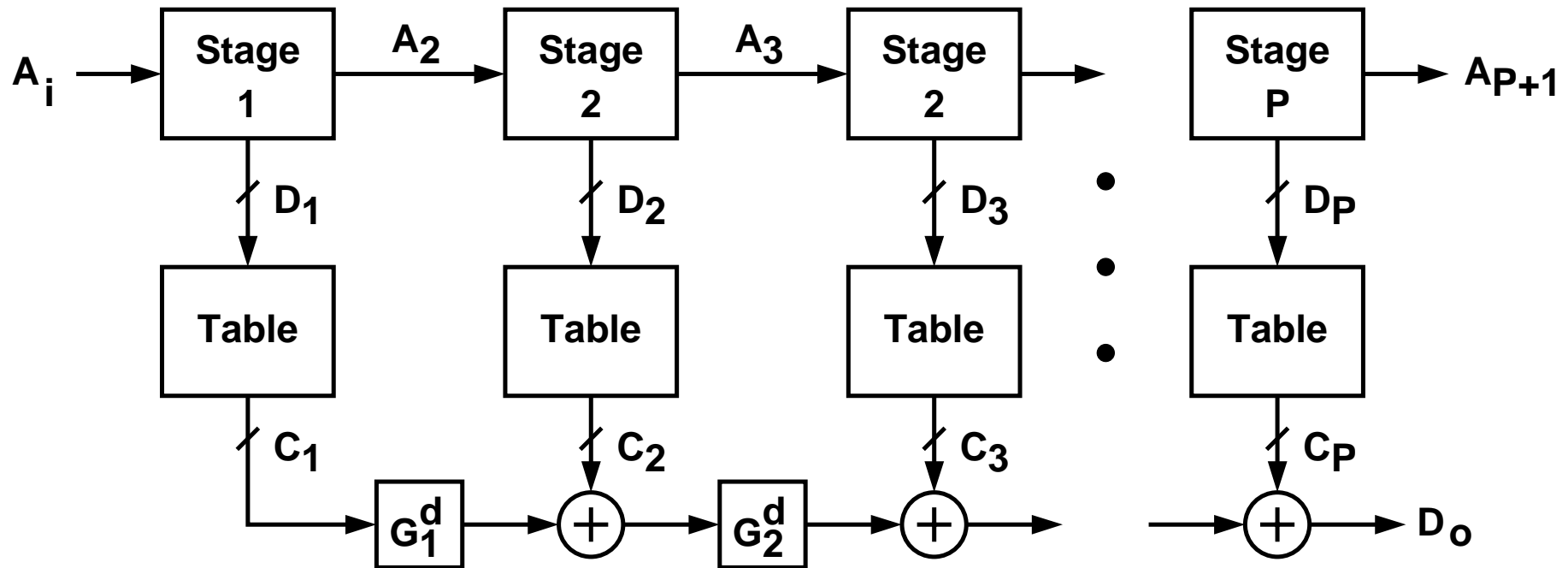
- Nonideal ADC, DAC, and G, can cause  $A_{j+1}$  in minimal design stretching over the nominal input range of the  $j + 1$  stage.

# Quantized-Feedforward Redundant Design



- To increase the nominal input range, one can increase  $M$ , the number of comparators in the ADCs, and the corresponding output levels in the DACs.
- The minimal+2 design provides an over-range capability of  $\pm\Delta A$ . The minimal+1 design provides an over-range capability of  $\pm\Delta A/2$ .
- It is also possible to avoid the over-range phenomenon by decreasing  $G_j$ .

# Digital Encoding for the Quantized-Feedforward Architecture



$$A_i = A_1^{da} + \frac{A_2^{da}}{G_1} + \frac{A_3^{da}}{G_1 G_2} + \dots + \frac{A_P^{da}}{G_1 G_2 \dots G_{P-1}} + Q$$

$$(A_i - Q) \cdot G_1^d G_2^d \dots G_{P-1}^d$$

$$= \left( \left( \left( A_1^{da} \right) G_1^d + A_2^{da} \frac{G_1^d}{G_1} \right) G_2^d + A_3^{da} \frac{G_1^d G_2^d}{G_1 G_2} \right) G_3^d + \dots + A_P^{da} \frac{G_1^d G_2^d \dots G_{P-1}^d}{G_1 G_2 \dots G_{P-1}}$$

# Digital Encoding for the Quantized-Feedforward Architecture

---

Let

$$C_j = A_j^{\text{da}}(D_j) \cdot \frac{G_1^d G_2^d \cdots G_{j-1}^d}{G_1 G_2 \cdots G_{j-1}}$$

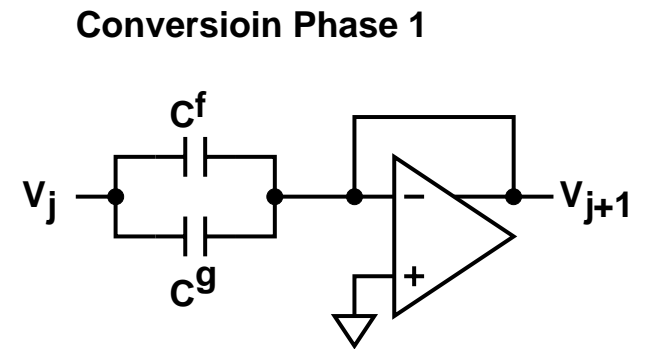
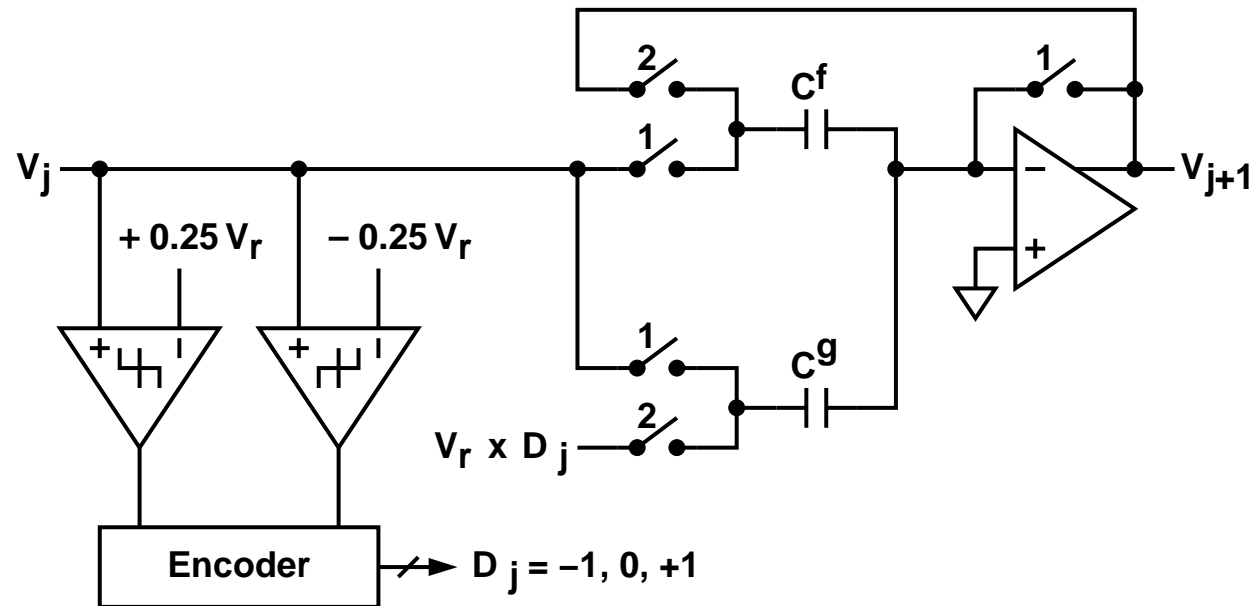
The digital output can be obtained by

$$D_o = \left( (C_1) G_1^d + C_2 \right) G_2^d + \cdots + C_{P-1} \left) G_{P-1}^d + C_P$$

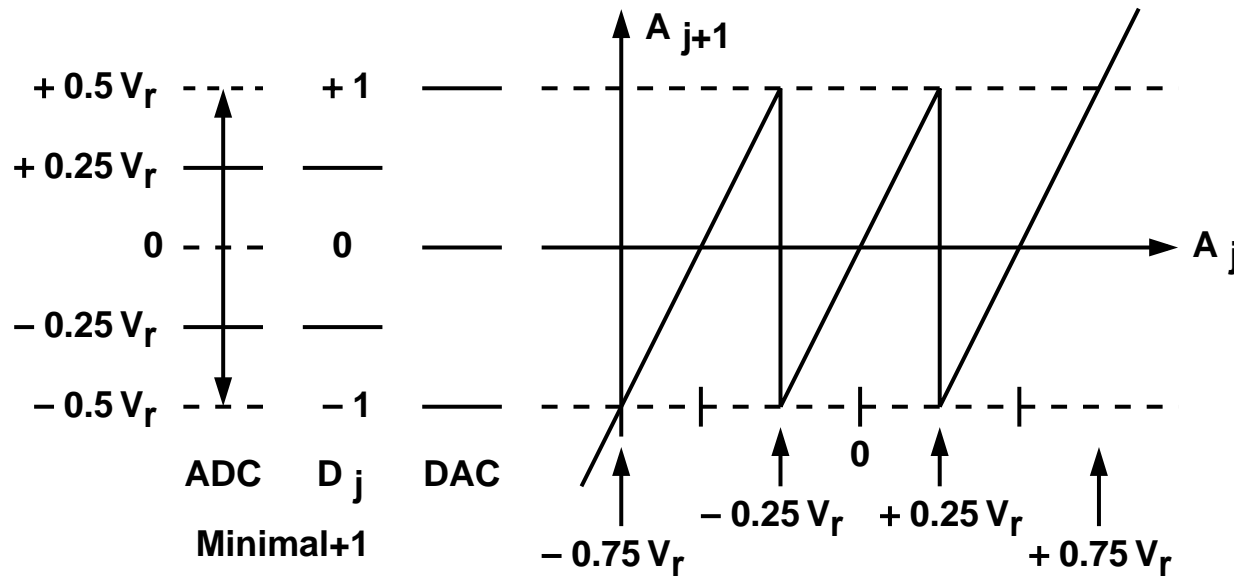
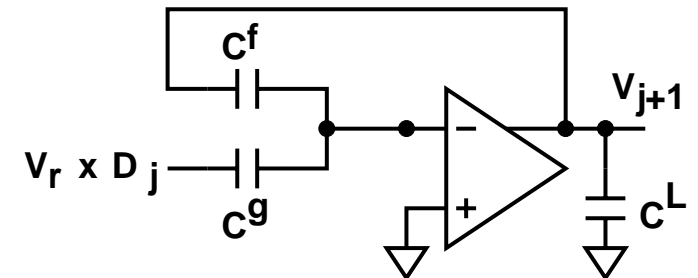
- Nonlinear A/D conversion occurs, if

$$C_j \neq \hat{A}_j^{\text{da}}(D_j) \cdot \frac{G_1^d G_2^d \cdots G_{j-1}^d}{\hat{G}_1 \hat{G}_2 \cdots \hat{G}_{j-1}}$$

# A Radix-2 1.5 Bit SC Pipeline Stage



Conversion Phase 2



## A Radix-2 1.5 Bit SC Pipeline Stage

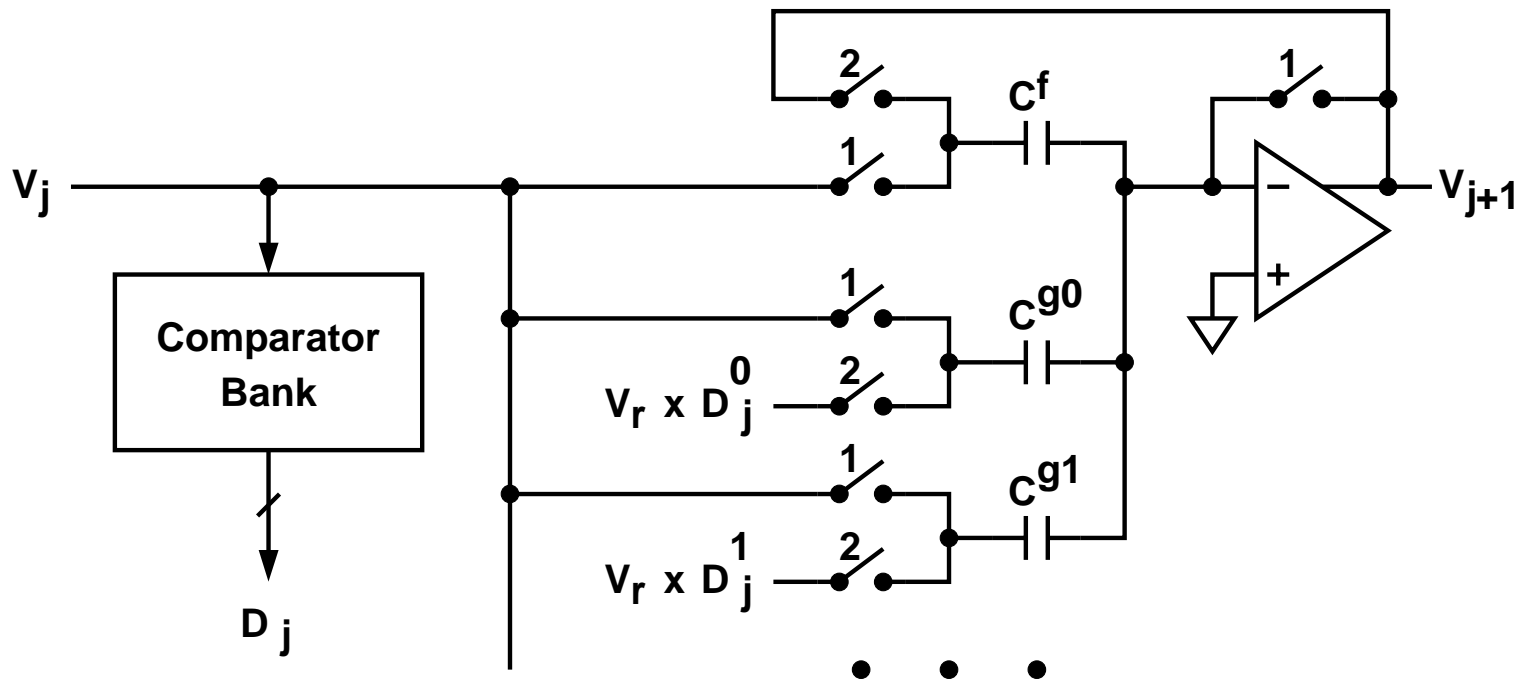
---

During phase 2

$$\begin{aligned} V_{j+1} &= V_j + \frac{C^g}{C^f}(V_j - V_r \times D_j) = \left(1 + \frac{C^g}{C^f}\right) \left(V_j - \frac{V_r}{1 + C^f/C^g} \times D_j\right) \\ &= 2 \times \left(V_j - \frac{V_r}{2} \times D_j\right) \quad \text{if} \quad C^f = C^g \end{aligned}$$

- The full range of the input/output is  $\pm 0.5V_r$ .
- The pipeline stage has input over-range capability of  $\pm 0.25V_r$ .

# Multi-Bit Switched-Capacitor Pipeline Stage



$$D_j = D_j^0 \cdot 2^0 + D_j^1 \cdot 2^1 + \dots + D_j^{K-1} \cdot 2^{K-1} \quad D_j^k \in \{-1, 0, +1\}$$

$$\frac{C^f}{2^0} = \frac{C^{g0}}{2^0} = \frac{C^{g1}}{2^1} = \dots = \frac{C^{g(K-1)}}{2^{K-1}} = C$$

$$V_{j+1} = G_j \times (V_j - \Delta V \times D_j) \quad G_j = 1 + \frac{C^{g0} + C^{g1} + \dots + C^{g(K-1)}}{C^f} = 2^K \quad \Delta V = \frac{V_r}{2^K}$$

# Switched-Capacitor Pipelined ADCs

---

The SC stage has a voltage gain of

$$G = 1 + \frac{C^g}{C^f} \quad C^g = C^{g0} + C^{g1} + C^{g2} + \dots$$

The settling time requirement can be expressed as

$$T_s = \frac{C^f + C^L}{G_m} \left( 1 + \frac{C^g}{C^f} + \frac{C^i}{C^f} \right) \cdot \ln 2^{y+1} \quad \Rightarrow \quad G_m = \frac{C^f + C^L}{T_s} \left( G + \frac{C^i}{C^f} \right) \cdot (y + 1) \ln 2$$

Other constraints are

$$\text{Total Power} \propto G_{m,1} + G_{m,2} + \dots + G_{m,P}$$

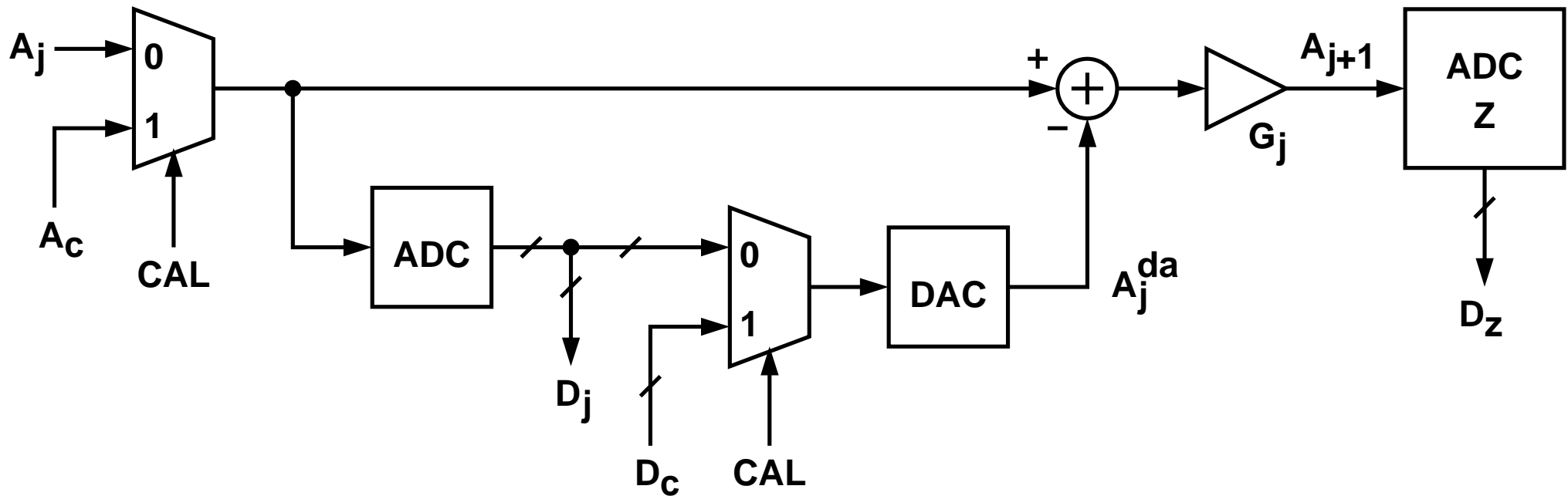
$$\text{Total Input Referred Thermal Noise Power} = P_\theta \sim kT \left[ \frac{1}{C_1^s} + \frac{1}{(G_1)^2 C_2^s} + \frac{1}{(G_1 G_2)^2 C_3^s} \dots \right]$$

# Switched-Capacitor Pipelined ADCs

---

- $G_m$  is the opamp's transconductance.
- $C^i$  is the opamp's input capacitance.
- $C_j^s = C_j^f + C_j^g$  is the  $j$ -stage sampling capacitances.
- $C^L$  includes  $C_{j+1}^s$  and input loading of the comparator bank in the  $j + 1$  stage.
- $y$  (bits) is the resolution requirement of the  $j$  stage.
- Use capacitor scaling,  $\alpha = C_j^s / C_{j+1}^s$ , total power dissipation can be minimized while maintaining noise performance. It can be shown that  $\alpha_{\text{opt}} \sim G$ .
- Increasing  $G$  (and  $M$ ) per stage generally reduces total power dissipation.
- Reference: D. Cline and P. Gray, "A Power Optimized 13-b 5Ms/s Pipelined ADC," JSSC, March 1996, pp. 294–303.

# Single-Stage Calibration and Digital Correction



The signal  $A_{j+1}$  is quantized the following Z-ADC with

$$A_{j+1} = \hat{G}_j \cdot \left[ A_j - \hat{A}_j^{\text{da}}(D_j) - A_j^{\text{os}} \right] = \frac{G}{\hat{G}} \cdot D_z + Q^{\text{os}} + Q$$

- $G/\hat{G}$  is the gain error,  $Q^{\text{os}}$  is the offset, and  $Q$  is the quantization error.

# Single-Stage Calibration and Digital Correction

---

During calibration,  $A_j$  is disabled and  $\hat{A}_j^{\text{da}}(D_c)$  is quantized by measuring

$$\hat{G}_j \cdot [A_c - A^{os}] = \frac{G}{\hat{G}} \cdot D_{z1} + Q^{os} + Q_1$$

$$\hat{G}_j \cdot [A_c - \hat{A}_j^{\text{da}}(D_c) - A^{os}] = \frac{G}{\hat{G}} \cdot D_{z2} + Q^{os} + Q_2$$

Subtracting the above two equations, we have

$$\hat{G}_j \cdot \hat{A}_j^{\text{da}}(D_c) = \frac{G}{\hat{G}} \cdot (D_{z1} - D_{z2}) + Q_1 - Q_2 = \frac{G}{\hat{G}} \cdot D_z(D_c) + 2Q^c(D_c) \quad D_c \in \{D_j\}$$

$$\Rightarrow \hat{A}_j^{\text{da}}(D_c) = \frac{G_j G}{\hat{G}_j \hat{G}} \cdot T_j(D_c) + \frac{2Q^c(D_c)}{\hat{G}_j} \quad T_j(D_c) = \frac{D_z(D_c)}{G_j} \quad D_c \in \{D_j\}$$

# Single-Stage Calibration and Digital Correction

---

The combined ADC with j-Stage and Z-ADC has the following characteristic:

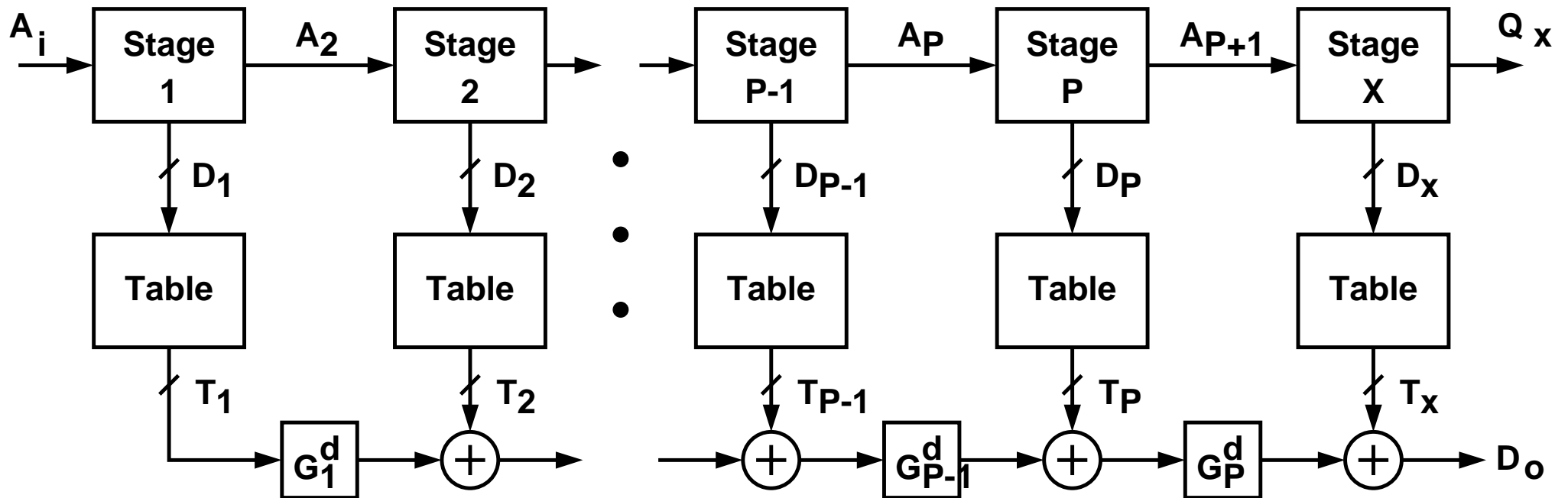
$$\begin{aligned}
 A_j &= \hat{A}_j^{\text{da}}(D_j) + A_j^{\text{os}} + \frac{A_{j+1}}{\hat{G}_j} = \frac{G_j G}{\hat{G}_j \hat{G}} \cdot T_j(D_j) + \frac{2Q^c(D_j)}{\hat{G}_j} + A_j^{\text{os}} + \frac{A_{j+1}}{\hat{G}_j} \\
 &= \frac{G_j G}{\hat{G}_j \hat{G}} \left[ T_j(D_j) + \frac{D_z}{G_j} \right] + \left( A_j^{\text{os}} + \frac{Q^{\text{os}}}{\hat{G}_j} \right) + \frac{2Q^c(D_j) + Q}{\hat{G}_j} \\
 &= \frac{G'}{\hat{G}'} \cdot D'_z + Q'^{\text{os}} + Q'
 \end{aligned}$$

$$\text{Digital Output} = D'_z = T_j(D_j) + \frac{D_z}{G_j} \quad \text{Gain Error} = \frac{G'}{\hat{G}'} = \frac{G_j G}{\hat{G}_j \hat{G}}$$

$$\text{Offset} = Q'^{\text{os}} = A_j^{\text{os}} + \frac{Q^{\text{os}}}{\hat{G}_j} \quad \text{Quantization Error} = Q' = \frac{2Q^c(D_j)}{\hat{G}_j} + \frac{Q}{\hat{G}_j}$$

- Nonideal  $\hat{A}_j^{\text{da}}$  and  $\hat{G}_j$  have no effect on the A/D linearity.

# Multi-Stage Calibration and Digital Correction



Assume the stage X ADC has a characteristic of

$$A_{P+1} = \frac{G_x}{\hat{G}_x} \cdot T_x + Q_x^{OS} + Q_x$$

- Calibration is performed stage-by-stage, from Stage P to Stage 1.

# Multi-Stage Calibration and Digital Correction

---

Use the  $X$  ADC to calibrate stage  $P$ . Then, the  $P + X$  ADC can be expressed as

$$A_P = \frac{G_P G_X}{\hat{G}_P \hat{G}_X} \left[ T_P + \frac{T_X}{G_P} \right] + \left( A_P^{\text{OS}} + \frac{Q_X^{\text{OS}}}{\hat{G}_P} \right) + \frac{2Q_{X,P}^c + Q_X}{\hat{G}_P}$$

Use the  $P + X$  ADC to calibrate stage  $(P - 1)$ . Then, the  $(P - 1) + P + X$  ADC can be expressed as

$$A_{P-1} = \frac{G_{P-1} G_P G_X}{\hat{G}_{P-1} \hat{G}_P \hat{G}_X} \left[ T_{P-1} + \frac{T_P}{G_{P-1}} + \frac{T_X}{G_{P-1} G_P} \right] + \left( A_{P-1}^{\text{OS}} + \frac{A_P^{\text{OS}}}{\hat{G}_{P-1}} + \frac{Q_X^{\text{OS}}}{\hat{G}_{P-1} \hat{G}_P} \right) + \frac{2Q_{X,P-1}^c + 2Q_{X,P}^c + Q_X}{\hat{G}_{P-1} \hat{G}_P}$$

Repeat the calibration procedures for stage  $(P - 2)$ ,  $(P - 3)$ ,  $\dots$ , 2, and 1.

# Multi-Stage Calibration and Digital Correction

---

The full calibrated ADC can be expressed as

$$A_i = \frac{G_T}{\hat{G}_T} \left[ T_1 + \frac{T_2}{G_1} + \dots + \frac{T_P}{G_1 G_2 \dots G_{P-1}} + \frac{T_x}{G_1 G_2 \dots G_P} \right] + Q_T^{OS} + Q_T$$

where

$$\frac{G_T}{\hat{G}_T} = \frac{G_1 G_2 \dots G_P G_x}{\hat{G}_1 \hat{G}_2 \dots \hat{G}_P \hat{G}_x}$$

$$Q_T^{OS} = A_1^{OS} + \frac{A_2^{OS}}{\hat{G}_1} + \dots + \frac{A_P^{OS}}{\hat{G}_1 \hat{G}_2 \dots \hat{G}_{P-1}} + \frac{Q_x^{OS}}{\hat{G}_1 \hat{G}_2 + \dots \hat{G}_P}$$

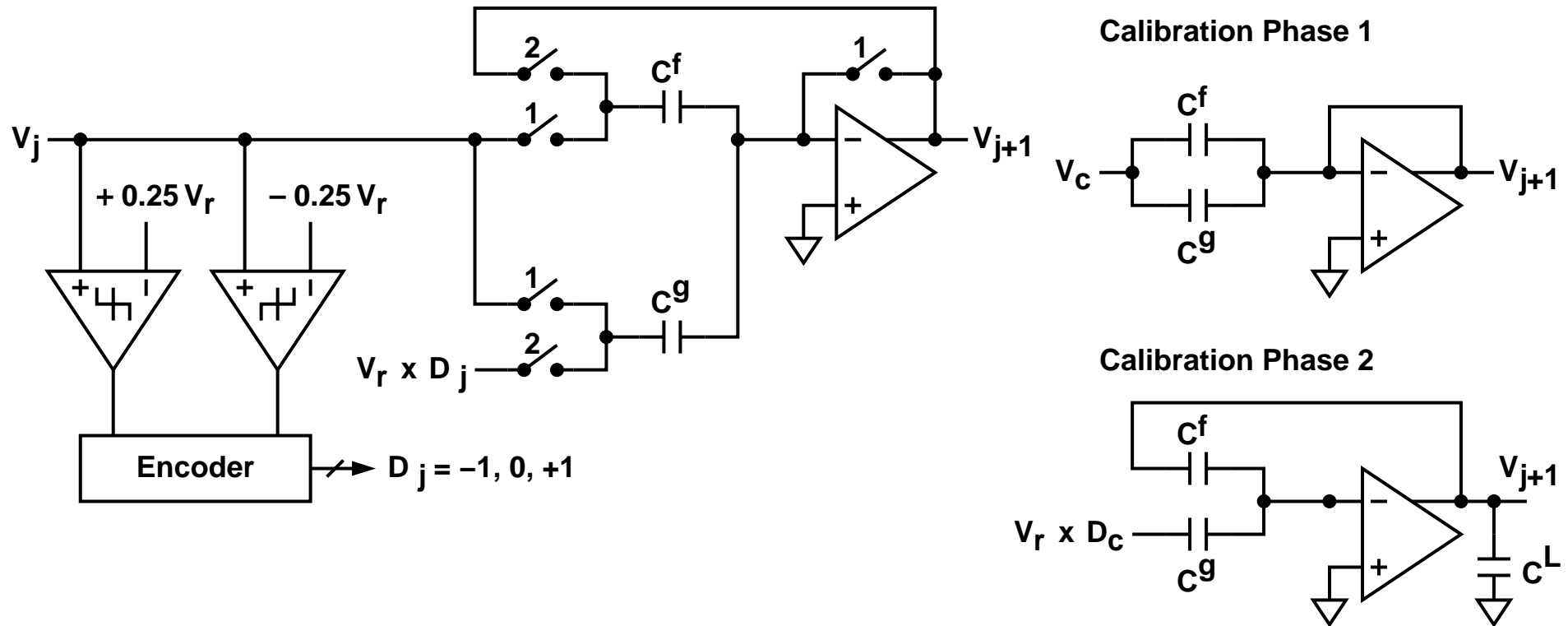
$$Q_T = \frac{2Q_{x,1}^c + 2Q_{x,2}^c + \dots + 2Q_{x,P}^c + Q_x}{\hat{G}_1 \hat{G}_2 \dots \hat{G}_P} \leq \frac{(2P + 1) \times |Q_x|_{max}}{\hat{G}_1 \hat{G}_2 \dots \hat{G}_P}$$

# Multi-Stage Calibration and Digital Correction

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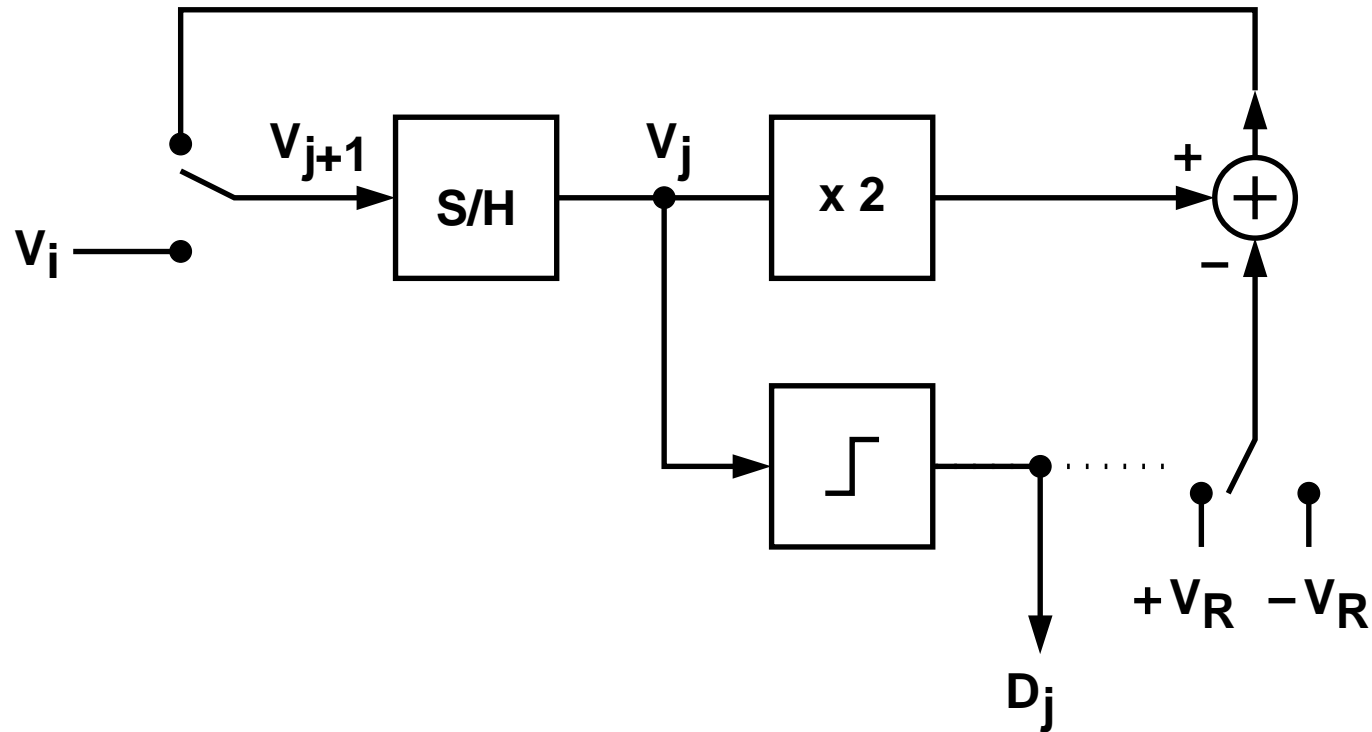
- The scaling factor  $G_T/\hat{G}_T$  and offset  $Q_T^{os}$  can be determined by quantizing two known input, e.g.,  $A_i = 0$  and  $A_i = A_{ref}$ .
- The effects of noise can be suppressed by averaging a number of successive measurements during calibration.
- During  $j$  stage calibration, to avoid overloading the  $A_{j+1}$  port, different  $\hat{A}_j^{da}(D_c)$  measurement may need different  $A_c$  value.
- On the circuit level, the effectiveness of calibration is limited by noises, interferences, nonlinear  $G_j$ , and amplifier transient behavior.

# Calibration of A Radix-2 1.5 Bit SC Pipeline Stage



- To calibrate  $\hat{A}_j^{da}(D_j = 1)$ . Obtain  $D_{z1}$  by letting  $V_c = 0.25V_r$  and  $D_c = 0$ , and obtain  $D_{z2}$  by letting  $V_c = 0.25V_r$  and  $D_c = 1$ . Then  $T_j(D_j = 1) = (D_{z1} - D_{z2})/G_j$ .
- To calibrate  $\hat{A}_j^{da}(D_j = -1)$ . Obtain  $D_{z1}$  by letting  $V_c = -0.25V_r$  and  $D_c = 0$ , and obtain  $D_{z2}$  by letting  $V_c = -0.25V_r$  and  $D_c = -1$ . Then  $T_j(D_j = -1) = (D_{z1} - D_{z2})/G_j$ .

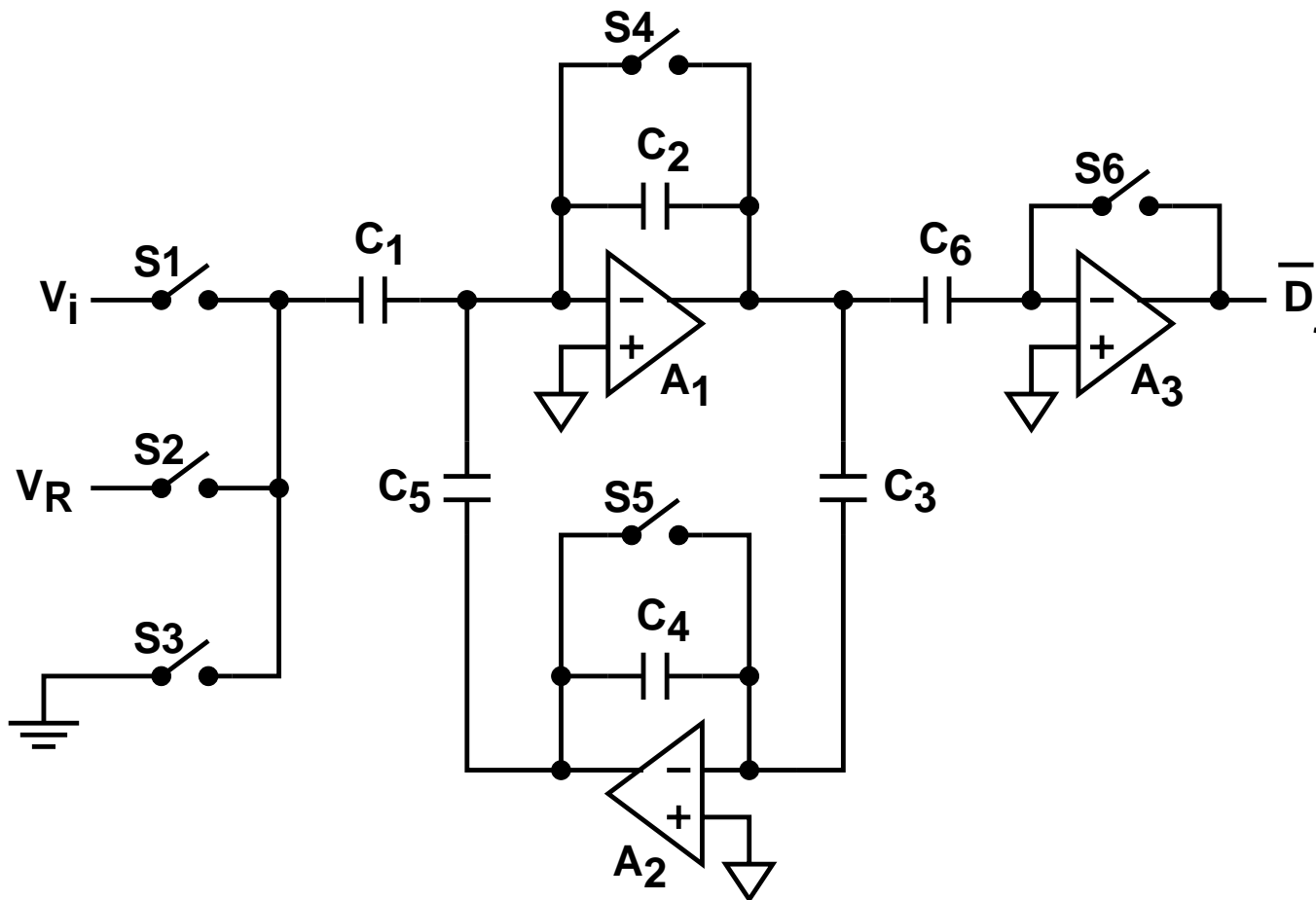
# A Radix-2 Cyclic ADCs



$$V_{j+1} = 2 \times V_j - D_j \times V_R = 2 \times \left( V_j + D_j \cdot \frac{V_R}{2} \right) \quad D_j \in \{+1, -1\}$$

- Start with  $j = 1$  and  $V_1 = V_i$ .
- For each cycle,  $j$  is increased by 1.

# A Radix-2 Switched-Capacitor Cyclic ADC



$$C_1 = C_2 = C_3 = C_4 = C$$

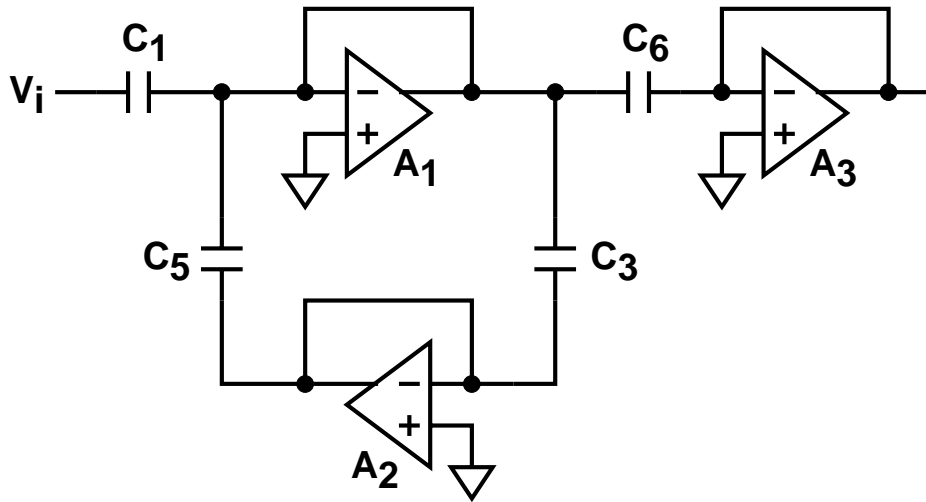
$$C_5 = 2C$$

$$D_j \in \{1, 0\}$$

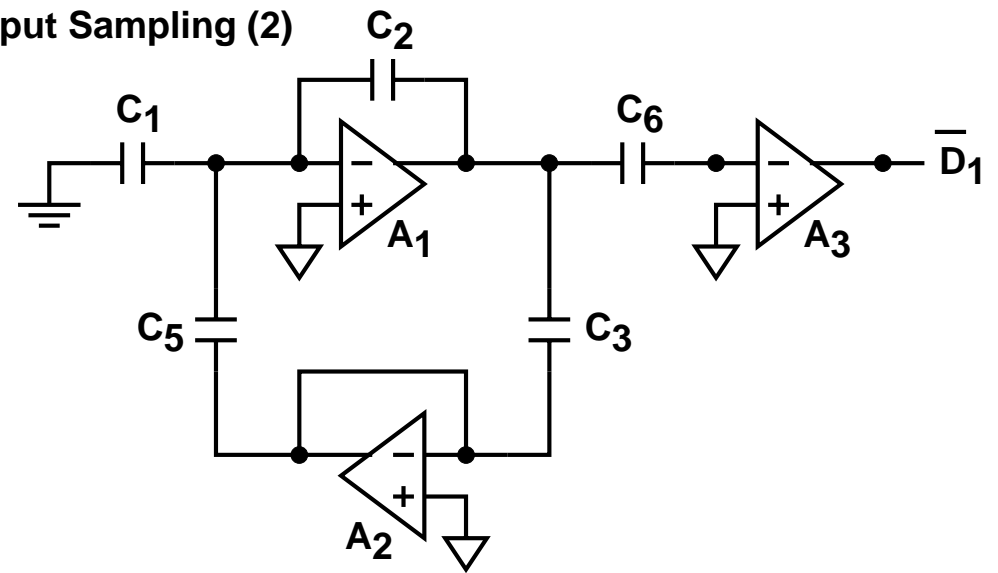
$$V_i = V_R \times \left[ \sum_{j=1}^N (D_j \cdot 2^{-j}) - \frac{1}{2} \right]$$

# A Radix-2 Switched-Capacitor Cyclic ADC

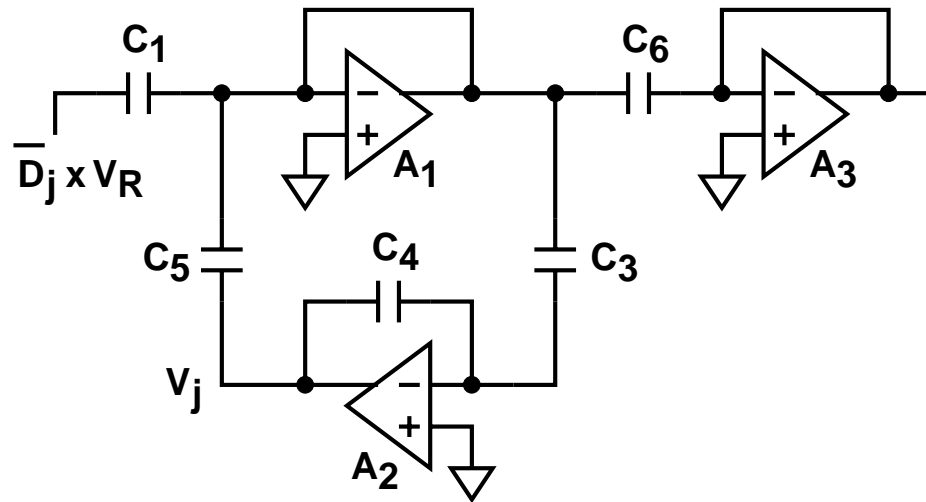
Input Sampling (1)



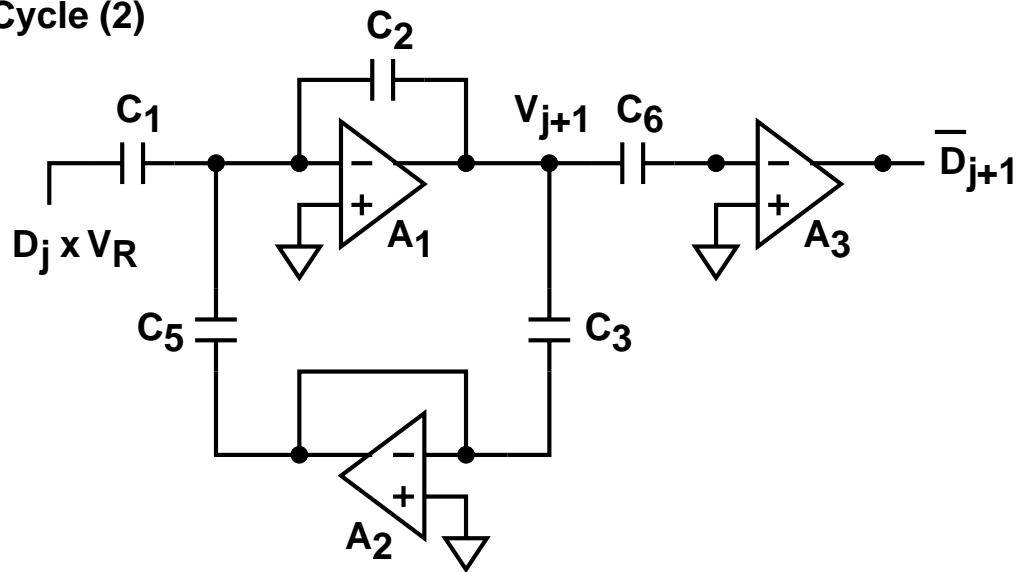
Input Sampling (2)



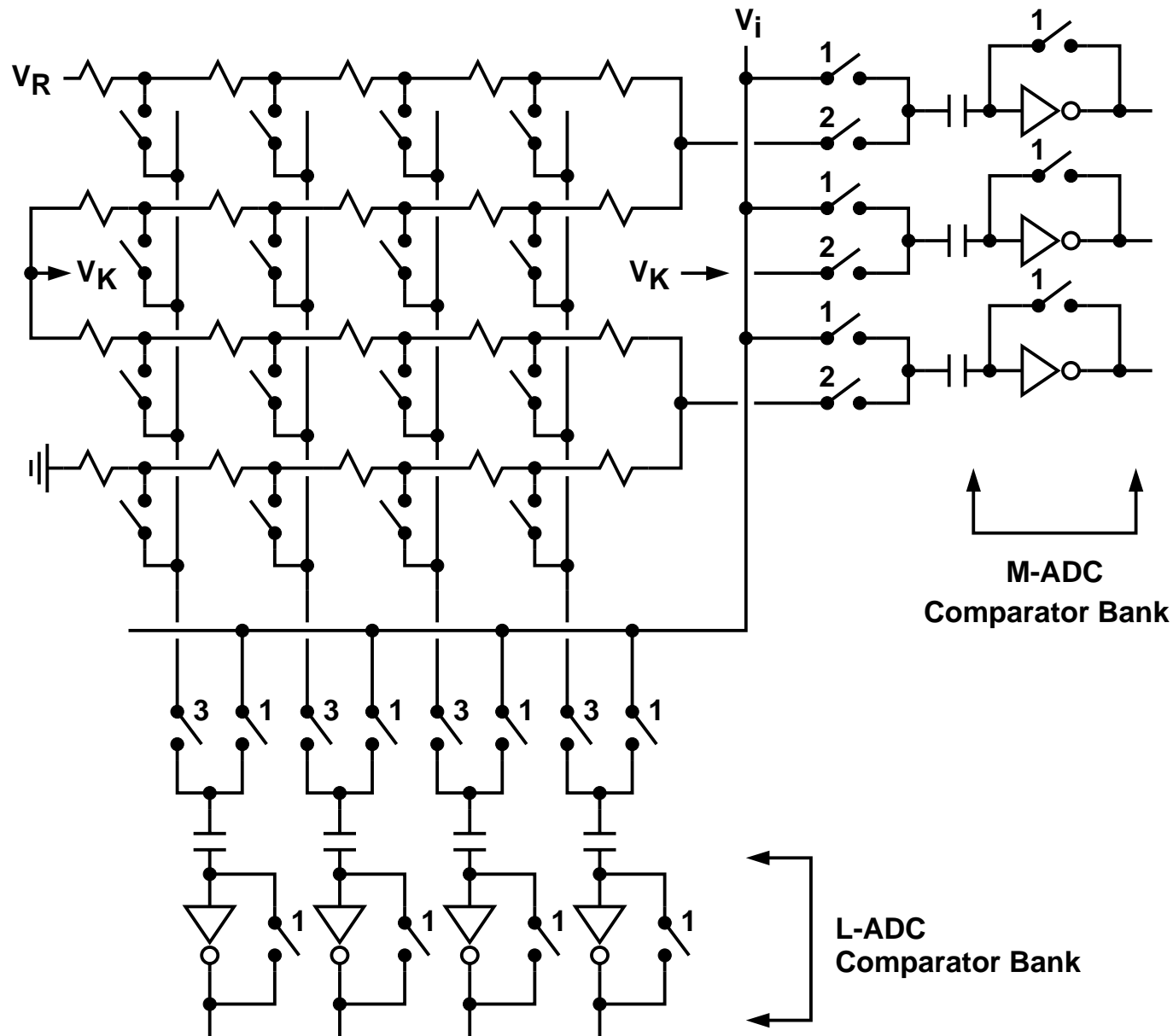
j-Cycle (1)



j-Cycle (2)



# A CMOS Subranging Flash ADC — Dingwall

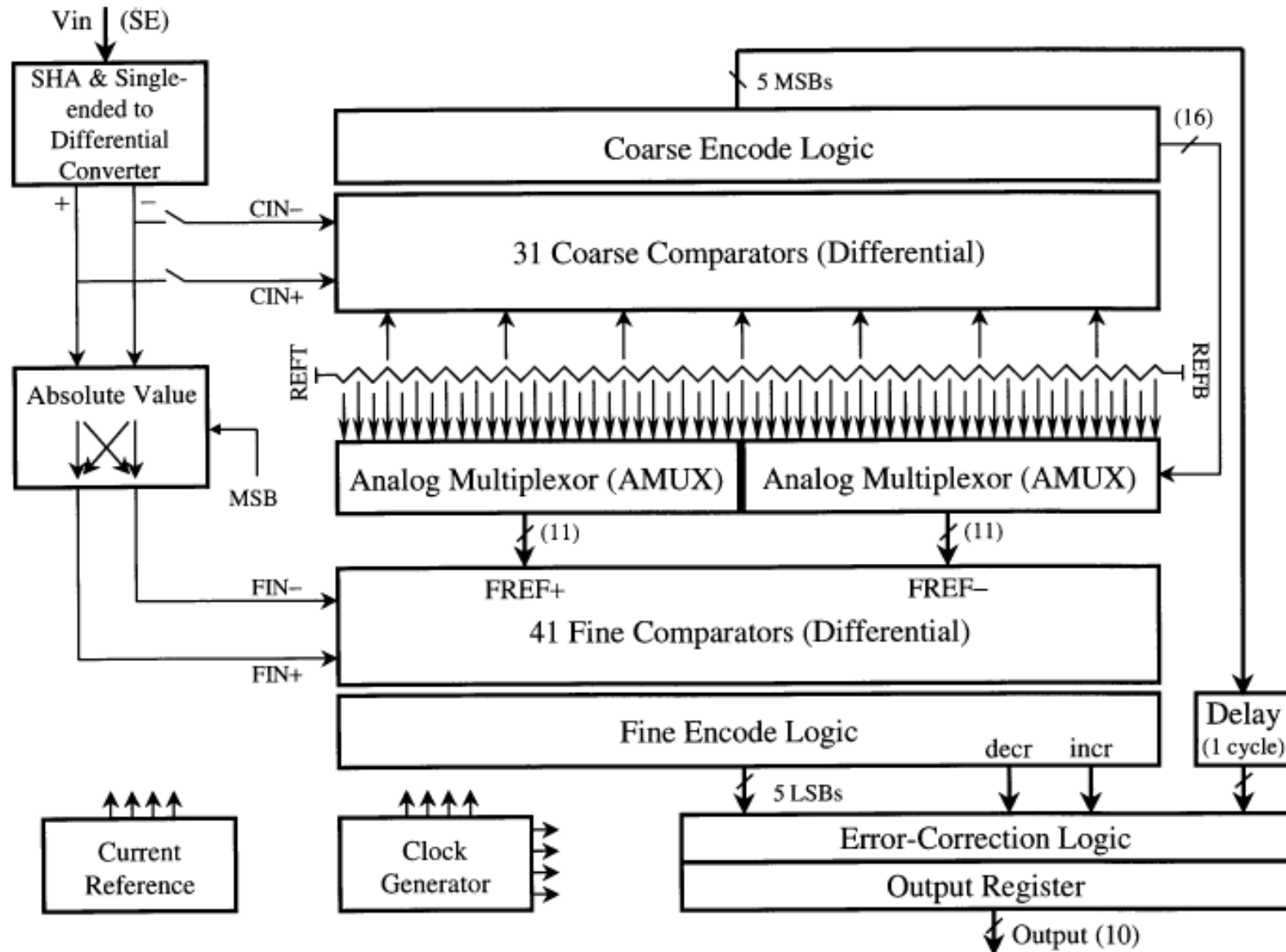


# A CMOS Subranging Flash ADC — Dingwall

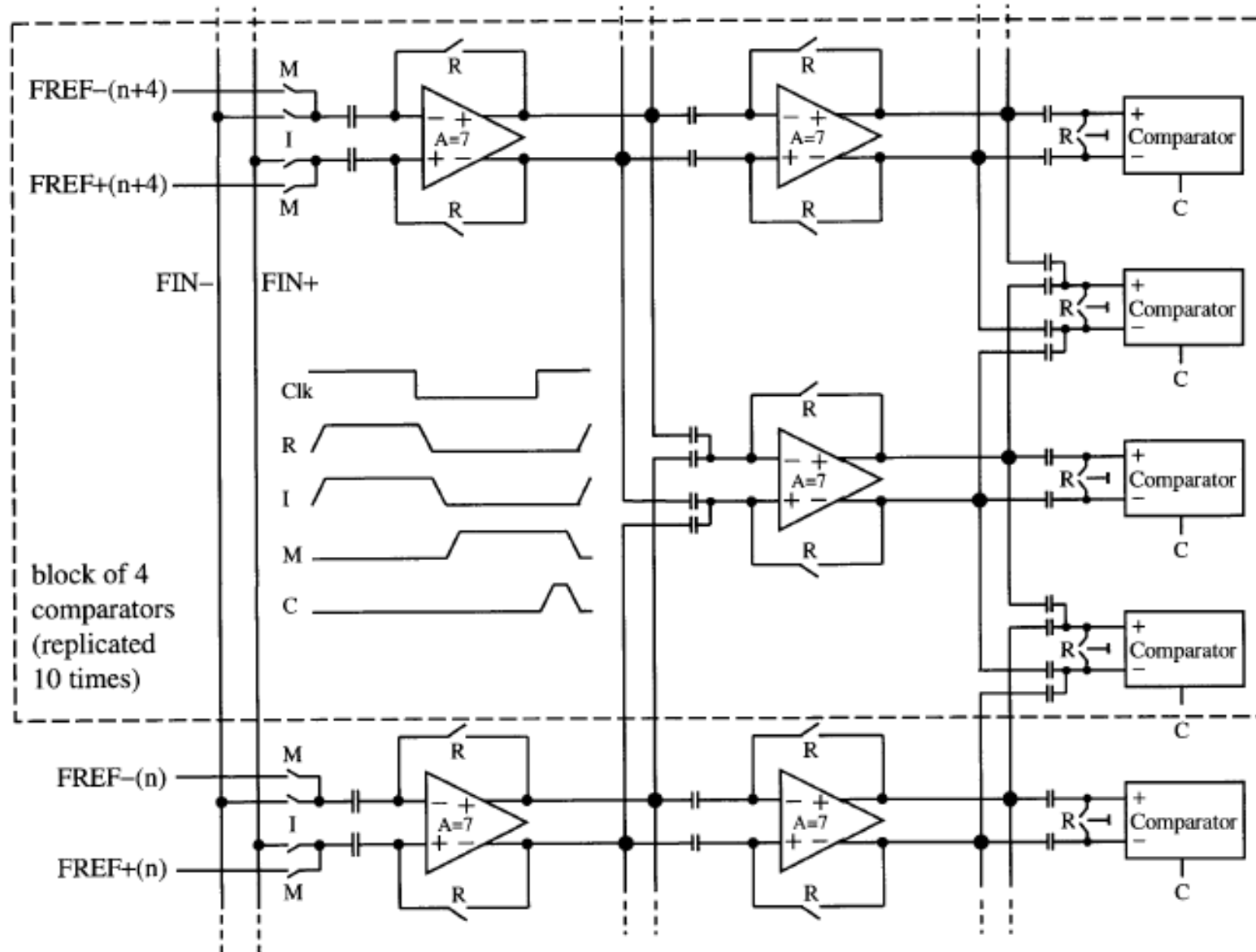
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- Two-Stage quantized-feedforward architecture.
  - The first-stage M-ADC has  $2^M - 1$  comparators, and  $G_1 = 1$ .
  - The second-stage L-ADC has  $2^L - 1$  comparators.
  - For minimal design,  $D_o$  has  $N = M + L$  bits.
- The S/H and the subtractor function is embedded in every comparator. Require no additional subtractor or DAC.
- Comparators in both M-ADC and L-ADC need to have N-bit accuracy.
- The input range of the L-ADC can be extended to prevent over-loading. The accuracy requirement for the M-ADC can then be relaxed.
- Reference: A. Dingwall, et. al., “An 8-MHz CMOS Subranging 8-Bit A/D Converter,” JSSC 12/1985, pp. 1138–1143.

# A CMOS Subranging Flash ADC — Brandt



# Interpolated Differential Comparator Bank

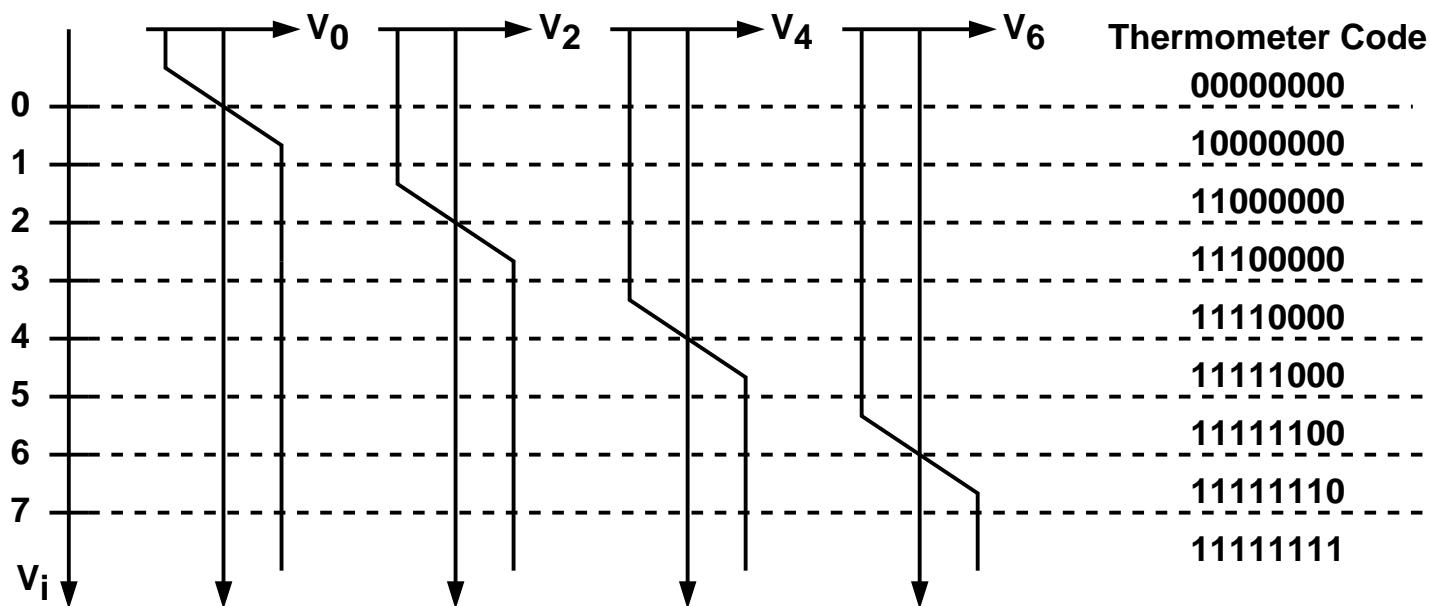
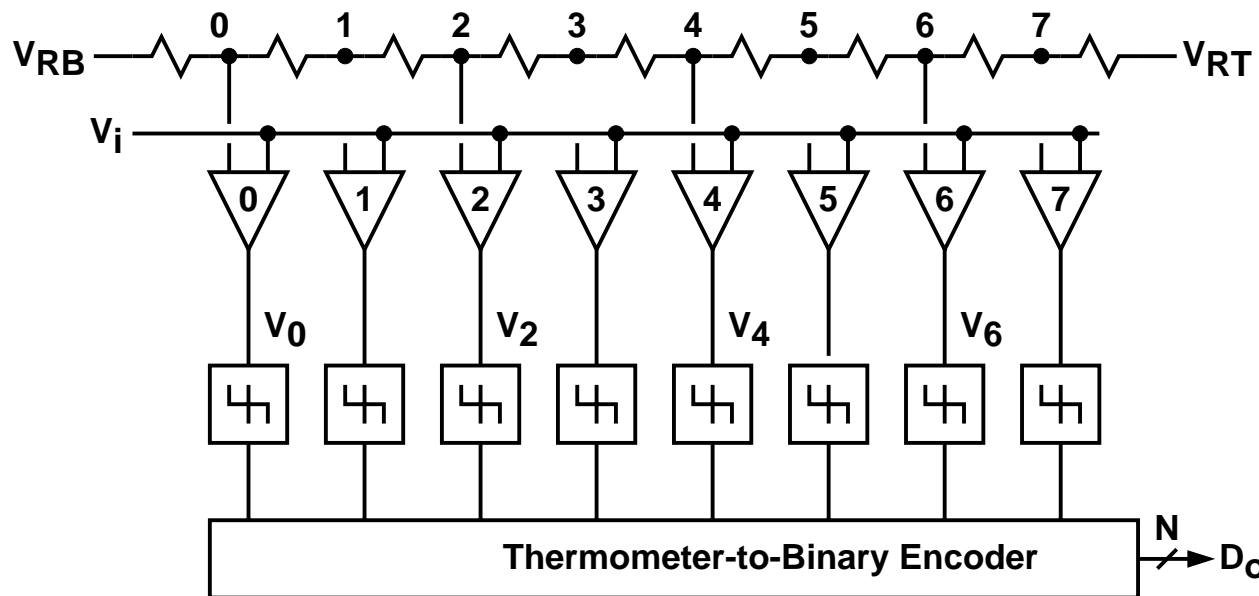


# A CMOS Subranging Flash ADC — Brandt

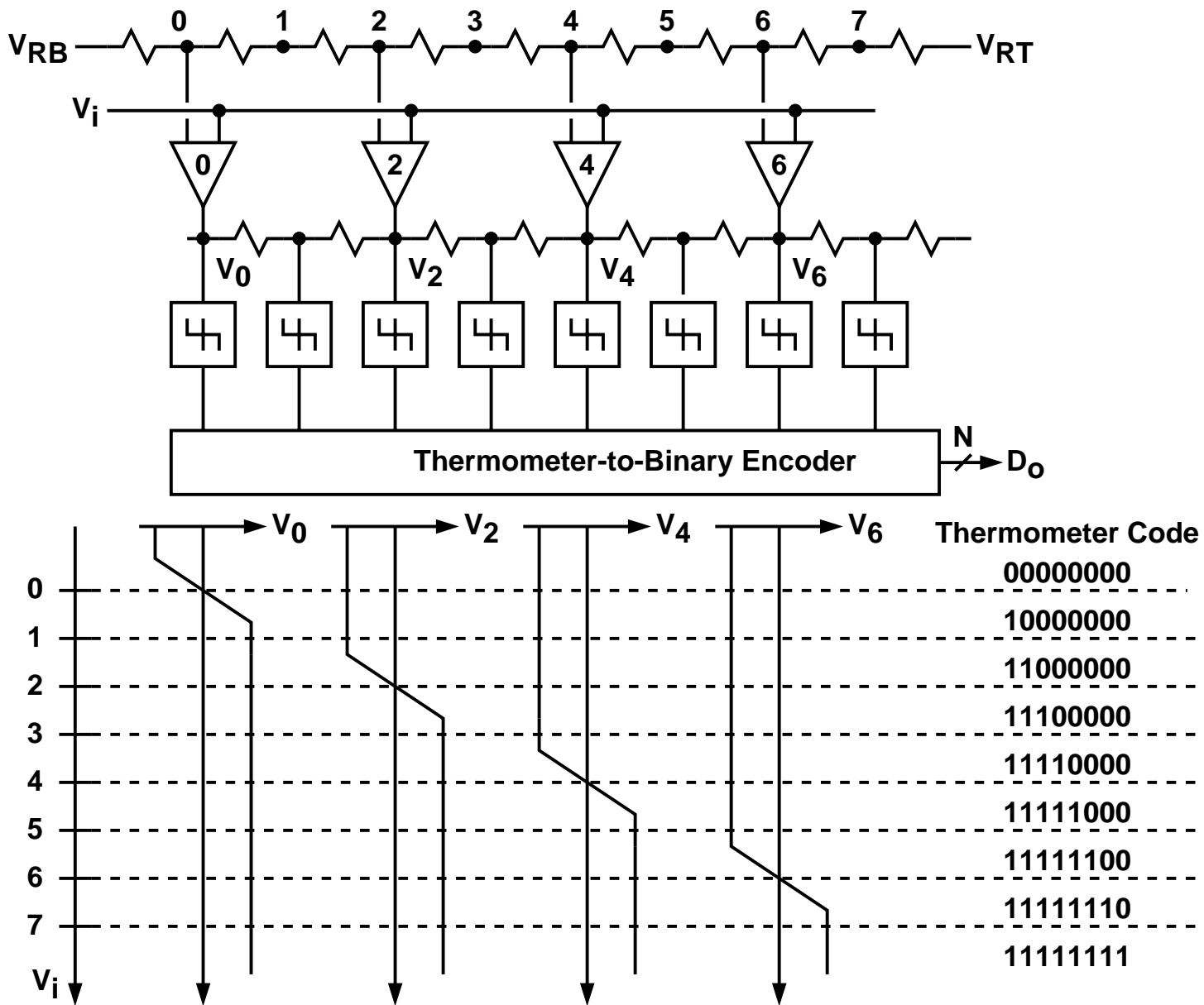
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- Two-stage quantized-feedforward differential architecture.
- The voltage ranges are  $C_{in+} - C_{in-} = [-2 \leftrightarrow +2]$  and  $F_{in+} - F_{in-} = [0 \leftrightarrow +2]$ .
- The absolute-value processing reduces the number of switches in the AMUXs by half. In addition, the settling time of the AMUX outputs is also reduced due to the reduction in output voltage swing and output capacitive loading.
- The interpolation scheme can reduce the number of “taps” from the reference ladder and reduce the number of preamplifiers. It also attenuates front-end sources of DNL, such as mismatches in the input sampling switches and resistor mismatch in the reference ladder.
- Reference: B. Brandt, et. al., “A 75-mW, 10-b 20-MSPS CMOS Subranging ADC,” JSSC 12/1999, pp. 1788–1795.

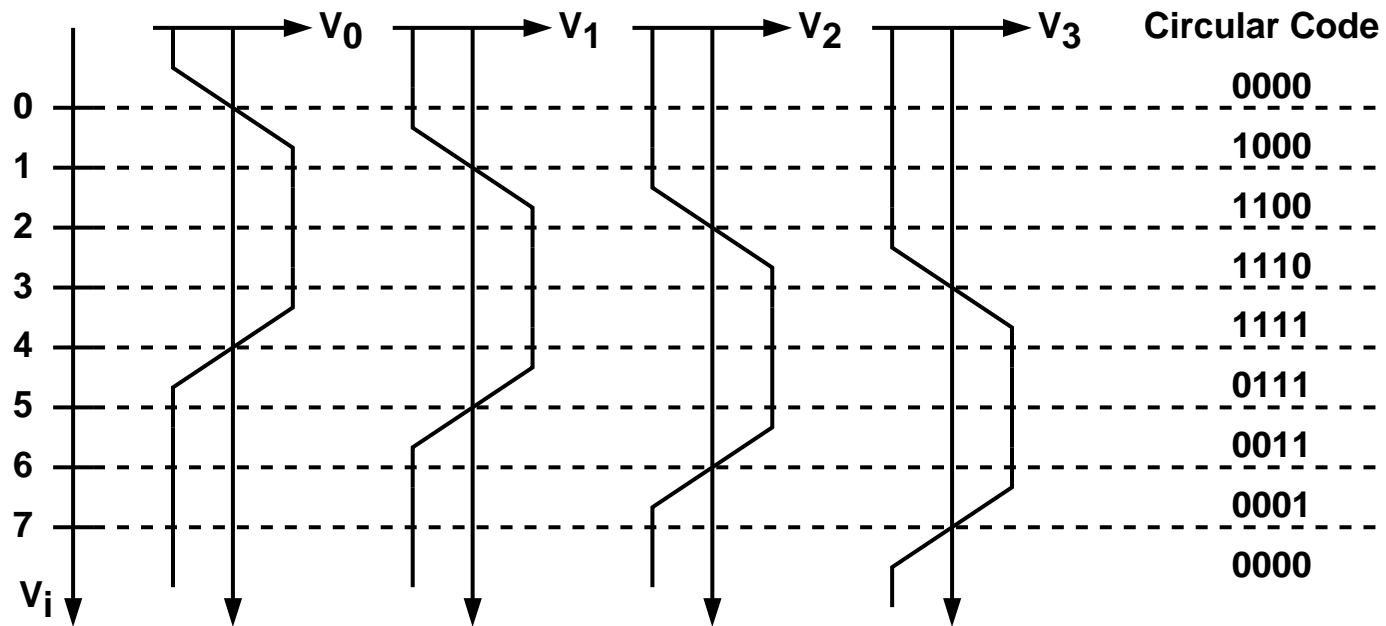
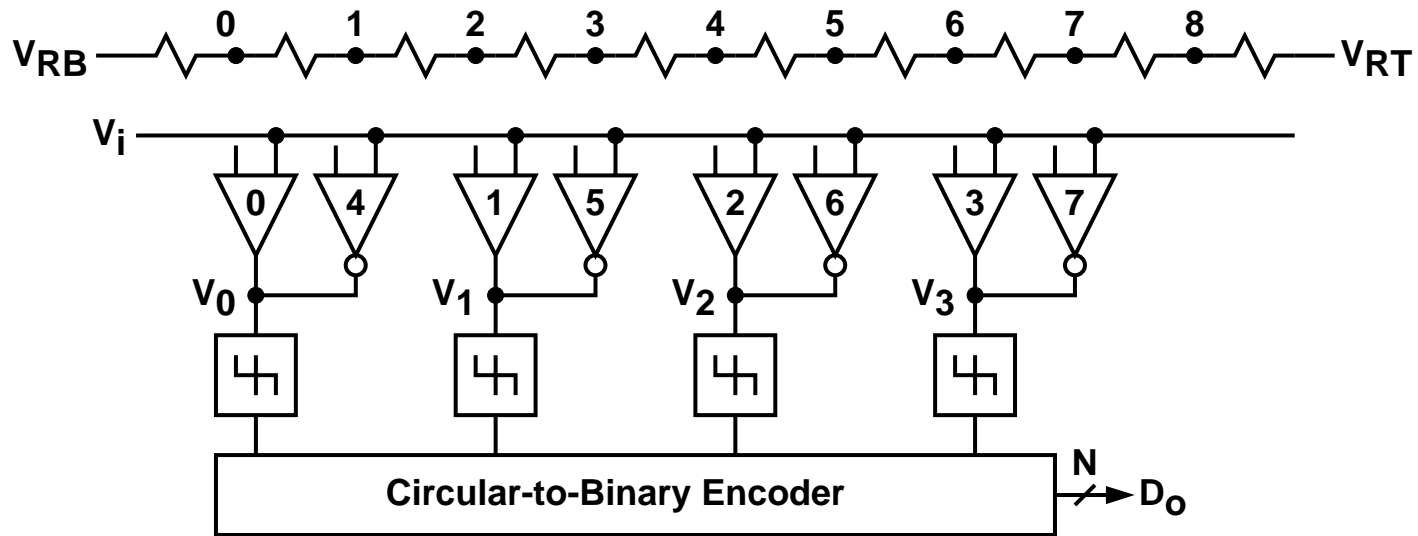
# Flash Quantization Architecture



# Resistor-String Interpolation



# Folding

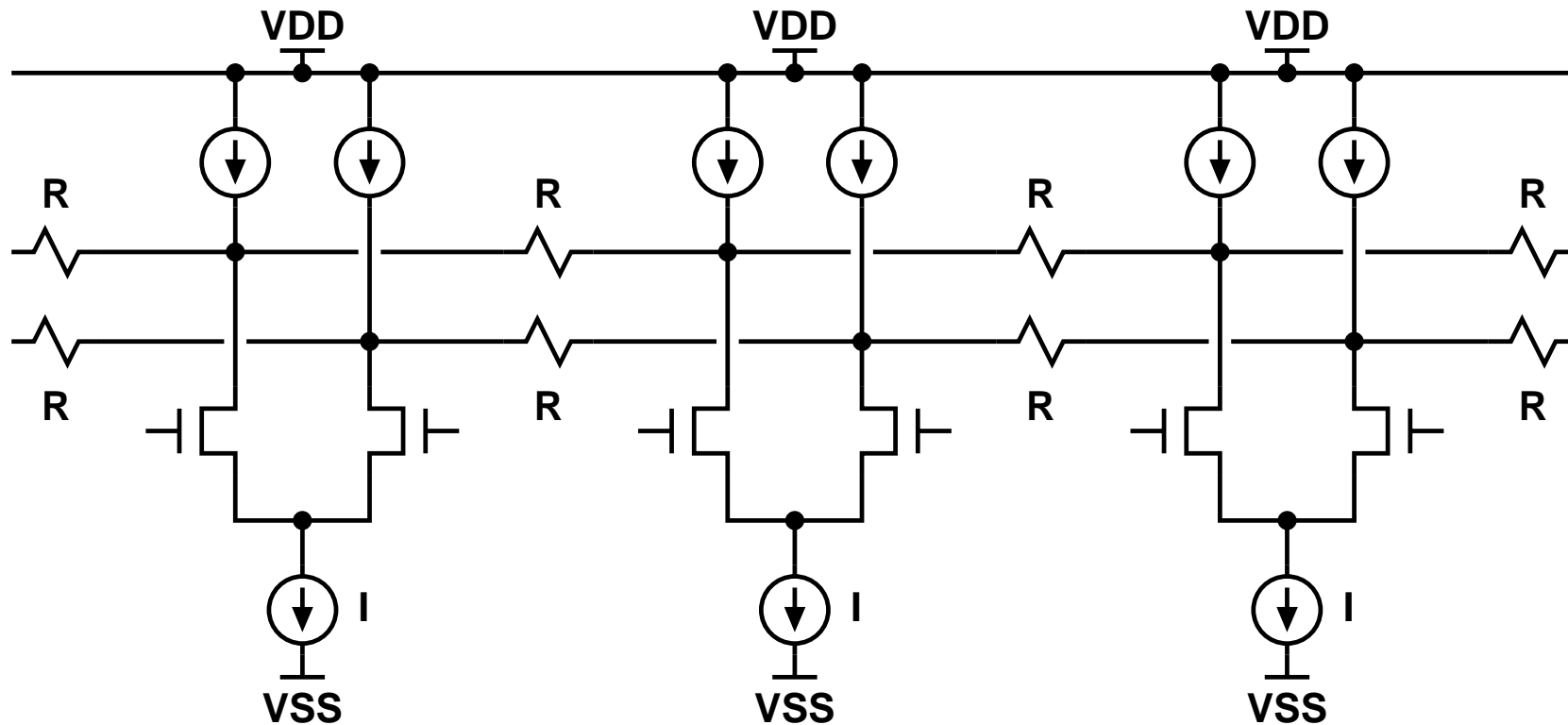


# Interpolation and Folding

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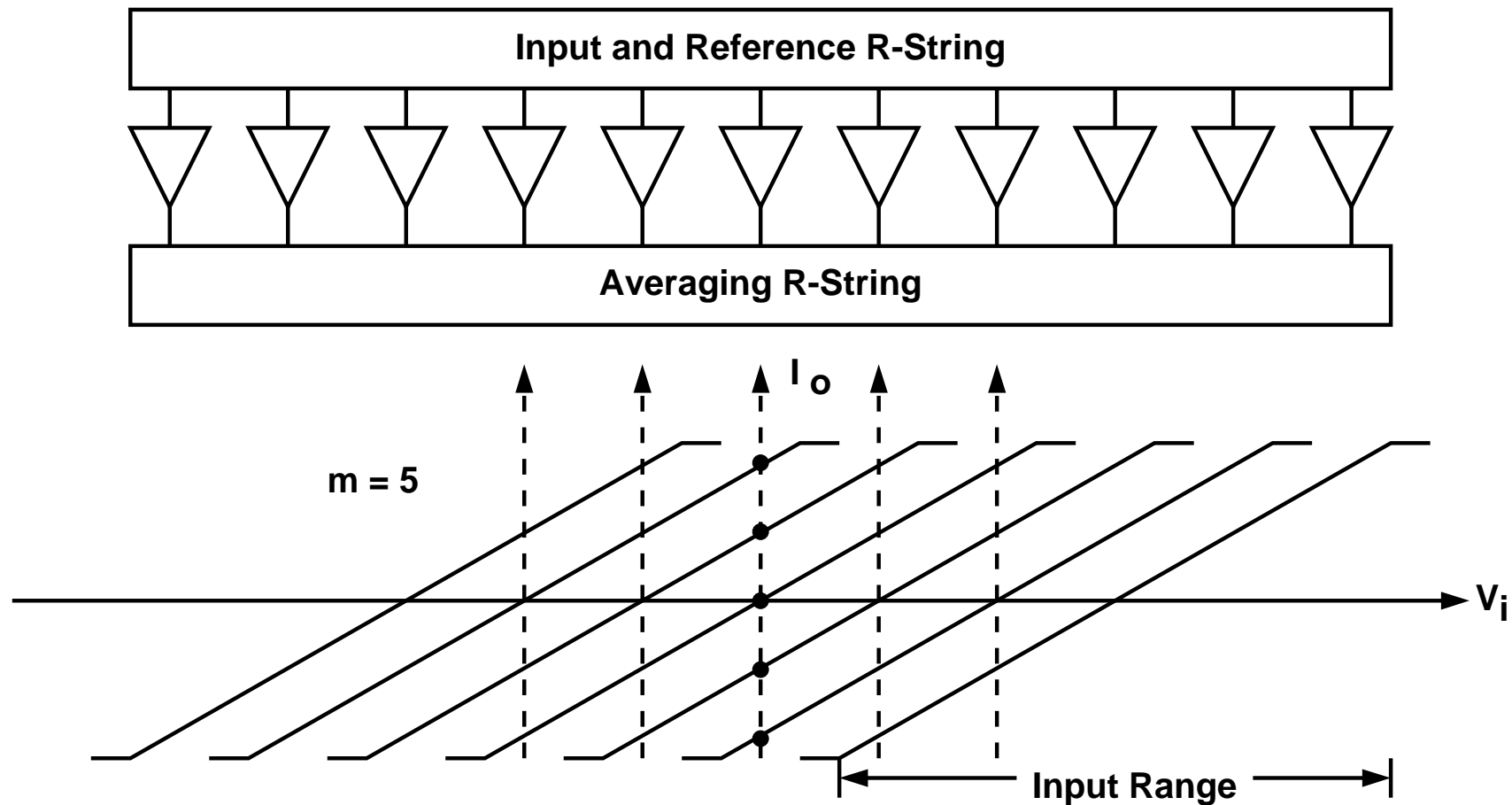
- The number of latch comparators is reduced by folding, while the number of folding blocks is reduced by interpolation.
- The interpolation can reduce the input capacitances for  $V_i$ ,  $V_{RT}$ , and  $V_{RB}$ , since the number of the preamplifiers is reduced.
- The interpolation can improve the DNL, due to the redistribution of mismatch errors.
- The interpolation technique can also be used with other types of signals, such as currents and charges.
- The folding circuit need only to be accurate near the zero-crossing points.

# Averaging Preamplifiers



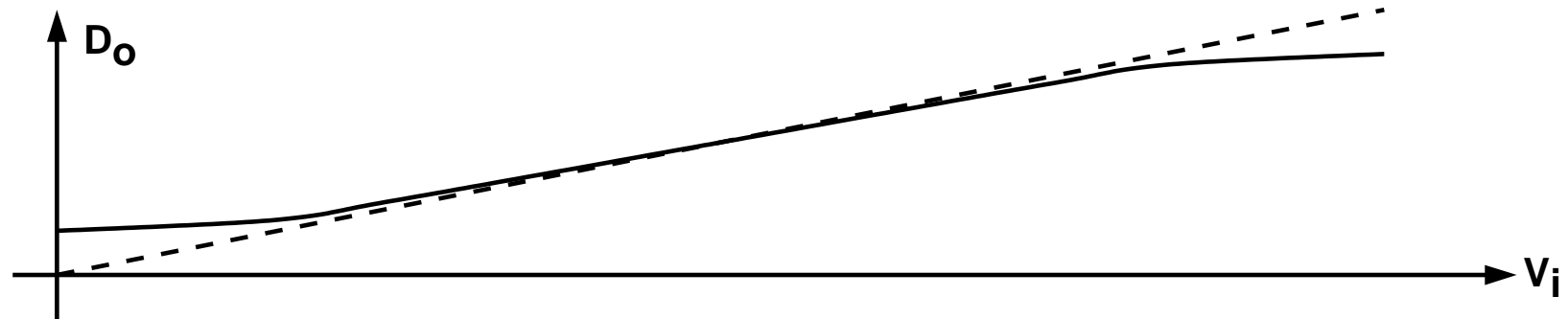
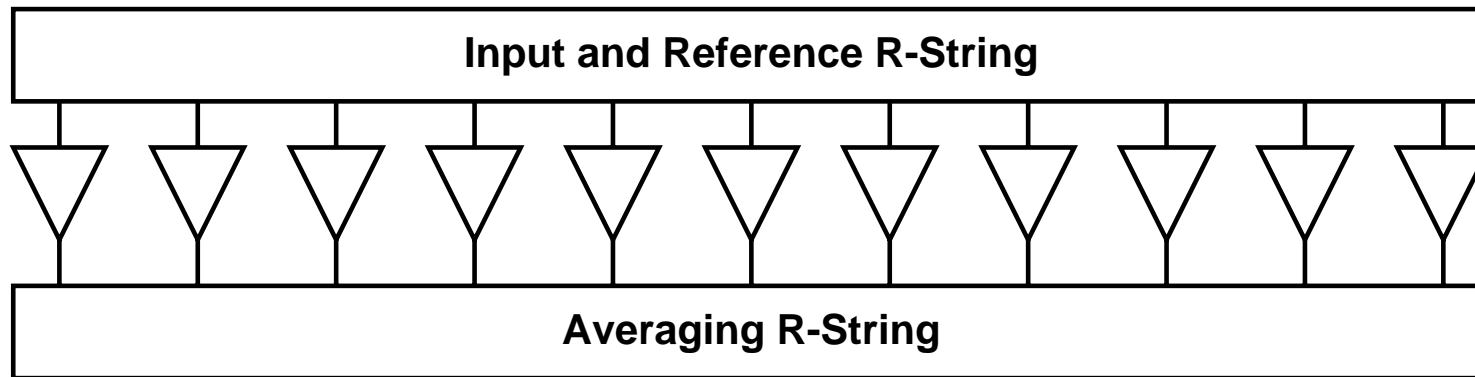
- The outputs are connected by interpolating resistor string.
- Gain is determined by  $R \times I$ .
- Speed is determined by  $R \times C$ .

# Effects of Averaging

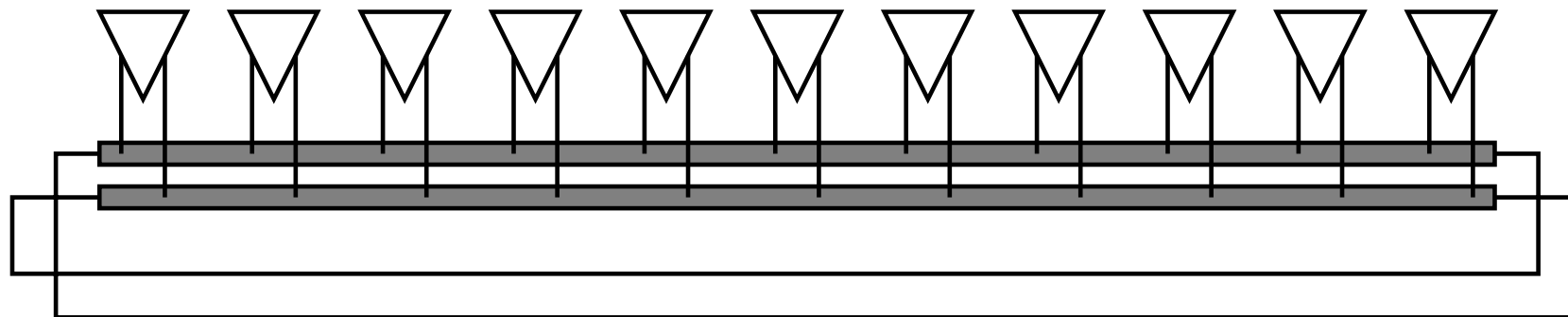


- Differential nonlinearity (DNL) improves with  $m$ .
- Integral nonlinearity (INL) improves with  $\sqrt{m}$ .

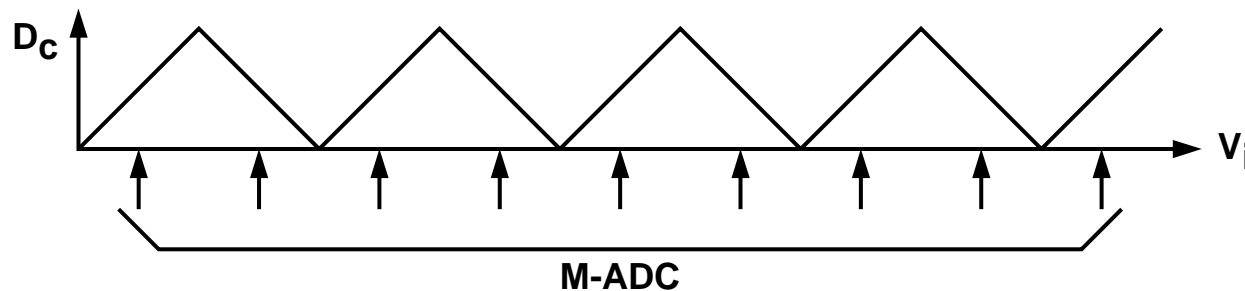
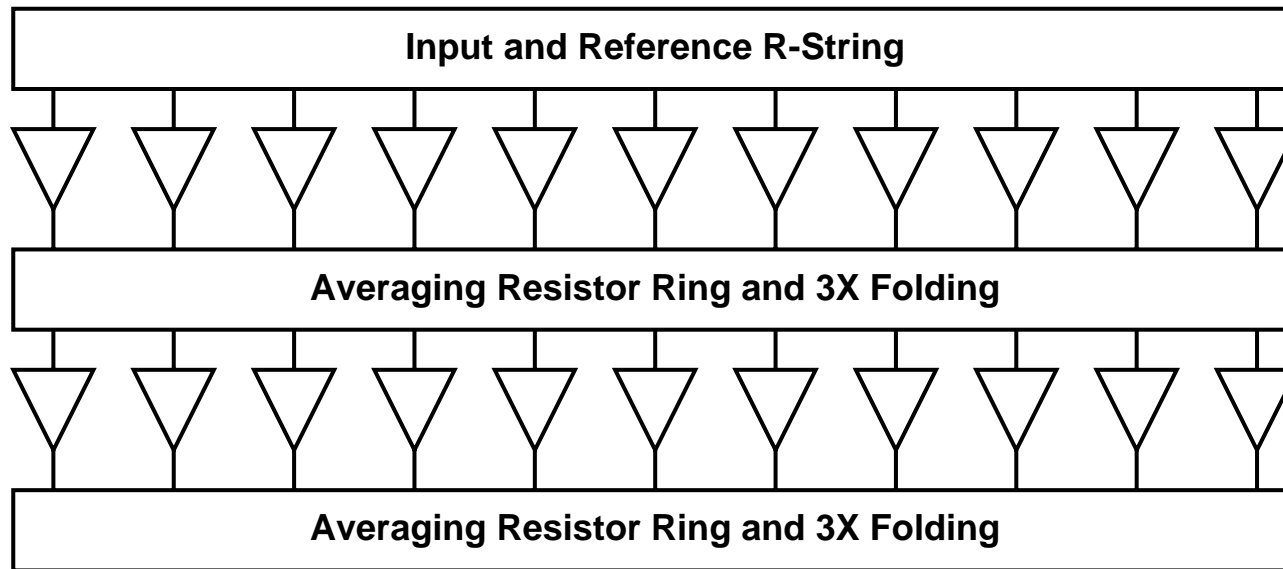
# Bending at the Edges Due to Averaging



Use Resistor-Ring to Mitigate Edge Effect

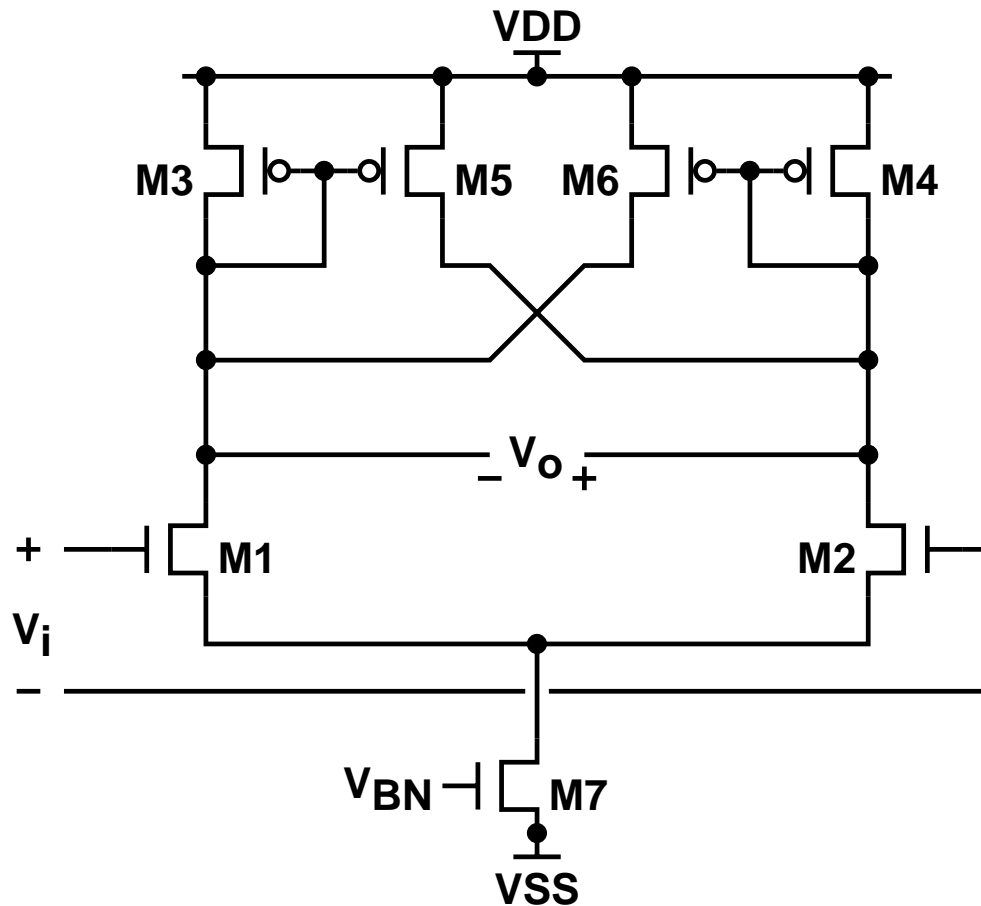


# Cascaded Folding



- Too many folding in one stage can cause gain-loss.
- Require odd number of single-stage folding to maintain continuity.

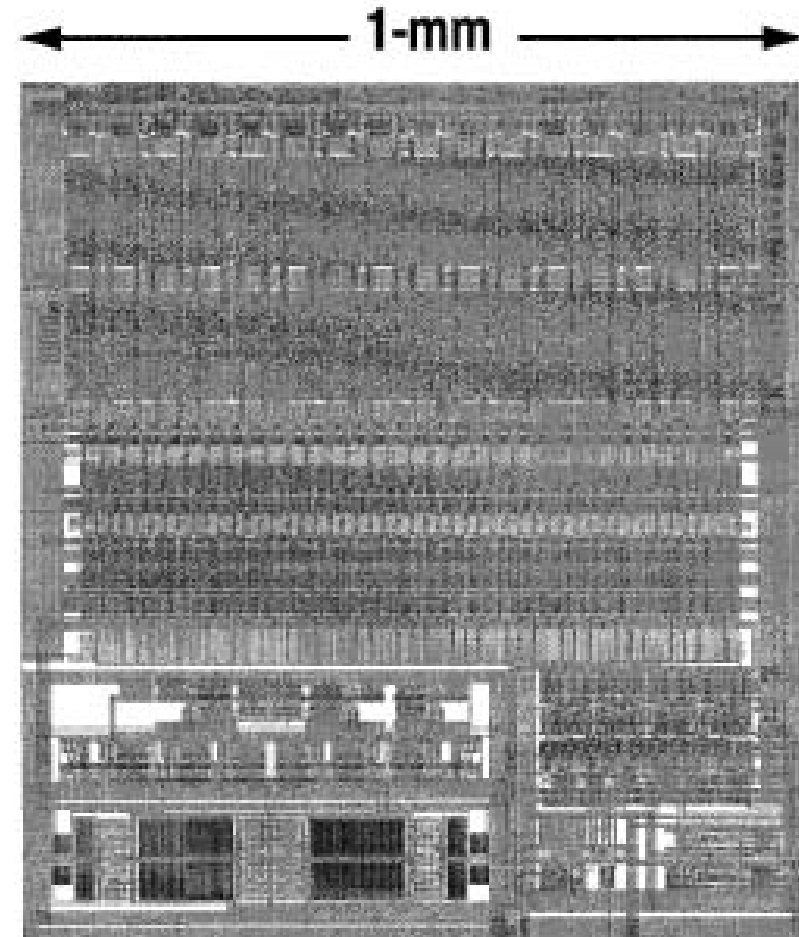
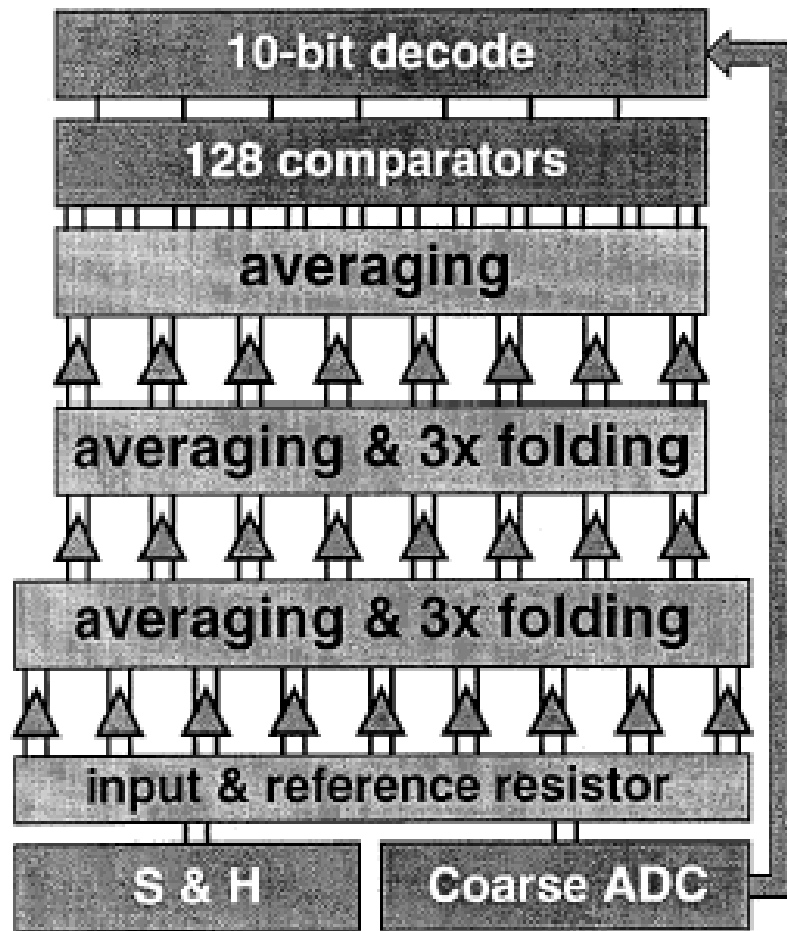
# Differential Preamplifier



$$A_{dm} = g_{m1} \cdot \frac{1}{g_{m3} - g_{m5}}$$
$$A_{cm} = \frac{g_{m1}}{1 + 2g_{m1}r_{o7}} \cdot \frac{1}{g_{m3} + g_{m5}}$$

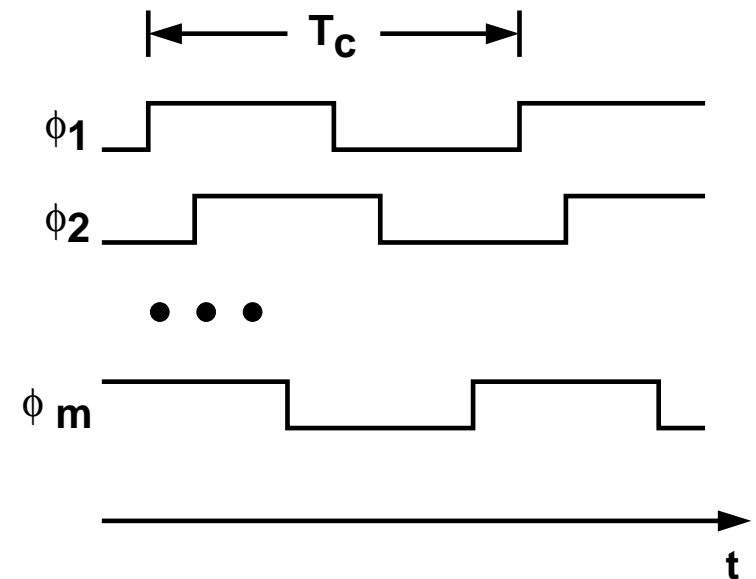
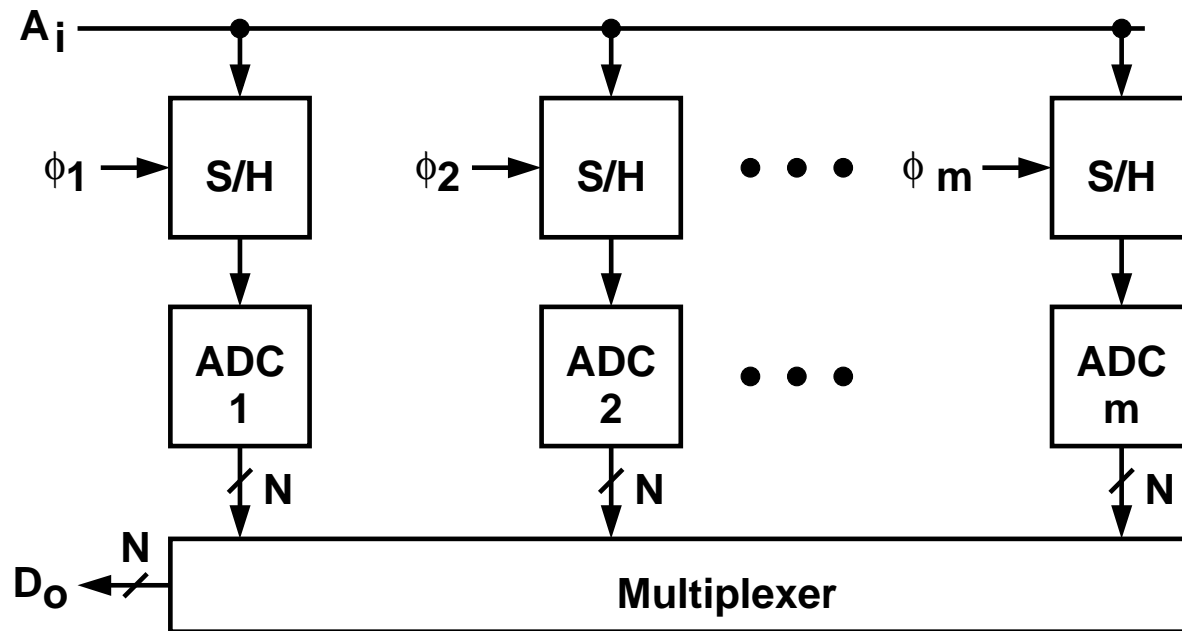
- Additional common-mode feedback is not required.

# A CMOS 10-Bit Folding ADC — Bult



- Reference: K. Bult, et. all, “An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm<sup>2</sup>,” JSSC 12/1997, pp. 1887–1895.

# Time-Interleaved Architectures

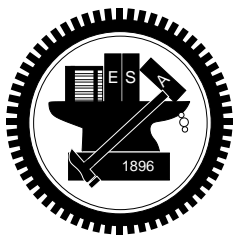


- The equivalent sampling rate is  $m/T_c$ .
- Clock phase as well as clock jitter need to satisfy  $N$ -bit accuracy.
- Any mismatch among the converter characteristics, including offset and gain, can appear as noises and/or spurious tones in  $D_o$ .

# Oversampling Converters

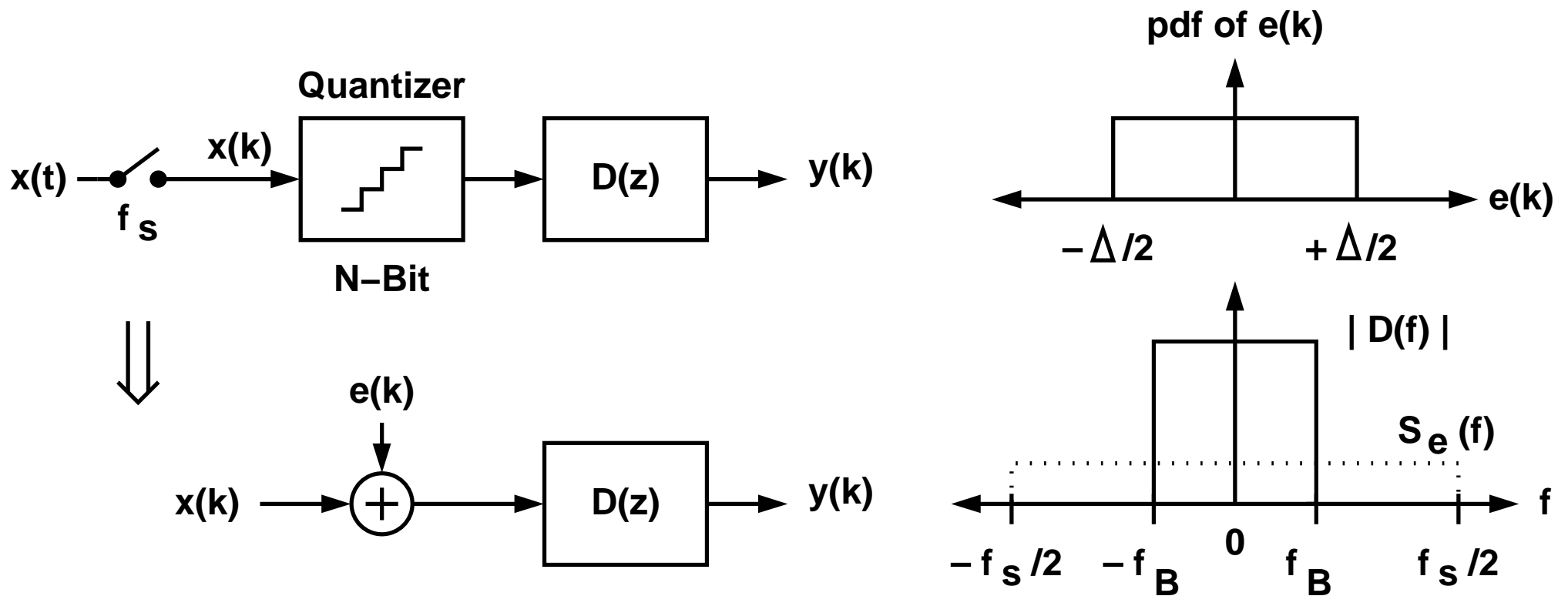
Jieh-Tsorng Wu

July 16, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Sampling and Quantization



$e(k)$  is a *quantization noise* due to the quantization process. With an ideal quantizer with step size  $\Delta$ , The pdf of  $e(k)$  is assumed to be uniformly distributed over  $-\Delta/2$  and  $+\Delta/2$ .

$$e(k) \equiv y(k) - x(k) \quad \text{Noise Power} = P_n = \int e^2 \text{pdf}(e) de = \frac{1}{12} \Delta^2$$

# Oversampling

---

Assume the noise  $e(k)$  is white and is independent of  $f_s$ , then the noise spectral density is

$$S_n(f) = \frac{P_n}{f_s} = \frac{1}{12} \Delta^2 \times \frac{1}{f_s}$$

For a full-scale sinusoidal input

$$x(k) = \frac{1}{2} A \sin(2\pi f_i \cdot kT_s) \quad A = 2^N \Delta \quad \text{Signal Power} = P_s = \frac{1}{8} \cdot A^2 = \frac{1}{8} \cdot 2^{2N} \Delta^2$$

Assume the bandwidth of  $x(k)$  is limited to  $f_B$ . The oversampling ratio, OSR, is defined as

$$\text{OSR} = \frac{f_s}{2f_B}$$

The noise at the output of  $D(z)$  filter is

$$P'_n = \int_{-f_B}^{+f_B} S_n(f) \cdot df = \frac{1}{12} \Delta^2 \times \frac{2f_B}{f_s}$$

# Oversampling

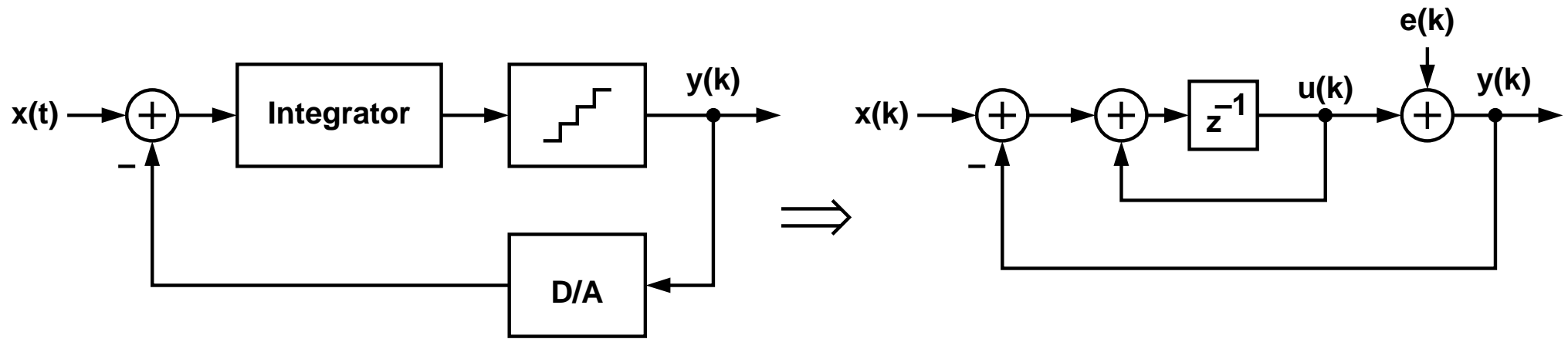
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The signal-to-noise ratio of  $y(k)$  becomes

$$\text{SNR}_{y,max} \equiv \frac{P_s}{P'_n} = \frac{3}{2} \times 2^{2N} \times \frac{f_s}{2f_B} = 1.76 + 6.02 \cdot N + 10 \log(\text{OSR}) \text{ dB}$$

- Oversampling gives a SNR improvement of 3 dB/octave or 0.5 bit/octave.
- High-speed digital filters,  $D(z)$ , are required.
- Oversampling also eases the anti-alias filter design for  $x(t)$ .
- Oversampling does not improve linearity. Linear quantizers are still required.
- One-bit quantizers and one-bit DACs are inherently linear. Therefore, they are often used in oversampling converters.

# First-Order $\Delta\Sigma$ Modulator



$$\text{Signal Transfer Function} = S_{TF}(z) = \frac{Y(z)}{X(z)} = z^{-1}$$

$$\text{Noise Transfer Function} = N_{TF}(z) = \frac{Y(z)}{E(z)} = 1 - z^{-1}$$

The noise transfer function in frequency domain is

$$N_{TF}(f) = N_{TF}(z)|_{z=e^{j2\pi f/f_s}} = \sin\left(\frac{\pi f}{f_s}\right) \times 2j \times e^{-j\pi f/f_s}$$

- Noise power is small near  $f = 0$  and becomes large near  $f = f_s/2$ .

# First-Order $\Delta\Sigma$ Modulator

---

The quantization noise power in the  $f_B$  frequency band is

$$P'_n = \int_{-f_B}^{+f_B} S_e(f) |N_{TF}(f)|^2 df = \int_{-f_B}^{+f_B} \frac{\Delta^2}{12} \frac{1}{f_s} \left[ 2 \sin \left( \frac{\pi f}{f_s} \right) \right]^2 \cdot df$$

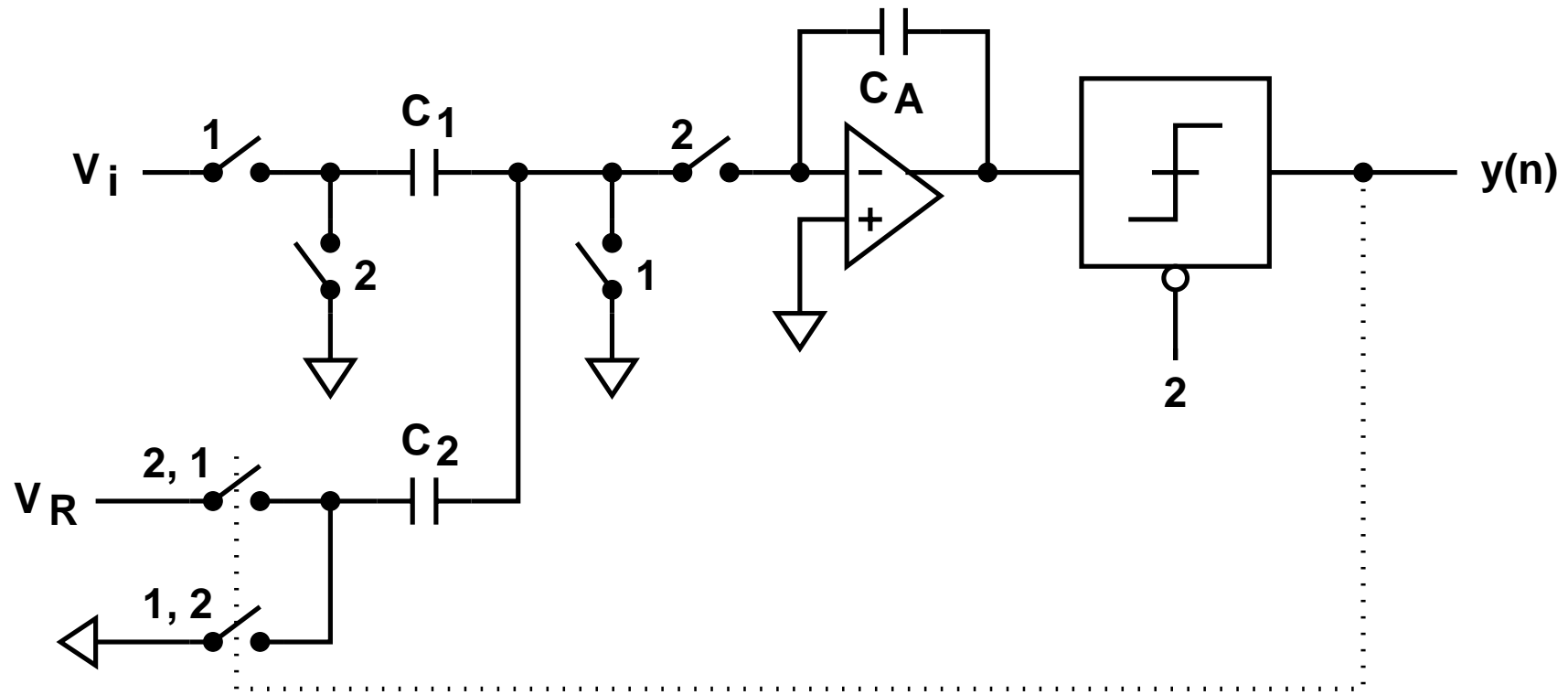
If  $\text{OSR} \gg 1$ , then

$$P'_n \approx \frac{\Delta^2}{12} \cdot \frac{\pi^2}{3} \left( \frac{2f_B}{f_s} \right)^3 = \frac{\Delta^2 \pi^2}{36} \frac{1}{\text{OSR}^3}$$

$$\text{SNR}_{y,max} \equiv \frac{P_s}{P'_n} = \frac{9}{2\pi^2} \times 2^{2N} \times \text{OSR}^3 = -3.41 + 6.02 \cdot N + 30 \log(\text{OSR}) \text{ dB}$$

- Oversampling gives a SNR improvement of 9 dB/octave or 1.5 bit/octave.
- The integrator's output is  $u(k+1) = x(k) - e(k)$ . If  $x$  is a dc input and bounded by the full range of D/A, then  $|e| < \Delta/2$  and  $|u|_{max} = |x| + \Delta/2$ .

# First-Order $\Delta\Sigma$ Modulator with SC Circuit Implementation



- One-bit  $\Delta\Sigma$  modulator.  $V_R = \Delta/2$ .
- The comparator latches on the falling edge of  $\phi_2$ . The output  $y(n) \in \{+1, -1\}$ .
- $C_1$  and  $C_2$  can be combined into one capacitor.

## Circuit Considerations

---

For an ideal integrator  $H(z)$ , we have

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad S_{TF}(z) = \frac{H(z)}{1 + H(z)} = z^{-1} \quad N_{TF}(z) = \frac{1}{1 + H(z)} = 1 - z^{-1}$$

- If the integrator includes a gain factor  $G$ , then

$$H(z) = G \times \frac{z^{-1}}{1 - z^{-1}} \quad S_{TF}(z) = \frac{Gz^{-1}}{1 - (1 - G)z^{-1}} \quad N_{TF}(z) = \frac{1 - z^{-1}}{1 - (1 - G)z^{-1}}$$

- Small deviations of  $G$  from unity have little effect on the overall performance, provided the net gain in the feedback loop is large.
- 10% gain accuracy of  $G$  is tolerable.

# Circuit Considerations

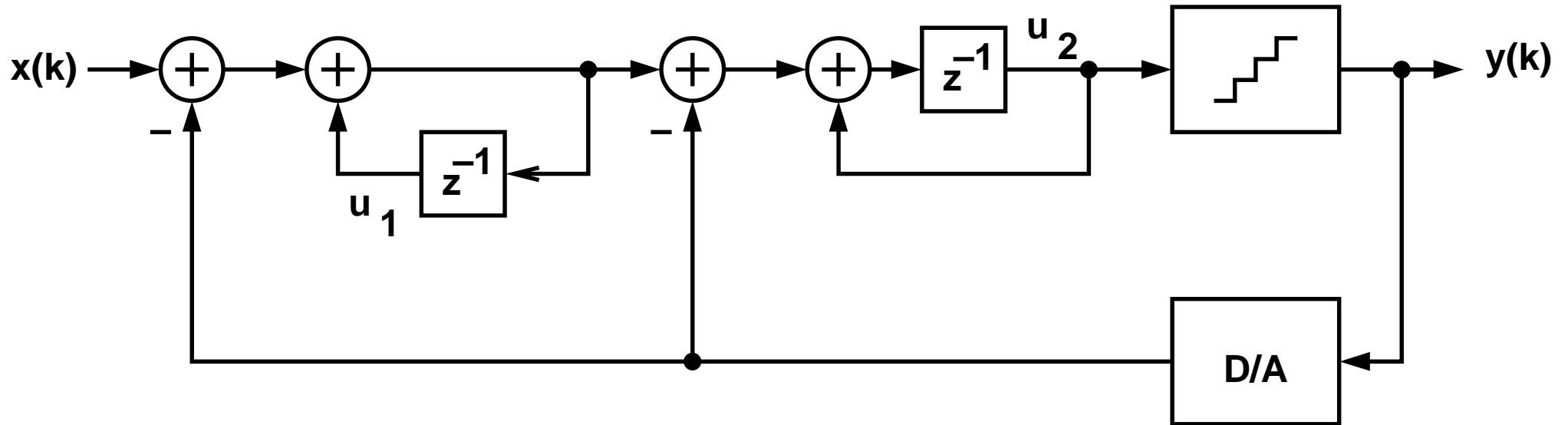
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- If the opamp has a finite gain of  $A_o$ , then

$$H(z) \approx \frac{z^{-1}}{1 - \beta z^{-1}} \quad \text{where} \quad \beta = 1 - \frac{1}{A_o}$$
$$S_{TF}(z) = \frac{z^{-1}}{1 + (1 - \beta)z^{-1}} \quad N_{TF}(z) = \frac{1 - \beta z^{-1}}{1 + (1 - \beta)z^{-1}}$$

- $N_{TF}(f)$  is flat for  $2\pi f / f_s < 1/A_o$ .
  - Want  $f_B \gg f_s / (2\pi A_o)$  or  $A_o \gg \text{OSR} / \pi$ .
  - Usually want  $A_o > 2\text{OSR}$ .
- Noises or harmonics arising from the quantizer's nonlinearity are suppressed by  $N_{TF}(z)$ , making the quantizer less critical.
  - The linearity of the D/A is very important.

## Second-Order $\Delta\Sigma$ Modulator



The transfer functions are

$$S_{TF}(z) = \frac{Y(z)}{X(z)} = z^{-1}$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = (1 - z^{-1})^2$$

The noise transfer function in frequency domain is

$$|N_{TF}(f)| = \left[ 2 \sin \left( \frac{\pi f}{f_s} \right) \right]^2$$

## Second-Order $\Delta\Sigma$ Modulator

---

If  $\text{OSR} \gg 1$ , the quantization noise power is

$$P'_n \approx \frac{\Delta^2 \pi^4}{60} \frac{1}{\text{OSR}^5}$$

And

$$\text{SNR}_{y,max} = \frac{15}{2\pi^4} \times 2^{2N} \times \text{OSR}^5 = -11.14 + 6.02 \cdot N + 50 \log(\text{OSR}) \text{ dB}$$

- Oversampling gives a SNR improvement of 15 dB/octave or 2.5 bit/octave.

# Integration Range in a Second-Order $\Delta\Sigma$ Modulator

---

The outputs of the integrators are

$$u_1(k+1) = x(k) - e(k) + e(k-1) \quad u_2(k+1) = x(k-1) - 2e(k-1) + e(k-2)$$

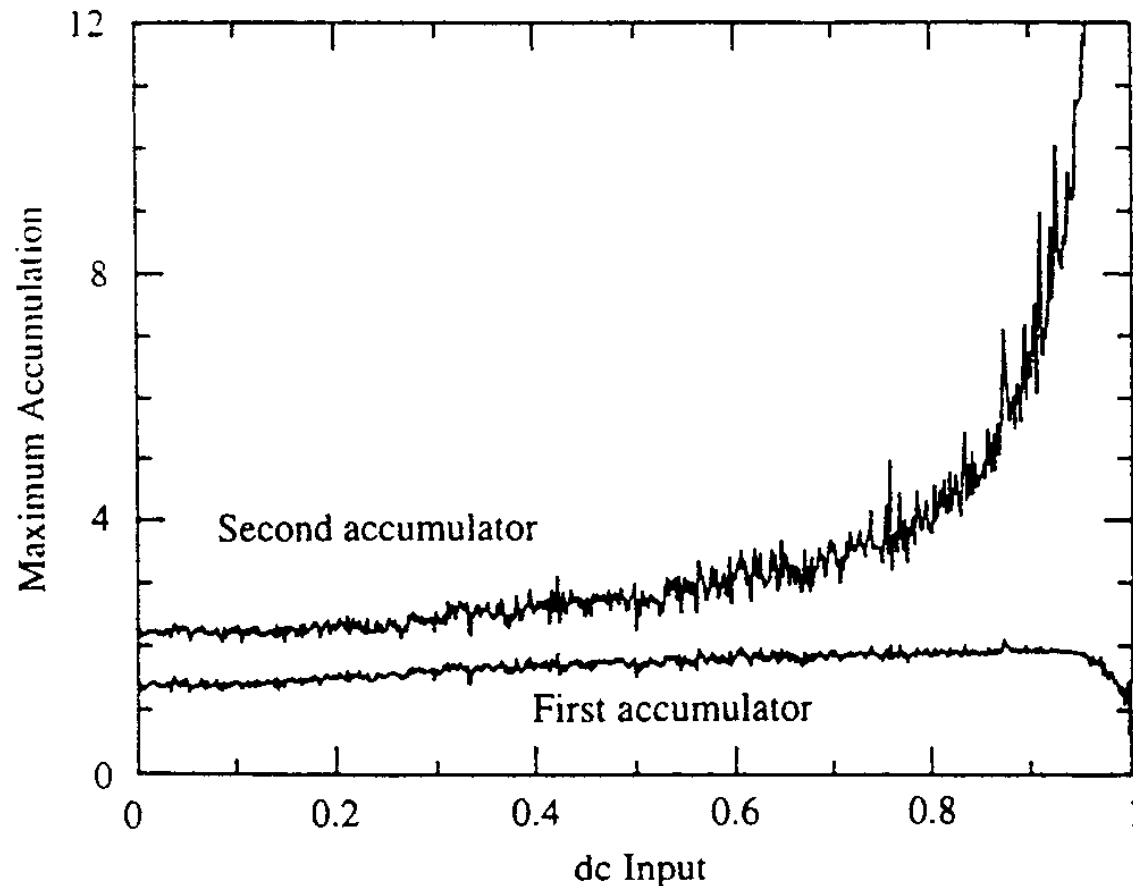
For multi-bit quantization:

- For small  $|x|$ ,  $e$  is bounded by  $\pm\Delta/2$ .
- If  $|e| < \Delta/2$ , then

$$|u_1| \leq |x(k)| + |e(k)| + |e(k-1)| \leq |x| + \Delta$$

$$|u_2| \leq |x(k)| + 2|e(k-1)| + |e(k-2)| \leq |x| + \frac{3}{2}\Delta$$

# Integration Range in a Second-Order $\Delta\Sigma$ Modulator



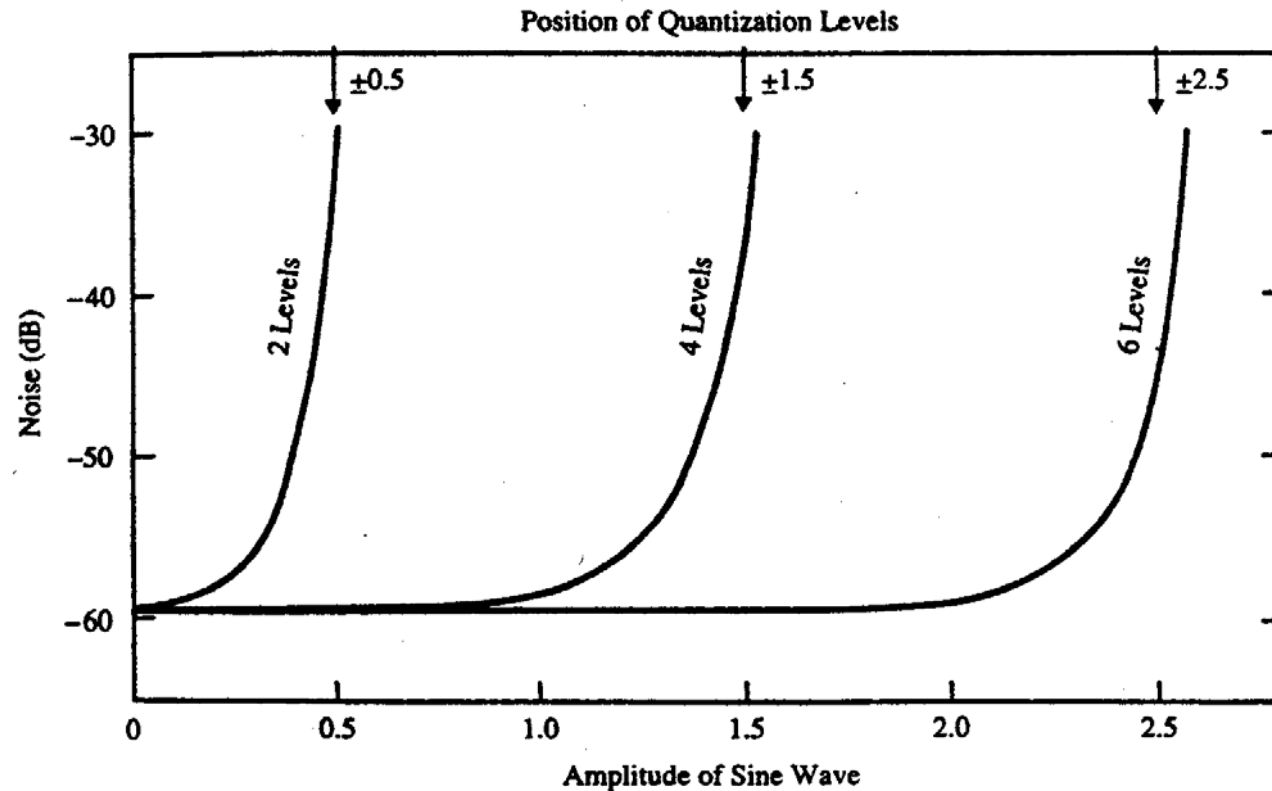
- One-bit quantization.
- D/A output levels are  $\pm 1$ .
- The integrators are bounded by

$$|u_1|_{max} = |x| + 2$$

$$|u_2|_{max} = \frac{(5 - |x|)^2}{8(1 - |x|)}$$

- In practice, the first accumulation is often clipped at  $\pm 2$ , and the second effectively  $\pm 4$ .

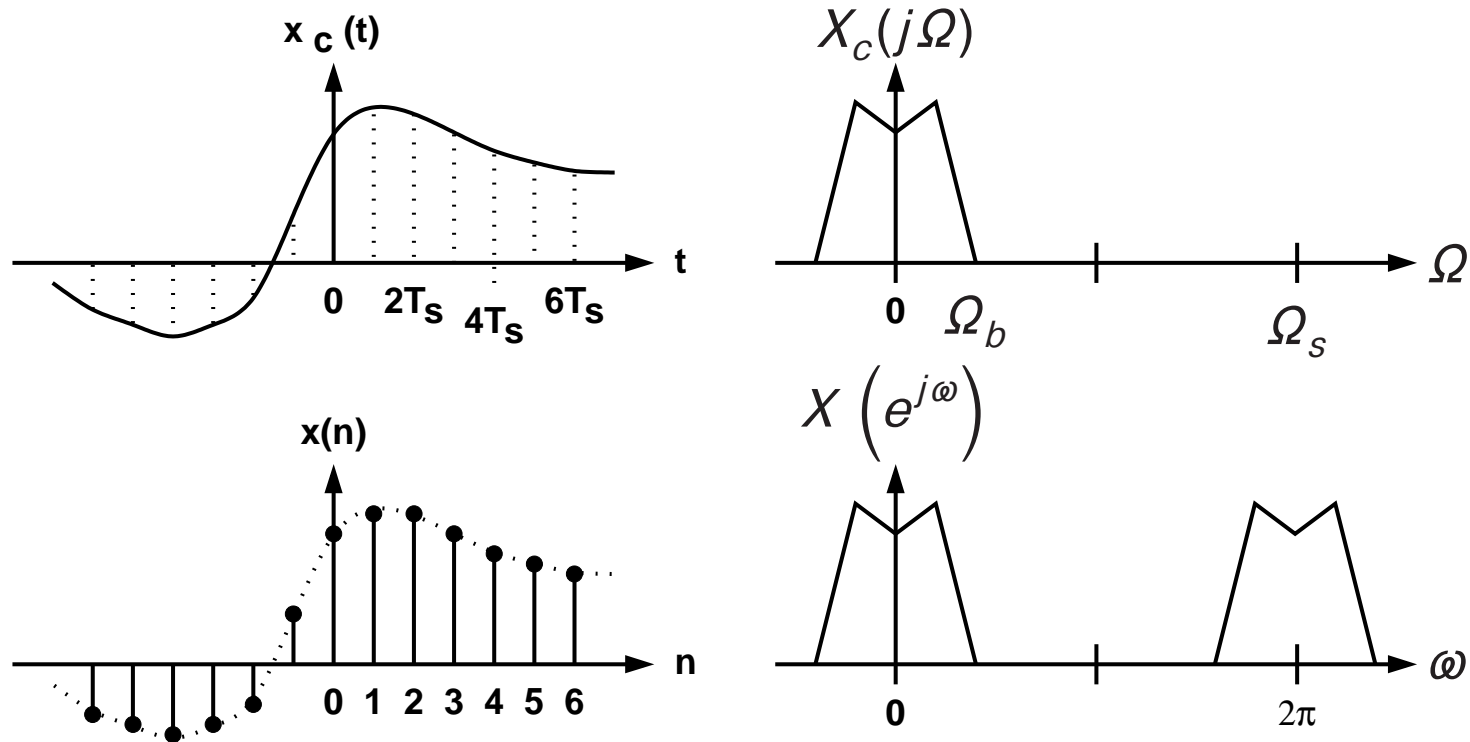
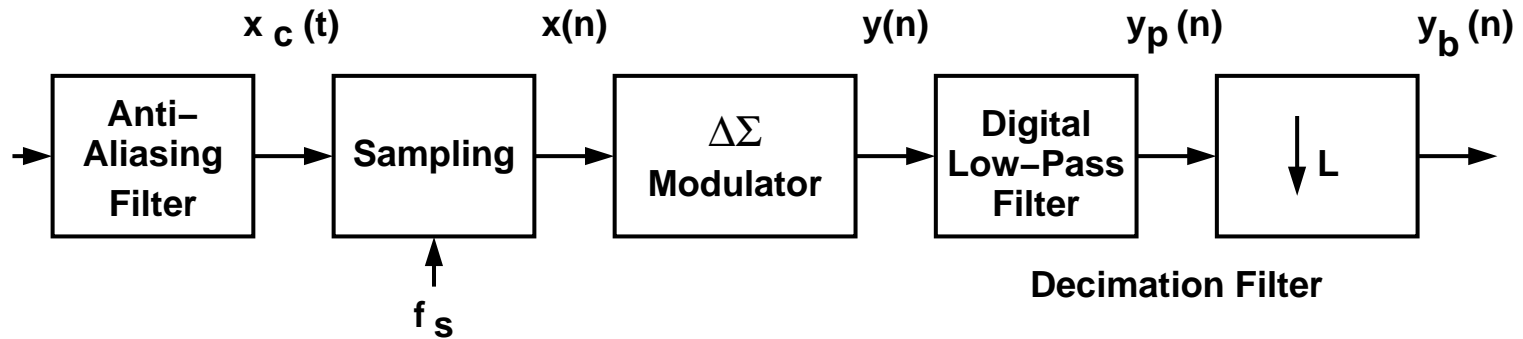
# Overloading in a Second-Order $\Delta\Sigma$ Modulator



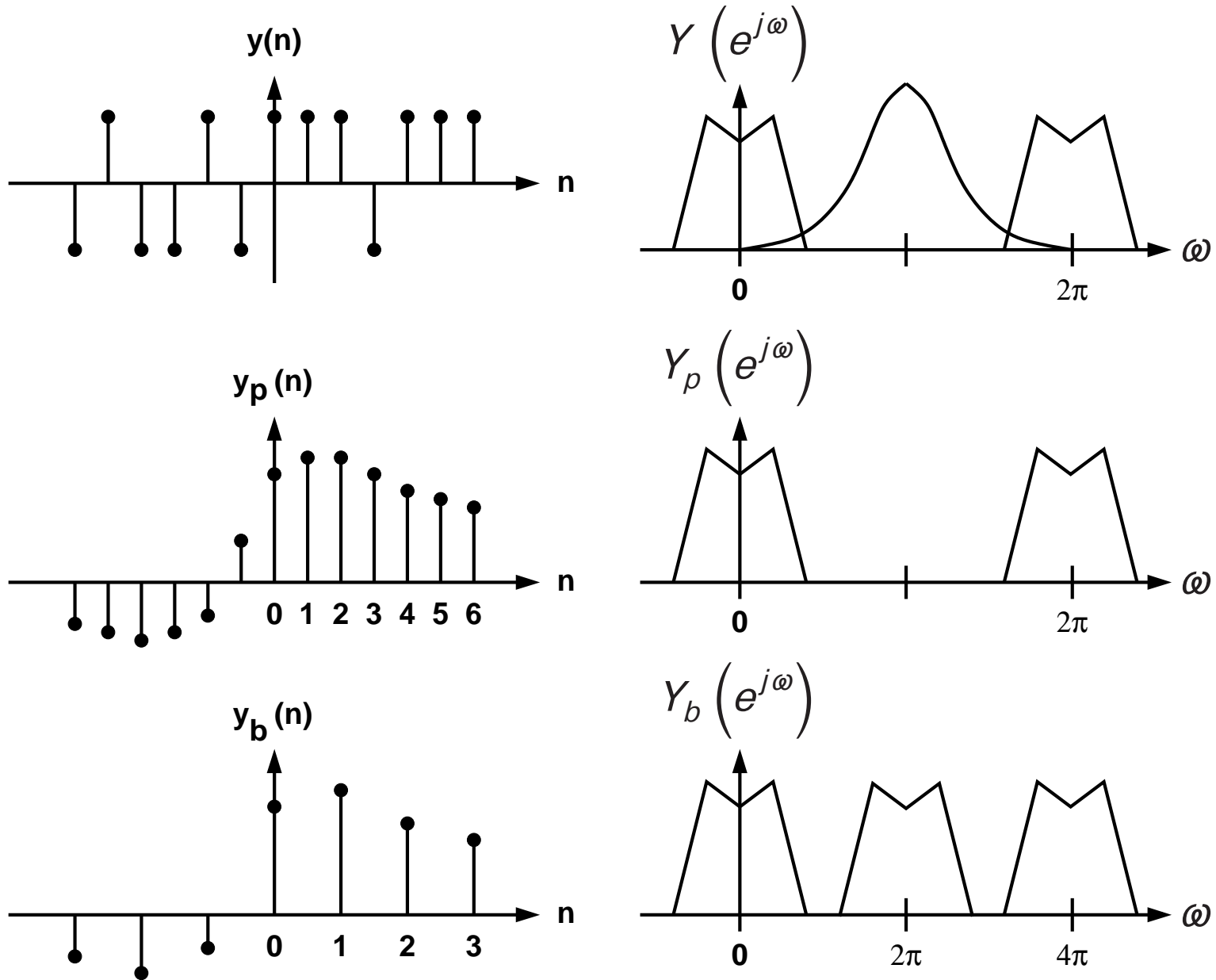
- D/A levels are  $\pm 0.5$ ,  $\pm 1.5$ , and  $\pm 2.5$ .
- $\Delta$  is the same for all three cases.

- For large  $x$ , the input to the quantizer can be so large that  $|e| > \Delta/2$ . The excess noise can degrade the SNR of  $y$ .
- In the two-level case (1-bit quantization), the comparator is theoretically overloaded for all conditions, except zero input with zero initial conditions.

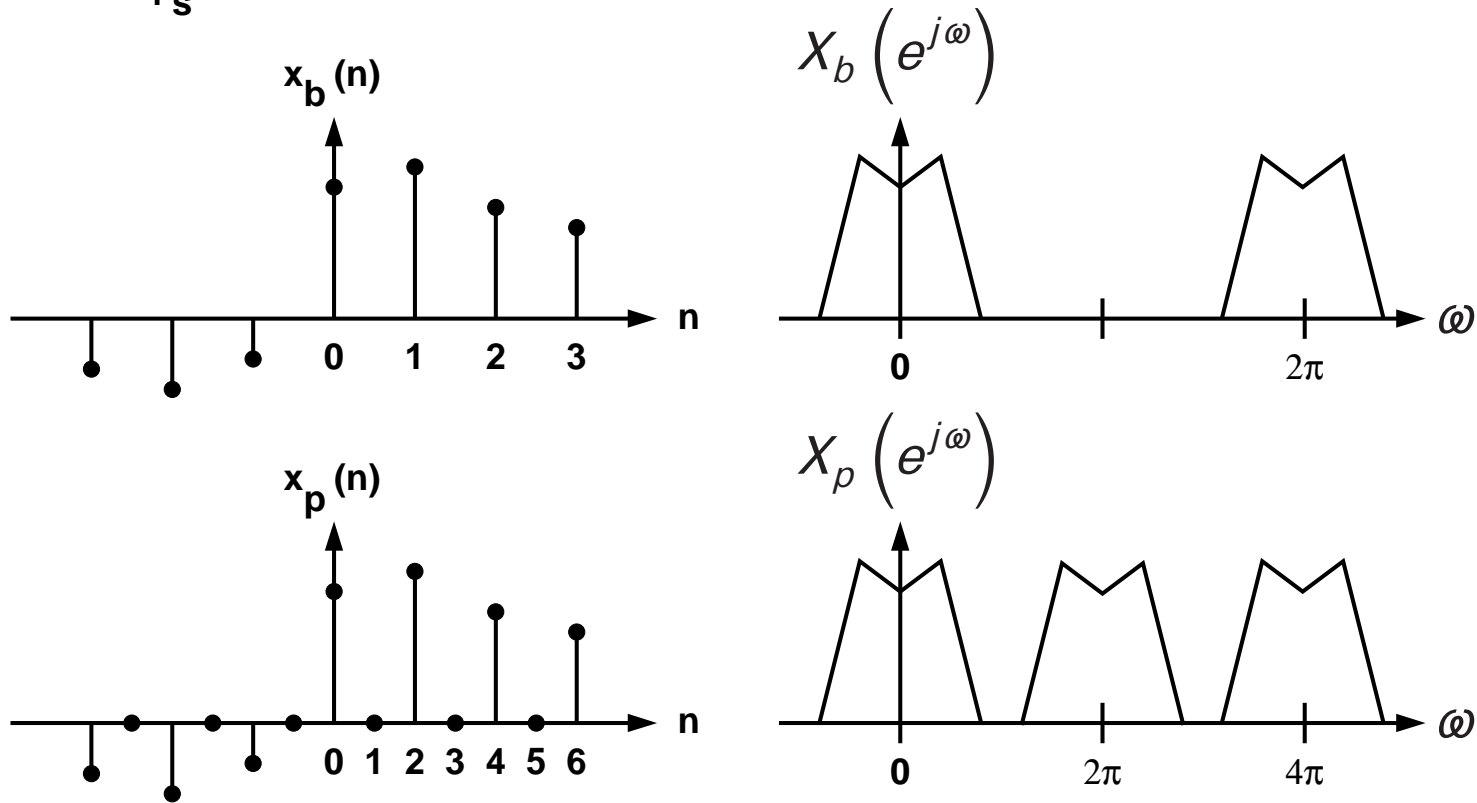
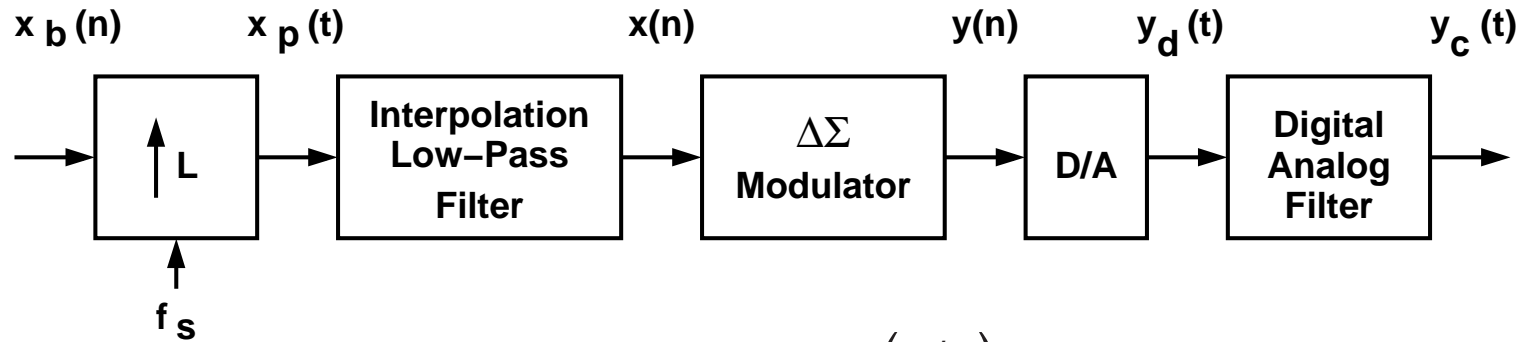
# Oversampling ADCs



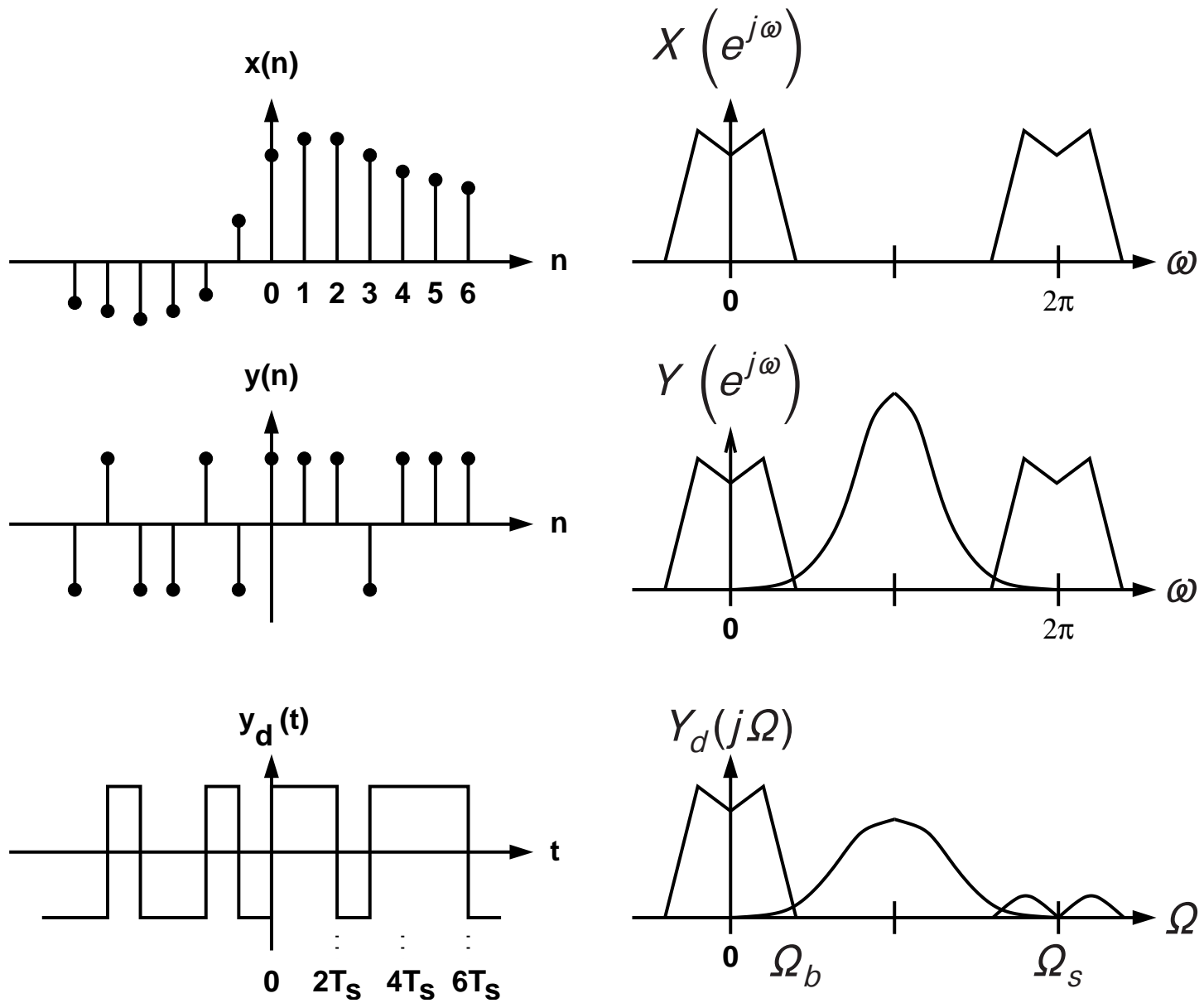
# Oversampling ADCs



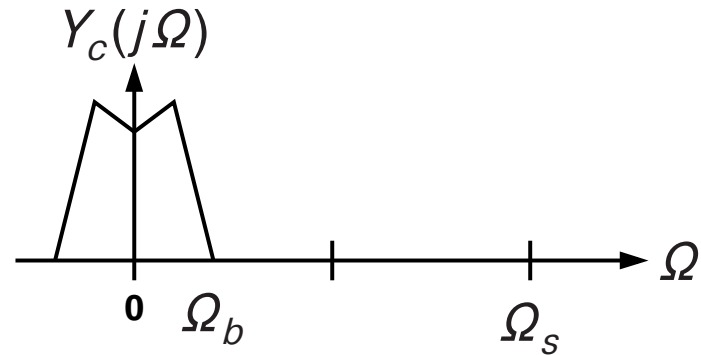
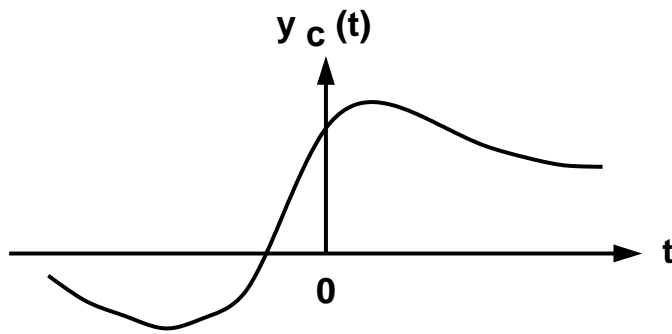
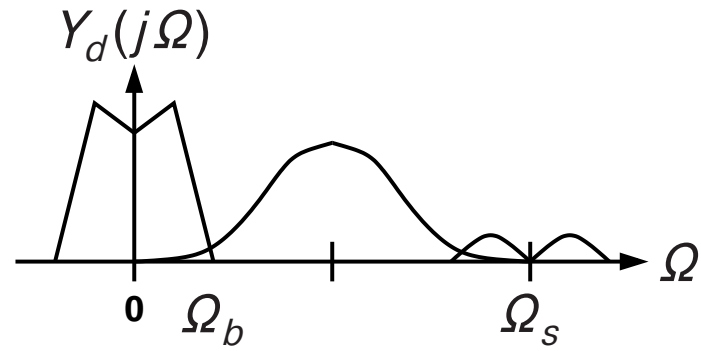
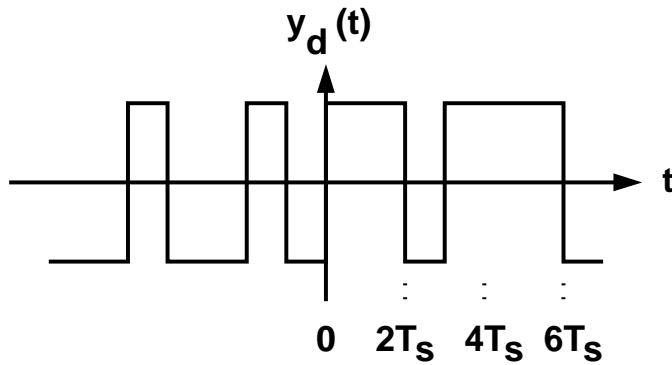
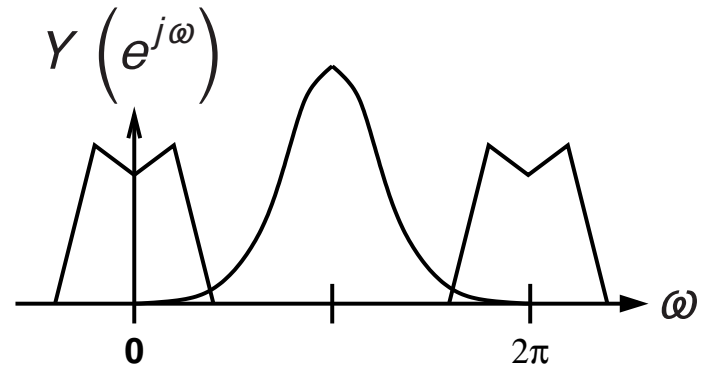
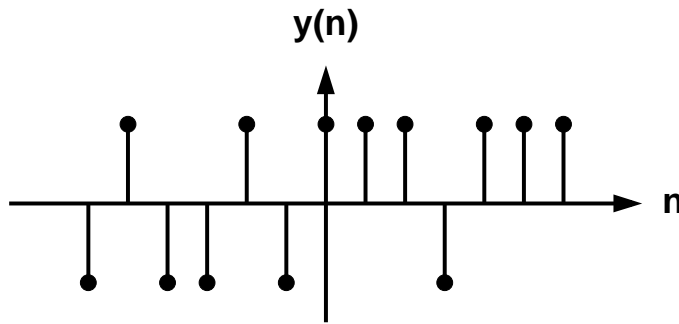
# Oversampling DACs



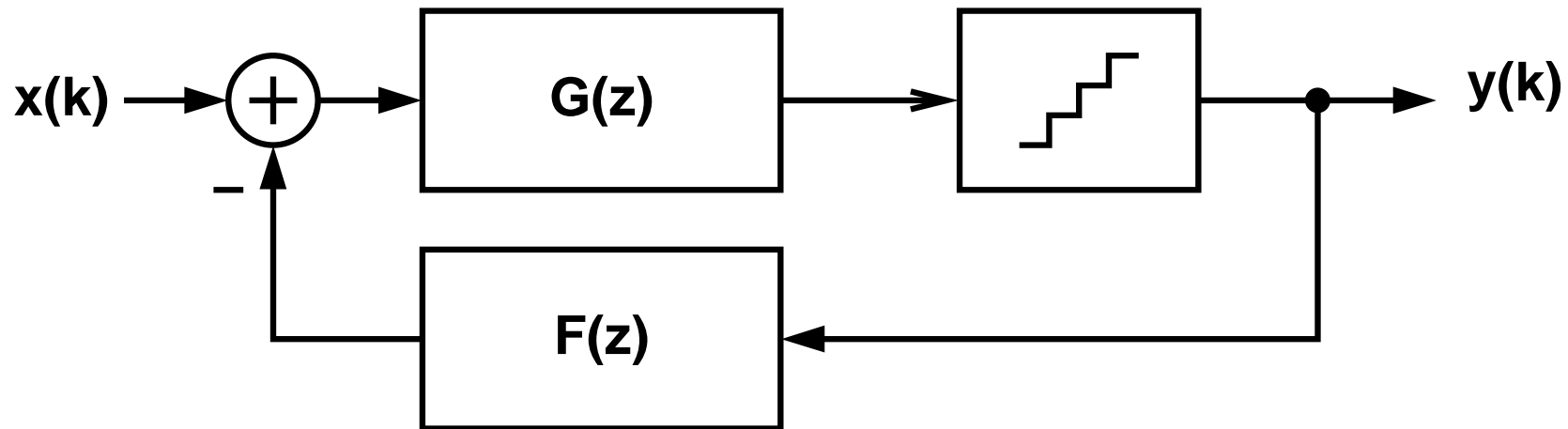
# Oversampling DACs



# Oversampling DACs



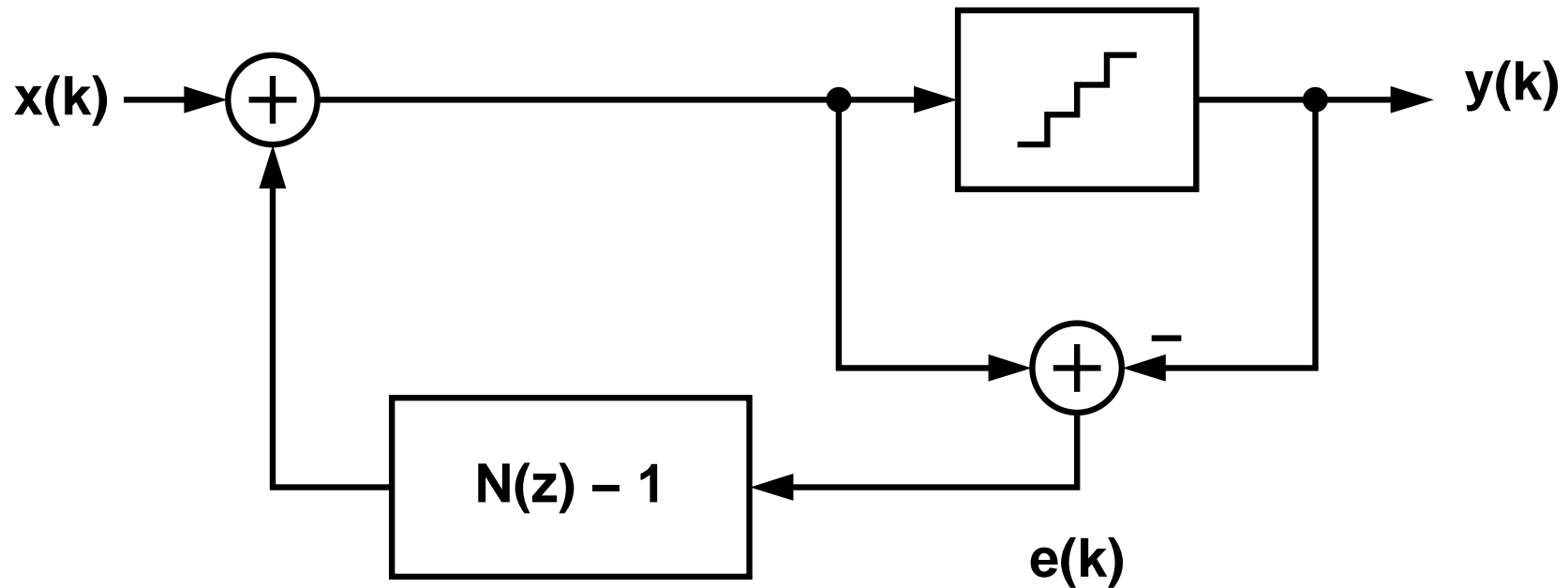
# General Single-Stage $\Delta\Sigma$ Modulator



$$Y(z) = \frac{G(z)}{1 + F(z)G(z)} \cdot X(z) + \frac{1}{1 + F(z)G(z)} \cdot E(z) = S_{TF}(z) \cdot X(z) + N_{TF}(z) \cdot E(z)$$

- OSR is typically between 16 and 256.
- The loop gain,  $L(z) = F(z)G(z)$ , need to be high in the band of interest.
- The poles  $L(z)$  are the zeros of  $N_{TF}(z)$ .
- Both  $S_{TF}(z)$  and  $N_{TF}(z)$  generally share the same poles, the roots of  $1 + L(z) = 0$ .

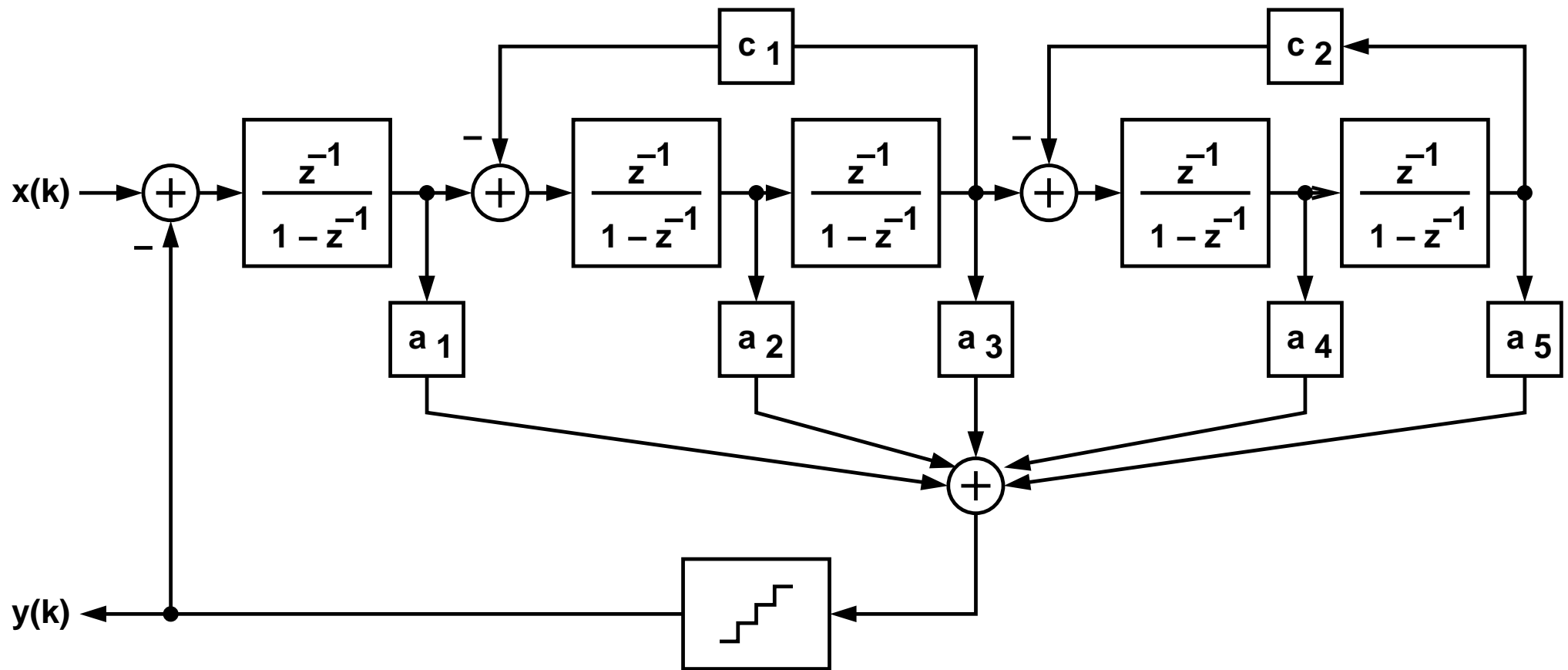
# General Single-Stage Error-Feedback Coder



$$Y(z) = X(z) + N(z) \cdot E(z)$$

- A slight coefficient error can degrade noise-shaping significantly.
- Not suitable for analog modulators, only appropriate for digital modulators.

# Single-Stage High-Order Modulators



- An  $N$ th-order noise-shaping modulator improves the SNR by  $(6N + 3)$  dB/octave, or equivalently,  $(N + 0.5)$  bits/octave.

# Single-Stage High-Order Modulators

---

If  $c_1 = c_2 = 0$ ,

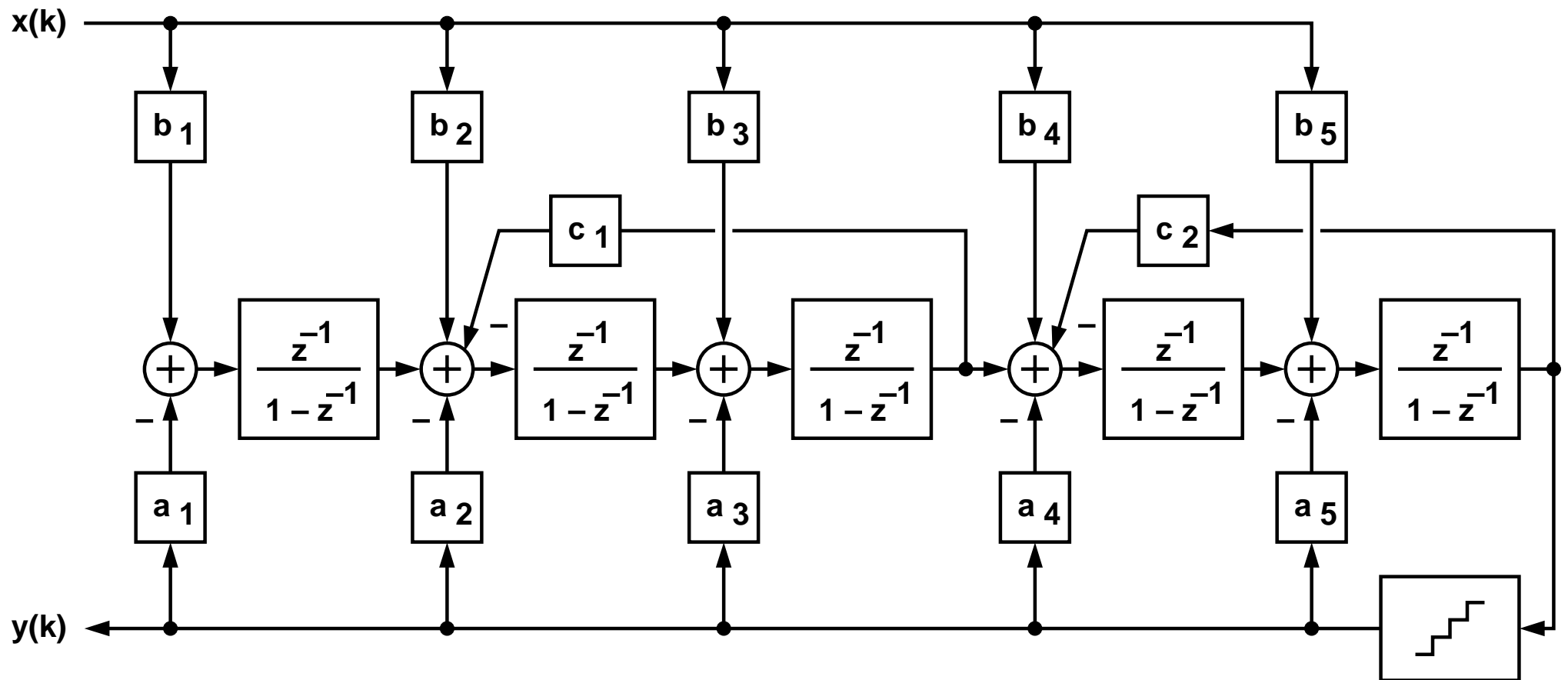
$$L(z) = G(z) = \frac{a_1}{(z-1)^1} + \frac{a_2}{(z-1)^2} + \frac{a_3}{(z-1)^3} + \dots$$

$$N_{TF}(z) = \frac{1}{1+L(z)} = \frac{(z-1)^n}{D(z)} \quad S_{TF}(z) = 1 - N_{TF}(z)$$

- $L(z)$  has all its poles at  $z = 1$  (or  $f = 0$ ).
- $N_{TF}(z)$  has all its zeros at  $z = 1$  (or  $f = 0$ ).
- Butterworth high-pass filters are often used for  $N_{TF}(z)$ .
- $S_{TF}(z)$  contains peaking at high frequencies.

If  $c_1 \neq 0$  and  $c_2 \neq 0$ , the poles of  $L(z)$  can be moved away from  $z = 1$  along the unit circle.

# Single-Stage High-Order Modulators



# Single-Stage High-Order Modulators

---

If  $c_1 = c_2 = 0$ ,

$$L(z) = \frac{a_1}{(z-1)^{n-0}} + \frac{a_2}{(z-1)^{n-1}} + \frac{a_3}{(z-1)^{n-2}} + \dots$$

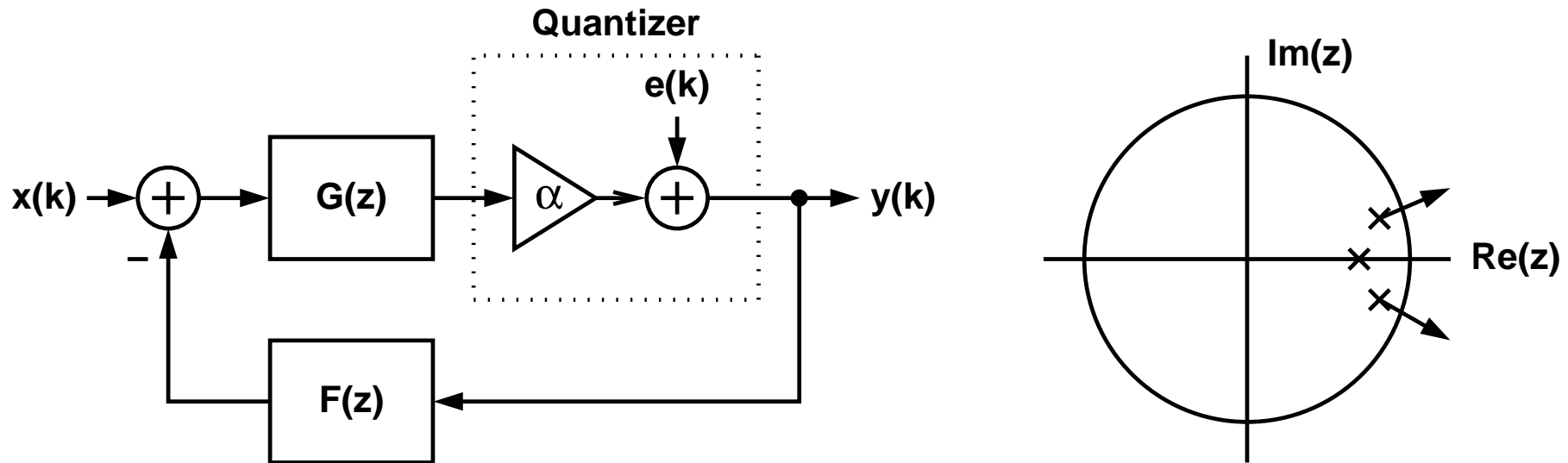
$$G(z) = \frac{b_1}{(z-1)^{n-0}} + \frac{b_2}{(z-1)^{n-1}} + \frac{b_3}{(z-1)^{n-2}} + \dots$$

$$N_{TF}(z) = \frac{1}{1+L(z)} = \frac{(z-1)^n}{D(z)} \quad S_{TF}(z) = \frac{b_1 + b_2(z-1) + b_3(z-1)^2 + \dots}{D(z)}$$

- The numerator of  $S_{TF}(z)$  is arbitrary, but has an order that is one less than  $D(z)$ .
- The  $S_{TF}(z)$  does not contain significant peaking.
- Each integrator output contain significant amounts of the input signal as well as filtered quantization noise.

If  $c_1 \neq 0$  and  $c_2 \neq 0$ , the poles of  $L(z)$  can be moved away from  $z = 1$  along the unit circle.

# Stability of Single-Stage High-Order Modulators



$$Y(z) = \frac{\alpha G(z)}{1 + \alpha G(z)F(z)} \cdot X(z) + \frac{1}{1 + \alpha G(z)F(z)} \cdot E(z)$$

- A modulator is called stable, if the input to the quantizer does not become overloaded, i.e.,  $e(k) \leq \pm\Delta/2$ .
- All high-order modulators ( $N > 2$ ) are conditionally stable.
- Modulators with multi-bit quantizer and DAC exhibit improved stability.

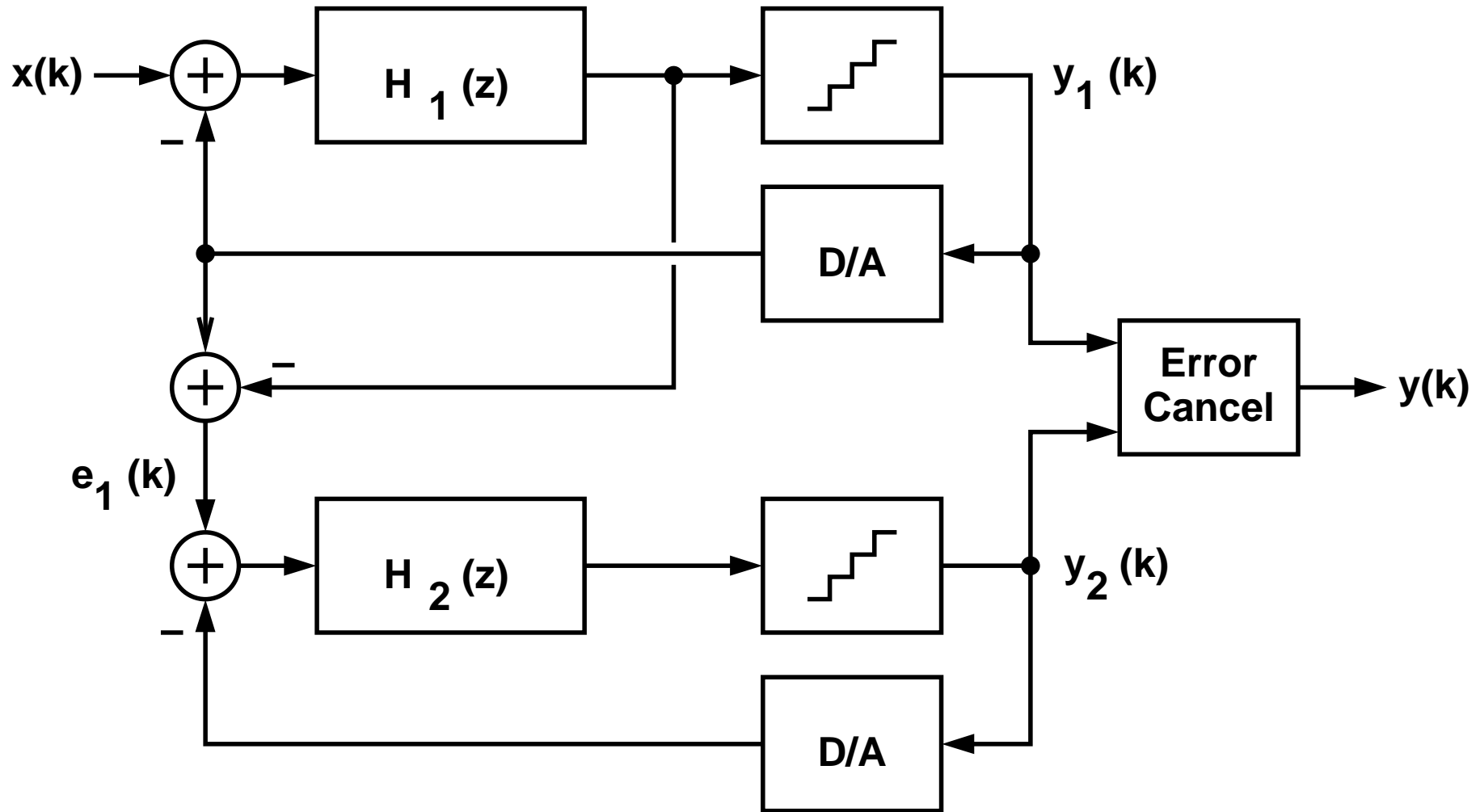
# Stability of Single-Stage High-Order Modulators

---

For single-stage modulators with one-bit quantizer and DAC:

- As a general rule of thumb, stability can be achieved by keeping  $\left| N_{TF} \left( e^{j\omega} \right) \right| \leq 1.5$ .
- A modulator can be made more stable by placing the poles closer to the zeros in  $N_{TF}(z)$ . But, the SNR is also degraded since the out-of-band gain of  $N_{TF}(z)$  is also reduced.
- Stability is also related to the input signal level. Typically want 50–80% of  $\Delta$  for stable input range.
- “Signal overload” and “power on” may cause a conditionally stable modulator to oscillate. Need additional mechanism to detect instability and force the loop becoming stable.

# Multi-Stage Cascaded Modulators



$$Y_1(z) = S_1(z) \cdot X(z) + N_1(z) \cdot E_1(z)$$

$$Y_2(z) = S_2(z) \cdot E_1(z) + N_2(z) \cdot E_2(z)$$

# Multi-Stage Cascaded Modulators

---

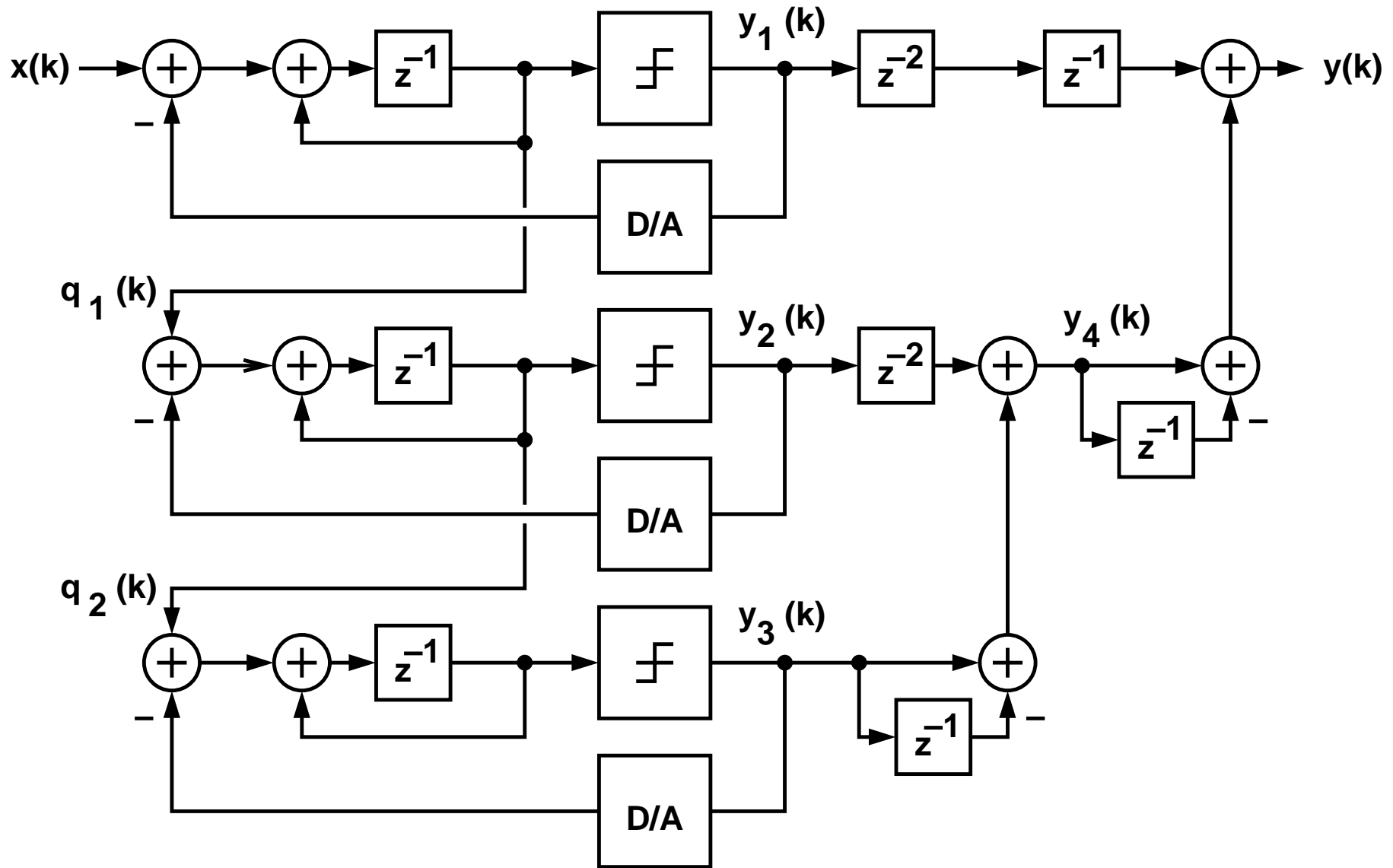
The error cancellation logic is

$$Y(z) = S'_2(z) \cdot Y_1(z) - N'_1(z) \cdot Y_2(z)$$

If  $S_2(z) = S'_2(z)$  and  $N_1(z) = N'_1(z)$ , then  $Y(z) = S_1(z)S_2(z) \cdot X(z) - N_1(z)N_2(z) \cdot E_2(z)$ .

- Also called multi-stage noise shaping (MASH) architecture.
- Individual loop can be low-order and stable. The resulting noise shaping function  $N_1(z)N_2(z) \cdots$  is high-order.
- Sensitive to mismatches between the analog and digital circuitry.
- For low-order loop, the finite opamp gain can cause noise leak-through.
- $y(k)$  has more than one bit, thus complicates the output DAC design in D/A applications or the decimation filter design in A/D applications.

# A Third-Order (1-1-1) Cascaded Modulators



## A Third-Order (1-1-1) Cascaded Modulators

---

The outputs of the quantizers are

$$\begin{aligned} Y_1 &= z^{-1}X + (1 - z^{-1}) E_1 & Q_1 &= Y_1 - E_1 = z^{-1}(X - E_1) \\ Y_2 &= z^{-1}Q_1 + (1 - z^{-1}) E_2 & Q_2 &= Y_2 - E_2 = z^{-1}(Q_1 - E_2) \\ Y_3 &= z^{-1}Q_2 + (1 - z^{-1}) E_3 = z^{-2}Q_1 - z^{-2}E_2 + (1 - z^{-1}) E_3 \end{aligned}$$

We have

$$Y_4 = z^{-2}Y_2 + (1 - z^{-1}) Y_3 = z^{-2}Q_1 + (1 - z^{-1})^2 E_3 = z^{-3}X - z^{-3}E_1 + (1 - z^{-1})^2 E_3$$

and

$$Y = z^{-3}Y_1 + (1 - z^{-1}) Y_4 = z^{-3}X + (1 - z^{-1})^3 E_3$$

## Idle Channel Tones (Pattern Noises)

---

For a 1st-order 1-bit modulator and  $\pm\Delta = \pm 1$ ,

$$y(k) = \text{sgn}[u(k)] = u(k) + e(k) \qquad u(k+1) = u(k) + x(k) - y(k)$$

If  $x(k) = 0$  and  $u(0) = 0$ , then

$$y(k) = (+1, -1) \dots \qquad e(k) = (+1, 0) \dots$$

If  $x(k) = 1/3$  and  $u(0) = 0$ , then

$$y(k) = (+1, -1, +1) \dots \qquad e(k) = (+1, -1/3, +1/3) \dots$$

If  $x(k) = 1/2$  and  $u(0) = 0$ , then

$$y(k) = (+1, -1, +1, +1) \dots \qquad e(k) = (+1, -1/2, 0, +1/2) \dots$$

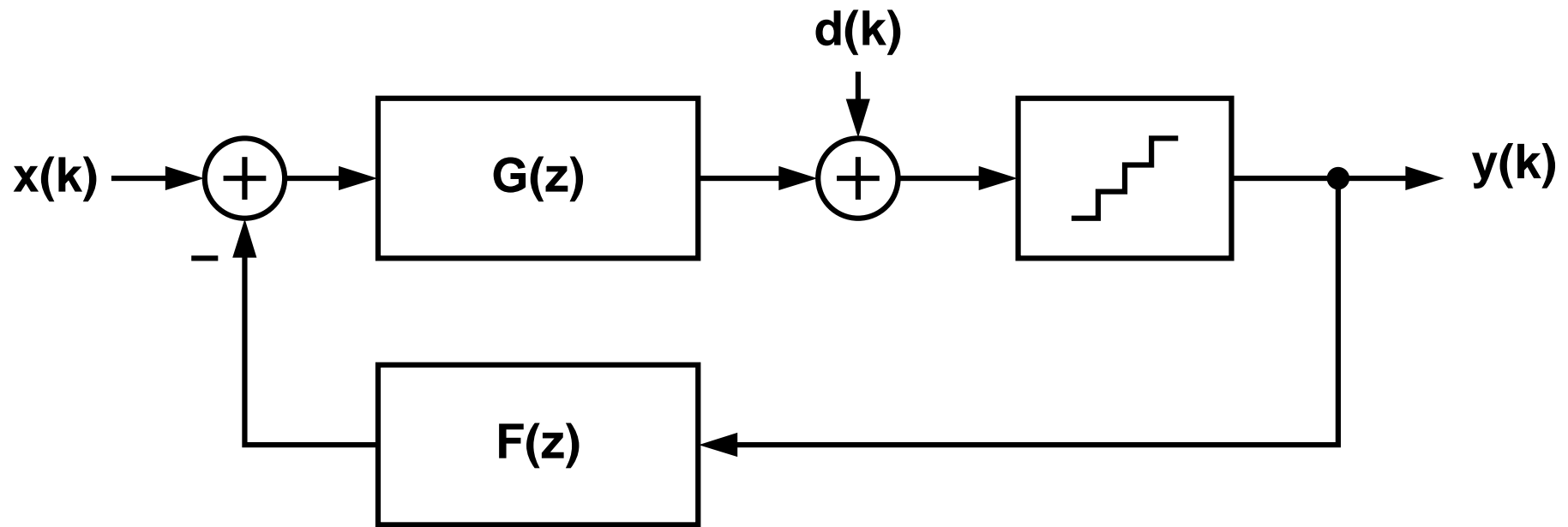
## Idle Channel Tones (Pattern Noises)

---

- In above examples,  $e$  is periodic and nowhere near white. Different initial states just shift the sequence and the values of  $e$ .
- For bounded input  $|u| < 1$ ,  $x$  is rational  $\Leftrightarrow y$  is periodic.
- Low-frequency tones cannot be filtered out by the following decimation filter.
- Tones also exists in higher-order modulators. The tones might not lie at a single frequency but instead be short-term periodic patterns.
- Nearly all types of modulators can produce very high-powered tones near  $f_s/2$ . Clock noise near this frequency can couple and demodulate these tones down into the baseband.
- For ac input, strong peaks and dips in the output noise power may be seen for certain input frequencies and amplitudes.

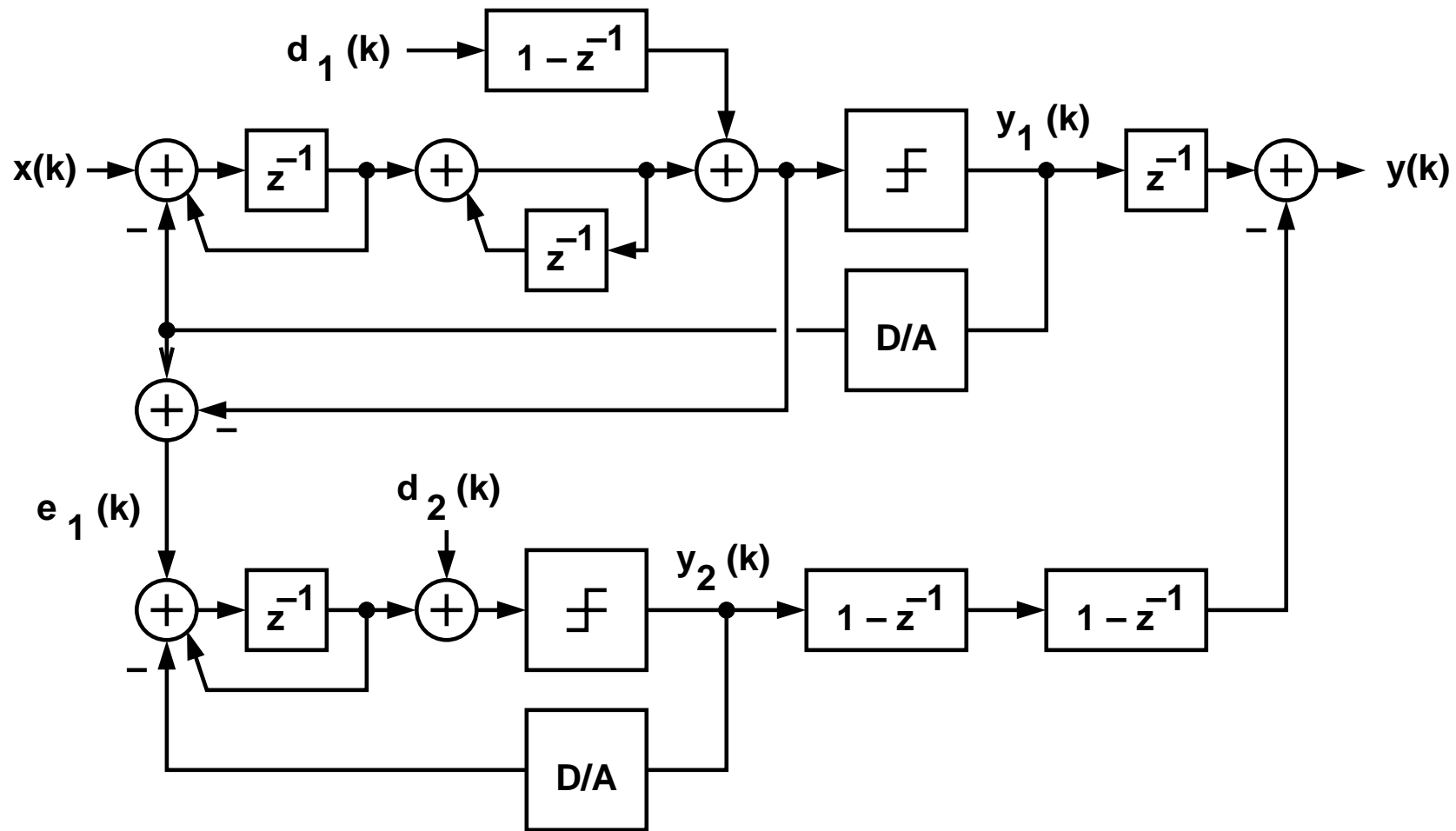
# Noise-Shaped Dithering for Single-Stage Modulators

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- $d(k)$  is a pseudo-random noise. It is usually generated by a PN sequence generator.
- The power  $d(k)$  must be comparable to that of  $e(k)$ . The pdf of  $d(k)$  usually spans more than  $\Delta/2$ .
- $d(k)$  may require 3–8 quantization levels for effective dithering.

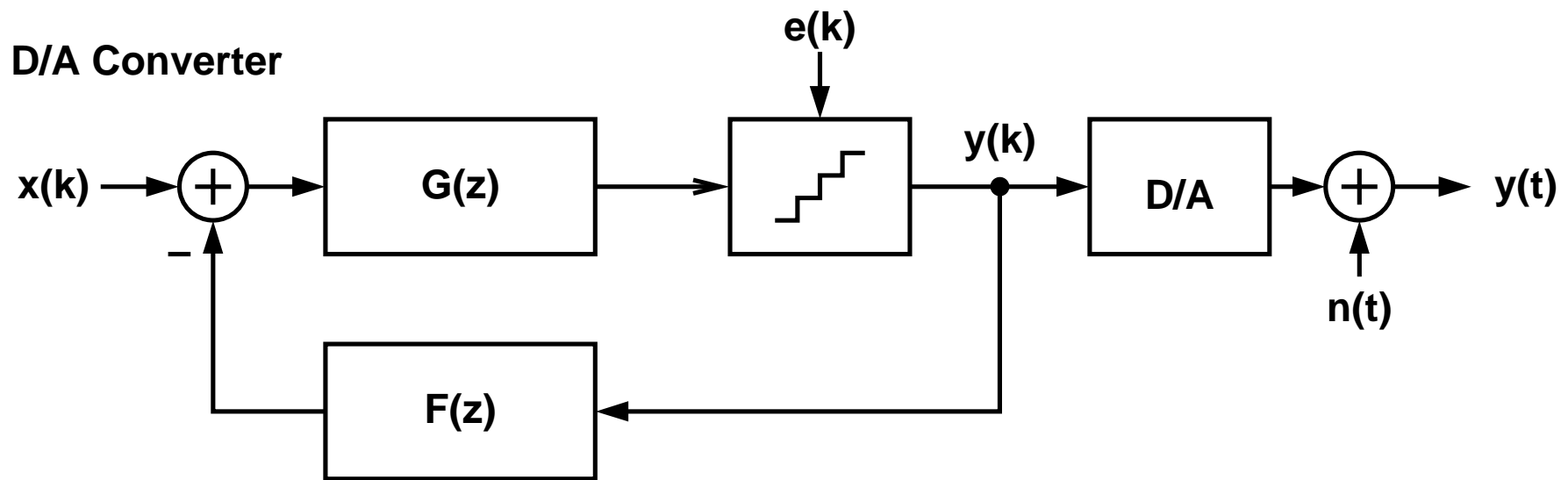
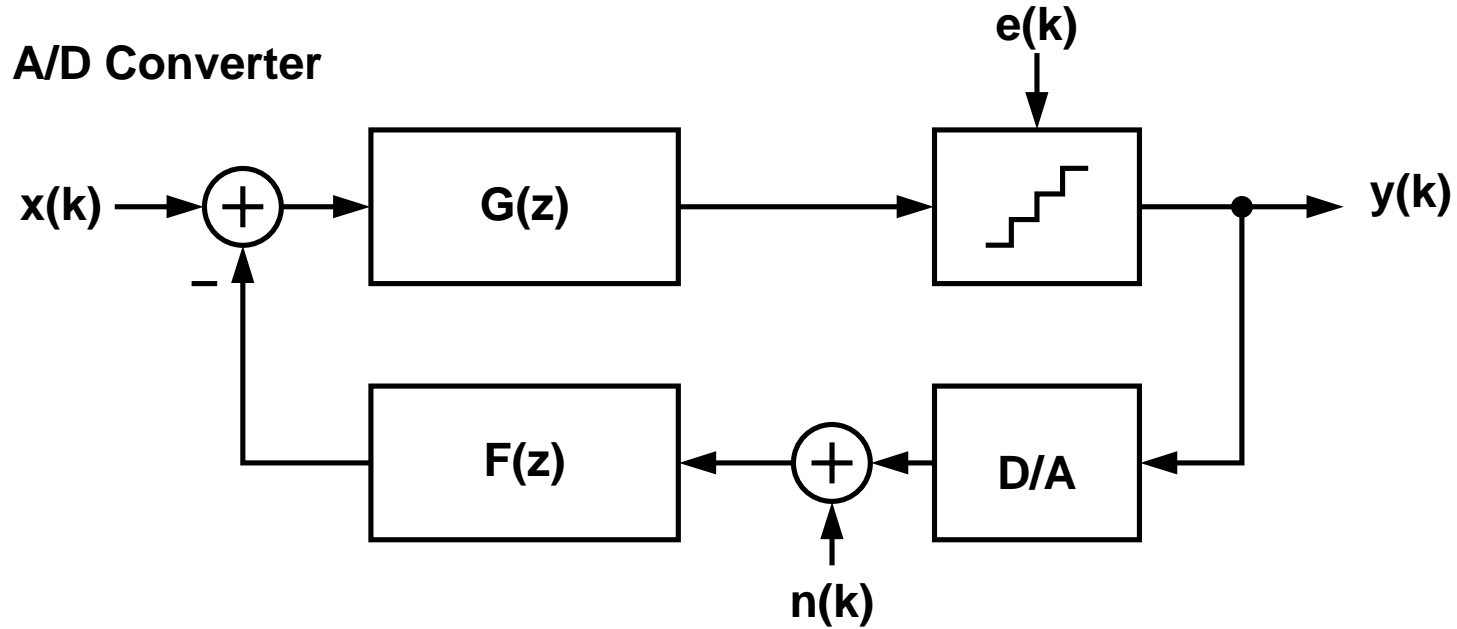
# Noise-Shaped Dithering for Multi-Stage Cascaded Modulators



$$Y_1 = z^{-1}X + (1 - z^{-1})^2 E_1 + (1 - z^{-1})^3 D_1 \quad Y_2 = z^{-1}E_1 + (1 - z^{-1}) E_2 + (1 - z^{-1}) D_2$$

$$Y = z^{-1}Y_1 - (1 - z^{-1})^2 Y_2 = z^{-2}X + z^{-1} (1 - z^{-1})^3 D_1 - (1 - z^{-1})^3 D_2$$

# Multi-Bit $\Delta\Sigma$ Modulator



# Multi-Bit $\Delta\Sigma$ Modulator

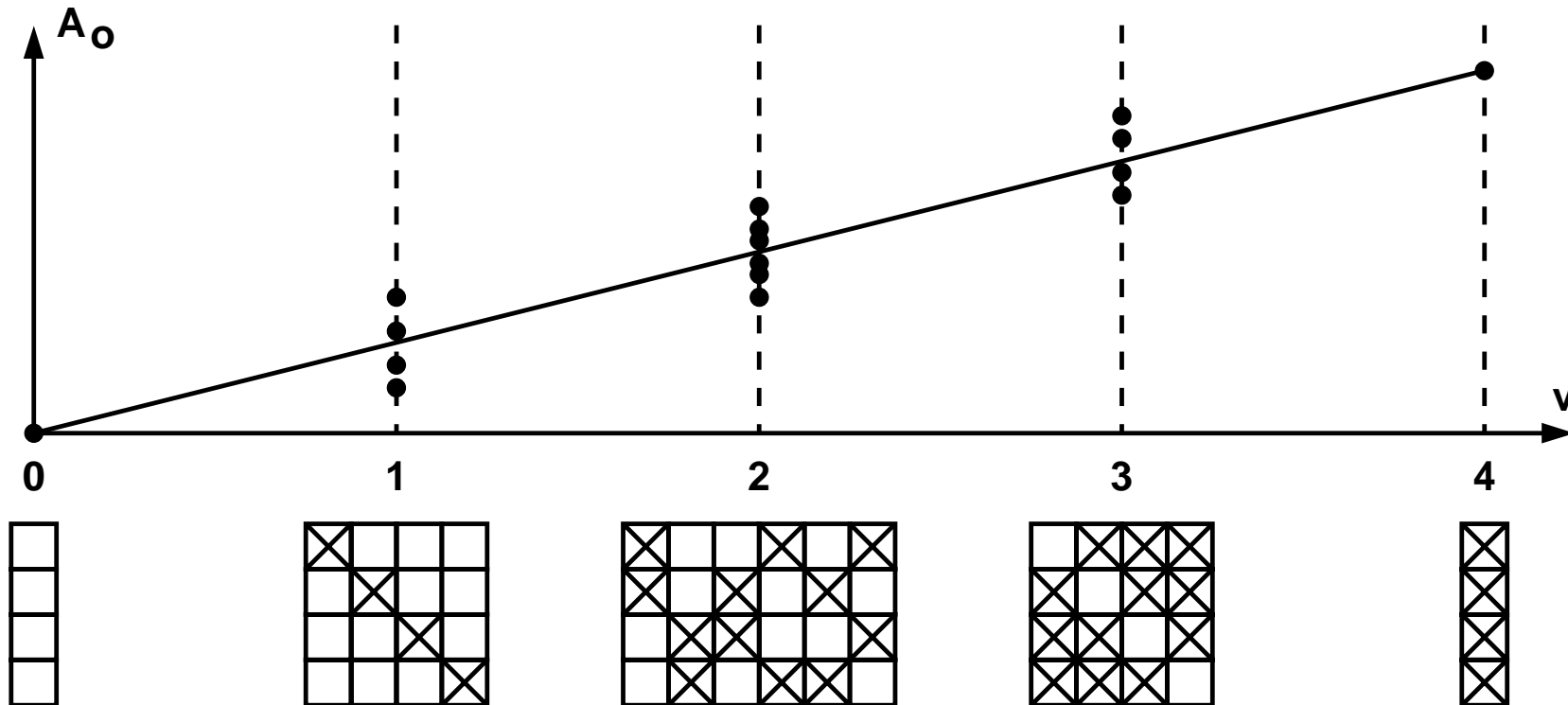
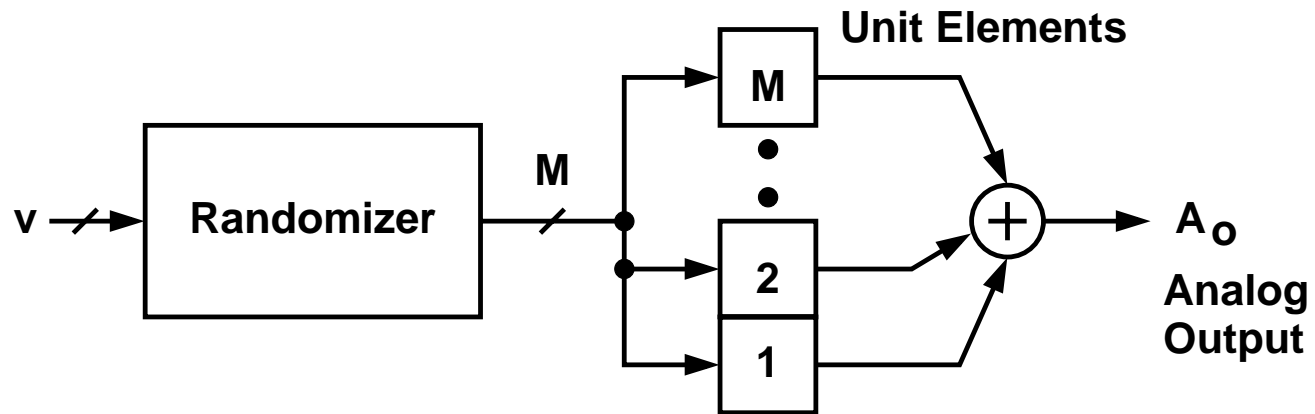
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For the A/D converter

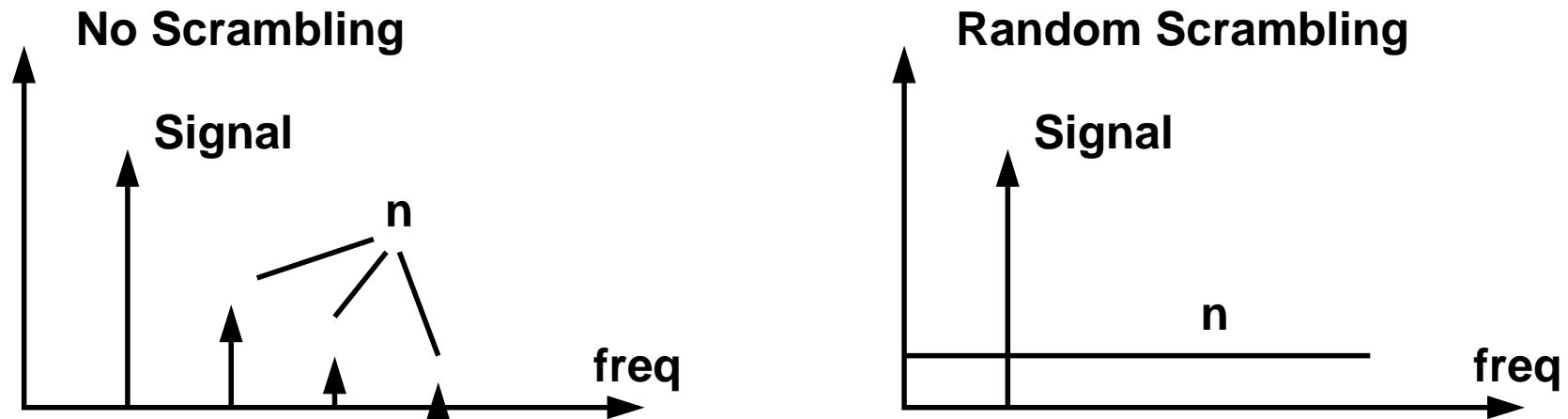
$$Y(z) = \frac{G(z)}{1 + F(z)G(z)}X(z) + \frac{1}{1 + F(z)G(z)}E(z) - \frac{F(z)G(z)}{1 + F(z)G(z)}N(z)$$
$$\approx S_{TF}(z)X(z) + N_{TF}(z)E(z) - N(z)$$

- Out-of-band noise is reduced. Requirements for the analog circuitry are less severe.
- Since they have better stability, more aggressive noise transfer functions may be used.
- The DAC linearity errors are not shaped. The DAC must be nearly as linear as the complete converter.

# Multi-Bit DAC — Dynamic Element Matching

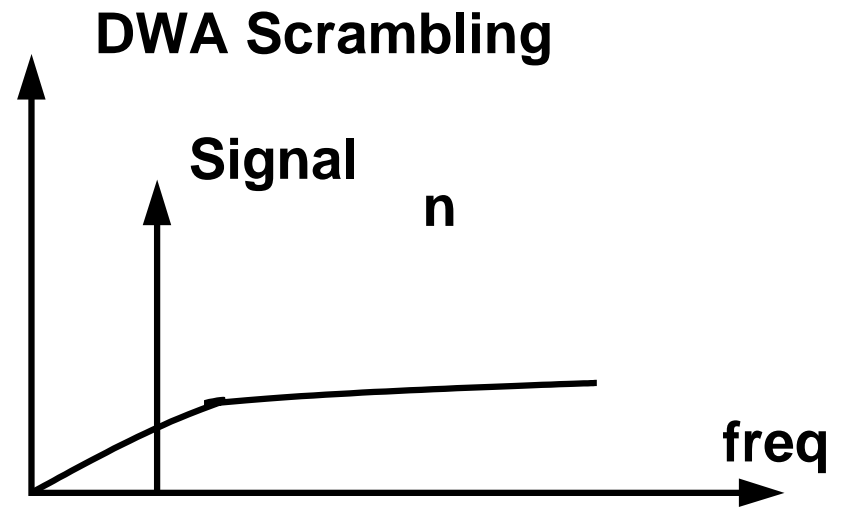
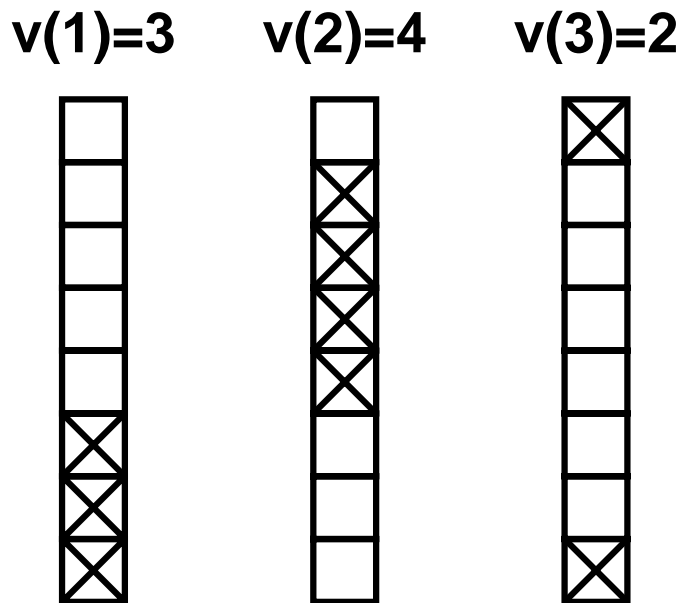
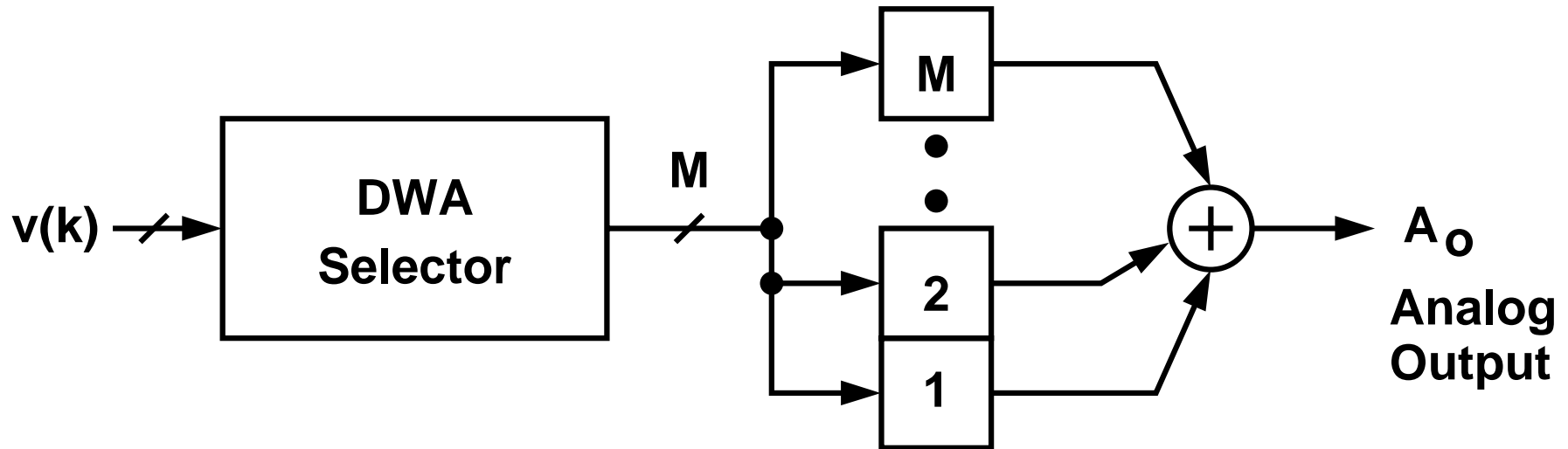


# Multi-Bit DAC — Dynamic Element Matching



- For any value of  $v$ , the averaged error in  $A_o$  is zero.
- Whitens the mismatch noise.
- The randomizer may consist of a thermometer-type encoder, a random-number generator, and a switchbox. Butterfly structure is often used to simplify the switchbox design.
- Reference: Ian Galton, "A Rigorous Error Analysis of D/A Conversion with Dynamic Element Matching," *Trans. on Circuits and Systems-II*, pp. 763–772, 12/95.

# Multi-Bit DAC — Data-Weighted Averaging

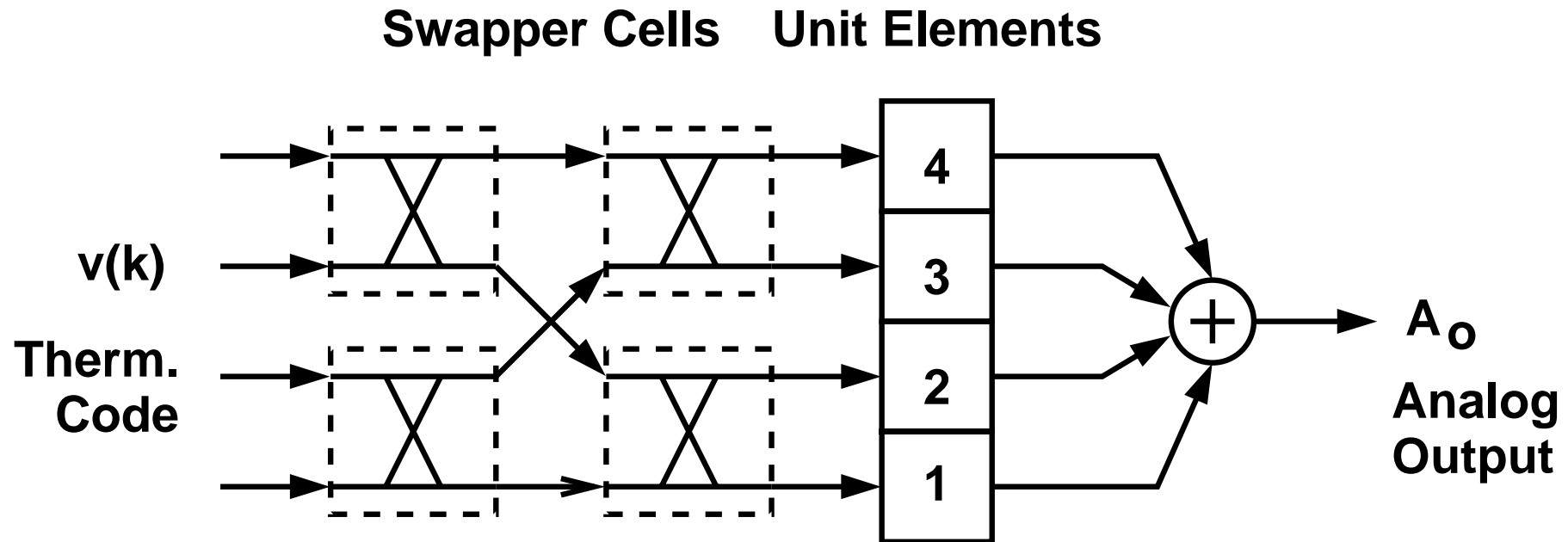


## Multi-Bit DAC — Data-Weighted Averaging

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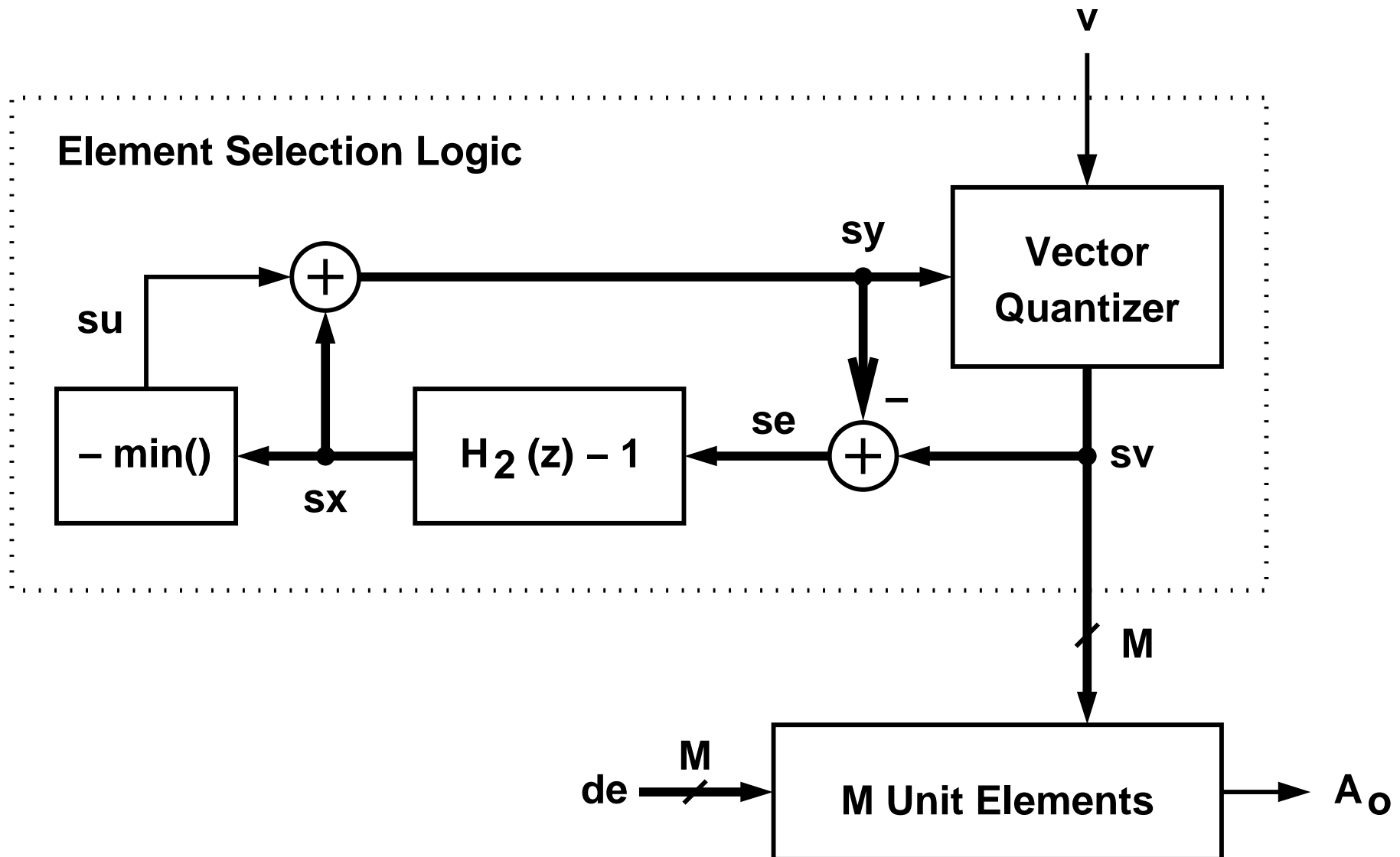
- Once every element in the array has been used, the cumulative error is zero. The errors induced by the use of each element are averaged out as soon as possible.
- Reference: R. Baird and T. Fiez, “Linearity Enhancement of Multibit  $\Delta\Sigma$  A/D and D/A Converters Using Data Weighted Averaging,” *Tran. on Circuits and Systems–II*, pp. 753–762, 12/95.

# Multi-Bit DAC — Noise-Shaped Scrambler



- Each swapper tries to equalize the activity of each of its outputs. Each output from the scramble is a first-order noise-shaped sequence.
- Reference: R. Adams, et al, "A 113dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling," ISSCC, pp. 62–63, 2/98.

# General Mismatch-Shaping DAC



# General Mismatch-Shaping DAC

---

- The element selection logic (ESL) is a collection of  $M$  digital  $\Delta\Sigma$  modulators, each possessing a  $N_{TF}(z)$  equal to  $H_2(z)$ , implemented with the error feedback structure and supplied with a common input.
- The vector quantizer uses information in the  $\mathbf{sy}$  vector to select which  $v$  elements to enable. Want to minimize  $\mathbf{se} = \mathbf{sv} - \mathbf{sy}$ .
- The  $\mathbf{sy} = \mathbf{sx} - \min(\mathbf{sx}) \cdot [11 \dots 1]$  function is a shifting operation which set the minimum component in  $\mathbf{sy}$  to zero. The purpose is to reduce the magnitude of  $\mathbf{sy}$  vector, in a manner that does not disturb the noise-shaping property of the selection logic.

# General Mismatch-Shaping DAC

---

Let  $\mathbf{de} = [e_1, e_2, \dots, e_M]$  be the DAC error vector.

- By definition,  $\mathbf{de} \cdot [\mathbf{0}]^T = 0$  and  $\mathbf{de} \cdot [\mathbf{1}]^T = 0$ , where  $[\mathbf{0}] = [00 \dots 0]$  and  $[\mathbf{1}] = [11 \dots 1]$ .
- $\mathbf{de} \cdot (\mathbf{sv}_1 + \mathbf{sv}_2)^T = \mathbf{de} \cdot \mathbf{sv}_1^T + \mathbf{de} \cdot \mathbf{sv}_2^T$
- $\mathbf{de} \cdot \mathbf{sv}^T + \mathbf{de} \cdot \overline{\mathbf{sv}}^T = 0$

For the error-feedback structure, we have

$$\mathbf{SV}(z) = SU(z) \cdot [\mathbf{1}] + H_2(z) \cdot \mathbf{SE}(z)$$

# General Mismatch-Shaping DAC

---

The vector quantizer obeys

$$\mathbf{SV}(z) \cdot [\mathbf{1}]^T = V(z)$$

The analog output is

$$\begin{aligned} A_o(z) &= \mathbf{SV}(z) \cdot ([\mathbf{1}] + \mathbf{DE})^T \\ &= \mathbf{SV}(z) \cdot [\mathbf{1}]^T + \mathbf{SV}(z) \cdot \mathbf{DE}^T \\ &= V(z) + SU(z) \cdot [\mathbf{1}] \cdot \mathbf{DE}^T + H_2(z) \cdot \mathbf{SE}(z) \cdot \mathbf{DE}^T \\ &= V(z) + H_2(z) \left( \mathbf{SE}(z) \cdot \mathbf{DE}^T \right) \end{aligned}$$

# General Mismatch-Shaping DAC — First-Order Example

---

$$M = 4 \quad H_2(z) = 1 - z^{-1}$$

$$\mathbf{sv}(k) = VQ[\mathbf{sy}(k)] \quad \mathbf{se}(k) = \mathbf{sv}(k) - \mathbf{sy}(k) \quad \mathbf{sx}(k) = -\mathbf{se}(k - 1)$$

$k$	$v(k)$	$\mathbf{sy}(k)$	$\mathbf{sv}(k)$	$\mathbf{se}(k)$	$\mathbf{sx}(k)$
0	1	1, 1, 1, 1	1, 0, 0, 0	+0, -1, -1, -1	-0, +1, +1, +1
1	1	0, 1, 1, 1	0, 1, 0, 0	+0, +0, -1, -1	-0, -0, +1, +1
2	1	0, 0, 1, 1	0, 0, 1, 0	+0, +0, +0, -1	-0, -0, -0, +1
3	2	0, 0, 0, 1	1, 0, 0, 1	+1, +0, +0, +0	-1, -0, -0, -0
4	0	0, 1, 1, 1	0, 0, 0, 0	+0, -1, -1, -1	-0, +1, +1, +1
5	4	0, 1, 1, 1	1, 1, 1, 1	+1, +0, +0, +0	-1, -0, -0, -0
6	2	0, 1, 1, 1	0, 1, 1, 0	+0, +0, +0, -1	-0, -0, -0, +1

- Since  $\mathbf{de} \cdot \mathbf{sv}^T = -\mathbf{de} \cdot \overline{\mathbf{sv}}^T$ , we can add [1] to  $\mathbf{sy}$  at any time.
- The first-order algorithm is similar to the data-weighted averaging algorithm.

# General Mismatch-Shaping DAC — Second-Order Example

---

$$M = 4 \quad H_2(z) = (1 - z^{-1})^2$$

$$\mathbf{sv}(k) = \mathbf{VQ}[\mathbf{sy}(k)] \quad \mathbf{se}(k) = \mathbf{sv}(k) - \mathbf{sy}(k) \quad \mathbf{sx}(k) = -2\mathbf{se}(k - 1) + \mathbf{se}(k - 2)$$

$k$	$v(k)$	$\mathbf{sy}(k)$	$\mathbf{sv}(k)$	$\mathbf{se}(k)$	$\mathbf{sx}(k)$
0	1	1, 1, 1, 1	1, 0, 0, 0	+0, -1, -1, -1	-0, +2, +2, +2
1	1	0, 2, 2, 2	0, 1, 0, 0	+0, -1, -2, -2	-0, +1, +3, +3
2	1	0, 1, 3, 3	0, 0, 1, 0	+0, -1, -2, -3	-0, +1, +2, +4
3	2	0, 1, 2, 4	0, 0, 1, 1	+0, -1, -1, -3	-0, +1, +0, +3
4	0	0, 1, 0, 3	0, 0, 0, 0	+0, -1, +0, -3	-0, +1, -1, +3
5	4	1, 2, 0, 4	1, 1, 1, 1	+0, -1, +1, -3	-0, +1, -2, +3
6	2	2, 3, 0, 5	0, 1, 0, 1	-2, -2, +0, -4	+4, +3, +1, +5

# General Mismatch-Shaping DAC — Second-Order Example

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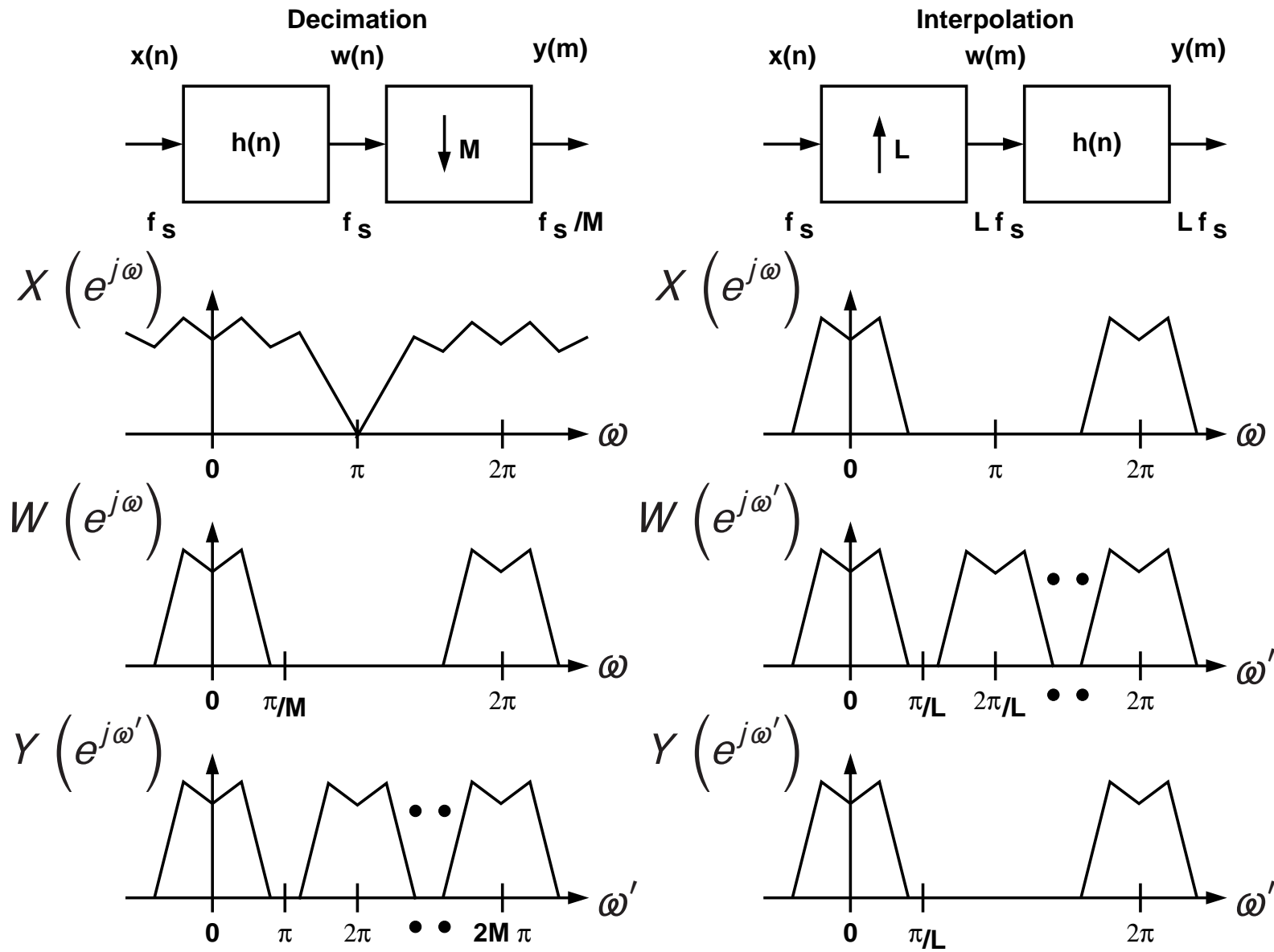
- The element selection logic (ESL) is stable, i.e, **se** is bounded, for  $H_2(z) = \left(1 - z^{-1}\right)^2$ , as long as  $v$  stays away from the extremes of its range.
- When a binary modulator is unstable with an  $N_{TF}(z)$  equal to  $H_2(z)$ , the corresponding ESL algorithm must also be unstable.
- Adding dither to **sy** may be necessary to whiten the noise caused by a deterministic selection algorithm.

# Multi-Bit Unit Elements

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- If polarity reversal or repeated use of an unit element in one period is allowed, the components of  $\mathbf{sv}$  need not be restricted to  $\{0, 1\}$ .
- Multi-bit can enhance the stability of the ESL in the same manner that multi-bit feedback enhances the stability of a regular  $\Delta\Sigma$  modulator.
- The key circuit constraint is the need to ensure that each usage of an element results in the same error.

# Decimation and Interpolation



# Decimation and Interpolation

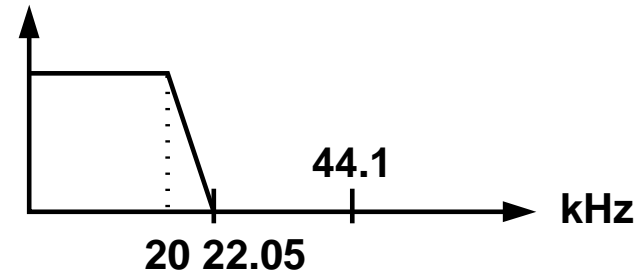
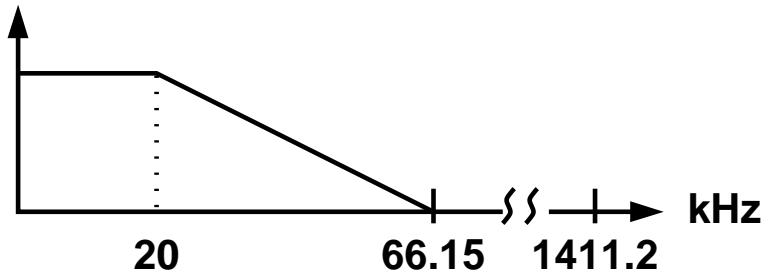
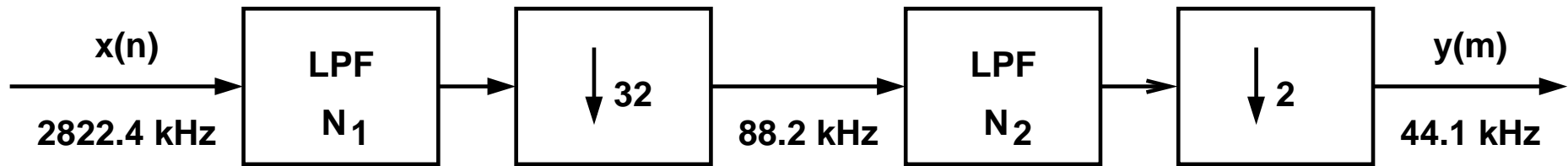
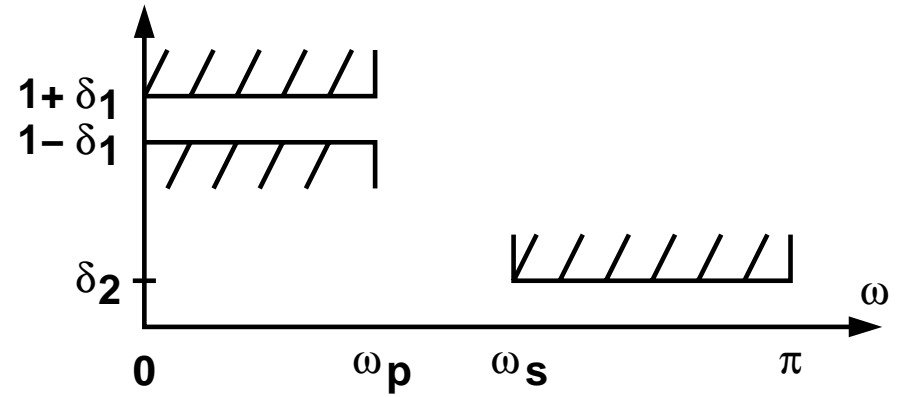
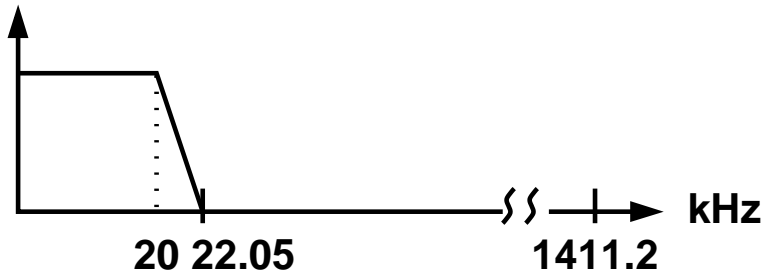
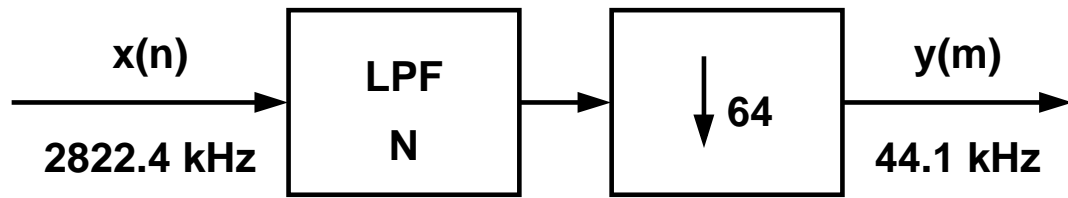
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$$\text{Decimation Filter} = y(m) = \sum_{k=-\infty}^{\infty} h(k)x(Mm - k)$$

$$\text{Interpolation Filter} = y(m) = \sum_{k=-\infty}^{\infty} h(m - kL)x(k)$$

- The processes of decimation and interpolation are in effect duals.
- A filter defined for one process can often be used for other if the same parameters are used.
- An architecture that is efficiently defined for one process can often be transposed for used as an efficient architecture in the dual process.

# Multi-Stage Rate Conversion



# Multi-Stage Rate Conversion

---

- The order  $N$  of an equiripple FIR filter is

$$N \approx \frac{f(\delta_1, \delta_2) - g(\delta_1, \delta_2)(\Delta\omega)^2}{\Delta\omega} \approx \frac{-10 \log_{10}(\delta_1 \delta_2) - 13}{14.6 \Delta\omega}$$

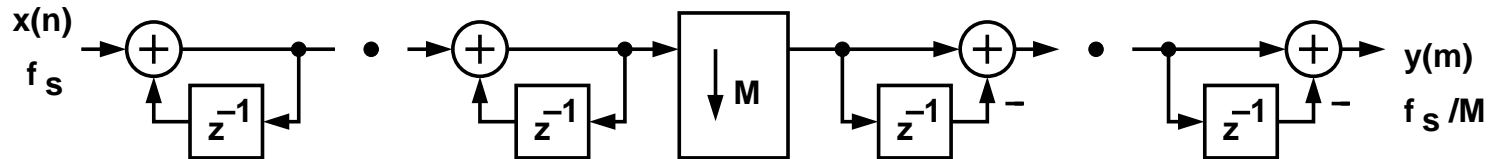
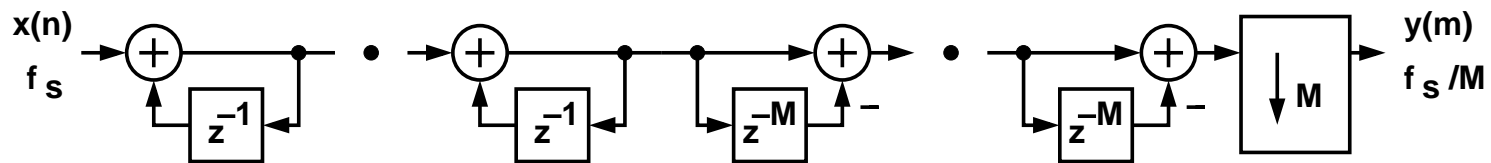
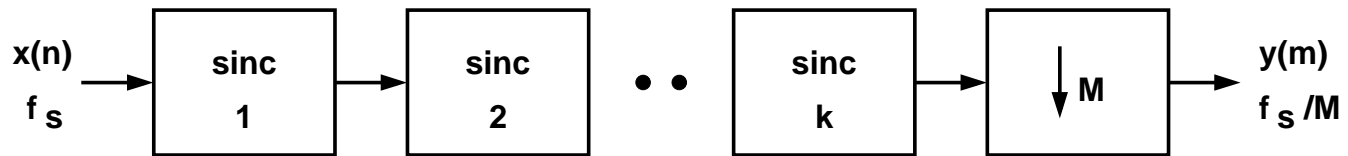
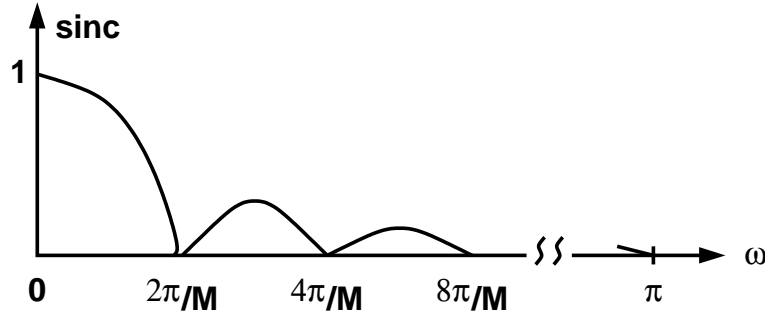
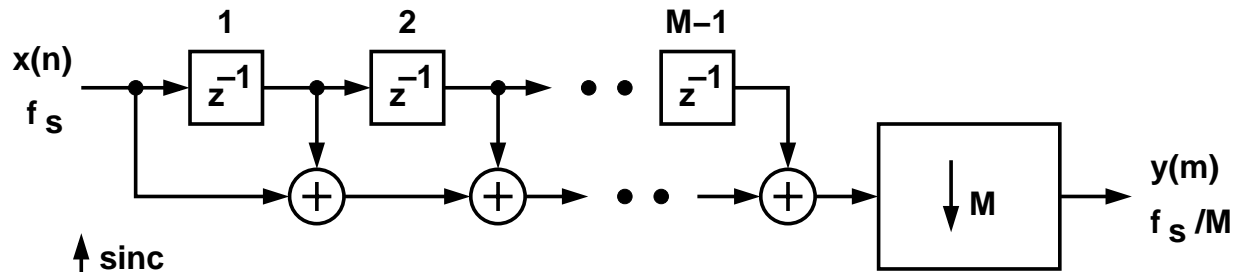
$$f(\delta_1, \delta_2) = (0.005309x_1^2 + 0.07114x_1 - 0.4761)x_2 - (0.00266x_1^2 + 0.5941x_1 + 0.4278)$$

$$g(\delta_1, \delta_2) = 11.012 + 0.51244(x_1 - x_2)$$

$$\Delta\omega = \frac{\omega_s - \omega_p}{2\pi} \quad x_1 = \log_{10} \delta_1 \quad x_2 = \log_{10} \delta_2$$

- For the single-stage design,  $\delta_1 = 0.001$ ,  $\delta_2 = 0.00001$ , then  $N = 6250$ . For the two-stage design,  $\delta_1 = 0.001/2$ ,  $\delta_2 = 0.00001$ , then  $N_1 = 291$  and  $N_2 = 205$ .
- Practical considerations sometimes lead to the conclusion that a two-stage design is best.
- For most cases, the choice of 2 : 1 for the last stage is both the theoretically best option as well as the most practical one.

# sinc<sup>k</sup> Filters



# sinc<sup>k</sup> Filters

---

The sinc filter transfer function is

$$H_1(z) = \frac{1}{M} \sum_{i=0}^{M-1} z^{-i} = \frac{1}{M} \left( \frac{1 - z^{-M}}{1 - z^{-1}} \right)$$

$$H_1(e^{j\omega}) = \frac{1}{M} \cdot \frac{\sin(\omega M/2)}{\sin(\omega/2)} = \frac{\text{sinc}(\omega M/2)}{\text{sinc}(\omega/2)} \quad \text{sinc}(x) = \frac{\sin(x)}{x}$$

The sinc<sup>k</sup> filter transfer function is

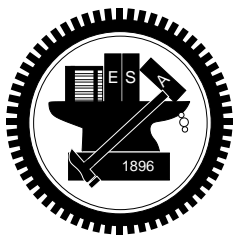
$$H(z) = [H_1(z)]^k = \frac{1}{M^k} \left( \frac{1 - z^{-M}}{1 - z^{-1}} \right)^k = \frac{1}{M^k} \cdot \left( \frac{1}{1 - z^{-1}} \right)^k \cdot (1 - z^{-M})^k$$

- The integrator-differentiator architecture is inherently stable, when 2's-complement arithmetic is used due to its wrap-around characteristic.

# Phase-Locked Loops

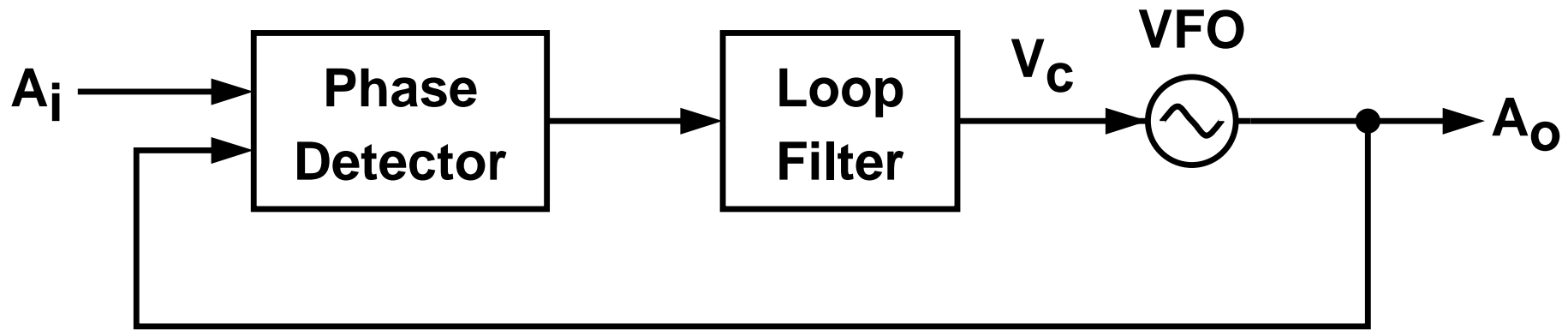
Jieh-Tsorng Wu

July 16, 2002



National Chiao-Tung University  
Department of Electronics Engineering

# Phase-Locked Loops (PLLs)



$$A_i = g_1(\omega_i t + \theta_i)$$

$$A_o = g_2(\omega_o t + \theta_o)$$

$$\omega_o = \omega_{oo} + K_c \cdot V_c$$

- $g_1$  and  $g_2$  are periodic functions with  $2\pi$  period.
- When the loop is *locked*, the frequency of the VCO is exactly equal to the average frequency of the input.
- The loop filter is a low-pass filter that suppresses high-frequency signal components in the phase difference.

# Phase-Locked Loops (PLLs)

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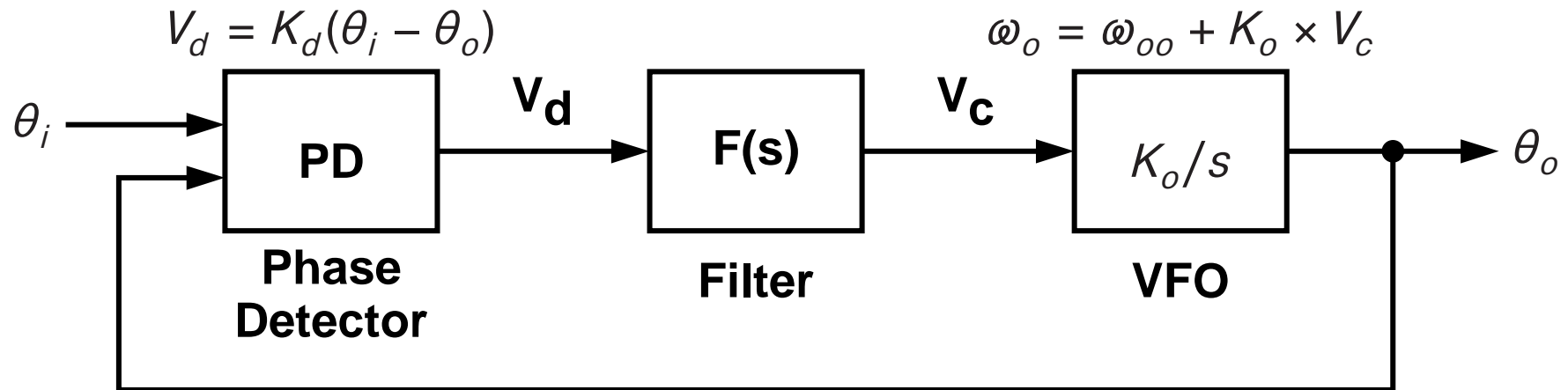
## Applications:

- Automatic frequency control.
- Frequency and phase demodulation.
- Data and clock recovery.
- Frequency synthesis.

## References:

- Roland E. Best, *“Phase-Locked Loops,”* 2nd Edition, McGraw-Hill, Inc., 1993.
- Dan H. Wolaver, *“Phase-Locked Loop Circuit Design,”* Prentice-Hall, Inc., 1991.
- Floyd M. Gardner, *“Phaselock Techniques,”* 2nd Edition, John Wiley & Sons, 1979.

## Basic Model



When the PLL is locked,

$$V_d(s) = K_d \cdot [\theta_i(s) - \theta_o(s)] = K_d \theta_e(s) \quad \theta_e = \theta_i - \theta_o$$

$$V_c(s) = F(s) \cdot V_d(s)$$

$$\int \omega_o dt = \omega_{oo}t + \int K_o V_c dt = \omega_{oo}t + \theta_o \quad \Rightarrow \quad \theta_o(s) = V_c(s) \cdot \frac{K_o}{s}$$

- $\theta_e$  is the phase error,  $K_d$  is the phase-detector gain factor, and  $K_o$  is the VCO gain factor.

## Basic Model

---

System equations are

$$V_d = K_d \cdot (\theta_i - \theta_o) = K_d \cdot \theta_e \quad V_c = F(s) \cdot V_d \quad \theta_o = V_c \cdot \frac{K_o}{s}$$

The transfer functions are

$$\frac{\theta_o}{\theta_i} = \frac{K_o K_d F(s)}{s + K_o K_d F(s)} = H(s)$$

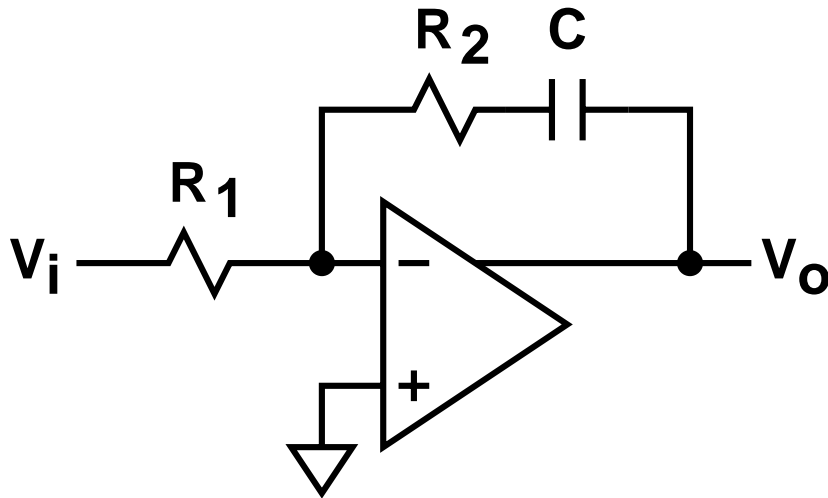
$$\frac{\theta_e}{\theta_i} = \frac{s}{s + K_o K_d F(s)} = 1 - H(s)$$

$$\frac{V_c}{\theta_i} = \frac{s K_d F(s)}{s + K_o K_d F(s)} = \frac{s}{K_o} \cdot H(s)$$

$$\Rightarrow H(s) = \frac{\Delta\omega_o}{\Delta\omega_i} = K_o \cdot \frac{V_c}{\Delta\omega_i} \quad \Delta\omega_i = \omega_i - \omega_{oo} \quad \Delta\omega_o = \omega_o - \omega_{oo}$$

- $H(s)$  is the closed-loop transfer function.

## Second-Order PLL — Active Lag-Lead Filter



$$F(s) = -\frac{s\tau_2 + 1}{s\tau_1}$$

$$\tau_1 = R_1C$$

$$\tau_2 = R_2C$$

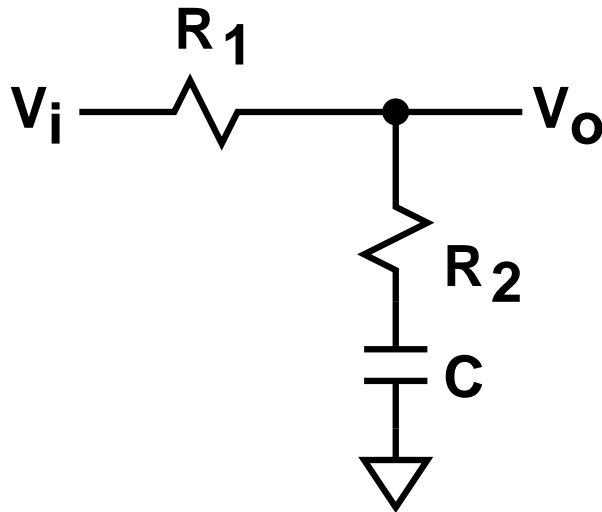
$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1}}$$

$$\zeta = \frac{\omega_n}{2} \cdot \tau_2$$

- $\omega_n$  is the *pole frequency* of the loop.
- $\zeta$  is the damping factor.  $Q_p = 1/(2\zeta)$  is the pole quality factor.

## Second-Order PLL — Passive Lag-Lead Filter



$$F(s) = \frac{s\tau_2 + 1}{s\tau_1 + 1}$$

$$\tau_1 = (R_1 + R_2)C$$

$$\tau_2 = R_2C$$

$$H(s) = \frac{s \left[ 2\zeta\omega_n - \omega_n^2 / (K_o K_d) \right] + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1}}$$

$$\zeta = \frac{\omega_n}{2} \left( \tau_2 + \frac{1}{K_o K_d} \right)$$

- If  $R_2 = 0$ , then

$$\tau_1 = \frac{1}{R_1 C} = \frac{1}{\omega_{LF}}$$

$$\omega_n = \sqrt{K_o K_d \omega_{LF}}$$

$$\zeta = \frac{\omega_n}{2K_o K_d}$$

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

# High-Gain Second-Order PLL Frequency Response

---

If  $K_o K_d \tau_2 \gg 1$  in the passive filter, then

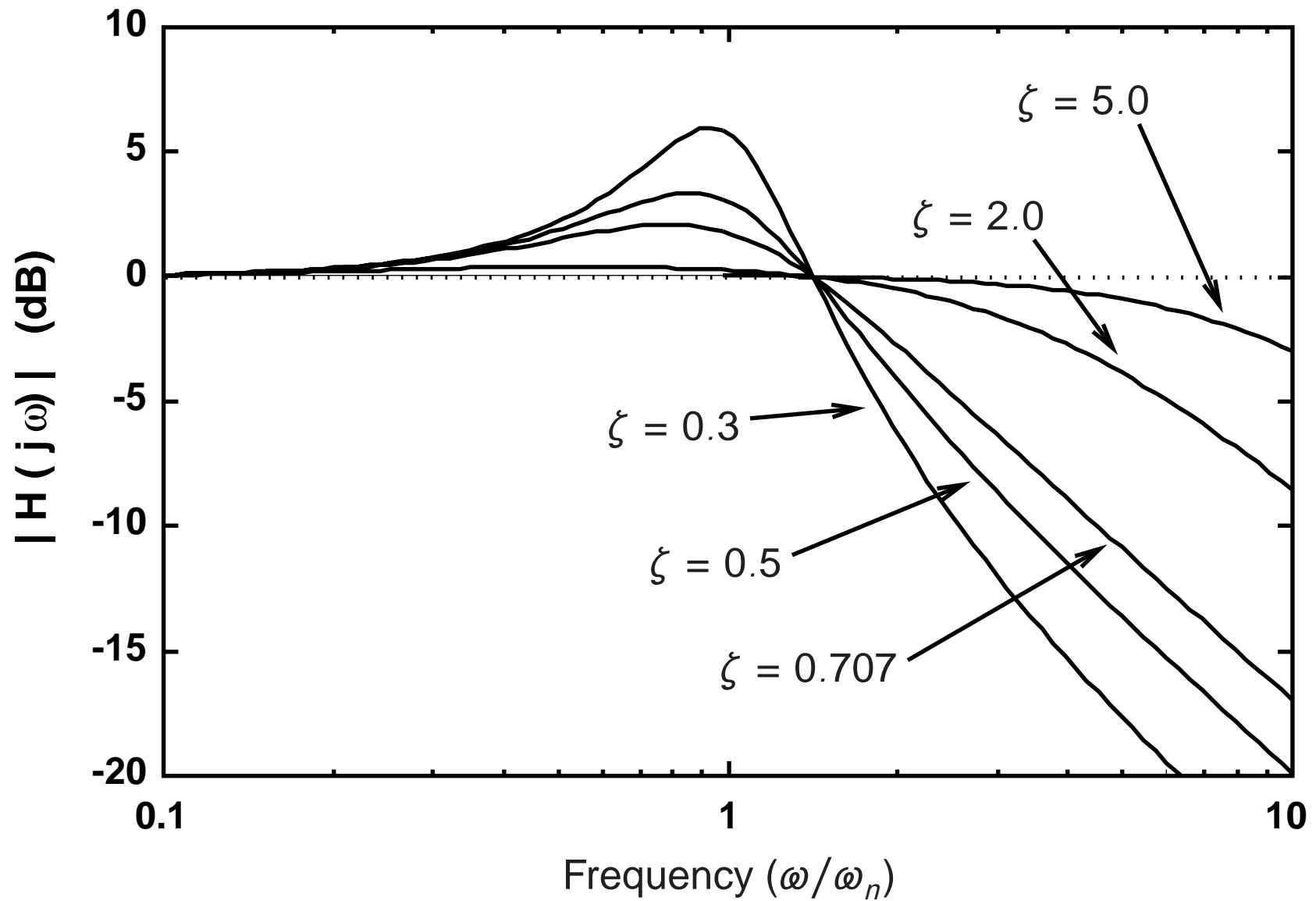
$$H_{\text{passive}}(s) \approx H_{\text{active}}(s) = \frac{2\zeta \omega_n s + \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2}$$

And the  $-3$  dB bandwidth of  $H(s)$  is

$$\omega_{-3\text{dB}} = \omega_n \left[ 2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1} \right]^{1/2}$$

- Usually choose  $\omega_n < \omega_i/10$  to remove the high-frequency components at  $\omega_i, 2\omega_i, \dots$ , existing in the phase detector's output.
- The PD output's high-frequency components can show up as spurious tones in the frequency spectrum of the PLL's output.

# High-Gain Second-Order PLL Frequency Response



# Step Response of a Two-Pole System

---

Consider the following two-pole transfer function

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \text{Poles} = s_{1,2} = \left(-\zeta \pm \sqrt{\zeta^2 - 1}\right) \omega_n$$

- If  $\zeta > 1$ , the system is overdamped, and both poles are real.

$$\text{Step Response} = 1 - \frac{1}{2\sqrt{\zeta^2 - 1}} \left( \frac{1}{k_1} e^{-k_1\omega_n t} - \frac{1}{k_2} e^{-k_2\omega_n t} \right)$$

$$k_1 = \zeta - \sqrt{\zeta^2 - 1} \quad k_2 = \zeta + \sqrt{\zeta^2 - 1}$$

- If  $\zeta = 1$ , the system is critically damped, and both poles are at  $-\omega_n$ .

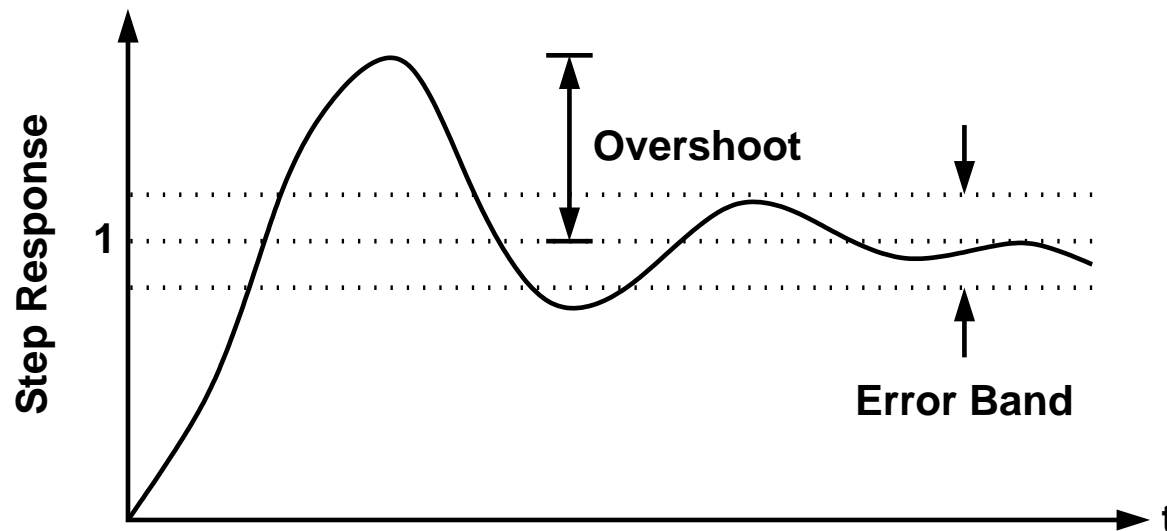
$$\text{Step Response} = 1 - (1 + \omega_n t) e^{-\omega_n t} \approx 1 - e^{-\omega_n t / (2\zeta)} \quad \text{if } 4\zeta^2 \gg 1$$

# Step Response of a Two-Pole System

- If  $\zeta < 1$ , the system is underdamped.

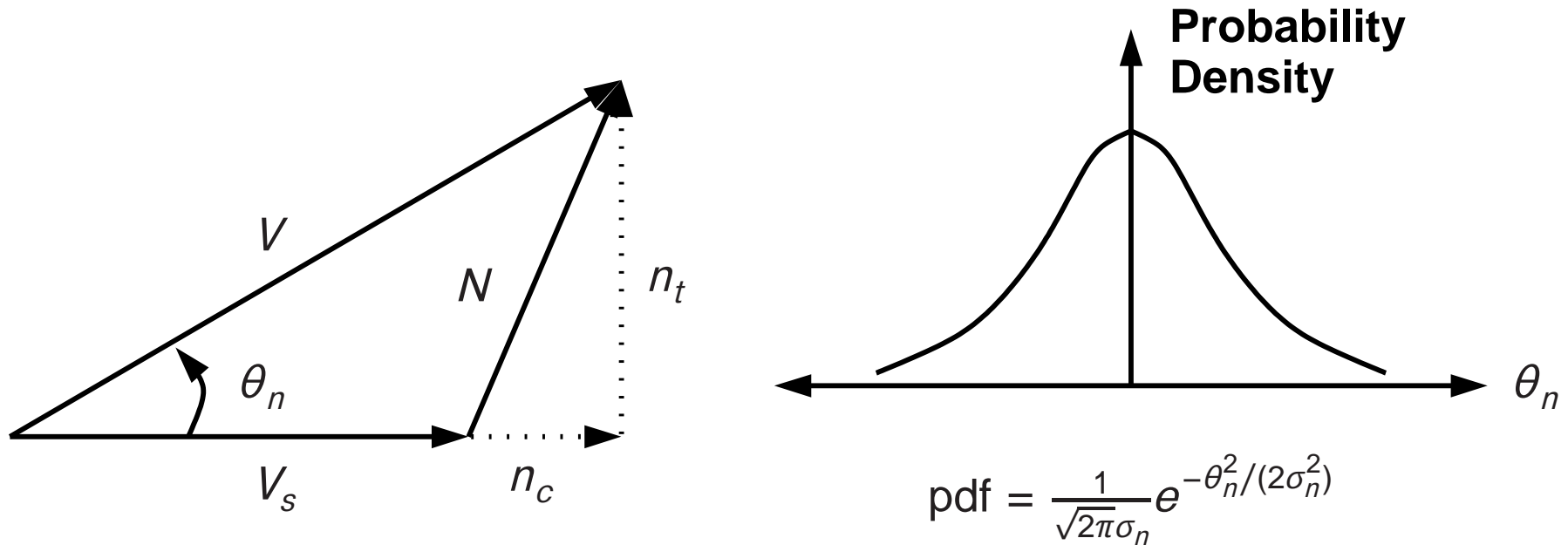
$$\text{Step Response} = 1 - \left( \frac{\zeta \omega_n}{\omega_d} \cdot \sin \omega_d t + \cos \omega_d t \right) e^{-\zeta \omega_n t} \quad \omega_d = \sqrt{1 - \zeta^2} \cdot \omega_n$$

$$\% \text{ Overshoot} = 100e^{-\pi / \sqrt{1/\zeta^2 - 1}}$$



- For PLL, choose  $\zeta > 1/\sqrt{2} = 0.707$  to avoid excessive ringing.

# Phase Jitter



$$v(t) = s(t) + n(t) = V_s \sin(2\pi f_o t) + n(t)$$
$$n(t) = n_c(t) \sin(2\pi f_o t) + n_t(t) \cos(2\pi f_o t)$$

The phase jitter is

$$\theta_n(t) = \tan \left[ \frac{n_t(t)}{V_s + n_c(t)} \right] \approx \frac{n_t(t)}{V_s}$$

# Phase Jitter

---

Assume that

$$\overline{n^2} = \frac{1}{2} \cdot \overline{n_c^2} + \frac{1}{2} \cdot \overline{n_t^2} \quad \overline{n_c^2} = \overline{n_t^2}$$

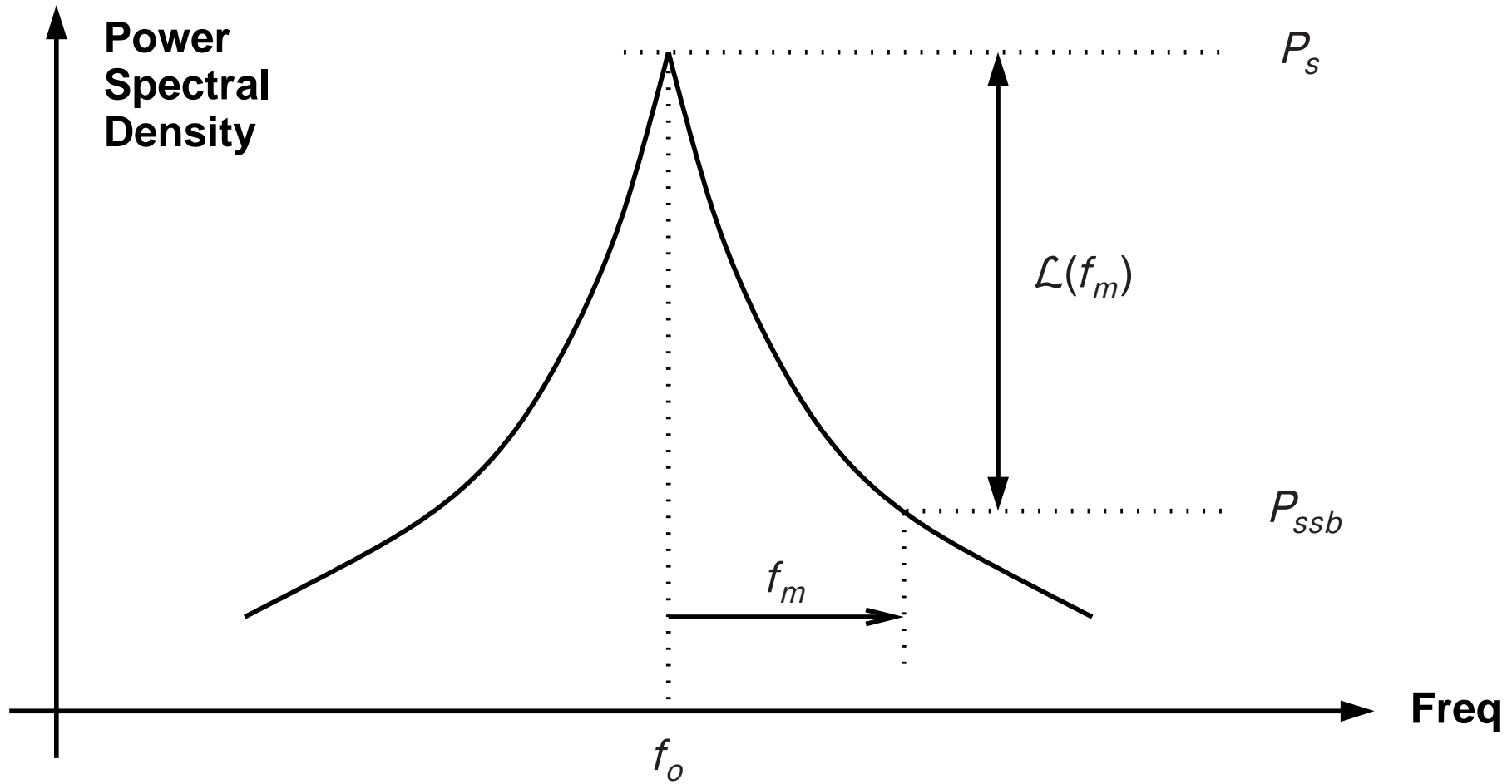
Then, we have

$$\sigma_n^2 = \overline{\theta_n^2} = \frac{\overline{n_t^2}}{V_s^2} = \frac{\overline{n^2}}{V_s^2} = \frac{1}{2} \cdot \frac{1}{\text{SNR}}$$

- SNR is the signal-to-noise ratio, and can be expressed as

$$\text{SNR} \equiv \frac{V_s^2/2}{\overline{n^2}}$$

# Phase Noise



$$v(t) = V_s \sin [2\pi f_0 t + \theta_n(t)]$$

# Phase Noise

---

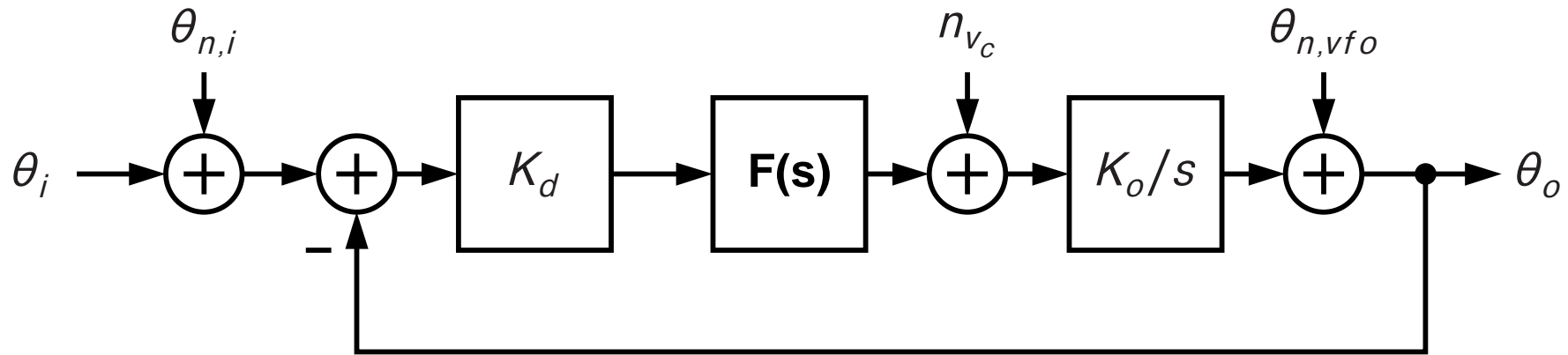
- The phase noise  $\mathcal{L}(f_m)$ , usually in dBc, is the ratio of the single-sideband (SSB) power in a 1-Hz bandwidth  $f_m$  Hz away from the carrier to the total signal power, i.e.,

$$\mathcal{L}(f_m) \equiv \frac{P_s}{P_{ssb}}$$

- Let  $S_{\theta_n}(f)$  be the power spectral density of  $\theta_n(t)$  in frequency domain, it can be shown that

$$S_{\theta_n}(f_m) \approx 2\mathcal{L}(f_m) \quad \text{and} \quad \overline{\theta_n^2} = \int_0^{\infty} S_{\theta_n}(f) df$$

# PLL Noise Response



Let  $\theta_{n,o}$  be the phase noise in  $\theta_o$ , we have

$$\frac{S_{\theta_{n,o}}}{S_{\theta_{n,i}}} = \left| \frac{K_o K_d F(s)}{s + K_o K_d F(s)} \right|_{s=j\omega}^2 = |H(j\omega)|^2$$

$$\frac{S_{\theta_{n,o}}}{S_{\theta_{n,vfo}}} = \left| \frac{s}{s + K_o K_d F(s)} \right|_{s=j\omega}^2 = |1 - H(j\omega)|^2$$

$$\frac{S_{\theta_{n,o}}}{S_{n_{vc}}} = \left| \frac{K_o}{s + K_o K_d F(s)} \right|_{s=j\omega}^2 = \left| [1 - H(j\omega)] \cdot \frac{K_o}{j\omega} \right|^2$$

# PLL Noise Response

---

Consider only a white noise  $S_{\theta_{n,i}}(f)$  in  $\theta_i$ ,

$$\overline{\theta_{n,o}^2} = \int_0^{\infty} S_{\theta_{n,i}}(f) |H(j2\pi f)|^2 df = S_{\theta_{n,i}}(f) \times B_L$$

$B_L$  is the noise bandwidth of  $H(j2\pi f)$ , i.e.,

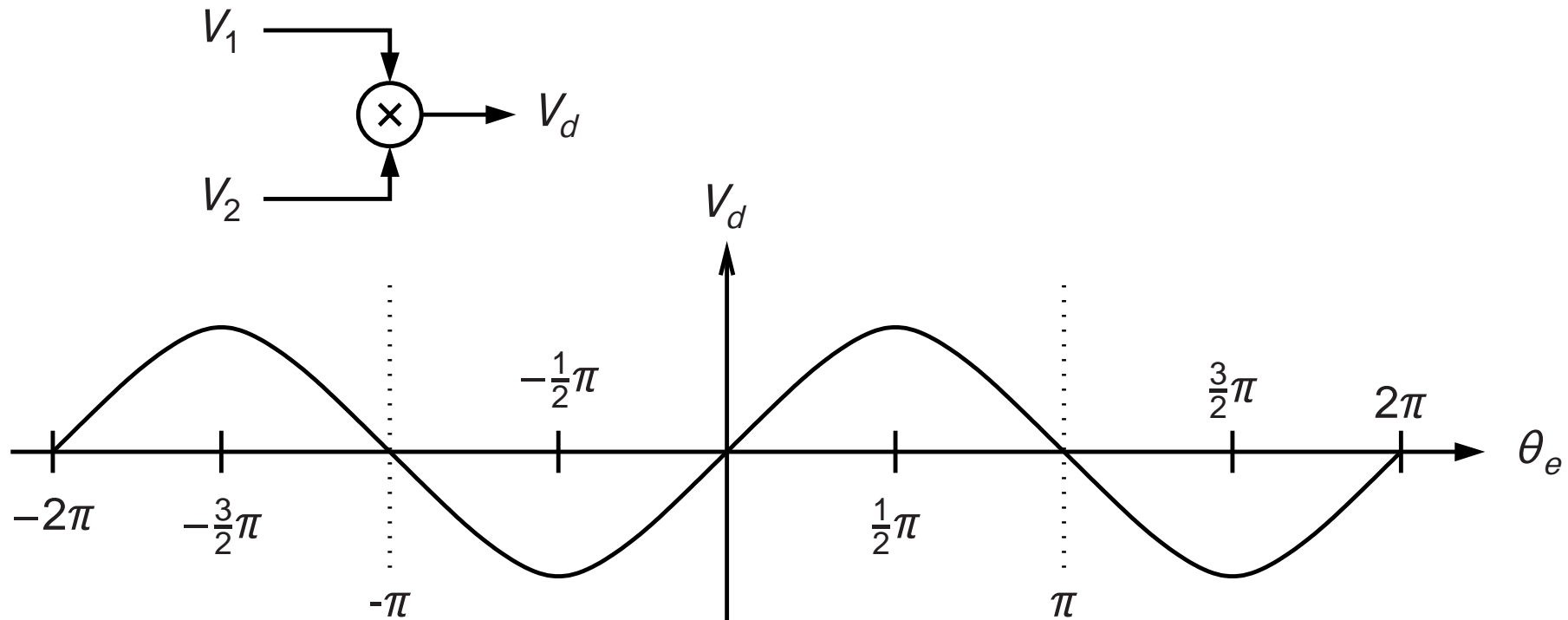
$$B_L \equiv \int_0^{\infty} |H(j2\pi f)|^2 df$$

For the 2nd-order PLL with active lag-lead filter

$$B_L = \frac{1}{2} \omega_n \left( \zeta + \frac{1}{4\zeta} \right)$$

- $B_{L,min}$  occurs at  $\zeta = 0.5$ .
- $B_L < 1.25B_{L,min}$  for  $0.25 < \zeta < 1.0$ .

# Phase Detection Using Analog Multiplier



$$V_1(t) = V_1 \sin(\omega t + \theta_1) \quad V_2(t) = V_2 \cos(\omega t + \theta_2)$$

$$V_d(t) = kV_1(t)V_2(t) = \frac{1}{2}kV_1V_2 [\sin(\theta_1 - \theta_2) + \sin(2\omega t + \theta_1 + \theta_2)]$$

# Phase Detection Using Analog Multiplier

---

The  $2\omega$  component will be filtered out by the loop filter, hence consider the dc component only

$$V_d = \frac{1}{2}kV_1V_2 \sin(\theta_1 - \theta_2) = K_d \cdot \sin(\theta_e) \quad \theta_e = \theta_1 - \theta_2$$

- $K_d$  is the phase-detector gain factor, and  $\theta_e$  is the phase error.
- If  $\theta_e \ll 1$ ,  $v_d \approx K_d\theta_e$ .
- $V_1(t)$  and  $V_2(t)$  are  $90^\circ$  out of phase when  $\theta_e = 0$ .

# PLL Tracking Performance — Hold-In Range

---

From the final value theorem

$$\lim_{t \rightarrow \infty} \theta_e(t) = \lim_{s \rightarrow 0} s\theta_e(s) = \lim_{s \rightarrow 0} \frac{s^2 \theta_i(s)}{s + K_o K_d F(s)}$$

The *hold-in range*,  $\Delta\omega_H$ , is the frequency range in which a PLL can maintain lock *statically*.

$$\omega_i = \omega_o + \Delta\omega_H \quad \theta_i(t) = \Delta\omega_H \cdot t \quad \theta_i(s) = \Delta\omega_H / s^2 \quad \Rightarrow \quad \lim_{t \rightarrow \infty} \theta_e(t) = \frac{\Delta\omega_H}{K_o K_d F(0)}$$

- For a sinusoidal PD, the criterion becomes

$$\lim_{t \rightarrow \infty} \sin \theta_e(t) = \frac{\Delta\omega_H}{K_o K_d F(0)} < 1 \quad \Rightarrow \quad \Delta\omega_H = K_o K_d F(0)$$

For a 2nd-order PLL with active filter,  $F(0) \rightarrow \infty$ , thus  $\Delta\omega_H \rightarrow \infty$ .

## PLL Tracking Performance — Pull-Out Range

---

The *pull-out range*  $\Delta\omega_{PO}$  is the frequency-step limit below which the PLL does not skip cycles but remains in lock.

- For a sinusoidal PD

$$\Delta\omega_{PO} = 1.8\omega_n(\zeta + 1) \quad \text{for} \quad 0.5 < \zeta < 1.4$$

# Noisy PLL Tracking Performance

---

Define the SNR of a PLL as

$$\text{SNR}_L \equiv \frac{1}{2\theta_{n,o}^2}$$

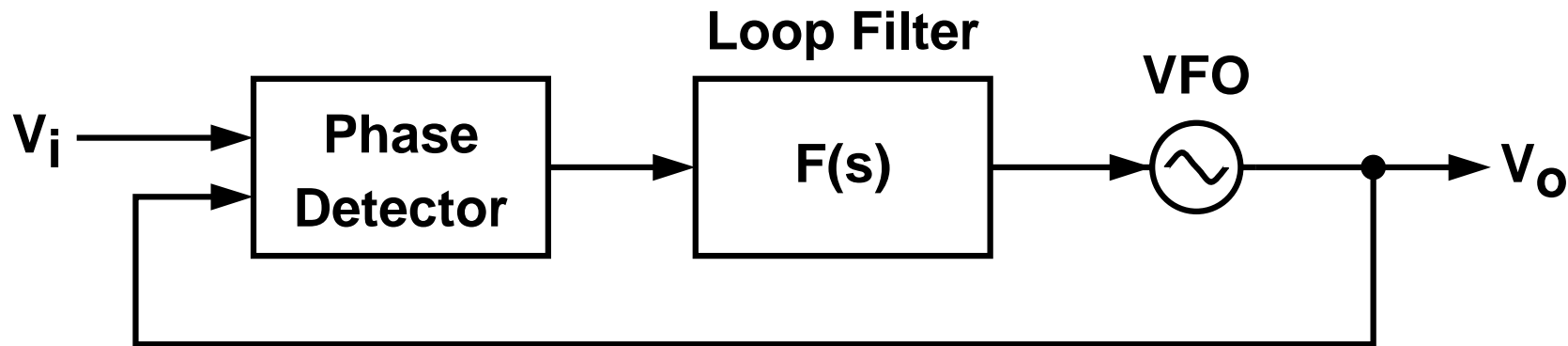
- As a rule of thumb,  $\text{SNR}_L > 6$  dB is required for stable operation.

For low  $\text{SNR}_L$ , the VFO phase occasionally slips one or more cycles as compared to the input. Define  $T_{AV}$  as the average time between cycle slips.

- For a 1st-order loop  $T_{AV} \approx \frac{\pi}{4B_L} e^{4\text{SNR}_L}$ , where  $B_L$  is the PLL noise bandwidth.
- For a 2nd-order loop with  $\zeta = 0.707$   $T_{AV} \approx \frac{1}{B_L} e^{\pi\text{SNR}_L}$ .
- The slips of a 1st-order loop are almost always single, isolated events.
- The slips in a 2nd-order loop tend to bunch in bursts.

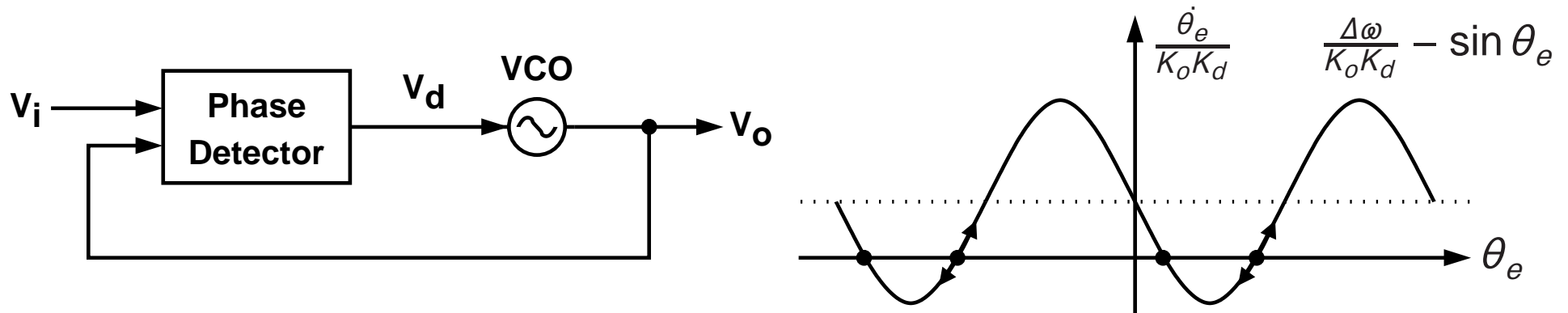
# PLL Acquisition Behavior

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- The process of bringing a PLL into lock is called *acquisition*.
- Acquisition is inherently a nonlinear phenomenon.
- An  $n$ th-order PLL contains  $n$  integrators (VFO, capacitors, ...). With each integrator there is associated a state variable of the loop: phase, frequency, frequency rate, and so on. To force the loop into lock, it is necessary to bring each of the state variables close to the corresponding parameters of the input signal. Therefore, we should speak of phase acquisition, frequency acquisition, and so forth.

# Phase Acquisition of a First-Order Loop



$$V_d = K_d \cdot \sin \theta_e$$

$$\omega_o = \omega_{oo} + K_o \cdot V_d$$

$$\theta_e = \theta_i - \theta_o$$

$$\theta_e = \theta_i - \theta_o = \omega_i t - \omega_{oo} t - \int_0^t K_o K_d \sin \theta_e dt - \theta_o(0)$$

$$\Rightarrow \frac{d\theta_e}{dt} = \dot{\theta}_e = \Delta\omega - K_o K_d \sin \theta_e \quad \Delta\omega = \omega_i - \omega_{oo}$$

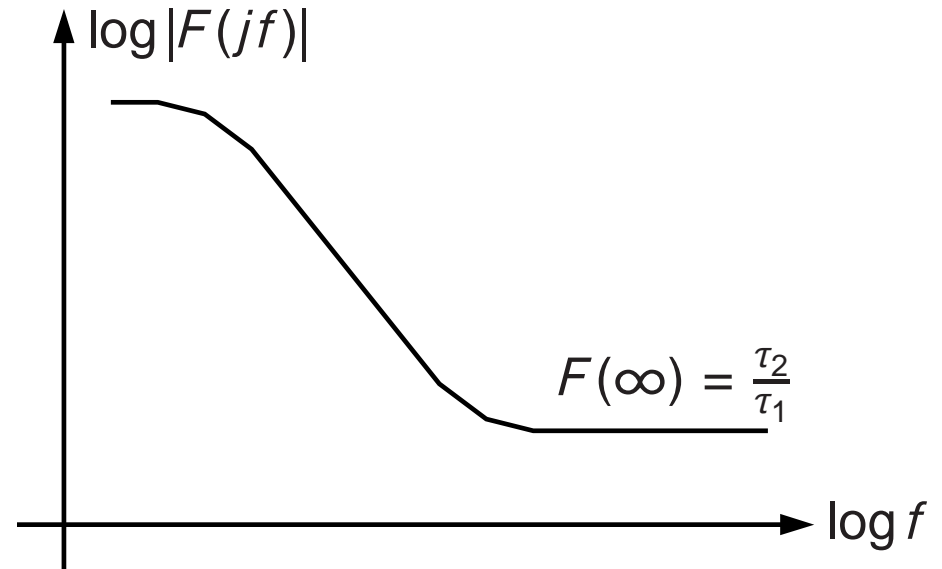
- The loop is locked when  $\dot{\theta}_e = 0$ .
- There is no cycle skipping in the acquisition process.

# Phase Acquisition of a Second-Order Loop

---

The *lock-in range*,  $\Delta\omega_L$ , is the frequency range over which the PLL can acquire lock without cycle slipping.

By practical considerations, the lock-in process of a higher-order loop is so fast that it can be approximated by the phase acquisition process of a 1st-order loop with gain  $K = K_o K_d F(\infty)$ .

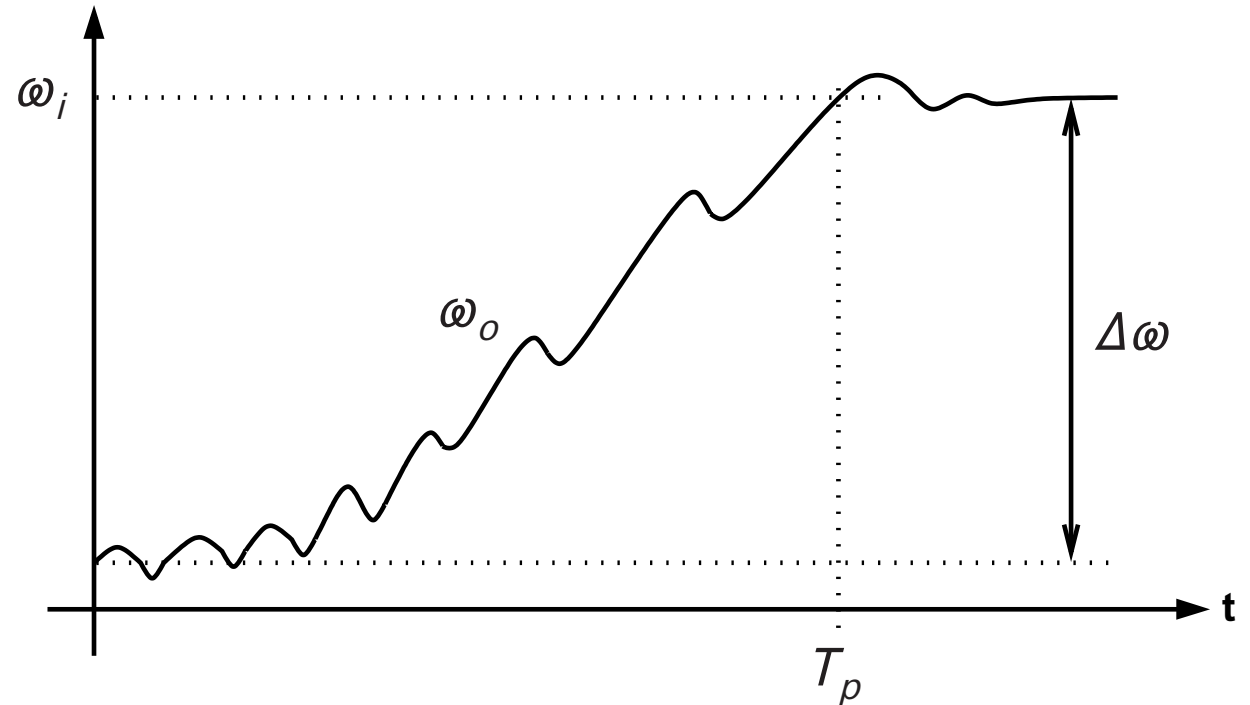


- For a PLL with sinusoidal PD,

$$\text{Lock-In Range} = \Delta\omega_L \approx K_o K_d F(\infty) = 2\zeta\omega_n \quad \text{Lock-In Time} = T_L \approx \frac{1}{\omega_n}$$

# Frequency Acquisition — The Pull-In Process

The *pull-in range*,  $\Delta\omega_p$ , is the maximum initial frequency offset for the pull-in process to occur.

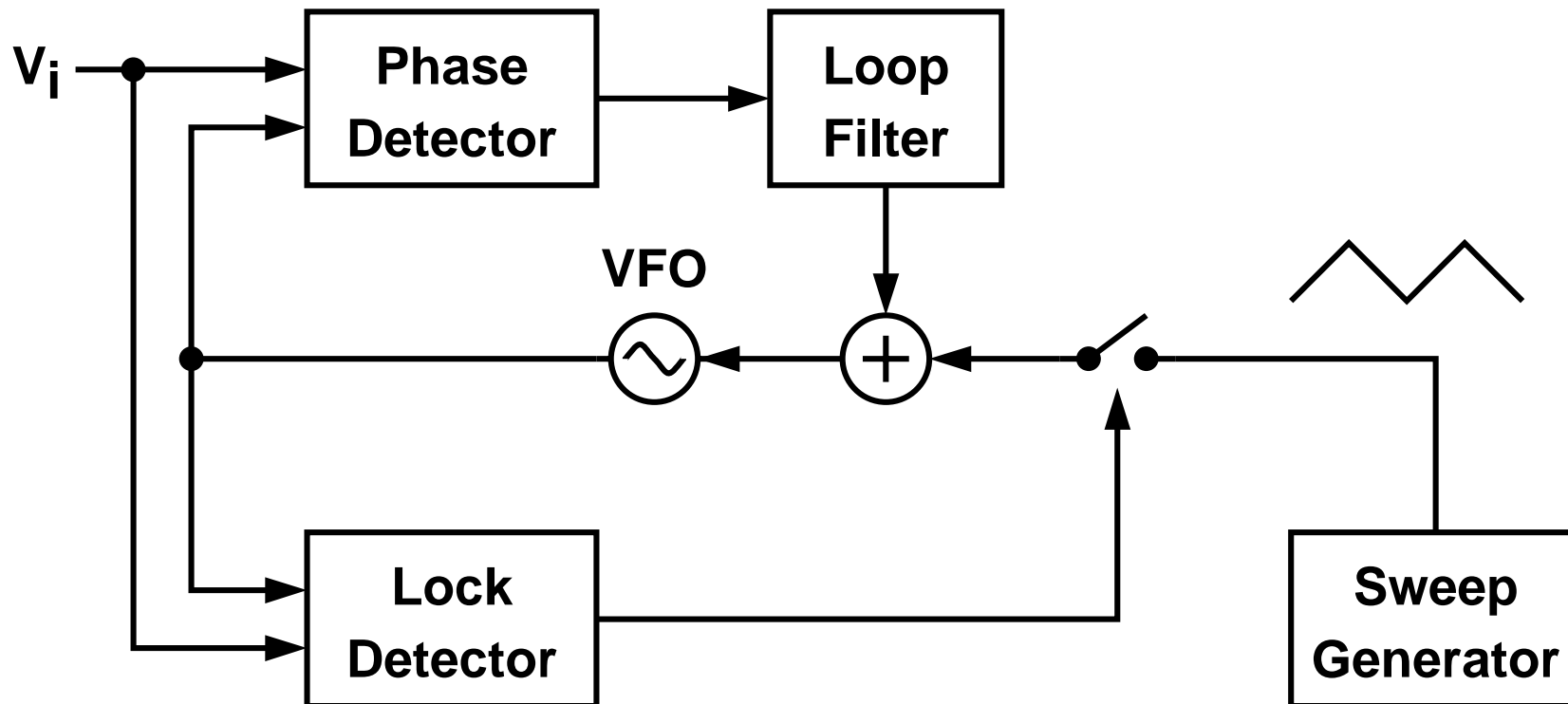


- For a 2nd-order PLL,

$$\text{Pull-In Range} = \Delta\omega_p \approx \frac{8}{\pi} \sqrt{\zeta \omega_n K_o K_d - \omega_n^2} \approx \frac{8}{\pi} \sqrt{\zeta \omega_n K_o K_d} \quad \text{if } K_o K_d \gg \omega_n$$

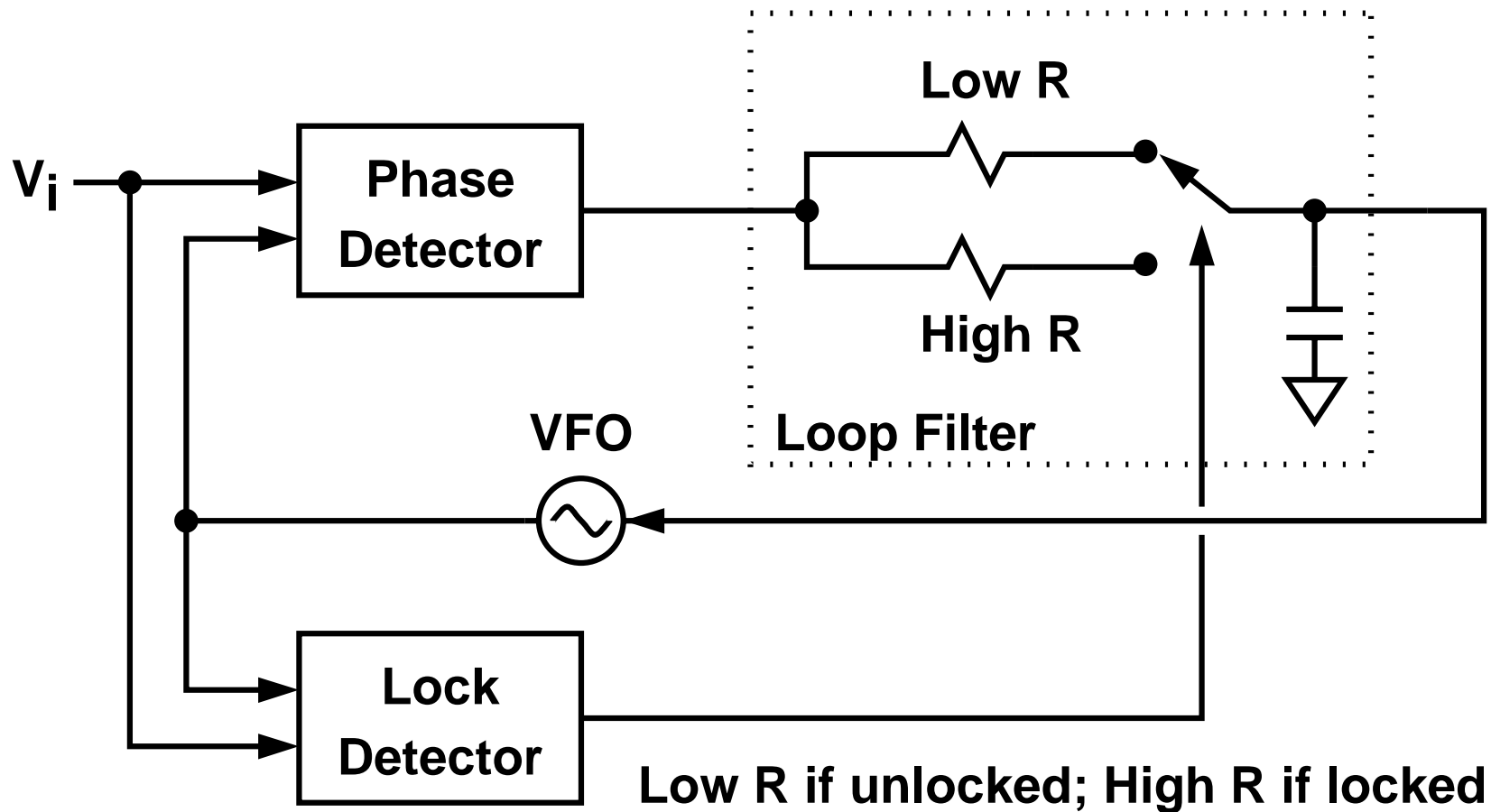
$$\text{Pull-In Time} = T_p \approx \frac{\Delta\omega^2}{2\zeta \omega_n^3}$$

# Aided Frequency Acquisition — Frequency Sweeping



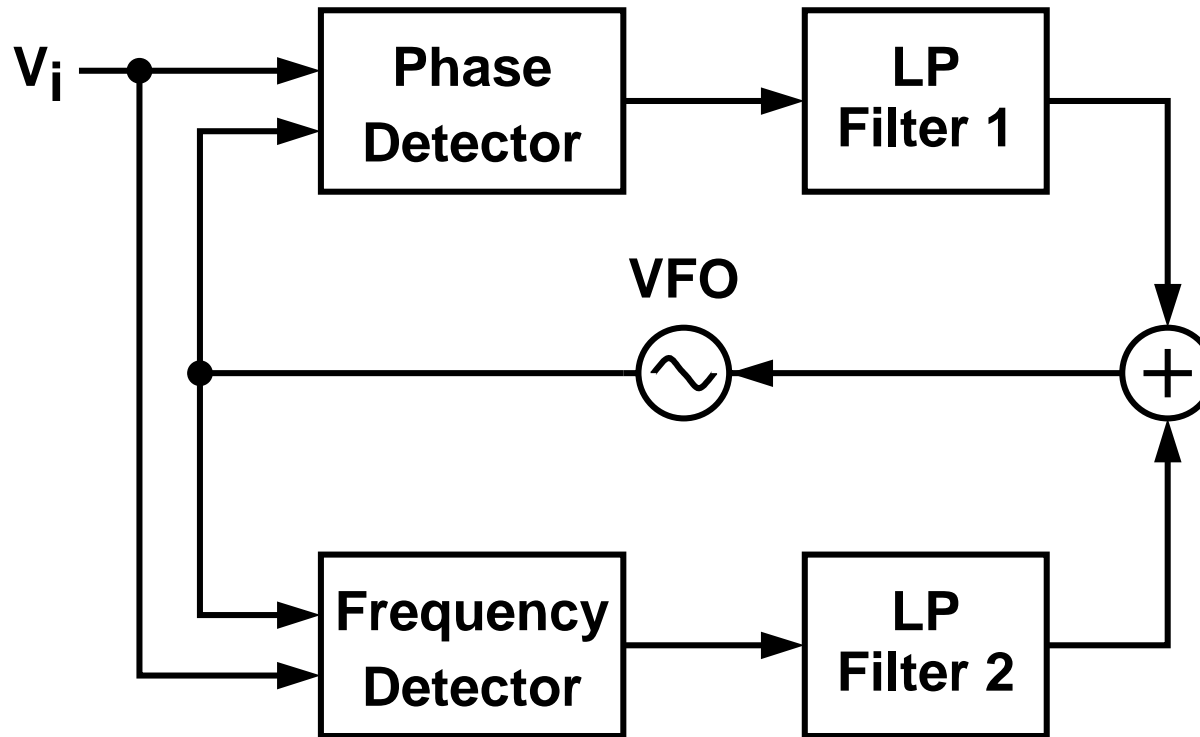
- Use sweep to bring the VFO close to the frequency of locking.

# Aided Frequency Acquisition — Loop Filter Switching



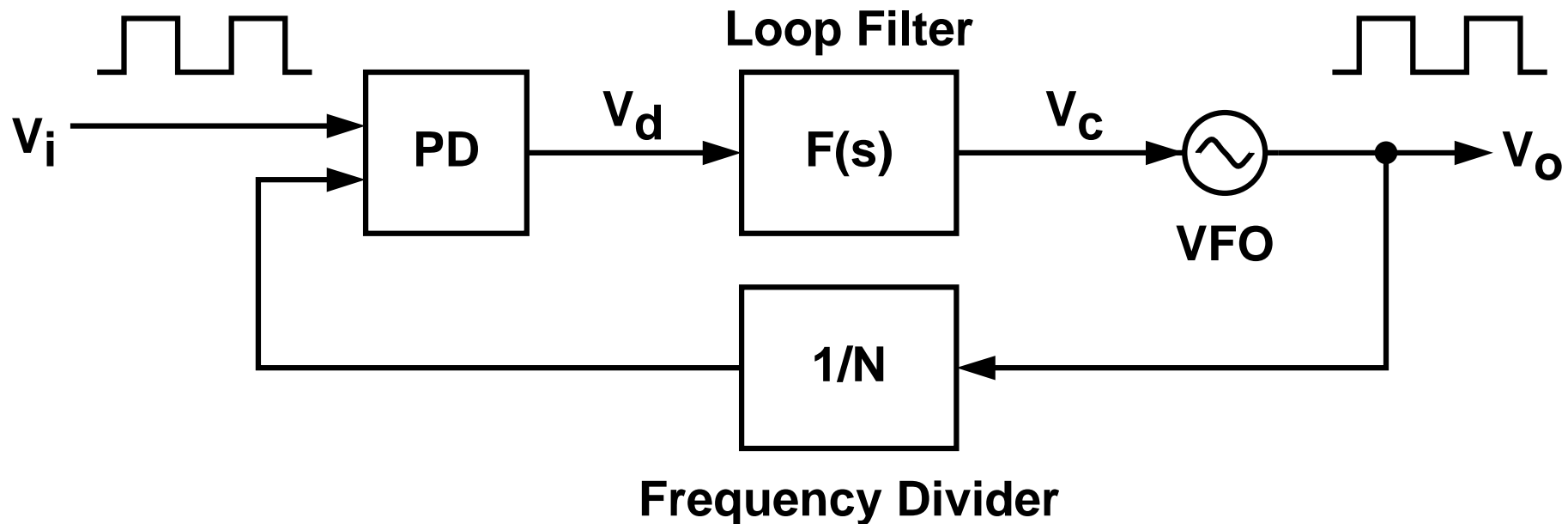
- The frequency pull-in can be painfully slow in a narrowband loop. Sometimes, a wider loop bandwidth is preferred.

# Aided Frequency Acquisition — Dual Loops



- Contains a phase-locked loop (PLL) and a frequency-locked loop (FLL).
- The FLL should dominate during frequency acquisition.
- The PLL should be dominant when the phase is locked.

# Digital Phase-Locked Loops (DPLLs)



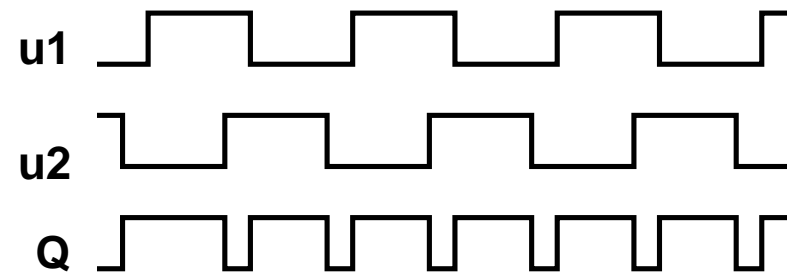
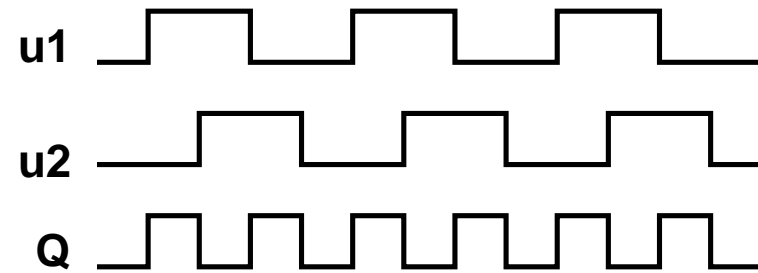
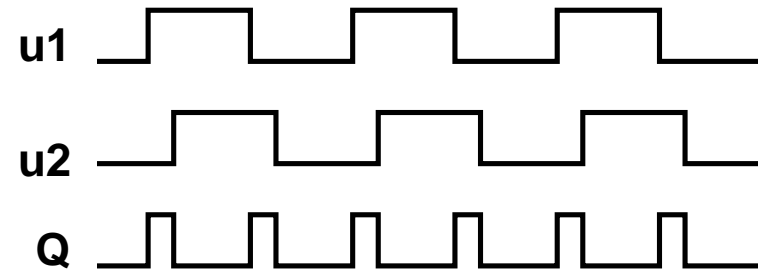
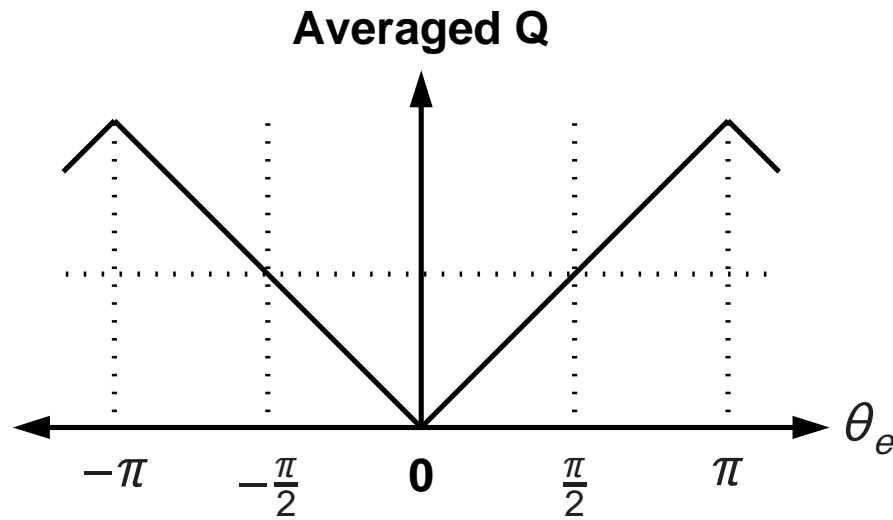
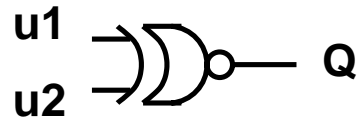
To calculate loop dynamics, combine the VFO and the frequency divider as a new VFO.

$$\omega_o = \omega_{oo} + K_o \cdot V_d \quad \Rightarrow \quad \omega'_o = \frac{\omega}{N} = \frac{\omega_{oo}}{N} + \frac{K_o}{N} \cdot V_d = \omega'_{oo} + K'_o \cdot V_d$$

$$\omega'_{oo} = \frac{\omega_{oo}}{N} \quad K'_o = \frac{K_o}{N} \quad \theta'_o = \frac{\theta_o}{N}$$

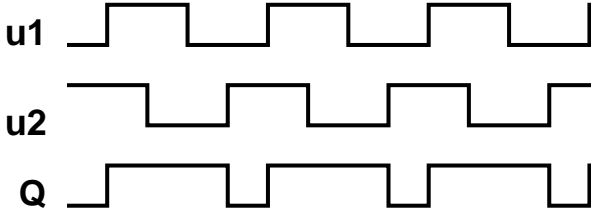
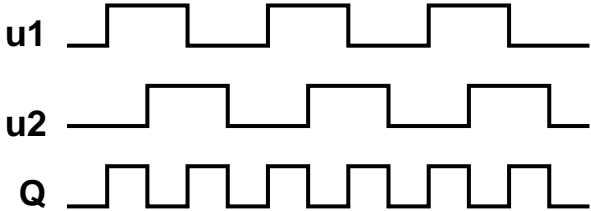
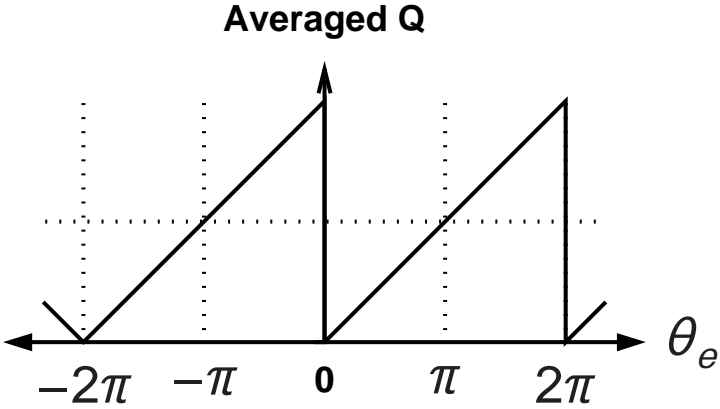
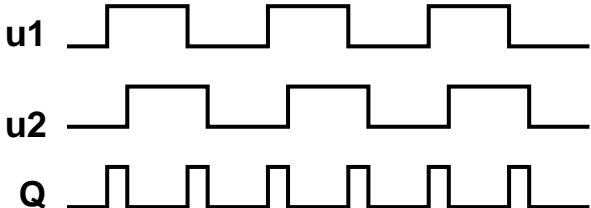
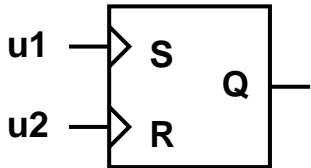
- $\theta_i$  and  $\theta_o$  are not available except during the rising and falling transitions.

# XOR Phase Detector

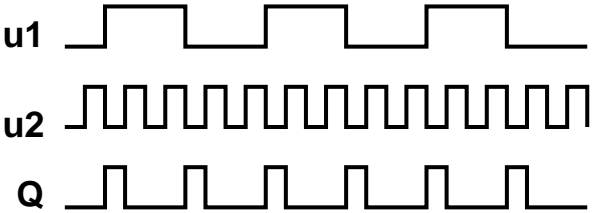
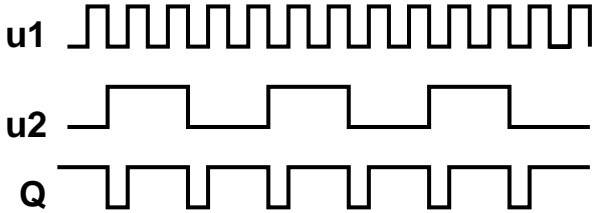


- The PD characteristic is strongly dependent on the duty-cycle of  $u_1$  and  $u_2$ .

# Edge-Triggered Set-Reset Phase Detector



## Frequency Discrimination Capability

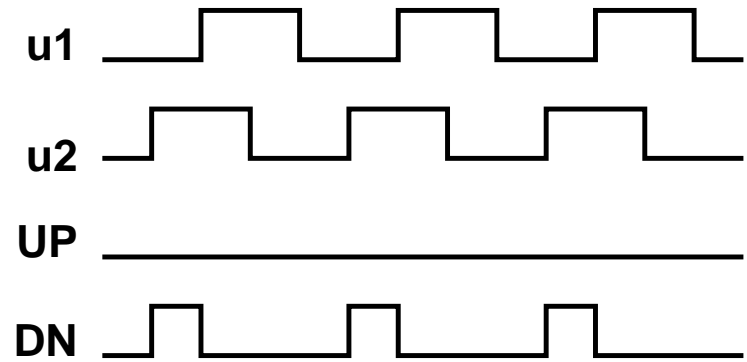
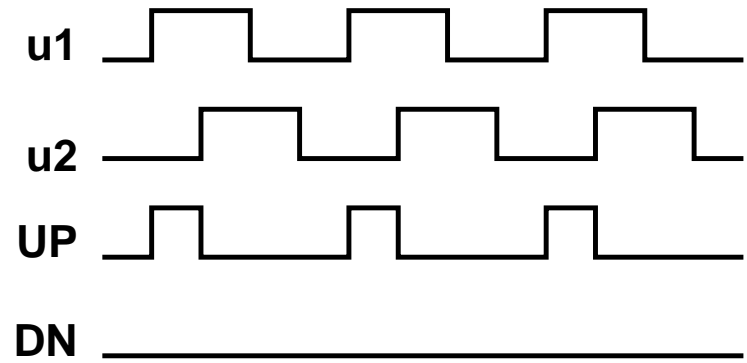
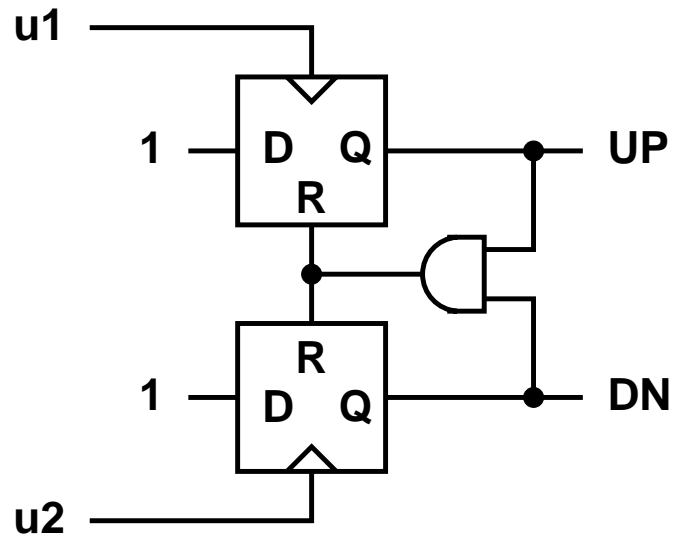


# Edge-Triggered Set-Reset Phase Detector

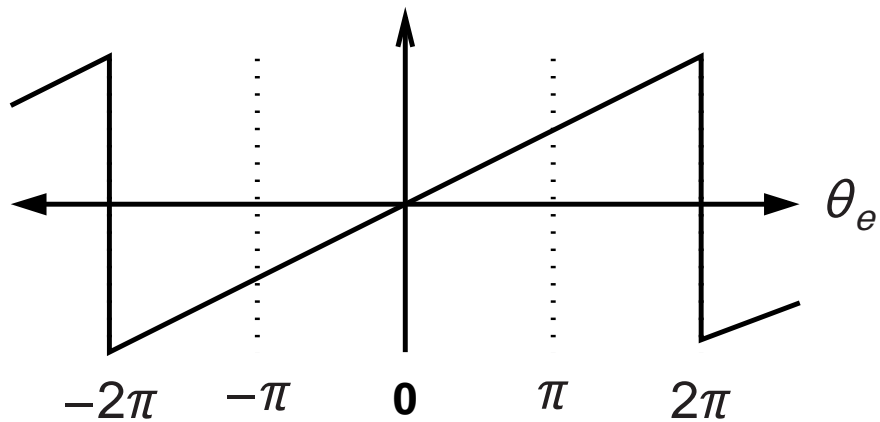
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- The PD is edge-sensitive, the duty-cycle of  $u_1$  and  $u_2$  is irrelevant.
- If  $f_1 \gg f_2$  or  $f_1 \ll f_2$ , the PD has frequency discrimination capability, which can improve frequency acquisition speed of the PLL.
- However, when  $f_1 \approx f_2$ , the frequency-sensitive behavior is lost, and the PLL relies on the pull-in process for frequency acquisition.

# Sequential Phase-Frequency Detector (PFD)



Averaged (UP-DW)

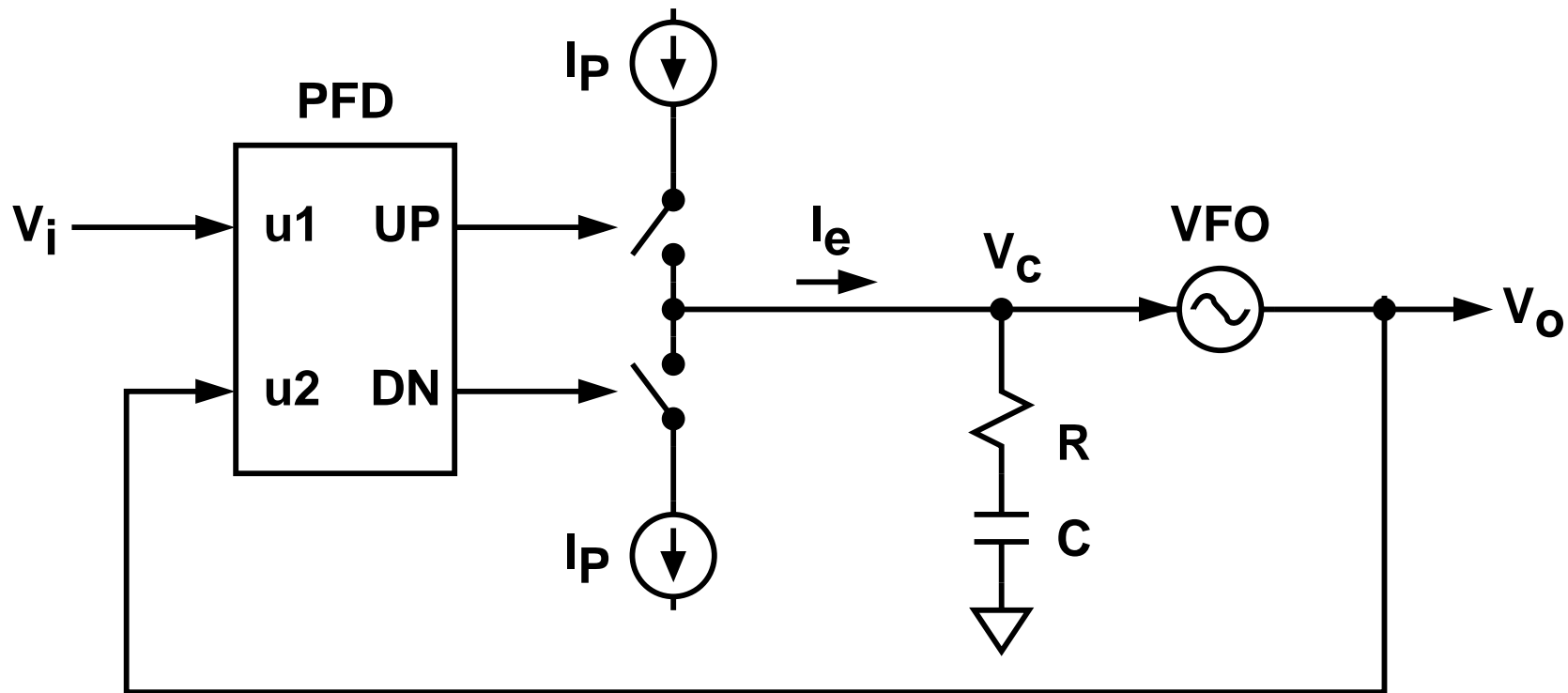


# Sequential Phase-Frequency Detector (PFD)

---

- The PFD is edge-sensitive, the duty-cycle of  $u_1$  and  $u_2$  is irrelevant.
- The PFD can discriminate the frequency difference for even the smallest  $f_1 - f_2$ .
- A PLL with the PFD can have infinite pull-in range. The frequency acquisition aid provided by the PFD is akin to frequency sweeping.
- When using the PFD, a missing transition or an extra one in either  $u_1$  or  $u_2$  can cause a large error signal to appear. The effects will propagate for more than one cycle. Great caution is required to use the PFD in a noisy environment.

# Charge-Pump Phase-Locked Loops



The “on” time of either UP or DN is  $t_p = |\theta_e|/\omega_i$  for each period  $1/f_i$  of the input signal. The average error current  $I_e$  over a cycle is

$$I_e = I_P \times \frac{t_p}{T_i} = I_P \times \frac{\theta_e}{2\pi} \qquad \omega_i = 2\pi f_i = \frac{2\pi}{T_i}$$

# Charge-Pump Phase-Locked Loops

---

The voltage  $V_c$  can be expressed as

$$V_c(s) = I_e(s) \left( R + \frac{1}{sC} \right) = \theta_e(s) \times \frac{I_P}{2\pi} \left( R + \frac{1}{sC} \right)$$
$$\frac{V_c(s)}{\theta_e(s)} = K_d F(s) = \frac{I_P}{2\pi} \left( R + \frac{1}{sC} \right)$$

The VFO has the following characteristic:

$$\omega_o = \omega_{oo} + K_o \cdot V_c \quad \Leftrightarrow \quad f_o = f_{oo} + K'_o \cdot V_c \quad K'_o = \frac{K_o}{2\pi}$$

Using the continuous-time approximation, we have

$$\frac{\theta_e(s)}{\theta_i(s)} = H_e(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad \frac{\theta_o(s)}{\theta_i(s)} = H(s) = 1 - H_e(s)$$

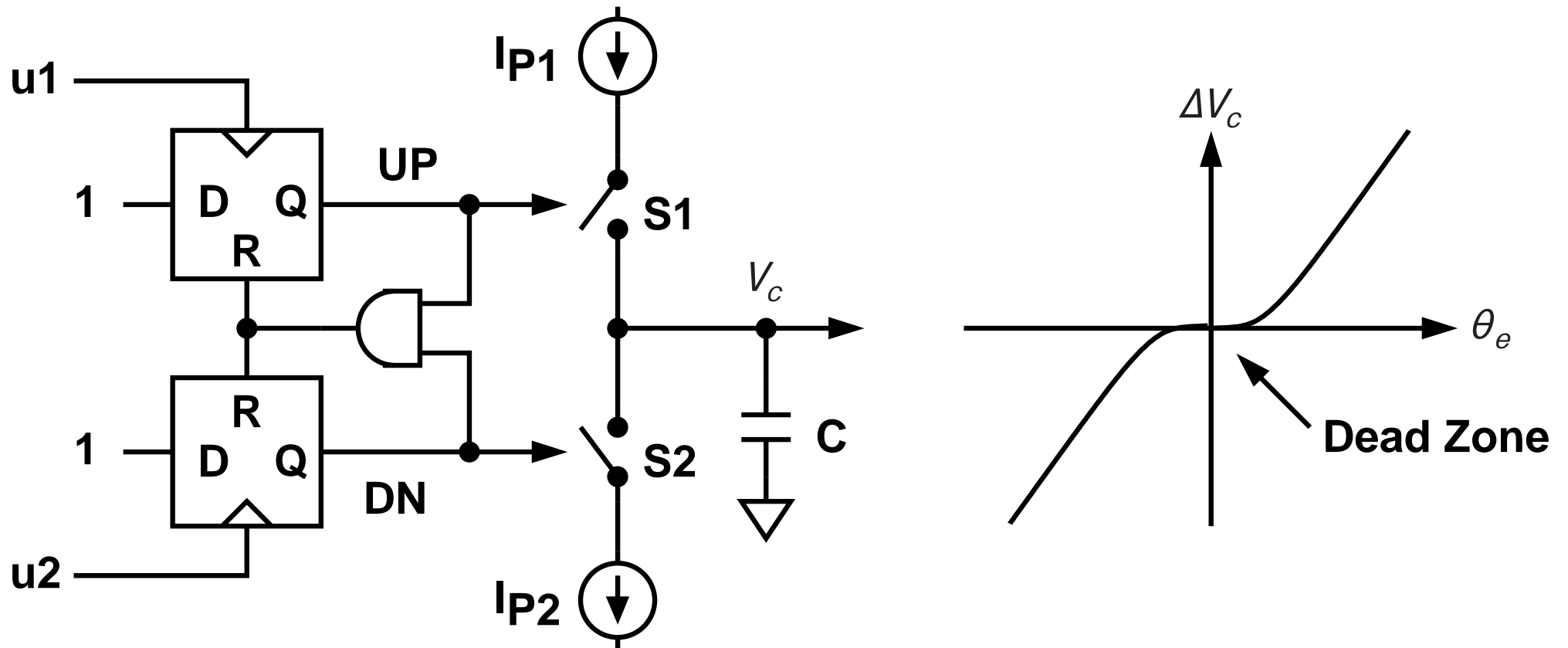
$$\omega_n = \left( K'_o \times \frac{I_P}{C} \right)^{1/2} \quad \zeta = \frac{1}{2} [K'_o \times (I_P R) \times (RC)]^{1/2}$$

# Charge-Pump Phase-Locked Loops

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- The PLL behaves as a 2nd-order loop with active lag-lead filter.
- Discrete-time model can be used for more accurate analysis. Reference: Hein, *z-Domain Model for Discrete-Time PLLs*, Trans. CAS, 11/88, pp. 1393–1400.
- During the pump interval  $t_p$ , a voltage step of  $I_p R$  occurs at the VFO input. This granularity effect may be intolerable in some systems.
- The voltage step  $I_p R$  may overload the VFO, making the previous linear analysis invalid.
- The granularity effect can be mitigated with an additional capacitor  $C_p$  in parallel with the earlier  $RC$  network, thus forming a 3rd-order PLL.
- Reference: Floyd Gardner, “Charge-Pump Phase-Lock Loops,” IEEE Trans. Commun., Nov. 1980, pp. 1849–1858.

# PFD and Charge-Pump Filter



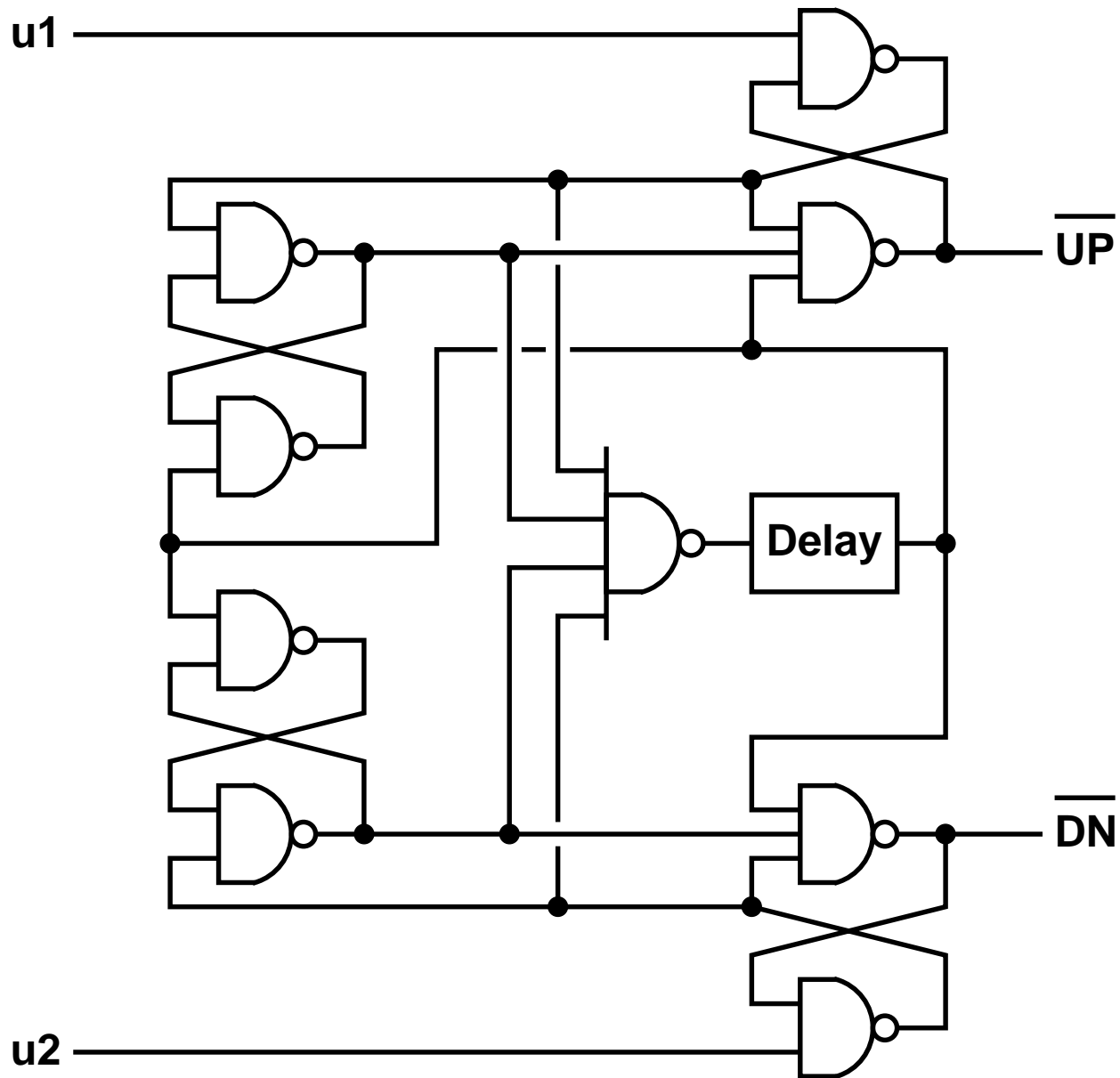
- The dead zone is caused by the slowness of the  $S1$  and  $S2$  switches.

# PFD and Charge-Pump Filter

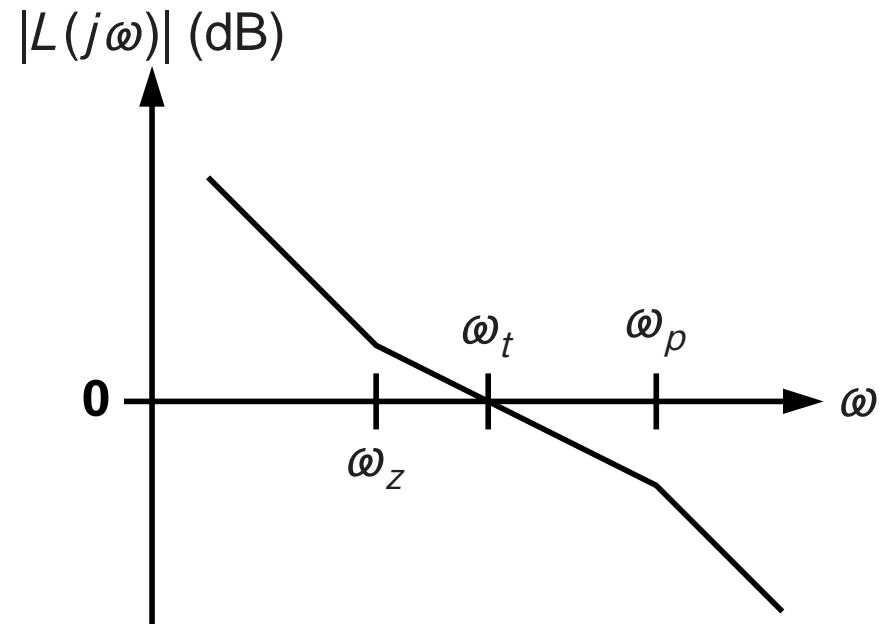
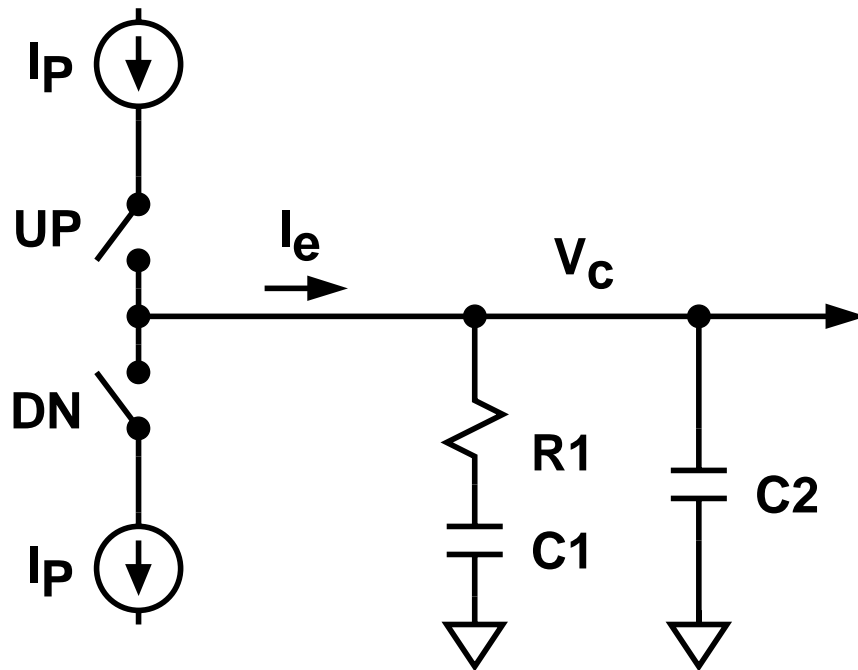
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- When  $\theta_e$  falls in the dead zone, the PFD's conversion gain is decreased, causing a reduction in  $\omega_n$  and  $\zeta$ , and the degradation of  $\theta_o$  phase noise.
- The dead zone can be eliminated by allowing UP and DN to be activated simultaneously for a short time even if the phase difference is zero. Then, any mismatch between  $I_{P1}$  and  $I_{P2}$  can cause a phase offset and consequently spurs in the output spectrum.
- The finite output impedance of the  $I_{P1}$  and  $I_{P2}$  current sources can also cause phase offset.
- Charge sharing in the S1 and S2 switches can also cause glitches at  $V_c$ .

# PFD with Delayed Reset



# Third-Order Charge-Pump PLLs



The loop filter transfer function is

$$\frac{V_c(s)}{\theta_e(s)} = K_d F(s) = \frac{I_p}{2\pi} \left[ \left( R_1 + \frac{1}{sC_1} \right) \parallel \frac{1}{sC_2} \right] = \frac{I_p}{2\pi s(C_1 + C_2)} \times \frac{sR_1C_1 + 1}{sR_1(C_1 \parallel C_2) + 1}$$

$$\omega_z = \frac{1}{R_1C_1} \quad \omega_p = \frac{1}{R_1(C_1 \parallel C_2)}$$

## Third-Order Charge-Pump PLLs

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The loop gain of the 3-order PLL is

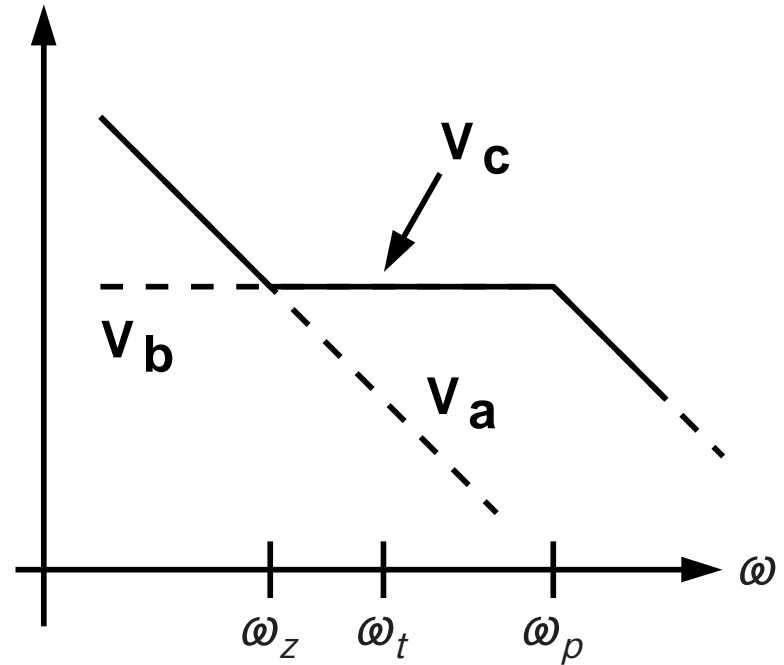
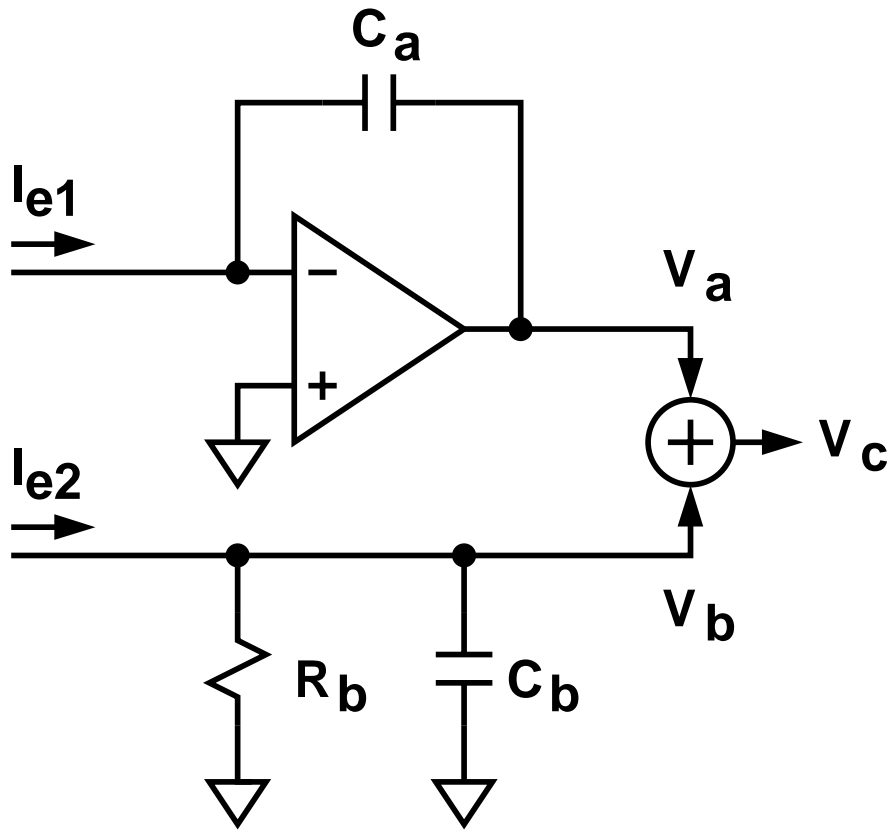
$$L(s) = \frac{K_o}{s} \times K_d F(s) = \frac{K'_o I_P}{s^2(C_1 + C_2)} \times \frac{s/\omega_z + 1}{s/\omega_p + 1}$$

Let  $\omega_t/\omega_z = \alpha > 1$  and  $\omega_p/\omega_t = \beta > 1$ , then

$$\omega_t \approx \frac{K'_o I_P}{(C_1 + C_2)\omega_z} = K'_o \cdot I_P R_1 \cdot \frac{C_1}{C_1 + C_2}$$
$$R_1 = \frac{1}{K'_o I_P} \cdot \omega_t \quad C_1 = K'_o I_P \cdot \frac{\alpha}{\omega_t^2} \quad C_2 = K'_o I_P \cdot \frac{1}{\beta \cdot \omega_t^2}$$

- $\alpha = 4$  and  $\beta = 4$  gives a phase margin  $\approx 60^\circ$ .

# Multi-Path Charge-Pump Filter



$$I_{e1} = I_{P1} \times \frac{\theta_e}{2\pi}$$

$$I_{e2} = I_{P2} \times \frac{\theta_e}{2\pi}$$

# Multi-Path Charge-Pump Filter

---

The loop filter transfer function is

$$\frac{V_c(s)}{\theta_e(s)} = K_d F(s) = \frac{I_{P1}}{2\pi} \cdot \frac{1}{C_a} + \frac{I_{P2}}{2\pi} \left( R_b \parallel \frac{1}{sC_b} \right) = \frac{I_{P1}}{2\pi s C_a} \times \frac{sR_b \left( C_b + C_a \cdot \frac{I_{P2}}{I_{P1}} \right) + 1}{sR_b C_b + 1}$$
$$\frac{1}{\omega_z} = R_b \left( C_b + C_a \cdot \frac{I_{P2}}{I_{P1}} \right) \approx R_b C_a \cdot \frac{I_{P2}}{I_{P1}} \qquad \frac{1}{\omega_p} = R_b C_b$$

The loop's unity-gain frequency is

$$\omega_t \approx \frac{K'_o I_{P1}}{C_a \omega_z} = K'_o \cdot I_{P2} R_b$$

- $\omega_z$ ,  $\omega_p$ , and  $\omega_t$ , can be set using smaller capacitors and resistors.
- Reference: J. Craninckx and M. Steyaert, *A Fully Integrated CMOS DCS-1800 Frequency Synthesizer*, JSSC, 12/98, pp. 2054–2065.