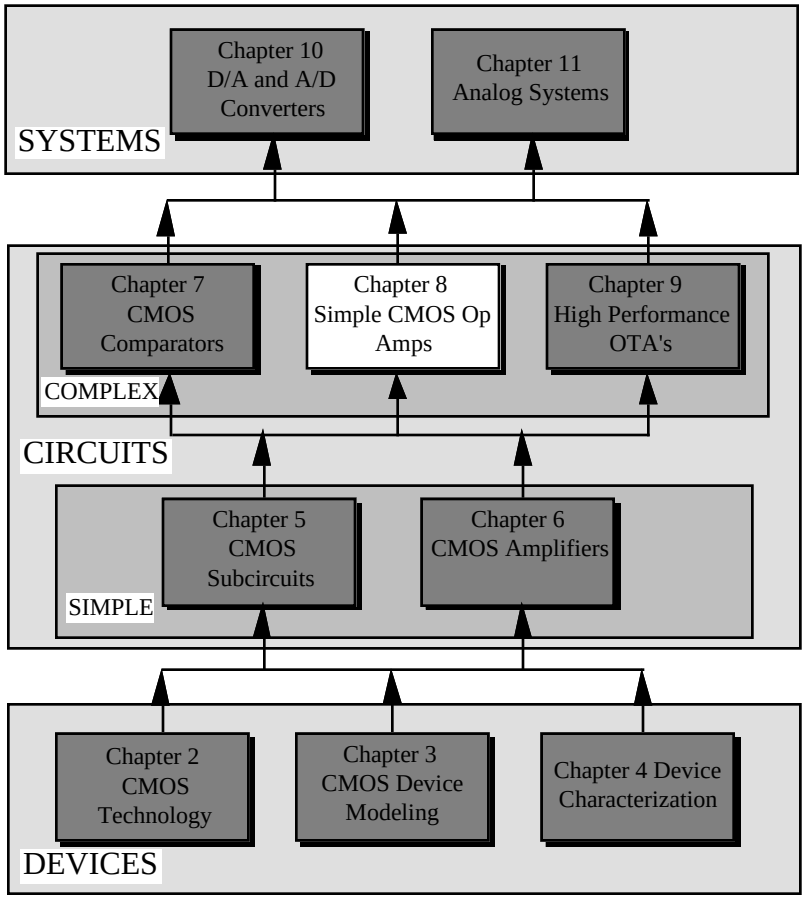
VIII. SIMPLE CMOS OPERATIONAL AMPLIFIERS (OP AMPS) AND OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS (OTA'S)

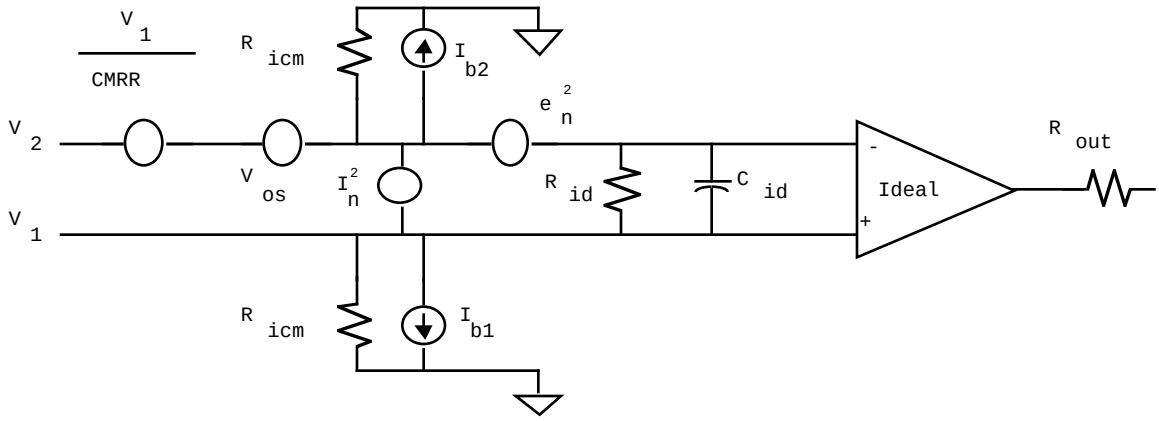
Contents

Organization



Op Amp Characteristics

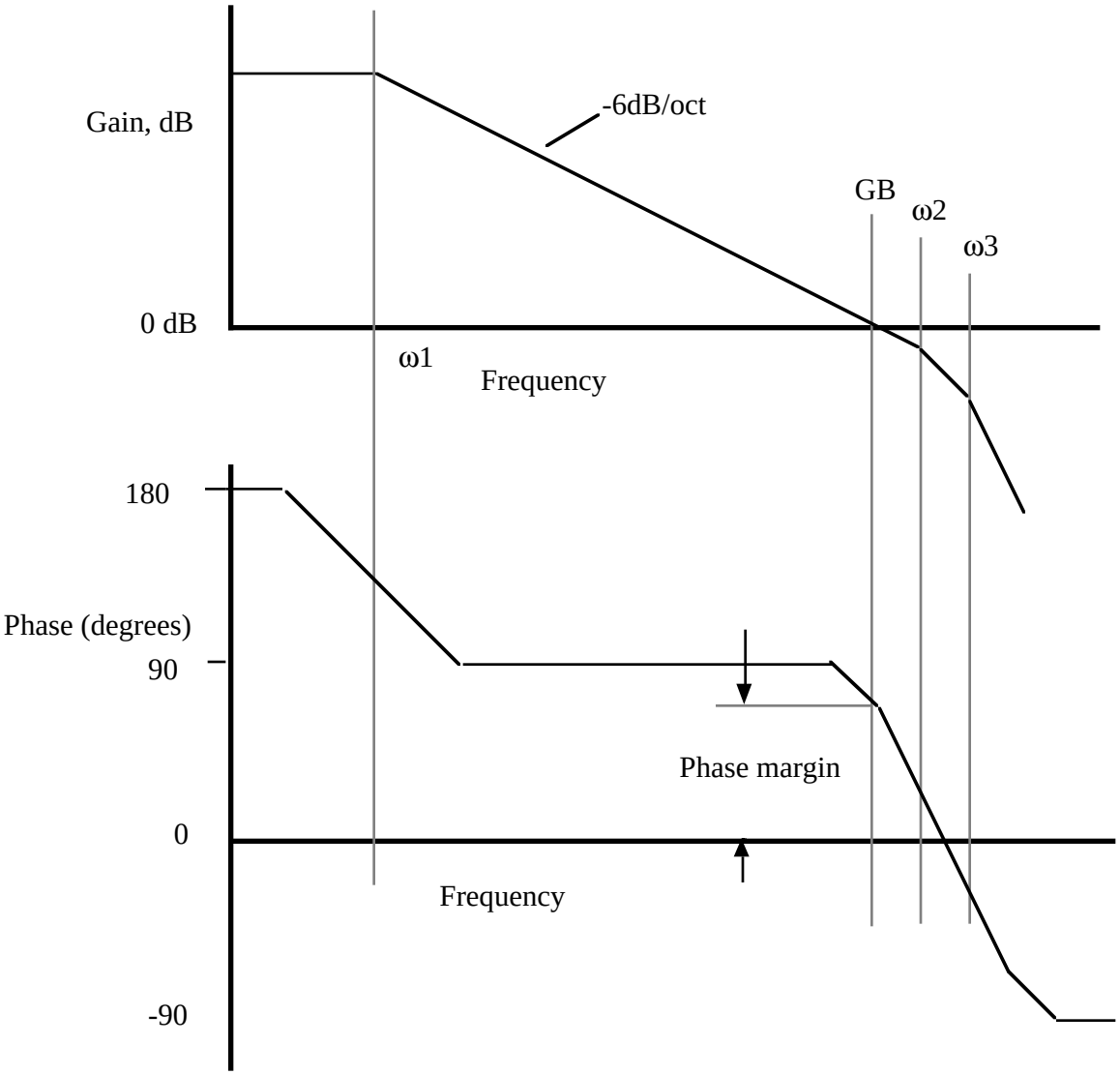
Non-ideal model for an op amp



Boundary Conditions	Requirement
Process Specification	See Tables 3.1-1 and 3.1-2
Supply Voltage	+5 V ±10%
Supply Current	100 μA
Temperature Range	0 to 70°C
Typical Specifications	
Gain	≥ 80 dB
Gainbandwidth	≥ 10 MHz
Settling Time	≤ 0.1 μsec
Slew Rate	≥ 2 V/μsec
Input CMR	≥ ±2 V
CMRR	≥ 60 dB
PSRR	≥ 60 dB
Output Swing	≥ 2 VP-P
Output Resistance	Capacitive load only
Offset	≤ ±5 mV
Noise	≤ 50nV/$\sqrt{\text{Hz}}$ at 1KHz
Layout Area	≤ 10,000 square μm

Frequency Response

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\cdots}$$



Power supply rejection ratio (PSRR):

$$\text{PSRR} = \left(\frac{\Delta V_{DD}}{\Delta v_{OUT}}\right) \cdot A_{vd}(s) = \frac{A_{vd}(s)}{A_{ps}(s)} = \frac{\frac{v_{out}}{v_{in}}(v_{ps}=0)}{\frac{v_{out}}{v_{ps}}(v_{in}=0)}$$

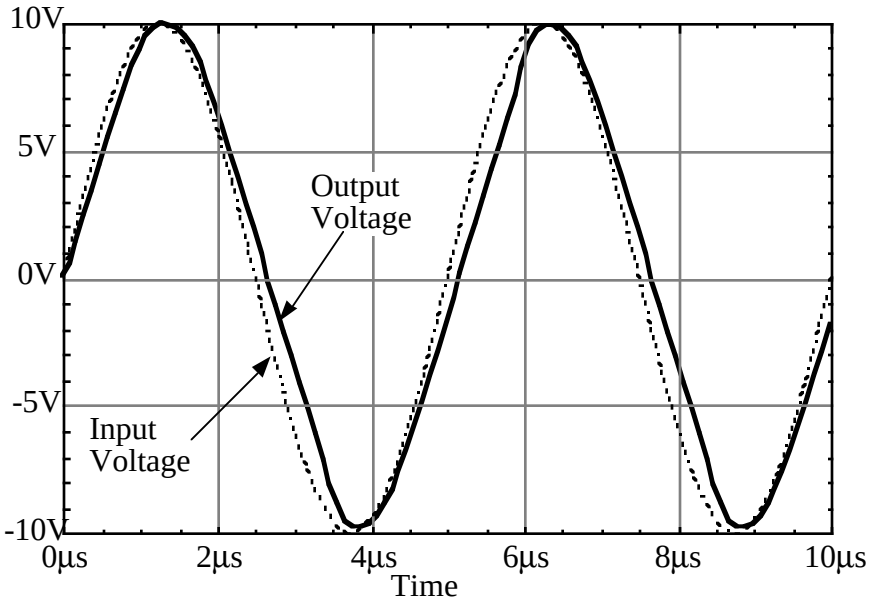
Common-mode input range (ICMR).

Maximum common mode signal range over which the differential voltage gain of the op amp remains constant.

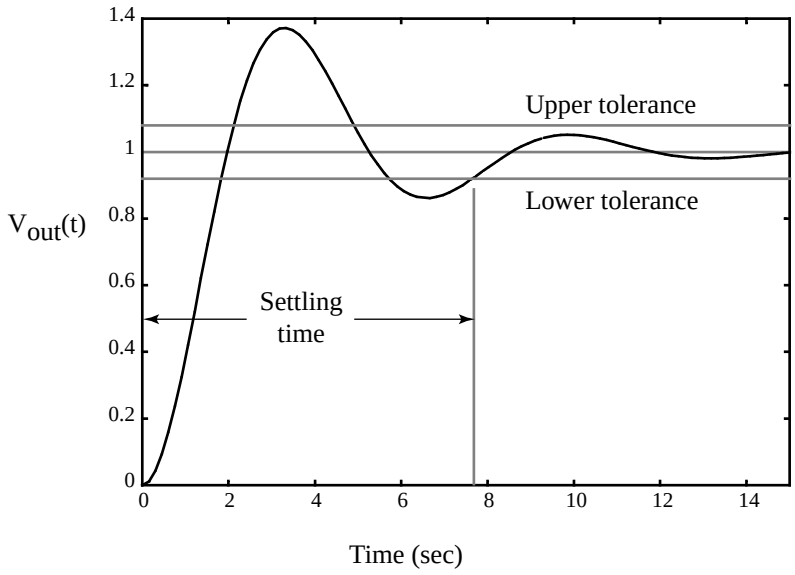
Maximum and minimum output voltage swing.

Slew rate:

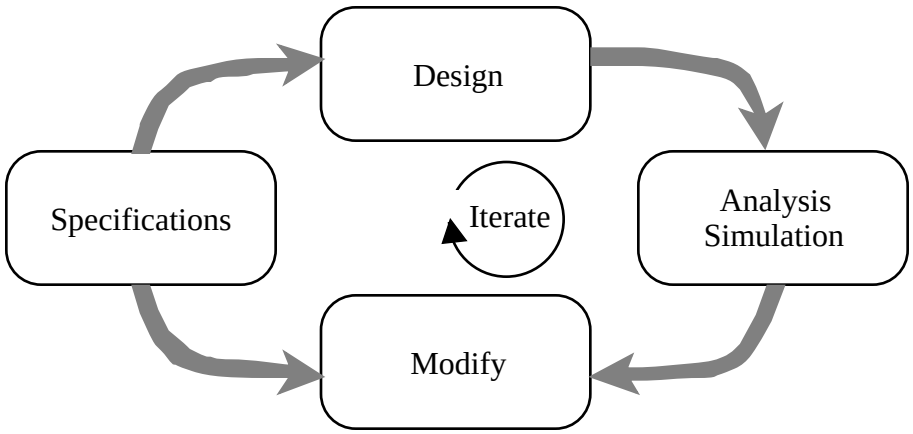
$$\text{Slew rate} = \max\left(\frac{\Delta v_{OUT}}{\Delta t}\right)$$



Settling Time



Design Approach



Specifications:

- Gain
- Output voltage swing
- Settling time
- Power dissipation
- Supply voltage
- Silicon area
- Bandwidth
- PSRR
- CMRR
- Noise
- Common-mode input range

Design Strategy

The design process involves two distinct activities:

Architecture Design

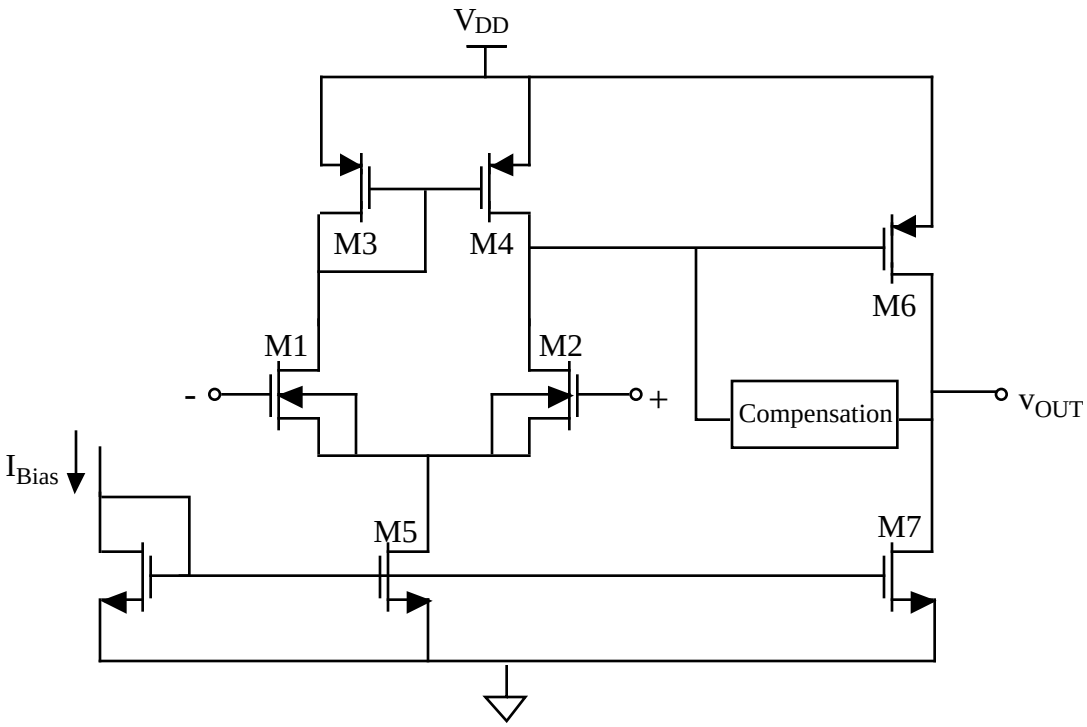
- Find an architecture already available and adapt it to present requirements
- Create a new architecture that can meet requirements

Component Design

- Design transistor sizes
- Design compensation network

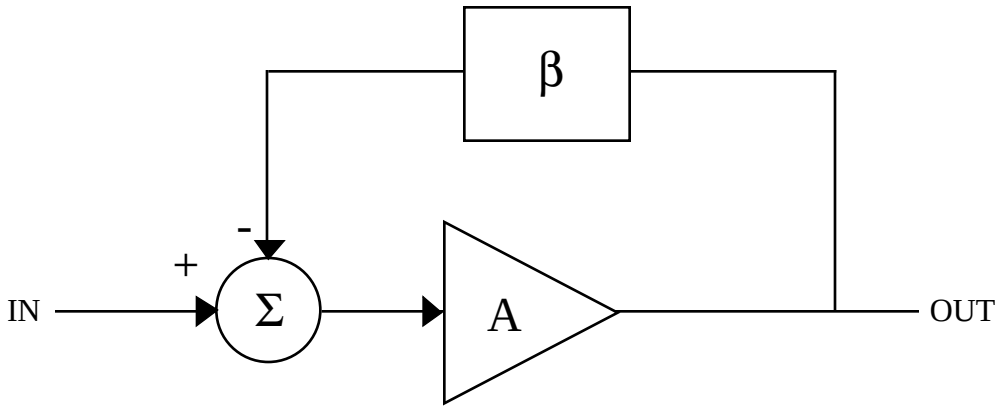
If available architectures do not meet requirements, then an existing architecture must be modified, or a new one designed. Once a satisfactory architecture has been obtained, then devices and the compensation network must be designed.

Op Amp Architecture



Compensation

In virtually all op amp applications, feedback will be applied around the amplifier. Therefore, stable performance requires that the amplifier be compensated. Essentially we desire that the loop gain be less than unity when the phase shift around the loop is greater than 135˚

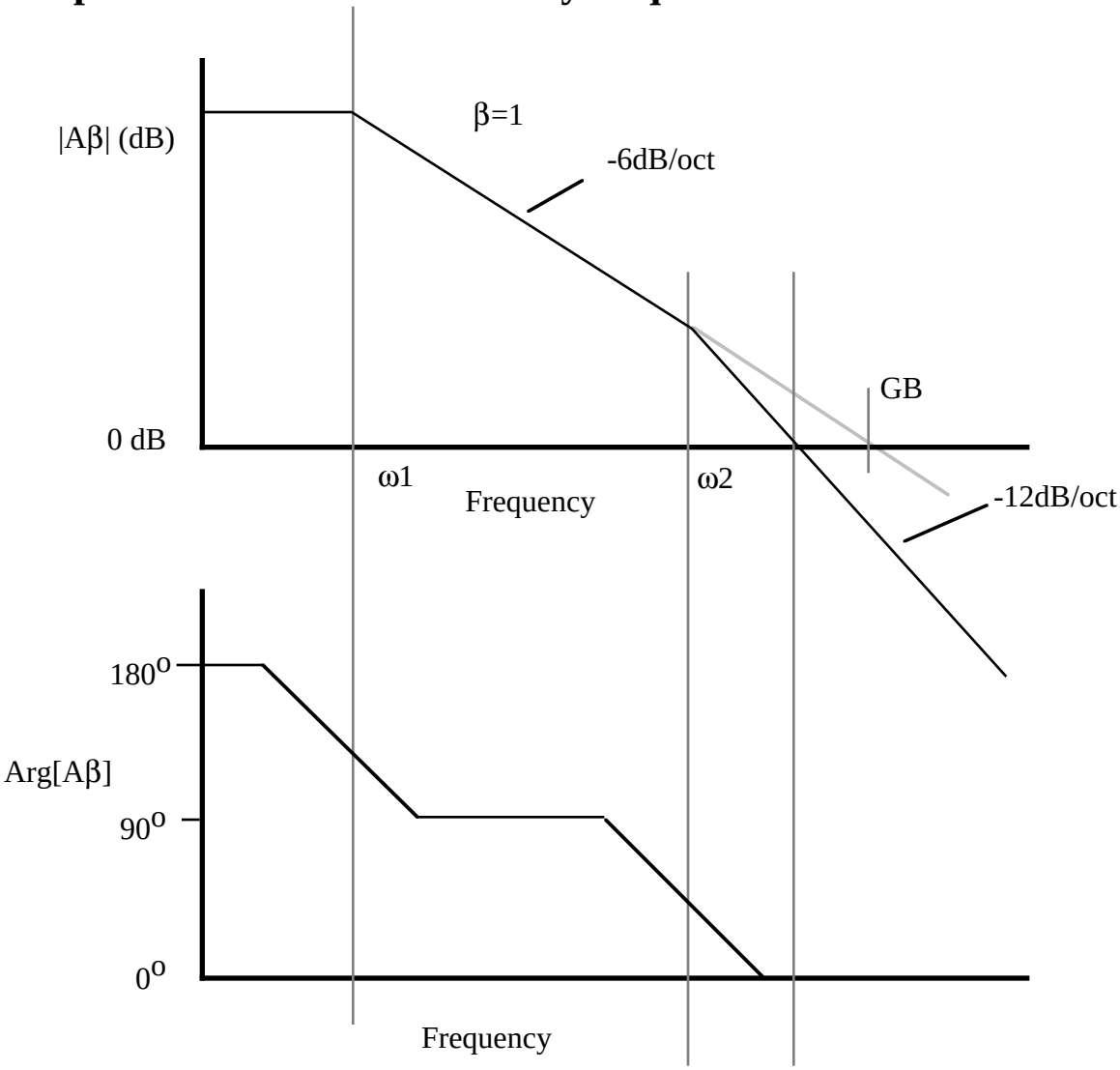


$$\frac{OUT}{IN} = \frac{A}{1 + A\beta}$$

Goal: $1 + A\beta > 0$

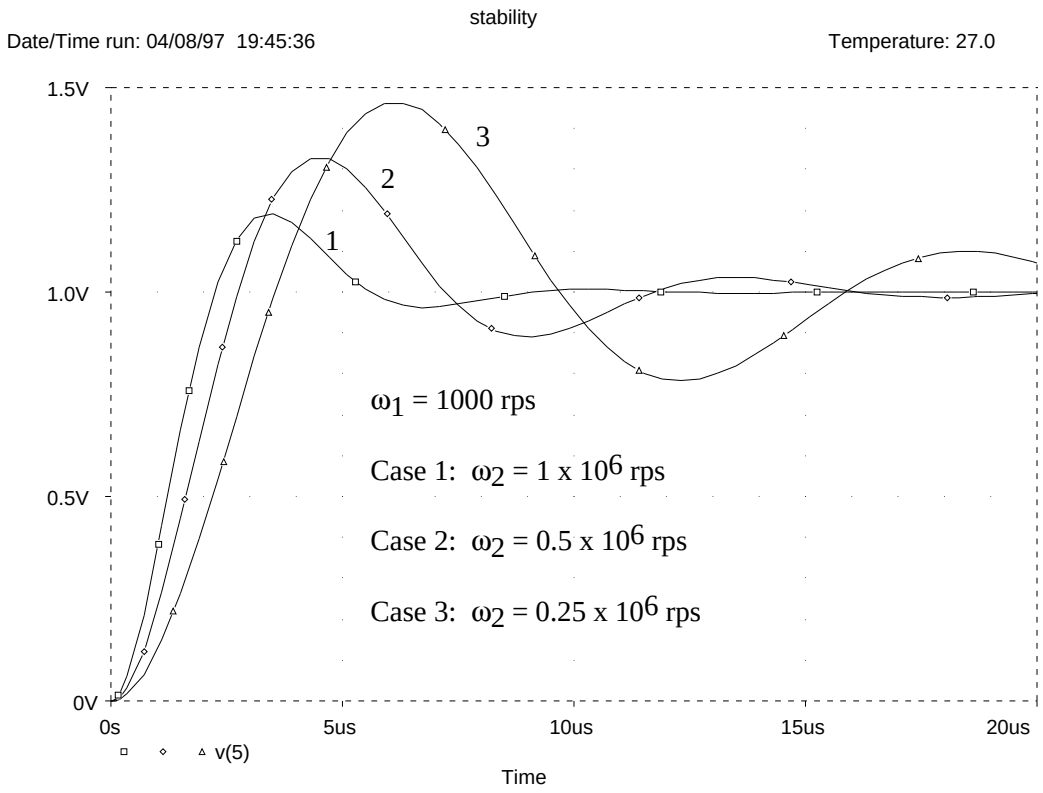
Rule of thumb: $\arg[A\beta] < 135^\circ$ at $\text{mag}[A\beta] = 1$

Graphical Illustration of Stability Requirements



Step Response of Two-Pole System

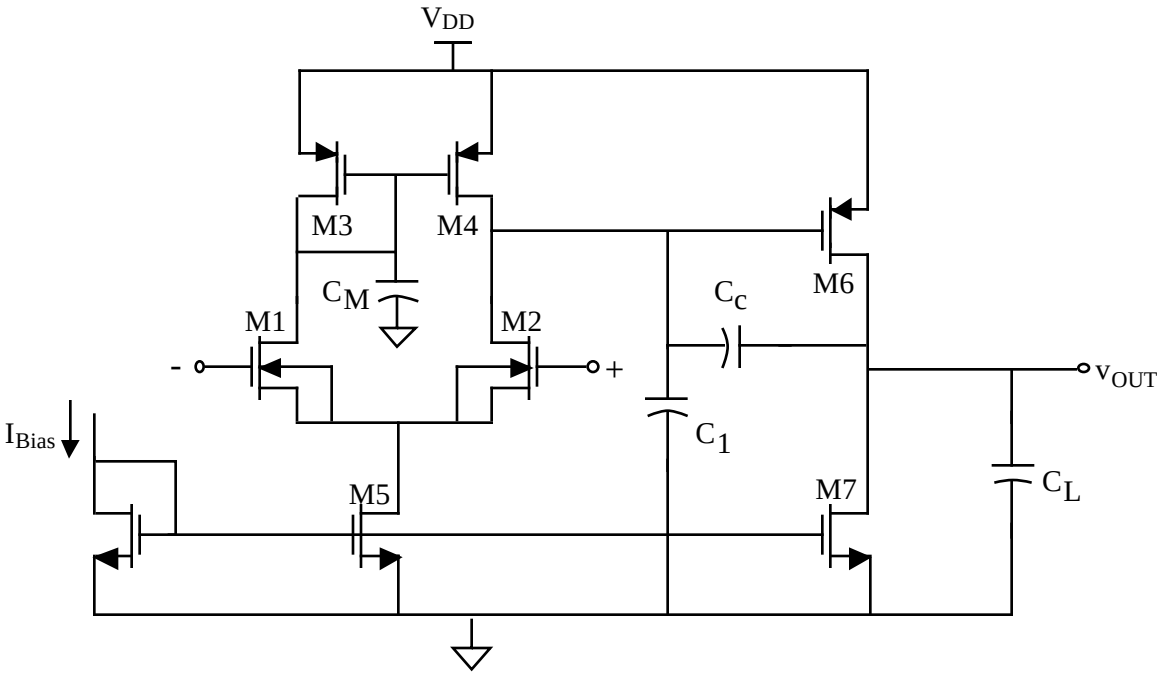
Impact of placing ω_2 at different locations:



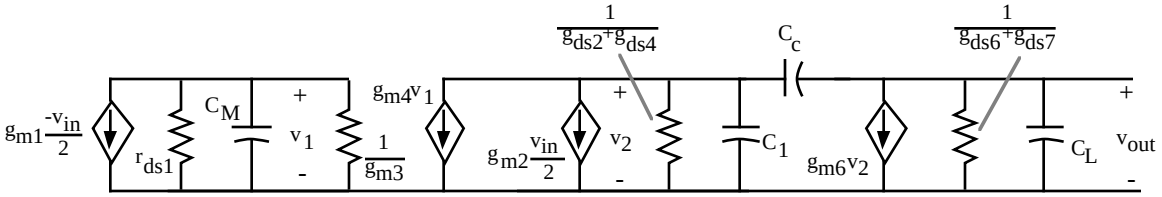
Types of Compensation

1. Miller - Use of a capacitor feeding back around a high-gain, inverting stage.
    - Miller capacitor only
    - Miller capacitor with an unity-gain buffer to block the forward path through the compensation capacitor. Can eliminate the RHP zero.
    - Miller with a nulling resistor. Similar to Miller but with an added series resistance to gain control over the RHP zero.
2. Self compensating - Load capacitor compensates the op amp (later).
3. Feedforward - Bypassing a positive gain amplifier resulting in phase lead. Gain can be less than unity.

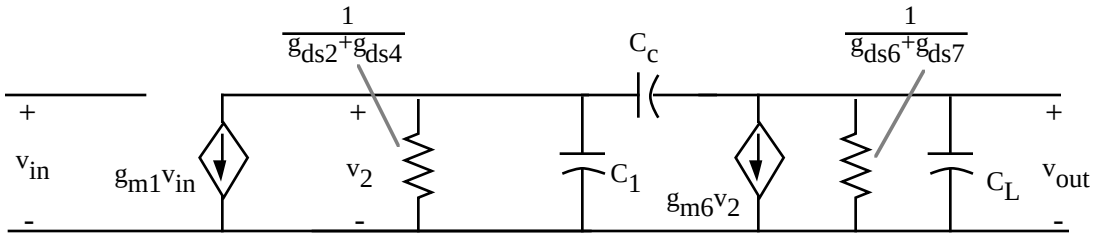
Miller Compensation



Small-signal model



Simplified small-signal model



Analysis

$$\frac{V_O(s)}{V_{\text{in}}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})(1 - sC_c/g_{mII})}{1 + s[R_I(C_1 + C_c) + R_{II}(C_L + C_c) + g_{mII}R_IR_{II}C_c] + s^2R_IR_{II}[C_1C_L + C_c(C_1 + C_L)]}$$

$$p_1 \cong \frac{-1}{g_{mII}\, R_I\, R_{II}\, C_c}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_1C_L + C_LC_c + C_1C_c}$$

$$p_2 \cong \frac{-g_{mII}}{C_L}$$

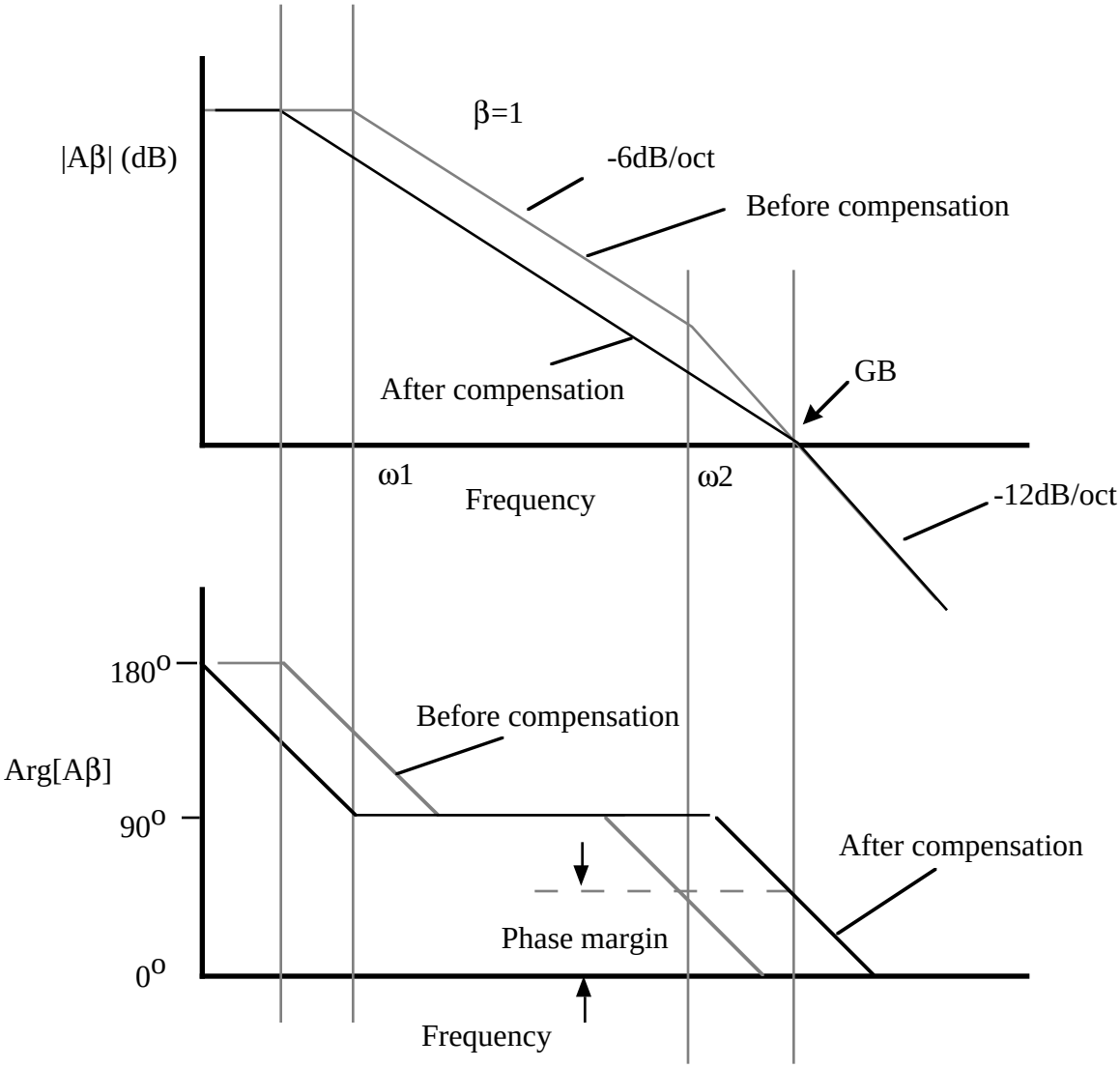
$$z_1 = \frac{g_{mII}}{C_c}$$

where

$$g_{mI} = g_{m1} = g_{m2} \qquad g_{mII} = g_{m6}$$

$$R_I = \frac{1}{g_{ds2} + g_{\text{ds4}}} \qquad R_{II} = \frac{1}{g_{ds6} + g_{ds7}}$$

Miller Compensation



Conditions for Stability

• Unity-gainbandwith is given as:

$$GB = A_v(0)\cdot|p_1| = (g_{mI}g_{mII}R_IR_{II})\cdot\left(\frac{1}{g_{mII}R_IR_{II}C_c}\right) = \frac{g_{mI}}{C_c}$$

• The requirement for 45° phase margin is:

$$\text{Arg}[A\beta] = \pm 180° - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z}\right) = 45°$$

Let $\omega = GB$ and assume that $z \geq 10GB$, therefore we get,

$$\pm 180° - \tan^{-1}\left(\frac{GB}{|p_1|}\right) - \tan^{-1}\left(\frac{GB}{|p_2|}\right) - \tan^{-1}\left(\frac{GB}{z}\right) = 45°$$

or

$$135° \approx \tan^{-1}(A_v(0)) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1) = 90° + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + 5.7°$$

$$39.3° \approx \tan^{-1}\left(\frac{GB}{|p_2|}\right) \Rightarrow \frac{GB}{|p_2|} = 0.818 \Rightarrow \boxed{|p_2| \geq 1.22GB}$$

• The requirement for 60° phase margin:

$$\boxed{|p_2| \geq 2.2GB \text{ if } z \geq 10GB}$$

- If 60° phase margin is required, then the following relationships apply:

$$\frac{g_{mII}}{C_c} > \frac{10g_{mI}}{C_c} \quad \Rightarrow \quad \boxed{g_{mII} > 10g_{mI}}$$

Furthermore,

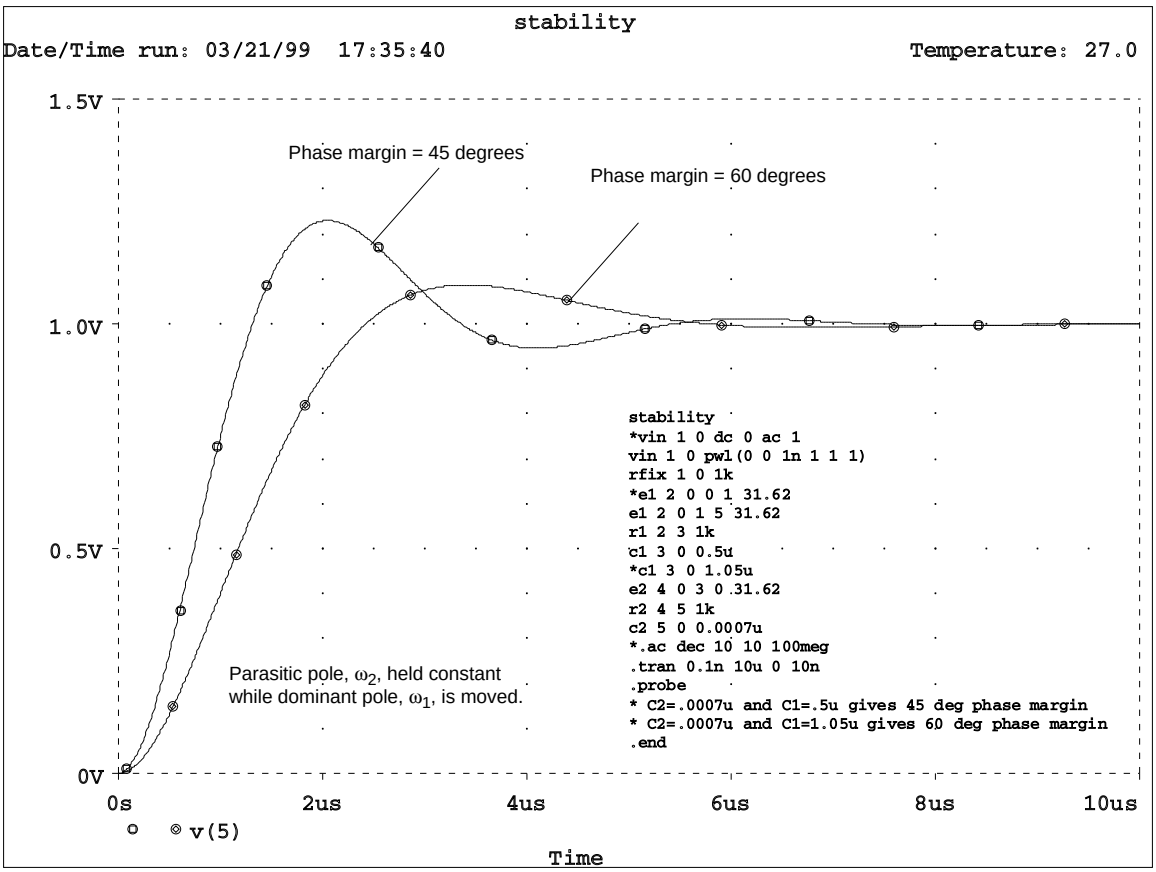
$$\frac{g_{mII}}{C_2} > \frac{2.2g_{mI}}{C_c}$$

which after substitution gives:

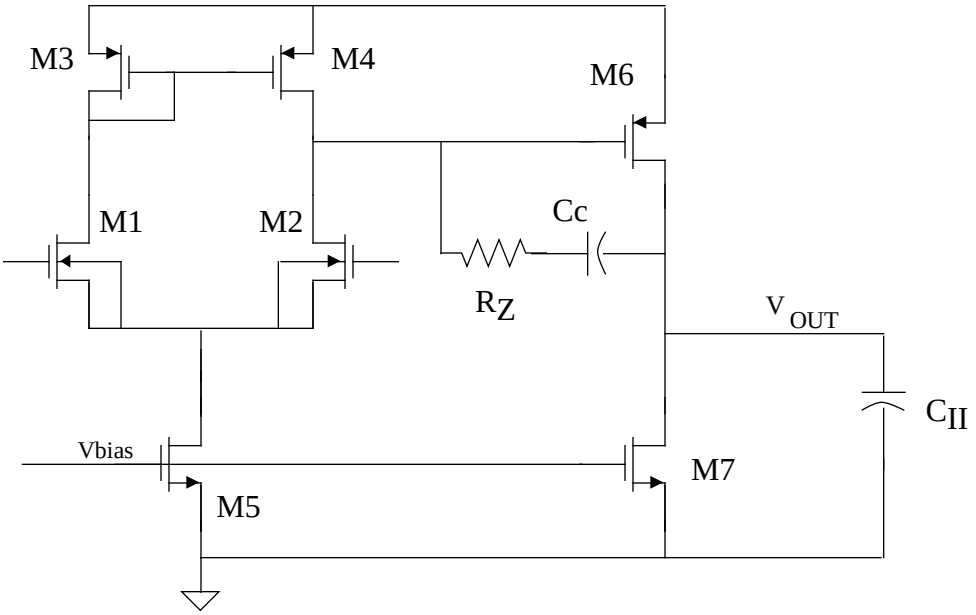
$$\boxed{C_c > 0.22C_2}$$

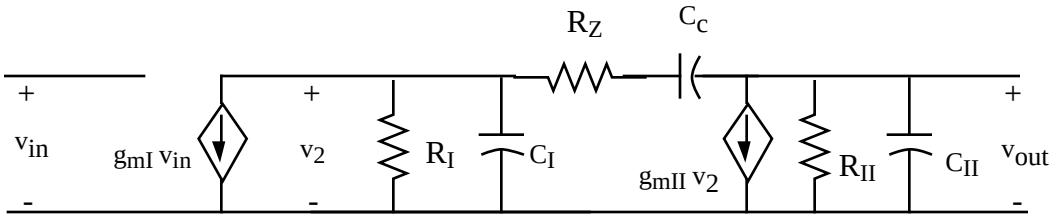
Note:

$g_{mI} = g_{m1} = g_{m2}$ and $g_{mII} = g_{m6}$


stability
Date/Time run: 03/21/99 17:35:40
Temperature: 27.0
1.5V
1.0V
0.5V
0V
Phase margin = 45 degrees
Phase margin = 60 degrees
Parasitic pole, ω2, held constant
while dominant pole, ω1, is moved.
stability
*vin 1 0 dc 0 ac 1
vin 1 0 pwl(0 0 1n 1 1 1)
rfix 1 0 1k
*e1 2 0 0 1 31.62
e1 2 0 1 5 31.62
r1 2 3 1k
c1 3 0 0.5u
*c1 3 0 1.05u
e2 4 0 3 0 31.62
r2 4 5 1k
c2 5 0 0.0007u
*.ac dec 10 10 100meg
.tran 0.1n 10u 0 10n
.probe
* C2=.0007u and C1=.5u gives 45 deg phase margin
* C2=.0007u and C1=1.05u gives 60 deg phase margin
.end
0s
2us
4us
6us
8us
10us
v(5)
Time

Eliminating RHP Zero





$$g_{mI}V_{\text{in}} + \frac{V_I}{R_I} + sC_IV_I + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_I - V_o) = 0$$

$$g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_o + \left(\frac{sC_c}{1 + sC_cR_z}\right)(V_o - V_I) = 0$$

These equations can be solved to give

$$\frac{V_o(s)}{V_{\text{in}}(s)} = \frac{a\{1 - s[(C_c/g_{mII}) - R_zC_c]\}}{1 + bs + cs^2 + ds^3}$$

where

$$a = g_{mI}g_{mII}R_IR_{II}$$

$$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_IR_{II}C_c + R_zC_c$$

$$c = [R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II}) + R_z C_c (R_I C_I + R_{II} C_{II})]$$

$$d = R_I R_{II} R_z C_I C_{II} C_c$$

If R_z is assumed to be less than R_I or R_{II} and the poles widely spaced, then the roots are

$$p_1 \cong \frac{-1}{(1 + g_{mII} R_{II}) R_I C_c} \cong \frac{-1}{g_{mII} R_{II} R_I C_c}$$

$$p_2 \cong \frac{-g_{mII} C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \cong \frac{-g_{mII}}{C_{II}}$$

$$p_3 = \frac{-1}{R_z C_I}$$

and

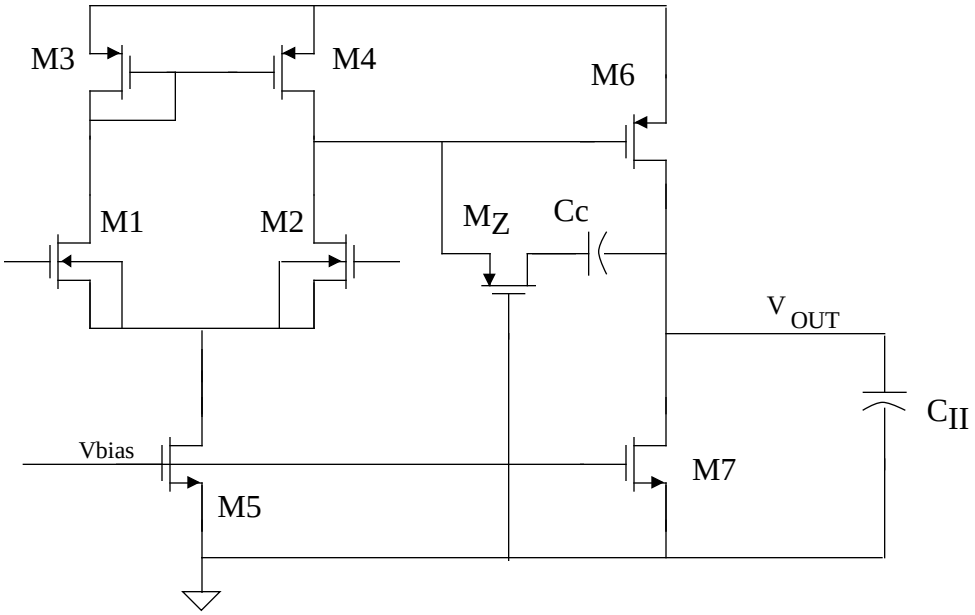
$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)}$$

By setting

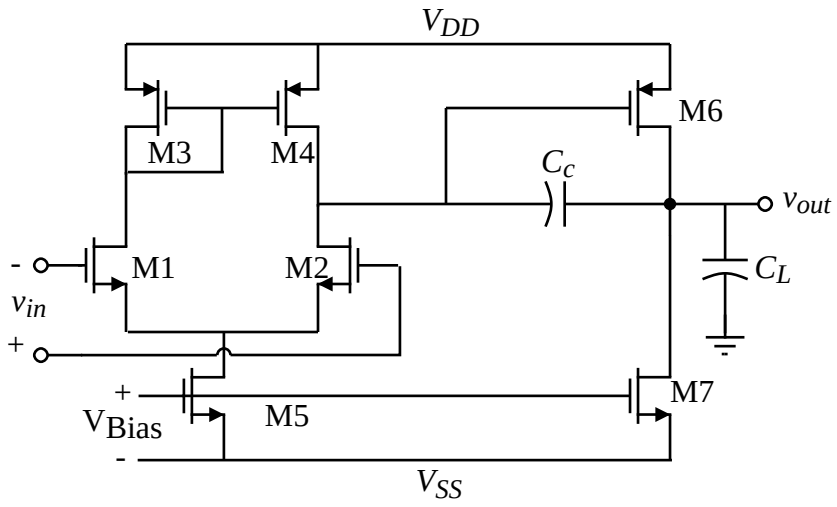
$$R_z = 1/g_{mII}$$

The RHP zero moves to infinity

Implementing Compensation Resistor



Two-Stage Operational Amplifier Design



Important relationships:

$g_{m1} = g_{m2} = g_{mI}$, $g_{m6} = g_{mII}$, $g_{ds2} + g_{ds4} = G_I$, and $g_{ds6} + g_{ds7} = G_{II}$.

$$\text{Slew rate } SR = \frac{I_5}{C_c} \tag{1}$$

$$\text{First-stage gain } A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \tag{2}$$

$$\text{Second-stage gain } A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)} \tag{3}$$

$$\text{Gain-bandwidth } GB = \frac{g_{m1}}{C_c} \tag{4}$$

$$\text{Output pole } p_2 = \frac{-g_{m6}}{C_L} \tag{5}$$

$$\text{RHP zero } z_1 = \frac{g_{m6}}{C_c} \tag{6}$$

$$\text{Positive CMR } V_{\text{in(max)}} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{\text{(max)}} + V_{T1(\text{min})}) \tag{7}$$

$$\text{Negative CMR } V_{\text{in(min)}} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(\max)} + V_{DS5}(\text{sat}) \tag{8}$$

$$\text{Saturation voltage} V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \tag{9}$$

All transistors are in saturation for the above relationships.

The following design procedure assumes that specifications for the following parameters are given.

1. Gain at dc, $A_v(0)$
2. Gain-bandwidth, *GB*
3. Input common-mode range, ICMR
4. Load Capacitance, C_L
5. Slew-rate, *SR*
6. Output voltage swing
7. Power dissipation, P_{diss}

Choose a device length to establish of the channel-length modulation parameter λ.

Design the compensation capacitor C_c. It was shown that placing the loading pole p_2 2.2 times higher than the *GB* permitted a 60° phase margin (assuming that the RHP zero z_1 is placed at or beyond ten times *GB*). This results in the following requirement for the minimum value for C_c.

$$C_c > (2.2/10)C_L$$

Next, determine the minimum value for the tail current I_5, based upon slew-rate requirements. Using Eq. (1), the value for I_5 is determined to be

$$I_5 = SR\ (C_c)$$

If the slew-rate specification is not given, then one can choose a value based upon settling-time requirements. Determine a value that is roughly ten times faster than the settling-time specification, assuming that the output slews approximately one-half of the supply rail. The value of I_5 resulting from this calculation can be changed later if need be.

The aspect ratio of M3 can now be determined by using the requirement for positive input common-mode range. The following design equation for $(W/L)_3$ was derived from Eq. (7).

$$S_3 = (W/L)_3 = \frac{I_5}{(K'_3)\,[V_{DD} - V_{\text{in}}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2}$$

If the value determined for $(W/L)_3$ is less than one, then it should be increased to a value that minimizes the product of *W* and *L*. This minimizes the area of the gate region, which

in turn reduces the gate capacitance. This gate capacitance will affect a pole-zero pair which causes a small degradation in phase margin.

Requirements for the transconductance of the input transistors can be determined from knowledge of C_c and *GB*. The transconductance g_{m2} can be calculated using the following equation

$$g_{m1} = GB(C_c)$$

The aspect ratio $(W/L)_1$ is directly obtainable from g_{m1} as shown below

$$S_1 = (W/L)_1 = \frac{g_{m1}^2}{(K'_2)(I_5)}$$

Enough information is now available to calculate the saturation voltage of transistor M5. Using the negative ICMR equation, calculate V_{DS5} using the following relationship derived from Eq. (8).

$$V_{DS5} = V_{\text{in}}(\text{min}) - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{1/2} - V_{T1}(\text{max})$$

If the value for V_{DS5} is less than about 100 mV then the possibility of a rather large $(W/L)_5$ may result. This may not be acceptable. If the value for V_{DS5} is less than zero, then the ICMR specification may be too stringent. To solve this problem, I_5 can be reduced or $(W/L)_1$ increased. The effects of these changes must be accounted for in previous design steps. One must iterate until the desired result is achieved. With V_{DS5} determined, $(W/L)_5$ can be extracted using Eq. (9) in the following way

$$S_5 = (W/L)_5 = \frac{2(I_5)}{K'_5(V_{DS5})^2}$$

For a phase margin of 60°, the location of the loading pole was assumed to be placed at 2.2 times *GB*. Based upon this assumption and the relationship for $|p_2|$ in Eq. (5), the transconductance g_{m6} can be determined using the following relationship

$$g_{m6} = 2.2(g_{m2})(C_L/C_c)$$

Since S_3 is known as well as g_{m6} and g_{m3}, assuming balanced conditions,

$$S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$$

I_6 can be calculated from the consideration of the "proper mirroring" of first-stage the current mirror load of Fig. 6.3-1. For accurate current mirroring, we want V_{SD3} to be equal to V_{SD4}. This will occur if V_{SG4} is equal to V_{SG6}. V_{SG4} will be equal to V_{SG6} if

$$I_6 = \frac{(W/L)_6}{(W/L)_4} I_1 = \left(\frac{S_6}{S_4}\right) I_1$$

Choose the larger of these two values for I_6 (Eq. 19 or Eq. 20). If the larger value is found in Eq (19), then $(W/L)_6$ must be increased to satisfy Eq. (20). If the larger value is found in Eq. (20), then no other adjustments must be made. One also should check the power dissipation requirements since I_6 will most likely determine the majority of the power dissipation.

The device size of M7 can be determined from the balance equation given below

$$S_7 = (W/L)_7 = (W/L)_5 \left(\frac{I_6}{I_5}\right) = S_5 \left(\frac{I_6}{I_5}\right)$$

The first-cut design of all *W/L* ratios are now complete. Fig. 6.3-2 illustrates the above design procedure showing the various design relationships and where they apply in the two-stage CMOS op amp.

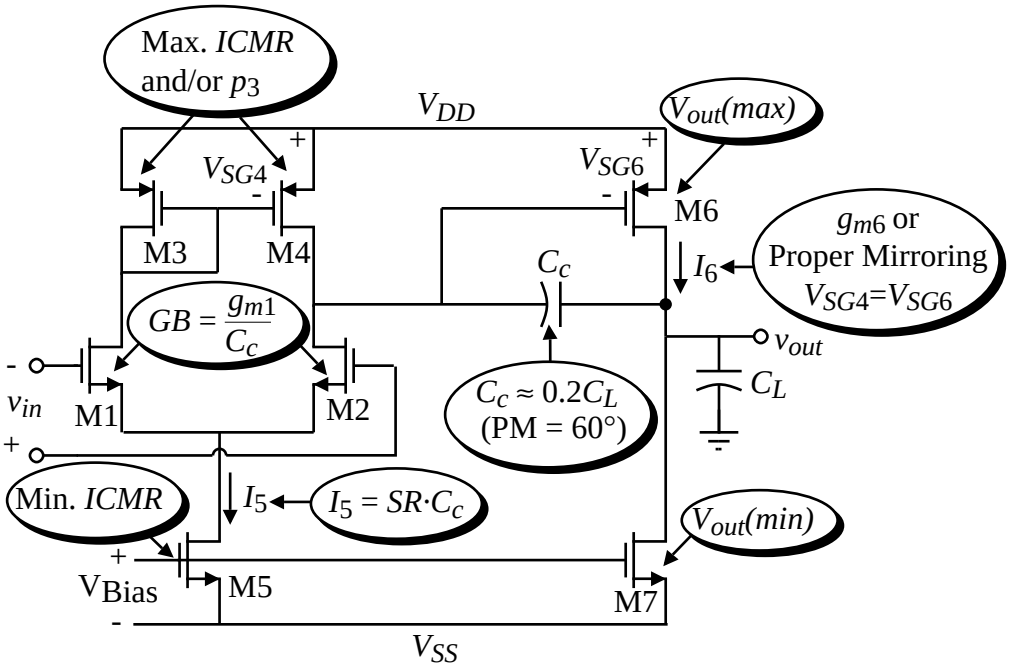


Figure 6.3-2 Illustration of the design relationships and the circuit for a two-stage CMOS op amp.

At this point in the design procedure, the total amplifier gain must be checked against the specifications.

$$A_v = \frac{(2)(g_{m2})(g_{m6})}{I_5(\lambda_2 + \lambda_3) I_6(\lambda_6 + \lambda_7)}$$

If the gain is too low, a number of things can be adjusted. The best way to do this is to use the table below, which shows the effects of various device sizes and currents on the

different parameters generally specified. Each adjustment may require another pass through this design procedure in order to insure that all specifications have been met. Table 6.3-2 summarizes the above design procedure.

Dependencies of device performance on various parameters

	Drain Current		M1 and M2		M3 and M4		Inverter	Inverter Load		Comp. Cap..
	I_5	I_7	W/L	L	W	L	W_6/L_6	W_7	L_7	C_c
Increase DC Gain	$(\downarrow)^{1/2}$	$(\downarrow)^{1/2}$	$(\uparrow)^{1/2}$	$\uparrow$		$\uparrow$	$(\uparrow)^{1/2}$		$\uparrow$	
Increase GB	$(\uparrow)^{1/2}$		$(\uparrow)^{1/2}$							$\downarrow$
Increase RHP Zero		$(\uparrow)^{1/2}$					$(\uparrow)^{1/2}$			$\downarrow$
Increase Slew Rate	$\uparrow$									$\downarrow$
Increase C_L										$\downarrow$

Design Procedure:

This design procedure assumes that the gain at dc (A_v), unity gain bandwidth (GB), input common mode range (V_{in}(min) and V_{in}(max)), load capacitance (C_L), slew rate (SR), settling time (T_s), output voltage swing (V_{out}(max) and V_{out}(min)), and power dissipation (P_{diss}) are given.

1. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.
2. From the desired phase margin, choose the minimum value for C_c, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

   $$C_c > 0.22C_L$$

3. Determine the minimum value for the "tail current" (I_5) from the largest of the two values.

   $$I_5 = SR \cdot C_c$$

   $$I_5 \cong 10\left(\frac{V_{DD} + |V_{SS}|}{2 \cdot T_s}\right)$$

4. Design for S_3 from the maximum input voltage specification.

   $$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\text{max}) - |V_{T03}|(\text{max}) + V_{T1}(\text{min})]^2} \geq 1$$

5. Verify that the pole of M3 due to C_{gs3} and C_{gs4} (=$0.67W_3L_3C_{ox}$) will not be dominant by assuming it to be greater than 10 GB

   $$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

6. Design for S_1 (S_2) to achieve the desired GB.

   $$g_{m1} = GB \cdot C_c \Rightarrow S_2 = \frac{g_{m2}^2}{K'_2 I_5}$$

7. Design for S_5 from the minimum input voltage. First calculate V_{DS5}(sat) then find S_5.

   $$V_{DS5}(\text{sat}) = V_{in}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\text{max}) \geq 100 \text{ mV}$$

   $$S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

8. Find g_{m6} and S_6 by the relationship relating to phase margin, load, and compensation capacitors, and the balance condition.

$$g_{m6} = 2.2g_{m2}(C_L/C_c)$$

$$S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$$

9. Calculate I_6 :

$$I_6 = (S_6/S_4)I_4 = (S_6/S_4)(I_5/2)$$

10. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = (I_6/I_5)S_5$$

11. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

$$P_{diss} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

12. If the gain specification is not met, then the currents, I_5 and I_6, can be decreased or the W/L ratios of M2 and/or M6 increased. The previous calculations must be rechecked to insure that they have been satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate increase of some of the W/L ratios in order to satisfy input and output swings.
13. Simulate the circuit to check to see that all specifications are met.

Example: Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-1 and 3.1-2, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications. Assume the channel length is to be 1μm.

A_V > 3000V/V	V_{DD} = 2.5V	V_{SS} = -2.5V
GB = 5MHz	C_L = 10pF	SR > 10V/μs
V_{out} range = ±2V	$ICMR$ = -1 to 2V	P_{diss} ≤ 2mW

Solution

Calculate the minimum value of the compensation capacitor C_c,

$$C_c > (2.2/10)(10\text{ pF}) = 2.2\text{ pF}$$

Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3 \times 10^{-12})(10 \times 10^6) = 30\ \mu\text{A}$$

Next calculate $(W/L)_3$ using ICMR requirements.

$$(W/L)_3 = \frac{30 \times 10^{-6}}{(50 \times 10^{-6})[2.5 - 2 - .85 + 0.55]^2} = 15$$

$$g_{m3} = \sqrt{2 \times 50\text{x}10^{-6}\ \text{x}15\text{x}10^{-6} \times 15} = 150\mu\text{S}$$

Therefore

$$(W/L)_3 = (W/\text{L})_4 = 15$$

Check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the C_{ox} = 0.4fF/μm^2. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_pS_3I_3}}{2(0.667)W_3L_3C_{ox}} = 15.75\text{x}10^9(\text{rads/sec})$$

or 2.98 GHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

The next step in the design is to calculate g_{m1}

$$g_{m1} = (5 \times 10^6)(2\pi)(3 \times 10^{-12}) = 94.25\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{{g_{m1}}^2}{2K'_NI_1} = \frac{(94.25)^2}{2 \cdot 110 \cdot 15} = 2.79 \approx 3.0$$

Next calculate V_{DS5}

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30 \times 10^{-6}}{110 \times 10^{-6} \cdot 3}} - .85 = 0.35\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from Eq. (16)

$$(W/L)_5 = \frac{2(30 \times 10^{-6})}{(50 \times 10^{-6})(0.35)^2} = 4.49 \approx 4.5$$

From Eq. (20) of Sec. 6.2, we know that

$$g_{m6} \geq 10 g_{m1} \geq 942.5\mu\text{S}$$

Assuming that $g_{m6} = 942.5\mu\text{S}$

$$(W/L)_6 = 15 \ \frac{942.5 \times 10^{-6}}{150 \times 10^{-6}} = 94.25$$

Using the equations for proper mirroring, I_6 is determined to be

$$I_6 = (15 \times 10^{-6})(94.25/15) = 94.25\ \mu\text{A}$$

Finally, calculate $(W/L)_7$

$$(W/L)_7 = 4.5\left(\frac{94.25 \times 10^{-6}}{30 \times 10^{-6}}\right) \approx 14.14$$

Check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{min}(\text{out}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2 \times 94.25}{110 \times 14.14}} = 0.348\text{V}$$

which is much less than required. At this point, the first-cut design is complete. Examining the results shows that the large value of M7 is due to the large value of M5 which in turn is due to a tight specification on the negative input common mode range. To reduce these values the specification should be loosened or a different architecture (i.e. p-channel input pair) examined.

Now check to see that the gain specification has been met

$$A_v = \frac{(2)(94.25 \times 10^{-6})(942.5 \times 10^{-6})}{30 \times 10^{-6}(.04 + .05)38 \times 10^{-6}(.04 + .05)} = 19{,}240$$

which meets specifications.