Improving OP-AMP Phase Margin Tutorial

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1 ABSTRACT

This paper discusses the problems of degraded phase margin due to the RHP zero when designing large GB op-amp circuits. Using the op-amp example from another tutorial solutions to the RHP zero will be given.

2 INTRODUCTION

As mentioned in the introduction on op-amps the Miller compensation capacitor Cc is added across the output stage (Figure 1) to introduce a low frequency dominant pole so splitting this from the other circuit poles formed by the load capacitor and parasitic capacitors.

The basic MOS two-stage compensated OP-AMP is shown in Figure 1 and shows the location of the Miller capacitor Cc across M8.

The output stage M8 is an inverter and a low frequencies Cc is open-circuit (high-impedance).

2.1.1 The Zero

As the frequency rises the impedance of Cc falls and in effect introduces a short across M8 thus removing the inverting action. This is shown on figure 2 where path A is the normal path through the device M8 and path B is where the capacitor Cc has shorted across device M8 negating the inverting action of the stage.

3 SOLUTIONS

3.1.1 Nulling Resistor

In this scheme a resistor is placed in series with the Miller compensation resistor Cc. This has the effect of moving the RHP zero to the LHP and results in improvement of the phase margin.

4 DESIGN EQUATIONS

The dominant pole of the circuit is known as the Miller pole and effectively places a gain multiplied capacitor Cc from the gate to ground:

ie **C2 = Cc x (Gm8.RO1.RO2)**

At high(ish) frequencies the signal feeds back through M8 via the capacitor Cc causing the output impedance to fall. This will result in the output pole to rise in frequency.

As we move higher in frequency the device M8 will lose gain but signal will still be able to 'feed forward' through Cc as indicated by path B (Figure 2).

This feed forward of the signal will instead of being attenuated by M8 (Where the phase margin may be very low) will just pass straight through Cc with minimum attenuation. We might therefore have > 0dB for 0 phase margin and the circuit will become degenerative (positive feedback).

With reference to the op-amp circuit shown in **Figure 3**, the value of the nulling resistor Rz is simply given by:

The zero frequency is given by :

$$\omega_{zero} = \frac{1}{Cc\left(\frac{1}{gm_6} - Rz\right)}$$

$$\therefore \text{If } Rz >= \frac{1}{gm_6} \quad \text{then} \quad \omega_{zero} = 0$$

Where :

In saturation, in terms of voltage

$$gm_6 = \frac{K_P.W_6}{L_6}(V_{GS6} - V_{TP}) \quad \text{or}$$

In saturation, in terms of current

$$gm_6 = \sqrt{\frac{2.K_P.W_6.I_6}{L_6}}$$

In reality we move the RHP zero well into the LHP and this occurs if:

$$\frac{1}{Cc\left(\frac{1}{gm_6} - Rz\right)} = \frac{-gm_6}{C_{Load} + C_E} \quad \text{CE is small}$$

Rearrange to get Rz

$$Rz \approx \frac{C_{LOAD} + Cc}{gm_6.Cc}$$

We can see the effect of adding the 'nulling' resistor by modifying the op-amp example design to have a wide bandwidth. This can be achieved by increasing W1/W2, decreasing Cc or by increasing I5 which all will degrade the phase margin. Using the op-amp example the 'Miller' capacitor has been reduced to increase the gain bandwidth to ~ 10MHz as shown in **Figure 1**.

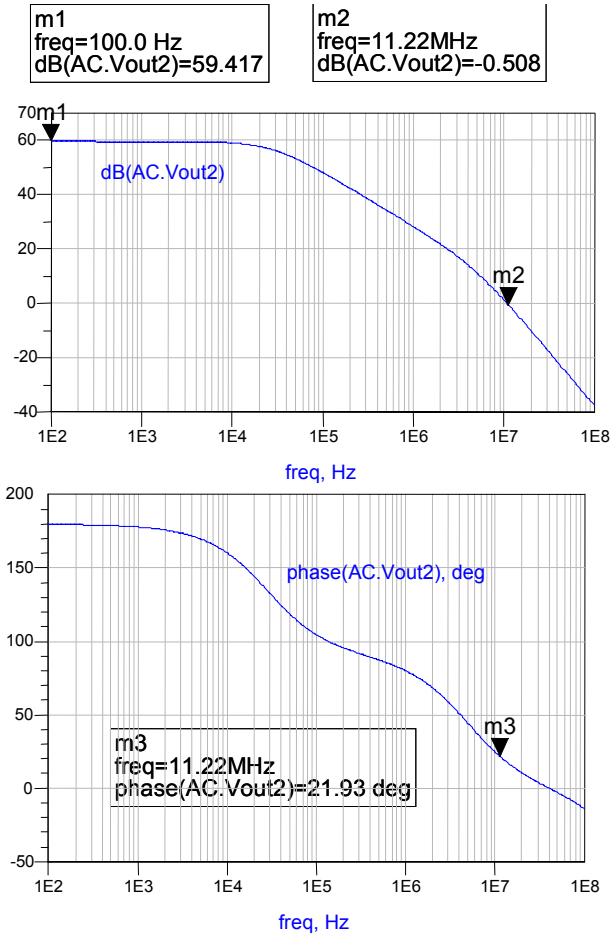


Figure 1 Modified op-amp (from the op-amp example tutorial) with increased gain bandwidth to ~ 20MHz. The 'Miller' capacitor has been reduced to 0.25pF (from 1.5pF) and has now degraded the phase margin from 62 degrees to 21 degrees.

From the op-amp example we found gm6 to be $500uAV^{-2}$. Therefore the value of Rz will be:

$$\text{Simple case } Rz = \frac{1}{gm_6} = \frac{1}{500E^{-6}} = 2K\Omega$$

However to cancel the first non - dominant pole we use

$$Rz \approx \frac{C_{LOAD} + Cc}{gm_6.Cc} \quad \therefore Rz \approx \frac{15E^{-12} + 0.25E^{-12}}{500E^{-6}.0.25E^{-12}} = 122K\Omega$$

Adding this 'nulling' resistor modifies the op-amp frequency response as shown in **Figure 2**.

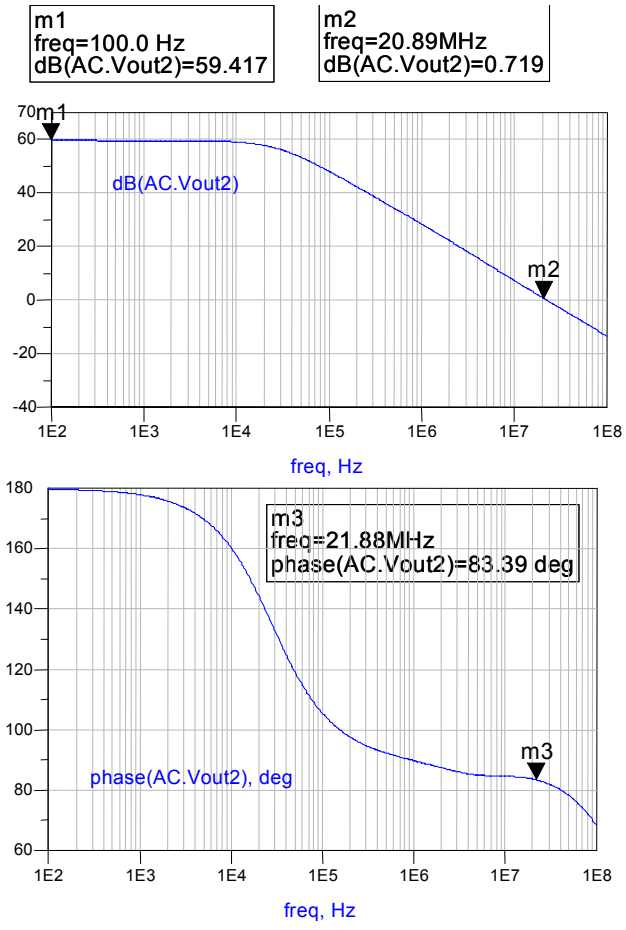


Figure 2 Effect on the op-amp frequency reponse by adding the 'nulling' resistor Rz. We can see that the phase margin has now increased to ~ 84degrees.

The addition of the 122Kohm 'nulling' resistor has increased the gain bandwidth from 11MHz to 20MHz with

a substantial improvement in phase margin from 21 degrees to 84 degrees.

The next section deals with the implementation of Rz using a MOSFET device.

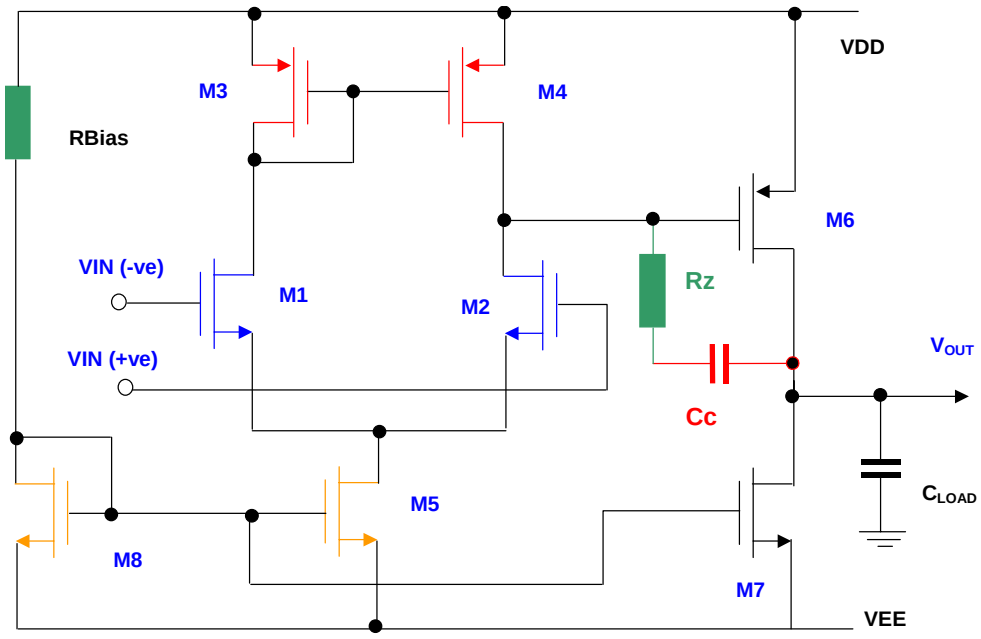


Figure 3 Simple Compensated OP-Amp circuit with Miller capacitor Cc added across M8 to produce the dominant pole.

combination of the differential amplifier current mirror resistance and the differential stage d-s.

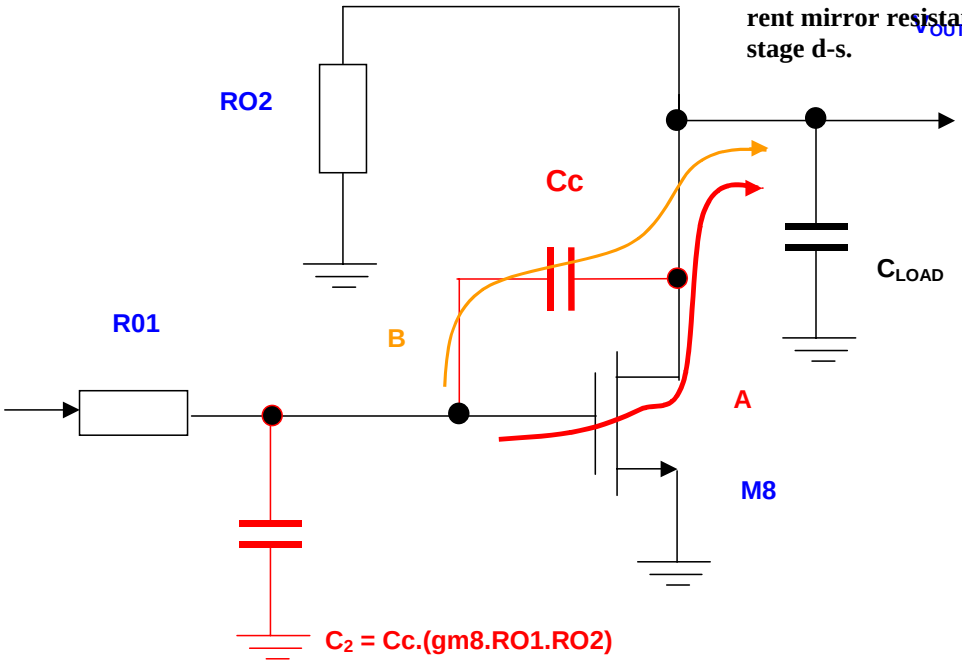


Figure 2 AC schematic of the output stage. The differential amplifier presents an impedance of RO1 to M8 gate. RO1 is the parallel

5 IMPLEMENTAION OF RZ

The resistor Rz can be implemented using a MOSFET device biased in it's active region, such that it acts as a resistor in series with the Miller capacitor Cc. The circuit arrangement is shown in **Figure 4**.

The expression for device 9 is as follows:

$$Rz = \frac{1}{K_P \frac{W_9}{L_9}\left(V_{gs9} - V_{TP}\right)}$$

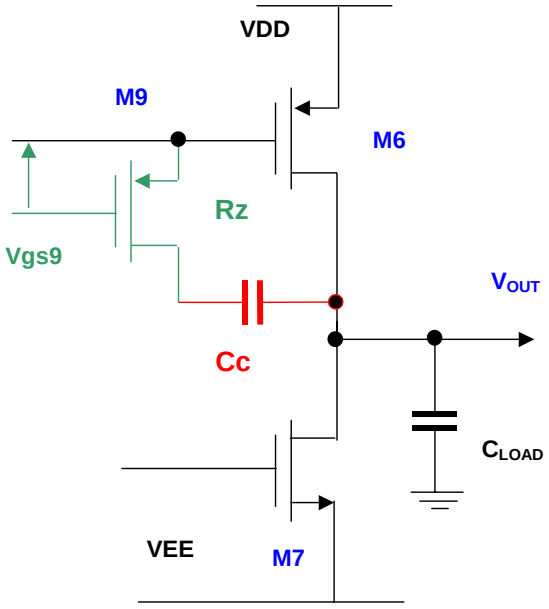


Figure 4 Implementaion of the 'Nulling' resistor Rz using a P-type device biased in it's active region.

Assuming we want a resistor Rz of value 122K we can calculate the required gate voltage for M9.

$$\frac{1}{K_P \frac{W_9}{L_9}.Rz} + V_{TP} = V_{gs9} \;\; ; \text{Assume } \frac{W_9}{L_9} = 1$$

$$\frac{1}{1.5035E^{-5} \cdot \frac{1}{1}.122E^{3}} + \left|-0.8889\right| = 1.43V$$

We can see that the gate of M9 will be referenced against the VSAT of M4 (see **Figure 1**). So if we mirror using another identical device connected to the gates of M3/M4, we will also get VSAT4. If we now add a device connected as a diode we can design it's Vds to be the 1.43V required by device M9. We will finally have to add a third device to ground to complete the voltage division change as shown in **Figure 5**.

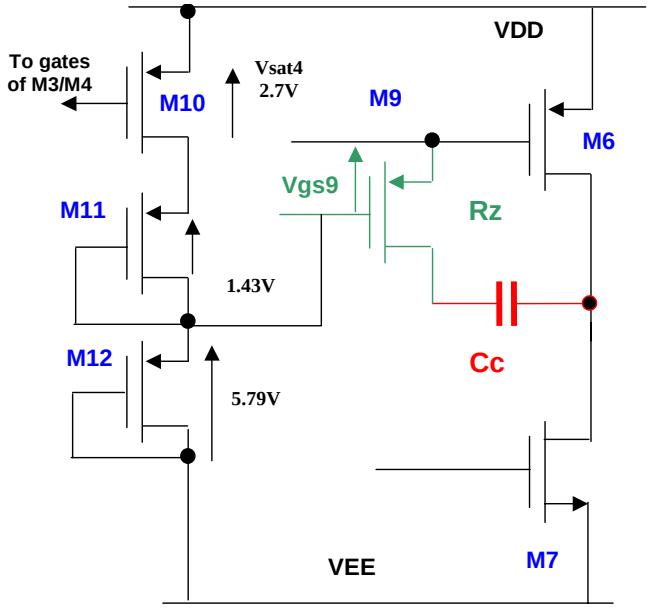


Figure 5 Bias references for FET M9. M10 has the same VSAT as M4 and M11 develops the required vgs for M8. M12 completes the voltage division chain.

Calculations of diodes M11 and M12:

Device M11 generates the gate voltage for M9 by having a VSAT of 1.43V.

$$V_{DS11} = VT + \sqrt{\frac{2.I_D.L_{11}}{K_P.W_{11}}} \quad \text{Rearrange to get } \frac{W}{L}$$

$$\frac{W_{11}}{L_{11}} = \frac{KP\left(V_{DS11} + VT\right)^2}{2.ID} \quad ID = 10uA \;\; \therefore$$

$$\frac{W_{11}}{L_{11}} = \frac{1.5035E^{-5}\left(1.43 + 0.889\right)^2}{2.10E^{-6}} = 9$$

Finally the VSAT of M12 needs to be 5.79V to complete the voltage division chain:

$$V_{DS11} = VT + \sqrt{\frac{2.I_D.L_{12}}{K_P.W_{12}}} \quad \text{Rearrange to get} \quad \frac{W}{L}$$

$$\frac{W_{12}}{L_{12}} = \frac{KP(V_{DS12} + VT)^2}{2.ID} \quad ID = 10uA \quad \therefore$$

$$\frac{W_{12}}{L_{12}} = \frac{1.5035E^{-5}(5.79 + 0.889)^2}{2.10E^{-6}} = 0.11$$

ie $W = 1$ and $L = 9$

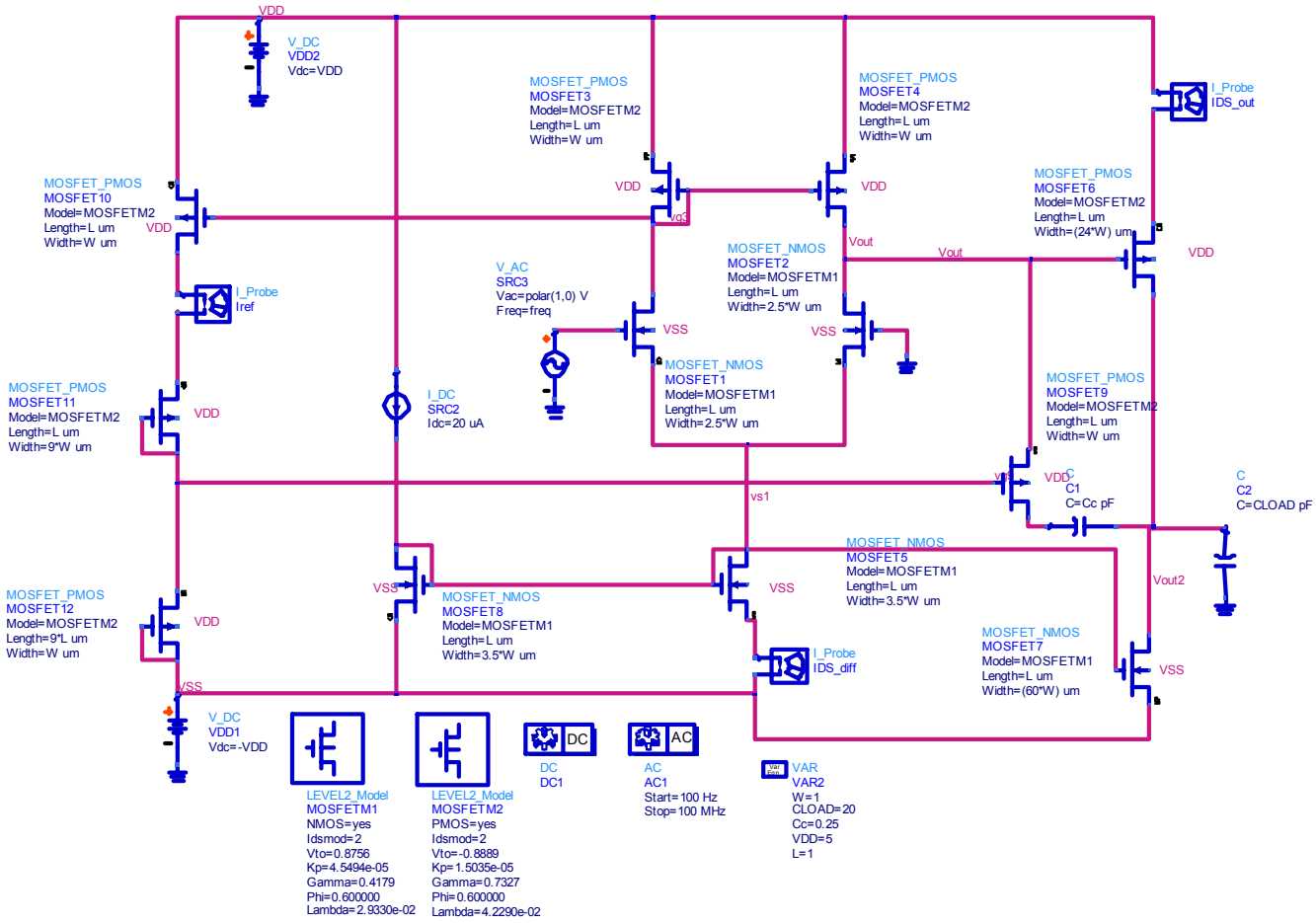
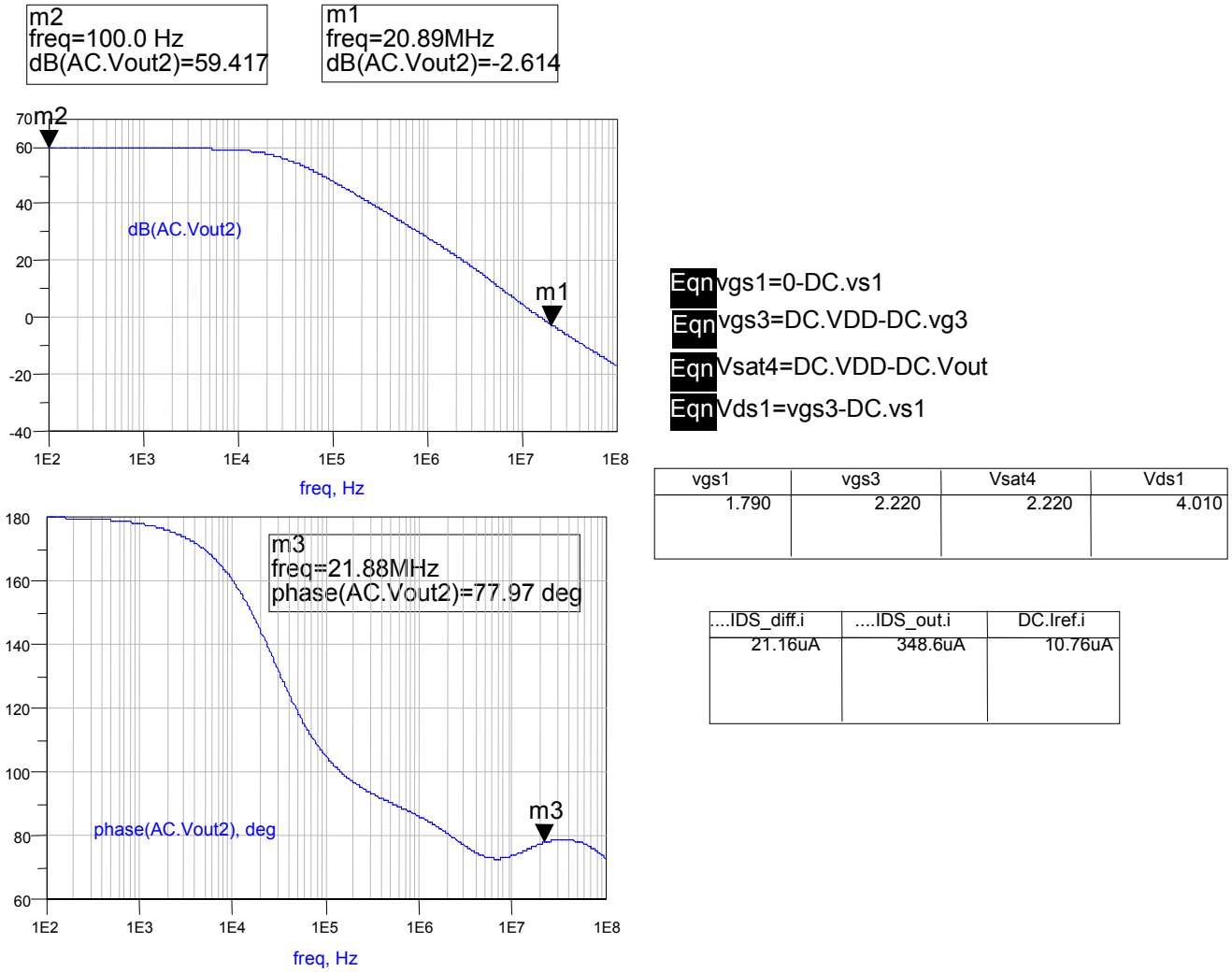


Figure 6 Completed Op-Amp circuit with MOSFET Rz in series with the Miller capacitor Cc. The devices of M10 – M12 set the correct bias to M9 to present a resistance of 122K in series with Cc.

The calculated values for the bias network, were added to the op-amp circuit as shown in **Figure 6**. This ADS circuit was analysed to predict the phase margin with the resulting plot of **Figure 7**. We can see that we have improved the phase margin of the amplifier to ~77 degrees by using the correctly biased P-type FET M9 to present a resistance Rz in series with the Miller capacitor Cc.

6 CONCLUSION

This tutorial has described use of a nulling resistor to cancel out the effects of the RHP zero to greatly improve phase margin when designing large gain bandwidth op-amps. The implementation of the nulling resistor using a MOSFET device in series with the Miller capacitor, together with it's biasing network was described.



vgs1	vgs3	Vsat4	Vds1
1.790	2.220	2.220	4.010

....IDS_diff.i	....IDS_out.i	DC.Iref.i
21.16uA	348.6uA	10.76uA

Figure 7 Simulation of the final op-amp circuit of Figure 6. The phase margin is now 78 degrees