# Power MOSFET Basics

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Power MOSFETs have become the standard choice for the main switching devices in a broad range of power conversion applications. They are majority carrier devices with no minority carrier injection, superior to Power Bipolar Junction Transistors (BJTs) and Insulated Gate Bipolar Transistors (IGBTs) in high frequency applications where switching power losses are dominant. They can be paralleled because the forward voltage drops with increasing temperature, ensuring an even distribution of current among all components. The major categories of Power MOSFETs are:

1. N-Channel Enhancement-Mode Power MOSFET
2. P-Channel Enhancement-Mode Power MOSFET
3. N-Channel Depletion-Mode Power MOSFET

N-channel enhancement-mode is the most popular for use in power switching circuits because of low on-state resistance compared to P-channel devices. An N-channel depletion-mode Power MOSFET differs from the enhancement-mode in that it is normally ON at 0V gate bias and requires a negative gate bias to block current [2].

Vertical DMOS Structure

A simplified vertical DMOS Power MOSFET with four layers of $n^+pn^-n^+$ structure is termed as N-Channel Enhancement-Mode Power MOSFET shown in Figure 1. A positive gate voltage (V_{gs}), higher than the gate threshold level ($V_{gs(th)}$) will create an n-type inversion channel under the gate oxide, connecting the source to the drain and allowing a current to flow. The gate threshold voltage is defined as the minimum gate bias required for creating the n-type inversion channel under the gate oxide. Power MOSFET has a parasitic BJT and an intrinsic body diode as integral parts of its structure as shown in Figure 1 [2].
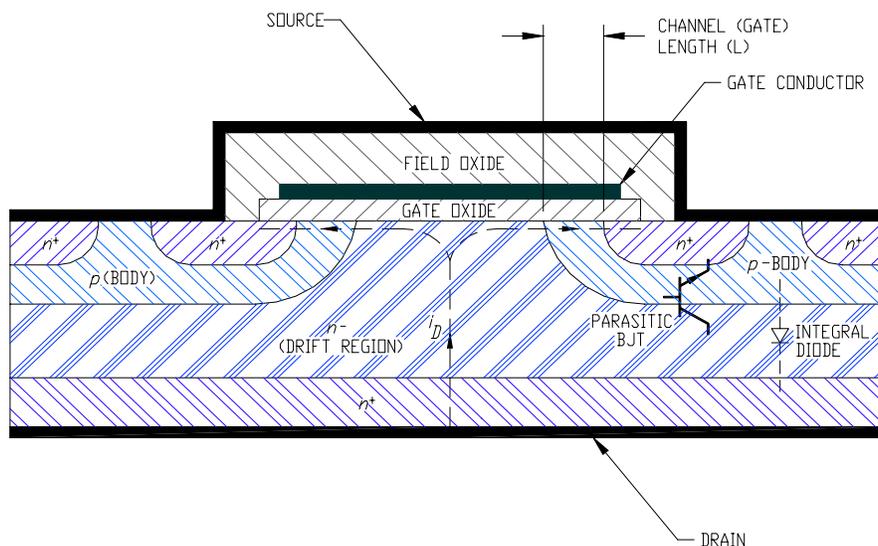
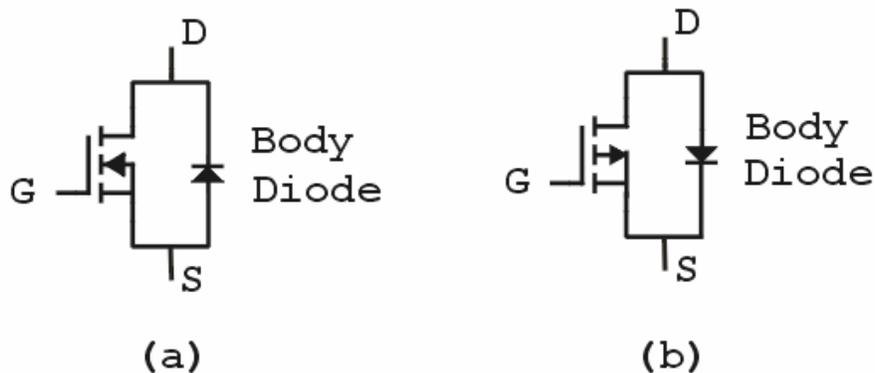**Figure 1**: N-Channel Enhancement-Mode Power MOSFET Structure [2]

Intrinsic Components
Parasitic BJT:
Power MOSFET has a parasitic BJT as an integral part of its structure as shown in Figure 1. The body region serves as the base, the source as the emitter and the drain as the collector. It is important to keep this BJT OFF of all times by keeping the potential of the base as close to the emitter potential as possible. This is accomplished by shorting the body and the source part of the MOSFET. Otherwise, the potential at the base would turn on the BJT and lead the device into the "latchup" condition, which would destroy the device [2].

Body Diode:
An intrinsic body diode is formed in the body-drain p-n junction connected between the drain and source as shown in Figure 1. Figure 2 shows the circuit symbols for both N-channel and P-channel enhancement types Power MOSFETs.

Figure 2: (a) N-channel (b) P-channel enhancement-mode Power MOSFET

The body diode is convenient in circuits that require a path for the reverse drain current (called "free wheeling current") such as half-bridge and full-bridge converter circuits in motor control applications [2].
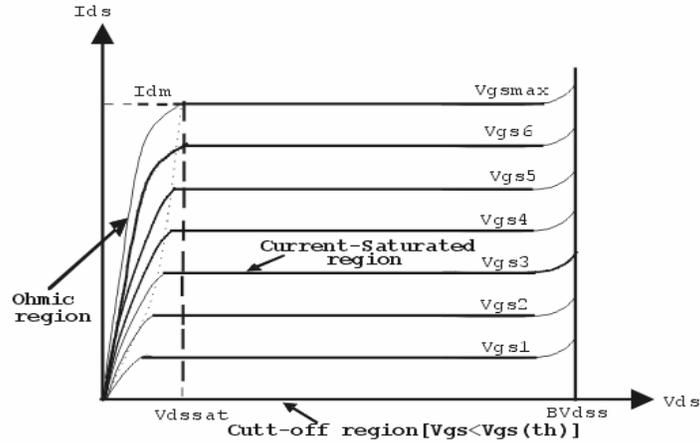
Power MOSFET Characteristics

Static Behavior
The static behavior is defined by the output characteristics, on-resistance, and the transconductance of the device.

Output Characteristics:
The output characteristics for an N-channel enhancement-mode Power MOSFET with the drain current (I_{ds}) as a function of drain-source voltage (V_{ds}) with gate-source voltage (V_{gs}) as a parameter are shown in Figure 3.

**Figure 3**: N-channel enhancement-mode Power MOSFET I-V Characteristics

It has regions labeled as Ohmic, Current-Saturated and Cut-off. In the Cut-off region, the gate-source voltage (V_{gs}) is less than the gate-threshold voltage ($V_{gs(th)}$) and the device is an open-circuit or Off. In the Ohmic region, the device acts as a resistor with almost a constant on-resistance, ($R_{DS(on)}$) defined by V_{ds} /$I_{ds.}$ In the current-saturated region, the drain current is a function of the gate-source voltage and defined by,

$$I_{ds} = K \bullet (V_{gs} - V_{gs(th)})^2 = g_{fs} \bullet (V_{gs} - V_{gs(th)}) \qquad \text{Equation (1)}$$

where K is a parameter depending on the temperature and device geometry and g_{fs} is the current gain or transconductance of the device. When the drain voltage (V_{ds}) is increased, the positive drain potential opposes the gate voltage bias and reduces the surface potential in the channel. The channel inversion layer charge decreases with increasing V_{ds} and ultimately, it becomes zero when the drain voltage equals to $(V_{gs} - V_{gs(th)})$. This point is called the channel pinch-off point where the drain current becomes saturated [2].

On-resistance $R_{DS\,(on)}$:
The on-resistance determines the conduction power dissipation and increases with increasing temperature as shown in Figure 4.
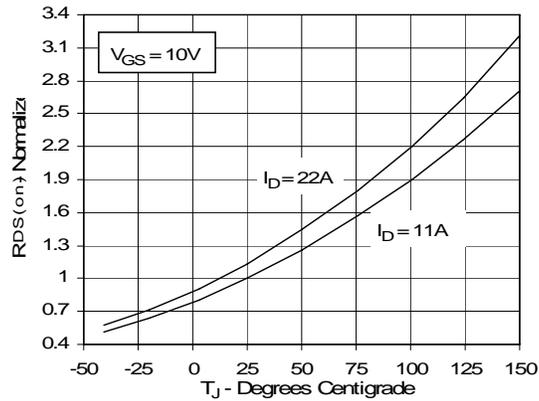
Figure 4: Increase on-resistance $R_{DS\,(on)}$ with temperature T_J for Power MOSFET

The on-resistance can be defined by,

$$R_{DS(on)} = R_{Source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml} \qquad \text{Equation (2)}$$

Where,

R_{Source} = Source diffusion resistance

R_{ch} = Channel resistance

R_A = Accumulation resistance

R_J = "JFET" component-resistance of the region between the two-body regions

R_D = Drift region resistance

R_{sub} = Substrate resistance

R_{wcml} = Sum of Bond Wire resistance, the Contact resistance between the source and drain metallization and leadframe contributions.

The temperature coefficient of $R_{DS\,(on)}$ is positive because of majority-only carrier movement. It is a useful property, which ensures thermal stability when paralleling the devices.

Transconductance g_{fs}:
The Transconductance is defined as the change in drain current divided by the change in gate voltage for a constant drain voltage:

$$g_{fs} = \frac{dI_D}{dV_{gs}}\Big|V_{ds=cons\tan t} \qquad \text{Equation (3)}$$

A large transconductance is desirable to obtain a high current handling capability with low gate drive voltage and for achieving high frequency response. A typical variation of transconductance as a function of drain current is shown in Figure 5. The reduction in the mobility with increasing temperature severely affects the transconductance of Power MOSFET.
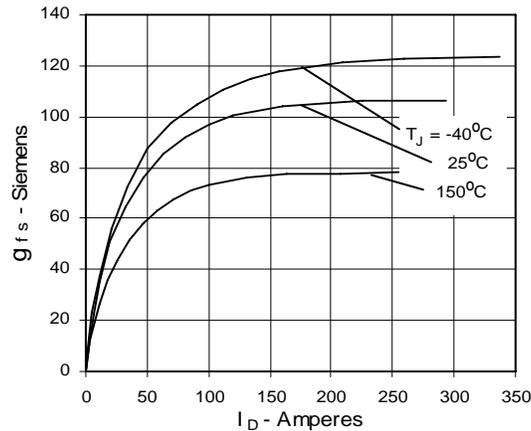
Figure 5: Transconductance vs the Drain Current [2]

Dynamic Behavior

The dynamic behavior is described by the switching characteristics of power MOSFET. The intrinsic capacitances, resistance, gate charge and the reverse recovery characteristics of the body diode play significant role in the dynamic performance of the device.

Intrinsic Capacitances:

Power MOSFET's dynamic behavior depends on the intrinsic resistance and capacitance, which has components as gate-to-source capacitance (Cgs), gate-to-drain capacitance (Cgd) and drain-to-source capacitance (Cds) as shown in Figure 6. The datasheet normally defines three parameters related to the intrinsic capacitances as.

Input capacitance, $\qquad C_{iss} = C_{gs} + C_{gd}$

Output capacitance, $\qquad C_{oss} = C_{ds} + C_{gd}$

Reverse transfer capacitance, $\qquad C_{rss} = C_{gd}$

**Intrinsic Resistance, Rg:**

The intrinsic resistance shown in Figure 6 is a part of the total gate resistance with external gate and driver resistances. It's omitted in IXYS datasheet because its value is much lower in magnitude and has very little influence on the switching time, which contributes the switching losses. Together with MOSFET input capacitance, the gate resistance forms an RC network that determines the voltage change at the MOSFET gate and thus the switching time.
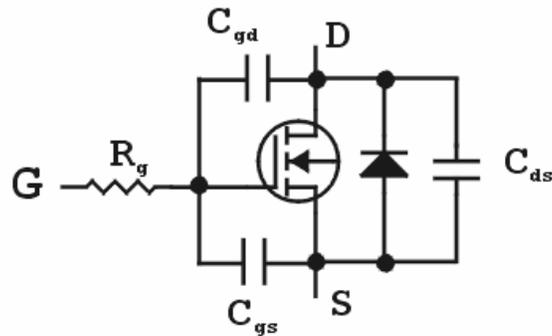
Figure 6: Power MOSFET parasitic components [2]

Gate Charge:
It's the amount of charge that is required during MOSFET's turn-on and turn-off transitions. The switching speed depends on the speed at which a gate driver can charge or discharge the input gate charge. A typical gate charge waveform for a Power MOSFET in a resistive-load circuit is shown in Figure 7.
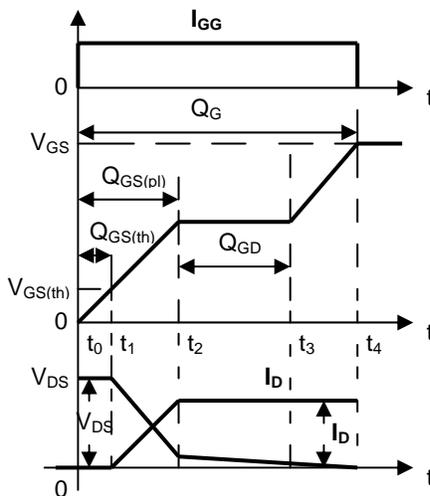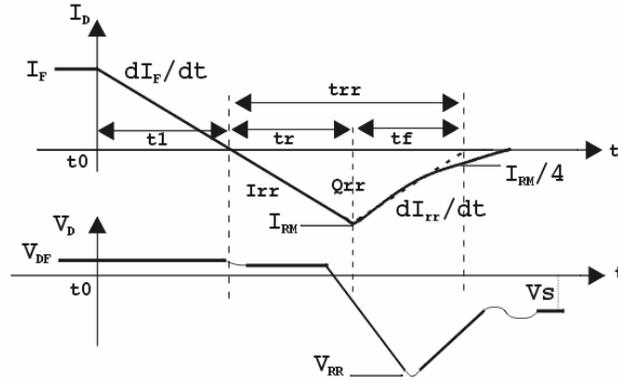

Figure 7: Basic gate charge waveform of Power MOSFET during turn-on transition with resistive load [4].

The basic equation to determine the gate charge is

$$Q_G = \int_{t0}^{t4} i_{GG}(t)dt$$ Equation (4)

Body Diode's Reverse Recovery Characteristics:
The body diode exhibits very slow reverse recovery with large reverse recovery current as shown in Figure 8.

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Figure 8: Typical reverse recovery waveforms for body diode in power MOSFET

The reverse recovery time is defined by $t_{rr} = t_r + t_f$. This time is also known as the storage time because it is the time that is taken to sweep out the excess charge, Q_{rr}.

Device Ruggedness

The ruggedness of Power MOSFET can be described by the following three major characteristics.

1. Avalanche Energy
2. Commutating dv/dt Capability
3. Forward-Biased Safe Operating Area (FBSOA) Capability

Avalanche Energy:

The avalanche condition arises when the voltage across the device exceeds its breakdown voltage. Two types of failures occur in this condition. The first failure called the "BJT latching", occurs when the current induces sufficient voltage across the device's internal base resistance (Rb) and turns-on the parasitic BJT. The second failure is thermally induced and occurs when the avalanche condition raises the device temperature sufficiently high over the rated maximum temperature.

The avalanched rated device is designed to be robust and tolerant of voltage transient in excess of their breakdown voltage. The latest technology manufactures devices in which the parasitic BJT is suppressed and the avalanche ruggedness is measured in terms of avalanche energy E_{AS}, E_{AR} and UIS (Unclamped Inductive Switching) test.
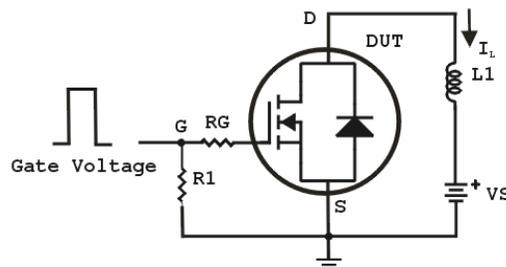
Figure 9: UIS test circuit for Power MOSFET ruggedness evaluation.

Figure 9 shows a test circuit for UIS. A gate pulse turns-on the MOSFET and allows the load current (I_L) to ramp up according to the inductor value (L1) and the drain supply voltage (Vs). At the end of gate pulse, the MOSFET turns-off and the current continues to follow causing the voltage across the MOSFET to rise sharply. The over voltage is clamped at the breakdown voltage (V_{BR}) until the load current reaches zero [1].

Commutating dv/dt Capability:
The Power MOSFET structure contains a parasitic BJT, which could be activated by an excessive rise rate of the drain-source voltage (dv/dt), particularly immediately after the recovery of the body diode. Good Power MOSFET design restricts this effect to very high values of dv/dt.

Forward Bias Safe Operating Area (FBSOA) Capability:
The FBSOA is a datasheet figure of merit that defines the maximum allowed operating points. Figure 10 shows a typical FBSOA characteristic for an N-Channel Power MOSFET. It is bounded by the maximum drain-to-source voltage V_{DSS}, maximum conduction current I_{DM} and constant power dissipation lines for various pulse durations. In this figure, the set of the curves shows a DC line and four single pulse operating lines, 10ms, 1ms, 100 µs and 25 µs. The top of each line is truncated to limit the maximum drain current and is bounded by a positive slope line defined by the $R_{ds\,(on)}$ of the device. The right hand side of each line is terminated at the rated drain-to-source voltage limit (Vdss). Each line has a negative slope and is determined by the maximum allowed power dissipation of the device P_d:

$$P_d = [T_{J\,(max)} - T_C] / Z_{thJC} = V_{DS}\, I_D \qquad \text{Equation (6)}$$

where Z_{thJC} is the junction-to-case transient thermal impedance and $T_{J\,(max)}$ is the maximum allowed junction temperature of the MOSFET.
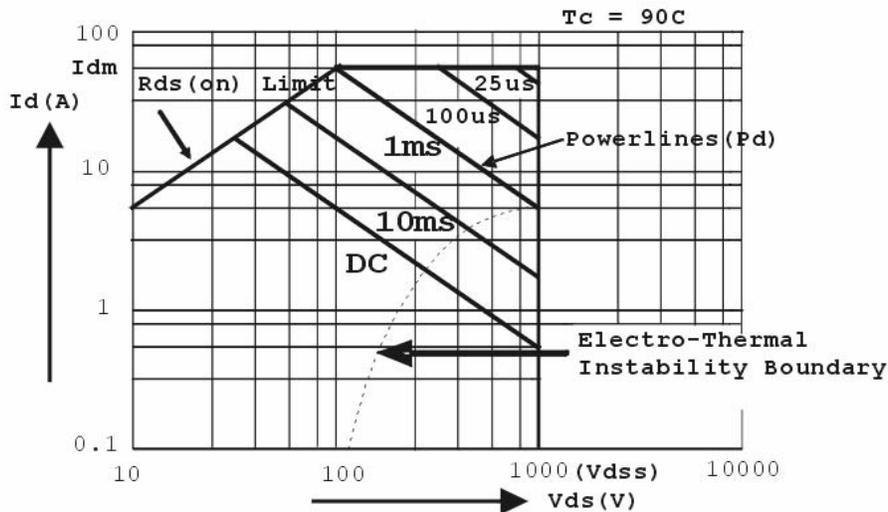
Figure 10: Typical FBSOA graph for an N-Channel Power MOSFET

These theoretical constant power curves are derived from calculation with assumption of essentially uniform junction temperature across the Power MOSFET die. This assumption is not always valid, especially for a large die MOSFETs. Firstly, the edge of a MOSFET die soldered to the mounting tab of a power package has generally lower temperature compared to the center of the die, the result of lateral heat flow. Secondly, material imperfections (die attach voids, thermal grease cavities, etc.) may cause local decrease of thermal conductivity, i.e. increase of local temperature. Thirdly, fluctuations in dopant concentrations and gate oxide thickness and fixed charge will cause fluctuations of local threshold voltage and the current gain (g_{fs}) of MOSFET cells, which will also affect local temperature of the die. Die temperature variations are mostly harmless in case of switched mode operation; however, these can trigger catastrophic failure in linear mode operation with pulse duration longer than time required for a heat transfer from the junction to the heat sink. Modern Power MOSFETs optimized for a switch-mode applications were found to have limited capability to operate in the right-side bottom corner of the FBSOA graph, the area to the right of the Electro-Thermal Instability boundary in Figure 10.

Electro-Thermal Instability (ETI) can be understood as a result of positive feedback mechanism on the surface of the Power MOSFET forced into linear mode of operation:
- There is a local increase of junction temperature;
- This causes local decrease of $V_{gs(th)}$ (MOSFET threshold voltage has negative temperature coefficient);
- This causes increase of local current density, $J_{ds} \sim (V_{gs} - V_{gs(th)})^2$;
- Increase of local current density causes increase of local power dissipation and further increase of local temperature.

Depending on the duration of the power pulse, heat transfer conditions and features of the design of MOSFET cells, the ETI may cause a concentration of all the MOSFET current into current filament and formation of a "hot spot". This normally causes MOSFET cells in that specified areas to loose gate control and turns on the parasitic BJT with consequent destruction of the device [3].

Thermal Behavior

Power MOSFET has junction temperature (T_J) limitation. It should be operated below the maximum junction temperature (T_{JM}) specified in the datasheet to ensure reliability. The heat generated within the silicon chip is typically dissipated by means of a heat sink into the ambient surroundings. The thermal system for a Power MOSFET with heat sink, which conveys the heat, can be represented as a network of thermal resistances and thermal capacitances as shown in Figure 11.
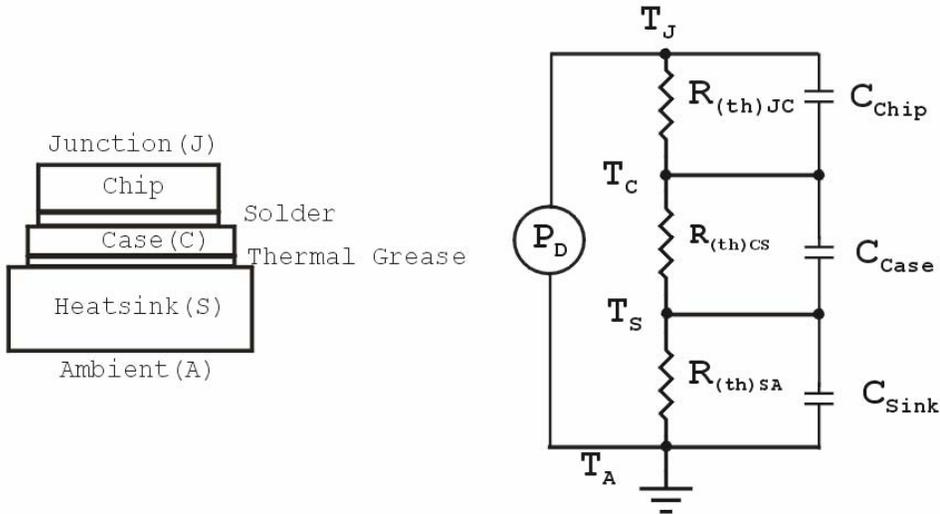
Figure 11: Power MOSFET Chip thermal model with simplified chip/heat sink system

The transient process involved in the transfer of heat through the chip and its heat sink, while simultaneously heating it, can be modeled in terms of the charging of the thermal capacitances through the thermal resistances. The heat generated at the junction flows through the chip to the case and then to the heat sink. The junction temperature rise above the ambient surrounding (T_A) is directly proportional to this heat flow and the junction-to-ambient thermal resistance (R_{thJA}). The steady-state junction temperature can be defined by:

$$T_J = P_D R_{(th)JA} + T_A \leq T_{JM} \qquad \text{Equation (7)}$$

where, P_D = Maximum power dissipated in the junction. The total thermal resistance between junction and ambient is,

$$R_{(th)JA} = R_{(th)JC} + R_{(th)CS} + R_{(th)SA} \qquad \text{Equation (8)}$$

The steady-state thermal resistance is not enough for finding peak junction temperatures for pulsed applications. When a power pulse applied to the device, the peak junction temperature varies depending on peak power and pulse width. The thermal resistance for junction-to-case at a given time is called transient thermal resistance and it is defined by:

$$Z_{(th)JC}(t) = r(t)R_{(th)JC} \qquad \text{Equation (9)}$$

where r(t) is a time dependent factor that defines the thermal capacity of the device. For short pulse, the r(t) value is small but for long pulse, it approaches 1 that means the transient thermal resistance approaches to steady-state thermal resistance. A typical transient thermal resistance curve is shown in Figure 12. It approaches the steady-state value at long pulse values. It can be used to estimate the peak temperature rise for square wave power pulses, which is typical in power supply design circuits [2].
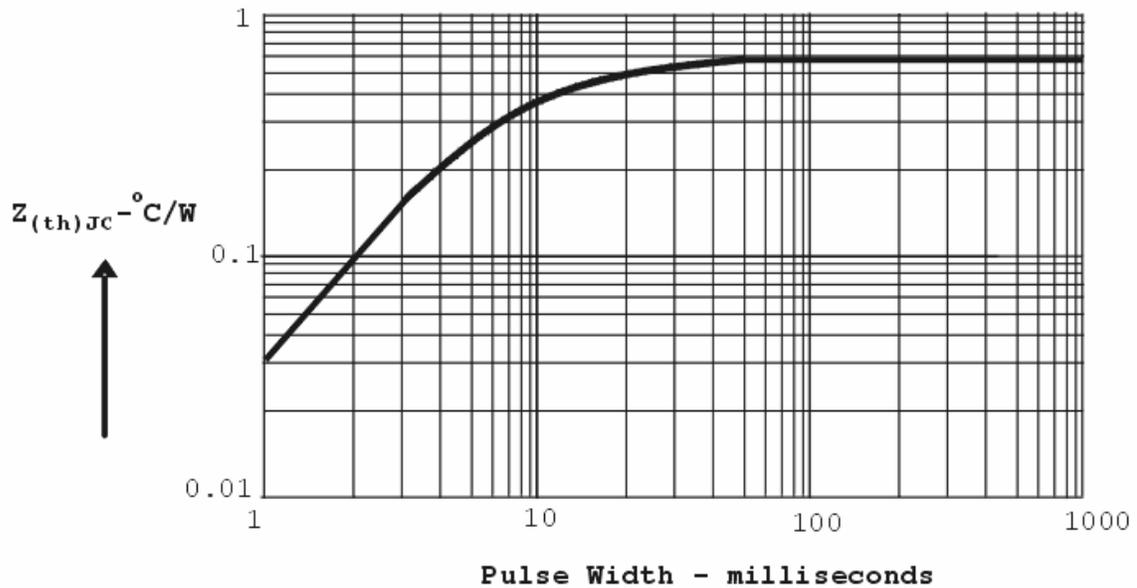
Figure 12: Transient thermal impedance curve for junction-to-case of an N-channel power MOSFET [2].

References:
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[2]   B. Jayant Baliga, "Power Semiconductor Devices" PWS Publishing Company, 1996.
[3]   Abdus Sattar, Vladimir Tsukanov, "Power MOSFETs for Linear Applications", Applications Note, IXYS Corporation, 2006.
[4]   "Discrete Semiconductor Devices—Part 8-4: Metal-oxide-semiconductor field-effect transistors (MOSFETs) for power switching applications" British Standard, BS IEC 60747-8-4:2004.