

Characterization of a Two-Stage Opamp

EE 415/515

Harry Li
University of Idaho

Table of Content

<u>Sections</u>	<u>Description</u>	<u>Page</u>
<i>Section 1.0</i>	Circuit Schematics	3
<i>Section 2.0</i>	DC Characteristics Measurements	4
2.1	Input Offset Voltage Measurement	4
2.2	Input Common Mode Range (CMR) Measurement	5
2.3	Output Voltage Swing (SWG) Measurement	6
<i>Section 3.0</i>	AC Characteristics Measurements	7
3.1	Open Loop Differential Gain (A_D) Measurement	7
3.2	Common Mode Rejection Ratio (CMRR) Measurement	10
3.3	Power Supply Rejection Ratio (PSRR) Measurement	12
3.4	Output Resistance (R_{OUT}) Measurement	14
<i>Section 4.0</i>	Transient Characteristics Measurement	16
4.1	Slew Rate Measurement	16
4.2	Phase Margin Measurement	18
<i>Section 5.0</i>	Equipment Used for the Laboratory Measurement	19
<i>Section 6.0</i>	Reference	19

I. Circuit Schematic

TWO STAGE OPAMP Laboratory Measurement

The two stage op amp characteristics were being measured in the laboratory. These measurements were then compared with *HSpice* simulations. The circuit schematic is seen in Fig. 1.

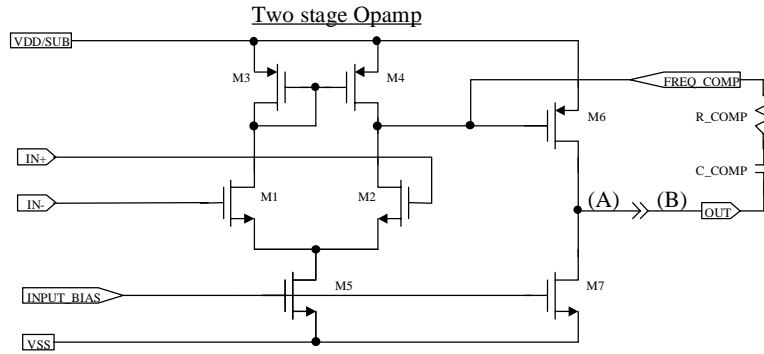


Figure 1 - Transistor level schematic ($C_{COMP} = 3 \text{ pF}$, $R_{COMP} = 5 \text{ K}$).

2.0 DC Characterization

2.1 DC Offset Voltage Measurement

Test Procedure:

1. Set up the unity-gain-feedback op amp circuit shown in Figure 2.1a.

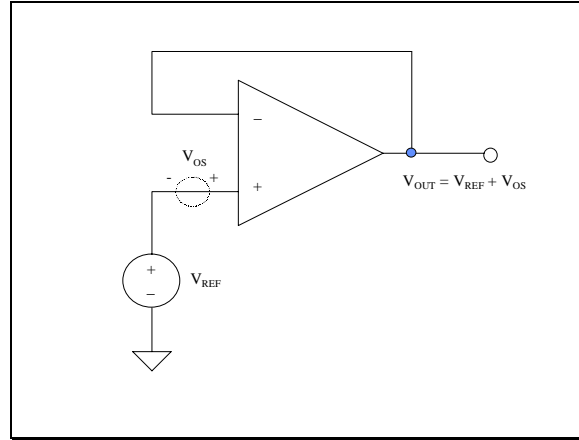


Figure 2.1a: Input Offset Voltage Measurement Circuit

2. Set V_{REF} at 5V.
3. Measure the V_{OUT} and V_{REF} using a Digital Multimeter (DMM).
4. Calculate the offset voltage, V_{OS} using **(Eq. 2.1)**:

$$V_{OS} = V_{OUT} - V_{REF} \quad \text{(Eq. 2.1)}$$

5. Continue to calculate V_{OS} for other V_{REF} values.

The V_{OS} measurement results are tabulated in Table 2.1. V_{OS} was then averaged over all these measurements of V_{OS} .

2.2 Input CMR Voltage Measurement

Test Procedure:

1. Setup the non-inverting unity-gain op amp circuit shown in Figure 2.2a.

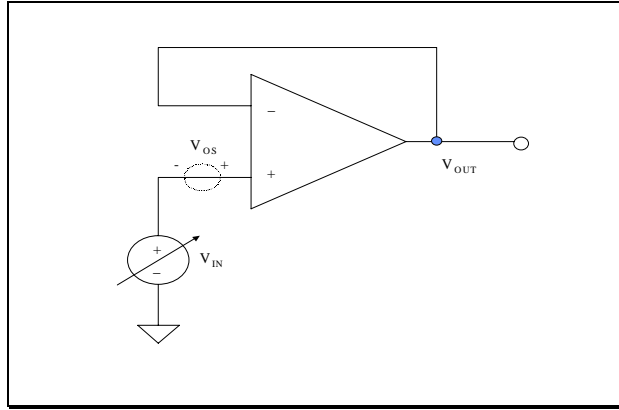


Figure 2.2a: Input CMR Voltage Measurement Circuit

2. Vary V_{IN} from 0 to 5V with $\approx 0.1V$ step.
3. For each V_{IN} , record the corresponding V_{OUT} using the DMM.
4. Plot V_{OUT} versus V_{IN} . The linear range of V_{OUT} versus V_{IN} is the CMR.

The results from the CMR simulations, as depicted in Figure 2.2b.

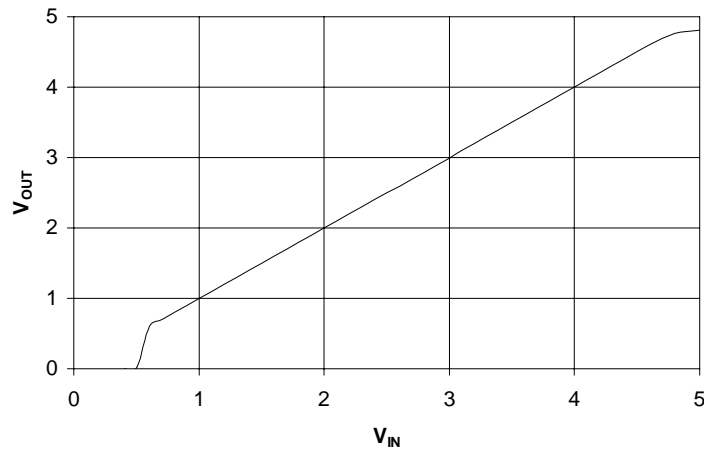


Figure 2.2b: Simulated Input Common Mode Range (CMR)

2.3 Output Swing SWG Measurement

Test Procedure

1. Setup the inverting gain op amp circuit as shown in Figure 2.3a.
2. Choose a gain of 10 V/V for the op amp circuit. This is to ensure that the output voltage clipping is due to SWG, and not CMR. Also select values for R and $10R$ to be sufficiently large so as not to strain the current sinking and sourcing capabilities of the op amp. The measured values for the selected R and $10R$ were $98.3\text{k}\Omega$ and $992\text{k}\Omega$, respectively.

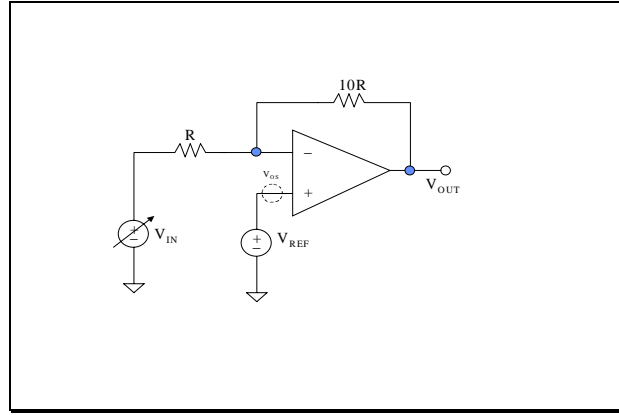


Figure 2.3a: Output Swing Voltage Measurement Circuit

3. Set V_{REF} to 2.5V.
4. Vary V_{IN} from 2V to 4V with $\approx 0.1\text{V}$ step.
5. For each V_{IN} , record V_{IN} and corresponding V_{OUT} using the DMM.
6. Plot V_{OUT} versus V_{IN} . The range of V_{OUT} is the SWG.

Figure 2.3b shows the simulated results of the SWG.

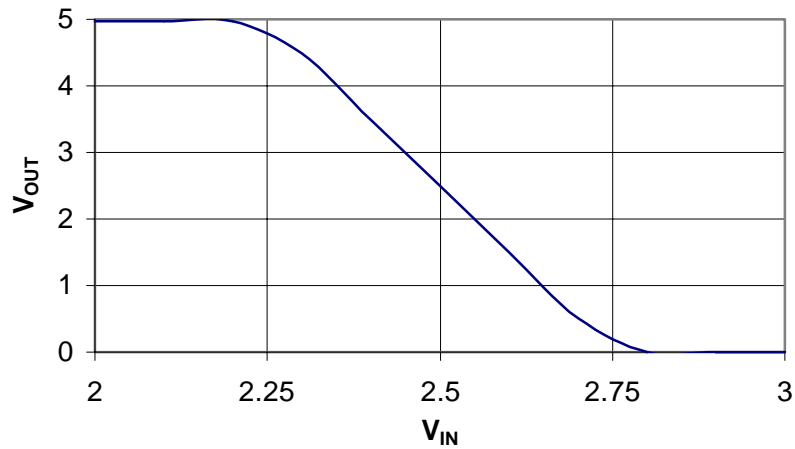


Figure 2.3b: Simulated Output Voltage Swing (SWG).

3.0 AC Characterization

3.1 Open Loop Differential Gain, A_D , Measurement

Test Procedure

1. Setup the circuit shown in Figure 3.1a.
2. Configure for A_D measurement.
3. Offset-null the CA3140 op amp of the unity gain buffer in the feedback loop. This buffer prevents feedforward of the input signal as well as loading effect of the feedback resistors. The CA3140 is a 4.5MHz, BiCMOS Op Amp with MOSFET Input/Bipolar Output.

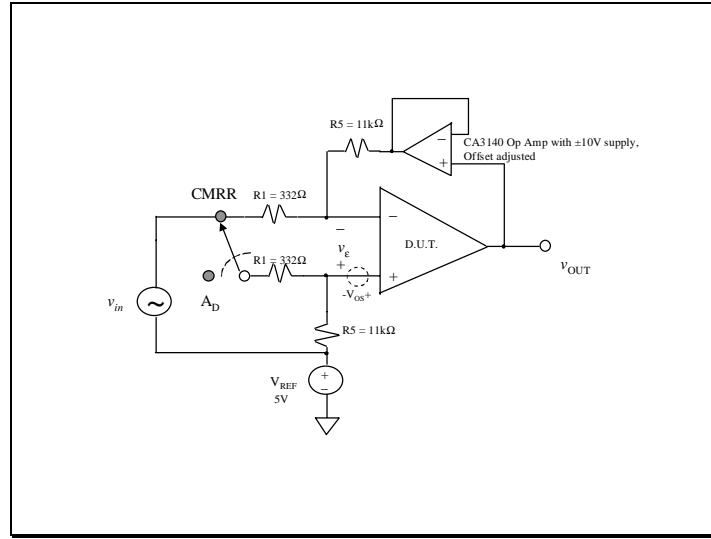


Figure 3.1a: Open Loop Differential Gain and CMRR Measurement Circuit

4. Using a function generator, generate the signal v_{in} and set the amplitude of v_{in} to be 0.02V peak. Remember to DC offset v_{in} by $V_{REF} = 5.0V$.
5. Vary the frequency of v_{in} exponentially from 10Hz to 2MHz
6. Using the oscilloscope, measure the peak-to-peak amplitude of v_{out} and v_e for each frequency of v_{in} . Use the autoranging and average features of the oscilloscope to get a better reading.
7. Because v_e is too small, amplify v_e before taking its measurements. For this purpose, a “500^{V/V} closed loop gain” differential input amplifier (as shown in Figure 3.1b on the next page) is built. The output of amplifier of Figure 3.1b is given as follows:

$$v_{OUT}(\text{of Figure 3.1b}) = 2 \frac{R1}{R} \frac{R3}{R2} (v_2 - v_1) \quad (\text{Eq. 3.1})$$

8. Knowing the amplitudes of v_{out} and v_e , calculate A_D using:

$$A_D = 20 \log_{10} \left(\frac{v_{out}}{v_e} \right) \text{ [dB]} \quad (\text{Eq. 3.2})$$

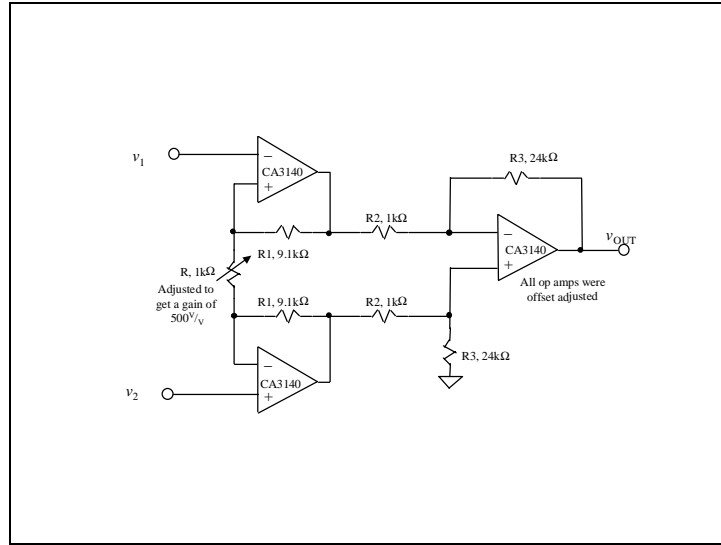


Figure 3.1b: Differential Input Voltage Amplifier

9. Plot the A_D versus frequency in a semilog plot.

Figure 3.1c shows the simulation results.

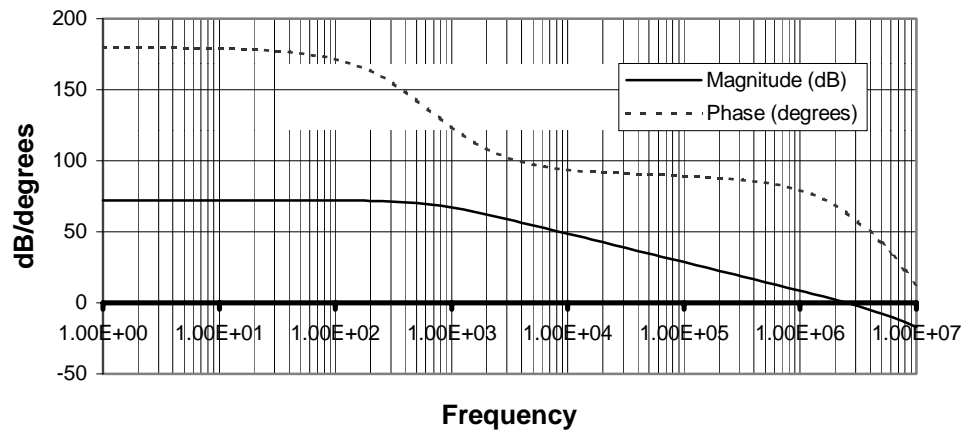


Figure 3.1c: Simulated Open Loop Differential Gain and Phase.

Measurement Accuracy Limitations:

- The open loop gain of the CA3140 decreases with frequency. This causes the unity gain buffer in the feedback loop to deviate from the ideal “ $1^V/V$ ” over frequency. For example, A_D for CA3140 at 10Hz is 100dB. At 40kHz, the A_D drops to 40dB and at 400kHz, its value is 20dB.
- Limited accuracy of the measurement instruments, e.g., the oscilloscope only has voltage per division of 20mV/DIV.
- The ideal “500V/V gain” of the differential input amplifier decreases with frequency. For more accurate measurements, the closed-loop gain of the differential input amplifier was characterized as shown Figure 3.1d. From this characterization, the amplification factor of v_e over frequency can be determined.

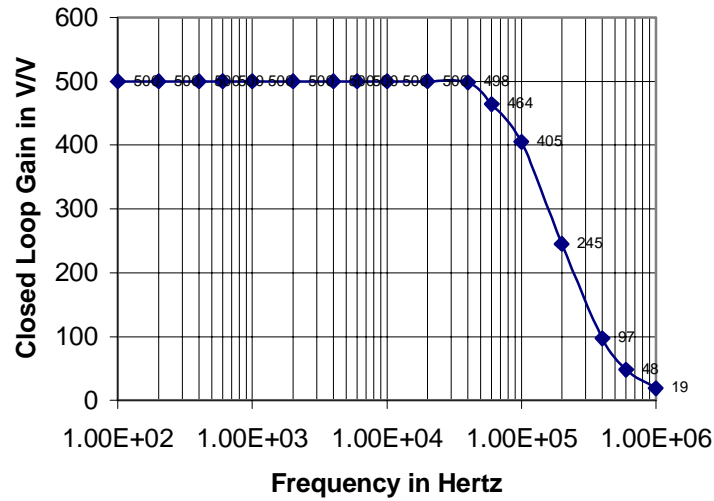


Figure 3.1d: Characterization of the Closed-Loop Gain of the Differential Input Amplifier

3.2 CMRR Measurement

Test Procedure

- 1 Setup the circuit shown in Figure 3.1a.
- 2 Configure for CMRR measurement.
- 3 Using a function generator, generate the signal v_{in} and set the amplitude of v_{in} to be ¹0.2V peak. Remember to DC offset v_{in} by $V_{REF} = 2.5V$.
- 4 Vary the frequency of v_{in} exponentially from 10Hz to 1MHz
- 5 Using the oscilloscope, measure the peak-to-peak amplitude of v_{out} and v_{in} for each frequency of v_{in} . Use the autoranging and average features of the oscilloscope to get a better reading. Amplify v_{out} if it is too small to measure, especially at lower frequencies. In this case, use the “500^V/_V closed loop gain” differential input amplifier.
- 6 From the measured v_o and v_{in} , calculate the CMRR as follows:

The output voltage of the circuit of Figure 3.1a configured for CMRR measurement can be expressed in terms of the differential gain, A_D , common mode gain, A_{CM} , and the input voltage of the op amp. This is shown in **(Eq. 3.3)**:

$$v_o = A_D(v_+ - v_-) + A_{CM}\left(\frac{v_+ + v_-}{2}\right) \quad (\text{Eq. 3.3})$$

Substituting the values of v_+ and v_- into **(Eq. 3.3)**, the **(Eq. 3.4)** follows:

$$\frac{A_{CM}}{2} = \frac{\frac{v_o}{v_{in}} - A_D\left(K1 - K2 - \frac{v_o}{v_{in}} \cdot F \cdot K3\right)}{K1 + K4 + \frac{v_o}{v_{in}} \cdot F \cdot K3} \quad (\text{Eq. 3.4})$$

where

$$K1 = \frac{R_5}{R_5 + R_1} \quad K2 = \frac{R_5 + R_B}{R_5 + R_1 + R_B}$$

$$K3 = \frac{R_1}{R_5 + R_1 + R_B} \quad K4 = \frac{R_5}{R_5 + R_1 + R_B}$$

$$F = \frac{1}{1 + \frac{1}{A_{OL}}}$$

R_B is the output resistance of the CA3140, which is found to be 60Ω from the data sheet. Besides that, A_{OL} is the open loop differential gain of the CA3140 over frequency obtained from the data sheet.

Finally, the CMRR was obtained from the following relationship:

¹ Difficulty in reading small values of v_{out} requires v_{in} to be set at larger amplitude.

$$CMRR = \frac{A_D}{A_{CM}} \quad (\text{Eq 3.5})$$

Because of the extensive calculations involved, a MATLAB program was written to do the calculation loads. All of the above equations are reference from [1].

10. Plot CMRR versus frequency in a semilog plot.

Figure 3.2a compares the measured and the simulated CMRR.

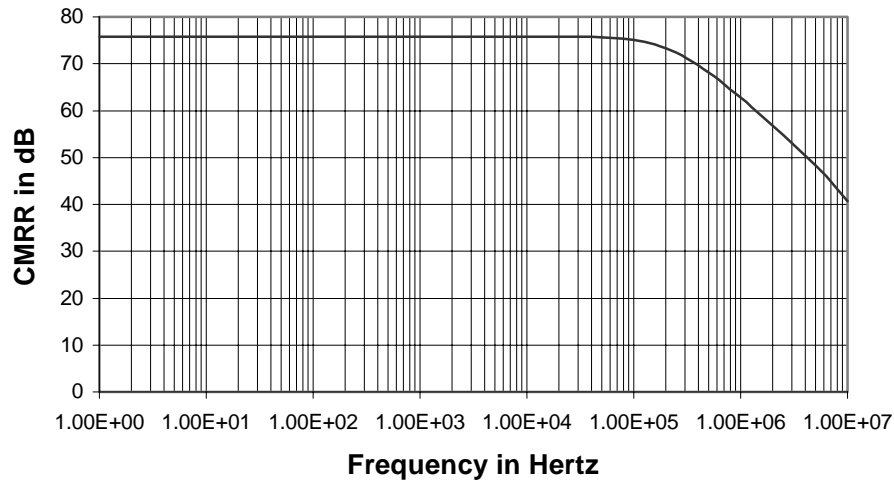


Figure 3.2a: Simulated CMRR

Possible Causes of Differences in Measurement and Simulation Data:

- SPICE does not model errors due to mismatch such as those caused by process gradient and geometrical considerations (such as noncommon-centroid layout).
- The measurements are limited by the precision of the resistors used in the measurement.

3.3 Power Supply Rejection Ratio, PSRR, Measurement

Test Procedure

1. Setup the circuit shown in Figure 3.3a.

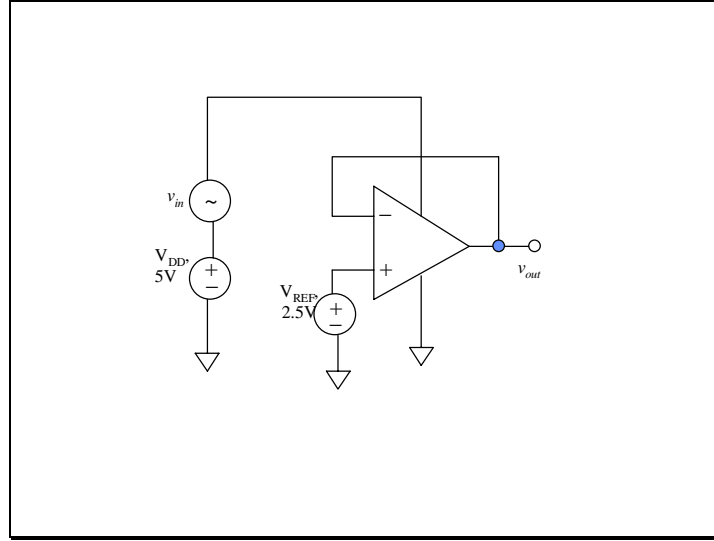


Figure 3.3a: PSRR Measurement Circuit

2. Using a function generator, generate the signal v_{in} and set the amplitude to ²0.1V peak. Connect v_{in} in series with the power supply, $V_{DD} = 5V$.
3. Vary the frequency of v_{in} exponentially from ³120Hz to 6MHz.
4. Using the oscilloscope, measure the peak-to-peak amplitude of v_{out} and v_{in} for each frequency of v_{in} . Use the *average* and *autoranging* features of the oscilloscope to get a better reading. Amplify v_{out} if it is too small to measure, especially at lower frequencies. In this case, use the “500^V/V closed loop gain” differential input amplifier.
5. From the measured v_o and v_{in} , calculate PSRR as follows:

$$PSRR = 20 \log_{10} \left(\frac{v_{in}}{v_{out}} \right) \text{ [dB]} \quad (\text{Eq. 3.6})$$

6. Plot the PSRR over frequency in semilog plot.

² Difficulty in measuring v_{out} requires v_{in} to be set at larger amplitude.

³ Problems were accounted for lower frequency measurements because “ground-loop signals at 60Hz” terribly corrupt the output voltage measurements.

The simulated results are shown in Figure 3.3b.

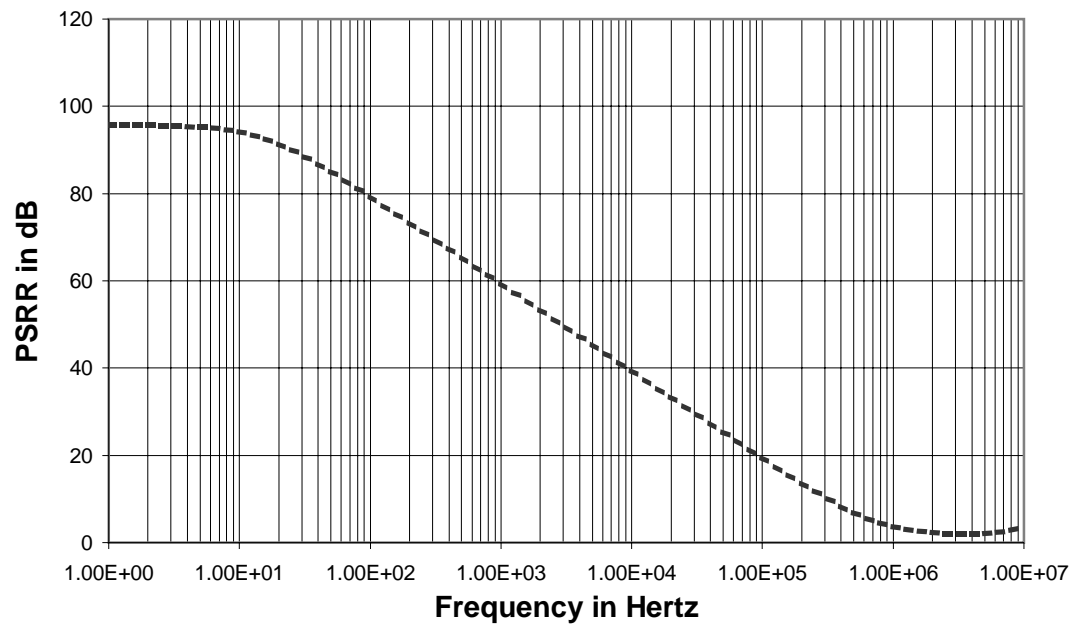


Figure 3.3b: Simulated PSRR

3.4 Output Resistance Measurement

Test Procedure

1. Setup the circuit shown in Figure 3.4a.

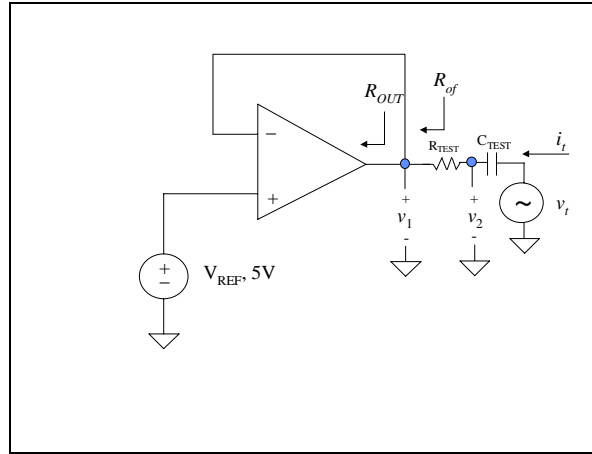


Figure 3.4a: R_{OUT} Measurement Circuit

2. Using a function generator, generate the signal v_{in} and set its amplitude to be 0.2V peak. Repeat steps 2 through 6 as the frequency of v_{in} is varied exponentially from ⁴10Hz to 1MHz.
3. Determine the rms value of i_t by placing a test resistor in series between the output of the op-amp and v_{th} and measuring the voltage drop across the test resistor. The capacitor C_{TEST} is used to AC couple the test signal into the op-amp's output and should be large (greater than 10 μ F). Ensure that the test resistor is large enough to generate an AC voltage across it that can be resolved by the o-scope or DMM.
4. For each frequency of v_{in} , measure the rms of v_1 using an averaging scope or a DMM. The voltage v_1 may need to be amplified if too small to observe.
5. Calculate the output resistance of the closed-loop amplifier, R_{of} , using the following:

$$R_{of} = \frac{v_1}{i_t} \quad (\text{Eq. 3.7})$$

6. Since this amplifier configuration uses shunt feedback sampling in the output, the true output impedance of the amplifier is the open-loop value designated as R_{OUT} , and is found by multiplying R_{of} by $(1 + A\beta)$. The value A is the open-loop gain at that frequency and β is the feedback factor, which in this case, is one.

⁴ Problems were accounted for lower frequency measurements because "ground-loop signals at 60Hz" terribly corrupt the output voltage measurements.

Figure 3.4b illustrates the simulated R_{OUT} .

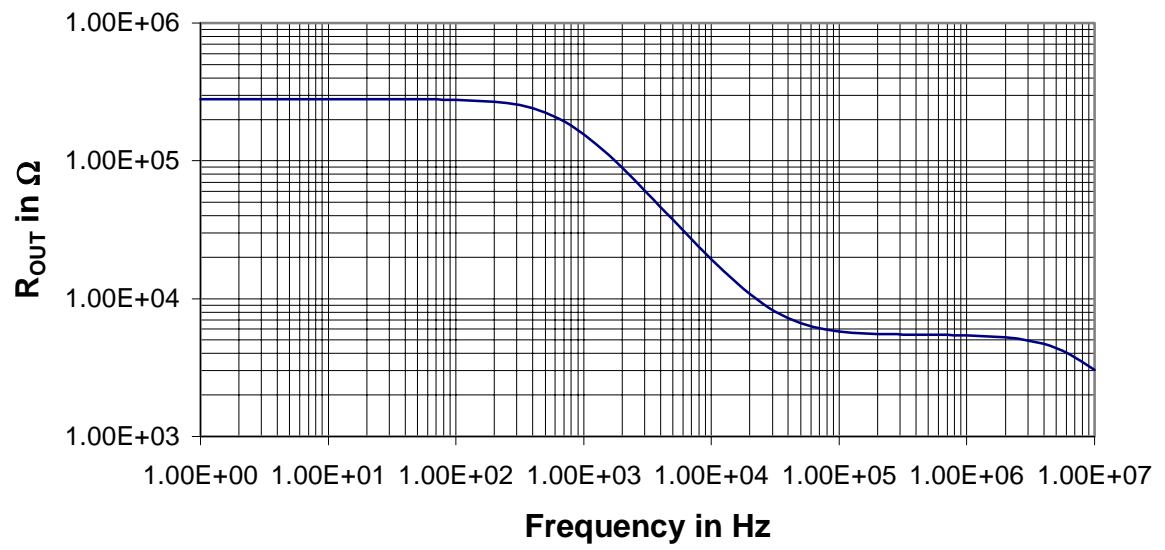


Figure 3.4b: Simulated R_O .

4.0 Transient Characteristics

4.1 Slew Rate Measurements

Test Procedure

1. Setup the non-inverting unity-gain op amp circuit shown in Figure 3.4a.

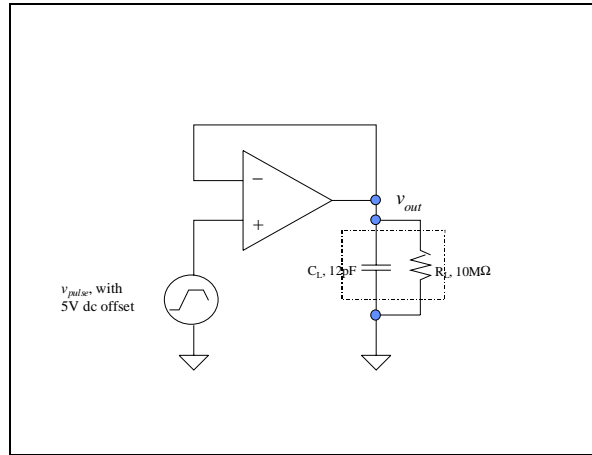


Figure 4.1a: Measurement Circuit for Transient Response

2. Generate the signal v_{pulse} using a function generator and set the amplitude to swing -2V to 2V , dc offset by 2.5V .
3. Using an oscilloscope, measure the slew rate of the output voltage, v_{out} . The observed v_{out} should look like in Figure 4.1b.

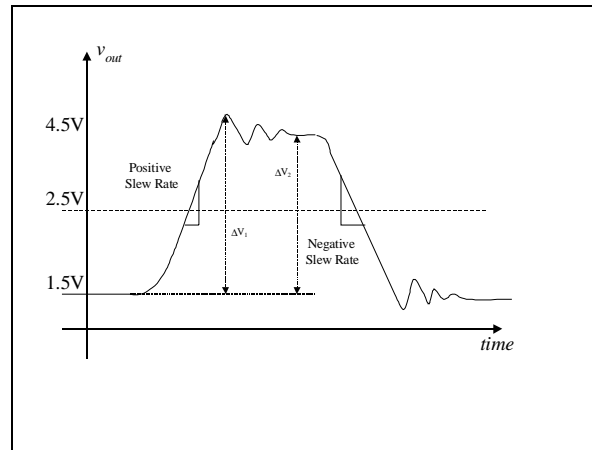


Figure 4.1b: Observed Transient Response of v_{out}

The measured slew rates are compared to the Level 3 and Level 49 simulations, as tabulated in Figure 4.1c & d.

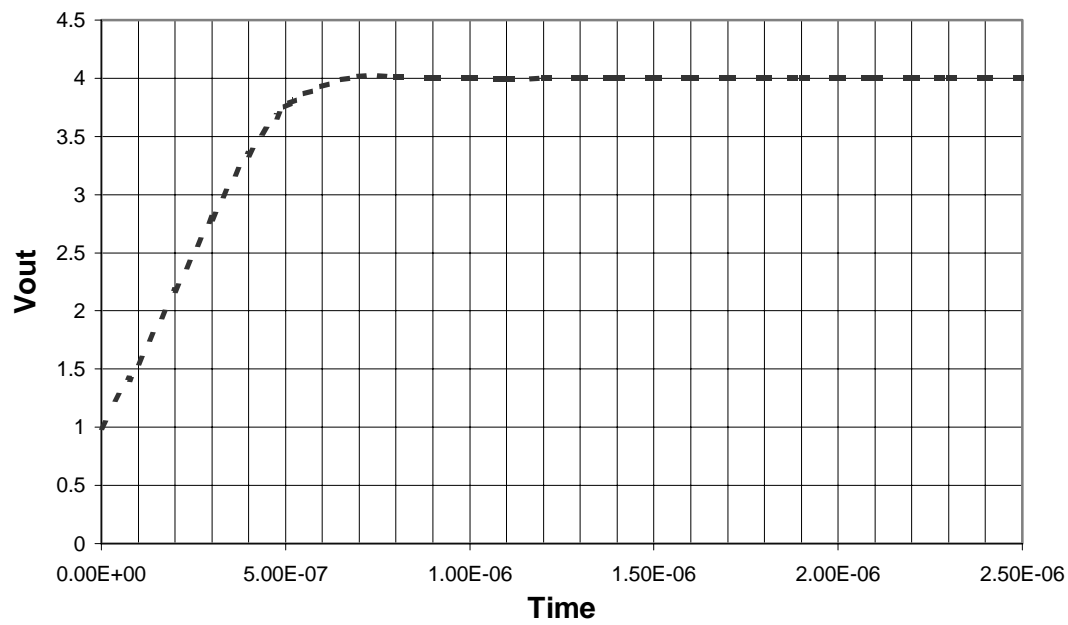


Figure 4.1c: Simulated Positive Slew Rate

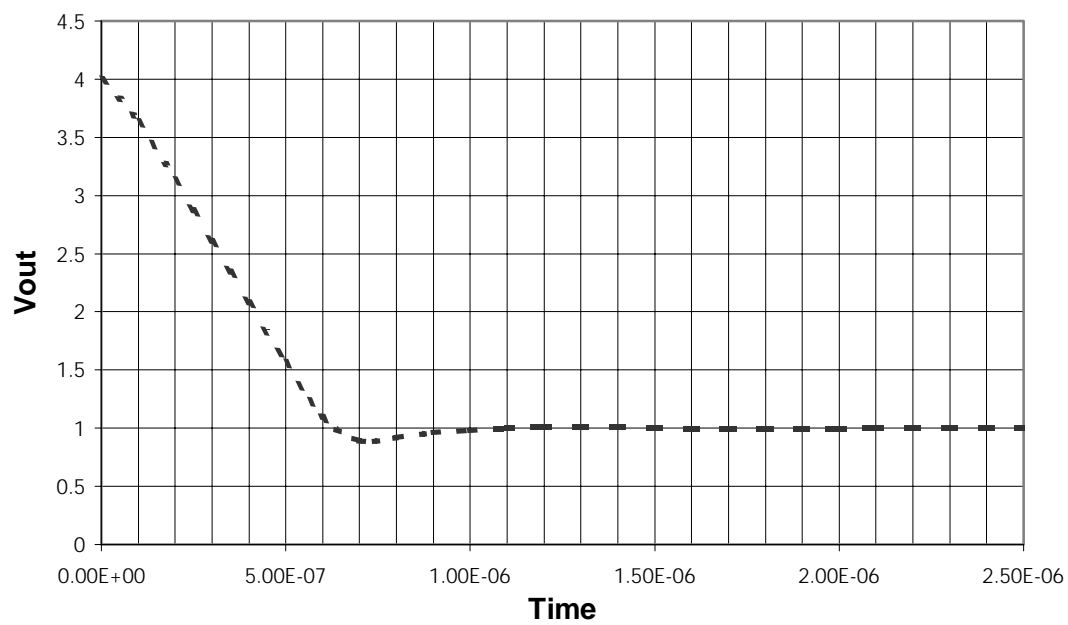


Figure 4.1d: Simulated Negative Slew Rate

4.2 Phase Margin based on Overshoot Measurements

Test Procedure

1. Use the same circuit setup as in Figure 4.1a.
2. Generate the signal v_{pulse} using a function generator and set the amplitude to swing 5V to 6V, i.e., a 1V step input with reference to 5V. Be sure that v_{pulse} is not too large to cause the devices to be non-linear.
3. Using an oscilloscope, measure the overshoot of the output voltage, v_{out} .
4. From the measured overshoot, the phase margin of the op amp can be approximated assuming the transient response is that of a second order system [1].
5. For phase margin calculations, use the following:

$$Percentage\ Overshoot = e^{\frac{-\pi\xi}{\sqrt{1-\xi^2}}} \quad (\text{Eq. 4.1})$$

$$\Phi_M = \tan^{-1} \left\{ 2\xi \sqrt{\frac{1}{\sqrt{4\xi^4 + 1} - 2\xi^2}} \right\} \quad (\text{Eq. 4.2})$$

The overshoot measured was 19.75% and $\xi=0.4588$, resulting in a measured phase margin of 48.4°.

5.0 Laboratory Equipment Used

1. Philips PM5139 Function Generator, 0.1mHz ~ 20MHz
2. Hewlett Packard E3631A 0 ~6V, 5A / 0 ~ ± 25 V, 1A Triple Output DC Power Supply
3. Fluke 8842A Multimeter
4. Fluke PM3380A Autoranging Combiscope 100MHz

6.0 Reference

- [1] Willy M. C. Sansen, "Measurement of Operational Amplifier Characteristics in the Frequency Domain", *IEEE Transactions on Instrumentation and Measurements*, Vol. 1M-34, No. I, March 1985.