# Sr. Layout Engineer Resume

★★★★★ 3.00 /5 (Submit Your Rating)

## SUMMARY

- Hands - on experience in IC MASK Design, verification using Cadence Virtuoso-XL/Opus, Assura & Dracula DRC/ LVS, Encounter, Calibre DRC/LVS and Magic.
- Hands-on experience in Cadence SKILL programming, C, Perl and UNIX shell scripts.
- Knowledge of CMOS process concepts and layout techniques, Latch-up theory and prevention techniques, ESD and protecting techniques
- Floor planning concept, matching, noise, high frequency issues, Bipolar and analog circuits.
- Knowledge of Verilog HDL and UNIX Operating system.
- Extensive training in IC Mask Design using Cadence OPUS, Cadence SKILL programming.
- Strong desires to learn and explore new technologies.

## PROFESSIONAL EXPERIENCE

**Sr. Layout Engineer**

**Confidential**

**Responsibilities:**

- Implemented analog custom layout including 4G PLL, Continues Time Linear Equalizer, Slicer, Phase Interpolator and Serial to Parallel converter.
- Implemented Bandgap reference.
- Implemented analog custom layout including 12 bit SAR ADC, Charge integrator, Analog Filter, LDO and TX/RX buffer.

**Sr. Mask Design Contractor**

**Confidential**

**Responsibilities:**

- Implemented analog custom layout including PLL, output driver and digital interface.
- Implemented layout porting from different projects.

**Sr. Mask Design Contractor**

**Confidential**

**Responsibilities:**

- Implemented analog custom layout includi[illegible]DO, DAC, low noise FGA, Input/output buffers, etc.



**Sr. Mask Design Consultant**

**Confidential**

**Responsibilities:**

- Verification rule decks, PDK installation and edition.
- Setup QRC for parasitic extraction and building Pcells such as Guard-rings.
- Building standard cell library.
- Implemented adpll layout including LDO, XO, Input/output buffers,
- Bandgap, high speed output divider, etc.
- Integration and tape out for a parallel optics 4-channel transceiver.

**Sr. Mask Design Engineer**

**Confidential, Los Altos, CA**

**Responsibilities:**

- Worked on a large family of standardized and full-custom PLL and DLL hard macros
- CMOS processes from 130nm to 28 nm and for leading-edge foundries such as TSMC, Global Foundry and NEC.
- Implemented analog/mixed-signal layout design of PLLs and DLLs.
- Manipulated layout CAD flows with shell scripts.
- Implemented PLL and DLL porting for different technologies.

**Sr. Mask Design Engineer**

**Confidential, San Jose, CA**

**Responsibilities:**

- In depth understanding of RFIC design requirement.
- Built custom layout to match devices, shield critical signals to ground line for noise reduction.
- Implemented PLL layout including voltage reference, phase detector, charge pump, VCO, ESD device, bonding pads and bus planning.
- Built custom layout of various analog devices including Mixer, LNA, IF filter, power amplifier, DAC, bandgap, etc.
- Implemented top level chip integration and tape out activities.
- Proficient in SKILL programming, provided SKILL routines for layout and schematic library search and layout automation.
- Building Pcells such as Guard-ring and stacked via, etc.
- Implemented SKILL routines for layout and schematic library checking, schematic tree search, and floating gate checking, etc.
- Implemented DRC rule files.

**IC Layout Designer**

**Confidential, Sunnyvale, CA**

**Responsibilities:**

- Performed CMOS IC layout design in 0.18um & 0.35um technology using Cadence OPUS, Dracula, Mentor Calibre and Hercules.
- Built custom layout of the various SRAM leaf cells including row decoder, column decoder, Read/Write circuits, and peripheral interface cells etc.
- Proficient in Standard Cell Layout: complex logic gates, D flip-flops, latches, storage registers and tri-state buffers, etc.

**Software Engineer**

**Confidential, San Jose, CA**

**Responsibilities:**

- Worked on the Secure A-Key Management System (SAMS) which enable wireless service providers to securely manage the secret keys for the authentication process using C, Java, PL/SQL, perl, and shell scripts in the UNIX environment.
- Studied and developed deposition mechanism and technique of Electron Cyclotron Resonance Microwave Plasma Chemical Vapor Deposition (ECR-MPCVD) Silicon Nitride in LSI thin-film technology.