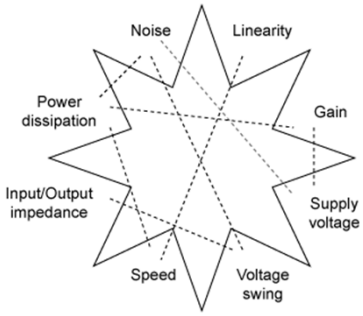
Analog design trade-offs

- Analog design octagon



- Balancing performance with real devices

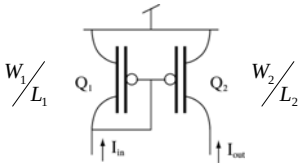
Current mirrors

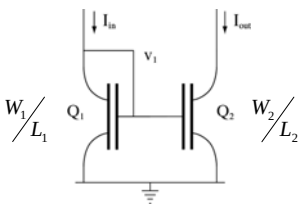
- Large signal behavior
  - Current controlled current source
    - Equal transistor sizes with same gate voltage
      - Give same current

$$I_{out} = I_{in}$$

        - » Sink or source
      - Assuming active region
      - Ignoring channel shortening
  - Fixed gain current amplifier
    - Different transistor sizes

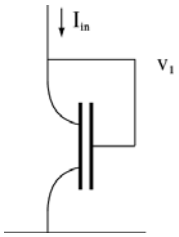
$$I_{out} = \frac{W_2 L_1}{W_1 L_2} I_{in}$$





Diode connected MOS transistor

- Shorting drain-gate
  - V-I relation
    - Strong inversion
    - Active region by connection
    - Ignoring channel shortening



$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{tn}\right)^2 \Rightarrow$$

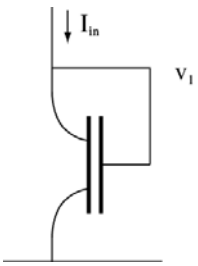
$$\left(V_{GS} - V_{tn}\right)^2 = \frac{2}{\mu_n C_{ox}\left(W/L\right)} I_D \Rightarrow$$

$$V_{GS} = V_{tn} + \sqrt{\frac{2}{\mu_n C_{ox}\left(W/L\right)}} \cdot \sqrt{I_D}$$

Diode voltage is changing by the square of the drain current

Diode connected MOS transistor

- V-I relation
  - Weak inversion
  - Active region by connection
  - Ignoring channel shortening



$$I_D = I_S e^{\frac{V_G - V_{T0} - nV_S}{nU_T}}$$

$$V_S = 0$$

$$I_D = I_S e^{\frac{V_G - V_{T0}}{nU_T}} \Rightarrow$$

$$V_G = V_{T0} + nU_T \cdot \left(\ln\left(I_D\right) - \ln\left(I_S\right)\right)$$

Diode voltage is changing with the natural logarithm of the current

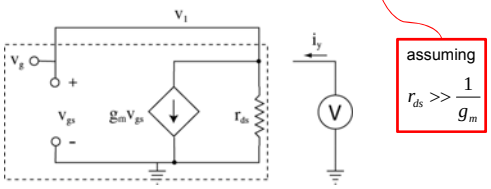
Diode connected transistors are also called compressors
(I→ln(V) or sqrt(V))

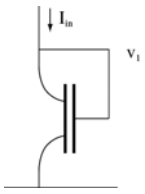
Diode connected transistor

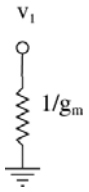
- Small signal model
  - Finding Thévenin equivalent
  - Applying test voltage v_y measuring i_y

$$i_y = \frac{v_y}{r_{ds}} + g_m v_y \Rightarrow \frac{v_y}{i_y} = r_{ds} \| \frac{1}{g_m} \approx \frac{1}{g_m}$$

assuming $r_{ds} >> \frac{1}{g_m}$

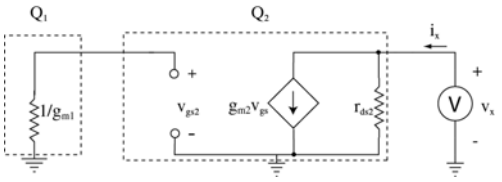




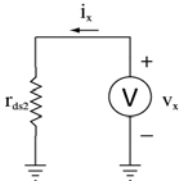


Mirror equivalent

- Small signal model



- No current through gate → V_{gs1}=0 implies $V_{gs2}g_{m2}$=0

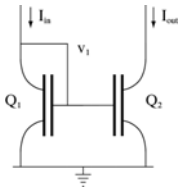


The small signal output impedance is equal to the output impedance of the output transistor (r_{ds2})

  - Current mirror output current is set by input, but some small-signal errors occur due to finite output resistance

Current mirror example

- Current gain of 2
- Output error <5μA at
  - 100μA current load
  - Max 1V output voltage change



$$\mu_n C_{ox} = 92\,{}^{\mu A}\!/_{V^2}, V_{tn} = 0.8V, r_{ds} = {}^{8000L(\mu m)}\!/_{I_D(mA)}$$

$$r_{out} = \frac{1V}{5\mu A} = 200k\Omega$$

Find the minimum output transistor length

$$r_{out} = r_{ds2} = \frac{8000L}{I_D} \Rightarrow L > \frac{r_{out} I_D}{8000} = \frac{200k \cdot 0.1}{8000} = \underline{2.5\mu m}$$

- Effective input voltage V_{eff} >0.5V

Find the maximum output transistor width

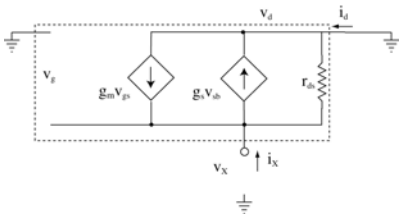
$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}V_{eff}^2 \Rightarrow W < \frac{2LI_D}{\mu_n C_{ox} V_{eff}^2} = \frac{2 \cdot 2.5\mu m \cdot 50\mu A}{92\,{}^{\mu A}\!/_{V^2} \cdot 0.25V^2} = \underline{10.9\mu m}$$

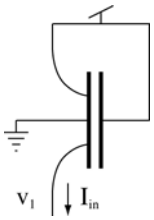
${}^{W_2}\!/_{L_2} = {}^{10\mu}\!/_{3\mu}$ and ${}^{W_1}\!/_{L_1} = {}^{5\mu}\!/_{3\mu}$

Feasible transistor sizes

Diode using source

- Diode-connected drain large signal behavior
  - Front-gate *and* back-gate





Lower impedance than standard diode! Why?

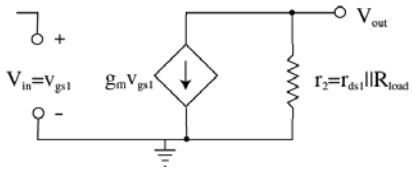
Other drawbacks?

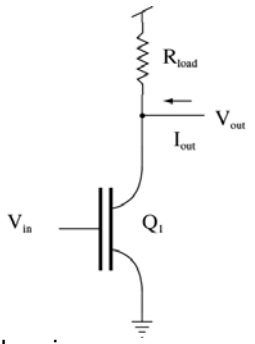
$$v_g = -v_X, v_{sb} = v_X$$

$$i_X = \frac{v_X}{r_{ds}} + g_m v_X + g_s v_X \Rightarrow \frac{v_X}{i_X} = r_{ds} \| \frac{1}{g_m + g_s} \approx \underline{\frac{1}{g_m + g_s}}$$

Common-source amplifier

- Inverting amplifier - resistive load
  - Small signal gain





$$A_V = \frac{v_{out}}{v_{in}} = -g_{m1}\left(r_{ds1}\|R_{load}\right)$$

  - High-impedance linear resistive load for high gain → high supply voltage

$$R_{load} = 200k\Omega, I_D = 100\mu A \Rightarrow$$
$$V_{\text{supply}} = 200k\Omega \cdot 100\mu A = \underline{20V}$$

Typical supply <3V!

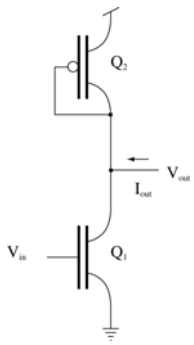
Common source with diode load

$$R_{load} = \frac{1}{g_{m2}}$$

$$A_V = \frac{v_{out}}{v_{in}} = -g_{m1}\left(r_{ds1}\left\|\frac{1}{g_{m2}}\right.\right) \approx -\frac{g_{m1}}{g_{m2}}$$

$$g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_D} \quad \text{with} \quad I_{D1} = I_{D2} \Rightarrow$$

$$A_V = -\frac{g_{m1}}{g_{m2}} = -\frac{\sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}I_{D1}}}{\sqrt{2\mu_p C_{ox}\frac{W_2}{L_2}I_{D2}}} = -\sqrt{\frac{\mu_n W_1/L_1}{\mu_p W_2/L_2}}$$



- The voltage gain is independent of bias current and voltages
  - Provided active region
- The gain set by design
- Headroom?

CS stage with source diode

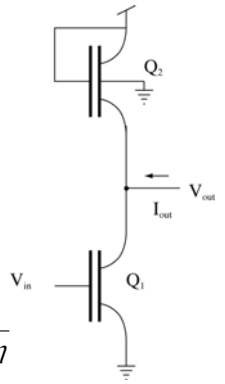
$$R_{load} = \frac{1}{g_{m2} + g_s}$$

$$A_V = \frac{v_{out}}{v_{in}} = -g_{m1}\left(r_{ds1} \left\| \frac{1}{g_{m2} + g_s} \right. \right) \approx -\frac{g_{m1}}{g_{m2} + g_s} = -\frac{g_{m1}}{g_{m2}} \frac{1}{1+\eta}$$

for $\eta = \frac{g_s}{g_{m2}}$

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D} \quad \text{with} \quad I_{D1} = I_{D2} \Rightarrow$$

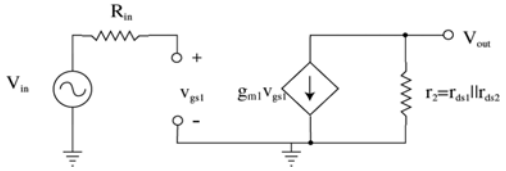
$$A_V = -\frac{g_{m1}}{g_{m2}} \frac{1}{1+\eta} = -\frac{\sqrt{2\mu_n C_{ox} \frac{W_1}{L_1} I_{D1}}}{\sqrt{2\mu_n C_{ox} \frac{W_2}{L_2} I_{D2}}} \frac{1}{1+\eta} = -\sqrt{\frac{W_1/L_1}{W_2/L_2}} \frac{1}{1+\eta}$$



- Lower Q_2 impedance

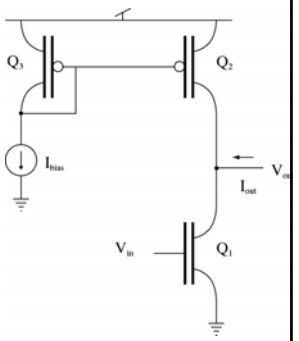
Common-source amplifier

- Popular gain stage
  - Inverting amplifier with current load
    - Triode or active region
  - Small signal equivalent



$$A_V = \frac{v_{out}}{v_{in}} = -g_{m1} \cdot R_2 = -g_{m1}\left(r_{ds1} \| r_{ds2} \right)$$

  - Typical gain of -10 to -100
  - High gain at low supply voltage
    - Exploring nonlinear transistor characteristics



Common-source stage keypoints

- Simple and popular gain stage
- High input impedance
- Passive load for high frequency (RF)
- Active load provide high resistive equivalent due to non-linearity giving higher gain

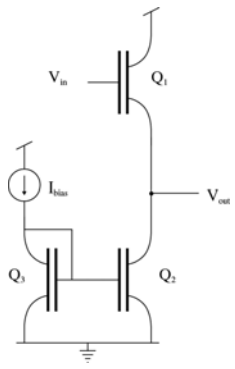
Source follower

- Large signal behavior
  - Output voltage "follows" input voltage
    - Diode drop offset
      - Unit gain amplifier (A≈1)
      - Voltage buffer
      - Current gain

$$V_{out} = V_{in} - V_{GS} \Rightarrow$$

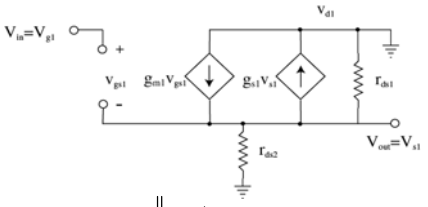
$$V_{out} = V_{in} - \left(V_{tn} + \sqrt{\frac{2}{\mu_n C_{ox}(W/L)}} \cdot \sqrt{I_D} \right)$$

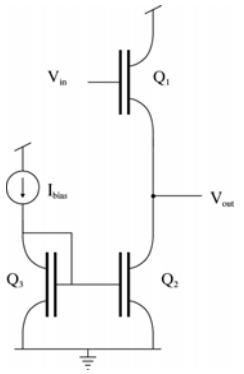
    - Ignoring channel shortening and body effect
      - Voltage drop increase with square root of current
  - Used as buffer/driver for larger loads



Source follower

- Small signal model





$$\frac{1}{G_{S1}} = R_{S1} = r_{ds1} \left\| r_{ds2} \right\| \frac{1}{g_{s1}}$$

$$v_{gs1} = v_{in} - v_{out} \qquad v_{out} G_{S1} - g_{m1}(v_{in} - v_{out}) = 0 \Rightarrow$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + G_{S1}} = \frac{g_{m1}}{g_{m1} + g_{s1} + g_{ds1} + g_{ds2}}$$

g_{s1} is 1/10 of g_{m1} and $g_{ds1(2)}$ is 1/10 of g_{s1}
•Body effect major error term

Source follower keypoints

- Voltage gain close to one
- Affected by body-effect
- Can provide large current gain

Common gate application

- Impedance matching
  - 50Ω transmission line

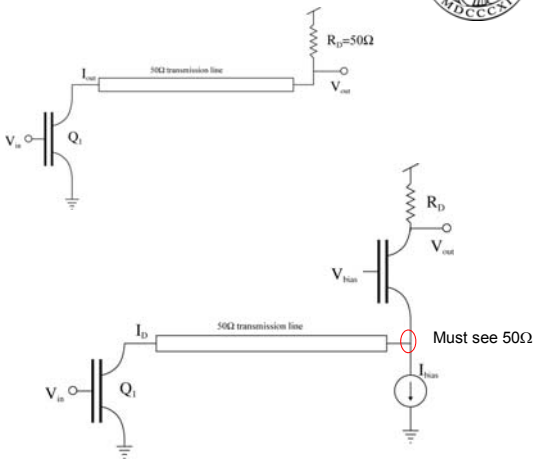
$$A_V = -g_{m1} \cdot R_D$$

  - With common gate

$$A_V = -g_{m1} \cdot R_D$$

$$\frac{1}{g_m + g_{mb}} = 50\Omega$$

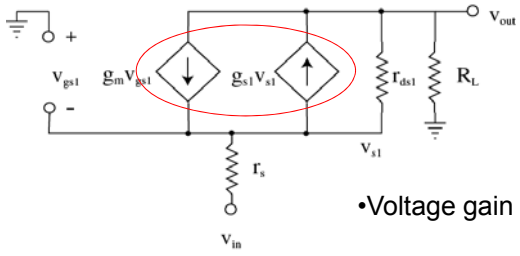
Achieved by proper sizing

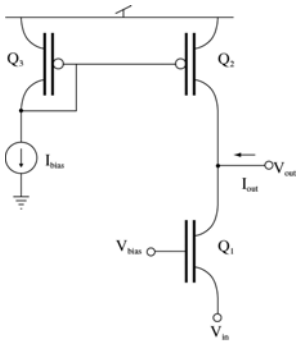


• The common gate allow for much higher RD giving higher overall gain

Common-gate amplifier

- Low impedance input
  - Typical 50Ω matching
  - Voltage gain as common-source





•Voltage gain

$$v_{gs1} = -v_{s1}$$

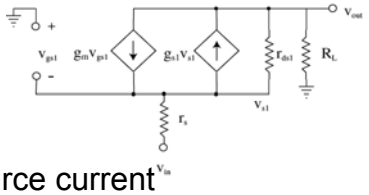
For grounded gate circuits
Always combine currents sources

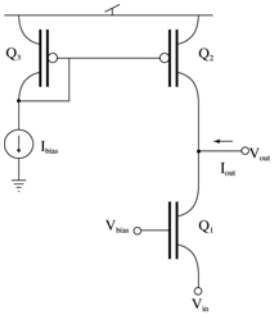
$$(g_{m1} + g_{s1})v_{s1}$$

$$v_{out}(G_L + g_{ds1}) - v_{s1}g_{ds1} - (g_{m1} + g_{s1})v_{s1} = 0 \Rightarrow$$

$$\frac{v_{out}}{v_{s1}} = \frac{g_{m1} + g_{s1} + g_{ds1}}{G_L + g_{ds1}} = (g_{m1} + g_{s1} + g_{ds1})(R_L \parallel r_{ds1}) \approx g_{m1}(R_L \parallel r_{ds1})$$

Common gate amp analysis





- Source current

$$i_s = (g_{m1} + g_{s1})v_{s1} + (v_{s1} - v_{out})g_{ds1}$$
$$= (g_{m1} + g_{s1} + g_{ds1})v_{s1} - g_{ds1}v_{out}$$

- Input admittance

$$\frac{1}{r_{in}} = \frac{i_s}{v_{s1}} = \frac{(g_{m1} + g_{s1} + g_{ds1})}{1 + \frac{g_{ds1}}{G_L}} \cong \frac{g_{m1}}{1 + \frac{g_{ds1}}{G_L}} \Rightarrow r_{in} = \frac{1}{g_{m1}}\left(1 + \frac{R_L}{r_{ds1}}\right)$$

$$r_{ds1} \approx R_L \Rightarrow r_{in} \cong \frac{1}{g_{m1}} \qquad R_L >> r_{ds1} \Rightarrow r_{in} > \frac{1}{g_{m1}}$$

Twice the expected input impedance

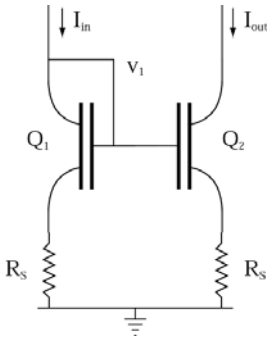
The drain voltages is too "weak"

Common-gate keypoints

- Voltage gain similar to common-source stage
- Provide low input impedance
  - May increase for low frequency signals
- Suitable for matched transmission lines
- Used extensively in RF circuits

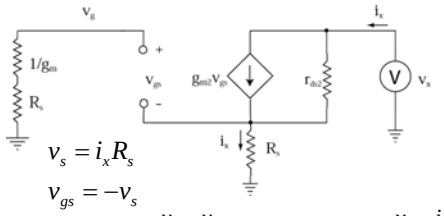
Source-degeneration

- Increase output impedance
  - Reducing error due to output voltage variation
  - Making soft reference
  - Resistor
    - Linear voltage dependence
  - MOS transistor
    - Linear drain resistance
    - Square (exponential) gate-source dependence
  - Increased output current
    - Restricted by reduced gate-source voltage



Source degenerated mirror

- Small signal model



$$v_s = i_x R_s$$

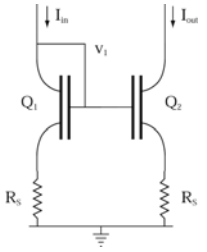
$$v_{gs} = -v_s$$

$$i_x = g_{m2} v_{gs} + \frac{v_x - v_s}{r_{ds2}} \Rightarrow i_x = -i_x g_{m2} R_s + \frac{v_x - i_x R_s}{r_{ds2}} \Rightarrow$$

$$r_{out} = \frac{v_x}{i_x} = r_{ds2}\left(1 + R_s\left(g_{m2} + g_{ds2}\right)\right)$$

$$r_{out} \approx r_{ds2}\left(1 + R_s g_{m2}\right)$$

Output impedance increased by $(1+R_s g_{m2})$



With body effect

$$g_{m2} \rightarrow \left(g_{m2} + g_{s2}\right)$$

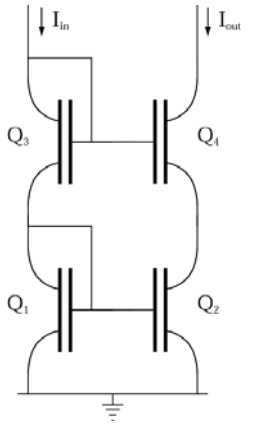
$$r_{out} \approx r_{ds2}\left(1 + R_s\left(g_{m2} + g_{s2}\right)\right)$$

- Increased output impedance → more accurate current copy

What about headroom?

High impedance mirrors

- Resistors hard to get in CMOS
  - Have to use MOS-devices for degeneration
- Cascode mirror
  - Softening sources with additional current-mirror



Using formula from source degeneration

$$r_{out} = r_{ds4}\left(1 + R_s\left(g_{m4} + g_{s4} + g_{ds4}\right)\right)$$

setting $R_s = r_{ds2} \Rightarrow$

$$r_{out} = r_{ds4}\left(1 + r_{ds2}\left(g_{m4} + g_{s4} + g_{ds4}\right)\right)$$

$$r_{out} \approx r_{ds4}\left(r_{ds2} g_{m4}\right)$$

Output impedance increased by $r_{ds2}g_{m4}$

Disadvantage:
$V_{out} > 2V_{eff} + V_{tn}$

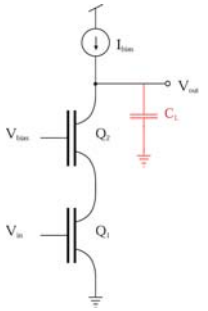
Cascode gain stage

- Single stage inverting amplifier
  - Improving performance
  - Combine common source feeding into common gate stage
  - Large gain
    - Low output impedance
    - High gain of common source transistor
    - High quality current sources
  - No speed loss with increased gain
  - Two variants
    - Telescopic configuration
    - Folded cascode configuration

Cascode gain stage

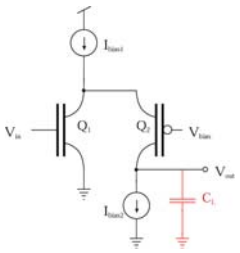
- Improve output impedance
  - "locking" Q1 drain voltage absorbing output voltage variations with Q2

•Telescopic cascode gain stage



DC level shift or headroom reduction

•Folded cascode gain stage



Reduced gain due to PMOS transistor

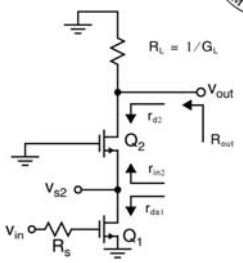
Cascode gain stage analysis

- Impedance looking into Q_2

$$r_{d2} = g_{m2} r_{ds1} r_{ds2}$$

- Small signal total output impedance is $r_{d2} \| R_L$
  - Assuming high quality current source

$$R_{out} = r_{d2} \| R_L$$



- Gain
  - Common gate input admittance

$$g_{m2} = \frac{1}{r_{in2}} = \frac{(g_{m2} + g_{s2} + g_{ds2})}{1 + \frac{R_L}{r_{ds2}}} \cong \frac{g_{m2}}{1 + \frac{R_L}{r_{ds2}}}$$

  - Common gate gain

$$\frac{v_{out}}{v_{s2}} = \frac{g_{m2} + g_{s2} + g_{ds2}}{G_L + g_{ds2}} \approx g_{m2}(R_L \| r_{ds2}) = \frac{g_{m2}}{g_{ds2} + G_L}$$

  - Common source gain

$$\frac{v_{S2}}{v_{in}} = -g_{m1}(r_{ds1} \| r_{in2}) = -\frac{g_{m1}}{g_{ds1} + g_{in2}}$$

  - Total gain

$$A = \frac{v_{s2}}{v_{in}} \frac{v_{out}}{v_{s2}} \cong -g_{m1}(r_{ds1} \| r_{in2}) g_{m2}(R_L \| r_{ds2})$$

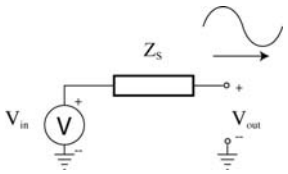
Cascode stage usage

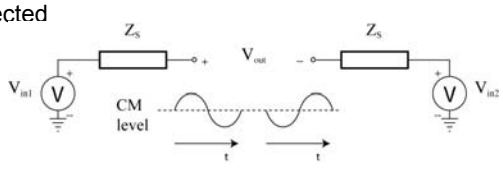
- Large gain for low frequencies $R_{out} = r_{d2} \parallel R_L$
  - Giving R_L must be large provided by high quality current mirror
    - With output resistance in the order of: $R_L = g_{m-p} r_{ds-p}^2$
  - Approximate by assuming transistors are close to equal
    - Dropping indices
  - Q2 admittance $g_{m2} = \frac{1}{r_{in2}} \cong \frac{g_m}{1 + g_{ds} g_m r_{ds}^2} \cong g_{ds} \Rightarrow r_{in2} \cong r_{ds}$
  - CS gain: $\frac{v_{S2}}{v_{in}} = -g_{m1}\left(r_{ds1} \parallel r_{in2}\right) = -\frac{1}{2} g_m r_{ds}$
  - CG gain: $\frac{v_{out}}{v_{s2}} \approx g_{m2}\left(R_L \parallel r_{ds2}\right) = g_m r_{ds} \quad \text{for } R_L >> r_{ds}$
  - Overall gain

$$A = \frac{v_{s2}}{v_{in}} \frac{v_{out}}{v_{s2}} \cong -\frac{1}{2} g_m^2 r_{ds}^2$$

Differential amplifiers

- Single ended signal
  - Signal swing relative to fixed potential
- Differential signal
  - Difference between two nodes
    - Equal swing around fixed potential
    - Opposite signal excursion
  - Better noise immunity
    - Common mode noise rejected
    - Power supply noise rejection





Important circuit invention with increased usage in advanced CMOS technology

MOS differential pair

- Standard input stage
  - Differential input $v_{in} = v^+ - v^-$
  - Ignoring output impedance

$$i_{d1} = i_{s1} = \frac{v_{in}}{r_{s1} + r_{s2}} = \frac{v_{in}}{1/g_{m1} + 1/g_{m2}}$$

  - Assuming I_{bias} split equally

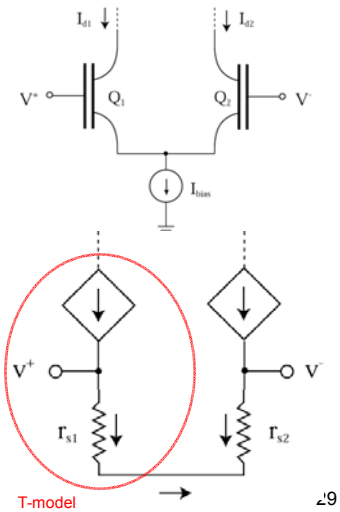
$$g_{m1} = g_{m2} \Rightarrow i_{d1} = \frac{g_m}{2} v_{in}$$

    - Similar for other branch

$$i_{d2} = i_{s2} = -i_{d1} \Rightarrow i_{d2} = -\frac{g_m}{2} v_{in}$$

  - Defining

$$i_{out} = i_{d2} - i_{d1} \Rightarrow \underline{i_{out} = g_m v_{in}}$$



Differential pair

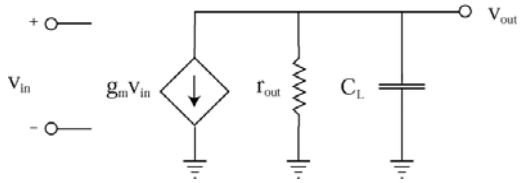
- Adding a P mirror $i_{d4} = i_{d3} = -i_{s1}$
- Output voltage

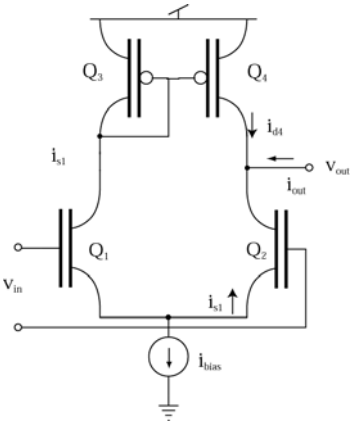
$$v_{out} = (i_{s1} - i_{d4}) r_{out} = 2 i_{s1} r_{out} = g_m r_{out} v_{in}$$

- Voltage gain

$$A_V = \frac{v_{out}}{v_{in}} = \underline{g_m r_{out}}$$

- Simplified model





Output impedance

$r_{out} = v_x / i_x, \quad i_x = i_{x1} + i_{x2} + i_{x3} + i_{x4}$

Finding currents $i_{x1} = \dfrac{v_x}{r_{ds4}}$

assuming $r_{ds1}, r_{ds2} >> r_{s1}, r_{s2}$

$$i_{x2} = \frac{v_x}{r_{ds2}}$$

assuming $r_{s1} = r_{s2}$

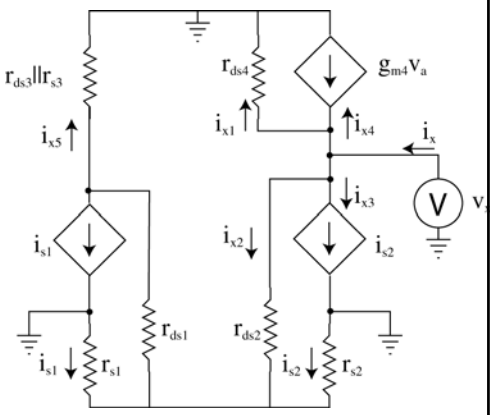
$$i_{s1} = i_{s2} = \frac{-v_x}{2r_{ds2}}$$

since $i_{x4} = i_{x5}$

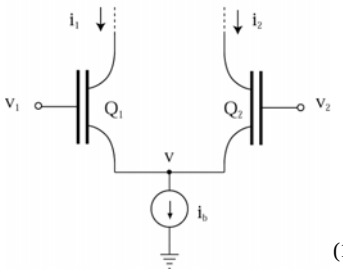
$$i_{x4} = -i_{s1} = -i_{s2} = -i_{x3}$$

$$r_{out} = \frac{v_x}{i_{x1} + i_{x2} + i_{x3} + i_{x4}} = \frac{v_x}{v_x / r_{ds4} + v_x / r_{ds2}}$$

$$r_{out} = r_{ds2} \,||\, r_{ds4} \Rightarrow \underline{A_v = g_m (r_{ds2} \,||\, r_{ds4})}$$



Weak inversion diff pair analysis



$$I_1 = I_0 \exp\left[\frac{v_1 - nv}{nU_T}\right] \quad (1)$$

$$i_2 = I_0 \exp\left[\frac{v_2 - nv}{nU_T}\right] \quad (2)$$

$$i_b = i_1 + i_2$$

$$i_b = I_0 \exp\left[-\frac{v}{U_T}\right]\left(\exp\left[\frac{v_1}{nU_T}\right] + \exp\left[\frac{v_2}{nU_T}\right]\right)$$

giving

$$\exp\left[-\frac{v}{U_T}\right] = \frac{i_b}{I_0} \frac{1}{\exp\left[\frac{v_1}{nU_T}\right] + \exp\left[\frac{v_2}{nU_T}\right]}$$

(1) and (2) gives:

$$i_1 = i_b \frac{\exp\left[\frac{v_1}{nU_T}\right]}{\exp\left[\frac{v_1}{nU_T}\right] + \exp\left[\frac{v_2}{nU_T}\right]}$$

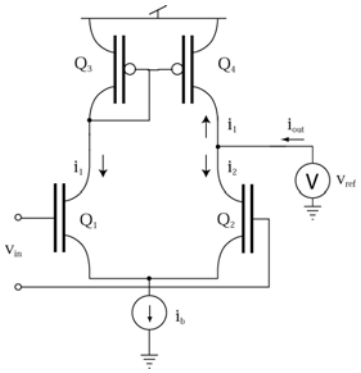
$$i_2 = i_b \frac{\exp\left[\frac{v_2}{nU_T}\right]}{\exp\left[\frac{v_1}{nU_T}\right] + \exp\left[\frac{v_2}{nU_T}\right]}$$

Transconductance amplifier

- Differential pair with current output
  - voltage → current
  - Weak inversion characteristics

$$i_{1(2)} = \frac{i_b}{1 + e^{\frac{v_1 - v_2}{nU_T}}}$$

$$\underline{i_{out}} = i_1 - i_2 = \underline{i_b \tanh\left(\frac{v_1 - v_2}{2nU_T}\right)}$$



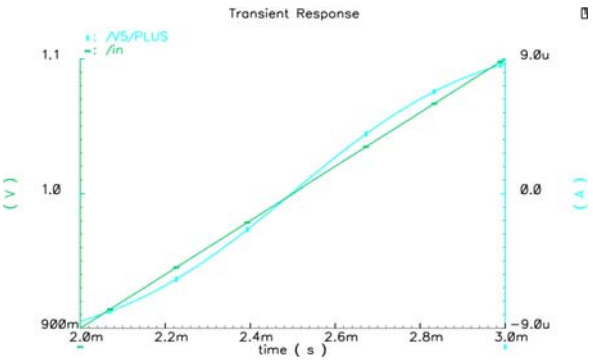
Transconductance amplifier

- Transconductance

$$g_m = \frac{\partial i_{out}}{\partial(v_1 - v_2)}$$

$$= g_{m1(2)} = \frac{i_b}{2nU_T}$$

  - Linear region
    - <200 mV



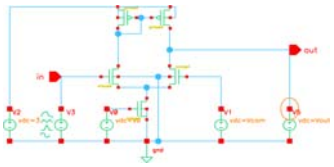
Cadence simulation

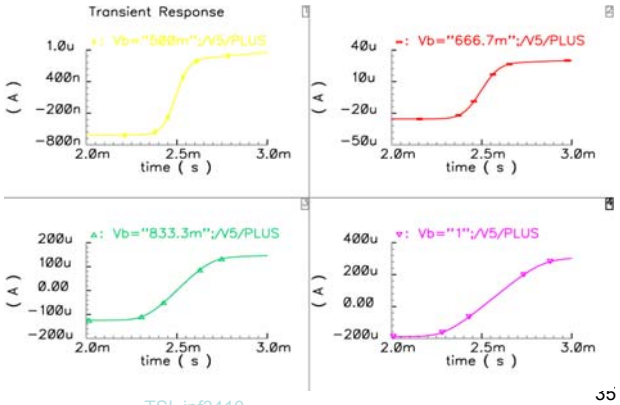
Diff pair cadence analysis

Diff voltage in: 1V

Current out:

4 different bias voltages:
0.5V to 1V



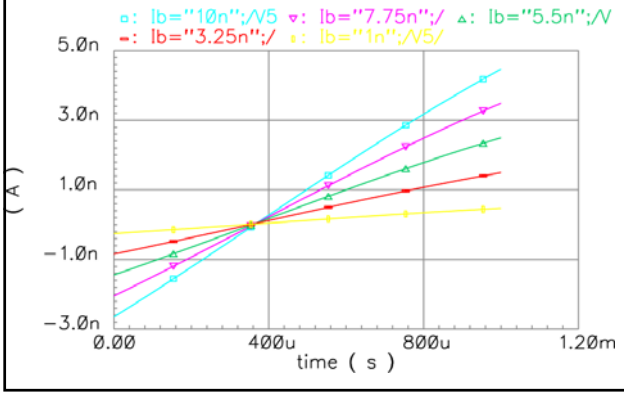


Linear diff pair transfer

- Transconductance
  - Vdiff: [-25mV, 25mV]
  - Ib: [1nA,10nA]

$$i_{out} = \frac{i_b}{2nU_T}(v_1 - v_2) \quad \text{giving}$$

$$g_m = \frac{i_b}{2nU_T}$$



Inserting values:

$$g_m \approx \frac{10nA}{2 \cdot 1.5 \cdot 25mV} = \frac{1}{7.5} \, nA/mV$$

reading graph (10nA):

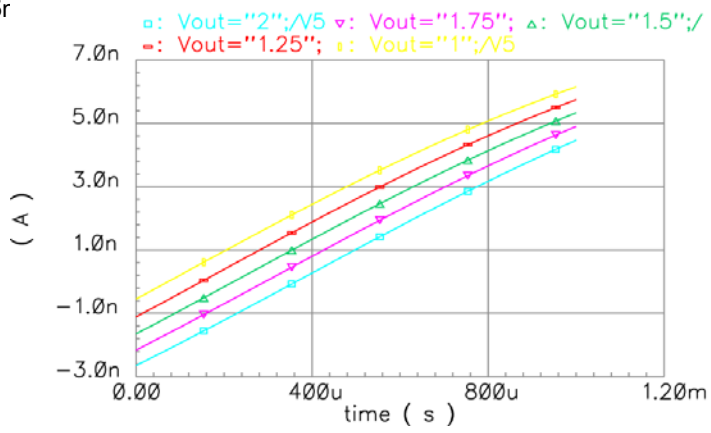
$2.8nA$ change in $20mV$ gives:

$$\frac{2.8nA}{20mV} = \frac{1}{7.2} \, nA/mV$$

Diff pair output conductance

- Cadence simulations
  - Varying output voltage

- Vout: [1V,2V]
- Input diff:[-25r
- Ib=10nA



Keypoints

- Simple mirror have a small signal input resistance $\frac{1}{g_m}$
- CS stage is popular with high input impedance and active load maintain headroom
- CD stage, no voltage gain (=1) and may be unstable
- CG similar performance to CS, but with low input impedance
- Source degeneration increase output resistance
- Cascode techniques increase output resistance
- Diff pairs are very popular as input stage