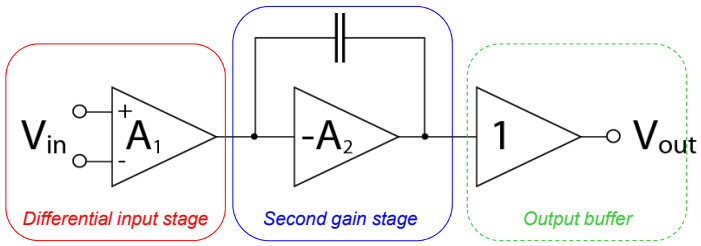
Opamp design

- Two stage opamp
  - Generic amp topology
  - Gain and frequency response
  - Offset and slew rate limitations
  - Input stage
  - Compensation
  - Feedback

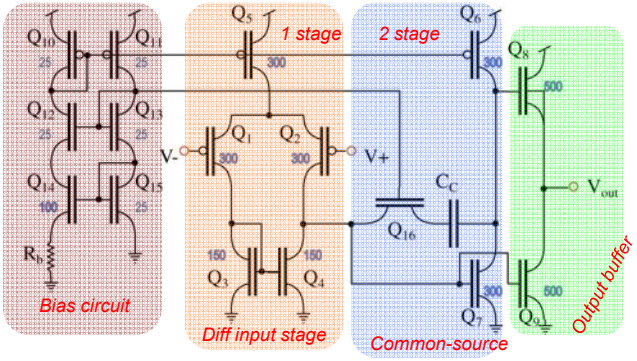
Classic opamp still suitable for CMOS technology (also bipolar)

Two stage OPAMP



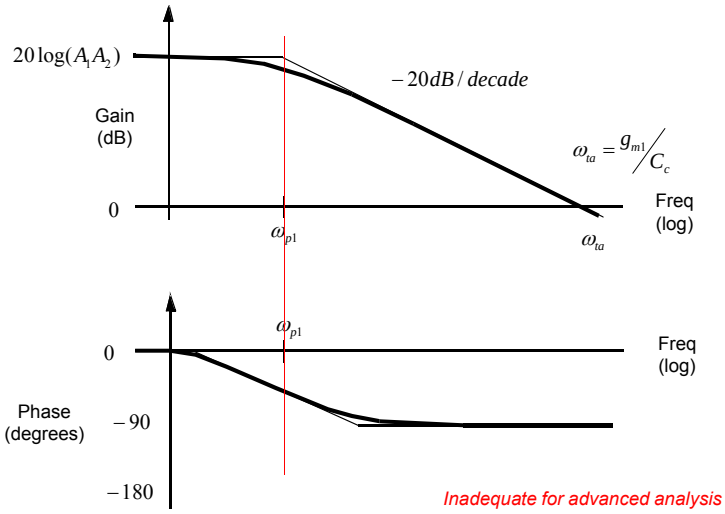
- Two gain stages (A_1 and A_2)
- Compensated second stage (Miller capacitance)
- Output buffer for resistive loads
  - Not present for capacitive loads

CMOS OPAMP topology



- PMOS diff input stage
- Numbers realistic transistor widths
  - Length 1-2 times minimum
- Output buffer dropp for capacitive loads

First order model



Inadequate for advanced analysis

Opamp gain

- Gain for diff pair – 1. stage

$$A_{v1} = g_{m1}\left(r_{ds2} \,\|\, r_{ds4}\right) \qquad g_{m1} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \sqrt{2\mu_n C_{ox}\frac{W}{L}\frac{I_{bias}}{2}}$$

  - Typical gain 50-100

$$\lambda = \frac{k_{ds}}{2L\sqrt{V_{DS} - V_{eff} + \Phi_0}}$$

- Gain of common source – 2. stage

$$A_{v2} = -g_{m7}\left(r_{ds6} \,\|\, r_{ds7}\right) \qquad k_{ds} = \sqrt{\frac{2K_s\varepsilon_0}{qN_A}}$$

  - Typical gain 50-100

$$r_{ds} \cong \frac{1}{\lambda I_D}$$

- Gain of source follower – output buffer

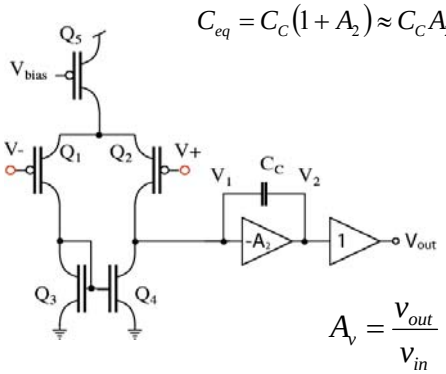
$$A_{v3} = \frac{g_{m8}}{G_L + g_{m8} + g_{s8} + g_{ds8} + g_{ds9}} \qquad g_{s8} = \frac{\gamma g_m}{2\sqrt{V_{SB} + |2\phi_F|}}$$

  - Gain ≈1
  - Not included for capacitive loads

Frequency response

- Midband frequencies
  - Below unit-gain frequency
  - Above frequencies without compensation effects

$$C_{eq} = C_C\left(1 + A_2\right) \approx C_C A_2 \qquad A_1 = g_{m1}Z_{out1} = g_{m1}\left(r_{ds2} \,\|\, r_{ds4} \,\|\, \frac{1}{sC_{eq}}\right)$$



at midband freq C_{eq} dominates

$$A_1 = g_{m1}\frac{1}{sC_{eq}} = g_{m1}\frac{1}{sC_C A_2}$$

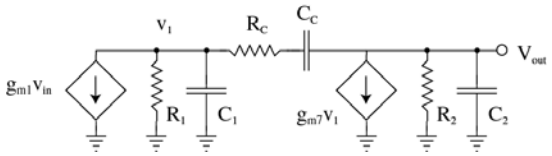
$$A_v = \frac{v_{out}}{v_{in}} = A_1A_2A_3 \approx g_{m1}\frac{1}{sC_C A_2}\cdot A_2 \cdot 1 = \frac{g_{m1}}{sC_C}$$

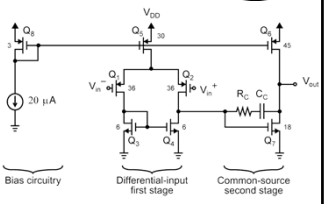
Unit-gain frequency proportional to g_m assuming A_3=1

setting $|A_v(j\omega_{ta})| = 1$ *and solve*

$$\omega_{ta} = \frac{g_{m1}}{C_C} = \frac{I_{D5}}{V_{eff\,1}C_C}$$

Small signal opamp model





$$R_1 = r_{ds4} \| r_{ds2} \text{ and } C_1 = C_{db2} + C_{db4} + C_{gs7}$$
$$R_2 = r_{ds6} \| r_{ds7} \text{ and } C_2 = C_{db7} + C_{db6} + C_{L2}$$

- Assume R_C=0 give transfer function

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}g_{m7}R_1R_2\left(1 - \frac{sC_C}{g_{m7}}\right)}{1 + sa + s^2b}$$
$$a = (C_1 + C_C)R_2 + (C_1 + C_C)R_1 + g_{m7}R_1R_2C_C$$
$$b = R_1R_2(C_1C_2 + C_1C_C + C_2C_C)$$

- Assume widely separated poles

$$D(s) = \left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right) \approx 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}}$$

- Dominant pole

$$\omega_{p1} = \frac{1}{R_1[C_1 + C_C(1 + g_{m7}R_2)] + R_2(C_1 + C_C)}$$
$$\approx \frac{1}{R_1C_C(1 + g_{m7}R_2)}$$
$$\approx \frac{1}{g_{m7}R_1R_2C_C}$$

- Non-dominant pole

$$\omega_{p2} = \frac{g_{m7}C_C}{C_1C_2 + C_1C_C + C_2C_C}$$
$$\approx \frac{g_{m7}}{C_1 + C_2}$$

- *Increasing g_{m7} → increased pole distance*
  - *Pole splitting compensation*
- *Cc may decrease ω_{p1}*

- Additional zero

$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}g_{m7}R_1R_2\left(1-\frac{sC_C}{g_{m7}}\right)}{1+sa+s^2b} \qquad \Rightarrow \omega_Z = -\frac{g_{m7}}{C_C}$$

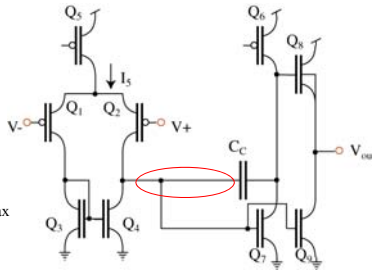
  - Right half-plane→negative phase shift with decreased PM
  - Stability issues
  - Hard to get rid of, but pole distance is increased with g_{m7}
- Have to make R_C >0
  - Zero-pole with some resistive element $\omega_Z = -\frac{1}{C_C\left(1/g_{m7}-R_C\right)}$
    - May eliminate that zero-pole by setting $R_C = \frac{1}{g_{m7}}$
    - Alternatively try to cancel ω_{p2} with ω_z

$$\frac{g_{m7}}{C_1+C_2} = -\frac{1}{C_C\left(1/g_{m7}-R_C\right)} \Rightarrow R_C = \frac{1}{g_{m7}}\left(1+\frac{C_1+C_2}{C_C}\right)$$

    - "Overcompensation" might even be wise: $\omega_Z = 1.2\omega_t$

$$R_C >> 1/g_{m1} \Rightarrow \omega_Z \approx \frac{1}{R_C C_C}, \quad \omega_t \approx g_{m1}/C_C \text{ gives } R_C = \frac{1}{1.2g_{m1}}$$

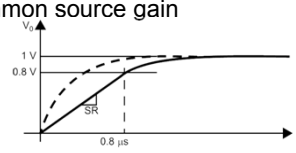
Slew rate



- Fastest change on output
  - For large input signals

$$SR = \left.\frac{\partial V_{out}}{\partial t}\right|_{\max} = \frac{1}{C}\left.\frac{\partial Q_{out}}{\partial t}\right|_{\max} = \frac{1}{C}I_{\max}$$

- What node is lagging?
  - Output buffer gain of 1
  - Miller compensation eliminates common source gain
  - Gain primarily in input stage
    - Lagging due to capacitive load
    - Current limited by tail current, I_5



$$SR = \frac{I_5}{C_C} = \frac{2I_1}{C_C} = \frac{2I_1\omega_{ta}}{g_{m1}} = V_{eff1}\cdot\omega_{ta} \qquad V_{eff} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(W/L)}}$$

Increasing slew-rate in two stage OPAMPs can only be done by
- *Increasing unit-gain frequency → increase ω_{p2} keeping PM*
- *Increasing effective voltage of diff pair*

NMOS diff-pair or PMOS diff-pair?

- PMOS
  - Higher saturation voltage (V_{eff})
  - Less flicker noise (1/f) noise
  - Lower mobility (transconductance)
- NMOS
  - Lower saturation voltage (V_{eff})
  - Higher transconductance (mobility 2-3 times higher)
- According to book:
  - PMOS diff pair due to improved slew-rate
  - Giving NMOS second stage
- In low-voltage modern process:
  - Always folded cascode giving same type in input and drive
  - NMOS input with NMOS drive may be better than PMOS on both

Systematic errors

- Systematic offset with V_{in}=0
  - Output should be $V_{dd}/2$
  - Splits tail current

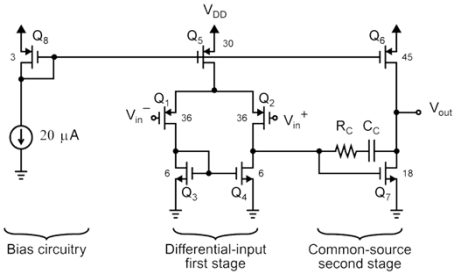
$$I_4 = I_5/2$$

  - Pull-up and pull-down current should match

$$I_7 = I_6$$

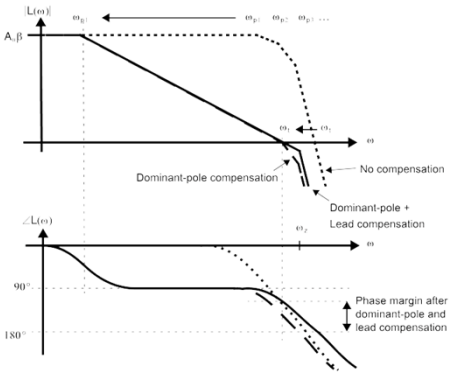
  - Adjusted by current gain

$$\frac{(W/L)_7}{(W/L)_4} = 2\frac{(W/L)_6}{(W/L)_5}$$



Opamp compensation

- Dominant-pole compensation $\omega_t \approx \beta\omega_{ta}$
  - Forcing a feedback system to have 1. order response up to loop unit-gain frequency ω_t
  - Stable system with increased PM
- Lead compensation
  - Adding zero, ω_z, just above ω_t
  - May improve PM with 20°



Compensation procedure

- Exploring zero $L(s) \approx A(s)\frac{Z_1}{Z_1 + Z_2}$
  - Coarse approximation
- Dominant pole
  - Determined by C_C and ω_t

    $\omega_t = L_0\omega_{p1} = \beta g_{m1}/C_C$
    - Proper C_c used for dominant pole compensation
- Lead compensation
  - Using R_C to tune zero, ω_z
    - Adding a third pole, but at HF
  - May cancel zero: $R_C = 1/g_{m7}$
  - Even better, locate zero at second pole:

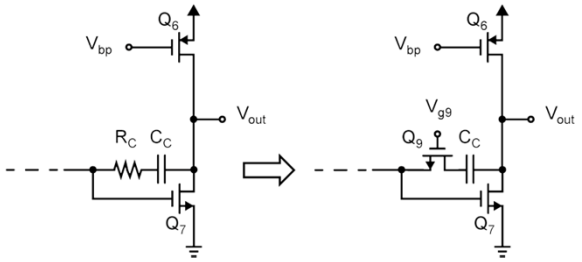
$$\omega_{p2} = \frac{g_{m7}C_C}{C_1C_2 + C_1C_C + C_2C_C} = \frac{-1}{C_C(1/g_{m7} - R_C)} \Rightarrow R_C = \frac{1}{g_{m7}}\left(1 + \frac{C_1 + C_2}{C_C}\right)$$

  - Increasing R_C even further slightly above second ole does it!

$$\omega_z \approx \frac{-1}{C_C\left(\frac{1}{g_{m7}} - R_C\right)} \qquad R_C \geq \frac{1}{g_{m7}} \text{ give } \omega_z < 0$$

Compensation

- Compensation resistor
  - Replaced by transistor in triode region



$$R_C = r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{eff}}$$

- Opamp compensation procedure

1. Start with some $C_C' = (\beta g_{m1}/g_{m7}) C_L$ setting unit-gain frequency close to second pole
2. By simulation (SPICE, CADENCE) find frequency with -125° phase shift (gain A')
   - Our aimed unit gain frequency ω_t
3. Choose new C_C such that ω_t is unit-gain freq of L(s)
   - C_C=C_C'A' giving 55° phase margin
   - A couple of simulation iterations may be necessary
4. Choose R_C : $$R_C = \frac{1}{1.2\omega_t C_C}$$
   - Giving phase margin of 85° (+30°) leaving 5° for variations

   Almost optimum lead compensation for any opamp
5. Sometimes phase margins are not adequate, then increase C_C
6. Replace R_C with a transistor

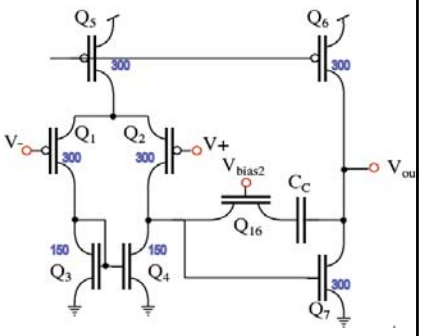
$$R_C = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{16} V_{eff\,16}}$$

Two stage opamp compensation

- Dominant pole compensation
  - Setting the ω_{p1} and ω_t since
    $$\omega_t = A_0\omega_0$$
  - Q_{16} operate in triode region
    - Resistive element

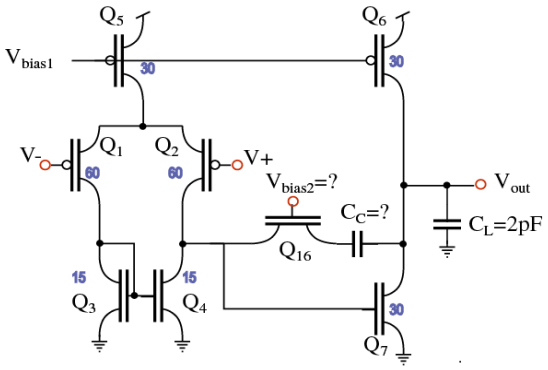
$$R_C = r_{DS16} = \frac{1}{\mu_n C_{ox}\frac{W}{L}V_{eff16}}$$

    - Resistive element ensures left half-plane zero
      - Damping element
    - *Lead compensation*

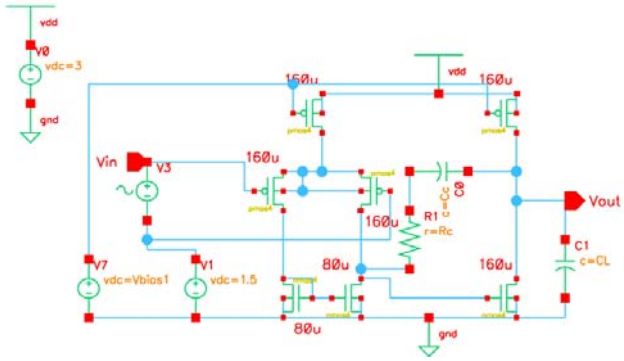


Opamp compensation example

- Find best compensation network C_c and R_c for:



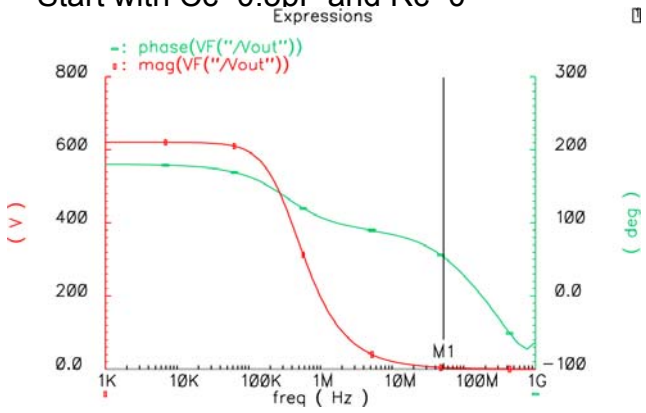
- Find bias voltage:



Vbias1=2.3V give 84μA tail current

Found by simple simulation run displaying tail current

- Start with Cc=0.5pF and Rc=0



0° phase in CADENCE display is -180° actual phase shift

Find (180-125)=55° phase shift at ωt=50.1MHz with gain A'=3.7

$$C_C = C_C' A' = 0.5\,pF \cdot 3.7 \approx 1.9\,pF$$

- New simulation with Cc=1.9pF give
  - ω_t=44.7MHz with A'=1.32

$$C_C = C_C^{'} A^{'} = 1.3pF \cdot 1.32 \approx 2.5pF$$

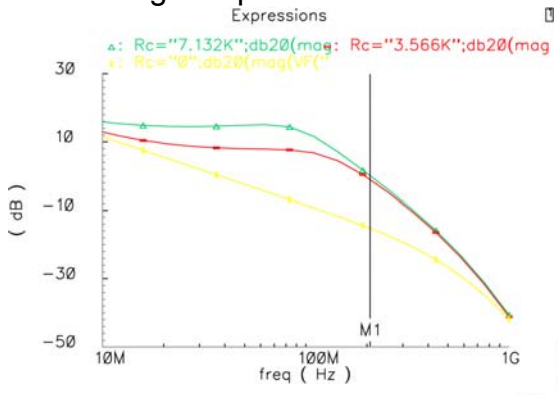
- New simulation with Cc=2.5pF give
  - ω_t=41MHz with A'=1.2

$$C_C = C_C^{'} A^{'} = 2.5pF \cdot 1.2 \approx 3.1pF$$

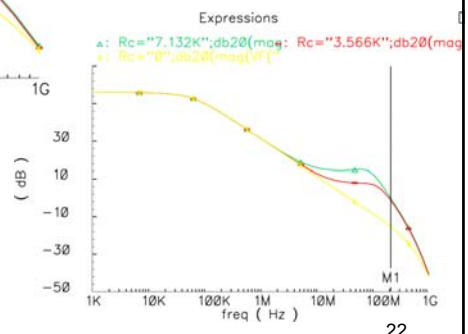
- New simulation with Cc=3.1pF give
  - ω_t=37.7MHz with A'=1.00
- Finding Rc

$$R_C = \frac{1}{1.2\omega_t C_C} = \frac{1}{1.2 \cdot 37.7 \cdot 10^6 \cdot 3.1 \cdot 10^{-12}} \approx 7132\Omega$$

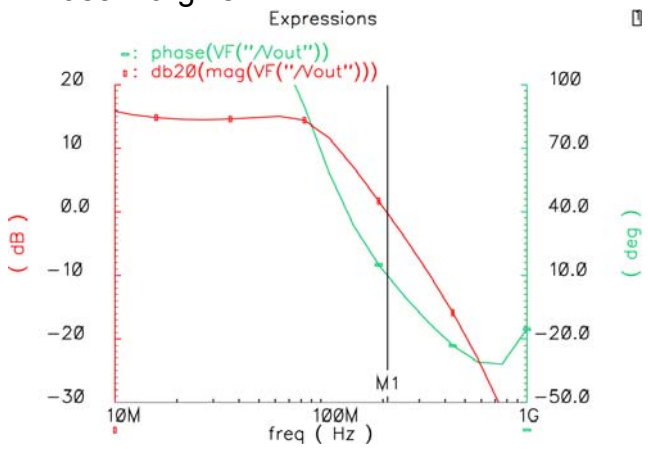
- Adding compensation resistor Rc



Give unit-gain freq of 209MHz

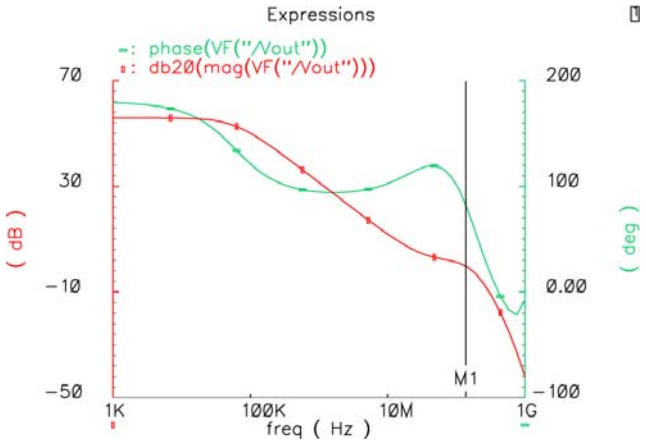


- Phase margins?



Phase margins only 10° !!!

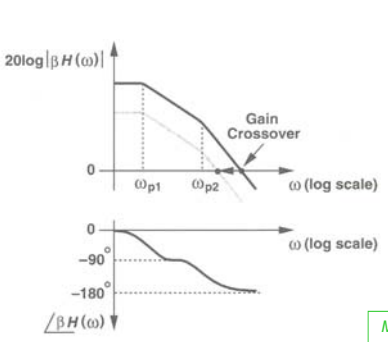
- What to do?
  - Book: increase Cc
  - Try to decrease Rc

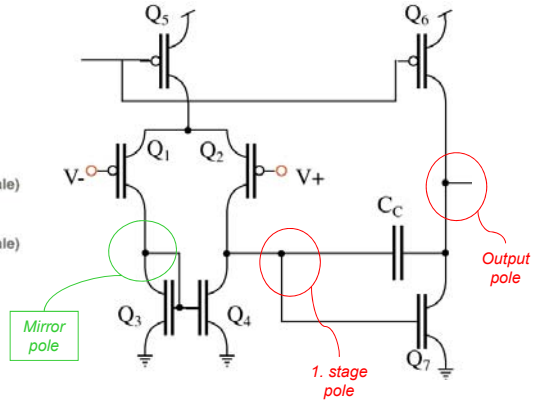


Give unit-gain freq of 133MHz with PM=84° with Rc=2050Ω

Two-pole amplifier

- Dominant poles of two-stage amps





  - 1. stage
    - High gain
    - Dominant pole at output

Advanced mirrors and opamps

- Advanced Current Mirrors
  - Wide-Swing Current Mirrors
  - Enhanced Output-Impedance Current Mirrors
- Advanced OTAs
  - Folded-Cascode OTA
  - Current-Mirror OTA
  - Fully Differential OTAs
    - Folded-Cascode
    - Current-Mirror
    - Common-Mode Feedback Circuits
  - Current-Feedback Opamps
- Simulation Example

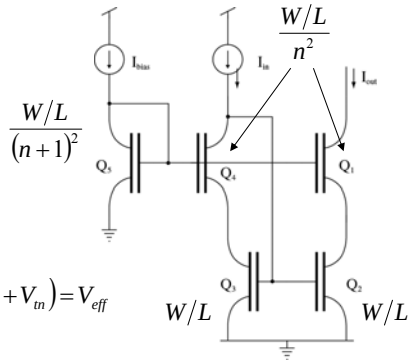
Wide swing current mirror

- Bias mirror transistors close to triode region
  - assuming

$$I_{bias} \approx I_{in}$$

$$V_{eff} = V_{eff2} = V_{eff3} = \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}(W/L)}}$$

$$V_{eff5} = (n+1)V_{eff}$$



  - Giving

$$V_{eff1} = V_{eff4} = nV_{eff}$$

$$V_{G5} = V_{G1} = V_{G4} = (n+1)V_{eff} + V_{tn}$$

$$V_{DS2} = V_{DS3} = V_{G5} - V_{GS1} = V_{G5} - (nV_{eff} + V_{tn}) = V_{eff}$$

  - Minimum output voltage

$$V_{out} > V_{eff1} + V_{eff2} = (n+1)V_{eff}$$

    - Q_2 and Q_3 on the edge of triode region

Ordinary cascode: $V_{out} > 2V_{eff} + V_{tn}$

- What n?
  - Often a small number

$$n = 1 \Rightarrow V_{out} > 2V_{eff}$$

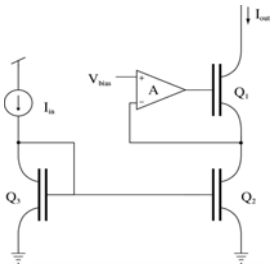
  - Typical effective voltage
  - Extend swing to 0.4V to 0.5V off rail $V_{eff} = [0.15V, 0.25V]$
- What bias current?
  - The input current varies….
  - Biasing current a little larger than max(I_{in})
  - Lower biasing might introduce slew rate problems
    - Might be tolerated for low frequency applications
- Practical hints
  - Make Q_5 W/L smaller than nominal value to ensure active region
  - Reduce L of Q_2 and Q_3 close to minimum maximizing frequency
  - Let Q_1 and Q_4 be longer to reduce short channel effects

Enhanced output-impedance

- Mirror with opamp gain boosting
  - Feedback to keep V_{ds2} stable

$$R_{out} \approx g_{m1} r_{ds2} r_{ds1} (1 + A)$$

  - Output impedance boosted by the gain of the opamp +1
    - Gain boosting
    - No more stacking



One opamp for each mirror….

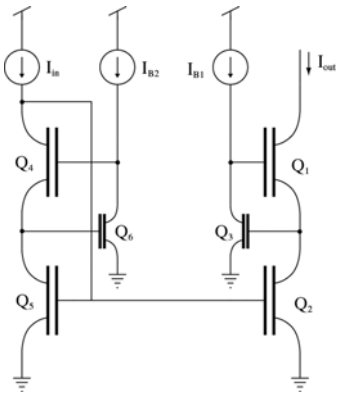
Simplified output enhancement

- Opamp → common source amp
  - Loop gain $\frac{g_{m3} r_{ds3}}{2}$
  - Output impedance

$$r_{out} \approx \frac{g_{m1} g_{m3} r_{ds1} r_{ds2} r_{ds3}}{2}$$

  - Input network ensure matching

NOT WIDE-SWING: $V_{out} > 2V_{eff3} + V_{tn}$



Wide swing, enhanced mirror

- Diodes as level shifters

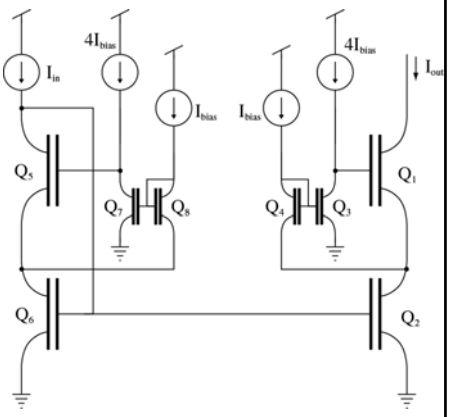
$$I_{in} \approx 7I_{bias}$$

  - Q_3 and Q_7 biased with 4 times current density

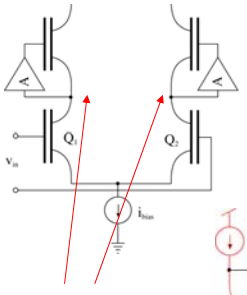
$$V_{out} > 2V_{eff}$$

  - Double power compared to previous
  - Might require compensation

Triple cascoding

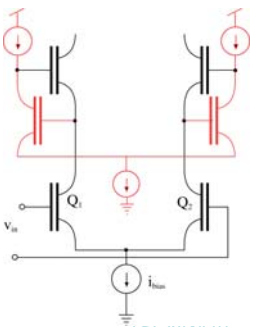


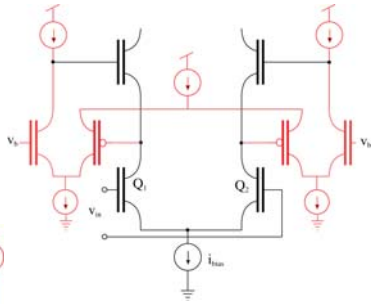
Diff pair boosting



Differential signal

Regulated cascode
• swing-limited

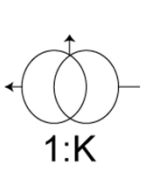


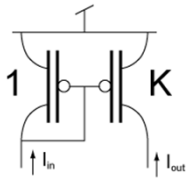


Regulated cascode diff pair

Current mirror symbol

- Several mirror circuit solutions
- Generic symbol

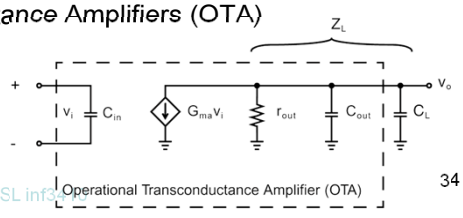




  - Arrow indicate input side
  - Direction of current flow

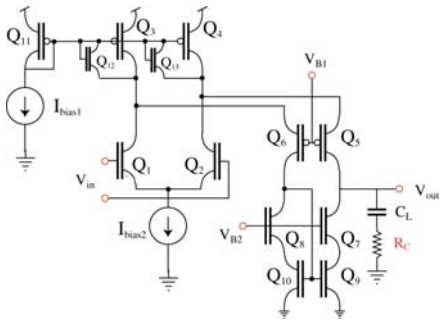
Modern op amps

- MOSFETS loads are mostly capacitive
  - Drop output buffer
  - Enabling large swing, high gain single stage aamps
  - Only output node high impedance
  - Internal node low impedance
    - Reduced voltage swing
  - Compensation by output capacitive loading
    - Increased stability, but lower speed
  - Transconductance
    - Most important parameter
  - Operational Transconductance Amplifiers (OTA)



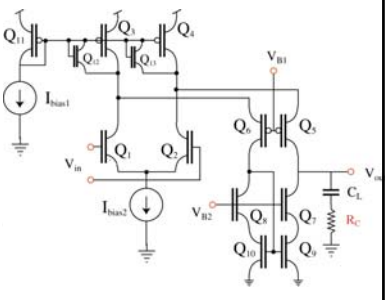
Folded cascode opamp

- Operational Transconductance Amplifier – OTA



  - Folding give same bias voltage on input and output
  - Typical
  - gain 700 to 3000

- Compensation achieved using load capacitor
  - No internal compensation
- As load increases, opamp slower but more stable
- Useful for driving capacitive loads only
- Large output impedance
  - not useful for driving resistive loads
  - Reduced with feedback
- Internal nodes low impedance
- Single-gain stage but dc gain can still be large (say 700 to 3000)
- Shown design makes use of wide-swing mirrors
- Simplified bias circuit shown
- Inclusion of Q_{12} and Q_{13} for improved slew-rate



- Small signal analysis

$$A_V = \frac{V_{out}(s)}{V_{in}(s)} = g_{m1} Z_L(s) = \frac{g_{m1} r_{out}}{1 + s r_{out} C_L}$$

  - Ignoring HF poles and zeros → diff-pair transconductance
  - With output enhanced impedance

$$r_{out} \approx \frac{g_m r_{ds}^2}{2}$$

    - » Quite high
  - Mid-band frequencies: $A_V \approx \frac{g_{m1}}{sC_L}$ unit-gain frequency: $\omega_{ta} = \frac{g_{m1}}{C_L}$
  - Unit-gain freq with feedback:

$$\omega_t = \beta \frac{g_{m1}}{C_L}$$

    - Amp bandwidth maximized
      - High input transconductance using nMOS and wide devices
      - By maximizing bias current though the differential pair

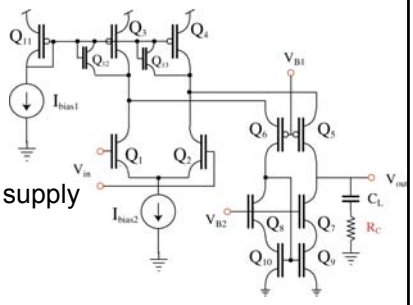
- Design guidelines for maximum bandwidth
  - Maximizing g_m of input pair
    - Use nMOS and wide devices
  - Choose current of input stage larger than output cascode
    - also maximizes dc gain
    - Might go as high as 4:1 ratio
  - Large input g_m results in less thermal noise
  - Second poles due to nodes at sources of Q_5 and Q_6
    - Minimize areas of drains and sources at these nodes with good layout techniques
- Insufficient phase margins
  - Lead compensating load capacitor in parallel with load capacitance

$$A_V = \frac{g_{m1}}{\frac{1}{r_{out}} + \frac{1}{R_C + 1/sC_L}} \approx \frac{g_{m1}(1 + sR_C C_L)}{sC_L}$$

    - Lead resistance R_C may be chosen to place a zero at 1.7 times unit gain frequency
  - Increase current and devices widths of output stage

Slew rate

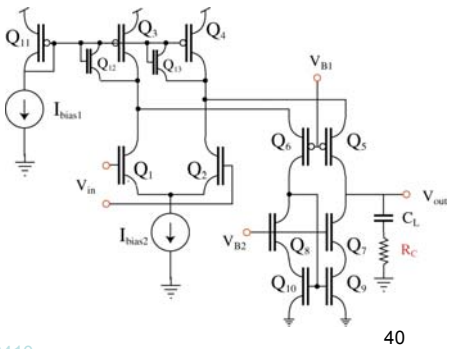
- Q_{12} and Q_{13} turned off during normal operation
  - Improve slew-rate
- Q_2 turned off due to large input voltage
  - Q_1 sinking tail current through Q_3
  - With Q_2 off. Q_4 current through Q_5
  - Charging load capacitance: $SR = \frac{I_{D4}}{C_L}$
- Drain of Q_1 pulled near negative power supply
  - Since $I_{bias2} > I_{bias1} \rightarrow Q_1$ in triode
  - Must recover going out of slew-rate
  - Adding significant slewing time
- Add Q_{12} (and Q_{13}) to clamp node closer to positive power supply
- Q_{12} (and Q_{13}) also dynamically increase bias currents during slew-rate limiting
  - They pull more current through Q_{11} thereby increasing bias current in Q_3 and Q_4



Example: Folded-cascode

- AMS 0.35µm 3.3V process
  - ±1.5V supply
  - 1mW power
  - Input stage – output stage ratio 4:1
  - Q_{11} = 1/30$Q_{3(4)}$ (Q_{11} current ignored for power)
  - Maximum width 300µm
    - Unit length 0.6µm
  - $V_{eff} \approx 0.25V$
  - Assume C_L=10pF load
  - Assume

$$\mu_n C_{ox} \approx 3\mu_p C_{ox} = 100\,\mu A/V^2$$



- Major current

$$I_{tot} = I_{D3} + I_{D4} = 2(I_{D1} + I_{D6})$$

- We want

$$I_{D1} = 4I_{D6}$$

- Defining $I_B = I_{D5} = I_{D6}$
  - Give

$$I_{tot} = 2(I_{D1} + I_{D6}) = 10I_B$$

- With maximum 1mW power consumption

$$I_B = I_{D5} = I_{D6} = \frac{I_{tot}}{10} = \frac{1mW/3V}{10} = 33\mu A$$

  - Giving

$$I_{D3} = I_{D4} = 5I_{D5} = 165\mu A$$

$$I_{D1} = I_{D2} = 4I_{D5} = 132\mu A$$

- Using

$$\frac{W}{L} = \frac{2I_{Di}}{\mu_i C_{oxi} V_{eff}^2}$$

Q_1	300/0.6
Q_2	300/0.6
Q_3	270/0.6
Q_4	270/0.6
Q_5	54/0.6
Q_6	54/0.6
Q_7	18/0.6
Q_8	18/0.6
Q_9	18/0.6
Q_{10}	18/0.6
Q_{11}	9/0.6
Q_{12}	9/0.6
Q_{13}	3/0.6

- Input stage transconductance

$$g_{m1} = \sqrt{2I_{D1}\mu_n C_{ox}(W/L)} = \sqrt{2 \cdot 132\mu A \cdot 100\,\mu A/V^2 \cdot (300/0.6)} = 3.6\,mA/V$$

- Unit gain frequency

$$\omega_t = \frac{g_{m1}}{C_L} = \frac{3.6\,mA/V}{10\,pF} = 3.6 \times 10^{-8}\,rad/s = 57MHz$$

- Slew rate

$$SR = \frac{I_{D4}}{C_L} = \frac{165\mu A}{10\,pF} = 16.5 \cdot 10^6\,V/s = 16.5V/\mu s$$

  - Adding clamp transistor, increase current

$$I_{bias2} = I_{D3} + I_{D12} = 264\mu A$$

    - » Since $I_{D3} = 30I_{D11}$ and $I_{D11} = 5.5\mu A + I_{D12}$
    - Give

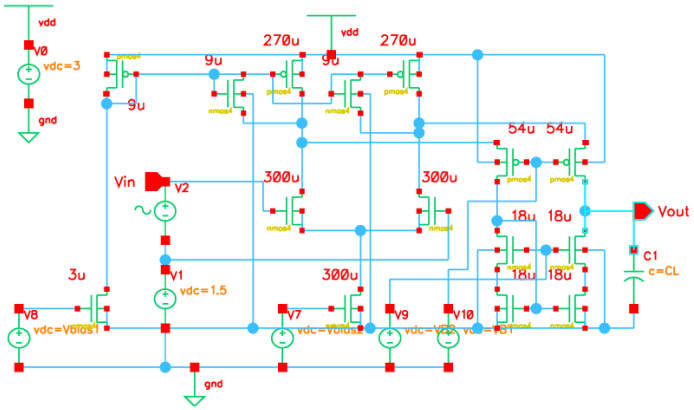
$$I_{D11} = \frac{264\mu A + 5.5\mu A}{31} = 8.7\mu A$$

    - and

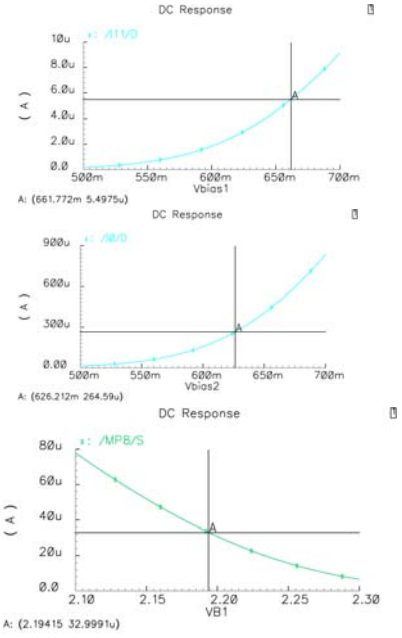
$$I_{D4} = 30 \cdot 8.7 = 261\mu A \Rightarrow SR = \frac{261\mu A}{10\,pF} = 26.1V/\mu s$$

Cadence simulation

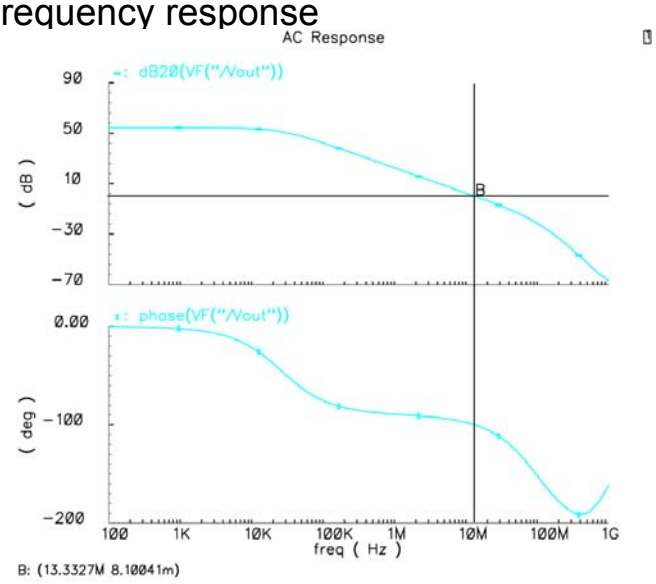
- Entering schematics



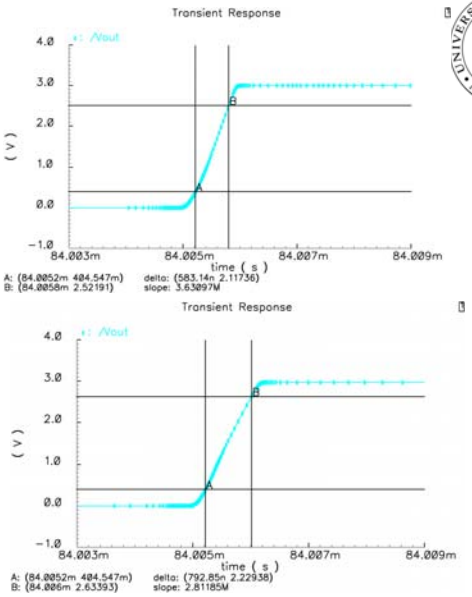
- DC operation points
  - Vbias1 for 5.5µA current
    - Vbias1=662mV
  - Vbias2 for 264µA current
    - Vbias2=626mV
  - VB1 for 33µA
    - VB1=2.194V



- Frequency response

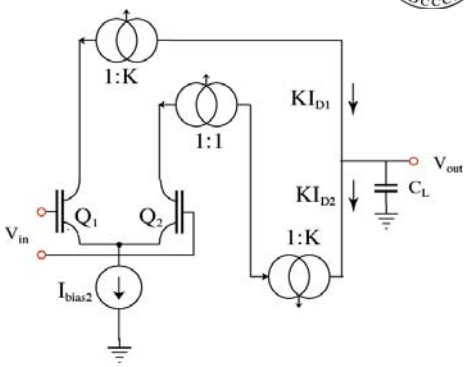


- Slew rate
  - With clamp
  - Giving approx. 3.6V/µs
  - Without clamp
  - Giving approx. 2,8V/µs

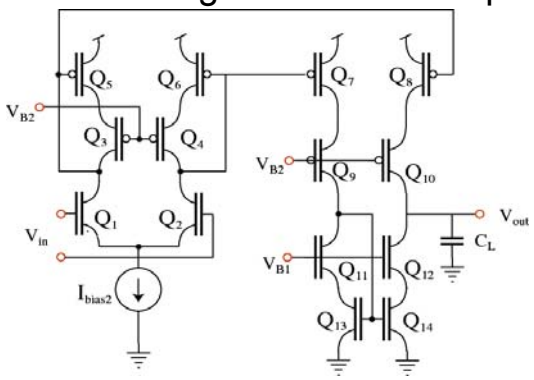


Current mirror opamp

- Low impedance nodes
  - Except output node
- Extra gain in current mirrors



- Wide swing current mirror opamp



$$I_{14} = KI_1 = K\frac{I_b}{2}$$

$$A_V = \frac{V_{out}(s)}{V_{in}(s)} = Kg_{m1}Z_L(s) = \frac{Kg_{m1}r_{out}}{1+sr_{out}C_L} \approx \frac{Kg_{m1}}{sC_L}$$

K factor is current gain from mirrors

Maximum K is around 5

- Unit gain frequency

$$\omega_{ta} = \frac{kg_{m1}}{C_C} = \frac{2kI_{D1}}{C_C V_{eff,1}}, I_{total} = (3+K)I_{D1} \Rightarrow \omega_{ta} = \frac{K}{3+K}\frac{2I_{D1}}{C_C V_{eff,1}}$$

  - Transconductance and unit-gain frequency increase with K
    - Assuming limited by load capacitance, not other HF poles
    - Often K=5 is practical
    - Increased K
      - Larger capacitance at drain of Q_1 (Q_2 and Q_9 as well)
        - » Moving down HF poles
      - Load capacitance may have to be increased to maintain stability
        - » Decreased bandwidth
  - For high bandwidth K might be lowered to 1

- Power

$$I_{total} = (3+K)I_{D1} = (3+K)I_b/2$$

- Slew rate
  - Assuming large input swing
  - All bias current one way

$$SR = \frac{KI_b}{C_L}$$

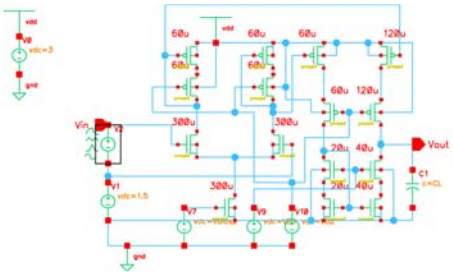
  - Larger K improve slew rate
  - Often better slew rate than folded cascode
  - Larger bandwidth as well
    - Folded cascode has better noise performance

Example: current mirror opamp

- Similar constraints as folded cascode opamp
  - Bias current

$$I_b = \frac{2I_{total}}{(3+K)} = \frac{2\,1mW/3}{(3+2)} = 130\mu A$$

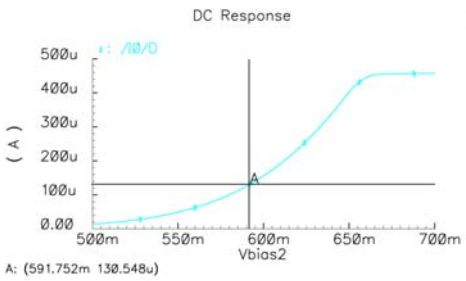
  - Gives 65µA in all input stage transistors
  - Output stage transistors twice as much current
- Using $\frac{W}{L} = \frac{2I_{Di}}{\mu_i C_{oxi} V_{eff}^2}$
  - Finding sizes



Q_1	300/0.6
Q_2	300/0.6
Q_3	60/0.6
Q_4	60/0.6
Q_5	60/0.6
Q_6	60/0.6
Q_7	60/0.6
Q_8	120/0.6
Q_9	60/0.6
Q_{10}	120/0.6
Q_{11}	20/0.6
Q_{12}	40/0.6
Q_{13}	20/0.6
Q_{14}	40/0.6

51

- Setting biasing
  - Tail current 130µA
  - V_{bias2} = 0.591V



  - Setting cascode voltages

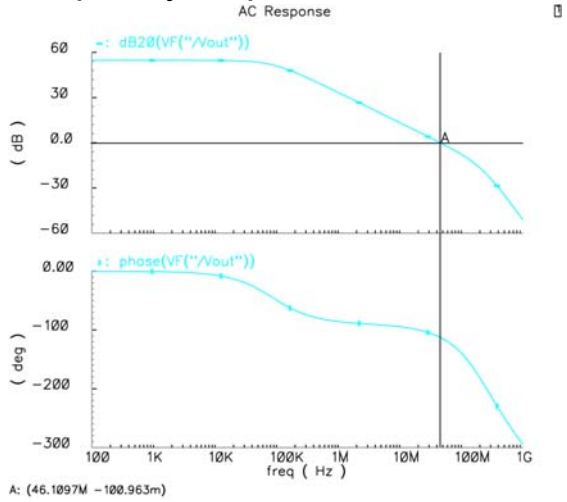
$$V_{bias} = (n+1)V_{eff} + V_{tn}$$

- Assuming $V_{tn} = 0.7V$ $V_{tp} = 0.9V$ $V_{eff} = 0.25V$
- Finding

$$V_{B1} = 1.2V$$
$$V_{B2} = 1.4V$$

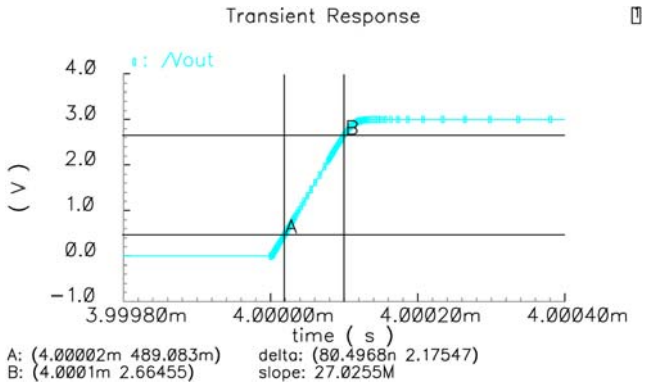
52

- Frequency response



$$g_{m1} = \sqrt{2I_{D1}\mu_n C_{ox}(W/L)} = 2.5\,mA/V \qquad \omega_t = \frac{Kg_{m1}}{C_L} = 79MHz$$

- Slew rate



- Simulated: $SR = 2.17/0.08 = 27.1\,V/\mu s$
- Theory: $SR = \frac{KI_b}{C_L} = \frac{2 \cdot 65\mu A}{10\,pF} = 26\,V/\mu s$

Linear settling time

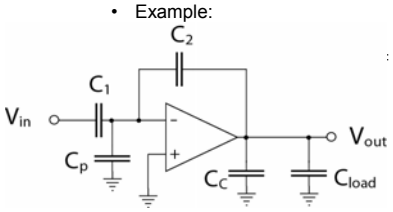
- Time constant for linear settling time

$$\omega_{-3dB} = \omega_t \approx \beta\omega_{ta}$$

  - Classic 2-stage opamps ω_t relatively independent of load
  - Not the case for folded-cascode and current-mirror opamps
    - High impedance output
    - ω_{ta} strongly related to load

$$\omega_{ta-folded-cascode} = \frac{g_{m1}}{C_L} \quad \omega_{ta-current-mirror} = \frac{Kg_{m1}}{C_L}$$

  - Settling time dependent on both feedback factor and load
  - Analyzing open-loop behavior to find capacitive load
    - Example:



$$\frac{1/\left[s(C_1+C_p)\right]}{1/\left[s(C_1+C_p)\right]+1/sC_2} = \frac{C_2}{C_1+C_p+C_2}$$

Open loop output load

$$C_L = C_C + C_{load} + \frac{C_2(C_1+C_p)}{C_1+C_p+C_2}$$

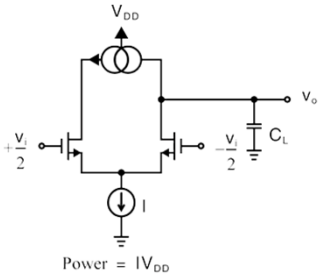
  - High-impedance opamps are fine internally on-chip
    - Load compensation is simple, but may limit performance

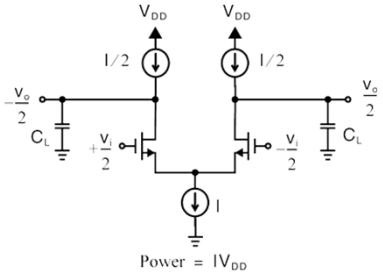
Topology comparison

	Gain	Output Swing	Speed	Power dissipation	Noise
Telescopic	Medium	Low	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-stage	High	Highest	Low	Medium	Low
Gain-boosted	High	Medium	Medium	High	Medium

Fully differential opamps

- Single-ended similar to fully differential opamp

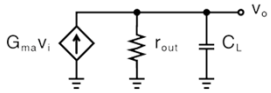




  - Double signal swing
  - Double area?

Single-ended ↔ diff amp

- Small signal comparison

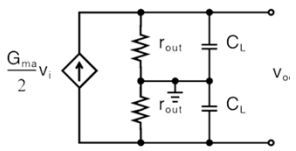


dc gain: $G_{ma}r_{out}$

$\omega_{-3dB} = 1/(r_{out}C_L)$

$\omega_{ta} = G_{ma}/C_L$

(a)



dc gain: $\frac{G_{ma}}{2}2r_{out} = G_{ma}r_{out}$

$\omega_{-3dB} = 1/(r_{out}C_L)$

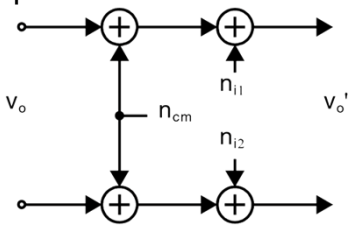
$\omega_{ta} = G_{ma}/C_L$

(b)

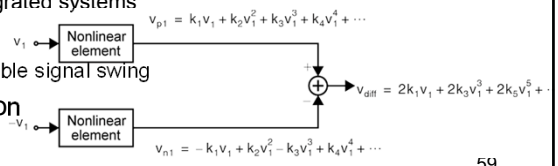
  - Basically the same small-signal performance

Diff amp advantage

- Noise performance

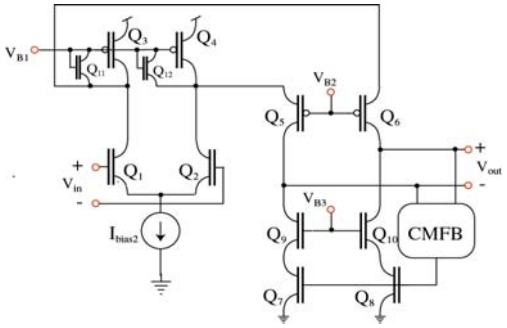


  - Common mode systematic noise injected in both half-signals
  - Cancel when looking at difference
    - Cancel fluctuations in supply and biasing
      - Major issue in integrated systems
  - Random noise double!
    - Still SNR is OK with double signal swing
  - Only odd order distortion
    - Tend to be smaller

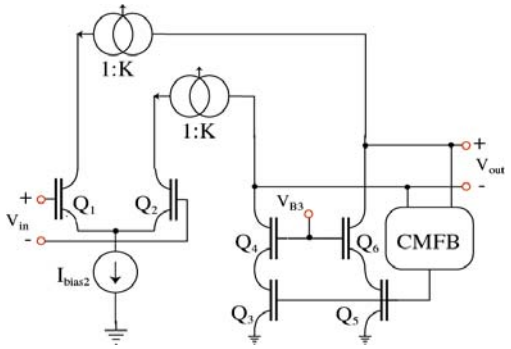


Common-mode feedback

- CMFB circuits
  - Defining output common-mode (average) voltage
  - Keeping common-mode voltage half-way between rails
  - Will add additional power consumption



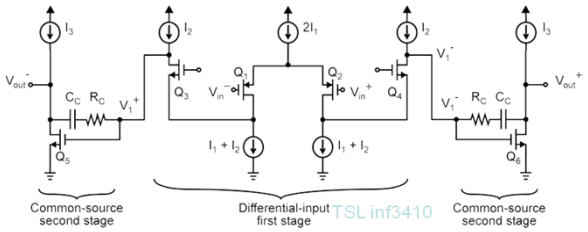
- Differential current mirror opamp



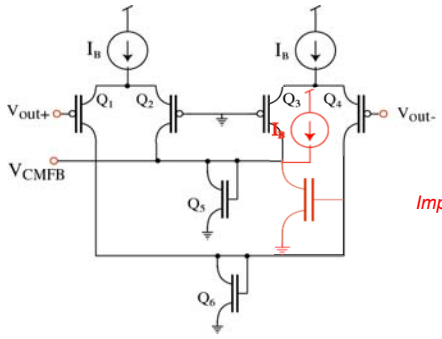
  - pMOS version also feasible
    - nMOS for high-order pole bandwidth limitations and lower thermal noise
    - pMOS for high DC-gain and unit-gain bandwidth and lower flicker noise

Common-mode feedback

- Two approaches:
  - Continuous time
  - Switched capacitor (SC)
- The purpose of the CMFB circuit is to keep the common-mode (average) output voltage at a constant level
  - Halfway between the power-supply voltages
- The speed of the CMFB circuit should be comparable to the unity-gain frequency of the differential path
  - Avoiding noise on the power rails



- Continuous time, double diff pair



Improved common mode gain

  - Positive difference will increase V_{cmfb}
  - Negative difference will decrease V_{cmfb}
- Negative feedback through lower current regulator

Common mode gain

- Differential input

$$V_{in} = V_+ - V_-$$

- Common mode voltage

$$V_{CM} = \frac{V_+ + V_-}{2}$$

  - Real amplifiers are non-ideal:

$$V_{out} = Av_{in} + A_{CM}v_{CM}$$

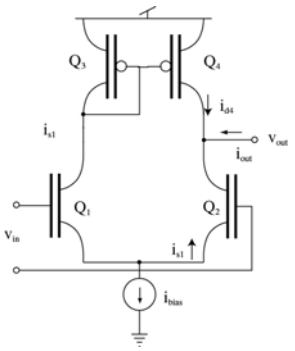
    - A should be large while A_{CM} should be small
  - Common mode rejection – CMRR

$$CMRR = 20\log\frac{|A|}{|A_{CM}|}$$

  - Power supply rejection ration – PSRR

$$PSRR = 20\log\frac{|V_{out-ripple}|}{|V_{ripple}|}$$

    - Ratio between power ripple and the ripple visible on the output



Keypoints

- Classical opamp: differential input stage + CS 2. stage + optional unit-gain buffer
- Overall gain equal to product of stage gain
- Dominating pole is 2. stage input pole (CS) due to Miller effect
- Second pole at output → may be increase by 2. stage transconductance
- Slew rate giving maximum drive capability of output for large signals and may only be improved by 1) increase 1. stage effective voltage (g_{m1}) or move second pole upwards
- Compensation is done by pole splitting usually by exploring Miller capacitance
- Differential amps have less common mode noise, but require additional common mode feedback circuit on output stage
- Current mirror opamps are good and easy to use.