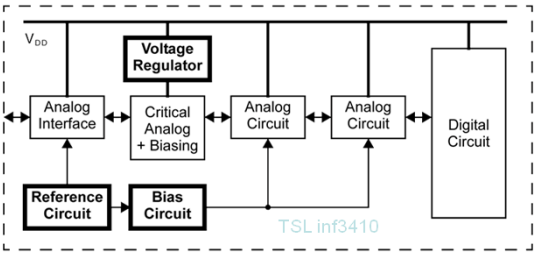
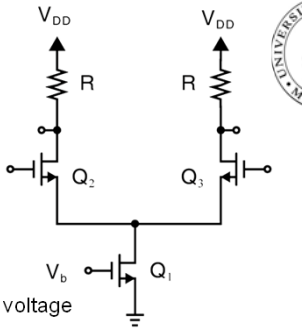
Biasing, references, regulators

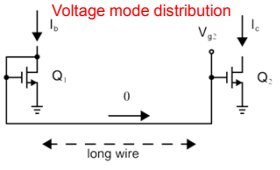
- Providing suitable working conditions for analog circuit elements
  - Bias circuit
    - Setting DC voltages or currents
  - Reference
    - Generate constant and absolute voltage
      - Independent of working conditions
  - Regulator
    - Improve DC voltage or currents keeping them stable

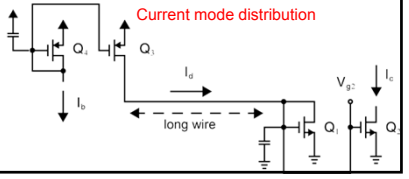


Bias circuits

- What bias voltage?
  - Assuming 10-20% device variations
  - Constant drain current in match diff-pair?
  - Constant voltage drop over R?
  - Constant gain?
- Good bias circuit
  - Monitor important parameters and adapt bias voltage
  - May be large
  - Must be reused by several sub-circuits
  - Using current mirrors
    - Voltage mode
      - Major variations due to mismatch
    - Current mode distribution
      - Somewhat better
      - Local mirror
      - Decoupling caps added locally

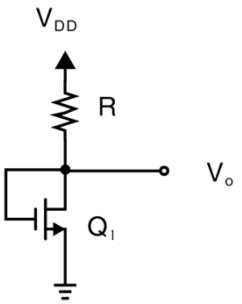




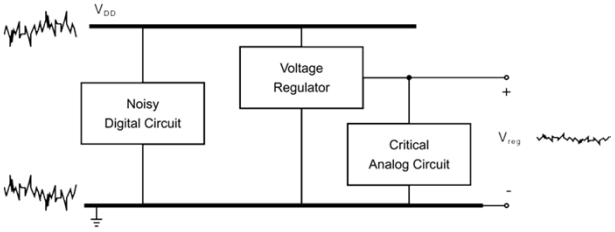


Reference circuits

- Proved some stable voltage for biasing
  - Simple combination of MOS + resistor
  - May size nMOS for suitable output voltage
    - Nonlinear element



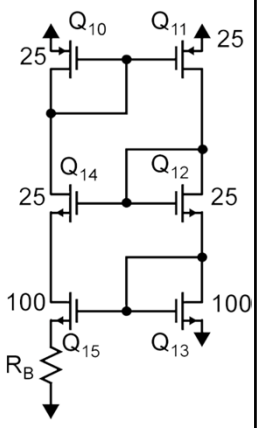
Regulator



- Reduce supply voltage
  - Stabilize supply voltage for improved performance
- Filter noisy supply
  - Ground ref may still convey noise

Constant transconductance

- Bias circuit maintaining constant transconductance
  - Assuming $(W/L)_{10} = (W/L)_{11}$
  - Same current in both branches
  - We have $V_{GS13} = V_{GS15} + I_{D15}R_B$
  - Giving: $V_{eff\,13} = V_{eff\,15} + I_{D15}R_B$
  - Since $I_{D13} = I_{D15} \qquad g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$
  - Giving $g_{mn} = \dfrac{2\left[1-\sqrt{\dfrac{(W/L)_{13}}{(W/L)_{15}}}\right]}{R_B} \approx g_{m13}$
  - For $(W/L)_{15} = 4(W/L)_{13} \Rightarrow \quad g_{m13} = \dfrac{1}{R_B}$
  - G_{m13} and all other nMOS transconductances are stabilized
    - Generated from same current $g_{mn} = \sqrt{\dfrac{(W/L)I_D}{(W/L)I_{15}}} \approx g_{m13}$

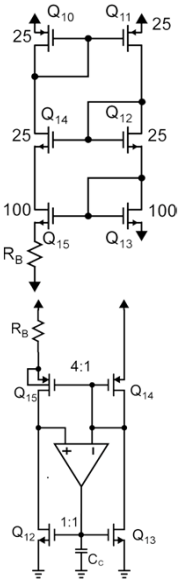


Constant transconductance

- PMOS devices

$$g_{mp} = \sqrt{\frac{\mu_p}{\mu_n}\frac{(W/L)I_D}{(W/L)I_{15}}} \approx g_{m13}$$

  - Unfortunately mobility variations are significant
- Additional compensation for
  - Temp, body …
- Second stable state
  - All zero → bootstrap circuit
- May increase power at high temperatures

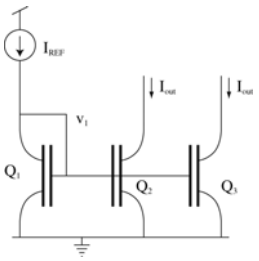


References

- Reference voltage or current
  - Used for controlling opamp characteristics
  - *Never submit a bias voltage directly from pad*
  - *Always use current input for setting references!*
    - Voltage
    - Current
- High quality reference (V or I)
  - Independent of supply voltage
  - Independent of process variations
  - Independent or well-defined temperature behavior
    - Balancing negative temperature dependence of PN junction (forward biased) with a positive temperature dependence of PTAT (proportional to absolute temperature) circuits

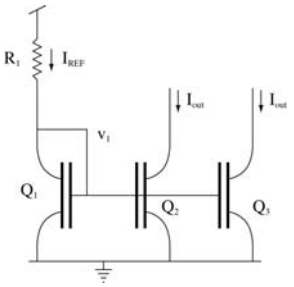
Reference circuit

- Generic reference



- Resistive current generator
  - Known load → good approximation
  - Sensitivite to Vdd

$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1}$$



Need some sort of self-biasing!

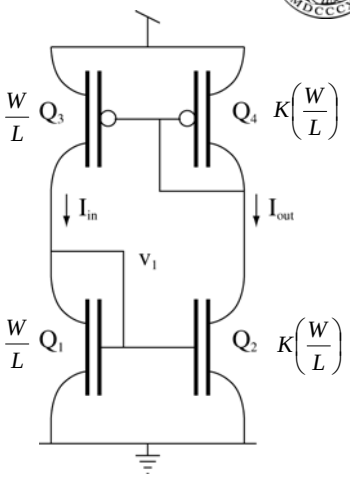
Supply independent current

- Bootstrapping reference
  - Using scaling

    $I_{out} = K \cdot I_{REF}$

    - Ignoring channel shortening
  - Diodes driven by current sources
    - Relatively independent of supply
    - Giving any current level with K

Tend to use power

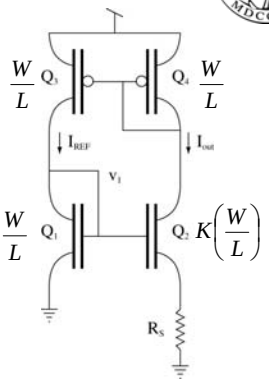


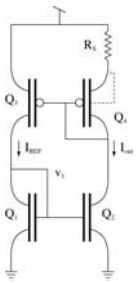
Reference with current control

- Resistor reduce Q_2 current
- P-mirror ensure $I_{out} = I_{REF}$
- Output current
  - Strong inversion behavior

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_n} \cdot \frac{1}{R_S^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2$$

    - Independent of supply
  - Body effect error
- Channel length modulation
  - Problematic in all these circuits





Start-up problem

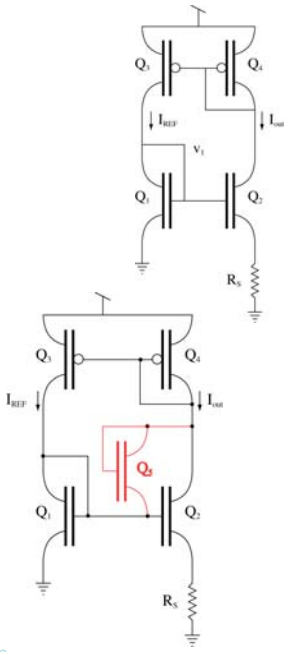
- Two stable operating points
  - Current defined by R_s and K
  - No current at all!
- Diode only working at start-up

$$V_{th1} + V_{th5} + |V_{th4}| < V_{DD}$$

  - Get some current

$$V_{gs1} + V_{th5} + |V_{th4}| > V_{DD}$$

  - Off during normal operation



Temperature compensation

- Combining positive and negative temperature dependence

$$V_{REF} = V_{neg-TC} + KV_{pos-TC}$$

  - Should give no temperature dependence (one must be scaled with K)
- Negative temperature source
  - PN junction diode

$$I_C = I_S \exp(V_{BE}/V_T) \text{ for } V_T = kT/q, I_S \propto \mu kTn_i^2$$

μ - mobility

n_i - minority carrier concentration

  - Forward biased diode temperature dependence

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T},$$

$$m \approx -3/2$$

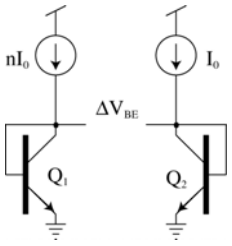
$E_g \approx 1.12eV$ - bandgap energy of silicon

  - Typical

$$V_{BE} \approx 750mV, T = 300^\circ K \rightarrow \partial V_{BE}/\partial T \approx -1.5 mV/^\circ K$$

- Positive temperature circuit
  - Two bipolars with different currents
    - *Base-emitter difference proportional to temperature*
      - Discovery from 1964

$$\Delta V_{BE} = V_T \ln n \Rightarrow \frac{\partial V_{BE}}{\partial T} = \frac{k}{q} \ln n$$



    - Room temperature

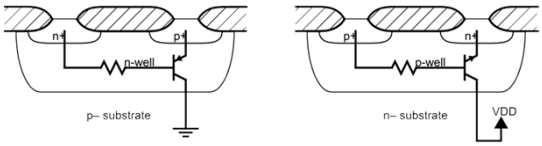
$$\partial V_T / \partial T \approx +0.087\, mV/^{\circ}K$$

- Bandgap reference

$$V_{REF} = V_{BE} + K\left(V_T \ln n\right)$$

  - Let $K \ln n \cdot 0.087\, mV/^{\circ}K = 1.5\, mV/^{\circ}K \Rightarrow K = 17.2$
  - Give $V_{REF} = V_{BE} + 17.2 V_T \approx 1.24V$

Parasitic PNP bipolar in CMOS



- Bandgap CMOS circuit
  - Left branch

$$V_{ref} = V_{EB1} + V_{R1}$$

  - Assume high gain amp giving same voltage

$$V_{R2} = V_{EB1} - V_{EB2} = \Delta V_{EB}$$

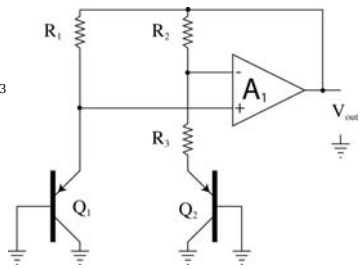
  - Current through R_2 equal current through R_3

$$V_{R3} = \frac{R_3}{R_2} V_{R2} = \frac{R_3}{R_2} \Delta V_{EB}$$

  - Voltage over R_1 equal voltage over R_3

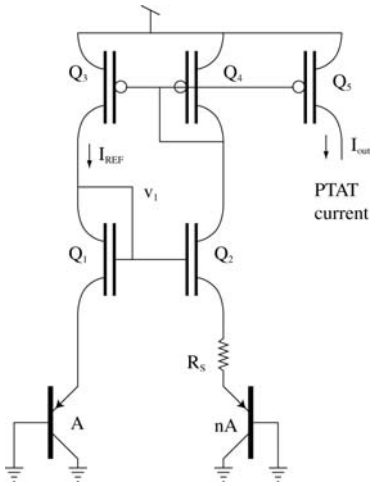
$$V_{ref} = V_{EB1} + \frac{R_3}{R_2} \Delta V_{EB}$$

  - giving $K = \frac{R_3}{R_2}$



PTAT current generator

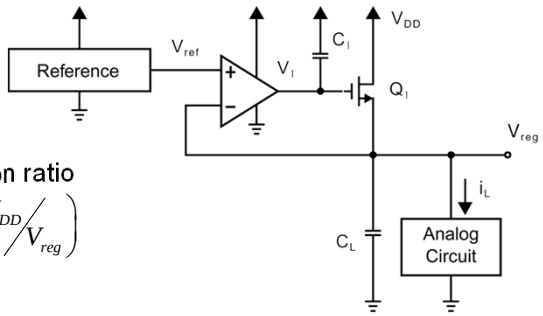
- Read off the compensated current



Voltage regulators

- Quiet and stable on-chip voltage
  - Input reference
  - Amp gain

$$V_{ref} \approx V_{reg}$$

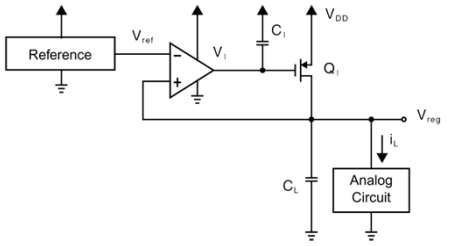


- Specifications
  - Power-supply rejection ratio

$$PSSR(\omega) = 10\log_{10}\left(V_{DD}/V_{reg}\right)$$

  - Output impedance
  - Dropout voltage
    - Minimum voltage between supply and regulated voltage

Low Drop-out regulator

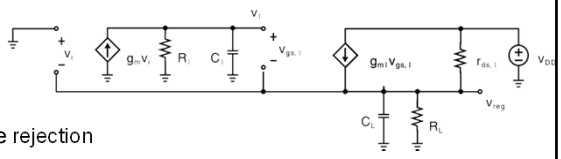


- Dropout voltage
  - Maximum regulated voltage
- pMOS for minimal voltage drop
  - Notice reversed amp polarity
- Regulating loop

$$L(s) = \frac{G_{ma} R_{oa} g_{m1} R_L'}{\left(1 + \frac{s}{\omega_{pa}}\right)\left(1 + \frac{s}{\omega_{pL}}\right)}$$

- Amp pole

$$\omega_{pa} = \frac{1}{R_{oa} C_1'} \qquad C_1' = C_1 + C_{gs1}$$



  - Amp pole dominant → worse rejection
- Output pole

$$\omega_{pL} = \frac{1}{R_L' C_L}$$

  - Output ole dominant → more power in feedback amp