

Digital Design of a Digital Combination Lock

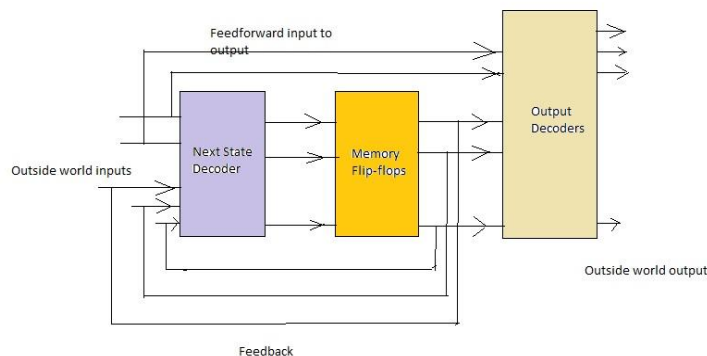
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ABSTRACT: This paper investigates a finite state machine based combination (Digital) lock using several modules, both combinational and sequential circuitry, using Verilog coding and simulated in Xilinx ISE 14.2.

1. INTRODUCTION

In this design, the main part is the FSM based controller. The function of that controller is to detect when a user has entered the 4 digit secret code. Now a Finite State Machine is basically a sequential circuit which follow pre-user-defined number states to control a number of inputs where each and every state is a stable entity that the FSM can occupy. It consists of a next state decoder, memory flip-flops and output decoder. Two kinds of finite state machine occur, viz. Moore machine and Melay machine. Now the Moore machine differs from the Melay one in the sense that it does not have any feed-forward paths. The following figure shows the block diagram of a Melay based FSM.



Now I'll define all the input and output ports and interconnect them such a way in Verilog coding so that one can utilise the combination lock.

2. DESIGNED CIRCUITRY AND ITS FUNCTION

In the very beginning of this project ,I developed a the following circuit diagram which consists of the key-pad-through which the user can press the secret code word to open the lock, decimal to BCD encoder, two-bit counter, mux and an 8 input nand gate. But in this design some kinds of synchronisation problems occur among the mux output and encoder output.

For this reason I changed the design methodology.

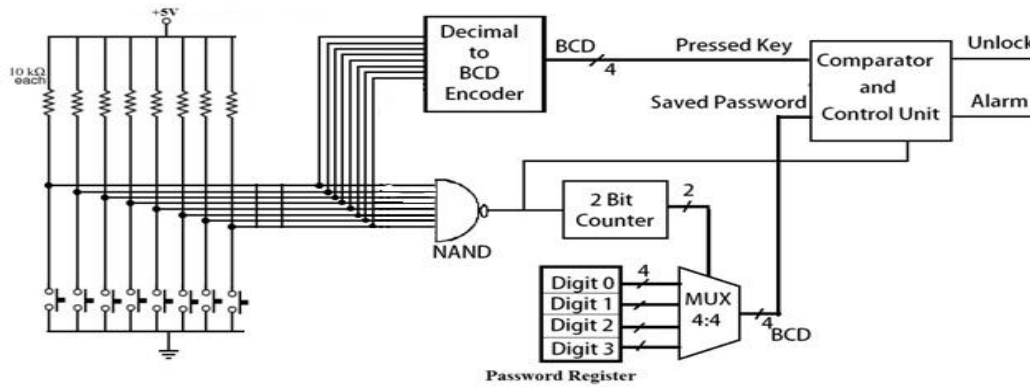


Fig. 1 Basic combinational lock system

Now to modify the above problem and to introduce better and secured functioning I introduced two edge-detector circuits, a timer circuit and a seven-segment display. The following diagram shows the new proposed digital combination lock system.

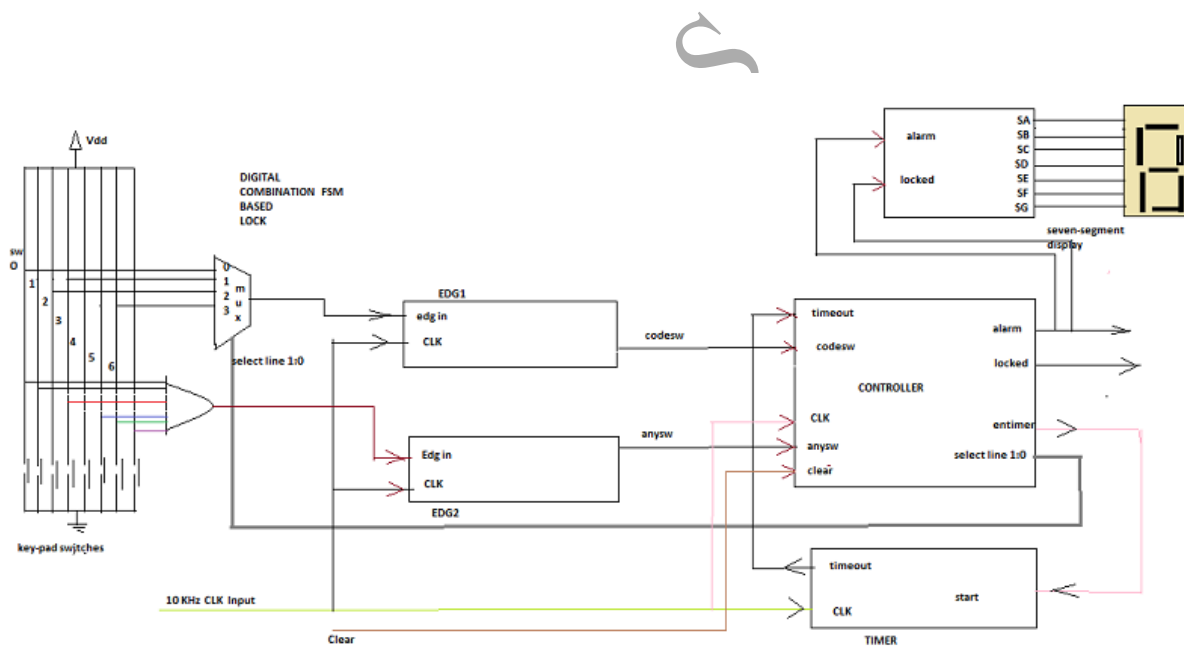


Fig. 2 Proposed digital combination lock system

It has eight active-low push button switches where switches 0,3,2 and 6 are hardwired through a 4:1 multiplexer. It is the secret code word. The 8 input AND gate provides Allsw that goes to 0 if any switch is pressed. The mux output goes 0 logic if the switch being pressed corresponds to mux select address input as mux is able to select each switch in the code in a correct sequence. Mux output will go low only when the correct switch has been pressed.

Up to this point, the circuit operates asynchronously. But the controller is a fully synchronous environment. So the mux output and Allsw output is totally unpredictable and creates erroneous output. This problem is overcome by using edge detector circuit labelled edg1 and edg2. The edge detector produces a single clock cycle length logic 1 pulses at the output. The codesw and anysw are feed directly into the controller. The edge detectors and FSM are clocked by the same signal to ensure proper synchronisation.

The block diagram indicates a Timer circuit which interfaces with the FSM via entimer(enable timer) and timeout(timer timed out)clocked by the same clock which provides an automatic locking mechanism returning the system to the locked state after a delay of 30 s subsequent to the system entering the unlocked state. The master clock signal is intended to have a frequency of 10 Hz, so the timer implements the required delay by counting to 300.

The controller works based on the following state diagram.

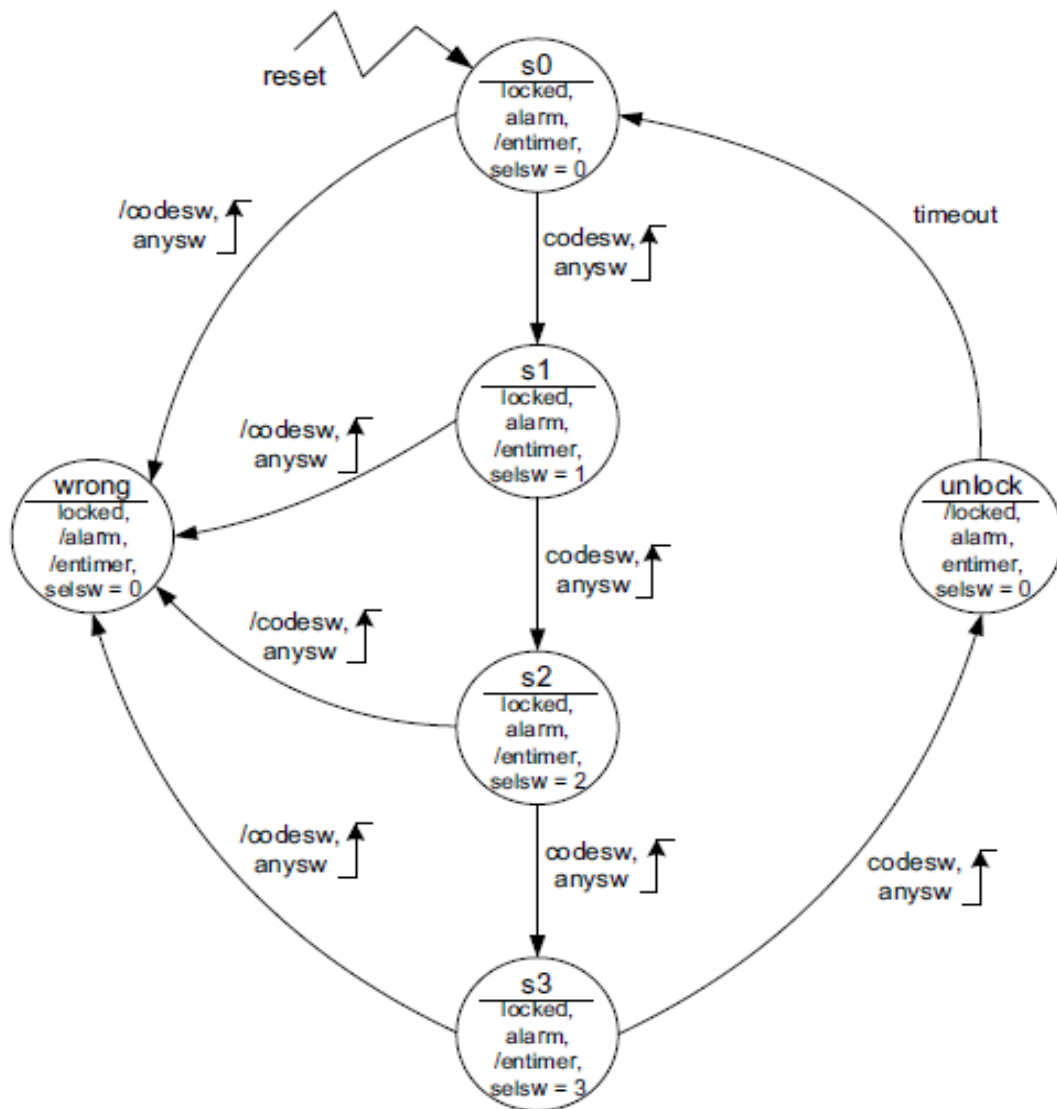


Fig. 3 Diagram of controller works

3. EXPERIMENTAL RESULTS

In the Verilog coding, the test module generates a 10 Hz clock using an initial sequential block-coding.

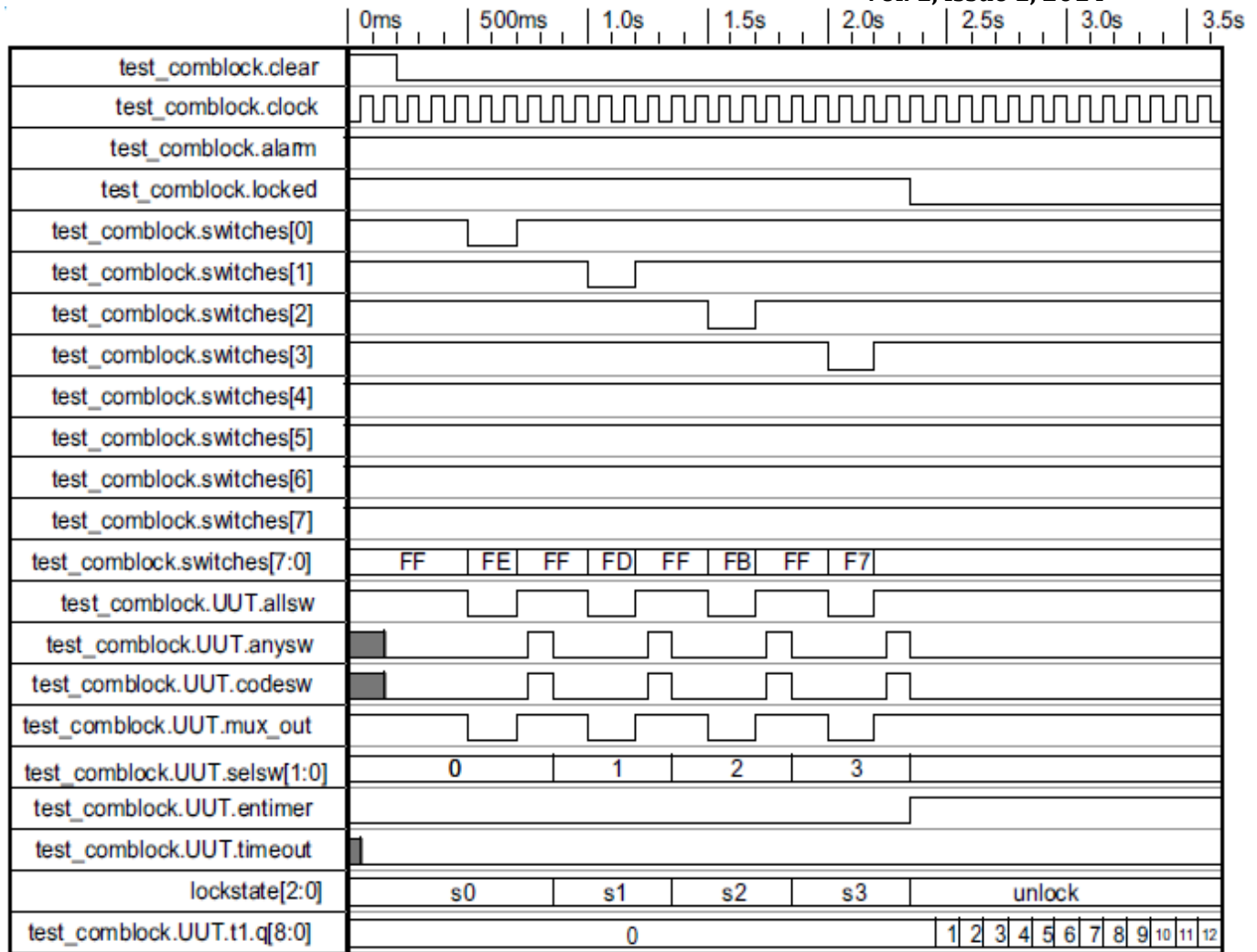


Fig. 4 Combination lock simulation using Xilinx ISE for the application of the correct switching sequence.

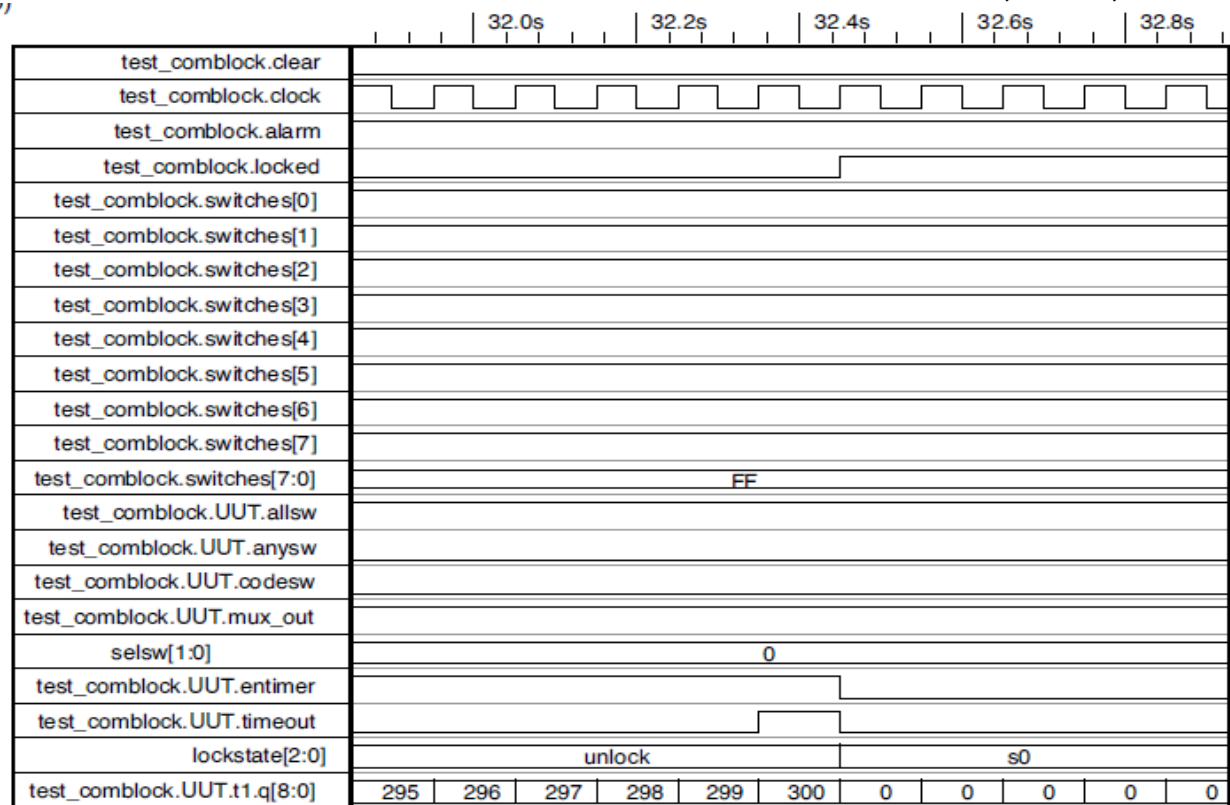


Fig. 5 Automatic locking feature.

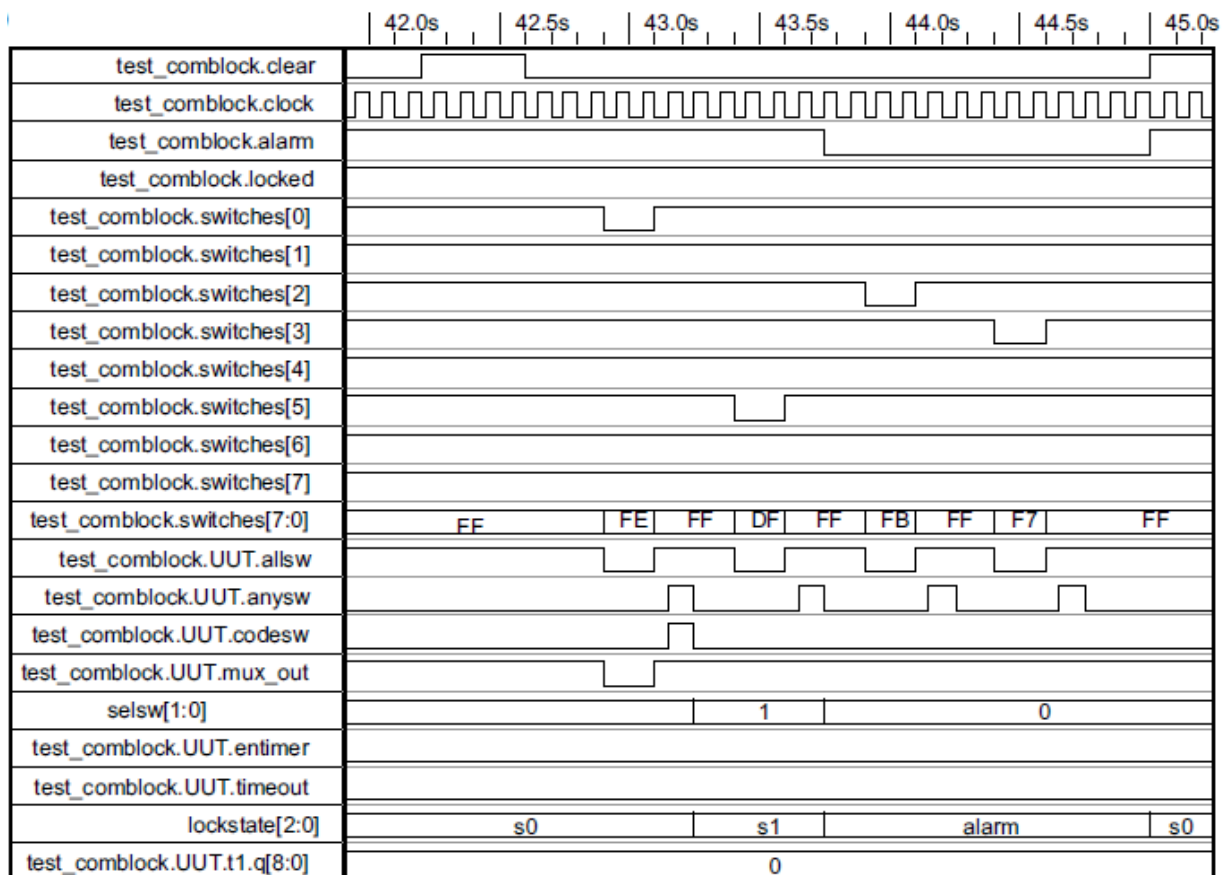


Fig. 6 incorrect key input sequence.

4. CONCLUSION

The whole digital lock system provides a secured architecture and without knowing the correct password sequence, it is impossible to open it. In every wrong entry, the system goes in a locked state and an alarm occurs. However, if the total power loss of the system occurs, then it will go in the locked state and in that time nobody can open it. To solve this problem, an internal battery connection is required to activate the system during power failure.

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