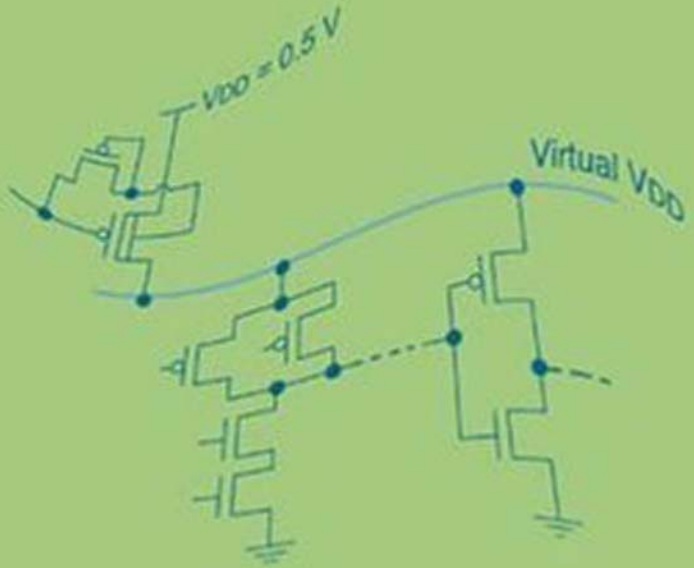
Fully-Depleted SOI CMOS Circuits and Technology

for Ultralow-Power Applications



Takayasu Sakurai
Akira Matsuzawa
Takakuni Douseki

Springer

FULLY-DEPLETED SOI CMOS CIRCUITS AND TECHNOLOGY FOR ULTRALOW-POWER APPLICATIONS

Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications

by

TAKAYASU SAKURAI
University of Tokyo, Japan

AKIRA MATSUZAWA
Tokyo Institute of Technology, Tokyo, Japan

and

TAKAKUNI DOUSEKI
NTT MicroSystem Integration Labs., Kanagawa, Japan

Springer

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List of Contributors

Numbers in parentheses indicate the chapter.

Makoto Yoshimi (1), (8.3.2), SOITEC Asia, Inc.
Hideaki Matsuhashi (2), Oki Electric Industry Co. Ltd.
Toshiaki Tsuchiya (2.2), Interdisciplinary Faculty of Science and Engineering, Shimane University.
Yasuhisa Omura (2.3), Department of Electronics, Kansai University.
Akira Matsuzawa (3), Tokyo Institute of Technology.
Takakuni Douseki (3.2-3.5), (4), (7), NTT Microsystem Integration Labs., NTT Corporation.
Hiroshi Shimomura (3.9), Semiconductor Company, Matsushita Electric Industrial Co., Ltd.
Masashi Yonemaru (4.3), AV Systems Group, Sharp Corporation.
Koji Fujii (4.4), NTT Microsystem Integration Labs., NTT Corporation.
Atsushi Kameyama (4.4), (5.4), STI-DC, Toshiba America Electronic Components, Inc.
Hiroshi Kawaguchi (4.7), Institute of Industrial Science, University of Tokyo.
Tsuneo Tsukahara (5), (7.2), NTT Microsystem Integration Labs., NTT Corporation.
Minoru Kozaki (5.2.1), Semiconductor Operations Div., Seiko Epson Corporation.
Masayoshi Kinoshita (5.2.2), Semiconductor Company, Matsushita Electric Industrial Co., Ltd.
Akihiro Sawada (5.2.7), Semiconductor Company, Matsushita Electric Industrial Co., Ltd.

Yasuyuki Matsuya (5.3), NTT Microsystem Integration Labs., NTT Corporation.
Jun Terada (5.3.1), NTT Microsystem Integration Labs., NTT Corporation.
Yoshitsugu Inagaki (5.3.3), Semiconductor Company, Matsushita Electric Industrial Co., Ltd.
Tsuneaki Fuse (5.4), Broadband System LSI Development Center, Semiconductor Company, Toshiba Corporation.
Yusuke Ohtomo (5.5), NTT Microsystem Integration Labs., NTT Corporation.
Hiroshi Koizumi (5.5.5), NTT Microsystem Integration Labs., NTT Corporation.
Shunsuke Baba (6), (7.3), Oki Electric Industry Co. Ltd.
Kazuyoshi Nishimura (6.4), NTT Microsystem Integration Labs., NTT Corporation.
Yoshifumi Yoshida (7.4), Seiko Instruments Inc.
Norio Hama (7.4), Semiconductor Operations Div., Seiko Epson Corporation.
Tohru Mogami (8), System Device Research Labs., NEC Corporation.
Toshiro Hiramoto (8.2), Institute of Industrial Science, University of Tokyo.
Ken Uchida (8.3.1), Advanced LSI Technology Laboratory, Toshiba Corporation.
Shin-ichi Takagi (8.3.1), Graduate School of Frontier Science, University of Tokyo.
Toshinori Numata (8.3.3), Advanced LSI Technology Laboratory, Toshiba Corporation.
Takayasu Sakurai (8.4), Center for Collaborative Research, and Institute of Industrial Science, University of Tokyo.

PREFACE

The most important issue confronting CMOS technology is the power explosion of chips arising from the scaling law. Bulk-Si devices are now running into a number of fundamental physical limits, and SOI technology provides a promising low-power solution to chip implementation. Research and development on SOI technology have been accelerating rapidly since 1998, when IBM announced that they would use partially-depleted (PD) SOI technology to make the PowerPC MPU. Motorola and AMD have also produced a number of MPUs made with SOI devices. Recently, Sony, Toshiba, and IBM announced that they would employ SOI devices for the next-generation broadband engine: the CELL processor.

The next generation of SOI technology employs fully-depleted (FD) devices. According to the ITRS roadmap, FD-SOI technology will be necessary to preserve the scaling law. It has the additional advantage of ultralow-power operation, with the power consumption being less than 10 mW. Ultralow-power VLSIs are attracting a great deal of attention because they will be key components of network computing and services in the coming ubiquitous-IT society. The visible manifestation of this trend is the increasing number of mobile phones, electronic dictionaries, game sets, and personal digital assistants, for which it is imperative to reduce the power consumption as much as possible to prolong battery life. Oki Electric began producing a microcontroller and an RF chip made with FD-SOI devices for use in ultralow-power radio-controlled watches. As the demand for smaller, more

power-efficient devices grows, FD-SOI technology will become increasingly important.

Technical books on circuit design methods for PD-SOI devices in applications such as ultrahigh-speed microprocessors have been published; but no books have yet appeared that systematically cover design methods for FD-SOI devices in ultralow-power applications. This book covers topics ranging from the minimum required knowledge of the fabrication of SOI substrates and FD-SOI devices to the latest developments in device and process technologies, ultralow-voltage circuits such as digital circuits, analog/RF circuits, and DC-DC converters. Each technique is fully explained using figures. Furthermore, the book gives three examples of ultralow-power applications based on FD-SOI technology, providing every reader with practical knowledge on the technology and the circuits.

We hope that this book will further the understanding of FD-SOI technology and ultralow-voltage circuit techniques for FD-SOI devices.

Acknowledgements

In 1978 Katsutoshi Izumi (formerly of NTT, and now a professor at Osaka Prefecture University) invented the SIMOX substrate, a type of SOI substrate; and since that time, NTT has been involved in research and development on SOI technology as it relates to substrates, device fabrication, and circuits. Just 20 years later, Tetsushi Sakai (now a professor at the Tokyo Institute of Technology) and his group demonstrated the effectiveness of high-speed, low-power fully-depleted (FD) SOI devices in a 120K-gate-level CMOS VLSI on a SIMOX wafer. The FD-SOI technology we see today in Japan is due in large part to the inventiveness and persistence of Izumi and Sakai. The authors are grateful to them for their guidance and foresight.

This book concerns the application of FD-SOI devices to ultralow-voltage, ultralow- power wireless systems. It is based on the findings and achievements of the Japanese national SOI project, which was supported by the New Energy and Industrial Technology Development Organization. The management efforts of Junzo Yamada and Hakaru Kyuragi (now with NTT Electronics) in the SOI project are greatly appreciated, as is the help with the fabrication of FD-SOI LSIs provided by Katsuzi Iguchi, Akio Kawamura, and Toshio Naka of Sharp Corporation, and Kiyotaka Imai and Shinya Maruyama of NEC Corporation.

The authors also thank Professors Kunihiro Asada (Tokyo University) Hiroshi Ishihara (Tokyo Institute of Technology), and Mitsumasa Koyanagi (Tohoku University) for their sustained faith in the technology's promise and for their valuable comments. The authors are also indebted to the following individuals for their valuable support and for helpful discussions: Yuichi Kado and Mitsuru Harada (NTT Corporation); Eiji Ikuta and Kazuya Fujimoto (Sharp Corporation); Koichi Oguchi, Teruo Takizawa, and Aritsugu Yajima (Seiko Epson Corporation); Jun Osanai and Fumiyasu Utsunomiya (Seiko Instruments Inc.); Mutsumi Mitarashi, Kouichi Morikawa, Kouichi Tani, and Tadashi Chiba (Oki Electric Industry Co. Ltd.); Junji Nakatsuka (Matsushita Electric Industrial Co., Ltd.); Shigeyoshi Watanabe (Toshiba Corporation); Kiyoshi Takeuchi and Toshiaki Koh (NEC Corporation), Takao Yonehara and Kazuhiko Ohmi (Canon Inc.); and Shouji Shiraishi (JEITA). Finally, we would like to express our appreciation to Yoshie Kinebuchi for her editorial support.

Chapter 1

INTRODUCTION

1.1 Why SOI?

Reducing power consumption has become the most important issue in LSI circuit technology. Bulk-Si devices are now running into a number of fundamental physical limits. Among the problems are that the carrier mobility is decreasing due to impurity scattering, the gate tunneling current is increasing as the gate insulator becomes thinner, and the p-n junction leakage is increasing as the junction becomes shallower. These trends make conventional scaling less and less feasible. As a result, the operating voltage tends to be set higher than what a scaled-down device was expected to need to achieve the desired speed performance. This is certainly the case for MPUs, for which speed is the top priority. The heat generated by today's MPUs is close to exceeding the level that can be handled by conventional cooling schemes. On the other hand, ubiquitous network computing is becoming a reality in our daily lives because of the many conveniences it affords. The visible manifestation of this trend is the increasing number of mobile phones, electronic dictionaries, game sets, and personal digital assistants (PDAs). In these systems, it is imperative to reduce the power consumption as much as possible to prolong battery life.

Silicon-on-insulator (SOI) technology features a low capacitance, which enables high-speed operation. That is, the supply voltage can be lowered to cut power consumption while adequate speed is provided. However, the advantages

of SOI technology are not limited to the areas of speed and power; they also include good radiation hardness, the ability to withstand high temperatures, and the ability to handle high voltages. This technology also enables the fabrication of micro-electro-mechanical systems (MEMS) for control systems. Furthermore, it allows flexible device design; for example, the properties of the substrate can be set independently of those of the device layer because an insulator separates devices from the substrate.

The fully-depleted (FD) SOI MOSFET discussed in this book is a special type of SOI MOSFET. In addition to high speed and low power, it exhibits steep subthreshold characteristics, negligible floating-body effects, and small short-channel effects.

The purpose of this chapter is to provide the reader with basic information on SOI and FD-SOI MOSFETs. The topics include the structure of an SOI substrate, the history of the technology, the differences between FD- and PD-SOI MOSFETs, and applications of SOI technology.

1.2 What is SOI? — Structure —

Figure 1.1 compares the structures of bulk-Si and SOI substrates. The key feature of the SOI structure is the layer of silicon dioxide just below the surface. It is called the buried oxide (BOX), and is made by the oxidation of Si or oxygen implantation into Si, as described later. Regarding the thin Si film on the BOX, if it is single crystal, the MOSFETs made in it are called SOI devices; but if it is polycrystalline, then they are called thin-film transistors (TFT), which is a different category of devices. This film is called the top Si layer, the SOI layer, or just the Si film. The Si substrate beneath the BOX is called just that—Si substrate—or supporting substrate, handle wafer, or base wafer. The terms “Si body” and “SOI body” refer to the part of the SOI layer that constitutes the body of a MOSFET.

The range of thicknesses of the SOI and BOX layers in Fig.1.1 are those typically used in LSI applications. Figure 1.2 shows where common SOI applications fall in a graph that plots these two thicknesses against each other. It is common to use a BOX several microns thick both for MEMS, in which case the mechanical parts are made in the SOI layer, and for high-power applications, which must withstand high voltages of several tens or hundreds of volts. For CMOS LSI applications, which are the main interest of this book,

the thickness of the SOI layer is different for partially-depleted (PD) and fully-depleted (FD) devices. The features of these devices will be discussed in detail later, but here it should be pointed out that the thickness of the SOI layer for an FD-SOI MOSFET is usually set to about one-third the effective channel length in order to avoid a punch-through current. So, the SOI layer is much thinner in FD- than in PD-SOI devices. Moreover, it becomes thinner, as devices are scaled down.

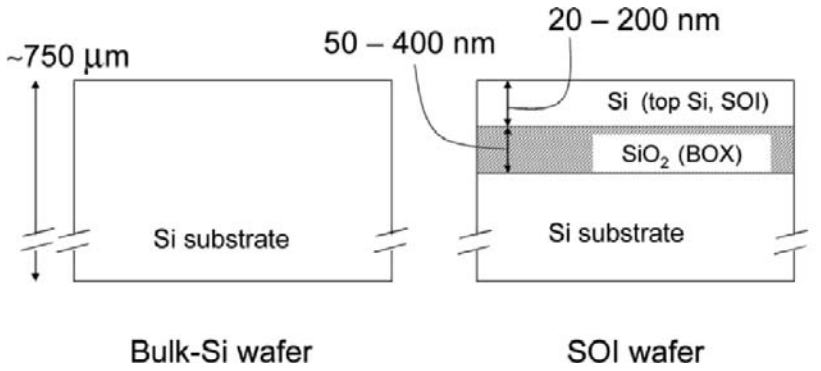

Fig. 1.1 Structures of bulk-Si and SOI substrates for CMOS LSIs.

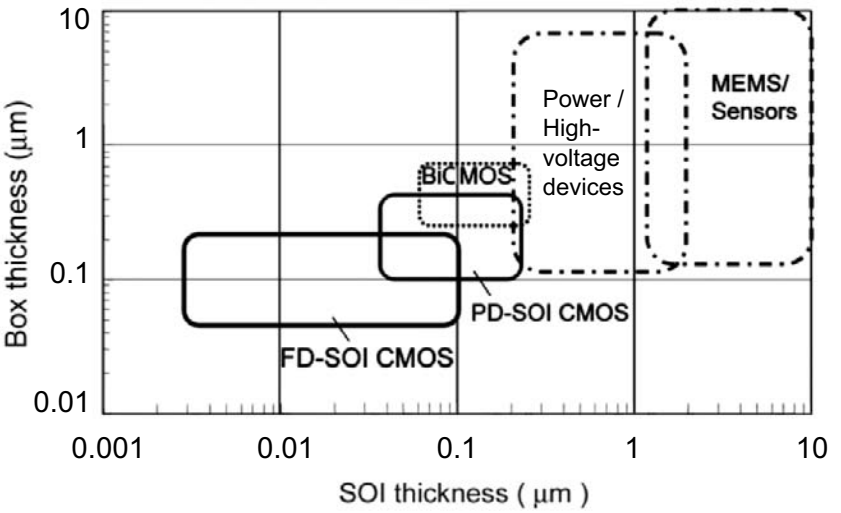

Fig. 1.2 Classification of SOI applications according to thicknesses of SOI and BOX layers.

1.3 Advantages of SOI

The BOX layer gives SOI MOSFETs many advantages over their bulk-Si counterparts. The ones listed below are common to PD- and FD-SOI devices. Those specific to the FD-SOI structure will be described in Section 1-5 and in more detail in Chapter 2.

A. Negligible drain-to-substrate capacitance

Figure 1.3 shows a schematic diagram of the capacitances in bulk-Si and SOI MOSFETs. In SOI devices, the capacitance between the drain (source) and the substrate is negligibly small because of the dielectric constant of SiO_2, which is lower than that of Si, and the thickness of the BOX. This helps improve the switching speed of CMOS devices, as can be seen in the relationship between power consumption and access time for a 4-Mb SRAM in Fig. 1.4 [1.1]. For a given access speed, SOI devices consume only one-half to one-third the power of bulk Si devices; and for a given power consumption, they are 20% to 25% faster. This amount of improvement is typical for SOI CMOS. It is worth noting that this improvement in speed roughly corresponds to the performance gain obtained by jumping ahead one technology generation.

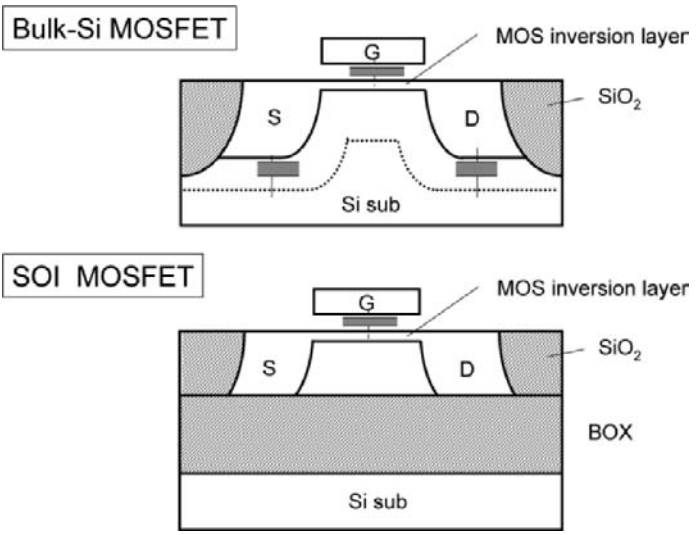

Fig. 1.3 Capacitances of bulk-Si and SOI MOSFETs.

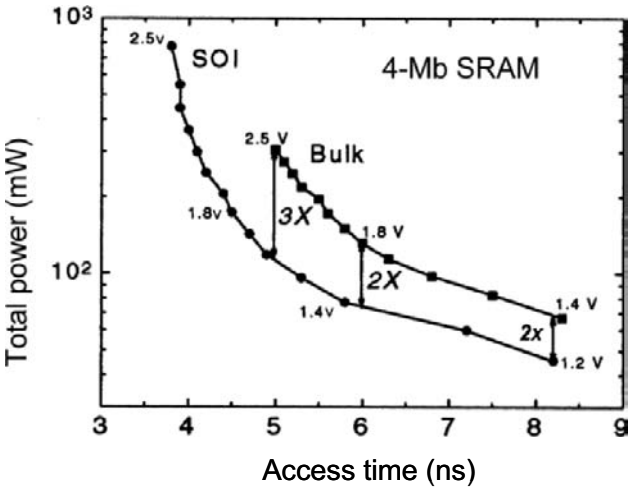

Fig. 1.4 Speed and power consumption of bulk-Si and SOI MOSFETs [1.1]. *(Reproduced by permission of The Electrochemical Society, Inc.)*

B. Positive body bias improves speed of stacked gates

The independent body bias of SOI MOSFETs makes them faster in a stacked-gate structure. In the stacked gates made with bulk-Si MOSFETs in Fig. 1.5, the negative body bias of the circled transistor is generated by the current flowing to the ground. This increases the threshold voltage and lowers the operating speed. In contrast, the body bias of stacked SOI MOSFETs is positive because it takes a value between the source and drain biases. This yields a lower threshold voltage for stacked transistors, thereby enhancing the operating speed. It should be noted that the advantage of stacked gates is that they reduce the area occupied by a circuit.

C. No latch-up

Latch-up occurs when the parasitic p-n-p-n (or n-p-n-p) thyristor in a CMOS structure turns on, which limits the maximum operating voltage. Figure 1.6 shows that, unlike a bulk-Si device, there is no parasitic thyristor in an SOI device. As a result, it is immune to latch-up; and thus there is no need for either a special circuit layout to prevent latch-up or a special device process, such as one to create a buried low-resistivity region.

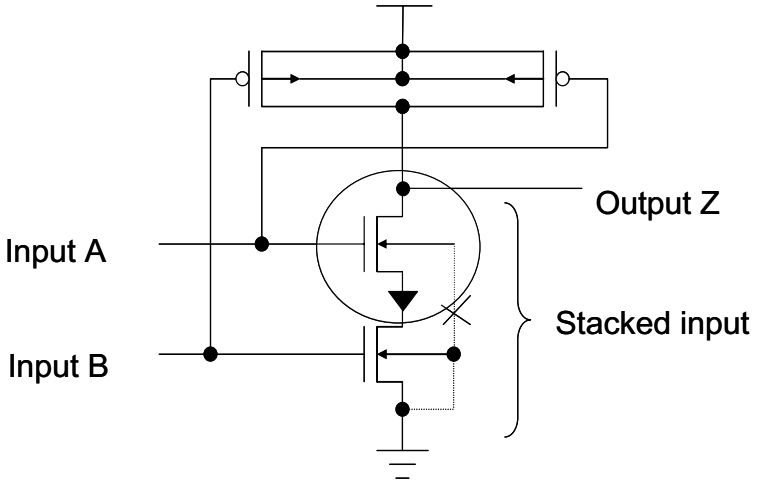

Fig. 1.5 Stacked gates provide high speed. The drain current of the circled MOSFET is enhanced in an SOI structure due to the lack of body effects.

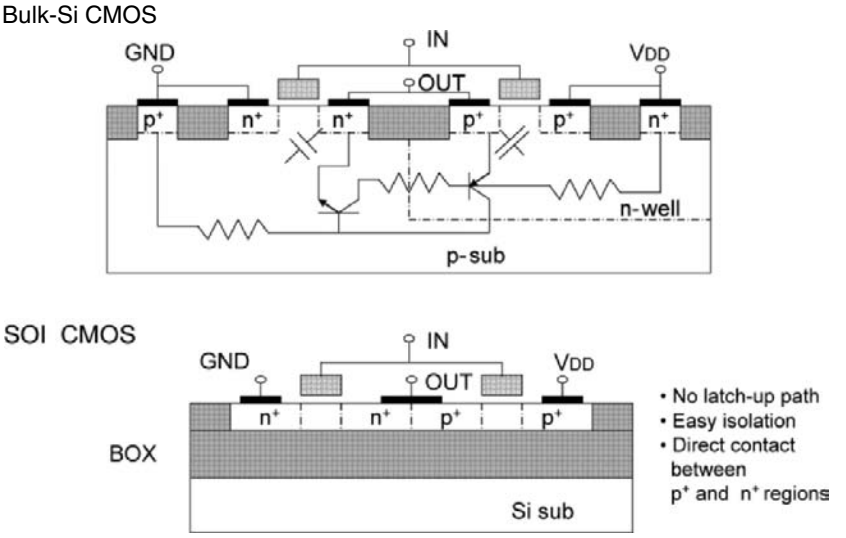

Fig. 1.6 Unlike bulk devices, SOI devices have no parasitic thyristor, and thus are latch-up free. The fabrication process is also simpler.

D. Ideal device isolation and smaller layout area

SOI devices are laterally isolated from each other by an insulator film, and vertically isolated from the substrate by the BOX, which makes the isolation ideal. As a result, devices can be packed closer together than bulk ones. In addition, the n^+ and p^+ diffusion regions at the output of a CMOS inverter can be connected directly to each other, as shown in Fig. 1.6, which makes the area of a device smaller than that of a bulk one. The shallow-trench-isolation (STI) process is also simpler because the groove to be filled is very shallow.

E. Good soft-error immunity

SOI devices exhibit excellent radiation hardness to alpha particles, neutrons, and other particles. Alpha particles are generated by trace amounts of radioactive elements in IC materials. They have an energy of approximately 5 MeV, which enables them to penetrate Si to a depth of about 25 μm. Along the trajectory, they generate electron-hole pairs, which results in negative and positive charges of around 10 fC in every micron. This is sufficient to destroy the memory charge of a DRAM cell or upset the memory state of an SRAM. Neutrons generated by secondary cosmic rays also induce soft errors [1.2].

Figure 1.7 shows the soft error rate (SER) for a 64-kbit DRAM made on an SOI substrate as a function of the thickness of the SOI layer [1.3]. The SER decreases as the layer becomes thinner. This indicates that most of the electron-hole pairs generated by alpha particles are blocked by the BOX and do not affect the device layers, as shown in the diagram on the right.

F. Small p-n junction leakage

The leakage current of a p-n junction is significantly smaller in an SOI structure because the impurities in the n^+ and p^+ regions diffuse deeply into the thin Si film, leaving a p-n junction only at the sidewall of the diffused area. A low p-n junction leakage current is generally beneficial in every type of application; but it is especially important in applications requiring a low stand-by power, such as mobile phones and PDAs, because it prolongs battery life.

Table 1.1 summarizes the advantages of SOI technology described above.

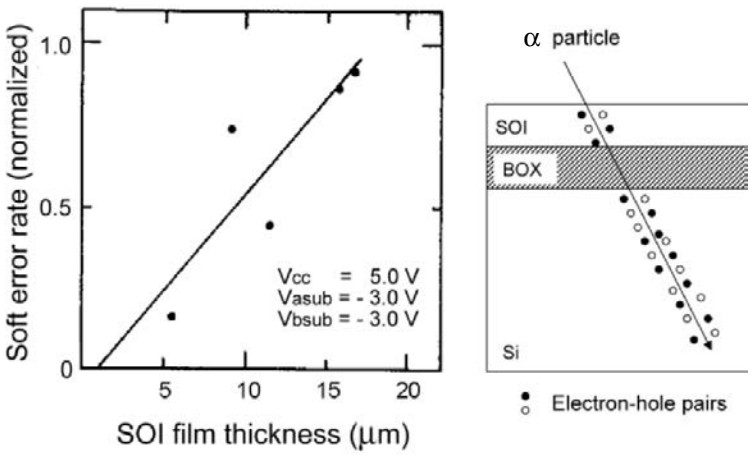

Fig. 1.7 Soft-error immunity of SOI DRAM. (From H. Gotou et al. [1.3]. ©1987 IEEE.)

Table 1.1 Advantages of SOI technology.

1.	Negligible drain-to-substrate capacitance
2.	Small body effects, fast stacked gates
3.	No latch-up
4.	Simple device isolation, smaller area
5.	Excellent radiation hardness
6.	Small junction leakage current
7.	Reduced short-channel effects

1.4 History of the Development of SOI Technology

This section reviews the history of the development of SOI technology. Before SOI technology became available for the production of ULSIs, a great number of issues ranging from the material for SOI wafers to device and circuit design had to be resolved. The problems were solved by a profusion of new ideas and a tremendous research effort. Table 1.2 lists the important events in the history of SOI technology.

The idea of building MOSFETs on an insulator goes back to the 1960s, and first implemented in the thin-film transistor (TFT) [1.4]. It subsequently appeared in the silicon-on-sapphire (SOS) structure, which was made by growing single-crystal Si epitaxially on single-crystal sapphire (Al_2O_3). SOS devices were expected to provide high-speed performance because of their low capacitance, and they were actually used to make high-speed logic LSIs [1.5] until the early 90s. However, SOS eventually gave way to bulk-Si technology in the high-speed area, because of some serious drawbacks: The high dislocation density arising from the lattice mismatch at the sapphire/Si interface caused a non-negligible leakage current in MOSFETs. The aluminum in the sapphire substrate tended to migrate into the epitaxial film, complicating the fabrication process. The residual compressive strain due to the large difference between the coefficients of thermal expansion of sapphire and Si degraded the electron mobility. Finally, floating-body effects produced abnormal behavior that negatively impacted circuit operation.

Table 1.2 History of development of SOI technology.

1978	Demonstration of CMOS by SIMOX (NTT, K.Izumi)
1981-90	3-dimensional IC project in Japan
1985	High-temperature annealing in SIMOX
1986	Fully-depleted SOI MOSFETs (HP, Toshiba)
1990	Lowering the operating voltage of LSIs (<2V)
1992	PACE (Hughes)
1994	ELTRAN (Canon)
1994	Low-dose SIMOX, ITOX technology (NTT)
1995	UNIBOND (LETI)
1997-2003	Gate array (Mitsubishi), PowerPC (IBM), MPC (Motorola), Watch controller (Oki), Opteron (AMD), CELL (Sony, IBM, Toshiba)

SOI devices for integrated circuits first became feasible with the development of separation by implanted oxygen (SIMOX) technology. In 1966, Watanabe and Tooi [1.6] implanted oxygen ions into Si using an RF gas discharge, and found the infrared absorption peak, the breakdown voltage, and the dielectric constant of the implanted film to be identical to those of thermally grown SiO_2.

In 1978, Izumi, et al. of NTT [1.7] discovered that the implantation of oxygen into Si at an acceleration voltage of 150 kV and a dose of 1.2 x 10^{18} cm^{-2} followed by annealing at a temperature of 1150°C produced a continuous buried SiO_2 layer with excellent electrical characteristics and left a thin layer of single-crystal Si on the surface. They called the technology SIMOX, and used it to demonstrate a fast 19-stage CMOS oscillator. Figure 1.8 illustrates the SIMOX process, including the improvements made in the 90s.

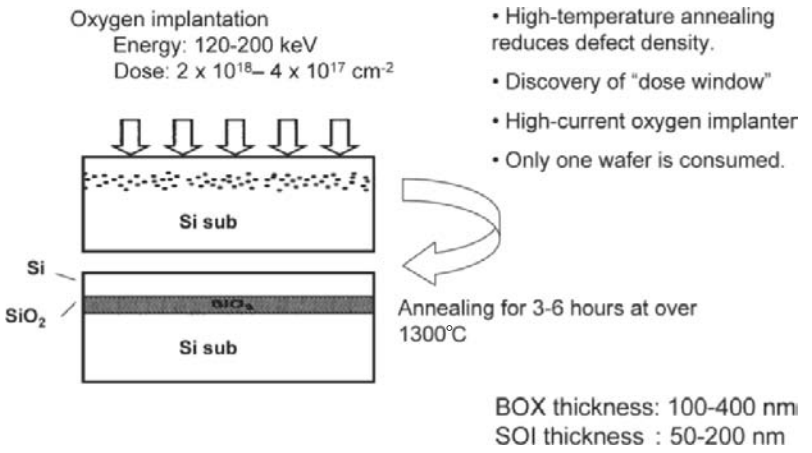

Fig. 1.8 SIMOX process [1.7].

The 80s saw intensive research on the technique of recrystallization with a laser or e-beam [1.8]. Studies in this area were also carried out as part of a Japanese national R&D project aimed at fabricating 3-dimentional integrated circuits (ICs). This project included research on the fabrication and evaluation of SOI substrates, the design and simulation of SOI devices, circuit design technology for 3D ICs, and many other things. These studies greatly enhanced our understanding of SOI devices. In particular, various abnormal phenomena caused by floating-body effects were analyzed in great detail using device simulations [1.9].

Fully-depleted (FD) SOI MOSFETs began attracting attention in the middle of the 80s because they have a number of advantages over partially-depleted (PD) devices [1.10], [1.11]. As will be shown later, FD devices exhibit much smaller floating-body effects and better characteristics in the short-channel

region. Still, for both types of devices, the drain breakdown voltage is at most 2 to 3 V, which is much less than the typical supply voltage (5 V) of the LSIs of that time. During that period, the main topics on which device engineers concentrated their efforts were the analysis of drain breakdown phenomena and the improvement of the drain breakdown voltage of SOI MOSFETs [1.12].

In the 90s, concern mounted that the ever-increasing power dissipation of LSIs could be a limiting factor. This triggered a transition from n-channel MOSFETs to CMOS FETs, which have since become the standard high-speed, low-power devices. At the same time, the supply voltage, the reduction of which is the key to lowering power consumption, started to drop from 5 V to 3 V to less than 2 V. Because of this, the low breakdown voltage of SOI MOSFETs, which had long been regarded as a fatal drawback, was no longer an issue, thus giving them an opportunity to make their debut.

Numerous demonstrations over the next several years showed that SOI CMOS FETs were 20% to 30% faster than bulk devices, and consumed one-third to one-half the power. This difference corresponds to about a one-generation jump ahead. Still, it seemed a bit too early for SOI to be considered a production-level technology for making LSIs because the SOI wafer technology was still immature (in terms of quality and production capacity), and the infrastructure for circuit design (device modeling, circuit design tools, etc.) was inadequate.

Regarding SIMOX technology, there was an important improvement in the 80s. It was found that raising the annealing temperature above 1300°C drastically reduced the dislocation density from 10^9 cm^{-2} to 10^6 cm^{-2} [1.13]. Moreover in the 90s, the “dose window” was discovered [1.14], ITOX technology was born [1.15], the throughput of SIMOX technology was increased by a factor of 5, the dislocation density was reduced to as low as 10^2 to 10^3 cm^{-2}, and a way was found to make the BOX/SOI interface smooth.

At the same time, the demand for high-quality SOI wafers was increasing. Wafer bonding [1.16], [1.17] was thought to be the solution to making good SOI wafers because it provided high crystal quality and a mass-production capability. However, the combination of wafer bonding and conventional grinding could not produce a top Si film of the required thinness (~100 nm) and uniformity (for instance, a variation in thickness of less than 10%).

In 1992, plasma-assisted chemical etching (PACE) was developed by Hughes Danbury Optical Systems [1.18]. As shown in Fig. 1.9, PACE involves wafer bonding, and then conventional grinding to thin the donor wafer (Wafer A) down to a thickness of several microns. Finally, the variation in the thickness of the SOI layer across the wafer is measured, and the layer is planarized with localized gas plasma by adjusting the scan speed according to the thickness of the Si. It has been reported that the variation in thickness can be reduced to just ±4.5 nm (±1.2%) for a film 374.3 nm thick. PACE is an extension of the technology used to polish the mirrors of the Hubble space telescope. The success of PACE opened the way to the use of wafer bonding for the fabrication of thin-film SOI wafers.

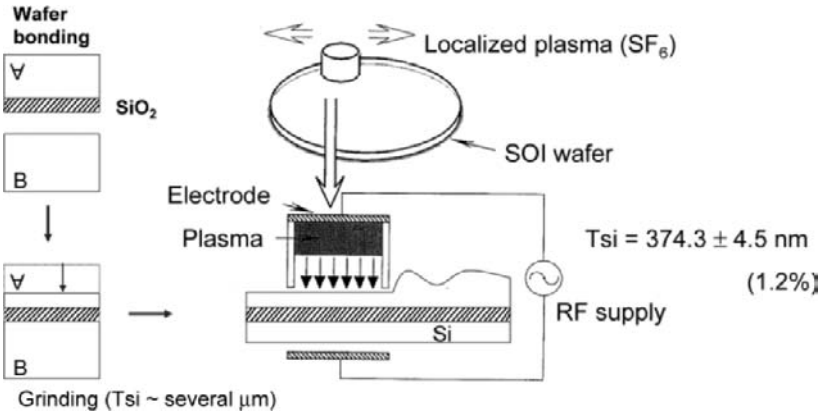

Fig. 1.9. PACE process [1.18].

In 1994, Canon developed the ELTRAN process (Fig. 1.10) [1.19]. First, a donor wafer is prepared by growing a double layer of porous Si on a Si substrate, epitaxially growing a layer of Si on top, and oxidizing the surface. Then, the donor wafer is bonded to a handle wafer; and the donor substrate is split from the porous Si layer with a jet of water. Finally, the wafer is completed by etching off the porous layer and planarizing the surface. Since the active SOI layer is made of epitaxial film, it is free from defects, such as crystal-originated particles (COPs), and thus has a high crystal quality. The donor wafer can be recycled.

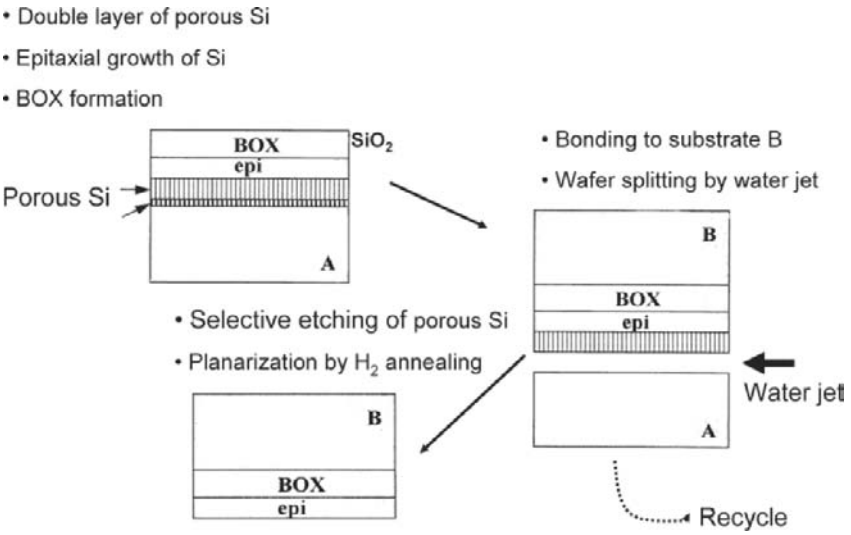

Fig. 1.10 The ELTRAN process [1.19].

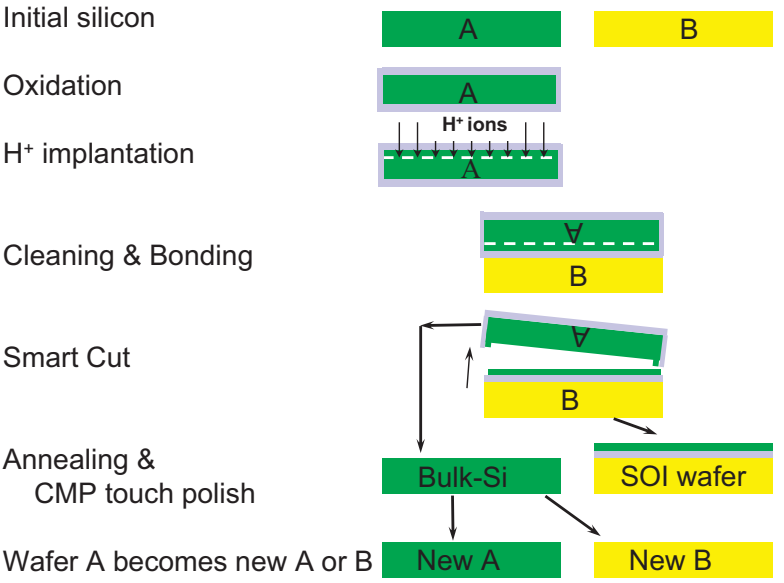

Fig. 1.11 The UNIBOND process [1.20].

In 1995, LETI reported a UNIBOND substrate made with Smart Cut technology [1.20]. The process (Fig. 1.11) involves implanting hydrogen into a Si donor wafer, bonding the donor to a handle wafer, splitting off the donor wafer at a temperature of 500 to 600°C, and finally planarizing the surface. The hydrogen dose required to strip the Si surface is from 3×10^{16} to 1×10^{17} cm^{-2}, which is less than the oxygen dose used for low-dose SIMOX. The donor wafer can be recycled in the same way as in ELTRAN technology.

In addition, SiGen Corporation reported that the use of plasma doping [1.21] rather than ion implantation to embed hydrogen in Si provides a higher throughput because of the high density of ions in the plasma.

As shown above, a number of ways of making SOI wafers were developed in the 90s. They were used for the test fabrication of various SOI devices, such as MPUs, low-power logic circuits, RF/mixed-signal circuits, DRAMs, and some others. These tests revealed both the advantages of SOI technology and also the problems that needed to be solved.

At the same time, circuit modeling and circuit simulation technology also made progress, which enabled circuit engineers to use commercially available circuit design tools equipped with reliable circuit models.

In the fall of 1997, Mitsubishi announced that they would market low-power gate arrays made with SOI technology [1.22]. In the following year, IBM announced that they would use it to make the PowerPC MPU [1.1]. Oki Electric, on the other hand, developed a microcontroller for a low-power watch made with FD-SOI MOSFETs [1.23], which was used in a Casio watch in 2001. Sony, Toshiba, and IBM announced in the same year that they would employ SOI for the next-generation broadband engine, CELL [1.24], [1.25]. Motorola announced that the number of MPU chips they produced with SOI technology from the beginning of 2002 to the fall reached 800,000 [1.26]. In the spring of 2003, AMD began marketing the 64-bit Opteron, an MPU made on an SOI process, and announced that they would make all future MPUs with SOI rather than bulk-Si technology [1.27].

In this way, SOI entered the mainstream of LSI technology. The range of applications now extends from MPUs and low-power LSIs to RF/mixed-signal and high-voltage circuits. Fig. 1.12 shows various SOI applications together with their current status; and Fig. 1.13 shows pictures of representative SOI products.

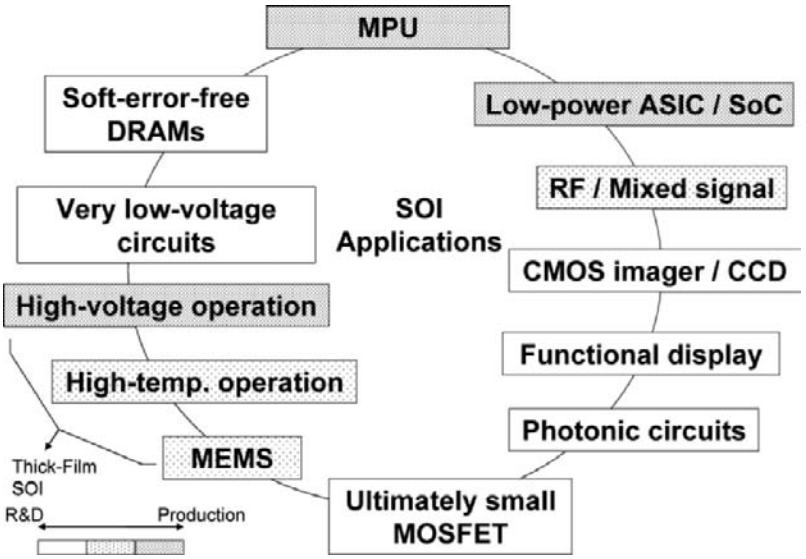

Fig. 1.12 Applications of SOI technology and their status.

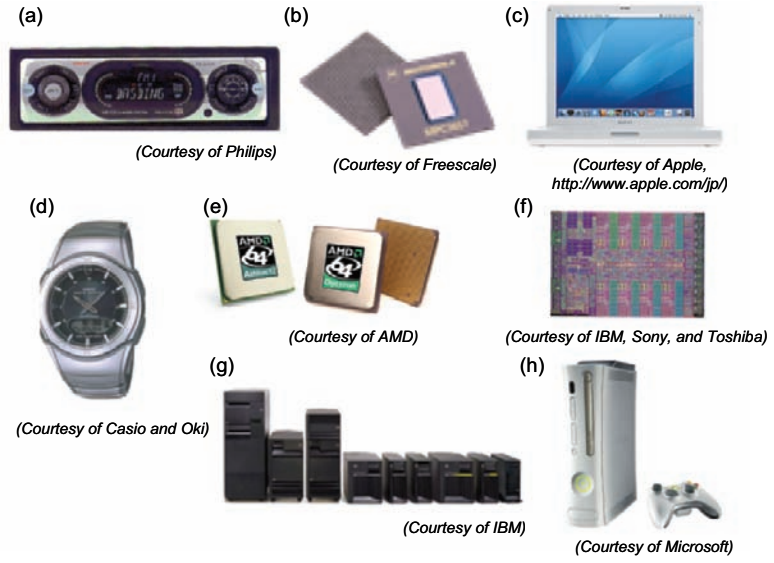

Fig. 1.13 Products made with SOI devices: (a) Audio power amplifiers and voltage regulators, (b) Power PC processors, (c) iBook G4 Laptop, (d) Low-power watch, (e) 64-bit MPUs, (f) CELL processor, (g) IBM eServer iSeries, and (h) Xbox360 video-game system.

1.5 Partially-Depleted (PD) and Fully-Depleted (FD) SOI MOSFETs, and Future MOSFETs

As mentioned before, fully-depleted (FD) SOI MOSFETs, which are the main theme of this book, have a number of advantages over partially-depleted ones. This section briefly reviews their structural features and electrical characteristics.

Figure 1.14 shows schematic cross sections of PD- and FD-SOI MOSFETs. The key feature of an FD-SOI MOSFET is that the depletion region reaches all the way to the bottom of the Si film. As a result, the body region is fully depleted, as the name of the device indicates. The advantage of this is that it markedly reduces floating-body effects.

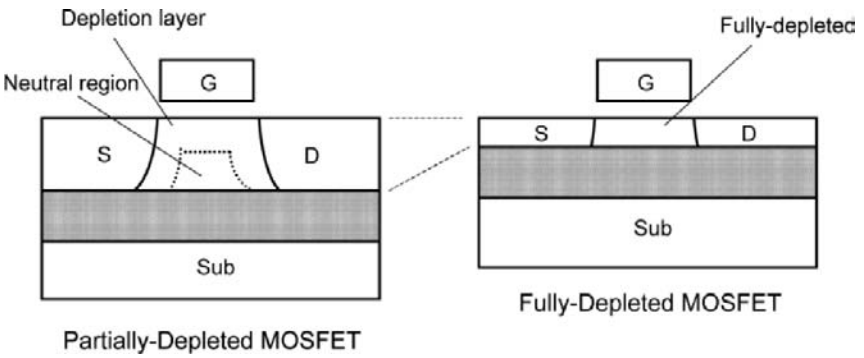

Fig. 1.14 Schematic cross sections of partially-depleted (PD) and fully-depleted (FD) SOI structures.

Figure 1.15 shows the equivalent circuit of an SOI MOSFET, a familiarity with which is necessary to understand what floating-body effects are. In the PD-SOI structure, the body potential varies with the number of holes that accumulate in the body and with the voltage of the electrodes. Both of these factors affect the electrical characteristics of the MOSFET by modifying the threshold voltage.

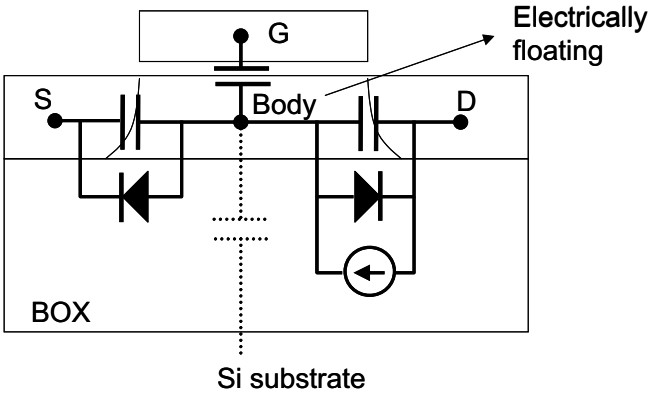

Fig. 1.15 Equivalent circuit of SOI MOSFET.

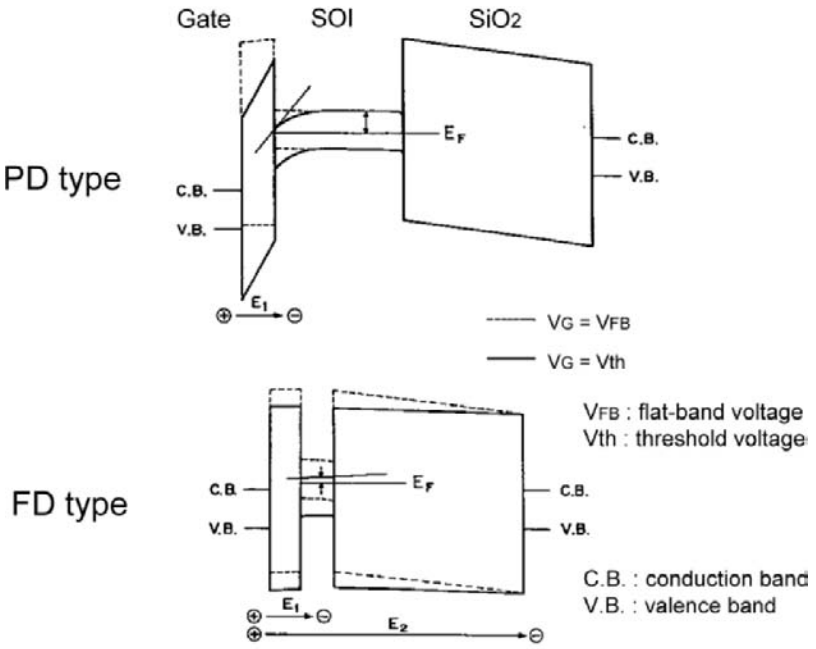

Fig. 1.16 Energy band diagrams for PD- and FD-SOI MOSFETs. E_F denotes the Fermi energy of the source.

Figure 1.16 compares energy band diagrams for PD- and FD-type SOI structures [1.11]. The potential barrier to holes between the body and the source is lower in the FD type. As a result, hardly any holes accumulate in the body (Fig. 1.17), which mitigates floating-body effects. In addition, the surface electric field is weak, which enhances carrier mobility. Since there is no punch-through current when the Si film is thin enough, the FD type can be scaled down to make the channel region shorter just by thinning the Si film. So, there is no need to dope the Si film; and one of the intrinsic properties of undoped Si is a high electron mobility. Moreover, since the gate potential provides good control of the channel potential, the subthreshold slope is steeper than in the PD-type, making low-voltage operation possible.

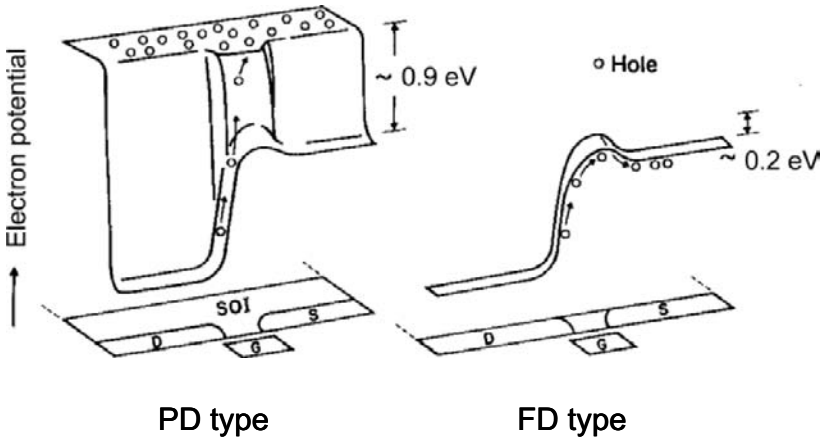

Fig. 1.17 Two-dimensional electron potential in PD- and FD-SOI MOSFETs.

Figure 1.18 shows the structural evolution of MOSFETs for the next couple of technology generations. Most of the devices are the FD type. The problems encountered when FD-SOI MOSFETs are scaled down is discussed in Chapter 8.

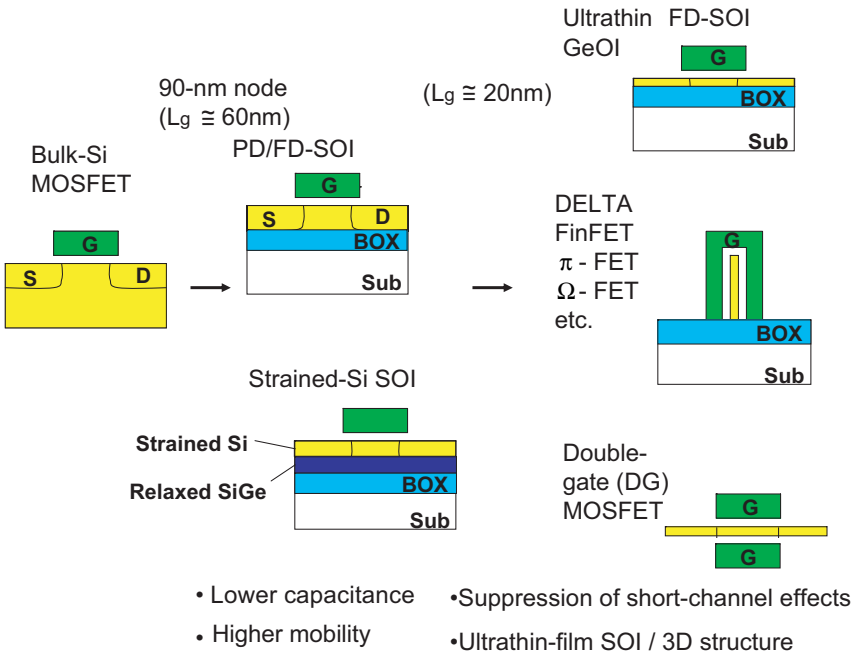

Fig. 1.18 Evolution of MOSFET structure.

1.6 Summary

After many years of research and development, SOI technology has finally become a reality. Applications range from MPUs and low-power LSIs to RF/mixed-signal and high-voltage circuits. The special features of FD-SOI MOSFETs suppress floating-body effects. Moreover, their high resistance to punch-through, high carrier mobility, steep subthreshold characteristics, and so on make it possible to fabricate high-performance scaled-down MOSFETs operating at a low voltage.

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Chapter 2

FD-SOI DEVICE AND PROCESS TECHNOLOGIES

2.1 Introduction

With silicon-on-insulator (SOI) technology, MOSFETs are formed in a thin top Si layer (SOI layer) separated from the Si substrate by an insulating film. This structural feature provides SOI devices with several advantages for high-speed, low-power operation. SOI devices are divided into two types, depending on the operating mode: fully-depleted (FD) and partially-depleted (PD). The difference mainly derives from the thickness of the SOI layer, with the layer generally being thinner for FD-SOI devices. In PD-SOI devices, there is an undepleted neutral region at the bottom of the SOI layer; but in FD-SOI devices, the entire body region is fully depleted. This provides FD-SOI devices with additional advantages, such as a low threshold voltage, a small leakage current, and smaller floating-body effects. Because of these features, FD-SOI devices exhibit better performance at low supply voltages; and lowering the supply voltage is one of the most effective ways to reduce power consumption. An understanding of the fundamental behavior of FD-SOI devices is essential for the design of FD-SOI circuits. This chapter first describes the basic features of SOI devices and the difference between the characteristics of FD- and PD-SOI MOSFETs. Next, as an aid to device design, a theoretical analysis of the DC characteristics of FD-SOI MOSFETs is presented. Finally, the process technology for FD-SOI CMOS devices is

explained; and problems with the technology that arise when the SOI layer is very thin are discussed, along with some solutions.

2.2 FD-SOI Devices

2.2.1 Basic Features of SOI Devices

SOI CMOS devices are formed in a thin top Si layer (SOI layer) separated from the substrate by an insulating film. An insulator is also used to completely isolate nMOSFETs and pMOSFETs from each other. As a result, a CMOS structure fabricated on an SOI substrate exhibits better characteristics in some respects than one built on a conventional bulk-Si substrate, such as a lower parasitic capacitance, no latch-up problems, a lower junction leakage current, and higher immunity to soft errors. The low parasitic capacitance, which is related to high-speed and low-power operation, is discussed below.

In order for signals to propagate inside an LSI, the MOSFETs have to charge and discharge a load capacitance consisting of the drain junction capacitance, gate capacitance, and interconnection capacitance. Among them, the drain junction capacitance is about one order of magnitude smaller in an SOI MOSFET than in a device made on a bulk-Si substrate.

As shown in Fig. 2.1, the drain junction capacitance of an SOI MOSFET can be broken down into the vertical junction capacitance (C_{JV}) between the drain and the substrate, and the lateral junction capacitance (C_{JL}) between the side wall of the drain and the body. C_{JV} can be further decomposed into the series connection of the capacitance (C_{JVB}) of the buried oxide (BOX, silicon oxide film with a permittivity 1/3 that of Si) and the capacitance (C_{JVD}) of the depletion layer that extends beneath the BOX. The thickness of the body region is typically no more than 0.1–0.2 μm in SOI substrates for CMOS circuits, and the area of the drain-body junction is very small. As a result, C_{JL} is small. When an SOI nMOSFET is fabricated on a p-type substrate, the drain layer is made n^+ type so that a potential difference remains, even when the drain voltage is zero, due to the difference between the Fermi levels of the drain layer and the substrate; and a depletion layer thus forms underneath the BOX. During circuit operation, even though the potential of the drain layer changes from zero to the supply voltage, a depletion layer forms underneath the BOX at either potential.

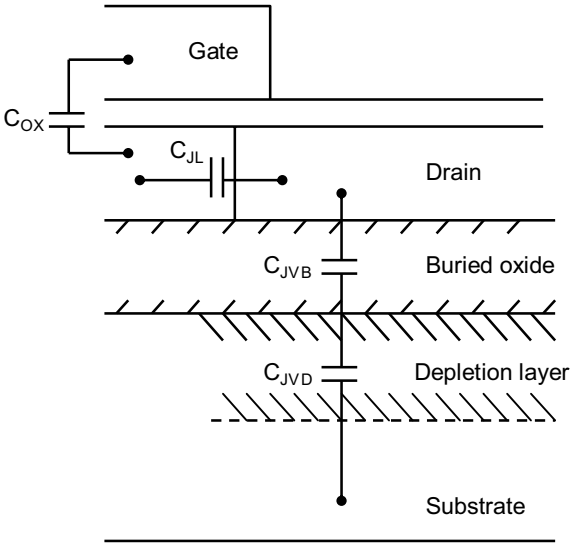


Fig. 2.1 Drain junction capacitance of SOI MOSFET. *(Reproduced by permission of Realize Advanced Technology Limited.)*

Figure 2.2 shows the results of calculations to determine how C_{JV}, C_{JL}, and C_J (= C_{JV} + C_{JL}) vary with substrate impurity concentration for a 90-nm-thick BOX. For comparison, it also shows C_J for a MOSFET formed on a bulk-Si substrate, calculated using the following assumptions: gate length (L) = 0.2 μm; gate width (W) = 10 μm; thickness of body layer = 50 nm; lateral dimensions of drain layer = 1 μm × 10 μm; and drain voltage = 2 V. The impurity concentration of the body region was also assumed to be 3×10^{17} cm^{-3}. The solid circle shows a measured value of C_J; it agrees well with the calculations. In an SOI structure, it is possible to use a low substrate impurity concentration on the order of 10^{14} cm^{-3}. That, coupled with the fact that the capacitance of the depletion layer underneath the BOX is small, provides a drain junction capacitance about 10 times smaller than that of a bulk-Si MOSFET. Furthermore, in an SOI device, the drain junction capacitance hardly varies at all with drain voltage; whereas in a bulk device, as the drain voltage (V_D) becomes smaller, the width of the depletion layer at the drain n^+-p junction decreases in proportion to $(V_{bi}+V_D)^{1/2}$, resulting in a larger junction capacitance (V_{bi} is the built-in potential). Accordingly, the more the LSI supply voltage is decreased in order to reduce power dissipation, the greater the benefits afforded by the smaller junction capacitance of SOI structures.

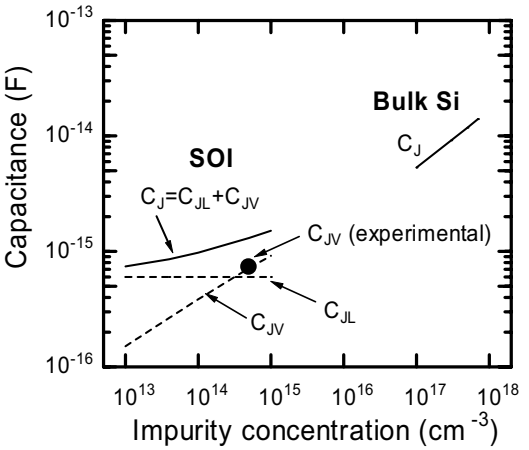


Fig. 2.2 Calculated dependences of drain-body capacitance (C_{JL}), drain-substrate capacitance (C_{JV}), and drain junction capacitance ($C_J = C_{JL} + C_{JV}$) on the impurity concentration of the substrate for FD-SOI and bulk-Si MOSFETs. (The calculations assumed $T_{BOX} = 90$ nm). *(Reproduced by permission of The Electrochemical Society, Inc.)*

For an SOI pMOSFET fabricated on a p-type substrate, the drain layer is p^+ type. So, the substrate side comes very close to the flat band condition when the drain voltage is zero. Consequently, no depletion layer forms underneath the BOX. However, a depletion layer starts to grow when a slight positive voltage is applied to the drain. During circuit operation, the drain layer of a pMOSFET changes from 0 V to the positive supply voltage; and a depletion layer usually forms underneath the BOX. Accordingly, the effect of the drain junction capacitance in pMOSFETs is similar to that in nMOSFETs.

So, one of the key characteristics of SOI CMOS structures is that they have a smaller junction capacitance than bulk-Si CMOS structures; and the difference becomes more pronounced as the supply voltage drops. We will now consider the extent to which the smaller junction capacitance affects overall LSI performance.

The power dissipation (P) and the signal propagation delay time (τ) of a CMOS LSI are given by the following formulae:

$$P = KC_{load}V_{DD}^2 f + I_{leak}V_{DD} + I_{SC}V_{DD} \tag{2.1}$$

$$\tau = C_{load}V_{DD} / I_{DSAT} = \frac{C_{load}V_{DD}}{\frac{W\mu\varepsilon}{LT_{OX}}(V_{DD} - V_{th})^2}. \tag{2.2}$$

In (2.1), the first term is the power dissipated by the charging and discharging of the load capacitance (C_{load}), where V_{DD} is the supply voltage, f is the operating frequency, and K is the activity factor of a gate. The second term is the power dissipation resulting from the leakage current (I_{leak}) in standby mode. The third term is the power associated with the short-circuit current (I_{sc}) flowing between the power-supply and ground lines. In (2.2), I_{DSAT} is the saturated drain current, T_{ox} is the thickness of the gate oxide film, μ is the carrier mobility, and ε is the permittivity of the gate oxide film. These formulae show that reducing the parasitic capacitance C_{load} is an effective way to lower the power dissipation and boost the speed. Since an SOI CMOS structure has a rather low drain junction capacitance, this technique is more effective in circuits where most of the total load capacitance is the junction capacitance, and the interconnection capacitance is only a small part.

Moreover, steep subthreshold characteristics can be obtained when using a fully-depleted MOSFET (described below); and it is possible to make the threshold voltage (V_{th}) lower than in either a partially-depleted or a bulk-Si device. As a result, since the term $(V_{DD}–V_{th})^2$ in (2.2) can be made larger, it is possible to achieve even higher speed and/or a lower power dissipation.

Figure 2.3 compares the performance of 48-bit multipliers fabricated as gate arrays with 40,000 gates using bulk-Si and SOI CMOSFET circuits with the same subthreshold leakage current (off current) [2.1]. In both cases, the gate oxide film was 5 nm thick. The SOI circuit is 24% faster than the bulk one at a supply voltage of 2 V, and the difference increases to 32% at 1.5 V and 46% at 1 V. This shows that SOI CMOS circuits operate faster than bulk-Si circuits at a given supply voltage, and that the supply voltage can be set lower for a given speed, thus enabling a significant reduction in power dissipation. It can also be seen that the speed difference between SOI and bulk-Si CMOS circuits becomes more pronounced as the supply voltage decreases.

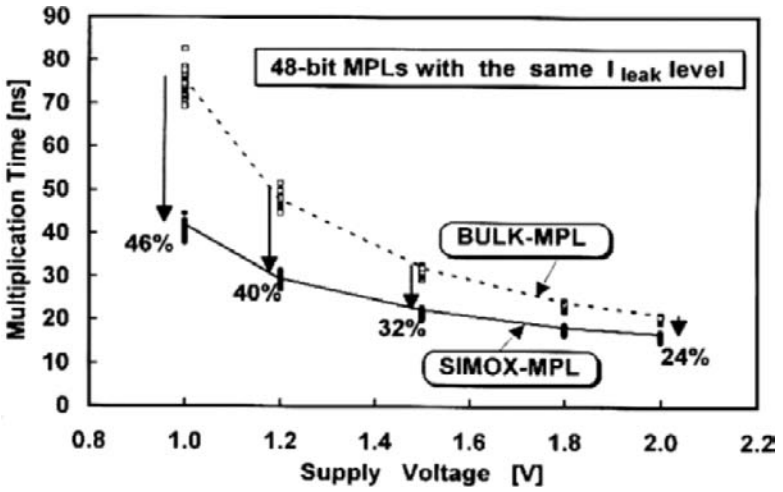


Fig. 2.3 Dependence of multiplication time on supply voltage for SOI (SIMOX) and bulk-Si CMOS multipliers. (From Y. Kado et al. [2.1]. ©1995 IEEE.)

2.2.2 Operating Modes of SOI MOSFETs

SOI MOSFETs have two modes of operation: fully-depleted (FD) and partially-depleted (PD). The difference between them is described below with reference to Fig. 2.4, taking an nMOSFET as an example. In the figure, (a) shows the cross-sectional structure of an FD-SOI MOSFET; (b) is an energy band diagram along the line A–A′ in (a), which runs through the source, body, and drain near the bottom of the body region; and (c) is an energy band diagram showing how the energy bands change along the line B–B′ in (a), which runs from the gate oxide film down into the body region near the source end. The corresponding figures for a PD-SOI MOSFET are shown in Fig. 2.4(d-f). In an FD-SOI device, the entire body region is depleted in both the "on" and "off " states, as shown in Fig. 2.4(a). This results from the fact that an FD-SOI device generally has a thinner body region than a PD-SOI device. For example, the body region is about 100–200 nm thick in a PD-SOI device, but at most about 50 nm thick in an FD-SOI device.

In contrast to an FD-SOI device, a PD-SOI device has an undepleted neutral region at the bottom of the body region, as shown in (d). This difference results in a different potential distribution inside the body region. In an FD-SOI device, the entire body region has a potential gradient in the depth direction, as shown in (c); and the gate field extends right into the BOX. In a PD-SOI device, the influence of the gate field stops inside the body region, as shown in (f); and there is a neutral region with no potential gradient at the bottom of the body region. Accordingly, the potential difference between the top and bottom of the body region is larger in a PD-SOI device; and the potential barrier to holes between the source and body near the bottom of the body region is higher.

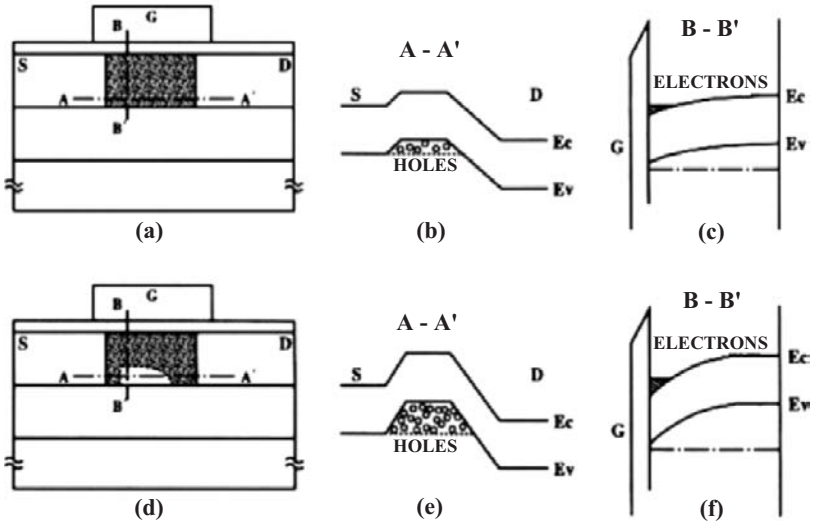


Fig. 2.4 FD- and PD-SOI MOSFETs. (a) Cross section of an FD-SOI device, (b) the energy band diagram along the line A-A′, and (c) the energy band diagram along the line B-B′. (d-f) show the corresponding figures for a PD-SOI device. *(Reproduced by permission of Realize Advanced Technology Limited.)*

This difference in the barrier height for holes leads to a difference in the number of holes that accumulate in the body region. Holes are generated by impact ionization near the drain. During the operation of an nMOSFET, when channel electrons pass through the high-electrical-field region near the drain, they gain energy from the field and jump to higher energy levels. The

high-energy electrons collide with valence electrons and generate more electrons and holes (impact ionization). The electrons flow into the drain, and the holes flow toward the source via the bottom of the body region. When this happens, more holes accumulate at the bottom of the body region in a PD-SOI than in an FD-SOI device because a PD-SOI device has a higher potential barrier. This leads to a large difference between the floating-body effects (described below) of the two types of devices, such as the kink in the drain current-voltage characteristics and the stability of the dynamic characteristics.

As a way of presenting an overview of the structural parameters used to design FD-SOI MOSFETs, Fig. 2.5 shows the results of simple calculations to determine the proper relationship among the impurity concentration (N_A), the maximum thickness (T_B) of the body region, and the threshold voltage (V_{th}). T_B and V_{th} are given by

$$T_B = \sqrt{2K_{Si}\varepsilon_0(2\phi_F)/qN_A} \tag{2.3}$$

$$V_{th} = V_{FB} + 2\phi_F + \frac{qN_A T_B}{C_{OX}}, \tag{2.4}$$

where

$$\phi_F = (kT/q)\ln(N_A/n_i), \tag{2.5}$$

K_{Si} is the relative permittivity of silicon, ε_0 is the permittivity of a vacuum, q is the charge on an electron, V_{FB} is the flat band voltage, C_{OX} is the capacitance of the gate oxide film, k is Boltzmann's constant, T is the absolute temperature, and n_i is the intrinsic impurity concentration. T_B is taken to be the width of the channel depletion layer when a threshold voltage is applied (with a surface potential of $2\phi_F$). To make an FD-SOI device, the channel depletion layer must just reach the BOX, thus depleting the entire body region, which means that the thickness of the body region must be no larger than T_B. That is, T_B is the maximum thickness. More precisely, in an FD-SOI MOSFET the body region must remain fully depleted over the range of gate voltages from 0 V up to the threshold voltage. Accordingly, since the body must befully depleted at a surface potential of approximately ϕ_F and not $2\phi_F$, T_B in the figure should be thought of as a rough estimate of the maximum allowable thickness of the body region of an FD-SOI MOSFET.

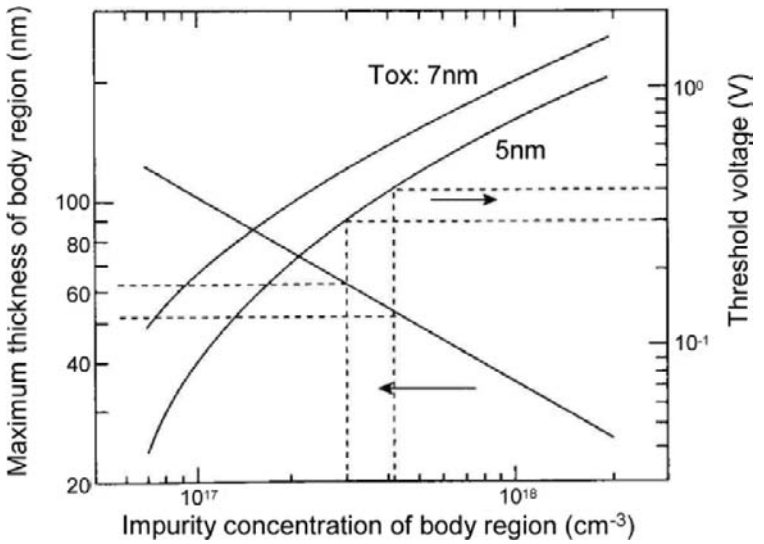


Fig. 2.5 Dependence of the maximum thickness of the body region on the impurity concentration of the body region needed to make an FD-SOI MOSFET. *(Reproduced by permission of The Electrochemical Society, Inc.)*

The threshold voltage actually depends on the drain voltage, that is, it decreases with drain voltage due to parasitic bipolar effects in FD-SOI devices, as described below. The threshold voltages in the figure are thus the values at low drain voltages.

Under these assumptions, the figure shows that, to obtain an FD-SOI MOSFET with a 5-nm-thick gate oxide film and a threshold voltage of 0.3–0.4 V, for example, the thickness of the body region must be at most 50–60 nm.

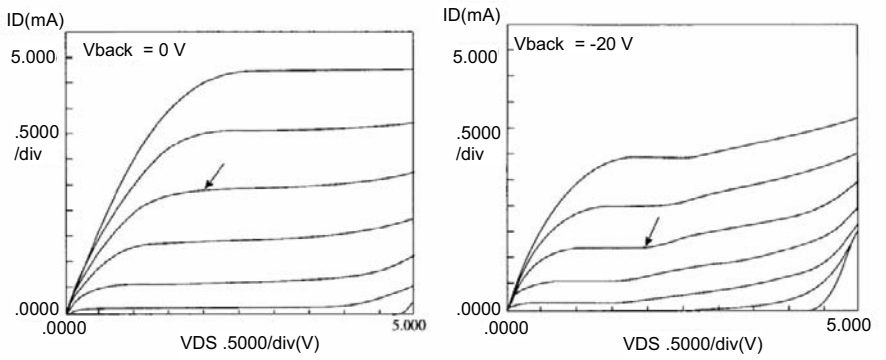
PD-SOI devices exhibit none of the advantages of FD-SOI MOSFETs described below (kink-free drain current-voltage characteristics, steep subthreshold characteristics, stability with regard to dynamic floating-body effects, etc.); and their characteristics are basically the same as those of bulk-Si MOSFETs. However, they do have the advantages of SOI structures mentioned in section 1.3 (low parasitic capacitance, excellent latch-up immunity, low junction leakage current, high immunity to soft errors). To obtain a low junction capacitance, which is an important reason for using SOI

technology, the source and drain layers must either extend all the way down to the BOX or come very close to doing so. However, unlike in FD-SOI devices, the channel depletion layer must not be allowed to reach the BOX. So, the body region of a PD-SOI device must be at least 100 nm thick.

2.2.3 Basic Characteristics of FD- and PD-SOI MOSFETs

A. Kink in drain current-voltage characteristics

Figure 2.6 shows the drain current-voltage characteristics of FD- and PD-SOI nMOSFETs [2.2]. PD-SOI devices exhibit what is called a "kink", which is a sharp rise in drain current as the drain voltage increases at a fixed gate voltage. As mentioned in Section 2.2.2, electrons flowing in the channel are accelerated and jump to higher energies in the high-electrical-field region near the drain, thereby generating large numbers of electrons and holes by impact ionization. The electrons flow towards the drain, and the holes flow towards the source along the bottom of the body region. Since there is a potential barrier to holes at the source end, the holes begin to accumulate in the body region. As more and more accumulate, the body potential increases and the barrier height decreases, which allows more holes to flow out to the source across the barrier. Consequently, the number of holes that can accumulate in the body region is such that the number flowing out to the source balances the number generated by impact ionization.



(a) (b)

Fig. 2.6 Drain current-voltage characteristics of (a) FD-SOI and (b) PD-SOI nMOSFETs. (From J. P. Colinge [2.2]. ©1988 IEEE.)

Since a PD-SOI device has a higher potential barrier to holes than an FD-SOI device does, it allows more holes accumulate in the body region. When a large number of holes accumulate there, the potential of the body region rises to a positive value; and this bias effect causes the threshold voltage of a MOSFET to drop, thereby increasing the drain current. As a result, as shown in Fig. 2.6, acute impact ionization takes place as the drain voltage increases, causing a kink to appear in the drain current-voltage characteristics. Thus, the kink effect in PD-SOI MOSFETs originates from the change in the body potential.

To examine these changes in more detail, we look first at the process governing the body potential of PD-SOI MOSFETs under steady-state conditions, which is described by the model proposed by Tihanyi, et al. [2.3] and is shown in Fig. 2.7(a). Here, I_{ch} is the channel current, I_D is the drain current, I_{Dn} is the electron current at the drain, and M is the avalanche multiplication factor of impact ionization ($I_{Dn} = M \cdot I_{ch} = I_D$). In addition, I_H is the hole current generated by impact ionization, I_{HS} is the hole current at the source, I_{HSu} is the substrate (the undepleted neutral body region) current, and I_{HL} is the reverse leakage current at the drain junction. Figure 2.7(b) shows the forward current-voltage (I_{SSu} vs. U_{SSu}) characteristics of the p-n junction between the source and the neutral body region; and Fig. 2.7(c) shows how I_{HSu} varies with drain voltage (U_D).

When $U_D < U_{D1}$, no impact ionization takes place; and I_{HSu} is equal to the drain junction leakage current, I_{HL} . Under these conditions, the potential of the neutral body region is such that the forward current (I_{SSu}) flowing across the junction between the source and the neutral body region equals the reverse leakage current (I_{HL}) at the drain junction, resulting in potential U_1, as shown in (b). But when $U_D > U_{D1}$, the resulting impact ionization causes the substrate current to increase. In this case, the potential of the neutral body region is such that, for example, I_{SSu} equals IHSu at a drain voltage of U_{D2}, as shown in (c). So, the potential of the neutral body region changes to U_2, as shown in (b). In other words, the potential of the neutral body region is zero when U_D is zero and is fixed at U_1 over the range $0 < U_D < U_{D1}$, in which no impact ionization takes place; but it increases with U_D when impact ionization occurs at $U_D > U_{D1}$.

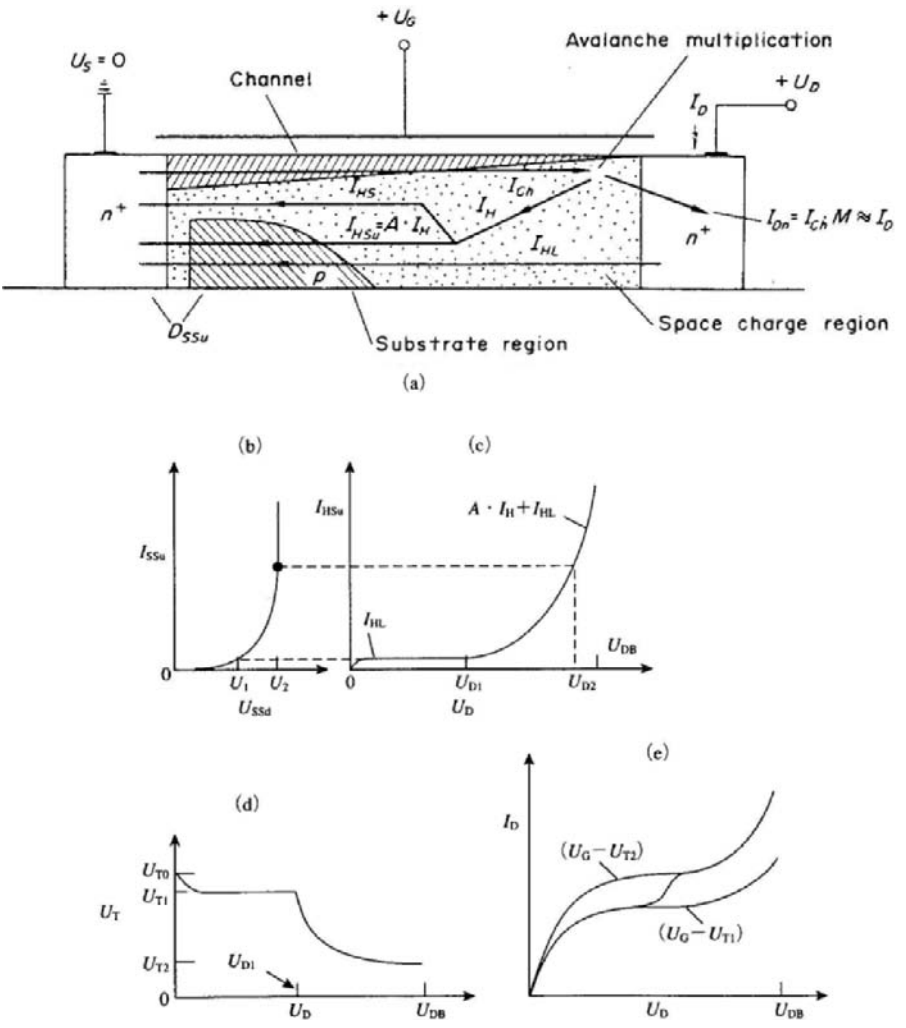


Fig. 2.7 (a) Cross section and current distribution of a PD-nMOSFET. Schematic characteristics of (b) source-substrate diode I_{SSu} (V_{SSu}); (c) substrate current I_{HSu} (V_D); (d) threshold voltage; and (e) bend in drain current I_D (V_D). *(Reprinted Solid-State Electronics, Vol. 16, T. Tihanyi et al., pp. 309-314, Copyright (1975), with permission from Elsevier.)*

However, as the potential of the neutral body region increases, I_{SSu} increases sharply; so the potential tends to level off. This increase in the potential causes what is called a substrate bias effect that lowers the threshold voltage of a MOSFET, as illustrated in Fig. 2.7(d). When U_D is zero, the potential of the neutral body region is also zero; and the device has a threshold voltage of U_{T0}. The potential of the neutral body region is grater than zero when U_D is greater than zero; but it remains fixed at U_I over the range $0 < U_D < U_{D1}$, in which there is no impact ionization. So, the threshold voltage decreases slightly and then remains constant at U_{T1}. When $U_D > U_{D1}$, impact ionization occurs; and the potential of the neutral body region increases beyond U_I. As a result, the threshold voltage falls below U_{T1} to U_{T2}.

Thus, as shown in Fig. 2.7(e), in the range of drain voltages for which impact ionization does not occur, a key feature of the drain current-voltage characteristics is that the threshold voltage of a MOSFET is U_{T1}; but when impact ionization occurs, the threshold voltage falls to U_{T2} and the characteristics jump to a different type with that threshold voltage. This results in the kink effect in PD-SOI MOSFETs because they have a floating-body region.

To suppress the kink, the body potential has to be fixed by providing a body terminal that extracts holes from the body region. Various methods of fabricating a body terminal have been proposed [2.4]; but they all increase the device area, which imposes further constraints on layout design. So, this is a remedial measure that should only be taken when absolutely necessary.

One feature of FD-SOI devices is that they do not exhibit this sort of kink. In an FD-SOI device, the potential barrier to holes at the source end is small, even deep within the body region, because the body region is depleted all the way down to the bottom. As a result, there is little accumulation of holes in this region; so a kink cannot appear. Since there is no need to resort to a body terminal to eliminate kink, FD-SOI devices have the advantage of being smaller than PD-SOI devices with a body terminal, and can thus be integrated into LSIs at higher densities. They make it easier to design layout patterns, and they make it possible to draw upon existing resources for circuit design and layout design that have previously been developed for devices fabricated on a bulk-Si substrate.

B. Steep subthreshold slope in FD-MOSFETs

An important feature of FD-SOI MOSFETs is their steep subthreshold characteristics [2.5]. The subthreshold swing of an FD-SOI device is close to 60 mV/dec at room temperature, which is the limiting value for MOSFETs. The subthreshold characteristics are the drain current vs. gate voltage (I_D vs. V_G) characteristics at gate voltages below the threshold voltage. In this region, the drain current increases exponentially with gate voltage because it is proportional to the number of carriers with enough thermal energy to cross the potential barrier between the source and channel, as shown in the formula

$$I_D = \beta \exp(-\frac{q\phi_B}{kT}), \tag{2.6}$$

where β is a constant of proportionality and ϕ_B is the barrier potential. ϕ_B can be written in terms of the built-in potential (V_{bi}) of the source-channel p-n junction and the channel surface potential (ϕ_S) as follows:

$$\phi_B = V_{bi} - \phi_S . \tag{2.7}$$

As the gradient of $\log(I_D)$ vs. V_G in the subthreshold region becomes steeper, the drain leakage current (off current) at $V_G = 0$ becomes smaller. In addition, for a given off current, a steeper gradient allows the threshold voltage to be made smaller. Producing high-speed LSIs with a low power dissipation requires the use of MOSFETs with a low threshold voltage and a small off current, which in turn requires a steep gradient. The gradient is expressed as the subthreshold swing, S, which is defined to be the change in gate voltage needed to change the drain current by one decade in the subthreshold region, as shown by the following formula. (S is given in units of mV/dec.)

$$S = 1/(\partial \log(I_D)/\partial V_G) \tag{2.8}$$

$$= \frac{kT}{q} \ln(10) / \frac{\partial \phi_S}{\partial V_G} . \tag{2.9}$$

According to (2.9), S becomes smaller as the rate at which the channel surface potential changes with gate voltage becomes larger, resulting in steeper subthreshold characteristics.

Figure 2.8 shows typical subthreshold characteristics of FD-SOI and bulk-Si MOSFETs (and PD-SOI MOSFETs). As mentioned at the outset, FD-SOI devices have steeper subthreshold characteristics than bulk or PD-SOI devices, with S being close to the limiting value. To put it another way, for a given change in gate voltage, the channel surface potential changes more in an FD-SOI device than in bulk or PD-SOI devices. The reason for this is explained below.

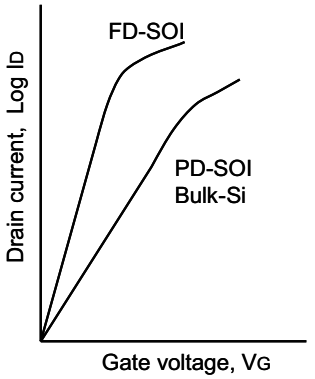


Fig. 2.8 Subthreshold characteristics of FD-SOI, PD-SOI, and bulk-Si MOSFETs.

Figures 2.9(a) and (b) show the cross-sectional structures of bulk-Si and FD-SOI MOSFETs, together with equivalent circuits of the capacitance between the gate and substrate. The gate-substrate capacitance of the bulk structure is comprised of the series connection of the gate-oxide capacitance (C_{ox}) and the channel-depletion-layer capacitance (C_D). In the FD-SOI structure, since the body region is fully depleted, the gate-substrate capacitance is comprised of the series connection of C_{ox} and the body-depletion-layer capacitance (C_B) together with the capacitance (C_{BOX}) of the buried-oxide film, which has one-third the relative permittivity of silicon. For the sake of simplicity, we disregard the capacitance of the depletion layer underneath the BOX. Based on these equivalent circuits, the relationship between the channel surface potential (ϕ_{SBS} for a bulk-Si and ϕ_{SFD} for an FD-SOI MOSFET) and the gate voltage is given by

$$\phi_{SBS} = \frac{C_{OX}}{C_{OX} + C_D} V_G , \tag{2.10}$$

$$\phi_{SFD} = \frac{C_{OX}}{C_{OX} + C_{SOI}} V_G , \tag{2.11}$$

where

$$C_{SOI} = \frac{C_B}{1 + C_B / C_{BOX}} . \tag{2.12}$$

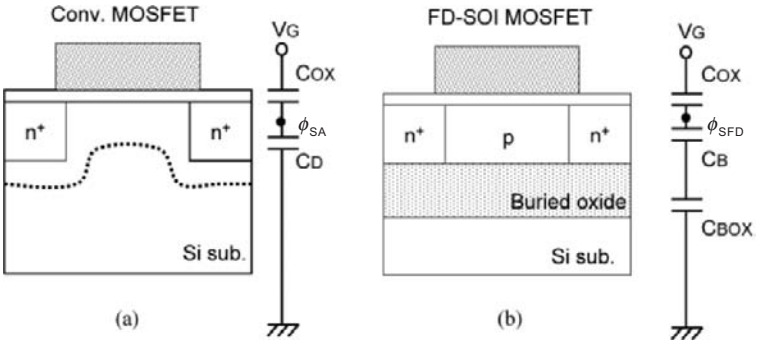


Fig. 2.9 Cross sections and gate-substrate capacitances of (a) a bulk-Si MOSFET and (b) an FD-SOI MOSFET. *(Reproduced by permission of Realize Advanced Technology Limited.)*

If we assume, for instance, that the impurity concentration of the channel region of a bulk-Si MOSFET is 1×10^{17} cm^{-3} and that an FD-SOI MOSFET has a 50-nm-thick SOI layer and a 100-nm-thick BOX, then $C_D = 1\times10^{-7}$ F/cm^2 and $C_{SOI} = 3\times10^{-8}$ F/cm^2. Incidentally, for a gate-oxide thickness of 5 nm, (2.10) and (2.11) yield $\phi_{SBS} = 0.87\cdot V_G$ and $\phi_{SFD} = 0.96\cdot V_G$, which shows that the change in channel surface potential with gate voltage is greater for an FD-SOI device. A PD-SOI device behaves in the same way as a bulk-Si MOSFET because the channel depletion layer does not reach the BOX.

Thus, since the body region of an FD-SOI device is fully depleted, it is connected in series to the small capacitance of the BOX, thereby providing both better control of the channel surface potential by means of the gate voltage and also steep subthreshold characteristics.

C. Dynamic floating-body effects

Since an SOI device is fully isolated, the body potential is not fixed and changes for a variety of reasons. The effects brought about by these changes are referred to collectively as floating-body effects. In particular, dynamic floating-body effects that occur when a device is operating in a circuit can give rise to complex behavior. The main causes of changes in body potential are impact ionization and majority carrier redistribution in the body region, which occur as the gate and drain switch between high and low levels [2.6]. This section reviews these phenomena, and shows that FD-SOI devices are more stable than PD-SOI devices with respect to floating-body effects.

(1) Effect of impact ionization

For the nMOSFET in Fig. 2.10, some of the holes generated by impact ionization in the high-electric-field region near the drain accumulate in the body region and raise the body potential to a positive value. Since the number of accumulated holes depends on the time constants of hole creation and annihilation, the device exhibits complex behavior when operating dynamically in an LSI.

Figures 2.11(a) and (b) show drain current waveforms for PD- and FD-SOI devices, respectively, when a single pulse is applied to the drain, followed by a single pulse to the gate after a time delay of t_d (as illustrated in Fig. 2.11(c)), with the height of the drain pulse as a parameter [2.7]. The characteristics of a PD-SOI device were simulated by applying a negative voltage to the back of the substrate of an FD-SOI device in order to form an accumulation layer at the bottom of the body region. The height of the drain pulse varied from 0.2 V to 2 V. The drain pulse had a rise time (t_{rD}) of 100 ns; and the gate pulse had a height of 1 V and a rise time (t_{rG}) of 50 ns. As shown in (a), the drain current of the PD-SOI device exhibits transient characteristics immediately after the rising edge of the gate pulse when the drain voltage is 1.5 V or more; and the drain current saturates in a shorter time as the drain voltage increases.

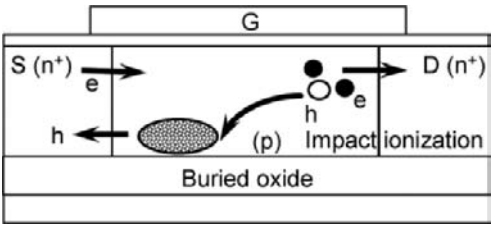


Fig. 2.10 Floating-body effects due to impact ionization.

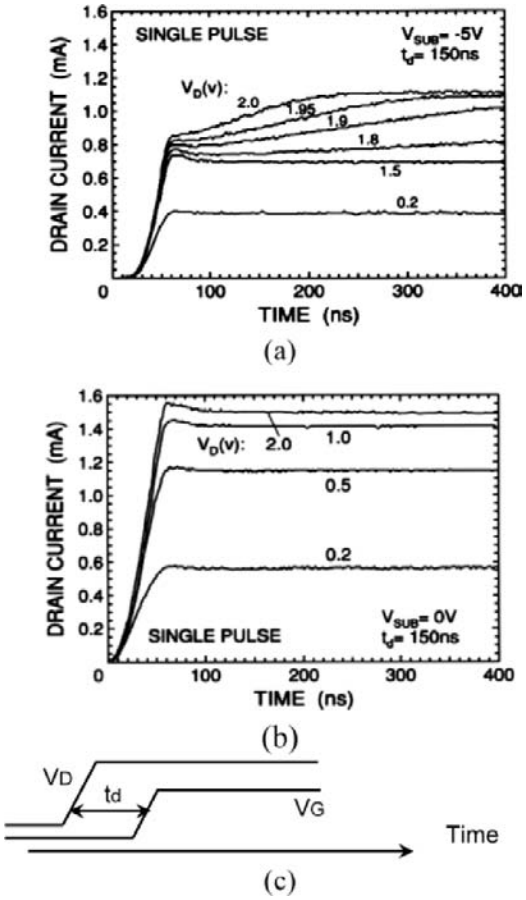


Fig. 2.11 Dynamic floating-body effects due to impact ionization in (a) PD-SOI and (b) FD-SOI nMOSFETs for the input gate and drain pulses in (c). *(Reproduced by permission of Realize Advanced Technology Limited.)*

At drain voltages of 1.5 V and above, impact ionization generates a significant number of holes; and the number becomes larger at higher drain voltages. Accordingly, as the drain voltage increases, the holes pile up faster in the body region and the threshold voltage drops at a faster rate, causing the increase in drain current to take place sooner. In this way, differences in the number of holes generated during the operation of a PD-SOI device give rise to differences in the rate at which holes accumulate in the body region, which

appear as differences in the transient characteristics. On the other hand, no such transient characteristics are observed in FD-SOI devices, as shown in (b). Thus, at voltages for which impact ionization occurs, a PD-SOI MOSFET will exhibit complex behavior that depends on the pulse conditions, while an FD-SOI MOSFET will function stably. This difference arises because the entire body region of an FD-SOI device is depleted, which makes the potential barrier to holes between the source and body region smaller than in a PD-SOI device, thereby allowing fewer holes to accumulate in the body region.

As described above, a PD-SOI device exhibits pronounced dynamic floating-body effects associated with impact ionization. To suppress these effects, the device must be provided with an extra terminal to fix the body potential by extracting holes. In contrast, an FD-SOI device can be said to be stabilized against dynamic floating-body effects, and thus has no need of a body terminal.

(2) Effects of majority carrier redistribution

Figure 2.12 roughly illustrates phenomena associated with majority carrier redistribution in a PD-SOI nMOSFET. When the gate voltage changes from the low to the high level, the channel depletion layer grows wider, driving away the holes (majority carriers) that it encounters along the way. The holes accumulate at the bottom of the body region and raise the body potential to a positive value. Since the source junction is forward-biased, the holes then flow out towards the source. Next, when the gate returns to the low level, holes are needed to make the channel depletion layer narrower so that a neutral region can form. But since the holes have already flowed out, there is a shortage, which creates a negative body potential that causes holes to be supplied from the source as a reverse-biased junction current. In this way, the body potential varies due to the surplus or shortage of holes in the body region arising from the outflow and supply of holes at the source junction and the expulsion and restoration of holes due to the growth and contraction of the channel depletion layer. In addition, since similar phenomena are associated with the growth and contraction of the drain depletion layer as the drain changes between high and low levels, the body potential of devices operating in an LSI exhibits complex behavior. The phenomena associated with majority carrier redistribution only cause problems in PD-SOI MOSFETs; while in principle, they do not even occur in FD-SOI devices because the entire body region is always depleted.

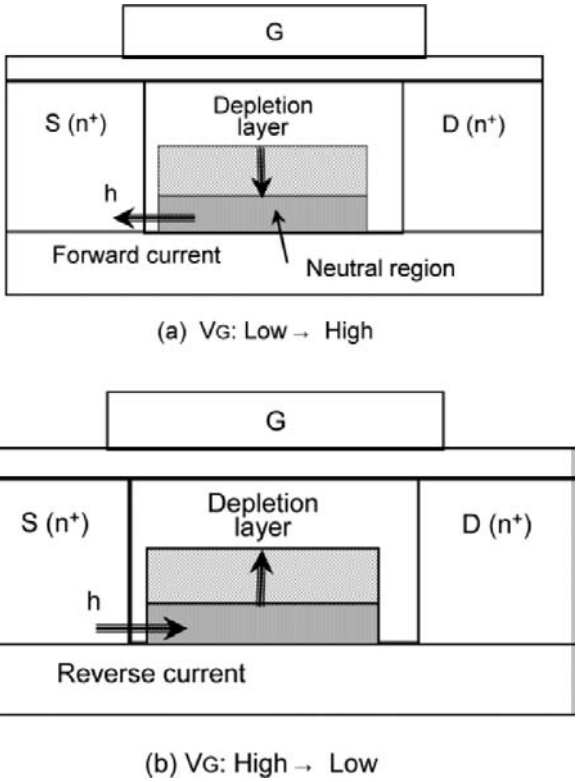


Fig. 2.12 Dynamic floating-body effects due to majority carrier redistribution in PD-SOI MOSFETs (a) when VG switches from a low to a high level and (b) when VG switches from a high to a low level. *(Reproduced by permission of Realize Advanced Technology Limited.)*

Figure 2.13 shows some simulation results on the change in the floating-body potential during switching events in a PD-SOI nMOSFET operating as an inverter [2.8]. When the gate (inverter input) changes from the low to the high level, the channel depletion layer grows and drives away the holes that have accumulated at the bottom of the body region. Consequently, the body potential rises to a positive value during the first 50 ps or so. But once the gate has switched to the high level, the drain (inverter output) changes from the high to the low level, and the holes that are needed to make the drain depletion layer shrink and to form a neutral region are obtained from the accumulated holes, which causes the body potential to drop. After that, the flow of holes out to the source (or the recombination of holes) causes the number of holes in

the body region to decrease starting at about 10^{-3} s (with a certain time constant); and so the body potential drops toward the steady-state value.

On the other hand, when the input changes from high to low, not enough holes are available to make the channel depletion layer shrink and the width of the depletion layer return to the steady-state value. So, the body potential drops to a negative value for the first 100 ps or so. But when this happens, the drain (inverter output) changes from low to high, causing the drain depletion layer to grow and drive holes away. Thus, the body potential increases at around 50 ps. After that, the influx (or creation) of holes due to the reverse-biased currents flowing through the source and drain junctions causes the body potential to rise toward the steady-state value after about 10^{-1} s.

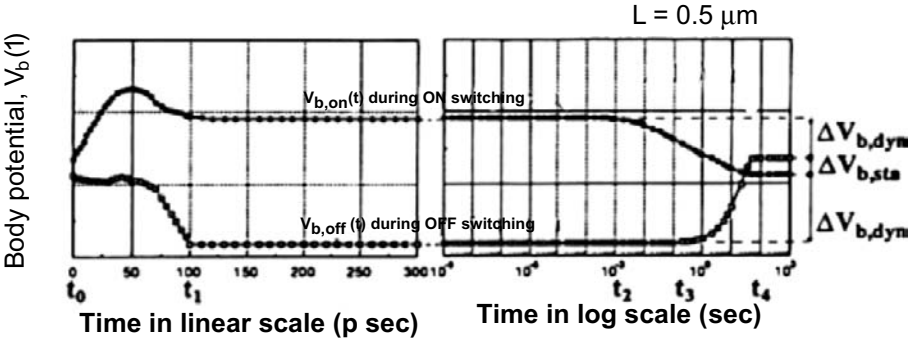


Fig. 2.13 Change in floating-body potential during switching events in a PD-SOI nMOSFET operating as an inverter. *(Reproduced by permission of The Electrochemical Society, Inc.)*

These floating-body effects have been reported to cause transient phenomena in the access transistors of DRAMs and SRAMs that can lead to a loss of charge in memory cells [2.9], and are also associated with similar problems in the pass transistors of logic circuits [2.10].

However, there have also been reports that a quantitative understanding of floating-body effects enables us to exploit them [2.11]–[2.13]. One application is a microprocessor made with PD-SOI devices that exhibits a performance 20–35% better than that obtainable with bulk-Si devices. This improvement was achieved by exploiting floating-body effects and a reduced junction capacitance in combination with back-gate effects. In the sense amplifier and other circuits for which timing is critical, the devices have a body terminal to

fix the body potential; but the other circuits use PD-SOI devices with a floating body.

D. Parasitic bipolar effects in FD-SOI MOSFETs

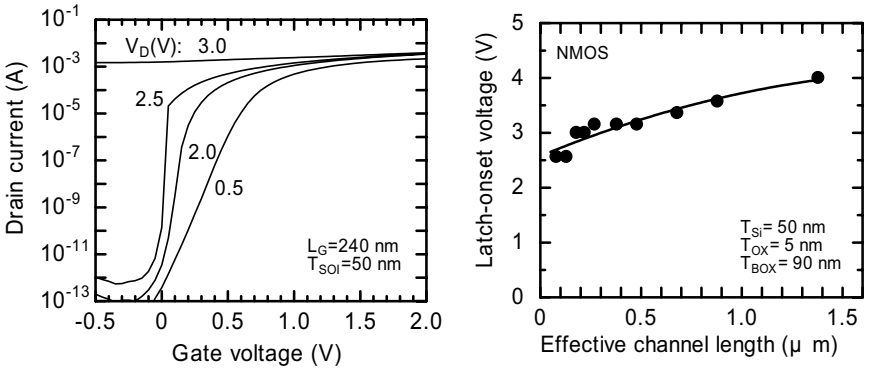
A major part of the appeal of FD-SOI MOSFETs is that they suppress the kink in the drain current-voltage characteristics without using a body terminal. But although a kink does not appear, the devices are still susceptible to a kind of floating-body effect known as parasitic bipolar effects. These effects occur when the source, body, and drain of MOSFETs act as the emitter, base, and collector of parasitic transistors in which the base current consists of majority carriers produced by impact ionization [2.14]. Since the body region is more depleted in FD- than in PD-SOI devices, the injection efficiency of the emitter of the parasitic bipolar transistors is higher, which makes these effects more likely to occur. When they do occur, they have a number of consequences, such as a reduction in the breakdown voltage between the source and drain, abnormally steep subthreshold characteristics beyond the theoretical limit, a larger off current, and a smaller threshold voltage.

Figure 2.14(a) illustrates a phenomenon resulting from parasitic bipolar effects called single-transistor latch because it causes latch-up in a single MOSFET device [2.15]. At a drain voltage of 2.5 V, the subthreshold characteristics are abnormally steep; and at 3 V, the gate can no longer prevent a large current from flowing through the device. When this happens, the device is said to be latched. This phenomenon causes problems, such as the malfunctioning of an LSI and a reduced drain breakdown voltage. Moreover, as the figure shows, parasitic bipolar effects can increase the off current and lower the threshold voltage, even without leading to latch-up.

Figure 2.14(b) shows how the effective channel length affects the drain voltage at which single-transistor latch occurs (the latch onset voltage) due to parasitic bipolar effects [2.7]. It can be seen that the effective channel length is of little consequence, which means that there is nothing that can be done to make FD-SOI MOSFETs work at a supply voltage of 5 V or 3.3 V. Conversely, FD-SOI devices are well-suited to LSI applications that use a low supply voltage of about 1 V or less, where parasitic bipolar effects do not occur and the full potential of the devices can be realized.

Suppressing parasitic bipolar effects in FD-SOI devices entails: (i) suppressing the generation of majority carriers by impact ionization, (ii) reducing the injection efficiency of the emitter of parasitic bipolar transistors,

and (iii) lowering the transport efficiency with which minority carriers injected into the base are conveyed to the collector. Techniques that are reported to be effective include introducing electron-hole recombination centers near the source by Ar ion implantation [2.16], and using SiGe for the source region to reduce the potential barrier to holes between the source and body [2.17]. In both techniques, holes (for an nMOSFET) are extracted from the body region to prevent the potential there from becoming positive and to reduce the emitter injection efficiency.



(a) (b)

Fig. 2.14 (a) Single-transistor latch due to parasitic bipolar effects. (b) Dependence of latch-onset voltage on effective channel length. *(Reproduced by permission of The Electrochemical Society, Inc.)*

E. Self-heating effects

We have seen the beneficial effects that the buried insulating film underneath an SOI MOSFET has on the electrical characteristics. However, the thermal properties must also be considered. The thermal conductivity of the silicon oxide film typically used for the buried insulator is 1.4 $Wm^{-1}K^{-1}$, which is two orders of magnitude smaller than that of Si (140 $Wm^{-1}K^{-1}$). As a result, the Joule heat generated by the drain current cannot easily escape through the BOX and the substrate. This gives rise to self-heating, which raises the channel temperature [2.18].

A large amount of Joule heat is generated in the saturation region, where the drain voltage and current are both large; and the resulting increase in temperature reduces the drain current by lowering the carrier mobility, and

may lead to the appearance of a differential negative resistance in the drain current-voltage characteristics. Accordingly, different drain current-voltage characteristics may be obtained when measuring the steady-state drain current with a DC supply, and when measuring the drain current with a pulse supply, which causes less heating and is thus less likely to induce self-heating, even under the same drain and gate bias conditions.

The Joule heat generated in the channel is dissipated by the interconnections via the contacts on the source and drain layer, and via the gate oxide film and gate electrode. Consequently, considering the ease with which Joule heat is dissipated, the increase in channel temperature caused by self-heating is governed by the structural parameters of the device, such as the thickness of the SOI layer, the distance between the channel and the source/drain contacts, and the thickness of the BOX [2.19].

As an example, Fig. 2.15 shows some experiment results on how the thickness of the SOI layer affects the channel temperature vs. device power characteristics. The results for a bulk-Si MOSFET are also shown for comparison. The figure shows that the channel temperature increases both in proportion to the device power and also as the SOI layer becomes thinner.

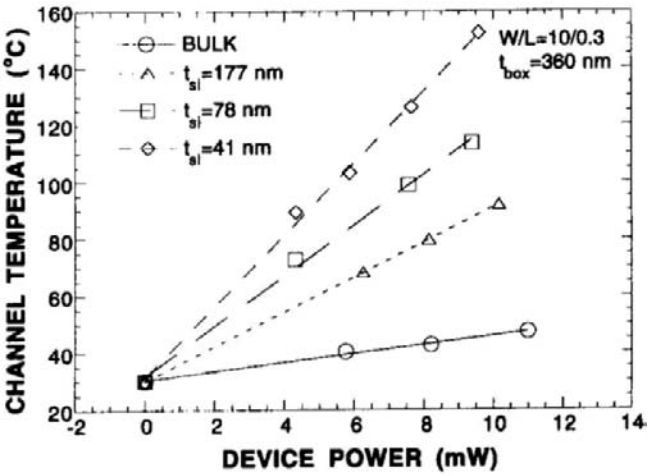


Fig. 2.15 Channel temperature versus power for SOI devices, with the thickness of the SOI layer as a parameter, and for a bulk device for comparison. (From L. Su et al. [2.19]. ©1994 IEEE.)

Figure 2.16 shows the results of similar measurements on devices with a BOX of various thicknesses. Clearly, the temperature increases as the BOX becomes thicker; but the effects of self-heating are fairly small in a low-voltage circuit with a power consumption of about 1 mW.

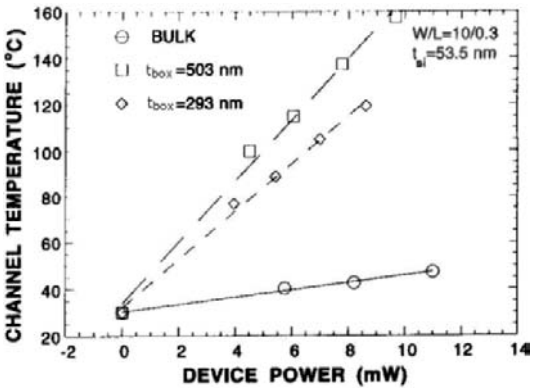


Fig. 2.16 Channel temperature versus power for SOI devices, with the thickness of the BOX as a parameter, and for a bulk-Si device for comparison. (From L. Su et al. [2.19]. ©1994 IEEE.)

According to a recent report, the time constant of thermal heating is about 100 ns [2.20], which means that dynamic self-heating effects can be ignored in digital circuits in which the switching speed of the devices is faster than that. However, it has also been reported that problems can occur in analog circuits [2.21]. The application of SOI technology to analog circuits is an issue that requires further study.

2.3 Theoretical Basis of FD-SOI Device Operation: DC Operation

Figure 2.17 shows a schematic cross section of an SOI MOSFET. In the following, we assume an n-channel SOI MOSFET. Since there are two channels inside the body, there are six current flows at the onset of inversion: the front-channel current, the back-channel current, the band-to-band tunneling currents at the front and back interfaces of the drain junction, and double injection currents at the source junction. On the other hand, in the subthreshold region, there are subthreshold currents at the front and back interfaces. This chapter focuses on the DC characteristics of FD-SOI MOSFETs, and presents a theoretical analysis of the subthreshold and post-threshold current characteristics as an aid to device design.

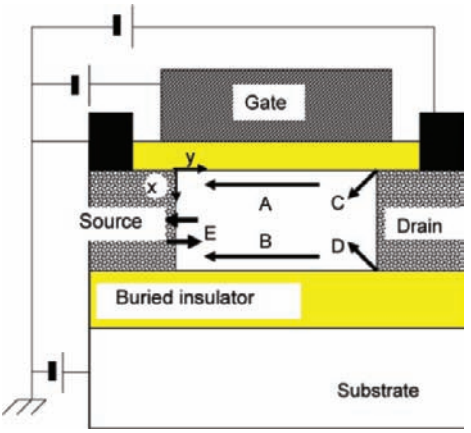


Fig. 2.17 Cross section and operation of fully-depleted SOI MOSFET. A: Normal front channel, B: Normal back channel, C: Avalanche and band-to-band tunneling current (front side), D: Avalanch eand band-to-band tunneling current (back side), E: Double injection due to parasitic bipolar action

2.3.1 Subthreshold Characteristics

Many papers have described the basic features of the subthreshold characteristics of FD-SOI MOSFETs [2.22]. The input capacitance consists of

4 components in series: (1) the capacitance of the gate insulator, (2) the capacitance of the SOI layer (which is equivalent to the depletion layer of a bulk MOSFET), (3) the capacitance of the buried insulator, and (4) the capacitance of the depletion layer beneath the buried insulator, if the buried insulator is thin. As a result, the effective input capacitance in the subthreshold region is quite small, which makes the subthreshold swing small [2.22].

In the subthreshold regime, the drain current (Fig. 2.18) is given by

$$I_{D(sub)} = I_{D(sub),\,front} + I_{D(sub),back} + I_{D(sub),other}\ , \tag{2.14}$$

where $I_{D(sub),front}$ and $ID_{(sub),back}$ are the subthreshold currents near the front and back interfaces, respectively, and $I_{D(sub),other}$ is the combined current attributable to parasitic phenomena, such as simple avalanche at the drain junction [2.23], band-to-band (BTB) tunneling at the drain junction [2.24]-[2.25] and the generation-recombination (GR) process [2.26]. For simplicity, this discussion will focus on $I_{D(sub),front}$.

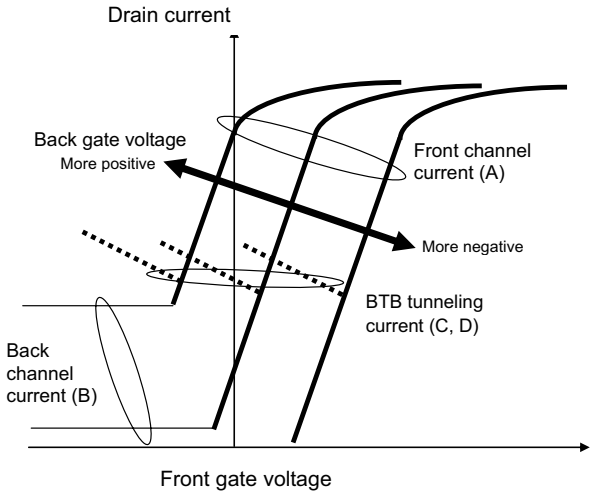


Fig. 2.18 Subthreshold and off-state current characteristics of FD-SOI MOSFET.

For an n-channel SOI MOSFET, it is

$$I_{D(sub),front} = -qAD_n \frac{dn}{dy} = qAD_n \frac{n(0) - n(L)}{L}, \tag{2.15}$$

where A is the cross-sectional area of the channel; and n(0) and n(L) are the electron concentrations at the edges of the source and drain, respectively. They are given by

$$n(0) = n_i \exp\left[\frac{\left(E_F - E_i + q\phi_{s,front}\right)}{kT}\right] \quad \text{and} \tag{2.16}$$

$$n(L) = n_i \exp\left[\frac{\left(E_F - E_i + q\phi_{s,front} - qV_D\right)}{kT}\right], \tag{2.17}$$

where $\phi_{s,front}$ is the surface potential at the top of the SOI layer. If we assume the effective channel depth to be kT/qE_s, where E_s is the surface electric field [2.27], the subthreshold current can be written as

$$I_{D(sub),front} = \mu_n \left(\frac{W}{L}\right) q \left(\frac{kT}{q}\right)^2 \left(\frac{n_i^2}{N_A}\right) \left\{1 - \exp\left[\frac{-qV_D}{kT}\right]\right\} \frac{\exp\left[\frac{q\phi_s}{kT}\right]}{E_S}, \tag{2.18}$$

where μ_n is the electron mobility calculated from the Einstein relation $D_n = \mu_n kT/q$. The theoretical expression for the E_s of an FD-SOI MOSFET is different from that for a bulk MOSFET because the depth profile of the internal potential is different [2.22]. Nevertheless, we can derive the following basic expression for the subthreshold swing from (2.18) if we neglect the influence of interface states for simplicity.

$$S = \left(\frac{kT}{q}\right) \ln(10) \left\{1 + \frac{C_s}{C_{ox}}\right\}, \tag{2.19}$$

where

$$C_s = \frac{C_{SOI}C_{BOX}C_{sub}}{(C_{SOI}C_{BOX} + C_{BOX}C_{sub} + C_{sub}C_{SOI})}, \quad (2.20)$$

C_{ox} ($=\varepsilon_{ox}/T_{ox}$) is the capacitance of the gate oxide layer, C_s is the total capacitance of the substrate, C_{SOI} ($= \varepsilon_{Si}/T_{SOI}$) is the equivalent capacitance of the SOI layer, C_{BOX} ($=\varepsilon_{ox}/T_{BOX}$) is the capacitance of the buried-oxide (BOX) layer, C_{sub} is the capacitance of the depletion layer beneath the BOX when the substrate is p-type, T_{ox} is the thickness of the gate oxide layer, T_{SOI} is the thickness of the SOI layer, and T_{BOX} is the thickness of the BOX. As seen in (2.19), the basic expression for S is the same for FD-SOI and bulk MOSFETs, although the complete expression for C_s is quite different. S is usually smaller for an FD-SOI MOSFET than for a bulk MOSFET because C_s is smaller than the depletion layer capacitance of a bulk MOSFET.

When $I_{D(sub),back}$ exists, we obtain the following expression for S:

$$S = \frac{dV_{FG}}{d\left[\log\left(I_{D(sub),front} + I_{D(sub),back}\right)\right]}. \quad (2.21)$$

This means that the subthreshold current near the back interface degrades the subthreshold swing of the front gate. The main conclusions that can be drawn from (2.19) are listed below.

A. Influence of T_{SOI} on S

The most common way to suppress short-channel effects is to reduce T_{SOI} [2.22], which makes C_s approach C_{BOX} ($=\varepsilon_{ox}/T_{BOX}$), as shown by (2.20). This means that T_{BOX} limits the straightforward reduction of S. In other words, T_{BOX} should be large in consideration of S.

B. Influence of T_{BOX} on S

A less common way to suppress short-channel effects is to reduce T_{BOX} [2.28] and [2.29], which makes C_s approach C_{SOI} ($= \varepsilon_{si}/T_{SOI}$), as shown by (2.20). This often causes S to increase. To prevent that, T_{ox} should also be reduced when T_{BOX} is reduced.

C. DIBL (front interface) and BIBL (back interface) (Fig. 2.19)

In a short-channel bulk MOSFET, drain-induced barrier lowering (DIBL) [2.30] near the source junction at the front interface significantly degrades the

subthreshold swing. In an FD-SOI MOSFET, buried-insulator-induced barrier lowering (BIBL) [2.28] near the source junction at the back interface also significantly influences the subthreshold swing. The reason for this is that the lateral electric field extends quite far into the buried insulator because the insulator has a much lower permittivity than Si. There are two ways to suppress this extension: one is to make the buried insulator (ex. SiO_2) thinner, and the other is to replace it with a high-k material. However, the latter degrades the subthreshold swing because reducing the equivalent oxide thickness (EOT) pulls down the body potential at the back interface of the SOI layer.

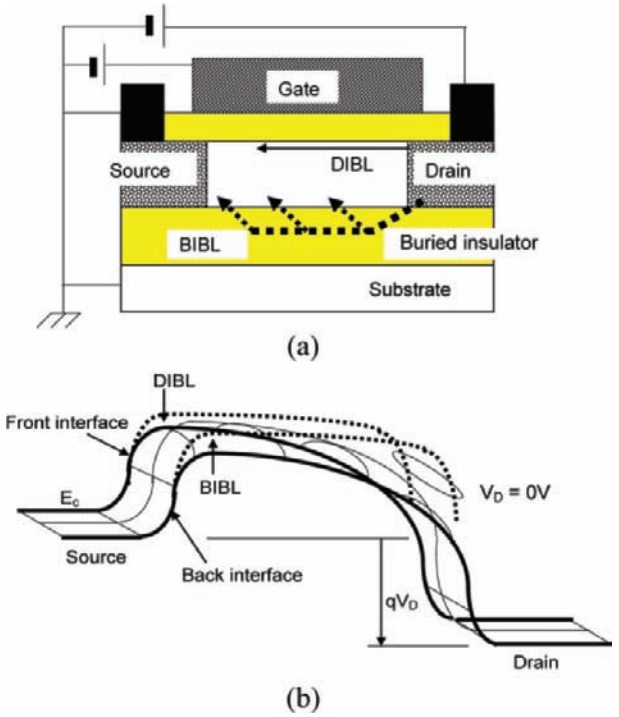


Fig. 2.19 (a) Schematic and (b) potential profiles of DIBL and BIBL in FD-SOI MOSFET.

D. Influence of band-to-band tunneling current

Band-to-band (BTB) tunneling often occurs in the gate-drain overlap region

[2.24]. It is sometimes called the gate-induced drain leakage (GIDL) current. For a thin SOI MOSFET, it also has a significant influence on DC and AC operation [2.25], [2.31], and [2.32].

An empirical expression for this current is [2.24]

$$I_{D(sub),others} = A_0 E_{SS} \exp\left[\frac{-B_0}{E_{SS}}\right], \tag{2.22}$$

where A_O and B_O are constants that depend on the device parameters, and E_{SS} is the surface electric field of the overlap region. Since the gate oxide and BOX layers of recent ultrathin SOI MOSFETs tend to be very thin, the electric fields of the gate-drain and drain-substrate overlap regions are higher than those of previous devices. As a result, the contribution of the BTB tunneling current to the subthreshold characteristics is apt to be significant [2.32].

2.3.2 Post-threshold Characteristics

In the post-threshold regime, the drain current is given by

$$I_{D(post)} = I_{D(post),front} + I_{D(post),back} + I_{D(post),other}, \tag{2.23}$$

where $I_{D(post),front}$ is the inversion channel current along the front interface, $I_{D(post),back}$ is the inversion channel current along the back interface, and $I_{D(post),other}$ is the parasitic current, which consists of an additional floating-body-induced current [2.3], a parasitic bipolar current [2.15], and an avalanche current [2.33]. The discussion below focuses on $I_{D(post),front}$.

In practice, the post-threshold channel current consists mainly of the drift current, which is accelerated by the drain-to-source electric field. It is analyzed in a way similar to the conventional gradual channel approximation. The key difference comes from the limited depletion region beneath the channel, as shown in Fig. 2.17. When T_{SOI} is larger than the depth of the depletion layer, an SOI MOSFET operates just like a bulk one under a DC bias, and is called a partially depleted (PD) SOI MOSFET. So, it should have almost the same drain current as a bulk MOSFET. The expression for the drain current of an SOI MOSFET is derived below.

We start from the Ohmic relation

$$I_{D(post),front} = -W\mu_n Q_n(V)\frac{dV}{dy} \ , \qquad (2.24)$$

where V is the local channel potential and $Q_n(V)$ is the local electronic charge density. This is the expression for the local current inside the device, if we neglect the diffusion and other currents like the GR current. Since an SOI MOSFET has both front and back channels, the discussion will focus on the front one ($I_{D(post),front}$) for simplicity.

We obtain the following relation for $Q_n(V)$ from Poisson's equation for the SOI layer [2.34], [2.35]:

Q_n =total induced charge density of semiconductor
– depletion charge density of SOI layer
– total induced charge density of substrate beneath buried insulator,

$$= -C_{ox}\left(V_{FG} - V_{FB,front} - \phi(0) - V\right) + qN_A T_{SOI} + \varepsilon_s \left.\frac{d\phi(x)}{dx}\right|_{x=T_{SOI}} \ , \qquad (2.25)$$

where the potential gradient at the back interface ($d\phi(x)/dx|_{x=TSOI}$) is [2.37]

$$\left.\frac{d\phi(x)}{dx}\right|_{x=T_{SOI}} = \frac{qN_A}{2C_{SOI}} + \frac{\left(\phi(T_{SOI}) - \phi(0) - V\right)}{T_{SOI}} \ . \qquad (2.26)$$

This yields the approximation [2.28]

$$\phi(T_{SOI}) = \frac{\left\{-\left(\frac{1}{2}\right)qN_A T_{SOI} + C_{BOX}V'_{BG} + C_{SOI}\left[\phi(0) + V\right]\right\}}{\left(C_{SOI} + C_{BOX}\right)} \ , \qquad (2.27)$$

where V'_{BG} is the effective back-gate bias. Substituting (2.25)-(2.27) into (2.24) and integrating it from source to drain, we obtain the following expression for $I_{D(post),front}$:

$$I_{D(post),front} = \left(\frac{W}{L}\right)\mu_n C_{ox}\left[V_{FG} - V_{th}^{*} - \frac{(1+\alpha)V_D}{2}\right]V_D \ , \qquad (2.28)$$

where

$$V_{th}^{*} = V_{FB,front} + (1+\alpha)\,\phi_{s,front} + \left(\frac{3}{2}\right)(1+\gamma)\frac{qN_A\ T_{SOI}}{C_{ox}} - \alpha\ V'_{BG} \ , \qquad (2.29)$$

and α and γ are the geometrical parameters

$$\alpha = \frac{C_{SOI}C_{BOX}}{C_{ox}(C_{SOI} + C_{BOX})} \ , \qquad (2.30)$$

$$\gamma = \frac{C_{SOI}}{3(C_{SOI} + C_{BOX})} \ . \qquad (2.31)$$

α is not zero in either an FD-SOI or a bulk MOSFET. When we reduce T_{BOX} in order to suppress short-channel effects, we must also reduce T_{ox} and/or T_{SOI} to suppress the increase in α.

In many cases, we have the condition $T_{BOX} >> T_{SOI}$ and $T_{BOX} >> T_{ox}$. When C_{BOX} approaches 0 (T_{BOX} is close to infinity), (2.28) can be simplified. That is, if we assume that the BOX is very thick, the electric field across it is quite low; so there is almost no depletion or accumulation of charge beneath it. Thus, $Q_n(V)$ can be simplified to

Q_n = total induced charge density of semiconductor
– depletion charge density of SOI layer

$$= -C_{ox}\left(V_{FG} - V_{FB,front} - \phi_{s,front} - V\right) + qN_A W_D(V) \ . \qquad (2.32)$$

For a PD-SOI MOSFET, this expression holds because $W_D(V) < T_{SOI}$. This suggests that $I_{D(post)}$ is almost the same as that for a bulk MOSFET. However, for an FD-SOI MOSFET, $W_D(V) > T_{SOI}$. So, we have to replace the above expression with

$$Q_n = -C_{ox}\left(V_{FG} - V_{FB,front} - \phi_{s,front} - V\right) + qN_A T_{SOI} \quad . \tag{2.33}$$

Since this is an approximate expression, the quantitative agreement with experimental results is not discussed. Substituting the new expression for $Q_n(V)$ into the Ohmic relation (2.24) and assuming current continuity yields the following expression for $I_{D(post),front}$:

$$I_{D(post),front} = \left(\frac{W}{L}\right)\mu_n C_{ox}\left[V_{FG} - V_{th,front} - \frac{V_D}{2}\right]V_D \quad , \tag{2.34}$$

where the threshold voltage of an FD-SOI MOSFET ($V_{th,\,front}$) is

$$V_{th,front} = V_{FB,front} + \phi_{s,front} + \frac{qN_A T_{SOI}}{C_{ox}} \quad . \tag{2.35}$$

This expression was derived in order to explain the threshold voltage of an FD silicon-on-sapphire (SOS) MOSFET. It means that the threshold voltage of an FD-SOI MOSFET is usually smaller than that of a bulk one with the same device parameters, as you would expect. Since the depth of the depletion layer is limited to T_{SOI}, the drop in the gate oxide voltage is also smaller, which often results in a lower effective surface electric field, accompanied by the apparent enhancement of the electron mobility [2.36]. However, it should be noted that there are some conditions for T_{SOI} and N_A that produce a lower surface electric field [2.37]. The saturated drain current ($_{ID(post)sat}$) is given by

$$I_{D(post)sat} = \left(\frac{W}{2(1+\alpha)L}\right)\mu_n C_{ox}\left[V_{FG} - V_{th,front}\right]^2 \quad . \tag{2.36}$$

This expression means that an FD-SOI MOSFET has a larger drivability than either a PD-SOI or a bulk MOSFET because of the low threshold voltage and high carrier mobility. This is a significant advantage. Finally we address the issue of volume inversion. When T_{SOI} is very small, the potential profile in the depth direction is flat at the onset of surface inversion; and the inversion layer also spreads over the body [2.39]. Simulations show that the drivability is doubled [2.38]. However, we can really only expect such good performance in long-channel devices [2.39] because the transverse field is effectively reduced when the body is extremely thin [2.40].

2.3.3 Short-Channel Effects

First of all, we derive the theoretical expression for the threshold voltage of an FD-SOI MOSFET [2.28], [2.34]. The depletion approximation and Poisson's equation yield the following relation:

$$\phi(x) = \phi_b + \left(\frac{qN_A}{2\varepsilon_{si}}\right)(T_{SOI} - x)^2 - (T_{SOI} - x)\left.\frac{d\phi(x)}{dx}\right|_{x=T_{SOI}}, \qquad (2.37)$$

where

$$\phi_b = \frac{\left[-\left(\frac{1}{2}\right)qN_A T_{SOI} + C_{BOX}V'_{BG} + C_s\phi_{s,front}\right]}{(C_s + C_{BOX})}. \qquad (2.38)$$

This in turn yields

$$V_{th} = V_{FB,front} + \phi_{s,front} + \frac{qN_A T_{SOI}}{C_{ox}} + \left(\frac{\varepsilon_{si}}{C_{ox}}\right)\left.\frac{d\phi(x)}{dx}\right|_{x=T_{SOI}}$$

$$= V_{FB,front} + (1+\alpha)\phi_{s,front} + \left(\frac{3}{2}\right)(1+\gamma)\frac{qN_A T_{SOI}}{C_{ox}} - \alpha V'_{BG}\ . \qquad (2.39)$$

Considering a simple phenomenalistic model of short-channel effects, we obtain

$$Vth = V_{FB,front} + f_{DIBL}(1+\alpha)\phi_{s,front} + \left(\frac{3}{2}\right)f_{CS}(1+\gamma)\frac{qN_A T_{SOI}}{C_{ox}} - \alpha V'_{BG}, \qquad (2.40)$$

where f_{DIBL} is the DIBL factor and f_{CS} is the charge-sharing factor. Generally speaking, an FD-SOI MOSFET is not very susceptible to DIBL because the effective surface potential is deeper than for a bulk MOSFET, as can be seen in (2.39). It can also be seen that there is comparatively little charge sharing in an FD-SOI MOSFET because the depletion charge density is lower than in a bulk MOSFET.

In FD-SOI MOSFETs, the body is fully depleted, which means that the entire SOI layer functions as a charged insulator. The drain-induced potential easily penetrates the SOI and BOX layers, which results in BIBL, as shown in Fig. 2.19. To suppress it, we have to make the BOX thinner, as explained in the previous section. However, that degrades the subthreshold swing because the potential at the SOI/BOX interface is easily pinned by the substrate potential. Thus, it is necessary to optimize the thicknesses of the SOI and BOX layers.

2.4 FD-SOI CMOS Process Technology

SOI process technology for CMOS circuits is very similar to the technology for bulk-Si devices. The main structural difference is that SOI wafers have a buried-oxide (BOX) layer between the SOI layer and the silicon substrate. In one sense, the BOX layer simplifies the fabrication process because it provides a perfect isolation structure. On the other hand, the difficult technologies needed for processing the SOI layer, especially the thin SOI layer of FD-SOI devices, makes the SOI process more complex than the bulk one.

This section first describes the typical fabrication process for thin-film FD-SOI CMOS devices. It is applicable to the quarter-micron generation. Then, problems with the FD-SOI process and some solutions are discussed.

2.4.1 Fabrication Process for FD-SOI CMOS Devices

The main steps in the fabrication of FD-SOI CMOS devices are illustrated schematically in Fig. 2.20. For each step, the bulk-Si and FD-SOI processes are compared and the differences and advantages are pointed out.

Step 1: Field oxidation
The purpose of the first step is device isolation. There are many ways to isolate the active-Si region, such as the local oxidation of silicon (LOCOS), shallow trench isolation (STI), and mesa [2.41]. A simpler, cheaper process can be used for SOI devices than for bulk ones because the vertical isolation already exists in the form of the BOX. For FD-SOI devices, LOCOS can be used down to an isolation width of 0.20 μm because the active-Si layer is much thinner in FD-SOI than in bulk-Si or PD-SOI devices. [2.42].

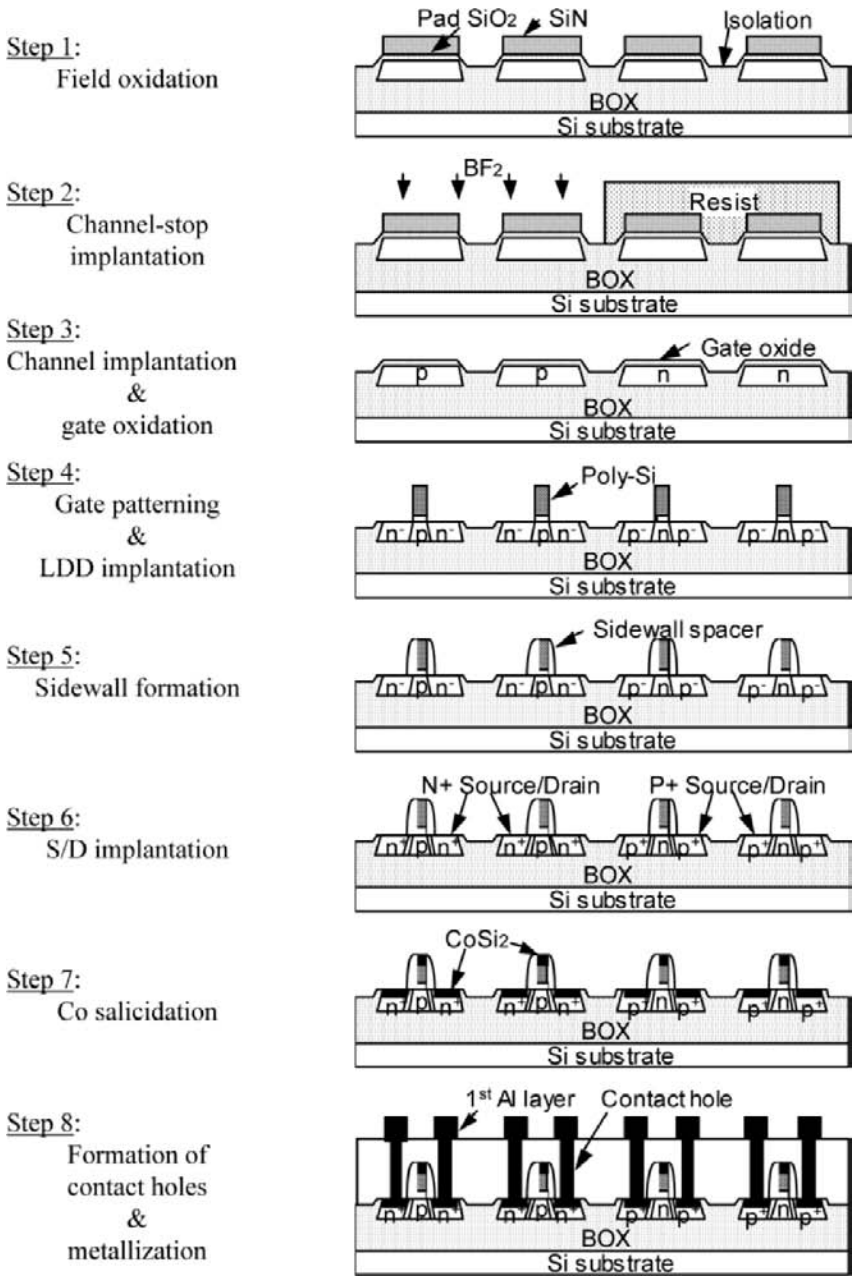


Fig. 2.20 Fabrication process for FD-SOI CMOS devices.

Another advantage of SOI devices is that perfect isolation can be achieved by surrounding SOI islands with SiO_2. This allows higher integration densities than is possible with bulk CMOS and provides latch-up-free operation.

Step 2: Channel-stop implantation
Boron is implanted into just the n-channel region using BF_2 as the source. The energy is low enough that the boron does not penetrate the SiN film used as a mask for field oxidation. This step suppresses leakage current. In bulk devices, boron implantation (channel-stop implantation) prevents the surface inversion of the Si under the field oxide, which would create a leakage path between n-channel devices. In SOI devices, a similar type of implantation prevents source-to-drain leakage at the edges of the SOI regions under the gates. The edge leakage current flows through a parasitic channel, which has a V_{th} lower than that of the main channel. Boron implantation raises the V_{th} of the parasitic edge transistor above that of the main transistor, thus suppressing the edge leakage current. p-channel devices do not usually have this problem, probably because of the different segregation properties of the channel dopants: the boron for the n-channel tends to segregate into oxide, while the arsenic or phosphorus for the p-channel tends to segregate into Si.

Step 3: Channel implantation and gate oxidation
Next, channel implantation to set V_{th} and gate oxidation are performed. There are two differences between the channel implantation conditions of SOI and bulk processes. The first is that an SOI device does not need a well structure. This reduces both the number of process steps and the cost. The other is that the implantation energy is lower for FD-SOI than for bulk devices because the SOI layer is very thin (T_{SOI} < ~60 nm). If the energy used for SOI devices is too high, a great deal of impurities will be implanted into the BOX through the SOI layer, which will cause variations in V_{th}. The effect of channel doping is discussed in 2.4.2 A.

Step 4: Gate patterning and LDD implantation
After gate patterning, implantation to form a lightly doped drain (LDD) is performed. One advantage of FD-SOI devices is that they do not require drain engineering because the source and the drain are very shallow due to the thin SOI layer. In some generations, LDD implantation is not necessary [2.42], [2.44]. However, as the gate length shrinks, short-channel effects become more of a problem in FD-SOI devices. In the bulk process, extension and pocket implantation are commonly used to suppress short-channel effects and to obtain a higher drain current. The effectiveness of pocket implantation in the FD-SOI process is discussed in 2.4.2 B.

Step 5: Sidewall formation
This step involves the deposition of dielectric film and subsequent etch back by reactive ion etching (RIE) to form the gate sidewall. The etching requires a high selectivity [2.43]. If it is too small, the source and drain regions are etched during over-etching, which makes the active-Si (SOI) layer too thin. This in turn makes the resistance of the source and drain (S/D) too high and can cause contact failures.

Step 6: S/D implantation
n+ and p+ S/D regions are formed by high-dose implantation; and rapid thermal annealing (RTA) activates the dopants. Since both dopants are also implanted into the poly-Si, gates become n+ and p+ poly-Si for n- and p-channel MOSFETs, respectively. The implantation energy for FD-SOI devices is critical. A dose on the order of 10^{19} cm^{-3} makes Si amorphous; but amorphized Si can be recrystalized by activation annealing if there is a layer of crystal underneath it. The danger is that, if the SOI layer in the S/D regions is fully amorphized, it cannot be recrystalized because only the BOX layer remains underneath. So, the energy must be low enough that the SOI layer is not fully amorphized.

Step 7: Co salicidation
Salicidation (self-aligned silicidation) is often used to reduce the sheet resistances of the S/D and the gate. Reports have appeared on the use of $TiSi_2$ [2.44], $CoSi_2$ [2.45], and NiSi [2.46] for this purpose in the FD-SOI process. The difficulties with salicidation for FD-SOI devices derive from the extreme thinness of the SOI layer; the silicide must be thinner than that layer. That is, excess Ti or Co produces a high sheet resistance because it turns the SOI layer into mono-silicide, which has a high resistivity, rather than di-silicide, which has a low resistivity. Moreover, there is another reason to keep the silicide from reaching the BOX. Complete silicidation results in a high S/D series resistance because it makes the area of the lateral interface between the active-Si and silicide regions too small. To obtain a reasonably low series resistance, the thickness of the silicide should be no more than 80% of the thickness of the SOI layer [2.47].

Step 8: Formation of contact holes and metallization
In the final step, an interlayer dielectric film is deposited, and contact holes are formed. The etching method used to open the holes must have a high

selectivity and not etch the Si [2.43]. Then, the same metallization process as that used for bulk Si is carried out. These are the typical steps in the SOI fabrication process.

Fig. 2.21 shows a cross-sectional TEM image of a fabricated 0.15-μm FD-SOI MOSFET. The Si in the channel region is 40 μm thick, the BOX is 200 μm thick, and the gate oxide is 2.5 μm thick.

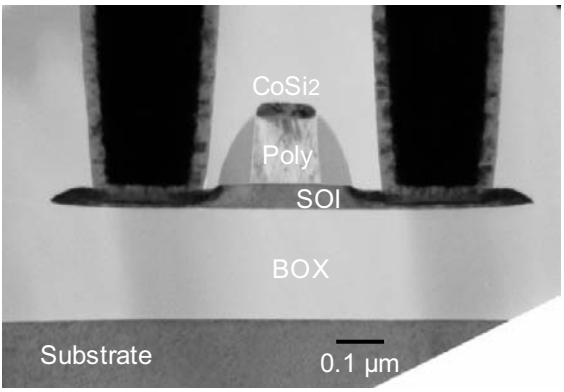


Fig. 2.21 Cross-sectional TEM micrograph of a 0.15-μm FD-SOI MOSFET.

2.4.2 Problems and Solutions in FD-SOI Process Technology

In order to obtain a fully-depleted body and suppress short-channel effects (SCE) in scaled-down SOI CMOS devices, the SOI layer must be very thin (T_{SOI} < ~50 nm). [2.29], [2.48] The difficulty in mass-producing FD-SOI devices comes from the thinness of this layer. The main problems and some solutions are illustrated in Fig. 2.22.

The first problem concerns the fact that the threshold voltage (V_{th}) of an FD-SOI device depends on the thickness (T_{SOI}) of the SOI layer. Since T_{SOI} is generally not uniform across a wafer, variations in V_{th} inevitably arise. In order to obtain a V_{th} comparable to that for a thick SOI layer, a thin SOI layer must have a higher substrate doping concentration (N_A). It is thought that V_{th} becomes more sensitive to T_{SOI} as the SOI layer becomes thinner. A simple

solution is to improve the uniformity of T_{SOI} across a wafer. However, T_{SOI} is not always uniform in commercially available SOI wafers, and that makes it necessary to control the channel doping profile.

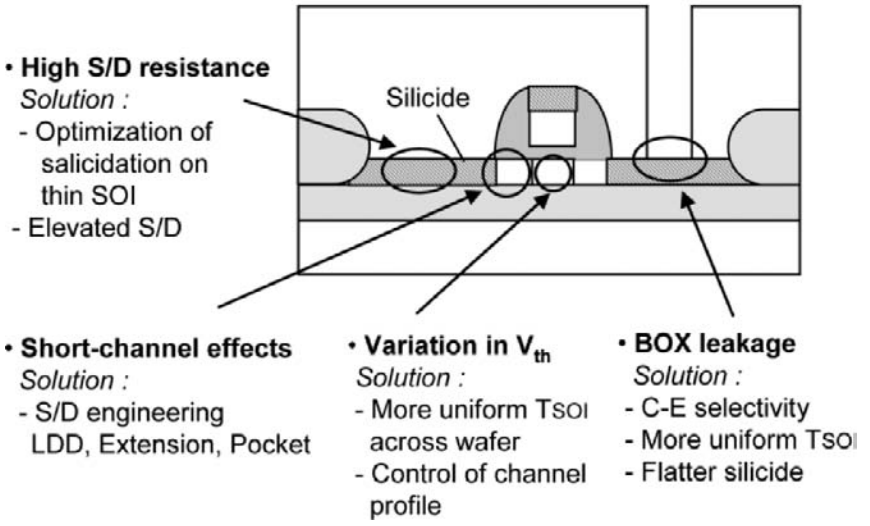


Fig. 2.22 Problems and solutions in fabrication of thin-film FD-SOI devices.

The second problem is short-channel effects, which increasingly degrade control of V_{th} as the gate length becomes smaller. Several methods have been proposed to solve this problem, such as the further thinning of the SOI layer and the use of a multigate structure [2.49], [2.50]. Section B below discusses the effectiveness of a source/drain extension structure with pocket implantation, which is a common S/D engineering technique for bulk-Si devices.

The third problem is the leakage current between the SOI layer and the substrate through the BOX, which leads to device failure due to excessive standby current in circuits. There is speculation that the cause is a threading pinhole through the BOX that forms when the contact holes are opened. In order to prevent pinholes, the selectivity of contact-hole etching, the uniformity of T_{SOI}, and the flatness of the silicidized SOI layer must all be improved.

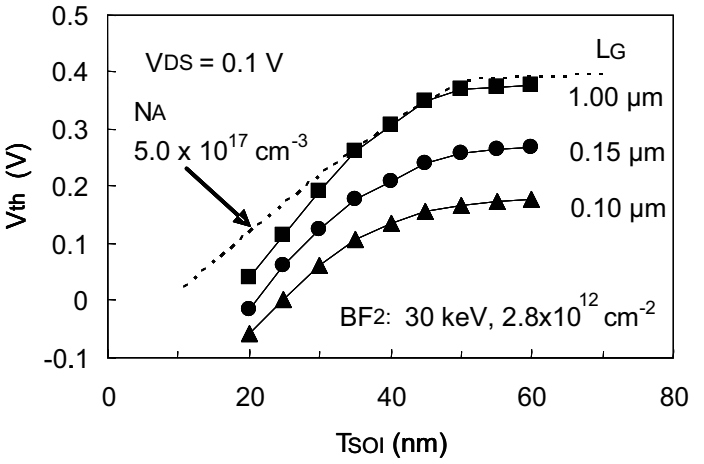
The fourth problem is an increase in the parasitic source/drain series resistance, which degrades circuit speed. One solution is to optimize the salicidation conditions for a thin SOI layer. Another is to use a thicker SOI layer for the S/D regions than for the channel region. There are two ways of accomplishing that. One is to use a thick SOI film and thin the channel regions by LOCOS (recessed channel [2.51]). The other is to use a thin SOI film and use selective epitaxial growth to make the source and drain regions thicker (elevated S/D [2.52], [2.53]).

A. Variation in V_{th}

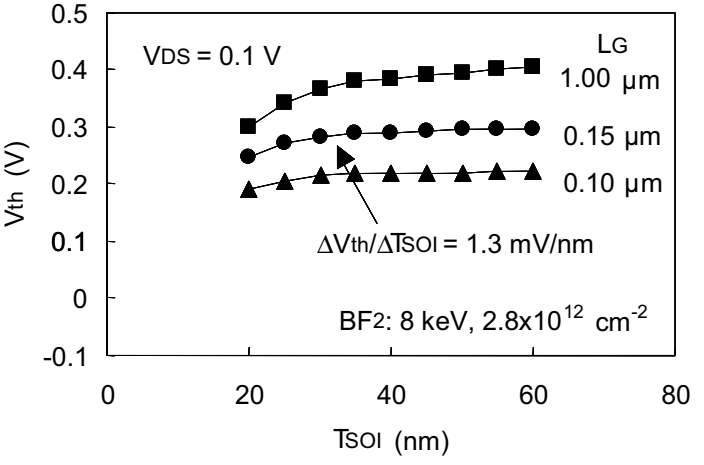
Sherony et al. [2.54] demonstrated through simulations and experiments that designing the channel implantation so that the dose in the SOI layer would be constant reduced the sensitivity of V_{th} to T_{SOI} in devices with a relatively long gate (L = 2 μm) . However, it is not clear that this would work with a short gate and a thin SOI layer. In order to find a way to reduce the sensitivity of V_{th} to T_{SOI}, simulations and experiments were carried out to investigate the effect of the channel implantation conditions on 0.15-μm FD-SOI nMOSFETs .

Figure 2.23 shows some simulation results on the dependence of V_{th} on T_{SOI} for two channel implantation energies (8 keV, 30 keV). The dependence is much weaker for the lower implantation energy, for which $\Delta V_{th}/\Delta T_{SOI}$ is as low as 1.3 mV/nm. It was found that, at the lower energy, almost all the dopant is implanted into the 25-nm-thick SOI layer; and the dose is almost uniform within that layer. On the other hand, at the higher energy, the channel doping characteristics are almost the same as for a constant N_A, which is indicated by the dotted line in Fig. 2.23(a).

Figure 2.24 shows the dependence of V_{th} on T_{SOI} for 0.15-μm FD-SOI nMOSFETs fabricated using a channel implantation energy of 8 keV. The dotted line indicates the results of a simulation that assumed the experimental conditions. Just as for the simulation results in Fig. 2.23, Vth is almost independent of T_{SOI} when T_{SOI} is between 25 and 40 nm. On the other hand, the difference in V_{th} between devices with gate lengths of 1.0 and 0.15 μm (V_{th} roll-off) decreases as the SOI layer becomes thinner. This seems to be due to the fact that the gate has a stronger electric field than the drain when the SOI layer is thin. These results indicate that, even for 0.15-μm FD-SOI nMOSFETs in a thin SOI layer, optimizing the channel implantation conditions can reduce the sensitivity of Vth to TSOI and suppress short-channel effects.



(a)



(b)

Fig. 2.23 Simulation results on dependence of V_{th} on T_{SOI} for 0.15-μm FD-SOI nMOSFETs with different channel-implantation energies: (a) 30 keV and (b) 8 keV.

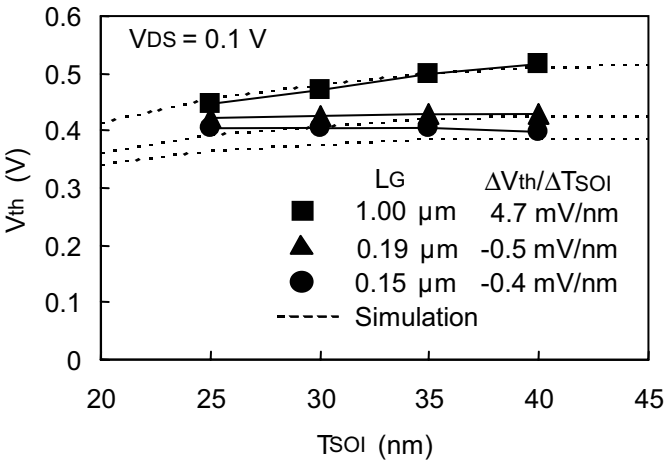


Fig. 2.24 Dependence of V_{th} on T_{SOI} for 0.15-μm FD-SOI nMOSFETs fabricated with a low channel-implantation energy (8 keV).

Figure 2.25 is a plot of the standard deviation (σ) of V_{th} vs. T_{SOI} for 0.15-μm FD-SOI nMOSFETs fabricated with a low channel implantation energy. σ is small enough (< 10 mV) when TSOI is between 25 and 40 nm.

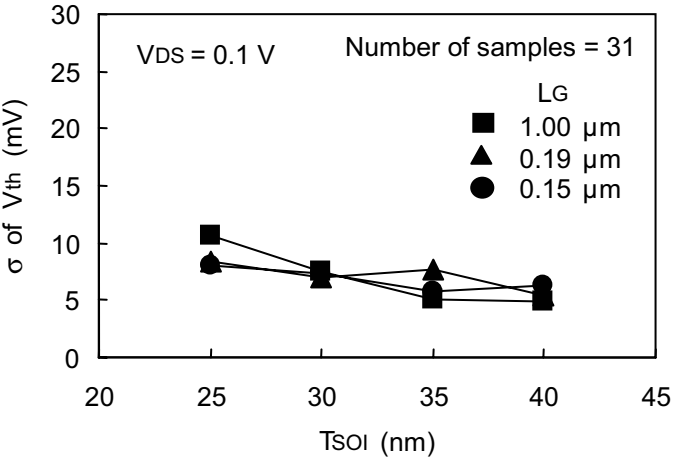


Fig. 2.25 Standard deviation (σ) of Vth vs. T_{SOI} for 0.15-μm FD-SOI nMOSFETs fabricated with a low channel-implantation energy (8 keV).

B. Short-channel effects

An SOI depletion-mode MOSFET with an undoped body has a high carrier mobility due to both the suppressed vertical electric field and also reduced impurity scattering [2.55]. This is a feasible FD-SOI device because a thin SOI layer eliminates punch-through and the perfect isolation eliminates latch-up. However, the problem with it is that the control of V_{th} becomes worse as the gate length is reduced due to short-channel effects. One solution is a source/drain extension structure with pocket implantation, which reduces V_{th} roll-off and provides a high drivability, as explained below.

Figure 2.26 shows the measured and simulated gate length dependence of V_{th}, with the doping concentration of the pocket region as a parameter. The results show that increasing the pocket doping concentration not only reduces V_{th} roll-off, but also suppresses the change in V_{th} with gate length.

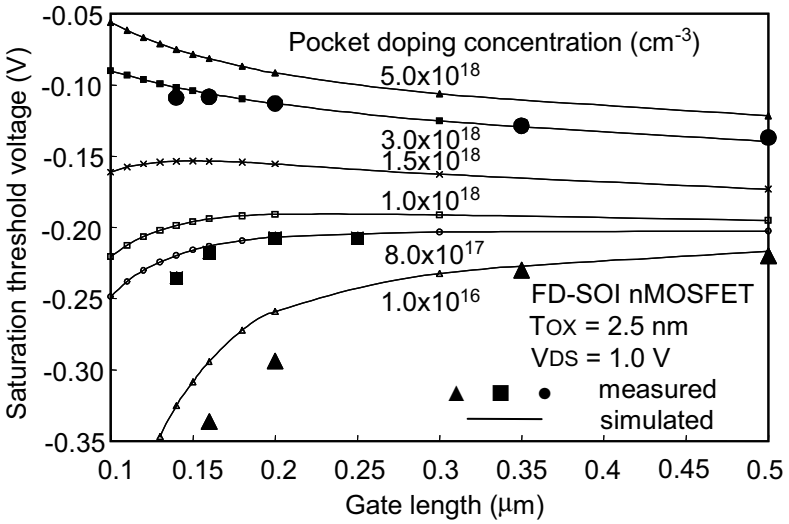


Fig. 2.26 Measurement and simulation results on dependence of V_{th} on gate length for undoped-channel nMOSFETs, with pocket doping concentration as a parameter.

Figure 2.27 compares the DC characteristics of enhancement-mode (N_{body} = 3.0×10^{17} cm^{-3}) and depletion-mode (N_{body} = 1.0×10^{15} cm^{-3}) SOI nMOSFETs with an undoped body and a gate length of 0.15 μm. Short-channel effects are comprehensively suppressed in the depletion-mode type, and the current drivability is about 1.5 times larger than that of the enhancement-mode type. The better current drivability results from the lower V_{th} and the higher mobility, which in turn come from reduced impurity scattering and suppression of the effective field.

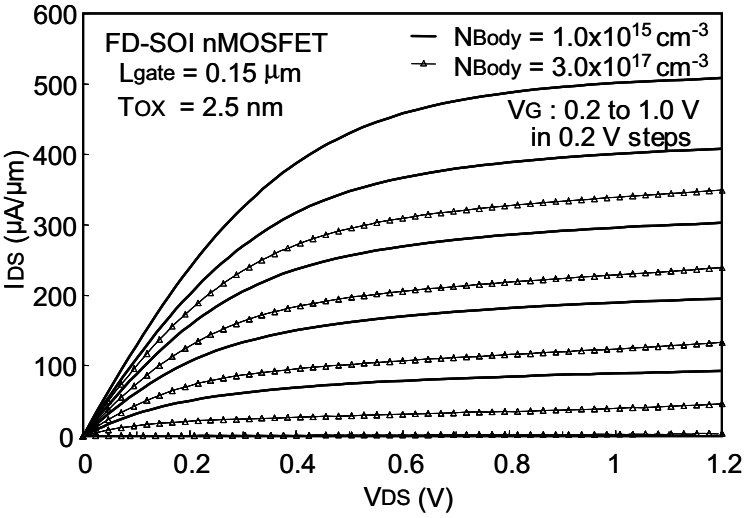


Fig. 2.27 Measured I_{DS}-V_{DS} characteristics of depletion-mode and enhancement-mode nMOSFETs.

In order to separate the effect of the higher mobility, the drain current of nMOSFETs with various gate lengths was measured at $V_{GS} - V_{th} = 1$ V (Fig. 2.28). It can be seen that the drain current of a depletion-mode MOSFET with an undoped body is 10 to 25% higher than that of an enhancement-mode MOSFET.

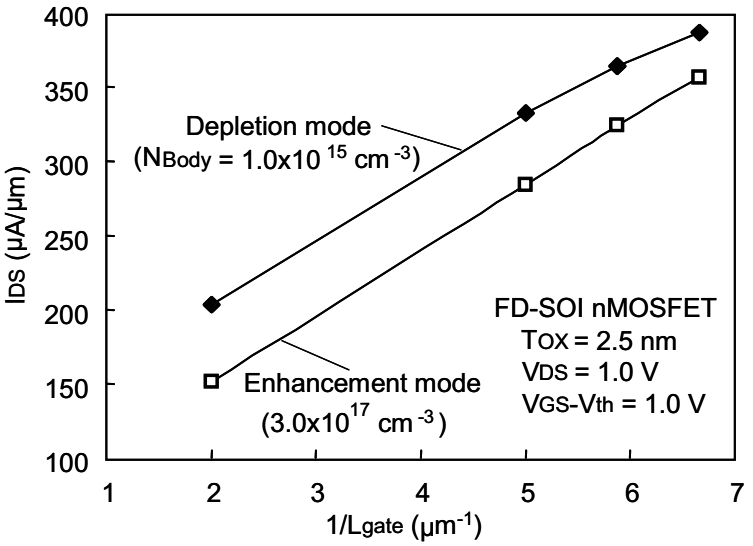


Fig. 2.28 Relationship between normalized drain current and gate length for depletion- and enhancement-mode nMOSFETs.

C. BOX leakage

Figure 2.29 shows a cross-sectional TEM image of a leakage point in the BOX after conventional silicidation with $CoSi_2$. Notice the pinhole that formed during contact-hole etching on a thin spot of the silicidized SOI layer. Thin spots seem to appear at triple junctions of silicide grains; so, the BOX leakage strongly depends on the grain size of the silicide.

The problem of poor manufacturability due to BOX leakage was overcome by using the contact-hole-etching-prior-to-second-annealing (CHEPSA) Co salicide process module [2.56]-[2.58], which is illustrated in Fig. 2.30. As the name indicates, the contact-hole etching is performed before the second rapid thermal annealing (RTA) for salicidation. AFM measurements of a silicide surface showed the typical peak-to-valley height to be 3 nm after the 1st RTA and 35 nm after the 2nd. With CHEPSA, the surface morphology of the silicide during contact-hole etching is almost the same as that after the 1st RTA because the 2nd RTA is performed after the contacts have been opened.

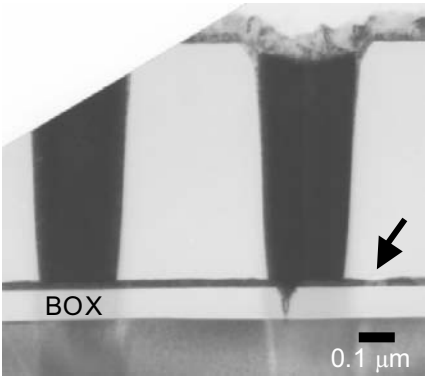


Fig. 2.29 TEM image of a leakage point in the BOX. The substrate is a SIMOX wafer and conventional Co salicidation was used. The arrow indicates local thinning.

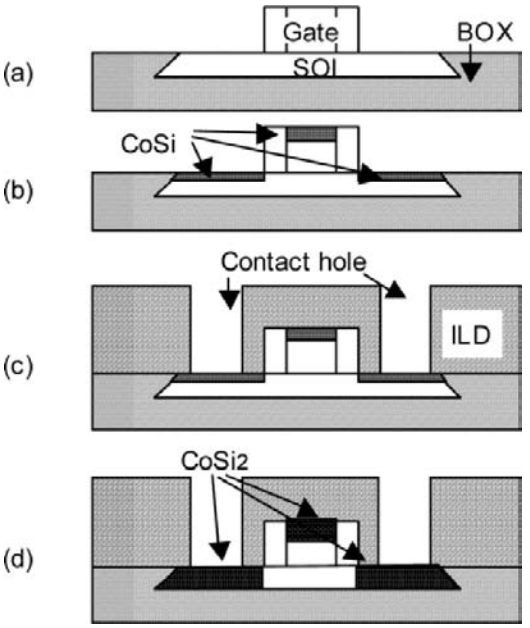


Fig. 2.30 Steps in the CHEPSA Co salicide process: (a) initial state; (b) deposition of Co, first rapid thermal annealing (RTA) and wet stripping; (c) deposition of interlayer dielectric (ILD) and etching of contact holes; and (d) second RTA for salicidation.

The distribution of the BOX leakage current for conventional and CHEPSA Co salicide processes is shown in Fig. 2.31. The current was measured on an SOI island with an area of 1 mm^2 containing 400,000 contacts. The excellent BOX leakage characteristics for CHEPSA are due to the fact that the silicide surface is flat when the contact holes are opened.

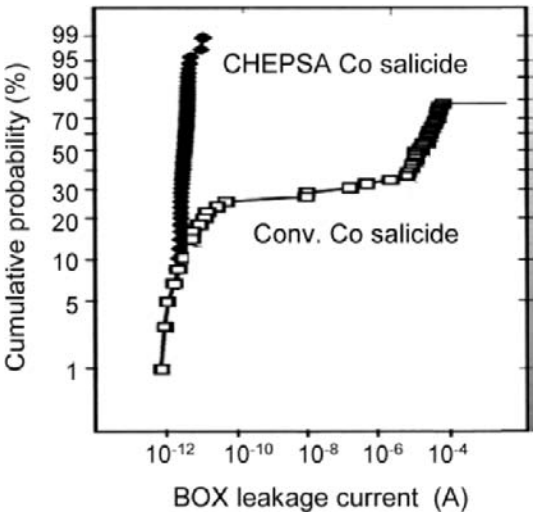


Fig. 2.31 Distribution of BOX leakage current for CHEPSA and conventional salicide processes. (T_{SOI} = 46 nm)

The sheet resistance (R_S) of Co salicide over a patterned n+ diffusion layer is shown in Fig. 2.32, with the thickness of the SOI layer under the gate electrode as a parameter. The SOI layer is about 7 nm thinner in the S/D regions than under the gate electrode. The data show that R_S is low enough in the S/D regions when T_{SOI} is 30 nm or more, and that it is too high when t_{SOI} is 25 nm. The high values are attributable to the CoSi that remains after the 2nd RTA because there is not enough Si to form $CoSi_2$. These results indicate that CHEPSA solves the problem of BOX leakage and that the S/D sheet resistance is not an issue if a 40-nm-thick SOI layer is used.

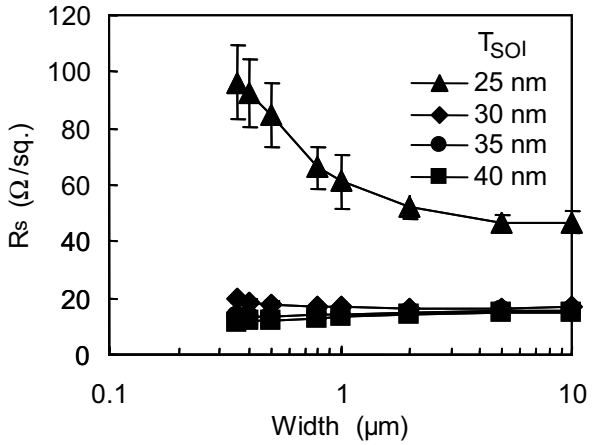


Fig. 2.32 Sheet resistance (Rs) of Co salicide over patterned n+ diffusion layer, with T_{SOI} as a parameter.

D. High S/D sheet resistance

The previous section showed that the sheet resistance of the S/D regions can be made low enough for SOI layer thicknesses down to 30 nm by optimizing the salicidation conditions (Fig. 2.32). However, when T_{SOI} is less than 30 nm, it is difficult to reduce it because there is insufficient Si to make disilicide. One solution is the selective epitaxial growth (SEG) of Si on the S/D regions [2.53], which is called the elevated-S/D process.

SEG is performed as follows: After fabrication of the structure shown in Fig. 2.20 Step 5, RCA cleaning with an HF dip is performed. Next, the wafers are loaded into an LP-CVD reactor and subjected to an H_2 bake to remove the native oxide on the SOI layer. Finally, Si film is selectively deposited using a continuous supply of SiH_2Cl_2, HCl, and H_2 gases.

Figure 2.33 shows SEM photographs of the active-Si region (SOI island) after SEG on a 30-nm-thick SOI layer at 800°C for three H_2 baking temperatures between 830°C and 930°C. When the baking temperature is 880°C or more, the Si agglomerates; and when it is 830°C, there is no agglomeration, but the surface of the film is rough. Furthermore, when it is below 800°C, no Si is deposited.

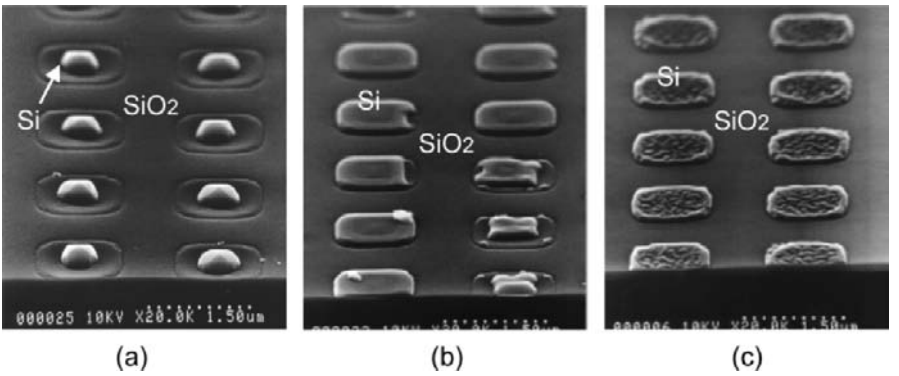


Fig. 2.33 SEM photograph of active-region patterns after SEG at 800°C for H_2 baking at (a) 930°C, (b) 880°C and (c) 830°C. (T_{SOI} = 30 nm.)

The cross-sectional TEM photograph in Fig. 2.34(a) of the SOI layer just before SEG shows that an amorphous layer extends down to a depth of 3 nm from the surface. A SIMS analysis revealed that this layer contains a great deal of carbon and cannot be removed by H_2 baking. The carbon is probably incorporated during sidewall etching, and it prevents SEG after H_2 baking at a low temperature. Removal of this carbon-contaminated layer by pretreatment with CF_4 and O_2 plasma enables SEG, even after H_2 baking at a temperature as low as 800°C , as shown in Fig. 2.34(b).

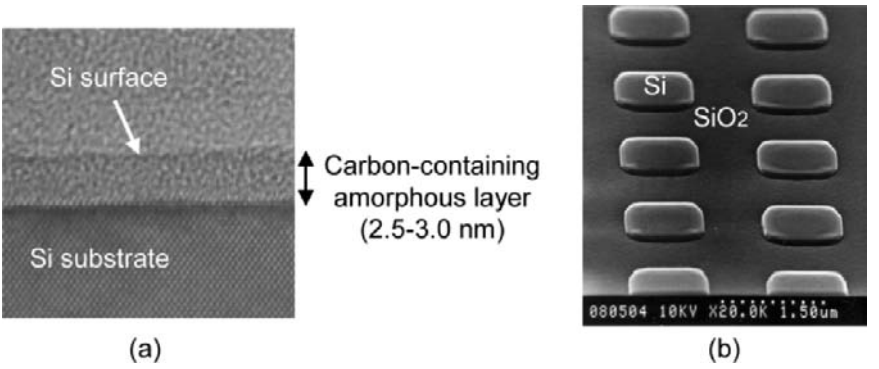


Fig. 2.34 (a) Cross-sectional TEM photograph of surface amorphous layer containing high concentration of carbon, and (b) SEM photograph of active-region patterns after removal of carbon-contaminated layer, H_2 baking at 800°C, and SEG.

However, if T_{SOI} is less than 30 nm, agglomeration cannot be prevented when the H_2 baking temperature is 800°C. Figure 2.35 shows how the length (L_{agg}) of the agglomeration region varies with T_{SOI}, with the temperature used for epitaxy as a parameter. Lagg is defined to be the amount of shrinkage at the edge of an SOI island during epitaxy. The data show that, for a given process temperature, there is a critical thickness above which epitaxial growth is stable. By reducing the temperature of the SEG process to 680°C, Si can be grown on an SOI layer as thin as 15 nm without agglomeration. However, since the growth rate of Si drops exponentially as the growth temperature becomes lower, it is also important to select proper gas sources for the epitaxy that provide a high growth rate.

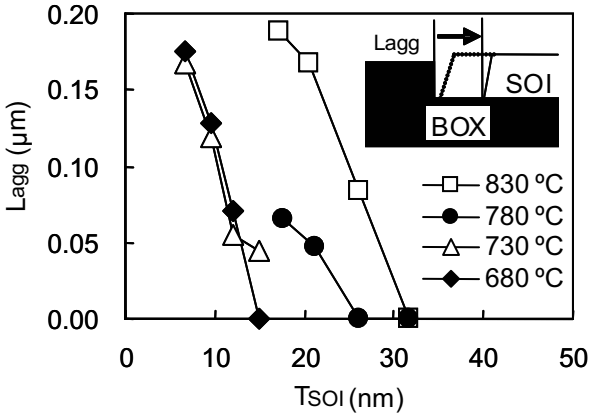


Fig. 2.35 Agglomeration length (L_{agg}) after SEG (as defined in inset) vs. T_{SOI}, with temperature used for SEG as a parameter.

The optimized SEG process was used to fabricate 0.15-μm FD-SOI MOSFETs. Figure 2.36 shows a cross-sectional TEM photograph of one taken before Co salicidation. A 40-nm-thick SEG film was formed on the SOI layer, which provides a channel thickness of 25 nm.

Figure 2.37 shows the dependence of R_s on T_{SOI} for two types of devices, one made with, and one made without, SEG. The SEG film was 40 nm thick, and Co silicide was formed on the S/D regions. Without SEG, Rs is 15 Ω/sq. when T_{SOI} is 30 nm or more; but it increases dramatically when T_{SOI} falls below that value. The use of SEG keeps Rs as low as about 6 Ω/sq., regardless of T_{SOI}.

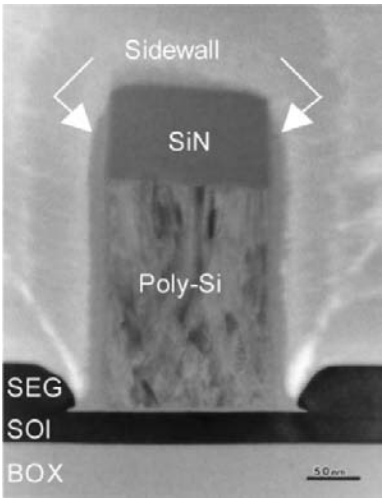


Fig. 2.36 Cross-sectional TEM photograph of a fabricated 0.15-μm FD-SOI MOSFET before Co salicidation. The SiN prevents SEG on the poly-Si gate.

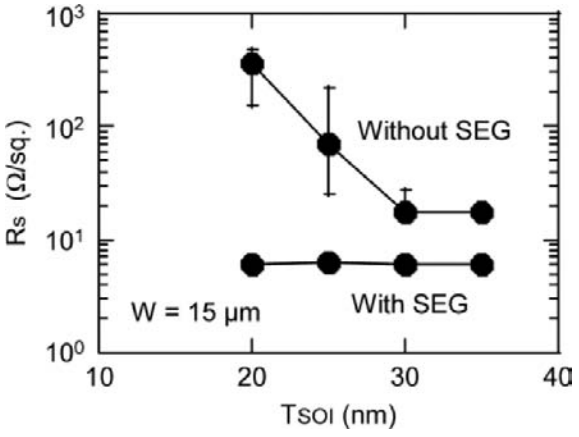


Fig. 2.37 Dependence of sheet resistance of S/D regions on thickness of SOI layer after Co salicidation. (T_{SEG} = 40 nm)

2.5 Summary

This chapter described FD-SOI devices and process technologies. First, the basic features of SOI devices were presented and compared with those of bulk devices; and the difference between the FD and PD operating modes was explained. In addition, the basic characteristics of FD- and PD-SOI MOSFETs (kink, subthreshold slope, floating-body effects, parasitic bipolar effects, self-heating effects) were discussed; and the advantages of FD-SOI over PD-SOI devices were pointed out. Then, the DC characteristics of FD-SOI MOSFETs were discussed in terms of the subthreshold and post-threshold currents. Finally, the typical FD-SOI CMOS fabrication process for the quarter-micron generation was explained; and problems with the process related to the thinness of the SOI layer of FD-SOI devices were discussed, along with some solutions.

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Chapter 3

ULTRALOW-POWER CIRCUIT DESIGN FOR FD-SOI DEVICES

3.1 Introduction

The use of mobile systems with communication functions has expanded rapidly in recent years. Considering the coming era of ubiquitous or pervasive network computing, the number and variety of mobile units is expected to increase much more. This type of equipment requires further miniaturization and longer battery life, and will eventually evolve into self-powered mobile systems. Maintenance-free systems without a battery would be ideal terminals for ubiquitous network computing.

Ultralow-power circuit design is essential to meet these requirements. For CMOS LSIs, which are the key components of mobile systems, lowering the supply voltage and the use of SOI devices are the most effective design approaches to reducing power dissipation. In this regard, multi-threshold (MT) CMOS/SOI circuits, which are suitable for supply voltages as low as 0.5 V, have already been developed [3.1], [3.2]. This circuit technology has been extended to LSIs for mobile equipment; and various digital and analog components (CPU, memory, analog/RF circuit, DC-DC converter) for ultralow-power mobile systems have been developed [3.3].

This chapter first describes the target application we will use as an example and the ultralow-power LSIs used make it, and explains the key to designing

this type of LSI. Second, ultralow-voltage circuit techniques for reducing the power dissipation of LSIs are examined. Finally, the reasons why FD-SOI devices are suitable for ultralow-voltage digital and analog/RF circuits are discussed.

3.2 Ultralow-Power Short-Range Wireless Systems

Figure 3.1 shows where the performance of our target application falls in relation to that of other types of applications. SOI devices are already being used in ultrahigh-speed and microwatt applications like servers and watches, but not in wireless mobile equipment like PDAs, which still have power dissipations ranging from 100 mW to 1 W. Our aim is to make the power dissipation about two orders of magnitude less than that of conventional LSIs; and our target application is a short-range wireless system. The LSIs for this system should operate at a speed of over 100 MHz and have a power dissipation from 1 to 10 mW. LSIs with these specifications will certainly be required for future mobile systems, such as fourth-generation (4G) wireless terminals; and they will pave the way to batteryless mobile systems.

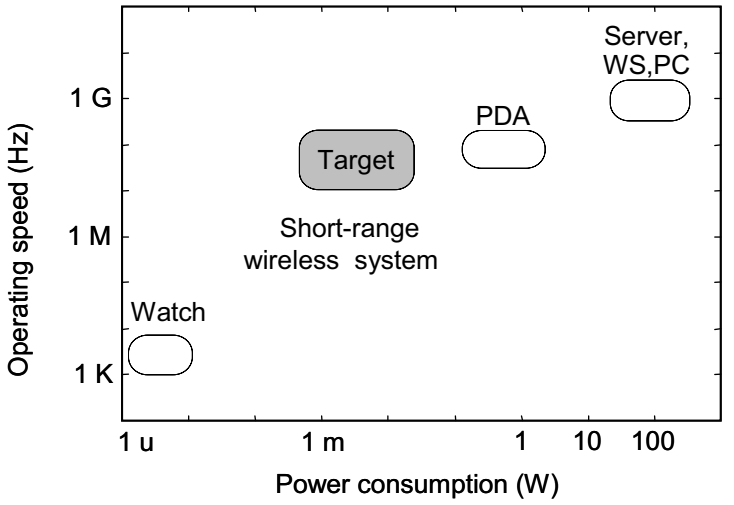


Fig. 3.1 Target application of ultralow-power LSIs.

Figure 3.2 shows the relationship between power consumption and the power generated by green-energy (GE) and ambient-energy sources, such as the light, kinetic, and thermal energy sources around us. The gray area is the region where a GE source can effectively be utilized. The maximum power it can generate is proportional to its size. GE sources are already being used in microwatt applications such as watches, but such devices cannot communicate wirelessly. Cellular phones are wireless communication tools, but they dissipate more power than can be generated by a GE source of the same size. To supply power to a cellular phone, a GE source would have to have an area larger than 5000 cm^2. What all this means is that self-powered wireless systems require ultralow-power circuit technology.

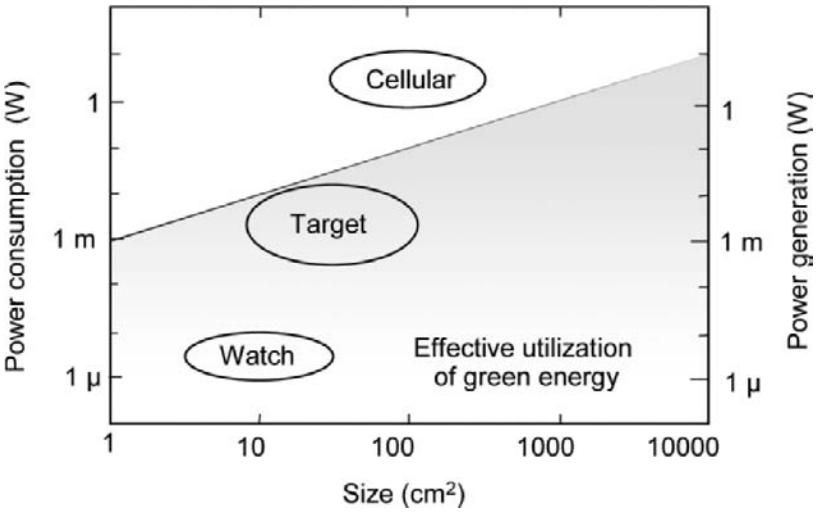


Fig. 3.2 Target application suitable for batteryless operation with green-energy sources.

Figure 3.3 shows a block diagram of a self-powered wireless system utilizing a GE or ambient-energy source. It consists of an analog/RF block for wireless signal processing, a digital signal processing block, and a DC-DC converter block for the energy source. To achieve ultralow-power operation, the DC-DC converter reduces the supply voltage down to 0.5 V for the digital block, and down to 0.5-1 V for the analog/RF block. The goal is a power dissipation of about 1 mW for the digital components and about 10 mW for the analog/RF ones.

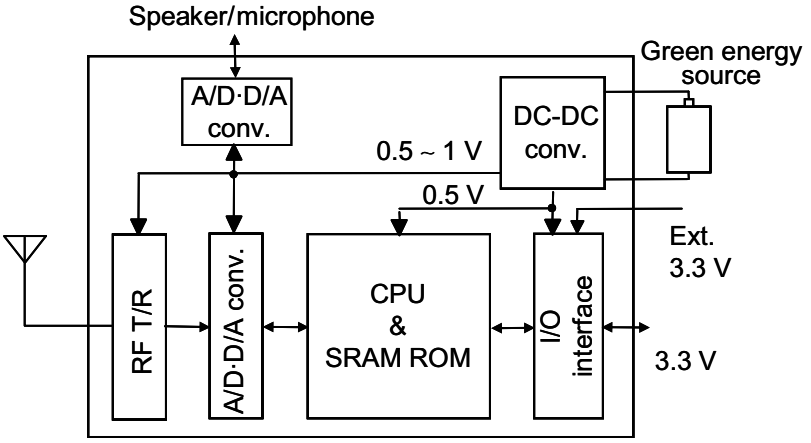


Fig. 3.3 Block diagram of ultralow-power short-range wireless system.

3.3 Key Design Factor for Ultralow-Power LSIs

Power efficiency is the most important factor in designing LSIs for mobile systems [3.4] because it determines battery life. If we plot power efficiency versus power dissipation (Fig. 3.4), then CPUs naturally fall into two groups. One is speed-oriented processors designed for speeds of over 1 GHz. These dissipate a great deal of power. The other is low-power-oriented processors designed with power efficiency in mind. They exhibit low power dissipation while providing adequate speed.

The power dissipation goal for a digital CPU is 1 mW. This would make the power efficiency about two orders of magnitude larger than that of conventional processors used in mobile equipment.

Just as for digital circuits, power efficiency is also the top priority for analog circuits. The goals for our ultralow-voltage ADC and RF chips are shown in Fig. 3.5.

The power efficiency of an analog circuit is

$$Power\ \ efficiency = \frac{(dynamic\ \ range) \times 2 \times bandwidth}{power\ \ dissipation}.$$

For an RF circuit, it is

$$Power\ \ efficiency = \frac{(Data\ \ rate) \times (transmission\ \ distance)^2}{power\ \ dissipation}.$$

Like CPUs, analog and RF chips can also be categorized into two groups, depending on whether they are oriented toward speed or low power. The target application is a short-range wireless system, such as a Bluetooth or an unlicensed radio band system; and the goal is to make the power efficiency about one or two orders of magnitude larger than that of conventional systems.

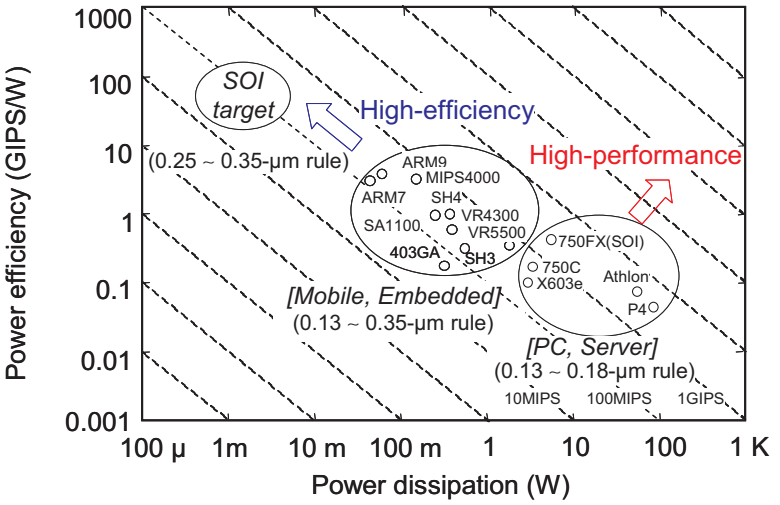
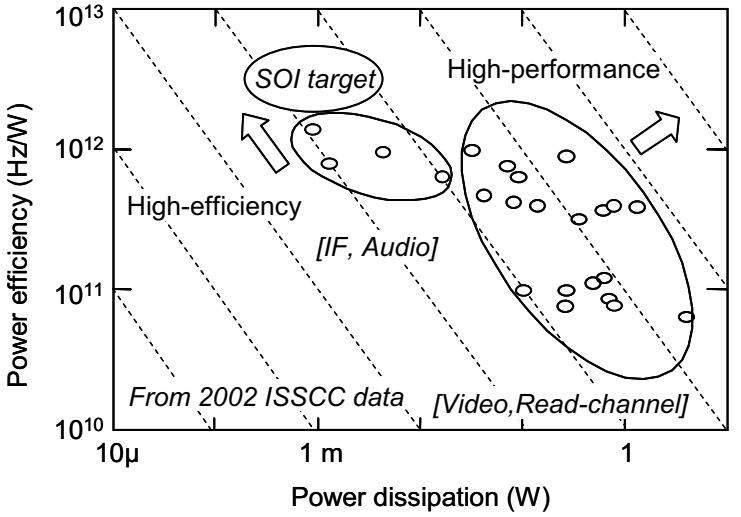
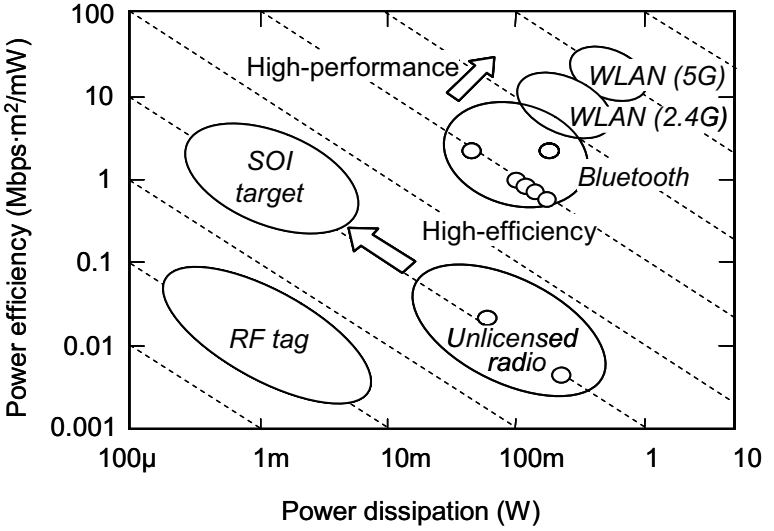


Fig. 3.4 Target performance of ultralow-voltage MTCMOS/SOI CPU.



(a)



(b)

Fig. 3.5 Target performance of ultralow-power analog circuits: (a) ADCs and (b) RF chips.

3.4 Ultralow-Voltage Digital-Circuit Design

3.4.1 Key Technologies

For ultralow-power LSIs in mobile wireless systems, the supply voltage must be lowered without diminution of the operating speed. This can be accomplished by reducing the threshold voltage of the MOSFETs. The power dissipation of CMOS circuits consists mainly of the dynamic power dissipation involved in charging and discharging the output capacitance, and the static power dissipation due to the subthreshold leakage current. The relationship between the two is shown in Fig. 3.6.

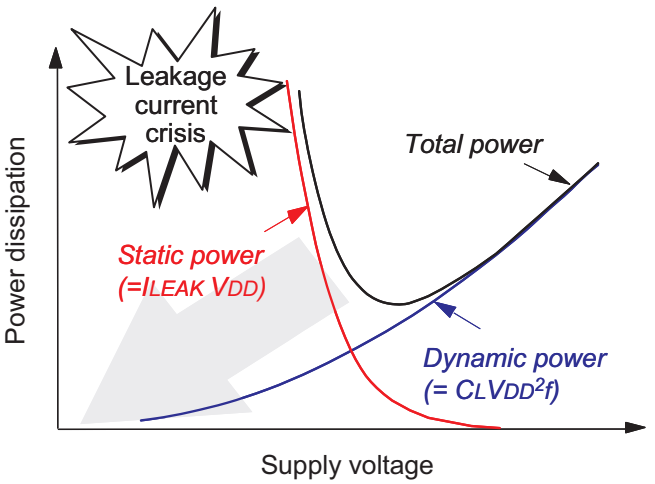


Fig. 3.6 Relationship between power dissipation and supply voltage in CMOS LSIs.

At larger supply voltages, the dynamic power dissipation is dominant; and the total power decreases in proportion to the square of the supply voltage. But when the supply voltage drops below a certain point, the threshold voltage of the MOSFETs must be set close to 0 V. This causes the static power dissipation due to the leakage current to increase exponentially; so the total power dissipation also increases. Hence, the suppression of the leakage current is the main issue in making ultralow-voltage LSIs.

There are two keys to suppressing the leakage current: fully-depleted (FD) SOI technology and MTCMOS/SOI technology [3.2]. Regarding the former, Figure 3.7 shows the structures of 0.25-μm FD-SOI MOSFETs. The gate oxide is 5 nm thick, and the buried oxide is 100 nm thick. The top silicon (SOI) layer is as thin as 50 nm, which is thinner than the surface depletion layer. The drain current family is shown in Fig. 3.8.

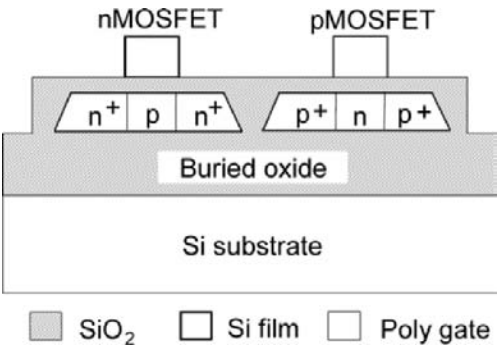


Fig. 3.7 Structure of fully-depleted (FD) SOI MOSFETs.

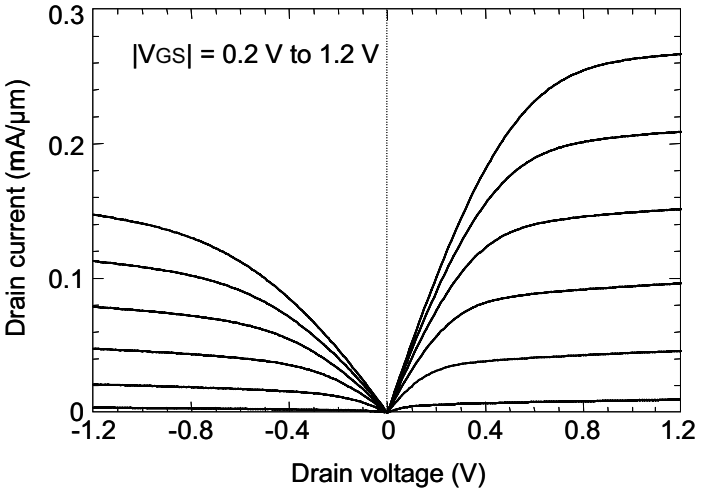


Fig. 3.8 Drain current-voltage characteristics of 0.25-μm FD-SOI MOSFETs.

Even though the devices do not have body terminals, the drain currents are smooth and there is no kink, as is observed in partially-depleted SOI MOSFETs [3.4].

FD MOSFETs have two important features that help suppress the leakage current at low supply voltages: They are three terminal devices and they have a steep subthreshold slope. Figure 3.9 illustrates layout patterns for an SRAM cell. Since FD MOSFETs do not have a well or a fourth body terminal, as bulk devices do, the isolation for n- and p-MOSFETs is smaller and the layout occupies about 30% less area than that for bulk devices. The small layout area, or in other words, the small output load capacitance, helps to maintain the current drivability at ultralow supply voltages. This means that the threshold voltage does not have to be reduced excessively, which helps suppress the leakage current.

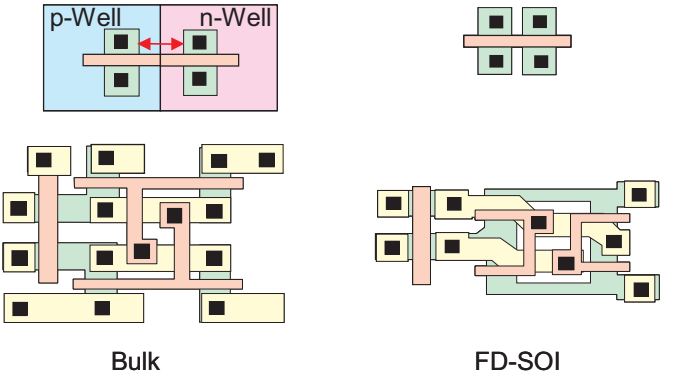


Fig. 3.9 Layout areas for bulk and FD-SOI devices.

The ID-VG characteristics of FD-SOI MOSFETs (Fig. 3.10) exhibit a small subthreshold swing close to the ideal value of 60 mV/decade [3.4]. This is because, owing to the thin SOI layer and the thick buried oxide, the depletion capacitance in the channel region is too small to affect the surface potential, and because the subthreshold current acts as a bipolar current. This allows the threshold voltage to be reduced without any increase in the leakage current, thereby making operation at ultralow voltages possible.

In addition to measures taken at the device level, there is also one that can be taken at the circuit level, namely, the use of MTCMOS/SOI circuits, which are composed of low-, medium-, and high-V_{th} MOSFETs (Fig. 3.11). The medium-V_{th} CMOS blocks are used for noncritical paths, thereby suppressing the leakage current in the active mode; and the high-V_{th} power-switch transistor reduces the leakage current in the sleep mode.

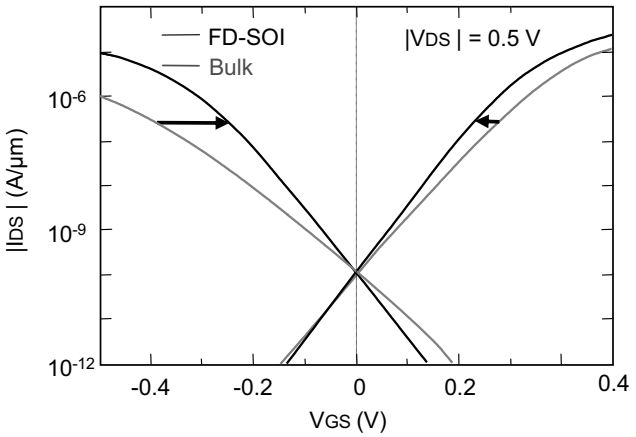


Fig. 3.10 I_D-V_G characteristics of 0.25-μm FD-SOI MOSFETs.

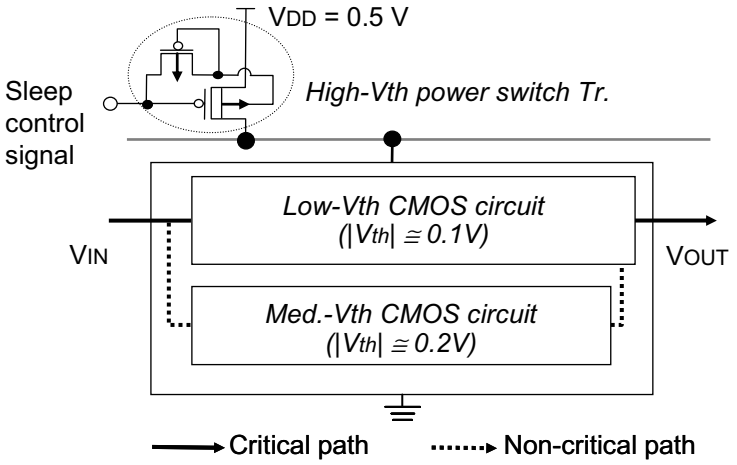


Fig. 3.11 MTCMOS/SOI circuit scheme.

3.4.2 Estimation of Energy Reduction

This section explains the model used to estimate how much various circuit techniques reduce the energy at an ultralow supply voltage under constant speed conditions.

(1) Estimation model
The energy dissipated by an MTCMOS/SOI circuit, including that dissipated during the sleep period, is given by

$$E = t_{act} \times P_{act} + t_{sleep} \times P_{sleep}, \tag{3.1}$$

where t_{act} (t_{sleep}) is the duration of operation in the active (sleep) mode, and P_{act} (P_{sleep}) is the corresponding power dissipation.

The power dissipation of an MTCMOS/SOI circuit in the active mode is given by

$$P_{act} = \kappa N C_{eff} V_{DD}^2 \left(\frac{1}{L_D t_{pd}} \right) + \beta N I_0 10^{-\frac{V_{th}}{S}} V_{DD}, \tag{3.2}$$

N: Number of gates
κ: Activity factor of a gate
C_{eff}: Average output capacitance per gate
L_D: Logic depth
I_0: Leakage current per gate at the threshold voltage
S: Subthreshold swing
β: Ratio of number of low-V_{th} MOSFETs to number of medium-V_{th} MOSFETS

This formula does not include the leakage current of medium-V_{th} MOSFETs because their threshold voltage is set to a high level, which makes the leakage current two orders of magnitude lower than that of the low-V_{th} MOSFETs.

The power dissipation of an MTCMOS/SOI circuit in the sleep mode is

$$P_{sleep} = \delta N I_0 10^{-\frac{V_{th(H)}}{S}} V_{DD}, \tag{3.3}$$

where δ is the ratio of the channel width of the power-switch transistors to that of the low- and medium-V_{th} MOSFETs, and $V_{th(H)}$ is the threshold voltage of the high-Vth MOSFETs.

The delay time of an MTCMOS/SOI circuit is

$$t_{pd} = \left(\frac{1}{2} - \frac{1 - V_{th}/V_{DD}}{1+\alpha} \right) t_T + \frac{1}{2} \frac{C_{eff} V_{DD}}{I_D} \ , \tag{3.4}$$

where

$$t_T = \left(\frac{0.9}{0.8} + \frac{V_{D0}}{0.8 V_{DD}} \ln \frac{V_{D0}}{e V_{DD}} \right) \frac{C_{eff} V_{DD}}{I_D} \tag{3.5}$$

and

$$I_D = I_{D0} \left(\frac{V_{DD}/V_{DD0} - V_{th}/V_{DD0}}{1 - V_{th0}/V_{DD0}} \right)^{\alpha} . \tag{3.6}$$

The first term in (3.4) depends on the input waveform, and is proportional to the input-waveform transition time (t_T) of the CMOS circuit [3.5]. The second depends on the output capacitance (C_{eff}) and is the time needed to charge it. I_D is the saturation current; and α is the velocity saturation index, which is related to the carrier mobility. I_{D0} is the saturation current normalized to a supply voltage of V_{DD0} and a threshold voltage of V_{th0}.

Equispeed lines in the supply voltage-threshold voltage plane can be calculated from the delay time formulae (3.4)-(3.6) [3.6]. Figure 3.12 shows some results for MOSFETs with a velocity saturation index (α) of 1.4. The delay-time parameter (λ) is normalized to a supply voltage of 2 V (V_{DD0} = 2 V) and a threshold voltage of 0.4 V. Equispeed lines calculated without taking the input-waveform transition time into account are also shown for comparison [3.7].

When the input-waveform transition time is taken into account, the equispeed lines are lower when the threshold voltage is below about 0.2 V. This means that reducing the threshold voltage has a much larger effect on the delay time

related to the input-waveform transition time than on that related to the output capacitance. This is because the improvement of the former is affected by both the threshold voltage and the saturation current, which is determined by the threshold voltage in (3.4) and (3.5); but that of the latter is due only to the saturation current.

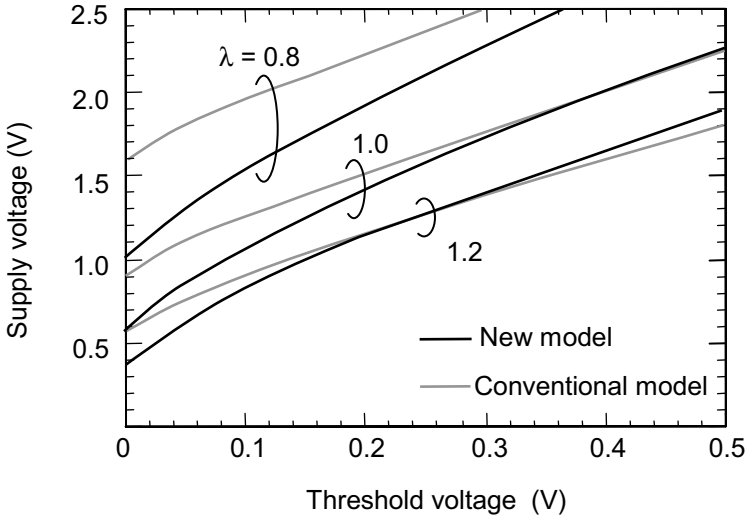
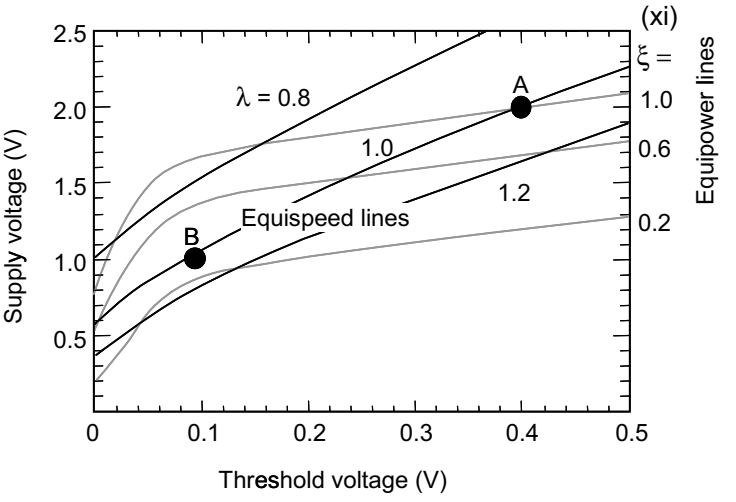
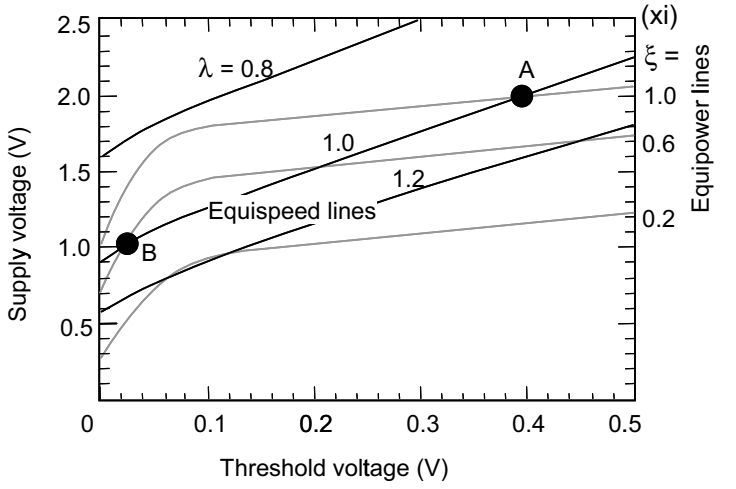


Fig. 3.12 Equispeed lines for a CMOS circuit based on a new model that takes the input-waveform transition time into account and a conventional model that does not, for three delay-time parameters (λ).

Equipower lines in the supply voltage-threshold voltage plane can also be calculated for an MTCMOS/SOI circuit from (3.1)-(3.6). As an example, Fig. 3.13 shows data for a CMOS/SOI circuit that has only an active mode and single-V_{th} MOSFETs [$\beta = 1$ in (3.2)]. The parameters related to the LSI scheme are assumed to be $\kappa = 0.1$ and $L_D = 30$. The power-dissipation parameter (ξ) is also normalized to a supply voltage of 2 V and a threshold voltage of 0.4 V.



(a)



(b)

Fig. 3.13 V_{DD} vs. V_{th} design space for evaluating power dissipation of CMOS LSIs under constant-speed conditions based on (a) evaluation model that includes the slew rate and (b) the conventional model.

The lines based on a model that includes the slew rate show that, if we reduce the supply voltage from 2 V to 1 V and set the threshold voltage to 0.1 V, then for a given delay time the power dissipation is one-fourth of that of a 2-V circuit. On the other hand, for the conventional model, the power dissipation can only be reduced by 45% of that of a 2-V circuit because the threshold voltage on the equispeed line is close to 0 V.

(2) Evaluation

By using a graph with equispeed and equipower lines in the supply voltage-threshold voltage plane, we can determine the optimum supply voltage, which is the one that provides the smallest energy dissipation for a given speed. This gives us a way of estimating the energy reduction provided by various circuit techniques. Figure 3.14 shows the dependence of energy dissipation on supply voltage for several schemes, with the energy dissipation being normalized by the minimum energy dissipation of a conventional CMOS circuit. For a delay time parameter (λ) of 1.5, which is normalized by the delay time at a supply voltage of 2 V and a threshold voltage of 0.4 V, the optimum supply voltage of a conventional bulk CMOS circuit is 1.05 V and the optimum threshold voltage is 0.25 V.

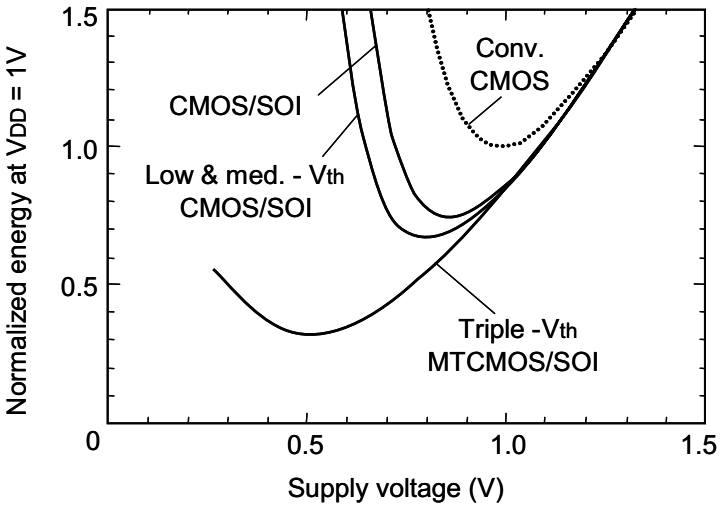


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Fig. 3.14 Energy reduction possible with FD-SOI technology

The figure shows that a single-V_{th} CMOS/SOI circuit composed of FD-MOSFETs dissipates 25% less power than a conventional CMOS circuit if we reduce the supply voltage from 1 V to 0.85 V and the threshold voltage from 0.25 V to 0.2 V. In addition, a dual-V_{th} CMOS circuit with low- and medium-V_{th} MOSFETs dissipates over 10% less power than a single-V_{th} CMOS/SOI circuit at a supply voltage of 0.8 V and a threshold voltage of 0.17 V. Moreover, an MTCMOS circuit dissipates over 35% less power than a dual-V_{th} CMOS circuit at a supply voltage of 0.5 V and a threshold voltage of 80 mV. In short, at a supply voltage of 0.5 V, an MTCMOS circuit dissipates less than half the power of a conventional CMOS circuit.

3.5 Robustness of Ultralow-Voltage Operation

MTCMOS/SOI circuits are more robust than CMOS circuits at supply voltages below 1 V. One reason is that floating-body effects are suppressed when the supply voltage is very low. Another is that variations in the delay time of a CMOS circuit are suppressed over a wide range of operating temperatures at ultralow supply voltages [3.8]. This section describes the characteristics in detail.

3.5.1 Suppression of Floating-Body Effects

When a large voltage of over 1 V is applied to an FD-SOI MOSFET, parasitic bipolar action due to impact ionization near the drain terminal occurs and the potential of the floating-body part increases. This lowers the threshold voltage of an MTCMOS circuit, which in turn shortens the delay time. Since parasitic bipolar action intensifies at low operating frequencies, delay time depends on operating frequency. Special techniques are usually needed to suppress this action, such as Ar ion implantation into the source and drain regions [3.9] to create recombination centers; but ultralow voltages obviate the need for such measures.

Confirmation of this idea comes from CMOS logic gates fabricated on a 0.25-μm CMOS/SIMOX process. The dependence of delay time on operating frequency for supply voltages of 0.5 V and 1 V (Fig. 3.15) reveals no parasitic bipolar effects; that is, the delay time is constant regardless of operating frequency.

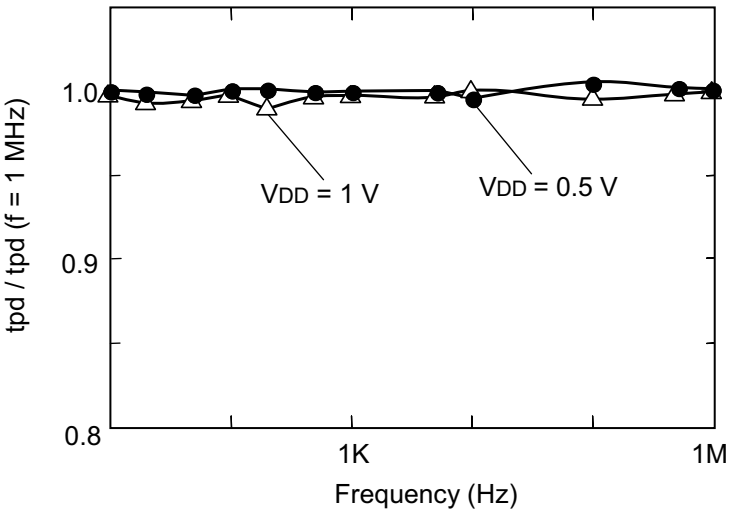


Fig. 3.15 Delay time vs. operating frequency of FD CMOS/SOI circuits at supply voltages of 0.5 V and 1 V.

3.5.2 Suppression of Threshold-Voltage Fluctuations due to Operating Temperature

Another advantage of FD-SOI MOSFETs is that the threshold voltage varies little with operating temperature. One factor influencing the threshold voltage is the depletion charge. It is determined by the thickness of the SOI layer, and the operating temperature has little effect on it.

For bulk devices, the threshold voltage is

$$V_{th} = -\Phi_{MS} + \phi_f + Q_B / C_{OX}, \tag{3.7}$$

where

$$Q_B = \sqrt{2\varepsilon_{si} q N_D (2\phi_f)}, \tag{3.8}$$

T is operating temperature, Φ_{MS} is the difference in work function between a metal and a semiconductor, ϕ_f is the Fermi potential, C_{OX} is the gate oxide capacitance, and N_D is the doping concentration.

The change in V_{th} with operating temperature *(dVth/dT)* is then given by

$$\frac{dV_{th}}{dT} \cong \frac{d\phi_f}{dT}\left(1+\frac{1}{C_{OX}}\left(\frac{2\varepsilon_{si} q N_D}{2\phi_f}\right)^{\frac{1}{2}}\right). \tag{3.9}$$

Since $d\phi_f/d_T$ is negative, the threshold voltage drops as the temperature rises.

For FD-SOI devices, the depletion charge (Q_B) is determined by the thickness of the SOI layer and is constant regardless of operating temperature. So, the change in threshold voltage becomes

$$\frac{dV_{th}}{dT} \cong \frac{d\phi_f}{dT}. \tag{3.10}$$

This means that the change in threshold voltage with operating temperature is smaller in FD-SOI MOSFETS than in bulk devices. Table 3.1 lists the threshold voltage characteristics of 0.25-μm MOSFETs. Notice that the change in threshold voltage for FD-SOI devices is about half that for bulk ones.

Table 3.1 Threshold-voltage characteristics of 0.25-μm MOSFETs.

	SOI		BULK			
	Dual-poly		Dual-poly		Single-poly	
	n	p	n	p	n	p
|ΔVth| (mV/°C)	0.60	0.55	0.99	0.94	0.99	2.05
S (mV/decade)	70	73	78	80	78	100
ΔS (mV/decade/°C)	0.24	0.24	0.34	0.31	0.34	0.45

Figure 3.16 shows the dependence of normalized delay time on operating temperature for a circuit fabricated on a 0.25-μm CMOS/SIMOX process, and also for a circuit fabricated on a bulk CMOS process with the same design rule for comparison. FD-MOSFETs exhibit flat delay-time characteristics, while the delay time of bulk devices increases a great deal as the operating temperature drops due to a large increase in the threshold voltage.

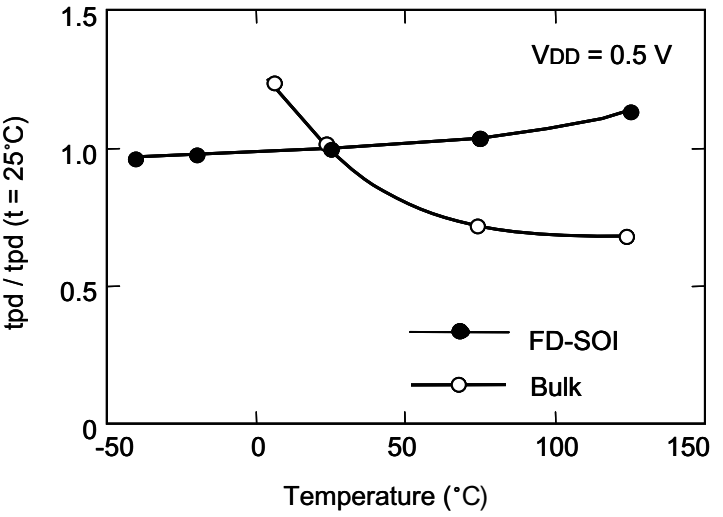


Fig. 3.16 Normalized delay time of basic logic gate vs. operating temperature.

3.6 Prospects and Issues in Low-Voltage Analog Circuits

3.6.1 Prospects

Analog circuits generally require higher operating voltages than digital ones. However, there is a strong demand for low-voltage analog circuits to reduce the power consumption of battery-operated equipment and to satisfy the requirements of scaled-down devices [3.10].

Battery operation requires a low voltage, such as 0.9 V for a single dry cell. A silver oxide cell and a zinc-air cell, which are small dry cells suitable for small portable equipment such as pagers and medical monitors, produce voltages of 1.55 V and 1.4 V, respectively. A DC/DC converter can boost the battery voltage, but the low conversion efficiency and large area and volume make it poorly suited to portable equipment. Furthermore, devices for ubiquitous networking and wearable electronic devices of the future will have to be small. So, analog circuits that run on the low voltage supplied by one small dry cell will be needed in the coming era of ubiquitous networking.

The scaling down of devices is a very effective way to boost speed while reducing both operating current and the area occupied. This necessitates low-voltage operation, which is extremely important in maintaining the progress in circuit performance, even for analog circuits.

3.6.2 Issues

Lowering the voltage is an effective way to reduce power consumption in both analog and digital circuits and is required for scaled-down devices. However, this can cause problems in analog circuits, such as a narrower dynamic range and poorer performance. Furthermore, the circuit topology must be changed to address the issue of narrow head room; and this often results in an increase in operating current. So, lowering the voltage does not always lead to lower power consumption in analog circuits.

The main problems with lowering the voltage of analog circuits are the narrower dynamic range of signals and the smaller circuit head room. The dynamic range becomes narrower as the voltage is reduced. The power (S_p) of a sinusoidal signal with a swing of V_{pp} is

$$S_p = \frac{V_{pp}^2}{8}. \tag{3.11}$$

On the other hand, the noise power (N_p) for a load capacitance of C is

$$N_p = \gamma \frac{kT}{C}, \tag{3.12}$$

where γ is the excess noise coefficient. Therefore, the signal-to-noise ratio (SNR) is

$$SNR = \frac{CV_{pp}^2}{8\gamma kT}. \tag{3.13}$$

A differential circuit has twice the signal swing and twice the number of noise sources, yielding

$$SNR_{diff} = \frac{CV_{pp}^2}{4\gamma kT}. \tag{3.14}$$

So, the capacitance of a differential circuit needed to obtain the target SNR for a given signal swing is

$$C = \frac{4\gamma kT \cdot SNR_{diff}}{V_{pp}^2}. \tag{3.15}$$

Fig. 3.17 shows needed capacitance as a function of SNR for several signal swings at a temperature of 500 K and a γ of 1 [3.11]. The capacitance increases rapidly as the voltage drops. For example, a signal swing of 5 V requires a capacitance of only 0.1 pF to yield an SNR of 80 dB, while a signal swing of 0.5 V requires 10 pF. A larger capacitance results in a higher operating current.

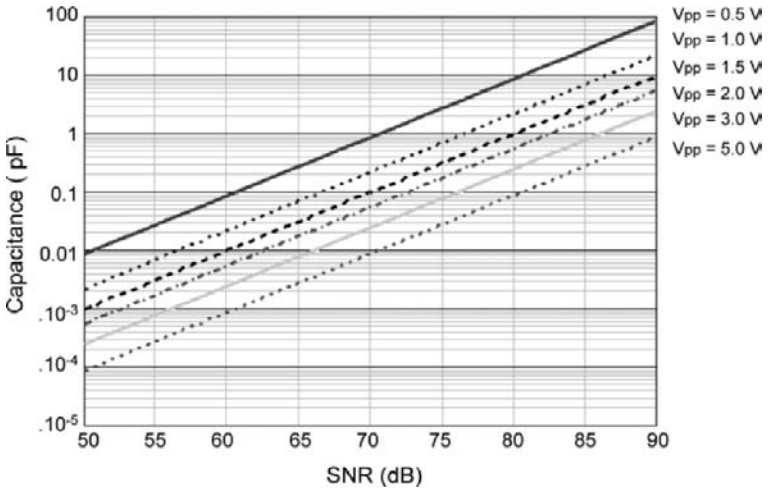


Fig. 3.17 Needed capacitance vs. SNR for several signal swings. (T = 500 K, $\gamma = 1$)

For a single stage amplifier, the gain-bandwidth product (GBW) for a load capacitance of C is

$$GBW = \frac{g_m}{2\pi C} = \frac{I_{sink}}{2\pi C V_{eff}}, \tag{3.16}$$

where gm is transconductance, Isink is the sink current, and V_{eff} is the effective gate voltage ($V_{eff} = V_{GS}-V_{th}$). We can write I_{sink} in terms of SNR_{diff}, GBW, and V_{pp} as

$$I_{sink} = \frac{8\gamma\pi kT \cdot V_{eff} \cdot SNR_{diff} \cdot GBW}{V_{pp}^2}. \tag{3.17}$$

In other words, the operating current of the amplifier is proportional to the product of SNR_{diff} and GBW and inversely proportional to the square of the signal swing.

The power consumption (P_d) is

$$P_d = V_{DD} \cdot I_{sink} = 8\gamma\pi kT \cdot V_{eff} \frac{V_{DD}}{V_{pp}^2} \cdot SNR_{diff} \cdot GBW \,. \tag{3.18}$$

It is approximately given by

$$P_d \approx 8\gamma\pi kT \cdot V_{eff} \cdot \frac{SNR_{diff} \cdot GBW}{V_{DD}} \,. \tag{3.19}$$

So, lowering the voltage of an analog circuit does not always reduce the power consumption. The results are similar for many types of analog circuits.

Another problem with analog/RF circuits is the increase in phase noise. The minimum phase noise of a CMOS LC oscillator (L_{min}) is

$$L_{min}(f_m) = kT \frac{\gamma}{V_{DD}} \frac{\pi f_0 L}{Q} \left(\frac{1}{V_{DD}} + \frac{2}{V_{eff}} \right) \left(\frac{f_o}{f_m} \right)^2 , \tag{3.20}$$

where f_o is oscillation frequency, fm is offset frequency, L is inductance, and Q is the quality factor [3.12]. This equation tells us that phase noise is inversely proportional to the square of the operating voltage. This is because the noise power is determined by Q, and the signal swing is proportional to V_{DD}. So, the phase noise increases as V_{DD} decreases.

3.7 Technology Scaling, Analog Performance, and Performance Trend for Electrical Systems

Technology scaling increases analog performance, but it also gives rise to serious problems. However, electrical systems have followed this trend and many of the problems have been solved.

3.7.1 Technology Scaling and Analog Performance

Fig. 3.18 shows the circuit schematic of a differential amplifier. We make the following assumptions: amplifiers are connected in series; the Miller effect is neglected; the required capacitance is much smaller than the load capacitance; and the load capacitance consists of the drain and gate capacitances of the next gain stage.

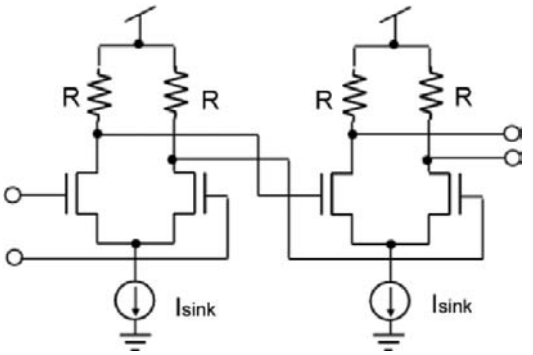


Fig. 3.18 Circuit diagram of differential amplifier.

Then, the gain-bandwidth product (GBW) of this amplifier is

$$GBW = \frac{g_m}{2\pi\left(WC_j + \frac{2}{3}C_{ox}LW\right)} = \frac{I_{sink}}{\pi\left(WC_j + \frac{2}{3}C_{ox}LW\right)V_{eff}}, \tag{3.21}$$

where W is gate width and L is gate length.

Since $I_{sink} = \frac{\mu C_{ox}}{2}\frac{W}{L}V_{eff}^2$ and $C_{ox} = \frac{\kappa}{L}$, (3.21) can be written as

$$GBW = \frac{\mu V_{eff}}{2\pi L^2\left(\frac{2}{3} + \frac{C_j}{k}\right)}, \tag{3.22}$$

which tells us that GBW is inversely proportional to the square of the gate length. (3.22) shows that devices must be scaled down further to increase GBW, if the required SNR is low enough.

Fig. 3.19 shows GBW as a function of design rule [3.13]. The GBW of state-of-the-art 0.18-μm devices is about eight times larger than that of 0.5-μm devices.

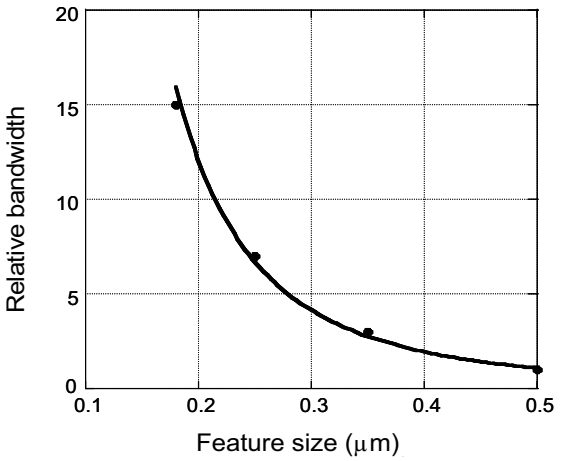


Fig. 3.19 GBW as a function of design rule.

3.7.2 Performance Trend of Electrical Systems

In wireless systems, which are one of the most important types of electrical systems, the bandwidth has been increasing and the required dynamic range has been decreasing. Table. 3.2 lists the signal bandwidth and phase noise of various wireless systems.

The acceptable phase noise has been increasing along with the bandwidth, except for narrow-band CDMA. Thus, in newer wireless systems, the gain bandwidth is larger and the required dynamic range is smaller. This trend matches the trend in device technology and shows the importance of low-voltage operation in analog circuits made with scaled-down devices.

Table 3.2 Signal bandwidth and phase noise of wireless systems.

Standard	Service year	Bandwidth	Phase noise
GSM	1992	200 kHz	-125.4
DECT	1992	1.728 MHz	-107.3
PDC	1993	32 kHz	-135.1
PHS	1995	300 kHz	-125.2
PCS	1995	30 kHz	-129.8
Bluetooth	1998	1 MHz	-104
N-CDMA	1998	1.25 MHz	-141
WLAN(11a)	1999	16.6 MHz	-111.2
WLAN(11b)	1999	11 MHz	-114.4
W-CDMA	2001	15 MHz	-115.8

3.8 Low-Voltage Analog Circuit

3.8.1 Basic Amplifier

The minimum operating voltage of an analog circuit is basically determined by the circuit topology, the transistor parameters, and the signal swing. For a basic non-inverting CMOS operational amplifier (Fig. 3.20), the minimum operating voltage (V_{DD_min}) is

$$V_{DD\_min} = V_{D\_sat1} + V_{D\_sat2} + V_{D\_sat3} + \left|V_{thp}\right| + V_{swing}, \qquad (3.23)$$

where V_{D_sat} is the minimum drain-source voltage needed to keep the transistor operating in the saturation region; a reasonable value is 0.15 V. For V_{D_sat} = 0.15 V, V_{thp} = 0.25 V, and V_{swing} = 0.4 V, V_{DD_min} is 1.1 V.

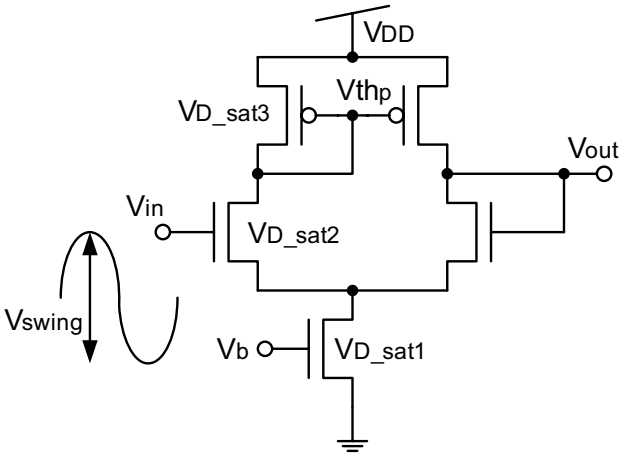


Fig. 3.20 Basic CMOS operational amplifier.

A differential inverting amplifier (Fig. 3.21) is suitable for low-voltage operation. Since the signal swing at the input terminals is almost zero, only the output signal swing must be taken into account. Furthermore, the effective signal swing can be doubled by using differential signals; and the SNR can be increased by making the swings of the single-ended signals the same.

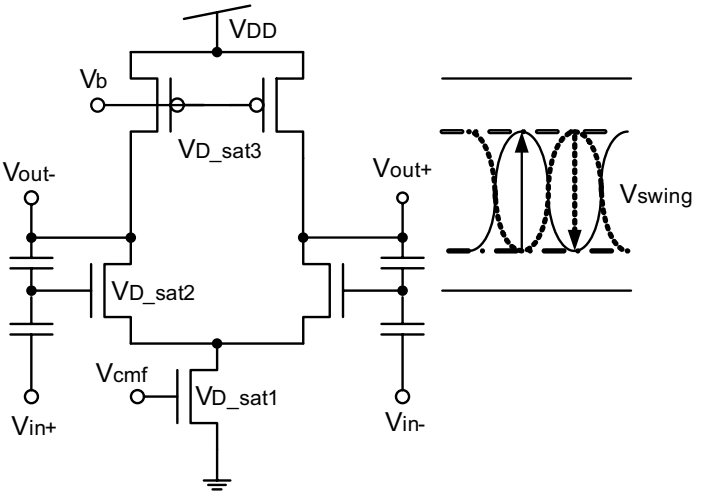


Fig. 3.21 CMOS differential inverting amplifier.

The minimum operating voltage (V_{DD}_min) is

$$V_{DD\_min} = V_{D\_sat1} + V_{D\_sat2} + V_{D\_sat3} + V_{O\_swing} . \quad (3.24)$$

A CMOS differential amplifier (Fig. 3.22) can be made using a folded cascode circuit. The minimum operating voltage (V_{DD}_min) is determined by the output nodes and is

$$V_{DD\_min} = V_{D\_satn1} + V_{D\_satn2} + V_{D\_satp1} + V_{D\_satp2} + V_{O\_swing} . \quad (3.25)$$

For V_{D_sat} = 0.15 V and V_{O_swing} = 0.4 V, V_{DD_min} is 1.0 V. The effective output voltage swing is as large as 0.8 V_{pp}, which is twice that of the single-ended circuit in Fig. 3.20.

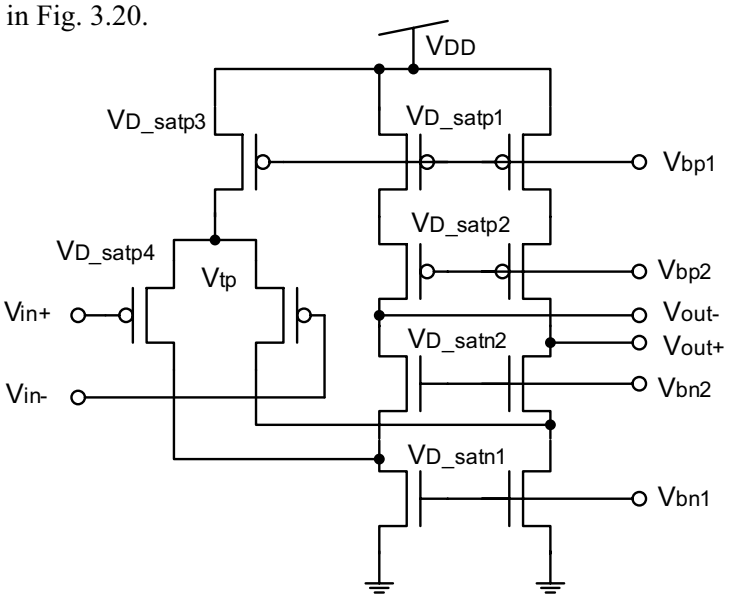


Fig. 3.22 CMOS differential amplifier using folded cascode circuit.

A two-stage amplifier (Fig. 3.23) can provide an even larger output swing. Again, the minimum operating voltage is determined by the output nodes and is

$$V_{DD\_min} = V_{D\_satn3} + V_{D\_satp5} + V_{O\_swing} . \quad (3.26)$$

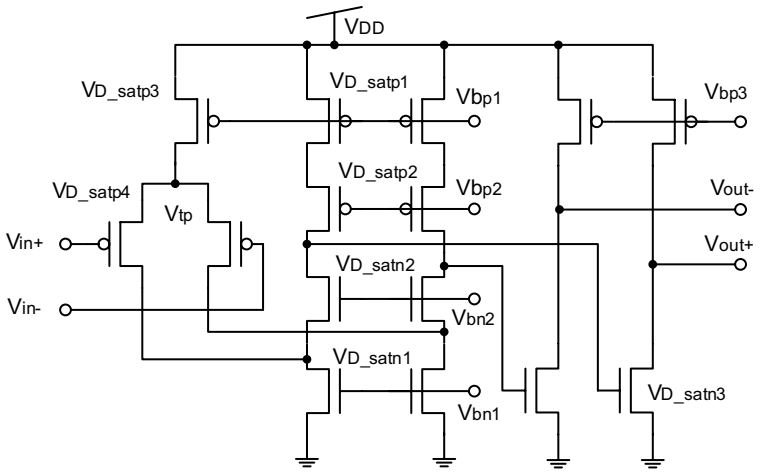


Fig. 3.23 Two-stage CMOS amplifier.

This circuit provides an output voltage swing as large as 1.4 V_{pp} in the differential mode at an operating voltage of 1.0 V. However, the gain-bandwidth product is smaller and the power consumption is larger than those of a single-stage amplifier.

3.8.2 Switches

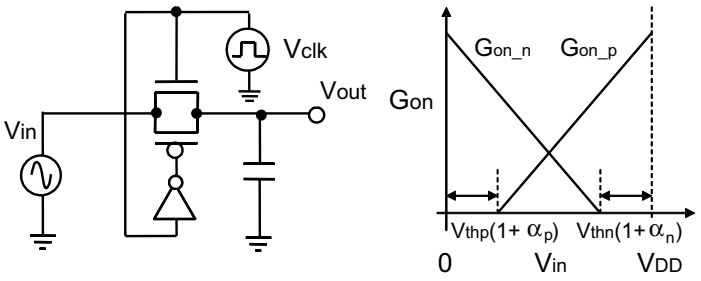
The rapid degradation in the performance of switches as the operating voltage becomes lower is a serious obstacle to reducing the voltage of analog circuits.

Figure 3.24 shows a CMOS sample-and-hold circuit and the on-conductance of a switch. The on-conductances of nMOS and pMOS switches are given by

$$G_{on\_n} = \mu_n C_{ox} \frac{W_n}{L_n}\left(V_{DD} - V_{in} - V_{thn}\left(1+\alpha_n\right)\right) \tag{3.27a}$$

$$G_{on\_p} = \mu_p C_{ox} \frac{W_p}{L_p}\left(V_{in} - \left|V_{thp}\left(1+\alpha_p\right)\right|\right), \tag{3.27b}$$

where α is the change in threshold voltage due to the back gate. As the input voltage increases, the on-conductance of an n-channel switch decreases and reaches zero at an input voltage of $V_{DD} - V_{thn}(1+\alpha_n)$. In contrast, that of a p-channel switch is zero at a low input voltage and rises as the input voltage increases above $V_{thp}(1+\alpha_p)$. Consequently, the total on-conductance decreases as the operating voltage drops. If V_{DD} is less than $V_{thn}(1+\alpha_n) + V_{thp}(1+\alpha_p)$, the switch cannot conduct.



(a) (b)

Fig. 3.24 Analog switch. (a) CMOS sample-and-hold circuit and (b) on-conductance of switch.

One solution to this problem is to use a bootstrap switch circuit (Fig. 3.25) [3.14]. A charged capacitance connects the gate and source of the switch transistor to keep the gate-to-source voltage constantly high, regardless of the input voltage.

This circuit exhibits a high on-conductance and a weak dependence on input voltage, which causes signal distortion. Even though it provides low-voltage operation, actual applications are limited to a sample-and-hold circuit because it occupies such a large area and consumes so much power. A simpler circuit needs to be developed.

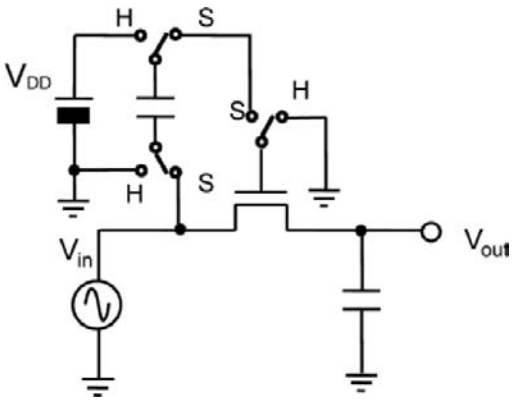


Fig. 3.25 Bootstrap switch circuit. (From A. M. Abo et al. [3.14]. ©1999 IEEE.)

3.8.3 Use of Passive Components

The use of passive components is often an effective way to reduce the operating voltage. The mixer circuit in Fig. 3.26 employs LC tanks instead of conventional current sources [3.15]. An LC tank can be regarded as a pure resistance at the resonance frequency and has a resistance of almost zero under a DC current. So, an LC tank enables the operating voltage to be made 0.2 V lower than that needed to sustain a current source.

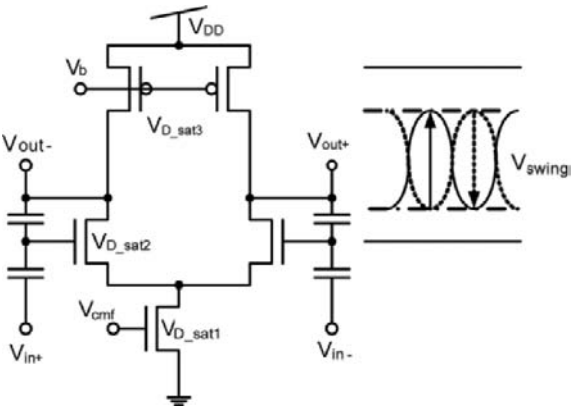


Fig. 3.26 Mixer circuit using LC tanks.

Thus, this mixer provides sub-1-V operation through the use of LC tanks. However, judicious use of LC tanks is recommended because they occupy a much larger area than current sources.

3.9 Fully-Depleted SOI Devices for Ultralow-Power Analog Circuits

Most analog circuits employ a combination of three basic analog functions [3.16]:

- Conversion from gate voltage to drain current (V-to-I). The coefficient is the transconductance (g_m).
- Conversion from drain current to drain voltage (I-to-V). The coefficient is the drain resistance (r_O).
- Conversion from gate-to-source voltage to drain-to-source conductance (V-to-G). The coefficient is the on-conductance (G_{on}).

This section first compares the DC characteristics of FD-SOI MOSFETs and bulk MOSFETs, and then describes the RF characteristics of MOSFETs and inductors made with FD-SOI technology.

3.9.1 Transconductance (g_m)

The ratio of transconductance to drain current (g_m/I_D) is a very important figure of merit for analog circuits. It occurs in the formula for the DC gain of a MOSFET:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{\Delta I_D}{g_{ds}} \cdot \frac{1}{\Delta V_{in}} = \frac{g_m}{g_{ds}} = \frac{g_m}{I_D} \cdot V_A , \tag{3.28}$$

where g_{ds} is the output drain conductance and V_A is the Early voltage [3.17].

This equation tells us that a larger gm/ID means a more efficient analog device. On the other hand, g_m/I_D for the two types of inversion is given by [3.18]:

Weak inversion: $$\frac{g_m}{I_D} = \frac{dI_D}{I_D \cdot dV_G} = \frac{ln(10)}{S} = \frac{q}{nkT} \tag{3.29a}$$

Strong inversion: $$\frac{g_m}{I_D} = \sqrt{\frac{2\mu C_{ox} W/L}{nI_D}}\,. \qquad (3.29b)$$

The factor n, which is related to the body coefficient, is a measure of the ideality of the coupling between the gate voltage and the surface potential and is also found in the formula for the subthreshold swing (S):

$$S = \frac{nkT}{q} \cdot ln(10) \qquad \text{(mV/dec).} \qquad (3.30)$$

Typical values of n range between 1.05 and 1.10 for FD-SOI MOSFETs and between 1.3 and 1.5 for bulk ones.

Figure 3.27 compares the measured g_m/I_D characteristics of FD-SOI and bulk devices, both of which have a gate length of 0.35 µm and a gate width of 10 µm; Table 3.3 lists the device parameters. The small body factor of FD-SOI devices provides a maximum g_m/I_D of about 34 V^{-1}, while the value is only 28 V^{-1} for bulk ones.

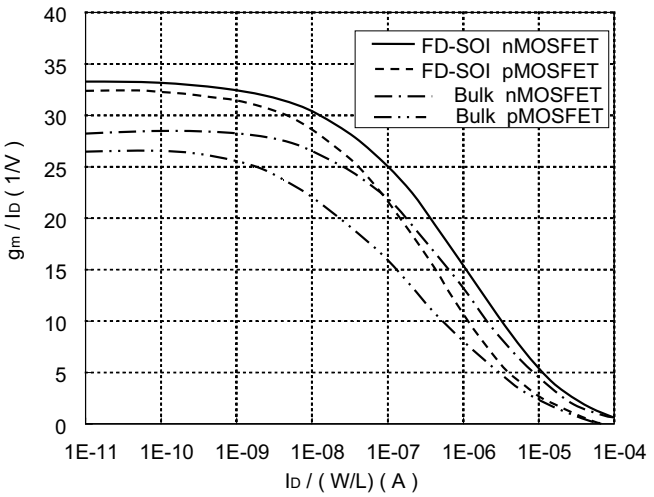
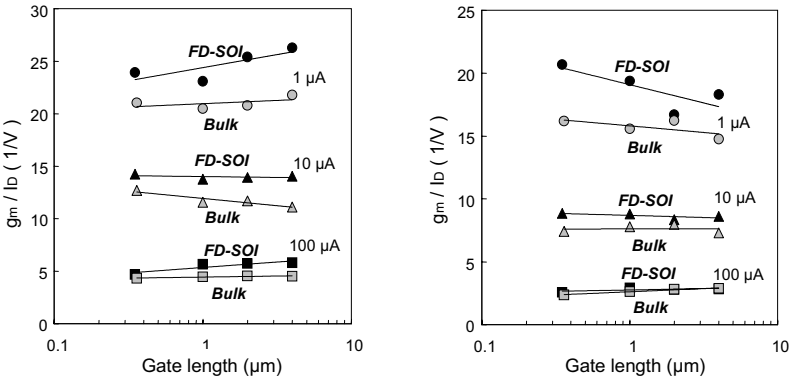


Fig. 3.27 g_m/I_D in saturation region (W = 10 µm, L = 0.35 µm).

Table 3.3 Parameters of bulk and FD-SOI MOSFETs.

	g_m/I_D	V_{th}	n
Bulk nMOS	28.8 V^{-1}	0.65 V	1.37
Bulk pMOS	26.5 V^{-1}	0.60 V	1.46
FD-SOI nMOS	33.3 V^{-1}	0.15 V	1.16
FD-SOI pMOS	32.4 V^{-1}	0.15 V	1.19

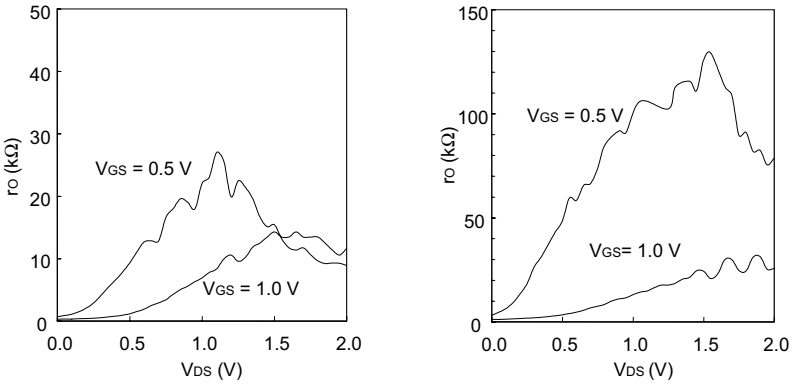
A graph of g_m/I_D versus gate length (Fig. 3.28) with current as a parameter shows that g_m/I_D is higher for FD-SOI than for bulk MOSFETs at all current levels. In this regard, it has been reported that partially-depleted SOI devices have low g_m/I_D [3.19]. These results demonstrate that FD-SOI devices are suitable for analog circuits.



(a) nMOSFET (b) pMOSFET

Fig. 3.28 g_m/I_D vs. gate length for 0.35-μm FD-SOI and bulk devices with current level as a parameter.

The r_O-V_{DS} characteristics (Fig. 3.29) of FD-SOI devices indicate that the output resistance is large enough. This is because there is no kink effect.



(a) nMOSFET (b) pMOSFET

Fig. 3.29 r_O characteristics of FD-SOI devices.

3.9.2 On-Conductance (Gon) of CMOS Analog Switch

A CMOS analog switch (Fig. 3.24(a)) is a key component of analog circuits, and is composed of nMOS and pMOS transistors connected in parallel. As mentioned before, the on-conductance of a switch decreases as the supply voltage drops. The minimum operating voltage (V_{DD_min}) can be expressed as a function of the threshold voltages (V_{th}) and body factors (n) of the n- and pMOSFETs [3.18]:

$$V_{DD\_min} = \frac{V_{thp} \cdot n_n + V_{thn} \cdot n_p}{n_n + n_p - n_n \cdot n_p}. \tag{3.31}$$

Figure 3.30 shows the measured on-conductance for a V_{DD} of 1 V. The gate width (W) was 10 μm for nMOSFETs and 30 μm for pMOSFETs; and the gate length (L) was 1.0 μm for both. The device parameters are listed in Table. 3.3 above.

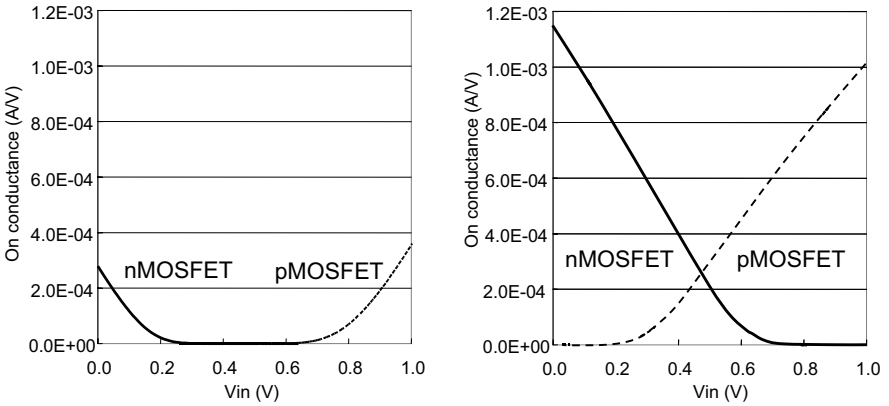


Fig. 3.30 Measured on-conductance of FD-SOI and bulk analog switches at V_{DD} = 1 V. (L = 1.0 μm , W_n =10 μm, W_p = 30 μm)

Figure 3.31 shows the on-conductance characteristics of FD-SOI and bulk CMOS switches. The threshold voltages of the bulk devices were adjusted to make the off-state leakage current 100 pA/μm; that is, the values were 0.23 V for nMOSFETs and -0.26 V for pMOSFETs.

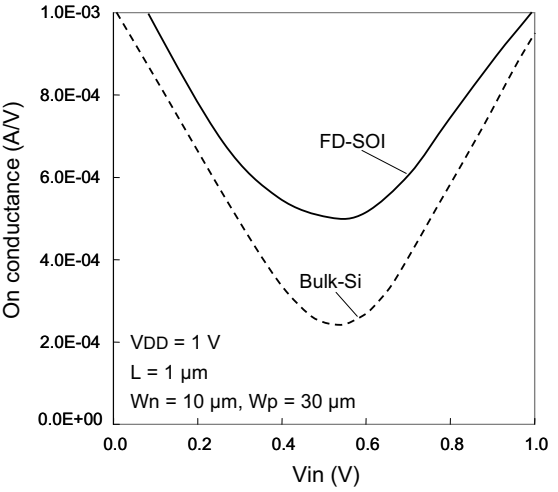


Fig. 3.31 On-conductance characteristics of FD-SOI and bulk CMOS analog switches with adjusted threshold voltages.

FD-SOI devices provide a higher on-conductance than bulk CMOS ones due to the low body factor. This makes FD-SOI technology an attractive way to fabricate low-voltage analog circuits.

3.9.3 RF Characteristics of FD-SOI Devices

The three primary RF characteristics are:

- Cut-off frequency (f_T), which is the frequency at which the current gain is equal to unity;
- Maximum oscillation frequency (f_{max}), which is the frequency at which the power gain is equal to unity; and
- Minimum noise figure (NF_{min}), which is given by Fukui's approximation with K as a fitting factor [3.20].

The formulas for these parameters are:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}, \tag{3.32}$$

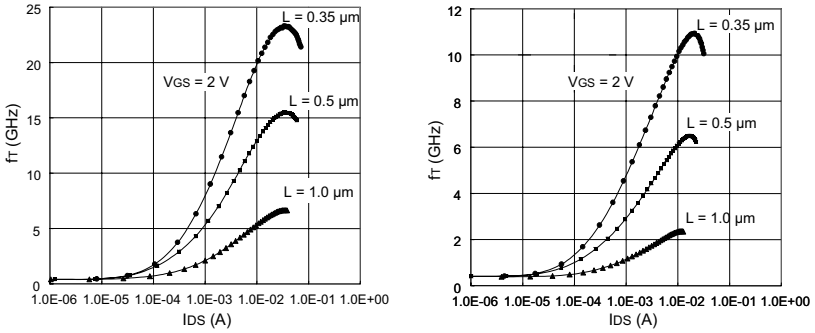
$$f_{max} = \frac{f_T}{2\sqrt{(R_g + R_i)(g_{ds} + 2\pi \cdot f_T \cdot C_{gd})}}, \tag{3.33}$$

$$NF\ min = 1 + K \cdot \frac{f}{f_T} \cdot \sqrt{g_m \cdot (R_g + R_s)}, \tag{3.34}$$

where the variables are as follows:

g_m:	Transconductance
C_{gs}:	Gate-source capacitance
C_{gd}:	Gate-drain capacitance
R_g:	Gate resistance
R_i:	Real part of the input impedance due to non-quasi-static effects
R_s:	Source resistance
g_{ds}:	Drain conductance.

The downscaling of CMOS devices has resulted in great improvements in the RF performance of bulk and SOI MOSFETs [3.21]-[3.36]. Equations (3.32) and (3.33) indicate that, while f_T can be increased by reducing the gate length, fmax depends strongly not only on gm and gds, but also on parasitic components. Research efforts are now under way to investigate and to optimize device structures to improve f_{max} and NF_{min} [3.32]-[3.36]. Figure 3.32 plots f_T against drain current for various gate lengths. 0.35-μm FD-SOI n- and pMOSFETs with a width of 200 μm exhibit an f_{Tpeak} of 23 GHz and 11 GHz, respectively.



(a) nMOSFET (b) pMOSFET

Fig. 3.32 Cut-off frequency of 0.35-μm FD-SOI n- and p-MOSFETS for three gate lengths. (W = 200 μm = 5 μm × 40 lines)

The values are similar to those of 0.35-μm bulk devices with gate widths of 100 μm and 200 μm (Fig. 3.33). In addition, the dependence of maximum stable gain (MSG) and maximum available gain (MAG) on frequency (Fig. 3.34) shows the fmax of 0.35-μm n- and pMOSFETs to be 29 GHz and 20 GHz, respectively, for W = 200 μm (5 μm × 40).

SOI devices can easily be made on a high-resistivity substrate because they are latch-up free. This provides a higher f_{max} (Fig. 3.35 (a)), probably due to the smaller parasitic capacitance with respect to the substrate and the smaller RF power loss in the substrate. A small junction capacitance and the use of a high-resistivity substrate for extrinsic elements reduce the power loss, even if the intrinsic power gain is the same [3.25]. The degree of improvement in the

power gain, which is related to f_{max}, is C_{db}^2, where C_{db} is the drain-bulk capacitance. On the other hand, the degree of improvement in the current gain, which is related to f_T, is C_{db} [3.37]. The minimum noise figure (NF_{min}) is also lower when SOI devices are made on a high-resistivity substrate (Fig. 3.35 (b)).

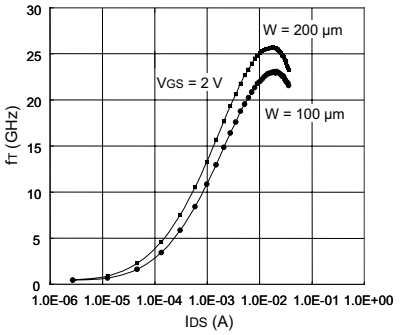


Fig. 3.33 Cut-off frequency of 0.35-µm bulk nMOSFET for two gate widths.

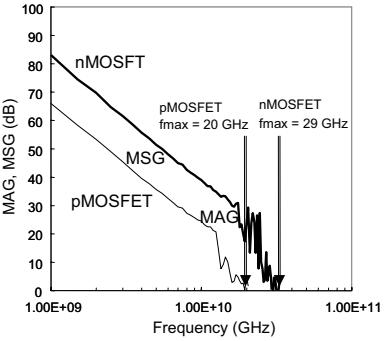
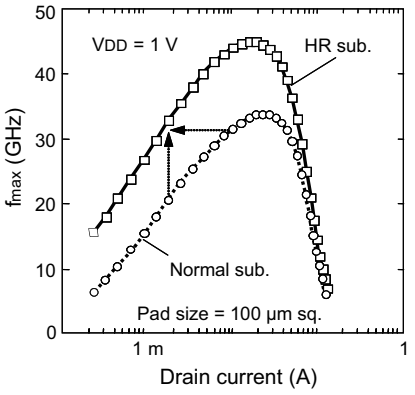


Fig. 3.34 MSG and MAG for 0.35-µm FD-SOI MOSFETs. (W =200 µm = 5 µm × 40)



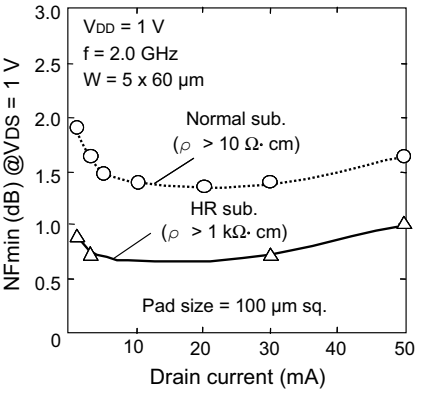


Fig. 3.35 f_{max} and NF_{min} of FD-SOI devices made on a normal (low-resistivity) substrate and on a high-resistivity (HR) substrate.

A comparison of the pad capacitance and the Q of inductors for normal (low-resistivity) and high-resistivity substrates (Fig. 3.36) reveals that the use of a high-resistivity substrate yields better characteristics. In short, FD-SOI technology combined with a high-resistivity substrate provides better RF performance.

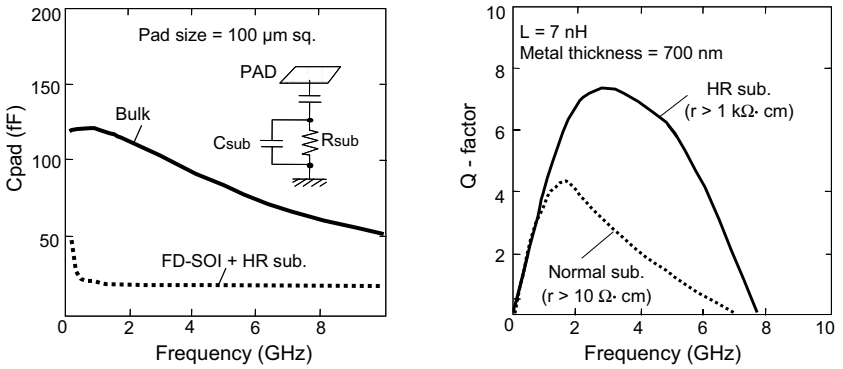


Fig. 3.36 Effective pad capacitance of bulk and FD-SOI circuits and Q of inductor made on normal (low-resistivity) substrate and on high-resistivity (HR) substrate.

3.10 Future Direction of RF and Mixed Signal Systems

As LSI technology progresses, more and more electrical systems are being integrated on chips. Almost all electrical systems contain analog circuits, and the need for analog interfaces is increasing along with advances in networking. So, the importance of mixed-signal technology will continue to increase.

Analog circuits with a relatively low speed and a large dynamic range are conventionally fabricated using 0.35- or 0.25-μm transistors. However, high-speed analog circuits that do not have a large dynamic range require scaled-down transistors. The most serious problem with the use of such transistors is operation at low voltages. Some low-voltage analog-circuit techniques were reviewed above. However, not only circuit techniques, but also system techniques are needed. Sigma-delta modulation is a good solution.
The sigma-delta ADC in Fig. 3.37 has a signal bandwidth of 2 MHz and a dynamic range of 53 dB [3.38]. The operating voltage is as low as 0.9 V, and the power consumption is just 1.5 mW. The amplifier consists of a simple CMOS circuit suitable for low-voltage operation.

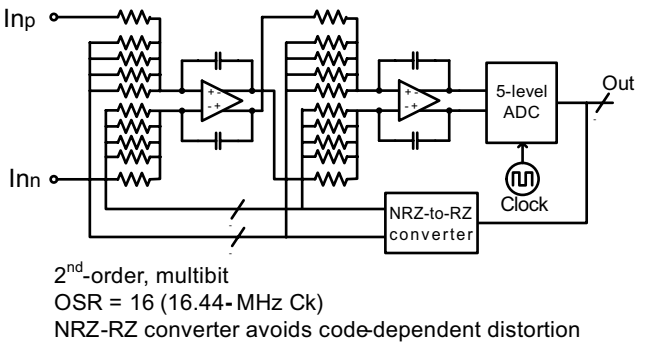


Fig. 3.37 Low-voltage sigma-delta ADC. (From T. Ueno et al. [3.38]. ©2004 IEEE.)

The sigma-delta method pushes the noise spectrum out of the target frequency band. So, the effective noise power is

$$V_n^2 = \gamma \frac{kT}{C} \cdot \frac{1}{M}, \tag{3.35}$$

where M is the oversampling ratio. This equation tells us that in-band noise can be sufficiently suppressed by raising the oversampling ratio. In addition, the allowable threshold voltage mismatch is larger, and the required amplifier gain is smaller. This yields a larger dynamic range in spite of the low voltage. This system technique will increasingly be used to achieve a large dynamic range with low-voltage circuits because boosting the speed is an effective way to increase the dynamic range.

Current mismatch is another problem with scaled-down devices operating on a low voltage; a digital calibration technique is very effective in solving it.

A high-speed 14-bit DAC usually employs large transistors to reduce current mismatch. However, this degrades the dynamic performance, and increases both power consumption and layout area. To solve this problem, small transistors with a gate length of 0.13 μm are used, and current mismatch is resolved using a digital calibration technique [3.39]. Even when digital calibration is used, the overhead area is very small because the devices are scaled down. As a result, a 9-LSB error can be reduced to 0.4 LSB. Moreover, the area and power dissipation are dramatically smaller; the area is 1/50 and the power dissipation is 1/20 that of previous 14-bit DACs.

A more radical idea for future wireless LSIs is “digital architecture” [3.40] [3.41]. These LSIs must be able to handle multiband and multistandard wireless communications. Also, the area occupied by the analog circuit should be as small as possible to reduce costs. Scaled-down digital devices provide more flexible characteristics and a smaller area than conventional analog technology. In an all-digital PLL (Fig. 3.38), conventional analog circuits, such as the charge pump, filters, and VCO in the PLL, are replaced by digital circuits [3.41].

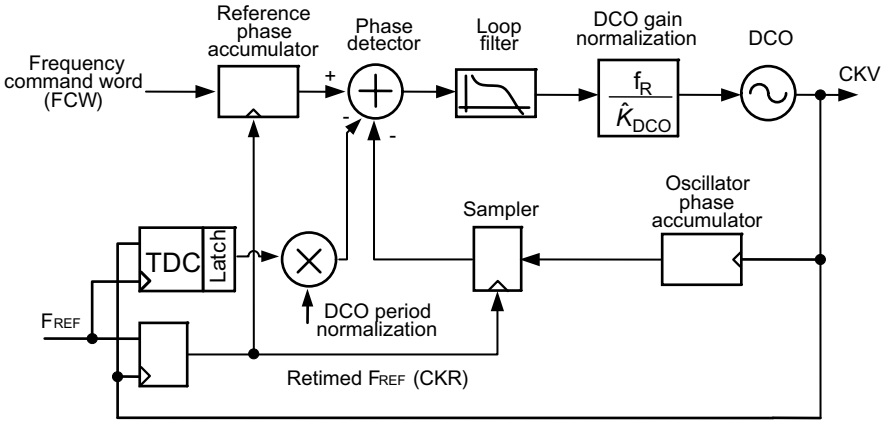


Fig. 3.38 All-digital PLL and polar transmitter. (From R. B. Staszewski et al. [3.41]. ©2005 IEEE.)

Even though digital technology is being used more widely, there will always be a need for analog circuits in future mixed-signal LSIs. A higher speed and a larger signal bandwidth will require scaled-down devices. However, it is quite difficult to make analog circuits that operate at an extremely low voltage, such as 0.5 V. The good news for analog people is that the lowering of the operating voltage in future CMOS technology will become more moderate. Figure 3.39 shows the trend in design rule and operating voltage for CMOS devices, as laid out in the ITRS 2003 Technology Roadmap [3.42]. The operating voltage of digital circuits will be around 1.0 V for high-performance devices up to the year 2014; while for conventional analog circuits, it will be 2.5 V or 1.8 V. However, scaled-down devices running on a supply voltage of about 1 V will be used for the high-speed, large-signal-bandwidth analog circuits of future RF and mixed-signal LSIs.

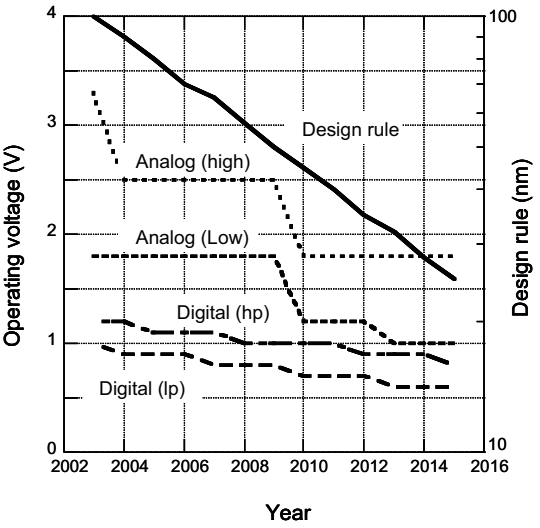


Fig. 3.39 Design rule and operating voltage in ITRS 2003 Technology Roadmap.

3.11 Summary

FD-SOI devices are the best choice for low-voltage, low-power analog circuits as well as for low-voltage digital circuits. Fully-depleted devices have almost an ideal subthreshold swing, exhibit a low off-state leakage current, and allow the threshold voltage to be reduced. This decreases the propagation delay of digital logic circuits, especially at low voltages, and also increases the transconductance. Thus, a large enough transconductance can be obtained at a smaller drain current than is possible with conventional bulk CMOS transistors. Furthermore, low-Vth transistors with a small leakage current are useful for making good low-voltage analog switches. The parasitic capacitance is small, and a high-resistivity substrate can be used because FD-SOI devices do not experience latch-up. This contributes to a low power consumption and also high performance in RF applications, such as a high fmax and a low NF. Lowering the voltage may not always boost analog performance; but a high operating frequency requires scaled-down devices running on a low voltage. The trend in electrical systems supports this strategy. In short, FD-SOI devices have great potential for use in future digital and mixed-signal LSIs.

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Chapter 4

0.5-V MTCMOS/SOI DIGITAL CIRCUITS

4.1 Introduction

This chapter describes an MTCMOS/SOI circuit scheme that makes it possible to reduce the supply voltage down to 0.5 V and presents various digital circuits that show how effective the scheme is. For combinational logic circuits, a method of clustering multi-V_{th} logic gates is explained, and demonstrated in an adder and a multiplier. Also described are a pass-transistor-type adder, a wave-pipelined multiplier based on the MTCMOS/SOI circuit scheme, and a frequency divider based on an ED-CMOS/SOI circuit scheme, all of which provide both high speed and low power at a supply voltage of 0.5 V. For a sequential logic circuit, such as a flip-flop circuit or a memory, which needs a data-hold function in the sleep mode, a multi-V_{th} data-hold circuit scheme that does not degrade the speed in the active mode is explained. Finally, a V_{DD}-hopping scheme, which is a system-level technique to reduce the power based on the MTCMOS/SOI circuit scheme, is presented. The effectiveness of the V_{DD}-hopping scheme is demonstrated in a CPU operating at supply voltages between 0.5 and 0.9 V.

4.2 MTCMOS/SOI Circuits

4.2.1 Combinational Circuits

The MTCMOS/SOI circuit scheme (Fig. 4.1) is based on SOI process technology [4.1]. Combining fully-depleted (FD) SOI low-V_{th} CMOS logic gates and a partially-depleted (PD) SOI variable-V_{th} power-switch transistor makes it possible to achieve high speed in the active mode and cut off the leakage current of the CMOS logic gates in the sleep mode.

This section describes the characteristics of each part of an MTCMOS/SOI circuit. For low-V_{th} CMOS logic gates, FD-SOI MOSFETs provide high speed at an ultralow supply voltage because they are not affected by the junction capacitance, which increases significantly at supply voltages below 1 V. This is quite different from the situation for conventional bulk MOSFETs, in which the body is tied to the supply line. In addition, FD-SOI MOSFETs exhibit better current drivability than their bulk counterparts because they have a small subthreshold swing and the threshold voltage can be reduced without any increase in the subthreshold current.

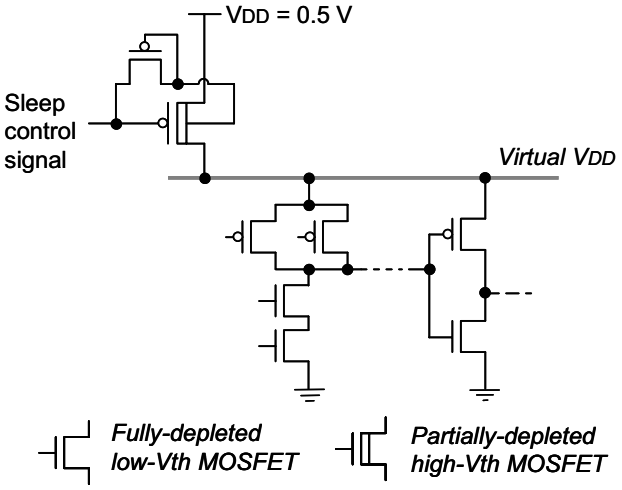


Fig. 4.1 MTCMOS/SOI circuit scheme.

In the PD-SOI MOSFET used for the power-switch transistor, the body is connected to the gate, which allows the threshold voltage to be reduced and the channel conductance to be increased in the active mode without any increase in the leakage current in the sleep mode. The technique of connecting the body directly to the gate and varying the threshold voltage depending on the operating mode is used in DT MOSFETs [4.2], provided that the supply voltage is less than 0.8 V. Figure 4.2(a) shows the static current characteristics of a DT MOSFET. When the supply voltage is applied, the p-n junction diode between the source and body is forward biased. Since the built-in potential of the diode is 0.8 V, if the supply voltage exceeds that value, a large leakage current flows from the body to the gate. To apply this technique over a wide range of supply voltages, we use a variable-V_{th} MOSFET, in which a reverse-biased diode consisting of a small, low-V_{th} MOSFET is inserted between the body and the gate. Figure 4.2(b) shows the static current characteristics in this case. When the supply voltage is over 0.8 V, the reverse-biased diode clamps the forward bias of the p-n junction diode between the body and the source, thereby suppressing the gate leakage current. The leakage current is less than 0.1 μA when the reverse-biased diode is one-tenth the size of the high-V_{th} MOSFET, which has a channel width of 10 μm.

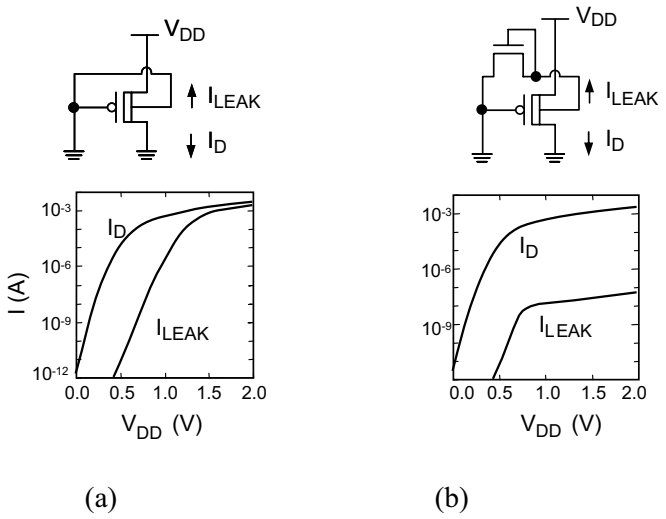


Fig. 4.2 Static current characteristics of (a) variable-V_{th} DT MOSFET and (b) variable-V_{th} MOSFET combined with low-V_{th} MOSFET.

Figure 4.3 shows the drain current characteristics of a variable-V_{th} MOSFET and a conventional MOSFET with a fixed body bias. The drain-source voltage was set to -50 mV to enable estimation of the channel conductance, which is an important factor in a power-switch transistor. In the sleep mode (V_{GS} = 0 V), the drain currents of the two MOSFETs are the same because they have the same body bias. In the active mode (V_{GS} < 0 V), the variable-Vth MOSFET has a larger drain current because the forward body bias reduces the threshold voltage. More specifically, at a gate voltage of -0.5 V, the drain current, or in other words, the channel conductance, is more than two times larger than that of the conventional one.

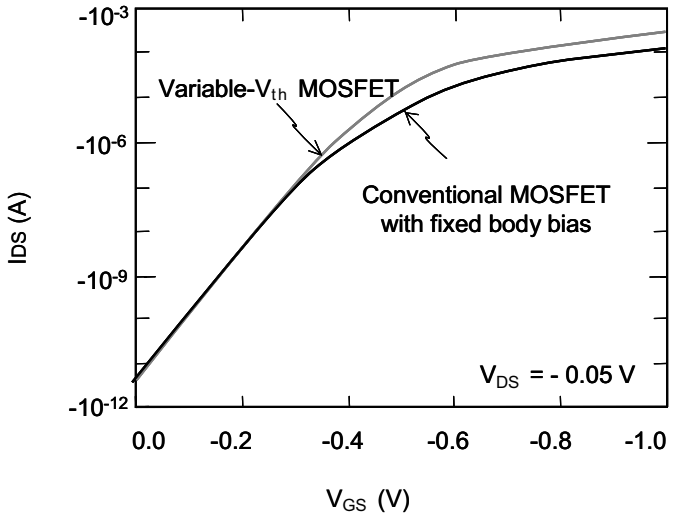


Fig. 4.3 Drain current characteristics of variable-V_{th} and conventional MOSFETs.

To estimate the delay time of a logic gate, a gate-chain TEG was designed and fabricated on a 0.25-μm MTCMOS/SOI process [4.1]. The TEG contains many logic gates for inverters, NAND gates, NOR gates, and other things. It enables estimation of the dependences of delay time and power consumption on the number of fanouts and wire length. The TEG consists of standard cells. In a standard cell, the n- and p-MOSFETs of low-V_{th} CMOS logic gates have channel widths of 3 μm and 6 μm, respectively; while the high-V_{th}

power-switch transistors have channel widths twenty times larger than those values. The delay time of an unloaded 2-NAND logic gate is 80 ps at a supply voltage of 1 V and 197 ps at 0. 5 V.

Figure 4.4 shows the estimated dependence of delay time on supply voltage for a fundamental logic gate (2-input NAND gate with 3 fanouts and a wiring length of 1 mm). The two curves are for devices made on MTCMOS/SOI and bulk MTCMOS processes with the same design rule [4.1]. The figure shows that only the MTCMOS/SOI circuit can operate at a supply voltage of 0.4 V without any serious increase in the delay time. At a supply voltage of 1 V, the delay time is 273 ps, which is less than half that of the bulk MTCMOS circuit; and at 0.5 V, it is 710 ps, which is one-third that of the bulk one.

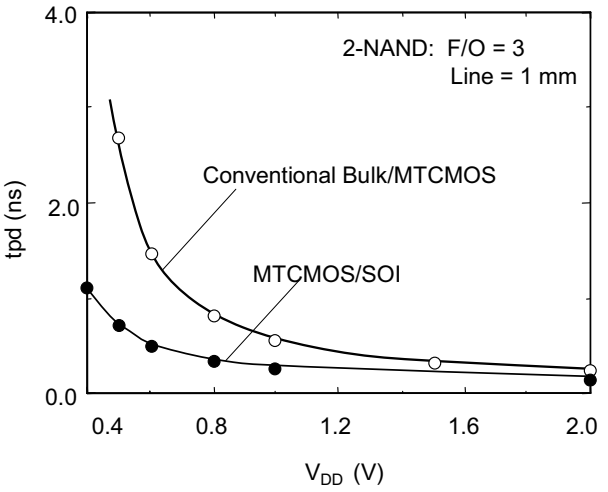


Fig. 4.4 Estimated delay-time characteristics of a fundamental logic gate in a 0.25-μm MTCMOS/SOI circuit and in a 0.25-μm bulk MTCMOS circuit.

Figure 4.5 shows the delay times of two power-switch transistors. Since the one consisting of a variable-V_{th} MOSFET has a large channel conductance and a small threshold-voltage variation [4.3], the delay time and its variation are less than those of a conventional MOSFET with a fixed body bias. At a supply voltage of 0.4 V, the delay time of the former is 1125 ps. This is 10%

smaller, and the variation is 30% smaller, than the value for the conventional scheme.

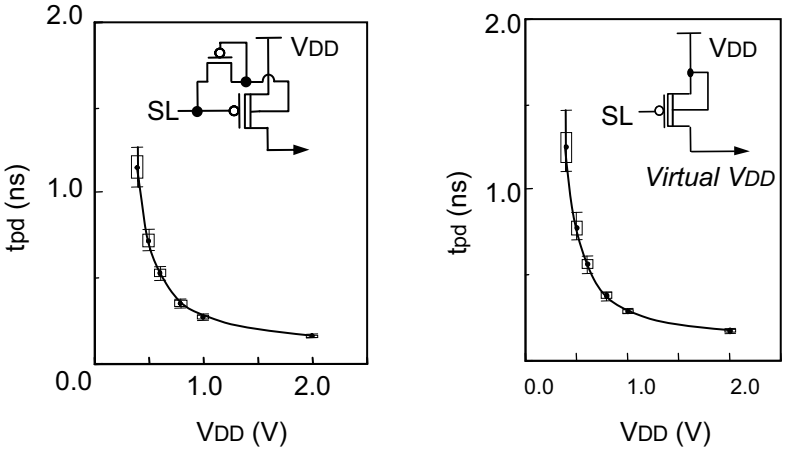


Fig. 4.5 Comparison of power-switch transistors: (a) Variable-V_{th} MOSFET and (b) conventional MOSFET with fixed body bias.

4.2.2 Sequential Circuits

The MTCMOS/SOI circuit scheme makes it possible to reduce the leakage current in low-V_{th} combinational logic circuits in the sleep mode, while maintaining the speed in the active mode. However, with this scheme special care must be taken in the design of sequential logic circuits with memory functions, such as latches and flip-flops. The data in latches must be preserved during the sleep period. The problem is that, in an MTCMOS circuit, the power-switch transistor is off in the sleep mode and the virtual supply voltage is close to the ground level; so the data in circuits connected to the virtual supply line are lost.

The solution is to add a data-hold circuit (Fig. 4.6) for the sleep mode that is connected to the supply line, which provides the power needed for storing data. It consists of high-V_{th} MOSFETs to suppress the leakage current. There are various ways of implementing such a circuit.

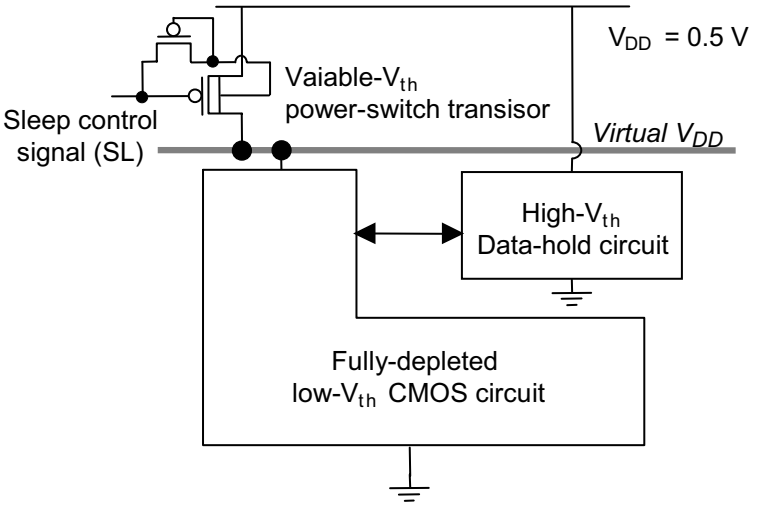
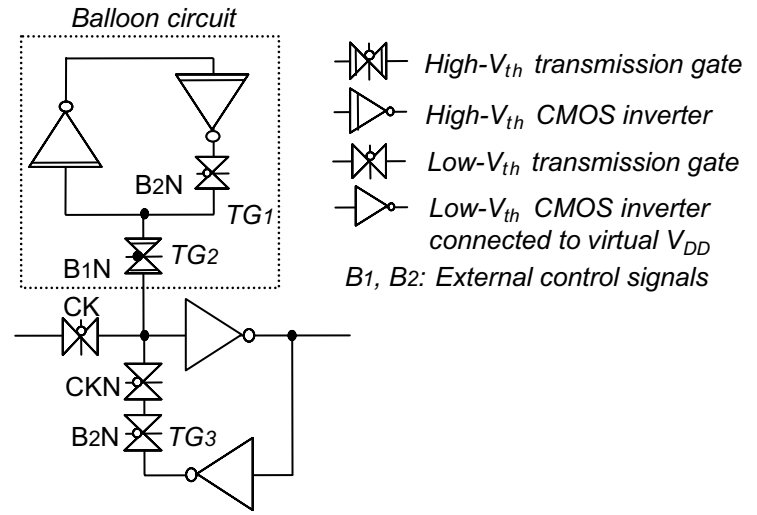


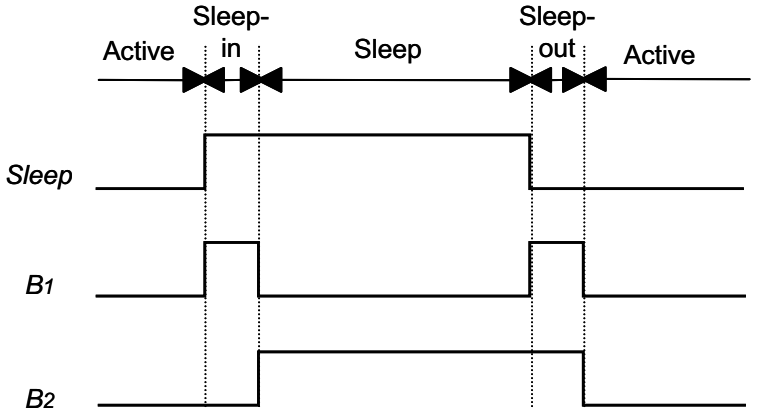
Fig. 4.6 MTCMOS/SOI data-hold circuit scheme.

One type of MTCMOS latch (Fig. 4.7(a)) consists of a standard latch combined with a memory cell called a balloon circuit [4.4]. The balloon circuit is connected to the supply line and is thus always powered to preserve the data in the sleep mode. It is composed of two high-V_{th} CMOS inverters and two switches consisting of the transmission gates TG_1 and TG_2.

The timing chart (Fig. 4.7(b)) for the control signals to the transmission gates shows that the operation of the balloon circuit can be broken down into four periods corresponding to the states of the latch: active, sleep-in, sleep, and sleep-out.



(a)



(b)

Fig. 4.7 (a) Circuit diagram of MTCMOS latch consisting of a standard latch and a balloon circuit, which is a memory cell that preserves the data in the sleep mode; and (b) timing chart for external control signals. (From S. Shigematsu et al. [4.4]. ©1997 IEEE.)

• **Active period**: The balloon circuit is cut off from the latch by the switch TG2. This keeps the load on the latch small so that its speed is not affected. In this period, the balloon circuit does nothing.

• **Sleep-in period**: This is the period of transition from the active to the sleep mode. The switch TG_2 turns on and TG_1 remains off; so the data in the latch are read-out to the balloon circuit, thus readying the latch for the sleep mode.

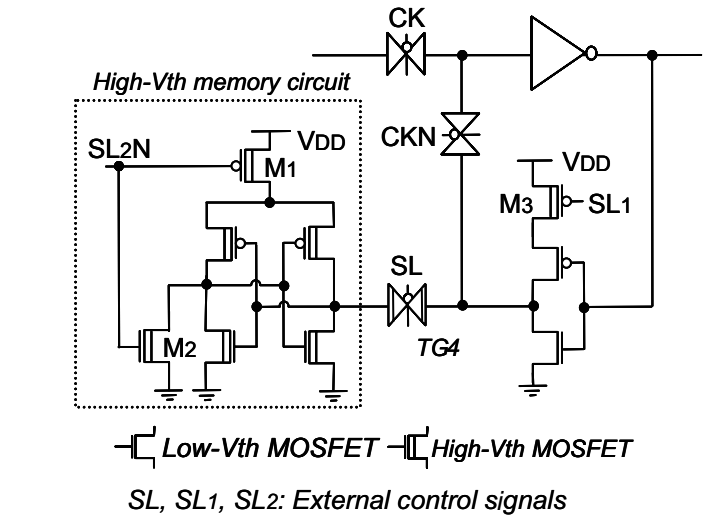
• **Sleep period**: The balloon circuit preserves the data during the sleep mode because TG_1 is on and the switches TG_2 and TG_3 isolate the data. Since TG_2 consists of high-V_{th} MOSFETs, it cuts off the leakage current path from the balloon circuit.

• **Sleep-out period**: This is the period of transition from the sleep to the active mode. The switch TG_2 turns on, restoring the data to the latch.

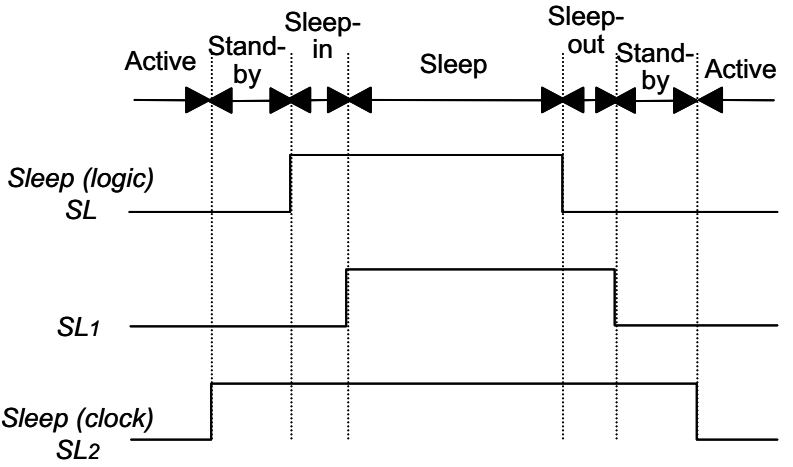
Since the state of the balloon circuit changes only during the transitional periods, the latch smoothly resumes operation whenever it comes out of the sleep mode and re-enters the active mode. Furthermore, the balloon circuit is isolated from the forward data path during the active period; so, it does not become a bottleneck during high-speed operation of the main low-V_{th} circuit.

Another type of MTCMOS latch (Fig. 4.8) employs a high-V_{th} memory circuit attached to the feedback loop of the latch [4.5]. Since the feedback loop is a non-critical path, the memory circuit is added to the output of the inverter in the loop. A switch consisting of the transmission gate TG_4, which is made of high-V_{th} MOSFETS, is placed between the latch and the memory circuit to control read/write operations. The memory circuit is composed of two high-V_{th} inverters and the two switches M_1 and M_2.

The timing chart (Fig. 4.8(b)) for the control signals to the switches shows that the operation of the memory circuit can be broken down into six periods corresponding to the states of the latch: active, stand-by, sleep-in, sleep, sleep-out, and stand-by.



(a)



(b)

Fig. 4.8 High-V_{th} memory circuit attached to the feedback loop of an MTCMOS latch. (a) Circuit diagram. (b) Timing chart for external control signals.

• **Active period**: The switches M_1 and M_2 set the output of the memory circuit to the high-impedance state, which prevents the memory circuit from disturbing the operation of the latch, even though TG_4 is on. Since there is no additional circuit in the forward data path, the latch operates faster than one with a balloon circuit. In this period, the memory circuit does nothing.

• **Stand-by period**: This is the period of transition between the active and sleep-in modes. The switch M_1 of the memory circuit turns on; and the data in the latch are read-out to the memory, readying the latch for the sleep-in mode.

• **Sleep-in period**: This is the period of transition between the stand-by and sleep modes. The switch TG_4 turns off, isolating the memory circuit from the latch and cutting off the leakage current from the memory circuit.

• **Sleep period**: The switch M_3 of the inverter in the latch turns off, destroying the data, which is now safely stored in the memory circuit.

• **Sleep-out period**: This is the period of transition between the sleep and stand-by modes. TG_4 turns on, reconnecting the memory circuit to the latch and thus readying the latch to enter the stand-by mode.

• **Stand-by period**: This is the period of transition between the sleep-out and active modes. The switch M_3 of the inverter in the latch turns on, and the data in the memory are read-out to the latch.

Figure 4.9 shows a delayed flip-flop (DFF) with an MTCMOS latch. In this case, the clock signal is the high level in the sleep mode. So, the MTCMOS latch is used as the master latch of the DFF. The memory control switch TG_5 is inserted in the feed-forward circuit of the main latch circuit so that the sleep signal itself initiates a read-out operation through the use of an internal control signal generator [4.5].

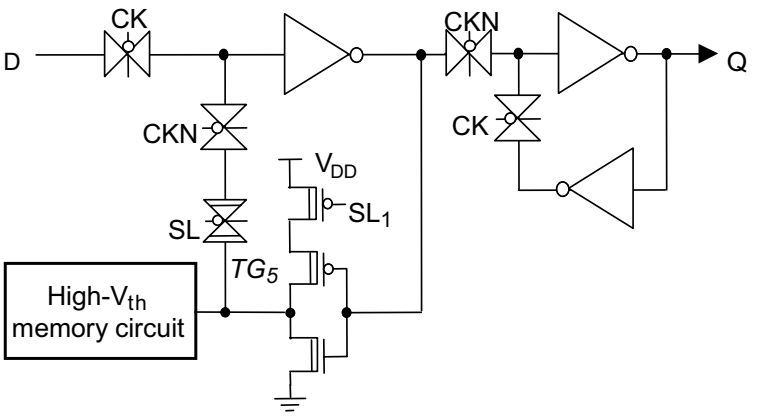


Fig. 4.9 MTCMOS DFF with high-V_{th} memory circuit.

To verify that the data-hold scheme functions properly, an MTCMOS DFF with a high-V_{th} memory circuit was designed and used in a 1/8 frequency divider, which was fabricated on a 0.25-μm MTCMOS/SIMOX process [4.5]. The gate oxide was 5 nm thick; the active Si layer, 50 nm thick; and the buried oxide, 100 nm thick. The absolute values of the threshold voltages of the low- and high-V_{th} MOSFETs were 0.1 and 0.2 V, respectively.

Figure 4.10 shows the operating waveforms, including those for the sleep period. The operating frequency was 100 MHz, and the sleep period was 100 ns long. The results show that the circuit stores the data of the high level during the sleep period, which is exactly what it is designed to do.

Figure 4.11 shows how maximum input frequency depends on supply voltage for the DFF in the frequency divider. The characteristics of a DFF with a balloon circuit are also shown for comparison. The maximum input frequency of the DFF with the high-V_{th} memory circuit in the feedback loop is 700 MHz at 0.5 V, which is 100 MHz higher than that of a DFF with a balloon circuit.

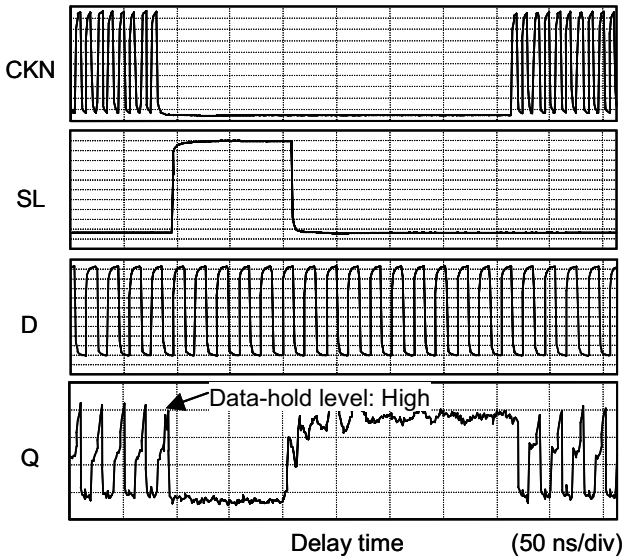


Fig. 4.10 Measured waveforms of MTCMOS DFF, including those for the sleep mode.

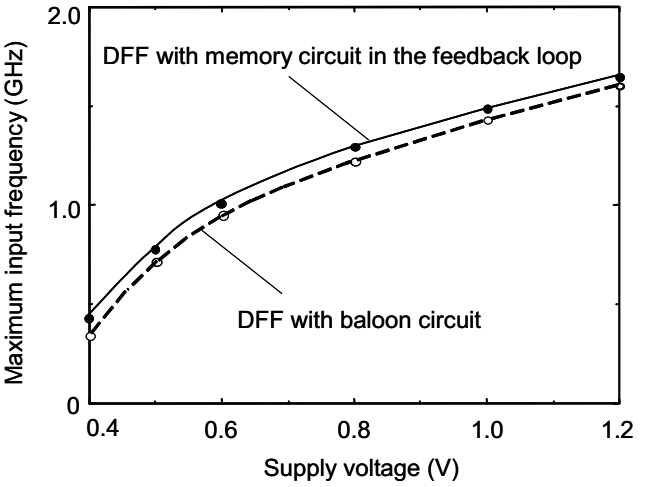


Fig. 4.11 Maximum input frequency vs. supply voltage for DFF with high-V_{th} memory circuit in the feedback loop (used in 1/8 frequency divider) and for DFF with balloon circuit.

4.3 Adder

When the logic block of an MTCMOS/SOI circuit is composed only of low-V_{th} MOSFETs, the leakage current is cut off in the sleep mode, but not in the active mode. A good way to reduce the active-mode leakage current without any degradation in speed is to use medium-V_{th} FD-SOI MOSFETs for the non-critical paths of CMOS logic gates. The result is the triple-V_{th} MTCMOS/SOI circuit scheme in Fig. 4.12 [4.6].

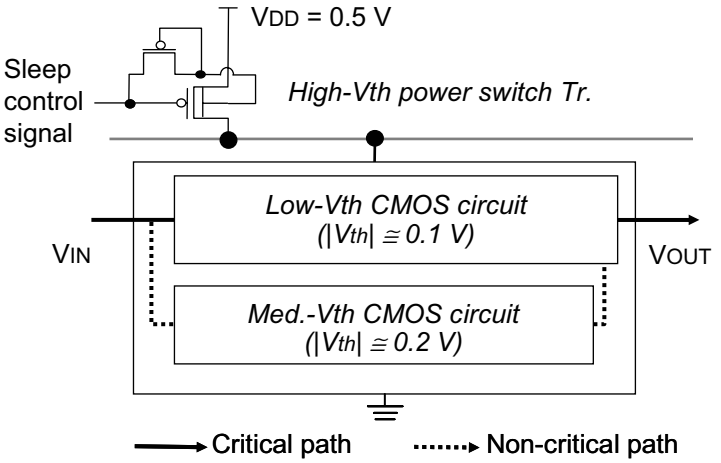


Fig. 4.12 Triple-V_{th} MTCMOS/SOI circuit scheme.

Figure 4.13 shows how delay time and leakage current depend on threshold voltage for FD-SOI and bulk devices. For FD-SOI devices, if we set the low V_{th} to 0.1 V and the medium V_{th} to 0.2 V, a medium-V_{th} logic gate is only about 50% slower than a low-V_{th} one, while the leakage current is about two orders of magnitude smaller. The fact that FD-SOI MOSFETs have a small subthreshold swing close to the ideal value of 60 mV/decade makes it possible to obtain these leakage current characteristics. For bulk devices, which have a large subthreshold swing of 85 mV/decade, increasing V_{th} from 0.1 V to 0.2 V only reduces the leakage current by about one order of magnitude. To obtain the same leakage current as that of an FD-SOI device, the medium Vth has to be up around 0.3 V. This makes the delay time about three times longer than that of a low-V_{th} CMOS circuit. In short, it is difficult to fine-tune the

threshold voltages of bulk devices to reduce the leakage current in the active mode.

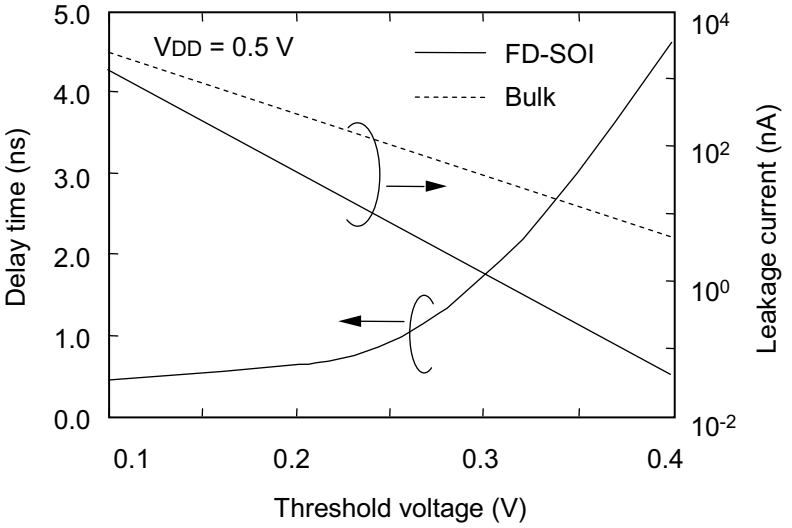


Fig. 4.13 Dependence of circuit performance on threshold voltage.

This section describes the application of the triple-V_{th} MTCMOS/SOI circuit scheme to the design of adders.

4.3.1 Carry Look-Ahead Adder

Figure 4.14 shows a 4-bit carry look-ahead (CLA) adder based on the MTCMOS/SOI circuit scheme. The adder consists of a sum part and a carry part.

The sum signal is

$$S_i = A_i \oplus B_i \oplus C_{i-1} \quad (i = 0,...,3), \tag{4.1}$$

where A_i and B_i are the inputs of the ith stage of the adder, C_i is the carry signal of the ith stage, and $C_{-1} = C_{in}$.

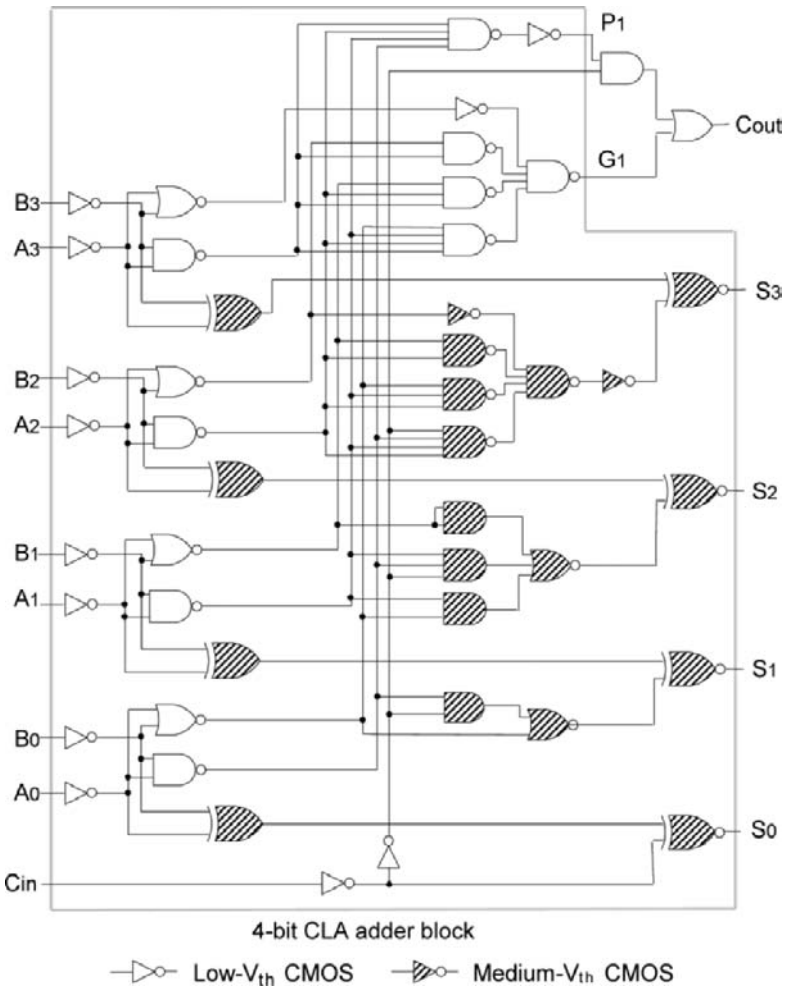


Fig. 4.14 Circuit diagram of multi-V_{th} 4-bit CLA adder.

The carry signal is given by

$$C_i = g_i + p_i \cdot C_{i-1}, \tag{4.2}$$

where

$g_i = A_i \cdot B_i$ (generate signal)

$p_i = A_i + B_i$ (propagate signal).

The output of the carry part can thus be expanded as follows:

$$C_{OUT} = g_3 + p_3 \cdot C_2$$

$$= g_3 + p_3 \cdot [g_2 + p_2 \cdot C_1]$$

$$= g_3 + p_3 \cdot g_2 + p_3 \cdot p_2 \cdot g_1 + p_3 \cdot p_2 \cdot p_1 \cdot C_0]$$

$$= g_3 + p_3 \cdot g_2 + p_3 \cdot p_2 \cdot g_1 + p_3 \cdot p_2 \cdot p_1 \cdot [g_0 + p_0 \cdot C_{in}]$$

$$= g_3 + p_3 \cdot g_2 + p_3 \cdot p_2 \cdot g_1 + p_3 \cdot p_2 \cdot p_1 \cdot g_0 + p_3 \cdot p_2 \cdot p_1 \cdot p_0 \cdot C_{in}. \quad (4.3)$$

If we define

$$G_1 \equiv g_3 + p_3 \cdot g_2 + p_3 \cdot p_2 \cdot g_1 + p_3 \cdot p_2 \cdot p_1 \cdot g_0$$

and

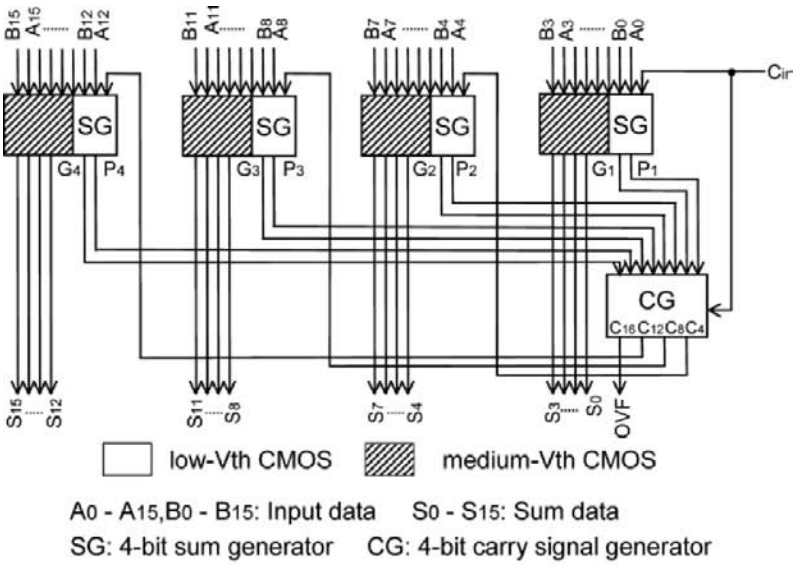
$$P_1 \equiv p_3 \cdot p_2 \cdot p_1 \cdot p_0,$$

then (4.3) becomes

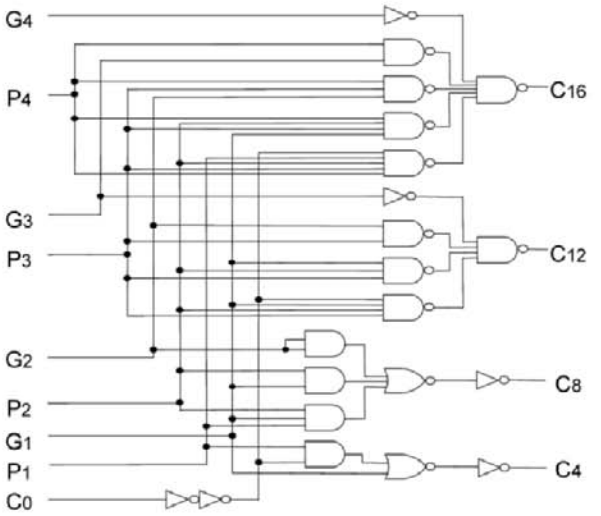
$$C_{OUT} = G_1 + P_1 \cdot C_{in}. \quad (4.4)$$

For a 4-bit CLA adder, the critical path is in the carry part. So, low-V_{th} CMOS logic gates are used for that part, and medium-V_{th} ones are used for the sum part. Since there are almost equal numbers of medium- and low-V_{th} logic gates, the triple-V_{th} scheme reduces the active leakage current to half that for the dual-V_{th} scheme.

To verify the proper operation of an adder based on the triple-V_{th} MTCMOS/SOI circuit scheme, a 16-bit CLA adder was designed and fabricated on a 0.25-μm MTCMOS/SOI process [4.6]. The block diagram in Fig. 4.15(a) shows that the adder consists of four 4-bit CLA adder blocks and a 4-bit carry-signal generator.



(a)



(b)

Fig. 4.15 (a) Block diagram of 16-bit CLA adder based on multi-V_{th} CMOS scheme, and (b) circuit diagram of 4-bit carry-signal generator.

The carry part, which is the critical part, is composed of low-V_{th} CMOS logic gates; and the sum part is composed medium-V_{th} ones. The circuit diagram of the 4-bit carry-signal generator is shown in Fig. 4.15(b).

In the carry-signal generator, the carry signal is

$$C_{4i} = G_i + P_i \cdot C_{4(i-1)} \qquad (i = 1,...,4), \tag{4.5}$$

where

$$G_i = g_{4i-1} + p_{4i-1} \cdot g_{4i-2} + p_{4i-1} \cdot p_{4i-2} \cdot g_{4i-3}$$

$$+ p_{4i-1} \cdot p_{4i-2} \cdot p_{4i-3} \cdot g_{4i-4}$$

and

$$P_i = p_{4i-1} \cdot p_{4i-2} \cdot p_{4i-3} \cdot p_{4i-4}.$$

So, the C_i's for the four look-ahead stages are:

$$C_4 = G_1 + P_1 \cdot C_0$$

$$C_8 = G_2 + P_2 \cdot G_1 + P_2 \cdot P_1 \cdot C_0$$

$$C_{12} = G_3 + P_3 \cdot G_2 + P_3 \cdot P_2 \cdot G_1 + P_3 \cdot P_2 \cdot P_1 \cdot P_0$$

$$C_{16} = G_4 + P_4 \cdot G_3 + P_4 \cdot P_3 \cdot G_2 + P_4 \cdot P_3 \cdot P_2 \cdot G_1 + P_4 P_3 P_2 P_1 C_0. \tag{4.6}$$

The delay time of the adder is 5.2 ns at a supply voltage of 0.5 V, and the power dissipation is 0.15 mW at an operating frequency of 100 MHz. The distribution of delay times among the paths is shown in Fig. 4.16, along with data on an all-low-V_{th} adder for comparison. The use of two V_{th}'s shifts the distribution toward a larger delay time without significantly increasing the maximum delay time. The effectiveness of the multi-V_{th} CMOS technique in reducing the leakage current can be seen in Fig. 4.17. Since there are about the same number of low- and medium-V_{th} CMOS logic gates, the leakage current is only half that of an all-low-V_{th} CMOS circuit.

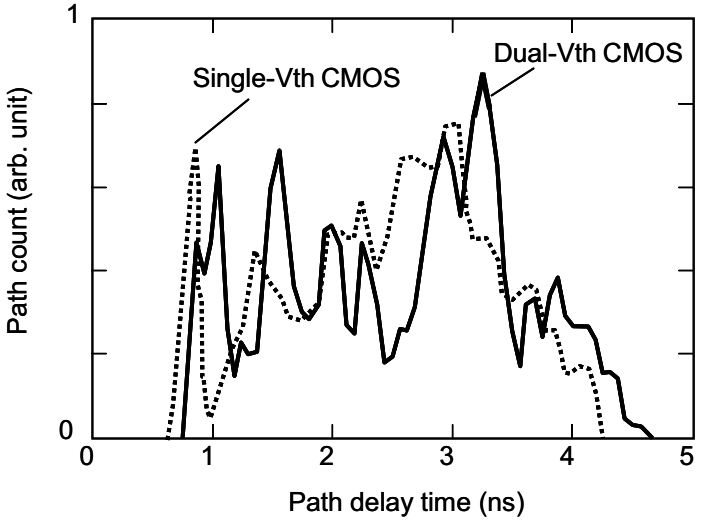


Fig. 4.16 Distribution of delay times among signal paths for single- and dual-V_{th} 16-bit CLA adders.

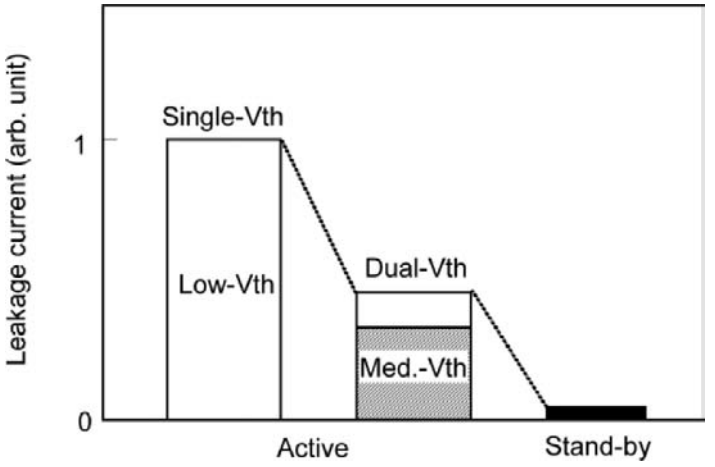
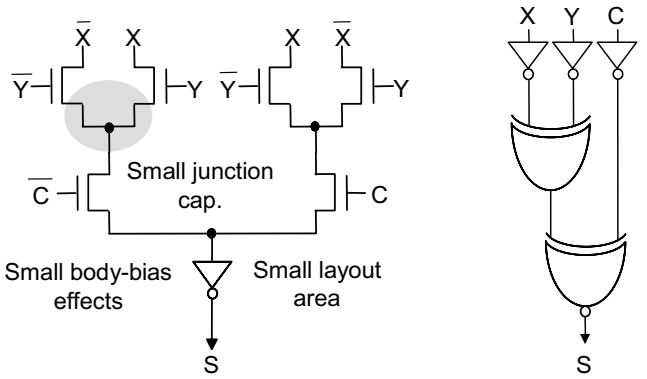


Fig. 4.17 Comparison of leakage currents of 16-bit CLA adders based on single- and dual-V_{th} MTCMOS circuit schemes.

4.3.2 Carry Select Adder

The key features of FD-SOI devices are a small junction capacitance, small body-bias effects, and a small layout area. They enable the use of pass-transistor logic, which improves circuit performance. Fig. 4.18 shows a half adder based on this logic. In pass-transistor logic, the input and output terminals are the source and drain terminals of MOSFETs. This configuration boosts the speed and lowers the power dissipation because the capacitances of the terminals are small and the current drivability of the MOSFETs is large due to the small body-bias effects. In addition, FD-SOI devices do not have a well or a fourth body terminal; so, the device isolation is smaller. The small layout area reduces the wiring capacitance, which causes large delay times in large LSIs. This section describes a carry-select adder based on pass-transistor logic



(a) (b)

Fig. 4.18 Ultralow-voltage half-adder scheme suitable for CMOS/SOI circuits. (a) Pass-transistor circuit. (b) Conventional logic gate.

Figures 4.19 and 4.20 show a 4-bit carry-select adder based on pass-transistor logic. The sum and carry signals are given by

$$S_i = A_i \oplus B_i \oplus C_{i-1} \quad (i = 0,...,3) \tag{4.7}$$

$$C_i = A_i \cdot B_i \cdot \overline{C_{i-1}} + (A_i + B_i) \cdot C_{i-1}\,. \tag{4.8}$$

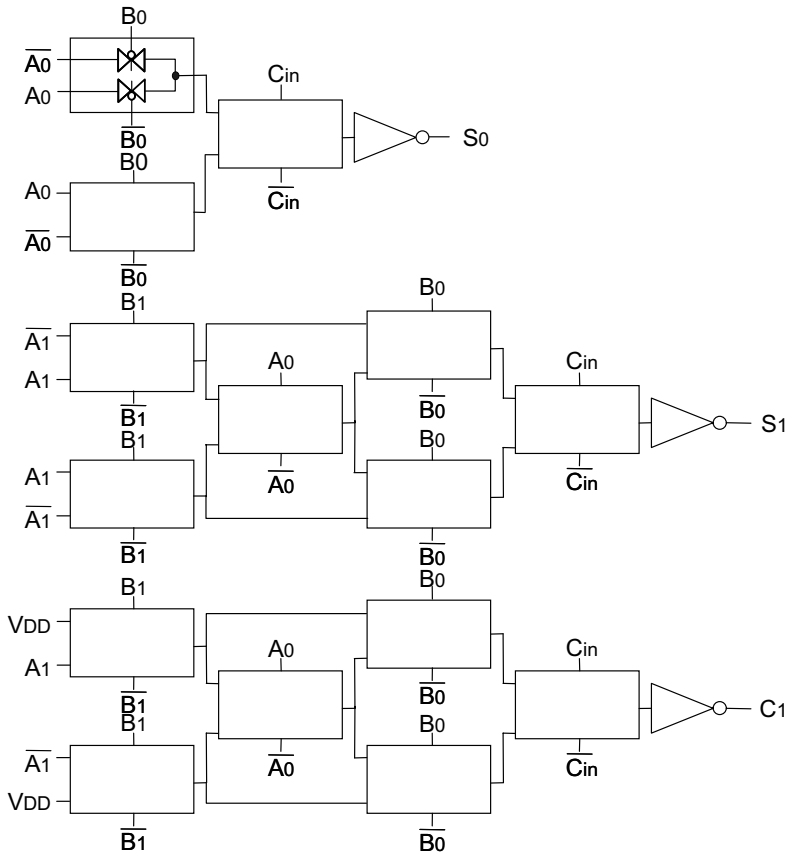


Fig. 4.19 Circuit diagram of 4-bit carry-select adder based on pass-transistor logic (0-carry propagation).

For 0-carry propagation, the sums S_0 and S_1 are

$$S_0 = (A_0 \oplus B_0)\cdot\overline{C_{in}} + (\overline{A_0 \oplus B_0})\cdot C_{in} = \overline{(A_0 \oplus B_0)\cdot C_{in} + (\overline{A_0 \oplus B_0})\cdot\overline{C_{in}}}$$

$$S_1 = \overline{(A_1 \oplus B_1)\cdot C_0 + (\overline{A_1 \oplus B_1})\cdot\overline{C_0}}, \tag{4.9}$$

where

$$C_0 = (A_0 + B_0) \cdot C_{in} + A_0 \cdot B_0 \cdot \overline{C_{in}} = (A_0 \cdot \overline{B_0} + B_0) \cdot C_{in} + A_0 \cdot B_0 \cdot \overline{C_{in}}$$

$$\overline{C_0} = (\overline{A_0} \cdot B_0 + \overline{B_0}) \cdot \overline{C_{in}} + \overline{A_0} \cdot \overline{B_0} \cdot C_{in}$$

And the carry signal C_1 is

$$C_1 = (A_1 + B_1) \cdot C_0 + A_1 \cdot B_1 \cdot \overline{C_0} = (A_1 \cdot \overline{B_1} + B_1) \cdot C_0 + (\overline{\overline{A_1} \cdot B_1 + \overline{B_1}}) \cdot C_0$$

$$\overline{C_1} = (\overline{A_1} \cdot B_1 + \overline{B_1}) \cdot \overline{C_0} + \overline{A_1} \cdot \overline{B_1} \cdot C_0 . \qquad (4.10)$$

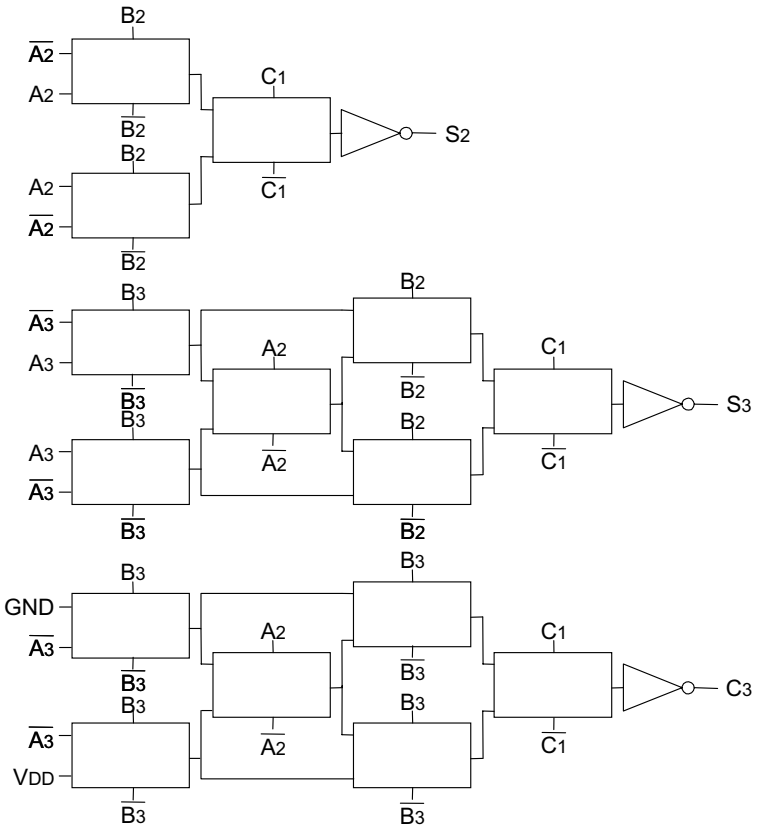


Fig. 4.20 Circuit diagram of 4-bit carry-select adder based on pass-transistor logic (1-carry propagation).

For 1-carry propagation, the sums S_2 and S_3 are

$$S_2 = \overline{(A_2 \oplus B_2) \cdot C_1 + (\overline{A_2 \oplus B_2}) \cdot \overline{C_1}}$$

$$S_3 = \overline{(A_3 \oplus B_3) \cdot C_2 + (\overline{A_3 \oplus B_3}) \cdot \overline{C_2}}, \qquad (4.11)$$

where

$$C_2 = (A_2 \cdot \overline{B_2} + B_2) \cdot C_0 + A_2 \cdot B_2 \cdot \overline{C_0}$$

$$\overline{C_2} = (\overline{A_2} \cdot B_2 + \overline{B_2}) \cdot \overline{C_0} + \overline{A_2} \cdot \overline{B_2} \cdot C_0$$

And the carry signal C_3 is

$$C_3 = (A_3 \cdot \overline{B_3} + B_3) \cdot C_2 + (\overline{\overline{A_3} \cdot B_3 + \overline{B_3}}) \cdot C_2 . \qquad (4.12)$$

Figure 4.21 compares the simulated dependences of delay time on supply voltage for three types of 4-bit adders. Since the threshold voltages of the SOI devices are smaller than those of bulk devices under the same leakage current conditions, the delay time of CMOS/SOI gates is much shorter than that of CMOS/bulk gates. Pass-transistor logic maintains the high-speed performance at low supply voltages of less than 1 V, and provides significantly smaller delay times at ultralow supply voltages of less than 0.5 V.

To assess the effectiveness of triple-V_{th} MTCMOS/SOI pass-transistor logic, 32-bit adders were designed and fabricated on 0.35-μm and 0.25-μm MTCMOS/SOI processes [4.7]. The graph of delay time vs. supply voltage in Fig. 4.22 indicates that, for the 0.25-μm process and a supply voltage of 0.5 V, we can obtain a delay time of 10 ns, which corresponds to the mobile-use target of 100 MHz.

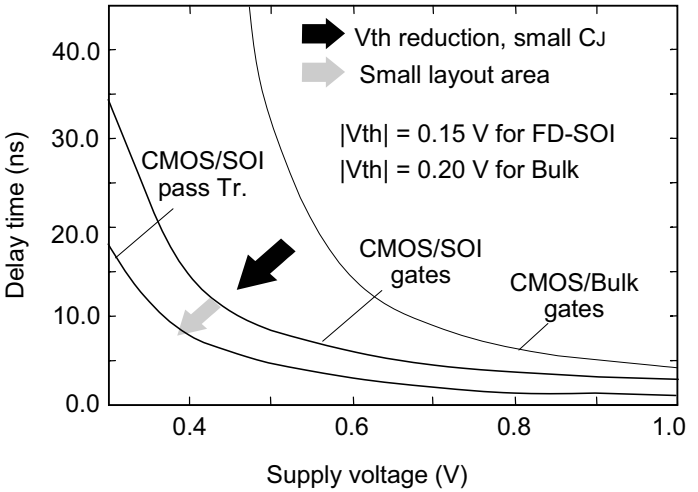


Fig. 4.21 Simulated delay-time characteristics of pass-transistor-type 4-bit adders.

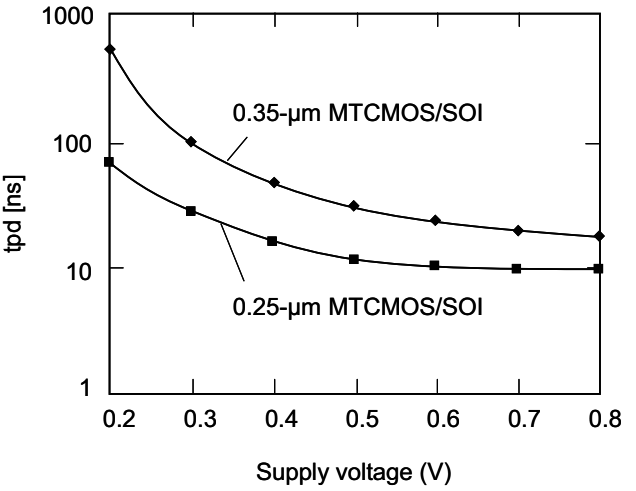
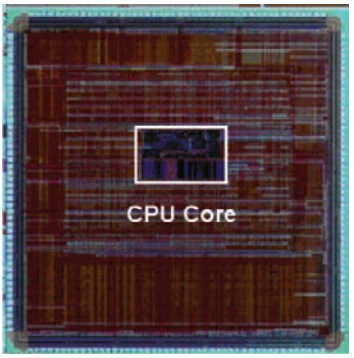


Fig. 4.22 Delay-time characteristics of fabricated 32-bit carry-select adders based on pass-transistor logic.

As another demonstration of this technology, the 32-bit RISC CPU [4.7] in Fig. 4.23, which is based on a 32-bit carry select adder, was also fabricated. The operating frequency is 25 MHz at a supply voltage of 0.65 V, and the power efficiency is 28 GIPS/W.



(a)

Specifications of 32-bit RISC CPU

Process technology	0.35-μm triple-metal MTCMOS/SOI
Threshold voltage	$\|V_{thL}\|$ = 0.15 V $\|V_{thH}\|$ = 0.35 V
Core size	1.8 mm X 1.2 mm
Tr. count	740,000
Maximum frequency	25 MHz @0.65 V
Power dissipation	0.7 mW (@25 MHz) < 1 μW in sleep mode
Power efficiency	28 GIPS/W

(b)

Fig. 4.23 32-bit RISC CPU with 32-bit carry select adder: (a) microphotograph and (b) specifications.

4.4 Multiplier

Figure 4.24 illustrates the principle of multiplication. The symbols (*A0*, *B0*, *P0,0*, etc.) represent binary digits. The multiplicand is consecutively multiplied by each bit of the multiplier, resulting in a number of partial products, which are shifted and summed to yield the final product. For example, if we multiply $\{A7,A6,\ldots,A1\}$ by $B3$, which is the fourth least significant bit of $\{B7,B6,\ldots,B0\}$, then we obtain the partial product $\{P7,3,P6,3,\ldots,P0,3\}$. This row is shifted left by three digits to align it with the bit position of $B3$, and added to the other partial products to yield the final product $\{P15,P14,\ldots,P0\}$. To boost the speed and lower the power dissipation of a multiplication circuit, the partial products must be reduced in number and summed in parallel.

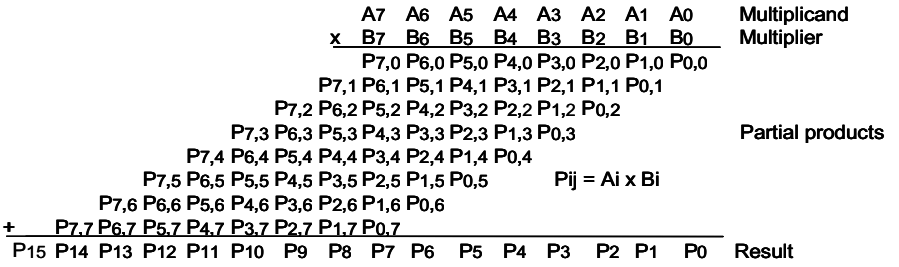


Fig. 4.24 Principle of 8 × 8-bit multiplication.

4.4.1 Booth-Encoder and Wallace-Tree Multiplier

Figure 4.25 shows a Booth-encoder and Wallace-tree multiplier. Booth encoding involves converting the multiplier, B, from a signed binary integer into a signed radix- 4 integer as follows:

$$B = \sum_{j=0}^{n/2-1} (B_{2j-1} + B_{2j} - 2B_{2j+1}) \times 2^{2j}$$

$$\equiv \sum_{j=0}^{n/2-1} C_j \times 2^{2j}, \quad C_j \in (-2,-1,0,1,2) \tag{4.13}$$

The encoding is performed by mapping a combination of three consecutive binary bits into one of the signed radix-4 digits -2, -1, 0, -1 or 2. Since the

encoding halves the number of digits in the multiplier, it also halves the number of partial products to be added up [4.8].

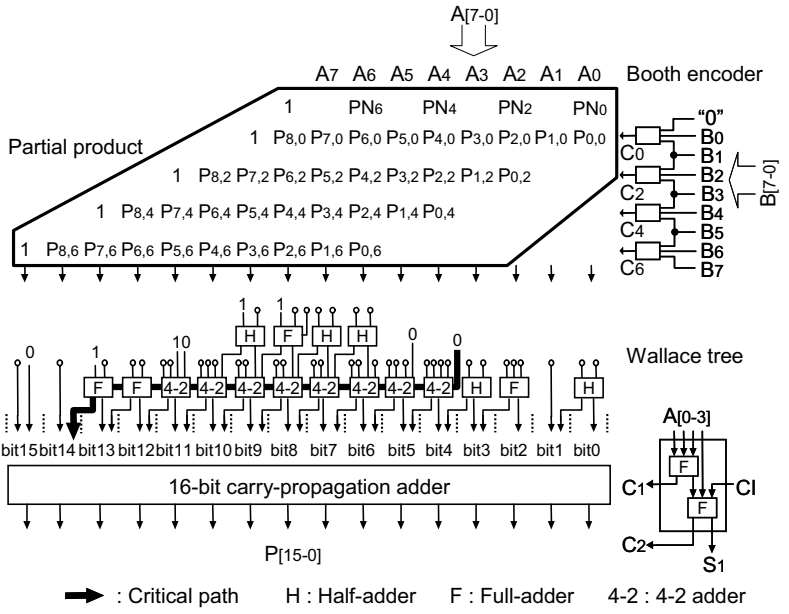


Fig. 4.25 8×8-bit Booth-encoder and Wallace-tree multiplier.

A circuit for generating a partial product in the Booth-encoding scheme is somewhat complex because multiplying a radix-4 digit by a binary one requires shift and inversion operations. Figure 4.26 shows the circuit diagram of a Booth encoder and partial-product generator, and Table 4.1 shows the corresponding truth table. The encoder assigns a radix-4 digit to the three inputs B_{2j+1}, B_{2j}, and B_{2j-1}, and maps it into a combination of the three control values X, $2X$, and PN_{2j}. The subscript j runs from 0 to 3, and the edge value B_{-1} is set to 0. X is given by $B_{2j} \oplus B_{2j-1}$; $2X$ is given by $\overline{B_{2j+1}} \cdot B_{2j} \cdot B_{2j-1} + B_{2j+1} \cdot \overline{B_{2j}} \cdot \overline{B_{2j-1}}$; and PN_{2j} is the input B_{2j+1}. Using these three control outputs and the two consecutive bits A_i and A_{i-1}, the partial product $P_{i,2j}$ is calculated as follows:

$$P_{i,2j} = (X \cdot A_i + 2X \cdot A_{i-1}) \oplus PN_{2j}, \tag{4.14}$$

where the subscript *i* runs from 0 to 7. *P8,2j* in Table 4.1 is the extended sign in Fig. 4.25. It is calculated in the same way as a partial product, with the edge value *A8* being equal to *A7* and with an additional inverse operation.

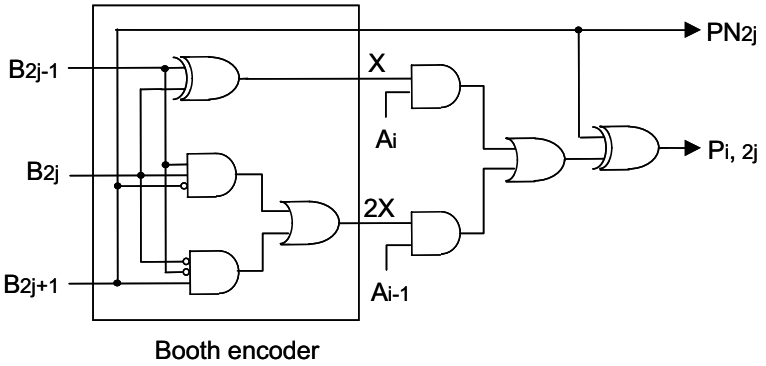


Fig. 4.26 Circuit diagram of Booth encoder and partial-product generator.

Table 4.1 Generation of partial products.

B_{2j+1}	B_{2j}	B_{2j-1}	C_{2j} (decimal)	X	2X	PN_{2j}	$P_{i,2j}$	$P_{8,2j}$
0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	A_i	$\overline{A_7}$
0	1	0	1	1	0	0	A_i	$\overline{A_7}$
0	1	1	2	0	1	0	$\overline{A_{i-1}}$	$\overline{A_7}$
1	0	0	-2	0	1	1	$\overline{A_{i-1}}$	A_7
1	0	1	-1	1	0	1	$\overline{A_i}$	A_7
1	1	0	-1	1	0	1	A_i	A_7
1	1	1	0	0	0	0	0	0

The circuit that adds up the partial products consists of a Wallace-tree block and a carry-propagation adder block. The Wallace-tree block performs sums in parallel; it consists of a half adder, a full adder and a 4-2 adder, which is a cascade of two full adders, as shown in the inset of Fig. 4.25.

If we design this multiplier using the triple-V_{th} MTCMOS/SOI circuit scheme, we need to know where the critical path runs and which logic blocks are on it because those blocks must be made with low-V_{th} MOSFETs.

For the small number of multiplications in Fig. 4.25, it is easy for a circuit designer to find the critical path. That is, the critical path of the Wallace tree is the carry part; so the 4-2 adder, which is the main component of that part, should be made with low-V_{th} MOSFETs. However, as the number of multiplications increases, the Wallace tree becomes more complicated, making it harder to manually find the critical path. The solution is an automatic search tool, such as the one used to design the 54 × 54-bit multiplier described below.

Figure 4.27 shows a block diagram of a 54 × 54-bit multiplier. It consists of a second-order Booth encoder, a partial-product generator, a Wallace tree, and a 108-bit adder. The encoder and generator are on the critical path and are made with low-V_{th} MOSFETs. The Wallace tree and the adder are made with low- and medium-V_{th} MOSFETs because some of the blocks they contain are on the critical path and some are not. However, it is difficult to find the critical path in the Wallace tree manually and thus make the proper threshold voltage assignments, because the circuit paths related to sum and carry signals are complicated.

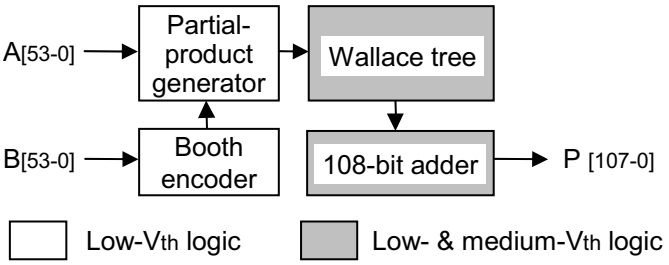


Fig. 4.27 Block diagram of 54 × 54-bit Booth-encoder and Wallace-tree multiplier.

So, we use an EDA tool [4.9], which automatically assigns low- and medium-V_{th} MOSFETs to the proper logic gates. Figure 4.28 illustrates the optimization procedure (left) and the distribution of the delay times among the paths of the circuit before and after optimization (right). The optimization starts with a circuit consisting of all low-V_{th} CMOS logic gates. Then, some low-V_{th} gates are replaced with medium-V_{th} ones under the condition that the maximum delay time remains the same. Finally, the optimized circuit is obtained.

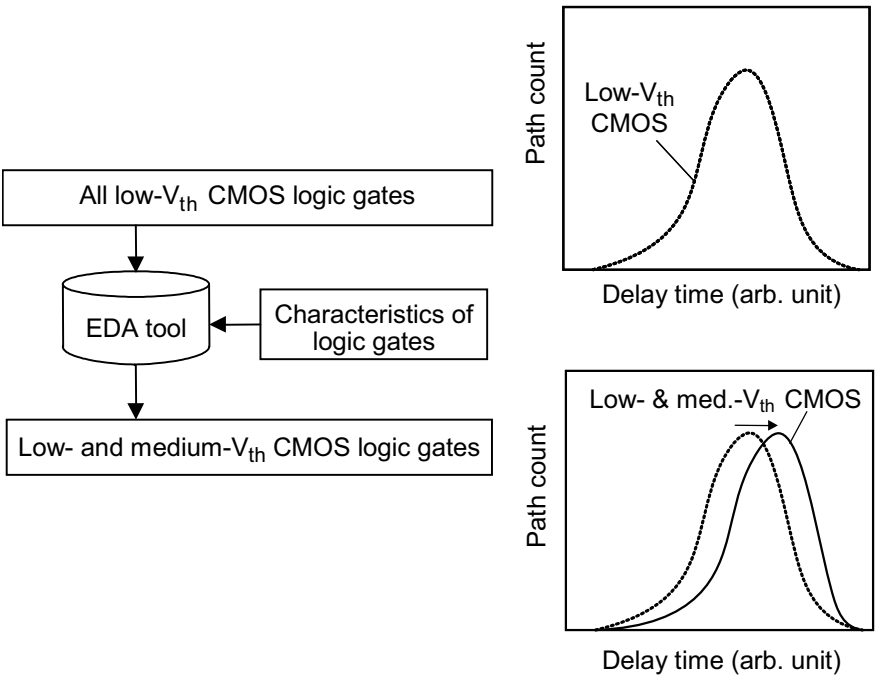


Fig. 4.28 Multi-V_{th} optimization with EDA tool.

The EDA tool was used to optimize the 54 × 54-bit multiplier for 1-V operation. Figure 4.29 shows the resulting delay-time distribution. The optimization shifts the distribution towards higher values without increasing the maximum value. The reduction in leakage current obtainable with this optimization is shown in Fig. 4.30. In the optimized multiplier, the number of low-V_{th} logic gates is 5% of the number of medium-V_{th} ones; and the leakage current is half that of an all-low-V_{th} circuit.

To verify the effectiveness of this design method, a 54 × 54-bit multiplier was designed and fabricated on a 0.25-μm MTCMOS/SOI process [4.9]. The absolute values of the threshold voltages of low- and medium-V_{th} MOSFETs are 0.1 V and 0.2 V, respectively. The multiplier operates on a supply voltage of 0.5 V; and the power dissipation is 2.8 mW at an operating frequency of 30 MHz.

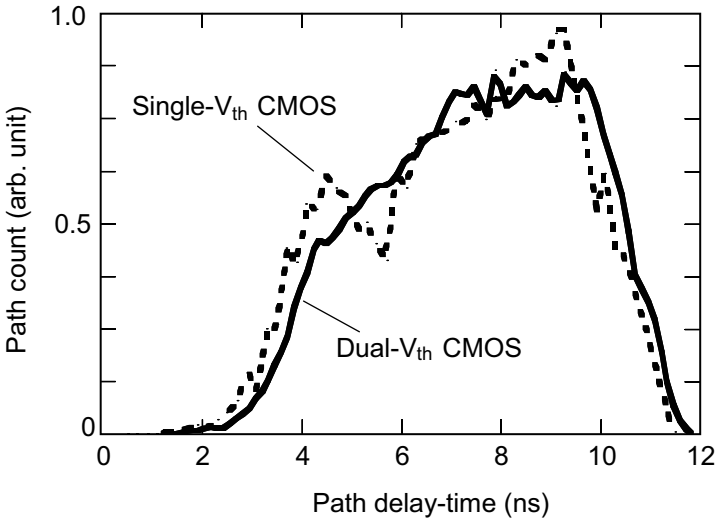


Fig. 4.29 Distribution of delay times among paths of 54 × 54-bit multiplier.

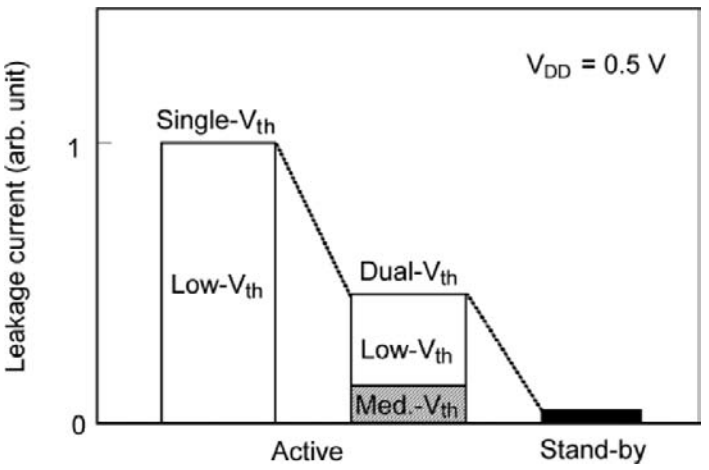


Fig. 4.30 Reduction in leakage current obtainable with multi-V_{th} CMOS circuit.

4.4.2 Wave-Pipelined Multiplier

0.5-V FD-SOI circuit design enables us to obtain an ultralow power dissipation that is around one or two orders of magnitude smaller than that of a conventional circuit with a supply voltage of 1-2 V. However, it is very difficult to obtain the same speed. For example, a 0.5-V multiplier made on a 0.25-μm FD-SOI process has an operating frequency below 50 MHz [4.9]. This is good enough for an ultralow-power system, but it is not good enough if we require almost the same performance provided by a conventional circuit running on a supply voltage of 1.5-2 V.

An interesting approach to achieving high speed is wave pipelining [4.10, 4.11]. It theoretically provides the maximum throughput by employing pipeline combination logic without latches. However, the actual throughput is limited by a number of factors, including variations in gate delay within each stage due to differences in rise and fall times, the dependence of delay on slew rate, variations in V_{DD}, and the coupling capacitance of the wiring.

Below, a wave-pipelined 8 × 8-bit multiplier is discussed as an example. The design employs a unique configuration in conjunction with a circuit design method that reduces variations in gate delay. The result is a latch-less design from input to output.

Figure 4.24 illustrates the calculation scheme. The one-bit partial product $P_{i,j}$ is obtained by ANDing the one-bit input Ai of the multiplicand A and the one-bit input B_j of the multiplier B. The nth output bit P_n is obtained by summing the $P_{i,j}$'s at each bit and the carries from lower bits. Thus, the procedure can be divided into several stages.

In our design, an nth-bit bit-sliced multiplier is composed of the following stages:

1st stage: Sum 2-bit partial products from 8-bit partial products.
2nd stage: Sum 2-bit sums from 1st stage and 2-bit carries from lower bits ((n-1)th bit) of 1st stage.
3rd stage: Sum 2-bit sums from 2nd stage and 2-bit carries from lower bits ((n-1)th bit) of 2nd stage.
mth stage: Sum 1-bit sums from (m-1)th stage at nth bit and 1-bit carry from (m-1)th stage at (n-1)th bit. For an 8 × 8-bit multiplier, m ranges from 4 to 15.

Figure 4.31 shows an example of the bit-slice calculations at P^7 (n = 7) from the 1st to the 15th stages. The stages from the 4th onward deal only with carries from lower bits; and it should be noted that there are 15 stages for an 8 × 8-bit multiplier because it is necessary for the output of P^{15} (MSB) to handle all the carries, and this is true for all the bit-slices in the wave pipeline scheme.

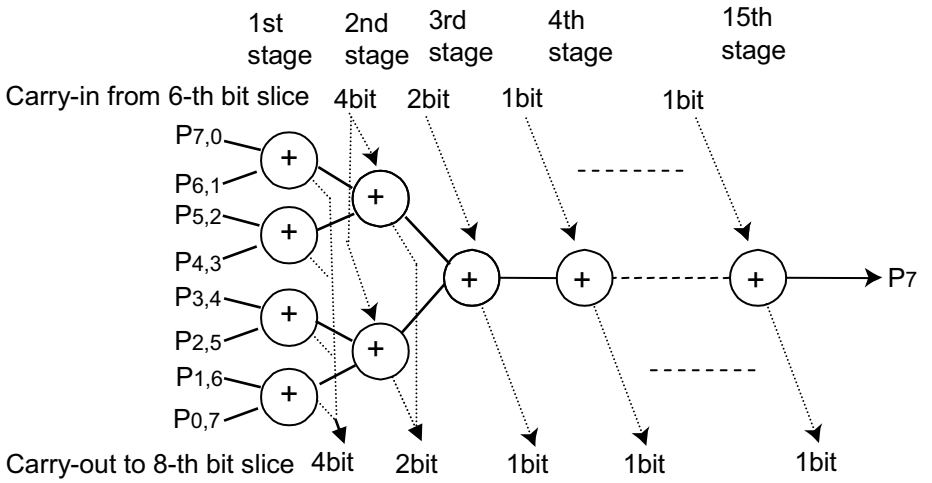


Fig.4.31 Partial-product generation and bit-slice sum process for 7th bit slice, in which P^7 is generated.

Figure 4.32 shows a schematic of a 1-bit-slice multiplier. It is composed of four half adders combined with two 2-way ANDs in the input stage, two 4-to-2 adders, three full-adders, and 11 half adders. In this figure, the input signals IA_i and IB_i are the ith inputs from the multiplicand A and the multiplier B, respectively; the input signal $ICmk$ is the kth carry-in from the mth stage of a lower neighbor ((n-1)th bit); and the output signal OC_{mk} is the kth carry-out to the mth stage of a higher neighbor ((n+1)th bit). Thus, aligning this 1-bit slice from bit 0 to bit 15 produces an 8 × 8-bit multiplier. As shown in Fig. 4.33, this multiplier is designed by aligning 16 bit-slices in parallel, which are obtained by inputting A_0-A_7 and B_0-B_7, to yield the 16-bit product P_0-P_{15}. In this configuration, every path from the inputs (A_i/B_i) to the output (P_j) has the same number of stages.

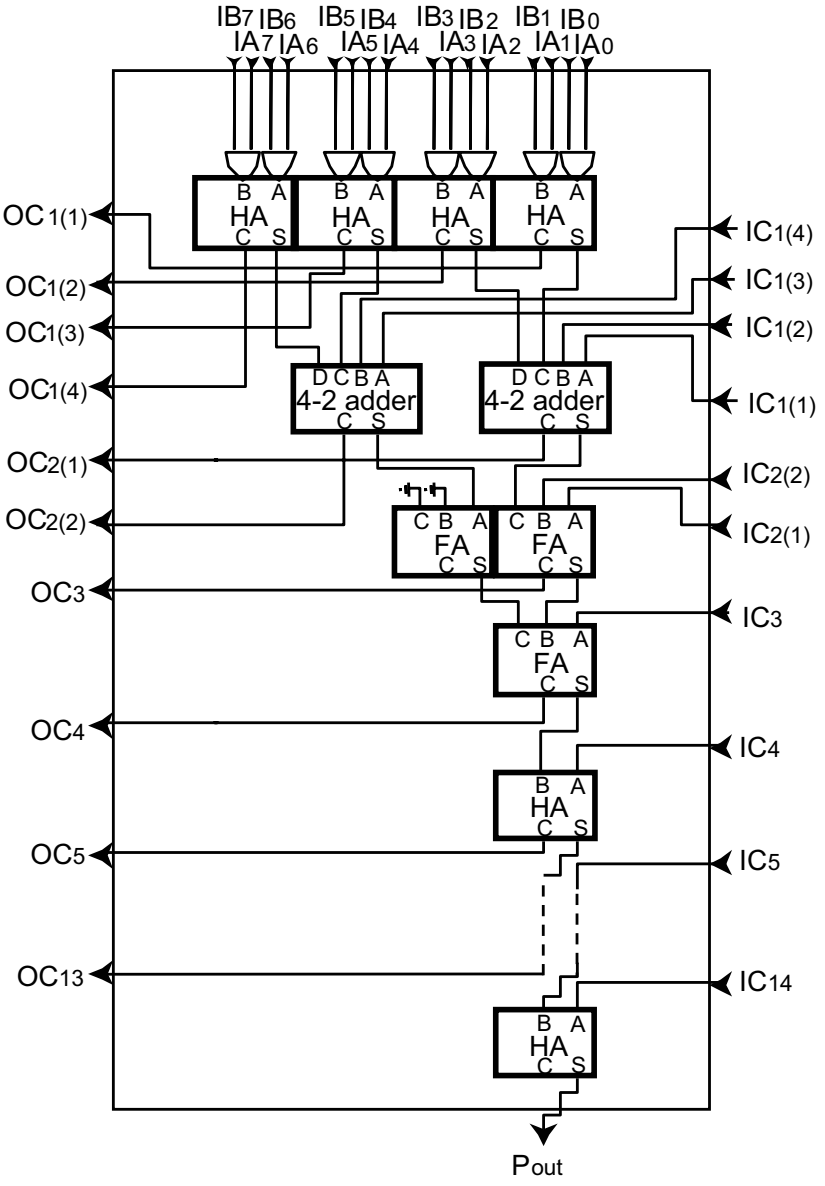


Fig 4.32 Block diagram of bit-slice design for 8×8-bit multiplier.

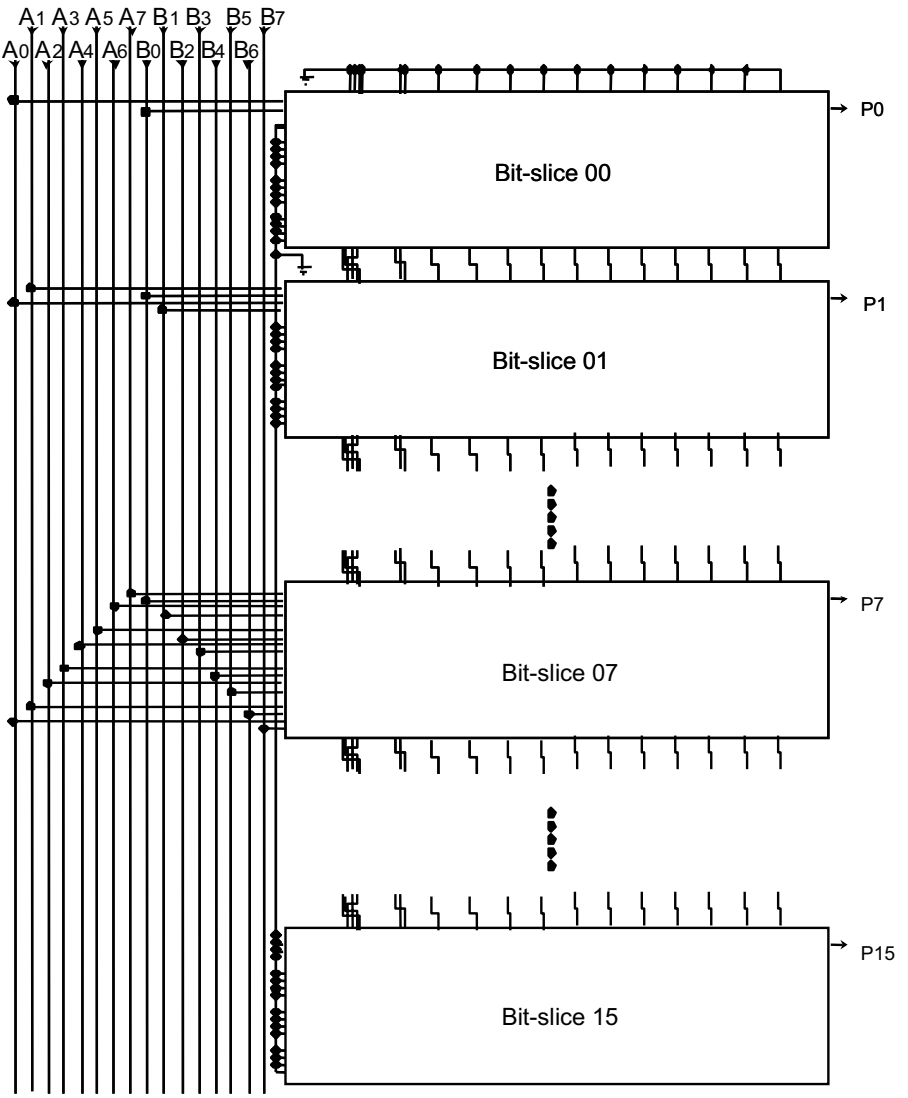


Fig. 4.33 Block diagram of 8 × 8-bit multiplier.

As mentioned before, a special circuit design is used to reduce variations in gate delay within each stage. Figure 4.34 shows a schematic diagram of a full adder (FA) composed of three true/complement buffers, ten 3-input NAND gates, two 4-input NAND gates, and four inverters. The inverters are used as buffers to reshape the output waveforms. The configuration related to the carry logic is modified from that of a conventional circuit to reduce gate delay variations. More specifically, the number of fan-ins of the NAND gates is changed from 2 to 3, and two dummy NAND gates are inserted to give the buffers the same number of fan-outs. Thus, after true/compliment generation, all the gates within a given stage have the same numbers of fan-ins and fan-outs as shown in Fig.4. 34.

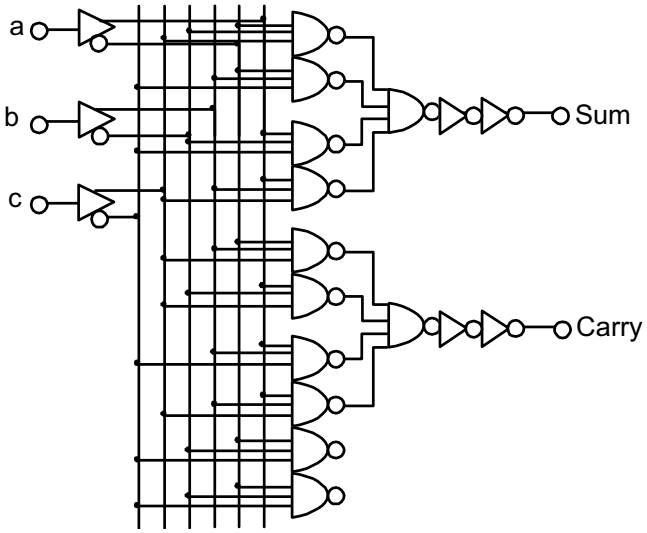


Fig. 4.34 Full-adder circuit for wave-pipelined multiplier.

Care must be taken in the layout to ensure that, for a given stage, all the paths have the same load capacitance and all the gates are the same size. Since the sum path is generally shorter than the carry path, additional wire is inserted into the sum path to give it the same wiring capacitance as the carry path.

Figure 4.35 shows a circuit schematic and the gate delay of a 3-input NAND gate designed to have little variation in gate delay between inputs and outputs.

The gate delay is almost the same for different inputs. The beta ratio of the transistors in a gate, which is defined to be the gate width of a pMOSFET (W_p) divided by that of an nMOSFET (W_n), is set so that the rise and fall times of the inputs for a given stage are almost the same. In most cases, a beta ratio of two satisfies this requirement. However, for some gates, especially those in the output buffer circuit of a full adder, the beta ratio is greater than two to increase the throughput.

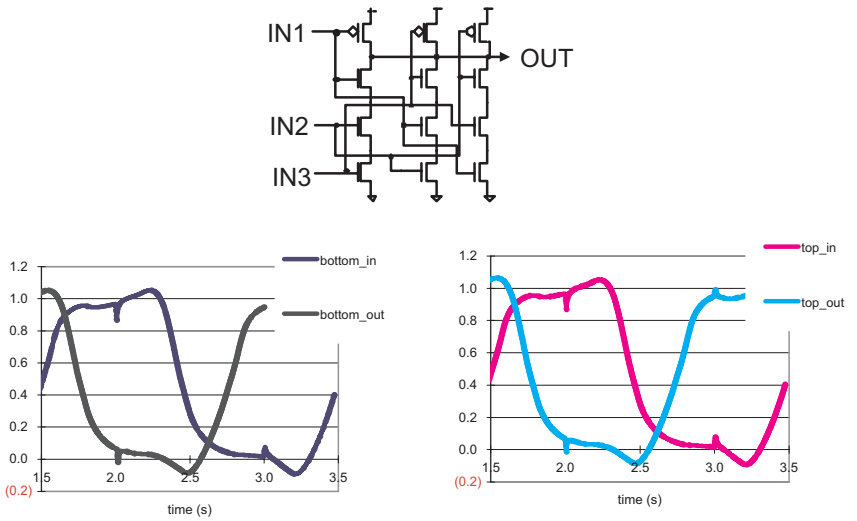


Fig. 4.35 3-input NAND gate and gate delay performance.

The true/complement generator circuit is also important in making the delay the same for both true and complement signals. It employs an interpolation method, as shown in Fig. 4.36. The OUT terminal is connected to the 1st and 3rd stage buffers, while OUTB is connected directly to the 2nd stage buffer. This design concept is also used for other internal cells, such as the half-adder, the 4-to-2 adder, and the half-adder with a 2-way NAND gate employed in the 8 × 8-bit multiplier.

An 8 × 8-bit multiplier with the above design was fabricated on a 0.25-μm FD-SOI process. The pMOSFETs and nMOSFETs had threshold voltages of V_{thp} = -0.15 V and V_{thn} = 0.15 V, respectively. These are optimized values for low-power operation at a V_{DD} of 0.5 V. Since FD-SOI devices have a subthreshold swing close to the ideal value of 60 mV/decade at room

temperature and a much smaller junction capacitance than bulk devices, they are the best choice for achieving low-power operation at a supply voltage of 0.5 V while suppressing the leakage current in the standby mode. The chip contains 46,000 devices, including those for the input and output latches and the 9,000 devices for testing. The die size is 1 mm × 3 mm.

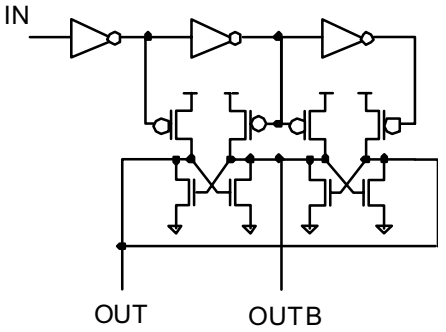


Fig. 4.36 True/complement generator circuit.

The proper operation of the circuit was verified by a comparison of test vectors using a FIFO buffer memory following the output of the multiplier. High-speed test results (Fig. 4.36) demonstrate that the chip operates at a data rate of 230 Mbps at a V_{DD} of 0.5 V, and at a data rate of 430 Mbps at a V_{DD} of 0.8 V.

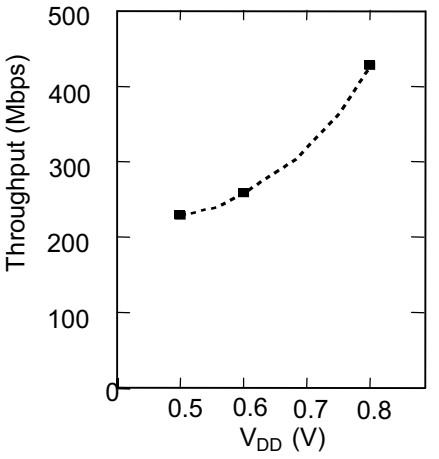


Fig. 4.37 Measured data rate vs. V_{DD}.

4.5 Memory

Figure 4.38 shows a block diagram of a CMOS static memory. It consists of CMOS memory cells in a 2^N row by 2^M column array and a peripheral circuit. The peripheral circuit is composed of an address decoder; a write circuit for input data; and a readout circuit, such as a sense amplifier and an output buffer. The array has 2^{N+M} memory cells, each of which is accessed by an address N+M bits long, with the first N bits being the row address and the rest being the column address. The row address selects one from among 2^N word lines, and the column address selects one from among 2^M bit-line pairs. There is only one cell at the intersection of a word line and a bit-line pair.

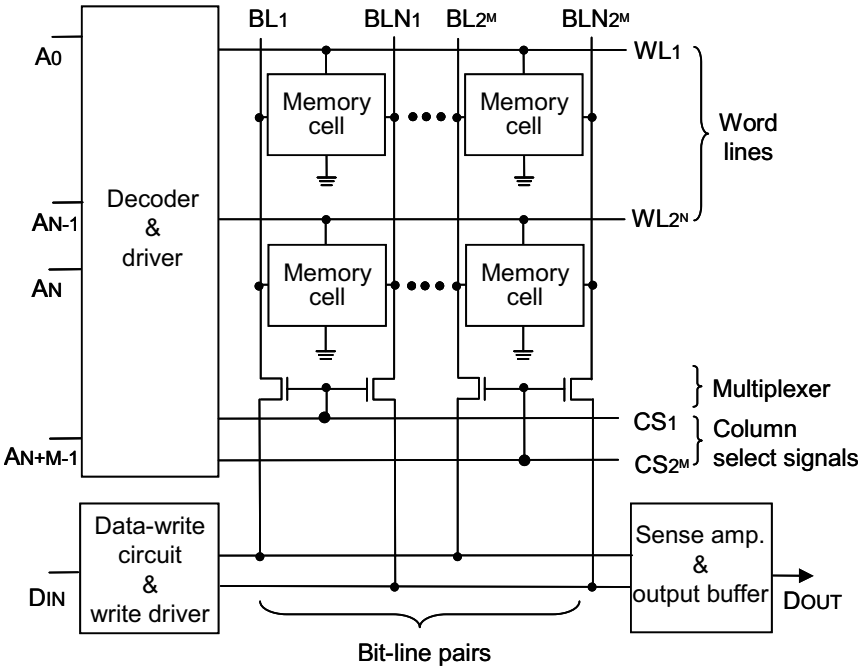


Fig. 4.38 Block diagram of SRAM.

Figure 4.39 shows a circuit diagram of a memory cell and the associated peripheral circuit. A memory cell has 6 transistors and consists of cross-coupled CMOS inverters and access transistors. The access transistors connect a cell to the word line WL_i and the bit-line pair BL_i and BLN_i. A write circuit is also

connected to the bit-line pair through a multiplexer (bit-line selector). In a write operation, the write circuit sets either BL_i or BLN_i to the GND level and the other one to $V_{DD} - V_{th}$. When word line WL_i is selected, the access transistors store the input data in the cell. In a read operation, the write circuit is set to the high-impedance state; and a precharge circuit connected to the bit-line pair precharges the bit lines to $V_{DD} - V_{th}$. When the word line is selected, the stored data are read out to the bit lines. Then, these data are generated on the data line through the multiplexer.

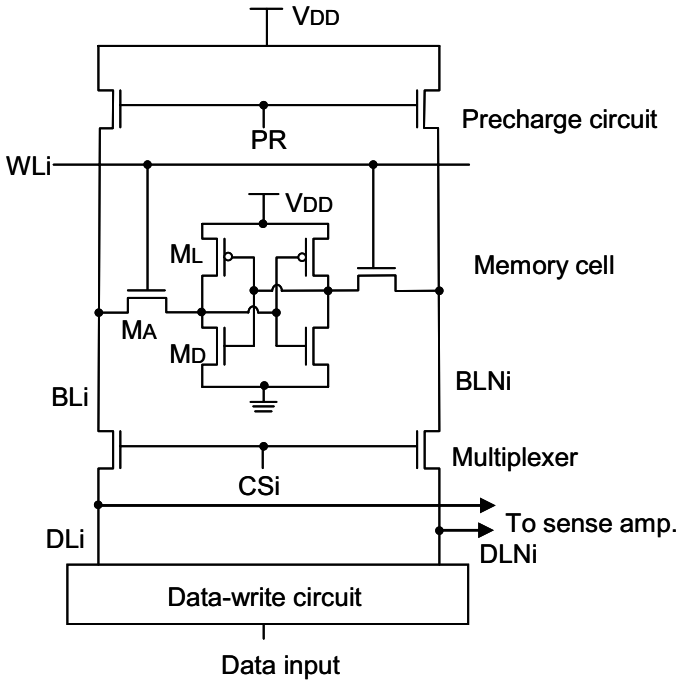


Fig. 4.39 CMOS memory cell and its direct peripheral circuit.

4.5.1 Design of Ultralow-Voltage Memory Cell

Robust operation of a memory cell is difficult to achieve at an ultralow supply voltage below 1 V because the noise margin of a cell decreases in proportion to the supply voltage. So, the design must take the noise margin into account.

The static-noise margin (SNM) [4.12] is a useful parameter in the design of ultralow-voltage memory cells. However, the SNMs for read and write operations behave quite differently in that, as one increases, the other decreases. The problem is how to balance them.

Figure 4.40 shows a model for estimating the SNM for a read operation [4.12]. The voltage sources E_r are sources of static noise, which is a DC disturbance, such as offsets and mismatches due to process variations and variations in operating conditions. The SNM of a memory cell is defined to be the maximum value of E_r. It is obtained by drawing curves of the input-output characteristics of the cross-coupled inverters Inv. A and Inv. B, and finding the largest possible square that will fit between them.

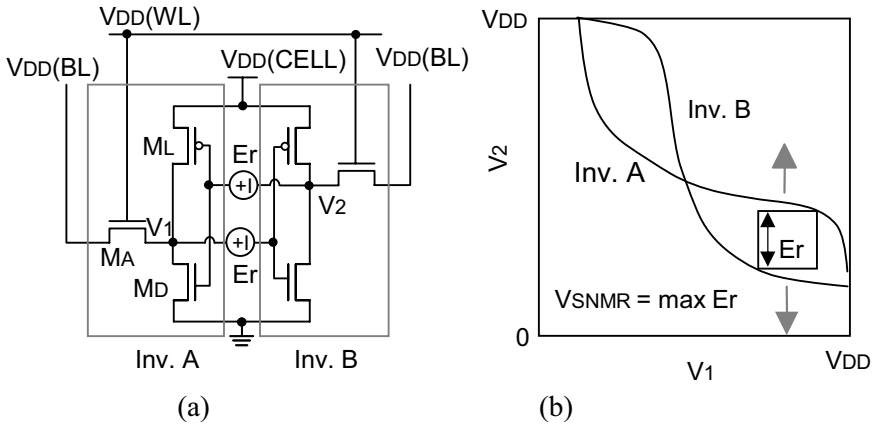


Fig. 4.40 Model for estimating static-noise margin of memory cell for readoperation: (a) circuit diagram and (b) estimation procedure.

Fig. 4.41 shows a model for estimating the SNM for a write operation [4.13]. E_w indicates the sources of static noise. In this case, the SNM of a memory cell is defined to be the minimum value of E_w. It is obtained by finding the smallest possible square between the curves for the input-output characteristics of the cross-coupled inverters Inv. C and Inv. D in the region $V_2 < V_1$. To do this, we first draw a square between the curves with the upper left corner touching the line $V_1 = V_2$, and then move the square downwards, keeping two corners on the curves. Then, we choose the smallest from among all the squares drawn.

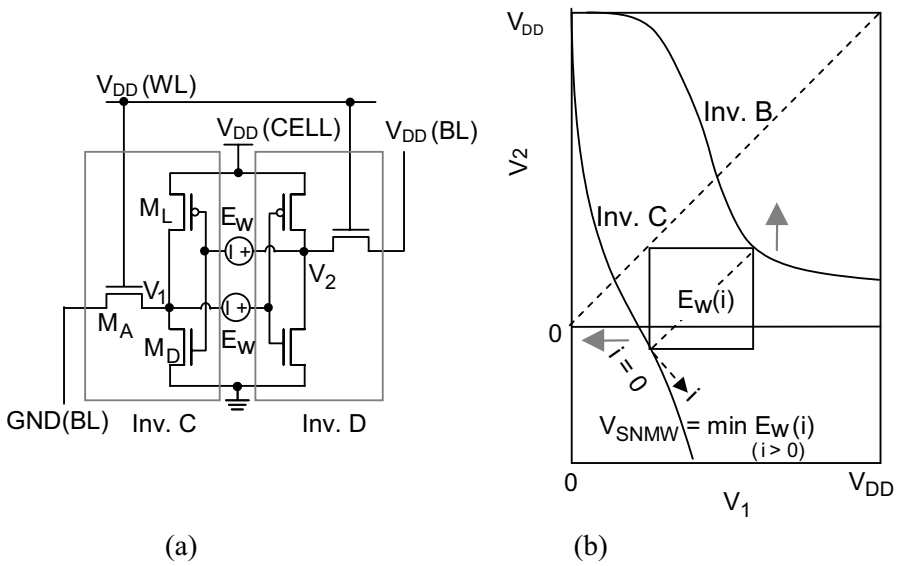


Fig. 4.41 Model for estimating static-noise margin of memory cell for write operation: (a) circuit diagram and (b) estimation procedure.

Considering the SNM models for both read and write operations, the following measures are required to increase the noise margin of an ultralow-voltage memory cell.

A. Read operation

For Inv. A:

The gradient of the inverter characteristics at the logic threshold voltage of the inverter must be steep ($\partial V_1/\partial V_2 = \infty$).

=> *The threshold voltages of the driver transistor (M_D) and the load transistor (M_L) must be reduced.*

The logic threshold voltage of the inverter must be increased and set close to $V_{DD}/2$.

=> *The current drivability of the load transistor must be set close to that of the drive transistor ($[\beta(M_L)/\beta(M_D)] = 1$).*

For Inv. B:

The output voltage of the inverter at an input voltage of V_{DD} must be decreased.

=> *The current drivability of the driver transistor must be set larger than that of the access transistor ($[\beta(M_D)/\beta(M_A)] > 1$).*

B. Write operation
For Inv. C:
The output voltage of the inverter at an input voltage of 0 V must be decreased.
=> *The current drivability of the access transistor must be set much larger than that of the load transistor ([$\beta(M_L)/\beta(M_A)$] << 1).*
=> *The low level of the bit line must be boosted with a negative bias.*
For Inv. B:
The output voltage of the inverter at an input voltage of V_{DD} must be increased.
=> *The current drivability of the access transistor must be set larger than that of the driver transistor ([$\beta(M_A)/\beta(M_D)$] >1).*
=> *The voltage to the word line must be boosted over V_{DD} to increase the current drivability of the access transistor.*
=> *Either the GND level of Inv. B or the high level V_{DD}(BL) of the bit line must be boosted [4.14].*

Since the SNMs for read and write operations have opposite tendencies, the current-drivability ratios $\beta(M_D)/\beta(M_A)$ and $\beta(M_L)/\beta(M_A)$ must be adjusted together. In practice, the access transistor is designed with the minimum feature size, and the feature size of the driver transistor is set so that $\beta(M_D)/\beta(M_A) > 2$. Then, the feature size of the load transistor is optimized so that the two SNMs are in balance.

With bulk-Si devices, if the threshold voltage of an ultralow-voltage memory cell is reduced to obtain a constant noise margin, the leakage current increases exponentially. One way to suppress the leakage current is to use fully-depleted SOI MOSFETs, which are also used in logic circuits. Another is to employ a multi-V_{th} circuit scheme. The next section describes an SRAM scheme that employs both methods.

4.5.2 MTCMOS/SOI SRAM Scheme

In the MTCMOS/SOI SRAM scheme (Fig. 4.42) [4.15], the power-switch transistor is off in the sleep mode, and the data in the low-V_{th} CMOS circuits connected to the virtual supply line are lost. So, a memory cell connected to the supply line is required to store the data. The decoder circuit and the readout circuit of the SRAM are composed of MTCMOS circuits, just like digital LSIs; and the memory cells consist of multi-V_{th} FD-SOI MOSFETs for ultralow-voltage operation.

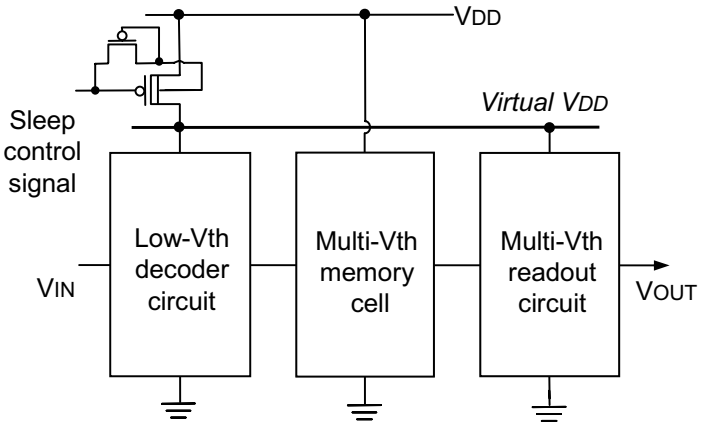


Fig. 4.42 Ultralow-voltage MTCMOS/SOI memory scheme.

4.5.3 Multi-V_{th} Memory Cell

The multi-V_{th} memory cell in Fig. 4.43 is based on a dual-port scheme, which has separate write and read ports; and the read port is composed of low-V_{th} MOSFETs. In a conventional single-port high-V_{th} memory cell made with SOI devices, even if the supply voltage is reduced to 0.5 V, data is written by boosting the bit-line with a negative bias. But a high-V_{th} memory cell generates errors during a read operation. So, four low-V_{th} MOSFETs are added to a conventional cell to improve the read performance. Even so, there is no increase in the leakage current in the stand-by mode. This is because the low-V_{th} MOSFETs are not connected to the high-V_{th} data-storage nodes; and in the stand-by mode, their drains, which are connected to the bit lines, are set to the ground level by the high-V_{th} multiplexer.

Figure 4.44 shows the SNMs of single- and multi-V_{th} memory cells during a read operation. They both drop as the supply voltage decreases. But the noise margin of a multi-V_{th} cell is more than twice that of the single-V_{th} one because the read port of the multi-V_{th} cell is not affected by the data-storage node.

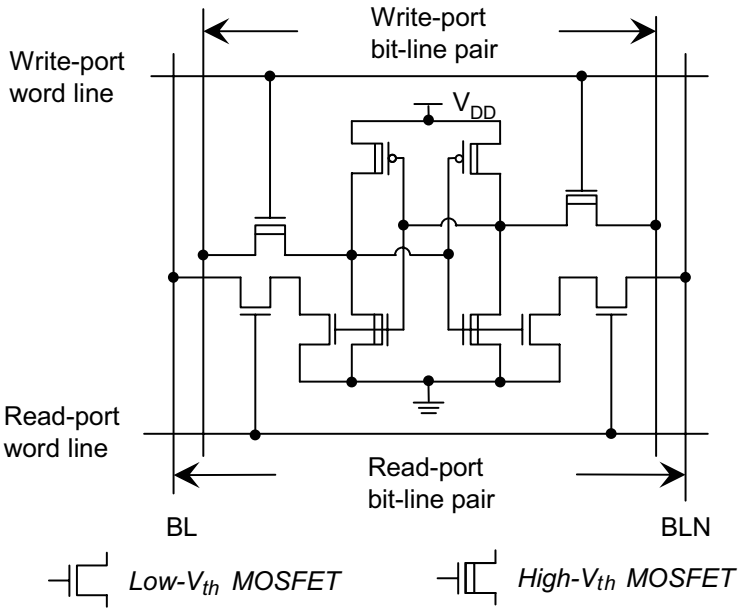


Fig. 4.43 Multi-V_{th} dual-port memory cell.

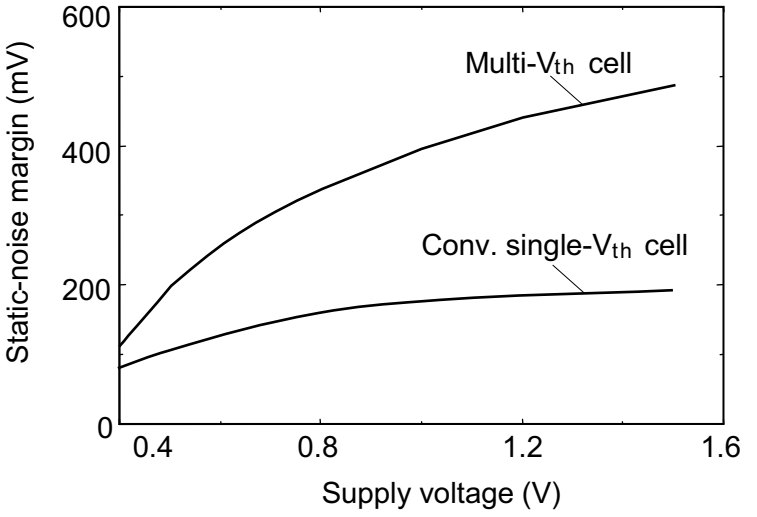


Fig. 4.44 Static-noise margins of single-V_{th} and multi-V_{th} memory cells.

4.5.4 Multi-V_{th} Readout Circuit

The readout circuit for multi-V_{th} memory cells (Fig. 4.45) consists of a low-V_{th} bit-line equalizer, a high-V_{th} multiplexer, a low-V_{th} precharge circuit, and a multi-V_{th} sense amplifier.

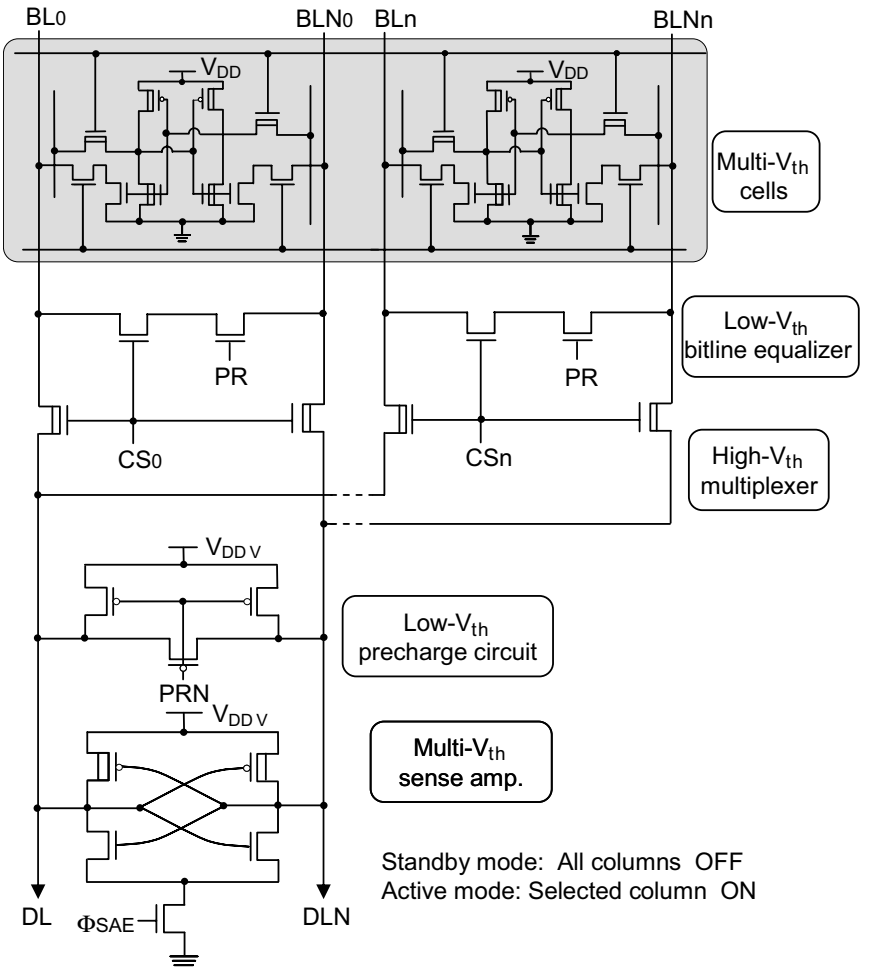


Fig. 4.45 Selective precharge scheme using high-V_{th} multiplexer and multi-V_{th} sense amplifier.

The key part is the high-V_{th} multiplexer. It is composed of a high-V_{th} nMOSFET transmission gate, and thus provides low power and high speed. The equivalent circuit is shown in Fig. 4.46.

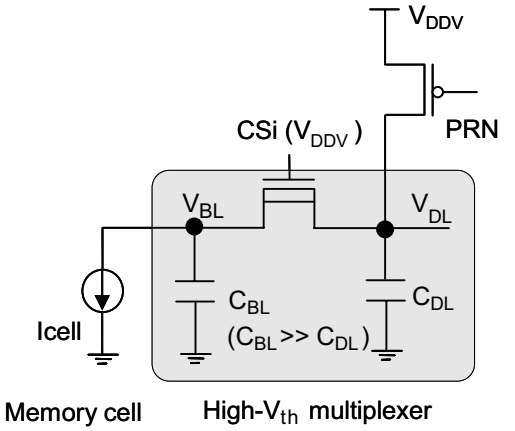


Fig. 4.46 Equivalent circuit of high-V_{th} multiplexer.

Use of a high-V_{th} multiplexer has two advantages. The first is that it reduces the power dissipated by the readout circuit. Most of that power is used to precharge and discharge the large bit-line capacitance. The power dissipation is given by

$$P_{BL} = \frac{1}{2} C_B (V_{DD} - V_{th})^2 f , \tag{4.15}$$

where C_B is the bit-line capacitance, V_{DD} -V_{th} is the precharge level set by the nMOSFET transmission gate, and f is the operating frequency. Since the power dissipation is proportional to the square of the precharge level, reducing this level by using high-V_{th} nMOSFETs lowers the amount of power needed.

The second advantage is that the multiplexer operates at high speed because it acts as a pre-amplifier due to a charge-sharing operation, thus accelerating the amplification by the sense amplifier that follows.

The pre-amplification mechanism can be explained as follows. The bit line and data line are initially precharged to voltages of $V_{BL} = V_{DD} - V_{th}$ and $V_{DL} = V_{DD}$, respectively. When one memory cell is selected and its access transistor turns on, the voltage of the bit line, which has a large capacitance, slowly discharges. Once V_{BL} drops below the trigger voltage $V_{DD} - V_{th}$, the multiplexer turns on. Then, charge redistribution occurs, which brings V_{DL} close to V_{BL}.

From the formula for charge redistribution, we derive the following equation:

$$C_{DL}\left(\frac{\Delta V_{DL}}{\Delta t}\right) = C_{BL}\left(\frac{\Delta V_{BL}}{\Delta t}\right) = I_{cell}. \tag{4.16}$$

So, the output voltage of the multiplexer (ΔV_{DL}) is given by

$$\Delta V_{DL} = \left(\frac{C_{BL}}{C_{DL}}\right)\Delta V_{BL}. \tag{4.17}$$

Since the bit-line capacitance is much larger than the data-line capacitance, the multiplexer acts as a preamplifier.

Simulations based on 0.35-μm MTCMOS/SIMOX technology were used to examine the effect of the high-V_{th} multiplexer on the performance of the SRAM circuit. The power-dissipation characteristics of the multiplexer in Fig. 4.47 show that increasing V_{th} reduces the power dissipation. More specifically, increasing it from 0.15 to 0.35 V, reduces the power dissipation by 60% at a V_{DD} of 1 V and by 80% at a V_{DD} of 0.5 V.

The delay-time characteristics of the multiplexer are shown in Fig. 4.48. The capacitance of a bit line connected to multi-V_{th} memory cells composed of SOI devices, which have a small junction capacitance, is smaller than that of one connected to memory cells composed of bulk devices. For a row of 512 memory cells, the bit-line capacitance is 0.4 pF for SOI and 0.8 pF for bulk. As a result, at a V_{DD} of 0.5 V, the delay time of the multiplexer in the SOI SRAM is less than 75% that of one in a bulk SRAM.

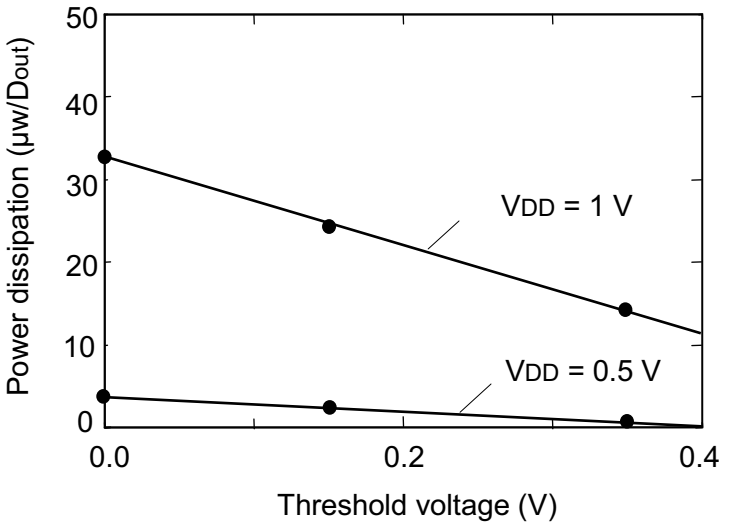


Fig. 4.47 Power dissipation vs. threshold voltage for multiplexer.

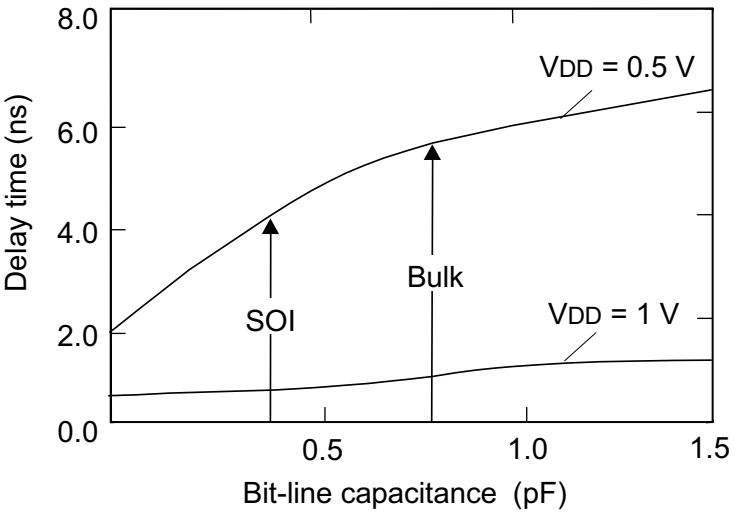
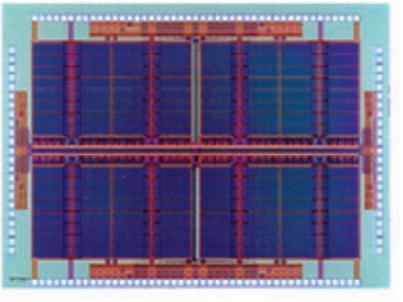


Fig. 4.48 Power dissipation vs. threshold voltage for multiplexer.

To verify the effectiveness of the MTCMOS/SOI SRAM scheme with multi-V_{th} memory cells, a 256-Kb SRAM was designed and fabricated on a 0.35-μm

MTCMOS/SIMOX process. The gate oxide was 7 nm thick; the active Si layer, 50 nm thick; and the buried oxide, 100 nm thick. The absolute values of the threshold voltages of the low- and high-V_{th} MOSFETs were 0.15 and 0.35 V. A microphotograph and the specifications of the SRAM are shown in Fig. 4.49. A memory cell is 30% larger than a conventional single-port cell. The maximum operating frequency is 22 MHz at a supply voltage of 0.5 V. The power dissipation is 1.1 mW in the active mode and less than 0.1 μW in the sleep mode.



(a)

Specifications	
Process technology	0.35-μm, 3-metal, MTCMOS/SOI
Supply voltage	0.5 V for memory core 1.4 V for I/O interface
Threshold voltage	$\|V_{th}L\|$ = 0.15 V $\|V_{th}H\|$ = 0.35 V
Organization	32 Kw x 8 bit
Chip size	7.8 mm x 4.6 mm
Memory cell size	2.8 μm x 18.8 μm
Maximum cycle time	22 MHz
Power dissipation	1.1 mW (@10 MHz) < 1 μW in sleep mode

(b)

Fig. 4.49 256-Kbit MTCMOS/SOI SRAM: (a) microphotograph and (b) specifications.

4.6 Frequency Divider

When MTCMOS/SOI technology is applied to the design of ultrafast LSIs operating at speeds of 1 GHz or more, such as frequency dividers, the most important point is the threshold voltage of the low-V_{th} CMOS circuits. It can be set lower than for digital logic LSIs because the operating gates of ultrafast LSIs have a large activity factor which means that the ratio of the dynamic to the static power dissipation is large.

4.6.1 CMOS Frequency Divider

The CMOS/SOI frequency divider with a toggle flip-flop (TFF) circuit in Fig. 4.50 employs a dual-rail scheme to achieve both high speed and robust operation at an ultralow supply voltage.

Figure 4.51 shows how maximum operating frequency depends on the threshold voltage of a TFF fabricated on a 0.25-μm MTCMOS/SOI process [4.16]. The characteristics of a CMOS/bulk circuit with the same design rule are also shown for comparison. As the threshold voltage drops, the maximum operating frequency improves for both circuits; but when it becomes negative, the degree of improvement gradually becomes smaller.

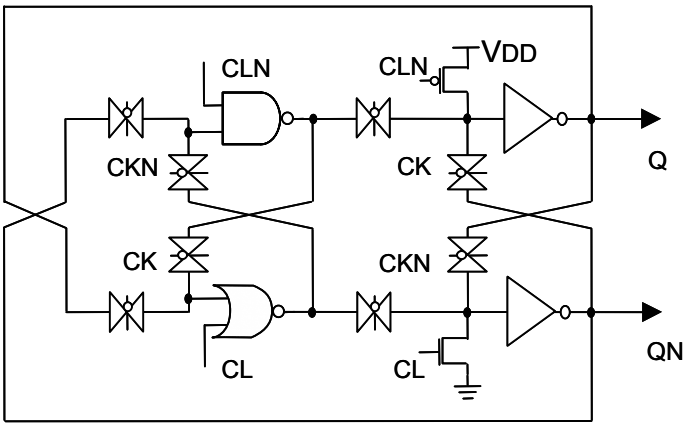


Fig. 4.50 CMOS frequency divider with dual-rail toggle flip-flop (TFF) circuit.

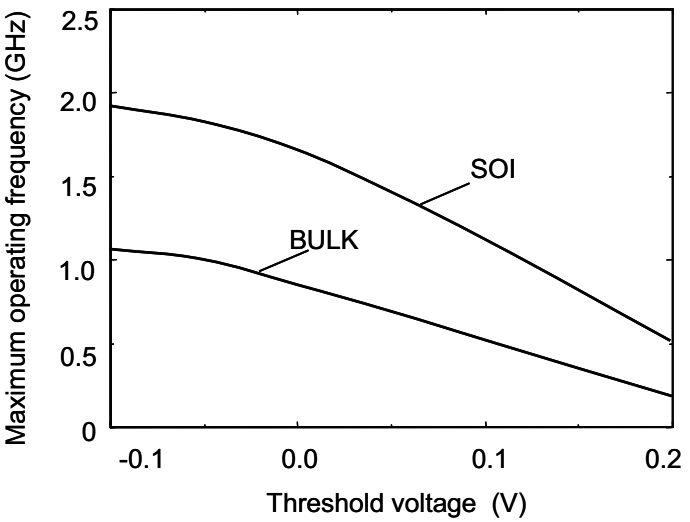


Fig. 4.51 Maximum operating frequency vs. threshold voltage for SOI and bulk CMOS dual-rail TFFs.

To find out why this happens, the delay time of CMOS inverters was estimated. The results are shown in Fig. 4.52, along with the rise and fall times of the output signal, which correspond to the slew rate. For a bulk device, reducing the threshold voltage improves both the delay time and the slew rate. In contrast, for an FD-SOI device, the slew rate is almost constant in the positive threshold voltage region due to the feed-forward effect of the CMOS inverter [4.17].

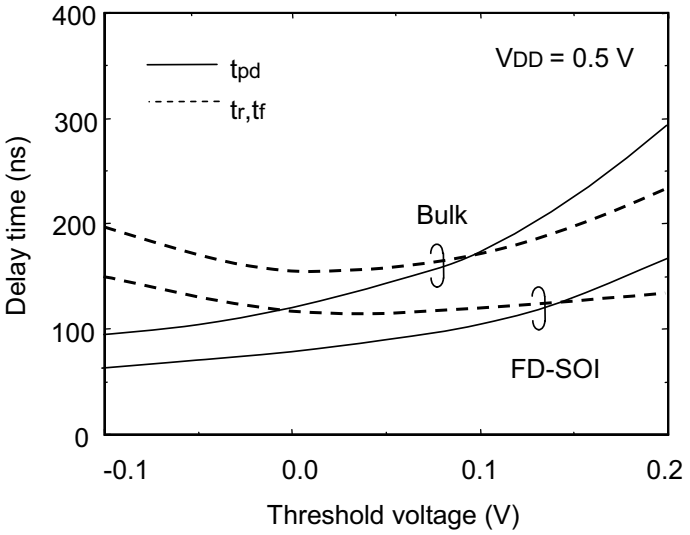


Fig. 4.52 Delay time (t_{pd}) and slew rate (t_r, t_f) vs. threshold voltage for FD-SOI and bulk CMOS inverters.

The feed-forward effect is illustrated in Fig. 4.53. Since an FD-SOI device has a small junction capacitance, the output capacitance of a CMOS/SOI circuit is small; the value is comparable to that of the input/output coupling capacitance. As a result, the coupling capacitance causes the output of a CMOS circuit to either exceed the supply voltage or drop below the ground level. This is the feed-forward effect. It increases the delay time, but delays the fall and rise of the output, and keeps the slew rate of the output steep when the threshold voltage is positive. In consequence, a CMOS/SOI circuit is faster than a bulk CMOS one. But at negative threshold voltages, the feed-forward effect is suppressed due to the large leakage current of the MOSFETs; and so the delay time of the CMOS/SOI circuit is close to that of the bulk one. This means that, for a CMOS/SOI circuit, the threshold voltage should be set close to 0 V.

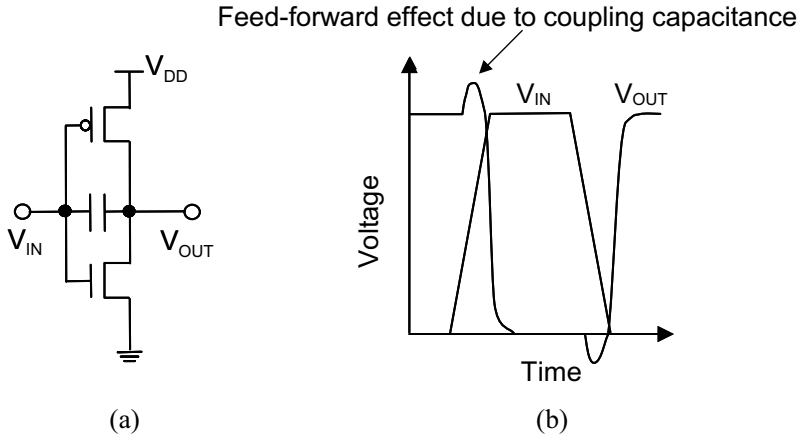
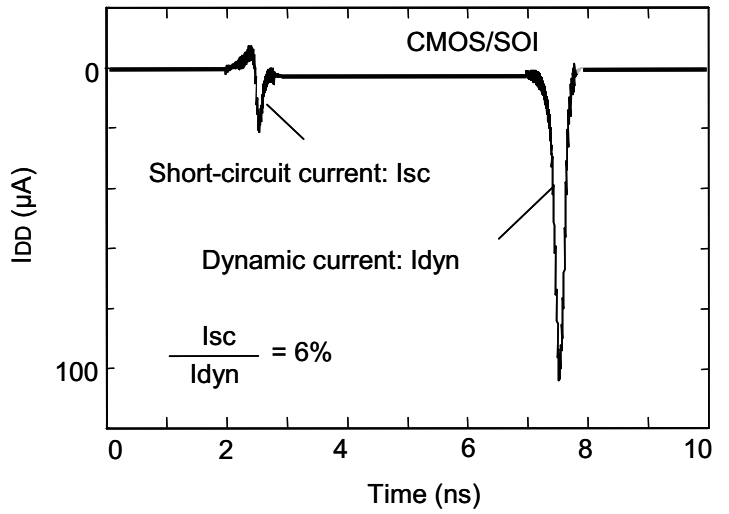


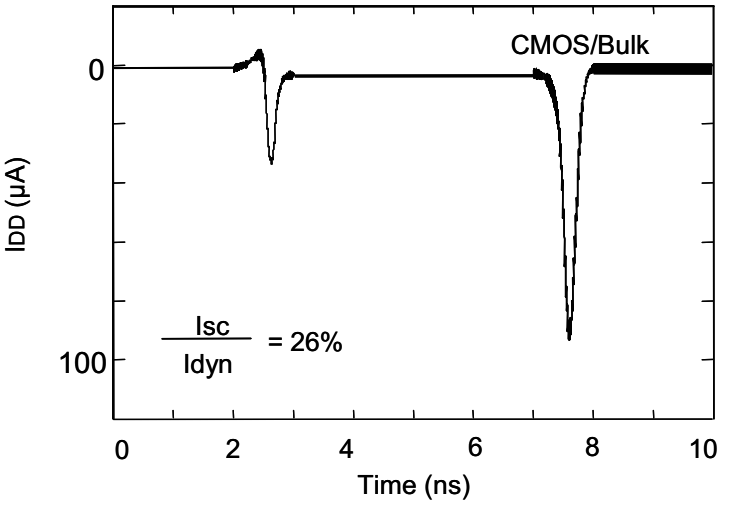
Fig. 4.53 Feed-forward effect in CMOS/SOI circuit. (a) Equivalent circuit of CMOS inverter. (b) Increase or decrease in output voltage due to feed-forward effect.

Another advantage of a zero-V_{th} CMOS/SOI circuit is low power dissipation. Since the circuit has a steep slew rate due to the feed-forward effect, there is no increase in the short-circuit power dissipation, even if the threshold voltage is 0V. The characteristics of the short-circuit current of a zero-V_{th} CMOS/SOI circuit are shown in Fig. 4.54 along with those of a conventional zero-V_{th} CMOS/bulk circuit with the same design rule. The short-circuit current was estimated from the current I_{DD} that flows through the pMOSFET.

When the input of the CMOS circuit changes from the LOW to the HIGH level, the short-circuit current is estimated from I_{DD} because the discharging current for the output capacitance flows through the nMOSFET. In contrast, the charging current for the output capacitance flows through the pMOSFET. So, I_{DD} represents the dynamic current required to charge the output capacitance. The ratio of the measured short-circuit current to the dynamic current is 6% for the CMOS/SOI circuit and 26% for the CMOS/bulk circuit. This shows that the CMOS/SOI circuit suppresses the short-circuit current.



(a)



(b)

Fig. 4.54 Characteristics of short-circuit current of zero-V_{th} CMOS/SOI and CMOS/bulk circuits.

4.6.2 ED-MOS Frequency Divider

To further improve the performance of ultrahigh-speed LSIs, we use an ED-MOS circuit [4.18], which combines enhancement- and depletion-mode nMOSFETs. Figure 4.55 compares ED-MOS circuits and a conventional CMOS circuit.

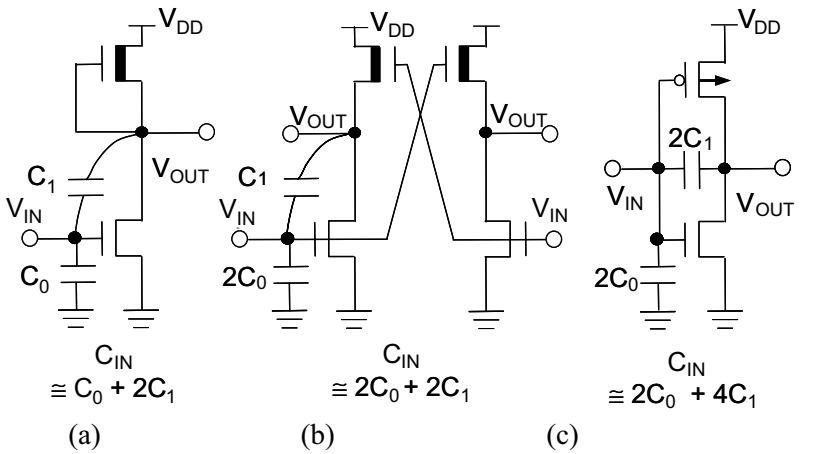


Fig. 4.55 Ultrahigh-speed SOI circuits. (a) ED-MOS circuit. (b) Differential ED-MOS circuit. (c) Conventional CMOS circuit.

Both single- and dual-rail ED-MOS circuits provide much higher operating speeds than the CMOS circuit, because ED-MOS circuits have a small input/output coupling capacitance and because the input load capacitance is smaller than that of the CMOS circuit. The input load capacitance of each circuit is also shown in the figure. If we let the gate-source capacitance of the driver nMOSFET be C_0 and the gate-drain capacitance be C_1, then the input load capacitance of a single-rail ED-MOS circuit is $C_0 + 2C_1$. This is because the contribution of the input/output coupling capacitance, that is, the gate-drain capacitance, C_1, must be counted twice due to the Miller effect [4.17]. For the dual-rail ED-MOS circuit, if we let the gate-drain capacitance of the depletion-mode nMOSFET be C_0, then the input load capacitance is $2C_0 + 2C_1$. The gate-source capacitance of the depletion-mode nMOSFET must not be included in the input load capacitance because the nMOSFET acts as a source-follower circuit. On the other hand, for the conventional CMOS circuit,

if the gate-source and gate-drain capacitances of the pMOSFET are the same as those of the nMOSFET, the input/output coupling capacitance is $2C_1$ and the input load capacitance is $2C_0 + 4C_1$. So, the ED-MOS circuits have smaller input load capacitances than the CMOS circuit, which yields a higher operating speed.

However, since an ED-MOS circuit is a ratioed circuit, it is necessary to keep the conductance ratio of each MOSFET constant in order to obtain ultrahigh-speed operation over a wide range of supply voltages. A fully-depleted SOI device makes it possible to adjust the conductance ratio by using a substrate bias. The structure of a fully-depleted SOI device is shown in Fig. 4.56.

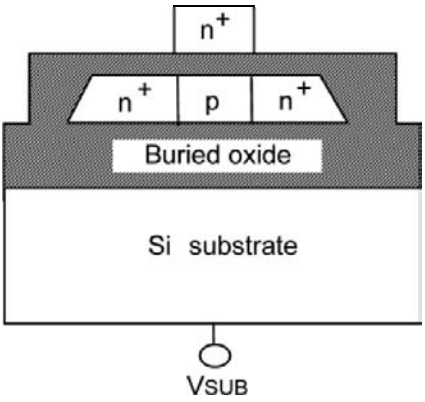


Fig. 4.56 Structure of fully-depleted SOI device.

Figure 4.57 shows the simulated dependence of threshold voltage on channel doping concentration for an nMOSFET. When the threshold voltage is negative, it does not depend on the doping concentration and can be controlled by the substrate bias. But when the threshold voltage is positive, it is determined by the doping concentration; so, the influence of the substrate bias on the threshold voltage is very small. For an ED-MOS/SOI circuit composed of both depletion-mode and enhancement-mode MOSFETs, the V_{th} shift of the depletion-mode MOSFETs due to the substrate bias is larger than that of the enhancement-mode MOSFETs. This enables us to adjust the conductance ratio of each MOSFET based on the difference between the V_{th} shifts.

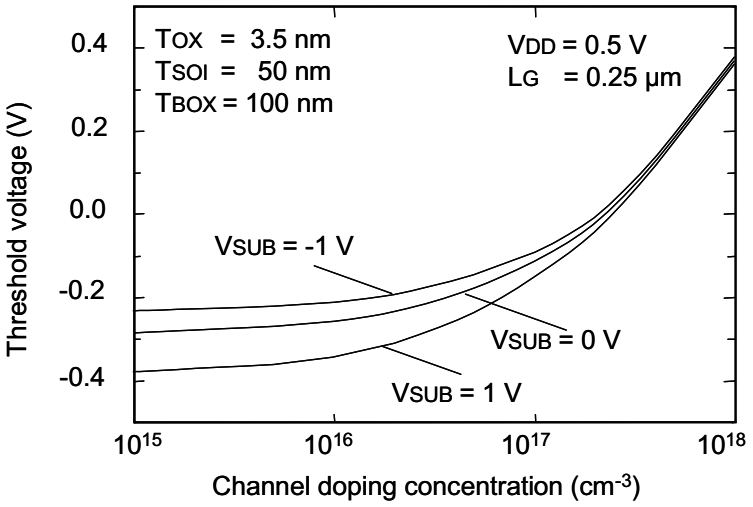


Fig. 4.57 Comparison power efficiency of E/D-MOS/SOI TFF and conventional frequency dividers.

The dual-rail ED-MOS frequency divider [4.19] with a trigger flip-flop (TFF) in Fig. 4.58 is composed of a push-pull ED-MOS logic circuit, a depletion-mode nMOSFET transmission gate, and a push-pull ED-MOS accelerator. The accelerator suppresses the degradation in signal amplitude.

Figure 4.59 shows the speed performance of a frequency divider fabricated on a 0.25-μm MTCMOS/SOI process. When the substrate bias is 0 V, the threshold voltages of the depletion- and enhancement-mode nMOSFETs are -0.13 and 0 V, respectively. To achieve a high operating speed at any supply voltage, the substrate bias is changed to suit the supply voltage. At a supply voltage of 0.5 V, the substrate bias is 1.8 V, which makes the threshold voltage of the depletion-mode nMOSFET the designed value of -0.2 V. In this way, a maximum operating speed of 5.2 GHz is obtained.

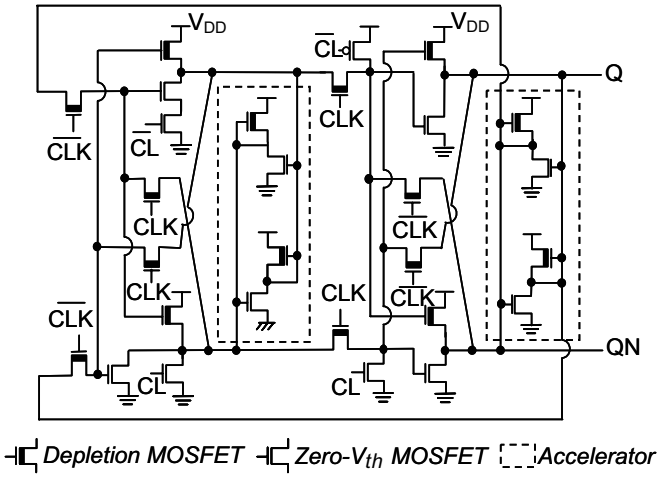


Fig. 4.58 Ultrahigh-speed TFF with ED-MOS/SOI circuits.

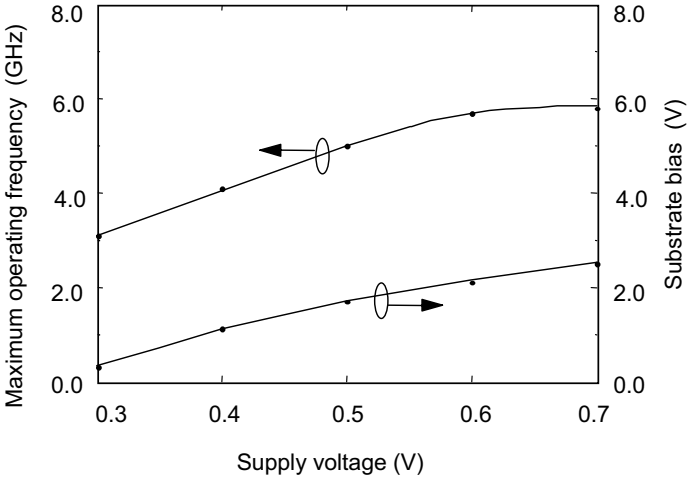


Fig. 4.59 Maximum operating speed and substrate bias vs. supply voltage for frequency divider fabricated on 0.25-μm MTCMOS/SOI process.

Simulation results on the speed improvement obtainable with various ED-MOS circuits are shown in Fig. 4.60. The results for a conventional dual-rail zero-V_{th} CMOS TFF are also shown for comparison. The supply voltage is 0.5 V. The maximum operating frequency is normalized by that for the differential zero-V_{th} CMOS TFF. If we replace the CMOS logic circuit in a zero-V_{th} CMOS TFF with a push-pull ED-MOS logic circuit, the operating speed improves about 10%. An ED-MOS accelerator and a depletion-mode nMOS transmission gate improve the operating speed about 35%. As a result, a differential ED-MOS TFF, which consists of an ED-MOS logic circuit, an accelerator, and a depletion-mode nMOS transmission gate, is 50% faster than a dual-rail zero-V_{th} CMOS TFF. A dual-rail ED-MOS TFF dissipates a power of 0.9 mW at an operating speed of 5.2 GHz. Under the same speed condition, a dual-rail zero-V_{th} CMOS TFF requires a supply voltage as high as 1 V and dissipates twice as much power.

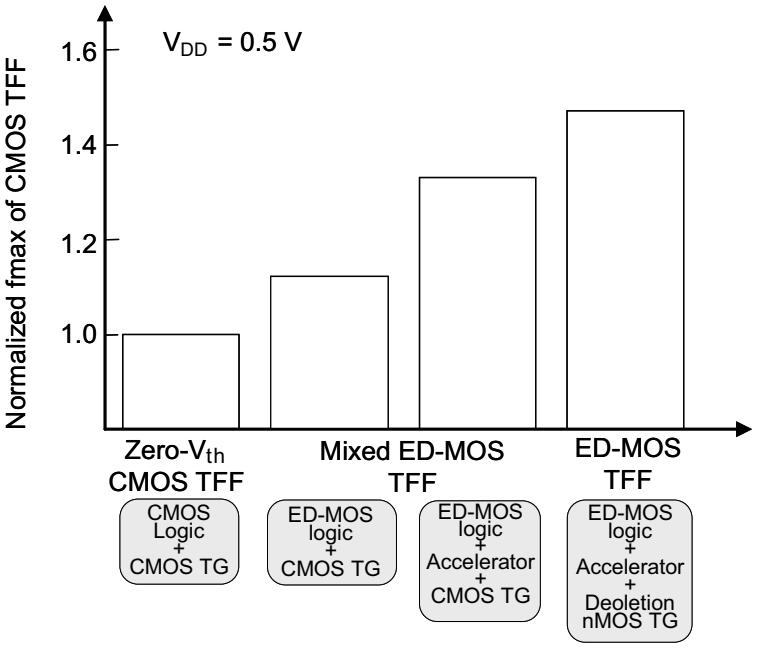


Fig. 4.60 Improvement in operating speed of frequency divider through the use of ED-MOS circuits

The power efficiency of a dual-rail ED-MOS frequency divider is shown in Fig. 4.61 along with the characteristics of the main reported dividers [4.20] -[4.22] for comparison. Only the ED-MOS/SOI circuit dissipates less than 1 mW of power and achieves a high power efficiency of over 10 GHz/mW.

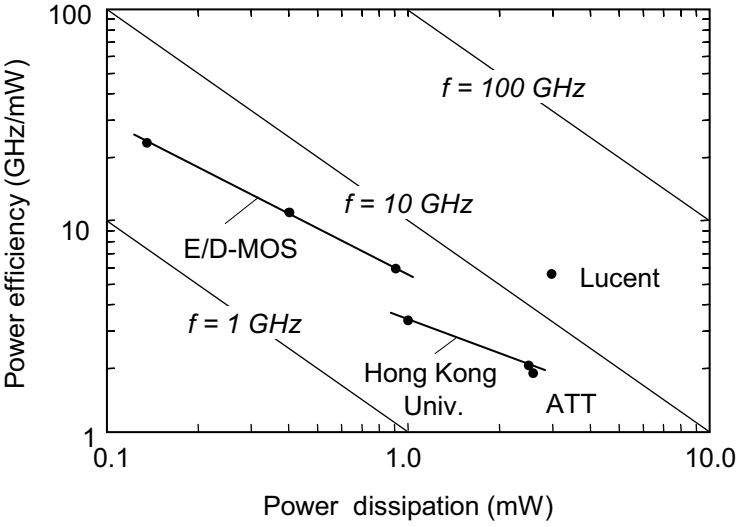


Fig. 4.61 Comparison power efficiency of E/D-MOS/SOI TFF and conventional frequency dividers.

4.6.3 ED-CMOS Frequency Divider

The 1/8 frequency divider based on a dual-rail ED-CMOS/SOI circuit scheme in Fig. 4.62 combines an ultrahigh-speed ED-MOS TFF and low-power zero-V_{th} CMOS TFFs. The first-stage ED-MOS TFF exhibits the highest frequency. The second-stage zero-V_{th} CMOS TFF reduces the leakage current while running at half the speed of the first-stage TFF. In addition, the increase in the short-circuit power dissipation is also suppressed, even when the threshold voltage is 0 V.

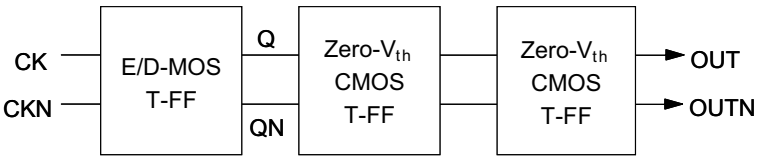


Fig. 4.62 1/8 static frequency divider made with ED-CMOS/SOI circuits.

To verify the effectiveness of the ED-CMOS/SOI circuit scheme, a 1/8 frequency divider was designed and fabricated on a 0.25-μm fully-depleted SOI process. The gate oxide was 3.5 nm thick; the active Si layer, 50 nm thick; and the buried oxide in the SIMOX wafer, 100 nm thick. The threshold voltages of the depletion-mode and zero-V_{th} MOSFETs are -0.13 V and -0.01 V, respectively, for the nMOSFETs and -0.02 V for the pMOSFETs.

The operating waveforms for a supply voltage of 0.3 V are shown in Fig. 4.63. The maximum operating frequency is 3.6 GHz and the power dissipation is 0.3 mW. A substrate bias of 0.6 V was applied to adjust the threshold voltage of the depletion-mode nMOSFETs. The jitter of the output waveform is 53 ps, and the variation is suppressed to less than 2.5%.

The dependence of maximum operating frequency on supply voltage is shown in Fig. 4.64 for dividers with a variable and a fixed substrate bias. If the substrate bias is fixed, the ratio of the current drivabilities of depletion-mode and enhancement-mode MOSFETs changes; and there is no increase in operating speed as the supply voltage increases. In contrast, adjusting the substrate bias enables us to obtain a maximum operating frequency of 5.4 GHz at a supply voltage of 0.5 V. In this case, the substrate bias is 1.5 V.

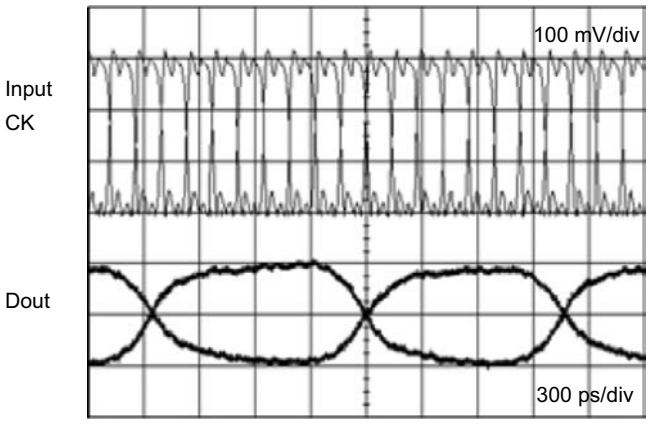


Fig. 4.63 Measured waveforms of 1/8 frequency divider made with ED-CMOS/SOI circuits.

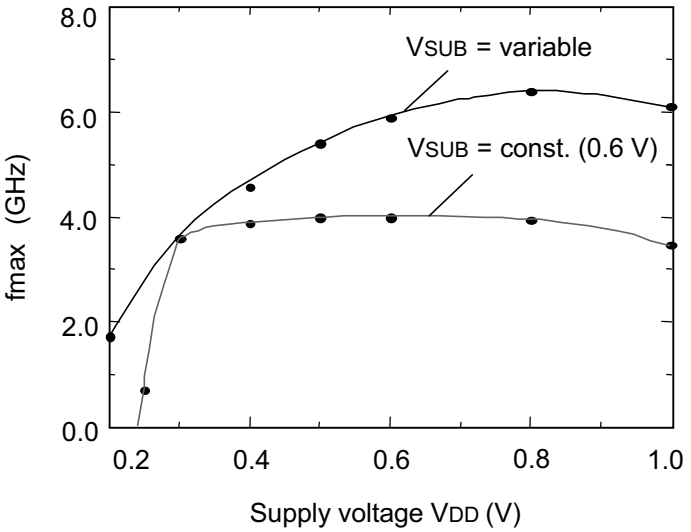


Fig. 4.64 Maximum operating frequency vs. power dissipation of 1/8 frequency dividers.

Figure 4.65 shows the dependence of maximum operating frequency on power dissipation for ED-CMOS/SOI and zero-V_{th} CMOS/SOI dividers. For a power

dissipation of 1 mW, the maximum operating frequency of the ED-CMOS circuit is about 1.5 times larger. And for a given maximum operating frequency of 5 GHz, the ED-CMOS circuit dissipates only one-fourth the power of the zero-V_{th} CMOS circuit.

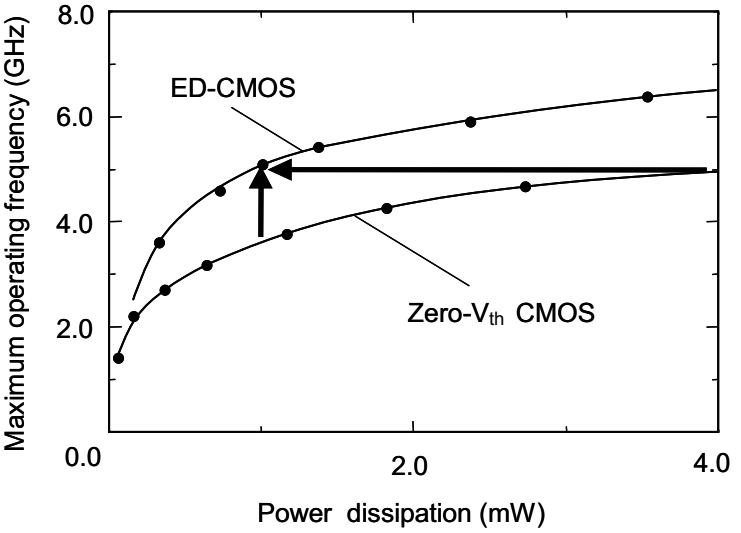


Fig. 4.65 Maximum operating frequency vs. supply voltage of the 1/8 frequency dividers.

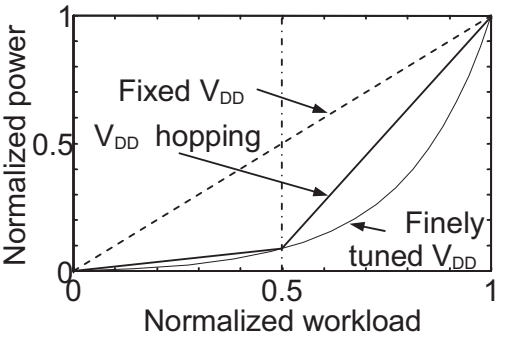
4.7 CPU

Portable systems, such as PDAs and cellular phones, now require high-performance, low-power processors. The most basic way to reduce power is to lower the supply voltage (V_{DD}) because the power is proportional to V_{DD}^2. According to this scenario, the ITRS roadmap predicts that, in 2013, V_{DD} will be as low as 0.5 V. FD-SOI technology is a promising way to fabricate this generation of devices because it provides superior characteristics. That is, the subthreshold slope is steeper than that for bulk CMOS devices, and the swing is near the ideal value of 60 mV/decade, which helps suppress the leakage current. In addition, FD-SOI devices have a smaller junction capacitance, which makes them suitable for high-speed operation.

This subsection discusses the design methodology for a processor with a target speed of 400 MHz and a supply voltage of 0.5 V. A general rule of thumb is that the threshold voltage (V_{th}) should be less than 20% of V_{DD} for high-speed circuits. When V_{DD} is 0.5 V, we set V_{th} to less than 0.1 V in the logic part of the processor. The memories use higher values of V_{DD} and V_{th} to suppress the leakage current of the cells because the memories contain most of the transistors. So, a dual-V_{DD}, dual-V_{th} scheme is employed to achieve both low power and high speed. Moreover, the higher V_{DD} enables operation at double speed (800 MHz), which allows a V_{DD}-hopping scheme [4.24] to be implemented.

First, the V_{DD}-hopping scheme is briefly explained. The power can be reduced when the workload is low because we can lower the frequency, which enables the reduction of V_{DD}. A higher V_{DD} is used only when high performance is needed. This is the basis of the V_{DD}-hopping scheme. As shown in Fig. 4.66(a), if frequency levels and V_{DD}s can be finely tuned, the relationship between power and workload is given by the thin solid line. But in reality, fine tuning is not possible. For two-level V_{DD} hopping, the half frequency (f/2) is used with the low V_{DD}; and the full frequency (f) is used with the high V_{DD}. These two frequencies are set so as to enable safe synchronization between the processor and peripheral circuits. In this two-level scheme, f/2 and the low V_{DD} are used when the workload is less than 50%; and f and the high V_{DD} are used when the workload is over 50 %. The thick solid line shows the power dependence. V_{DD} hops between the two voltages depending on the performance required. This scheme consumes much less power than a fixed-V_{DD} scheme (dotted line).

In a multimedia application such as MPEG4 video encoding and decoding, the load on the processor is not constant because it depends on the data. In this kind of application, there is a chance to lower the frequency, which is why V_{DD} hopping is suitable for multimedia applications. It has been shown that high performance is required only during 8% of the encoding time for a typical MPEG4 bitstream [4.25]. Figure 4.66(b) shows an MPEG4 encoding system with a V_{DD} -hopping scheme; it consumes 75% less power than a fixed-V_{DD} scheme [4.25].



(a)

(b)

Fig. 4.66 (a) Power dependence on workload. (b) V_{DD} -hopping system.

As mentioned above, V_{DD} hopping provides dynamic power management in which V_{DD} and the frequency change adaptively, depending on the workload of the processor. In contrast, in V_{th} hopping [4.26], V_{th} is changed directly by means of the body bias to control the leakage power; this is thought to be more effective than V_{DD} hopping when the leakage current is large. Unfortunately,

however, V_{th} hopping is not applicable to FD-SOI devices because they have no body terminal, which is the basis for V_{th} hopping. Even so, with the help of drain-induced barrier lowering (DIBL), V_{DD} hopping is an effective low-power technique for FD-SOI devices, even when the leakage power is large, as will be shown below.

Figure 4.67 shows a block diagram of a processor based on a dual-$V_{DD,}$ dual-V_{th} scheme. V_{DDL} is the low V_{DD} , and can be switched between 0.5 V and 1 V. V_{thL} is the low V_{th}, which is 0 V. Similarly, V_{DDH} can be switched between 1 V and 2 V; and V_{thH} is 0.3 V. V_{DDL} and V_{thL} are used in the logic part to achieve high speed, while V_{DDH} and V_{thL} are used in the instruction memory, data memory, and register files, which have a low activation ratio and a low dynamic power. The instruction and data memories both have a capacity of 2 kb (128 words × 16 bits). The register files have room for sixteen words and are based on a 2-read-port, 1-write-port cell. In the processor, since V_{DDH} is $2V_{DDL,}$ V_{DDH} tracks the change in V_{DDL} so that a balance is maintained between the critical paths of the logic part and those of the memories. The external-memory interface downloads and uploads memory content. For high-speed operation, a voltage-controlled oscillator (VCO) generates a clock at frequencies up to 1 GHz. It can output either f or $f/2$ for V_{DD} hopping through the use of a frequency selector. The supply voltage of the VCO is always set to V_{VCO} for stable operation. Monitoring 1/64 of the VCO output provides accurate information on the internal operating frequency.

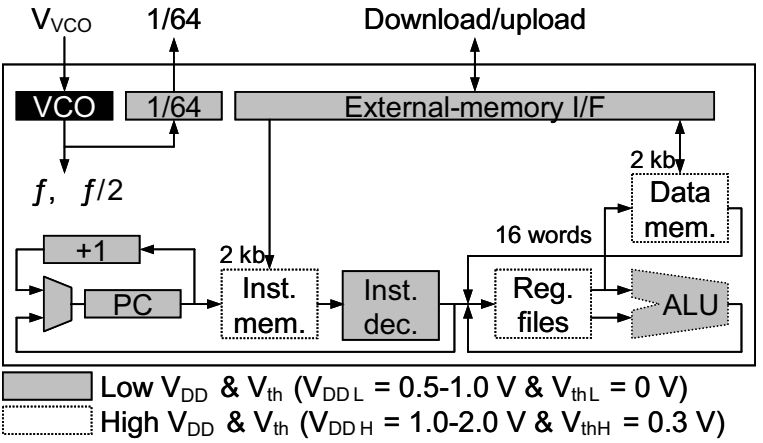


Fig. 4.67 Block diagram of processor.

The ALU is based on a 16-bit Kogge-Stone binary adder (Fig. 4.68) to achieve the highest speed. The critical path is in the adder, and the delay time is determined by a path through 6 gates connected in series, namely, one gate that issues a generate or propagate signal, four gates for the binary look-ahead part, and one gate that outputs a sum from a carry. At a V_{DDL} of 0.5 V, the delay is 1.5 ns without pipeline flip-flops, and 2.1 ns with pipeline flip-flops. The ALU also has a shifter and a bit operator.

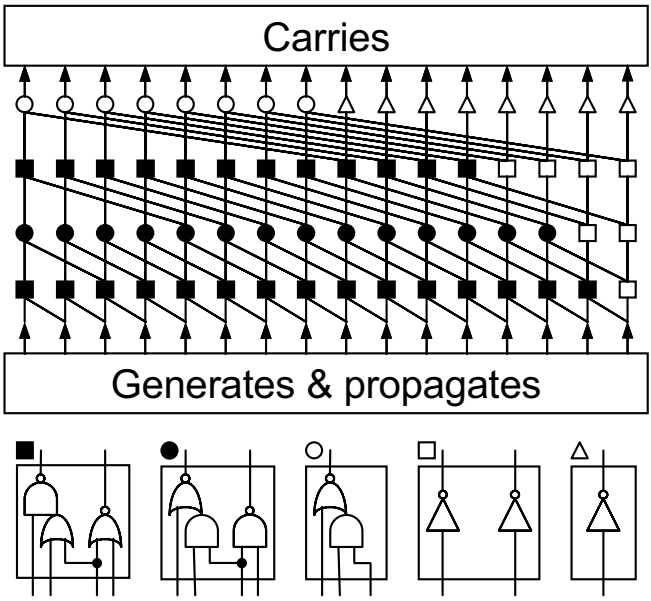


Fig. 4.68 16-bit Kogge-Stone adder.

Figure 4.69 shows a block diagram of an SRAM for the processor. We cannot use the low-V_{th} (V_{thL}) for an SRAM cell because that would result in a large leakage current, which would dramatically increase the power dissipation of the SRAM. So, we use V_{DDH} and V_{thH} for the cells. For stable operation, the word lines and bit lines also run on a supply voltage of V_{DDH}. The buffers and predecoders, however, should use V_{DDL} because they are interfaces between the memory core and the logic part. It is quite reasonable to reduce the dynamic power of the buffers and predecoders because they have long wires and many fanouts, and the dynamic power dominates. As a result of these assignments, level-up converters are needed at the interface between the memory core and the buffers.

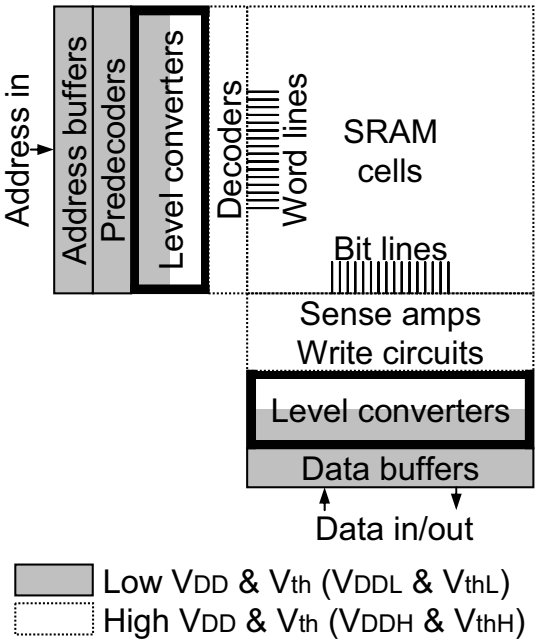


Fig. 4.69 Block diagram of SRAM.

Level-up conversion is handled by the replica-biasing level-up converter in Fig. 4.70(a). It is twice as fast as the conventional type in Fig. 4.70(b) [4.27] because it incorporates a decoding function and does not need a slow cross-coupled configuration. The decoder and its replica circuit may exhibit a large static current when the series of decoding nMOSFETs turns on. This static current does not matter because the replica circuit is shared, and only one of the decoders is activated and consumes power. Again, when the nMOSFETs turn on, they fight against the high-V_{th} pMOSFET load, which makes the input margin small. In order to deal with the small input margin, the voltage divider always keeps the bias voltage in the middle of V_{DDL}, thereby compensating for differences among the strengths of the n- and pMOSFETs. A voltage divider, which is commonly used in DRAMs, is useful in suppressing the static current.

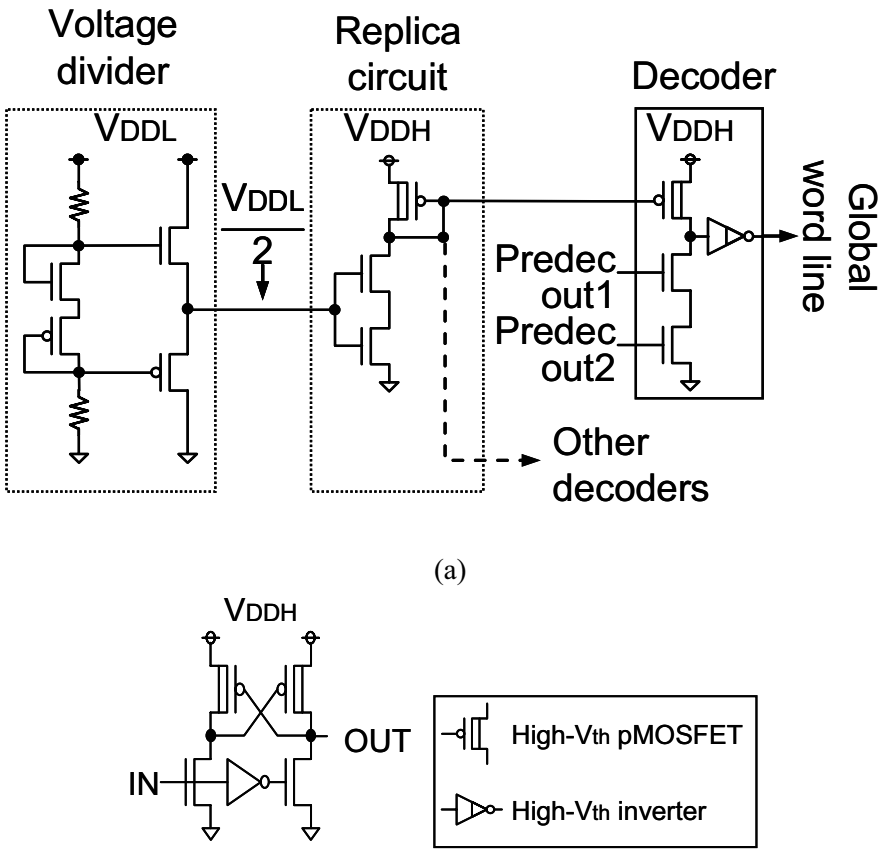
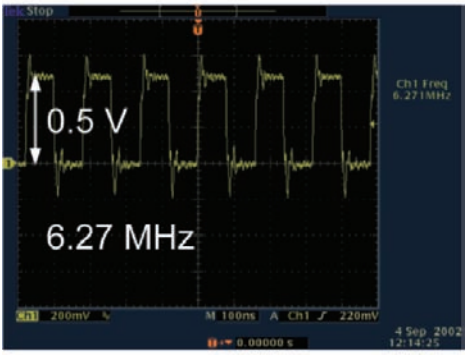


Fig. 4.70 Level-up converters: (a) replica-biasing and (b) conventional.

Figure 4.71(a) shows a measurement setup with an LSI tester, which externally switches between the two V_{DD}s. Even though the processor works at a high frequency, slow testing is possible because it has an interface to external memory. The monitored output of the VCO in Fig. 4.71(b) has a voltage of 0.5 V and a frequency of 6.27 MHz. Since this is 1/64 of the internal operating frequency, the figure shows that the processor is working at a voltage of 0.5 V and a frequency of 400 MHz.

(a)



(b)

Fig. 4.71 (a) Measurement setup. (b) Monitored output of VCO.

Figure 4.72 is a micrograph of the processor chip. It was made on a 0.25-μm, triple-metal FD-SOI process with dual V_{th}'s. The logic part contains about 2000 gates, including those for the peripheral circuits of the memories and register files. It was designed with the cell library described in the next paragraph. The memories, which work at a supply voltage of V_{DDH}, account for 85% of the transistor count.

A compact cell library was used for the logic synthesis of the processor [4.28]. It has only 20 kinds of logic gates (Fig. 4.73) because a small number of logic gates does not significantly degrade the performance [4.28]. Limiting the number to 20 makes it possible to fine-tune the design of each cell so that the

processor works even under worst-case conditions. For instance, for a 2-input NOR with a V_{DDL} of 0.5 V, correctly sizing the transistors is of critical importance because the ratio of the on-current of a pMOSFET to the off-current of an nMOSFET is only 33, which is much smaller than in a conventional design.

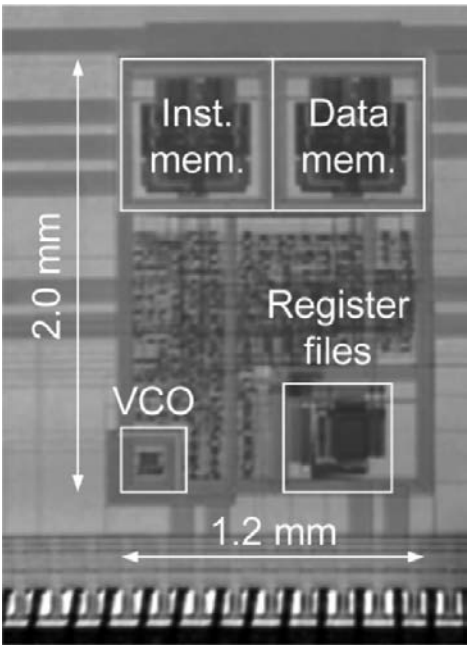


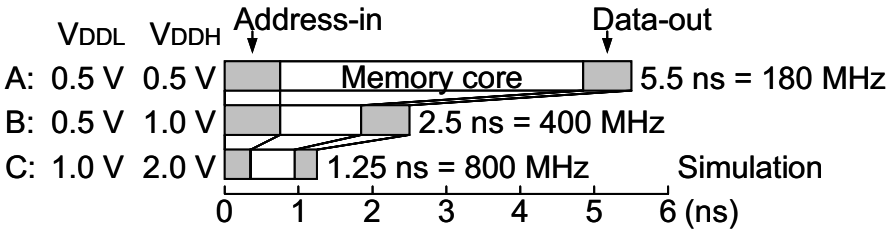
Fig. 4.72 Micrograph of processor chip.

INV x 3	NAND x 3
NOR x 3	AOI x 2
OAI x 2	EXOR
EXNOR	MUX x 2
DFF x 2	CLKBUF

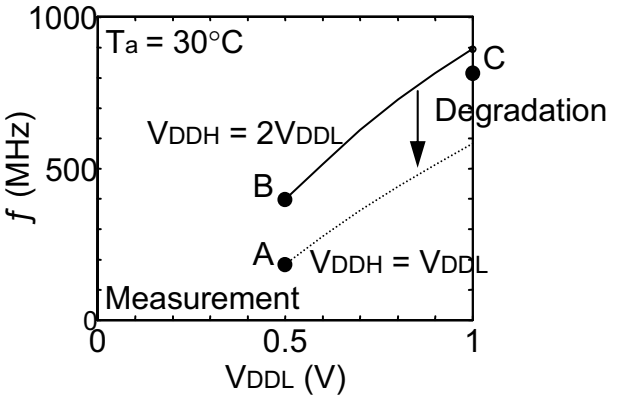
Fig. 4.73 Types of gates in compact cell library.

The bar graphs in Fig. 4.74(a) show a breakdown of the simulated SRAM delay for three cases. The critical delay of the processor is the memory read-out time.

In Case A, both V_{DDL} and V_{DDH} are 0.5 V; and operation is not very fast because the decoders, bit lines, and sense amplifiers in the memory core take a long time to carry out their functions. The processor is assumed to work at a frequency of 400 MHz in Case B and at 800 MHz in Case C. Figure 4.74(b) shows the measured dependence of operating frequency on V_{DDL} for the three cases. The solid line is for $V_{DDH} = 2V_{DDL}$, and the dotted line is for $V_{DDH} = V_{DDL}$. The difference between the simulation and measurement results for Case C is due to an error in the SPICE model file for a V_{DDL} of 1 V. Clearly, V_{DDH} should be $2V_{DDL}$ for high-speed operation. However, V_{DDH} should not be fixed at 2 V because the replica-biasing level-up converter might fail to convert a voltage when V_{DDL} is 0.5 V.



(a)



(b)

Fig. 4.74 (a) Breakdown of delay in access time and (b) performance of SRAM.

Figure 4.75 shows the measured dependence of operating frequency on V_{DDL} for $V_{DDH} = 2V_{DDL}$ at room temperature (30°C) and a high temperature (100°C). At room temperature, the processor operates at a speed of 400 MHz when V_{DDL} = 0.5 V, and at 800 MHz when V_{DDL} = 0.9 V. So, V_{DD} hopping from 400 MHz to 800 MHz is possible by changing V_{DDL} from 0.5 V to 0.9 V. Another interesting point is that the delay has a positive temperature dependence. It has been pointed out that, when V_{DD} is below 1 V and V_{th} is set to a moderate value, the circuit delay generally has a negative temperature dependence [4.29]. However, this processor has the usual positive temperature dependence because V_{th} is zero.

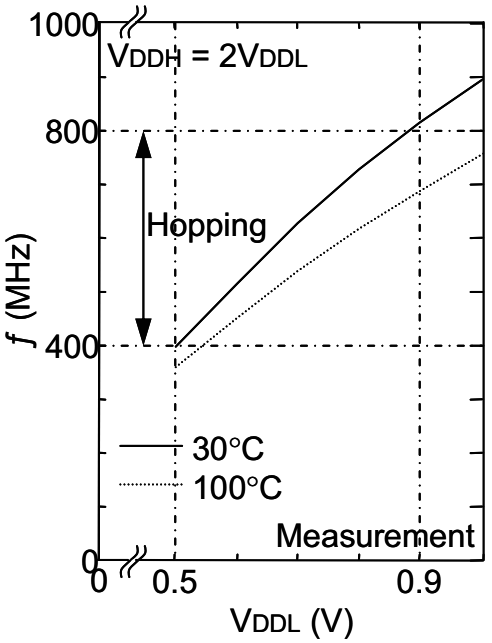


Fig. 4.75 Measured operating frequency.

The graph in Fig. 4.76 shows how leakage current depends on V_{DDL} when the clock is stopped. At a high ambient temperature of 100°C, the leakage current is 3.6 times greater than the value at room temperature. It should be noted that at both temperatures, the leakage current strongly depends on V_{DDL}. This is due to DIBL. Without DIBL, the leakage current would be constant even if V_{DDL} changed.

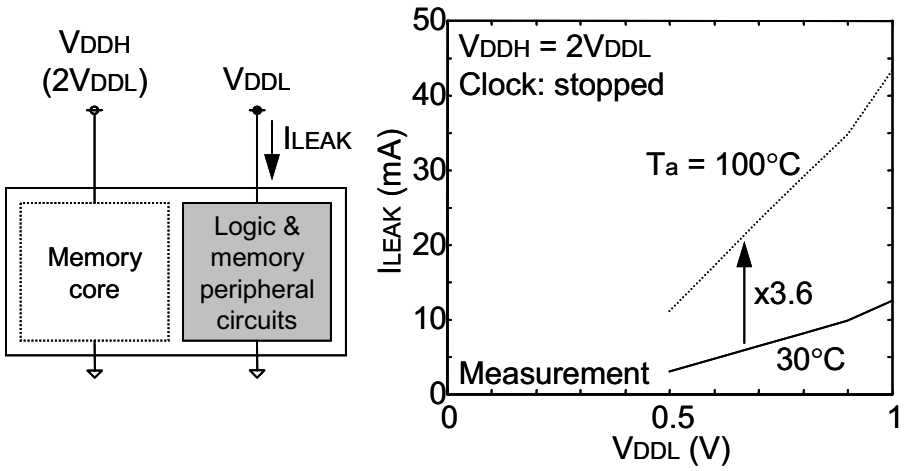


Fig. 4.76 Measured leakage current characteristics.

Figure 4.77 shows the measured power characteristics at temperatures of 30°C and 100°C. The total power (P_{TOTAL}) is the sum of the leakage power (P_{LEAK}) and the dynamic power. When V_{DDL} changes from 0.5 V to 0.9 V, P_{TOTAL} jumps from 3.5 W to 29 W at room temperature. Note that P_{TOTAL} and P_{LEAK} exhibit a similar dependence on V_{DDL} at the two temperatures. In other words, it is possible to effectively scale the power by changing V_{DDL}, but not by changing V_{thL}. This, in turn, demonstrates that V_{DD} hopping is still effective in FD-SOI circuits when the voltage is below 1 V, where we can enjoy its power scaling benefits.

Figure 4.78 analytically shows the power scaling benefits of V_{DD} hopping. In the formula for P_{LEAK}, V_{thL} is zero, λ is the DIBL coefficient, and S is the sub-threshold swing. The dynamic power ($P_{DYNAMIC}$) is proportional to $V_{DDL}^{2.5}$. This is derived using the alpha-power law with α set to 1.5. If λ is zero, which means that there is no DIBL, there is no power scaling benefit because the relationship between power and V_{DDL} is linear. On the other hand, if λ is 0.1, the simulated curve for P_{LEAK} agrees well with the measured curve. Furthermore, P_{LEAK} is quite similar to $P_{DYNAMIC}$, which demonstrates the power scaling benefits of V_{DD} hopping.

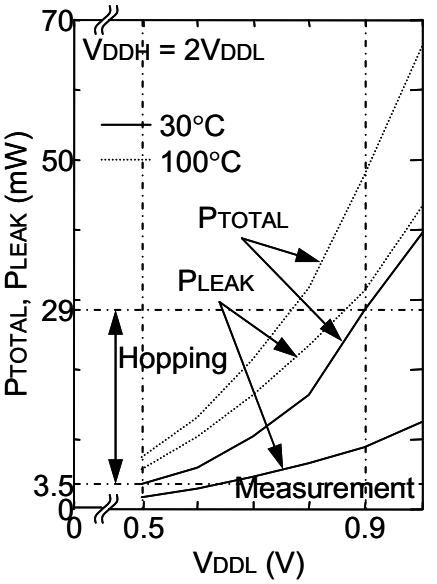
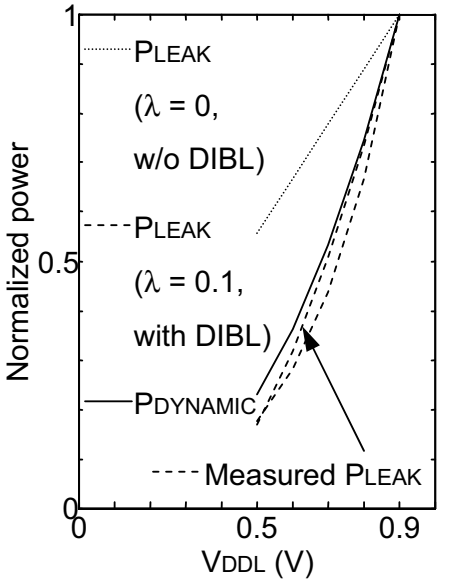


Fig. 4.77 Measured power.



$$P_{LEAK} \propto V_{DDL} \cdot I_0 \cdot 10^{-\frac{V_{th}-\lambda \cdot V_{DDL}}{S}}$$
$$\propto V_{DDL} \cdot 10^{\frac{\lambda \cdot V_{DDL}}{S}}$$
$$P_{DYNAMIC} \propto f \cdot V_{DDL}^2$$
$$\propto \frac{(V_{DDL}-V_{thL})^{\alpha}}{V_{DDL}} \cdot V_{DDL}^2$$
$$\propto V_{DDL}^{2.5}$$

Fig. 4.78 Power scaling.

4.8 Summary

This chapter described various 0.5-V digital circuits based on the MTCMOS/SOI circuit scheme and implemented primarily with FD-SOI MOSFETs. First, a method of clustering multi-V_{th} logic gates was presented; and its effectiveness was demonstrated in an adder and a multiplier. A pass-transistor-type adder and a wave-pipelined multiplier based on the MTCMOS/SOI circuit scheme were also explained to demonstrate techniques for achieving both high speed and low power at a supply voltage of 0.5 V. Then, the scheme for a 0.5-V MTCMOS/SOI SRAM consisting of multi-V_{th} memory cells and a multi-V_{th} readout circuit was described. The SRAM has a data-storage function and operates at a high speed with a low leakage current. As an example of an ultrahigh-speed 0.5-V LSI operating at a frequency of over 1 GHz, a frequency divider with an ED-CMOS/SOI circuit was presented that combines an ED-MOS circuit and a zero-V_{th} CMOS/SOI circuit. Finally, a V_{DD}-hopping scheme based on the MTCMOS/SOI circuit scheme was described, and its effectiveness in reducing power consumption was demonstrated in a 0.5/0.9 V CPU.

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Chapter 5

0.5 -1 V MTCMOS/SOI ANALOG/RF CIRCUITS

5.1 Introduction

As we enter the era of ubiquitous networking, wireless communications become increasingly important and pervasive. So, there is now a strong demand for low-output-power, low-power, radio-frequency (RF) LSIs for short-range radio applications, such as Bluetooth, ZigBee, and UWB, which are the major systems in ubiquitous communications. Furthermore, greater and greater numbers of sensors, microphones, cameras, etc. gather information about the world and output processed information as analog signals to actuators, speakers, displays, etc. So, high-performance analog-to-digital (A/D) and digital-to-analog (D/A) converters are indispensable at the interface with the real world. Since most systems now use multiple supply voltages for various LSIs, we need DC-DC converters that provide voltages from 0.5 V to 1 V and I/O circuits for interfacing low-voltage LSIs with conventional 3.3-V circuits. This chapter describes analog/RF circuits—RF building blocks, A/D and D/A converters, DC-DC converters, and I/O circuits with electrostatic discharge (ESD) protection—all of which are fabricated with fully-depleted CMOS/SOI technology and can operate at a low voltage between 0.5 V and 1V.

5.2 RF Building Blocks

If the frequency of signals is converted from the RF to the intermediate frequency (IF), the image signal has a frequency that is two times IF away from the RF signal. As a result, interference from the image signal is folded onto the IF frequency. A superheterodyne transceiver requires an external RF band-pass filter (BPF) to sufficiently reject the image signal. However, because the image rejection specifications are relaxed in short-range radio applications such as Bluetooth, an image-rejection mixer can provide sufficient image-rejection performance without an external BPF. This makes a low-IF receiver suitable for short-range radio transmission [5.1] [5.2] [5.3]. Figure 5.1 shows a generic RF transceiver for Bluetooth with low-IF architecture in the receiver. Since the year 2000, there have been a number of product announcements for CMOS RF transceivers based on Bluetooth, and many papers in this field have been presented. At present, however, the main objective is a single-chip configuration; and one of the main problems is power consumption, which is still as large as 100 mW or more. In the receiver, the image-rejection mixer cancels the image signal, thereby allowing only the desired signal to be output. The limiting amplifier boosts the desired signal up to a level that can be demodulated. In the transmitter, the VCO frequency is directly modulated by the baseband signal, the bandwidth of which is limited by a Gaussian low-pass filter (LPF). The power amplifier provides an output power of 0 to 4 dBm. A (piezoelectric) crystal oscillator is needed to produce precise carrier frequencies. Circuit bias points are stabilized by voltage reference generators against variations in the power supply and temperature. This section describes the major RF building blocks.

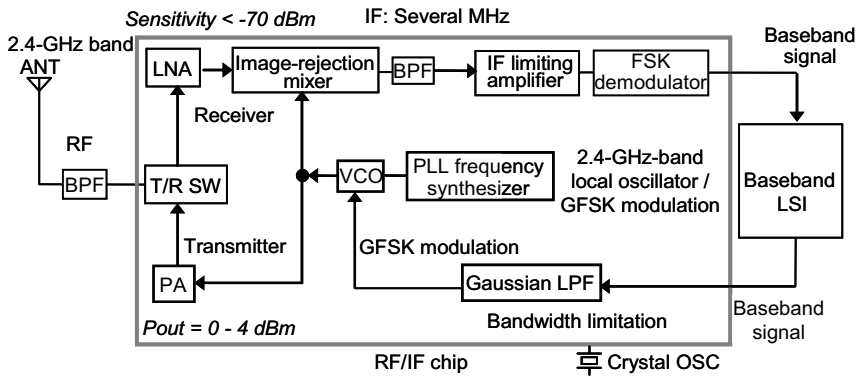


Fig. 5.1 Low-IF transceiver for Bluetooth.

5.2.1 Piezoelectric Oscillators

Figure 5.2 (a) is a circuit diagram of a type of piezoelectric oscillator called a Colpitts oscillator; and Fig. 5.2 (b) shows an equivalent circuit of a piezoelectric resonator. The motional impedance (Z_m) consisting of R_1, C_1, and L_1 is a measure of the mechanical-vibration properties, while the parallel capacitance (C_0) is a purely electrical factor unrelated to vibrations. The angular frequency (ω_s) of the mechanical resonance is the frequency that yields the minimum $|Z_m|$, and is given by

$$\omega_s = \frac{1}{\sqrt{C_1 \cdot L_1}}. \tag{5. 1}$$

In the small-signal equivalent circuit of a Colpitts oscillator (Fig. 5.3 (a)), the transconductance (g_m) is the sum of the transconductances of the pMOSFET and nMOSFET. The resistor RF, which gives the MOSFETs a self-bias, usually has a large resistance; so, it is omitted. The impedance Z_c as viewed from the terminals, which are separate from Z_m, is [5.4]

$$Z_c = -R_n + jX \tag{5.2}$$

where

$$R_n = \frac{C_G C_D}{C_0^{\,2}} \cdot \frac{g_m}{g_m^{\,2} + (\omega C_T)^2}, \tag{5.3}$$

$$X = \frac{-1}{\omega C_0} \cdot \frac{g_m^{\,2} + \omega^2 C_T (C_G + C_D)}{g_m^{\,2} + (\omega C_T)^2}, \tag{5.4}$$

$$C_T \equiv C_G + C_D + \frac{C_G C_D}{C_0}. \tag{5.5}$$

Using the formula for Z_c (5.2) allows us to simplify Fig. 5.3 (a) to Fig. 5.3 (b). Since piezoelectric resonators have narrow-band resonance characteristics, both C_1 and L_1 exhibit an extremely large reactance. Thus, the reactance (X) may be neglected, allowing us to further simplify Fig. 5.3 (b) to Fig. 5.3 (c).

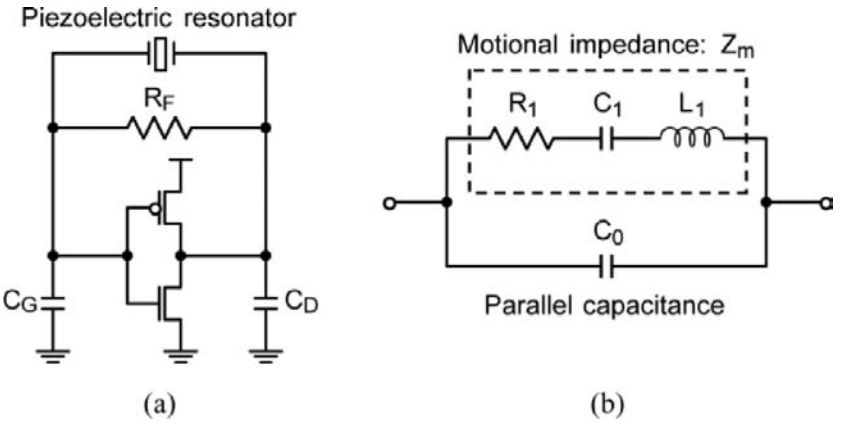


Fig. 5.2 (a) Colpitts oscillator and (b) equivalent circuit of a piezoelectric resonator.

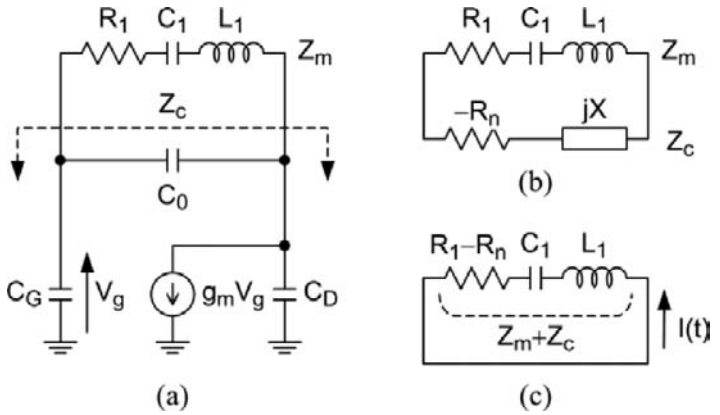


Fig. 5.3 (a) Small-signal equivalent circuit of Colpitts oscillator; (b) and (c) simplified representations of (a).

When a power source is connected to the oscillator, a voltage arises between the terminals of the resonator, generating an initial current (I(0)) in Z_m. The transient response of the current is calculated as follows:

$$I(t) = I(0)\exp\left(\frac{R_n - R_1}{2L_1}\cdot t\right)\cdot\cos\left(\sqrt{\omega_s{}^2 - \left(\frac{R_n - R_1}{2L_1}\right)^2}\cdot t\right). \qquad (5.6)$$

Therefore, the following condition must be satisfied to increase the amplitude of I(t) and excite oscillations:

$$R_n > R_1 . \tag{5.7}$$

Note that the amplitude of I(t) cannot increase infinitely in an actual circuit, because the output amplitude of the amplifier does not exceed the supply voltage. As the amplitude increases to its maximum value, R_n decreases to the equilibrium state $R_n = R_1$. Thus, the formula for I(t) (5.6) tells us that the angular frequency in the steady state is ω_s.

Here, a design process yielding a circuit that satisfies (5.7) is explained. The formula for R_n (5.3) states that the larger C_0 is, the lower R_n is. Thus, C_0 must be set as high as possible. At the start of the process, we set g_m to an arbitrary value (which means an arbitrary transistor size). Then, from (5.3) we calculate a contour plot, such as Fig. 5.4, which shows how R_n is related to C_G and C_D. In this case, the calculations employed a resonance frequency of 10 MHz, a C_0 of 5 pF, and a g_m of 2 mS. R_n reaches a maximum of 780 Ω when $C_G = C_D$ = 11 pF.

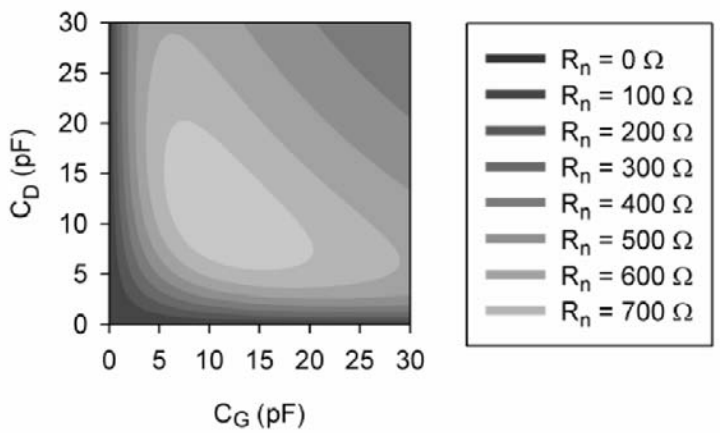


Fig. 5.4 Contour plot of Rn in graph of C_G vs. C_D.

Next, we use the maximum R_n to adjust gm. Figure 5.5 shows a graph of how the theoretically possible values of R_n depend on gm. It was obtained using the same conditions as those for Fig. 5.4. As gm increases, the possible value of Rn becomes greater. So, g_m can be reduced if R_n is sufficiently high, and must

be raised if R_n is too low. After g_m is adjusted, R_n is calculated again in the same way as before. Repeating this process a number of times yields the optimum combination of g_m, C_G and C_D.

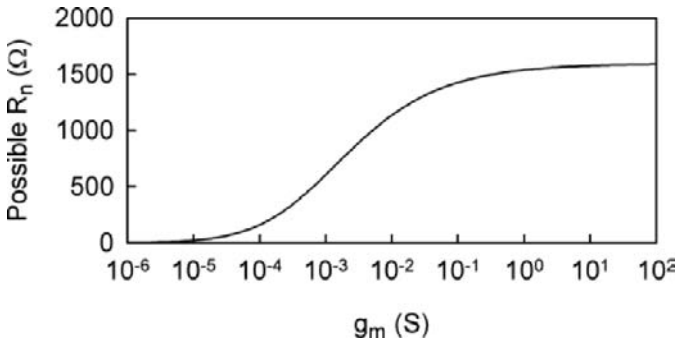


Fig. 5.5 Dependence of possible values of R_n on g_m.

From Fig. 5.5, it is clear that the maximum value of R_n remains finite as g_m tends toward infinity. This indicates the limit of a Colpitts oscillator. The upper limit on R_n is [5.5]

$$R_n(\max) = \frac{1}{2\omega C_0}. \tag{5.8}$$

Unfortunately, $R_n(\max)$ declines as the frequency increases. So, we need a different approach to obtain a high operating frequency. Figure 5.6 (a) shows a circuit diagram of a 3-stage Colpitts oscillator suitable for high frequencies [5.5]. The circuit consists of three amplifiers, A_1 to A_3, connected in a cascade.

An examination of this circuit reveals that the phase delay (θ) due to A_1 and A_2 must be taken into account. In the small-signal equivalent circuit (Fig. 5.6 (b)), the total transconductance (g_m) is the value obtained by multiplying the transconductance of A_3 by the voltage gains of A_1 and A_2. R_n and X for this circuit are calculated in the same way as before:

$$R_n = \frac{C_G C_D}{C_0^{\,2}} \cdot \frac{g_m \cos\theta}{g_m^{\,2} - 2 g_m \omega C_T \sin\theta + (\omega C_T)^2} \tag{5.9}$$

$$X = \frac{-1}{\omega C_0} \cdot \frac{{g_m}^2 - g_m \omega (C_T + C_G + C_D) sin\theta + \omega^2 C_T (C_G + C_D)}{{g_m}^2 - 2 g_m \omega C_T sin\theta + (\omega C_T)^2} \quad (5.10)$$

The denominator of (5.9) is non-negative, which means that cosθ > 0 is necessary in order to make R_n positive. It is interesting that R_n becomes infinite if the following two conditions are satisfied:

$$g_m = \omega C_T \quad (5.11)$$

$$\theta \to 0.5\pi - 0\,. \quad (5.12)$$

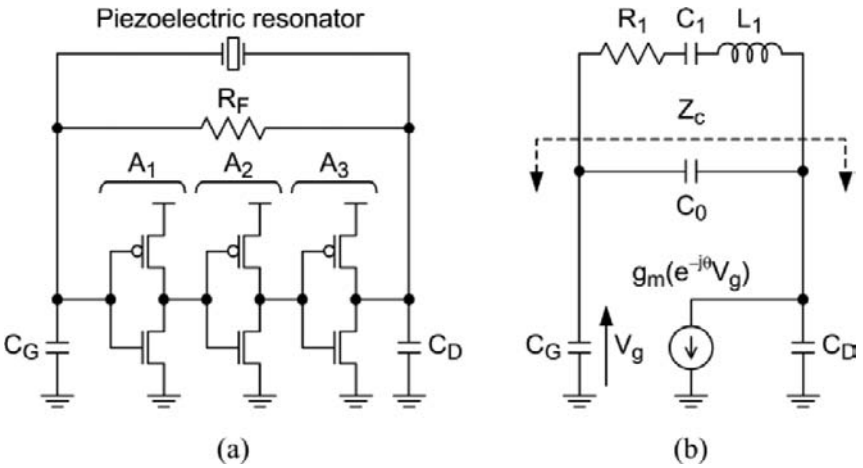


Fig. 5.6 (a) 3-stage Colpitts oscillator and (b) small-signal equivalent circuit.

This means that R_n has no limit in a 3-stage Colpitts oscillator. Therefore, if the appropriate circuit parameters are chosen, the power consumption will be very low. However, if the intention is to obtain a very large R_n, the oscillation frequency will shift away from the target value. To avoid this, θ should be kept under about 0.3π. It should also be noted that, if the small-signal output resistances of A_1 and A_2 are large, that is, if the MOSFETs are largely unaffected by channel length modulation, θ will approach π, thereby making

R_n negative. In that case, θ must be adjusted, even though it means sacrificing g_m to some extent. Placing a resistor between the input and output terminals of A_2 is one possible technique.

Fig. 5.7 shows the measured power consumption of two types of piezoelectric oscillators fabricated with FD-SOI MOSFETs. A two-stage output buffer without a load was added to the 10-MHz AT-cut crystal oscillator; and a 50-Ω load was added to the 315-MHz surface-acoustic-wave (SAW) oscillator through an AC coupling capacitor. Both oscillators have an extremely low power consumption and operate at a low supply voltage.

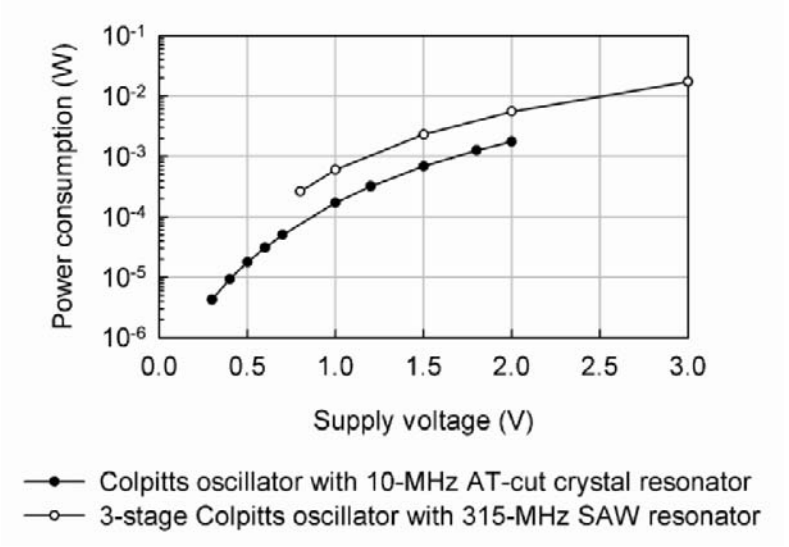


Fig. 5.7 Measured power consumption of piezoelectric oscillators.

5.2.2 Voltage Reference Generator

Analog circuits need a voltage reference circuit that generates a fixed voltage independent of power supply and temperature. Generally, a bandgap reference (BGR) circuit is used for this purpose. Figure 5.8 (a) shows a common design. The reference voltage is determined by diodes and resistors; the output voltage (V_{o1}) is about 1.25 V and is given by

$$V_{01} = V_A + R_2 \times \frac{V_A - V_C}{R_1}. \tag{5.13}$$

This circuit requires a supply voltage of over 1.25 V to generate the reference voltage. However, since CMOS LSIs made with SOI technology will use a voltage of less than 1 V, another BGR circuit is needed.

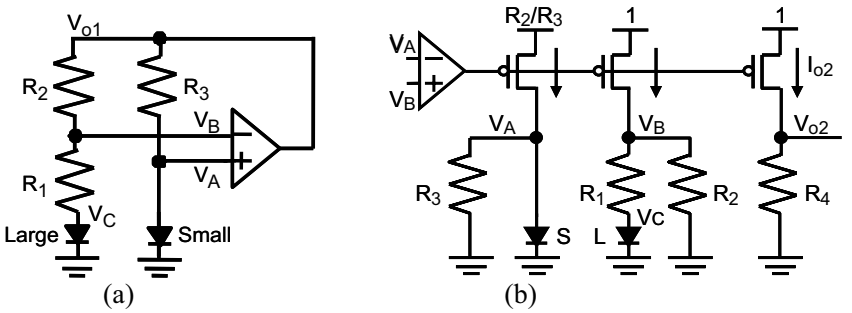


Fig. 5.8. Bandgap reference circuits: (a) conventional type and (b) low-supply-voltage type.

One example is the low-voltage type in Figure 5.8 (b) [5.6]. The reference voltage (V_{o2}) is determined by the reference current (I_{o2}) and the resistor R_4. I_{o2}, in turn, is determined by diodes and resistors, and is independent of power supply and temperature. The output voltage is given by

$$V_{02} = R_4 \times \left[\frac{V_A}{R_2} + \frac{V_A - V_C}{R_1} \right]. \tag{5.14}$$

To design a BGR circuit, we need designs for MOSFETs, resistors, and diodes. Designs are usually available for the first two, but not for diodes because they are rarely used in other types of digital or analog circuits. In a bulk diode structure (Fig. 5.9 (a)), the cathode is the p-diffusion area, and the anode is the n-diffusion area below that. This type of structure cannot be formed in FD-SOI devices because the layer under the p-diffusion area is the buried oxide. For FD-SOI devices, the diode characteristics are determined by the parasitic p-n junction of an SOI MOSFET (see Fig 5.9 (b)). In an nMOSFET, there is a p-diffusion area under the poly-silicon gate, provided that no channel area is formed. This area constitutes the cathode, and the source and drain areas constitute the anode.

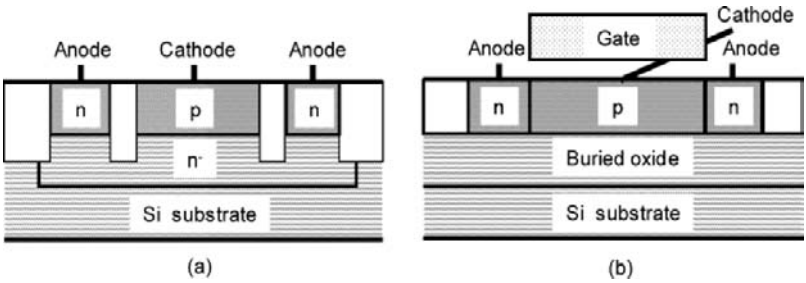


Fig. 5.9 Diode structures for bandgap reference circuit made on (a) bulk CMOS process and (b) FD-SOI process.

Figure 5.10 shows the characteristics of an FD-SOI diode. Fig. 5.10 (a) shows the current-voltage characteristics for the cathode-anode voltage (V_A in Fig. 5.8) of a small diode; and Fig. 5.10 (b) shows the current-voltage characteristics for the cathode-anode voltage (V_C in Fig 5.8) of a large diode with an area 18 times greater than that of the small one. The large diode exhibits ideal characteristics because the curves are linear, but the small diode does not because of the change in slope at a voltage of about 0.75 V. This change reflects the pronounced influence of the parasitic resistor at voltages above 0.75 V, and it necessitates the use of a V_A below 0.75 V to obtain ideal characteristics in a small diode. Figure 5.10 also shows the temperature characteristics of (c) V_A and (d) V_A-V_C. By exploiting the temperature characteristics through optimization of the resistors, we can make the output voltage of the BGR circuit independent of temperature.

Figure 5.11 shows the dependence of output voltage on (a) supply voltage and (b) temperature for a BGR circuit with a low supply voltage fabricated on an FD-SOI process. The curves in (a) are almost flat (-10 mV/V) when the supply voltage is greater than 0.9 V; and the temperature characteristics in (b) are fairly flat (-0.02 mV/°C).

Thus, a reference voltage for FD-SOI circuits operating at a supply voltage of 1 V or less can be generated by using a low-supply-voltage BGR circuit and FD-SOI diodes.

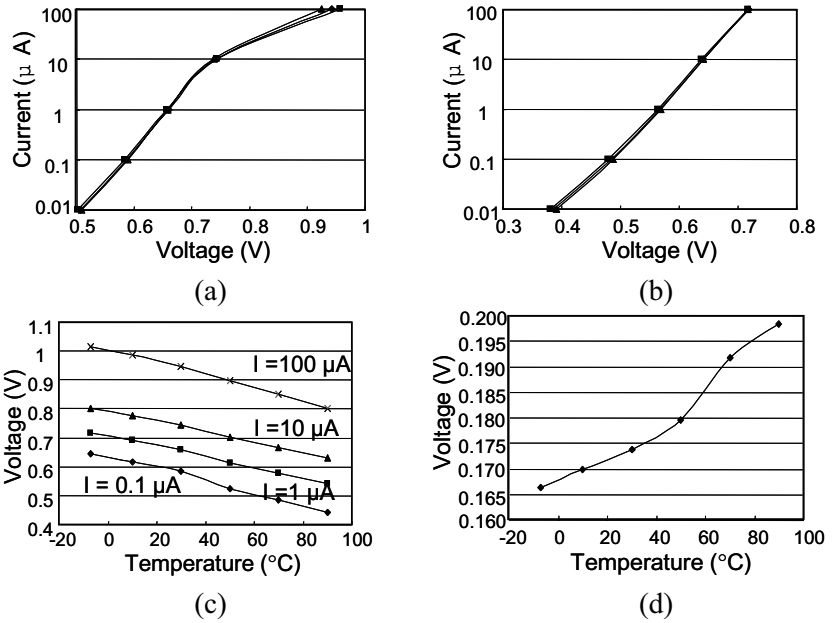


Fig 5.10 Characteristics of FD-SOI diode. (a) Current-voltage characteristics of small-area diode. (b) Current-voltage characteristics of large-area diode. (c)Temperature characteristics of small-area diode. (d) Temperature characteristics of V_A-V_C.

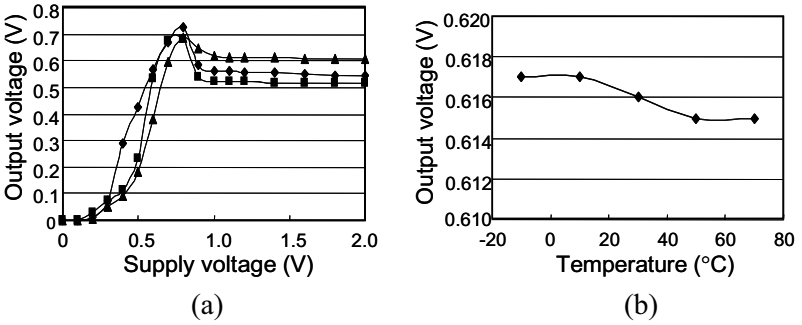


Fig 5.11 Dependence of output voltage on (a) supply voltage and (b) temperature for BGR circuit fabricated on FD-SOI process.

5.2.3 Transmit/Receive Switches

Since Bluetooth employs time division duplexing (TDD), a transmit/receive switch (T/R SW) is needed between the antenna and the RF transceiver. MOSFETs are suitable for T/R switches because the ON and OFF states are easy to control by means of the gate bias. Moreover, SOI MOSFETs provide very good isolation at high frequencies because of their low parasitic capacitance with respect to the Si substrate.

A single-pole double-throw (SPDT) switch (Fig. 5.12) switches the signal path from the antenna to the RF transceiver between the receiver (Rx) path and the transmitter (Tx) path in the time domain. The gate length of the SOI devices is 0.35 μm and the gate bias is 1 V or 0 V.

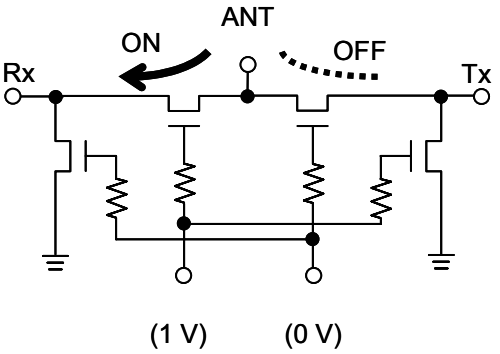


Fig. 5.12 Transmit/receive switch in 0.35-μm SOI.

Figure 5.13 compares the measured ON/OFF performance of an SOI switch with that of a 0.18-μm bulk CMOS switch [5.7]. Around a frequency of 2 GHz, the SOI switch has an isolation of more than 30 dB, which is about 6 dB larger than that of the bulk one. Furthermore, the ON-state insertion loss of the SOI switch is a few dB smaller than that of the bulk one at frequencies above 4 GHz.

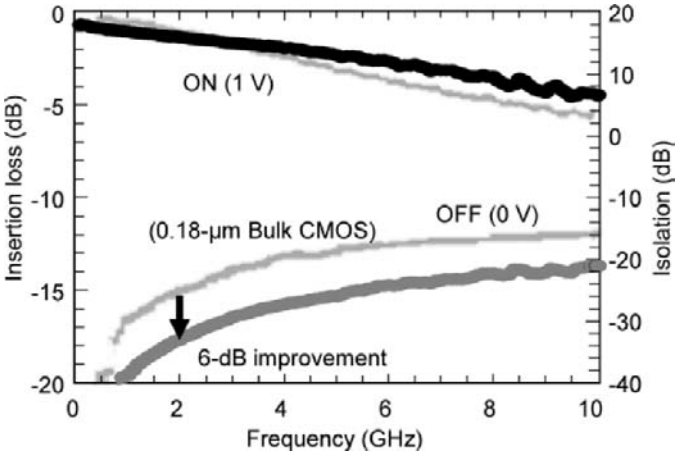


Fig. 5.13 Measured performance of SOI and bulk T/R switches.

The intermodulation performance (Fig. 5.14) of SOI devices with a gate length of 0.2 μm was measured by the two-tone test at tone frequencies of about 2.4 GHz. Even when the gate-control voltage is as low as 1 V, we can obtain a third input intercept point (IIP3) of more than 10 dBm. These results show that SOI devices are very suitable for RF T/R switches.

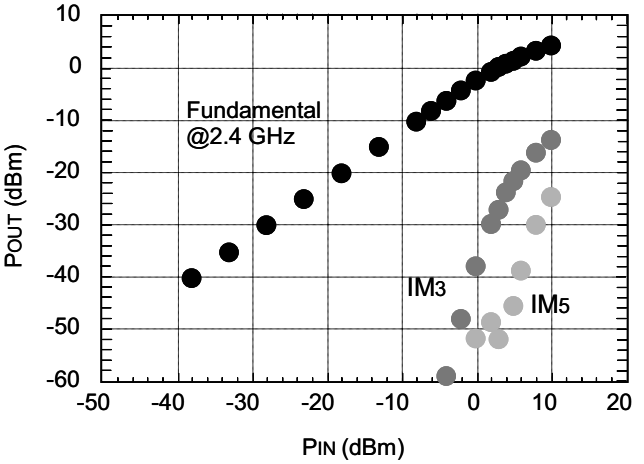


Fig. 5.14 Large-signal dependence for T/R switch made on 0.2-μm SOI process.

5.2.4 Low-Noise Amplifiers (LNAs)

The first stage of an RF receiver needs a low-noise amplifier (LNA) to amplifiy very weak signals with low added noise. Figure 5.15 shows a circuit schematic of a cascode LNA with a stack of two nMOSFETs. Cascoding transistors yields both a small Miller capacitance with respect to the input and a large isolation between the input and output terminals. This enables us to design the input and output matching circuits independently and thus obtain excellent high-frequency performance. The input impedance can be matched to 50 Ω by using the source inductor (L_S). The gate impedance (Z_G) is given by

$$Z_G = \frac{L_S\, g_m}{C_{GS}} + j\omega L_S + \frac{1}{j\omega C_{GS}}. \tag{5.15}$$

If the real part of $L_S \cdot g_m / C_{GS}$ is set to 50 Ω and a series inductor (L_G) is inserted to cancel the capacitive component, then 50-Ω matching is obtained.

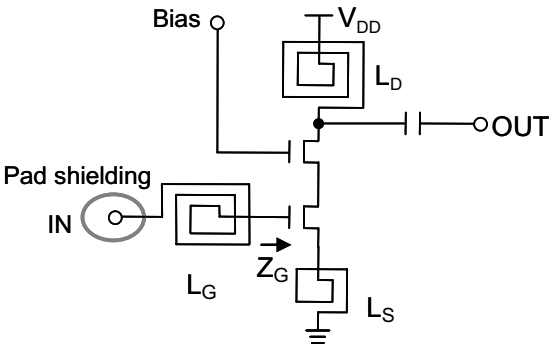


Fig. 5.15 Cascode LNA in CMOS/SOI.

In the layout of the LNA, a pad-shielding technique [5.8] improves the noise performance. The shielding employs the fifth metal layer for the signal pad, which is shielded by the grounded first metal layer. By avoiding signal injection into the resistive Si substrate, we can obtain a low signal loss at the input pad, and thus a lower noise figure (NF). Because fully-depleted SOI devices have small body-bias effects, a cascode LAN can operate at a low voltage of 1 V.

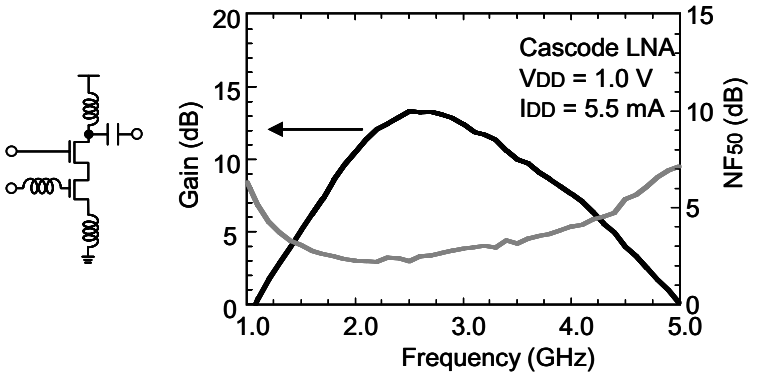


Fig. 5.16 Measured performance of cascode LNA.

Figure 5.16 shows the measured performance of a cascode LNA fabricated on a 0.2-μm CMOS/SOI process. It dissipates 5.5 mW at a supply voltage of 1 V; and at a frequency of around 2.4 GHz, it exhibits a gain of 13 dB and an NF of 2.5 dB. The measured performance of a grounded-source LNA is shown in Fig. 5.17 for comparison. It dissipates more than twice as much power (13 mW), and exhibits a lower gain of 10.6 dB and a similar NF of 2.3 dB.

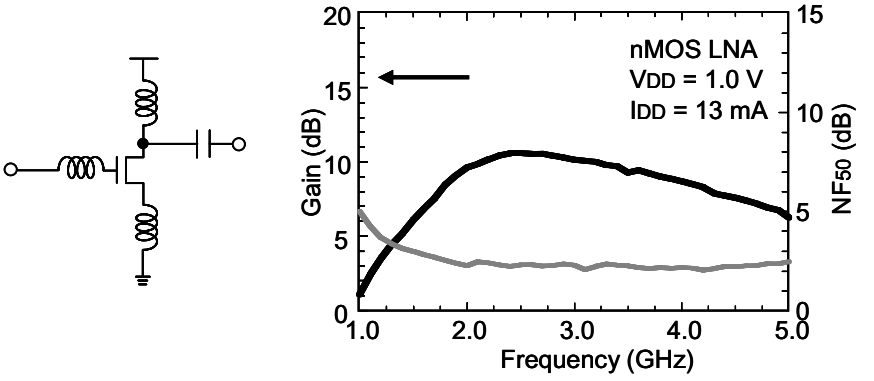


Fig. 5.17 Measured performance of common-source LNA.

So, a cascode LNA made on a fully-depleted CMOS/SOI process is very useful at a low supply voltage of around 1 V.

5.2.5 Power Amplifiers (PAs)

Because short-range wireless systems can function with a low output power, low-voltage on-chip power amplifiers can be used. For example, for Class-3 Bluetooth, a small power of 1 mW (0 dBm) is sufficient.

A power amplifier (Fig. 5.18) can be made from an output stage and a driver amplifier. Since the stage before the power amplifier usually has differential outputs, the driver amplifier has differential inputs and an inductive load output, which serves as a differential-to-single-ended converter. The output stage has a cascode configuration similar to that of the LNA. Although the output voltage of the cascode stage exceeds the supply voltage in the power saturation mode because of the inductive load, 1-V operation alleviates the breakdown problem with the transistors. At the output of the amplifier, an LC trap (series resonator) attenuates the second harmonic.

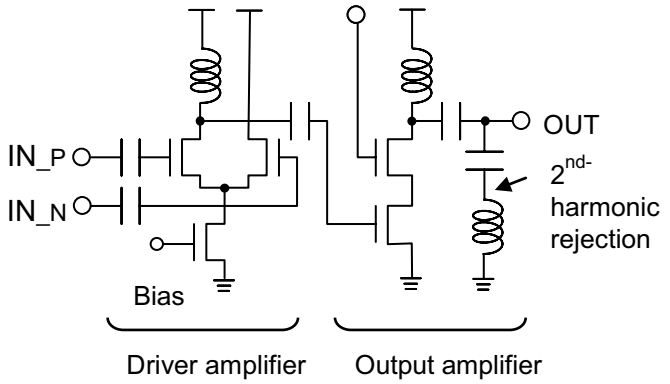


Fig. 5.18 Cascode power amplifier.

The measured input-output characteristics of an output stage fabricated on a 0.2-μm CMOS/SOI process are shown in Fig. 5.19. At a supply voltage of 1 V, the small-signal gain is 10 dB, and the saturation output power is 5 dBm. Figure 5.20 shows the measured input-output characteristics of a power amplifier with a driver amplifier. It dissipates 7 mW at a supply voltage of 1 V, and has a small-signal gain of about 22 dB and a saturation output power of 1.8 dBm for an input power of –10 dBm.

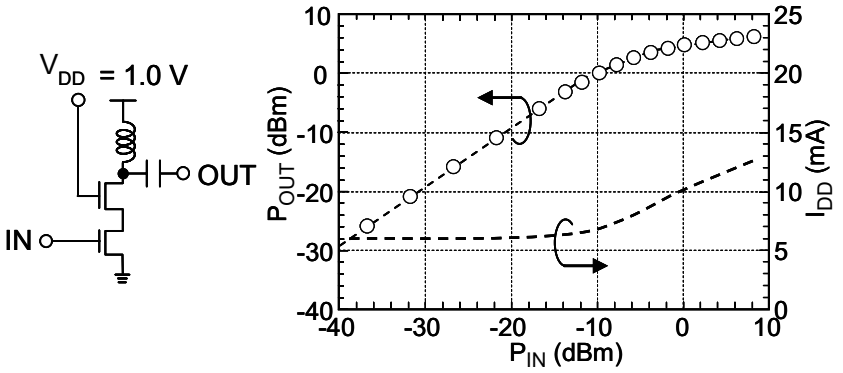


Fig. 5.19 Measured input-output characteristics of output stage.

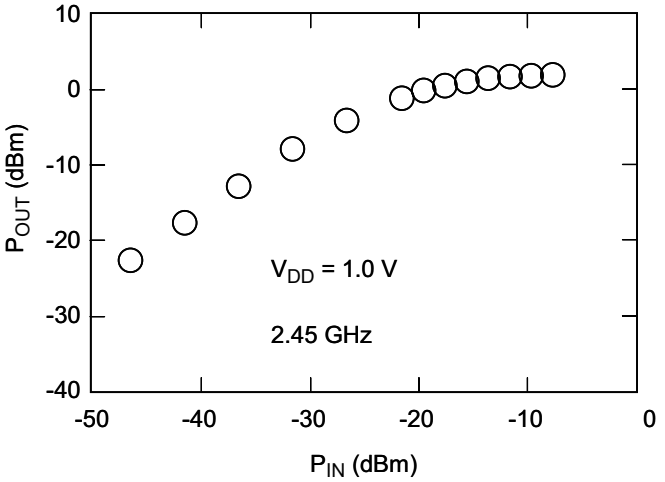


Fig. 5.20 Measured input-output characteristics of power amplifier with driver amplifier.

So, a CMOS/SOI power amplifier with a cascode output stage is very useful for short-range radios, even at a low supply voltage of around 1 V.

5.2.6 Mixers and Image-Rejection Receiver

A. Low-voltage mixers

Mixers perform frequency conversion in wireless transmitters and receivers based on analog multiplication as follows:

$$\cos\omega_s t \cdot \cos\omega_{LO} t = \frac{1}{2}\cos(\omega_S + \omega_{LO})t + \frac{1}{2}\cos(\omega_S - \omega_{LO})t\,, \qquad (5.16)$$

where ω_S and ω_{LO} are the angular frequencies of the information signal and the local oscillator (LO) signal, respectively. The frequency-sum component is used for up-conversion, and the frequency-difference component is mainly used for down-conversion. Mixers are also indispensable for quadrature modulation and demodulation because a kind of frequency conversion is performed between the baseband and carrier-band signals.

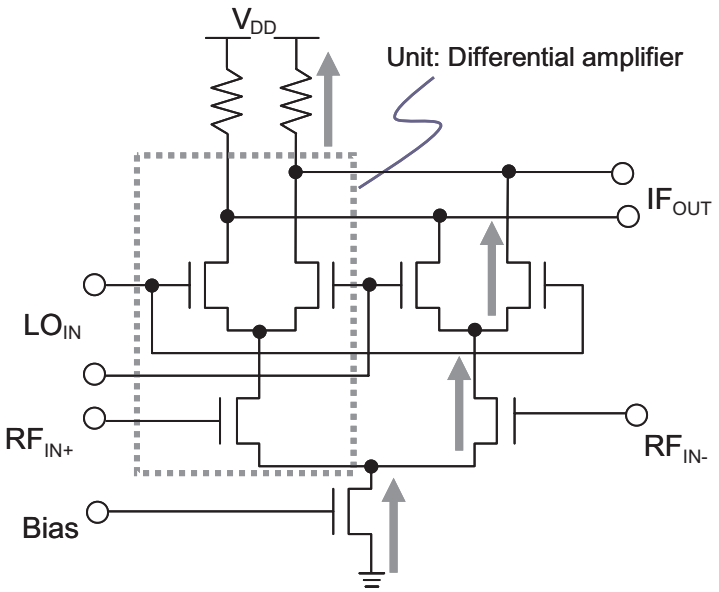


Fig. 5.21 Circuit diagram of Gilbert-cell mixer.

The most common type of mixer is a Gilbert-cell mixer (Fig. 5.21). It normally has a stack of three transistors with a drain-to-source voltage of

about 0.7 V. It is a kind of analog multiplier that converts the frequency of sine-wave signals. When the differential pairs connected to the local oscillator (LO) are completely switched, the conversion gain is a maximum. In this state, the LO signal has an approximately rectangular waveform; so the result of the multiplication is given by

$$\cos\omega_S t \cdot \frac{4}{\pi}(\cos\omega_{LO}t - \frac{1}{3}\cos 3\omega_{LO}t + \frac{1}{5}\cos 5\omega_{LO}t - \cdots)$$
$$= \frac{4}{\pi}\cos\omega_S t \cdot \cos\omega_{LO}t + \frac{4}{\pi}\cos\omega_S t \cdot (-\frac{1}{3}\cos 3\omega_{LO}t + \frac{1}{5}\cos 5\omega_{LO}t - \cdots). \quad (5.17)$$

The first term is the product of the fundamental LO component and the RF signal, and is the result of adding the coefficient $4/\pi$ to Eq. (5.16). Consequently, the coefficient of the frequency-sum and frequency-difference components is $2/\pi = (4/\pi)\cdot(1/2)$. The other terms are the products of the LO harmonics and the RF signal; they are undesired components and are filtered out.

Due to the transistor stack, the minimum supply voltage that ensures that all the transistors operate in the saturation region is around 2 V. This has made the mixer an obstacle to the operation of RF circuits at low voltages. To lower the supply voltage, the transistors stack must be eliminated. One solution is an LC-tank (parallel resonator consisting of an inductor and a capacitor) folding technique, in which the current source of the transistors is replaced with an LC tank, thereby reducing the DC voltage drop [5.9].

Before this technique is explained, a brief review of an LC-tank circuit is first presented. RF systems combine a high-frequency RF signal and a narrow-band baseband signal; and so their main feature is a small bandwidth. This is why LC-tank circuits are very useful for low-voltage, low-power RF operation. At the resonance frequency, the impedance of an LC tank reaches a peak value of $R_S Q^2$, where R_S is the series resistance (see Fig. 5.22). Consequently, an LC tank is equivalent to a current source in that it provides a high impedance. Figure 5.22(b) shows the measured impedance; the peak value is about 250 Ω, and the value drops to around 5 Ω at low frequencies. The circuits described below are fabricated on a 0.2-μm fully-depleted CMOS/SOI process.

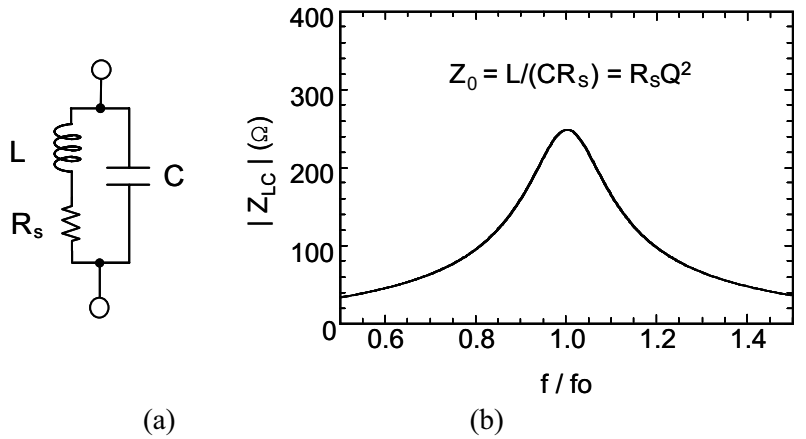


Fig. 5.22 (a) Equivalent circuit and (b) measured impedance of LC-tank circuit.

One application of an LC tank is a mixer (Fig. 5.23). First, an LC tank connected to the ground replaces the current source to make the DC drop zero (Fig. 5.23(a)). This is possible because an LC tank has a high enough impedance at around its resonance frequency. At this stage, there are still two transistors in the stack. Next, for the RF input, the nMOSFET pair is replaced with a pMOSFET one (Fig. 5.23(b)) and the polarity is changed. We call this process the "folding technique;" and it completely eliminates the stack of MOSFETs. However, a DC bias current cannot flow from V_{DD} ((Fig. 5.23(c)). So, DC paths from nodes A and B to the ground are added using LC tanks. Figure 5.23(d) shows a schematic of the resulting LC-tank folded mixer with a complementary configuration. At the resonance frequency, the RF signal passes from the RF differential pair to the LO differential pairs. In contrast, the DC currents flow from the power supply to the ground through the LC tanks. Using LC tanks and the folding technique eliminates the transistor stack, thereby enabling operation at low voltages below 1 V. Although there are twice as many current paths as in a Gilbert cell, the total current can be decreased by optimizing the sizes and biases of the n- and pMOSFETs because their DC operating points can be set independently. This issue comes up again in the discussion of the image-rejection receiver.

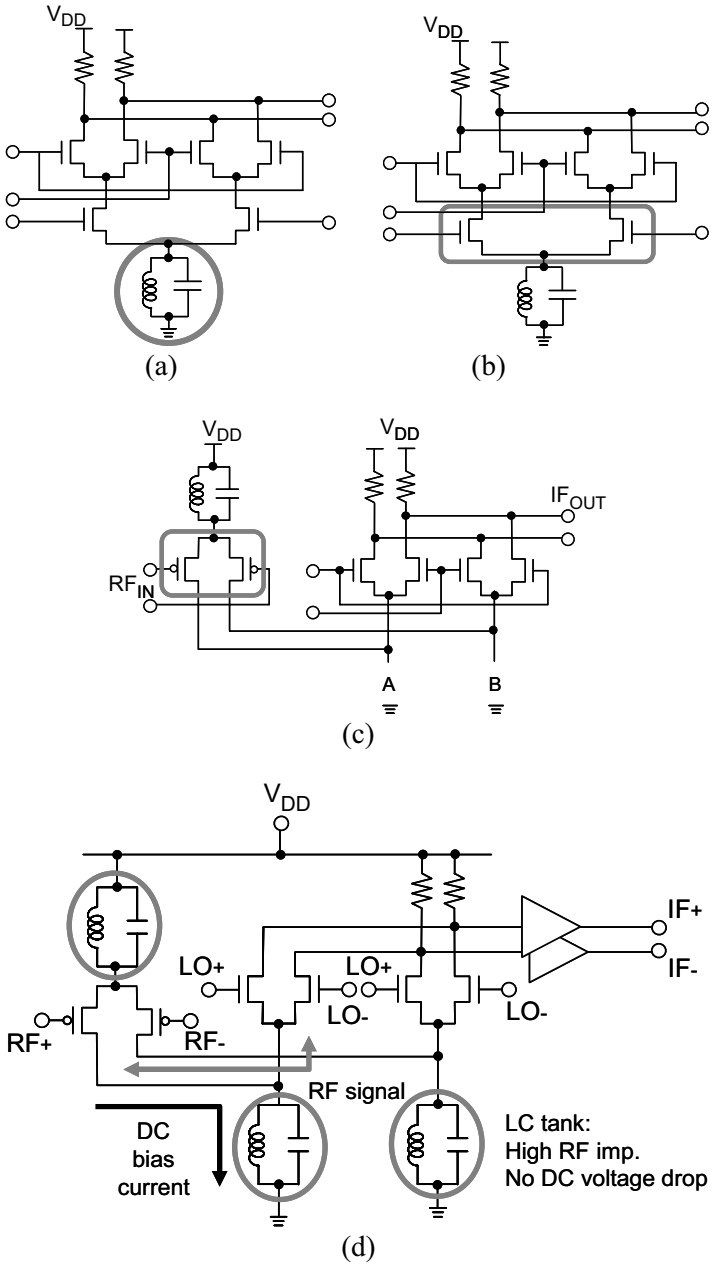


Fig. 5.23 LC-tank folding technique: (a) Phase 1, (b) Phase 2, (c) Phase 3: LC-tank folding technique, and (d) LC-tank folded mixer.

Now, let's consider the transfer function, or in other words the small-signal gain, from the RF input to the IF output when the LO pairs are completely switched. In this calculation, the resistance R_1, which equals $R_S Q^2$, replaces the tank impedance at the resonance frequency (see Fig. 5.24).

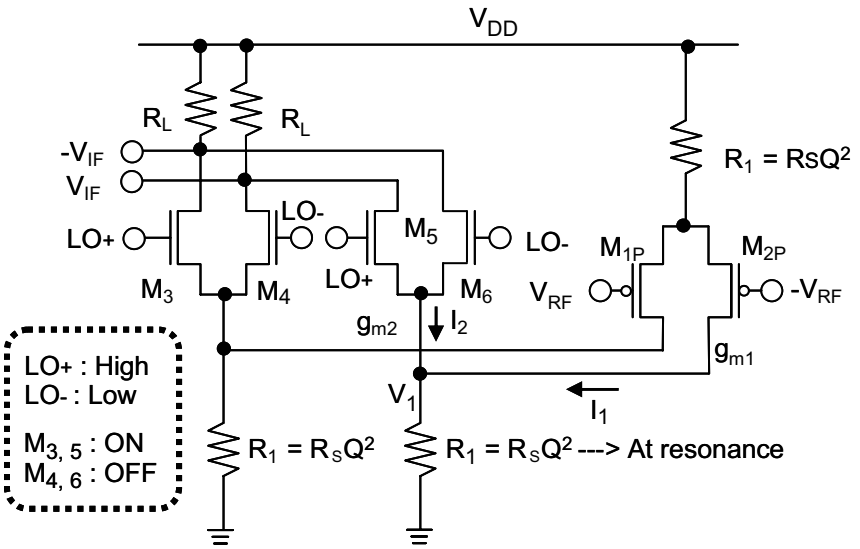


Fig. 5.24 Small-signal analysis of mixer.

If transistors M_3 and M_5 are on, we obtain the following equations from Kirchhoff's law:

$$I_1 = g_{m1}\, V_{RF}\,, \tag{5.18}$$

$$V_1 = (I_1 + I_2)\, R_1\,, \tag{5.19}$$

$$I_2 = -g_{m2}\, V_1\,, \tag{5.20}$$

$$V_R F = -R_L\, I_2\,. \tag{5.21}$$

These equations yield

$$I_2 = -\frac{g_{m2}\, R_1}{1 + g_{m2}\, R_1} i_1 \cong -I_1\,. \tag{5.22}$$

This means that most of the RF current (I_1) becomes the current $-I_2$ flowing through transistor M_5, provided that the impedance of the tank at the resonance frequency is sufficiently high. The small-signal gain (G) of a folded cascode amplifier is given by

$$G = \frac{V_{IF}}{V_{RF}} = -\frac{(g_{m2} R_1) g_{m1} R_L}{1 + g_{m2} R_1} \cong -g_{m1} R_L . \tag{5.23}$$

Therefore, when $g_{m2} \cdot R_1 >> 1$, the small-signal gain is determined by the product of the gm of the RF pair and the load resistance R_L. When the LO pairs are completely switched, the conversion gain is $-(2/\pi) g_{m1} R_L$, which is the gain in (5.23) multiplied by $2/\pi$.

The single-sideband (SSB) noise figure and conversion gain of the mixer (Fig. 5.25) were measured at supply voltages of 1 and 0.5 V. The IF was set to 170 MHz. At a supply voltage of 1 V, the current dissipation of the core circuit is 19 mA; the conversion gain is 6.7 dB at a local frequency of 2 GHz; and the SSB noise figure is 16.1 dB. Moreover, this mixer can operate at a supply voltage as low as 0.5 V.

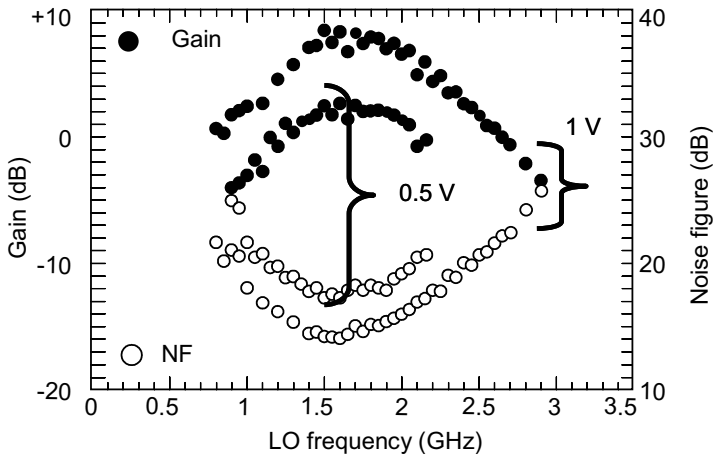


Fig. 5.25 Noise figure and conversion gain of mixer.

The intermodulation performance (Fig. 5.26) shows that IIP3 is – 6 dBm, which is sufficient for short-range radio applications such as Bluetooth.

The circuit techniques explained above can be used to build 1-V front-end circuits for short-range wireless systems like Bluetooth. Next, an image-rejection receiver fabricated on a 0.2-μm CMOS/SOI process is described.

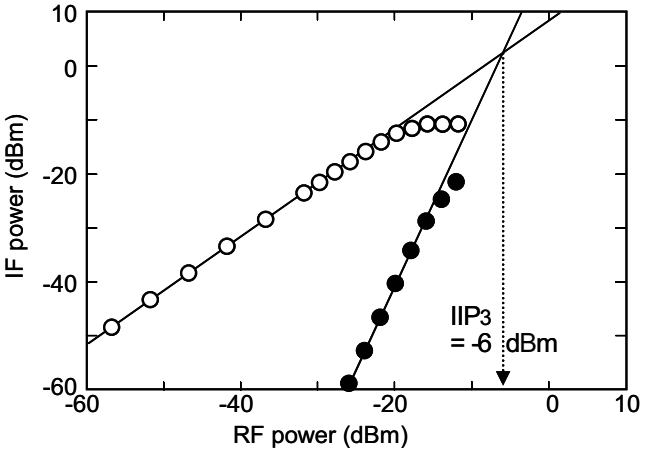


Fig. 5.26 Large-signal input-output dependence of mixer.

B. Image-rejection receiver

A low-voltage low-IF image rejection receiver (Fig. 5.27) was designed using the LC-tank folding technique [5.3]. It consists of an LNA, a quadrature mixer employing LC-tank folding, and three-stage LO and IF polyphase filters. The quadrature mixer and the two polyphase filters constitute an image-rejection mixer.

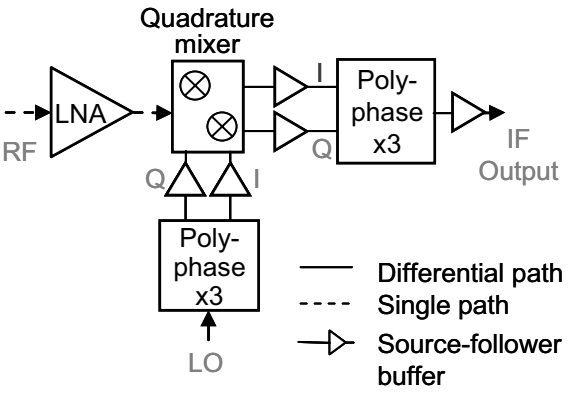


Fig. 5.27 1-V image-rejection receiver in 0.2-μm CMOS/SOI.

In superheterodyne and low-IF transceivers, RF signals are converted to IF signals; and the frequency of the image signal is two times IF away from RF (see Fig. 5.28 (a)). Consequently, the interference from the image signal is folded onto the IF frequency. For this reason, a superheterodyne transceiver needs an external RF band-pass filter (BPF) to sufficiently reject the image signal. However, since the image-rejection specifications are relaxed in short-range radio applications such as Bluetooth, an image-rejection mixer can provide a sufficient image-rejection ratio without an external BPF. In the complex-signal domain, an image-rejection mixer separates and rejects only the image signal. This is because the phase of the image signal rotates in the opposite direction, as shown in the phase diagram in Fig. 5.28 (b). An image-rejection mixer performs this operation on a chip.

A 3-stage LO-band polyphase filter (Fig. 5.29) produces a quadrature LO signal with a phase that is shifted 90° from that of the differential LO signal [5.10]. Note that each stage is given a different RC time constant to enlarge the bandwidth. This makes a multistage configuration suitable for LSI production, in which the variations in the absolute values of the resistances and capacitances are relatively large.

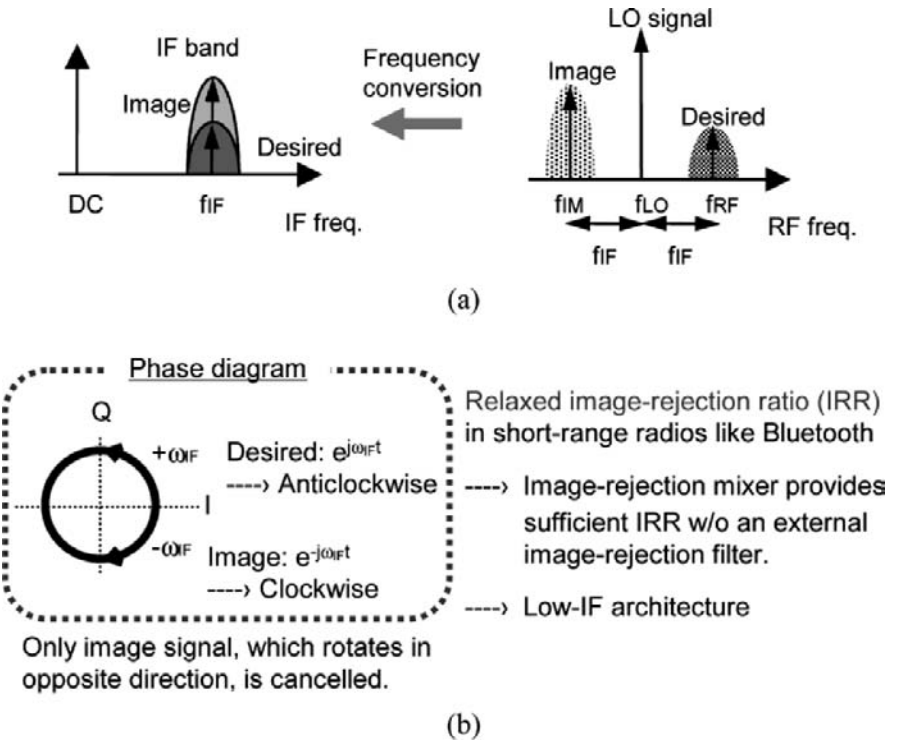


Fig. 5.28 (a) Image interference. (b) Image-rejection method.

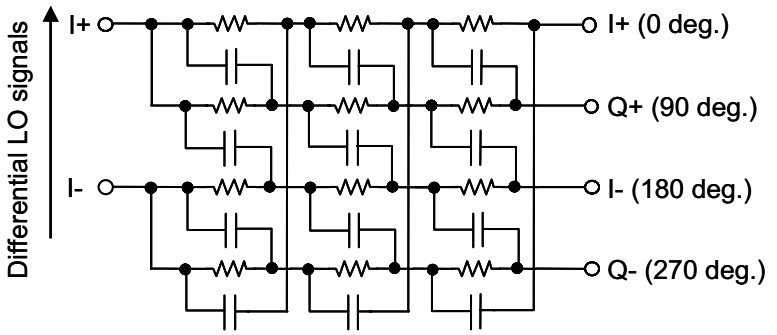


Fig. 5.29 3-stage LO polyphase filter for quadrature-LO generation.

Figure 5.30 shows a schematic of an IF polyphase filter for image rejection. The I and Q outputs of the quadrature mixer are fed into the filter to cancel only the image signal.

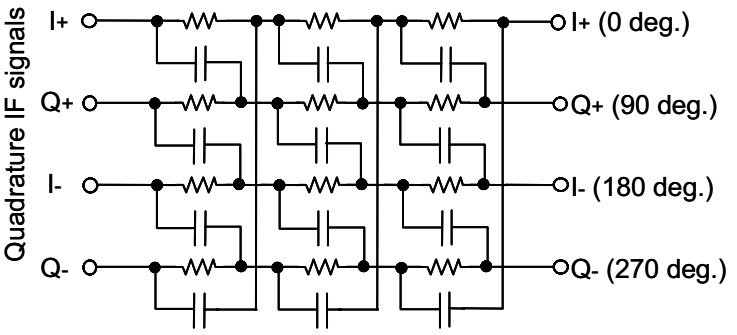


Fig. 5.30 3-stage IF polyphase filter for image rejection.

The quadrature mixer in Fig. 5.31 is different from the LC-tank folded mixer described above in that it has an nMOS single-to-balance converter, the differential outputs of which are AC-coupled to I/Q mixing cores. The combination of a transistor current source and an LC tank improves the balance characteristics. The I/Q mixing cores are combined at nodes A and B to reduce the area occupied by the LC tanks. Furthermore, this configuration improves the quadrature characteristics of LO signals, thereby providing good image rejection. Regarding bias conditions, the single-to-balance converter operates in the Class-A mode because it has to provide good linearity and low noise, while the I/Q mixing cores operate in the Class-B mode to save power.

From the measured dependence of mixer gain on LO-bias voltage (Fig. 5.32), we find that the mixer gain has a peak value around the Vth of the LO-pair transistors. At that point, the DC idle currents of the I/Q mixing cores are nearly zero. Because the LO signals have a finite transition time, there is a period of overlap in which both transistors of each LO pair are on. If this period is relatively long in the Class-A mode, part of the output signal will be lost. Operation in the Class-B mode shortens the overlap period, and thus provides the peak gain.

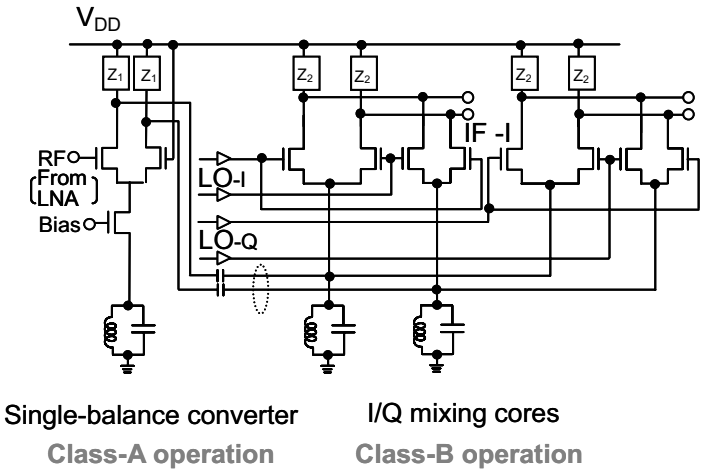


Fig. 5.31 Low-voltage quadrature mixer.

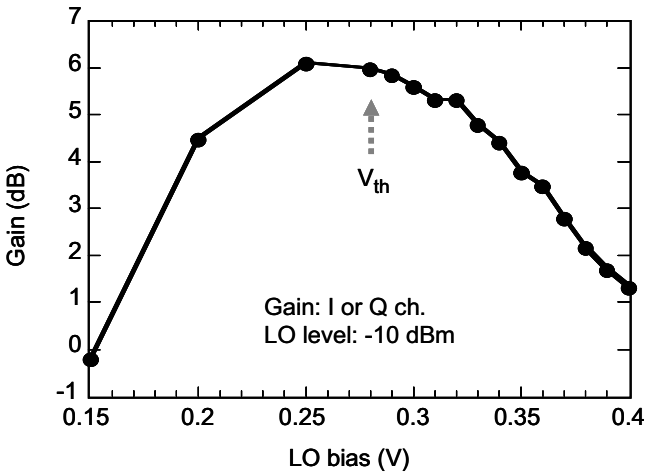


Fig. 5.32 Measured mixer gain versus LO bias.

An image-rejection receiver (Fig. 5.33) was fabricated on a 0.2-μm CMOS/SOI process. The chip is 3.8 mm × 2.2 mm in size, and the spiral inductors occupy a relatively large area.

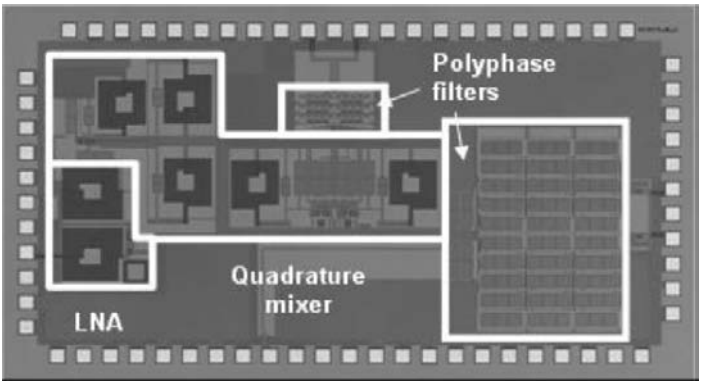


Fig. 5.33 Photomicrograph of image-rejection receiver.

The measured performance of the receiver (Fig. 5.34) shows that the image rejection ratio (IRR) is 49 dB. The receiver consumes 12 mW of power at a supply voltage of 1 V. The total noise figure (NF) of the receiver is 10 dB, and the noise figure of the LNA is 3.1 dB.

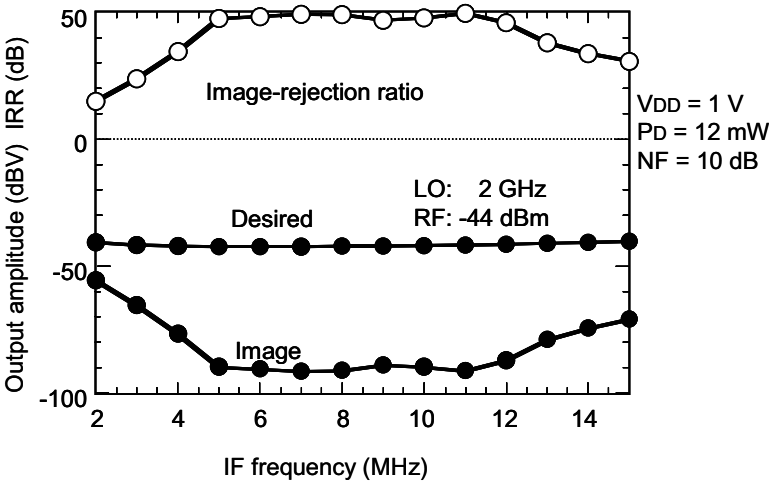


Fig. 5.34 Image-rejection characteristics.

5.2.7 Voltage-Controlled Oscillator (VCO)

This chapter concerns ultralow-power inductor-capacitor (LC)-based voltage-controlled oscillators (VCOs) made on the FD-SOI process. A VCO is a key component of wireless communication front-end ICs and requires high performance, such as low noise, a wide tuning range, low power consumption, and so on. Power consumption is an especially important consideration for mobile equipment.

The benefits of making a VCO on the FD-SOI rather than the standard CMOS process are as follows:

(1) It is easy to lower the threshold voltage of FD-SOI transistors, which enables the supply voltage and power consumption of a VCO to be reduced.
(2) The source/drain junction capacitances of transistors are smaller than those in a standard CMOS VCO. As a result, the oscillation frequency is higher, the tuning range is wider, and the power consumption is lower.
(3) It is possible to use a high-resistivity substrate, which provides a lower substrate loss and lower VCO noise.

So, the characteristics of an FD-SOI VCO are a high oscillation frequency, a wide tuning rage, low noise, and low power consumption.

Differential LC-VCOs (see Fig. 5.35) were fabricated on a 0.35-μm triple-metal FD-SOI process. The negative-gm transistors are complementary MOSFETs. The differential spiral inductor is made in the top metal layer, which has the normal thickness. VCOs were fabricated on two types of substrates: one with a normal (low) resistivity of ~10 Ωcm and one with a high resistivity of ~1 kΩcm. The inductor on the low-resistivity substrate has a quality factor (Q) of about 4. The varactor consists of an nMOS transistor. The VCO has MIM capacitors controlled by 3 bit lines for coarse tuning.

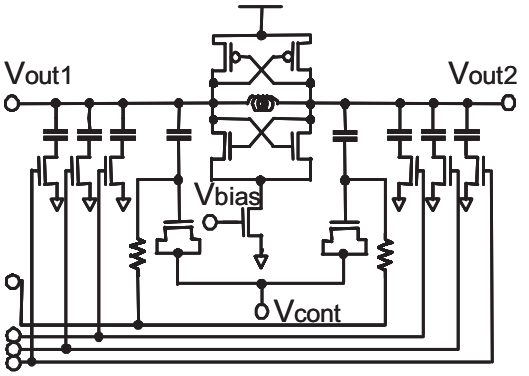


Fig. 5.35 Circuit schematic of LC-VCO.

The minimum operating currents of the two LC-VCOs were measured as a function of supply voltage (Fig. 5.36). Note that the use of the FD-SOI process enables a VCO to operate at a supply voltage as low as 0.8 V. The minimum operating current is smaller for the high-resistivity than for the low-resistivity substrate because the substrate loss is lower.

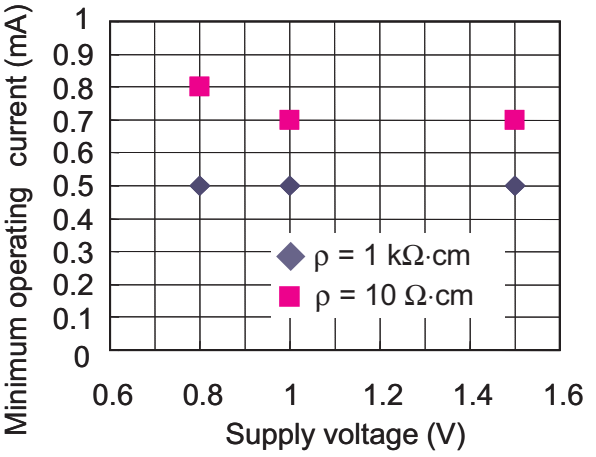
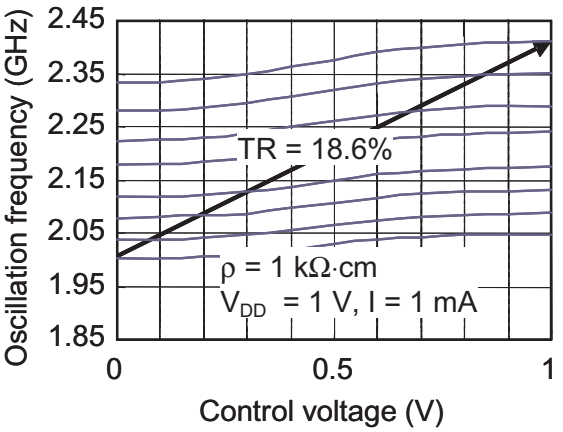
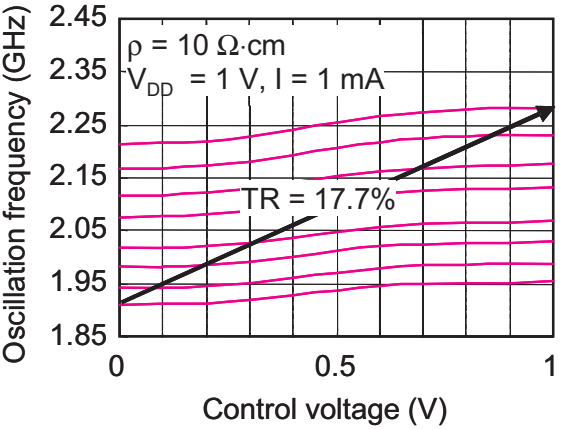


Fig. 5.36 Minimum operating current of VCO.

The frequency characteristics of the two LC-VCOs in Fig. 5.37 are for a supply voltage of 1 V and an operating current of 1 mA.



(a)



(b)

Fig. 5.37 Frequency characteristics of VCOs on (a) high-resistivity substrate and (b) low-resistivity substrate.

For the high-resistivity substrate, the center frequency (f_0) is 2.206 GHz and the tuning range (TR) is 18.6%; while for the low-resistivity substrate, f_0 is 2.063 GHz and TR is 17.7%. The high-resistivity substrate provides a higher operating frequency and a wider tuning range.

The phase noise characteristics (Fig. 5.38) at a supply voltage of 1 V and an operating current of 1 mA show that the phase noises are -107.5 dBc/Hz and -108.3 dBc/Hz for the low- and high-resistivity substrates, respectively.

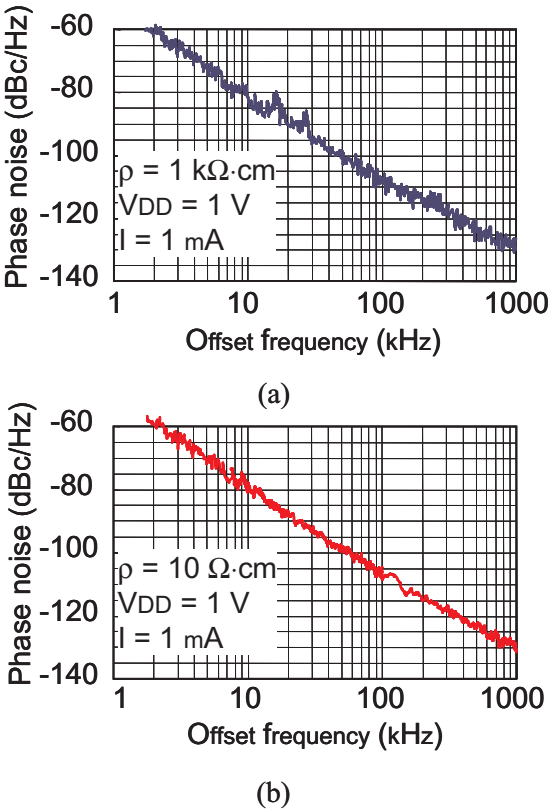


Fig. 5.38 Phase noise characteristics of VCOs on (a) high-resistivity substrate and (b) low-resistivity substrate.

Since the Q of the spiral inductor is not very high (Q = 4 at a frequency of 2 GHz for the low-resistivity substrate), the phase noise characteristics are inferior to those of recently reported VCOs. They can be improved by using a thick metal on-chip spiral inductor to raise Q. The fact that there is no hump in the phase noise spectrum means that there is no degradation due to other noise contributors [5.15].

The phase noise at an offset frequency of 1 MHz was measured as a function of operating current at an operating voltage of 1 V (Fig. 5.39). The data are better for the high-resistivity than for the low-resistivity substrate, with the difference being about 1 dB. Since phase noise is inversely proportional to Q^2, the use of a high-resistivity substrate improves Q by about 15%.

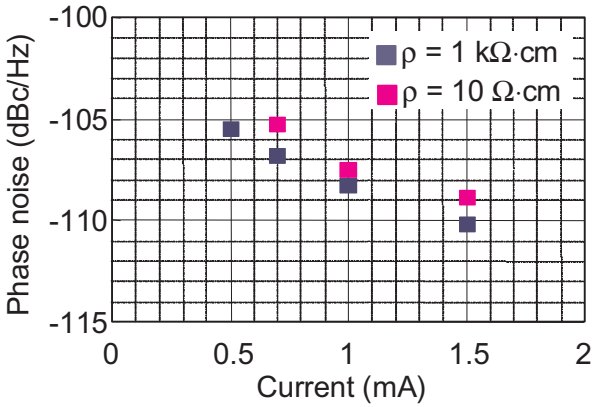


Fig. 5.39 Phase noise vs. operating current for two VCOs.

From the key characteristics of the two FD-SOI LC-VCOs (Table 5.1), it is clear that the FD-SOI process enables the fabrication of ultralow-power (< 1 mW) VCOs.

Table 5.1 Characteristics of FD-SOI VCOs.

Substrate resistivity (Ω·cm)	1000		10	
Supply voltage (V)	1			
Current (mA)	1.0	0.5	1.0	0.7
f_0 (GHz)	2.206	2.235	2.063	2.108
TR (%)	18.6	19.5	17.7	18.1
Phase noise (dBc/Hz) for f_{offset} = 1 MHz	-108.3	-105.5	-107.5	-105.3
Figure of merit (FOM)	175.9	273.3	174.4	172.5

We can use the figure of merit (FOM) defined in the following equation to compare the performance of LC-VCOs made on FD-SOI and bulk CMOS processes.

$$\mathrm{FOM} = 10 \cdot \log\left(\frac{f_0}{1\,\mathrm{GHz}} \cdot \frac{1\,\mathrm{MHz}}{f_{\mathrm{offset}}} \cdot \frac{1}{\mathrm{CN}} \right), \tag{5.24}$$

where f0 is the oscillation frequency, f_{offset} is the offset from the oscillation frequency, and CN is the phase noise.

The dependence of FOM on power consumption (Fig. 5.40) for FD-SOI LC-VCOs and recently reported bulk CMOS LC-VCOs shows that FD-SOI devices consume less power. The numbers from [1] to [4] in Fig. 5.40 correspond to references [5.11] to [5.14], respectively. It should be possible to further boost the performance by improving the Q of the inductor. It can be concluded that the FD-SOI process enables fabrication of the low-power VCOs needed for the realization of ubiquitous networking.

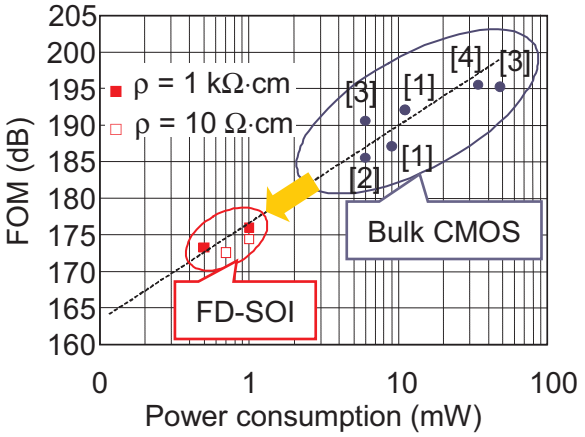


Fig. 5.40 Figure of merit for FD-SOI and bulk CMOS VCOs.

5.2.8 Limiting Amplifiers

Because the RF gain stage has to amplify not only the desired signal but also undesired strong signals, the RF gain should be set to a moderate level to avoid intermodulation distortion and desensitization. So, the IF gain stage is given sufficient gain after channel selection, which makes the desired signal dominant. In frequency modulation schemes, such as Gaussian-filtered frequency shift keying (GFSK), the envelope is constant and only phase information is used, thus enabling the use of limiting amplifiers.

In the limiting amplifier in Fig. 5.41, six differential unit amplifiers are cascaded to obtain a small signal gain of about 60 dB. Because of the DC connection, the DC offset voltages must be cancelled to avoid undesired effects, such as gain saturation at low input levels. The output DC levels are negatively fed back to the first stage through a low-pass filter consisting of large resistors and large external capacitors, thereby allowing each unit amplifier to be optimized to produce the maximum gain.

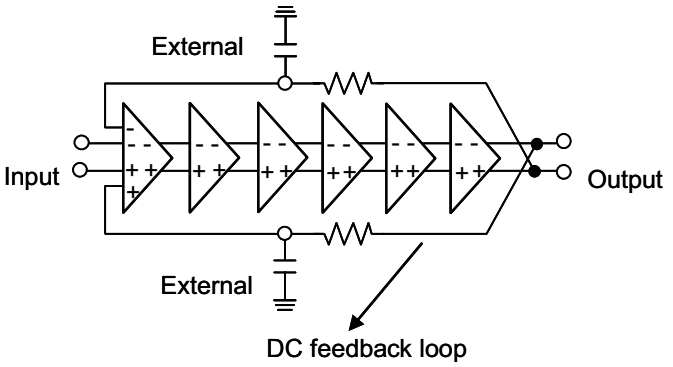


Fig. 5.41 IF-stage limiting amplifier with DC feedback loop.

The first-stage amplifier (Fig. 5.42) has two differential nMOSFET pairs and common nMOSFET loads. One differential pair constitutes a signal amplifier, and the other pair is used for the negative DC feedback. The unit amplifiers following the first stage are conventional differential amplifiers with nMOSFET loads.

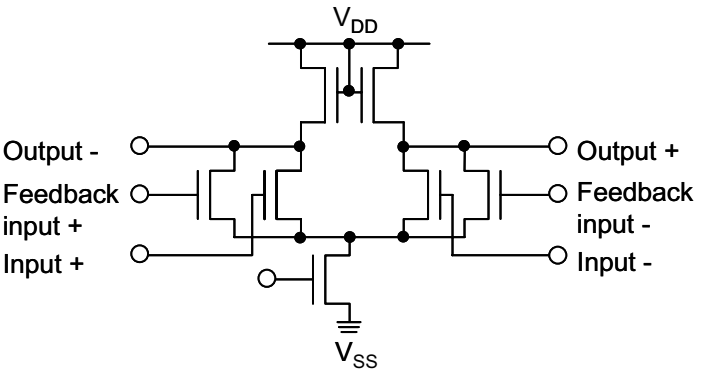


Fig. 5.42 Input amplifier with dual inputs.

The measured characteristics (Fig. 5.43) of a limiting amplifier fabricated on a 0.2-µm CMOS/SOI process show the small-signal gain to be about 60 dB and the limiting output level to be –12 dBm at input levels of over –70 dBm. The power dissipation is 2.1 mW at a supply voltage of 1 V and an operating frequency of 6 MHz.

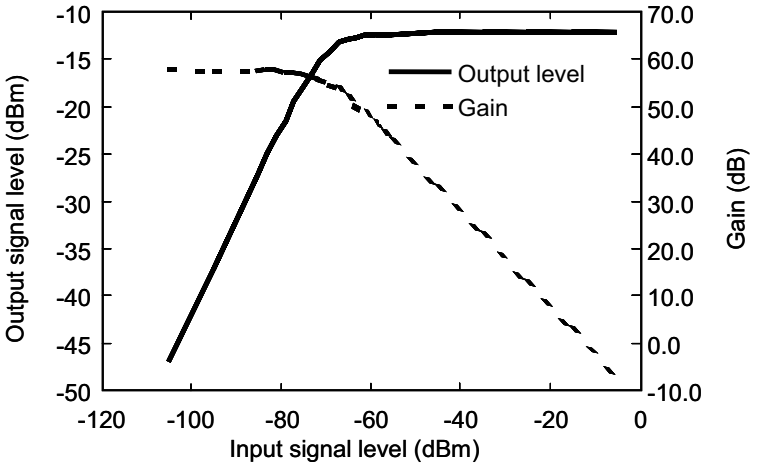


Fig. 5.43 Measured characteristics of limiting amplifier.

5.2.9 gm-C Filters

An RF transceiver requires a channel selection filter in the receiver and a Gaussian or Nyquist pulse-shaping filter in the transmitter. On-chip filtering is indispensable to reducing the size and cost of an RF module. This section describes a g_m-C filtering technique for a supply voltage of 1 V.

First of all, the principle of a g_m-C filter (Fig. 5.44) is explained. An LC low-pass filter (LPF) (Fig. 5.44 (a)) can, for instance, be converted into a g_m-C filter (Fig. 5.44 (b)) by replacing the real inductor (L) with an equivalent inductor ($L = C \cdot g_m^{-2}$) consisting of four g_m cells and one capacitor. The gm cell produces a current signal proportional to the differential-input voltage and ideally has an infinite output impedance. In a conventional gm cell (Fig. 5.44 (c)), transistors M_1 and M_2 operate in the triode region and provide an output current (I_{OUT}) proportional to the differential voltage (V_D). The drain currents (I_{D1} and I_{D2}, respectively) of the two transistors are

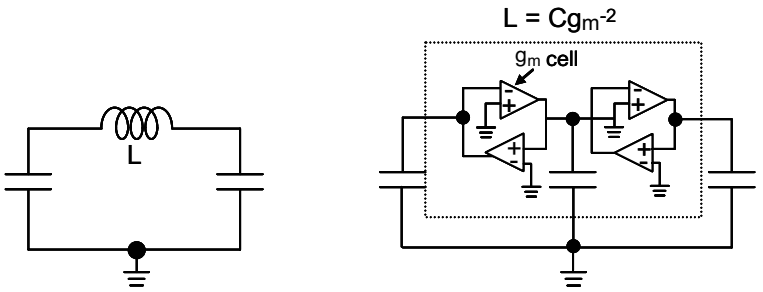
$$I_{D1} = \beta[(V_{1P} - V_{th})V_C - V_C^2] \tag{5.25}$$

$$I_{D2} = \beta[(V_{1N} - V_{th})V_C - V_C^2], \tag{5.26}$$

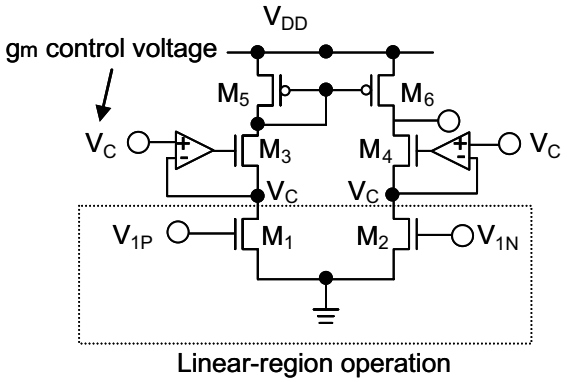
where β is determined by the carrier mobility, the capacitance, and the ratio of gate width to gate length. Thus, the output current is proportional to the control voltage (V_C):

$$I_{OUT} = I_{D1} - I_{D2} = \beta(V_{1P} - V_{1N})V_C = \beta V_D V_C . \tag{5.27}$$

The low-voltage gm cell in Fig. 5.45 has a folded structure so that it can operate at 1 V and provide the maximum input and output dynamic range [5.16][5.17]. The input and output stages are folded using current-mirror circuits. The undoped pMOSFETs produce a constant gm because the drain-to-source voltage is constant in the input stage. They operate in the triode region, even when the input signal is large, thus improving the input dynamic range and linearity. The control signal (V_C) adjusts the value of gm by means of a regulated-cascode configuration. The output stage has a regulated-cascode structure to enhance the output impedance. The common-mode feedback circuit rejects common-mode noise and fixes the output DC level. The regulated-cascode structure consists of an undoped transistor and a differential amplifier.



(a) (b)



$V_{1P} = V_D/2 + V_{CM}$
$V_{1N} = -V_D/2 + V_{CM}$

(c)

Fig. 5.44 Configuration of g_m-C filter. (a) Original C-L-C low-pass-filter, (b) g_m -C filter after replacement of inductor in (a) with g_m -C circuits, and (c) g_m cell.

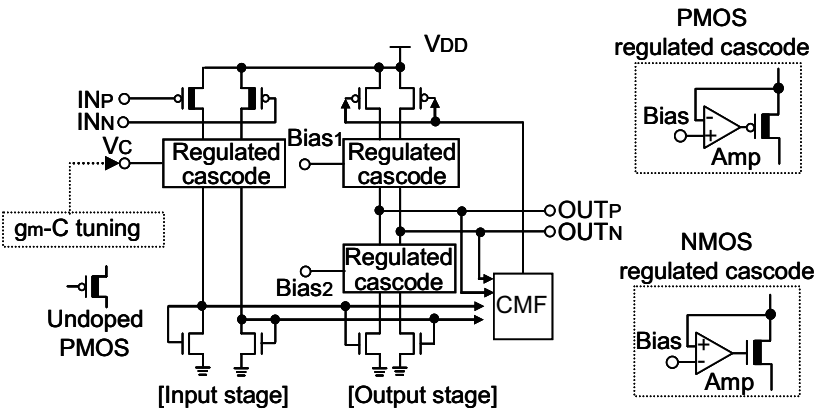


Fig. 5.45 gm cell for 1-V operation.

The architecture of a gm-C tuning circuit is shown in Fig. 5.46. The circuit receives a 1-MHz reference signal produced from the reference frequency signal of an external crystal and generates the control voltage (V_C). V_C modifies gm so as to stabilize the filter characteristics against variations in process, temperature, and supply voltage. Two gm cells and two capacitors form a 90° phase shifter for the 1-MHz reference signal. The mixer detects the phase difference (φ) between the reference signal and the signal output by the phase shifter based on the following equation:

$$\cos \omega t \cdot \sin(\omega t + \varphi) = [\sin \varphi + \sin(2\omega t + \varphi)] / 2 \cong \varphi / 2 . \qquad (5.28)$$

A feedback loop with an operational amplifier maintains the phase shift at 90°. Therefore, the generated control voltage keeps the C/gm time constant at a fixed value. This tuning circuit needs only two gm cells, and is thus advantageous for low-power operation.

The gain response (Fig. 5.47) of the gm-C low-pass filter was measured at operating voltages between 0.8 and 1.5 V. This filter is a third-order Butterworth filter with a 1-MHz bandwidth. The control voltage from the gm-C tuning circuit ensures that the cutoff frequency of the filter characteristics is kept constant, regardless of variations in supply voltage.

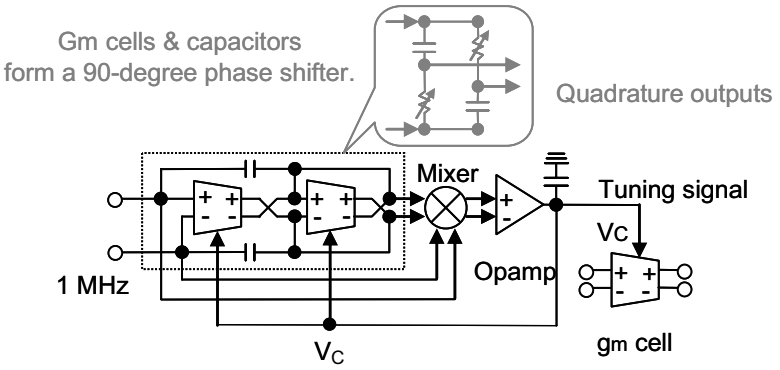


Fig. 5.46 gm-cell tuning circuit.

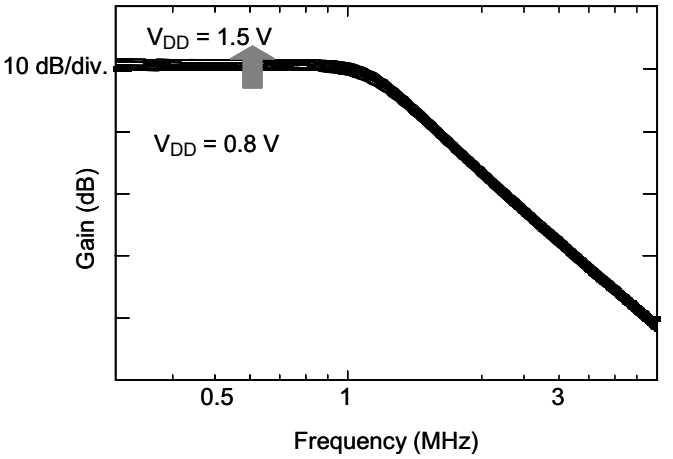


Fig. 5.47 Measured characteristics of LPF.

5.3 A/D and D/A Converters

In analog signal processing LSIs with a feature size of 0.1 μm or less, digital signal processing (DSP) methods, which allow low-voltage operation, are widely used because, in principle, they do not reduce the S/N ratio. However, the A/D and D/A conversion circuits that serve as front ends for analog blocks can degrade the accuracy because digital processing provides less accuracy than the required accuracy. So, A/D and D/A conversion circuits are a major factor determining accuracy. Two problems that arise with devices operating at a low supply voltage of about 1 V or less are lower speed due to the lower VGS and a smaller SNR due to the narrower dynamic range. One solution is to reduce the threshold voltage. From the relationship between the supply voltage of a push-pull amplifier and the unity-gain frequency (which corresponds to gain-bandwidth product) (Fig. 5.48), we can see that reducing the threshold voltage greatly improves the operating speed at supply voltages below 1 V.

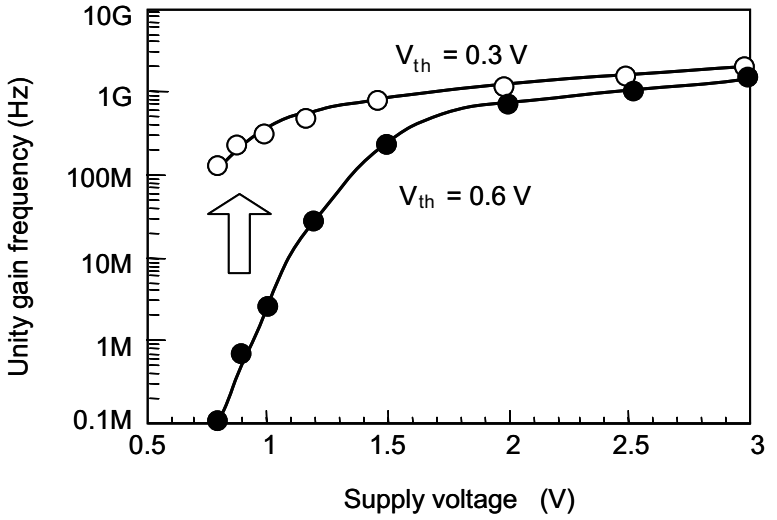


Fig. 5.48 Effect of lowering threshold voltage on amplifier characteristics.

However, it also tends to increase the leakage current, which results in a large degradation in accuracy in an analog circuit operating in the charge or current mode. The low leakage current of SOI transistors prevents the degradation in accuracy due to the leakage current, thus allowing the threshold voltage to be reduced.

This section describes the design of low-voltage A/D and D/A converters made with SOI transistors, a cyclic A/D converter based on switched-capacitor (SC) circuit technology, a sigma-delta A/D converter with improved accuracy, and a current-steering D/A converter with improved speed.

5.3.1 Cyclic A/D Converter

Many applications require low-power circuits. In sensor networks, for instance, low-power circuits provide sensor nodes with a long battery life. A cyclic A/D converter is suitable for the front end of the sensors in the nodes.

A. Comparison with pipeline A/D converter

In contrast to a pipeline converter (Fig. 5.49 (b)), which has multiple stages and feeds the residue forward to the next stage, a cyclic A/D converter (Fig. 5.49 (a)) has only a one-stage comparator because the amplified residue is fed back and all the bits are calculated successively. If we let n be the bit resolution of the converter and m be the bit resolution of a single stage, then a pipeline converter requires n/m stages. So, the cyclic type is smaller than the pipeline type.

A converter consumes two kinds of power: dynamic power, which is consumed during a conversion operation, and static power due to the bias current and so on. So the power consumptions of the two types of converters are given by

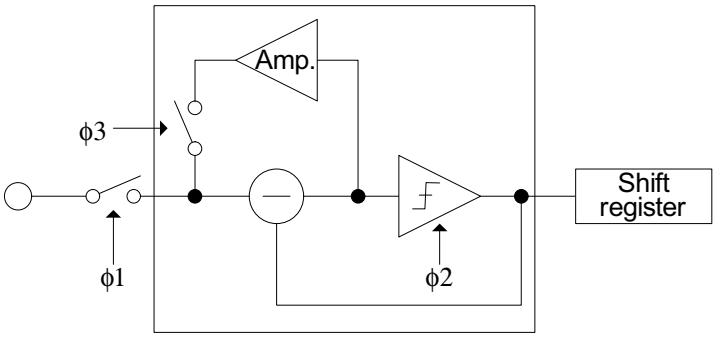
$$P_{cyclic} = DP_{cyclic} + SP_{cyclic}, \tag{5.29}$$

$$P_{pipeline} = \frac{n}{m} \cdot DP_{pipeline} + \frac{n}{m} \cdot SP_{pipeline}, \tag{5.30}$$

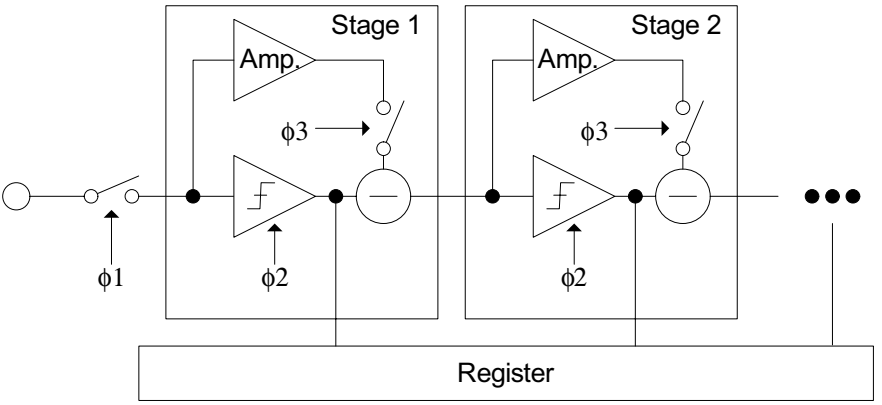
where DP and SP are the dynamic and static power of a single stage, respectively. For a given sampling frequency, the operating speed of one stage of the cyclic converter is n/m times faster than that of the pipeline type.

So, the relationship between the cyclic type and the pipeline type for the dynamic power is given by:

$$DP_{cyclic} = \frac{n}{m} \cdot DP_{pipeline} \,. \tag{5.31}$$



(a) Cyclic A/D converter



(b) Pipeline A/D converter

Fig. 5.49 Block diagrams of cyclic and pipeline A/D converters.

In general, a pipeline converter consumes less power than a cyclic one because the slower stages of the pipeline converter employ lower supply voltages. But this is not true when the supply voltage is fixed or when the supply voltage cannot be lowered any further. The comparator and op-amp in a stage need reference voltages, which are generated by a current-mirror circuit or a ladder resistance. The power consumed by a pipeline converter for reference-voltage generation cannot be made *m/n* times lower than that consumed by a cyclic one. So, a pipeline converter consumes more static power than a cyclic one:

$$SP_{cyclic} < \frac{n}{m} \cdot SP_{pipeline} . \tag{5.32}$$

Moreover, the leakage current of transistors is not negligible in low-power circuits; and a much larger current flows in a pipeline converter because of the large size of the circuit. From equations (5.29) to (5.32), it is clear that a cyclic A/D converter consumes less power than a pipeline one:

$$P_{cyclic} < P_{pipeline} . \tag{5.33}$$

B. Advantages of FD-SOI technology for low-voltage SC circuit

Analog switches, especially switched-capacitor circuits, are widely used in analog circuits because of their high accuracy. But at voltages below 1 V, the degradation in the on-conductance of an analog switch is a serious problem. In the switch of a sample-and-hold (S/H) circuit (Fig. 5.50), the source voltage is biased at around $V_{DD}/2$, and V_{gs} is also around $V_{DD}/2$, which is close to the threshold voltage (V_{th}). This results in a small on-conductance and seriously degrades the switching speed. Moreover, an analog switch made with bulk devices exhibits body effects because the source terminal is biased at $V_{DD}/2$; and the effects increase V_{th}, which is fatal for low-voltage operation. So, a conventional RC technique [5.18] is commonly used.

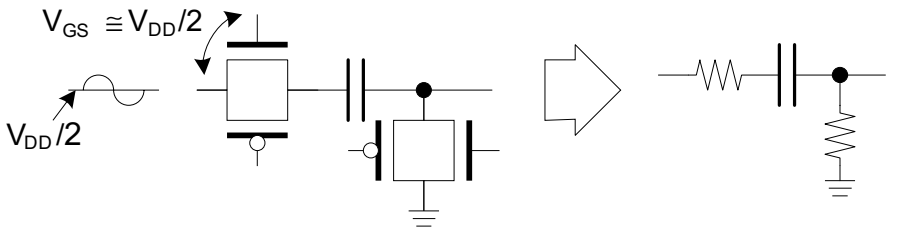
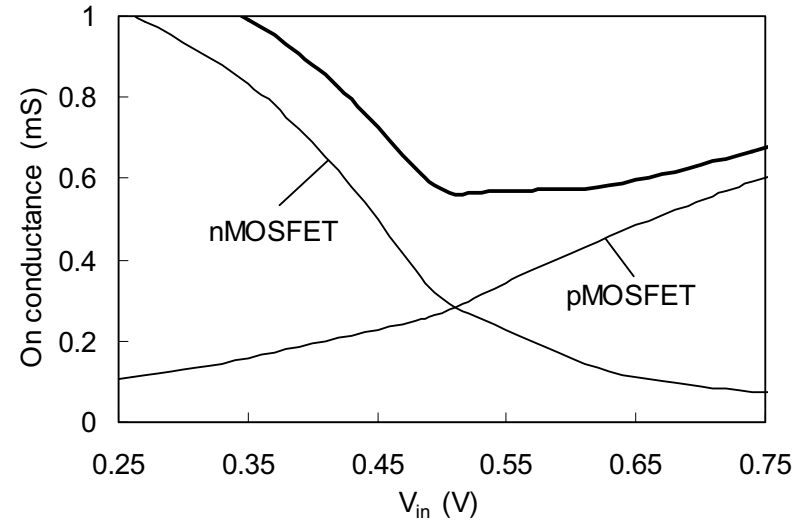


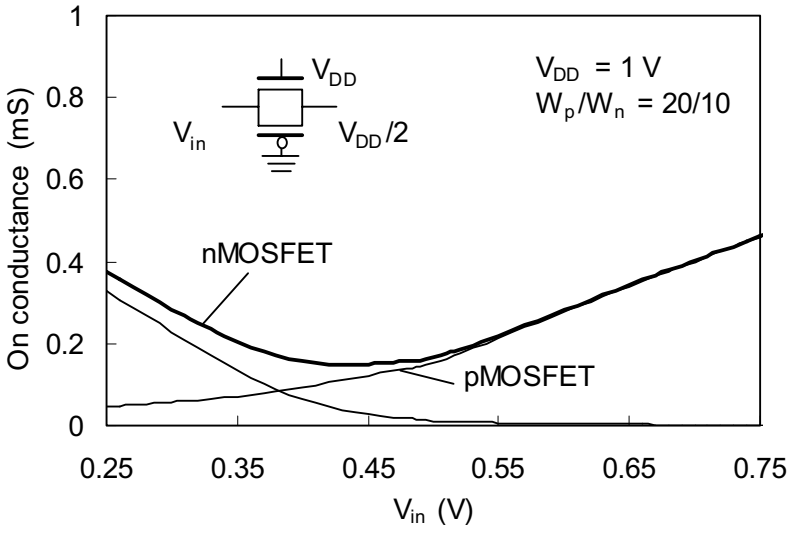
Fig. 5.50 Schematic and simple model of analog switch.

One way to overcome these problems is to use FD-SOI devices for analog switches. The body effects are negligible because the body floats electrically and the voltage to it is always near the source voltage. This is one advantage of FD-SOI devices over bulk ones. Moreover, FD-SOI devices have steep subthreshold characteristics that enable the use of a lower V_{th}. As a result, an A/D converter with an FD-SOI S/H circuit can function at a lower supply voltage. The simulation results in Fig. 5.51 show how on-conductance depends on input voltage for a CMOS TG-type analog switch. V_{DD} was assumed to be 1 V, and the threshold voltages of the FD-SOI and bulk devices were set so as to make the leakage current the same for both types. The on-conductance is larger for the FD-SOI switch than for the bulk one, which means that the FD-SOI switch has a faster settling time for a given supply voltage, and that it provides a higher accuracy for a given sampling frequency.

The accuracy of an A/D converter depends on the characteristics of the analog switches it contains. Lowering V_{DD} makes the on-conductance smaller and the settling time longer. This limits the sampling frequency, and thus the accuracy, of the converter. The simulation results in Fig. 5.52 show the relationship between V_{DD} and maximum sampling frequency for cyclic A/D converters for 8-bit accuracy. With an FD-SOI converter, V_{DD} can be set as low as 0.9 V at a sampling frequency of 8 kHz, which is the frequency used for voice signals; whereas the V_{DD} for the bulk converter is 1.4 V. Considering battery operation, the ability to function at a low voltage below 1 V is a big advantage of low-power devices.



(a)



(b)

Fig. 5.51 Characteristics of low-voltage analog switches made with (a) FD-SOI and (b) bulk devices.

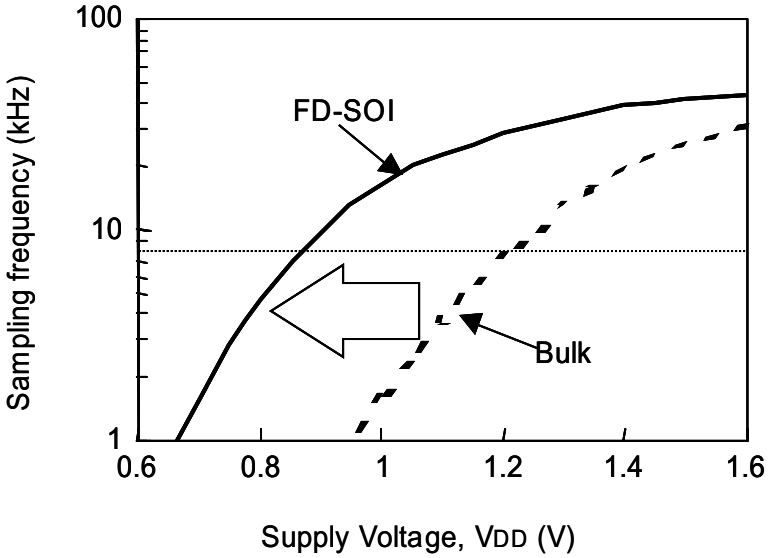


Fig. 5.52 Sampling frequency vs. supply voltage for FD-SOI and bulk A/D converters.

C. Circuit technique for suppressing leakage current

A/D converters for low-power devices have to handle a wide range of sampling frequencies. The FD-SOI S/H circuit described above is useful for a high sampling frequency of several kilohertz. At a low sampling frequency, such as tens of hertz, however, the degradation in accuracy due to leakage current cannot be ignored. Furthermore, the consumption of power by the DC current in the analog block is wasteful because the block remains active during the entire sampling period, even after conversion is complete.

A new clocking technique that suppresses the degradation in accuracy and manages the power consumption solves these problems. In the new scheme (Fig. 5.53), the clock has the highest sampling frequency. At a low frequency, after conversion is complete, the A/D converter sleeps until the next sampling period. As a result, the active time is only 125 μs for all sampling frequencies. In contrast, with the conventional scheme, it is 10 ms at a sampling frequency of 100 Hz (Fig. 5.53). The power consumption for the new scheme is 1/80 that for the conventional one.

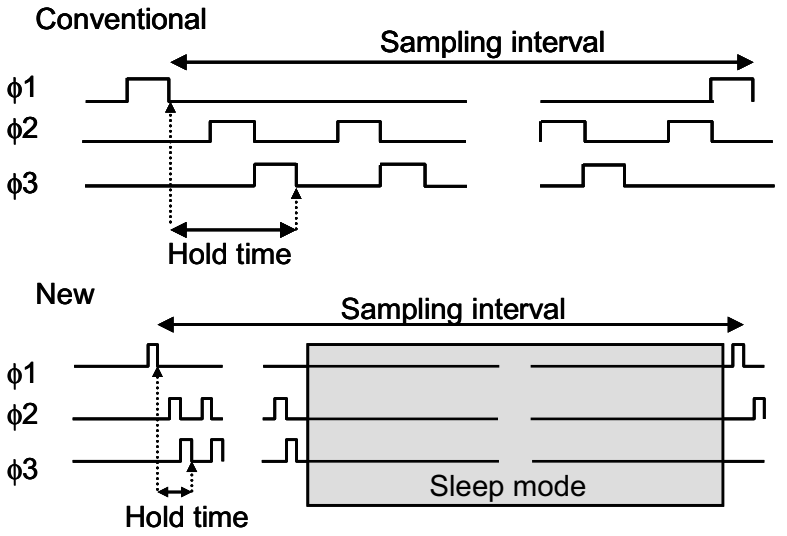


Fig. 5.53 Timing charts of conventional and new clocking schemes.

Figure 5.54 shows how effective the technique is in suppressing the degradation in accuracy. The total voltage drop is as small as 60 μV, and the accuracy is as high as 12 bits. For the conventional scheme, the values are 2.3 mV and 6 bits, respectively, at a sampling frequency of 100 Hz.

As the output impedance of the circuit in front of the A/D converter increases, the tracking speed of the S/H circuit falls, which may increase distortion and reduce the accuracy of the S/H circuit. In this case, inserting a unity gain buffer, such as a voltage follower, between the circuit and the converter decreases the output impedance and suppresses the degradation in the performance of the converter. The new clocking scheme can also switch the buffer off during the sleep mode to save power.

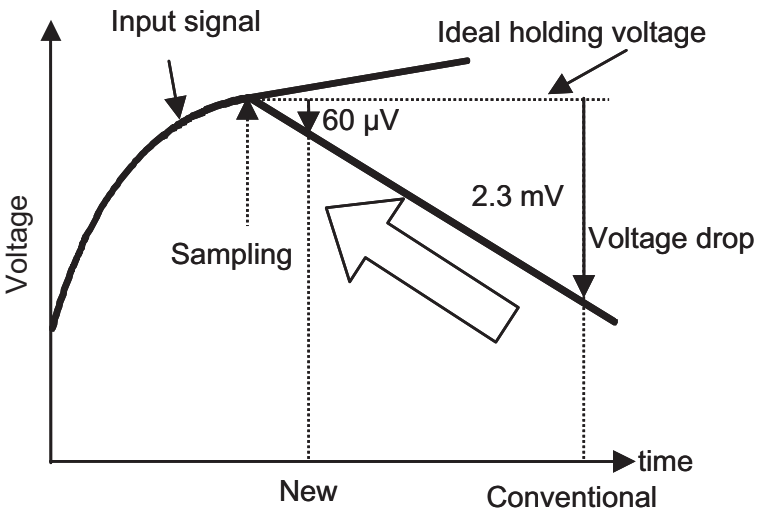


Fig. 5.54 Degradation in accuracy due to leakage current.

D. Example of cyclic A/D converter

A cyclic A/D converter (Fig. 5.55) was designed and fabricated on a 0.2-μm CMOS/SOI process. The core size is 0.5 mm x 2.0 mm. The active power consumption is 350 μW at 8 kHz. It can handle sampling frequencies from 8 Hz to 8 kHz. The spectrum of a 100-Hz input signal at a sampling frequency of 1 kHz is shown in Fig. 5.56. The signal-to-noise and distortion ratio (SNDR) is 32 dB, which indicates that the effective number of bits (ENOB) is 5.0. The specifications of the converter are listed in Table 5.2.

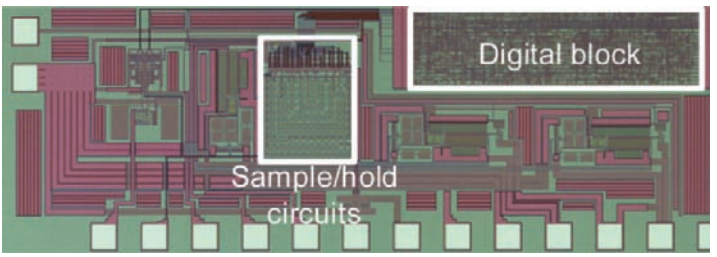


Fig. 5.55 Microphotograph of fabricated A/D converter.

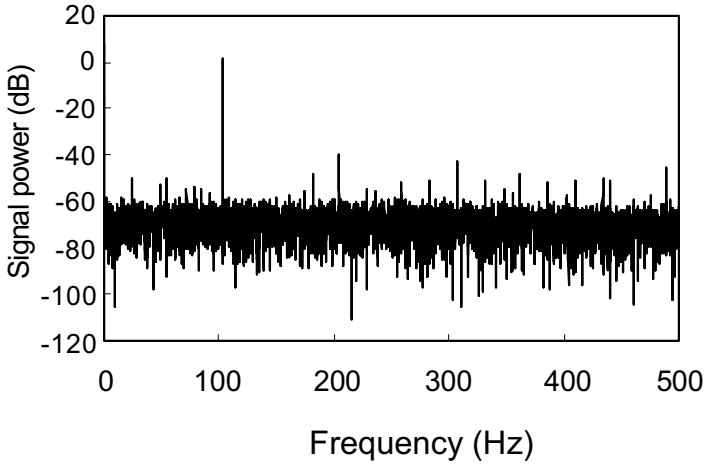


Fig. 5.56 Spectrum of A/D converter output.

Table 5.2 Specifications of A/D converter.

Resolution:	8 bits
Sampling frequency:	8 Hz - 8 kHz
Signal-to-noise ratio:	32 dB (ENOB: 5.0)
Process:	0.2-μm CMOS/SOI
Area:	1 mm^2
Supply voltage:	1 V
Power consumption:	350 μW @ 8 kHz

An A/D converter for low-power devices should be small, consume little power, and be able to handle various sampling frequencies and resolutions. Cyclic architecture has advantages over pipeline architecture in that it yields a smaller circuit that consumes less power at a given supply voltage because the static power consumption is lower. Moreover, since an FD-SOI analog switch has a larger on-conductance and better accuracy than a bulk one at a given voltage, an A/D converter made with FD-SOI analog switches can provide the same accuracy and handle the same sampling frequency at a lower supply

voltage. A fabricated cyclic A/D converter exhibits an SNDR of 32 dB and consumes 350 μW of power at a sampling frequency of 8 kHz.

5.3.2 Sigma-Delta A/D Converter

Sigma-delta A/D conversion requires neither an S/H circuit, which must have a high accuracy, nor weighted circuits, which are greatly affected by process variations. The principle of first-order sigma-delta modulation is illustrated in Fig. 5.57. Sigma-delta modulation, which shapes the quantization-noise spectrum and suppresses the noise at lower frequencies, makes it possible to obtain a high accuracy even if a low-accuracy quantizer is used. Furthermore, it improves accuracy by increasing the sampling rate. Increasing the oversampling rate to improve accuracy matches the trend in digital circuits to achieve higher speed with scaled-down devices. So, it is suitable for low-voltage operation. This section describes the design of a very accurate A/D converter based on sigma-delta modulation that operates at a supply voltage of 1 V or less.

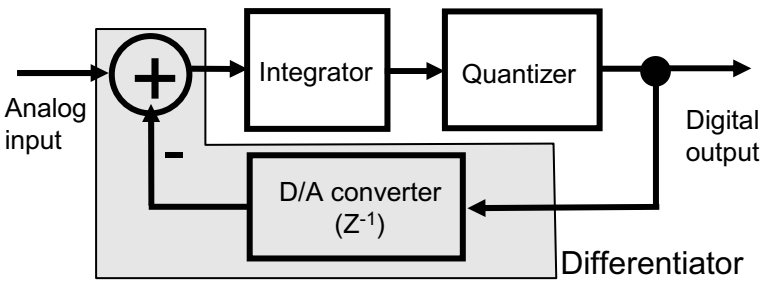


Fig. 5.57 Principle of first-order sigma-delta modulator.

A. Effectiveness of sigma-delta modulation

If we let Q be quantization noise, which is a basic parameter of an A/D converter, N_q be the circuit noise generated by the quantizer itself, X be the input, and z be the z-function, then the output (Y) of a simple sigma-delta modulator is

$$Y = X + \left(1 - z^{-1}\right)Q + \left(1 - z^{-1}\right)N_q . \tag{5.34}$$

The shaping factor ($1-z^{-1}$) affects both the quantization noise and the circuit noise of the quantizer. A high oversampling frequency from 64 to 256 times the Nyquist frequency makes ($1-z^{-1}$) very small, thus providing high-accuracy conversion with a low quantization error. Since accuracy increases with sampling frequency, it is not affected very much by a reduction in supply voltage. This feature makes the method suitable for obtaining high accuracy at a supply voltage of 1 V or less.

B. Differential operation at low voltages

As explained above, the quantizer does not determine the accuracy of a noise-shaping A/D converter, as it does for ordinary A/D converters. The major factor determining the accuracy is the integrator. A full-differential integrator provides higher integrator accuracy because it suppresses external noise, power supply noise, etc. The simplest full-differential integrator (Fig. 5.58) consists of a differential amplifier, a resistor, and a capacitor.

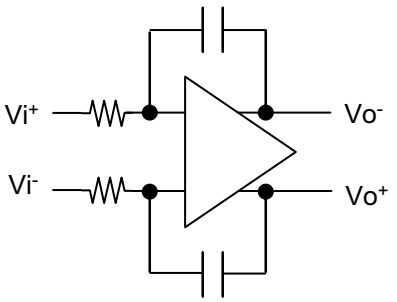


Fig. 5.58 Configuration of full-differential integrator.

In a differential amplifier with common-mode feedback circuits (Fig. 5.59), the common-mode feedback circuit fixes the DC bias level of the output. However, if the supply voltage of the amplifier is very low, common-mode feedback circuits cause oscillations, large ringing, and other unstable behavior, because the current drivability of the MOSFETs in the feedback circuits and the feedback gain are poor at low voltages.

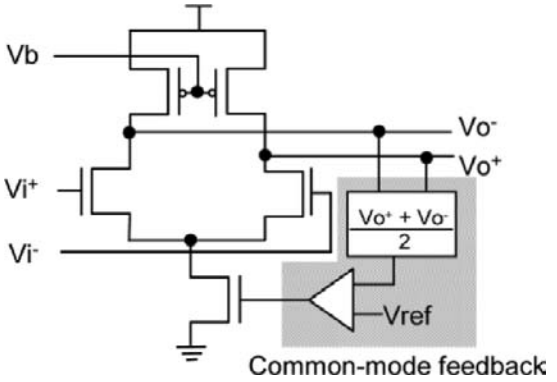


Fig. 5.59 Schematic of differential amplifier.

One way to cope with that problem is to use a pseudo-differential circuit based on a single-ended differential amplifier, which does not require common-mode feedback and can operate at low voltages, yet is just as effective as a full-differential circuit. Figure 5.60 illustrates such a circuit for use in an A/D converter.

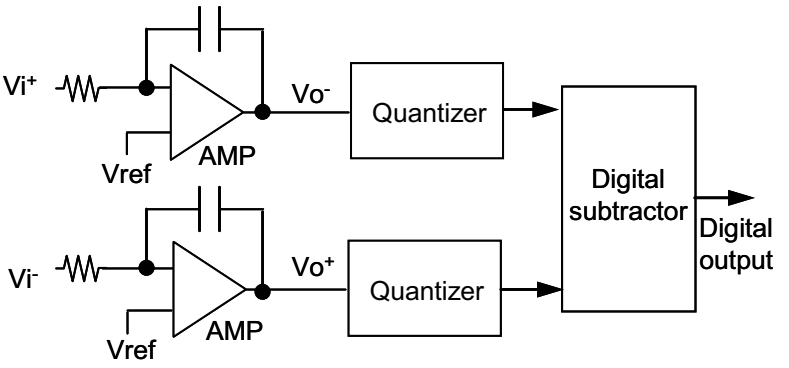


Fig. 5.60 Diagram of pseudo-differential integrator and quantizer circuit.

This method involves first inputting the differential signal into two single-ended differential amplifiers and digitization using the single input of

the quantizer, followed by differential processing by a digital subtractor. Thus, the amplifier can be a simple single-ended differential amplifier, which operates stably even at low voltages. Furthermore, although both the structure and operation of a 2-bit or higher differential quantizer are complex, the pseudo-differential configuration solves the problem by enabling the use of the simplest voltage comparator configuration. In an analog circuit, addition can be carried out simply by current summing, etc.; but subtraction requires a differential amplifier or other such device, which makes the scale of the analog circuit so large that low-voltage operation becomes problematic. In a pseudo-differential circuit, however, subtraction can be carried out with a digital subtractor, which is not readily affected by low voltages; so, this method is suitable for low-voltage differential designs.

C. Performance of sigma-delta A/D converter at voltages below 1 V

An example of a continuous-time-integration sigma-delta A/D converter that employs a pseudo-differential configuration is shown in Fig. 5.61. One feature of this circuit is that the shaping module can be implemented with a simple amplifier, resistors, and capacitors. That eliminates the circuit elements of the common-mode feedback circuit and the analog switch, which exhibit poor performance at low supply voltages.

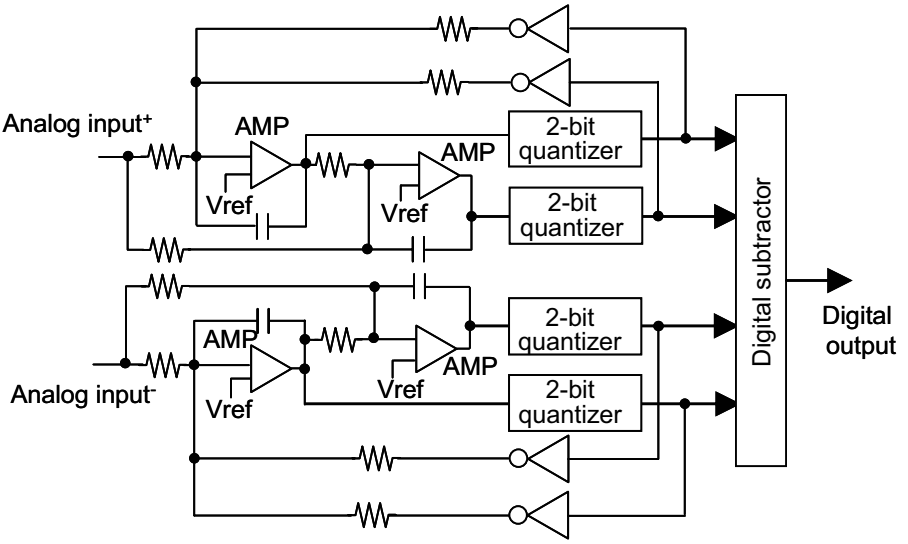


Fig. 5.61 Pseudo-differential second-order sigma-delta A/D conversion circuit.

The A/D converter was fabricated on a 0.35-μm FD-SOI CMOS process. The gate oxide was 7 nm thick; the active-Si layer, 50 nm thick; and the buried oxide, 100 nm thick. The absolute value of the threshold voltage was 0.15 V. A MIM capacitor was also used.

The output spectrogram (Fig. 5.62) was measured for 0-dB (0.125-Vpp) 1-kHz sine-wave input at a supply voltage of 0.5 V. There is secondary and tertiary high-frequency distortion at a power level of about -80 dB. The noise floor is -70 dB in the audio band and -90 dB in the 200-kHz band (baseband for communications: 400 kbps). The SNR characteristics, which include the total harmonic distortion (THD), for a power level of 78 dB were obtained in the 20 kHz band for 0-dB input and a dynamic range of 72 dB. They are equivalent to 14-bit accuracy, including an error of ±1/2 LSB.

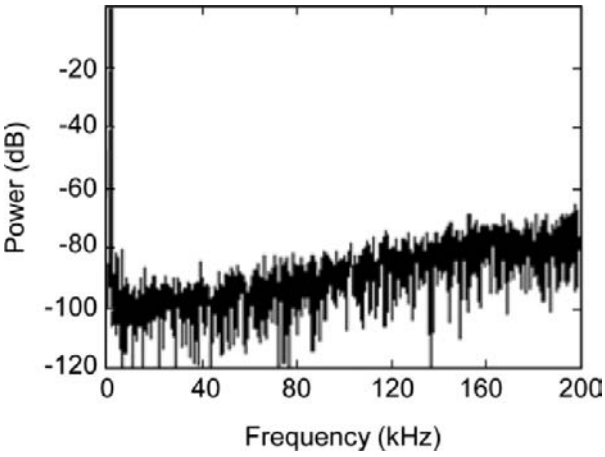


Fig. 5.62 Measured power spectrum of A/D converter.

The dependence of dynamic range on supply voltage (Fig. 5.63) shows that the converter operates at voltages between 0.5 V and 0.9 V. When the supply voltage is 0.9 V, the dynamic range increases to 84 dB. The characteristics for a 0.5-V power supply are listed in Table 5.3.

In summary, the use of SOI transistors and low-voltage circuit technology enables the fabrication of a 0-dB sigma-delta A/D converter that runs on a

supply voltage of 0.5 V. It provides 14-bit accuracy for audio use and 9-bit accuracy for digital-communications baseband use. These results demonstrate that a practical analog circuit can be implemented, even for a very low supply voltage of about 0.5 V, and that the SOI process makes feasible a highly accurate analog circuit that is suitable for use in consumer audio equipment.

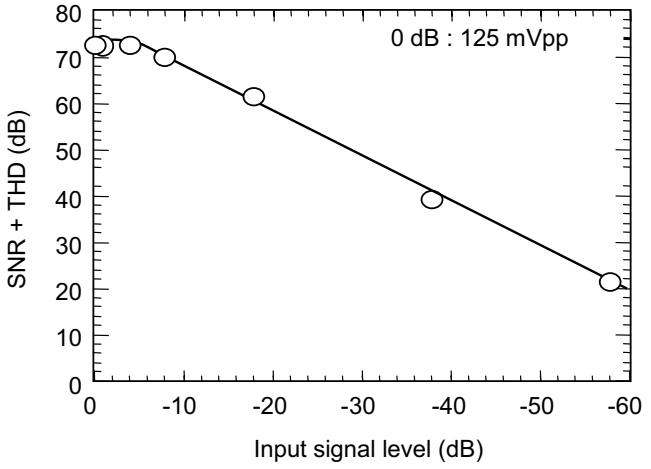


Fig. 5.63 Measured SNR performance of A/D converter.

Table 5.3 Performance of A/D converter.

Signal bandwidth	20 kHz	200 kHz
Resolution	14 bits	9 bits
SNR + THD	72 dB	55 dB
Dynamic range (DR)	78 dB	59 dB
Supply voltage	0.5 V	
Input dynamic range	125 mV (V_{DD} /4)	
Power consumption	1.3 mW	
Chip size	4 mm × 4 mm	

5.3.3 Current-Steering D/A Converter

Low-power digital-to-analog converters (DACs) are essential components of ultralow-power mobile systems. One promising candidate is a current-steering DAC because it consists mainly of current sources, switches, and a resistor load, which enables it to run on an ultralow supply voltage. This chapter describes a current-steering DAC made with FD-SOI devices.

First, this chapter explains the benefits of using FD-SOI devices for this type of circuit, and also the key points of the circuit design. Then, the typical characteristics of an SOI DAC are presented. Finally, the problem of device mismatch when using FD-SOI circuits, which is an important design consideration for current-steering DACs, is considered.

A. Benefits of using FD-SOI devices

The use of FD-SOI devices for analog circuits provides better frequency performance than that obtainable with bulk CMOS devices because the capacitances are lower, the current drivability is higher, there are no body effects, and so on. In addition, the smaller substrate coupling provides lower noise and helps prevent latch-up. These features make FD-SOI technology very useful for fabricating system LSIs with analog and digital blocks [5.19]. In addition, the low threshold voltage, the small influence of the drain-diffusion and junction capacitances, and the small body-bias effects markedly boost the dynamic performance, including the spurious free dynamic range (SFDR) and signal-to-noise ratio (SNR), which are especially important specifications for communication systems and networks. Finally, this technology makes it possible to fabricate a very high-performance current-steering DAC that operates at a supply voltage of less than 1.0 V.

A 10-bit current-steering DAC (Fig. 5.64) consists of current sources, current-switching circuits, a decoder for selecting the current source, bias circuits, and reference circuits. The input bits (D_0-D_9) of the decoder circuit control the current-switching circuits. This is a general structure in which the most significant bits are 4-bit thermometer coded, the middle bits are also 4-bit thermometer coded, and the least significant bits are 2-bit binary weighted. The outputs of the current sources are summed directly to a resistor load (R_L).

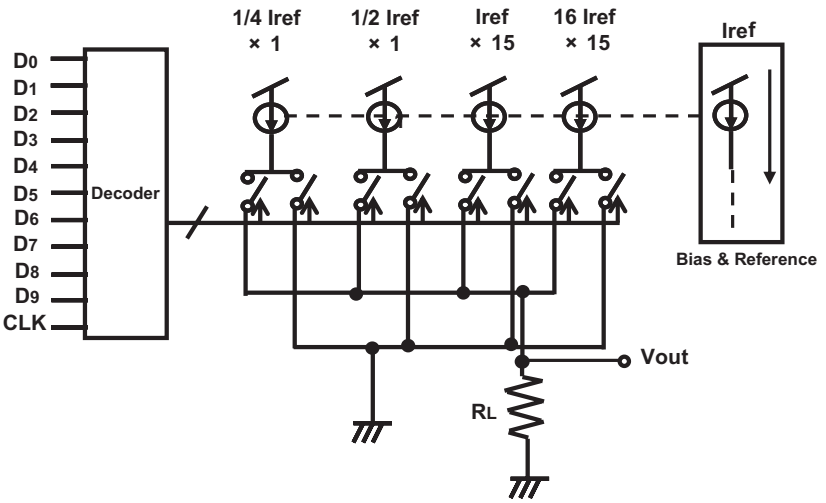


Fig. 5.64 Block diagram of 10-bit current-steering DAC.

B. Measured performance

To verify the effectiveness of the current-steering scheme, a 10-bit DAC was fabricated on a 0.35-μm FD-SOI process; and the linearity, settling performance, and power consumption were evaluated. The characteristics were measured at a sampling frequency of 60 MHz and a supply voltage of 1.0 V at room temperature. The integral nonlinearity error (INL) and differential nonlinearity error (DNL) are shown in Fig. 5.65.

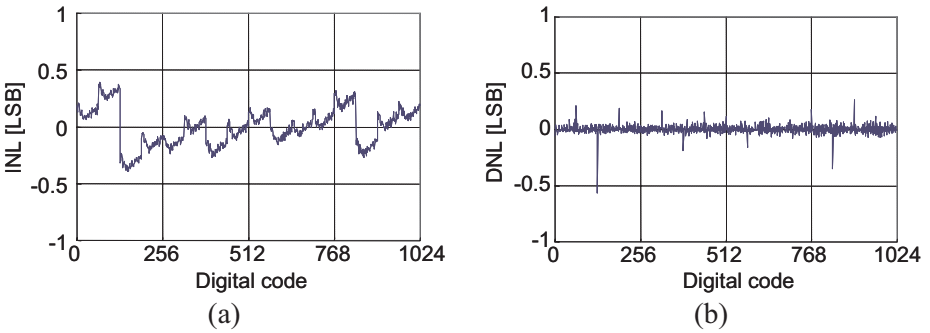


Fig. 5.65 Measured (a) INL and (b) DNL of 10-bit FD-SOI DAC.

The INL was found to be less than +0.67 LSB/-0.67 LSB and the DNL to be less than +0.6 LSB/-0.6 LSB. For comparison, the INL and DNL of a 3.3-V DAC made on a 0.35-μm bulk CMOS process were also measured (Fig. 5.66), and found to be almost the same as those of the SOI DAC. This demonstrates that a DAC made on an FD-SOI process can operate at an ultralow voltage with good linearity.

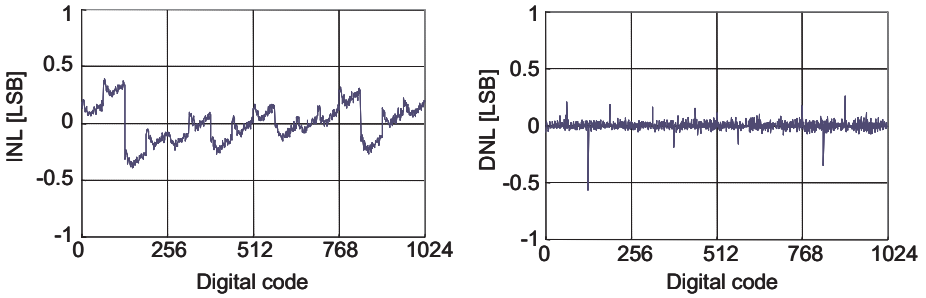


Fig. 5.66 Measured (a) INL and (b) DNL of 10-bit DAC made on 0.35-μm bulk CMOS process.

The dependence of linearity on supply voltage (Fig. 5.67) shows that this DAC maintains good performance at supply voltages below 1.0 V, which means that it is suitable for ultralow-power mobile systems.

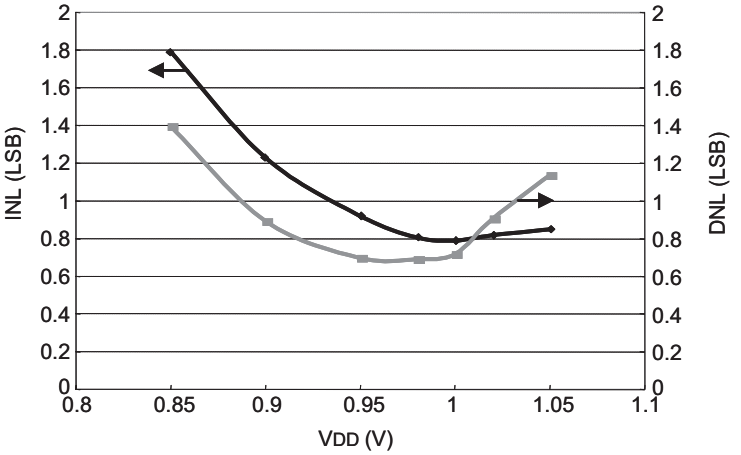


Fig. 5.67 Linearity vs. supply voltage.

The rise and fall settling times at a supply voltage of 1 V are 3.2 ns and 6.2 ns, respectively. The overshoot and undershoot are due to the parasitic elements of the test board. And the power consumption is 3.4 mW at a sampling frequency of 60 MHz.

C. Effects of device mismatch

The final topic is device mismatch. Accurate current sources and the reduction of device mismatch are critical design considerations for a current-steering DAC. For the DAC described above, the sizes of the current-source transistors were determined using a Monte-Carlo linearity error simulation with N = 1000, assuming that the transistor mismatch was the same for 0.35-μm FD-SOI and 0.35-μm bulk CMOS devices. The current distribution due to transistor mismatch is discussed below.

The output of a current-source transistor in the saturation region is given by the following equation [5.20]:

$$I \approx \frac{\beta}{2}(V_{GS} - V_{th})^2 \cdot (1 + \lambda V_{DS}), \tag{5.35}$$

where β is the transconductance, V_{GS} is the gate-source voltage, λ is the channel length modulation factor, and V_{DS} is the drain-source voltage.

The transconductance is given by

$$\beta = \mu_0 \bullet C_{OX} \bullet \frac{W}{L}, \tag{5.36}$$

where μ_0 is the charge mobility, C_{OX} is the gate oxide capacitance per unit area, W is the gate width, and L is the gate length.

Differentiating equation (5.35) with respect to V_{GS}, $V_{DS,}$ and λ yields

$$\frac{\Delta I}{I} = \frac{\Delta\beta}{\beta} + 2 \cdot \frac{\Delta V_{GS} - \Delta V_{th}}{V_{GS} - V_{th}} + \frac{\Delta\lambda \cdot V_{DS} + \lambda \Delta V_{DS}}{1 + \lambda V_{DS}}. \tag{5.37}$$

Based on equation (5.37) and assuming ΔV_{GS}, ΔV_{DS}, and $\Delta\lambda$ are very small, the equation for the current distribution (σ) is

$$\sigma^2\left(\frac{\Delta I}{I}\right) \approx \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{4\cdot\sigma^2(\Delta V_{th})}{(V_{GS} - V_{th})^2}. \tag{5.38}$$

Since $\Delta\beta/\beta$ and ΔV_{th} are given by

$$\frac{\Delta\beta}{\beta} = \frac{A_\beta}{\sqrt{WL}}, \tag{5.39}$$

$$\Delta V_{th} = \frac{A_{V_{th}}}{\sqrt{WL}}, \tag{5.40}$$

where A_β and A_{Vth} are constants of proportionality indicating the degree of transistor mismatch, the distributions of the normalized transconductance mismatch $\sigma^2(\Delta\beta/\beta)$ and the threshold voltage $\sigma^2(\Delta V_{th})$ are

$$\sigma^2\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta^2}{WL}, \tag{5.41}$$

$$\sigma^2(\Delta V_{th}) = \frac{A_{V_{th}}^2}{WL}. \tag{5.42}$$

So, we can write (5.38) as

$$\sigma^2\left(\frac{\Delta I}{I}\right) \approx \frac{A_\beta^2}{WL} + \frac{4}{(V_{GS} - V_{th})^2}\cdot\frac{A_{V_{th}}^2}{WL}. \tag{5.43}$$

Hence, to obtain well-matched transistors, they should be as close together as possible and as large as possible.

The effects of device mismatch on the linearity of the DAC were investigated by using a Monte-Carlo simulation. In the simulation, $A_{V_{th}}$ and A_β were assumed to be 2.90 mV·μm and 0.46%·μm respectively. The linearity error for N = 1000 is shown in Fig. 5.68. The results are similar to the measurement results (Fig. 5.65). Since the transistor mismatch ($A_{V_{th}}$ and A_β) is almost the same for FD-SOI and bulk CMOS devices, the measured linearity error for both is similar to the simulated linearity error. This means that FD-SOI devices are suitable for making DACs operating at an ultralow voltage.

Furthermore, when determining transistor size, we must consider not only mismatch between transistor pairs, but also transistor mismatch in the current-source array of the DAC, the parasitic resistance of the power lines to the current-source transistors, and the effects of various types of noise.

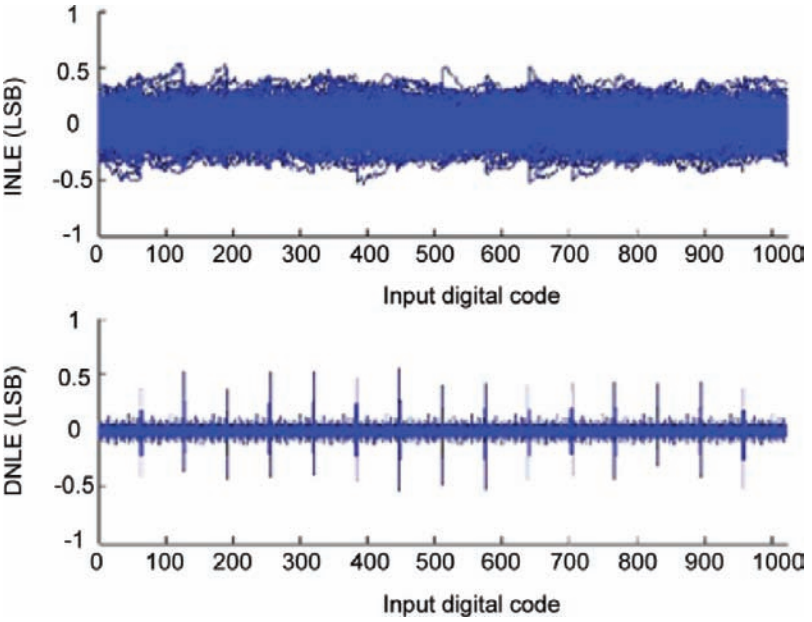


Fig. 5.68 Simulated linearity of 10-bit FD-SOI DAC.

5.4 DC-DC Converter

As mentioned in Chapter 4, a DC-DC converter is needed to reduce the supply voltage to 0.5 V for digital blocks and to 0.5-1.0 V for analog/RF blocks. Power conversion efficiency (η) is the most important factor, since it affects the battery life of mobile equipment.

5.4.1 Design of DC-DC Converter

Since batteries generally produce a voltage greater than 0.5 V, LSIs running on a supply voltage of 0.5 V require a voltage down-converter (DC-DC converter). An on-chip series regulator is a common method of reducing the supply voltage. However, its power conversion efficiency (η) is approximately determined by the ratio of output voltage to input voltage, and the η for generating 0.5 V from the battery voltage is less than 50%. Thus, a series regulator is not the best solution for mobile equipment, for which battery life is a primary consideration. Two converters are discussed below: a switched-capacitor-type converter and a buck converter; and η is a focal point for both.

5.4.2 Switched-Capacitor (SC)-Type Converter

This section explains the basics of generating $V_{DD}/2$ as an example of using capacitors for down-conversion (Fig. 5.69). The complementary control signals (ϕ, $\overline{\phi}$) connect the switching capacitor (C_{SW}) and the load capacitor (C_L) in series in one half cycle and in parallel in the next half cycle. When the control signals are applied during several cycles, the output voltage (V_{out}) converges to $V_{DD}/2$ when the capacitors are connected in parallel. Let us examine this in more detail.

Assuming that the load current through the output resistor (R_L) is negligible and thus has no effect on V_{out}, we can write V_{out} in the present cycle ($V_{out}^{(n)}$) as a function of V_{out} in the previous cycle ($V_{out}^{(n-1)}$) as follows:

$$V_{out}^{(n)} = \frac{2C_{SW}C_L}{\left(C_{SW}+C_L\right)^2}\cdot V_{DD} + \frac{\left(C_{SW}-C_L\right)^2}{\left(C_{SW}+C_L\right)^2}\cdot V_{out}^{(n-1)}. \tag{5.44}$$

In the steady state, where $V_{out}^{(n)} \approx V_{out}^{(n-1)} \equiv V_{out}$, V_{out} is then given by

$$V_{out} \approx \frac{V_{DD}}{2} \tag{5.45}$$

That is, V_{out} converges to $V_{DD}/2$ no matter what the values of C_{SW} and C_L are.

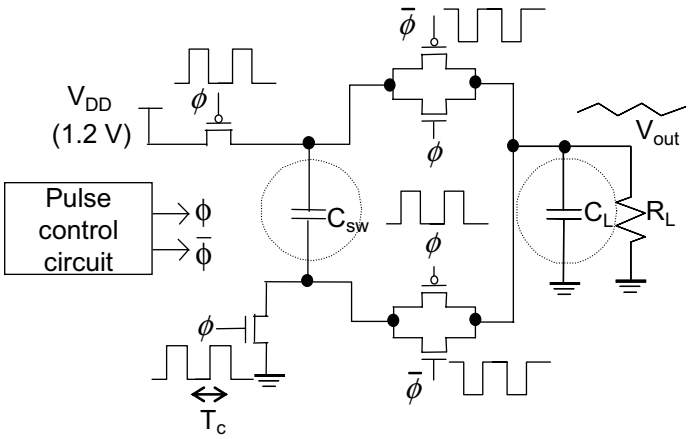


Fig. 5.69 Switched-capacitor-type converter scheme.

The features of an SC-type converter are:

1. The output voltage is determined by the circuit configuration.
2. η is high when the load is light.
3. In the steady state, the maximum source-drain voltage of each MOSFET is $V_{DD}/2$, which is half that for a buck converter.

The third feature suggests that SC-type converters are well-suited to future scaled-down device technologies, as is discussed in Section 5.4.5.

Let us consider the η of an SC-type converter.

Fig. 5.70 shows the equivalent circuit of an SC-type converter. R_{on} is the on-resistance of the output transistors (assuming that all the transistors have the same on-resistance), and d is the duty ratio for the clock ϕ. In addition, R_{SC} $(= T_c/(2C_{SW}))$ is the switching resistance, which is a loss element only for SC-type converters.

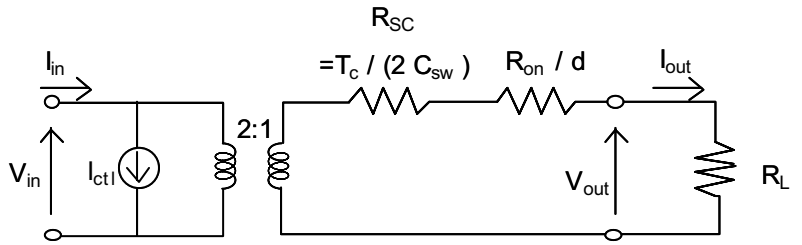


Fig. 5.70 Equivalent circuit for SC-type converter.

The average input current (I_{in}) and the average output current (I_{out}) satisfy the following equation:

$$I_{in} - I_{ctl} = \frac{I_{out}}{n}, \tag{5.46}$$

where I_{ctl} is the current dissipated by the charging and discharging of the gate plus that dissipated by the pulse control circuit, and n is the voltage conversion ratio with respect to the source (Here, we assume an n of 2.). If we assume that $C_{SW} \cdot R_L >> T_c$ (where T_c is the cycle time for ϕ and $\overline{\phi}$) and that the ripple in the output is negligible, the output voltage is given by

$$V_{out} \approx \frac{V_{in}}{n} - \left(R_{SC} + \frac{R_{on}}{d} \right) \cdot I_{out}, \tag{5.47}$$

where R_{SC} is

$$R_{SC} = \frac{T_c}{2C_{SW}}. \tag{5.48}$$

Then, the η of the converter is given by

$$\eta = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}} = \left[1 - n \cdot (R_{SC} + \frac{Ron}{d}) \cdot \frac{Iout}{Vin} \right] \cdot \frac{I_{out}}{I_{out} + n \cdot I_{ctl}}. \tag{5.49}$$

The first term of the product in (5.49) concerns the loss related to R_{SC} and R_{on}, while the second term concerns the loss related to the pulse control circuit.

This equation implies that a higher switching frequency results in a higher conversion efficiency because it reduces R_{SC}. However, in practice, a high switching frequency results in a large current dissipation due to the charging and discharging of the pulse control circuit (higher I_{ctl}). Note that we need to take into consideration the parasitic resistances due to wiring, packaging, and off-chip passive devices in an actual design, since they increase R_{on}.

Once we determine V_{in} and n, we obtain I_{in} and V_{out} as a function of I_{out} from (5.46) and (5.47), respectively. Then, we use (5.49) to calculate $P_{in}(=V_{in} \cdot I_{in})$, $P_{out}(=V_{out} \cdot I_{out})$, and η. The η for an SC-type converter was calculated using the following conditions: V_{DD} (=V_{in}) = 1.2 V, n = 2, C_{SW} = 1 μF, T_c = 1 μs, d = 0.4, and R_{on} = 0.5 Ω (the gate width is 16 mm for a pMOSFET and 4 mm for an nMOSFET made on a 0.35-μm process).

In the ideal case ($P_{ctl} \equiv V_{in} \cdot I_{ctl}$ = 0 mW), η reaches 99% at an output power (P_{out}) of 1 mW and 95% for P_{out} = 10 mW. In practice, if we consider a pulse control circuit made on a 0.35-μm process, P_{ctl} ($=V_{in} \cdot I_{ctl}$) would be in the range of 0.2-0.4 mW for a converter with an output power of 10 mW. This would yield an η of 94%.

5.4.3 Buck Converter

In a buck converter (Fig. 5.71), the input pulse applied by the pulse-width-modulation (PWM) circuit forces the output driver to generate pulses with a certain duty ratio. The pulses generated by PWM (PWMout) are filtered by a series-connected LC circuit, yielding a DC output (V_{out}).

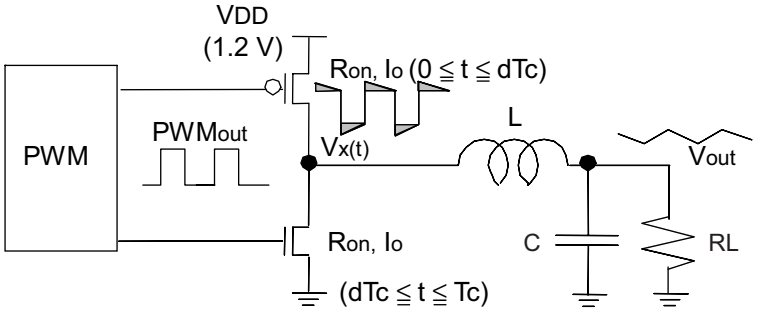


Fig. 5.71 Buck converter scheme.

The features of a buck converter are:

1. The output voltage (V_{out}) is determined by the duty ratio (d) of the PWM.
2. η is high even when P_{out} is high.
3. It is composed of a small number of elements.

Let us consider the η of a buck converter.

Let R_{on} be the on-resistance of the transistors in the final-stage buffer and I_0 be the output current. The total power loss of the converter (P_{loss}) is given by

$$P_{loss} = I_0^2 R_{on} + P_{VX} + P_{ctl}, \tag{5.50}$$

where the first term on the right side is the power loss due to R_{on} and I_o; the second term (P_{VX}) is the power loss caused by the excess voltage due to the LC filter (gray regions in Fig. 5.71); and the third term (P_{ctl}) is the sum of the power dissipated by the PWM control circuits, the inductor loss due to R_{LP}, and the leakage loss caused by the off-state leakage current (I_{leak}) of the final-stage buffer. Note that the power loss due to short-circuit current is ignored in this case, since a pulse phase shift circuit prevents on-on overlap.

We calculate I_0 in (5.50) as follows: Considering the waveforms of the output voltage of the buck converter in Fig. 5.72, the output voltage ($V_x(t)$) during a certain cycle is

$$Vx(t) = \begin{cases} V_{DD} + \Delta Vx(t) - I_0 R_{on}, 0 \le t \le dT_C \\ \\ -\Delta Vx(t) - I_0 R_{on}, dT_C \le t \le T_C \end{cases}, \tag{5.51}$$

where $\Delta Vx(t)$ is the excess output overshoot or undershoot due to LC filtering. In most cases, the pull-down nMOSFET and the charging pMOSFET have the same on-resistance; so, the overshoot waveform at a high output level and the undershoot waveform at low output level are symmetrical (Fig.5.72).

Then, V_{out} is approximately given by

$$V_{out} = \frac{1}{T_c} \int_0^{T_c} Vx(t)dt \approx d \cdot V_{DD} - I_0 R_{on}. \tag{5.52}$$

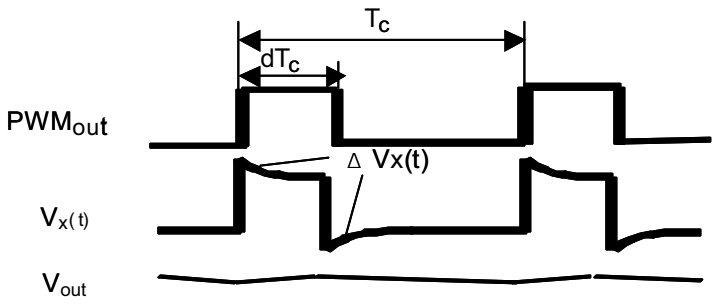


Fig. 5.72 Waveforms of buck converter at three nodes.

So, I_0 is

$$I_0 = \left(\frac{d \cdot V_{DD} - V_{out}}{R_{on}} \right). \tag{5.53}$$

Next, P_{VX} in (5.50) is given by

$$P_{VX} = \frac{V_{DD}^2}{R_{on}} \cdot f(d, \beta), \tag{5.54}$$

where

$$\begin{aligned} f(d,\beta) = \frac{1}{\beta} \Big[& \Big\{ P_1^2 + (P_1 - Q_1)^2 \Big\} \Big(1 - e^{-2d\beta} \Big) \\ & - 2Q_1 d\beta \{ 2P_1 - Q_1(1 - d\beta) \} e^{-2d\beta} \\ & + \Big\{ P_2^2 + (P_2 - Q_2)^2 \Big\} \Big(1 - e^{-2(1-d)\beta} \Big) \\ & - 2Q_1(1-d)\beta \{ 2P_2 - Q_2 - Q_2(1-d)\beta \} e^{-2(1-d)\beta} \Big]; \end{aligned} \tag{5.55}$$

d is the duty ratio of a chopped pulse; $\beta\ (\equiv T_C/T_{LC} = T_C/\sqrt{LC})$ is a constant determined by the resonance cycle time of the LC circuit and the cycle time of a chopped pulse; and P_1, P_2, Q_1, and Q_2 are written as follows:

$$P_1 = \frac{(1-d\beta)e^{-(2-d)\beta} - \{1+(1-d)\beta\}e^{-(1-d)\beta} - (1-\beta)e^{-\beta} + 1}{(1-e^{-\beta})^2},$$

$$P_2 = \frac{-(1+d\beta)e^{-d\beta} + \{1-(1-d)\beta\}e^{-(1+d)\beta} - (1-\beta)e^{-\beta} + 1}{(1-e^{-\beta})^2},$$

$$Q_1 = \frac{1-e^{-(1-d)\beta}}{1-e^{-\beta}},$$

$$Q_2 = \frac{1-e^{-d\beta}}{1-e^{-\beta}}.$$

If we assume $d = 0.5$ for simplicity, then $f(d,\beta)$ is [5.21]

$$f(0.5,\beta) = \frac{2}{\beta}\cdot\frac{1-\beta e^{-\beta/2} - e^{-\beta}}{\left(1+e^{-\beta/2}\right)^2} \approx \frac{\beta^2}{48}. \tag{5.56}$$

When β is below 0.4, (5.56) is a good approximation with an accuracy of 1%.

Then, the η of a buck converter is

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}}, \tag{5.57}$$

where P_{out} ($=V_{out}\cdot I_{out}$) is the output power.

The η was calculated from (5.50)-(5.57) under the following conditions: V_{DD} = 1.2 V, V_{out} = 0.5 V, T_c = 1 μS, R_{on} = 0.5 Ω, L = 4 μH, and C = 64 μF. In the ideal case (P_{ctl} = 0 mW), η reaches 96% at a P_{out} of 15 mW; and it is greater than 90% when P_{out} is in the range 2-50 mW. In practice, when P_{out} = 15 mW, η is 95% for P_{ctl} = 0.2 mW and 93% for P_{ctl} = 0.4 mW.

5.4.4 Applicable Zones for SC-Type and Buck Converters

Based on the discussions in Sections 5.4.2 and 5.4.3, we can plot curves of η as a function of P_{out} for both SC-type and buck converters. An examination of the curves reveals the P_{out} zones where each type of converter is applicable. This section discusses these zones.

Let us calculate η as a function of output power for both SC-type and buck converters under the constraint that the macroblocks of both converters are the same size. When we do a layout using a 0.35-μm FD-SOI process, the total gate width of an SC-type converter is empirically 1.8 times larger than that of a buck converter because the gate-source voltages of the two nMOSFETs in the SC-type converter are only 0.6 V in the steady state.

The area of the converter is determined mostly by the area of the final-stage MOSFETs, since all the passive elements (C and L) are off-chip. Thus, as long as the same block size is assumed, R_{on} for an SC-type converter should be 1.8 times larger than that for a buck converter. The calculations for Fig. 5.73 assumed that the final-stage MOSFETs had a total gate width of 10 mm; that is, R_{on} is 1.0 Ω for a buck converter and 1.8 Ω for an SC-type converter. In addition, we assumed P_{ctl} = 0.2 mW, which is the actual value for our design.

For each converter, η exhibits a peak at a particular output power. Below that output power, η decreases. This drop occurs because the loss related to the control circuits (P_{ctl}) becomes dominant in the SC-type converter and the loss related to the excess voltage due to the LC filter (P_{vx}) becomes dominant in the buck converter. Above that output power, η also decreases because the loss related to resistance, such as R_{on}, becomes dominant in both converters. Since the output resistance of the SC-type converter is the sum of R_{sc} and R_{on}, while that of the buck converter is only R_{on}, the η of the SC-type converter decays more rapidly.

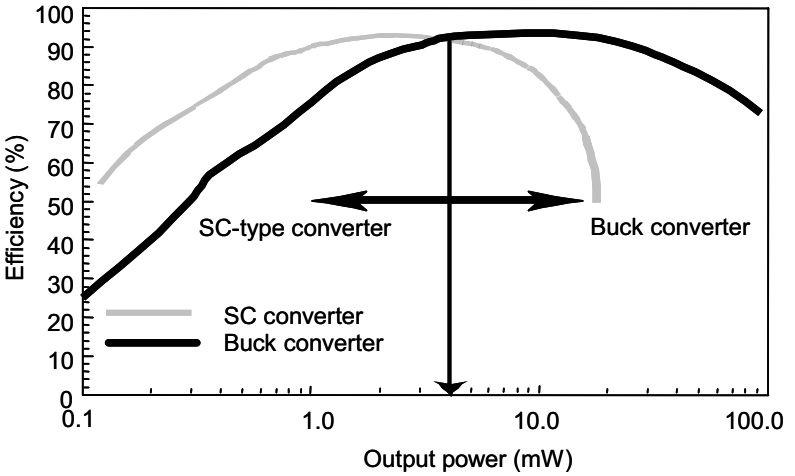


Fig. 5.73 Calculated conversion efficiency vs. Pout for SC-type and buck converters.

An SC-type converter exhibits a high η of more than 90% when P_{out} is as low as 1-4 mW, while a buck converter exhibits a high η when Pout is greater than 5 mW. This means that an SC-type converter is more suitable when P_{out} is in the range of a few milliwatts, while a buck converter is more suitable when P_{out} is a few tens of milliwatts.

To confirm the results of the calculations, SC-type and buck converters were fabricated on a 0.35-μm FD-SOI CMOS process.

The SC-type converter is composed of switching MOSFETs and a pulse control circuit consisting of drivers, a 1-MHz oscillator, and a comparator. The comparator compares V_{out} with the reference voltage; and if V_{out} is greater, the comparator disables the oscillator. The chip is 1 mm × 1.5 mm in size. The final stage has a total gate width of 18 mm, and consists of an 8-mm pMOSFET, two 4-mm nMOSFETs, and a 2-mm nMOSFET. The C_{SW} and C_L used for the measurement were 0.33 μF and 3.3 μF, respectively.

The buck converter employs PWM control to produce a variable V_{out}. The oscillation frequency is 1 MHz, and the chip is 0.9 mm × 2.0 mm in size. The final stage consists of an 8-mm pMOSFET and a 2-mm nMOSFET. The

off-chip elements used for the measurements were an L of 15 μH and a C of 55 μF.

The measurement results (Fig. 5.74) show that both converters have a high η of more than 85%. They also show that the η of the buck converter is higher than that of the SC-type converter when Pout exceeds 4 mW; and the reverse is true when Pout is below 4 mW. So, η exhibits the same type of behavior as shown in the calculation results. The measured η for the buck converter is almost the same as the calculated one. Although the fabricated SC-type converter has a larger final driver than that assumed in the calculations, it has a slightly lower η. This is caused by parasitic capacitances and resistances, wire-bonding, and so on. From the measurements, we can also see the applicable zones for the two converters, which should be taken into account when designing circuits with high-efficiency on-chip converters.

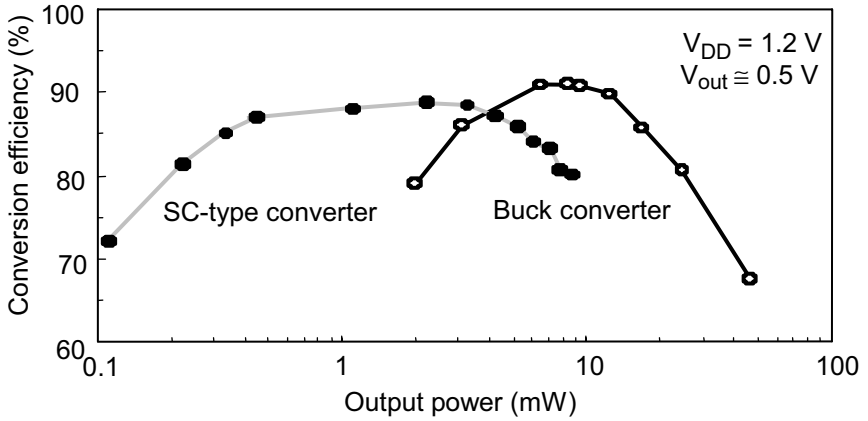


Fig. 5.74 Measured conversion efficiency of SC-type and buck converters.

5.4.5 On-Chip Distributed Power Supplies for Ultralow-Power LSIs

With the continued scaling-down of semiconductor devices, chip power dissipation will be reduced more and more; and ultralow-power LSIs with a power dissipation of a few milliwatts will be used in wireless systems. These LSIs will require an on-chip power supply. This section describes fully-on-chip power supplies for 0.5-V LSIs .

There are two basic types of fully-on-chip power supply systems: single and distributed (Fig. 5.75). A single power supply system (SPSS) employs one on-chip power unit to supply power to all the macroblocks on a chip (Fig.5.75 (left)). This configuration is well suited to a simple LSI containing only one kind of macroblock (e.g. It contains small logic circuits and simple memory.). However, it is not the best solution for system LSIs, such as the one in Fig. 3.3, which contains several large-scale logic block, analog blocks, and memories. The IR drop through the power bus lines cannot be ignored and will become a problem because the drop degrades the switching speed of the 0.5-V logic blocks. Another problem with SPSS is that the supply voltage must be set to that of the macroblock with the highest V_{DD}, such as an analog block or a memory, which usually require a high voltage.

In contrast, a distributed power supply system (DPSS) (Fig. 5.75 (right)) makes it possible to suppress the IR drop and adjust the supply voltage for each unit. Thus, DPSS is much better suited to ultralow-voltage LSIs. In addition, it is easier to implement DPSS with FD-SOI than with bulk technology, since

1. FD-SOI devices are latch-up free, even when multiple power supplies are used;
2. the pass gates of an SC-type converter made with FD-SOI devices have a larger drivability than those made with bulk ones; and
3. better isolation can be achieved by using a high-resistivity substrate.

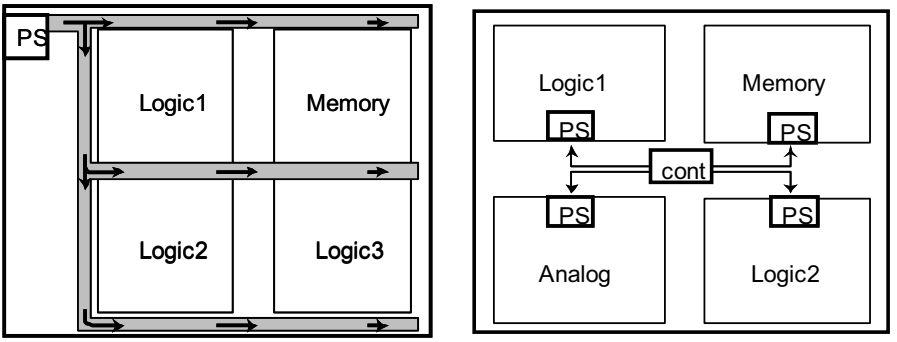


Fig. 5.75 Single (left) and distributed (right) power supply systems.

A. Fully-on-chip power supply system based on SC-type converter

This section further describes a DPSS for ultralow-power LSIs. If we specify that the power supply system must be fully on chip, a buck converter is very difficult to implement because it requires an inductance on the order of micro henries, which is three orders of magnitude larger than that of current integrated inductors. An SC-type converter does not have this drawback because capacitors are easy to fabricate on a chip. Below, a fully-on-chip SC-type converter is described as an example of a DPSS.

The η of a fully-on-chip SC-type converter can be calculated from the measurement results for 0.35-μm FD-SOI devices presented in previous sections. Assuming an advanced circuit design based on scaling, P_{ctl} could be as low as 0.06 mW; and we assume the ratio of C_L to C_{SW} to be 3.0, which is still effective in suppressing the degradation in the ripple characteristics. The calculations were made for switching frequencies (f_{SW}) of 4 MHz and 8 MHz. For fully-on-chip integration, the capacitances are three orders of magnitude smaller than those for discrete components; thus, we need to use a higher switching frequency to reduce the R_{SW} of the converter.

Fig. 5.76 shows the relationship between C_{SW} and P_{out}, assuming an η of 80%. When P_{out} is over 1 mW, the voltage drop caused by R_{SW} is very large, which degrades η. Thus, a high C_{SW} is necessary to keep η high. When P_{out} is below 0.4 mW, P_{ctl} is large, which degrades η. Thus, below a certain value of P_{out} (0.2 mW at f_{SW} = 4 MHz, 0.3 mW at f_{SW} = 8 MHz), it is impossible to obtain an η of 80%.

We find that C_{SW} must be at least 1.5 nF at a P_{out} of 1 mW. Thus, the total capacitance must be 6 nF (a C_L of 4.5 nF plus a C_{SW} of 1.5 nF to make the ratio 3) to obtain a P_{out} of 1 mW for an η of 80% when the switching frequency is 8 MHz. If we employ a 0.25-μm FD-SOI process, for which a 6-nF capacitor has an area of 0.6 mm^2, then a fully-on-chip SC converter will be around 0.8 mm^2 in size, since the circuit occupies an area of 0.2 mm^2. To obtain a P_{out} of 2.5 mW, the total capacitance (C_{SW} + C_L) must be at least 16 nF, as estimated from Fig. 5.76. This yields a converter size of around 1.8 mm^2, which is 5-8% of the area of a macroblock (5 mm x 5 mm) on a chip.

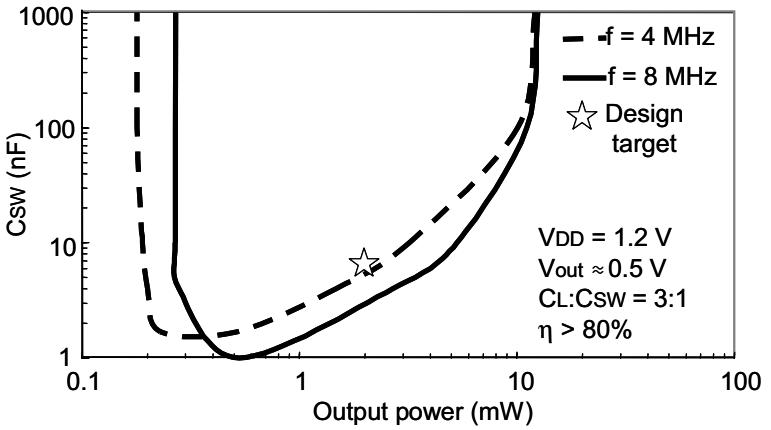


Fig. 5.76 Dependence of capacitance on output power for SC-type converter with 0.5-V output.

A fully-on-chip 2:1 SC-type converter unit was designed and fabricated on a 0.25-μm FD-SOI process. The target η was over 80% for a P_{out} of 2 mW and an f_{SW} of 4 MHz; this point is the star in Fig.5.76. The chip contains two 7-nF on-chip capacitors and switching MOSFETs in a 1 mm × 2 mm area. Without control circuits, η is 82% when P_{out} = 2 mW at a V_{out} of 0.5 V and a V_{DD} of 1.2 V. The output ripple is as small as 43 mV_{pp}; this should become smaller when the C_L for the loading macroblocks and decoupling capacitors in an actual application is added.

B. Prospects for scaled-down on-chip SC-type converters

As process technology evolves, the scaling-down of devices will certainly improve the performance of on-chip converters; and an important factor in predicting performance is the layout area for each generation. A converter unit is composed of 3 blocks: on-chip capacitors; final-stage driver MOSFETs; and a pulse control circuit, including driving circuits. In order to estimate the area of each block for the 0.15-μm, 0.25-μm, and 0.35-μm technology generations, we assume the following:

1. For a 0.25-μm process, a capacitor will occupy an area of 1 mm^2, which means that the on-chip capacitance is 16 nF (a C_{SW} of 4 nF and a C_L of 12 nF). Note that this yields an η of 80% for an f_{SW} of 4 MHz and a P_{out} of 2.5 mW.

2. The area occupied by the pulse-control circuit can be estimated from that for a buck converter made on a 0.35-µm FD-SOI process [5.22].

The area of an on-chip SC-type converter for each generation was normalized by that for a 0.35-µm process (Fig. 5.77). The areas for the driver and control circuit decrease with the square of the scaling factor. On the other hand, the area of a capacitor depends on the thickness of the gate oxide; and for a 0.15-µm process, it is 1/3 that for a 0.35-µm process. Since the capacitor occupies the most area and is the main factor determining the size, the area for a 0.15-µm process is around 1/3 that for a 0.35-µm process.

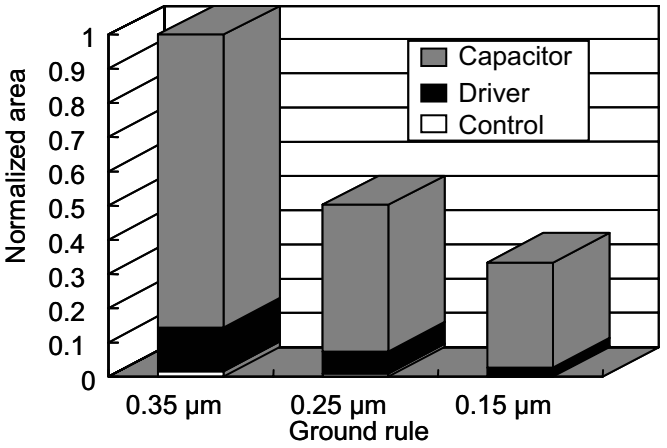


Fig. 5.77 Estimated area of macroblock for SC-type converter for three technology generations.

To estimate the η of an on-chip SC-type converter for a 0.15-µm process, we first calculate R_{SC} and R_{on} for a 0.25-µm process using (5.48) and the previous experimental results. The values in Table 5.4 were obtained under the following measurement conditions: V_{in} = 1.2 V, V_{out} = 0.5 V, C_{SW} = 7 nF, T_c = 250 ns, and d = 0.4.

For these conditions, the measured η_{sc} of the SC-type converter without control circuits is 82.0%. Assuming that the area of a macroblock is the same for the two processes, R_{SC} is 38% smaller for the 0.15-µm process due to the larger C_{SW}; and R_{on} is 40% smaller due to scaling. So, if we do not take P_{ctl}

into account, η is 89% when I_{out} = 4 mA and 94.5% when I_{out} = 2 mA (see Table 5.4). If we further assume an advanced circuit design with a P_{ctl} of 0.06 mW, then we obtain an η of about 87% when I_{out} = 4 mA and 90% when I_{out} = 2 mA.

Thus, device scaling should enable us to make high-efficiency fully-on-chip SC-type converters with an η of almost 90%. This is indispensable for ultralow-voltage LSIs in the near future; and an intelligent power supply system such as DPSS will be employed for ultralow-power FD-SOI LSIs.

Table 5.4 Efficiency of on-chip SC-type converters.

Ground Rule	R_{SC} (Ω)	R_{ON} (Ω)	I_{OUT} (mA)	η_{SC} (%)	η (%)
0.25 μm	17.86	3.656	4	82.0	-
0.15 μm	11.07	2.194	4	89.0	86.8
			2	94.5	90.0

5.5 I/O and ESD-Protection Circuitry for Ultralow-Power LSIs

I/O circuit design for ultralow-power is very important since the conversion gain to a conventional 3.3 V CMOS interface is very large; and there are design challenges in providing electrostatic-discharge (ESD) protection for FD-SOI devices.

5.5.1 Standard Interface Trends

One advantage of CMOS FD-SOI technology is the large power savings from the use of a low supply voltage. When the power supply for internal circuits is reduced to 0.5 V, the connection to external devices and equipment requires a special I/O circuit design to handle the large difference in operating voltages. Although the operating voltage of LSI circuits continues to decrease as CMOS transistors are scaled down [5.23], the reduction in the interface voltage lags far behind this trend, with the operating voltage of the Universal Serial Bus (USB) and other standard interfaces remaining at 3.3 V (Fig. 5.78). The difference between internal operating voltage and interface voltage will not fall below 2 V over the next ten years.

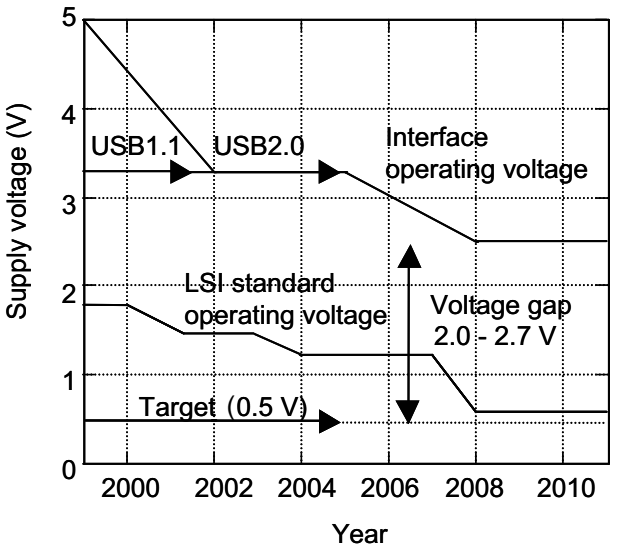


Fig. 5.78 Trend in operating-voltage gap for interface circuits.

5.5.2 Problems with I/O Circuits for 0.5-V/3.3-V Conversion

The problems with conventional I/O circuits when converting between 0.5 V and 3.3 V, assuming full-rate USB operation (12 Mb/s or more), are illustrated in Fig. 5.79. The output circuit (a) amplifies a 0.5-V input signal to an amplitude of 3.3 V; and the input circuit (b) reduces a 3.3-V signal to an amplitude of 0.5 V. Circuits that convert signal levels differing by over 2 V are needed so that low-voltage SOI devices can interface with standard peripherals. However, there are a couple of problems with conventional circuits:

1. The source/drain, source/gate, and gate/drain voltages of some of the transistors in the circuits are larger than the breakdown voltage (2 V) of FD-SOI devices [5.24] [5.25].
2. When conventional output circuits drive the final-stage nMOS transistors with a 0.5-V input signal, the available drive current is not large enough to drive the output load at the USB rate.
3. Furthermore, the pMOS transistors are not turned off and consume power due to the leakage current.

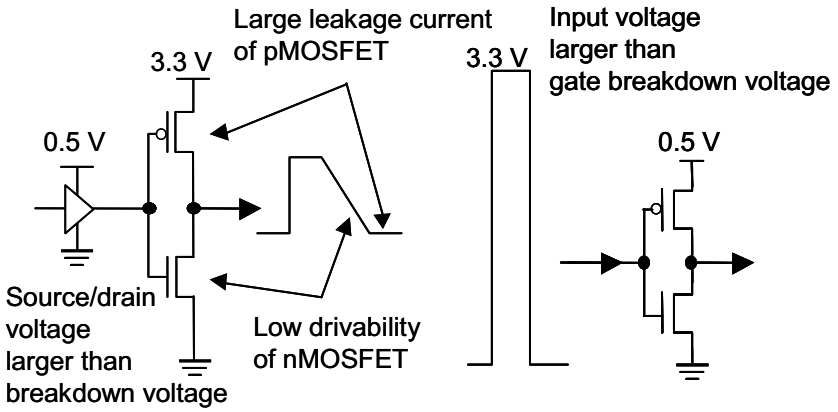


Fig. 5.79 Drawbacks of conventional interface circuits: (a) Output circuit converting internal 0.5 V to external 3.3 V (b) Input circuit converting external 3.3 V to internal 0.5 V.

One solution to the 2nd and 3rd problems is to supply a voltage of 3.3 V to the transistor gates; but this simple modification gives rise to the 1st problem.

5.5.3 Guidelines for Design of Interface Circuits

A. Output circuit

A cascode circuit is useful for reducing the voltage applied to transistors. A cascode output stage (Fig. 5.80) can be made with two pMOS and two nMOS transistors. Proper selection of the gate voltages makes it possible to set the source/drain and gate/source voltages of all the transistors to less than the breakdown voltage (V_B) for a supply voltage of 3.3 V when either (a) 0 V or (b) 3.3 V is output. The gate voltage of the pMOSFET connected to the output pin is set to a voltage greater than V_B and less than 3.3 V – V_B. To put the pMOSFET connected to the 3.3 V power supply in the OFF state, a swing signal between 3.3 V and V_{AP1} is fed to the gate.

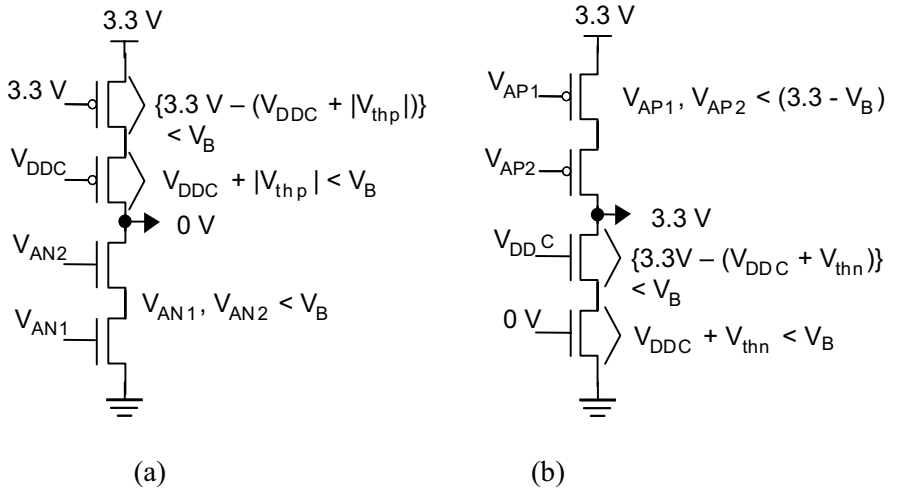


Fig. 5.80 Output stage structures and gate voltages that keep the voltages applied to the transistors less than the breakdown voltage (V_B) for an output voltage of (a) 0 V and (b) 3.3 V.

Next, to increase the operating speed, the drivability of the p- and nMOSFETs are equalized. The I-V characteristics of a grounded nMOSFET and a pMOSFET connected to a 3.3 V power supply are compared in Fig. 5.81. The

nMOSFET runs on an internal voltage of V_{DD}, and the pMOSFET runs on 3.3 V – V_{DD} (V_{AP1}). Based on the balance or imbalance between the drivabilities of the p- and nMOSFET, we can divide the supply voltage (V_{DD}) into three regions.

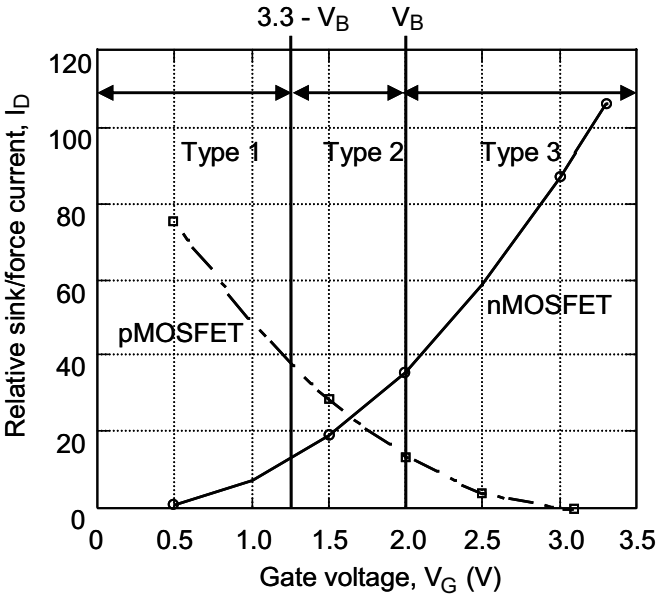


Fig. 5.81 Relative sink/force current vs. gate voltage for output transistors.

Each region has a different optimum circuit structure (Fig. 5.82):

Type 1: $V_{DD} \leq 3.3\ V - V_B$
This necessitates a configuration that pulls the drive voltage of the nMOSFET up to V_B.

Type 2: $3.3\ V - V_B < V_{DD} < V_B$ [5.23]
This allows a configuration that clamps the drive voltage of the nMOSFET and pMOSFET at a fixed value (V_{DDC}).

Type 3: $V_{DD} \geq V_B$ [5.23]
This necessitates a configuration that pulls the drive voltage of the pMOSFET down.

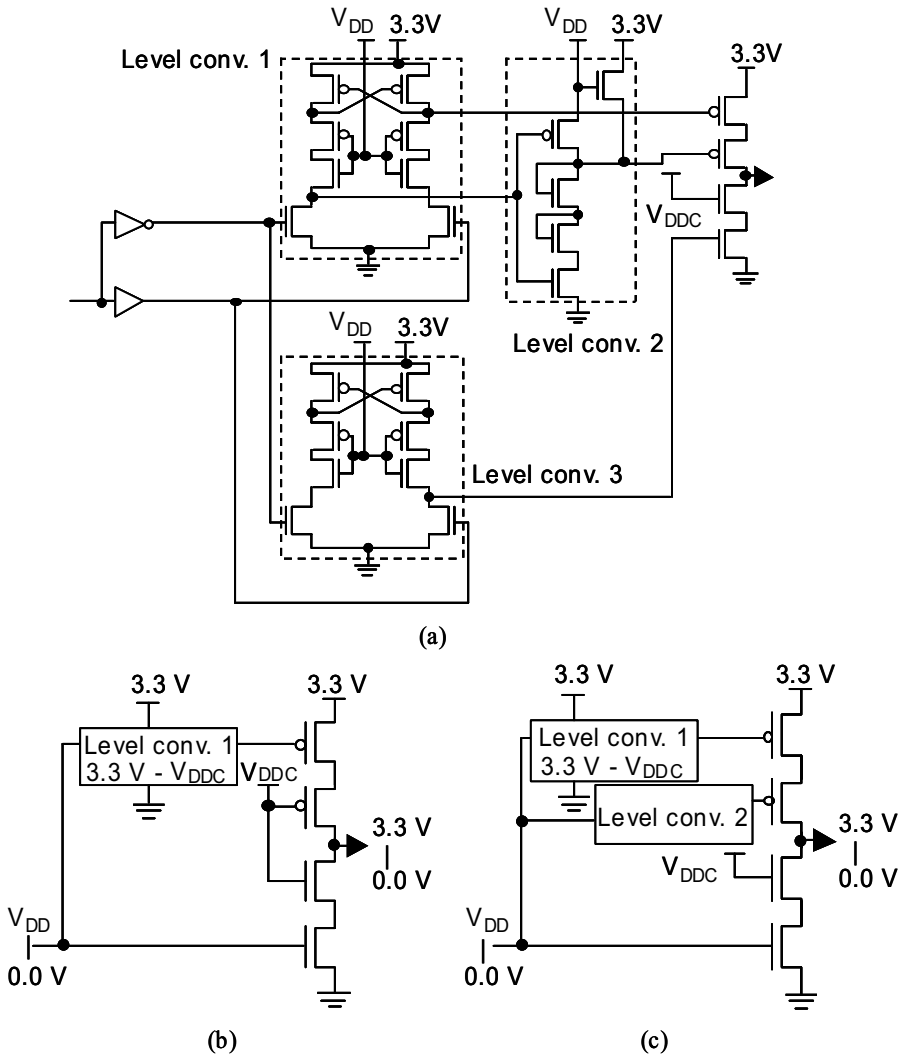


Fig. 5.82 Output circuit structures providing high drivability when the voltage applied to the transistors is lower than the breakdown voltage (V_B): (a) Type1: $V_{DD} \leq 3.3\ V - V_B$, (b) Type 2: $3.3\ V - V_B < V_{DD} < V_B$, (c) Type 3: $V_{DD} \geq V_B$.

If we employ SOI devices that follow the trend in Fig. 5.78, Type 1 should be selected because the supply voltage (V_{DD} = 0.5 V) is less than 3.3 V – V_B.

B. Input circuit

Two types of input circuits have been devised for 0.5-V/3.3-V conversion: the feedback type (Fig. 5.83 (a)) and the pMOS cascode type (Fig. 5.83 (b)). The feedback type has two-stage clamping nMOSFETs attached to the input pin. When a voltage of V_{DDC} is applied to the gates of these nMOSFETs, the high-level input (3.3 V) to the inverter is reduced to $V_{DDC} - V_{thn}$, where V_{thn} is the threshold voltage of an nMOSFET. V_{DDC} is selected so that the voltage applied to the clamping nMOSFETs and the inverter gate does not exceed the gate/source voltage.

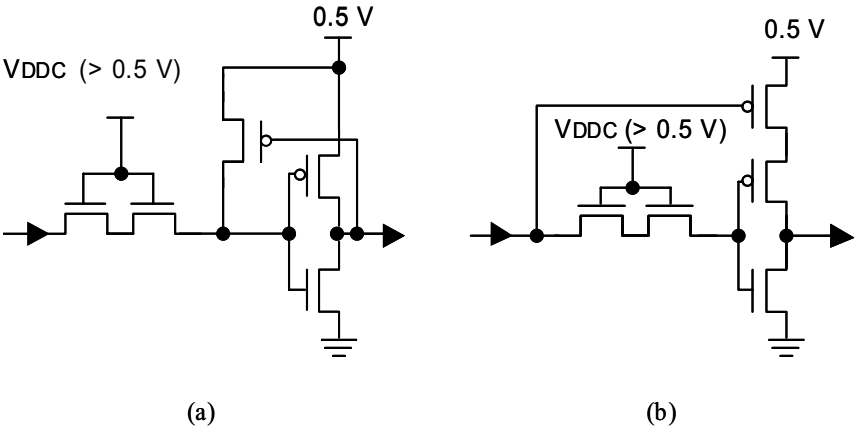


Fig. 5.83 Input buffer circuits: (a) feedback type (b) pMOS cascode type.

The pMOS cascode type, on the other hand, can be used when the supply voltage is greater than 3.3 V – V_B. With a 0.5-V supply, however, this type is difficult to use for two reasons: The voltage applied to the gate of the pMOSFET connected to the power supply exceeds the limit on the gate/source voltage for 3.3 V input; and the drivability of cascode two-stage pMOSFETs is extremely low.

5.5.4 Performance of I/O Circuits

A. Output circuit

Two designs for an output circuit that converts 0.5 V to 3.3 V (Fig. 5.82(a)) were evaluated: one that uses Type 2 and one that fixes the gate voltage at V_{DD}. Simulations showed that the voltages applied to the gate, source, and drain of the transistors were less than the breakdown voltage (V_B = 2 V). The circuits were fabricated on a 0.35-μm CMOS/SOI process. The output waveforms (Fig. 5.84) show that both types of circuits convert the voltage level from 0.5 V to 3.3 V.

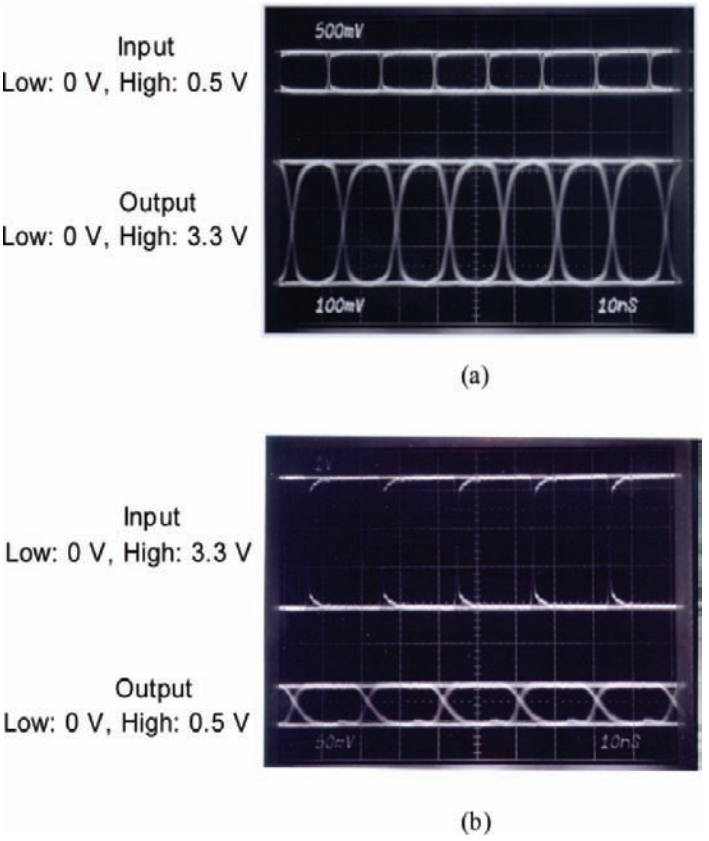


Fig. 5.84 Measured I/O waveforms: (a) 70-Mb/s eye pattern for output buffer (b) 50-Mb/s eye pattern for input buffer.

The speed was estimated with an output signal duty ratio of the output circuit of 50% ±10% as the operating criterion. Type 2 operates at up to 70 MHz, while the type using a fixed V_{DDC} operates at up to 40 MHz. This difference in speed stems from the sensitivity of the output signal duty ratio to V_{DDC} . Both types provide an adequate speed margin for the full-rate USB specification of 12 Mb/s.

B. Input circuit
Two designs for an input circuit (Fig. 5.83(a)) that converts 3.3 V to 0.5 V were tested: Type 1, which employs a feedback circuit, and Type 2, which does not. Just as for the output circuit, simulations showed that the voltages applied to all the transistors did not exceed the breakdown voltage. Although it was necessary to adjust the clamping voltage (V_{DDC}), both types converted signals from 3.3 V to 0.5. For an output duty ratio of 50% ±10%, operation at speeds of up to 50 MHz is possible, as shown in Fig. 5.5.7, which provides an adequate speed margin for the full-rate USB specification.

In conclusion, considering the connection between SOI circuits operating at an extremely low voltage (0.5 V) and standard interfaces, an interface circuit that can handle a level difference of over 2 V will become necessary in the next ten years. Since SOI devices have the disadvantage of a low breakdown voltage, input and output circuits that reduce the voltage applied to transistors have been designed. The design target is to achieve the USB operating speed with an output duty ratio of 50% ±10%. For the output circuit, a cascode connection for the output stage transistors was used as a base. The gate voltages of the transistors were selected based on the relationship between operating voltage and breakdown voltage. This method offers a variety of optimum output circuits that provide high drivability, without exceeding the maximum allowable voltage applied to the transistors. For the input circuit, a feedback-type circuit that employs clamping transistors is used for the same purpose. The result of these designs is the achievement of speeds that exceed the full-rate USB specification of 12 Mb/s for both output circuits that convert 0.5 V to 3.3 V and input circuits that convert 3.3 V to 0.5 V.

5.5.5 ESD Protection with FD-SOI Devices

The physical cause of circuit failure due to electrostatic discharge (ESD) is thermal breakdown associated with excessive current. For SOI devices, a thick oxide film surrounds the thin Si active layer, which makes the heat dissipation much poorer than for bulk devices. An nMOS protection device provides only

about one-half the ESD protection of a bulk device of the same size [5.24]. A bulk MOS transistor also contains a diode between the substrate and the source and drain as a parasitic device, while an SOI device has a buried-oxide film for insulation, eliminating the possibility of a vertical parasitic diode that could be beneficial under forward stress [5.25]. An FD-SOI nMOS device, on the other hand, exhibits parasitic bipolar action that results in a lower snap-back trigger voltage (V_{T1}) than for bulk devices. This makes it easier to obtain uniform snap-back operation, which is an important characteristic of multifinger layouts.

Figure 5.85 shows the typical snap-back characteristics of FD-SOI nMOSFETs with CVD tungsten covering the source and drain regions. These results were obtained by transmission line pulse (TLP) measurements, in which a charged coaxial cable discharges into the target device.

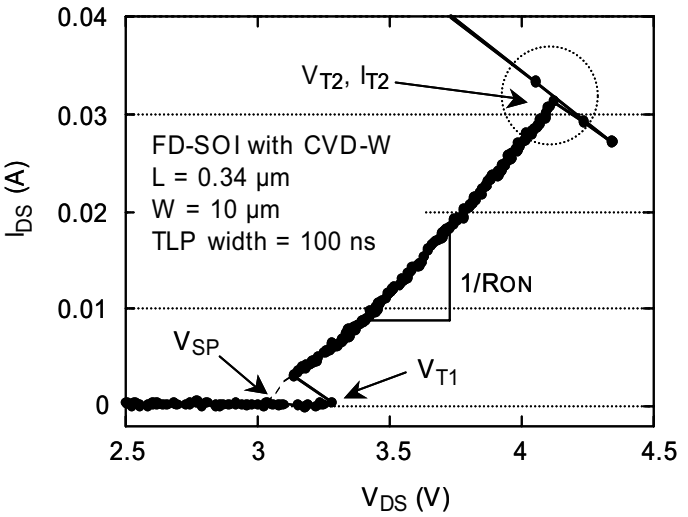


Fig. 5.85 Snap-back characteristics of FD-SOI nMOSFET obtained by transmission line pulse measurements.

An FD-SOI nMOSFET has a much lower V_{T1} (< 3.5 V) than ordinary 0.5-μm bulk devices (8-12 V). Even if the amount of protection provided by a unit-size protection device is small, the ESD protection level can be boosted by increasing the number of fingers because a low V_{T1} helps all the fingers

turn on at the same time. A means of achieving a uniform flow of ESD current in protection devices is of prime importance for FD-SOI devices. Some layout and circuit techniques for ESD protection are described below.

5.5.6 Design and Layout Requirements for ESD Protection

There are two approaches to building an ESD protection-circuit network for low-voltage FD-SOI devices: layout-oriented and circuit-oriented.

A. Layout-oriented approach

An FD-SOI MOSFET does not have a parasitic diode that can handle forward stress (e.g., a negative-voltage surge with respect to the ground) like bulk devices do. One solution is to connect lateral diodes in parallel with a multifinger MOSFET to produce a merged-diode layout (Fig. 5.86).

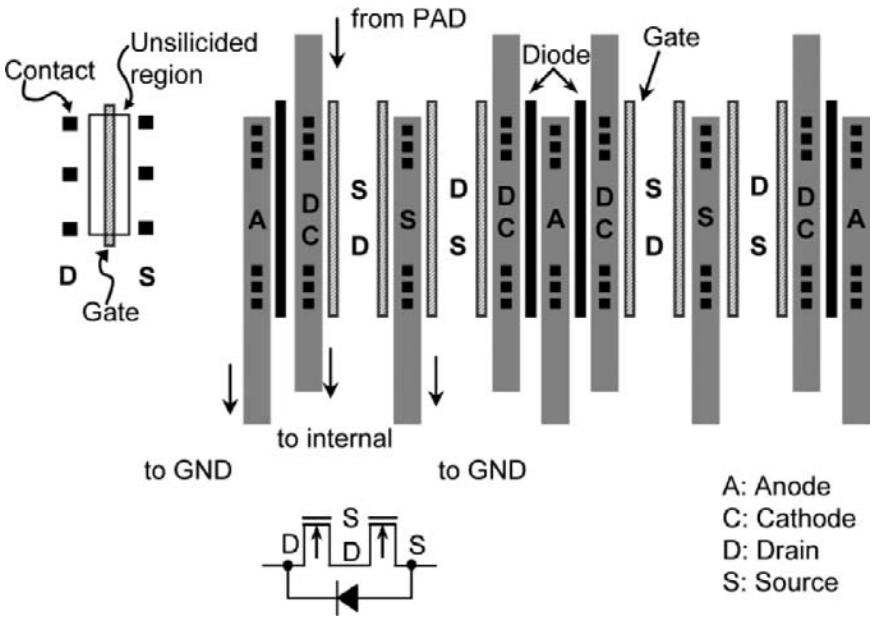


Fig. 5.86 Merged-diode layout for ESD protection circuit.

Salicide control technology (Fig. 5.86 (left)), which blocks the formation of silicide in the gate region of a protection device, is commonly used to improve ESD protection in both SOI and bulk devices. Salicide control increases the on-resistance during bipolar operation, which helps all the fingers turn on at exactly the same time, thereby preventing the localization of ESD current in one finger. The width of the unsilicided region is an important parameter, as is the distance between the contact and the gate. Since the trigger voltage (V_{T1}) for FD-SOI snap-back operation is a low 3-4 V, the effect of ballast resistance is large, even for a narrow unsilicided region. Even a device that is completely covered with silicide (that is, made without control processing) exhibits a high degree of protection if the threshold voltage is low [5.26].

A short gate length (L) in a protection transistor is desirable from the standpoint of efficient turn-on during an ESD event; but since the gate width (W) is large (> 500 μm), off-state leakage can be a problem. In an FD-SOI device, L is preferably 0.25-0.35 μm for a variety of reasons, including threshold-voltage considerations. At the same time, the second breakdown current (I_{T2}) of an FD-SOI nMOSFET is about 2-4 mA/μm (Fig. 5. 85). This requires a gate width of 250-750 μm to provide an ESD protection level of 2000 V in the Human Body Model (HBM) because the maximum current flowing into a pin is about 1-1.5 A. To provide protection against a voltage of 5000 V, the protection of unit devices themselves needs to be improved and new circuit-oriented techniques need to be developed.

B. Circuit-oriented approach

In a submicron FD-SOI transistor, the source/drain breakdown voltage is usually less than 3 V due to parasitic bipolar effects. In addition, the breakdown voltage of the gate-oxide film is too small to handle a supply voltage of 3.3 V when the oxide film is as thin as about 5 nm. This is also a problem for bulk devices with a feature size of 0.18 μm or less, and finding a way of enabling fine devices to handle a large supply voltage has become an issue of concern. One commonly used method is to connect MOS devices in a cascode fashion. ESD protection is provided by a two-stage cascode configuration. In practice, this is no different from a conventional single-stage configuration; but care must be taken when increasing the number of stages because the voltage drop required for protection likewise increases. Simulations based on the HBM show that this method enables devices with a 5-nm-thick gate-oxide film to withstand a pulse-voltage stress of about 8-9 V [5.27].

Power-supply pins also require electrostatic-discharge protection circuits, just as do other I/O pins. This involves using power lines as surge paths, which means that a protection circuit between power lines can serve as a second line of defense for I/O circuits. Forcing a surge to flow through a protection circuit between power lines makes it possible to obtain an effect commensurate with the increase in the size of the protection device. For example, the use of lateral diodes described in Section 5.5.6 not only increases protection against forward stress, but also provides an alternate surge circuit, as shown in Fig. 5.87 (the broken lines with arrows indicate the surge paths for a positive ESD voltage with respect to the ground).

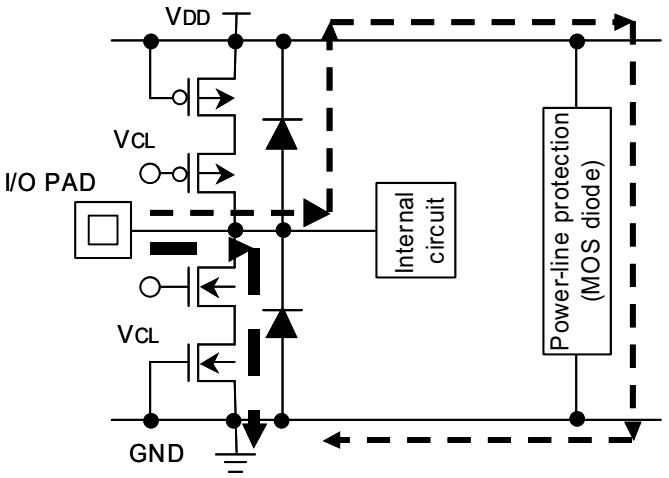


Fig. 5.87 Cascode ESD protection circuit for LVTTL I/O.

Bulk devices and partially-depleted (PD) SOI devices can employ both parasitic devices with the well or substrate as an element and also body-bias effects for ESD protection. In contrast, FD-SOI devices, in which the body floats and is fully depleted, cannot readily employ the substrate for ESD protection. On the other hand, parasitic bipolar action results in an extremely small trigger voltage, which makes it relatively easy to achieve uniform turn-on. Given a layout and circuit design that fully exploits these characteristics, FD-SOI devices can achieve a level of ESD protection equivalent to that of bulk ones, while also providing better protection for next-generation high-speed I/O circuits because of their small parasitic capacitance.

5.6 Summary

This chapter concerns analog/RF circuits, and first discussed RF building blocks. Next, cyclic and noise-shaping A/D converters and a current-steering D/A converter were presented. Finally, DC-DC converters for a power supply between 0.5 V and 1 V, and 0.5-V I/O circuits with ESD protection were described. All these circuits are fabricated on an FD-SOI CMOS process and operate at a low voltage of 1 V or less.

These analog/RF building blocks enable the development of very low-power ubiquitous wireless systems, in which the major LSIs run on a power supply of 0.5-1 V and interface with 3.3-V peripheral circuits.

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Chapter 6

SPICE MODEL FOR SOI MOSFETs

6.1 Introduction

For accurate circuit simulations, the SOI SPICE model must take floating-body and self-heating effects into account, even for FD-SOI MOSFETs. These effects are incorporated in the latest SOI models [6.1],[6.2] and are reflected in circuit simulations. This chapter describes the configuration of the SPICE model for SOI MOSFETs, explains the method of parameter extraction for the model, and describes the influence of the parameters on circuit behavior.

6.2 SPICE Model for SOI MOSFETs

Circuit simulations in the field of SOI MOSFETs require an accurate SPICE model that describes the special characteristics of these devices. Generally, a device is modeled in SPICE using an equivalent circuit consisting of passive elements, active elements, and current sources. A cross section of an SOI MOSFET and the corresponding equivalent circuit are shown in Fig. 6.1.

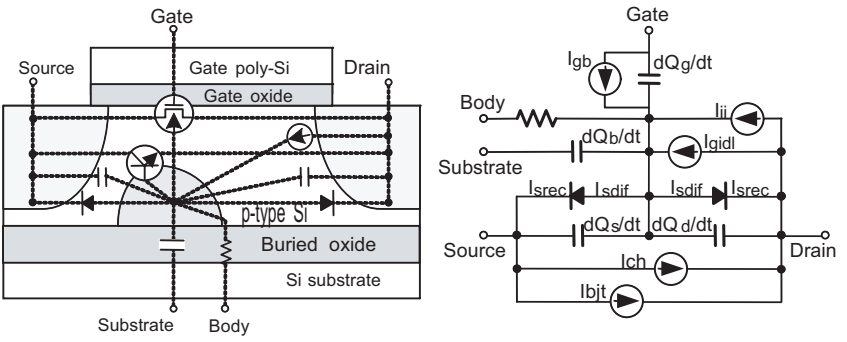

Fig. 6.1 (a) Cross section of SOI nMOSFET and (b) equivalent circuit used as SPICE model.

Since an SOI MOSFET is completely separated from the substrate by a buried-oxide layer, it has five terminals: source, drain, gate, body, and substrate. The body connects the source and drain through a p-n junction diode, and it also capacitively couples the gate and substrate. In a floating-body device, the body potential is determined by the charge created by the capacitive coupling between the various electrodes and the body, and the various currents within the body.

The physical model includes six currents:

- the drift-diffusion current (I_{ch});
- the impact ionization current (I_{ii});
- the gate-induced drain leakage current (I_{gidl});
- the gate tunneling current (I_{gb});
- the body-source and body-drain p-n junction diode current (I_{sdif}, I_{srec}); and
- the current (I_{bjt}) that flows in the parasitic bipolar transistor formed by the source, body and drain.

This yields the model in Fig. 6.1(b) [6.3].

As discussed in Section 2.2.2, there are two types of SOI MOSFETs: fully-depleted (FD) and partially-depleted (PD). The only difference between them is that an FD device has a smaller body-source built-in potential, and therefore a smaller potential barrier height than a PD device. The BSIMSOI MOSFET SPICE model [6.2] incorporates the concept of body-source built-in potential lowering to unify the PD and FD models [6.4]. This model makes it unnecessary to have two sets of parameters for the two types of devices. This chapter describes how the model parameters for BSIMSOI are extracted.

6.3 Parameter Extraction

In the parameter extraction procedure (Fig. 6.2) for the SOI SPICE model [6.5], the parameters of each element of the equivalent circuit (Fig. 6.1(b)) are extracted from the measured electrical characteristics of SOI MOSFETs. These parameters are then used for circuit-level verification. This section explains the important points in each step of the extraction procedure and how the parameters affect circuit performance.

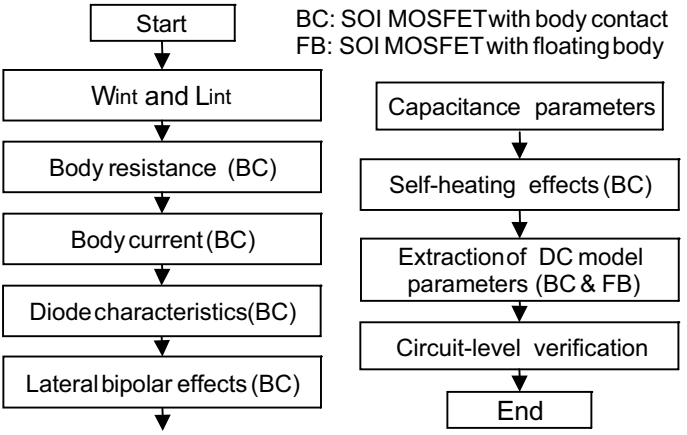

Fig. 6.2 Parameter extraction procedure for SPICE model of SOI MOSFET.

(1) Test structures for parameter extraction

Typical layouts of SOI MOSFETs [6.6] used for parameter extraction are shown in a Fig. 6.3. There are two types of MOSFETs: floating-body and body-contact. In the latter, the body is connected to either the ground or the supply-voltage line. In order to extract parameters for a floating-body device, those for a body-contact device must also be extracted using both an H-shaped and a T-shaped gate. An SOI MOSFET with a body contact is used to measure the parasitic bipolar characteristics, the characteristics of the p-n junction diode between the body and source, and the body current created by impact ionization when the body is grounded. It is also used to extract the basic MOSFET parameters. To determine the circuit delay for floating-body SOI MOSFETs, which is used to model floating-body effects, a delay circuit consisting of an SOI MOSFET with a body contact is needed for comparison.

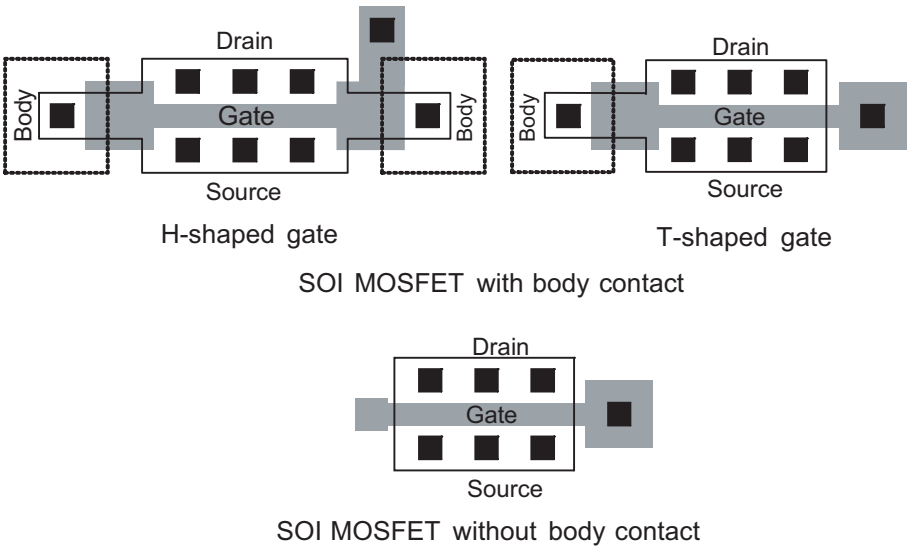

Fig. 6.3 Layouts of SOI MOSFETs used for parameter extraction.

(2) Extraction of gate length and gate width

The physical length (L) and width (W) of the channel must be extracted for SOI MOSFETs in the same way as for bulk MOSFETs. Various ways of doing that have been reported [6.7]-[6.9], but basically they are extracted by examining how the electrical characteristics depend on size. Since L and W

depend on the shape of the gate, two test structures with differently shaped gates are used (Fig. 6.3); and they are fabricated in various sizes.

(3) Body resistance

As the SOI layer becomes thinner, the body resistance increases and becomes distributed over a wider area as the channel width increases [6.10]. So, the body resistance must be extracted for an accurate simulation.

The body resistance is determined by the four-terminal method using a MOSFET with an H-shaped gate (Fig. 6.3), which has a terminal at each end. The body-resistance parameters RBODY and RBSH are extracted from the measured current-voltage characteristics (Fig. 6.4).

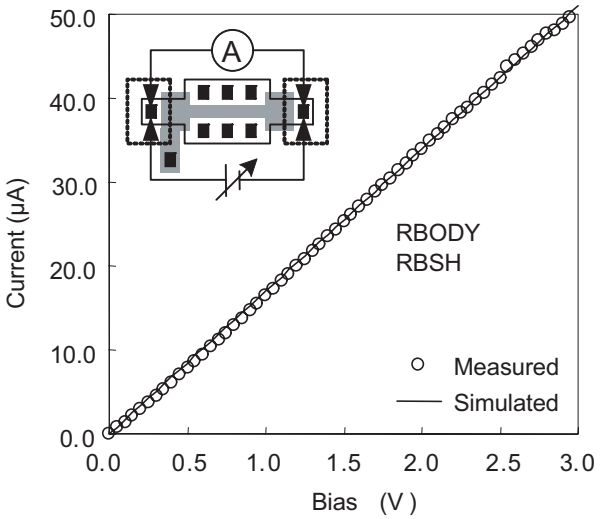

Fig. 6.4 Current-voltage characteristics used to extract the body resistance.

(4) Body current due to impact ionization

In a floating-body PD-SOI MOSFET, a kink occurs in the DC characteristics when the drain voltage is high, as can be seen in the V_{DS}-I_{DS} characteristics simulated using the SOI model (Fig. 6.5(a-b)). It results from excess drain current in the channel due to a drop in the threshold voltage. This drop is caused by a rise in the body potential, which allows holes generated by impact ionization to accumulate in the body. In order to accurately simulate a kink

with the SOI model, it is necessary to extract the impact ionization parameters from the dependence of body current on gate voltage (Fig. 6.6) [6.11].

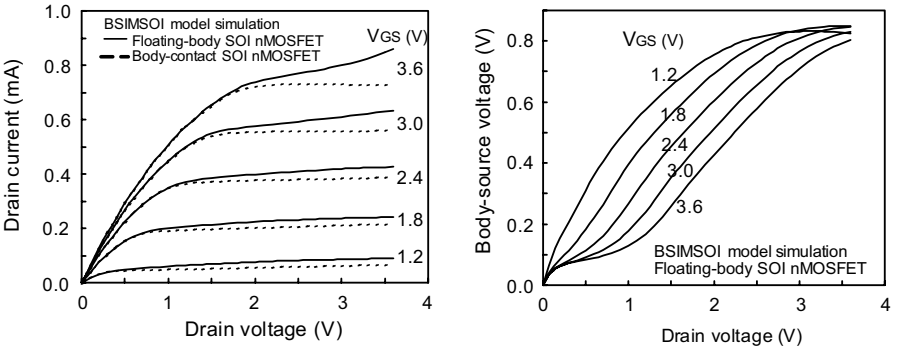

Fig. 6.5 Simulation results on drain current vs. drain voltage and body source voltage vs. drain voltage.

The body resistance affects the current flowing through the body terminal of a body-contact SOI MOSFET. The SOI MOSFET model does not take the shape of the gate into account; so the MOSFETs used for parameter extraction should have the same type of gate as the devices used in circuit design.

In a body-contact PD-SOI MOSFET, no kink occurs because body terminals discharge holes. Moreover, FD-SOI MOSFETs do not exhibit a kink, either, because the low potential barrier between the body and source does not allow holes to accumulate in the body.

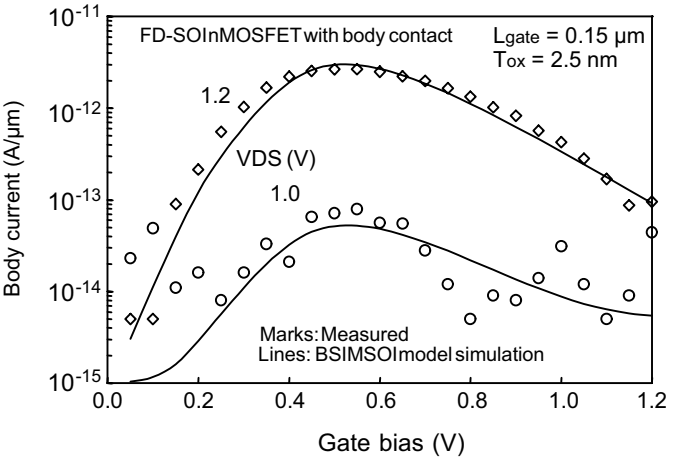

Fig. 6.6 Measured and simulated body current due to impact ionization.

(5) Characteristics of p-n junction diode

In the SPICE model of a MOSFET, the body-source and body-drain p-n junctions are modeled as p-n diodes [6.12]. The characteristics of the p-n junction diodes determine the transient body potential of a floating-body PD-SOI MOSFET [6.10],[6.13]. A MOSFET with an H- or T-shaped gate (Fig. 6.3) is used to measure the current characteristics of the p-n diode between the body and source or drain. The forward-current characteristics of a p-n junction diode are shown in Fig. 6.7. The inflection point in the curve of forward current versus voltage is used as the boundary between the generation-and-recombinat ion region and the diffusion region, and parameters are extracted from each region separately.

(6) Characteristics of parasitic bipolar transistor

A floating-body SOI MOSFET has a lateral parasitic bipolar transistor consisting of the source, body, and drain, which act as the emitter, base and collector, respectively [6.14]. The trigger base current of this transistor is made up of majority carriers produced by impact ionization. When it turns on, there are various consequences, such as a reduction in the breakdown voltage between the source and drain, abnormally steep subthreshold characteristics, increased off-leakage current, and a lower threshold voltage. So, it is necessary to determine the characteristics of this transistor, with the main ones being the Gummel (Fig. 6.8(a)) and the Early (Fig. 6.8(b)) characteristics. A MOSFET with an H-shaped gate (Fig. 6.3) is also used to measure the current characteristics of a lateral parasitic bipolar transistor.

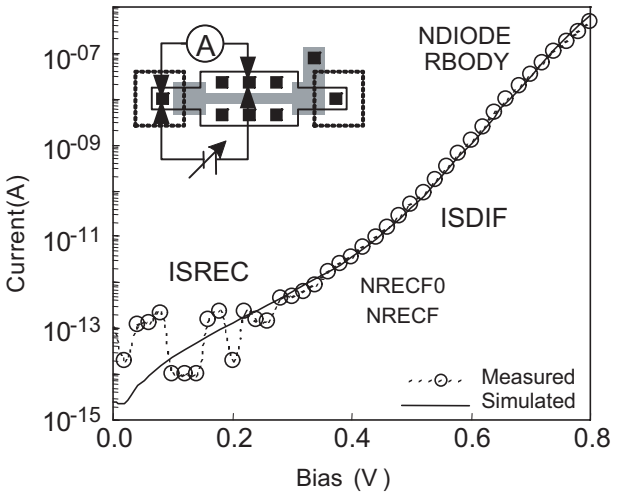

Fig. 6.7 Forward-current characteristics of p-n junction diode.

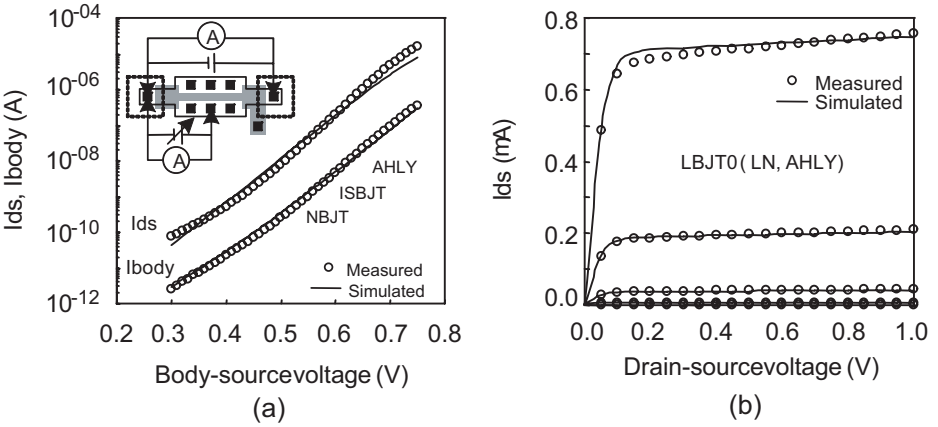

Fig. 6.8 Characteristics of parasitic bipolar transistor. (a) Gummel characteristics and (b) Early characteristics.

(7) Capacitance characteristics

An accurate capacitance model is more important for an SOI than for a bulk MOSFET because the transient behavior due to capacitance coupling affects the gate delay time [6.3]. The method of measuring each capacitance and the main parameters extracted are shown in Fig. 6.9.

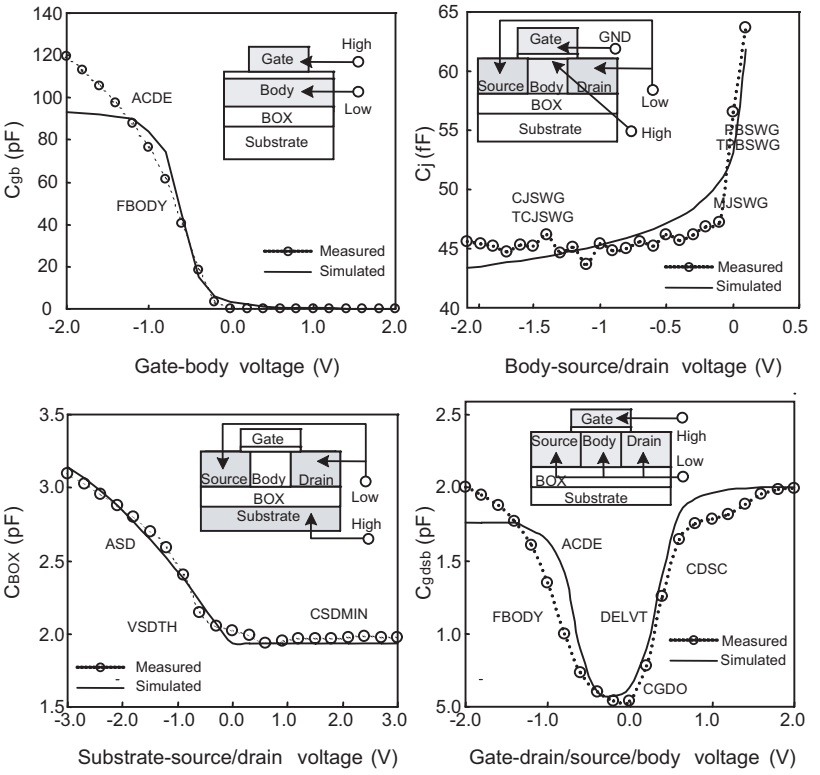

Fig. 6.9 Various C-V measurements.

The capacitances of an SOI MOSFET are modeled by adding SOI-specific capacitances to the bulk C-V model [6.12]:

- the capacitance between the sidewall of the source or drain and the substrate;
- parasitic MOS capacitances between the source or drain and the buried oxide, and between the buried oxide and the substrate; and
- body-to-back-gate coupling.

(8) Self-heating effects

Self-heating is another phenomenon that is not incorporated in the bulk model. An SOI MOSFET is surrounded by SiO_2, which has a lower thermal conductivity than Si; so the heat generated when the device is operating does not dissipate as easily as in a bulk MOSFET. Self-heating causes a local rise in the temperature of a MOSFET, thereby reducing the DC current. The temperature increase is proportional to the current flow per unit time, which in turn depends on the supply voltage and the operating frequency [6.15].

Figure 6.10 shows the measured drain current-voltage characteristics of an SOI nMOSFET with a 2.5-nm-thick gate oxide, a 50-nm-thick SOI film, and a 200-nm-thick buried oxide. It compares the results of DC measurements with those for no self-heating obtained from small-signal S-parameter measurements.

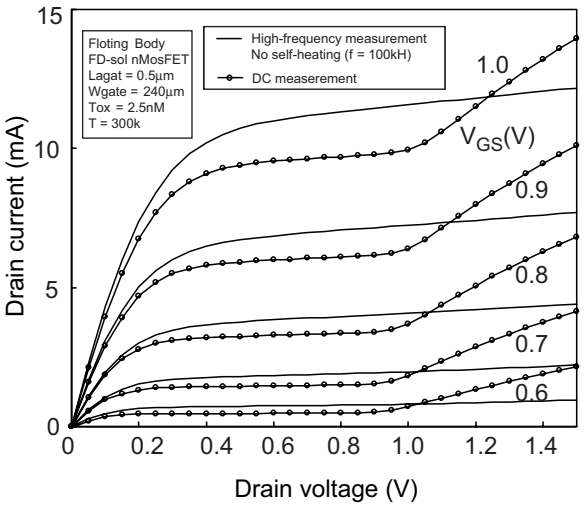

Fig. 6.10 Drain-current characteristics obtained from DC and small-signal S-parameter measurements.

For the small-signal data, the drain current was calculated by integrating the Y parameter obtained from the measured S parameters. As the figure shows, when the frequency is high enough (in this case, 100 MHz), the AC output signal exhibits neither a kink nor degradation in the drain current due to

self-heating. So, if the model parameters are extracted solely from the DC characteristics, the internal temperature of the device will be overestimated and the delay time will be greatly overestimated, resulting in the possibility of a worst-case overestimation.

The effects of self-heating can be incorporated into the SOI model by considering an equivalent circuit containing two current sources: the thermal resistance (R_{th}) and the thermal capacitance (C_{th}) between the device and its surroundings [6.16].

Reported methods of measuring the effects of self-heating involve the application of pulses [6.17] and AC conductance [6.18],[6.19]. In the pulse method, high-speed pulses are applied for a short time; and the resulting increase in the temperature of the device is measured. Although this method provides very accurate results, it has the drawback of being difficult. In the AC conductance method, the dependence of drain conductance on frequency is modeled using the equation [6.20]

$$G_{ds} = G_0 - \frac{I_0 + G_0 V_0}{V_0 - (G_{th} + jwC_{th}) \cdot \dfrac{\Delta T}{\Delta I}}, \tag{6.1}$$

where G0 is the intrinsic drain conductance, G_{th} is the thermal conductance, C_{th} is the thermal capacitance, and R_{th} is the thermal resistance.

The parameters are extracted as described above by measuring the conductance at high frequencies (Fig. 6.11).

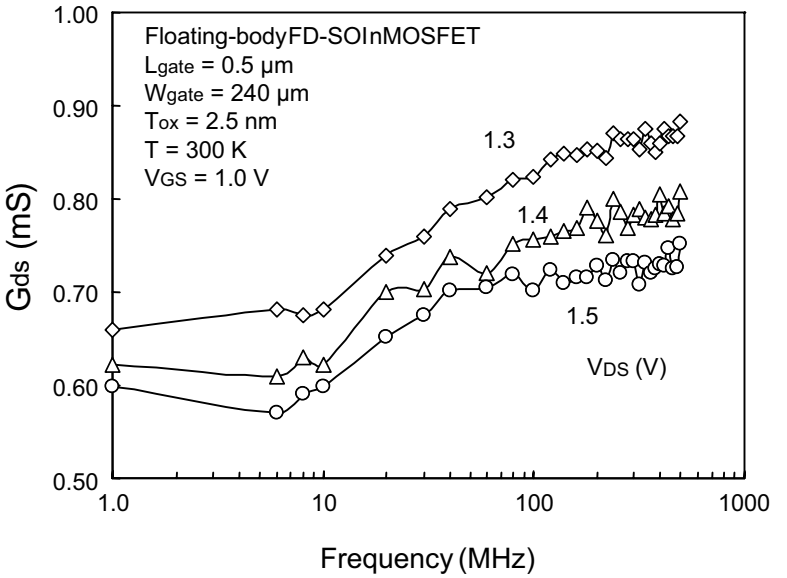

Fig. 6.11 Frequency dependence of output conductance of nMOSFET.

(9) DC characteristics

Regarding the extraction of the DC parameters, the current-voltage characteristics are measured in the same way as for bulk MOSFETs. The DC parameters are first extracted for a body-contact SOI MOSFET; and for a floating-body MOSFET, the various parameters for parasitic devices and self-heating that were previously extracted are used. The recommended procedure for extracting the parameters of a bulk MOSFET is discussed in [6.12],[6.21]. Finally, the testing and evaluation of the extracted parameters are carried out by comparing simulation results with the measured circuit delay for both body-contact and floating-body SOI MOSFETs.

(10) Circuit-level verification (history effect)

The accuracy of the extracted parameters needs to be verified by a delay evaluation at the circuit level. In particular, it is necessary to determine if the simulation results accurately reflect the dynamic behavior due to the history effect of the floating-body potential [6.22]. In a floating-body SOI MOSFET, the transient body potential is determined not only by the charges flowing into and out of the body region, but also by the initial charge on the body (past history). However, since the history effect is caused by fluctuations in the flow of holes into and out of the body region, it is very small in FD-SOI devices

because the body region is always depleted. So, whether or not there is a history effect must be checked through gate-delay measurements.

Figure 6.12 shows the test circuit used to assess the history effect. It contains of long gate-delay path (166 inverters) and a short gate-delay path (16 inverters). The delay time per gate can be derived from the measured delay time of this circuit.

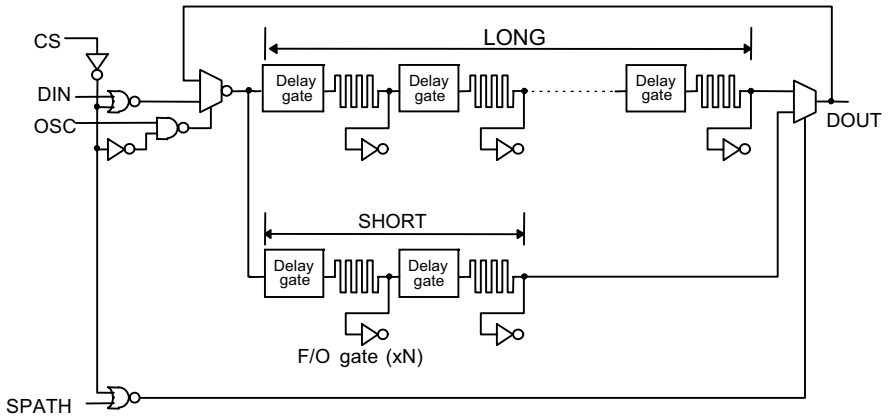

Fig. 6.12 Circuit for measuring delay time.

Figure 6.13 shows how measured gate delay changes over time for inverters made with floating-body SOI MOSFETs with the various threshold voltages listed in the figure. The front gate oxide was 4.5 nm thick, the SOI film was 50 nm thick, the buried oxide was 200 nm thick, and the channel length was 200 nm. The devices with a high threshold voltage (top, middle) were partially depleted, and those with a low threshold voltage (bottom) were fully depleted. The vertical axis is the percent deviation in delay time from the average of the final fall- and rise-time delays. In these measurements, input signals with a frequency of 250 kHz and a duty cycle of 50% were applied to a CMOS inverter after the injection of two types of hold signals (~3 ms), one starting from the DC ground level (0 V) and one from V_{DD} (1.8 V).

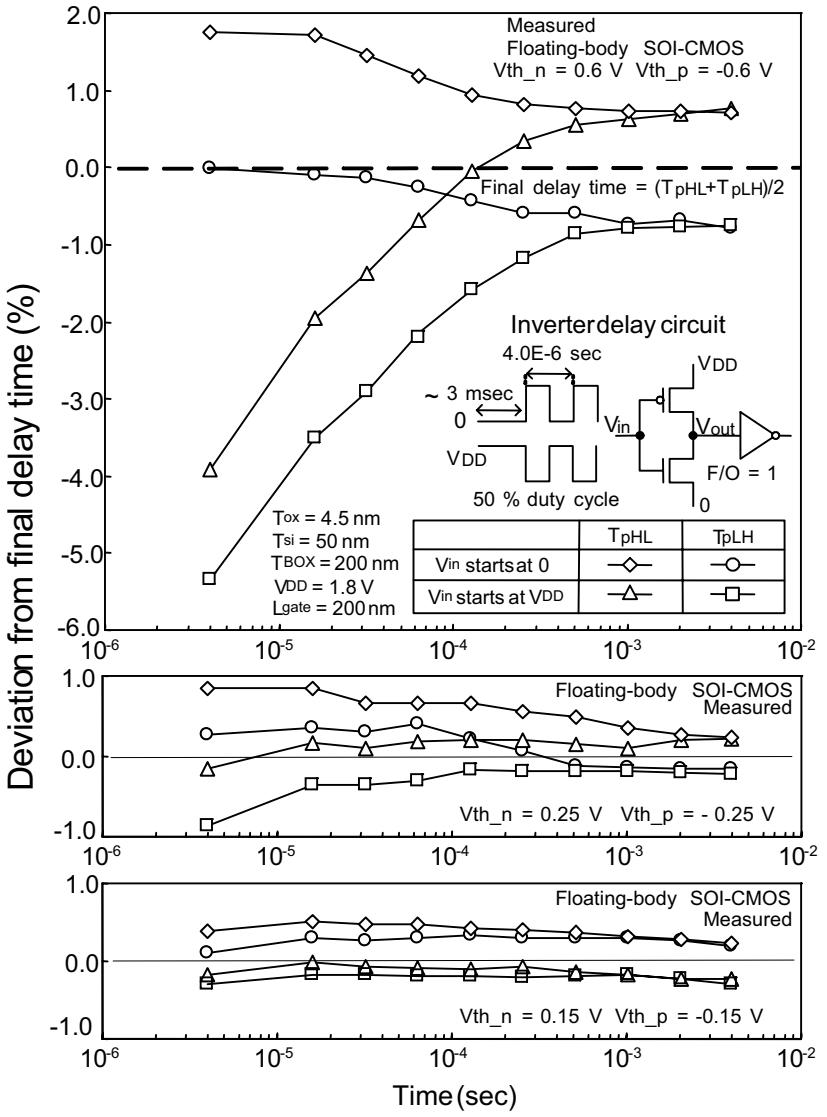

Fig. 6.13 Measured deviation in delay time from final delay time of SOI CMOS inverters with various threshold voltages, where the final delay time is defined to be the average of the final rise- and fall-time delays. The delay time of a PD-SOI CMOS inverter (top, middle) depends on the initial conditions, while that of an FD-SOI CMOS inverter (bottom) is constant.

As shown in Fig. 6.13, the delay time of a floating-body PD-SOI MOSFET depends strongly on the initial state of the input wave; and it is influenced by the history effect, which becomes weaker as the threshold voltage decreases.

A SPICE simulation on the time-wise change in the gate delay of an inverter made with floating-body PD-SOI MOSFETS (Fig. 6.14) was carried out, assuming that an input signal with a frequency of 50 MHz and a duty cycle of 50% was applied after two types of hold signals (~30 ns), one starting from the DC ground level (0 V) and one from V_{DD} (1.8 V).

Figures 6.15 and 6.16 show the time-wise change in the initial state of the body potential for the inverter used to obtain the data in Fig. 6.14. As can be seen, the fall-time delay (T_{pHL}) and the rise-time delay (T_{pLH}) change in response to changes in the body bias of the p- and n-MOSFETs.

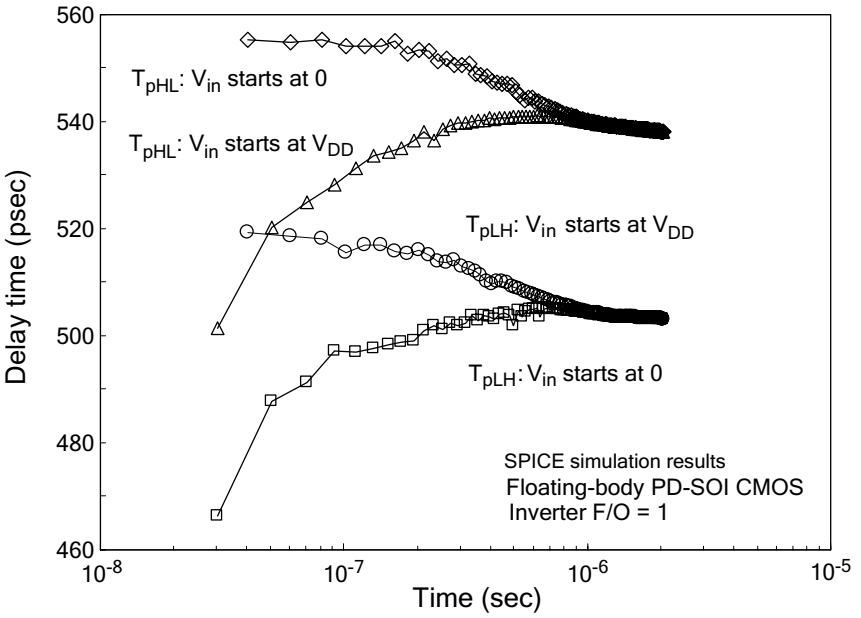

Fig. 6.14 Simulated delay time of PD-SOI CMOS inverter.

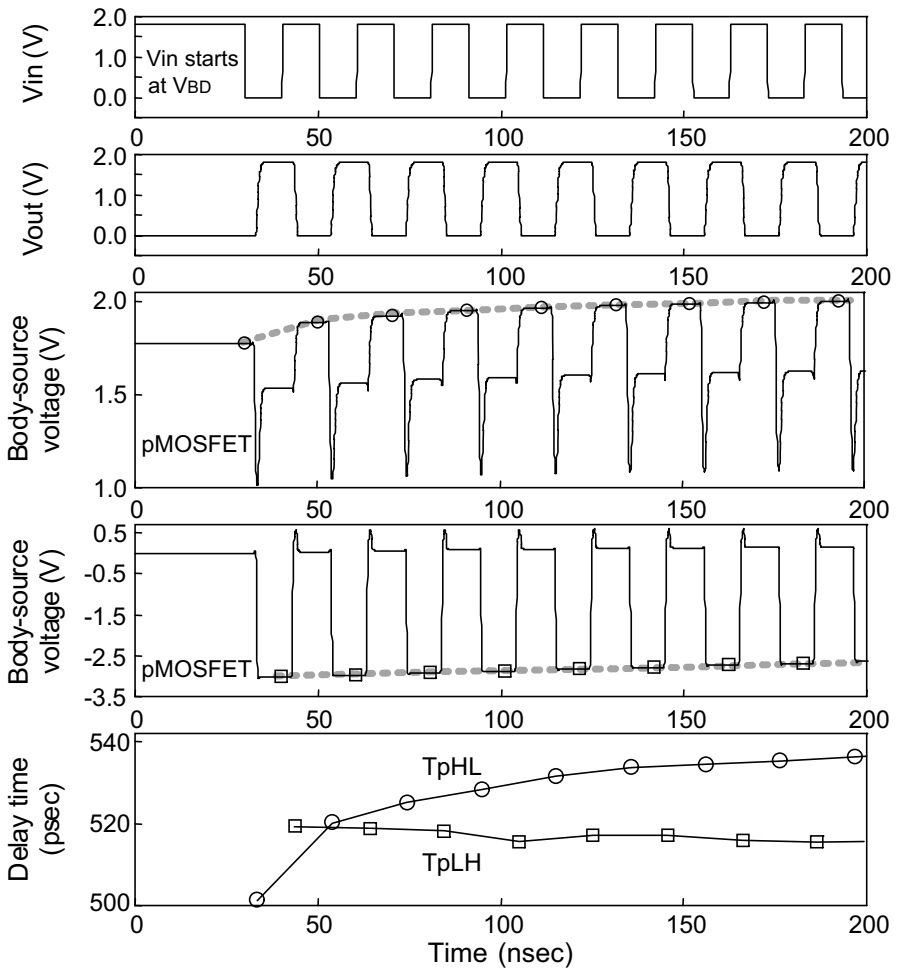

Fig. 6.15 Time-wise change in initial state of CMOS inverter used to obtain data in Fig. 6.14: (a) input signal, (b) output signal, (c) body voltage of pMOSFET, (d) body voltage of nMOSFET, and (e) delay time of inverter when V_{in} starts at V_{DD}.

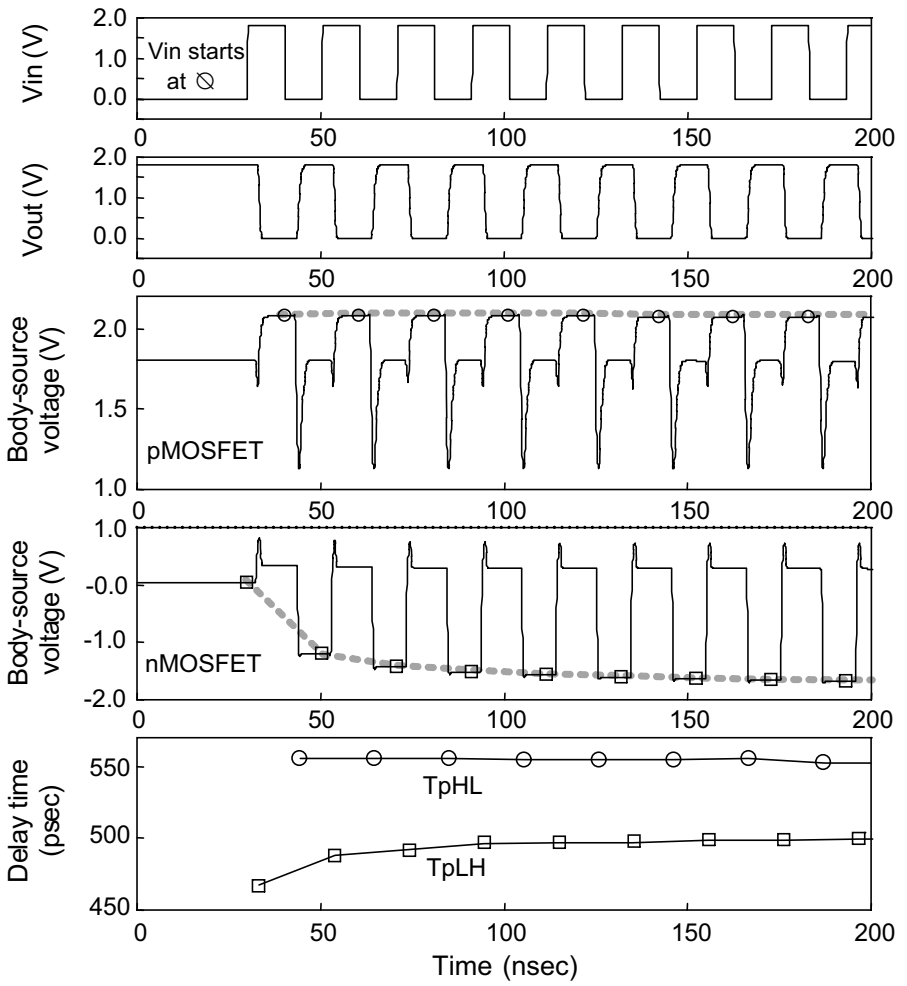

Fig. 6.16 Time-wise change in initial state of CMOS inverter used to obtain data in Fig. 6.14: (a) input signal, (b) output signal, (c) body voltage of pMOSFET, (d) body voltage of nMOSFET, and (e) delay time of inverter when V_{in} starts at 0.

As we have seen, the characteristics of the p-n junction diode are important in modeling the history effect. Figure 6.17 shows simulation results on what happens when the value of the body-to-source/drain p-n junction diode current (ISDIF) is lowered from 1.613E-06 to 1.0E-09. Reducing the forward current of the p-n junction diode suppresses the change in the body bias, thereby making the change in delay time smaller.

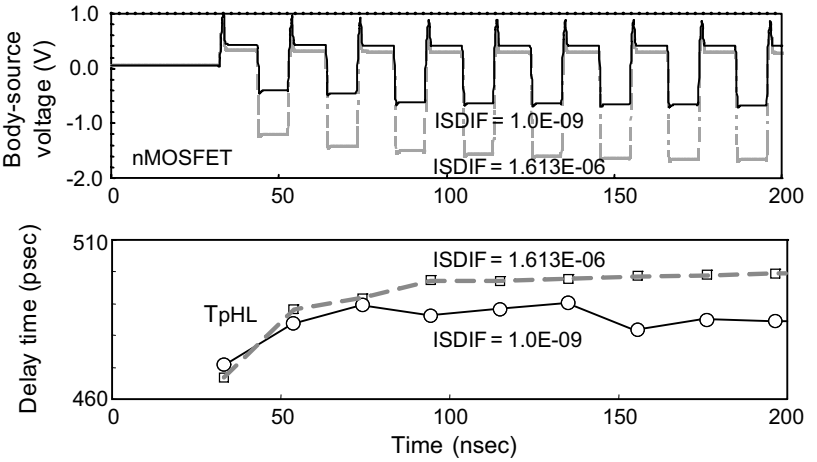

Fig. 6.17 Simulated body potential for two values of the parameter ISDIF (body-to-source/drain injection saturation current).

6.4 Example of SOI MOSFET Simulation

(1) SOI MOSFET simulation using BSIMSOI
The Berkeley BSIM models have become the industry standard for bulk Si. The BSIMSOI is based on the BSIM3 bulk MOS model, and newly incorporates a unified body-source built-in potential lowering model. Figures 6.18 and 6.19 show an example of BSIMSOI model parameters for both n- and pMOSFETs. The BSIMSOI model uses up to about 140 parameters in its model definition, and works with most SPICE simulators

Figure 6.20 shows an example of a netlist for the simulation of ID-VD characteristics. The main difference between the descriptions of SOI and bulk devices is the pin-outs. In an SOI MOSFET, the fourth node is the substrate, and the fifth node is the body. The body node is not connected in a floating-body device. In this netlist, mn_bf represents a floating-body MOSFET, and mn_bc represents a body-contact MOSFET. The IDS-VDS characteristics simulated using this netlist and the model parameters in Fig. 6.20 are shown in Fig. 6.5. As can be seen, the behavior of the body is monitored by using a netlist monitor statement in the PRINT command in Fig. 6.20.

Figures 6.21 and 6.22 are an example of a netlist for a gate delay-time simulation. The results of using this netlist and the model parameters in Fig. 6.18 and 6.19 are shown in Fig. 6.14. As can be seen, the SOI MOSFET model explains the history effects that appear in gate delay measurements like Fig. 6.13 very well.

```
* FILE name:  soi_nmos.inc
* SPICE:      HSPICE 2004.9 later  (HSPICE is a trademark of Synopsys, Inc.)
* MODEL:      BSIMSOI3.2
* Device:     SOInMSOFET

.model  nch NMOS
+ Level=57  VERSION=3.2  SOIMOD=1  SHMOD=1
+ PARAMCHK=0  BINUNIT=1  MOBMOD=1  CAPMOD=3  TNOM=25
+ TOX=4.5E-09  TSI=5.25E-08  TBOX=2E-07  NCH=1.66E+18  NSUB=1E+015
+ XJ=4E-08  VBSA=2.862  NOFFFD=1  VOFFFD=0.6902  K1B=1.161  K2B=0
+ DK2B=0  DVBD0=0  DVBD1=0  MOINFD=1062  WINT=0  LINT=6E-09
+ VTH0= 0.95 K1=0.475  K2=0  K3=-7.244  K3B=0  NLX=1E-08
+ DVT0=1.862  DVT1=0.2064  DVT2=-7.247E-05  DVT0W=1E-15  DVT1W=5.3E+06
+ U0=131.2  UA=-9.23E-10  UB=6.409E-19  UC=0
+  WU0=-22  WUA=-4.2E-10  WUB=3.605E-19
+ PU0=-2.464  PUA=-1.658E-011  PUB=-8.205E-021  PUC=0
+ VSAT=9.395E+04  A0=1.242  AGS=0.686  B0=1.588E-07  B1=1E-09  PA0=-0.072
+ KETA=0  KETAS=0  A1=0  A2=1  RDSW=1038
+ NFACTOR=0.442  VOFF=-0.09315  ETA0=0.455  ETAB=0  DSUB=0.56
+ CIT=0  CDSC=2.0e-5  CDSCB=0  CDSCD=0
+ PCLM=0.3162  PDIBLC1=0.1014  PDIBLC2=1.004E-05
+ DROUT=0.6209  PDIBLCB=0  PVAG=0  ALPHA0=1.428E-07  DELTA=0.01
+ FBJTII=0  BETA0=0.02374  BETA1=0  BETA2=0.09534  VDSATII0=0.8974
+ VDSATII0=0.8  lii=5E-08  tii=-0.2  ESATII=1E+07
+ SII0=1.544  SII1=0.2327  SII2=4.441E-014  SIID=4.441E-014
+ AGIDL=1E-015  BGIDL=1E+09  NGIDL=1.1  NTUN=14
+ NDIODE=1.118  NRECF0=2.563  NRECR0=0.5656
+ ISBJT=1.368E-07  ISDIF=1.613E-06  ISREC=0.01257  ISTUN=2E-05
+ LN=1.66E-06  VREC0=1E-06  VTUN0=0  NBJT=1.15  LBJT0=4.742E-06
+ VABJT=-2.175 AELY=5.409E+07 AHLI=1.066E-012  RBODY=721.5  RBSH=2547
+ RHALO=1E+015  IGMOD=0  TOXQM=3.2E-09  NTOX=1  TOXREF=2.5E-09  EBG=1.2
+ ALPHAGB1=0.35  BETAGB1=0.03  VGB1=300
+ VEVB=0.075  ALPHAGB2=0.43  BETAGB2=0.05
+ VGB2=17  VECB=0.026  XPART=0  CGSO=1.127E-10  CGDO=1.127E-10  CGEO=0
+ CJSWG=5.572E-011  PBSWG=0.05186  MJSWG=0.2502  TT=5.699E-12
+ NDIF=1  LDIF0=-0.009071  VSDFB=-1  VSDTH=-0.02336  CSDMIN=0.0001486
+ ASD=0.919  CSDESW=2.197E-11  CGSL=5.027E-11  CGDL=5.027E-11  CKAPPA=1
+ CF=1E-12  CLC=1E-07  CLE=0.6  DLC=6E-09  DLCB=6E-09  DELVT=-0.05012
+ FBODY=0.873  ACDE=1.581  MOIN=15
+ UTE=-0.9455  KT1=-0.3  KT1L=3.811E-09  KT2=-0.002477
+ UA1=1.239E-09  UB1=-1.016E-018  UC1=-5.6E-013  AT=2.911E+04
+ TCJSWG=0.0001  TPBSWG=0  CTH0=3.522E-05  RTH0=2.365E-02  PRT=760
+ NTRECF=0.4722  NTRECR=0.7315  XBJT=1.126  XDIF=1.052  XREC=0.7975  XTUN=0.01
```

Fig. 6.18 Example of parameters for the BSIMSOI3.2 nMOSFET model used in the simulations for this chapter.

```
* FILE name:  soi_pmos.inc
* SPICE:      HSPICE 2004.9 later  (HSPICE is a trademark of Synopsys, Inc.)
* MODEL:      BSIMSOI3.2
* Device:     SOIpMSOFET

.model   pch PMOS
+ Level=57  VERSION=3.2  SOIMOD=1  SHMOD=1
+ PARAMCHK=0  BINUNIT=1  MOBMOD=1  CAPMOD=3  TNOM=25
+ TOX=4.5E-09  TSI=5.25E-08  TBOX=2E-07  NCH=1.66E+18  NSUB=-1E+15
+ XJ=2.4E-08  VBSA=2.396  NOFFFD=1  VOFFFD=0.114  K1B=1  K2B=0
+ DK2B=0  DVBD0=0.558  DVBD1=0  MOINFD=1008  WINT=0  LINT=6E-09
+ VTH0=-0.73  K1=0.6  K2=0  K3=1.77  K3B=0  KB1=1
+ NLX=1E-010  DVT0=2.71  DVT1=0.4032  DVT2=-0.032  DVT0W=0
+ DVT1W=5.3E+06  DVT2W=-0.032
+ U0=65.13  UA=1E-10  UB=5.2E-19  UC=0
+ WU0=-19.57  WUA=-4.493E-10  WUB=4.898E-19
+ PU0=0.657  PUA=2.233E-10  PUB=-2.73E-20
+ VSAT=8.528E+04  A0=1.588  AGS=0.6107  B0=7E-08  B1=0  LA0=-0.2018  LAGS=0.1412
+ KETA=0  KETAS=0  A1=0  A2=1  RDSW=3060
+ NFACTOR=0.5546  VOFF=-0.1233  ETA0=0.3357  ETAB=-0.07  DSUB=0.56
+ CIT=0  CDSC=2.0e-4 CDSCB=0 CDSCD=0
+ PCLM=2.288  PDIBLC1=0.2265  PDIBLC2=0.004
+ DROUT=0.56  PDIBLCB=-0.234  PVAG=0  ALPHA0=1E-10  DELTA=0.01
+ FBJTII=0  BETA0=0.01747  BETA1=0  BETA2=0.09673  VDSATII0=0.9173
+ VDSATII0=0.8  lii=5E-08  tii=-0.2  ESATII=1E+07
+ SII0=1.072  SII1=4.441E-14  SII2=0.5126  SIID=0.02354
+ AGIDL=0  BGIDL=0  NGIDL=1.2  NTUN=10
+ NDIODE=1.124  NRECF0=1.555  NRECR0=10
+  ISBJT=1.088E-06  ISDIF=3.69E-06  ISREC=0.0003871  ISTUN=0
+ LN=2E-06  VREC0=0  VTUN0=0  NBJT=0.5137  LBJT0=8.017E-06
+ VABJT=10  AELY=0  AHLI=1.207E-11  RBODY=625.1  RBSH=1800
+ RHALO=1E+15  IGMOD=0  TOXQM=3.2E-09  NTOX=1  TOXREF=2.5E-09  EBG=1.2
+ ALPHAGB1=0.35  BETAGB1=0.03  VGB1=300
+ VEVB=0.075  ALPHAGB2=0.43  BETAGB2=0.05
+ VGB2=17  VECB=0.026  XPART=0  CGSO=2.512E-10  CGDO=2.512E-10  CGEO=0
+ CJSWG=8.356E-11  PBSWG=0.6507  MJSWG=0.9  TT=3.65E-012
+ NDIF=1  LDIF0=1  VSDFB=-1.345  VSDTH=0.28  CSDMIN=0.0001486  ASD=0.333
+ CSDESW=0  CGSL=0  CGDL=0  CKAPPA=0.6  CF=1E-20  CLC=1E-08
+ CLE=0  DLC=6E-09  DLCB=6E-09  DELVT=-0.07244  FBODY=1.187  ACDE=1.858
+ MOIN=15  UTE=-0.1502  KT1=-0.2322  KT1L=3.17E-09  KT2=0.022
+ UA1=3.664E-09  UB1=-2.911E-18  UC1=-5.6E-11  AT=3.3E+04
+ TCJSWG=0.0001  TPBSWG=0  PRT=0  CTH0=3.522E-05  RTH0=2.365E-02
+ NTRECF=0.3063  NTRECR=0.6602  XBJT=1.121  XDIF=1.07  XREC=0.8963  XTUN=0.01
```

Fig. 6.19 Example of parameters for the BSIMSOI3.2 pMOSFET model used in the simulations for this chapter.

```
*  SOI nMOSFET  Vds-Ids simulation
*  SPICE:         HSPICE 2004.9 later   (HSPICE is a trademark  of Synopsys, Inc.)
*  MODEL:       BSIMSOI3.2

.inc './soi_nmos.inc'
.para ln=0.2u   wn=1.0u  dn=2.0u
.temp 25

* Floating-body SOI nMOSFET
mn_bf   d   g   s   e          nch  w=wn  l=ln  ad='wn*dn'  pd= '(wn+dn)*2‘

* Grounded-body SOI nMOSFET
mn_bc   d   g   s   e    b    nch  w=wn  l=ln  ad='wn*dn'  pd='( wn+dn)*2‘

vg   g   0     dc  0.0
vd   d   0     dc  0.0
vs   s   0     dc  0.0
ve   e   0     dc  0.0
vb   b   0     dc  0.0
.dc   vd   0   3.6   0.1      sweep   vg   0.6   3.6   0.2

.print dc id=i(mn_bf)
+ Vth=LV9(mn_bf)   Vbody=LX52(mn_bf)  Vbs=LX43(mn_bf)
+ Temp=LX51(mn_bf)   Ich=LX44(mn_bf)   Iii=LX46(mn_bf)
+ Ibjt=LX45(mn_bf)   Ibs=LX5(mn_bf)

.print dc id=i(mn_bc)
+ Vth=LV9(mn_bc)   Vbody=LX52(mn_bc)  Vbs=LX43(mn_bc)
+ Temp=LX51(mn_bc)   Ich=LX44(mn_bc)  Iii=LX46(mn_bc)
+  Ibjt=LX45(mn_bc)   Ibs=LX5(mn_bc)

.end
```

Fig. 6.20 Example of netlist for SPICE DC simulation, the results of which are shown in Fig. 6.5.

```
*  Inverter delay time simulation (Vin start at Vdd & Vin start at 0 V )
*  SPICE:         HSPICE 2004.9 later   (HSPICE is a trademark of Synopsys, Inc.)
*  MODEL:       BSIMSOI3.2

.option nopage   method=gear  post ingold=2
.inc './inc_lib.sp'
.temp 25
.param  ln=0.2u lp=0.2u wn=0.8u wp=1.0u dn=1.0u dp=1.0u  cload=0.034pF
.param vdd$=1.8v tper$=10ns toff$=20ns tr$=0.2ns tf$=0.2ns nsampling$ = 210
x1   n1  n0  vdd 0   inv_fb
x2   n2  n1  vdd 0   inv_fb
x3   n3  n2  vdd 0   inv_fb
x4   n4  n3  vdd 0   inv_fb
x5   n5  n4  vdd 0   inv_fb
x6   n6  n5  vdd 0   inv_fb
x7   n7  n6  vdd 0   inv_fb
x8   n8  n7  vdd 0   inv_fb
vdd  vdd 0 vdd$

*Vin start at Vdd
vin n0 0 pwl (toff$ vdd$, 'tper$+toff$' vdd$, 'tper$+tr$+toff$' 0v,
          '2*tper$+tr$+toff$' 0v, '2*tper$+tr$+tf$+toff$' vdd$, R toff$ )
*Vin start at 0 V
*  vin n0 0 pwl (toff$ 0v, 'tper$+toff$' 0v,  'tper$+tr$+toff$' vdd$,
*  +           '2*tper$+tr$+toff$' vdd$, '2*tper$+tr$+tf$+toff$' 0v, R toff$ )

.param vm$='0.5*vdd$'
.inc './inc_delay_meas.sp'
.tran 0.1ns 'tper$*nsampling$'

*nmos information print out
.print tran  v(n0)  v(n6)  v(n7)
+ Vth = LV9(x7.mn_a)    Vbody   = LX52(x7.mn_a)    Vbs  = LX43(x7.mn_a)
+ Ich = LX44(x7.mn_a)   Iii     = LX46(x7.mn_a)    Ibjt = LX45(x7.mn_a)
+ Ibs = LX5(x7.mn_a)    SH_Temp = LX51(x7.mn_a)
*pmos information print out
.print tran  v(n0)  v(n6)  v(n7)
+ Vth = LV9(x7.mp_a)    Vbody   = LX52(x7.mp_a)    Vbs  = LX43(x7.mp_a)
+ Ich = LX44(x7.mp_a)   Iii     = LX46(x7.mp_a)    Ibjt = LX45(x7.mp_a)
+ Ibs = LX5(x7.mp_a)    SH_Temp = LX51(x7.mp_a)

*model parameter file include
.inc './soi_nmos.inc'
.inc './soi_pmos.inc'
.end
```

Fig. 6.21 Example of netlist for SPICE delay-time simulation, the results of which are shown in Fig. 6.14.

```
* File name: inc_lib.sp

* body contacted cmos inverter
.subckt inv_tb out in vdd gnd ln=0.2u lp=0.2u wn=0.8u wp=1.0u dn=1.0u dp=1.0u cload=0.034pF
mp_a out in vdd gnd vdd pch w=wp l=lp ad='wp*dp' pd='(wp+dp)*2' as='wp*dp' ps='(wp+dp)*2'
mn_a out in gnd gnd gnd nch w=wn l=ln ad='wn*dn' pd='(wn+dn)*2' as='wn*dn' ps='(wn+dn)*2'
cl out 0 cload
.ends inv_tb

* foating body cmos inverter
.subckt inv_fb out in vdd gnd ln=0.2u lp=0.2u wn=0.8u wp=1.0u dn=1.0u dp=1.0u cload=0.034pF
mp_a out in vdd gnd pch w=wp l=lp ad='wp*dp' pd='(wp+dp)*2' as='wp*dp' ps='(wp+dp)*2'
mn_a out in gnd gnd nch w=wn l=ln ad='wn*dn' pd='(wn+dn)*2' as='wn*dn' ps='(wn+dn)*2'
cl out 0 cload
.ends inv_fb
```

```
* File name : inc_delay_meas.sp

*TpHL measurement
.meas tplh_1 trig v(n0) val=vm$ fall=1 targ v(n7) val=vm$ rise=1
.meas tplh_2 trig v(n0) val=vm$ fall=2 targ v(n7) val=vm$ rise=2
.meas tplh_3 trig v(n0) val=vm$ fall=3 targ v(n7) val=vm$ rise=3
.meas tplh_4 trig v(n0) val=vm$ fall=4 targ v(n7) val=vm$ rise=4
.meas tplh_5 trig v(n0) val=vm$ fall=5 targ v(n7) val=vm$ rise=5
                :
.meas tplh_98 trig v(n0) val=vm$ fall=98 targ v(n7) val=vm$ rise=98
.meas tplh_99 trig v(n0) val=vm$ fall=99 targ v(n7) val=vm$ rise=99
.meas tplh_100 trig v(n0) val=vm$ fall=100 targ v(n7) val=vm$ rise=100

*TpLH measurement
.meas tphl_1 trig v(n0) val=vm$ rise=1 targ v(n7) val=vm$ fall=1
.meas tphl_2 trig v(n0) val=vm$ rise=2 targ v(n7) val=vm$ fall=2
.meas tphl_3 trig v(n0) val=vm$ rise=3 targ v(n7) val=vm$ fall=3
.meas tphl_4 trig v(n0) val=vm$ rise=4 targ v(n7) val=vm$ fall=4
.meas tphl_5 trig v(n0) val=vm$ rise=5 targ v(n7) val=vm$ fall=5
                :
.meas tphl_98 trig v(n0) val=vm$ rise=98 targ v(n7) val=vm$ fall=98
.meas tphl_99 trig v(n0) val=vm$ rise=99 targ v(n7) val=vm$ fall=99
.meas tphl_100 trig v(n0) val=vm$ rise=100 targ v(n7) val=vm$ fall=100
```

Fig. 6.22 Example of netlist for SPICE simulation, the results of which are shown in Fig. 6.14.

(2) SOI simulation using bulk MOS model
As shown in Fig. 6.13, in FD-SOI MOSFETs, the history effect does not occur or is negligible; and self-heating can also be ignored if the supply voltage is low. This allows us to use the bulk MOSFET model to compute the delay of logic and analog circuits made with these devices. Nevertheless, problems arise, as described below, when the bulk MOSFET model is used to extract parameters for the SOI MOSFET model.

One problem that occurs when the parameters of a floating-body SOI MOSFET are extracted using the bulk model is that the substrate terminal of the SOI MOSFET corresponds to the well terminal of the bulk device [6.6]. In a bulk CMOS inverter (Fig. 6.23(a)), the body (well) terminal of both n- and p-MOSFETs is connected to the same potential as the source. In contrast, for an SOI CMOS inverter (Fig. 6.23(b)), the substrate terminals of all the MOSFETs are connected to the ground level. Comparing the two devices, we see that the potentials are the same for bulk and SOI nMOSFETs, while the substrate terminal is different for bulk and SOI pMOSFETs.

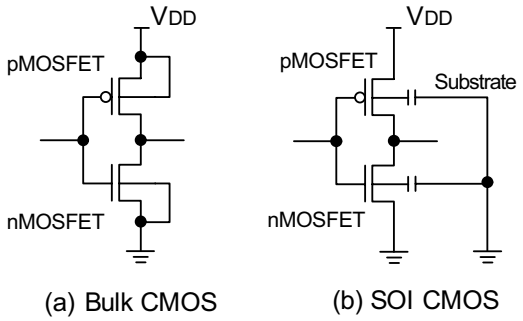

Fig. 6.23 Connection topology of CMOS inverter as represented in SPICE netlist.

When the bulk pMOSFET model is used to extract parameters for an SOI pMOSFET, the measurements are made by applying a negative potential relative to the source terminal (Fig. 6.24); and the values obtained are used as

data in the bulk model. However, although the pMOSFET parameters extracted in this way accurately reflect the characteristics, they do so only for the particular supply voltage (V_{DD}) used in the measurements. That is, the parameters do not yield accurate results at other supply voltages. Furthermore, when pMOSFETs are cascode connected, as they are in a CMOS NOR gate, the drain voltage is different for each MOSFET; and so the characteristics cannot be accurately simulated.

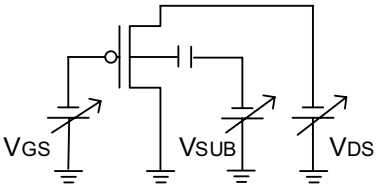

Fig. 6.24 Connections used in measurement of I-V characteristics of SOI pMOSFET.

As described above, an SOI MOSFET model is essential for the accurate simulation of circuits made with FD-SOI as well as PD-SOI devices. The latest circuit simulators employ models that can handle a continuum of representations from PD-SOI to FD-SOI devices; and simulations can also be carried out for various operating modes.

The SOI MOSFET model will be even more necessary for the design of circuits made with future FD-SOI devices in which the threshold voltage is adjusted by changing the substrate bias, such as an ED-CMOS circuit made with undoped FD-SOI MOSFETs [6.23] and an SRAM made with FD-SOI MOSFETs with a very thin BOX [6.24].

6.5 Summary

This chapter described the method of parameter extraction for the SOI SPICE model, and the influence of the parameters on circuit behavior. A sample netlist and parameters were shown, and the transient simulation results were found to agree with the measured ones very well. For accurate circuit simulations, the SOI SPICE model must take floating-body and self-heating effects into account, even for FD-SOI MOSFETs.

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Chapter 7

APPLICATIONS

7.1 Introduction

In the era of ubiquitous computing, there will be a great need for ultralow-power short-range wireless systems, such as systems that are self-powered by ambient energy sources. A severe ultralow-power requirement of 1-10 mW will arise for the LSIs of these systems. To verify the effectiveness of ultralow-voltage FD-SOI circuit techniques, which are based on the MTCMOS/SOI circuit scheme and target supply voltages from 0.5 to 1 V, various ultralow-power wireless systems were fabricated and evaluated. The technologies cover analog/RF circuits and a DC-DC converter. This chapter describes three ultralow-voltage wireless systems:

(1) 1-V Bluetooth RF transmitter and receiver;
(2) Solar-powered, radio-controlled watch;
(3) Self-powered short-range wireless system.

7.2 1-V Bluetooth RF Transceiver and Receiver

7.2.1 Transceiver

A. System architecture

A 1-V Bluetooth RF transceiver (Fig. 7.1) was fabricated on a 0.2-μm CMOS/SOI process [7.1] [7.2]. Section 5.2 describes most of the building blocks. Since Bluetooth is a time division duplexing (TDD) system and since MOSFETs are suitable for making a transmit/receive (T/R) switch, a T/R switch is integrated on the chip to reduce the number of off-chip components. A double-conversion receiver architecture with a first IF of 110 MHz was selected because the channel-select filter is off chip. An off-chip surface acoustic wave (SAW) filter was chosen because, although it increases the cost of the module, it makes the maximum usable level very large and because an on-chip channel-select filter would have increased power consumption. The image-rejection mixer (IRM) has an LC-tank folded structure for low-voltage operation. Both the RF filter and the IRM suppress out-of-band image signals.

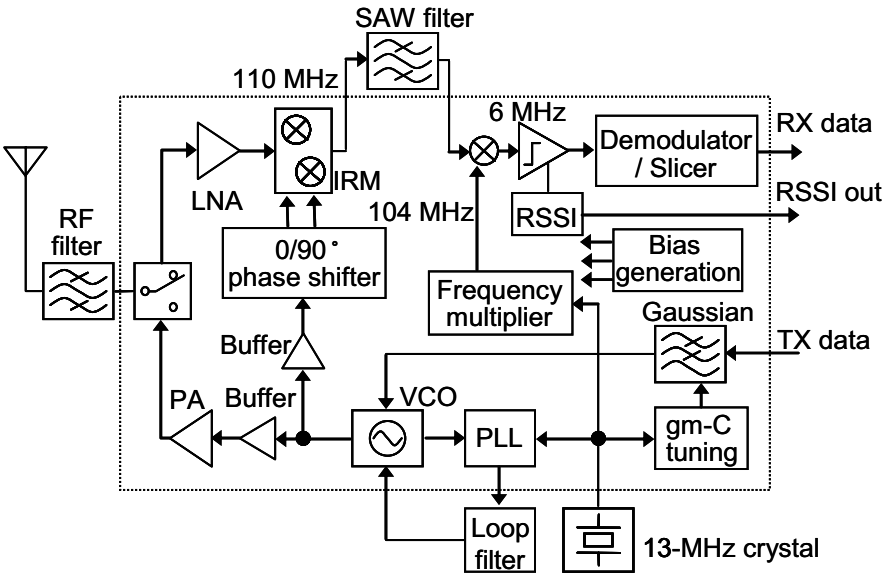


Fig. 7.1 1-V Bluetooth RF transceiver.

To make an on-chip quadrature demodulator with a low power consumption, the first IF is down-converted to 6 MHz (2nd IF) using a 2nd LO signal of 104 MHz. The 2nd LO signal is generated by a frequency multiplier (×8) from the reference frequency of an external 13-MHz crystal oscillator. Since Gaussian-filtered frequency shift keying (GFSK) employs a constant envelope, the 2nd IF is fed to a limiting amplifier and then to the demodulator. The limiting amplifier has a received-signal-strength indicator (RSSI) as well.

The transmit path starts with an on-chip Gaussian pulse-shaping g_m-C filter, and the output of the filter directly modulates the LC-tank voltage-controlled oscillator (VCO). During modulation, the PLL synthesizer is kept in the open-loop mode. The cascode power amplifier (PA) with a drive buffer (Buff) amplifies the modulated signal up to 1 mW (0 dBm), which is the Class-3 output power level.

B. PLL synthesizer

This section describes a PLL synthesizer with a VCO. The PLL synthesizer (Fig. 7.2) has an integer-N type configuration consisting of a reference divider, a phase frequency detector, a charge pump, a VCO, and a programmable divider [7.3].

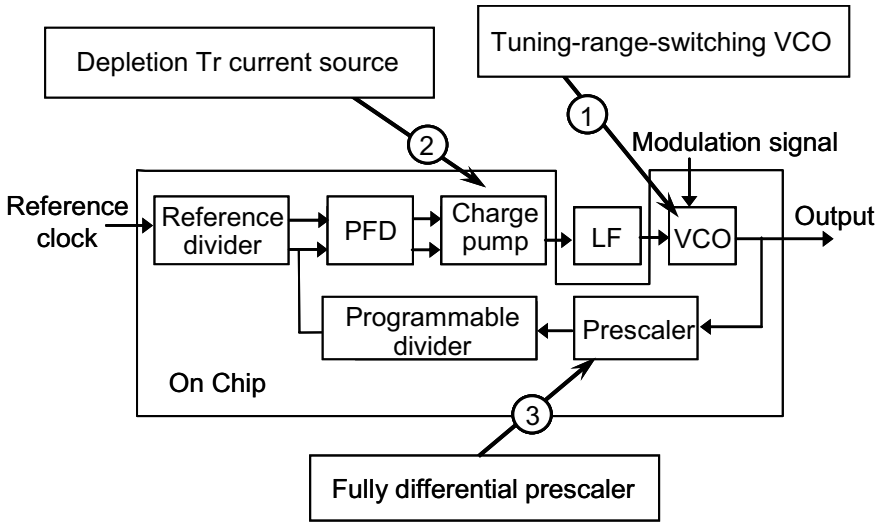


Fig. 7.2 Bock diagram of PLL synthesizer.

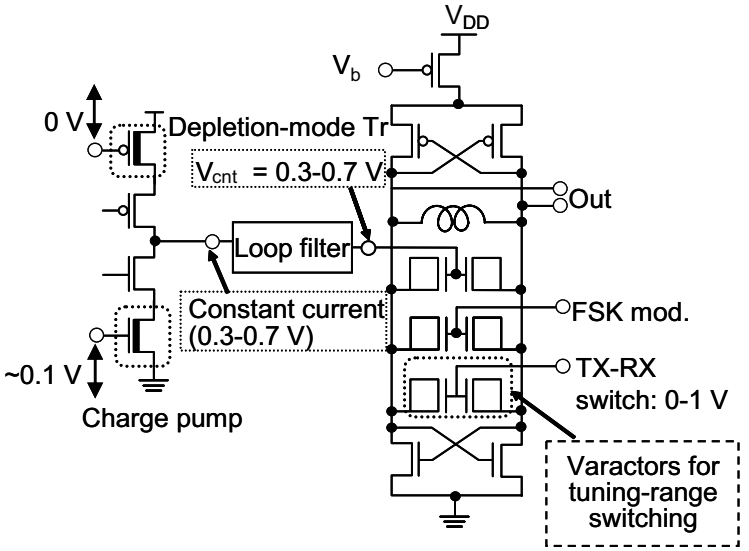
To keep the layout area small, the loop filter is not on the chip. The programmable divider is a pulse-swallow type and is composed of a dual-modulus prescaler and two CMOS counters.

This PLL synthesizer has three main features [7.3]:

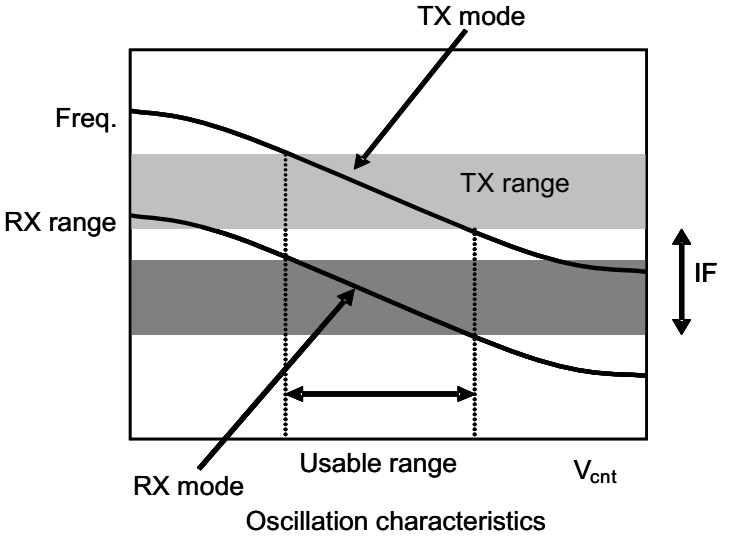
1. A tuning-range-switching VCO provides low-voltage operation and a 110-MHz frequency shift of the IF between the transmit and receive modes.
2. A charge pump using depletion-mode transistors as current sources provides constant current sourcing at a low supply voltage.
3. A fully-differential prescaler provides a sufficient operating margin at a low supply voltage

The VCO (Fig. 7.3(a)) employs a tuning-range-switching technique that provides a wide frequency range at a low supply voltage. It is a CMOS differential type, in which cross-coupled nMOS and pMOS pairs produce a negative resistance, and has three nMOS varactors (variable capacitors). Two of them are for fine and course frequency control, and the third is for GFSK modulation. To obtain a 110-MHz frequency shift between the transmit and receive modes (Fig. 7.3(b)), a 0-V or 1-V signal is applied to the gate of the coarse varactor. This configuration enables fast frequency switching because the output of the loop filter remains almost constant during a switching operation. The charge pump produces a constant current for output voltages between 0.3 V and 0.7 V, even on a 1-V supply, because the current sources are depletion-mode transistors.

A fully differential dual-modulus prescaler (Fig. 7.4) is used in the PLL because differential circuit architecture has advantages over single-ended architecture, especially when the supply voltage is low. At a low supply voltage, the amplitude of the signal has to be small, which means that the noise and DC offset margins of the signal are also small. On the other hand, the signal amplitude in a fully differential scheme is twice as large as that in a single-ended scheme. This makes the noise and DC offset margin of the signal large. The prescaler features two feedback paths (FF2 to FF1, FF3 to FF1) that provide differential signals. Since these paths determine the maximum operating frequency, making them differential is a very effective way to increase the frequency. This circuit is composed of a current-mode fully differential OR/NOR gate and a conventional D-FF.



(a)



(b)

Fig. 7.3 Tuning-range-switching VCO: (a) circuit with charge pump and (b) tuning

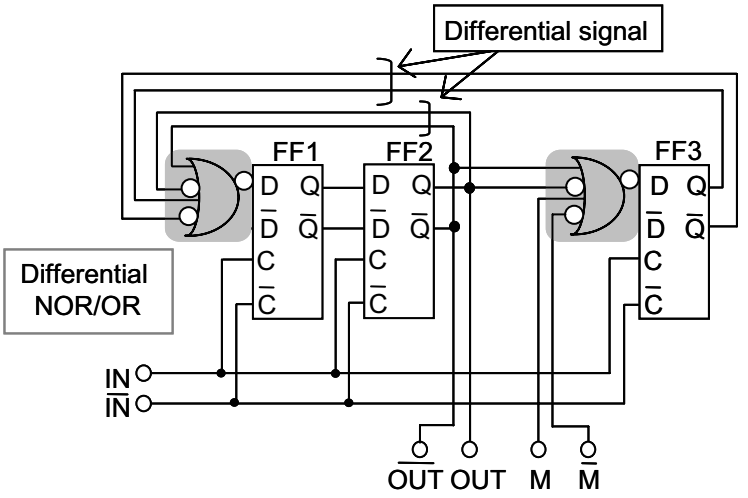


Fig. 7.4 Fully-differential dual-modulus prescaler.

The phase noise (Fig. 7.5) was measured in the phase-locking mode at an output frequency of 2.44 GHz. The loop bandwidth was designed to be about 10 kHz. The phase noise is about –104 dBc/Hz at an offset frequency of 1 MHz, which meets the Bluetooth specification, as indicated in the figure [7.4].

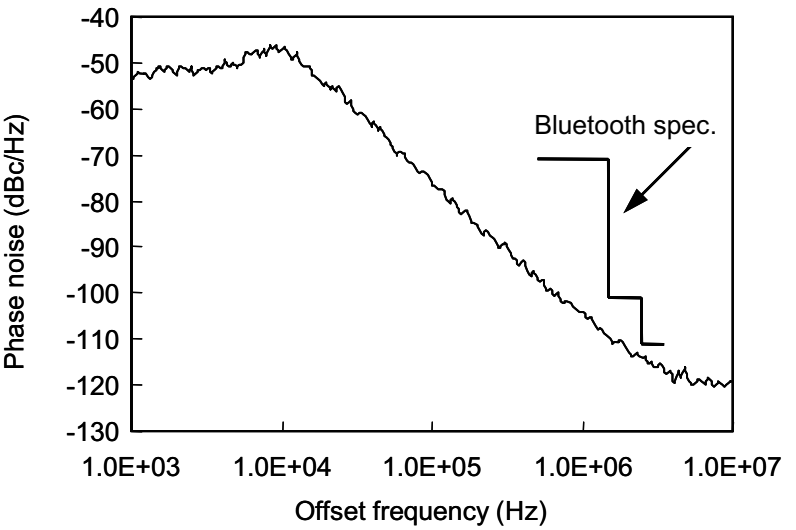


Fig. 7.5 Measured phase noise of PLL output.

C. Total performance

A prototype Bluetooth RF transceiver chip was fabricated on a fully depleted 0.2-μm CMOS/SOI process. Figure 7.6 shows the measured output eye diagram when the signal to the transmitter was modulated with a pseudorandom bit sequence. The transmitter outputs a power of -1 dBm; and the modulation index is about 160 kHz. Although the input baseband signal was a rectangular wave, the output waveform is smooth because of the on-chip Gaussian pulse-shaping filter.

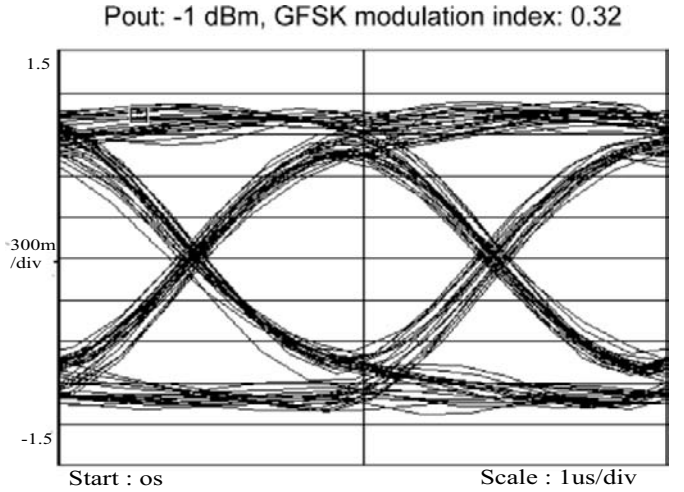


Fig. 7.6 Eye diagram of transmitter output signal.

The bit error rate (BER) (Fig. 7.7) was measured as a function of the input signal power of the receiver for 2.44-GHz RF input using external RF and channel-select filters. At a BER of 0.1%, the minimum detectable signal is about -77 dBm, which meets the Bluetooth specification of –70 dBm [7.4]. The LNA and IRM are designed to have moderate gains to meet the IIP3 requirement. This limits the noise figure of the receiver and thus its sensitivity. The BER is less than 10^{-6} when the signal level is larger than -65 dBm, and is less than 10^{-7} when the signal level is 0 dBm. Since an external channel-select filter is used, the maximum usable level is very high. In contrast, active filters cannot handle a high level because large signals cause current saturation, which limits circuit performance.

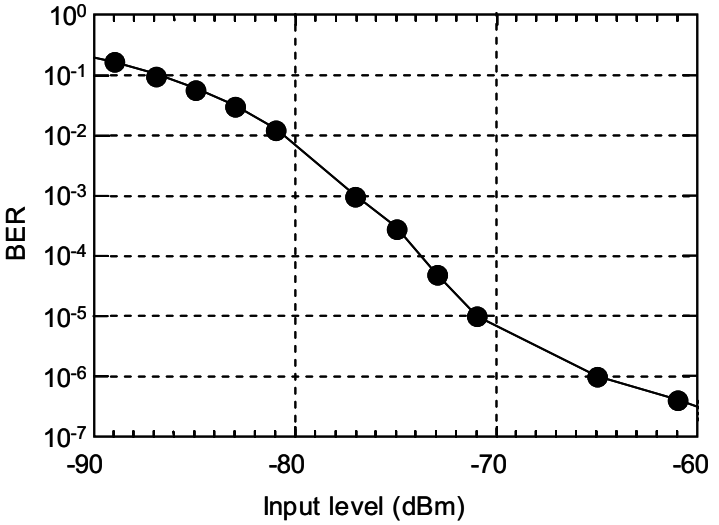


Fig. 7.7 Receiver sensitivity.

The chip (Fig. 7.8) is 5 mm × 5 mm in size. At a supply voltage of 1 V, the maximum power consumption is 33 mW in the transmit mode and 53 mW in the receive mode, yielding a time-averaged value of 43 mW.

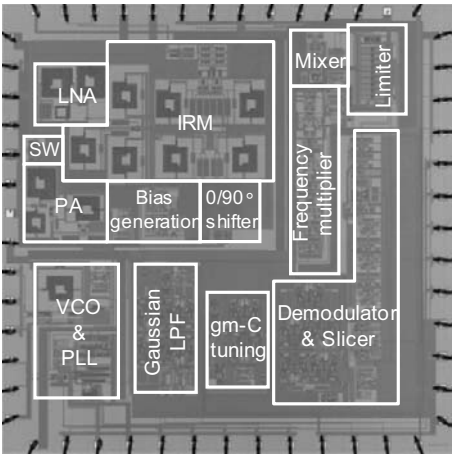


Fig. 7.8 Photomicrograph of 1-V Bluetooth transceiver.

7.2.2 Receiver

A bulky external SAW filter can be eliminated by including an active IF filter on the chip, thereby reducing the cost and size of an RF module. This section describes a 2.4-GHz CMOS/SOI FSK receiver with an integrated complex channel-select band-pass filter (BPF) that operates on a supply voltage of 1 V [7.5].

A. System architecture
In the receiver (Fig. 7.9), the quadrature mixer has an LC-tuned folded structure for low-voltage operation [7.1] [7.2]. The received signal is down-converted to a 2-MHz IF. The other RF circuits are almost the same as those of the Bluetooth transceiver. The complex channel-select BPF is a g_m-C type that suppresses the in-band image signal. The 2-MHz IF is fed to a limiting amplifier and then a frequency doubler. The frequency doubler doubles the frequency deviation of frequency modulation (FM) signals, which in turn doubles the modulation index. This improves the sensitivity of an FM demodulator. Since this receiver is a prototype, the chip does not contain a PLL synthesizer, an FM (FSK) demodulator, or the tuning circuit of the BPF.

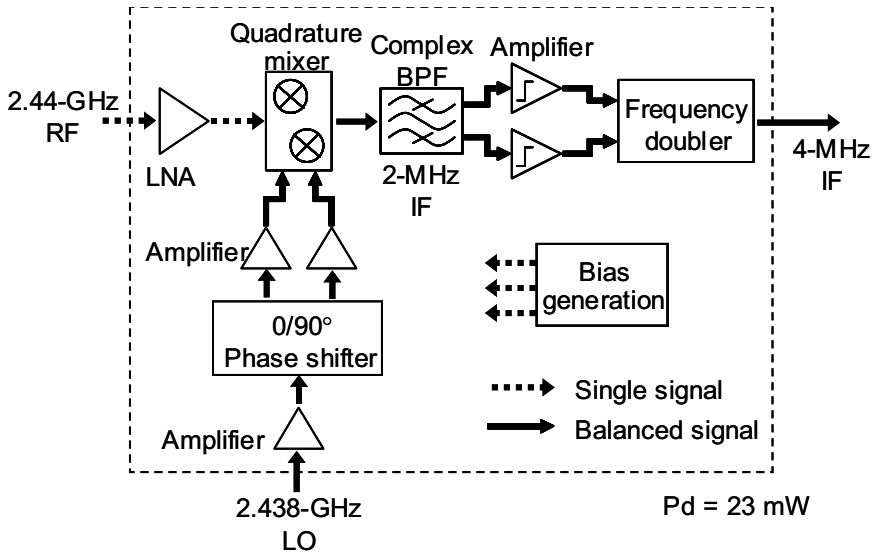
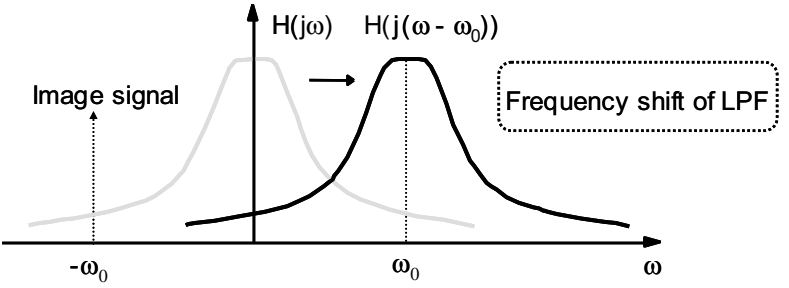


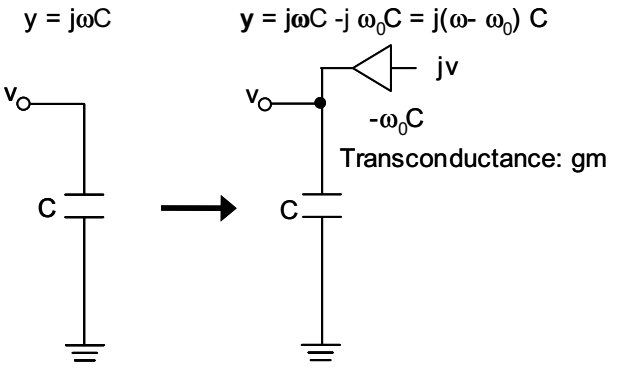
Fig. 7.9 Low-IF receiver with complex BPF.

B. Complex band-pass filter

The principle of a complex BPF is illustrated in Fig. 7.10 [7.6]. We begin with a low-pass filter ($H(j\omega)$), and asymmetrically shift the frequency using a quadrature signal and a g_m cell, which yields a complex filter ($H(j(\omega-\omega_0))$) and attenuation of the image signal in the negative frequency region. More specifically, the quadrature signal (jv) and the transconductance ($-\omega_0 C$) produce an equivalent frequency shift in the capacitive admittance ($j(\omega-\omega_0)C$). This type of filter is also called an active polyphase filter.



(a)



(b)

Fig. 7.10 Basics of complex BPF: (a) frequency shift of low-pass filter (LPF) and (b) circuit diagram.

Figure 7.11 shows the architecture of a complex BPF. Two fifth-order Butterworth low-pass filters with a bandwidth of 0.5 MHz are connected through g_m cells, which shift the center frequency of the filter response by about 2 MHz.

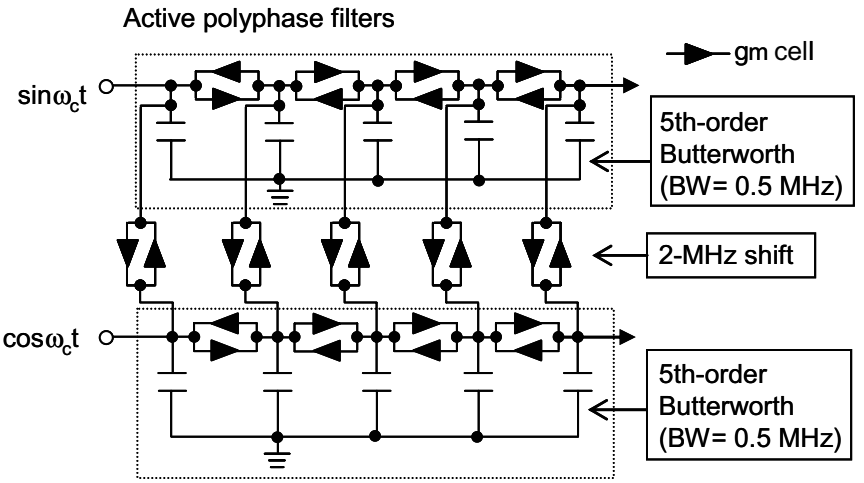


Fig. 7.11 Configuration of complex BPF.

The benefit a frequency doubler brings to FM demodulation (Fig. 7.12) is that, not only is the frequency doubled, the frequency deviation of FM signals is as well, which in turn doubles the modulation index. This improves the sensitivity of the FM demodulator by about 6 dB because the voltage swing at the demodulator output is approximately proportional to the modulation index [7.7]. On the other hand, the S/N degradation should be less than 6 dB, which should improve the sensitivity by *6 dB – Δ(S/N)*.

The frequency response of the receiver (Fig. 7.13) was measured at the output of the complex BPF with a 2.438-GHz LO. The gain is 33 dB and the image-rejection ratio is 36 dB, which meets the Bluetooth specification [7.4]. The gains of the LNA, the quadrature mixer, and the complex BPF are designed to be 17 dB, 4 dB, and 12 dB, respectively.

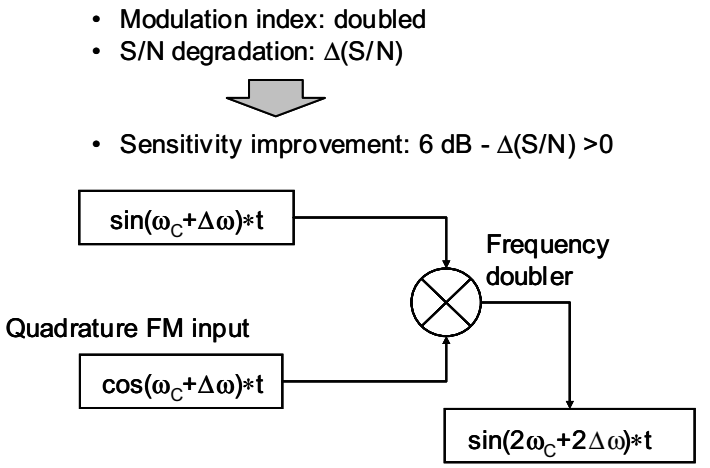


Fig. 7.12 Benefits of using frequency doubler.

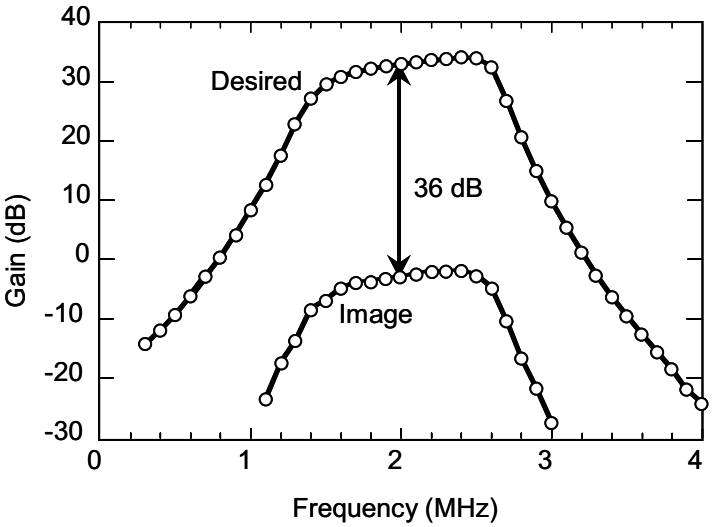


Fig. 7.13 Measured frequency response of 2.4-GHz CMOS/SOI FSK receiver.

C. Total performance

The BER (Fig. 7.14) was measured as a function of input signal power at the output of the frequency doubler and at the output of the complex BPF using an external demodulation IC (Motorola MC13055). The input was a 2.44-GHz signal GFSK modulated at 1 Mb/s. At a BER of 0.1%, the minimum detectable signal level is about –76.5 dBm at the output of the frequency doubler. This sensitivity meets the Bluetooth specification of –70 dBm [7.4]. The point is that the frequency doubler improves the BER performance by 2.2 dB at a BER of 0.1%, and by 3 dB at 0.001%. The power dissipation of the receiver is 23 mW at a supply voltage of 1 V.

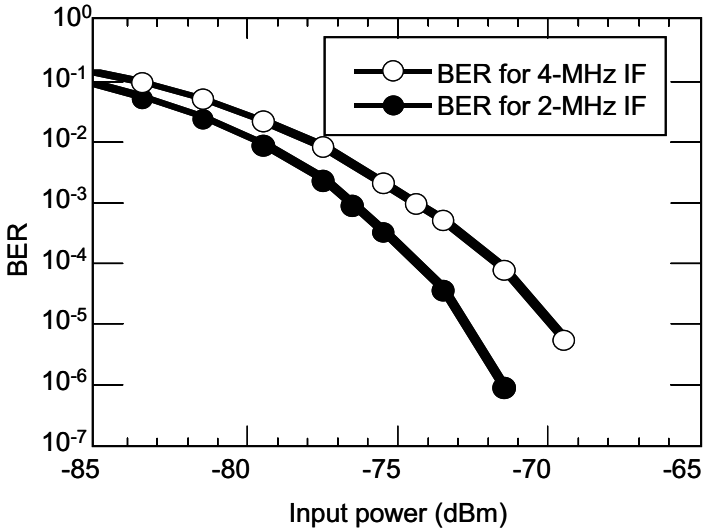


Fig. 7.14 Measured receiver sensitivity.

7.3 Solar-Powered, Radio-Controlled Watch

Consumers are always looking for fashionable wristwatches that unfailingly display the correct time and do not need any maintenance, such as the replacement of a battery. The solar-powered radio-controlled wristwatch was developed as a solution [7.8]. It receives time calibration radio signals that keep it accurate. The energy source is electric power generated by a solar panel and stored in a rechargeable battery.

Figure 7.15 shows the structure of a solar-powered wristwatch. The size depends on the size of the battery. To be fashionable, a watch must be thin; so the battery has to be small. And that means that the LSI in the watch cannot consume much power.

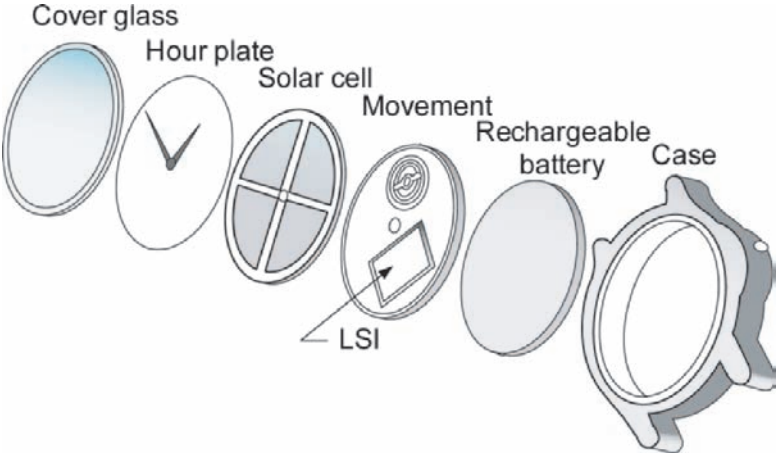


Fig. 7.15 Exploded view of solar-powered radio-controlled wristwatch.

Over the years, the current consumption of conventional bulk-CMOS LSIs for wristwatches has steadily decreased due to advances in circuit design, the use of a multiple-threshold-voltage CMOS scheme, and various layout techniques. However, we are approaching the limit of this technology and it is difficult to further reduce the power with bulk-CMOS devices.

The solution is to use fully-depleted silicon-on-insulator (FD-SOI) CMOS technology. This section describes a wristwatch LSI as one application of this technology.

(1) Configuration of conventional bulk-CMOS LSI
A conventional wristwatch LSI (Fig. 7.16) made on a bulk-CMOS process contains a RAM, a ROM, a CPU, and regulator circuits. The step-down circuit converts the 3 V supplied by the battery to 1.5 V; and this is further changed to 1.1 V and 0.7 V by voltage regulator circuits.

A crystal-oscillator circuit generates 32-kHz signals for time management, and the supply voltage is set to a low value of 0.7 V to reduce power consumption. This circuit operates continuously, and 0.7 V is the smallest voltage at which it can maintain oscillations.

The CPU, RAM, ROM, and step-up circuit (see Fig. 7.16) keep track of the time and control the movement of the watch hands based on signals from the crystal-oscillator circuit. The supply voltage of these circuits is set to 1.1 V so that they operate fast enough to wake up every second and process incoming time calibration signals. The processing takes only about 10 ms. Then, they go back to sleep when the processing is finished.

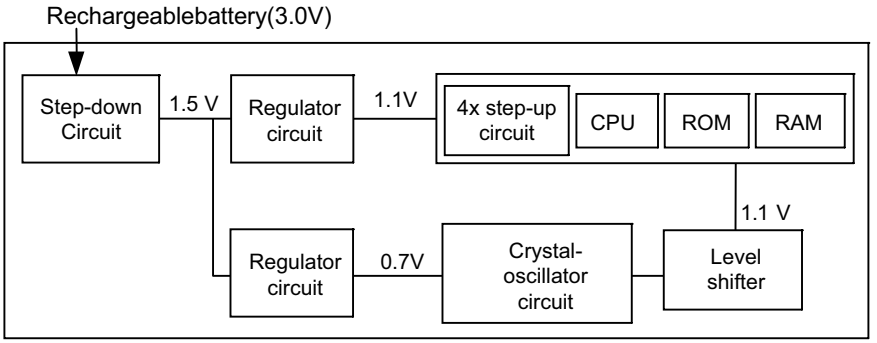


Fig. 7.16 Block diagram of watch LSI in bulk CMOS.

To suppress the power dissipation of this type of LSI, we need to reduce both the supply voltage and the threshold voltage of the MOSFETs in the digital circuits, such as the CPU, RAM, and ROM. But lowering the thereshold voltage causes an exponential increase in the leakage current. This increases the total power dissipation because the power dissipation of this LSI, which is usually in the sleep mode, is mainly determined by the standby current due to the leakage current of the MOSFETs. To suppress the leakage current, a new type of MOSFET that has a low threshold voltage and a small enough leakage

current is required.

(2) Advantages of FD-SOI MOSFETs

FD-SOI MOSFETs have several features that make them suitable for low-power LSIs [7.9]. One is that the junction capacitance is smaller than for bulk MOSFETs. The junction capacitance is proportional to the surface area of the junction, which is the sum of the areas of the horizontal and vertical surfaces of the source/drain diffusion layer. In an FD-SOI MOSFET, the planar capacitance is very small because the bottom of the diffusion layer rests on a thick oxide layer. So, the total capacitance is only about one-tenth that of a bulk MOSFET, as can be seen in the measured voltage dependence of the junction capacitance in Fig. 7.17.

As a result, the power consumption of an FD-SOI MOSFET is lower because the smaller total capacitance makes the charge/discharge current smaller.

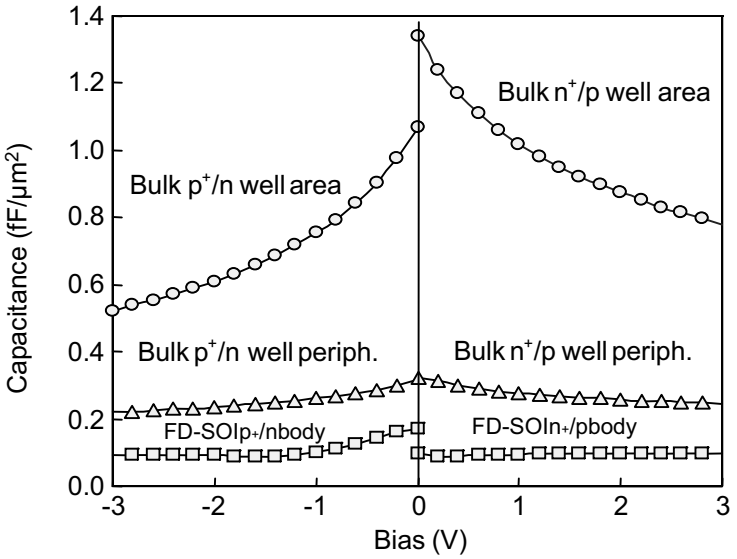


Fig. 7.17 Junction capacitances of bulk and FD-SOI MOSFETs.

For a given off-state leakage current, the threshold voltage of an FD-SOI MOSFET is lower than that of a bulk one (Fig. 7.18) because the subthreshold slope is steeper. Consequently, the power consumption can be reduced by lowering the supply voltage, which also helps to maintain performance.

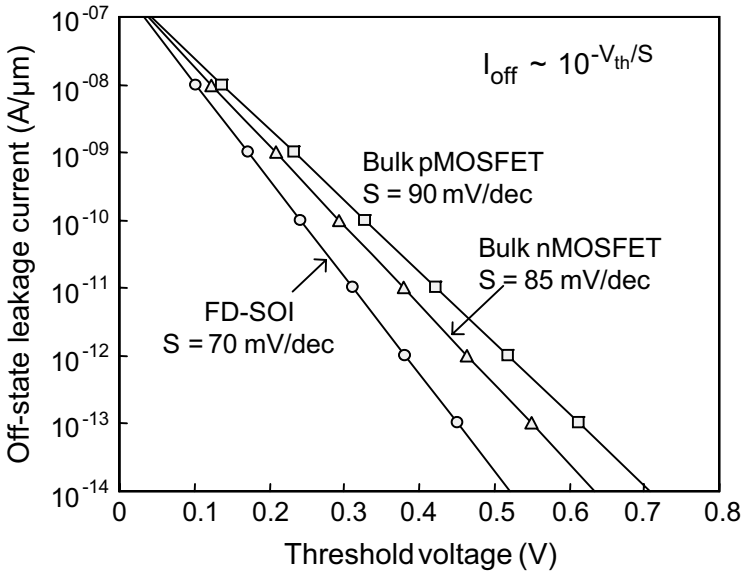


Fig. 7.18 Off-state leakage current vs. threshold voltage for bulk and FD-SOI MOSFETs.

(3) Watch LSI in FD-SOI CMOS

Figure 7.19 shows a block diagram of a wristwatch LSI made with FD-SOI CMOS devices. FD-SOI CMOS technology enables all the circuits to operate at a supply voltage of 0.7 V, which eliminates the regulator and level-shift circuits for 1.1 V that are needed in the bulk LSI.

In addition, it also enables the use of a low threshold voltage with no increase in standby current. So, this configuration reduces both the layout area and current consumption. Moreover, the power consumption is lower because the charge/discharge current is smaller due to the smaller total capacitance.

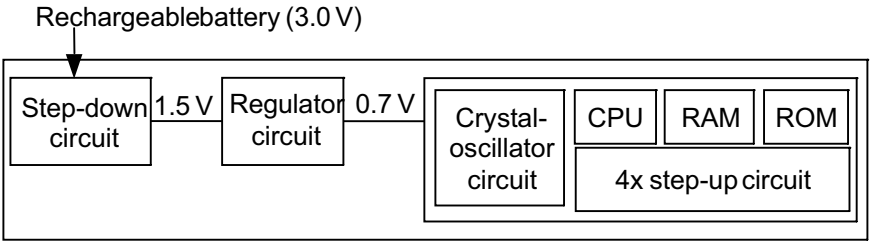


Fig. 7.19 Block diagram of wristwatch LSI in FD-SOI CMOS.

Figure 7.20 shows a photograph of a solar-powered radio-controlled watch [7.10] and a watch LSI [7.11] fabricated on a 0.35-μm FD-SOI CMOS process. This LSI consumes 40% less power than a bulk one.

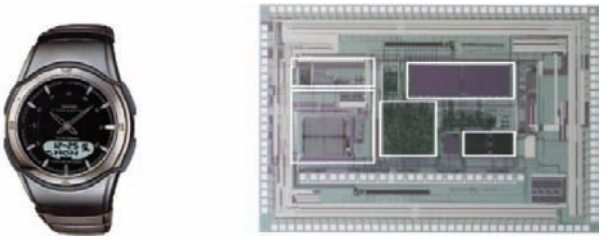


Fig. 7.20 Solar-powered radio-controlled watch and custom watch LSI.

7.4 Batteryless Short-Range Wireless System

A block diagram of a self-powered short-range wireless system [7.12] that operates on green-energy (GE) sources is shown in Fig. 7.21. The system consists of a transmitter and a receiver, and uses a 300-MHz-band low-power wireless transmission scheme [7.13].

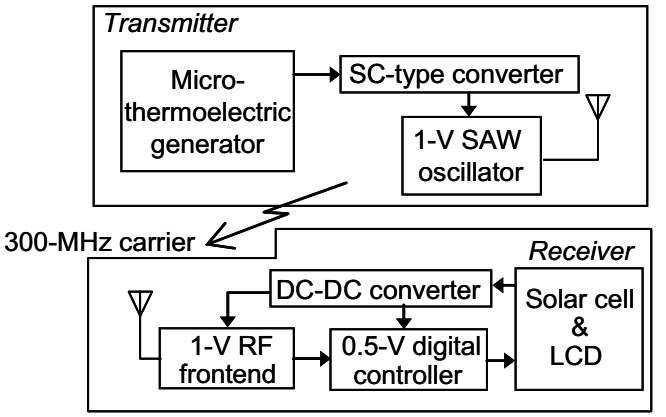


Fig. 7.21 Block diagram of self-powered short-range wireless system.

7.4.1 Transmitter

The transmitter consists of a switched-capacitor (SC)-type DC-DC converter and a SAW oscillator. The power source is either a thermoelectric (TE) generator or a micro-electric generator. The TE element in the micro-TE module [7.12] consists of two Bi-Te compounds and electrodes that are sandwiched between insulated metal plates to produce a temperature difference in each compound (Fig. 7.22).

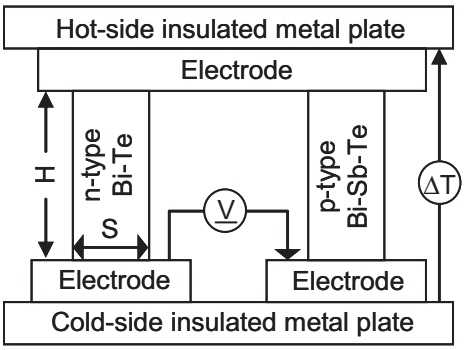


Fig. 7.22 Device structure of the TE generator.

A photograph of the micro-TE module is shown in Fig. 7.23. It contains 1200 TE elements.

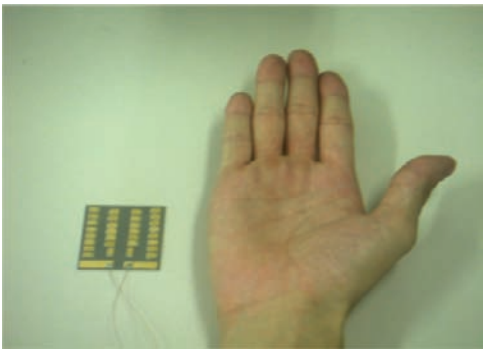


Fig. 7.23 Photograph of micro-TE module.

The TE-module generates a positive output voltage when the hot-side plate is warmed. The dependence of output voltage on the temperature difference between the hot- and the cold-side plates is shown in Fig. 7.24.

When the temperature difference is 5˚C, the module outputs 1 V without an output load, and generates a power of up to 1.25 mW. On the other hand, when the hot-side plate is cooled, it generates a negative voltage proportional to the temperature difference.

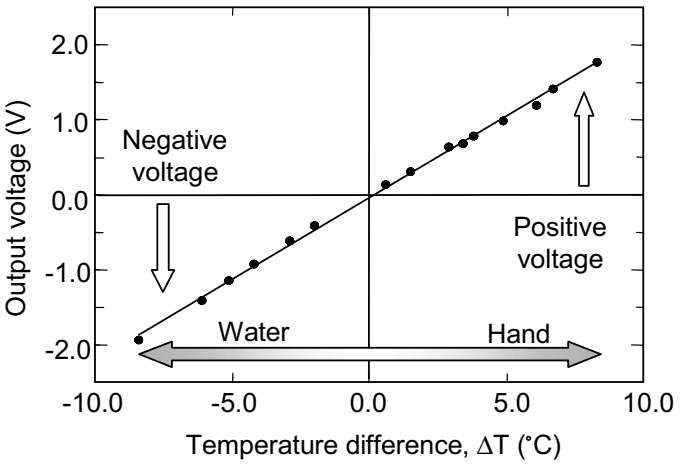


Fig. 7.24 Output characteristics of micro-thermoelectric (TE) generator.

An SC-type DC-DC converter (Fig. 7.25) was developed that operates with an electrical power source of either polarity [7.12]. It actually consists of two converters, one for a positive and one for a negative power source.

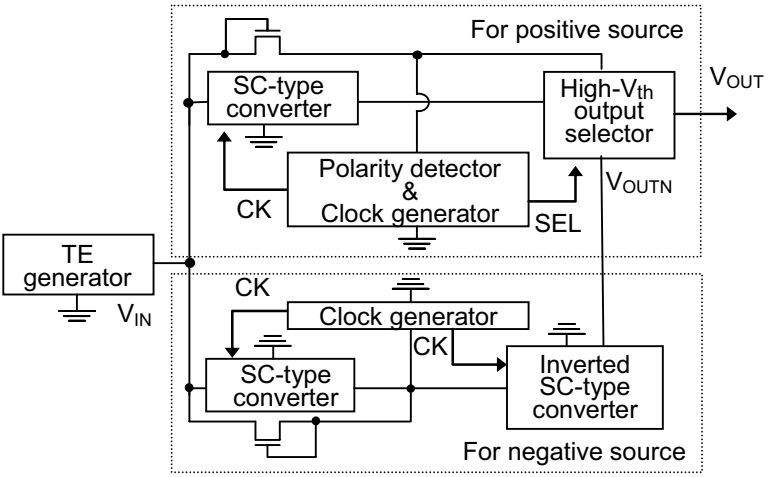


Fig. 7.25 Switched-capacitor-type DC-DC converter scheme for power sources of either polarity.

The inputs of the converters are directly connected in parallel. The converter outputs a positive supply voltage because the wireless system contains analog/RF circuits that are designed based on the ground level. An inverter function that inverts a negative supply voltage to a positive one is therefore added to the negative-power-source converter.

When a negative voltage is applied by the TE generator, the clock generator is activated first. The clock signal initiates a boosting operation by the converter. The inverted SC-type converter changes the boosted negative supply voltage to a positive output voltage (V_{OUTN}).

When a positive supply voltage is applied to the negative-power-source converter, the converter stops the boosting operation automatically without any increase in leakage current. Fully-depleted CMOS/SOI circuits make such operation possible.

The leakage current characteristics of FD-SOI and bulk CMOS inverters are compared in Fig. 7.26 for a negative supply voltage. For the bulk one, in which the body terminals of the MOSFETs are connected to the substrate or a well, the leakage current increases exponentially. In contrast, the FD-SOI circuit suppresses the leakage current because the body terminals of the MOSFETs float.

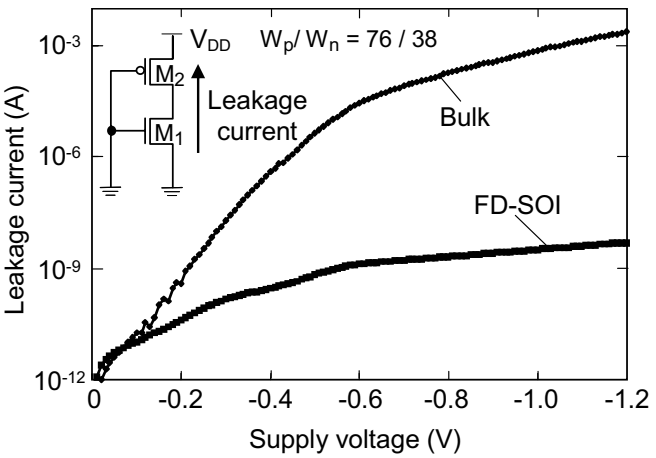
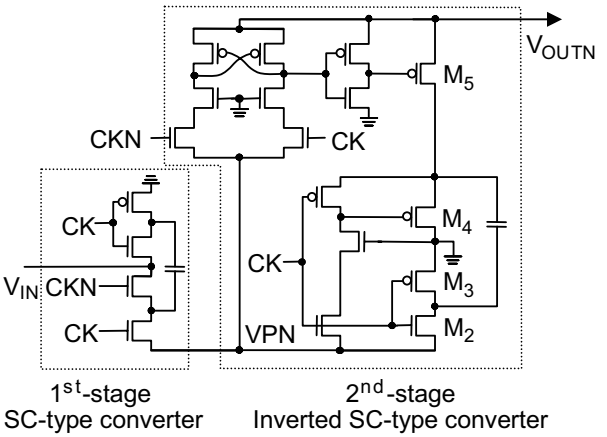
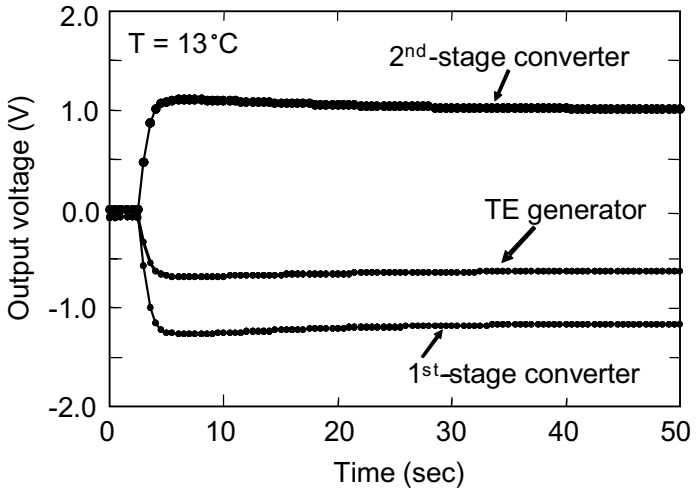


Fig. 7.26 Characteristics of FD-SOI an bulk CMOS inverters for negative supply voltage.

The circuit diagram of the SC-type DC-DC converter for a negative power source is shown in Fig. 7.27(a).



(a)



(b)

Fig. 7.27 SC-type DC-DC converter: (a) circuit diagram for negative power source and (b) output characteristics.

The first-stage converter boosts the output in the negative direction by a charge-pumping operation carried out by the four series-connected MOSFETs and a capacitor. Then, the inverted second-stage converter boosts the output to a positive voltage using these four MOSFETs and a capacitor. Since two MOSFETs, M4 and M5, need a positive voltage for a switching operation, the gates are controlled by the internal CMOS circuits, which have a level-shift circuit.

The output voltage characteristics of the negative-source converter are shown in Fig. 7.27(b). The hot-side plate of the generator was cooled with water to 13˚C. The output load of the converter was 1 kΩ. The generator supplies a power of up to 1.6 mW and outputs about -0.7 V. Each stage of the converter boosts the input voltage, with the final output being almost exactly 1 V.

The SC-type DC-DC converter supplies a constant power to the 1-V SAW oscillator. FD-SOI devices make it possible to produce a 300-MHz signal with a power consumption of less than 1 mW. The RF output power level is about –33 dBm for a 50-Ω load at a supply voltage of 1 V. At 1 V, the current consumption is 800 μA [7.13], and the output power level is in compliance with the regulations for a 300-MHz-band unlicensed radio system.

7.4.2 Receiver

The receiver consists of an RF front-end circuit block, a digital controller operating on 0.5 V, and an LCD. The power source is a solar cell. The RF front-end circuit block detects the 300-MHz carrier and outputs the detected signal in a binary format. The digital controller receives the continuous detected signal for 0.8 second and then displays a fixed message on the LCD.

A photograph of the digital controller on a board is shown in Fig. 7.28. The board is 5 cm x 14 cm in size. It consists of an 8-bit CPU, a 256-kbit SRAM, a 256-kbit ROM, and an SC-type down-converter. All the LSIs are composed of fully-depleted MTCMOS/SOI circuits and operate on the 0.5 V from the down-converter. By lowering the supply voltage to 0.5 V, a power dissipation of about 1 mW was obtained at an operating frequency of 10 MHz.

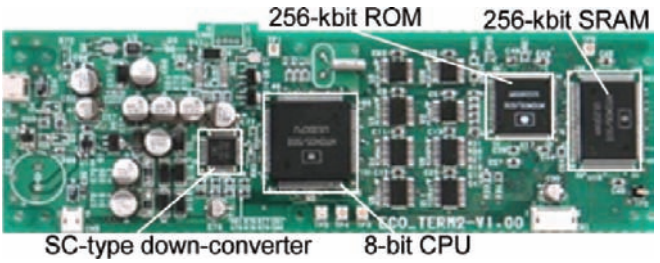


Fig. 7.28 Photograph of 0.5-V digital controller in the receiver circuit.

A self-powered wireless system composed of the transmitter and the receiver is shown in Fig. 7.29. When something is placed on the transmitter, it generates power and transmits data. The receiver detects the wireless signal and displays the data on an LCD. The transmitter operates on only the heat from a hand or the cooling effect of cold water. Since the thermoelectric generator instantaneously generates a high power, the transmitter also functions as a sensor in this application. For the receiver, a solar cell that continuously generates a constant level of power is required because the receiver must always be ready to detect a signal. Tests showed that data could be transmitted wirelessly over a distance of 5 m without a battery.

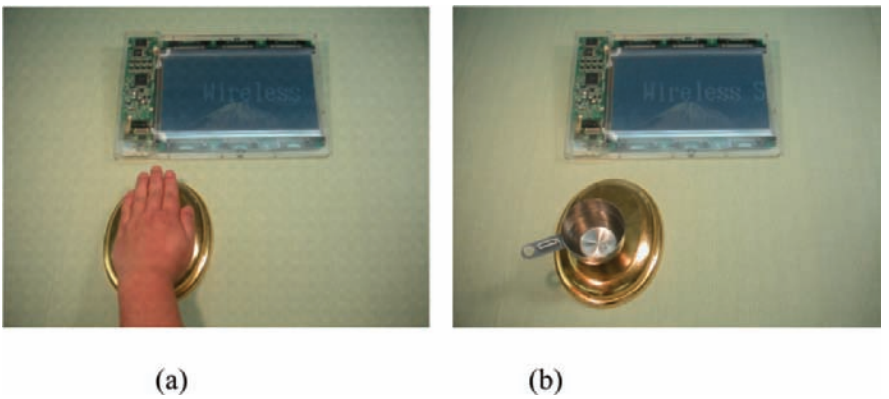


Fig. 7.29 Self-powered short-range wireless system using ambient heat.

Two other applications of the self-powered short-range wireless system [7.14] are shown in Fig. 7.30. The one on the left is a hanger-type transmitter that is driven by the weight of hanging clothes. And the one on the right is a pen-type transmitter driven by the movement of an internal weight when the pen is shaken. In both cases, the development of a 1-mW-level transmitter and a micropower generator makes batteryless operation possible.

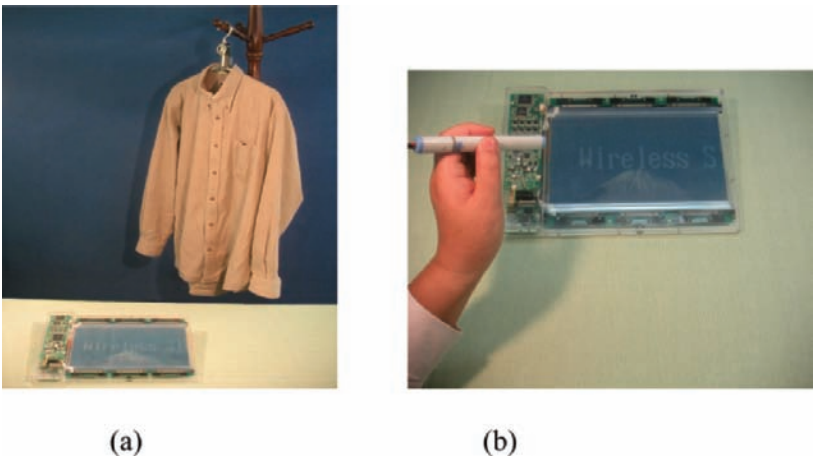


Fig. 7.30 Other applications of self-powered short-range wireless system: (a) hanger-type transmitter and (b) pen-type transmitter.

The key features of the wireless system are:

Transmitter	
Power source	Thermoelectric generator
Power dissipation	1 mW
TX frequency	312 MHz, CW
Output power level	-33 dBm
Receiver	
Power source	Solar cell
Power dissipation	40 mW

7.5 Summary

This chapter described three ultralow-voltage wireless systems based on MTCMOS/SOI circuits, which are mainly made with FD-SOI MOSFETs.

1. Bluetooth RF transmitter and receiver system:
Fabricating all the RF components with FD-SOI MOSFETs makes it possible to reduce the supply voltage down to 1 V. This ultralow-power 2-GHz-band short-range wireless system with an average power dissipation of less than 40 mW was the first demonstration of a CMOS radio system.

2. Longwave-radio-controlled watch system:
All the electrical components (such as the receiver and digital controller, but not the LCD)) are made with FD-SOI MOSFETs. The supply voltage is 0.7 V, and the power consumption is on the 10-μW level. This makes self-powered operation possible using a solar cell.

3. 300-MHz-band short-range wireless system:
A 1-V SAW oscillator, a switched-capacitor-type DC-DC converter and a 0.5-V digital controller were designed based on the MTCMOS/SOI circuit scheme. The system operates on just the energy from ambient sources, such as the light, kinetic, and thermal sources around us.

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Chapter 8

PROSPECTS FOR FD-SOI TECHNOLOGY

8.1 Introduction

FD-SOI technology is a promising way of fabricating low-power devices with the advantages of a steep subthreshold slope, a low junction leakage, and a low junction capacitance. There is now a great need for FD-SOI devices with a gate length of less than 100 nm because scaling down Si MOSFETs is the best way to lower power consumption. However, serious issues arise in devices with such a small gate length, such as short-channel effects, the need to adjust the threshold voltage, and the steepness of the subthreshold slope. To find the best way to achieve higher performance, new device designs and future trends in FD-SOI MOSFETs must be discussed.

This chapter first describes structures for nano-scale FD-SOI devices and future trends. Next, device and substrate technologies for ultrathin FD-SOI MOSFETs with a gate length below 100 nm are considered. Finally, power-aware electronics and the potential of FD-SOI devices to provide a solution are discussed.

8.2 Evolution of Nanoscale FD-SOI Devices

The scaling down of MOS devices for VLSIs has been going on for more than 30 years in the ceaseless effort to achieve higher performance and higher levels of integration. The gate length is now less than 50 nm at the production level and sub-10-nm devices have been reported at the research level [8.1]-[8.3]. In short, silicon MOSFETs have already entered the nanoscale regime. However, since it is very difficult to scale down a conventional single-gate MOSFET to the extent required, there is a need for new device structures for nanoscale integrated circuits. Innovative structures based on FD-SOI technology will certainly make a significant contribution to advances in device miniaturization and to the enhancement of device performance.

These new devices are generally called "non-classical CMOS". The International Technology Roadmap for Semiconductors (ITRS) [8.4] describes them as "a path to scaling down CMOS to the end of the roadmap using new structural designs and new materials for transistors." Some of these devices are already being touted as mainstream technologies for the 45-nm technology node and beyond.

The main challenges we face in the further miniaturization of MOSFETs are:

1. Increasing the saturation current while reducing the power supply.
2. Reducing leakage current and short-channel effects.
3. Achieving uniform device parameters across a chip and from chip to chip.

To meet these challenges, the ITRS offers two approaches leading to non-classical CMOS: (1) the development of new materials with better carrier transport properties and (2) the creation of new transistor structures with improved electrostatics.

Figure 8.1 illustrates the structural evolution of FD-SOI MOSFETs. Starting from the basic single-gate structure, innovation has led to the emergence of double-gate [8.5], triple-gate [8.6], and gate-all-around structures [8.7]. A device with two or more gates is called a multigate device. Increasing the number of gates boosts device performance and immunity to short-channel effects due to the stronger electrostatic control of the channel by the gate. The drawback is that the fabrication process becomes more complicated because of the three-dimensional nature of the structure. There are three versions of the double-gate type: planar, vertical, and FinFET, with the direction of electron

transport being different in each [8.5]. There are also two versions of the gate-all-around type.

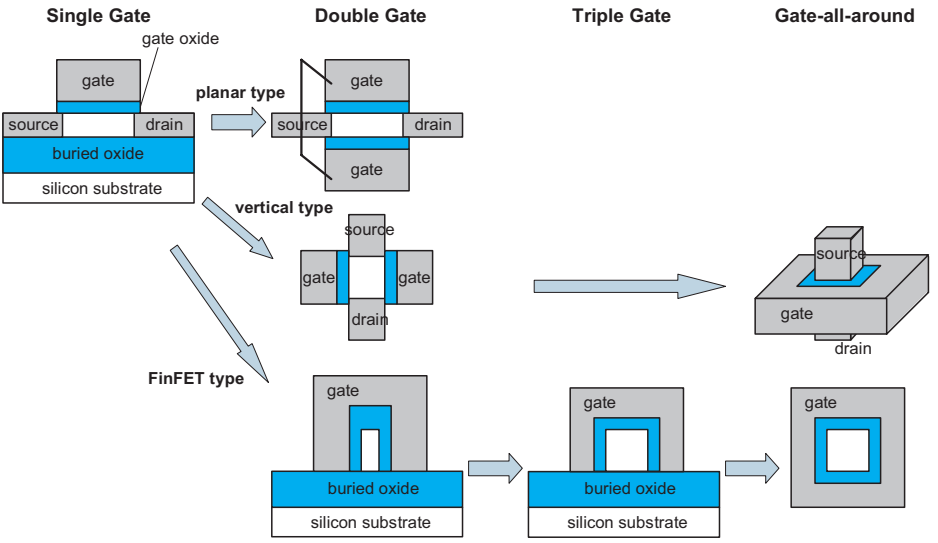


Fig. 8.1 Evolution of FD-SOI devices from single-gate to multigate structures.

The subthreshold swings of single-, double-, and triple-gate FD-SOI MOSFETs were simulated as a function of gate length (Fig. 8.2) to compare the short-channel effects [8.8] [8.9]. The thickness of the SOI layer was assumed to be the same for the three devices. The single-gate device has severe short-channel effects because the gate does not adequately control the potential. The gate length must be more than about 4 times the thickness of the SOI layer to suppress these effects. On the other hand, the double- and triple-gate MOSFETs have much smaller short-channel effects; so, the gate length can be about twice the thickness of the SOI layer. Moreover, the triple-gate device has slightly better characteristics than the double-gate one because the three gates provide stronger control of the channel potential.

Generally speaking, the fabrication processes for planar double-gate and gate-all-around devices are very complicated. In contrast, the FinFET type can be fabricated on a semi-planar process that is not complicated. So, FinFET double-gate and triple-gate devices are considered to be the most promising designs for the nanoscale regime. In fact, among the sub-10-nm MOSFETs already reported, the FinFET type exhibits the smallest short-channel effects and the best performance [8.3].

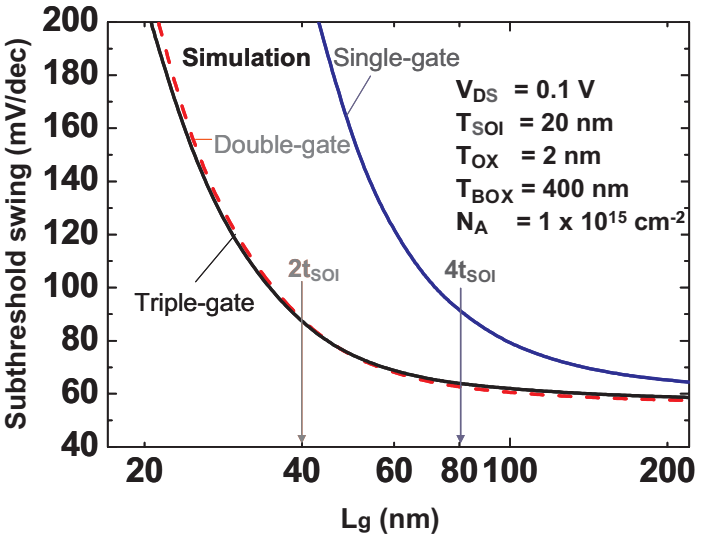


Fig. 8.2 Simulated subthreshold swing of single-, double-, and triple-gate MOSFETs as a function of gate length.

However, although the FinFET type solves the problems of leakage and short-channel effects, the other challenges listed above must also be addressed. Strained-silicon technology, including the use of biaxial strain in a SiGe layer [8.10] and uniaxial strain from process-induced stress [8.11], is one of the most effective methods of enhancing the saturation current. Moreover, the key to reducing parameter variations both on a chip and from chip to chip is the use of a back-gate bias to control the threshold voltage after chip fabrication [8.9]. Multigate FD-SOI technology must be combined with these technologies to meet all the challenges in the nanoscale regime.

Figure 8.3 shows the evolution of non-classical CMOS in the nanoscale regime [8.12]. Strained-silicon technology, FD-SOI multigate device technology, and back-gate bias control technology must be combined. They improve carrier transport, suppress short-channel effects, and provide parameter control after chip fabrication, respectively. At present, the combination of the first two technologies is being pursued. Strained-SOI [8.10] and process-induced strained-SOI devices [8.13] have already been reported. A more complicated combination—three-dimensional strained multigate MOSFETs—has also been reported [8.14]. In addition, back-gate bias control technology has been applied to the design of FD-SOI MOSFETs [8.15] [8.16].

Although these technologies can be combined in many ways, the combination of all three, leading to a threshold-voltage-controllable three-dimensional FD-SOI multigate MOSFET, will ultimately be needed for nanoscale integrated circuits of the future.

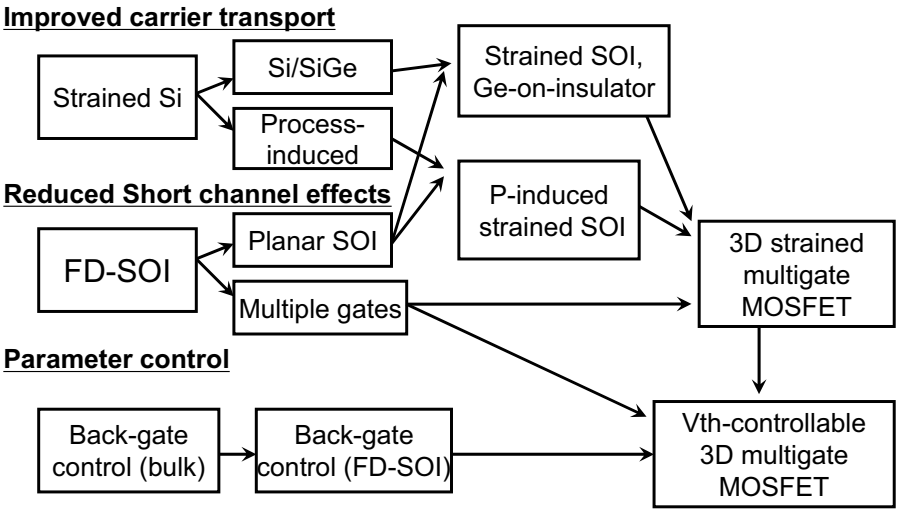


Fig. 8.3 To meet the three challenges in the nanoscale regime, non-classical CMOS will evolve through the combination of strained-silicon technology, FD-SOI multigate-device technology, and back-gate bias control technology.

8.3 Device and Substrate Technologies for Ultrathin-Body SOI MOSFETs

8.3.1 Ultrathin-Body SOI MOSFETs

A. Introduction

MOSFETs fabricated on a silicon-on-insulator (SOI) substrate with an extremely thin SOI layer have attracted a great deal of attention, in part because of their better immunity to short-channel effects. To enhance this immunity, the thickness of the SOI layer should be from about one-third to one-fourth the gate length. For instance, it should be 5-6 nm when the gate length is 20 nm. When the SOI layer is 10 nm thick or less, the device is called an ultrathin-body SOI MOSFET. On the other hand, the envelope function of the inversion-layer electrons in bulk MOSFETs has a width of approximately 10-20 nm. As a result, electrons in an ultrathin (5-6 nm) SOI layer are strongly confined by the gate oxide (GOX) and the buried oxide (BOX), thus bringing quantum mechanical effects into play.

This chapter concerns the low-field electron mobility of ultrathin-body SOI MOSFETs. This is one of the most important physical properties determining the performance of MOSFETs, including decanano- and nano-scale MOSFETs, since a higher mobility yields both greater velocity overshoot [8.17] and a higher injection velocity [8.18]. Section B is a theoretical discussion of how the thickness of the SOI layer (T_{SOI}) affects the electron mobility of SOI MOSFETs.

It is shown that, as the SOI layer becomes thinner,
1. electron mobility decreases when 5 nm < T_{SOI} < 20 nm;
2. electron mobility increases when 3 nm < T_{SOI} < 5 nm ; and
3. electron mobility again decreases when T_{SOI} < 3 nm.

Section C discusses a new scattering mechanism arising from variations in the thickness of the SOI layer. It is peculiar to SOI MOSFETs with an extremely thin SOI layer and is caused by quantum confinement effects.

B. Electron mobility of ultrathin-body SOI MOSFETs

First, the energy levels of the 2-dimensional (2D) electron system of the inversion layer at the surface of a bulk (100) Si MOSFET is discussed. There are two types of subbands in the inversion layer at a (100) surface: 2-fold valleys at the center of 2D k-space, and 4-fold valleys along the k_x and k_y axes. Figure 8.4 illustrates the main features of the subbands, with the ellipses indicating a constant energy. The lower conductivity mass of electrons in the 2-fold valleys yields both higher mobility and also a higher effective mass perpendicular to the Si/SiO_2 interface, which results in a thinner inversion layer, a narrower electron envelope function, and a lower subband energy. The situation is the opposite for the 4-fold valleys: the inversion layer is thicker, the electron envelope function is broader, and the subband energy is higher. As a result, electrons tend to occupy the 2-fold valleys, which enhances overall mobility because the mobility of a Si MOSFET is determined by the average of the mobilities of the 2- and 4-fold valleys weighted by the electron occupancy of each.

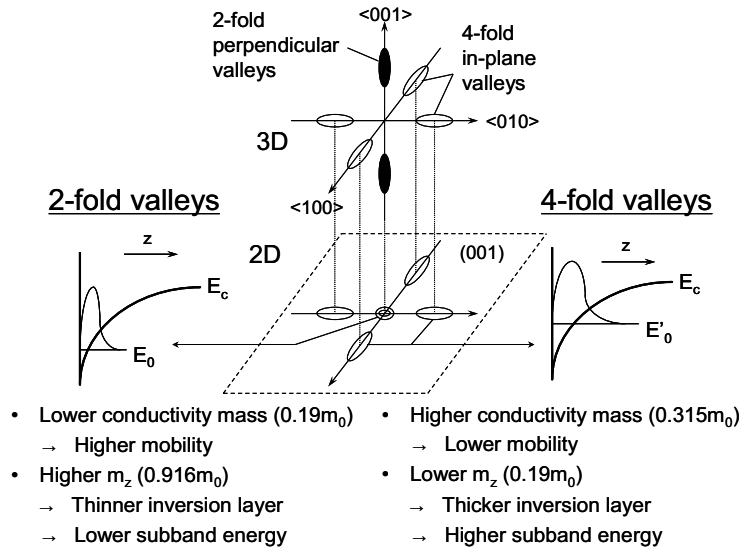


Fig. 8.4 Subband structure of Si MOS interfaces.

Unfortunately, in bulk-Si MOSFETs, the occupancy of the 2-fold valleys is not very high because the difference between the lowest subband energy of the 2-fold valleys (E_0) and that of the 4-fold valleys (E'_0) ($\Delta E_0 = E'_0 - E_0$) is small and the density of states of the 4-fold valleys is larger than that of the 2-fold valleys (Fig. 8.5). Consequently, the electron mobility of bulk-Si MOSFETs is smaller than that for the 2-fold valleys. This means that, if ΔE_0 can intentionally be raised, the inversion layer mobility will be enhanced because more electrons will occupy the 2-fold valleys.

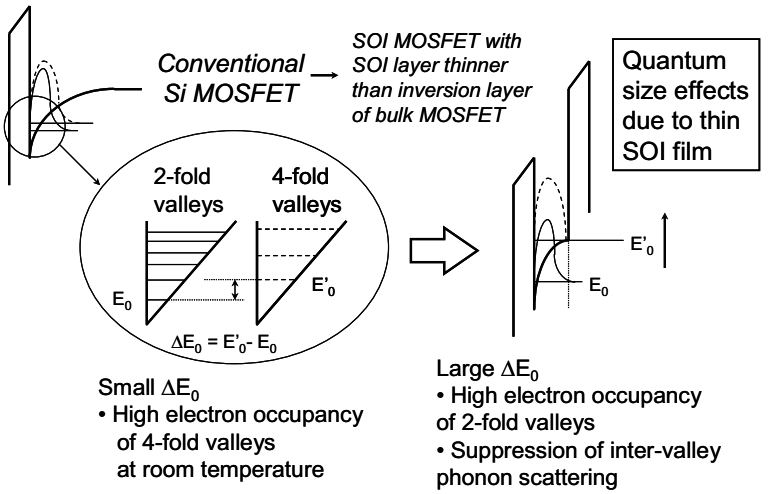


Fig. 8.5 Band structures of (left) bulk MOSFET and (right) SOI MOSFET with an SOI layer that is thinner than the inversion layer of the bulk MOSFET. Quantum size effects in the SOI layer modulate the subbands.

One way to increase ΔE_0 is to exploit the quantum size effects that occur in ultrathin-body SOI MOSFETs (Fig. 8.5). Given that the SOI layer is thinner than the inversion layer of a bulk MOSFET, as T_{SOI} decreases, the subband energy levels of the 4-fold valleys should increase more rapidly than those of the 2-fold valleys because the 4-fold valleys have a broader envelope function. As a result, ΔE_0 should increase. This modulation of the subband structure by means of quantum size effects in an ultrathin SOI film should lead to a higher occupancy of the 2-fold valleys, and thus a higher total mobility. In the

discussion below, the inversion layer mobility of SOI MOSFETs is analyzed theoretically based on subband calculations to determine whether the above supposition is valid or not.

The 2D subband structure of an SOI MOSFET was determined from self-consistent calculations [8.19] [8.20] [8.21], in which Poisson's and Schrodinger's equations are solved self-consistently for an ideal SOI structure. The SOI layer was assumed to have a uniform thickness and no interface roughness. The effects of interface roughness and variations in the thickness are discussed in Section C. Calculations were made for 20 subbands (10 each for the 2- and 4-fold valleys) so as to accurately describe the electron occupancy of subbands in the inversion layer at room temperature.

Regarding the scattering mechanism, only phonon scattering was taken into account because it the main type affecting the mobility of bulk-Si MOSFETs at room temperature and is an intrinsic scattering mechanism. The inversion layer mobility was calculated using a relaxation time approximation [8.20]. A low substrate impurity concentration of 5×10^{15} cm^{-3} was used for both bulk and SOI MOSFETs so that the effect of the thickness of the SOI layer could be isolated. The temperature was assumed to be room temperature, and the thickness of the SOI layer ranged from 20 nm down to 2 nm.

Fig. 8.6 shows graphs of calculated mobility versus the strength of the effective normal field, E_{eff}, with the thickness of the SOI layer (T_{SOI}) as a parameter. The mobility of bulk MOSFETs is also indicated by the open circles for comparison. For SOI MOSFETs, mobility has a complicated dependence on T_{SOI}:

1. When 5 nm < T_{SOI} < 20 nm, the mobility decreases as T_{SOI} decreases, particularly when E_{eff} is low.
2. When 3 nm < T_{SOI} < 5 nm, the mobility increases as T_{SOI} decreases. An important point is that the mobility for a T_{SOI} of around 3 nm is higher than the mobility of bulk MOSFETs when E_{ff} has a moderate or high value. In addition, the dependence of mobility on E_{eff} becomes weaker as T_{SOI} decreases.
3. When 2 nm < T_{SOI} < 3 nm, the mobility decreases as T_{SOI} decreases.

The physical origins of this complicated T_{SOI} dependence and the enhanced mobility of ultrathin-body SOI MOSFETs is analyzed below.

In order to understand the T_{SOI} dependence, two factors need to be considered: one is the change in the subband energy difference between the 2- and 4-fold valleys (ΔE_0) due to quantum size effects; and the other is the dependence of the inversion layer mobility on inversion layer thickness. As mentioned above, increasing ΔE_0 should raise the occupancy of the 2-fold valleys, resulting in higher mobility. In addition, it should also help to suppress inter-valley phonon scattering from the 2-fold to the 4-fold valleys, as has been reported to occur in strained-Si MOSFETs [8.20] [8.22], which suggests that it should further increase the inversion layer mobility. In short, as TSOI decreases, the mobility of SOI MOSFETs should increase because ΔE_0 becomes greater.

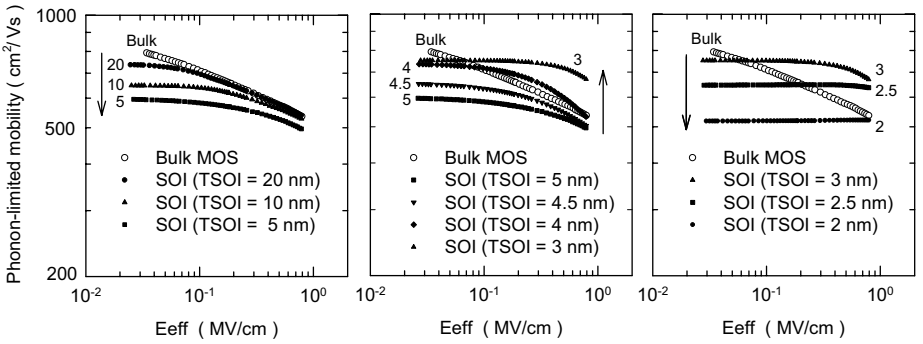


Fig. 8.6 Calculated phonon-limited mobility of bulk MOSFET and SOI MOSFET for 2 nm ≤ T_{SOI} ≤ 20 nm.

On the other hand, the phonon-limited mobility of the inversion layer becomes smaller as the thickness (W) of the inversion layer decreases [8.23] [8.24]. If we assume that only a single subband is occupied, the mobility limited by intra-valley acoustic phonon scattering for the 2DEG is approximately given by [8.23] [8.24]

$$\mu_{ac} = \frac{q}{m_c} \cdot \frac{\hbar^3 \rho s_l^2}{m_d n_v D_{ac} k_B T} \cdot W, \tag{8.1}$$

where

$$W = \left(\int |\varphi(x)|^4 dx \right)^{-1}$$

$$\approx \left(\frac{256 \varepsilon_{Si} \hbar^2}{81 m_z q^2} \right)^{1/3} \left(N_{dpl} + \frac{11}{32} N_s \right)^{-1/3} \propto E_{eff}^{-1/3}, \tag{8.2}$$

m_c: Conductivity mass
m_d: Density-of-states mass
n_v: Valley degeneracy
D_{ac}: Deformation potential of acoustic phonons
s_l: Velocity of sound
W: Effective thickness of inversion layer
$\varphi(x)$: Envelope function of 2DEG
ε_{Si}: Permittivity of Si
m_z: Effective mass perpendicular to Si/SiO_2 interface
N_{dpl}: Concentration of space charges at surface
N_s: Carrier concentration at surface.

Thus, the mobility of the inversion layer is proportional to its thickness. This relationship comes from the fact that, as electrons become more spatially confined, the frequency bandwidth of phonons that can couple with the 2DEG becomes larger, thereby reducing the mobility limited by intra-valley phonon scattering. That is, when the SOI film is thinner than the inversion layer of a bulk MOSFET, this mechanism causes the mobility of an SOI MOSFET to decreases as T_{SOI} decreases because the inversion layer thickness is limited by T_{SOI}, as shown later. In short, as T_{SOI} decreases, the greater ΔE_0 and the thinner inversion layer have opposite effects on inversion layer mobility, leading to the complicated behavior described above.

The calculated dependence of mobility on T_{SOI} can be understood by looking at how the subband structure changes as T_{SOI} decreases (Fig. 8.7):

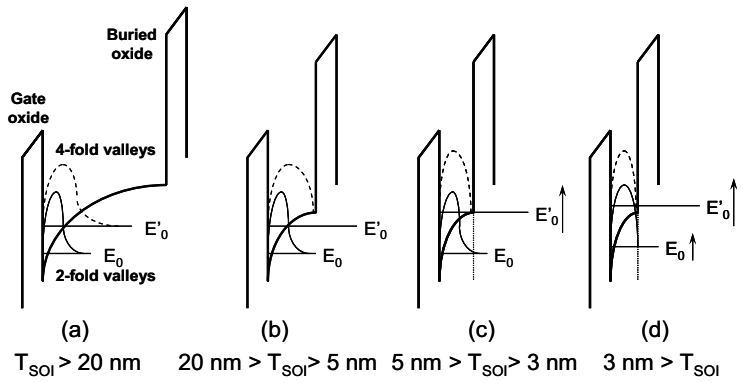


Fig. 8.7 Change in band structure of SOI MOSFET as SOI layer becomes thinner.

(a) When $T_{SOI} > 20$ nm, SOI and bulk MOSFETs have the same subband structure, and thus the same inversion layer mobility.

(b) When $5 \text{ nm} < T_{SOI} < 20$ nm, the thickness of the SOI layer physically limits the extent of the electron envelope function, particularly in the 4-fold valleys. This, in turn, limits the inversion layer thickness, and thus the total mobility.

(c) When $3 \text{ nm} < T_{SOI} < 5$ nm, the subband energy levels of the 4-fold valleys are raised more rapidly than those of the 2-fold valleys because of quantum size effects in an ultrathin SOI film. Since the inversion layer is broader for the 4-fold than for the 2-fold valleys, quantum size effects appear first in the 4-fold valleys. This raises the electron occupancy of the 2-fold valleys, thereby increasing the total mobility. In addition, the suppression of inter-valley phonon scattering, which increases ΔE_0, also contributes to a higher mobility [8.20] [8.22].

(d) However, when $T_{SOI} < 3$ nm, almost all the electrons already occupy the 2-fold valleys and the inversion layer thickness for the 2-fold valleys is also physically limited by the thickness of the SOI layer. This causes the mobility to decrease as T_{SOI} becomes smaller.

The electron mobility for the 2- and 4-fold valleys (Fig. 8.8), which means the mobility averaged over the subbands of these valleys, was calculated for an Eeff of 0.26 MV/cm ($N_s = 3 \times 10^{12}$ cm^{-2}) as a function of T_{SOI}. For the 4-fold valleys, it decreases monotonically as T_{SOI} becomes smaller. For the 2-fold valleys, the behavior is more complicated: As T_{SOI} becomes smaller, the mobility falls somewhat in the range 5 nm < T_{SOI} < 20 nm, rises to a peak at around T_{SOI} = 3 nm, and then drops sharply in the range 2 nm < T_{SOI} < 3 nm.

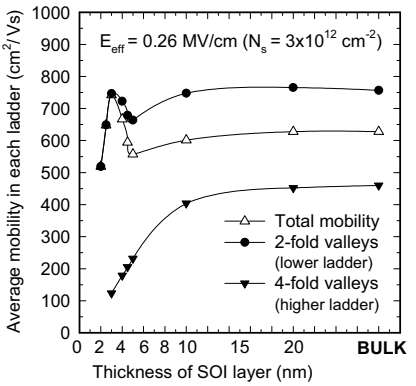


Fig. 8.8 Calculated electron mobility for 2- and 4-fold valleys, and total mobility. The lower and higher ladders correspond to 2-fold and 4-fold valleys.

The decreasing mobility for both types of valleys as T_{SOI} becomes smaller is explained by the dependence of inversion layer mobility on inversion layer thickness in Eq. (8.1). In particular, when T_{SOI} < 3 nm, the thickness of the SOI layer directly determines the extent of the envelope function, and thus the inversion layer thickness, as shown later. As a result, the mobility drops rapidly as T_{SOI} becomes smaller. On the other hand, the higher mobility for the 2-fold valleys around a T_{SOI} of 3 nm is attributable to the suppression of inter-valley phonon scattering. It has been reported that the suppression of inter-valley phonon scattering associated with band splitting between the 2- and 4-fold valleys due to tensile strain significantly enhances the mobility of strained-Si MOSFETs fabricated on a SiGe substrate [8.20] [8.22].

When $T_{SOI} > 5$ nm, the total mobility (open triangles in Fig. 8.8) is intermediate between the values for the 2- and 4-fold valleys, just as for bulk MOSFETs, because of the partial electron occupancy of the 4-fold valleys. However, as T_{SOI} approaches 3 nm, the total mobility approaches that for the 2-fold valleys; and when $T_{SOI} < 3$ nm, it is the same as that for the 2-fold valleys. This is consistent with the higher occupancy of the 2-fold valleys as T_{SOI} decreases. Furthermore, in this T_{SOI} range, the higher mobility for the 2-fold valleys due to the suppression of inter-valley phonon scattering also enhances the total mobility. So, it can be concluded that the enhanced mobility of SOI MOSFETs with an ultrathin SOI film is attributable both to the greater occupancy of the 2-fold valleys and to the suppression of inter-valley phonon scattering.

C. SOI-thickness-fluctuation-induced scattering

The previous section concerned the characteristics of the low-field electron mobility for a uniformly thick SOI layer, and ignored the influence of interface roughness. However, Sakaki *et. al* [8.25] and Gold [8.26] studied the influence of interface roughness on the mobility of the two-dimensional electron gas in quantum wells and reported that potential variations caused by variations in the width of a quantum well (d) scatter carriers and limit the mobility (μ_r). Variations in well width produce spatial variations in the ground level energy

$$E_0 = \frac{h^2}{8m^* d^2}, \tag{8.3}$$

where h is Planck's constant and m^* is the effective mass of an electron. The change in potential is

$$\Delta V = \frac{\partial E_0}{\partial d}\Delta, \tag{8.4}$$

based on the assumption that the roughness has a Gaussian distribution characterized by height (Δ). So, the mobility can be written as

$$\mu_r \propto \left(\frac{\partial E_0}{\partial d}\Delta\right)^{-2} \propto d^6. \tag{8.5}$$

This type of scattering could limit the mobility of ultrathin-body MOSFETs with an extremely thin SOI layer. Since the roughness of the Si/SiO_2 interface is ±1 atomic layer, it is reasonable to assume that the variation in the thickness of the SOI layer (δT_{SOI}) is at least 4 atomic layers (Fig. 8.9(a)).

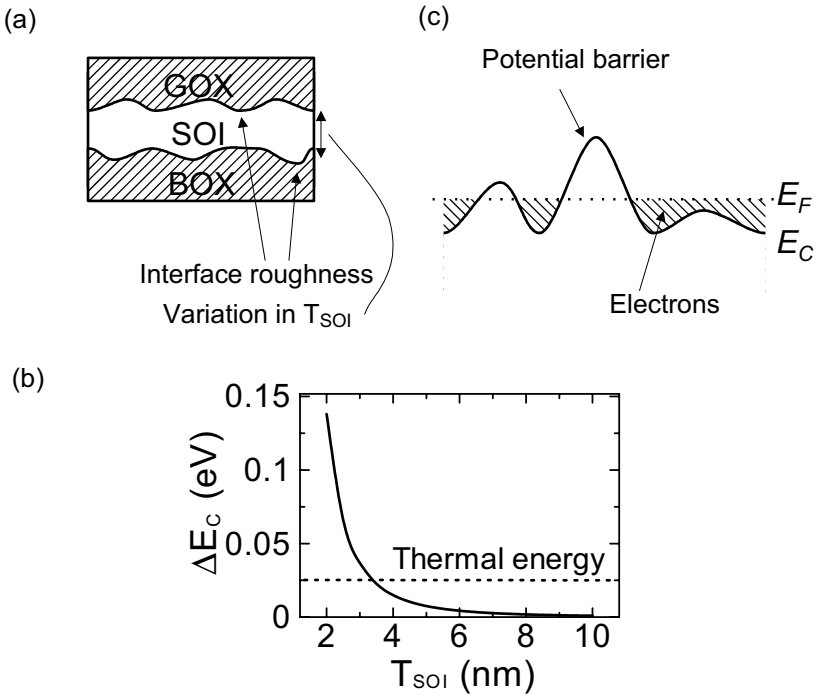


Fig. 8.9 (a) Schematic of ultrathin SOI film. Roughness of Si/SiO_2 interface produces variations in thickness of SOI layer. (b) Calculated change in conduction band energy (ΔE_C) caused by a variation in T_{SOI} of 4 atomic layers as a function of average T_{SOI}. (c) Illustration of how ΔE_C affects carrier scattering.

When T_{SOI} is very small, the envelope function of inversion layer electrons is determined by T_{SOI}, which directly modulates the subband energy. The calculated change in conduction band energy (ΔE_C) caused by a δT_{SOI} of 4 atomic layers (Fig. 8.9(b)) reveals that, when $T_{SOI} < \sim 4$ nm, ΔE_C exceeds the thermal energy at room temperature. That is, a substantial δT_{SOI} induces the

formation of potential barriers inside an ultrathin SOI layer (Fig. 8.9(c)). Since these barriers should work as scattering potentials for carriers, the electron mobility is limited by δT_{SOI}. In order to determine whether scattering due to δT_{SOI} reduces electron mobility or not, the mobility of ultrathin-body MOSFETs was investigated for 2.3 nm < T_{SOI} < 8 nm.

An ultrathin-body SOI MOSFET with a recessed-gate structure (Fig. 8.10(a)) was employed to eliminate the parasitic source/drain resistance. Devices were fabricated on UNIBOND wafers, which have a 200-nm-thick p-type Si film with a resistivity of 10 Ωcm and a buried oxide over 400 nm thick. The SOI channel was left undoped and had a thickness of less than 10 nm after the formation of a 10-nm-thick gate oxide. A cross-sectional TEM image of one device (Fig. 8.10(b)) shows that an ultrathin (2.4 nm) SOI channel was successfully formed. In addition, T_{SOI} was determined for all the MOSFETs as follows: First, the V_{th} shift induced by a substrate bias was measured for all the devices. Since a substrate bias has less effect on V_{th} as the body becomes thinner, a smaller V_{th} shift corresponds to a smaller T_{SOI}. These measurements yielded relative values of T_{SOI} for the devices. Then, the relationship between T_{SOI} and V_{th} shift was empirically determined from the TEM images of several devices. Finally, this relationship was used to precisely estimate T_{SOI} for the other devices.

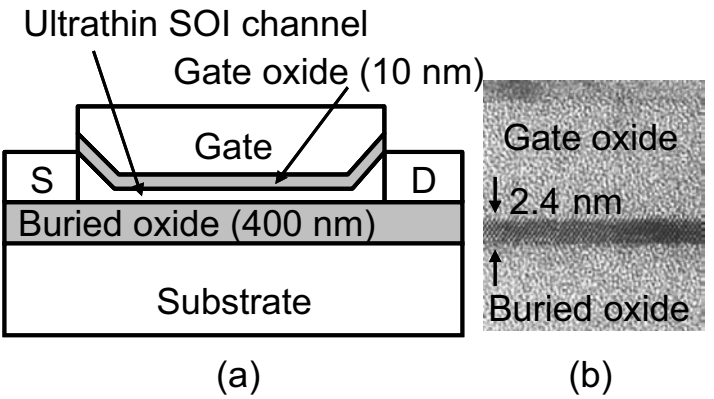


Fig. 8.10 (a) Schematic of recessed-gate ultrathin-body SOI MOSFET. (b) TEM image of fabricated device showing SOI channel.

The effective mobility was determined from the drain conductance measured at a drain voltage of 5 mV; and the surface carrier concentration was determined from the gate-channel capacitance versus gate voltage characteristics.

Measured curves of electron mobility (μ_e) versus effective field (E_{eff}) show that the mobility drops as T_{SOI} decreases (Fig. 8.11(a)), and that this trend is especially pronounced when E_{eff} is low. To determine the physical origin of the degradation in mobility, the characteristics were measured again at a low temperature of 25K (Fig. 8.11(b)), because phonon scattering is suppressed at a low temperature, allowing the effects of other scattering mechanisms to be observed more clearly. Over a wide range of T_{SOI} from 5.7 nm to 60 nm, the μ_e-E_{eff} characteristics exhibit a universal relationship independent of T_{SOI}, indicating that the effects of Coulomb and roughness scattering on electron mobility are basically the same for all the MOSFETs, and that the smaller mobility at room temperature when $T_{SOI} > 5.7$ nm is due to phonon scattering. On the other hand, when $T_{SOI} < 5$ nm, the rapid drop in mobility as T_{SOI} decreases suggests the emergence of an additional scattering mechanism in this range of thicknesses.

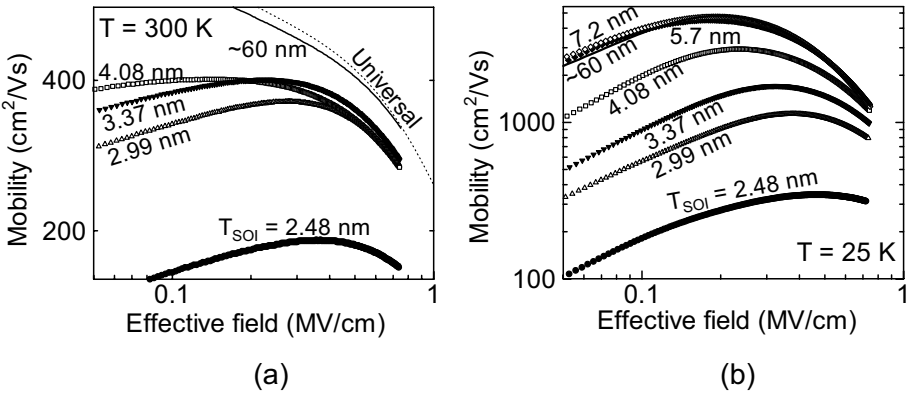


Fig. 8.11 Electron mobility vs. effective field measured at a temperature of (a) 300K and (b) 25K for various values of T_{SOI}.

To assess the involvement of δT_{SOI} in the drop in mobility, the dependence of mobility on TSOI at a low temperature of 25K was measured at an E_{eff} of 0.1 MV/cm (Fig. 8.12(a)). When $T_{SOI} < 3$ nm, the mobility is proportional to T_{SOI}^6, showing that, in this range of thicknesses, scattering due to potentials induced by δT_{SOI} is the main cause of the decrease in mobility. On the other hand, when $T_{SOI} > 5.7$ nm, μ_e is constant, which means that it is determined by Coulomb scattering. The temperature dependence of μ_e for a T_{SOI} of 2.48 nm (Fig. 8.12(b)) is qualitatively the same as that for a quantum well with width variations [8.25][8.26]: As the temperature increases, the mobility gradually rises owing to the greater kinetic energy of the electrons, and then falls when phonon scattering comes into play. This is the first observation of δT_{SOI}-induced scattering in ultrathin-body MOSFETs, and it occurs when $T_{SOI} < 4$ nm. Note that, in contrast to scattering due to surface roughness in bulk MOSFETs, δT_{SOI}-induced scattering requires the structural confinement of electrons within a very thin SOI layer. Moreover, it also limits the mobility when E_{eff} is low, because the confinement is not affected by the surface electric field.

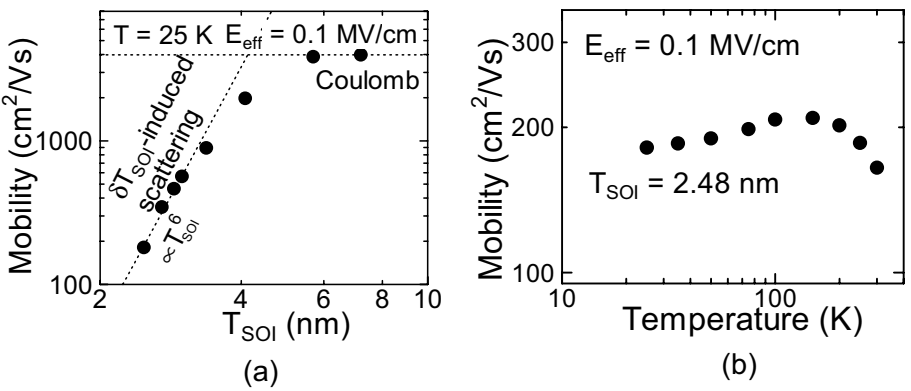


Fig. 8.12 Dependence of electron mobility (a) on T_{SOI} at a temperature of 25K and (b) on temperature for a T_{SOI} of 2.4 nm and an E_{eff} of 0.1 MV/cm.

D. Conclusion

An effective strategy for enhancing the inversion layer mobility of Si MOSFETs is to increase the subband energy difference between the 2- and 4-fold valleys at a (100) Si surface. One way to modulate the subband structure is to employ an SOI MOSFET with an SOI film thinner than the inversion layer of a bulk-Si MOSFET. When T_{SOI} is around 3 nm, the mobility is higher than that of bulk MOSFETs. The enhanced mobility is attributable to the higher occupancy of 2-fold valleys and the suppression of inter-valley phonon scattering, both of which arise from significant subband modulation due to the thinness of the SOI layer. The complicated dependence of mobility on T_{SOI} results from two competing mechanisms: one is that the mobility increases as the subband energy difference between the 2- and 4-fold valleys becomes greater, and the other is that the mobility decreases as the inversion layer becomes thinner. The results presented above demonstrate that SOI MOSFETs with an ultrathin SOI film are promising high-speed devices, provided that an ultrathin SOI film with a very uniform thickness and almost no interface roughness can be formed.

In addition, the carrier transport mechanism operating in ultrathin-body MOSFETs (2.3 nm < T_{SOI} < 8 nm) was experimentally investigated over a wide range of temperatures from 25K to 300K. It was found that carrier scattering due to variations in the thickness of the SOI layer strongly affects the electron mobility at room temperature when T_{SOI} < 4 nm and is the dominant scattering mechanism affecting electron mobility at low temperatures when T_{SOI} < 3 nm. Note that this carrier scattering mechanism is also operative in narrow-channel MOSFETs, such as the FinFET. When T_{SOI} < 4 nm, an atomically flat ultrathin SOI film is required to prevent the degradation in mobility due to δT_{SOI}.

8.3.2 SOI Wafer Technologies for Future MOSFETs

This section concerns the current status of SOI wafer technology and various SOI substrate structures for future MOSFETs.

In FD-SOI MOSFETs, the thickness of the SOI film is set so as to prevent punch-through by the current flowing in the interior of the film. Theoretical analyses and experimental data have shown that the thickness should be less than about one-third the channel length [8.27]. This means that the SOI film must become thinner and thinner as FD-SOI MOSFETs are scaled down.

The roadmap for the thickness of the SOI film of commercially available SOI wafers (Fig. 8.13) indicates that the thickness will decrease in step with the technology node. Mass production has already reached the 90-nm node, at which the Si film is as thin as 50 nm; and test fabrications are being carried out on wafers with a Si film as thin as 20 nm.

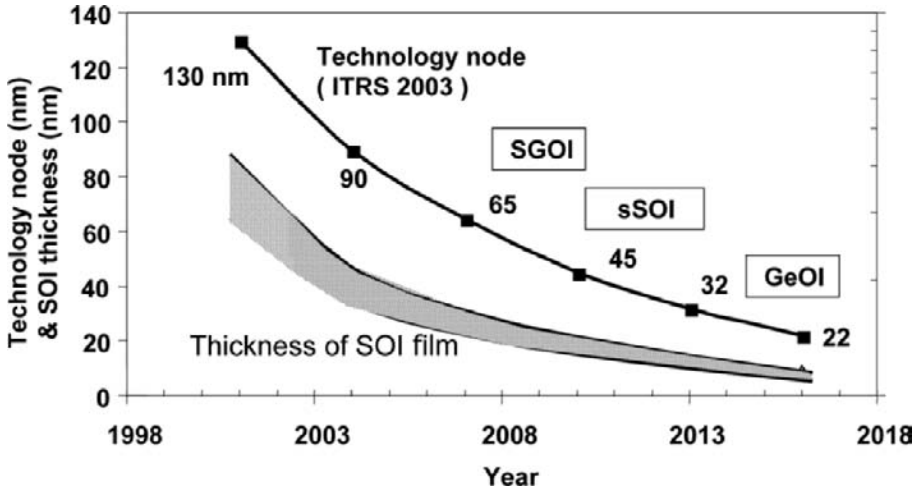


Fig. 8.13 Roadmap for thickness of SOI film on commercially available SOI wafers and for introduction of new substrate structures.

Regarding the uniformity of the thickness, which determines the variation in the device characteristics of short-channel FD-SOI MOSFETs, a deviation of ±1 nm has been reported to be achievable with the most advanced technology

for 300-mm-diameter SOI wafers [8.28]. If we assume that a deviation of ±10% in the thickness of the Si film is acceptable, then current technology has the potential to produce SOI wafers with a Si film 10 nm thick.

On the other hand, the electron mobility tends to degrade significantly when the Si film is thinner than about 5 nm (see Section 8.3.1), and the same is true of the hole mobility. If carrier scattering due to potential variations arising from non-uniformity in the thickness of the Si film is responsible for this mobility degradation [8.29], there is still room to improve the mobility by improving substrate technology.

Another way to enhance carrier mobility through SOI substrate technology is to use a novel structure, such as strained Si on SiGe on insulator (SGOI), strained Si on insulator (sSOI), and Ge on insulator (GeOI) (Fig. 8.14). In SGOI and sSOI, biaxial tensile strain is given to Si film to enhance the electron and hole mobilities.

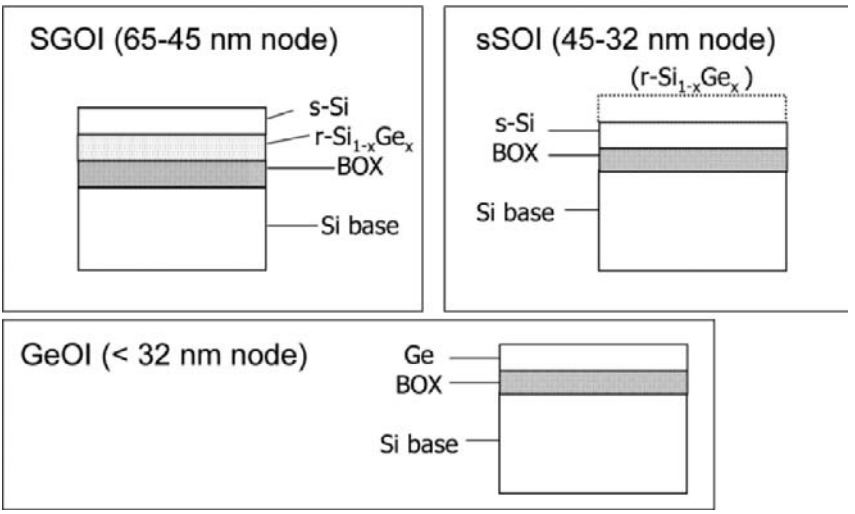


Fig. 8.14 Strained-SOI (SGOI, sSOI) and GeOI substrates for future MOSFETs. s-Si means strained Si, and r-$Si_{1-x}Ge_x$ means relaxed $Si_{1-x}Ge_x$.

Figure 8.15 illustrates the mechanism. For electrons, biaxial tensile strain along the x-y plane raises the six-fold degeneracy of the conduction band. This makes the energy lower for z-axis valleys than for the other valleys; so, more electrons concentrate in the z-axis valleys. Since the z-axis valleys have

the smallest conductivity mass of electrons in the x-y plane, the average mobility of electrons in the MOSFET channel is higher than that of devices made without strain in the Si. The mobility enhancement for a Ge content of 20% has been found experimentally to be in the range of 60-80% for electrons and 15-25% for holes [8.10].

Regarding the technology itself, strain is introduced into a Si film by growing Si epitaxially on a relaxed $Si_{1-x}Ge_x$ layer, which has a larger lattice constant than Si. The atoms in strained Si expand in the lateral direction by approximately 0.8% for a Ge content of 20%. In SGOI, strained Si is grown after the relaxed $Si_{1-x}Ge_x$ layer together with the BOX is transferred to a base wafer. In sSOI, on the other hand, strained Si is first grown on the $Si_{1-x}Ge_x$ layer of a donor wafer, and then transferred with the BOX to a base Si wafer; and finally, the $Si_{1-x}Ge_x$ layer is etched off [8.30].

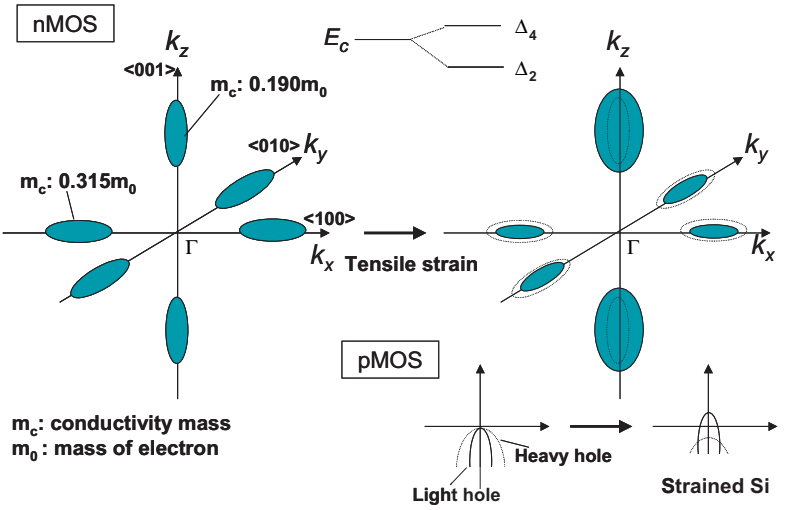


Fig.8.15 Effect of strain on Si.

In the GeOI structure, a thin Ge film is formed on the BOX layer. Since Ge has a larger mobility (or in other words, a smaller effective mass) than Si, the drain current should be larger, even for an ultrashort channel, in which no carrier scattering occurs and the ballistic mode dominates [8.31]. A GeOI substrate is made by splitting off the surface layer of a Ge wafer or an epitaxially grown Ge film, and bonding it to a Si substrate with a BOX film [8.32].

8.3.3 Design of FD-SOI MOSFETs in Sub-100-nm Regime

FD-SOI MOSFETs are promising devices for low-power applications because of their steep subthreshold slope and low junction capacitance. In addition, the threshold voltage of the front gate can be tuned by means of a back-gate bias or a substrate bias. Two important design issues must be considered when these devices are scaled down to the sub-100-nm regime: adjustment of the threshold voltage and maintenance of the steep subthreshold slope. This section discusses these issues using the results of two-dimensional device simulations.

A. Optimization of threshold voltage and drive current
There are three ways of adjusting the threshold voltage:

I. changing the work function (Φ_m) of the gate,
II. changing the channel doping concentration (N_{SOI}), and
III. changing the back-gate bias (V_g^{back}).

To determine which is best, it is necessary to examine how they affect short-channel effects and the drive current. This was done through simulations on an FD-SOI nMOSFET (Fig. 8.16) using the three sets of parameters in Table 8.1. The values were chosen so as to make the threshold voltage 0.2 V for a long-gate device. A heavily doped Si substrate was used as the back-gate electrode.

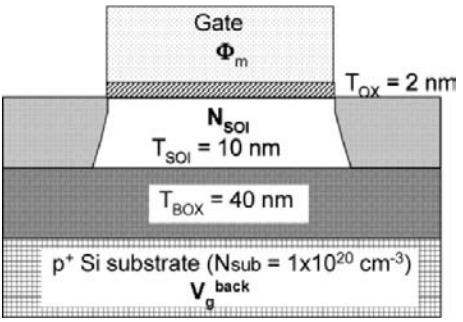


Fig. 8.16 Structure of FD-SOI MOSFET.

Table 8.1 Values of Φm, N_{SOI}, and V_g^{back} needed to set V_{th} to 0.2 V for a long-gate FD-SOI nMOSFET.

	Type I	Type II	Type III
	Changing Φ_m	Changing N_{SOI}	Changing V_g^{back}
Work function, Φ_m	**4.34 eV**	n+ Poly Si	n+ Poly Si
Channel doping concentration, N_{SOI}	1×10^{15} cm^{-3}	**2.3×10^{18} cm^{-3}**	1×10^{15} cm^{-3}
Back-gate bias, V_g^{back}	0 V	0 V	**-4.4 V**

The threshold voltage roll-off characteristics (Fig. 8.17(a)) show that changing either the back-gate bias (type III) or the work function of the gate (type I) suppresses short-channel effects more than changing the channel doping concentration (type II), with the former being slightly more effective than the latter. We can understand the reason for the differences by looking at the depth profiles of the potential in the middle of the gate for short- and long-gate devices in Fig. 8.17 (b) and (c), respectively.

Looking at the potential of long-gate devices with the same threshold voltage in Fig. 8.17(c), we see that type I has the lowest surface potential and that type III has the lowest potential at the interface between the SOI film and the buried oxide. For a short-gate device, type I makes the surface potential lower than type II. The short-channel effects are different for these two methods because the space charge affects the threshold voltage in different ways for each. For type II, the threshold voltage is almost completely determined by the size of the space charge. So, a decrease in the charge sharing of the space charge by the p-n junctions around the drain region lowers the threshold voltage of a short-channel device. For type I, on the other hand, the threshold voltage is primarily determined by the difference in work function between the gate and the substrate, rather than by the potential drop across the gate oxide when the channel doping concentration is low. Consequently, the threshold voltage is much less dependent on the charge sharing of the space charge, leading to stronger immunity to short-channel effects.

Looking at the potential at the interface between the SOI film and the buried oxide for a short-gate device (Fig. 8.17 (b)), we see that back-gate control fixes the back-gate potential at a lower value than do the two other methods, in which a back channel forms. This is because the back-gate bias pins the potential at the back interface, even when the gate is short. As a result,

back-gate control suppresses drain-induced barrier lowering (DIBL) through the buried oxide.

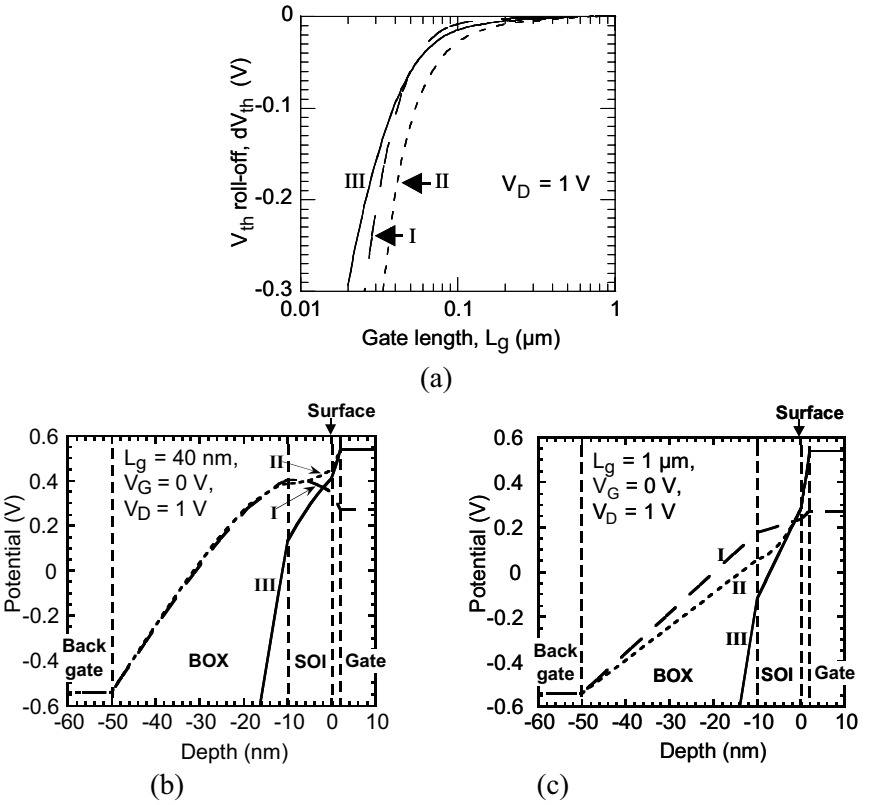


Fig. 8.17 Effect of parameters in Table 8.1 on (a) the threshold voltage roll-off characteristics, and (b) and (c) the depth profile of the potential in the middle of the gate for short- and long-gate devices, respectively.

It should be noted that short-channel effects are especially reduced in devices with a thin SOI layer, a thin buried oxide, and a ground plane because the change in the back potential between the substrate and the buried oxide associated with shortening the channel is suppressed. Moreover, variations in the threshold voltage arising from variations in the thickness of the SOI layer, which is one of the most serious problems in FD-SOI MOSFETs, are much

smaller for type I and type III than for type II. This is because the space charge, which is the main cause of threshold voltage variations in type II, is negligible in type I and type III [8.33]-[8.36].

Fig. 8.18 shows the I_D-V_G characteristics of a long-gate device. Type I yields the highest drive current because it provides the highest gate work function, which results in the weakest surface electric field and thus the highest mobility. Based on the above analysis, the combination of back-gate control and gate-work-function control should provide the best results from the standpoints of both short-channel effects and drive current.

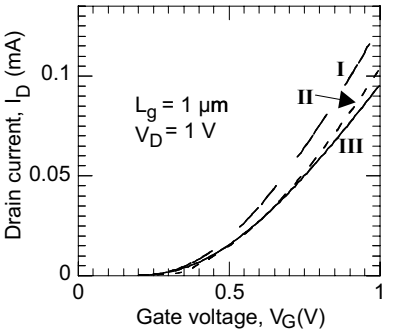


Fig. 8.18 I_D-V_G characteristics for three methods of V_{th} control.

Fig. 8.19 shows how the threshold voltage shift due to short-channel effects, and also drive current, vary with the gate work function. The back-gate voltage was adjusted so as to yield the same threshold voltage for each value of the gate work function for a long-gate device. It can be seen that short-channel effects are the smallest when the gate work function is around 4.1 to 4.2 eV. In this range, the drain current is higher than that obtainable with type III. Two factors are involved in reducing short-channel effects: control of the surface potential by the gate work function and control of the back potential by the back gate.

An important point regarding the relationship between the gate work function and short-channel effects in this study is that, as the work function increases, the back-gate bias is also increased to keep the threshold voltage constant; and as a result, the behavior of short-channel effects is influenced by changes in both the gate work function and the back-gate bias. So, the reason why the

short-channel effects exhibit a minimum at a particular gate work function and back-gate voltage is that they are affected in opposite ways by these two parameters. Increasing the work function lowers the front surface potential of an SOI MOSFET, which, in turn, suppresses short-channel effects when the body is thin. On the other hand, increasing the back-gate bias raises the back surface potential of an SOI MOSFET, which enhances short-channel effects. These opposite effects produce the minimum. The existence of the minimum means that the combination of these two control methods produces the optimum result. So, it is unnecessary to dope the channel.

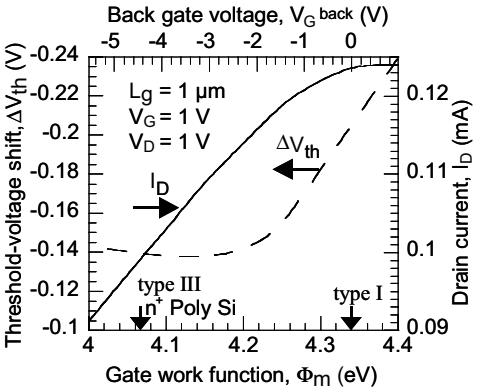


Fig. 8.19 Dependence of threshold voltage shift due to short-channel effects, and also drive current, on the gate work function. The threshold voltage shift is defined to be the difference in threshold voltage between devices with gate lengths of 1 μm and 40 nm. The back-gate voltage was adjusted so as to yield the same threshold voltage for each value of the work function for a long-gate device.

Increasing the work function of the gate also has another advantage in that it reduces the normal electric field, resulting in higher mobility. So, the drive current increases linearly with gate work function. Just as for nMOSFETs, for pMOSFETs also, short-channel effects exhibit a minimum at a particular gate work function and the drive current is higher [8.36].

Several techniques for continuously changing the gate work function have been devised [8.37]-[8.39], making it possible to optimize both the gate work function and the back-gate voltage. In summary, a combination of back-gate and gate-work-function control, along with an undoped SOI layer, constitutes

the best method of adjusting the threshold voltage from the standpoints of both short-channel effects and drive current.

B. Control of subthreshold swing - Buried insulator engineering -

A small subthreshold swing is one of the biggest advantages of FD-SOI MOSFETs, and the keys to obtaining it are a small substrate capacitance and the suppression of short-channel effects. A variety of SOI substrates have been devised to provide these conditions, such as those with an ultrathin SOI layer [8.40], a thin buried-oxide layer [8.41], and a buried air-gap layer [8.42]. However, there is a limit to how thin the buried oxide can be made because, below that limit, the subthreshold swing increases [8.40], as explained below. This section discusses how the subthreshold swing is affected by various SOI structural parameters, particularly those associated with the buried oxide, such as thickness and permittivity.

Fig. 8.20(a) shows how subthreshold swing changes with buried-oxide thickness for various gate lengths from 1 μm down to 40 nm. The SOI layer was assumed to be 10 nm thick. For each thickness, the threshold voltage is set to the back-gate voltage. For a long-gate device, the subthreshold swing increases monotonically as the buried oxide becomes thinner. In contrast, for a short-gate device, it exhibits a minimum, indicating that there is an optimum thickness for the buried oxide. The same type of behavior also appears in devices with a thinner SOI layer (Fig. 8.20(b)), although the subthreshold swing is smaller.

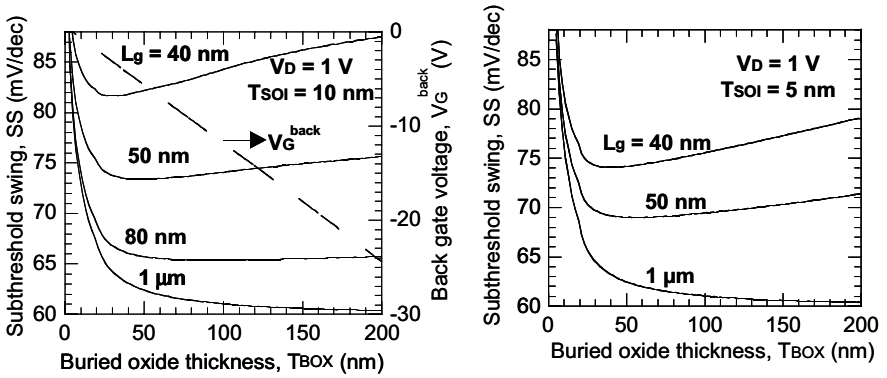


Fig. 8.20 Subthreshold swing vs. thickness of buried oxide with gate length as a parameter for (a) T_{SOI} = 10 nm and (b) T_{SOI} = 5 nm.

These subthreshold characteristics can be explained by examining how the thickness of the buried oxide affects both the capacitance of, and DIBL through, the buried oxide. Fig. 8.21 illustrates how the thickness affects the subthreshold swing. For a long-gate device, the factors affecting subthreshold swing can be represented by a one-dimensional equivalent circuit consisting of the gate-oxide capacitance, the SOI body capacitance, and the buried-oxide capacitance connected in series.

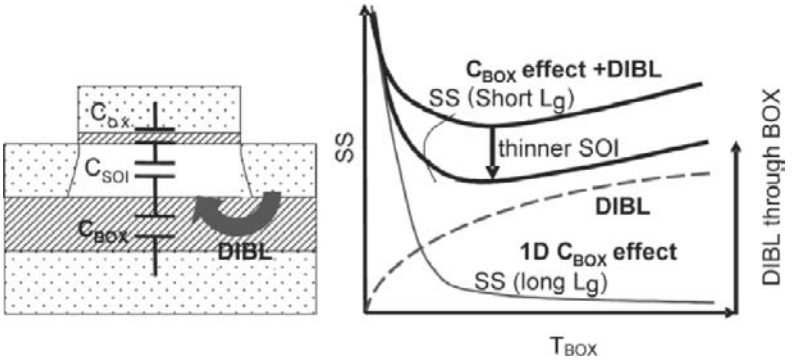


Fig. 8.21 Diagram illustrating relationship between subthreshold swing and the thickness of the buried oxide of FD-SOI MOSFETs.

This yields the following equation [8.43]:

$$S = \frac{kT}{q} \ln 10 \left(1 + \frac{C_{SOI}}{C_{OX}} \cdot \frac{C_{BOX}}{C_{BOX} + C_{SOI}} \right), \tag{8.6}$$

where S is the subthreshold swing; kT/q is the thermal voltage; and C_{SOI}, C_{OX}, and C_{BOX} are the capacitances of the SOI layer, the front-gate oxide, and the buried oxide, respectively. As the buried oxide becomes thicker, the buried-oxide capacitance becomes smaller and the front-gate-oxide capacitance becomes larger, thereby reducing the subthreshold swing. On the other hand, for a short-gate device, the influence of DIBL through the buried oxide, which is caused by the lateral penetration of the field from the drain into the channel, is superimposed on the effect of the buried-oxide capacitance [8.44]. A thicker buried oxide enhances DIBL because the electric field from the drain penetrates laterally through the BOX into the channel region (arrow in Fig. 8.21), which increases the subthreshold swing. On the other hand, a

thinner buried oxide suppresses DIBL because the field penetrates all the way through the BOX to the substrate and does not reach the channel. Since the buried-oxide capacitance and DIBL have opposite effects on subthreshold swing as the thickness of the buried oxide changes, the subthreshold swing exhibits a minimum at a particular thickness. Thus, it is not only possible, but also necessary, to optimize of thickness of the buried oxide in order to minimize the subthreshold swing in sub-100-nm FD-SOI MOSFETs.

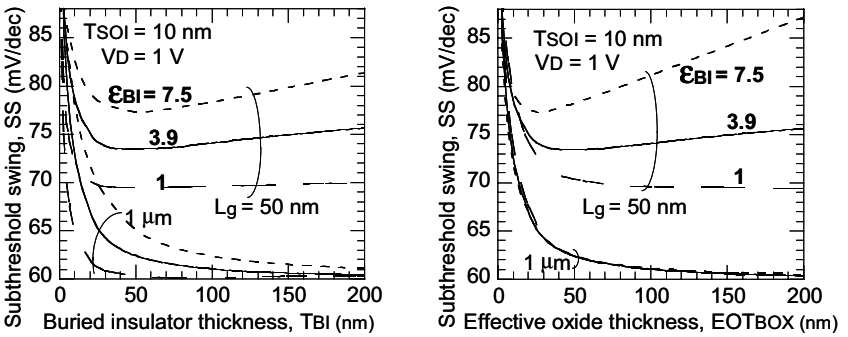
One way to further reduce the subthreshold swing is to replace the buried oxide with a different insulator (buried insulator) that has a lower permittivity. Fig. 8.22 (a) shows the relationship between subthreshold swing and the thickness of the buried insulator for two gate lengths, with the permittivity of the buried insulator as a parameter. Air, silicon dioxide, and silicon nitride are used as examples. The subthreshold swing decreases as the permittivity decreases, regardless of gate length. In addition, when the permittivity is one and the gate is short, the subthreshold swing is almost constant. In contrast, for other values of the permittivity, the subthreshold swing exhibits a pronounced minimum, indicating that the thickness of the buried insulator needs to be optimized.

To investigate the physical origin of the dependence of subthreshold swing on permittivity, the swing is plotted against equivalent oxide thickness (EOT_{BOX}) in Fig. 8.22(b). EOT_{BOX} is defined by the following equation:

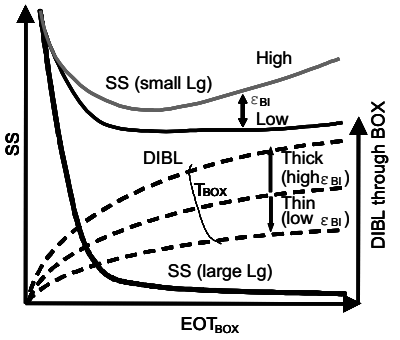
$$C_{box} = \frac{\varepsilon_{SiO_2}}{EOT_{BOX}} = \frac{\varepsilon_{BI}}{T_{BI}} \quad , \tag{8.7}$$

where ε_{SiO2} and ε_{BI} are the permittivities of silicon dioxide and the buried insulator, respectively; and T_{BI} is the thickness of the buried insulator. When the gate is long, the curve of subthreshold swing vs. EOT_{BOX} is unaffected by the permittivity. In contrast, when the gate is short, a lower permittivity makes the subthreshold swing smaller and weakens the dependence of swing on EOT_{BOX} when EOT_{BOX} is large. Fig. 8.7(c) illustrates how the permittivity of the buried insulator affects the subthreshold swing. For a long-channel device, its effect can be described by a one-dimensional equivalent circuit consisting of a series of capacitances. This yields the same values of the swing as a function of EOT_{BOX}, regardless of the permittivity of the buried insulator. For a short-channel device, this relationship does not hold; a lower permittivity suppresses DIBL, thereby making the subthreshold swing smaller. This is

because a lower permittivity reduces the buried-insulator thickness for a given EOT_{BOX} (thus reducing the subthreshold swing) according to (8.7). In conclusion, using a low ε_{BI} in combination with the optimum thickness of the buried insulator suppresses any increase in the subthreshold swing of FD-SOI MOSFETs when the gate length is reduced below 100 nm.



(a) (b)



(c)

Fig. 8.22 (a) Subthreshold swing as a function of the thickness of the buried insulator, with the permittivity of the buried insulator as a parameter. (b) Subthreshold swing as a function of the effective thickness of the buried oxide. (c) Schematic diagram illustrating how the permittivity of the buried insulator affects DIBL and the subthreshold swing.

8.4 Power-Aware Electronics and Role of FD-SOI Technology

One of the most serious problems confronting CMOS technology is the power explosion of chips originating from the scaling law (Fig. 8.23) [8.45]-[8.47]. In addition, the number of processors per person is steadily increasing (Fig. 8.24) as electronic devices become more pervasive; and this makes the power explosion even worse.

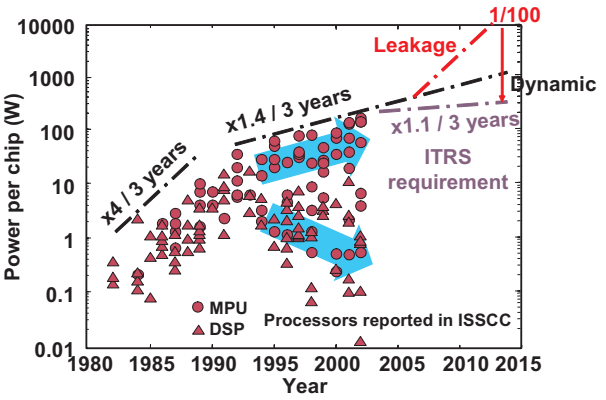


Fig. 8.23 Trend in power consumption per chip.

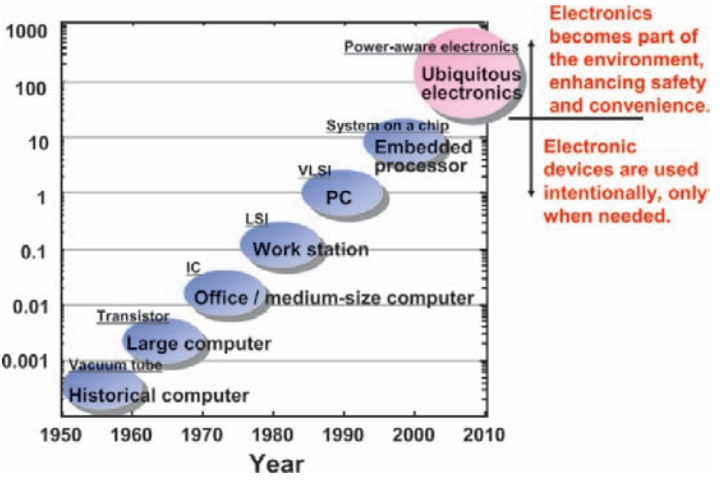


Fig. 8.24 Number of processors per person.

If the power per chip is not dramatically reduced, LSIs will consume most of the energy society produces. So, a greater awareness of the power problem is needed throughout the electronics industry.

8.5 Summary

In this context, FD-SOI technology, which provides a low-power solution to chip implementation, will become increasingly important. Another issue the semiconductor industry will have to cope with is that process variations become larger as devices are scaled down. The variation in threshold voltage (V_{th}), for example, is increasing relative to the supply voltage (Fig. 8.25). This gives rise to a higher leakage current and lower yields. One promising solution is to adaptively control V_{th} with the second gate voltage of a double-gate structure (Fig. 8.26). This structure is easier to build with FD-SOI than with bulk CMOS technology. So, FD-SOI technology will undoubtedly play an important role in power-aware electronics.

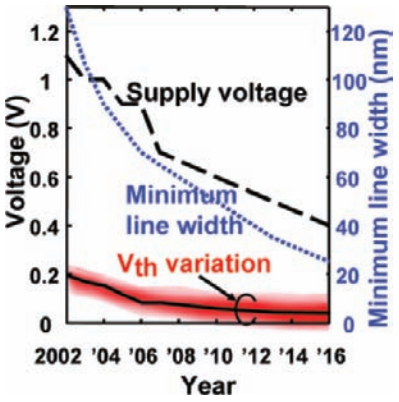


Fig. 8.25 Threshold-voltage variation.

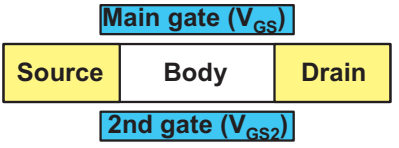


Fig. 8.26 Double-gate MOSFET structure in FD-SOI CMOS.

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