William J. Greig

Integrated Circuit Packaging, Assembly and Interconnections

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DEDICATION

To my family,

my wife Joan

and

our children, their spouses and grandchildren

Karen – Christopher, Ryan, Kevin
Billy and Cathy – Alli, Jeff, Shauna
Joni and Fred – Danny, Kerri, Traci Jo
Jimmy and Colleen – Maggie, Molly, Katie, Claire
Ronny and Meryl – RJ, Connor
Steven
Kenny

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Preface

The integrated circuit with each new generation has been characterized by increasing functionality. In the 1980's Very Large Scale Integrated Circuits (VLSIC) began to emerge with transistor counts approaching one million plus per chip! The IC package quickly became more than a "chip carrier". Now the packaging had to address the electrical, mechanical and thermal requirements of the IC, and had to do so cost-effectively. A package costing more than the chip was not an option. In addition, the demands of the marketplace for product that was "smaller, better and cheaper" came into play.

As a result the late '80s saw paradigm shifts in IC packages and packaging options. Area array packages, in particular, the Ball Grid Array (BGA) began to emerge that more effectively addressed increasing chip I/O count. Ceramic packaging for high performance circuits (microprocessors digital signal processors) gave way to organic based packages, the plastic BGA (PBGA), offering a more favorable solution to package cost. And the hybrid circuit suddenly became a multichip module!

Over the past 15 years the author has developed and presented professional development courses at various technical symposia as well as on-site at semiconductor, component and equipment manufacturers and materials suppliers facilities. The courses have covered topics that make up the electronic manufacturing arena focusing on packaging and assembly of the integrated circuit.

This book evolved from these courses and discusses the many changes that have taken place not only with the physical package itself but also the currently available packaging options and assembly technologies. It is intended to serve as an *introduction* to IC packaging and assembly providing sufficient coverage to afford a working knowledge of the basic concepts and technologies. The book is intended for personnel new to the industry and, those indirectly involved in electronics manufacturing such as upper management, quality assurance, procurement, marketing and sales, and equipment manufacturers and material suppliers. For those directly involved the book can serve as a useful *overview* of new and emerging technologies.

The First Chapter is discussion of electronic manufacturing that basically describes the packaging and assembly of the integrated circuit. It identifies the various levels of microelectronic assembly, i.e., Level 1.0 interconnects – chip to package and Level 2.0 – chip or package to a substrate board and the packaging options, – single chip, multichip and chip on board.

The Second Chapter briefly reviews the integrated circuit manufacturing process and the *applicability* of much of the procedures and practices to IC packaging and assembly. It highlights the significance of a cleanroom operating environment and the photolithographic process in particular, as a model for implementing a proven high yield cost effective manufacturing technology.

Subsequent Chapters 3 and 4, discuss the trends in the IC package, the Chip Scale Package, and Wafer Level Packaging. Chapter 5 covers Multichip Packaging and the various sub-classifications – the hybrid circuit, the multichip module, System

in Package, System on Packaging and the rapidly developing 3-D Packaging that includes stacking of both multiple die and packages.

Working with bare die as opposed to package devices is discussed in Chapter 6 and covers the subject of Known Good Die or KGD. It presents the concerns associated with bare die and multichip applications and the problem related to the lack of sufficient electrical testing of unpackaged die to insure the device meeting full electrical specifications. Various approaches to resolving this problem and providing for Known Good Die are discussed.

The assembly of a bare die onto an organic board, Chip on Board (COB) is covered in Chapter 7. Implementation and incorporation into Surface Mount Assembly lines and concerns are included. A "packageless packaging" approach makes it a viable packaging option offering both increased component density and an enhanced reliability at the Level 2.0 printed circuit board (PCB) assembly.

The Level 1.0 interconnect technologies are covered in subsequent chapters, C&W Assembly in Chapter 8, TAB in Chapter 9, and Flip Chip Bumping and Assembly, Chapter 10 and 11 respectively.

The last four chapters, 12 through 15, cover the manufacturing technologies, namely Thin Film, Thick Film, Cofired Ceramic and the Organic Laminate Technology, for packages – SCP and MCP, and High Density Interconnect (HDI) substrates. The Thin Film process technology is highlighted as the leading technology in meeting the challenges that arise with the packaging and assembly of current and future integrated circuits. It basically emulates the IC manufacturing and therefore has the inherent capability for achieving very fine line conductor circuitry and the high wiring density required for high density interconnects supporting Levels 1.0 and 2.0. The application of the Thin Film Technology to Thick Film, Cofired and Laminate, to further enhance the overall advantages of each is also discussed. Chapter 15 presents a discussion of a combined Thin Film and Laminate process (Build Up Technology, BUT) as a key enabler for Level 2.0 interconnect substrates that adequately accommodates all current and future IC packaging and assembly technologies.

Acknowledgements

I was fortunate in having spent my early years in the electronics industry at RCA working on materials and process development supporting the early manufacture of both the transistor and the integrated circuit that followed. I am indebted to my mentor during those early years, the late Arnold Rose, who guided me and provided me the opportunity to become deeply involved in the many process technologies that are still part of IC manufacturing.

Over the years that followed there were many individuals who help expand my areas of expertise and made it possible for me to write this book. There were and are many and to attempt to recognize everyone would be nearly impossible and would add many pages to this book. And I am certain I would be missing many as well. They come from all areas of industry and include: component manufacturers, equipment manufacturers and material suppliers, manufacturer reps and of course, my colleagues in consulting.

There are several however that I must acknowledge since they were particularly helpful in bring this book to fruition. In particular I am extremely thankful to Richard Brown, an industry consultant, author, instructor of professional development courses who provided invaluable insight. I am most grateful for the many discussions, his suggestions and critiques he provided that were so helpful.

I must also recognize and thank the following all of whom contributed in many and varied ways: Russ Atkinson, Avid Associates; Lee Levine, K&S; Tom Terlizzi, Aeroflex Plainview Inc.; Ray Fillion, GE Global Research; and Bruce Romenesko, Johns Hopkins University, Applied Research Laboratory.

I would be remiss if I didn't also thank the many companies that granted permission to use the copyrighted photographs, figures and tables used in the book. Finally, I want to thank the editorial staff at Springer without whose help there simply would not be any book.

In all probability I omitted several individuals who also made valuable contributions and for this I am truly sorry. I thank them "in absentia".

About the Author

A graduate of Fordham University with a BS in Physics Bill has had extensive experience in Microelectronics covering semiconductor processing and assembly, hybrid circuits, and PWB fabrication and assembly. He began his career with RCA Semiconductor Division and subsequently worked for General Electric and Lockheed Electronics. While at RCA he was awarded six U.S. patents covering wafer processing and semiconductor assembly. At General Electric he was a staff engineer and consultant for hybrid circuits and PWB manufacturing.

As Manager of Advanced Development at Lockheed, he was directly responsible for the design, construction, and operation of a state of the art Microelectronic Packaging facility supporting research, development, and manufacture of advanced hybrid circuits and multichip modules.

He became an independent consultant in 1988. His clients have included material suppliers, assembly equipment manufacturers, and component manufacturers.

His consulting activities has included work at NASA Headquarters in Washington D.C. where he provided technical expertise and assistance in developing an Advanced Integrated Circuit Packaging and Assembly Program.

Bill specializes in packaging and assembly, focusing on high density substrate manufacturing, and chip assembly including flip chip and chip scale packaging.

His company offers assistance in technology assessment and implementation, and specializes in technical audits of manufacturing operations directed towards yield improvement and reliability enhancement.

He has developed several educational and training courses which are offered at various national and international symposia and on-site presentations.

He is an active member of IMAPS where he is a Fellow of the Society and Past President of the Garden State Chapter.

1 Electronic Manufacturing and the Integrated Circuit

1 — MICROELECTRONICS AND THE TRANSISTOR [1]

The “Microelectronics Age” essentially began in 1947 with the invention of the transistor at Bell Laboratories. This historic solid state device was capable of both amplifying and switching (on/off) electrical signals. Its introduction spawned many new electronic products featuring major changes affecting end product characteristics, performance, and reliability.

The first transistor was based on the semiconductor Germanium (Ge), and became commercially available in the early 1950s. Transistors based on the superior properties and manufacturability of silicon (Si) followed later in the decade replacing Ge in almost all applications.

The overall impact of the transistor in the marketplace was immediate with rapid growth in high volume production. Compared to the then active electronic component, the vacuum tube, the transistor was significantly smaller and lighter, and required a considerably lower level of power for operation. Transistors made possible a quantum jump in electronic product *miniaturization*. Early applications were in the consumer market and included portable radios and hand-held calculators.

Use of the transistor as a switching device lead to early applications in the computer industry This quickly accelerated further development of the transistors highlighted by higher operating frequencies and faster switching speeds.

1.1 — The Integrated Circuit and Moore’s Law (2-5)

A little over a decade after the transistor went into production, a major development in solid state device technology occurred with the invention of the Integrated Circuit (IC). Co-invented by Jack Kilby of Texas Instruments and Bob Noyce of Fairchild Semiconductor in 1958, the IC consisted of multiple transistors interconnected on a single silicon die.

The IC went into production in the 1960s. Like the transistor, IC manufacturing experienced an equally rapid growth characterized by the introduction of ICs with increasing transistor count and functionality.

The number of transistors on the IC obviously determined the IC’s ultimate level of functionality. It therefore represented another quantum jump in miniaturization while at the same time provided a major increase in electrical functionality and performance.

In 1965, Gordon Moore, at Fairchild at the time, published a paper in which he noted that the IC's "complexity" was roughly doubling every year of manufacture and predicted that it would continue to do so in the future. This subsequently became known as Moore's Law. Over the years Moore's Law has undergone some modification, namely in the timeframe for doubling and the definition of "complexity" (Figure 1-1).

In 1971 another significant but related event occurred with the invention of the microprocessor [6] at Intel Corporation. Basically, a "computer on a chip", its introduction had a far reaching impact on the entire electronics industry. The demand for microprocessors with increased performance was immediate and a driving force in a continuing and intensive development effort of all aspects of the technology covering IC design, manufacturing, and applications engineering.

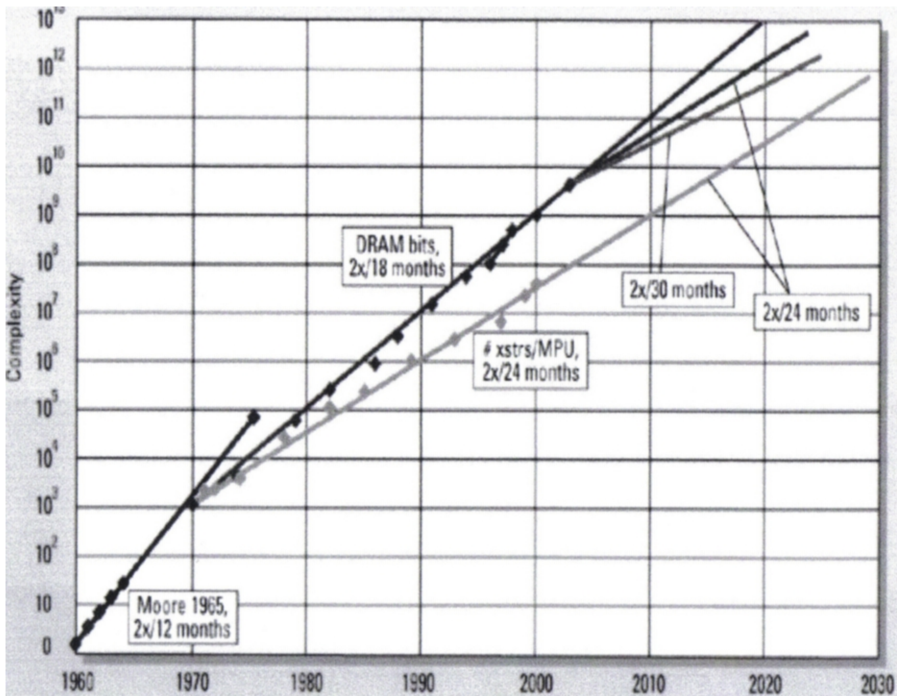


Figure 1-1. Moore's Law [3]

With the introduction of the microprocessor and the Dynamic Random Access Memory (DRAM) during the 1970s, some parameter modifications to Moore's Law were needed. In particular, the timeframe for doubling is a best fit at 24 months for the microprocessor and 18 months for the DRAM. In addition, for the microprocessor "complexity" indicates the number of transistors per device while for the DRAM it is the number of bits per device. Further modifications with Moore's Law are expected in the future particularly with the DRAM extending the doubling to 24 months and possibly 30 months.

The single transistor device of the early ‘50s is now, slightly over 50 years later, an IC containing literally millions of transistors and expected to reach a billion transistors by the end of the decade.

1.2 — Electronics Manufacturing and the Technology Drivers

Perhaps not surprising, the IC as well as the marketplace (i.e. end product) are the drivers that influence the packaging and assembly technologies that are the heart of the manufacturing process. It is a marketplace for example, that during the last decade has experienced a tremendous increase in the number, variety and the availability of electronic products. All have taken advantage of the ever-increasing performance potential of the integrated circuit. The marketplace can be segmented into two types of product. One is driven primarily by the requirement for high performance, and the other by size and cost. The latter is represented by the high volume but low cost products, all requiring portability, such as cell phones, camcorders, laptops, digital cameras, personal digital assistant (PDAs) and the like. The high-performance, high-reliability products are typically those used for avionics, space, and military applications.

The life cycle of many of the products, particularly in the high volume consumer categories, is on the order of one year or less. To be marketable and remain competitive, however, next generation models must be “smaller, better, and cheaper”. This requirement has in fact become the mantra of the electronics industry and strongly influences product manufacture impacting both the packaging and assembly of ICs.

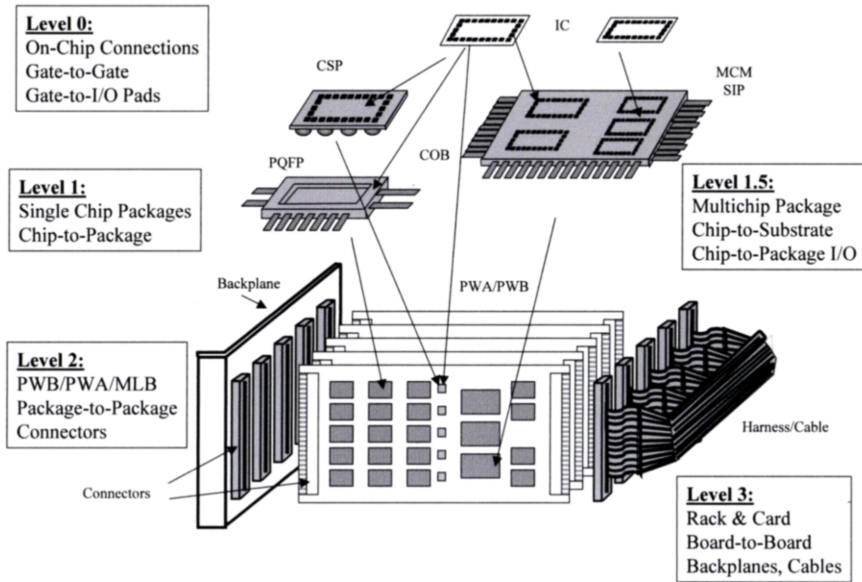
1.2.1 — The Manufacturing Process [7,8]

The Electronics Manufacturing Process is graphically represented in Figure 1-2. The process starts with the IC and takes it through a series of steps, referred to as “Packaging Levels” or “Levels of Interconnection” involving assembly of both bare die and packaged components.

Successful manufacturing ideally means realizing chip level performance in the end product. It therefore requires attention to the following:

- Identifying and accommodating the electrical, mechanical and thermal requirements inherent in the IC, and
- Selecting those manufacturing technologies that incorporate attributes that will contribute to an end product that is “smaller, better, and cheaper”.

Meeting this challenge is a continuing and on going effort. It has resulted in the IC’s physical package, as well as the assembly of both the die and the package, undergoing paradigm shifts in both materials and process technologies.



(Courtesy General Electric Global Research)

Figure 1-2. The Electronic Manufacturing Process

1.2.2 — Packaging Options

The graphical representation of the process shows three packaging options or paths: Single Chip Packaging (SCP), Multichip Packaging (MCP), and Chip on Board (COB). SCP (Figure 1-3(a)) has been the industry's standard from the beginning, while MCP (Figure 1-3(b)) is a variant involving assembling multiple die in a single package. COB (Figure 1-3(c)) is an option that basically eliminates the packages with bare die assembled directly to the second level interconnect substrate, the printed wiring board (PWB).

The three packaging scenarios each offer specific advantages and disadvantages. Selection of a particular option is dependent on several factors based on both the IC and the end product requirements. These are discussed in Chapters 3, 5, and 7, respectively.

1.2.3 — Levels of Interconnect/Packaging

The manufacturing process for mostly all electronic products follows the three "Packaging Levels" indicated. They are described as:

- ✓ **Level 1.0**—covering the connection (assembly) of the die to a package (SCP) or substrate (MCP).

The interconnect technologies, Figure 1-4, include:

(a) Chip and Wire—C&W
(b) Tape Automated Bonding
(c) Flip Chip (FC) Bonding

Each of these is discussed in detail in Chapters 8, 9, 10 and 11.

When multiple die are connected to a package/substrate, (**Level 1.5** in Figure 1-2), the substrate must provide the necessary interconnections between die. This is accomplished by an embedded conductor interconnect network within the package. These package/substrates are manufactured using thick film/cofired ceramic, thin film or laminate printed wiring board (PWB) processes that are discussed in chapters 12, 13, 14 and 15, respectively.

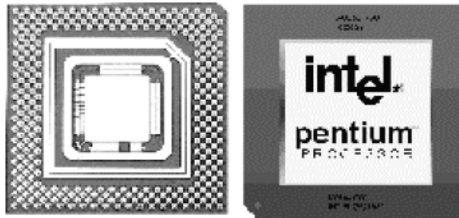


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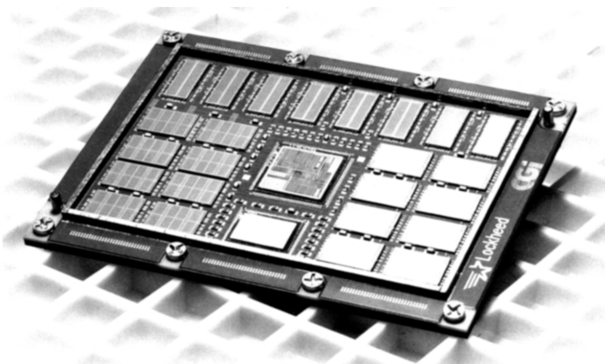
Figure 1-3(a). Single Chip Packaging



(Courtesy Lockheed Martin)

Figure 1-3(b). Multichip Packaging

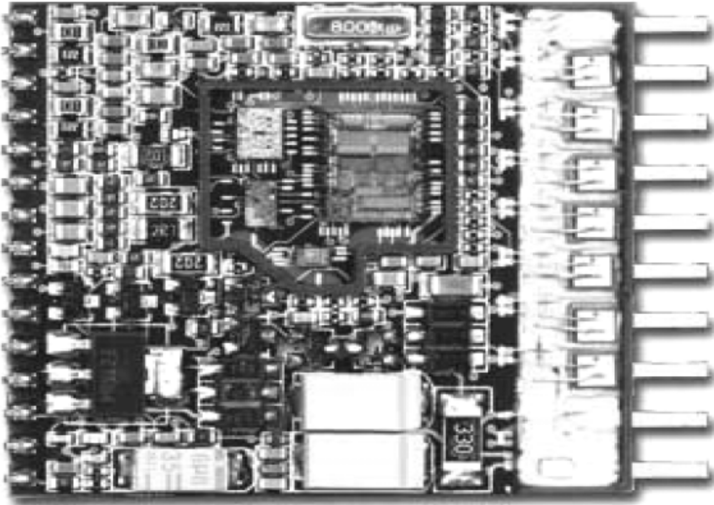


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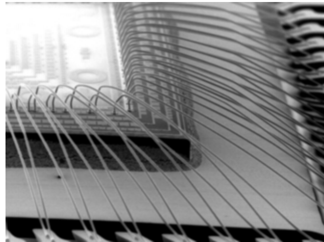
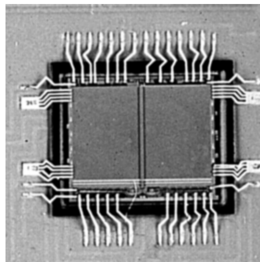
Figure 1-3(c). Chip On Board



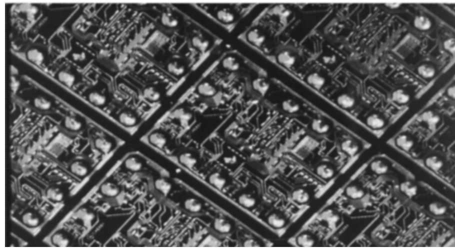
(Courtesy Kulicke & Soffa)

Figure 1-4(a). Chip & Wire



(Courtesy International Micro Industries)

Figure 1-4(b). TAB

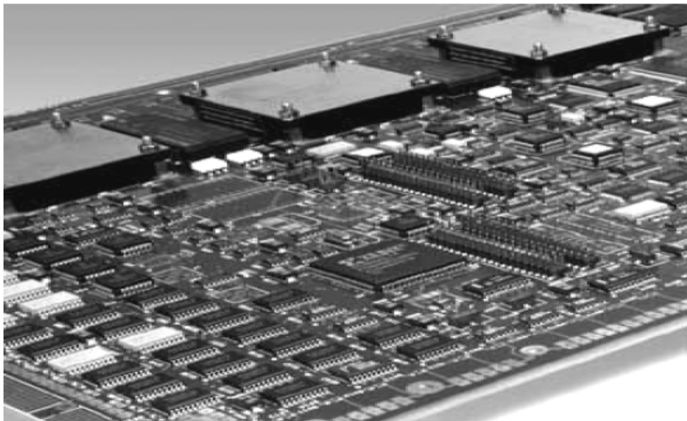


(Courtesy IBM Corp.)

Figure 1-4(c). Flip Chip

- ✓ **Level 2.0**—refers to the interconnection of multiple bare die and/or packages through a substrate interconnect. This is typically a printed wiring board (PWB), an organic based substrate but can also be ceramic. The board, with components attached, is referred to as a printed circuit board (PCB) or a printed wire assembly (PWA). (Figure 1-5).

- ✓ **Level 3.0**—refers to assembly to a PWB (motherboard) of multiple Level 2.0 board assemblies. Again, the motherboard provides the interconnections between assemblies.



(Courtesy IBM Corp.)

Figure 1-5. Printed Circuit Board (PCB) or Printed Wiring Board Assembly (PWBA)

1.3 — A Technology Driver—The Integrated Circuit

Obviously packaging must address the needs of the IC, accommodating the performance and/or reliability. In doing so, not only the packaging, but also the device assembly is impacted.

The IC has changed significantly over the years and will continue to do so. As a consequence changes in the packaging and associated assembly processes were necessary and have occurred. Knowing future device needs should therefore be equally important.

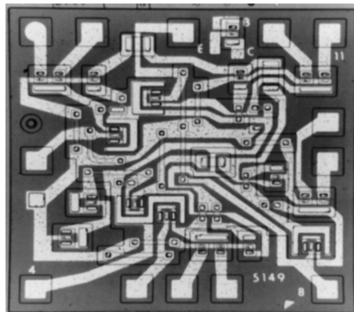
1.3.1 — About the Integrated Circuit

Silicon (Si), Gallium Arsenide (GaAs) and Silicon Germanium (SiGe) are the semiconductor materials currently available and used in IC manufacturing. However, the overwhelming majority of ICs are still silicon based.

Fabrication of the IC involves sophisticated materials, processes, and highly specialized and dedicated equipment that have been developed over a period of 40 years. Because the IC contains features as small as tenths of micrometers (microns, μm) and nanometers (nm), an ultraclean manufacturing environment is necessary to minimize the presence of the many "contaminants" that can adversely affect the manufacture. Yield is a critical process metric that dictates the eventual cost of these functionally dense and sophisticated devices.

1.3.2 — The Integrated Circuit—Physical Characteristics

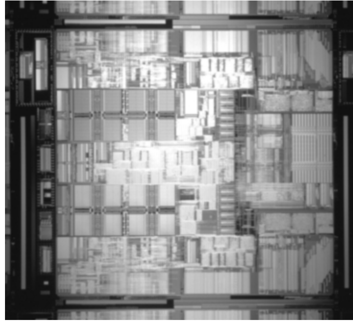
Figure 1-6 is a photograph of an IC manufactured in the late '60s with minimum feature size in the 10-micrometer range. Individual transistors are readily discernible under low magnification interconnected by a single level of aluminum (Al) metal. The minimum line width for the Al interconnect is 20 micrometers. Aluminum metallization interconnects the many transistors that make up an IC.



(Courtesy RCA)

Figure 1-6. IC circa 1970, Single Level Al Metallization ≈ 20 Micrometers Minimum Line Width

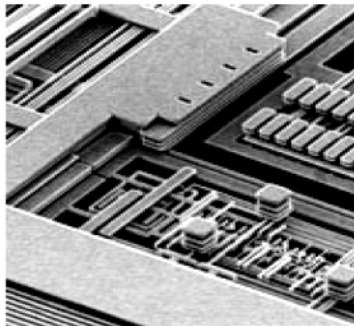
ICs currently in high volume production, Figure 1-7(a), have feature sizes as small as 100 nanometers with several layers of interconnecting metallization. The trend, particularly for the very high performance, high-speed devices, is to use copper instead of the traditional Al metallization because of the higher conductivity of copper, Figure 1-7(b).



(Courtesy IBM Corp.)

Figure 1-7(a). IC circa 2000, Multilevel Metallization

All of this, the decreasing feature size, the increased functional density and performance, has been achieved with the starting silicon wafer going from 25 millimeter (mm) diameter to 300 mm. Smaller feature size and larger wafers mean more die being realized through common processes. And more die per wafer equates to lower cost per device.



(Courtesy IBM Corp.)

Figure 1-7(b). SEM Photomicrograph Multilevel Copper Interconnect, Minimum Line Width ≈ 2 micrometers

Increased functional density means increased complexity. As a consequence the number of photomasks, the major tool needed to manufacture the IC, has increased from less than 10 to 30 and more.

To illustrate, using the Intel microprocessor as the example, the number of transistors on the 4004 in 1971 was 2,250. For the Pentium 4, introduced in 2000, the transistor count is 42,000,000.

1.4 — The International Roadmap for Semiconductors (ITRS) [9]

Prior to roughly the mid '80s, packaging of the IC was of little concern. However, with the arrival of Very Large Scale Integrated Circuits (VLSICs), such as the Intel 486 microprocessor, it became evident that improper packaging of the IC could in fact seriously limit device performance, and in some cases degrade reliability as well. To address this issue properly, it should be obvious that knowing the inherent characteristics of *present and future* ICs and the relevance of those characteristics to packaging and assembly is of extreme importance.

The best source for acquiring this information is through the International Technology Roadmap for Semiconductors (ITRS) [9,10]. This readily available and frequently updated document provides a roadmap presenting an assessment of the semiconductor industry's technology requirements based on the continuing development of the IC. It is compiled through the cooperative effort of global industry manufacturers and suppliers, government organizations, consortia, and universities. ITRS identifies the technological challenges and needs facing the semiconductor industry typically over a 15 year time period.

The ITRS also conveniently breaks out the various Product Sectors, or areas of application, within the industry. These are identified as:

- Low Cost—<$300 watches, calculators
- Hand-Held—<$1000 camcorders, cell phones
- Cost-Performance—<$3000 desktops/laptop computers
- High-Performance—>$3000 space, military, medical electronic
- Harsh Environments—automotive, deep well sensors
- Memory—DRAMS, Static Random Access Memories (SRAM)

Table 1-1 is taken directly from the 2005 report and shows major characteristics for current and future (projected) ICs.

The data presented clearly indicates that the number of I/Os will increase along with increased functionality. The I/O count therefore can be expected to influence the packaging and assembly. For example, the impact of accommodating high I/Os affects the layout of the chip itself; the first level interconnects, that is, the chip assembly; the physical package itself; and the Level 2 interconnect boards.

Table 1-2 is also from the 2005 Roadmap and presents the anticipated increase in I/O count into the next decade by product sector.

Table 1-1. Overall IC Characteristics (ITRS Technology Roadmap (ITRS 2005))

	2001	2004	2007
Feature Size (μm)	0.18	0.12	0.10
Gates/Chip	5	10	20
Bits/Chip			
-DRAM	1G	4G	16G
-SRAM	256M	1G	4G
Wafer Processing Cost ($/cm^2)	$3.70	$3.60	$3.50
Chip Dia. (mm)	20–400	200–400	200–400
Defect Density (defects/cm^2)	0.01	0.004	0.002
No. of Interconnect Levels—Logis	5–6	6	6–7
Max Power (W/die)			
-High-Performance	40	40–20	40–200
-Portable	4	4	4
Power Supply Voltage (V)			
-Desktop	2.2	1.5	1.5
-Portable	1.5	1.5	1,5
No. I/Os	2,000	3,500	5,000
Performance (MHz)			
-off chip	250	350	500
-on chip	500	700	1,000

Table 1-2. Single Chip Pin Count (ITRS 2005)

Year of Production	2010	2015	2018
Low Cost	208–777	325–1213	421–1576
Cost-Performance	780–2782	1216–4339	1581–5642
High-Performance	4009	6402	8450
Harsh	642	934	1235

1.4.1 — Impact of I/O Count at Chip Level

An increase in number of I/O pads, the result of increased functionality, requires a significant change in the physical layout of the IC. Accommodating I/O count means changes in the IC's I/O pad size, pitch and overall format. Traditionally, I/O pads have been positioned along the perimeter of the chip, 100 micrometers square on 200-micrometer pitch. This peripheral format has always been ideal for chip and wire assembly and as a result a huge infrastructure to support this technology is currently in place. However in order to accommodate very high I/O without adversely disrupting the in-place infrastructure requires changes to be implemented. Options available are basically limited to smaller pad size and pitch and/or two or even three staggered rows of peripheral pads.

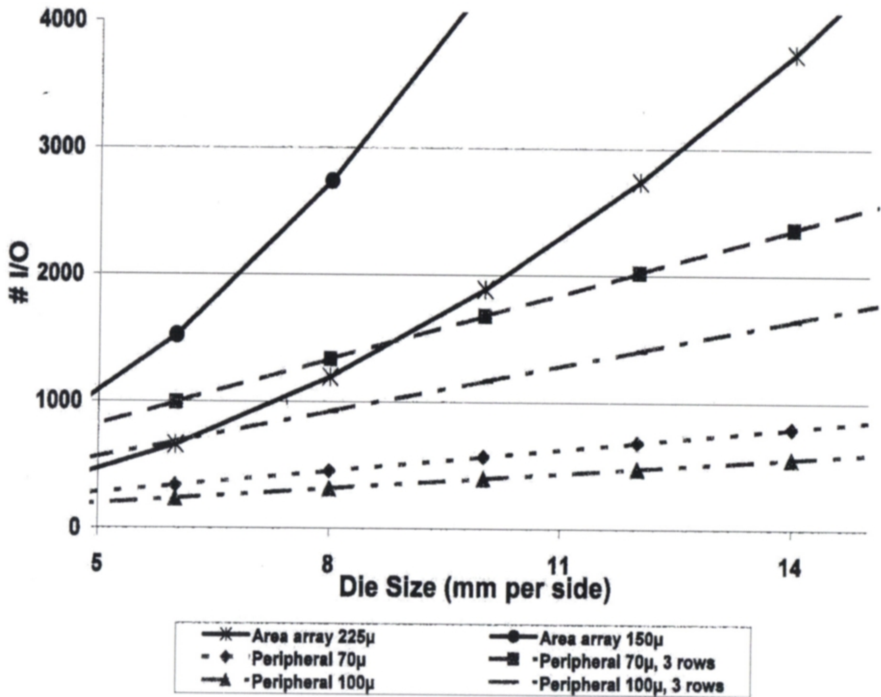
Each change, however, generates other problems. For example, the main concern with peripheral format is that the number of I/O pads needed cannot be allowed to dictate the final chip size. Chip size must be based on active circuit area requirements only. Multiple rows will provide additional I/Os but results in larger die. This in turn means fewer die per wafer and therefore a higher cost per device.

The I/O counts at the levels indicated in Table 1-2 for the Cost-Performance and High-Performance sectors covering microprocessors (μP), digital signal processors (DSP) and Application Specific Integrated Circuits (ASICs) are significant and effectively dictates a necessary shift from peripheral I/O pad format to area array (Figure 1-8(a)) that allows the entire surface of the IC to be used for I/O pad terminations.

Figure 1-8(b) shows the number of I/O that can be accommodated for a given chip size for a peripheral layout at various pad pitch versus an area array.

The single row peripheral format is designed specifically for chip & wire assembly. To accommodate higher I/O count, smaller pads on smaller pitch and multiple staggered rows were introduced. An area array format at the chip level easily accommodates significantly higher I/Os at the chip level emerging as a face down bonded first-level assembly. Further discussions of chip & wire and flip chip are contained in Chapters 9 and 11, respectively.

Figure 1-8(a). Peripheral and Area Array I/O formats



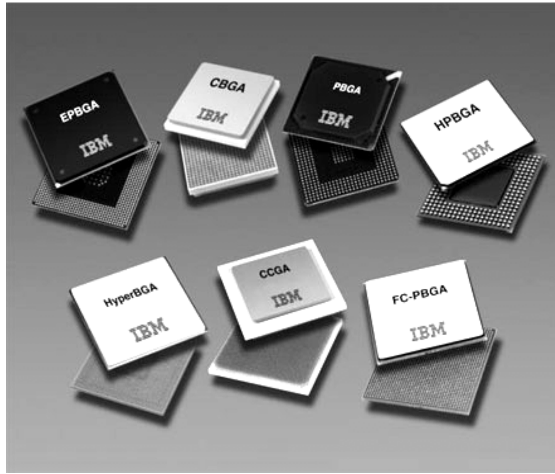
(Courtesy Die Products Consortium)

Figure 1-8(b). I/O Capabilities: Peripheral Format vs. Area Array

1.4.2 — Impact of I/O on the Package

The effect of increasing I/O on the IC package has a similar effect as on the chip namely, a switch to area array. Area array format packages include Pin or Pad Grid Arrays (PGA), and Ball Grid Arrays (BGA) (Figure 1-9).

While accommodating the high I/O count, area array also requires a smaller footprint on the PWB. This effectively increases the packaging efficiency at the board level. The entire attachment process to the PWB is also simplified with the BGA vs. leaded packages such as the Quad Flat Packages. However, higher I/O count packages may require more sophisticated PWBs with finer lines and spaces and higher wiring capability The cost and availability of such boards are a serious concern. It can be a potential roadblock to the use of not only high I/O count BGAs, but Chip Scale Packages (CSPs) and flip chip, technologies that fully support, to various degrees, “smaller, better, cheaper” objectives. Packaging of the IC is addressed in more detail in Chapter 3.



(Courtesy IBM Corp.)

Figure 1-9. Area Array Packages—BGAs

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2 Integrated Circuit Manufacturing: A Technology Resource

2 — IC MANUFACTURING TECHNOLOGIES

While the integrated circuit drives the packaging and assembly, the IC manufacturing process, and associated methodologies, serves as an invaluable technology resource. IC manufacturing is made up of a "Front End" and a "Back End". The "Front End" encompasses the actual fabrication of the IC and is most often referred to as "Wafer Fab". The "Back End" covers subsequent packaging, assembly, and testing of the IC. Many of the materials, the processes, procedures, and equipments, particularly those associated with the photolithography, have direct application to relevant packaging and assembly needs.

Areas of application for these types of methodologies supporting current and future IC packaging and assembly include:

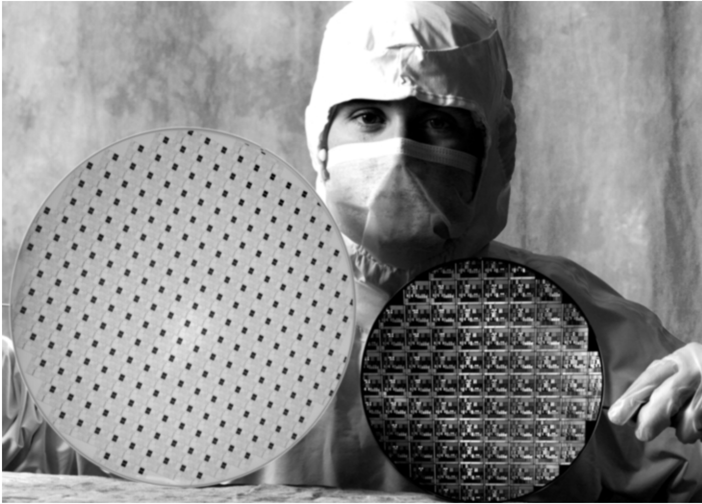
- Wafer bumping for TAB and flip chip,
- Wafer Level Packaging (WLP) for Chip Scale Packages (CSP),
- Interconnect Substrates for MCPs, and
- Level 2 High Density Interconnects, HDI PWBs.

The IC photolithographic process and the above applications share the same basic technology for pattern transfer. The inherent advantages of much of the IC methodologies can best be assessed by first reviewing the various processes emphasizing some of the important "lessons learned" and secondly (and perhaps more importantly) their significance and impact on yields and cost-effective manufacturing.

2.1 — Overview of the IC Manufacturing Processes [1–4]

An IC is fabricated in a wafer format. Multiple ICs are manufactured simultaneously on a single wafer. Today wafers are processed in 6", 8" and 12" diameters (Figure 2-1). When completed, a wafer can contain literally hundreds or thousands of ICs. Larger wafers produce more devices and since the cost to manufacture changes little with size, the cost per IC is less. This of course assumes yields are maintained in the transition from smaller to larger wafers. The switch to the larger wafer, however, is also costly, typically involving a rather significant investment in new process equipment capable of handling the larger size wafers. The current 12" wafer

is projected to remain in place through the next decade. Most major semiconductor houses, which in the U.S. include Intel, Texas Instruments and Freescale Semiconductor (formerly Motorola), are now processing 12" wafers. The 6" and 8" wafers are found in the foundries. Foundries are facilities that provide wafer manufacturing services to “fab-less” ASIC design houses.



(Courtesy IBM Corp.)

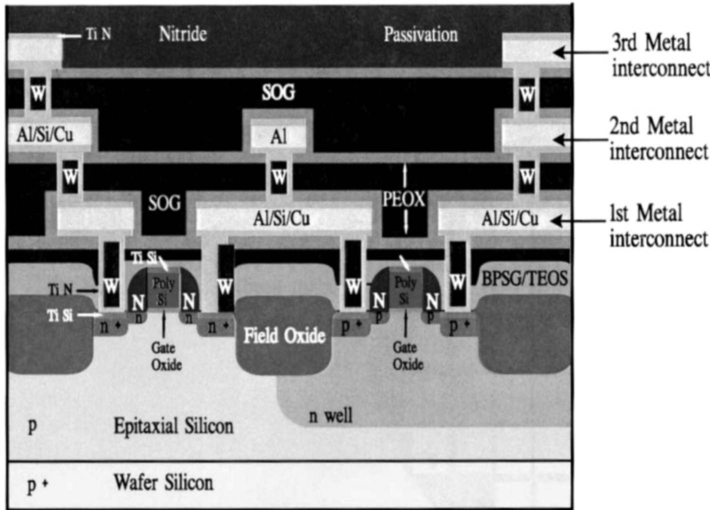
Figure 2-1. A 300 mm (12") and 200 mm (8") Diameter Silicon Wafer

The IC, basically a multilayered structure (Figure 2-2), is fabricated in a sequential process. Controlled impurities that create the active transistors are first embedded in the silicon using processes such as oxidation, ion implantation, and diffusion. This is followed by the deposition of conductor and dielectric materials that form a multilevel conductor network. The network literally interconnects the millions of embedded transistors that may be contained within a single IC. This multilevel conductor network terminates at metallized bond pads on the surface of the IC that allow for access to the outside world when the IC is assembled into a package.

Each layer within the structure shown must be properly defined using a pattern-transfer process wherein an image on a photomask is transferred onto the surface of a wafer. To complete an IC as many as 25 or more photomasks, each containing a different image, are required.

Because of the many steps involved in the manufacture of the IC major problems arise resulting in the loss of functional devices. This adversely affects overall yield of devices and directly impacts manufacturing costs. Devices are lost because of defects and contamination introduced during manufacture.

The processes currently in place have evolved over the years from a continuing and dedicated effort directed towards one objective, that is, *to eliminate or minimize generation of defects and contaminants at each and every step in the manufacturing process and thereby optimize yields.*



(Courtesy PTI Seminars, Inc.)

Figure 2-2. Schematic Cross-Section of a Si Integrated Circuit

Major sources of defects are particulates in the operating environment, the materials and processes themselves, the equipment, and associated fixtures and tooling. In addition, operator involvement during manufacture can be a further contributor to yield loss due to improper dress, procedural errors and mishandling of wafers.

Identification of the various sources of defects and their elimination has resulted in many changes. As IC feature sizes began to rapidly decrease and complexity increased, critical changes were needed. These included, most notably,

- Strict control of the manufacturing environment and operator protocols, and
- Continuing development of "near defect-free" photolithographic processes covering the photomask and the exposure/imaging/printing equipment and tooling.

2.2 — The Manufacturing Environment [5–6]

With decreasing feature size it became obvious that "particulates" contained in normal room air, when inadvertently deposited on the wafer could create a defect that would result in loss of one or many ICs. A "cleanroom" operating environment to control the particulates in the air was essential. The level of control required changed with each generation of IC. *The level of cleanlines, and degree of controls are dictated by the particular process and device requirement, e.g., minimum feature size*. Table 2-1 lists levels of cleanliness for cleanrooms and defines particle sizes and limits. The lower the classification number the higher level of control both as to the size and the number to be found in a given volume of air.

Table 2-1. Cleanroom Classifications [US FED STD 209E Cleanroom Standards]

	Maximum Number of Allowable Particle of Indicated Size per ft^3					
Class	0.1 µm	0.2 µm	0.3 µm	0.5 µm	1 µm	5 µm
1	35	7	3			
10	350	75	30	10		
100		750	300	100	10	1
1,000				1,000	100	10
10,000				10,000	1,000	100
100,000				100,000	10,000	1,000

Other sources of contaminants to be controlled include process chemicals, bacteria from process water, metallic ions found in process chemicals. and operator and equipment related static discharge. High purity, high resistivity (18 megohms) deionized water (treated to remove metallic ions) is used extensively during IC manufacturing supporting the many rinsing and cleaning operations. Special plumbing and the use of filters insure removal of damaging particles. In addition, harmful bacterial contamination is removed by an ozone or ultraviolet light exposure treatment. Process chemicals are similarly subjected to much the same types of treatments and controls.

Control of the room temperature (T) and relative humidity (RH) is also an essential part of any cleanroom operating environment. Lack of control of T and RH can adversely effect both materials and equipment and contribute to critical process irregularities. This is of particular significance in the photolithographics area where materials like photosensitive resists and associated processes are affected. And, because resist materials are sensitive to ultraviolet (uv) light, all photolithographic processes are performed in a room with special lighting (yellow lighting) that eliminates unintentional but damaging exposures.

The “Back End” cleanroom requirements however, are quite different. Levels of control are orders of magnitude greater for “Front End” than “Back End”. “Back End” processing is usually maintained in a Class 1000 and higher operating environment. Early cleanrooms were Class 100. Today IC wafer fab is performed in Class 1 cleanrooms. And, to further enhance the level of cleanliness, special processes, e.g. the photolithographic processes, are performed in separate enclosures within the cleanroom (Figure 2-3).

2.2.1 — Operator Protocols

Strict operator protocols were also instituted and incorporated including,

- Special training covering proper handling and storage of wafer,
- The wearing of special cleanroom garments, and
- Well-defined cleanroom operating procedures.

(Courtesy National Semiconductor)

Figure 2-3. A Class 1 Cluster Cell within a Class 10 Cleanroom

(Courtesy IBM Corp.)

Figure 2-4. Robotic Wafer Handling

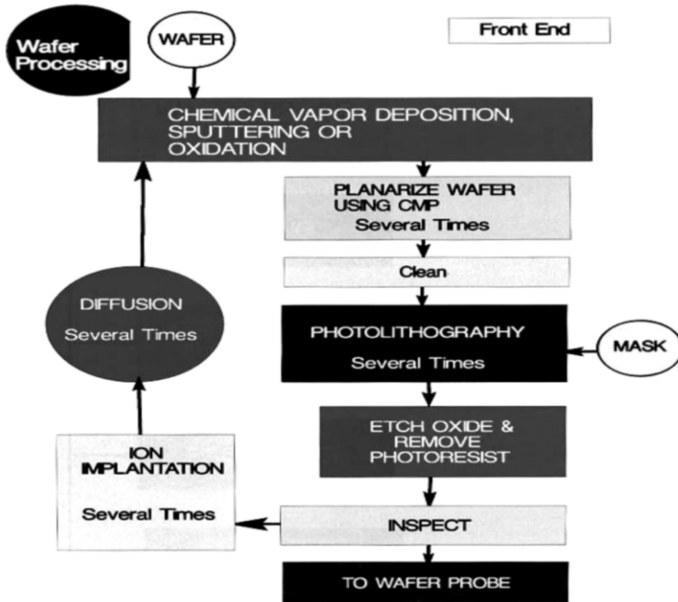
In Wafer Fab operators are required to wear gowns worn specifically to eliminate particulates that could be introduced by the operator and the operator's personal clothing.

Use of "robotics" (Figure 2-4) as well as other automated wafer handling equipment and fixturing are implemented to minimize, wherever possible, operator intervention and potential operator induced damage resulting from mishandling and electrostatic discharge.

2.3 — The Photolithographic Process [7]

The basic manufacturing processes, shown in Figure 2-5, can be grouped as follows:

- Deposition Processes—including Oxidation, Diffusion/Ion Implantation, Chemical, Vapor Deposition (CVD), Sputtering
- Photolithography—Exposure (Printing, Imaging), Developing, and
- Pattern Transfer—including Etching and Plating



(Courtesy PTI Seminars, Inc.)

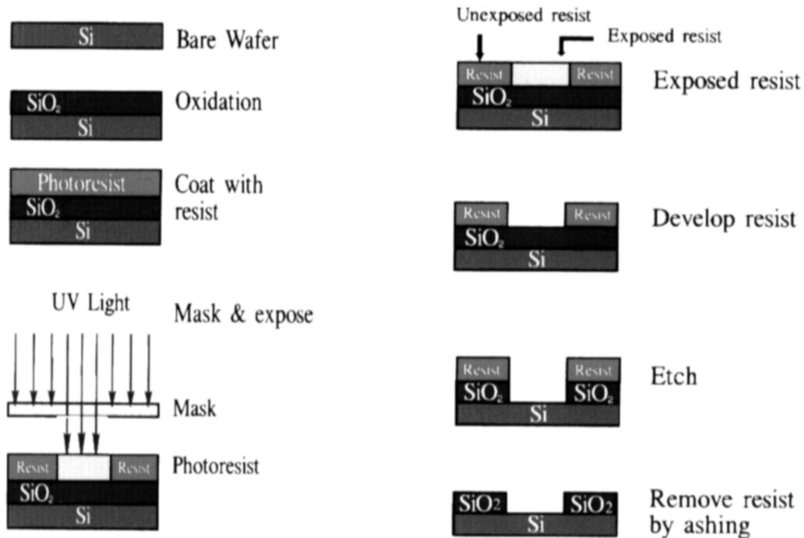
Figure 2-5. Si Wafer Fab, The Front End Processes

Photolithography is a multi-step pattern transfer process that covers:

1. Application of a photosensitive material (photoresist or resist) to a wafer or substrate.
2. Patterning of the resist by exposure to a UV light source through a patterned photomask.
3. Completion of the pattern transfer by immersion of the exposed resist in a developer.
4. Using the patterned resist as a mask for chemical etching of exposed metals or dielectrics, or as a template for selective deposition of a metal by a plating process.

2.3.1 — The Basic Pattern Transfer Process

The IC photolithographic process for pattern transfer is highly sophisticated and has been designed to ensure "near zero defects" and high yield of ICs with feature sizes in the 100-nanometer range. The basic process is shown in Figure 2-6.



(Courtesy PTI Seminars, Inc.)

Figure 2-6. The Basic Pattern Transfer Process

It begins with the application of a photoresist film that when patterned, will function as either an etch mask or as a template, to selectively deposit a metal by plating. Figure 2-6 shows the "etch" or "subtractive" process for patterning a silicon dioxide (SiO_2) layer to be used as a mask for the introduction of impurities into the silicon to form the transistors.

Basic to the process is:

- The photomask,
- The photosensitive resist film, and
- The mask aligner/exposure/printer equipment.

2.3.2 — Photolithographic Tooling—The Photomask/Reticle [8]

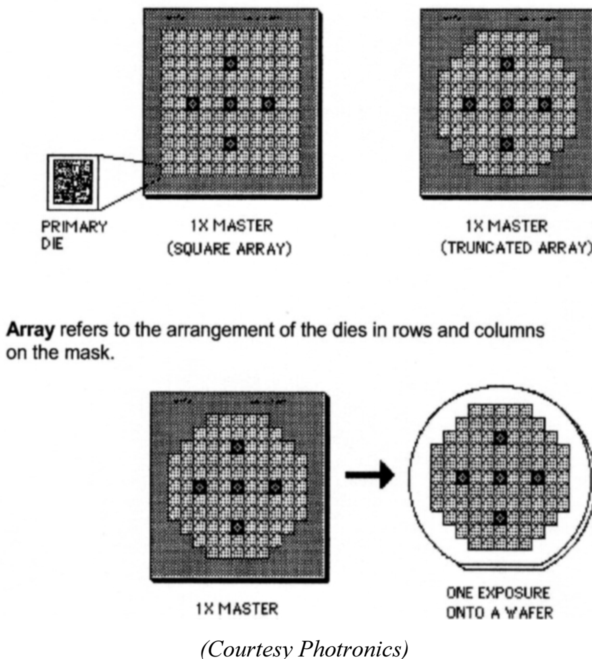
The primary tool and the most critical item in the photolithographic manufacturing process is the photomask. As used in the manufacture of the IC it is typically a high quality, high precision glass or quartz plate. Glass is used because it is not easily damaged and is extremely stable—not susceptible to dimensional changes when subjected to variations in room temperature and relative humidity. Patterned images on the glass mask are an opaque chromium or Al film. The hard surface chrome is highly durable and yields patterns with exceptionally sharp edge acuity insuring well-defined image transfer.

Mask manufacture, therefore, is just as critical as that of the actual IC. The transferred patterns simply *cannot be better* than the patterns on the photomask. As many as 25+ different patterns (photomasks) are typically required to manufacture an integrated circuit. A defective pattern on any mask results in a defective die. Hence each mask must be of the highest quality, and ideally, free of defects to insure the maximum possible yield. Insuring a defect free photomask requires that each and every pattern on a mask be critically inspected. Performed by an operator, it is labor intense and subject to error. Today, automatic optical mask inspection equipment allows for 100% inspection of each and every image on a mask. While all patterns on a multi-image mask may not be completely defect free, the inspection can help identify useable masks that are repairable or are at an acceptable defect level for use in production. The mask manufacturing process sequence is shown in Appendix B.

The mask image is pattern transferred using the same basic processes described in Figure 2-6 with multiple in-process inspections and measurements included to insure precise replication of the image as derived from a computer automated design (CAD) database. All mask manufacturing is accomplished under the same operational enviroment and operator protocols as the IC.

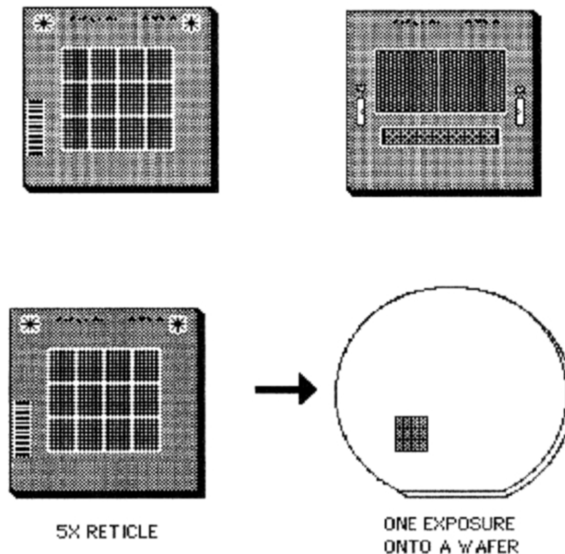
2.3.3 — Types of Photomasks

There are basically two types of photomasks: the array mask and the reticle (Figures 2-7(a) and (b)). The area array mask contains multiple sites each with the same pattern or image.



(Courtesy Photronics)

Figure 2-7(a). An Array Photomask



(Courtesy Photronics, Inc.)

Figure 2-7(b). A Reticle

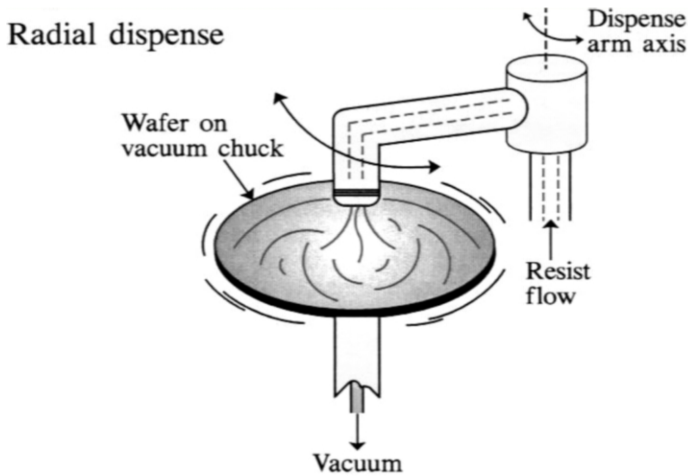
The reticle is a photomask that is specifically intended for use in projection printers, specifically wafer steppers, and contains a single image or a grouping of the same image. The images can be 1X, 2X or 10X of the final feature size to be transferred onto the wafer.

Reticles offer several advantages compared to array masks particularly in regard to inspect for defective images. Since there is only one or a few images, inspection times are significantly reduced. Similarly, with magnified images inspection is further simplified enabling "near-perfect" masks to be presented into manufacturing.

2.3.4 — Photosensitive Materials (Photoresists) [9]

In IC manufacturing the photosensitive film deposited on the Si wafer is liquid and is applied by dispensing. Graphically represented in Figure 2-8, it shows a wafer mounted on a vacuum chuck that can be rotated at very high rpm. The dispensing can be done while the wafer is either stationary (dynamic) or rotating (radial). Similarly the dispensing arm can be fixed or moved across the wafer. The volume of resist dispensed must be sufficient to insure complete coverage of the wafer. Following application the resist is cured to form a hard coating. It is then exposed through a photomask and developed to complete the patterning of the resist. The resist is now ready for the etching process.

When a metal conductor is to be patterned, the final thickness of the resist is critical. As an etch mask it must be of sufficient thickness to insure complete removal of unprotected metal. The final thickness of the resist will be determined by



(Courtesy PTI Seminars, Inc.)

Figure 2-8. Deposition of Liquid Photoresist by Spinning

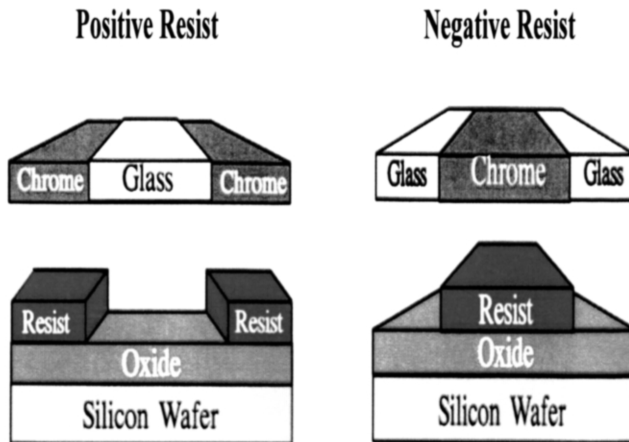
the viscosity of the resist and the rotational speed of the chuck. This thickness is typically the same or slightly greater than the thickness of metal to be etched. For IC metallization, it is normally 1 μm or less in thickness.

There are other alternative resist materials and coating processes available but they are not necessarily employed in the manufacture of the IC. These include spray coating of liquid resist, dry film resist and electrodeposited spray coating. Thicker resist films are better suited for packaging and assembly applications such as bumping and HDI substrates, where metals are several microns thicker than the IC metallization. These are discussed further in Chapter 12.

2.3.5 — Types of Photoresist

There are two types of photoresist materials: a positive acting resist and a negative acting resist. When a positive resist is exposed to uv light of the proper wavelength it undergoes what is referred to as photo-softening and upon developing in a water based solution is completely removed. If a photomask is used during exposure the same pattern on the mask will be transferred to the resist film. With negative resist the reverse takes place. Exposure to uv light results in a photo-hardening or photo-polymerization of the resists. Thus the pattern transferred to the resist will be a reverse tone of the pattern on the mask. The two processes are illustrated graphically in Figure 2-9, and Table 2-2 compares the salient features of each.

Positive resist is used extensively in most IC patterning process, offering several advantages over negative resist, not the least of which is it is environmentally friendly. It also has inherently superior fine feature size capability and is used exclusively whenever line widths less than 1.5 μm are required.



(Courtesy PTI Seminars, Inc.)

Figure 2-9. Positive and Negative Acting Photoresist

Table 2-2. Comparison of Positive and Negative Resists [7]

Positive Resist	Negative Resist
Photo-softening	Photo-hardening
Environmentally Friendly	Biological Hazard
Developer—water based	Developer—solvent based
Fine Line Capability << 1μm	Features < 1μm
Cost—expensive	Cost—low, << positive
Adhesion—poor (requires use of primer)	Adhesion—good (no primer required)

2.3.6 — Exposure Systems for Printing/Imaging

The most common exposure system, (Figure 2-10) consists of an ultraviolet light source and a substrate or wafer holder. When a mask holder and precision stages are added, permitting movement of the substrate and/or photomask for alignment purposes, the system becomes a msk aligner.

Over the years new exposure systems/mask aligners were developed. Each new system addressed elimination of process/equipment generated defects. The various systems used in IC manufacture and the attributes of each follows.

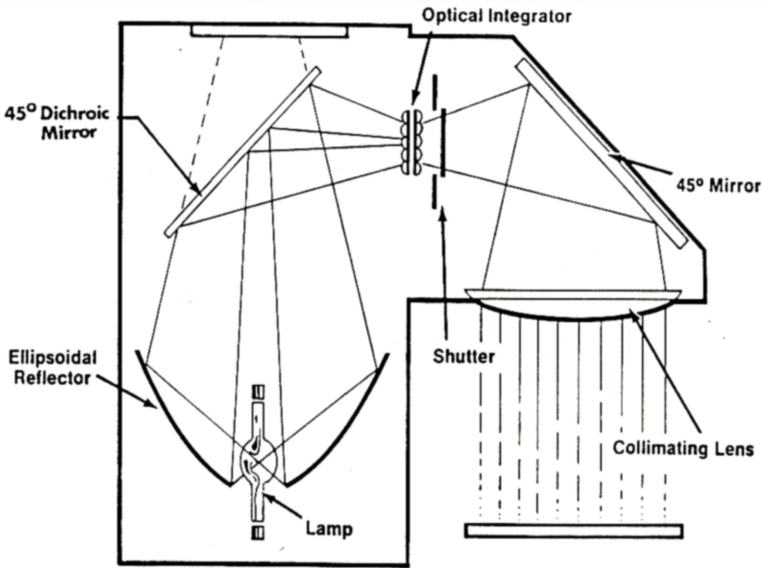
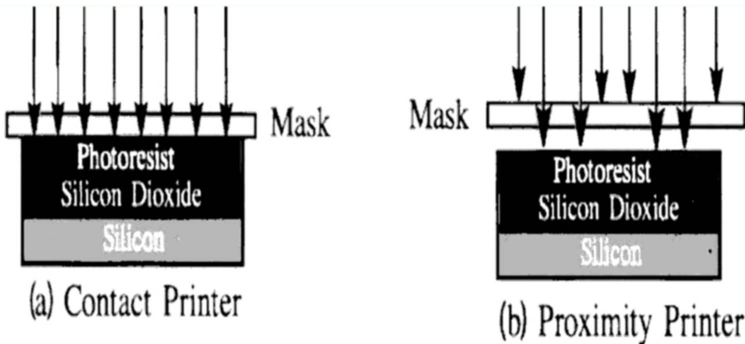


Figure 2-10. The Basic Exposure System [9]

2.3.6.1 — Contact and Proximity Printer

Figure 2-11 schematically illustrates both the contact printer and the proximity or off-contact Printer.

The (contact printer Figure 2-11(a)), was the exposure system in use in early IC manufacturing. For optimum image tranfer from mask to resist, positive contact of mask to the coated wafer is necessary and must be maintained during the entire exposure cycle. This results in damage both to the mask and the resist coating that translates to defective patterns on the wafer and loss of yield.



(Courtesy PTI Seminars, Inc.)

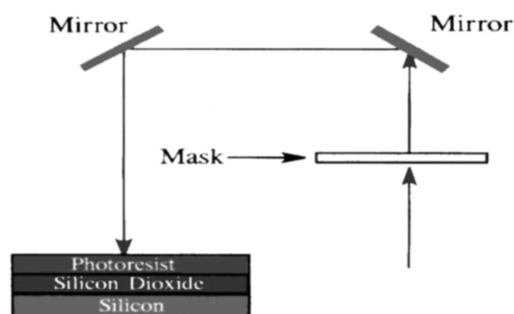
Figure 2-11. (a) Contact Printer; (b) Proximity Printer

To eliminate this problem, the proximity or off-contact printer, (Figure 2-11(b)) was developed. With the mask separated from the wafer (approximately 25µm/ 0.001") damage to the mask and the resist was greatly minimized. However proximity printing resulted in loss of resolution versus contact printing.

2.3.6.2 — The Projection Printer

To address this particular problem, the projection printer, Figure 2-12, was developed.

The projection printer has the photomask completely removed from the wafer. The mask image is optically projected onto the wafer. This is accomplished with greater resolution than achievable with contact printing. The photomask itself is a standard array mask the same as used in contact or proximity printing. The projection printer *totally eliminates* damage to either the mask or the resist coating on the wafer.



(Courtesy PTI Seminars, Inc.)

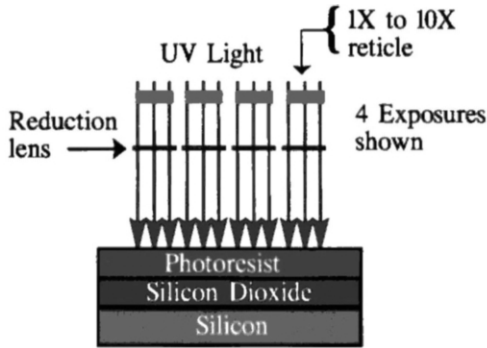
Figure 2-12. Projection Printer

The introduction of a projection printer by Perkin Elmer in the '70s represented a significant advancement in wafer fabrication technology and stands out as a major contributor to the continued development and producibility of ICs with minimum features down to the micron and submicron range, and with exceptionally high yields.

2.3.6.3 — The Wafer Stepper and Step and Scan Projection Systems

Further developments in projection printing are shown in Figure 2-13. In this case, the standard array photomask is replaced by a reticle that contains a single image at 1X. Only one site is exposed to uv at a time. The wafer, which is mounted on a computer controlled x-y table, is programmed to step to the next adjacent site following each exposure. This is repeated until the entire wafer has been exposed. This type of exposure system is known as a "Wafer Stepper".

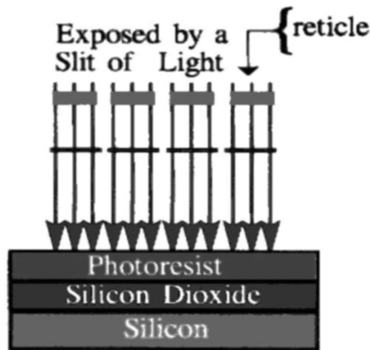
The single image reticle can also be a magnified image up to 10X. Magnified images are optically projected and reduced to 1X at the wafer using a reduction lens inserted in the optical path as shown in the figure.



(Courtesy PTI Seminars, Inc.)

Figure 2-13. The Wafer Stepper Projection System

The "Stepper", in turn, also underwent further development. Since this is a sequential process, it is time-consuming. To overcome this drawback more than one site was added to the reticle and a section of the wafer instead of a single site was being exposed. This "Step and Scan" mode is illustrated in Figure 2-14.



(Courtesy PTI Seminars, Inc.)

Figure 2-14. The Step and Scan Projection System

2.4 — IC Methodologies and Packaging, Assembly, Interconnections

Application of IC process methodologies, aka, the Thin Film process, when applied to packaging, assembly and interconnections, can provide the needed cost-effective, high yield, high density wiring capability. For wafer bumping and WLP, where finished wafers are involved, and where the "added value" is at an absolute maximum, yield loss is untenable and extremely costly. "Near defect-free" processing is therefore essential. When the thin film technology is combined with thick film, cofired ceramic and the laminate PWB manufacturing technologies

(Chapters 13, 14 and 15), it provides for an enhanced capability that effectively extends areas of application for each of the respective technologies.

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3 Packaging the IC—Single Chip Packaging

3 — THE IC PACKAGE [1,2]

Starting with the transistor, the package has functioned as both a carrier and as an enclosure. As a carrier it allows the device's functionality to be fully accessed and to be assembled and electrically interconnected to other devices (Level 2.0). As an enclosure it provides protection from physical damage and a supportive and controlled operating environment for the device. The earliest ICs followed the same packaging format as the transistor (a TO-5 metal package) differing only in the number of leads (Figure 3-1).

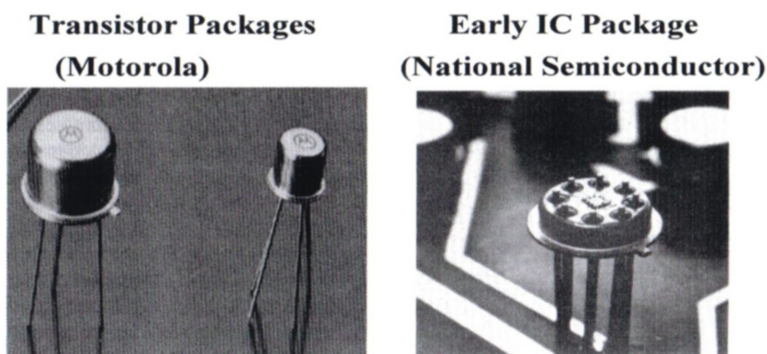


Figure 3-1. Transistor and an Early IC Package (TO-5 Outline)

Physically the package has undergone many changes, responding to the needs of the IC, the end product, and certainly cost considerations. Ideally the guidelines have always been to:

- Provide a package that fully supports the IC, responding to inherent thermal, mechanical and electrical requirements,
- Avoid, if possible, having the package *limit chip performance*,
- Make the package as small as possible, and finally,
- Provide a cost-effective package that does not represent a substantial percentage of the final device's selling price.

3.1 — Trends in IC Packaging [3–4]

Figure 3-2 graphically presents the industry's past history and current trends in IC packages. In particular, it shows the influence of accommodating both increasing I/O count and miniaturization.

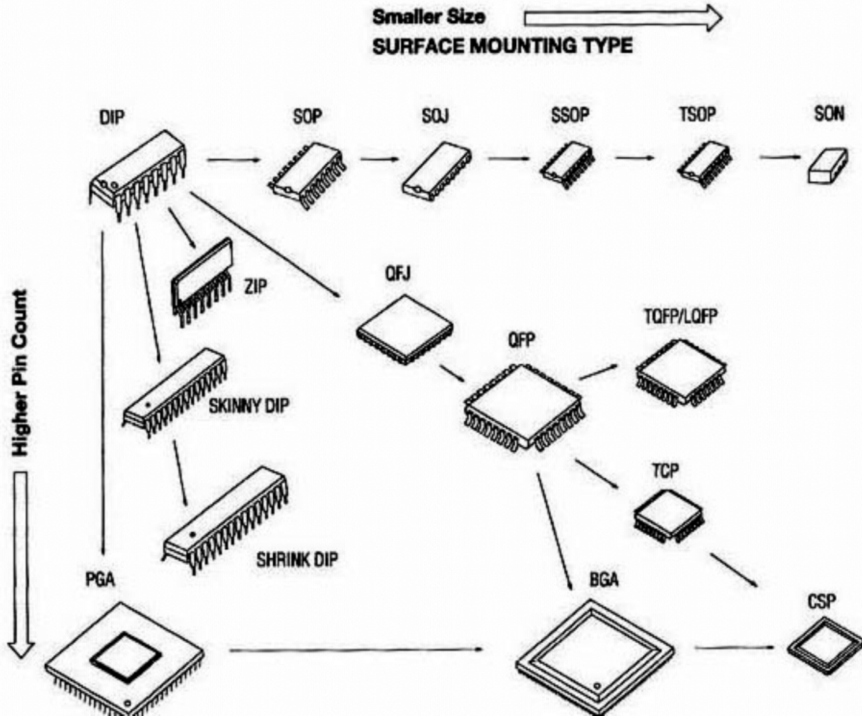


Figure 3-2. IC Package History and Trends

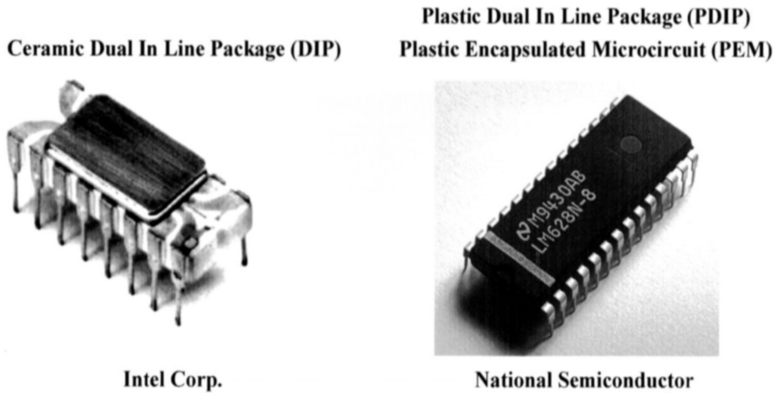
The package miniaturization has been driven by the continuing demand for smaller, better, cheaper end product. Miniaturization is marked not only by a smaller package, but also an improvement in Packaging Efficiency (PE) which is defined as *the ratio of the area occupied by the active device(s), i.e. the Si die and the area required to attach the packaged device to the next level of interconnect, the PWB.*

Higher PE, in turn results in improved device performance at Level 1 and Level 2. At Level 2, the smaller packages means very significant increase in the number of components that can be accommodated per square inch of board area.

3.1.1 — Evolution of IC Packaging—Addressing I/O Count

Increasing I/O count has always been a driver that influenced the package. The metal package gave way early on to a ceramic-based package to better handle the increased I/O count. The ceramic package leads were on 2.5 mm (100 mils) pitch, and more rigid and robust compared to the metal package. The leads were along two opposite

sides, hence the name Dual Inline Package or DIP. In today's world, while some ICs are still packaged in ceramic, the vast majority of ICs (>95%) are now a lead frame based plastic encapsulated package, (a PDIP) also referred to as a Plastic Encapsulated Microcircuit or PEM (Figure 3-3(a)). All Dual Inline Packages were designed for through-hole insertion onto a PWB as shown in Figure 3-3(b).



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(National Semiconductor)

Figure 3-3(a). Ceramic and Plastic Dual Inline Packages

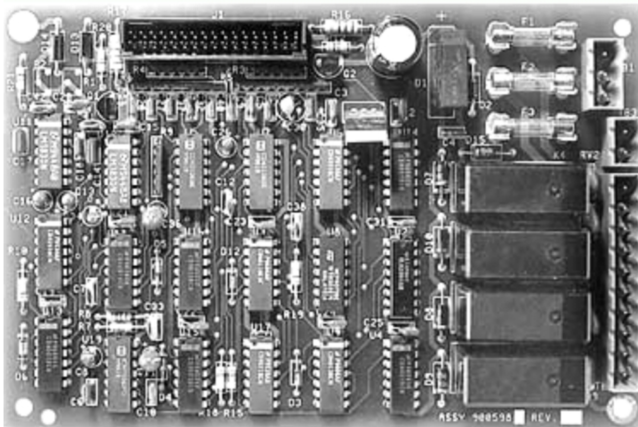
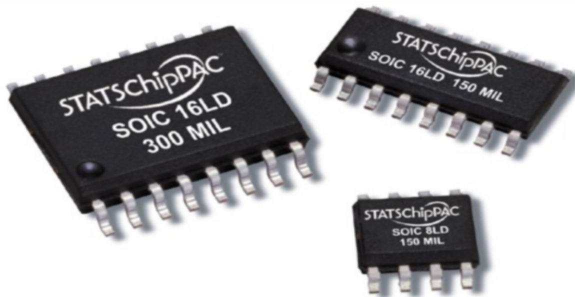


Figure 3-3(b). PCB with Through-Hole Solder Attached DIPs

3.1.2 — The Flat Pack, SMT, and PWB Assembly

Higher I/O counts precipitated the development of the Flat Pack (FP). The flat pack also had leads on two sides but on 1.125 mm (50-mil) pitch to accommodate more than double the I/O count for the same package size.

Perhaps more importantly, the flat pack was not "through-hole" attached but rather was designed to be surface mounted and solder attached to the PWB. This represented a paradigm shift in assembly technology at the board level and opened the door to Surface Mount Technology (SMT). Miniaturized versions of the flat pack are referred to as Small Outline Packages or SOP. One popular package is the SOIC, or small outline IC package, shown in Figure 3-4(a). Making a package smaller is not limited to the x–y dimensions but to the z-direction as well. The TSOP or Thin Small Outline Package, for example, is a thinner version of a SOP.



(Courtesy STATS Chip PAC Ltd.)

Figure 3-4(a). Small Outline IC Packages (SOIC)

3.1.2.1 — Surface Mount Technology (SMT) [5–7]

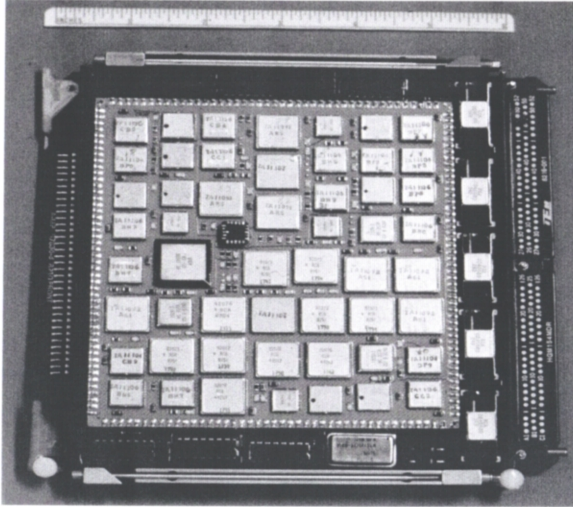
SMT has all components, *both passive and active devices*, solder attached directly to the top surface of the board. It eliminates plated through holes required for the DIP. SMT impacts Level 2.0 assembly, i.e., the PWB, by roughly doubling the component density, increasing the reliability, and decreasing overall cost of the assembled board. Figure 3-4(b) is a PCB with all surface mounted components.

Surface mount devices (SMD) and surface mount assembly allows for cost savings to be realized in board manufacture and component assembly.

For example,

- Through-holes for component attach can be eliminated making manufacture of the board cheaper since the drilling and subsequent plating processes to metallize the through-hole are no longer required. Fewer steps means lower cost to manufacture. In addition to increased component density the wiring density is also increased with board area required for the through-holes now available for routing of conductor traces.

- The increase in packaging and wiring density means the total number of boards required for a complete system can be reduced and,
- Reliability is improved by eliminating plated through-holes and related failure mechanisms and fewer boards required.



(Courtesy Hybrid Sources, Inc.)

Figure 3-4(b). PCB with Surface Mounted Components

3.1.3 — The Quad Flat Pack (QFP)

Further increase in I/O count resulted in the introduction of the Quad Flat Pack (QFP) with leads on all four sides. The QFP, available in ceramic and plastic, PQFP, was also designed for surface mount (Figure 3-5).

(Courtesy STATS ChipPAC Ltd.)

Figure 3-5. Plastic Quad Flat Pack, PQFP

The QFP package quickly became an industry standard. Increasingly higher counts were addressed by reducing the lead pitch. For example, the 50 mil lead pitch gave way to smaller pitch, 20 mil down to 12 mil. Unfortunately, with the finer pitch packages, the assembly and the attachment to the PWB became increasingly more difficult. Alignment and placement problems became more demanding, as did the stencil printing of the solder paste. In addition, the very fine pitch packages often experienced leads shorting because of the reduced spacing between the leads. And of course the problem of maintaining planarity of the leads was magnified, making handling of the packages more difficult.

3.2 — Area Array Packages—PGA, BGA

Use of peripheral pads with increasing I/O count unfortunately meant larger packages This brought about another paradigm shift in package I/O format from the traditional peripheral to an area array layout that allowed pads to be placed within the body (bottom surface) of the package (Figure 3-6).

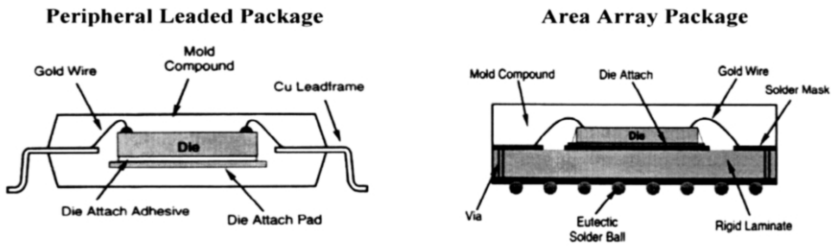
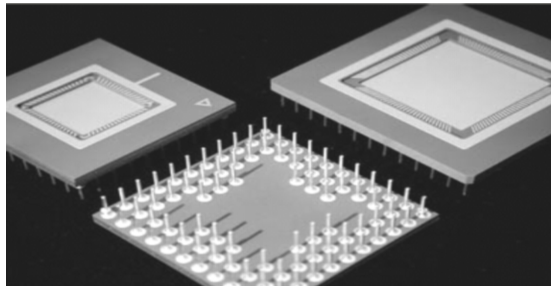


Figure 3-6. Peripheral leaded Package vs. Area Array Package

The earliest area array package was a ceramic Pin Grid Array (PGA) with pins on 100-mil pitch (Figure 3-7). While allowing for a higher I/O count, at the board level (Level 2.0) the PGA needed to be through-hole solder attached or socketed to the PWB. As a result the cost to manufacture the board was significantly impacted by the need for large numbers of through-holes to accommodate the PGA.

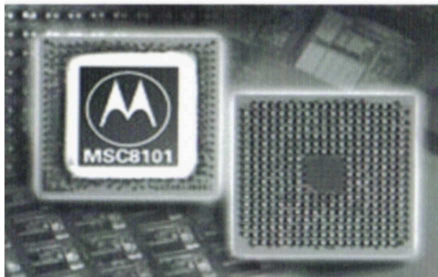


(Courtesy Global Chip Materials)

Figure 3-7. The Pin Grid Array Package (PGA)

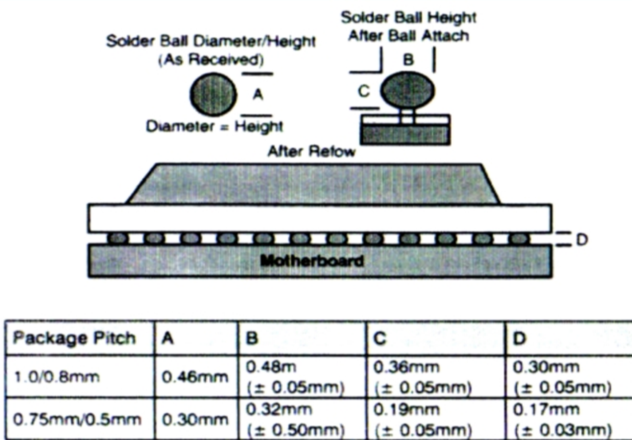
This lead to the development of Ball Grid Array (BGA) packages (Figure 3-8(a)) with solder balls replacing the pins. The BGA, like its predecessors the FP and QFP was totally compatible with surface mount assembly. The solder balls are on a smaller pitch, Figure 3-8(b), ranging from 1 mm (40 mil) down to 0.5 mm (20 mil), totally confined within the body of the package. It immediately presented a much higher I/O count capability for a given package size and it required a smaller footprint for attachment to the Level 2 PWB versus QFPs.

For these reasons area array packages in general, and BGAs in particular, have moved rapidly into mainstream manufacturing.



(Courtesy Freescale Semiconductor)

Figure 3-8(a). BGA Package



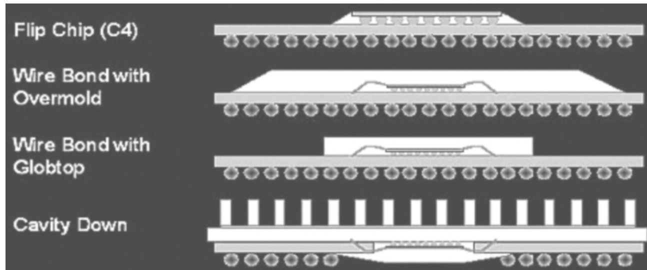
Package Pitch	A	B	C	D
1.0/0.8mm	0.46mm	0.48m (± 0.05mm)	0.36mm (± 0.05mm)	0.30mm (± 0.05mm)
0.75mm/0.5mm	0.30mm	0.32mm (± 0.50mm)	0.19mm (± 0.05mm)	0.17mm (± 0.03mm)

Figure 3-8(b). BGA—Typical Bump Diameters And Pitch

BGAs are available in ceramic as well as plastic and come in many different configurations. Common to all BGAs however, is the substrate interconnects (embedded conductor network) that act as a "transposer" or "bridge" between the chip and the Level 2 PWB. The substrate interconnect can be ceramic, a rigid organic laminate, or an organic tape: a flex circuit.

3.2.1 — The Ceramic Ball Grid Array, CBGA

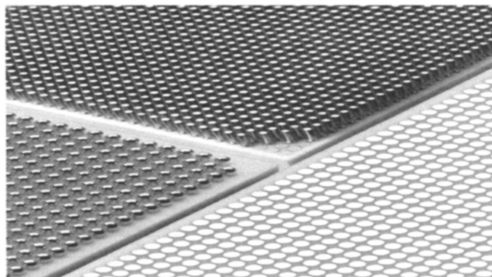
Figure 3-9 schematically shows various ceramic package configurations. The ceramic substrate interconnect is manufactured using cofired ceramic technology (Chapter 14). The die assembly can be Chip & Wire or flip chip. In the cavity down structure shown in the figure, an external heat sink is attached to enhance thermal management capabilities. Packages can be finished by glob topping, or epoxy molding. A further variation allows for a seal ring to be attached providing a fully hermetic cavity enclosure.



(Courtesy IBM)

Figure 3-9. Ceramic BGA Configurations

Ceramic BGAs can be supplied with solder bumps or solder columns (typically high lead 5Sn95Pb) as shown in Figure 3-10. The solder column provides for increased gap between the package and the substrate and greater solder volume. Both add significantly to board level (Level 2.0) reliability.



(Courtesy IBM)

Figure 3-10. Ceramic BGA, Ceramic Column BGA, Pad BGA

3.2.2 — The Plastic Ball Grid Array, PBGA

Increased IC I/O count is the result of increased device functionality, which in turn means more complex packages with higher wiring density within the package. This leads to a significant increase in cost of manufacture. particularly ceramic PGA and BGA packages. As a result, in the late '80s/early '90s, BGA packages began

appearing manufactured using organic laminate PWB technology. Intel's microprocessor packaging is an example of the move to the laminate package. The earliest microprocessor was in a ceramic DIP, a later processor in a ceramic PGA, and finally the Pentium 4 in a plastic BGA (Figure 3-11). The PBGA configurations are similar to the CBGA (Figure 3-12).

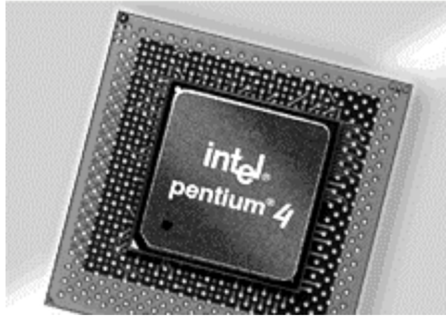


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Figure 3-11. Intel's Pentium 4 in Plastic BGA

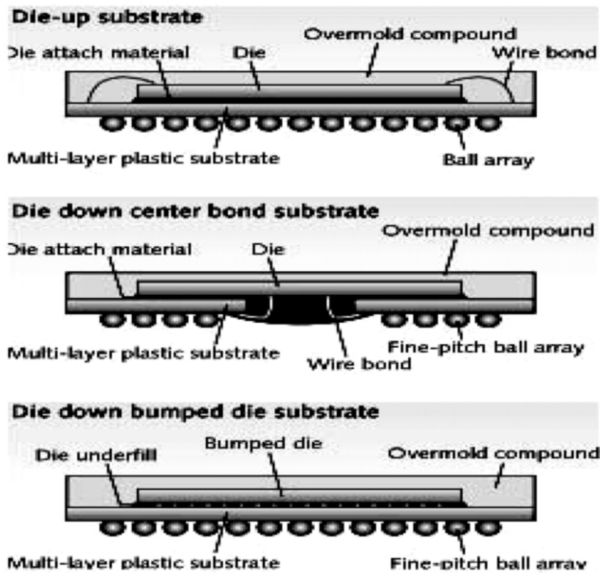
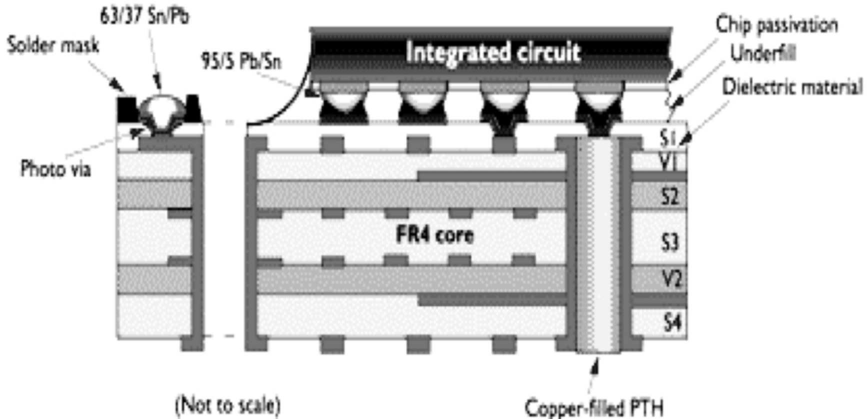


Figure 3-12. PBGA Configurations with Rigid Laminate

Bump sizes and pitch for the PBGA are the same as CBGA. Pitch and number of bumps are critical in determining the PWBs design needs. This is particularly true for flip chip in package, FCIP, and some CSP applications. The smaller the pitch, (for FC 0.125 mm), the more complex is the design, and more importantly, limited

availability of board manufacturers with the required manufacturing capabilities. These require high density interconnect with lines and spaces on the order of 0.025–0.050 mm (1–2 mils) and vias similar in size and pitch, manufactured using what is called Build Up Technology or BUT. BUT combines both laminate and thin film processing to produce a board shown schematically in Figure 3-13. Laminate and BUT technologies are discussed in detail in Chapter 15.



(Courtesy IBM Corp.)

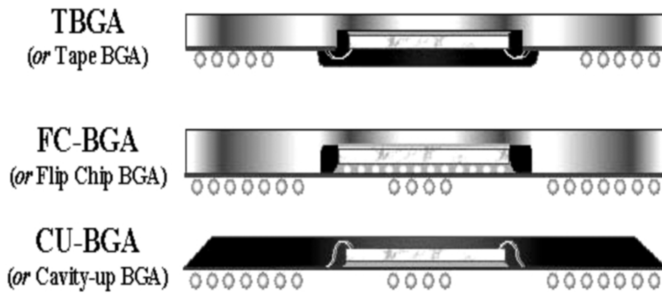
Figure 3-13. Schematic Flip Chip in Package (FCIP) PBGA

3.2.3 — Tape Ball Grid Array, TBGA

An increasing number of BGAs are being manufactured using a flex circuit or "tape" as the substrate. The flex circuit can be a single or double-sided patterned conductor interconnect. Referred to also as a "transposer". it replaces the ceramic or rigid organic substrate providing transition from the die to the package output pads or bumps. Use of the tape results in a reduced package thickness. The combination of a proper die attach adhesive and the tape, typically polyimide film 0.025 mm (1 mil) thick, acts as compliant media that can offset mismatch in Coefficient of Thermal Expansion (CTE) between the die and the package, enhancing life cycle performance when subjected to thermo-mechanical stresses.

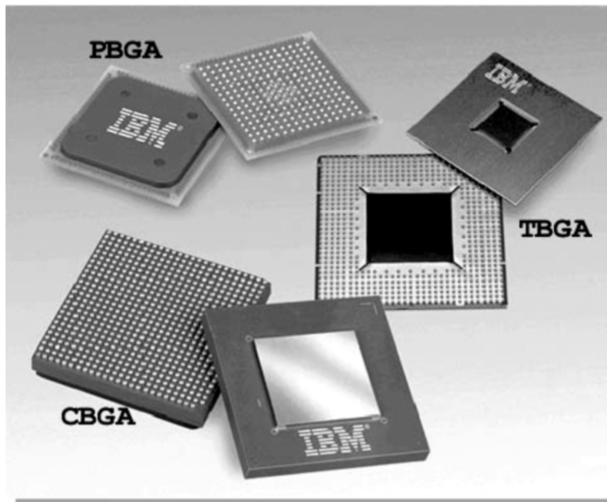
3.2.4 — TBGA Structures

A metal stiffener is usually used in Tape BGA structures to provide rigidity and robustness. It also acts as a heat sink in the cavity up wire bonded version, as seen in (Figure 3-14). The die can be wire bonded or flip chip attached directly to the tape and overmolded. The overmolding, in turn, provides mechanical support much like the "stiffener". Note that like CBGA and PBGA the I/O pads are usually not full array and are located outboard of the die which decreases the packaging efficiency. Figure 3-15 shows examples of CBGA, PBGA, and TBGA.



(Courtesy 3M Corp.)

Figure 3-14. Tape BGA Configurations



(Courtesy IBM)

Figure 3-15. CBGA, PBGA, TBGA

3.3 — BGA Surface Mount Assembly [8,9]

All BGAs are surface mounted using a solder reflow process. The solder reflow process features a unique characteristic referred to as "self-alignment". Self-alignment can be described as the *repositioning* of a misaligned package or die by surface tension while the solder is in the liquidus state. It effectively corrects the misalignment of the package at the time of placement. It results in complete wetting of the substrate pads by the solder and the package ending up "perfectly" aligned.

The attachment process itself is dependent upon the solder bump material and the substrate. For the CBGA the bumps are usually high lead e.g., 5Sn95PB (reflow

temperature 350°C). For PBGAs the bumps are eutectic 63Sn37Pb (reflow temperature 200–220°C) or can be one of the no lead solders such as 96.5Sn3Ag0.5Cu (with a melting point from 217º–220ºC and a reflow temperature approximately 260°C). However, because of the higher reflow temperatures associated with the no lead solders, the availability of organic boards with the higher glass transition temperature (Tg) needed and the associated increased cost, are valid concerns.

CBGAs, PBGAs and TBGAs can be directly soldered to a ceramic substrate. However, the CBGA's high lead bumps prohibits direct attachment to the PWB because of the high melting point of the solder. However, CBGAs with high lead bumps can be attached to a PWB by first stencil printing eutectic solder paste on the board's pads. After package placement the paste is reflowed. The high lead bumps do not melt however, the eutectic solder when liquidus dissolves a small portion of the bump and on solidification creates a solder bond. The bumps in effect retain their original size and effectively act as "standoffs". The gap between the bottom of the package and the surface of the board is thus the same as the bump height on the die, typically 0.075–0.10 mm (3–4 mils). The larger gap enhances the application of underfill, which if needed, enhances reliability and robustness. The underfill also acts like a moisture barrier providing protection for the device and any conductor traces that may run under the package.

PBGAs with eutectic bumps can be solder reflow attached directly to the PWB with or without the use of stencil printed solder paste on the pads. The advantage to use of solder paste is that it provides an added volume of solder that results in increased bump size following reflow and, like the high lead bumps, a larger chip to package gap.

3.4 — BGA Attributes

Area Array Packages, in particular the BGAs, have very quickly become a staple in electronic manufacturing. Area array has many attributes compared to other packages, e.g., QFPs. These include:

- Accommodating high I/O count ICs more effectively and efficiently.
- Self-Aligns, therefore placement accuracy is less critical.
- Requires smaller footprint at board level.
- Better thermal management.
- A robust finished assembly.

3.5 — BGA Concerns

The BGA has emerged as the ideal package for the high performance ICs and ASICs, and for I/O counts starting around 300. Because all connections are made under the package it is impossible to visually inspect all solder connections after assembly as is the case with peripheral leaded packages. To realize high assembly yields therefore, it is necessary to put in place more in process controls both pre- and post-assembly.

Pre-assembly controls include:

- Visual inspection of bumped die to identify missing bumps, defective bumps, or irregular size bumps.
- X-ray inspection to identify excessive internal voids in bumps.
- PWB inspection for footprint defects, excessive board warpage and cleanliness.

Post-assembly controls include:

- Inspection of package attachment using techniques such as X-rays and Ultrasonics.
- Electrical testing prior to any underfilling or conformal coating.

3.6 — The Future

Area array packaging has proven to be both a short and long term solution to increasing I/O count of the IC and the demands of end product. Variations in area array packaging, in particular, rapidly emerging Chip Scale Packaging (CSP) and Wafer Level Packaging (WLP) (Chapter 3) now offer a smaller version of the BGA, with packaging efficiencies (PE) of 80% and higher. Ideally a PE of 100% is most desirable as is the case with flip chip (Chapter 9). Flip chip and WLP are essentially "packageless packages", with a packaging efficiency of 100% since the area of the die and the area required for attachment to the next level are the same. Wafer level packaging is generically similar to flip chip since the "packaging" process is accomplished while the IC is still in wafer format with processes comparable to flip chip. It differs structurally however, with features that effectively minimize the problems with handling, testing, and assembly associated with flip chip.

CSP, WL-CSP and Flip Chip fully complement each other and can be expected to become the dominant packaging technologies of the future.

Packaging efficiencies >100% is of course the panacea of the packaging engineer. Emerging 3-D packaging technologies such as die stacking in a CSP do in fact provide a PE that readily exceeds 100%. 3-D packaging is discussed in Chapter 5.

3.7 — Lead-Free Manufacturing [10–15]

Removal of Hazardous Substances (RoHS) is a directive currently in place in the United Kingdom, Europe and the Pacific Rim that calls for the removal of all hazardous substances from electronic products. There is also legislation currently banning hazardous materials in all electronic products sold in Japan. Compliance is mandated by 2006. Failure to comply negates sale of products within the European Union and Japan.

RoHS impacts packaging and assembly of the IC at Levels 1.0 and Level 2.0. Banned substances include, lead (Pb), mercury (Hg), cadmium (Cd) hexavalent chromium (Cr^{+6}), poly brominated bephenyls (PBB) and poly brominated diphenyl ethers (PBDE). Clearly, the most dominant of these is lead and is widely used at both

Level 1.0 and Level 2.0 packaging. At level 1.0 lead is used for some die attach and is prevalent for applications involving flip chip. In addition, package leads and most BGAs contain lead bearing solders. At Level 2.0 the most common solder for component attachment is eutectic SnPb 63/37.

The challenge has been to find a lead-free replacement solder. The effort has been global since the 1990's. Within the U.S., various groups made up of industry-wide companies that make up the electronic manufacturing infrastructure, have formed consortia to jointly address the effective implementation of lead-free manufacturing of all electronic products. Companies involved include semiconductor and component manufacturers, electronic manufacturing services, and material and equipment manufacturers.

Two such groups are the National Electronic Manufacturing Initiative, NEMI, (now called *i*NEMI) and the Massachusetts Lead-Free Solder Consortium.

3.7.1 — Lead-Free Processing and Concerns

Two lead-free replacement solders have emerged, SnAgCu and SnAg. Both contain roughly 4% Ag with the Cu around 0.5%. The SnAgCu has been shown to provide reliable results for SMT solder processes, where most of the development efforts have been concentrated, and for BGA solder bumps. SnAg on the other hand, is recommended for wave soldering. The liquidus temperature for SnAgCu is 217ºC and the reflow peak temperature of 240ºC to 260ºC. This compares to eutectic SnPb with a liquidus of 183ºC and a reflow of 205ºC to 230ºC. The difference in liquidus is 34ºC and dictates significantly higher reflow temperature for the lead-free solders. Processing at the higher temperatures is a major concern affecting many facets of lead-free electronic manufacturing. The reflow process has been and continues to be investigated directed towards arriving at the lowest acceptable temperature while optimizing the reflow profile to insure minimal temperature variation (ΔT) across the board.

Many components including actives and passives are not capable of surviving the higher process temperatures particularly with the multiple exposures that are encountered when there is doubled-sided assembly required. Further high temperature may also be experienced when rework is necessary. Component manufacturers are working towards providing devices with increased high temperature survivability.

The PWB can also be damaged because of the higher temperatures with delamination and warpage being major concerns. Both occurrences can be catastrophic at this particular stage of the process especially at a time when components are becoming smaller and the component density at the board level is expected to increase. Another aspect of lead-free solder is that the surface energy is usually lower than that of eutectic solder which means that the self-alignment of packages (BGAS and CSPs) as well as WL-CSPs and flip chip is less effective. This in turn can affect the pick and place equipment that may be in place and necessitate acquiring additional placement equipment.

While the concerns associated with implementing lead-free manufacturing are many, the mandate is clear, and the requirement for environmentally friendly end product will not go away.

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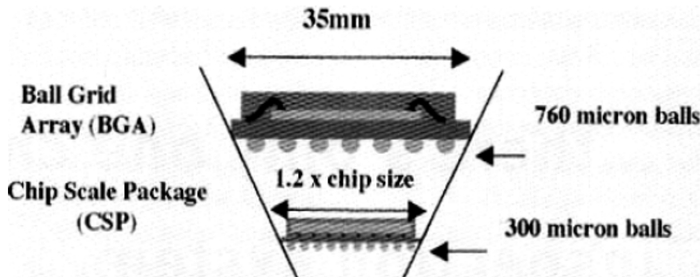
4 The Chip Scale Package

4 — THE CHIP SCALE PACKAGE, CSP

The Chip Scale Package introduced in the early '90s is essentially a smaller version of the BGA and represents the continuing trend in package miniaturization.

Industry arbitrarily defines a CSP as *any package that is no larger than 1.2 times the area of the die.* However, in many instances a package is classified as a CSP if it is simply "near-die size". CSPs share many of the same attributes as the flip chip including areas of application.

When first introduced, the CSP was presented as a viable alternative to the flip chip, particularly in size, but offering all the advantages of a packaged device including pre-assembly testing and easier handling. An important feature of the CSP that differentiates it from the flip chip is that both the bumps and bump pitch are larger (>0.2 mm, 8 mils) than those of the flip chip (typically 4–5 mils). Figure 4-1 illustrates how the BGA and the CSP compare relative to package size and bump diameters.



(Courtesy National Semiconductor)

Figure 4-1. BGA vs. CSP

This is a significant attribute since it can enhance reliability and requires a less sophisticated and more readily available PWB. While the flip chip is applicable to the full spectrum of I/O count the CSP is more appropriate to the lower end.

The number of package pads that can be accommodated will typically depend upon the bump size and pitch, and overall die size.

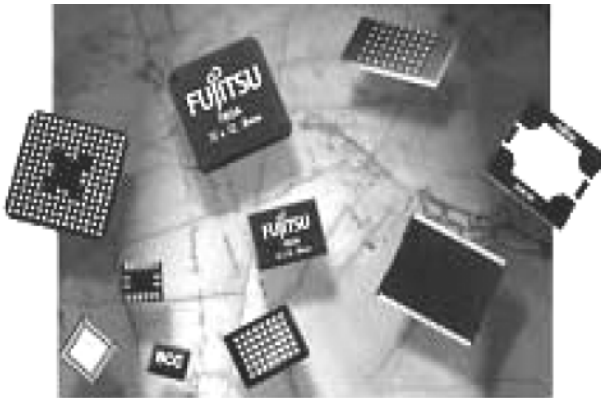
The larger the bump and the bump pitch the less I/Os that can be accommodated for a given die size. However, it is an advantage to always have the bumps and the bump pitch be as large as possible mindful of the effect of each on the PWB. As will

be seen with flip chip (Chapter 10) on organic substrates, the reliability, or life cycle performance under thermo-mechanical stress, is influenced by both the bump size and pitch. Underfill an organic material (primarily an epoxy) is used to fill the gap between the die or CSP and the PWB. It is intended to extend life cycle perfomance. Larger bumps provide for a bigger gap, while increased pitch allows for enhanced flow of the underfill material. Figure 4-2 shows examples of CSPs from Fujitsu in various I/O configurations.

Memory product, that is, Flash, SRAM, DRAM, etc. are the targeted market for the CSP, particularly for applications in telecommunications, wireless, computer, and consumer areas where portability is a major consideration.

4.1 — Chip Scale Package Manufacturing Technologies

The manufacturing technologies available for CSPs interestingly cover both singulated die as well as die still in wafer format. In the latter case all "packaging" is performed on the wafer and is referred to as Wafer Level Packaging, WLP, or WL-CSP. For both the singulated die and the WLP there are many variations, some of which are discussed in the following sections.

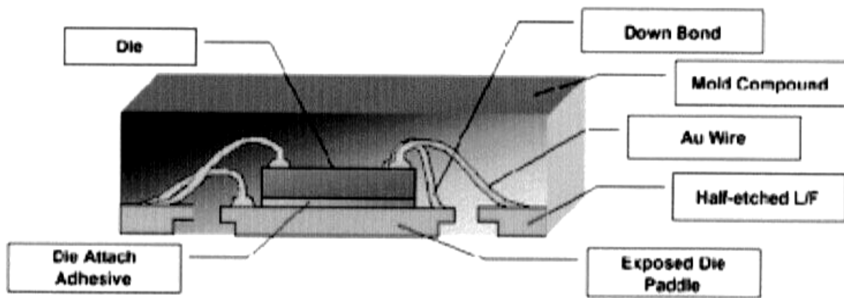


(Courtesy Fujitsu Microelectronics America)

Figure 4-2. CSP Packages

4.1.1 — The Singulated Die CSP

For singulated die there is a "substrate interconnect" that is manufactured separately. The substrate contains a conductor network that redistributes and integrates the bond pads from the die to the package I/O pads in an area array layout. The particular "substrate" used is the differentiator identifying the type of CSP. For example, it can be a leadframe (Figure 4-3(a)), a rigid laminate board (Figure 4-3(b)), or a tape/flex circuit (Figure 4-3(c)). The leadframe CSP, unlike most CSPs has the I/O pads located on the bottom of the package but along the perimeter of the package. The die are wire bonded. For the laminate or tape, there are two options for die attach: chip & wire or flip chip.



(Courtesy Amkor Technology, Inc.)

Figure 4-3(a). Lead Frame Based CSP (Small Outline No-Leads, SON)

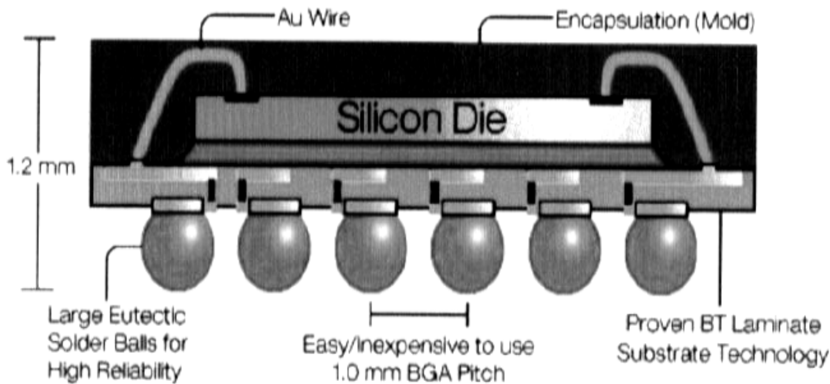


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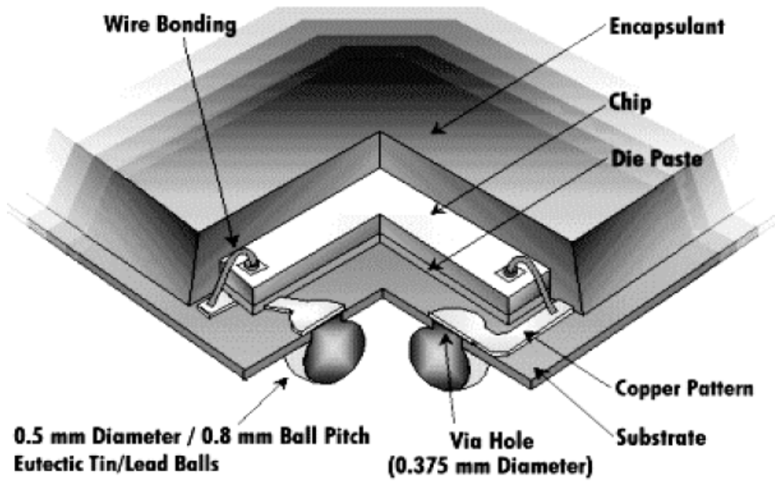
Figure 4-3(b). Laminate-Based CSP

4.1.2 — CSP and Wire Bonding

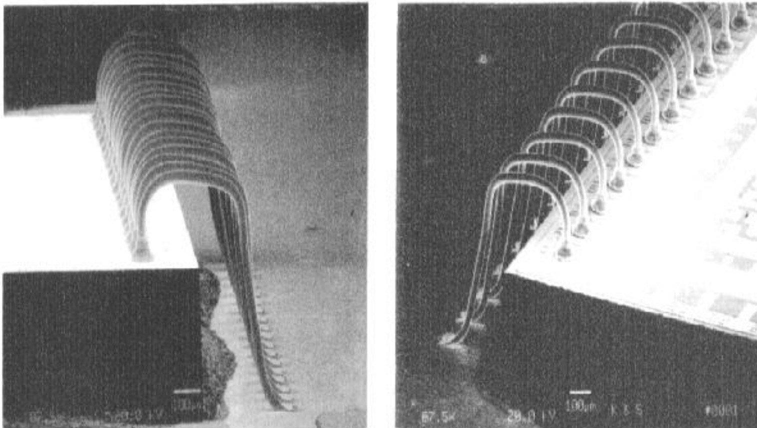
With face up CSPs, the wire bonding must often be modified in order to minimize the package footprint and still conform to the 1.2 times the die size requirement.

Figure 4-4 is a scanning electron micrograph (SEM) of what has become known as the "CSP Loop" wire profile. Note that the wire has a low short loop with the second bond to the package less than roughly 12 mils from the edge of the die. It was developed specifically to reduce the area required to fully interconnect a device to a package or substrate. It also allows devices to be placed much closer to each other in MCP applications. Note also, that in order to achieve this, it is necessary that the pads on the package be roughly the same pitch as the die. This latter requirement can impact the availability by limiting the number and availability of suppliers with the needed fine line capability.



(Courtesy Texas Instruments)

Figure 4-3(c). Tape Based CSP

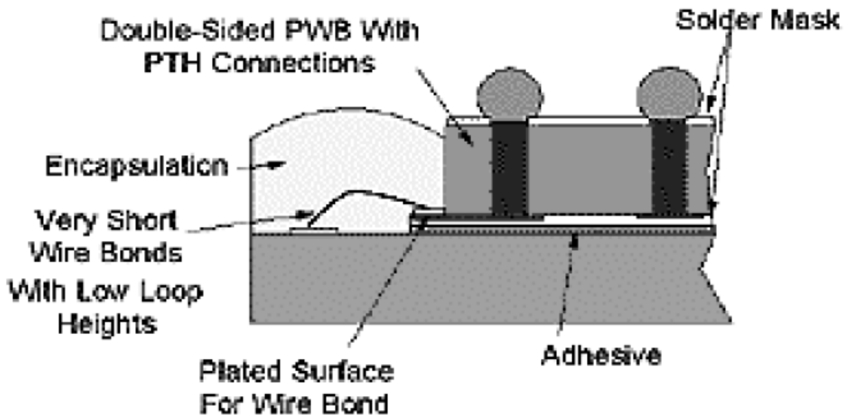


(Courtesy Gaiser Tool)

Figure 4-4. The CSP Loop

4.1.3 — Varying Structures

Figure 4-5 is a graphical representation of a CSP from OKI Semiconductor. The CSP is very similar to the μBGA but uses a laminate substrate as the interconnect medium. However, since the substrate is smaller than the die the package is actually the same size as the die.



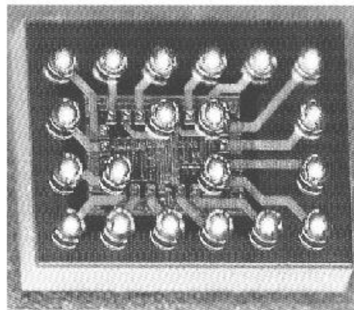
(Courtesy OKI Semiconductor)

Figure 4-5. Schematic of CSP on Rigid Organic Substrate

4.1.4 — The Embedded Chip CSP [3]

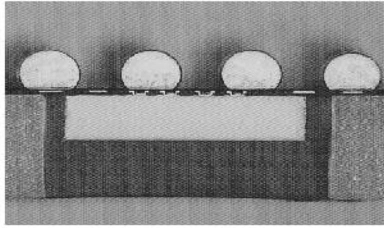
Figure 4-6(a) is a photomicrograph of an “embedded” chip CSP from Fraunhofer IZM. A cross-section of the device is shown in Figure 4-6(b).

The CSP is fabricated using a process based upon a “Chips First” MCM technology (discussed in detail in Chapter 12) that basically makes contact to the die bond pads (there is no wire bonding) as part of the overall interconnect process. The entire interconnect is on the surface of the die terminating in an area array format package. The process is similar to an RDL.



(Courtesy Fraunhofer IZM)

Figure 4-6(a). Embedded CSP

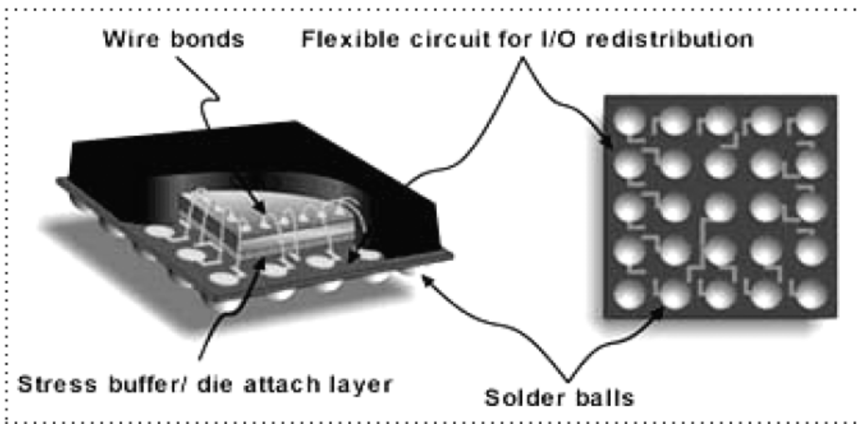


(Courtesy Fraunhofer IZM)

Figure 4-6(b). Metallurgical Cross-Section Embedded CSP

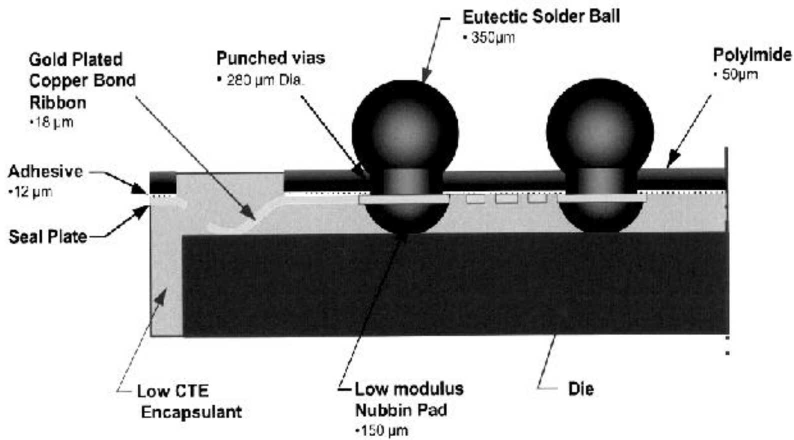
4.2 — The μBGA™ [4]

μBGA™ is the registered trademark for a CSP developed by Tessera Inc. Fully patented, it identifies a somewhat unique interconnect, die assembly, and final encapsulation processes. The interconnect is basically a metallized and patterned flex circuit. Assembly can be either chip & wire (Figure 4-7(a)) or the die can be attached to the flex through cantilevered Ni-Au plated Cu leads bonded to the Al bond pads on the die similar to Tape Automated Bonding (TAB) a level 1.0 interconnect technology (discussed in Chapter 9). The latter approach is shown schematically in Figure 4-7(b).



(Courtesy Tessera Technologies)

Figure 4-7(a). Chip & Wire Bonded μBGA™ (Face-Up)

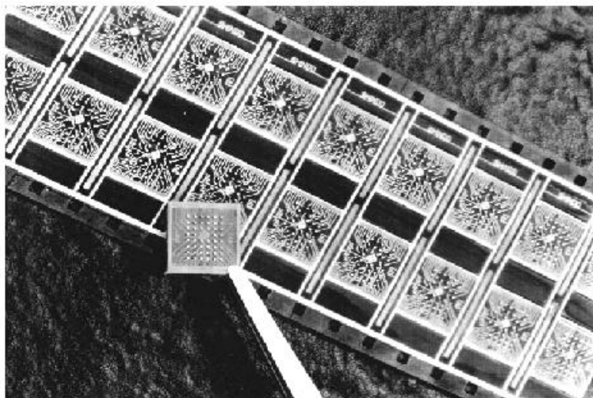


(Courtesy Tessera Technologies)

Figure 4-7(b). The μBGA™ Tape Lead Bonded Face-Down

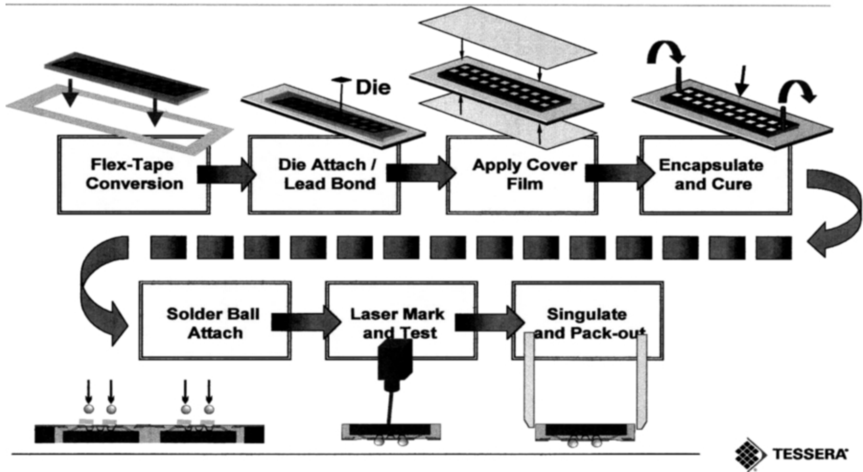
The flex circuit interconnect or "interposer", is a polyimide tape or film that supports a patterned single or double-sided copper circuitry. The manufacture of the tape is basically the same as used for TAB tape. The tape is manufactured in a "strip" format, as shown in Figure 4-8. Once assembled the die remain in the tape through all remaining processing. As with all the configurations, assembly of the singulated die is followed by epoxy molding and package singulation. The assembly process for the μBGA™ is shown in Figure 4-9.

A single frame from the tape is shown in Figure 4-10 and highlights the attachment of the cantilevered leads.



(Courtesy Tessera Technologies)

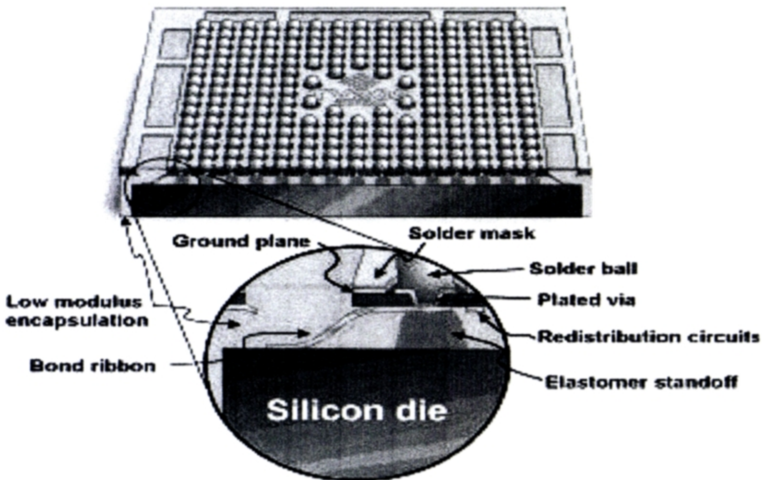
Figure 4-8. μBGA™ "Interposer" Tape Format and a Singulated CSP



(Courtesy Tessera Technologies)

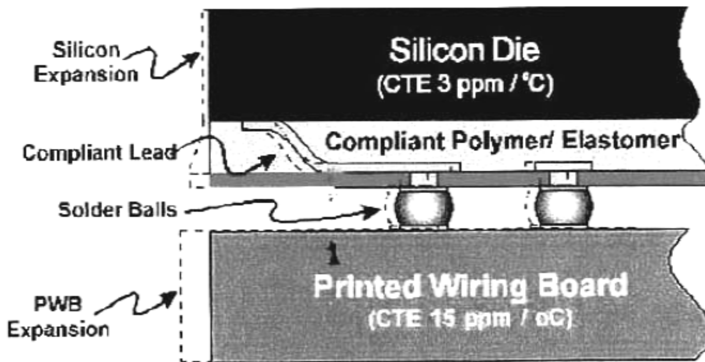
Figure 4-9. µBGA™ Lead Bonding Assembly Process

The uBGA™ uses a low modulus die attach adhesive and encapsulant. Under thermomechanical stress these materials provide compliancy that absorbs the expansions and contractions occurring as a result of the differences in coefficient of thermal expansion of the silicon die, the polyimide tape, the solder bumps and the PWB. Figure 4-11 illustrates the structured compliancy of the µBGA™.



(Courtesy Tessera Technologies)

Figure 4-10. µBGA™ Lead Bonding Die Attach



(Courtesy Tessera Technologies)

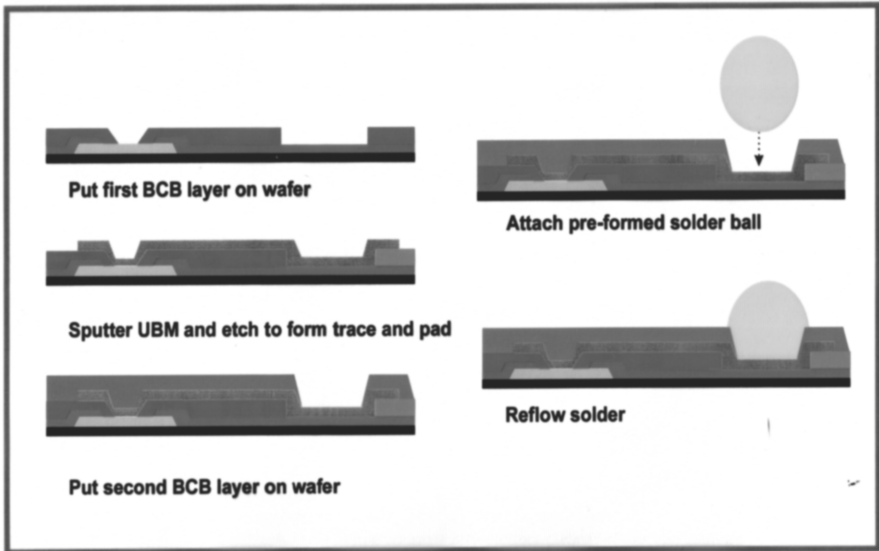
Figure 4-11. µBGA™ Structured Compliancy

4.3 — Wafer Level Packaging—The WLP [5–10]

Wafer Level Packaging effectively eliminates the need for a separate die assembly. It incorporates manufacture of all the interconnects to the die and from die to package I/Os while still in wafer form. WLP is an extremely cost-effective process. *It is essentially a thin film-based process in which final device packaging is completed at the wafer level prior to singulation of the ICs.* The process almost *always* includes a redistribution of the peripheral I/O pads on the die to an area array contained totally within the body of the chip. All wafer level packages are exact die size. A WL-CSP and a flip chip therefore, are the same size differing only in the bump size and pitch.

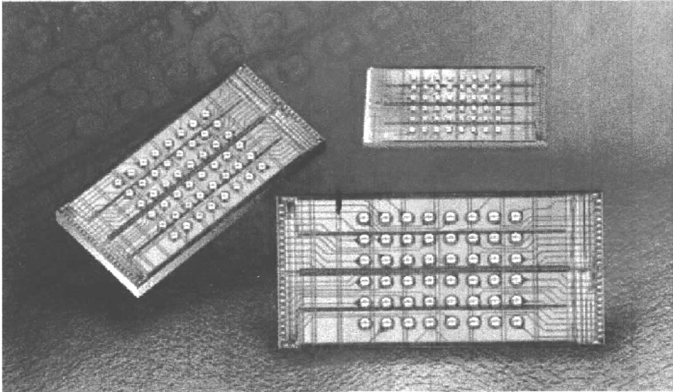
4.3.1 — WLP Processes

While there are several different WLP processes they are all very similar and closely follow the thin film process described in Chapter 2. Figure 4-12 shows a process used in manufacturing Flip Chip International's *Ultra* CSP®. The redistribution layer, or RDL, from die pads to I/O pads uses a deposited and patterned conductor and dielectric. The RDL metallization, in this case, is a tri-metal stack of Al, NiV, and Cu. Unlike flip chip the solder balls, or bumps, are not evaporated or plated (both limited to bumps less than 200 µm) but rather mechanically placed using specially designed ball placement equipment in a separate off-line operation. Examples of WL-CSP memory devices are shown in Figure 4-13.



(Courtesy Flip Chip International LLC)

Figure 4-12. The UltraCSP® Process

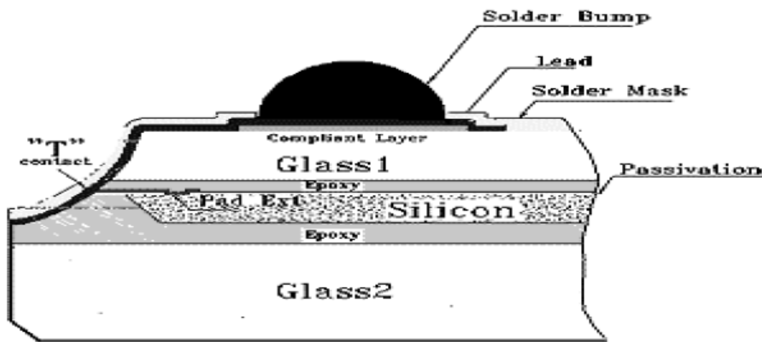


(Courtesy Flip Chip International LLC)

Figure 4-13. WL-CSP

Several companies offer WL-CSPs manufactured using different processes, metallization and dielectric materials. The variations are in some instances unique.

Figure 4-14 is a schematic cross-section of a CSP from Shellcase that uses non-conventional materials and processes.



(Courtesy Shellcase)

Figure 4-14. The ShellCase CSP

The process includes the following:

- A silicon wafer is fully encapsulated in epoxy and embedded between two glass substrates,
- Deposition and patterning of the conductor metallization extending the die I/O pads into the "streets" that separate the die on the wafer,
- Mechanically thinning the wafer,
- Mounting the thinned wafer onto a glass substrate,
- Backside etching to remove silicon from the "streets" to expose the extended IC I/O bond pads,
- A proprietary metallization process that includes the deposition and patterning, and relocates and terminates the IC pads on the top surface of the glass substrate for placement of the solder balls.

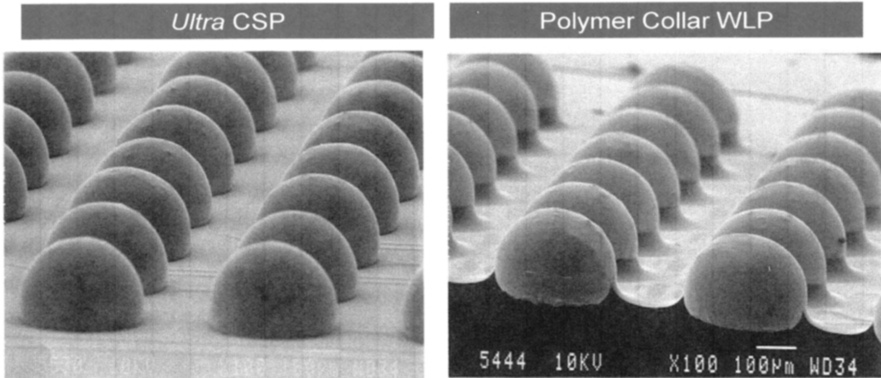
Mounting the wafer to a second glass plate completes the process. This is followed by sawing to separate the individual CSPs.

4.4 —Reliability Concerns [11–13]

When a WL-CSP is solder attached to a PWB and the assembly is subjected to thermo-mechanical stresses such as extreme temperature excursions or power cycling, cracks may appear in the solder joints. Referred to as solder fatigue the cracking is the result of the difference in Coefficient of Thermal Expansion (CTE) between the silicon, at 3 parts per million (ppm) and the PWB, typically 17 ppm. The cracks originate at the corner joints farthest from the center of the package and propagate with continuing stress. Eventually there is complete separation and the device experiences an electrical "open".

To address this problem, a modification to the process shown in Figure 4-12 evolved that, based on reliability test results, has demonstrated an increased life cycle performance by as much as 50%. Called Polymer Collar, the difference in appearance of the solder balls between the *Ultra* CSP® and the modified process is shown in Figure 4-15.

Use of an epoxy underfill (discussed in Chapter 11) is also used in many cases to further enhance reliability of the attachment. The underfill compensates for the mismatch in CTE and for mechanical stress that can be experienced during qualification testing, e.g., drop tests, and from warpage of the printed circuit board.



(Courtesy Flip Chip International LLC)

Figure 4-15. Flip Chip International's *Ultra*CSP® with Polymer Collar

With the many different CSP structures there is obviously a need to look carefully at each manufacturer's reliability data and assess its applicability to end product needs and operating environment.

4.5 — Summary

In summary the CSP is a smaller version of the BGA and follows the trend towards package miniaturization. CSPs can be manufactured using singulated die or in wafer format. A CSP can accommodate multichip as well as single chip packaging.

The CSP can be characterized as follows:

- Near-die size or die size depending primarily on whether the devices start as singulated die or are in wafer format.
- The package I/O pads are located on the bottom surface and are contained within the body of the package for surface mount attachment to the PWB.
- Bump diameter and bump pitch are smaller than a BGA but larger than a flip chip.
- The CSP has a Packaging Efficiency, (PE) no less than 80%. Can be 100% if processed in wafer format, or >100% if stacked die are involved.
- And finally because the CSP is close to or the same as the die size, it has direct applicability to COB and MCP. It basically offsets lack of KGD and therefore offers higher module yields. Reliability performance of the package however must be taken into consideration.
- WL-CSP and flip chip are both true die size.

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5 Multichip Packaging

5 — MULTICHIP PACKAGING (MCP) [1,2]

Multichip Packaging (MCP) defines a packaging option in which multiple die and/or packaged devices (SOICs, CSPs) are incorporated into a single package. The MCP may be considered as an alternative to an Application Specific Integrated Circuit (ASIC). Compared to the ASIC it is a viable option offering lower cost and faster time to market. It presents many advantages providing for a significant increase in packaging efficiency by replacing multiple packages with a single package (Figure 5-1). There is also a major reduction in overall size and weight.

MCP by definition includes the following types of packaging technologies:

- The Hybrid Circuit (HC) or Hybrid Integrated Circuit (HIC)
- The Multichip Module (MCMs)
- 3-D Packaging, and
- System in Package (SiP) or System on Package (SoP).

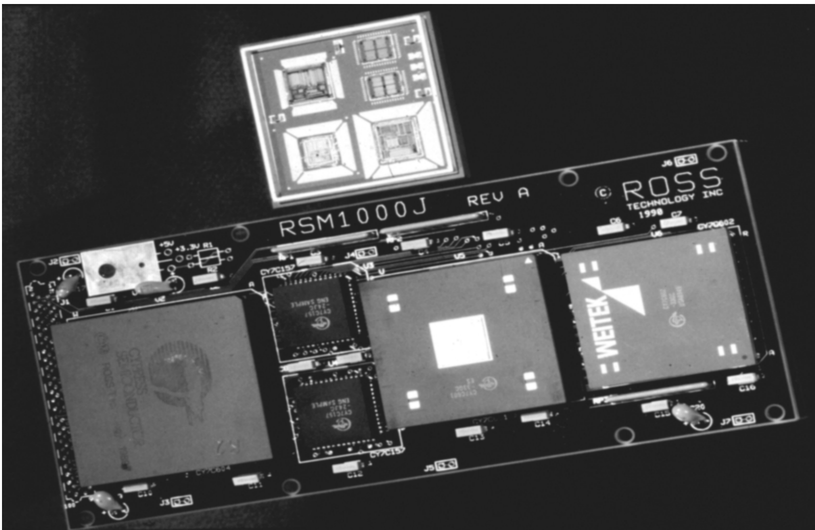


Figure 5-1. Multichip vs. Single Chip Packaging

Common to each is an interconnect substrate that together with chip & wire, TAB, and flip chip interconnects combine to complete the attachment and interconnection of multiple components, both actives and passives. The substrate, which serves as a physical support structure, provides the electrical interconnections between the various components and therefore must be fully supportive of the IC and the overall mechanical, thermal, and electrical requirements. Table 5-1 demonstrates one of the many benefits to be realized with MCP, not necessarily at the component level, but rather at the system level. As indicated, using DIPs, 28 PWBs, 5"x5" are required at the systems level. Using SMT reduces the number of PWBs, 6"x9", while implementing MCP results in a system comprised of 5 PWBs, 5"x5" in size. The area is less than 1/3rd that with SMT and almost 1/10th with DIPs. In addition, the system's power is decreased almost 50%.

Table 5-1. Comparing DIP, SMT, MCP at System Level *(Courtesy Hughes Aircraft)*

Interconnect Technology	Quantity PWBs	Size	Area	Power (watts)
DIP	28	5" x 5"	700 sq. in.	258
SMT	5	6" x 9"	270 sq. in.	158
MCP	5	4" x 4"	80 sq. in.	158

5.1 — MCP Substrate/Package Technologies [3,4]

MCP substrate interconnects are manufactured using thick film, cofired ceramic, thin film or organic laminate technology. The thick film and cofired ceramic technologies share a common patterning process, namely screen printing. Thick film has been a dominant manufacturing technology since the 1960s used in the manufacture of early single chip ceramic packages and hybrid circuits.

The cofired ceramic tape process appeared in the early 1970s providing a multilayer conductor interconnect accommodating more advanced ICs and at the same time fully completed packages, with lead or pins and seal rings for hermetic enclosures inplace. Component assembly was all that was required. Complete packages can be manufactured in the various formats, i.e., quad flat pack (CQFP) or an area array, PGA or BGA, supporting SCP or MCP applications. Today both thick film and cofired ceramic tape are mature manufacturing technologies with well established reliability databases.

All of the substrate manufacturing technologies are covered in detail in chapters 12 through 15.

5.2 — The Hybrid Circuit

A hybrid circuit is defined as an assembly containing both active semiconductor devices (packaged and unpackaged) and passive components (deposited and discrete) interconnected on a common substrate offering a specific circuit function. The active devices, include diodes, transistors, or integrated circuits, while passive devices are resistors, capacitors, and inductors. The substrate is ceramic, aluminum oxide, Al_2O_3,

with patterned thick film conductors, resistors and dielectrics. Figure 5-2 shows an early hybrid circuit (circa'60s) with diodes, transistors and deposited resistors and discrete capacitors. The active devices are chip and wire assembled to a single level gold conductor deposited on the ceramic substrate and patterned using thick film screen printing. The substrate is shown mounted into a metal package with wires bonded from the substrate I/O pads to the package leads. A metal lid can then be welded in place to provide a hermetic enclosure that allows the assembly to be electrically tested and function in a benign or controlled environment.

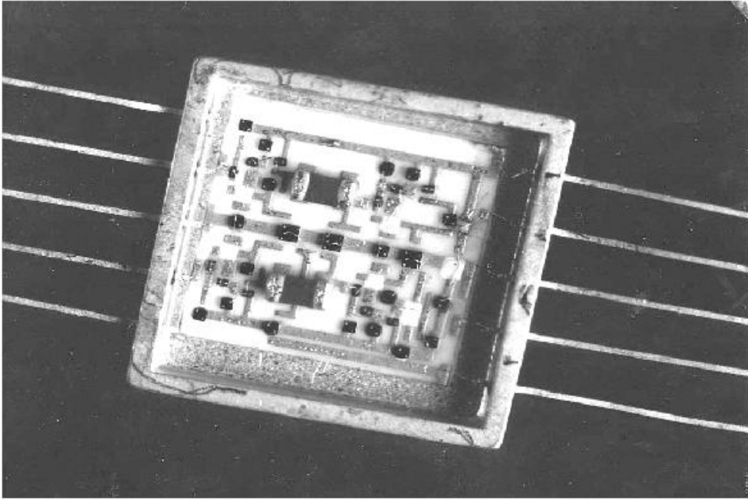


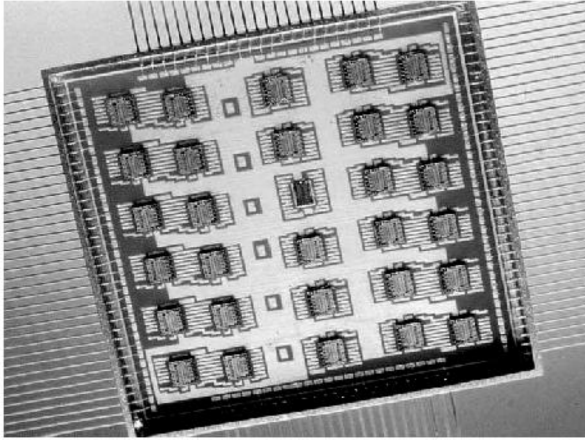
Figure 5-2. Hybrid Circuit with Transistors and Diodes (Circa 1960s)

5.2.1 — The IC and the Hybrid Circuit

With the emergence of the IC in the late '60s, it was widely believed that the hybrid circuit would quickly lose significance as a packaging technology. However, when the IC became readily available it was quickly incorporated into the hybrid (Figure 5-3) as the active device replacing the earlier diodes and transistors. Hybrids, almost exclusively ceramic based, come in many configurations depending primarily on the end application. Figure 5-4 shows, for example, an RF/Microwave hybrid. It includes active devices—diodes, transistors and integrated circuits, and passive components—resistors and capacitors. For the RF/microwave unit, the devices are eutectic and epoxy attached and Au wire bonded. The base substrate is aluminum oxide (Al_2O_3), the interconnect is thick film Au to which is added a thin film Au metallized microstrip sub-assemblies. Deposited thick film passives, mostly resistors, are part of the interconnect. In addition, there are discrete chip resistors and capacitors mounted to the conductor interconnect using epoxy or solder. Again the assembly is mounted into a metal package.

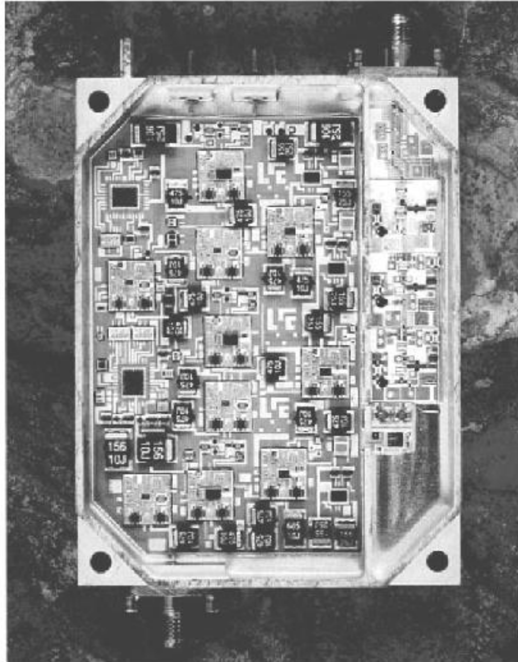
The hybrid circuit was the predecessor of the multichip module and ideal for many custom applications not available at the time as a monolithic IC. The hybrid circuit, with addition of the integrated circuit, achieved an immediate increase in

both functional density and packaging efficiency. With the elimination of multiple packages the potential for improved reliability was an added value.



(Courtesy Lockheed Martin)

Figure 5-3. Multiple ICs on Multilevel Thick Film Conductor Pattern (Circa early 1980s)



(Courtesy Teledyne Microelectronics)

Figure 5-4. RF/Microwave Hybrid Circuit

5.3 — The Multichip Module (MCM)

With each new generation of IC the hybrid circuit became increasingly more functionally dense and the multichip hybrid circuit became a Multichip Module (MCM).

The MCM can perhaps best be described as an advanced hybrid circuit. For many applications such as digital, it is basically a multichip hybrid assembly but of significantly higher level of complexity and overall functionality. It is typically characterized by the ICs that are at least Very Large Scale Integration (VLSI), i.e., >100,000 transistors per IC and higher. Also the substrate interconnect, referred to as a high density interconnect (HDI), is specifically designed and manufactured with high conductivity conductors and dielectric layers having low dielectric constant, to enhance the electrical, mechanical and thermal requirements needs of the IC.

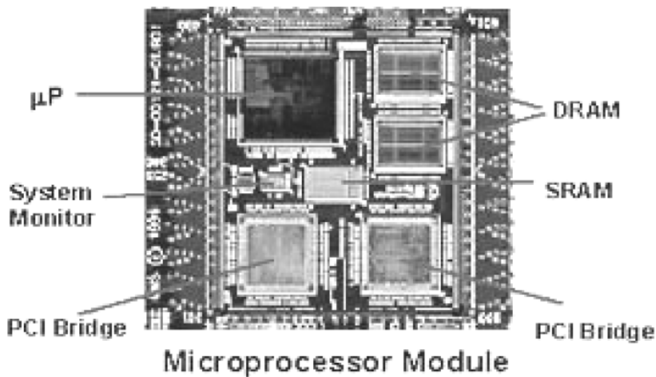
5.3.1 — Types of MCMs

MCMs are identified by the manufacturing process used to produce the interconnect substrate.

Thus,

- An **MCM-D** has an interconnect substrate fabricated employing thin film technology with deposited conductors and dielectrics patterned using a photolithographic process. Figure 5-5(a) shows a populated MCM-D. Note that like the hybrid, it is mounted in a package.

  The thin film manufacturing technology is covered in Chapter 12.



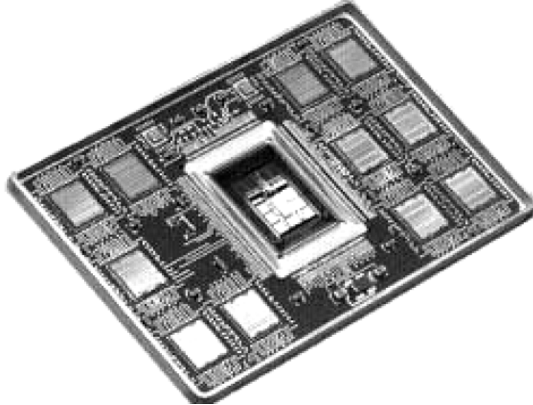
(Courtesy National Semiconductor)

Figure 5-5(a). MCM-D (mounted on PWB)

- **MCM-C** implies an interconnect substrate, or package, manufactured using multilayer thick film or cofired ceramic tape processes. In either case, the conductors and dielectrics are deposited and patterned using screen printing. Figure 5-5(b) is a populated cofired MCM-C. The cofired ceramic technology provides for both an embedded conductor interconnect network and a

package combined in a single monolithic structure. A multilayer thick film interconnect, however, in most configurations may require mounting into a package that is usually metal.

The Thick Film and Cofired Ceramic Technologies are detailed in Chapters 13 and 14.



(Courtesy Aeroflex, Inc.)

Figure 5-5(b). MCM-C Cofired Ceramic Package

- **MCM-L** uses an interconnect substrate fabricated using organic laminate PWB processes. Figure 5-5(c) shows a populated and an over-molded MCM-L. The lamination process for both the MCM-L and the Level 2.0 PWB are discussed in Chapter 15.

(Courtesy Amkor Technology, Inc.)

Figure 5-5(c). Laminate MCM-L in Molded BGA Package. Top—Molded Package; Left—Wire Bonded ICs; Right—Bottom of Package

5.4 — 3-D Packaging [5]

It is quite apparent that the MCM achieves sizeable reduction in size, weight, and volume mainly through elimination of multiple packages that results in packaging efficiencies in some cases in excess of 90%. Clearly the packaging is two-dimensional (2-D), that is, space utilization is confined to a plane with x and y dimensions only. Maximum packaging efficiency with 2-D packaging is by definition 100%. The ongoing demands for increased functionality in an absolute minimum overall package volume has lead to the extension of MCM 2-D technology to a 3-D format. 3-D packaging, by definition, covers packaging in not only x and y but in the z or vertical direction as well. It immediately provides for a significant increase in achievable packaging efficiencies that are greatly in excess of 100%.

Today's 3-D packaging covers the stacking of both multiple packages and die, and combination of the two. Interestingly, 3-D packaging is not a new concept and actually preceded conventional 2-D. Figure 5-6 shows an example of a very early packaging approach developed at RCA in the late 1950s early 1960s under a government funded program called "Micromodules". Individual active devices, in this case transistors and diodes, and passives: resistors, capacitors, and inductors, were individually mounted on separate ceramic substrates. Interconnecting conductor traces were terminated at the edges of each substrate. The substrates were then stacked and vertical riser wires soldered to the edges of the substrates in the stack to electrically interconnect the various mounted components.

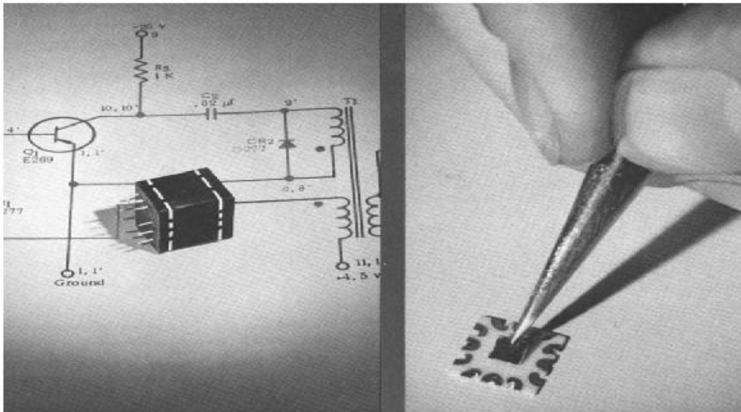


Figure 5-6. Earliest 3-D Packaging: The RCA Micromodule [5]

Ironically, the Micromodule was ahead of its time, and for many reasons, mostly cost. It gave way to the then emerging 2-D hybrid circuit. It was, however, the precursor of the cofired ceramic tape packaging technology (Chapter 14).

Today, 3-D packaging, in the form of stacked die and packages, (Figure 5-7), is rapidly moving into mainstream manufacturing. The prime market and a driving force is memory product. Stacked memory is particularly attractive for applications in the high volume cellular communications products area. The early stacked die packages contained a Flash Memory and a SDRAM in a CSP.

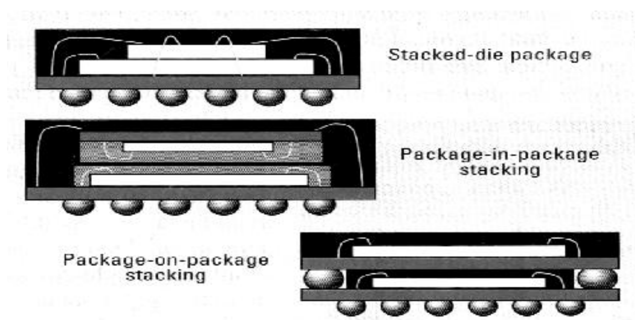


Figure 5-7. 3-D IC Stacking Options [7]

5.4.1 — Stacked Packages [6–8]

The stacking of packages took place in the mid 1980s as a response to the need for increased memory capability in select applications where available space was at a premium. Stacking was the enabler and was accomplished while maintaining the same single package "footprint" at the board level.

Stacked packages, also called "Package on Package" (PoP), are shown in Figure 5-8.

The stacking of packages includes MCPs as well.

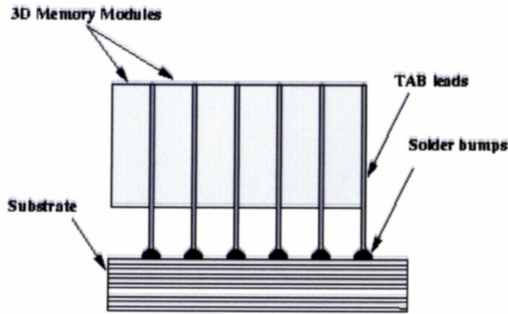
(Courtesy Irvine Sensor Cotp.)

Figure 5-8. Stacked TSOPs

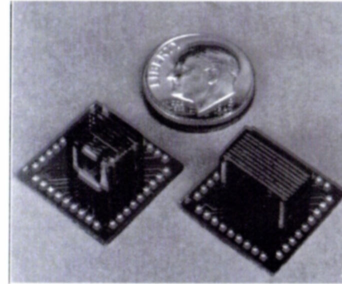
5.4.2 — Die Stacking [9]

In the late 1980s, the Defense Advanced Research Programs Agency funded several programs for the development of mass memories. During that timeframe Texas Instruments developed a high-density memory consisting of unpackaged stacked die. It was based on tape automated bonding (TAB) technology (Chapter 11) and featured a bond pad relocation metallization and a gold bumping process, both with the devices in wafer format. Following singulation, the die are attached to the TAB tape and electrically tested. Electrically good devices are then stacked forming a cube. The TAB leads are needed on one side only, and serve as pins for attachment to a substrate. This is illustrated schematically in Figure 5-9(a). Figure 5-9(b) shows

an actual cube attached to a substrate and includes quantitative data comparing the memory capacity of the cube versus packaged devices, in through-hole (DIP), SMT (flat pack), and 2D MCM approach. Note that the total capacity of the cube will be dependent upon the memory capacity of the individual die.



(a)Schematic Stacked TAB Bonded Memory Die



(b)Memory Stack

(Courtesy Texas Instruments)

Figure 5-9. (a) Schematic 3-D Memory Cube; (b) TI's 3-D Memory Cube

Die stacking is basically the physical assembly of one or more die directly over previously attached die, "piggy back" style. Today the most popular die stacking technology is straightforward die-on-die using wire bonding as Figure 5-10(a) is an actual wire bonded 2-die stack. Figure 5-10(b) is a cross-section of a 2-die stack with one flip chip bonded die and a second die wire bonded. It is the complete electronics for a hearing aid and dates back to the early 1990s.

(Courtesy Intel Corp.)

Figure 5-10(a). Wire Bonded Stacked Die

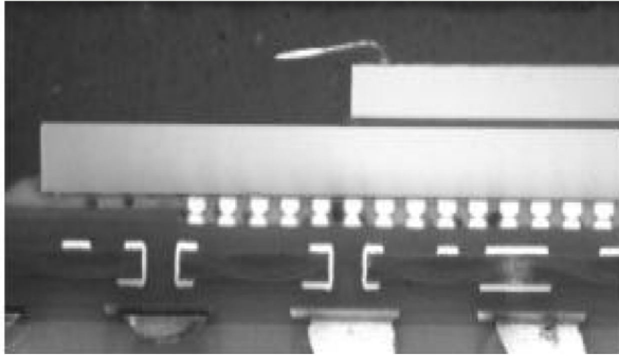


Figure 5-10(b). 2 Die Stack Flip Chip/Wire Bonded

While a portion of the die stacking process follows conventional chip & wire assembly there are exceptions and begin with the die. In order to keep the final package as thin as possible all die to be stacked are thinned while still in wafer format. A sample assembly process is presented in Figure 5-11. The die attach adhesive for stacking is typically a silicone and is applied as a film or preform. In some cases it is deposited onto the wafer after thinning but prior to die singulation.

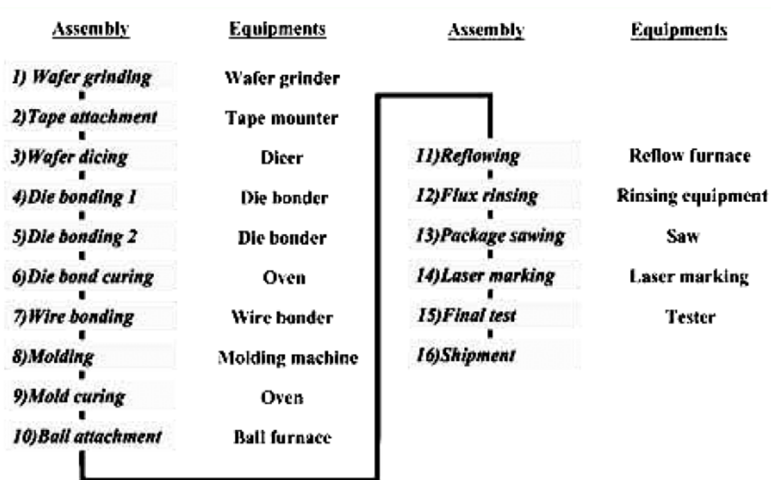
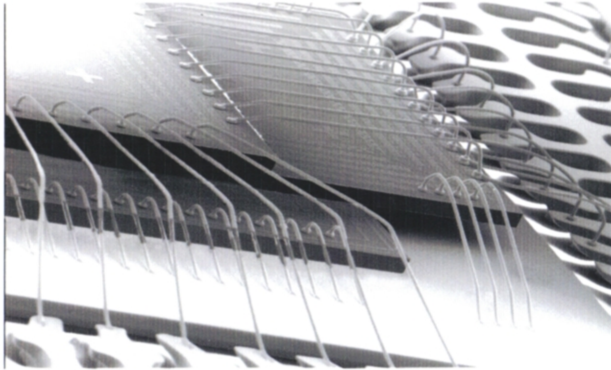


Figure 5-11. A 2 Die Stacking/Package Process Flow

With stacked die the wire bonding, in particular the wire loop profile, is critical. Figure 5-12 shows a SEM of a 3-die stack illustrating the different die orientations and wire loop profiles dictated by the location of the die in the stack. Figure 5-13 is a 4-die stack in which two die of the same size require the insertion of a "spacer", typically a blank Si die, to provide needed separation for wire bonding. Note that the conventional ball bond on the top die has been modified to present an ultra low wire loop from the die pads to the substrate. Figure 5-14 shows the many stacking

configurations that are now becoming available. Note that die stacking is readily incorporated into MCM assemblies as well.



(Courtesy Kulicke & Soffa)

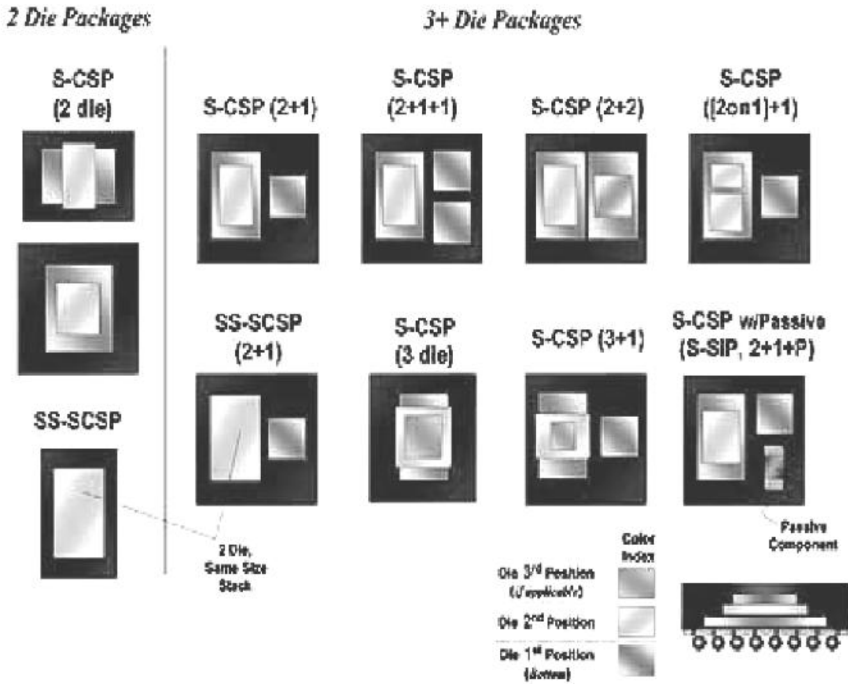
Figure 5-12. 3 Die Stack

(Courtesy Kulicke & Soffa)

Figure 5-13. SEM of a 4 Stacked Die Assembly with 2 Spacers

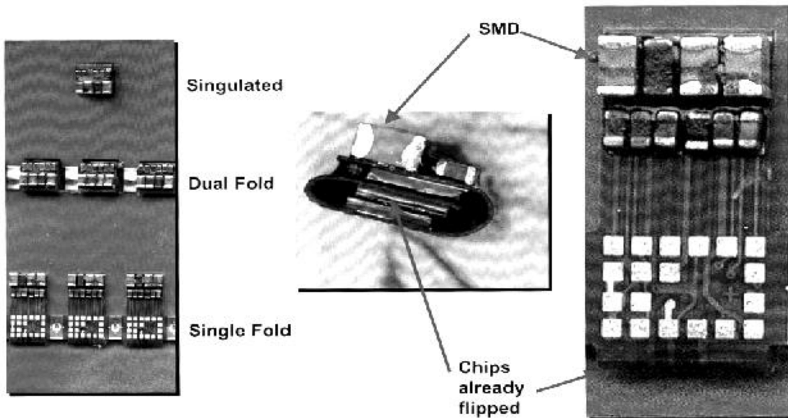
5.5 — 3-D Packaging and the Flex Circuit [10,11]

The flex circuit is used in various applications involving packaging. While typically offering a reduction in size and weight, e.g., the TBGA, and CSP, the flex circuit is also a contributor in several 3-D packaging approaches, in particular, stacked packages and is referred to as "folded flex packaging". The technology takes advantage of the bending capability of the flex circuit. A very early application of the folded flex technology was once again in hearing aids as seen in Figure 5-15. Figure 5-16 is example of the many configurations possible with this packaging technology.



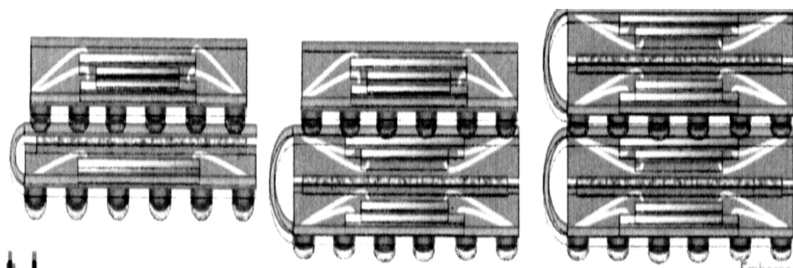
(Courtesy Amkor Technology, Inc.)

Figure 5-14. Various Stacked Die Configurations [6]



(Courtesy Teledyne Microelectronics)

Figure 5-15. Folded Flex: Hearing Aid Application

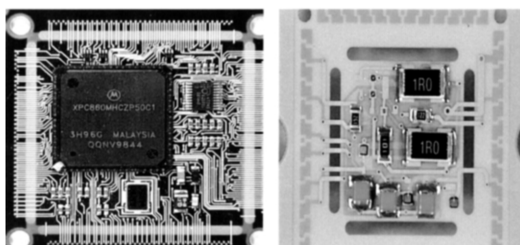


(Copyright 200x, Intel corporation. Reproduced by Permission)

Figure 5-16. Folded Flex Stacked Packages

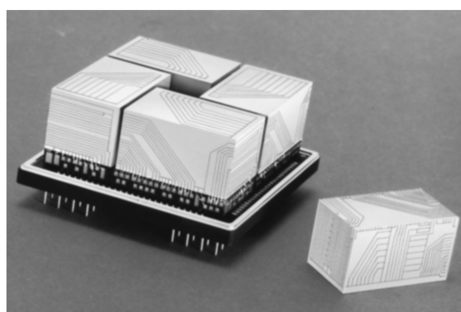
5.5.1 — 3-D Plus Technology [12]

A flex circuit is also the baseline interconnect for a 3-D packaging technology from 3-D Plus [12]. Metallized and patterned flex in a 35mm film format acts as the carrier for both packaged and unpackaged devices as shown in Figure 5-17(a). Individual layers can be electrically tested prior to stacking. The inner layers in the stack are interconnected by conductor traces running vertically along the sides as can be seen in Figure 5-17(b).



(Courtesy 3-D Plus S.A.)

Figure 5-17(a). Flex inner layers with Packaged and Unpackaged Components

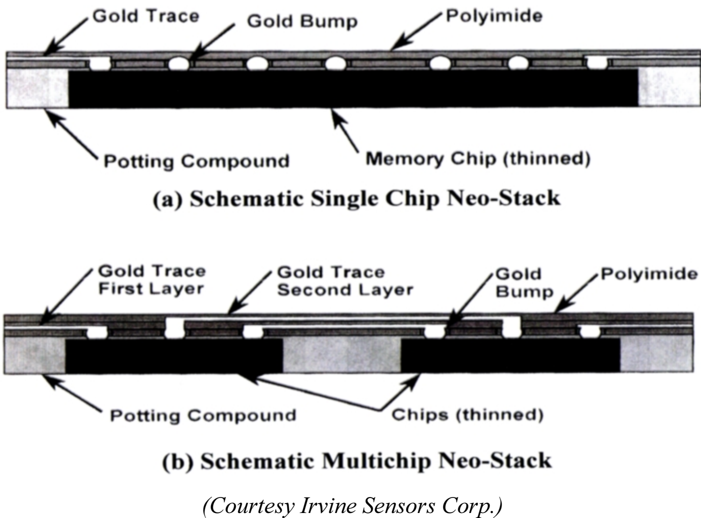


(Courtesy 3-D Plus S.A.)

Figure 5-17(b). Finished Cube Showing Inner Layer Interconnections

5.5.2 — Neo-Stack™ Technology [13]

Another 3-D approach is from Irvine Sensor called Neo-stack™. The patented process features stacked layers each containing one or more devices and a flex (polyimide) film supported conductor interconnect. Figures 5-18(a) and (b) are schematic cross-sections of a single die layer and a multi-die layer respectively. Note that all circuitry terminates at the edges of the flex film. The individual layers following stacking (lamination) are accessed by way of a vertical interconnect shown in Figure 5-18(c). Neo-stack™ uses only fully tested die to enhance yields and negate the need for any rework.

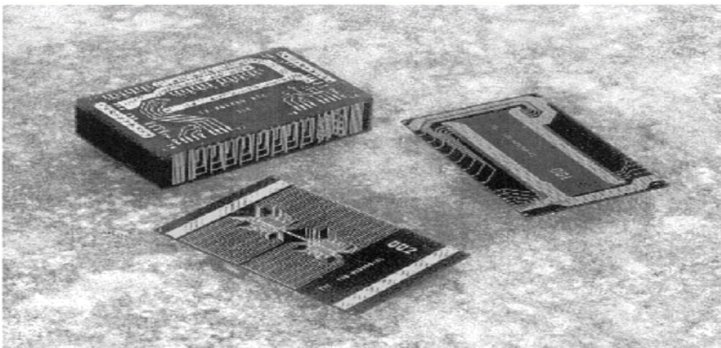


(a) Schematic Single Chip Neo-Stack

(b) Schematic Multichip Neo-Stack

(Courtesy Irvine Sensors Corp.)

Figure 5-18. (a) Single Chip Neo-Stack™ inner layer; (b) Multichip Inner Layer



(Courtesy Irvine Sensors Corp.)

Figure 5-18(c). 19-Layer Smart Flash Stack including Two Neo-Stack™ Layers

5.6 — Die Stacking Using Silicon Thru-Vias [14–19]

While the die stacking as discussed significantly increases packaging efficiency and improved performance, further enhancement in the latter can still be realized. In actuality the various stacking structures shown are not true 3-D (sometimes referred to as 2½D) since interconnects (wire bonds) are all at the die perimeters. True 3-D (vertical integration) requires that the metallization layers that interconnect multiple transistors on an IC be interconnected in the vertical direction within the stack. The technologies required for fabricating the vertical interconnects and the die stacking make use of both semiconductor process technologies as well as MEMS based processes. Aggressive development efforts are on going, including some government funded (DARPA) programs. Active programs on vertical device integration are in-place at several R&D facilities (e.g. MCNC-RDI, Fraunhofer-Munich, ASET Japan), start-ups (e.g. Ziptronix) and at major semiconductor companies (e.g. IBM, Toshiba, Infineon). Mainstream manufacturing is predicted in some cases, as soon as a late 2007–2008 timeframe.

5.6.1 — Vertical Interconnect Processes

To achieve die stacks with vertical interconnections the die to be stacked must first have been designed and manufactured specifically for stacking using vertical interconnects. Then these structures require metallized and filled through vias in the body of the silicon die. The silicon-through via process in one case involves reactive etching of the silicon to form the via, followed by the deposition of a dielectric layer (SiO_2), then a conductive seed, layer (TiN/Cu). An electroplated Cu to filling the via follows. Typical dimensions for a through-via is 10µm on a side. The etching is anisotropic resulting in extremely straight sidewalls. A graphic description of the process is presented in Figure 5-19(a). Figure 5-19(b) is a metallographic cross-section of a Cu filled via.

Following via formation, there is a wafer thinning operation using chemical-mechanical polishing (CMP). The thinned wafer is now ready for the stacking or bonding process. The wafer bonding is a critical step in the stacking process. Precision alignment of wafer to wafer is required and must be maintained during the actual bonding process that involves application of heat and pressure. Figure 5-20 is a schematic representation of die vertically interconnected and bonded using Cu-Sn-Cu eutectic for attachment. Highlighted are the various materials and interfaces. Note in this example the via fill metal is tungsten, W.

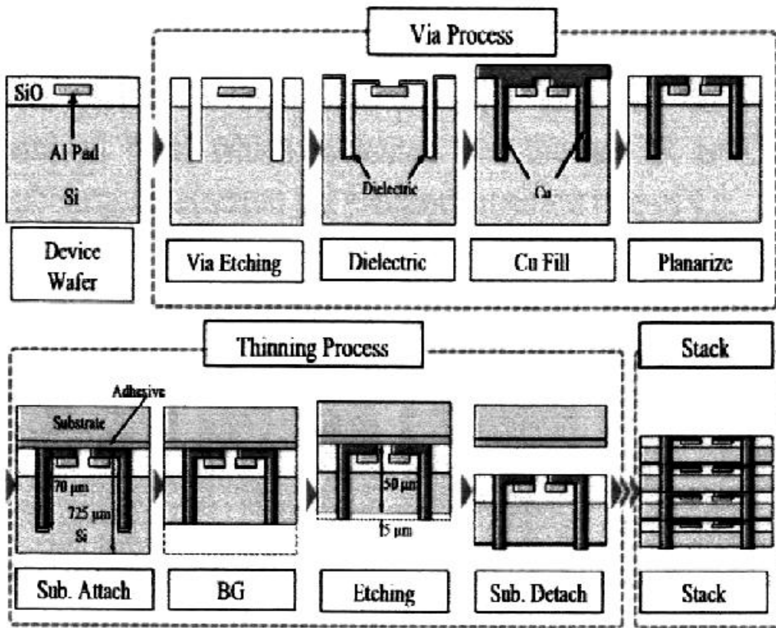


Figure 5-19(a). Vertical Integration Silicon Through-Via Die-to-Die Stacking Process [19]

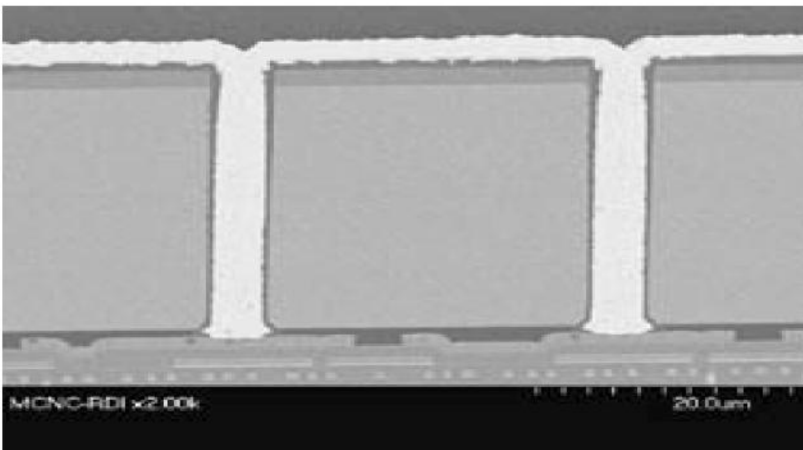


Figure 5-19(b). Cu filled Silicon Through Vias [19]

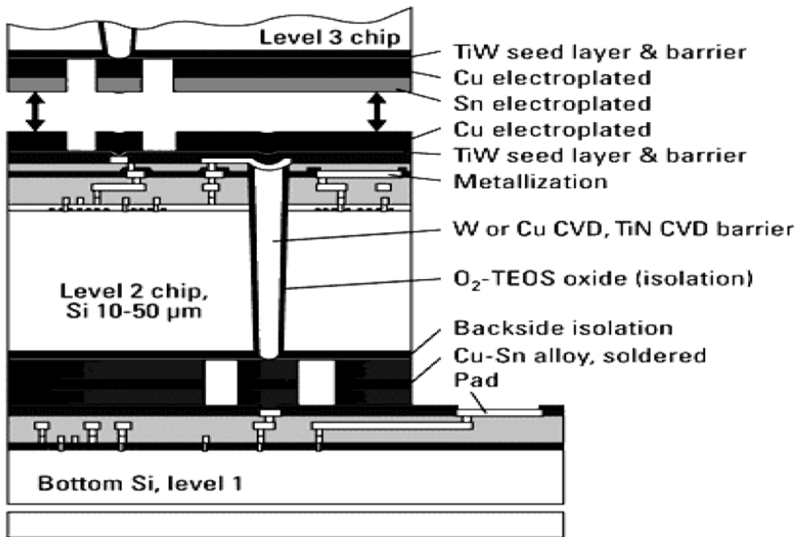


Figure 5-20. Schematic Cross-Section of Vertically Interconnected Stacked Die [19]

5.7 — System in Package (SiP)/System on Package (SoP) [20–23]

The 3-D initiative has spawned new concepts in multichip packaging. The concepts of System in Package (SiP) and System on Package (SoP) are now emerging. Some consider the two to be synonymous, that is, referring to packaging that provides for complete system or subsystem functionality in a minimal form factor. Others deem SiP to be any package that contains *stacked die* with a near-CSP footprint at the board level. SoP, on the other hand is perceived as a package that is essentially a micro-PCB assembly combining packaged and unpacked active and passive components and where the package-substrate interconnect is a critical element in overall system functionality. Figure 5-21 graphically illustrates the salient features of MCM, SiP, and SoP.

Both SiP and SoP concepts are extremely effective solutions to realizing multi-device technologies and achieving necessary system performance in contrast to a monolithic silicon structure, the so-called System on Chip.

While the SiP typically utilizes one device technology, for example CMOS, the SoP readily accommodates different die technologies, (Si, GaAs and SiGe based), as well as different die functions (logic, memory, rf, analog and digital) in the same package. Other technologies such as MEMS and optical components can also be included along with the passive components, as well as antennas, filters and resonators.

SoP component assembly basically incorporates industry standard interconnect technologies—Level 1.0 chip & wire and flip chip, for bare die and Level 2.0 surface mount processes for packages.

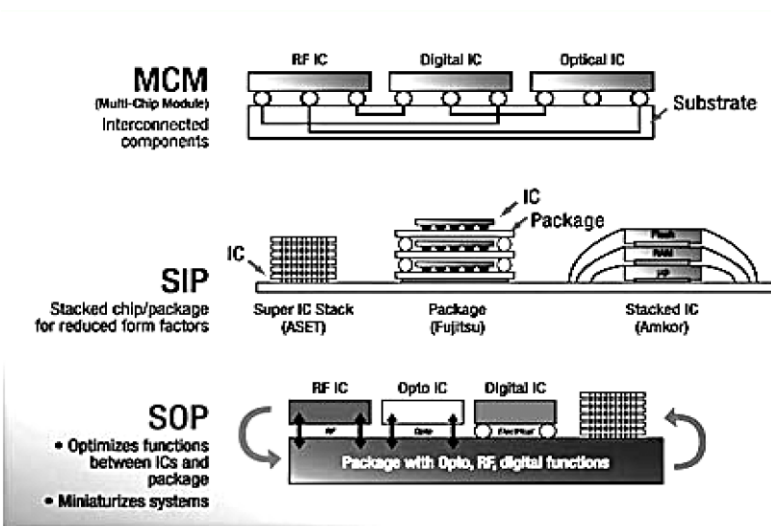


Figure 5-21. MCM vs. SiP vs. SoP [20]

Significant advantages of SiP and SoP versus SoC include shorter development time, lower development cost and lower risk. Table 5-2 lists critical items and the advantages/disadvantages of SiP vs. SOC.

Figure 5-22 presents cost and packaging efficiencies for the various packages and packaging approaches available.

Table 5-2. Advantages of System on Package vs. System On Chip [23]

System on Chip (SOC)	System in Package SiP
✓ Performance driven	✓ Minimum footprint
✓ Larged die, high I/O count,	✓ Z-direction integration
✓ Die/package area ratio <100%	✓ Die/package area ratio >>100%
✓ Long term time to market	✓ Low cost 1.7X
✓ High cost	✓ Short time to market
	✓ Technology mix: CMOS, GaAs, SiGe
	✓ Design mix: analog, digital
	✓ Assembly technology mix: wire bond, flip chip, embedded passives

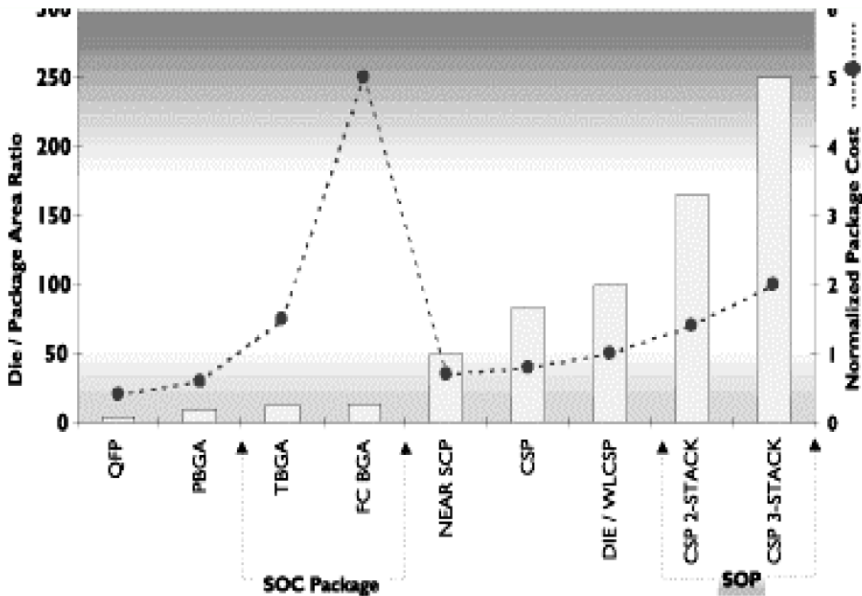


Figure 5-22. Cost/Benefits SiP/SoP vs. SoC [23]

5.8 — Summary—Benefits of Multichip Packaging

MCP, and 3-D in particular, inherently offers the following advantages:

- Application specific functionality—similar to an ASIC but with shorter time to market, lower cost, and potential for optimizing performance and functionality.
- Increased packaging efficiency/miniaturization vs. single chip and multiple packages.
- Improved electrical performance—short interconnects, chips placed closer to each other to enhance signal propagation.
- Allows for use of mixed technologies—Si, SiGe, GaAs, device technologies, to further enhance performance and extend functionality.
- Improved reliability—multiple packages eliminated; total number of interconnects significantly reduced.
- Cost-effective, particularly at the system level.

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6 Known Good Die (KGD)

6 — THE KGD STORY [1]

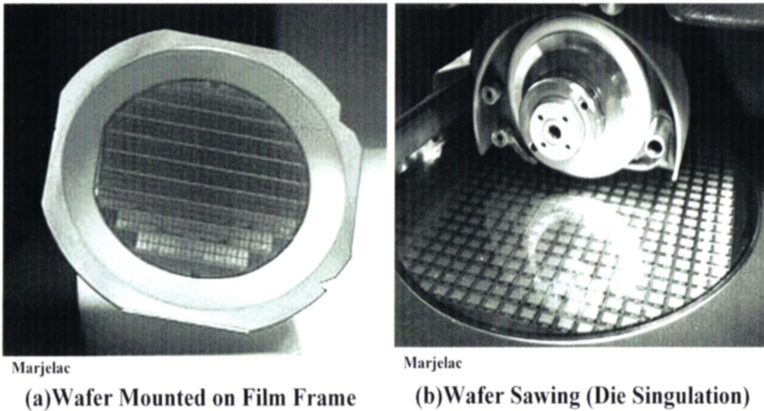
It began with the emergence of the hybrid circuit in the 1960s. The hybrid circuit basically required an expertise that was heretofore totally confined to the semiconductor's "back end" manufacturing. It was not however a matter simply of "copying". This new venture came with its own unique problems that began first with the availability of bare die, and secondly, with the questionable electrical integrity of the die. Available bare die were only minimally tested to specification, limited to wafer probe testing that is basically intended as a screening test only. Thus, a hybrid circuit assembly with multiple die of questionable electrical integrity would run a high probability of failing final electrical testing, resulting in either scraping the part or a "reworking". Rework involves attempting to remove defective die and replacing with another die.

6.1 — The Semiconductor Assembly/Packaging/Test Process

The IC manufacturing "Back End" process covers the assembly, packaging and electrical testing of the IC. "Back End" processing begins following wafer probe where 100% electrical testing of each IC on the wafer occurs. The testing is to determine nominal functionality and is not at the same level as final package testing.

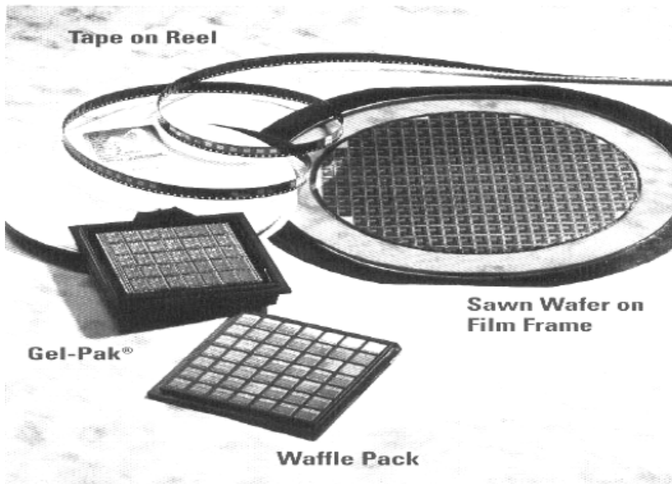
Defective devices on the wafer are identified by dispensing an epoxy dot (inking) or by storing the location of the device (mapping) in a computer database. Yields on mature product at this point will typically be in the very high 90's%. The wafer is next mounted on a film for sawing and die singulation (Figure 6-1). Following a cleaning the film is expanded to further separate the die and facilitating removal of die from the film.

Inked die (defective) die can be removed from the film leaving only those die that passed the electrical testing. The film containing only "good" die can be placed on a die bonder to begin the assembly process, or the die can be picked and placed into waffle packs, GelPaks or in tape (Figure 6-2). It is at this point that bare die become available for subsequent in house assembly or availability to the merchant market.



(Courtesy Majelac Technologies)

Figure 6-1. (a) IC Wafer on Film Frame; (b) Wafer Sawing

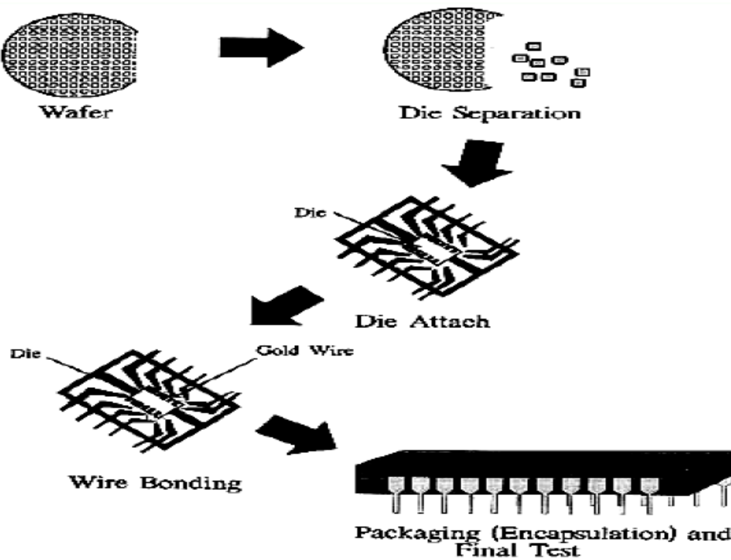


(Courtesy Kulicke & Soffa)

Figure 6-2. Waffle Pack, Gel-Pak®, Tape, Film Frame

6.1.1 — Assembly

Figure 6-3 illustrates the basic assembly process for a plastic encapsulated IC package. The finished, packaged IC is then subjected to full electrical testing and burn-in to verify that the IC meets the manufacturer's electrical specifications.



(Courtesy PTI Seminars, Inc.)

Figure 6-3. IC Plastic Encapsulated Package Process

6.1.2 — MCP Assembly

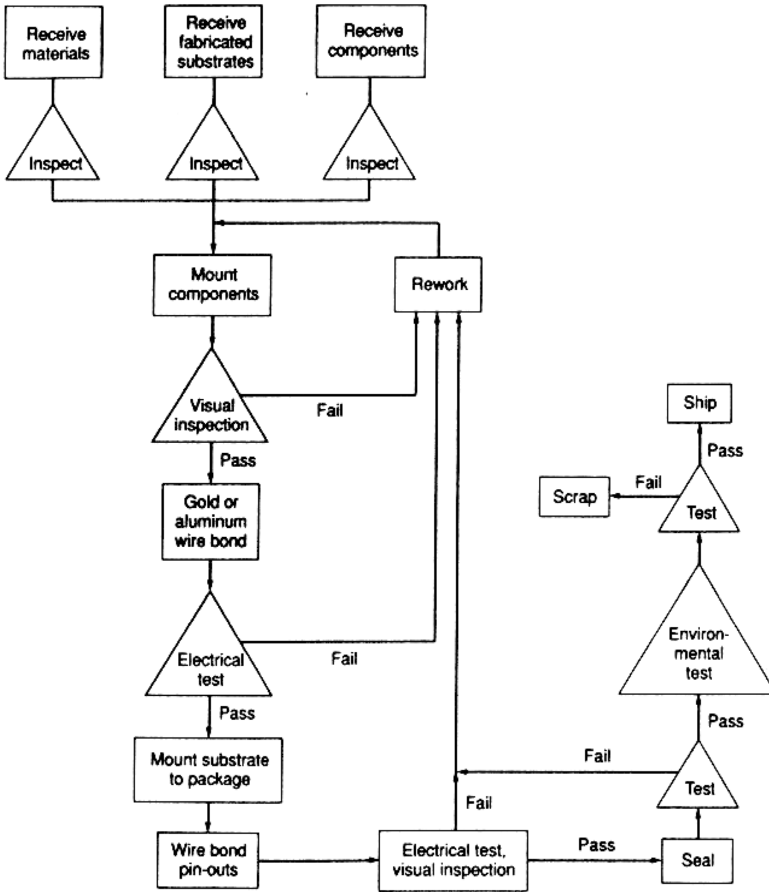
The MCP assembly process quite obviously is more complex. The key to successful implementation of a hybrid circuit as well as more sophisticated MCPs, i.e., MCMs, involves properly addressing the problems associated with working with bare unpackaged die. This includes not just the addition of necessary capitol equipment such as die bonders and wire bonders but putting in place complete die management procedures, covering storage, handling, inspections, and the assembly process. It requires specially trained operators and a technically competent and supportive staff. A typical process flow for an MCP is shown in Figure 6-4.

Note the frequent inspections and how the rework process is integrated into the manufacturing process. The intent is clear: identify both visual defects as well as electrical rejects as early in the process as possible to minimize rework on fully assembled devices when value added is at a premium.

6.2 — The Bare Die Problem [2,3]

Bare die can be obtained from the semiconductor manufacturer, a distributor, or third party chip supplier. Typically, the IC die will be identified by type as well as a "lot number". The lot number indicates all die were processed as a group at the same time.

The major concern however, is the electrical integrity of the die. Unlike packaged devices, the bare die lack the full electrical testing needed to verify conformance to electrical specifications. Bare die also are not normally subjected to burn-in, as is the case with the packaged devices. Thus the early "infant mortality" failures screened out in the burn in process with packaged devices go undetected with bare die. Bare die must therefore be considered only "potentially good" if based only on a wafer probe electrical testing.



(Courtesy Aeroflex, Inc.)

Figure 6-4. MCP Assembly/Test Process Flow

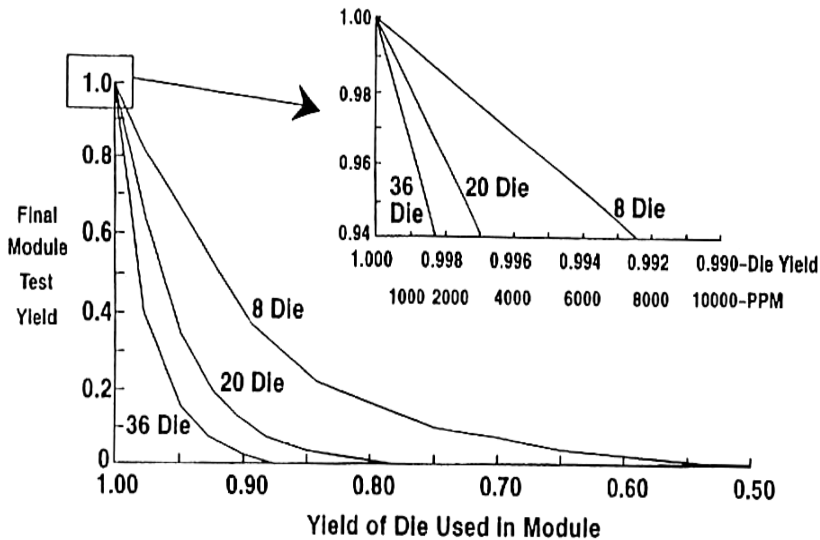


Figure 6-5. Multichip Assembly/Electrical Yield vs. Electrical Yield of Die

The wafer probe is not a "test to spec" because not all testing can be performed until the device is in the package. This lack of confidence in electrical integrity that exists with bare die is critical in *all* multichip packaging and COB applications. It can be a major obstacle to implementation if not taken into consideration in early up-front planning. Defective die adversely affect the electrical yields of all multichip assemblies.

Figure 6-5 illustrates the impact of defective die on multichip electrical yield. For example, an 8 chip module with a "guaranteed" die yield of 99.2% will result in a module yield of 94%. However, if the die yield is only 90%, the module yield would be an intolerable 40%.

The figure also shows that for a given yield of die the module yield decreases with increase in the number of die per module. The more devices the greater the probability that a defective device is present. Thus an MCM containing 2 or 3 die (Few Chip Module, (FCM)) presents a reduced risk factor versus an MCM with 8-10 die.

In any case, in order to avoid loss of an assembly with multiple die, a rework procedure is required to enable defective die to be identified, removed and replaced with another die. The risks associated with rework, however, include the following:

- Potential damage to the substrate bond pads, the conductor interconnect, or the substrate itself in removing a defective die resulting in the need to scrap the entire assembly; and
- Generation of latent or incipient damage that goes undetected that may compromise long-term reliability.

Another problem with rework is: it is *not a solution* but rather a work-around that could easily become unmanageable if the number of assemblies requiring re-work becomes excessive. Rework can be expensive and should only be considered based on cost considerations. If the rework is more expensive than the assembly (silicon and package), the assembly should be scraped.

6.3 — Addressing the Bare Die Problem—Wafer Lot Acceptance Testing

When purchasing bare die in the early days of hybrid circuits,a “Lot Acceptance Test” (LAT) or an “Element Evaluation Test” (EET) was usually requested. LAT involved taking a small sample of die from the lot, assembling it into packages and performing full electrically testing and burn-in. The final yield will include not only the electrical yield through burn-in, but losses that may have been incurred in the assembly. LAT serves as an “indicator” of what can be expected from using die from that specific lot.

Typical LAT sample size is 10 die. A larger sample size will provide a higher level of confidence in the electrical integrity of the die lot. However, there is usually a substantial cost increase associated with the larger sample size.

With ICs currently in production, particularly microprocessors, DSPs and ASICs, LAT may not be a cost effective solution. For these types of devices the cost of the die and the packages needed for testing often make this approach prohibitive.

Additionally, while the number of devices per package is critical the types of devices involved are also a factor. The more mature the devices (length of time in high volume production), the greater the level of confidence will be in the wafer probe testing and the subsequent integrity of the die. ASIC devices on the other hand, will usually lack extensive manufacturing history of electrical yields. Correlation between wafer electrical yield vs. final package yield is simply not always available. Effective wafer testing based on long-term experience, will directly impact final package electrical yield.

6.4 — Known Good Die (KGD) [4,5]

The Acronym, KGD, was coined in the late 1980s to identify bare die that were subjected to additional electrical testing and/or stress screenings following singulation to verify that the die are in fact electrically “good”. Significant interest in and requirements for KGD coincided with the increased activity in Multichip Modules and has continued in supporting stacked die and SiP/SoP applications.

Many of the semiconductor manufacturers who had previously shown little interest in even selling bare die, have been driven by increased demands and have initiated efforts directed towards developing programs to make KGD available.

Various approaches evolved that included the following:

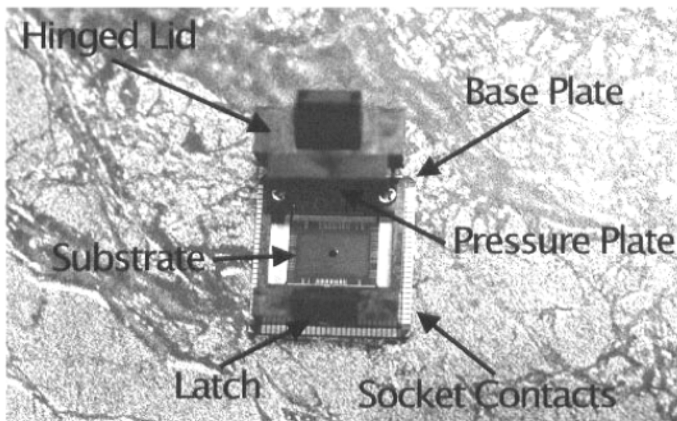


Figure 6-6. The DiePak Die Carrier

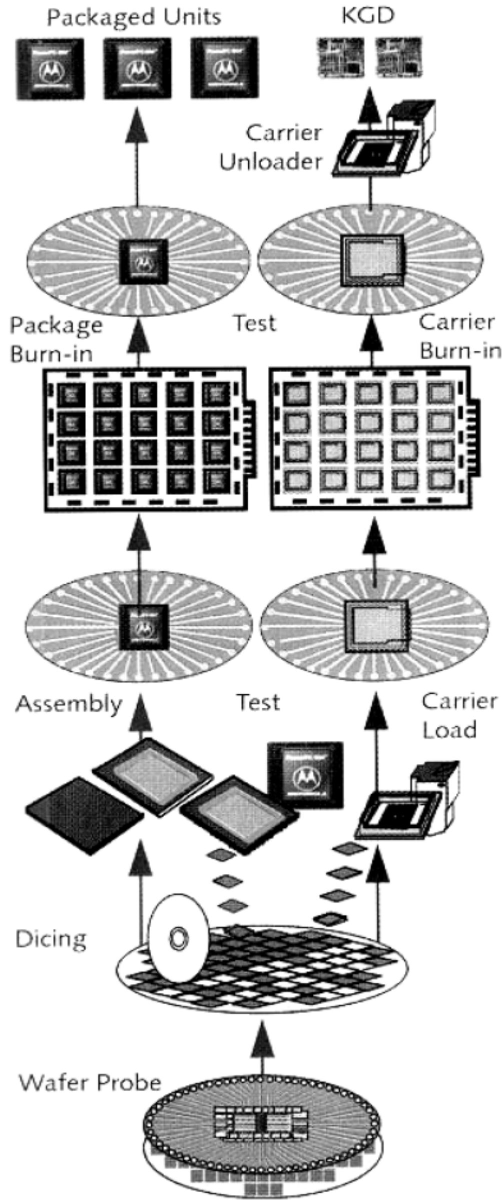
- More extensive die testing in wafer format with or without added stress screening such as testing at high and low temperatures at wafer probe.
- Placing the die in a temporary carrier allowing for complete electrical testing and burn-in. A die carrier (DiePak from Aehr Systems) is shown in Figure 6-6.

In this latter case, the process developed includes automatic die loading and unloading, pre-burn-in test, burn-in, and final testing, and finally shipping of KGD. Figure 6-7 illustrates the process flow for both bare die and packaged devices.

One ASIC manufacturer offers 4 KGD test options ranging from room temperature and high temperature (125°C) wafer probing only, to 3 different levels of testing that includes burn-in using die carriers. The first option adds a wafer probe but at an elevated temperature (Option 1). Figure 6-8 describes more extensive KGD test procedures involving the use of temporary carriers (Options 2, 3, and 4).

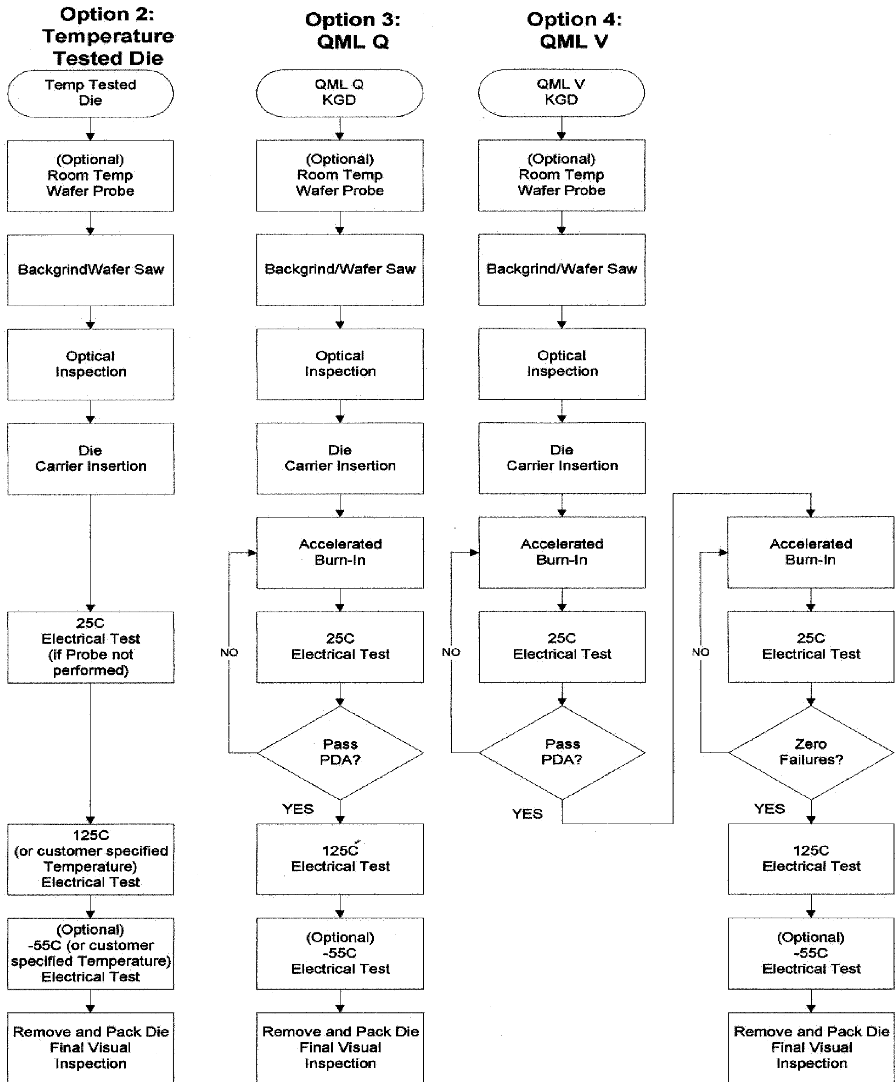
KGD does not come without problems, notably, cost and reliability concerns. Cost for KGD can be excessive. KGD carriers, for example, can be expensive and a dedicated carrier is required for each IC type. Obviously the cost factor can be amortized with high volumes, but for low volume types alternative approaches must be considered.

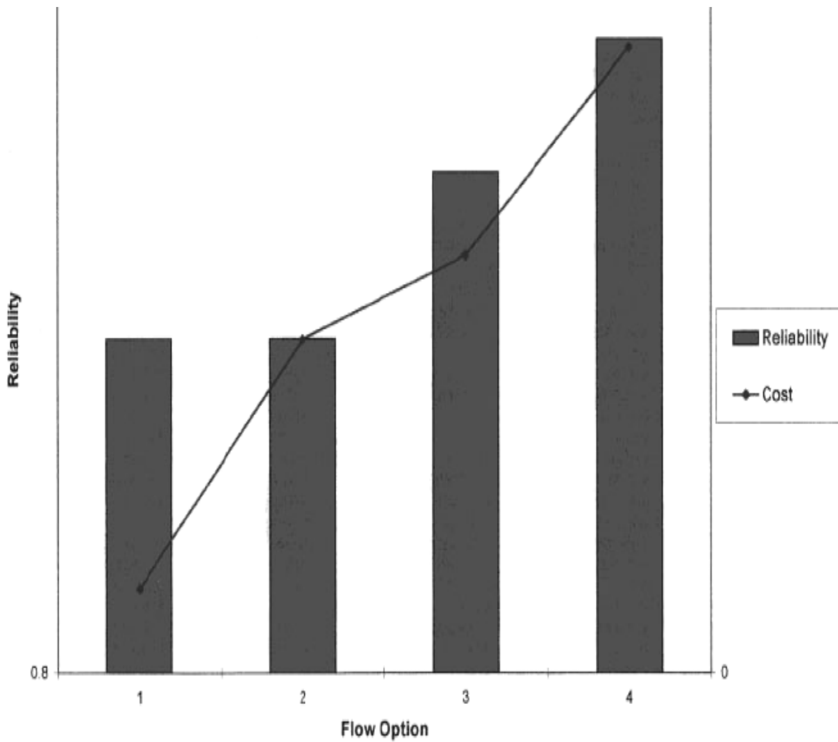
The cost factor thus becomes toatally dependent on the end product requirements, for example, for the more critical military application, KGD can be warranted. On the other it might be hard to justify the added cost for KGD for use on commercial end products. Figure 6-9 shows cost/reliability tradeoffs based on the KGD test options presented in Figure 6-8.



(Courtesy Freescale Semiconductor)

Figure 6-7. Die Flow for Package Device and KGD Die in Temporary Carrier


Option 2:
Temperature
Tested Die
Temp Tested
Die
(Optional)
Room Temp
Wafer Probe
BackgrindWafer Saw
Optical
Inspection
Die
Carrier Insertion
25C
Electrical Test
(if Probe not
performed)
125C
(or customer specified
Temperature)
Electrical Test
(Optional)
-55C (or customer
specified Temperature)
Electrical Test
Remove and Pack Die
Final Visual
Inspection
Option 3:
QML Q
QML Q
KGD
(Optional)
Room Temp
Wafer Probe
Backgrind/Wafer Saw
Optical
Inspection
Die
Carrier Insertion
Accelerated
Burn-In
25C
Electrical Test
NO
Pass
PDA?
YES
125C
Electrical Test
(Optional)
-55C
Electrical Test
Remove and Pack Die
Final Visual
Inspection
Option 4:
QML V
QML V
KGD
(Optional)
Room Temp
Wafer Probe
Backgrind/Wafer Saw
Optical
Inspection
Die
Carrier Insertion
Accelerated
Burn-In
25C
Electrical Test
NO
Pass
PDA?
YES
Accelerated
Burn-In
25C
Electrical Test
NO
Zero
Failures?
YES
125C
Electrical Test
(Optional)
-55C
Electrical Test
Remove and Pack Die
Final Visual
Inspection



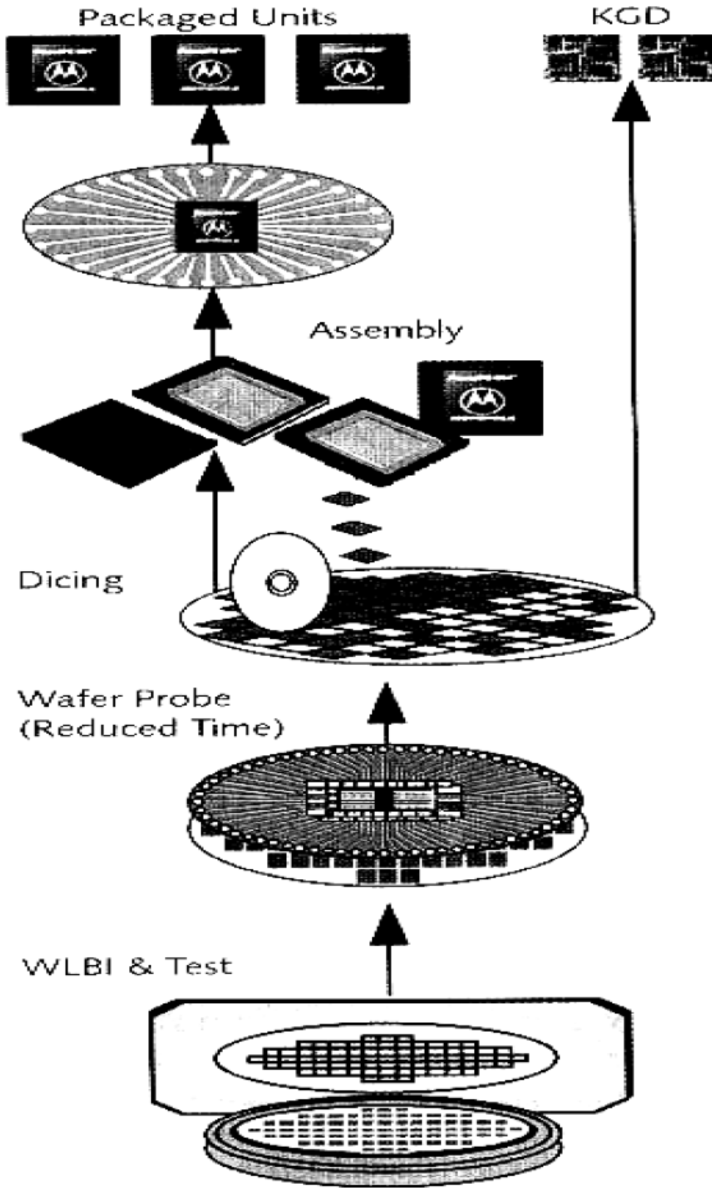
(Courtesy Aeroflex, Inc.)

Figure 6-9. Cost/Reliability Tradeoffs

6.5 — Wafer Level Burn-in and Test (WLBT) [6–8]

Driven by the continued interest in MCP, in particular, the emergence of Stacked Die Packaging, Wafer Level Packaging and SiP/SoP, active development of more cost-effective techniques for improving the availability of KGD has continued. Figure 6-10 shows the process in development for providing KGD through extensive testing and burn-in while the devices are in wafer format.

This approach is dependent upon the use of a full wafer contactor, which may be a probe card or a sacrificial metal layer that is removed following testing. This is the most cost-effective KGD process and is also extremely attractive to the semiconductor manufacturer since it effectively eliminates loss of costly packages resulting from the presence of defective die entering the assembly area.



(Courtesy Freescale Semiconductor)

Figure 6-10. Wafer Level Burn-in and Test

6.6 — Industry Responsiveness

Lack of KGD should not be considered a roadblock to MCP, for example Few Chip Modules (FCM), with roughly 4 or less die, are not nearly as prone as modules with many die. Availability of KGD is, however, a critical aspect of successful implementation and continued development of many MCP technologies, in particular. the "chips first" and die stacking technologies. All major semiconductor manufacturers have KGD programs in place. In addition, several third party chip suppliers offer KGD programs as well. A consortium was also established in 2000 to support and coordinate industry activities in KGD. The Die Product Consortium (DPC) is "… an ongoing project to develop methods that promote improved die product quality, reliability, handling, shipping and associated infrastructure". The consortium membership is comprised of several semiconductor manufacturers including Motorola, Intel, IBM, National Semiconductor, Texas Instruments, LSI Logic and Samsung Electronics.

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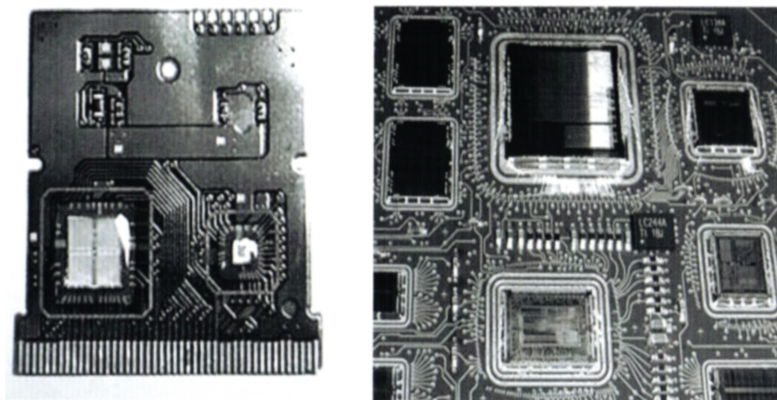
7 Packaging Options—Chip on Board

7 — DIRECT CHIP ATTACH (DCA) AND CHIP ON BOARD (COB)

The phrase, Direct Chip Attach (DCA) refers to the *assembly of bare die to a package or substrate* and applies to SCP, MCP or COB applications [1]. It usually includes a connector as part of the assembly for attachment to Level 3.0 The connecter distinguishes a COB assembly from an MCM-L. COB, historically, has referred to chip and wire assembly of bare die to a second level PWB. COB, in this particular case, is significant because it effectively bypasses assembly of the die into a package and the subsequent assembly of that package to the PWB. As a result it presents itself as a "packageless" IC packaging option. With elimination of the package there is a significant reduction in both size and weight to be realized. Figure 7-1 contains examples of COB assemblies, a few chip COB and a high density multichip assembly. COB can also be combined with SMT components on the same board as illustrated in Figure 7-2.



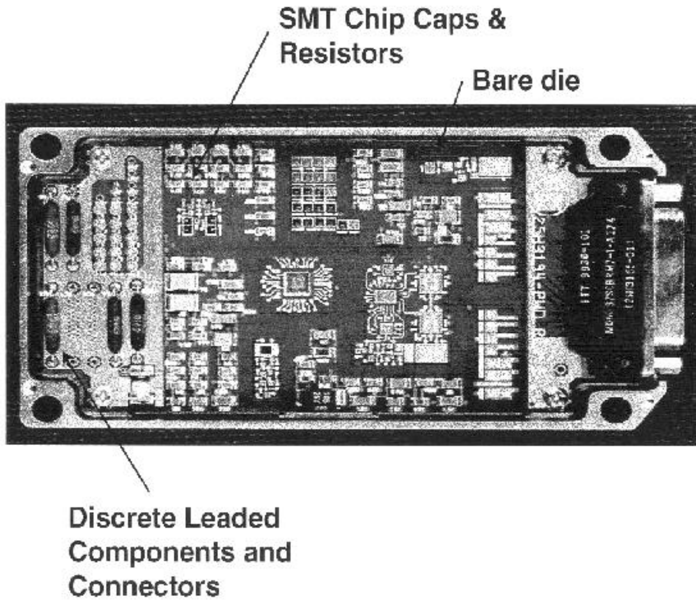
(Courtesy De Products Consortium) *(Courtesy Interconnect Systems Inc.)*

Figure 7-1. (left) Chip on Board Assembly; (right) MCM-L

7.1 — The COB Process [2,3]

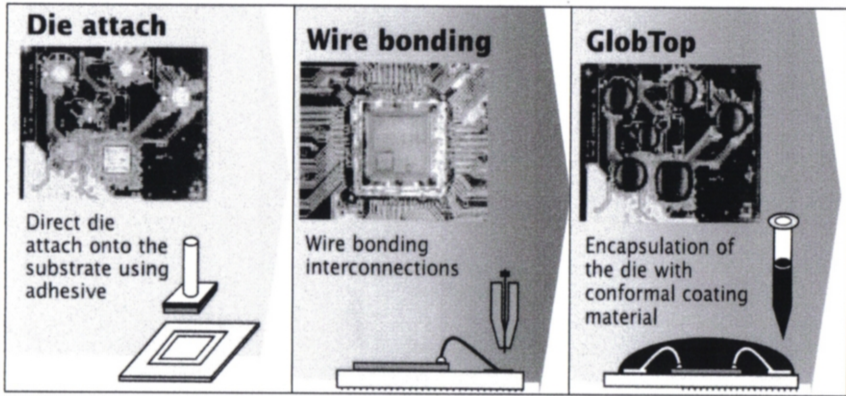
With the emergence of the organic substrate as a viable alternative to ceramic COB terminology now applies to SCP (the PBGA) and MCP (an MCM-L) applications covering Level 1.0 and Level 2.0 assemblies.

The COB process involves three basic steps—epoxy die attach, wire bonding, and an encapsulation step. Figure 7-3 graphically illustrates the complete COB process. COB utilizes chip & wire assembly, a mature interconnect technology with an established reliability and infrastructure within the semiconductor industry. However, direct application of the same processes to an organic substrate is not practical. Organic boards present unique problems related primarily to wire bonding. The wire bonding process operating window is much smaller as a result. Bonding parameters, and in-process controls used with ceramic substrates must be modified. For example, the inherent temperature limitations and the "softness" of organic substrates adversely affect both the thermosonic Au and the room temperature ultrasonic Al wire bonding processes. The wire bonding for COB is therefore more restrictive, requiring more stringent substrate material specifications and tighter in-process monitoring and controls. COB also requires a qualified technical supporting staff and properly trained operators to be in place.



(Courtesy Aeroflex)

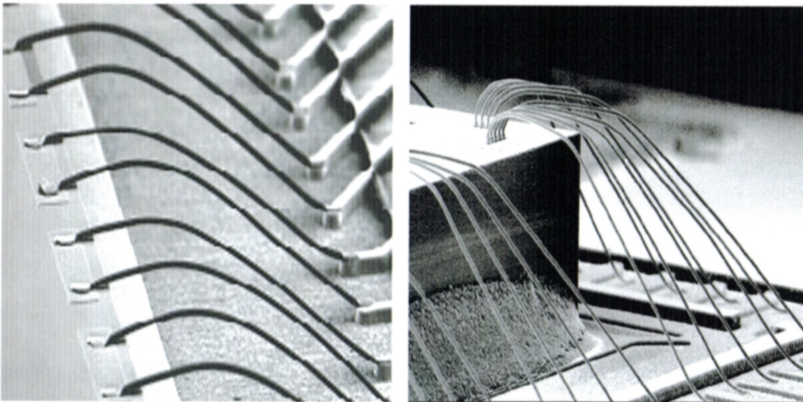
Figure 7-2. SMT/COB Assembly



(Courtesy C-MAC Micro Technology)

Figure 7-3(a). COB Assembly: Die Attach, Wire Bonding, Encapsulation (Glob Top)

Only adhesives are used for die attachment because of temperature limitations with organic boards. The wire bonding for COB is typically Al ultrasonic wedge bonding or thermosonic gold ball bonding (Figure 7-3). The copper cladding on the PWB must be overplated with nickel (Ni) and gold (Au). The thickness of both the Ni and Au are critical and dependent upon whether the bonding is ultrasonic Al or thermosonic Au. Al ultrasonics is a room temperature process while thermosonic is at an elevated temperature.



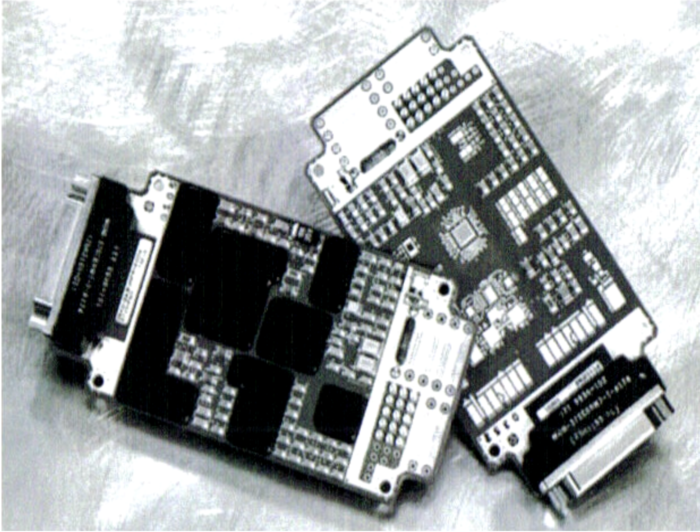
(b) (c)

(Courtesy National Semiconductor)

Figure 7-3. (b) Wedge Bonding on PWB; (c) Ball Bonding on PWB

7.1.2 — Encapsulation

Encapsulation is necessary with COB assemblies to provide both mechanical and environmental protection. The encapsulation, commonly called "Glob Top", is shown in Figure 7-4.



(Courtesy Aeroflex, Inc.)

Figure 7-4. Assemblies Before and After Glob Top Encapsulation

Table 7-1 is a list of some of the materials available for encapsulation including both the material properties and comments. All are applied by a dispensing process, except for paralyene, which is deposited by vacuum vapor deposition.

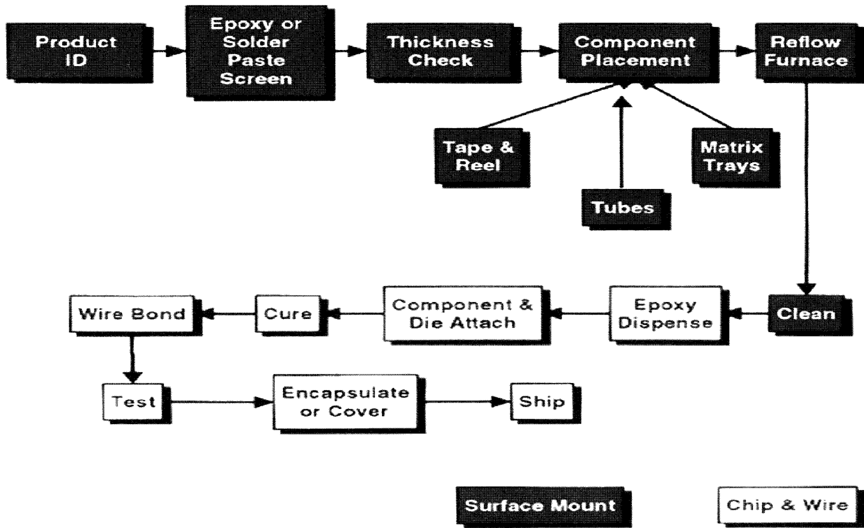
7.1.3 — Level 2.0 Assembly Compatibility

COB can readily be incorporated into through hole and surface mount assemblies as shown in Figure 7-5. In these type of mixed technologies, the COB portion of the assembly occurs after the through-hole and surface mount assembly has been completed.

The actual footprint area required on the PWB will be a function of the wire bonding process and the printed wiring board minimum line width/space capability, and the area needed for the encapsulation. Ideally footprint bond pads that match those on the die, in terms of size and pitch, will yield the minimum area for attachment. To this minimum area must be added an area extending beyond the substrate bond pads for the encapsulant, as seen in Figure 7-4.

Table 7-1. Encapsulants for COB [1]

Coating Material	Properties	Comments
Epoxy Resin	▪ Excellent chemical resistance ▪ Excellent mechanical properties ▪ Excellent wetting for application ▪ Good adhesion ▪ Acceptable moisture barrier	▪ Needs compliant buffer ▪ Coating for low stress ▪ Rework is very difficult ▪ short shelf life (one component)
Silicone resin	▪ Excellent electrical properties: dielectric constant and loss factor ▪ Mechanically tough and flexible ▪ Resistant to high temperature ▪ Lower moisture absorption than epoxy ▪ Low stress after cure	▪ High coefficient of thermal expansion compared to acrylic and epoxy resins ▪ Low resistance to hydrocarbons ▪ High cost
Polyurethane resin	▪ Good mechanical properties: toughness, abrasion resistance and flexibility ▪ Good adhesion to die and substrates ▪ High chemical resistance ▪ Low moisture absorption ▪ Low viscosity ▪ Low cost	▪ Most widely used ▪ Stable only to 135˚C ▪ Flammable ▪ Difficult to rework ▪ Unsuitable for high frequency circuits
Acrylic resin	▪ Excellent moisture resistance ▪ Good dielectric properties ▪ Poor chemical resistance ▪ Poor mechanical abrasion resistance ▪ Easy application ▪ Fast drying	▪ Easy to rework ▪ Suitable for automated, high volume production ▪ Ultraviolet curable ▪ Modification available (urethane acrylic)
Parylene (Paraxylylene)	▪ Penetrates hard-to-reach places (applied as vapor) ▪ Excellent chemical, mechanical, and electrical properties ▪ Excellent moisture resistance	▪ Masking of non-coated areas difficult ▪ Difficult to rework ▪ Needs expensive equipment to apply



(Courtesy Teledyne Microelectronics)

Figure 7-5. SMT/COB Process Flow

7.2 — Flip Chip On Board (FCOB) [4,5]

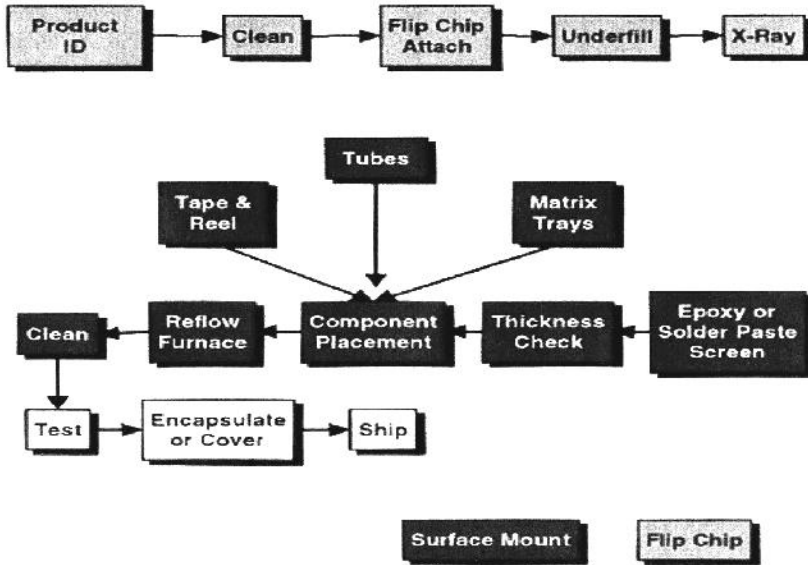
Flip Chip, sometimes referred to as the "Ultimate Surface Mount Device" is completely compatible with a through-hole/SMT assembly. Figure 7-6 shows the process flow for a flip chip and SMT mix assembly line.

Because it is solder attached, flip chip, like the BGA and the CSP, has the ability to "self-align" during reflow. "Self-alignment" allows for misalignment at device placement by as much as 25% to 50%. As a result, flip chip can in some instances be assembled using existing SMT assembly equipments requiring only modifications for pick up of the die. Fully automatic flip chip assembly equipment has now been developed capable of accurate placement at very high throughput, enhancing the inherent low cost features of this assembly technology.

7.2.1 — Flip Chip on Board Assembly

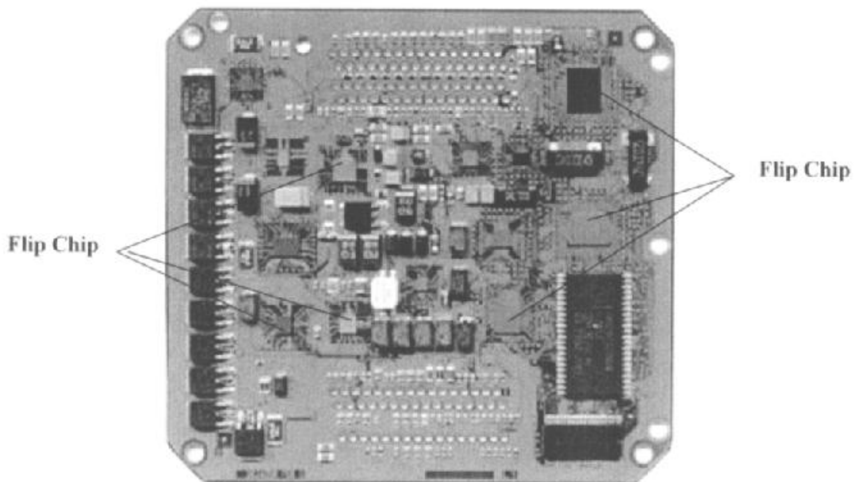
For reliability reasons an underfill is required in most FCOB applications to extend life cycle performance under thermo-mechanical stresses. The underfill also negates the need for any encapsulation. An FCOB assembly is shown in Figure 7-7.

Table 7-2 is a comparison between COB and Flip Chip while Figure 7-8 shows area size advantages for COB, TCOB, and FCOB vs. SMT.



(Courtesy Teledyne Microelectronics)

Figure 7-6. Flip Chip/SMT Assembly Process

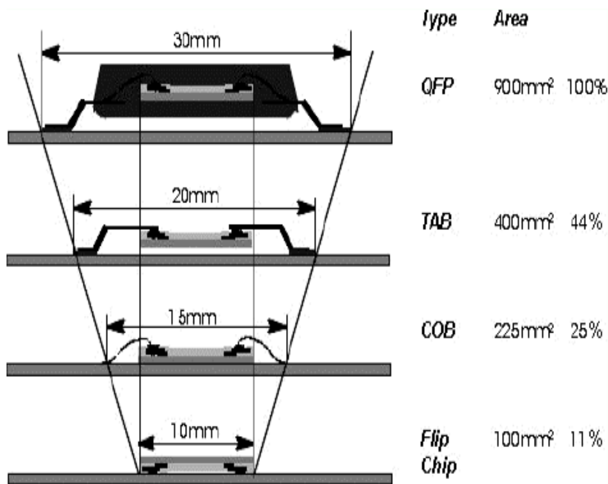


(Courtesy Delphi Autmotive Systems)

Figure 7-7. SMT/Flip Chip on Board, FCOB

Table 7-2. COB vs. FCOB/WLP [4]

Item	Chip On Board (COB)	Flip Chip (FC)/Wafer Level Packaging (WLP)
Package Type	N/A	▪ Real chip size package
Device Body Size	• Same as chip size	▪ Same as chip size
Terminal Design of Device	▪ All terminal pads located in adaptable pitch on chip	▪ All terminal pads located in adaptable pitch on chip
Quality Assurance of Device	▪ Difficult (especially burn-in test)	▪ Easy
Interconnection of Board	• Wire Bonding (WB)	▪ Solder ball terminal
Mounting Area on Board	▪ Same as chip for FCB ▪ Slightly larger than chip area (fan-out for WB)	▪ Same area as chip size
Reliability after Board Mounting	▪ Encapsulation material required	▪ WLP – near equal to conventional package; May require underfill ▪ Underfill required for FC
Mountability on Board	▪ Facility for bare chip assembly required ▪ Difficult to repair/rework	▪ Multiple parts reflow available ▪ Compatibles w/ SMT assembly processes



(Courtesy National Semiconductor)

Figure 7-8. Comparing QFP, TAB, COB, Flip Chip Footprint on PWB

7.3 — Summary

COB/FCOB offer the following:

- A reduced manufacturing process—die assembled directly to second level interconnect, the PWB.
- COB can be incorporated into SMT lines. FCOP completely compatible with SMT.
- Reduced size, weight and attachment area at board level results in board assembly miniaturization with an increased PWB packaging efficiency.
- A low profile assembly.
- Enhanced reliability—no package "problems" and less connections and
- Improved electrical performance—package parasitics eliminated.

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8 Chip & Wire Assembly

8 — CHIP & WIRE ASSEMBLY [1]

Chip & Wire assembly involves the attachment of the die to a package or substrate followed by connecting wires from the die bond pads to the same package or substrate. Bell Laboratories originally developed this attachment technology in the late 1950s for the assembly of silicon planar transistors. Three connections were needed, one to the back of the Si die, the collector electrode, and two to the top surface, the emitter and base electrodes. Attachment to the collector was achieved by alloy bonding the die to a gold plated package. This was realized by placing the Si die in contact with the Au plating while simultaneously applying heat (~400ºC), agitation, and pressure.

Attachment to the emitter and base electrodes involved bonding Au wires (1 or 2 mils diameter) by application of heat (~350–400ºC) and pressure (~40–80 gram force). This "thermocompression" (TC) bonding process was totally operator dependent and a fully manual operation. The operator was required to separately align the wire and the bonding tool, first to the pads on the die and then to the package pads. A "wedge" shaped bond was formed at the die pad and the package similar to that shown schematically in Figure 8-1.

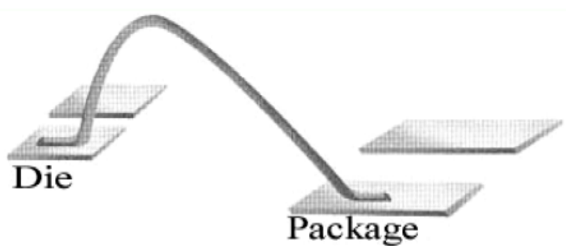


Figure 8-1. Classic Wedge Wire Bond

8.1 — Die/Wire Bonding and Bonder Equipment Development [2]

Specially designed, but manually operated die bonders and wire bonders were used early on for assembly. Highly skilled and specially trained operators were essential for both the die and wire bonding processes. Manual assembly was therefore labor

intensive and quickly became a cost factor in transistor manufacture. This necessitated significant machine related development efforts.

There were also process related reliability problems that had to be addressed associated with the thermocompression method of wire bonding. For example, the high temperatures required for wire bonding resulted in rapid interdiffusion of the Au and Al and the formation of an intermetallic, $AuAl_2$, referred to as "purple plaque", formed at the interface of the wire and the bond pad. The intermetallic, being extremely brittle was the source of frequent catastrophic electrical failures, i.e., "opens", with many devices.

To address this problem ultrasonic Al wire bonding was developed that allowed for a monometallic bond to be formed between the Al wire and the Al pad on the die. Bonding to the die and the Au plated package were achieved at room temperature. While largely resolving the "purple plaque" problem, ultrasonic wire bonding was even more labor intensive and less productive than thermocompression.

At the time, many of the transistor manufacturers were actively working in-house on new machine developments. These activities were directed towards improving the overall productivity by reducing both the operator dependence (labor content) while at the same time addressing reliability problems.

The burgeoning transistor business also attracted outside equipment manufactures to become involved. At the forefront was Kulicke and Soffa, K&S, a specialty machine manufacturer, who became involved with Bell Labs early on, assisting in very early wire bonding equipment development. K&S subsequently became the first merchant equipment supplier of die bonders and wire bonders to the semiconductor industry. K&S was and remains today a major contributor in advanced development of wire bonding technology.

In addition to the ultrasonic wire bonder, early machine developments attributable to K&S included the Au Ball Bonder and the Thermosonic (TC/US) Wire Bonder. All represented significant advancements in wire bonding technologies.

Perhaps most noteworthy of these early developments was the Au Ball Wire Bonder and the introduction of the "capillary" bonding tool. This combined the wire and the bonding tool as a single entity rather than separately. The wire was inserted and automatically fed into the bonding tool and the operator only had to align the tool containing the wire to the bond pads. An added feature, from which the bonder got its name, was the formation of a Au ball at the tip of the capillary created by a small hydrogen flame—later replaced with an Electronic Flame Off (EFO) that melted the tip of the wire. The ball, which was approximately 3 times the diameter of wire, was bonded to the die bond pad using the capillary. This provided for a larger bond area at the die pad and a more robust joint (Figure 8-2).

The thermosonic bonder combined thermocompression and ultrasonic energy to achieve a bond. The ultrasonics allowed both the temperature and the pressure to be significantly lowered. Au wire bonding could then be reliably achieved at temperatures as low as 100°C rather than the higher temperatures for thermocompression. The operator however, still had to align the bonding tool to the die and package pads.

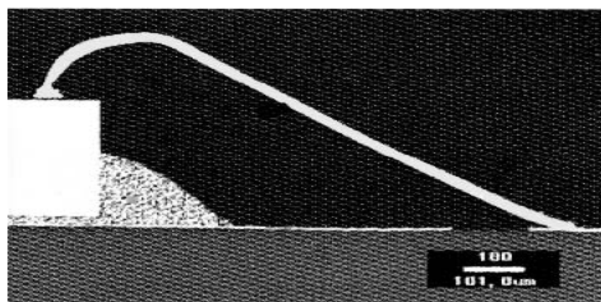


Figure 8-2. Classic Wire Ball Bond

8.2 — Impact of the IC on Bonding and Bonder Development

Problems associated with assembly of the transistor were exacerbated by the integrated circuit. The number of wire connections increased from that required for a single transistor from 2–3 to 8–10 for the very early ICs. This resulted in further increase in the already costly assembly process. The continuing increase in I/O count had a significant impact on the entire semiconductor industry. Cost remained a major factor with semiconductor manufacturers and needed to be addressed in order to remain competitive in a rapidly maturing industry and more importantly an expanding marketplace. Labor cost became paramount and semiconductor manufacturers looked for and found the answer "offshore", outside the continental United States in the Far East, notably Japan, where labor rates were orders of magnitude lower. As a result, the major semiconductor manufacturers quickly moved their assembly operations offshore.

Concurrently, equipment manufacturers were seeking ways to reduce the labor content in assembly. This effort resulted in the development of the computer controlled automatic wire bonder. While automatic bonders significantly reduced both the cost and the level of skill required of the operator it still could not halt the move "offshore" with the lower labor rates. The automatic bonders were simply shipped "offshore" to replace the manual bonders.

However, the development of the automatic wire bonder was a major contributor to lower cost assembly while at the same time providing an enhanced reliability by minimizing operator dependence. Interestingly, the automatic wire bonding owes its extraordinary performance capability to an IC, the microprocessor. Conversely, the automatic wire bonder has been a critical part of the assembly infrastructure and an "enabler" fully supporting new generations of ICs of ever increasing complexity and functionality, with increasing I/O count and shrinking pad size and pitch.

8.3 — The Chip and Wire Assembly Process [3]

Figure 8-3 shows an assembly process flow that is typical for current plastic encapsulated ICs (also referred to as Plastic Encapsulated Microcircuits, or PEMs).

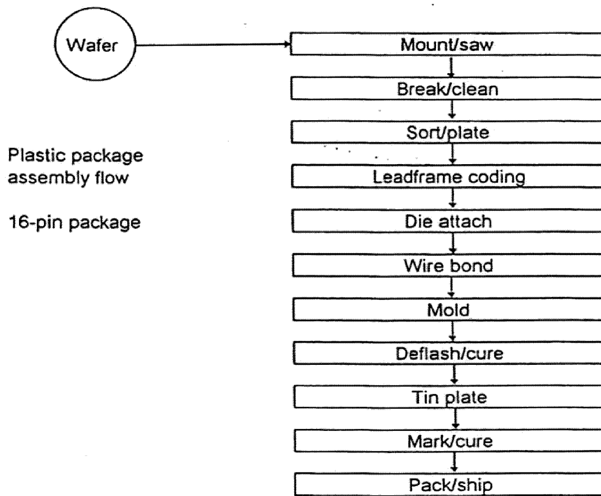


Figure 8-3. IC Assembly Process for PEMs

In die bonding the Si transistor, where a connection was needed to the backside of the die, an alloy or eutectic process was used for electrical and mechanical connection to the package. With the IC, however, all connections are brought out on the top surface of the IC and an organic adhesive can be used for the die attach and wire bonding for all necessary electrical connection. Eutectic bonding however is used whenever high conductivity electrical or thermal requirements need to be addressed. For ICs, this represents a very small percentage (<<1%) of all ICs produced. Table 8-1 compares the advantages and disadvantages of Eutectic Bonding vs. Adhesive Die Bonding.

8.4 — Bonding Wire: Au, Al, and Cu [4]

Au, Al and Cu are all used for wire bonding ICs. The overwhelming majority of ICs are Au wire ball bonding. The material properties for each are shown in Table 8-2.

8.4.1 — Aluminum (Al) Wire

Al wire, in the past, was used almost exclusively wherever the device's operation and environment involved excessive power or temperature cycling. Al wire is typically used for bonding power transistors and power hybrids as seen in Figure 8-4. More recently, the move to organic packages for SCP and substrates for COB and MCM-L applications has resulted in an increase in use of room temperature ultrasonic Al bonding.

8.4.2 — Copper (Cu) Wire [5]

Cu wire has always been of particular interest and was promoted early on as a possible replacement for Au, based solely on potential cost savings. In light of

today's ICs however there is more to be considered then just the cost factor. From a materials point of view it has much to offer compared to both Au and Al.

Table 8-1. Eutectic vs. Adhesive Bonding [1]

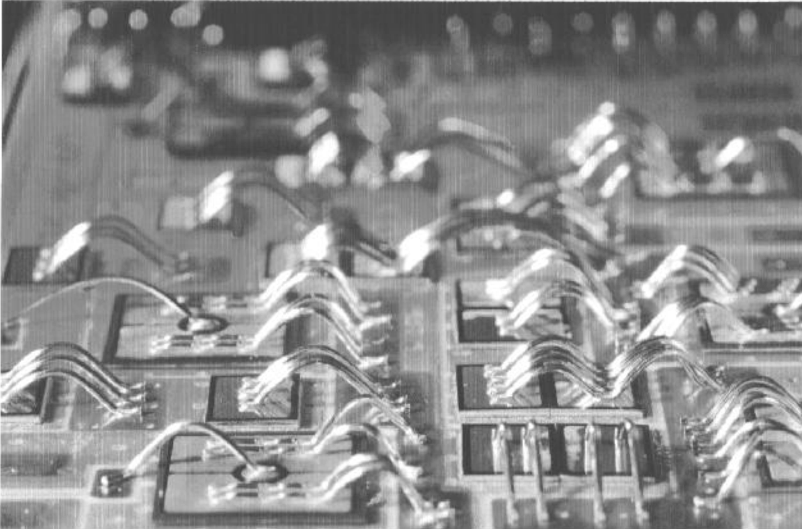
Eutectic/Alloy	Organic/Adhesive
▪ Higher electric conductivity	▪ Electrical conductive or insulating
▪ Higher thermal conductivity	▪ Lower thermal conductivity
▪ High material cost	▪ Low material cost
▪ High temperature process (>220º C)	▪ Low temperature process (<150º C)
▪ No volatiles/No "bleed out"	▪ Outgassing contaminants/Epoxy "bleed out"
▪ May require flux or special ambients	▪ No flux or special ambient
▪ Can be rigid and brittle difficult to rework	▪ Inherently flexible
▪ Some eutectics (soft solders) contain lead	▪ Easy to rework
	▪ Lead-free and environmentally friendly

Table 8-2. Material Properties of Al, Cu, and Au Wire [4]

Properties	Al	Cu	Au
Thermal Conductivity (W/m-ºK)	237	403	319
Melting point (ºC)	660	1083	1064
Electrical resistivity (Ohm-m ºC)	2.7×10^{-8}	1.7×10^{-8}	2.3×10^{-8}
Elastic modulus (Pa)	3.4×10^{10}	1.3×10^{10}	7.7×10^{10}
Yield strength (Pa)	1.0×10^{7}	6.9×10^{7}	1.7×10^{8}
Ultimate Tensile Strength (Pa)	4.5×10^{7}	2.2×10^{8}	2.1×10^{8}
Coefficient of Thermal Expansion (ppm/ ºC)	46	16	14
Percentage Elongation (%)	50	51	4

Unlike the problem with Au and Al and the formation of destructive intermetallic compound formation (IMC) there is a dramatic difference with Cu and Al. Figure 8-5 shows metallurgical cross sections of Au-Al and Cu-Al and charts the growth of IMC for both Au-Al and Cu-Al after exposure to elevated high temperatures. After exposure to a temperature of 200ºC for 200 hours the IMC formation was excessive for the Au-Al while the Cu-Al showed minimal formation after 180C for 800 hours.

In addition to reduced IMC formation Cu wire offers higher thermal and electrical conductivities, higher tensile strength and elongation and an increased "ball neck" strength. All these contribute to a more robust interconnect that is also more resistant to "wire sweep" (shorting of adjacent wires during molding), a problem encountered with Au wire and exacerbated with fine pitch bonding.



(Courtesy Orthodyne Electronics)

Figure 8-4. Al Wire Bonding on Power Hybrid

Less costly Cu wire is now being afforded more serious consideration as being more accommodating than Au to changes that have taken place with the IC such as very fine pitch I/O pad format and the change to Cu metallization on the IC itself.

There are problems however, that must be taken into consideration. Because Cu readily oxidizes at elevated temperatures the wire bonder must be modified to provide a neutral or reducing atmosphere during the critical ball forming and the actual first and second bonds. There is also a reduction in throughput.

8.5 — Bonding Methods [6]

Methods for bonding wires to connect semiconductor devices include:

- Thermocompression Bonding (TC)—requires application of elevated temperature and a mechanical force to the wire during bonding,
- Ultrasonics Bonding (US)—room temperature bonding using application of ultrasonic energy and mechanical force,
- Thermosonic Bonding (TC/US) —a combination of TC and US; requires elevated temperature (<TC), ultrasonic energy (<US) and mechanical force (<TC).

Table 8-3(a), (b), and (c) lists the advantages and disadvantages of TC, US and TC/US bonding methods.

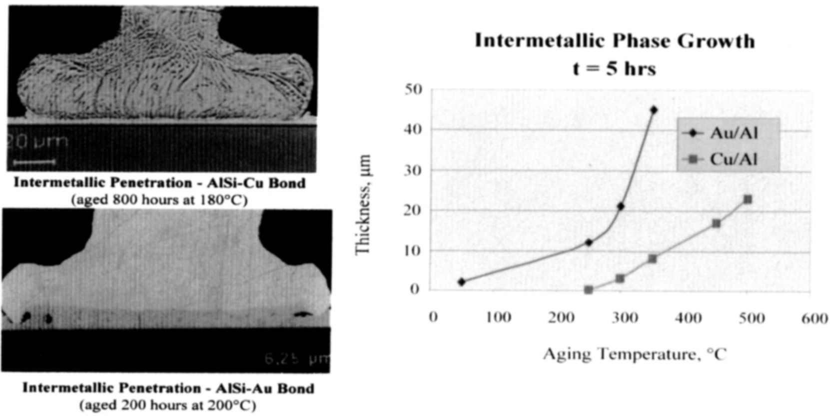


Figure 8-5. Metallurgical Cross Sections of Au and Cu Ball Bonds on Al with Data on Growth Rates at Elevated Temperatures [5]

Table 8-3(a). Advantages/Disadvantages of Thermocompression Bonding [1]

Advantages	Disadvantages
▪ Excellent reliability with Au wire to Au pads ▪ Simple 2+parameter machine setup ▪ Omni-directional bonding with ball bonding ▪ Negligible damage to die ("cratering")	▪ High temperature process >300 C ▪ Very susceptible to contamination ▪ Wedge bonding unidirectional; throughput <TC/US ▪ Susceptible to formation of intermetallics with Au wire and Al pads—"Purple Plague"

Table 8-3(b). Advantages/Disadvantages of Ultrasonic Bonding [1]

Advantages	Disadvantages
▪ Least susceptible to contaminants ▪ Bonds formed at room temperature ▪ Capable of very fine pitch ▪ Excellent reliability—Al wire to Al bond pads ▪ Capable of bonding very large diameter wire, >> 2 mils ▪ Inherent low loop	▪ Uni-axial bonding only; slower than ball bonding ▪ Source of damage to die (cratering) ▪ 3 parameter machine setup ▪ More difficult to automate vs. TC/US

Table 8-3(c). Advantages/Disadvantages of Thermosonic Bonding [1]

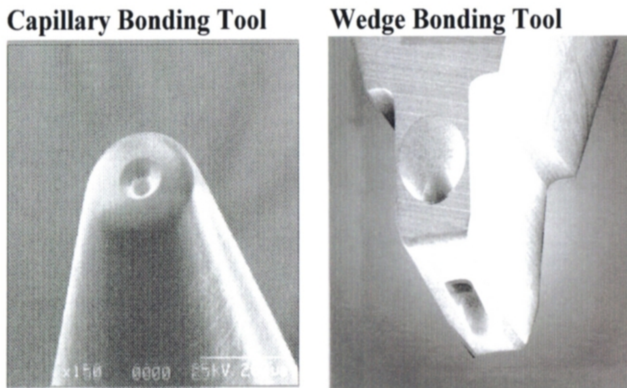
Advantages	Disadvantages
▪ Lower temperature (100–150 C) vs. TC (>300 C) ▪ Reduced U/S energy required vs. room temperature U/S ▪ Lower occurrence of cratering vs. U/S ▪ Omni-directional bonding therefore highest throughput ▪ Readily automated	▪ 4 parameter machine setup ▪ Susceptible to contaminants, > U/S, <TC

8.6 — Types of Bonds [7–10]

The type of bonds formed is determined by the bonding tool, which is either a capillary or wedge (Figure 8-6).

The capillary produces a ball bond (first bond) on the die and a crescent bond (second bond) on the package. The wedge tool, in turn, creates a wedge bond on both the first and second bonds.

A SEM of a Au ball bond and an Al wedge bond are shown in Figure 8-7. Note that the ball bond is much larger than the original wire while the wedge bond is only slightly larger in width than the original wire.



(Courtesy Gaiser Tool)

Figure 8-6. Bonding Tools—Capillary and Wedge Bonding Tools

8.7 — The Ball Bonding Process

Ball bonding uses either thernocompression or thermosonic process and Au or Cu wire. Thermosonic Au ball bonding has emerged as the most dominant wire bonding

method in high volume production. It is more readily automated because it features omni-directional capillary travel and therefore higher throughput and a lower cost bonding process in high volume production. Using automatic ball bonders 14 wires per second are possible. The ball bonding process sequence is illustrated in Figure 8-8.

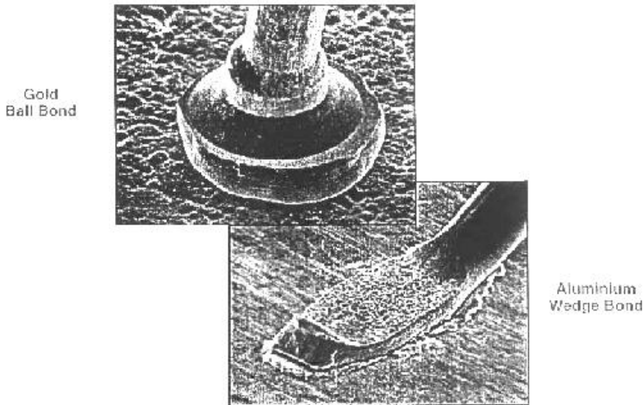


Figure 8-7. SEM Au Ball Bond and Al Wedge Bond

8.8 — Wedge Bonding

Wedge bonds are formed primarily with Al wire and ultrasonic bonding. Wedge bonding inherently offers several advantages when compared to ball bonding, including a low loop wire profile and finer pad pitch capability. The low loop feature has made it attractive for applications such as PC cards, Smart Cards and thin small outline packages (TSOPs).

The wedge bonding process sequence for both thermosonic and ultrasonic is illustrated in Figure 8-9. Note that to bond the wire, the bond tool and wire travel is always inline requiring a rotation of either the bonding tool assembly or the substrate for each wire. This unidirectional motion increases the bonding cycle time and reduces throughput.

As noted in Table 8-3(b) use of ultrasonics has been identified as the primary source of cratering or cracking of the silicon directly under the Al bonding pad. Thus, for GaAs devices, which are notably more brittle than Si, extra care must be given to the amount of ultrasonic energy that is applied and the timing during the wire bonding process. GaAs devices for this reason, are often bonded using thermocompression rather than thermosoniscs. The latest automatic thermosonic bonders, with increased programming capability, are now able to minimize cratering as a problem as previously experienced.

8.9 — Obstacles to Quality and Reliable Wire Bonding [1,3,11]

There are many obstacles that need to be addressed and controlled in order to put into operation a quality wire bonding process. Providing for clean surfaces for either die bonding or wire bonding is of paramount importance.

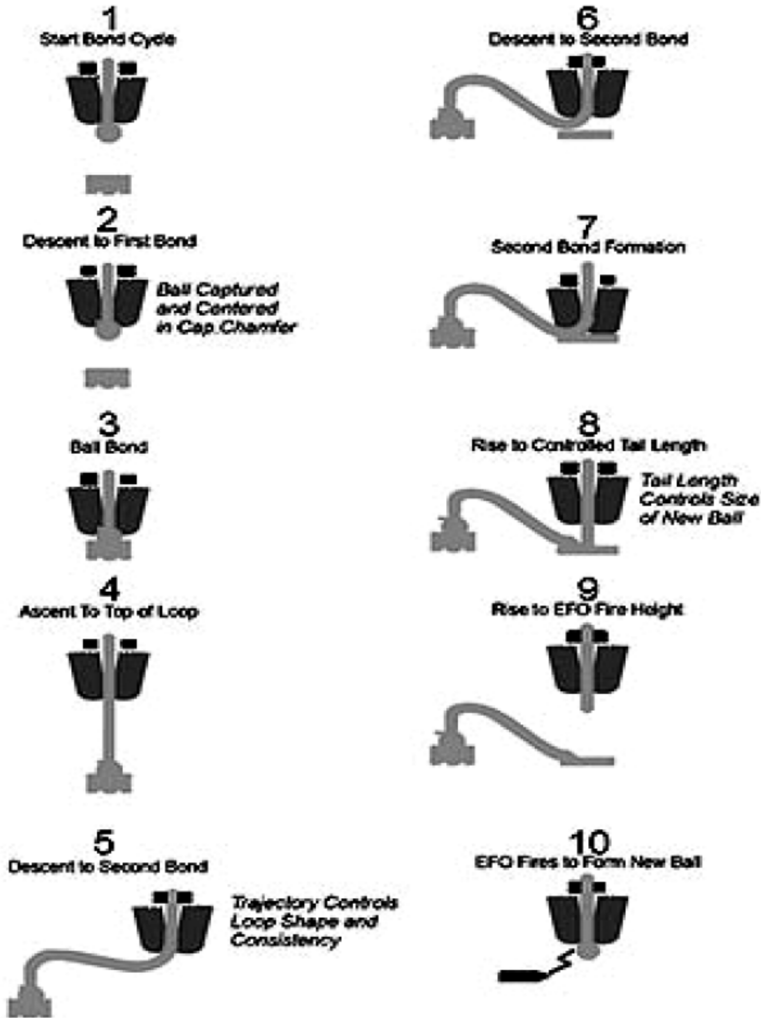


Figure 8-8. The Ball Bonding Process [7]

Regardless of the methods used to die bond and wire bond a bare die to a package, it is essential that all bonding surfaces be clean, i.e., free of any contaminants, that would prevent or inhibit successful and reliable attachment/ bonding of the parts.

It is equally important that when parts have been cleaned, special precautions must be in place to prevent recontamination from occurring. This becomes more critical when there is a significant time differential or additional processing takes place between the cleaning and the actual bonding step.

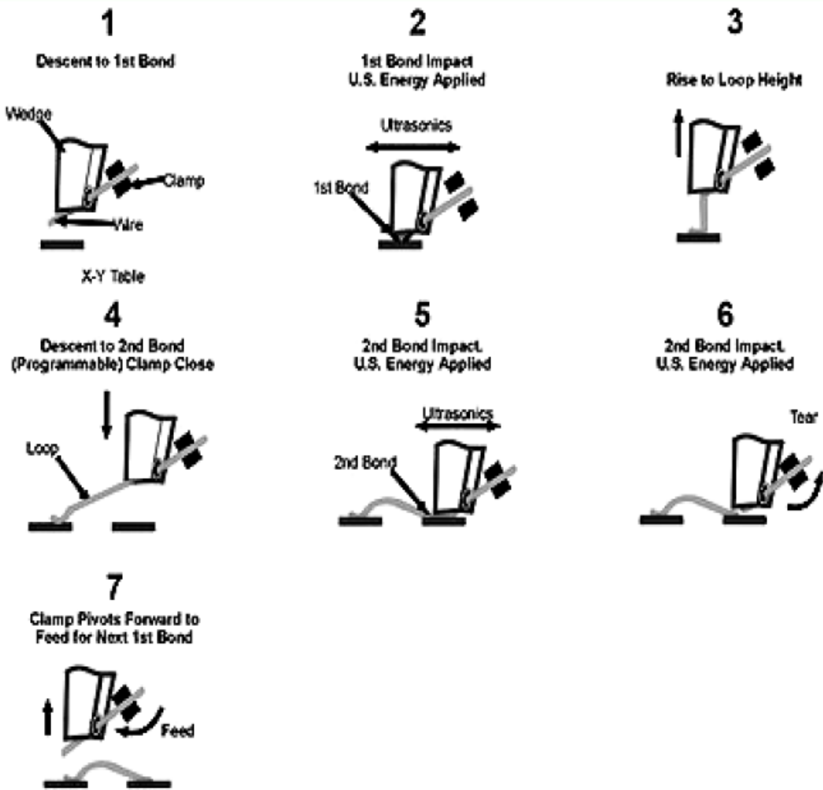


Figure 8-9. The Wedge Bonding Process [8]

Cleaning processes include both wet chemical and dry processes.

Dry processes include plasma cleaning, UV/ozone cleaning, and high vacuum, high temperature baking.

Mechanical abrading or burnishing of the metal traces, in particular thick film metallization has also been used to improve the surface for wire bonding.

The particular cleaning process employed is generally dictated by the parts to be cleaned and the contaminants involved.

The most widely used and current industry standard for cleaning parts for wire bond assembly is plasma cleaning [12]. A dry process, it has been shown to be highly effective in improving the quality and reliability of wire bonds. Typically it follows die attach, preferably immediately prior to the actual wire bonding process.

There are many different kinds of equipment available for doing plasma cleaning. Designs vary. The process parameters for the most part are those

recommended by the manufacturer based on his experience and the type of cleaning required. It is not unusual that changes in process parameters are needed to meet particular needs. Process parameters are usually determined empirically.

Table 8-4 provides a list of various sources of contaminants that lead to poor quality and unreliable bonding.

Additionally and equally critical are the following:

- Die/substrate metallization
- The bonding surface metallurgies
- Wire properties—purity, elongation, tensile strength
- Post-bonded wire—wire deformation, pull strength
- The wire bonder—setup and maintenance
- Work holder/tooling
- Substrate flatness

Table 8-5 provides a list of various sources of contaminants that lead to poor quality and unreliable bonding.

Table 8-4. Sources of Contamination that Lead to Poor Quality Bonds [1]

Contaminants	Sources
From halogens	Plasma etching (dry processing), Epoxy out-gassing, Silox etch, Photoresist stripper, Solvents (TCA, TCE, chloro-fluro's)
From plating	Thallium, Lead, Chromium, Nickel, Brighteners, Iron, Copper, Hydrogen
Sulfur from packing containers	Packing containers, Cardboard & paper, Ambient air, Rubber bands
Miscellaneous organic contaminants	Epoxy out-gassing, Photoresist, Ambient Air, Spittle
Others that cause corrosion or inhibit bonding	Sodium, Phosphorous, Moisture, Carbon, Copper, Chromium, Bismuth, Cadmium, Glass, Vapox, Nitride, Silver, Tin

8.10 — Metallurgical Concerns and Surface Finishes

A critical concern relative to the bonding surfaces is the metallurgical compatibility of contacting metals. Obviously, while there are many metals and combinations of metals involved, the metallurgies must not only be compatible but bondable. One must be concerned with not just successfully bonding a wire to either the die or package but also with the quality and long-term reliability of the bond so formed. Many stresses can be experienced during the operational life cycle of the IC. These stresses can involve power and temperature cycling that can result in degradation of the bonds, resulting from interdiffusion of the metals and the formation of IMC as previously discussed. Table 8-4 is list of metal combinations and their reliability rankings.

Table 8-5. Metallurgical Compatibility of Wire bonding Materials [1]

Reliability		
High ↑	**Au–Au**	
	Al–Al	
	Au–Ag	Reliability established by high volume production
	Al–Ni	
Low ↓	**Au–Au**	
High ↑	**Au–Cu**	Reliability established by laboratory experiments or low volume production only. Acceptable for commercial production. Copper wire bonds may crater Si
	Ag–Cu	
Low ↓	**Al–Cu**	
Very Low ↓	**Al–Ag**	Use only with great caution

8.10.1 — Surface Conditions

In addition to the metallurgical compatibility of the bonding metal there are also many surface conditions that adversely affect the quality of the bonds and ultimately the long-term reliability. The surfaces of most concern are the die bond pads and the package/substrate pads.

Surface conditions to be addressed include surface roughness and the hardness of metal film. Both can hinder attaining consistently good, reliable bonding. Ideally, bondable metals should be "soft" and present a smooth surface free of imperfections such as blisters and voids. In general, the "harder" the metal and the rougher the surface the more difficult it is to achieve repeatably good quality and reliable bonds.

Surface roughness and hardness are for the most part, a product of the materials and particular process employed in depositing the metal films. Deposition processes cover the full spectrum of thick and thin film as well as wet chemical processes, electrolytic and electroless plating. Each contributes in somewhat different ways.

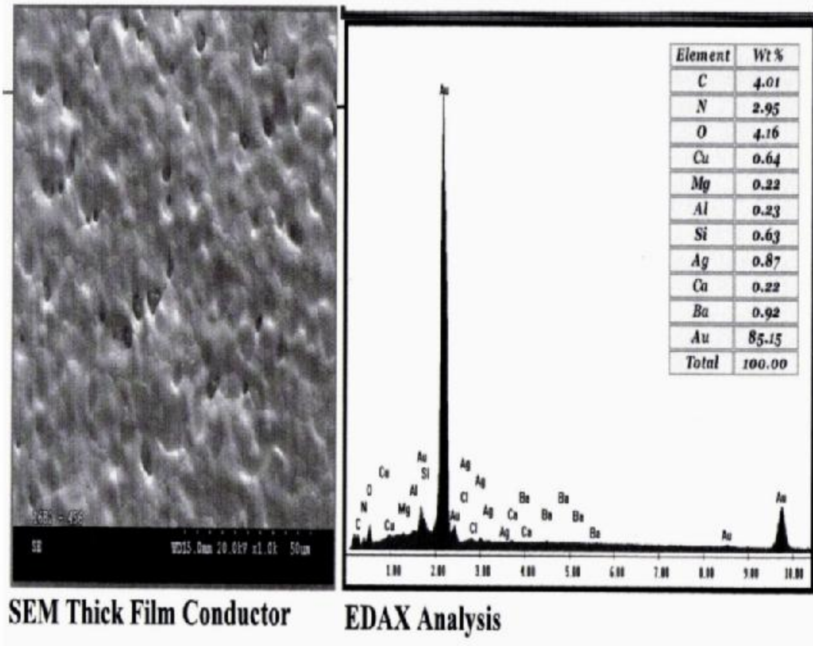
8.10.2 — Thick Film Deposits

Good quality and reliable wire bonding to screen printed thick film conductors is very much dependent upon the overall composition of the film. The metal particles, both their size and type, affect the bondability. Finer grain size provides for a smoother surface finish and better bonding. Figure 8-10 shows a SEM of a thick film conductor after firing. The surface roughness as well as porosities in the film is clearly evident.

The same figure presents the results of electron dispersive spectrographic analysis (EDS) of the film composition that identifies the elements contained in the film. This type of analysis is invaluable as a process control or in failure analysis since it can provide evidence of impurities that can hinder bonding. Glass, for example, is used in most thick films to enhance film adhesion to the substrate, and has been identified as a source for poor bondability and a concern for long-term reliability.

The screen printing process for patterning the thick film can also contribute to surface roughness. Figure 8-11 shows wire bonds on a screen printed thick film. The film clearly shows replication of the screen's mesh producing surface roughness.

Reliable bonds to thick film are achievable, however, the entire wire bonding process must be tailored accordingly and requires significantly more monitoring using in-process controls.



Element	Wt%
C	4.01
N	2.95
O	4.16
Cu	0.64
Mg	0.22
Al	0.23
Si	0.63
Ag	0.87
Ca	0.22
Ba	0.92
Au	85.15
Total	100.00

Figure 8-10. SEM—Thick Film and EDAX Analysis

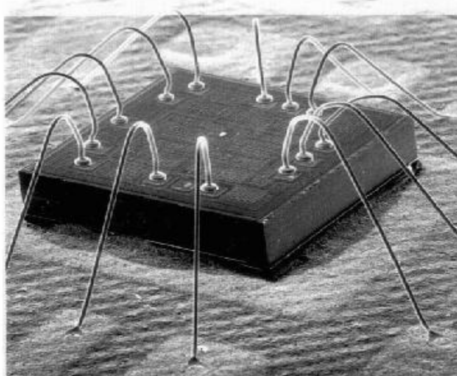


Figure 8-11. Wire Bonding on Screen Printed Thick Film

8.10.3 — Plated Deposits

Electroplating Au or Ag is the most widely used method for depositing wire bondable films on lead frames, packages and substrates. The quality of the deposited film, i.e., bondability, is affected by several factors inherent in the plating process such as the chemical make-up of the bath, the plating conditions (DC, periodic reverse, or pulse), bath temperature and current density. Each contribute to the quality of the plated film. Film properties that can be affected are film density and imperfections (voids and blisters), the hardness, grain size and surface roughness.

A critical factor in realizing good film bondability is to control the hardness of the deposit. The hardness of the film is obviously determined by the chemical make-up (purity) of the plating bath and further influenced by the plating mode and process parameters (i.e. the current density).

In general, the rule of thumb is, the purer the bath the softer the deposit, and the finer the grain size the better the bondability.

For Au films, providing a high purity plating bath typically entails starting with 99.99% purity and maintaining that level by performing routine bath analysis looking for presence of known elements that contribute to film hardness such as nickel, carbon chromium, and thallium.

In addition, the actual hardness of the plating films can be quantitatively checked and used as an in-process control. Such in-process monitoring can be an extremely effective tool that eliminates suspect films from getting into the assembly operation. It is also an additional check on possible plating problems.

High temperature heat treatment of plated films is effective in determining the quality of plated films. Plated parts are typically heat treated at an elevated temperature (typically 350ºC) to routinely check for blistering and for checking hardness of bondable films. Blistering results in voids in films and can adversely affect acceptable bondability.

The hardness of the deposited films immediately following plating and after a heat treatment is an effective indicator of potential plating bath contamination problems. Plated Au films, for example, are typically highly stressed, with a Knoop microhardness of roughly 80–90. Following the heat treatment, which is intended to anneal the film, the hardness should be expected to drop to roughly 40–50 Knoop, an indication of a “soft” deposit. If the initial hardness is >100 or if there is no change in the post anneal reading, the plated film and the bath becomes suspect. The heat treatment can be used as a qualitative indicator of film purity. Any change in the appearance of the gold, e.g. darkening, following annealing is a further indication of a potential plating bath problem.

8.10.4 — Thin Film Deposits

IC bond pad metallization is thin film Al or Al-1% Si and is deposited by sputtering. The Al is fine grained, presenting a smooth surface for bonding. In practice, a smoother surface supports better, more reliable, repeatable quality bonding. Thin films deposited by sputtering are readily controlled for purity since the film is typically the same chemical composition as the source target.

8.11 — Handling and Storage

Films can be readily verified as bondable by wire bonding an appropriate size sample of both die and packages before they are sent into production. The verification should be part of incoming inspection. Bondable films can however, be easily rendered non-bondable as a result of surface contaminants encountered in either the pre-wire assembly processing (e.g. die attach) or in improper handling and storage. Halogens, for example, are contaminants that hinder successful bonding. Halogens can be deposited on the die pads after die bonding from the epoxy die adhesive bleed out or from an earlier faulty photoresist stripping process. Somewhat ironically, cleaning processes, including wet chemical solvent cleanings or a plasma cleaning, can in fact also be a source of contamination. Both die and packages need to be properly stored, preferably in nitrogen filled cabinets that minimize formation of oxide films on the Al bond pads. Care is needed regarding packaging containers and papers that might contain sulfur and come in contact with parts during shipping or storage.

8.12 — Verifying Wire Bonding Quality

Available test procedures for establishing and maintaining good quality and reliable wire bonding include wire pull testing (destructive and non-destructive) and bond or ball shear testing. These are illustrated in Figure 8-12. Ball shear testing is always destructive while pull testing can be destructive or non-destructive.

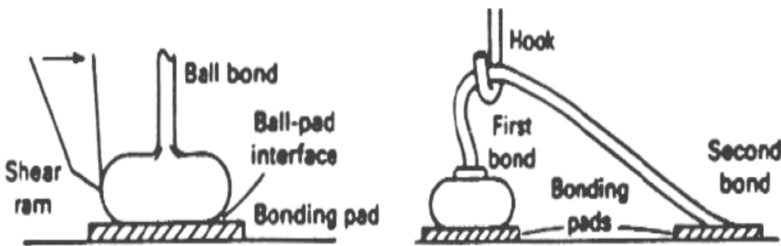


Figure 8-12. Schematic Ball Shear (left) and Wire Pull Testing (right) [1]

The destructive wire pull and the ball or bond shear testing are used extensively for:

- Incoming inspections to verify bondability of both die and packages/substrates
- Establishing wire bonder operating parameters (bonder setup)
- Verifying wire bonder operation (in-process control)

Characteristically, with both test methods, the metric for establishing an acceptable level of quality is the gram-force required to create a break in a wire or a separation at a bond interface. Special pull test equipment is available that is manually operated or completely automatic. The latter records and prints out the

gram-force at destruct, the average of the samples, and the 3-sigma values. The pass/fail criteria for the wire pull testing are shown in Table 8-6 (a) and (b) for both Au and Al wire respectively. It is established based on the particular wire properties, including wire diameter and tensile strength.

Table 8-6(a). Au Wire Destructive Pull Test Criteria [Ref. Mil Std 883]

Au Wire Size (Inches)	Destruct Force (Grams)	Non-destruct (Grams)	Post 300 C (Grams)
0.0008	2.4	1.6–2.2	0.5
0.001	3.0	2.1–2.7	1.0
0.0012	3.7	2.7–3.3	1.8
0.0015	5.0	3.7–4.3	3.0
0.002	7.5	5.7–6.3	4.6

Table 8-6(b). Al Wire Destructive Pull Test Criteria [Ref. Mil Std 883]

Au Wire Size (Inches)	Destruct Force (Grams)	Non-destruct (Grams)	Post 300 C (Grams)
0.001	2.3	1.7–2.3	1.0
0.005	28	21.3–23.5	19.8
0.010	100	76–84	72

The Post 300ºC values refer to pull test results following heat treatment of wire bonds at 300ºC for a specified period of time, typically 100 hours. It is used to assess the long-term reliability of the wire bonding. All destructive testing is done on samples or coupons. Non-destructive testing however is performed as an in-process control on regular product. It involves non-destructive pull testing of 100% of the wires on a finished assembly. Wires are pulled at a gram-force that is less than the average pull force experienced on destructive tests. It can in some instances be very effective in helping to develop a database that monitors the percent defective (failures per million, ppm) for the process. This in turn, serves as an effective indicator of overall process performance. 100% non-destructive wire pull testing can be very time-consuming and therefore costly. It does however provide confirmation that all wires on an assembly have been properly bonded and that no minimal bonded wires are present. It is a requirement that is often called out on high reliability programs for military and space applications.

In addition to the pass/fail criteria, point of failure and failure mode will normally be included in the pull test results to provide a more complete assessment of the overall wire bonding process. Failures at interfaces, that is bond lifts at the die bond pad or on the package are obviously a concern even if the gram-force is acceptable. Bond lifts will often results in a second sample to be run. Bond lifts are usually a sign of surface contamination. Similarly, a significant change in the

dominant failure mode, for example, wire breaks at mid-span to wire breaks at the heel of the second bond, might well indicate a problem with the capillary or wedge tool. Figure 8-13 identifies the types of failure that can be encountered with ball and wedge bonding. Bond shear is used less than the wire pull testing. It is however effective in process development, establishing machine bonding parameters and also for evaluating bondability of packages and substrates.

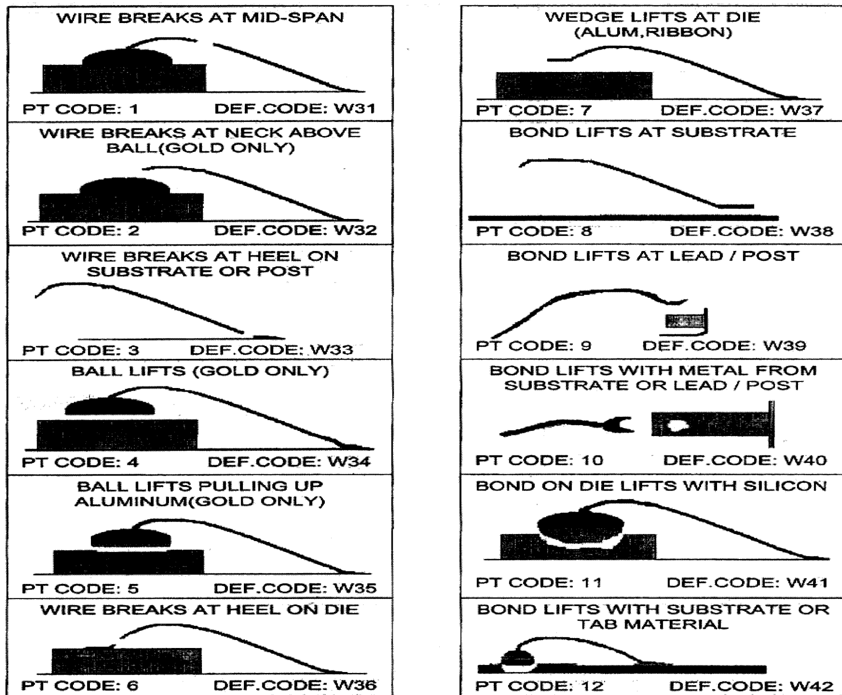


Figure 8-13. Wire Bonding Failure Modes/Sites [Ref. Mil Std 883]

8.13 — Responding to the IC and End Product [13,14]

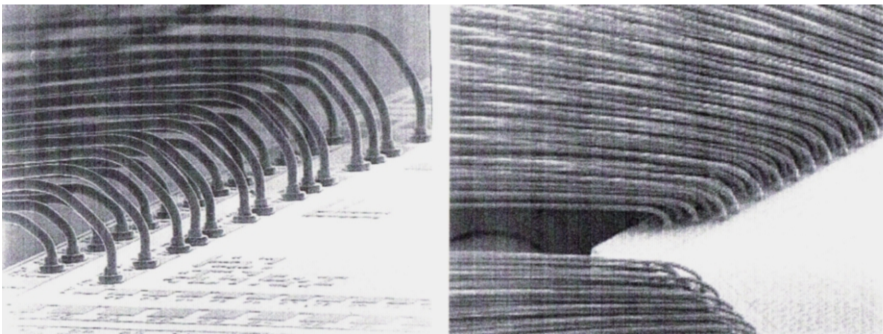
The IC and end product are continually undergoing changes. These changes have and will continue in the future to present challenges to the wire bonding processes. For the IC it comes from the ever-increasing I/O count and for the end product it is the challenge of providing increasing functionality in the smallest possible package. In the latter case for example, it takes in the very difficult job of wire bonding multiple die stacked in a CSP. The automatic wire bonder has been the key enabler in addressing these challenges.

Wire bonding is a heavily entrenched technology within the semiconductor industry with an established infrastructure. While flip chip has total compatibility with the IC and the I/O count, it is essential wire bonding survive the threat from flip chip as the dominant first level interconnect.

Accommodating increasing I/Os has necessitated changes in design of the IC chip, in particular the wire bonding pad configuration. The problem is simply—how does one increase the number of bond pads on a chip without increasing the size of the die?

Wire bond pad layout has always been confined totally to the perimeter of the die and remains an absolute prerequisite. The initial thrust therefore, was directed towards reducing the size and pitch of the bond pads. The industry standard with regard to bond pad design rules, and most commonly used has been 100µm square pad and 200µm pitch. These gave way to 50µm pads on 100µm pitch that immediately resulted in a doubling of the number of pads. And this occurred with no change in die size. Additional increase in I/O pad capability could obviously be realized by continuing to further reduce pad size and pitch. Out of necessity the industry has seen pitch go to 70µm and 45µm and is currently at a 35µm pitch. Figure 8-14 shows SEMs of "standard" 200 µm pad pitch and 35 µm pitch.

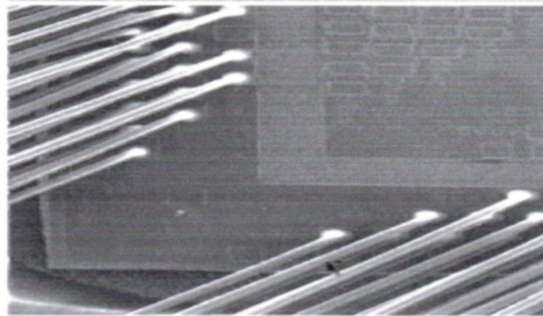
An alternate approach to increased I/O capability that affected the size of the die was to go to multiple rows of pads. With the adjacent rows staggered the "effective" pitch is roughly doubled with 2 rows and tripled with 3 staggered rows. An advantage is that the increased pad capacity is obtained without reducing the pad size or pitch. For example, if it were important to retain a 100µm pad size 2 staggered rows would again roughly double the number of available pads of the same 100µm size. Figure 8-14(a) is SEMs showing wire bonding using 2 and 3 staggered rows.



(Courtesy Kulicke & Soffa)

Figure 8-14(a). Two and Three Staggered Row I/O Pad Configurations

The staggered rows increase the number of pads that can be accommodated but it is at the expense of valuable Si real estate. This impacts the die size, which in turn means less die are available per wafer resulting in a higher chip cost. The extra real estate required is clearly evident from Figure 8-14(b).



(Courtesy Kulicke & Soffa)

Figure 8-14(b). 3 Staggered Rows of Bond Pads

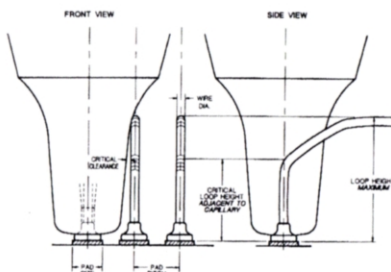
8.13.1 — Impact of Fine Pitch on Wire Bonding [15]

Fine pitch wire bonding featuring smaller pad size and pitch presented problems that impacted the bonding tools, both capillary and wedge, and the wire and the package.

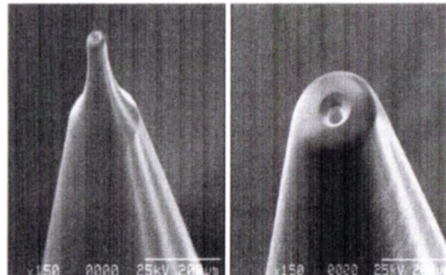
The tools had to be reduced in size in order allow for tool clearance to the bond pad without damaging the previously bonded wire. Figure 8-15 illustrates the "problem" and shows both the standard and redesigned capillary tools.

The tip of the redesigned tool base is now referred to as a "bottleneck" and is critical to accomplishing fine pitch bonding.

A similar change in design of the wedge bonding tool was also necessary.



Fine Pitch Wire Bonding Capillary Redesign



"Bottleneck" Capillary for Fine Pitch and Standard Capillary

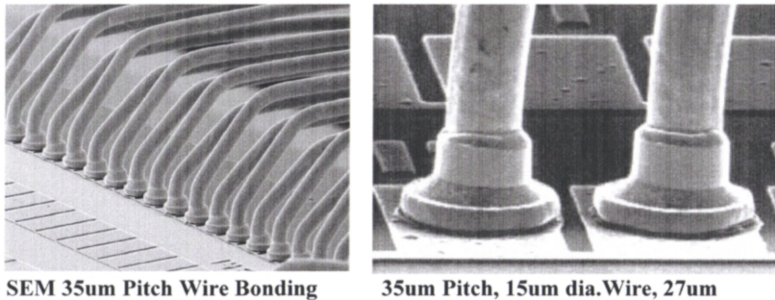
(Courtesy Gaiser Tool)

Figure 8-15. Capillary Re-Design for Fine Pitch Applications

8.13.2 — Impact of Fine Pitch on the Bonding Wire

With reduction in pitch from 200 to 100 to 45, and finally 35ums, the pad sizes have also been reduced in size. For example, with 35µm pitch the pad size is 25µm x 25µm. For ball bonding, this obviates the use of the 25µm diameter wire that

typically has a ball size of roughly three times that of the wire. As a consequence, the wire diameter and the ball diameter must be reduced. Figure 8-16 is SEMs of 35μm pitch ball bonding, showing a wire diameter of 15μm and a ball size of 27μm. Note the ball diameter is now roughly twice the wire diameter.



(Courtesy Kulicke & Soffa)

Figure 8-16. Fine Pitch Ball Bonding

8.13.3 — Impact of Fine Pitch on the Package and the Bonder [16,17]

Accommodating very high I/Os at the package level introduces additional problems mostly associated with fan-out and the layout of the I/O pads on the package. The package layout design takes into consideration both the wire bonding, in particular, producibility concerns and the package manufacturability. The PBGA, for example, is not capable of providing bond pads on the same fine pitch as the die and as a consequence, a fan-out of package pads is the only viable alternative. The pads are a much larger size and at much greater pitch.

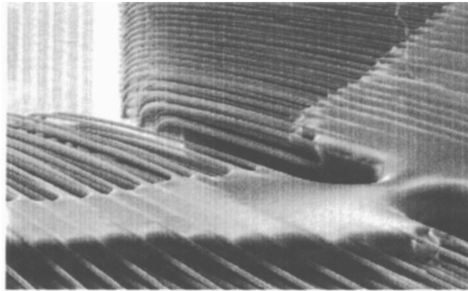
A typical wire bonded PBGA designed specifically for fine pitch and high I/O count is shown in Figure 8-17. The design results in very long wire loops.

(Courtesy Kulicke & Soffa)

Figure 8-17. PBGA Showing Fan Out of Package Pads and Long Loop Wire Bonds

The combination of fine pitch, staggered rows and the package requires added control and performance on the wire bonder. For example, finer pitch entails greater placement accuracy of the first bond. At 35μm pitch, a 27μm ball must be placed on a 30μm pad.

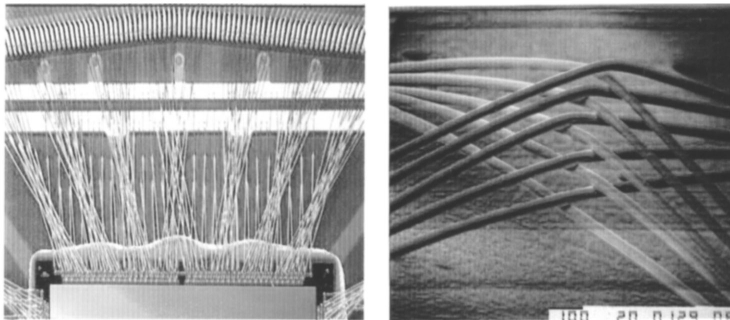
Additionally, the increased number of wires, longer loops and close spacing became a concern at the transfer molding process and the occurrence of wire sweep. Wire sweep refers to the shorting of adjacent wires that results from the physical flow of encapsulant during molding. With the finer pitch and the longer loops, rejects from sweep increase significantly. One solution to this problem is to coat the wires immediately after bonding with an epoxy that effectively locks the wires in place. An example of this is shown in Figure 8-18.



(Courtesy Kulicke & Spoffa)

Figure 8-18. No Sweep Encapsulant

Recently, Microbonds, Inc. introduced a proprietary insulated Au wire to further address very high-density fine pitch bonding applications. The wire is totally compatible for use with current wire ball bonders. Wires can be in physical contact with each other without causing electrical shorts. Insulated wire effectively eliminates problems associated with wire sweep. Figure 8-19 illustrates the wiring density achievable and a close-up SEM of wires crossing each other.



(Courtesy Microbonds Inc.)

Figure 8-19. High Density Fine Pitch Wire Bonding with Insulated Wires

Innovative packaging has also presented added challenges requiring a response. The demand for package miniaturization starting with TSOP and the CSP as well as niche applications including smart cards and PC cards, mandated changes in the classic wire loop profile. All called for a significant lower loop height. This low loop profile was also essential for the CSP, which had the added requirement for the second bond to be placed close to the edge of the die. And finally, there is the challenge of die stacking that necessitated changes in the first ball bond, "customized" loop profiles and both forward and reverse wire bonding to complete an assembly. Figure 8-20 shows examples of the low loop the CSP loop and the forced forward ball bond.

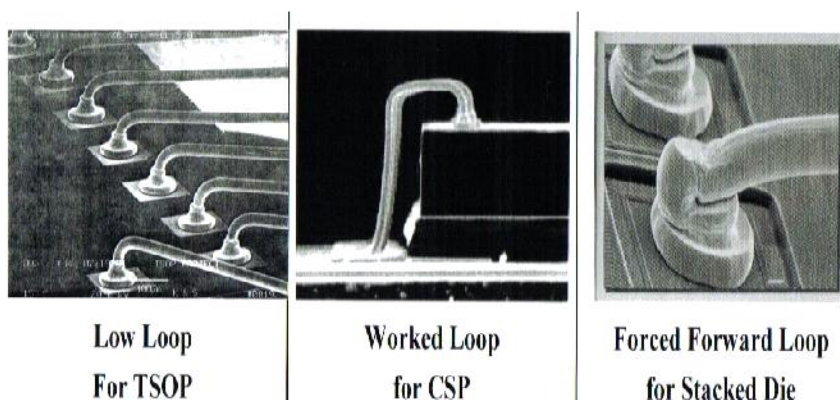


Figure 8-20. Wire Bonding Responding to Changing Packaging Technologies

8.14 — Wire Bonding on Organic Substrates, The PBGA and PWB

Organic packages and substrates present some unique problems that need to be addressed for successful wire bonding. Compared to inorganic packages, specifically ceramic, the organic package is limited to lower process temperatures and lacks the same structural rigidity.

Manufactured employing the laminate technology, the metallization is Cu cladding that for the most part is plated with Ni and Au, either electrolytic or Electroless Nickel Immersion Gold (ENIG) to accommodate wire bonding. The ENIG is used as the surface finish on most PBGAs. Nickel thickness of 150–200 microinches and 8–10 microinches for the Au has been found satisfactory for ultrasonic Al wire bonding while 20–40 microinches Au is better suited for thermosonic Au ball bonding.

In the Ni-Au system the nickel functions as a diffusion barrier preventing Cu from diffusing through and into the Au and subsequently degrading the wire bond. The Au acts as a passivation barrier protecting the underlying nickel from oxidizing. With ultrasonic Al, the amount of Au needed is minimal since the Al wire bond actually occurs at the nickel interface and oxidation of the Ni is less of a concern with ultrasonic bonding. Thicker Au is required however, for thermosonic Au since the bond is between the Au wire and the Au layer.

ENIG has many advantages not the least of which is that it does not require a plating buss as is the case with electrolytic Ni-Au. The buss complicates the design and uses excessive board real estate. ENIG requires no buss and can be deposited selectively using solder masking. Thus, the Ni-Au can be deposited only where needed—on the contact pads on the board.

ENIG however, is not without problems. The plating process is costly and not environmentally friendly necessitating hazardous waste measures to be in place. Highly reliable PBGAs for SCPs are being produced with ENIG.

There are issues however, for MCMs and COB applications. Problems arise due for the most part, on exposure to elevated temperatures for extended periods of time that occurs when multiple die are to be Au ball bonded. The added time of exposure can result in diffusion of the Ni through the Au and oxidation of the Ni at the surface inhibiting the wire bonding. The more die to be bonded, the longer the exposure to elevated temperature. For COB the situation is acerbated since the PWB also sees elevated temperature during the SMT solder reflow that precedes the chip & wire assembly. This same problem can also manifest itself in poor solder joints on reflowed surface mount components. The solution depends upon strict controls on the Ni, its composition (in particular the phosphorous content) and the Au thickness. A thin but dense Au layer can be a much more effective barrier and a protective layer for the Ni.

8.14.1 — Insuring Wire Bondable Organic Substrates

Because of the temperature limitation associated with organic substrates many of the incoming and in-process inspections, controls and monitoring that take place with lead frames and ceramic packages cannot be implemented. Any sort of heat treatment, for example heat treating at 350ºC to properly anneal electroplated plated Au, is prohibitive. This creates a burden on verification and assessment of the bondability of incoming organic boards.

This same limitation forces the temperature for thermosonic bonding of Au wire to be lowered from 140ºC–170ºC to 100ºC–120ºC. The reduction in bonding temperature forces both the pressure and ultrasonic energy to be increased to compensate. As a consequence, the wire bonding process “window” is appreciably reduced.

8.14.2 — “Soft” Substrates

There are a variety of organic substrates exhibiting various degrees of rigidity. FR-4 and polyimide boards are the most commonly found in manufacturing today but do not present nearly the amount of problems that are encountered with PTFE boards. The PTFEs are referred to as “soft” substrates and are used for high frequency applications RF, microwave and millimeter wave. The softness of these substrates impact both thermosonic and ultrasonic wire bonding to the substrate bond pads. In particular, the ultrasonic energy being transmitted to the wire during bonding is absorbed within the organic layer resulting in less energy being transmitted to the wire for bonding. Increasing the ultrasonic energy or the gram-force to compensate can create other problems such as “sagging” or “cupping” of the bond pad into the dielectric, resulting in weak bonds or poor bonding yields. This is illustrated in Figure 8-21.

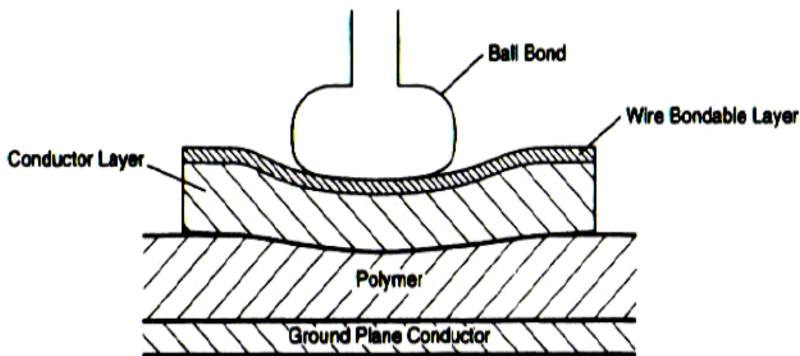


Figure 8-21. Bond Pad "Cupping" on "Soft" Substrate [1]

It obviously results in further reduction in the process window although it can be compensated for, to some degree, by using larger bond pads and thicker Ni under plate. Neither approach however, is totally acceptable for the very high frequency applications.

Successful bonding on organic substrates requires careful attention to all aspects of factors affecting wire bonding. Wire, die, and packages must be properly specified, inspected and qualified at incoming inspection. Bonders must be properly set up, maintained, and qualified through frequent in-process testing. And finally, the assembly process must be fully supported by a highly technically competent engineering staff.

8.15 — Summary

Wire bonding has been and will continue to be the principle Level 1.0 interconnect. It has extended its capability in addressing I/O counts approaching 1000. And most importantly, it is and will remain the primary interconnect for the rapidly emerging stacked die packaging technology supporting SiP and SoP.

Without argument the continuing success of this interconnect technology in support of IC packaging is due entirely to the automatic bonder. And, ironically, it owes its extraordinary performance to an IC—the microprocessor.

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9 Tape Automated Bonding—TAB

9 — BACKGROUND—MINIMOD [1,2]

An assembly technique, called MiniMod, was introduced by the General Electric Co. in the early 1970s. Like flip chip, it was initially developed to address low cost assembly of the transistor and subsequently the integrated circuit. Common to flip chip, MiniMod featured Au bumped pads and "gang" or "mass" bonding of all connections to the die and to the package in a single operation. There were, however, differences. MiniMod incorporated use of a patterned metal on an organic film or tape (a flex circuit) to accomplish the interconnection between die and package.

The tape or film (polyimide, Kapton™) with the patterned metal interconnect is fabricated in a strip format similar to movie film. With pre-punched sprocket holes to facilitate machine handling of the tape through various manufacturing operations, an automated system presented itself. This combination of automation and "gang bonding" offered the potential for significant cost savings to be realized. MiniMod eventually became Tape Automated Bonding, or simply TAB.

9.1 —Tape Automated Bonding [3,4]

Figure 9-1 is a schematic representation of a single frame TAB assembly with key features of the tape identified. It shows the IC bonded in place to cantilevered leads patterned and supported on the film. The patterned tape is in essence a "flex circuit" and represents the earliest application of flex in microelectronic packaging. In today's jargon the flex circuit is often referred to as an "interposer" and is the same basic technology used in the manufacture of the μBGA CSP.

Table 9-1 presents the key elements in a TAB assembly and the typical dimensions.

9.2 — The TAB Tape

Figure 9-2 shows a tape for an early microprocessor. It essentially features a patterned "micro-lead frame" of clad Cu supported on an organic film that is typically Kapton™ (polyimide). For attachment of the IC, the Cu is Ni and Au plated.

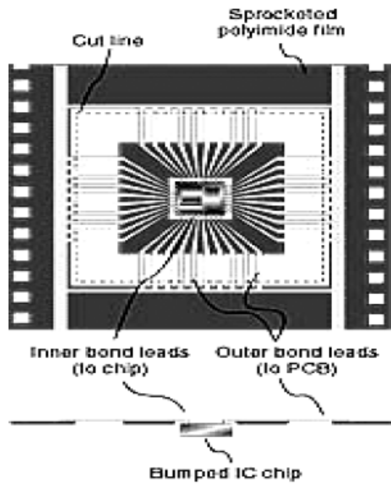
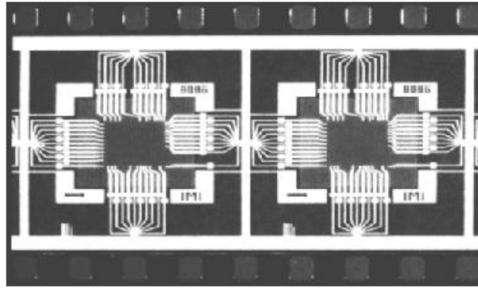


Figure 9-1. Schematic of a Single Frame TAB Assembly [1]

Table 9-1. Key Elements of a TAB Assembly [4]

TAB Element	Dimensions
Bump	
Square	15–120 µm wide; 10–30 µm high
Truncated Sphere	80–100 µm wide; 25 µm high
Interface Metallurgy	
Adhesion and Barrier Layers	0.08–1 µm
Bonding Layer	0.1–0.3 µm
Lead	
Thickness	18–70 µm
Inner lead Pitch	30–100 µm
Outer Lead Pitch	50–635 µm
Plating Thickness	0.25–2 µm
Polymeric Tape	
Width	8–70 mm
Thickness	25–125 µm
Polymeric Adhesive	12.7–25.4 µm
Die Passivation	1–2.5 µ

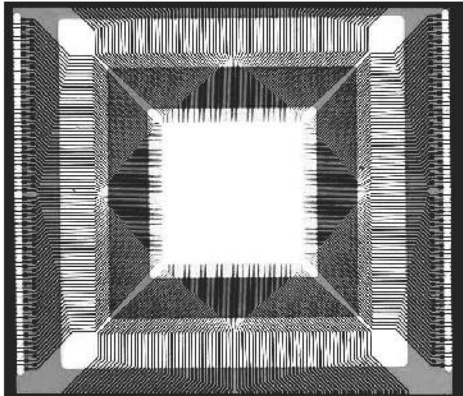


(Courtesy International Micro Industries, IMI)

Figure 9-2. Microprocessor IC TAB Tape—35mm Tape

Early tapes were 8 mm in width. However, in order to accommodate larger die and higher I/O count tapes were subsequently produced in 35 and 70 mm formats. Figure 9-3 shows an IC of considerably higher I/O count bonded to a 70 mm tape.

The strip format combined with pre-punched sprocket holes fostered ready machine-assisted handling, including a reel-to-reel input and output, for manufacture of the tape, the die assembly, and device electrical tests.



(Courtesy International Micro Industries)

Figure 9-3. Close-up of TAB Tape (70 mm) for Very High I/O Count IC

9.2.1 — TAB Tape: Types and Manufacture

There are three types of tape manufacture, one-layer, two-layer and three-layer tape. (Figure 9-4):

- The one-layer tape is basically unsupported metal foil patterned photolithographically and chemically etched.
- Two-layer tape uses a supporting polymer film for metallization that is deposited by sputtering, followed by the patterning using a selective plate up

process. The cantilevered leads in this case are plated Cu with Ni-Au over plate or all Au.

- Three layer tape uses a clad Cu foil on supporting polymer film. An adhesive is used between the foil and the polymer film. A subtractive etching process patterns the Cu.

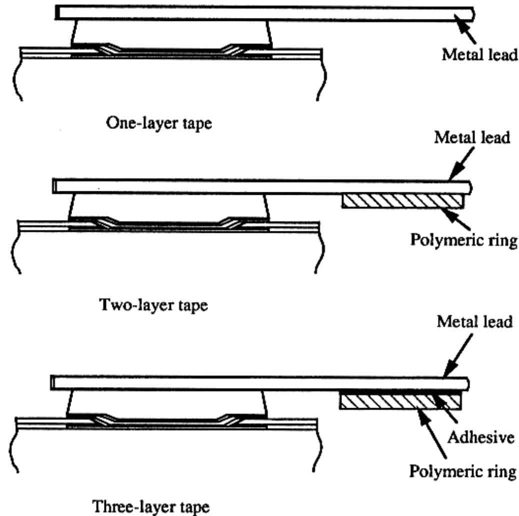


Figure 9-4. Types of TAB Tapes [4]

Table 9-2 is a comparison of the three types of TAB tapes. Note that two layer and the three-layer tape, when properly designed, allows bonded die to be electrically tested before excising. This has particular importance for MCP applications. This allows MCMs, for example, to contain many more die per package without incurring severe loss in module yields that would otherwise be experienced without pre-assembly testing.

Figure 9-5 shows a tape layout that includes an annular ring of polyimide. This annular ring permits the leads to be cut but the bonded device to be retained on the tape and the devices to be electrically tested, failures to be excised, and good devices to be maintained in the stripfilm format for subsequent processing including bonding of the outer leads to the package followed by an encapsulation.

As an option, inner lead bonded devices can also be excised from the tape and placed in carriers for electrical testing. Use of a carrier offers the additional advantage allowing the TAB assembly to be subjected to a burn-in as well. Carriers containing TAB assemblies are shown in Figure 9-6.

Table 9-2. Comparing Tape Options [6]

Attributes	One-Layer	Two-Layer	Three-Layer
Testable in tape	No	Yes	Yes
Copper	Rolled	Electro-deposited	Either
Usual gauge	2 oz.	1 oz.	1 oz.
Base film thickness	N/A	50µm	127µm
Sprocket defined in	etched Cu	etched Cu	Punched polymeric film
Lead count	Low	Medium	High
Resistance to handling damage	Poor	Good	Good
Cost	Low	Medium	High
Temperature stability	Excellent	Good	Poor
Positional accuracy	Medium	Medium	High

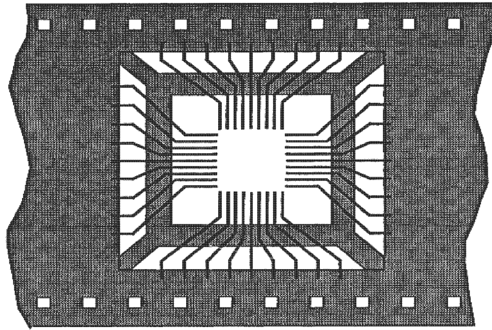
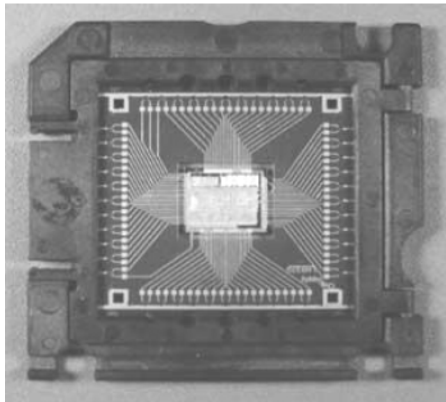


Figure 9-5. Tape Layout with Annular Ring [4]



(Courtesy International Micro Industries)

Figure 9-6. Excised TAB Assembly in Carrier for Testing

9.3 — TAB Assembly

TAB assembly begins with attachment of the die to the cantilevered inner leads. As with the flip chip, bumps are usually required. The bumps, typically gold, can be fabricated while the die are in wafer format using the thin film electrolytic plating process previously described. As an alternative, however, the bumps may be added to the TAB leads as part of the tape lead patterning process. A schematic close-up of the cantilevered leads and bumped die is presented in Figure 9-7(a). The Bumped TAB tape is shown in Figure 9-7(b). In both cases the bumps function as standoffs to prevent shorting of the TAB leads to the edge of the die.

A third method is to provide bumps by stud bumping. Stud bumping as previously discussed, has an advantage in that it can be applied to singulated die. Along this same line Tektronics introduced a “bumpless” inner lead attachment that entails direct bonding of the TAB leads to the Al bond pads on the die. Today this direct bonding of TAB leads is used on the µBGA™. The leads again are thermosonic bonded to the pads. The Bumpless TAB approach is seen in Figure 9-7(c).

It should be properly noted that only the electroplated bump process offers completely sealed Al pads, a critical attribute affecting reliability that is lacking with stud bumps (Chapter 10), the Bumped Tape TAB and the Bumpless TAB.

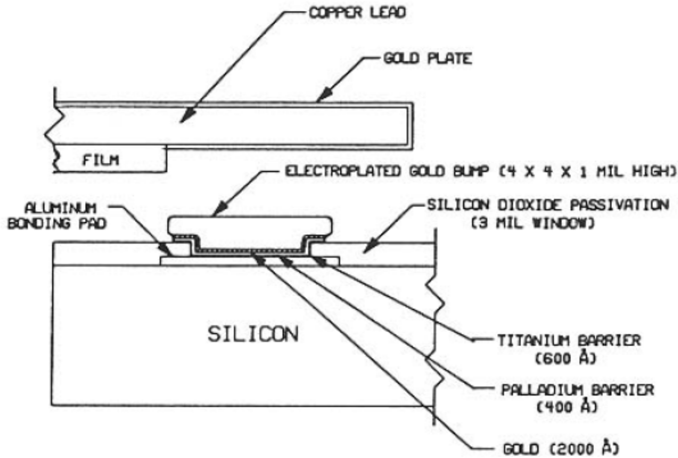


Figure 9-7(a). Schematic Bumped Die TAB [3]

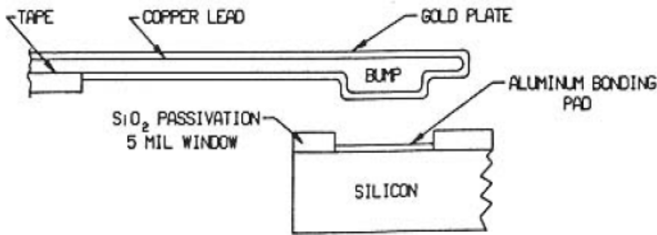


Figure 9-7(b). Bumped Tape TAB [3]

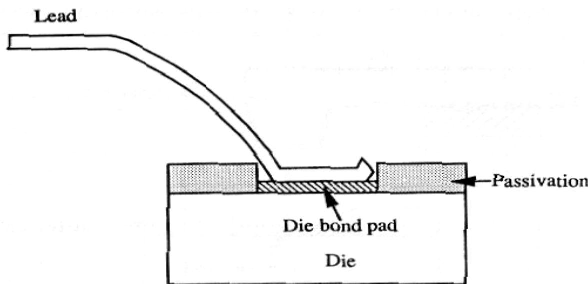


Figure 9-7(c). TAB Lead on Al Pad [4]

9.3.1 — Inner Lead Attachment Processes

Minimally modified wire bonding equipment is used for the inner lead attach, that is, the tape to the die. Attachment technologies are also similar to wire bonding and include thermocompression, thermosonic, and ultrasonic. A solder reflow attach is also an available option with solder bumped die. While TAB was originally intended to provide for gang bonding, a sequential single point bonding process subsequently emerged as a more reliable approach. This was precipitated by problems associated with Si cratering and non-bonded leads, all related to non-uniformity of plated bumps that was acerbated with higher I/O count ICs. Single-Point TAB bonding effectively negated these problems but resulted in significant decrease in productivity.

Single point bonding also eliminated the need for dedicated bonding tools for each IC type. One relatively simple bonding tool was all that was needed. And most importantly, it was readily implemented, being completely compatible with existing ball bonding equipment requiring the substitution of a simple flat tipped tool for the standard wire-bonding capillary.

9.3.2 — TAB Automation

The TAB tape strip format is totally attuned with a semi-automatic assembly process, particularly for the inner lead bonding process. The tape inner lead bonding assembly process is illustrated in Figure 9-8. The die are presented in an appropriate x-y matrix that allow each die to be positioned and aligned to the TAB's inner leads. The leads

are then bonded in a sequential mode that effectively emulates the wire ball bonding process. When all leads have been bonded, the tape is raised releasing the die from the matrix. The tape, which can be arranged in an inline reel-to-reel configuration, is then forwarded bring the next frame to the align/bond position and the process repeated.

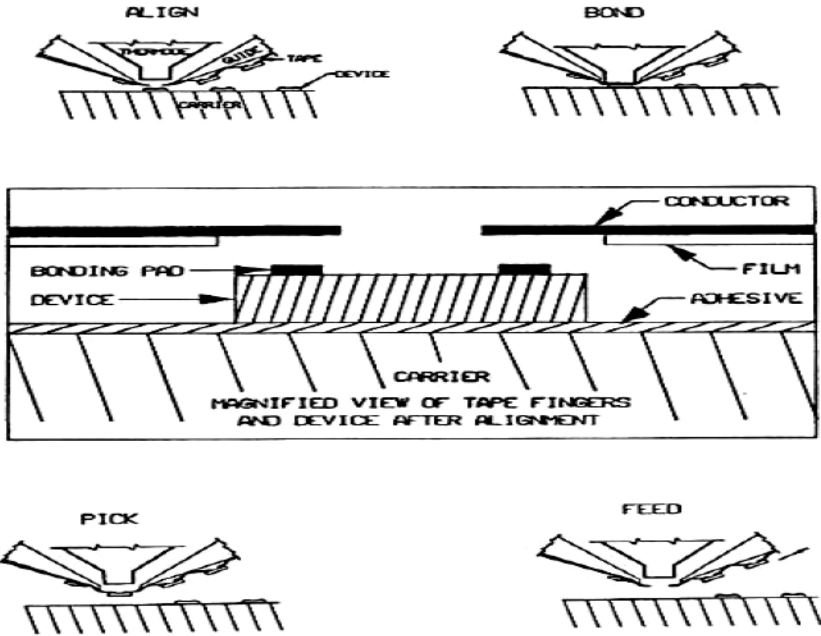


Figure 9-8. TAB Inner Lead Bonding Process [3]

9.3.3 — TAB Mounting and Attachment to Package/Substrate

TAB assemblies are attached to a package or substrate in one of three configurations, as shown in Figure 9-9. They are, face-up, flip or face- down, and recessed or cavity mounted. Each of the options offer advantages and disadvantages. For example:

- Face-up TAB is preferred since it provides ready heat sinking capability. Face-up will usually require the outer leads to be formed prior to bonding to a package. The formed leads further minimizes the potential for lead shorting to the die while at the same time producing stress relief when subjected to thermo-mechanical forces such as temperature and/or power cycling, and thermal shock. On The negative side, formed leads require a much larger footprint for attachment to the package or substate.
- Flip TAB or face-down TAB requires the smallest "footprint" of the three but loses ready heat sinking capability but, like flip chip, it can be readily fixed by the addition of a thermally conductive underfill material to the TAB assembly).

Examples of the face-up and flip TAB are shown in Figure 9-10.

- Recessed or cavity mount offers ready heat sinking without the need for lead forming and a "footprint" slightly less than the face up mount. A disadvantage is the added cost of the package/substrate.

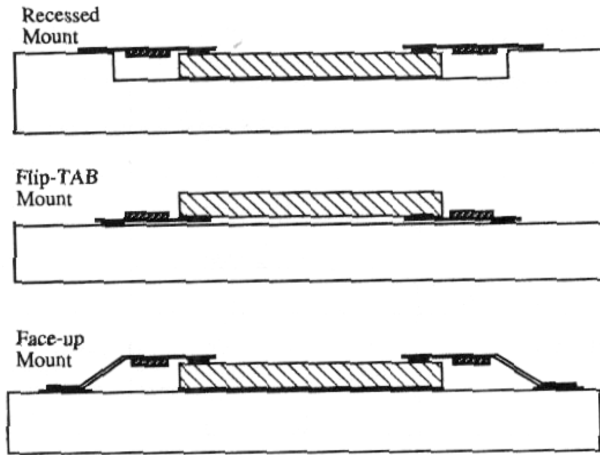
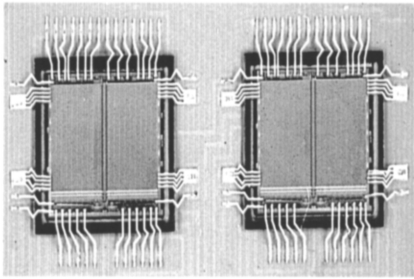
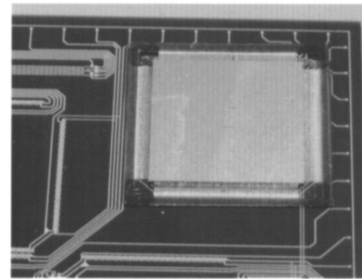


Figure 9-9. TAB Package/Substrate Attachment Options [5]





(Courtesy International Micro Industries)

Figure 9-10. Face Up and Flip TAB Bonding

TAB attachment, or outer lead bonding, techniques are essentially the same as with inner lead bonding and will be dictated primarily by the package/substrate properties and the metallization. Table 9-3 lists the various methods of inner lead bonding and lists the attributes, typical metallurgies needed for each, the metal thicknesses, and typical assembly equipment parameters. For the outer lead bonding, theromosonic bonding is more or less the norm on ceramic while solder attach is preferred for organic substrates.

Table 9-3. Comparison TAB Inner Lead Bonding Techniques [5]

Attributes/Technology	Thermocompression	Thermosonic	Ultrasonic	Solder
Material Systems	Au–Au	Al–Au	Al–Au	Sn–Sn
(Bump/Lead plating)	Au–Al	Al–Al	Al–Al	Sn–Solder
	Cu–Au	Au–Au		Au–Solder
	Cu–Cu			Solder
Bonding Technique	Gang/	Single Point	Single Point	Gang/Single Point
	Single Point			
Potential Die Damage	High	Medium	Low	Low
Temperature (°C)	150–300 (sub)	150–250	200–400	Ambient
	400–500 (Tool)			
Bond Time	0.2–1.0 sec	~ 20 msec	~ 20 msec	1–6 sec
Fine Pitch Capability	Excellent	Good	Good	Fair

9.4 — Reliability Concerns [4–6]

TAB Assemblies have many interfaces that present concerns relative to reliability. In general the more interfaces the greater is the potential for problems. Figure 9-11 identifies the location of various potential failure sites. Failure mechanisms that affect TAB assemblies include,

- Delamination (1, 4, 5)
- Lead Fractures (2, 3, 6, 7)

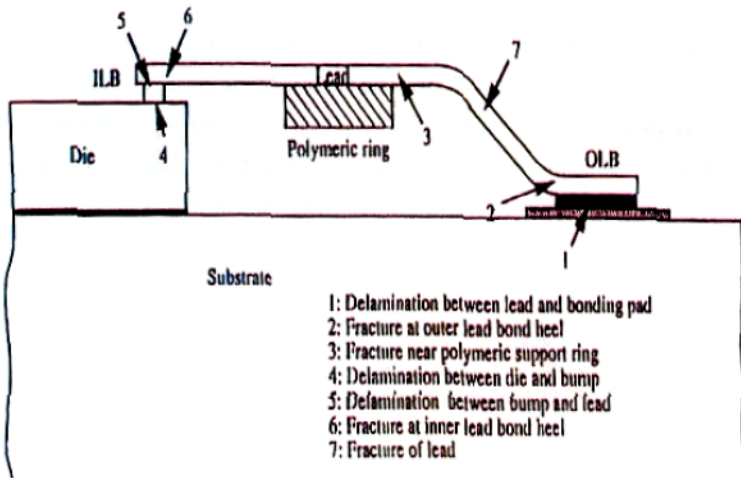


Figure 9-11. TAB Failure Sites [3]

Delamination generally occurs at bond interfaces. Delamination can be attributed primarily to the bonding materials and the process. It can be properly addressed by exercising tight control of the interface materials, in particular, the plated Au, its purity and softness, and the bonding parameters including temperature, ultrasonic energy and the bonding gram-force.

Lead fractures appear to be the direct result of the lead forming employed to assist in the face-up bonding. It can be easily eliminated by going to a flip TAB that also offers the advantage of a smaller footprint for the attachment.

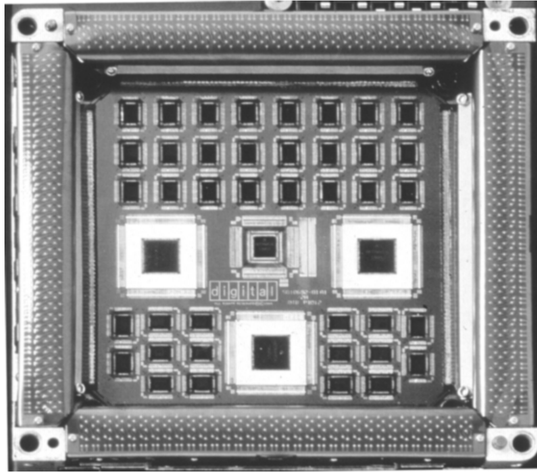
9.5 — Areas of Applications

When first introduced TAB generated much interest as a cost effective first level alternative with the potential for supporting high volume, low cost IC assembly. It generated several in-house development programs within the major semiconductor manufacturers including Motorola, TI and RCA. Implementation however uncovered problems all of which impacted the cost factor. These included cost associated with putting in place wafer bumping operation, the cost of the tape and dependence on a limited number of tape manufacturers, plus the major investment in capitol equipment and tooling required for automated reel-to-reel assembly.

To those outside the semiconductor venue, in particular hybrid circuit/MCM manufacturers, a key feature of TAB was the fact that it offered a way to address the problem of assembling pre-tested devices for MCP and COB applications. Indeed, as previously discussed TAB bonded devices could be electrically tested and burned-in before being assembled into MCPs. It was in effect the first KGD approach long before KGD became an item with MCM applications. In fact, if the TAB device was "glob topped" it in reality also became the first "near-die size" CSP. To these manufacturers it meant more and more die could be assembled onto a substrate with little or no rework required due to electrically defective devices.

Electronic equipment manufacturers, in particular, Tektronics and Digital Equipment Corporation, committed heavily to TAB. Figure 9-12 shows an assembly, a central processing unit (CPU), from Digital Equipment that used TAB for all devices. This allowed for pre-assembly electrical testing of every device, that in turn made possible an enhanced and acceptable final assembly yield.

TAB applications in the U.S. are now quite limited but are still finding favor "offshore" for niche applications in the high volume low cost arena such as calculators and watches. TAB technology, however remains a very strong factor in the manufacture of μBGA packaging.



(Courtesy International Micro Industries)

Figure 9-12. Microprocessor Module (~5"x5") with all TAB Device Assembly

9.6 — Summary

TAB came with great promise in the early 1970s, challenging C&W as the Level 1.0 interconnect of choice. It lost out however with the introduction of the automatic wire bonder. It did have a resurgence in the early 1980s because of its pre-assembly test capability and provided the first KGD. TAB also made available a "near-die size" package, fully tested, including burn-in, ready for assembly into a hybrid circuit or a PWB. Its downfall was the cost factor. Manufacture of the tape was expensive and a new tape design was needed for each IC adding further to the cost. Additionally, it required a sizeable investment in capitol equipment. It simply could not compete with C&W.

It left a legacy that continues today in the use of flex circuits in packaging, as a temporary carrier for KGD, and more importantly, in the manufacture of CSPs and 3-D packaging.

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10 Flip Chip—The Bumping Processes [1–4]

10 — BACKGROUND

The cost factor associated with chip & wire assembly was one of increasing concerns with the emergence of the IC. This precipitated major development programs in most semiconductor houses directed towards new, less costly assembly processes. These included Beam Leads (BL) from Bell Laboratories, Flip Chip (FC) from IBM, and Tape Automated Bonding (TAB) from General Electric. From these efforts, two technologies survive and currently provide alternatives to chip & wire assembly for the IC, flip chip (FC) and TAB.

10.1 — IBM's Flip Chip Transistor

Flip chip, as an alternative first level assembly process, was developed by IBM in the 1960s and was introduced in 1973 on the IBM System 3 mainframe computer. Delco, also in the early 1970s, became active in applying flip chip technology to a bourgeoning automotive electronics market.

Figure 10-1 is a schematic of the IBM flip chip transistor and shows a ceramic package containing 3 flip chip transistors. The package is ceramic with screen printed conductors and resistors.

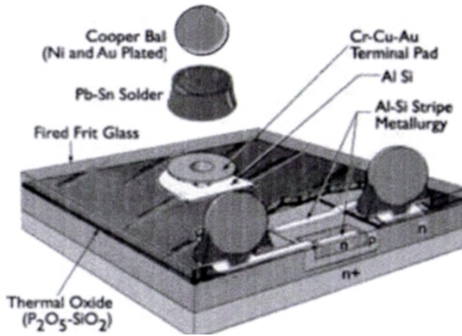
10.1.1 — The IBM Flip Chip Process

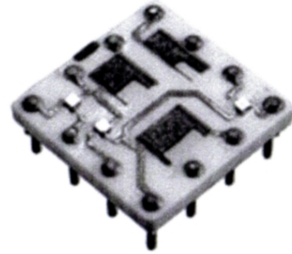
The manufacturing process for the flip chip included:

- Deposition and patterning of a glass frit (for "passivation") to expose the Al bonding pads, and
- Deposition and patterning, using a metal mask, of a solderable material (Cr-Cu-Au) over the exposed Al bond pads.

This layered metallurgy is referred to as the Under Bump Metallization, or UBM. Using a solder perform over each pad, Ni and Au plated Cu balls were individually placed onto the preform and the solder preform reflowed. All this was accomplished while the devices remained in wafer format—the first "Wafer Level Packaging" process.

(a) Flip Chip Transistor **(b) Flip Chip Assembly**





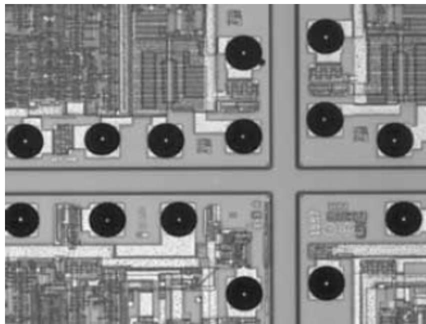
(Courtesy IBM Corp.)

Figure 10-1. (a) IBM's Flip Chip Transistor; (b) Multichip Transistor Assembly

The devices, following singulation, were assembled to a package by a solder reflow process. The device was attached face down, hence, the name "flip chip". The Cu balls in this case do not melt but rather serve as standoffs to negate the possibility of damage to the device surface during attachment.

10.1.2 — Flip Chip from Transistors to ICs

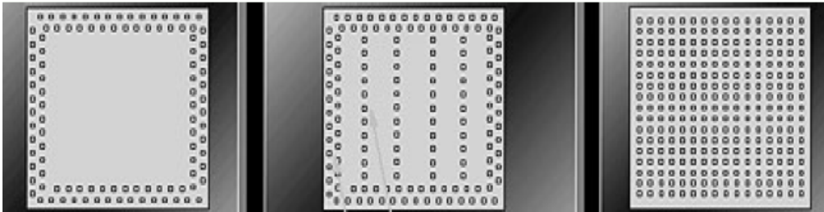
The flip chip transistor inevitably gave way to a flip chip IC, with bumps deposited directly over the bond pads located around the periphery of the die like that shown in Figure 10-2. As the I/O count increased, however, alternate pad configurations emerged. With today's ICs, pad configurations vary with the most common still a peripheral format, in single or staggered double rows. These formats represent the majority of current ICs, designed not for flip chip but rather for wire bonding.



(Courtesy Fraunhofer IZM)

Figure 10-2. IC with Bumps Directly on Bond Pads

With the high performance devices, the microprocessors and DSPs with very high I/O counts, the pad layouts moved to either a combination of peripheral and array area or full area. Full array devices are typically designed specifically for flip chip bumping. The three configurations are illustrated in Figure 10-3.

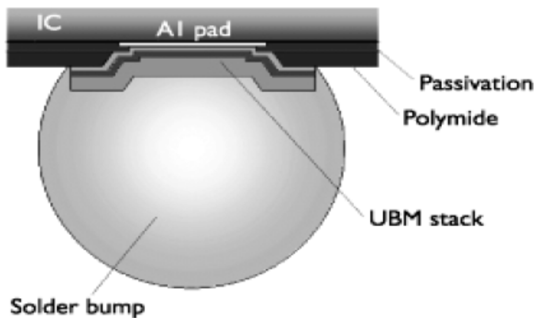


(Courtesy IBM Corp.)

Figure 10-3. IC I/O Pad Formats: (L to R) Dual Row Peripheral, Peripheral + Partial, Area Array

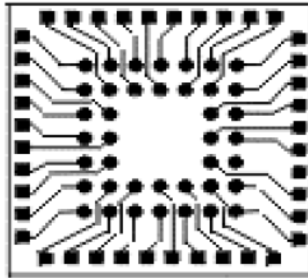
For low I/O count single row peripheral pads, bumps may be deposited directly over the existing bond pads as shown in Figure10-4(a) assuming compatible pad size and pitch, typically 100 micron pads and 200 microns pitch and greater.

With smaller pitch a "remetallization" or "redistribution" of the pads may be necessary to accommodate the bumps for flip chip assembly. This is achieved by providing a second layer of metal—using a thin film process—that allows for relocation of the I/O pads from peripheral to an area array format. This is illustrated in Figure 10-4(b). Figure 10-4(c) shows a schematic cross section of the redistribution layer (RDL), and Figure 10-4(d) an actual IC with the redistribution layer clearly visible. If properly designed the RDL can offer a way of avoiding problems associated with "die shrink". This is realized by relocating the bumps closer into the center of the die as is also shown in Figure 10-4(b). It should be noted that the re-distribution process is basically the same for both the flip chip and the Wafer Level CSP.



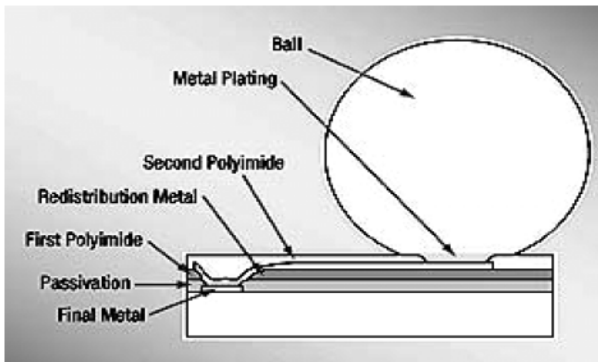
(Courtesy Flip Chip International)

Figure 10-4(a). Direct Bump on Pad



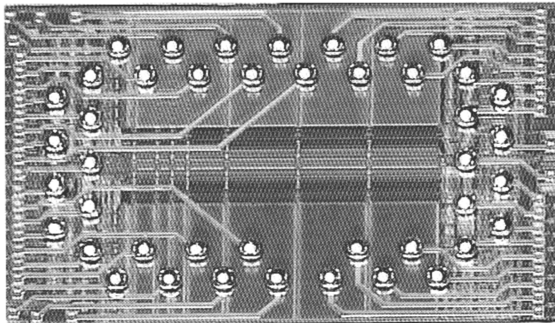
(Courtesy Flip Chip International)

Figure 10-4(b). Schematic Redistribution Layer (RDL)



(Courtesy Unitive)

Figure 10-4(c). Schematic of Relocated Pad and Bump



(Micron Technology)

Figure 10-4(d). SDRAM Flip Chip with Redistributed Bond Pads

10.2 — Wafer Bumping [5–8]

Flip chip and Wafer Level CSP, as previously discussed, share a key characteristic, namely, both are true die size differing only in I/O bump geometry, that is, bump diameter and pitch. It should therefore be obvious that both would also share common processing except for the actual deposition of the bumps. Thus, discussion of flip chip wafer bumping is therefore fully applicable to the manufacture wafer level packages as well.

There are several wafer bumping processes available. Selection of a particular process is dependent for the most part on the end product and particular application to be addressed. Thus, concerns such as temperature limitations, materials, and most importantly, the cost factor must be considered. In addition, the impact of RoHS, Removal of Hazardous Substances (discussed in Chapter 3) in end product dictating minimal use of solders containing lead is a concern as well. It begins with identifying the type of bumps which in turn dictates the subsequent assembly process.

10.2.1 — Bump Metallurgy and Selection [9,10]

Commonly used materials for bumping include Au, Cu and most solders. Solders however, are the most preferred attachment medium. Table 10-1 list several solders with their melting points, most frequently used in flip chip applications. It includes lead-free SnAg and SnAgCu solders. The latter has emerged as the favored lead-free replacement for eutectic and other lead bearing solders.

Table 10-1. Reflow Temperatures for Common Solder Bump Materials

Solder Composition (%)	Reflow Temperature (ºC)
95Pb5Sn	330–340
63Sn37Pb (eutectic)	215–225
50Pb50In	260
37Pb63Sn	290
95.5Sn3.5Ag1.0Cu	235–255
96.5Sn3.5Ag	230–250

One can also classify bumps based on their characteristic as part of the attachment medium. They include:

- Totally remeltable Bumps

  Remeltable bumps, also referred to as “collapsible bumps”, include all solders. They are used extensively in the majority of flip chip applications. Soft solder attachment, which covers high lead/tin (ceramic based package/ substrate) and eutectic tin lead (ceramic and organic package/substrate) in particular, is the most preferred assembly process for flip chip. The height of the bumps after reflow assembly are less than the original “as deposited” height. It is this final bump height that determines the spacing or “gap” between the face of the chip and the package/substrate surface.

- Partly remeltable Bumps

  Partly re-meltable bumps, or "non-collapsible", include Au, Cu bumps and high Pb bumps capped with eutectic SnPb or Sn. In the latter case the capping allows reflow attachment, at 200–230ºC, of high Pb bumped flip chip to an organic board. The non-meltable bumps do not change dimensionally following reflow and thus function effectively as a "standoff", providing for a controlled "gap" spacing. A larger "gap" is preferred particularly when an underfill is to be applied for enhanced reliability (Chapter 11). Use of Cu bumps also offer the added advantages of high electrical and thermal conductivity, bump properties that become increasingly pertinent in addressing future generation ICs.

- Non-meltable Bumps

  Non-meltable bumps include Au, Cu and Ni-Au and are used in applications where solder attachment is impractical, e.g., non-solderable materials. Non-meltable bumps are used most frequently with adhesive as the attachment medium. Au and Ni-Au bumps are also assembled using thermocompression, ultrasonics, or thermocompression bonding methods. These require specialized equipment for flip chip assembly, a flip chip aligner-bonder, which as the name implies, allows an operator to first align the flip chip to the matching footprint on the package and then bond the die by applying heat, pressure and/or ultrasonic energy.

- Polymeric Bumps

  Adhesive bumps, conductive or non-conductive polymers, are used mostly in applications where soldering is not possible because of the high processing temperature or the materials involved are not solderable.

10.2.2 — Under Bump Metallization (UBM) [10,11]

Wafer bumping for both flip chip and TAB are two-step processes covering the deposition of an under bump metallization (UBM) and followed by the deposition of the bump material. The UBM is crucial and provides a solderable contact to the device's non-solderable Al bond pads. The UBM is a critical part of the overall bumping process and is a determining factor in long-term reliability. The selection of the proper UBM will be based on several issues that must be taken into consideration. The bump metallurgical composition is a key factor. Table 10-2 lists various bump materials and the favored UBM.

10.2.3 — UBM Deposition Processes

Prior to the UBM deposition and depending upon the device and the particular bumping process a polyimide "passivation" layer may be deposited to provide protection for the device's metallization interconnections from attack from chemicals

that might be used in both the UBM deposition and patterning processes. The metals are deposited by:

- Vacuum deposition, that is, evaporation or sputtering, or
- Chemical deposition (Electroless Ni/Immersion Gold—ENIG)

Table 10-2. Typical Bump Materials and Favored UBM [5]

Bump Material	UBM Layers
Au	Ti/W-Au
High Pb (95/5)	Ti-Cu, Ti/W-Cu, Cr-CrCu-Cu-Au, Al-NiV-Cu
Eutectic SnPb (63/37)	same as high lead, Ni-Au
SnAgCu (95.5/3.5/1.0)	Al-NiV-Cu
SnAg (96.5/3.5)	Ni-Au

10.2.3.1 — Deposition of UBM by Evaporation or Sputtering [12]

The UBM process, which follows, involves the sequential deposition of the metal layers in a sputtering or evaporation process. The UBM is typically a multilayered metal structure consisting of an initial layer that acts as an "adhesion" layer to the Al. This is followed by a "barrier" layer that is intended to prevent the unwanted interdiffusion of the various metals and the Al pads.

The adhesion layer is usually in the 0.1–0.2 µm thickness range and the barrier layer(s) which also provides high conductivity and the required solderable metal is thicker, typically several microns thick. A final thin layer of Au is often needed to provide protection to the solderable metal layer that might be prone to oxidation, as is the case for example, with Cu.

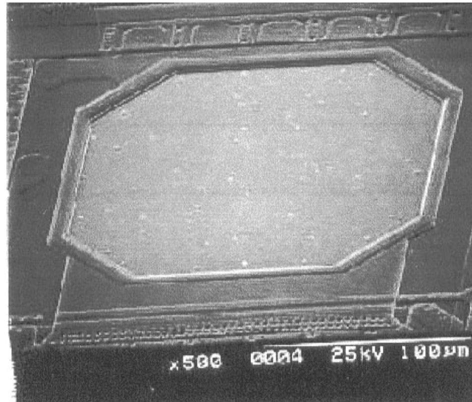
Depending upon the particular bumping process the UBM may or may not be patterned prior to the actual bumping. Note that the UBM is typically designed to overlap the passivation opening over the bond pad. This effectively seals off the Al metallization. This insures no Al metal is exposed during any subsequent bumping process, eliminating possible damage to the IC's pad metallization.

10.2.3.2 — Chemical Deposition—ENIG [13,14]

A Ni-Au UBM can be deposited using a wet chemical process. In this wafer based process the Ni is deposited using electroless Ni and an immersion Au plating (ENIG). The step-by-step process is as follows:

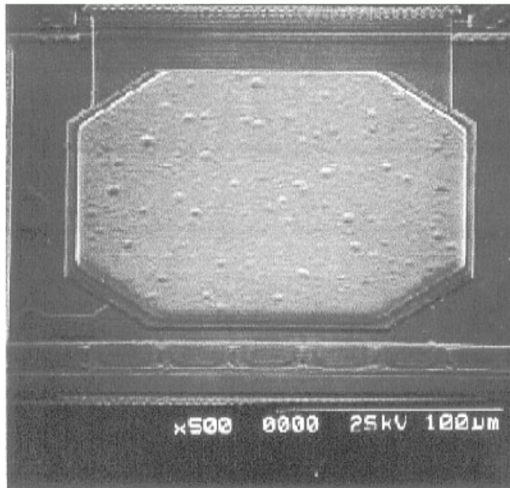
- Clean Al pads
- Activate Al using a zincate solution
- Electroless plate Ni
- Immersion plate Au

Figure 10-5(a) is a SEM of an Al pad (as received), Figure 10-5(b) an Al pad after the zincate process, and electroless Ni and immersion Au plating.



(Courtesy IC Interconnect)

Figure 10-5(a). Al Pad as Received



(Courtesy IC Interconnect)

Figure 10-5(b). Al Pad after Electroless Ni/Immersion Au Plating (5 microns thick)

10.3 — Bump Deposition Processes

Several bump technologies have been developed supporting flip chip assembly. They include:

- Direct Bump/Ball Placement
- Evaporation
- Electrolytic Plating

- Stencil Printing
- C4NP (IBM)
- Jet Printing
- Electroless Plating

The type of bump basically dictates the flip chip assembly process. For example solder infers a reflow solder assembly while a Ni-Au bump or stud bump typically implies an adhesive attach process.

With solder bumps and solder reflow the preferred process for flip chip assembly, electroplating and stencil printing are currently the dominant technologies within the industry. C4NP, however, has recently been introduced by IBM and appears to offer several notable advantages, i.e., low cost and a highly efficient use of all available solders including lead-free.

10.3.1 — Direct Bump/Ball Placement [15]

The first flip chip bumping process, as previously described for the IBM transistor, used Ni-Au plated Cu balls manufactured separately and mechanically deposited. Figure 10-6 illustrates one of several methods for bump/ball placement onto packages. Unlike other bumping methods with spheres the size of the balls (bumps), it is not process limited. Bumps/Balls as small as 100–125µm can be directly placed. Hence, this method has application to BGAs, CSPs *and* Flip Chip. Considered to be unacceptable early on because of increase in I/O count of the IC, it has experienced a resurgence due in no small part to the development of placement equipment and the emergence of area array packages.

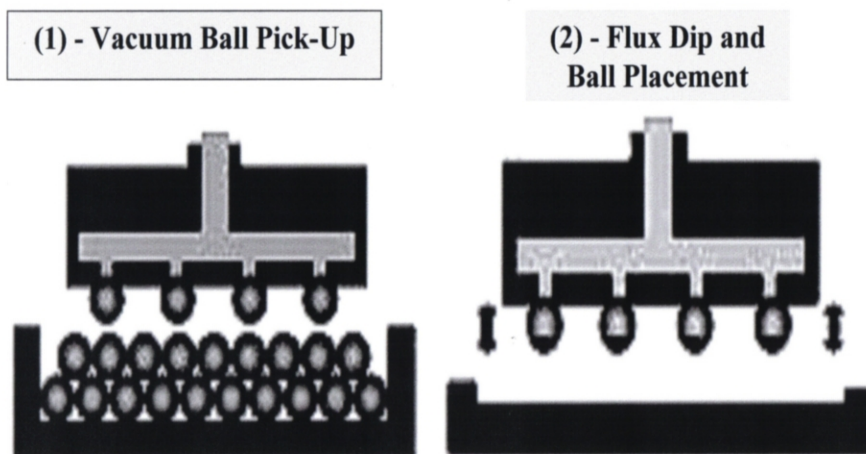
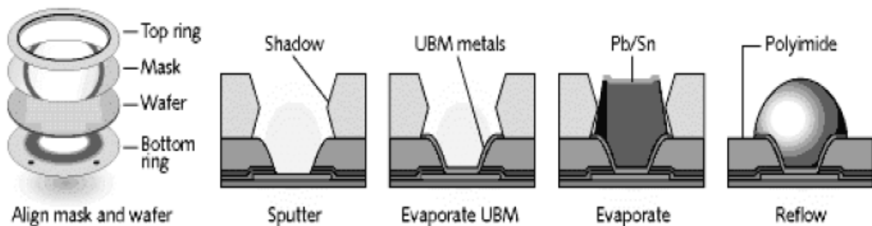


Figure 10-6. Ball Placement by Vacuum Process [15]

10.3.2 — Bumping by Evaporation: The IBM C-4 Process

From the beginning the IBM approach for device attachment was solder based. With the emergence of the IC, IBM proceeded to develop a process to replace the use of discrete spheres. Referred to as C-4 or Controlled Collapse Circuit Connection, it involved the deposition and patterning of a UBM, followed by the selective deposition by evaporation of a high lead solder through a metal mask. Figure 10-7(a) describes the C-4 evaporation process.

The metal mask is critical to the deposition and patterning of the UBM and the solder. The mask, typically molybdenum (moly, Mo), is fabricated using a patterned photosensitive resist and chemically etching the moly using the resist as the etching mask. When the moly mask is aligned to the wafer, the openings in the mask will correspond to the locations on each IC on the wafer where bumps are required.



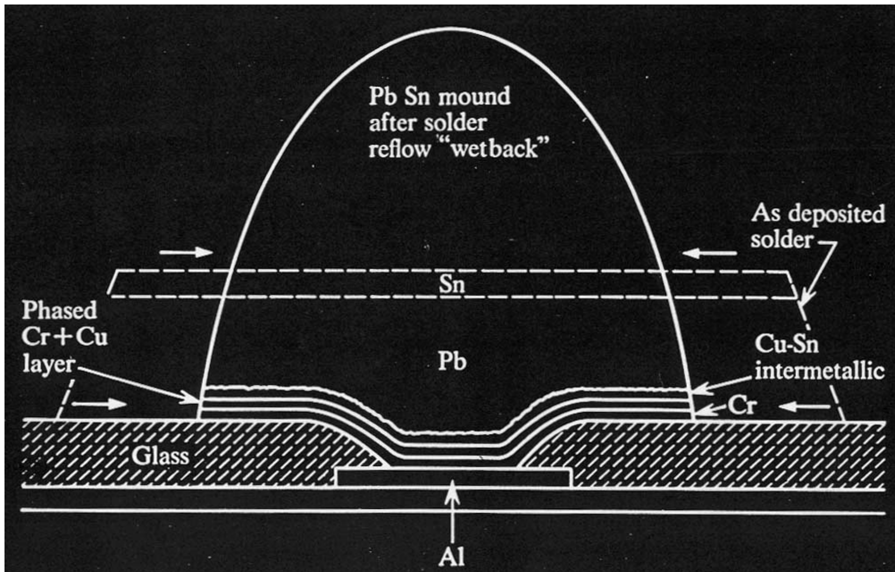
(Courtesy Freescale Semiconductor)

Figure 10-7(a). The Evaporation Bumping Process (C-4)

Figure 10-7(b) shows the as deposited solder and illustrates the change that takes place in the geometry of the evaporated bump after reflow. Note that the evaporated bump is trapezoid in shape and extends beyond the UBM. On reflow however, the solder is confined and can only adhere to the UBM. The UBM thus influences the size of the reflowed bump, which is now spherical in shape and higher than the as deposited bump. Both the amount of solder deposited, the geometry of the opening in the moly mask, and the area of the UBM control the final bump height that is critical for assembly. For a constant solder volume and fixed mask geometry, the bump height after reflow is a function of the area of the UBM—the smaller the area, the greater the bump height and vice versa. In this case the UBM is a Bump Limiting Metal, or BLM.

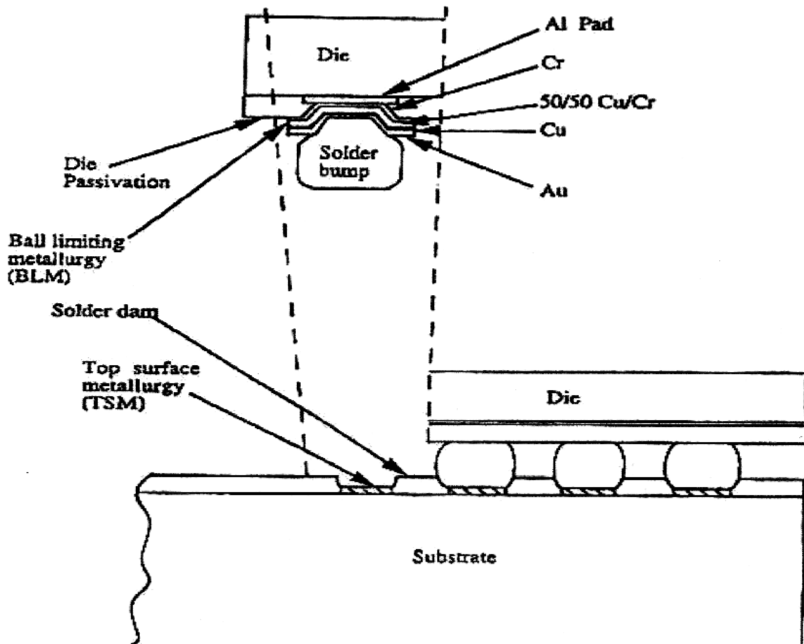
The evaporation process has limitations. Masks to accommodate both increasing I/O count and reduced bump pitch become increasingly more difficult to manufacture and are limited to ICs with I/O count of approximately 3000 and a minimum 200 microns pitch. Additionally, the number of solder alloys that can be evaporated is limited.

The evaporation bumping process when combined with an assembly process as illustrated in Figure 10-7(c) comprises the basic IBM C-4 process technology. The solderable metal pad on the package is "dammed" to restrict flow of solder at liquidus. This, along with the BLM on the die will control the final reflowed bump



(Courtesy IBM Corp.)

Figure 10-7(b). Schematic of C-4 Evaporated Bump Before and After Reflow



(Courtesy IBM Corp.)

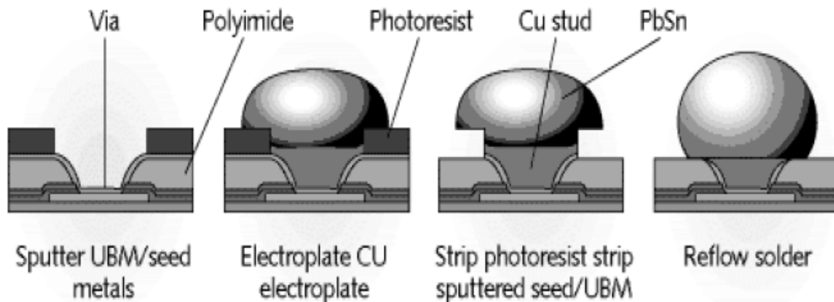
Figure 10-7(c). Solder Dammed Substrate Pad (C-4)

size, that in the end equates to the final bump height, and therefore, the gap between the surface of the die and the package. IBM offered the complete C-4 process under licensing. The cost was prohibitive and for many interested in implementing flip chip this cost factor was, arguably, instrumental in delaying extensive exploitation of the technology. The C-4 process was, however, licensed by several major companies notably, Delco Motorola, Texas Instruments, and Intel.

10.3.3 — Electroplated Bumps [16,17]

Electroplated bumping processes were developed as a more cost-effective approach to bumping by evaporation. The key to all electroplating processes is the photoresist film which when defined, acts as the template or mask, allowing the selective deposition of fairly thick (>25µm) metals and alloys. Figure 10-8 shows the electroplated process sequence for solder bumps.

The process is typical thin film. Following the deposition and patterning of a passivation layer the UBM is sputter deposited. Photoresist is applied and patterned. Using the UBM, which covers the entire wafer, as a plating buss and the resist as a mask, solder is selectively plated. Following stripping of the resist, the UBM is etched away using the plated solder as an etch mask. The plated solder is then reflowed.



(Courtesy Freescale Semiconductor)

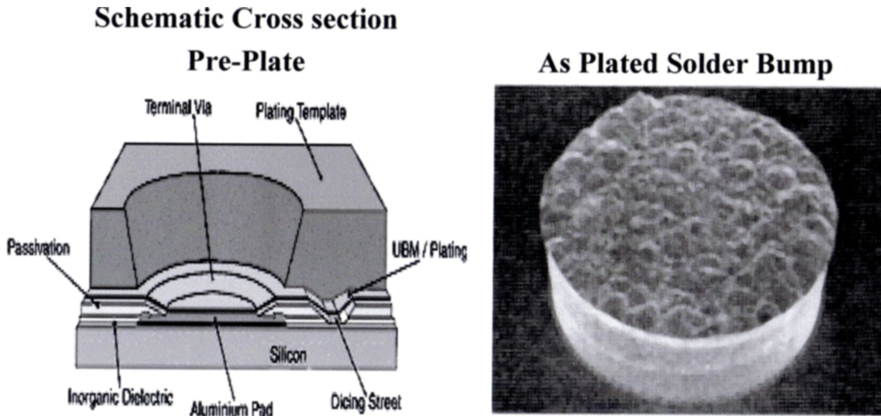
Figure 10-8. The Electroplated Solder Bumping Process

Figure 10-9(a) shows a schematic cross-section of a typical bumping site prior to the plating. Also shown is an as-plated solder bump. Solder bumps for flip chip are typically 75 to 125 microns in height and diameter on 200 to 225 micron pitch. However since photoresist is used as the mask, bump pitch down to 150 microns are readily achievable. Solders that can be electroplated include PbSn and Eutectic PbSn and the lead-free SnAgCu.

10.3.3.1 — Copper and Gold Plated Bumps

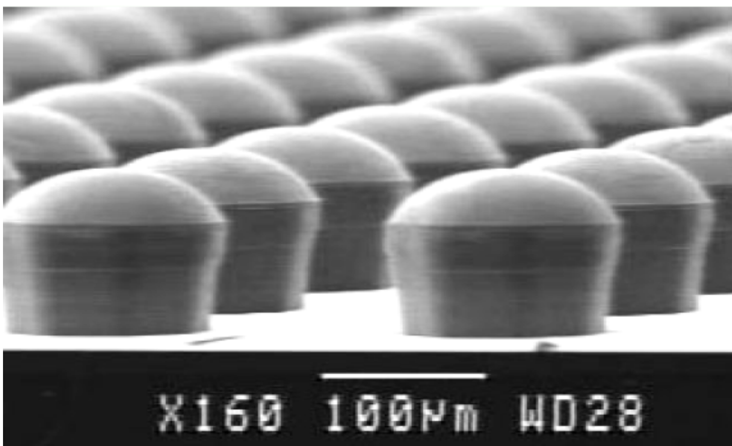
The electroplating processes for both Cu and Au are very similar. For Cu bumps, the UBM and process sequence is basically identical. It is essential for this process however, that the resist mask be thicker than the final bump thickness. It is basically

an extension of the Cr-Cu UBM deposition process. The Cu is merely plated much thicker. Figure 10-10 is a SEM of electroplated Cu bumps. The Cu bumps typically have a thin layer of either eutectic SnPb or Sn added for solder attachment at the next level.



(Courtesy IBM Corp.)

Figure 10-9. Schematic Cross-section of Bump Site Pre-Plating and AS-Plated Bump



(Courtesy TMLI Corp.)

Figure 10-10. SEM Electroplated Cu Bumps

For Au plated bumps, a seed layer of TiW/Au is deposited by sputtering. The TiW/Au layer functions as a plating buss and using a patterned resist film as a plating mask additional Au is selectively plated up to a desired thickness. After stripping the resist, the relatively thin sputtered TiW/Au (approximately 0.25 mi-

crons) is chemically etched away with the electroplated bump serving as the mask. Some of the Au bump is removed by the etching. However, since the bump thickness is on the order of 20 to 25 microns the effect is negligible. Figure 10-11 shows plated Au bumps, all with straight sided vertical walls resulting from a well defined resist that is thicker than the plated up bump. When the resist mask is thinner than the thickness of the plated bump a mushroom shape results since the resist no longer confines the plating to the vertical direction only. For very fine pitch bond pads mushroom bumps must be avoided and use of the thicker resist is a necessity. Au bumps are typically used for Tape Automated Bonding and for applications where die attachment is with an adhesive or accomplished using thermosonics or ultrasonics, e.g. SAW devices.

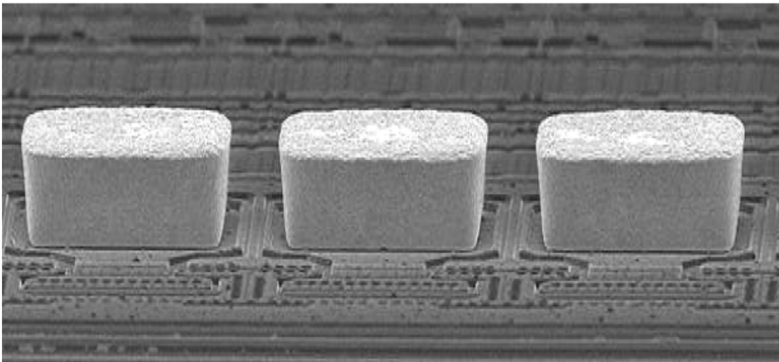


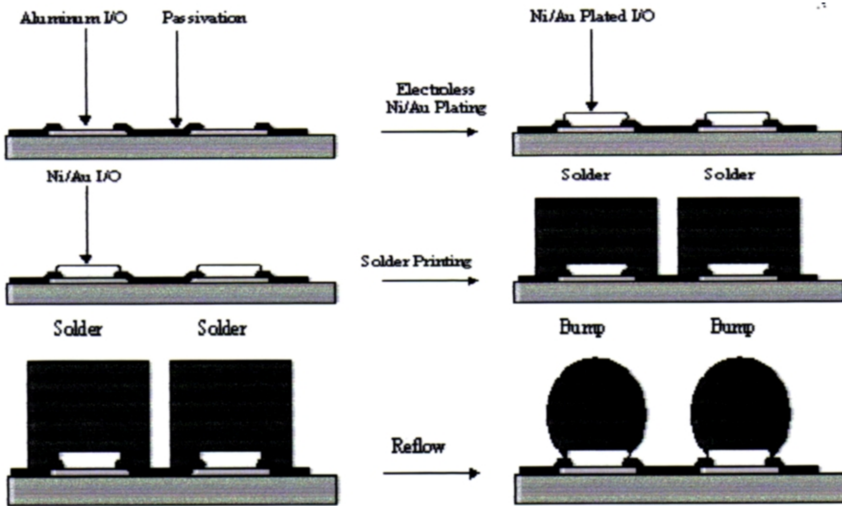
Figure 10-11. Electroplated Au Bumps

10.3.4 — Bumping by Stencil Printing [18–20]

Use of stencil printing for bumping is confined to solder pastes and adhesives (conductive epoxy). For solder the final bump size is a function of the stencil thickness and the area of the opening in the stencil. The printed solder paste is deposited over an area larger than the UBM. Upon reflow the solder wetting will be confined to the area of the UBM. Figure 10-12(a) shows a complete wafer bumping process including the UBM deposition and the subsequent bump deposition using stencil printing.

The stencil is usually metal however an alternative approach uses an organic film as a template (e.g., photosensitive film, polyimide or BCB, or a pre-defined Kapton™ film). Figure 10-12(b) graphically illustrates both stencil print processes.

Stencil manufacturing technology currently limits application to bump pitch of 200 microns and greater.



(Courtesy IC Interconnect)

Figure 10-12(a). Wafer Bumping Process Using Stencil Printing

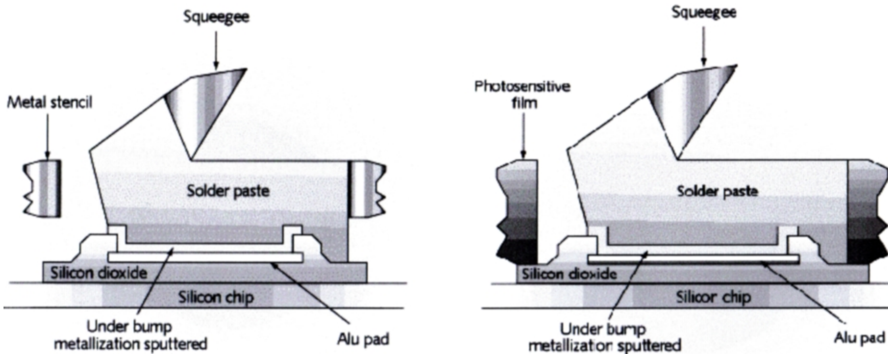


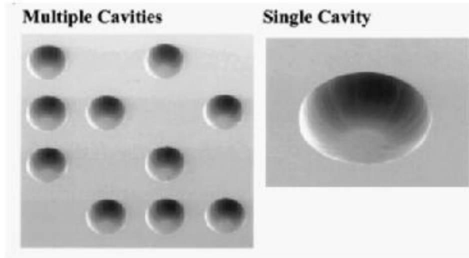
Figure 10-12(b). Bumping by Stencil Printing [8]

10.3.5 — The IBM C-4NP Bumping Process [21–23]

IBM recently developed a new low cost bumping process called C-4NP. Totally environmentally friendly it provides for a process capable of depositing any solder alloy, high lead, eutectic SnPb, and lead-free. No pastes are involved, only molten solder. The solder bumps are more uniform and void free since they are deposited while in the molten state. The wafer, with a sputtered UBM in place, is only subjected to a single “dry” solder transfer step. Additionally, the process is capable of accommodating much tighter pitch (less than 100 microns).

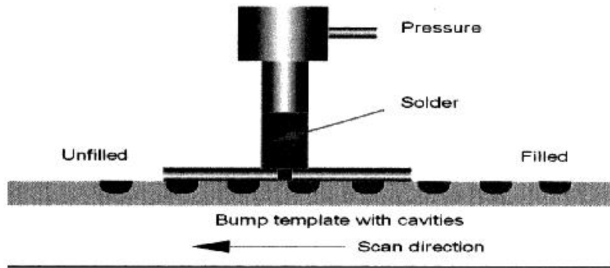
The process makes use of a glass substrate mold. The mold has a TCE matching that of silicon. The mold contains cavities that correspond to the bond pads on a

particular IC. The cavities are produced using photolithography and chemical etching of the glass. A photomicrograph of a mold is shown in Figure 10-13(a). The cavities are filled with molten solder in a solder fill process illustrated in Figure 10-13(b). The Solder transfer to the wafer is presented in Figure 10-13(c).



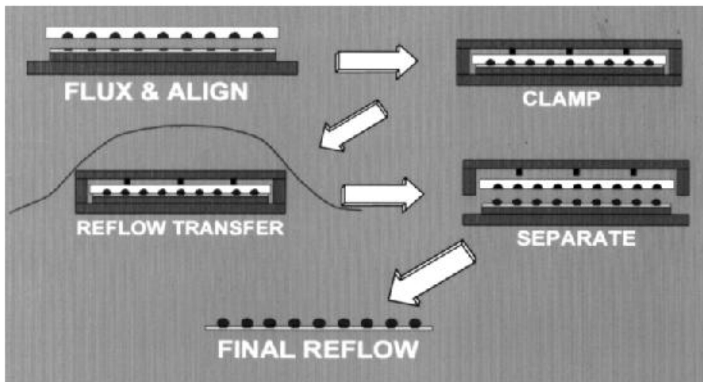
(Courtesy IBM/SUSS MicroTec)

Figure 10-13(a). C4NP Mold with Cavities Corresponding to Bump Locations



(Courtesy IBM/SUSS MicroTec)

Figure 10-13(b). Molten Solder Filling of Mold Cavities



(Courtesy IBM/SUSS MicroTec)

Figure 10-13(c). Molten Solder Bump Transfer to Wafer

C4NP is an IBM patented process. SUSS Microtec under a technology and licensing pact with IBM will assist in the commercialization of C4NP and will be the prime supplier of all necessary equipment associated with the process. Under terms of the agreement C4NP licensing is included in the purchase of the equipment through SUSS Microtec.

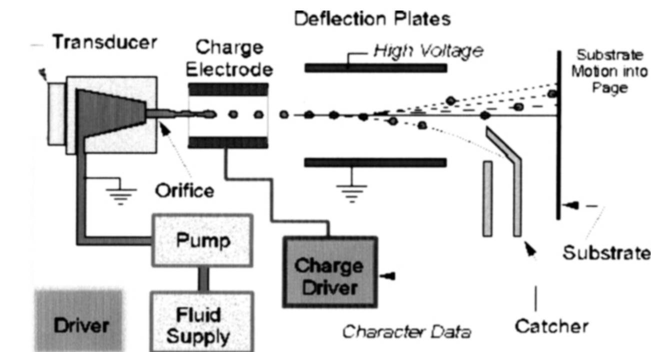
C4NP is a key enabler to low cost lead-free wafer bumping. The low cost is because of the simplicity of the process and the high yields achievable. It is also capable of meeting future requirements for smaller diameter and finer pitch bumps. Bumps 75µm diameter and 150µm are available and 25µm bumps on 50µm pitch is realizable.

10.3.6 — Solder Bumping by Jet Printing [24,25]

Using technology similar to that used in ink jet printing, molten solder microspheres can be deposited onto a variety of substrates. Molten droplets 25 to 250 microns in diameter can be deposited at rates in access of 2000 per second.

Jet printing requires specialized equipment. There are two processing modes for solder jet printing: the demand mode and the continuous mode. The latter offers significantly higher deposition rate than the demand mode. Figure 10-14 is a schematic representation of the continuous mode ink jet bumper and shows a sample of 100µm eutectic 63Sn37Pb solder bumps deposited by solder jet printing.

In the continuous mode molten droplets are continuously generated. Molten drops upon being dispensed from the orifice are electrostatically charged. A second electrostatic field at the substrate controls drop placement. The molten solder droplet is approximately twice the diameter of the orifice. Solder bumps as small as 25µm can be deposited.



(Courtesy MicroFab Technology, Inc.)

Figure 10-14. Continuous Mode Solder Jet Technology

10.3.7 — The Electroless Ni/Immersion Au (ENIG) Process [26]

The electroless Ni-Immersion Au process is unique in that the process is low cost, "maskless", and serves as a method for depositing a UBM and by extension, a complete bumping process. This is realized by simply increasing the thickness of the electroless Ni deposit. The Au, in this case serves to prevent passivation of the nickel (and subsequent loss of solderability) and therefore is typically on the order of 0.05–0.5 microns thick.

Figure 10-15 contains a schematic cross-section of a Ni-Au bump and a SEM of a 20 micron bump.

Because the plating is confined to the Al pad only, as the Ni plating is increased to provide a thicker bump, the plating assumes a "mushroom" shape, overlapping the opening in the device passivation as seen in the figure. Bump heights in the 15 to 20 micron range are achievable. The overlapping, roughly equivalent to the bump height, limits application to a minimum pad pitch of 150–200μm. Non-recurring charges however, are low since no photomask is required unless an optional passivation layer is added prior to beginning the Ni-Au plating.

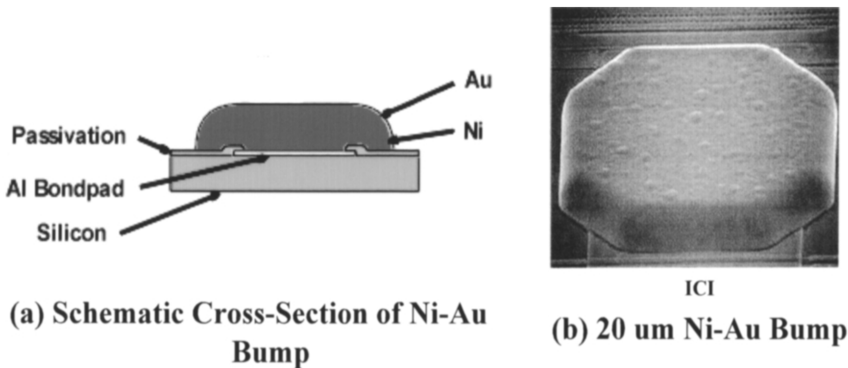


Figure 10-15. (a) Schematic Cross-section of NiAu Bump; (b) 20μm Ni-Au Bump

10.4 — Comparing Flip Chip Solder Bumping Processes

Table 10-3 compares the various bumping processes. The most commonly used processes for bumping are electroplating (electrolytic and ENIG) and stencil (metal and template) printing. The C-4 evaporation process has been included to provide an historical perspective highlighting the development of more cost effective processes that more fully support high volume manufacturing needs. The C-4NP, while not yet fully established into mainstream manufacturing is included to emphasis the on-going development of "next generation" wafer bumping. Not included however is jet plating which is less production oriented and more appropriate for bumping low I/O count devices, e.g., WLP and BGAs requiring bumps larger than 200μm.

A key attribute taken into consideration in the comparison is the ability to consistently produce and maintain critical bump properties, namely, precise and uniform metallurgical composition and physical dimensions, i.e., diameter and pitch

over the entire wafer. Thus any process which uses available bulk solder as the bump sort is preferred for controlling bump composition as is the case for both stencil printing and the C-4NP processes. Of these two, however the C-4NP process would appear to offer inherently better dimensional consistency and control.

Table 10-3. Comparing Wafer Bumping Processes

Process	Evaporation (C-4)	Plating Electrolytic/ENIG#	Stencil/ Template Printing	C4NP
Process Cost	1	3/5	4/5	5
Throughput (wafers/hr.)	1	3/4	5/5	5
Useable Solder Alloys	2	3/1	5/5	5
Tooling Cost: Equipment and Fixtures	1	3/5	4/4	1
Bump Size/Pitch Limitations	1	4/1	1/3	5
Process Complexity	1	3/5	4/5	5
Wafer Yield*	1	4/3	3/4	5
Reliability Potential**	4	4/3	4/4	5
Technical Support	1	2/2	3/3	5
Infrastructure in Place	3	5/4	5/3	1
Proven in Manufacturing	5	4/4	5/5	1 (TBD)
Environmental Concerns	4	3/3	3/3	5

Rating: (1) Least Favorable => (5) Most Favorable
* Related to Bump Size and Pitch | ** Overall Quality of the Bump

10.5 — Polymer/Bumps [27]

Polymeric materials, both epoxies and elastomers, are used as bump materials for several niche applications where solder is prohibitive because of temperature limitation imposed by the materials involved or the lack of solderable metals. Another consideration to be taken into account for selecting a polymer as the bump material is the cost factor.

10.5.1 — Conductive Epoxy Bumps

For flip chip, isotropic conductive epoxy (Ag filled) paste is stencil printed and deposited directly over the die bond pads while devices are still in wafer format. When deposited directly onto the Al however, a high contact resistance develops over time after curing and subsequent assembly, necessitating the addition of a UBM, typically ENIG. A stencil printed conductive epoxy bump is shown in Figure 10-16).

(Courtesy Flip Chips. Com)

Figure 10-16. Stencil Printed Conductive Epoxy Bump (75µm)

Because it is a stencil printing process the same limitations exist, namely, bump pitch of 150–200µm or greater. Additionally, the typical epoxy bump lacks the electrical and thermal conductivity compared to metal bumps and therefore is not appropriate for high performance devices. The conductive epoxy bumps are favored for low-end product applications such as calculators, watches, and smart cards.

10.5.2 — Elastomeric Bumps [28]

There is a considerable difference with elastomeric bumps. An elastomer has the unique property of readily absorbing an applied force by deforming or "stretching" but returning to its original shape upon removal of the force. This resiliency is in all directions x, y and z. A WLP process, called ELASTec®, developed and now in production at Infineon Technologies, utilizes a "soft" silicone material as a non-conductive elastomeric bump and includes it as part of the insulating layer in the pad redistribution process. Following patterning the insulating layer, the elastomeric bumps are deposited by either stencil printing or by spin coating and photolithographic patterning. The photo-patterned bumps use a photosensitive silicone. Bumps range from 25 to 175µm in height.

The redistribution metallization (Ti/Cu/Ni/Au) is deposited and patterned onto the insulating layer and the bumps. Figure 10-17 shows the patterned redistribution metallization and an array of relocated bumps. A close-up of a single bump is also included.

There are several aspects of ELASTec® packaging that are significant. Because of the resiliency of the bump in the z direction, electrical probe testing and burn-in can be more readily accomplished. The needle-like probes, used in wafer electrical testing are replaced by Au plated flat pads. This arrangement eliminates damage to the bumps and simplifies burn-in. This has significant relevance to the development of a Wafer Level Test and Burn-in technology.

In addition, resiliency in x and y direction provides for stress relief for packages assembled to PWBs subjected to thermo-mechanical forces (temperature or power cycling). By compensating for the mismatch in CTE between the die and the board (3 ppm vs. 18–29 ppm respectively) no underfill (discussed in Chapter 11) is needed.

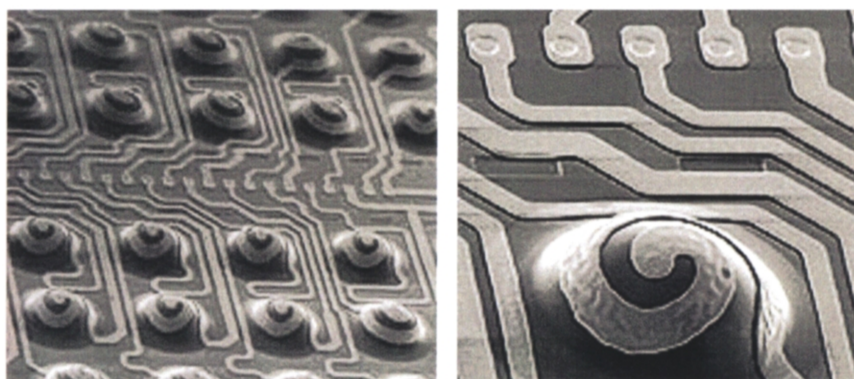


Figure 10-17. Elastomeric Bumps [28]

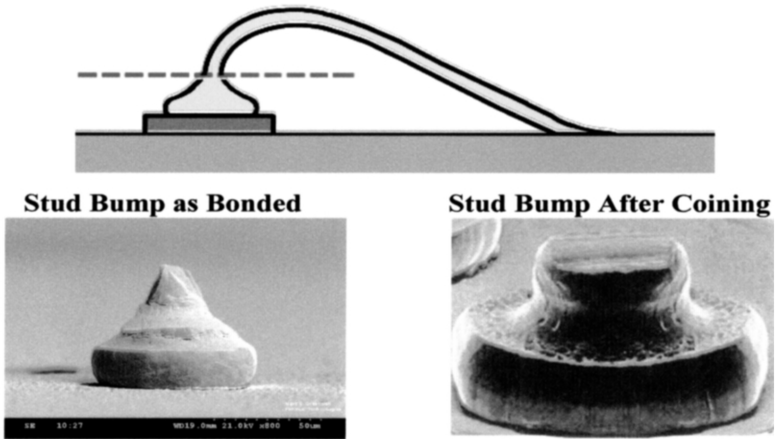
10.6 — Stud/Ball Bumping [29,30]

Bumping in wafer format is now well established with many dedicated bumping service providers available within the industry. This service however is not accommodating to the many low volume component manufactures (hybrid circuits and MCPs) who would like to use flip chip to take advantage of the many significant attributes offered by the technology. Typically the low volume requirements mean a single wafer is usually more than adequate for the quantity of devices needed. The problem is primarily one of availability and the excessive cost incurred for bumping a single wafer.

A solution arrived in the early 1980s with the emergence of stud or ball bumping. It was aimed primarily at elimination of the need for wafers altogether and allow bumping of readily available singulated die. Using a conventional wire ball bonder, the bump is formed by cutting the wire immediately after the actual ball bond has been made. The bumps function as standoffs allowing the singulated die to be flip chip attached to a package or substrate. While Cu, and to a much lesser degree solder, can be processed, Au stud bumps are currently the most commonly used for flip chip assembly. SEMs of a Au stud bump "as bonded" and after "coining" are shown in Figure 10-18. The "coining" operation levels the top of the bump and provides for a flatter surface and an increased bonding area.

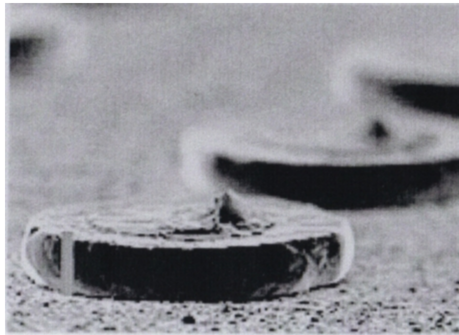
Growing interest in use of stud bumping has precipitated further development of stud bumping processes. Responding to this interest wire bonder manufacturers now offer equipment designed specifically for ball bumping featuring wafer level capability. Added features include "as bonded" bumps that do not require coining (Figure 10-19).

Figure 10-20, for example, highlights the versatility of the technology as well, including the stacking of bumps to provide for increase standoff and "gap height" and the bumping of area array device I/O format. It should be obvious that if a device can be wire ball bonded it can also be stud bumped which extends the technology into high I/O count fine pitch devices.



(Courtesy Palomar Technologies)

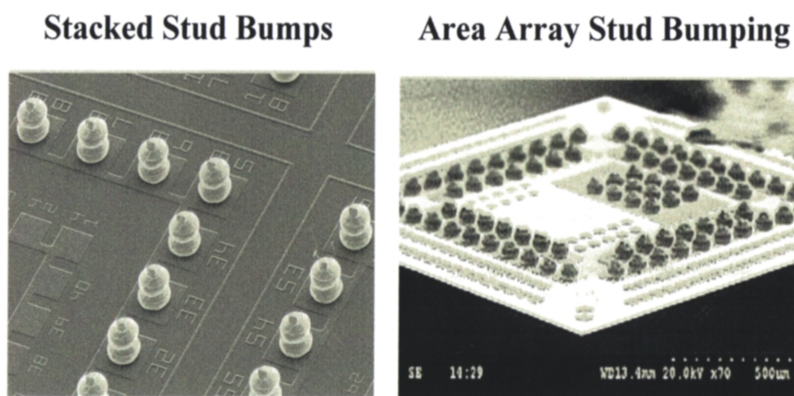
Figure 10-18. Au Stud Bumps as Bonded and After Coining



(Courtesy Palomar Technologies)

Figure 10-19. Coined Stud Bumps As Bonded

Stud bumping early on was considered a temporary solution to assist in developing the necessary engineering base prior to flip chip implementation. This would then be followed by transition to a wafer bumping technology for volume production. There has been, however, a significant number of applications in which stud bumping has proven to be a more viable alternative and a highly reliable technology. Further impetus is provided by the availability of dedicated ball bumping bonder equipment supporting wafer level stud bumping in a high volume environment if required.



(Courtesy Kulicke and Soffa)

Figure 10-20. Stacked and Area Array Stud Bumps

10.7 — Trends in Bumping Technology [31]

The International Roadmap for Semiconductors 2003 indicates continuing increases in IC I/O counts, reaching in excess of 4000 in 2010, greater than 6000 in 2015 and 8500 in 2018 for the high-performance devices. To accommodate these levels the bump size and pitch will need to decrease accordingly. ITRS indicates bump pitch over the same timeframe going from the current 150–200μm to 75μm. With decreasing pitch there is a corresponding decrease in bump height and width. Thus, for current 200um bumps the typical bump height is 100μm and width 125μm. For bump pitch less than 125μm, the corresponding bump height and width will be less than 75μm and 100μm respectively.

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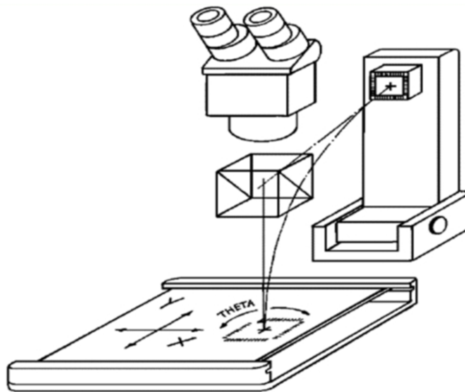
11 Flip Chip Assembly

11 — BASIC FLIP CHIP ASSEMBLY [1–4]

Flip chip device assembly entails three basic steps: a die pick-up, an alignment and placement to the package/substrate footprint, and a final attachment or bonding step. For pick-up, die can be presented in various carriers much the same as those used for chip and wire assembly including waffle packs, GelPak ™, a reel tape or a sawed wafer mounted on a film frame. The die can be either face-up or facedown. If face-up the die must be picked and "flipped" for alignment and placement.

For attachment, the face-down die must be aligned (bumps to pads) with the corresponding footprint on the package/substrate. The alignment, in a manual mode, is achieved by simultaneously viewing the bumped side of the die and the package "footprint". An operator manipulates the die in x, y, and theta to achieve proper alignment. Figure 11-1 graphically illustrates the alignment of a flip chip using a bi-directional mirror to simultaneously view both the die and package footprint.



(Courtesy FINETECH GmbH & Co.)

Figure 11-1. (right) Manual Flip Chip Aligner Bonder; (left) Schematic of Bi-directional Viewing of Die and Package/Substrate Footprint

For fully automated operation optical pattern recognition is added for the alignment to eliminate operator dependence and realize complete machine control insuring precise placement accuracy and repeatability.

Some force may be required for placement of the die. The amount of force will depend upon the bump metallurgy and the attachment process. For example, when there are multiple die involved and there is a "batch" or mass bonding, as is the case for solder bumps, near-zero force is required for placement.

For bonding involving non-collapsible bumps, the amount of pressure to be applied must be sufficient to provide positive contact of the bump to the metallized footprint pad. The amount of force applied can range from a few grams to over 100 grams per bump to complete the bonding.

11.1 — Flip Chip Bonding Processes [5–8]

Flip chip bonding processes include:

- Solder Reflow
- Theromocompression (TC) bonding
- Ultrasonic (US) bonding
- Thermosonic (TC/US) bonding, and
- Adhesive attachment

The solder reflow process is clearly the most dominant flip chip assembly process. The other methods involve devices with non-collapsible bumps and require dedicated equipment, namely a Flip Chip Aligner Bonder, for accomplishing "picking, aligning, placement and bonding" of the die. These bonding processes are usually "non-batch" processes and for the most part are used in niche type applications.

Choosing the right process will generally be dictated by the following:

- Flip chip die availability,
- Reliability requirements dictated by the end product,
- Bump metallurgy,
- The package/substrate materials,
- Major equipment needs, and
- Associated costs factors.

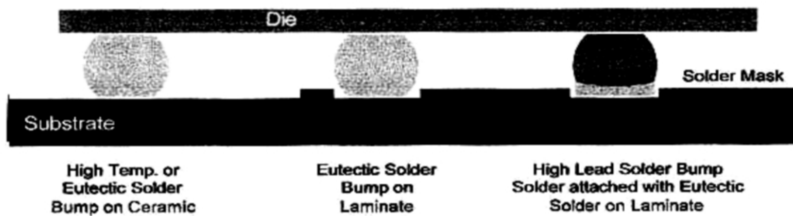
Today, many ICs, in particular high performance microprocessors, ASICs and DSPs, are designed and manufactured as solder bumped flip chip. The majority of devices however, are not readily available in flip chip format and therefore the selection process is at the discretion of the user who must then take into consideration all of the remaining factors listed above.

In the decision making, reliability of the end product should be an over riding consideration. For example, a *high-reliability* military product would most likely call for solder bumped flip chip and a cofired ceramic hermetic package. On the other hand, a smart card or PC card, which will be subjected to a less severe and less critical operational environment, would use an organic substrate or flex circuit and an adhesive for attachment of stud bumped die.

11.2 — The Solder Reflow Process

Solder reflow process options are dictated by the bump and the package/substrate materials. Direct bonding of high lead alloy bumps (C-4), for example, is restricted to ceramic substrate packages because of the high reflow temperatures (>350° C) required. The ceramic package obviously allows for direct bonding with eutectic alloy bumps as well. The same eutectic bumps with lower reflow temperature (approximately 200° C) can also be attached directly to a laminate (organic) board. High lead bumps can also be attached to the laminate substrate by using a stencil printed eutectic solder paste on the board or using a tin capped bump. See the illustration in Figure 11-2.

As with most solder operations, a flux is used to improve the solder wetting Figure 11-3 graphically presents a typical flip chip solder process. The flux can be applied as shown, by dipping the bumps into the flux or by dispensing flux directly onto the package or board. However, when high lead or Cu bumps are attached to a laminate board, a eutectic solder paste containing flux is usually stencil printed selectively onto the footprint pads on the board. The flip chip assembly is completed by application of an underfill that fills the gap between die and package.



(Ref. JIS J-STD-0121 IPC 01/96)

Figure 11-2. Solder Reflow Options

11.2.1 — Advantages of Solder Reflow for Flip Chip Assembly

Flip chip bumps are routinely 75 to 125 micron (3 to 5 mils) bump diameter compared to 250 (10 mils) and 750 (30 mils) for CSP and BGA respectively. The smaller the bump the greater the placement accuracy (die bumps to substrate pads) required for successful attachment. Flip chip therefore should require greater placement accuracy. However, as with any solder reflow process there is a "self-alignment" feature. During reflow, with the solder in the liquidus state, surface tension forces exerted by the molten solder will cause a misaligned die to routinely reposition itself and end up perfectly aligned with the package/substrate pads. This "self alignment" is illustrated in Figure 11-4. The significance of self-alignment is that solder bumped die can tolerate a misalignment by as much as 25% to 50% of the bump diameter and yet be perfectly aligned following reflow.

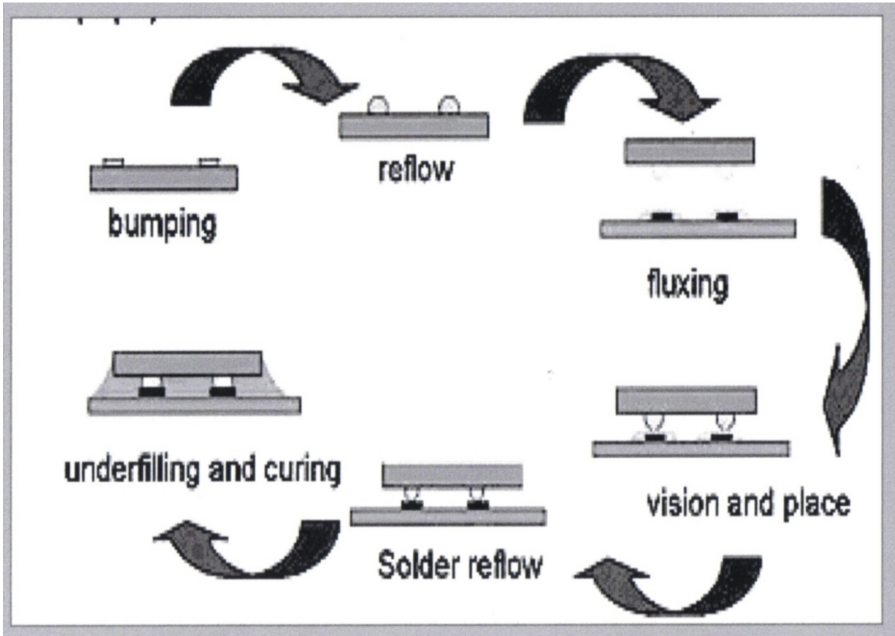


Figure 11-3. Flip Chip Solder Reflow Process [5]

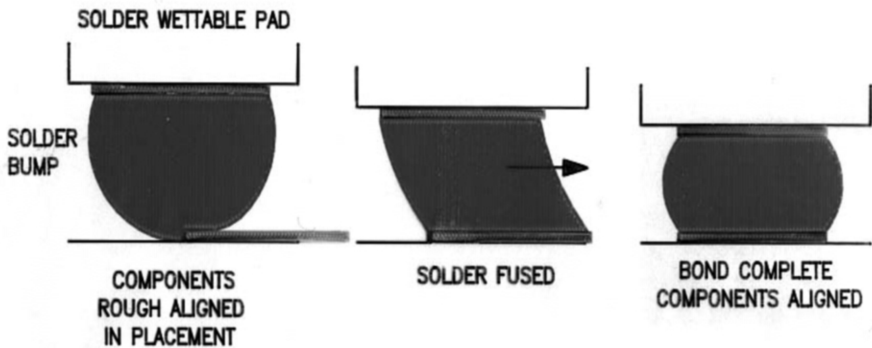
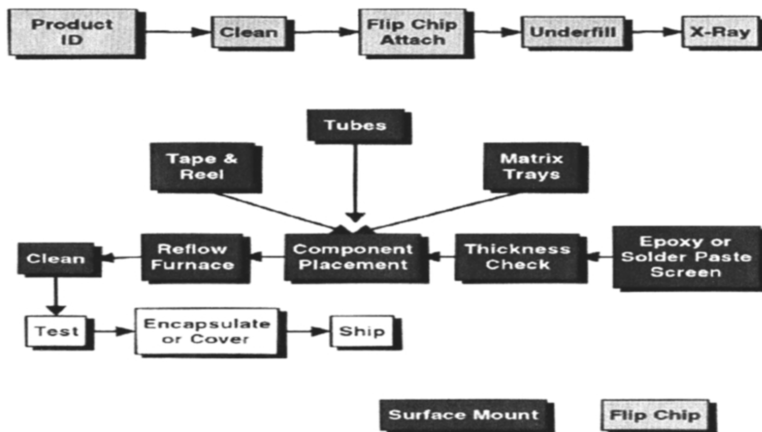


Figure 11-4. Solder Reflow and Self-Alignment

Solder reflow, because of self-alignment, basically involves a "pick—place—reflow" of the die. The process allows for multiple parts to be attached to a substrate and reflowed when fully populated. Flux, used to enhance soldering, serves as glue effectively holding the die in place following placement prior to the reflow. Solder reflow is therefore a batch process with all devices flip chip bonded in a single step. The "self-alignment" feature, in turn, has enabled many existing SMT assembly platforms (basic SMT component pick and place equipment) to be used for flip chip

assembly and usually with little or no modifications. Figure 11-5 shows a flow chart for a production line combining SMT and flip chip assembly.

The flip chip solder reflow process is clearly compatible with mainstream SMT processes and in some instances transparent to existing manufacturing lines. This compatibility contributes to an inherent manufacturing scenario favoring high volumes, high yields, and low cost.



(Courtesy Teledyn Microelectronics)

Figure 11-5. SMT/Flip Chip Assembly

11.3 — Flip Chip Solder Joint Reliability [9–13]

Reliability concerns of solder bumped flip chip solder are similar in many respects to any solder attached component. There are however, mitigating differences. Failure mechanisms have been identified for flip chip assemblies resulting from thermal, mechanical and electrical stresses and device operating environments.

Critical factors affecting the reliability of a soldered flip chip assembly include:

- The die—the larger the die the greater the susceptibility to solder fatigue.
- Bump size—the larger the bump the greater the survivability under stress. Larger bumps at the same time, provide improved current carrying characteristics with reduced incidence of electromigration failures. Additionally, assembly, cleaning, and underfill processes are all enhanced.
- Bump metallurgy—high lead alloys and alloys containing indium have higher survivability than eutectic and "no-lead" solders. Lead-free solders, however, perform better in harsh environments.
- The package/substrate material properties, the design and structure.

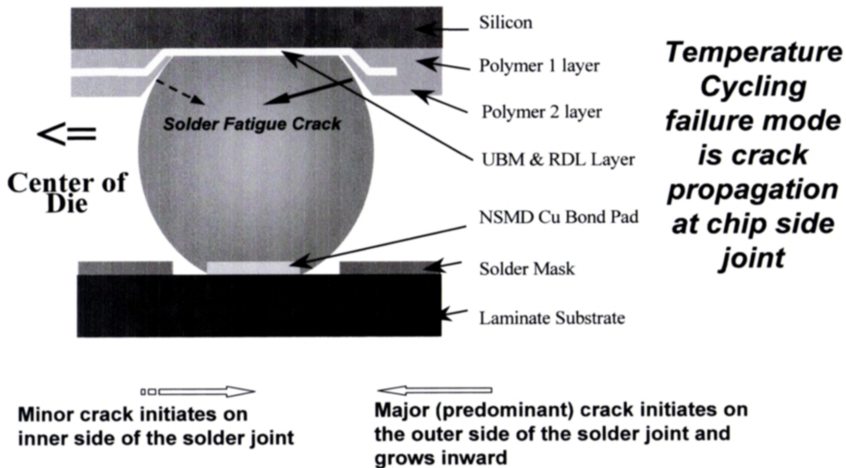
It is not always possible to fully address all these factors. Little can be done with regard to die size. Larger bumps on the other hand are possible depending upon I/O pad size and pitch and are available with WL-CSP.

Major failure mechanisms affecting reliability of flip chip assemblies include:

- Solder Fatigue
- Intermetallic Compound Formation (ICM)
- Electromigration/UBM Consumption
- Corrosion
- Silicon Cratering

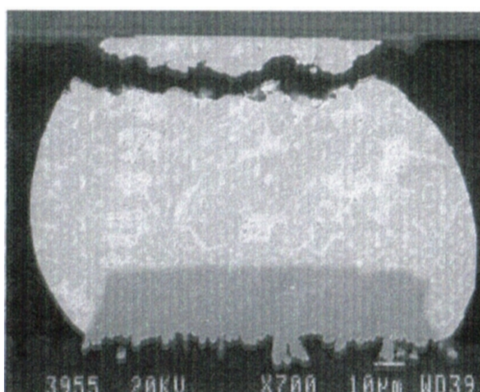
11.3.1 — Solder Fatigue

Solder fatigue is the most common failure mechanism encountered and of major concern with flip chip assemblies. It occurs when solder joints are subjected to thermo-mechanical stress. Because of the mismatch in CTE between the die and the package/substrate, cracks are generated within the solder along grain boundaries close to the bump-die pad interface. The cracks are observed initially at the edge of the bump-die pad interface. With continuing stress a crack will propagate and eventually result in complete separation causing an electrical open and a functional device failure. Figure 11-6(a) is a schematic illustrating solder fatigue for an FCOB application. Figure 11-6(b) is a metallurgical cross-section of a solder fatigue failure after thermal cycle testing.



(Courtesy Flip Chip International)

Figure 11-6(a). Schematic of a FCOB Solder Joint Fatigue Failure



(Courtesy Flip Chip International)

Figure 11-6(b). Metallurgical Cross-Section of Solder Fatigue Cracking in Eutectic SnPb

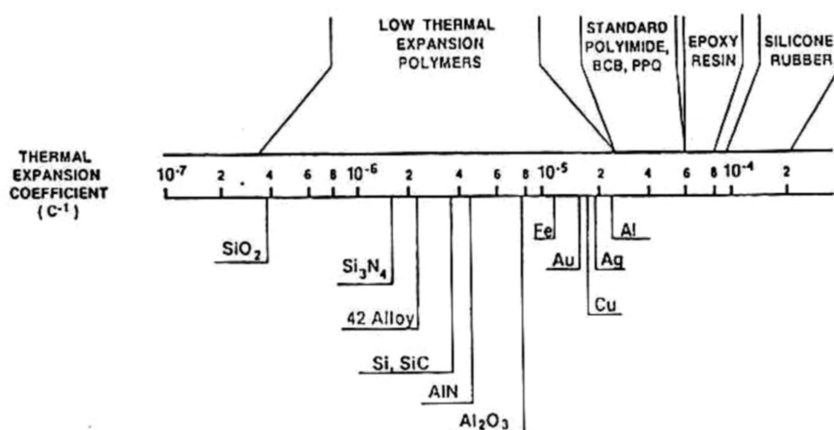


Figure 11-7. CTE Values for Various Microelectronic Packaging Materials

CTE values for many of the materials employed in microelectronic packaging are presented in Figure 11-7.

The silicon die with a CTE of roughly 3.5 x 10–6 per degree C (read as 3.5 ppm) die is mismatched to most common package/substrate material such as organics, (FR4, CTE at 12–18 ppm), as well as ceramics (alumina, CTE ~7.5 ppm). The larger the difference in CTE the greater will be the susceptibility to solder fatigue failure under thermo-mechanical stress. Arguably then, a worse case scenario is realized with flip chip on board applications with an assembly structure as illustrated in Figure 11-6.

Table 11-1 lists the properties of the most common organic substrates.

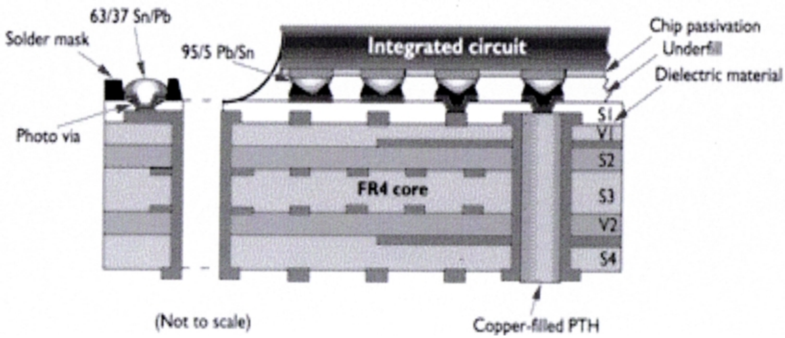


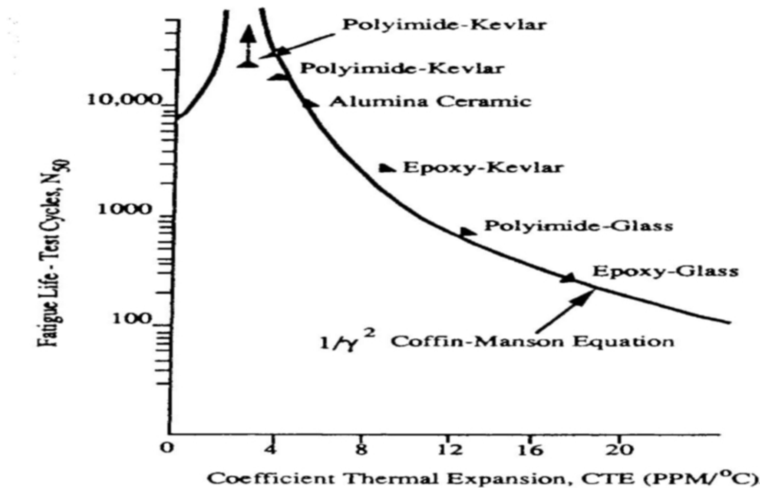
Figure 11-8. Flip Chip Assembly on Organic Substrate (FCOB)

Table 11-1. Materials Properties of Some Organic Substrates

Material	Dielectric Constant	Dissipation Factor	Prop Delay (ps/inch)	CTE, X,Y (ppm)	CTE, Z (ppm)	Tg (°C)	Moisture Uptake (%)
FR4	4.8			16		125	
	3.9–4.4		168			180	0.04–0.2
	4.3			13–18		135	0.1
	4.8	0.022		12–16	80		
BT Epoxy	4.2			14		180	
	4.0		170			195	0.40
	4.3			15–16			0.05
Polyimide	4.5			13		250	
	4.3		173			230	0.35
	4.2			10–14		250	0.35
	4.5	0.01		12–14	60		
Cyanate Ester	4.5			15		230	
	3.7		163				0.39
	3.6			8–10		230	0.8
PTFE Composite	2.9	0.001		16	24		0.05
	2.6–2.8	0.003		17	50		0.07
	2.3		140				

Figure 11-9 presents some empirical data relating the effects of package/substrate CTE on survivability, i.e., Fatigue Life, when subjected to temperature cycling 0° C to 100° C. The list includes aluminum oxide ceramic and several organic substrates. The most popular organic substrates, epoxy-glass (delta

CTE = 6x) and FR-4 (delta CTE = 4x) both fail at less than 1000 cycles, whereas, ceramic (alumina, delta CTE = 2x) survives 10,000 cycles.



(Courtesy IBM Corp.)

Figure 11-9. Fatigue Life vs. Substrate CTE; TC/ 0–100ºC

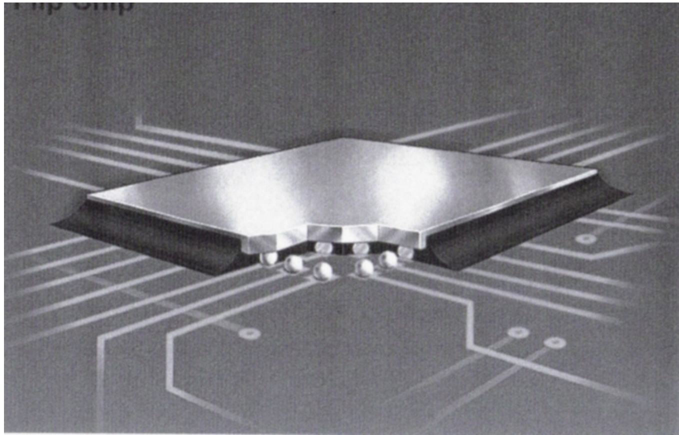
11.3.1.1 — Addressing Solder Fatigue

The PWB is the most widely used second level interconnect and critical to realizing reliable electronic assemblies. With the many advantages offered by FCOB an extended and enhanced fatigue life is essential. This infers achieving the same level of reliability or survivability obtained with packaged components.

11.3.1.2 — Flip Chip Encapsulation/Underfill [14–16]

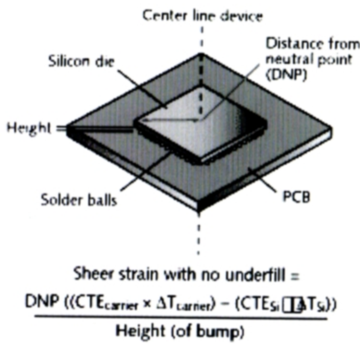
It has been found that use of an encapsulant or "underfill". typically an epoxy material, will significantly enhance the fatigue life of FCOB. The encapsulant basically fills the space between the die and the package, as shown graphically in Figure 11-10. The underfill, with a CTE close to that of the substrate effectively "locks" the die to the package/substrate, thereby distributing the strain uniformly across the entire chip.

Analysis of solder fatigue failures show that the bumps located the farthest distance from the geometric center of the die experience the greatest strain when subjected to thermo-mechanical stresses such as temperature or power cycling. Thus corner bumps are usually the first to fail. Hence the greater the distance from the die center (larger the die). the shorter the fatigue life. Figure 11-11(a) illustrates the DNP or distance from neutral point, while Figure 11-11(b) shows the Von Mises strain on each bump, referenced to the DNP, with and without underfill. The effectiveness of the underfill in distributing the stress over the entire die is presented in Figure 11-12 using Micro Moire Pattern analysis.



(Courtesy Henkel Corp.)

Figure 11-10. Flip Chip with Underfill



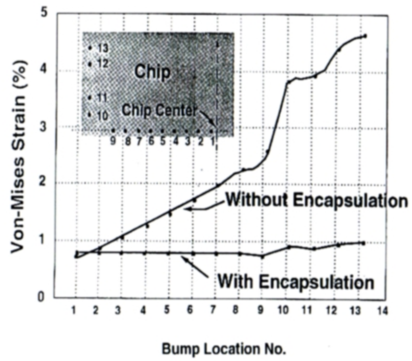
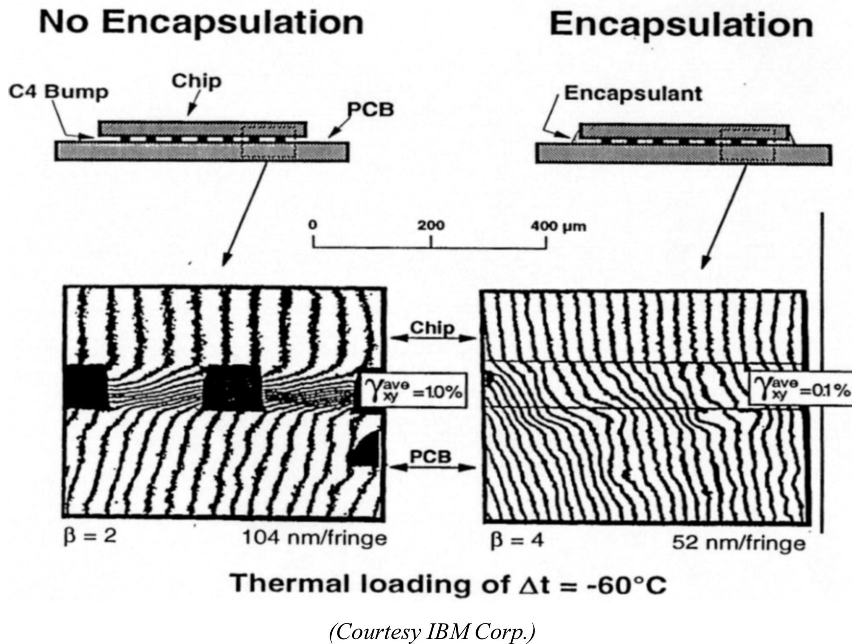


Figure 11-11. (a) Distance From Neutral Point (DNP);
(b) Von-Mises Strain at Each Bump Location with/without Underfill (IBM)

11.3.1.3 — Underfill Processes

Underfill is obviously critical for most FCOB applications. Unfortunately the underfill also presents some difficulties in high volume production because of the processes involved in both the actual application and the subsequent curing. The time required to deposit the material and allow full flow of the underfill under the die as well as the curing process are time consuming creating a "bottleneck" to high volume production flow.



(Courtesy IBM Corp.)

Figure 11-12. Micro Moire Pattern Analysis of FCOB With/Without Underfill

The most common method of applying underfill is by dispensing, as illustrated in Figure 11-13(a). Deposited along the edge of the die the underfill flows under the die by capillary action. Critical factors associated with this process, as with all the underfill processes, include:

- The material itself, in particular, flow properties
- Cleanliness of assembly
- Gap height—the larger the bumps the higher the gap, and
- Bump pitch—the greater the pitch the easier the flow of underfill

New materials as well as alternative application processes are continually being developed and introduced to address these problems. Of note is the use of a flux containing epoxy applied by dispensing or stencil printing onto the substrate prior to placement of the die. This "no flow" (no clean) process is shown schematically in Figure 11-13(b). This process not only reduces the number of process steps but also allows for the option of electrically testing the die before reflow bonding. Another option would involve applying the epoxy directly to the wafer rather than the substrate.

Formulating the "no flow fluxing" material is critical. A filler is used to tailor the CTE of the underfill, ideally to that of the substrate. But it is without problems. Increased placement force may be necessary to insure more positive contact with the UBM prior to reflow. And, too much filler can impede the solder flow at liquidus resulting in a reduction in "self-alignment" and potentially poor solder joints.

Reduction in “self-alignment” means greater die placement accuracy is required and increased process cycle time. Eliminating the filler altogether however results in a higher than desired CTE and problems with delamination at the substrate interface.

Figure 11-13(c) schematically describes application of an underfill applied at the wafer level. The underfill processes shown in Figure 11-13(b) and (c) both offer the advantage of an improved production flow.

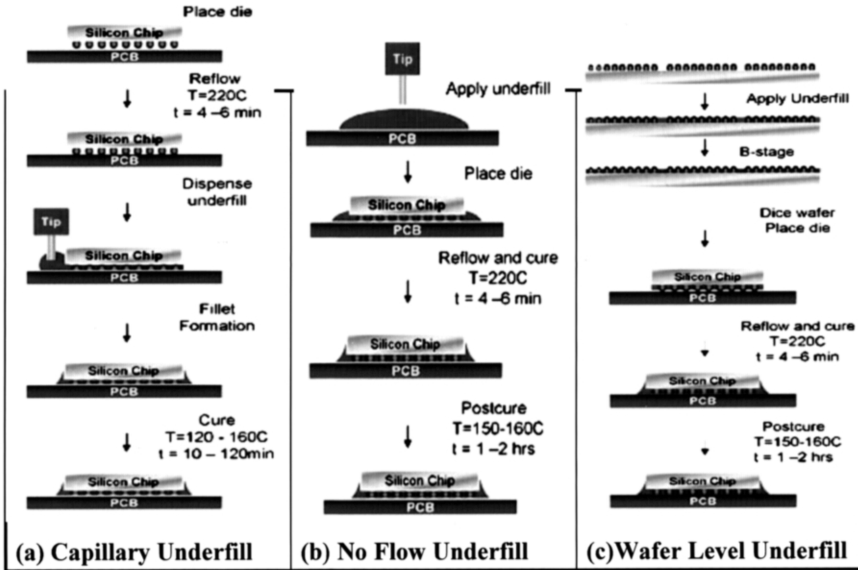


Figure 11-13. (a) Underfill Dispensing and Capillary Flow; (b) No Flow Underfill; (c) Wafer Level Underfill Process [16]

All underfill processes work best with large bumps and bump pitch. Application of underfill is therefore more challenging with flip chip tan with WLPs.

While the underfill effectively enhances fatigue life for solder attached flip chip for both lead containing and lead-free solders, it also can bring with it its own reliability problems. For example, underfill related problems include package/ substrate warpage, delamination and voiding. Warpage takes place as a result of the epoxy material, the curing temperature, assembly processes and the device operating temperature. Low cure temperatures, fast curing time and a high glass transition temperature with low moisture absorption are themost desirable properties. Delamination is the result of poor adhesion of the underfill caused by improper prior cleaning and the application and curing processes. Voiding results from the flow properties of the underfill and the method of application, the die size and bump layout, i.e., peripheral or area array, bump height and pitch.

The best solution lies in the use of silicon as a package/substrate. This approach brings with it many other benefits since silicon is also amenable to embedding of both active and passive devices that add significant enhancements to SiP and SoP future designs and applications.

11.3.2 — Intermetallic Compounds (IMC) /UBM Consumption [17–19]

Intermetallic compound formation results from the interdiffusion of metals that make up the UBM and the solder bump. The initial layer of IMC is essential to the attachment process and the forming of a metallurgical bond between the solder bump and the UBM. However, when a flip chip is exposed to high temperatures for extended periods of time, e.g., the solder reflow assembly process, or the particular end product application, the IMC layer initially formed increases in thickness. This increase is associated with a decrease in thickness of the UBM. The consumption of the UBM and the increase in thickness of the IMC create high resistance contacts and because of the inherent brittleness can result in electrical opens. To minimize the adverse effects of IMC formation, the metallurgies of both the UBM and the solder bump must be carefully selected. Compatible UBM/Bump compositions are presented in Chapter 10, Table 11-2. Because the IMC formation basically involves both Cu from the UBM and Sn from the bump solder it has been found that addition of small amounts of Cu (<1.0%) to eutectic SnPb results in significant reduction in dissolution of the UBM and an enhanced reliability. Eutectic SnPb for example, fails rapidly at temperatures above 140ºC, whereas a near eutectic SnPbCu has been shown to survive 3000 hrs HTS at 150ºC.

11.3.3 — Electromigration

Electromigration is the physical movement of bump solder as a result of the flow of current, device junction temperature and time. The movement is in the direction of current flow and like IMC results in high contact resistance and/or opens. Reliability screening is High Temperature Operating Life (HTOL), typically 150ºC, at a current density based on the device and the particular conditions to be experienced in the end product application. Once again it is a major concern for automotive applications where both high temperatures and high currents are common. The same SnPbCu near eutectic alloy that limits UBM dissolution also minimizes electromigration and improves reliability by roughly a factor of 3 over SnPb.

11.3.4 — Corrosion

Corrosion is the result of chemical reactions occurring between the UBM and the bump solder. The reaction can result in opens and shorts and can take place during solder bump reflow, solder reflow or during end product operation. When shorts are observed they will typically be the result of dendritic filament formation. These conductive filaments are formed whenever there is present moisture, ionic contaminants and a bias voltage applied to two adjacent conductors. Corrosion failures are more prevalent with Level 2.0 printed circuit board assemblies under end product operating conditions While it does take place on the board, it is more apt to be observed unfortunately, on the die where spacing between lines is significantly smaller.

Corrosion failures can be minimized by eliminations of the accelerants moisture and ionic contamination. Flip Chip underfill while used primarily for enhancing fatigue life of solder bumped flip chip provides an added level of passivation that also limits moisture condensation on the die surface. Ionic contaminants however, must be removed prior to application of underfill. Proper cleaning can readily

remove contaminants and insure better adhesion of the underfill to the die surface and the package/substrate.

Reliability screening for corrosion involves Temperature/Humidity/Bias (HTB) testing.

11.3.5 — Silicon Cratering

Cratering refers to the fracturing or cracking of the silicon directly under the bond pad. The cratering can occur during bumping, flip chip assembly and/or operating life of the device. It is an incipient type of failure mechanism in that it is not always immediately evident. The initial crack is not totally destructive but does become so with time, particularly under device operating life. The end result is an electrical open.

Cratering results primarily from stress and strain in the UBM resulting from the deposition conditions, e.g., sputtering versus ENIG. In sputtering, the stress in the film is dependent upon the UBM deposition parameters. High sputtering rates, for example, result in a more highly stressed film.

Cratering is also a concern in wire bonding occurring most frequently with ultrasonic and thermosonic ball bonding. Hence if stud bumping is employed silicon cratering becomes a greater concern especially if there is an added coining step.

11.4 — Reliability and Lead-Free Solders [20,21]

Currently and with cost as a major driver, the overall packaging scenario favors use organic packages and substrates at Level 1.0 and Level 2.0 respectively with solder reflow flip chip die attachment. Added to this is the inevitable move to lead-free solders replacing the in-place and well understood eutectic SnPb. The lead-free brings with it problems associated primarily with the higher process temperatures required (200–220°C SnPb vs. 240–260°C no-lead) and the detrimental impact on the organic packages/substrates.

However, as discussed, lead-free SnAg(3.5) and SnAg(3.5)Cu(0.6) have been shown to offer improved reliability for applications involving high temperatures and high currents, conditions that are currently encountered with most automotive electronic products and will need to be addressed with future generations of high performance ICs.

Table 11-2 shows relative performance of flip chip on organic of 2 leading lead-free solders and eutectic SnPb on HTS and HTOL screening tests SnPb.

Clearly the lead-free performs better than the eutectic. It is also evident the enhanced reliability that is due the presence of Cu in the solder and further gain in reliability is realized with increase in the Cu content.

Table 11-2. Lead and Lead-Free Solders Performance on HTS and HTOL Reliability Screening [17]

Alloy	Relative Reliability HTS	Relative Reliability HTOL
63SnPb	1	1
Sn-3.5Ag	0	0.8
Sn-3.5Ag-1.0Cu	7	3.7
Sn-3.4Ag-2.0Cu	16	4.8

11.5 — Solder Reflow Attach: Comments, Concerns

The solder reflow is the preferred process for mainstream manufacturing for FCIP and FCOB applications. A key factor in the selection is the compatibility with existing SMT component assembly lines.

Solder reflow process attributes include

- Batch processing offering high volume throughput
- "Self-alignment" providing wide tolerance in die placement
- A "Near zero force" die placement minimizing potential for damage to the device
- With underfill a robust FCOB assembly with enhanced reliability.

Experience with solder reflow FCOB has helped to identify failure mechanisms and enabled reliability requirements to be put in place. Table 11-3 lists the various failure mechanisms for both flip chip and wafer level packages and the industry accepted qualification test methods and test conditions used to insure high quality and reliability.

11.6 — Alternative Flip Chip Bonding Methods [22,23]

Flip chip bonding using thermocompression, thermosonic and ultrasonics will normally use die with non-meltable bumps. The bumps may be plated (Au, NiAu or CuAu) or stud (Au or Cu) bumps. An Aligner Bonder which is basically a modified wire bonder is employed to sequentially pickup the die, align die to "footprint" and finally bond the die. The actual bonding parameters, temperature, force, ultrasonic energy and hold time at bond, are similar to those used in wire bonding.

The process sequence is "pick (face-down)—align—place—bond". It differs from solder reflow in that each die is processed separately rather than in batch. As a result, there is reduced throughput and added manufacturing cost for assembly as well as increased potential for damage associated with the need for application of force and ultrasonic energy to complete the bond.

Applications involving these types of bonding process are very much low volume, niche oriented applications, such as assembly of laser diodes, Saw devices and Focal Plane Arrays.

11.7 — Adhesive Flip Chip Attachment [24,25]

There are several reasons for considering use of adhesives for attachment of flip chip devices

- It is a low temperature process (150 C to 200 C) allowing use of lower cost substrates such as polyesters that cannot tolerate the higher soldering temperatures.
- Adhesives can be used for applications wherein the conductor materials to be contacted are not solderable, e.g., Liquid Crystal Displays.
- With certain adhesive attachment processes the adhesive will serve the dual function of attachment medium and the underfill.
- Totally amenable with stud bumping it offers a cost effective approach to evaluating flip chip prior to committing to implementation into high volume production.
- And finally, adhesive attach is *lead free and environmentally friendly*.

Table 11-3. Reliability Screening Tests for Solder Bumped FC/WLP [12]

	Failure Mechanism	Test Method	Test Condition—FC	Test Condition—WLP
Package Level Specification	N/A	Pre-Ccndition	Bake at 125°—24 hrs, soak per JESD22-A112, then 3 cycles	JEDEC Level 1 and 3
	Solder Fatigue	Thermal Cycle	N/A	-65/150ºC 1000 Cycles
	Corrosion	Autoclave	121ºC, 100% RH, 36psia 96 hrs	121ºC, 2 atm, 100% RH 168 hrs.
	Silicon Cratering	Bump/Die Shear	Constant shear speed, Shear within the solder (no JEDEC Std)	Constant shear speed, shear within the solder (no JEDEC Std)
Board Level Specifications	Solder Fatigue	Thermal Cycle on FR-4 Board	-40/125ºC, 1000 cycles 20 min ramp/10 min dwell	-40/125ºC, 1000 cycles 15 ramp and dwell
	Electro-migration	High Temp Op-Life	mAmps TBD, 1000 hrs, $T_J = 150$ºC	mAmp TBD, 1000 hrs. $T_J = 150$ºC
	Excessive IMC/UBM Consumption	High Temp Storage	150ºC, 1000 hrs.	150ºC 1000 hrs.
	Corrosion	85ºC/85% RH	85ºC/85% RH/5V Bias 1000 hrs.	85ºC/85% RH/5V Bias 1000 hrs.

11.7.1 — Types of Adhesives

Adhesives are available as conductive, either isotropic or anisotropic, and non-conductive or insulating. Conductive adhesives contain filler materials to provide a level of electrical and thermal conductivity. The non-conductive adhesives contain no filler material, and are essentially the same as the adhesives used for die bonding. The anisotropic adhesives, however, are unique and specially formulated to provide conduction in the z-direction only and are therefore referred to as z-axis adhesives.

11.7.2 — Isotropic Conductive Adhesive (ICA) Attach

Isotropic adhesives conduct in all directions x, y, and z, and are available as a paste for application by "dipping" or stencil printing and as preforms. The conductive paste adhesive can be stencil printed onto to the substrate or the bumps can be dipped after pick up prior to the alignment/placement. The stencil printing and dispensing of the epoxy must be selective, that is, the ICA must be deposited only on the substrate bond pads. Like the reflow process. all die can be placed prior to the final cure. The attachment is completed upon the batch curing of the epoxy. While isotropic conductive adhesive attach process allows batch processing there is no self-alignment of the die and as a consequence placement accuracy is radically more critical. Typically, placement accuracy of 10 to 20% of the die bump diameter is called for. Machine assisted (a flip chip-aligner bonder) alignment for each die is necessary to achieve this tighter tolerance (~ 10 to 12μm) placement. As with the solder reflow process assembly platforms with optical recognition are used where alignment accuracy (<<10μm) is critical. The isotropic adhesive attach process is shown graphically in Figure 11-14. Again, like the solder process, underfill may be required to add robustness to the assembly and to enhance reliability.

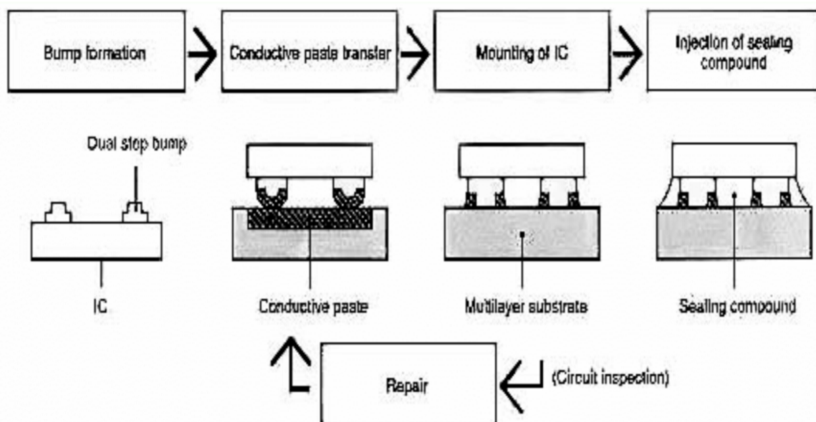
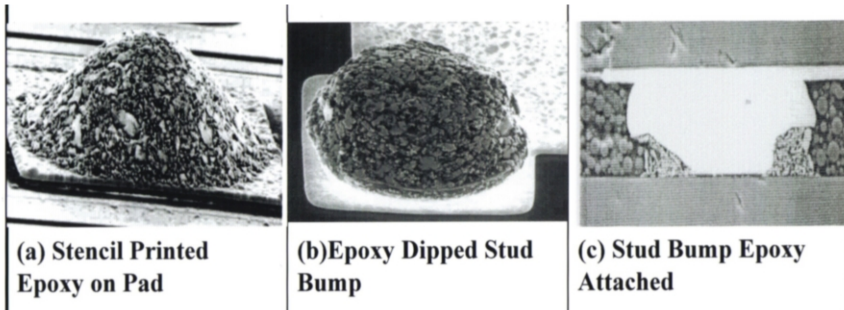


Figure 11-14. Flip Chip Isotropic Adhesive Attachment

Figure 11-15(a) shows a stencil printed epoxy adhesive on a substrate pad, Figure 11-15(b) a stud bump with epoxy dipped isotropic adhesive and Figure 11-15(c) a cross-section of an isotropic adhesive attached bump.



(Courtesy Flip Chips.Com)

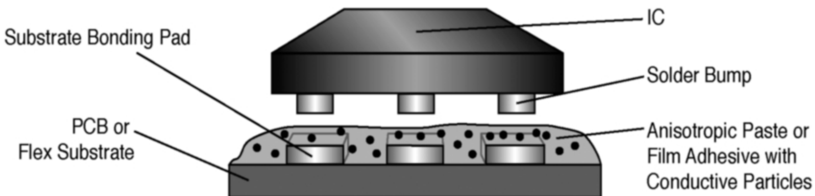
Figure 11-15. (a) Stencil Printed Epoxy; (b) Epoxy Dipped Stud Bump; (c) Cross-section Isotropic Epoxy Attached

11.7.3 — Anisotropic Adhesive Attach

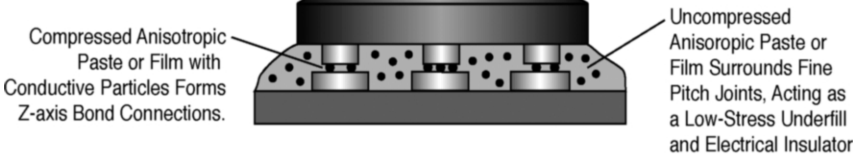
The anisotropic conductive adhesive (ACA) or z-axis adhesive is a thermoset or thermoplastic material. The ACA contains a very stable matrix of metallized beads (glass or polymer). The beads are typically 3–5 microns in diameter nickel and gold plated then coated with a final insulating layer. The beads are dispensed such that there is absolute minimal contact in the x and y directions. To achieve attachment using ACA, the adhesive is first deposited by dispensing, stencil printing, or as a film or perform, completely covering the substrate "footprint" area.

Key features of the material and the process are illustrated in Figure 11-16.

Before Cure . . .



After Cure . . .
(Hear and Low Pressure)



(Courtesy Hitachi Chemical Co, America Ltd.)

Figure 11-16. Anisotropic Conductive Adhesive Attach

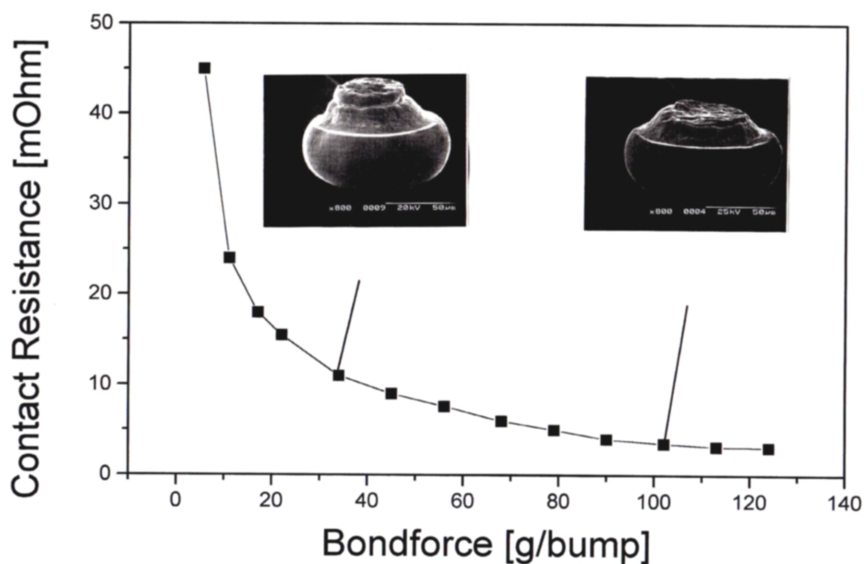
Because placement accuracy is critical a flip chip aligner bonder is used to pick the die, align, and place with sufficient force to compress the adhesive and cause the conductive particles to make contact between the die bumps and the substrate bond pads,creating the necessary conductive path from the die to the substrate. Curing the adhesive is achieved at approximately 150 to 200° C, while maintaining pressure on the die.

Because the electrical conductivity will depend upon the density of conductive beads contacted, the bumps must be aligned such that the compression of the adhesive occurs totally within the area of the substrate pad. This can be enhanced by making the bump and the substrate pad as large as possible, e.g., coining of stud bumps, and by having a die placement accuracy of approximately 10% of the bump diameter. With decreasing bond pad size and pitch, placement accuracy becomes even more critical.

A significant attribute of the anisotropic adhesive process is that the adhesive remains in-place after curing negating the need for a separate underfill step.

11.7.4 — Non-Conductive Adhesive (NCA) Attach

The non-conductive adhesive attach process is similar to the anisotropic except the adhesive, contains no filler. Again an aligner bonder is required for picking, aligning, placement and attachment. In this case however the lowest contact resistance is dependent upon the bump physically contacting the pad metal. Thus the force required to achieve attachment is much higher. Figure 11-17 shows the effect of bonding force on the resulting contact resistance.



(Courtesy Fraunhofer IZM)

Figure 11-17. Non-conductive Adhesive FC Bonding Contact Resistance vs. Applied Force

Curing again requires temperature and continued application of a force. When cured the adhesive actually provides an intrinsic compressive force that enhances the contact between the die and the substrate. As with the anisotropic adhesives the non-conductive adhesive acts as the underfill. It is also the least costly of all the adhesives processes.

11.7.5 — Adhesive Attach Summary/Concerns

From a production viewpoint, use of an isotropic adhesive offers the potential for the highest throughput. The anisotropic and non-conductive adhesive processes are hampered by lower throughputs, attributable to greater placement accuracy, and a time consuming curing step that requires maintaining both the temperature and a compressive force to complete the attachment. On the other hand, the need for the added step for underfilling is eliminated.

A variation in processing of anisotropic and non-conductive that reduces the production cycle is an option. It involves reducing total process time by changing to a two-step semi-batch process. Similar to the isotropic process, deposition of the adhesive is followed by alignment and placement of the die into the adhesive briefly applying pressure and temperature sufficient to B-stage the adhesive. This is repeated for each die. A fully populated substrate is then subjected to a final “batch curing” which includes a final application of temperature and pressure to complete the attachment process. While not capable of the same level of throughput the trade-off in eliminating the underfill process must be taken into consideration in evaluating the various adhesives processes.

11.8 — Adhesive Bumps [26,27]

A process for flip chip attachment using adhesive (polymer) bumps was introduced by Polymer Flip Chip, Inc. The same adhesive is used for attachment of the bump to the package/substrate. The adhesive for both bump and substrate is an isotopic conductive paste formulation. Because of a reaction between the adhesive bump and the aluminum pad, an electroless Ni-immersion Au UBM is required. Bumps and substrate adhesive are both deposited by stencil printing. While in wafer format, bumps are stencil printed directly over Ni-Au plated aluminum bond pads and cured. The actual assembly and attachment process is the same as adhesive attachment with stud bumps.

The process is as follows:

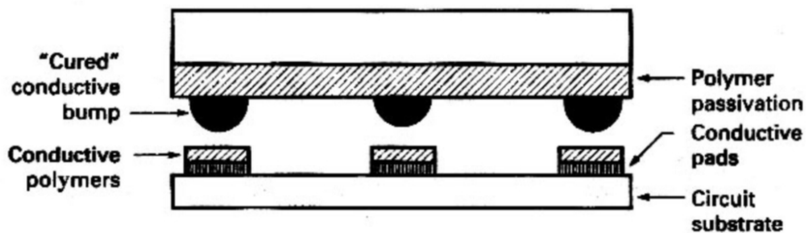
Wafer process:

- Clean device wafer and electroless Ni-immersion Au plate UBM
- Deposit polyimide passivation layer by stencil printing, exposing only the die bond pads
- Stencil print conductive adhesive bump over UBM and cure
- Mount wafer on film and separate individual devices by sawing

Assembly process:

- Stencil print conductive adhesive selectively on substrate "footprint" pads
- Assemble devices to substrate
- When fully populated cure substrate adhesive to complete attachment

The resulting structure is shown schematically in Figure 11-18.



(Courtesy Polymer Assembly Yechnology, Inc.)

Figure 11-18. Conductive Polymer Bumps and Attachment

11.9 — Summary: Advantages of Flip Chip as a First Level Interconnect

Flip chip along with WLPs are rapidly moving into mainstream manufacturing. Both are area array packages offering high packaging efficiency, high density, and a high volume cost-effective assembly process. As a Level 1.0 technology, it more than adequately addresses increasing I/Os and is a significant contributor to "smaller, better, cheaper" end product.

Flip chip and LP attributes include:

- Totally accommodating to high I/O count and I/O formats,
- A true die-size "package"—high packaging efficiency,
- If solder attached "Self Alignment",
- Offers improved overall performance—low inductance leads,
- With underfill, enhanced reliability, and
- A robust, low profile assembly,
- Minimum footprint for attachment—high density Level 2.0 Packaging,
- Fully supports end product requirements for "smaller, better, cheaper".

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12 HDI Substrate Manufacturing Technologies: Thin Film Technology

12 — HIGH DENSITY PACKAGE/SUBSTRATE MANUFACTURING TECHNOLOGIES

Successful electronics manufacturing means being responsive to the packaging and the assembly demands of both the IC and end product. Paramount to this success is the interconnect substrates that support Level 1.0 single chip and multichip packaging and the all important Level 2.0 printed wiring board (PWB). Technologies for the manufacture of these interconnects include:

- Thin film
- Thick film/Cofired ceramic (Chapters 13/14)
- Laminate/Organic (Chapter 15) and,
- Build Up Technology (BUT)—A combination of laminate and thin film.

These multilevel interconnect structures are characterized by high wiring densities that combine fine line high conductivity traces and small interlevel vias. While the technologies discussed here are basically mature processes, all continue to evolve in response to device and end product requirements.

12.1 — Thin Film Technology [1–5]

The thin film process incorporates relevant IC wafer manufacturing technology and methodology as well as applicable practices and procedures. The processing makes available a viable high volume, cost effective manufacturing scenario fully supporting the interconnect packaging and assembly needs of Levels 1.0 and 2.0.

When performed in a proper manufacturing environment, such as a "cleanroom" similar to that shown in Figure 12-1, the thin film process readily addresses the high density interconnection requirements dictated by current and future high performance ICs.

Table 12-1 lists current leading edge and state-of-the-art dimensional capabilities covering fine lines, spaces, via diameters and pitch using the thin film process.

Figure 12-1. Thin Film Cleanroom

Table 12-1. Thin Film Process Capability [20]

Characteristics	Current	Leading Edge	State of the Art
Via Diameter (μm)	20	10	<10
Via Pitch (μm)	50	25	<25
Line Width (μm)	25	10–12	<10
Line Space (μm)	25	12	<10
Line Pitch (μm)	50	25	<20
Substrate Size:			
X/Y (mm)	127–150	150	600
Z (mm)	0.6–12	1.5	
Number Conductor Layers	2–4	6	6

Because the thin film process essentially emulates the photolithographic aspects of IC wafer fab it obviously has many advantages, offering

- Smallest feature resolution and therefore the highest wiring density
- High performance materials availability
  - High conductivity conductors
  - Low k dielectrics
- Metallization systems that can be tailored to accommodate wire bonding, flip chip and solder attachment
- A low temperature process, generally below 300°C and therefore
- Ready availability of a variety of base substrates both inorganic and organic.

The thin film process can also be readily combined with other technologies such as thick film, cofired ceramic and printed wiring board to enhance capability and extend areas of application.

12.2 — The Patterning Process

The most common thin film conductor patterning processes applicable to the vast majority of Levels 1.0 and 2.0 interconnects, are a semi-addtiive, involving selective electroplating, and a subtractive process in which unprotected metal is selectively removed by etching. The two processes are illustrated in Figure 12-2.

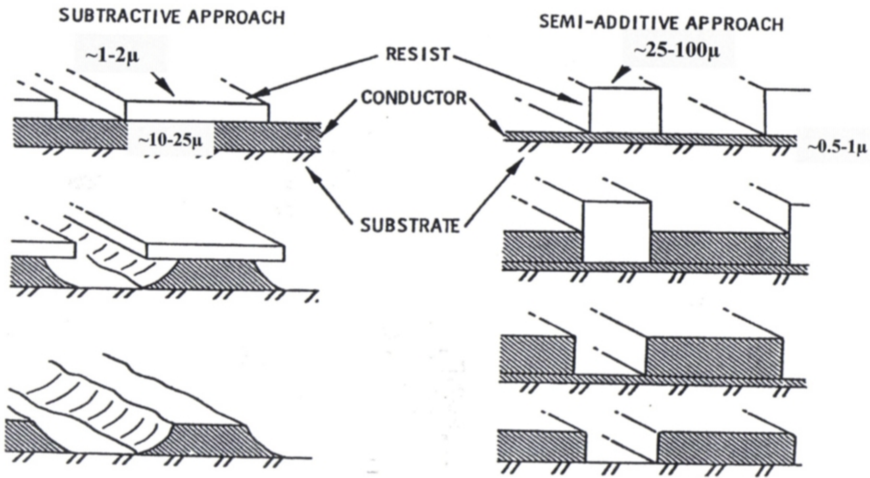
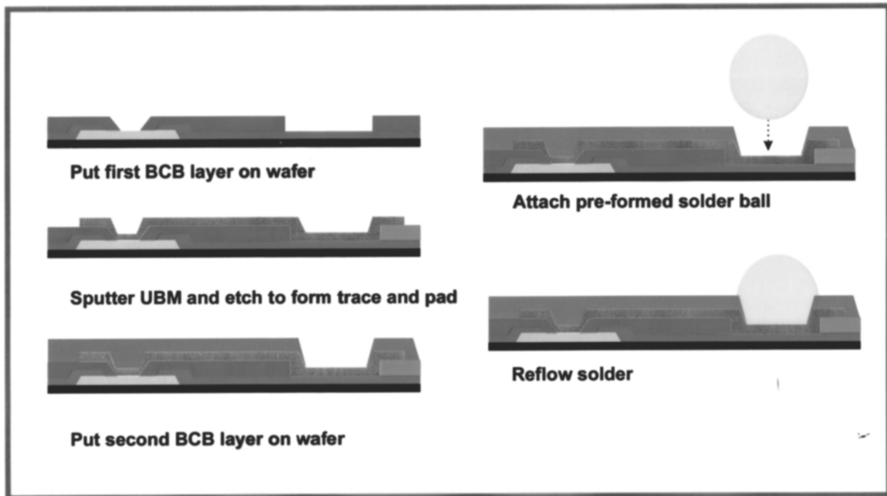


Figure 12-2. Subtractive Etch and Selective Plate Up Patterning Processes

Depending upon the particular process, the thickness of the initial deposited metal will vary from less than 1 micron (semi-additive) to several microns (subtractive). For example, if semi-additive processing is employed, a thin layer of metal is deposited and a thick layer of photoresist applied and patterned to allow for selective plate-up of additional metal to a desired final thickness. For the subtractive process a thicker metal is deposited by sputtering, plating (electroless + electrolytic) or cladding. This is followed by application and patterning of a layer of photoresist. The unprotected metal is then removed by a wet chemical or dry etchant. Interestingly the subtractive etch process is used for the patterning of the very thin aluminum metallization (<1μm) on the IC and the very thick copper (35μm) cladding in laminate PWB manufacturing.

Figure 12-3 graphically describes a thin film process, step-by-step, for producing a WL-CSP. The process basically involves a redistribution of the IC peripheral I/O bond pads to an area array format. It uses benzocyclobutane (BCB) as the insulator and Al-Ni/V/Cu for the conductor metal. The conductor metal is patterned by subtractive etching.



(Courtesy Flip Chip International)

Figure 12-3. Thin Film Process for WL-CSP (Ultra CSP®)

Photoresist patterning is the key to producing both thick metal deposits for bumping and very fine lines and spaces and small vias yielding high wiring densities. Patterned features are characterized by well-controlled geometries and dimensional tolerances. Critical aspects of the patterning process have been discussed in Chapter 2, and include: the photomask, the resist itself, and the exposure system.

12.2.1 — The Photomask

For packaging and assembly applications with minimum line width and spaces approaching 25–50μm, hard surface glass masks become indispensable. Emulsion (halide on polyester) film photo-tooling cannot provide the dimensional stability, image edge acuity and useful print life considered necessary. Chrome masks and iron oxide are preferred for most applications. The iron oxide mask is particularly useful and practical for multilevel structures because the image is transparent or "see-through" and therefore greatly simplifies mask alignment to previously patterned layers.

12.2.2 — The Photoresist: Liquid, Dry Film, Electrodeposited [6,7]

In IC wafer fab liquid resists deposited by spin coating are used exclusively. WLP, FC and HDI, in general, require thicker metal deposits and consequently, require thicker layers of resist. While thick layers are achievable by spin coating, alternative methods and materials are also available including spraying coating of liquid resist, use of a dry film resist applied by lamination and an electrodeposited resist.

The selection of a particular type of resist depends upon many factors. A major consideration is the minimum feature size required. The "rule of thumb" is the smaller the feature size the thinner the resist coating. The liquid resist and the

electrodeposited resist readily provide for thin coatings. The dry film resist is applied by lamination, a process that does not lend itself for use on large diameter wafers (>200mm) that can be 100–125um thick. On the other hand, spin coating of liquid resists is not practical on very large substrates. Hence, dry film resist is used extensively in the manufacture of PWBs.

When liquid resist is applied by spin coating the thickness of the deposited film will be dependent upon the particular resist formulation (viscosity, solids content) and the spin speed (rotations per minute, rpm). Thus, the slower the speed, the thicker the coating will be, and the higher the rpm the thinner the coating.

Table 12-2 lists applicable properties of two liquid resists, a positive acting resist and negative acting high solids. Note the substantial increase in attainable coating thickness of the negative acting resist. This results primarily from the high solis content.

Table 12-2. Typical Properties of Spin on Liquid Resist [6]

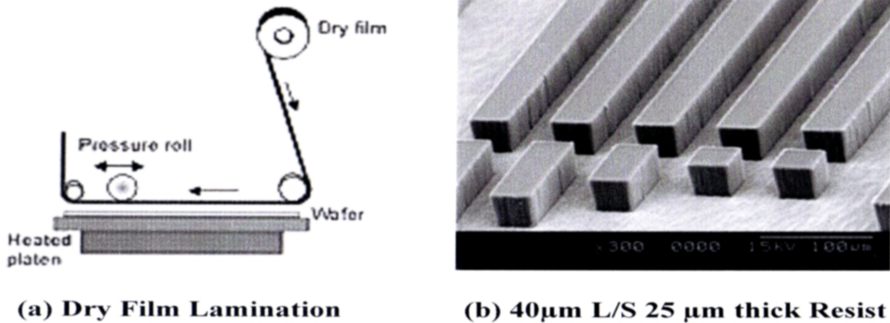
Property	Positive	Negative (high solids)
Film Thickness (μm)	1–20	40–140
Exposure Energy (mJ/cm^2)	210–400	800–2000
Developer	TMAH	Acid, TMAH, KOH
Use	Acid Plating, Etching	Acid Plating, Etching
Remover (Stripper)	NMP Proprietary, Solvents	NMP, Solvents, hydroxides
Feature Resolution (μm)	<5	<5

Dry film resist, applied by lamination as illustrated in Figure 12-4(a), is available as positive or negative acting and range in thickness from 12.5μm (0.5 mils) up to 50μm (2.0 mils). Table 12-3 lists typical properties of a negative acting dry film resist. Positive dry film resists are also available but the exposure energy for very thick layers is excessive resulting in long exposure times.

Table 12-3. Dry Film Phototresist Properties [6]

Property	Dry Film Resist
Tone	Negative
Film Thickness	25–100 microns
Exposure Energy	25–100 mJ/cm^2
Developer	Carbonate
Use	Electroplating/Etching Mask
Remover	Hydroxide
Feature Resolution	1:1 feature: film thickness depend

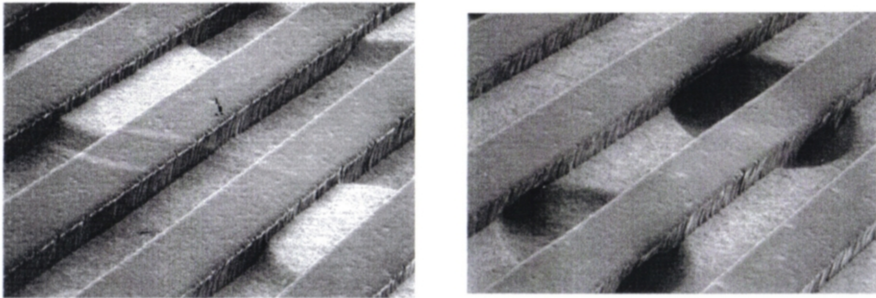
Dry film has excellent adherence to metals and is widely used in PWB manufacturing for patterning by either selective plate-up or subtractive etch. Figure 12-4(b) shows 40μm lines and spaces on a 25μm thick dry film resist. Note worthy is the straight sided wall geometry. Distinctive features of the dry film are the thickness control and "tenting" ability as illustrated in Figure 12-5. The "tenting" feature is used to protect plated substrate through-holes while other features are being etched.



(a) Dry Film Lamination **(b) 40μm L/S 25 μm thick Resist**

(Courtesy Hitachi Chemical Co. America, Ltd.)

Figure 12-4. Dry Film Lamination and Patterning



(Couretsy Dupont Printed Circuit Materials)

Figure 12-5. (Left) Dry Film Applied Over Previously Patterned Structure; (Right) Substrate Vias or Holes

Another alternative process with some rather unique features is the electrodeposited (ED) or electrophoretic resist. The ED resist process is similar to the semi-additive electroplate process and requires a plating buss. The bath is an aqueous emulsion that contains "micelles" or electrically charged polymers, plus solvents and photosensitizers. Depending upon electrical connectivity the deposited resist will be either a positive or negative tone. Following plating the deposit is baked to drive off water forming a hardened film. Table 12-4 lists the properties of ED resists.

Table 12-4. Electrodeposited Photoresist Properties [6]

Property	Positive Tone	Negative Tone
Film Thickness	2–20 microns	5–50 microns
Exposure Energy	250–450 mJ/cm^2	800–1500 mJ/cm^2
Developer	TMAH, Carbonate	Organic Acid
Use	Acid Plating, Etching	Acid Alkaline Plate and Etch
Remover	Hydroxide	NMP proprietary
Feature Resolution	<5 microns*	<5 microns*

* Dependant upon thickness

The thickness of the resist is dependent upon the bath composition, bath temperature and plating voltage. The process is self-limiting with maximum thickness roughly 20\um for the positive and 50um for the negative resist. The deposited resist is extremely conformal as evident from Figure 12-6, where 25um lines are patterned over a 45um thick, 100um wide feature.

The process is currently being used in wafer bumping and WLP.

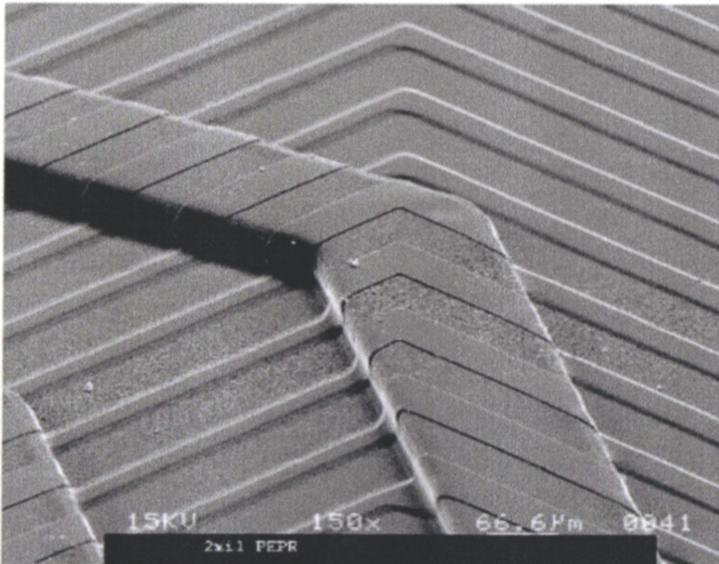


Figure 12-6. Electrodeposited Resist: Patterned for Selective Plate-up of 25um Lines Over Previously Patterned 45um Thick 100um Wide Feature [6]

12.2.3 — Exposure Systems [8–10]

There are many factors that must be taken into consideration in selecting an appropriate exposure system, not the least of which is cost. For applications where

minimum feature is roughly 25um, a proximity mask aligner is more than adequate. Where feature sizes are 10um and less a 1X stepper projection aligner would be a better choice, although more costly. Negative aspects for the mask aligner are mostly mask related costs. A full area array mask is far more expensive than a 1X singleare mage reticle used on the stepper. The print life of the reticle exceeds that of the array by greater than a factor of 10. While yields are lower for the mask aligner, the initial capital investment, operation and maintenance costs of the 1X stepper are substantially higher. Whereas the stepper offers higher resolution it has a considerably lower throughput that results in increased manufacturing cost.

Table 12-5 compares the attributes of a Mask Aligner and 1X Projection Stepper.

Table 12-5. Mask Aligner vs. 1X Stepper [7]

Criteria (# Preferred)	Mask Aligner	1X Stepper
Capital Investment	#	
Operating Cost	#	
Throughput	#	
Mask Cost		#
Ease of Operation	#	
Resolution		#
Side wall profile		#
Alignment Accuracy	#	#
Overlay Accuracy		#
Mask Print Life		#

12.3 — Processing an HDI Substrate Interconnect [11,12]

The following is a generic step-by-step process description for a two conductor layer interconnect that might apply to the manufacture of a single or multichip package, inorganic or organic based.

1. Select and prepare substrate.
2. Deposit dielectric (if required, e.g., if using a metal substrate).
3. Deposit first metal layer and define conductor pattern.
4. Deposit second dielectric layer and define vias.
5. Deposit second metal layer and define conductor pattern.
6. Deposit third dielectric (passivation) layer and define openings to expose all bonding pads.
7. Plate bond pads if required.

Implementation of the technology involves a significant investment in facilities (cleanroom) and capitol equipment that include:

- A vapor deposition system, i.e., sputterer, and/or electron beam vacuum evaporator, for depositing metals and dielectric films
- A mask aligner/exposure system (Stepper) for patterning photosensitive materials that will act as an etch mask or as a template for electrolytic or electroless plating
- An electroplating module
- Chemical or plasma stations for cleaning, developing, etching, etc.

In addition, but equally important is the tooling, fixturing, and storage facilities necessary for maintaining the substrates in a near-pristine condition throughout the entire manufacturing process.

12.3.1 — Subtractive Etching vs. Selective Plate-up Process and HDI

In the subtractive etch process the patterned photoresist functions as a "etch mask" In the semi-additive process a very thin layer of metal is first deposited to serve primarily as a plating buss. The photoresist is patterned removing resist from those areas where a plated-up metal is to be selectively deposited. The resist, in this case, is used as a "plating mask" or template to selectively confine the plating rather than an etch mask.

The selective plate-up process is used for applications:

- Where fine lines and spaces are a prerequisite and require well-controlled, tight tolerance geometries, i.e., Wafer Level Packaging (WLP) and HDI for MCP and Level 2.0 PWBs, and
- Wafer bumping where a thick conductor metal is required.

12.3.1.1 — Subtractive Etch Process

Subtractive etch can be a dry or a wet process. Ion milling for example is a dry etch process and is typically used in niche type applications where use of wet chemical processing is inappropriate or prohibitive.

Wet chemical etch when used with thick metals, roughly greater than 10–12 μm—like the copper clad PWBs—will often require the photomask images to have dimensions larger than the desired dimension on the finished part. This is to compensate for the isotropic properties of most wet chemical etching processes, that is, etching occurs equally in all directions, x, y and z. The so-called "undercutting" in x and y effectively leaves the etched metal conductor with a trapezoidal cross-section, with the top surface smaller in width than the bottom (Figure 12-7). To help compensate for this the image on the photomask is dimensionally adjusted, i.e. enlarged to produce a wider resist pattern. This modification is referred to as the "Correction or Etch Factor". The increase in the size of the image on the photomask will depend upon the thickness of the metal and can be as much as twice the thickness of the metal to be etched. The degree of "undercutting" is also very much dependent upon the etching technique and equipment. For example, parts that are presented to the etch solution vertically generally exhibit less "undercutting" than parts that are etched horizontally. It should also be obvious that the thinner the metal, the smaller the correction that is needed.

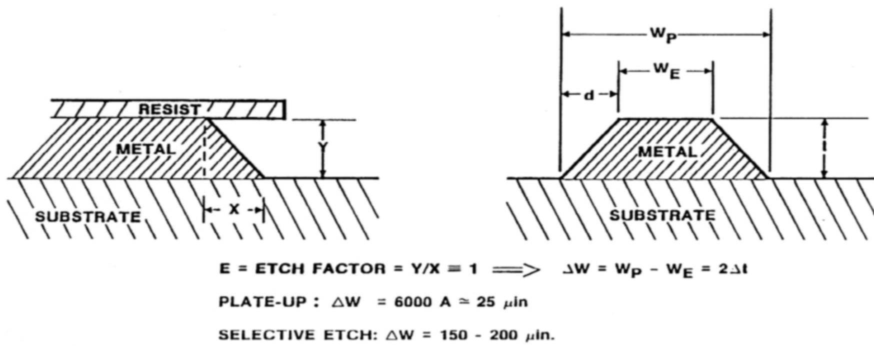


Figure 12-7. Subtractive Etch Process; The “Etch Factor” [1]

12.3.1.2 — Semi-Additive Process [13,14]

With the semi-additive or selective plate-up process there is no etch factor and therefore the pattern features on the mask are the same as the dimensions on the finished part. It also allows for a degree of control of the geometry of the plated conductor not attainable with the subtractive etch. Because the patterned photoresist acts as a template for the plating the post plated conductor will replicate that of the patterned resist. If the resist has straight-sided walls the conductor will exhibit sides that are straight-sided as well. If the walls are slopped the sides of the conductor will also be sloped. As a result, a pre-plate inspection of the patterned resist is possible and a predetermination made of the finished plated conductor shape and dimensions. “Out of spec” parts can simply be stripped and new resist deposited and patterned thereby insuring high process yields.

12.4 — Thin Film Materials

A variety of materials for manufacturing HDI are available covering substrates, conductor metals and dielectrics. For example, the low temperature aspect of the thin film process allows for application to inorganic *or* organic substrates, unlike the thick film and cofired ceramic technologies that are both high temperature processes.

Processes available for depositing conductors such as sputtering and evaporation allow selection of very high conductivity metals. Similarly, the availability of dielectric materials with varying properties and deposition processes allow choosing the “right” material for a particular application.

12.4.1 —Conductor Materials

The thin film process typically deposits conductor material by sputtering, a deposition process which can also be used to deposit dielectric materials.

Conductor metals are all chosen for their high electrical conductivity properties as listed in Table 12-6.

Table 12-6. Conductor Metals

Material	Resistivity (microhms-centirmeter)
Silver (Ag)	1.62
Copper (Cu)	1.72
Gold (Au)	2.45
Aluminum (Al)	2.69

While Ag has the highest conductivity it is also susceptible to conductive filament formation (whiskers) that results from the presence of moisture. Hence it is not used with an organic dielectric. When Ag is embedded in an LTCC it is hermetically protected and the high conductivity properties can be fully realized. As a consequence, for package and board interconnects, Cu and Al are the inner layer metals of choice. When Cu is used as the conductor metal, an adhesion layer metal, e.g., Ti, Ti/W, or Cr, must be deposited first, much like an under bump metallization. Au is normally not used as an inner layer conductor metal. It is however used as an over-plate with Cu. For example, Ni-Au over Cu is required for the top surface termination metal to prevent corrosion of the Cu and provide the proper metallurgy for component attachment (solder, wire bonding).

Table 12-7 lists commonly used metals and their function.

12.4.2 — Dielectric Materials

In selecting a suitable dielectric for HDI interconnections the following attributes should be taken into consideration:

- Low Dielectric Constant (<4)
- Low Coefficient of Thermal Expansion (CTE) Close to Silicon
- Good Mechanical Properties
  - High Elongation
  - High Fracture, Toughness
- Good Adhesion
  - to Conductor Metals (Cu, Al)
  - to Substrates—Ceramic, Si, Metals
- Low Water Absorption
- Thermal Stability to 400ºC
- Low Solvent absorption
- Processability
  - Pinhole-Free Films
  - Planarization
  - Via Formation

Aluminum readily reacts with the various substrates and dielectrics and therefore does not require the deposition of the adhesion/barrier metals. It is also not necessary for a top surface over-plating unless there is the need to provide for solder attachment. Al is typically deposited by sputtering or electron beam evaporation.

Table 12-7. Metals and Their Function *(Courtesy Advanced Technical Ceramics)*

Material Function	Types of Material	Range of Values	Comments
Resistor	Tantalum-Nitride (TaN)	25–150 ohms/sq (max)	25–125 ohms/sq (Std)
	Nickel-Chromium (NiCr)	50–250 Angstroms	
Adhesion	Titanium-Tungsten (TiW)	250–750 Angstroms	Ideal for High Temperatures
	Chromium (Cr)	250–750 Angstroms	Limited to Low Temperatures
Barrier	Nickel (Ni)–Sputtered	750–1500	Standard Barrier
	Nickel (Ni)–Plated	40–100µin (1–2.5µm)	High Conductivity Barrier
	Palladium (Pd)–Sputtered	750–1500	Minimum 2 mil features
	Platinum (Pt)	10–200µin (0.4 to 5µm)	
Conductor	Gold (Au)	400–1000	
	Copper (Cu)	10–200µin (0.4–5µm)	
High Current Conductor	Gold (Au)	400–1000µin (10–25µm)	3 mil traces minimum
	Cu/Ni/Au	1.5–4.0 mils 37–100µm	5 mil traces typical

Processability refers to preferred endprocess properties For example, a pinhole-free interlayer dielectric is an absolute to ensure against shorting between conductor layers. Planarization is a measure of the degree of coverage of deposited (and cured) dielectric with respect to the underlying conductor topography. Ideally, the deposited layer should provide a top surface that is flat, rather than conformal. The degree of planarization achieved is schematically defined in Figure 12-8. In practice the thicker the dielectric with respect to the underlying feature the greater the degree of planarization. Finally, the dielectric selected should allow vias to be readily formed using processes that are compatible with high volume production.

Materials suitable as inner layer dielectrics include:

- Silicon Dioxide (SiO_2)
- Polyimides (PI)
- Benzocyclobutane (BCB)—commercially available as Cyclotene™
- Liquid Crystal Polymers (LCP)
- Fluoropolymers
- Epoxies

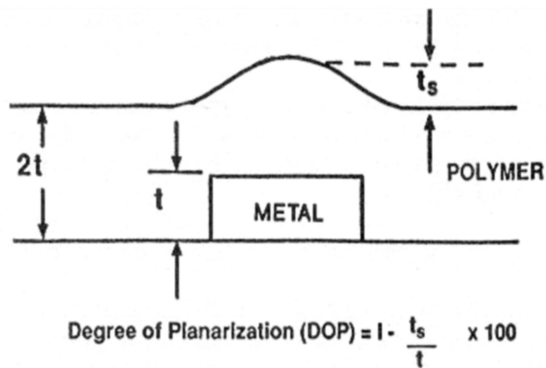


Figure 12-8. Planarization of a Deposited Dielectric [1]

Of these SiO_2 is an inorganic and is deposited by either sputtering or chemical vapor deposition. Deposition is critical and stress in the SiO2 film is a major concern and achieving an acceptable degree of planarization is difficult. For most HDI applications the organic materials are preferred. They are readily deposited and are available as liquid or as a dry film.

For Level 1.0 MCP interconnects the most commonly used dielectric is either polyimide (PI) or benzocyclobutene (BCB). Table 12-8 lists typical material properties for both PI and BCB.

Table 12-8. Material Properties for Polyimide and BCB [20]

Material ► Properties ▼	Polyimide	BCB
Electrical:		
Volume Resistivity (Ω-cm)	$>10–14x10^{-6}$	$1.8–2.0x10^{-19}$
Sheet resistance (Ω/sq)	4–10 megohms	
Dissipation factor	10^{-3}	$8x10^{-4}$
Dielectric constant	3.0–3.5	2.65
Mechanical:		
Adhesion (gms/mm)		
Tensile Strength (MPa)	115	87
Elastic Modulus (MPa)	40	
Tensile Modulus (GPa)		2.9
Elongation (%)	10–25	6
CTE (ppm/°C)	20–40	52

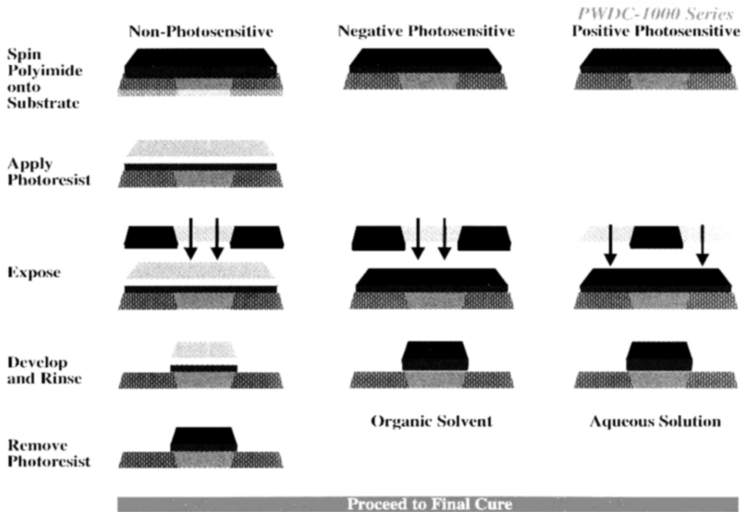
12.4.3 — Via Patterning in Dielectric Layers

Via patterning in a dielectric is a major consideration in selecting a particular material. Dielectric layer via generation process options include:

- Laser ablation
- Plasma
- Photo-patterning

Each offers certain advantages. For example, laser and plasma are "dry" processes and therefore more "environmentally friendly". Laser processes however are sequential, that is, vias are formed one at a time. The plasma and photo-patterning processes (wet chemical) are all batch or parallel processes with all vias formed in a single step.

Photo-patterning is a photolithographic based process that uses either photosensitive or photodefinable dielectric materials. The photodefinable uses a resist and a subtractive etch for patterning. The photosensitive dielectric contains a photosensitizer that allows patterning directly upon exposure to an ultraviolet light source. The photosensitive materials are available in positive and negative formulations. The processes are graphically presented in Figure 12-9. Both options are used extensively in the manufacture of MCM-D interconnect substrates, redistribution processing and wafer level packaging.



(Courtesy Dow Corning)

Figure 12-9. Photodefineable vs. Photosensitive (+/–) Via Patterning

Laser patterning by ablation is more extensive in the manufacture of Level 1.0 organic SCP and Level 2.0 HDI substrates (Chapter 15) where very large panels or boards—too large for most optical exposure systems—are routinely processed.

Figure 12-10 compares achievable via diameters for various laser systems and the photo-patterning process.

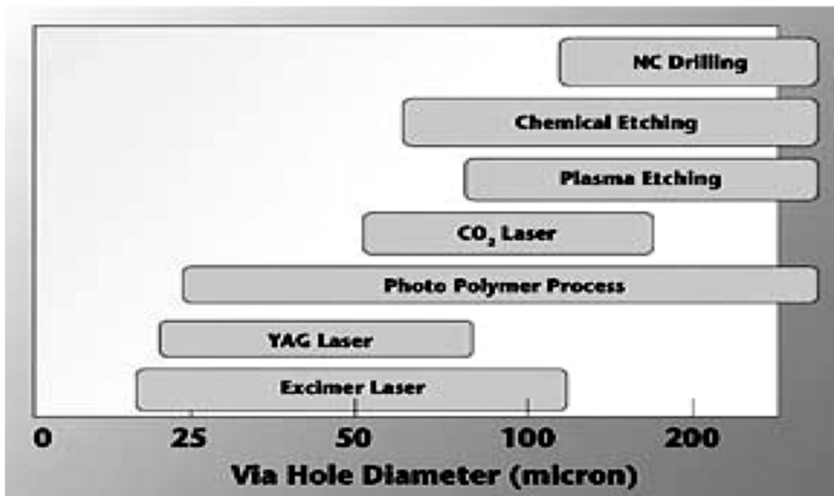


Figure 12-10. Achievable Via Diameters Using Laser and Photo-Patterning

12.4.4 — Substrates

The most common substrates in use for HDI include:

- Ceramic/Glass-Ceramic
- Silicon
- Metals
- Organic Boards—rigid and flexible film

Table 12-9 lists the various package/substrate materials and their key properties that are important considerations in packaging the IC.

Basically, the substrate typically functions merely as a rigid support of a multilevel conductor interconnect (Figure 12-11). Usually MCM-D substrates are mounted into packages, metal or cofired ceramic, much the same as a hybrid circuit. The package serves as a hermetic enclosure as well as the interface to electrical testing and the next assembly level.

The substrate can also be previously fabricated with embedded conductor interconnect layers, e.g. power and ground, and/or deposited components, e.g., passives and in some special cases active devices. Thin film interconnects are used on both cofired ceramic and laminate substrates containing embedded power and ground planes to provide the fine line capability needed to accommodate fine pitch, high I/O flip chip and Wafer Level-CSPs. The process is illustrated in Figure 12-12 for a cofired ceramic substrate. This combination of the two technologies, namely, cofired and thin film, when used as a MCM package, is referred to as a MCM-C/D. When applied to laminates it becomes a MCM-L/D (Figure 12-13).

Table 12-9. Thermal Properties of Select Inorganic Materials [3]

Material	Thermal Conductivity W/m—ºC	Coefficient Thermal Expansion CTE—ppm ºC
Ceramic		
Beryllium Oxide	150–300	6.3–7.5
Silicon Carbide	120–270	3.5–4.6
Aluminum Nitride	82–320	4.3–4.7
Silicon Nitride	25–35	2.8–3.2
Silica	1.5	0.6
Aluminum Oxide	15–33	4.3–7.4
Steatite	2.1–2.5	8.6–10.5
Fosterite	2.1–4.1	11
Titanate	3.3–4.3	7–10
Cordierite	1.3–4.0	2.5–3.0
Mullite	5.0–6.7	4.0–4.2
Metals		
Molybdenum	138	3.0–5.5
Copper-Tungsten 10/90	209	6.0
Tungsten	174–177	4.5
Kovar	15–17	5.9
Others		
Silicon	*125–148*	*2.3*
Diamond	2000–2300	1.0–1.2
Quartz	43	1.0–5.5

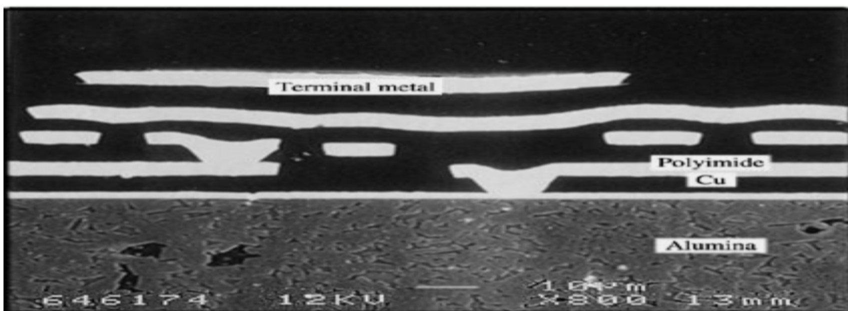
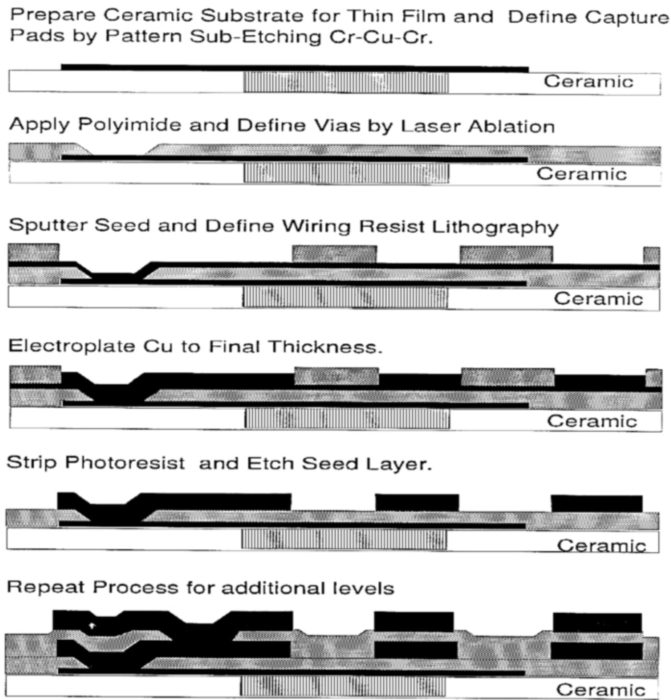
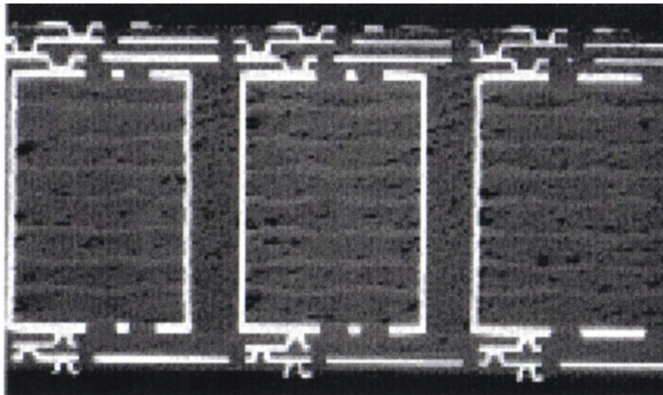


Figure 12-11. Metallurgical Cross-Section Thin Film Multilayer Interconnect on Ceramic Substrate



(Courtesy IBM Corp.)

Figure 12-12. Thin Film Interconnects on Co-fired Ceramic Substrate



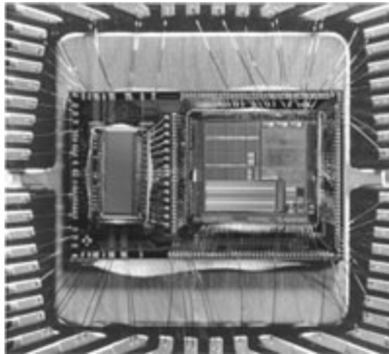
(Courtesy Kyocera America)

Figure 12-13. Thin Film Multilayer Interconnect on PWB (MCM-L/D)

Application of this same technology to organic boards offers a positive approach to the manufacture of Level 1.0 IC single chip packages, i.e., the PBGA, and critical HDI Level 2.0 interconnects. It provides high-density wiring capability accommodating currently available, as well as future component packaging and assembly technologies including fine pitch wire bonding with minimal fanout, WL-CSP and flip chip.

12.4.5 — The Silicon Substrate [15,16]

Of all the various substrate materials available the most interesting is silicon. It makes an ideal substrate for many MCP applications, particularly SiP and SoP. Its use immediately eliminates one serious reliability concern relating to mismatch in CTE between the silicon device and the substrate. At the same time it also has a favorable thermal conductivity (150W/mK). Figure 12-14 shows a few chip MCM consisting of a Si substrate supporting a multilevel interconnect, with polyimide as the dielectric and Al as the conductor. The Si substrate assembly is mounted onto a leadframe.

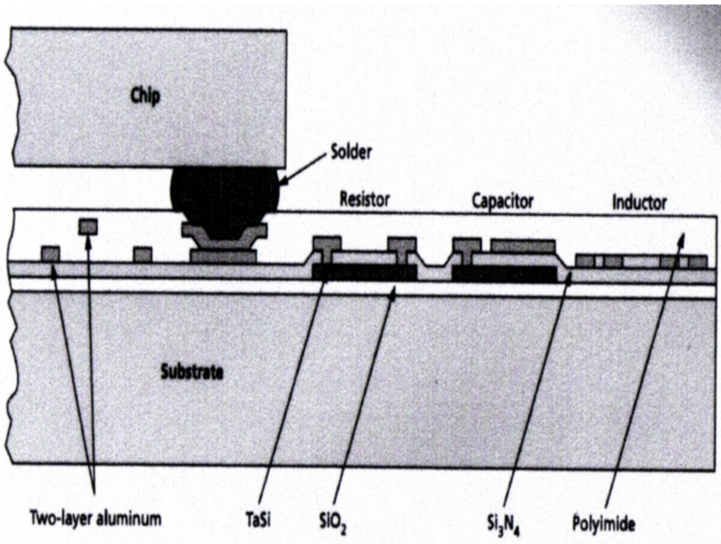


(Courtesy Strand Interconnect AB)

Figure 12-14. Si Substrate Supporting Multilevel Thin Film Interconnect for MCM

Perhaps the most important attribute of the Si substrate is the ability to pre-configure a customized substrate by embedding not only passive elements (resistors, capacitors) but active devices (diodes, transistors, *and integrated circuits*) as well. Figure 12-15 schematically presents a cross-section of a silicon substrate with embedded passives in the interconnect network. Replacing the discretes with embedded equivalent thin film passives, either within the Si substrate or the conductor interconnect circuitrym, many advantages accrue affecting cost and reliability.

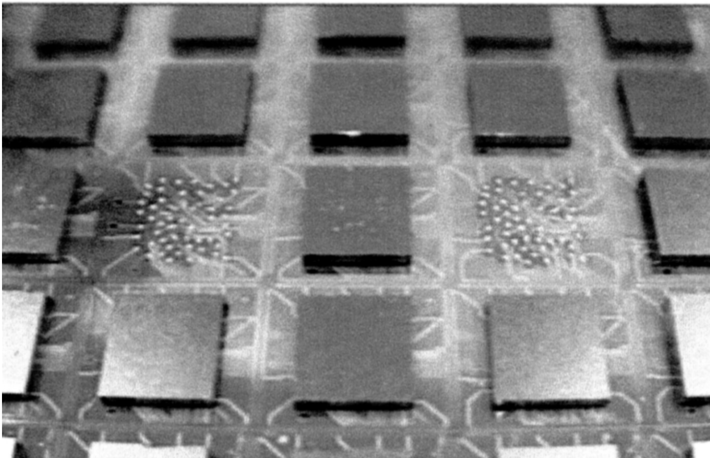
Embedding of discrete passives eliminates the need for assembly and opens up available area for additional wiring capability. The end result is reduced cost with increased functionality per unit area, i.e., more active devices can now be accommodated utilizing the area formally occupied by discrete passive components.



(Courtesy SyChip, Inc.)

Figure 12-15. Schematic Cross-Section of a Si Substrate with Embedded Active and Passive Devices

Figure 12-16 shows DRAM memory die flip chip attached to a thin film interconnect that was fabricated directly onto ASIC devices while in wafer format. The "Chip on Chip" assembly is packaged in the same size package as the single chip ASIC.

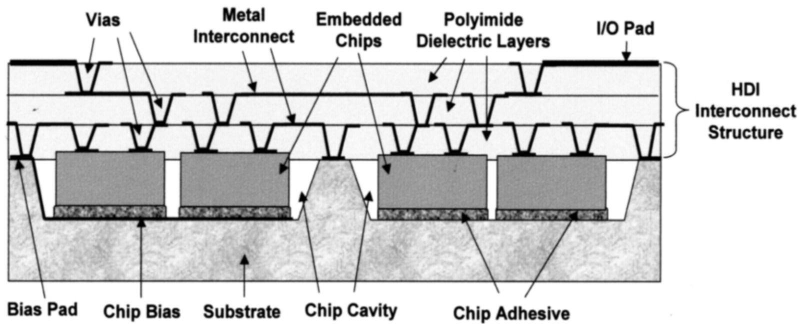


(Courtesy SyChip Inc.)

Figure 12-16. DRAM Chips Flip Chip Assembled on Electrically Tested ASICs

12.5 — Alternative Thin Film Processes for MCP Applications [17]

Conventional MCPs are assembled using Chip & Wire, TAB, or Flip Chip to previously fabricated interconnect substrates. In the mid 1980s the General Electric Co. introduced a new approach, utilizing a process in which chips are first assembled to a substrate and the chip-to-chip interconnects achieved by using a combination thin film-laminate process. This resulted in a structure shown in schematic cross-section in Figure 12-17, and became known as the GE HDI process or "Chips First" packaging.



(Courtesy GE Global Research)

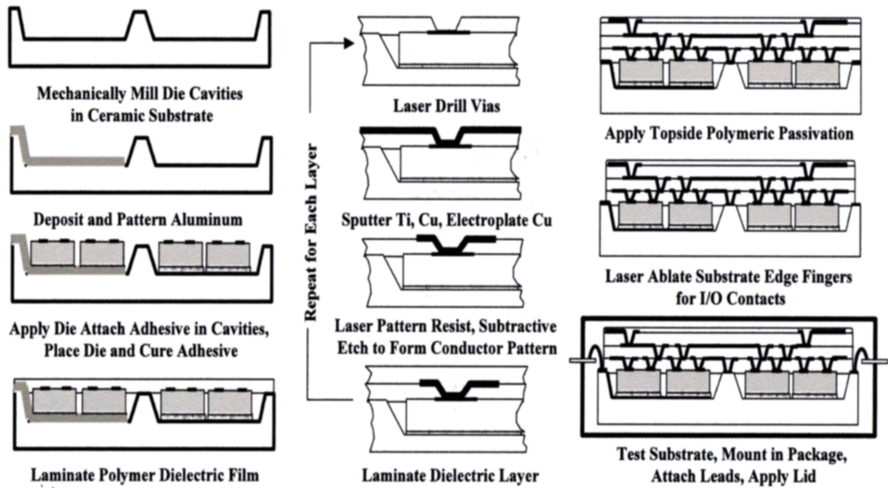
Figure 12-17. GE HDI "Chips First" MCM

12.5.1 — The GE HDI Process

A step-by-step description of the process is schematically represented in Figure 12-18. The process begins with substrate preparation that includes configuration of cavities. The number and size of the cavities corresponds to the chips to be assembled. The depths of the cavities vary and are dictated by the thickness of the various die, that will often vary depending upon the device manufacturer. The intent is to have the surface of each device at the same level. After attachment of the die, a 25μm thick fully cured Kapton™ film (polyimide) is laminated over the substrate using a thin 12μm polymeric adhesive.

A laser system designed specifically for the application first locates the bond pads on each of the devices and then drills vias through the Kapton® and adhesive exposing the Aluminum metallized pad. The first layer of metallization, Titanium-Copper, is sputter deposited followed by a plate up of copper to build up the thickness. Patterning of the conductor involves application of a photoresist that is subsequently exposed by a computer controlled laser lithography system driven directly from the circuit's design database. A wet chemical etching completes the conductor patterning. Another layer of dielectric is applied and the process is repeated to produce additional conductor layers as may be required.

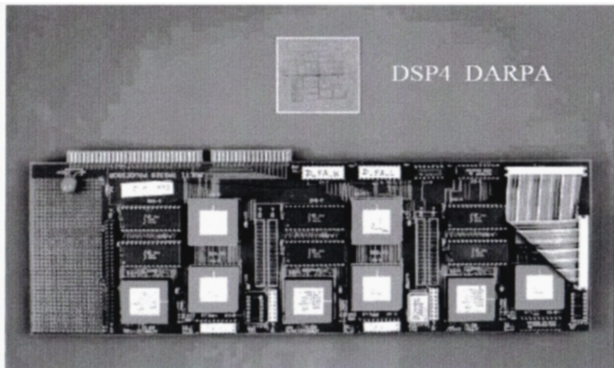
Use of liquid polyimide or BCB in place of the Kapton® and standard photolithographic processing are options that eliminate film lamination and the laser lithography equipment. It does require however, that the die placement equipment has a readily achievable placement accuracy of +/–5μm or better.



(Coutesy GE Global Research)

Figure 12-18. The "Chips First" (GE HDI) MCM Process Flow

The process offers several advantages. It essentially eliminates first level interconnects. There is no wire bonding, TAB or flip chip and it readily accommodates embedding of discrete passives. It also achieves very high packaging efficiency as is evident from Figure 12-19 showing a GE HDI MCM and the SMT printed circuit assembly version.



(Courtesy GE Global Research)

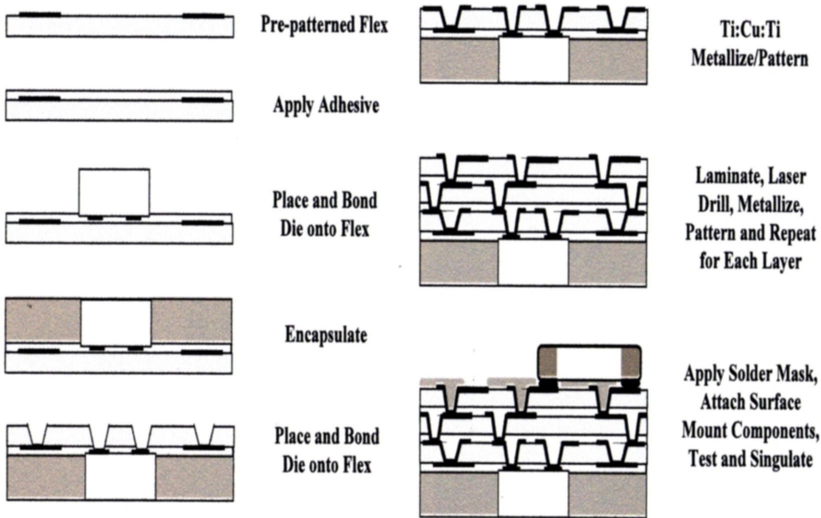
Figure 12-19. GE HDI MCM and SMT Printed Circuit Board Assembly

GE HDI however does have some problems. The process is costly vs. "Chips Last" approach and, most importantly, rework is complicated, difficult and costly. A defective chip, detected only after the process is completed, cannot be easily

removed/replaced. Often an entire assembly must be scrapped. This can be addressed to some degree by using only Known Good Die or judicially selecting only mature die with a very high probability of electrical integrity, or a combination of both. There is of course, the added cost factor associated with KGD.

12.5.2 — Low Cost "Chips First" MCM [18]

A modified GE HDI process had been developed and demonstrated that addressed the some of these cost factors. The low cost version eliminates the ceramic substrate as illustrated in Figure 12-20. A large process panel capability has been added that enables multiple units to be fabricated concurrently. It is now referred to as an Embedded Chip Build Up (ECBU) process packaging technology.

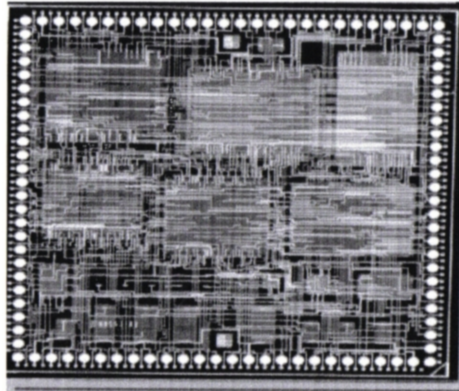


(Courtesy GE Global Research)

Figure 12-20. The Low Cost GE HDI or Embedded Chip Build Up (ECBU) Process

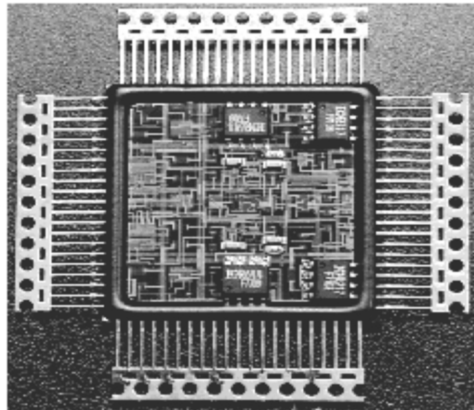
The process now begins with a flex circuit film, that has the pre-patterned first level metal interconnect in place, to which the die are adhesively attached. An encapsulation follows which in effect serves as the substrate. A process similar to the GE-HDI process follows. Figure 12-21(a) shows a fully embedded MCM that includes discrete passives. The MCM is terminated with solder balls in a peripheral format.

A key feature of the "chips first" ECBU approach that is not immediately apparent is that it readily offers a 3-D capability. An additional metallization layer can be added to support the assembly of more devices to the top surface while still in panel format. These can be packaged devices or bare chips and include actives and passives. An example is shown in Figure 12-21(b).



(Courtesy GE Global Research)

Figure 12-21(a). An ECBU MCM with Embedded Active and Passives



(Courtesy Lockheed Martin Corp.)

Figure 12-21(b). An ECBU MCM with Embedded Actives and Passives and Package Devices and Discrete Passives Mounted on Top Layer

12.5.3 — The Bumpless Build Up Layer (BBUL) Interconnect Package [19]

In 2001, Intel announced a new packaging approach being developed specifically for future microprocessors that are expected to operate at 20 Gigahertz and higher, containing in excess of a billion transistors. Called Bumpless Build Up Layer (BBUL) packaging, it is similar to the low cost GE HDI in that it is a "chip first" approach for both single chip and multichip applications. It employs a process that is a combination of thin film and laminate technologies.

The process sequence is shown in Figure 12-22. It begins with an organic substrate panel with a hole punched out to allow insertion of the device.

This is analogous to the GE HDI starting ceramic. Figure 12-23 shows Intel's current microprocessor packaging and the BBUL package. Figure 12-24 is the multichip version BBUL.

BBUL packaging offers:

- A thinner and lighter package
- Higher wiring density
- High performance and lower power

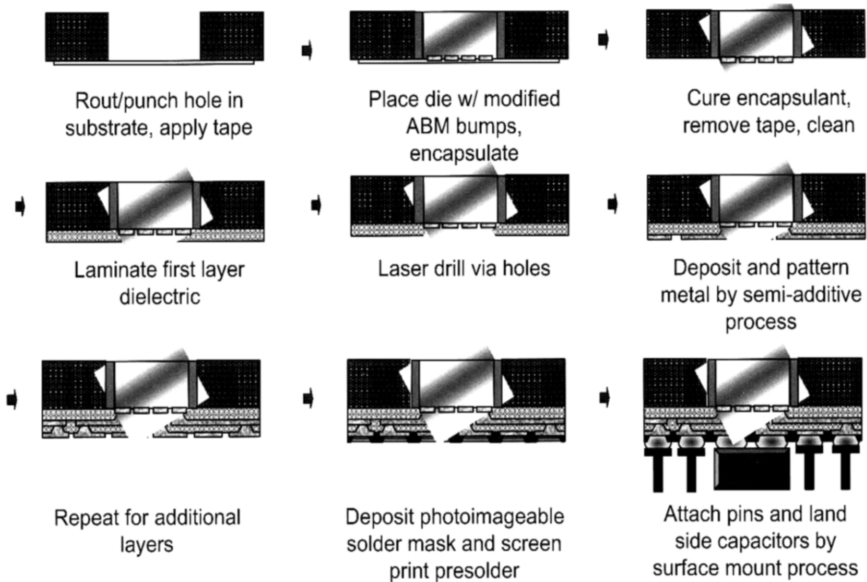


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Figure 12-22. The Intel BBUL Process for Microprocessors

12.5.4 — Summary "Chips First" Technologies

The "Chips First" (GE-HDI) and Intel's BBUL technologies are assembly/ interconnect processes that offer

- Die assembly with "direct" metallurgical connection to the die pads. No wire bonding or flip chip bumping
- A multiplayer interconnect structure typically consisting of
  - A 25µm Kapton™ film dielectric layer laminated using a polymer based adhesive
  - A sputter deposited and plated Copper metallization (4 µm to 15 µm thick) metal
- Laser patterned fine lines and space:
  - (48 µm line width/54 µm spacing/102µm pitch)

- Laser drilled or photodefined microvias:
  — (45 µm at top of via/25 µm width at bottom of via)
- Interconnect density of 1000 linear inches/inch^2 at 4 layers

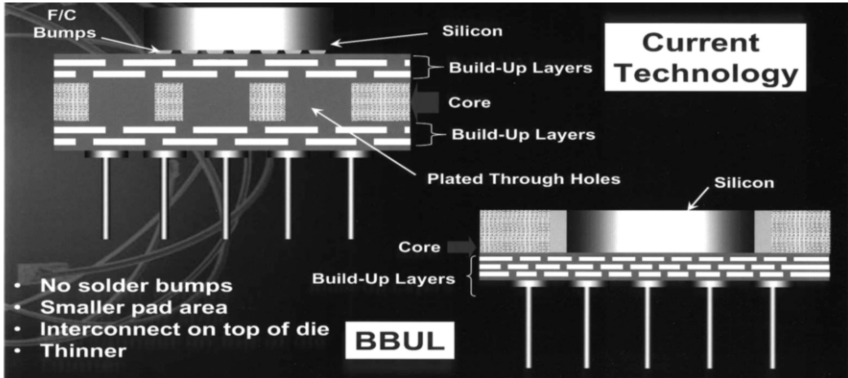

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Figure 12-23. Intel's Current Microprocessor Package and the BBUL

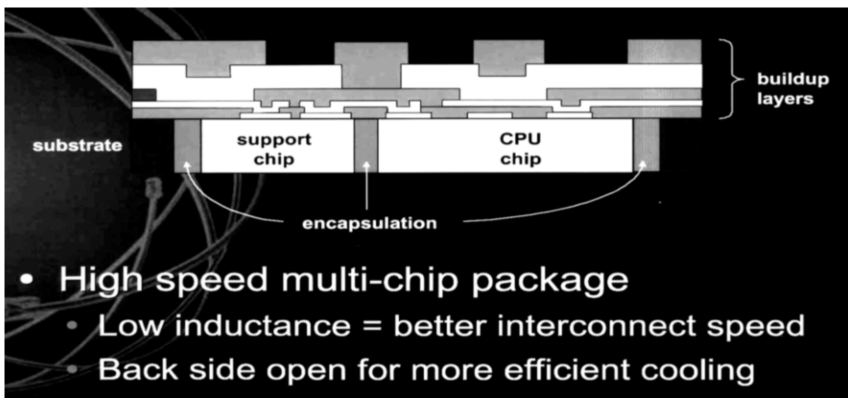

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Figure 12-24. Intel's Multichip BBUL

Note: Use of photolithographic processing using liquid PI or BCB in place of the Kapton™ and the laser lithography, offers the capability of thinner dielectric layers and finer lines and smaller microvias.

The "chips first" type of interconnect process has several features that may not be immediately apparent including close placement of die, and finally a readily achievable 3-D capability. The major concern with "Chip First" MCMs remains—the *lack of a reliable, low cost approach to rework, dictating the absolute need for KGD*.

The interconnect process technology itself, because it shares similar processes, may very well have a more significant value as a way of fabricating very high density interconnects for Level 1.5 COB/MCM-L and Level 2.0 COB/(HDI) PWBs.

12.6 — High Density Interconnects—Cost and Yield Considerations

The thin film process offers the interconnect wiring densities essential to support packaging and assembly needs of current and future ICs. It is the baseline process for flip chip bumping and for the manufacture of multilevel conductor interconnects supporting Level 1.0 WLP, SCP and MCP and Level 2.0 PWBs. It is ideal for wafer bumping and WLP, where yield loss is unacceptable. By applying applicable IC methodologies a "near defect-free" process can be configured and put in place. The particular needs are varied. Table 12-10 for example, lists the current patterning requirements, in terms of target line widths for Level 1.5 Multichip Package interconnects and Level 2.0 PWB, and process panel size. The IC is included for comparison purposes.

There are other differences however, between IC manufacturing and the manufacture of packages and interconnect substrates, in particular high I/O count BGAs, MCPs and HDI PWBs. A totally different scenario comes into play that must be addressed. Unlike an IC that is typically much less than 1-inch square, SCPs and MCPs are much larger in size and are manufactured on very large panels rather than wafers. For the PWB the panel size is larger. And like the IC, the cost to manufacture is obviously affected by the number of piece parts that can be processed on a given size wafer, substrate or panel. The more parts the lower is the cost per part. By the same token, the larger the piece parts the fewer parts per panel and the higher the unit cost.

The size of the individual part therefore is a critical factor that strongly influences achievable yields. Consider Figure 12-25, for example. It shows the effect a particular level of particulate contamination on the yield of parts of various sizes for a given size wafer/panel. The larger the part, the more susceptible it is to this type of contaminant. As a consequence, the need for "near defect-free" processing and a proper operating environment becomes even more critical and essential if acceptable yields are to be achieved.

The challenge therefore in manufacture of HDI substrates and PWBs in particular, is to put in place a manufacturing scenario that adequately addresses these concerns. To be critically reviewed are the following:

- Process Wafer/Substrate/Panel Size—Selection should be based on process equipment availability and the potential for the highest achievable yield. Large panel size offering large number of parts is not always the best solution.
- Incorporating high yield processes closely emulating the applicable IC photolithographic processes and procedures including as a minimum,
  - A contamination controlled cleanroom operating environment,
  - Hard surface glass masks,
  - Off-contact or projection printing.

Table 12-10. Patterning Requirements for Various Package/Substrate Interconnects

Packaging Technologies	Min. Feature Size (µm)	Typical Process Substrate Size [in Production] (~Square Inches)	Manufacturing Technology
Multichip Packaging	10–100	4–144	Thin Film
▪ WLP	10–25	6–12 inches (Diameter–Wafer)	Thin Film
▪ MCM-D	10–25	16–144	Thick Film Cofired Ceramic
▪ MCM-C	75–100	16–25	
Printed Wiring Board	25–100	100–700	Laminate
▪ SCP/HDI PWB	25–75	36–144	Laminate/But
▪ MCM-L/Adv PWB	75–100	400–760	Laminate
Integrated Circuit	*0.1–1.0*	*6–12 inches (Diameter–wafers)*	

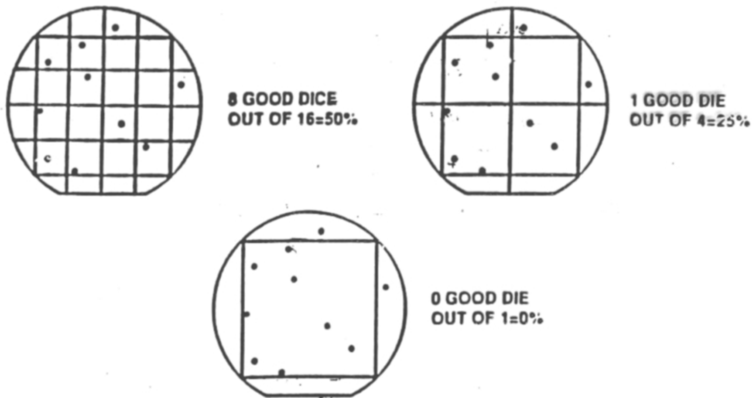

Figure 12-25. Substrate Size/Yield and Defect Density

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13 HDI Substrate Manufacturing Technologies: Thick Film Technology

13 — THICK FILM TECHNOLOGY

Early ceramic IC packages were manufactured using the thick film process for the metallization. A metal interconnect was selectively deposited onto a ceramic substrate by screen printing a patterned conductive paste or ink. A drying and firing of the patterned paste followed the screening. This same basic process, “print, dry, and fire” continues to be used today in the manufacture of much more complex multilevel conductor interconnect substrates for MCPs, in particular hybrids and MCMs. A MCP when manufactured using thick film processes is referred to as a MCM-C.

13.1 — The Thick Film Process

The thick film substrate manufacturing process for multilevel applications is a sequential build up process and is schematically detailed in Figure 13-1.

The entire process begins with selection of the substrate. The majority of applications call for inorganic substrates primarily ceramic because of the high process temperatures involved. The most commonly used substrates include aluminum oxide or alumina (Al_2O_3), clearly the most dominant, beryllium oxide (BeO), and aluminum nitride (AlN). The selection is based primarily on the end application. For example, if there are heat dissipation issues to be addressed, BeO and AlN would be preferred in deference to Al_2O_3. BeO offers high thermal conductivity while AlN has slightly lower thermal properties but a CTE better matched to silicon. A list of various ceramic and metal substrates with their respective thermal properties is shown Table 12-9 in the previous chapter.

Following substrate cleaning, the first conductor layer is processed through “print, dry and fire”. The drying is at 120ºC–150ºC. During the drying, solvents in the paste are removed. The firing is at 800ºC–900ºC. Both the drying and firing are in air. When the metal is copper however, the firing is in nitrogen.

The high temperature firing result in oxidation of the binders and subsequent bonding of the functional elements to the substrate and/or underlying layers i.e., conductors or dielectrics.

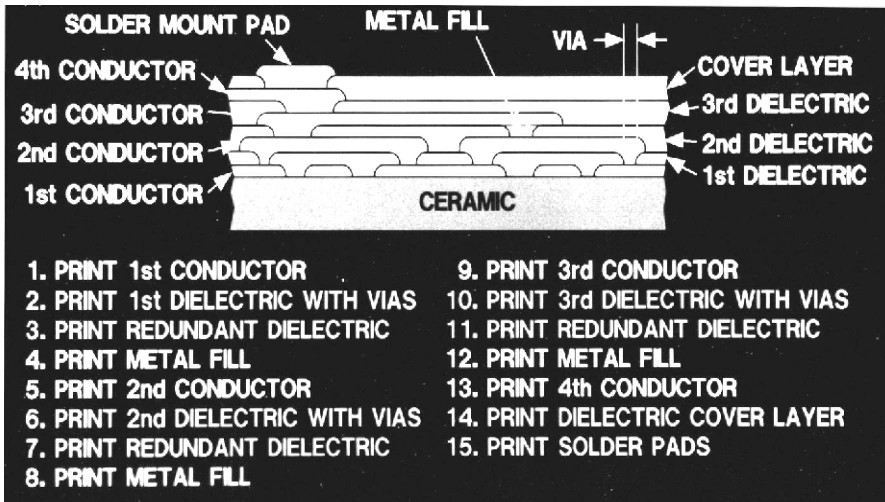


Figure 13-1. The Multilayer Thick Film Process Sequence

The first level metal and all subsequent metal layers are typically followed by a double “print, dry and fire” of dielectric layers, each patterned with vias in place. The vias allow connections to be made between two levels of metal. The intent of the double print is to provide a thicker layer and, more importantly, to minimize the possibility of pinholes in the initial dielectric that could result in shorting between the two conductor layers.

Following the double dielectric and prior to adding a second level conductor layer there is a via fill. A conductive metal is deposited into the vias dried and fired to help level the surface and improve contact of a second level metal to the first level metal. If two levels of metal are all that are needed a final top layer dielectric or glaze is deposited. The glaze is selectively deposited in a pattern that leaves the underlying metal exposed only in those areas where components are to be attached or interconnects.

13.2 — The Patterning Process

Fabrication of quality interconnects substrates (well defined features with tight tolerance) using thick film patterning results from selection of appropriate materials (pastes), tooling (screens) and equipment (printer), in combination with well-defined, well-controlled and monitored processes. The materials selection will be based, at least initially, upon the desired properties: for example. for a conductor, the conductivity and the method of component attachment, that is, solder attach or wire bonding. The screen and the printer are key to well-defined and repeatable patterns generation. The drying and firing parameters, usually those recommended by the paste manufacturer, complete the bonding of the various layers to the substrate and each other.

13.2.1 — Thick Film Pastes/Inks

Thick film pastes (or inks) are available as polymers, solders, or cermets. It is the latter, the cermets, that are the most widely employed in the manufacture of interconnect substrates.

Cermet pastes are available from several manufacturers in various formulations such as conductors, dielectrics (for use as insulators, passivation layers or encapsulants), and resistor materials. Thick film pastes are made up of two constituents, a functional part that establishes the print properties (conductor, or dielectric, etc.), and a vehicle part that imparts proper "rheology", that is, the flow properties, or "printability", of the paste.

Table 13-1 lists common thick film formulations. Monometallic conductor materials listed include gold, silver, and copper. With the very high solubility of gold and silver in solders, improved soldering can be realized by the addition of palladium or platinum to reduce very rapid "leaching" of both metals.

Variations in formulations will vary with suppliers. Pastes are normally manufactured and used as a set that is fully compatible with conductor, dielectric and resistor materials. The manufacturer will also recommend the process parameters to be followed. Pastes are also formulated specifically for use with different substrate materials.

Table 13-1. Most Common Thick Film Formulations

Conductor	Resistor	Dielectric	Green Tape
Au, Pt/Au	$Bi_2Ru_2O_7$	Glass	Glass-Ceramic
Ag, Pd/ Ag	RuO_2	Glass-Ceramic	
Ag/Pd		$BaTiO_3$	
Ag/Pt			
Cu, Ni			
Binder:	Glass: Borosilicate, Aluminum Silicate Oxide: CuO Mixed: Glass+Oxide		
Vehicle:	Volatile Phase: Terpineol Non-volatile Phase: Ethyl Cellulose		

13.2.2 — The Screen and the Screen Printer

The printing step is arguably the most critical, and the screen and the screen printer are certainly key factors in the quality of the deposited patterns for both conductors and dielectrics.

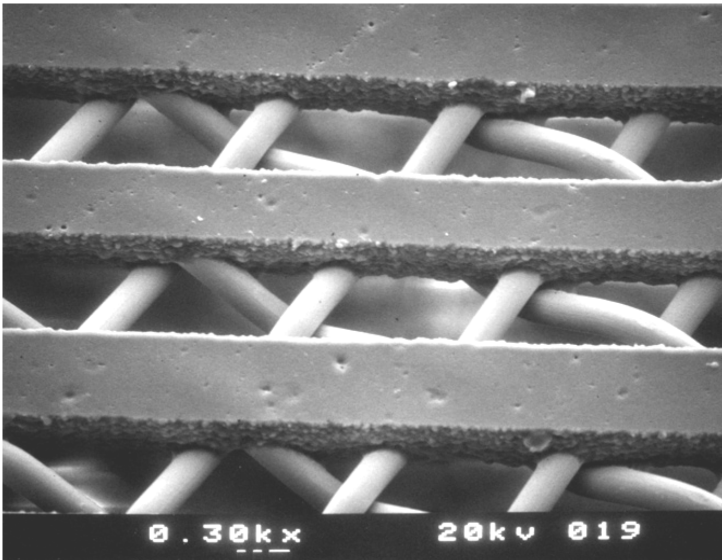
The screen is usually a stainless steel mesh that is first stretched and attached to an aluminum frame. A photosensitive emulsion is then applied to one side of the mesh and photolithographically patterned. The process removes emulsion in selected areas. A 50µm (2 mil) patterned emulsion on a 300 mesh screen is shown in Fig-

ure 13-2(a). Figure 13-2(b) is a fully patterned screen for printing onto a 4"x4" substrate.

The thickness of the deposited pattern will be determined by the combined thickness of the mesh, the emulsion and the particular paste. The thicker the emulsion the thicker the print will be. Similarly, different mesh size provides varying openings, which allow more or less material to be deposited.

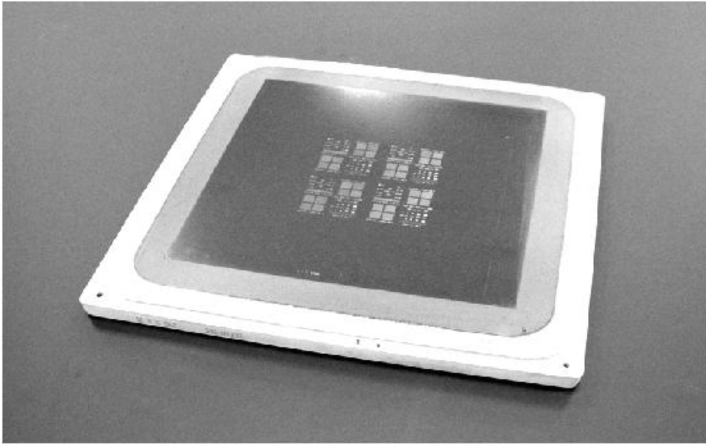
The emulsion thickness is typically 0.0004 inches. Thicker emulsion however limits the minimum line width meaning thicker but wider traces. Fine lines require thinner emulsion, which unfortunately results in thinner conductor material as well.

The printing process is illustrated graphically in Figure 13-3. The paste is applied to the top of the screen and using the squeegee, forced through openings in the screen wherever there is no emulsion. The paste is thus deposited onto the substrate in the desired pattern.



(Courtesy SEFAR Printing Solutions, Inc.)

Figure 13-2(a). Photo-Patterned Emulsion (2 mils l/s) on 360 SS Mesh



(Courtesy SEFAR Printing Solutions, Inc.)

Figure 13-2(b). Fully Patterned Screen

Figure 13-4 is a manually operated screen printer showing the screen and "squeegee". The substrate is not shown but would be in place directly under the screen. Using micrometers the screen is centered onto the substrate or aligned to a previously deposited pattern.

The process has many variables that together influence the end result. In the case of a conductor trace, it is the correct thickness and conductivity or sheet resistance that is critical. Figure 13-5 illustrates the printing process and the variables that need monitoring on a real time basis.

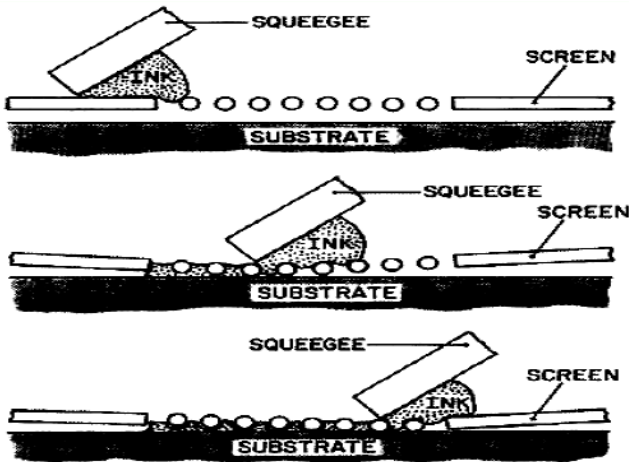
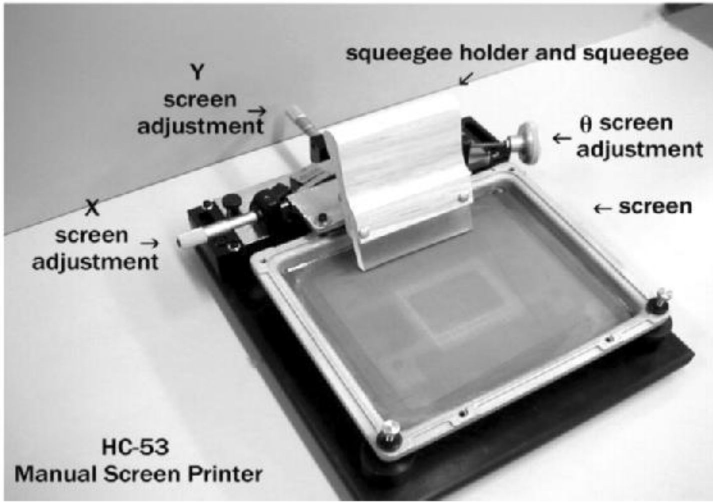


Figure 13-3. Screen Printing Process [1]



(Courtesy Affiliated Manufacturers, Inc.)

Figure 13-4. Manual Screen Printer

Screen printing is both a science and an art. Process parameters are for the most part determined empirically by highly skilled technicians. These parameters once established are transferred to the printer operator, who provides the necessary assistance needed to maintain process settings and insure quality performance. Semi-automatic and fully automatic screen printers (Figure 13-6) together with experienced operators can provide the process controls and monitoring that are essential to support high volume production.

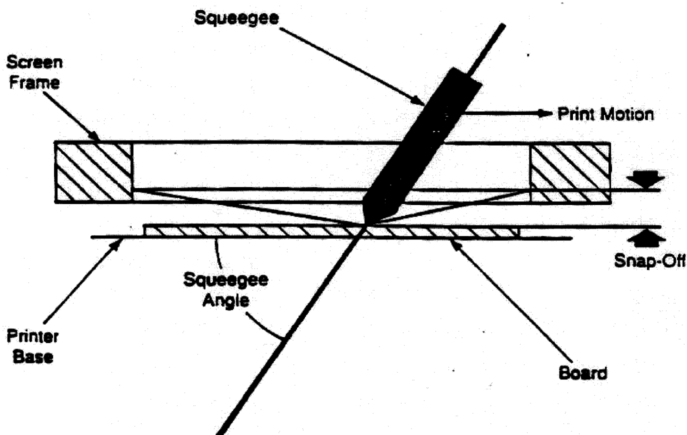


Figure 13-5. Thick Film Printing Variables Requiring Monitoring

(Courtesy Affiliated Manufacturers, Inc.)

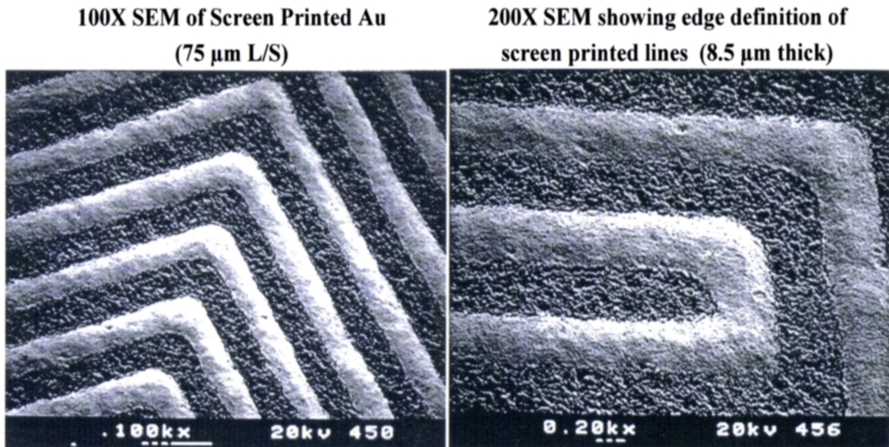
Figure 13-6. Automatic Thick Film Screen Printer

13.3 — Thick Film Screen Printing and MCM-C/HDI

High I/O count ICs with increasing functionality require substrate interconnects and packages with very high wiring densities achieved with finer lines and spaces and equivalent size vias. Current screen printing technology has limitations in addressing these needs. Ideally, conductors should have high conductivity, sharp edge acuity, straight-sided walls and smooth surfaces.

The quality of screen printed patterns, conductor in particular, is generally poor in edge acuity; exhibit slopping sides, and with a rough surface finish. Edge acuity is a reflection of both the screen and the substrate surface. Poor surface finish results from the paste, in particular particle size, and the screen mesh. Typical thick film conductor traces exhibit tapered edges as a result of the screen printing and the flow properties of the paste. Figure 13-7 are examples of screen printed thick film conductors exhibiting sloping sides and poor edge acuity.

In a production mode screen printing is currently limited to 3 mil minimum lines and spaces, and 8 mil diameter vias on substrates that are generally no larger than 4"x4" in size. For very high wiring densities, as needed in most high-performance MCM-C applications, inability to pattern finer lines and spaces must be compensated for by adding more layers. However, more layers mean more prints and more high temperature firings. Unfortunately, as the number of layers increase, yields tend to



(Courtesy Heraeus CMD)

Figure 13-7. Screen Printed Thick Film Au Conductor trace

decrease, due in part to problems relating to increasing substrate camber (warpage) and poor surface topography hampering the subsequent printing processes.

However, some rather high-density interconnect boards have been successfully manufactured in a high volume mode. Figure 13-8(a), for example, shows a multilayer interconnect board (MIB) that is 4"x6" that contains over 20 thick film copper conductor layers. These Al_2O_3 ceramic boards were used in place of an organic PWB on several military programs to take advantage of the better thermal properties of ceramic and to provide a better CTE match with the leadless ceramic chip carrier packages. Figure 13-8(b) shows a MIB circuit board with surface mounted ceramic chip carriers.

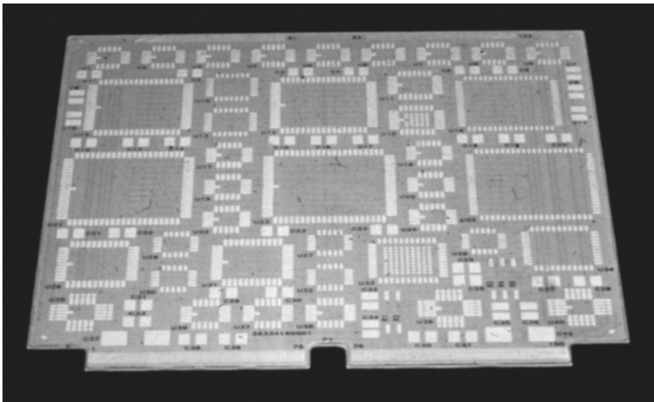
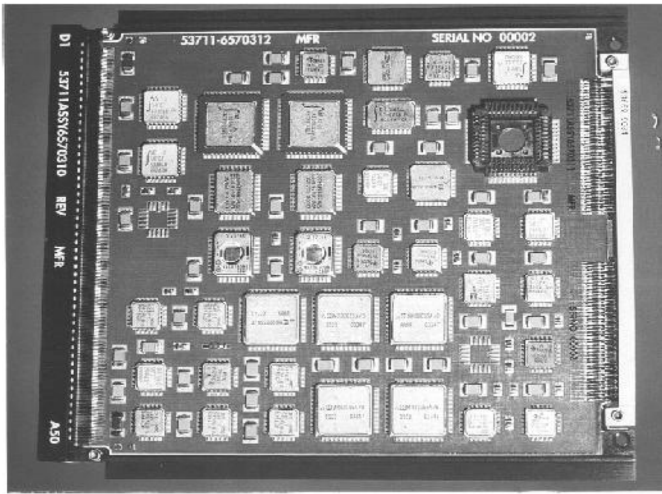


Figure 13-8(a). Thick Film Multilayer Interconnect Board (MIB)



(Courtesy Hybrid Sources Inc.)

Figure 13-8(b). Cofired Ceramic MIBs Populated with Ceramic Chip Carrier Packages

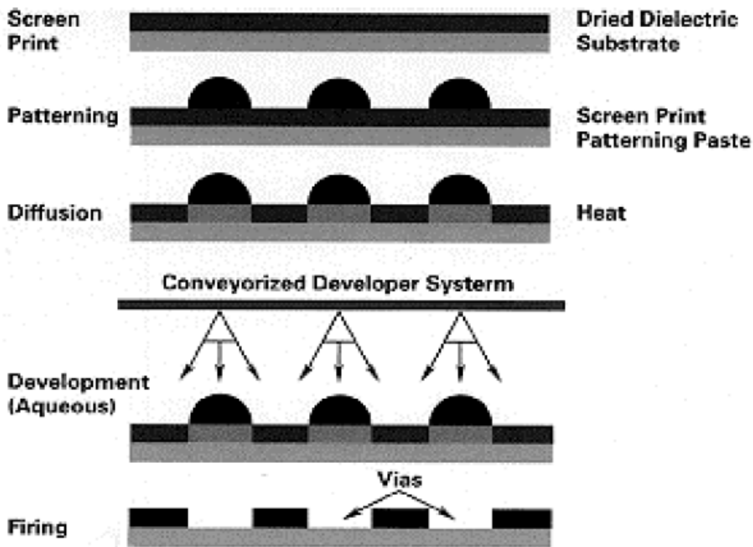
13.4 — Advanced Thick Film Patterning Processes

Development efforts are on-going, directed towards achieving finer lines, a reduction in via size and an overall improvement in the quality of screen printed thick film conductors and dielectrics. Recent advances in both screen technology and ultra fine particle conductor pastes have resulted in achieving finer lines and spaces as small as 2 mils. In addition new materials and processes have been introduced that provide a significantly higher level of patterning capability. Specifically, they include a process developed by Dupont called Diffusion Patterning™ and use of photodefinable or photosensitive materials that are patterned by applying conventional thin film processes.

13.4.1 — The Diffusion Patterning™ Process

Diffusion Patterning™ addresses the smaller thick film dielectric via issue specifically. It is an "imaging" process, shown graphically in Figure 13-9, that provides vias as small as 125 microns in diameter.

A screen printed "image paste" is deposited onto a previously deposited and dried dielectric layer wherever a via is required. During a heat treatment the "imaging paste" diffuses into the dielectric increasing the solubility of the dielectric in an aqueous developer solution. Vias so generated are more reproducible resulting in much higher yields than realized with standard screen printing. A minimal capital investment covering acquisition of a conveyorized or batch type developer station is all that is required to implement into the current thick film manufacturing line.



(Dupont Microcircuit Materials)

Figure 13-9. Diffusion Patterning ™ Process

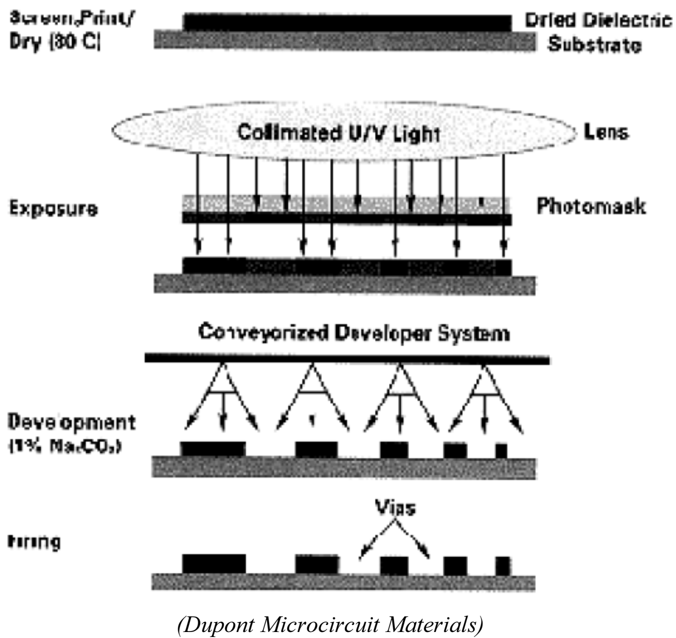
13.4.2 — Photosensitive/Photodefinable Thick Film Patterning

Continuing developments in thick film paste directed specifically to finer lines and smaller vias resulted in the introduction of both photodefinable and photosensitive materials and processes.

The photodefinable process uses a screen printed and fired blanket layer of thick film conductor or dielectric. The layer is patterned by first applying a photoresist film, exposing it to a UV light source through a photomask, developing, and finally chemical etching of the material using the resist film as an etch mask.

By adding a photosensitizer to the conductor or dielectric paste the process is greatly simplified and use of a photoresist is completely eliminated. The screen printed and dried paste is patterned again by exposure to a UV light source followed by development of the pattern in an aqueous solution. The patterned paste is then fired to complete the process. The process flow for a photosensitive dielectric paste is shown in Figure 13-10. Figure 13-11(a) and (b) are SEMs of a photo-patterned via and conductor traces. Note the very sharp edge definition in contrast to the screen printed lines shown previously in Figure 13-7.

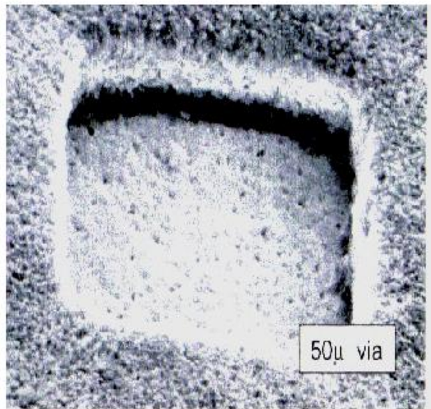
As is seen in the SEMs the process is capable of 25μm lines/spaces and 50μm vias. To implement, the capital investment is somewhat higher in cost. In addition to a developer station, a mask aligner/exposure system is also required. The cost for the latter can range anywhere from $50,000 to more than $100,000 (proximity printer vs. projection aligner).



(Dupont Microcircuit Materials)

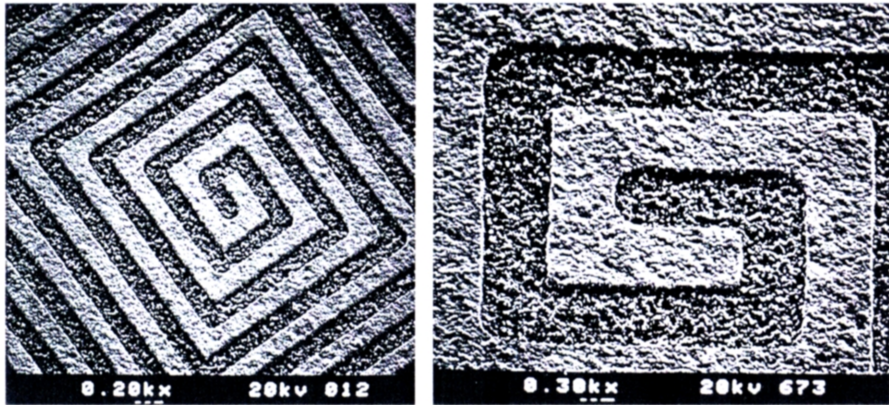
Figure 13-10. Dupont Fodel® Photosensitive Thick Film Paste Processing

Both the photodefinable and the photosensitive thick film materials are available from several paste manufacturers. These include Dupont, whose materials are marketed under the name Fodel®, and Heraeus' KQ product line.



(Courtesy Heraeus CMD)

Figure 13-11(a). Photo-Patterned 50 um Via in Thick Film Dielectric



(Courtesy Heraeus CMD)

Figure 13-11(b). Photo-Patterned Thick Film Au Conductor Traces; Left: 28 um lines, 22 um spaces; Right: 50 um lines, 4.5 um thick

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14 HDI Substrate Manufacturing Technologies: Cofired Ceramic

14 — THE COFIRED CERAMIC TAPE TECHNOLOGY [1]

Much of the early work that eventually lead to the introduction of cofired ceramic technology as a viable microelectronic packaging technology took place at RCA in Somerville, NJ. A patent (3,192,086) for monolithic tape cast ceramics was issued in 1965 to W. J. Gyurk. A second patent (3,189,978) "Method for Manufacturing Multilayer Circuits" was issued to H. W. Stetson in the same year. Both were assigned to RCA. Basically, the patents define the cofired ceramic processes used in the manufacture of semiconductor packages both past and present. Figure 14-1 is taken from the Stetson patent.

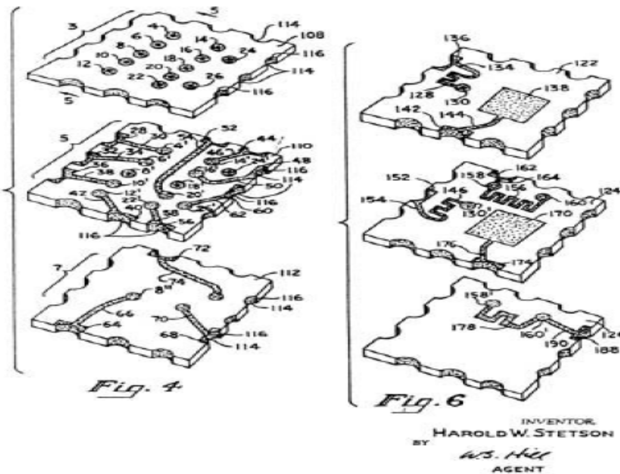


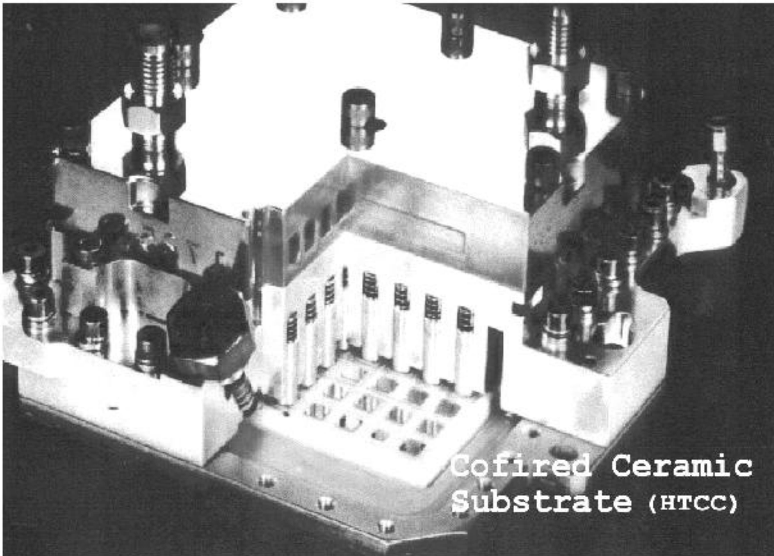
Figure 14-1. Patent on Cofired Ceramic Manufacture Issued to Harold W. Stetson, RCA

A co-worker of Gyurk and Stetson, Bernard Schwartz, who was a major contributor to the development of the technology, left RCA to join IBM. At IBM, he was instrumental in the introduction of the cofired ceramic tape process and largely responsible for its implementation and subsequent enhancement as a premiere

packaging technology. At IBM all packaging activities were directed towards supporting their microelectronic and computer programs, in particular, their mainframe computers, today's servers. The cofired technology, specifically, addressed high-performance multichip packaging, employing high-density multilayer cofired ceramic interconnect substrates and flip chip assembly.

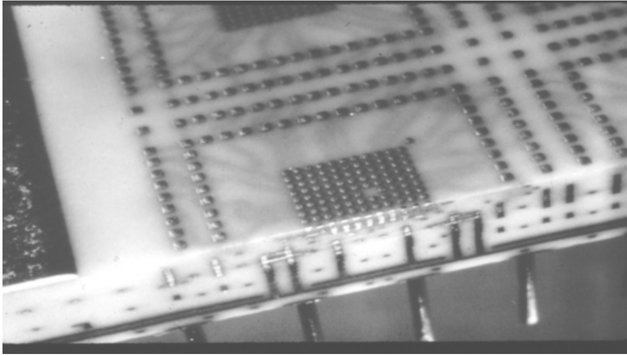
14.1 — IBM's Multilayer Interconnect (MLI) Packaging Program [2,3]

IBM developed an exceptionally high level of expertise to support their packaging programs. By the 1970s, they developed a high volume cofired ceramic tape manufacturing capability that produced package-interconnect substrates accommodating in excess of 100 flip chip devices. In the early 1980s they announced the Thermal Conduction Module (TCM), the processor unit for the IBM 3081 computer. The TCM is shown in Figure 14-2(a). It was slightly over 3"x 3" and contained 33 layers of conductor/dielectric. Conductor metallization was tungsten and the dielectric Al_2O_3. The top layer tungsten was overplated with nickel and gold to accommodate flip chip solder attachment. With 118 flip chips, each with 121 I/Os assembled to this interconnect package substrate. it clearly represented the most complex and functionally dense interconnect substrate package in the industry. A metallographic cross-section of the substrate is shown in Figure 14-2(b).



(Courtesy IBM Corp.)

Figure 14-2. (a) IBM Thermal Conduction Module (TCM)



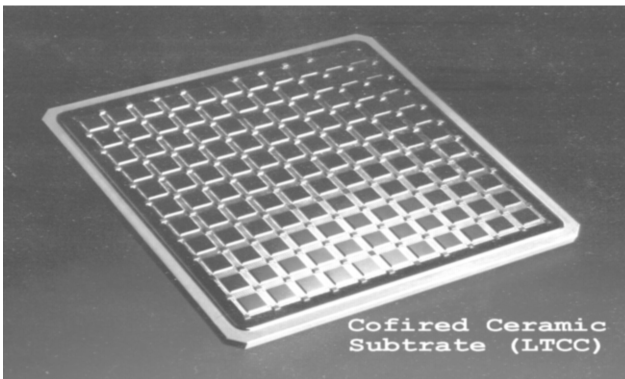
(Courtesy IBM Corp.)

Figure 14-2(b). Cross-Section of TCM Ceramic Substrate Interconnect

The next generation TCM, which appeared in the late 1980s, is shown in Figure 14-3(a). It was approximately 5"x 5" and had over 60 conductor/dielectric layers. The conductor metallization was high conductivity copper. Again the top layer was nickel and gold overplated. The dielectric was cordierite, which has a TCE more closely matched to silicon. There were121 flip chip ICs attached each with over 600 I/Os.

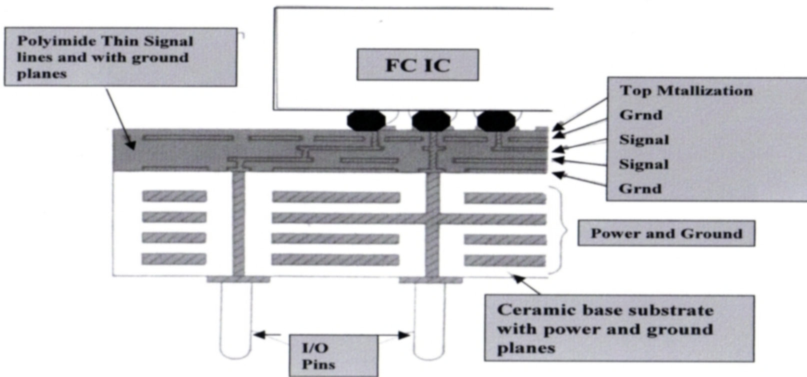
In order to more effectively and efficiently handle the wiring density required and to accommodate high I/O count IC flip chip assembly, two signal layers of thin film conductor/dielectric were added as illustrated in Figure 14-3(b).

IBM nurtured the technology and demonstrated manufacturability with widespread implementation. In doing so, IBM established an invaluable reliability database for both flip chip and cofired ceramic packaging.



(Courtesy IBM Corp.)

Figure 14-3(a). Next Generation TCM



(Courtesy IBM Corp.)

Figure 14-3(b). A Cofired Ceramic Package with Thin Film Signal Layers and Top Layer Metallization

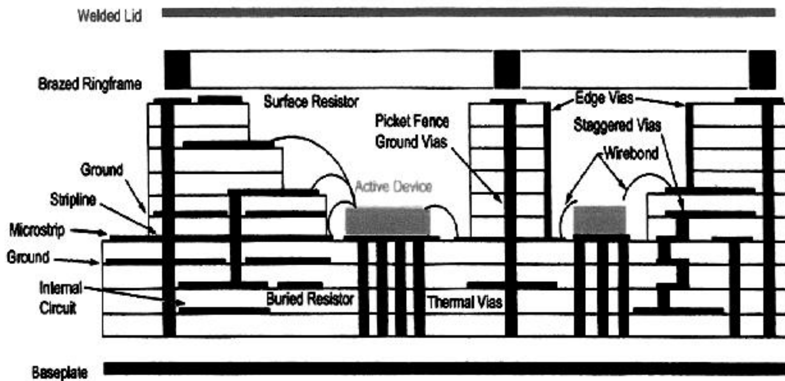
14.2 — The Co-fired Ceramic Technology [4,5]

The thick film "print, dry and fire" dielectric process presented several problems including the need for double processing to compensate for pinholes, and an inability to produce well defined vias much less than 10 mils in diameter. The cofired ceramic tape process is based on the use of an "unfired" or "green" ceramic tape (Figure 14-4) that upon firing will serve as the inner layer dielectric. The cofired process essentially replaces the thick film dielectric with a thick ceramic layer that is "pinhole-free" and has extremely well defined and reproducible vias (and cavities) produced by punching or mechanical or laser drilling.

(Courtesy Heraeus CMD)

Figure 14-4. Unfired ("Green") Ceramic Tape

The process is similar to that used in the manufacture of a multilayer PWB with individual layers being processed separately, then collated, stacked, and fired The result is a monolithic, multilayer, multilevel interconnect structure offering many options, such as cavities to accommodated active devices, seal rings for providing hermetic cavities, pins/leads for attachment at the next level, and embedded passives. One such structure is schematically illustrated in Figure 14-5.



(Courtesy American Technical Ceramics)

Figure 14-5. Cofired Ceramic Optional Instruction Features (LTCC)

The conductor patterning, for each of the layers and the via fills, is primarily by screen printing and is performed on the "green tape".

Another key feature of the cofired ceramic tape process is that it is a "parallel process" with each layer processed separately as opposed to the thick film "sequential process". This allows each layer, covering via generation, via fill and conductor patterning to be individually inspected for defects prior to moving to the next step. Defective layers can therefore be readily removed and replaced.

14.3 — The Cofired Ceramic Tape Process

The ceramic tape process is described in Figure 14-6. The post firing process step includes adding seal rings and I/O pins and plating as needed.

The cofired ceramic process is extremely flexible providing a variety of multilevel interconnect boards or complete interconnect substrate/packages supporting SCP and MCP.

14.4 — High Temperature Cofired Ceramic HTCC

There are two cofired processes: a high temperature and a low temperature. The High Temperature Cofired Ceramic or HTCC process has been in place since the 1970s. HTCC has been the process used for the manufacture of most single chip ceramic packages beginning with the DIP and the PGA. With HTCC, the "green" ceramic,

most commonly aluminum oxide, (but can also be beryllium oxide, or aluminum nitride) is fired at 1440ºC to 1880ºC. Because of this high process temperature, the available conductor metals are limited to the refractory metals, namely tungsten, molybdenum, platinum and palladium. And, since they readily oxidize the firing is in an inert or reducing atmosphere.

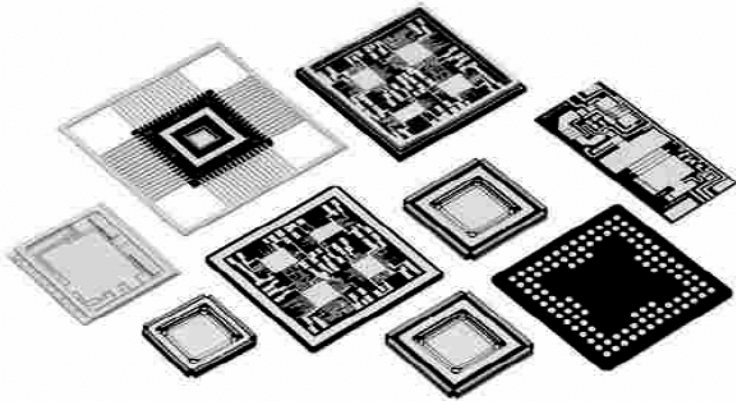
(Courtesy American Technical Ceramics)

Figure 14-6. The Cofired Ceramic Tape Process

Refractory metals however, are also very poor conductors. As a consequence, in a post-firing step the top surface traces are overplated with nickel and gold to enhance component attachment and interconnects. Figure 14-7(a) shows single chip and multichip cofired ceramic packages ready for component assembly and hermetic sealing. Figure 14-7(b) is a Level 2 HTCC multilayer interconnect board with seal rings in selected areas for hermetic sealing.

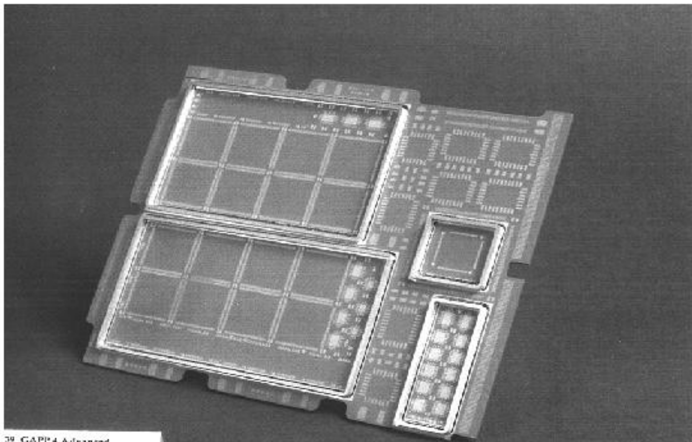
14.5 — Low Temperature Co-fired Ceramic LTCC [6,7]

The Low Temperature Cofired Ceramic, or LTCC process was introduced in the late 1980s. The LTCC process offers many of the same features as the HTCC process but uses firing temperatures of 850ºC to 1000ºC. This is quite significant since the lower temperature allows for the incorporation of the same high conductivity conductor metals used for thick film, notably silver, copper, and gold. Figure 14-8 shows a variety of SCPs and MCPs that are manufactured using the LTCC process.



(Courtesy Polese Inc.)

Figure 14-7(a). HTCC Hermetic Single and Multichip Packages

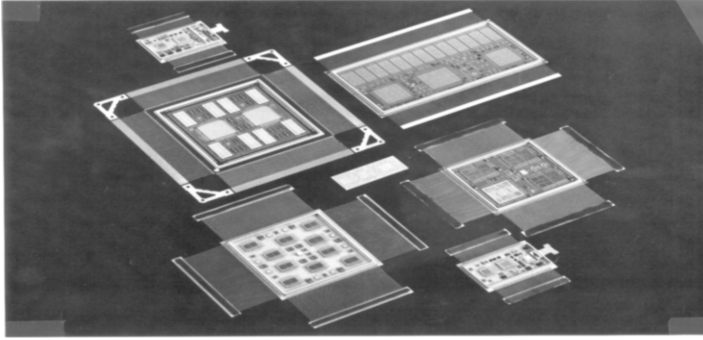


(Courtesy Lockheed Martin)

Figure 14-7(b). HTCC Multilayer Interconnect Board with Select Areas for Hermetic Sealing

14.6 — Comparing Thick Film, HTCC and LTCC

Materials usage for HTCC and LTCC and their properties are shown in Table 14-1. Table 14-2 summarizes the advantages and disadvantages of HTCC vs. Thick Film and LTCC vs. HTCC.



(Courtesy CTS Microelectronics)

Figure 14-8. LTCC Multichip Packages

Table 14-1. Cofired Ceramic Materials and Properties [10]

	LTCC	HTCC
Dielectric/Ceramic	A. Cordierite MgO, Sio2, Al2O3 B. Glass/Al2O3 Mixtures SiO2, B2o3 glass PbO, SiO2, B2O3, CaO glass C. Crystalizable Glass/Ceramics Compounds from Alkaline Earths, SiO_2, Al_2O_3 Phase Diagrams	Al2O3 BeO AlN
Firing Temp	850–1000ºC	1450–1880ºC
Conductors	Au, Ag, Cu, Pd/Ag	W, Mo, Pt, Pd
Conductor Resistivity	1.6–2.3 µΩ-cm	5.5–21 µΩ-cm
Dielectric Constant	3.5–9	7–10
Tf (ppm/ºC)	15 to 0 to –56	–50–100
Dielectric Loss (Q)	500–1400	500–10,000
Dielectric CTE	3–7 ppm/ºC	3.3–7 ppm/ºC
Thermal Conductivity	2–6 W/m-ºK	15–240 W/m-ºK
Cofire Resistors	10,100, 1,000 Ω/sg.	N/A
Cofire Capacitors	K = 8–40	N/A

14.7 — Advanced LTCC Processes [8,9]

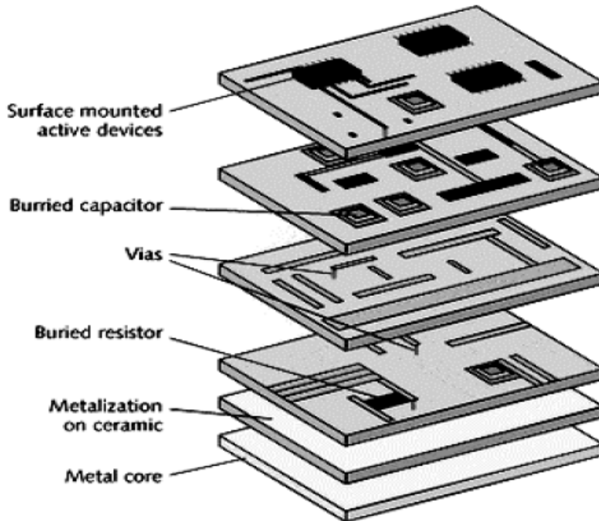
A potential impediment to achieving high yield cofired ceramic high density interconnect boards with 25–50μm lines/spaces and vias is the shrinkage factor experienced with the cofired tape processes. Ceramic tape following firing normally undergoes dimensional shrinkage in all three axis, x, y, and z. The shrinkage varies on a lot-to-lot basis from 10–16% depending upon the final composition of the ceramic. While the shrinkage can be determined for each lot, it becomes more critical as the feature sizes decrease and the substrate or panel sizes increase. It must also be taken into consideration in the initial design of the circuitry since the position of the "as printed patterns on" the unfired tape will be different after the tape is fired.

Table 14-2. Advantages/Disadvantages Thick Film, HTCC, LTCC [10]

Technology	Advantages	Disadvantages
Thick film	High conductivity metals Wire bondable/solderable metals Internal passives Low temperature firing Lowest capital investment	Multiple printings Multiple firings Sequential process
HTCC	Mature process Established reliability database Parallel process Single firing Punched vias Thick dielectric Improved print resolution Smooth planar surface	High firing temperature Low conductivity metals Highest capital investment
LTCC	Parallel process Thick dielectric Punched vias Single lower firing temperatures High conductivity metals Wire bondable/solderable metals Internal passives Lower capital investment	Lower thermal conductivity

Several modified processes have been introduced to address this particular problem. All involve constraining the tape during the firing step by mechanical means, use of a sacrificial layer, a fired ceramic or metal substrate. An example of

the latter is shown schematically in Figure 14-9 in which the process begins with a metal substrate that serves as the constraining medium. Referred to as LTCC-M, it not only reduces x-y shrinkage but also offers an excellent platform for applications requiring thermal management.



(Courtesy Lamina Ceramics, Inc.)

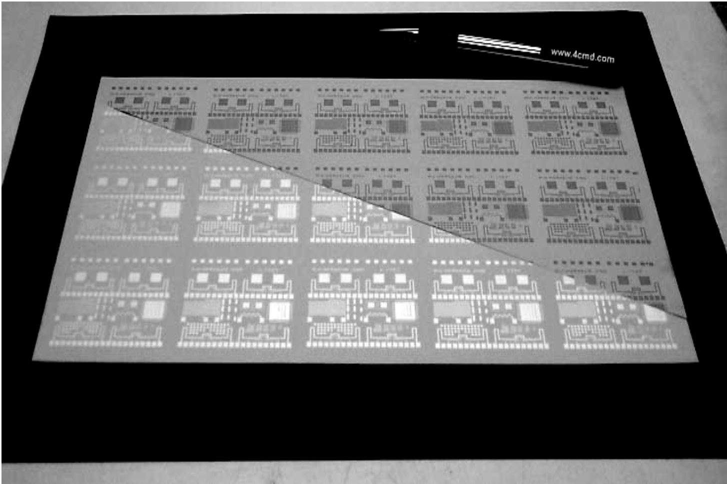
Figure 14-9. LTCC-M, A Constrained Cofired Ceramic Tape Process

While constraining processes are effective in reducing the shrinkage to varying degrees, a recently introduced self-constrained LTCC tape, called Heralock™, from Heraeus CMD, offers near-zero shrinkage. Heralock™ eliminates the need for a constraining medium. It densifies in the z-direction but most importantly less than 0.2% in the x-y directions and extends LTCC processes to significantly larger area substrate applications.

Self-constrained LTCC offers the following benefits:

- Design Flexibility—1:1 Design Rules with "Print to Fired" feature dimensions the same.
- Process Simplicity—Achieves "near-zero" shrinkage without external constraints. Layer to layer alignment accuracy significantly enhanced.
- Overall Process Improvement—
  - — Allows for large area substrates/panel formats
  - — Camber free
  - — Minimizes rejects (misalignments, etc.), increases yields.
- All of the above contribute heavily to significant cost savings.
- Figure 14-10 shows a 7"x 11" panel manufactured using Heralock™ LTCC tape.

Self constrained tape is also available from other suppliers including Dupont and Ferro.



(Courtesy Heraeus CMD)

Figure 14-10. Large Area Panel (7"x 11") Using Heralock™ Self-Constrained LTCC Tape

14.8 — Summary Co-fired Ceramic Process Technologies

In general the cofired ceramic tape technology, both HTCC and LTCC, has several outstanding features that include:

- Thick, "pinhole-free" inner dielectric layers
- Reproducible and well-defined punched, mechanical or laser drilled vias
- Unfired tape can be readily cut allowing for embedded cavities
- Totally amenable with in-process inspections
- A single firing (does however, require a multiple stepped ramping temperature profile)
- Upon firing the stack becomes a monolithic structure with a hermetically sealed embedded conductor network
- Excellent planar top and bottom surface topography
- A top and bottom surface available for component assembly
- Excellent surface metallization, typically nickel-gold plating, for wire bonding/flip chip and component solder attachment
- An integrated package providing complete hermeticity for both interconnect and components
- Allows for large area substrate/panel formats

- And finally, a more cost-effective packaging technology with the introduction of the LTCC self-constrained tape and the elimination of the "shrinkage problem" simplifying design and allowing larger size substrates to be processed

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15 Substrate Manufacturing Technologies: Organic Packages and Interconnect Substrate

15 — THE LEVEL 2.0 PRINTED WIRING BOARD [1,2]

The organic based PWB has been and continues to be the key "enabler" within the interconnect hierarchy that is electronic manufacturing. It is clearly the most dominant Level 2.0 interconnect substrate and is found in most electronic products. Historically, extensive use of organic substrates began during World War II. Obviously its complexity as an interconnect substrate has increased significantly over the years.

The traditional PWB is basically an organic substrate with a copper foil clad on one side or both sides of the board. The clad copper is patterned or circuitized using the photoresist/subtractive etching process. Early PWBs were simple single layer conductor boards. Later, double-sided PWBs with conductor traces on both sides of the board were introduced. Top and bottom layers were interconnected using wires or metal clips inserted into through holes drilled into the substrate. These boards served exclusively as the Level 2.0 interconnect through the 1950s and into the late 1970s at which time the multilayer PWB appeared. Double sided multilayer boards (MLB) contain three or more conductor levels, consisting of the two outer layers and x-number of inner layers totally embedded within the substrate. The key to this technology was the plated through-hole (PTH). First mechanically drilled then plated, the PTH provides connection to the various embedded inner layer conductor circuitry. A PTH is illustrated graphically in Figure 15-1(a). A metallurgical cross-section of a PTH via is shown in Figure 15-1(b).

The PTH at the time, represented a major advance in interconnect technology offering a very significant increase in the achievable wiring density. This in turn meant the availability of Level 2.0 PWBs having the capability for accommodating a considerable higher number of components and increased levels of functionality.

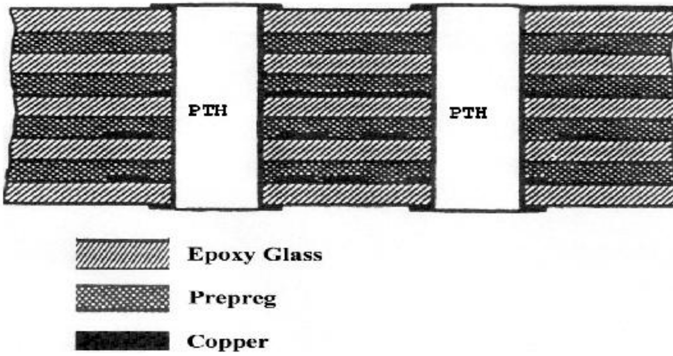


Figure 15-1(a). Multilayer PWB with Plated-Through Holes

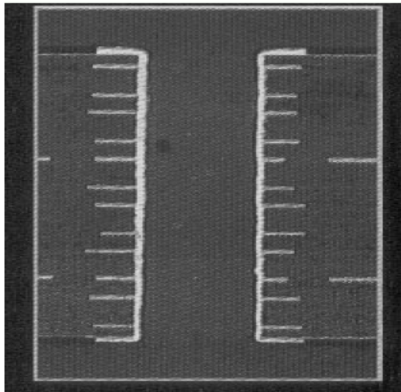


Figure 15-1(b). Plated Through-Hole Via

Further developments that followed included:

- An increase in availability of a variety of organic materials (See Tables 15-1 and 15-2),
- Increased process panel sizes as large as 24 inches by 32 inches; Note: Larger panels allowes more parts to be processed simultaneously, with subsequent reduction in the cost of individual parts,
- A continuing move to smaller lines and spaces (10/10 mils lines/spaces to 8/8 to 4/4)—to provide increased wiring density, and
- Introduction of smaller diameter PTH vias (20 mils to 10–12, to 6–8) as well as blind and buried vias (mechanically drilled) that further increased wiring density.

In general, PWBs can be classified based upon structure and manufacture into three distinct groups:

- Conventional PWBs—single, double sided and multilayer structures with mechanically drilled or punched PTHs to connect multiple inner layer conductor circuitry.
- Advanced PWBs—refers specifically to multilayered structures with mechanically drilled or punched blind, buried, and PTH vias, with diameters >150µm (6 mils).
- HDI PWBs—multilayered structures with blind, buried, and PTH, microvias with diameters <150µm, and generated by non-mechanical processes.

Table 15-1. Typical Electrical Properties of Some Laminate Materials [2]

(Dielectric Constant Typical 50%–60% Resin Content @100ºC)

Material Type	Dielectric Constant: 1 MHz	Dielectric Constant: 10 MHz	Dielectric Constant: 100MHz	Dissipation Factor
Epoxy Glass	4.5	4.3	4.2	.020–.025
Polyimide Glass	4.0	3.9	3.95	.010–.012
Polyimide Film	4.0	3.7	3.6	.020–.030
Bismaleimide Triazine Glass (BT)	4.2	4.1	4.0	.011–.013
Cyanate Ester	3.5	3.4	3.2	.005–.007

Table 15-2. Typical Thermal Properties of Some Laminate Materials [2]

Material Type	Glass Transition Temp (ºC)	Thermal Conductivity (BTU/(hr)(ºF)
Epoxy Glass	145	.25
Polyimide Glass	260	.30
Polyimide Film	40	.13
Bismaleimide Triazine Glass (BT)	185	.25
Cyanate Ester Glass	245	.25

15.1 — Overview of Conventional MLB Processing [3–5]

The conventional MLB is fabricated using a lamination process and mechanically drilled through-hole vias and electroless and electrolytic copper plating. Inner layers, composed of an organic core with an adhesively bonded (clad) copper foil are individually patterned, analogous to the cofired ceramic tape process. The clad copper is typically 1.4 mils (1.0 oz) or 2.8 mils (2.0 oz.) thick and is photo-patterned using subtractive etching. See Figure 15-2.

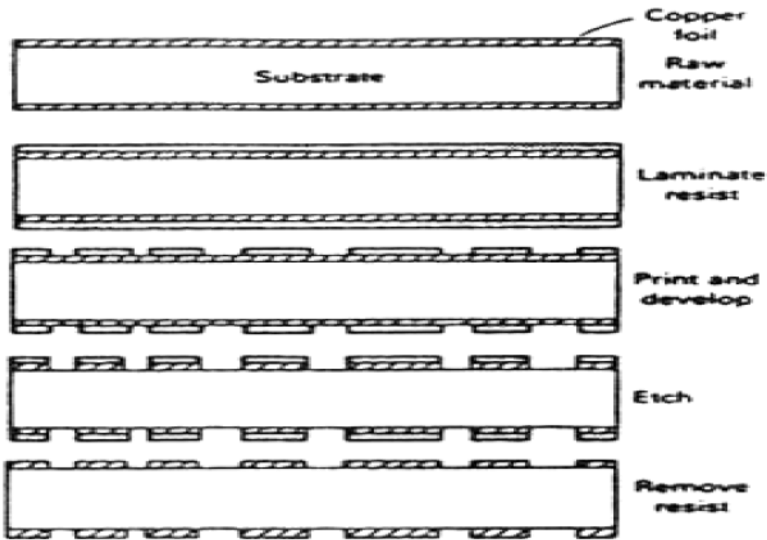


Figure 15-2. Inner Layer Patterning Process Sequence [2]

The two outer layers, top and bottom, also with copper cladding but non-circuitized, are combined with the inner layers collated and stacked in proper sequence, with each layer separated by a film of adhesive (pre-preg). Finally the stack is laminated under pressure and temperature (~150ºC) forming a monolithic multilayer conductor interconnect structure.

Following lamination, through-hole vias are mechanically drilled, cleaned ("desmeared") and plated to a specified final thickness. The subtractive etching process then patterns both outer layers.

The top layer and/or bottom circuitry may require additional plating, such as solder, nickel-gold, tin, or silver, depending upon the subsequent component attachment processes.

15.2 —The PBGA and the MCM-L

In the mid 1980s driven by potential cost reduction, the PWB laminate process drew the interest of both semiconductor and hybrid circuit manufacturers for use as an alternative technology for substrate and package covering both single chip (PPGA, PBGA) and multichip applications (Hybrids, MCM-L). The traditional laminate PWB process with very large panel sizes yields significantly more circuit substrates or packages than can be realized with ceramic-based technologies. More parts per panel meant lower unit cost. As a result a paradigm shift occurred with packages moving from ceramic to organic, primarily with the high volume, cost-sensitive products and the emergence of the PBGA and the laminate MCM-L. Figure 15-3(a) is a schematic of the typical PBGA. Figure 15-3(b) shows a strip of PBGAs prior to assembly and after die attach, epoxy molding, and singulation.

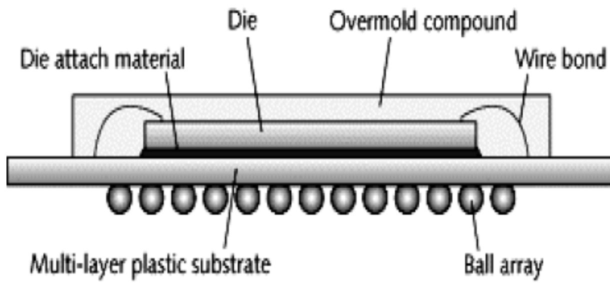
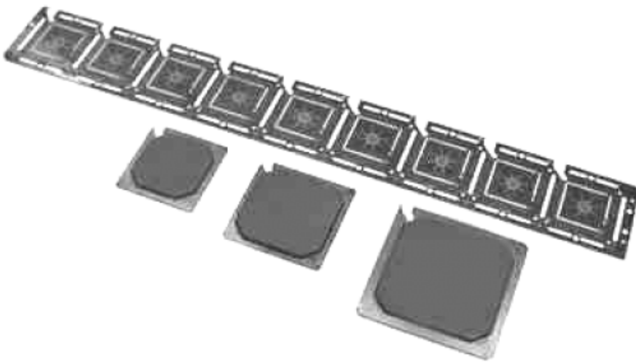


Figure 15-3(a). Schematic Plastic BGA

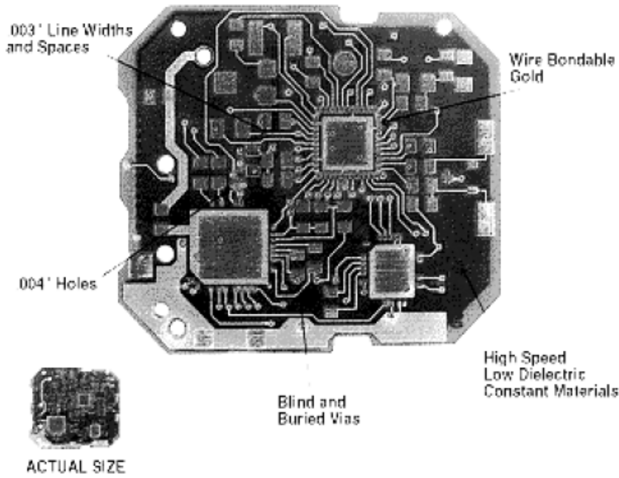


(Courtesy Marjelac Technologies)

Figure 15-3(b). PBGAs in Strip Format and After Epoxy Molding/Singulation

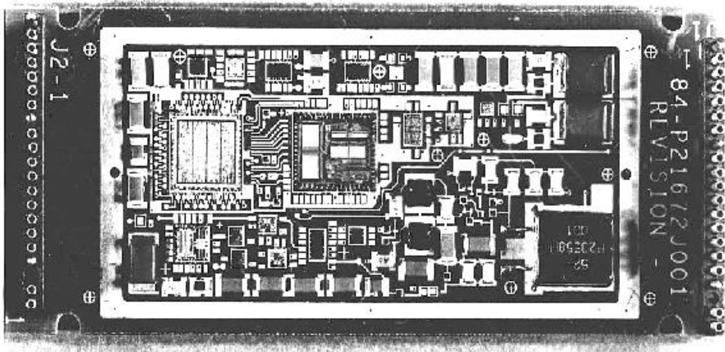
15.3 — Impact of the IC on Packaging and Interconnect Technology [6,7]

Addressing IC I/O count and the need for increased wiring density for both SCP and MCM-L applications can be achieved through reduction of line width and spacing and the implementation of microvia technology. In order to accommodate the IC and at the same time minimize the footprint area needed for attachment, substrate/package bond pads should ideally approach the pad size and pitch of the IC. For chip & wire assembly this equates to a pad pitch of 75 to 100 µm (3–4 mils) and lines widths/pitch of 25 to 50 µm (1–2 mils). Figure 15-4(a) shows a fine line MCM-L substrate. Figures 15-4(b) is a populated MCM-L.



(Courtesy Speedy Circuits)

Figure 15-4(a). Unpopulated MCM-L Substrate



(Courtesy Motorola)

Figure 15-4(b). MCM-L—Multichip Module with Laminate Substrate

15.3.1 — The PWB Challenge

With the continued development and ready availability of ICs with increasing performance, functionality and I/O counts, plus marketplace demands for "smaller, better, cheaper" end product, the traditional laminate technology for fabricating PWBs becomes challenged. In order to fully accommodate the newer packaging technologies that included already mainstream BGAs, as well as the emerging CSP and WL-CSPs/flip chips, higher density interconnect substrates (HDIs) are needed.

These HDIs can be characterized by significantly higher wiring density resulting from,

- Targeted lines and spaces and substrate/package bond pads in the range of 25 to 50μm, to accommodate fine pitch I/O die bond pads and minimize "fanout", permitting "near-die-side" wire bonding, and
- Implementation of vias with similar dimensions in via diameter and pitch.

The standard lamination processes lacks the capability to effectively realize these objectives. Even with use of thinner copper foil, while capable of achieving lines down to 75μm it does so at the expense of reduced yields and consequently a higher cost.

The solution however, is once again the application of thin film processes similar to those employed for the manufacture of MCM-D interconnects.

15.3.2 — Build Up Technology [8,9]

The capabilities of the thin film process have already been discussed in Chapter 12. When thin film is applied to manufacture of organic type HDI substrates the process is referred to as Build Up Technology (BUT), or Sequential Build Up Process (SBU). Rapidly becoming mainstream, BUT/SBU addresses Level 1.0 interconnect applications in the manufacture of SCPs, (PBGAs) and MCPs (MCM-Ls) and the Level 2.0 HDI PWB.

15.4 — Vias and HDI

While it is quite obvious that the wiring density of an interconnect is a function of the minimum line widths and spacing achievable the via type, the diameter and the pitch are equally important.

There are three distinct *types* of vias:

- Through-hole
- Blind, and
- Buried.

These are illustrated in Figure 15-5. Figure 15-6 illustrates how the type of via influences the substrate size.

It shows that a six layer board with conventional mechanically drilled through-hole vias only, can be reduced in size (x and y) simply by adding more layers but with added cost. On the other hand, if *blind and buried vias* are used the smaller size can be retained and the number of layers reduced back to the original six layers. Use of mechanically formed blind and buried vias however, requires each inner layer to be laminated separately as opposed to mass lamination. Hence this approach is obviously more costly as well. Conversely, when non-mechanically formed (e.g., photo-patterned) blind and buried vias are used the size remains the same and the number of layers are reduced to five layers and further cost savings.

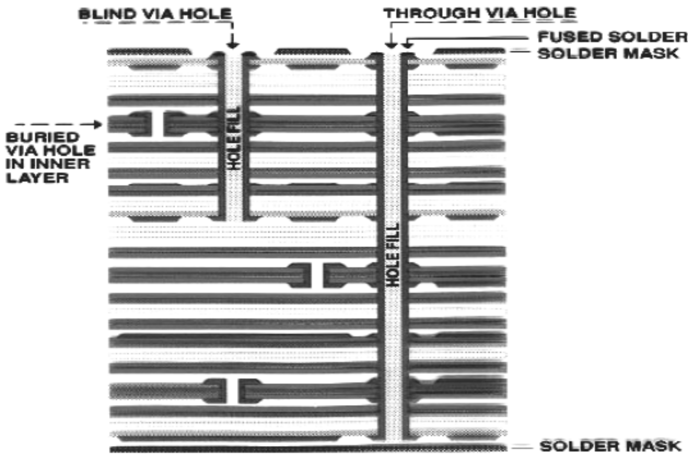


Figure 15-5. Through-Hole, Blind, and Buried Vias

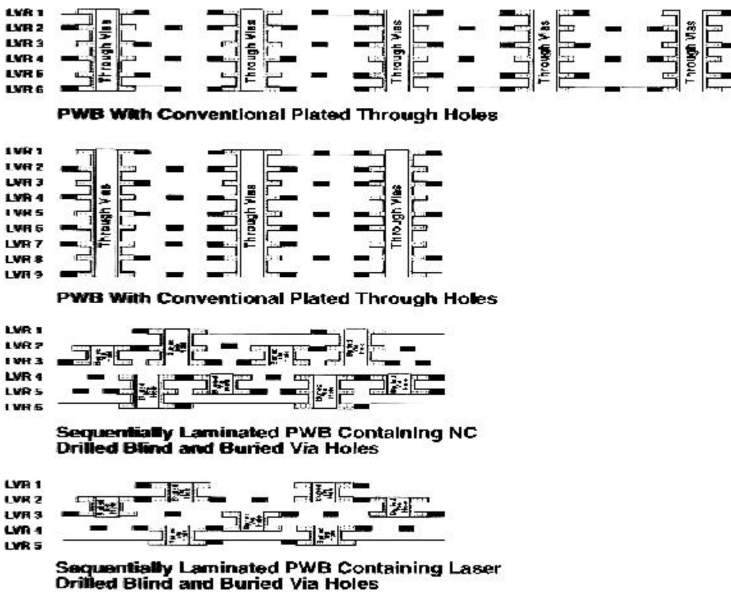


Figure 15-6. Effect of Via Type on Board Size

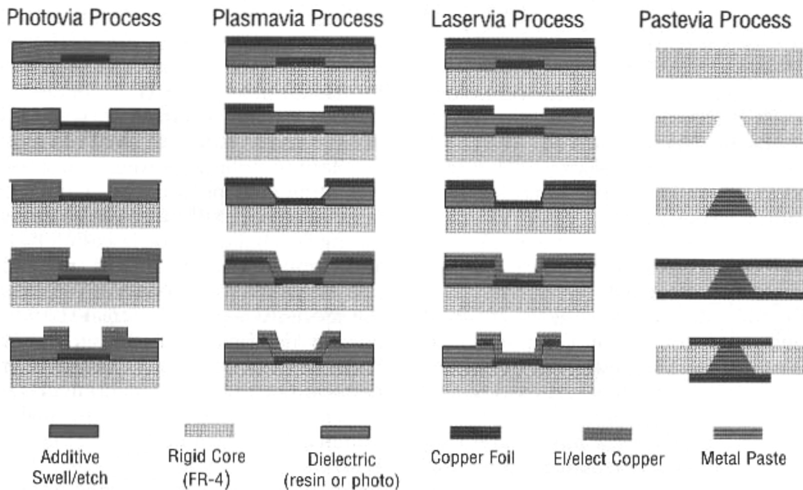
15.4.1 — Microvias

Mechanically drilled vias are limited to diameters down to approximately 150 µm (6 mils), basically becoming too costly below that value due in part to rapid deterioration of the drill bit.

Alternative methods for the generation of vias include:

- Wet or dry (plasma) etching,
- Laser drilling (ablation),
- Photo-imaging, and,
- Conductive ink-formed vias.

These processes are illustrated in Figure 15-7.



(Courtest H.T. Holden, Private Communication)

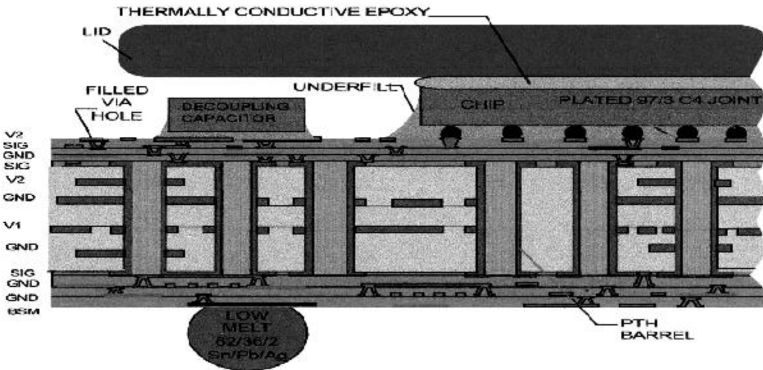
Figure 15-7. Methods of Via Generation

All are readily capable of producing vias that are very much less than 150 μm in diameter down to the desired 25 to 50 μm diameter and pitch range. IPC, the Association Connecting Electronic Industries, has defined any via that is equal or less than 150 μm (6 mils) in diameter as a "microvia".

15.5 — IBM's SLC and HDI PWB Build Up Technology (BUT)

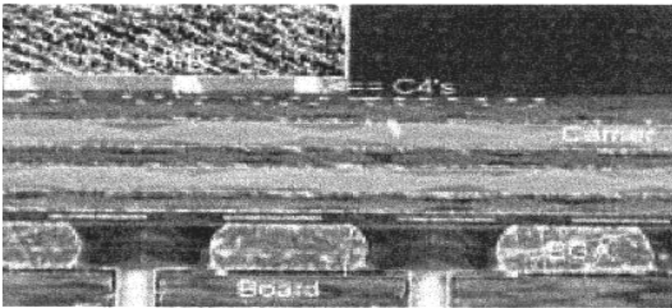
In the early 1990s, with cost as the driver, IBM introduced the Surface Laminar Circuit, SLC technology. Developed in Japan, it addressed high I/O count and C-4 flip chip assembly and replacing IBM's cofired ceramic packaging technology with a lower cost organic package. The SLC structure is shown schematically in Figure 15-8(a). Figure 15-8(b) is a cross-section of an actual SLC BGA. Figure 15-9 shows a single chip PBGA package.

SLC in effect applies thin film type processes, that effectivel provide for fine lines and spaces and microvias, to a core FR-4 board to produce the required wiring density for C-4 flip chips. It is a Build Up Technology process and is clearly an HDI with applicability to SCP and MCP and Level 2.0 applications.



(Courtesy IBM Corp.)

Figure 15-8(a). Schematic IBM's Surface Laminar Circuit-SLC BGA



(Courtesy IBM Corp.)

Figure 15-8(b). Cross-section SLC Flip Chip Package

(Courtesy IBM Corp.)

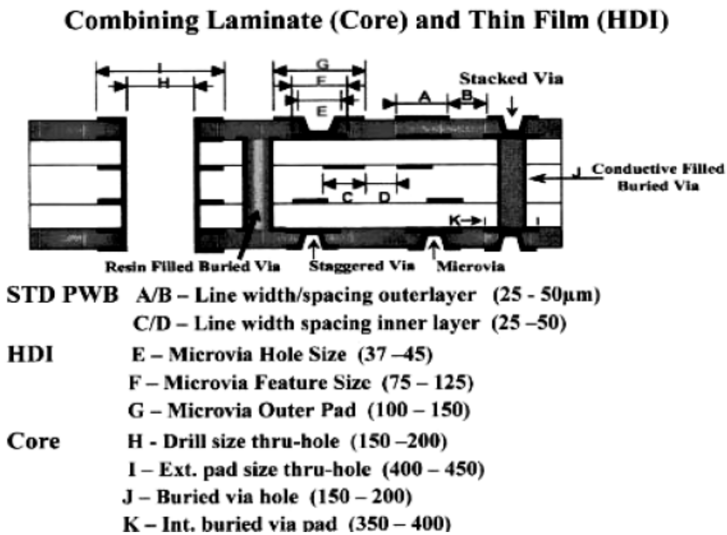
Figure 15-9. Single Chip SLC/BUT PBGA

15.5.1 — The Level 2.0 HDI PWB

While the approach is similar to that used on IBM's cofired packages and interconnects, there are differences in the materials and the processing. In the case of the SLC, the dielectric is a photo imageable epoxy rather than a polyimide or BCB. It is applied using a dry film lamination process. Like polyimide and BCB the vias are defined by photo imaging or by laser ablation. The early SLC vias were 100–125 μm in diameter with 200–300 μm diameter lands.

The metallization process is slightly different as well. There is no sputtering for depositing the metals. An electroless copper plating process deposits copper across the surface of the panel and into the vias, followed by the deposition and patterning of a photoresist layer. The patterned resist then acts as a mask for the selective electrolytic plate-up of the copper conductor. Figure 15-9 shows PBGAs manufactured using the SLC/BUT process.

Figure 15-10 is a schematic showing what one might call the ideal dimensions for an HDI PWB for the current timeframe. The schematic shows two HDI layers per side and a core (FR-4) with two layers also. This type of structure is referred to as 2–2–2 HDI.



(Courtesy Honeywell)

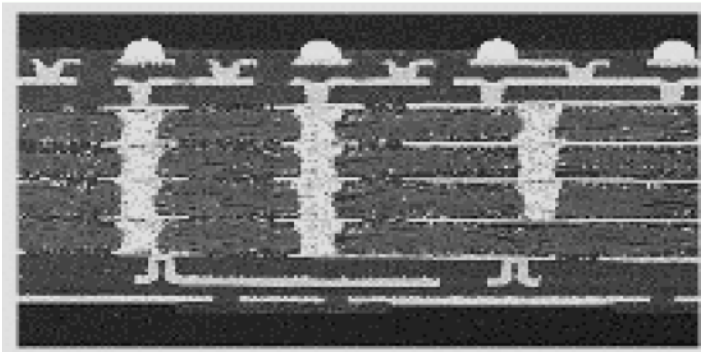
Figure 15-10. Key Feature Dimensions for the HDI PWB

Kyocera is one of several suppliers offering HDI PWBs. Kyocera's technology includes High Density Build Up (HDBU) and Super-High Density Build Up PWBs. The key features for these structures are shown in Figure 15-11. The HDBU uses a core with PTH vias. The Super HDBU uses stacked microvias that allow for a reduction in the number of HDI layers from 4 per side to 2. A cross section of a Super-HDBU PWB showing the stacked vias is shown in Figure 15-12.

		HDBU	Super-HDBU
Typical Structure		4 / 2 / 4 250mm PWR/GND SIGNAL PWR/GND SIGNAL PWR/GND PWB PWR/GND PWR/GND PWR/GND PWR/GND PWR/GND 550mm	2 / 3 / 2 220mm PWR/GND SIGNAL PWR/GND SIGNAL PWR/GND SIGNAL PWR/GND CPCore 220mm Good Z routing capability Build up Layer Reduction
Core	Via Structure	Through Hole	Stacked Via
	Via Pitch	550	220

(Courtesy Kyocera SLC Technologies)

Figure 15-11. The HDBU and Super HDBU



(Courtesy Kyocera SLC Technologies)

Figure 15-12. Cross-section Super-HDBU 2–3–2 PWB

15.6 — Current Status Microvia HDI PWBs [10,11]

In today's market, single and double sided PWBs, supporting through-hole and SMT, are still the main interconnect boards followed by conventional PWB and advanced PWBs. However, the trend in packages is clearly in the direction of area array format (BGAs) with significantly increasing I/O count, and the slow but inevitable emergence of CSP, WLPs and flip chip into mainstream electronics manufacturing. As a consequence HDI PWBs will become the essential Level 2.0 interconnect substrate. Figure 15-13 shows a market forecast for multiplayer board manufacture. It indicates a continuing increase in the manufacture of MLB boards in general, and a rapid rate of increase in MLBs with microvias.

15.7 — Enhancing HDI PWBs—Embedded Passives [12,13]

The PWB provides the interconnects not only between active devices, packaged or unpackaged, but passive components as well. In fact in many cases the number of passives, primarily resistors, and capacitors greatly outnumber the active components. Cell phones in particular use passives in quantities that account for approximately 80% of the total component count. Figure 15-14 provides examples of cell phone features and component count from three different manufacturers.

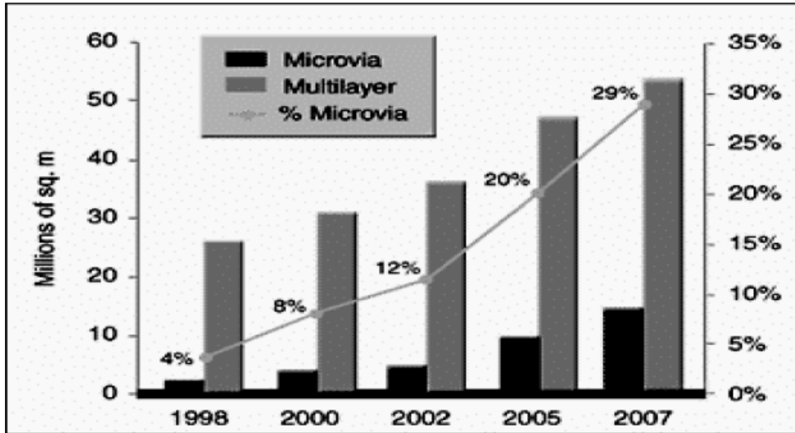


Figure 15-13. Multilayer and Microvia PWB Projections [6]

	Motorola V3688	Sanyo C304SA	Panasonic P208
Standard	GSM	CDMA	PDC
Size	8.3 x 4.3 x 2.6 cm 93 cm³	12.7 x 3.9 x 1.4 cm 89 cm³	12.3 x 3.9 x 1.4 cm 67 cm³
Weight	83 g	80 g	57 g
Components	Unit(%)	Unit(%)	Unit(%)
Large IC	13 (2.0%)	20 (3.0%)	10 (2.3%)
Discretes	69 (10.4%)	51 (7.6%)	26 (6.0%)
Passives	**527 (79.5%)**	**556 (83.1%)**	**342 (78.8%)**
RF Components	7 (1.1%)	12 (1.8%)	7 (1.6%)
Connectors	8 (1.1%)	11 (1.6%)	7 (1.6%)
Others	39 (5.9%)	19 (2.8%)	42 (9.7%)
Total	**663 (100%)**	**669 (100%)**	**434 (100%)**

(Courtesy PrismarkPartners, LLC)

Figure 15-14. Cell Phone Key Features and Component Count

While necessary for electrical reasons, as termination and/or pull-up resistors and decoupling capacitors, discrete passives occupy valuable real estate on the board, require “pick and place” assembly and require two connections per attached component. In a high component count, high volume environment these “negative” aspects of using discrete passives adversely affect the board size, impact cost, and increase reliability concerns.

Use of passives that are embedded within the inner layer interconnect represents a viable solution that essentially eliminate the negatives. Board size can effectively be reduced since real estate required for discrete components is eliminated or space becomes available for additional active components or added wiring. Component assembly and attachment are also eliminated.

15.7.1 — Embedded Passives Technologies

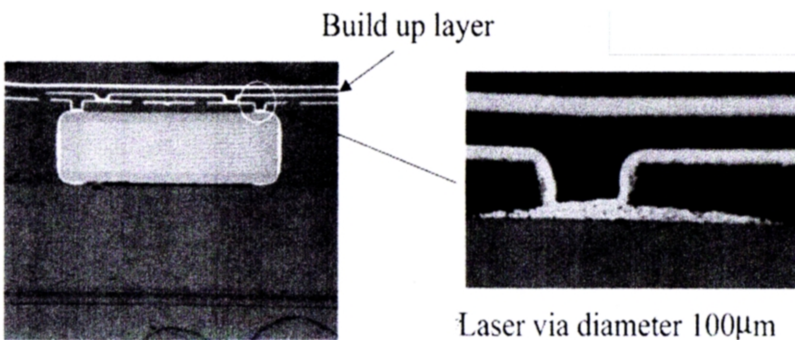
Embedding resistors and capacitors encompasses materials and processes somewhat similar in kind to those already discussed under thick film/cofired ceramic, thin film and laminate technologies.

Embedding technologies applicable to organic laminates include the following:

- Embedded Discrete Chips,
- Filled and Unfilled Laminates,
- Screen Printed Resistor and Capacitors, and
- Etchable Thin Film Resistors Laminates and Plated Resistors on PWB.

15.7.2 — Embedded Discrete Capacitors

Using a “chips first” type process discrete capacitors, as well as active devices, can be readily embedded into laminate type interconnect strutures. An embedded discrete capacitor is illustrated in Figure 15-15.



(Courtesy Fraunhofer IZM)

Figure 15-15. Embedded Discrete Capacitor

15.7.3 — Resistor and Capacitor Embedding by Lamination

Figure 15-16 illustrates typical use of a laminate to produce an embedded planar capacitor compared to a discrete capacitor. In this case the embedded capacitor is introduced basically as another inner layer laminate.

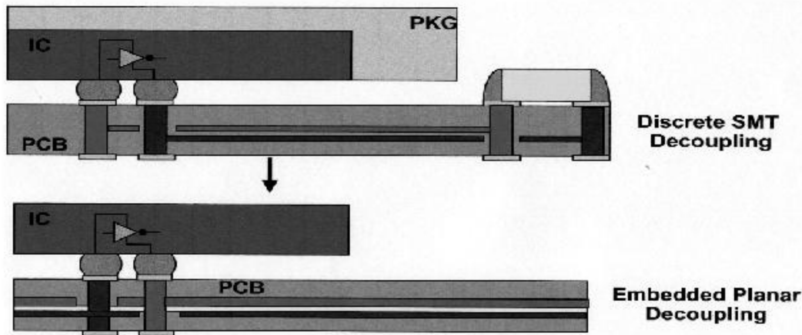


Figure 15-16. Discrete vs. Embedded Planar Decoupling Capacitor [12]

There are several suppliers including DuPont, of resistor and capacitor materials suitable for embedding applications. All paste formulations selectively deposited using the same stencil print process as used in the standard thick film patterning process.

Thin film passives are also available from suppliers that include Ohmega, Gould and Shipley. Resistor and capacitor material can be deposited onto an organic laminate or film using deposition processes such as sputtering and/or plating. The patterning is either by mechanical masking or a photo-defined resist to form the desired geometry.

15.8 — Technology Status

Clearly, embedded passives, either in component format i.e., Integrated Passive Devices (IPD) or embedded into packages or substrate interconnects, are currently moving into mainstream manufacturing particularly in those markets previously noted. There are several obstacles, near term, that impede large scale implementation. These include the need to more fully evaluate the cost advantages to be realized, balancing cost of the materials and processes for embedding, versus cost of the discretes and the assembly. The benefits of embedded passives can however, offset an expected increased cost for the manufacture of HDI PWB.

Additionally, there is a continuing effort in the development and introduction of new materials. The interest is there and the market continues to expand. Clearly, embedded passives is an emerging technology with high potential for becoming mainstream within the next few years. Product demands in the end will drive the technology.

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Acronyms and Definitions

ACA – Anisotropic Conductive Adhesive
ACF – Anisotropic Conductive Film
APWB – Advanced Printed Wiring Board
ASIC – Application Specific Integrated Circuit

BBUL – Bumpless Build Up Layer
BCB – Benzene Cyclobutene (Cyclotene)
BGA – Ball Grid Array
BUT – Build Up Technology

C-4 – Controlled Collapse Chip Connection
C-4NP – C-4 New Process
CAD – Computer Aided Design
C & W – Chip and Wire
CBGA – Ceramic Ball Grid Array
CC – Chip Carrier
CMOS – Complimentary Metal Oxide Semiconductor
CMP – Chemical Mechanical Polishing
COB – Chip On Board
CSP – Chip Scale Package

DCA – Direct Chip Attach
DIP – Dual Inline Package
DRAM – Dynamic Random Access Memory

ECBU – Embedded Chip Build Up
ESD – Electro Static Discharge

FC – Flip Chip
FCA – Flip Chip Assembly
FCM – Few Chip Module
FCOB – Flip Chip On Board
FCIP – Flip Chip In Package
FP – Flat Pack
FQFP – Fine Pitch Quad Flat Pack

GaAs – Gallium Arsenide

HC – Hybrid Circuit
HDI – High Density Interconnect
HDI-PWB – High Density Interconnect Printed Wiring Board

HIC – Hybrid Integrated Circuit
HTCC – High Temperature Cofired Ceramic

I/O – Input/Output
IC – Integrated Circuit
ICA – Isotropic Conductive Adhesive
ILB – Inner Lead Bond
ICF – Isotropic Conductive Film

KGB – Known Good Board
KGD – Known Good Die

LCCC – Leadless Ceramic Chip Carrier
LCD – Liquid Crystal Display
LCP – Liquid Crystal Polymer
LDCC – Leaded Ceramic Chip Carrier
LID – Leadless Inverted Device
LSI – Large Scale Integration
LTCC – Large Scale Integration

Micro BGA (μBGA) – Micro Ball Grid Array
MCM – Multichip Module
MCM-C – Multichip Module-Ceramic (Thick Film or Cofired Ceramic)
MCM-D – Multichip Module-Deposited (Thin Film)
MCM-L – Multichip Module-Laminate (Lamination)
MCP – Multichip Package
MEMS – Micro Electro Mechanical System
MIB – Multilayer Interconnect Board
MIC – Microwave Integrated Circuit
MLB – Multilayer Board
MLC – Multilayer Ceramic
MMIC – Monolithic Microwave Integrated Circuit
MPM – Multi Package Module
MOS – Metal Oxide Semiconductor
MQFP – Metric Quad Flat Pack
MSI – Medium Scale Integration
MTBF – Mean Time Between Failures
MTTF – Mean Time To Failure

NCA – Non-Conductive Adhesive
NCF – Non-Conductive Film

OLB – Outer Lead Bond

PBGA – Plastic Ball Grid Array
PCA – Printed Circuit Assembly
PE – Packaging Efficiency

PGA – Pin Grid Array
PI – Polyimide
PLCC – Plastic Leaded Chip Carrier
PoP – Package on Package
PPM – Parts Per Million
PQFP – Plastic Quad Flat Pack
PTF – Polymer Thick Film
PTH – Plated Through Hole
PCB – Printed Circuit Board
PWA – Printed Wire Assembly
PWB – Printed Wiring Board

QFP – Quad Flat Pack
QFN – Quad Flat Pack No Leads

RAM – Random Access Memory
ROM – Read Only Memory

SAW – Surface Acoustic Wave
SBB – Stud Ball Bump
SCP – Single Chip Packaging
SEM – Scanning Electron Microscope
SEM – Standard Electronic Module
Si – Silicon
SiGe – Silicon Germanium
SIP – Single Inline Package
SiP – System in Package
SLC – Sequential Laminar Circuitry
SoP – System on Package
SMA – Surface Mount Assembly
SMD – Surface Mount Device
SMT – Surface Mount Technology
SOC – System on Chip
SOIC – Small Outline Integrated Circuit
SON – Small Outline No Leads
SOP – Small Outline Package
SOT – Small Outline Transistor
SSI – Small Scale Integration

TAB – Tape Automated Bonding
TBGA – Tape Ball Grid Array
TCE – Temperature Coefficient of Expansion
TC – Thermocompression (bonding)
Tg – Glass Transition Temperature
TS – Thermosonic (bonding)

ULSI – Ultra Large Scale Integration
US – Ultrasonic (bonding)

VLSI – Very Large Scale Integration

WL-CSP – Wafer Level Chip Scale Package
WLP – Wafer Level Packaging

Compiled by W.J. Greig

Microelectronics Glossary

A

ACTIVE CIRCUIT AREA – All areas on the die from outside edge of the bond pads inward.

ACTIVE DEVICE – An electronic device, a bare die or a packaged component a diode, transistor or integrated circuit.

ADHESION – The sticking together of two different materials.

ALLOY – A solution of two or more metals.

ALUMINA – Aluminum oxide (AI_2O_3). Ceramic substrates used in microelectronic applications are made of formulations that are primarily (92%, 96% and 99%+) alumina.

AMBIENT – The temperature and/or pressure and/or humidity of the atmosphere surrounding a device.

ANISOTROPIC – Single directional material property, as opposed to isotropic with material properties the same in all directions. For example, an anisotropic conductive adhesive is conductive in the z-direction only.

ANNEALING – Slow heating and/or cooling of a material to relieve stresses and thereby stabilize the material properties.

ANODIZING – An electro-chemical process for oxidizing metals, most often aluminum.

APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) – A custom designed, not off the shelf, IC intended for a distinct application.

AREA ARRAY – Refers to the configuration of the I/O pads on a device or package. Pads are arranged in an x-y grid format with pins, solder balls or columns for attachment.

ARTWORK – The circuit pattern, typically a drawing at 10X, from which screens or photomasks can be fabricated using photographic reduction.

ASSEMBLY – The attachment of components, – packaged or bare die – active and passives, to a package, substrate or board. Also refers to a substrate or board to which components have been attached.

ASSEMBLY DRAWING – A drawing showing where each component is to be attached onto a substrate or board and the assembly sequence of the parts.

B

BACK END – In semiconductor manufacturing the point at which all wafer processing has been completed and testing, assembly and packaging begins.

BAKE – Subjecting a part, package, board, substrate or an assembly to an elevated temperature. Used primarily to drive off moisture or contaminants, e.g. organics, or assess quality of surface finish, e.g. blisters in plating. Used to react compo-

nents with in a formulation, e.g. photoresist or a polymer to pre-cure or fully cure.

BALL BOND – In chip and wire assembly, a bond formed with a capillary tool where the end of the wire has first been shaped into a ball.

BALL BONDING – A wire bonding technique in which the wire is inserted into a capillary tool and by heating a ball is first formed at the end of a wire. The bond is formed between the ball and a metal pad by heating and application of pressure by the bonding tool (capillary).

BALL GRID ARRAY (BGA) – A packaging technology in which a device's I/O pads are arranged as an array of conducting pads on the base of the package. Small balls of solder are attached to each conducting pad.

BALL BUMPING – The process of forming or placing bumps on packages or bare die, in wafer format or singulated, using a wire ball bonder.

BARE DIE – An unpackaged transistor, diode or integrated circuit.

BISBENZOCYCLOBUTANE (BCB) – High purity polymer resins formulated as high-solids, low viscosity solutions developed for specifically for microelectronic applications including use as an inner layer dielectic in multilevel metallization structures.

BERYLLIA – Beryllium Oxide (BeO). A ceramic used to fabricate substrates having very high thermal conductivity.

BINDERS – Materials, usually organic, added to thick film paste to enhance the flow properties during printing and firing. Binders are also added to ceramics as sintering aids.

BLEED OUT – Die attach adhesives will leak out from under the die before it is cured. This "leakage" is called "bleed". Since wire bonds will not stick in areas where bleed has occurred it is important that bleed not exceed a few mils. Bleeding can be controlled by formulation (filler particle size, resin/hardener selection) and process (cure temperature, out time). In addition material will bleed differently on different surfaces (silver, Nickel, palladium, solder mask, polyimide).

BOARD – Typically refers to a printed wiring board (PWB) or a printed circuit board (PCB).

BOND – A permanent attachment to form an electrical or mechanical interconnection.

BONDABILITY – Those conditions of surface condition, technique and materials that enhance attachment of two materials together.

BOND AREA – The area within which the attachment is to be accomplished. On an active device or package/substrate it is referred to as the bond pad.

BOND DEFORMATION – In wire bonding it is the change in dimensions of the wire at the attachment point produced by the bonding tool and the application of temperature, a mechanical force and/or ultrasonic energy. The deformation is usually measured as a percentage of deformation to original wire diameter in units of wire diameter.

BONDING ENVELOPE/BONDING WINDOW – The range of bonder machine parameters/settings over which acceptable bonds may be obtained.

BOND INTERFACE – In the case of a wire bond it is the wire to the bonding pad surface. In the case of adhesive die attach it is the die to adhesive surface and the adhesive to substrate surface.

BOND LIFT-OFF – The failure mode where a bonded wire separates from the bonding surface.

BONDING SCHEDULE – The various parameter settings on a bonder for wire bonding, for example, the settings for temperature, applied force, bonding time and power.

BOND STRENGTH – In wire bonding, the pull force at failure of a bonded wire when subjected to a destructive wire pull test or bond shear. Several failure modes are possible including bond lifts and wire breaks. The bond strength is measured in grams of force.

BONDING WIRE – Fine gold, aluminum or copper wire used to make electrical connection between the active device bond pads and the package or substrate pads.

BOW – The deviation from flatness of a package/substrate or board. Same as warpage and camber.

BUMPING PROCESS – The deposition of bumps, typically solder or other conducting material onto device bond pads to be used for the attachment medium to a package or substrate. Most commonly performed while devices are in wafer format. Typically involves deposition and patterning of an under bump metallization followed by the bump deposition by electroplating or stencil printing of solder paste. See Wafer Bumping. For CSP and BGA, balls are mechanically placed using specially designed placement equipment. Bumping is also accomplished using wire bonding. See Stud Bumping.

BURN-IN – The process of electrically stressing a device at an elevated temperature for an adequate period of time intended to cause rapid failure of marginal devices.

C

CAMBER – The amount of bow or warpage in a board or substrate. See BOW.

CAPILLARY – In wire bonding a tool used to guide wire and to apply pressure to form a bond between the wire and a metallized pad on a device, package or substrate.

CAPILLARY ACTION – The action by which the surface of a liquid in contact with walls of a capillary tube or between two closely spaced plates is drawn into the tube or between the plates by a wicking action. An example of capillary action is in the flip chip assembly, the underfill is dispensed next to the die and the material is pulled into the gap by the force of capillary action.

CENTRIFUGE – A method of testing circuits and packages by spinning at high speed. Places high “G” loads (a centrifugal force) on IC’s and bonds to evaluate mechanical robustness).

CERAMIC – An inorganic material that is a non-conductor of electricity. Examples are alumina (Al_2O_3), beryllia (BeO), aluminum nitride (AlN) steatite, or forsterite. All have high temperature melting points. Ceramics are used extensively in microelectronics manufacturing as packages or substrates.

CERDIP – A ceramic dual in-line package.

CERMET – A mixture of glass and/or ceramic, it has come to mean the general class of high resistivity thick film resistors and dielectrics paste materials that are fired at temperatures above 500°C.

CHAMFER – A corner or edge of a substrate or board that is broken or shaped to eliminate a sharp edge or to identify a desired part's orientation.

CHEMICAL VAPOR DEPOSITION (CVD) – Deposition by reduction or decomposition of a material to vapor onto a substrate. Generally accomplished in a plasma system.

CHIP – (1) Active – Unpackaged bare die, e.g. a diode, transistor, or IC. (2) Passive – A discrete capacitor, resistor, inductor.

CHIP CARRIER – A type of package or substrate, used to enable electrical testing and provide mechanical and environmental protection to active devices. See also PACKAGE.

CHIP AND WIRE ASSEMBLY (C&W) – Wire bonding bare die to a package, substrate or board using Au, Al or Cu wire for electrical interconnection.

CHIP ON BOARD (COB) – Assembly of bare die wire bonded to an organic substrate or printed wiring board. As a packaging option COB is classified as a "packageless packaging" approach that enhances reliability with the elimination of the package. The bare die may be glob topped with an organic coating to protect the wire bonds and die.

CHIP SCALE PACKAGING (CSP) – A package format where the package area is no more than 1.2 times the area of the die.

"CHIPS FIRST" PACKAGING – A packaging technology where all die are first attached to a substrate or organic film and interconnect circuitry to individual die and between die is subsequently fabricated into a finished single or multichip package. There is no wire bonding, flip chip or TAB assembly required.

"CHIPS SECOND" PACKAGING – A packaging technology in which all die are assembled using chip & wire, flip chip or TAB, to a pre-fabricate package or substrate containing the necessary interconnect circuitry.

CHLORINATED SOLVENTS – Hydrocarbon liquids containing chlorine. Most commonly used in cleaning processes.

CIRCUIT – A conductor interconnect for a number of elements and/or devices designed to perform a desired electrical function.

CLAMPING FORCE – In wire bonding, the force applied to the wire by the bonding tool to affect a bond.

CLADDING – A method of applying a metal foil to a substrate. See COPPER CLADDING.

CLEAN ROOM – An area in which a high degree of cleanliness is realized and maintained by controlling the generation and distribution of particulate matter inside the room. Cleanliness is achieved by air filtering systems in a controlled environment, i.e., temperature and humidity. Clean rooms are classified based on the allowable number and size of particles of per cubic feet. For example, a Class 100 clean room refers to a room in which no more than 100 particles greater than 0.5 micrometers in diameter are present.

COEFFICIENT OF THERMAL EXPANSION (CTE) – How much a material grows when heated and shrinks when cooled. The unit of measure is parts per million

(ppm) per degree centigrade. The CTE differences (CTE mismatch) among the materials in a semiconductor package will cause stress as the part is exposed to temperature changes in its working life. In most cases, it is important for an epoxy connecting two materials to have a CTE that falls between the CTE's of the materials being joined.

COFIRING – Firing of two or more materials at the same time.

COLD SOLDER JOINT – A solder connection that was made at too low a temperature. The joint usually appears rough and dull and is generally unreliable.

COMPATIBLE – Refers to materials that can be used together with minimum adverse reaction, e.g. the bonding wire and the die or package metal bond pad.

COMPONENT – A packaged active or discrete passive device.

CONDUCTIVE ADHESIVE: An adhesive material (usually epoxy) that has metal powder (usually silver or gold) added to increase electrical conductivity. Same as conductive epoxy.

CONDUCTIVE EPOXY – A polymer resin that has been made conductive by the addition of a metal powder, usually silver or gold.

CONDUCTIVITY – The ability of a material to conduct electricity.

CONDUCTOR – A class of materials that conduct electricity.

CONDUCTOR FILM – a metal trace deposited by thick or thin process and patterned on a substrate.

CONDUCTOR SPACING – The distance between adjacent conductor traces. Measured from the outside edge one trace to the inside edge of another.

CONDUCTOR WIDTH – A measurement of a conductor trace from edge to edge.

CONDUCTOR THICKNESS – The height of a conductor trace, measured from the substrate to the top surface of the conductor.

CONFORMAL COATING – A thin nonconductive coating that may be organic (polyimide, for example) or inorganic (glass) whose purpose is to protect circuitry and circuit elements. Conformal coatings are typically non-planarizing.

CONTACT PRINTING – (1) A method of screen printing whereby the screen is in contact with the substrate to be printed and there is zero snap-off. (2) In the photolithography image transfer process where the photomask and resist coated substrate are in intimate contact.

CONTACT RESISTANCE – A measure of the quality of an electrical connection between two contact pads, e.g., a wire bond. Contact resistance is measured in milli-ohms.

CONTINUOUS BELT FURNACE – A furnace that uses a moving belt to transport parts through the furnace.

CONTROLLED COLLAPSE – Minimization of the amount of decrease in bump size, e.g. solder ball diameter, following reflow attachment.

COPPER CLADDING – A sheet of Cu foil bonded to an organic core to form the base material for a printed wiring board.

CRAZING – Fine cracks found in brittle materials.

CRITICAL DIMENSION – In microelectronics packaging, the smallest feature size to be defined in patterned circuitry.

CROSSOVER – Transverse crossing of a metal by another metal without electrical contact and achieved by the deposition of an insulating layer between the conductors at the area of crossing.

CROSSTALK – Signals from one conductor trace leaking into another nearby conductor because of capacitive or inductive coupling or both.

CURE – A non-specific term that is widely used to mean the solidification of a polymer. Curing can be accomplished by applying heat or UV light.

CURE TIME – The time required to fully harden an organic material, e.g., an epoxy, under a defined set of conditions.

CUSTOM CIRCUITS – A circuit designed for a single specific application. See Application Specific Integrated Circuit.

CYCLIC STRESS – A method of testing circuits by subjecting them to various cycles of temperature, or power, humidity or voltage. A method of doing accelerated testing.

CYCLOTENE®™ – The commercially available version of BCB, the insulating polymer derived from bisbenzocyclobutane.

D

DEFECT – An anomaly that is in non-conformance with normally accepted characteristics.

DEFINITION – The sharpness of a deposited pattern, or the exactness with which a feature is patterned with respect to the intended design.

DEGRADATION – A debilitating change in a material characteristic or a device performance.

DENSITY – In packaging: Refers to the number of components on a circuit or board or the amount of conductor circuitry on a device package, a substrate or board.

DEVICE – A bare die (an element) or a packaged component.

DEWETTING – A condition that results when molten solder has coated a surface and upon cooling recedes leaving areas of uncovered base material.

DICE – Plural of die.

DIE – An unpackaged semiconductor, e.g. a diode, transistor or an integrated circuit, separated from a wafer. Also referred to as a bare die or a chip.

DIE ATTACH – Bonding of semiconductor die to a package/substrate. Same as die bonding.

DIE ATTACH – Adhesive attachment of a semiconductor die to a package/substrate. Can be thermally conductive or non-thermally conductive.

DIE BONDING – The process of attaching a semiconductor die to a package, substrate or board with a eutectic or solder alloy.

DIE BONDER – The machine used for die bonding.

DIELECTRIC – Any material that does not conduct electricity, an insulator, such as glass, ceramic or epoxy. Sometimes used to refer to a nonconducting ink or paste.

DIELECTRIC BREAKDOWN VOLTAGE – The threshold voltage that causes a dielectric layer to conduct electricity.

DIELECTRIC CONSTANT – A property of a dielectric material that is a measure of the ability of a material to store an electric charge.

DIELECTRIC LAYER– A film of insulating material separating two conductor films or as an insulating layer on a metal surface to allow deposition of a layer

of conductive circuitry. Also refers to application of an insulator to function as a passivation layer.

DIELECTRIC LOSS – The power lost in a dielectric layer when placed in an A/C field.

DIELECTRIC STRENGTH – The maximum electric gradient a dielectric layer can withstand without breaking down. Expressed in units of volts/mil.

DIE-SHEAR TEST – A test to determine the shear strength of the bond between a die and the base it is bonded to.

DIFFUSION – The movement of atoms from regions of high concentration to low concentration. Diffusion depends on temperature, concentration and the mobility of the specific material.

DIRECT BOND COPPER (DBC) – The high temperature direct bonding of copper foil to a ceramic by means of the copper-oxygen eutectic.

DIRECT CHIP ATTACH (DCA) – Refers to the assembly of bare die to a package, substrate or board.

DISCRETE COMPONENT – Packaged active or passive devices as opposed to bare die.

DISSIPATION FACTOR – Tangent of the dielectric loss angle. The ratio of the resistive component of a capacitor to the reactance.

DOUBLE SIDED BOARD – A printed wiring board with conductive circuitry on both sides of the board.

DRY AIR – Air that has had moisture removed. Dryness is specified by the dew point, e.g. –40°C.

DRY FILM RESIST – A relatively thick (.12.5 mils) photosensitive film applied by lamination.

DRY PRESSING – A method of making ceramic parts whereby ceramic powder is compacted in a mold and fired in a furnace to sinter the powder.

DRY PRINT – A thick film print that has gone through the drying stage.

DUAL IN LINE PACKAGE (DIP) – A package having two rows of leads, with equal spacing on two opposing sides and designed for through-hole attachment onto a printed wiring board.

DUCTILITY – The ability of a material to be deformed without fracture.

E

EDGE DEFINITION/EDGE ACUITY – The sharpness of a pattern deposited by a thick film or thin film process. See Definition.

ELECTRICAL ISOLATION – Separating two or more conductors from each other by means of a dielectric.

ELECTROLESS DEPOSITION – The deposition of an electrically conductive film from an autocatalytic plating solution without the use of electric current.

ELECTROPLATING – The deposition of an electrically conductive film from a solution (plating bath) of the ions of that metal, by means of an electric current.

ELECTRONIC PACKAGING – A process involving the interconnection of semiconductor devices into packages (single or multichip), substrates or boards to complete the manufacture of a fully functional electronic system or subsystem.

ELEMENT – A bare unpacked die typically referring to an Integrated Circuit.

ELEMENT EVALUATION – Assembly and electrical testing of a sample of bare die taken from a manufacturing lot to assess the electrical integrity (number of parts electrically good following assembly and burn-in) of the particular die lot. Also called a Lot Acceptance Test (LAT).

ELONGATION – The ratio of wire length at rupture to original length. A measure of ductility. Measured in percent.

EMBEDDED LAYER – A conductive or passive layer deposited between two dielectric layers.

EMULSION – In screen printing, the light sensitive material used to pattern coat a mesh screen. When exposed and patterned it is used for depositing distinct patterns of thick film paste that are subsequently dried and fired.

ENCAPSULANT – A material that seals or covers a semiconductor to provide mechanical and environmental protection. Typical materials are: molding compound, glob top, dam & fill and potting compound.

ENCAPSULATE – To coat or cover with an organic material (epoxy or silicone) an assembled device to provide mechanical and environmental protection.

ENVIRONMENTAL TEST – A test to determine the integrity of an electronic assembly under various external conditions.

EPOXY – A family of thermoset or thermoplastic polymers used in microelectronic packaging for bonding, encapsulation, and underfilling.

EPOXY – Family of thermosetting resins that are used as the media for bonding and/or protecting semiconductor devices. The main advantages of epoxy are the ability to form strong bonds to many surfaces, low processing temperature and low cost. Epoxies come in many variations with different properties.

ETCHED METAL MASK – A metal foil where the pattern is made by a wet or dry etches process.

ETCHING – The process of removing unwanted material by wet (chemical) or dry (plasma) processes using appropriate masking (a resist or another metal).

EUTECTIC – The metallurgical composition two or more metals (alloy) that has a melting point significantly lower than that of the higher melting metal.

EUTECTIC TEMPERATURE – The melting temperature of a specific eutectic alloy composition.

EXPOSURE – The process of transferring a pattern from a photomask to a photosensitive film coated wafer or substrate by using an appropriate energy source, such as ultraviolet light, laser, e-beam or x-ray.

F

FAILURE ANALYSIS – A process to determine reasons why a device, circuit or assembly does not meet performance specifications.

FAILURE MECHANISM – A process intended to determine cause for the failure of a device, circuit or assembly fails to meet its intended performance specifications, e.g., and open or shorted conductor trace.

FAILURE RATE – The ratio of the number of failures to the total number tested. Usually specified as %/1000 hours of operation.

FATIGUE – With solder bonds, a failure mechanism caused by exposure to repetitive levels of mechanical stress over time resulting from mismatch in thermal coefficient of expansion, e.g. a bare die and an organic substrate or board.

FEEDTHROUGH – A method of making electrical connection between both faces of a circuit board, substrate or package, e.g., a plated through-hole or through a package wall.

FILLED POLYMER – The addition of a powder (ceramic or metal) to change the thermal and/or electrical properties of the polymer e.g. silver particles to an epoxy to increase electrical conductivity or born nitride to an epoxy to improve thermal conductivity.

FILLER – The general term for any addition agent into a material to change its properties, i.e., electrical and/or thermal conductivity.

FILLET – Refers to the extension around the edge of a die from the adhesive or alloy used in bonding a die to a package, substrate or board.

FILM – Any thin layer on the surface of a substrate such as a thick or thin film conductor or dielectric, or a layer of moisture, or contaminant.

FINAL SEAL – The manufacturing operation wherein a lid is attached – soldering, welding or with an epoxy – that completes the enclosure of a microcircuit into a package with a controlled ambient.

FIRING – The process of heating screen printed thick film materials to an elevated temperature in a furnace, to transform the paste into its final functional form.

FIRST BOND – In chip and wire assembly, the first bond in a sequence of two or more bonds made to a wire.

FLAT PACK – A package for microcircuits having the leads extending from 2 opposing sides and designed specifically for surface mounting onto a printed wiring board.

FLEX CIRCUIT – Interconnect circuitry supported on a thin flexible organic film (Kapton®/polyimide), typically 25 micrometers thick. Circuitry can be single sided, double sided or multilayer.

FLEXIBLE COATING – A polymer film that remains non-rigid after curing.

FLIP CHIP (FC) – A leadless device typically an integrated circuit that is designed to be attached, face down to a package, substrate or board by means of bumps on deposited each bond pad. No wire bonding is used. The flip chip is bumped typically while in wafer format.

FLIP CHIP ATTACHMENT – The process that completes the electrical connection of an active device by facedown bonding to a package/substrate.

FLUX – In soldering, a resinous material the dissolves oxides and improves wetting of a solder to a metal surface.

FLUX RESIDUE – Soldering flux remaining after soldering and cleaning.

FOIL – A thin continuous sheet of metal, usually copper, applied to an organic board by cladding and subsequently patterned as conductor traces.

FOLDED FLEX PACKAGING – Stacked packages interconnected using flex circuitry.

FORMING GAS – A mixture of H_2 and N_2, typically less than 5% H_2. Used wherever a reducing non-oxidizing atmosphere is needed, e.g., eutectic die bonding or fluxless soldering.

FRONT END – In semiconductor manufacturing: refers to those manufacturing processes in which multiple integrated circuits are formed in and on a semiconductor wafer. Front end processes end with wafer electrical testing.

FUNCTIONAL CIRCUIT ELEMENTS – Refers to bare die, i.e., diodes, transistors and integrated circuits.

G

GALLIUM ARSENIDE (GaAs) – A semiconductor typically used for high-speed, high frequency circuit applications.

GLASS BINDER – The glass powder added to a thick film ink to hold the functional particles together and to promote adhesion to the surface of the ceramic.

GLASSIVATION – A method of passivating a semiconductor die by coating with a glass layer leaving only the bond pads exposed.

GLAZE – General term for a glass coating.

GLAZED SUBSTRATE – A ceramic substrate that has been coated with a glass layer for smoothness.

GLOB TOP – An epoxy encapsulant. Typically used for Chip on Board.

GRAM-FORCE – In wire bonding or flip chip attachment the amount of physical force required to create an open bond.

GREEN – A term used to identify an unfired ceramic sheet or tape. For example, a "green" substrate is one that has been formed, but has not been fired.

GROUND PLANE – A conductive layer used as a common reference point for one or more electrical connections.

H

HALOGENS – The elements Chlorine, Fluorine, Bromine and Iodine.

HALOGENATED SOLVENTS – Organic liquids containing one or more of the halogens. Generally used as cleaning solvents. For example, trichloroethane.

HARD SOLDER – Solders containing Au, e.g., 80%Au/20%Sn, melting point 280ºC.

HARDNESS – A material property. The ability of a material to resist penetration.

HARDNESS – Property of a material to resist indentation or scratching.

HEAT SINK – A piece of high thermal conductivity material slightly larger than the component (bare die or packaged) used to conduct heat away from the heat-sensitive device. Examples are most metals and diamond.

HEEL OF THE BOND – In wire bonding, that part of the wire where deformation begins. It is noted on the first and second bond in wedge bonding and the second bond in ball bonding.

HEEL BREAK – A break in a bonded wire at the heal of the bond.

HERMETIC SEAL – Capping of a package containing an active device to provide an enclosure that maintains a controlled ambient.

HIGH TEMPERATURE CO-FIRED CERAMIC (HTCC) – A monolithic multilayer ceramic package or substrate containing an embedded conductor interconnect circuit. Individual layers of ceramic with patterned conductor traces (typically

tungsten or molybdenum) are processed separately, inspected, collated, stacked and co-fired at temperatures in the range of 1400 to 1600°C.

HI-K CERAMIC – A ceramic material with high dielectric constant.

HIGH PURITY ALUMINA – Alumina with over 99.9% Al_2O_3 content.

HOSTILE ENVIRONMENT – An environment that has a degrading effect on an electronic device or assembly e.g. automotive or space environments.

HYBRID CIRCUIT (HC) – A multi-component assembly containing active devices (bare or packaged) and passives (deposited or discrete) interconnected on a rigid insulating substrate (ceramic or organic) by a deposited (thick or thin film) conductor network that can be single or multilayered. Also referred to as Hybrid Integrated Circuit (HIC) or Hybrid Microcircuit.

I

INERT ATMOSPHERE – A gas atmosphere composed on one of the inert gases, i.e., non-oxidizing, non-reducing. Ar or N_2 are most commonly used.

INFANT MORTALITY – Early device electrical failures occurring when subjected to stress conditions, e.g., burn-in testing. Electronic components are generally characterized by an initially high failure rate that decreases with increasing time. (Bathtub curve).

INJECTION MOLDING – Molding of electronic packages by forcing a heated liquid epoxy into a steel mold containing the parts to be encapsulated.

INK or PASTE – A general term for screenable thick film compositions.

INSERTION LOSS – The difference between power received at the load before and after the insertion of a device in the line.

INSPECTION LOT – A sample quantity of devices, representing a production lot, submitted at one time, to determine compliance with acceptance requirements as specified on the procurement documents.

INSULATORS – A class of materials with high insulation resistance. Also refers to thermal or electrical insulators.

INTEGRATED CIRCUIT (IC) – A microcircuit or microchip. A single semiconductor die (Si, GaAs, SiGe) containing multiple transistors interconnected by a single or multiple layers of patterned conductors, each separated by a layer of dielectric. This monolithic structure may also contain passive elements as well. An IC is also referred to as microcircuit or microchip.

INTERCONNECTION – Use of conductive metal, e.g. wires, bumps and packages or substrates with embedded conductor circuitry, to electrically link a single device or multiple devices with each other.

INTERFACE – The boundary between two materials, e.g. in wire bonding the area of contact between the wire and the metal bond pad or between a deposited metal and an electro or electroless plated metal.

INTERMETALLIC COMPOUND (IMC) – A compound of two or more metals that have a characteristic crystal structure and defined composition. Referred to simply as Intermetallic, an IMC is characteristically brittle and high resistivity.

ISOTROPIC – As related to etching of films, etch rate the same in all directions x, y and z. Also relates to conductive adhesives, electrically conductive in all directions x, y and z.

J

JUNCTION TEMPERATURE – The temperature in the region of transition between p- and n- type semiconductor in a transistor structure. Excessively high junction temperature can degrade device reliability and lead to complete failure.

K

KIRKENDALL EFFECT – The occurrence of void formation in a material caused by diffusion of atoms across an interface the result of exposure to elevated temperature. Excessive voiding can result in an electrical open.

KNOWN GOOD CIRCUIT (KGC) – A circuit that has been tested to preclude presence of destructive defects that after assembly of all elements and components would not be electrically functional.

KNOWN GOOD DIE (KGD) – A qualification or process that verifies an unpackaged semiconductor die has been electrically tested to a specific level of quality and/or integrity relative to the packaged device's electrical specifications.

L

LAMINAR FLOW – A constant directional flow of highly filtered air across a work surface or area. The flow can be parallel or perpendicular to the work surface.

LAMINATE – A layered structure of sheets bonded together under heat pressure.

LAMINATE THICKNESS – In a printed circuit board, the thickness of the core and metal cladding prior to further processing.

LASER TRIM – The upward adjustment of a film resistor by cutting and physically removing material by means of a laser.

LAYOUT – A dimensioned drawing of a patterned circuit containing conductor traces and deposited passives. Used in the fabrication of thick film screens or photomasks. The layout is typically at some magnification, e.g. 10X, and is subsequently photographically reduced to 1X on a master plate or film that is used to produce a screen or mask.

LEACH – In soldering: the dissolution of a metal into molten solder. Leaching can ensure proper bonding to the metal is achieved. Excessive leaching can result in a poor solder bond.

LEAD – Part of a package. Rigid or semi-rigid the leads are the external I/Os of the device and allow electrical and mechanical access and subsequent attachment of the package to the next assembly level.

LEAD FRAME – A metal frame that has been patterned by etching or stamping with defined leads and a base tab, to which a bare die is attached and wire bonded. The assembly is transfer molded except for the leads. All plastic packages DIPs, FPs, QFPs, are lead frame based.

LEADLESS DEVICE – A semiconductor carrier or package having no input/output external leads extending out from the package body.

LEADLESS INVERTED DEVICE (LID) – A ceramic package designed specifically for transistors (late 1950s) for use on hybrid circuits. It had no leads but rather

metallized pads for solder attachment directly onto a ceramic substrate. It was the first semiconductor package that to be surface mounted.

Level 1.0 INTERCONNECTIONS – Refers to the assembly of bare die to a package, substrate or board.

Level 1.5 INTERCONNECTIONS – Refers to the assembly of multiple bare die to a package or substrate (Multichip Packaging).

LEVEL 2.0 INTERCONNECTIONS – Refers to the assembly of bare die, packaged components and discretes to a printed wiring board or ceramic board a Printed Wiring Board Assembly, a PWBA, or a Printed Circuit Board a PCB.

Level 3.0 INTERCONNECTIONS – Refers to assembly of printed circuit boards to another printed wiring board called a "mother board".

LEVELING – In thick film screen printing: The settling of thick film paste after printing. Leveling can minimize screen mesh marks in the printed paste.

LIFE TEST – The test of a component or assembly typically under actual use conditions or accelerated temperature for an extended period of time.

LINE CERTIFICATION – Verification that a production process meets applicable process procedures, specifications and control standards.

LINE DEFINITION – A measure of the dimensional exactness and quality of a patterned feature, e.g. a conductor trace, as replicated from an image on a screen or photomask.

LINES – Another term for a patterned conductor trace.

LIQUIDUS – The temperature above which an alloy is completely molten. The temperature where melting is completed for a non-eutectic alloy.

LIQUID RESIST – A photosensitive liquid generally applied to a substrate by spinning. Other techniques include spraying, dipping, curtain coating meniscus coating and electrodeposition.

LITHOGRAPHY – The transfer of a pattern or image from one medium to another, e.g. from a photmask to a photosensitive film (resist) deposited onto a wafer or substrate. Resist requires exposure to an appropriate energy source ultraviolet light, electron beam, laser or x-rays. If light is used to affect the transfer, the term "photolithography" applies.

LOOP – The wire profile formed by a bonding wire between the first and second bonds.

LOOP HEIGHT – The maximum distance of the wire loop from the surface of the first bond.

LOSS TANGENT – The ratio of irrecoverable to recoverable part of electrical energy introduced into an insulating material by the establishment of an electric field within the material.

LOW LOSS SUBSTRATE – A substrate that absorbs little energy when subject to high frequencies and is therefore suitable for microwave applications.

LOW TEMPERATURE COFIRED CERAMIC (LTCC) – Multilayer ceramic circuit package similar to HTCC but fired at temperatures 850–1000°C usually with thick film gold paste instead of refractory metals such as tungsten or molybdenum.

M

MASK – A metal foil, a polyester film or a glass plate that contains well defined features or images used for the patterning of deposited films or for the manufacture of screens for screen printing of thick film pastes.

MESH SIZE – The number of openings in a screen. A 350 mesh screen has 350 openings per linear inch or 105,625 openings per square inch.

MEAN TIME BETWEEN FAILURES (MTBF) – Used to express failure rate.

METAL MASK – A foil or thin sheet of metal, a stencil into which appropriate features have been generated by selective chemical etching.

METALIZATION – The metal film on a semiconductor die used to connect electrically different areas on the die. A film pattern (single or multilayer) of conductive material deposited on a substrate to interconnect electronic components, or the metal film on the bonding area of a substrate which becomes a part of the bond and performs both an electrical and a mechanical function.

MICROCHIP/MICROCIRCUIT – An integrated circuit.

MICROELECTRONICS – The area of electronic manufacturing specifically associated with *assembly and packaging of semiconductor die*, i.e., diodes, transistors and integrated circuits, covering single chip packaging, multichip packaging and chip on board applications.

MICROCRACK – A small crack, usually not visible to the naked eye.

MICROSTRIP – A microwave transmission component.

MIGRATION – An undesirable phenomenon whereby metal ions, e.g., silver, are transmitted across an insulated surface, in the presence of adsorbed moisture and an electrical potential.

MIL SPEC – A Military Specification.

MODULUS OF ELASTICITY – Modulus is the amount of force per cross-sectional area of a material (stress) required to change the shape of the material divided by the amount of change in shape (strain). For example, it is the force applied to a steel rod that is required to cause the rod to stretch or get longer divided by the amount the rod stretches. Modulus is a measure of the flexibility or elasticity of a material. The lower the number the more elastic the material. A rubber band has a very low modulus because it stretches very easily. An aluminum bar has a higher modulus because it takes more force to stretch it. Glass has a very high modulus; it will usually break before it stretches.

MOISTURE STABILITY – The stability of a component or material under the conditions of high humidity.

MONOLITHIC INTEGRATED CIRCUIT – An integrated circuit.

MOS DEVICE – Abbreviation for Metal Oxide Semiconductor device.

MOTHER BOARD – A circuit board used to interconnect smaller circuit board assemblies.

MULTICHIP MODULE (MCM) – A multichip assembly similar to a hybrid circuit, but of a higher level of complexity comprised of at least two Very Large Scale Integration ICs. The MCM is designed and structured to be supportive of the electrical, mechanical and thermal needs of the ICs.

MULTICHIP PACKAGING (MCP) – A packaging option in which multiple chips are assembled into a package. MCP generically covers Hybrid Circuits, Multichip Modules, and System in Package, System on Package and Stacked Die.

METALLIZATION – Refers to metal interconnections on a wafer, package, substrate or board.

MULTILEVEL METALLIZATION – Two or more levels of metal (circuitry) forming electrical interconnections for active and passive components, discrete or deposited, to create a functioning electronic circuit. Individual metal layers are isolated from each other by a dielectric. Vias in the dielectric allow for interconnection between the metal layers.

N

NECK BREAK – In ball bonding, a wire breaks directly above the ball bonds.

NEGATIVE IMAGE – The reverse image of the to-be-patterned feature.

NONCONDUCTIVE EPOXY – An epoxy material (a polymer resin) of very high electrical resistivity.

O

OFF CONTACT – (1) In screen printing, the normal printing set up whereby the screen is not in contact with the substrate prior to the printing stroke. (2) In Thin Film Photolithography, a printing mode where mask is not in direct contact with photosensitive resist on the wafer, substrate or board. Also called Proximity Printing.

OHMIC CONTACT – An electric contact that has a linear voltage vs. current relationship. It is a measure of the electrical conductivity of a bond and is expressed in terms of milliohms.

OHMS PER SQUARE – A measure of the electrical resistivity or sheet resistance of a conductor film.

ORGANIC FLUX – A solder flux composed of rosins and organic solvents.

OUTGAS – Relates to the amount of weight loss of an adhesive during curing or at elevated temperatures due to solvent evaporation. Any solvent or low boiling temperature components of a polymer formulation can evaporate. The temperature and conditions entirely depend on the materials of the formulation. Bubbles, formed as the outgas materials tries to escape, can form voids in the die attach, underfill or encapsulant. These vapors can also condense on nearby die bond pads and package pads and interfere with wire bonding.

OVERCOAT – A thin coating of insulating material applied to a component or assembly for the purpose of providing additional mechanical and environmental protection (may be organic or inorganic).

OVERGLAZE – An inorganic coating of a fired thick film paste composed of glass frit.

OXIDIZING ATMOSPHERE – Gaseous ambient containing oxygen.

P

PACKAGE – An enclosure or carrier, metal or plastic, for a semiconductor die or substrate assembly, with I/O terminals to provide electrical access and attachment to the next assembly level. Both metal and plastic packages provide for mechanical protection from damage. The metal package however affords the highest level of environmental protection by providing a hermetic enclosure, i.e. a controlled and constant ambient, for the device(s).

PACKAGE LID – A flat metal plate used to completely seal a package cavity to provide a hermetic enclosure.

PACKAGE on PACKAGE (PoP) – Stacked packages.

PAD – That portion of a conductive pattern designed for device attachment. e.g., die bonding, wire bonding.

PANEL – A large substrate. Typically refers to the organic substrate used in printed wiring board manufacturing.

PASSIVATION – An insulating layer (organic or inorganic) deposited directly over a circuit element to protect the surface primarily from ionic contaminants, moisture and mechanical damage. See OVERCOAT.

PASSIVE COMPONENTS – Components that do not change their basic character when an electrical signal is applied, e.g., resistors, capacitors and inductors.

PASSIVE NETWORK – A circuit composed of multiple passive devices, deposited or discrete.

PEEL STRENGTH – In thin films, it is the force required to peel or strip a deposited film from a substrate. It is typically expressed as a gram-force.

PELLICILE – An optically transparent membrane mounted on a machined metal frame and attached to a reticle to prevent airborne contaminants or damage from handling. Contaminants on the membrane surface are out-of-focus during exposure.

PHASE DIAGRAM – Also known as an equilibrium diagram. A chart, generally, of two or more elements (an alloy) showing their phases over temperature and composition range when equilibrium has been reached.

PHOTOETCH – A process of patterning a metal film by exposing and developing a photosensitive film and using the resist as a mask to etch away exposed metal.

PHOTOETCHABLE THICK FILM – A post-fired thick film patterned using photoresist as an etch mask.

PHOTOIMAGABLE THICK FILM – A fully screened, pre-fired, thick film that is inherently sensitive to ultra violet light and can be patterned without using a photoresist and does not require chemical etching.

PHOTOMASK – Glass plate containing a pattern or image (positive or negative) to be transferred to a wafer or substrate. Used in the photolithographic process, each pattern consists of opaque areas that prevent ultra violet light from passing through and exposing an underlying photosensitive resist. Following a development step patterning of the resist is complete and can be used as a mask for etching or as a plating template.

PINHOLE – Small voids that occur in a deposited film.

PITCH – The sum of the width of a trace and the space separating two adjacent traces.

PLANARIZATION – The deposition of a film such that the surface of the film is relatively flat and unaffected by the underlying topography. Planarization is strongly dependent upon the material properties (e.g., solids content and the thickness of the coating). A planar coating is the opposite of a conformal coating.

PLASTIC ENCAPSULATED MICROCIRCUIT (PEM) – A device encapsulated with an organic material.

PLASTIC ENCAPSULATION – Mechanical and environmental protection of a completed device by embedding it in a plastic, typically an epoxy.

PLASMA – An ionized gas composed of equal number of positive and negative charges.

PLATED THROUGH-HOLE (PTH) – A hole in an organic substrate made conductive by plating the non-conductive sides of the hole to allow electrical connection from one surface to the other. The electrically conductive PTH also makes connection to inner conductor layers in a multilayer printed wiring board.

PLUG IN PACKAGE – A package with leads arranged such that they can be inserted into a socket in the vertical direction as opposed to the longitudinal direction, e.g. a flatpack.

POLYIMIDE – An insulating polymer derived by condensing an anhydride and diamine. With high Tg it used as the base material for printed wiring boards requiring higher temperature processing. Used also as an interlayer dielectric in thin film multilayer interconnects.

POLYMER – Compounds consisting of large molecules made up by a linked series of short molecules called monomers. When the shot molecules join together to form the long molecules, the material is said to have cured or polymerized. The structure of the polymer contributes most of the physical characteristics of the materials containing them.

POLYMERIZE – Bonding of two or more monomers to form a polymer. The process of polymerizing is also called curing.

POROSIT – A measure of the quality of a film, conductive or insulating, with respect to the absence of voids.

POSITIVE IMAGE – The true picture of a pattern, as opposed to the negative.

POTTING COMPOUND – Resin used to encapsulate or seal large areas of a device or combination of devices. Potting compounds are normally poured or dispensed into a device enclosure, filling the entire area.

PREFORM – A sheet of material, punched into a specific shape. Preforms are typically used for die or substrate attach, e.g., solder preforms or epoxy preforms.

PREPREG – Sheet material (e.g., glass fabric) impregnated with a resin cured to an intermediate stage (B-stage resin).

PRE SEAL VISUAL – The process in which a device or assembly is visually inspected prior to final lid sealing.

PRESSED ALUMINA – A method of making alumina parts, such as substrates, by pressing the powder in a mold and then firing.

PRINT & FIRE – A term associated with the thick film patterning process. It specifically refers to post-screen printing processing of a thick film paste that completes the patterning process.

PRINTED CIRCUIT BOARD (PCB) – A printed wiring board with assembled components. Also referred to as a Printed Wiring Board Assembly (PWBA).

PRINTED WIRING BOARD (PWB) – A organic based substrate/board – single, double-sided or multilayer with photopatterned conductor traces on both sides and all inner layers in multilayer structures forming an electrical interconnect circuit structure.

PRINTING PARAMETERS – Operating conditions that affect the screening operation such as off-contact spacing, squeegee speed, squeegee pressure, etc.

PRODUCTION LOT – Parts manufactured on the same production line(s) by means of the same production techniques, materials, controls, and design at the same time. The production lot is usually date coded to permit control and traceability as required for maintenance of reliability programs.

PROJECTION PRINTER – A photolithography exposure system that exposes an image onto a wafer or substrate by optically projecting the image from the mask. There is no physical contact between the mask and the wafer or substrate. The mask used on a projection printer is referred to as a reticle.

PULL STRENGTH – In wire bonding, it is a measure of the strength of a fully bonded wire when subjected to a destructive force, as in wire pull testing.

PURPLE PLAGUE – One of several gold-aluminum intermetallic compounds (IMC) formed when bonding gold to aluminum and activated by exposure to elevated temperature. The IMC is purple in color and very brittle that eventually leads to failure of the bond.

PULL TEST – A test to measure the amount of force needed to destructively cause a bonded wire to fail.

PUSH OFF STRENGTH – In wire bonding, the amount of force (in pounds or grams) required to separate a wedge bonded wire or a ball bond from a metallized bond pad.

PUSH OFF TEST – A test to determine quality of a bonded wire or a deposited bump.

Q

QUARTZ – Single crystal SiO_2.

R

REACTIVE or REFRACTORY METALS – A class of metals or alloys that have similar characteristics including very low electrical conductivity and very high melting temperatures. Used as conductor material in high temperature cofired ceramic (HTCC) processing requiring firing temperatures in excess of 1200°C. Readily oxidizing, a reducing atmosphere is necessary during firing. Refractory metals include molybdenum (Mo), and tungsten (W).

REAL ESTATE – Refers to the total surface area of a chip, substrate or board.

REDUCING ATMOSPHERE – An atmosphere in a furnace or oven, typically containing hydrogen, and used to prevent oxidation of parts.

REFLOW SOLDERING – Soldering technique involving application of solder followed by heating in a furnace or oven to a temperature above the melting point of the solder. The parts are bonded upon cooling and solidification of the solder.
REGISTRATION – The proper positioning of a substrate or board; the alignment of a screen or photmask to another circuit pattern on a substrate or board.
REGISTRATION MARKS – Marks used for positioning and used for aligning of photomasks for multiplayer structures.
RESIN – An organic substance that is polymeric in structure and predominantly amorphous.
RESIST – Same as Photoresist. A photosensitive coating when exposed and developed provides a patterned template for etching or selective plating.
RETICLE – A photomask used on projection printers. Typically contains a single image at IX or 5X, 10X or a grouping of the same image also at magnification.
REWORK – All work performed, except testing, on a circuit after initial fabrication in order to replace defective parts for compliance with specifications.
RHEOLOGY – Refers to the flow properties of liquids.
ROSIN FLUX – An organic acid used to clean mating surfaces prior to or during soldering.

S

SAPPHIRE – Single crystal aluminum oxide.
SCANNING ELECTRON MICROSCOPE (SEM) – A microscope that uses a beam of electrons for viewing small objects at very large magnification.
SCHEMATIC – A representative drawing in a symbolic format of an item, e.g. a process flow chart, or a detailed diagram of a functional electronic circuit.
SCREEN – A network of interwoven metal wire or fabric (a mesh) mounted on a solid frame. Upon application and selective patterning of an emulsion film on one side of the mesh the screen is ready for thick film printing.
SCREEN FRAME – A metal or plastic frame that holds the screen taut and serves as a means of mounting the screen onto the printer.
SCREEN PRINTING – The process of transferring an image to a substrate by forcing a paste, using a squeegee, through a selectively masked stencil screen.
SCRIBE LINE – The lines that separate the die from each other on a wafer. It is also referred to as the "street". It is where the dicing or singulation occurs.
SCRUBBING – Agitation of a silicon die on a gold bonding pad, at elevated temperature, to form a eutectic.
SECOND BOND – In wire bonding, the last bond that completes the attachment of the wire.
SELECTIVE PLATING – An electroplating technique whereby only certain areas are plated, typically using a patterned photoresist as the mask.
SEMICONDUCTOR – A materials that has an electrical conductivity between a conductor and an insulator. The conductivity can be changed by the introduction of impurities and the creation of selected areas with different carriers of current, i.e. electrons (n-type) and holes (p-type) and the formation of a p-n junction that is the building block of a solid-state diode, transistor, and integrated circuit.

SHEET RESISTANCE – The electrical resistance of a thin sheet of material with uniform thickness as measured across opposite sides of a unit square and is expressed in ohms/square.

SHELF LIFE – The useful life of a material, after date of manufacture. Shelf life may vary from minutes, in the case of mixed epoxies, to years.

SILICON THRU VIA – A chemically etched through hole in a silicon die, filled or plated to provide electrical connectivity. Used as the vertical interconnect for stacked die. Requires specially designed ICs.

SINGLE SIDED BOARD – A PWB with circuitry on one side only.

SIINGULATION – The process of separating individual die from a wafer.

SINTERING – The heating at an elevated temperature of two or more metals to allow interdiffusion to occur to enhance the bonding between the materials involved.

SKIN EFFECT – The increase in resistance of a conductor at microwave frequencies due to the tendency of current to concentrate at the conductor surfaces.

SLUMP – The tendency of a thick film ink to spread after printing causing vertical walls of a conductor to spread out diagonally.

SOFT SOLDER – A low temperature (generally below 300°C) melting solder alloy, e.g. eutectic SnPb 63/37.

SOLDERABILITY – The ability of a metal to be wet by solder.

SOLDER BALLS – Large solder bumps typically >200 micrometers in diameter. Solder balls are used for attachment of area array packages, e.g. BGAs, CSPs.

SOLDER BUMPS – Small balls of solder <200 micrometers in diameter used to make electrical connections on face down bonded flip chips and Wafer Level CSPs.

SOLDER DAM – A solder mask. A non-solderable material applied across a conductor to limit the spreading of molten solder. Applied by screening or dry film lamination.

SOLDERING – The process of joining parts, typically metals, by melting and solidification of a metal or metals (an alloy) having a melting point that is below that of the parts being bonded.

SOLDER RESIST – A solder mask. A photosensitive organic material patterned for selectively depositing solder material.

SOLVENT RESISTANT – The degree to which a material is unaffected by solvents.

SPUTTERING – The process of removing atoms from a source target by means of a high voltage created plasma. The dislodged atoms are deposited as a thin film onto a substrate.

SQUEEGEE – The part of a screen printer used to physically force thick film paste through a screen.

STEATITE – A ceramic composed of magnesium, aluminum and silicate.

STENCIL – A metal foil with patterns selectively etched through the foil. Stencils as opposed to screens are used where thicker films are required, e.g. solder paste is stencil printed rather than screen printed.

STEP AND REPEAT PROJECTION PRINTER – An exposure system in which the wafer or substrate onto which an image is projected is indexed from site to site in order to completely expose an entire wafer or substrate. Referred to as a Stepper.

STITCH BOND – The second bond in ball bonding.
STRESS FREE – A material state in which there is little or no internal forces causing stress.
STRESS RELIEF– The process of making a material stress free. Usually by heating (annealing).
STRIPLINE – A planar microwave transmission geometry consisting of a center conductor surrounded on both sides by an insulator.
SUBSTRATE – The base material upon which passivation layers, metallizations and circuit elements may be added to build a device, package or an assembly.
SURFACE FINISH – For substrates: A measure of the smoothness of the surface. For PWBs: The overplating of copper traces to accommodate various component attachments, e.g., soldering, wire bonding.
SURFACE MOUNT – Component attachment wherein all connections, typically solder, are made on the top surface circuitry rather than into sockets or plated through holes.
SURFACE TENSION– A force that exists between liquids and a surface.
SURFACTANT – A contraction of the words surface active agent. A chemical that promotes wetting with a liquid.
SYSTEM IN PACKAGE (SiP) – A packaged component providing full system functionality. It can refer specifically to a single package containing stacked die with all die are the same device technology, e.g. CMOS. Wire bonding is the dominant means of interconnecting the stacked die.
SYSTEM ON PACKAGE (SoP) – Same as SiP or more specifically a packaged component with full system functionality like an MCM but with stacked die, single and stacked packages. It accommodates different device technologies, Si, GaAs, SiGe, as bare or packaged die, as well as different die functions – logic, memory, rf, analog and digital. Other technologies, MEMS as well as optical components can also be included. Passives and other components including, antennas, filters, resonators, can be added to the package. A SoP might be considered as an HDI PWB assembly reduced to a single package component – in a CSP package format.

NOTE: The deference between SiP and SoP are not universally accepted within the microelectronics community. Many consider no difference and use only SiP to refer to all approaches offering full system functionality.

T

TAPE – (1) A dried and cast homogeneous slurry of ceramic powder, sintering aids and organic binders. The cast product is formed into shape and fired to form substrates and packages. Prior to the firing the tape is often referred to as “green ceramic. (2) A term used in referring to very thin (typically 25μm thick) fully cured organic materials (e.g., Kapton®, polyimide).

TAPE CASTING – The process of casting ceramic into long, flexible sheets. Tape casting is used in the manufacturing of alumina substrates.

TARNISH – Chemical changes that occur on the surface of metals due to the action of oxygen or sulfur.

TEMPERATURE AGING – Subjecting a circuit to an elevated temperature for an extended period of time intended to reduce stress and stabilize the unit.

TEMPERATURE CYCLING – A test that subjects a device or assembly to alternating high and low temperatures over an extended period of time.

TEST PATTERN – A circuit designed to provide early evaluate electrical performance and/or properties of a device or material. For example test patterns are used on wafers as part of the in-process controls to monitor the manufacturing processes.

THERMAL CONDUCTIVITY – The rate at which heat is transferred by a material.

THERMAL GRADIENT – The changes in temperature across an interface or through a material.

THERMAL MISMATCH – The differences in thermal expansion coefficient (TCE) of materials that are joined together. A mismatch in TCE between materials generates stress when subjected to any thermo-mechanical forces. Stress can result in degradation in a joint including complete separation.

THERMOPLASTIC – An organic material that can be cured reheated and remelted without change in properties.

THERMAL SHOCK – A condition whereby devices are subjected alternately to extreme heat and extreme cold. Similar to temperature cycling but the time between to the two temperature extremes is significantly shorter and sometimes executed using a liquid-to-liquid bath.

THERMOCOMPRESSION BONDING – In wire bonding: The metallurgical attachment of a wire to a device or package bond pad by application of both temperature and force.

THICK FILM – Refers to a process and materials: A patterning process involving screen printing of a thick film paste followed by drying of the printed paste and a high temperature firing (800ºC) to complete the process. Pastes are available as conductor, resistor or dielectric materials (generally greater than 10 microns thick).

THICK FILM CIRCUIT – A circuit manufactures by the thick film process.

THICK FILM TECHNOLOGY – Encompasses the thick film materials and the patterning processes.

THIN FILM – A patterning process that basically emulates the IC wafer photolithographic process. Materials are deposited, conductors typically by sputtering or electroless plating and insulators, applied by spinning and subsequently curing, or lamination. The patterning involves use of a photoresist that when patterned serves as an etch mask or a selective plate-up template. The thin film process offers the finest line resolution and highest wiring density.

THIXOTROPIC – A property of thick film pastes becoming more fluid (a decrease in viscosity) as a force is applied physically forcing the paste through the a patterned screen.

TINNED – Generally has come to mean the part has been coated with solder.

TRANSFER MOLDING – A method of packaging an IC. In a molding press a molten plastic, an epoxy, is transferred under heat and pressure into a cavity holding fully assembled devices on a lead frame.

TRIMMING – A method of accurately adjusting the value of a deposited resistor or capacitor to a desired value.

U

ULTRASONIC BONDING – In wire bonding: A wire bonding process that uses ultrasonic energy to join two metals.

UNDER BUMP METALLIZATION (UBM) – A layered metal structure deposited and patterned over Al bond pads to provide a solderable surface for the deposition or placement of solder bumps or balls for flip chip and Wafer Level CSPs.

UNDERFILL – When a die is flip chip attached the CTE mismatch of the substrate and die can create stress on the joints causing them to fail over time or extended thermal cycling. In order to reduce the stress, a polymer material is flowed or otherwise placed under the die. This material is called underfill. Underfill that flows under the die after is attached is called conventional underfill. Underfill that is placed under the die before the die is attached is called no-flow underfill.

UNDERGLAZE – A glass coating applied to a substrate to improve the surface finish prior to the deposition of any metallization.

UV CURING – The polymerization or cross linking of low molecular weight materials using ultraviolet (UV) light as the energy source.

V

VAPOR DEPOSITION – The deposition of films onto a substrate by evaporation techniques.

VEHICLE – Refers to the organic liquids (solvents or thinners) that are part of the overall make-up of a thick film paste**.** These liquids help in the mixing of the solid particles in the paste and at the same time help in adjusting the viscosity to improve the thick film screen printing process.

VERTICAL INTEGRATION – Die stacking where silicon thru vias provide interconnections between die.

VIA – An opening formed in a dielectric layer or substrate and metallized to create an electrical connection between two or more conductor layers.

VISCOSITY – The speed of fluid flow and/or the resistance to shear. Usually measured in Centipoise (csp).

VITREOUS – Glass like or glassy. The opposite of crystalline.

VITREOUS BINDER – A glass phase used in cermet pastes to promote adhesion.

VOID – A hole in an encapsulant, die attach adhesive or underfill is called a void. Voids can exist because air is trapped during the dispense and bond process (the hole is “surrounded” by polymer and gets trapped) or can form because the polymer releases gas during curing. Voids reduce the adhesion strength. They can also trap moisture and reduce the device reliability.

VOLATILES – Any material that evaporates or boils rapidly at the temperature at which it is used or processed is said to be volatile. Many organic materials that are used as solvents are volatile. If a polymer requires the use of such solvents (because it won't flow without help) it is said to contain volatile material. When volatile materials escape they can create voids and must be processed accordingly.

W

WAFER – A thin slice of semiconductor crystal. Serves as the substrate during the fabrication of the integrated circuit.
WAFER LEVEL PACKAGE (WLP) – A process (thin film) where an area array package is formed while the device is still in wafer format. Like a flip chip the package is actual die size and is therefore a CSP (a WL-CSP).
WARPAGE – See BOW.
WAVE SOLDERING – A process for soldering where board assemblies are brought into contact with a gently overflowing wave of molten solder.
WEDGE BOND – A wire bond made with a wedge tool.
WETTING – The spreading of molten solder (or glass) on a clean metal.
WIRE BONDING – A process that uses a thin wire (Au, Al, Cu) for electrically connecting a device to a package, substrate or board. Two bonds are required to complete the connection. Bonding methods include Thermocomprssion (requires application of heat and pressure to the wire; Ultrasonics (require application of pressure and ultrasonic energy but at room temperature), and Thermosonics (requires application of heat, pressure and ultrasonic energy). The bonding tool used determines types of bonds. A capillary produces a ball bond and a wedge tool a wedge or stitch bond.
WIRE SAG – The failure of bonding wire to maintain the loop described by the arc of the bonding tool.
WIRE SWEEP – The movement of bonding wire during the injection molding of the package. May result in shorting of adjacent wires.
WOVEN SCREEN – Refers to a particular type of screen used in thick film printing.

Z

Z-AXIS – The vertical out of plan direction.
Z-AXIS ADHESIVE – See anisotropic conductive adhesive.

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