cadence

Quick Reference for Encounter® RTL Compiler

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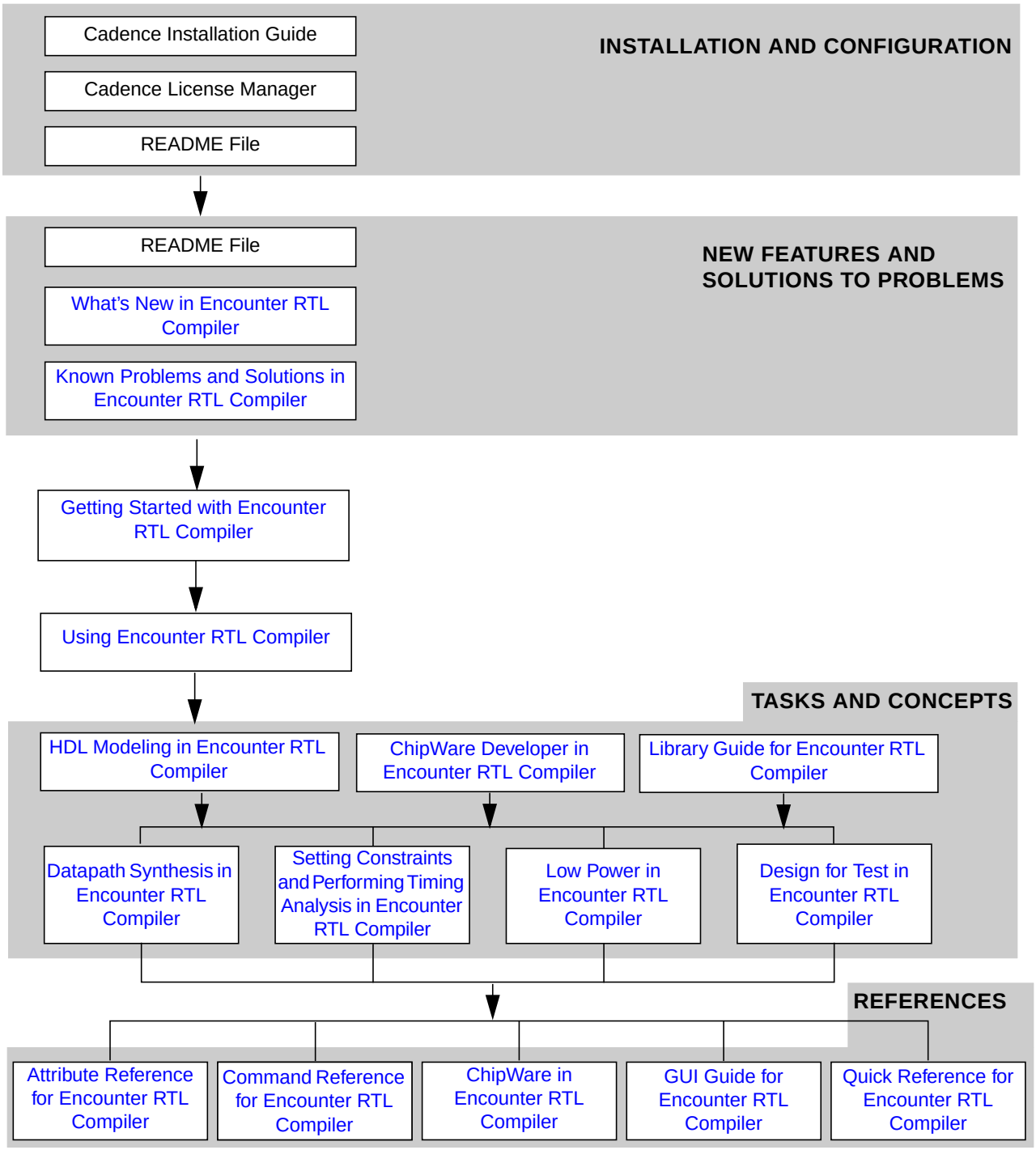
Contents

How to Use the Documentation Set



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List of Commands with Syntax

The following table provides an alphabetical listing of the commands with their syntax.

Command Listing with Syntax
add_command_help *command_name help*
all_inputs [-design *design*]
all_outputs [-design *design*]
analyze_testability [-library *string*] [-effort {low|medium|high}] [-atpg_options *string*] [-fault_sample_size *integer*] [-etlog *file*] [-directory *string*] [*design*]
basename *pathname*
cd [*directory*]
change_names [-local] [-force] [-vhdl] [-verilog] { -net | -instance | -design | -subdesign | -port_bus | -subport_bus} [-log_changes *string*] [-case_insensitive] [-prefix *string*] [-suffix *string*] [-first_restricted *string*] [-restricted *string*] [-last_restricted *string*] [-replace_char *string*] [-reserved_words *string*] [-max_length *number*] |-map *string*][-allowed *string*...]
check_design [-undriven] [-unloaded] [-multidriven] [-unresolved] [-constant] [-assigns] [-all] [*design*] [> file] 1
check_dft_rules [*design*] [-max_print_violations *integer* | > *file*] [-max_print_fanin *integer*]
clock_gating { connect_test | declone| import | insert_in_netlist | insert_obs | join | remove | share | split}
clock_gating connect_test
clock_gating declone [-hierarchical] [-no_clock_tree_traversal]

Command Listing with Syntax

```
clock_gating import
     [-start_from instance] [-hierarchical]
```

```
clock_gating insert_in_netlist
```

```
clock_gating insert_obs
     [-hierarchical] [-max_cg integer]
     [-ignore_clock_constraint]
     [-exclude instance...]
```

```
clock_gating join
     [-hierarchical] [-max_level integer]
     [-multi_fanouts] [-start_from instance]
```

```
clock_gating remove
     [-hierarchical | -cg_list instance_list]
```

```
clock_gating share
     [-hierarchical] [-max_level integer]
```

```
clock_gating split
     [-hierarchical] [-max_level integer]
     [-power_driven] [-start_from instance]
```

```
clock_ports [design] 4
```

```
configure_pad_dft -mode {input | output | tristate}
     -test_mode test_signal {pin|port}
```

```
connect_scan_chains [design]
     [-preview] [-auto_create_chains]
     [-incremental] [-chains chain_list]
     [-elements element_list] [-pack]
```

```
create_library_domain domain_list
```

```
create_mode [-design design] -name mode_names
```

```
define_attribute {-obj_type string} {-data_type string}
     [-hidden] [-help_string string]
     [-check_function string] [-compute_function string]
     [-default_value string] string
     {-category string}
```

```
define_clock -name string [-domain string]
     -period integer [-divide_period integer]
     [-rise integer] [-divide_rise integer]
     [-fall integer] [-divide_fall integer]
     [-design design] [pin|port] [-mode mode_name]...
```

```
define_cost_group [-weight integer] -name string
     [-design design]
```

Command Listing with Syntax

```
define_dft {abstract_segment | fixed_segment
     | floating_segment | preserved_segment | scan_chain
     | scan_clock_a | scan_clock_b | shift_enable
     | shift_register_segment | test_clock | test_mode }
```

```
define_dft abstract_segment [-name segment_name]
     {-module subdesign|-instance instance|-libcell cell}
     -sdi subport -sdo subport
     -clock_port subport [-fall|-rise]
     [ -tail_clock_port subport
       [-tail_edge_fall | -tail_edge_rise] ]
     { -shift_enable_port subport -active {high|low}  | -connected_shift_enable }
     [ -test_mode_port subport
       -test_mode_active {high|low} ]...
     -length integer [-skew_safe]
```

```
define_dft fixed_segment [-name segment_name]
     elem_name [elem_name] ...
```

```
define_dft floating_segment [-name segment_name]
     elem_name [elem_name] ...
```

```
define_dft preserved_segment [-name segment_name]
     { elem_name [elem_name] ... [-sdi pin] [-sdo pin]
     | -analyze -sdi {pin|port} -sdo {pin|port} }
     [-connected_shift_enable]
     [-connected_scan_clock_a]
     [-connected_scan_clock_b]
```

```
define_dft scan_chain [-name name]
     {[-sdi sdi -sdo sdo [-create_ports]
       {-shared_out [-shared_select test_signal] |
        -non_shared_out}
      [-shift_enable test_signal]
      [-head segment] [-tail segment] [-body segment]
      [-complete | -max_length integer]
      [-domain test_clock_domain [-edge {rise|fall}]]
      [-terminal_lockup {level_sensitive|edge_sensitive}]
      [-hookup_pin_sdi pin] [-hookup_pin_sdo pin]
      [-configure_pad {tm_signal | se_signal} ]
     |-analyze -sdo sdo [-sdi sdi]
       {-shared_out  | -non_shared_out} }
```

```
define_dft scan_clock_a
     [-name name] [-no_ideal] driver
     [-period integer] [-divide_period integer]
     [-rise integer] [-divide_rise integer]
     [-fall integer] [-divide_fall integer]
     [ [-hookup_pin pin [-hookup_polarity string]]
       [-configure_pad {tm_signal|se_signal}]
     | [-create_port]]
```

Command Listing with Syntax

```
define_dft scan_clock_b
     [-name name] [-no_ideal] driver
     [-period integer] [-divide_period integer]
     [-rise integer] [-divide_rise integer]
     [-fall integer] [-divide_fall integer]
     [ [-hookup_pin pin [-hookup_polarity string]]
       [-configure_pad {tm_signal|se_signal}]
     | [-create_port]]
```

```
define_dft shift_enable [-name name] -active {low|high}
     [-default] [-no_ideal]
     [ [-hookup_pin pin [-hookup_polarity string]]
       [-configure_pad {tm_signal|se_signal}]
     | [-create_port]]
     {pin|port} [-design design]
```

```
define_dft shift_register_segment [-name segment_name]
     -start_flop instance
     -end_flop instance
```

```
define_dft test_clock -name test_clock
     [-design design] [-domain test_clock_domain]
     [-period integer] [-divide_period integer]
     [-rise integer] [-divide_rise integer]
     [-fall integer] [-divide_fall integer]
     |-hookup_pin pin [-hookup_polarity string]]
     [-controllable] {pin|port} [{pin|port}] ... 1
```

```
define_dft test_mode [-name name] -active {low | high}
     [-no_ideal] [-scan_shift] driver
     [ [-hookup_pin pin [-hookup_polarity string]]
       [-configure_pad {tm_signal|se_signal}]
     | [-create_port]] [-design design] 5
```

```
define_level_shifter_group -from_library_domain library_domain
     -to_library_domain library_domain [-name string]
     -libcells cell_list
```

```
derive_environment [-name string] [-sdc_only] instance
```

```
dirname pathname
```

```
dirs
```

```
echo [-nonewline] string... [> file]
```

```
edit_netlist {bitblast_all_ports | connect
     |dedicate_subdesign | disconnect
     |group|new_design | new_instance
     |new_port_bus |new_primitive |new_subport_bus
     |ungroup | uniquify}
```

```
edit_netlist bitblast_all_ports {design|subdesign...}
```

Command Listing with Syntax

```
edit_netlist connect {pin|port|subport}
     {pin|port|subport}
```

```
edit_netlist dedicate_subdesign instance [instance]...
```

```
edit_netlist disconnect {pin|port|subport}
```

```
edit_netlist group -group_name group_name
     instance [instance]...
```

```
edit_netlist new_design -name string [-quiet]
```

```
edit_netlist new_instance [-name string]
     {design|subdesign|libcell} [-quiet]
     {subdesign|design}
```

```
edit_netlist new_port_bus -name string
     [-left_bit integer] [-right_bit integer]
     {-input|-output|-input -output}
     [design]
```

```
edit_netlist new_primitive [-name string] [-inputs integer]
     [-quiet] logic_function {design|subdesign}
```

```
edit_netlist new_subport_bus -name string
     [-left_bit integer] [-right_bit integer]
     {-input|-output|-input -output}
     instance
```

```
edit_netlist ungroup [-prefix string] instance...
```

```
edit_netlist uniquify {subdesign|design}
```

```
elaborate [-parameters integer...] [top_module_name]...
     [-libpath path]... [-libext extension]...
```

```
encrypt [-vlog] [-vhdl] [-pragma] input_file_name [> file]
```

```
exit
```

```
external_delay
     {-input min_rise min_fall max_rise max_fall
     |-output min_rise min_fall max_rise max_fall}
     [-clock  object] [-edge_rise | -edge_fall]
     [-level_sensitive] [-accumulate]
     [-name string] {port|pin}... [-mode mode_name]
```

```
fanin [-min_logic_depth integer] [-max_logic_depth integer]
     [-min_pin_depth integer] [-max_pin_depth integer]
     [-startpoints] [-structural] {pin | port | subport}... 5
```

```
fanout [-min_logic_depth integer] [-max_logic_depth integer]
     [-min_pin_depth integer] [-max_pin_depth integer]
     [-endpoints] [-structural] {pin | port}... 8
```

Command Listing with Syntax

```
filter [-invert] [-regexp] attribute_name
     attribute_value ... [object_list...]
```

```
find root_path [-maxdepth integer] [-mindepth integer]
          [-ignorecase] [-vname] [-option...|*] object
```

```
fix_dft_violations
     { -clock -test_mode test_signal
       [-test_clock_pin {pin|port} [-rise | -fall]]
     | { -async_set | -async_reset
       | -async_set -async_reset }
       [ -async_control test_signal]
       -test_mode test_signal
       [-insert_observe_scan
         -test_clock_pin {pin|port} [-rise | -fall]]}
     [-violations violation_object_id_list]
     [-preview] [-dont_check_dft_rules] [dont_map]
      [-design design] 8
```

```
get_attribute {attribute_name [object]
     |-h type [attribute_name]}
```

```
get_user_attribute attribute_name object
```

```
hdl_create binding binding_name -operator operator_name
     [hdl_comp | bindings]
```

```
hdl_create component component_name [hdl_lib | components] 1
```

```
hdl_create implementation implementation_name
     [-v5 | -v01 | -vhdl | -vhdl]
     [hdl_comp | implementations] 3
```

```
hdl_create library library_name 5
```

```
hdl_create operator operator_name [-signed | -unsigned] 6
```

```
hdl_create package pkg_name -path path_to_pkg [hdl_lib | packages] 7
```

```
hdl_create parameter parameter_name [-hdl_invisible]
     [hdl_comp | parameters] 9
```

```
hdl_create pin pin_name {-input | -output | -inout}
     [pins | hdl_oper | hdl_comp]
```

```
help [command]...[> file]
```

```
include file...
```

```
inout_mate {subport_bus|port_bus|subport|port|pin}
```

```
insert_dft
     { analyzed_test_points  shadow | test_point
     | user_test_point | wrapper_cell }
```

Command Listing with Syntax

```
insert_dft analyzed_test_points [-library string]
     {-input_tp_file file
     | [-atpg [-atpg_effort {low|medium|high}]
       [-atpg_options string]]
       [-rrfa_effort {low|medium|high}]
       [-rrfa_options string] [-output_tp_file file]}
     [-max_number_of_testpoints integer ]
     [-min_slack integer] [-test_mode test_signal]
     [-test_clock_pin {port|pin}][design]
```

```
insert_dft lockup_element
     actual_scan_chain [actual_scan_chain]...
```

```
insert_dft shadow_logic -around instance
     [-test_mode test_signal]
     {-mode bypass
     |-mode no_share -test_clock_pin {port|pin}
          [-fall |-rise]
     |-mode share -test_clock_pin {port|pin}
          [-fall |-rise] }
     [-exclude pins | -only pins ] [-group pins]...
     [-balance] [-dont_map] [-preview]
```

```
insert_dft test_point -location {pin|port}...
     -test_mode test_signal
     -type {async_0 | async_1 | async_any
          | control_0 | control_1
          | control_node -node {pin|port}
          | control_observe_0 | control_observe_1
          | control_observe_node -node {pin|port}
          | control_scan | -observe_scan | scan
          | sync_0 | sync_1 | sync_any }
     [-test_clock_pin {pin|port} [-fall|-rise] ]
     [-dont_map]
```

```
insert_dft user_test_point -location {pin|port|subport}
     -cell {design|subdesign|libcell}
     -cfi {pin|port} [-cfo {pin|port}]
     -connect string [-connect string]...
     -name name
```

```
insert_dft wrapper_cell -location pin_list
     [-floating_location_ok]
     [-skipped_locations_variable Tcl_variable]
     [-shared_through {buffer|combinational}]
     [-wck pin] -wsen pin
     {-decoded_select_cfi pin
     |-wint pin -wext pin [-wcap pin]}
     [-guard {0|1} -wig pin -wog pin]
     [-name segment_prefix]
```

Command Listing with Syntax

```
lcd directory
```

```
level_shifter {check | import | insert | remove | update}
```

```
level_shifter check
```

```
level_shifter import
```

```
level_shifter insert [-from_library_domain library_domain]
     [-to_library_domain library_domain]
     [-instance_from instance...]
     [-instance_to instance...]
     [-location {from | to}]
     [-dedicate_level_shifter libcell]
```

```
level_shifter remove
     { [instance]...
     | [-from_library_domain library_domain...]
       [-to_library_domain library_domain...]
       [-instance_from instance_list]
       [-instance_to instance_list]
       [-hierarchical] }
       [-invalid_only]
```

```
level_shifter update
```

```
license {checkout | list}
```

```
license checkout [-wait]
```

```
license list
```

```
lls directory
```

```
lpwd
```

```
ls [-computed] [-attribute] [-long] [-dir]
     [-width integer] [object]... [>file]
```

```
man { command_name | attribute_name | message_ID}
```

```
mesg_make -group string -id number
     -short_desc string -long_desc string
     {-error|-warning|-info_priority number}
```

```
mesg_send message string
```

```
multi_cycle
     { {-from {instance|external_delay|clock|port|pin}...
       |-through {instance|port|pin}...[-through...]...
       |-to {instance|external_delay|clock|port|pin}...}...
       |-paths string}
     [-launch_shift integer]
     [-capture_shift integer] [-name string] [-lenient]
     [-mode mode_name]
```

Command Listing with Syntax

```
mv [-flexible] object new_name [-slash_ok]
```

```
parse_options cmd file_var [args] [str var]...
```

```
path_adjust
     { {-from {instance|external_delay|clock|port|pin}...
       |-through {instance|port|pin}...[-through...]...
       |-to {instance|external_delay|clock|port|pin}...}...
       |-paths string }
     -delay integer [-name string] [-lenient]
     [-mode mode_name]
```

```
path_delay
     { {-from {instance|external_delay|clock|port|pin}...
       |-through {instance|port|pin}...[-through...]...
       |-to {instance|external_delay|clock|port|pin}...}...
       |-paths string}
     -delay integer [-name string] [-lenient]
     [-mode mode_name]
```

```
path_disable
     { {-from {instance|external_delay|clock|port|pin}...
       |-through {instance|port|pin}...[-through...]...
       |-to {instance|external_delay|clock|port|pin}...}...
       |-paths string}
     [-name string] [-lenient] [-mode mode_name]
```

```
path_group
     {{-from {instance|external_delay|clock|port|pin}...
      |-through {instance|port|pin}...[-through...]...
      |-to {instance|external_delay|clock|port|pin}...}...
      |-paths string}
     [-name string] -group string [-lenient]
     [-mode mode_name]
```

```
popd
```

```
predict_qos [-reference_config_file string]
     [-parasitic_output_file string]
     [-abandon_existing_placement] [design]
```

```
pushd directory
```

```
pwd
```

```
quit
```

Command Listing with Syntax

```
rc [-cmdfile string] [-E] [-execute command] [-files file]...
     [-gui] [-lsf_cpus integer] [-lsf_queue string]
     [-logfile log_file_name] [-no_custom] [-nologfile]
     [-queue] [-use_license {RTL_Compiler_L |
     RTL_Compiler_Ultra | RTL_Compiler_Verification |
     FE_GPS | SOC_Encounter_GPS | First_Encounter_GXL |
     SOC_Encounter_GXL | Virtuoso_Digital_Implement}]
      [-vdi] [-version]
```

```
read_def def_file
```

```
read_dfm coefficients_filename
```

```
read_dft_abstract_model
     [-ctl [-segment_prefix string] [-instance instance]]
      file
```

```
read_encounter config configuration_file
```

```
read_hdl [-v5 | -v01 | -sv | -vhdl]
     [-library library_name]
     [-top top_module_name]
     [-define macro=value] file_list
     [-netlist]
```

```
read_netlist [-top top_module_name] [-define macro=value] file_list
```

```
read_saif [-scale scale_factor]
     [-update [-weight weight_factor]]
     [-instance instance] file
```

```
read_sdc [-stop_on_errors] [-no_compress] [-mode mode_name] file
```

```
read_spef spef_file
```

```
read_tcf [-scale scale_factor]
     [-update [-weight weight_factor]]
     [-verbose] [-instance instance]
     [-ignorecase] file
```

```
redirect [-append] [-tee] [-variable] target command
```

```
remove_assigns [-buffer libcell] [design | subdesign]
```

```
replace_scan [design]
```

```
report {area | clock_gating | clocks | datapath
     | design_rules | dft_chains | dft_registers
     | dft_setup | gates | hierarchy | instance
     | level_shifter | memory | messages | nets
     | operand_isolation | port | power | qor
     | summary | timing | yield}
```

```
report area {-depth integer] [-min_count integer] [design]... [> file]
```

Command Listing with Syntax

```
report clock_gating
     { [-gated_ff] [-ungated_ff] [-detail] [-summary]
       [-no_hierarchical] [-cg_instance instance...]
     | [-multi_stage]} [> file]
```

```
report clocks [-ideal] [-generated] [clock]...[> file] [-mode mode_name]
```

```
report datapath [-full_path] [-no_header] [-no_area_statistics] [-mux] [-all]
     [design] [-max_width string] [> file]
```

```
report design_rules [design]... [> file]
```

```
report dft_chains [design] [> file]
```

```
report dft_registers [-pass_tdrc] [-fail_tdrc]
     [-lockup] [-latch] [-dont_scan] [-misc]
     [-shift_reg] [design] [> file]
```

```
report dft_setup design [> file]
```

```
report dft_violations [-async] [-clock]
     [-abstract] [-shiftreg]
     design [> file]
```

```
report gates [-power] [design]
     [-library_domain library_domain_list] [> file]
```

```
report hierarchy -module string [-filename string] [design]
```

```
report instance [-timing] [-power] instance... [> file]
```

```
report memory [> file]
```

```
report messages [-all] [-include_suppressed] [-error]
     [-warning] [-info] [> file]
```

```
report nets [-pin pin...] [-minfanout integer] [-maxfanout integer]
     [net |instance]... [-sort string] [-cap_worst integer] [> file]
```

```
report operand_isolation
     [-oi_instance instance...] [> file]
```

```
report port [-delay] [-driver] [-load] port... [> file]
```

```
report power
     {-rtl [-detail] [-flat [-nworst number]] [-sort mode]
          [instance]...
     | [-hier | -flat [-nworst number]] [-depth number]
          [-sort mode] [instance | net]... }
     [> file]
```

```
report qor [-levels_of_logic] [design]... [> file]
```

Command Listing with Syntax

```
report scan_power [-clock float]
     [ -flop float
     | -atpg [-atpg_options string]
     | -scan_vectors file ]
     [-library string] [> file}
```

```
report sequenial [-instance_hier instance] [-hier] [subdesign |design] [> file]
```

```
report summary [design]... [> file]
```

```
report timing [-endpoints] [-lint] [-full_pin_names]
     [-num_paths integer] [-slack_limit integer]
     [-worst integer]
     [-from {instance|external_delay|clock|port|pin}...]
     [-through {instance|port|pin}...]...
     [-to {instance|external_delay|clock|port|pin}...]
     [-paths string] [-exceptions exception...]
     [-cost_group cost_group] [> file]
     [-mode mode_name]
```

```
report yield [-depth integer] [-min_count integer]
     [> file]
```

```
report level_shifter
     { [instance_list]
     | [-detail] [-hierarchical]
       [-from_library_domain library_domain...]
       [-to_library_domain library_domain...]
       [-instance_from instance_list]
       [-instance_to instance_list] }
      [> file]
```

```
reset_attribute [-quiet] attribute_name [object...] | -h type [attribute_name]}
```

```
reset_design [-verbose] [design]
```

```
reset_scan_equivalent [libcell]...
```

```
resume
```

```
retime [-prepare] [-min_area] [-min_delay]
     [-effort {high | medium | low}]
      [design|subdesign ...]
```

```
rm object... [-quiet]
```

```
set_attribute
     { attribute_name attribute_value [objects] [-quiet]
     | -h type [attribute_name]}
```

```
set_compatible_test_clocks
     {-all | list_of_test_clocks} [-design design]
```

Command Listing with Syntax

```
set_scan_equivalent
     -non_scan_cell libcell -scan_cell libcell
     [-tieoff_pins string] [-pin_map list_of_pin_groups]
```

```
set_user_attribute attribute_name attribute_value object
```

```
sh command_string
```

```
specify_paths
     {-from {pin|port|clock|external_delay|instance}... |
     -from_rise_clock {pin|port|clock|external_delay|instance}... |
     -from_fall_clock {pin|port|clock|external_delay|instance}... |
     -from_rise_pin {pin|port|clock|external_delay|instance}... |
     -from_fall_pin {pin|port|clock|external_delay|instance}... |
     -through {pin|port|instance}... |
     -through_rise_pin {pin|port|instance}... |
     -through_fall_pin {pin|port|instance}...[-through...]...|
     -to {pin|port|clock|external_delay|instance}... |
     -to_rise_clock {pin|port|clock|external_delay|instance}... |
     -to_fall_clock {pin|port|clock|external_delay|instance}... |
     -to_rise_pin {pin|port|clock|external_delay|instance}... |
     -to_fall_pin {pin|port|clock|external_delay|instance}... }
     [-capture_clock_pins pin... |
     -capture_clock_pins_rise_clock pin... |
     -capture_clock_pins_fall_clock pin... |
     -capture_clock_pins_rise_pin pin... |
     -capture_clock_pins_fall_pin pin... ]
     [-lenient] [-mode mode_name] [-domain clock_domain]
```

```
state_retention {define_driver | define_map | swap}
```

```
state_retention define_driver
     [-replace] [-hierarchical]
     [-pin_class string]
     [-driver {pin|port}]
     [-driver_polarity {active_low|active_high}]
     [-instances instance_list] 0
```

```
state_retention define_map
     [-hierarchical]
     [-cell_type string]
     [-hdl_proc_name string]
     [-instances instance_list] 2
```

```
state_retention swap
     [-hierarchical]
     [-start_from instance]
     [-connect_power_gating_pins] 4
```

```
suppress_messages [-n integer] message_id...
```

```
suspend
```

Command Listing with Syntax

```
synthesize [-csa_effort {high|medium|low}]
     [-effort {high|medium|low}]
     [-to_generic] [-to_mapped] [-incremental]
     [-no_incremental] [design]...
```

```
ungroup [-all] [-flatten] [-simple] [-only_user_hierarchy]
     [-threshold <integer>][-exclude instance...] instance...
```

```
unsuppress_messages message_id...
```

```
what_is object
```

```
write_atpg
     { -cadence [> file] | -mentor | -stil [> file]}
     [-decimals_ok] [-picoseconds]
     [-test_clock_waveform test_clock]
     [-apply_inputs_at integer]
     [-apply_bidirs_at integer]
     [-strobe_outputs_at integer]
     [-strobe_width integer]
```

```
write_dft_abstract_model [-ctl] [design] [> file]
```

```
write_do_lec [-top string] [-golden_design string]
     [-revised_design string] [-sim_lib string]
     [-sim_plus_liberty] [-logfile string] [-env_var string]
     [-hier] [-flat] [-no_exit] [-save_session string]
     [-verbose] [> file]
```

```
write_encounter design [-basename string]
     [-gzip_files][-reference_config_file config_file]
     [-preserve_avoid_cells] [-ignore_scan_chains]
     [-ignore_library_domains] [-floorplan string]
     [-lef lef_files] [design]
```

```
write_forward_saif
     [-library library_path...|-library_domain library_domain]
     [ > file ] 5
```

```
write_hdl [-suffix string] {design|subdesign}...
     [-abstract] [-generic] [-depth integer]
     [-equation] [ > file]
```

```
write_scandef
     [-partition partition -chains chain [chain]...]...
     [-version {5.4|5.5}]
     [-end_chains_before_lockups]
     [-dont_use_timing_model_pins] [design] [ > file]
```

```
write_script [-hdl] [design] [> file]
```

```
write_sdc [-dc]  [-version {1.1|1.3|1.4}] [-strict]
     [design] [> file] [-mode mode_name]
```

Command Listing with Syntax

```
write_tcf [-duration simulation_period] [-computed]
     [-hierarchical] [-include_hier_ports] [> file] 7
```

```
write_template [-split] [-no_sdc] [-dft] [-power] [-full] [-simple] [-area]
     [-retime] [-n2n] [-msv] [-multimode] [> -outfile] string
```

2

List of Attributes by Object Type

List of Attributes by Object Type

actual_scan_chain	
analyzed {true | false}	RO
connected_shift_enable {true | false}	RO
domain *string*	RO
edge {rise | fall | any}	RO
elements *string*	RO
reg_count *integer*	RO
scan_clock_a *string*	RO
scan_clock_b *string*	RO
scan_in *string*	RO
scan_out *string*	RO
shared_output {true | false}	RO
shared_select *string*	RO
shift_enable *string*	RO
terminal_lockup *string*	RO
actual_scan_segment	
active {low | high}	RO
clock *string*	RO
clock_edge {fall | rise}	RO
connected_scan_clock_a {true | false}	RO
connected_scan_clock_b {true | false}	RO
connected_shift_enable {true | false}	RO
core_wrapper {true | false}	RO
dft_tail_test_clock *string*	RO
dft_tail_test_clock_edge {rise | fall}	RO
dft_test_clock *string*	RO
dft_test_clock_edge {rise | fall}	RO
elements *string*	RO
instance *string*	RO
reg_count *integer*	RO

scan_clock_a *string*	RO
scan_clock_b *string*	RO
scan_in *string*	RO
scan_out *string*	RO
shift_enable *string*	RO
skew_safe {true | false}	RO
tail_clock *string*	RO
tail_clock_edge {rise | fall}	RO
type {abstract | fixed | floating | preserve | shift_register}	RO
clock	
clock_hold_uncertainty *integer*	RW
clock_network_early_latency *integer*	RW
clock_network_late_latency *integer*	RW
clock_setup_uncertainty {*integer* | *string*}	RW
clock_source_early_latency *integer*	RW
clock_source_late_latency *integer*	RW
divide_fall *integer*	RO
divide_period *integer*	RO
divide_rise *integer*	RO
exceptions *string*	RO
fall *integer*	RO
inverted_sources *string*	RW
latch_max_borrow {*float* | no_value}	RW
non_inverted_sources *string*	RW
period *integer*	RO
rise *integer*	RO
slew {min_rise min_fall max_rise max_fall}	RW
constant	
net *string*	RO
pin_capacitance *string*	RO
unique_versions *string*	RO
wire_capacitance *string*	RO

cost_group	
exceptions *string*	RO
slack {*float* | no_value}	RO
slack_by_mode *string*	RO
tns *string*	RO
weight *integer*	RW
design	
arch_filename *string*	RW
area *string*	RO
cell_area *string*	RO
cell_count *integer*	RO
checkpoint_dofile_naming_style *name*	RW
checkpoint_netlist_naming_style *name*	RW
def_file *def_filename*	RO
dft_connect_scan_data_pins_during_mapping {loopback | floating | ground}	RW
dft_connect_shift_enable_during_mapping {tie_off | floating}	RW
dft_dont_scan {true | false}	RW
dft_lockup_element_type {level_sensitive | edge_sensitive}	RW
dft_max_length_of_scan_chains {*integer* | no_value}	RW
dft_min_number_of_scan_chains {integer | no_value}	RW
dft_mix_clock_edges_in_scan_chains {true | false}	RW
dft_scan_map_mode {tdrc_pass | force_all | preserve}	RW
dft_scan_output_preference {auto | non_inverted | inverted}	RW
entity_filename *string*	RW
force_wireload {*custom_wireload* | none | auto_select |inherit}	RW
fplan_height *microns*	RW
fplan_width *microns*	RW
hdl_filelist **{***hdl_library language_standard* **{***hdl_file* ...**}** **}**...	RW
hdl_parameters *string current_value*	RO
hdl_user_name *string*	RW
ideal_seq_async_pins {true | false}	RW
ignore_library_drc {true | false}	RW

ignore_library_max_fanout {true | false}	RW
latch_borrow {*float* | no_value}	RW
latch_borrow_by_mode **{***mode_name_1 delay_value***}** [**{***mode_name_1 delay_value***}**]...	RW
latch_max_borrow {*float* | no_value}	RW
latch_max_borrow_by_mode **{***mode_name_1 delay_value***}** [**{***mode_name_2 delay_value***}**]...	RW
library_domain *domain*	RW
lp_clock_gating_add_obs_port {true | false}	RW
lp_clock_gating_add_reset {true | false}	RW
lp_clock_gating_cell *path_name_for_cell*	RW
lp_clock_gating_control_point {none | precontrol | postcontrol}	RW
lp_clock_gating_exclude {true | false}	RW
lp_clock_gating_max_flops *integer*	RW
lp_clock_gating_min_flops *integer*	RW
lp_clock_gating_module *string*	RW
lp_clock_gating_style {none | latch | ff}	RW
lp_clock_gating_test_signal *test_signal_object*	RW
lp_default_probability *float*	RW
lp_default_toggle_rate *float*	RW
lp_internal_power *float*	RO
lp_leakage_power *float*	RO
lp_map_to_srpg_cells {true | false | *srpg_libcell*}	RW
lp_net_power *float*	RO
lp_optimize_dynamic_power_first {true | false}	RW
lp_power_optimization_weight *float*	RW
lp_srpg_pg_driver *string*	RW
max_cap_cost *string*	RO
max_capacitance {*float* | no_value}	RW
max_dynamic_power *float*	RW
max_fanout {*float* | no_value}	RW
max_fanout_cost *string*	RO
max_leakage_power *float*	RW

max_trans_cost *string*	RO
max_transition {*integer* | no_value}	RW
net_area *string*	RO
preserve {true | false | delete_ok | map_size_ok | size_ok | size_delete_ok}	RW
retime {true | false}	RW
slack {*float* | no_value}	RO
slack_by_mode {{*mode_name_1 delay_value*} [{*mode_name_2 delay_value*}]...}	RO
state *string*	RW
timing_driven_muxopto {true | false}	RW
tns *string*	RO
user_defined *string*	RW
wireload *string*	RO
yield *number*	RW
exception	
adjust_value {*float* | no_value}	RO
cost_group *string*	RO
delay_value {*float* | no_value}	RO
exception_type {multi_cycle | path_delay | path_disable | path_adjust | path_group}	RO
from_points *string*	RO
lenient {true | false}	RO
max {true | false}	RW
paths *string*	RO
precluded_path_adjusts *string*	RO
priority *integer*	RO
shift_capture {*integer* | no_value}	RO
shift_launch {*integer* | no_value}	RO
through_points *string*	RO
to_points *string*	RO
user_priority *integer*	RW
external_delay	
clock *string*	RO

clock_network_latency_included {true | false}	RW
clock_rise {true | false}	RO
clock_source_latency_included {true | false}	RW
delay *integer_list*	RO
exceptions *string*	RO
external_delay_pins *string*	RO
input_delay {true | false}	RO
level_sensitive {true | false}	RO
hdl_arch	
library_domain *domain*	RW
location *pathname*	RO
ungroup {true | false}	RW
hdl_bind	
avoid {true | false}	RW
constraint *constraint_setting*	RW
operator *operator_name*	RO
param_association *string*	RW
pin_association *string*	RW
priority *integer*	RW
unbound_oper_pin *unbound_setting*	RW
hdl_comp	
avoid {true | false}	RW
location *pathname*	RW
ungroup {true | false}	RW
hdl_comp_arch	
avoid {true | false}	RW
location *pathname*	RO
ungroup {true | false}	RW
hdl_impl	
avoid {true | false}	RW
language *language_version*	RO

legal *formula*	RW
location *pathname*	RW
pre_elab_script {*UNIX_path*}	RW
preserve_techelts {true | false | delete_ok | map_size_ok | size_ok | size_delete_ok }	RW
priority *integer*	RW
technology *library_name*	RW
ungroup {true | false}	RW
hdl_inst	
component *string*	RO
preferred_impl *implementation_name* [*hdl_inst_pathname*]	RW
ungroup {true | false}	RW
hdl_label	
preferred_comp {*component_name*}	RW
preferred_impl {*implementation_name*}	RW
hdl_lib	
avoid {true | false}	RW
is_chipware {true | false}	RW
hdl_oper	
signed {true | false}	RO
hdl_pack	
default_location *pathname*	RO
location *pathname*	RO
hdl_param	
formula *string*	RW
hdl_parameter {true | false}	RO
hdl_pin	
bit_width *formula*	RW
direction {input | output | inout}	RO
permutable_group *group_name*	RW

hdl_proc	
group *string*	RW
hdl_subp	
map_to_module *string*	RO
map_to_operator *string*	RO
return_port *string*	RO
instance	
buffer {true | false}	RO
cell_area *string*	RO
dft_abstract_dont_scan {true | false}	RO
dft_dont_scan {true | false}	RW
dft_inherited_dont_scan {true | false}	RO
dft_mapped {true | false}	RO
dft_part_of_segment {abstract | fixed | floating | preserve | shift_register}	RO
dft_status {Passes DFT Rules | Fails DFT Rules | Abstract Dont Scan | Dont scan | Misc non scan}	RO
dft_test_clock *string*	RO
dft_test_clock_edge {rise | fall}	RO
dft_test_clock_source {*pin*|*port*|*bus*}	RO
dft_violation {clock | async set | async reset} #(violation_Id_number)	RO
disabled_arcs {0 | 1 | no_value}	RW
disabled_arcs_by_mode **{***mode_name_1 libarcs***}** [**{***mode libarcs***}**]...	RW
dont_retime {true | false}	RW
exceptions *string*	RO
file_row_col *Tcl_list*	RO
flop {true | false}	RO
hard_region {true | false}	RW
hdl_proc_name *string*	RW
hierarchical {true | false}	RO
inherited_preserve {true | false | delete_ok | map_size_ok | size_ok | size_delete_ok}	RO
inverter {true | false}	RO

latch {true | false}	RO
latch_borrow {*float* | no_value}	RW
latch_borrow_by_mode **{***mode_name_1 delay_value***}** [**{***mode_name_2 delay_value***}**]...	RW
latch_max_borrow {*float* | no_value}	RW
latch_max_borrow_by_mode **{{***mode_name_1 delay_value***}** [**{***mode_name_2 delay_value***}**]...**}**	RW
libcell *string*	RW
library_domain *domain*	RO
lp_clock_gating_exclude {true | false}	RW
lp_default_probability *float*	RW
lp_default_toggle_rate *float*	RW
lp_internal_power *float*	RO
lp_leakage_power *float*	RO
lp_map_to_srpg_cells {true | false | *srpg_libcell*}	RW
lp_map_to_srpg_type *string*	RW
lp_net_power *float*	RO
lp_srpg_pg_driver **{{***class driver polarity***}...}**	RW
preserve {true | false | delete_ok | map_size_ok | size_ok | size_delete_ok}	RW
primitive_function *string*	RO
retime_original_registers *register_name*	RO
sequential {true | false}	RO
slack {*float* | no_value}	RO
subdesign *string*	RO
timing_case_disabled_arcs *string*	RO
timing_case_disabled_arcs_by_mode {*mode_name_1* {*libarc_a libarc_b*...}} [*mode_name_2* {*libarc_c libarc_d*...}]...}	RO
timing_model {true | false}	RO
trace_retime {true | false}	RW
tristate {true | false}	RO
unique_versions *string*	RO
unresolved {true | false}	RW
user_defined *string*	RW

write_vlog_port_association_style {default | positional | named | }	RW
level_shifter_group	
from_library_domain *string*	RO
level_shifter_cells *string*	RO
to_library_domain *string*	RO
libarc	
enabled {true | false}	RW
from_pin *path*	RO
liberty_attributes *string*	RO
real_enabled {true | false}	RO
type { borrow_arc | clear_arc | clock_edge_arc | combo_arc | hold_arc | preset_arc | recovery_arc | removal_arc | setup_arc | tristate_disable_arc | tristate_enable_arc }	RO
libcell	
adder {true |false}	RO
area *string*	RW
asynch_clear *string*	RO
asynch_preset *string*	RO
avoid {true | false}	RW
buffer {true | false}	RO
cell_leakage_power *float*	RW
clock *string*	RO
clock_gating_integrated_cell *string*	RO
combinational {true | false}	RO
flop {true | false}	RO
inverter {true | false}	RO
is_clock_gating_cell {true | false}	RO
is_isolation_cell {true | false}	RW
is_level_shifter {true | false}	RO
latch {true | false}	RO
latch_enable *string*	RO
liberty_attributes *string*	RO

pad {true | false}	RO
power_gating_cell {true | false}	RO
power_gating_cell_type *string*	RW
preserve {true | false}	RW
scan_enable *string*	RO
scan_in *string*	RO
sequential {true | false}	RO
sync_clear *string*	RO
sync_enable *string*	RO
sync_preset *string*	RO
timing_model {true | false}	RO
tristate {true | false}	RO
usable {true | false}	RO
user_defined *string*	RW
libpin	
async_clear_phase {active_high | active_low | none}	RO
async_preset_phase {active_high | active_low | none}	RO
capacitance *string*	RW
clock_gate_clock_pin {true | false}	RO
clock_gate_enable_pin {true | false}	RO
clock_gate_obs_pin {true | false}	RO
clock_gate_out_pin {true | false}}	RO
clock_gate_reset_pin {true | false}	RO
clock_gate_test_pin {true | false}	RO
clock_phase {active_high | active_low | none}	RO
fanout_load *float*	RO
function *string*	RO
higher_drive *string*	RO
incoming_timing_arcs *string*	RO
input {true | false}	RO
internal {true | false}	RO
is_iq_function {true | false}	RO

is_iqn_function {true | false}	RO
isolation_cell_enable_pin {true | false}	RW
latch_enable_phase {active_high | active_low | none}	RO
level_shifter_enable_pin {true | false}	RO
liberty_attributes *string*	RO
lower_drive *string*	RO
outgoing_timing_arcs *string*	RO
output {true | false}	RO
power_gating_pin_class *string*	RO
power_gating_pin_phase {active_low | active_high | none}	RO
scan_enable_phase {active_high | active_low | none}	RO
scan_in_phase {active_high | active_low | none}	RO
signal_level *string*	RO
sync_clear_phase {active_high | active_low | none}	RO
sync_enable_phase {active_high | active_low | none}	RO
sync_preset_phase {active_high | active_low | none}	RO
tristate {true | false}	RO
user_defined *string*	RW
library	
cap_scale_in_fF *float*	RO
default_power_rail *string*	RO
default_wireload *string*	RW
files *string*	RO
leakage_power_scale_in_nW *float*	RO
liberty_attributes *string*	RO
power_rails *Tcl_list*	RO
time_scale_in_ps *integer*	RO
usable_comb_cells *integer*	RO
usable_seq_cells *integer*	RO
usable_timing_models *integer*	RO
version *string*	RO

library_domain	
active_operating_conditions *string*	RO
is_default {true|false}	RW
library **{{***lib* [*lib*]...**}** [**{***lib* [*lib*]...**}**]...**}**	RW
operating_conditions *string*	RW
power_library *domain*	RW
wireload_selection {*table* | none | default}	RW
message	
count *integer*	RO
help *string*	RO
id *integer*	RO
max_print {*integer* |no_value}	RW
print_count *integer*	RO
priority *integer*	RO
severity {Info | Error | Warning}	RO
type *string*	RO
message_group	
is_user {true | false}	RO
net	
drivers *string*	RO
ideal {true | false}	RO
loads *string*	RO
logic0_driven {true| false}	RO
logic1_driven {true| false}	RO
lp_asserted_probability *float*	RW
lp_asserted_toggle_rate *float*	RW
lp_computed_probability *float*	RO
lp_computed_toggle_rate *float*	RO
lp_net_power *float*	RO
lp_probability_type {asserted | clock | computed | constant | default}	RO
lp_toggle_rate_type {asserted | clock | computed | constant | default}	RO

num_drivers *integer*	RO
num_loads *integer*	RO
preserve {true | false | delete_ok}	RW
unique_versions *string*	RO
user_defined *string*	RW
operating_condition	
liberty_attributes *string*	RO
process *string*	RW
temperature *string*	RW
tree_type *string*	RW
voltage *string*	RW
pin	
break_timing_paths {true | false | propagate_slews}	RW
capturer {true | false}	RO
causes_ideal_net {true | false}	RO
clock_hold_uncertainty *integer*	RW
clock_network_early_latency *integer*	RW
clock_network_late_latency *integer*	RW
clock_setup_uncertainty {*integer* | *string*}	RW
clock_source_early_latency *integer*	RW
clock_source_late_latency *integer*	RW
clock_sources_inverted *string*	RO
clock_sources_non_inverted *string*	RO
connect_delay {*float* | no_value}	RO
dft_controllable *string*	RW
direction {in | out | inout}	RO
endpoint {true | false}	RO
exceptions *string*	RO
external_delays *string*	RO
external_delays_by_mode {*mode external_delay*} [{*mode external_delay*}]...}	RO
ideal_driver {true | false}	RW
ideal_network {true | false}	RW

inverting_clocks *string*	RO
latch_max_borrow {*float* | no_value}	RW
latch_max_borrow_by_mode **{***mode*_name_1 *delay_value***}** [**{***mode_name_2 delay_value***}**]...	RW
launcher {true | false}	RO
libpin *string*	RO
lp_asserted_probability *float*	RW
lp_asserted_toggle_rate *float*	RW
lp_computed_probability *float*	RO
lp_computed_toggle_rate *float*	RO
lp_net_power *float*	RO
lp_probability_type {asserted | clock | computed | constant | default}	RO
lp_toggle_rate_type {asserted | clock | computed | constant | default}	RO
net *string*	RO
non_inverting_clocks *string*	RO
pin_capacitance {*float* | no_value}	RO
preserve {true | false | delete_ok}	RW
propagated_clocks *pin_name*	RO
propagated_clocks_by_mode {{*mode_name_1* [*clock_info_1*]...} [{*mode_name_2* [*clock_info_2*]...}]...}	RO
propagated_ideal_network {true | false }	RO
prune_unused_logic {true | false}	RW
rf_slack *rise fall*	RO
slack {*float* | no_value}	RO
slack_by_mode {{*mode_name_1 delay_value*} [{*mode_name_2 delay_value*}]...}	RO
slew {*rise fall*}	RO
startpoint {true | false}	RO
timing_arcs *string*	RO
timing_case_computed_value {0 | 1 | no_value}	RO
timing_case_computed_value_by_mode {*mode* [0 | 1]} [{*mode* [0 | 1]}]...	RO
timing_case_logic_value {0 | 1 | no_value}	RW
timing_case_logic_value_by_mode **{***mode_name_1 case_analyis_value***}** [**{***mode_name_2 case_analysis_value***}**]...	RW

unique_versions *string*	RO
user_defined *string*	RW
wire_capacitance {*float* | no_value}	RO
wire_resistance {*float* | no_value}	RO
wireload_model *string*	RO
pin_bus	
bits *string*	RO
port	
break_timing_paths {true | false | propagate_slews}	RW
bus *string*	RO
causes_ideal_net {true | false}	RO
clock_hold_uncertainty *integer*	RW
clock_network_early_latency *integer*	RW
clock_network_late_latency *integer*	RW
clock_setup_uncertainty {*integer* | *string*}	RW
clock_source_early_latency *integer*	RW
clock_source_late_latency *integer*	RW
clock_sources_inverted *string*	RO
clock_sources_non_inverted *string*	RO
connect_delay {*float* | no_value}	RO
direction {in | out | inout}	RO
endpoint {true | false}	RO
exceptions *string*	RO
external_delays *string*	RO
external_delays_by_mode {*mode external_delay*} [{*mode external_delay*}]...	RO
external_driven_pin_fall *string*	RW
external_driven_pin_rise *string*	RW
external_driver {min_rise min_fall max_rise max_fall}	RW
external_driver_from_pin {min_rise min_fall max_rise max_fall}	RW
external_driver_input_slew {*integer* | no_value}	RW
external_fanout_load {*float* | no_value}	RW
external_non_tristate_drivers *integer*	RW

external_pin_cap {*float* | no_value}	RW
external_resistance {min_rise min_fall max_rise max_fall}	RW
external_wire_cap {*float* | no_value}	RW
external_wire_res {*float* | no_value}	RW
external_wireload_fanout {*integer* | no_value}	RW
external_wireload_model *string*	RW
fixed_slew {min_rise min_fall max_rise max_fall}	RW
ideal_driver {true | false}	RW
ideal_network {true | false}	RW
ignore_external_driver_drc {true | false}	RW
lp_asserted_probability *float*	RW
lp_asserted_toggle_rate *float*	RW
lp_computed_probability *float*	RO
lp_computed_toggle_rate *float*	RO
lp_net_power *float*	RO
lp_probability_type {asserted | clock | computed | constant | default}	RO
lp_toggle_rate_type {asserted | clock | computed | constant | default}	RO
max_capacitance {*float* | no_value}	RW
max_fanout {*float* | no_value}	RW
max_transition {*integer* | no_value}	RW
net *string*	RO
pin_capacitance {*float* | no_value}	RO
port_delay {*rise fall*}	RO
propagated_clocks *port_name*	RO
propagated_clocks_by_mode {*mode_name_1* [*clock_info_1*]...} [{*mode_name_2* [*clock_info_2*]...}]...	RO
rf_slack *rise fall*	RO
slack {*float* | no_value}	RO
slack_by_mode {{*mode_name_1 delay_value*} [{*mode_name_2 delay_value*}]...}	RO
slew {*rise fall*}	RO
startpoint {true | false}	RO
timing_case_computed_value {0 | 1 | no_value}	RO

timing_case_computed_value_by_mode {{*mode* [0 | 1]} [{*mode* [0 | 1]}]...}	RO
timing_case_logic_value {0 | 1 | no_value}	RW
timing_case_logic_value_by_mode **{***mode_name_1 case_analyis_value***}** [**{***mode_name_2 case_analysis_value***}**]...	RW
unique_versions *string*	RO
user_defined *string*	RW
wire_capacitance {*float* | no_value}	RO
wire_resistance {*float* | no_value}	RO
port_bus	
bits *string*	RO
direction {in | out | inout}	RO
order *integer*	RO
root	
active_operating_conditions *string*	RO
area_per_unit_len {*float*}	RW
aspect_ratio *number*	RW
bit_blasted_port_style *string*	RW
bsub_options *bsub_option_name*	RW
bus_naming_style *string*	RW
cap_table_file {capacitance_table_file}	RW
capacitance_per_unit_len {*float*}	RW
case_analysis_sequential_propagation {true | false}	RW
checkpoint_flow {true | false}	RW
command_log *string*	RW
delayed_pragma_commands_interpreter *string*	RW
delete_unloaded_insts {true | false}	RW
delete_unloaded_seqs {true | false}	RW
derive_bussed_pins {true | false}	RW
dft_identify_internal_test_clocks {true | false}	RW
dft_prefix *string*	RW
dft_report_empty_test_clocks {true | false}	RW
dft_scan_style {muxed_scan | clocked_lssd_scan}	RO

dp_area_mode {true | false}	RW
dp_perform_csa_operations {true | false}	RW
dp_perform_sharing_operations {true | false}	RW
dp_perform_speculation_operations {true | false}	RW
dp_postmap_downsize {true | false}	RW
dp_postmap_upsize {true | false}	RW
drc_first {true | false}	RW
endpoint_slack_opto {true | false}	RW
exact_match_seqs_async_controls {true | false}	RW
find_object_threshold *integer*	RW
gen_module_prefix *string*	RW
hdl_allow_inout_const_port_connect {true | false}	RW
hdl_array_naming_style *string*	RW
hdl_async_set_reset "*comma_separated_list_of_signals*"	RW
hdl_auto_async_set_reset {true | false}	RW
hdl_auto_sync_set_reset {true | false}	RW
hdl_bit_blast_threshold *integer*	RW
hdl_delete_transparent_latches {true | false}	RW
hdl_enable_proc_name {true | false}	RW
hdl_error_on_blackbox {true | false}	RW
hdl_error_on_latch {true | false}	RW
hdl_ff_keep_explicit_feedback {true | false}	RW
hdl_ff_keep_feedback {true | false}	RW
hdl_filelist **{***hdl_library language_standard* **{***hdl_file* ...**} }**...	RW
hdl_infer_unresolved_from_logic_abstract {true | false}	RW
hdl_language {v5 | v1 |vhdl |sv}	RW
hdl_latch_keep_feedback {true | false}	RW
hdl_max_loop_limit *integer*	RW
hdl_max_recursion_limit *integer*	RW
hdl_parameter_naming_style *string*	RW
hdl_preserve_dangling_output_nets {true | false}	RW
hdl_preserve_unused_registers {true | false}	RW

hdl_record_naming_style	RW
hdl_reg_naming_style *string*	RW
hdl_search_path *Tcl_list*	RW
hdl_sync_set_reset "*comma_separated_list_of_signals*"	RW
hdl_track_filename_row_col {true | false}	RW
hdl_trim_target_index {true | false}	RW
hdl_unconnected_input_port_value {0 | 1 | X | none}	RW
hdl_undriven_output_port_value {0 | 1 | X | Z | none}	RW
hdl_undriven_signal_value {0 | 1 | X | none}	RW
hdl_use_default_parameter_values_in_name {true | false}	RW
hdl_use_parameterized_module_by_name {true | false}	RW
hdl_use_port_default_value {true | false}	RW
hdl_use_techelt_first {true | false}	RW
hdl_vector_naming_style *string*	RW
hdl_vhdl_case {lower | upper | original}	RW
hdl_vhdl_environment {common | synopsys}	RW
hdl_vhdl_lrm_compliance {true | false}	RW
hdl_vhdl_preferred_architecture *string*	RW
hdl_vhdl_read_version {7 | 3}	RW
ignore_scan_combinational_arcs {true | false}	RW
ignore_unknown_embedded_commands {true | false}	RW
information_level *integer*	RW
input_asynchro_reset_blk_pragma *string*	RW
input_asynchro_reset_pragma *string*	RW
input_case_cover_pragma *string*	RW
input_case_decode_pragma *string*	RW
input_map_to_mux_pragma *string*	RW
input_pragma_keyword *string*	RW
input_synchro_reset_blk_pragma *string*	RW
input_synchro_reset_pragma *string*	RW
inst_prefix *string*	RW
interconnect_mode {ple | wireload}	RW

lef_library {lef_library}	RW
lib_lef_consistency_check_enable {true | false}	RW
lib_search_path *Tcl_list*	RW
library **{{***lib* [*lib*]...**}** [**{***lib* [*lib*]...**}**]...**}**	RW
lp_clock_gating_prefix *string*	RW
lp_insert_clock_gating {true | false}	RW
lp_insert_operand_isolation {true | false}	RW
lp_multi_vt_optimization_effort {low | medium | high}	RW
lp_operand_isolation_prefix *string*	RW
lp_power_analysis_effort {low | medium | high}	RW
lp_power_unit *power_unit*	RW
lp_toggle_rate_unit *toggle_unit*	RW
memory_limit *integer*	RW
memory_usage *integer*	RO
merge_seqs_into_multibit_cells {true | false}	RW
multibit_seqs_from_different_banks {true | false}	RW
multibit_seqs_members_naming_style {list_of_strings}	RW
number_of_routing_layers *integer*	RW
operating_conditions *string*	RW
optimize_constant_0_flops {true | false}	RW
optimize_constant_1_flops {true | false}	RW
optimize_constant_latches {true | false}	RW
optimize_yield {true | false}	RW
parse_control_command *string*	RW
path *string*	RW
platform_wordsize *integer*	RO
program_name *string*	RO
program_short_name *string*	RO
program_version *string*	RO
resistance_per_unit_len {*float*}	RW
retime_reg_naming_suffix { string }	RW
runtime *float*	RO

scale_of_cap_per_unit_len {*float*}	RW
scale_of_res_per_unit_len {*float*}	RW
script_begin *string*	RW
script_end *string*	RW
script_search_path *string*	RW
site_size *microns*	RW
source_verbose {true | false}	RW
stdout_log *log_file_name*	RW
super_thread_servers {*machine_names*}	RW
synthesis_off_command *string*	RW
synthesis_on_command *string*	RW
time_recovery_arcs {true | false}	RW
ui_respects_preserve {true | false}	RW
ungroup_separator *string*	RW
uniquify_naming_style *string*	RW
unmap_scan_flops {false | not_mapped_for_dft | true}	RW
use_scan_seqs_for_non_dft {true|false}	RW
wireload_mode {default | physical | top | enclosed| segmented}	RW
wireload_selection {*table* | none | default}	RW
wlec_cut_point *string*	RW
wlec_env_var *string*	RW
wlec_flat_r2n {true | false}	RW
wlec_lib_statetable {true | false}	RW
wlec_new_hier_comp {true | false}	RW
wlec_no_exit {true | false}	RW
wlec_save_ssion *string*	RW
wlec_sim_lib *string*	RW
wlec_sim_plus_lib {true | false}	RW
wlec_uniquify {true | false}	RW
wlec_use_lec_model {true | false}	RW
wlec_verbose {true | false}	RW
write_vlog_bit_blast_constants {true | false}	RW

write_vlog_bit_blast_mapped_ports {true | false}	RW
write_vlog_declare_wires {true | false}	RW
write_vlog_empty_module_for_logic_abstract {true | false}	RW
write_vlog_line_wrap_limit *integer*	RW
write_vlog_no_negative_index {true | false}	RW
write_vlog_top_module_first {true | false}	RW
write_vlog_unconnected_port_style { none | partial | full }	RW
scan_chain	
body *string*	RO
complete {true | false}	RO
dft_hookup_pin_sdi {*pin*|*port*|*bus*}	RO
dft_hookup_pin_sdo {*pin*|*port*|*bus*}	RO
domain *string*	RO
edge {rise | fall | any}	RO
head *string*	RO
max_length *integer*	RO
scan_clock_a *string*	RO
scan_clock_b *string*	RO
scan_in *string*	RO
scan_out *string*	RO
shared_output {true | false}	RO
shared_select *string*	RO
shift_enable *string*	RO
tail *string*	RO
terminal_lockup {none | level_sensitive | edge_sensitive}	RO
scan_segment	
active {low | high}	RO
clock *string*	RO
clock_edge {fall | rise}	RO
connected_scan_clock_a {true | false}	RO
connected_scan_clock_b {true | false}	RO
connected_shift_enable {true | false}	RO

core_wrapper {true | false}	RO
dft_status {Passes DFT Rules | Fails DFT Rules}	RO
dft_tail_test_clock *string*	RO
dft_tail_test_clock_edge {rise | fall}	RO
dft_test_clock *string*	RO
dft_test_clock_edge {rise | fall}	RO
dft_violation {abstract_testmode | clock | async set | async reset} #(violation_Id_number)	RO
elements *string*	RO
instance *string*	RO
reg_count *integer*	RO
scan_clock_a *string*	RO
scan_clock_b *string*	RO
scan_in *string*	RO
scan_out *string*	RO
shift_enable *string*	RO
skew_safe {true | false}	RO
tail_clock *string*	RO
tail_clock_edge {fall | rise}	RO
test_modes *string*	RO
type {abstract | fixed | floating | preserve | shift_register}	RO
seq_function	
d_function *string*	RW
subdesign	
allow_csa_subdesign {true | false}	RW
allow_sharing_subdesign {true | false}	RW
allow_speculation_subdesign {true | false}	RW
arch_filename *string*	RW
boundary_opto {true | false}	RW
candidate_impls {{impl_directory_1 bind_name_1}{impl_directory_2 bind_name_2} ...}	RO
cell_area *string*	RO

cell_count *integer*	RO
delete_unloaded_seqs {true | false}	RW
dft_dont_scan {true | false}	RW
entity_filename *string*	RW
force_wireload {none | auto_select | inherit}	RW
fplan_height *microns*	RW
fplan_width *microns*	RW
hard_region {true | false}	RW
hdl_filelist **{***hdl_library language_standard* **{***hdl_file* ...**} }**...	RW
hdl_parameters *string current_value*	RO
hdl_user_name *string*	RW
instances *string*	RO
library_domain *domain*	RW
logical_hier {true | false}	RO
lp_clock_gating_exclude {true | false}	RW
preserve {true | false | delete_ok | map_size_ok | size_ok | size_delete_ok}	RW
retime {true | false}	RW
retime_hard_region { true | false }	RW
selected_impl {impl_directory bind_name}	RO
speed_grade {very_slow | slow | medium| fast | very_fast}	RO
sub_arch *string*	RO
timing_driven_muxopto {true | false}	RW
user_defined *string*	RW
user_speed_grade {very_slow | slow | medium | fast | very_fast}	RW
user_sub_arch {booth | non-booth}	RW
wireload *string*	RO
subport	
bus *string*	RO
causes_ideal_net {true | false}	RO
direction {in | out| inout}	RO
lp_asserted_probability *float*	RW
lp_asserted_toggle_rate *float*	RW

lp_computed_probability *float*	RO
lp_computed_toggle_rate *float*	RO
lp_net_power *float*	RO
lp_probability_type {asserted | clock | computed | constant | default}	RO
lp_toggle_rate_type {asserted | clock | computed | constant | default}	RO
net *string*	RO
pin_capacitance {*float* | no_value}	RO
unique_versions *string*	RO
user_defined *string*	RW
wire_capacitance {*float* | no_value}	RO
wire_resistance {*float* | no_value}	RO
subport_bus	
bits *string*	RO
direction {in | out| inout}	RO
order *integer*	RO
test_clock	
controllable {true | false}	RW
dft_hookup_pin {*pin*|*port*|*bus*}	RO
dft_hookup_polarity {inverted|non_inverted}	RO
divide_fall *integer*	RW
divide_period *integer*	RW
divide_rise *integer*	RW
fall *integer*	RW
off_state {0 | 1}	RO
period *integer*	RW
rise *integer*	RW
root_source_pins *list*	RO
root_source_polarity {inverting | non_inverting}	RO
sources *string*	RW
user_defined {true|false}	RO
test_signal	

active {low | high}	RW
dedicated_pin {true | false}	RW
default_shift_enable {true| false}	RW
dft_hookup_pin {*pin*|*port*|*bus*}	RO
dft_hookup_polarity {inverted|non_inverted}	RO
divide_fall *integer*	RW
divide_period *integer*	RW
divide_rise *integer*	RW
fall *integer*	RW
ideal {true| false}	RW
period *integer*	RW
pin *string*	RW
rise *integer*	RW
scan_shift {true | false}	RW
type {scan_clock_a| scan_clock_b| shift_enable | test_mode}	RW
user_defined {true|false}	RO
violation	
description *string*	RO
file_name *string*	RO
fixed {true | false}	RO
endpoints string	RO
id *integer*	RO
line_number *integer*	RO
reg_count *integer*	RO
registers *instance_list*	RO
root_node {*pin* | *port* | *bus*}	RO
segments *list*	RO
type {async | clock}	RO
wireload	
fanout_cap *string*	RW
liberty_attributes *string*	RO

3

List of Attributes and Associated Object Types

The following table provides an alphabetical listing of the attributes with their syntax.

Attribute Listing with Syntax	Object Type
active {low | high}	actual_scan_segment scan_segment test_signal
active_operating_conditions *string*	library_domain root
adder {true |false}	libcell
adjust_value {*float* | no_value}	exception
allow_csa_subdesign {true | false}	subdesign
allow_sharing_subdesign {true | false}	subdesign
allow_speculation_subdesign {true | false}	subdesign
analyzed {true | false}	actual_scan_chain
arch_filename *string*	design subdesign
area *string*	design libcell
area_per_unit_len {*float*}	root
aspect_ratio *number*	root
async_clear_phase {active_high | active_low | none}	libpin
async_preset_phase {active_high | active_low | none}	libpin
asynch_clear *string*	libcell

Attribute Listing with Syntax	Object Type
asynch_preset *string*	libcell
avoid {true | false}	hdl_bind hdl_comp hdl_comp_arch hdl_impl hdl_lib libcell
bit_blasted_port_style *string*	root
bit_width *formula*	hdl_pin
bits *string*	pin_bus port_bus subport_bus
body *string*	scan_chain
boundary_opto {true | false}	subdesign
break_timing_paths {true | false | propagate_slews}	pin port
bsub_options *bsub_option_name*	root
buffer {true | false}	instance libcell
bus *string*	port subport
bus_naming_style *string*	root
candidate_impls {{impl_directory_1 bind_name_1}{impl_directory_2 bind_name_2} ...}	subdesign
cap_scale_in_fF *float*	library
cap_table_file {capacitance_table_file}	root
capacitance *string*	libpin
capacitance_per_unit_len {*float*}	root
capturer {true | false}	pin
case_analysis_sequential_propagation {true | false}	root

Attribute Listing with Syntax	Object Type
causes_ideal_net {true | false}	pin port subport
cell_area *string*	design instance subdesign
cell_count *integer*	design subdesign
cell_leakage_power *float*	libcell
checkpoint_dofile_naming_style *name*	design
checkpoint_flow {true | false}	root
checkpoint_netlist_naming_style *name*	design
clock *string*	actual_scan_segment external_delay libcell scan_segment
clock_edge {fall | rise}	actual_scan_segment scan_segment
clock_gate_clock_pin {true | false}	libpin
clock_gate_enable_pin {true | false}	libpin
clock_gate_obs_pin {true | false}	libpin
clock_gate_out_pin {true | false}}	libpin
clock_gate_reset_pin {true | false}	libpin
clock_gate_test_pin {true | false}	libpin
clock_gating_integrated_cell *string*	libcell
clock_hold_uncertainty *integer*	clock pin port
clock_network_early_latency *integer*	clock pin port

Attribute Listing with Syntax	Object Type
clock_network_late_latency *integer*	clock pin port
clock_network_latency_included {true | false}	external_delay
clock_phase {active_high | active_low | none}	libpin
clock_rise {true | false}	external_delay
clock_setup_uncertainty {*integer* | *string*}	clock pin port
clock_source_early_latency *integer*	clock pin port
clock_source_late_latency *integer*	clock pin port
clock_source_latency_included {true | false}	external_delay
clock_sources_inverted *string*	pin
	port
clock_sources_non_inverted *string*	pin
	port
combinational {true | false}	libcell
command_log *string*	root
complete {true | false}	scan_chain
component *string*	hdl_inst
connect_delay {*float* | no_value}	pin port
connected_scan_clock_a {true | false}	actual_scan_segment scan_segment
connected_scan_clock_b {true | false}	actual_scan_segment scan_segment

Attribute Listing with Syntax	Object Type
connected_shift_enable {true | false}	actual_scan_chain actual_scan_segment scan_segment
constraint *constraint_setting*	hdl_bind
controllable {true | false}	test_clock
core_wrapper {true | false}	actual_scan_segment scan_segment
cost_group *string*	exception
count *integer*	message
d_function *string*	seq_function
dedicated_pin {true | false}	test_signal
def_file *def_filename*	design
default {true|false}	library_domain
default_location *pathname*	hdl_pack
default_power_rail *string*	library
default_shift_enable {true| false}	test_signal
default_wireload *string*	library
delay *integer_list*	external_delay
delay_value {*float* | no_value}	exception
delayed_pragma_commands_interpreter *string*	root
delete_unloaded_insts {true | false}	root
delete_unloaded_seqs {true | false}	root subdesign
derive_bussed_pins {true | false}	root
description *string*	violation
dft_abstract_dont_scan {true | false}	instance
dft_connect_scan_data_pins_during_mapping {loopback | floating | ground}	design
dft_connect_shift_enable_during_mapping {tie_off | floating}	design
dft_controllable *string*	pin

Attribute Listing with Syntax	Object Type
dft_dont_scan {true | false}	design instance subdesign
dft_hookup_pin {*pin*|*port*|*bus*}	test_clock test_signal
dft_hookup_pin_sdi {*pin*|*port*|*bus*}	scan_chain
dft_hookup_pin_sdo {*pin*|*port*|*bus*}	scan_chain
dft_hookup_polarity {inverted|non_inverted}	test_clock test_signal
dft_identify_internal_test_clocks {true | false}	root
dft_inherited_dont_scan {true | false}	instance
dft_lockup_element_type {level_sensitive | edge_sensitive}	design
dft_mapped {true | false}	instance
dft_max_length_of_scan_chains {*integer* | no_value}	design
dft_min_number_of_scan_chains {integer | no_value}	design
dft_mix_clock_edges_in_scan_chains {true | false}	design
dft_part_of_segment {abstract | fixed | floating | preserve | shift_register}	instance
dft_prefix *string*	root
dft_report_empty_test_clocks {true | false}	root
dft_scan_map_mode {tdrc_pass | force_all | preserve}	design
dft_scan_output_preference {auto | non_inverted | inverted}	design
dft_scan_style {muxed_scan | clocked_lssd_scan}	root
dft_status {Passes DFT Rules | Fails DFT Rules | Abstract Dont Scan | Dont scan | Misc non scan}	instance
dft_status {Passes DFT Rules | Fails DFT Rules}	scan_segment
dft_tail_test_clock *string*	actual_scan_segment scan_segment
dft_tail_test_clock_edge {rise | fall}	actual_scan_segment scan_segment

Attribute Listing with Syntax	Object Type
dft_test_clock *string*	actual_scan_segment instance scan_segment
dft_test_clock_edge {rise | fall}	actual_scan_segment instance scan_segment
dft_test_clock_source {*pin*|*port*|*bus*}	instance
dft_violation {abstract_testmode | clock | async set | async reset} #(violation_Id_number)	scan_segment
dft_violation {clock | async set | async reset} #(violation_Id_number)	instance
direction {in | out | inout}	pin port port_bus subport subport_bus
direction {input | output | inout}	hdl_pin
disabled_arcs {0 | 1 | no_value}	instance
disabled_arcs_by_mode **{***mode_name_1 libarcs***}** [**{***mode libarcs***}**]...	instance
divide_fall *integer*	clock test_clock test_signal
divide_period *integer*	clock test_clock test_signal
divide_rise *integer*	clock test_clock test_signal
domain *string*	actual_scan_chain scan_chain
dont_retime {true | false}	instance
dp_area_mode {true | false}	root
dp_perform_csa_operations {true | false}	root

Attribute Listing with Syntax	Object Type
dp_perform_sharing_operations {true | false}	root
dp_perform_speculation_operations {true | false}	root
dp_postmap_downsize {true | false}	root
dp_postmap_upsize {true | false}	root
drc_first {true | false}	root
drivers *string*	net
edge {rise | fall | any}	actual_scan_chain scan_chain
elements *string*	actual_scan_chain actual_scan_segment scan_segment
enabled {true | false}	libarc
endpoint {true | false}	pin port
endpoint_slack_opto {true | false}	root
endpoints *string*	violation
entity_filename *string*	design subdesign
exact_match_seqs_async_controls {true | false}	root
exception_type {multi_cycle | path_delay | path_disable | path_adjust | path_group}	exception
exceptions *string*	clock cost_group external_delay instance pin port
external_delay_pins *string*	external_delay
external_delays *string*	pin port
external_delays_by_mode {*mode external_delay*} [{*mode external_delay*}]...	port

Attribute Listing with Syntax	Object Type
	pin
external_driven_pin_fall *string*	port
external_driven_pin_rise *string*	port
external_driver {min_rise min_fall max_rise max_fall}	port
external_driver_from_pin {min_rise min_fall max_rise max_fall}	port
external_driver_input_slew {*integer* | no_value}	port
external_fanout_load {*float* | no_value}	port
external_non_tristate_drivers *integer*	port
external_pin_cap {*float* | no_value}	port
external_resistance {min_rise min_fall max_rise max_fall}	port
external_wire_cap {*float* | no_value}	port
external_wire_res {*float* | no_value}	port
external_wireload_fanout {*integer* | no_value}	port
external_wireload_model *string*	port
fall *integer*	clock test_clock test_signal
fanout_cap *string*	wireload
fanout_load *float*	libpin
file_name *string*	violation
file_row_col *Tcl_list*	instance
files *string*	library
find_object_threshold *integer*	root
fixed {true | false}	violation
fixed_slew {min_rise min_fall max_rise max_fall}	port
flop {true | false}	instance libcell
force_wireload {*custom_wireload* | none | auto_select |inherit}	design
force_wireload {none | auto_select | inherit}	subdesign

Attribute Listing with Syntax	Object Type
formula *string*	hdl_param
fplan_height *microns*	design subdesign
fplan_width *microns*	design subdesign
from_library_domain *string*	level_shifter_group
from_pin *path*	libarc
from_points *string*	exception
function *string*	libpin
gen_module_prefix *string*	root
group *string*	hdl_proc
hard_region {true | false}	instance subdesign
hdl_allow_inout_const_port_connect {true | false}	root
hdl_array_naming_style *string*	root
hdl_async_set_reset "*comma_separated_list_of_signals*"	root
hdl_auto_async_set_reset {true | false}	root
hdl_auto_sync_set_reset {true | false}	root
hdl_bit_blast_threshold *integer*	root
hdl_delete_transparent_latches {true | false}	root
hdl_enable_proc_name {true | false}	root
hdl_error_on_blackbox {true | false}	root
hdl_error_on_latch {true | false}	root
hdl_ff_keep_explicit_feedback {true | false}	root
hdl_ff_keep_feedback {true | false}	root
hdl_filelist **{***hdl_library language_standard* **{***hdl_file* ...**}** **}**...	design root subdesign
hdl_infer_unresolved_from_logic_abstract {true | false}	root

Attribute Listing with Syntax	Object Type
hdl_language {v5 | v1 |vhdl |sv}	root
hdl_latch_keep_feedback {true | false}	root
hdl_max_loop_limit *integer*	root
hdl_max_recursion_limit *integer*	root
hdl_parameter {true | false}	hdl_param
hdl_parameter_naming_style *string*	root
hdl_parameters *string current_value*	design subdesign
hdl_preserve_dangling_output_nets {true | false}	root
hdl_preserve_unused_registers {true | false}	root
hdl_proc_name *string*	instance
hdl_record_naming_style	root
hdl_reg_naming_style *string*	root
hdl_search_path *Tcl_list*	root
hdl_sync_set_reset "*comma_separated_list_of_signals*"	root
hdl_track_filename_row_col {true | false}	root
hdl_trim_target_index {true | false}	root
hdl_unconnected_input_port_value {0 | 1 | X | none}	root
hdl_undriven_output_port_value {0 | 1 | X | Z | none}	root
hdl_undriven_signal_value {0 | 1 | X | none}	root
hdl_use_default_parameter_values_in_name {true | false}	root
hdl_use_parameterized_module_by_name {true | false}	root
hdl_use_port_default_value {true | false}	root
hdl_use_techelt_first {true | false}	root
hdl_user_name *string*	design subdesign
hdl_vector_naming_style *string*	root
hdl_vhdl_case {lower | upper | original}	root

Attribute Listing with Syntax	Object Type
hdl_vhdl_environment {common | synopsys}	root
hdl_vhdl_lrm_compliance {true | false}	root
hdl_vhdl_preferred_architecture *string*	root
hdl_vhdl_read_version {7 | 3}	root
head *string*	scan_chain
help *string*	message
hierarchical {true | false}	instance
higher_drive *string*	libpin
id *integer*	message violation
ideal {true | false}	net test_signal
ideal_driver {true | false}	pin port
ideal_network {true | false}	pin port
ideal_seq_async_pins {true | false}	design
ignore_external_driver_drc {true | false}	port
ignore_library_drc {true | false}	design
ignore_library_max_fanout {true | false}	design
ignore_scan_combinational_arcs {true | false}	root
ignore_unknown_embedded_commands {true | false}	root
incoming_timing_arcs *string*	libpin
information_level *integer*	root
inherited_preserve {true | false | delete_ok | map_size_ok | size_ok | size_delete_ok}	instance
input {true | false}	libpin
input_asynchro_reset_blk_pragma *string*	root
input_asynchro_reset_pragma *string*	root
input_case_cover_pragma *string*	root

Attribute Listing with Syntax	Object Type
input_case_decode_pragma *string*	root
input_delay {true | false}	external_delay
input_map_to_mux_pragma *string*	root
input_pragma_keyword *string*	root
input_synchro_reset_blk_pragma *string*	root
input_synchro_reset_pragma *string*	root
inst_prefix *string*	root
instance *string*	actual_scan_segment scan_segment subdesign
interconnect_mode {ple | wireload}	root
internal {true | false}	libpin
inverted_sources *string*	clock
inverter {true | false}	instance libcell
inverting_clocks *string*	pin
is_chipware {true | false}	hdl_lib
is_clock_gating_cell {true | false}	libcell
is_iq_function {true | false}	libpin
is_iqn_function {true | false}	libpin
is_isolation_cell {true | false}	libcell
is_level_shifter {true | false}	libcell
is_user {true | false}	message_group
isolation_cell_enable_pin {true | false}	libpin
language *language_version*	hdl_impl
latch {true | false}	instance libcell
latch_borrow {*float* | no_value}	design instance

Attribute Listing with Syntax	Object Type
latch_borrow_by_mode **{***mode_name_1 delay_value***}** [**{***mode_name_1 delay_value***}**]...	design instance
latch_enable *string*	libcell
latch_enable_phase {active_high | active_low | none}	libpin
latch_max_borrow {*float* | no_value}	clock design instance pin
latch_max_borrow_by_mode **{{***mode_name_1 delay_value***}** [**{***mode_name_2 delay_value***}**]...**}**	instance design pin
launcher {true | false}	pin
leakage_power_scale_in_nW *float*	library
lef_library {lef_library}	root
legal *formula*	hdl_impl
lenient {true | false}	exception
level_sensitive {true | false}	external_delay
level_shifter_cells *string*	level_shifter_group
level_shifter_enable_pin {true | false}	libpin
lib_lef_consistency_check_enable {true | false}	root
lib_search_path *Tcl_list*	root
libcell *string*	instance
liberty_attributes *string*	libarc libcell libpin library operating_condition wireload
libpin *string*	pin
library **{{***lib* [*lib*]...**}** [**{***lib* [*lib*]...**}**]...**}**	library_domain root

Attribute Listing with Syntax	Object Type
library_domain *domain*	design hdl_arch instance subdesign
line_number *integer*	violation
loads *string*	net
location *pathname*	hdl_arch hdl_comp hdl_comp_arch hdl_impl hdl_pack
logic0_driven {true| false}	net
logic1_driven {true| false}	net
logical_hier {true | false}	subdesign
lower_drive *string*	libpin
lp_asserted_probability *float*	net pin port subport
lp_asserted_toggle_rate *float*	net pin port subport
lp_clock_gating_add_obs_port {true | false}	design
lp_clock_gating_add_reset {true | false}	design
lp_clock_gating_cell *path_name_for_cell*	design
lp_clock_gating_control_point {none | precontrol | postcontrol}	design
lp_clock_gating_exclude {true | false}	design instance subdesign
lp_clock_gating_max_flops *integer*	design
lp_clock_gating_min_flops *integer*	design
lp_clock_gating_module *string*	design

Attribute Listing with Syntax	Object Type
lp_clock_gating_prefix *string*	root
lp_clock_gating_style {none | latch | ff}	design
lp_clock_gating_test_signal *test_signal_object*	design
lp_computed_probability *float*	net pin port subport
lp_computed_toggle_rate *float*	net pin port subport
lp_default_probability *float*	design instance
lp_default_toggle_rate *float*	design instance
lp_insert_clock_gating {true | false}	root
lp_insert_operand_isolation {true | false}	root
lp_internal_power *float*	design instance
lp_leakage_power *float*	design instance
lp_map_to_srpg_cells {true | false | *srpg_libcell*}	design instance
lp_map_to_srpg_type *string*	instance
lp_multi_vt_optimization_effort {low | medium | high}	root
lp_net_power *float*	design instance net pin port subport
lp_operand_isolation_prefix *string*	root
lp_optimize_dynamic_power_first {true | false}	design

Attribute Listing with Syntax	Object Type
lp_power_analysis_effort {low | medium | high}	root
lp_power_optimization_weight *float*	design
lp_power_unit *power_unit*	root
lp_probability_type {asserted | clock | computed | constant | default}	net pin port subport
lp_srpg_pg_driver **{{***class driver polarity***}...}**	instance
lp_srpg_pg_driver *string*	design
lp_toggle_rate_type {asserted | clock | computed | constant | default}	net pin port subport
lp_toggle_rate_unit *toggle_unit*	root
map_to_module *string*	hdl_subp
map_to_operator *string*	hdl_subp
max {true | false}	exception
max_cap_cost *string*	design
max_capacitance {*float* | no_value}	design port
max_dynamic_power *float*	design
max_fanout {*float* | no_value}	design port
max_fanout_cost *string*	design
max_leakage_power *float*	design
max_length *integer*	scan_chain
max_print {*integer* |no_value}	message
max_trans_cost *string*	design
max_transition {*integer* | no_value}	design port
memory_limit *integer*	root

Attribute Listing with Syntax	Object Type
memory_usage *integer*	root
merge_seqs_into_multibit_cells {true | false}	root
multibit_seqs_from_different_banks {true | false}	root
multibit_seqs_members_naming_style {list_of_strings}	root
net *string*	constant pin port subport
net_area *string*	design
non_inverted_sources *string*	clock
non_inverting_clocks *string*	pin
num_drivers *integer*	net
num_loads *integer*	net
number_of_routing_layers *integer*	root
off_state {0 | 1}	test_clock
operating_conditions *string*	library_domain root
operator *operator_name*	hdl_bind
optimize_constant_0_flops {true | false}	root
optimize_constant_1_flops {true | false}	root
optimize_constant_latches {true | false}	root
optimize_yield {true | false}	root
order *integer*	port_bus subport_bus
outgoing_timing_arcs *string*	libpin
output {true | false}	libpin
pad {true | false}	libcell
param_association *string*	hdl_bind
parse_control_command *string*	root

Attribute Listing with Syntax	Object Type
path *string*	root
paths *string*	exception
period *integer*	clock test_clock test_signal
permutable_group *group_name*	hdl_pin
pin *string*	test_signal
pin_association *string*	hdl_bind
pin_capacitance {*float* | no_value}	pin port subport
pin_capacitance *float*	constant
platform_wordsize *integer*	root
port_delay {*rise fall*}	port
power_gating_cell {true | false}	libcell
power_gating_cell_type *string*	libcell
power_gating_pin_class *string*	libpin
power_gating_pin_phase {active_low | active_high | none}	libpin
power_library *domain*	library_domain
power_rails *Tcl_list*	library
pre_elab_script {*UNIX_path*}	hdl_impl
precluded_path_adjusts *string*	exception
preferred_comp {*component_name*}	hdl_label
preferred_impl {*implementation_name*}	hdl_label
preferred_impl *implementation_name* [*hdl_inst_pathname*]	hdl_inst
preserve {true | false | delete_ok | map_size_ok | size_ok | size_delete_ok}	design instance subdesign
preserve {true | false | delete_ok}	net pin

Attribute Listing with Syntax	Object Type
preserve {true | false}	libcell
preserve_techelts {false | delete_ok | size_delete_ok }	hdl_impl
primitive_function *string*	instance
print_count *integer*	message
priority *integer*	exception hdl_bind hdl_impl message
process *string*	operating_condition
program_name *string*	root
program_short_name *string*	root
program_version *string*	root
propagated_clocks *pin_name*	pin
propagated_clocks *port_name*	port
propagated_clocks_by_mode {{*mode_name_1* [*clock_info_1*]...} [{*mode_name_2* [*clock_info_2*]...}]...}	pin port
propagated_ideal_network {true | false }	pin
prune_unused_logic {true | false}	pin
real_enabled {true | false}	libarc
reg_count *integer*	actual_scan_chain actual_scan_segment scan_segment violation
registers *instance_list*	violation
resistance_per_unit_len {*float*}	root
retime {true | false}	design subdesign
retime_hard_region { true | false }	subdesign
retime_original_registers *register_name*	instance
retime_reg_naming_suffix { string }	root

Attribute Listing with Syntax	Object Type
return_port *string*	hdl_subp
rf_slack *rise fall*	pin port
rise *integer*	clock test_clock test_signal
root_node {*pin* | *port* | *bus*}	violation
root_source_pins *list*	test_clock
root_source_polarity {inverting | non_inverting}	test_clock
runtime *float*	root
scale_of_cap_per_unit_len {*float*}	root
scale_of_res_per_unit_len {*float*}	root
scan_clock_a *string*	actual_scan_chain actual_scan_segment scan_chain scan_segment
scan_clock_b *string*	actual_scan_chain actual_scan_segment scan_chain scan_segment
scan_enable *string*	libcell
scan_enable_phase {active_high | active_low | none}	libpin
scan_in *string*	actual_scan_chain actual_scan_segment libcell scan_chain scan_segment
scan_in_phase {active_high | active_low | none}	libpin
scan_out *string*	actual_scan_chain actual_scan_segment scan_chain scan_segment
scan_shift {true | false}	test_signal

Attribute Listing with Syntax	Object Type
script_begin *string*	root
script_end *string*	root
script_search_path *string*	root
segments *list*	violation
selected_impl {impl_directory bind_name}	subdesign
sequential {true | false}	instance libcell
severity {Info | Error | Warning}	message
shared_output {true | false}	actual_scan_chain scan_chain
shared_select *string*	actual_scan_chain
	scan_chain
shift_capture {*integer* | no_value}	exception
shift_enable *string*	actual_scan_chain actual_scan_segment scan_chain scan_segment
shift_launch {*integer* | no_value}	exception
signal_level *string*	libpin
signed {true | false}	hdl_oper
site_size *microns*	root
skew_safe {true | false}	actual_scan_segment scan_segment
slack {*float* | no_value}	cost_group design instance pin port
slack_by_mode {{*mode_name_1 delay_value*} [{*mode_name_2 delay_value*}]...}	cost_group design pin port

Attribute Listing with Syntax	Object Type
slew {min_rise min_fall max_rise max_fall}	clock
slew {*rise fall*}	pin port
source_verbose {true | false}	root
sources *string*	test_clock
speed_grade {very_slow | slow | medium| fast | very_fast}	subdesign
startpoint {true | false}	pin port
state *string*	design
stdout_log *log_file_name*	root
sub_arch *string*	subdesign
subdesign *string*	instance
super_thread_servers {*machine_names*}	root
sync_clear *string*	libcell
sync_clear_phase {active_high | active_low | none}	libpin
sync_enable *string*	libcell
sync_enable_phase {active_high | active_low | none}	libpin
sync_preset *string*	libcell
sync_preset_phase {active_high | active_low | none}	libpin
synthesis_off_command *string*	root
synthesis_on_command *string*	root
tail *string*	scan_chain
tail_clock *string*	actual_scan_segment scan_segment
tail_clock_edge {fall | rise}	scan_segment actual_scan_segment
technology *library_name*	hdl_impl
temperature *string*	operating_condition
terminal_lockup {none | level_sensitive | edge_sensitive}	scan_chain

Attribute Listing with Syntax	Object Type
terminal_lockup *string*	actual_scan_chain
test_modes *string*	scan_segment
through_points *string*	exception
time_recovery_arcs {true | false}	root
time_scale_in_ps *integer*	library
timing_arcs *string*	pin
timing_case_computed_value {0 | 1 | no_value}	pin port
timing_case_computed_value_by_mode {{*mode* [0 | 1]} [{*mode* [0 | 1]}]...}	port pin
timing_case_disabled_arcs *string*	instance
timing_case_disabled_arcs_by_mode {*mode_name_1* {*libarc_a libarc_b*...}} [*mode_name_2* {*libarc_c libarc_d...*}]...}	instance
timing_case_logic_value {0 | 1 | no_value}	pin port
timing_case_logic_value_by_mode **{***mode_name_1 case_analyis_value***}** [**{***mode_name_2 case_analysis_value***}**]...	pin port
timing_driven_muxopto {true | false}	design subdesign
timing_model {true | false}	instance libcell
tns *string*	cost_group design
to_library_domain *string*	level_shifter_group
to_points *string*	exception
trace_retime {true | false}	instance
tree_type *string*	operating_condition
tristate {true | false}	instance libcell libpin

Attribute Listing with Syntax	Object Type
type { borrow_arc | clear_arc | clock_edge_arc | combo_arc | hold_arc | preset_arc | recovery_arc | removal_arc | setup_arc | tristate_disable_arc | tristate_enable_arc }	libarc
type {abstract | fixed | floating | preserve | shift_register}	actual_scan_segment scan_segment
type {async | clock}	violation
type {scan_clock_a| scan_clock_b| shift_enable | test_mode}	test_signal
type *string*	message
ui_respects_preserve {true | false}	root
unbound_oper_pin *unbound_setting*	hdl_bind
ungroup {true | false}	hdl_arch hdl_comp hdl_comp_arch hdl_impl hdl_inst
ungroup_separator *string*	root
unique_versions *string*	constant instance net pin port subport
uniquify_naming_style *string*	root
unmap_scan_flops {false | not_mapped_for_dft | true}	root
unresolved {true | false}	instance
usable {true | false}	libcell
usable_comb_cells *integer*	library
usable_seq_cells *integer*	library
usable_timing_models *integer*	library
use_scan_seqs_for_non_dft {true|false}	root

Attribute Listing with Syntax	Object Type
user_defined *string*	design instance libcell libpin net pin port subdesign subport
user_defined_signal {true|false}	test_clock test_signal
user_priority *integer*	exception
user_speed_grade {very_slow | slow | medium | fast | very_fast}	subdesign
user_sub_arch {booth | non-booth}	subdesign
version *string*	library
voltage *string*	operating_condition
weight *integer*	cost_group
wire_capacitance {*float* | no_value}	pin port subport
wire_capacitance *float*	constant
wire_resistance {*float* | no_value}	pin port subport
wireload *string*	design
wireload *string*	subdesign
wireload_mode {default | physical | top | enclosed| segmented}	root
wireload_model *string*	pin
wireload_selection {*table* | none | default}	library_domain root
wlec_cut_point *string*	root
wlec_env_var *string*	root

Attribute Listing with Syntax	Object Type
wlec_flat_r2n {true | false}	root
wlec_lib_statetable {true | false}	root
wlec_new_hier_comp {true | false}	root
wlec_no_exit {true | false}	root
wlec_save_ssion *string*	root
wlec_sim_lib *string*	root
wlec_sim_plus_lib {true | false}	root
wlec_uniquify {true | false}	root
wlec_use_lec_model {true | false}	root
wlec_verbose {true | false}	root
write_vlog_bit_blast_constants {true | false}	root
write_vlog_bit_blast_mapped_ports {true | false}	root
write_vlog_declare_wires {true | false}	root
write_vlog_empty_module_for_logic_abstract {true | false}	root
write_vlog_line_wrap_limit *integer*	root
write_vlog_no_negative_index {true | false}	root
write_vlog_port_association_style {default | positional | named | }	instance
write_vlog_top_module_first {true | false}	root
write_vlog_unconnected_port_style { none | partial | full }	root
yield *number*	design

4

Functional Groups

This section provides access to information according to the functional groups of the tool.

Multiple Supply Voltage

Commands	
create_library_domain	level_shifter remove
define_level_shifter_group	level_shifter update
level_shifter check	report level_shifter
level_shifter import	write_encounter
level_shifter insert	

Attributes	
design	
library_domain	
hdl_arch	
library_domain	
instance	
library_domain	
level_shifter_group	
from_library_domain	level_shifter_cells
to_library_domain	
library_domain	
active_operating_conditions	is_default
library	operating_conditions
power_library	wireload_selection
subdesign	
library_domain	

Input and Output

Commands	
encrypt	write_dft_abstract_model
read_def	write_do_lec
read_encounter	write_encounter
read_hdl	write_hdl
read_netlist	write_scandef
read_saif	write_script
read_sdc	write_sdc
read_tcf	write_tcf
read_spef	write_template
write_atpg	

Attributes	
design	
arch_filename	checkpoint_netlist_naming_style
checkpoint_dofile_naming_style	entity_filename
hdl_filelist	hdl_user_name
hdl_arch	
ungroup	
hdl_bind	
avoid	constraint
param_association	pin_association
priority	unbound_oper_pin
hdl_comp	
avoid	location
ungroup	
hdl_comp_arch	
avoid	ungroup
hdl_impl	
avoid	legal
location	priority

Attributes	
technology	ungroup
hdl_inst	
ungroup	
hdl_lib	
avoid	is_chipware
hdl_param	
formula	
hdl_pin	
bit_width	permutable_group
hdl_proc	
group	
Instance	
write_vlog_port_association_style	
root	
bit_blasted_port_style	cap_table_file
checkpoint_flow	command_log
delayed_pragma_commands_interpreter	hdl_allow_inout_const_port_connect
hdl_filelist	hdl_language
hdl_search_path	hdl_track_filename_row_col
hdl_vhdl_case	hdl_vhdl_environment
hdl_vhdl_lrm_compliance	hdl_vhdl_preferred_architecture
hdl_vhdl_read_version	ignore_unknown_embedded_commands
input_asynchro_reset_blk_pragma	input_asynchro_reset_pragma
input_case_cover_pragma	input_case_decode_pragma
input_map_to_mux_pragma	
input_pragma_keyword	input_synchro_reset_blk_pragma
input_synchro_reset_pragma	inst_prefix
lef_library	lib_search_path
library	parse_control_command
path	script_begin
script_end	script_search_path
synthesis_off_command	synthesis_on_command
ungroup_separator	wlec_cut_point

Attributes	
wlec_env_var	wlec_flat_r2n
wlec_lib_statetable	wlec_new_hier_comp
wlec_no_exit	wlec_save_ssion
wlec_sim_lib	wlec_sim_plus_lib
wlec_uniquify	wlec_use_lec_model
wlec_verbose	write_vlog_bit_blast_constants
write_vlog_bit_blast_mapped_ports	write_vlog_declare_wires
write_vlog_empty_module_for_logic_abstract	write_vlog_line_wrap_limit
write_vlog_no_negative_index	write_vlog_top_module_first
write_vlog_unconnected_port_style	
subdesign	
arch_filename	entity_filename
hdl_filelist	hdl_user_name

Physical Layout Estimator

Commands
predict_qos

Attributes	
design	
fplan_height	fplan_width
root	
area_per_unit_len	aspect_ratio
capacitance_per_unit_len	interconnect_mode
lib_lef_consistency_check_enable	number_of_routing_layers
resistance_per_unit_len	scale_of_cap_per_unit_len
scale_of_res_per_unit_len	site_size
subdesign	
fplan_height	fplan_width

Design for Manufacturing

Commands	
read_dfm	report_yield

Attributes
design
yield
root
optimize_yield

Constraints

Commands		
create_mode	external_delay	path_disable
define_clock	multi_cycle	path_group
define_cost_group	path_adjust	specify_paths
derive_environment	path_delay	

Attributes	
clock	
clock_hold_uncertainty	clock_network_early_latency
clock_network_late_latency	clock_setup_uncertainty
clock_source_early_latency	clock_source_late_latency
inverted_sources	latch_max_borrow
non_inverted_sources	slew
cost_group	
weight	
design	
force_wireload	ideal_seq_async_pins
ignore_library_drc	ignore_library_max_fanout
latch_borrow	latch_borrow_by_mode
latch_max_borrow	latch_max_borrow_by_mode
max_capacitance	max_fanout
max_transition	
exceptions	
max	user_priority
external_delay	
clock_network_latency_included	clock_source_latency_included
instance	
disabled_arcs	disabled_arcs_by_mode
hard_region	latch_borrow
latch_borrow_by_mode	latch_max_borrow

Attributes	
latch_max_borrow_by_mode	
pin	
break_timing_paths	clock_hold_uncertainty
clock_network_early_latency	clock_network_late_latency
clock_setup_uncertainty	clock_source_early_latency
clock_source_late_latency	ideal_driver
ideal_network	latch_max_borrow
latch_max_borrow_by_mode	preserve
timing_case_logic_value	timing_case_logic_value_by_mode
net	
preserve	
port	
break_timing_paths	clock_hold_uncertainty
clock_network_early_latency	clock_network_late_latency
clock_setup_uncertainty	clock_source_early_latency
clock_source_late_latency	external_driven_pin_fall
external_driven_pin_riseb	external_driver
external_driver_from_pin	external_driver_input_slew
external_fanout_load	external_non_tristate_drivers
external_pin_cap	external_resistance
external_wire_cap	external_wire_res
external_wireload_fanout	external_wireload_model
fixed_slew	ideal_driver
ideal_network	ignore_external_driver_drc
max_capacitance	max_fanout
max_transition	timing_case_logic_value
timing_case_logic_value_by_mode	
root	
case_analysis_sequential_propagation	drc_first
operating_conditions	time_recovery_arcs
wireload_mode	wireload_selection

Attributes	
subdesign	
force_wireload	hard_region

Synthesis

Commands	
elaborate	retime
synthesize	

Attributes	
design	
hdl_parameters	preserve
retime	
hdl_impl	
pre_elab_script	preserve_techelts
hdl_inst	
preferred_impl	
hdl_label	
preferred_comp	preferred_impl
instance	
dont_retime	hdl_proc_name
inherited_preserve	preserve
trace_retime	unresolved
pin	
prune_unused_logic	
root	
bus_naming_style	delete_unloaded_insts
delete_unloaded_seqs	derive_bussed_pins
dp_perform_csa_operations	dp_perform_sharing_operations
dp_perform_speculation_opertions	endpoint_slack_opto
gen_module_prefix	hdl_array_naming_style
hdl_async_set_reset	hdl_auto_async_set_reset
hdl_auto_sync_set_reset	hdl_bit_blast_threshold
hdl_delete_transparent_latches	hdl_enable_proc_name
hdl_error_on_blackbox	hdl_error_on_latch
hdl_ff_keep_feedback	hdl_ff_keep_explicit_feedback

Attributes	
hdl_infer_unresolved_from_logic_abstract	hdl_latch_keep_feedback
hdl_max_loop_limit	hdl_max_recursion_limit
hdl_parameter_naming_style	hdl_preserve_unused_registers
hdl_preserve_dangling_output_nets	hdl_record_naming_style
hdl_reg_naming_style	hdl_sync_set_reset
hdl_trim_target_index	hdl_unconnected_input_port_value
hdl_undriven_output_port_value	hdl_undriven_signal_value
hdl_use_default_parameter_values_in_name	hdl_use_parameterized_module_by_name
hdl_use_port_default_value	hdl_use_techelt_first
hdl_vector_naming_style	merge_seqs_into_multibit_cells
multibit_seqs_from_different_banks	multibit_seqs_members_naming_style
optimize_constant_0_flops	optimize_constant_1_flops
optimize_constant_latches	retime_reg_naming_suffix
timing_driven_muxopto	uniquify_naming_style
use_scan_seqs_for_non_dft	
subdesign	
allow_csa_subdesign	allow_sharing_subdesign
allow_speculation_subdesign	boundary_opto
delete_unloaded_seqs	hdl_parameters
preserve	retime
retime_hard_region	user_speed_grade
user_sub_arch	

Analysis

Commands		
clock_ports	report dft_setup	report operand_isolation
fanin	report dft_violations	report port
fanout	report gates	report power
report area	report hierarchy	report qor
report clock_gating	report instance	report scan_power
report clocks	report level_shifter	report sequential
report datapath	report memory	report summary
report design_rules	report messages	report timing
report dft_chains	report nets	report yield
report dft_registers	report operand_isolation	

Attributes	
clock	
divide_fall	divide_period
divide_rise	exceptions
fall	period
rise	
cost_group	
exceptions	slack
slack_by_mode	tns
design	
area	cell_area
cell_count	max_cap_cost
max_fanout_cost	max_trans_cost
net_area	slack
slack_by_mode	tns
wireload	
exceptions	
adjust_value	cost_group
delay_value	exception_type

Attributes	
from_points	lenient
paths	precluded_path_adjusts
priority	shift_capture
shift_launch	through_points
to_points	
external_delay	
clock	clock_rise
delay	exceptions
external_delay_pins	input_delay
level_sensitive	
hdl_arch	
location	
hdl_bind	
operator	
hdl_comp_arch	
location	
hdl_impl	
language	
hdl_inst	
component	
hdl_oper	
signed	
hdl_pack	
default_location	location
hdl_pin	
direction	
hdl_subp	
map_to_module	map_to_operator
return_port	
instance	
buffer	cell_area
exceptions	file_row_col
flop	hierarchical

Attributes	
inverter	latch
libcell	primitive_function
retime_original_registers	sequential
slack	subdesign
timing_case_disabled_arcs	timing_case_disabled_arcs_by_mode
timing_model	tristate
unique_versions	
constant	
net	pin_capacitance
unique_versions	wire_capacitance
net	
drivers	ideal
loads	logic0_driven
logic1_driven	num_drivers
num_loads	unique_versions
pin	
capturer	causes_ideal_net
clock_sources_inverted	clock_sources_non_inverted
connect_delay	direction
endpoint	exceptions
external_delays	external_delays_by_mode
inverting_clocks	launcher
libpin	net
non_inverting_clocks	pin_capacitance
propagated_clocks	propagated_clocks_by_mode
propagated_ideal_network	rf_slack
slack	slack_by_mode
slew	startpoint
timing_arcs	timing_case_computed_value
timing_case_computed_value_by_mode	unique_versions

Attributes	
wire_capacitance	wire_resistance
wireload_model	
pin_bus	
bits	
port	
bus	causes_ideal_net
clock_sources_inverted	clock_sources_non_inverted
connect_delay	direction
endpoint	exceptions
external_delays	external_delays_by_mode
net	pin_capacitance
port_delay	propagated_clocks
propagated_clocks_by_mode	rf_slack
slack	slack_by_mode
slew	startpoint
timing_case_computed_value	timing_case_computed_value_by_mode
unique_versions	wire_capacitance
wire_resistance	
port_bus	
bits	direction
order	
root	
active_operating_conditions	
subdesign	
candidate_impls	cell_area
cell_count	instances
logical_hier	selected_impl
speed_grade	sub_arch
wireload	
subport	
bus	causes_ideal_net
direction	net
pin_capacitance	unique_versions

Attributes	
wire_capacitance	wire_resistance
subport_bus	
bits	direction
order	

Datapath Analysis

Commands
report datapath

Attributes	
root	
checkpoint_directory	dp_postmap_upsize
dp_area_mode	dp_perform_shannon_operations
dp_perform_csa_operations	dp_perform_sharing_operations
dp_postmap_downsize	dp_perform_speculation_operations
subdesign	
allow_csa_subdesign	allow_sharing_subdesign
allow_speculation_subdesign	speed_grade
user_speed_grade	

Design for Test

***Constraint*/Command**	
analyze_testability	insert_dft shadow_logic
check_dft_rules	insert_dft test_point
configure_pad_dft	insert_dft user_test_point
connect_scan_chains	insert_dft wrapper_cell
define_dft abstract_segment	read_dft_abstract_model
define_dft fixed_segment	replace_scan
define_dft floating_segment	report dft_chains
define_dft preserved_segment	report dft_registers
define_dft scan chain	report dft_setup
define_dft scan_clock_a	report dft_violations
define_dft scan_clock_b	report scan_power
define_dft shift_enable	reset_scan_equivalent
define_dft shift_register_segment	set_compatible_test_clocks
define_dft test_clock	set_scan_equivalent
define_dft test_mode	write_atpg
fix_dft_violations	write_dft_abstract_model
insert_dft analyzed_test_points	write_scandef
insert_dft lockup_element	

Attributes	
actual_scan_chain	
analyzed	connected_shift_enable
domain	edge
elements	reg_count
scan_clock_a	scan_clock_b
scan_in	scan_out
shared_output	shared_select
shift_enable	terminal_lockup

Attributes	
actual_scan_segment	
active	clock
clock_edge	connected_scan_clock_a
connected_scan_clock_b	connected_shift_enable
core_wrapper	dft_tail_test_clock
dft_tail_test_clock_edge	dft_test_clock
dft_test_clock_edge	elements
instance	reg_count
scan_clock_a	scan_clock_b
scan_in	scan_out
shift_enable	skew_safe
tail_clock	tail_clock_edge
type	
design	
dft_connect_scan_data_pins_during_mapping	dft_connect_shift_enable_during_mapping
dft_dont_scan	dft_lockup_element_type
dft_max_length_of_scan_chains	dft_min_number_of_scan_chains
dft_mix_clock_edges_in_scan_chains	dft_scan_map_mode
dft_scan_output_preference	
instance	
dft_abstract_dont_scan	dft_dont_scan
dft_inherited_dont_scan	dft_mapped
dft_part_of_segment	dft_status
dft_test_clock	dft_test_clock_edge
dft_test_clock_source	dft_violation
pin	
dft_controllable	
root	
dft_identify_internal_test_clocks	dft_prefix
dft_report_empty_test_clocks	dft_scan_style
unmap_scan_flops	

Attributes	
scan_chain	
body	complete
dft_hookup_pin_sdi	dft_hookup_pin_sdo
domain	edge
head	max_length
scan_clock_a	scan_clock_b
scan_in	scan_out
shared_output	shared_select
shift_enable	tail
terminal_lockup	
scan_segment	
active	clock
clock_edge	connected_scan_clock_a
connected_scan_clock_b	connected_shift_enable
core_wrapper	dft_status
dft_tail_test_clock	dft_tail_test_clock_edge
dft_test_clock	dft_test_clock_edge
dft_violation	elements
instance	reg_count
scan_clock_a	scan_clock_b
scan_in	scan_out
shift_enable	skew_safe
tail_clock	tail_clock_edge
test_modes	type
subdesign	
dft_dont_scan	
test_clock	
controllable	dft_hookup_pin
dft_hookup_polarity	divide_fall
divide_period	divide_rise
fall	off_state
period	rise

Attributes	
root_source_pins	root_source_polarity
sources	user_defined_signal
test_signal	
active	dedicated_pin
default_shift_enable	dft_hookup_pin
dft_hookup_polarity	divide_fall
divide_period	divide_rise
fall	ideal
period	pin
rise	scan_shift
type	user_defined_signal
violations	
description	endpoints
file_name	fixed
id	line_number
reg_count	registers
root_node	segments
type	

Low Power Synthesis

Commands	
clock_gating connect_test	read_tcf
clock_gating declone	report clock_gating
clock_gating import	report operand_isolation
clock_gating insert_in_netlist	report power
clock_gating insert_obs	report gates -power
clock_gating join	state_retention define_driver
clock_gating remove	state_retention define_map
clock_gating share	state_retention swap
clock_gating split	write_forward_saif
read_saif	write_tcf

Attributes	
design	
lp_clock_gating_add_obs_port	lp_clock_gating_add_reset
lp_clock_gating_cell	lp_clock_gating_control_point
lp_clock_gating_exclude	lp_clock_gating_max_flops
lp_clock_gating_min_flops	lp_clock_gating_module
lp_clock_gating_style	lp_clock_gating_test_signal
lp_default_probability	lp_default_toggle_rate
lp_internal_power	lp_leakage_power
lp_map_to_srpg_cells	lp_net_power
lp_optimize_dynamic_power_first	lp_power_optimization_weight
lp_srpg_pg_driver	max_dynamic_power
max_leakage_power	
instance	
lp_clock_gating_exclude	lp_default_probability
lp_default_toggle_rate	lp_internal_power
lp_leakage_power	lp_map_to_srpg_cells
lp_map_to_srpg_type	lp_net_power

Attributes	
lp_srpg_pg_driver	
libcell	
cell_leakage_power	power_gating_cell
power_gating_cell_type	
libpin	
power_gating_pin_class	power_gating_pin_phase
library	
leakage_power_scale_in_nW	
net	
lp_asserted_probability	lp_asserted_toggle_rate
lp_computed_probability	lp_computed_toggle_rate
lp_net_power	lp_probability_type
lp_toggle_rate_type	
pin	
lp_asserted_probability	lp_asserted_toggle_rate
lp_computed_probability	lp_computed_toggle_rate
lp_net_power	lp_probability_type
lp_toggle_rate_type	
port	
lp_asserted_probability	lp_asserted_toggle_rate
lp_computed_probability	lp_computed_toggle_rate
lp_net_power	lp_probability_type
lp_toggle_rate_type	
root	
lp_clock_gating_prefix	lp_insert_clock_gating
lp_insert_operand_isolation	lp_multi_vt_optimization_effort
lp_operand_isolation_prefix	lp_power_analysis_effort
lp_power_unit	lp_toggle_rate_unit
subdesign	
lp_clock_gating_exclude	
subport	
lp_asserted_probability	lp_asserted_toggle_rate
lp_computed_probability	lp_computed_toggle_rate

Attributes	
lp_net_power	lp_probability_type
lp_toggle_rate_type	