Tutorial on FPGA Design Flow based on Aldec Active-HDL

ver 2.0

Updated: Fall 2013

Preparing the Input:

Download examples associated with this tutorial posted at

http://ece.gmu.edu/tutorials-and-lab-manuals

as **design_flow_examples.zip**

VHDL Source Files: Unzip the file "design_flow_examples.zip" and make sure that you obtain the folder **lab3_demo** with the following files:

RTL VHDL code:
clock_divider.vhd
counter.vhd
SSegCtrl.vhd
lab3_demo_package.vhd
lab3_demo.vhd

Testbench:
lab3_demo_tb.vhd

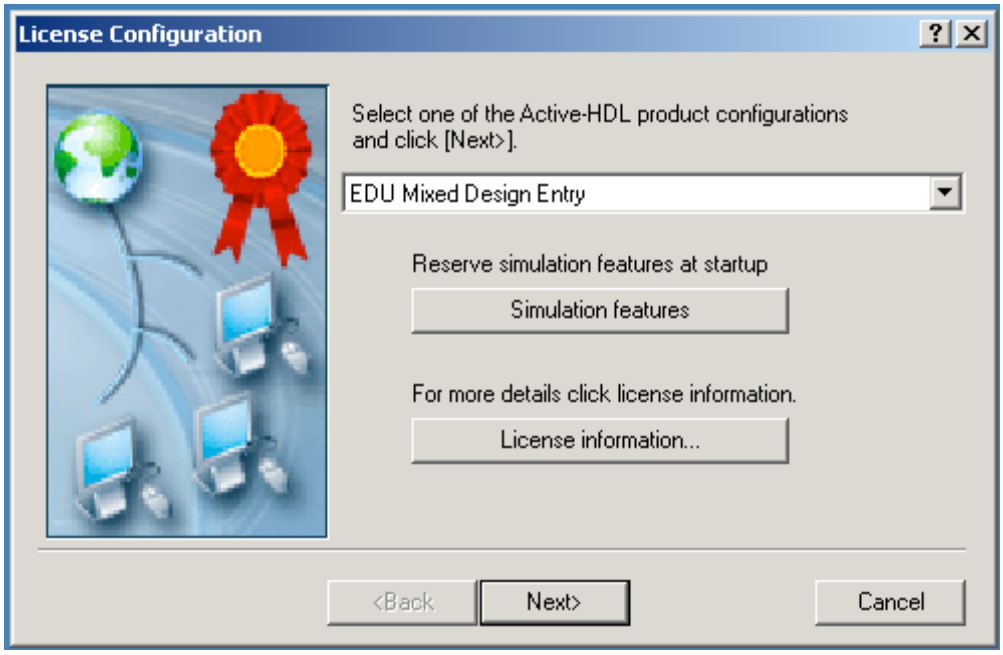
User Constraints File:
lab3_demo_basys2.ucf
lab3_demo_nexys3.ucf

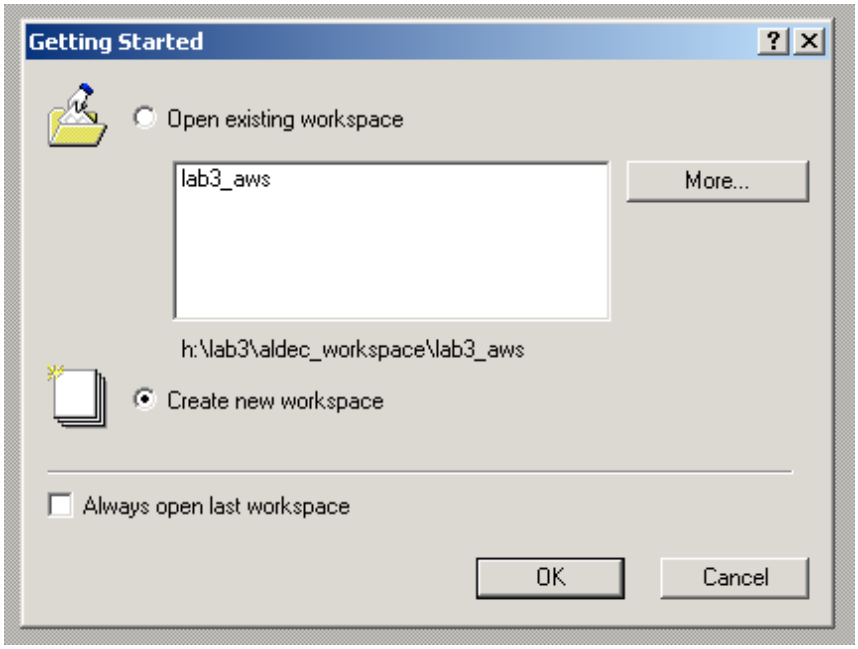
Current Version of Tools: This tutorial has been tested using the following versions of **CAD Tools**

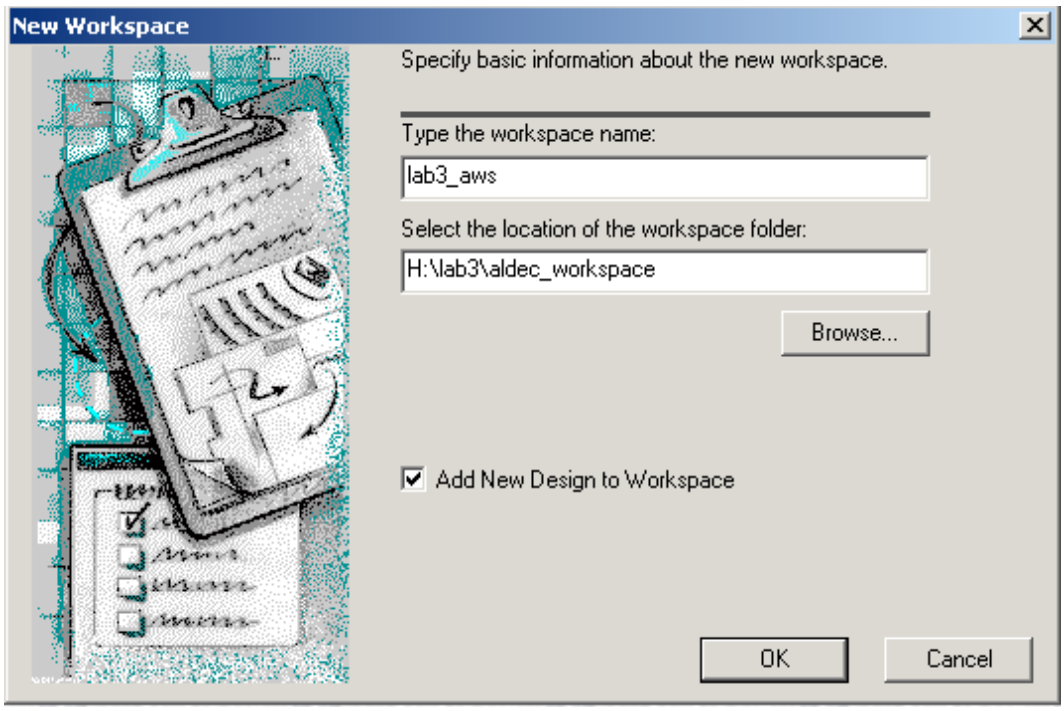
1. **Simulator** (Active-HDL versions: 7.2, 8.2, 8.3, 9.1and 9.2)
2. **Synthesis Tools** (Xilinx ISE Webpack XST ver. 13.2, 14.2, 14.6 and Synplify Premier DP ver. D-2010-03)
3. **Implementation Tools** (Xilinx ISE/WebPack ver. 13.2, 14.2, 14.6)
4. **FPGA Board** (Digilent Basys2, Digilent Nexys3)

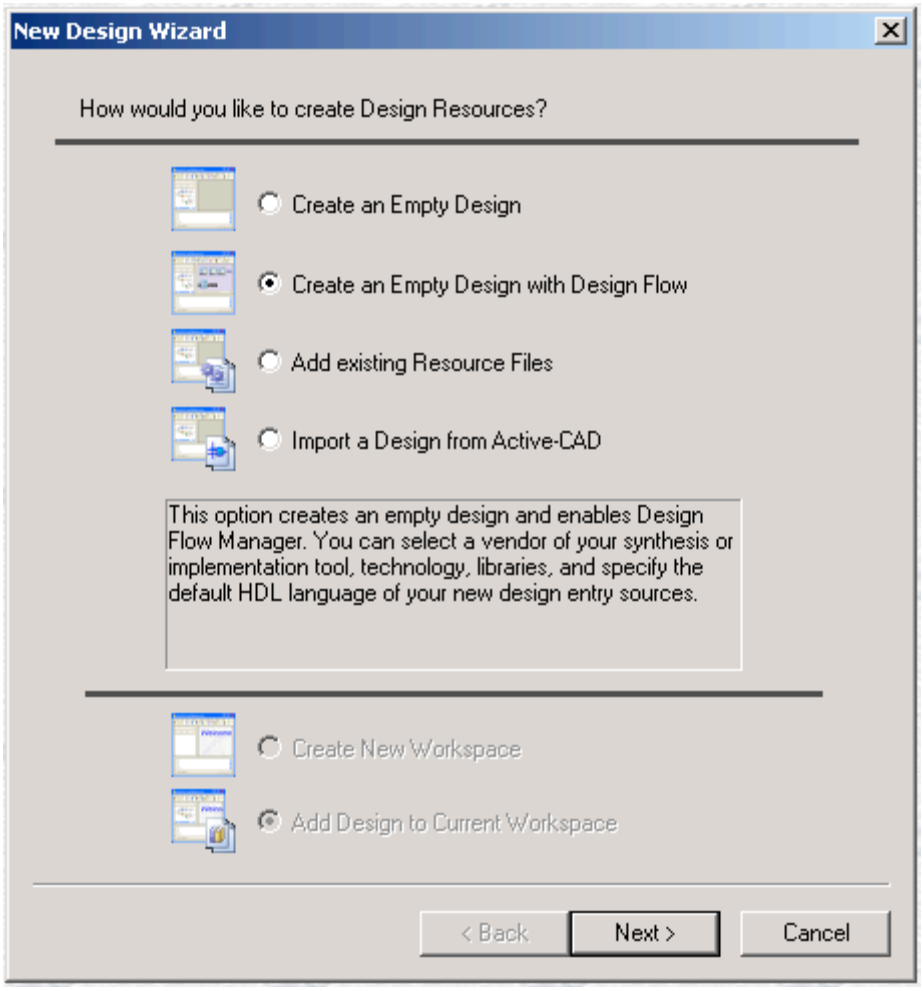
Table of Contents

1. Project Settings



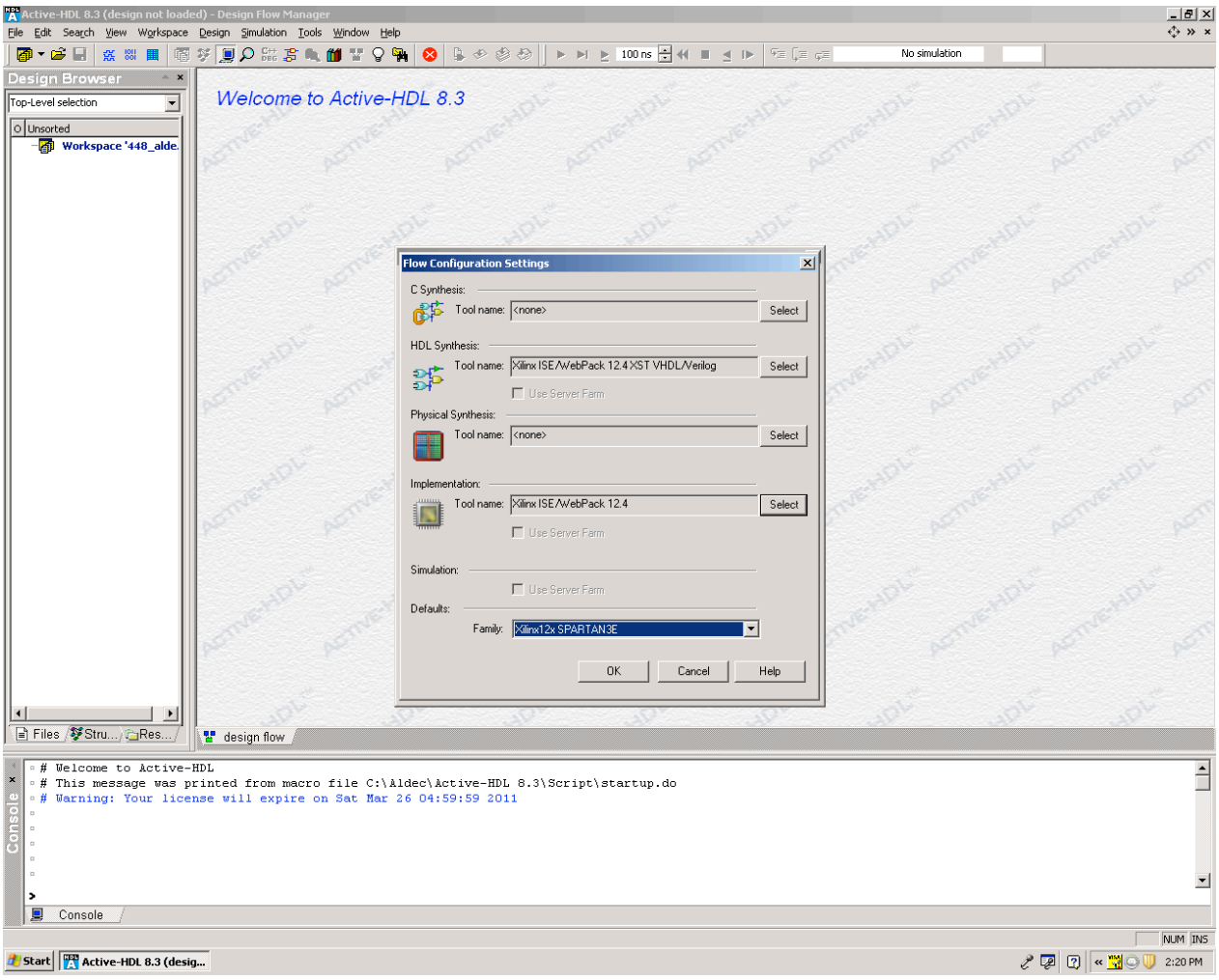



New Workspace
Specify basic information about the new workspace.
Type the workspace name:
lab3_aws
Select the location of the workspace folder:
H:\lab3\aldec_workspace
Browse...
Add New Design to Workspace
OK
Cancel



Create new workspace and choose ***Create an Empty Design with Design Flow*.**

Press **Next**. You will see a picture similar to the one shown below.



Verify that **Flow Configuration Settings** are defined as follows: Synthesis Tool:

- ***Xilinx ISE/WebPack <version number> XST***

Implementation Tool:

- ***Xilinx ISE/WebPack <version number>***

Default Family:

- ***Xilinx<version number>x SPARTAN 6***

If not, click at the **Flow Configuration Settings** button and adjust appropriately.

Also choose,

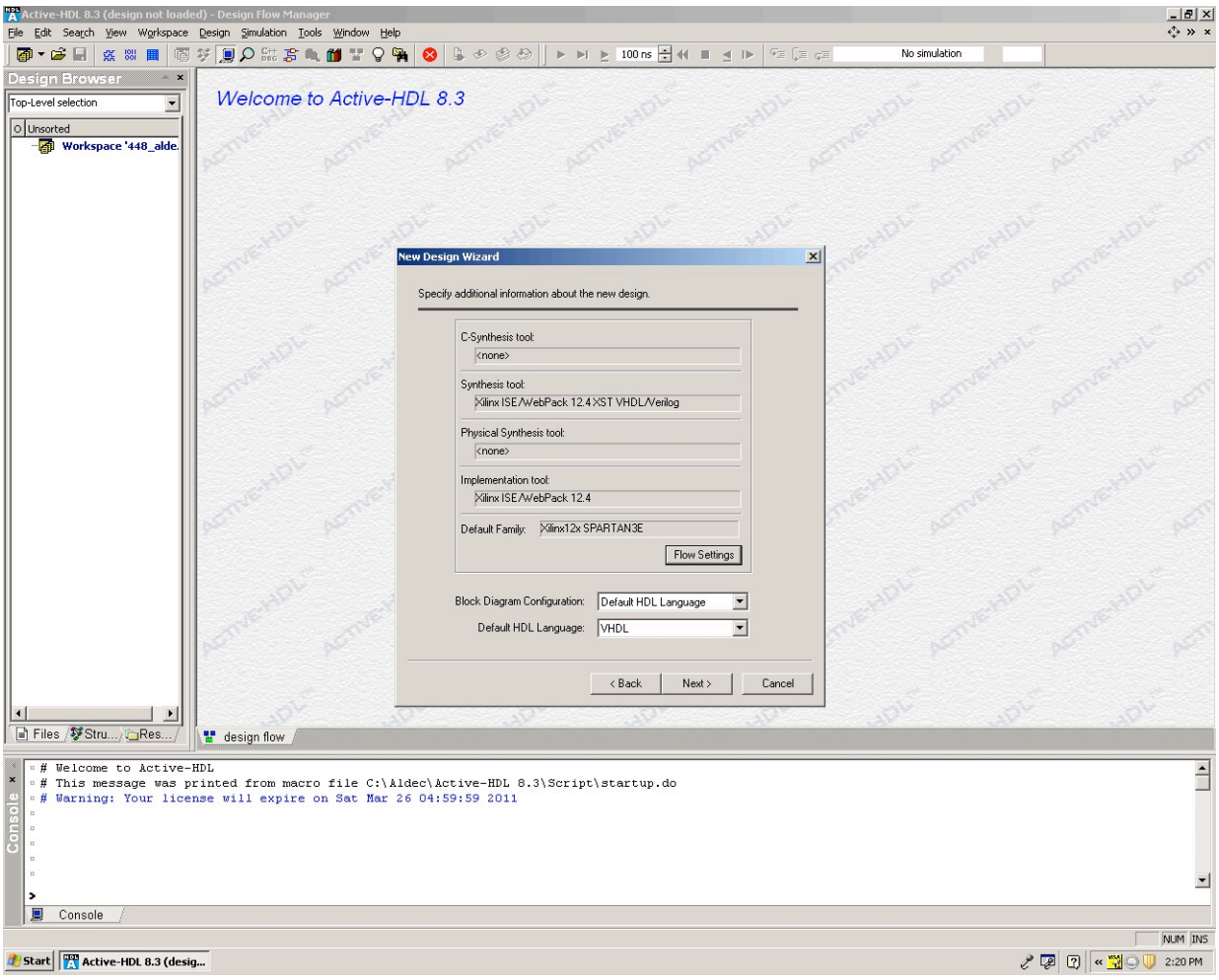
Block Diagram Configuration

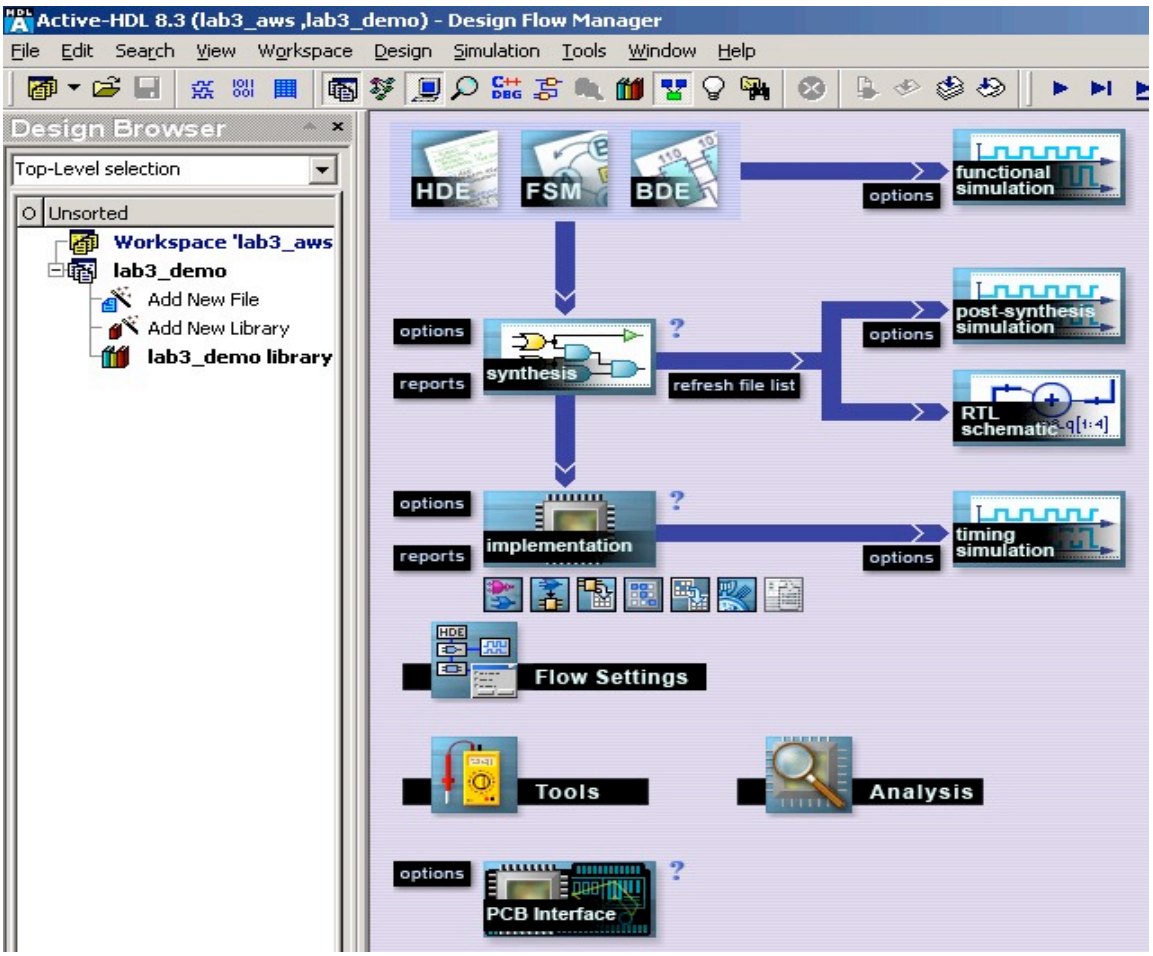
- ***Default HDL Language***

Default HDL Language

- ***VHDL***

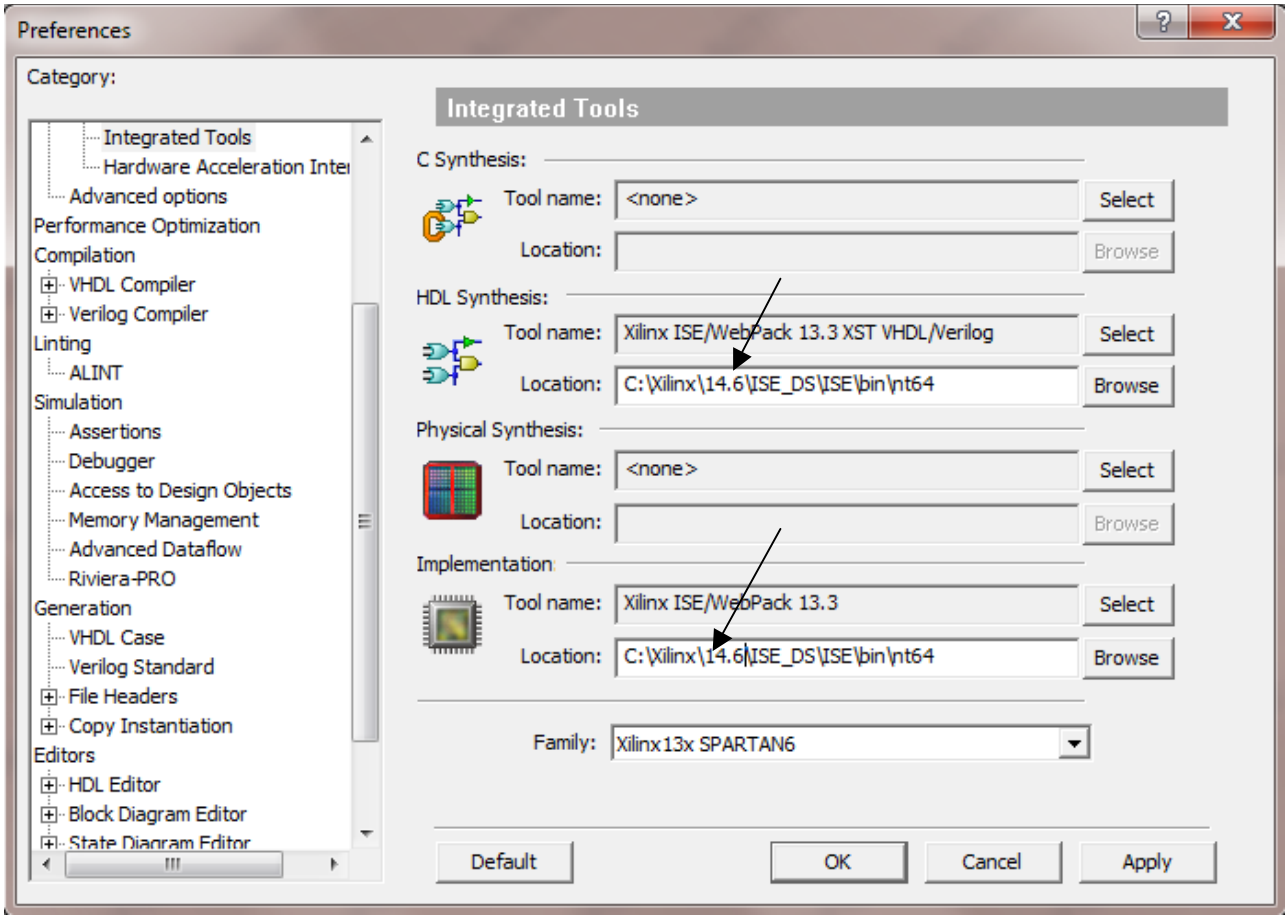
Once done, select **Next** and then **Finish**





Now you should see a screen divided into several parts, with a Flow panel on the right side. If you do not see the Flow panel on the right side as shown in the picture, you can press **Alt+3** or go to View menu and click on **Flow** from the top menu bar to open the panel.

Go to **Tool→Preferences.** In the category expand **Tools→ Flow→ integrated tools.** Browse to the latest synthesis and implementation tools and select them appropriately.



Below example refers to the versions of tools available in the GMU Labs. For home use, you may need to use different versions of tools and program paths.

Synthesis tools:

1. Xilinx XST <version number> (Browse to Xilinx/<version number>/ISE/bin/nt/xst.exe)
2. Synplify Premier DP (Select to Synplify Premier with DP <version number>. Click on "Select" for "Tool name" under the option "HDL Synthesis" and then select the category “synopsys”) (available only in the ECE Labs).

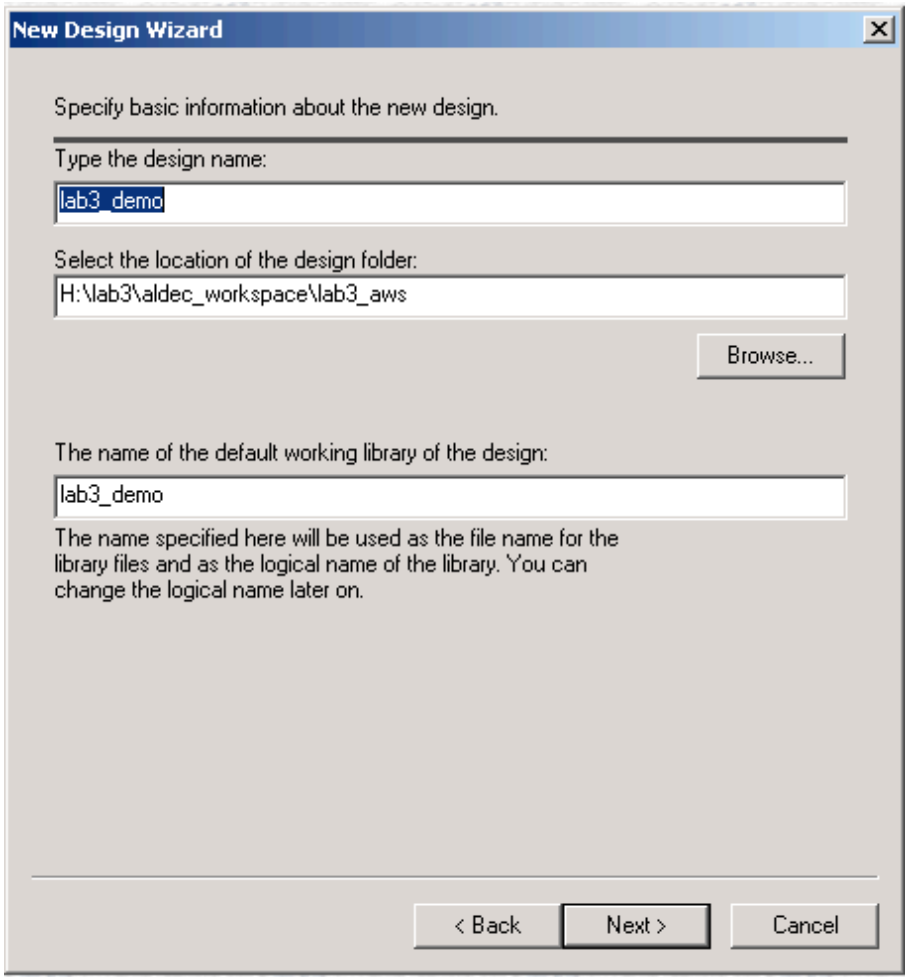
Implementation tool:

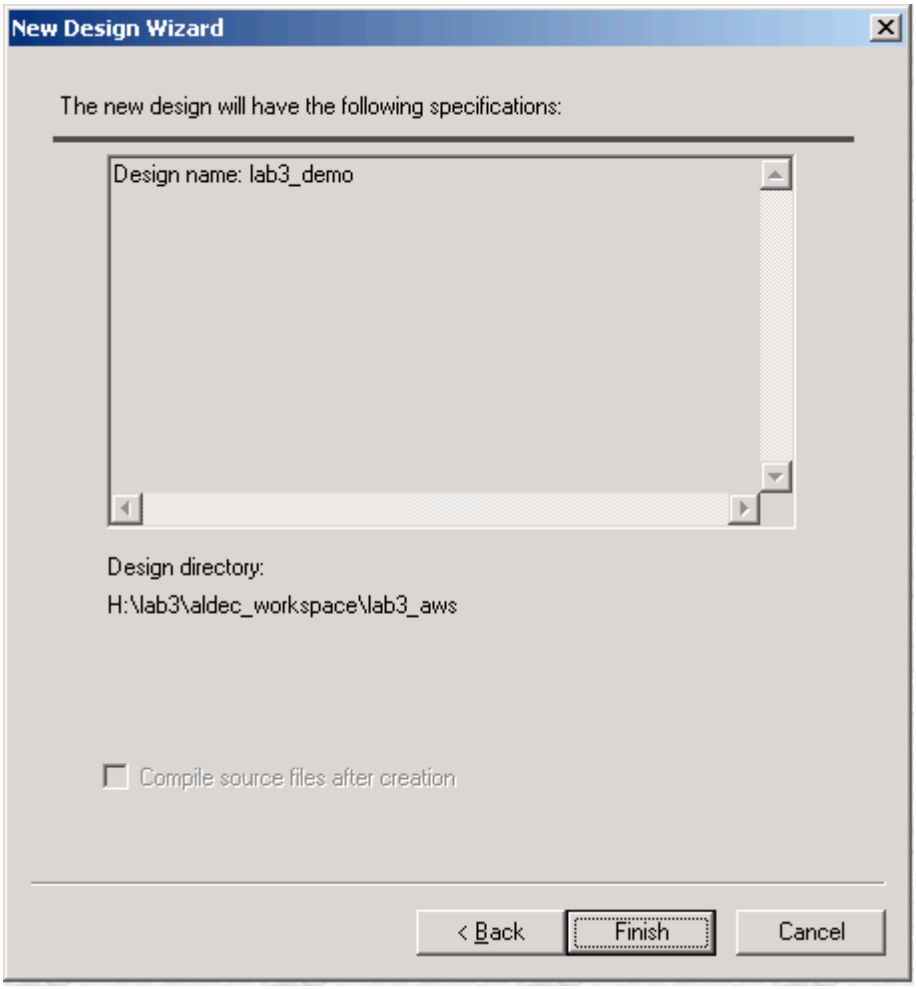
Xilinx ISE/WebPack <version number> (Browse to Xilinx/<version number>/ISE/bin/nt/xst.exe)

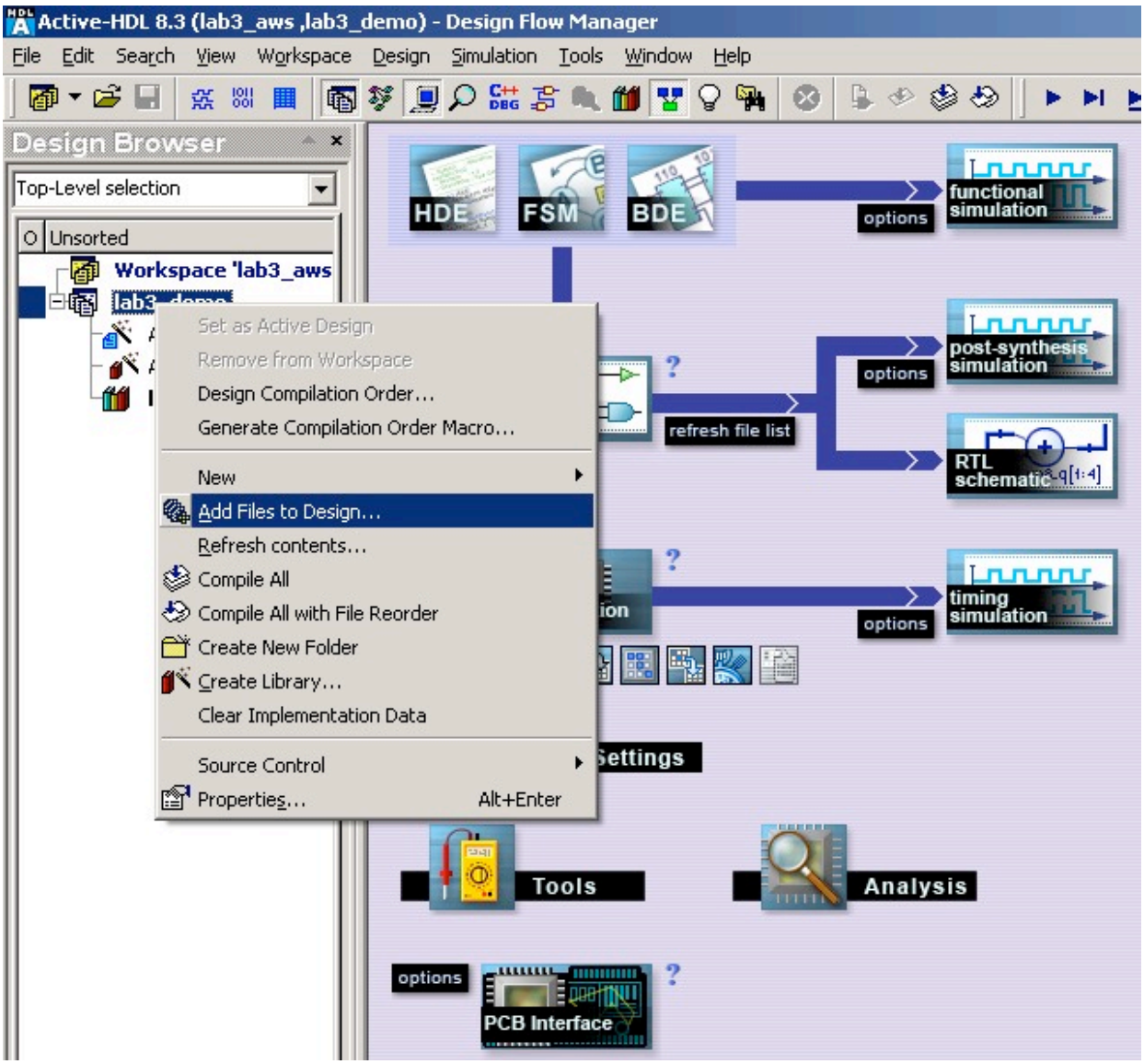
If the tools for HDL synthesis and implementation are already selected then click on **OK**. If not, choose the tools as shown above and the path accordingly. Please note that you will be able to select only one synthesis tool at a time.

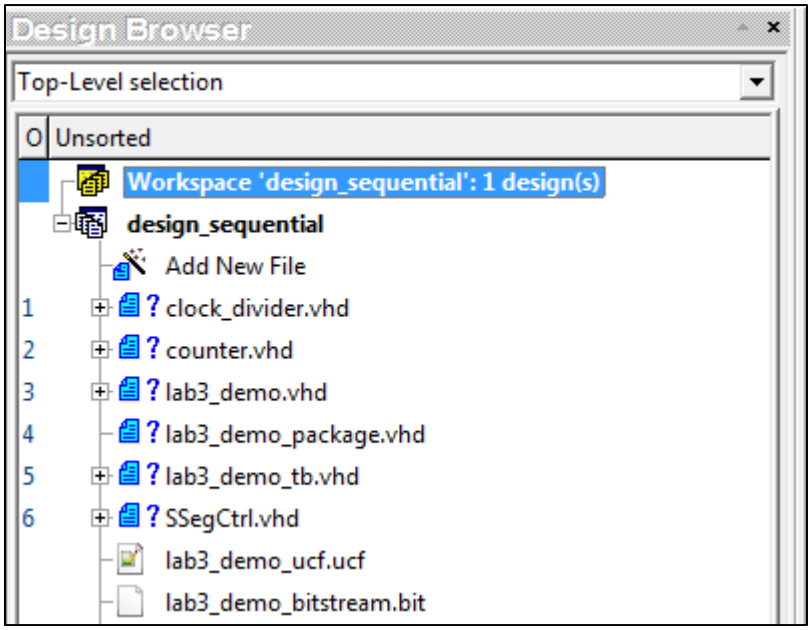
Specify the new design name (e.g., lab3_demo).

Add and compile all files describing your circuit, including a testbench (e.g., all VHDL files from lab3_demo). Then, test your design if it works correctly in the functional simulation as you would normally do. If you are following the tutorial by using lab3_demo, make sure you change the ***slow_clock_period,*** located inside ***lab3_demo_package.vhd,*** to a number suitable for simulation (5). It will take a long time to simulate otherwise.

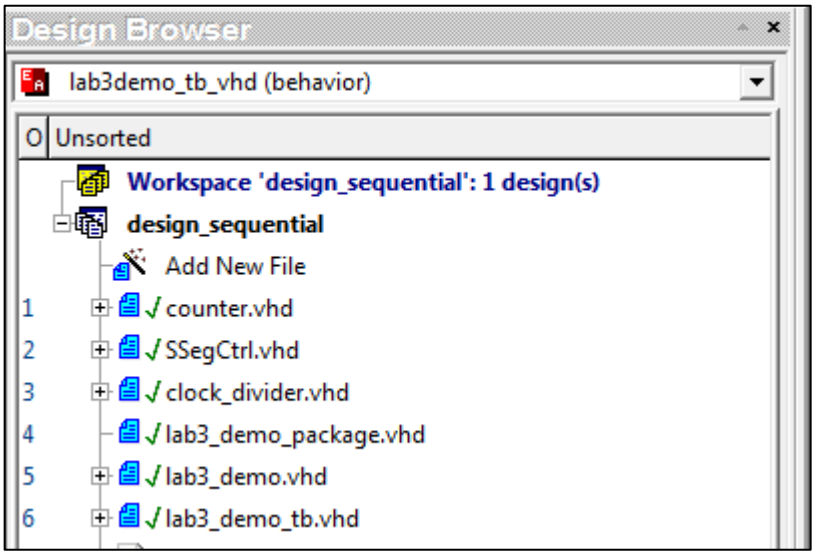



New Design Wizard
The new design will have the following specifications:
Design name: lab3_demo
Design directory:
H:\lab3\aldec_workspace\lab3_aws
Compile source files after creation
< Back
Finish
Cancel


Active-HDL 8.3 (lab3_aws ,lab3_demo) - Design Flow Manager
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
Top-Level selection
Unsorted
Workspace 'lab3_aws
Set as Active Design
Remove from Workspace
Design Compilation Order...
Generate Compilation Order Macro...
New
Add Files to Design...
Refresh contents...
Compile All
Compile All with File Reorder
Create New Folder
Create Library...
Clear Implementation Data
Source Control
Properties... Alt+Enter
HDE
FSM
BDE
options
functional simulation
post-synthesis simulation
refresh file list
RTL schematic
timing simulation
Settings
Tools
Analysis
PCB Interface


Design Browser
Top-Level selection
Unsorted
Workspace 'design_sequential': 1 design(s)
design_sequential
Add New File
1 clock_divider.vhd
2 counter.vhd
3 lab3_demo.vhd
4 lab3_demo_package.vhd
5 lab3_demo_tb.vhd
6 SSegCtrl.vhd
lab3_demo_ucf.ucf
lab3_demo_bitstream.bit

Compile all VHDL files (these files do not include the constraints files with the extension .ucf). Go to Design menu and choose “Compile All” option.

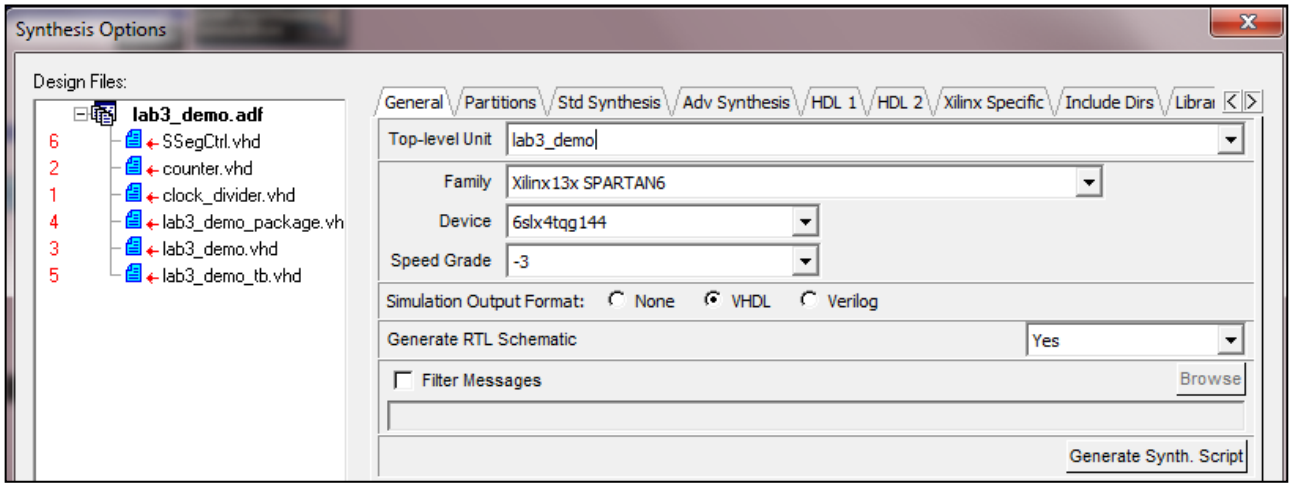


Synthesis

Synthesis can be done either by using Xilinx XST or Synplify Premier DP.
Xilinx XST can be used both at school and at home. Synplify Premier DP is available only at school.

2.1 Synthesis using Xilinx XST

2.1.1 Synthesis Options

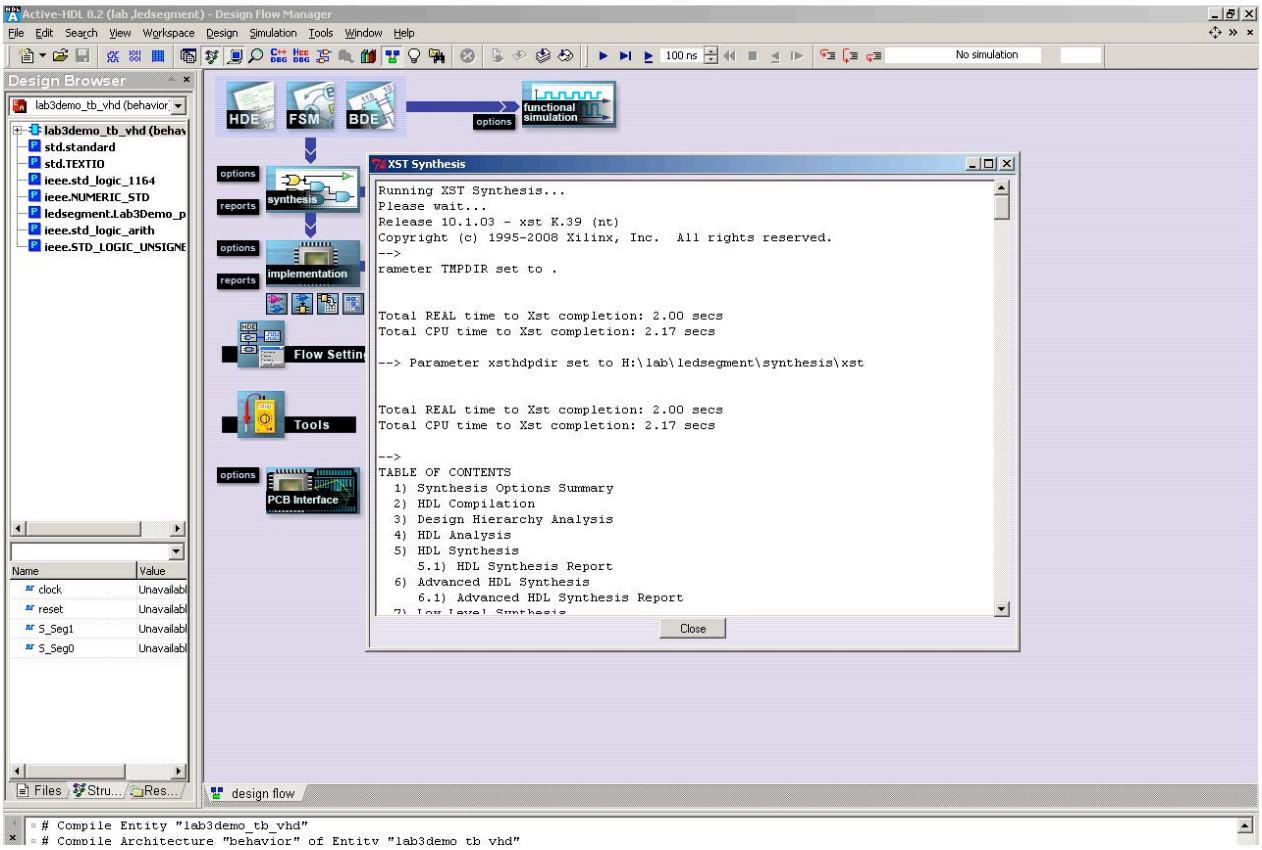


Click at the **options** button next to the **synthesis** icon. Under **Synthesis Options** select ***Update synthesis order***. Arrange your files in the order from the bottom to the top of the design hierarchy. Exclude your non-synthesizable files, such as testbench. Also select a correct **Top-level Unit**, which is lab3_demo in the example you follow.

Make sure that your settings under **General** tab are
as follows:

Family : Xilinx<version_number>x SPARTAN6
Device : XC6SLX16
Speed Grade : -3.

Under **Std Synthesis** and **Adv Synthesis** tabs, you can adjust optimization goal of the synthesis tool for various results. Most notably, you can tell the synthesis tool to optimize for either *area* or *speed*. To select either one of them, click on **Std Synthesis** tab and chose **Optimization Goal** to be either **Speed** or **Area.**
Click on OK when you are done with option settings.



Click on the **synthesis** button and wait until synthesis is completed.

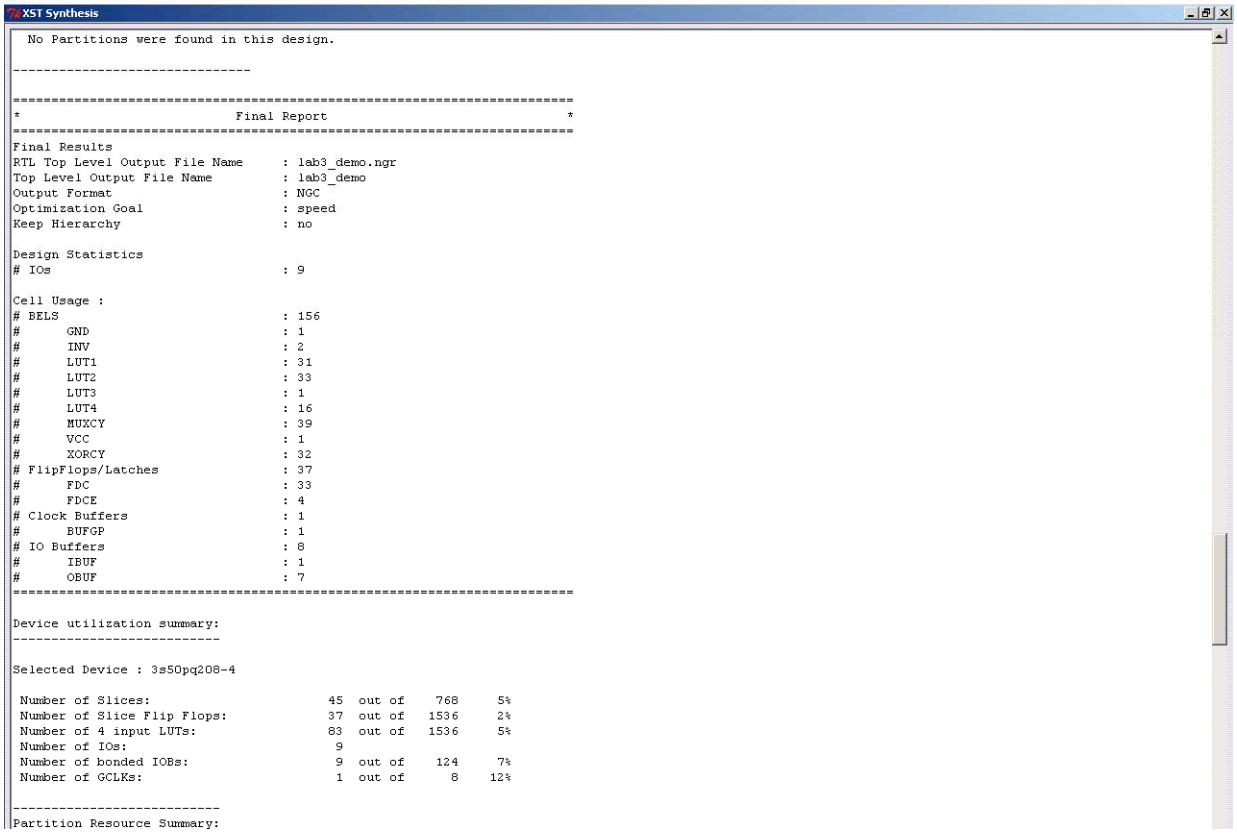
2.1.2 Synthesis Report

Minimum clock period, critical path, and resource utilization can be found from the report file generated after synthesis. To view this file, click on the **reports** button next to the **synthesis** icon.

Minimum clock period, maximum frequency, and critical path can be found under Timing Summary section. Looking at the critical path can give you an idea which portions of your code to change in order to improve the circuit performance.

Resource utilization is located in the Final Report section.

Example Report: Resource Utilization



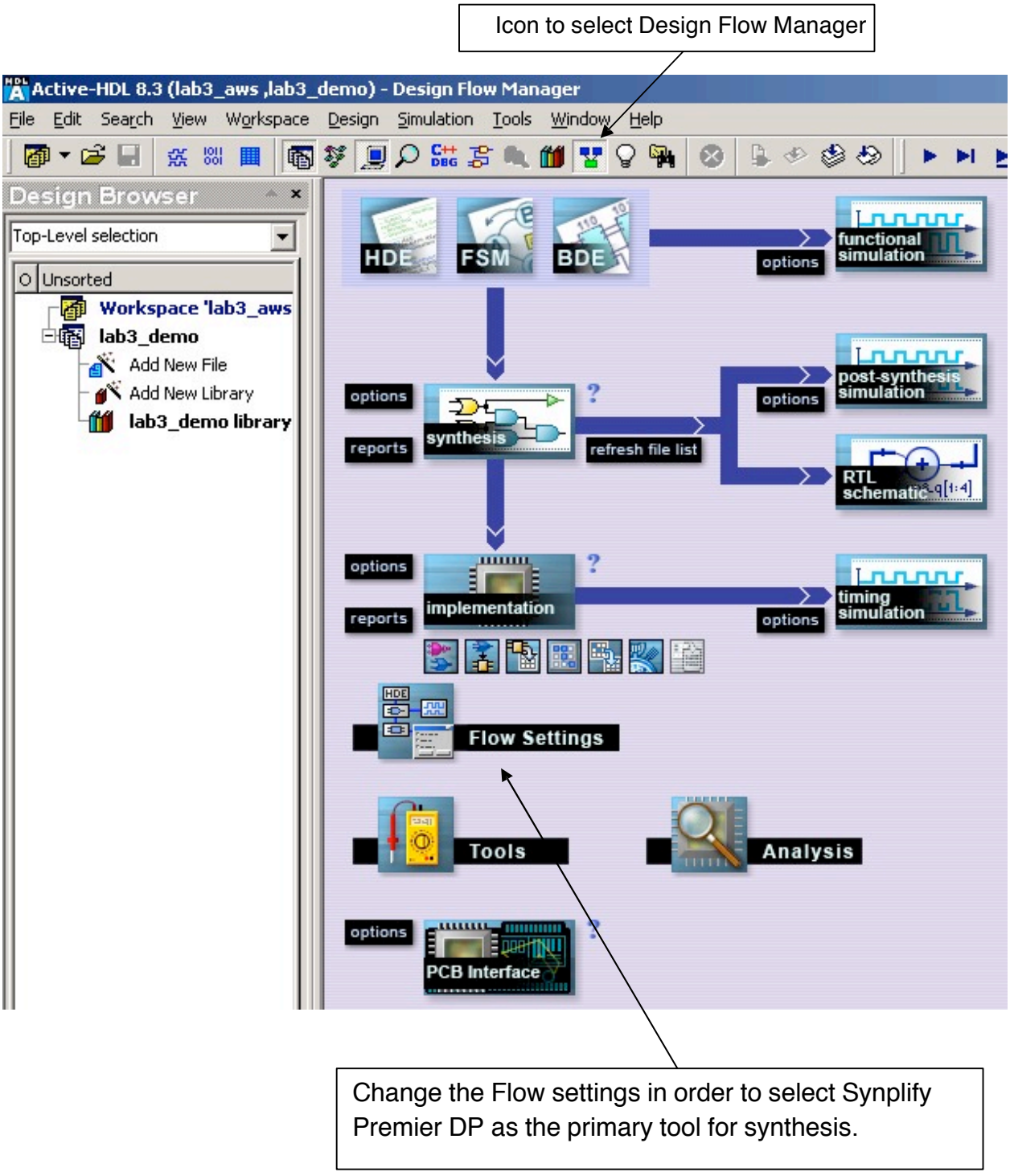
Example Report: Minimum Clock Period and Critical Path

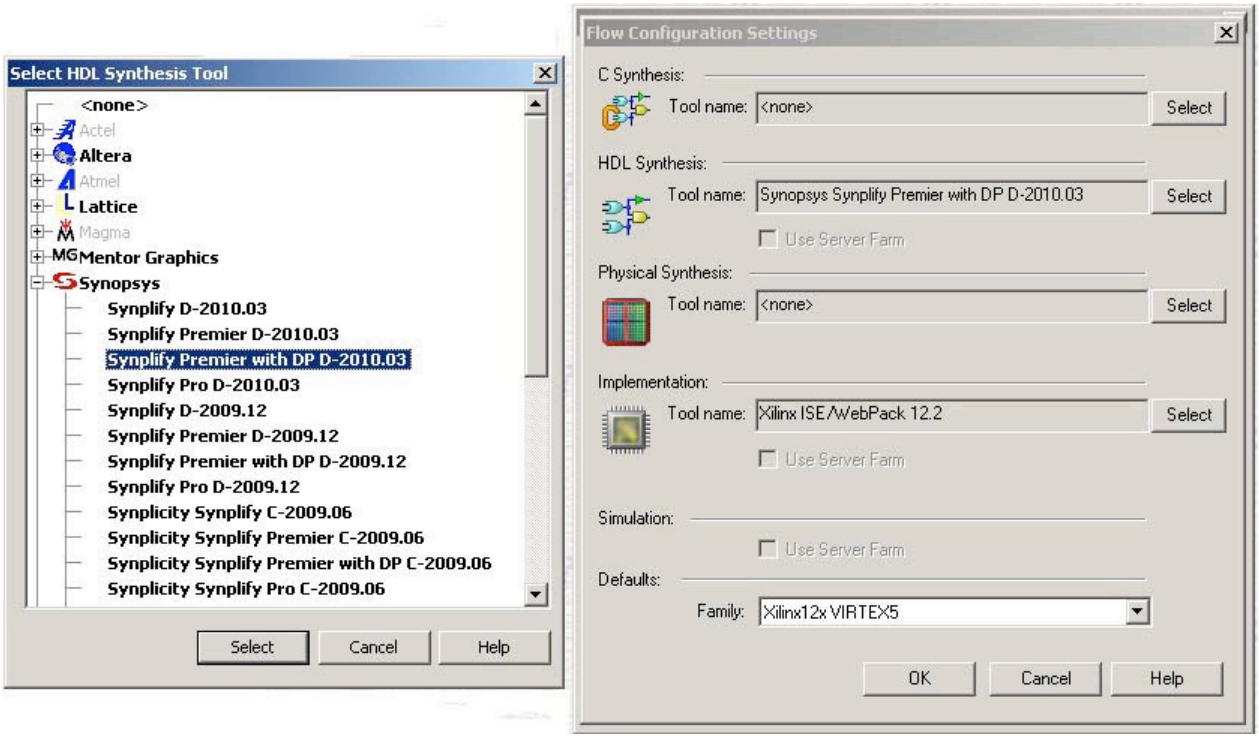
XST Synthesis

```
-----------------------------------+------------------------+-------+

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 7.497ns (Maximum Frequency: 133.387MHz)
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: 9.199ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clock'
  Clock period: 7.497ns (frequency: 133.387MHz)
  Total number of paths / destination ports: 1598 / 41
-------------------------------------------------------------------------
Delay:               7.497ns (Levels of Logic = 33)
  Source:            slow_clock_gen/counter_1 (FF)
  Destination:       slow_clock_gen/counter_31 (FF)
  Source Clock:      clock rising
  Destination Clock: clock rising

  Data Path: slow_clock_gen/counter_1 to slow_clock_gen/counter_31
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDC:C->Q              2   0.720   1.216  slow_clock_gen/counter_1 (slow_clock_gen/counter_1)
     LUT1:I0->O            1   0.551   0.000  slow_clock_gen/Mcount_counter_cy<1>_rt (slow_clock_gen/Mcount_counter_cy<1>_rt)
     MUXCY:S->O            1   0.500   0.000  slow_clock_gen/Mcount_counter_cy<1> (slow_clock_gen/Mcount_counter_cy<1>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<2> (slow_clock_gen/Mcount_counter_cy<2>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<3> (slow_clock_gen/Mcount_counter_cy<3>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<4> (slow_clock_gen/Mcount_counter_cy<4>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<5> (slow_clock_gen/Mcount_counter_cy<5>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<6> (slow_clock_gen/Mcount_counter_cy<6>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<7> (slow_clock_gen/Mcount_counter_cy<7>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<8> (slow_clock_gen/Mcount_counter_cy<8>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<9> (slow_clock_gen/Mcount_counter_cy<9>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<10> (slow_clock_gen/Mcount_counter_cy<10>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<11> (slow_clock_gen/Mcount_counter_cy<11>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<12> (slow_clock_gen/Mcount_counter_cy<12>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<13> (slow_clock_gen/Mcount_counter_cy<13>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<14> (slow_clock_gen/Mcount_counter_cy<14>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<15> (slow_clock_gen/Mcount_counter_cy<15>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<16> (slow_clock_gen/Mcount_counter_cy<16>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<17> (slow_clock_gen/Mcount_counter_cy<17>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<18> (slow_clock_gen/Mcount_counter_cy<18>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<19> (slow_clock_gen/Mcount_counter_cy<19>)
     MUXCY:CI->O           1   0.064   0.000  slow_clock_gen/Mcount_counter_cy<20> (slow_clock_gen/Mcount_counter_cy<20>)
```

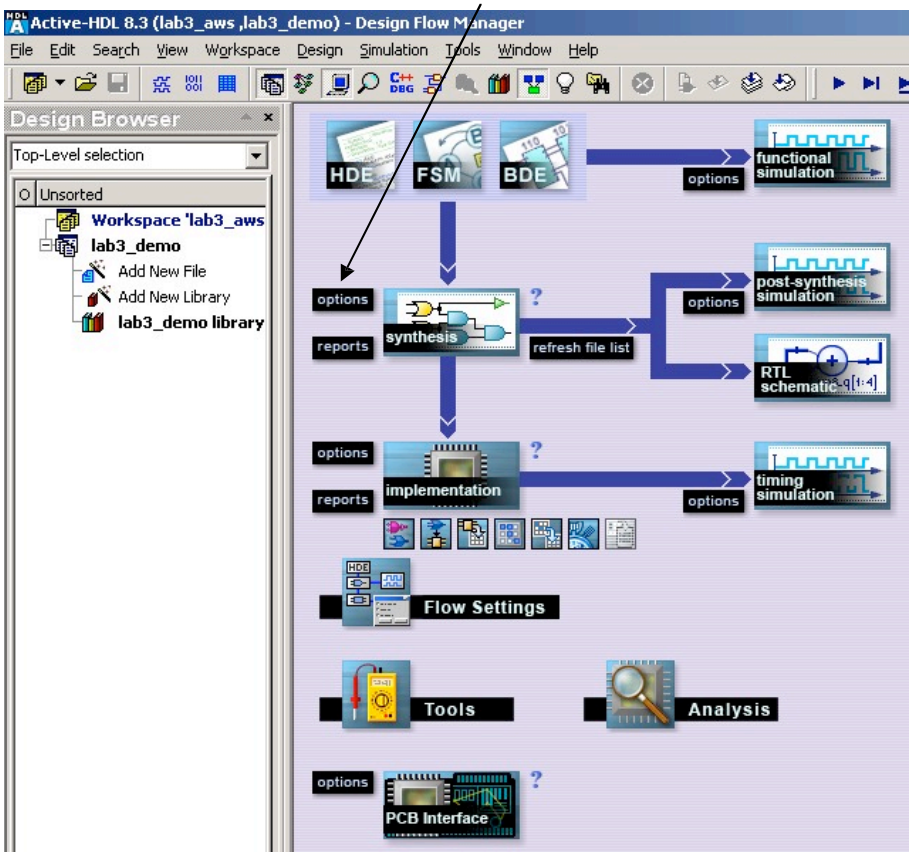
2.2 Synthesis using Synplify Premier DP

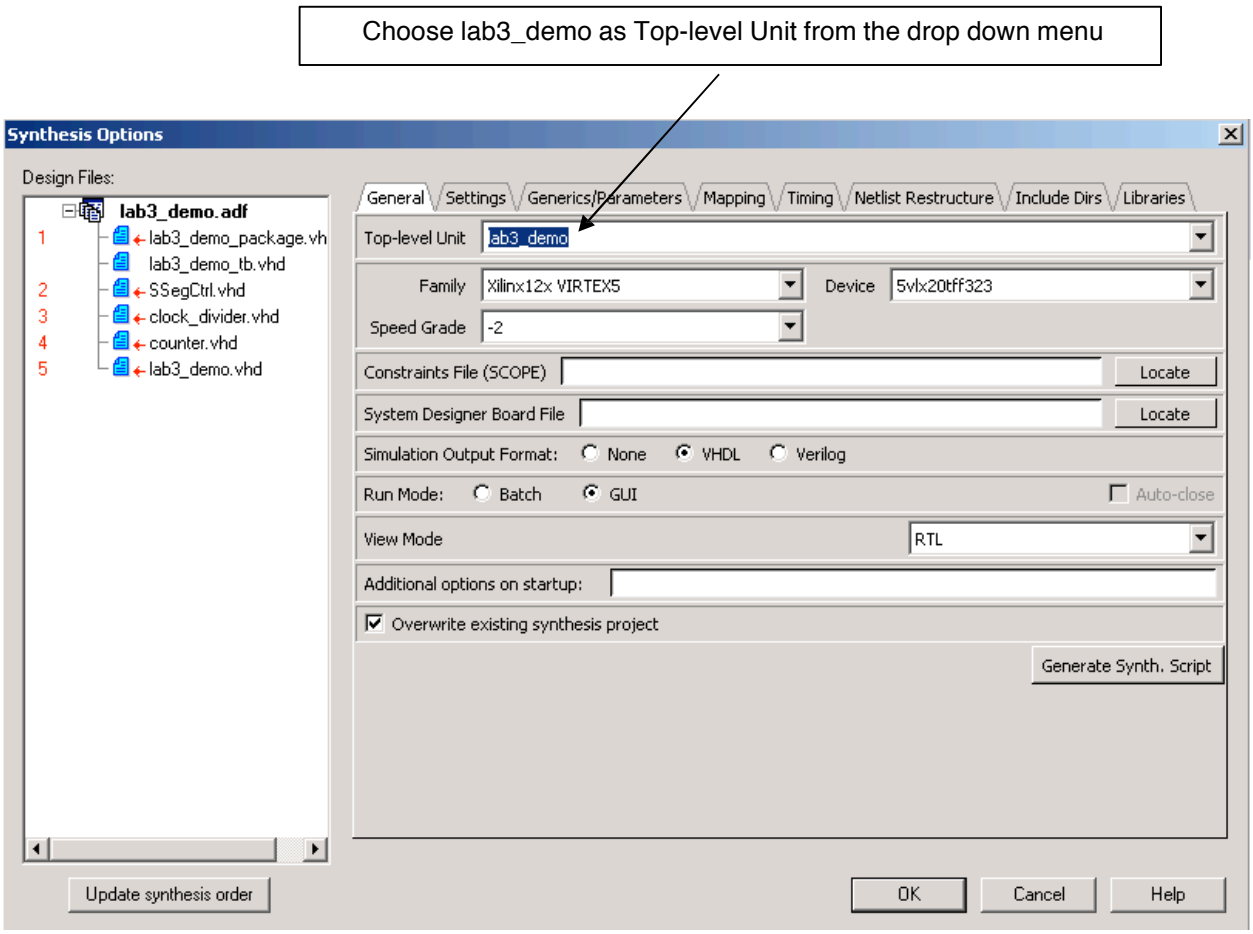
2.2.1 Synthesis Options:



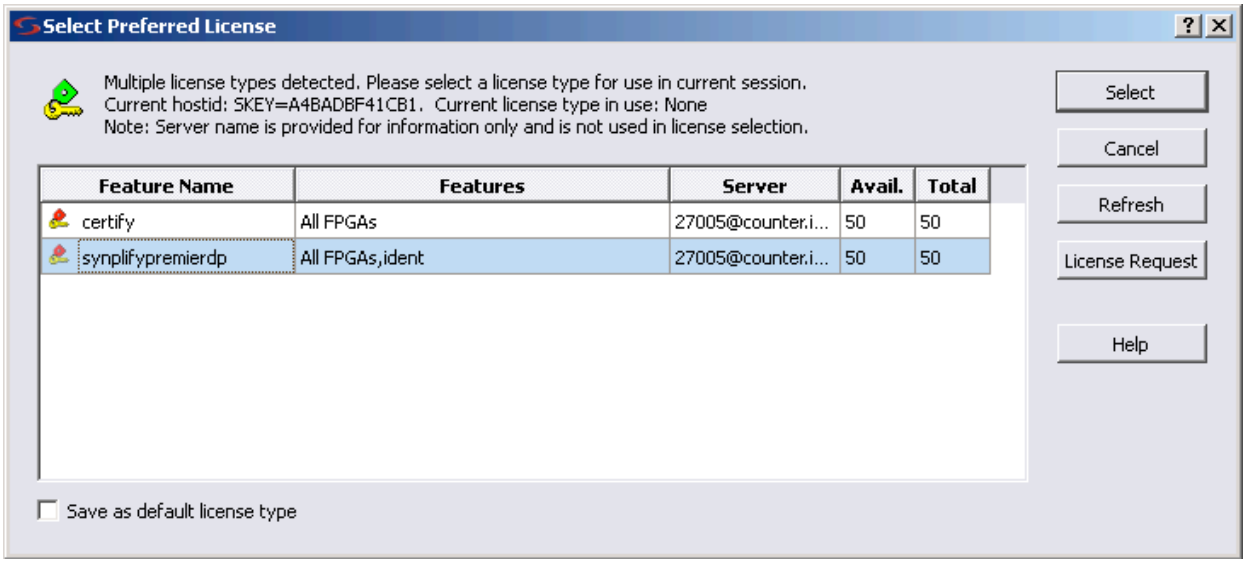


Click on options button to select the synthesis options



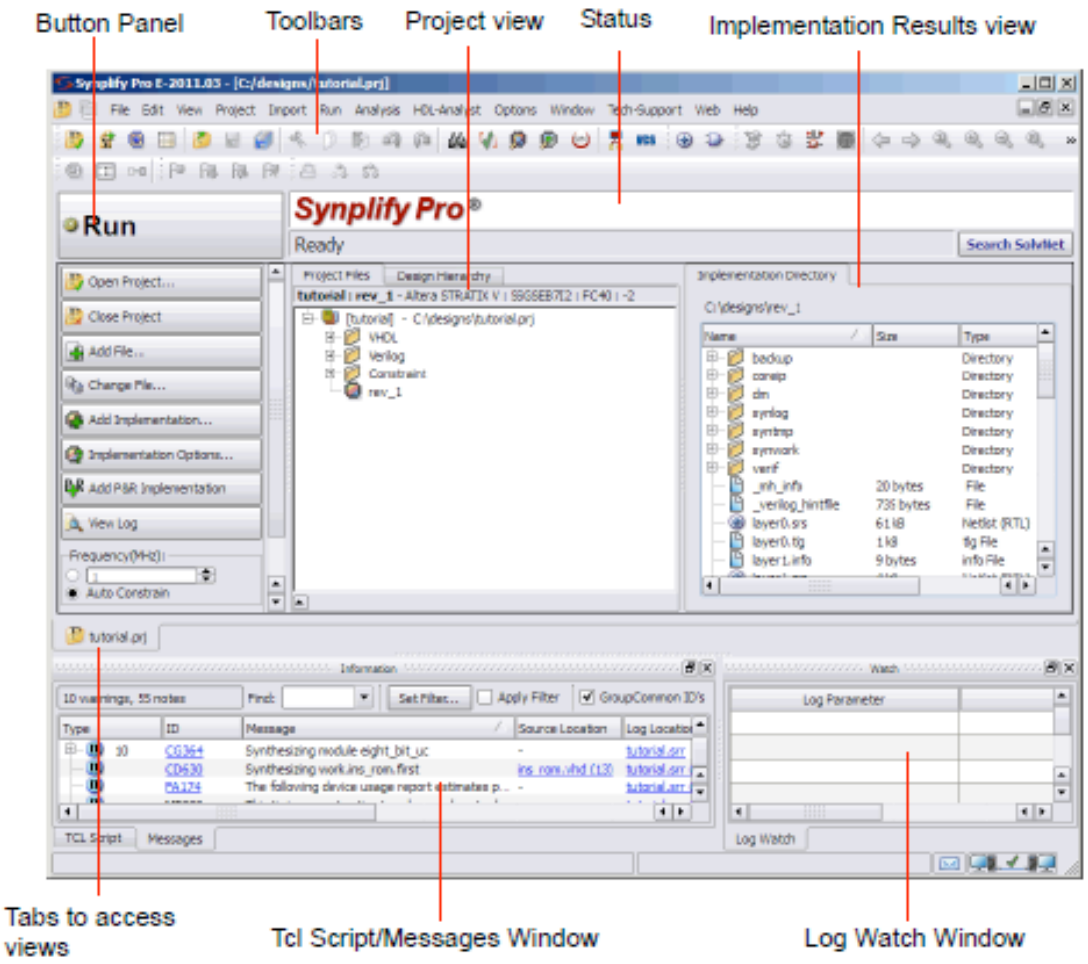


Click OK and then click the “synthesis” button right next to the option button in the Design flow manager. Choose “synplifypremierdp” as your default license type.

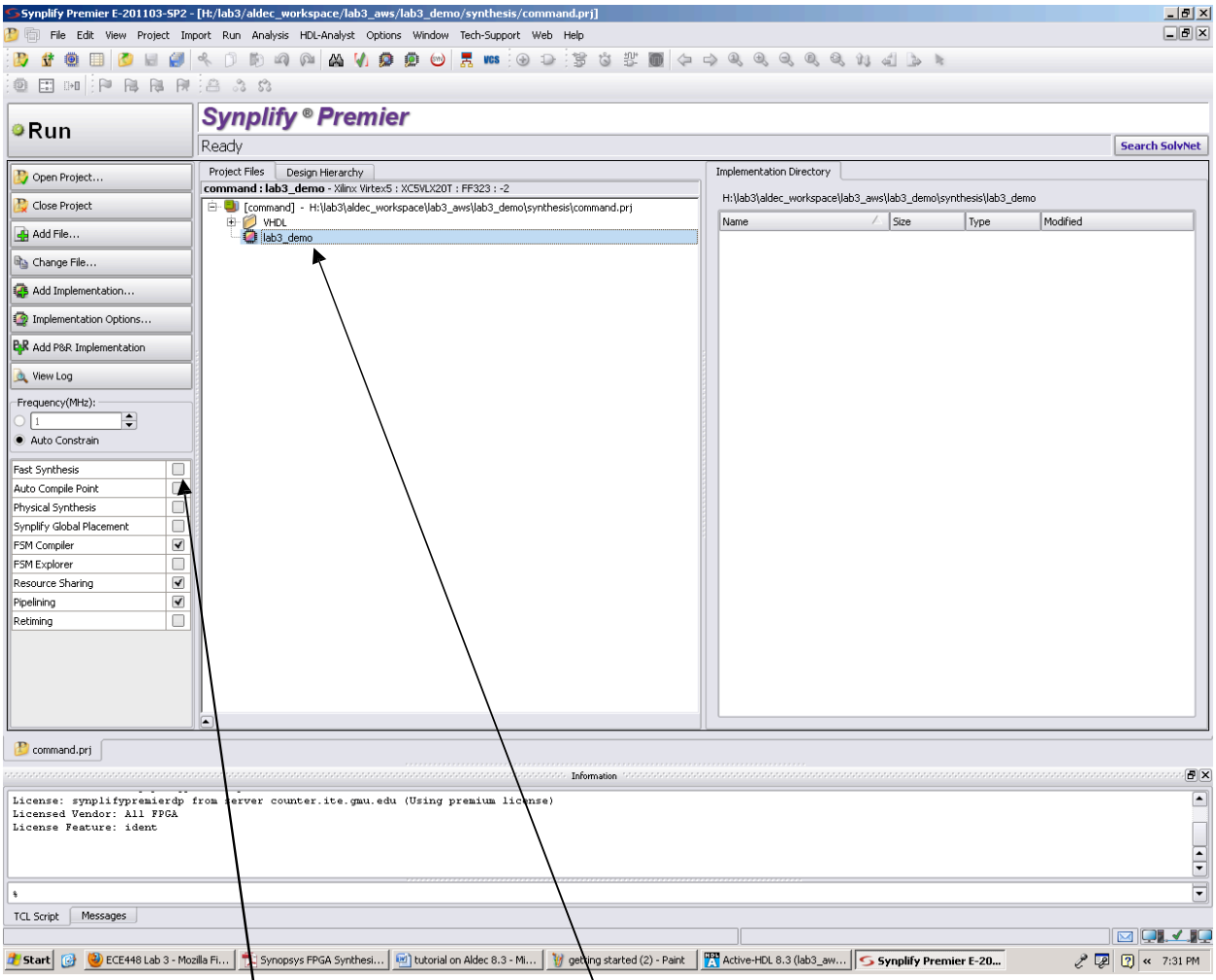


After applying appropriate settings, click on synthesis in the design flow. You should see the following new window.

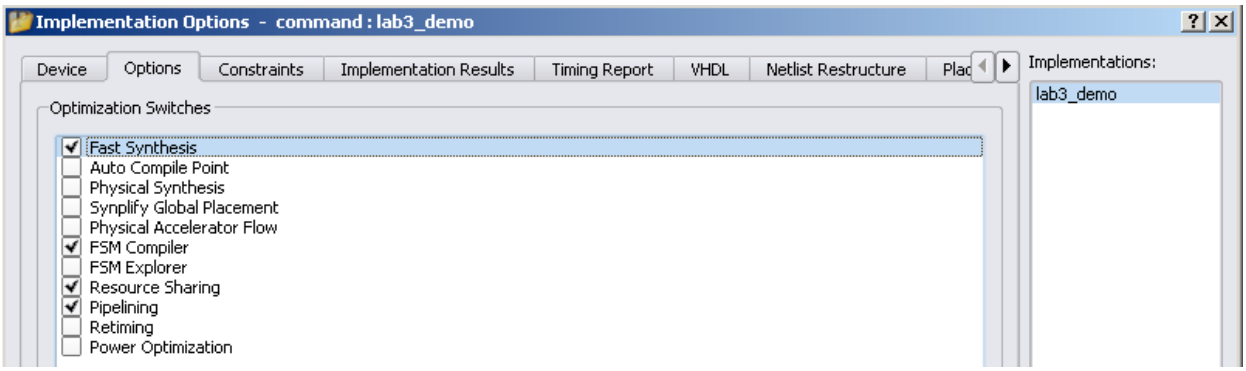
Synplify Pro and Synplify Premier Standard Interface



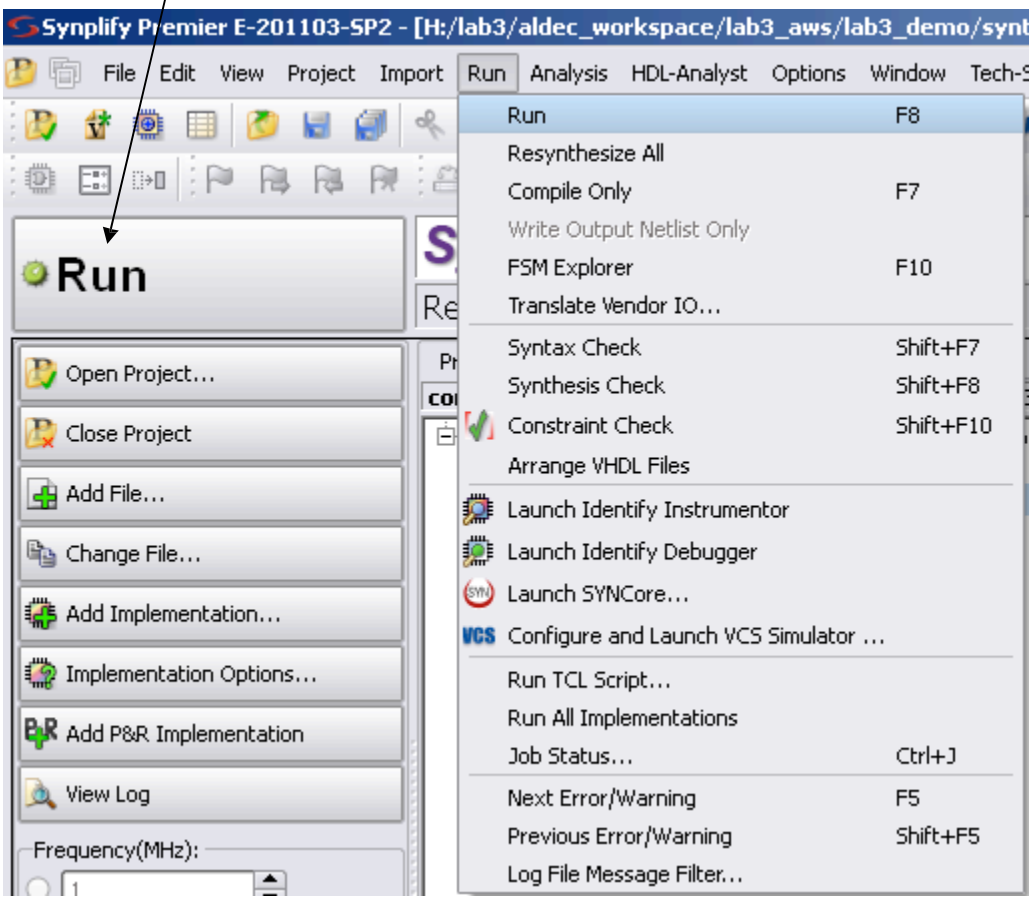
There is no need to create a project and adding VHDL source files. Tool will automatically select lab3_demo as default project.

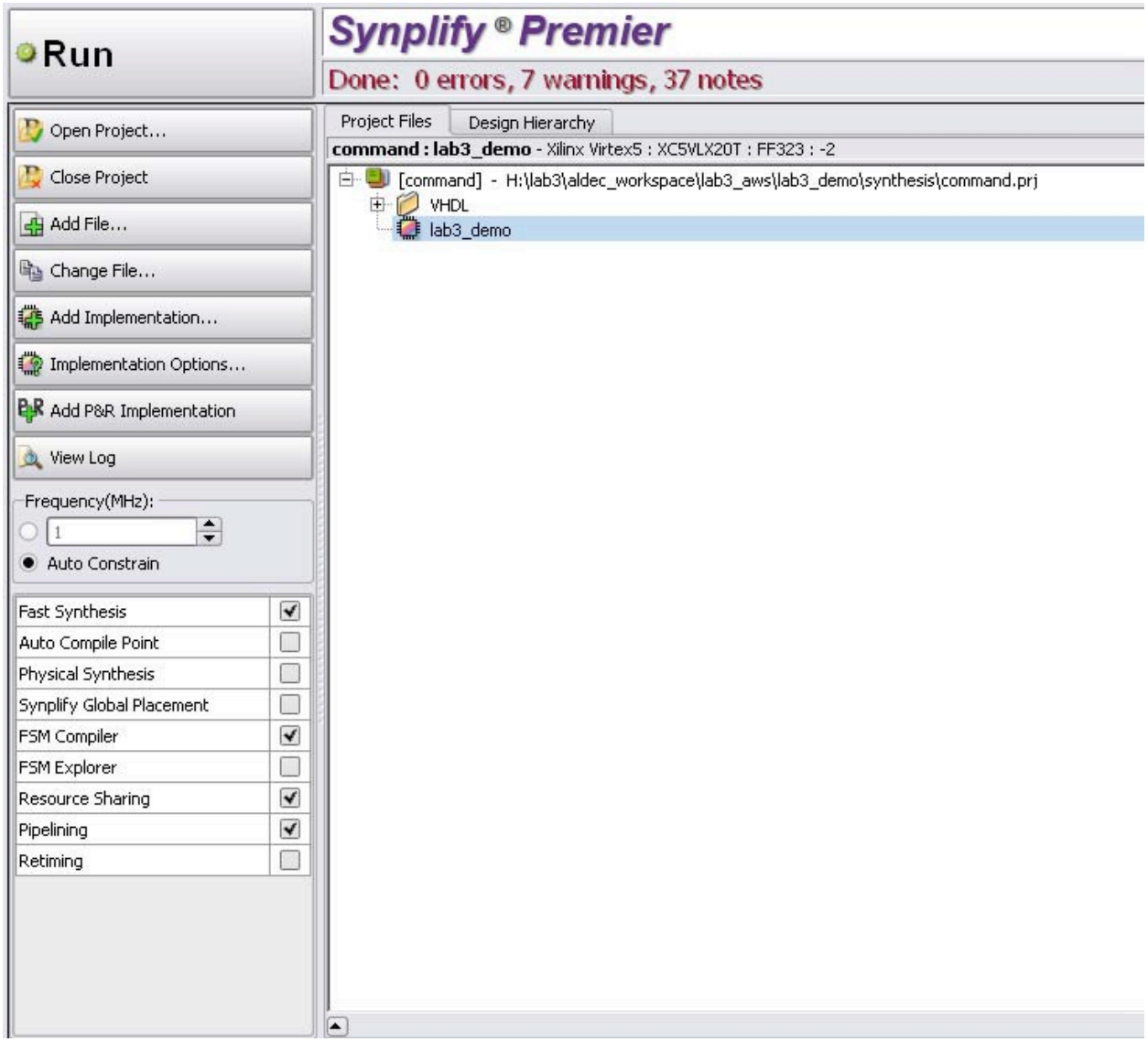


Choose the “Fast Synthesis” option and deselect “Physical Synthesis” option. Alternatively, double-click lab3_demo to select the appropriate synthesis options.

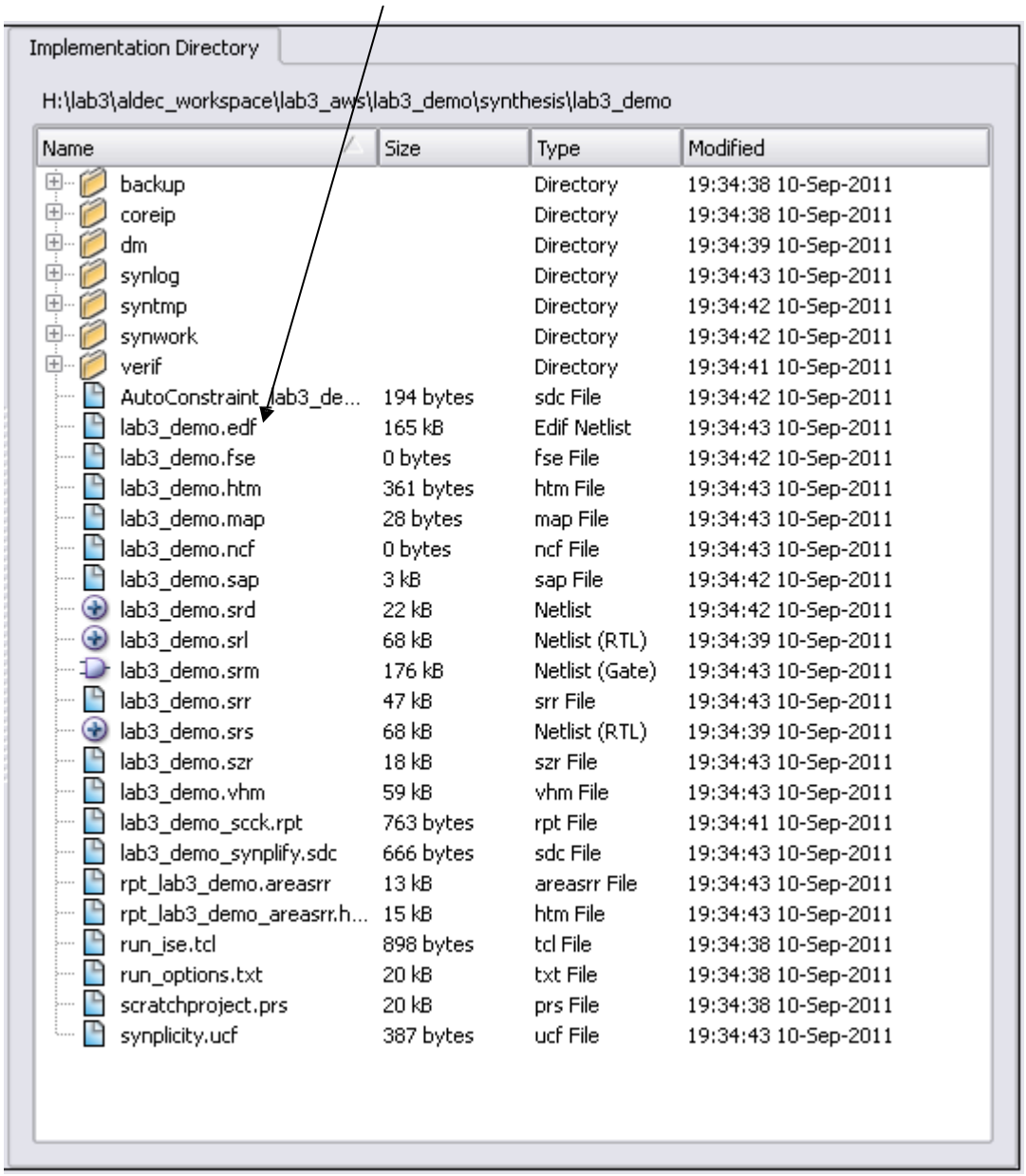


Click on “Run” in the Button panel or select “Run” from the Run menu. Alternatively, press F8 as the shortcut to this menu.




Run
Synplify ® Premier
Done: 0 errors, 7 warnings, 37 notes
Open Project...
Close Project
Add File...
Change File...
Add Implementation...
Implementation Options...
Add P&R Implementation
View Log
Frequency(MHz):
1
Auto Constrain
Fast Synthesis
Auto Compile Point
Physical Synthesis
Synplify Global Placement
FSM Compiler
FSM Explorer
Resource Sharing
Pipelining
Retiming
Project Files
Design Hierarchy
command : lab3_demo - Xilinx Virtex5 : XC5VLX20T : FF323 : -2
[command] - H:\lab3\aldec_workspace\lab3_aws\lab3_demo\synthesis\command.prj
VHDL
lab3_demo

After synthesis, Synplify Premier DP will generate the netlist file lab3_demo.edf in the synthesis folder under the path ..\synthesis\lab3_demo. This file is required by Aldec Active-HDL <version number> for post-synthesis simulation and by Xilinx ISE for implementation.

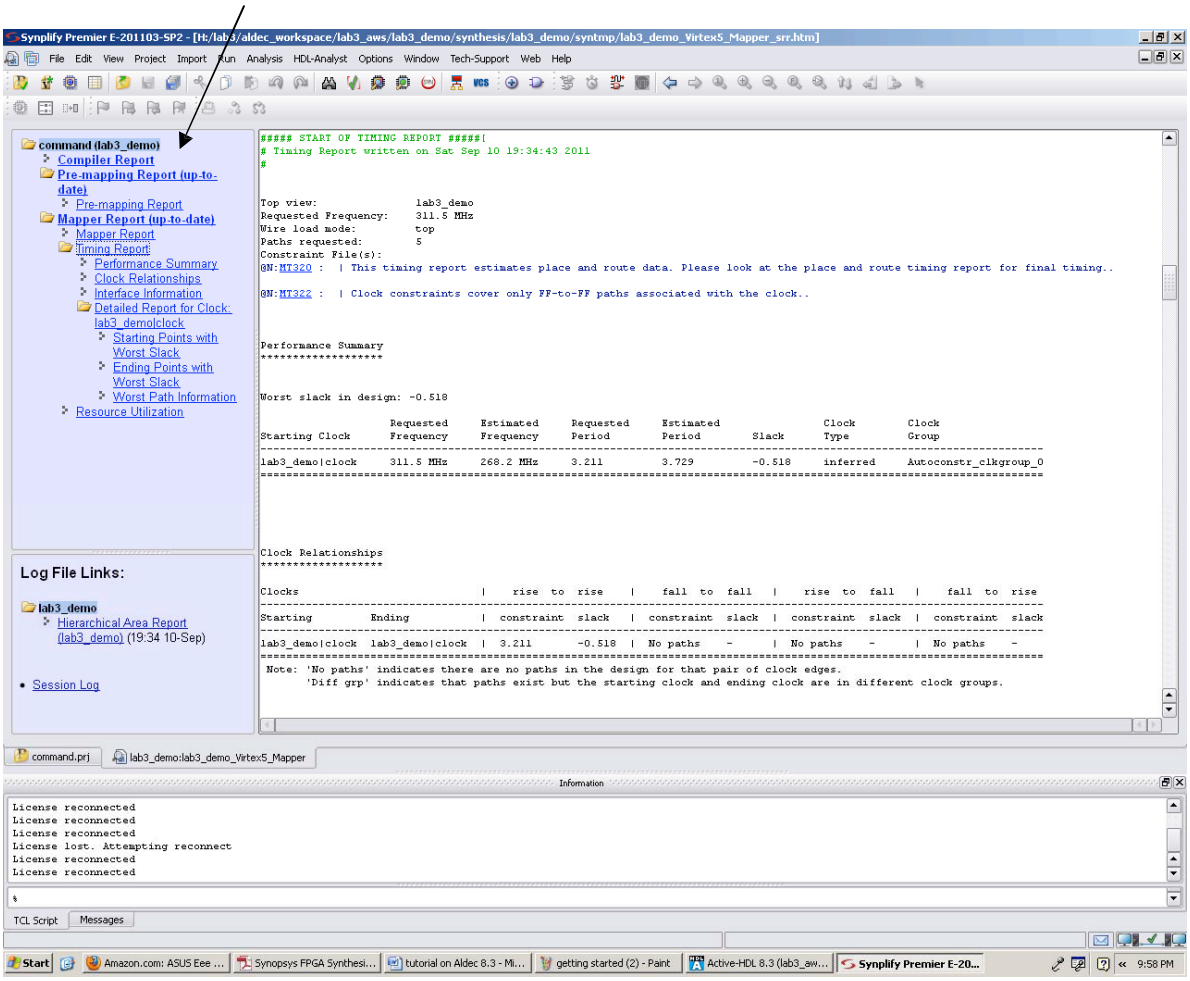


2.2.2 Synthesis Report

Analyze the results, using report file, the HDL Analyst schematic views, the Message window and the Log Watch window.

Log Watch window:

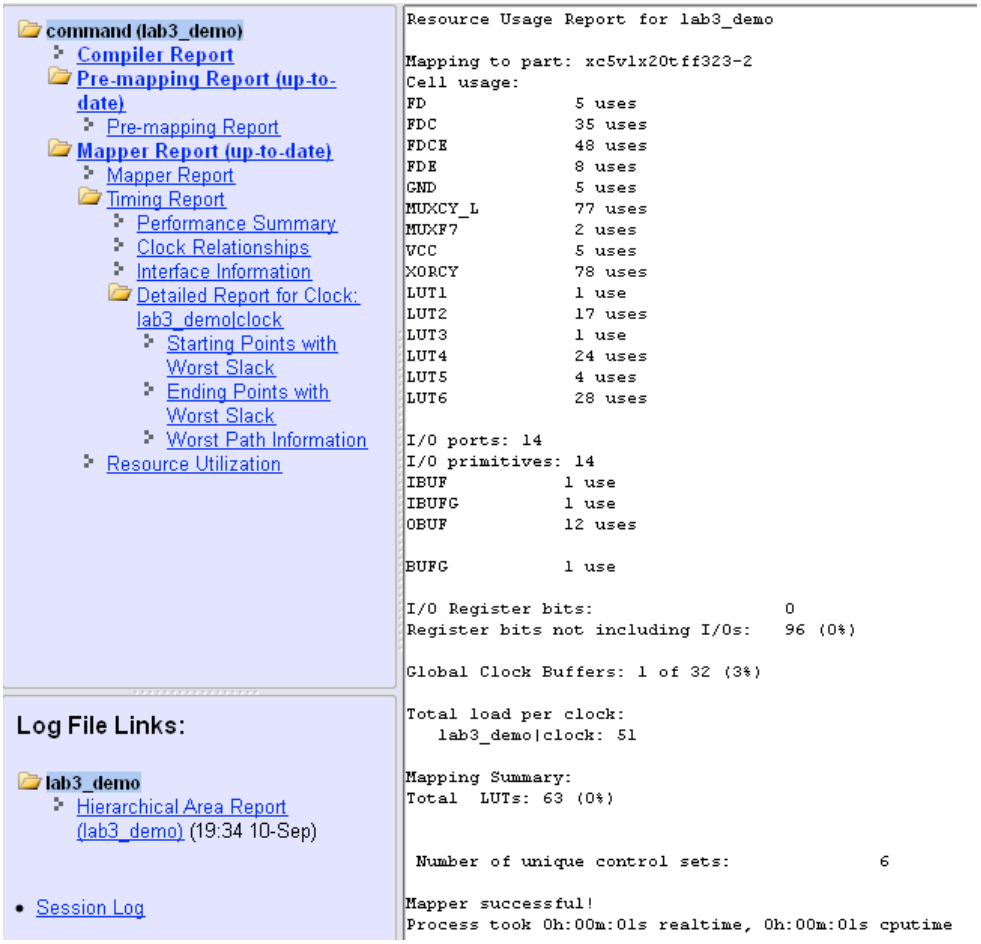
Select **Compiler Report** to analyze the performance summary, timing information, critical path, and resource utilization of the design.



Timing Information:

```
##### START OF TIMING REPORT #####[
# Timing Report written on Sat Sep 10 19:34:43 2011
#


Top view:               lab3_demo
Requested Frequency:    311.5 MHz
Wire load mode:         top
Paths requested:        5
Constraint File(s):
@N:MT320 :  | This timing report estimates place and route data. Please look at the place and route timing report for final

@N:MT322 :  | Clock constraints cover only FF-to-FF paths associated with the clock..



Performance Summary
*******************


Worst slack in design: -0.518

                    Requested     Estimated     Requested     Estimated               Clock        Clock
Starting Clock      Frequency     Frequency     Period        Period        Slack     Type         Group
------------------------------------------------------------------------------------------------------------
lab3_demo|clock     311.5 MHz     268.2 MHz     3.211         3.729         -0.518    inferred     Autoconstr_clkgroup_0
============================================================================================================
```

Mapper Report:



Critical Path Information:

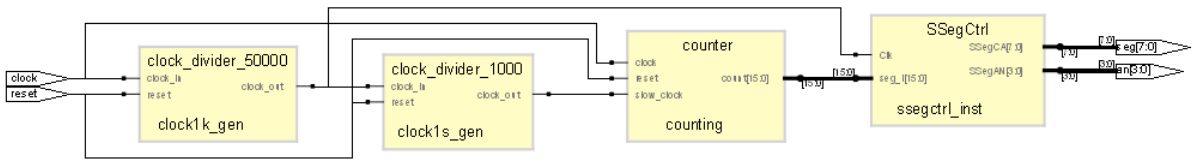
```
Worst Path Information
View Worst Path in Analyst
**********************


Path information for path number 1:
      Requested Period:                       3.211
    - Setup time:                             0.194
    + Clock delay at ending point:            3.682
    = Required time:                          6.698

    - Propagation time:                       3.535
    - Clock delay at starting point:          3.682
    = Slack (critical) :                      -0.518

    Number of logic level(s):                 3
    Starting point:                           clocklk_gen.counter[1] / Q
    Ending point:                             ssegctrl_inst.SSegCA_1[0] / CE
    The start point is clocked by             lab3_demo|clock [rising] on pin C
    The end   point is clocked by             lab3_demo|clock [rising] on pin C

Instance / Net                                      Pin      Pin               Arrival     No. of
Name                                        Type    Name     Dir     Delay     Time        Fan Out(s)
-------------------------------------------------------------------------------------------------
clocklk_gen.counter[1]                      FDC     Q        Out     0.375     4.056       -
counter[1]                                  Net     -        -       0.421     -           3
clocklk_gen.clk_div\.un2_counter_0_5        LUT6    I0       In      -         4.477       -
clocklk_gen.clk_div\.un2_counter_0_5        LUT6    O        Out     0.602     5.079       -
un2_counter_0                               Net     -        -       0.206     -           1
clocklk_gen.clk_div\.un2_counter_6          LUT6    I1       In      -         5.285       -
clocklk_gen.clk_div\.un2_counter_6          LUT6    O        Out     0.516     5.801       -
un2_counter                                 Net     -        -       0.595     -           14
clocklk_gen.clock_RNIFVCP                   LUT2    I1       In      -         6.396       -
clocklk_gen.clock_RNIFVCP                   LUT2    O        Out     0.086     6.482       -
clock_RNIFVCP                               Net     -        -       0.734     -           40
ssegctrl_inst.SSegCA_1[0]                   FDE     CE       In      -         7.216       -
=================================================================================================
Total path delay (propagation time + setup) of 3.729 is 1.773(47.6%) logic and 1.956(52.4%) route.
Path delay compensated for clock skew. Clock skew is added to clock-to-out value, and is subtracted from setup time value
```

Note: Critical path information is also available in HDL Analyst view for better visibility.

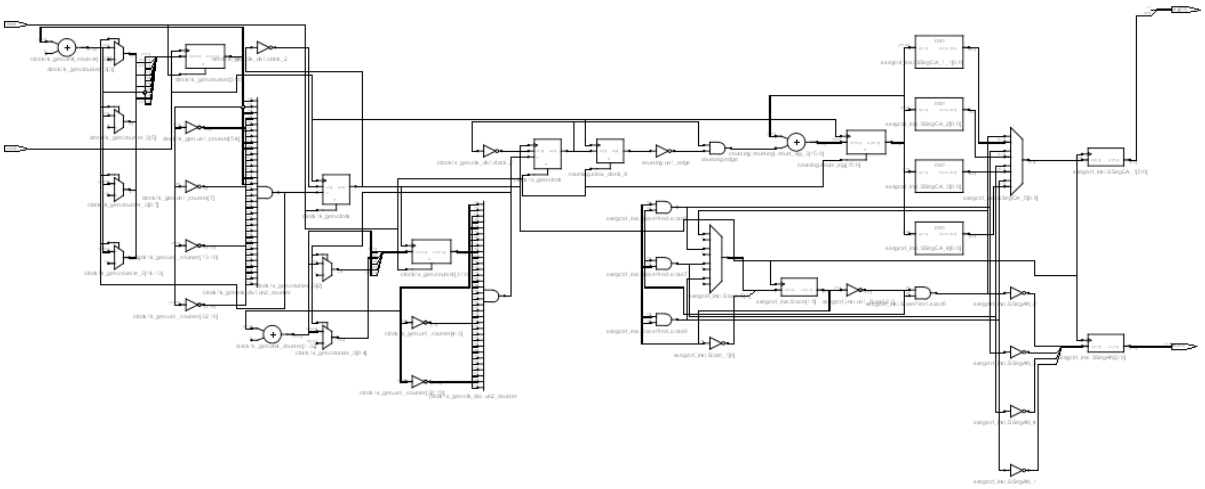
HDL Analyst schematic views:

Select **HDL Analyst-> RTL->Hierarchical View** or **Flattened View** to view the design graphically.

RTL Hierarchical view: most designs are hierarchical so interactive hierarchical viewing helps to better analyze the design.

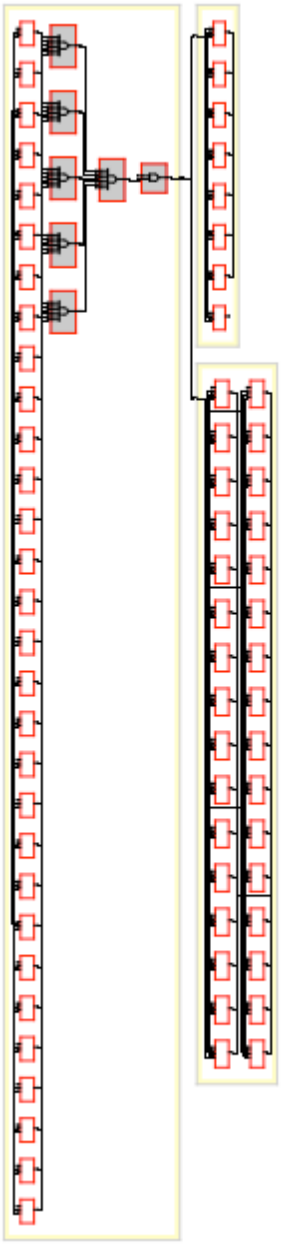


RTL Flattened view: Flattening removes hierarchy so you can view the logic without hierarchy levels.

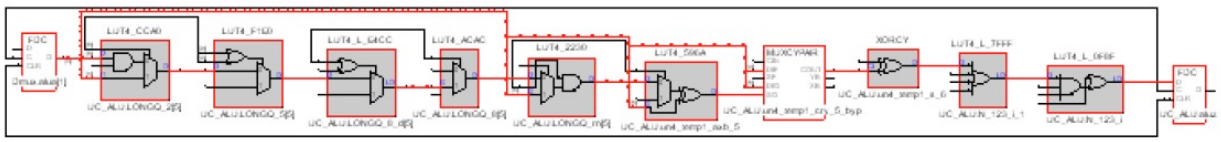


Critical path: lab3_demo

To generate a view of critical path with Physical analyst tool, click on **show critical path (stopwatch icon**  **)** or select the command from the menu.

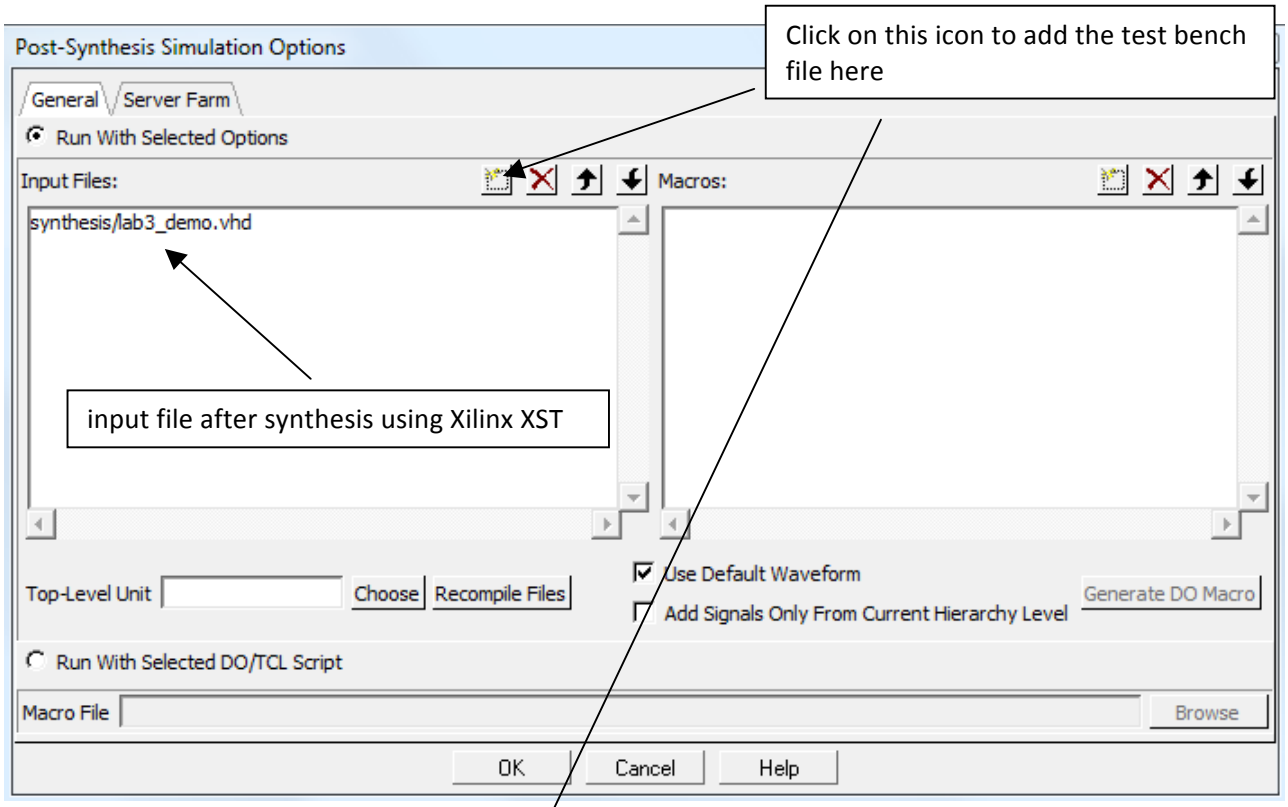


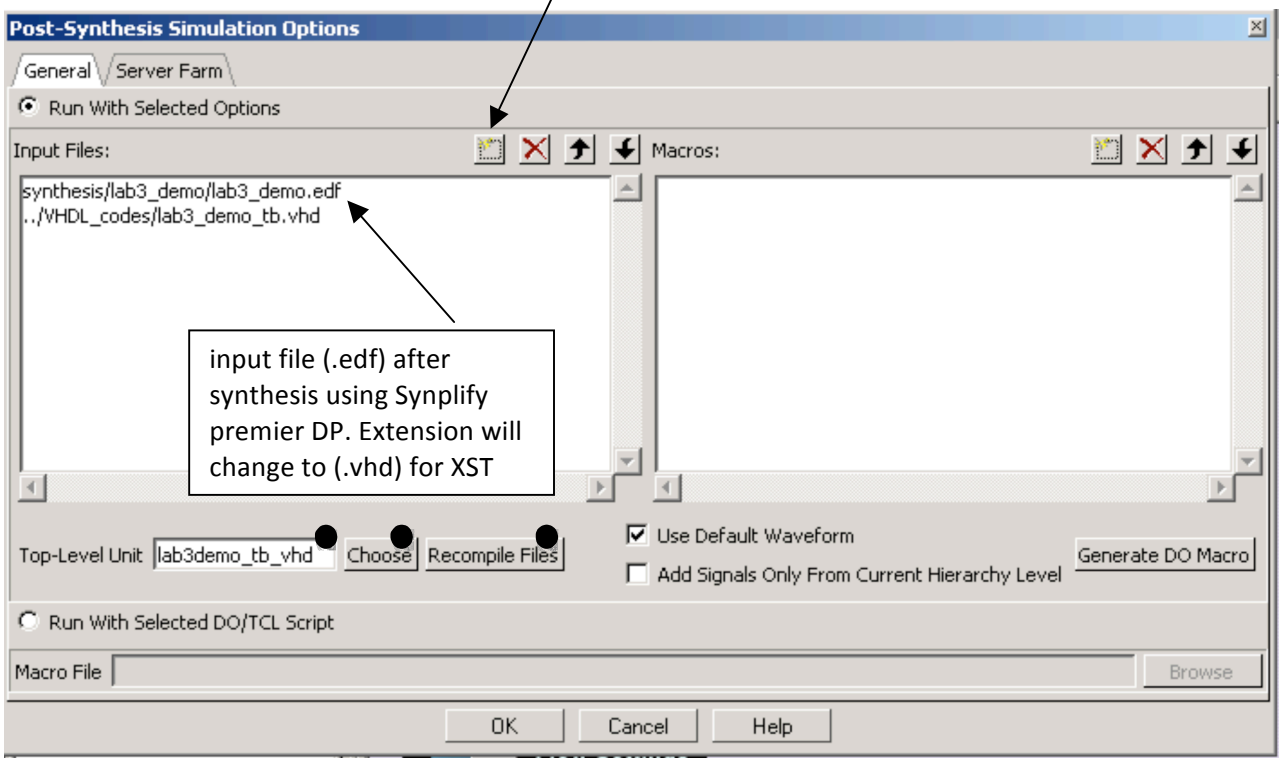
Example report: Critical path

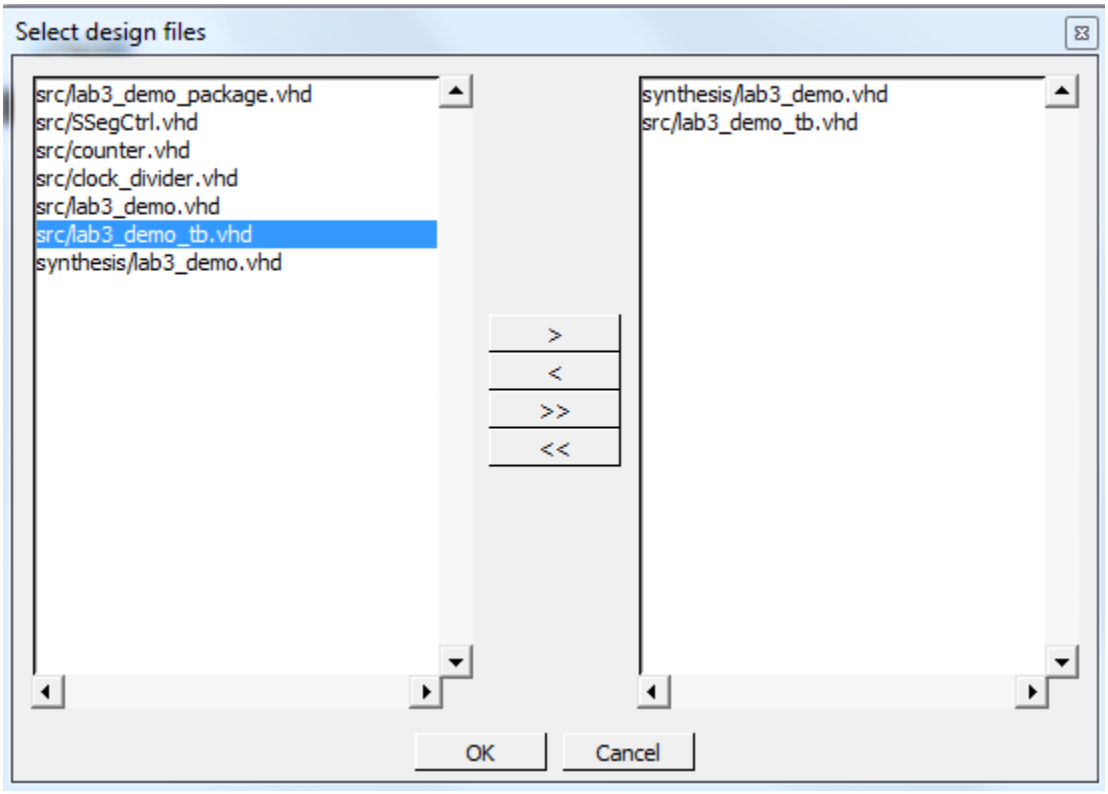


2.3 Post-Synthesis Simulation

Click on the option button next to **post-synthesis simulation** to select the input files. The input file is automatically generated and is included in the post-synthesis simulation option based on your selection for synthesis tool (Xilinx XST or Synplify premier DP).







Click at the **options** button next to the **post-synthesis simulation** icon. Remove the default input file, and select netlist file "lab3_demo.edf" for Synplify Premier DP or "lab3_demo.vhd" for Xilinx XST from synthesis folder and your testbench as an input file by clicking at the button close to the cross sign (marked by a dot). Then, select **Recompile Files.** Once done, choose the appropriate top-level unit, which is *lab3_demo_tb.vhd* in this example.

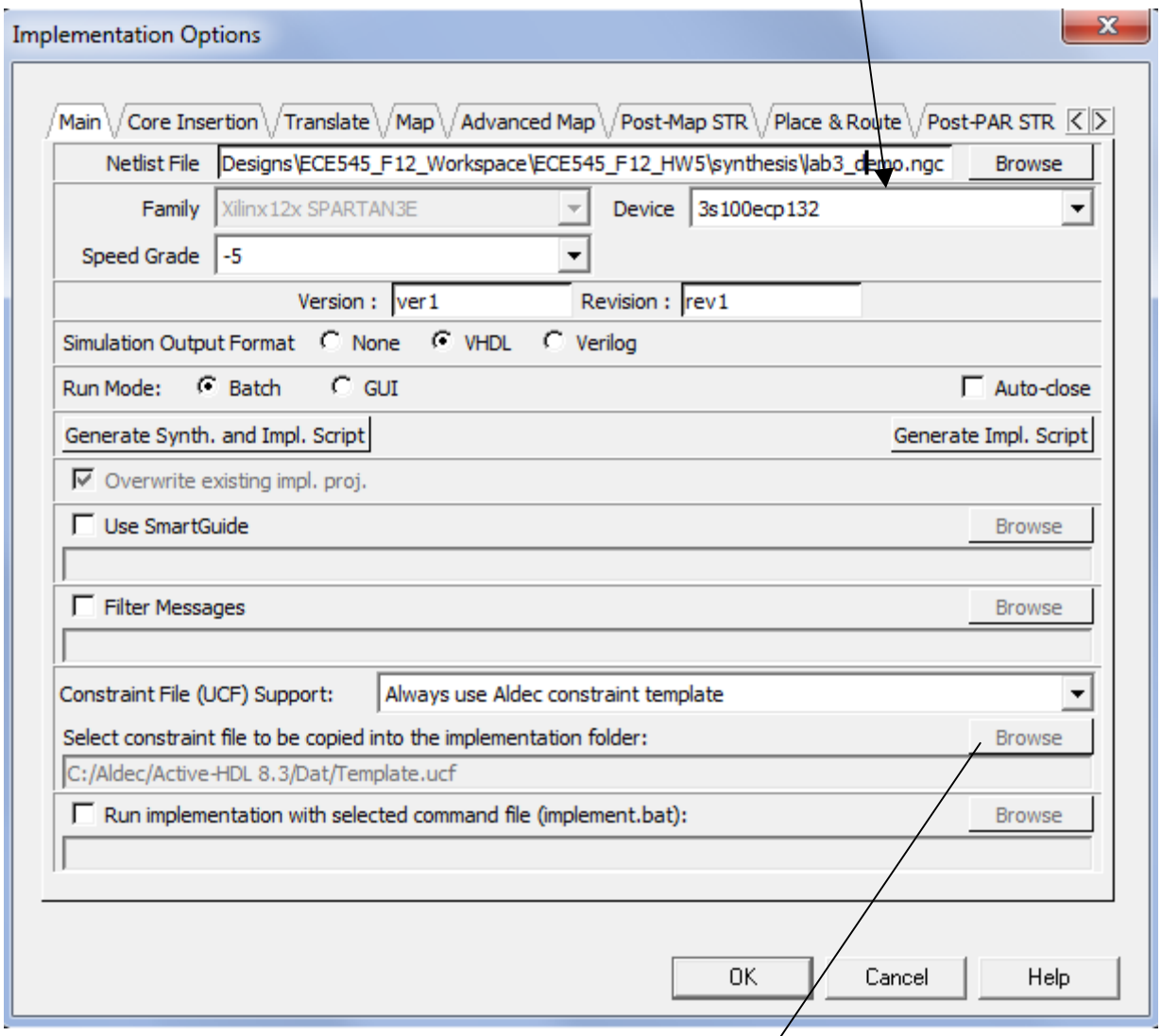
Press **OK**, and then select **post-synthesis simulation**. Now you should see timing waveforms similar to the ones obtained during functional simulation. The difference is that the components and signals are now mapped into appropriate FPGA hardware.

3 Implementation

3.1 Implementation Options

Click on the option button next to timing simulation to perform setting for timing simulations.

Browse to synthesis folder and find Netlist file lab3_demo.edf generated after synthesis (Synplify premier DP) or lab3_demo.ngc afer synthesis (Xilinx XST)



Browse to user constraint file lab3_demo.ucf (use this file only when you want to upload bit stream and program FPGA. Otherwise, skip this step

Click at the **options** button next to the **implementation** icon. Select the correct **Netlist File** which is a file with the same name as your top level VHDL file and the extension *.edf (for Synplify Premier DP) or *.ngc (for Xilinx Implementation tool). This file is normally located in the synthesis folder of your workspace. Use this file to implement your design. Choose the correct FPGA Family, Device and Speed Grade, the same as used during the Synthesis phase:

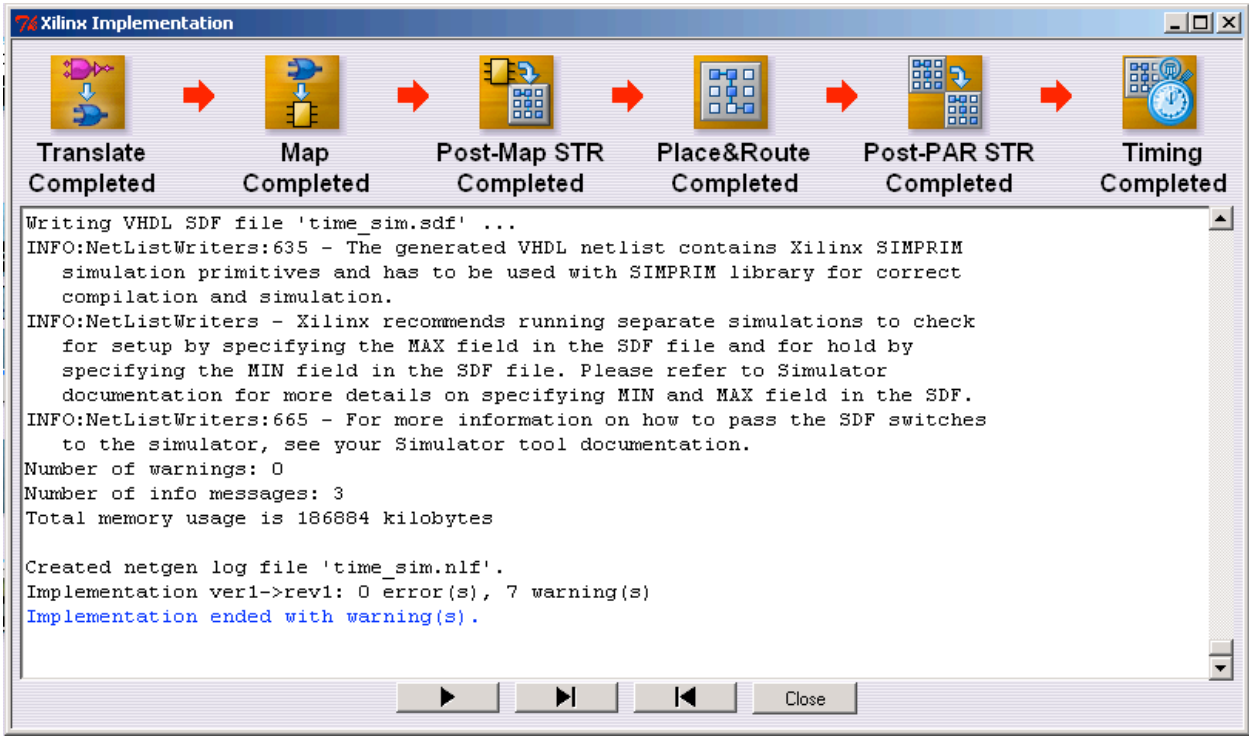
In our example these should be (please ignore values given in the screen shot above):

Family : Xilinx<version_number>x SPARTAN6

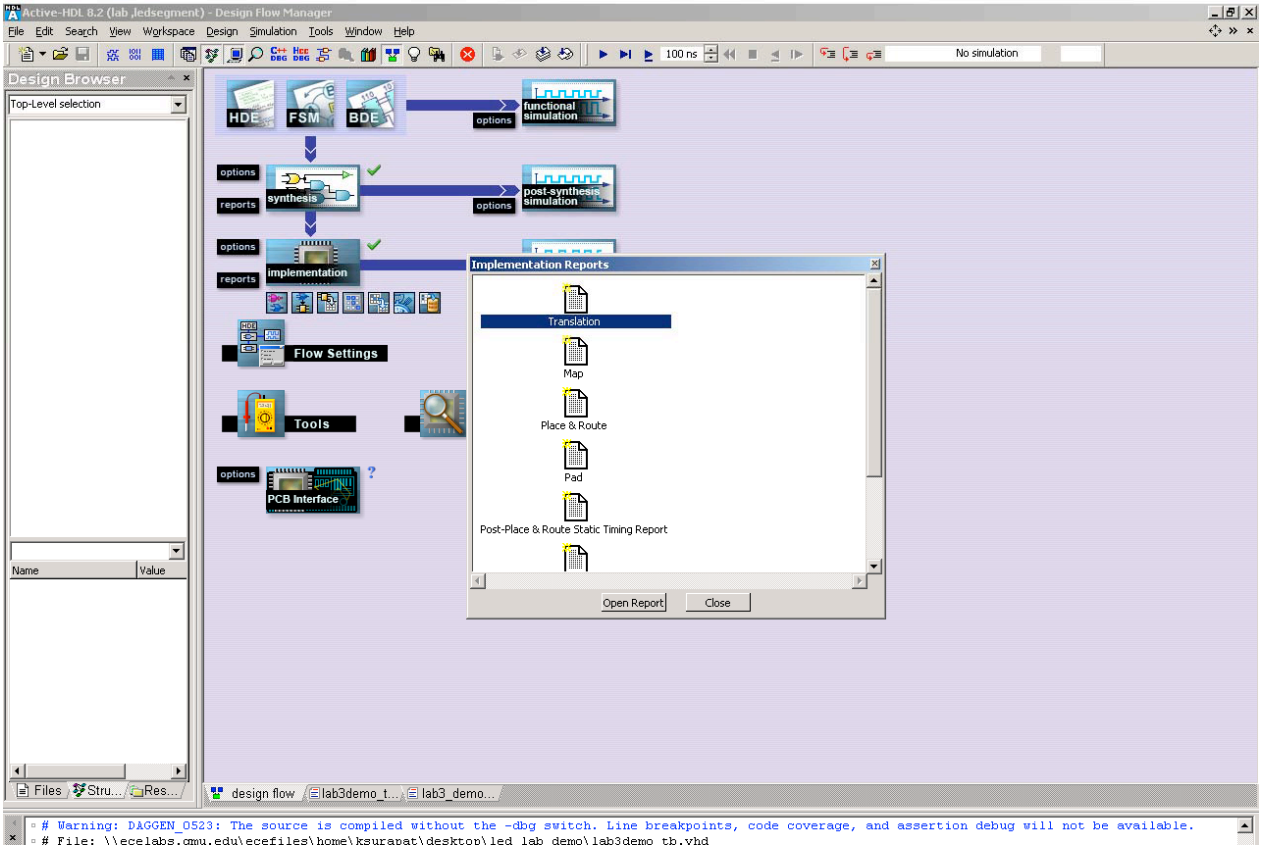
Device : XC6LX16-CS324.

Speed Grade : -3.

3.1 Implementation Reports Analysis



Similarly to synthesis, you can access the generated reports by clicking the **reports** button**,** near the **implementation** icon. Unlike synthesis log, implementation report is divided into several smaller reports, which are named differently. Below is a list of reports in which you can find the most useful information about your design after implementation, such as resource utilization, maximum clock frequency, and critical path:



Resource Utilization:

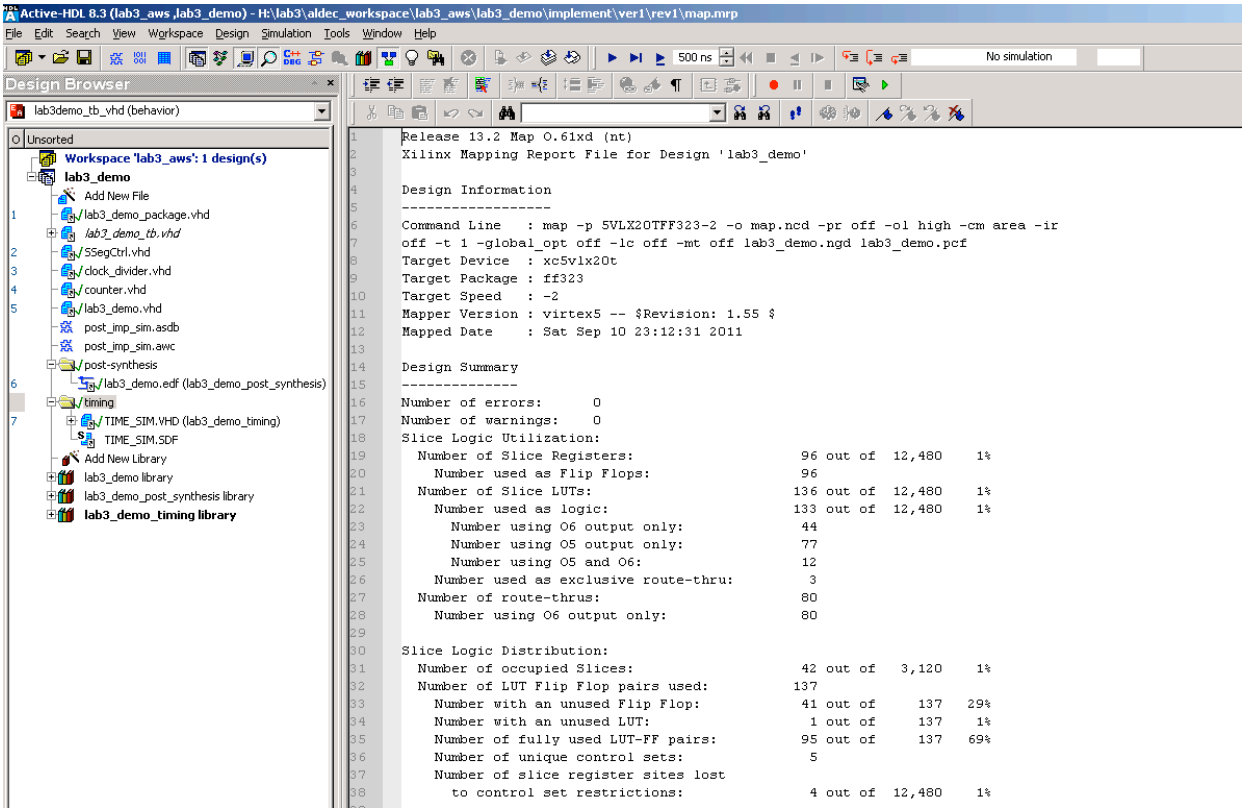
- Map : See *Design Summary*
- Place & Route : See *Device Utilization Summary*

Note: Place & Route provides overall information about the design after placing and routing. Map provides a more detailed summary of resource utilization.

Minimum Clock Period (Maximum Frequency):

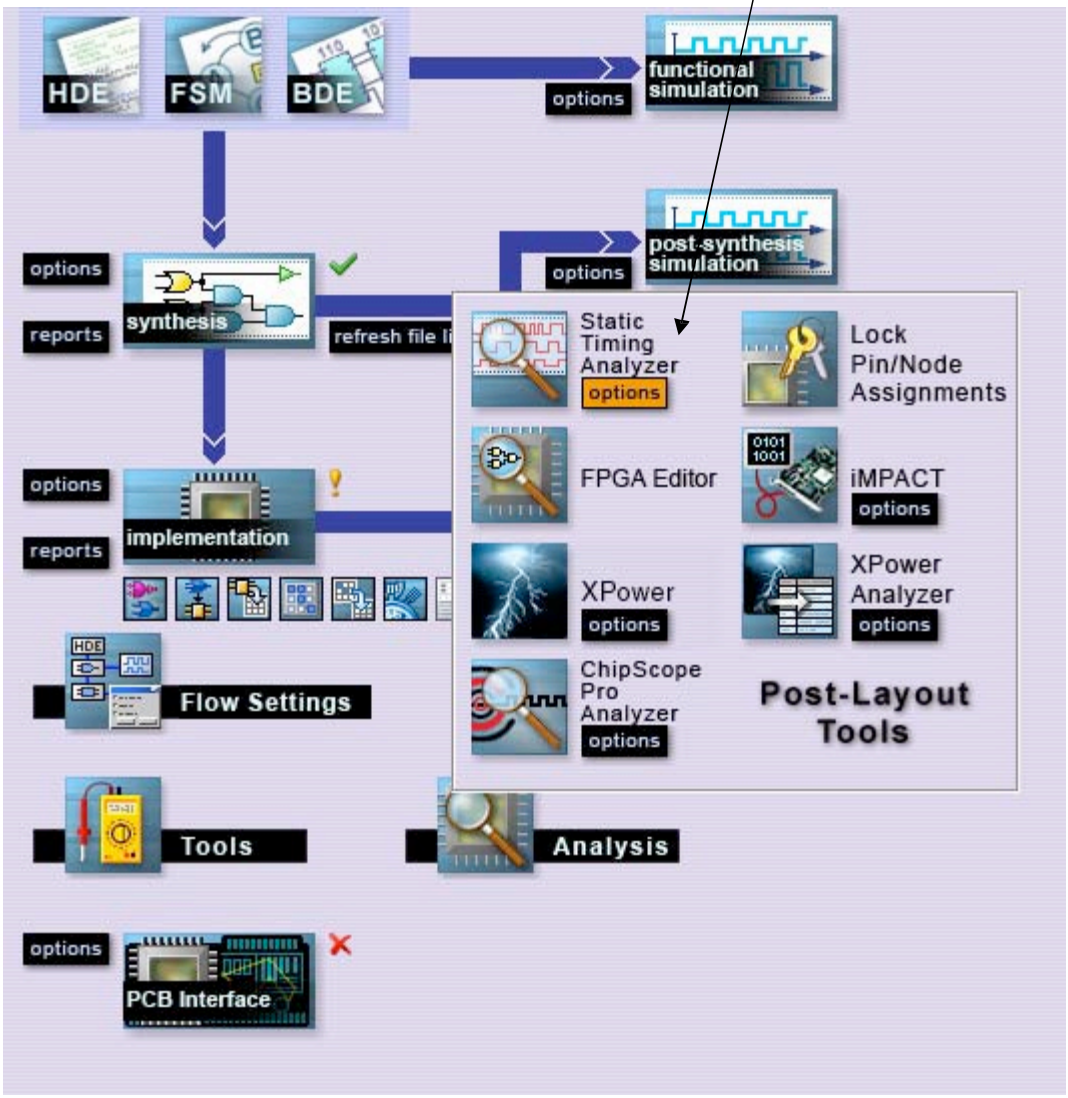
- Post-Place & Route Static Timing Report

This file describes the worst case scenario in terms of minimum clock period. However, since the implementation tools do not provide complete information, please refer to **Timing Analysis** below for a more detailed report.
Note: Post-Map Static Timing Report can be ignored because it provides timing report before placing & routing, and thus cannot correctly predict interconnect delays.

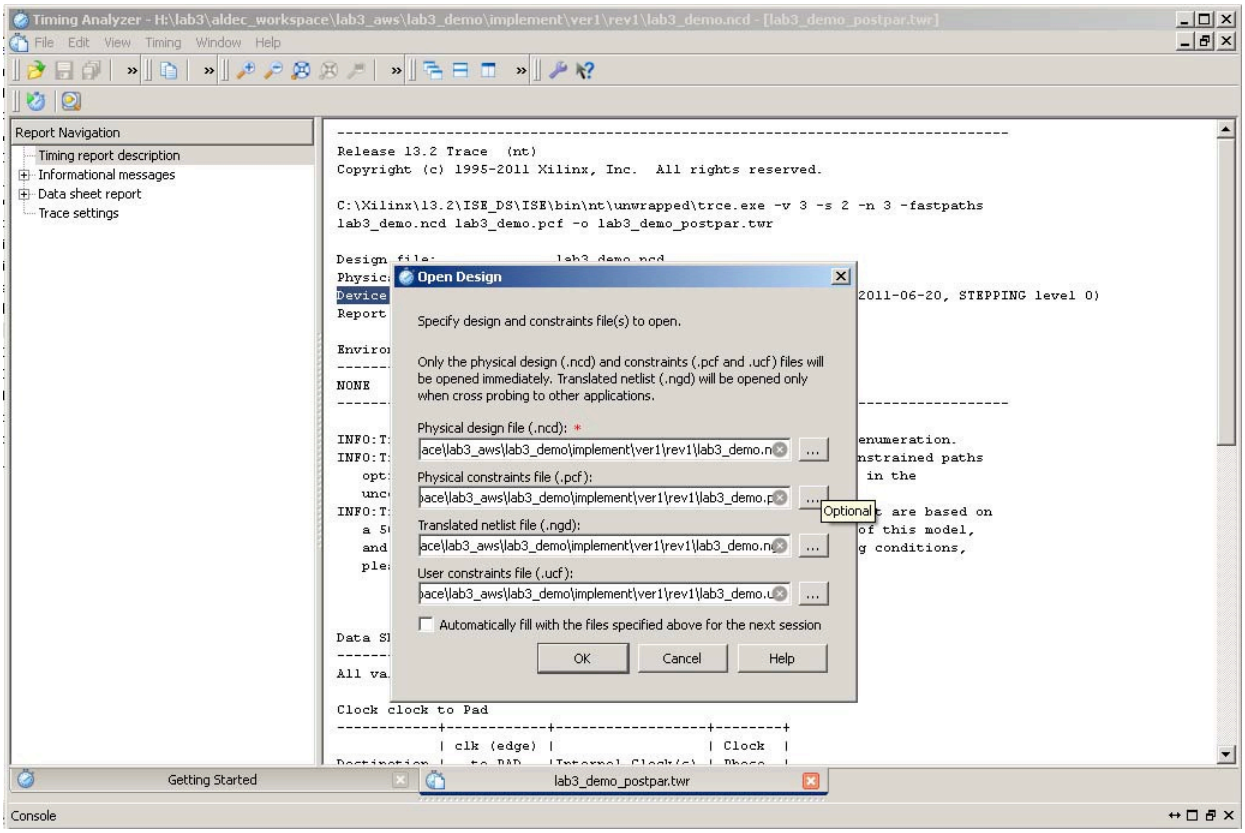

Active-HDL 8.3 (lab3_aws ,lab3_demo) - H:\lab3\aldec_workspace\lab3_aws\lab3_demo\implement\ver1\rev1\map.mrp
File Edit Search View Workspace Design Simulation Tools Window Help
500 ns
No simulation
Design Browser
lab3demo_tb_vhd (behavior)
Unsorted
Workspace 'lab3_aws': 1 design(s)
lab3_demo
Add New File
lab3_demo_package.vhd
lab3_demo_tb.vhd
SSegCtrl.vhd
clock_divider.vhd
counter.vhd
lab3_demo.vhd
post_imp_sim.asdb
post_imp_sim.awc
post-synthesis
lab3_demo.edf (lab3_demo_post_synthesis)
timing
TIME_SIM.VHD (lab3_demo_timing)
TIME_SIM.SDF
Add New Library
lab3_demo library
lab3_demo_post_synthesis library
lab3_demo_timing library
Release 13.2 Map O.61xd (nt)
Xilinx Mapping Report File for Design 'lab3_demo'
Design Information
Command Line : map -p 5VLX20TFF323-2 -o map.ncd -pr off -ol high -cm area -ir
off -t 1 -global_opt off -lc off -mt off lab3_demo.ngd lab3_demo.pcf
Target Device : xc5vlx20t
Target Package : ff323
Target Speed : -2
Mapper Version : virtex5 -- $Revision: 1.55 $
Mapped Date : Sat Sep 10 23:12:31 2011
Design Summary
Number of errors: 0
Number of warnings: 0
Slice Logic Utilization:
Number of Slice Registers: 96 out of 12,480 1%
Number used as Flip Flops: 96
Number of Slice LUTs: 136 out of 12,480 1%
Number used as logic: 133 out of 12,480 1%
Number using O6 output only: 44
Number using O5 output only: 77
Number using O5 and O6: 12
Number used as exclusive route-thru: 3
Number of route-thrus: 80
Number using O6 output only: 80
Slice Logic Distribution:
Number of occupied Slices: 42 out of 3,120 1%
Number of LUT Flip Flop pairs used: 137
Number with an unused Flip Flop: 41 out of 137 29%
Number with an unused LUT: 1 out of 137 1%
Number of fully used LUT-FF pairs: 95 out of 137 69%
Number of unique control sets: 5
Number of slice register sites lost
to control set restrictions: 4 out of 12,480 1%

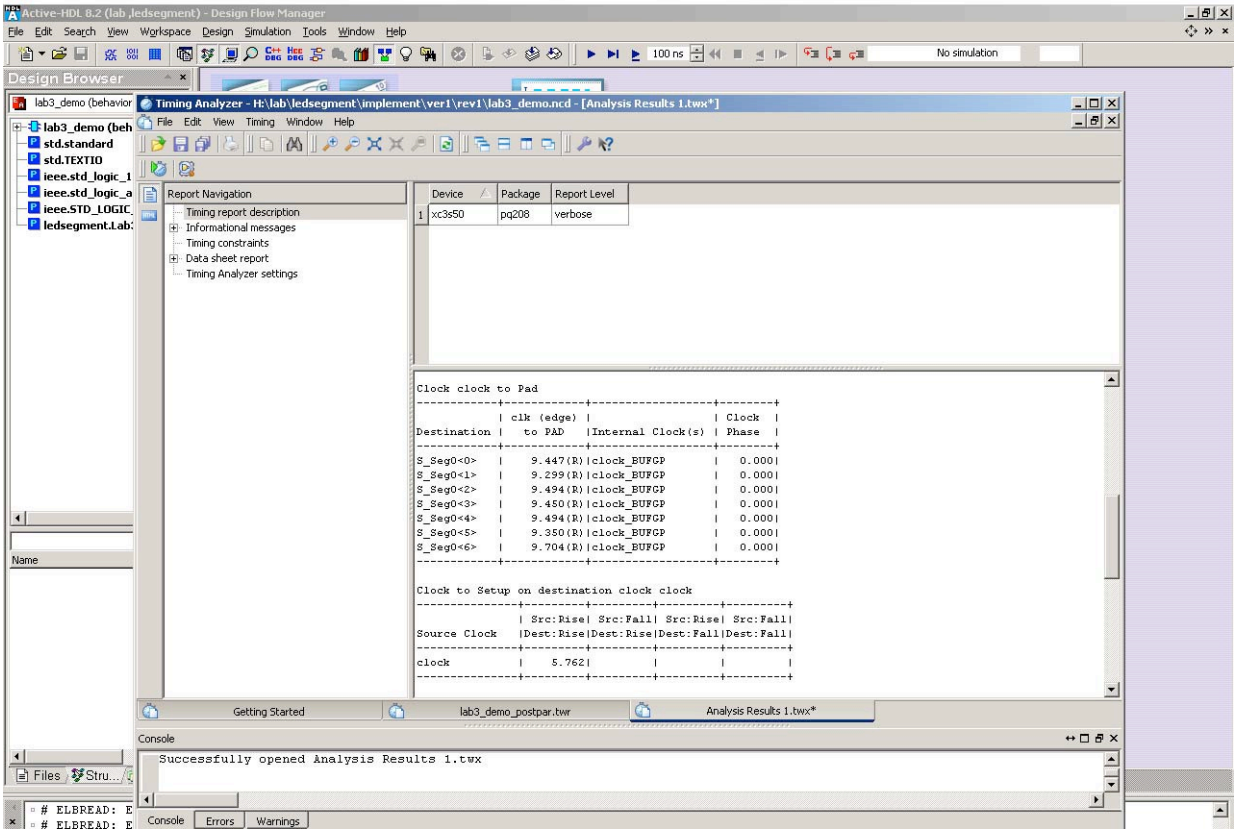
Timing Analysis (Clock Period, Maximum Frequency and Critical Path)

For the detailed analysis of critical path and minimum clock period (or maximum frequency) a separate timing analyzer provided by Xilinx should be used. To generate the report, select **Analysis -> Static Timing Analyzer** from the **Flow** panel. This will open Xilinx Timing Analyzer. You can also navigate to the program from the Windows menu. The path used in the ECE labs at GMU is by **Start->All Programs -> VLSI Tools -> Xilinx ISE ->Accessories ->Timing Analyzer**.



Once the program is opened, select **Open**, choose netlist file located in /implement/ver1/rev1 of your workspace, *.ncd, and press **OK**. Selecting **Analyze against Auto Generated Design Constraints** will generate a static timing report.

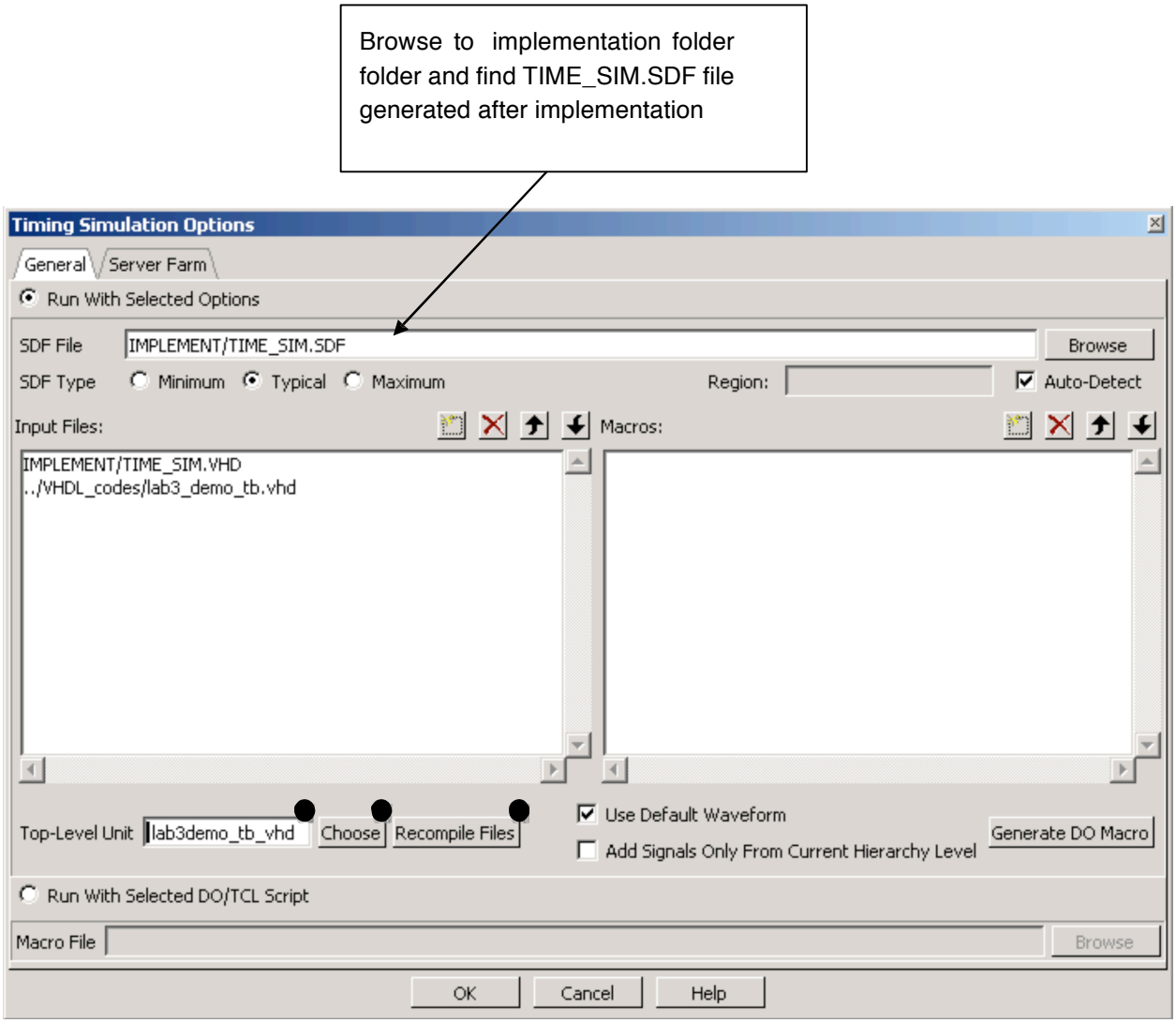

Timing Analyzer - H:\lab3\aldec_workspace\lab3_aws\lab3_demo\implement\ver1\rev1\lab3_demo.ncd - [lab3_demo_postpar.twr]
File Edit View Timing Window Help
Report Navigation
Timing report description
Informational messages
Data sheet report
Trace settings
Release 13.2 Trace (nt)
Copyright (c) 1995-2011 Xilinx, Inc. All rights reserved.
C:\Xilinx\13.2\ISE_DS\ISE\bin\nt\unwrapped\trce.exe -v 3 -s 2 -n 3 -fastpaths
lab3_demo.ncd lab3_demo.pcf -o lab3_demo_postpar.twr
Open Design
Specify design and constraints file(s) to open.
Only the physical design (.ncd) and constraints (.pcf and .ucf) files will be opened immediately. Translated netlist (.ngd) will be opened only when cross probing to other applications.
Physical design file (.ncd): *
Physical constraints file (.pcf):
Optional
Translated netlist file (.ngd):
User constraints file (.ucf):
Automatically fill with the files specified above for the next session
OK
Cancel
Help
Clock clock to Pad
Getting Started
lab3_demo_postpar.twr
Console


Active-HDL 8.2 (lab ,ledsegment) - Design Flow Manager
File Edit Search View Workspace Design Simulation Tools Window Help
Design Browser
lab3_demo (behavior
lab3_demo (beh
std.standard
std.TEXTIO
ieee.std_logic_1
ieee.std_logic_a
ieee.STD_LOGIC_
ledsegment.Lab:
Timing Analyzer - H:\lab\ledsegment\implement\ver1\rev1\lab3_demo.ncd - [Analysis Results 1.twx*]
File Edit View Timing Window Help
Report Navigation
Timing report description
Informational messages
Timing constraints
Data sheet report
Timing Analyzer settings
Device
Package
Report Level
xc3s50
pq208
verbose
Clock clock to Pad
Destination
clk (edge) to PAD
Internal Clock(s)
Clock Phase
S_Seg0<0> 9.447(R) clock_BUFGP 0.000
S_Seg0<1> 9.299(R) clock_BUFGP 0.000
S_Seg0<2> 9.494(R) clock_BUFGP 0.000
S_Seg0<3> 9.450(R) clock_BUFGP 0.000
S_Seg0<4> 9.494(R) clock_BUFGP 0.000
S_Seg0<5> 9.350(R) clock_BUFGP 0.000
S_Seg0<6> 9.704(R) clock_BUFGP 0.000
Clock to Setup on destination clock clock
Source Clock
Src:Rise Dest:Rise
Src:Fall Dest:Rise
Src:Rise Dest:Fall
Src:Fall Dest:Fall
clock 5.762
Getting Started
lab3_demo_postpar.twr
Analysis Results 1.twx*
Console
Successfully opened Analysis Results 1.twx
Console
Errors
Warnings
Files
Stru...
ELBREAD: E
ELBREAD: E

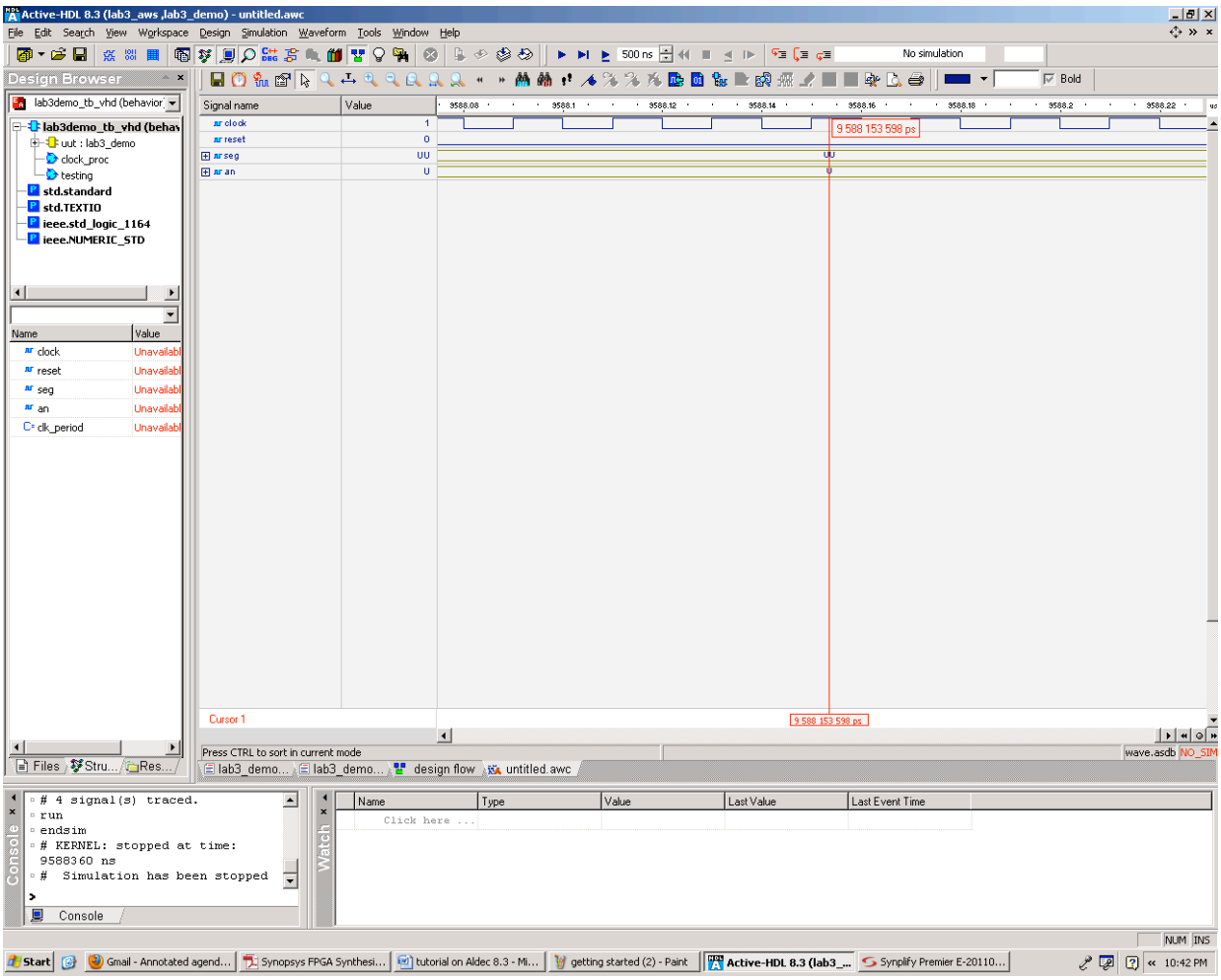
```
================================================================================
Timing constraint: Default OFFSET OUT AFTER analysis for clock "clock_c"

 34 items analyzed, 0 timing errors detected.
 Maximum allowable offset is  13.751ns.
--------------------------------------------------------------------------------
Offset:                 13.751ns (clock path + data path + uncertainty)
  Source:               counting/count_sig[0] (FF)
  Destination:          S_Seg0(3) (PAD)
  Source Clock:         clock_c rising
  Data Path Delay:      11.735ns (Levels of Logic = 3)
  Clock Path Delay:     2.016ns (Levels of Logic = 2)
  Clock Uncertainty:    0.000ns

  Clock Path: clock to counting/count_sig[0]
    Delay type         Delay(ns)  Logical Resource(s)
    -------------------------  -------------------
    Tiopi                 0.829   clock
                                  clock_ibuf/IBUFG
    net (fanout=1)        0.001   clock_ibuf/IBUFG
    Tgi0o                 0.401   clock_ibuf/BUFG
    net (fanout=19)       0.785   clock_c
    -------------------------  -------------------
    Total                 2.016ns (1.230ns logic, 0.786ns route)
                                  (61.0% logic, 39.0% route)

  Data Path: counting/count_sig[0] to S_Seg0(3)
    Delay type         Delay(ns)  Logical Resource(s)
    -------------------------  -------------------
    Tcko                  0.720   counting/count_sig[0]
    net (fanout=12)       1.641   count(0)
    Tilo                  0.608   seven_seg_0/S_1df3_i_a2_2
    net (fanout=2)        0.585   seven_seg_0/N_46
    Tilo                  0.608   seven_seg_0/N_9_i
    net (fanout=1)        2.442   N_9_i
    Tioop                 5.131   S_Seg0_obuf[3]
                                  S_Seg0(3)
    -------------------------  -------------------
    Total                11.735ns (7.067ns logic, 4.668ns route)
                                  (60.2% logic, 39.8% route)
```

Example Report: Clock period, Maximum Frequency and Critical Path.

3.2 Timing Simulation

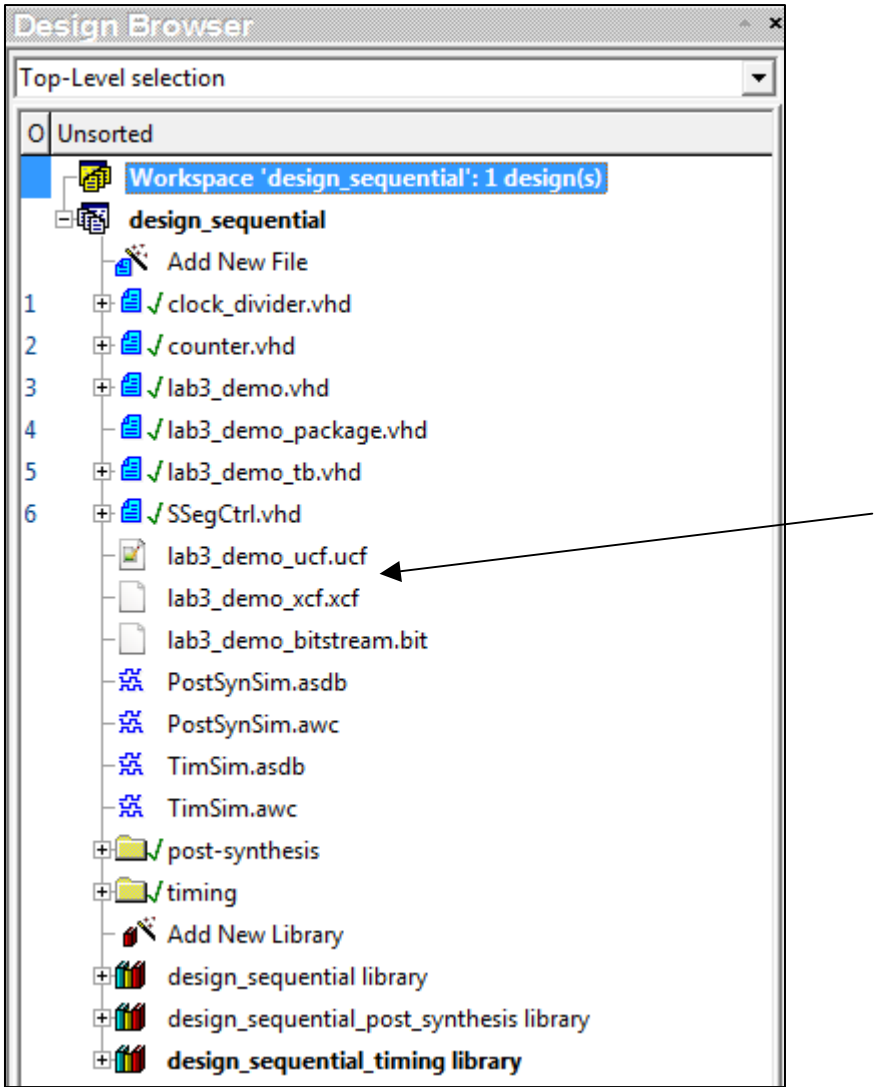


Click at the **options** button next to the **timing simulation** icon. Select your testbench as the Top-Level Unit. Afterwards, select **timing simulation**, which will generate timing waveforms based on your netlist after implementation. You should notice timing delays compared to the waveforms from your post-synthesis simulation & functional simulation.

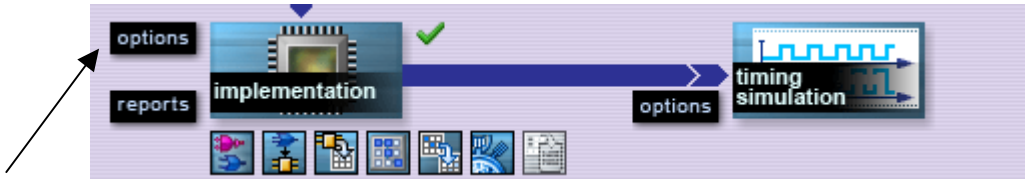


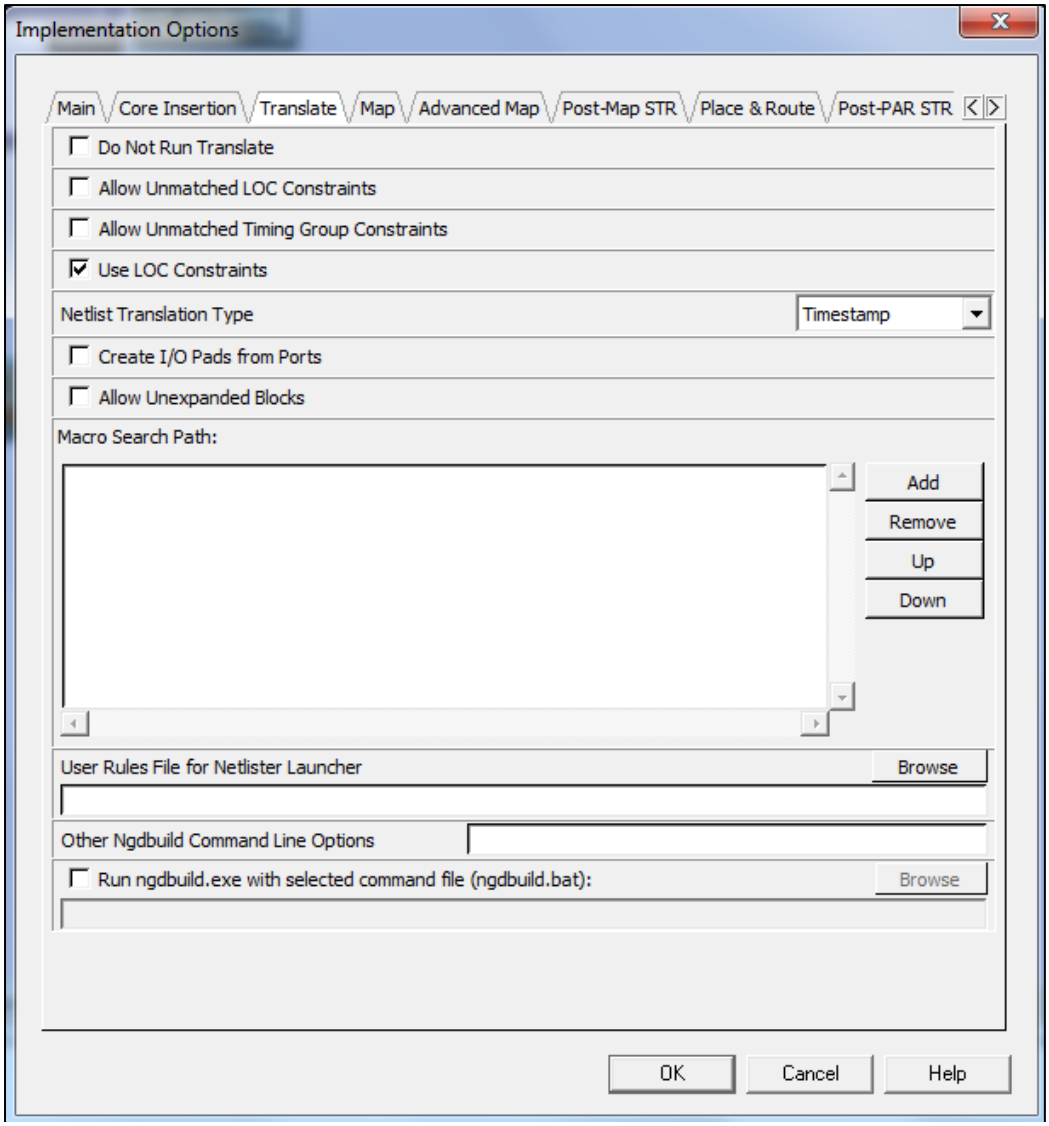
Specifying the frequency/ Time Period: Open any text editor and create two files (one with extension .xcf and the other with extension .ucf). Specify constraints regarding Synthesis in the xcf file and constraints related to Implementation in the ucf file. Edit both xcf and ucf files to specify timing constraints regarding the clock, e.g.,

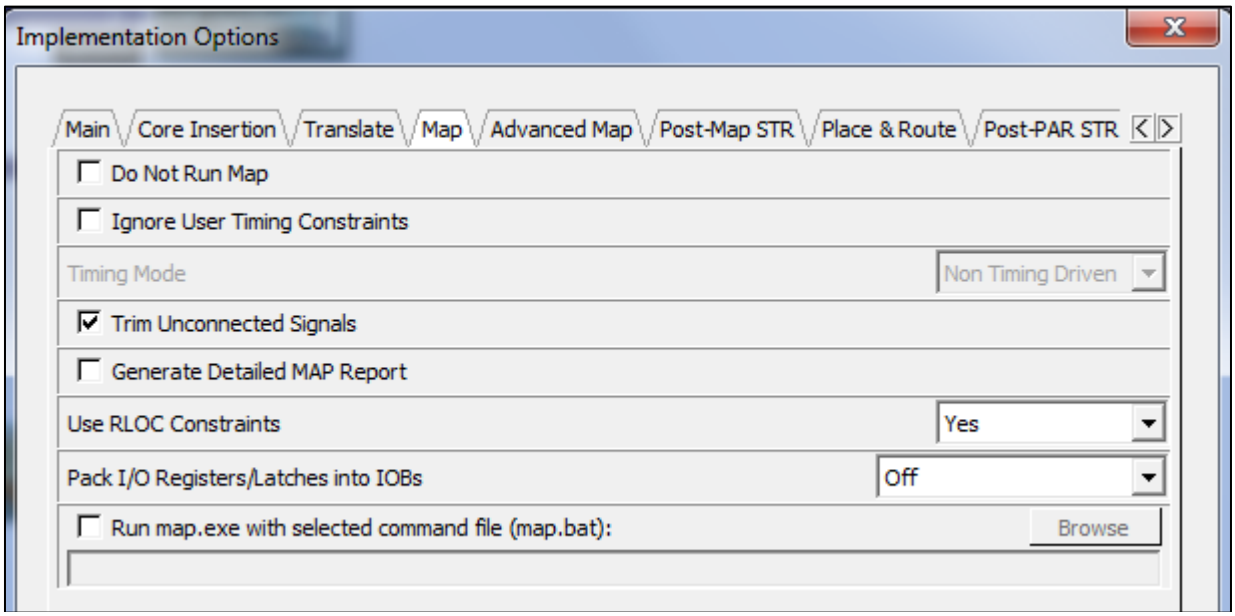
NET "clk" PERIOD = 10 ns;

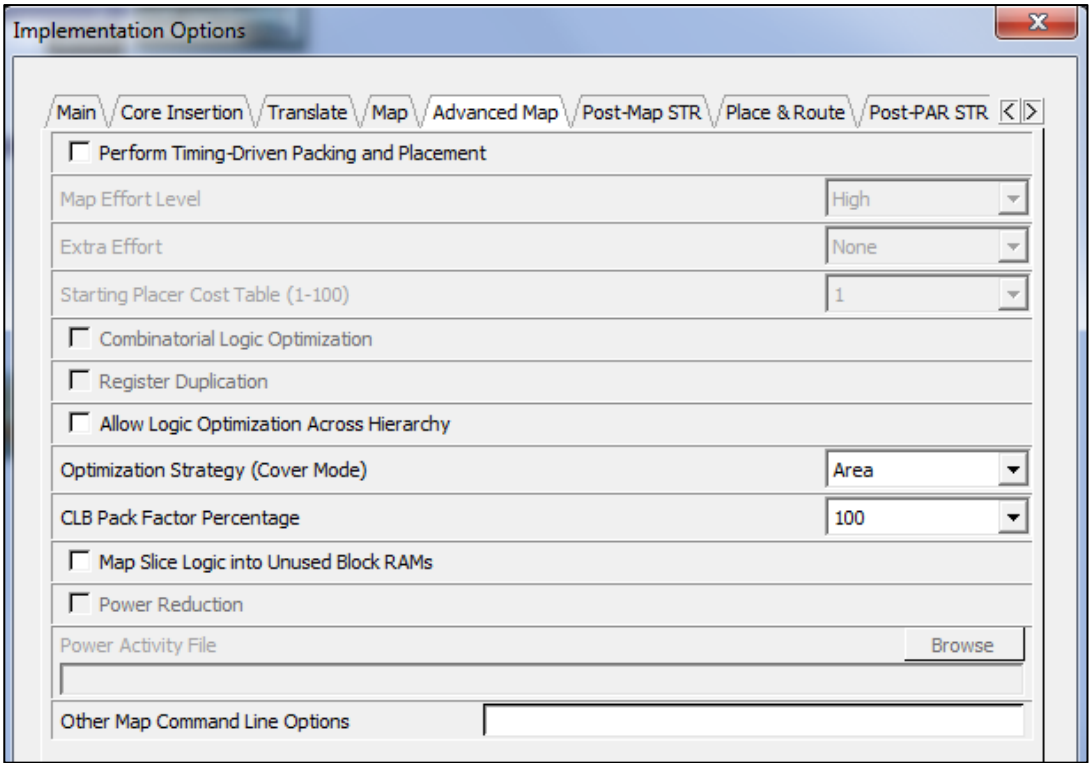


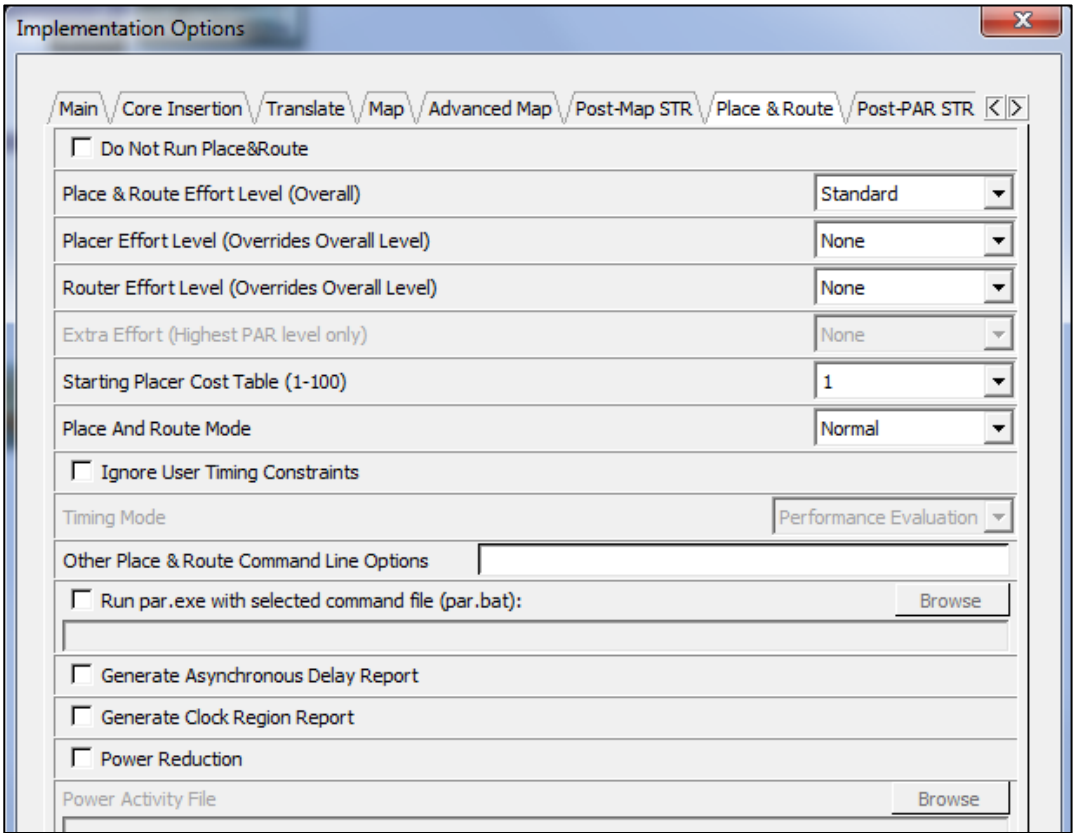
Optimization strategies: Click on the **options** icon beside implementation to select a complete list of optimization strategies (Translate, map, place & route optimizations)



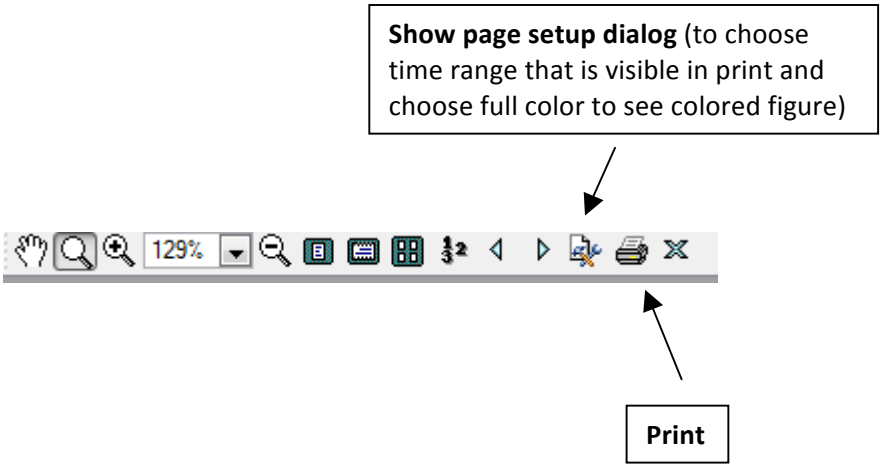

Implementation Options
Main
Core Insertion
Translate
Map
Advanced Map
Post-Map STR
Place & Route
Post-PAR STR
Do Not Run Translate
Allow Unmatched LOC Constraints
Allow Unmatched Timing Group Constraints
Use LOC Constraints
Netlist Translation Type
Timestamp
Create I/O Pads from Ports
Allow Unexpanded Blocks
Macro Search Path:
Add
Remove
Up
Down
User Rules File for Netlister Launcher
Browse
Other Ngdbuild Command Line Options
Run ngdbuild.exe with selected command file (ngdbuild.bat):
Browse
OK
Cancel
Help


Implementation Options
Main
Core Insertion
Translate
Map
Advanced Map
Post-Map STR
Place & Route
Post-PAR STR
Do Not Run Map
Ignore User Timing Constraints
Timing Mode
Non Timing Driven
Trim Unconnected Signals
Generate Detailed MAP Report
Use RLOC Constraints
Yes
Pack I/O Registers/Latches into IOBs
Off
Run map.exe with selected command file (map.bat):
Browse


Implementation Options
Main
Core Insertion
Translate
Map
Advanced Map
Post-Map STR
Place & Route
Post-PAR STR
Perform Timing-Driven Packing and Placement
Map Effort Level
High
Extra Effort
None
Starting Placer Cost Table (1-100)
1
Combinatorial Logic Optimization
Register Duplication
Allow Logic Optimization Across Hierarchy
Optimization Strategy (Cover Mode)
Area
CLB Pack Factor Percentage
100
Map Slice Logic into Unused Block RAMs
Power Reduction
Power Activity File
Browse
Other Map Command Line Options

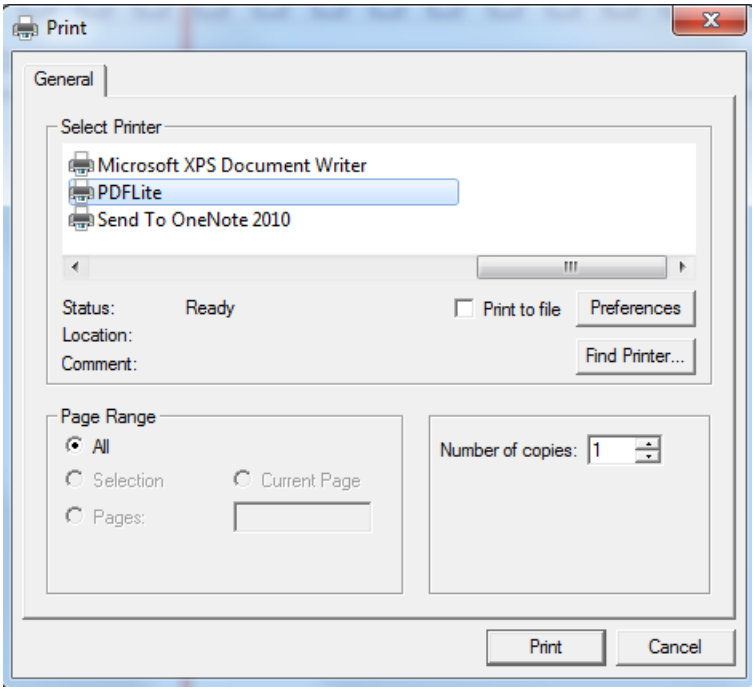

Implementation Options
Main
Core Insertion
Translate
Map
Advanced Map
Post-Map STR
Place & Route
Post-PAR STR
Do Not Run Place&Route
Place & Route Effort Level (Overall)
Standard
Placer Effort Level (Overrides Overall Level)
None
Router Effort Level (Overrides Overall Level)
None
Extra Effort (Highest PAR level only)
None
Starting Placer Cost Table (1-100)
1
Place And Route Mode
Normal
Ignore User Timing Constraints
Timing Mode
Performance Evaluation
Other Place & Route Command Line Options
Run par.exe with selected command file (par.bat):
Browse
Generate Asynchronous Delay Report
Generate Clock Region Report
Power Reduction
Power Activity File
Browse

Print the output waveform in PDF format: In order to view all the important details of the behavioral, post-synthesis, post-translate, post-map and post-place & route simulations in waveform in PDF format, use 3rd party tools (PDF creator, PDF Lite, etc). Go to file menu and click on the print preview.

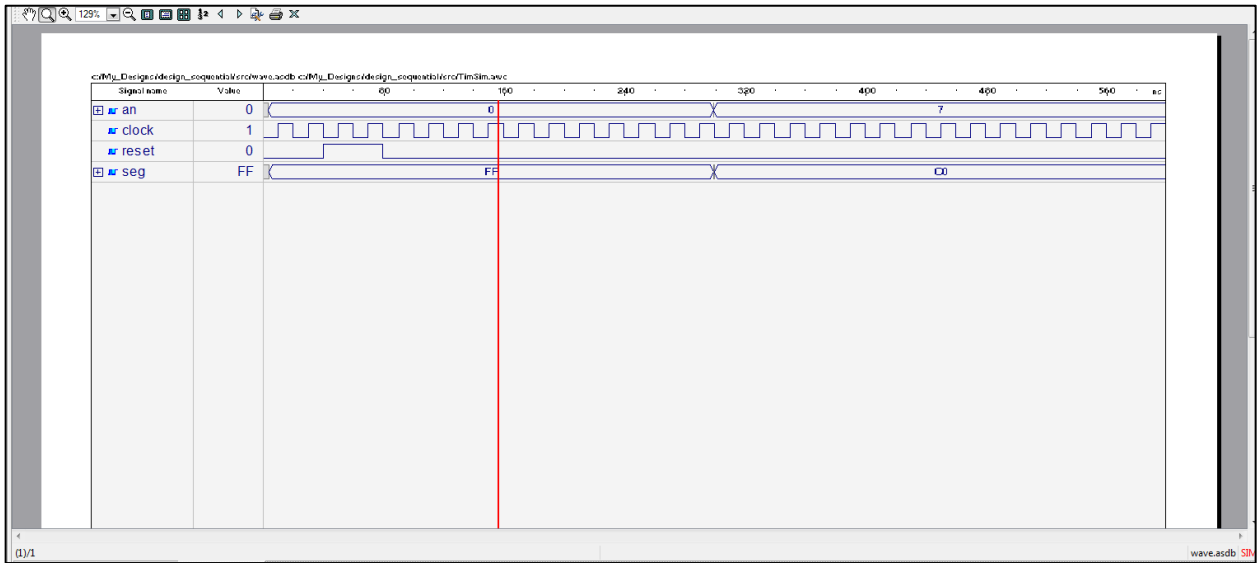


A pop up will appear when you click **Show page setup dialog** icon. It will give you the option to select time range (full range or for a specific range) and an option to have colored or black and white figure.

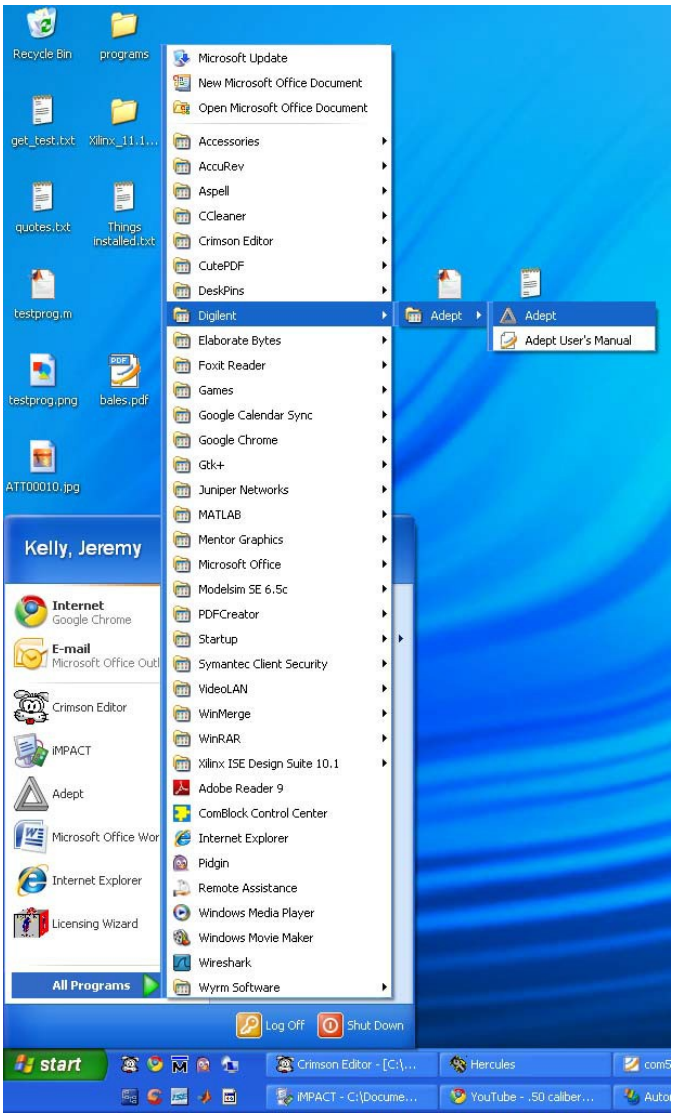
Click OK and chose PDF Lite or any other tool to do PDF conversion. After completing the print setup, a new window pops up and ask you to save the file in PDF format.



Here is the output waveform of post-translate simulation in PDF format.



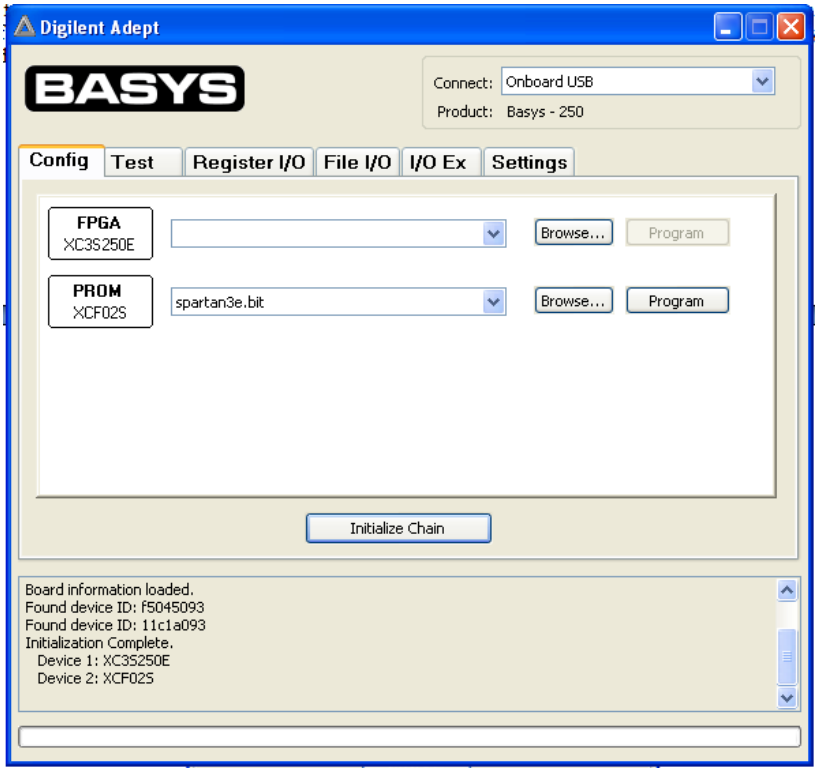
4. Uploading Bitstream to FPGA Board:



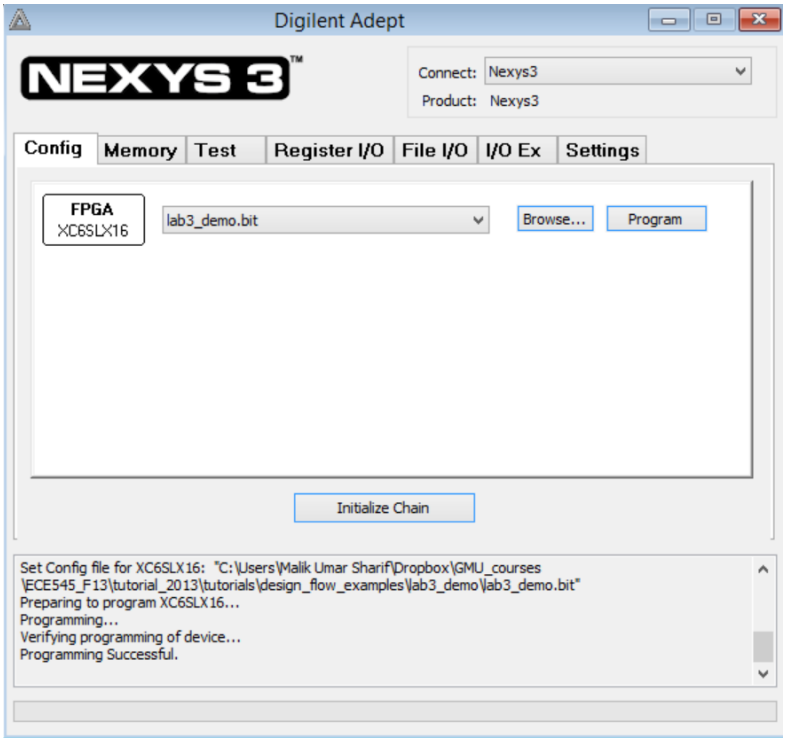
Before uploading Bit file, make sure that you change your **constant values** in all your files to proper values, and re-synthesize/re-implement all the files. In particular, in our example, please change the value of the constant slow_clock_period in the Lab3Demo_package.vhd.

Select the Adept program as shown in the picture above. When the program is opened, a device will be shown if it is connected and recognized. Select the bit file by clicking **Browse** and finding the appropriate file. Click **Program** to program the device.

a. Uploading bit stream on Basys2 board:



b. Uploading bit stream on Nexys3 board:


Digilent Adept
NEXYS 3™
Connect: Nexys3
Product: Nexys3
Config
Memory
Test
Register I/O
File I/O
I/O Ex
Settings
FPGA
XC6SLX16
lab3_demo.bit
Browse...
Program
Initialize Chain
Set Config file for XC6SLX16: "C:\Users\Malik Umar Sharif\Dropbox\GMU_courses
\ECE545_F13\tutorial_2013\tutorials\design_flow_examples\lab3_demo\lab3_demo.bit"
Preparing to program XC6SLX16...
Programming...
Verifying programming of device...
Programming Successful.