

3DFFT: Thermal Analysis of Non-Homogeneous IC using 3D FFT Green Function Method

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ABSTRACT

Due to the roaring power dissipation and gaining popularity of 3D integration, thermal dissipation has been a critical concern of modern VLSI design. The availability for chip-level 3D thermal analysis is crucial for thermal integrity analysis. In this paper, we formulated an analytical Green function solution of the 3D temperature distribution in a multi-layer integrated circuit substrate. The proposed analytical solution differs from the previously reported results in two ways: (a) This is a 3D temperature distribution solution, while only 2D solutions are reported in the past; and (b) a rectangular coordinate system is used rather than the cylindrical coordinates used in the past which leads to a more proper and accurate representation to the VLSI geometry. Experimental results demonstrate the speed advantage of our approach and the accuracy within the error 0.5% when compared with commercial computational fluid dynamics software ANSYS^[13].

Keywords

CAD, Fourier Transform, Thermal Modeling, Green's Function, Multi-layer, Simulation, 3DFFT

1. INTRODUCTION

In modern VLSI chips, clock frequency and device count are ever increasing and shrinking of nano-scale device geometry is still going on. This, in turn, will significantly increase power dissipation of the device, which produce high temperature of the device. Furthermore, 3D integration of heterogeneous ICs holds tremendous promise for SoCs. From Fig 1&2, at least 3 or 4 substrates can be integrated within one module. This integration will also lead to the huge reduction of the size of electronic system. However, this also contribute to increase temperature of the IC because each substrate of the IC will plays as the thermal barrier due to low thermal conductivity.

Nowadays, many advanced physical computer aided integrated circuit design tools have incorporated thermal-aware design methodologies to mitigate the negative

impacts due to thermal effects. The success of these thermal-aware physical CAD tools depends on the capability how accurate and efficiently it can evaluate temperature profile of 3D chip for a given power source distribution

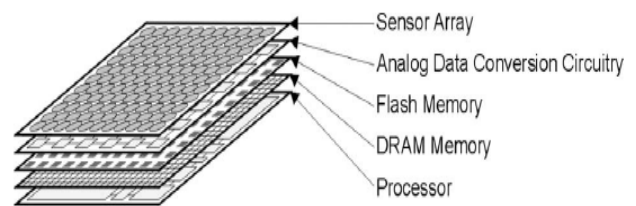


Fig 1. 3D integration of heterogeneous IC. (from [13])

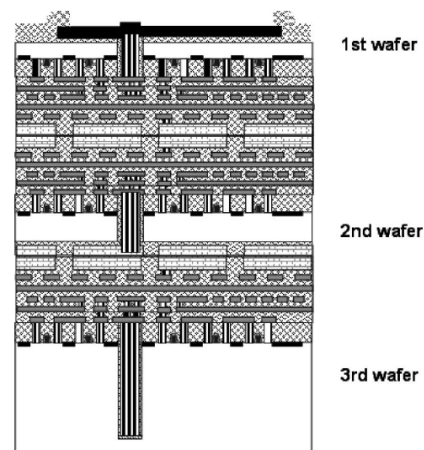


Fig2. 3D stacking of multi substrate. (from [13])

A temperature evaluation engine is often called upon numerous times during the design optimization process of thermal-aware CAD tools. As such, accuracy and speed of such a temperature distribution evaluation algorithm is of paramount importance.

Temperature evaluation of a 3D IC can be begun by solving a Poisson equation. One way to solve this equation

is to use finite element based methods such as those commercial computational fluid dynamics (CFD) simulation software packages. The analysis of temperature distribution on an inhomogeneous substrate layer using finite element method is reported in [8] and [9]. An advantage of these methods is that they may take into account heat transfer discontinuity across the heterogeneous interface. However, the computation burden is often too expensive for accurate temperature distribution simulation of giga-scale devices. This case is particularly distinct when only detailed temperature profile over a small region of the entire chip is desired.

A second approach to solve the Poisson equation based on the image method such as those reported by K.J Scott in [1], [2]. This method may also encounter computational difficulty as it requires the evaluation of an infinite summation for each layer. This excessive computation burden makes it impractical to apply this method to evaluate temperature profile of multi-layer substrate with 4 and more layers.

A solution (numerical in x-y and analytical in z direction) of green function in inhomogeneous multi-substrate has been developed by Niknejad, Gharpurey and Meyer [10] to solve the substrate coupling problem. Their approach was applied to thermal modeling by Zhan and Sapatnekar [5] who proposed a workaround to focus on top surface (2D) temperature distribution to support temperature-aware physical CAD tools such as placement and routing. However, it does not address the issue of 3D temperature distribution over inhomogeneous multi-layer substrate and uses processed data such as the heat dissipation rate of a standard cell instead of utilizing primitive data such as the interconnect size, and resistivity of the material, etc.

J.Zhao in [3] and B.Wang in [4] use fast Hankel transform of green function under cylindrical coordinates for evaluating temperature profiles in a multi-layer substrate. These solutions are semi-analytical; and would require additional efforts to solve integration of nonlinear equations. Furthermore, cylindrical coordinate system is not good for managing various geometrical structure of each circuit component. Thus, we paid attention on the solution of green function in inhomogeneous multi-substrate well verified by Gharpurey [10].

In this paper, we proposed rectangular coordinate mathematical model to simulate temperature distribution for a single circuit component like interconnect wire in 3D multi-layer substrate. This method can be utilized to simulate geometrically complicated physical structures without extra complexity overhead. Our result distinguishes itself from previously reported results in that it is a complete analytical solution for the steady state 3D temperature distribution of a multi-layer substrate IC chip. Compared to results evaluated using commercial CFD simulation tool ANSYS [13], our results differ by less than 0.3% in numerical values.

The remaining of this paper is organized as follows: In section 2, the analytical Green's function solution will be derived. In section 3, simulation result, comparison with ANSYS and discussion will be provided. We will give conclusion in section 4.

2. Green function approach for the analysis of temperature distribution

A substrate of integrated circuits has at least four and five layers, each of which has different doping material and density. Silicon substrates with different doping materials and densities have different dielectric constants. This difference incurs the crystallographic difference and becomes the main reason that each layer has different thermal conductivity. Variation in thermal conductivity causes variation of the heat flux dissipation. For instance, SiO₂ layer in SOI substrate is the insulation layer to disturb the heat flux from moving forward and make the heat dissipated from MOSFET floating within the substrate. The effect of self-heating by blocking the path of heat dissipation is well known. Interconnect wire in the circuit also dissipate power steadily, which become dominant heat source in 3D stacked microelectronic structure. In order to predict catastrophic phenomenon due to the floating heat, we need to get accurate data plot of temperature in 3D substrate.

The general heat diffusion equation under rectangular coordinates is given in [5].

$$\rho C_p \frac{\partial T(x,y,z,t)}{\partial t} = \nabla(k(x,y,z,T)\nabla T(x,y,z,t)) + g(x,y,z,t) \quad (1)$$

where T is the temperature, k is the thermal conductivity, g is the power density per volume of the source, ρ is the density of the material, and C_p is the specific heat. In case of wire interconnect of power supply, it steadily dissipate power. Therefore, for the convenience of the computation, we assume the convergence condition and the left time transient term will be zero. Equation (1) will be

$$\nabla(k(z)\nabla T(x,y,z)) = -g(x,y,z) \quad (2)$$

The thermal conductivity $k(x,y,z,t)$ is constant within a single homogenous layer. Therefore, the equation (2) will be

$$k(z)\nabla(\nabla T(x,y,z)) = -g(x,y,z) \quad (3)$$

The temperature function can also be described as the integral form

$$T(r) = -\int g(r)G(r,r')dv \quad (4)$$

$$g(x,y,z) = -\int g(r)\delta(r,r')dv \quad (5)$$

where $G(r, r')$ is the green function of the temperature and $\int dV$ is the volume of power source. Green function can be found in the converted form of the equation (3).

$$k\nabla(\nabla G(r, r')) = -\delta(r - r') \quad (6)$$

Now we find a solution of green function for the single substrate layer with the dimension of $L_x=a$, $L_y=b$, $L_z=L$.

Let's assume that $G(x, y, z, x', y', z') = X(x, x')Y(y, y')Z(z, z')$. We use rectangular coordinate instead of cylindrical coordinate. Many papers use cylindrical coordinate for the simplicity of the solution in the infinite plane. However, it also increase computational complexity and degrade the reliability of simulated data when we simulate long interconnect wire or any other complicated structure because long wire is hard to be transformed to the cylindrical coordinate. We selected rectangular coordinate to avoid such inefficiency. Thus, this variable independence results in

$$YZ \frac{d^2 X}{dx^2} + ZX \frac{d^2 Y}{dy^2} + XY \frac{d^2 Z}{dz^2} = -\frac{\delta(x-x')\delta(y-y')\delta(z-z')}{k} \quad (7)$$

Now we need to define boundary conditions in order to solve equation (6). At first, we define three boundary conditions in 3D wall.

$$(B.1) \frac{\partial X(x, x')}{\partial x} = 0 \text{ at } x = 0, a$$

$$(B.2) \frac{\partial Y(y, y')}{\partial y} = 0 \text{ at } y = 0, b$$

$$(B.3a) -k \frac{\partial Z(z, z')}{\partial z} = h(Z(z, z') - T_a) \text{ at } z = z_s$$

$$(B.3b) k \frac{\partial Z(z, z')}{\partial z} = h(Z(z, z') - T_a) \text{ and } z = z_o$$

T_a is the ambient temperature. (B.1) and (B.2) is adiabatic boundary condition to assume that the heat flux is blocked in the horizontal way. (B.3) is the convective boundary condition that heat flux can flow only in the vertical way. For the convenience of the computation, we let ambient temperature $T_a = 0$.

From (B.1) & (B.2), we get

$$X(x, x') = \left(\sum_{m=0}^{\infty} X_m(x') \cos\left(\frac{m\pi x}{a}\right) \right) \quad (8.a)$$

$$Y(y, y') = \left(\sum_{n=0}^{\infty} Y_n(y') \cos\left(\frac{n\pi y}{b}\right) \right) \quad (8.b)$$

We express $\delta(x - x')$ in terms of the Fourier cosine expansions

$$\delta(x - x') = \frac{2}{a} \sum_{m=0}^{\infty} \cos\left(\frac{m\pi x'}{a}\right) \cos\left(\frac{m\pi x}{a}\right)$$

$$\delta(y - y') = \frac{2}{b} \sum_{n=0}^{\infty} \cos\left(\frac{n\pi y'}{b}\right) \cos\left(\frac{n\pi y}{b}\right) \quad (9)$$

From (8) & (9), we derive following equation by removing some part.

$$\left(\frac{d^2 Z}{dz^2} - \left(\left(\frac{m\pi}{a} \right)^2 + \left(\frac{n\pi}{b} \right)^2 \right) Z \right) * \frac{a}{2} * \frac{b}{2} = -\frac{\delta(z - z')}{k} \quad (10)$$

Let $r = \sqrt{(m\pi/a)^2 + (n\pi/b)^2}$ and we get

$$\frac{ab}{c'} \left(\frac{d^2 Z}{dz^2} - r(m, n)^2 Z \right) = -\frac{\delta(z - z')}{k}$$

At $m \neq 0$ $n \neq 0$, $c' = 4$

At $m = 0$ $n \neq 0$ or at $m \neq 0$ $n = 0$, $c' = 2$

$$\text{At } m = 0 \text{ } n = 0, \quad d^2 Z / dz^2 = -\delta(z - z') / abk \quad (13)$$

Then we apply following four boundary condition to the equation.

$$(B.4) Z''(z') = Z'(z')$$

$$(B.5) \left. \frac{\partial Z(z, z')}{\partial z} \right|_{z=z'+\delta}^{z=z'-\delta} = \frac{-c'}{abk}$$

$$(B.6) Z_k(z_{k+1}) = Z_{k+1}(z_{k+1})$$

$$(B.7) k_k \frac{\partial Z_k(z_{k+1})}{\partial z} = k_{k+1} \frac{\partial Z_{k+1}(z_{k+1})}{\partial z} \quad \text{at } z = z_{k+1}$$

We get the solution of equation (13)

$$Z''(z, z') = A''(e^{r(z-L)} + \alpha e^{-r(z-L)}) A'(e^{r(z')} + \beta e^{-r(z')})$$

$$Z'(z, z') = A'(e^{r(z)} + \beta e^{-r(z)}) A''(e^{r(z'-L)} + \alpha e^{-r(z'-L)}) \quad (14)$$

By letting

$$B'' = \frac{k^* r + h}{k^* r - h} A'' = \alpha A'' \quad \text{at the top } z=L$$

$$B' = \frac{k^* r - h}{k^* r + h} A' = \beta A' \quad \text{at bottom } z=0 \quad (15)$$

$$A_{k+1} = \frac{(k_{k+1} + k_k)}{2k_{k+1}} A_k + \frac{(k_{k+1} - k_k)}{2k_{k+1}} B_k e^{-2r(z_{k+1}-L)}$$

$$B_{k+1} = \frac{(k_{k+1} - k_k)}{2k_{k+1}} A_k e^{2r(z_{k+1}-L)} + \frac{(k_k + k_{k+1})}{2k_{k+1}} B_k \quad (16)$$

$$A'' A' = \frac{c'}{2abk_j r (A_j'' B_j' e^{-r(L)} - A_j' B_j'' e^{r(L)})} = C_{mn} \quad (18)$$

Now we get the final solution of poisson equation.

Above power source in layer j,

$$G(x, y, z, x', y', z') =$$

$$\sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \left[C_{mn} (A_k'' e^{r(z-L)} + B_k'' e^{-r(z-L)}) (A_j' e^{r(z')} + B_j' e^{-r(z')}) \right]$$

Below power source in layer j,

$$G(x, y, z, x', y', z') =$$

$$\sum_{m=1}^{\infty} \sum_{n=1}^{\infty} \left[C_{mn} (A_k' e^{r(z)} + B_k' e^{-r(z)}) (A_j'' e^{r(z'-L)} + B_j'' e^{-r(z'-L)}) \right] \quad (19)$$

In the case that $m=n=0$, equation (19) reduces to

Above power source

$$Z_{00,k}^u(z, z') = \frac{1}{A_{00,j}^u B_{00,j}^l - A_{00,j}^l B_{00,j}^u} (A_{00,k}^u z + B_{00,k}^u) (A_{00,j}^l z' + B_{00,j}^l)$$

Below power source

$$Z_{00,k}^l(z, z') = \frac{1}{A_{00,j}^u B_{00,j}^l - A_{00,j}^l B_{00,j}^u} (A_{00,k}^l z + B_{00,k}^l) (A_{00,j}^u z' + B_{00,j}^u) \quad (20)$$

Then we can find the formula for temperature distribution by integrating (19) over 3D substrate dimension.

From [4], average temperature per volume v_i is defined as

$$\overline{T(x, y, z)}_i = -\frac{1}{V_i} \int \int \int g(r') G(r, r') dv_i dv_j \quad (21)$$

$$= -\frac{\overline{g}}{V_i V_j} \int_{x=a1}^{x=a2} \int_{y=b1}^{y=b2} \int_{z=c1}^{z=c2} \int_{x'=a3}^{x'=a4} \int_{y'=b3}^{y'=b4} \int_{z'=c3}^{z'=c4} G(x, y, z; x', y', z') dx dy dz$$

$$\overline{T(x, y, z)}_i = -\frac{\overline{g}}{V_i V_k} \times \left(\begin{array}{l} (a/m\pi)^2 (b/n\pi)^2 \times C_{mn} \times 1/r^2 \\ (\sin(m\pi \cdot a2/a) - \sin(m\pi \cdot a1/a)) \\ (\sin(m\pi \cdot a4/a) - \sin(m\pi \cdot a3/a)) \\ (\sin(n\pi \cdot b2/b) - \sin(n\pi \cdot b1/b)) \\ (\sin(n\pi \cdot b4/b) - \sin(n\pi \cdot b3/b)) \\ (A_k^u e^{r(c2-L)} - A_k^u e^{r(c1-L)} - B_k^u e^{-r(c2-L)} + B_k^u e^{-r(c1-L)}) \\ (A_j^l e^{r(c4)} - A_j^l e^{r(c3)} - B_j^l e^{-r(c4)} + B_j^l e^{-r(c3)}) \end{array} \right) \quad (32)$$

where A_k^u , the constant of the layer k above power source,

A_j^l , the constant of the layer below power source within the layer j at which power source is located.

When $m=n=0$,

$$\overline{T(x, y, z)}_{00} = -\frac{1}{a \cdot b \cdot k_j (A_{00,j}^u B_{00,j}^l - A_{00,j}^l B_{00,j}^u)} * (A_{00,k}^u (c2 + c1) / 2 + B_{00,k}^u) (A_{00,j}^l (c4 + c3) / 2 + B_{00,j}^l)$$

3. Experimental Results

We have two experimental purposes. The one is to get the data output as accurate as that from present commercial tools. Then we need to present how efficient our solver is. We are going to perform comparison experiment with that of commercial tools based on finite element method and then present running time of our solver for various number of circuit structures.

The out simulator, 3DFFT was implemented with C language and executed on a PC with a 1.4GHz Pentium 4 processor and 1GB of memory. First, consider a multilayer substrate with the size $10\text{mm} \times 10\text{mm} \times 5\text{mm}$. The substrate have 5 layers with thickness 0.5mm , 2mm , 4mm , 4.5mm , 5mm from the bottom to the top. Though wire size are a little too bigger than that in real integrated circuit, it is just used for the

convenience of accuracy comparison between our solver and ANSYS^[14]. The heat conductivity of each layer are $1, 2, 10, 2, 1$ from the bottom $[\text{W}/(\text{m} \cdot \text{K})]$ and that of copper wire interconnect is $383[\text{W}/(\text{m} \cdot \text{K})]$. An interconnect wire with the size $0.5\text{mm} \times 2\text{mm} \times 0.5\text{mm}$ is located at the coordinate of $x=5\text{mm}$, $y=4\text{mm}$, $z=3\text{mm}$. The effective heat transfer coefficient h is assumed to be $500 [\text{W}/(\text{m}^2 \cdot \text{K})]$ in bottom and top surface. The ambient temperature is assumed to be 0K that simulation plot shows only the temperature increment due to power dissipation of a source. We assume that the supply voltage is 5V and the current is 5mA . Hence, this copper interconnect wire steadily dissipate the power of 0.025W .

Fig 3 and Fig 4 shows simulation result using commercial CFD software(ANSYS) and our solver in multilayer substrate. Temperature range in ANSYS is from $2.434(\text{K})$ to $2.677(\text{K})$ and output in our simulator ranges from $2.481(\text{K})$ to $2.688(\text{K})$. The table 1 shows that output of our approach at several coordinates corresponds well to the output of commercial CFD software within the error of 0.5% .

Fig 5 shows temperature profile for the I-form placement of wire. Temperature profile on the left figure shows that our solver can represent temperature distribution by heat dissipation of multiple wires in the very sophisticated way. The plot in Fig 4 includes 20×20 nodes to represent the whole temperature distribution in the horizontal surface. Totally 40000 computations is required to produce this plot for each surface, which cost about 0.45 seconds with 25KB memory. ANSYS produces 2194 nodes, 9239 elements for this case, of which takes 52.2 seconds with 39MB. It is found that huge amount of memory will be saved in 3DFFT because it is only the computation intensive process.

The computational overhead of green function solver increases linearly by the number of the structure. The complexity of computing green function is $O(n \cdot l)$ where n is the number of node, l is the number of layers. Fig 6 shows running time for the simulation of varied circuit structures such as standard cells, interconnect wire, and etc. This simulation was performed on the condition that the substrate size is $10\text{mm} \times 10\text{mm} \times 5\text{mm}$, size of standard cells are around $0.5\text{mm} \times 0.5\text{mm} \times 0.005\text{mm}$, size of wires is $5\mu\text{m} \times 0.1\mu\text{m} \times 0.1\mu\text{m}$. It is found in the figure 6 that running time increases linearly by the number of structure. Though running time of finite element method is not critically affected by the number of wire, if the structures of small size are uniformly distributed on the whole die, software tools by finite element method should make huge number of meshes before computation, which took several dozens of minutes without relation to the number of structure. However, 3DFFT solver of green function can decrease running time proportional to the decrease of number of structure, which means we can have flexibility in running time by the tradeoff between accuracy and running time because we can reduce the number of the structure by approximation method to combine locally close structures.

4. CONCLUSION

In this paper, we presented a 3D thermal analysis method based on green function and Fourier transform. The above simulation represents that we can get highly accurate data as such as finite element method, we can simulate any forms of structure without the geometrical restriction and the running speed is much higher than finite element method. This work will be useful in determining actual heat dissipation data of any standard cell and data pile of standard cell will be able to be also utilized to construct temperature distribution of a whole substrate and then assist us to find a hot spot in any region of the substrate.

5. FURTHER WORKS

Until this moment, considering thermal coupling phenomenon of two heated wire and non-dissipating wire into 3DFFT solver is not verified yet. We assume that it may be very hard to find analytical solution considering these phenomenon and now consider using approximation method or composite approach of green function and finite element method.

6. REFERENCES

- [1] K.J.Scott, "Electrostatic Potential Green's Functions for Multi-Layered Dielectric Media", *Philips J.Res.* 45, 293-324,1990
- [2] K.J.Scott, "Practical Simulation of PRINTED CIRCUIT BOARDS and related structures," *JOHN WILEY & SONS INC.*,1994
- [3] J. Zhao et al, "Efficient Three-Dimensional Extraction Based on Static and Full-wave Layered Green's Functions", *DAC 98*, June 15-19, 1998
- [4] B. Wang, P. Mazumder, "Fast thermal analysis for VLSI circuits via semi-analytical Green's function in multi-layer materials," *Proceedings of the 2004 International Symposium on Circuits and Systems*, vol 2, pp. 409-412, May 2004.
- [5] Y. Zhan, and S. S. Sapatnekar, "Fast computation of the Temperature Distribution in VLSI Chips Using the Discrete Cosine Transform and Table Look-up," *Design Automation Conference, 2005. Proceedings of the ASP-DAC 2005. Asia and South Pacific*, vol 1, pp. 87-92, Jan. 2005
- [6] G.O. Workman, J.G. Fossum, S. Krishnan, M.M. Pelella, "Physical modeling of temperature dependences of SOI CMOS devices and circuits including self-heating," *IEEE Transactions on Electron Devices*, vol 45, no 1, pp.125-133, Jan 1998.
- [7] Y.K. Cheng, P. Raha, Chin-Chi Teng, Elyse Rosenbaum, and Sung-Mo Kang. "Illiads-t: An electrothermal timing simulator for temperature-sensitive reliability diagnosis of CMOS VLSI chips", *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol 17, no.8 , pp. 668-681,Aug 1998.
- [8] T.T. Wang, Y.M. Lee, and C. C. P. Chen, "3D Thermal ADI- An Efficient Chip-Level Transient Thermal Simulator," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol 21, 12, pp. 1434-1445, Dec 2002.
- [9] S. Rzepka, K. Banerjee, E. Meusel, and C. Hu, "Characterization of Self-Heating in Advanced VLSI Interconnect Lines Based on Thermal Finite Element Simulation," *IEEE Trans. Components, Packaging, and Manufacturing Technology, Part A*, vol. 21, pp. 406-411 Sept 1998.
- [10] A.M. Niknejad, R. Gharpurey, R.G. Meyer, "Numerically stable Green function for modeling and analysis of substrate coupling in integrated circuits," *IEEE Trans on Computer-Aided Design of Integrated Circuits and Systems*, vol 17, 4, pp.305-315, April 1998.

- [11] J. X. An, S.P. Sinha, A. Wei, M. M. Pelella, and N. J. Kepler, "SOI device and technology: modeling, characterization, and simulations", *Proceedings. 6th International Conference on Solid-State and Integrated-Circuit Technology*, vol 1, 22- 25, pp 643 – 649, Oct. 2001.
- [12] DEAN G.DUFFY, "Green's Functions with Applications," CHAPMAN & HALL/CRC, 2001
- [13] Robert S. Patti, "Three-Dimensional Integrated Circuits and the Future of System-on-Chip Designs", *Proc. of the IEEE*, vol.94, No. 6, June 2006
- [14] ANSYS 10.0 <http://www.ansys.com/>
- [15] MATHCAD 12.0 <http://www.mathsoft.com/>

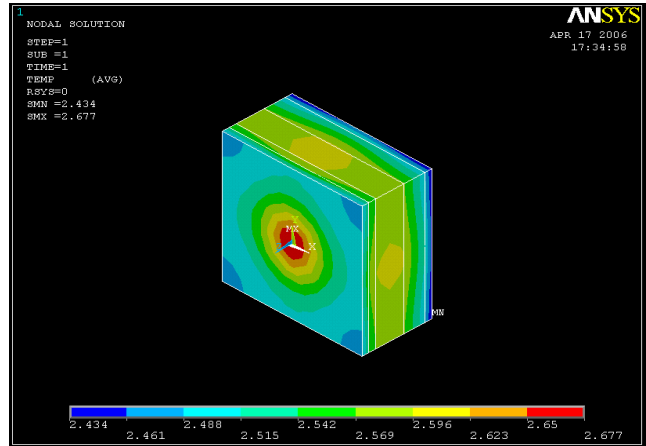


Fig 3. Temperature plot using ANSYS

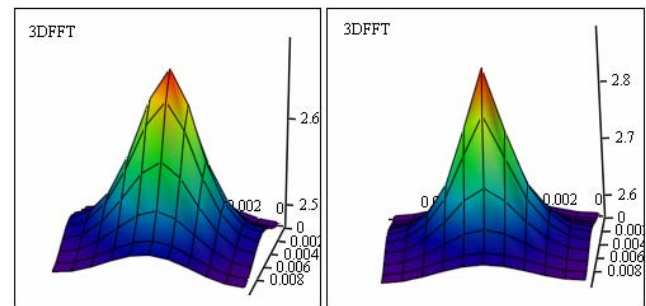


Fig 4. Temperature distribution of layers with conductivity $k=1,2,10,2,1$ (left) at top surface (right) at $z=3.5\text{mm}$ just above power source.

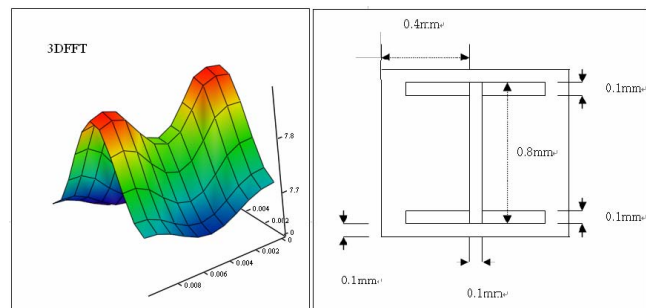


Figure 5. Temperature Distribution of T-form wire interconnect. (One vertical wire lies beyond two horizontal wire around the middle of the substrate.)

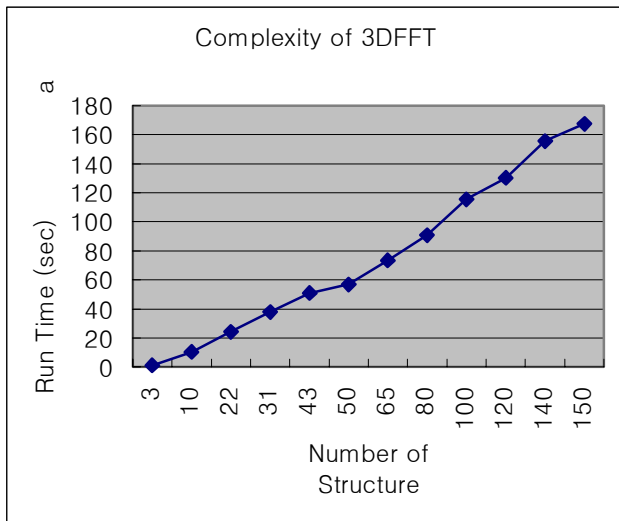


Fig 6. Increase of running time vs number of structure

Table 1. Accuracy comparison of outputs from 3DFFT and ANSYS at top surface

X[m]	Y[m]	ANSYS	3DFFT	Error(%)

1.04E-03	4.39E-03	2.5137	2.513	0.027847
2.01E-03	4.11E-03	2.5356	2.534	0.063101
3.08E-03	4.72E-03	2.5887	2.587	0.06567
4.07E-03	4.70E-03	2.6458	2.65	-0.15874
5.09E-03	4.62E-03	2.6733	2.683	-0.36285
6.01E-03	4.93E-03	2.6413	2.65	-0.32938
7.09E-03	4.68E-03	2.5784	2.58	-0.06205
8.25E-03	5.03E-03	2.5297	2.532	-0.09092
9.05E-03	4.55E-03	2.5129	2.513	-0.00398
1.00E-02	4.00E-03	2.5039	2.51	-0.24362

Table 2. Comparison of ANSYS and 3DFFT in running condition

	ANSYS	3DFFT
Running time	52.2(s)	0.71(s)
Memory usage	39.625MB	25KB