

A Fast and Flexible Thermal Simulation Tool Validated on Smart Power Devices

B. Desoete, P. Vanmeerbeek, P. Moens, and R. Gillon

AMI Semiconductor Belgium BVBA, Oudenaarde, Belgium

Abstract

In this paper we demonstrate a temperature simulation tool developed in Matlab, which is able to predict the temperature distribution on a full chip as a function of time. The tool allows to take into account any number of power sources with an arbitrary power waveform. The results have been verified versus commercial software and versus measurements on silicon, directly by probing integrated temperature sensors, and indirectly by measuring the DMOS self-heating effect. The tool allows the designer or system architect to assess hot spot effects on floorplan level in a faster and more flexible way than with expensive commercial software.

Introduction

Thermal effects are known to become more and more a limiting factor in smart power technologies [1-2]. Indeed, high local temperatures can occur in dynamic operation, which may degrade the lifetime of the devices significantly, or affect neighbouring circuitry adversely. These high internal temperatures are caused by the combination of a high ambient temperature, typical for automotive applications, and a high local temperature rise, due to the high power density levels which can reach values of the order of several kW/mm².

In order to enable system architects and designers to quantify in an early phase local temperatures during dynamic operation, we have developed a simulation tool in Matlab, which is based on analytical equations. The tool is able to calculate temperature distributions on floorplan level as a function of time with good accuracy. The added value lies in the fact that very fast temperature simulations can be performed compared to dedicated numerical software. In addition the tool allows to evaluate the temperature rise for different circuit bias conditions and device lay-outs in a very flexible way.

The simulations have been validated in three ways. First, the results have been compared to the ones from commercial software tools. Second, measurements on integrated temperature sensing diodes have been performed and compared to simulations. Third, pulsed measurements on DMOS devices have been performed in order to indirectly probe device temperature increase through the temperature dependence of electron mobility. Fourth, measurements on product level have been confirmed by the simulation tool.

Description of simulation tool

The thermal simulation tool is based on the Green's function solution of the heat diffusion equation for a homogeneous rectangular power source, with the assumption of an adiabatic top surface, while the other surfaces are assumed to be at an infinite distance from the power source [3]:

$$\Delta T(x, y, z, t) = \frac{\sqrt{\alpha}}{4kWL\sqrt{\pi}} \int_{t'=0}^t \left[\operatorname{erf}\left(\frac{W/2+x}{\sqrt{4\alpha(t-t')}}\right) + \operatorname{erf}\left(\frac{W/2-x}{\sqrt{4\alpha(t-t')}}\right) \right] \cdot \left[\operatorname{erf}\left(\frac{L/2+y}{\sqrt{4\alpha(t-t')}}\right) + \operatorname{erf}\left(\frac{L/2-y}{\sqrt{4\alpha(t-t')}}\right) \right] \cdot \frac{1}{\sqrt{t-t'}} \cdot \exp\left(-\frac{z^2}{4\alpha(t-t')}\right) \cdot P(t') \cdot dt',$$

where W and L are the dimensions of the power source, $P(t)$ is the power dissipation as a function of time, and k and α are the thermal conductivity and diffusivity respectively. The solution assumes a constant k , although in reality its value in silicon is dependent on temperature.

This solution is valid for power sources sufficiently far from the die edges, compared to a corresponding thermal diffusion length. However, in order to extend the validity of the model, adiabatic die edges need to be taken into account using the method of images [4], as illustrated in Fig. 1. In order to properly limit the number of power sources to include in the calculation, a thermal boundary is defined which is determined by a typical thermal diffusion length.

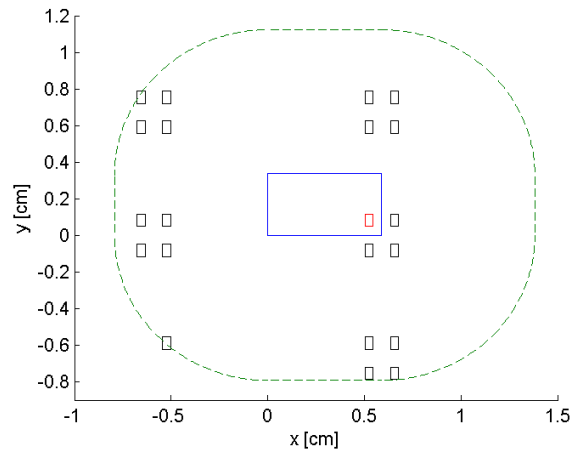


Fig. 1: Boundaries and structures used inside analytical thermal simulation tool (blue: die; red: power source; green: thermal diffusion boundary; black: image sources inside boundary). For this example the thermal diffusion boundary corresponds to $t = 100$ ms.

A graphical user interface has been developed around the tool, as can be seen on Fig. 2. Different panels allow to define the die size, any number of rectangular power sources, any number of sensor points, and the simulation specifications. The power sources can be defined as periodic pulse waveforms or as piecewise linear waveforms, or alternatively can be read in from a file. The user can choose between temperature distributions as a function of position for certain times, or temperature evolutions as a function of time for the different sensor points.

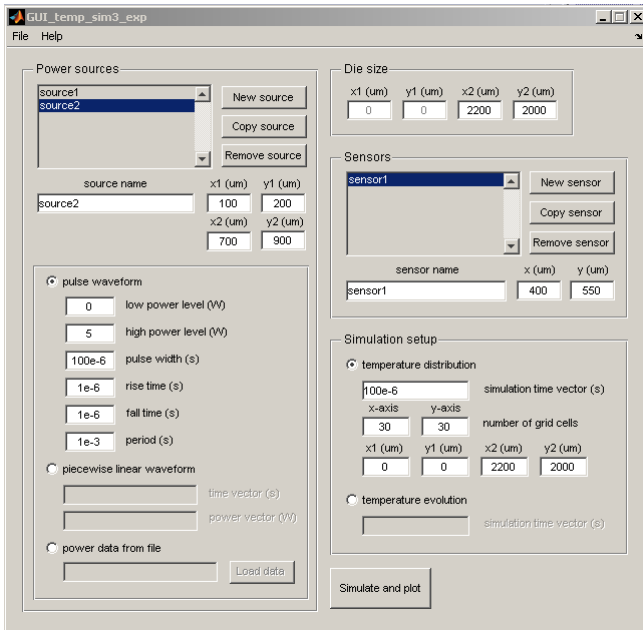


Fig. 2: Graphical user interface of thermal simulation tool developed in Matlab. Different panels allow to define die size, power sources, sensors, and simulation specifications.

As an example, Fig. 3 shows the temperature distribution for the PNPB application, as simulated for system architects, 0.9 ms after application of a triangular power pulse to each of the 8 drivers (worst-case condition). The power pulse and the central driver temperature as a function of time are shown in Fig. 4. This simulation allowed to estimate the peak temperature to be about 100 degrees higher than ambient temperature, and also showed that the thermal shut-down circuit, located in the center of the die, would not be able to sense the hot spots because of the short pulse duration. Simulations showed that the shut-down circuit would see a maximum temperature increase of only 6 degrees after about 7 ms.

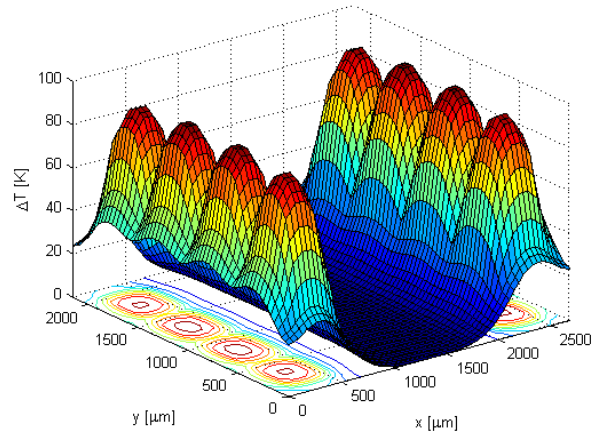


Fig. 3: Temperature increase after 0.9 ms at the surface of a die containing 8 power sources, as predicted by the thermal simulation tool. The power waveform as a function of time can be seen on Fig. 4.

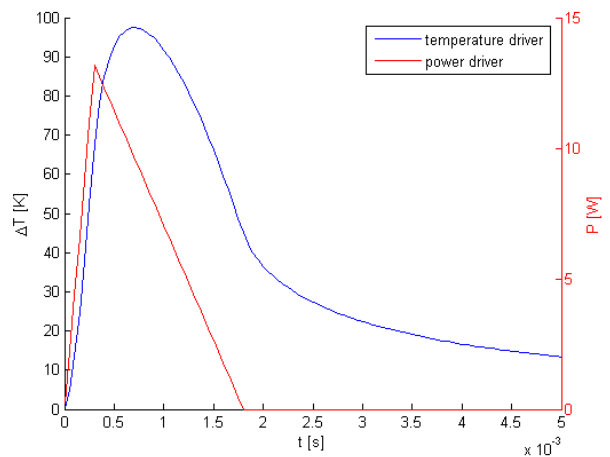


Fig. 4: Power and temperature increase as a function of time in the center of the second driver, which is shown in Fig. 3.

The simulation time of the Matlab tool is shown in Fig. 5 for the configuration shown in Fig. 3, where a grid of about 1000 points was chosen. The increase in simulation time is caused by the growing number of mirror sources that need to be taken into account for larger transient times. Although the speed of the simulation tool is already very satisfactory, it is possible to further improve the speed with about a factor 60 by implementing simplified formulae based on an approximation of the mathematical error function by a piecewise linear function [3]. Fig. 6 shows that this approximation introduces errors of only about 5%.

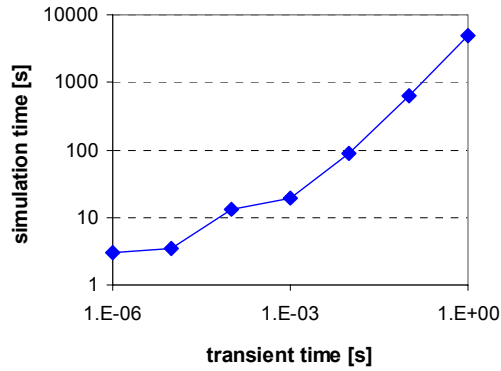


Fig. 5: Matlab simulation time as a function of transient time for the configuration shown in Fig. 3.

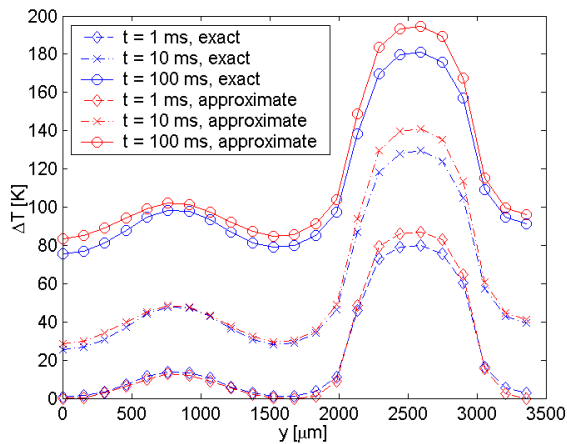


Fig. 6: Comparison of exact and approximate solution of analytical thermal simulation tool for a typical application with two power sources.

Validation against commercial software

The analytical thermal simulation tool has been validated against results from commercial simulators based on the finite-element method. Fig. 7 shows the temperature increase in a cross-section of a multi-finger DMOS driver, as simulated by the commercial simulator MSC.Marc. The hot spots at the drains can clearly be distinguished. Fig. 8 shows the results from the analytical tool, where the power sources also have been defined to be concentrated in the drain regions. A good agreement is obtained for the case of a thin copper layer, as could be anticipated from the adiabatic boundary assumption. Also shown on Fig. 8 is the approximate solution where the power is assumed to be uniformly distributed over the driver area. This approximation is generally good enough and will be adopted for simulations on floorplan level.

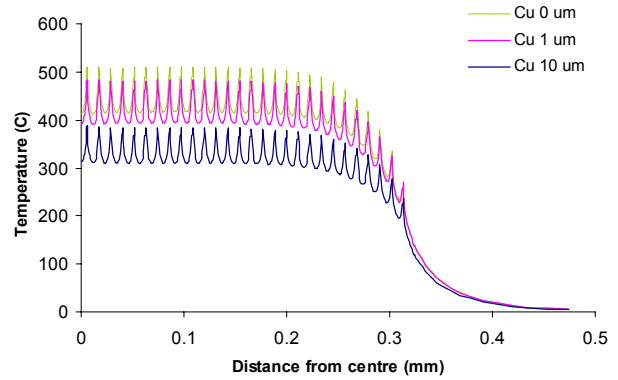


Fig. 7: Temperature increase after 50 μ s in a cross-section through the center of a DMOS device, as predicted by the numerical thermal simulation tool MSC.Marc. The device under study has a geometry of 608 by 616 μ m and consists of 56 parallel channels. The power as a function of time has a triangular shape with a sharp peak of 400 W at the start, ramping down to zero in 100 μ s, representing the switching of an inductive load, and is assumed to be generated homogeneously inside the drain regions. Three different thickness values for the copper top metal have been used.

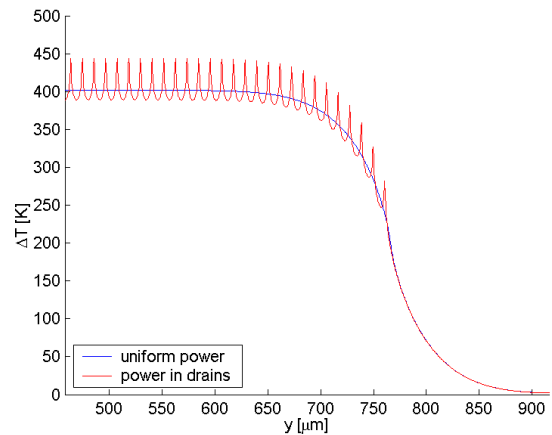


Fig. 8: Temperature increase after 50 μ s in a cross-section through the center of a DMOS device, as predicted by the analytical thermal simulation tool, for the same inputs as in Fig. 7. Both a simulation with concentrated power sources in the drain regions, and a simulation with a uniform power distribution, have been performed.

In order to validate the results from the tool on a larger time scale, a comparison has been made with results from the commercial simulator Flotherm, which takes into account the complete package of the device. Fig. 9 and Fig. 10 show a comparison between both simulations, with temperature on a linear and a logarithmic scale respectively. For times smaller than about 100 ms the temperature is slightly overestimated by the Matlab tool. For very small times this can be attributed to the fact that the numerical software is using grid cells with a finite thickness, in contrast to the analytical software which assumes the power sources to be infinitely thin. For larger times this overestimation can be linked to the fact that in the Matlab tool the thermal conductivity k has been chosen to be 1 W/(K.cm), a value which is higher than the value at room temperature.

For times larger than about 100 ms the influence of the package starts to play a role, leading first to an underestimation by the Matlab tool until about 10 s, and to a failure to predict the temperature saturation for times larger

than about 10 s. We can conclude that there is a quite good correspondence up to about 10 s, proving the validity of the analytical model for diffusion lengths significantly larger than the die dimensions.

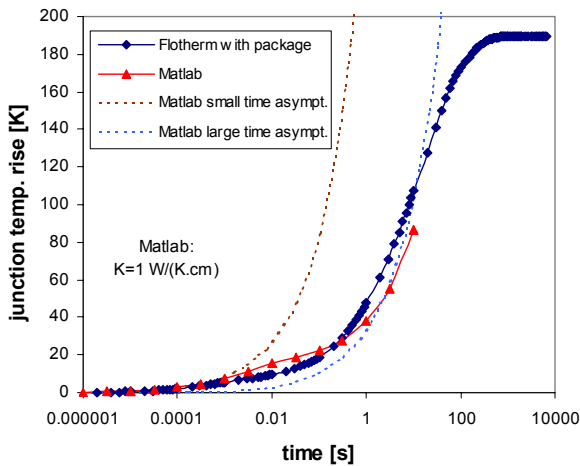


Fig. 9: Temperature increase as a function of time at the central point of a DMOS driver, located at the edge of a die, as simulated by the commercial tool Flotherm and the Matlab tool, for a power step function of 2 W (linear y-axis scale). Also shown are the theoretical asymptotes for small and large times in the Matlab tool.

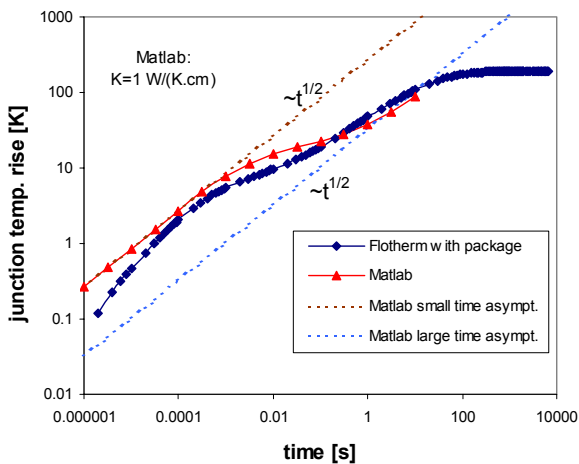


Fig. 10: Temperature increase as a function of time at the central point of a DMOS driver, located at the edge of a die, as simulated by the commercial tool Flotherm and the Matlab tool, for a power step function of 2 W (logarithmic y-axis scale). Also shown are the theoretical asymptotes for small and large times in the Matlab tool.

Validation using integrated temperature sensors

In order to be able to directly measure the local temperature in a transient condition, dedicated DMOS drivers with integrated temperature sensing diodes have been designed and laid out in AMIS' I3T50 technology. Diodes have been placed both inside and outside the large vertical DMOS devices. A constant forward current of 100 μA is forced through the diodes, so that the measured voltage drop is linearly dependent on the absolute temperature. The diodes have been calibrated until 300 $^{\circ}\text{C}$.

Fig. 11 shows a comparison between simulated and measured temperature increase along a cutline through the

center of a device with an aspect ratio of 3.4, across the device channels, for a power pulse of 22 W until 2 ms. Outside the driver there is a perfect correspondence between simulations and measurements. Inside the driver the correspondence is very good towards the end of the pulse, but for smaller times the simulations seem to overestimate the temperature. This is caused partly by the fact that the sensors are not located exactly at the same place as the power sources, but may also be linked to the fact that shortly after application of the pulse, part of the heat is stored in the metal lines on top of the driver. This needs to be investigated further.

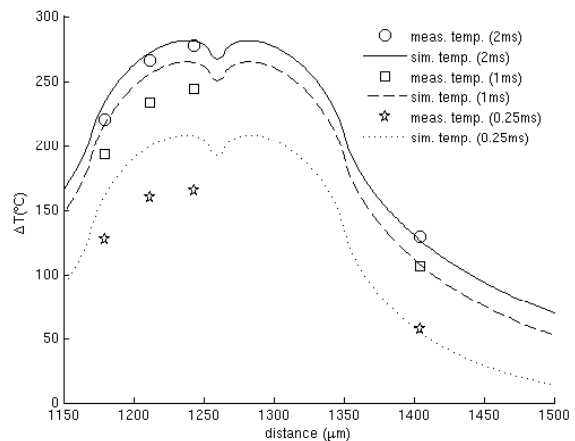


Fig. 11: Temperature increase along a cutline through the center of the device across the device channels, for a power pulse of 22 W. Lines represent simulations, while symbols represent measurements by diode sensors. Three internal diodes and one external diode are shown. The central dip in the simulated temperature distribution is caused by the presence of a relatively large drain contact.

Validation on transistor level

The simulation tool has also been validated against pulsed measurements on DMOS devices. Two different measurement set-ups have been used for this purpose. The first set-up can withstand moderate power levels and is typically used to characterise medium sized devices. A square signal is applied to the gate, while the drain current is measured by probing the voltage over a variable resistor [5].

Fig. 12 shows typical DMOS output characteristics for different pulse widths. The decrease in drain current for a specified bias condition is assumed to be mainly determined by the decrease in electron mobility as a function of temperature, expressed by $I_D/I_{D0} = (T/T_0)^{-k}$, where k has been determined by performing measurements at varying ambient temperatures. Fig. 13 shows a comparison between the results from the analytical model and the results obtained with the described method, for two different device geometries. A very good agreement is observed.

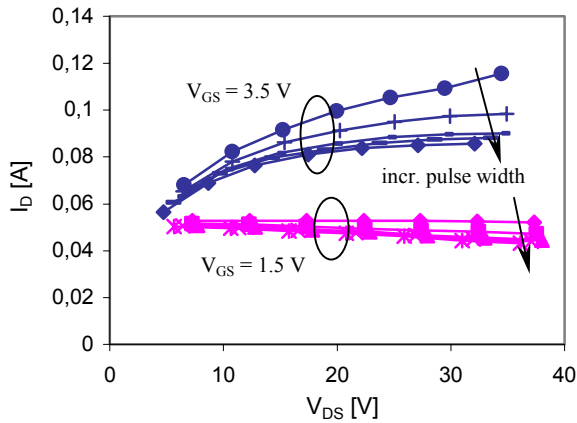


Fig. 12: Pulsed drain current measurements of an I3T80 VDMOS device with 8 parallel channels of 80 μm width. The applied pulse widths are 1, 10, 50, 100, and 200 μs .

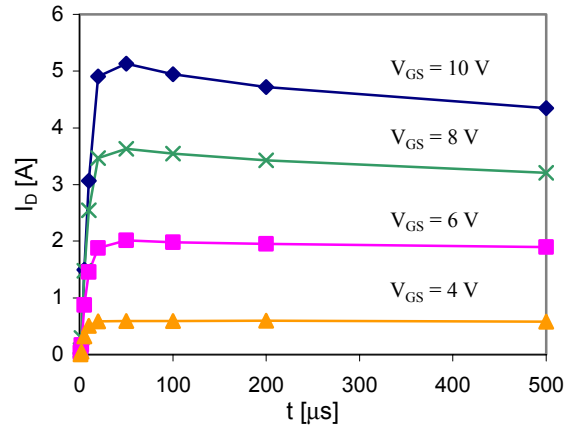


Fig. 14: Pulsed measurements with energy capability set-up of drain current as a function of time, for a square I2T100 LDMOS device with a size of 450 μm at $V_{\text{DS}} = 10\text{ V}$.

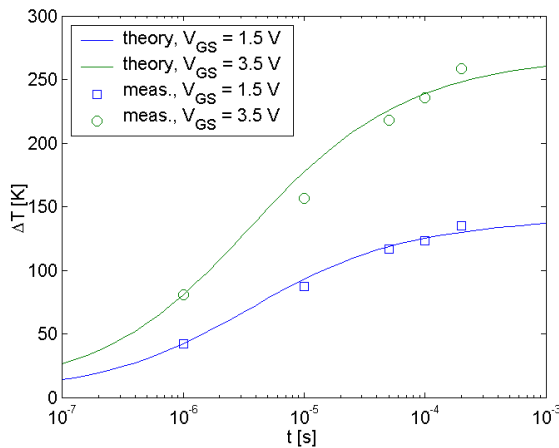


Fig. 13: Temperature increase as a function of time at the central point of an I3T80 VDMOS device with 8 parallel channels of 80 μm width, as simulated by the analytical thermal simulation tool (full lines). The measured drain currents at $V_{\text{DS}} = 30\text{ V}$, as shown in Fig. 7, have been used to predict corresponding temperature increases (symbols). The reference temperature at 1 μs has been chosen to be the same as simulated by the analytical model.

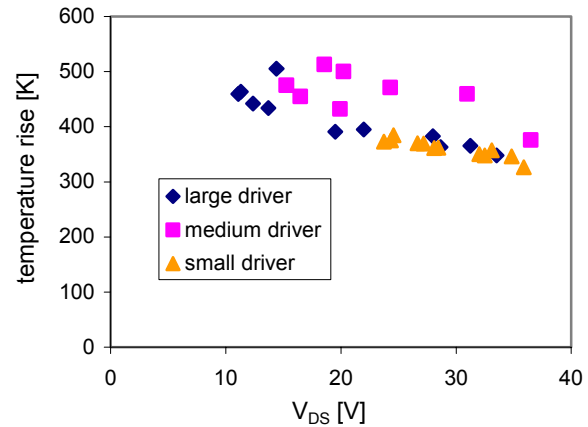


Fig. 15: Temperature increase at failure, as predicted by the analytical thermal simulation tool, for three different square I2T100 LDMOS devices (with sizes equal to 115, 230, and 450 μm), as a function of V_{DS} . Each point corresponds to a particular bias condition and power, which, together with the time to failure, serve as inputs to calculate the corresponding temperature increase.

The second set-up can withstand higher power levels and is used for energy capability measurements. Fig. 14 shows typical DMOS drain current measurements as a function of time. For three different square drivers, processed in AMIS' I2T100 technology, and for a set of bias conditions, energy capability measurements have been performed. The power and time to failure serve as an input to the analytical model. Fig. 15 shows the resulting temperature prediction as a function of drain voltage. For a large range of input powers and pulse widths, a temperature increase at failure between 400 and 500 K is obtained, confirmed by TCAD simulations. The lower values for higher drain voltages can be explained by the occurrence of impact-ionisation, i.e. a combination of thermal and electrical failure.

Validation on product level

The thermal simulation tool has already been used several times to predict the temperature increase in transient conditions on product level. For the OCPEX product, designed in AMIS' I2T00 technology, we were able to cross-check our predictions with measurements. The product contains a large driver with several thermal shut-down circuits located very close to it. In bench tests at 85 $^{\circ}\text{C}$ ambient temperature, one of these sensors was found to turn off the driver after 5 ms. These sensors were supposed to trip at 165 $^{\circ}\text{C}$.

Fig. 16 and Fig. 17 show the temperature increase in the driver and at the temperature sensor, as a function of time and place respectively. The simulations show that after 5 ms the sensor temperature has increased by 80 $^{\circ}\text{C}$, which is in perfect agreement with the observed behaviour. Remark also that the internal driver temperature at shut-down is around 300 $^{\circ}\text{C}$, which is still low enough to prevent device failure, as can be seen on Fig. 15, although the situation is marginal. Measurements confirmed that the circuit was still functional

after shut-down.

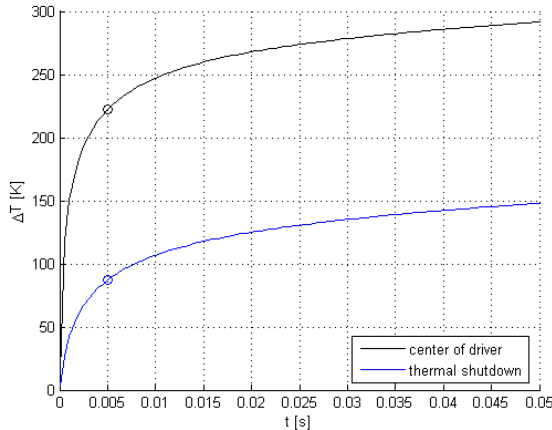


Fig. 16: Simulated temperature increase in the OCPEX product, both in the center of the driver and at the hottest thermal shut-down circuit, for a driver power of 30 W. The circles indicate the temperature at the moment of shut-down.

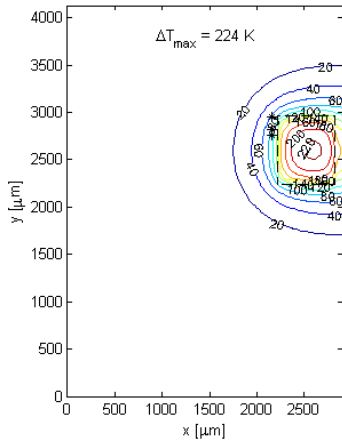


Fig. 17: Simulated temperature increase in the OCPEX product after 5 ms, for a driver power of 30 W. The driver is indicated by a dashed rectangle, while the thermal shut-down circuits are indicated by asterisks.

Conclusion

In this paper we have demonstrated a thermal simulation tool based on analytical equations. The tool is able to calculate temperature distributions as a function of time for any number of power sources on floorplan level, and serves as a fast and flexible aid to system architects and circuit designers. The tool has been validated against commercial software. Its results have been verified on silicon using integrated temperature sensing diodes. Pulsed measurements on DMOS transistors have indirectly proven its correctness, and finally also on product level the results have been cross-checked.

Acknowledgements

This work has been performed in the frame of the Compose project (Characterisation, optimisation and modelling of integrated power semiconductor devices), funded by the Flemish government. The authors also wish to thank J. Meersman for his valuable contributions.

References

- (1) P. Hower, C-Y. Tsai, S. Merchant, T. Efland, S. Pendharkar, R. Steinhoff, and J. Brodsky, "Avalanche-induced Thermal Instability in Ldmos Transistors," in *Proc. of the ISPSD Symp.*, 2001, pp. 153-156.
- (2) V. Khemka, V. Parthasarathy, R. Zhu, A. Bose, and T. Roggenbauer, "Detection and Optimization of Temperature Distribution Across Large-Area Power MOSFETs to Improve Energy Capability," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 1025-1032, June 2004.
- (3) N. Rinaldi, "On the Modeling of the Transient Thermal Behavior of Semiconductor Devices," *IEEE Trans. Electron Devices*, vol. 48, no. 12, pp. 2796-2802, Dec. 2001.
- (4) N. Rinaldi, "Generalized Image Method With Application to the Thermal Modeling of Power Devices and Circuits," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 679-686, April 2002.
- (5) C. Anghel, A.M. Ionescu, N. Hefyene, and R. Gillon, "Self-Heating Characterization and Extraction Method for Thermal Resistance and Capacitance in High Voltage MOSFETs," in *Proc. of the ESSDERC Conf.*, 2003, pp. 449-452.