Novel 3D Electro-Thermal Robustness Optimization Approach of Super Junction Power MOSFETs under Unclamped Inductive Switching

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Abstract

This paper presents a novel approach to optimize the electro-thermal robustness of a super-junction power MOSFET under unclamped inductive switching (UIS) conditions. The loosely coupled electro-thermal simulation has been used to predict accurately the interaction between the core active device and the termination rings. The simulation results have been validated by the emission microscopy (EMMI) measurements and the transient IR thermography photos.

Keywords

Super-junction Power MOSFET, UIS, electro-thermal robustness.

1. Introduction

Power MOSFET failure due to unclamped inductive switching (UIS) conditions is one of the most prevalent failure modes encountered. The ruggedness, which characterizes the device capability to handle high avalanche currents during the applied stress, is a critical criterion for many applications. In the avalanche regime and during the UIS event, the power MOSFETs generates considerable amount of heat because of huge dissipation of electrical power. In addition to that, the breakdown voltage depends strongly on the junction temperature. Therefore the electro-thermal simulation is necessary to assess the electrical as well as the thermal behavior of the power MOSFETs

The super junction transistor presented in this paper, uses a principle of the local charge balance and is a non-planar structure [1]. Referring to experimental data and TCAD simulations during the UIS pulse [2,3], the avalanche current in the core device flows deeper in the structure, while the avalanche current in the termination rings is located at the top surface. Therefore also the heat dissipation is located at different depth in the silicon which is very specific for this type of power MOSFET and which imposes clear limitations for traditional 1D/2D based finite element analysis and compact thermal models.

In previous works, several approaches of electro-thermal simulations have been presented for power MOSFET. In [4-6] 1D/2D electro-thermal simulation methods were reported to successfully describe the thermal behavior of the power devices. However those 2D methods are not suitable for the type of the power MOSFET (heat sources located at different depth in the silicon) studied in this work, for which the third dimension is vital to simulate. In [7] a power MOSFET equivalent circuit for the transient thermal impedance is reported for compact modeling purposes. This type of device modeling is relatively simple and offers a solution that can be used in commercial simulators. However this compact type of electro-thermal model does not provide useful information about the device design level. Moreover, for the power MOSFET in avalanche regime (this work), it must be ensured that the maximum permissible junction temperature is not exceeded, which is impossible to solve by conventional means, i.e. using a Zth-diagram.

In more recent work [8], a 3D fully coupled electro-thermal simulation have been reported to evaluate the robustness of power MOSFET in forward condition. The present work focuses on the avalanche regime and uses the loosely coupled method, which represents significant reduction of computation time compared to the fully coupled one.

This paper reports for the first time on a novel 3D approach, for this type of super-junction power MOSFET. The novelty manifests in its capability of predicting accurately the electro-thermal interaction between the core active device and the termination rings. The method presented in this paper, provides good in depth concurrent optimizations of electrical and thermal designs and performance in order to improve the ruggedness of the power MOSFET.

The breakdown voltages as a function of temperature and current have been derived from TCAD simulation in the avalanche regime. An empirical model has been extracted and converted to Spice. The loosely coupled electro-thermal simulations principle has been used. The results of the simulations have been confirmed by the measurements data from the electronic microscopy (EMMI) and from the transient IR thermography photos. The simulation results have been used to optimize the robustness of the power MOSFET.

2. Device Description

The device consists of an active area (core device) and a set of termination rings (see Fig. 1a, 1b and 1c). In this device the termination structure does not consist of super junction trenches but a set of rings which provides the freedom to control the voltage window between the breakdown voltage of the termination rings (BVTerm) and the breakdown voltage of the core active device (BVCore). Different scenarios of charge balance and voltage windows between BVTerm and

BVCore have been investigated. This paper reports mainly on the method used by presenting one case of optimal charge balance and BVTerm > BVCore (see Fig. 1d).

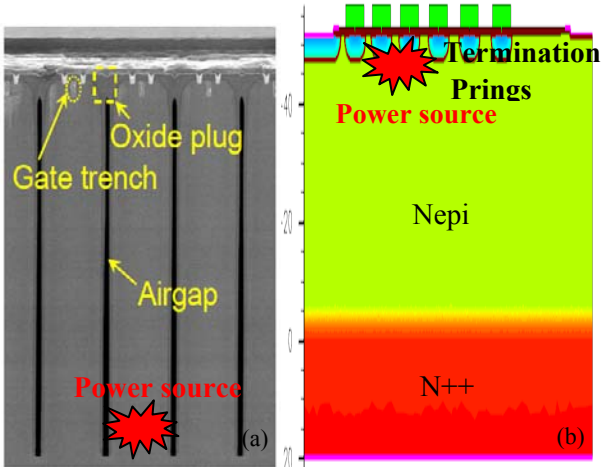

Fig. 1a: Schematic cross section of the core device showing the air gap, the super junction and the gate trenches. Under UIS condition the power is dissipated at the bottom of the core active device.

Fig. 1b: Schematic cross section of the termination rings. Under UIS conditions the power is dissipated at the surface of the termination rings.

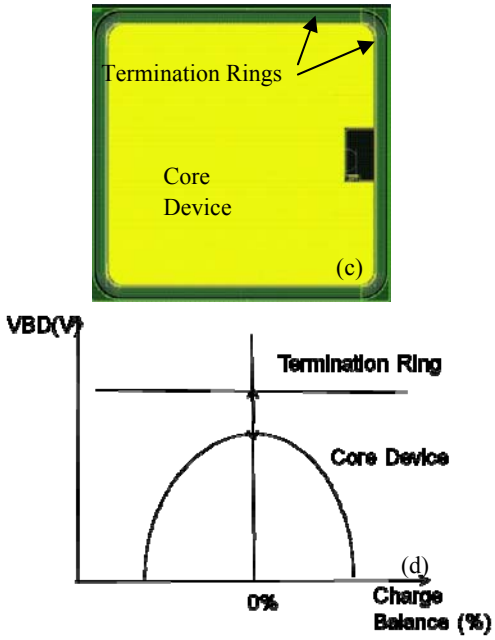

Fig. 1c: Top view of the full MOSFETS, core active device and termination rings.

Fig. 1d: Illustration of the VBD of the core device and the termination rings versus the charge balance of the super junction trenches.

3. Methodology

The novel approach used in the present contribution is described below in three steps:

1/ First TCAD simulations under DC breakdown conditions have been performed on the core device as well as on the termination rings. The TCAD simulations have been calibrated to the measurements data performed in [3]. As an example the resulting I-V characteristics in avalanche regime and for optimal charge balance are presented in Fig. 2. From these figures one can see clearly that BVCore and BVTerm both strongly depend on temperature and injected current.

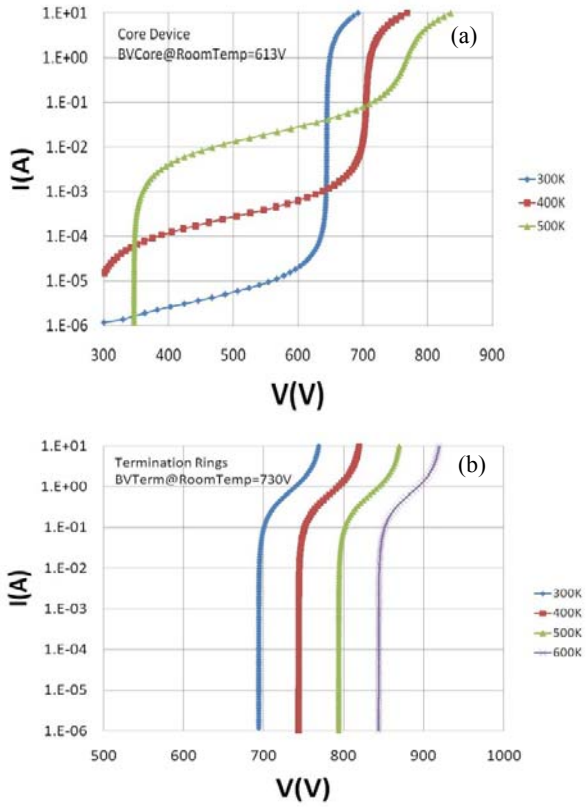

Fig. 2a: TCAD simulation of the I-V characteristics of the core device at different temperatures under DC breakdown condition. Simulations are for a 10A rated device. Full line is the behavioral model BVCore (T,ICore).

Fig. 2b: TCAD simulation of the I-V characteristics of the termination rings at different temperatures under DC breakdown conditions. Simulations are for a 10A rated device. Full line is the behavioral model BVTerm (T,ITerm).

2/ Second the dependencies of BVCore and BVTerm as a function of temperature and injected current have been empirically modeled. (See the equations of BVCore(T, ICore) and BVTerm(T,Iterm) in Fig. 3). These equations were converted into Spice model.

3/ Third a loosely coupled electro-thermal simulator was used, consisting of HeatWave™ [9], a FEM thermal engine and Spectre as a Spice engine. The simulator uses the relaxation method [10] with separate but synchronized thermal and electrical simulations. The advantages of the method are the relative simplicity of the implementation, the speed up of the simulation time and the capability of full structure analysis. The drawback is the difficulty to achieve

convergence in case of fast change of electrical power, which is the case of the studied power MOSFET in this paper. To remedy this problem, a smoothing function was introduced in the behavioral model in order to keep control of the convergence of the simulator and the computation time. To represent non-uniform heat distribution, the core active device as well as the termination rings has been segmented into smaller pieces, represented as well electrical as lumped device in Spice and thermal as power boxes in HeatWave. The number of segments, the size of each segment and the placement in 3D are user defined. This method allows to control the accuracy versus the simulation time. HeatWave reads the layout, the locations as well as the geometry of the power sources and the package properties. The thermal engine solves the heat equations and provides the local increase in temperature, a parameter called (trise), for each segment. This trise (rise in temperature) is passed to the corresponding device segment in Spice. A new updated value of breakdown voltage and thus power is generated and provided back to HeatWave. The principle of the loosely coupled is illustrated in Fig. 3.

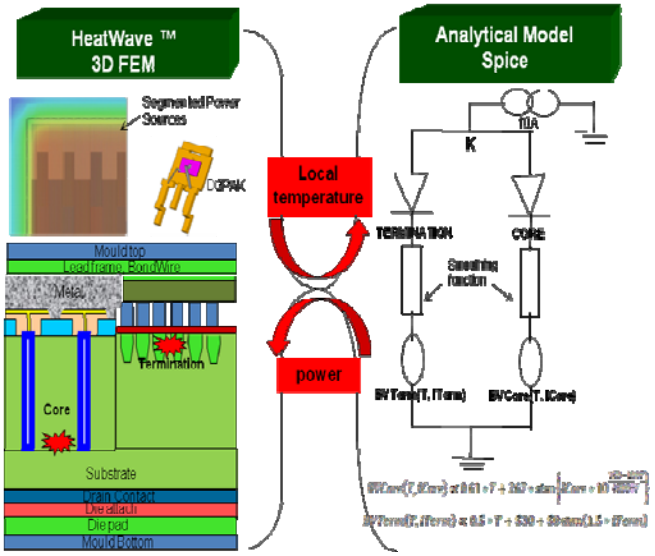

Fig. 3: Schematic representation of the electro-thermal concept used. On the left side, the thermal engine, HeatWave, takes into account the layout, location and geometry of dissipated power as well the material and technology properties from the device and the package. On the right the behavioral models of the breakdown voltages of the core device and termination rings are shown. Local temperature and power are exchanged during the electro-thermal simulations under UIS condition.

4. Experimental Results

A typical UIS pulse is shown in Fig. 4a. The total avalanche current decays from 10A down to 0A in 125us. In Fig 4a also the simulated currents in the core active device and in the termination rings are shown. One can easily see that a part of the injected current goes into the termination rings. Since the termination rings are much smaller in area compared to the active core, the current needs to be properly balanced. The Emission Microscopy (EMMI) measurements, shown in Fig. 4b, confirm the current distribution between core active device and termination rings as simulated in Fig. 4a.

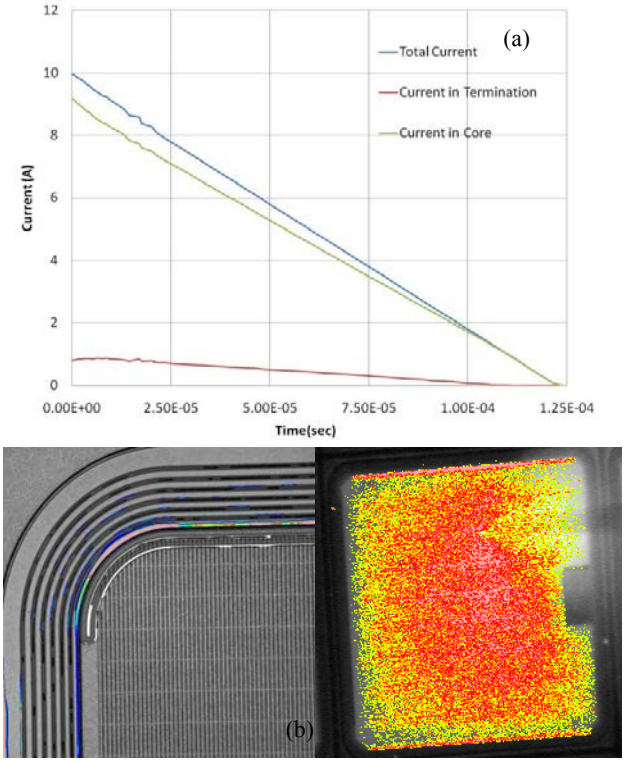

Fig. 4a: The simulated total avalanche current, current in the termination rings and in the core device during the UIS pulse.

Fig. 4b: EMMI measurements photos show the activation of the termination rings (left) and on the core active device (right) and thus confirms the balance of current between termination rings and core device, for different avalanche current densities.

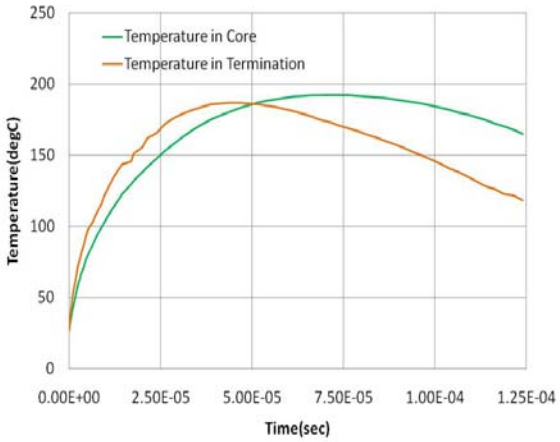

Fig. 5: The simulated maximum temperature in the core as well as in the termination rings during the UIS pulse. The termination, being smaller than the core device, heats faster.

The simulated temperatures are depicted in Fig. 5. Since the volume of the heat source in the termination rings is

smaller, for the same injected current, the termination rings will heat up faster compared to the core device.

A 3D snap shot of the simulated temperature distribution in the core device as well as in the termination rings is shown in Fig. 6.

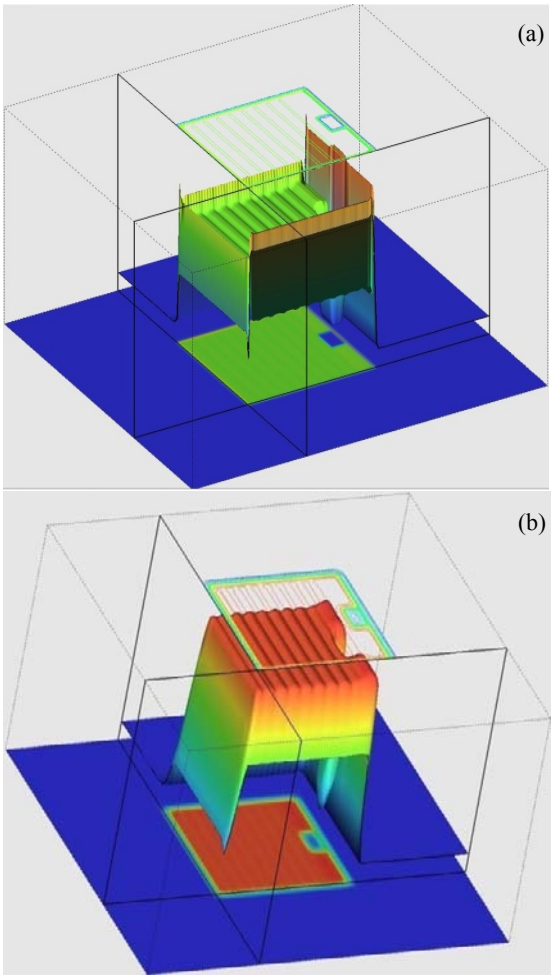

Fig. 6: 3-Dimensional temperature profile in the termination rings at 25us (a) and in the core device at 80us (b) during the UIS pulse. The termination rings are heated by the core device, while the core device is not heated by the termination.

In this paper a new approach was presented that can accurately simulate and optimize the electro-thermal robustness of a super junction power MOSFET. This method uses 3D electro-thermal simulation to predict the distribution of UIS current in termination rings and core device, as well for a packaged as for a non-packaged device. Out of these simulations also the optimal voltage window between BVCore and BVTerm can be deducted. In order to validate the new simulation method, the simulated voltage during the UIS pulse has been compared to the measured one and a good agreement has been obtained (see Fig. 7).

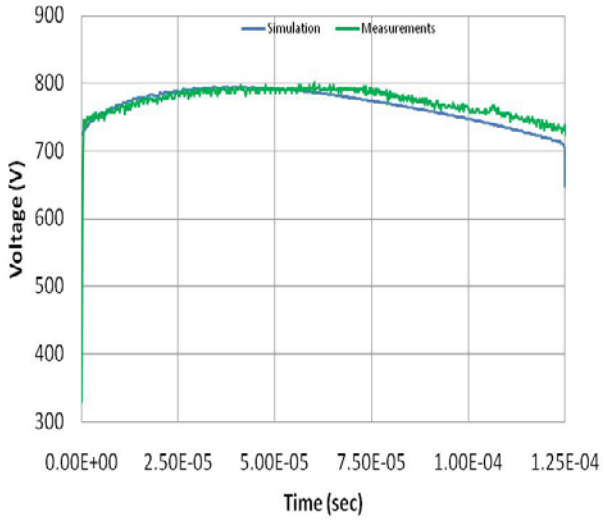

Fig. 7: The simulated BV is compared to the measured UIS curve. A good agreement is obtained between the simulation results and the measurements of the UIS curve.

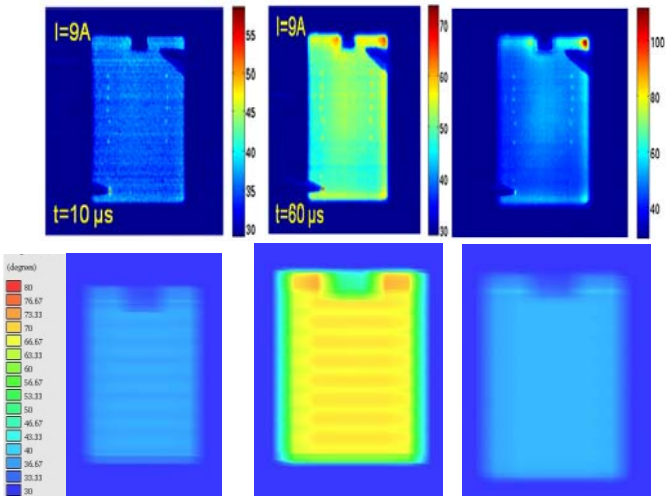

Fig. 8: First row shows the transient IR thermography photos performed during the UIS pulse (decaying from 9A down to 0A in 170us) taken at 3 different times and showing the heating-cooling of the core device. The second row shows the corresponding electro-thermal simulation for the same bias condition. The level of temperature is lower than the one reported in Fig. 5, in this case the device is bigger and the power density is lower. A good agreement is obtained between the simulation and the experimental data.

Further validation has been performed by comparing the simulation results to the transient IR thermography [10]. Also good agreement is observed between the simulation and the thermography photos (see Fig. 8).

5. Conclusions

By combining the physical aspects of the device taken from TCAD simulations and the geometrical and thermal aspects taken from layout and package, in full 3D, an optimal balance of power between core active device and termination rings is achieved. This method offers a novel and practical

approach to analyze and optimize the robustness of super junction MOSFETs for UIS. The EMMI measurements as well as the transient IR thermography photos validate the electro-thermal interaction between core active device and termination rings predicted by the novel approach.

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