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Electro-Thermal Characterization and Simulation of Integrated Multi Trenched XtremOS Power Devices

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Abstract-This paper presents a new methodology to characterize and simulate the electro-thermal aspects of packaged power drivers using multi-trenched XtremOS devices. Electrical device data is collected by pulsed and DC measurements. Thermal data is collected through on-chip sensors -and through a full surface high resolution transient interferometric mapping (TIM). For the first time a data driven segmented electro-thermal transient model is proposed to describe accurately the thermal profile behavior for the multi-trenched devices. Further investigations of the thermal heating impact on the driver due to the low thermal conductivity of the trenches (SiO₂) have been carried out.

I. INTRODUCTION

Over the last years, smart-power IC technologies have continuously shrunk in device dimensions and grown in complexity. Consequently power demands as well as die temperature have increased. Many reliability failure mechanisms strongly accelerate at high temperature [1] and the need for accurate electro-thermal simulation becomes critical.

In a previous work [2], thermal heaters between trenches were used to assess the thermal resistance of trench based structure on non active devices. This work presents a new technique that has the advantage of sensing the temperature during the transient on-off regime of the XtremOS.

The measurements on built-in temperature sensors have been complemented by the transient interferometric mapping (TIM) inspection [3] which is a powerful tool to visualize eventual hotspots. The analysis of the collected data was used to extract a segmented model consisting of a gallery of unit-cells that describe the location and the position of the heat sources. The resulting electro-thermal model was validated using transient electro-thermal simulation and the simulation results are

compared to the measurement data. The impact of the low thermal conductivity of the trenches (SiO₂) is being investigated.

II. EXPERIMENTAL RESULTS

The device under study is an integrated multi-trenched XtremOS device [4]. Fig. 1 shows a top layout view and a cross section of the 10hm power driver. The driver consists of 3 pockets separated by the isolation trenches and every pocket contains the gate termination trenches.

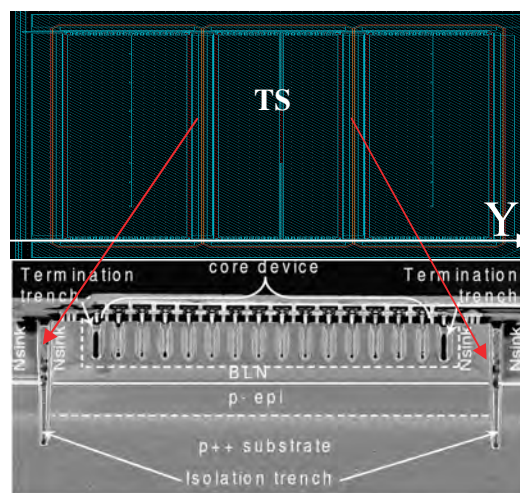


Fig. 1. Top layout view of the power driver XtremOS 10hm and the corresponding zoom in cross section of the device.

Indicated on Fig. 1 is also the built-in temperature sensor. This T-sensor (TS) represents the poly resistor of one of the central



gate trenches, and is measured in a region where the temperature will not deviate very much from its maximum. The drivers have been assembled in a SOIC package which were mounted on PCB and electro-thermally characterized.

The measured voltage across the central trench gate resistance (TS) at different temperatures is presented in Fig. 2. The calibration curve shows a high linearity and will be used to deduce the maximum junction temperature measured during the steady state and the transient electrical pulsing.

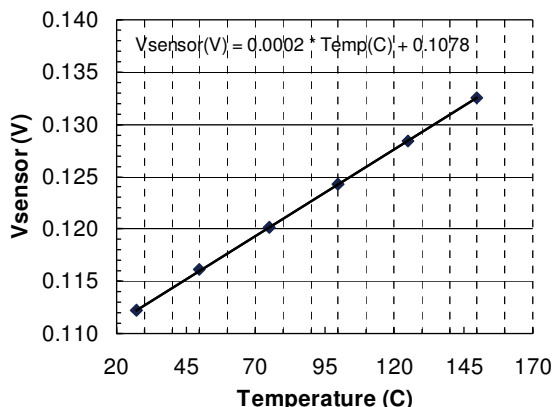


Fig. 2. Measured voltage across TS versus the temperature. This calibration curve is used to deduce the measured temperature in Fig. 3 and 4.

In a first step the electro-thermal characterization has been carried out in a steady state. The measured elevated Tjunction sensed on (TS) versus the electrical power is shown in Fig .3. The deduced thermal impedance Zth is also plotted. The fact that the trenches are filled with silicon oxide (SiO2) for which the thermal conductivity exhibits weak temperature dependence, results in almost constant Zth.

The measured temperature in transient mode of the driver in its package mounted on its PCB is presented in Fig. 4a and Fig .4b. The voltage on the drain is maintained constant, the gate is pulsed during 1ms (short pulses in Fig .4a) and 100ms (long pulses in Fig .4b) and the duty cycle is 50% and 67% respectively.

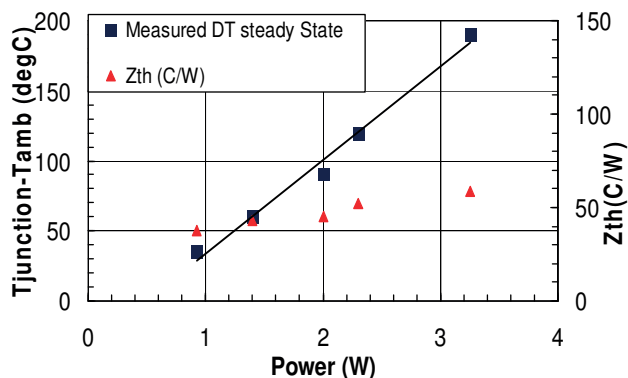


Fig. 3. Measured maximum elevated junction temperature versus electrical power, and the resulting thermal impedance in steady state.

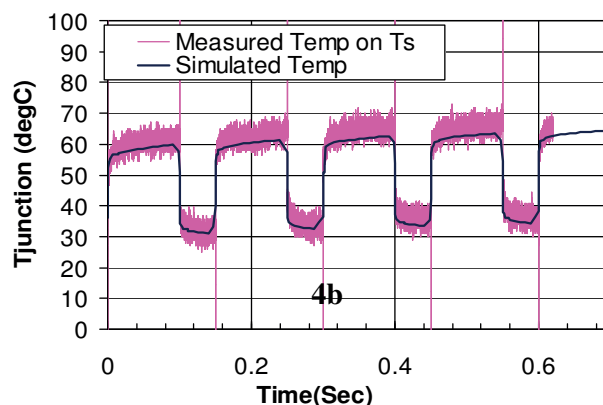
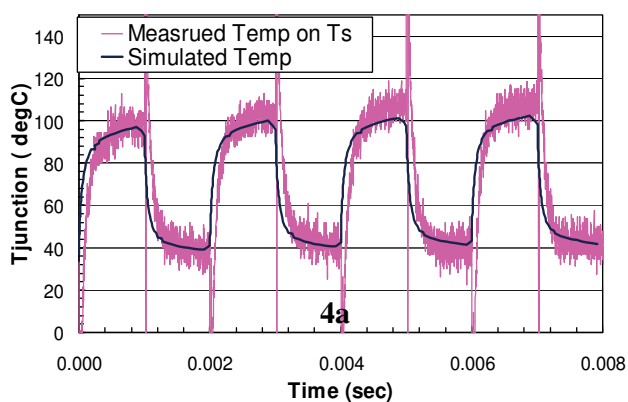


Fig. 4a. Measured elevated junction temperature for short pulses P=4W. Fig 4.b. Measured elevated junction temperature for long pulses P=1.2W. The electro-thermal simulation is also plotted. Very good agreement is observed between measurements and simulations.

Measured phase distributions for different time instants during a 100 μ s single stress pulse obtained by TIM technique are presented in Fig. 5, showing homogeneous power dissipation. The maximum of phase signal and thus the maximum of temperature occurs at the center of the middle pocket. This confirms the convenient location of TS capable of sensing the maximum elevation of $T_{junction}$.

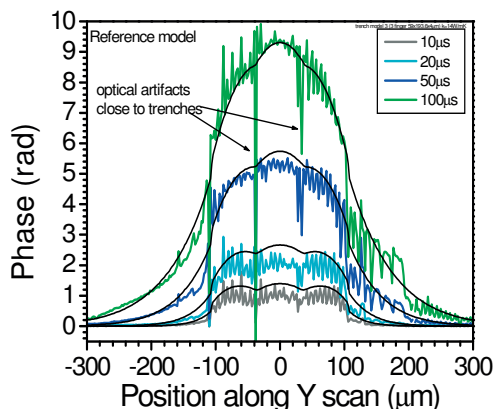


Fig. 5. The phase distributions measured with the TIM technique across the gate trenches, compared to simulation (black curves). Power was 5.3W. The phase shift is proportional to the integral of temperature distribution along the probe beam.

III. ELECTRO-THERMAL MODELING AND SIMULATION

The main objective to reach is to simulate and predict accurately the temperature distribution in the driver. To reach this, the driver was segmented into sub cells [5]. Each sub-cell is made electro-thermally aware (contains an accurate description of the heat source locations and shapes) which implies that current density distribution is correctly reflected. A graphical representation of the proposed model is presented in Fig. 6. The drawing illustrates in 3D and cross section the heat sources location and the gate and isolations trenches. The gallery of sub-cells is placed into a commercial transient electro-thermal simulator HeatWave [6]. The simulator uses the principle of loosely coupled electro-thermal simulation. A separate thermal network is built based on the layout and power source information (location, power value) and solved separately from the electrical network. This approach was chosen in order to better deal with the large time constant differences between thermal and electrical networks. The power transients simulated electrically are fed to the thermal simulator, which converts them into thermal transient. In order to reduce the computation time, the temperature values in the electrical simulator are updated only when a sufficient

temperature change occurs, and vice versa.

The results of the electro – thermal simulation using the proposed model is presented and compared to the measurement data in Fig. 4. A good agreement is obtained between measurements and simulation suggesting the valid methodology of the segmentation. Fig. 7 shows 3D and 2D snapshots of the electro – thermal simulation. This figure can be easily compared to Fig. 5 obtained by the TIM. Both figures show clearly the 3 maximum shapes of temperature in the three pockets. The electro-thermal simulation predicts accurately the location and the absolute value of the maximum junction temperature elevation relative to the ambient.

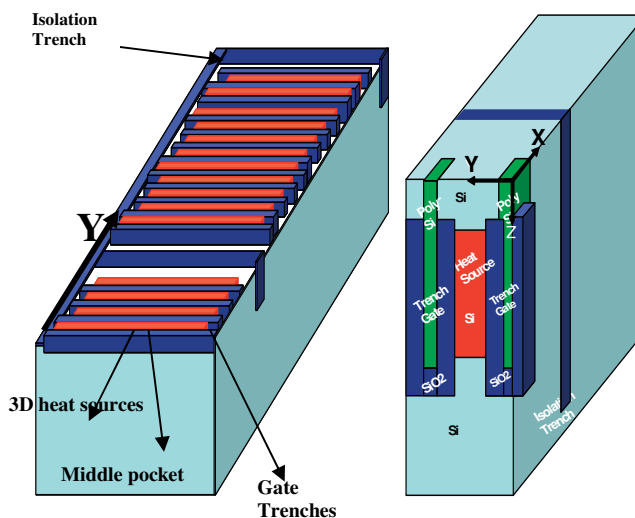


Fig. 6. 3D Geometrical representation (half of the driver is displayed) of the segmented model: dark blue shows the gate terminations and the trench isolation while the red boxes show the locations of the heat sources. The cross section shows a zoom in between 2 gate trenches.

Further investigations to study the thermal impact of the silicon-oxide trenches termination and isolation have been carried out. Fig. 8 shows the simulation of the reference model where the trenches are filled with SiO₂ (real case) compared to the case where trenches are absent. For low level of power, the effect of the trenches is barely noticeable. However the more power is dissipated, the temperature difference between the trench and no-trench case becomes larger. This can be attributed to the fact that when the heat waves propagate laterally, they tend to mirror on the thermal barriers of the trenches resulting in higher $T_{junction}$ in the driver.



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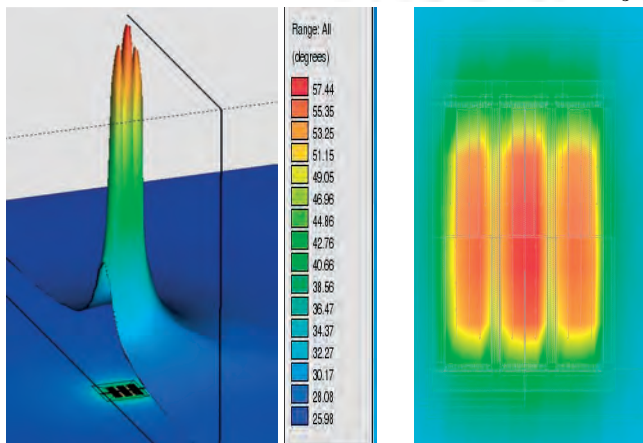


Fig. 7. Results of the electro-thermal simulation using the model of Fig. 6. These snapshots are taken at 100ms and the power is 1.2Watts.

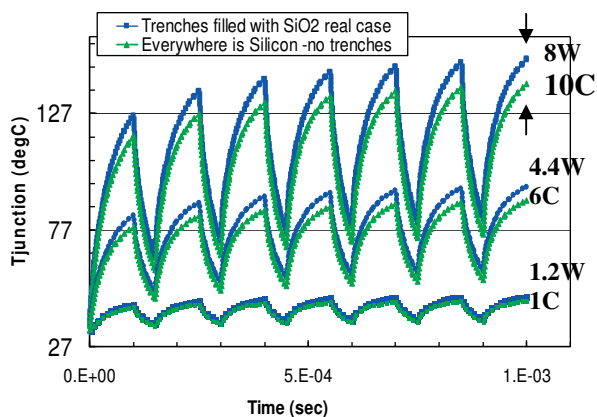


Fig. 8. Simulation of junction temperature elevation at 3 level of powers for 2 configurations : blue curves is the case in which the trenches are filled with silicon-oxide (thermal conductivity is 1.4 W/mK, heat capacity per unit volume $2.2E6 \text{ J/Km}^3$), green curves is the case where the trenches are absent, silicon filled in the complete pocket (thermal conductivity of the silicon is 156 W/km at 25C and decreases when rising the temperature, heat capacity per unit volume 1.63 E6 J/Km^3).

IV. CONCLUSION

A new methodology of electro-thermal characterization and simulation of power drivers has been presented and demonstrated using a multi-trenched integrated XtremOS device. Information on the heat source locations shapes and magnitudes have been extracted from the measurement data and the TIM inspection. This data was used to segment the power driver into a gallery of sub elements that are electro-thermally aware. The proposed model has been electro-thermally validated and a good agreement with the measured

data has been demonstrated. It has been found out that the effect of the low thermal conductivity of the trenches, acting like thermal barriers, becomes significant at high level of electrical power.

ACKNOWLEDGMENT

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REFERENCES

- [1] N. Rinaldi, "Electro-thermal phenomena in power devices and IC's", *ISPSD2006 Short Course*, Naples, June. 2006, pp. 4.
- [2] J. Roig et al, "Thermal resistance assessment in multi-trenched power devices", *Microelectronic Reliability*, 48, (2008), pp 1479-1484.
- [3] G. Haberehnlner et al, "Thermal Imaging of Smart Power DMOS Transistors in the Thermally Unstable Regime Using a Compact Transient Interferometric Mapping System", *Microelectronic Reliability*, 49, (2009), pp.1346-1351.
- [4] B. Desoete et al, "Integrated Submicron Switching Transistor Breaking the Si Limit at 100V", *ISPS 2008*, Prague, pp. 149-152.
- [5] J. Rhayem et al, "New Methodology on Electro-Thermal Characterization and Modeling of Large Power Drivers using Lateral PNP BJTs", *EUROSIM2010, Bordeaux*, in press.
- [6]. R. Gillon et al, "Practical Chip-Centric Electro-thermal Simulations", *THERMINIC2008*, Rome, September. 2008, pp. 220-223.