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Beyond-CMOS Nanodevices 1

Edited by
Francis Balestra

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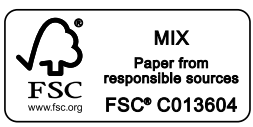

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General Introduction

Microelectronics, based on complementary–metal–oxide semiconductor (CMOS) technology, is the essential hardware enabler for electronic product and service innovation in key growth markets, such as communications, computing, consumer electronics, automotives, avionics, automated manufacturing, health and the environment. The global semiconductor industry underpins 16% of the world's total economy and is growing every year. The worldwide market for electronic products is estimated to be more than $1,800 billion, and the related electronics services market more than $6,500 billion. These product and service markets are made possible by a $310 billion market for semiconductor components and an associated $90 billion market for semiconductor equipment and materials. The new era of nanoelectronics, which started at the beginning of the current millennium with the smallest patterns in state-of-the-art silicon-based devices below 100 nanometers, is making an exponential increase in system complexity and functionality possible.

Nanoelectronics allow the development of smart electronic systems by switching, storing, monitoring, receiving and transmitting information. With respect to its societal relevance, the ubiquitous nanoelectronics is also closely linked to the notion of ambient intelligence, which is a vision of the future where people are surrounded by intelligent intuitive interfaces that are embedded in all kinds of objects and an environment that is capable of recognizing and responding to the presence of different individuals in a seamless way.

Since the invention of the transistor in 1947 at Bell Labs, followed by the first silicon transistor in 1954 and the concept of integrated circuits in 1958 at Texas Instruments, progress in the field of microelectronics has been tremendous, which has revolutionized society. In these last 50 years, dramatic advances have been achieved in the packing density of transistors. This has resulted in the density of transistors on an integrated chip (IC) doubling every two years (Moore's law) since the 1970s. At the beginning of the 1970s, the first microprocessor had only about

2,000 transistors (10 μm gate length), and the world's first two-billion transistor processor was reported in 2008 in 65 nm CMOS technology.

The same trend can be observed for memories. The dynamic random access memory (DRAM) capacity has been raised from 1 kb in 1970 to several Gb at present. Several billion transistor static random access memory (SRAM) chips have also been realized. For non-volatile memories, 256 Gb have been demonstrated. This increase in transistor count and memory capacity has led to increased processing power, now measured in thousands of millions of instructions per second (MIPS).

Moore's law also means a decreasing cost per function; the transistor price has dropped at an average rate of about 1.5 per year (about 10^8 since the beginning of the semiconductor industry).

However, according to the International Technology Roadmap for Semiconductors and ENIAC Strategic Research Agenda, there are big challenges to overcome in order to continue progressing in the same direction.

The minimum critical feature size of the elementary nanoelectronic devices (physical gate length of the transistors) will drop into the sub-decananometer range in the next decade. In the sub-10nm range, "Beyond-CMOS" devices, based on nanowires, nanodots, carbon electronics or other nanodevices, will certainly play an important role and could be integrated onto CMOS platforms in order to pursue integration down to nanometer structures. Silicon (Si) will remain the main semiconductor material for the foreseeable future, but the required performance improvements for the end of the roadmap for high performance, low- and ultra-low power applications will lead to a substantial enlargement of the number of new materials, technologies, device and circuit architectures.

Therefore, new generations of nanoelectronic ICs present increasingly formidable multidisciplinary challenges at the most fundamental level (novel materials, new physical phenomena, ultimate technological processes, novel design techniques, etc.).

In this timeframe, performance will also derive from heterogeneity, referring to the increasing diversity of functions integrated onto CMOS platforms as envisaged in the "More than Moore" (MtM) approach.

This book and the related book *Beyond-CMOS Nanodevices* 2 (Volume 2), also published by ISTE and Wiley, offer a comprehensive review of the state of the art in innovative Beyond-CMOS nanodevices for developing novel functionalities, logic and memories dedicated to researchers, engineers and students.

The book particularly focuses on the interest of nanostructures and nanodevices (nanowires, small slope switches, 2D layers, nanostructured materials, etc.) for advanced MtM (radio frequency (RF), nanosensors, energy harvesters, on-chip electronic cooling, etc.). Volume 2 focuses on Beyond-CMOS logic and memory applications.

MtM functions allow the world of digital computing and data storage to interact with the real world. MtM devices typically provide conversion of non-digital as well as non-electronic information, such as mechanical, thermal, acoustic, chemical, optical and biomedical functions, to digital data and vice versa. Clearly, MtM technologies and products provide essential functional enrichment to the digital CMOS-based mainstream semiconductors. MtM has become one of the major innovation drivers for a very broad spectrum of societally relevant applications.

There has been increased interest recently for using nanoscale Beyond-CMOS devices in the More Moore and More than Moore domains:

– miniaturization remains a major enabler for price reduction, functionality multiplication and integration with electronics;

– the CMOS technology is facing dramatic challenges for future low power, high performance and memory applications;

– nanoscale Beyond-CMOS structures can improve devices' intrinsic performance and enable new functionalities.

Nanotechnologies will also offer powerful ways to bring added value, in terms of cost, reproducibility, sensitivity, automation, analysis and new functionality in healthcare applications such as *in vitro* diagnostics or drug delivery, as well as in environment control (e.g. water, air and soil), agriculture and food, transport monitoring, ambient intelligence, defense or homeland security. A wide range of sensor types will be required, such as biochemical sensors, sensors for liquid and gas spectroscopy.

As a very good example, nanowires have received much attention from the research and development (R&D) community as components for electrical circuits based on CMOS-compatible processes. Although the R&D activities for nanowires were initiated to address the future need of IC technologies beyond the physical limits of CMOS, more and more R&D activity nowadays is devoted to using nanowires to create innovative MtM products.

Other fields in which nanostructured materials and nanodevices could be of great interest are in the domain of energy-autonomous systems using energy harvesting, for wireless sensor networks, *in situ* monitoring for mobile systems, body-area

networks, biomedical devices or mobile electronics; these systems will become very important in the future for the development of "green/sustainable" applications.

The integration of many different types of devices will be needed – for example, bio-sensors, nanoelectro mechanical structure (NEMS) devices, nanocomponents for logic and memory, energy scavenging systems and RF interfaces, for the development of these future nanoelectronics systems.

This book, and Volume 2, are thus reviewing innovative nanoscale structures that can improve performance and/or enable new functionalities in future terascale ICs and nanosystems. The convergence of More Moore and Beyond-CMOS, on the one hand, and the merging of MtM and Beyond-CMOS, on the other hand, have been extensively studied in scientific literature over the past few years. The two books offer a detailed overview of the most recent advances in these fields which have gained strong momentum for many applications.

In the MtM field, very sensitive nanosensors for biological and chemical products, mechanical, solar and thermoelectric energy harvesters, localized cooling on a chip with management of heat transfer using nanostructures, and high-performance, small–size and low-cost RF passive components using nanodevices or nanostructured materials are highlighted.

In order to develop future autonomous nanosystems, which will be needed for many applications of high industrial and societal relevance (monitoring of health and environment, internet of things, etc.), the main challenges are the development of CMOS-compatible technologies and using mainly "green" materials, the reduction of the energy consumption of sensors, computing and RF communication, together with the increase in the energy harvested from the environment.

The four parts of this book, and Volume 2, have been written by scientists, from universities and research centers, strongly involved in teaching and research programs related to nanoelectronic devices and circuits. Because of their expertise and international commitment, they are very well informed on the state of the art of the physics and technologies and the evolution of nanoelectronic materials, components, circuits and systems.

Part 1 of this volume reviews the nanosensing field, including Si nanowire biochemical sensors, fabrication of nanowires, functionalization techniques, sensitivity, integration of SiNWs with CMOS and portable system for real-time impedimetric measurements on nanowires biosensors.

Part 2 of this volume outlines new materials, nanodevices and technologies for energy harvesting, dedicated to vibrational energy harvesting (piezoelectric and

electromagnetic energy transducers), thermal energy harvesting (thermal transport at nanoscale, porous silicon for thermal insulation on silicon wafers, spin-dependent thermoelectric effects, composites of thermal shape-memory alloy and piezoelectric materials), nanowire-based solar cells, and smart energy management and conversion (power management solutions for energy harvesting devices, sub-mW energy storage solutions).

Part 3 of this volume highlights on-chip electronic cooling, including silicon-based cooling elements (Schottky barrier junctions, strained silicon Schottky barrier mK coolers, silicon mK coolers with an oxide barrier, silicon cold electron bolometers, integration of detector and electronics), thermal isolation through nanostructuring (lattice cooling by physical nanostructuring, porous silicon platforms, crystalline membrane platforms, etc.) and tunnel junction electronic coolers.

Part 4 of this volume addresses new materials, nanodevices and technologies for RF applications, devoted to substrate technologies for silicon-integrated RF and millimeter wave (mm-wave) passives, metal nanolines and antennas for RF and mm-wave applications, and nanostructured magnetic materials (nano-composite materials, nanomodulated continuous films) for high-frequency applications.

Volume 2 gives an overview of Beyond-CMOS nanodevices for logic and memory applications, including small slope switches (tunnel field effect transistor (FET), ferroelectric gate FET, NEMS), nanowires (ultimate CMOS, ultimate memories with new solutions offered by nanowire technologies in terms of charge storage and resistive change types), two-dimensional (2D) layers and devices for More Moore and More than Moore (graphene and other 2D materials).

Francis BALESTRA
April 2014

PART 1
Silicon Nanowire Biochemical Sensors

Part 1 Introduction

In today's world of ultimate electronic scaling, the quest for ever-new application areas is obvious. In the effort to simplify and speed up biomolecule detection, ultra-scaled integrated electronics has been suggested and demonstrated in solutions for biochemical sensing. A biochemical sensor is a device that determines the presence of a specific molecule in a liquid by converting the concentration of the molecule into an output signal. Biochemical sensors are used in areas such as analytical chemistry, biotechnology, medical diagnosis and environmental sciences. A general trend is to scale down the sensor dimensions in order to achieve higher sensitivity, shorter response times and miniaturized analytical systems that are of desktop or even handheld size. These small-sized systems would enable several analytical applications where the determination of a specific molecule could be easily made in the field experiment. One potential application is in the medical area where small-sized systems could enable point-of-care analysis near the patient in the hospital, in the ambulance or in the patient's home.

In recent years, silicon nanowires have been shown to have a great potential in biochemical sensors due to their large surface-to-volume ratio (enabling high sensitivity), very small size comparable to molecules (enabling small sampling volumes), label-free detection (avoiding fluorescence tagging) and the possibility of integrating several nanowire sensors (enabling the reduction of size and cost of system). The basic operation of the silicon nanowire is based on the electric field effect, where a charge on the silicon nanowire surface modulates the free carrier concentration in the silicon nanowire and thus modulates the silicon nanowire conductivity. The silicon nanowire thus converts the presence of a molecule in the liquid into a detectable electrical signal. This is an attractive feature since it can potentially enable integration of the sensor element (the silicon nanowire) with electronics onto the same small-scale semiconductor chip. Typically, semiconductor

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chips range in size from 1 mm^2 to about a few cm^2, and by integrating the signal processing on the same chip as the silicon nanowire a very small footprint system can potentially be realized.

Although the principle of field-effect detection is simple, there are several issues that need to be solved to make possible a silicon nanowire-based sensor that can enable a miniaturized label-free biochemical sensor. It is desirable to introduce a low-cost method to integrate silicon nanowires onto the same semiconductor chip that is used to build the electronic read-out circuitry. The sensor also needs to have a good selectivity, i.e. only to detect the molecule of interest and not other charged molecules or ions present in the liquid. Selective detection of molecules in a liquid is based first on attaching molecules, called probes, onto a bare or oxide-covered silicon nanowire (this is called functionalization of nanowires) and then by inserting the silicon nanowire into the liquid containing the molecule of interest (this is often called the analyte). After ample time (response time), the analyte will bind to the probe and the binding event will change the charge at the surface of the silicon nanowire and thereby modulate the conductance in the silicon nanowire. The electrical output signal of the sensor is thus given by the measured silicon nanowire conductance change. Achieving good selectivity and good sensitivity of a silicon nanowire-based sensor is challenging since, in realistic liquids, there are often several different charged molecules and ions present that can have a profound impact on the selectivity and the sensitivity. Moreover, the concentration of ions and non-interesting molecules can vary significantly from application to application. A potential approach to address the challenges in nanowire-based sensors and fully explore the potential of silicon nanowire-based sensor is the integration with complementary metal–oxide–semiconductor (CMOS) technology that would enable an advanced scaled and low-cost sensor. This would also enable the full advantage of using CMOS circuits for advanced read-out techniques, for example signal amplification and filtering. In Chapter 1, we describe silicon nanowire fabrication techniques followed by techniques to functionalize nanowires in Chapter 2. Chapter 3 deals with the sensitivity of silicon nanowire sensors and Chapter 4 discusses a potentially low-cost integration scheme of silicon nanowires with CMOS technology. Finally, in Chapter 5, an example of a developed portable system using an advanced read-out technique with a full impedimetric measurement of silicon nanowires is presented.

1

Fabrication of Nanowires

1.1. Introduction

Several fabrication processes of silicon nanowires have been developed in the research community. They can be divided into bottom-up or top-down approaches. The earliest reports of silicon nanowire fabrication often used bottom-up approaches (e.g. the vapor–liquid–solid (VLS) or similar mechanisms) to realize silicon nanowires. These methods are based on the fact that a seed particle on the silicon surface acts as a sink for the silicon atoms in the liquid phase and silicon nanowires grow out of the surface with the seed particle on the top. With these bottom-up approaches, it is relatively easy to realize nanowires at a low cost. However, one of the major drawbacks of these approaches is that the placement of the nanowires is determined by the position of the seed particle, and the exact position of the seed particle is difficult to precisely control. Also normally the bottom-up methods result in a random network of silicon nanowires on the silicon surface. Because of the random placement and the out-of-plane growth, it is not straightforward to integrate the bottom-up fabrication methods with the traditional approach used to manufacture electronics, such as complementary metal–oxide–semiconductor (CMOS) circuits, which relies on lithographic methods to transfer patterns into layers on a silicon wafer.

In the research community, the most common top-down technique to pattern sub-100 nm dimensions, needed for silicon nanowire fabrication, is electron beam lithography (EBL). With EBL, feature sizes below 100 nm are easy to achieve and patterns below 10 nm have been realized. There is no mask required since the method relies on the precision of an electron beam that is programmed to expose areas in a resist. This makes the method highly flexible and fast prototyping can be

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made without the need for mask fabrication. The combination of being a maskless technique and having high resolution is the fundamental reason for the widespread use of EBL in the research community. The major drawback of this technique is that the writing process is serial in nature and thus extremely time-consuming. Therefore, wafer-scale fabrication is challenging with write times of several hours per wafer depending on the amount of features to be written.

With the overall goal of integrating silicon nanowires with CMOS circuits, a viable approach is to use conventional top-down techniques, used in CMOS manufacturing, to realize a vast amount of silicon nanowires on a silicon wafer. From a technological point of view, this is straightforward but a major challenge is to achieve a low-cost solution that is suitable for sensor applications. Conventional top-down optical patterning techniques, such as deep-ultraviolet (UV) and immersion deep-UV photolithography, are currently the industry standard for leading-edge semiconductor manufacturing. However, these techniques are extremely tool expensive (e.g. an immersion 193 nm wavelength tool with resolution less than 80 nm can cost more than € 15 m) and demand a high-volume application in order to be cost-effective. Generally, they are only accessible to large-scale integrated circuit manufacturers. For low-volume applications, conventional I-line (wavelength of 365 nm) optical stepper lithography is much less capital intensive with tool prices in the range of approximately € 0.2 m to € 0.3 m. However, I-line lithography tools can only print pattern resolutions of about 350 nm in the resist which is not adequate for pattern silicon nanowires with less than 100 nm feature sizes. With advanced techniques such as sidewall transfer lithography (STL), which is nowadays used by the semiconductor industry and referred to as self-aligned-double-patterning (SADP), it is possible to pattern deca-nanometer size silicon nanowires with I-line lithography and achieve high wafer scale throughput.

This chapter is organized as follows: section 1.2 describes top-down fabrication of silicon nanowires using EBL, which combined with optical lithography can be a viable approach if not too many silicon nanowires need to be patterned on a wafer. Section 1.3 describes the STL technique using I-line stepper lithography to pattern a vast amount of silicon nanowires on a silicon wafer. In section 1.4, we describe how bottom-up Si nanowires synthesized by VLS – CVD can be assembled at low cost in an efficient way for further use as a sensing material.

1.2. Silicon nanowire fabrication with electron beam lithography

1.2.1. *Key requirements*

As discussed above, one key route toward sensitive nanoscale sensor devices is the creation of large surface-to-volume ratio sensing areas. Hence, dense arrays of

nanowire structures with a high length-to-width ratio are favorable building blocks for such devices. In Figure 1.1, a semi-dense array of silicon nanowire features is presented as an example. It is obvious that the relatively high aspect ratio – the height of the features is roughly three times their width – significantly contributes to a large surface-to-volume ratio. These long quasi-one-dimensional nanowires have to be fabricated with good critical dimension (CD) control as well as low line edge and line width roughness (LER and LWR), which pose special challenges on the lithographic processes used to define these structures.

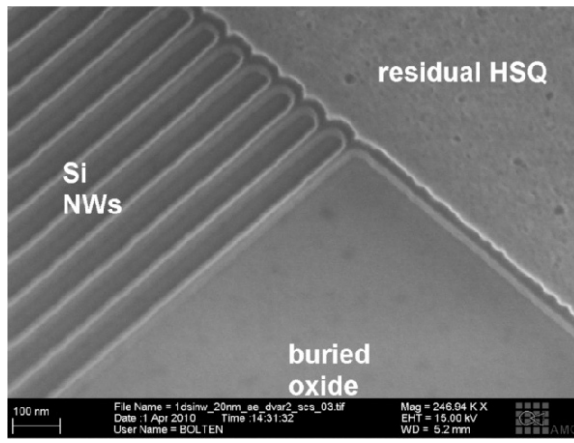


Figure 1.1. *Array of silicon nanowire features after dry etching and partial removal of residual HSQ resist*

Especially in a research and development (R&D) environment where the influence of design variations such as nanowire width, height, length and the number of parallel nanowires per device on device performance is investigated, it is crucial to guarantee a very high degree of control over CDs, LER and LWR.

1.2.2. *Why electron beam lithography?*

One lithographic technique which offers the high resolution needed for the fabrication of nanowire devices and which is capable of fulfilling the requirements discussed above is EBL.

Using EBL, silicon nanowires with widths of 10 nm and below can be fabricated as being comparably fast, flexible, efficient, reproducible and with good quality, as can be seen in Figure 1.2 where some parallel sub-10 nm features in 40 nm hydrogen silsesquioxane (HSQ) resist are shown.

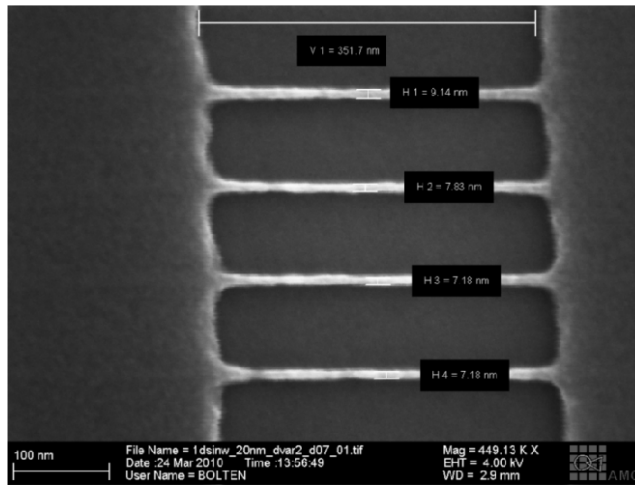


Figure 1.2. *Sub-10 nm lines in 40 nm HSQ resist, defined by EBL using a Vistec EBPG 5200 system operated at 100 kV*

Speed, flexibility and efficiency are mainly achieved due to the fact that EBL is a maskless lithographic technique, allowing the direct exposure of the design on a sample or wafer without the need to first fabricate a mask. This not only helps to reduce the time between design and a first exposure run dramatically – in an ideal scenario, the design can be exposed literally minutes after it has been finalized – but also offers the flexibility to routinely adapt the design if the first results suggest such changes without the cost of a new mask and the time delay of a mask fabrication. Hence, EBL is ideally suitable as a prototyping technique for novel device concepts such as nanoscale sensors. Furthermore, using the right tools, materials and processes, EBL offers resolution well below 10 nm at a quality level and with a reproducibility which can be hardly challenged by other lithographic techniques.

1.2.3. *Lithographic requirements*

For sensing devices, dense quasi-one-dimensional arrays of nanostructures fabricated with a high degree of CD control and low LER and LWR are needed. Translated into requirements for lithography, this means that:

– resist materials must offer smooth resist profiles;

– resist materials must offer resolution of 10 nm and better;

– resist masks must be suitable as a mask for dry etching;

– resist material and development processes need to offer high contrast to resolve dense nanowire features;

– the overall lithographic process must be robust enough to guarantee good CD control and a reasonable degree of reproducibility even for feature sizes of ~10 nm.

1.2.4. *Tools, resist materials and development processes*

When aiming to fulfill such demanding lithographic requirements as listed above, the choice of EBL tool is essential for the results that can be achieved. With EBL systems mainly based on a converted scanning electron microscope, such as the RAITH 150 line of EBL tools, the acceleration voltage limits the resolution for dense nanostructures at a given resist thickness due to forward scattering of the electrons within the resist layer. EBL systems like the Vistec EBPG series or the tools fabricated by JEOL offer acceleration voltages up to 100 kV, significantly reducing the forward scattering and hence increasing the achievable resolution for dense structures.

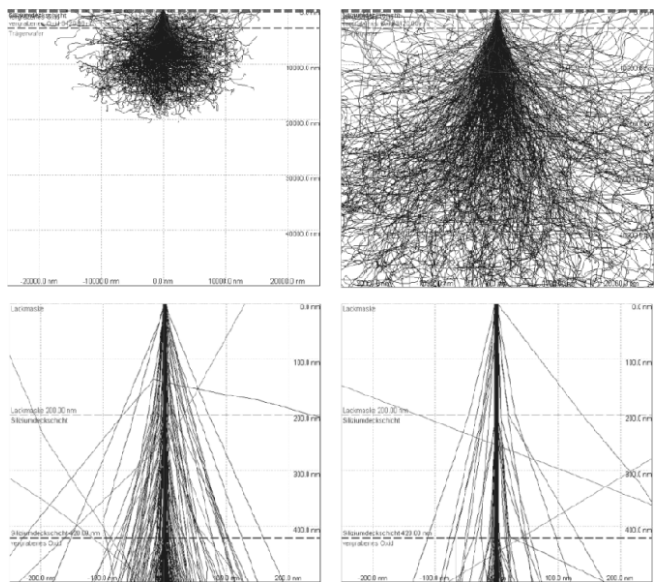


Figure 1.3. *Monte-Carlo simulations of electron scattering. Left-hand side images: 50 kV acceleration voltage; right-hand side image: 100 kV acceleration voltage. Top row: overview; bottom row: detailed view of resist layer, in this case 200 nm thick. For a color version of this figure, see www.iste.co.uk/balestra/nanodevice1.zip*

In Figure 1.3, this is demonstrated using trajectories of Monte-Carlo simulations for two acceleration voltages: 50 and 100 kV. It is clearly obvious that the forward scattering in the resist layer and the upper substrate stack layers is reduced with increasing acceleration voltage. At the same time, the higher acceleration voltage causes an increased backscattering.

Inorganic negative tone resist materials such as HSQ offer the potential to exploit the theoretically almost unlimited resolution of EBL. Such materials also yield smooth resist profiles and hence help to minimize LER and LWR. As the features have not just to be defined in a resist material but also need to be transferred into the substrate material via dry etching, the resist mask must have a sufficient thickness for this subsequent etching process; hence, resist masks with an initial thickness of less than 40–50 nm are not suitable for fabrication purposes.

In order to better use the potential of HSQ, a high contrast development process, either based on highly concentrated tetramethylammonium hydroxide (TMAH) developer solutions or developers that contain sodium hydroxide (NaOH) and sodium chloride (NaCl), is necessary. The latter are not compatible with standard CMOS processing environments but offer slightly better contrast; hence, higher resolution for dense features while TMAH is fully compatible with CMOS technology. Under optimized processing conditions feasible for a reliable fabrication of dense HSQ nanometer-scale features, the resolution which can reproducibly be achieved with TMAH is almost identical to the one demonstrated for NaOH/NaCl.

1.2.5. *Exposure strategies and proximity effect correction*

Another important aspect in the process of defining dense nanometer-scale structures by EBL is the choice of an appropriate exposure strategy and the application of an efficient proximity effect correction (PEC).

Regarding the exposure strategy, multipass grayscale exposure techniques, which basically divide the exposure into n sub-exposures with an exposure dose of roughly $1/n$ of the nominal exposure dose for the structure, can significantly reduce the LER and LWR. The slight misalignments between the sub-exposures lead to an increased overlap of the EBL exposure shots, stitching errors can be improved using overlaps between the sub-exposures and the effect of shot noise is reduced to the division of each shot into the sub-exposure shots. Especially for dense nanostructures a multipass exposure strategy with a reasonable number of sub-exposures does not significantly increase the overall exposure time, in contrast to what one might expect at first glance. Due to the nature of the design consisting of dense nanometer-scale features, low beam currents are used for such exposures.

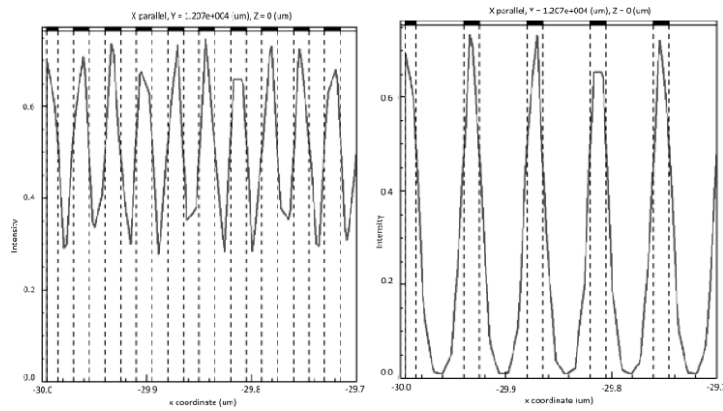
With a low beam current, the shot frequency is, for state-of-the-art EBL systems with maximum writing frequencies of 50 MHz and above, usually well below this maximum. Hence, a multipass exposure strategy can often be applied using the same exposure parameters such as beam step size and beam current, and it simply makes better use of the speed potential of the system. An increase in exposure time by applying such techniques is therefore mainly caused by the increase of stage movements, beam blanking operations and similar operations' contribution to the exposure overhead.

As shown in Figure 1.3, the use of a high acceleration voltage minimizes forward scattering at the cost of increased backscattering. While forward scattering directly reduces the achievable resolution, the influence of the backscattered electrons on the overall exposure result can be minimized by applying a PEC. The amount of dose contribution due to forward scattered and backscattered electrons for each part of a design is calculated and the primary exposure dose for each shot is carefully adjusted taking those additional dosage contributions into account. In addition to changing the exposure dose for each area of the design, it is also possible to apply slight changes to the design itself to compensate for the proximity dosage.

1.2.6. *Technology limitations and how to circumvent them*

Using state-of-the-art EBL systems and processes, nanostructures with feature sizes well below 10 nm can be realized with reasonable reproducibility and quality. Using HSQ and an initial resist thickness of ~40 nm, resist features significantly below 8 nm tend to collapse due to their mechanical instability caused by their high aspect ratio of 5 and above. Thinner resist layers are usually not suitable for pattern transfer into an silicon-on-insulator (SOI) substrate with a top silicon thickness of 50 nm. Using thinner, substrate material can be helpful to enable a further reduction of the resist thickness and hence the feature size. Employing standard CMOS-compatible processing techniques, features with widths less than ~30 nm can be realized as 1:1 line/space structures. To achieve a 1:1 line/space ration below 30 nm, either other, non-compatible developer solutions or special double exposure techniques need to be used.

One such approach has been developed and realized within the framework of the Nanofunction project. As shown in Figure 1.4, even after applying a fine-tuned PEC the modulation depth of the intensity profile of the exposure dose will quickly become insufficient to resolve ultra-dense features if feature size and feature spacing are reduced to 20 nm and below.



a) b)

Figure 1.4. *Simulated effective exposure intensity profile for 15 nm line/space structures. Gray line: intensity profile. Black and white boxes on top of plot and dashed lines: line/space regions and desired intensity profile. Simulated using the LayoutBEAMER software. a) Line/space ratio 1:1 and b) line/space ratio 1:3*

An efficient way to overcome this limitation is to utilize the excellent overlay accuracy offered by state-of-the-art EBL systems and to use a divide-and-conquer approach to replace the challenging task of fabricating such ultra-dense nanoscale features by the challenge of fabricating two sets of less densely packed but well-aligned nanowire features. This strategy is depicted in Figure 1.5. To create a line/space structure with 15 nm 1:1 features, the problem is divided into two exposures, each consisting of 15 nm wide line features with a 60 nm period, hence a 1:3 line/space ratio. As shown in Figure 1.4, such features can be easily defined. After the first exposure, shown in dark grey in Figure 1.5, the substrate is unloaded from the EBL system and developed. Subsequently, the substrate is recoated with resist and reloaded into the system, and the second exposure, shown in light gray, is performed after a very careful alignment of the substrate and with a fine-tuned dose to compensate effects caused by the existence of the first set of line features adjacent to the features that have to be defined during the second exposure.

The importance of a very precise control of the overlay between both sub-exposures can be seen in Figure 1.6, which shows the resulting line features for the case of a slight misalignment in the range of 5 nm between both exposures. The effect of the misalignment does not only effect the positioning of both sets of lines with respect to each other but also leads to a significant increase in LER and LWR as well as to areas where the resist is not completely removed between the lines.

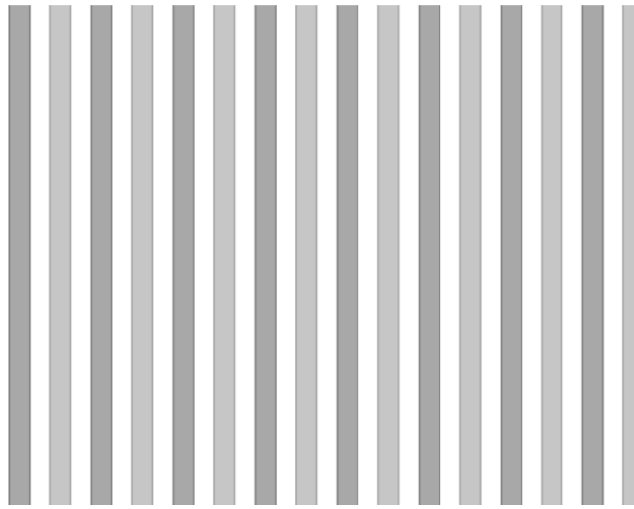


Figure 1.5. *Detail of the design of the exposed 15 nm half pitch grating. First exposure layer in dark gray and second layer in light gray*

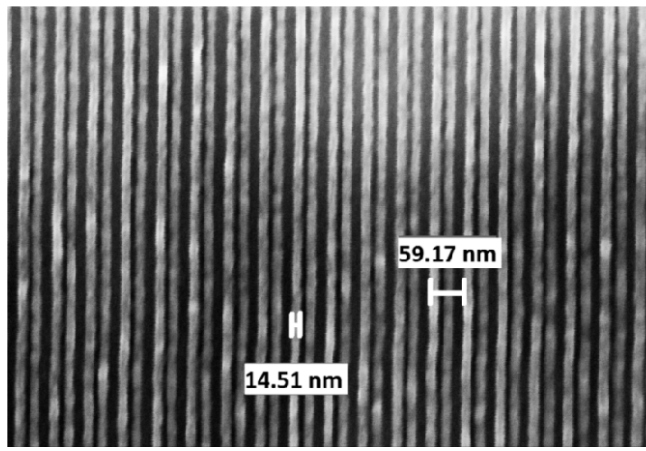


Figure 1.6. *Slightly misaligned 15 nm wide HSQ resist features*

If an alignment accuracy better than 5 nm can be achieved, no such effects occur and 20 nm and 15 nm 1:1 line/space ratio features can be defined using standard fully CMOS-compatible processing, as shown in Figure 1.7.

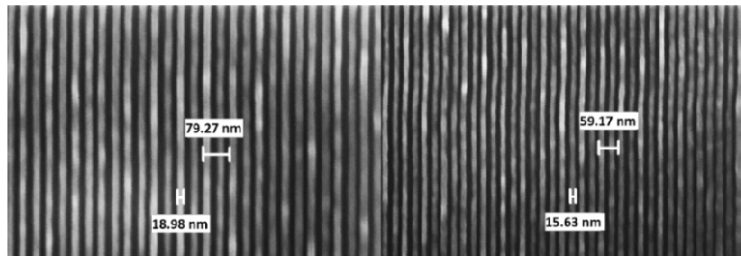


Figure 1.7. *Exposure result for dense nanoline structure in 40 nm HSQ resist. Left hand side: 20 nm half pitch, right hand side: 15 nm half pitch*

Dense nanowire features, defined in a 40 nm thick resist layer with excellent etching properties and hence being easily transferable to a substrate material by means of dry etching, can offer excellent surface-to-volume ratios and are, therefore, well suited for a large variety of sensing applications.

1.3. Silicon nanowire fabrication with sidewall transfer lithography

Optical stepper lithography is a top-down standard patterning technique developed for the semiconductor industry to print patterns in a resist layer over a full wafer scale with a high throughput of more than 50 wafers/h. Optical lithography is used to pattern the different layers in the fabrication of CMOS circuits and it is thus attractive to use the same optical lithography for fabrication of silicon nanowires. STL enables pattern lines of arbitrary small line width using conventional I-line lithography [CHO 02, HÅL 06]. The final silicon nanowire width is determined by the deposition and etching techniques rather than the resolution limit of the optical lithography. Figure 1.8 shows the STL method for patterning of silicon nanowires in the silicon layer of a silicon-on-insulator wafer. The basic principle is simple and straightforward; first deposition of a hard mask and a support material is followed by patterning of the support material. In this step, it is important to achieve vertical sidewalls of the support material with as low sidewall surface roughness as possible. Then a spacer material is deposited and etched back leaving the spacer material on the sidewall of the support material. The thickness of the spacer material will determine the final silicon nanowire width, hence the name STL. The key to achieving the final targeted nanowire width is that the deposition of the spacer material is conformal and that the etch-back is anisotropic. The support material is etched and a high selectivity to the spacer material and to the hard mask is mandatory. Finally, the hard mask is patterned by optical lithography and the spacer material together with the resist is used as masks to transfer the patterned to the underlying hard mask. After removal of the spacer material and the resist, a third mask can be used to cut part of the lines created in the hard mask if it is desirable.

This could be necessary if only one nanowire is desired since the first mask that creates an opening in the support material always creates a closed ring, and therefore without the third cut mask the formed nanowires will always be in a closed loop. The final step is to etch the silicon layer to form the silicon nanowires using the hard mask as a mask. The STL process can thus produce planar nanowires on wafer scale using conventional I-line optical lithography with three lithography masks and deposition and etching process technology.

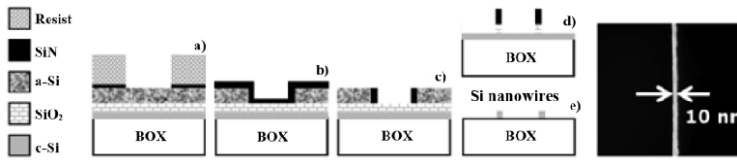


Figure 1.8. *Schematic of the STL process using SiO_2 hard mask, amorphous-Si as support layer, SiN as hard mask for etching the support layer and SiN as the spacer material. Silicon nanowires are formed in the silicon layer of a silicon-on-insulator wafer where BOX is the buried oxide. The top view SEM picture to the right shows a 10 nm wide silicon nanowire fabricated by STL with a line width roughness of 1.5 nm*

The STL process can be implemented with various material combinations. In the following, we describe a process using only common and compatible materials in a CMOS process technology such as SiO2, Si and SiN as depicted in Figure 1.8 [GUD 11]. SiO2 as a hard mask is attractive because reactive ion etching of Si using Cl2/HBr/O2 chemistry has a very high selectivity of >100:1 between Si and SiO2. The high selectivity allows the SiO2 hard mask to be relatively thin and still acts as a mask for Si etching. A thin hard mask is beneficial for the transfer of the narrow width spacer material into the hard mask. In STL, the line edge roughness is determined by the patterning of the support material and it is thus important to reduce the sidewall roughness of the resist and remove any resist residuals at the bottom of the resist, e.g. by a light O2 plasma ashing before patterning the support material. It is also important that the support material itself does not induce a sidewall roughness. Figure 1.9 depicts the sidewall surface roughness measured by atomic force microscope or microscopy (AFM) for different spacer materials. The relatively large grains of poly-SiGe inflict a high sidewall roughness [GUD 08] and it is thus preferable to use crystalline or rather amorphous support materials to minimize the sidewall roughness. An important aspect of an STL process with an amorphous support material is that the line edge roughness is determined by the sidewall roughness of the support material, and since the final silicon nanowire width is determined by the deposited thickness of the spacer material the roughness of the two silicon nanowire edges is correlated and it is actually possible to achieve lower line width roughness than the line edge roughness. This would not be possible using direct patterning of the resist since the two edges will be uncorrelated in that

case. In [GUD 11], it was demonstrated that silicon nanowires with line edge roughness of 3 nm and a line width roughness of less than 2 nm can be achieved using an amorphous Si spacer material. Using Si as support materials also allows the use of highly anisotropic Cl2/HBr/O2 reactive ion etching chemistry with high selectivity to both SiN (hard mask for amorphous Si etching) and the SiO2 hard mask under the support material. Furthermore, the Si support material can be wet stripped in TMAH with extreme selectivity toward SiO2 and SiN. Finally, the SiO2 hard mask should be etched using SiN spacers as a mask. This etch is a delicate step when implementing STL with the SiO2/Si/SiN material combination. Commonly used reactive ion etching with CHF3/CF4 chemistry only provides an etch rate of SiO2 a few times higher compared to SiN; so care must be taken not to erode the SiN spacer while etching SiO2 hard mask. There is a delicate trade-off in the SiO2 hard mask thickness given the targeted silicon nanowire width. A thicker SiO2 hard mask will cause more erosion of the SiN spacer and thus put a lower limit on how thin SiN spacer materials can be and therefore limit the minimum silicon nanowire width that can be achieved. A thinner SiO2 hard mask will allow for thinner SiN spacers to be used, therefore allowing for thinner silicon nanowire widths, but too thin an SiO2 hard mask will not work as a proper mask for the reactive ion etching of silicon. Especially, the first step in silicon etching employs a relatively low selectivity etch toward SiO2 in order to break through any native oxide on the silicon surface. The selectivity in the breakthrough etch sets a minimum thickness of the SiO2 hard mask. By a proper choice of materials and layer thicknesses together with conformal deposition and well-controlled reactive ion etching, the STL process can be fast and can achieve a high yield as indicated in Figure 1.10 where a top view of several 60 nm wide nanowires can be seen. The inset in Figure 1.10 is a SEM showing a single 60 nm wide silicon nanowire fabricated in the silicon layer of an SOI wafer.

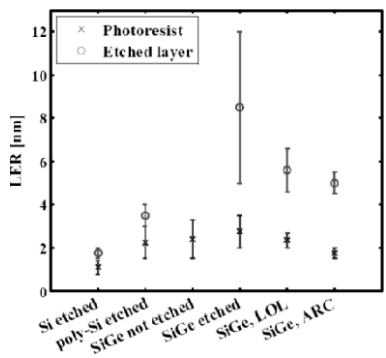


Figure 1.9. *Line edge roughness of etched spacer support materials. Polycrystalline materials exhibit a higher sidewall surface roughness after anisotropic etching. Polycrystalline SiGe support material has a line edge roughness more than 5 nm, and with silicon support material as low as 2 nm in line edge roughness can be achieved*

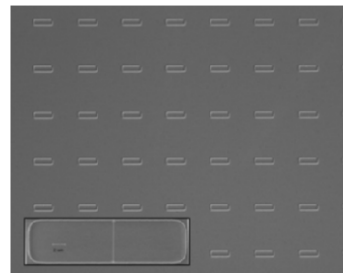


Figure 1.10. *Top view optical microscope picture showing 60 nm wide SiN spacer material fabricated using STL. In total, 48 out of 1,024 nanowires in a matrix are seen in the picture. More than 100 chips each with 1,024 nanowires were patterned on a single SOI wafer. The inset displays an individual Si nanowire after transfer into the Si layer*

1.4. Si nanonet fabrication

A nanostructured network (nanonet) is defined as a random network of high aspect ratio nanostructures (nanowires (NWs) or nanotubes (NTs)) [GRU 07, ZHA 12]. When its thickness is of the same order of magnitude than the length scale of its individual component, the nanonet is considered as three-dimensional (3D) because the percolation properties of such networks show 3D-typical characteristics. On the opposite, network that is significantly thinner will show two-dimensional (2D) percolation properties (see Chapter 3). Examples of such 2D and 3D nanonets are shown in Figure 1.11.

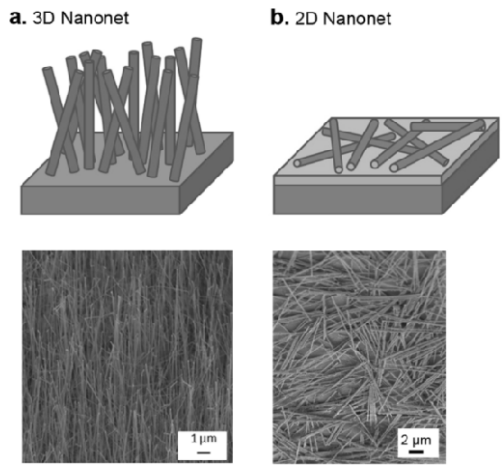


Figure 1.11. *3D nanonet: schematic representation and top-view SEM image of 3D Si nanonet a). 2D nanonet: schematic representation and top-view SEM image of 2D Si nanonet b)*

On the one hand, as explained in section 1.1, several drawbacks make the 3D nanonet integration more complex. On the other hand, and as described in detail in Chapter 2 (section 2.3), 2D nanonets have several unique properties which arise either from the individual components, the NWs or NTs, or from the structural properties of the network itself that facilitate the integration as a sensor.

In the literature, 2D nanonets are mainly fabricated by solution-based assembly of the NWs or NTs (e.g. spray coating [FER 04, KAE 05], Langmuir–Blodgett [ACH 06, PAR 08, TAO 03] and vacuum filtration [LI 06, WU 04]), which enables the fabrication of nanonets having a wide range of thicknesses, from sub-monolayer coverage to over 1 μm thickness. In the recent years, such nanonets based on carbon NTs have been studied and integrated into chemical and biological sensors that exhibit high sensitivity to gas or biological molecules [BYO 06, STA 05, WOO 07]. However, very little literature has been reported for Si nanonets.

Among the solution-based assembly methods for the nanonet fabrication, the vacuum filtration method is highly simple, versatile, low cost and scalable to large areas [DAL 08, DE 09, HU 04, MAD 10, WOO 07, WU 04]. The process itself guarantees the film homogeneity. The nanonets assembled by this method can be easily deposited at room temperature onto various types of substrates: transparent or opaque, conductor or insulating, flexible or rigid.

1.4.1. *Si NWs fabrication*

For this work, the silicon nanowires were grown on silicon <1 1 1> substrates by reduced pressure chemical vapor deposition (RP-CVD) using the Au-catalyzed VLS mechanism [WAG 64]. The growth was performed in a CVD furnace Easy TubeTM 3000 from first nano at 650°C under a pressure of 3 torr. Silane (SiH_4) was used as the silicon precursor with flow of 40 sccm. Hydrogen chloride (HCl) was also added during the growth in order to inhibit the gold diffusion and the lateral growth [GEN 12, POT 11]. Phosphine (PH_3) was added to dope the SiNWs with phosphorus.

The as-grown vertically standing SiNWs in the <1 1 1> direction (Figure 1.11a) are typically 10 μm in length with a diameter between 70 and 100 nm leading to an aspect ratio (length over diameter) above 100. Such an aspect ratio is necessary to favor the nanonet cohesion and the interconnection between the nanowires. Indeed, we experimentally demonstrated that in the case of too small an aspect ratio (around 10–20), the resulting network is inhomogeneous and of bad quality.

1.4.2. *Si nanonet assembling*

The 2D Si nanonets are assembled by the vacuum filtration method [SER 13]. First, silicon nanowires are dispersed in deionized water by ultrasonication for 5 min. Then, the nanowire solution is characterized by absorption spectroscopy using a Tecan Infinite 1000 in order to determine qualitatively the nanowire concentration in the solution. The absorbance scans are carried out from 230 to 1,000 nm with a 2 nm step to analyze the spectral properties of the nanowire solution. Further dilutions of the solution are done until its absorbance at 400 nm equal to 0.06. Thus, the nanowire amount in the solution can be reproducible from one solution to another even if the nanowire concentration is not quantitatively determined. After the dilution, the SiNW solution is filtered through a 0.1 μm porous nitrocellulose membrane (47 mm in diameter). As the solvent goes through the pores, the nanowires are trapped on the membrane surface forming subsequently an interconnected random network: the 2D Si nanonet (Figure 1.11(b)). Different volumes of SiNW solution are filtered in order to prepare thin networks of controllable thickness and density. Finally, the network is transferred onto various substrates by membrane dissolution due to a treatment with an acetone liquid bath for 30 min.

1.4.3. *Si nanonet morphology and properties*

Once the NW concentration in the solution is fixed by absorption intensity at 400 nm, the network density depends on the volume of the SiNW solution filtered as shown in Figure 1.12. Figures 1.12(a) and (b) display the SEM images of 2D Si nanonets with different NW density. We can notice the nanonet homogeneity that is in fact guaranteed by the filtration method. Indeed, when a network area on the membrane becomes thicker, the filtration speed in that region decreases although it increases in other regions that maintain the homogeneity. By analyzing the SEM images, the SiNW density on the surface is determined and it is shown in Figure 1.12(c) as a function of the volume of solution filtered for a given absorption intensity at 400 nm (0.06).

The observed linear dependence in Figure 1.12(c) demonstrates that the density of nanowires in the network can be monitored by simply controlling the volume of solution filtered through the membrane for a given absorbance at a specific wavelength.

In this condition (Absorbance 0.06 at 400 nm; volume 30–160 mL), each fabricated Si nanonet with density lower than 100×10^6 NW.cm^{-2} is, on the one hand, sufficiently thin to guarantee a good adhesion on the substrate even after

further immersions in solution for functionalization steps (see Chapter 2). On the other hand, such nanonets have been successfully deposited on numerous substrates: glass, polyethylene, silicon, silicon dioxide and silicon nitride over surfaces of around 1 cm^2.

Moreover, the so-assembled Si nanonets are well above the percolation threshold allowing conduction across the system: two-probe measurements at room temperature for most of these devices show non-linear, symmetric *I–V* characteristics with high current level despite the numerous inter-NW junctions in the network. Indeed, as described in Chapter 2 (Figure 2.9), even for the wider devices (1,000 µm) that contain several hundreds of NW–NW junctions per percolation path, the current is not negligible [TER 13].

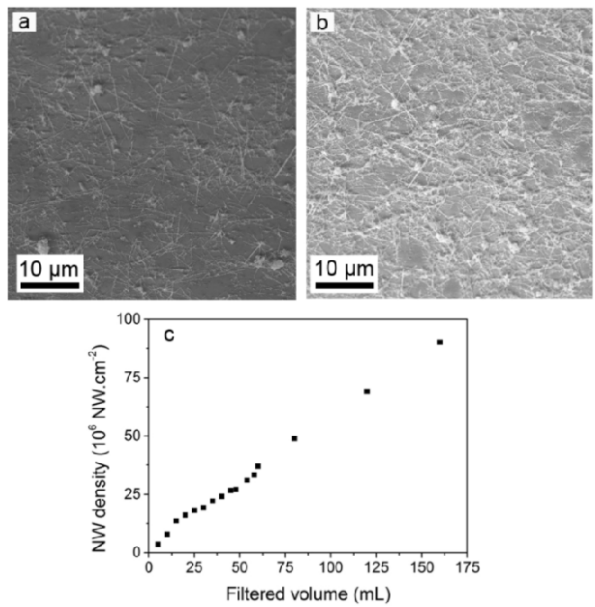


Figure 1.12. *Si nanonets assembled by the vacuum filtration method. SEM images of Si nanonets assembled using solution of same absorbance at 400 nm using different filtered volumes leading to different NW densities: a) 45 mL, 27 × 10^6 NW.cm^{-2}; b) 60 mL, 37 × 10^6 NW.cm^{-2}; c) SiNW density as a function of the SiNW solution volume for a given absorbance at 400 nm (0.06). The NW density is determined from SEM images of nanonets elaborated from different volume filtered of SiNW solution. For each volume studied, several images are analyzed at different locations on the nanonet leading to the mean density*

Considering the observed properties, including the precise control over NW density in the nanonet enabled by the filtration method, the enhanced specific area of these materials, the good adhesion on various substrates, the reproducibility and the very interesting electrical behavior, such 2D random networks are particularly well designed for integration into innovative gas- and biosensing devices with an improved sensitivity, using a low-cost fabrication method compatible with large-scale applications. As a result, the Si nanonets represent a bottom-up, low-cost alternative for the design of field-effect sensors that could be integrated above IC.

1.5. Acknowledgments

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2

Functionalization of Si-Based NW FETs for DNA Detection

2.1. Introduction

From a general point of view, biosensors are devices where the quality of the detected signal in terms of magnitude and reproducibility upon the biomolecular recognition event depends on two main characteristics of the sensitive material: (1) its intrinsic properties and (2) its biomodified surface.

As described in Chapter 1, the nanowire physico-chemical and morphological properties – size, diameter and length – depend on the elaboration conditions. These properties are critical for biodetection. The surface biomodification is also an important characteristic of the biosensor. It results from the surface functionalization process, which aims to anchor receptor groups or probe molecules to the surface of the nanowires (NW) that recognize the target analytes through their high specificity and strong binding in the buffer environment (Figure 2.1). The target–receptor interaction then varies the surface potential of the NW channel and modulates the channel conductance, which is collected by a detection system.

This process must be thoroughly performed and controlled. The biomolecular probes must be strongly attached to the surface material through covalent (or assimilate) bonding to the NW surface. Their coverage rate must be homogeneous and adapted to the surface morphology. This means that their conformation and their surface distribution should not produce steric hindrance for the target recognition (Figure 2.2).

Chapter written by Valérie STAMBOULI, Céline TERNON, Pauline SERRE and Louis FRADETAL.

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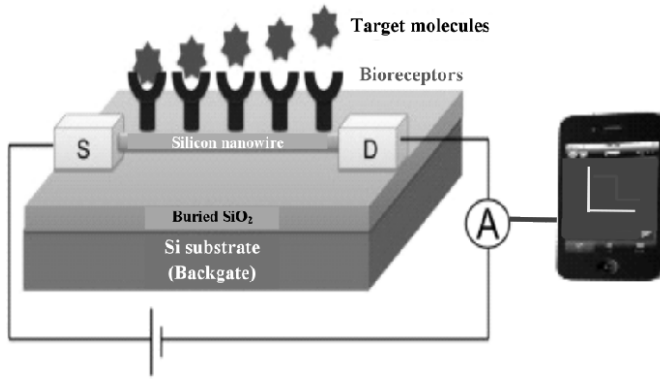

Figure 2.1. *Cartoon of the functionalized nanowire with receptor molecules specifically recognizing targets and giving rise to an electrical signal. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

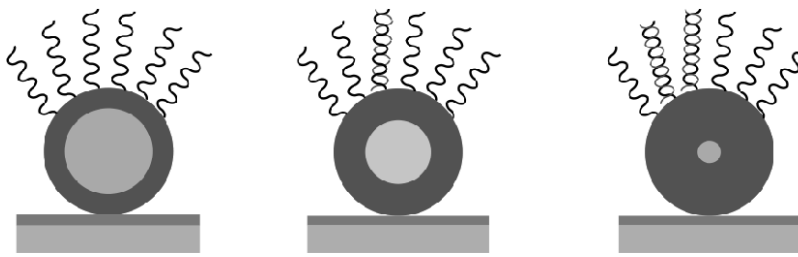

Figure 2.2. *Cartoon (cross section) of the functionalized nanowire with charged receptor molecules (in black) specifically recognizing targets (in red) and giving rise to a change of the NW depleted zone*

In the case of single nanowire for nano-FET biodetection, a localized and selective biomodification process is required. The aim is notably to confine the biomolecules on the NW and to protect the NW immediate environment (metal contacts) from the functionalization reagents which may alter them and thus alter the signal. Therefore, it is clear that the NW functionalization process is a key step in the fabrication of the bio NWFET.

In the case of the most generally used silicon nanowires (Si NWs), because Si NWs have a native oxide coating similar to other oxide-based NWs, the linkage of the receptor is straightforward. However, depending on the target molecule to be detected, there are several ways to functionalize the NW Si surface. On the one hand, extensive data exist for the covalent modification of the native oxide. Its chemical surface modification is performed using alkoxysilane derivatives giving

rise to the formation of Si–O–Si bonds and to self-assembled monolayers with functional groups at the end [PAT 06, ZHE 05]. Silane coupling chemistry is widely employed in the fabrication of Si NW devices [NOY 09, WAN 06, BAL 10]. On the other hand, when the oxide layer is undesirable, it can be etched away using HF, leaving hydrogen-terminated surface, which can subsequently react with terminal olefin groups to form stable covalent Si–C bonds [CHA 11, STR 05].

In our case, we present the DNA functionalization using the silane chemistry which has been performed on two different and original Si-based NW devices:

– randomly oriented Si NW networks, also called “nanonets”;

– SiC single NWs.

Each of these morphologies presents its advantages and disadvantages. Their interest and originality within the field of DNA biosensors as well as the results obtained after their functionalization are presented in the following sections. Before that, the functionalization process is briefly described.

2.2. Functionalization process

The process used to functionalize the different Si-based nanostructures is adapted from the one used for silicon dioxide and metal oxide planar surface [STA 06]. It is divided into four main steps that are presented in Figure 2.3(a).

The first step is the hydroxylation of the surface. This step creates hydroxyl groups which are at the origin of the hydrophilicity of the surface. The hydroxylation can be achieved via several chemical treatments. Some of them involve hydrofluoric acid HF or NH4F [SCH 08], Piranha solution H_2O_2/H_2SO_4 [GAO 11] or oxygen plasma [FRA 14].

The next step (step 2, Figure 2.3) is the grafting of the aminopropyltriethoxysilane (APTES). APTES assures a covalent attachment of DNA on the semiconductor substrate. This is performed by either liquid phase deposition (LPD) or by the chemical vapor deposition (CVD) technique that we have used. Compared to the liquid phase technique, the vaporized APTES has a lower viscosity than the liquid one; therefore, this method is expected to give better results in the case of nanostructures. The samples are placed inside a sealed chamber with nitrogen gas and a small volume of liquid APTES (150 µl). The temperature is set up at 80° for 1 h. Following silanization, the samples are rinsed with pure ethanol and deionized water, and then annealed at 110°C for 1 h. To make a chemical bonding between the amine functions of both APTES and DNA strands, the samples

are immersed in a solution of a cross linker – glutaraldehyde – in water. This corresponds to step 3 (Figure 2.3). After drying, the single strand DNA probe grafting (step 4) is carried out by depositing 2 µl drops of a DNA solution diluted in a phosphate buffer (C = 10 µM) on the surface. After that, the surface is biomodified and ready for detection of single strand DNA target by hybridization.

To perform the hybridization, a solution of complementary DNA strands (variable concentration) is spread out on the sample surface. These target strands are labeled with a fluorescent cyanine Cy3 molecule. After 45 min at 42°C, the samples are rinsed with saline solution to remove all unbound targets from the surface and dried with nitrogen. In the case of NWs, this functionalization process is combined with lithography and lift-off techniques. This part will be described further.

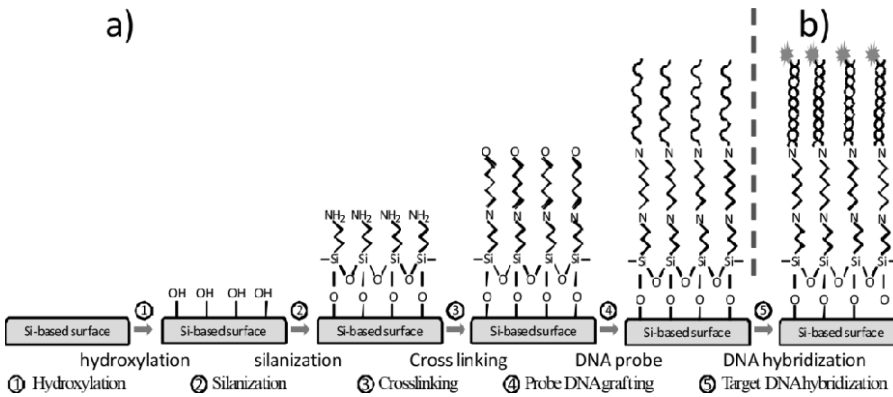

Figure 2.3. *Flow chart of chemical process on Si-based surface*

2.3. Functionalization of Si nanonets for DNA biosensing

A nanostructured network (nanonet) is defined as a random network of high aspect ratio nanostructures, NWs or nanotubes (NTs) [ZHA 12, GRU 07]. When its thickness is of the same order of magnitude as the length scale of its individual component, the nanonet is considered to be three-dimensional (3D) because the percolation properties of such network show 3D-typical characteristics. On the contrary, a network that is significantly thinner will show two-dimensional (2D) properties. Examples of such 2D nanonets are shown in Figure 2.4.

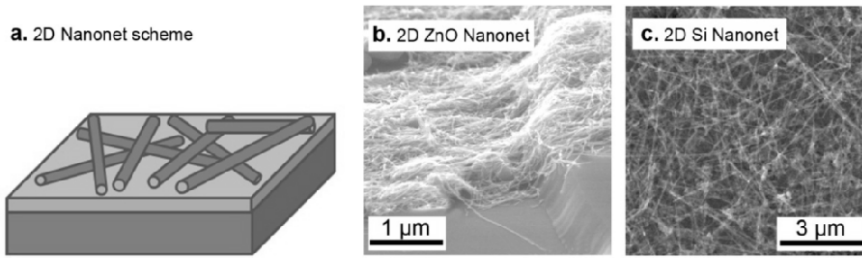

Figure 2.4. *a) Schematic representation of 2D nanonet. b) SEM image of 2D ZnO nanonet deposited across a 500 nm SiO_2 step, aspect ratio (ZnO NWs) = 400; the nanonet is highly flexible and is able to adapt to the substrate morphology with good conformity and without any crack. c) SEM image of 2D Si nanonet with density of 80 × 10^6 NWs.cm^{-2}*

A nanonet has several unique properties that arise either from the individual components, the NWs or NTs, or from the structural properties of the network itself. They include:

– *High surface area/high porosity*: due to the component geometry, the surface area drastically increases, in comparison with thin film. Besides, a lot of space is still available for the addition of a functional material due to the high porosity.

– *Electrical conductance*: the so-defined nanonet is above the percolation threshold and the larger the NW conductivity is, the better the network conductance is. Factors such as NW/NW contacts play a major role and need to be studied and optimized.

– *Optical transparency*: a network of high aspect ratio nanostructures has high transparency, approaching 100% when aspect ratio tends to infinity.

– *Mechanical robustness and flexibility*: a random network of interwoven NWs has significantly higher flexibility than those of a thin film as illustrated in Figure 2.4(b) for a ZnO nanonet.

– *Reproducibility and fault tolerance*: at the macroscopic scale, the nanonet involves several thousands of NWs so that the observed properties result from a large scale statistics averaging the individual NW properties. Moreover, breaking a conducting path in the network leaves many others still present and the overall nanonet properties are stable. As a result, in contrast to individual components, nanonets offer high reproducibility of the physical properties coupled with easy manufacturability.

– *High-quality components*: it is easier to grow error-free NWs than thin films over a large area. As a consequence, high NW quality implies better electrical and optical properties.

– *Functionalization ability*: by attaching chemical species or nanoscale materials such as nanoparticles (NPs) with well-defined functionality, it is possible to add properties induced by the synergy between NWs and NPs.

Almost all of these properties are advantageous in the case of sensing applications. As a consequence, such nanonets composed of Si NWs have been studied in the framework of DNA hybridization detection with and without a label.

For biological applications, the silicon NWs are particularly attractive due to the fact that (1) Si NWs are one of the best characterized examples of semiconducting NWs, (2) their surface is covered with a native oxide which can be easily functionalized for bio-applications [CHA 11, VOI 04]. With the help of Vapor–Liquid–Solid (VLS) growth of Si NWs, it is possible to precisely control both the dopant concentration and their aspect ratio [DHA 10] (Figure 2.5). Therefore, such NWs have been chosen as building blocks of 2D nanonets for DNA hybridization detection.

The nanonets can be prepared by various fabrication techniques including the direct growth (by CVD, for example [TER 09, BAR 06], the inclusion of the nanostructures into a polymeric embedding medium [BRE 04, HAG 00, MON 06, VEL 05], or the self-assembly from solution [KAE 05, ACH 06]. This last strategy, solution-based assembly, is particularly attractive since it enables the fabrication of nanonets with a wide range of thicknesses, from sub-monolayer coverage to over 1 μm thick. Among the solution-based assembly methods, the filtration method that we will use is highly versatile and allows the production of homogeneous 2D nanonets over large surfaces [WU 04, HEO 08, LI 06, DE 09]. The fabrication procedure requires that a solution of the Si NWs be filtered using standard vacuum filtration apparatus. During filtration, the nanostructures are gradually deposited on the filter surface forming the nanonet, which acts as the filter cake. The nanonet can then be transferred to the desired surface by dissolving the filter in an appropriate solvent. Varying the volume or the concentration of the filtered solution allows us to precisely control the nanonet thickness. This process of cake formation ensures a good homogeneity of the nanonet. Indeed, as the nanostructures accumulate on the filter surface, the flow resistance in these regions increases so that the solution flow will increase toward regions which have accumulated fewer nanostructures. Moreover, due to this simple and original self-controlled homogenization mechanism, the process can be upscaled to large sample dimensions, in connection with the filter size (see Chapter 1 for detail).

Following the controlled, reproducible, homogeneous and well-interconnected network fabrication, the obtained NW networks (Figure 2.6) can be easily deposited

at room temperature onto various types of substrates: transparent or opaque, conductor or insulating, flexible or rigid.

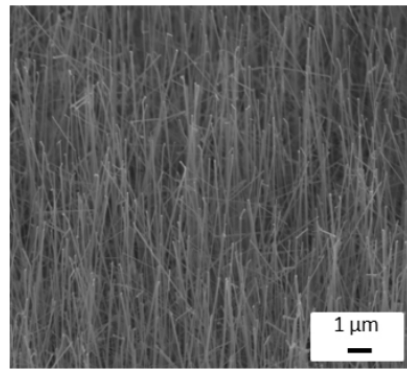

Figure 2.5. *SEM image of n-doped silicon nanowires synthesized by the vapor–liquid–solid method. The degenerated nanowires are about 10 µm in length with a diameter between 70 and 100 nm leading to an aspect ratio above 100*

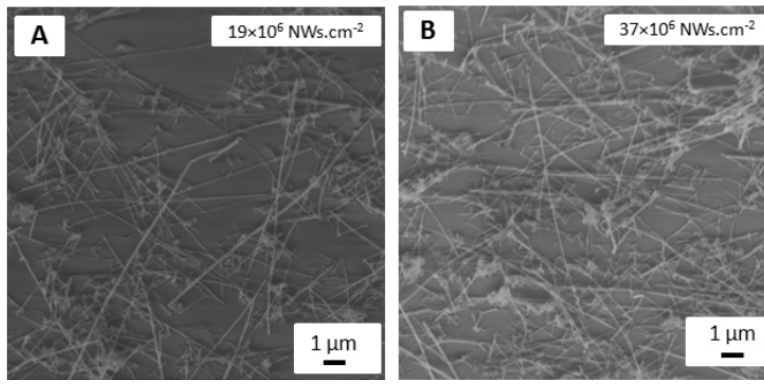

Figure 2.6. *SEM images of Si nanonets on Si_3N_4/Si substrate with a) low and b) high NW density*

2.3.1. *Detection of DNA hybridization on the Si nanonet by fluorescence microscopy*

Then, for the first time, the Si nanonets have been integrated into a DNA biosensor. After the covalent DNA grafting on the Si NW networks using the functionalization process previously described (Figure 2.3) and due to the optical

detection of DNA hybridization, the DNA immobilization onto the network surface was demonstrated. An enhanced sensitivity and good selectivity for this innovative sensor were evidenced.

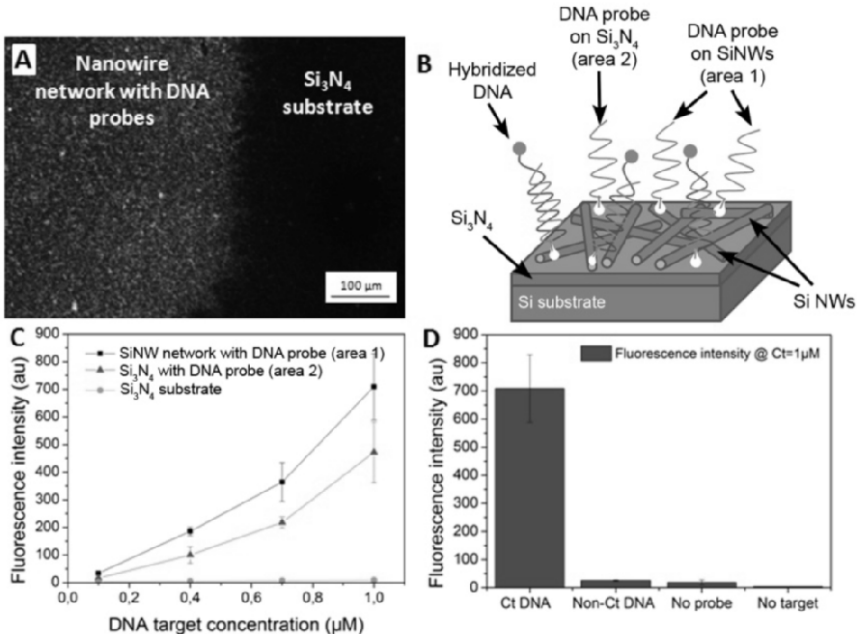

Figure 2.7. *Optical detection of the DNA hybridization with a Cy3 labeled target. a) Typical fluorescence micrograph for a target DNA concentration of 1 µM showing a signal on the Si nanonet. b) Schematic of the Si nanonet on Si_3N_4 substrate showing the DNA grafting on the NWs or on the substrate. c) Fluorescence intensity is reported versus the DNA target concentration depending on the considered surface. d) Fluorescence intensity on nanonets when exposed to complementary DNA target (Ct DNA), to non-complementary DNA target (non-Ct DNA), without DNA probe on the network (no probe) and without DNA target (no target). The data on the graphs c) and d) are from the averaged values of four independent Si nanonets which are described by the variability bars on these graphs [SER 13]*

As shown in both the typical fluorescence image of a DNA drop border (Figure 2.7(a)) and its corresponding schematic (Figure 2.7(b)), the hybridized DNA is essentially located on the Si nanonet [SER 13]. In comparison, the surface underneath Si_3N_4 surface which is not totally covered by the Si NW exhibits less fluorescence. As expected, the Si NWs are more sensitive, probably due to their higher specific area. This trend is systematically confirmed when decreasing the DNA target concentration (Figure 2.7(c)). A limit of detection as low as 10 nM was

obtained. Further optimizations to enhance the signal are under investigation by modifying the geometrical parameters of the Si nanonet.

Finally, the selectivity of the device was also tested by using non-complementary fluorescent DNA targets (non-Ct DNA) as shown in Figure 2.7(d). The non-complementary DNA signal is just slightly higher than the one of the non-specific adsorption of DNA target (no target) and more than 30 times lower than one of the complementary DNA target, demonstrating very high selectivity of the samples.

2.3.2. *Preliminary electrical characterizations of NW networks*

The final goal of the work being the electrical detection of DNA hybridization, the electrical properties of the Si nanonets are investigating as a function of morphological and geometrical parameters. In order to perform the electrical measurements, metallic electrodes with a diameter of 200 µm are deposited by e-beam evaporation through a shadow mask with variable inter-electrode distance (from 25 to 1,000 µm). After treatment with hydrofluoric acid vapor, a trilayer contact composed (from bottom to top) of 120 nm thick nickel, 180 nm thick aluminum and 50 nm thick gold (Au/Al/Ni) is deposited onto Si nanonet deposited on Si_3N_4/Si substrate as shown in Figure 2.8.

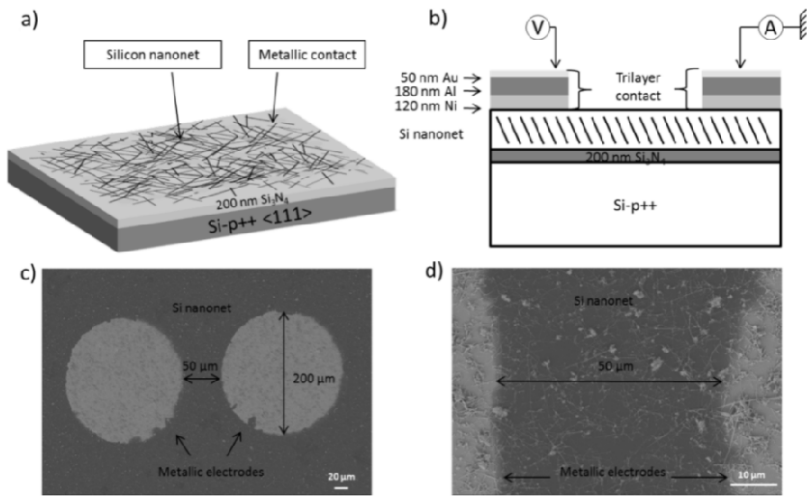

Figure 2.8. *Schematics (a and b) and SEM top view images (c and d) of the processed electrical test structure based on Si nanonet. The nanonet was transferred onto an insulating 200 nm thick silicon nitride layer. 200 µm diameter metallic contacts Ni (120 nm)/Al (180 nm)/Au (50 nm) with 50 µm pad pitch were deposited by e-beam evaporation through a shadow mask*

Whatever the type of the Si NWs (degenerated, n-doped or p-doped), the current can flow through the network [TER 13]. Figure 2.9 shows typical electrical characteristics for n-degenerated Si nanonets with density of 80×10^6 NWs.cm^{-2} (as shown in Figure 2.4(c)).

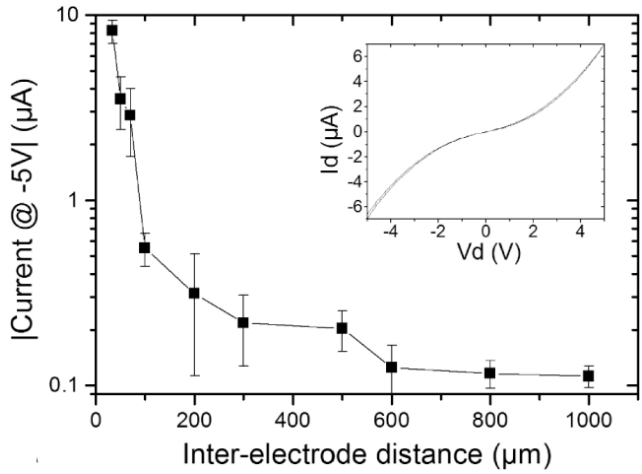

Figure 2.9. *Si nanonet electrical properties: current intensity at -5V as a function of the inter-electrode distance. The inset exhibits a typical bidirectional I–V curve for 50 µm interelectrode distance. [Voltage step 0.1 V]. Si nanonet with density of 0.8 × 10^8 NWs.cm^{-2} [TER 13]*

The inset in Figure 2.9 shows a typical bidirectional *I–V* characteristic for 50 µm interelectrode distance. Two-probe measurements at room temperature for most of these devices show nonlinear, symmetric *I–V* characteristics with a high current level despite the numerous inter-NW junctions in the nanonet. Indeed, even for the wider devices (1,000 µm) that contain several hundreds of NW–NW junctions per percolation path, the current is not negligible. Moreover, no hysteresis is observed on the *I*(V) curve. The rectifying response observed for both negative and positive applied bias suggests a back-to-back Schottky configuration that possibly originates from a potential barrier at the metal/NW junctions [CHI 12, HER 06]. Figure 2.9 displays the current as a function of the inter-electrode distance. The systematic decrease with increasing the distance between electrodes suggests that an intrinsic property of the network is measured confirming that the rectifying response is due to Schottky contact between the metallic electrode and the Si nanonet.

The influence of each step of the functionalization process (silanization, linker, ssDNA grafting) on Si nanonet electrical properties are under study. Depending on

the doping of the Si NWs (n or p), the current increases or decreases after functionalization steps. However, as of now, no clear tendency has been drawn after DNA hybridization, and our work is still in progress.

To conclude, the nanonet geometry is attractive for DNA hybridization detection. Concerning the labeled detection, the sensors based on Si nanonets exhibit an enhanced sensitivity in comparison with standard planar sensors. Moreover, the sensor specificity and reusability have also been demonstrated. These promising results open the route to a new type of DNA sensors and are the first step to the development of Si-based DNA sensors relying on the electrical detection of hybridization.

2.4. Functionalization of SiC nanowire-based sensor for electrical DNA biosensing

In future applications, NW FETs devices are expected to be integrated *in vivo* [CAS 04]. In this perspective, silicon carbide (SiC) NW is a promising substance due to the excellent physical and electrical properties of SiC. SiC wide bandgap (2.36 eV for 3C-SiC) and high electron mobility (900 $cm^2.V^{-1}.s^{-1}$ for 3C-SiC) enable the realization of efficient FETs. Also SiC exhibits high mechanical and chemical resistance. It is a biocompatible material [DEE 11a] currently used in the biomedical field as coating for implants [GON 03] or as an electrode for brain-machine interface [FRE 11]. SiC NWs are studied to enhance cellular reproduction in tissue regeneration [DEE 11b] and also for nanoelectronic in harsh or biological environments [ZEK 11, GOD 10, SEN 09]. SiC is used in various forms for different kinds of detection, planar SiC, SiC nanoparticles, nanocrystalline electrodes, and SiC NW with the purpose of protein-sensitive FETs fabrication. To the best of our knowledge, no devices taking advantages of the nanowire for electrical detection of biochemical molecules are reported.

2.4.1. SiC nanowire-based sensor functionalization process

The aim is to functionalize SiC NWs to make nanobio-FET transistors for high DNA sensitivity, as shown in Figure 2.8. In the case of a SiC nanowire-based sensor, the functionalization process described in section 2.2 (Figure 2.3) was first tested on planar and nano pillars SiC [FRA 11, FRA 13]. Therefore it should be suited to the specificities of the nanowire environment.

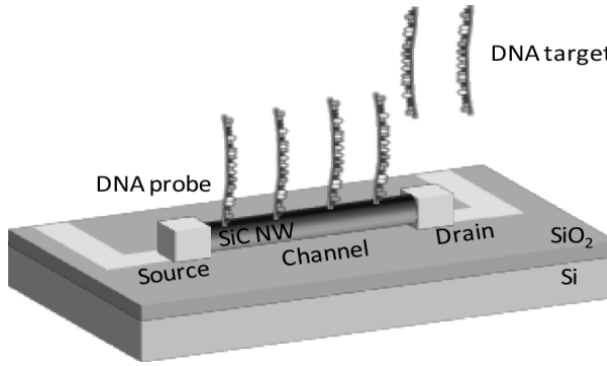

Figure 2.10. *Detection of DNA with a SiC NW FET*

The functionalization process has been performed after the device fabrication process to allow the 600°C temperature required for the nickel–gold contact annealing. The FET fabrication process is fully described in [ROG 11]. The DNA probes must be localized accurately on the nanowire to guarantee the best sensitivity. To precisely localize the DNA probes, the functionalization process is coupled with lithography and lift-off steps (Figure 2.11). Before silanization, an electrosensitive resist, polymethylmethacrylate (PMMA) diluted at 4%, is spin-coated on the bare SiC sample. A 1 μm width area is opened by electronic lithography and development along the nanowire. Then, the functionalization process is started with silanization followed by glutaraldehyde grafting. The sample is immersed in acetone for 20 min to remove the resist. After lift-off, the functionalization is ended by DNA grafting. In this study, the electronic lithography is chosen because it is possible to use the same pattern twice in the process. Optical lithography can also be used to create DNA patterns [LEN 11] but the resolution is limited. Moreover, e-beam lithography enables us to specifically functionalize areas smaller than 0.5 μm square (Figure 2.12).

In the present case, a wider area is lithographed to keep the nanowire away from the border effects. Unlike the process described in [TAN 04], the lift-off is performed after the glutaraldehyde grafting because the molecule is very reactive and will be physisorbed on the substrate if the resist is removed before. The lift-off is facilitated by the large difference between the thickness of the PMMA layer and the APTES one, 270 nm against 5–6 nm. Moreover, the immersion in acetone does not modify the properties of the organic layers including APTES and glutaraldehyde obtained from the first step of the functionalization process.

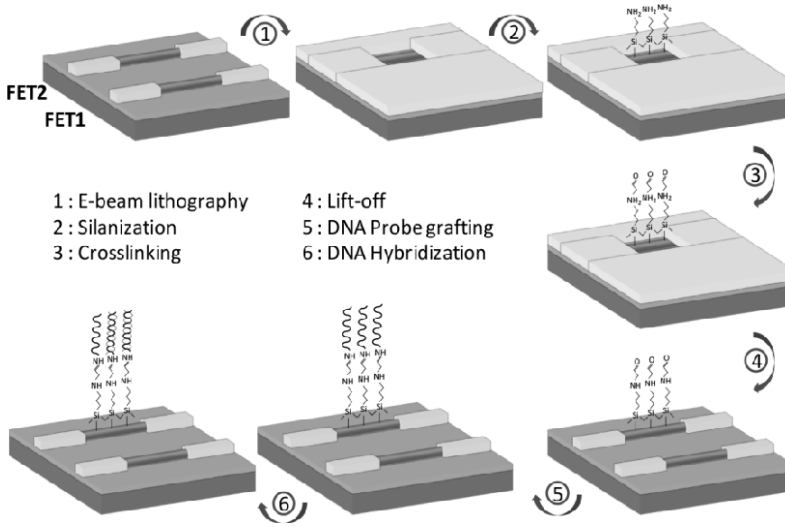

Figure 2.11. *Flow chart of the localized functionalization process used to DNA bio-modified a SiC. Two SiC NWFET are drawn: FET1 is not functionalized (reference) whereas the second one (FET2) is functionalized for DNA hybridization detection*

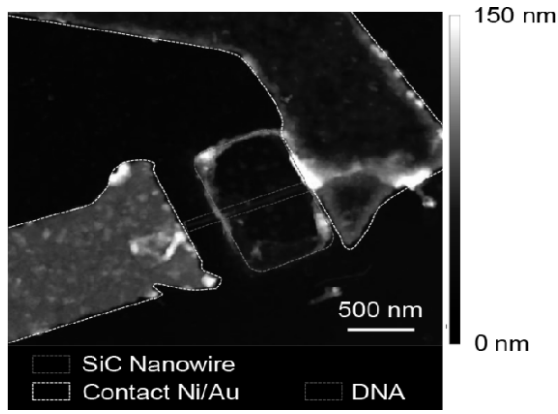

Figure 2.12. *AFM view of a DNA modified SiC nanowire contacted with metallic contacts*

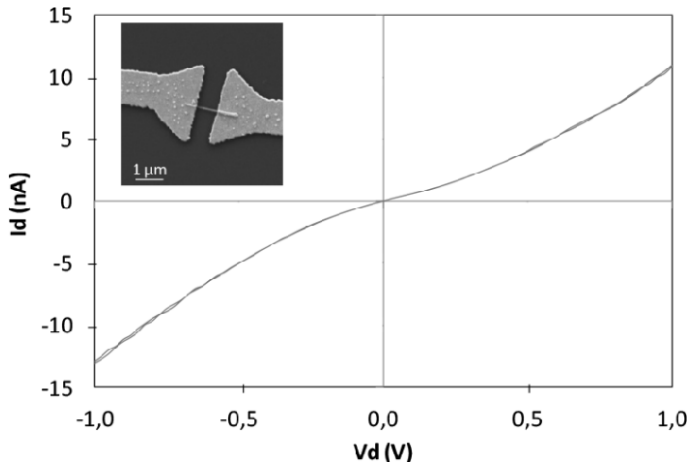

Figure 2.13. *I_d–V_d characteristics of a non-annealed SiC NWFET. The inset is a SEM view of the SiC NW (diameter 50 nm, length 2 µm) between metallic contacts (V_g = 0V)*

In a preliminary step, the electrical characteristics of the bare transistors have been studied. Figure 2.13 shows a SEM view of this transistor (see inset) and the I_d–V_d characteristic with a drain bias range of [-1;1 V]. This characteristic is typical of a transistor exhibiting a symmetric, non-ohmic behavior which is representative of NWFET with no annealed contacts. The current through the NW which acts as the channel is investigated. For a source-drain voltage of 1 V, I_d is equal to 12 nA.

2.4.2. *DNA electrical detection from SiC nanowire-based sensor*

I(V) characteristics of the SiC NW transistors are measured (Figure 2.14) between each step of the functionalization process. On a single chip, two sensors are analyzed. One transistor is functionalized, while another one is not functionalized, acting as a reference. The evolution of the current obtained at potential value of 1 V is reported (1) before and after DNA probe grafting, and (2) after hybridization (Figure 2.14). To enhance the statistic, the measurements are performed seven times at each step.

The mean value of the current falls by 22% ranging from 14.9 ± 0.09 nA to 11.6 ± 0.05 nA after the DNA probes grafting. After hybridization, the decrease is about 7%. The grafting of negatively charged DNA molecules followed by their hybridization on an n-doped NW induces a decrease in the measured current. During these two steps, the current in the non-functionalized NW FET does not change more than ±0.6%. Compared to this value, the value of 7% is significant enough to

conclude that the detection of the DNA targets is effective. It also confirms the lack of DNA molecules attached to the reference NW. The percentage ratio between the current reduction obtained from (1) DNA probe grafting and (2) from hybridization is approximately 3. Thus, it is possible to estimate that 30% of the DNA probe molecules immobilized on the NW hybridized with DNA targets. Besides, the sensor selectivity is demonstrated because the measured current does not change after hybridization of non-complementary target. Cycles of denaturation and re-hybridization are performed leading to the possibility of reusing the sensor.

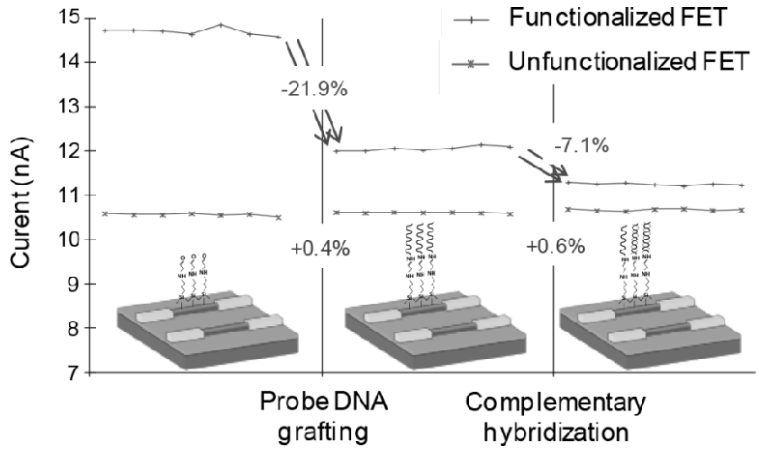

Figure 2.14. *Plot of the current of both the functionalized SiC NWFET (in blue) and the non-functionalized one (in red) during DNA attachment ($C_{DNA\ probes}$ = 10 μM, $C_{DNAtargets}$ = 2 μM). The percentages represent the variation of the mean current between the two steps*

To conclude, these results obtained on novel NW material provide bases for promising devices that fully exploit the excellent SiC properties. To further characterize this sensor, measurement with lower DNA probe and target concentrations need to be conducted.

2.5. Acknowledgments

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3

Sensitivity of Silicon Nanowire Biochemical Sensors

3.1. Introduction

As explained in the Introduction (Part 1) and Chapter 2, label-free biochemical sensors based on silicon nanowires (Si NWs) achieve selectivity to target molecules by means of a functionalization layer deposited on top of the thin dielectric that encloses the current-carrying wire. This layer consists of receptor molecules that selectively bind to the target molecules in the electrolyte. The binding process perturbs the device electrostatics and modulates the direct current (DC) or alternating current (AC) conductance (G) of the wire via surface reactions or charge displacement. The amplitude of the modulation is strongly affected by the electrolyte concentration via Debye screening effects.

The chapter is organized as follows. We first review the main definitions of sensitivity. Then, in section 3.2, we discuss the relation between sensitivity and noise. Section 3.3 discusses the main physical ingredients necessary to model and simulate the sensitivity of bio-nanosensors. Experimental and modeling investigation on the sensitivity of sensors composed of random nanoarrays is reported in section 3.4. Conclusions are summarized in section 3.5.

3.1.1. *Definitions*

Although this is not the only possible choice, many nanowire (NW) sensor readout schemes measure the DC conductance of the wire; consequently, the

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sensitivity of the sensor is typically defined as the relative change in the conductance:

$$S = \frac{G - G_0}{G_0} = \frac{\Delta G}{G_0} \qquad [3.1]$$

where G and G_0 are, respectively, the DC conductance with and without target molecules on the NW surface.

Note that if the goal is to characterize the sensitivity of the NW structure itself, then it is appropriate to use a normalized sensitivity, S_{NW}, defined as [LEE 10]:

$$S_{NW} = \frac{\Delta G}{G_0} \cdot \frac{1}{N_{ext}} \qquad [3.2]$$

where N_{ext} is either the density of charge due to the presence of target molecules at the surface of the NWs (if the molecule distribution is dense enough to be treated as a continuum) or the number of such charges (in the case of discrete localized molecules). The latter definition of sensitivity (S_{NW}) has the advantage of characterizing the detection capability of the NW, independently of the efficiency of the functionalization layer and the concentration of target molecules in the electrolyte. This is useful to optimize NW design (dimensions, doping level) and biasing. In contrast, the former definition (S) is useful to optimize the functionalization process or to study the screening effects for a given NW geometry.

Since the FET sensor is often biased at constant V_{DS} in the triode region, the conductance in equation [3.1] can be replaced by the drain current, giving:

$$S = \frac{I_D - I_{D0}}{I_{D0}} = \frac{\Delta I_D}{I_{D0}} \qquad [3.3]$$

When in the presence of positively or negatively charged analytes, the I_D (V_G) characteristics are shifted in opposite directions. The sensitivity can be estimated as the gate voltage shift in the characteristics needed to achieve the same current in both charged and uncharged cases at a given reference current I_{D0}, or equivalently voltage V_{G0}. This gate voltage shift is often referred as the threshold voltage shift, ΔV_{TH}, although it is in fact a function of the bias point, because the I_D (V_G) characteristics are not just shifted horizontally. Indeed, while staying on the same order of magnitude, ΔV_{TH} has a tendency to decrease when increasing the inversion level of the NW transistors (NWTs), i.e. ΔV_{TH} is a decreasing function of I_D or V_G. This is because the slope of the I_D (V_G) characteristics is slightly modified by the presence of the charged analyte.

To support the discussion above and compare the definitions of sensitivity (equation [3.3] or the voltage shift), we have simulated with a quantum transport model based on the non-equilibrium Green's function (NEGF) formalism the template structure in Figure 3.1 in the presence of a single (both positive and negative) charge analyte [AFZ 12], and a DNA strand [AFZ 13]. Results for the single charge analyte in air are reported in Figure 3.2. For the negative charge case, the slope of the I_D (V_G) curves is improved as the negative charge pushes the channel closer to the back gate, therefore improving gate coupling, while in the positive charge case, the charge attracts the electron channel closer to the front gate, therefore degrading back gate coupling. Since both ΔV_{TH} and ΔI_D sensitivities are related through the device drain current-gate voltage local characteristics, we see that the best current sensitivity is obtained in the subthreshold regime where this relation is exponential.

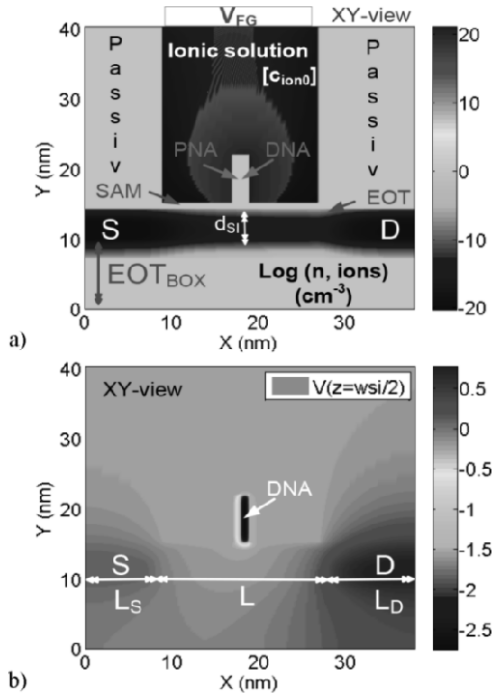

Figure 3.1. *XY-plots in the Z-plane cutting across the middle of the NW with a 20-base long single-strand DNA (with 1 negative charge/base) linked to its complementary PNA (0 charge/base) receptor on the top gate/SAM linker stack and a 25 nm surrounding 100 mM NaCl ionic solution. a) Carrier concentration (electrons, ions). b) Potential profile. V_G= -0.25 V. V_{BKG} is left floating. d_{SI} = 3 nm, L=20 nm. S/D extensions: L_S = 8 nm L_D=12 nm, V_D = 0.7 V, doping $N_+ = 10^{20}$ cm^{-3}. Oxide: Front: Al_2O_3, EOT=0.5 nm. Back: SiO_2, EOT_{BOX}. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices1.zip*

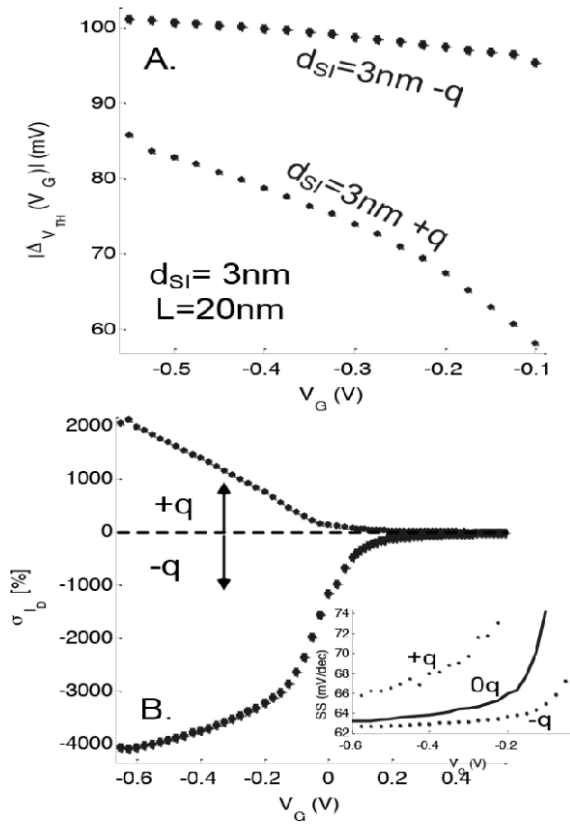

Figure 3.2. *Results of NEGF simulations of the structure in Figure 3.1 but with a single positive (+q) or negative (-q) charge as analyte in air. Plot A) Absolute value of the V_{TH} shift and B) relative current variation $\sigma_{ID} = \Delta I_D/(\min(I_{D,i})$ (%) as a function of $V_G = V_{BKG,0q}$ for a charged analyte in air. d_{SI} = 3 nm. L = 20 nm. V_D = 0.7 V. EOT = EOT_{BOX} = 0.5 nm. t_{SAM} = 0 nm. In $I_{D,i}$, the subscript i stands for the charged or uncharged case. The minimum of the charged or uncharged current is taken for the normalization to have consistent results when comparing +q and -q cases*

As we will explain in the next section and as is clear from Figure 3.2, the sensitivity depends on many parameters (including the NW bias). Values of sensitivity ranging from 1% up to factors as large as 100% have been reported in the literature for NW sensing biological species [HAH 04, STE 07a, STE 07b, ZHE 05]. Different sensitivity data are thoroughly compared in [DEV 11] considering the experimental conditions such as the pH of the buffer solution, the charge associated with the receptor and target molecules as well as their average distance from the gate dielectric.

3.1.2. *Main parameters affecting the sensitivity*

The sensitivity depends on many geometrical and material parameters of the sensor, as well as on the bias. The DC conductance of an FET sensor is often measured in the linear region and on long channel NWs. In such cases, S is not so sensitive to the applied V_{DS}.

The biasing of the fluid-gate and back-gate, instead, has a significant impact on the sensitivity, as discussed, for example, in [CHA 11]. The sensitivity is larger when the Si NW is operated just below threshold, since this operation point maximizes the impact of the sensed charge on the channel charge (and thus conductance) [CHA 11, NAI 07b]. The gate bias also has an impact on the screening induced by the electrolyte [SHO 12].

Debye screening is one of the main phenomena limiting the sensitivity: the ions in the electrolyte arrange themselves to screen the charge of the target molecules. In this respect, the higher the ion concentration in the buffer solution, the lower the sensitivity to target molecules. Unfortunately, for most analytes employed in real experiments, the ion concentration in the electrolyte cannot be reduced below a minimum level without affecting the properties of the target molecules and impeding their binding to the receptors.

The geometrical NW parameters (e.g. diameter and doping) affect the sensitivity in different ways. Thin films (or small diameter NWs) with low doping are the structures expected to provide the best sensitivity [NAI 07b, PAL 13].

We note that Si NW biosensors are sensitive to the charge concentration at the surface. Since it takes a finite amount of time for the molecules in the electrolyte to reach the surface, a severe trade-off exists between sensitivity and settling time [NAI 06, NAI 07a].

3.2. Sensitivity and noise

Diffusion of the target molecules and binding with the receptors is a random process, which results in noise when measuring the sensor characteristic [HAS 05, DEE 06].

However, noise performance of a FET biosensor has been shown to be dominated by the low-frequency noise (LFN) of the transistor itself [GO 12, RAJ 11, TAR 11]. This can originate from the intrinsic 1/f LFN of the device and the LFN associated to the contact resistance. In a well-optimized Si technology, the first source is usually dominant (excepted may be if the transistor is driven deep in

strong inversion regime) and will be considered here [RAJ 11]. For number fluctuation noise, including correlated mobility fluctuation but neglecting front-to-back gate coupling effects [ZAF 07], the current noise power spectral density is given by [GHI 91, JAY 89]:

$$S_I = \left(1 + \alpha\mu_0 \, c_{ox} \frac{I_D}{g_m}\right)^2 g_m^2 S_{VFB} \qquad [3.4]$$

$$S_{VFB} = \frac{\delta K_B T q^2 N_t}{f W L C_{ox}^2} \qquad [3.5]$$

where α, the Coulomb scattering coefficient, and δ, the tunneling attenuation distance, are for Si typically equal to 10^4 V s/C and 0.1 nm, respectively. C_{ox} is the gate oxide capacitance per unit area and WL is the area under the gate. N_t is the density of oxide traps. The other symbols have their usual meaning.

By integrating the current noise power over the measurement bandwidth (between f_1 and f_2, low and high frequency cutoff, respectively), the total integrated noise, ∂i_d, and from there the signal-to-noise ratio (SNR) can be obtained:

$$SNR = \frac{\Delta I_D}{\partial i_d} = \frac{\Delta I_D}{\sqrt{\ln\left(f_2/f_1\right)}\sqrt{S_{I\,(f=1Hz)}}} \qquad [3.6]$$

The above equation has been applied to the device in Figure 3.1, taking ΔI_D and g_m from NEGF simulations. We see that the devices biased at the front gate achieve a better SNR. One of the reasons is that the front gate area is three times bigger than the back gate area. The best case is achieved for the front case bias with grounded back gate voltage (i.e. with maximum ΔV_{TH}). This is because the equivalent gate bias noise is approximately the same for both front gate- and back gate-biased cases (the noise is dominated by the number of fluctuations and we have neglected gate coupling effects as a first approximation). Consequently, despite its higher current sensitivity, which is directly proportional to the increase of the physical input signal, the back gate floating case also features a higher current noise that leads to a lower SNR.

For the back gate-biased case with EOT_{BOX} = 10 nm, the increase of ΔV_{TH} by about a factor of 10 due to the higher EOT [AFZ 13] is more than compensated by an increase of the noise, therefore not improving the intrinsic SNR of the device itself. Such observations are supported by analogy with a detailed study for pH sensors in [GO 12], where it was found that, despite the increase of the gate voltage shift per pH (sensitivity) when using a back gate bias scheme and increasing the

EOT, the intrinsic device SNR was not improving. Such an amplification, however, can still be of interest if the overall SNR of the system is dominated by the noise of the next amplification and instrumentation stages.

Noise considerations have been used in [COU 12] to optimize arrays of nanosensors. To resolve the conflicting considerations between achieving high sensitivity and SNR, on the one hand, that push toward small nanoscale devices, and high probability of detection and low measurement time as well as compatibility with current micro-spotter technologies, on the other hand, that push toward large micro-scale devices, an array of nanoscale single analyte-sensitive detectors per spot should be used in order to increase the probability of detection and reduce the measurement time while keeping the overall single analyte detection and resolution range [COU 13].

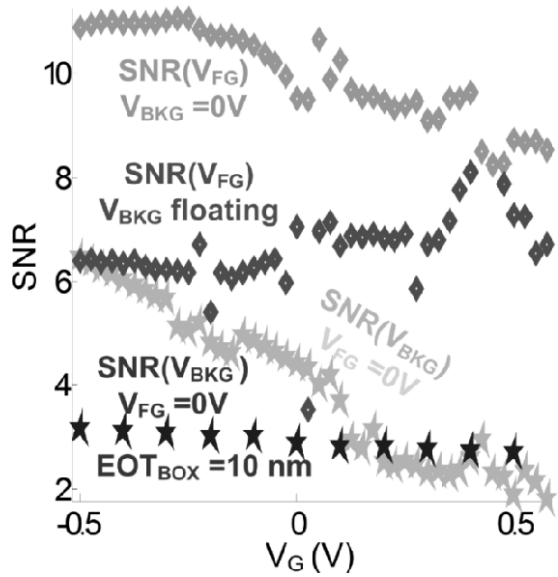

Figure 3.3. *Simulated SNR for different front ($V_G = V_{FG}$) and back gate ($V_G = V_{BKG}$) bias. d_{SI} = 3 nm. L = 20 nm. V_D = 0.7 V. V_D = 0.7 V. c_{ion0} = 100 mM. The device structure is in Figure 3.1. NEGF simulations have been used for ΔI_D, whereas the noise has been computed by integrating the noise spectrum in equation [3.6]. N_t has been set here equal to $2.3 \cdot 10^{18}$ eV^{-1} cm^{-3} which is quite typical for Si NWs [RAJ 11]. Noise is integrated between f_1 = 0.1 Hz and f_2 = 5 Hz. If not specified, EOT_{BOX} = 0.5 nm.*

3.3. Modeling the sensitivity of Si NW biosensors

Due to the complex dependence of sensitivity on bias, geometry and material parameters, the availability of advanced modeling tools can be very beneficial for the task of sensor optimization. Many approaches are currently employed in this field. In small-diameter NW sensors, quantum effects are relevant and the NEGF formalism is used [AFZ 12], as we did in Figures 3.2 and 3.3. The NEGF approach is, however, limited to short channel NWs, whereas many fabricated devices are long channel ones.

Due to low V_{DS} used in many read-outs, the sensor response can be related to the change in the channel free charges induced by the target molecules. A two-dimensional (2D) electrostatic problem in the wire section is thus adequate to describe the change in conductance. In planar sensors (i.e. nanoribbons with large width), the electrostatic problem becomes essentially one-dimensional (1D) in the section normal to transport [GO 10, CHA 11, SHO 12]. Electrolyte screening is a mandatory process in such models and, in general, the Poisson–Boltzmann (PB) equation in the electrolyte (see section 3.3.1) has to be solved together with the Poisson and transport equations in the semiconductor film, although the models in [GO 10, CHA 11, SHO 12] consider only the electrostatics in the silicon NW.

Going beyond this physical picture of the NW/electrolyte system requires coupling the drift–diffusion equation in the NW with the PB equation in the electrolyte, as done, for example, in [NAI 07b]. In principle one could use COMSOL and still have general purpose codes. Another possibility is to exploit the similarity between the equations describing positive and negative ions in the electrolyte and those for holes and electrons in a semiconductor. An "electrolyte material" is thus defined in commercial TCAD simulators [YOU 12, PAL 13]. An example of sensitivity simulations based on this approach is reported in Figure 3.4, where we see that reducing the film thickness and selecting the proper bias results in enhanced sensitivity. However, a quite large density of target charges has been considered in these calculations and, on the other hand, the concentration of ions in the electrolyte is low.

A more realistic example is reported in Figure 3.5, now considering a three-dimensional (3D) simulation and a density of target molecules of 1.5×10^{11} cm^{-2}, which roughly corresponds to 20 DNA molecules (10 receptors + 10 target molecules) per device (which is 2 μm × 50 nm in Figure 3.5). Since the molecule charge is negative, it further depletes the channel with respect to the depletion caused by the receptors, thus the conductance is reduced. The sensitivity increases at low V_{BG} because the channel is closer to depletion. The figure also shows the effect of the distance Δz between the target molecules and the receptors for different molar concentration. For Δz = 0 nm the molar concentration of the ions in the electrolyte

has a minor effect on the variation of the conductance. However, for Δz = 5 nm the sensitivity becomes essentially zero at high ion concentration. In fact, whereas for c_0 = 1.5 mM the Debye length in the electrolyte is λ_{el} = 8 nm and thus comparable with Δz, for c_0 = 150 mM we have λ_{el} = 0.8 nm.

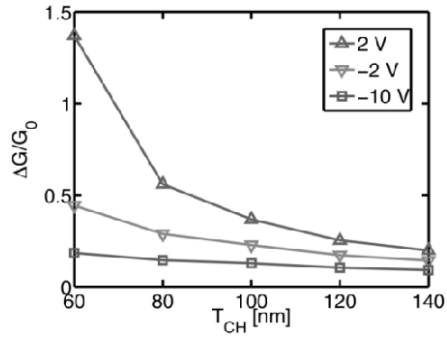

Figure 3.4. *Normalized change of conductance for an SOI device (T_{OX} = 10 nm, T_{BOX} = 600 nm, L = 10 μm, $N_A = 10^{17}$ cm^{-3}) at low V_{DS} as a function of the silicon film thickness. The charge concentration of target molecules per unit area is 10^{13} cm^{-2} (modeled as a uniform layer with thickness 5 nm and dielectric constant equal to $2\varepsilon_0$ placed on top of the gate oxide). The ion concentration in the electrolyte is 10^{-7} M. Different fluid-gate biases are considered*

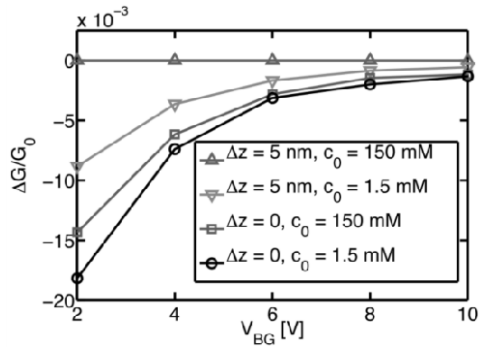

Figure 3.5. *Relative change of conductance induced by a uniform layer of charge mimicking the target molecules bound to a uniform layer of charged receptors as a function of the back-gate voltage for a nanowire with L = 2 μm, T_{OX} = 2 nm, T_{CH} = 100 nm and a width W_{CH} = 50 nm. Doping is $N_A = 10^{16}$ cm^{-3}. The symbol Δz indicates the distance between the 1 nm dielectric layer mimicking the charged target molecules and the top of the 1 nm layer mimicking the charged receptors (electrolyte is assumed in between). V_{DS} = 1 V and V_{FG} = -0.2 V (fluid-gate voltage which maximizes the sensitivity, keeping the device channel close to depletion). The density of charge in the two layers is 1.5×10^{11} cm^{-2}. The sensitivity (as defined in equation [3.1]) here is much smaller than in the previous figures, but this is consistent with the much lower density of charged molecules. To compare structures with different concentration of receptors, we should indeed use equation [3.2]*

3.3.1. *Modeling the electrolyte*

Models based on a description of the electrolyte as a continuum medium are mostly based on the PB equation. For a Z:Z electrolyte, the electrostatic potential V is given by (in 1D, for simplicity):

$$\varepsilon \frac{dV^2}{dx^2} = -qZ\left(c^+ - c^-\right) \qquad [3.7]$$

where the permittivity ε of the electrolyte is often assumed to be constant, although in reality a high electric field at the interface gives rise to a preferential polarization of the water molecules, so that the local permittivity is reduced [GON 12]. The ion concentrations are given by

$$c^{\pm} = c_0 \exp\left(\mp \frac{Zq\left(V - V_{ref}\right)}{k_B T}\right) \qquad [3.8]$$

where c_0 is the concentration in the bulk of the solution, where the electrostatic potential is set to V_{ref}.

Linearization of equations [3.7] and [3.8] gives the expression for the Debye screening length [KOH 06]:

$$\lambda_D = \sqrt{\frac{\varepsilon k_B T}{\sum_{m_a}\left(Z_m q\right)^2 c_{0m} + \sum_{m_c}\left(Z_m q\right)^2 c_{0m}}} \qquad [3.9]$$

where we consider m_a anion species and m_c cations.

Equation [3.8] does not model volume exclusion and steric effects due to the finite size of the ions at the electrolyte/dielectric interface. These mechanisms are accounted for by the modified Poisson–Boltzmann (MPB) equation [BOR 00]:

$$c^{\pm} = \frac{c_0 \exp\left(\mp \dfrac{Zq\left(V - V_{ref}\right)}{k_B T}\right)}{1 - 2c_0 a^3 + 2c_0 a^3 \cosh\left(\dfrac{Zq\left(V - V_{ref}\right)}{k_B T}\right)} \qquad [3.10]$$

where ions are treated as hard spheres with radius a.

Comparison between PB and MPB is reported in Figure 3.6: the steric effects are very important at high ion concentrations and high applied voltages (where $\frac{4}{3}\pi a^3 c^{\pm} >> 1$) and the PB theory gives unphysical results in this regime. Furthermore, Figure 3.6 shows that the insertion of a dielectric "compact" layer can somehow mimic the steric effects when the PB equation is used, thus avoiding excessively large surface concentrations [PAL 13]. The discrepancy between PB calculations without compact layers and the other two models is especially large in close proximity to the electrode.

Advanced models for the electrolyte also in AC excitation conditions have been presented for nano-electrode arrays [PIT 12, PIT 13a, PIT 13b]. The same degree of accuracy should be employed also for Si NW, in particular when considering AC readouts going beyond the limitation of the DC conductance measurements (see Chapter 5 of Part 1 in this book).

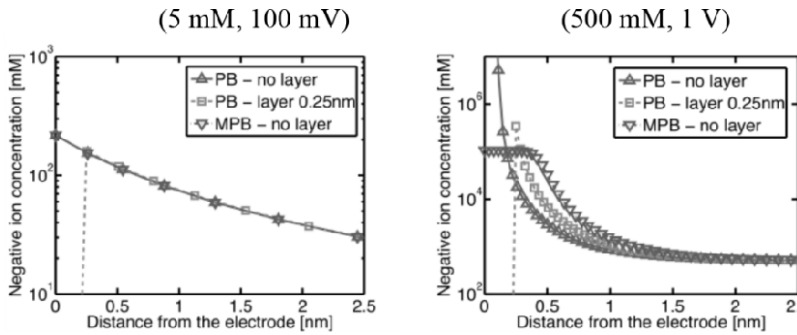

Figure 3.6. *Relative ion concentration in a 1D structure consisting of an electrolyte with an electrode on the bottom (y = 0) and a fluid gate on the top. The solution of the PB with and without an insulating layer with the thickness of the typical Na+ or Cl- ion radius (a = 0.25 nm) is compared to the numerical solution of the MPB*

Another important model ingredient is the inclusion of chemical reactions at the electrolyte/oxide interface. In fact, although usually in negligible concentration when compared to other ions in buffered solutions, the natural water ions, and in particular H^+, are of importance in order to account for the pH and voltage-dependent surface charge density at the oxide–solution interface [HAL 96]. The surface charge density (σ_0) can be computed using the site-binding model [YAT 74]:

$$\sigma_0 = q.N_S \frac{a_{H_S^+}^2 - K_a K_b}{K_a K_b + K_b a_{H_S^+} + a_{H_S^+}^2} \qquad [3.11]$$

where K_a and K_b are the dissociation constants and N_S is the concentration of available surface sites. The surface concentration $a_{H_S^+}$ of H+ ions can be computed solving a PB equation for such ions, although it can also be simply found as the bulk H+ ions concentration (which is related to the pH of the solution) multiplied by $\exp[-\Delta V/(k_B T)]$, where ΔV is the voltage drop between the bulk of the electrolyte and the interface. If the oxide interface is not properly passivated, this charge can strongly reduce the sensitivity of the NW. Recent experimental results have shown an important reduction of NW response to pH after alkyl-silane functionalization that is consistent with a reduction by 3 orders of magnitude of the density of available oxide sites N_S [TAR 12]. NEGF simulations in [AFZ 13] have shown that in this case the original S (without oxide charge) can be restored.

3.4. Sensitivity of random arrays of 1D nanostructures

As introduced in the Introduction (Part 1) and Chapter 2, random arrays of NWs can lead to the fabrication of low-cost sensors. However, the analysis of their electrical response to DNA hybridization is not straightforward. Going beyond the simple observation of a change in current may allow us to quantify the amount of hybridized DNAs but this requires the ability to precisely characterize the field-effect (FE) mechanisms that govern the electrical response to a change in the external charge.

In such random arrays, the FE mechanisms are quite different from what is normally observed in standard MOS transistors. In particular, the number of NWs which experience a change in their internal electron charge is quite different from the number of NWs that are effectively conducting current between the electrodes. Most extraction methods [MOU 10] make the assumption that these numbers are the same. This is completely justified for standard FE device operation where the channel is both the region where free carries are accumulated and the region where current flows. In contrast, in a random array of NWs, any NW that is contacted electrically to at least one electrode, even by a very resistive conducting path, has its free carriers charge modulated by the application of an external electrostatic control. However, some of these NWs will probably carry no current, giving a negligible contribution to detection mechanisms based on current measurements. Indeed, the only NWs that contribute effectively to the current modulation are those placed on a small resistance path between the electrodes. The difference between these two populations of NWs directly influences the sensitivity of the sensor. Sensitivity thus strongly depends on percolation effects, which are influenced by several parameters, essentially the areal density of NWs and the

geometry of the device (distance between the electrodes and device width). In order to analyze these effects in detail, we will consider thin film transistors (TFT) fabricated on a random network of carbon nanotubes (RN-CNT) as in Figure 3.7.

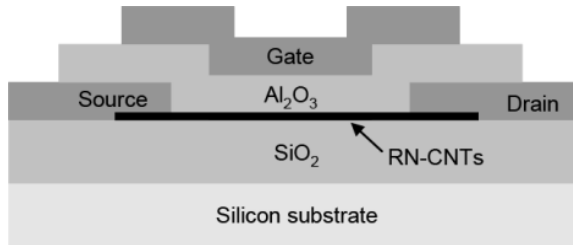

Figure 3.7. *Schematics view of the devices with random network of carbon nanotubes under study*

Devices under study are incorporating a top gate. In the case of an FE sensor, this top gate would, of course, be removed and current modulation would be obtained by changes in the charge at the surface of the NWs instead of changes in the charge of the capacitive gate or (as shown further with the LNS study) changes in the charge trapped at the interface between CNTs and gate insulator. All three mechanisms have being driven by Fes in common, and it is the purpose of this section to analyze how they can be affected by percolation effects in random networks of 1D structures.

3.4.1. *Electrical characterization*

Analysis of static *I–V* characteristics allows simple extraction of most parameters that characterize the FE operation, especially the conductance gain β which gives the linear dependence of channel conductance with gate voltage V_{GS} in the ohmic regime of operation of the transistor. With a simplified model of the transistor, β is equal to:

$$\beta = \frac{W}{L} \cdot C_{ox} \cdot \mu_0 \qquad [3.12]$$

It can be easily extracted using the *Y* function method, which has the advantage of suppressing the artifacts arising from series resistance effects at the source and drain contacts, among others [GHI 88]. A key parameter of β is the oxide capacitance C_{ox} of the top gate. The other parameters are the low field mobility

μ_0 and the length L and width W of the channel. In standard FE devices, C_{ox} is either calculated, using the plate capacitance model (C_{2D}) which assumes that charge control is uniform, or measured, using the split CV method [SOD 82]. The latter method consists of measuring gate-to-channel capacitance C_{gc} for gate voltage V_{gs} varying from accumulation to inversion. The variation of capacitance between these two regimes gives an experimental evaluation (C_{exp}) of C_{ox}. In the case of RN-TFTs, it was concluded that the plate capacitance does not necessarily give a good evaluation of the experimental capacitance value. However, due to the quite high density of CNTS used in these experiments (20 CNT/μm^2), which was above the percolation threshold, the plate model under-estimated the experimental value by about only 20% in the devices under study [JOO 12, JOO 13b].

Despite their agreement, neither of these values may be valid for the analysis of current control because all the CNTs that are charged are not necessarily involved effectively in current conduction between the electrodes. This will be further analyzed with the support of LFN measurements in next section.

3.4.2. *Low-frequency noise characterization*

It has been shown that the LFN is an important parameter, which affects the detection limit of a sensor [LEE 10]. We used the same devices as in previous sections to analyze LFN [JOO 12, JOO 13b]. First, it was checked that in these devices, LFN was originating from trapping/detrapping effects at the surface of the CNTs or at their junctions. Indeed, the power spectral density of drain current noise was well fitted by a carrier number fluctuation model with correlated mobility fluctuations [GHI 91]. Using this model, trap density values in the range of 10^{15} cm^{-2} eV^{-1} were extracted, whether with the plate capacitance model or with the experimental value C_{exp}. In contrast, the density of interface traps extracted from $I_d(V_{gs})$ characteristics in the sub-threshold regime (from the sub-threshold slope) was instead in the range of 5×10^{13} cm^{-2} eV^{-1} for the same devices. There is thus a large discrepancy, of about a factor of 100, between the evaluation based on LFN and the direct evaluation from current–voltage curves [JOO 13b]. The main factor that explains this discrepancy is most probably the inaccurate evaluation of gate capacitance. This will be further analyzed in the following section.

3.4.3. *Simulation of electron conduction in random networks of 1D nanostructures*

In order to get a better understanding of percolation effects and of their influence on the difference between charge control and current control in random networks, we carried out a simulation analysis [JOO 13a]. The simulation framework is based

on the assumption that CNTs can be considered as stiff 1D conductors with a homogeneous distribution in space. Such a model may hold for any quasi-1D nanostructures, including NWs, such as those presented in previous sections. Random networks were generated by a Monte Carlo procedure where the position and orientation of each 1D nanostructure (sticks in Figure 3.8) was randomly selected. The number of nanostructures was set by the product of the areal density of nanostructures ρ_{CNT} by the active region area $W \times L$. In this study, the CNT length was kept constant for simplicity (L_{CNT} = 1 µm). The numerical procedure involves several steps: locate junctions positions, calculate all the distances between adjacent junctions, identify the CNTs that are directly connected to an electrode build an ordered connectivity matrix of the network, identify all the paths that connect one electrode to the other, and finally identify both the shortest paths (from a geometrical point of view) and the less resistive paths (from a current conduction point of view). The less resistive paths (red paths in Figure 3.8) were found using a modified Floyd's algorithm [COR 01]. We also accounted for the junction resistance between nanostructures and for the conductivity of the nanostructures, which was used to compute the resistance of each segment [JOO 13a]. A Spice equivalent circuit of the network was then built based on the connectivity matrix. Several conclusions can be drawn from these simulations.

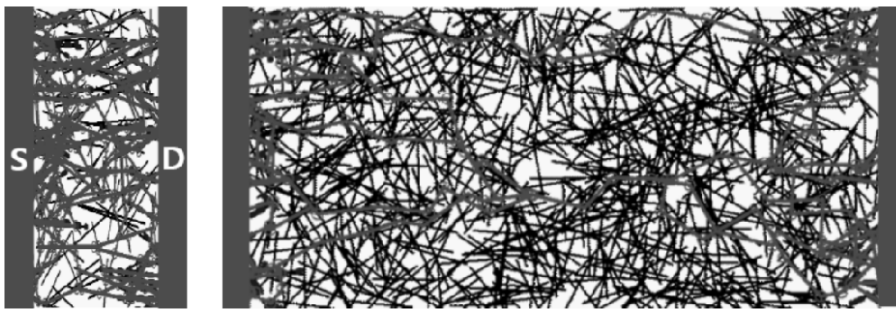

Figure 3.8. *Representative examples of random networks generated by Monte-Carlo simulation. Low resistance paths are highlighted in red. Inter-electrode distance, L_{mask}, is equal to 2 µm (left) or 10 µm (right), respectively. In both cases, W_{mask} = 5 µm, ρ_{CNT} = 20 µm^{-2}, L_{CNT} = 1 µm. Blue sticks correspond to CNTs that are connected to one of the electrodes, while red sticks visualize the conduction paths of minimum resistance. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices1.zip*

First, as expected, the percolation probability P, i.e. the probability that there is at least one path connecting the two electrodes, is increasing with ρ_{CNT}, $1/L$ and W. The percolation probability was well fitted by a modified error function of the areal density of CNTs [JOO 13a].

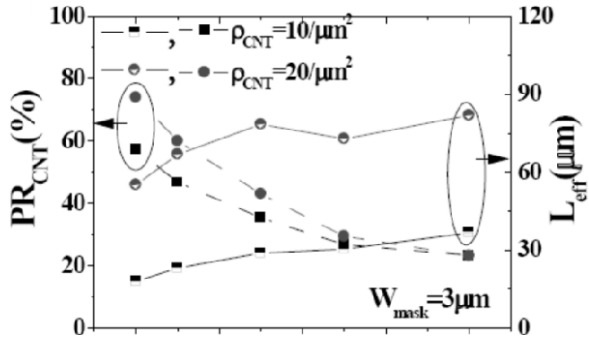

Figure 3.9. *Percentage (PR_{CNT}) of CNTs which are on a small resistance path and total developed length (L_{tot}) of these current paths as a function of inter-electrode distance L, for two values of the areal density of 1D nanostructures*

From these simulations, we calculated the percentage PR_{CNT} of CNTs that are effectively involved in current conduction. This percentage saturates quite rapidly with W. In contrast, it strongly decreases when L increases (Figure 3.9), which means that less CNTs are involved in current control mechanisms in long devices. We also calculated the total developed length L_{tot} of the less resistive paths. This parameter was used to calculate the equivalent number (N_{ch_sim}) of parallel paths per unit of device width with equivalent length L: $N_{ch\_sim} = (L_{tot}/L)/W$. For comparison, we also calculated the number of paths per unit of width which can be deduced from the plate capacitance model, $N_{ch\_C2D} = C_{2D}/C_{1D}$, and the one which can be deduced from the experimentally measured C_{ox} value, $N_{ch\_exp} = C_{exp}/C_{1D}$. In these expressions, C_{1D} is the linear capacitance of a CNT and is essentially a function of its diameter (which is the range of 0.8 nm–1.2 nm in this experiment) as:

$$C_{1D} = \frac{2\pi\varepsilon}{\cosh\left(\frac{2t}{d}\right)} \qquad [3.13]$$

where ε and t refer to gate dielectric layer permittivity and thickness, and d to CNT diameter. The comparison between these three evaluations is displayed in Figure 3.10, which clearly shows the influence of percolation effects in decreasing the number of paths between the electrodes when inter-electrode distance, L, increases.

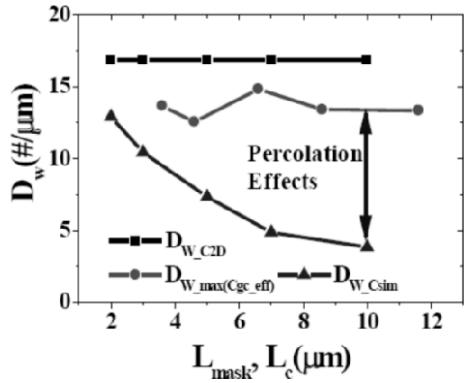

Figure 3.10. *Comparison between three different evaluations of the equivalent number of independent channels, based on the 2D plate capacitance model (squares), on the experimentally measured value of C_{ox} (circles) and from simulation (triangles). Influence of percolation effects increases as inter-electrode distance L increases*

3.4.4. *Discussion*

With the support of simulation results, we recalculated the density of traps N_{st}, extracted from LFN measurements, and the interface trap density D_{it}, extracted from subthreshold slope. The value of the capacitance used for N_{st} extraction was now the 1D capacitance corresponding to the total number of CNTs connected to either source or drain. By doing so, the extracted values of N_{st} and D_{it} were now lying within one decade instead of more than two. We think that this residual difference is due to the assumption of independent parallel channels in the estimation of N_{ch_sim}, while, as seen in Figure 3.8, realistic paths can share many sections. In fact, for the tested range of geometries and CNT areal density, we found that the best estimation of C_{ox}, which allowed N_{st} and D_{it} to become equal, was in fact C_{1D}/W. Trap density values were then reaching reasonable values, around a few 10^7 cm^{-1} eV^{-1} [JOO 13b]. This 1D capacitance model should be employed for parameter extraction to correctly account for percolation effects. The same capacitance model should be used to quantify in a reliable way the amount of grafted charges in sensors based on random networks of 1D nanostructures out of conductance measurement.

3.5. Conclusions

To summarize, we have reviewed and analyzed many aspects related to the sensitivity of biosensors based on NWs. First, we have seen that many definitions of sensitivity are possible, based either on the perceptual change of conductance (or drain current) in the presence of target molecules or on the associated voltage shift.

The sensitivity depends on many geometrical parameters, on the biasing and on the ion concentration of the electrolyte. Short channel, thin NWs operating close to threshold is the option which provides a good noise/sensitivity trade-off, preferably in arrays, in order to obtain measurable signals and increase the chances to capture molecules. These arrays can be well organized (top-down fabrication, meaning well controlled) or random (bottom-up fabrication, implying low cost). Interface quality is critical. Electrolyte screening degrades the sensitivity, requiring buffer solutions with low ion concentration and pushing toward the use of AC readouts.

Accurate models for the sensor sensitivity have been developed and used for sensor optimization. Such models feature specific ingredients to correctly describe the electrolyte screening accounting for the finite size of the ions, to include the charge induced by chemical reactions at the interfaces and to describe percolation effects in random arrays. Models have allowed us to obtain a better understanding of how to optimize the sensor sensitivity and the SNR. For example, sensing based on the back-gate increases the sensitivity but also the noise so that the SNR is not significantly improved with respect to sensing at the fluid-gate. Accurate AC models will become useful to design and optimize AC readout strategies to overcome Debye screening.

3.6. Acknowledgments

Pierpaolo Palestri, Luca Selmi and Federico Pittino would like to thank Professor David Esseni (University of Udine, Italy) for many helpful discussions. Many thanks to Massimo Gallon, Federico Saccon, Paolo Scarbolo and Riccardo Sette for their help in the simulations of section 3.3. Mireille Mouis and Gérard Ghibaudo would like to thank Massimo Mongillo, who is currently at CEA/LETI, Grenoble, France, and who contributed to this work during his postdoctoral research at IMEP-LAHC, Grenoble, France, with the support of the NanoFunction Network of Excellence.

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4

Integration of Silicon Nanowires with CMOS

4.1. Introduction

Silicon nanowires exhibit attractive characteristics that have motivated their use as the sensor element in a biochemical sensor system. These characteristics include large surface-to-volume ratios (enabling high sensitivity), comparable size to molecules (enabling small sampling volumes), label-free detection (avoiding fluorescence tagging) and the possibility to integrate multiple devices (enabling reduced size and low systems cost). A full biochemical sensor system is rather complex and needs to physically interact with an electrolyte solution. Further system requirements are also needed to accurately and reliably transform the analyte concentration into an electrical signal and finally present the measured concentration in a comprehensible way to the user. It has been shown (see Chapter 1) that it is possible to fabricate silicon nanowires on a silicon wafer using conventional process technology employed in the semiconductor industry. In the research community, silicon nanowires are often fabricated on a chip and connected to the electrolyte solution through micro-fluidic channels. Isolated electrical connections to the silicon nanowire chip enable the connection of a read-out chip or to an external current/voltage meter. Chapter 5 describes a system that exploits a full nanowire impedance mapping as a function of measurements frequency of the silicon nanowires. Although the small silicon nanowires are used as the basic sensor element in such a system, the system itself becomes area consuming, and it is still a challenge to realize a small-sized handheld system. By full integration of silicon nanowires onto the same chip as the *complementary metal–oxide–semiconductor* (CMOS) circuits, it is possible to truly realize small-size systems with its benefits of reduced cost and increased mobility. Adding CMOS circuitry to

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the same chip as the fabricated silicon nanowires will also allow multiple advanced on-chip functions, e.g. electrically selectable individual silicon nanowires, reference signal monitoring and advanced readout methodologies. An integrated silicon nanowire and CMOS circuit chip would also allow more design freedom with respect to interaction with the full biochemical sensor system, including interaction with the electrolyte solution.

4.2. Overview of CMOS process technology

The CMOS fabrication process is divided into two parts, called the front-end-of-line (FEOL) and back-end-of-line (BEOL) processing. In the FEOL, the active components (the p-channel and the n-channel transistors) are fabricated. Following the transistor fabrication, isolation layers and several metallization layers are employed in the BEOL to electrically connect the transistors and to fabricate bond pads for connection to the outside world. The total thickness of the inter-metallic dielectric is about 1–4 μm thick depending on the number of metallization layers. In the FEOL, high-temperature processing (T ~500–1050°C) is possible for material depositions and activation of dopants in single-crystalline Si. The transistors are fabricated on single-crystalline Si wafers (called bulk Si CMOS) and the transistors are then isolated by p-type and n-type regions in the Si wafer. Alternatively, transistors can also be fabricated in the single-crystalline layer of a silicon-on-insulator (SOI) wafer. Then the transistors are isolated by the insulating dielectric (usually SiO_2) surrounding the transistors and the silicon layer can have a low doping concentration (~10^{15} cm^{-3}). Thus, it is possible to fabricate isolated, low doped, single-crystalline Si nanowires in the thin silicon layer of an SOI wafer. In the BEOL, the permitted temperature budget is restricted (T_{max} ~450°C) due to the metal layers that already exist on the wafer. The limited temperature budget and the fact that the inter-metallic isolation layer is an amorphous dielectric make it challenging to fabricate the single-crystalline silicon nanowires after the BEOL process.

4.3. Integration of silicon nanowire after BEOL

It is highly desirable to integrate new functionalities as late as possible in an advanced CMOS chip fabrication process in order to interfere as little as possible with the transistor performance and to keep extra costs at a minimum. A relatively straightforward scheme to integrate silicon nanowires with CMOS circuits is to add silicon nanowires to a prefabricated CMOS chip. This is an attractive approach, because the design and the fabrication of the CMOS chip can be made using standard semiconductor foundries in the exact same way as a CMOS chip made for electronic applications. This approach has, in particular, been used in biotechnology

applications, where metal electrodes are used for biosensing, e.g. multi-electrode arrays for neuroscience and cell-based biosensors [GRA 11]. The geometrical size and shape of the electrode arrays are then designed and implemented in the top-level metal layer of the CMOS chip. Post-CMOS processing is relatively simple and involves only opening up passivation layer to the electrodes and to isolate the bond pads in the package from the active sensor area. In the case of integration of silicon nanowires, the situation is more complex since the silicon nanowires have to be connected to predefined contact areas in the top metal layer. Normal silicon processing used in the FEOL is not possible to use since several key processes, such as silicon growth and dopant activation, involve temperatures above the maximum temperature that the BEOL metallization layers can withstand. Therefore, the silicon nanowires have to be defined on another substrate and then transferred to the prefabricated CMOS chip or wafer. Silicon nanowires fabricated with bottom-up approaches are often transferred to substrates with predefined contacts for electrical evaluation and the same methods can be used to transfer silicon nanowires to prefabricated CMOS chips. However, the transfer methods are often manual processes, i.e. they are very time-consuming and do not lend themselves to a low-cost biosensor fabrication process. Potentially, the transfer of a large number of silicon nanowires to the electrode contacts using the vacuum filtration method (see Si nanonet assembly in section 1.4.2) can be a cost-efficient method for integrating silicon nanowires with CMOS circuits in a post-CMOS process scheme.

4.4. Integration of silicon nanowires in FEOL

Silicon nanowires can also be integrated with CMOS circuits by fabricating the silicon nanowires in the FEOL in a CMOS process. Huang *et al.* used the heavily doped polycrystalline silicon layer available in a commercial 0.35 μm bulk-Si foundry process to realize silicon nanowires in a biomolecular sensing chip [HUA 13]. Access to the polycrystalline layer was achieved by etching an opening in the dielectric layers used in the metallization stack. This integration scheme is a low-cost scheme, but the quality of the silicon nanowires as sensing elements is questionable due to their high doping concentration, polycrystalline nature and relatively large size (170 nm height and 625 nm width).

Single-crystalline silicon nanowires are typically made in the thin (<50 nm thick) silicon layer of a SOI wafer. We have investigated the integration approach to merge the silicon nanowire fabrication into a fully depleted SOI CMOS process where the metal-oxide-semiconductor-field-effect-transistor (MOSFET) channel is made in the thin silicon layer of the SOI wafer [JAY 13]. This allows us to simultaneously define the MOSFET channels and the silicon nanowires for sensing, thus enabling a potentially low-cost integration scheme. The silicon nanowires were defined with conventional I-line stepper lithography and the sidewall transfer lithography (STL)

(see the STL process in section 1.3) technique that enables a vast amount of silicon nanowires to be fabricated using conventional lithography combined with deposition and etching processes. We have implemented the STL process in a cluster tool equipped with chambers for reactive ion etching (RIE) and plasma-enhanced chemical vapor deposition (PECVD). The cluster tool allows for PECVD deposition of SiO_2, SiN and amorphous Si at 400°C in one chamber, and SiO_2 and SiN RIE in a separate chamber. A third chamber is used for the Si RIE. The ability to deposit and etch all involved layers in one tool allows the STL process to be reliable and with a good throughput.

The full silicon nanowire and CMOS process flow is depicted in Figure 4.1. The key feature of the integration scheme is that the silicon nanowires are defined in the single-crystalline Si layer, used as channel materials in the MOSFETs, thus enabling integration of Si nanowires with good quality for biochemical sensing.

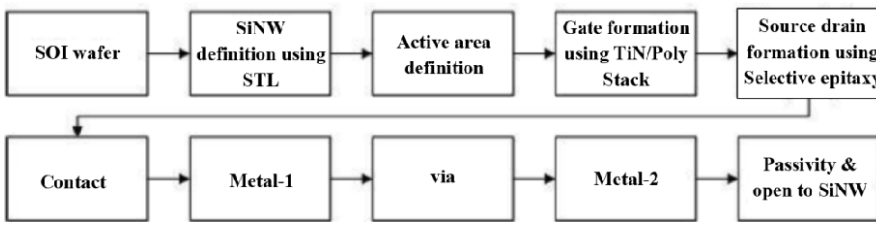

Figure 4.1. *Process flow of silicon nanowire integration in a fully depleted CMOS process. Using sidewall transfer lithography (STL), the silicon nanowires are defined in the silicon layer used as channel for the MOSFETs. At the end of the process, the metal interconnects are passivated and locally holes are etched in the passivation layer to enable access of the electrolyte solution to the silicon nanowires*

After MOSFET gate formation using TiN/polysilicon stack, a two-layer stack consisting of 10 nm PECVD SiO2 and 20 nm PECVD SiN is deposited uniformly over the silicon nanowires and MOSFET devices. As seen in section 4.2, this double layer deposition is performed to mask the silicon nanowires (Figure 4.2(c), left), and to create spacer structure for the MOSFET devices used in the biosensing control array (Figure 4.2(c), right). The source and drain openings are defined using lithography and the SiO_2/SiN stack is dry etched. A 40 nm thick, *in situ* doped SiGe was selectively deposited on the source and drain regions of the silicon nanowires as well as the MOSFETs (Figure 4.2(c)). The SiO_2 on top of the MOSFET gate and the SiN on top of the SiNW act as a mask for the selective SiGe growth.

Following the SiGe epitaxy growth, a second two-layer stack consisting of 20 nm PECVD SiO_2 and 60 nm PECVD SiN is deposited uniformly over the wafer (Figure 4.2(d)). This layer will act as a second-spacer before silicide (NiSiGe)

formation. A 400 nm SiO_2 dielectric stack was deposited with PECVD and the contact was patterned and etched down to the silicide layer. The interconnects were fabricated with physical vapor deposition of 460 nm Al on top of 100 nm TiW. After completing the MOSFET fabrication and metallization, a hole is opened up in the passivation layer locally where the silicon nanowires are located. The electrolyte solution thus will not be in contact with the metal interconnects nor the contacts to the silicon nanowires, but will only expose the silicon nanowires. At the edge of the die, openings were made to the Al bond pads. At the end, a forming gas anneal (10% H2 in N2) at 400°C completed the process.

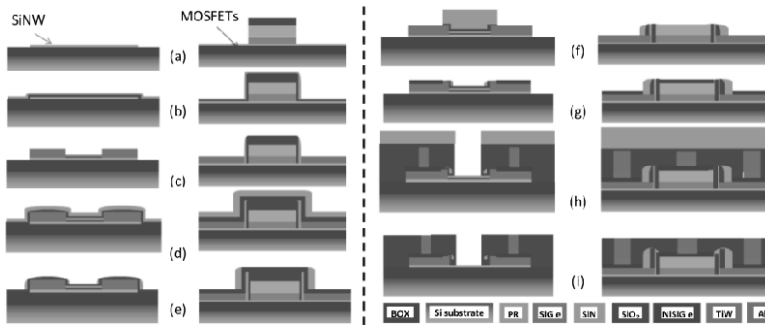

Figure 4.2. *Schematic cross-sections of the two structures: (left) silicon nanowires and (right) MOSFETs using in situ doped SiGe, NiSiGe, first-level metallization and passivation. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

4.5. Sensor architecture design

A CMOS process that allows the integration of silicon nanowires, as described in the previous section (section 4.5), offers a vast amount of design opportunities to enhance the performance of the silicon nanowire-based sensor. Much more advanced read-out methodologies than only measure the change in silicon nanowire conductance can be employed. In Chapter 5, a circuit for measuring the impedance as a function of measurement frequency is described. In this chapter, we describe a sensor design that allows measurement of the conductance variations of biosensitive silicon nanowires in a serial manner by using on-chip integrated CMOS circuitry. The biochemical sensor consists of a 32 by 32 array of pixels. Figure 4.3 shows the layout of a single pixel and Figure 4.4 depicts a simplified circuit diagram of the sensor. Each pixel consists of one silicon nanowire, one fluid gate and one PMOSFET for row selection. There is an opening in the passivation layer to let the electrolyte solution to only be in contact with the silicon nanowire and the fluid gate. The pixel size is 16 by 16 μm^2. Horizontal and vertical shift register is used to select individual silicon nanowires in the *n* by *n* matrix by sequentially selecting row and

column. The circuitry consists of eight input/output pins, V_{DD} and V_{SS} for supply voltage, clock signal, enable signal to the shift registers, fluid gate, back gate and V_{ref} is used to set V_{DS} of the silicon nanowires. The output pin I_{OUT} is used to measure the current through the silicon nanowire. The fluid gate and the back gate set the bias point of the silicon nanowires. The shift registers select the pixels in a sequential manner and the current in each silicon nanowire is read out by sensing the current I_{OUT} in the time domain. Since typical response times of charge-based biochemical sensors are in the order of seconds or more, the sensor will be able to read all individual silicon nanowires in real time, even using mature CMOS technology with 0.5 µm gate length.

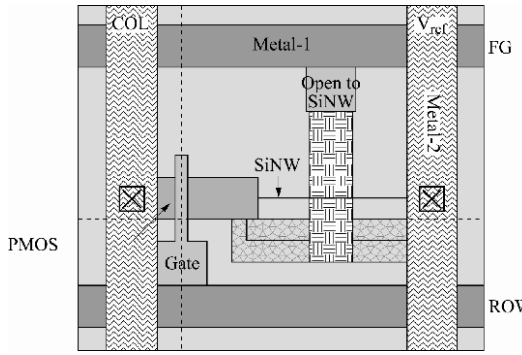

Figure 4.3. *Layout of a single pixel showing the silicon nanowire, metal layers, PMOSFET and fluid gate. The isolation layers are open locally to the silicon nanowire allowing the electrolyte solution access to the fluid gate and the silicon nanowire*

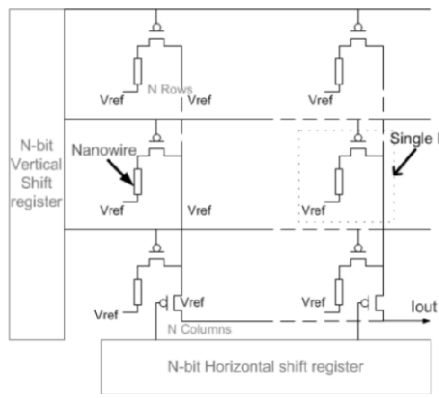

Figure 4.4. *A simplified circuit diagram showing each pixel with its silicon nanowire and select transistor. Vertical and horizontal shift registers are used to sequentially address each pixel and read the current (I_{OUT}) through the nanowires*

An N by N array needs an N-bit horizontal and vertical shift register to select the individual pixel. For example, a 32 by 32 array needs a 32-bit horizontal and a 32-bit vertical shift register as shown in Figure 4.5. The shift register is realized using a positive edge triggered D-type flip-flop with set and reset. The output of the horizontal shift register is connected to the input of the vertical shift register. Feedback of each shift register is connected back to the input. Thus, the current in each silicon nanowire (I_{OUT}) is measured in the time domain and the sensor can potentially be a small-sized system since only eight input/output connections need to be connected to the sensor chip although the state of 1,024 individual silicon nanowires can be sensed. The input/output bond pads are placed about 2.5 mm from the silicon nanowire elements in order to ease the packaging and allow isolation of the bond pads from the electrolyte solution.

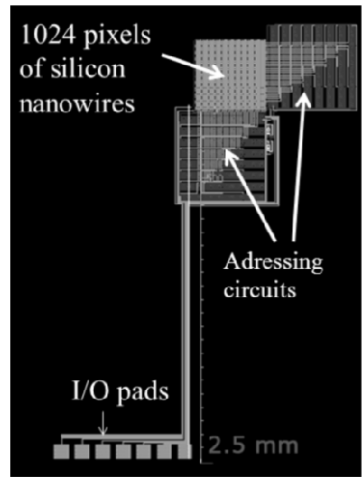

Figure 4.5. *Layout of a 32 by 32 pixel array with shift registers to address individual silicon nanowires in each pixel. The total area is 1.35 mm^2. At the bottom are the I/O pads, about 2.5 mm away from the 1,024 silicon nanowires and the address circuits*

4.6. Conclusions

Integration of silicon nanowires with CMOS circuits can enhance the performance of silicon-based biochemical sensors. The CMOS circuitry allows advanced new functionality to be implemented in the sensor but still achieves a compact and small-size sensor. Silicon nanowires can be integrated after the CMOS chip has been fabricated which benefits from the fact that the chip design is not

altered compared to conventional methodology of designing and fabricating CMOS chips for electronic applications. The main obstacle for this integration scheme is to find a cost-efficient way to place silicon nanowires on the top surface of the CMOS chip and to connect them to predefined contact areas without degrading the CMOS circuitry. Integration of silicon nanowires can also be achieved by defining the silicon nanowires in the silicon layer of a SOI wafer. This scheme demands that the CMOS process should be adapted to define the silicon nanowires in the same process flow as the one used to define the MOSFETs. We showed that this scheme can be implemented in a fully depleted CMOS process, allowing an advanced and small-size biochemical sensor based on silicon nanowires as sensing elements.

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5

Portable, Integrated Lock-in-Amplifier-Based System for Real-Time Impedimetric Measurements on Nanowires Biosensors

5.1. Introduction

The sensitivity and selectivity properties of nanowire interfaces have the potential to revolutionize the field of ubiquitous and pervasive biosensing since the fabrication can be performed using very low-cost nanofabrication processes, based on simple and mature photolithography and standard semiconductor processing techniques, as described in Chapter 1. Among possible applications, there are point of care medical diagnosis and environmental monitoring. However, the great advantages of nanowire sensing could be fully exploited only if the devices are coupled with compact and efficient interfaces.

This chapter focuses on the design and testing of a portable and compact stand-alone hybrid system comprising the electronic readout and the microfluidic interface, directly pluggable to the laptop for real-time impedimetric measurements on nanowires biosensors. Indeed, even if the literature presents many works on nanowire-based sensors, typically the readout apparatus for these sensors is bulky and expensive and requires skilled personnel (see Figure 5.1). To enable the routine application of predictive, preventive and personalized healthcare, these biochemical test sensors will have to work at a much larger scale, at much lower cost and preferably also in point-of-care locations rather than exclusively in clinical laboratories.

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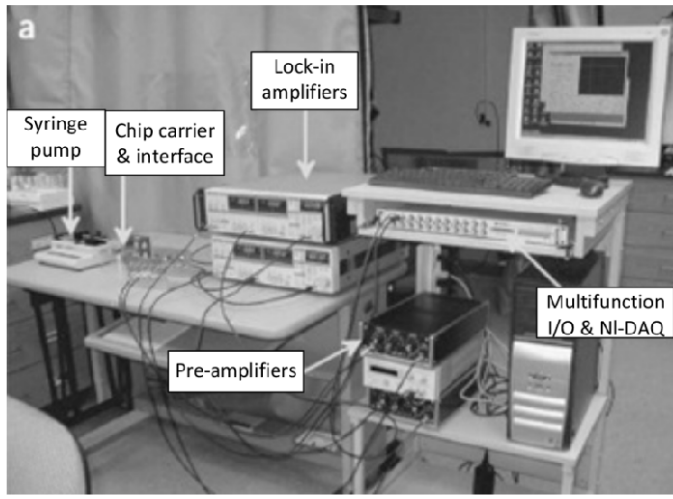

Figure 5.1. *Example of a typical nanowire readout apparatus*

Within the above purposes, integrated sensor systems are emerging as important candidates for the development of point of care devices because of their intensive use in portable applications and lower price compared to the commercial instruments [MAN 12, XU 10, OFF 09, GRA 07]. Integration of the sensor chips with custom electronics into a user-friendly package would provide a new approach to decentralized healthcare management. However, fully integrated biosensing systems have the drawback of tremendously high testing costs, not compatible with preliminary tests on biosensors in experimental conditions.

Usually, studies on nanowire sensing involve direct current (DC) conductance measurements; however, we believe that a compact interface based on a lock-in amplifier technique could implement phase-sensitive measurements that could open new scenarios in nanowire applications. More specifically, we will investigate how complex impedance sensing may detect bioanalytical events occurring at the nanowire transducer surface, such as molecular interactions between the receptors layer and targets biomolecules, as well as the ionic screening effects due to mobile ions present in the solution [STE 07].

5.2. Portable stand-alone system

This system is based on a complex impedance interface implemented into an integrated circuit (IC) device embedded into a compact printed circuit board (PCB) together with microfluidics. Thus, the overall hybrid system comprises the

low-power fully integrated impedimetric interface (described in the next section), an electronic circuitry to set the back gate voltages and the module used to host and to electrically address the nanowires (or nanowire set) in the chip and the proper microfluidics.

The system is designed to perform four terminal measurements (also known as Kelvin sensing) and it is particularly tailored for low-resistive sensors. Due to its high versatility, it is suitable for the study of nanowire-based sensors, performing user-friendly measurements at different working frequencies in order to investigate capacitive effects related to bio-nanodevices.

We think that phase-shift data could be more meaningful, with respect to the standardly-used magnitude impedance or simple DC conductance ones, to highlight the various capacitive effects acting on functionalized nanowires surface, so as to use this sensing approach on nanowire-based sensors with particular interest on the investigation of the phase-shift response.

More specifically, the selected approach is based on the generation of the sinusoidal input signal starting from a ΔΣ-modulated sine wave created using Matlab and memorized on a read-only memory (ROM) in the field programmable gate array (FPGA). The squared wave voltage signal is then filtered, converted into the stimulating signal and sent to the device under test (DUT). This ensures the perfect synchronization of the input signal frequency with the clock frequency that controls the ΔΣ demodulation performed inside the microchip.

The whole stand-alone hybrid portable system is controlled by using the developed custom data acquisition software designed in Java. It has a user-friendly interface, which enables us to easily control all the selectable options of the integrated impedimetric interface, for instance the gain and the working frequency.

The main features of the whole portable stand-alone system are the following:

– real-time alternative current (AC) impedimetric measurements in the range 1–25 KHz;

– modular approach with electronics separated by specific fluidics enabling the easy interchangeability of different sensor chips;

– internal input voltage provided by the FPGA module;

– A/D conversion by integrated band-pass ΔΣ modules;

– universal serial bus (USB) power supply where the board power supply is raised to a suitable DC-DC converter [IR 13] to ensure a high measurement range.

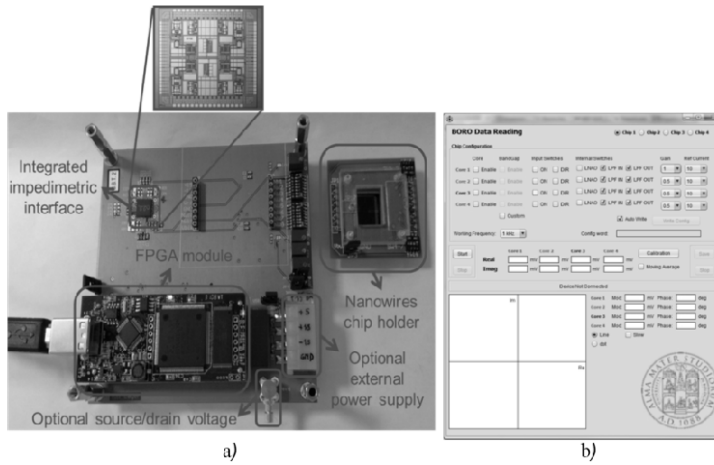

Figure 5.2. *a) Picture of the realized portable stand-alone acquisition system comprising the integrated impedimetric interface developed by the research group, the FPGA module and the nanosensor array holder module which connect the selectable bio-nanosensor to the readout electronics. b) Screenshot of the developed data acquisition software interface*

5.3. Integrated impedimetric interface

The integrated impedimetric interface used in the hybrid portable system is designed in a 0.35 µm CMOS technology [CRE 12a, CRE 12b] enabling the real-time complex impedance readout, and it works by imposing a reference current at a certain frequency to the sensor under test and measuring the voltage response, and possibly sweeping the working frequency over a defined range of values.

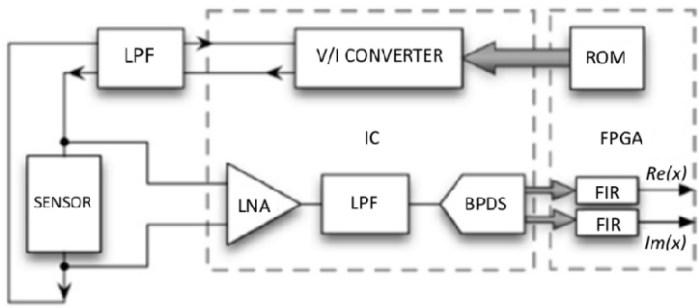

Figure 5.3. *Block diagram of the integrated impedimetric interface system developed by the research group [CRE 12]*

The IC occupies 1.32 mm^2 and hosts four identical cores and implements the lock-in technique based on a band-pass delta-sigma (BPDS) approach. Each core comprises an integrated fully differential low-noise amplifier (LNA) followed by an anti-aliasing switched-capacitor filter and a BPDS analog-to-digital converter [SCH 04]; thus, the demodulation is easily performed in the digital domain by using a couple of exclusive or (XOR) gates, getting rid of the need of hard to design analog multipliers, such as Gilbert cell mixers [MAN 10] or chopped systems [GOZ 09] which are sources of non-idealities and nonlinearities.

The delta-sigma converters are oversampling converters working at a sampling frequency much higher than the signal bandwidth. A delta-sigma converter is generally composed of an integrator (which acts as a low-pass filter), a comparator and a 1-bit digital to analog converter (DAC) in the feedback loop. The main advantage of this circuit is the straight reduction of the in-band quantization noise due to the feedback loop and the oversampling operation, yielding a very high resolution [SCH 04], provided that the high-frequency quantization noise resulting from the noise shaping is digitally filtered, usually using a cascade of finite impulse response (FIR) filters. This is accomplished by the use of a FPGA, which digitally filters and down-samples the 1-bit data streams to achieve the desired resolution.

Substituting the integrator with a band-pass filter, it is possible to implement a BPDS converter that is able to digitize narrowband signal modulated at a selectable frequency providing the real and imaginary parts of the input signal. The developed solution implements a BPDS in the pseudo-two-path switched-capacitor architecture [FRA 97, PAL 89], where the sampled in-phase and quadrature components of the sinusoidal input wave are sent alternatingly to two symmetric paths performing the multiplication by ±1, as shown in Figure 5.4.

In particular, it must be noted that the sinusoidal input is sampled at a frequency $f_s=4\cdot f_0$; thus, the samples are exactly separated by a temporal shift of 1/4 of the sinusoidal input period, which is equivalent to a 90° phase shift, between the samples going to one branch with respect to the other. This yields a single-bit digital output given by the combination of the two digital data streams containing the in-phase and quadrature component of the input signal at a scalable frequency and proportional to the selectable modulating frequency; for instance, with a working frequency of 1 KHz, the two real and imaginary part streams have a frequency of 2 KHz and are serialized in a unique output data stream of 4 KHz frequency, which is sent to the FPGA.

The system can work using the scalability of the clock generated by a quartz oscillator embedded in the FPGA from 500 KHz to 12.5 MHz, enabling the possibility to select a modulating frequency in the range from 1 to 25 KHz and thus resulting in output data streams in the range 4–100 KHz.

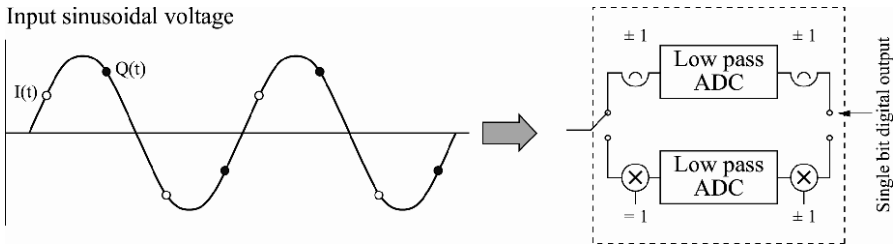

Figure 5.4. *Working principle sketch of the pseudo-two-path BPDS converter*

The sinusoidal input voltage signal is amplified by an LNA that uses a capacitive fully differential architecture with the AC coupling at input pins that blocks the DC voltage and low voltage drift.

The implemented solution enables us to select the gain among eight different values, given by the ratio between the feedback and the input capacitors, resulting in a high flexibility of the interface and enabling the use for different applications.

Moreover, as illustrated in Figure 5.3, in order to achieve a high resolution [CRE 12], the designed IC is able to internally generate four sinusoidal stimulating-current signals of amplitude 10 μA–150 μA–300 μA-1mA starting from the ΔΣ-modulated signal stored in the ROM and using four replicated H-bridge-based architectures to ensure the different amplitude current signal flowing across the DUT in both directions.

5.4. Impedimetric measurements on nanowire sensors

Preliminary tests, obtained performing frequency sweeps in the range of frequencies from 1 KHz up to 1 MHz by using Novocontrol Alpha-A Impedance analyzer [ALP 13], demonstrated a reproducible behavior for two considered successive functionalization steps, silanization (APTES) and cross linker (succinic acid) treatments, as shown in Figure 5.5.

Phase-shift data clearly show a shift related to the particular chemical group, which has the effect of significantly changing the slope of the phase plot. Moreover, performing the same analysis using two different concentrations of buffer solutions (1 and 10 mM phosphate buffer solutions, respectively), it was possible to demonstrate that the results are slightly sensitive to buffer concentration, but also that the interesting observed behavior is repeatable and effectively dependent on the molecular layer on the nanowires surface and probably on the related change of the surface capacitance.

These results once again confirm the possibility of achieving further information on nanowire surfaces considering phase-shift data. In the considered situation, indeed, no significant changes enable us to recognize the four different experimental conditions in the impedance magnitude plot, while the two functionalization treatments are clearly distinguishable by the phase plot.

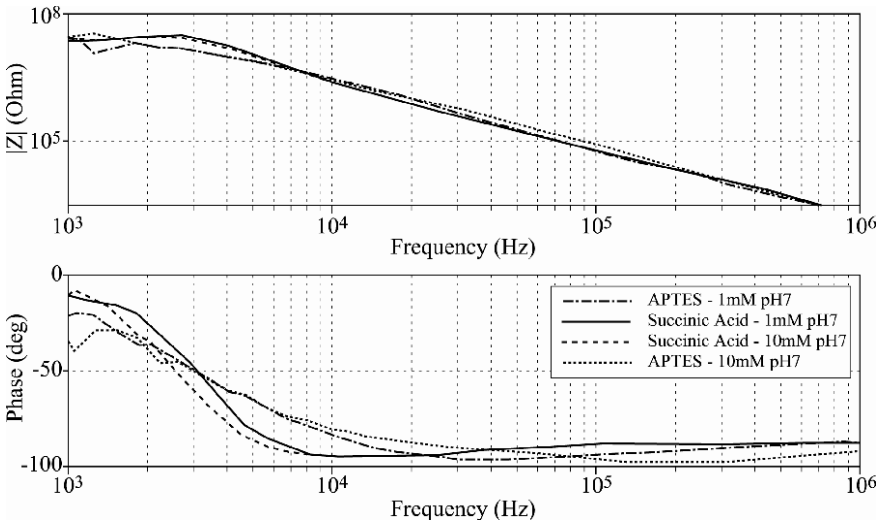

Figure 5.5. *Experimental Bode plot of APTES and succinic acid-treated nanowires demonstrating the effect of different functionalization layers at different frequencies. The data obtained using two different electrolyte solution concentrations also confirm that the devices are more sensitive to the different molecular treatment layers than to the changes of electrolyte solution concentration and confirm the repeatability of the obtained result*

Finally, real time AC pH measurements on bare nanowires were performed using the developed portable stand-alone system.

A pseudo-reference electrode was inserted into a solution and the back gate and liquid gate contacts were fixed at the same potential in order to work in the linear accumulation regime [HAK 12, KNO 11]. Different pH levels (pH 4-11) sodium phosphate solutions at 10 mM concentration were used and obtained admittance magnitude and phase data are reported in Figure 5.6.

Referring the variations to the values obtained for the first pH value of 4 and normalizing the impedance magnitude and phase-shift data for the respective full-scale values (in order to calculate the comparable percentage variation), it was

possible to obtain the values reported in Figure 5.7(a). Considering the response at 1 KHz, the percentage variations in magnitude were found to be higher compared to the values for phase shift; conversely, considering the data obtained using a 4 KHz stimulating frequency, the behavior is the opposite and the percentage variations, even if lower in absolute value because of the attenuation given by the low-pass filter behavior, give higher results for the phase-shift data compared to the magnitude values. This result indicates that the phase-shift data can be effectively used to have similar information compared to the one obtained using the standard conductivity measurements; however, there is a range of frequency in which the sensitivity is higher considering the phase-shift data instead of the magnitude ones.

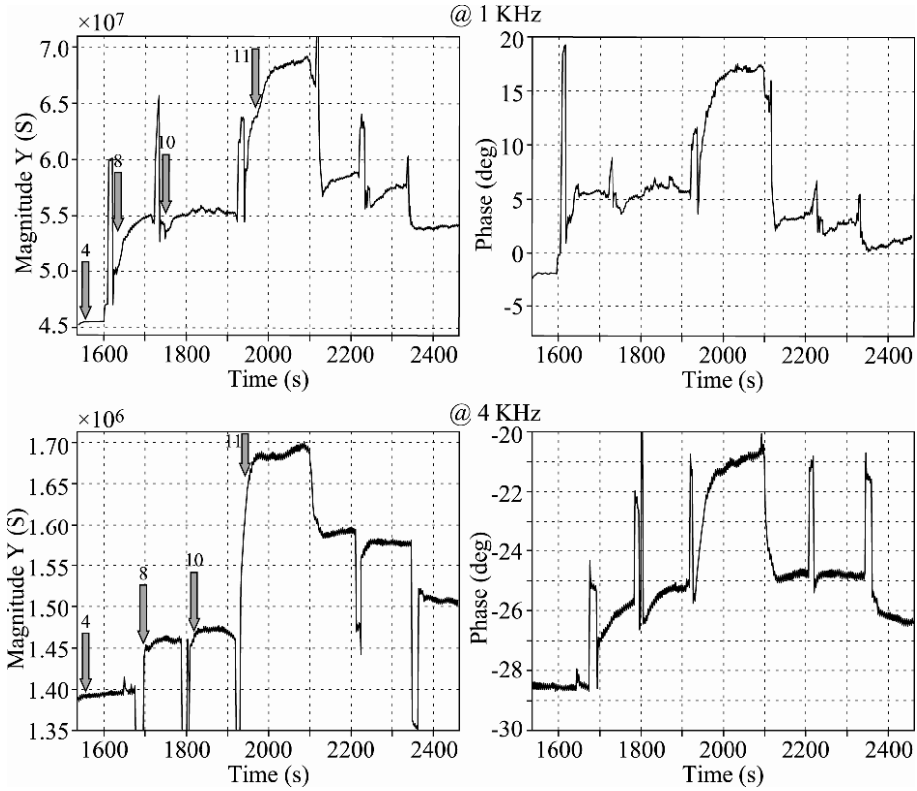

Figure 5.6. *AC real-time measurements of different pH-level buffer solutions at two different working frequencies of 1 and 4 KHz, using bare nanowires. Arrows show when the solution with the indicated pH level was changed*

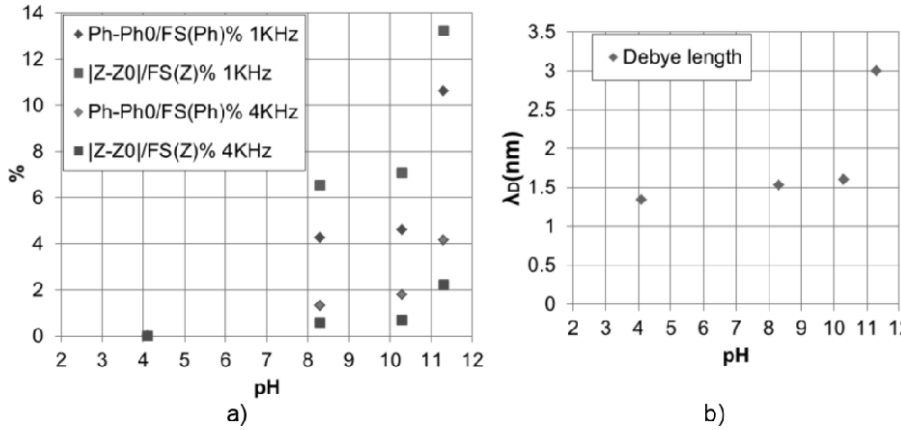

Figure 5.7. *Experimental values of different pH-level buffer solutions, obtained by the mean levels of real-time AC measurements once stabilized, at two different working frequencies of 1 and 4 KHz, using bare nanowires. a) Percentage variation of impedance magnitude and phase shift referred to the pH 4 values (Ph0 and Z0) and normalized for the respective full-scale values. As can be seen, phase-shift data yield a bigger percentage value, compared to impedance magnitude variations, at 4 KHz. b) Debye lengths of the different 10 mM solutions used*

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PART 2
New Materials, Devices and Technologies for Energy Harvesting

Part 2 Introduction

Energy harvesting or energy scavenging is the process by which energy is extracted from external sources (e.g. solar, thermal and vibrational energy), captured and stored for small, wireless autonomous devices for applications ranging from wearable electronics to personal healthcare devices and wireless sensor networks. The present interest in such application fields and the steady development of electronic devices with low-power consumption motivates the research on electronic systems capable of harvesting energy from the surrounding environment. Power harvesting from the environment has been one of the most challenging issues faced by industrial and academic research for the last several years. It holds the promise of sustainable ubiquitous and pervasive electronic systems, which will overcome many limitations in power supply set by electrochemical cells and will pave the way toward indefinite operation. However, many limiting factors are still delaying the deployment of this vision in practical applications, pertaining to the strict requirement of dealing with very low available power densities, often as low as a few microW/cm^3 [VUL 09]. Moreover, ambient energy sources are often irregular or sporadic, and energy transducers produce highly variable output voltages, ranging in many practical cases from few hundreds of mV to tens of V, thus making it difficult to optimize power conversion.

Currently, most energy harvesters can provide, in practical cases, an output power density of about 10–100 μW/cm^3 [CHA 08]. In this scenario, mechanical vibrations, thermoelectric gradients and solar sources represent the most viable solution for supplying low-power electronic systems (such as wireless sensor nodes or personal healthcare devices).

In the following four chapters, the main aspects of a complete harvesting system are analyzed, including the different technologies available to extract the

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environmental energy and the interfaces between the “core” harvesting device and the load (system to be powered).

Chapter 6 deals with vibrational energy harvesting systems, employing piezoelectric and electromagnetic effects. After an introduction, an overview of state-of-the-art vibration energy transducers employing the piezoelectric effect is presented in section 6.2, where microelectromechanical systems (MEMS) prototypes realized in the framework of the nanofunction project will be also presented. Near-field characterization techniques as well as electro-mechanical modeling and simulation required for the design of the energy harvesting transducers will be illustrated. In section 6.3, electromagnetic generators presented in the literature including large scale discrete devices and integrated versions are reviewed, where the results achieved on vibration energy harvesters exploiting both electromagnetic and piezoelectric effects will be derived.

Chapter 7 presents some recent experimental advances in the field of thermoelectric energy conversion and harvesting. Focus is put on the prospects of materials’ nanostructuration for an improved thermoelectric figure of merit in order to replace rare or toxic materials. The main advantage of nanostructuration arises from a decrease of thermal conductivity, due to the enhanced role of confinement and interfaces in thin films, quantum wells, or wires, not speaking of the potential engineering of roughness or composition. Sections 7.2 and 7.3 will be devoted to this subject. In section 7.2, ultrathin self-suspended films will serve as model systems to explain the physics of phonon transport in such structures, describe the characterization methods that can be used to probe it and develop reliable models. Section 7.3 will describe porous silicon as an example of very low thermal conductivity material due to its nanostructured nature. This material can be used as an effective local thermal isolation substrate on the Si wafer, thus allowing the development of on-chip high-performance heating, cooling or thermoelectric devices. The thermal conductivity of porous Si was determined for the first time at cryogenic temperatures down to 20 K and it was demonstrated that at low temperatures, porous Si thermal conductivity is more than four orders of magnitude lower than that of bulk crystalline Si, thus also proving its importance for use in cooling devices. A good-performance thermoelectric generator using a simple and robust technology based on thermal isolation on the Si wafer by a thick porous Si layer was also demonstrated. Research toward alternative solutions was also presented. Section 7.4 is devoted to the new field of spin caloritronics and its potential for thermal energy harvesting, with an experimental insight into the spin Seebeck effects. Finally, because direct conversion from thermal to electric energy is not the only route for thermal energy harvesting, section 7.5 will give the example of a composite solution, which combines thermal to mechanical conversion, by means of a memory-shape alloy, followed by a mechanical to electrical conversion, by means of a piezoelectric material.

Chapter 8 deals with energy harvesting from solar sources. Photovoltaic energy is one of the most promising sources of renewable electricity and recent applications include energy harvesting for autonomous electronic systems. In this application contest, silicon nanowire-based solar cells are an attractive approach for realizing solar cells with a small volume, efficient light trapping scheme and high-collection efficiency in the case of radial junctions. In fact, the high aspect ratio of nanowires enables significant reduction in solar cell thickness without loss of optical absorption while simultaneously providing effective carrier collection in the case of radial junctions. Efficiencies similar to or higher than those obtained with first-generation solar cells (about 14–18%) are expected for single-junction nanowire solar cells with a cost reduction due to material consumption and low-cost growth methods [GAM 11].

Finally, Chapter 9 deals with the power management circuits for indoor light energy harvesting, thermoelectric energy harvesting and vibration energy harvesting areas. The objective of power management circuit design is toward higher conversion efficiency, ultra-low power consumption and low-energy storage leakage losses [WAN 12].

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6

Vibrational Energy Harvesting

6.1. Introduction

Energy harvesting is an attractive way to power electronic systems such as wireless sensors without using batteries or other energy storages with limited lifetime. Among the energy harvesters proposed from different sources (e.g. light, thermal gradient, strain, vibrations, electromagnetic field, air flow and pressure variations), vibrations pervasively available in different environments (indoor and outdoor) represent an attractive option for the development of adequate sources for low power supplying or for extending the autonomy of remote sensors and portable electronics. Power harvested from mechanical vibrations represents a very promising energy source with estimated power in the μW–mW range [ROU 04a].

Vibration-powered generators are typically inertial spring and mass systems (Figure 6.1) which employ three main transduction mechanisms to extract energy from vibrations: piezoelectric, electromagnetic and electrostatic. Piezoelectric generators employ active materials that generate a charge and, therefore, a voltage when mechanically stressed. Electromagnetic generators harvest energy from vibrations by employing the electromagnetic induction arising from the relative motion between a magnetic flux gradient and a conductor. Electrostatic generators use the vibration-induced relative movement between electrically isolated charged capacitor plates against the electrostatic force to generate energy. Other solutions employing either electrets or magnetostrictive materials for the mechanical energy conversion have also been proposed [WAN 08, KAR 08a].

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Microelectromechanical systems (MEMS) technology was largely investigated to achieve vibration energy harvesters that can be potentially integrated with low-power applications such as wireless sensor network (WSN) nodes [AMM 05, ERI 05, JEO 05, BEE 06, ROU 03]. Piezoelectric transducers have often been proposed to implement easily exploitable energy harvester solutions mainly because of their low-cost manufacturing process and the potential integration with complementary metal–oxide semiconductor (CMOS) technology. Nevertheless, electromagnetic transducers were also explored due to their complementary advantages compared to piezoelectric transducers, and solutions combining both transduction harvesters were proposed to improve the energy density and the conversion efficiency [BEE 07a].

In order to be used in practical applications, the energy harvesters have to deliver a minimum output power and voltage, which are required by power converters to operate with acceptable efficiency. Unfortunately, this is not always the case, and several energy harvesters proposed in the literature have low output power and voltages, are large and bulky, and their efficiency is shown to peak only in a very narrow frequency range, thus making such devices unsuitable to scavenge energy from actual ambient vibrations. For this reason, research activities have been oriented to improve the power efficiency and the output power of the vibration energy harvester, to decrease the size of the transducers, to decrease the operating frequency, to match the low frequency ambient vibrations and to widen their bandwidth to maximize the energy collection (ambient vibrations rarely occur at exact frequencies) [MUR 09].

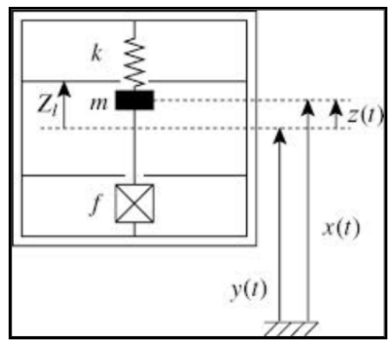


Figure 6.1. *Illustration of the generic principle of vibration energy harvesting*

This chapter will present a short overview of the MEMS energy harvesters employing both piezoelectric and electromagnetic effects both proposed in the literature and developed in the framework of the Nanofunction project.

A short overview of state-of-the-art vibration energy transducers employing the piezoelectric effect is presented in section 6.2, where MEMS prototypes realized in the framework of the Nanofunction project will also be presented. Near-field characterization techniques as well as electromechanical modeling and simulation required for the design of the energy harvesting transducers will be illustrated.

Electromagnetic generators presented in the literature including large-scale discrete devices and integrated versions are reviewed in section 6.3, where the results achieved on vibration energy harvester exploiting both electromagnetic and piezoelectric effects will be derived. Modeling and simulation results will be presented to demonstrate the feasibility of the proposed device concepts.

6.2. Piezoelectric energy transducer

6.2.1. *Introduction*

Vibration energy can be converted into electric energy by piezoelectric MEMS transducers, which are preferable to electromagnetic and electrostatic transducers because of their CMOS technology compatible manufacturing process and higher energy density [BEE 07a].

Piezoelectric harvesting is based on the piezoelectric effect: when a piezoelectric material is subjected to a mechanical stress or strain, a charge is generated, which allows us to convert mechanical energy (induced by either vibration or movement) into electrical power. There are two piezoelectric operation modes: d_{31} or d_{33} mode. In the d_{31} mode, the stress or the strain is perpendicular to the direction in which the charge is generated, whereas in the d_{33} mode the stress and the electric field have the same direction.

Figure 6.2 illustrates the principle of the operation of a piezoelectric harvester: a cantilever beam with an inertial mass *M* (which can be also omitted) can be covered by a piezoelectric material. As the beam is bent, the piezoelectric material is subjected to a stress or a strain, which induces an asymmetric charge distribution; therefore, a voltage is generated on the capacitor. Similarly, any moving/bending structure (e.g. membrane) can be covered with a piezoelectric material to realize a vibration energy harvester.

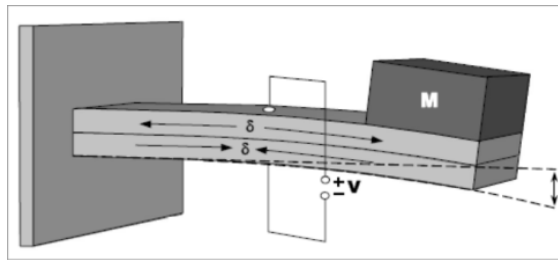


Figure 6.2. *Stress or strain in a piezoelectric material causes an asymmetric charge distribution in the material, and hence a voltage over a capacitor*

6.2.2. *State-of-the-art devices and materials*

Most of the vibration energy harvesters based on the piezoelectric effect have a cantilever structure with a mass at the end of the beam and a layer of piezoelectric material deposited on the beam and connected to the electrode.

MEMS technology has been widely investigated as a potential low cost manufacturing technique for vibration energy harvester fabrication, particularly attractive for harvester miniaturization and integration. Piezoelectric transducers exploiting thin films of piezoelectric materials were widely proposed in the literature.

Commonly used piezoelectric materials including piezoceramics (lithium niobate, $LiNbO_3$, barium titanate, $BaTiO_3$, lead titanate $PbTiO_3$, lithium tantalite and $LiTaO_3$) and quartz crystals are not suitable for vibration microgenerators because of their relatively large size and incompatibility with silicon substrates. On the contrary, piezoelectric thin film materials, such as lead zirconate titanate (PZT) piezoceramic, polyvinylidene fluoride (PVDF) polymer, polycrystalline zinc oxide (ZnO) and aluminum nitride (AlN) layers, were exploited for MEMS transducer fabrication because of their compatibility with standard microelectronic processing technologies.

The capability of effectively harvesting energy from vibrations depends on both material and device architecture, which should be designed to provide mechanical amplification of the applied stresses in order to allow larger strains, i.e. larger charge/voltage generation.

The most significant property of piezoelectric material is the electromechanical coupling coefficient that describes the efficiency of the conversion of a mechanical strain into an electrical energy. This parameter depends directly on piezoelectric

coefficients and elastic modulus, while it is inversely proportional to the dielectric constant of the material.

Among the most used piezoelectric materials for vibration energy harvesting applications, the PZT piezoceramic has the highest electromechanical coupling coefficient, and therefore it has been for a long time the preferred choice for the fabrication of the piezoelectric harvesters reported in the literature, despite its low dielectric constant. Nevertheless, PZT is extremely brittle (this limits the maximum strain that can be absorbed before rupture), and its processing is troublesome. Indeed, PZT requires poling or postdeposition annealing to exhibit piezoelectricity, and, being a ferroelectric material, it cannot undergo a temperature above the Curie temperature, which is lower than 300°C for thin films of PZT.

Despite processing issues, prototypes of PZT-based micropiezoelectric cantilevers with interesting performances have been proposed in the literature. In [MIT 08], the cantilever beams were made up of aluminum, the proof mass was steel and PZT layers were glued on the top and bottom of the proof mass. The harvester generates 32.5 μW of power from 47 m/s^2 vibrations at 150 Hz. Zhou *et al.* in developed transducers relying on interdigitated electrodes to operate in the more efficient d_{33} mode. The model developed by Zhou predicted a power density greater than 2 $\mu Wmm^2/g$ for a PZT cantilever of dimensions 100 μm × 200 μm with a natural frequency of 1 kHz. Jeon *et al.* in [JEO 05] reported 1 μW of continuous electrical power delivered to a 5.2 MΩ resistive load at 2.4 V from a 170 μm × 260 μm PZT beam at a resonance frequency of 13.9 kHz.

A cantilever with 1.64 μm PZT thick-layer proposed in [LIU 06] shows 898 mV voltage and 2.16 μW power output at resonant frequency of 608 Hz under a 1 g acceleration. Isarakorn *et al.* [ISA 11] reported on a MEMS vibration energy harvesting device based on a 1000 × 2500 × 0.5 μm^3 PZT epitaxial thin film on a silicon platform exhibiting a power of 13 μW at a resonance frequency of 2.3 KHz under 1g acceleration. Shen *et al.* showed that a micromachined PZT cantilever based on a silicon-on-insulator (SOI) structure achieved an average power of 0.32 W and power density of 416 W/cm^3 when the device is excited at 0.75*g* acceleration at its resonant frequency of 183.8 Hz [SHE 09].

Despite the large electromechanical coupling coefficient, the low dielectric constant of PZT limits the maximum voltage this material can generate. In order to increase the generated voltage, a piezoelectric material with a lower dielectric constant such as the aluminum nitride (AlN) is desirable, which has been recently proposed for the fabrication of vibration harvesting transducers. Despite the lower electromechanical coupling coefficient, the lower dielectric constant of AlN allows us to generate a much higher voltage compared to PZT, and the harvested power provided by AlN can either be equal to or exceed the power obtained with PZT.

In addition, AlN has other important additional benefits compared to PZT: AlN is biocompatible; its fabrication process is easier and is fully compatible with CMOS technology. Indeed, AlN thin films can be grown using low temperature techniques (below 400°C), such as sputtering. The deposition of AlN films is extremely versatile, and excellent crystallinity and orientation are easy to be achieved on different substrates including dielectrics, semiconductors, metals and flexible substrates like polymers.

A few energy harvesting transducers exploiting piezoelectric properties of AlN thin films started to be reported in the literature. A 1.5×0.75 mm^2 AlN cantilever device with a AlN piezoelectric layer of 1 μm has been shown to produce an output power of 60 nW dissipated on a resistive load at 900 Hz with an acceleration of 10 ms^{-2} [MAR 05].

Van Schaijk *et al.* showed a MEMS AlN cantilever providing an output power of 10 μW under an acceleration as high as 8g at a resonance frequency slightly higher than 1 KHz [SCH 08]. The same group reported on a $2.1 \times 7 \times 0.8$ mm^3 MEMS AlN-based cantilever beam generating an output power of 60 μW at 572 Hz under 2 g acceleration [ELF 09].

Other materials with lower piezoelectric coefficients such as GaN and ZnO have also been investigated because of their piezoelectric and mechanical properties, which look particularly promising as the device sizes are reduced at the nanoscale [HIN 12, ZHA 04, MIN 12, XU 11]. Furthermore, nanoscale vibration energy harvesting devices based on ZnO working in a non-resonant mode [ZHU 12b] were proposed, which are complementary to MEMS devices when a sensibility to smaller forces is required [ARD 12].

Besides the exploration of new piezoelectric materials, the research efforts in the last years have also been oriented to scale the sizes of the vibration energy transducers and widen their frequency bandwidth of operation.

Scaling the energy harvester devices was pursued to develop new classes of microsystems useful in several fields spanning from Wireless Sensor Networks (WSN), to wearable/implantable electronics, robotics and medicine, where the energy harvester is integrated with the core of the system represented by sensors, logic and transceivers. Unfortunately, scaling the transducer sizes proportionally reduces the power that can be harvested from vibrations, while increasing the transducer resonant frequency at which the energy harvester operates at the maximum efficiency far away from the spectrum of vibration frequency commonly available in the environment, thus contributing to further lower the collected power.

Another promising application for piezoelectric energy harvesters concerns the use of MEMS technology on soft substrates, such as kapton or polyethylene terephthalate (PET) compatible with soft electronics, thus allowing us to recover much more power because of the bending of the entire electronic system structure [PAN 10]. In this context, transducers based on AlN thin films on polyimide flexible substrates showing promising piezoelectric, mechanical and electrical properties have already been developed [PET 11].

6.2.3. *MEMS piezoelectric vibration energy harvesting transducers*

In this section, we present and discuss the design and characterization of MEMS vibration energy transducer prototypes realized in the framework of the Nanofunction project.

Two different device architectures relying on piezoelectric AlN thin films have been designed and fabricated, as discussed in the following sections: (1) the arrays of small area free-standing rings of bent cantilevers and (2) large area cantilevers.

6.2.3.1. *Arrays of free-standing rings of bent cantilevers*

Arrays of free-standing rings of bent cantilevers consist of an AlN layer, sandwiched between two Mo electrodes, grown on commercial substrates, i.e. a thin SiO_2 sacrificial layer on a thick (100) silicon substrate. Mo/AlN/Mo structures are deposited by DC magnetron sputtering by using a LLSEVO Unaxis system.

In free-standing rings, Mo/AlN/Mo structures roll up because of the AlN built-in strain controlled by the deposition process. The Ring-MEMS (RMEMS) (see Figures 6.3(a) and (b)) has been designed to obtain resonances at low frequencies. Its elastic property and the additional torsional degree of freedom allow us to achieve a good power density and high efficiency at low frequency and for low vibrational forces.

The 400-nm thick AlN layer was deposited in a mixed atmosphere of Ar and N_2 with a working pressure of $1.3 \cdot 10^{-3}$ mbar, power of 2.25 kW and a DC bias of −65 V, by using a LLSEVO Unaxis sputtering system. The control of the deposition parameters related to the Mo and AlN layers, such as bias and N_2/Ar pressure ratio allows controlling the residual stress [GIO 09, KAR 08b].

The top and bottom Molybdenum (Mo) electrodes are 85 and 120 nm thick, respectively. Molybdenum was chosen as the electrode material because of the following properties: (1) it promotes a preferential (002) orientation of the AlN film, (2) it has a low resistivity and (3) it can be easily etched by H_2O_2, thus reducing the complexity of device fabrication.

The fabrication process of the piezoelectric MEMS rings is based on optical lithography and wet chemical etching. Mo layers are chemically etched by an H_2O_2-based solution while the AlN layer is etched by an H_3PO_4-based solution. To release the structure from the substrate, a HF-based solution is used to remove the SiO_2 sacrificial layer: the high residual stress rolls up the realized strips, thus, forming the RMEMS as shown of Figure 6.3(a). Arrays of RMEMS structures of different sizes (i.e. widths and diameters) are fabricated by using micromachining techniques. Different growth conditions and layer thicknesses allow us to modify the residual stress and tune the ring diameter. No proof masses have been applied to the devices. The most important steps in the fabrication process are sketched in Figure 6.4. Further details of ring devices are reported in [MAS 11].

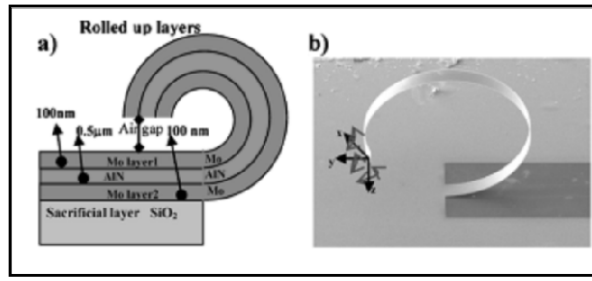


Figure 6.3. *a) Ring layout based on Mo/AlN/Mo structure; b) scanning electron microscope image of the RMEMS and torsional moments of the tip*

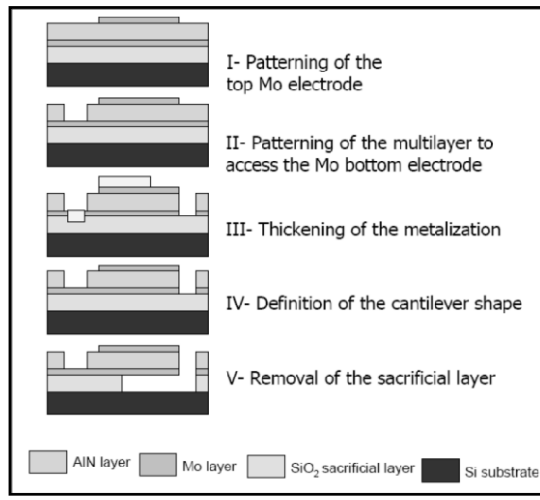


Figure 6.4. *Fabrication process steps of bent cantilevers. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The prototypes of arrays of AlN-based MEMS free-standing rings of bent cantilevers have been characterized by means of the experimental workbench for vibration energy harvester characterization shown in Figure 6.5, which is composed of an electrodynamic shaker for controlled vibration generation and a lock-in amplifier (LIA) to measure the root mean square (RMS) voltage generated by the excited devices.

Figure 6.8(a) shows the RMS open-circuit voltage V_{oc} generated by the RMEMS prototypes of average diameter of 170 μm tested at different acceleration levels. The highest generated voltage occurs around 64 Hz, which is to the main resonance frequency of the device and does not depend on excitation acceleration. The maximum open-circuit voltage is V_{oc} = 236 μV under 2.0 g acceleration. Moreover, two lower V_{oc} peaks occur at lower frequencies, i.e. at 40 and 48 Hz, probably due to torsional vibration mode of the ring structure of the MEMS transducer.

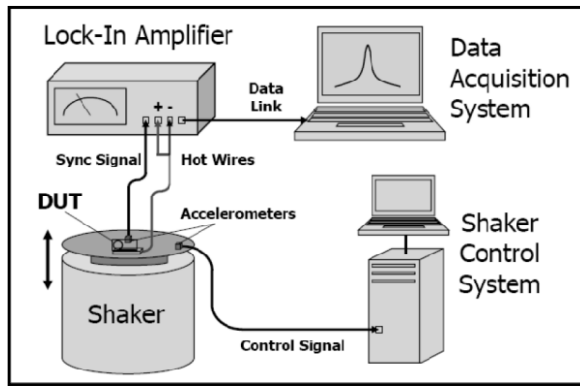


Figure 6.5. *Simplified block diagram of the workbench used for characterization of energy harvesters*

To evaluate the maximum output power provided by the RMEMS prototypes, we measured the output impedance at the power matching conditions, which is used to measure the RMEMS output power, as shown in Figure 6.6(b). The power generated by the RMEMS is 1.3 nW at the resonance frequency under a 2.0 g excitation acceleration. This value corresponds to a maximum power density of 30.2 μW/mm^3, which represents an excellent performance of the RMEMS cantilever if compared with those of AlN piezoelectric micropower generators at low frequency and PZT micropower generators reported in the literature [ISA 08]. This device architecture also allows us to achieve very low resonance frequency, opening new perspectives for micropiezoelectric MEMS energy harvesters.

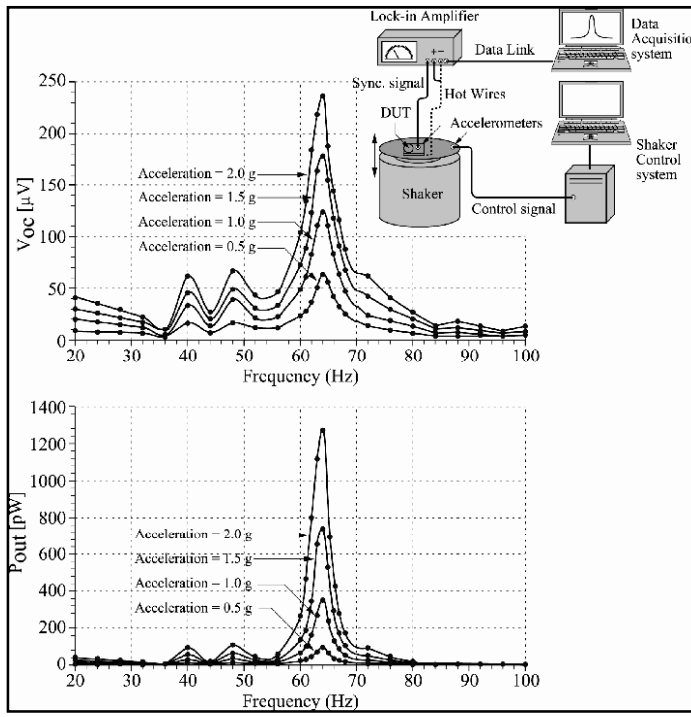


Figure 6.6. *a) Open-circuit voltage V_{oc} generated by the RMEMS excited at different accelerations; b)output power P_{out}*

Arrays of RMEMS bent cantilevers were also characterized by measuring the RMS open-circuit voltage (V_{oc}_rms) across the device terminals at different acceleration levels and the output power (P_{out}) provided under different resistive loads.

Figure 6.7(a) shows the open-circuit voltage measured on arrays composed of two identical bent MEMS cantilever prototypes connected in parallel. Each cantilever is 1500 μm long and 100 μm wide [BER 11]. The resonance frequencies are found at ~500 and ~1500 Hz, and the corresponding open-circuit voltages are around 300 and 500 μV, respectively. The multiple resonance frequencies along with the observed open-circuit voltages can be understood by using Finite Element Method (FEM) simulations, which show that the free end of the bent cantilever moves following an elliptical path in the three-dimensional (3D) space. We have found that the device deformation and movement does not depend strictly on the excitation direction, which allows relaxing the placement and the orientation issues of the transducer on the vibrating structures. However, smaller deformation means

lower RMS open-circuit voltage compared to classical cantilevers subjected to an excitation along the preferred direction, and a corresponding lower power generation for a given excitation. The same array has been characterized at the resonance frequency by varying the resistive load to maximize the power. The MEMS cantilevers provide an output power P_{out} of 0.4 pW with a resistance of 110 kΩ under an excitation acceleration of 2 g, see Figure 6.7 (b).

Beside the expected reduction of the collected power due to the scaling down of the vibration transducer area, the parallel connection of the cantilevers does not provide the expected increase in the collected power. This is probably due to the fact that the charges generated by each cantilever compensate each other (because of slightly different resonance frequencies) instead of summing up. This finding indicates that the power cannot be generated by connecting microsize MEMS transducers in series/parallel, and relatively large area cantilevers are required.

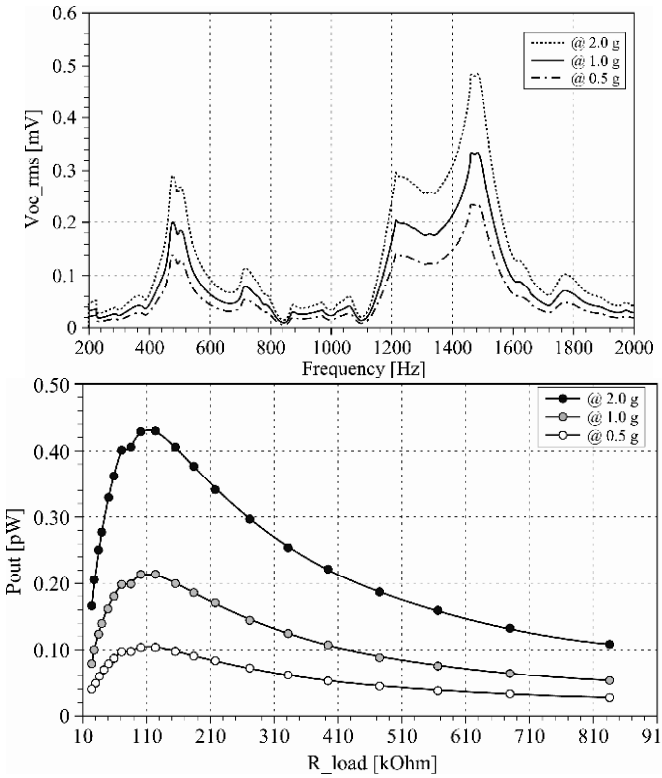


Figure 6.7. *a) RMS value of the open-circuit voltage measured across the devices terminals versus frequency at different acceleration levels; b) power versus resistive load at the resonance frequency of 1.502 kHz*

6.2.3.2. *Large area cantilevers*

These large area cantilevers are single beams with a large piezoelectric area in order to increase the generated voltage and the corresponding output power. Figure 6.8 shows a schematic layout of the large area vibration energy harvesters.

The piezoelectric area covers only the hinge area to reduce residual stress and avoid limiting the cantilever bending. Devices have an additional seismic silicon mass, which is a fraction of the silicon substrate underneath the cantilever that is used to decrease the fundamental resonance frequency. Thin hinges are adopted to maximize structures flexibility and increase displacement.

Following this strategy, cantilevers with different areas between 1 mm^2 and 1 cm^2 have been designed and realized by developing a new fabrication process. The main differences compared to the fabrication process of RMEMS free-standing rings previously described are related to the release of beams, which has required a deep etching process. The cantilever is composed of a 1 μm thick AlN piezoelectric layer, embedded into two Molybdenum (Mo) electrodes (about 250 nm thick), deposited by DC sputtering on a commercial Si/SiN/SiO_2 substrate.

The large-area piezoelectric cantilever consists of a silicon cantilever with a thin hinge with a 400 μm thick proof mass shaped into the silicon substrate at the end. Devices with different hinge thickness and geometry have been fabricated by conventional micromachining technique.

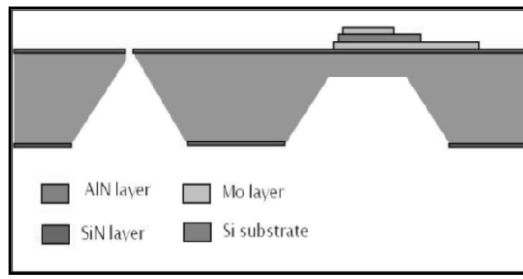


Figure 6.8. *Cross-section scheme of the large area energy harvester. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Figure 6.9 shows the top side and bottom side of a fabricated large area cantilever prototypes. The cantilever deflections and the resonance frequencies have also been measured by laser Doppler vibrometry.

Figure 6.10 shows RMS value of the open-circuit voltage (V_{oc}) at 1 g and 2 g acceleration measured on a 9 mm long and 7.2 mm wide cantilever with a 130 μm

thick hinge. The inset shows the generated power versus the resistive load at the first resonance frequency. At the resonance frequency of 1.508 kHz, this cantilever generates a V_{oc} of 301 and 520 mV under an acceleration of 1 g and 2 g, respectively. The output power generated at the resonance with an optimal load of 82 KΩ was 0.35 μW and of 1.25 μW at 1 g and 2 g, respectively.

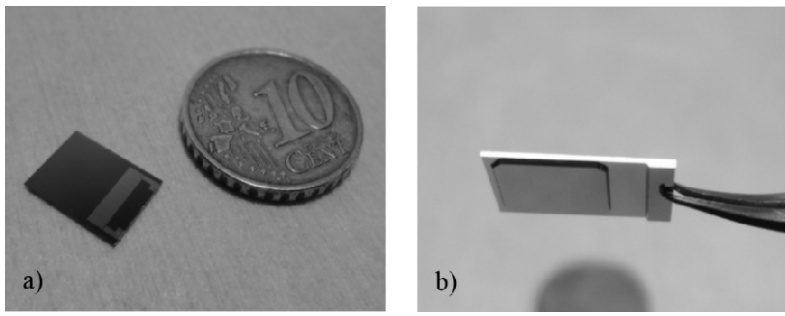


Figure 6.9. *a) top side and b) bottom side images of a realized large area energy harvester*

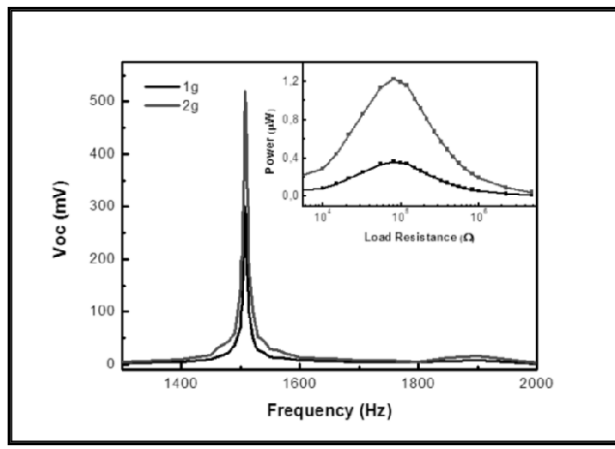


Figure 6.10. *Open-circuit voltage versus frequency carried out at 1 g and 2 g accelerations. The inset shows the corresponding generated power at different load resistances. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Figure 6.11 depicts the generated power at low acceleration levels for 6.5 mm long and 5.2 mm wide cantilevers with different hinge thickness (130 and 40 μm) at the first resonance frequency. The cantilever with 40 μm hinge thickness shows good performances: the first resonance frequency is at 780 Hz; the output power under an optimal load of 220 KΩ is 0.55 μW under a 1.5 g acceleration,

corresponding to an RMS open-circuit voltage of 800 mV. In the same conditions, the cantilever with thicker hinges provides 4 nW at 2.8 KHz resonance frequency, corresponding to a measured peak-peak root mean square open-circuit voltage V_{oc} of 32 mV.

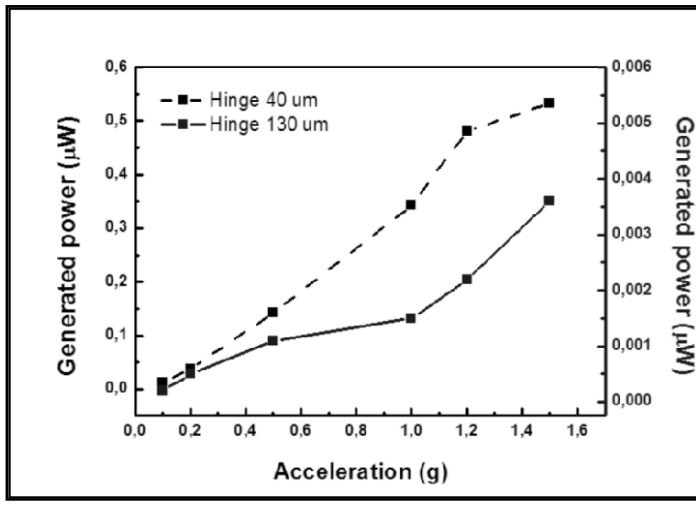


Figure 6.11. *Comparison between the generated power versus acceleration levels carried out at the first resonance frequency from large area cantilevers with different hinge thicknesses*

6.2.4. *RMEMS prototypes characterization and discussions of experimental results*

In this section, we present and discuss the experimental results obtained from the characterization of a RMEMS chip prototype for vibration energy harvesting purposes. The chip is composed of five different RMEMS having an average radius of 85 μm. For measuring the performances of the realized AlN-based RMEMS chip, we arranged the dedicated experimental setup. Vibrations were generated through an electrodynamic platform shaker, which is the Data Physics V400 /M8/VI with DSA1-2K amplifier. The RMEMS chip is fixed to the vibrating platform of the shaker, which provides a d_{31} excitation.

Vibration, frequency and acceleration are controlled by means of the SignalStar Vector Vibration Controller software, which allows a very fast and precise control of the shaker oscillations thanks to the accelerometer feedback signal required to monitor the effective shaker platform acceleration. The voltage generated by the

excited RMEMS is measured by means of a SRS SR530 analog LIA. The LIA synchronization signal is provided by an accelerometer fixed to the shaker platform.

For the characterization of the RMEMS prototypes, we measured both the open-circuit voltage and the maximum power provided by the RMEMS varying both vibration frequency and acceleration. The vibration frequency range considered spans from 20 to 100 Hz, since this range includes the typical vibration frequencies in environment and industrial applications [CHA 08, MOO 09, COT 09, SUZ 08a, SUZ 08b, ZHE 08, GIO 09, SUZ 10, TVE 10, ROU 03, KAR 07, COT 07, DAV 10].

Open-circuit voltages measured on the RMEMS chip prototype excited with different accelerations are plotted versus frequency. We do not consider acceleration values greater than 2.0 g (g = 9.807 m/s^2) as they are very rare in environment and industrial applications. The highest value of the open-circuit voltage, V_{oc}, generated by the RMEMS occurs at ~64 Hz independent of the excitation acceleration, indicating that the main resonance frequency of the RMEMS is f_0 = 64 Hz. The maximum open-circuit voltage is V_{oc} = 236 μV with a 2.0 g acceleration. Moreover, two lower V_{oc} peaks occur at lower frequencies, i.e. at 40 and 48 Hz, probably due to the torsional vibration mode of the ring structure of the MEMS transducer.

The quality factor of the RMEMS piezoelectric transducer ($Q = f_0/\Delta f$) decreases slightly at higher accelerations, dropping from 24 to 17 with acceleration levels going from of 0.5 g to 2 g, respectively. This is due to the air damping, which is a well-known mechanical loss factor [DAV 10].

In order to evaluate the maximum output power provided by the RMEMS chip, we derived the output impedance satisfying the power matching conditions [SAK 08]. Thus, we measured first the output impedance of the RMEMS transducer RMEMS~18 Ω. Surprisingly, the capacitive part of the RMEMS impedance is negligible compared to the resistive RMEMS one. The device resistance (impedance) turns out to be quite low, in the range of tens to hundreds of Ohms depending on frequency and sample size. We believe that such a low resistance value is primarily due to Molybdenum interdiffusion across the thin polycrytalline AlN layer having columnar structure. A trade-off between thin layers for optimal strain release and thick layers for resistance optimization has to be found in order to optimize yield of the RMEMS. Work is underway in our laboratories to assess this issue.

An optimized load impedance was employed in order to measure the RMEMS output power, at different frequencies and for different accelerations.

The power generated by the RMEMS is 1.3 nW at the resonance frequency under 2.0 g excitation acceleration. By normalizing the power to the total volume of the rings arranged in the chip we obtain a maximum power density of 30.2 $\mu W/mm^3$. Such a value is very high, indicating the excellent performance of the RMEMS compared to those recently reported in the literature (Table 6.1). The measured power density of the RMEMS chip is more than two order of magnitude higher than AlN piezoelectric micropower generators at low frequency and significantly higher than the best PZT micropower generator reported in the literature [SUZ 10]. The great advantage of the proposed AlN based solution is mainly due to its ring structure, which allows us to achieve very low resonance frequency compared to other solutions, thus opening new perspectives for piezoelectric MEMS energy harvesting applications. In fact, current vibration energy harvester solutions available on the market, with typical maximum power density of 0.1 μWmm^{-3} around 50–120 Hz [SUZ 08b], use very large-size vibrating structure requiring complex fabrication methods, and thus hardly exploitable for integrated electronic systems. Our RMEMS architecture overcomes these drawbacks and, by virtue of its microscale dimensions, can be used for a large number of applications, as low-frequency vibration energy sources are largely diffused in human and industrial environments.

6.2.5. *Near field characterization techniques*

The knowledge of the mechanical properties of the materials used on mechanical energy harvesters is important for their correct design. Several techniques can be used to characterize these properties, for example tensile tests [MAL 09], which require particular sample geometries ranging from the millimeter to the centimeter scale and a few microns thick, and nanoindentation [FAN 03] which requires only a thin layer of the material over a rigid substrate. An alternative method of characterization is the near field characterization technique using an atomic force microscopy (AFM) [HIN 11]. This last technique is advantageous as a controlled force can be applied at a specific location on a sample shaped as a cantilever (single or double clamped), the precise measurement of the deformation of the cantilever gives access to the mechanical properties (Young's modulus) and with a special electronic conditioning (i.e. conductive AFM tip, voltage and LIAs among others) the piezoelectric properties could also be measured [HIN 12, ZHA 04, MIN 12, QI 10]. Still, this technique has limitations: the maximum measurement window is in the order of 20 $\mu m \times 20 \mu m$ giving a maximum size of the measurable sample and the sample stiffness should be compatible with the force range capabilities of the AFM setup which is in the order of nN to μN.

In the framework of the Nanofunction project, the mechanical properties of the RMEMS (Mo/AlN/Mo) bent cantilever described in section 6.2.4 were measured

using the near field technique. A specific sample in the shape of a single clamped cantilever was prepared for this characterization. The original sample was fabricated using the technological process described in the previous section. The initial dimensions were: 500 µm × 100 µm in surface, a Mo bottom layer (120 nm), AlN (750 nm) and a Mo top layer (85 nm) [BER 11] (see Figure 6.14). A reduced dimension (1.26 µm wide and 17 µm long) was achieved by etching the former cantilever using Focused Ion Beam (FIB) before the final release of the cantilever. These dimensions were verified by scanning electron microscopy (SEM) and AFM (see Figure 6.14).

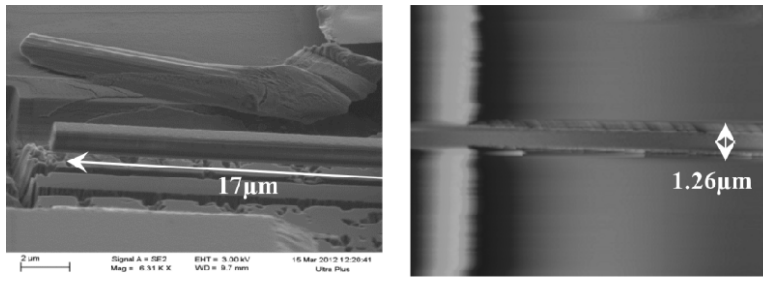


Figure 6.12. *Micro/nano AlN cantilever fabricated by FIB. a) AFM topographic image; b) SEM image. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The first step in the near-field technique is to obtain a topographic AFM image of the sample, then, a controlled force (in the order of 5 µN) was applied at different locations of the cantilever and the deformation in function of the force was measured. On the basis of this data, the Young's modulus can be calculated at different locations of the cantilever using equation [6.1]:

$$E = \frac{k_{slope} \Delta L^3}{3 I_y} \qquad [6.1]$$

where E is the Young's modulus of the three-layered material under test, k_{slope} is the slope of the curve of the applied force versus cantilever deformation, ΔL is the length of the cantilever and I_y is the quadratic moment of the cantilever. The obtained experimental mean value was 333±17 GPa (see Figure 6.15).

A simplified analytical model can also be developed to calculate the equivalent Young's modulus of the structure using the concept of homogenization [LI 08] to

define a mean stress and strain on the cantilever. Using this concept, the equivalent Young's modulus can be expressed as:

$$E_t = \frac{1}{h}\sum_{1}^{3} h_i E_i \cdot \qquad [6.2]$$

where h is the total thickness of the cantilever and the subindices (i) indicate the different layers (Mo and AlN) with their corresponding thicknesses and bulk Young's modulus, 329 GPa and 309 GPa, respectively. The theoretical mean value is 313 GPa representing 6% of error in the measurement (see Figure 6.15). These mechanical parameters can be used in the implementation of the electromechanical models described in the next section.

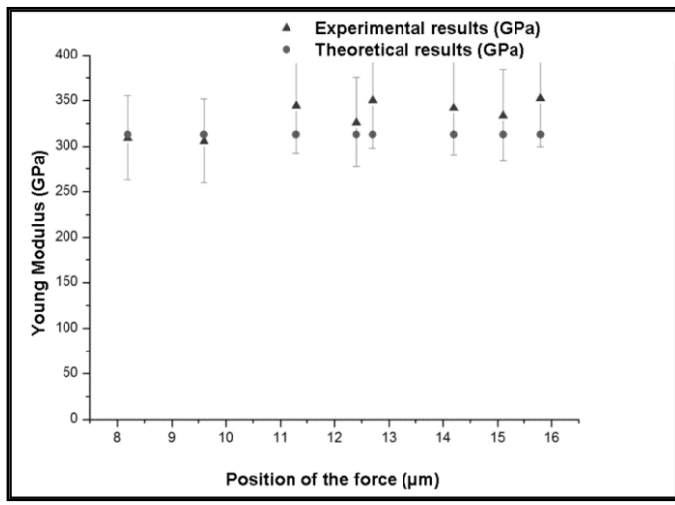


Figure 6.13. *Young modulus of the AlN/Mo piezoelectric cantilever. Experimental and theoretical values*

6.2.6. *Dedicated electro-mechanical models for piezoelectric transducer design*

Modeling is a key step on the design of mechanical energy harvesters in order to find guideline rules for their optimization. Several models have been proposed in the literature. Electromechanical models based on the Rayleigh-Ritz approach [DUT 07] and analytical distributed parameters [ERT 08] use a very precise description of the mechanical aspects and electromechanical coupling, but are limited to a resistive load. However, single degree of freedom models that could be used to evaluate the

design of more complex electrical loads have been proposed [ROU 04b, BAD 05, LEF 05], but they use a simplified description of the electromechanical coupling; thus, they cannot account for higher vibration modes of the harvester. Finite Element Method (FEM) models coupled with SPICE model for the load description have been also implemented [ELV 09, YAN 09b] improving the precision compared to previous models, although it requires complex automation routines to perform a simulation.

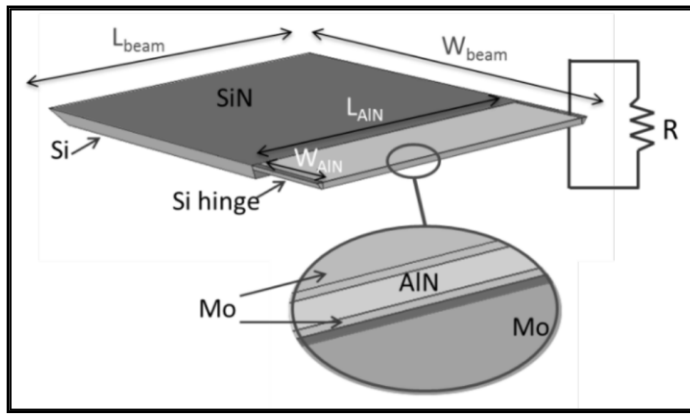
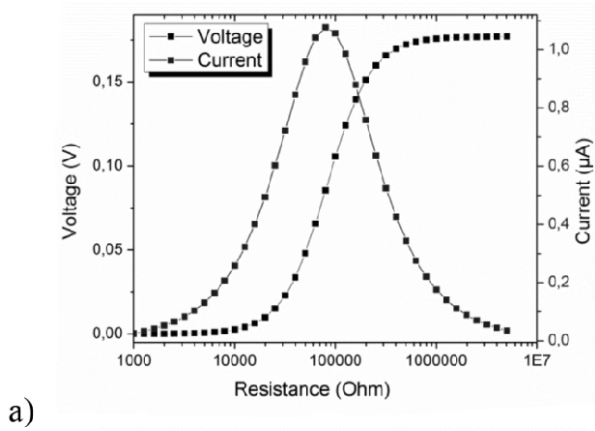


Figure 6.14. *Structure of the modeled piezoelectric energy harvester depicting the parameters modified for each device. The inset shows the thin piezoelectric three layers (Mo/AlN/Mo). A resistive load is connected to the device using a SPICE model*

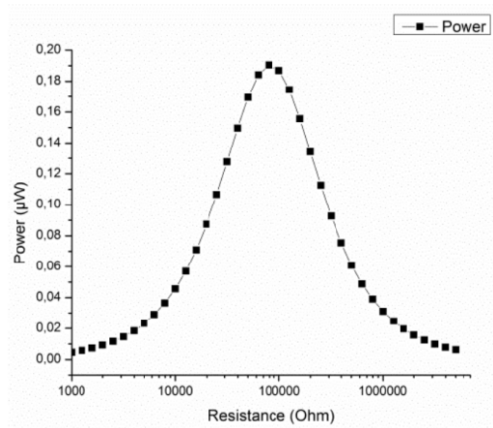
On the framework of the Nanofunction project, FEM coupled with SPICE models have been developed considering the mechanical, piezoelectric and electric equations of a mechanical harvesting device using COMSOL Multiphysics. The coupling was made within the same software avoiding complex routines.

To validate this approach, the fabricated and tested devices presented in section 6.2.3 were modeled when connected to a resistive load, although more complex structures and circuit loads can be simulated thanks to the FEM and SPICE descriptions.

The simulated structures (see Figure 6.16) consisted of 13,000 mesh elements (hexahedral and prism elements). The thickness of the different layers considered in the simulation were: Si substrate (400 μm), SiN (300 nm), both layers of Mo (300 nm) and AlN (1 μm). Two device dimensions have been simulated (see Table 6.1) for an input acceleration of 1g. Typical voltage, current and power graphs as a function of the resistance are shown in Figure 6.17 and the summary results of both devices are presented in Table 6.2.



a)



b)

Figure 6.15. *Simulated electrical output of a typical mechanical energy harvester, in this case device 1 (see the dimensions given in Table 6.1). a) Voltage and current in function of a resistive load; b) Power output in function of a resistive load. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Parameter	Device 1	Device 2
Resonance frequency (kHz)	1.66	3.17
Maximum cantilever deflection (μm)	4	2
Optimal resistive load (kΩ)	79.4	79.4
Optimal voltage (V)	85.5	87.6
Optimal current (μA)	1.08	1.1
Optimal power (nW)	190	190

Table 6.1. *Performance of the simulated devices for an acceleration of 1 g*

Parameter (mm)	L_{beam}	W_{beam}	L_{AlN}	W_{AlN}
Device 1	7.2	9	6.9	2
Device 2	5.2	6.5	4.9	1.5

Table 6.2. *Dimensional parameters of the two simulated devices*

The simulated performances of the devices are very similar in terms of electrical output (optimal load, voltage, current and power), the main differences are the resonance frequency, which is almost twice for the smaller device at the same time that the maximal displacement is divided by 2. Comparing these simulation results with the experimental data from section 6.2.3 reveals that the resonance frequency and the optimal load are very close to the simulated values (mainly for device 1). The electrical performances are in the same order of magnitude although in general underestimated by the simulation. This global underestimation has been previously observed on FEM simulations by Yang *et al.* [YAN 09b]. Many sources of error could explain these differences: the simulated devices geometries are not exactly the same as the fabricated devices; the intrinsic properties of the different materials could differ slightly from those considered on the simulation and some errors on the measurement could also be present.

6.3. Electromagnetic energy transducers

6.3.1. *Introduction*

Electromagnetic (inductive) harvesting is based on electromagnetic induction, i.e. a time varying magnetic field induces an electric current into a conductor according to Faraday's law. This principle, widely used in electric power generators, is also utilized for vibration energy harvesting at the microscale. A time varying magnetic field can be generated by movements, i.e. when the electrical conductor moves relative to the magnetic field, a voltage is induced in the conductor. Typically, the conductor is a coil, an inductor. Figure 6.16 illustrates this energy harvesting principle.

6.3.2. *State-of-the-art devices and materials*

The electromagnetic energy harvesters which have been researched so far are either macrosized discrete component structures or miniaturized structures utilizing MEMS fabrication techniques. However, a common aspect of the electromagnetic harvesters developed is that macrosized permanent magnets (PMs) are used to provide the required magnetic field. The development of films of PMs is still a

challenge. It was also concluded by Arnold [ARN 07] that power density decreases as the dimensions of the device are reduced. So, integration of electromagnetic energy harvesters is still an open field for research. So we can divide our literature review section into two parts – macrosized electromagnetic energy harvesters which are made up of discrete components and MEMS fabricated electromagnetic energy harvesting devices.

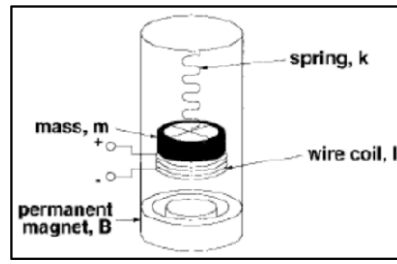


Figure 6.16. *The coil and the magnetic field move relative to each other, inducing a voltage $V = -d\varphi/dt$ in the coil*

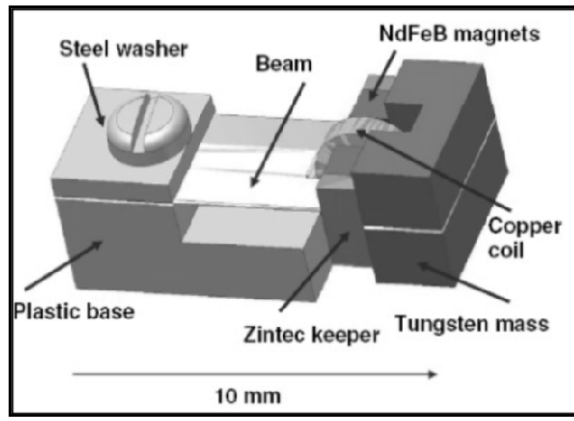


Figure 6.17. *An electromagnetic generator with an inertial mass and magnets on a cantilever and a stationary coil [BEE 07b]*

The modeling, simulation, manufacturing and testing of a cantilever spring-based moving magnet generator was described in [ELH 00] and [ELH 01]. A *C*-shaped

core of a soft magnetic material enclosed by a pair of NdFeB PMs was attached to the free end of a cantilever whose other end was anchored to a fixed frame. The *C*-shaped core acts as an easy return path for the magnetic field so that the flux density in the air gap is increased.

A fixed copper coil with 27 turns was attached to the fixed frame, thus allowing a relative displacement between the coil and the magnets when a base excitation is applied to the structure. 530 μW of power was generated of a 0.24 cm^3 total volume at 322 Hz and excitation amplitude of 25 μm. The excitation acceleration level used was very large and is not realized in many applications. The same structure generated approximately 40 μW at 1.2 g.

A smaller version of the electromagnetic harvesters presented in [JOH 03] was described in [BEE 07b] and [TOR 08]. The group from the University of Southampton reported this electromagnetic generator consisting of four NdFeB magnets located on an etched cantilever and a coil located in the moving magnetic field. At a frequency of 52 Hz (0.59 m/s^2), they measured 46 μW over a load resistance of 4 kΩ. The 3D model of the device is shown in Figure 6.17, and its volume is about 0.15 cm^3.

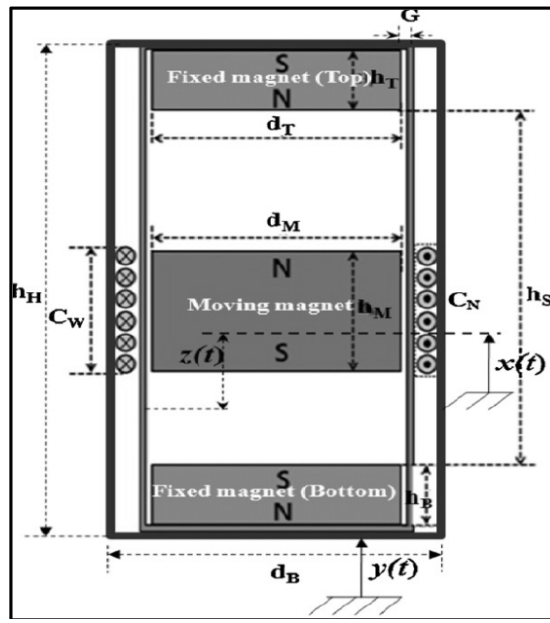


Figure 6.18. *Schematic of the generator mentioned in [FOI 12]*

There are a number of generators that replace the mechanical part of the resonator, i.e. the spring, with a magnetic spring based on the repulsion force between same polarity magnets [SAH 08]. Recently, Foisal *et al.* used the same kind of concept [FOI 12]. Figure 6.18 shows the construction of this generator. It consists of two similar magnets fixed on the two ends of the generator. Another moving back-to-back magnet is placed in the middle so that the repulsion force between the magnets keeps the moving magnets suspended between the two fixed magnets. A coil is wrapped around the housing of the generator. When the housing vibrates, the suspended moving magnets start to vibrate, and an induced EMF is generated in the coil, as the flux lines cut the coil. Thus, the magnetic repulsive force created by two fixed magnets on a moving mass works as a magnetic spring cantilever. A wire-wound copper coil is wrapped horizontally around the outside of the inner cylinder. The outer cylinder is used for the generator housing. When an external mechanical vibration is applied to the structure, the middle magnet will start to oscillate due to the magnetic repulsion of the two fixed magnets, so an AC voltage will be induced in the coil. Initially, a single frequency energy harvester was optimized in terms of the number of turns, coil width and coil position. Finally, two configurations of a multigenerator were fabricated. In model A, four individual generators are placed side by side; whereas in model B, the generators are placed one above the other. Both models can operate in the 7–10 Hz frequency range. The power densities of model A and model B are 21.92 $\mu W/cm^3$ and 52.02 $\mu W/cm^3$, respectively, at an acceleration of 0.5 g.

Electromagnetic energy harvester reported in [BOU 09], consists of stacked layers of housing, coil, spacer and mechanical resonator. The mechanical resonator is a flexible printed circuit board (PCB)-part sandwiched between two rigid PCB-parts (FR4) that serve as a frame. The flexible part of the resonator is a polyimide film that is 50 μm thick; on each side of the polyimide film a copper layer of 35 μm thickness is electrodeposited. The flexible part is laser-cut to the appropriate shape to fix the resonant frequency of the resonator. Since the harvester is in the standard configuration, two PMs are magnetically attached to both sides of the flexible parts to generate the required magnetic field. These magnets also act as active proof mass which define the resonant frequency of the harvester. Two copper wire-wound coils are used as electrical transducers that convert the deflection of the resonator into an electrical signal. The fabricated energy harvester has a power density of 44 μW/g and weighs 8.12 g.

In 2012, a group from Southampton University made an interesting publication in terms of magnetic arrangement by introducing the concept of the Halbach array in energy harvesting applications [ZHU 12a]. The Halbach array consists of two sets of magnets, i.e. main magnets and transit magnets. Their superimposition causes the concentration of field on one side of the array while cancellation of field on the other side.

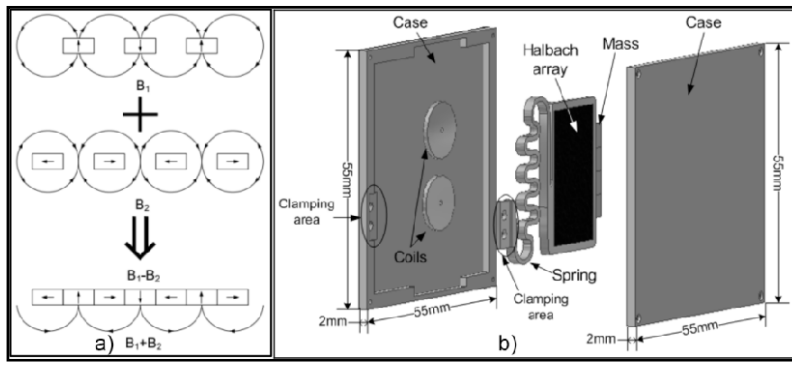


Figure 6.19. *a) Principle of the Halbach array; b) different components in the planar electromagnetic energy harvester using the Halbach array [ZHU 12a]*

Figure 6.19(b) shows the construction of the planar electromagnetic energy harvester using Halbach array. Two coils are attached to the case. A meander spring that carries the Halbach array and the inertial mass is clamped with that case. With external vibration, the Halbach array moves laterally due to the meander spring. The magnetic flux line cut by the coil induces voltage. Field strength at the active side of the Halbach array is measured to be about nine times than that at the quiet side. Thus, the electromagnetic field strength of the Halbach array is greater than that of conventional layouts of magnets of the same total volume. At low vibration level, the Halbach array does not show any advantage over conventional layouts. However, when the vibration level is increased so that the displacement of the magnets is comparable to the outer diameter of the coil, the energy harvester with a Halbach array has a 40% higher output power. Halbach arrangement can improve electromagnetic coupling in a limited space. This is the minimum space arrangement of magnets for a macroscale device with highest efficiency. Another benefit of the Halbach array is that due to the existence of an almost-zero magnetic field zone, electronic components can be placed close to the energy harvester without any chance of interference, which can potentially reduce the overall size of a self-powered device.

Harvesting energy from vibrations with multiple frequencies was discussed in [YAN 09a]. The structure consists of three PMs attached to an acrylic beam. Opposite each magnet, a printed coil with 10 turns is placed on a substrate using PCB technology.

The authors claim that energy can be harvested under the first, second and third vibration resonant modes of 369, 938 and 1184 Hz, respectively. The maximum output voltage and power from the first and second modes are 1.38 mV and 0.6 μW,

and 3.2 mV and 3.2 μW, respectively, for an excitation level of 14 μm. Although the authors showed the feasibility of harvesting energy from multiple frequencies, many design considerations were missed. First, at the second mode, the voltage generated from the first and third coils are 180 degrees out of phase, which requires the implementation of special circuitries in order to avoid signal destruction. Second, the voltage generated at the third mode is too low to be utilized, i.e. 0.0012 mV. Finally, the acceleration used was high, 0.76 g, and the nonlinearity effect that arises from the clamped-clamped supporting beam was not taken into account.

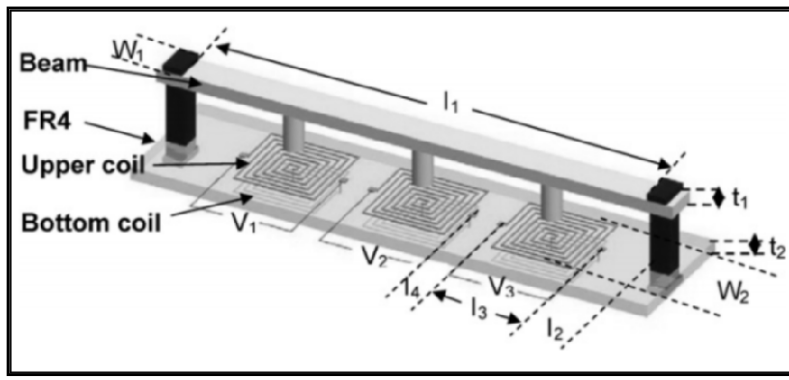


Figure 6.20. *Schematic drawing of the FR4 energy harvester [YAN 09a]*

So far we have discussed the published work on electromagnetic energy harvesting utilizing discrete components. This section presents a comprehensive survey of the most important reported work on the MEMS-based electromagnetic energy harvesters, including the working principles and configurations utilized.

The first vibration-based electromagnetic generator capable of generating 0.3 μW at an excitation frequency of 4.4 KHz and 0.5 μm vibration level was described in [WIL 96, SHE 97] with a generated voltage of only 8 mV. The structure used was a fixed planar micromachined gold coil with 13 turns, and a seismic 0.3 mm^3 SmCo PM weighing 2.4 mg was attached to a micromachined membrane using a polymide solution. The total volume of 25 mm^3 resulted in a small power density of 12 $\mu W/cm^3$. The design demonstrated that power generation of about 1 and 100 μW at 70 Hz and 330 Hz, respectively, was feasible. The main drawback of that design is the low induced voltage, which is the result of the low number of turns of the coil and the low magnetic field cutting the coils due to the open-circuited magnetic circuit design.

Koukharenko *et al*. [KOU 06] discussed the development and the testing of a laterally moving cantilever-based wound coil moving between a set of PMs. A copper coil with 600 turns is attached to a paddle supported by a micromachined beam cantilever, as shown in Figure 6.21. A housing of two perspex chips was constructed to accommodate the NeFeB rare earth magnets. The structure was designed to oscillate laterally, cutting the magnetic field to produce electric power. A total generator size of 100 mm^3 produces 0.1 μW of power at 1.6 KHz with a 0.4 g vibration source. As reported in [KUL 06] by Kulkarni *et al.*, the same structure produced 0.148 μW at an 8.08 kHz resonant frequency and a 3.9 m/s^2 acceleration. This design suffers from high parasitic damping between the copper wires and the housing, which in turn leads to a very small amount of generated power. An improved design using an electrodeposited copper coil rather than the wound coil was tested, as described in [KUL 06]. A 2 μm copper seed layer was sputtered on the paddle surface and then a mold 10 μm thick was spun, patterned and developed before the electrodeposition. A 65 turn coil with a silicon paddle resulted in a total oscillating mass of 0.014 g. The microgenerator generated a maximum power of 23 nW on a load of 52.7 Ω for an acceleration of 9.8 m/s^2, at a resonant frequency of 9.83 kHz. It should be recognized that in both these designs the generated power is very small due to the parasitic damping and small moving mass, which directly affects the amplitude of the power generated and the level of the required excitation frequency.

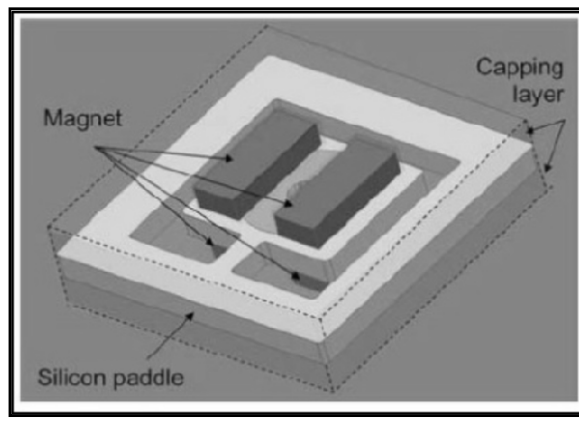


Figure 6.21. *Micromachined moving coil vibration-based electromagnetic energy harvester*

As described in [WAN 07], Wang *et al.* proposed a moving NeFeB magnet attached to a micromachined spiral copper spring that oscillates with respect to a

two-layer fixed micromachined spiral copper coil when a sinusoidal excitation is applied. Experimental results show that the prototype microgenerator can generate an open-circuit voltage of 60 mV AC peak to peak with 121.25 Hz input frequency and an acceleration of 1.5 g. Because the generator was tested with an open circuit, no generated power was reported.

The same group later modified the structure a little to accommodate two coils, one above and one below the planar spring [WAN 09]. The top coil and the bottom coil can generate the same electrical energy because of the symmetrical arrangement of the sandwiched structure. So the total electrical energy is increased after top coil and bottom coil are connected in series and the energy conversion efficiency is higher compared with single coil structure. If the sandwiched structure is sealed, the air damping generated by the inner air will decrease the amplitude of the magnet greatly and then influence the energy conversion efficiency. The air channel in silicon frame can overcome this disadvantage, decrease the air damping and then the output performance of the energy harvester can be increased further. The resonant frequency of the prototype is 280 Hz. The prototype can generate maximal load voltage of 142.5 mV and load power of 17.2 μW when the input vibration acceleration is 10 m/s^2.

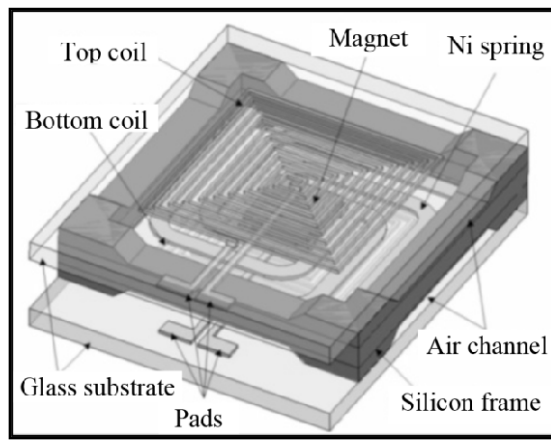


Figure 6.22. *Modified version of the generator proposed by Wang et al. [WAN 07] is described in their later work [WAN 09]*

In 2009, Jiang *et al.* [JIA 09] reported a harvester that is composed of a bidirectional micromagnetic array and serially connected microcoils. The electrical power is generated due to the relative motion between the magnetic array and

microcoils. The voltage output can be increased by connecting the microcoils in series.

Multifrequency MEMS-based electromagnetic energy harvester has been presented by Sari *et al.* [SAR 07, SAR 08]. The generator consists of multiple cantilevers with different resonant frequencies (i.e. different beam lengths). Identical coils have been deposited on the cantilevers. An NdFeB PM has been fixed at the center of the chip in order to provide the magnetic field necessary for the transduction, as shown in Figure 6.23. The load voltage of one cantilever is measured as 3.5 mV; when 40 beams are connected in series, the total load voltage is about 18 mV, with an output power of 0.4 μW over a frequency band of 300 Hz. Although the operating frequency band is fairly large, the output power is only less than 2% of the output power if all the cantilevers are tuned to the same frequency. In addition, the reported excitation acceleration level is very high, e.g. ≈49 g.

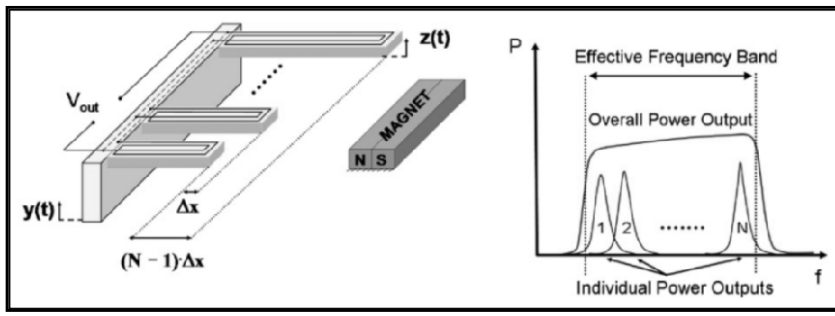


Figure 6.23. *Multicantilever electromagnetic generator proposed in [SAR 07] and [SAR 08]*

Another multifrequency sandwich-type electromagnetic vibration energy harvester has been reported recently [CHE 12]. Schematic design of the vibration energy harvester is shown in Figure 6.27. The harvester is composed of three resonant structures with different natural frequencies. The structures are two cantilevers each with bilayer coils and a plane spring with a magnet, respectively. The harvester takes advantage of three resonant structures and multilayer coils to increase the frequency range, voltage and power.

The different cantilevers with copper coils were designed to adapt to different frequencies. The plane springs with ellipse loop or *S* loop are designed to decrease the natural frequency and enhance the vibration amplitude. So the resonant frequency can be low enough to adapt to environmental frequency well.

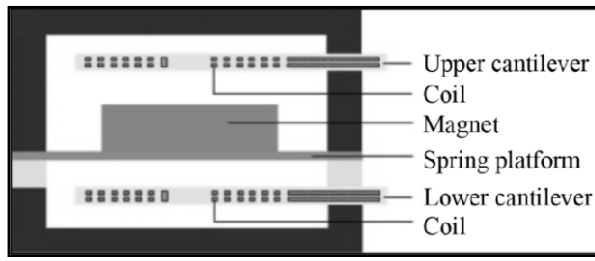


Figure 6.24. *Schematic of the multi-frequency sandwich type electromagnetic vibration energy harvester [CHE 12]*

Recently, nonlinear mechanisms have been widely incorporated in energy harvesting systems. The nonlinearity has the advantage of widening the effective bandwidth of the system. In 2009, Cottone *et al.* introduced a non-resonant (nonlinear) oscillator concept. The experimental setup used by the group is shown in Figure 6.25. They used the magnetic repulsive force between two opposite polarity magnets which are facing each other to introduce the nonlinearity. Later, this same concept was used by many researchers [COT 09, FER 11, WAL 12, TAN 11, AND 10] to utilize the effect of bistability to broaden the bandwidth.

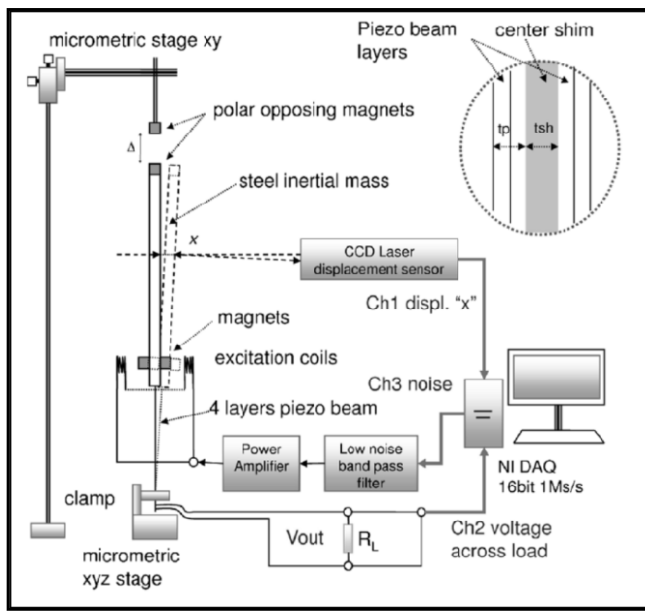


Figure 6.25. *Experimental setup used by Cottone et al. to introduce nonlinearity [COT 09]*

Nonlinearity could also be introduced mechanically by large deformation of the spring arms of harvesters. When deflection is small, the relationship between spring reaction force and deflection is linear. But for large deformations, in addition to linear bending, additional stretching effect also comes into play. This stretching is responsible for spring hardening effect. Dai *et al.* [DAI 12] showed by topology variation of spring arms that for angled spring arms, the nonlinear stiffness becomes optimum. So, a maximum bandwidth of 35 Hz is also obtained for this spring arm.

The following table compares the results from different published electromagnetic energy harvesters over the past few years.

Reference	Volume (mm^3)	Acceleration (m/s^2)	Frequency (Hz)	Voltage (mV)	Power (μW)	Load (Ω)
Macrosized Electromagnetic Energy Harvesters						
Yang *et al.*	2,700	18.64	40–80	9	0.4	50
Bouenden *et al.* 2009	1450	9.8	98	275(approx)	357.28	40
Xing *et al.* 2009	69X103	5.6	54	600	74 × 103	1
Yang *et al.*	324	7.45	369, 938, 1184	3.2	3.2	0.7
Zhu *et al.*	12.1X103	4.91	45	1.6	150	4,400
Foisal *et al.*	28X103	4.91	7–10		154(approx)	
MEMS-based Electromagnetic Energy Harvesters						
Wang *et al.*	315	10	280	142.5	17.2	81
Peng *et al.* 2011	660	4.91	242	28	0.55	37
Chen *et al.*	640		235	172	10	90
Tao 2012	20	9.81	365	0.021		

Table 6.3. *Different published electromagnetic energy harvesters over the past few years*

6.3.2.1. *Linear electromagnetic energy harvester design*

As can be seen from the literature review, most of the work is focused on linear resonator-based structures where a resonator is fabricated (either on macroscale or on MEMS scale) which will have a particular resonant frequency. On either side of the resonant frequency, the response falls off quickly. But at that resonant frequency, the harvester produces a significant amount of power. So here we will discuss the design and simulation of an electromagnetic energy harvester that has a particular resonant frequency.

A linear resonator structure intending to move easily along the in-plane direction has been designed. The schematic of the resonator structure is shown in Figure 6.26(a). On two sides of the central platform, meander springs are attached. The design is good for fabrication using MEMS processing techniques due to its small dimensions. So silicon has been chosen as the structural material for our simulations and calculations purpose. Detailed dimensions of the designed structure and material properties of silicon are listed below:

– length of the central paddle = 2.5 mm;

– width of the central paddle = 2.5 mm;

– thickness of the central paddle = 0.2 mm;

– width of the spring = 50 μm;

– mass = 3 X 10^{-6} Kg;

– Young's modulus of silicon = 165 GPa;

– density of silicon = 2330 kg/m^3.

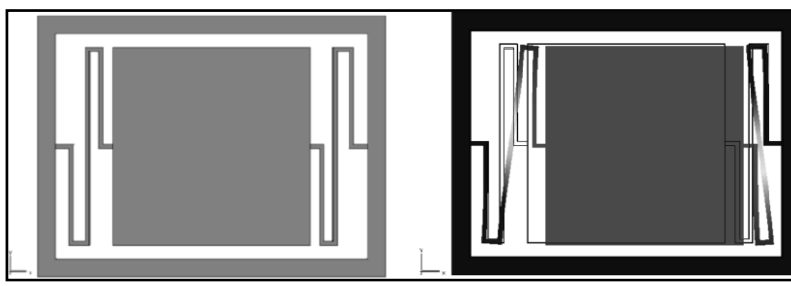


Figure 6.26. *a) Schematic of the resonator structure; b) displacement of the device at first resonant frequency. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Mechanical simulations of the resonator are done by COMSOL Multiphysics software. Simulated result of the structure shows that it has a resonant frequency of 1,582 Hz. The next two modes are at 3805 and 4549 Hz. The displacement of the structure in its first mode of vibration is shown in Figure 6.26(b). The unity of measure of the spring constant is 296.1 N/m, newtons per meter. Maximum stress that is generated within the structure is 0.21 MPa, which is much smaller than the yielding stress of silicon.

For electromagnetic simulation, we have chosen NdFeB grade 35 PMs. The coil in this case has an outer diameter of 2.5 mm and inner diameter of 0.3 mm. The dimensions of the magnets are $2.5 \times 0.5 \times 1$ mm^3. Since the design is ideal for batch fabrication, we have taken the micro coil for our simulation purpose. The coil has 80 turns. Thickness of the coil is 100 μm. We have already seen in the literature review section that Halbach array magnetic arrangement has a special characteristic that on one side of the array flux gets nullified whereas on the other side of the array magnetic flux is reinforced [ZHU 12a]. In our design, we have taken a five-magnet Halbach array arrangement to increase the magnetic flux linkage. The simulation result from Maxwell 2D solver is shown in the figure below.

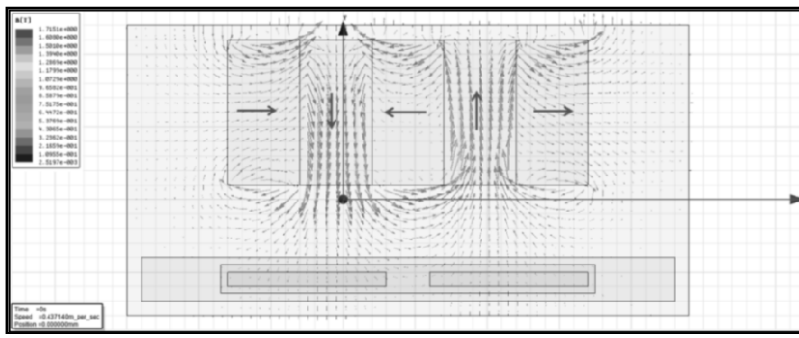


Figure 6.27. *Electromagnetic simulation of the model and magnetic flux line distribution is shown. The orientations of the magnets are marked by colored arrow. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

From this simulation, the change of flux linkage with respect to relative movement between magnets and coil is plotted, and from the slope of the curve, the rate of change of magnetic flux per turn is found to be 0.00172 for an input acceleration of 0.1 g and when the distance between the magnet array and coil is set 0.2 mm. The variation of load power and load voltage with load resistance is shown in Figure 6.28 for different distances between the magnet arrays and the coils. The same variation for different input accelerations is shown in Figure 6.30. Maximum power of 7.64 μW is generated for a load resistance of 554 Ohm for d = 0.2 mm and input acceleration of 0.1 g.

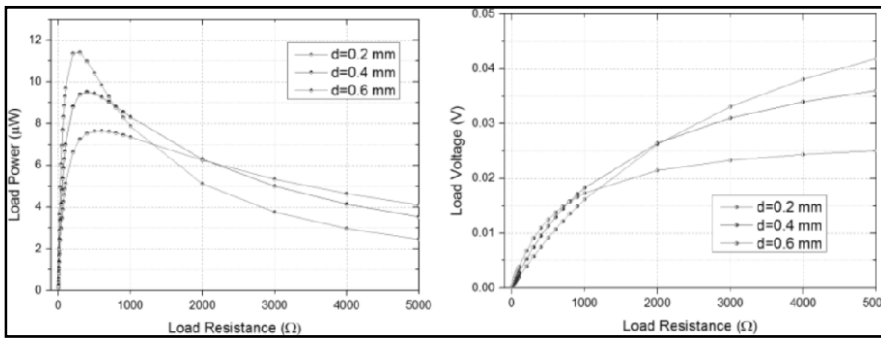


Figure 6.28. *Variation of load power and load voltage with load resistance for different distance (d) between magnet array and coil. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

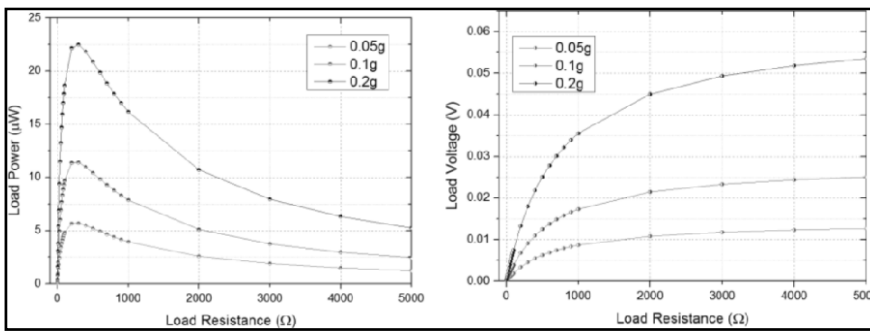


Figure 6.29. *Variation of load power and load voltage with load resistance for different input accelerations. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

6.3.3. *Vibration energy harvester exploiting both the piezoelectric and electromagnetic effect*

In order to harvest more energy from vibrations, some researchers have combined multiple transduction mechanisms in a single device. Hybrid vibration energy harvesters are devices that exploit two or more methods of transduction (typically electromagnetic, piezoelectric and electrostatic) for conversion of vibrational energy into electrical energy. A novel hybrid energy harvester integrated using both piezoelectric and electromagnetic energy harvesting mechanisms was reported by Yang *et al.* [YAN 10]. The device consists of a piezoelectric cantilever of multilayer piezoelectric transducers, PMs and double-layer planar copper coils

fabricated in PCB. They explored various combinations of relative position of coils and magnets on the lead zirconatetitanate (PZT) cantilever end and the poling direction of magnets on the output voltage of the energy. The maximum output voltage and power from the PZT cantilever are 0.84 V and 176 μW, respectively, under the vibrations of 2.5 G acceleration at 310 Hz. The maximum output voltage and power from the coils are 0.78 mV and 0.19 μW at the same vibration level.

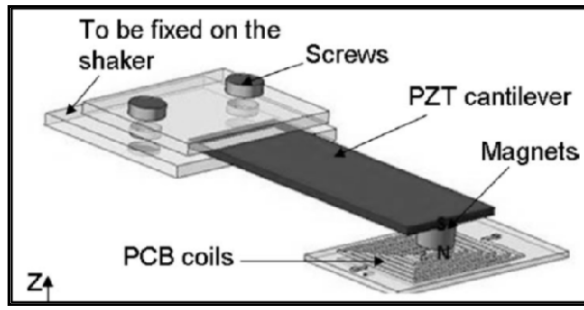


Figure 6.30. *Hybrid energy harvester using electromagnetic and piezoelectric transduction [YAN 10]*

Challa *et al.* coupled piezoelectric and electromagnetic energy harvesting techniques to provide higher electrical damping within the system [CHA 09]. They added an electromagnetic component to a primary piezoelectric energy harvesting device resulting in better matching of the total electrical damping to the mechanical damping in the system. The first coupled device had a resonance frequency of 21.6 Hz and produced a peak power output of ~332 μW, resulting in a 30% increase in power output, compared to 257 and 244 μW obtained from the optimized, stand-alone piezoelectric and electromagnetic energy harvesting devices, respectively. A second coupled device, utilizing the d_{33} piezoelectric mode, produced a 65% increase in power output over the corresponding single harvesting mode devices. Tadesse *et al.* reported another multimodal energy harvesting device combining electromagnetic and piezoelectric energy harvesting mechanism [TAD 09]. The device consisted of piezoelectric crystals bonded to a cantilever beam, the tip which had an attached PM oscillating within a stationary coil. The power generated from the fabricated prototype was found to be 0.25 W due to the electromagnetic mechanism and 0.25 mW due to the piezoelectric mechanism at 35 g acceleration and 20 Hz frequency.

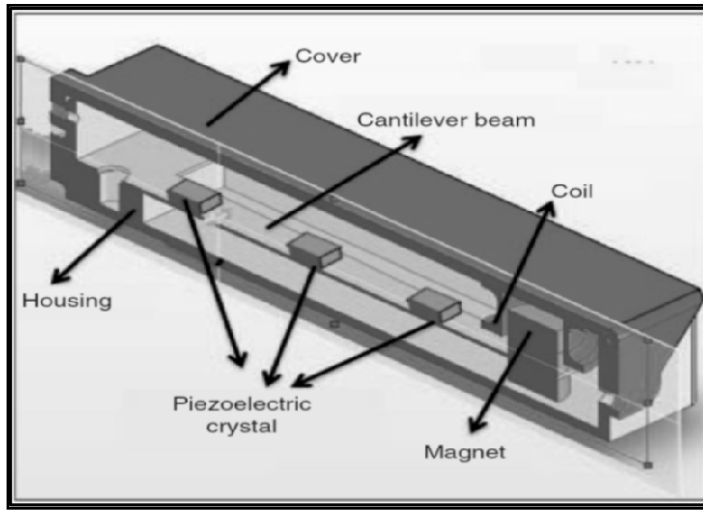


Figure 6.31. *Multimodal energy harvesting device [TAD 09]*

Another hybrid vibration energy harvesting mechanism integrating the effects of both electromagnetic induction and piezoelectricity was reported by Chen *et al.* [CHE 11]. Their structure consisted of three modules. The first module was an electromagnetic induction module comprising two pairs of bulk NdFeB PMs and one enameled copper coil. The second module was a piezoelectric energy harvesting module utilizing impact mode. The last module was another piezoelectric energy harvesting module based on impact-induced vibration. They stored the electric energy in capacitor via bridge rectifier. At vibration excitation amplitude of 4.5 mm and frequency of 13 Hz, it was found that, the harvested electric energy was 57.2 μJ due to impacted piezoelectric components, 429.3 μJ for piezoelectric components under impact-induced vibration and 6547.2 μJ from the electromagnetic induction component, in 30 s.

Sang *et al.* developed a hybrid energy harvester consisting of a cantilever beam bonding with two piezoelectric plates for piezoelectric energy conversion, and a PM attached at the end of the beam as a tip mass [SAN 12]. The maximum load power generated by the hybrid harvester was 10.7 mW on the optimal load resistance of 50 at the resonant frequency of 50 Hz with the acceleration of 0.4 g. The harvested power increased by 81.4% in comparison to 5.9 mW, which was produced by the stand-alone electromagnetic technique. Dayal *et al.* used a hybrid setup consisting of a piezostrip and electromagnetic harvester to provide sufficient voltage for the start-up operation of the energy harvester [DAY 12].

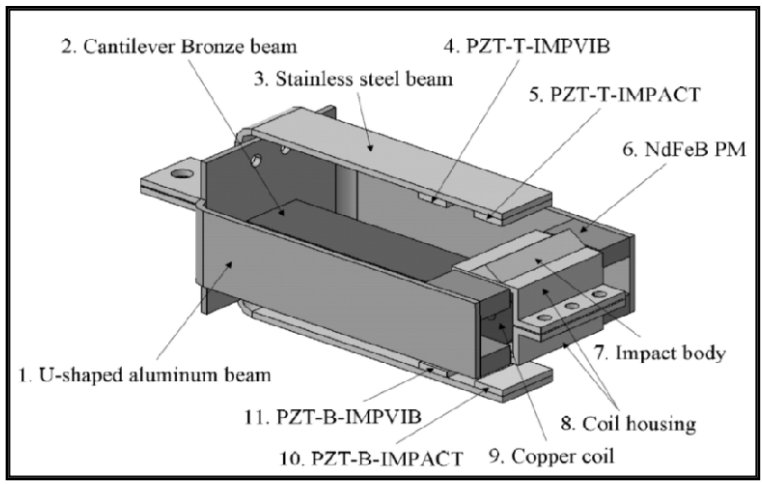


Figure 6.32. *Structure of the hybrid generator [CHE 11]*

6.3.4. *Device design*

An out-of-plane moving device consisting of four meandered cantilever structures holding a central movable platform was conceived. The central stage could be used to hold either a coil or an array of NdFeB magnets. The size of the device, made on 200 µm thick silicon wafer, is 8 mm × 8 mm excluding the frames. The central stage has a dimension of 5 mm × 5 mm, which is supported by four meandered cantilevers. The special meandered shape increases the effective length of the cantilevers, which in turn help to reduce the resonance frequency and increase the out-of-plane displacement of the central stage. Under an applied vibration of 1 g (9.8 m/s^2), the device resonated at a frequency of 95 Hz and produced a maximum deflection of 30 µm. The stress levels produced at the maximum deflection were well within the maximum tolerable limits.

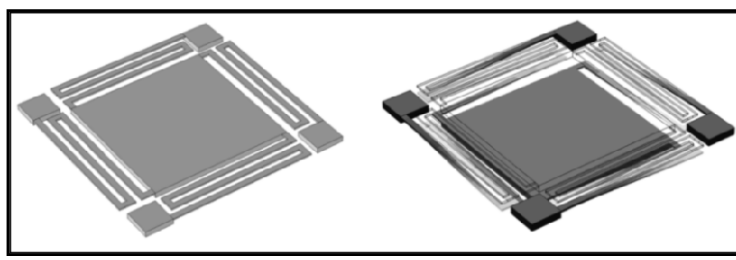


Figure 6.33. *Out-of-plane moving device structure and deflected position of the device. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

A copper microfabricated planar coil of 80 turns was mounted on the central stage and two six-magnet Halbach arrays were arranged above and below the coil.

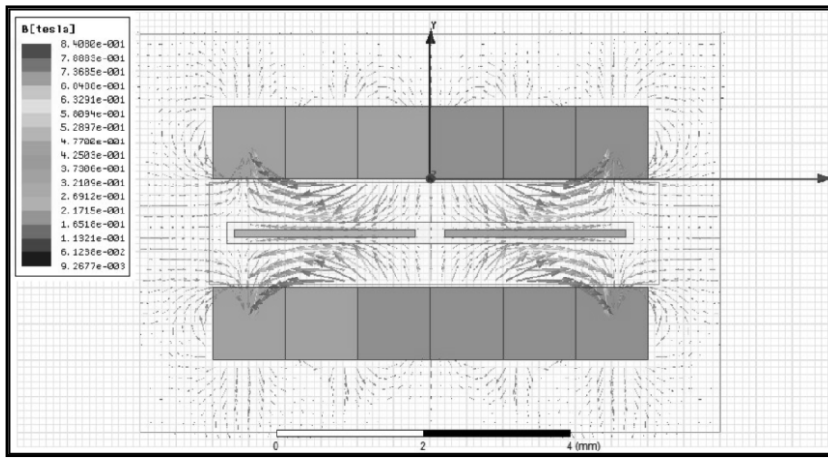


Figure 6.34. *Position of magnets and coils. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The change in flux linkage due to the vibration of the central stage induces electric potential in the coil. The change in flux gradient was 0.277 T/m. The simulation data were used to calculate the output voltage and power generated by the device. It was found that the device was able to generate a maximum power of 10 μW at a load resistance of 40 Ω. The output voltage at the maximum power level was found to be 6.5 mV.

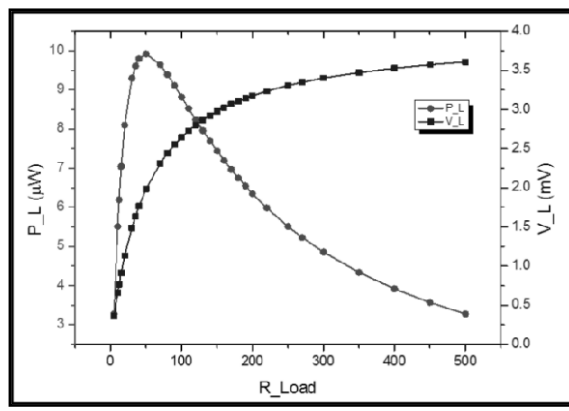


Figure 6.35. *Variation of load power and load voltage with load resistance*

It was found that the maximum power was generated at the same load resistance where the electromagnetic and parasitic damping was equal.

In order to realize a hybrid energy harvesting scheme, 0.5 μm thick piezoelectric AlN layer was deposited between aluminum electrodes on the meandered cantilevers of our simulated model (Figure 6.36). Silicon dioxide was used as an insulating layer between the silicon and the aluminum electrodes.

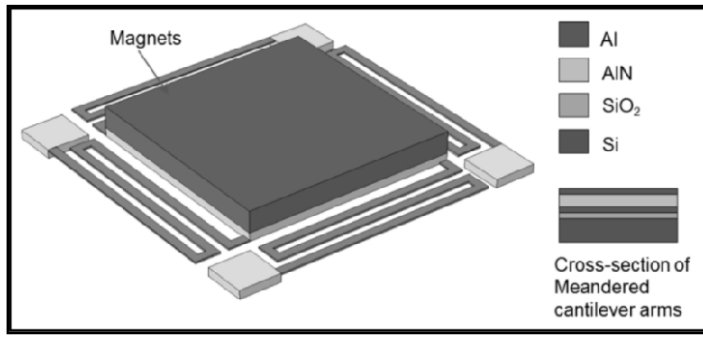


Figure 6.36. *Position of magnet array and cross-section of the cantilever beams. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

It was found from simulations that the maximum voltage generated for an external vibration of 1 g (9.8 m/s^2) was -3.8 V (Figure 6.37).

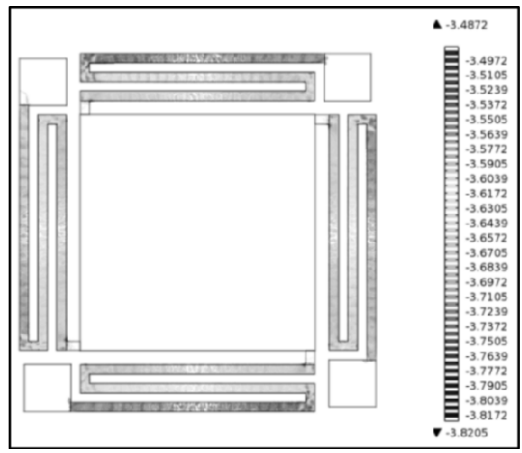


Figure 6.37. *Electric potential generated in the piezoelectric layer deposited on the meandered cantilever beams. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The maximum power generated from the piezoelectric transduction method is given by:

$$P = \frac{1}{2}CV^2 = \frac{1}{2}\frac{\epsilon A}{t}V^2 \quad [6.3]$$

where:

V = voltage across the piezoelectric material;

C = capacitance of the piezoelectric layer;

ϵ = permittivity of the piezoelectric material;

A = area of the piezoelectric layer;

t = thickness of the piezoelectric layer.

From equation [6.3], it was found that the maximum power harvested by the device using piezoelectric transduction was 0.132 μW.

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7

Thermal Energy Harvesting

7.1. Introduction

In most systems, a significant amount of power is wasted in heat. This is true at a global level [LAW 12] but also locally. In the specific framework of self-powered devices, e.g. autonomous sensor networks, there may be situations where heat is the only available source of energy. In more favorable cases where several sources of energy are available, it can be beneficial to combine them in order to increase the range of available resources and reduce the dependence of the sensor on environmental variations. There are several approaches to harvest thermal energy, which exploit either temperature gradient in space or temperature variation in time. Classical examples of these two approaches are thermoelectric harvesting and pyroelectric thermal energy harvesting, respectively.

In this chapter, we will present some recent advances in the field of thermal energy harvesting, starting with thermoelectric energy harvesting, with a focus on the prospects of materials nanostructuration. Research toward alternative solutions will also be presented. However, this chapter does not aim to be comprehensive. For instance, it will concentrate on experimental work and will not detail simulation issues and progress. In order to motivate the subjects that have been targeted here, a brief introduction about the basics is needed.

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7.1.1. *Basics of thermoelectric conversion*

Thermoelectric (TE) conversion is the most straightforward method to convert thermal energy into electrical energy, able to power such systems as autonomous sensor networks. It consists of taking advantage of the voltage difference, which is generated when a temperature gradient is maintained between the two contacts to a TE material (Seebeck effect). The Seebeck effect is primarily related to the difference in the energy distribution of free carriers between the two contacts. It is characterized by the Seebeck coefficient S. Generators can be built on this concept by assembling TE materials that are connected in series from an electrical point of view and in parallel from a thermal point of view, as schematically shown in Figure 7.1. The maximum efficiency, η_{max}, of such a thermoelectric generator (TEG) cannot exceed the Carnot efficiency limit, η_C:

$$\eta_C = \frac{T_H - T_C}{T_H} \qquad [7.1]$$

where T_C and T_H are the absolute temperatures of the cold and hot plates, respectively. In practice, it is even limited to lower values, both fundamentally due to Joule heating and thermal conduction across the material, and practically due to parasitic thermal paths and series resistances. Within the simplifying assumptions of a small temperature difference and no parasitics, η_{max} can be written as:

$$\eta_{\max} = \eta_C \cdot \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+\frac{T_C}{T_H}} \qquad [7.2]$$

where T is the mean absolute temperature and Z depends on the respective properties of the material in terms of thermal conductivity κ and electron conductivity σ. In a semiconducting material, heat conduction is mediated both by free carriers (electrons or holes) and by lattice vibrations (phonons), with respective contributions k_{el} and k_{ph} to thermal conductivity, respectively.

$$ZT = S^2 \cdot \frac{\sigma}{\kappa_{el} + \kappa_{ph}} \cdot T \qquad [7.3]$$

is a material parameter, which is used as the main figure of merit to characterize thermoelectric materials. A good thermoelectric material will be characterized by a large value of ZT, i.e. a large Seebeck coefficient, a large electron conductivity to reduce the Joule heating, and a low thermal conductivity to keep the temperature difference across the material.

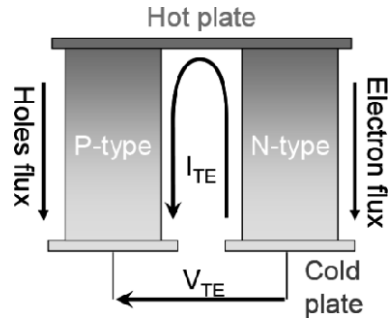

Figure 7.1. *Schematic structure of a TE generator cell. When a temperature difference is applied between the two plates, free carriers flowing from the hot plate to the cold plates allow a potential difference to be generated between the two cold plates*

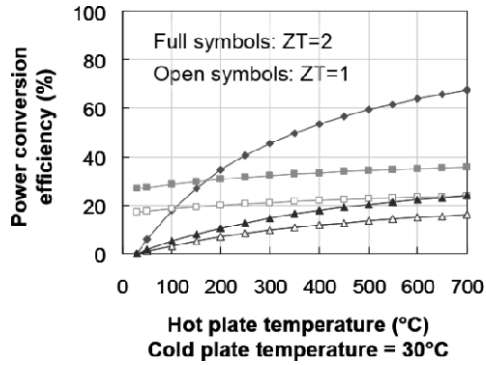

Figure 7.2. *Maximum power conversion efficiency calculated with equation [7.2]. Diamonds: Carnot efficiency η_C, squares: ZT dependent thermoelectric coefficient, triangles: maximum TE efficiency η_{max}*

Figure 7.2 shows how this maximum efficiency varies with ZT. It is clear from this figure that efficiency will be in any case limited for small values of $\Delta T=T_H-T_C$ and that large values of ZT are required.

7.1.2. *Strategies to increase ZT*

In principle, it is not straightforward to increase ZT. On the one hand, the Seebeck coefficient is also correlated to electron conductivity. This can be shown qualitatively, based on a first-order linearization of Boltzmann's equation, in the case of parabolic bands. S in semiconductors can then be expressed as:

$$S = \pm \frac{k_B}{q} \left[\frac{\int \frac{(\varepsilon - E_F)}{kT} \cdot \tau(\varepsilon) \cdot D(\varepsilon)\, v^2 \left[-\frac{\partial f(\varepsilon)}{\partial \varepsilon} \right] \cdot d\varepsilon}{\int \tau(\varepsilon) \cdot D(\varepsilon)\, v^2 \left[-\frac{\partial f(\varepsilon)}{\partial \varepsilon} \right] \cdot d\varepsilon} \right] \quad [7.4]$$

where k_B is Boltzmann's constant, v is the group velocity proportional to $\sqrt{\varepsilon}$, E_F is the Fermi level, τ is the energy-dependent scattering time, D is the density of states and f is the Fermi-Dirac statistics. $-\partial f / \partial \varepsilon$ is a bell-shaped function of width k_BT centered on E_F. By convention, S is negative for n-type materials and positive for p-type materials. It is usual to introduce the bulk Maxwellian integral, which is defined as:

$$\langle \varphi(\varepsilon) \rangle = \frac{\int \varphi(\varepsilon)\, D(\varepsilon)\, \varepsilon \left[-\frac{\partial f(\varepsilon)}{\partial \varepsilon} \right] d\varepsilon}{\int D(\varepsilon)\, \varepsilon \left[-\frac{\partial f(\varepsilon)}{\partial \varepsilon} \right] d\varepsilon} \quad [7.5]$$

for any function of energy φ(ε). Within this formalism, S is more simply expressed as [PIC 10]:

$$S = \pm \frac{k_B}{q} \frac{\left\langle \tau(\varepsilon) \cdot \frac{\varepsilon - E_F}{k_B T} \right\rangle}{\langle \tau(\varepsilon) \rangle} = \pm \frac{1}{qT} \left[\frac{\langle \varepsilon \cdot \tau(\varepsilon) \rangle}{\langle \tau(\varepsilon) \rangle} - E_F \right] \quad [7.6]$$

In the case of an isotropic band with conduction mass m_C, mobility is equal to:

$$\mu = \frac{q}{m_C} \langle \tau(\varepsilon) \rangle \quad [7.7]$$

which shows that S is not independent of free carrier mobility and therefore of electron/hole conductivity. On the other hand, thermal and electron conductivity are also correlated. In particular, the Wiedermann–Franz law

$$\kappa_{el} = \sigma \cdot T \cdot \left[\frac{\pi}{\sqrt{3}} \frac{k_B}{q} \right]^2 \quad [7.8]$$

couples σ and κ_{el} in degenerate materials. In semiconductors, a more general expression should be used, but with the same result of introducing a coupling between the flows of charges and heat associated with free carriers transport:

$$\kappa_{el} = \frac{\sigma}{q^2 T} \cdot \left[\frac{\left\langle \varepsilon^2 \tau(\varepsilon) \right\rangle}{\left\langle \tau(\varepsilon) \right\rangle} - \frac{\left\langle \varepsilon \tau(\varepsilon) \right\rangle^2}{\left\langle \tau(\varepsilon) \right\rangle^2} \right] \qquad [7.9]$$

These equations are valid for a single parabolic band, as well as in the case of a set of equivalent ellipsoidal bands such as the conduction band of silicon. They still use a simplified linear approach. In the presence of strongly varying potentials (e.g. due to nanoparticles, interfaces, confinement fields), more sophisticated approaches are needed, together with reliable experimental data.

Strategies to increase ZT first consisted of finding materials with large values of S, high electron/hole mobility and low lattice thermal conductivity. In practice (see Figure 7.3), materials with highly covalent inter metallic compounds of heavy elements (such as Pb, Hg, Bi, Tl, Sb or S, Se and Te) – or their alloys – featured the best compromise between these requirements [GAU 13]. However, most of these materials are rare or toxic. For instance, while most current commercial applications of TE generation in the low-temperature range (below 200°C) are based on Bi_2Te_3 alloys, Te is the 9th rarest element on Earth, and both Bi and Te are toxic, although less than Pb and As, respectively.

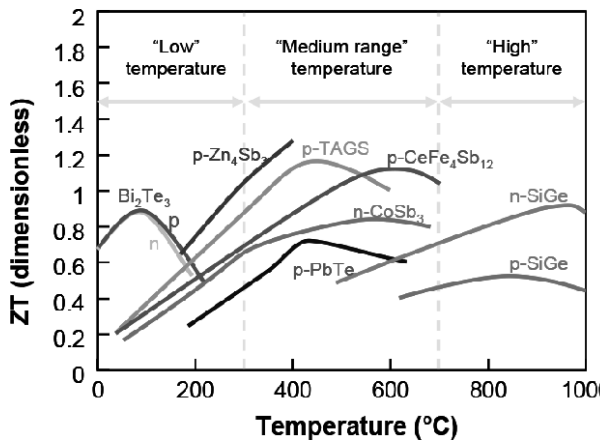

Figure 7.3. *Typical range of ZT values obtained with the most commonly studied bulk materials. ZT values hardly surpass 1. The denomination TAGS refers to compounds containing tellurium, antimony, germanium and silver such as, for instance, $(Ag_xSbTe_{x/2+1.5})_{0.15}(GeTe)_{0.85}$. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

However, as nanostructured materials have different electronic and vibrational properties from their bulk counterparts, they make it easier to engineer independently band structure, free carrier transport and phonon transport. Initially, reduced dimensionality was introduced as a means of increasing the power factor $S^2.\sigma$ by proper engineering of the band structure and density of states. Initial studies targeted superlattices [WHA 87, HIC 93a] and nanowires [HIC 93b]. However, in practice, the main interest of nanostructuration happened to arise from the reduction of lattice thermal conductivity [DRE 07]. Indeed, by introducing additional boundaries and local non-homogeneities in a material, it is possible to strongly increase phonon scattering, and even localize phonons, while keeping electron conductivity. Thus, much research is now devoted to the analysis of thermal conduction in nanostructured materials or materials that contain nanoscale constituents.

7.1.3. *Heavy-metal-free TE generation*

Generalized use of heavy metal compounds in applications that require the dissemination of large numbers of devices, such as sensor networks, raises clear environmental and recycling issues. The rarity of some key elements is also an issue. Solutions based on common elements such as silicon would make a breakthrough. However, materials with diamond or zinc-blende structures, such as Si, SiGe or III–V materials, feature high carrier mobility but at the same time low lattice thermal conductivities. Bulk silicon is ill-suited to thermoelectric application with figure of merit (ZT) values smaller than 0.01, while ZT values above 2 at 300 K are needed for useful power generation. Bulk SiGe is one of the best materials for thermoelectric generators, but operating at high temperatures. It is thus mandatory to study what can be expected from nanostructuration in these materials.

There has been considerable interest in the thermoelectric properties of Si/SiGe superlattices [KAT 98, SUN 99, HUX 02]. Moreover, it has been calculated that interface roughness of the interfaces in a Si/Ge superlattice reduces the thermal conductivity in both the in-plane and perpendicular directions [REN 06]. Performance is still limited by residual dislocations, due to lattice mismatch between SiGe alloys with different compositions [PAU 13]. This issue could in principle be solved with bottom-up grown 1D structures, which allow dislocation of free strain relaxation. Roughness engineering of semiconducting nanowires [HOC 08, BOU 08, MAR 10] have shown the most promise. Si-based nanowires alternating different Ge compositions along the growth axis show good prospects as well. However, up to now, they have been studied in the perspective of device applications, such as vertical tunnel-FETs [NAH 10], and their thermoelectric properties are mostly unknown. Another technique consists of nanostructuring materials using different

combinations of top-down and bottom-up processing steps to fabricate phonon glass/electron crystals materials [SOT 04].

A good understanding of phonon confinement and phonon scattering effects in these materials is key to any further phonon engineering. Since early experiments on confined optical phonons in GaAs-based systems [FAS 88], the influence of phonon confinement on electronic, optical, thermal and acoustical properties of materials has been demonstrated [BAN 95, MIT 99, STR 01, BAL 98a]. Due to microscale effects, macroscopic models of heat conduction such as Fourier's law of diffusive transport or the Cattaneao equation become invalid [MAJ 93, GOO 92, CHE 01], leading to incorrect predictions or to the transformation of some physical parameters into fitting parameters. For this reason, many researchers have focused their attention on different heat conduction formulations emanating from the Boltzmann transport equation (BTE) in an attempt to explain the size and time dependence of the heat transport in thin films [CHE 97, HYL 96], in nanowires [LID 03, BOU 07, LIU 05] and in free standing membranes [BAL 98b]. Suspended membranes, such as ultrathin Au [GRI 87], SiN [ZHA 03] and Si films [SOT 04, CUF 12], have proved to be a good test vehicle to study these issues experimentally and validate modeling approaches. This will be discussed in detail in section 7.2 while thermoelectric application of porous silicon will be presented in section 7.3.

7.1.4. *Alternatives to TE harvesting for self-powered solid-state microsystems*

In parallel, a different technique for thermoelectric energy harvesting is also explored. The spin Seebeck effect refers to the generation of spin currents and associated voltages in the presence of a temperature gradient in a ferromagnet [UCH 08]. Originally, it was thought to be a consequence of spin accumulation currents generated in the ferromagnet due to the different mobilities of the spin channels. This hypothesis was quickly discarded [XIA 10]. Current knowledge indicates the relevance of magnons, but this is not fully understood, in particular due to the influence and interaction with electrons [SIN 10]. From the application point of view, this concept has the advantage that the voltage difference is defined by the properties of the ferromagnetic material while electrical conduction takes place in a metallic line with no temperature gradient. This approach will be presented in section 7.4.

Another approach to overcome the intrinsic difficulty of maintaining a temperature difference across a conducting material consists of exploiting time variations of the temperature instead of spatial gradients. This process has been long considered as rather inefficient due to the thermal inertia of most systems. However, microelectromechanical systems (MEMS)-based concepts have emerged recently [PUS 12, HUN 12, LEB 11]. They have in common the use of a bilayer structure,

which spontaneously flips between two positions ensuring contact with a cold plate and a hot plate, respectively. With a proper temperature difference between the two plates and proper design, the bilayer can spontaneously oscillate. The problem of thermal harvesting is then turned into harvesting the oscillatory mechanical energy. Several new concepts have been proposed along these lines. They are gaining interest as MEMS scale down in size and oscillation frequency increases, thus increasing the efficiency of this new approach. Section 7.5 will give an example of integration of such a concept.

7.2. Thermal transport at nanoscale

Due to the large variety of promising technological applications, the concept of nanotechnology has become one of the most important and exciting fields encompassing many disciplines such as physics, chemistry, biology, medicine and engineering. At nanometric scale, material properties can be modified in comparison with the bulk counterpart. This is, in part, due to the effects of quantum confinement and also due to the increase of the surface to volume ratio. For example, a spherical particle with size of 30 nm has 5% of its atoms on its surface; at 10 nm this percentage has increased to 20%, while at 5 nm atoms at the surface account for almost/over 50% the total number [POO 03]. These factors can either enhance or degrade elastic, reactive, thermal, optical and electrical-properties.

Researching micro/nanofabrication has led to the discovery of novel materials, processes and phenomena at the nanoscale, which have in turn spurred technology growth at an astounding pace, while offering the first building blocks for the next green-industrial revolution.

The control of charge and heat transport in low-dimensional semiconductor structures has become a corner stone in these developments motivated, in part, by the increasing importance of thermal management, which is a consequence of the large power densities resulting from the continuous miniaturization of electronic components. On the other hand, the engineering of the thermal conduction opens a route to energy harvesting through, for example, thermoelectric generation. As a consequence, control of phonon generation, relaxation and propagation in the nanoscale is thought to hold the key to a number of scientific and technological advances.

One set of structures that have attracted a lot of attention is free-standing membranes, such as solids plates (slabs) or rods (bars) connected to solid substrate by the extremities. From single-atomic layers, e.g. graphene [BAO 09], to high purity and single-crystalline structure, e.g. Si membranes [SHC 13], these structures

have found use in a wide variety of interesting and important applications, including very sensitive sensors of forces [RUG 04] and mass [CHA 12a], low-loss macromolecule separator [STR 07], bolometer platforms [ERI 97, SIR 09] and opto-mechanical cavities [WIL 09], among others.

Moreover, as there is no interference from a substrate and as they can be fabricated following precise, controlled fabrication processes, these nanoscale objects facilitate the experimental analysis and comparison with theoretical models and constitute a textbook example of a nanoscale system. Their physical properties, e.g. electrical and thermal properties, can be dramatically different compared with thick samples or bulk counterparts, by orders of magnitude.

All these characteristics are of special interest from experimental and theoretical points of view.

7.2.1. *Brief review of nanoscale thermal conductivity*

Undoubtedly, the thermal conductivity, κ, is one of the most important and fundamental physical quantities. The thermal conductivity of a material governs its ability to transport heat and plays a fundamental role in the design and performance of the technological devices. The dominant carrier of heat energy depends on the type of material. It can be transported via charge carriers (electrons), lattice waves (phonons), electromagnetic waves (photons), or spin waves (magnons). For non-metallic, semiconductor and alloy materials, the dominant conduction process is the lattice thermal conduction, i.e. by phonons. A phonon is a pseudo-particle, which represents quantized modes of the vibrational energy of an atom or group of atoms in a lattice. Considering that the phonons are pseudo-particles, it is possible to associate an energy $\hbar\omega$ and a pseudo-momentum $p = \hbar q$, which obey Bose-Einstein statistics [SRI 90].

In a similar manner to electron energy, the phonon energy can be represented as a dispersion relation, i.e. a relationship between the phonon frequency and its wave vector. The slope of a dispersion relation curve determines the phonon group velocity, $v_g = d\omega/dq$. For the case of a bulk, the dispersion relation of phonons with low wave vector can be considered linear with the slope representing the sound velocity of the material. However, when the characteristic dimensions of the material decrease, this linear dependence no longer holds, and many discrete modes appear and the phonon energy is quantized. This spatial confinement affects the phonon group velocity, density of states, specific heat capacity, electron-phonon and phonon-phonon interactions, among others [BAN 95, BAL 98a, SOT 04, GRO 08, HUA 08, CUF 12, CHA 12, CUF 13]. Moreover, the decrease in dimensions puts an

upper limit on the phonon mean free path, because the acoustic wave cannot continue to travel in the medium due to the boundaries.

Recent experimental and theoretical reports point to an enhancement of the figure of merit, ZT, in thin films [MAJ 04, MAH 94, GOY 10, GHA 10, SIL 13], nanowires [BOU 08, HOC 08, DAV 11, MAR 12b, LIZ 12], superlattices [BRO 95, AKS 12, CEC 12, JHA 13] and suspended phononic crystals [YUJ 10, TAN 10, ELK 11], primarily as a result of the decrease of the thermal conductivity compared to the bulk counterpart, without a corresponding decrease in electrical properties. The reduction of the thermal conductivity in these systems has been associated with two principal factors: (1) the modification of the acoustic dispersion relation due to the additional periodicity (superlattices and phononic crystal structures) [HOP 10, REI 11, DEC 12] or spatial confinement of the phonon modes (thin films and nanowires) [BAL 98b, LID 03, HUA 07, MAA 11]; (2) the shortening of the phonon mean free path due to the diffuse scattering of phonons at the boundaries [HYL 96, ASH 97, LIU 04a, TAN 11].

To model heat transfer in nanostructures, advanced theoretical models are required, which can correctly take into account the frequency dependence of phonon-related properties. The majority of thermal conductivity models are derived from the phonon Boltzmann transport equation (PBTE) under the single-mode relaxation-time approximation [SRI 90]. For low-dimensional systems, Zou *et al.* [ZOU 01] classified the theoretical models into three types. The first model takes the bulk formulation for the thermal conductivity, introduces the modified dispersion relation caused by the spatial confinement and adds a boundary scattering rate to the total scattering rate through Mattiessen's rule [BAL 98b]. The second model uses the bulk dispersion relation and derives an exact solution of the PBTE after introducing diffusive boundaries conditions, according to a Knudsen flow model [HYL 96, ASH 97, WAL 99]. The third model, proposed by Zou *et al.* [ZOU 01], is a combination of these two approaches. This model takes the modified expression of the thermal conductivity, including the Knudsen flow model in addition to the modified dispersion relation. More recently, Huang *et al.* [HUA 07] developed one- and two-dimensional expressions for the thermal conductivity of thin films and nanowires, which include the modified expression of the relaxation time due to the boundaries.

The experimental measurement of the thermal conductivity involves two steps: the introduction of thermal energy into the system, heating, and the detection of the change of temperature or related physical properties due to the increase of the thermal energy, i.e. sensing. Both, heating and sensing, can be measured mainly by electrical or optical and/or a combination thereof. Table 7.1 summarizes measurements performed in Si nanostructures and reported in the past 10 years.

Reference	Nanostructure	Relevant dimensions (nm)	Type of measurement	Temperature (K)
[MAJ 13]	Inverse opals	18–38	Electrical, 3ω	30–400
[GRA 13]	Nanowires	50 and 200	Electrical, 3ω-SThM	Room temperature
[CLA 12]	Nanostructured Bulk	30–40	Electrical, commercial	2-300
[FES 12]	Nanowires	110–150	Optical, TDTR	Room temperature
[MAR 12a]	Periodic porous nanobridge	196	Electrical, 3ω	Room temperature
[WEI 12]	Porous nanowires	300–350	Optical, TDTR	Room temperature
[KIM 12]	Free-standing phononic crystal	500	Electrical, Joule heating	Room temperature
[FAN 12]	Mesoporous nanocrystalline thin films	140–340	Electrical, 3ω	25-315
[LIU 11]	Free-standing membrane	500 and 700	Optical, Raman thermometry	Room temperature
[WAN 11]	Nanocrystals	64–550	Electrical, 3ω	16-310
[YUJ 10]	Free-standing phononic nanomesh	22–25	Electrical, suspended heater and detector	80-320
[DOE 10]	Nanowires	30–300	Optical, Raman thermometry	Room temperature
[TAN 10]	Holey Si	100	Electrical, suspended heater and detector	20-300
[SCH 10]	Free-standing membrane	340	Optical, thermal transient grating	Room temperature
[HOC 08]	Nanowires	20–300	Electrical, suspended heater and detector	20-320
[BOU 08]	Nanowires	10 and 20	Electrical, suspended heater and detector	100-300
[HAO 06]	Thin films	50–80	Electrical, suspended heater and detector	Room temperature
[JUY 05]	Thin films	20–50	Electrical, on substrate heater and detector	Room temperature
[LIU 05]	Free-standing membranes	30	Electrical, Joule heating	300-450
[LIU 04a]	Free-standing membrane	20 and 100	Electrical, Joule heating	20-300
[LID 03]	Nanowires	22–115	Electrical, suspended heater and detector	20-320

Table 7.1. *Thermal conductivity measurements in Si nanostructures*

7.2.2. *The effect of phonon confinement*

The first thermal conductivity models for bulk systems [KLE 51, CAL 59, NAY 95, GLA 64] were based on the solution of PBTE under the single-mode relaxation time approximation. This approach provides the simplest picture of the phonon interactions considering that each phonon mode has a single-relaxation time independent of other modes, i.e. it assumes that all other phonons are at their equilibrium distribution [SRI 90]. The calculation of the thermal conductivity in semiconductor material implies the knowledge of three major frequency-dependent parameters, i.e. *specific heat capacity*, C_V, *group velocity*, v_g, and *mean free path*, Λ. The expression for thermal conductivity from the kinetic theory of gases is given by:

$$\kappa = \frac{1}{3} C_V v_g \Lambda \qquad [7.10]$$

Taking into consideration the contribution of each mode q with transverse (T) or longitudinal (L) polarization s, equation [7.10] becomes

$$\kappa = \frac{\hbar^2}{3VK_B T^2} \sum_{qs} v_{qs}^2 \omega_{qs}^2 \tau_{qs} n_{qs} (n_{qs} + 1) \qquad [7.11]$$

where $\hbar$ is the reduced Planck's constant, V is the total volume, T is the temperature, K_B is the Boltzmann constant, ω_{qs} is the phonon frequency, v_{qs} is the group velocity, n_{qs} is the Bose–Einstein equilibrium phonon distribution function and $\tau_{qs} = \Lambda_{qs}/v_{qs}$ is the total relaxation time of each mode. From equation [7.11], it is clear that to model the lattice thermal conductivity we need the dispersion relation, the total relaxation time of each mode and a numerical scheme for performing the integration within the Brillouin zone. The phonon dispersion relation can be calculated through several methods. However, the calculation of the intrinsic relaxation time and the summation over the Brillouin zone can be very time consuming and knowledge of anharmonic phonon-phonon scattering strengths is not yet sufficiently well-established [ALS 07].

7.2.2.1. *Modification of acoustic dispersion relation*

To calculate the dispersion relation, the elastic continuum model is often used. In this model, the discrete nature of the atomic lattice is ignored, and the material is treated as a continuum. This model can be derived from the theory of lattice vibrations by considering that the lattice deformations vary slowly on a scale determined by the range of the inter-atomic forces [KIT 04]. It is usually valid provided that the wavelength of elastic waves (λ) is significantly larger than the atomic lattice constant, a, i.e. $\lambda/a \geq 20$. This corresponds to wavelengths longer than approximately 10 nm, or frequencies less than approximately 100 GHz [MAX 54].

Using this model, Lamb [LAM 17] calculated the acoustic dispersion relation in free-standing membranes. The waves sustained by this membrane are the solution of the elasticity equation of the material with stress free as a boundary condition in $z = \pm a/2$, where a represents the thickness of the membrane, with infinite extent in x and y directions. For free-standing membranes the normal components of the stress tensor vanish on the surface. The acoustic equation of motion is given by

$$\rho \frac{\partial^2 U_i}{\partial t^2} = \frac{1}{2} \frac{\partial}{\partial x_j} \left[C_{ijkl} \left(\frac{\partial U_k}{\partial x_l} + \frac{\partial U_l}{\partial x_k} \right) \right] \quad [7.12]$$

where U_i is the displacement vector, C_{ijkl} is the fourth order elastic tensor, which has 81 components, but only 36 of these components are independent, due to symmetry considerations [NAY 95, AUL 73, SAD 04, ROS 04]. In isotropic materials, waves can travel equally well in all directions, and the elastic constant tensor can be further simplified to have two independent components.

In the isotropic case, the stress-strain relation C_{ijkl} tensor must be the same under rotation operations. This allows us to express the stress (T) and strain (E) relationship using only two independent components:

$$T_{ij} = \lambda E_{kk} \delta_{ij} + 2\mu E_{ij} \quad [7.13]$$

where λ is called Lamé's constant and μ is referred to as the shear modulus. Then the equation of motion is given by:

$$\frac{\partial^2 U}{\partial t^2} = v_T^2 \nabla^2 U + (v_L^2 - v_T^2) \nabla \cdot (\nabla U) \quad [7.14]$$

where $v_L = \sqrt{(\lambda + 2\mu)/\rho}$ and $v_T = \sqrt{\mu/\rho}$ are the longitudinal and transversal velocities, respectively, of acoustic waves in a given infinite medium.

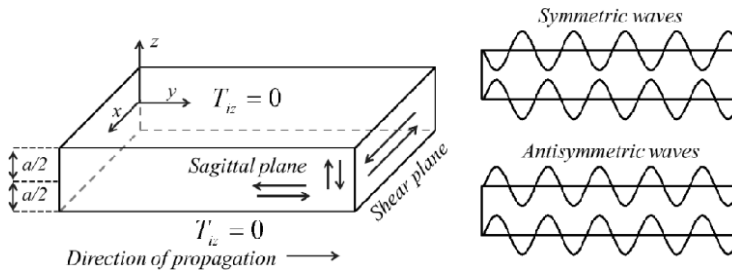

Figure 7.4. *a) Schematic of a membrane. b) Symmetric and antisymmetric waves*

The introduction of boundary conditions to infinite media changes the nature of the acoustic propagation. This generates two types of solutions: solutions with displacements confined to the sagittal (x, z) plane are called Lamb waves, while solutions with displacements perpendicular to the sagittal plane are called shear waves (SW) (see Figure 7.4). The Lamb waves can be further divided into two categories of modes: those with out-of-plane symmetric and antisymmetric displacements with respect to middle plane of the plate are known as dilatational waves (DW), and flexural waves (FW), respectively. The dispersion relation for SW has the following analytical expression [BAN 95]:

$$\omega_n = v_T (q_{//}^2 + q_{z,n}^2)^{1/2} \qquad [7.15]$$

where $q_{z,n} = n\pi/a$ takes only a discrete set of values at each in-plane component of the wave vector, $q_{//}$, since n is an integer. In contrast, the dispersion relation of sagittal waves cannot be written in a simple analytical form. Instead, it must be found solving the dynamical matrix, which yields the expression:

$$\frac{4q_{//}^2 q_{l,n} q_{t,n}}{(q_{t,n}^2 - q_{//}^2)^2} = -\left(\frac{\tan(q_{t,n} a/2)}{\tan(q_{l,n} a/2)} \right)^{\pm 1} \qquad [7.16]$$

where the exponents $+1$ and -1 correspond to symmetric and antisymmetric modes, respectively. The parameters q_l and q_t represent the longitudinal and transverse perpendicular component of the wave vector. The dispersion relation is then found through the relationship between two perpendicular wave vectors

$$\omega_n^2 = v_L^2 \left(q_{//}^2 + q_{l,n}^2 \right) = v_T^2 \left(q_{//}^2 + q_{t,n}^2 \right) \qquad [7.17]$$

By introducing equation [7.17] into equation [7.16], a nonlinear equation is obtained, where for each value of $q_{//}$ there are many values for $q_{t,n}$ and $q_{l,n}$. Figure 7.5 shows the dispersion relation (*a*) and group velocity (*b*) of a Si membrane. An interesting characteristic of the dispersion relation can be observed for small values of $q_{//}$. In this regime, the fundamental modes of the dilatational and flexural waves have a pseudo-analytic behavior making it possible to approximate the dispersion relation by linear and quadratic dependences, respectively [KÜH 07]. Thus, the acoustics vibrations are essentially localized at the surface and their amplitudes decrease exponentially from the surface to the interior of the membrane [BAN 95]. This dependence will be found important when determining the thermal properties in the low-temperature regime, where these modes became the most populated states.

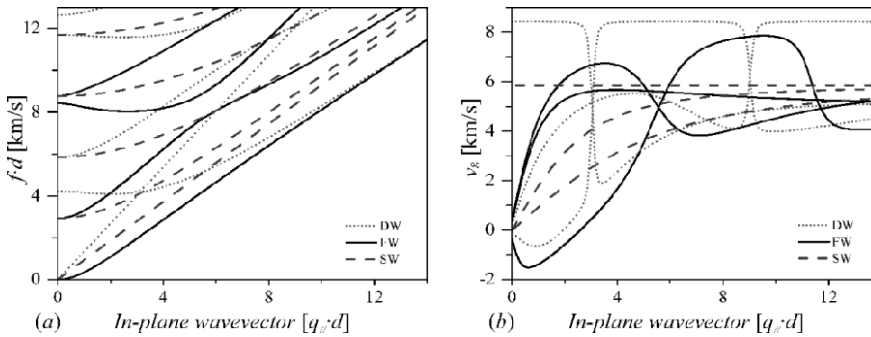

Figure 7.5. *a) Dimensionless acoustic dispersion relation, d·f, and b) group velocity, v_g, of the first three order of a Si membrane for dilatational (dotted lines, DW), flexural (solid lines, FW) and shear (dashed lines, SW) waves as a function of the dimensionless in-plane wavevector, $d \cdot q_{//}$*

7.2.2.2. *Modification of the specific heat capacity*

As seen above, the dispersion relation of membranes is not Debye-like and the acoustic dispersion relation is quantized. Therefore, it is not valid to integrate over all q space and, instead, the summation on the perpendicular direction is kept [PRA 98, HUA 08, CHA 12].

Figure 7.6 shows the calculated temperature dependence of the specific heat in Si membranes with thicknesses ranging from 1 to 120 nm. For comparison, the specific heat of the bulk Si is also plotted. As the membrane thickness increases, the bulk behavior is approached.

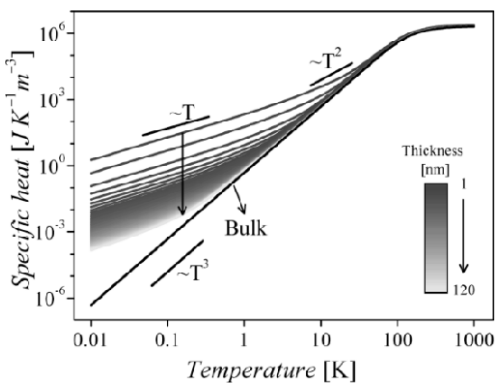

Figure 7.6. *Specific heat of Si as a function of temperature for the bulk (black line) and for membranes of thickness from 1 to 120 nm (following the heat color bar in the inset). For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

In the low-temperature regime, a departure from the cubic temperature dependence ($\propto T^3$) is evident, and as the membrane thickness decreases, a linear dependence is approached ($\propto T$). This behavior reflects the predominance of the fundamental flexural mode in the low-temperature regime owing to its quadratic dispersion. From Figure 7.6, it is possible to appreciate that size effects in the specific heat capacity are most significant at cryogenic temperatures and/or in ultra-thin membranes. Bulk values are quickly reached at higher temperatures.

7.2.2.3. *Phonon lifetimes*

The phonon lifetime is defined as the time taken for a phonon and/or a phonon wave packet to be scattered, attenuated or absorbed. In a solid crystal, a variety of scattering mechanisms exist, including impurities, isotopes, defects, dislocations, boundaries as well as collision with other carriers such as electrons, magnons, photons and phonons. Depending of the nature of the scattering mechanism, these can be divided into two types of interactions: inelastic scattering and elastic scattering.

Typically, the scattering due to impurities, isotopes, defects, dislocations or boundaries are modeled as elastic scattering, because they only produce a change in the direction of the phonon path. The scattering resulting as a consequence of collisions with other particles is modeled as inelastic scattering. These scatterings are treated mathematically as a consequence of anharmonic terms in the interatomic potential. The main scattering mechanism in the nanoscale is the surface roughness scattering. The effect of boundary scattering due to surface roughness may be introduced through a boundary condition on the steady-state BTE [ZIM 60].

7.2.2.4. *Decrease of thermal conductivity*

As shown above, the finite size of the membranes produces a discretization of the acoustic dispersion relation, with certain energy separation between the phonon modes, $\Delta E = \hbar\Delta\omega$. At the Brillouin zone center, this separation is approximately $\Delta E = \hbar\pi v_i/d$, where v_i can be longitudinal or transverse sound velocity. In the high-temperature regime and/or in thicker membranes, the energy between the modes is always much smaller than the thermal lattice energy, $E_{TH} = K_B T$; hence, many modes are occupied. In this case, the dispersion relation and the phonon density of states may be approached by the bulk-like behavior. Figures 7.7(a) and (b) show the lattice thermal energy and separation energy as a function of the temperature and thickness, respectively. For $T > 15$ K and $d > 15$ nm it is clear that the lattice thermal energy is much larger than the energy between the modes. In this regime, the bulk-dispersion relation is a good approximation. However, the bulk dispersion relation is not a good approximation when the energy separation exceeds the thermal energy, that is, $Td < \hbar\pi v_i/K_B$. In this regime, it is expected that the modification of the dispersion relation plays a role in the thermal properties [JOH 94].

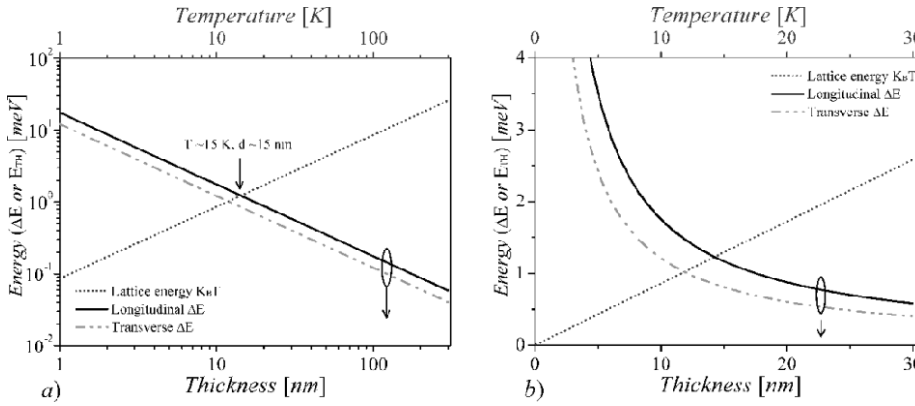

Figure 7.7. *a) Lattice thermal energy (dotted line) and separation energy (solid and dashed lines) as a function of the temperature and thickness, respectively. b) Magnified image of the low temperature/thickness regime*

Although there is not a formal procedure to decide when it is valid and/or useful to introduce the modifications of the dispersion relation, it is clear from the specific heat capacity that this modification is crucial at low temperatures and/or for smaller dimensions (thickness in the case of membranes).

Taking these facts into consideration, the reduction of thermal conductivity in Si thin films at room temperature can be attributed mainly to the shortening of the phonon mean free path due to the diffuse scattering of phonons at the boundaries [HYL 96, ASH 97, LIU 04a, TAN 11]. However, for small dimensions, compared to the phonon wave function, or in the low-temperature regime, the modification of the dispersion relation should be taken into account, including its effects on both group velocity and heat capacity [HUA 08, ZOU 01, KÜH 07].

The modeling of the thermal conductivity reduction is typically approached adding the phonon-boundary scattering term, τ_B, to the total relaxation time. It is estimated from the system thicknesses and/or diameter, the phonon group velocity and a correction factor parameter which will depend on the geometry of the system, F, $\tau_B = Fd/v_g(q)$. Sometimes, a specularity factor P, which represents the surface polish quality of the film/wire, is added [ZIM 60, CAS 38]. However, the boundary scattering is a surface phenomenon and the addition of an extra term in the total relaxation time is not particularly rigorous. Instead, it is necessary to include the boundary effect in the phonon mean free path. Following this concept, Fuchs [FUC 38] provided the first exact solution of the size effect in the electrical conductivity for thin films. Later, Chambers extended the models for nanowires

[CHA 50]. Sondheimer simplified the model for thin film and nanowires [SON 52]. The same concept was extended and adapted to calculate the reduced thermal conductivity of thin films [ASH 97, LIU 04a, ASH 98] and nanowires [WAL 99, STE 00].

The thermal conductivity simulation of free-standing membranes is carried out first by deriving the lattice thermal conductivity in a bulk system using the modified Callaway model under the single-mode relaxation time approximation [CAL 59, HOL 63]. Then, once the thermal conductivity for the bulk is determined, the effect of finite size is introduced through the Fuchs–Sondheimer boundary corrections [FUC 38, SON 52]:

$$\kappa_{bulk} = \frac{\hbar^2}{3k_B T^2} \sum_s \int v_{qs}^2 \omega_{qs}^2 \tau_{qs} n_{qs} (n_{qs} + 1) D_{qs} dq \qquad [7.18]$$

$$\frac{\kappa_{film}}{\kappa_{bulk}} = 1 - \frac{3}{2} \frac{(1 - P_q)}{\delta_s} \int_1^\infty (x^{-3} - x^{-5}) \frac{1 - e^{-x\delta_s}}{1 - p_q e^{-x\delta_s}} dx \qquad [7.19]$$

where D_{qs} is the phonon density of states, $P_q = \exp(4\pi\eta^2 q^2)$ is the fraction of phonons that are specularly reflected at the boundaries, η is the root mean square deviation of the surface from a reference plan [ZIM 60] (roughness), $\delta_s = d/\Lambda_s$ is the inverse of the Knudsen number and Λ_s is the bulk mean free path.

The bulk dispersion relation can be approximated using different approaches such as a sine function approximation, lattice dynamics and *ab initio* simulations, Debye-like, Holland approximation, Brillouin zone boundary condition and fourth-order polynomial fit, among others. [SRI 90, HOL 63, DEB 12, CHU 04, HOP 09]. If it is assumed that the first Brillouin zone is isotropic, then the dispersion relation is identical for any wave vector direction and it is possible to represent the Si bulk dispersion relation just taking the (100) direction.

The total relaxation time for each *s* polarization is limited by various scattering mechanisms such as boundary $\tau_{B,s}$, mass defect $\tau_{I,s}$ and Umklapp phonon-phonon interactions $\tau_{U,s}$. This can be obtained using Matthiessen's rule as [SRI 90]:

$$\tau_{q,s}^{-1} = \tau_{B,s}^{-1} + \tau_{I,s}^{-1} + \tau_{U,s}^{-1} \qquad [7.20]$$

The full calculation of the phonon lifetime could be very time consuming, and often some approximation can be used [CAS 38, KLE 55, SLA 64].

7.2.3. *Fabrication of ultrathin free-standing silicon membranes*

A convenient way to fabricate thin free-standing silicon membranes to investigate the thermal properties is to start with silicon-on-insulator (SOI) wafers. The fabrication includes thinning of the SOI film by thermal oxidation, oxide removal and releasing the membrane by deep etching through the handle wafer and the buried oxide layer (BOX). The windows to be opened on the backside are defined by photolithography and, consequently, double-side polished (DSP) SOI wafers are used. The thickness of the SOI film and BOX layer are typically a few hundreds of nm. The SOI film is thinned to the desired thickness by thermal oxidation, which provides very accurate control of the film thickness and atomic layer sharp interfaces between silicon and silicon dioxide. The grown oxide can be selectively removed in hydrofluoric acid (HF) or in buffered HF (BHF). Windows are patterned on the back-side of the wafer by optical lithography. The deep etching through the handle wafer can be done by wet etching in a tetramethylammonium hydroxide (TMAH) bath or by reactive ion etching (RIE) or by combining both. In RIE, SF_6-based chemistry provides good selectivity between silicon and oxide, and for TMAH, the selectivity is in practice infinite, leading in both cases to stopping of the deep etching at the handle wafer–BOX interface. The final removal of the BOX is carried out in BHF. During the fabrication process, the thickness of the layers is controlled by an optical reflectometer with accuracy better than 1 nm and confirmed by cross-sectional scanning electron microscopy (SEM).

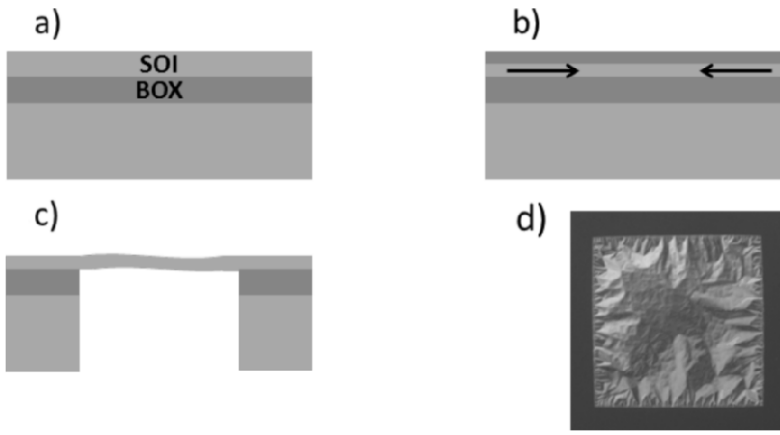

Figure 7.8. *a) SOI wafers used in the fabrication of the free-standing membranes have typically a few hundred nm thick SOI film and BOX layer. b) The SOI film is thinned by thermal oxidation. The thermal process creates compressive stress in the film, as shown by the arrows. c) After release, the membrane is relaxed and has a tendency to buckle. d) Optical micrograph of a released 1.4x1.4 mm^2 membrane with thickness of 9 nm. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Applying this process, a free-standing membrane with size in the range of several square millimeters and with thickness below 10 nm can be fabricated with relative ease. The process steps are schematically shown in Figure 7.8. However, the thermal processes used to thin the SOI film tend to create compressive stress in the film [IID 00], leading to buckling of the membranes after the release. The buckling can be potentially detrimental for experimental work, especially for optical measurements, because the angle of incidence of the laser beam may not be well defined, and can also prevent the use of membranes in device applications. In addition, the strain and, consequently, the elastomechanical properties of the membrane, cannot be tuned in a controlled manner because of the relaxation of the built-in stress. There are ways to overcome this problem and control the stress such as growing Si epitaxially on a SiGe buffer [ROB 06] or depositing thick SiN layers on the top and bottom of the Si layer [WAN 07]. However, these approaches do not allow fabrication of bare free-standing Si membranes with tunable strain.

One approach to control the strain in the membranes and to avoid buckling is to add a strain-compensating frame on the silicon membrane perimeter [SHC 13]. The strain can be tuned by varying the properties of the frame and the properties of the membrane can be engineered in controlled manner. The process is more complex than the above process and is described schematically in Figure 7.9. The fabrication process consists of the following steps: (1) oxidation and bonding the SOI wafer to a new Si handle wafer. The 20 nm thick thermal oxide grown on the SOI film acts as a new buried oxide layer in order to minimize the extra stress and buckling arising from the original thicker BOX layer. The original handle wafer is removed by mechanical back-grinding and wet etching in a hot TMAH solution, followed by the removal of the original BOX layer with BHF. The SOI layer is then thinned down by thermal oxidation and oxide stripping. (2) Deposition of a 20 nm thick silicon dioxide layer and a 280 nm thick low-stress silicon nitride layer by low-pressure chemical vapor deposition (LPCVD). Windows that define the size of the bare silicon membrane are opened into the nitride film. The nitride film has tensile strain and provides the strain compensation to avoid buckling. (3) Deposition of a 500 nm thick silicon dioxide layer by LPCVD and a 50 nm thick aluminum oxide layer by atomic layer deposition (ALD) for protection during the etching through the wafer which is carried out using a combination of deep RIE and wet TMAH etching. Finally, (4) the final release of the silicon membrane in BHF.

An example of the effect of strain compensation is shown in Figure 7.10. The relaxed membrane in Figure 7.10(a) shows buckling, with an amplitude of several micrometers, whereas the strain-compensated membrane of the same size in Figure 7.10(b) is completely flat.

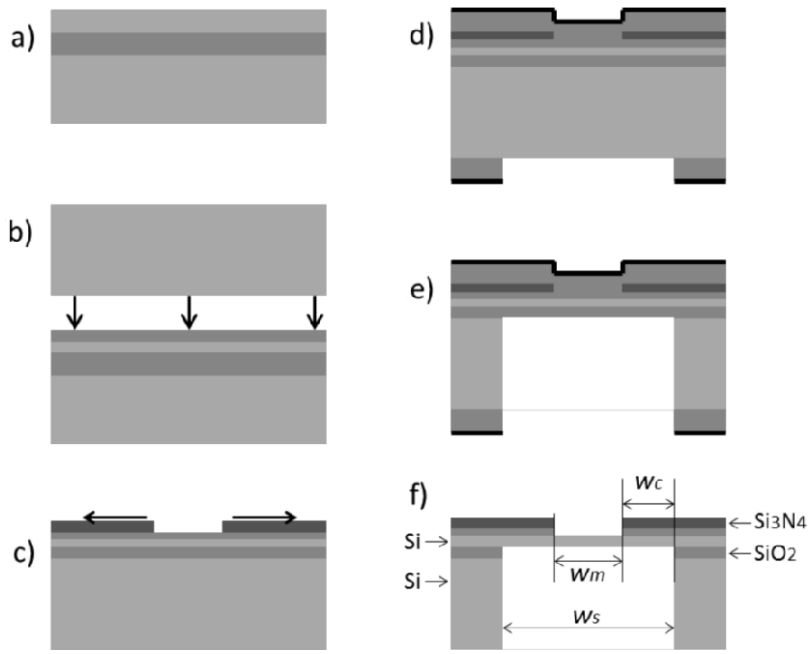

Figure 7.9. *Fabrication process for strain-compensated silicon membranes. The details are given in the text. The strain compensation effect due to the nitride membrane under tensile stress is shown in (c). The dimensions, i.e. the ratio w_c/w_m, define the amount of tensile strain in the free-standing bare silicon membrane*

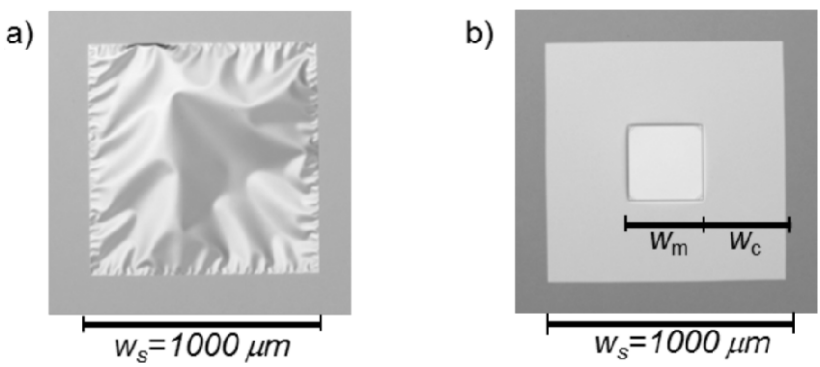

Figure 7.10. *a) Optical image of a 37 nm thick silicon membrane with area of 1 mm^2. The amplitude of the buckling is several μm. b) Optical image of a 37 nm thick silicon membrane with strain compensation. The area of the released membrane is 1 mm^2 and the area of bare silicon membrane 300×300 μm^2. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Strain affects the elastomechanical properties and band structure of the membrane. The LPCVD silicon nitride used in these experiments for strain compensation has a relatively low tensile stress of about 300 MPa. This stress and thickness of 280 nm of the nitride film create a tensile strain of 0.15% in a 6 nm thick membrane, resulting in tens of meV splitting in the conduction band and in the band gap of silicon [SHC 13]. By varying the growth conditions, the stress in the nitride film can be varied between 0 and 1000 MPa, and together with the control of the thickness of the film, the tensile strain in the silicon membrane can be substantially varied. The strain control provides an extra tuning parameter, in addition to the membrane thickness, for investigations of optical, electrical and thermal properties of low-dimensional systems.

7.2.4. *Advanced methods of characterizing phonon dispersion, lifetimes and thermal conductivity*

7.2.4.1. *Phonon dispersion*

To validate the impact of confinement effects on the thermal properties of nanostructures, the first step is the experimental determination of the phonon dispersion. It is crucial to measure and contrast with theory, the dependence of the phonon frequency on its propagation direction and magnitude. Several questions must be answered: is the elastic continuum model still valid at the nanoscale? Is quantum confinement important when the coherence of scattered phonons is masked by boundary or grain effects?

The optical experimental method to transfer energy and momentum between photons and phonons is known generically as inelastic light scattering (ILS) and it allows direct measurement of energy or frequency of phonon, vibrational and rotational states of molecules, as well as plasmons, excitons and magnons, and is a non-contact, non-destructive method, with no pre- or postprocessing required.

Historically, ILS from acoustic phonons has been known as Brillouin light scattering (BLS), while scattering from optical phonons and vibrational and rotational states of molecules, has been known as Raman scattering. From the point of view of quantum theory, Brillouin scattering is simply the first-order Raman scattering associated with a transition in the vibrational states of the acoustic vibrations [DEM 08].

In practice, the difference among ILS techniques is the apparatus needed to target the different frequency or energy ranges of the quasi-particles or vibrations targeted. The interaction of the quasi-particle with the photon causes a frequency downshift (Stokes) or a frequency upshift (anti-Stokes) depending on whether the energy is given or absorbed by the photon. The typical frequency range accessed by

BLS, extends from 500 MHz to several hundred GHz, which is suitable for measuring acoustic phonons.

In the quantum description of the interaction, the incident photon creates or annihilates a phonon, and the energy and momentum of the phonon is equal to the difference in energy and momentum between the incident and scattered photons. Two main inelastic light scattering processes from acoustic phonons are present in nanostructured materials: the photoelastic scattering mechanism and the *ripple* scattering mechanism:

– Photoelastic (or elasto-optic) scattering occurs due to time-dependent fluctuations in the polarizability of a material, caused by acoustic phonons.

– The ripple scattering mechanism differs from the photoelastic mechanism mainly in that the scattering strength does not depend directly on the strain, photoelastic constants or polarizability of the material. Instead, the strength of the scattered signal is proportional to the normal displacement of the acoustic wave, or ripple, since the change in phase is due to variations of the optical path length caused by the surface displacement. For this reason, the ripple scattering mechanism is stronger for surface acoustic waves, or waves which cause modulation at the surface, such as the flexural and dilatational waves in a membrane.

However, bulk waves will also cause surface displacement, and surface waves will also induce a strain, and therefore scatter light via the photoelastic effect; thus, in general, both effects must be taken into account. The relative importance of either effect is determined primarily by the scattering volume. Extensive discussions of both mechanisms can be found in [BEN 66, LOU 80].

To measure a dispersion relation, both frequency and wave vector magnitude and direction are required. The wave vector of the phonon involved in the scattering process is determined by the angle of scattering, which is defined through the scattering apparatus and the mechanism responsible of the ILS. The wave vector, q, involved in the scattering process depends on the scattering mechanism. In the general case of the photoelastic scattering, it is given by:

$$q = 2k\sin(\theta/2) \qquad [7.21]$$

where k and q are the wave vectors of the incident photon within the material and the generated/absorbed phonon, respectively, and θ is the angle between the incident and scattered light beams. In a backscattering configuration of θ=180 degrees, equation [7.21] becomes:

$$q = -2k \qquad [7.22]$$

where the magnitude of the wave vector is independent of the scattering angle and the direction of the wave vector within the sample is defined by Snell's law (see Figure 7.11).

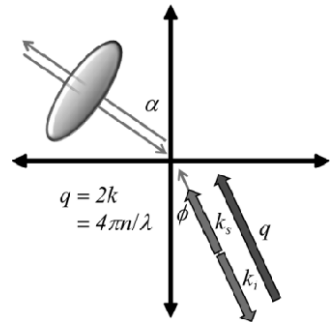

Figure 7.11. *Wave vector conservation in the photoelastic backscattering configuration. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

For the case of ripple scattering, the wave vector of the phonon involved is given by

$$q_x = k_{1i}^x - k_{1s}^x = 2k(\sin(\alpha_i) + \sin(\alpha_s)) \qquad [7.23]$$

where α_I and α_S are the incident and scattered angle, respectively, both defined with respect to the normal to the surface.

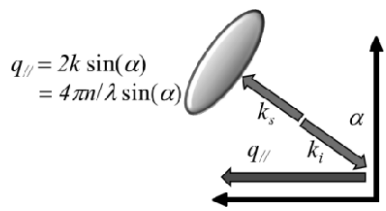

Figure 7.12. *Wave vector conservation in backscattering configuration via the ripple effect. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

For the backscattering configuration, the previous relation becomes:

$$q = 2k\sin(\alpha) = \frac{4\pi}{\lambda}\sin(\alpha) \qquad [7.24]$$

In this case, the magnitude of the wavevector changes as a function of the angle, while the direction remains constant, parallel to the surface in the scattering plane

(see Figure 7.12). The apparatus is shown in Figure 7.13 and is built in a backscattering geometry. A small prism or beam splitter is used to direct the light toward the sample, with an achromatic lens used to focus the light. As the scattering occurs at the focus of the lens, the backscattered light is collimated, and another lens placed after the prism is used to focus the light to the entrance pinhole of the spectrometer. A beam splitter is placed between the prism and the lens to form an image of the sample on a CMOS camera.

The incident radiation was provided by a diode-pumped solid state laser from Oxxius, with a free-space wavelength, λ, of 532 nm.

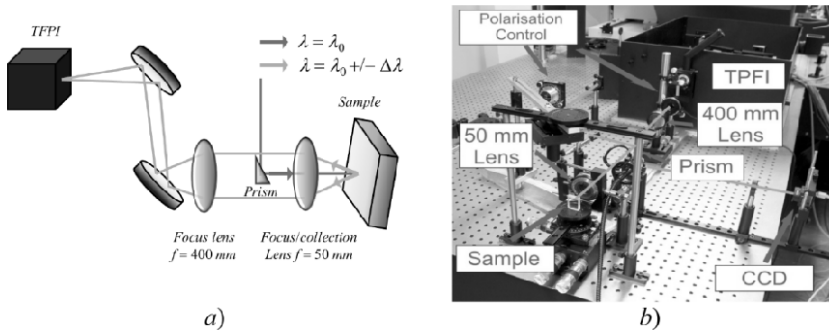

Figure 7.13. *a) Schematics of apparatus used for backscattering configuration. b) Photograph of apparatus used for backscattering configuration. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

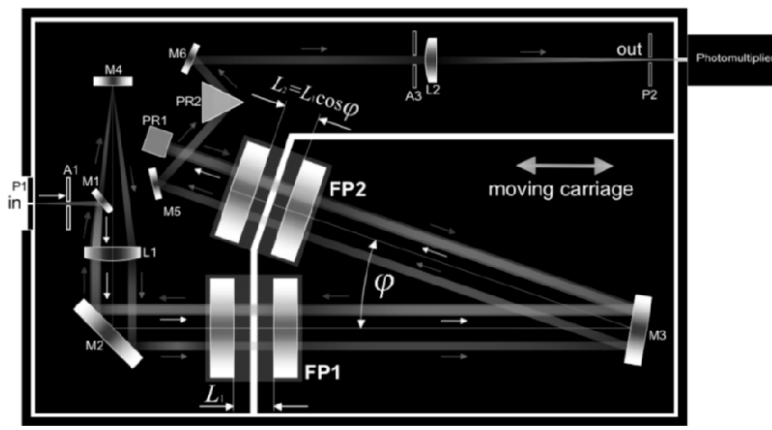

Figure 7.14. *Schematic of the Tandem Fabry-Perot interferometer, manufactured by JRS Instruments, Sandercock showing the light path [LIN 81]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The light inelastically scattered by optical and acoustic phonons undergoes an extremely small fractional change in frequency and a high-resolution spectrometer is required. We have used a Tandem Fabry-Perot interferometer (TPFI) for these purposes, which consists of two Fabry Perot Interferometers put in series (see Figure 7.14). In general, in Fabry-Perot interferometers the increase of the finesse is achieved by increasing the cavity length, but this reduces the free-spectral range. The tandem configuration overcomes this problem since the two cavities can be configured, using two slightly different cavity lengths, to be both resonant just at a certain wavelength and detuned for the neighboring supported modes. This greatly enhances the free spectral range, while maintain a high finesse.

Typical Brillouin spectra of Si membranes are shown in Figure 7.15. The spectra were taken using an Olympus 10X objective, with a numerical aperture of 0.5 and a spot size measured at full-width-half-max (FWHM) of 12.5 μm was used as the focus and collection lens for the thicker membrane [CUF 11].

The main difference with respect to the bulk counterpart is the multiple peaks observed in the membrane case. For the bulk system, just a single peak corresponding to the surface acoustic wave is seen. The first two peaks nearest to the central quasi-elastic peak are identified as the zero-order flexural and dilatational modes. In the 400 nm membrane, these are observed as independent peaks only at small angles, and quickly become indistinguishable. This is because the zero-order flexural and dilatational modes may be thought of as interacting surface acoustic waves on either surface of the membrane. The flexural mode corresponds to the case when these modes are in-phase, resulting in flexing of the membrane. The dilatational mode occurs when these waves are out-of-phase, thus resulting in a dilatational motion of the membrane. These modes can then be thought of as bonding and anti-bonding states of the surface acoustic modes, in analogy with bonding and anti-bonding states of molecular orbitals. The merging of these modes at large angles, or large values of $q_{//}$, is a consequence of the fact that at short wavelengths, the surface waves are confined to either surface and do not interact, thus behaving like bulk surface acoustic waves. This explains why the modes are distinguishable for a wider range of angles for the 200 nm membrane, as in the thinner membrane the modes interact at shorter wavelengths.

The full dispersion relations of the flexural and dilatational modes for these membranes in the (110) direction are shown in Figure 7.16. The theoretical curves were calculated by the partial wave method solving equation [7.12]**,** where the analytic equations for the flexural and dilatational membranes in an anisotropic membrane were solved using numerical root searching techniques [CUF 11].

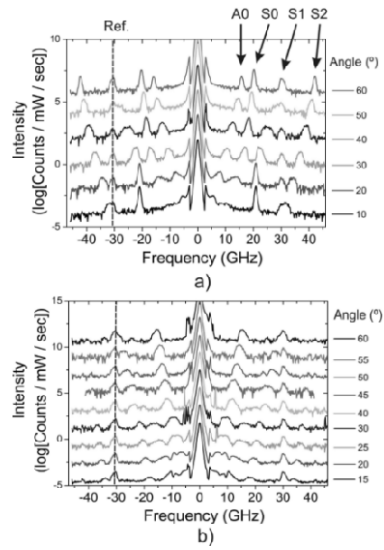

Figure 7.15. *Typical Brillouin spectra of free-standing Si membranes, with thickness values of a) 193 nm and b) 400 nm. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

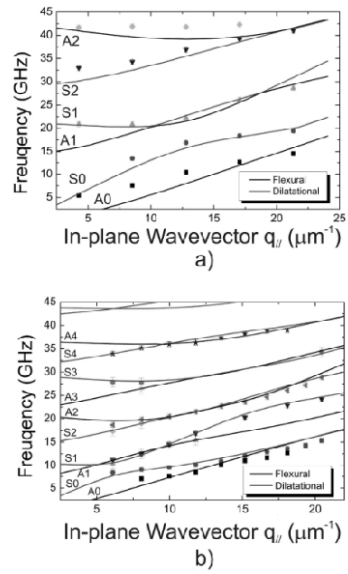

Figure 7.16. *Acoustic dispersion relation of free-standing Si membranes, with thickness values of a) 193 nm and b) 400 nm. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

7.2.4.2. *Phonon lifetime*

Understanding the lifetimes of heat-carrying phonons is essential for engineering thermal transport. The phonon lifetime refers to the time taken by a phonon or phonon wave packet to scatter or be attenuated. The reason for this attenuation may be either collision with impurities or defects within the sample or the boundaries of the sample, or due to the intrinsic anharmonicity of the lattice, which occurs even for perfect crystals. In conjunction with its group velocity, the phonon lifetimes define how far a phonon can carry its energy, which is known as the phonon mean free path. Despite the fundamental importance of these parameters, accurate measurements of phonon lifetimes are challenging, and their values are unknown in most materials. Even though silicon is the most important material for nanoscale devices, there are few direct measurements of phonon lifetimes in the gigahertz to terahertz range [DAL 09]. Moreover, many open questions remain about the relative contributions of intrinsic and extrinsic scattering processes at high frequencies in both bulk and nanoscale structures [UNT 10, DUQ 03, LIU 07]. In this section, we review some of the recently developed experimental methods designed to perform these elusive measurements.

One of the most fundamental approaches to measure phonon lifetimes is to first generate phonons with an impulse of some kind and then observe the rate at which they decay. As the dominant heat carrying phonons at room temperature have frequencies of the order of 1 THz and above, one of the challenges relates to exciting high-frequency phonons. One of the primary tools that enabled the study of these phonons was ultrafast laser spectroscopy, capable of generating very short pulses with very intense electric fields. These pulses, with durations of just a few picoseconds, and more recently down to sub-100 fs pulses, deliver very fast, powerful impulses, which generate high-frequency phonons. This development opened a field of study now known of picosecond acoustics or picosecond ultrasounds, and has been used to study many acoustic phenomena, including the mechanical properties of a wide range of materials, such as nanoscale thin films, multilayers, quantum wells, semiconductor heterostructures and nanocavities and even single biological cells.

7.2.4.2.1. Generation and detection of high-frequency phonons

The light-matter interactions that cause ultra-short laser pulses to excite high-frequency phonons are a rich and interesting field of study. The intense electric field of the short pulse interacts with the electron clouds of the material, which then generates strain through different mechanisms, depending on the material properties. The processes involved in semiconductors, such as silicon, are illustrated in Figure 7.17. When the pulse hits the sample, electrons are excited into the conduction band. These electrons decay rapidly while giving their energy to the lattice through phonon emission and come to thermal equilibrium with the lattice at

the bottom of the conduction band within ~1 ps. The subsequent dynamics then depend on carrier and thermal diffusion. The laser pulse causes strain via two separate mechanisms, namely thermal expansion, and the hydrostatic deformation potential. The thermal expansion is due to the anharmonicity of the lattice, whereas the deformation potential is due to the excitation of electrons into binding orbitals. In the case of bulk silicon, the stress caused by the deformation potential is about seven times greater than the thermal stress, and is compressive [WRI 95]. These stress terms then lead to the generation of acoustic phonons. Often, metal layers are used as transducers, especially for transparent films, which cannot absorb the radiation. Here, the dynamics are quite similar, except that electron–hole recombination is much faster.

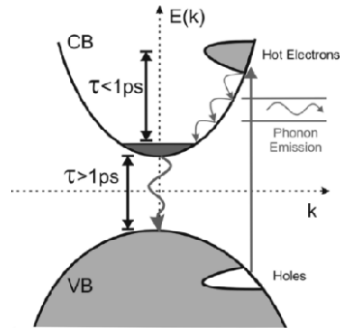

Figure 7.17. *Schematics of the response of a semiconductor to an ultra-short pulse. Electrons are excited from the valence band, VB, to the conduction band, CB, where they decay rapidly to the bottom of the conduction band through electron-electron collisions and phonon emission. The dynamics are then described by a slower decay involving electron-hole pair recombination, carrier diffusion and thermal diffusion. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

To detect these phonons, the strain dependence of the reflectivity for many materials is exploited, which occurs due to a change in the refractive index caused by the elasto-optic or photoelastic coefficients of the material. For many pico- and femtosecond experiments, one intense laser pulse will be used to excite phonons, while another weaker pulse or train of pulses is used to detect the corresponding change in reflectivity. These are collectively known as pump-probe measurements.

The first measurements involving the generation and detection of acoustic phonons by picosecond laser pulses were performed in the 1980s [THO 84, THO 86]. The technique was then applied to measure the attenuation of phonons in amorphous SiO_2, for frequencies up to 440 GHz [ZHU 91]. Recent experimental investigations have extended this work to measure phonons in superlattice cavities with frequencies of around 1 THz, where it was found that the lifetimes of high-frequency phonons could be limited by an average interface roughness of just

0.06 nm [ROZ 09]. For bulk samples, the phonon lifetimes are expected to be limited by the intrinsic anharmonicity, for which there are many models. Phonon wave packet experiments were performed in silicon with frequencies up to approximately 100 GHz. These results were analyzed with a simplified Akhieser relaxation damping model [AKH 39, DAL 09] of intrinsic scattering, assuming an average lifetime of high-frequency thermal phonons of 17 ps. Other intrinsic damping models include clamping losses [WIL 11], thermoelastic dissipation [LIF 00] and three-phonon interactions [ALS 07], which predict a different behavior depending on the frequency and temperature regimes. The generation and detection of coherent acoustic phonons at high frequencies is an ideal method to investigate these mechanisms and their relative importance compared to extrinsic scattering in nanostructures.

In particular, free-standing silicon membranes are model systems for such studies as they can be fabricated with precisely controlled dimensions and physical parameters, facilitating comparison with theoretical models. Additionally, as they are free-standing, the analysis is free from any effects of a substrate. Recently, measurements were performed on silicon membranes over a large range of thickness values from 7.7 ± 0.1 to 194 ± 1 (nm), allowing the investigation of the trend in phonon lifetime with frequencies up to ~500 GHz [POP 10]. A pump-probe technique known as asynchronous optical sampling (ASOPS) was used to generate and detect coherent acoustic phonons [BAR 07], with increased sensitivity and stability compared to traditional pump-and-probe methods.

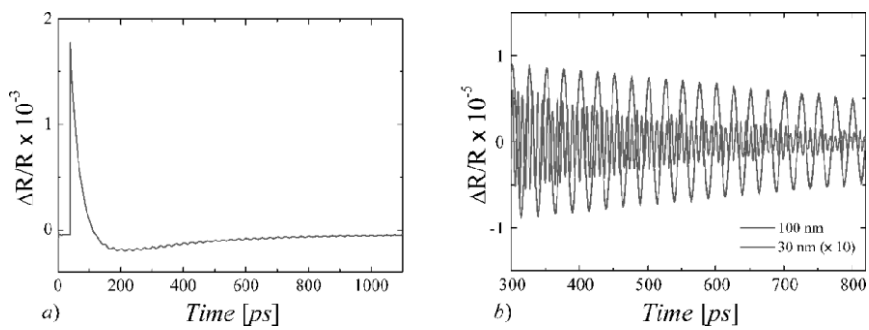

Figure 7.18. *a) Fractional change in reflectivity as a function of time in the 100 nm silicon membrane. The sharp initial change in reflectivity is due to the electronic response of the membrane. The subsequent weaker oscillations are due to the excited acoustic modes. b) Close-up of the acoustic modes after subtraction of the electronic response for membranes with 100 and 30 nm thickness shown by a black and a blue line, respectively. The sinusoidal decay of the reflectivity due to the first-order dilatational mode is clearly observed as a function of time, with a faster decay observed for the thinner membrane. The time trace of the 30 nm membrane has been magnified by a factor of 10 for clarity. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Figure 7.18(a) shows a typical time trace of the change in reflectivity induced by the laser pulse in a 100 nm silicon membrane. The initial spike at short times is related to the electronic response, while the subsequent oscillations result from the excited phonon modes. Figure 7.18(b) shows a close up of these modes, and a comparison for membranes of two different thickness values. It can be seen that the 30 nm membrane decays faster compared to the 100 nm membrane.

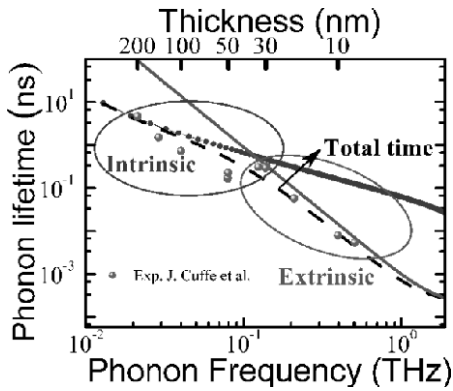

Figure 7.19. *Experimental and theoretical phonon lifetime of the first-order dilatational mode in free-standing silicon membranes as a function of frequency. Experimental data of free-standing silicon membranes with thickness values ranging from approximately 222 to 8 nm (dots). Solid line: extrinsic boundary scattering processes. Dotted thick line intrinsic three-phonon normal scattering processes. The total contribution, calculated using Matthiessen's rule, is shown by the solid-dashed line.*

The results from all the membranes are shown in Figure 7.19. It can be seen that the phonon lifetime decreases dramatically with membrane thickness, corresponding to higher phonon frequencies. These findings are compared with theories considering both intrinsic phonon scattering and extrinsic surface roughness scattering. The intrinsic phonon lifetimes were modeled by applying Fermi's golden rule to calculate three-phonon interaction probabilities [SRI 90] based upon a Debye model approximation, thus removing almost all free parameters from the calculation. The surface scattering was calculated following the approach of Ziman, including a wavelength-dependent specularity parameter [ZIM 60].

It was found that the combination of these models described the trend in phonon lifetimes over several orders of magnitude, changing from being dominated by the intrinsic effect for thicker membrane to being limited by surface roughness for thinner membranes.

While recent work reports measured phonon lifetimes covering almost two orders of magnitude in frequency in silicon nanostructures, further work is needed to generate and detect higher frequency phonons, which are most important for thermal transport at room temperature. Nevertheless, these recent experiments give valuable information enabling comparisons with models of phonon lifetimes, which can then be used to predict thermal transport in nanostructures.

7.2.4.3. *Thermal conductivity*

7.2.4.3.1. Raman thermometry

In recent years, novel contactless characterization techniques for thermal conductivity (or thermal diffusivity) determination have been progressively developed. Their main advantage as compared to electrical techniques is the lack of contacts and the preprocessing stage of the samples, thus making the fabrication process faster, easier and cost-efficient. Besides the steady-state method for thermal conductivity determination where good thermal contacts are mandatory [ZHA 95], the well-established 3ω technique for bulk and thin film samples [CAH 94] requires an initial lithography process followed by a metallic strip deposition and finally the bonding of electrical contacts. The latter represents a good example of the drawbacks of contact techniques since, although its experimental accuracy is usually good ≈5%, the fabrication process is sometimes difficult, e.g. due to largescale roughness of the samples which can result in breakage of the metallic strip. Scanning the thermal microscopy is also an interesting alternative, although the fabrication and calibration of the thermal tips can be quite challenging. Consequently, different groups have developed a variety of contactless advanced techniques such as, e.g. time-domain thermoreflectance (TDTR) [BUR 02a, BUR 02b], frequency-domain thermoreflectance (FDTR) [SCH 09], thermal transient grating (TTG) [GRA 95], the photoacoustic method [SWI 83], and Raman thermometry [LIU 11].

Raman thermometry is a contactless novel technique to determine thermal conductivity based on the local temperature measurement through the thermally-induced red-shift of optical phonons in a material. We recall that optical phonons generally experience a red-shift upon a temperature increase arising mainly from the thermal expansion of the lattice through the anharmonic interaction. In order to apply this technique, a main requirement is that the material under investigation has a detectable Raman signal from any of its optical modes. For example, amorphous materials and metals exhibit poor Raman signals. On the contrary, most inorganic and organic semiconductors, electrical insulators, and polymers exhibit many optical Raman modes depending upon their symmetry. In any case, the temperature dependence of just one optical mode will serve as local temperature probe.

A laser is focused onto the surface of a sample using a microscope objective with high numerical aperture (NA≈0.9) resulting in a spot about 1 μm in diameter. The

temperature of the focused spot can easily be obtained by fitting the spectral position of the observed Raman mode, given a previous calibration of its spectral position with temperature. Thus, increasing the incident laser power leads to local heating and to a red-shift of the observed Raman mode. The temperature increase in the spot region for a given incident laser power will depend on the thermal properties of the investigated material. The thermal conductivity of the sample can be extracted if a suitable heat diffusion model is adopted. For example, for bulk materials, the three-dimensional (3D) heat equation has to be solved considering a Gaussian power source [PER 99], i.e. the incident laser; whereas for thin films on a substrate the problem becomes analytically more complex due to the interface resistances and heat reflections [HUA 09a, HUA 09b]. For thin membranes, the solution is much simpler since the heat equation is reduced to two dimensions (2D) as we show in the following.

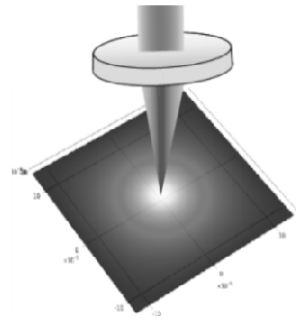

Figure 7.20. *Scheme of the Raman thermometry method. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Figure 7.20 shows a simple example of the application of Raman thermometry in ultrathin suspended Si membranes. The schematic diagram is a finite element simulation of the temperature distribution in a Si membrane upon heating with a Gaussian power source, here the incident laser, in its central position (yellow (pale gray = maximum power, black = minimum power). We noted that the thickness of the membranes ($d < 1$ μm) is small compared to the lateral dimensions ($L \approx 100$ μm), which justifies the use of a 2D heat conduction model. The left-hand side vertical axis of Figure 7.21(a) shows the temperature of the spot. The right-hand side vertical axis accounts for the relative Raman shift relative from its position at room temperature. The temperature rise of the laser spot increases as the thickness of the membranes decreases. This arises from a pure geometrical effect given by the increase of the power density distributed along the thickness of each membrane, as a well as from a reduction in their thermal conductivity. The thermal conductivity of each membrane is obtained by solving the stationary 2D heat equation based on the temperature rise the laser spot position as follows:

$$-\nabla^2 T = \frac{g(x,y)}{\kappa} = \frac{P_{Abs}}{2\pi d\sigma^2\kappa}\exp\left(\frac{r^2}{2\sigma^2}\right) \qquad [7.25]$$
$$T = 294K\,@\;\; Si\ frame$$

where $g(x,y)$ is the power generation function that we assume to be a Gaussian, based on the laser profile, and P_{Abs} is the absorbed laser power.

Figure 7.21(b) shows the results from the finite element simulations used to extract the thermal conductivity. The full symbols are the results obtained using the present technique in a series of Si suspended membranes, and the full symbols account for experimental data obtained using the thermal transient grating (TTG) technique in the same set of samples. We noted that the agreement between both techniques is quite satisfactory. The thermal conductivity of the membranes decreases with their thickness, which arises mostly from phonon boundary scattering at the membrane surfaces.

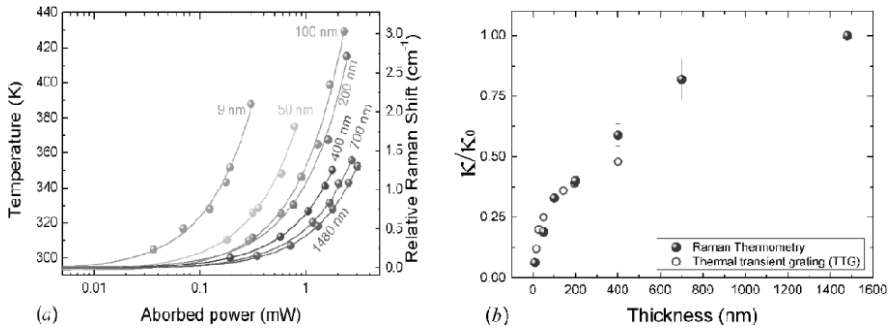

Figure 7.21. *a) Temperature at the laser spot as a function of the absorbed power for different membrane thickness. b) Thermal conductivity of each membrane calculated solving numerically the 2D stationary heat equation. The open symbols are results obtained using thermal transient grating (TTG) on the same membranes plotted here for comparison. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Thus, Raman thermometry offers particular advantages for a fast and contactless determination of the thermal conductivity.

7.2.4.3.2. Transient thermal grating (TTG) method

The TTG method is an optical technique for measuring thermal diffusivity [GRA 95]. While the thermal conductivity is a measure of how well a material conducts heat, the diffusivity is related to how quickly a material conducts heat. The thermal conductivity of a sample is the product of its diffusivity and volumetric heat capacity.

In this method, two short laser pulses are crossed on the sample to form an interference pattern. The absorption of the light causes a spatially periodic thermal grating, which in turn induces an optical phase and amplitude grating through the temperature dependence of the real and imaginary parts of the refractive index, respectively. A probe beam is diffracted from this transient grating and the thermal diffusivity can be determined from the rate of signal decay (see Figure 7.23(b)). As heat diffuses from the peak to the valley of the grating, the diffraction efficiency of the optical grating drops and the signal intensity decays exponentially with time. The thermal decay can then be characterized by a decay time τ, which is related to the thermal diffusivity α as

$$\alpha = \frac{1}{q^2 \tau} \qquad [7.26]$$

where $q = 2\pi/L$ is the grating wave vector corresponding to a grating period L. The grating period is controlled by the angle of incidence θ, and is given by

$$L = \frac{\lambda}{2} \sin(\theta/2) \qquad [7.27]$$

The TTG method has a number of advantages. As no adsorbed metal layer is required, neither electrical nor thermal contact resistances are introduced to the measurement or analysis. Although the diffusivity is measured, as opposed to measuring the thermal conductivity directly, this has the advantage that the absolute power does not need to be measured, which can be challenging for many nanoscale objects. The thermal length scale can also be easily varied by changing the grating period, which is useful to ensure diffusive transport, and can be used to observe ballistic phonon transport over micrometer distances in silicon at room temperature [JOH 13]. Finally, as the thermal grating is defined in the plane of the membrane, in-plane thermal transport is assured. A typical apparatus for performing a TTG measurement is shown in Figure 7.22.

As an example of the capabilities of this technique, this method was recently used to measure thermal transport in nanoscale silicon membranes, with thickness values ranging over two orders of magnitude from 15 nm to 1.5 μm. A typical time trace from the decay of the thermal grating in the silicon membranes is shown in Figure 7.23(b). The initial negative spike and fast decay is the contribution of electronic carriers while the slower exponential decay is related to the decay of the thermal grating. The electronic grating decays rapidly through ambipolar diffusion and Auger recombination on a time scale approximately one order of magnitude faster than the thermal decay.

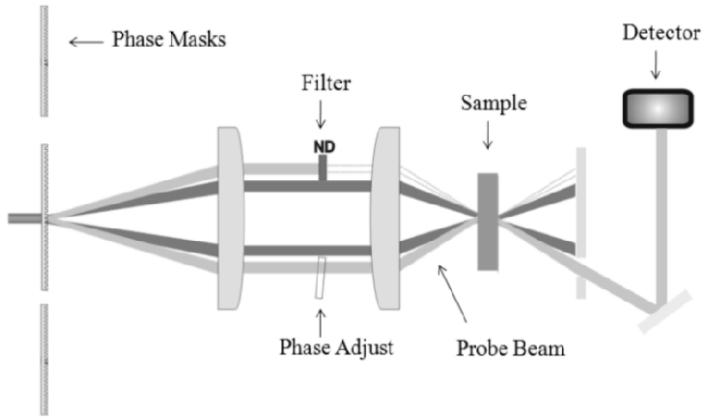

Figure 7.22. *Schematic of the four-beam transient thermal grating apparatus adapted from [JOH 13].The angle between the pump beams is controlled by splitting the beams with a diffraction grating (phase mask) with a well-defined pitch. The pump beams are later blocked, while the signal from the probe beam diffracted from the thermal diffraction grating is recorded. This signal is mixed with an attenuated reference beam for heterodyne detection*

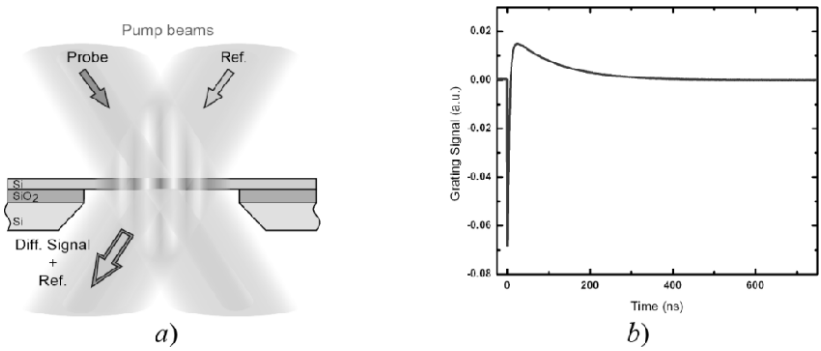

Figure 7.23. *a) Schematic of the silicon membrane sample and experiment. Two laser pulses are crossed on the suspended membrane to form a thermal grating. A third probe beam is diffracted from the thermal grating, which is mixed with a reference beam for heterodyne detection. b) Typical diffraction intensity as a function of time for a 400 nm silicon membrane. After the initial electronic contribution at short times, the rate of decay of the diffraction signal is related to the thermal diffusivity in the sample. Adapted from Johnson et al. [JOH 13]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The diffusivity as a function of grating spacing is shown in Figure 7.24. Data was collected for grating periods ranging from 7.5 to 25 μm. The diffusivity is seen to be constant as a function of grating spacing, indicating diffusive thermal

transport. From this data, the thermal conductivity can be calculated as $\kappa = \alpha C_V$ where $C_V = 1.64 \times 10^6$ J m^{-3} K^{-1} is the volumetric heat capacity of bulk silicon. The volumetric heat capacity of the membranes is not expected to change significantly from that of bulk silicon for membranes with thickness values down to 15 nm at room temperature, due to the relatively small change in the phonon density of states [HUA 08, CHA 12b].

The measured thermal conductivity values were compared with the Fuchs–Sondheimer model [SON 52, FUC 38], using phonon lifetimes calculated from the first principles [ESF 11], showing good agreement.

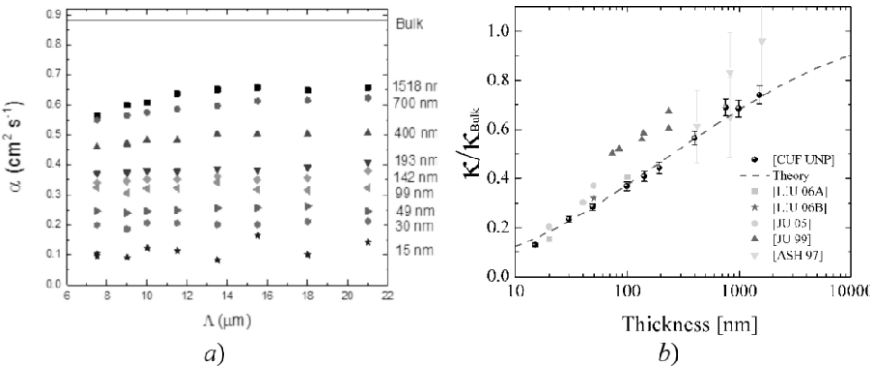

Figure 7.24. *a) Thermal diffusivities as functions of grating spacing in silicon membranes with thickness values ranging from ~ 15 nm to 1.5 μm. b) Thermal conductivity as a function of membrane thickness. The experimental points from this work [CUF UNP] (black dots) are in good agreement with calculation combining the Fuchs-Sondheimer model [SON 52, FUC 38] with phonon mean free paths calculated from first principles [ESF 11] (dashed line). Data from other thermal conductivity measurements on thin Si films are also shown for comparison. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

With these advanced characterization techniques, nanoscale thermal conductivity can now be measured with unprecedented accuracy. This can lead to the development and testing of novel nanoscale structures, including energy harvesting and thermoelectric devices.

The study of the phononic and thermal properties of suspended membranes is the key to determining the thermal behavior of more elaborated structures leading to advanced electronic and photonics devices based on SOI and other thin-film stacks. These include opto-mechanical crystals or advanced opto-NEMS, which exploit the strong interaction between photons and phonons [EIC 09] obtained by the engineered mechanical and photonic properties in such devices and that at room temperature are extremely sensitive to thermo-optical effects. It can be argued that

several state variables in the solid state are intrinsically linked to phonon properties when it comes to dissipation, coherence and low-power operation.

7.3. Porous silicon for thermal insulation on silicon wafers

7.3.1. *Introduction*

Porous Si is a material that results from the electrochemical etching of bulk crystalline Si. Its structure and morphology depend on the Si wafer type and resistivity and on the electrochemical conditions used for its fabrication. A detailed description of its fabrication and properties is presented in Part 4 of this book.

The highly porous Si material is nanostructured and has the properties of confined systems, including a very low thermal conductivity, which is much lower than that of bulk crystalline Si. This is attributed to the structure and morphology of the material, composed of Si nanostructures, interconnected nanowires and nanocrystals, separated by voids. Phonon confinement in the Si nanostructures composing the material and the presence of voids are at the origin of porous Si very low thermal conductivity. In addition, the exact model describing its temperature behavior is complicated by the existence of a shell native oxide surrounding Si nanocrystals/nanowires. The ratio of this oxide compared to the Si core plays an important role in the mechanism of thermal conduction, especially at low temperatures.

Due to the much lower thermal conductivity of porous Si compared to bulk crystalline Si, thick porous Si layers locally formed on the Si wafer can serve as a local insulation platform for the integration on it of different thermal devices.

7.3.2. *Thermal conductivity of nanostructured porous Si*

In porous Si, the thermal conductivity decreases significantly with increasing porosity due to the increasing “air/nanostructured Si” ratio and the increased phonon-wall scattering in the Si nanostructures. Theoretical models often treat the problem using kinetic theory of phonons [MAR 12a], molecular dynamic simulations [FAN 11], Monte Carlo simulations [RAN 08] or by using the so-called phonon hydrodynamics model [ALV 10], which is a generalization of Fourier’s law, incorporating non-local effects and thermal slip along the walls. Based on this last method, an analytical expression of the effective thermal conductivity of porous Si was obtained in [ALV 10] as a function of porosity, pore radius and phonon bulk mean free path.

Different techniques were used to determine the thermal conductivity of porous Si, including the 3ω method [GES 97] and the direct current (DC) method [SIE 12, VAL 13]. In most of them, the measurements were made at room temperature, while little work was devoted to the determination of porous Si thermal conductivity at low temperatures [GES 97, VAL 13].

Within the Nanofunction, the thermal conductivity of porous Si with 63% porosity was determined in the temperature range 20–350 K, using the DC method [VAL 13]. The value of the thermal conductivity was derived from experimental results, combined with simulations using 3D FEM analysis based on Comsol multiphysics software. The 3D model used for the analysis was designed using the exact dimensions of the fabricated experimental device. The differential steady-state heat conduction equation:

$$\nabla(-k \cdot \nabla T) = Q \qquad [7.28]$$

was solved using boundary conditions determined from the experiment. Negligible radiation losses and self-heating phenomena were assumed, and care was taken in all cases to limit the current to values that do not introduce any self-heating phenomena. The model was first applied to bulk crystalline Si, using as input parameters the data obtained from the experiment (temperature at the backside of the Si wafer and temperature on the Pt resistor). The thermal conductivity of p-type bulk crystalline Si was thus obtained in the temperature range 200–290 K and compared with previous experimental and theoretical results from the literature [GLA 64, LID 05].

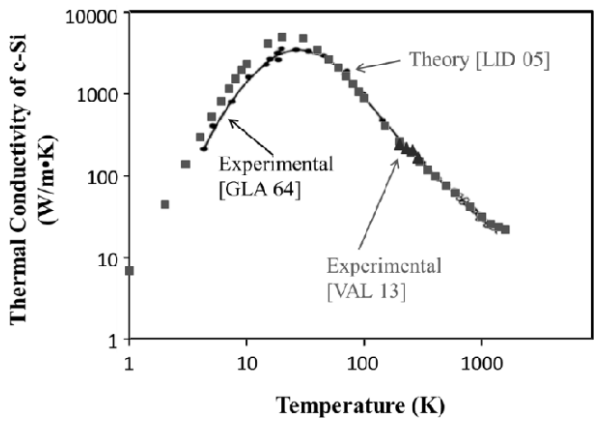

Figure 7.25. *Thermal conductivity of bulk crystalline Si as a function of temperature. Experimental [VAL 13, GLA 64] and theoretical results [LID 05]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The results are illustrated in Figure 7.25. The results from reference [VAL 13] are represented by triangles in the figure, while experimental results from [GLA 64] and theoretical results from [LID 05] are represented by circles and rectangles, respectively. From Figure 7.25, it is depicted that the results of [VAL 13] are in good agreement with those of the literature. This is a validation of the method used, which was then applied to the porous Si layer.

After the successful implementation on bulk c-Si, the method was applied to porous Si. The sample used was composed of a 40 μm thick porous Si layer on 340 μm thick bulk crystalline Si. A Pt resistor was integrated on the porous Si layer in the four-point probe configuration. The width of the Pt resistor was 20 μm and its length was 640 μm. The sample configuration is illustrated in Figure 7.26.

Porous Si was considered as an isotropic and homogeneous material, which is macroscopically a realistic approximation, since the PSi material from p-type Si is sponge-like, with homogeneous structure in the micrometer range. The values of thermal conductivity and heat capacity of bulk crystalline Si and Pt used in the simulation were taken from the literature [FLU 59, GLA 64].

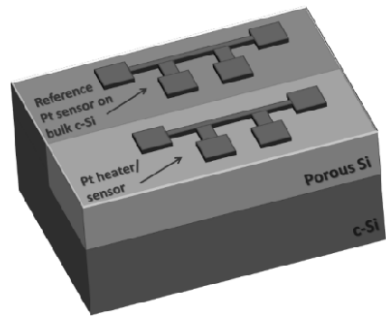

Figure 7.26. *Schematic representation of the sample used for porous Si thermal conductivity measurements in [VAL 13]. It is composed of one Pt sensor in four-point-probe configuration on a 40 μm thick porous Si layer and a similar Pt sensor on bulk crystalline Si*

The dissipated power per unit volume on the Pt resistor was calculated from the applied current, the measured voltage drop and the dimensions of the Pt resistor, using as boundary condition the temperature measured at the backside of the Si substrate.

The equation of continuity was solved at boundaries in thermal contact

$$-n_1 \cdot (-k_1 \cdot \nabla T_1) - n_2(-k_2 \cdot \nabla T_2) = 0 \qquad [7.29]$$

while the formula of continuity/symmetry

$$-n \cdot (-k \cdot \nabla T) = 0 \qquad [7.30]$$

was applied at every other boundary, assuming no heat transfer between the sample and the environment, as the measurements were performed in vacuum. The thermal conductivity of porous Si layer was the unknown parameter in the simulation, and it was calculated performing successive iterations until the average temperature over the entire volume of the resistor reached the measured temperature of the heater. The results obtained for the thermal conductivity of PSi as a function of temperature are illustrated in Figure 7.27 in comparison with those of bulk c-Si [GLA 64].

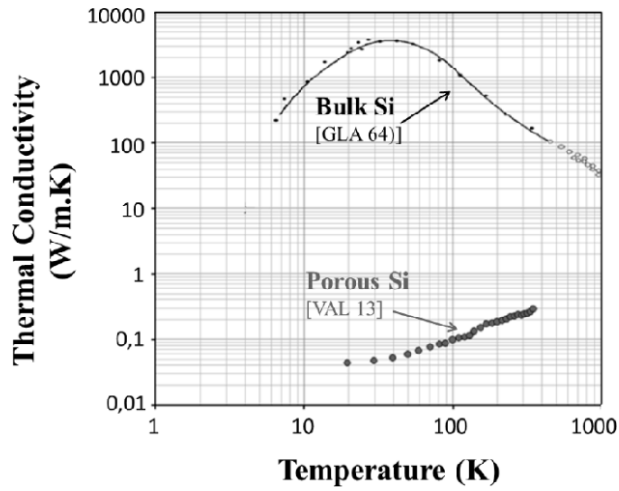

Figure 7.27. *Comparison of thermal conductivity of porous Si with that of bulk-crystalline Si*

Figure 7.27 illustrates that porous Si shows a much lower thermal conductivity than bulk crystalline Si, this difference exceeding four orders of magnitude at temperatures below 50 K and more than two orders of magnitude at room temperature. As can be seen in Figure 7.27, the temperature dependence of thermal conductivity of porous Si is monotonic and does not show any maximum for the measured temperature range, as in the case of bulk crystalline Si and other dielectric materials. This is a common behavior of glasses and other disordered materials at this temperature range, as illustrated in Figure 7.28. Phonon confinement in Si nanostructures composing porous Si, phonon-wall scattering and the existence of the native shell oxide surrounding Si nanostructures are expected to be at the origin of the above temperature dependence.

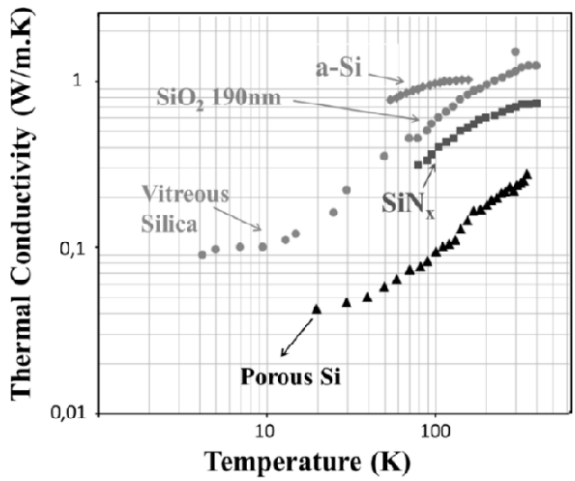

Figure 7.28. *Comparison of thermal conductivity of porous Si [VAL 13] with other low-k CMOS compatible materials taken from the literature: SiN_x and SiO_2 190nm [LEE 97], vitreous silica [SMI 78] and a-Si [CAH 89]*

It is deduced from Figure 7.28 that porous Si shows much lower thermal conductivity than the other usual low thermal conductivity materials (amorphous silicon, vitreous silica and silicon nitride). From all the above materials, the highly porous Si layer investigated in [VAL 13] shows the lowest thermal conductivity in the whole temperature range 20–350 K. This makes porous Si very adequate for use as a thermal isolation platform on the Si wafer for the on-chip integration of thermal (heating or cooling) devices and thermoelectrics.

7.3.3. *Thermal isolation using thick porous Si layers*

The effect of the PSi layer thickness on the temperature distribution as a function of depth from the PSi surface was investigated in [VAL 13] using FEM analysis. The same applied power was used for all samples. Two reference temperatures, 20 K and 290 K, were used. The maximum temperature difference on the heater as a function of porous Si layer thickness was determined. PSi layer thickness was taken between 10 and 100 µm. The results are given in Figure 7.29. The obtained maximum temperature difference on the heater under an applied heat power increases significantly with increasing PSi layer thickness for thicknesses below ~ 40 µm, while it tends to saturate for higher thicknesses.

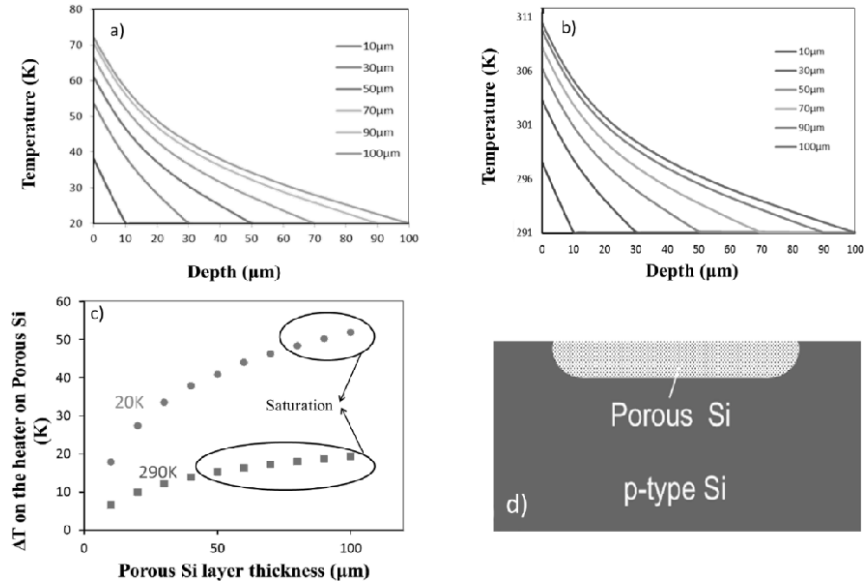

Figure 7.29. *Simulation results that show the effect of porous Si layer thickness on the thermal isolation from the Si substrate for a reference temperature of a) 20K and b) 290K. In c) the temperature difference on the heater is given for both reference temperatures as a function of porous Si layer thickness and in d) a schematic of the locally grown porous Si layer on bulk crystalline Si (micro-hotplate or micro-cooling platform) is depicted. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

From the above results, it is clearly demonstrated that thick porous Si layers provide an efficient local thermal isolation on the Si wafer that is very useful for the integration on Si of any thermal or thermoelectric device. The provided isolation is much more efficient at cryogenic temperatures, making it an excellent platform for use in cooling devices.

7.3.4. *Thermoelectric generator using porous Si thermal isolation*

7.3.4.1. *Introduction*

Thermoelectric generators are devices that take advantage of the Seebeck effect to convert heat into electrical power [DIS 99]. They are solid-state devices and therefore show excellent reliability combined with low noise operation and low fabrication cost. Their main disadvantage is their low conversion efficiency [CHE 05, LIM 05]. In order to assess the practical value of a thermoelectric generator, two factors have to be taken into account: the conversion efficiency and the cost of fabrication. The conversion efficiency is a factor dependent both on the

properties of the materials used and on the design and structure of the fabricated device. Most commercial devices use very efficient materials with figures of merit close to one [GOL 95]. Even though these types of materials have large efficiencies, they cannot be used in batch processing. As a result, their fabrication cost is higher than Si-based materials in batch Si processing. Such a material is polycrystalline Si (poly-Si). Even though its figure of merit and therefore its efficiency is low, this material is interesting for producing low-cost devices that can be combined on the same chip with Si electronics. In the literature, Si-based thermoelectric generators are almost exclusively MEMS devices. The thermal isolation in these devices is provided by the air or vacuum below the suspended membrane [HIC 93b, STR 04, HUE 08, WAN 09a, WAN 09b, XIE 10, SUJ 10]. However, although the provided thermal isolation in this case is excellent, the fabrication process is quite complicated and not compatible with standard Si processing. In addition, these devices are quite fragile. A much better solution is the thermal isolation described above, using a thick porous Si layer on bulk crystalline Si on which the thermoelectric generator can be integrated.

A thermoelectric generator (TEG) using local thermal isolation provided by a thick porous Si layer, locally formed on the Si wafer, was developed within the EU Nanofunction NoE and published in [HOU 13]. It takes advantage from the low thermal conductivity of porous Si [NAS 00, VAL 13] that is at room temperature, as described above, more than two orders of magnitude lower than that of bulk crystalline Si. This technology was successfully used in the literature in a number of thermal devices, such as in flow sensors [NAS 99, KAL 99, KAL 02] and gas sensors, working at low power consumption. Its successful implementation in a thermoelectric generator will be described below.

7.3.4.2. *Thermoelectric generator: design and fabrication*

The TEG using porous Si local thermal isolation is a miniaturized device composed of a silicon die of surface area below 1 mm^2 . The local porous Si layer is fabricated by electrochemical dissolution of bulk crystalline Si through a polycrystalline Si/silicon oxide masking layer, which is patterned to define the porous Si area. The fabrication conditions of the porous Si layer are described in [HOU 13]. The TEG is composed of a series of B-doped polycrystalline Si layers, contacted by Al. Two different devices were fabricated with different design topologies. The first device was a test device used to calibrate the thermoelectric generator (second device) and contained a polycrystalline Si heater and two series of thermocouples on both sides of this heater. In the TEG design, the heater was omitted (not necessary) and this helped to increase the density of thermocouples per unit surface area. An optical picture of the top view of the test device is depicted in Figure 7.30(a). The thermocouples have a length of 150 μm and each thermopile, made out of 10 thermocouples, covers an area of 150 μm × 400 μm. The distance

between the heater and the side of the thermocouples on the porous Si membrane was 40 μm.

The thermoelectric generator was composed of a series of 1,400 thermocouples, arranged along corresponding porous Si areas so as to have their hot contact on the porous Si layer and their cold contact on bulk crystalline Si. The length of each poly-Si leg of the thermocouples was 55 μm and its width was 10 μm. The total surface area covered by the thermocouples was 5.7 mm^2. Apart from the different topology and the absence of the heater in the TEG device, its fabrication process was exactly identical to that of the test device. An optical picture of the top view of the TEG is shown in Figure 7.30(b). In the case of the TEG, a temperature gradient between the "hot" contact of the thermocouples on porous Si and their "cold" contact on bulk crystalline Si, needed to test the device, has to be created externally by using appropriate encapsulation to allow local heating of only the "hot" contacts.

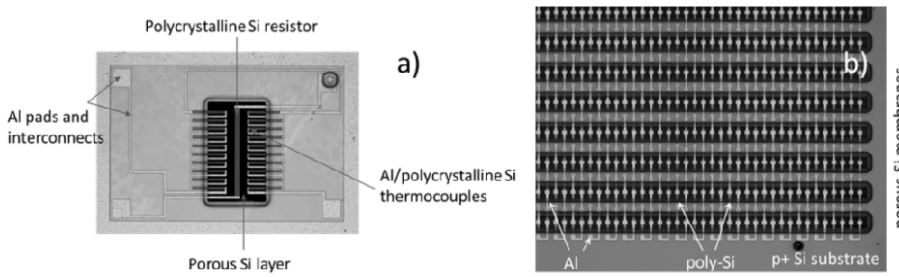

Figure 7.30. *a) Top view image of the first topology of the TEG device, depicting the porous Si layer, the polycrystalline Si resistor and the two series of thermocouples on its two sides, having their hot contact on the porous Si layer and their cold contact on bulk crystalline Si. b)Top view image of part of the second TEG device with 1,400 thermocouples in series*

7.3.4.3. *Encapsulation of the TEG device*

In order to translate a macroscopic temperature differential between the top and the bottom parts of the TEG to a temperature differential across the thermocouples, the encapsulation scheme of Figure 7.31 was followed. The poly-Si/Al thermocouples were covered by a thin dielectric, used for electrical isolation. This dielectric was a sputtered SiO_2 layer. A photoresist, 1.6 μm thick, was then spun on it and patterned so as to open holes over the porous Si layers. Finally, a thick Al cover layer was deposited and patterned so as to cover the entire active area of the device. Using this encapsulation scheme, a temperature applied to the top part of the Al cover is transferred to the "hot" part of the thermocouples, which lies on the porous Si layer and directly underneath the Al cover. On the other hand, the "cold" parts of the thermocouples that lie on the Si substrate are at the same temperature as

the bottom of the Si substrate as they are thermally isolated from the Al cover by the thick photoresist.

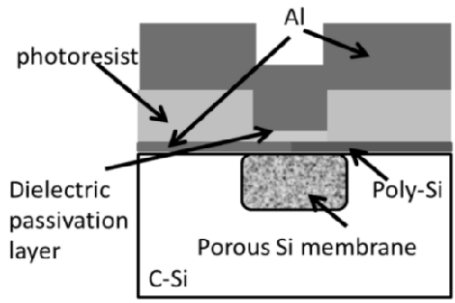

Figure 7.31. *Schematic representation of the cross-sectional view of the TEG encapsulation layers. The top Al layer serves to provide a stable "hot" contact temperature to the "hot"*

Finally, a housing was designed and fabricated in order to apply the macroscopic temperature differential between the top and bottom of the encapsulated TEG, composed of a top Al cover and a bottom Al chuck. This housing is schematically presented in Figure 7.32. The top Al cover is heated by a resistor, while the bottom Al chuck is at ambient temperature for small temperatures applied to the top Al cover. The temperature of both top and bottom parts of the housing is measured using commercial K-type thermocouples.

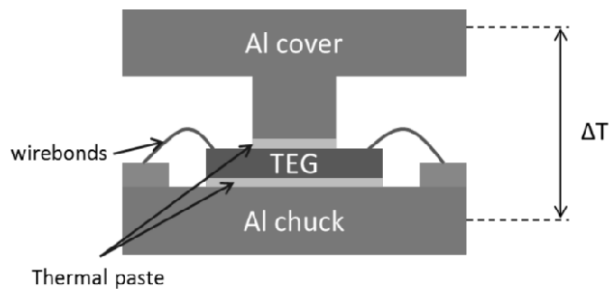

Figure 7.32. *Schematic representation of the housing used to transfer macroscopic temperature differentials to the thermoelectric generator (TEG)*

7.3.4.4. *TEG characterization and discussion*

1) Measurements on the test device

The output characteristics of the thermoelectric device were first obtained using the test device with the heater between the two series of thermocouples, which

serves to create the temperature gradient between the "hot" and "cold" contacts of the thermocouples. A current (I_{heater}) is passed through the heater using a current source, while the voltage drop across it (V_{heater}) is measured. A separate voltmeter was used to measure the output voltage of one of the series of thermocouples ($V_{thermopile}$). This is schematically illustrated in Figure 7.33.

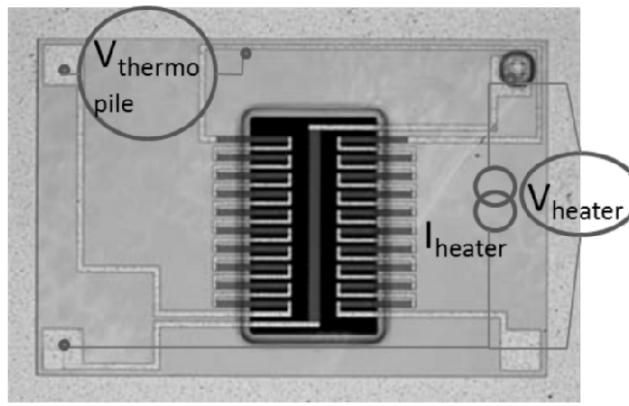

Figure 7.33. *Schematic representation of the circuit used for the characterization of the device on a picture of it*

The thermal isolation properties of the porous Si layer were tested by measuring the change of the heater resistance as a function of the applied power to it. The results are presented in Figure 7.34.

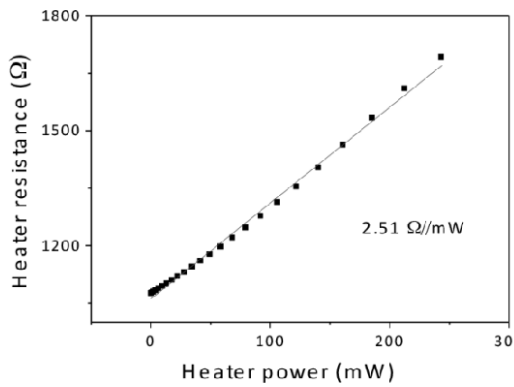

Figure 7.34. *Heater resistance as a function of the applied heater power*

From the slope of the plot in Figure 7.34, it can be seen that there is a 2.51 Ω/mW change in the heater resistance with the applied power. This is indicative of the good-thermal isolation provided by the porous Si layer considering that for the same heater on bulk crystalline Si this change is more than an order of magnitude smaller. Additionally, the plot of Figure 7.34 can be used to correlate the heater input power with the heater temperature. This can be done by correlating the value of the heater resistance with the temperature (measuring the value of the resistance for different values of temperature using very small power input).

The output signal across one of the thermopiles was also measured as a function of the applied power to the heater. The results are depicted in Figure 7.35. The slope of the curve is the responsivity of the device, measured for our TEG to be 0.72 V/W.

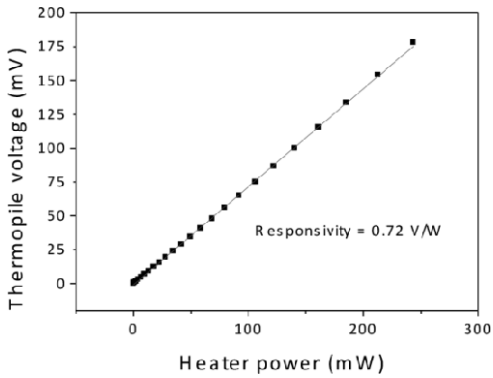

Figure 7.35. *Output voltage of one of the thermopiles as a function of the heater input power*

To measure the output power provided by each thermopile as a function of the heater input power, the output resistance of the thermopiles was measured to be 8.11 kΩ. A resistor of that value was placed in parallel with one of the thermocouples and the voltage across that resistor was measured as a function of the input power. The output power and current were then computed by measuring the voltage across the output resistor. The thermopile output power and voltage as a function of the heater input power are presented in Figure 7.36. The thermopile output power and current as a function of the heater input power are presented in Figure 7.37.

The measurements presented in Figure 7.34 along with the heater resistance versus temperature calibration curve can be combined with the results of Figure 7.37 to produce the plot of thermopile output power and current as a function of the heater temperature. This result is presented in Figure 7.38.

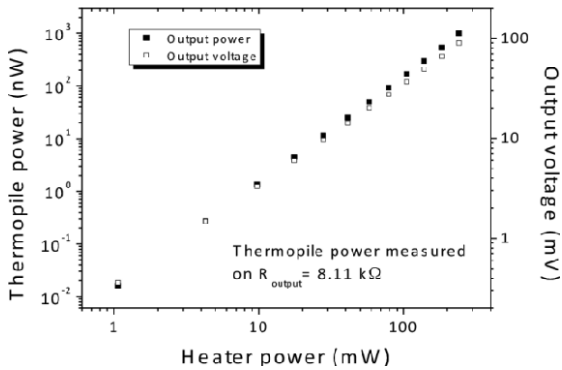

Figure 7.36. *Thermopile output power and voltage as a function of the heater input power*

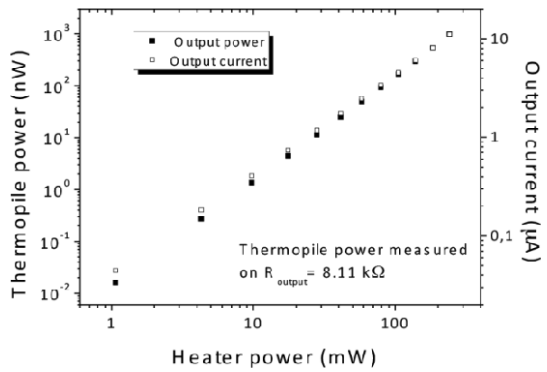

Figure 7.37. *Thermopile output power and current as a function of the heater input power*

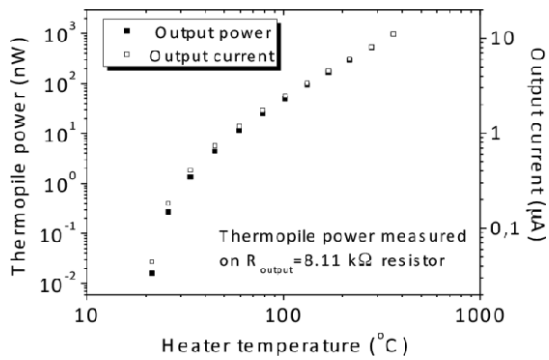

Figure 7.38. *Thermopile output power and current as a function of the heater temperature, with the assumption that the cold contact of the thermopiles is at room temperature*

Moreover, if we consider the output power of the thermopile over its area as a function of the temperature difference between the heater and room temperature (20 °C), we get the results of Figure 7.39. From this graph, the power efficiency factor φ of the fabricated thermoelectric generator can be calculated to be $\varphi = 0.015\ \mu W.cm^{-2}K^{-2}$. This result is very close to values reported in the literature for devices using far more complicated fabrication methods [HUE 08, XIE 10, SUJ 10, STR 04].

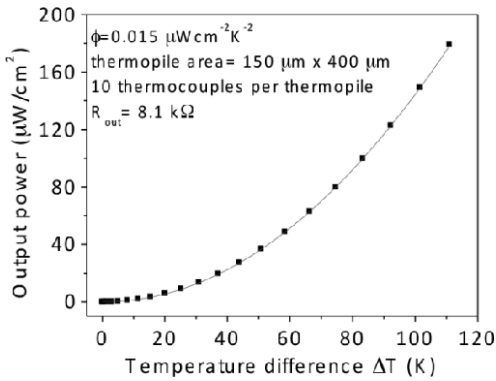

Figure 7.39. *TEG output power as a function of the applied temperature difference across the thermocouples*

2) Characterization of the encapsulated TEG

As mentioned above, the TEG device was composed of 1,400 thermocouples in series. This large number of thermocouples was used in order to increase the output voltage and power of the TEG compared to the test device. The measured output resistance was 0.4 MΩ, as expected.

The output voltage of the generator as a function of the macroscopic temperature differential ΔT applied to the housing is presented in Figure 7.40. The output power projected to a 1 cm^2 area device as a function of ΔT is presented in Figure 7.41. It can be clearly seen that the system delivers 0.4 $\mu W/cm^2$ of power for a 10 K temperature differential. This value exceeds the value reported in most papers in the literature under the same conditions, namely a naturally cooled bottom Al chuck and a small temperature differential [XIE 10, SUJ 10, WAN 09a]. Moreover this result is very close to practical applications using the heat generated by the body to power devices such as wristwatches. In these types of applications a power output of 1 $\mu W/cm^2$ for a ΔT of 10 K is considered to be the goal for a useful device [STR 04].

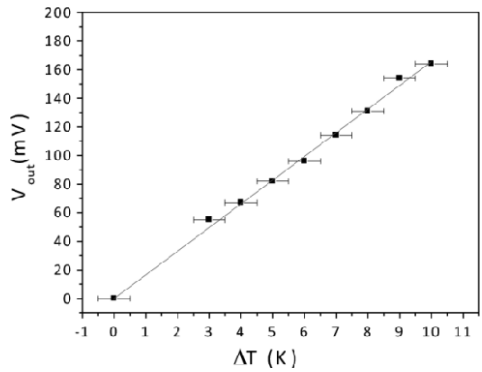

Figure 7.40. *Output voltage (V_{out}) of the generator as a function of the macroscopic temperature differential (ΔT) applied to the housing*

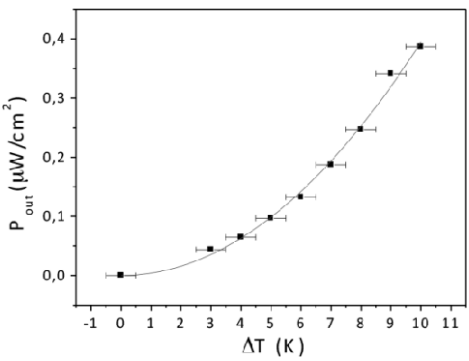

Figure 7.41. *Power output (P_{out}) projected to a 1 cm^2 device area as a function of the macroscopic temperature differential (ΔT) applied to the housing*

7.4. Spin dependent thermoelectric effects

The use of thermal gradients in a material to produce electrical energy, and vice versa, has enormous potential for applications in energy harvesting. However, applications are limited by the low efficiency of currently available materials and methods. The additional degrees of freedom provided by the electron spin and magnetic order have opened up a new research area that studies the interaction between the electron spin and heat, which is referred to as spin caloritronics.

Recent research has suggested that this new route can be used as a means of managing heat at the nanoscale and of controlling spin information by using heat currents.

However, potential applications of spin caloritronics require a detailed understanding of their fundamental properties, which are conceptually different from conventional thermoelectric effects. According to Bauer *et al.* [BAU 12], these new phenomena can be classified either as independent-electron (such as spin-dependent Seebeck) effects in metals that can be understood by the model of two parallel spin-transport channels with different thermoelectric properties, or as collective (such as spin Seebeck and magnon drag) effects, caused by magnons.

In this section we describe some of the basic concepts of spin-dependent thermoelectricity by using the universal two-spin current model and we discuss the spin-dependent Seebeck [SLA 10], the spin Seebeck [UCH 08] and the magnon-drag [COS 12] experiments. These experiments provide information on fundamental interactions that are essential in spin caloritronics, and make this field of research both complex and fascinating.

7.4.1. *Physical principle and interest for thermal energy harvesting*

Thermoelectricity in metals is governed by the electrical conductivity σ, the thermal conductivity κ, and by the Seebeck coefficient S. The Seebeck coefficient indicates that an applied temperature gradient across a conductor generates an electric field. In the two-spin current model, all of these parameters can be written as spin-dependent (↑, ↓ index referring to spin up and spin down). Therefore, the charge conductance is $\sigma = \sigma^{(\uparrow)} + \sigma^{(\downarrow)}$, thermal conductivity is $\kappa = \kappa^{(\uparrow)} + \kappa^{(\downarrow)}$ and the Seebeck coefficient is $S = (\sigma^{(\uparrow)}S^{(\uparrow)} + \sigma^{(\downarrow)}S^{(\downarrow)})/(\sigma^{(\uparrow)} + \sigma^{(\downarrow)})$.

In non-magnetic metals (NM), the population of spin up and down is the same; thus, the above parameters are equal. In a ferromagnet (FM), however, the transport processes for the majority and minority spins are different, leading to a spin-dependent conductivity $\sigma^{(\uparrow)}$, $\sigma^{(\downarrow)}$ and spin-dependent Seebeck coefficient $S^{(\uparrow)}$,$S^{(\downarrow)}$. In the linear response and using the Sommerfeld expansion

$$S^{(\uparrow,\downarrow)} = -e L_0 T \cdot \left.\frac{\partial \ln\left[\sigma^{(\uparrow,\downarrow)}(\varepsilon)\right]}{\partial \varepsilon}\right|_{\varepsilon_F} \qquad [7.31]$$

where ε is the energy and L_0 is the Lorenz constant, the physics of a thermoelectric spin model can be described by [JOH 87, BAU 12]:

$$\begin{pmatrix} J_C \\ J_S \\ J_H \end{pmatrix} = \sigma(\varepsilon_F) \begin{pmatrix} 1 & P & ST \\ P & 1 & P'ST \\ ST & P'ST & KT/\sigma \end{pmatrix} \begin{pmatrix} \nabla\mu_c / e \\ \nabla\mu_s / 2e \\ -\nabla T / T \end{pmatrix} \qquad [7.32]$$

where $J_{C,S,H} = J^{(\uparrow)} \pm J^{(\downarrow)}$ are the charge (C), spin (S) and heat (H) currents, respectively, and $P = (\sigma^{(\uparrow)} + \sigma^{(\downarrow)})/\sigma$ stands for the spin-polarization of the conductivity. We will also use the energy derivative $P' = \partial(P\sigma)/\partial\varepsilon$. The expression $\mu_c = \mu^{(\uparrow)} + \mu^{(\downarrow)}$ gives the charge electrochemical potential and $\mu_s = \mu^{(\uparrow)}) - \mu^{(\downarrow)}$ the spin accumulation.

According to equation [7.1], a temperature gradient drives a spin current in a conducting FM (the spin-dependent Seebeck effect) and spin accumulation drives a heat current (directly related to the spin-dependent Peltier effect), both proportional to P'ST. Conservation of charge and spin current at a contact between the FM and a normal metal (NM) results in spin injection into NM under voltage as well as temperature biases.

An electrically created spin accumulation can be detected by a switchable second ferromagnet in a lateral spin valve device [SIL 80, JOH 85, JED 02]. Using a similar device geometry, a thermally produced spin accumulation can be detected using the second ferromagnet and through temperature changes due to the Peltier effect [SLA 10, FLI 12].

In the *spin-dependent Seebeck* experiment [SLA 10], a temperature gradient is generated over an NM/FM interface. Since inside FM the individual Seebeck coefficients for the two spin channels $S^{(\uparrow)}$ and $S^{(\downarrow)}$ are not equal, a spin current proportional to $S^{(\uparrow)} - S^{(\downarrow)}$ flows through it even in the absence of a charge current, creating a spin accumulation μs which is maximum at the interface, and relaxes in the FM and NM on the length scale of the spin-flip diffusion lengths λ_F and λ_N. At a distance from the first FM electrode, the induced spin accumulation μ_s can be detected electrically with a second FM electrode via the thermoelectric interface potential $\Delta\mu = P\mu_s$. Because the FMs have different coercive fields, the spin accumulation is detected by the voltage variation as a function of magnetic field. The spin-dependence of the Seebeck coefficient combined with a heat current J_H therefore induces a spin current into the NM.

Following this demonstration, similar device geometry has been used to detect the reciprocal effect, i.e. the spin-dependent Peltier effect [FLI 12]. Here the heat current induced by injecting a spin current into the FM was detected in terms of the related temperature difference using a thermocouple.

The *spin Seebeck* experiment [UCH 08] refers to the generation of a transverse electromotive force in an NM in contact with an FM under a temperature gradient.

Current understanding of this effect hinges on the assumption that a spin current injected into the NM by the FM is transformed into an electric voltage by the inverse spin Hall effect (ISHE) [VAL 06, SAI 06]. Due to the spin–orbit interaction, the

ISHE is caused by the bending of electron orbits of up and down spins into opposite directions normal to their group velocity, producing a relatively large voltage for heavy metals.

The spin Seebeck effect was measured in ferromagnetic metals, in insulating FMs, ferromagnetic semiconductors and Heusler alloys, with similar phenomenology. The intrinsic physics is different from the spin-dependent Seebeck effect discussed above, because the conduction electron contribution is negligible, at least for the insulating materials. Here, the overall spin current is the result of an imbalance between the thermally excited spin currents over the interface by spin pumping [COS 06] and the fluctuating Johnson–Nyquist spin currents. To date, several features related to these experiments remain unexplained [BAU 12]. However, they have caught the attention of researchers because of the possibility of circumventing the relation between heat and thermal conductivities in thermoelectric devices. In the spin Seebeck effect experiments, the thermal gradient is applied on a material that can be a poor thermal conductor while the thermoelectric voltage builds up in a metal in contact with it that is transverse to the temperature gradient. The detailed understanding of these phenomena involves interactions between magnons, phonons and electrons. One of the methods that has been developed recently that provides such valuable information focuses on the detection of the magnon drag [COS 12].

7.4.2. *Demonstration of the magnon drag effect*

In ferromagnetic materials, conduction electrons are scattered by magnons, in addition to other electrons and phonons. Analogous to the scattering by phonons resulting in phonon drag effects, the electron-magnon interaction can produce magnon drag. In magnetic materials, a magnon current flows down the temperature gradient, which causes a thermoelectric voltage because of its interaction with the electron system.

However, a separation of the measured thermopower into the three different components–electron diffusion (S^e), phonon-drag (S^p) and magnon-drag (S^m)– is difficult in 3D FMs. At low temperatures the electron diffusion component dominates, whereas at high temperatures phonon drag and magnon drag may play a significant role. The presence of magnon drag is usually inferred indirectly from measurements of the temperature variation of the Seebeck effect, whose interpretation is usually problematic. Measurements as a function of magnetic field provide further information but the experiments have been performed above a few Tesla due to the low sensitivity of such measurements and in order to avoid the presence of magnetic domains and intrinsic anisotropic magnetoresistance that are common in thin films at low magnetic fields.

Because electron scattering by phonons and magnons are analogous, it has been long accepted that the phenomenology of magnon-drag should follow that of phonon drag, and the magnitude of the effect would be approximately given by $S^m \approx (C_m/ne)\,\alpha_m$. Here, C_m is the magnon specific heat, n is the electron density, e is the charge unit and α_m is the relative probability for a magnon to interact with a conduction electron. At low temperatures, where magnons interact predominantly with electrons, we would expect S^m to vary proportionally to $T^{3/2}$.

We recently demonstrated the use of a novel measurement scheme (see Figure 7.42) to study both magnon magnetoresistance and magnon-drag effects. It is based on a thermopile design that readily separates the contribution to the Seebeck coefficient of the magnons from the contributions of electrons and phonons. The scheme relies on the fact that a magnetic field parallel (antiparallel) to the magnetization leads to a decrease (increase) of the magnon population, as demonstrated by magnetoresistance measurements. This can be understood by inspecting the magnon dispersion relation for magnon wave vector k, which has the quadratic form $E(k) \approx Dk^2 + g\mu_B B_{int}$, where D is the magnon mass renormalization and $B_{int} = B+\mu_0 M$ corresponds to the magnetic-field induction B plus the ferromagnet magnetization $\mu_0 M$. A change in B modifies B_{int} and the magnon modes that are attainable at a given temperature. Therefore, a B antiparallel (parallel) to M should make the highest wave-vector modes (un)reachable.

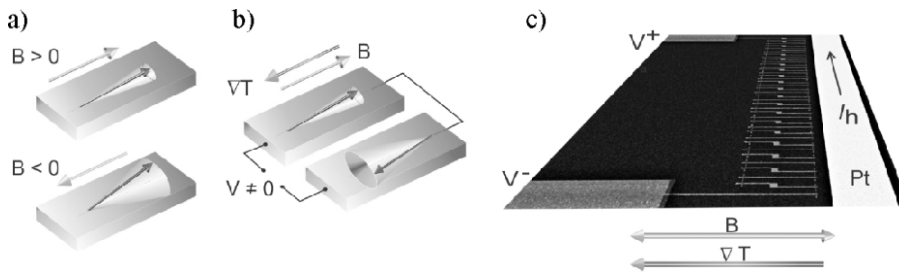

Figure 7.42. *Magnon-drag detection principle and geometry of the device. a) A ferromagnetic wire at a given temperature has a given population of magnons denoted by a magnetization precession angle. A magnetic field, B, applied parallel to the magnetization leads to a reduction of the magnon population. In contrast, an opposite B results in an increase of the magnon population. b) When the magnetizations are in the antiparallel configuration in the presence of B, a nonzero thermoelectric voltage is measured due to the magnon-drag, which is directly related to a different magnon population induced by B. c) Scanning electron microscope image (SEM) of a typical device which consists of a large number of pairs of Py nanowires (blue) connected by Ag (red) and having in proximity a wide Pt wire (yellow) which serves as a heater that generates a thermal gradient, ∇T. A voltage difference ΔV=V+-V- is measured as a function of the B applied along the wires. Adapted from [COS 12] © 2011 NPG. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The device consists of a large number of pairs of ferromagnetic (NiFe in [COS 12]) narrow wires placed between a hot and cold source and connected thermally in parallel and electrically in series. Each wire in a pair is identical to the other except for their geometry, which results in different coercive fields (B_{c1}, B_{c2}) to control the relative orientation of their magnetizations. When their magnetizations are in the antiparallel (AP) configuration in the presence of a magnetic field along the magnetization direction, the measured thermoelectric voltage is directly related to a difference in magnon population induced by the magnetic field. Other contributions to the thermoelectric voltage, such as electrons and phonons, are independent of the magnetization orientation and cancel out in each pair.

We measured the DC voltage generated between the V^+ and V^- electrodes as a function of a slowly sweeping magnetic field applied along the FM wires, while applying a temperature gradient along them. We take advantage of our geometry design. Because of symmetry arguments, in the parallel magnetization case, the thermoelectric voltages built up along the wires are the same and their contribution to $\Delta V=V^+ - V^-$ cancels out. In the AP configuration, the symmetry is broken simply because in the wires with the magnetization opposite to the magnetic field the magnon population is higher than in the wires with the magnetization parallel to it. Figure 7.42(a) shows typical data taken at 105 K [COS 12]. While sweeping the magnetic field from negative to positive, we observe a voltage when the magnetizations of the first wires flips at B_{c1}, resulting in an AP magnetization configuration. This voltage increases linearly with the field until the second wire flips at B_{c2} and, the magnetization is parallel again. At zero magnetic field, the voltage is zero independently of the magnetization configuration, which is direct evidence that the voltage is due to a difference in magnon population induced by the field. In addition, the thermopower is found to be linearly proportional to the square of the heating current, thus to the temperature gradient (see Figure 7.43(b)).

Figure 7.43(c) shows the temperature dependence of the magnon-drag effect. At low temperatures, the population of magnons is low and therefore the momentum transfer between the magnons and electrons will occur with high probability. Therefore, the temperature dependence comes entirely from the $T^{3/2}$ dependence of the specific heat. As the temperatures rises, the magnon population increases, and the magnon-magnon interaction becomes less rare. The magnon drag reaches a maximum when the interaction time due to magnon-electron scattering is comparable to that due to magnon scattering with any particles except electrons. At still higher temperatures, the magnon drag decreases because the magnon collision rate not involving electrons (with phonons and other magnons) rapidly increases and the momentum transfer to electron becomes ineffective.

The interpretation of these results by modeling will provide relevant information for the understanding of spin-dependent and spin Seebeck and Peltier effects. We also point out that the relationship between the dissipative spin-transfer-torque and the contribution of magnon drag to the thermoelectric power in conducting FMs can prove to be of crucial importance for current-driven domain-wall motion and spin torque experiments in general [LUC 11].

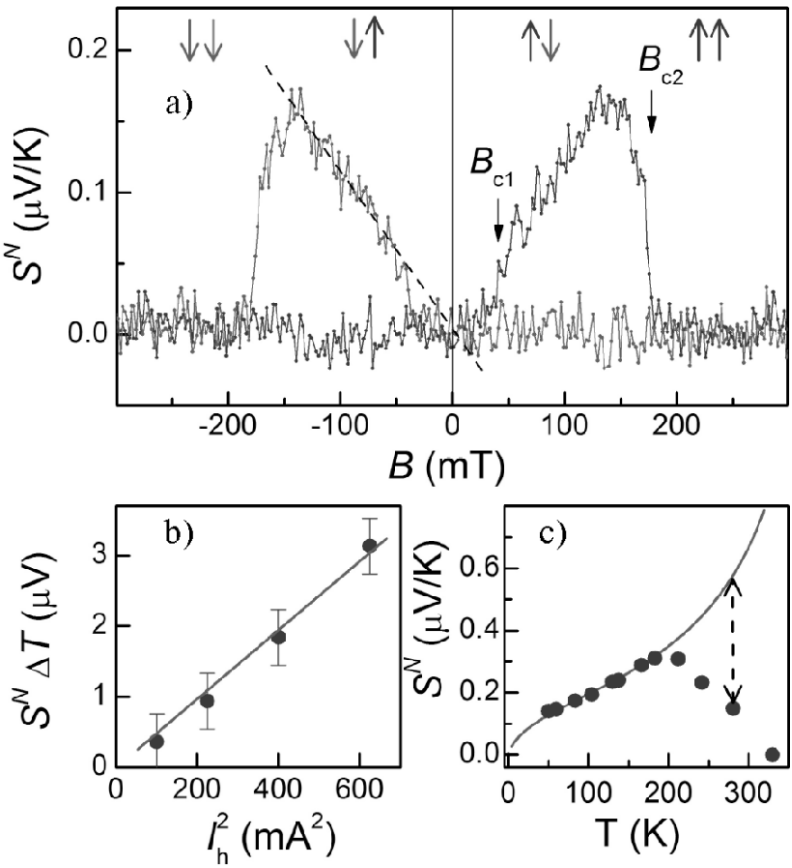

Figure 7.43. *Measurement of the magnon-drag effect. Thermoelectric power, S, as a function of B at 105 K. The red (blue) lines correspond to the negative (positive) sweep direction of the B. A d.c. voltage V that varies linearly with B and extrapolates to zero for B=0, is observed in the antiparallel configuration. b) Thermoelectric voltage V=SΔT as a function of the heat current, I_h at 50 K, the red line is a linear fit. c) Temperature variation of the magnon drag effect (solid circles). The line represents a best fit to simple modeling in the low-temperature regime. Adapted from [COS 12]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

7.5. Composites of thermal shape memory alloy and piezoelectric materials

This section explores an alternative route for thermal energy harvesting (TEH) with composites using the mechanical coupling between a thermal shape memory alloy (SMA) and a piezoelectric material.

7.5.1. *Introduction*

Besides macro-power systems such as solar cells, wind and watermills, unconventional small-scale power systems are in the process of emerging from labs. There is now an opportunity to harvest the many alternative energy sources that exist with the availability of ultra-low-power electronics. This trend is giving rise to substantial research activities in the field of micro or nano-energy harvesting. Micro- and nano-systems are – or will soon be – able to scavenge milliwatts or millijoules from vibrational, thermal and biological sources. But we have to keep in mind that this harvested power is derived from ambient sources so it is unregulated, intermittent and small. Indeed, ultra-low-power electronics (i.e. power management, voltage conversion, data storage and wireless transmission) are mandatory for applications. Thus, material engineering and electronic design are now part of a co-development scheme. This pattern is well established in the growing field of autonomous wireless sensors.

In less than a decade, micro-and nano-energy harvesting technologies have been developing based on single functional materials exploiting thermoelectricity or piezoelectricity mainly. More recently, smart materials or composites combining crossed-physical effects have been shown. Materials with enhanced properties will turn harvesting into a small but growing contributor to the world's energy market. Micro- and nanotechnologies now offer a real alternative over battery-powered solutions with virtually inexhaustible sources and no maintenance and little adverse environmental effects.

When considering thermal sources, which are the most prevalent in our environment, energy can be directly converted into electricity by means of thermoelectricity (Seebeck effect) or pyroelectricity. Thermoelectric and pyroelectric power generators are already demonstrated. However, applications require significant spatial and time dependent temperature gradients, respectively, to be efficient. This requires optimized cold source management systems. The cold source usually consists of a radiator whose size and shape can be quickly bound at small scales. Another strong limitation stems from the low voltage or current delivered by these generators, which requires complex and high power consuming buck boost converters for applications.

Another scheme pointed out is to indirectly convert heat into electricity through mechanical transformations using smart composite materials.

Smart composites originate from ordinary composites (i.e. used as structural materials) seeking enhanced properties from the bulk. But smart composites are well beyond this as they are tailored to control their shapes when subjected to external stimuli (i.e. electric, magnetic, mechanical and thermal).

The concept applies to TEH. Such a composite requires two materials being mechanically coupled. The first material (i.e. sensor) must exhibit large thermally induced strain. The second material (i.e. convertor) must exhibit large stress-induced electric voltage. Obviously, for the latter piezoelectric materials are best suited. For the former, thermal bimorph, thermoelastic materials and SMA can be used. In this way, thermally induced strain is converted into useful voltage with neither complex electronic nor cold source management system.

7.5.2. *Physical principle and interest for thermal energy harvesting*

The physical principle of TEH composites is based on the mechanical coupling between a thermal SMA and a piezoelectric material. The SMA element acts as a thermoelastic sensor. In the vicinity of the thermoelastic martensitic, phase transition temperature SMA exhibits unusual large thermally induced strains (i.e. up to 10%). Together with a large force generated at the phase transformation, SMA results in the largest known mechanical actuation energy density (i.e. up to 100 J/cm^3). The best candidates for thermal SMA are NiTi and TiNiCu alloys, which are used for industrial applications. Regarding piezoelectric materials, PZT exhibits superior piezoelectric properties for long. Thus, by coupling TiNiCu or NiTi with PZT materials, we may expect high thermal electric efficiency. TEH composites may harvest any natural time-dependent thermal variations (i.e. in opposition to forced) from few °C to hundreds of °C. As the physical principle is based on structural phase transition, the latter virtually resumes to a single temperature (i.e. the martensitic-to-austenite phase transition temperature). This temperature can be set by adjusting the SMA composition in a wide range from negative to positive values as well (see Figure 7.44). For applications, we have to consider the mechanical hysteresis of the material, which leads to a distribution of the transition temperature. By adjusting the SMA, composition hysteresis can be reduced down to a few °C as well.

Therefore, the expected benefits of TEH composites can be summarized as:

– use natural time-dependent temperature variations in contrast to forced gradients with thermoelectric generators. Therefore, neither radiator nor cold source management is considered;

– generate direct piezoelectric high voltage, which makes power management and voltage conversion simpler and lower power consuming than those of thermoelectric generators;

– be easily down sized as the crossed physical properties they depend on persist at micro and nano-scales, which contrasts with thermoelectricity.

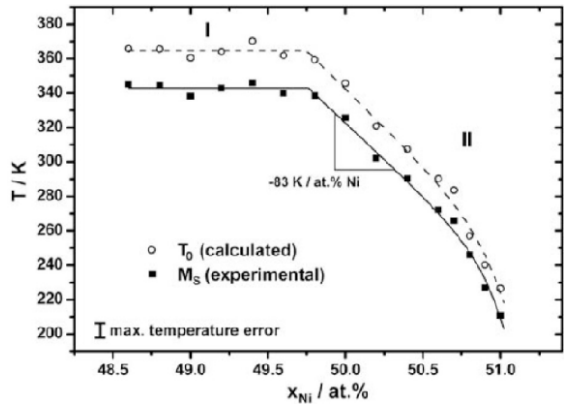

Figure 7.44. *Typical composition dependence of phase transition temperature for NiTi alloys from [FRE 10]*

7.5.3. *Novelty and realizations*

Although the concept of TEH composites was described earlier [JIA 01], there has been no application yet. The original theoretical scheme is shown in Figure 7.45. Such particulate-, wire- or pillar-based composites have not been fabricated with success for TEH applications so far.

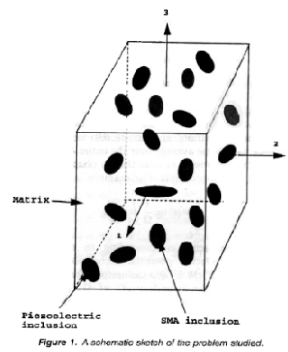

Figure 7.45. *Theoretical schematic sketch of TEH composite from [JIA 01]*

The first experimental result on harvesting natural thermal variations was reported in 2011 by our group, which is detailed later [ZAK 12]. It is based on a simplified composite scheme reducing to small TEH mechanical machines or thin-TEH laminated materials. Very recently, similar piezoelectric/SMA cantilever-type devices were shown as well [AVI 13]. The authors report significant generated power at various heating frequencies for temperature amplitude of about 100°C. The experimental value of energy generated per thermal cycle lies within the same order of magnitude (i.e. ~ 100 μJ). In our work, as smaller thermal variations (i.e. 10–60ºC) were investigated, higher experimental thermal electric efficiency is observed.

7.5.4. *Theoretical considerations*

In this section, theoretical considerations are presented regarding thermal electric efficiency. The energy conversion using SMA/piezoelectric harvester is discussed.

First, the phenomenon of shape–memory effect will be briefly introduced. During cooling, SMA undergoes martensitic transformation, which is a diffusionless first-order phase transition. As a result, the crystal lattice of SMA deforms by shear-like mechanism. The product of this transformation (i.e. cold) is called martensite and the parent phase (i.e. hot) is austenite. Not all the alloys undergoing martensite transformation exhibit shape memory (i.e. martensitic steels), but only those where this transformation is thermoelastic (i.e. the coherence between two phases is conserved). This coherent conservation allows reverse martensite transformation. Both direct and reverse transformations occur within a temperature interval (i.e. characterized by start and finish temperatures). In addition, thermodynamically conditioned thermal hysteresis prevents these temperatures from coinciding. Large stress and strain can be developed by SMA at heating up to 600 MPa and 10% for NiTi. Generally, the larger the strain and stress, the larger the temperature intervals and hysteresis. This imposes restrictions on the energy that can be harvested from a given system. Moreover, all these characteristics are significantly dependent on the SMA composition. That means that the choice of an optimal alloy and the adjustment of its composition for specific energy harvesting applications are required.

Thorough calculations of the efficiency of heat conversion into mechanical energy by SMA will not be provided here since so-called “martensitic engines” have been already intensively studied [WOL 80, BUL 90, LIU 04b, ZAK 10]. The input thermal energy required by the SMA body to perform mechanical work consists of the heat for increasing its temperature (i.e. by typically 20°C) and of the latent heat of transformation (i.e. ~20 J/g for NiTi). The typical value of input energy (i.e. heating SMA) is about 30 J/g. Specific mechanical work that can be produced by

SMA can be calculated as a product of the generated mechanical stress (i.e. ~ 500 MPa and 3% for NiTi). In this way, the extractable work can be estimated as 15 J/cm^3 or 2.3 J/g (i.e. with NiTi density of 6.5 g/cm^3). Therefore, the efficiency, which is the ratio of work to input heat, can be estimated close to 10%.

For TEH, this mechanical energy has to be converted into electricity. For this purpose, PZT material (i.e. PZT for lead zirconate titanate) with high mechanical coupling coefficient (i.e. k2 ~ 50%) is best suited.

Thereby, the total efficiency of SMA/piezoelectric harvester can be estimated close to 5%. This number is greater than those that we know for thermoelectricity and pyroelectricity (i.e. 0.1 to 1%).

It is worth noting that SMA can only produce work during heating and some mechanical bias elements (i.e. spring, elastic layer etc.) are needed to return to the cold state shape. This means that part of the work is lost into elastic energy within the bias elements. To minimize losses, the harvester should be designed in such a way that the piezoelectric element would act as a bias element for SMA. In the case of a laminated composite, a promising pre-strained configuration is proposed in this section.

7.5.5. *Examples of use*

The aim of this section is to describe two examples of use of TEH composites. The first example is in the form of a hybrid "machine" using two separated parts mechanically assembled and made up of shape–memory and piezoelectric materials, respectively. The second is based on a hybrid "laminated" structure using a multilayer of shape memory material and piezoelectric materials.

7.5.5.1. *Hybrid TEH "machine"*

7.5.5.1.1. Experimental details

The first example deals with a hybrid "machine" where the two functional materials are separated. SMA in the form of ribbon or wire is connected at its ends to a PZT plate (i.e. cantilever) through some intermediate elastic body (see Figure 9.46). Thereby, the "machine" uses the thermally induced linear strains of SMA (up to 5%) which bends the PZT cantilever-type plate through a specially designed, flexible mechanical structure. Here, the TEH "machine" operates at ambient temperature as the phase transition temperature of the SMA is ~70°C.

Note that a spring is used in this "machine", providing shape recovery of the SMA during cooling. We recall that the usual SMA is a one-way effect, since only

the high-temperature shape is memorized and the work is produced by SMA only at heating. It should be noted that an optimized TEH "machine" will not need spring since the piezoelectric material will be thicker and stiffer, thus acting as a spring itself. The optimized PZT thickness will allow us (1) to use all the strain generated by SMA and (2) to be stiff enough to return the SMA to its initial shape upon cooling.

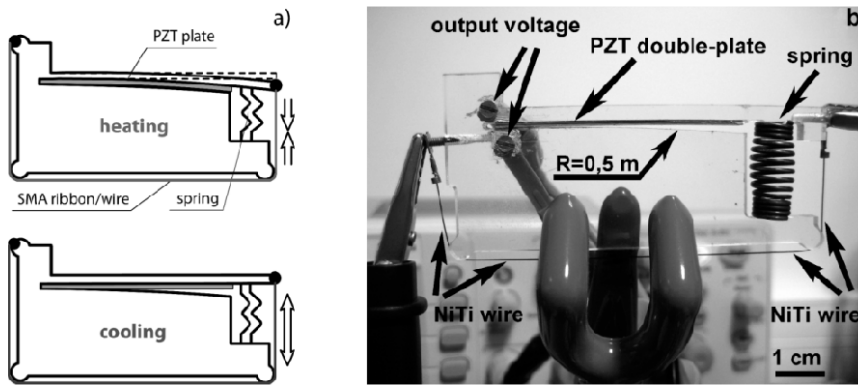

Figure 7.46. *a) Schematic views and b) photo of the TEH "machine"*

A commercial "PIC 255"-type PZT plate from "PI Ceramic GmbH" was used. A 0.5 mm thick plate was cut into 50×6 mm pieces. Two pieces were glued together using non-conductive commercial epoxy adhesive "3M Scotch-Weld DP460 Off-White" locally substituted with silver lacquer to provide an electrical connection between the electrodes. The sides of connection were chosen in such a way as to provide the charges of opposite signs on double-plate sides when bending (i.e. dual-g_{31} voltage generator configuration). After application of epoxy on the PZT plates and their connection, the double-plate was slightly pressed at room temperature for 24 hours.

Commercial NiTi wire from "Memry Corp." was used (13 mm long and 250 μm in diameter). When the wire was heated up for about 3 s through the thermoelastic transformation (~ 55-90ºC) using 1.7 W Joule heating, it shortened by 5 mm, which corresponds to a strain of 3.8%. When the wire shortened, the PZT double-plate bent. It was guided by the plexiglass bending frame which was shaped as an arc with a constant curvature radius of 0.5 m. Thereby, the piezoelectric element was subjected to a limited deformation that for a first approximation could considered as a homogeneous bending. With an assumption of pure bending, the maximal strain in the piezoelectric material is estimated at 0.1%. This value is close to the elastic strain limit in PZT (0.15%).

In a recent work [AVI 13], an alternative to resistive heating has been used with a non-contact method such as a light beam to heat the SMA. The light intensity and wavelength can be tailored from a remote location to modulate the temperature distribution and hence actuation characteristics of SMA.

7.5.5.1.2. Experimental results

Figure 7.47 shows the thermoelectric-like response of the TEH "machine" (i.e. in absolute value) for a single temperature change of ±35°C. The phase transition of the SMA occurs in the temperature region of ~ 55–90°C.

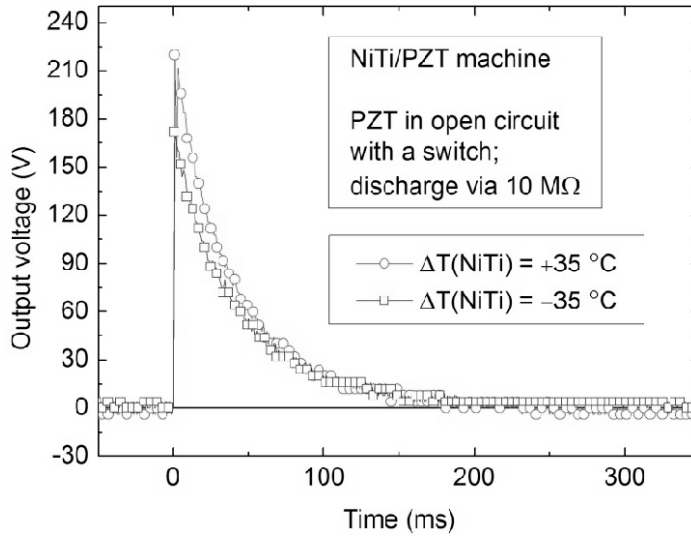

Figure 7.47. *Experimental output voltage (i.e. absolute value) of TEH "machine" for ±35 °C temperature variation*

When heating, a positive voltage is generated by the piezoelectric element, which bends due to the NiTi wire shortening. When cooling, the piezoelectric plate comes back to its original position and negative voltage is produced as well. We notice the remarkable high voltage of hundreds of volts that is a clear feature of the TEH composites. The maximum voltage is slightly lower when cooling, likely because of slower temperature variations at cooling resulting in higher charge leakage.

The experimental results show an indicative ratio of 6 V/°C for natural temperature variations. The equivalent thermal electric efficiency is of 3%. This

pattern contrasts with those of usual thermoelectric elements showing typically 0.1% with a cold source management. The remarkable high voltage is specific to the piezoelectric material and also originates from an optimized charges generating/collecting mode. Charges are generated in real open-mode circuit and accumulate in the piezoelectric element up to the maximum bending. Then, the circuit closes with a switch mechanism and the piezoelectric element fully discharges.

The total harvested energy is of 150 μJ for 35°C temperature variation (i.e. calculated from power versus time of discharge through 10 MΩ resistance). This gives a high figure of merit with 4 μJ/°C.

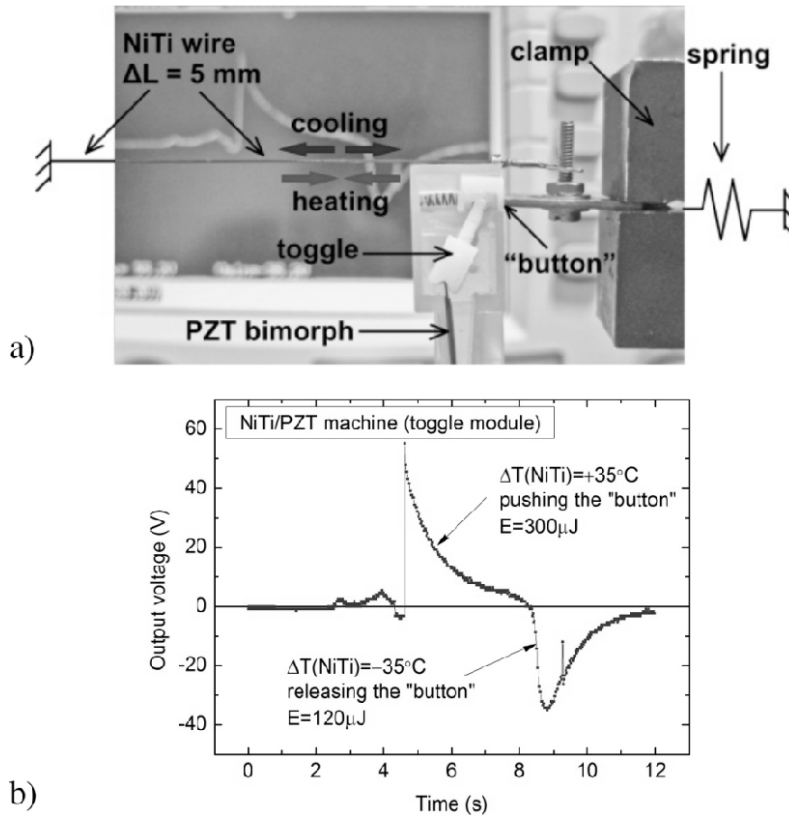

Figure 7.48. *a) Photo of toggle-type TEH "machine". b) Experimental output voltage for ±35°C temperature variation. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

In a recent evolution of the TEH "machine", a toggle mechanism (i.e. element based on commercial EnOcean linear motion converter) has been associated with the bending of the piezoelectric element (Figure 7.48). It results in larger harvested energy up to 400 μJ for the same temperature variation. The TEH figure of merit reaches as much as 11 μJ/°C, which is remarkable.

In terms of TEH applications, these numbers show that direct wireless transmission becomes possible (with ZigBee or EnOcean modules for example) with a simple step-down buck converter scheme. Therefore, simple autonomous wireless TEH sensors can be expected on the market soon.

7.5.5.1.3. Experimental results

The TEH "machine" is part of the new concept of TEH composite materials. It is best suited for compact autonomous wireless thermoelectric-like sensors. Hybridization of thermal shape memory alloy with piezoelectric materials leads to unusual large-thermal electric efficiency of several % without specific cold-source management. A remarkable feature of TEH composites consists of high voltage (i.e. hundreds of volts), allowing simple buck converter electronics. Finally, considering the volume of active materials, the density of harvested energy per °C for TEH "machine" is high (i.e. hundreds of $\mu J.cm^{-3}.K^{-1}$).

7.5.5.2. *Hybrid TEH laminated composite*

This second example of TEH composites illustrates another way of using SMA and piezoelectric materials in a laminated structure. Lamination is a usual fabrication process for composite materials. The main difference with the TEH "machine" is that the maximum thermally induced linear strains of SMA (up to 5%) cannot be used with the laminated structure as well. Indeed, as the SMA layer is mechanically not free, the mechanical stiffness of the piezoelectric layer plays a key role in the TEH laminated structure. Another difference is that in the laminated structures both SMA and piezoelectric layers are submitted to heat. Thus, we may expect pyroelectricity to occur in the piezoelectric layer. It is the aim of this section to show that pyroelectricity and shape–memory-drived piezoelectricity can be combined advantageously.

7.5.5.2.1. Experimental details

The TEH laminated composite was fabricated by assembling face-to-face SMA and piezoelectric bulk-type materials into a bilayer structure using cyanoacrylate glue (Figure 7.49). As for the TEH "machine", thermal sensing is ensured with SMA material. However, commercial NiTi wires are not well suited for lamination with a piezoelectric element here. Thus, SMA ribbons were used. The SMA material consists of recrystallized melt spun$Ti_{50}Ni_{25}Cu_{25}$ ribbons (i.e. 2 mm wide and 40 μm

thick) as detailed in [ZAK 10]. Before assembling with the piezoelectric material, the ribbon was pseudo-plastically pre-stressed in order to define a preferential deformation direction during thermoelastic transition to make it reversible. For a TEH laminated composite, the choice of the piezoelectric material is critical as its mechanical stiffness may hinder the thermally induced mechanical strain from the SMA material. Thereby, PZT plates (i.e. ceramics) cannot be used as for the TEH "machine". Therefore, flexible PZT material in the form of macro fiber composite (MFC) is best suited.

Here, we use commercial P1-type MFC from "Smart Materials Inc.". It consists of 100 µm diameter PZT fibers aligned horizontally between the top and bottom electrodes and packed with Kapton. The maximum operational strain reported in the datasheet is about 0.15%. Additionally, the P1-type advantageously uses the superior d_{33} piezoelectric effect of PZT by using interdigitated electrodes. When elongated or shortened, the PZT fibers generate electrical charges which can be collected at the bonding pads. As for the TEH "machine", an open/close charges accumulation/discharge scheme is used.

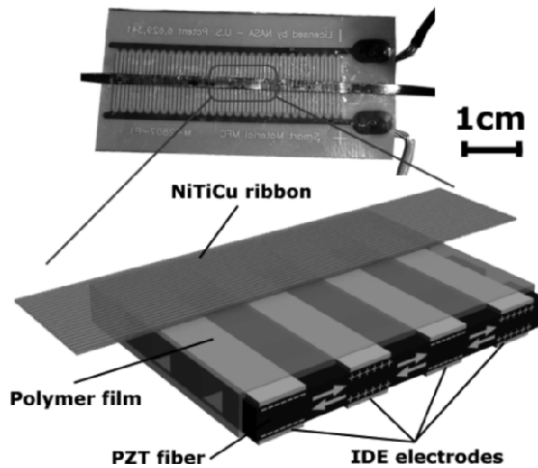

Figure 7.49. *Photo and schematic view of the TEH laminated composite (i.e. TiNiCu ribbon is glued on top of MFC with cyanoacrylate glue)*

To induce the deformation, the ribbon was Joule heated from ambient to 80°C in about 1 min (i.e. 2 W according to the ribbon resistance of 1.6 Ω).

7.5.5.2.2. Experimental results and discussion

The thermally-induced deformation of the SMA ribbon used with the TEH laminated is in the range of 0.1 to 0.6%. This number is consistent with those of MCF enduring 0.15% maximum strain. We can note that the start and finish temperatures of the direct and inverse transformations almost coincide and the hysteresis is rather small (i.e. less than 2°C).

Experimental generated voltage was measured with instant-discharge mode (i.e. real open circuit during deformation). A switch briefly closes when the selected temperature is reached and closes again when cooling is complete. Positive voltage is generated when heating as the TiNiCu ribbon contracts (i.e. MFC is bent with uniform tensile stress). Conversely, negative voltage is generated when cooling as the ribbon extends (i.e. MFC is bent with uniform compressive stress). This is consistent with MFC voltage coefficient $g_{33,}$ which is positive.

Figure 7.50 shows the temperature dependence of the output voltage of the TEH laminated composite. First, remarkable high voltage of a hundred volts is confirmed for the TEH "machine". Second, we can note that the thermal electric efficiency is slightly larger with TEH laminations (i.e. up to 6 V/°C). Again, this picture is in contrast to usual thermoelectrics elements characterized by one order of magnitude less.

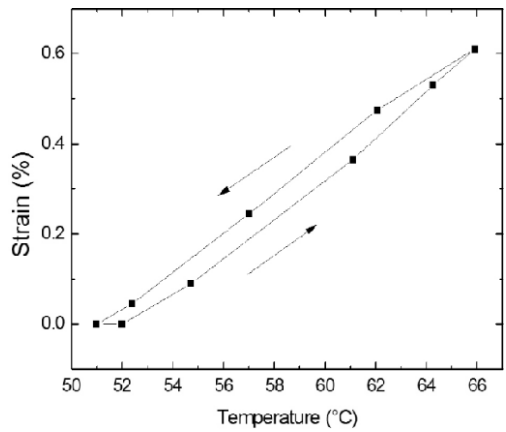

Figure 7.50. *Typical temperature dependence of flexural strain of the SMA used with the TEH laminated composite (i.e. recrystallized TiNiCu melt spun ribbon) from [AVI 13]*

Considering the volume of active materials, TEH laminations exhibit a lower figure of merit than TEH "machines" by 1:10 (i.e. 0.01 $mJ.cm^{-3}.K^{-1}$). This decrease is mainly to due to a lowered harvested energy for a similar voltage as the

capacitance of interdigitated piezoelectric elements is much lower than those of usual piezoelectric plates.

Thereby, TEH laminated composites are fully effective in converting SMA thermal strain to voltage within the phase transition region. Beyond this temperature region, only thermal dilatation is expected, which is few orders of magnitude lower and would not contribute significantly to voltage generation.

However, we may note that a significant voltage is already generated when heating (or cooling) before the SMA phase transition region. This behavior was not observed with the TEH "machine". It indicates that pyroelectricity superimposes to the TEH laminated composites. This is revealed in Figure 7.51, where the temperature dependence of output voltage of TEH laminated composite is compared to that of MFC alone.

In conjunction with this work, this experiment demonstrates that pyroelectric voltage measured with real instant-discharge mode can be large (i.e. 4 V/°C) with MFC, which was still uncertain with such piezoelectric composite materials. Therefore, pyroelectric voltage advantageously participates in the response of the TEH laminated composite (i.e. in the order of 20 to 30%). It is difficult to quantify more precisely the ratio between pyroelectric voltage and thermally induced deformation voltage as the effective temperature may significantly differ at the SMA and at the MFC surface, respectively (i.e. only part of the heat transfers from SMA to MFC). Optimization of heat transfer in TEH laminated composites may lead to a significant improvement as amplitudes of both effects are comparable (~ several V/°C).

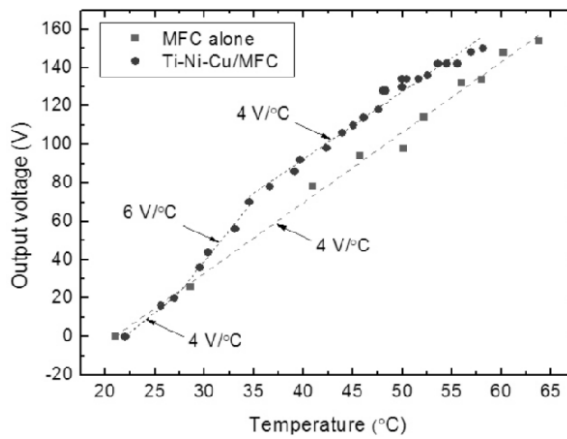

Figure 7.51. *Experimental temperature dependence of output voltage for TEH laminated composite and MFC alone, respectively*

To conclude, TEH laminated composite slightly differs from the TEH "machine" composite as the two functional elements are no longer separated. Mechanically speaking, lamination is negative (i.e. thermally induced SMA deformation is hindered). On the other hand, lamination is opened to pyroelectricity as both elements are heated. Therefore, TEH laminated composite offers attractive prospects for harvesting time-varying natural thermal fluctuations. It is best suited for ultra-compact TEH applications as lamination is thin (i.e. no radiator required).

7.5.6. *Summary of composite harvesting by the combination of SMA and piezoelectric materials*

This section lays the cornerstones of alternative thermal energy harvesting (TEH) applications based on a composite scheme. Composites offer the possibility of crossed-properties with enhanced or unusual performances. Here, the mechanical coupling between a thermal SMA and a piezoelectric material is pointed out. This combination leads to remarkable high thermal electric efficiency (i.e. several V/°C) and a large density of harvested energy (i.e. several hundreds of $\mu J.cm^{-3}.K^{-1}$). Two configurations of TEH composites were discussed. The first composite consists of a TEH "machine" using separately SMA and piezoelectric ceramic materials with a cantilever or toggle mechanical design (i.e. abutting edges). The second composite is based on laminations, where the SMA and piezoelectric layers are joined over the surface (i.e. glued to one face). The former has a larger thermal mechanical electric efficiency as the SMA material can deform more freely. The latter takes advantage of an additional pyroelectric effect as the piezoelectric element heats simultaneously. Finally, unusual large thermal electric efficiency of several % and remarkable figure of merit of several hundreds of $\mu J\ cm^{-3}.K^{-1}$ were demonstrated without specific cold source management. In terms of application, an outstanding feature of TEH composites consists of voltage of hundreds of volts allowing simple buck converters and ultra-low-power electronics. Thus, we conclude that TEH composites open the way for compact (i.e. ultrathin) thermoelectric-like generators and autonomous wireless thermal sensors.

7.6. Conclusions

As shown throughout this chapter, many new solutions are being explored at the research level to enhance the efficiency of thermal energy harvesting. Materials nanostructuration is offering strong opportunities to replace polluting or rare materials that are being used in present thermoelectric systems at low and medium temperature, while new concepts are starting to be studied or developed. However, these different approaches are featuring different capabilities. For instance, it is likely that thermoelectric applications will be preferred for quite large temperature

gradients in a temperature range which may be quite wide and unpredictable, while the association of thermally switchable materials with piezoelectric energy harvesting should be very efficient for the exploitation of limited temperature variations around a well-defined reference temperature. These different approaches will probably be developed in parallel as they are complementary rather than competing. They all offer exciting prospects both from the fundamental point of view and in terms of applications.

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8

Nanowire-based Solar Cells

8.1 Introduction

Photovoltaic energy is one of the most promising sources of renewable electricity and its rapid development during the last decade due to incentive policies have enabled us to reach grid parity in several European countries. Most of the installed modules are fabricated using bulk silicon wafers and p–n homojunctions also called first generation solar cells. Even if the actual price of photovoltaic modules is very low, many efforts are still necessary to decrease material consumption in order to limit gas emissions during the processing of silicon wafers used for the fabrication of these bulk silicon first generation solar cells. Second generation solar cells or thin film solar cells are good candidates to reach low prices and low material consumption. However improved light trapping schemes are necessary to maintain high efficiencies.

Nanowire (NW) based solar cells are an attractive approach to fabricating solar cells with efficient light trapping scheme and high collection efficiency in case of radial junctions (Figure 8.1). In fact, the high aspect-ratio of NWs permits us to significantly reduce the solar cell thickness without the loss of optical absorption while simultaneously providing the effective carrier collection in the case of radial junction. This structure benefits from the long optical path within the NW length and, by exploiting a radial junction, a shorter path for carrier collection corresponding to the wire radius is achieved, leading to a smaller carrier recombination rate [GAR 11, KEL 10]. Efficiencies similar to or higher than those obtained with first generation solar cells are expected for single junction NW solar cells with a cost reduction due to material consumption and low cost growth

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methods. A photoconversion efficiency as high as 7.9 and 13.8% has been reported for core–shell Si and InP NW arrays, respectively [PUT 10, WAL 13].

Concerning Si NW-based solar cells, important work has been achieved due to the possibility of fabricating thin, flexible and cheap solar cells with this widely used material. Moreover interesting heterostructures combining an amorphous Si (a-Si) shell with a crystalline Si (c-Si) core can be fabricated leading to promising efficiencies [JIA 12].

While many works have been published on Si NW-based structures, another structure based on ZnO NWs associated with a direct bandgap II–VI material shell received a renewed interest. In fact, ZnO can be grown within the NW morphology and covered with CdSe [LEV 05], ZnS [WAN 10], ZnSe [ZHA 12], or CdTe [CON 11, WAN 10] in order to create a type II band alignment heterojunction (Figure 8.1). In particular, CdTe with its bandgap energy of 1.5 eV correlated to an absorption coefficient higher than 104 cm^{-1} can absorb light in the wavelength range from 250 to 830 nm, which is particularly adapted for photovoltaic applications. A thin layer of this absorber is sufficient to absorb most of the visible solar spectrum even if the absorption of ZnO is negligible (due to its wide bandgap energy equal to 3.3 eV).

This chapter focusses on the designing and characterization of a-Si/c-Si and ZnO/CdTe NW-based solar cells. Silicon solar cells will be considered as a reference structure and ZnO/CdTe as a prospective structure based on a direct bandgap absorber.

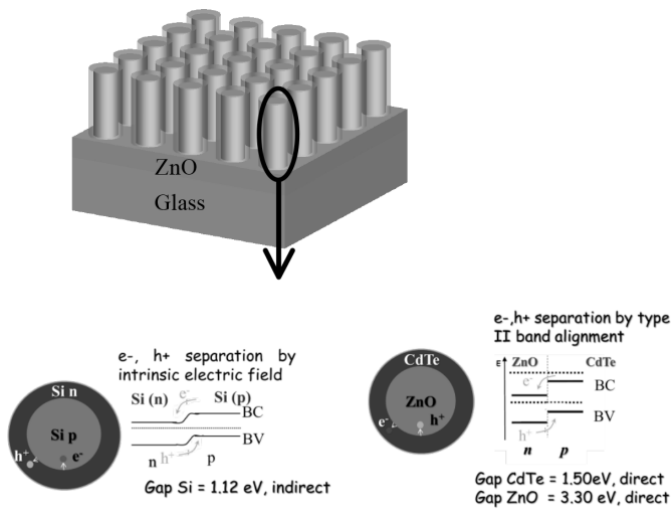

Figure 8.1. *Top: NW-based solar cell on low cost substrate. Bottom: cross-section and band diagram of Si and ZnO/CdTe NW solar cell*

8.2. Design of NW-based solar cells

In order to demonstrate the potentiality of c-Si/a-Si and of ZnO/CdTe core–shell NW arrays and to improve light absorption for photovoltaic applications, an optimization of light absorptance is usually performed by numerical optical simulation. Moreover, one drawback of NWs is the presumably high recombination rate due to the relatively large surface area of the front external interface with respect to the planar counterpart. In addition, a core–shell structure exhibits an interface between different materials which may be potentially affected by large recombination. Finally, electrical transport may be significantly influenced by traps and by relatively low carrier mobility in non-crystalline materials. Therefore, a predictive analysis of electrical performance by Technology Computer Aided Design (TCAD) simulation coupled to the optical simulations is required.

8.2.1. *Geometrical optimization of NW-based solar cells by numerical simulations*

The theoretical ideal photo-generated current improvement exhibited by NW arrays can be predicted by numerical simulation. The photo-generated current density can be compared to that of planar configuration to analyze the improvement induced by the nanostructuring of the solar cell surface. Concerning c-Si NW-based solar cells, several studies based on optical simulations have been published [LIN 09, WEN 11, KEL 09, KEL 10, KAI 11]. However, in the case of c-Si/a-Si (Figure 8.2) and ZnO/CdTe (Figure 8.3) structures, only a few attempts have been performed to optimize the absorption from an optical point of view by using numerical optical simulations. As the dimensions of the investigated structures are comparable to the incident radiation wavelength, diffraction effects play a decisive role in determining the optical behavior of NWs. Therefore the optical simulations of nanostructures must be performed by means of rigorous solvers of Maxwell equations such as the Finite Element Method (FEM) [JIN 02], the Transfer Matrix Method (TMM) [WHI 99] and the Finite Difference Time Domain (FDTD) [KUN 93] which have been used for example in [LIN 09, WEN 11, KEL 09] to calculate absorptance characteristics in NWs. However, methods such as FEM and FDTD are remarkably CPU- and memory-demanding especially for applications involving the optical simulations of NW-based solar cells. Recently the Rigorous Coupled-Wave Analysis (RCWA) method [MOH 81] has been adopted for the numerical simulation of the light absorption in thin film [AGR 10] and NW-based solar cells [KAI 11] allowing us to attain an excellent trade-off between accuracy and computational resources requirement, especially if compared with the FDTD method [SEM 12]. In [MIC 12, ZAN 13a, ZAN 13b, ZAN 13c], RCWA simulations result in an increased absorption of the NW array compared to their planar counterparts. In the following, the photo-generated current density is calculated as:

$$J_{ph} = \frac{q}{hc}\int A(\lambda) I_{ASTM}(\lambda)\lambda d\lambda \qquad [8.1]$$

where q, h and c are the electron charge, the Planck constant and the speed of light in vacuum, respectively. I_{ASTM} is the solar irradiance [AST XX]. J_{ph} is computed by assuming normal incidence of the light with respect to the device plane (θ = 0 degree and φ = 0 degree in Figure 8.1). In equation [8.1] $A(\lambda)$ denotes the absorptance as the ratio of the photo-generated photons within the semiconductor to the incident light at a given wavelength λ. In the following study, $A(\lambda)$ is computed for a relatively extended range of geometrical parameters, including the NW height H, the NW diameter D and the periodicity P (Figures 8.2 and 8.3). The optical databases used are taken from [MIC 12] for ZnO, from [ADA 93] for CdTe and from [PAL 88] for c-Si. The refractive index of glass substrate is 1.5.

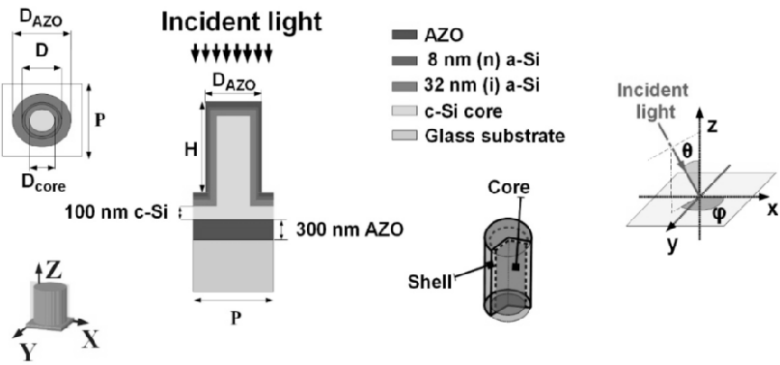

Figure 8.2. *Sketch of c-Si/a-Si core–shell NWs on glass substrate. D and P denote the shell diameter and the periodicity, respectively*

8.2.1.1. *Geometrical optimization of heterojunction core–shell c-Si/a-Si NW arrays*

The photo-generated current density J_{ph} has been calculated for NW array height H from 1 μm to 10 μm, periodicity P from 200 nm to 700 nm and ratio shell diameter D to P from 0.2 to 1.0; the maximum J_{ph} resulting from the maps illustrated in Figure 8.4 ranges from 18.25 mA/cm^2 (H = 1 μm, P = 400 nm and D/P = 0.7) to 22.94 mA/cm^2 (H = 10 μm, P = 450 nm and D/P = 0.8). In Figure 8.3(d) it is worth noting that the maximum photo-generated current density saturates with increasing H, therefore within the H-range 1–10 μm a good trade-off between absorption enhancement with respect to the planar counterpart (which features the same volume of c-Si of the corresponding NW, front 40 nm-thick a-Si layer, 200 nm-thick top AZO layer, 300 nm-thick bottom AZO layer and glass as substrate) and volume of

absorbing material is observed. In Figure 8.5 the monochromatic absorptance versus wavelength characteristic calculated for a 10 μm-height NW array (P = 450 nm and D/P = 0.8) is shown. It is worth noting that the calculated absorptance is markedly above 0.4 within the spectral range 450–800 nm. However, most of the solar optical power within the portion of the spectrum below the cut-off wavelength of the a-Si (730 nm) is absorbed by the NW shell (Figure 8.6). The transmittance of the NW array is negligible within the range of 300–680 nm. For radiation wavelength above 730 nm the absorption mainly occurs in the c-Si core region, however, part of the radiation is transmitted through the c-Si/AZO interface at the bottom, or reflected back to the NW because of Fresnel reflection.

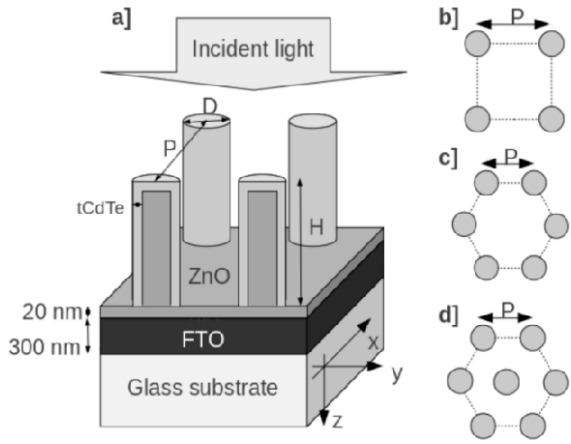

Figure 8.3. *a) Schematic view ZnO/CdTe NW arrays on FTO/glass substrate without conformal CdTe layer. The three investigated geometrical configurations are b) square, c) hexagonal and d) triangular*

8.2.1.2. *Geometrical optimization of type II band alignment core–shell ZnO/CdTe NW arrays*

The ZnO/CdTe core–shell NW arrays are usually deposited on a seed layer of ZnO nanoparticles (required for the formation of ZnO NWs [GUI 12]) grown on top of FTO/glass substrates as depicted in Figure 8.3. Fluorine doped tin oxide (FTO) and ZnO seed layer thicknesses are 300 and 20 nm, respectively. Square, hexagonal and triangular geometrical arrangements of ZnO/CdTe core–shell NW arrays (Figure 8.3(b–d)) have been investigated. For all geometrical configurations, the periodicity (P) is defined as the distance between the centers of two adjacent NWs. Here P varies within the range of 200–700 nm while the ratio D/P from 0.2 to 0.9. The CdTe thickness (t_{CdTe}) varies in the range of 20–100 nm. The effects of the substrate reflectivity are considered by replacing glass substrate with an ideal reflector.

Equation [8.1] is numerically calculated in the wavelength range of 300–830 nm since for higher wavelengths, ZnO/CdTe core–shell NW arrays do not absorb light.

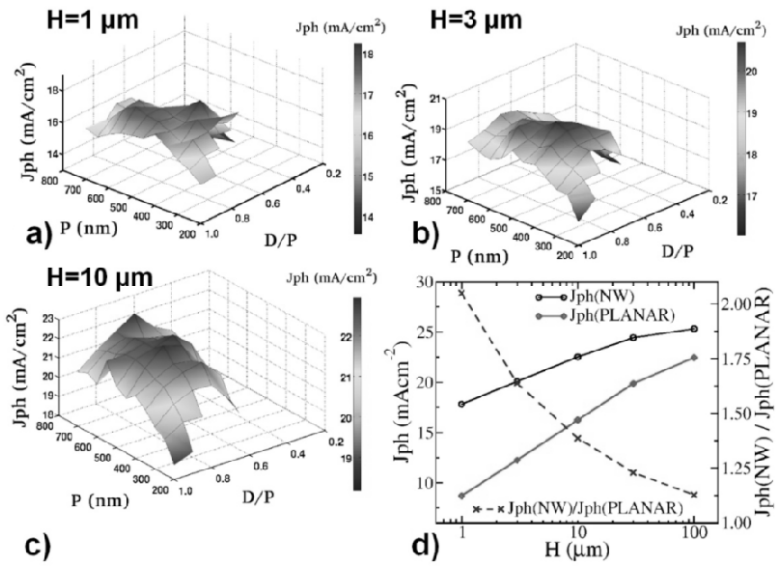

Figure 8.4. *Maps of the calculated photo-generated current density J_{ph} versus the ratio of shell diameter D to periodicity P for a) H = 1 µm, b) H = 3 µm and c) H = 10 µm; d) the calculated J_{ph} as a function of NW array height H. Comparison with planar counterpart is shown. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

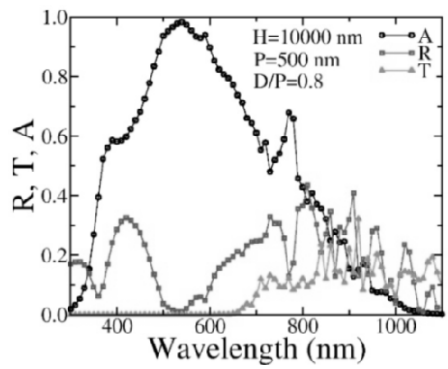

Figure 8.5. *Reflectance R, transmittance T and absorptance A characteristics versus wavelength of the NW*

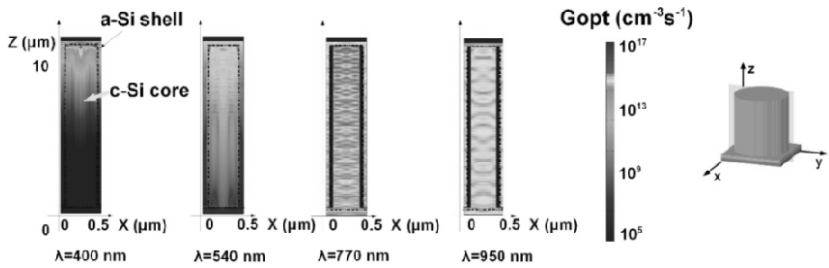

Figure 8.6. *Optical generation rate (Gopt) maps calculated by RCWA simulator in the symmetry cross-section of the NW (P = 500 nm, H = 10 μm, D/P = 0.8) at different wavelengths λ. The incident electric field amplitude is 600 V/m. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

A typical map of the ideal short-circuit current density for ZnO/CdTe NW arrays distributed in a square geometrical configuration is reported in Figure 8.7. The maximum J_{ph} of 24.89 mA/cm^2 is found for P = 350 nm and D = 210 nm. A small variation in the calculated J_{ph} around its optimum can be observed regardless of the considered geometrical configuration.

It is shown (Figure 8.8(a)) that, similar to the case of the c-Si/a-Si NW array, J_{ph} saturates for H > 10 μm close to the upper bound limit of 28.67 mA/cm² computed by using equation [8.1] (assuming unitary absorptance). This demonstrates that ZnO/CdTe NW arrays can effectively absorb light. The absorption properties of ZnO/CdTe NW arrays are investigated by adopting as figure of merit the enhancement factor, which is computed as the ratio of the J_{ph} for NW arrays to the J_{ph} for planar layers with the same amount of CdTe. For t_{CdTe} > 60 nm, the enhancement factor decreases from 1.6–1.8 for H = 1 μm to 1.43–1.37 for H = 30 μm (Figure 8.8(b)). However, for relatively large height arrays, the planar layers result in large light absorption due to larger CdTe volume. Indeed, the enhancement factor saturates to 1.37, confirming the excellent absorption properties of ZnO/CdTe NW arrays.

The photo-generated current density J_{ph} of ZnO/CdTe NW array is illustrated in Figure 8.9 either for glass substrates or for an ideal reflector. The photo-generated current density saturates at a smaller height for a given t_{CdTe} by using the ideal reflector with respect to the case of the glass substrate, revealing that light needs more passages through the structure to be completely absorbed. In addition, it can be seen in Figure 8.9 that J_{ph} calculated for the ideal reflector is comparable to that obtained in the case of FTO/glass substrates assuming twice longer NWs. Therefore the ideal reflector enhances the light path by a factor of 2. As H is increased, the volume of CdTe becomes larger reducing the enhancement due to the presence of the ideal reflector since light is almost entirely absorbed in the first passage.

The calculated J_{ph} map of ZnO/CdTe NW arrays with hexagonal geometrical arrangement is shown in Figure 8.8(a). It can be observed that the maximum obtained J_{ph} is slightly smaller than that calculated for the square geometrical configuration. However, a larger amount of CdTe is used in the hexagonal geometrical configuration revealing that the hexagonal geometrical configuration is much less effective. In the case of NW arrays arranged in the triangular distribution (Figure 8.8(b)), the optimum configuration result is close to that calculated in the case of the square geometrical configuration. However, the triangular geometrical configuration is denser than the square geometrical configuration.

In summary, by considering the trade-off between the amount of used volume of material and the photo-generated current density, the square geometrical configuration is more promising than both the hexagonal and triangular geometrical configurations. In addition, it is worth noting that, regardless of the configuration, optimum diameter D values are close to 200 nm while the fixed distance between NWs (P ~400 nm) in the case of the optimum geometries suggests that diffraction properties of the NW array also play a significant role on the absorption performance.

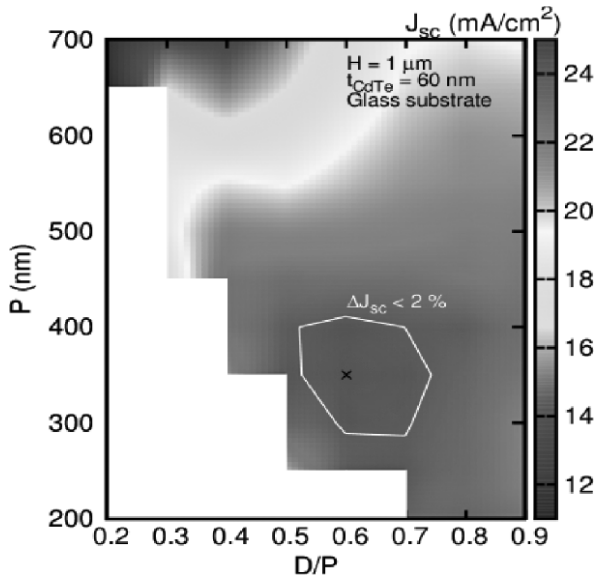

Figure 8.7. *Ideal short-circuit current density map (J_{sc}) as a function of P and D/P for the square geometrical configuration with t_{CdTe} = 60 nm and H = 1 µm. The black cross points to the optimal geometrical dimensions. The white contour shows the area in which the variations of the ideal short-circuit current density are smaller than 2%. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

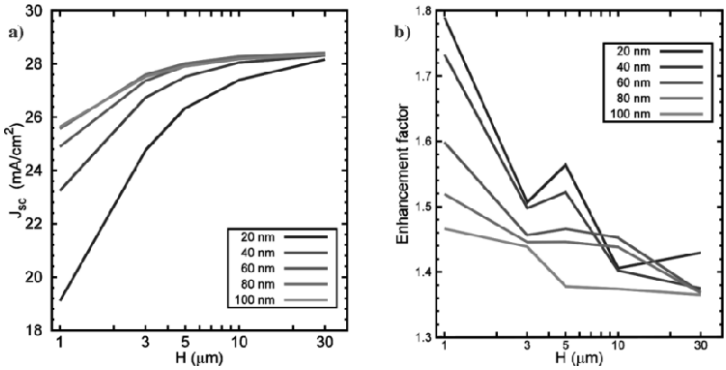

Figure 8.8. *a) Ideal short-circuit current density and b) enhancement factor as a function of H for different t_{CdTe}. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

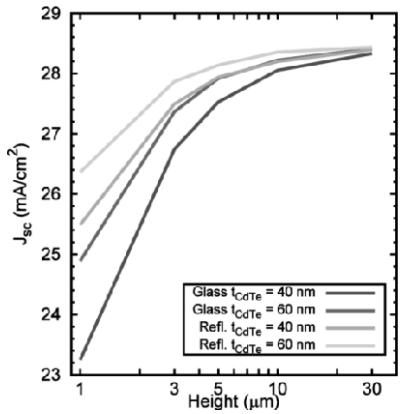

Figure 8.9. *Ideal short-circuit current density as a function of NW height for square geometrical configuration with either glass or ideal reflector substrates*

In contrast to Si NW arrays deposited on ZnO on glass substrate, ZnO/CdTe NW arrays with a lower NW compactness (lower ratio D/P) are more suitable for light absorption. Since CdTe is an efficient direct bandgap absorbing material, the optimum is not found for highly compact arrays like in the case of Si NW on ZnO on glass substrate. However, it is found for arrays exhibiting a very good anti-reflecting behavior and a good coupling between the incident light and the Bloch modes of the array. It is worth noting that, even with the small amount of CdTe considered in these simulations, the absorption is significantly higher in the case of ZnO/CdTe NW arrays than in the case of Si NW arrays.

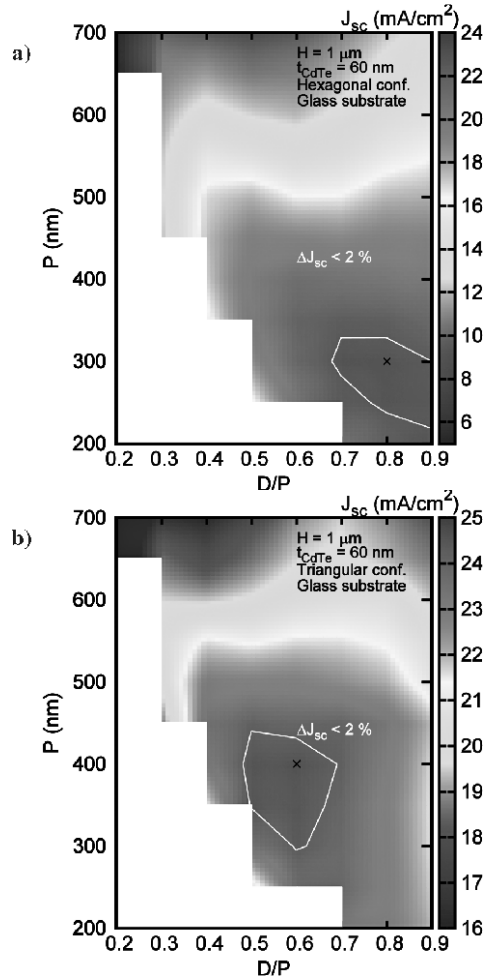

Figure 8.10. *Ideal short-circuit current density map as a function of P and D/P for the a) hexagonal and b) triangular geometrical configurations with t_{CdTe} = 60 nm and H = 1 µm. The black cross points to the optimal geometrical dimensions. The white contour shows the area in which the variations of the ideal short-circuit current density are smaller than 2%. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

8.2.2. *TCAD simulation of NW-based solar cells*

Pseudo 3D electrical simulations can be performed by exploiting the cylindrical symmetry of the structure. For that purpose, the optical generation rate calculated by RCWA on a 3D spatial grid is averaged over the azimuthal angle to perform the flattening to a 2D map [KEL 09], followed by interpolation on the device simulator

grid. The conservation of the total photo-generated carriers throughout the volume of the NW is ensured by the spatial integration of the photo-generated electron–hole pairs.

This procedure has been applied to the case of a-Si/c-Si NW based solar cells. Fermi–Dirac statistics is assumed. Losses due to Auger recombination [ALL 11], to single-level trapping Shockley–Read–Hall (SRH) recombination in c-Si, to surface recombination at AZO/silicon interfaces and at c-Si/a-Si interface as well as to trap assisted recombination in a-Si are accounted for. In a-Si, a continuous distribution of density-of-states (DOS) is adopted by assuming Gaussian mid-gap (MG) dangling bond (DB) states and exponential band-tails (BT) [LEE 09, BJE 10] (Figure 8.11). Since the device simulations are aimed at investigating the impact of recombination losses which are strongly geometry and material dependent, AZO layers have been replaced by ideal ohmic contacts with zero contact resistivity.

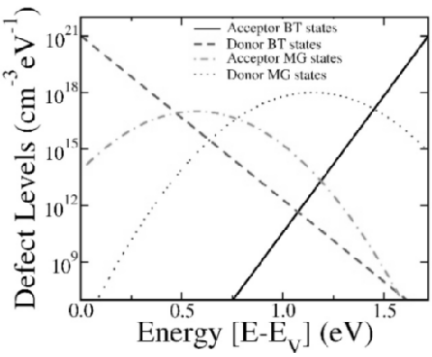

Figure 8.11. *Band-tail (BT) and Mid-gap (MG) density-of-states in n-type doped a-Si shell*

Simulations show a negligible sensitivity of the main figures of merit to the surface recombination between a-Si shell and front AZO, due to the passivation effectiveness of the heterojunction scheme (Figure 8.12). In addition, for shorter NWs the influence of the defects at the core/shell interfaces on conversion efficiency is mitigated by reducing surface area especially in the case of high defect concentration (Figure 8.13). As can been observed from Figure 8.14, the core/buffer interface defects degrade the collection efficiency of photo-generated carriers (ratio of short-circuit current to photo-generated current) characteristic over the whole spectrum, leading to a significant reduction of the short-circuit current density. However, for typical values of recombination velocity for intrinsic a-Si/c-Si interfaces reported in the literature [HER 10, KAN 09, ALL 11], the presence of the

a-Si shell is not expected to be detrimental to performance. Another critical parameter is the carrier mobility in the a-Si layers which is degraded at large doping concentrations and may potentially affect the short-circuit current density and the efficiency. From Figure 8.15 it can be observed that, if the hole mobility is in the range of 0.1—1 cm^2/Vs [FAN 99], the efficiency varies from approximately 8% to 10%.

Another drawback of amorphous materials is the presence of high defect concentration in particular in highly doped regions such as the n-type doped shell. The impact of peak concentration of mid-gap states in the doped a-Si shell (N_{DB}) on short-circuit current density is illustrated in Figure 8.16 for different NW heights. In the documented analyses N_{DB} for acceptor-like (donor-like) states ranges from 10^{17} (10^{18}) cm^{-3} eV^{-1} to 10^{20} (10^{21}) cm^{-3} eV^{-1} [PEI 09, FAN 99, BJE 10, HER 10, DIO 09, LU 11] in order to estimate the impact of doped a-Si defects on the figures of merit for realistic and worst-case situations. A relatively highly defective doped shell affects significantly the carrier collection efficiency η_c (Figure 8.14) at short wavelength values since the trap assisted electron–hole pairs annihilation mainly occurs in the NW highly doped shell, where the high energy photons are absorbed.

The calculated ultimate efficiency under the absence of recombination losses and under the assumption of relatively higher mobility for carriers in a-Si ranges from 8.64% (H = 1 μm) to 13.95% (H = 10 μm). However, when recombination losses are accounted for, the conversion efficiency ranges from 6.64% (H = 1 μm) to 9.71% (H = 10 μm).

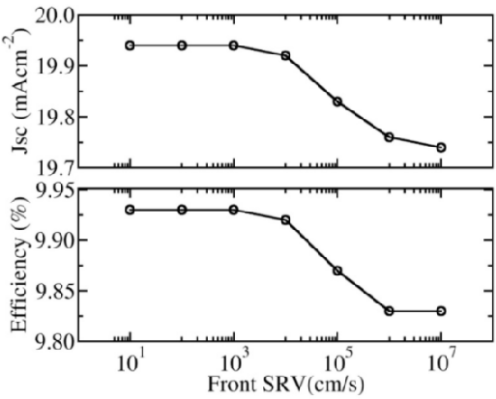

Figure 8.12. *Short-circuit current density (J_{sc}) and efficiency versus the front SRV at the shell/AZO top interface (H = 10 μm, P = 500 nm and D/P = 0.8)*

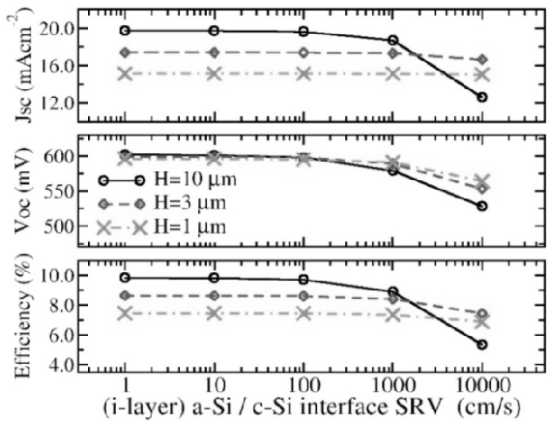

Figure 8.13. *Influence of the surface recombination velocity (SRV) (c-s) for carriers at the interface between core and shell (c-Si/a-Si). For SRVs above 1,000 cm/s the impact on the main figures of merit is significant*

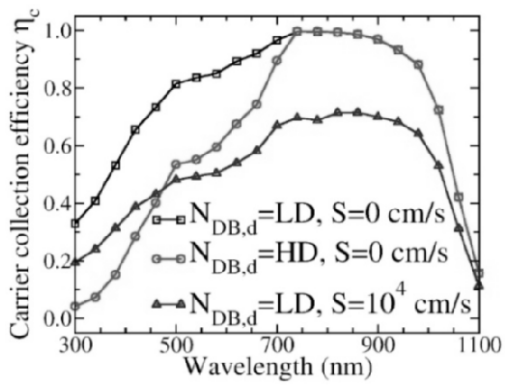

Figure 8.14. *Carrier collection efficiency for the c-Si/a-Si NW (P = 500 nm, D/P = 0.8) calculated as the ratio of carriers collected at electrodes to the amount of those photo-generated in the silicon. S denotes the SRV at the interface between the intrinsic a-Si layer and the c-Si core, while $N_{DB,d}$ denotes the Gaussian maximum density of the dangling bond donor-like states per unit of volume and energy in the n-doped a-Si layer (LD = 10^{18} cm^{-3} eV^{-1}, HD = 10^{21} cm^{-3} eV^{-1}); the maximum density of the dangling bond acceptor-like states is assumed to be one order of magnitude lower than $N_{DB,d}$. Three configurations are considered depending upon the defectiveness of the doped a-Si region and of the interface between a-Si i-layer (buffer) and the c-Si region (core)*

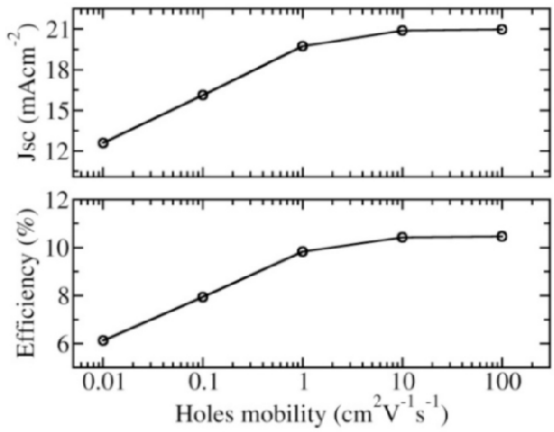

Figure 8.15. *Short-circuit current density (J_{sc}) and efficiency versus the hole band mobility in the a-Si shell (H = 10 µm, P = 500 nm and D/P = 0.8)*

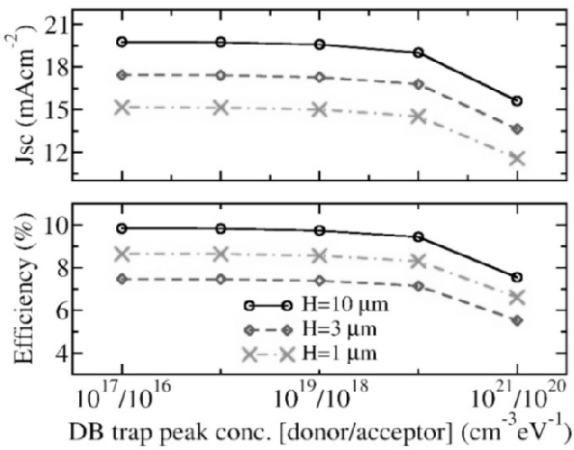

Figure 8.16. *Short-circuit current density (J_{sc}) and efficiency versus the peak density per unit volume and energy of the Gaussian distributed dangling bond (DB) states in the n-type doped a-Si shell (P = 500 nm and D/P = 0.8). The donor-like defect density is assumed to be ten times higher than that of acceptor-like states*

8.3. Fabrication and opto-electrical characterization of NW-based solar cells

8.3.1. *Elaboration of NW-based solar cells*

The experimental fabrication of cost-efficient and high quality core–shell NW arrays for compatibility with the photovoltaic industry represents a critical issue. There are two main approaches to elaborate the NW arrays: a bottom-up approach based on the growth of the NWs usually by Chemical Vapor deposition (CVD) and a top-down approach based on etching methods. For photovoltaic energy production, it is preferable to use low cost and competitive technologies. Therefore bottom–up techniques are preferable to top–down methods that consume material and increase the cost of the device.

Si NW arrays for photovoltaic applications are usually grown by CVD on top of silicon wafer, glass substrate or metal [GAR 11, KEL 10, FAN 09, TSA 07, ODO 11]. The most used technique is the vapor liquid solid (VLS) method which uses a metal catalyst to form a liquid eutectic with the desired NW material. Junction is preferably radial rather than axial for photovoltaic applications in order to increase collection probability (minority carriers only have to travel on a maximum distance corresponding to the radius of the NW). p–n junction can be formed by doping but due to the small diameter of the NW, there might be a complete doping of the NW instead of just the surface. Another way is to deposit a conformal and doped polysilicon layer on the NW. However the interface is usually highly recombinant. In order to passivate the surface of the NW and to create a junction, an interesting structure is the a-Si/c-Si heterostructure which has already demonstrated high efficiencies for first generation solar cells [TAK 11].

ZnO NWs can be grown with a wide variety of surface-scalable chemical and physical deposition techniques such as pulsed-laser deposition, vapor phase transport, CVD, metal–organic vapor phase epitaxy, chemical bath deposition (CBD) or electro-deposition [LAT 09, CON 11, SCH 07]. The radial heterojunction can then be formed by depositing CdTe with vapor phase epitaxy, close space sublimation (CSS), electro-deposition or successive ionic layer absorption and reaction [LEV 05, CON 11, WAN 10, SAL 11]. ZnO/CdTe NW array with a conformal coverage of the CdTe has been successfully grown by using CBD for ZnO growth and CSS for CdTe deposition, as shown in Figure 8.17 [CON 11]. The growth of the CdTe shell has been thoroughly investigated by scanning and transmission electron microscopy and follows the Volmer–Weber mechanisms: isolated three-dimensional (3D) islands nucleate on the NW top facet and sidewalls, subsequently coarsen and eventually coalesce to form a continuous two-dimensional (2D) layer. Until now, the interface between ZnO and CdTe has not exhibited any epitaxial relationship and the role of epitaxy in the process of light absorption and

charge carrier separation is still open. The first photovoltaic demonstrators were fabricated according to a wet chemical route with the use of an electrolyte.

Relatively low experimental efficiencies obtained up to now are mainly due to high SRV and series and shunt resistance. There are still technological improvements needed to grow high quality NWs and to reduce surface recombination.

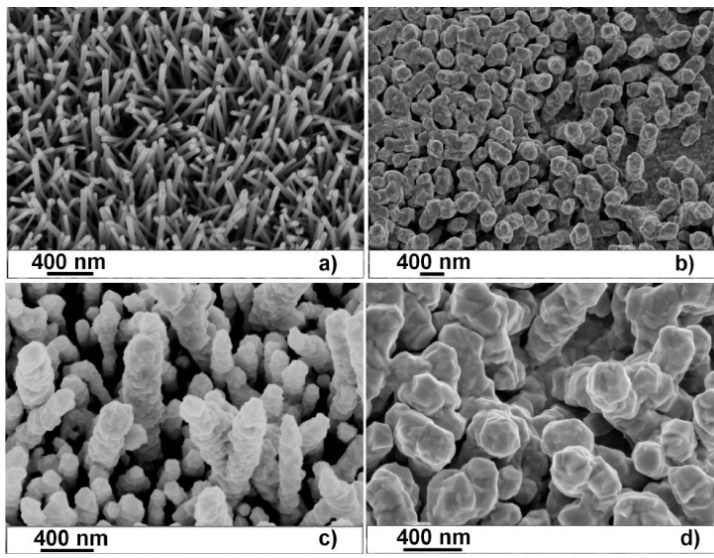

Figure 8.17. *SEM images of: (a) bare ZnO NWs; (b–d) ZnO/CdTe core/shell NWs. a) and c) are tilted views with a tilt angle of 23°; b) and d) are top views [CON 11]*

8.3.2. *Opto-electrical characterization of NW-based solar cells*

Usually, one of the main parameters permitting us to assess the quality of a solar cell is the power conversion efficiency. In order to analyze in more detail the limiting parameters, complementary experiments are necessary. In the case of NW-based solar cells, it is interesting to verify experimentally the gain in absorptance predicted by the simulations and to evaluate the influence of surface and bulk recombination. Thus, the characterization of NW arrays for photovoltaic applications should include the analysis of light absorption and carrier collection.

8.3.2.1. *Optical characterizations*

Different studies [GAR 11, KEL 10, HU 07, LI 09] of the NW arrays have shown that for a given [ALA 12] amount of material, they absorb light more

efficiently than conventional thin film solar cells. In order to check the improvement of light absorption in NW arrays and NW-based solar cells, reflectivity and transmission (when possible) measurements are usually performed on NW arrays with varying geometries and structures. A measurement setup with an integrating sphere is used to permit the measurement of diffuse and specular components of the reflectivity and/or transmission. Figure 8.18 presents a comparison of simulated and optical characterizations performed on silicon NWs etched on bulk silicon substrate. There is a correct correlation (since the peaks of the reflectivity are obtained for the same wavelengths) between experiments and simulations taking into account the fact that the NWs are not perfectly cylindrical and smooth. Moreover there might also be a small difference in refractive indexes used for the simulation.

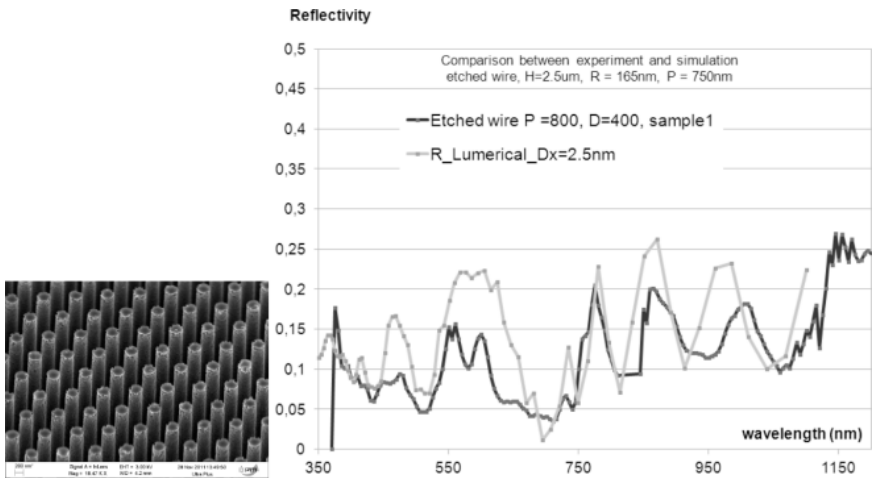

Figure 8.18. *Right: SEM view of the etched NWs. Left: comparison between experimental and simulated reflectivity of etched NWs*

Experiments and simulations have also shown that the optimum geometrical configuration in terms of NW period and diameter is in the range of a few hundred nanometers. For indirect bandgap material like Si, an increase in the NW height leads to a further increase in the optical absorption even in the case of NWs longer than 100 μm [HUA 12]. In Figure 8.19, the reflectivity obtained for NWs grown on Si wafer with different heights (constant diameter: 400 nm and pitch: 800 nm) as well as a polished silicon wafer are compared. The reflectivity of the Si NWs is significantly lower than that of the polished surface and a decrease of the reflectivity is observed when the height of the NWs increases due to a better light absorption.

Finally, measurements performed on finished solar cells permit us to confirm the results obtained on NW arrays. Figure 8.20 presents an example of measurement

done on 1 µm height Si NWs grown on Si wafer, and then on Si NWs covered with a-Si and on NW-based solar cells with a-Si and TCO. A decrease in reflectivity is observed for the final solar cell as expected by the simulation. It has to be noted that for wavelengths longer than 1050 nm, Si is transparent and the increase of reflectivity can be attributed to the highly reflective sample holder. Similar measurements done on ZnO NWs covered by CdTe (Figure 8.21) have shown the high absorptance of this structure as already demonstrated by the simulations.

8.3.2.2. *Electrical characterizations*

Concerning the electrical characterization, one important parameter for photovoltaic applications is the minority carrier lifetime or minority carrier diffusion length. This last value should be higher than the radius of the NW if we expect a good collection probability. The measured values depend on bulk recombination and on surface recombination (especially in low dimensionality structures). Therefore, usually, when measurements are performed, an "effective" value is measured. The main difficulty of these measurements is to use well-adapted techniques and models at low dimensions and lifetime NWs. On Si NWs, most of the diffusion length measurements are based on electron (EBIC: Electron beam induced current) [ALL 08] or light (LBIC: Light beam induced current) [KEL 08] beam scanning along one NW length with an axial junction or Schottky diode and on current variation measurement. To measure the lifetime of minority carriers, photoconductance decay measurements [BRY 11] and reverse recovery transient method (RRT) [JUN 11] have been also used and the extracted values are in the range of 0.3 ns–200 ns.

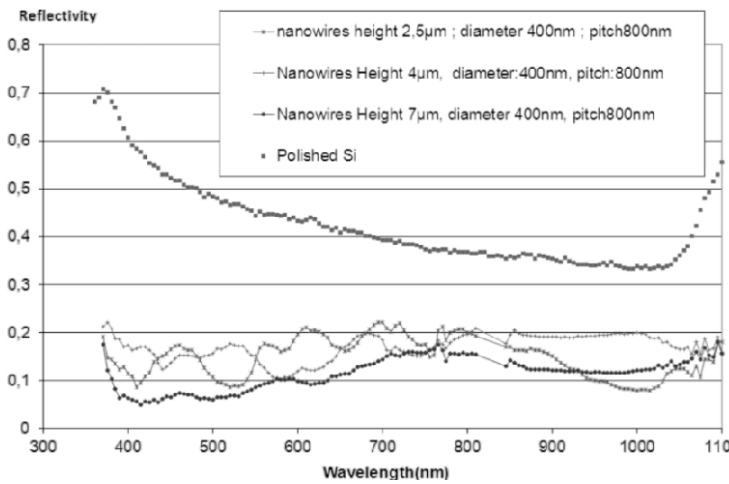

Figure 8.19. *Reflectivity of NWs with increasing height, compared with a polished Si wafer*

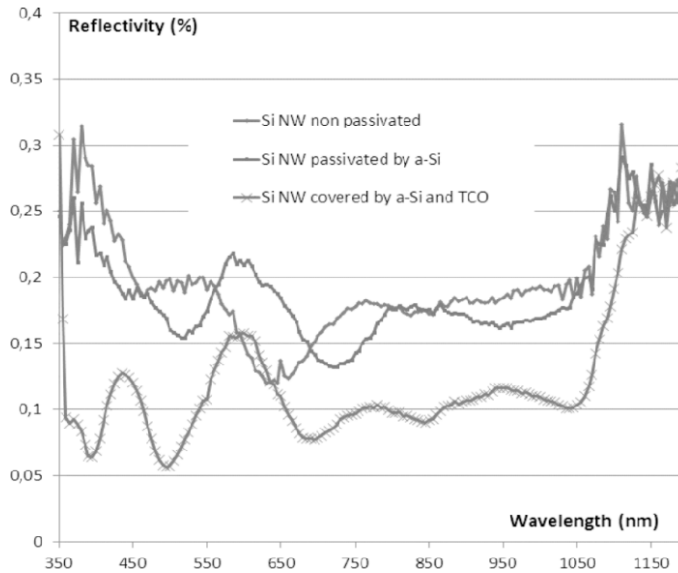

Figure 8.20. *Comparison among Si NWs, Si NWs covered with a-Si and Si NWs covered with a-Si and TCO*

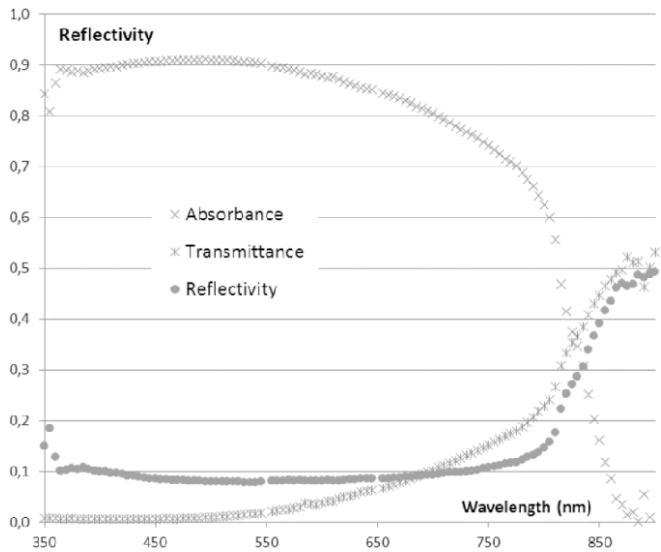

Figure 8.21. *Absorptance, transmittance and reflectivity measurements on ZnO/CdTe NWs*

An example of RRT measurement performed on a NW-based solar cell grown on Si wafer with a radial a-Si heterojunction and a TCO layer as contact is shown in Figure 8.22. The lifetime measured is 1.4 μs. This elevated value is probably taking into account the NW lifetime as well as the wafer lifetime.

In order to characterize bulk and interfacial recombination, current–voltage and capacitance spectroscopy measurement versus temperature allow obtaining complementary information to lifetime measurement. Such measurements performed on 1 μm high Si NW-based solar cells are presented in Figures 8.23 and 8.24. NW solar cells are fabricated with different types of catalyzers (C1 and C2 metals) and with a-Si/c-Si radial heterojunction. Contacts were formed with a conformal TCO layer. The advantage of this structure is to permit a good passivation of the NW's surface by a-Si and to permit the collection of the carriers due to the heterojunction [ODO 11]. The best results have been obtained on a solar cell grown on catalyst 1 showing the influence of the catalyst on the recombinations: the power conversion efficiency measured under AM1.5 conditions is about 5% (twice the one obtained with catalyst 2). The ideality factor deduced from the dark *I–V* curves (Figure 8.22) is between 1.4 and 2 and the activation energy (deduced from the Arrhenius plot) is about 0.5 eV which is close to half the crystalline Si bandgap traducing a recombination conductive mechanism. For the solar cells grown on catalyst 2, the saturation current and the ideality factor are higher than the values obtained with catalyst 1, traducing additional transport mechanisms in the structure probably induced by the metal catalyst contamination.

C–V measurements performed on the catalyst 1 sample enable us to extract the NW doping from the slope of the Mott–Schottky (Figure 8.23). The doping is equal to 5.34 × 1016 cm^{-3} at 280 K and decreases down to 3.6 × 1016 cm^{-3} at 100 K, revealing the presence of traps (with a density of Nt ~1.4 × 1016 cm^{-3}). From admittance spectroscopy, the activation energy of the trap was localized at 0.08 eV above the valence band. The capture cross-section is estimated to be 2 × 10-20 cm^2. This high density of traps might explain the limitation in power conversion efficiency.

Finally, current mapping on a-Si/c-si heterojunction performed by using a tunneling AFM (TUNA mode) can give some information on recombination locations in the device. One of the examples is Figure 8.25, where we can see that most of the current is flowing at the edges of the NWs, probably in the highly doped a-Si emitter.

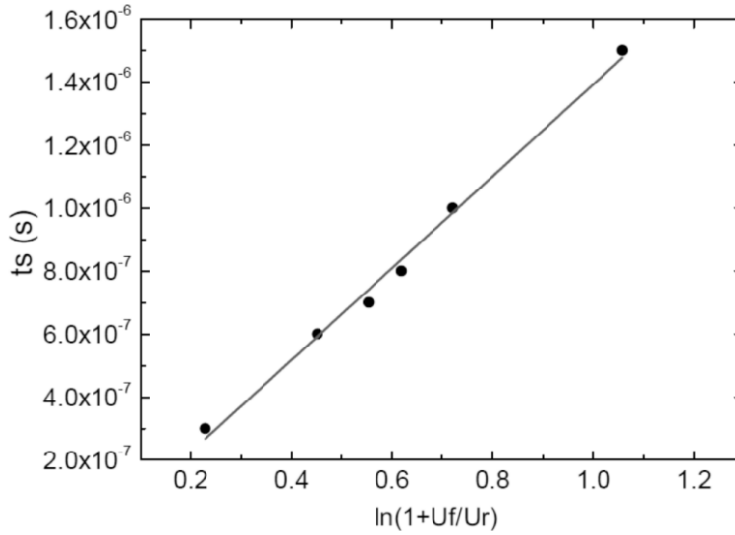

Figure 8.22. *RRT measurements performed on radial junction NW-based Si solar cells (NW ref). Uf is the forward voltage and Ur the reverse voltage; ts is the storage time. These voltage values are proportional to the corresponding current values*

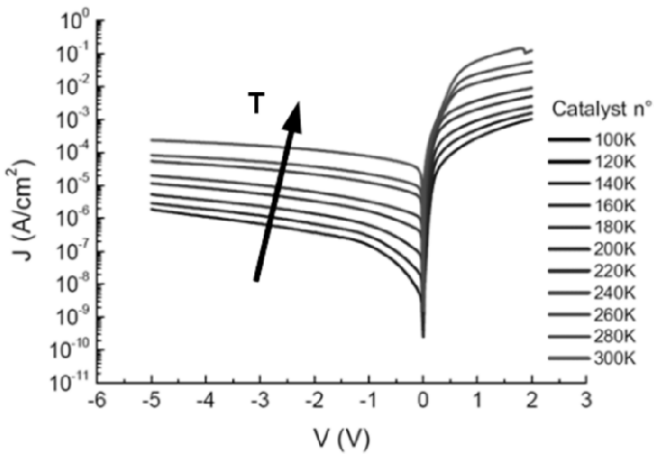

Figure 8.23. *Dark I–V–T measurements on NW-based solar cell grown on catalyst 1. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

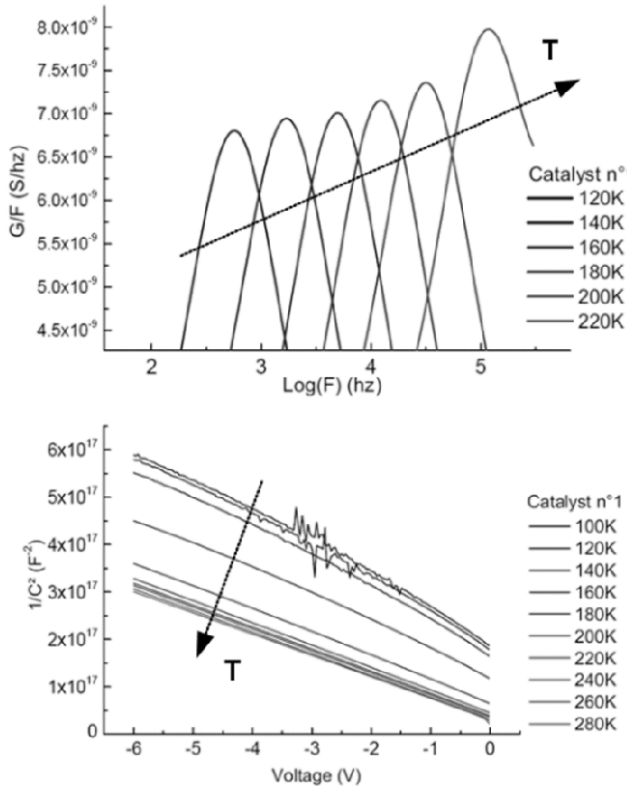

Figure 8.24. *Top: C–f–T on the same solar cell. Bottom: Mott–Schottky plot 1/C² versus V. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

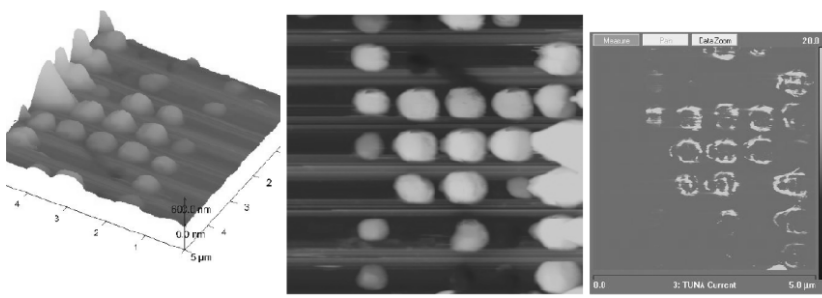

Figure 8.25. *a) and b) AFM topography image of p type Si NWs covered with n doped a-Si; c) TUNA current measured on the same NW array. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

In conclusion, the main limitations seem to be due to interface and bulk recombinations even if the bulk lifetime is high enough for carriers to reach the radial junction. Special care should be given to surfaces and interfaces between each deposition step [KAY 05].

8.4. Conclusion

Due to their ability to absorb light and to efficiently collect minority carriers, NW-based solar cells are promising structures for low cost and/or flexible photovoltaic applications. Optical and electrical simulations allow us to optimize the photovoltaic structure to reach the best efficiency and make it possible to evaluate the potential of the structure. As expected, direct bandgap materials lead to a less compact structure than indirect bandgap materials like silicon but even in this last case, absorption is significantly increased compared to a planar structure. As demonstrated by opto-electrical simulations and characterizations, special attention should be raised for the passivation of interfaces during solar cell elaboration. By improving all these aspects, very promising efficiencies have been reached on InP [WAL 13]. Other materials like ZnO NWs covered with a very thin absorber in Extremely Thin Absorber (ETA) solar cells are emerging as potential low cost candidates for photovoltaic applications. Some technological improvements are still necessary concerning these last materials but efficiencies as high as 4.74% have already been reached on these structures [XU 11].

8.5. Acknowledgments

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8.6. Bibliography

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9

Smart Energy Management and Conversion

9.1. Introduction

In the past few years, wireless sensor networks (WSN) have emerged from the research domain providing commercial solutions for many real-world applications. Currently, several WSN nodes have already been deployed in volume in commercial applications [KRI 05]. Among the anticipated applications, one of the areas of greatest potential is in Building Energy Management (BEM). By monitoring artificial lighting, temperature, CO_2 level, relative humidity, position of external shading devices and resultant actuation, a considerable percentage of energy can be saved and human comfort levels can be improved. For example, about 35% of North America's energy usage [ECM 06] and over 37% of CO_2 emissions [KIN 07] are attributed to the running of residential and commercial buildings. It has been estimated that the usage of intelligent sensor networks can result in 15–20% savings in total energy usage [GRI 04]. Due to such potential financial benefits and the political "green agenda", intensive research interests have been focused on this area [MEN 08].

Ease of deployment may enable these radio frequency-based sensor systems to replace most of the current "wired" (cable-connected) sensor systems in the foreseeable future. However, one major bottleneck for all WSN deployments has yet to be solved. This problem is the limited system lifetime due to the insufficient energy capacity of the small form factor battery power supply. For example, a WSN node designed at the Tyndall National Institute with temperature and relative

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Beyond-CMOS Nanodevices 1, First Edition. Edited by Francis Balestra.

humidity sensors [BAR 05] consumes an average of 0.25 mW when it operates on a low 0.1% duty cycle (fraction of time when sensing and transmitting occurs). Theoretically, powering from two standard 2000 mAh AA battery cells requires battery replacement approximately after every 200 days. In practice, however, the battery lifetime is even shorter due to leakage currents, temperature fluctuations, environmental humidity and other variable factors [DOY 93]. With the increasing deployment scale of nodes in WSN systems, for commercial, technical and logistical reasons, the market demands a 'deploy and forget' solution requiring the elimination of a battery replacement maintenance cycle. Energy harvesting technology could lead to this possibility of self-sustaining "infinite" lifetime motes, or at least the prolongation on the lifespan between battery replacements. This is becoming a significant focus area in WSN research in recent years because of the necessity of bridging the gap between the continuous power consumption of the WSN node and the limited available energy from the battery technology [HAY 09].

Many types of ambient energy sources are available. However, light illuminance [RAN 05], temperature gradients [DOM 09] and vibrations [ROU 05] have drawn the most attention within the research community, as a result of their relatively high technology readiness levels. For example, Table 9.1 shows the power density which has been obtained from different energy harvesting sources potentially available in BEM applications, i.e. indoor office illuminance, outdoor illuminance, human and machine vibration energy, and building thermal energy.

Energy sources	Power density
Indoor light (office 500 lux) [RAN 05]	300 $\mu W/cm^2$
Outdoor light (Standard, AM1.5)	100 mW/cm^2
Shoe insert piezoelectric [SHE 01]	300 $\mu W/cm^3$
Mechanical vibration [PER 07]	45 $\mu W/cm^3$
Thermoelectric (10^oC gradient) [ROU 03a]	15 $\mu W/cm^3$

Table 9.1. *Power density of various energy harvesting technologies*

In this chapter, power management circuits for indoor light energy harvesting, thermoelectric energy harvesting and vibration energy harvesting are introduced. The objective of power management circuit design is toward higher conversion efficiency, ultra-low power consumption and low energy storage leakage losses.

9.2. Power management solutions for energy harvesting devices

This section focuses on the design of power management circuits for energy harvesting technologies. The concept, design and implementations are introduced in detail. For thermoelectric energy harvesting, the main challenge is due to the ultra-low voltage (ULV) of the thermoelectric generator (TEG) module. ULV DC–DC converters are designed for this application. For photovoltaic energy harvesting, particularly indoor solar, the main challenge is low power maximum power point tracking (MPPT) design. For vibrational energy harvesting, the main difficulty is high efficiency AC–DC conversion. In addition to the power management circuits, the energy storage unit (ESU) is also an essential part of the system to store the energy and deliver the energy to the load.

9.2.1. *Ultra-low voltage thermoelectric energy harvesting*

Thermoelectric generators usually provide output voltages as low as tens of mV/K, with very low electrical series resistances [ROW 95]. Although thermoelectric generators with output voltages in the range of hundreds of mV/K based on microelectronic technologies are available [BOT 07], such devices also present high electrical resistances in the order of hundreds of Ω. For this reason, energy harvesting from thermal gradients generally requires handling very low input voltages, well below the threshold voltages of diodes or transistors, which prevent the use of conventional charge pumps or switching converters in order to boost the available voltage. This is essential for implementing fully autonomous and battery-less solutions, in which activating application circuits from a fully discharged state is mandatory.

At lower input voltage levels close to typical threshold levels for diodes and transistors, integrated circuit (IC) technology still enables design of charge pumps operating in a subthreshold region, such as for example in [CHE 10]. Other techniques, such as Vth-programming, as in [CHE 12], allow further reductions of the minimum activation voltage down to about 100 mV, at the expense of additional fabrication steps. In general, the minimum requirement for the input voltage is governed by the activation of an oscillator circuit, which then drives a capacitive charge pump or a switching converter. For this reason, threshold voltages of devices play an important role.

However, with input voltage in the order of tens of mV, other types of solutions are necessary. For example, in [RAM 11] a boost converter is used in order to pump up the voltage, but the switches initially require a mechanical activation for transferring energy from the thermoelectric transducer to an inductor. This

overcomes the problem of handling voltages much lower than the threshold voltage. However, a suitable mechanical excitation is not generally available in all types of solutions.

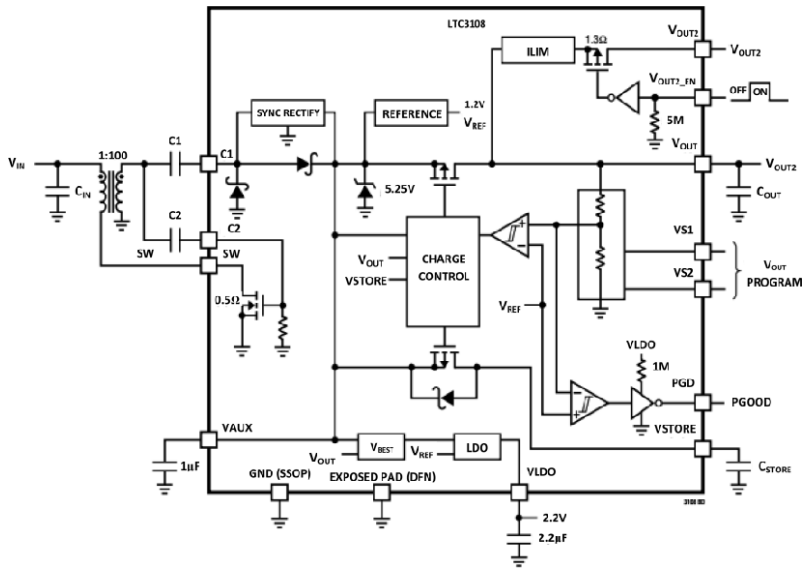

Figure 9.1. *Block diagram of the Linear Technology LTC3108 [LIN 10]*

A suitable approach for boosting very low voltages with no external energy source is the use of transformers. Such devices can be used to build up oscillators based on the Armstrong or the Meissner topologies, in which the feedback is generated by means of magnetically coupled inductors. When very low voltages are involved in this type of solution, a normally-on transistor, such as a depletion mode MOSFET or a JFET is usually required, in order to achieve a sufficient transconductance. This type of solution was proposed some time ago [DAM 97]. Recently, a very popular IC has also been developed by Linear Technologies [LIN 10] and adopts a similar topology. The LTC3108, shown in Figure 9.1, implements the above mentioned oscillator topology, and is reported to operate with input voltages as low as 20 mV. The IC also implements a complete power management system. However, the IC requires the addition of an external transformer with a turns ratio of some 10 s to one to boost the input voltage adequately, depending on the amplitude of the input voltage. This device allows current to flow from the TEG through the primary winding of the transformers, despite the very low input voltages. The excitation that propagates to the secondary winding of the transformer generates a feedback on the transistor, usually on the gate terminal, which modulates

the primary current. An oscillation is then started, and the higher number of turns on the secondary winding generates a higher voltage. At this point, a diode rectifier or even a passive voltage multiplier can be used to collect electrical charge at voltages much higher than the input. An extension of this topology was also presented in [IM 12], in which after the startup, the transformer is re-used in a more conventional switching converter, in order to improve efficiency during steady-state operation, once the circuit is started.

In this perspective, it is essential to shrink the dimension of the magnetic components in order to achieve even higher levels of integration. In-package and on-chip integration are expected to bring significant advantages. In this context, the main problem is to achieve sufficient performance and to guarantee minimum losses, both in the magnetic core and in the electrical conductors. The Nanofunction project has investigated this problem and elaborated a series of solutions. The research activity involved modeling and fabrication of new topologies of integrated micro-transformers, which are to be merged in a startup oscillator IC for a ULV harvesting solution. New topologies of micro-transformers which use bonding wires and patterned magnetic core, so called bondwire transformers [LU 10], have been designed and modeled. Since the startup converter requires high self-inductance and turns ratio to reach and maintain the oscillation, several types of magnetic cores to be mounted on-top of the micro-transformers have been investigated. Various high permeability and high saturation commercial cores are chosen and collected such as LTCC magnetic tapes, ferrite toroids and thin films. Moreover, various core shapes and thicknesses are selected and cut to minimize the footprint area of the prototypes. Since the startup converter requires low DC series resistance, various bonding wires have been modeled in terms of material, dimension and pad pitch. Bondwire transformer prototypes have also been realized on a PCB substrate with an ultrathin and ultranarrow technology.

In the design of power micro-magnetic components such as micro-inductors and micro-transformers, the choice of the magnetic structure is crucial in order to achieve high-inductance, minimize resistive losses at high frequency, and carry out the largest current available without saturating the core. The structure of micro-magnetic devices can be categorized into two main approaches which depend on the arrangements between coils and core. In the first approach the planar coils are enclosed by a multilevel magnetic core (such as spiral inductors), while in the second approach the multilevel conductors are wrapped around a planar magnetic core (such as toroidal and bondwire inductors). Generally, the main factors which characterize a good power micro-inductor are high-inductance value per unit area, low dc resistance to get high current, high Q-factor to maximize efficiency, and miniaturization capability which can be referred to as Power Supply in Package (PwrSiP) and Power Supply on Chip (PwrSoC) [MAT 12].

Frequency	Material	Deposition	Good	Bad
Low frequency (fop <1 MHz)	Soft ferrites (NiZn, MnZn)	Screen printing (IC not compatible)	↑ ρc, ↑ tc	↓ Bs, ↓ μrc, ↑ Hc
High frequency (fop >5 MHz)	Metallic thin films (NiFe, NiFeMo)	Sputtering, Electroplating (IC compatible)	↑ Bs, ↓ Hc, ↑ μrc	↓ ρc, ↓ tc
Very high frequency (fop >100 MHz)	Laminated metallic thin films nanocomposites	Sputtering, Electroplating (IC compatible)	↑ Bs, ↓ Hc	↓ ρc, ↓ tc

Table 9.2. *Summary of integrated soft magnetic materials used for power micro-magnetic components*

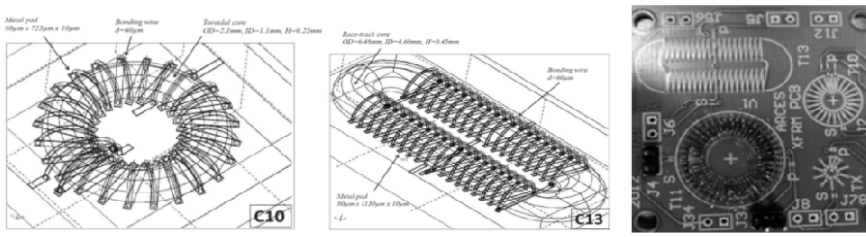

Figure 9.2. *Prototypes of bonding wire transformers developed in the Nanofunction project. Toroidal (left) and race-track (centre) topologies have been developed, and tested on a PCB prototype (right)*

The choice of the magnetic material is also shown to be essential. The main characteristics which define the performance of soft magnetic materials are: high resistivity, low coercivity, high saturation flux density, high relative permeability, high anisotropy field, and low core losses. High resistivity ρc (Ω·m) leads to low eddy current effects in the core which represents a dissipative loss of energy within the core and defines the maximum operation frequency fop (Hz). Furthermore, a high resistivity material has an increased skin depth δc (m) which ensures that the magnetic field intensity is constant with the film thickness tc (m). Low coercivity Hc (Oe) minimizes hysteresis loss at high frequencies, while high saturation flux density B_s (T) enhances current-handling capability. In order to get stable performance, the core should have high relative permeability μrc constant for high frequencies, and high anisotropy field H_k which increases the operation frequency and current-handling ability. The core losses are mainly composed of two different contributions: eddy current losses and hysteresis losses. Low core losses require soft magnetic materials with high resistivity and low coercivity field. Table 9.2.

shows a summary of integrated soft magnetic materials used for power devices.

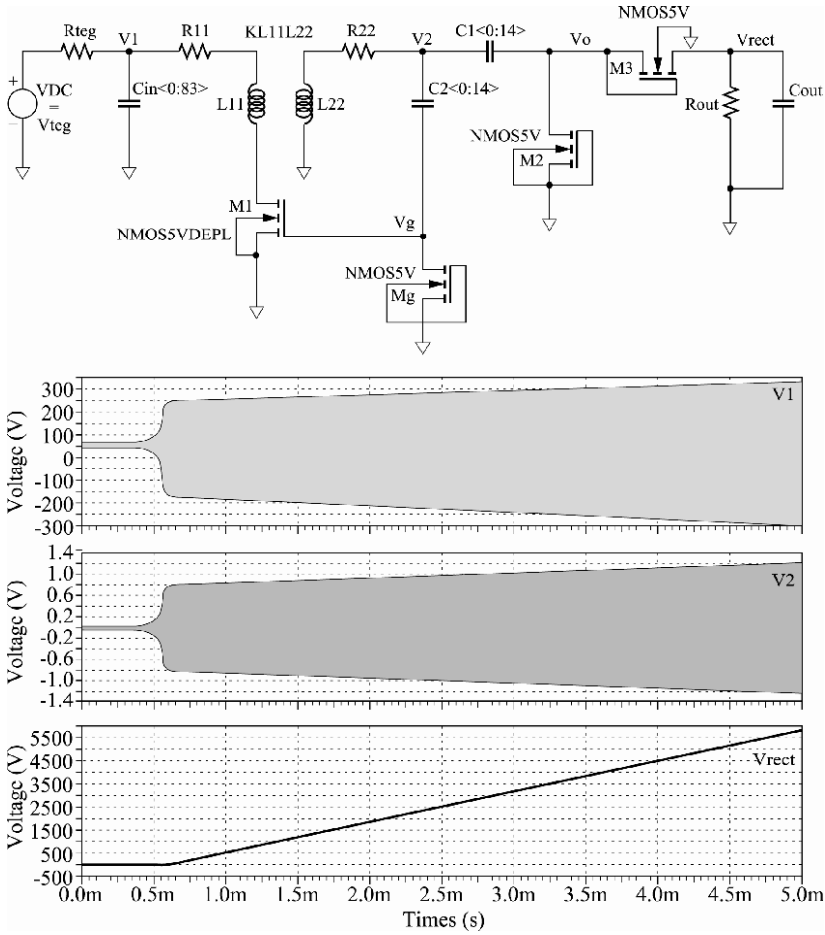

Figure 9.3. *Main oscillator topology with output rectifier (top). Circuit simulations of proposed converter and bonding wire transformer with n = 36.5. Steady-state response of primary voltage V1 (top graph), secondary voltage V2 (middle graph), and rectified output voltage Vrect (bottom graph) with Vteg = 40 mV, Rteg = 430 mΩ, Cout = 10 nF, Rout = 100 MΩ, single M1 and two parallel C1*

Among the developed prototypes, interesting results have been found. A toroidal transformer with a 4.95 × 4.95 mm^2 surface area enables turn ratios up to 1:38 using

gold conductors 80 µm wide. Figure 9.2 shows preliminary prototypes, based on two types of geometry. All the developed technologies, besides PCB implementations, are suitable for on-chip or in-package assembly. In order to validate system design, an IC implementing the schematic reported in Figure 9.3 was designed and fabricated. The proposed IC, suitable for operation with the above bondwire transformers, is based on a Meissner oscillator topology, as explained previously. Simulation results show that the proposed integrated solution, based on a CMOS IC and on the proposed micro-transformer, ensures circuit startup and a sufficient output voltage allowing above threshold operation of a conventional boost converter. The solution is compatible with on-chip or in-package assembly and is expected to provide performance comparable to external miniaturized magnetic components, thus yielding a higher level of integration in electronic design.

9.2.2. *Sub-1mW photovoltaic energy harvesting*

High accuracy MPPT circuits for large scale PV cells often consume over 100 mW of power, several orders of magnitude higher than the harvested power in the small PV cell, which is obviously not suitable for this application [KOU 01]. Several methods have been proposed to perform low power MPPT. Simjee and Chou proposed a PFM controller based fractional open circuit voltage (FVOC) MPPT method utilizing a buck converter structure. This MPPT operates above 80% at 20 mW solar power [SIM 08]. Dondi *et al.* introduced a PWM controller based FVOC MPPT with a similar buck converter structure and achieved up to 85% efficiency when PV cell generated 50 mW [DON 08]. Brunelli *et al.* suggested that it is possible to obtain MPPT power consumption around 1 mW with the FVOC MPPT method with optimized frequency and components selection [BRU 09a]. These work, although significantly enhancing the MPPT performance in lower power conditions, but still exceed the sub-mW PV cell output power. Brunelli suggests that due to the power consumption in the MPPT, for a small solar cell it is impractical to use the MPPT to improve conversion efficiency, and alternative methods should be adopted [BRU 09b]. Tan and Panda proposed a MPPT solution for wind energy harvesting using a boost converter structure to perform impedance matching through resistance emulator method [TAN 11]. This method shows the potential to further reduce the power consumption of MPPT theoretically into the sub-mW scale by adopting a low duty cycle ultra-low power micro-controller but was not verified by Tan and Panda due to difference in applications. Both [SIM 08] and [TAN 11] need a micro-controller to generate MPPT control signal, which obviously increases the system cost and complexity. Chini and Rovati introduced a PFM controlled boost converter similar to the design shown in this work with component selection for ultra-low power level, however, without synchronous rectification MPPT [CHI 10].

	Chini and Rovati [CHI 10]	Simjee and Chou [SIM 08]	Tan and Panda [TAN 11]	Simjee and Chou [SIM 06]	Dondi *et al.* [DON 08]
Converter	Boost	Buck	Boost	Buck	Buck
Control logic	PFM Control	PFM Control	PWM Control	PFM Control	PWM Control
Input power	1.6 mW	5 mW	9.36 mW	10 mW	50 mW
Efficiency	30%	47%	84%	45%	85%

Table 9.3. *Comparison of MPPT efficiency in lowest useable power level*

Table 9.3 shows a comparison of efficiency among various maximum power point tracking circuits at various power levels. A system architecture of the indoor PV cell-powered WSN node is presented in Figure 9.4. This proposes that the power autonomous system consists of five building blocks: (1) photovoltaic cells; (2) MPPT tracker; (3) ESUs; (4) output stage voltage regulator and; (5) wireless sensor node. By adopting this system architecture, both the input power and output power are optimized to ensure delivery of the maximum amount of useable energy to the WSN node. The multiple stage regulation reduces the energy conversion efficiency, a trade-off exists in the power losses and power gains in the power regulations. The main power losses in the system are illustrated in Figure 9.5. The power (voltage) level of the ESU is monitored by the WSN node in order to update the network on the remaining energy in each module. The power monitoring readings and power management simulations can provide an effective means to predict the system operation.

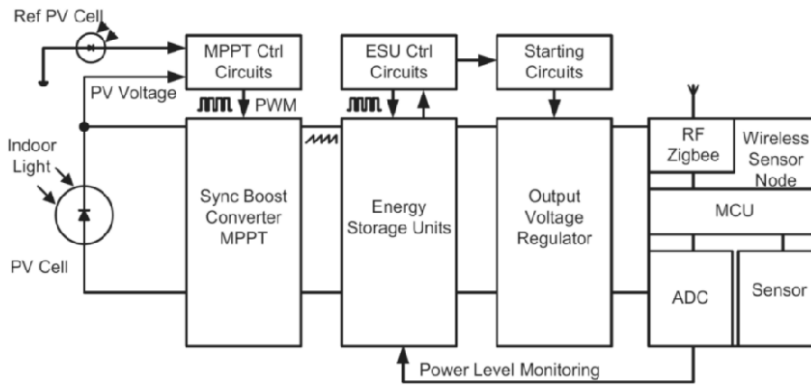

Figure 9.4. *Indoor light energy harvesting wireless sensor node*

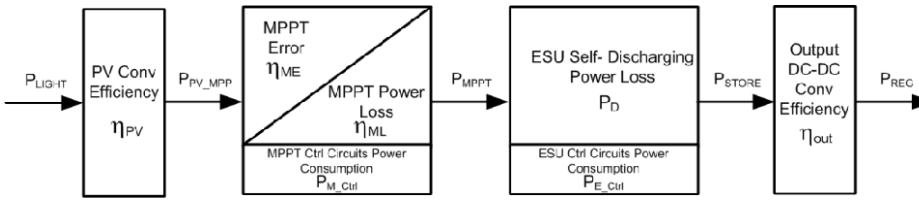

Figure 9.5. *Efficiency losses and power consumptions in the proposed energy harvester*

The indoor light power P_{Light} is harvested by the commercial off the shelf (COTS) amorphous silicon photovoltaic cell with a conversion efficiency at η_{PV}. The MPPT circuits adjust the control signal frequency based on lighting intensity to approach a near optimal voltage on the PV cell, thus approaching the ideal maximum power of PV cell P_{PV_MPP}.

A certain amount of power is lost due to the imprecision of MPPT; the efficiency loss due to the MPPT error is η_{ME} as shown in Figure 9.5. Inevitable efficiency losses in the MPPT procedure and the power consumption of the MPPT control circuits are expressed as η_{ML} and P_{M_Ctrl}. The output power of MPPT is expressed as P_{MPPT}. Based on input voltage and remaining energy in the ESU, the ESU control circuits choose to charge/discharge the hybrid energy storage. In both charging and discharge processes, a self-discharge power loss exists as P_D. Similar to the MPPT control circuit's power consumption, the ESU control circuit also has a power consumption P_{E_Ctrl}. The power transferred from ESU P_{STORE} is further optimized in the output voltage regulator, with an efficiency η_{out}, before connecting to the WSN node. The boost converter based output voltage regulator can be automatically started up by the ESU control circuits in case of power failure and the subsequent need to restart the system.

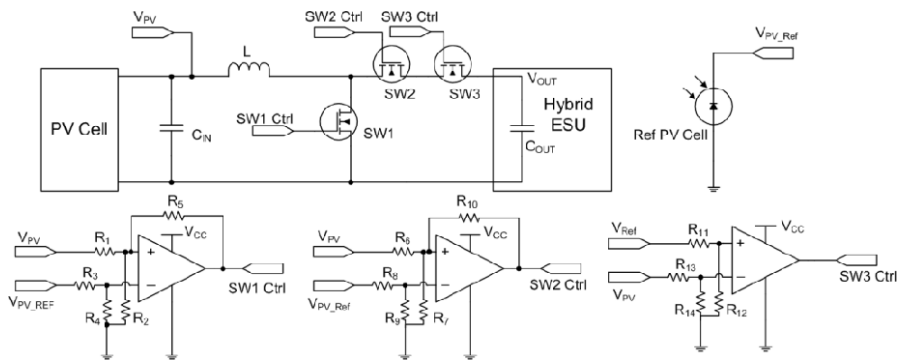

Figure 9.6. *Conceptual schematics of maximum power point tracking*

The schematic presentation of the synchronous boost converter based MPPT is shown in Figure 9.6. The MPPT consists of two main building blocks: (1) comparator-based MPPT controller and; (2) synchronous boost converter. The boost converter is controlled by PWM signals generated from the ultra-low power comparators. A secondary PV cell is used to obtain a reference open circuit voltage to set the theoretical V_{MPP}. Made from the same photovoltaic technology as the main PV cell, the pilot PV cell obtains an open circuit voltage V_{oc_ref} proportional to the main PV cell open circuit voltage. Hysteresis is adopted in the design to switch on transistor SW1 when input capacitor voltage (PV cell voltage) is higher than $V_{MPP} + V_{hyst1}$. The input capacitor is then discharged whilst the inductor L is charged with variable current $iL(t)$. Once the capacitor voltage drops to $V_{MPP} - V_{hyst1}$, the SW1 is turned off due to the hysteresis, the "ON" state time is t_0–t_1 as shown in Figure 9.7.

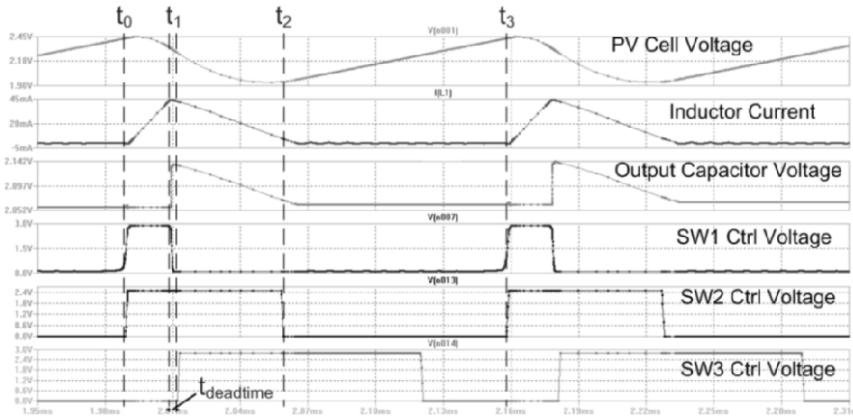

Figure 9.7. *Converter simulation and control signals of SW1, SW2 and SW3*

The average V_{mppt} is at 0.773 of the measured open circuit voltage. The average MPPT error is less than 1.8% of the ideal MPP ratio 0.760. The employment of the MPPT circuits achieves a 27% power increase when 500 lux illuminance is applied. It can be concluded that with an ultra-low power design of the maximum power point tracker, the MPPT can improve the power conversion efficiency. However, a considerable percentage of power loss is attributed to the MPP tracker. For low illuminance light energy harvesting, the power loss offsets most of the power gained from MPPT. The ultra-low current consumption of the MPPT subsystem enables the prototype to increase the power harvested from the PV cells by 30% in a 500 lux lighting condition. The carefully simulated and successfully implemented design consumes less than 50 μW power. The conversion efficiency with 0.5 mW input power is 81%.

9.2.3. *Piezoelectric and micro-electromagnetic energy harvesting*

Vibrations are widely diffused and common in several environments, for example, to name but a few, human and goods transportation or industrial machinery. Piezoelectric transducers can achieve high power density [ROU 03b] and several techniques [ROM 10a, LEF 06, ROM 08, DAL 08] have been developed in the past years to improve the effectiveness of the energy extraction process.

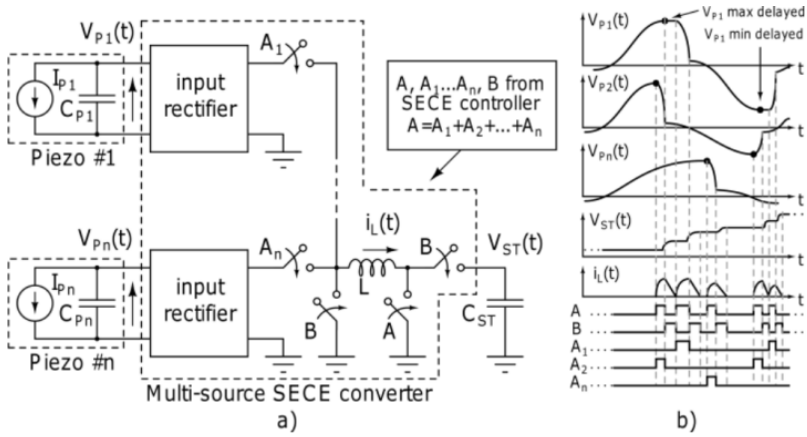

Figure 9.8. *a) Block diagram of a multi-source SECE converter for piezoelectric transducers, b) qualitative waveforms under ideal conditions [DIN 13]*

Converters based on the synchronous electrical charge extraction (SECE) scheme (Figure 9.8(a)) have proven to be more efficient than other passive interfaces (e.g. diode full bridge) and enable extraction of energy without any constraint between input voltage $V_P(t)$ and output voltage $V_{ST}(t)$. Moreover, harvesting energy from multiple piezoelectric transducers is a viable solution in order to increase input power [ROM 10b]: each extraction cycle lasts a small fraction of the repetition period (i.e. the vibration frequency) so a single shared inductor can be exploited to extract energy from several transducers (Figure 9.8(b)). Simultaneous requests to access the shared inductor can be handled delaying all the requests but one.

Figure 9.9 shows the top-level schematic of a multi-source converter suitable for piezoelectric energy harvesting [DIN 13]. Each transducer is connected to its input stage which rectifies the input voltage $V_{P1...5}(t)$ throughout an enhanced version of a Negative Voltage Converter (eNVC, Figure 9.10(a)) and then detects, with a peak detector, when the transducer voltage has reached a maximum, in order to trigger the start of an energy extraction cycle. The eNVC output is a rectified version of input voltage without forcing a way for current flow. Furthermore the n-channel

MOSFETs MA1-MB2 allow the complete discharge of CP, thus an increment of available energy for each energy extraction. Important features for an energy harvesting converter are the energetic autonomy and capability to start and operate from a no-energy state (i.e. V_{ST} = 0 V): a passive path (D1–D5) and Mdepletion in Figure 9.9 has been implemented to allow self-startup. Such a path is then disabled when the output voltage reaches a minimum level to guarantee correct operations of all circuits (V_{ST} > 1.4 V). The logic controller has been designed with asynchronous logic in order to avoid energy waste due to clock generation and manages the issues related to inductor sharing. In addition, the logic controller determines the correct timing for each conversion phase, based on the information provided by the voltage and current zero crossing circuits (ZCV and ZCC, respectively) included in the SECE core (Figure 9.9). Moreover, the SECE core embodies the power MOSFETs and their gate drivers together with a dynamic biasing circuit to further reduce the quiescent current drawn by the circuit.

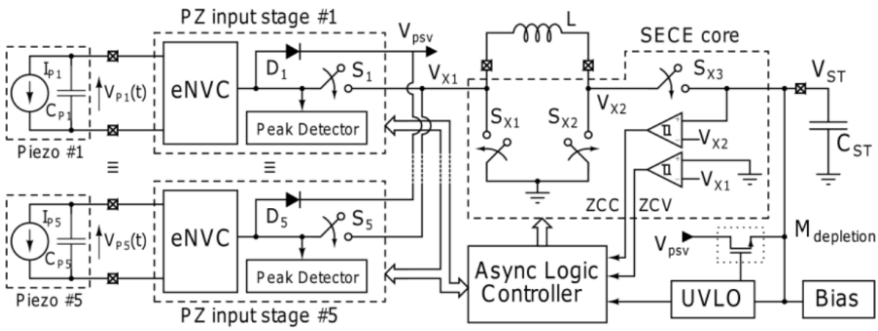

Figure 9.9. *Top-level schematic of a multi-source converter for energy harvesting from independent piezoelectric transducers [DOY 93]*

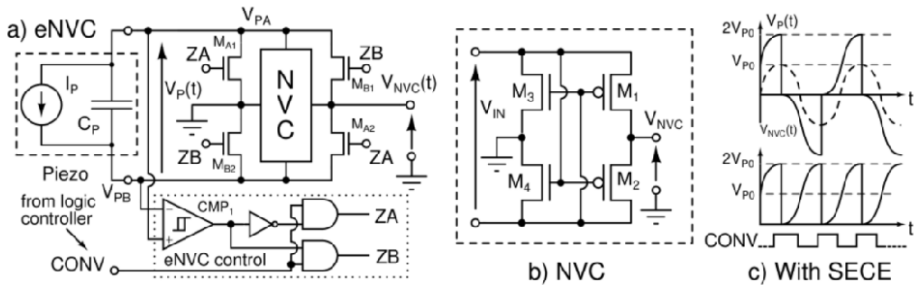

Figure 9.10. *a) eNVC and its driver circuit, b) standard NVC, (c) qualitative waveforms of input, output and control signal of the eNVC [DIN 13]*

The nano-power IC [DIN 13] designed for energy harvesting from multiple independent piezoelectric transducers reaches an efficiency that ranges from 70% to over 85%, including its own power consumption.

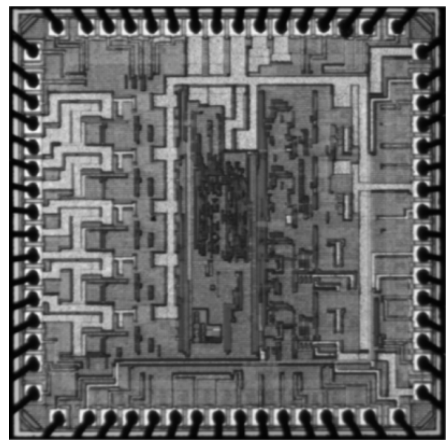

Figure 9.11. *Die photograph of the designed IC*

Due to nano-power design and energy aware techniques, the converter consumes a very low amount of energy both during the extraction process and in the time between extractions. The quiescent power is as low as 175 nW per source at V_{ST} = 2.5 V, leading to an overall quiescent power of 875 nW for handling five piezoelectric transducers. The IC, manufactured in a 0.32 μm BCD technology, has an area of 4.6 mm^2 and the die photograph is shown in Figure 9.11.

9.2.4. *DC/DC power management for future micro-generator*

In this section, we study power management units to supply next-generation ultra-low-power micro-controllers from future micro-generators for applications such as WSN or the Internet of Things.

Such applications require energy autonomous operation to avoid battery replacement and the micro-controller must therefore consume the lowest power possible at moderate computing power. For these reasons such future micro-controllers will be supplied at ULV (0.3–0.5 V) [BOL 13a]. Thus, there is a need for dedicated power management units to generate such ULVs with good conversion efficiency and voltage regulation. Furthermore, these power management

units must use as few external components as possible in order to reduce the system volume, the carbon footprint for its production [BOL 13b] and the assembly costs.

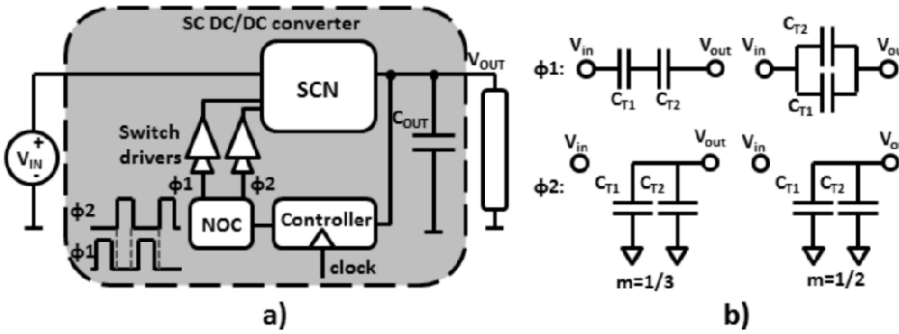

Figure 9.12. *a) Architecture of an SC DC/DC converter, b) examples of switched-capacitor network (SCN) with V_{out}/V_{in} conversion ratios of 1/3 and 1/2 at no load*

There are two main families of circuits able to deliver this ULV. Firstly, linear regulators dissipate energy in a passive component such as a resistor. Unfortunately the conversion efficiency is limited to the ratio between output and input voltage $V_{\text{out}}/V_{\text{in}}$. Secondly, switching converters use switches and inductors or capacitors to convert an input voltage to an output voltage. Inductive switching converters are well known but cannot easily be integrated on-chip and lack efficiency when supplying a low-power load [BEL 10]. Switched-capacitor (SC) DC/DC converters can be fully integrated on-chip due to the process features of mixed-signal CMOS technologies, and their efficiency remains high at low loads [PIQ 12, VAN 12]. Figure 9.12(a) shows a typical architecture of such a converter. A switched-capacitor network (SCN) performs the voltage conversion between input and output voltages by oscillating between two phases Φ1 and Φ2. Regulation of the output voltage is performed due to a controller that senses V_{out}. Control signals for the actuation of power switches are sent to a block generating non-overlapping clocks (NOC) which ensures that the switches that are ON during the first phase Φ1 are never activated at the same time as the switches that are ON during the second phase Φ2 which would result in unwanted short circuit currents. Gate drivers distribute the control signals from the NOC to the gate of the large power switches while keeping short rise and fall times. Finally an optional output filtering capacitor C_{out} reduces the voltage ripple on V_{out} due to the SCN switching. Figure 9.12(b) shows two examples of SCN with a $V_{\text{out}}/V_{\text{in}}$ conversion ratio of 1/3 and 1/2 at no load. This ratio can be obtained by inspection of the SCN configurations during the two phases Φ1 and Φ2

of the switching cycle. The power P_{out} that is delivered by such converters to the load is:

$$P_{out} = \alpha f_{sw}(V_{nl} - V_{out})V_{out}, \quad [9.1]$$

where α depends on the SCN topology, f_{sw} is the converter switching frequency, and V_{nl} is the converter output voltage at no load.

ULV digital circuits such as micro-controllers suffer from high sensitivity to process, voltage and temperature (PVT) variations [DEV 12]. Therefore they require a large voltage guard band on their supply voltage to ensure that no timing error occurs in the circuit critical paths in the worst-case PVT corner, which increases their power consumption. An adaptive voltage scaling (AVS) system using an SC DC/DC converter can be used to (1) provide efficiently the ULV for the digital circuit, while (2) being fully integrated on chip next to the load and while (3) cancelling the voltage guard band due to PVT variations [DEV 12]. Instead of delivering a constant V_{DD} to the circuit, the AVS adapts V_{DD} to ensure that the critical path delay is just below the cycle time of the micro-controller clock (f_{CLK}). The AVS thus compensates the actual PVT corner and avoids the V_{DD} guard band for worst-case PVT variation. The architecture of such an AVS system is shown in Figure 9.13. An SC DC/DC converter is used for the voltage conversion. The other blocks of the AVS system are fully digital. A PVT sensor made of a replica of the micro-controller critical path senses its maximal operating frequency under the actual PVT corner. It is also used to provide its clock signal to the load. The external inputs to the AVS system are the battery voltage (V_{BAT}), the value of the micro-controller target frequency (f_{TARGET}) as a digital code and an external low-frequency crystal clock as a reference.

During the high phase of the crystal clock, the frequency comparator counts the number of rising edges of the clock generated by the sensor and clock generation unit. On the falling edge of the crystal clock, the difference between the count result and f_{TARGET} is sent to the regulator. It decides if the circuit clock frequency f_{CLK} must be increased or decreased, to regulate the converter output voltage. It generates control signals which are sent to the decoder that converts them into signals compatible with the DC/DC converter driver. As stated in equation [9.1] the conversion ratio of SC DC/DC converters for a fixed P_{out} depends on the converter switching frequency. For a given P_{out}, the supplied voltage can thus be tuned by controlling the switching frequency of the SC DC/DC converter. The decoder signals control the block generating the converter clock to select its switching frequency. The converter output voltage supplies both the micro-controller and the PVT sensor and clock generation block. When V_{DD} varies, f_{CLK} is automatically adjusted, as the critical path replica (CPR) ring oscillator frequency is dependent on its supply voltage.

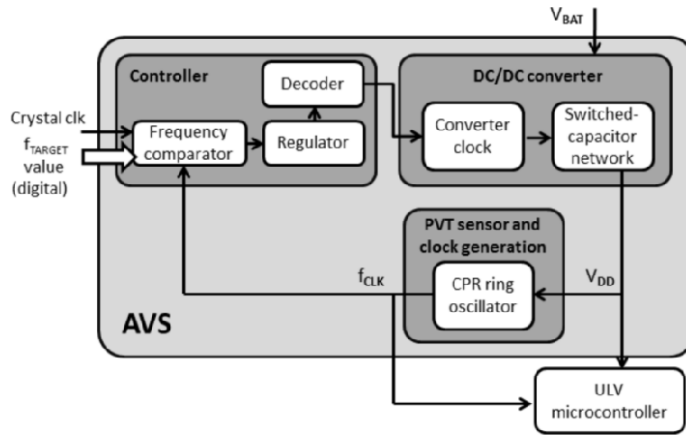

Figure 9.13. *Block diagram of the proposed adaptive voltage scaling system from [DEV 12]. A SC DC/DC converter is used for the voltage conversion, the PVT sensor and clock generation block is built with the same critical path replica (CPR) ring oscillator*

Figure 9.14 shows the transient behavior of such an AVS systems designed to supply the 0.4 V SleepWalker micro-controller SoC described in [BOL 13a]. The startup procedure is first illustrated: the micro-controller is in sleep mode (V_{DD} = 0 V with inactive DC/DC converter) and a wake-up request occurs. The clock of the DC/DC converter starts and it sends charges to a 3.3 nF C_{out}.

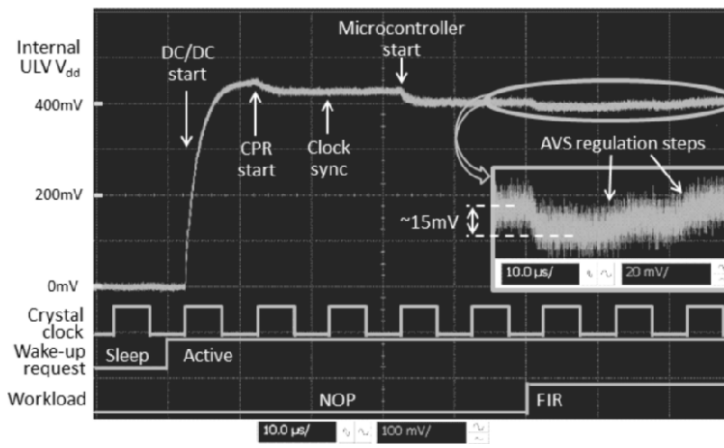

Figure 9.14. *Measured transient behavior of the voltage supplied by the adaptive voltage scaling systems used in [BOL 13a] at startup and for a steep workload change: the micro-controller goes from performing NOP operations to FIR looping*

At this stage, the current consumption of the ULV micro-controller is limited to leakage through the devices. Therefore the AVS output voltage (internal V_{DD}) rises close to the no-load voltage of the SC DC/DC converter, i.e. 500 mV. After one period of the crystal clock, the CPR ring oscillator is started and switching power is consumed, resulting in a small drop of the internal V_{DD}. The generated clock is then synchronized with the crystal clock and the operation of the micro-controller is finally started. The AVS loop starts regulating the micro-controller frequency at this stage. Figure 9.14 also shows the AVS loop response to a steep workload increase from NOP operations to FIR looping. When the workload changes, the internal V_{DD} only falls by 15 mV before going back to target 0.4 V.

9.3. Sub-mW energy storage solutions

There is currently a concerted international research effort to bridge the gap between energy demand and supply to enable truly autonomous wireless devices. This requires an increase in both the storage capacity of batteries and the efficiency of energy harvesting devices coupled with a decreased demand from the electronics. Ideally this would be manifest as device integrated energy storage that interfaces with energy harvesting components, provides power on demand to the electronic sensing, communication and display components and operates over the anticipated device lifetime. Ultimately the energy storage solution should occupy a footprint on chip no larger than the electronics it drives, with 1 mm^2 as an attractive long-term target for both. No such energy storage component exists today. Batteries are the most common energy storage option and since their introduction in the 1990s lithium ion batteries have exhibited the highest energy density which has been gradually improved in the intervening period from ~200 Wh/l to ~700 Wh/l through the use of improved materials and processing.

Solid state microbatteries which can be processed on Si have achieved similar volumetric energy densities with μm scale thin film materials in large area format, offering capacity retention over thousands of cycles [DUD 05]. In the 2D, thin film geometry, current deposition techniques and lithium ion diffusion limits the electrode thickness to several micrometers resulting in a battery dominated by the substrate and other inactive cell components. As thin films these 2D formats typically exhibit energy densities of ~60 $\mu Wh/mm^2$ or 0.2 J/mm^2. An energy budget of 1 mWh/day can support a WSN node used in BEM, with sensing and transmission every 20 min [OMA 08]. Clearly significant advances are required for energy storage devices to meet the demand in a reasonable footprint. The key challenges are to realize improved energy storage in a significantly decreased footprint for Si integration and high rate (power) capability during device interrogation and to decrease recharge time. These challenges require:

– Higher energy density materials, particularly at the cathode, where the current material, $LiCoO_2$, is 25 times less energy dense than lithium metal.

– 3D or 1D active materials structuring with increased aspect ratio providing additional material (stored energy) with respect to planar commercial thin film microbatteries.

– Nanoscale active materials with improved electronic conductivity or core/shell structures [HAS 10] to facilitate high rate solid state lithium ion transport.

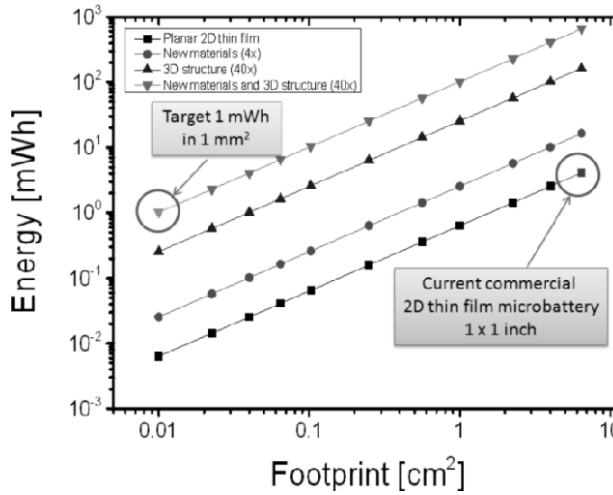

Figure 9.15. *A roadmap for microbattery energy storage requiring the development and integration of new materials which could yield up to 4 times improvement in stored energy and micro-or nanoarchitectures to increase the material quantity and surface area to deliver 1 mWh of energy in a 1 mm² footprint*

The need for more energy dense materials and structured electrodes is illustrated in Figure 9.15, where the target of 1 mWh of energy required for a building management WSN node currently has a 6.5 cm^2 footprint. In addition, current solid state microbatteries cannot meet the needs of the ICT systems at peak power during measurement and transceiver operation and require a hybrid energy source. This is due to the lithium diffusion limitation in the solid state electrolyte and cathode. On the other hand the solid state construction does facilitate the use of lithium metal anodes which have a large energy capacity by comparison with the typical carbon anodes (372 mAh/g) of most lithium ion batteries. If non-solid state electrolytes are

to be utilized then alternative high energy intercalation anodes such as Sn [WHI 99] (990 mAh/g), Ge [LAF 08] (1600 mAh/g) or Si [CHA 08] (4200 mAh/g) will be required to prevent dendritic short circuits on cycling. Core/shell [CUI 08] versions of these anodes may be required to alleviate mechanical stresses leading to poor cycling behavior and improving the electronic conductivity to access all of the high aspect ratio structures.

In the Nanofunction project, nanoscale materials have been investigated as a means to improve the energy storage and current delivery issues for both anodes and cathodes. Previous research had investigated Cu_6Sn_5 nanowires [ROH 11] (Theoretical capacity 605 mAh/g) as potential anodes for a lithium ion microbattery. In this work a Sn rich alloy (Theoretical capacity 830 mAh/g) was investigated to improve the capacity while still delivering an anode that can be structured on Si substrates in nanowire format and permit the use of polymer gel electrolytes to increase rate capability. The $CuSn_3$ nanowires achieved are shown below and representative voltammograms for approximately 6 µm long and 200 nm diameter nanowires are shown in Figure 9.16(a). Initial capacities of 740 mAh/g were recorded for the nanowires with a slow decrease on cycling as shown in Figure 9.16.(b). The lithium insertion (5 mA) and removal (3 mA) currents for these nanowires also indicate high rate capability.

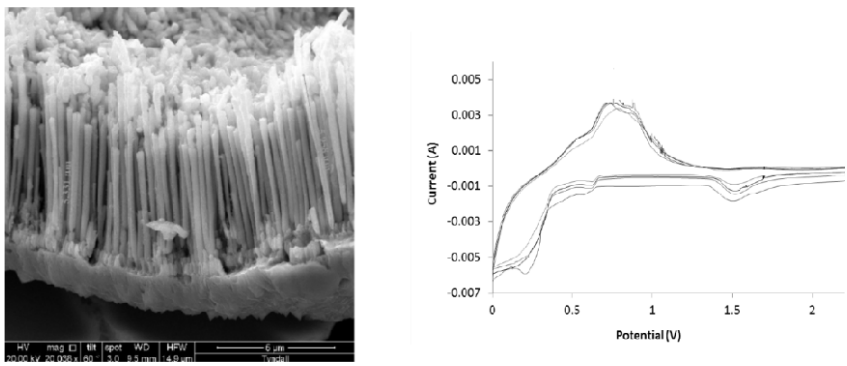

Figure 9.16. *$CuSn_3$ nanowires fabricated in an AAO template and cyclic voltammetry data for the nanowires*

MnO_2 as an alternative battery cathode to the standard $LiCoO_2$ material is desirable to eliminate the use of the more toxic heavy metal Co of the standard lithium battery and to decrease cost. To integrate the MnO_2 as a battery material required the use of Cu nanotube base supports, also formed in AAO by a method described previously [CHO 09] onto which the MnO_2 was deposited. This led to aligned MnO_2 nanowires anchored in the Cu supports as shown in Figure 9.17

forming a well adhered interface. The nanowires are 18 μm long and this aspect ratio of 90 (for 100 nm radius nanowires) results in an active surface area more than 100 times that of the planar footprint. The data for the 18 μm MnO_2 nanowires on Cu supports is shown in Figure 9.17. In the first cycle for the nanowires an improvement is observed for the peak position and rate capability of the lithium insertion and extraction with respect to micron scale MnO_2 material. The influence of the copper support is seen, however, at the more positive potentials and the electrode did not function as expected after the imposition of a high positive potential. Support materials more stable at the high positive potential required.

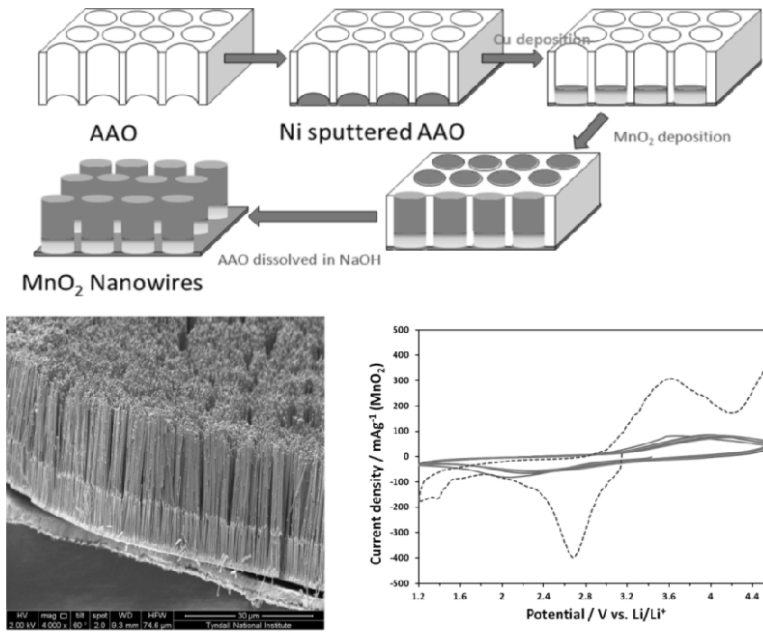

Figure 9.17. *a) MnO_2 nanowire fabrication route and b) adhered nanowires on Cu nanosupport. c) Li insertion and removal from MnO_2. The solid curves are cycles for <5 μm MnO_2 particles (Aldrich) dispersed on carbon. The dashed line is for the MnO_2 nanowires anchored on Cu*

Despite the gradual improvement, there is still a large gap between the energy density of typical cathodes in lithium ion batteries and those of lithium metal or alternative high energy anodes. Disruptive battery technologies such as a Li/sulfur or Li/air [ABR 96, BRU 11] can achieve the energy storage requirements of the ICT community. A theoretical energy density of 2.8 mWh/mm^3 (10 J/mm^3) has been estimated for a Li–air battery [ZHE 08] with non-aqueous electrolytes. It is recognized that the Li/air and other high energy systems have to overcome many

obstacles before they will be in widespread deployment but many researchers predict that this could be over the next ten to fifteen years. A very challenging scaling requirement has been shown in Figure 9.15, and that must be coupled with decreased power requirements in the ultimate device. An increasing focus on improved nanoarchitectures, electrode materials and integrated current collectors is required to surmount these obstacles and deliver high energy density solutions to meet the needs of the electronics industry.

9.4. Conclusions

This chapter introduced power management circuits and energy storage unit designs for sub-1mW low power energy harvesting technologies. This work has proposed three different types of power management circuit for the most frequently used energy harvesting technologies: thermo-electric, photovoltaic and vibrational energy harvesters. The solutions address several of the problems associated with energy harvesting, power management and storage issues including low voltage operation, self-start, efficiency (conversion efficiency as well as impact of power consumption of the power management circuit itself), energy density and leakage current levels. Additionally, efforts to miniaturize and integrate magnetic parts as well as integrate discrete circuits onto silicon are outlined to offer improvements in cost, size and efficiency. Finally initial results from efforts to improve energy density of storage devices using nanomaterials are introduced.

For thermo-electric energy harvesting, a transformer based ULV ultra-low power (sub-1mW) DC–DC conversion circuit has been proposed. It adopts a novel bonding wire transformer structure with several types of ferrite/metal material. The bonding wire transformer has been successfully developed in this project for system miniaturization. The implemented transformer obtains a turn ratio up to 1:38. In addition to the PCB implementation of the converter, this technique is also proposed to be utilized in standard CMOS process.

Ultra-low power maximum power point tracking has been developed in this project for sub-1mW indoor solar cells. The fractional open circuit voltage method is proposed in this work for simple and low power control circuits. The implementation of this MMPT method utilizes nanowatt level comparator logics instead of complicated DSP logics in order to further reduce the power consumption of the MPPT. A power loss simulation model is created to optimize the component selections. The module consumes less than 50 μW when the input power is less than 1 mW, whilst the end-to-end conversion efficiency of the MPPT circuit is >79.6% with 0.5 mW input power.

For vibration energy harvesting, a "nano-power" IC has been designed in a 0.32 μm STMicroelectronics BCD technology that can manage up to 5 AC–DC channels (e.g. piezoelectric transducers). The IC implements a boost converter based on SECE and it can be adapted to cover a wide input voltage range. For input voltage of 2.5 V, a peak efficiency of 85% is achieved in the AC–DC conversion.

An ultra-low supply voltage (<0.5 V) micro-controller has been designed in the framework of this project. A DC–DC converter for a future ULV micro-controller has been developed in this application. This DC–DC converter steps down the 1.2 V energy harvested power to 0.4 V supply voltage. The converter is manufactured using 65 nm standard CMOS process along with the micro-controller. The maximum conversion efficiency in room temperature is approximately 80%.

In terms of energy storage, nanoscale materials have been investigated as a means to improve the storage density and current delivery issues for both anodes and cathodes. Initial capacities of 740 mAh/g were recorded for the nanowires with a slow decrease on cycling. The lithium insertion (5 mA) and removal (3 mA) currents for these nanowires also indicate high rate capability. Nanowires 18 μm long were developed with an aspect ratio of 90 (for 100 nm radius nanowires) providing an active surface area more than 100 times that of the planar footprint.

Finally, these efforts have highlighted the importance of system level methodologies in optimizing the overall integrated solution rather than optimizing sub-elements in isolation. The benefits of collaboration in Nanofunction have also been clearly illustrated in terms of collaborative testing, specification definition, combining expertise in fabricating miniaturized parts and the synergizing of circuit elements from various project partners into next generation high miniaturized efficiency, low leakage multi-source energy harvesting and power management solutions.

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PART 3
On-chip Electronic Cooling

10

Tunnel Junction Electronic Coolers

10.1. Introduction and motivation

Currently, the only practical way to reach very low temperatures (mK regime) is to use large, massive cryostats and consume huge amounts of energy. By contrast, cooling just the active devices or, even better, just the electrons in a device requires far less energy, produces less waste heat to remove and can occur much faster. The aim of this work is to develop electronic cooling in complementary metal–oxide semiconductor (CMOS)-compatible nanoscale systems, with an emphasis on integrating the processes of cooling and the active purpose of the system, e.g. radiation sensing by a detector. This opens up a whole new scenario of integrated cooling and electronics that we have called "cooltronics". Such CMOS-based electronic cooling could have a widespread impact on future applications: the ease of implementation, through mass production silicon electronic technology, will extend access to really low temperatures for both existing applications and new ideas that will inevitably be developed once a simple cooling technology is made available. Extension to the nanoscale promises further functionality.

In some cases, the electron population can effectively be thermally decoupled from the host material. Then, only the electrons themselves need to be cooled to the lowest temperatures and not the lattice, which typically has a much higher heat capacity and so would require more energy to cool. This is particularly true for semiconductors, where the number density of electrons is many orders of magnitude lower than in metals, and will be discussed at greater length in Chapter 11. A thermally isolated, electronically cooled sensor's sensitivity and response rates can be dramatically increased in such a scenario. Applications already envisaged include single photon counting sensors, which can only operate efficiently at extremely low

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temperatures where they have higher gain and suffer less from electrical noise. Such self-cooled sensors would bring huge benefits in terms of sensitivity, cost and mission longevity to satellite-borne astrophysical applications. Their use in fluorescent light detection in biological assay analysis promises a revolution in medical and biological fields, particularly in disease detection, drug development and understanding of cell function.

The growing interest in quantum devices for sensing applications, and in the longer term for quantum information processing, also requires electrons to be cooled below 100 mK. However, in this case the quantum state of the electrons would be affected by being directly attached to the refrigeration elements and so an indirect cooling method is required. To ensure good thermal and electrical isolation from the outside world, the active devices are mounted on a membrane which is itself cooled by electronic refrigeration elements. Similarly, other payloads could be mounted on such a cooled membrane platform, with relevance for high sensitivity and low noise sensing and detection. There is particular interest in this technology for satellite-borne detectors where the reduction in mass and bulk of the cooling systems are key design aims to enable satellites to be launched with smaller vehicles. The absence of moving parts and indefinite hold time are also attractive for long-term missions. Optimizing the design of such systems requires knowledge of electron-phonon coupling and phonon dynamics in nanoscale structures, which will be addressed in Chapter 12.

10.1.1. *Existing cryogenic technology*

Typically, a cryostat will use liquid helium (He) to cool the system to about 1.4 K, brought below the 4.2 K boiling point of helium-4 at atmospheric pressure by pumping to reduce the vapor pressure. Then a second stage will use helium-3 as the refrigerant to reduce the temperature to just below 300 mK. For temperatures below this, it has been necessary to use a mixture of He-3 and He-4 in a dilution refrigerator, with temperature in the few mK regions being reachable with the most advanced systems. In recent years, there have been rapid advances in mechanical coolers, such that the “wet” cryogenics of the first He-4 stage can be replaced by a “dry” system. By using multistage pulse tube coolers, temperatures below 2 K can be achieved that can then be coupled to a further stage having a small dilution refrigeration unit to go to the mK regime. However, being a mechanical system, there is a certain amount of vibration, both from moving parts and from the continual expansion and contraction of the refrigerant gases, which can have amplitudes of a few micrometers at the cooled sample/sensor position. Furthermore, the dwindling ready supply of helium-3 emphasizes the importance of having a replacement for the whole dilution refrigerator technology.

An alternative approach is provided by adiabatic demagnetization where temperatures can be reduced from the base reached by a pulse-tube cooler into the mK region. By using sufficiently high magnetic fields (up to 10 T), temperatures below 100 mK can be accessed with a two-stage demagnetization. Disadvantages of this technology arise from the difficulty of screening the cooled region from the very high magnetic fields used and the fact that cooling is a single-shot operation with a limited time before recharging is required, although in commercial systems this has been reduced to times in order of the one hour.

By contrast, electronic refrigeration requires much lower powers, since only the active volume is being cooled, can operate for an unlimited period or can be switched on/off rapidly. The technology is still in its infancy, so this chapter will introduce the basic ideas of tunnel junctions as coolers and outline the issues that have to be addressed for an optimized system. The remainder of Part 3 will review progress made, within the Nanofunction project and elsewhere, in semiconductor-based cooling elements, nanostructured (yet robust) membranes and integrated refrigeration and detection elements. These will contribute to creating devices that require much lower power consumption to reach low temperatures than is currently possible.

10.2. Tunneling junctions as coolers

10.2.1. *The NIS junction*

The energy diagram of a normal metal-insulator-superconductor (NIS) tunnel junction is shown in Figure 10.1. Its behavior is analogous to a high pass filter; a current flows through the junction extracting only high energy (hot) electrons from the normal metal, for certain bias voltages. If the heat loads entering the electron gas by other means (mainly from the lattice) are sufficiently low, the cooling power of the tunnel current will reduce the electron temperature.

For a superconductor with an energy gap of 2Δ, Figure 10.2(a) shows that without an applied bias only very hot electrons with energies $E–E_{FN} > \Delta$ can enter the superconductor. This sets a first limit on a tunnel junction cooler with a particular superconductor to operate from a bath temperature T_b below Δ/k_B. Applying a bias, as in Figure 10.2(b) allows hot electrons with energies $E–E_{FN} > \Delta - eV$ to tunnel into the empty states above the superconducting energy gap. As the bias approaches $V = \Delta/e$ this will mean all electrons with energies above the Fermi energy in the metal can be extracted. By contrast, cold electrons ($E < E_{FN}$) are blocked by the energy gap in the superconductor. Each electron removes energy ($E–eV$), which is of order k_BT, from the metal corresponding to a cooling power of order $I\,k_BT/e$, where I is the current through the junction [NAH 94, FIS 99]. The

reduction in average electron energy corresponds to a lowering of the electron temperature, as seen in the tightening of the Fermi function shown in Figure 10.3. The maximum cooling power occurs for voltages closely approaching V = Δ/e. For V > Δ/e (Figure 10.2(c)), cold electrons are also extracted from the normal metal and the tunneling results in a net negative cooling power i.e. a heat load which, at high bias, is equivalent to Joule heating. Hence, the choice of superconducting material and its energy gap determines the range of bias voltages that can be applied and ultimately the temperatures over which the electronic cooler can operate.

The current flowing through an NIS junction for low temperatures is shown in Figure 10.4, where it acts as a refrigeration element, compared to room temperature. The low temperature tunnel current is ideally zero for $V < \Delta/e$, where tunneling is not allowed, then increases sharply at $V = \Delta/e$ after which the current asymptotically approaches the room temperature value given by $I = V/R_T$, where R_T is the characteristic, or normal state, resistance of the tunnel junction. The appearance of such a nonlinear IV curve demonstrates that a device is functioning as a tunnel junction and the extent of the zero current region can give an indication of its effectiveness as a cooling element.

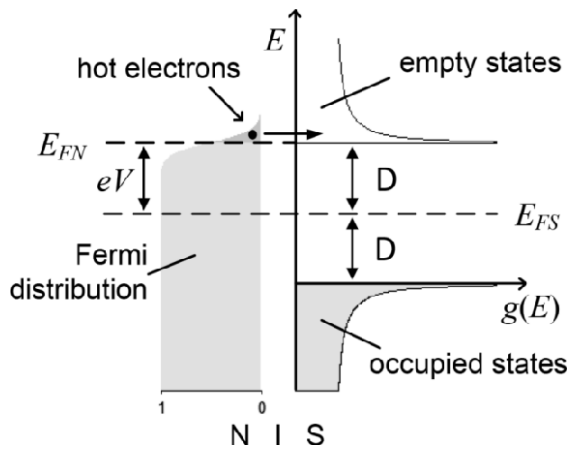

Figure 10.1. *The energy-level diagram of an NIS junction. The superconductor has an energy bandgap of 2Δ. A bias voltage, V=Δ/e, is applied across the junction, so that only electrons with energy greater than E_{FN} are allowed to tunnel through the insulator into the superconductor*

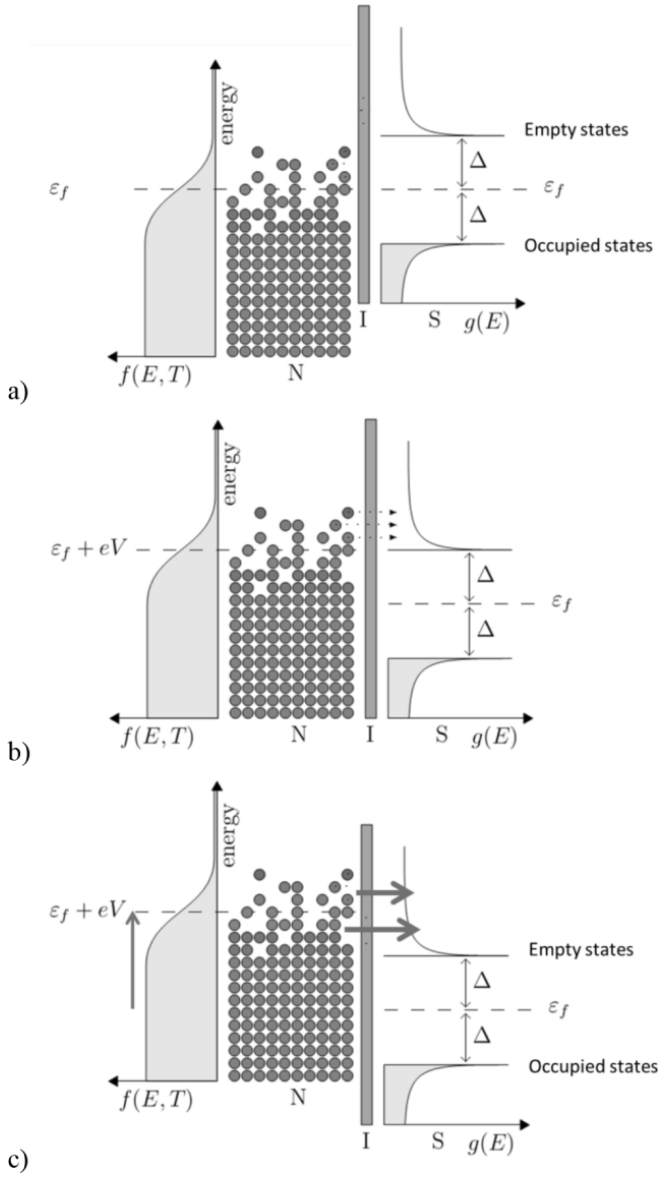

Figure 10.2. *The band alignment in an NIS junction under different bias conditions*: *a) zero-bias, no tunneling possible*; *b) optimal bias eV = Δ allows hot electrons to be extracted*; *c) excess bias eV > Δ also extracts cooler electrons*, *so no net cooling, but heating due to flow of larger current. (The spread of the Fermi distribution is exaggerated and should be much less than Δ). For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

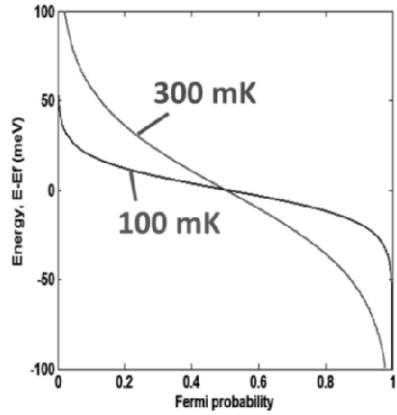

Figure 10.3. *Comparison of the Fermi function* $F(E,T) = \frac{1}{1+e^{(E-E_F)/kT}}$ *(the probability of a state of particular energy being occupied) at 300 mK and 100 mK, showing how reducing the numbers of electrons in the tails of the distribution leads to a lower temperature*

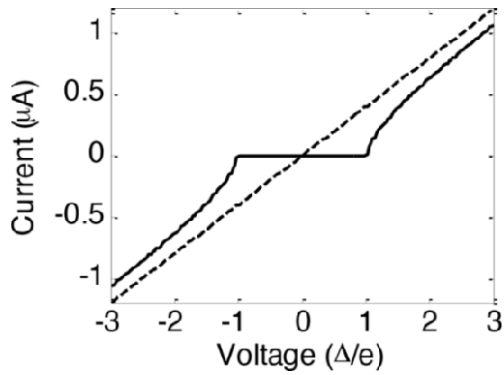

Figure 10.4. *I-V characteristic of the junction at low temperature (solid line) and room temperature (dashed line). The curves are calculated using equations [10.1] to [10.8] with the parameters:* $\Delta = 0.2$ *meV,* $R_T = 500\ \Omega$, $\Sigma = 10\ WK^{-5}m^{-3}$, $\Omega = 1\ \mu m^3$

10.2.2. *Cooling power*

The cooling power of an NIS junction arises from the current of high-energy electrons leaving the metal, each carrying its energy ($E-eV$) out of the system [NAH 94, JUG 99, LUU 00]. This current is given by equation [10.1] [ROW 76, NAH 94, BAR 95, LEI 96, FRA 97]

$$I = \frac{1}{e\ R_T}\int_{-\infty}^{\infty} F(E,\ V, T_e, T_b)\ \ g(E)\ \ dE\ . \qquad [10.1]$$

where $F(E,\ V, T_e, T_b) = f(E - eV, T_e) - f(E, T_b)$ [10.2]

and $f(E,T) = 1/\left[1 + \exp\left(E/\left(k_B T\right)\right)\right]$ [10.3]

Here, R_T is the normal state tunneling resistance, $f(E,T)$ is the Fermi–Dirac distribution function of electrons, T_e is the electron temperature in the normal metal and T_b is the temperature of the superconductor, assumed to be equal to the temperature of the thermal bath; $g(E)$ is the density of states within the superconductor, given by the Dynes formula [DYN 84, PEK 04]

$$g(E,\Gamma) = \left| \ \mathrm{Re}\left[\frac{E + i\Gamma}{\sqrt{\left(E + i\Gamma\right)^2 - \Delta^2}}\right] \right| \qquad [10.4]$$

where Γ is the density of states broadening factor. This current removes energy from the semiconductor at a rate [LEI 96]

$$P_{cool} = \frac{1}{e^2\ R_T}\int_{-\infty}^{\infty} (E - eV)\, F(V, T_e, T_b)\, g(E)\, dE\ . \qquad [10.5]$$

The maximum cooling power at any temperature is a function of the superconductor energy gap and the tunnel resistance and can be shown to be approximately:

$$P_{cool}\left(\max\right) = \frac{0.6}{e^2\ R_T}\sqrt{\Delta}\left(k_B T_e\right)^{3/2}\ . \qquad [10.6]$$

Electron-phonon coupling results in a heat flow between the electron gas and the lattice as the former is cooled, given by [WEL 94, ROU 85]

$$P_{e-ph} = \Sigma\ \ \Omega\ \ \left(T_e^n - T_b^n\right) \qquad [10.7]$$

where Σ is the material-specific electron-phonon coupling constant, Ω is the volume of the absorber, and T_e and T_b are the electron and phonon temperatures, respectively. The power n varies with the material of the island, and usually for normal metals n = 5 (see [KIV 03]). In the simplest case, assuming that the phonons

are at a fixed bath temperature, we may calculate the temperature up to which the electrons are cooled by finding the solution to equation [10.8]:

$$P_{cool} + P_{e-ph} = 0 \,. \qquad [10.8]$$

Figure 10.5 shows a graphical solution to equation [10.8] starting from three different bath temperatures (colored lines) of 300 mK, 400 mK and 500 mK. The bath temperature determines the amount of phonon heating $P_{e\text{-}ph}$ from equation [10.7]. The black line represents the junction maximum cooling power P_{cool} and their intersection is the minimum attainable temperature, in the absence of parasitic heat leaks or Joule heating. In this example, a particularly low tunneling resistance of 10 Ω has been used; higher tunnel resistances would decrease the junction cooling power in accordance with equation [10.6]. It should also be clear from equation [10.7] that the lattice heating would be reduced through having weaker electron-phonon coupling and by using a smaller junction volume, although that may also lead to a higher tunnel resistance.

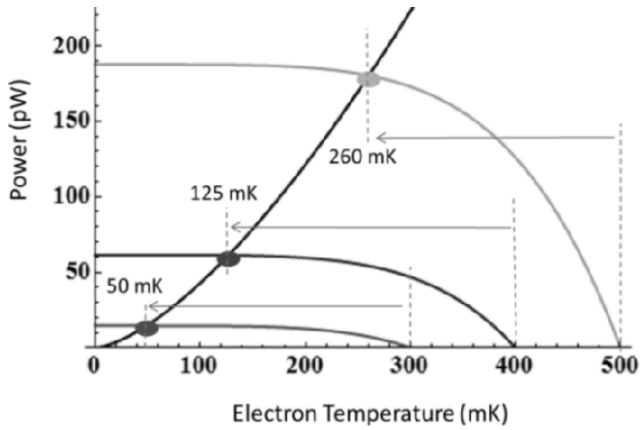

Figure 10.5. *Maximum cooling power of the junction as a function of electron temperature (black line) and phonon heating power for bath temperatures of 300 mK, 400 mK and 500 mK. Points of intersection show the minimum electron temperature that can be reached for each bath temperature. The curves are calculated using equations [10.1]–[10.7] with the parameters:* $\Delta = 0.2$ *meV,* $R_T = 10\ \Omega$, $\Sigma = 10^9\ WK^{-5}m^{-3}$, $\Omega = 6\ \mu m^3$. *For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

10.2.3. *Thermometry*

Small NIS probe junctions are also used to measure temperature; the small area increases the tunnel resistance, so that the cooling power of the junction is kept

small. If $k_B T_e << \Delta$ and $0 << eV < \Delta$, the current through an NIS junction, by thermally activated tunneling, is [LUU 00]

$$I(V) \approx I_a \exp\left[\left(eV - \Delta\right)/k_B T_e\right]. \quad [10.9]$$

So that if the junction is biased with a constant current, typically in the pA range, the voltage across the junction can be used as a measure of temperature following:

$$\frac{dV}{dT_e} \approx \left(k_B/e\right) ln\left(I/I_a\right). \quad [10.10]$$

Hence, the thermometer voltage has a suitably linear dependence on temperature. However, in real devices there is often a deviation in this linear dependence at the lowest temperatures [NAH 94]. This requires additional calibration, which can be achieved by comparing with the junction's electrical characteristics measured in a dilution refrigerator at a known bath temperature.

10.2.4. *The superconductor-insulator-normal metal-insulator-superconductor (SINIS) structure*

The cooling power of an NIS device can be doubled by using back-to-back junctions in a SINIS structure (Figure 10.6). The potential V is divided evenly between the two junctions that have equal tunnel resistance R_T. Electric current flows from right to left. Hot electrons tunnel out of the normal metal (or semiconductor) being cooled at the right-hand junction and are replaced by cold electrons, which enter at the left-hand junction. In this way, the Fermi distribution is being "tightened" from both the high and low energy sides and hence the electrons are cooled more efficiently. A factor of 2 can be included in equations [10.2], [10.5] and [10.6] to account for this and the total cooling power, P_{cool}, is then given by equation [10.12]. (From [GIA 06, section V.C.1])

$$F(E,\ V, T_e, T_b) = f(E - e\ \ (V/2), T_e) - f(E, T_b) \quad [10.11]$$

$$P_{cool} = \frac{2}{e^2\ \ R_T} \int_{-\infty}^{\infty} (E - e\ \ (V/2))\ \ F(E,\ V, T_e, T_b)\ \ g(E)\ \ dE \quad [10.12]$$

where R_T is the normal state tunnel resistance of a single NIS junction. Both junctions are assumed to have equal tunnel resistance; asymmetry in the junction resistances was shown to have only a weak effect, with a 7% change in cooling power for a factor of 2 difference in R_T [PEK 00b].

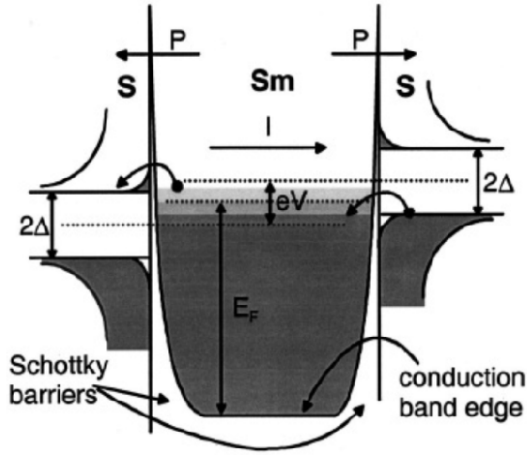

Figure 10.6. *Energy-band diagram illustrating cooling in the S–Sm–S structure. S denotes superconductor and Sm semiconductor. 2Δ is the energy gap in the superconductor, E_F is the Fermi energy of the semiconductor and P is the heat flow out of the semiconductor. V is the applied voltage and I is the resulting current. The gray areas denote the Fermi distribution of occupied electron states (from [SAV 01])*

10.2.5. *Double junction superconductor-silicon-superconductor (SSmS) cooler*

The region being cooled in a SINIS structure needs to contain a band of charge carriers that form a Fermi sea. As an alternative to electrons in a normal metal, electrons or holes in a degenerate semiconductor can also be used. In that case, the density of charge carriers will be several orders of magnitude lower, which will increase the amount by which the temperature can be changed for a given current, as a larger fraction of the Fermi sea can be accessed, but will reduce the cooling power of the device if it is being used for indirect cooling as the current is lower and so fewer electrons are removed. The junction between a semiconductor and a superconductor can also have a Schottky barrier, which provides the required tunnel barrier without the need for an additional insulating layer.

Savin *et al.* replaced the normal metal with a degenerate semiconductor (Sm), in the arrangement shown in Figure 10.6 [SAV 01]. Although this figure was used to illustrate a SINIS structure it actually shows the energy diagram of double junction SSmS cooler.

Another difference between metals and semiconductors is the strength of the electron- (or hole-)phonon coupling. This can be much weaker in semiconductors and means the charge carriers can more easily be thermally isolated from the lattice.

10.3. Limitations to cooling

Figure 10.7(a) shows a typical metal SINIS cooler fabricated by the Aalto (Helsinki) group, using e-beam lithography [PEK 04]. A central island of copper, of purity 6N (99.9999%), is connected to two superconducting aluminum reservoirs at either end of the island via Al_2O_3 tunnel barriers. Figure 10.7(b) shows the probe voltage/temperature versus the cooler voltage V_C. The plot shows a number of curves for different bath temperatures T_b, which can be read off in Figure 10.7(b) at the central point where $V_C = 0$. As the bias voltage is increased, the temperature drops and is observed to reach a minimum at biases just below 2Δ, with cooling being generally symmetrical with V_C due to the symmetric nature of the device. This maximum cooling ($T_{e,\,min}$ - T_b) varies with T_b: at high bath temperatures, cooling is limited by the high heating power of the lattice which, in metals, increases as T_b^5. At lower temperatures, cooling is limited by a reduction in the tunneling current, because there will be fewer hot electrons, as given by the Fermi distribution function. At the lowest bath temperature, the slight increase in temperature for low biases was attributed to non-equilibrium effects and states within the superconductor bandgap. This has been termed the "zero-bias anomaly".

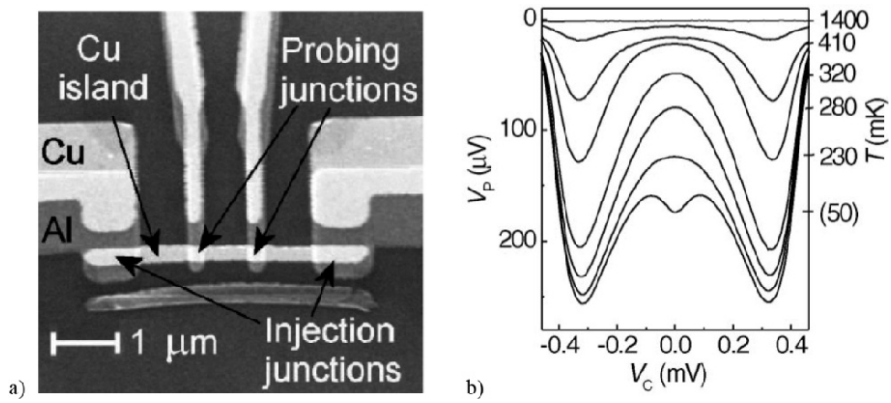

Figure 10.7. *a) Plan view scanning electron micrograph of a typical cooler fabricated using a double angle shadow mask technique. Al (dark gray) was deposited first, through a shadow mask, then the surface was oxidized. Cu (light gray) was then deposited though the same shadow mask, but from a different angle, so that Cu is above the Al in the junction regions. Note an unused Al island at the bottom of the picture is a consequence of this fabrication technique. b) Cooling data, where voltage V_P across the probe junctions for a constant current bias (28 pA) is shown against voltage V_C across the two injection junctions. Cryostat temperature, corresponding to the electron temperature on the N island at $V_C = 0$ is indicated on the right vertical axis. Below 100 mK this correspondence is uncertain (from [PEK 04])*

10.3.1. *States within the superconductor gap*

Real devices often contain imperfections and/or impurities, and the proximity of a normal metal may cause energy states to occur in the superconductor bandgap, which gives rise to junction leakage with electrons, not just the hot ones, able to move from the normal metal into these mid-gap states of the superconductor. These states in the superconductor bandgap can be modeled using the Dynes formula, (equation [10.4]). The parameter Γ is often expressed as a factor of the superconducting gap Δ, and its effect on the density of states is shown in Figure 10.8. This clearly demonstrates that the superconducting gap is heavily populated for Γ/Δ = 0.1 with a considerable degradation to the sharp peaks in density-of-states on either side of the gap that are responsible for the superconducting properties. Therefore, for working cooler devices, Γ must be kept much smaller and preferably well below 0.01 Δ.

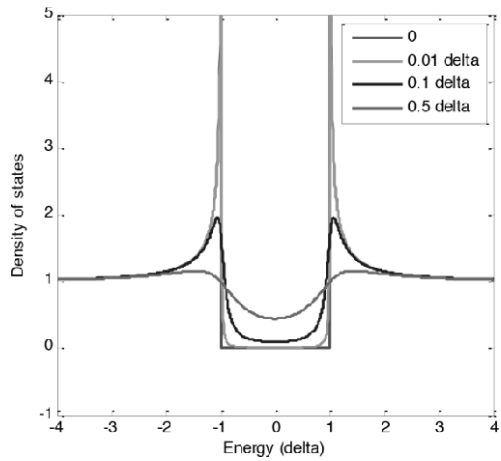

Figure 10.8. *Density-of-states, as given by the Dynes formula for Δ = 0.2 meV (approximate value for aluminum) and for different values of the smoothing parameter Γ, top to bottom Γ=0, 0.01Δ, 0.1Δ, 0.5Δ. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The combined effects of Γ and R_T are shown in the calculation of Figure 10.9. This theoretical model considers a silicon-based cooler, with a low electron-phonon coupling constant that leads to a lower minimum electron temperature, and takes vanadium as the superconductor. As vanadium has a gap four times larger than aluminum, cooling can be achieved from a higher bath temperature – in this case 1.2 K, which is within easy reach of mechanical pulse tube coolers. The minimum temperature that can be reached is clearly very sensitive to both Γ and R_T, with no cooling at all happening if either of these are too large.

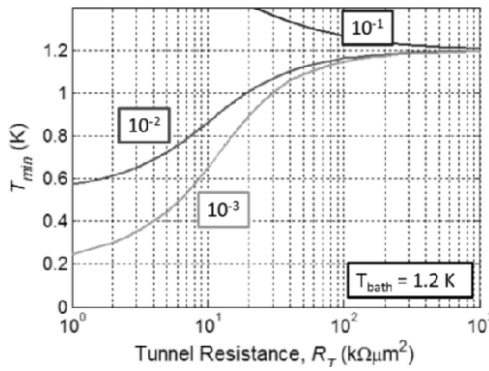

Figure 10.9. *Minimum temperature attainable in a silicon-vanadium S-Sm-S cooler starting from a bath temperature of 1.2 K as a function of tunnel resistance for Γ/Δ values of 0.1, 0.01, and 0.001 (indicated on the curves). For vanadium Δ = 0.8 meV. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

10.3.2. *Joule heating*

Leakage through the junction results in a heating power that is given by a $V^2/2R_{leak}$ term in the heat balance equation for a double junction. The factor of ½ comes from $2(V/2)^2/R_{leak}$ for the double junction device. R_{leak} is the leakage resistance per junction, whereas V is the voltage across two junctions. This leakage could, for instance, be caused by pin holes in the tunnel barrier. The model is also useful as an approximation to the effect of gap states in the superconductor or Andreev reflection. Figure 10.10 shows the effect of such a leakage current on the *T-V* plot of a cooler junction, characterized by heating above the bath temperature at low bias (see region ~0.2 mV) and a reduced cooling performance at higher bias (lower minimum T_e at 0.33 mV).

10.3.3. *Series resistance*

When comparing metal-based coolers with semiconductor ones, the resistivity of degenerately doped silicon (10^{-2}–10^{-4} Ωcm) is higher than that of normal metals such as copper (~10^{-6} Ωcm). This adds a series resistance between the cooler junctions, and hence a joule heating term to the heat balance equation, given by I^2R_{Si}, where I is the current though the device and R_{Si} is the resistance of the silicon island. At low temperatures and for $V < 2\Delta/e$, the tunnel current is low and the effective junction resistance dV/dI is very high, so most of the voltage drops across the junctions and there is little joule heating. At higher biases, as the tunnel current begins to increase, the joule heating increases and dV/dI drops to a lower value so that the voltage drop across the junctions becomes a smaller proportion of the total bias across the device;

the net effect of this is to spread out the temperature versus bias characteristic toward higher biases and also to increase the temperature minimum as shown in Figure 10.11. Note we have used a high R_{Si} = 1 kΩ to illustrate this point, but a typical silicon resistance is usually lower, the device mentioned in [SAV 03] with a dopant concentration of 4 × 10^{19} cm^{-3} had an R_{Si} of 150 Ω which results in only a small rise in the minimum temperature.

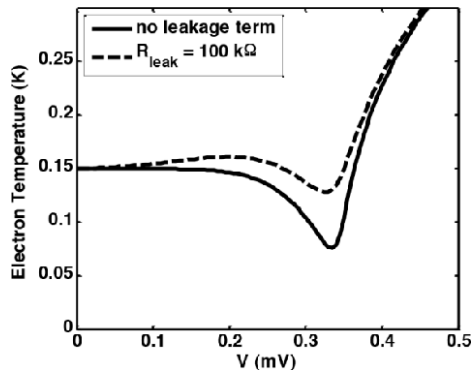

Figure 10.10. *Junction leakage heating with R_{leak} = 100 kΩ for each junction, compared to no leakage current. The following parameters were used, corresponding to values given in [SAV 03]: Δ = 0.17 meV, R_T = 750 Ohm, Σ = 10^8 $WK^{-5}m^{-3}$ and Ω = 4.2×10^{-17} m^{-3} for a typical silicon microcooler, with a carrier concentration of 4 × 10^{19} cm^{-3}. The superconductor density of states is assumed to be ideal, using equation [10.4]*

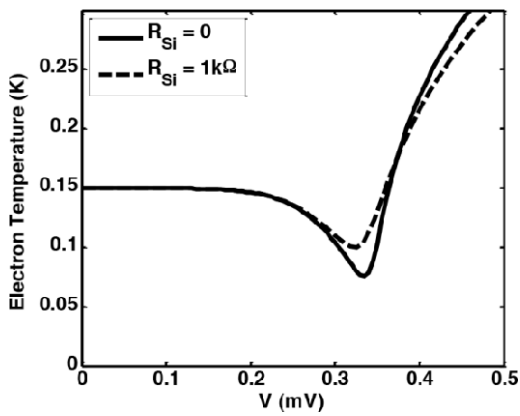

Figure 10.11. *Silicon resistance joule heating. Electron temperature versus cooler voltage bias for bath temperature T_P = 150 mK, R_{Si} = 0 (solid line) and R_{Si} = 1 kΩ (dashed line). Calculated using equations [10.1], [10.3], [10.4], [10.6]–[10.10] but with an additional I^2R_{Si} term in the heat balance equation [10.7] to account for the Joule heating. The other parameters are as used for Figure 10.10*

10.3.4. *Quasi-particle-related heating*

Quasi-particles entering the superconductor from the normal metal can cause significant heating of the normal metal if they linger near the junction [JOC 98]. Two quasi-particles can be recombined to form a superconducting Cooper pair and a phonon, which is absorbed by the junction. Second, quasi-particles may tunnel back through the barrier into the metal, effectively decreasing the net cooling current across the junction. These two mechanisms can be modeled jointly by the term [FIS 99, CLA 04]:

$$\beta \quad P_S . \qquad [10.13]$$

A simplifying assumption where $\beta < 1$ denotes the fraction of the power deposited in the superconducting electrode P_s that is returned to the metal. β is a parameter dependent only on the temperature of the surrounding bath, and

$$P_S = IV + P_{cool} \qquad [10.14]$$

Quasi-particle heating can seriously limit the cooling power of the device, and it is important to allow the quasi-particles to leave the tunneling region of the junction before they can tunnel back or recombine. The simplest solution is to use a thick superconductor, with minimum overlap between superconductor and normal metal to encourage diffusion away from the junction area [ULL 01, CLA 04]. It also helps us to use arrays of many small area junctions [LEO 99].

It is often beneficial to incorporate a "quasi-particle trap", consisting of a normal metal in contact with the superconductor, or via an oxide tunnel junction [CLA 04, ULL 00, PEK 00a]. A copper quasi-particle trap, outside the SINIS structure is shown in Figure 10.12. The quasi-particles minimize their energy by falling into the Cu, the trap should be some distance away from the junction, in order to not suppress the superconductivity at the junction by the inverse proximity effect [SOL 72].

As electrons are extracted from the normal metal, electron-electron scattering restores equilibrium. If the tunneling rate is too high compared to the relaxation rate, then the electrons in the normal metal will be driven out of equilibrium and eventually the extraction rate will be determined by the rate at which electron-electron scattering replenishes the tunneling channels [EDW 95, PEK 04]. Edwards *et al*. show that the relaxation rate falls at low temperatures and when this limits the extraction rate, the NIS cooling power can vary as T3 at low enough temperatures.

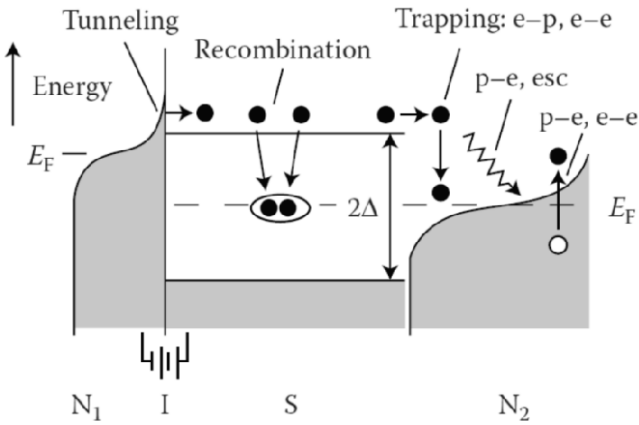

Figure 10.12. *Energy-level diagram. Occupied states are shaded. NIS junction electrodes are marked N_1 and S. Current flow through the junction creates quasi-particles in S. Some quasi-particles recombine before reaching an adjacent normal metal film marked N_2. Quasi-particles which scatter inelastically in N_2 are trapped. Quasi-particles relax in N_2 by electron-phonon (e-p) and electron-electron (e-e) interactions. A phonon (jagged line) emitted by a relaxing quasi-particle can interact with other electrons (p-e) or escape the trap (esc). Electrons in the trap are heated by phonon-electron (p-e) and electron-electron (e-e) interactions (from [ULL 00])*

Furthermore, inelastic scattering in the superconductor or the inverse proximity effect from the nearby normal region, could lead to states in the superconducting energy gap. Pekola *et al.* show how these effects may lead to anomalous heating near $V = 0$ at the lowest temperature, as shown in Figure 10.7(b) [PEK 04].

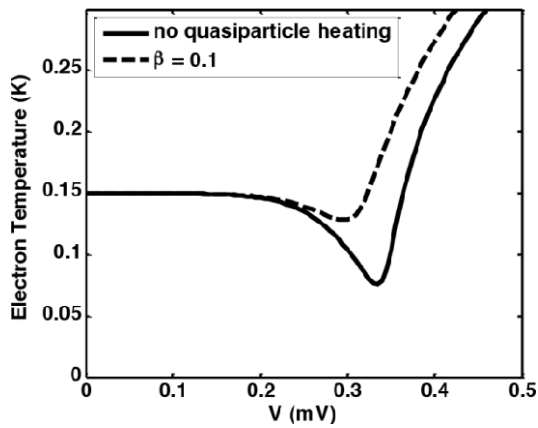

Figure 10.13. *Electron temperature with (dashed line) and without (solid line) quasi-particle heating. The other parameters are as used for Figure 10.10*

10.3.5. *Andreev reflection*

For voltages $eV << \Delta$, charge transfer occurs through Andreev reflection if the barrier transparency is high. An electron (hole) in the normal metal impinging on the superconducting interface is reflected as a hole (electron) and creates a Cooper pair in the semiconductor (Figure 10.14(a)). The energies of the hole and electron are located symmetrically around E_F and hence there is no energy transfer. The Andreev current is associated with a significant energy dissipation in the normal metal. Disorder in the normal metal, or reflection from a second barrier (due to close proximity), can greatly enhance this process; a carrier then experiences several collisions with the interface (Figure 10.14(b)).

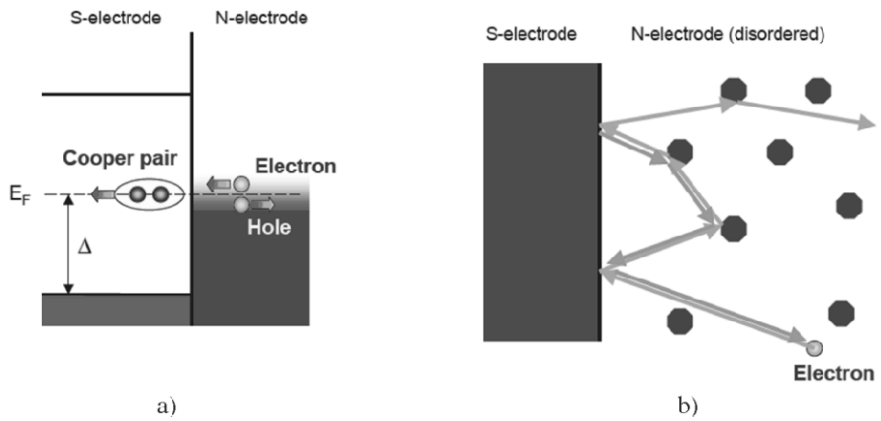

Figure 10.14. *a) Andreev reflection at an SN interface; b) multiple Andreev reflections due to scattering in the normal metal (figure from A. Savin, private communication)*

Bardas and Averin have shown that the junction cooling power is a function of the transparency of the junction and at low transparency the cooling power scales as T3/2 [BAR 95]. However, the cooling power reaches a peak at a particular transparency and then falls at higher transparencies as Andreev reflection begins to dominate. Also, as the temperature drops the peak transparency also drops, such that the Andreev process is stronger at low temperatures for a given tunnel junction and hence the cooling power may be reduced and heating may be observed.

The group of Coutois and Hekking in Grenoble have considered Andreev heating in the energy balance equation. Figure 10.15 shows the conductance versus bias characteristic of a SINIS cooler that they fabricated. The Cu above the Al on the right-hand side, accessed through an oxide barrier, acts as an effective quasi-particle

trap, at about 0.3 μm to the right of the cooler junctions. The upward curvature at $eV \leq \Delta$ is clear evidence of cooling. The temperature may be lowered from 230 mK at zero bias to < 50 mK at 2Δ/e. The zero bias anomaly seen in the 90 mK curve in Figure 10.15 is convincing evidence of an Andreev current.

The current voltage characteristics of the SINIS cooler are shown in Figure 10.16. It was necessary to include a significant heating term $I_A V$ to get a good fit to the data [RAJ 08]. The authors obtain excellent fits to their experimental data, without consideration of quasi-particle heating. This suggests that such heating has been minimized in their device geometry, which includes a quasi-particle trap within 0.3 μm of the junction, and a junction area of 1.5 × 0.3 μm. Giazotto has proposed a number of ways [GIA 02, GIA 06] for minimizing Andreev currents in these junctions but, as of now, no experiments have been carried out.

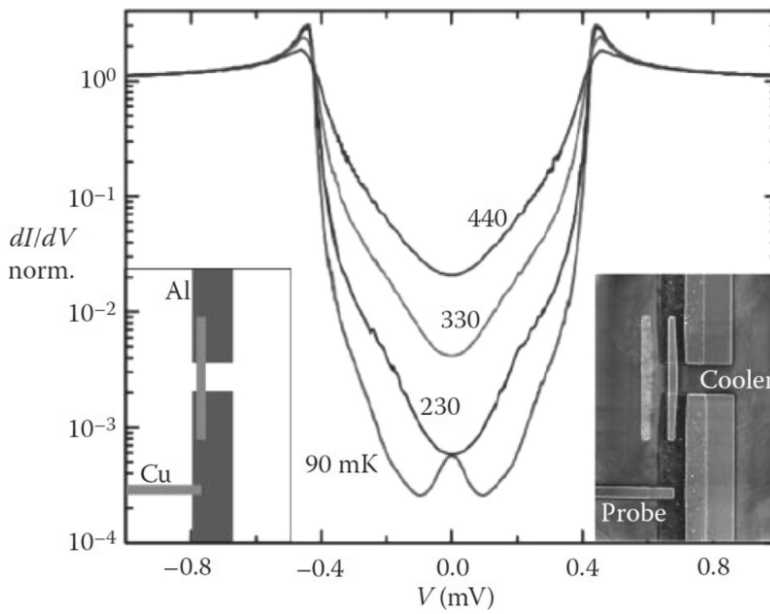

Figure 10.15. *Normalized differential conductance of an Al/Al_2O_3/Cu/Al_2O_3/Al cooler as a function of bias voltage at bath temperatures of 90, 230, 330 and 440 mK. Left inset: geometry of the sample. Right inset: scanning electron microscope micrograph of a typical cooler sample, normal metal Cu electrodes appear light gray, the two superconducting Al reservoirs are dark gray (from [RAJ 08])*

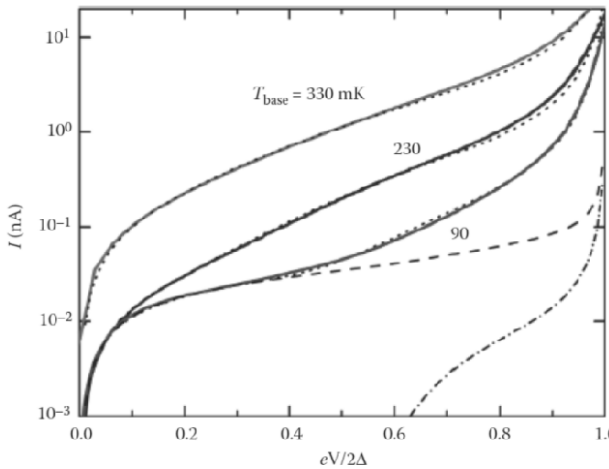

Figure 10.16. *Current-voltage characteristic of the SINIS cooler junction as a function of the voltage, at cryostat bath temperatures of 90, 230 and 330 mK together with best-fit calculated curves. Dot-dashed line: model including the cooling by the tunnel current. Dashed line: model including the Andreev current, but not the related heating. Dotted lines: full model taking into account the Andreev current and the related heating (from [RAJ 08])*

One way to remove Andreev reflection is to apply a magnetic field to the junction, which destroys the coherence of the quasi-particles. In an S-Sm-S junction, using silicon and aluminum, we have seen a small effect of magnetic field, as shown in Figure 10.17. The minimum temperature reached with 2 gauss applied is a couple of mK lower than in the absence of magnetic field. This could be evidence that Andreev reflection led to warming in the zero field case. However, this particular junction was certainly not optimized, as can be seen by the minimum temperature being only 246 mK; so there may be another explanation for the small change with field. Alternatively, this may be an indication that there would be a much larger effect of magnetic field in an optimized junction with a much lower minimum temperature.

10.4. Heavy fermion-based coolers

In an NIS junction, the density-of-states of the normal metal is approximately constant as the bias range is much less than the Fermi level. However, the density-of-states near the Fermi level of a heavy fermion metal differs significantly from that of a normal metal due to the existence of the resonant states or formation of hybridization gaps [LAW 81]. It has been suggested that the hybridization gap in a heavy fermion can be exploited to obtain electronic tunneling cooling in a normal-metal/insulator/heavy-fermion junction [GOL 03] in a similar way to the

superconducting gap that facilitates NIS junctions. For materials where the hybridization gap is large (many meV) this could be a very attractive way to make electronic coolers starting from much higher base temperatures; however, such devices have yet to be realized.

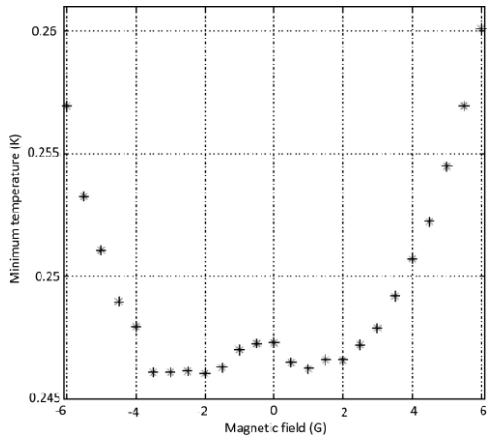

Figure 10.17. *Minimum temperature reached in an Al-silicon cooler as a function of applied magnetic field, showing possible effect of Andreev reflection increasing the minimum temperature in zero-magnetic field*

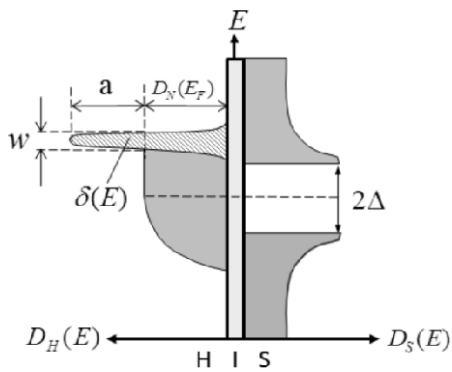

Figure 10.18. *Density-of-states in a heavy fermion-insulator-superconductor junction. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Theoretical calculations also suggest that the cooling performance of a SINIS refrigerator (Figure 10.18) can be significantly improved by replacing the normal metal in the junction with a heavy fermion metal. For most heavy fermion materials known to date, the resonant density-of-states can be 10–100 times higher than that of

normal metals, with the width of the resonant band ranging from 80 μeV to 7 meV [HEW 93]. This can be attributed to an increase in both tunneling current and tunneling conductance near the superconducting edge due to the resonant density-of-states in heavy fermion metals. Together with the possibility of suppressing the Andreev reflection, the superconductor-insulator-heavy fermion metal-insulator-superconductor (SIHIS) structure junction provides a good choice for developing improved mK electronic tunneling coolers.

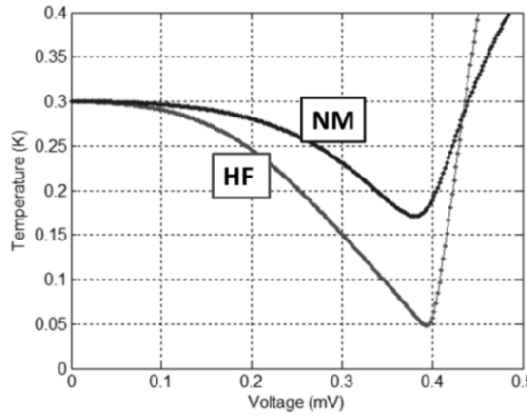

Figure 10.19. *Electron temperature obtained in a SIHIS (black HF curve) compared to a SINIS (light gray NM curve) cooler. The parameters are based on a realistic model of a SINIS junction, volume 2 μm^3, R_T 100 Ω and a bath temperature of 300 mK. The superconductor is Al with $\Gamma/\Delta = 10^{-3}$ and Δ = 0.2 meV*

Figure 10.19 shows the result of calculating the electron temperature obtained in a heavy fermion (HF) or normal metal (NM). For the given parameters, the minimum cooling temperature for a SINIS junction is 171 mK, while it is much lower, at 48 mK, for a SIHIS junction, indicating a substantial improvement by employing a heavy fermion metal. Note that the same parameter values are used for Σ, Γ and R_T for both the normal metal and heavy fermion in our calculation due to the lack of knowledge of these parameters in heavy fermions, which should be amended with actual values for a more reliable estimate of the cooling capability of SIHIS coolers.

10.5. Summary

This chapter has introduced the idea of cooling a normal metal by extracting the most energetic electrons through tunneling to a superconductor. The basic principles

of operation were outlined and some of the limitations on reaching the lowest electron temperatures were discussed. From this, it can be seen that quality of the interfaces is crucial to avoid mid-gap states in the superconducting energy gap and to minimize the tunneling resistance. The amount of heat entering the electronic system from the lattice greatly affects the minimum temperature obtained and can be minimized by using very small devices and/or reducing the coupling between the electrons and phonons of the material. This will be discussed further in Chapter 12, along with the related issue of using the electronic refrigeration elements to actually cool the lattice.

The normal metal being cooled can be replaced with an alternative conducting material, which can be a semiconductor, heavy fermion metal or another superconductor. In the latter case, multistage coolers can be envisaged that use superconductors with different energy gaps in each stage, with the gap matched to the temperature range of operation. More details of semiconductor-based coolers, where the reduced density of states compared to a metal can lead to lower minimum temperatures, will be discussed in Chapter 11.

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11

Silicon-based Cooling Elements

11.1. Introduction to semiconductor-superconductor tunnel junction coolers

Superconducting tunnel junction coolers were first produced in the 1990s [NAH 94, LEI 96]. Cooling from a bath temperature of 300 mK is technologically important because it is a temperature that can be reached using a simple ^{3}He sorption cycle refrigerator. Lower temperatures are typically achieved using complex and expensive ^{3}He/^{4}He dilution or adiabatic demagnetization refrigerators. Some success in electron cooling from 300 mK has been realized using normal metal-based coolers [LUU 00]. However, attempts to scale up the cooling to larger volumes have been challenged by the higher powers required and difficulties in thermalizing the hot quasi-particles entering the superconductor [FIS 99, NGU 13].

The cooling power and heating problems can be reduced by substituting the normal-metal island with a degenerate semiconductor. The basic principles of NIS cooling still apply and the superconductor–semiconductor (S–Sm) cooler presents some benefits compared with normal metal NIS junctions. First, in semiconductors, the electron–phonon (e-ph) coupling strength is generally weaker than in metals; in Si the electron-phonon conductance is typically a decade lower than that of normal metals [KIV 03]. This dramatically reduces the heat flow between the electrons, which are acting as the refrigeration medium and the lattice, meaning that the rate of heat removal from the electronic system can be lower to reach a given base temperature or that a lower electron temperature can be reached. Second, the Schottky barrier formed at the semiconductor-superconductor interface can act as the tunneling barrier and so no oxide layer is required. This makes fabrication more

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straightforward compared to standard shadow evaporation techniques, especially for large-area junctions where a few imperfections can induce large amounts of leakage. In principle, the Schottky barrier resistance and electron–phonon coupling can both be tuned by varying the doping level in the semiconductor. There are, however, disadvantages compared to normal metal coolers in that semiconductors have a higher resistivity than metals, even when highly doped, and hence generate more parasitic Joule heating. Quite large sub-gap currents also appear that degrade the cooler performance.

Despite the promised advantages, initial experiments of cooling electron gases within semiconductors did not demonstrate any significant cooling from 300 mK, because of the relatively high-junction resistances [SAV 01] and, as the doping density of silicon was increased, leakage and Joule heating became worse, negating the use of low resistance junctions [SAV 03]. This chapter will outline some of the progresses made during the nanofunction program on electron cooling from 300 mK in silicon-based junctions. There have been significant improvements, initially by optimizing device parameters to reach an electron temperature of 258 mK for a bulk silicon control, [PRE 11] and later to 90 mK for a strained silicon device with a low-leakage junction [RIC 14]. Further enhancement is expected, as increasing the strain in silicon reduces the electron-phonon coupling by a further decade when moving from unstrained silicon to 0.95% strained silicon, [MUH 11] and to three decades lower than copper when strained by 1.36% [RIC 13].

11.2. Silicon-based Schottky barrier junctions

Cooling in S–Sm structures was first reported by Savin *et al*. in 2001 [SAV 01] using n^+ silicon doped to 4×10^{19} cm^{-3} and aluminum as the super-conducting metal. A schematic diagram of the structure appears in Figure 11.1. A cooling power of roughly 0.5 pW was achieved with two 90 μm^2 junctions having a total junction tunneling resistance R_T of 800 Ω. Because of the small e–ph coupling, this small cooling power still led to a respectable 30% drop in temperature from 175 mK. In later work [SAV 03, SAV 04], they explored different n^+ doping levels N of the silicon island and found that the contact resistance R_T of the Al-Si interface reduced as $\exp(N^{-1/2})$, as expected from theory, although this advantage from increased doping is partially offset by an increase in e-ph coupling. Nevertheless, the cooling power should increase, because the e-ph coupling only increases linearly with the doping level, rather than exponentially for the tunnel resistance. Figure 11.2 depicts the competing effects on electron cooling of variations in R_T and e-ph coupling with doping level. However, a greater cooling effect was only seen from the higher bath temperatures, above ~300 mK, and for $N > 1 \times 10^{20}$ cm^{-3} the cooling effect reduced again. This was attributed to large-leakage currents through the barrier at lower transparencies, i.e. a large value of Γ/Δ in equation [10.4]. In Al–Si junctions, this

parameter has been found to be 0.01–0.1, which is a few orders of magnitude worse than in Al–Al_2O^3–Cu junctions.

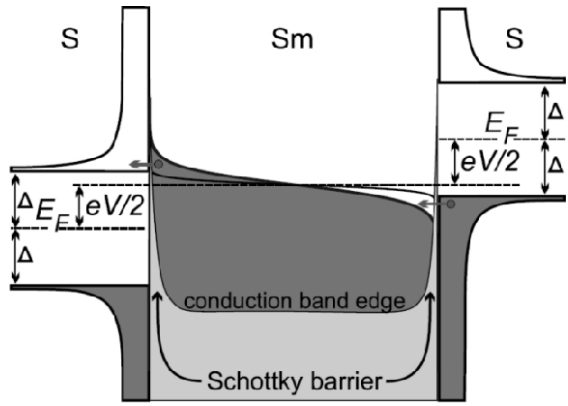

Figure 11.1. *The energy diagram of an S–Sm–S structure. Basic principles are identical to those in Figure 10.1. The insulating layers are replaced by a Schottky barrier at the Al–Si interface. The energy gap of the semiconductor plays no role, as the island is degenerately doped and only the conduction band is relevant, from [MUH 12]*

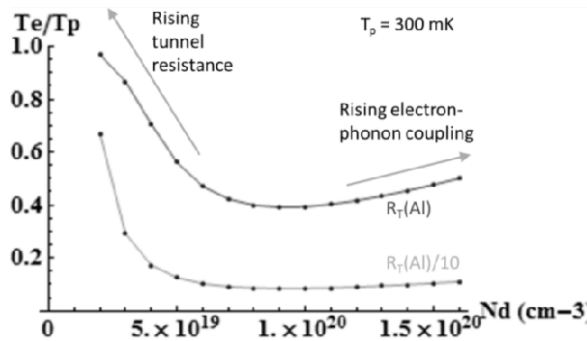

Figure 11.2. *Variation in cooling efficiency with level of n-doping in silicon for a Si-Al Schottky barrier junction. The beneficial effect of reducing R_T by an order of magnitude is also shown. In this figure sub-gap leakage is ignored*

Niobium–silicon SINIS junctions have also been studied [BUO 03]. The contact resistance between Nb and Si was found to be much smaller than between Al and Si, as expected with the smaller Schottky barrier height, but no cooling was observed. Again, this was because of large sub-gap leakage currents. Like Nb with its super-conducting transition temperature (T_c) of 8 K, vanadium has a larger superconductor gap ($\Delta = 0.8$ meV, $T_c = 5$ K) than Al ($\Delta = 0.2$ meV), which means cooling from a higher temperature should be possible (as mentioned already in Figure 10.9). Recently, progress was reported on making a V-Al SIS' cooler [QUA 11]. For a good quality junction it was necessary to first cover the oxide layer with a small amount of Al before depositing the V. The Al/V bilayer had a T_c of 4 K and the authors were able to achieve a significant temperature reduction of the quasiparticle system in Al from 1 K to 400 mK. Unfortunately, efforts to date in making Si-V semiconductor Schottky barrier tunnel junctions by this method have not yet been successful due to poor adhesion of the V.

PtSi is an interesting material to consider as a Schottky barrier to Si because of its role as a contact material in the semiconductor industry, due to their reliability and good-electrical characteristics. Coincidentally, PtSi has a T_c of around 1 K and so is a good candidate for electronic cooling. Hence, electronic coolers made with PtSi should be effective starting from much lower bath temperatures than with Al.

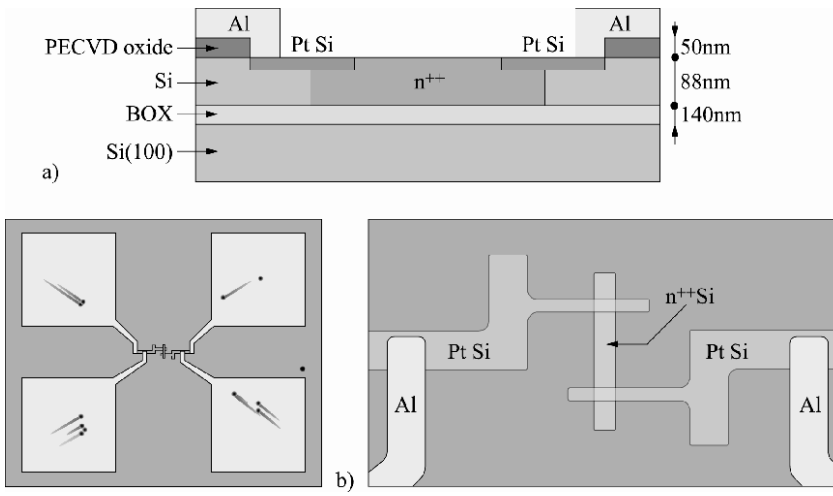

Figure 11.3. *a) Cross-section of the PtSi-Si device. The PtSi thickness was 10 nm. Aluminum contacts were patterned by lift-off. b) Optical image of the PtSi device and close up. The length of the central n^{++} island is ~30 μm and the junction areas are 2.5 μm by 5 μm*

PtSi-Si tunnel junctions were fabricated at the Jülich research center, as described in [PRE 13], with the device structure shown in Figure 11.3. A silicon on insulator substrate was used and the active areas were ion implanted with arsenic, giving a dopant concentration of ~ 8 $\times 10^{19}$ cm^{-3} after activation. Four point probe *I-V* measurements gave a sheet resistance of about 100 Ω/square, confirming the implanted dopant density. The series resistance R_S of 320 Ω is quite high, but only reduces the cooling achieved by about 20%, according to our calculations. As with many superconductors, the T_c of PtSi (and hence also Δ) is suppressed in thin films. In our device, there is a 10 nm thick PtSi film for which T_C was measured to be reduced to 0.786 K, compared to 1.015 K for a 100 nm film.

I-V measurements on the PtSi device were performed at 100 mK using a dilution refrigerator: the differential conductance is shown in Figure 11.4. Initially, an isothermal model, with $T_e = 100$ mK, was used to extract the tunneling resistance $R_T = 300$ Ω (3.75 kΩ μm^2), superconductor half-gap $\Delta = 0.07$ meV and Dynes leakage parameter $\Gamma/\Delta = 0.8 \times 10^{-2}$. This value is fairly typical of semiconductor devices, but not as low as found in normal metal-based coolers. Figure 11.4 shows that although there is good agreement at high biases, the isothermal model (dashed line) does not fit the experimental data for biases of less than 0.1 mV. In that region, the reduced current relative to the isothermal model is characteristic of cooling in the device [RAJ 07].

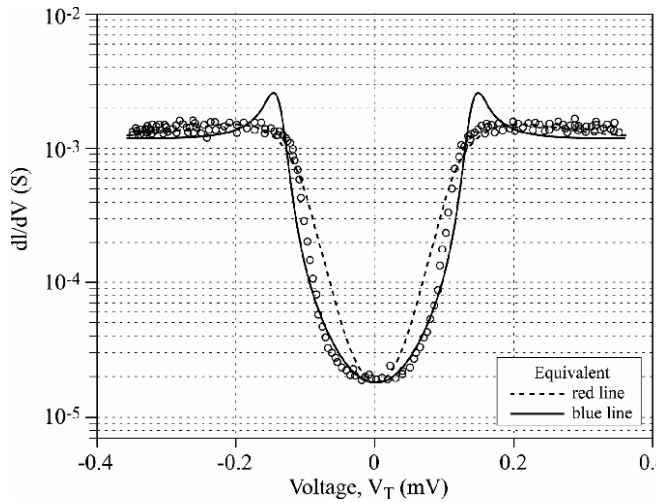

Figure 11.4. *Differential conductance for the PtSi cooler measured at 100 mK (circles). The dashed line shows a 100 mK isotherm fit to the model. The solid line gives a much better fit in the low-bias region using a cooling model*

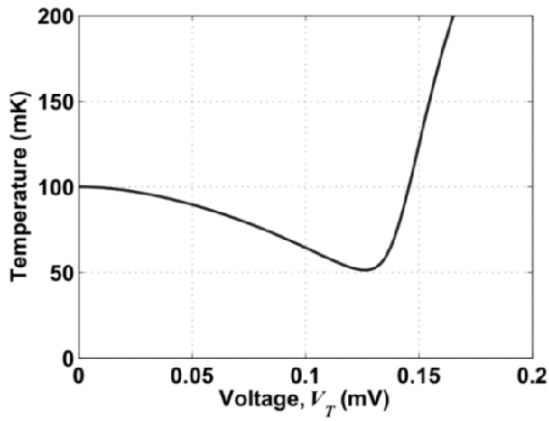

Figure 11.5. *Temperature-voltage calculation for a bath temperature of 100 mK using the cooling model and parameters obtained by fitting the I-V data*

The observed data can be reproduced much better using the cooling model outlined in Chapter 10, as shown by the solid line in Figure 11.4, particularly for biases < 0.1 mV where most of the cooling occurs. Parameters used in the fit are $\Sigma = 3.1 \times 10^8$ $Wm^{-3}K^{-6}$, taken from [KIV 04] for a similar sample, and a volume of 14 μm^{-3} from the measured dimensions in Figure 11.3. The model therefore shows that the silicon island cooled from 100 mK to about 50 mK, as shown in Figure 11.5, and the PtSi refrigeration element provided a cooling power of 0.72 pW at 100 mK. This demonstrates that enhanced cooling is possible at the lowest temperatures using a narrow band-gap superconductor, where the sub-gap leakage is reduced (because the energy integral is smaller), with cooling by a technologically interesting factor of 2 – from 100 to 50 mK.

11.3. Carrier-phonon coupling in strained silicon

Tunnel junction coolers function by directly cooling the electron system to an electron temperature T_e that is lower than that of the original thermal bath T_b and may also be different from the lattice temperature of the piece of material in which the electrons reside, the phonon temperature T_{ph}. The system as a whole is consequently not in thermal equilibrium with these three different temperatures identified in different parts, and other temperatures associated with for instance the superconductor and contact regions that will be warmer than T_b as they extract heat from the part being cooled. Indeed, it could be asked whether any of the sub-systems themselves are sufficiently close to an equilibrium for a “temperature” to be defined.

Within the electron system, an equilibrium described by Fermi-Dirac statistics (with a well-defined temperature) is maintained by electron-electron scattering, which is a much faster process than any other timescales being considered. Similarly, the phonons are described by Bose–Einstein statistics with a fast phonon-phonon scattering rate. However, the connection between the two systems depends on electron-phonon (e-ph) scattering, which can be considerably slower leading to a quasi-equilibrium with a difference between T_e and T_{ph}. The e-ph coupling is weaker at lower temperatures, which is the reason why electronic tunnel junction cooling becomes viable in the mK regime. The e-ph coupling strength also varies between materials, which means it can be tuned; reducing the e-ph coupling reduces the heat load on cooled electrons and allows lower carrier temperatures to be reached, but precludes effective membrane cooling by these cooled electrons.

Quasi-equilibrium with $T_e < T_{ph}$ is obtained when the cooling power of the tunnel junction is equal to the power received into the electron system from the lattice $P_{e\text{-}ph}$, as set out in equation [10.8] (ignoring any other radiative heating).To change the electron temperature by an infinitesimal amount dT_e requires an energy $C_e dT_e$, where the electronic heat capacity is $C_e = \gamma T$. The rate of change of this energy is provided e-ph coupling as $dP_{e-ph} = \tau_{e-ph}^{-1} C_e \, dT_e$ where the electron-phonon scattering rate is given by the power law $\tau_{e-ph}^{-1} = \alpha T_e^{\,p}$. Integrating from T_{ph} to T_e we get

$$P_{e-ph} = \Sigma \Omega \left(T_e^{\,p+2} - T_{ph}^{\,p+2} \right) \qquad [11.1]$$

which for normal metals with $p = 3$ reduces to the T^5 power law of equation [10.7] and shows that the parameter $\Sigma = \alpha\gamma/(p+2)$. In [SAV 01, SAV 04] the e–ph coupling in Si was also modeled with the T^5 power law, as in the normal metal case. However, according to [KIV 04] the theory of disordered metals [SER 00] is more appropriate to semiconductors, for which $p = 4$ leading to a T^6 power law. This temperature dependence was confirmed in [PRU 05] and quantitative agreement between experiment and theory obtained, provided the multiple conduction valleys of Si were included in the theoretical analysis. This degree of freedom is important in the low temperature e–ph coupling as phonon scattering can lift the valley degeneracy.

The six-fold conduction band valley degeneracy in silicon can also be reduced by straining the crystal (Figure 11.6). The conduction band is modified under tensile strain, produced by growing silicon epitaxially on a relaxed $Si_{1-x}Ge_x$ virtual substrate, into a two-fold degenerate level at a lower energy and a higher energy four-fold set. Prunnila [PRU 07] has shown that this has the potential to reduce e-ph coupling by a few orders of magnitude.

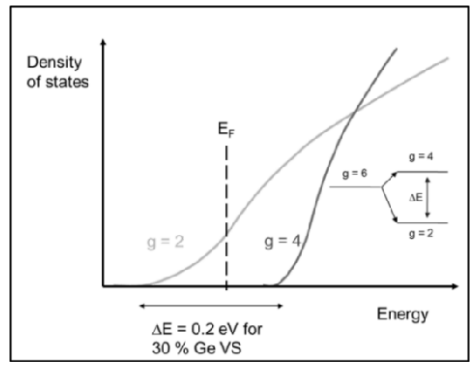

Figure 11.6. *Change of energy levels and density of states in strained silicon*

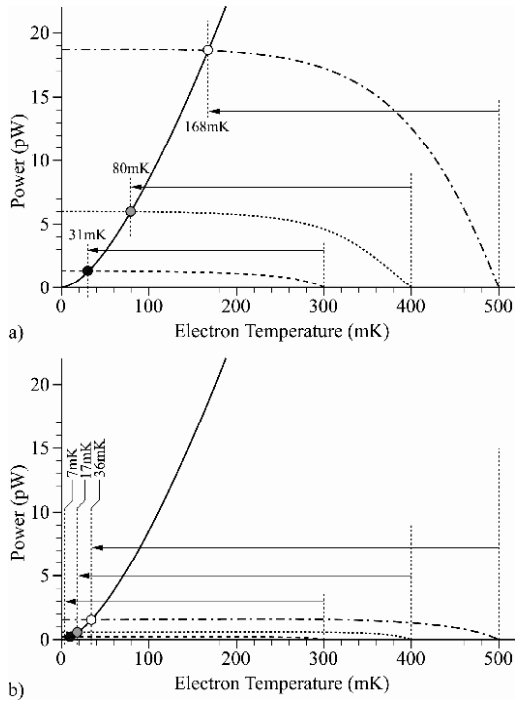

Figure 11.7. *Calculation of quasi-equilibrium base temperature based on balancing junction cooling power (solid line) with $P_{e\text{-}ph}$ from different phonon temperatures (dotted and dashed line). Points of intersection show the minimum electron temperature that can be reached for each bath temperature. (see Figure 10.5 for similar calc. with a metal cooler) The e-ph coupling constant Σ is reduced from a) 10^8 $Wm^{-3}K^{-6}$, to b) 10^7 $Wm^{-3}K^{-6}$, resulting in much lower base temperatures. Other parameters are the same: $\Omega = 6\ \mu m^3$; $\Delta = 0.2$ meV (Al), $R_T = 50\ \Omega$*

The impact on the minimum electron temperature reached of reducing Σ by a factor 10 in a Si-Al SSmS junction is shown in the calculations of Figure 11.7, where cooling to below 10 mK from a bath of 300 mK is predicted for parameters of an idealized junction. These parameters are not unrealistic and serve to show what could be possible, although they are demanding on reaching a low-tunnel resistance of 50 Ω and ignore other parasitic heating mechanisms. Figure 11.8 displays information on the electron cooling efficiency in a Si-Al junction for different e-ph coupling strengths, from which it can be seen that significant cooling performance from a starting point of 300 mK requires $\Sigma < 10^8$ $Wm^{-3}K^{-6}$ and that even weaker coupling is needed if cooling is to be effective from higher starting temperatures.

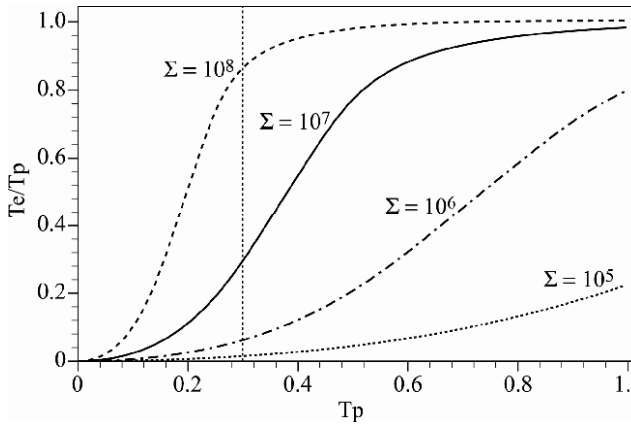

Figure 11.8. *Cooling ratio T_e/T_p for a range of e-ph coupling strengths Σ, shown as a function of the initial bath temperature which is assume to remain equal to the lattice temperature T_p. The vertical dashed line indicates performance at a bath temperature of 300 mK*

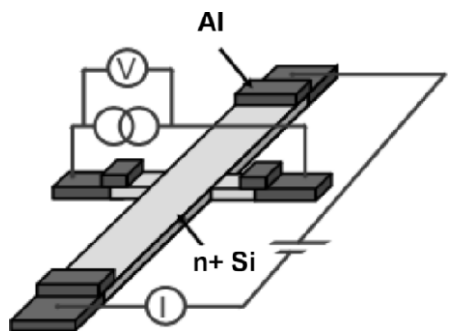

Figure 11.9. *Measurement setup for electron phonon coupling measurements*

11.3.1. *Measurement of electron-phonon coupling constant*

We have investigated [MUH 11] carrier-phonon coupling in unstrained silicon, with both n- and p-type dopants, and the effect of increasing the strain in silicon grown on a $Si_{1-x}Ge_x$ virtual substrate with the Ge fraction x of 20% and 30%. To measure this coupling constant, a heating experiment was designed in which a current was passed through a narrow bar of silicon and a tunnel junction thermometer midway along the bar used to measure the rise in electron temperature. The junctions in the middle of the bar have a constant current from a floating high-impedance current source and we monitor the induced voltage, which depends on T_e of the semiconductor island. The bias current through the thermometer junctions is selected so that it has a negligible heating effect and the thermometers are calibrated against a RuO thermometer in our dilution cryostat. Figure 11.9 shows the experimental setup and Figures 11.10–11.12 show how the measured electron temperature varied with heater power for different lattice temperatures. In each case, there is a point where the heat loss through e-ph coupling is insufficient to dissipate all the additional heat input, which leads the electron temperature increasing. It is clear from Figure 11.10 that this point is reached at much lower input power in the strained silicon bar than in the unstrained control, so the strained Si is always hotter. This clearly demonstrates that there is a weaker e-ph coupling in the strained Si.

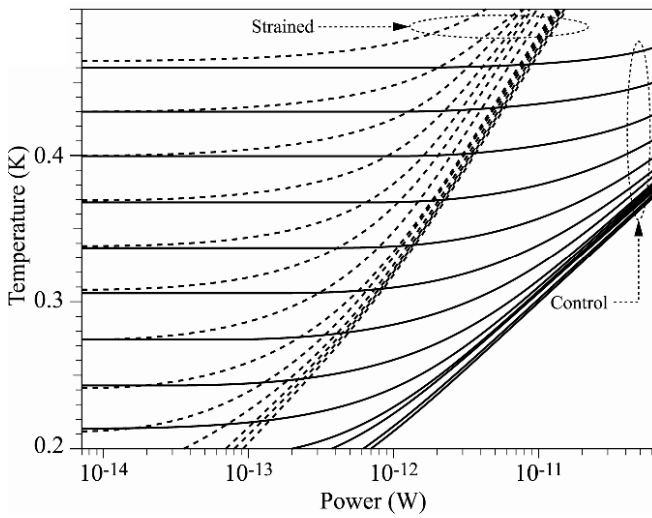

Figure 11.10. *Temperature recorded at the centre of the bar as a function of heater power. Each curve corresponds to a different initial lattice temperature. Solid curves are for bulk Si and dashed curves are for a Si epilayer under 0.95% strain through growth on $Si_{0.8}Ge_{0.2}$, from [MUH 11]*

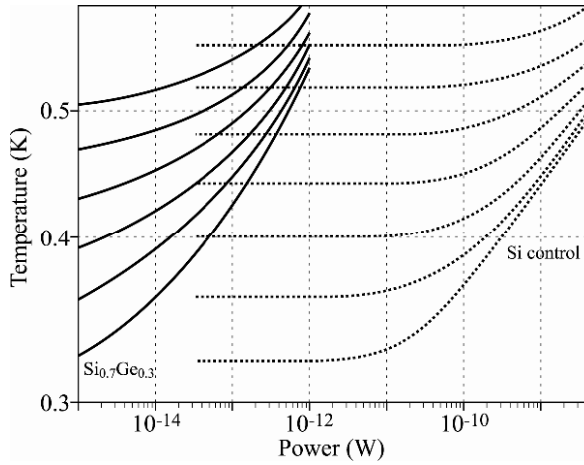

Figure 11.11. *As Figure 11.10 for a 1.36% strained Si sample grown on $Si_{0.7}Ge_{0.3}$ showing even more rapid increase in temperature for the more highly strained silicon*

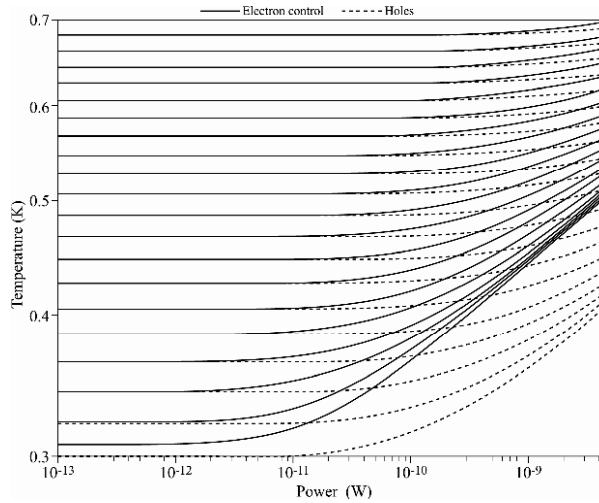

Figure 11.12. *As Figure 11.10 for a p-type Si sample showing a smaller increase in temperature, i.e. lower hole-phonon coupling (dashed lines) than electron-phonon coupling (solid lines)*

Comparing Figures 11.10 and 11.11, it can be seen that increasing the strain from 0.95% to 1.36% has quite a dramatic effect on heating in the electron gas and shows the e-ph coupling is continuing to decrease with increased strain. The results of a similar experiment on p-type Si are compared with the n-type control in Figure 11.12, where it can be seen that the hole temperature increases less than the electron temperature. This means the carrier-phonon coupling is stronger for holes in Si than for electrons.

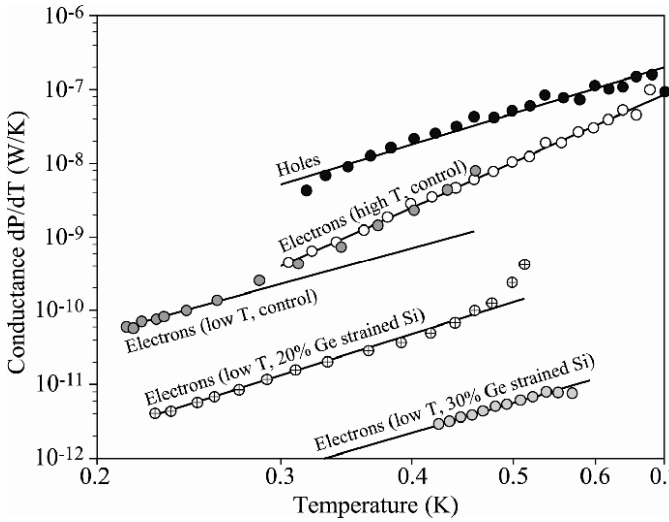

Figure 11.13. *Carrier-phonon conductance measurement results showing that the e-ph conductance decreases with increasing strain, reaching some four orders of magnitude lower than the hole-phonon conductance which is similar to values found in metals*

For a more quantitative measurement, Figure 11.13 shows the carrier-phonon conductance, defined in terms of the input Joule heating power P and the temperature as $G_{e\text{-}ph} = dP/dT_e$. It is clear that the e-ph conductance at 300 mK is at least a decade lower for the 0.95% strained Si compared to unstrained Si. The expected result from the theory of [PRU 07] would have been up to a factor of 1,000, although of the same T^5 slope. Increasing the strain to 1.36% produces much more reduction in $G_{e\text{-}ph}$ and now more closely approaches the scale of the theoretical prediction. This did not have such a strong dependence on degree of strain which suggests there is some additional experimental improvement in the coolers grown on

the 30% Ge virtual substrate over those on the 20% alloy. Overall, the heat flow from the phonon system decreases significantly and it can be useful for cooler applications. By contrast, the measured hole-phonon conductance is a factor of 10 higher than for electrons in unstrained Si at 300 mK, reducing to a factor of 2 at 600 mK. The e-ph coupling is a lot smaller than that in Cu, whereas the hole-phonon coupling is close to that of the metal [RIC 13]. It may therefore be possible to utilize this property of the p-doped material to cool the lattice, in addition to the carriers, or for lattice thermometry.

11.4. Strained silicon Schottky barrier mK coolers

Having established that strain in silicon can be beneficial for reaching low minimum temperatures via electronic cooling, we will now examine SSmS devices fabricated to incorporate a strained layer [PRE 11]. The device cross-section is shown in Figure 11.14(a) for a 20% Ge virtual substrate giving 0.95% strain in the over-lying silicon. The layout is shown in Figure 11.14(b).

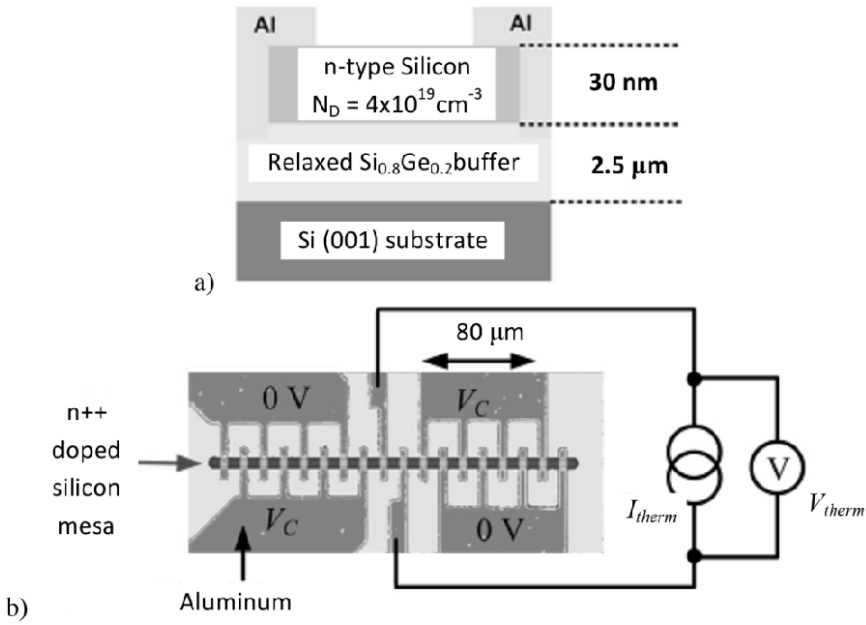

Figure 11.14. *a) Strained silicon electron cooler cross-section. b) The cooler layout. The central mesa is 222 µm long by 6 µm wide and the doped region is 30 nm thick, from [PRE 11]*

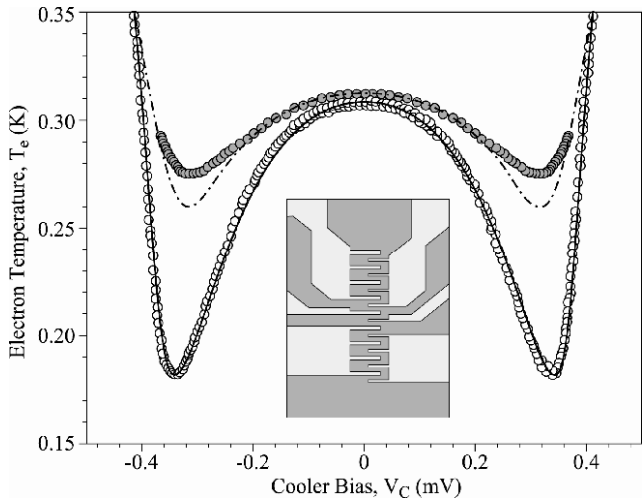

Figure 11.15. *Electron temperature as a function of junction bias in a 0.95% strained Si cooler with Al superconductor and an unstrained Si control starting from a bath temperature of 310 mK*

The device has an array of parallel 6 μm × 6 μm Al (200 nm thick) junctions that are used to cool the electron gas in the long thin central mesa. This geometry both improves the quasi-particle thermalization [LEO 99] and reduces the total resistance of the silicon to help minimize Joule heating. The central junction pair is used as a thermometer to measure the electron temperature in the middle of the mesa. Figure 11.15 demonstrates that electron cooling from a 300 mK bath to 174 mK was achieved in the strained Si device compared with only to 274 mK in the control.

The solid lines in Figure 11.15 are fits to the model developed in Chapter 10, which accounts for the reduced e-ph coupling and sub-gap leakage in the junctions. It can be seen that there is good agreement for the strained cooled, but less good agreement for the control. This could be because the control has a lower tunneling resistance, leading to more power dissipation in the superconductor and therefore quasi-particle heating which is not accounted for in the model.

The performance of the strained Si cooler, expressed as the ratio of final to initial electron temperatures, is seen to be considerably improved over the control in Figure 11.16 for the full range of bath temperatures. The calculated minimum temperatures based on the cooling model are shown by lines, using e-ph coupling of $\Sigma = 5 \times 10^8$ $Wm^{-3}K^{-6}$ in the unstrained (dashed line) and 2×10^7 $Wm^{-3}K^{-6}$ in the strained (solid line) devices, respectively. For these data, the cooling is still limited

by imperfections in the devices, particularly superconductor sub-gap leakage for which the calculations predict significantly better cooling if Γ can be reduced.

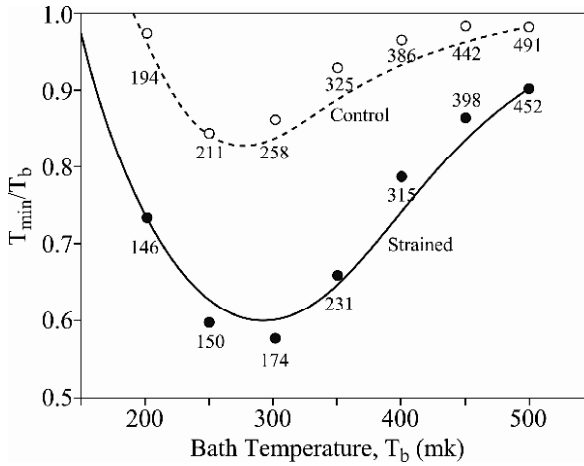

Figure 11.16. *Performance of unstrained control and a 0.95% strained cooler, from [PRE 11]*

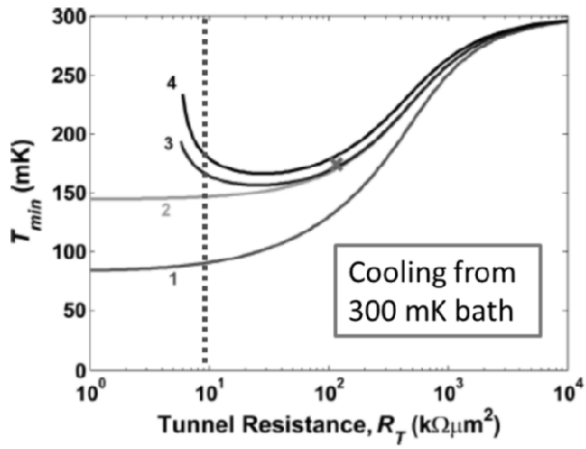

Figure 11.17. *Modeled minimum temperature in a 0.95% strained cooler from (1) balancing lattice heat input to cooling power; (2) including Γ = 0.01Δ; (3) as (2) + Joule heating; (4) as (3) + quasi-particle heating, from [PRE 11]*

From Figure 11.17 the influence of various heating mechanisms can be seen: curve (1) is for an ideal junction with the cooling power P_c matched by lattice heating $P_{e\text{-}ph}$, with tunnel resistance limiting the cooling; in curve (2), with finite Γ, additional heating occurs due to sub-gap leakage; curve (3) adds the effect of Joule heating that becomes dominant at small R_T; finally, inclusion of quasi-particle heating further increases the heating at small R_T when the junction becomes more transparent. Lower sub-gap leakage would pull down the minimum in curves 3 and 4, but only when the tunneling resistance is not too low.

11.5. Silicon mK coolers with an oxide barrier [GUN 13]

11.5.1. *Reduction of sub-gap leakage*

Sub-gap leakage is clearly a major performance limitation. The states induced in the middle of the superconductor gap arise from the interface of the superconductor to the semiconductor, due to the inverse proximity effect. To reduce this, the silicon surface was oxidized in the sputterer prior to deposition of the superconducting aluminum [RIC 14]. As shown in Figure 11.18, this leads to an S-I-Sm-I-S structure, but the oxide layer does not entirely replace the Schottky barrier for tunneling as it is very thin (1.8 nm). The high-doping (8×10^{19} cm^{-3}) results in a very low R_T (1.1 kΩ.μm^2) despite addition of the insulating oxide. Adding this thin oxide layer led to a 15-fold reduction in Γ (Figure 11.19), which greatly reduces the sub-gap leakage in the junctions and allows the use of low-resistance junctions, with commensurate improvements in cooling performance to reach 160 mK from 300 mK.

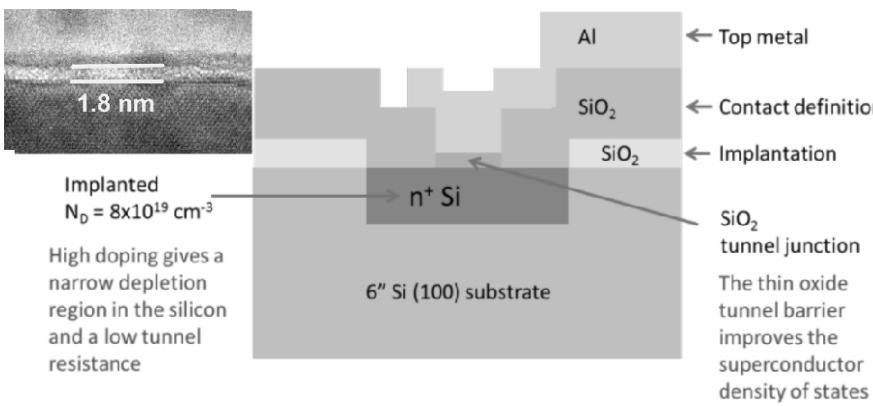

Figure 11.18. *Schematic cross-section of the oxide barrier silicon based cooler design. Inset shows TEM micrograph of the SiO_2 tunnel barrier, with Si below and Al above*

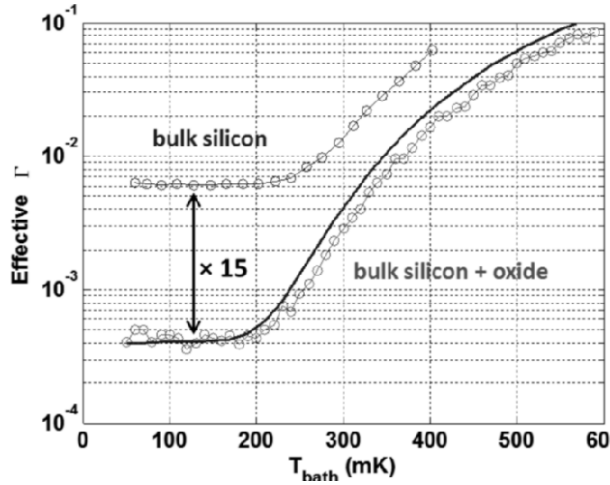

Figure 11.19. *Effective Γ from mid-gap to normal state conductance ratio. Solid line: simple model calculating dI/dV of isothermal cooler junction IV for different T_b*

11.5.2. *Effects of strain*

Finally, the advantages of the reduced sub-gap leakage from the oxide barrier can be combined with the low e-ph coupling of the strained wafers to demonstrate a significant improvement in electron cooling. Using devices grown on a 20%, Ge buffer with similar geometry to those of Figure 11.14, electrons were cooled from 300 mK to 90 mK as shown in Figure 11.20. This is a significant advance on earlier devices and meets a major milestone for electron cooling in strained silicon devices with greater than a factor of three reductions in T_e and reaching below 100 mK. An even larger cooling ratio is available when starting from a lower bath temperature, as shown in the full cooling curve plot of Figure 11.21 and the final comparison of the improvements realized via strain and sub-gap leakage reduction in Figure 11.22. Other routes to further improvement could come from repeating this process with higher strained Si (i.e. on the 30% Ge buffer) and from using higher doping in the silicon to reduce the series resistance, although there is a limit to how heavily the silicon can be doped without disrupting the crystal and losing the strain advantage.

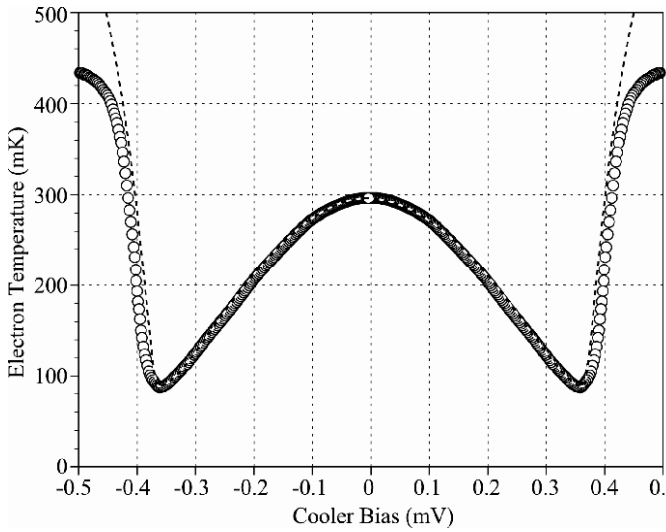

Figure 11.20. *Cooling result of 0.95% strained Al-SiO_2-Si-SiO_2-Al device. The electron temperature is reduced from 300 mK to 90 mK and fits well to the cooling model*

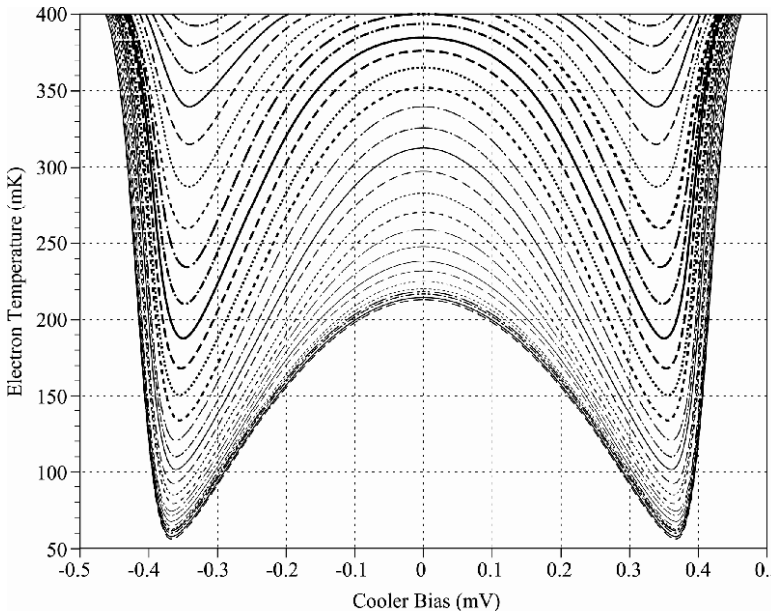

Figure 11.21. *Cooling of 0.95% strained Al-SiO_2-Si-SiO_2-Al device from different bath temperatures as a function of junction bias. The minimum temperatures from the lowest curves may be underestimated due to self-heating of the thermometer junctions*

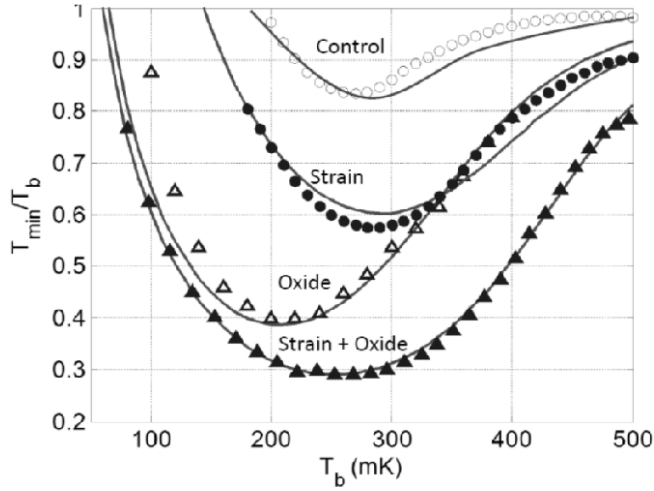

Figure 11.22. *Summary of cooling performance of Al-Si tunneling junctions from different bath temperatures, showing the improvements from strain (0.95%) and reduction in Γ*

11.6. The silicon cold electron bolometer

We now turn to a potential application that depends on cooling just the electronic system and takes advantage of good-thermal isolation from the lattice provided by the low e-ph coupling in strained silicon. Tunnel junction cooling allows an electron gas to be electronically cooled to ultra-low temperatures and when incorporated into a bolometer, very fast detectors are promised with high sensitivity, dynamic range and having high-resolution spectroscopic capabilities. For many years, scientists have been working to realize the great potential of the near-to-far infrared (IR) region of the electromagnetic spectrum for applications in the security, defense, biological, communication, information-technology, medical and, looking to the future, quantum information processing fields. The emergence of a viable THz technology has thus far been limited by the unavailability of sources and detectors with the required combination of performance, ruggedness, ease of use and low cost. With the notable exception of astronomical detectors, which operate at cryogenic temperatures, most of this work across the spectrum concerns the development of a room temperature device technology. While great strides have been made in 300 K THz sources in recent years, detector sensitivity remains severely limited, along with some of the other critical performance parameters like resolving power and dynamic range. Even cryogenic devices generally do not possess the full performance specification needed for the most demanding photometry and imaging applications, and their requirement for expensive and sophisticated cooling.

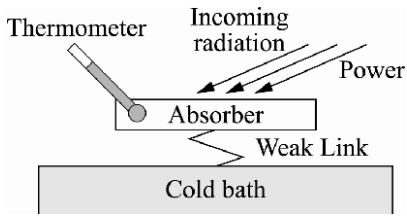

Figure 11.23. *Operation principle of cold electron bolometer*

Bolometers operate by detecting a change in the temperature of an absorber when radiation is absorbed, or by maintaining isothermal conditions using electro-thermal feedback, but this necessarily means that the electron system of the absorber is heated above that of the bath, producing higher noise. In a cold-electron bolometer (CEB) (Figure 11.23), the electron temperature rises when an incident photon flux arrives and it is this change in temperature that is measured.

In a CEB based on electronic cooling, the tunnel junctions are given a DC bias so that the absorber is cooled when biased close to Δ/e resulting in an increase in the responsivity [GOL 01]. The cooling action in the device also enhances the dynamic range and saturation power. Figure 11.24 shows the structure of our first basic (unstrained) Si CEB. The Si absorber is mounted between the terminals of a 150 GHz twin slot antenna, and aluminum is used as the superconductor. The antenna couples radiation and dissipates heat in the heavily n-doped Si. The associated Al-Si Schottky barrier tunnel junctions serve as the thermometer.

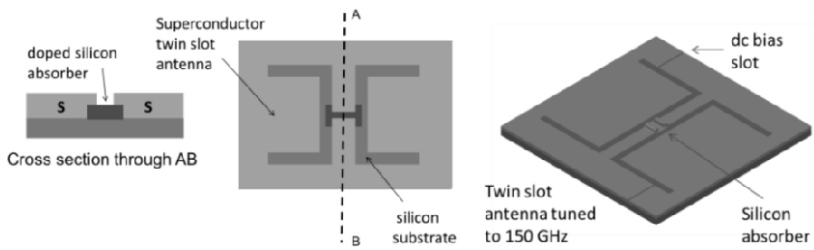

Figure 11.24. *Geometry of our bolometer, cross-section, plan view and 3D view*

The unstrained silicon cold-electron bolometer has been measured at a lattice temperature of 220 mK. The responsivity is shown in Figure 11.25 for varying DC bias of the device. The peak responsivity occurs where maximum cooling is expected (at around $2\Delta/e$, or 0.4 mV) and is 7×10^7 VW^{-1}. The noise equivalent power (NEP) is a measure of the noise background of the device and, in a well-optimized measurement system, is often limited by the phonon noise through

the e-ph conductance. As shown in Figure 11.26, the minimum in NEP occurs at the responsivity maximum and is 5×10^{-18} W Hz $^{-0.5}$ in the absence of radiation. This figure includes junction shot noise, amplifier and phonon noise, all of which could be reduced, and is a respectable initial measurement, comparable with other technologies. Measurements of the overall frequency response to noise of the system suggest a bolometer response time of less than 1.5 μs.

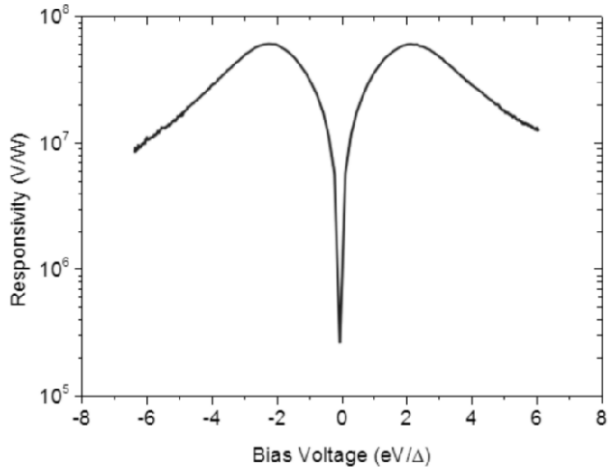

Figure 11.25. *Responsivity of the silicon bolometer as a function of bias*

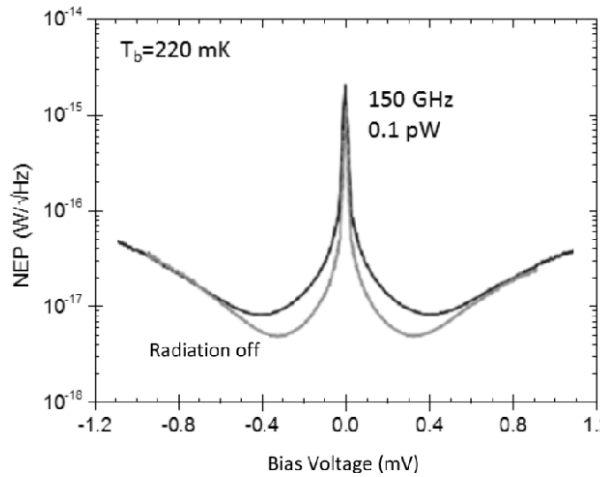

Figure 11.26. *Measurements of the NEP of a Si CEB at a bath temperature of 220 mK, and in the presence of 0.1 pW of radiation. The difference at the minima corresponds closely with the theoretical value of the photon noise*

Similar results were obtained in the strained silicon bolometer, but with a 350 mK phonon temperature, and are compared in Table 11.1. There is a substantial improvement in the strained Si case, both in terms of responsivity and low noise, even though the bath temperature is higher. These devices lack the improved tunnel junctions with oxide barriers, which would yield even better performance. Our tunneling model (discussed above) was used to fit the temperature changes in these devices and shows the cooling power at the bath temperature of 220 mK is just above 1 pW. Calculations were also undertaken of a fully optimized silicon bolometer and predict NEP values in the 10^{-22} W.Hz $^{-0.5}$ range and response times < 1 ns, which would enable single-photon counting and spectroscopy in the THz range, without the need for the normal wavelength dispersive front-end.

	T_b / T_e (mK)	Responsivity (V W^{-1})	Dark NEP (W Hz$^{-1/2}$)	Time constant (μs)
Unstrained	220/(145)	6×10^{6}	3×10^{-16}	<1.0 μs
Strained	350/(190)	5×10^{7}	1×10^{-17}	<1.0 μs

Table 11.1. *Measured bolometer parameters for strained and unstrained Si CEBs*

11.7. Integration of detector and electronics

Many of the noise measurements for the silicon CEB were limited by the performance of the amplifiers used. Amplification at low temperature becomes an essential part of such systems, but the power dissipation of the electronics cannot be allowed to interfere with the cooling process in the refrigeration elements. There is also an issue that the most advanced processing electronics are all designed for room temperature operation. Consequently, a hybrid approach is expected with initial amplification at the lowest temperature bath followed by a second stage at a well-heat sunk region and finally additional computationally intense processing at room temperature.

Silicon BJT transistors suffer from a freeze-out effect at 4 K rendering them rather useless. Hetero-junction bipolar transistors (HBT) do not suffer from freeze-out due to the germanium incorporated into the base [PRE 07], and exhibit lower noise, improved frequency response and higher current gain than at room temperature [KIV 06, CRE 05, WEI 09]. Both setups containing SiGe transistors and SQUIDs [KIV 06, VOI 08] and Si circuits only [PRE 07, VOI 08, WEI 09,

BAR 10, IVA 11] have been demonstrated. Bipolar-CMOS combinations include an operating amplifier with 0.5 μm SiGe BiCMOS technology operating at 4.2 K, using a bipolar input stage and otherwise of complementary metal–oxide semiconductor (CMOS) technology [KRI 06]. The integrated SiGe amplifier design in [BAR 10] can be regarded as state-of-the-art benchmark today. It has 4 GHz bandwidth, 29 dB gain and better than 0.15 dB noise figure with power consumption of 40 mW. It operates down to 24 K and below which it fails.

Many of the designs below those temperatures only use p-type transistors, because they are less prone to carrier freeze than n-type transistors. In an ADC operating at 4.2 K using complementary CMOS [CRE 07], only p-type transistors are used in the input stages and otherwise n-type transistors are used only when they can be biased outside the kink and hysteresis regime.

An interesting new possibility is to use fully depleted silicon on insulator CMOS (FDSOI) for cryogenic amplifiers [KRI 06]. Papers based on a rather old 0.5 μm process demonstrate the compatibility of FDSOI up to DA converter complexity even at 4.2 K [RAH 12]. Ring oscillators have been demonstrated down to 2.8 K with a 180 nm, partially depleted SOI (PDSOI) process [VER 10]. Narrow-line width FDSOI CMOS is now available commercially from ST Microelectronics and GlobalFoundries (28 nm process), but no circuits have yet been demonstrated.

Recent developments of single electron transistors (SETs) [KOP 13] look promising for cryogenic interface electronics. They would have the low dissipation, cryogenic operation and materials compatibility – all very attractive features. However, SETs are still in a rather preliminary phase. Only single transistors, not integrated circuits, hybrid SET-CMOS or SET-SiGe combinations, have been demonstrated so far. Most probably, a CMOS or SiGe output buffer will still be needed to drive the signal out.

11.8. Summary and future prospects

Prior to this work, semiconductor-based electron cooling was limited by the high resistance of tunnel junctions [SAV 01]. Previous studies had shown that as the doping density of silicon was increased; the leakage became worse, negating the use of low-resistance junctions [SAV 03]. We have demonstrated that an in-situ processing technique, prior to deposition of the superconductor, greatly reduces the sub-gap leakage in the junctions and allows the use of low-resistance junctions, [RIC 14] with commensurate improvements in device performance.

Most significantly, cooling from 300 mK to an electron temperature of 90 mK has been demonstrated in a strained silicon device, where the strain serves to increase thermal isolation between the electronic and phonon systems. Up to three decades of reduction in electron-phonon coupling has been measured in strained silicon, as compared to normal metals such as copper (unstrained silicon already has electron-phonon coupling a decade lower than Cu). We have calculated that when combined with the reduction in sub-gap leakage this reduction of the e-ph coupling could allow cooling to 30 mK from 300 mK in ideal junctions; this order of magnitude cooling would be a truly remarkable result which would dramatically enhance the potential of these devices. Going further, calculations predict that if Nb or V were to be used as the superconductor with strained silicon, cooling from 1.3 K to below 100 mK could be possible. Using a multistage device, it is easy to envisage cooling from initial temperatures reached by pulse tube coolers to final temperatures below 10 mK. Of course, there are many technological issues to be overcome before such devices are realized.

The reduction in e-ph coupling also shows promise for dramatic improvements in performance of bolometric detectors for a wide variety of electromagnetic radiation sensing applications using silicon based cold electron bolometers. Because, this is a silicon device, we can confidently expect integration advantages, leading to completely new scenarios in sensing and imaging. The construction of detector arrays, complete with integrated read-out systems, will be greatly facilitated through compatibility with well-developed silicon processing techniques. The modeling of optimized sSi-CEB devices shows that they can deliver an unequalled combination of sensitivity and linear dynamic range, which are important for new applications. Furthermore, the high speed and energy resolution of the device should lead to exceptional performance in single-photon detection, including spectroscopic analysis. Although cryogenic cooling is required, these devices can operate with a lattice temperature as high as 1 K, easily accessible using cryogen-free systems.

Turn-key refrigeration to mK temperatures, enabled here by e-cooling, could facilitate a plethora of exciting developments across several fields such as quantum information processing, where very cold electrons strongly decoupled from the phonons afford an exciting prospect for functional quantum-bit operation. Such mK refrigeration techniques could displace the complex, expensive and bulky dilution and adiabatic-demagnetization refrigerators now in use. There is also great potential to minimize heat loads with an all-Si bolometer array and first stage amplifier (e.g. a single-electron silicon transistor) enabling very considerable scaling down and simplification of heat pumping. As such, its application in environmental monitoring (including space-borne) is a particularly exciting prospect.

11.9. Acknowledgments

The collaboration between partners in Finland and the UK has been essential to the success of this project. Expertise in silicon epitaxial growth at Warwick has been complemented by experience and facilities for device fabrication and low-temperature measurements in Finland and detector characterization at the astronomy department at Cardiff University. The project work has been facilitated by support from a number of funding agencies: RCUK Basic Technology Programme EP/F040784/1 and EPSRC Platform Grant EP/J001074/1; European FP7 Programme under Grant Agreements #228464 (MICROKELVIN, Capacities Specific Programme), and #257375 (NANOFUNCTION); and by the Academy of Finland.

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12

Thermal Isolation through Nanostructuring

12.1. Introduction

Chapters 10 and 11 described the principles of electronic cooling with tunnel barrier junctions and showed how the electron temperature within a cooler device could be reduced by up to an order of magnitude. In this chapter, cooling of a platform will be considered, which requires the electronic coolers to extract heat by coupling to phonons within the platform material. Here, the cooling power of the devices becomes paramount, as opposed to the base temperature that could be reached, and must exceed heat leaks into the platform from the surroundings. This indirect cooling is desirable for systems where electrical isolation from the refrigeration elements is required, such as in quantum information applications or superconducting transition edge sensors (TESs), or where a quite different type of object is to be cooled.

12.2. Lattice cooling by physical nanostructuring

A key feature of electronic refrigeration is to control the phonon heat leak from the thermal bath to the device being cooled. At low temperature, the acoustic phonon wavelength approaches 1 μm, so it is relatively easy to produce nanoscale structures that are smaller than the phonon wavelength and so lead to quantization of the phonon energy spectrum. Then, this can then be utilized to control the phonon

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Chapter written by David LEADLEY, Vishal SHAH, Jouni AHOPELTO, Francesc ALZINA, Emigdio CHÁVEZ-ÁNGEL, Juha MUHONEN, Maksym MYRONOV, Androula G. NASSIOPOULOU, Hung NGUYEN, Evan PARKER, Jukka PEKOLA, Martin PREST, Mika PRUNNILA, Juan Sebastian REPARAZ, Andrey SHCHEPETOV, Clivia SOTOMAYOR-TORRES, Katerina VALALAKI and Terry WHALL.

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heat leak by fabricating a tunneling refrigerator on a two-dimensional (2D) membrane or one-dimensional (1D) nanowire. By placing the object to be cooled on a membrane that is thermally isolated from the environment as far as possible, it can be cooled via the membrane by "cold fingers" of the normal metal (or semiconductor) that extend from the tunnel junction coolers onto the membrane, as shown schematically in Figure 12.1 where four SINIS coolers cool an Si_3N_4 membrane on which a TES sensor is mounted.

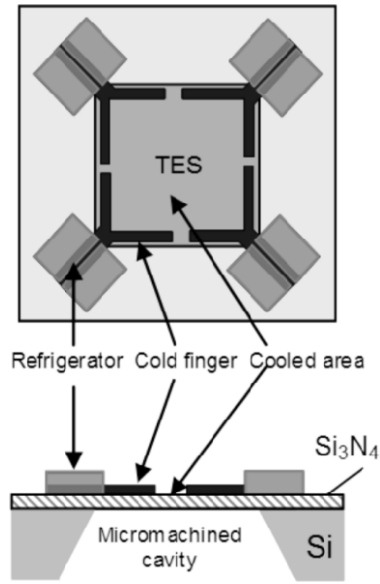

Figure 12.1. *Schematic view of an electronically cooled membrane carrying a transition edge sensor. The SINIS refrigeration elements (in the corners) include cold-finger extension of the cooled normal metal (black) that extract heat from the membrane*

The cooling power of such a system is typically some tens of picowatt, which is sufficient to cool a thin membrane, provided the heat leaks are small. Figure 12.2 shows a finite element simulation of the lattice temperature on a membrane such as shown in Figure 12.1. One way to reduce those leaks is to perforate the edge of the membrane and so reduce conduction into the edge, although this is technically difficult to achieve without damaging the device. In the first demonstration of membrane cooling, by the Aalto group [LUU 00], a small silicon nitride membrane was isolated from the thermal bath by four thin bridges, approximately 200 μm long and 5 μm wide, as shown in Figure 12.3. With only a picowatt level of cooling power, the temperature of the platform was reduced by a factor of two, from 200 mK down to 100 mK, and from 300 mK, a ×0.7 reduction was achieved.

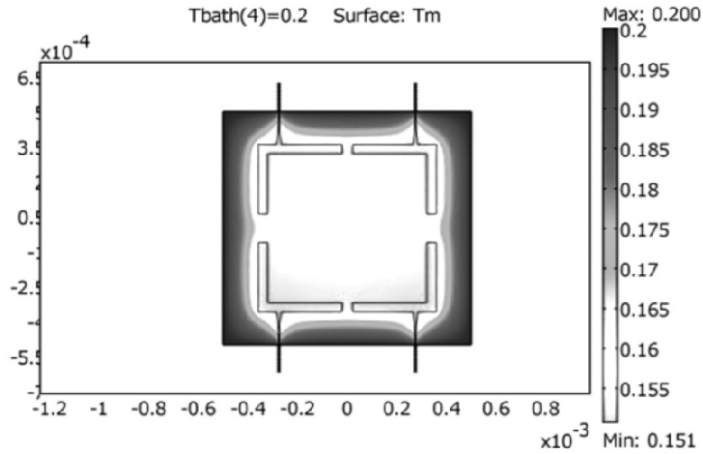

Figure 12.2. *FEM simulation of temperature on an Si_3N_4 membrane that is being cooled by four SINIS refrigerators from a bath temperature of 300 mK with 30 pW of cooling power*

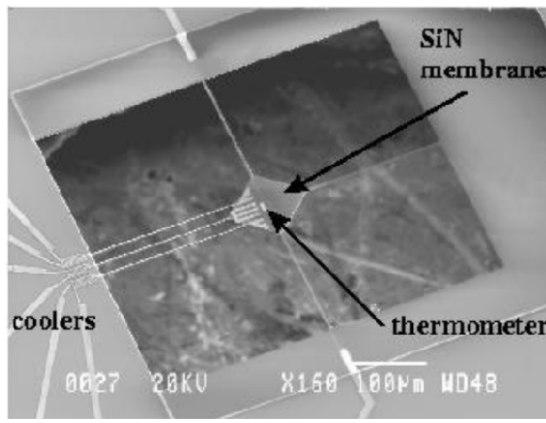

Figure 12.3. *Refrigeration of a small volume membrane thermally isolated by thin bridges. Cooling by a factor of two from 200 to 100 mK was achieved [LUU 00]*

The NIST group demonstrated that an Al TES (Figure 12.4), designed for X-ray detection, could be cooled on an Si_3N_4 membrane from 300 mK down to 190 mK, with a resulting improvement in TES performance by reducing its noise equivalent power [MIL 08]. This set-up had a larger cooling power of approximately 100 pW, which was tested by inducing a 22 pW heating power to the membrane and observing a temperature increase of 7 mK.

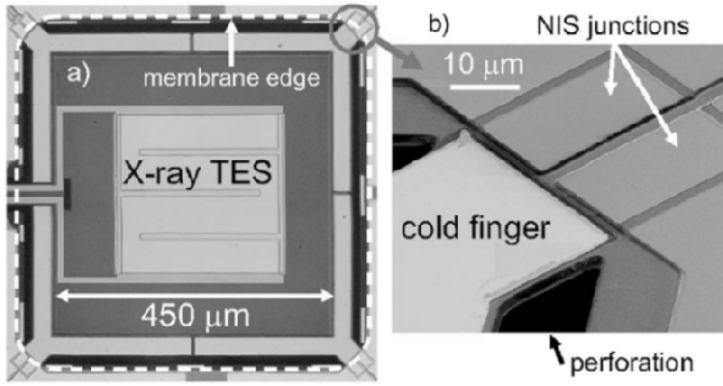

Figure 12.4. *a) Refrigeration of a TES on an Si3N4 membrane. The membrane is cooled by cold fingers that extend from NIS junctions, which is shown in more detail in b) [MIL 08]*

This membrane design was also used to cool the first macroscopic object – a 200 µm sided Ge cube [CLA05] (Figure 12.5), although the temperature only dropped modestly from 300 to 240 mK. More recently, NIST reported phonon cooling over a similar range (from 290 to 256 mK) of a much larger (1.9 cm^3) block of copper, with a cooling power of 700 pW generated at 290 mK [LOW 13]. The membrane, shown in Figure 12.6, was supported by eight 20 µm wide × 60 µm long legs to reduce thermal connection to the bath. Each leg is cooled by a pair of 7 µm × 32 µm NIS junctions that include a 500 nm layer of AlMn on top of the NIS junction as a quasi-particle trap. The AlMn cold fingers have additional Cu and Au layers deposited on them to increase their thermal conductivity. The authors of [LOW 13] forecast that cooling to 100 mK would be possible with a similar system that was optimised for cooling, rather than ease of fabrication.

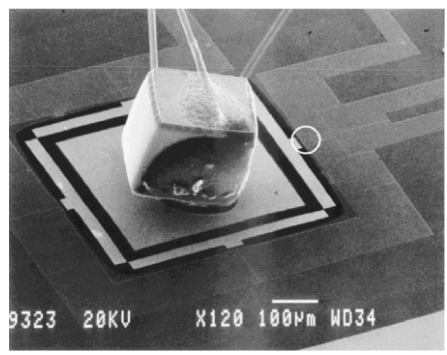

Figure 12.5. *Refrigeration of a bulk Ge cube with SINIS junctions. From T_b = 300 mK, the junctions were at 230 mK and a thermometer on the cube at 240 mK [CLA 05]*

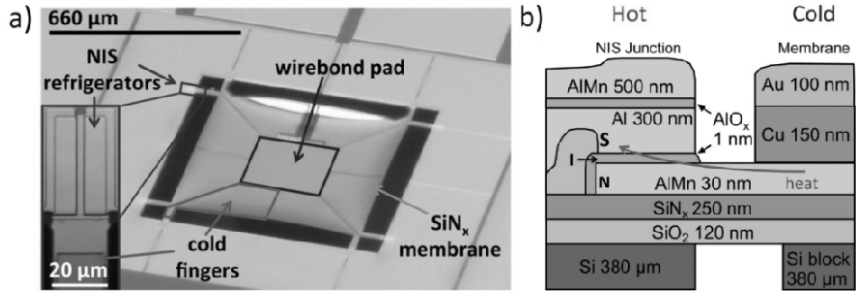

Figure 12.6. *a) Micrograph of a 370 nm thick membrane cooled by NIS junctions. Inset: enlarged view of a pair of NIS refrigerator junctions. b) Cross-sectional view showing critical nanoscale dimensions. Heat is transferred from the membrane to the superconductor, as shown by the curved arrow [LOW 13]*

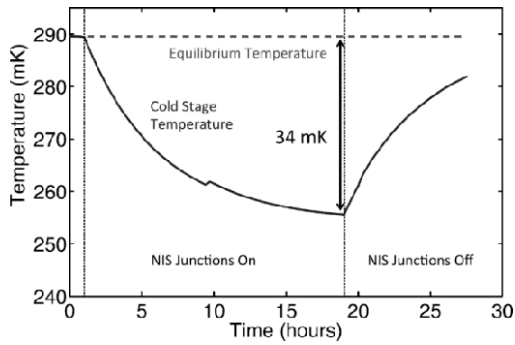

Figure 12.7. *Measured temperature of the suspended Cu stage as a function of time from turning the NIS coolers on at 1 h and off again after 18 h [LOW 13]*

In their most recent version of the SINIS cooler [NGU 13], the Aalto group have suspended a Cu normal metal between superconducting Al electrodes (Figure 12.8). These coolers have a junction size of 70 × 4 μm^2 and also make use of AlMn quasi-particle traps. These junctions can provide cooling power of up to 400 pW at 300 mK for an input power of 2 nW, as shown in Figure 12.9. The arrow marks the bath temperature at 250 mK, where sample C cools down to below 100 mK.

Four of these large coolers have been applied to cooling the Si_3N_4 membrane platform, as shown in Figure 12.10. Note how the cold finger extensions wrap around regions of decreasing size to protect the central region from heat leaks. Although in this case the Si_3N_4 membrane was not perforated at the edges, cooling of a thermometer in the central platform (curve labelled 'phonon on membrane' in Figure 12.10) was measured to below 200 mK from a bath temperature of 300 mK.

The electron temperature in the cold fingers, measured at the junctions (dotted curve), was 150 mK. Meanwhile, a thermometer placed on the surrounding chip (dashed curve) showed slight warming above the bath temperature as heat was being dissipated from the superconductors.

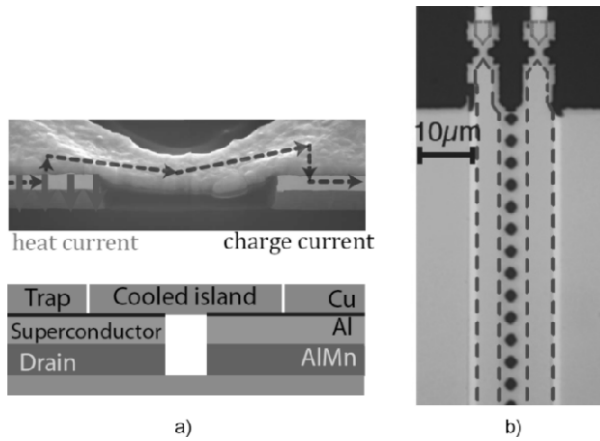

Figure 12.8. *a) SEM cross-section of the SINIS cooler junction, shown schematically below. b) Top view of the device. The dashed lines show the junction regions, with the normal metal extending to points at the top where temperature is measured [NGU 13]*

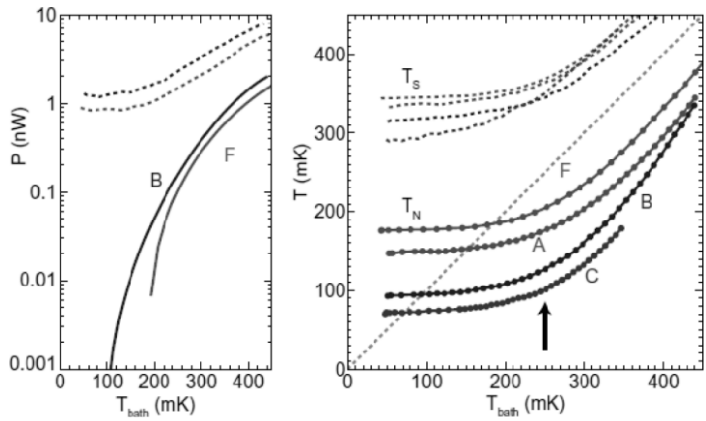

Figure 12.9. *a) Cooling power (solid lines) and input power (dashed lines) of two coolers as a function of the bath temperature. b) Calculated superconductor electron temperature (dashed lines) and measured normal metal temperature (solid lines) at optimum bias [NGU 13]. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices1.zip*

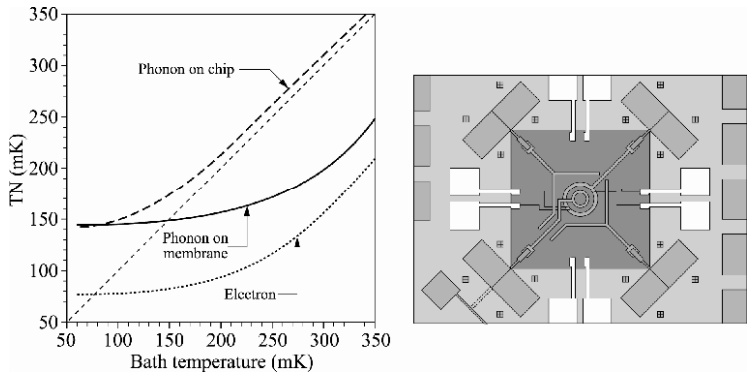

Figure 12.10. *Cooling of a non-perforated membrane by four SINIS junctions attached to cold fingers that are arranged to shield a central region [NGU 14]*

Another geometry that has been studied is in the form of a nanoscale beam, where the phonon dimensionality can be reduced to 1D. In this case, the heat flow from the lattice through electron–phonon coupling follows a T^3 power law, instead of the T^5 power law in three dimensions (3D) [HEK 08]. Coupling is between the electrons and the longitudinal phonon modes, since the electrons do not couple to the transverse flexural modes of the beam. The Helsinki group showed how a very small silicon nitride beam that has been physically suspended away from any substrate can be dramatically cooled to 40 mK, as depicted in Figure 12.11 [KOP 09]. While the experiment was not directly sensitive to any dimensionality or localization effects of the phonons in the beam, the authors did observe a power law of 2.8 at the lowest temperature and attributed this to the 1D–2D phonon scattering at the bridge–bulk interface. This geometry is not really amenable to supporting a payload but can be appropriate if the beam itself can be the sensor.

12.3. Porous Si membranes as cryogenic thermal isolation platforms

12.3.1. *Porous Si micro-coldplates*

Thick porous Si layers on the Si wafer constitute alternative structures that could replace the rather fragile silicon nitride membranes for use as thermal isolation platforms. The thermally isolating substrate is one of the most important building blocks of a cooling device. One of the most promising substrates in this respect is a thick porous Si layer locally formed on the Si wafer. Following the pioneering work of NCSRD/IMEL and the corresponding patent [NAS 98], porous Si has been demonstrated to be an excellent thermal isolation material on the Si wafer and its thermal conductivity at room temperature was studied by several groups. The voids

within a nanostructured porous Si layer and the low dimensionality of the highly porous Si skeleton serve to inhibit thermal transport within the layer. Thus, porous silicon shows excellent thermal isolation properties. In addition, it is compatible with CMOS processing [NAS 00]. Although it has not been used in cooled device applications so far, its excellent thermal isolation properties were already demonstrated at room temperature as a local heating platform on Si [TSA 03, PAG 04, TSE 03, KAL 03]. It has been extensively used in the form of porous Si membranes or thick films on a bulk Si platform in Si thermal sensors [KAL 99, KAL 02].

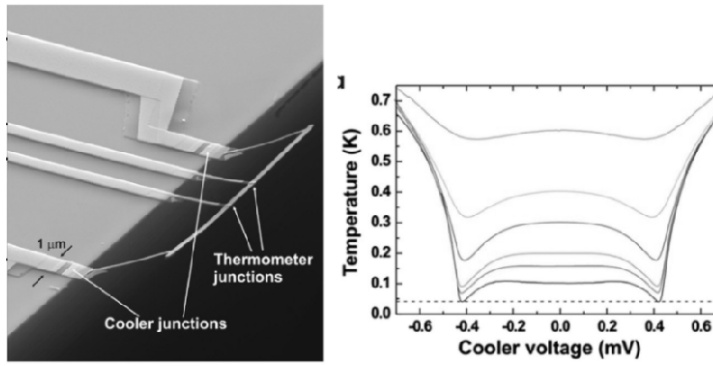

Figure 12.11. *SEM of a SINIS cooled suspended nanobeam. The copper normal metal strips are on top of the superconducting Al (seen as a darker grey). Cooler junctions are at the edge of the substrate, thermometer junctions are at the centre of the beam measuring lattice temperature at T_b = 50, 160, 200, 300, 400, 600 mK and dashed line corresponds to 42 mK [KOP 09]*

Porous Si is fabricated by electrochemical dissolution of bulk crystalline Si. Its properties depend on the electrochemical conditions used and the type and resistivity of the Si substrate. The structure and morphology of porous Si determines its electrical and thermal conductivity. Its thermal conductivity was extensively studied at room temperature using different techniques, including micro-Raman scattering [LYS 99], optical pump and probe measurements [BER 01], scanning thermal probe microscopy [LYS 00], the photoacoustic technique [BEN 97] and the dc method [LI 99, TSA 03], and has been modeled extensively [FED 08, CHU 11, NAN 06, GU 07]. Nanostructured porous Si shows a thermal conductivity similar or lower than that of SiO_2 at room temperature, with the additional advantage that very thick membranes (several microns or hundreds of microns) can be prepared. A thick porous Si layer on the Si substrate shows advantages including robustness and support for epitaxial overgrowth. Consequently, a simple and very robust micro-hotplate is a thick porous Si layer with the adequate structure and morphology, which in this application will become a “micro-coldplate”. For further

improved thermal isolation, a cavity can be simply fabricated underneath the porous structure by electrochemistry, keeping the planar topography and having excellent mechanical stability due to the large membrane thickness.

12.3.2. *Porous Si thermal conductivity*

The thermal conductivity of porous Si at room temperature has been studied by different groups; however, very little work has been devoted to the low temperature thermal conductivity of this material. There is a significant scattering between the values of porous Si room temperature thermal conductivity due to the fact that this property depends on the structure and morphology of porous Si, which changes with the electrochemical conditions used for its formation and the type and resistivity of the Si wafer used. The values in the literature for porous Si fabricated from p-type Si range from 0.03 to 7.33 $Wm^{-1}K^{-1}$ at room temperature for porosities of 89–45%, respectively [GES 97, SRI 07]. On the other hand, for PSi from (100) p-type wafers with resistivity in the range of 10–20 mΩ·cm, the reported thermal conductivity values range from 0.3 to 80 W/m·K for the as-formed material at room temperature, while this is limited in the range of 0.3–2.7 $Wm^{-1}K^{-1}$ for slightly oxidized material samples [LYS 99, DRO 95, BEN 97, MAC 99]. Low temperature measurements were previously performed only down to 40 K.

At NCSRD/IMEL, porous Si layers of different thickness, porosity, morphology and structure were fabricated using electrochemistry [VAL 13] and their thermal conductivity was determined in the temperature range 20–350 K by the dc method. An example of porous Si material that was studied in detail was a sponge-like porous Si layer with 60% porosity. The thickness of the layer was 40 μm. A schematic representation of the local porous Si layer on the Si wafer is shown in Figure 12.12, while in Figure 12.13, a cross-sectional scanning electron microscope (SEM) image of the porous Si layer used in [VAL 13] is depicted. The local porous Si layer on the Si wafer had high porosity and was composed of Si nanocrystals and nanowires interconnected in a porous Si skeleton. The material was nanostructured with sponge-like morphology.

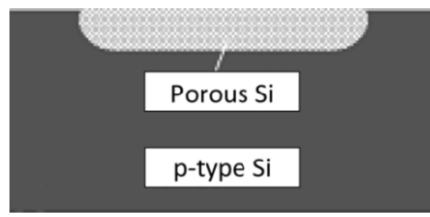

Figure 12.12. *Schematic representation of the local porous Si layer on the Si wafer*

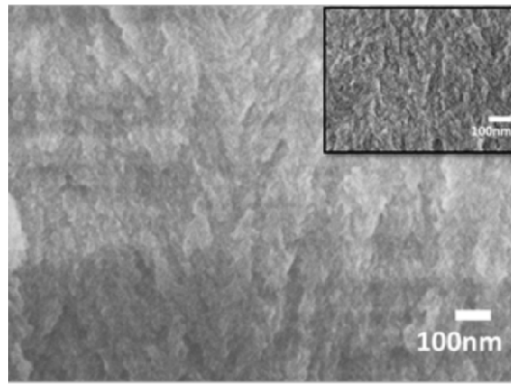

Figure 12.13. *Cross-sectional SEM image of the porous Si layer used in this work. The material is nanostructured with sponge-like morphology [VAL 13]*

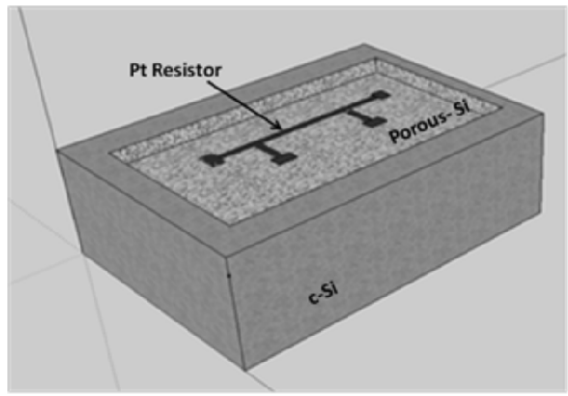

Figure 12.14. *Test structure used for the determination of the thermal conductivity of porous Si with the dc method. A Pt resistor is integrated on top of the porous Si layer with corresponding pads for four-point probe measurements [VAL 13]*

The test structure used for thermal conductivity measurements is illustrated in Figure 12.14. It includes a Pt resistor integrated on top of the porous Si layer with corresponding pads for four-point probe measurements. A similar resistor is integrated on oxidized bulk Si for use as a reference.

Simulations were performed using 3D finite element modeling with the Comsol Multiphysics software. The steady-state heat conduction equation was solved. The porous Si layer was considered as an isotropic and homogeneous material on bulk crystalline Si. The resistor temperature at zero-bias and that obtained after heating

with a given power were the boundary conditions used. The heating power per unit volume was calculated by assuming negligible radiation losses and self-heating phenomena, which is a good approximation for the current density used. An example of simulations is shown in Figure 12.15, illustrating the temperature distribution within a 40 μm thick porous Si layer at 350 K.

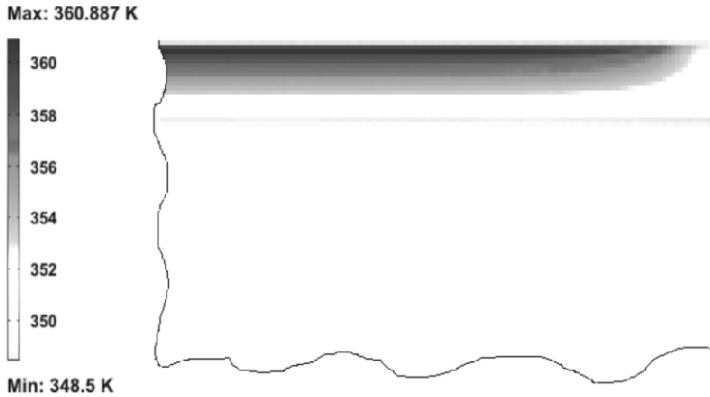

Figure 12.15. *Temperature distribution within a 40 μm thick porous Si layer at 350 K, extracted using Comsol Multiphysics software [VAL 13]*

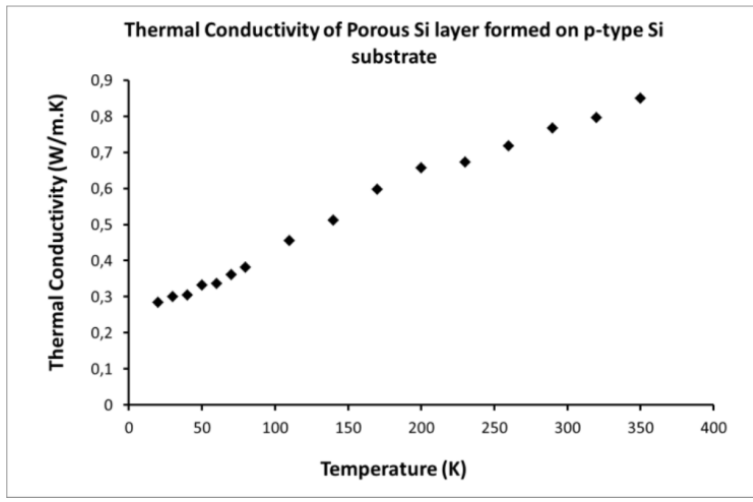

Figure 12.16. *Thermal conductivity of porous Si in the temperature range 20–350 K [VAL 13]*

The thermal conductivity of sponge-like porous Si with 60% porosity, fabricated as described above, is shown in Figure 12.16 in the temperature range from 20 to 350 K [VAL 13]. The reduced thermal conductivity of porous Si is attributed to its low dimensionality and voids within the porous structure. In Figure 12.17, a comparison is made between the thermal conductivity of porous Si and that of bulk crystalline Si. It is shown that the thermal conductivity of porous Si is more than four orders of magnitude lower than that of bulk crystalline Si at cryogenic temperature, which makes this material very appropriate for use as a local thermally insulating substrate on the Si wafer.

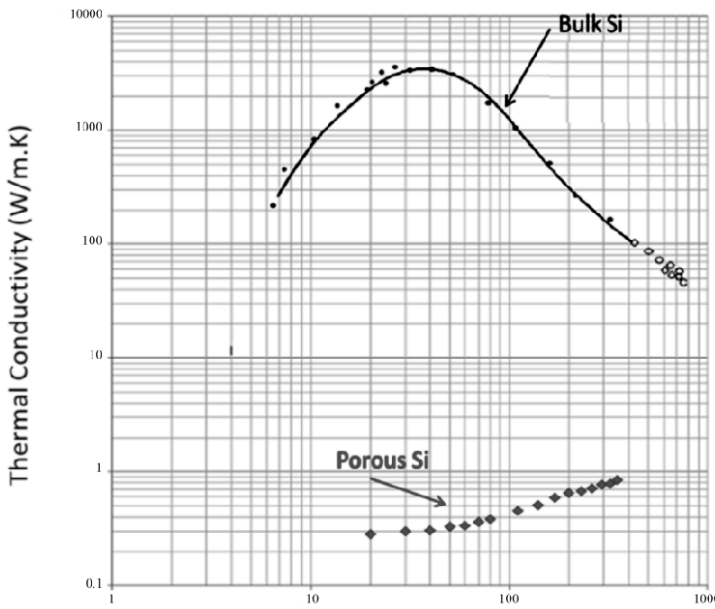

Figure 12.17. *Comparison of porous Si thermal conductivity (data from [VAL 13]) with that of bulk crystalline Si (data taken from [GLA64])*

In conclusion, the thermal conductivity of nanostructured porous Si layers was determined in the temperature range 20–350 K. It was demonstrated that it is more than two orders of magnitude lower than that of bulk crystalline Si, which makes it very appropriate for use as a local thermally insulating substrate on the Si wafer.

12.4. Crystalline membrane platforms

Crystalline membranes have a number of advantages over amorphous materials as platforms for cooling a payload: the greater structural integrity of a crystal means that thinner, and so less thermally massive, structures can be used for the same mechanical strength; the surface tends to be smoother; and there is the possibility to epitaxially grow complete device structures on the platform. Crystalline materials will, however, have a greater thermal conductivity than amorphous or polycrystalline material, meaning that heat is more easily transported through the platform. Although this does mean the thermal connection between cold fingers and payload is better, it also means that heat leaks will be enormous unless very thin membranes are used and steps taken to reduce conduction through the membrane edges. Here, we will consider some aspects of thin Si and Ge membranes.

12.4.1. *Strained germanium membranes*

A thin, flat and single-crystal germanium membrane could be an ideal platform for mounting sensors or to integrate photonic and electronic devices through standard silicon processing technology. The disadvantages of bulk crystalline Ge compared to Si wafers have plagued the development of Ge-based electronics: they are more brittle, heavier and more costly. Many of these problems can be overcome by growing a thin Ge layer epitaxially on a bulk Si wafer [SHA 11]. A two-temperature growth method was used, whereby a thin initial low-temperature deposition of Ge absorbed all the lattice mismatch and a subsequent thicker (~1 μm) layer grown at higher temperature produced virtually defect-free relaxed material. Two methods of producing Ge membranes from this starting material have been developed [SHA 12, TRU 14]. Figure 12.18 shows the process of [SHA 12] making a suspended Ge membrane by underetching the patterned Ge layer with an anisotropic TMAH etch. Structures such as the spider-web shown in Figure 12.19(a) have been produced, which could be used for thermal isolation of a cooled bolometer [GRI 00], with cold fingers following the web as shown in Figure 12.19(b).

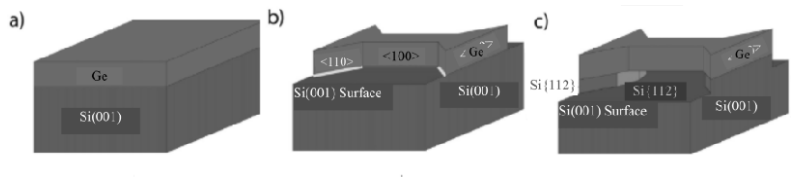

Figure 12.18. *Fabrication of underetched Ge membrane: a) the Ge-on-Si layer prior to patterning, b) the structure after lithography and dry etching and c) the suspended structure after anisotropic underetching [SHA 12]*

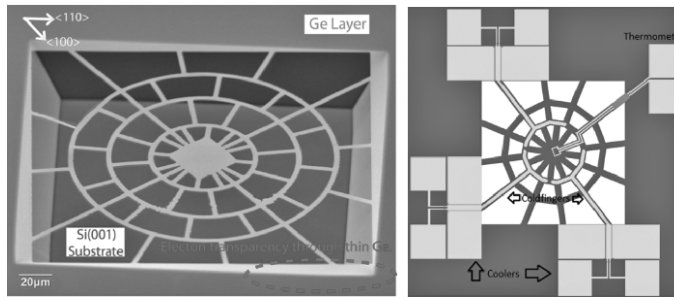

Figure 12.19. *a) SEM of etched, suspended Ge spider web; pale areas are partially electron transparent in the thinned regions. b) Schematic design of a SINIS cooled bolometer on a spider web platform*

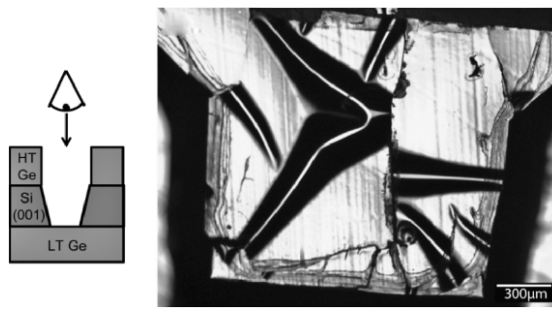

Figure 12.20. *a) Schematic profile for the LT Ge membrane with nominal thickness of 700 nm. b) DIC Nomarski imaging of the etched surface of the compressive Ge layer*

In a second approach [TRU 14], Ge layers were grown on either side of a double-side polished, thin Si substrate. On the "top" side, the Ge is deposited at high temperature that leads to a net tensile strain. (This is because the Si and Ge are fully lattice matched at the growth temperature, but have different thermal expansion coefficients so the Ge becomes tensile strained as the layers contract.) On the "bottom" side, the Ge is grown at a lower temperature, resulting in a compressively strained layer. The wafer is then etched from either the top or bottom face to produce a membrane. Figure 12.20 shows that the compressively strained membrane is rough and buckled, whereas the tensile strained membrane in Figure 12.21 is extremely smooth, with a surface roughness measured by atomic force microscopy (AFM) to be approximately 2 nm. These tensile strained Ge membranes can be produced with thicknesses from 60 nm up to 700 nm and areas up to 4 mm^2.

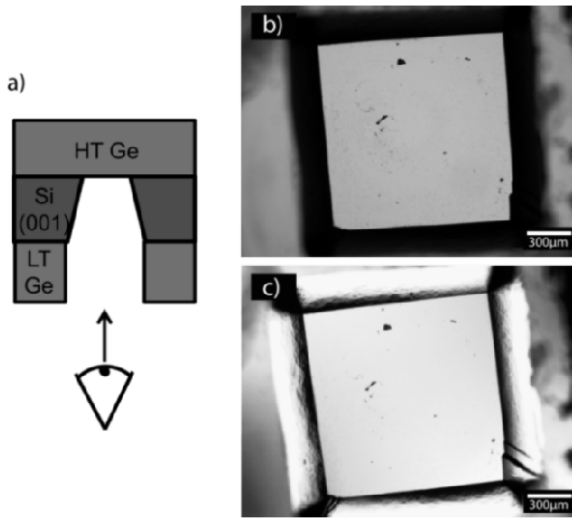

Figure 12.21. *a) Schematic profile for the HT Ge membrane; b) optical imaging of the etched surface of the tensile strained Ge layer; c) DIC Nomarski image of the same sample*

12.4.1.1. *Electrical isolation*

Although Ge layers grown epitaxially on Si (001) can be almost fully relaxed, with sub-nm roughness and low defect densities, they still suffer from electrical leakage by conduction through the dislocation network present at the interface [HES 92, SHE 99, LAN 04]. Most research has focused on reducing the threading dislocation density, but surface-to-surface conduction could also be prevented by removing the misfit dislocations [SHA 12]. To test this, two van der Pauw structures were fabricated from intrinsic Ge-on-Si, where one structure received the full processing so that the cross is suspended and the bulk pads are anchored to the substrate, as shown in Figure 12.22, and the other structure was not underetched to act as a control.

The variation of resistivity with temperature is shown in Figure 12.23. Above 150 K, the conductivity of the Si(001) substrate dominates in both cases. From 150 to ~90 K, free carriers in the Si substrate freeze out [SZE 07] and the resistivity increases. From 90 to 30 K, the resistivity of the two curves differs. Here, conduction is occurring within the Ge layer for both samples, but the additional conduction in the dislocation network further reduces the resistance of the unsuspended sample. In the suspended sample, the dislocation network has been etched away and no longer provides this conduction path. Below 30 K, carrier freeze out in the Ge is expected [MYR 05]. Only a minimal resistivity shift is

observed in the bulk Ge-on-Si sample, since conduction is dominated by transport through the misfit dislocation network, whereas the suspended sample shows a 100-fold increase in resistivity as its major conduction path is closed. Compared to a similar study in bulk Ge with induced dislocations [KOZ 93], the suspended Ge layer is exhibiting the typical conduction and temperature dependence consistent with transport dominated by impurities at a level of approximately 10^{16} cm^{-3}.

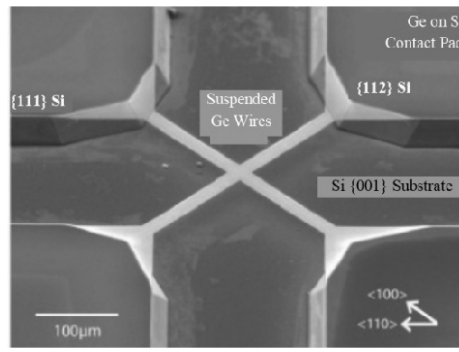

Figure 12.22. *Suspended van der Pauw cross with 20 µm wide arms made of up 1 µm thick undoped Ge*

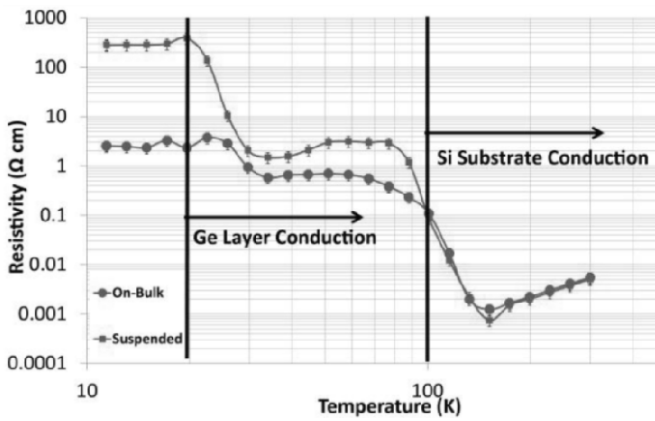

Figure 12.23. *Resistivity of the suspended (upper curve) and bulk (lower curve) crosses*

This result demonstrates that the Ge membrane can be produced with the misfit dislocation network removed, yet the tension remains because the membrane is

connected to the surrounding Ge that is tied to the Si support. This is further confirmed from high-resolution X-ray diffraction measurements of the tension in the membrane [SHA 14]. Scans across the membranes in different directions showed that the strain was isotropic. In addition, Bragg peaks arising from diffraction of the membrane had a narrower line profile than those from the surrounding material, which was interpreted as being due to removal of the additional scattering from the defected interface region in the case of the membrane.

12.4.1.2. *Membrane resonance*

Knowledge of the mechanical properties of these membranes is key to producing useful MEMS-related devices [BUR 90]. High Q-factors are desirable when the membranes are to be used as mechanical structures, whereas robustness to shock and mechanical stability (low Q) are more important for Ge optoelectronic and electronic devices, regardless of the resonant membrane behavior. The vibrational properties of Ge membranes can be measured using a piezoelectric transducer to actuate the vibration in combination with laser interferometry for detection [TRU 14].

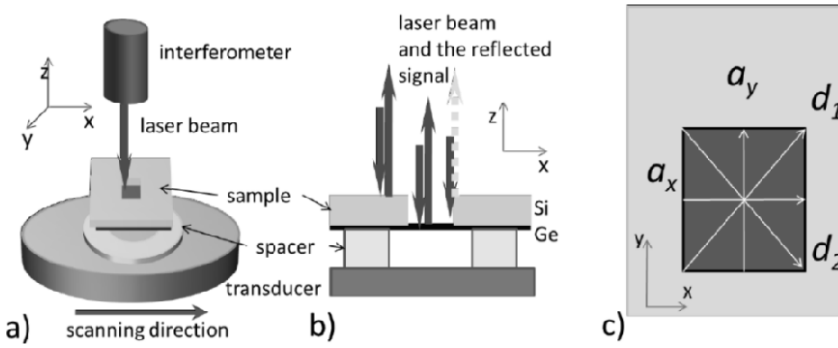

Figure 12.24. *The experimental arrangement for detecting resonance in the Ge membranes: a) transducer and sample in the vacuum chamber; b) close-up with spacer for free membrane movement; c) scanning directions across the membrane are shown*

For a 700 nm thick Ge membrane, the resonant frequencies of several modes were used to measure the residual tensile stress in the membrane, and the Q-factors investigated as a function of pressure from atmospheric to 5×10^{-4} mbar and frequencies up to 400 kHz [TRU 14]. The expected vibrational modes for a square membrane can be calculated and are shown in Figure 12.25. These modes can be detected in two ways: first by detecting at a fixed point and varying the frequency to find when this point is an anti-node. Figure 12.26 shows the resonant frequencies of a 700 nm thick Ge membrane.

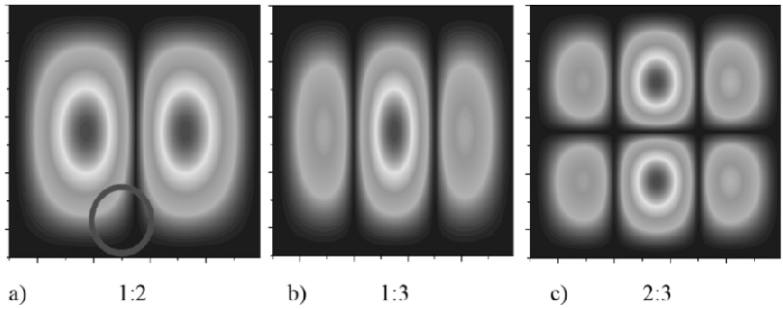

Figure 12.25. *Calculated membrane displacement profiles for 1:2, 1:3 and 2:3 pure vibrational modes. The circle in a) indicates the scanning beam size. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices1.zip*

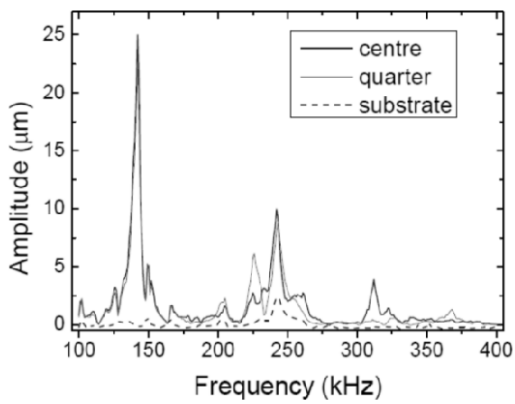

Figure 12.26. *The response of a 1 mm^2 Ge membrane to excitation at different frequencies, measured at points on the membrane where the maxima for odd (centre) and even (quarter) modes are expected. The substrate response (dashed line) is also included. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Second, with these fixed frequencies, scans were performed across the membrane in the directions shown in Figure 12.24(c), with the results shown in Figure 12.27. The oscillations of the membrane are clearly evident, with an amplitude of some hundreds of nanometers. Scans in perpendicular directions are similar (Figure 12.27), which shows there is not any significant stress anisotropy in the membrane. The fundamental 1:1 mode, with no nodal lines, appears in all the scans at 142 kHz. The mode at 225 kHz can be identified as a 2:1 mode, with a nodal line parallel to the a_x direction (Figure 12.25(a) rotated by 90º). The 312 kHz mode is a 3:1 dominant mode and the similar one at 322 kHz behaves like an interference of 1:3 and 3:1 modes, with equal contributions from each. This mode

splitting is a consequence of some small anisotropy in the membrane boundary conditions. From the frequencies of the observed vibrational modes, the stress in the membrane was estimated to be 0.22 GPa, slightly larger but similar to the value estimated from the lattice mismatch of 0.18 GPa.

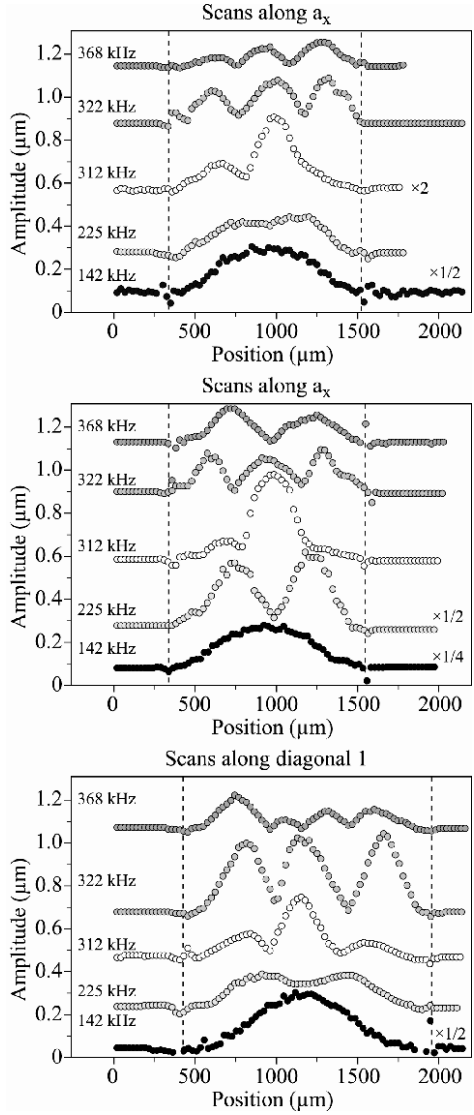

Figure 12.27. *Displacement profiles at the membrane resonant frequencies, showing motion consistent with the fundamental 2:1, 1:3, 2:3 and 3:2 modes with increasing frequency. Curves are offset, with a multiplication factor shown. Vertical lines indicate membrane edges*

The Q-factor of the membrane can be found from the full width half maximum (FWHM) of peaks in Figure 12.26. For the fundamental mode, it increases monotonously as the pressure is reduced, reaching Q = 3240 at 5×10^{-4} mbar. This is lower than values reported for poly-Ge and Si-Ge membranes [MAD 94], as might be expected as the Ge membrane has very low residual stress (high stress is associated with higher Q factors). These relatively low Q-factors mean energy is dissipated in the membrane and can benefit applications where high-amplitude vibrations are to be avoided. For the spider-web structures in Figure 12.19(a), with less rigid support to the edges of the central platform, even lower Q-factors would be expected and these could be extremely useful vibration isolation platforms.

In summary, a relatively simple technique has been developed to make crystalline and flat Ge membranes with thicknesses in the range approximately 50–1,000 nm. Since these membranes are produced by epitaxial growth, there is precise control of the Ge membrane thickness and, being single crystal, they can be used as platforms for other heterostructures. Tensile strain in the membrane is essential for the final quality and this strain was studied by both high-resolution X-ray diffraction (HR-XRD) and ultrasonic vibration. No significant stress anisotropy was detected using either technique, which means the platforms would be suitable for an array of devices or sensors that all need to be in the same stress environment, to be mounted on. By suspending the epitaxial Ge, the crystalline quality was improved by removing the misfit dislocation network from the Si/Ge interface. This improves the mechanical, optical and electrical properties of the suspended material. The membranes are robust against shock, and it can be seen that their main modes of vibration are well above frequencies commonly found in the environment (usually below 40 kHz). The membranes have many desirable qualities such as strain homogeneity, sub-nm roughness and a low Q-factor, which all suggest that they could be ideal device and/or integration platforms.

12.4.2. *Thermal conductance measurements in Si and Ge membranes*

In thin membranes, the phonon confinement can affect the thermal transport and significantly reduce the thermal conductivity (as discussed in section 7.2). The first experimental observation of confined acoustic phonons in nanometer-scale membranes was reported in 1987 in suspended 20 nm-thick Au films [GRI 87]. One year later, Fasol used Raman scattering spectroscopy to detect confinement of optical phonons in 10 monolayer thick AlAs/GaAs/AlAs [FAS 88]. Other works related to free-standing membranes have been reported in 100 and 200 nm Si_3N_4 films [ZHA 03], 30 nm Si films [SOT 04] and recently in Si films with thickness range from 8 to 400 nm [CUF 12]. These works have demonstrated a significant modification of the acoustic dispersion relation in confined systems. The in-plane thermal conductivity is specifically important in a multilayered thin film structure

where cross-plane thermal conductivity is usually very low. Although it can be determined by the 3ω method, the flow of the thermal energy in the cross-plane direction complicates the profiling. Several methods minimizing the effect of cross-plane heat conduction can be employed, especially when the in-plane thermal properties are of primary concern [JU 99a, JU 99b, CHE 97]. The membrane method utilizes strips of electrical heaters and temperature sensors fabricated on top of the nanostructure [ESP 03, CAH 03] (see Figure 12.28). Pioneering thermal measurements on free-standing membranes in the sub-Kelvin regime [LEI 98] reported heat transport and thermal relaxation times in 200 nm Si_3N_4 membranes. Years later, further works followed in the same material and temperature regime [KÜH 04, FEF 07, KAR 09]. Other measurements in low-dimensional systems were developed by Bourgeois, who investigated SiN_x and diamond membranes [SIK 12] and Si nanowires [HER 10a, HER 10b].

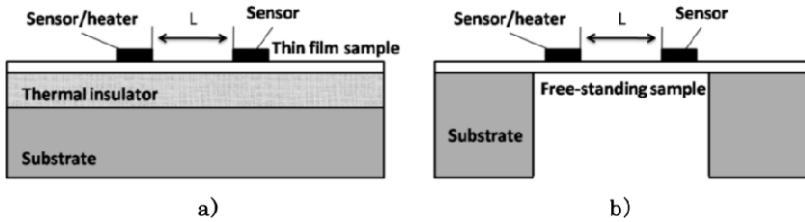

Figure 12.28. *Schematic diagram of structures used for in-plane thermal conductivity measurements in thin films: a) thin film on thermal insulator and b) free-standing membrane*

Another way to determine the thermal properties is by using the Raman peak position and FWHM, which are also sensitive to the sample temperature [HAR 70, VIE 01, PER 99]. When the temperature is increased, the Raman peaks shift to lower wave numbers and are broadened. This method is less reliable due to other contributions to the Raman spectral line-shape, such as embedded strain, strain due to a mismatch in thermal expansion, sample compositional/structural disorder [MIS 00, CAM 01], impurities and contamination of the sample as well as the presence of pseudo-phases and deformation of the material [CHA 10].

A high-resolution contactless technique based on Raman thermometry has been developed, which is suitable for thermal conductivity determination and thermal mapping of 1D and 2D structures [LIU 11, REP 13]. The method is generally applicable, provided that the samples exhibit a detectable Raman signal of an active mode, and a sufficiently large spectral shift as a function of temperature. The thermal conductivity is obtained by fitting the spatial decay of the thermal field using a diffusive model based on Fourier's law. The technique is based on a two-laser approach ($\lambda_1 = 407$ nm, $\lambda_2 = 488$ nm) to create and probe a thermal field in the nanostructure (see Figure 12.29(a)). While a *heating* laser with λ_1 produces a

thermal hotspot, a *thermometer* laser with λ_2 measures the spatial distribution of the local temperature through the temperature-dependent red shift of the longitudinal optical (LO) Raman mode, (Figure 12.29(b), similar to the case of the usual single-laser Raman thermometry). The main advantage of this technique as compared to other contactless techniques, e.g. based on infrared cameras, is its sub-micrometer spatial resolution, while maintaining the direct imaging capability of the temperature distribution.

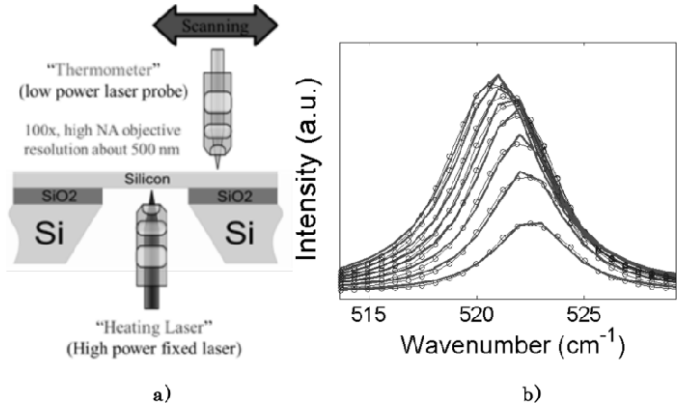

Figure 12.29. *a) Schematic diagram of the two-laser Raman thermometry experimental setup; b) LO mode Raman spectra from a 194 nm thick Si membrane under laser heating for absorbed laser powers of 0.2–5.3 mW*

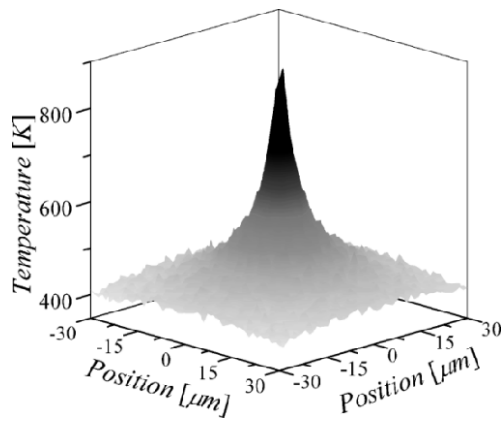

Figure 12.30. *2D thermal map of a 1 μm thick free-standing Si membrane from two-laser Raman thermometry*

This technique of 2-laser Raman thermometry (2LRT) has been applied to Si membranes of thickness ranged from 20 to 2,000 nm. A temperature rise of 200 K is measured at the position of the source decay slowly toward the edges of the membrane. Figure 12.30 shows a 2D thermal map of a 1 μm Si membrane, with a 200 K rise in temperature at the position of the source and a gradual return to equilibrium at the edges of the membrane. The heating laser is placed at the centre of the plot (0 μm) and the Raman signal is obtained by scanning the thermometer laser symmetrically at both sides of the source along a line. The Raman shift is converted to temperature by means of calibrated temperature dependence of the Raman peak position. The temperature distribution on the membranes exhibits a maximum at the source position and gradually decays to room temperature toward the frame of the membrane, which is in contact with the substrate. The thermal maps obtained contain a substantial amount of information: the thermal conductivity can be determined by fitting the temperature decay using an appropriate heat diffusion model, while the heat transport regime is given by the shape of the thermal decay.

The thermal conductivity of the membrane κ_{mem} is calculated from the local rise in temperature at the centre of the membrane as a function of the absorbed laser power. To calculate the temperature distribution inside the laser-heated Si membrane, we must solve the 2D heat flow equation:

$$\rho C_p \frac{\partial T}{\partial t} - \nabla \cdot \left(\kappa_{\text{mem}} \nabla T \right) = Q \qquad [12.1]$$

where ρ is the density, C_p is the specific heat and Q is the heat source term. The heat load within the slab is given by:

$$Q(r,z) = \frac{Q_0 A_b}{\pi a^2} \alpha \exp\left[-(r/a)^2 \right] \exp[-\alpha z] \qquad [12.2]$$

where Q_0 is the total power input, α is the absorption coefficient, and the two exponential terms correspond to a 2D Gaussian distribution and to the depth decay due to absorption, respectively. The thermal conductivity of the membrane is assumed to follow that of bulk Si, i.e. $\kappa_{\text{mem}} = \beta\, \kappa_{\text{bulk}}$ where β is a fitting factor that accounts for the reduced thermal conductivity in the membrane and $0.7 < \beta < 1.0$. In Figure 12.31(a), line scan of the experimental data through the centre of the membrane is shown, together with curves of temperature fields for different values of κ_{mem} departing from the bulk value $\beta = 1$ (dashed line), which are calculated by finite element simulations using the heat transfer model of the commercial software

COMSOL MultiPhysics. The profile is best adjusted to the experimental data when a decrease in the thermal conductivity in the membrane is taken into account ($\beta \approx 0.8$).

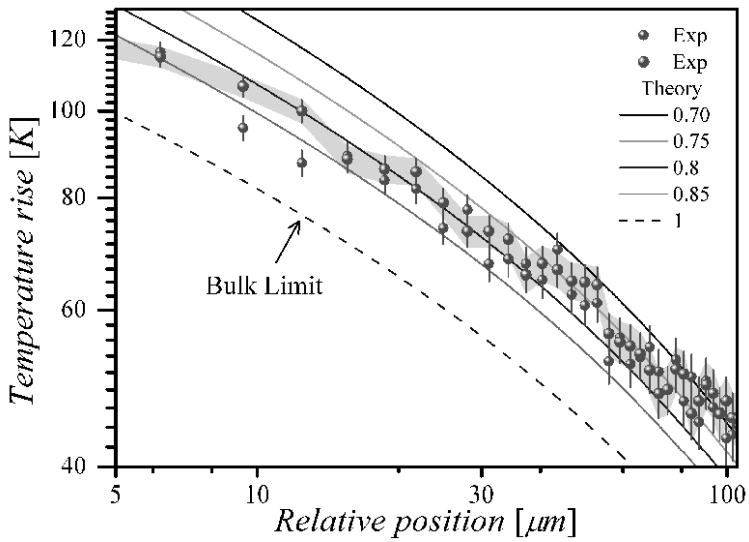

Figure 12.31. *Thermal line scan for a 1 μm thick free-standing Si membrane. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The temperature reached at the centre of the membrane for a given input laser power increases as the membrane thickness is decreased (Figure 7.18(a)), which clearly demonstrates a lower rate of heat dissipation for the thinner membranes. The relationship between change in the temperature and the absorbed power yields a value for the thermal conductivity, through the solution of the steady-state heat diffusion equation for the given geometry. The result demonstrates that the thermal conductivity of free-standing Si membranes is significantly reduced compared to the bulk value, by factors ranging from 0.7 for a 194 nm membrane down to below 0.1 for a 9 nm membrane.

Finally, Figure 12.32 compares the results obtained using Raman thermometry, (circles) with the data obtained using the thermal transient grating technique (squares) in the same set of samples. We note that the agreement between both techniques is quite satisfactory. The thermal conductivity of the membranes decreases with their thickness, which arises mostly from phonon boundary scattering at the surfaces of the membranes.

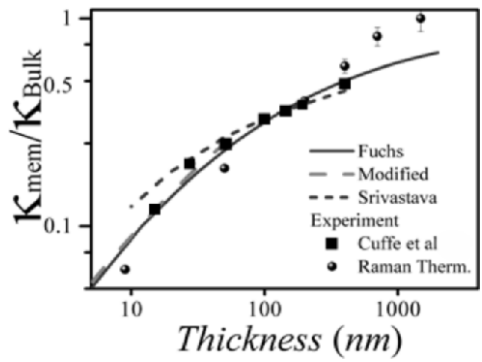

Figure 12.32. *Thermal conductivity of Si membranes: (squares) experimental measurement by TTG and (circles) Raman thermometry; (solid line) theoretical predictions using Fuchs-Sondheimer [FUC 38, SON 52], (dashed line) modified dispersion relation [HUA07], (short dashed line) Srivastava model [SRI 90]*

12.4.3. *Epitaxy-compatible thermal isolation platform*

A process has been developed to fabricate Ge or Si on SiO_2, which is commercially available as SOI layers and can be used with epitaxial techniques to create doped layers or heterostructures for S-Sm-S cooling junctions. The two main advantages of SiO_2 layers over Si layers are, first, that the SiO_2 is not strained to corrugate the structure and, second, that the thermal conductivity is orders of magnitude lower, thus isolating the platform from its surrounding substrate. A thick PECVD oxide layer was deposited on a silicon wafer and subsequently a metal layer overgrown. It was covered with a protective layer that allowed the underlying silicon to be locally chemically etch away, leaving a suspended membrane structure (Figure 12.33).

12.5. Summary of thermal conductance measurements

Thermal conductance measurements have been made on a range of different membrane structures. In addition to those reported above, the 3ω technique has been shown to be applicable to thin films of SiN_x and SiO_2 by comparison to values reported in the literature in Figures 12.34 and 12.35, respectively. All these thermal conductivity data are collected together in Figure 12.36. It can be seen that both the thin Si membrane and porous Si micro-coldplate are competitive low thermal

conductivity options in their relevant temperature range. In constructing an electronically cooled platform, this low thermal conductivity is vital to avoid heat leaking into the platform. Meanwhile, heat has to be extracted from the platform through the cold fingers, which therefore need a high thermal conductivity as provided by additional metallization shown in Figure 12.6(b) and a good thermal interface to the platform. The balance of heat flow is thus complex and needs to be very carefully optimized, both through modeling and in practice in order to cool to the lowest temperature.

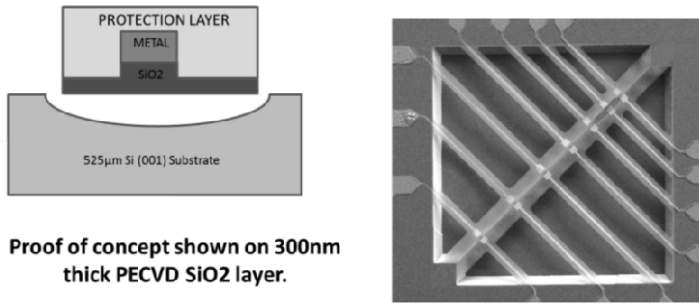

Figure 12.33. *Schematic diagram of an SiO_2 membrane complete with Al metal overlayer and SEM of the actual structure produced*

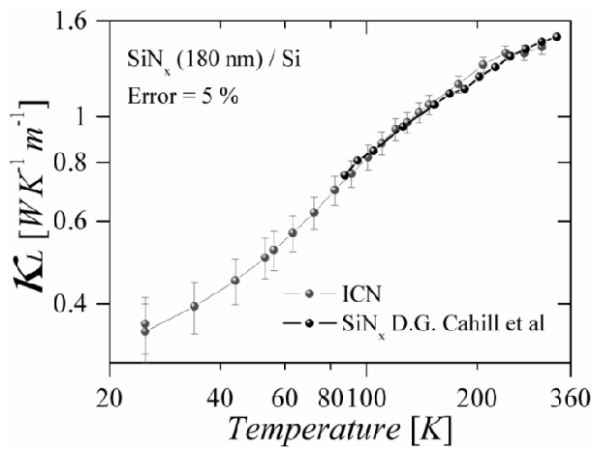

Figure 12.34. *Measurements to test the accuracy of the 3ω experimental setup in thin films. SiN_x/Si thin film with a thickness of 190 nm grown using LPCVD. The data in black circles represented quite established experimental data [CAH 03]. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices1.zip*

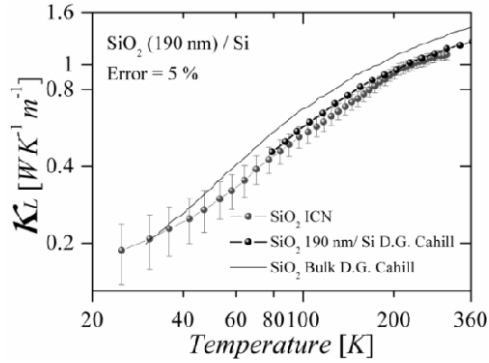

Figure 12.35. *As Figure 12.32 for a 190 nm thick SiO_2/Si thin film grown by thermal evaporation. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices1.zip*

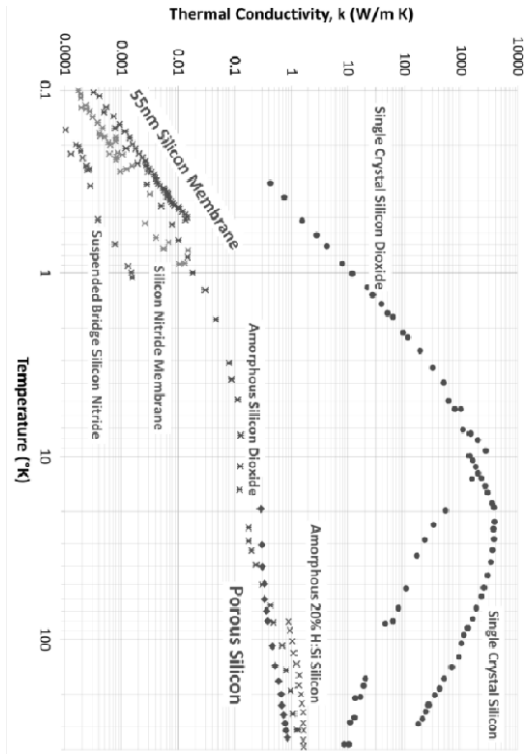

Figure 12.36. *Thermal conductivity of potential membrane materials as a function of temperature. The porous Si results are from [VAL 13]. For a color version of the figure, see www.iste.co.uk/balestra/nanodevices1.zip*

12.6. Acknowledgments

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PART 4

New Materials, Devices and Technologies for RF Applications

Part 4 Introduction

I.4.1. General

The increasing expansion of telecommunications applications and the use of increasingly higher frequency bands generate a need for high-performance RF and millimeter-wave (mm-wave) active and passive elements. Current CMOS technology evolution through miniaturization reached a high frequency of operation of the active devices that goes beyond 250 GHz (transistor maximum frequency). This high frequency of operation demonstrates the capability of co-integration on the same Si chip of RF and mm-wave analog electronic devices and circuits with CMOS logic elements. A high-performance functional CMOS logic/RF analog system-on-chip (SoC) at low cost and low power consumption is required in a large number of mass-market applications. However, the missing elements of this SoC are the high-performance passive devices realized on the same low-resistivity bulk Si substrate as CMOS logic devices.

At RF and mm-wave frequencies, we generally prefer using transmission lines (TLines) to realize different passive functions, instead of discrete elements. This is dictated by the necessity to avoid inaccuracies introduced by such discrete elements, due to the very small inductance and capacitance values required. Different TLines topologies can be used, depending on the specific fabrication technology. Microstrip TLines, composed of a metal line on the top Si wafer surface and a ground plane at the backside of the wafer, show the advantage of not being sensitive to the substrate properties. They were successfully used to fabricate high-performance passive components in a 32 nm general purpose bulk CMOS technology [ARN 08]. However, the co-planar waveguide transmission line (CPW TLine) topology offers better flexibility of application and better compatibility to CMOS technology. In this topology, both the TLine and the two ground planes on both sides of the line are

Introduction written by Androula G. NASSIOPOULOU.

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co-integrated on the front surface of the wafer. The drawback in this case is the crucial effect of the substrate characteristics on the line performance. A similar substrate effect is observed in the other key passive elements (inductors, antennas, filters, etc). The Si substrate used in bulk CMOS is a low-resistivity Si wafer (resistivity in the range of 1–10 Ω·cm), which is not adequate for the above RF passive device integration. Performance limitations by the low-resistivity substrate are related to the high attenuation in TLines, capacitive effects and eddy currents into the substrate and cross-talk between RF devices due to parasitic signal transfer into the substrate (coupling effect). To reduce the above effects, a substrate resistivity of 100 Ω·cm and beyond is required, which is not compatible with the CMOS bulk substrate and its increased cost. One proposed solution considering the CMOS substrate includes local thinning of the wafer underneath the devices using bulk Si micromachining. This technology needs front/back lithography alignment and introduces several complicated steps to the CMOS processing. Another solution is the use of a thick porous Si layer locally formed on the Si wafer to provide the necessary shielding to the passive devices that are integrated on it.

In Part 4 of this book, the main focus is on the following:

– Substrate materials and technologies for the integration of high-performance RF and mm-wave devices.

– An investigation of the properties of metal nanolines for their potential use as RF interconnects in next-generation integrated circuit (IC) technologies.

– Nanostructured magnetic materials for high-frequency applications.

This part is composed of three chapters, as follows.

I.4.2. Substrate materials and technologies for the integration of high-performance RF and mm-wave devices (Chapter 13)

Analog RF integrated circuits (RFICs) are essential for single-chip radios, wireless communication chips and other emerging high-frequency applications. They are intensively investigated toward achieving higher frequencies of operation to cover the mm-wave frequency bands [DOA 04]. Passive elements such as inductors, capacitors and antennas integrated on-chip are essential building blocks of these ICs. Of particular interest are TLines used for matching networks, baluns, power splitters and filters. Unfortunately, as explained above, the low-resistivity Si substrate constitutes a bottleneck to their successful integration on the Si chip. Good performance silicon integrated passive devices using CMOS technology process steps are currently developed on high-resistivity (HR) silicon, silicon-on-insulator (SOI) and InP substrates. However, the above substrates are not compatible with the

existing CMOS technology and, in addition, the TLines attenuation loss on these substrates is not better than 0.4–0.5 dB/mm at 60 GHz [BEL 10, HEI 98, GIA 07 CAT 07, MOR 10].

Different MS TLs realized with a dedicated mmW technology having two thick metal layers of 3 μm show quite the same performance, with attenuation loss of 0.5 dB/mm at 60 GHz for 50 Ω characteristic impedance TLs. However, in advanced CMOS digital technology notes, as for example the 32–28 nm one, the thickness of the layers in the back-end-of-line stack is reduced. Even the thicker upper metal layer thickness is reduced and it becomes smaller than 1 μm in the CMOS 32–28 nm technology node. It is also evident that even if we use the thicker upper metal layer for the fabrication of the TLs, the achieved attenuation loss is dramatically increased. A state-of-the-art attenuation loss of 0.9 dB/mm at 60 GHz has recently been obtained for MS TLines using sub-32 nm CMOS technology and low-resistivity Si (~10 Ω·cm). However, this result is achieved only with MS TLines, since in CPW TLines the attenuation loss into the low-resistivity Si substrate is high. In addition to the attenuation loss, another issue with CPW TLines on the low-resistivity/high dielectric constant Si substrate is the technological difficulty of realizing high-characteristic impedance, low attenuation loss TLines, necessary for baluns and power splitters.

As a replacement to the low-resistivity CMOS Si wafer, an HR Si substrate is used in order to achieve high-performance Si-based passive devices. The performance of an HR Si substrate as an RF substrate and the newly commercialized trap-rich HR Si substrate, called enhanced signal integrity (eSI) wafer, is the major subject of Chapter 13. The next chapter is devoted to porous Si as a local substrate on the low-resistivity Si wafer for the integration of RF passive devices. Porous Si is a versatile material formed on the Si wafer by electrochemical etching. It shows properties that are tunable by changing the fabrication conditions and the type and resistivity of the Si substrate. Within nanofunction NoE, a methodology was introduced to extract the dielectric function of porous Si by measuring the S-parameters of a CPW TLine integrated on a thick porous Si layer and combining these measurements with electromagnetic simulations to extract the dielectric permittivity and the loss tangent of the material. These parameters depend on the porosity, structure and morphology of the porous Si layer, which in turn depend on the type and resistivity of the starting Si wafer and the electrochemical conditions used for porous Si formation. It was found that a dielectric permittivity as low as 2 can be obtained for highly porous Si, which opens important possibilities in applications, not only for achieving high-quality factor/low loss TLines, but also a tunable characteristic impedance, interesting for a variety of applications. High-performance CPW TLines and inductors on a local 150 μm thick porous Si layer were obtained for frequencies up to 210 GHz. New device topologies

(slow-wave TLines and filters) were also designed, taking advantage of the use of a local porous Si substrate to improve their performance.

I.4.3. RF interconnects and nanoantennas using metal nanolines (Chapter 14)

CMOS technology evolution through miniaturization results in an increase in the frequency of operation of the active devices, reaching the mm-wave frequency range for the latest technology nodes. In this respect, high-quality passive components are also needed in order to achieve an overall improvement in circuitry performance. In current CMOS technology, the TLines for the RF circuits are fabricated on the top metal layer of the back-end-of-line (BEOL), which has a thickness of a few microns and thus assures low conductor losses. However, for higher system integration density and/or three-dimensional circuit architectures, the use of lower level metal layers in BEOL, with smaller thickness, is of great significance. The use of such layers could be possible if the introduced interconnect resistance is not excessively high so as to compromise circuit performance. Interconnects in this case must be developed to be suitable for the circuit speed expected from miniaturization. To design such interconnects, the properties of thin metal lines at RF and mm-wave frequencies should be understood and appropriate TLine architectures and topologies are found. Very little work is found in the literature concerning this field, most of them dealing with carbon nanotubes. Within nanofunction, we investigated the properties of Al and Cu nanolines for their use in interconnect technology and nanoantennas. Methods to correctly measure electromagnetic wave propagation through corresponding TLines were developed by considering different de-embedding schemes. The effect of losses in the substrate was also considered by introducing a local porous Si layer underneath corresponding devices.

I.4.4. Nanostructured magnetic materials for high-frequency applications (Chapter 15)

Components using soft-magnetic materials are central to the operation of many ICT products, including inductors and transformers micromechanical components such as switches, read/write heads and sensors. Conventional magnetic core technology is currently dominated by discrete/sintered cores that are not compatible with the current trends toward miniaturization and integration. Recently, magnetic cores integrated onto silicon microchips or printed circuit board (PCB) as a part of microelectronic modules have received increased attention from the scientific/engineering community. The focus of research on such cores can be divided into two major categories: (1) a quest for improved magnetic materials capable of operating at high frequency and (2) a quest for suitable integration techniques.

In Chapter 15, a review of the current state-of-the art of research in this field is presented. Major results obtained within the nanofunction NoE on the development of nanomodulated magnetic materials and the investigation of their main properties are also presented. More specifically, an investigation of the static and dynamic magnetic properties of nanomodulated thin films was performed in view of the development of high-frequency soft-magnetic cores for next-generation integrated passive devices. Unique three-dimensional ferromagnetic nanostructured layers were fabricated by using a combination of different technologies (electrodeposition, nanoimprint lithography), forcing the macrospin configuration to follow a wave-like propagation of magnetization that collectively generates in-plane and out-of-plane dipoles. In a square array of magnetic nanostructures, the magnetic ordering is determined by a minimization of collective magnetostatic energy, whereas the overall magnetic anisotropy energy depends on the dipolar interactions. In general, the isolated nanostructures, which are bigger than a single domain, try to form a vortex (minimum energy state) at remanence state. In the work performed, the competition between two different dipoles (in-plane and out-of-plane) and possible spin pinning between two consecutive dipoles through continuous ferromagnetic media keeps the magnetization stable in the direction of the applied field and resists vortex formation. The magnetic interaction between two different dipoles generates a collective metastable magnetic configuration and a step-like MH curve is observed. To further elucidate this point, the angle of applied field direction was varied with respect to pattern array, which shows a rotation of dipoles with the rotation of the applied field. The variation of magnetic anisotropy was investigated by measuring coercivity in different directions, which shows a clear trend of fourfold anisotropy symmetry in the square array structure. These results were validated by micromagnetic simulations. A generalized model was developed for different anisotropy symmetries. In addition, the way in which these unique nanostructures of a continuous ferromagnetic film can induce magnetic dipoles at submicron scale at predefined locations and play a key role in tuning the global static and dynamic magnetic properties of the film due to dipole–dipole interactions was also elucidated. Gradual formation of magnetic dipoles and their tunability have been studied in detail by magnetic force microscopy (MFM) imaging, high-resolution static (SQUID) magnetic measurements and wideband (1 MHz–9 GHz) dynamic (complex permeability spectra) measurements.

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13

Substrate Technologies for Silicon-integrated RF and mm-wave Passive Devices

13.1. Introduction

Passive devices are essential elements for any RF circuit. Their on-chip integration is pursued as a simple, cost effective and more efficient alternative to off-chip passives that require complicated interconnects to active circuits and are, in general, bulky. Furthermore, it is a necessary step toward the future digital/RF analog system-on-chip (SoC) [BUS 03, BEN 03], which aims at integrating on the same chip high density–high speed digital with RF analog electronic circuits (ICs). Such a system can potentially provide the best performance in terms of size, reliability and cost. The main bottleneck toward such SoC is the low-resistivity Si substrate used in CMOS technology, which introduces significant RF losses, coupling and nonlinearity of RF devices [ROD 12]. Alternative substrate solutions investigated in the past studies include high-resistivity Si (HR-Si) [HEI 98], high-resistivity silicon-on-insulator (HR-SOI) [LED 08] and high-resistivity Si with a trap-rich layer between the Si substrate and the silicon oxide top layer (trap-rich HR-Si) [LED 05]. However, all the above solutions deviate from the goal of co-integration of CMOS logic with RF analog ICs, due to incompatibility of HR-Si with the CMOS Si substrate.

A promising solution is the local porous Si substrate solution, in which a thick porous Si layer is locally formed on the Si wafer in order to provide the necessary

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RF shielding for the RF devices [KIM 03, CON 08a, CON 08b, ZAC 09, GAU 08]. Work within the EU FP7 NoE Nanofunction project contributed substantially toward demonstrating that this solution is a viable one [SAR 13a, SAR 13b, SAR 13c, ROD 13, NAS 13]. The superiority of the local porous Si isolation technology has been demonstrated for coplanar waveguide transmission lines (CPW TLines) [ISS 11, SAR 13d] and inductors on porous Si [CON 07, SAR 13c] for the frequency range from DC up to 210 GHz. An advantage was also demonstrated for integrated antennas on porous Si compared with similar antennas on bulk crystalline Si [SAR 13e].

Novel RF device topologies were recently introduced for improving the quality factor of the transmission lines at RF. One such topology is for example the slow-wave transmission line topology developed in [SEK 81], taking advantage of the so-called slow-wave effect. High-performance slow-wave or shielded CPW TLines (S-CPW TLines) on the low-resistivity Si substrate are obtained using this topology, first implemented in CMOS technology in [CHE 03]. A lot of work has recently been done on these devices [KAD 08, VEC 09, FRA 13]. In the slow-wave topology, a shielding layer composed of metal strips is introduced between the CPW TLine and the Si substrate, designed to provide the adequate RF shielding from the Si substrate. With this approach, quality factors as high as 40 and more can be achieved. However, such S-CPW TLines cannot lead to high-characteristic impedances. Also, the solution can be given by the porous Si substrate, which can be used both for improving the quality factor of the TLine and for offering a very large choice of characteristic impedances, from 20 Ω to more than 150 Ω. This helps us in the design of very different RF circuits such as baluns, power dividers, filters etc.

In this chapter, we will focus mainly on two different Si-based substrates: (1) high-resistivity Si substrate, including HR-Si, HR-SOI and trap-rich HR-Si and (2) porous Si substrate. A full comparison between the two is presented by integrating similar CPW TLines on both of them and measuring their properties under similar conditions.

13.2. High-resistivity Si substrate for RF

The Si wafer used in CMOS technology has a resistivity in the range of 1–10 Ω.cm, and it is not adequate for the integration of RF transmission lines due to the induced substrate losses. It is thus mandatory to replace it with a low-loss substrate material. An HR silicon substrate is one of the solutions to reduce the high-frequency losses associated with the substrate conductivity as much as possible. High-quality coplanar waveguides presenting insertion loss of less than 2 dB/mm at 200 GHz, as well as low- and high-pass filters at mm-waves, have been

successfully built in an industrial HR silicon-on-insulator (SOI) CMOS process environment [GIA 07a, GIA 07b].

13.2.1. *Losses along coplanar waveguide transmission lines*

The insertion loss of a coplanar waveguide transmission line (CPW TLine) lying on a lossy silicon substrate depends on the conductor loss (α_{cond}) and the substrate loss (α_{sub}), which is inversely proportional to the effective resistivity of the substrate. The effective resistivity represents the value of the substrate resistivity that is actually seen by the coplanar devices. This parameter accounts for the wafer inhomogeneities (i.e. those of the oxide covering the Si wafer) and space charge effects, and corresponds to the resistivity that a uniform (without any oxide or space charge effects) silicon wafer should have in order to sustain identical RF substrate losses. The effective resistivity is extracted from the measured S-parameters of the CPW line with a method depicted in [LED 05b]. Simulation results shown in Figure 13.1 outline how this parameter affects substrate and total losses for a 50-Ω CPW with 1 µm-thick Al line, a central conductor width of 40 µm and spacing between conductors of 24 µm. These data are obtained with analytical formulas presented in [HEI 93] and assuming metal conductivity of 3 x 10^7 S/m. It is seen that substrate losses (α_{sub}) are small (~0.1 dB/cm) when ρ_{eff} is close to 3 kΩ.cm and become insignificant compared with conductor losses (α_{cond}) when ρ_{eff} reaches 10 kΩ.cm. Keeping substrate losses at low levels is a priority target when designing high-performance integrated silicon systems [HEI 98]. In this field, HR silicon wafers (>3 kΩ.cm) are considered as promising candidates for radio frequency-integrated circuits [REY 95] and mixed-signal applications [BEN 03]. HR-Si substrates are available on the market. However, oxide-passivated HR wafers are known to suffer from parasitic surface conduction (PSC) due to fixed charges (Q_{ox}) in the oxide [WUY 99]. Indeed, charges within the oxide attract free carriers near the substrate surface, reducing the effective resistivity (ρ_{eff}) seen by coplanar devices and increasing substrate losses. It has been demonstrated in [LED 03] that values as low as $Q_{ox} = 10^{10}$ cm^{-2} could lower the value of resistivity by more than one order of magnitude in the case of 50-Ω CPW transmission lines. The PSC can also be formed underneath metal lines with the application of a DC bias (V_a) [SCH 03]. The extracted line loss and effective substrate resistivity as a function of the DC bias applied to the central conductor of a CPW line are, respectively, presented in Figure 13.2(a) and 13.2(b) for different substrates, oxide layers and metallic lines, as summarized in Table 13.1. Techno A and B are wafers coming from industry, while the three other wafers named C, D and E are home processes with one metal layer. In all cases, the metallic structures are patterned on either oxidized p-type HR unibond SOI (techno A, B, C) or oxidized p-type HR bulk Si (techno D and E) substrates.

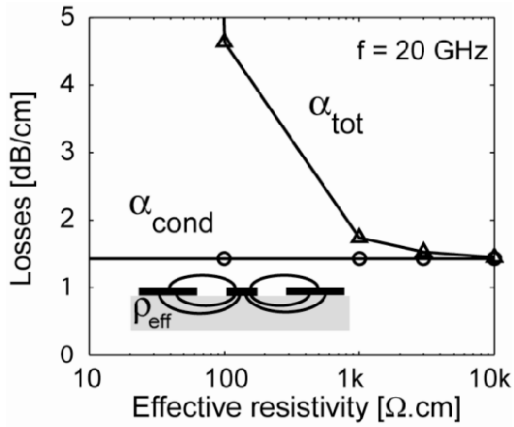

Figure 13.1. *Total (α_{tot}) and conductor (α_{cond}) losses as a function of ρ_{eff} at 20 GHz for a CPW line geometry according to [HEI 93]*

Techno	Starting wafer	Metal layers	Oxide thickness (µm)	Si passivation	Oxide type
A	HR-SOI	M3	3	No	BOX +oxidized SOI + inter-layer dielectrics
B	HR-SOI	M5-M6	4.1	No	BOX +oxidized SOI + inter-layer dielectrics
C	HR-SOI	M1	0.3	No	BOX + oxidized SOI
D	HR-Si bulk	M1	1	No	PECVD
E	HR-Si bulk	M1	1	Polysilicon	PECVD

Table 13.1. *Additional information on the different technologies investigated in Figure 13.2. The data in columns 3 and 4, respectively, indicate the metal layers that were used and the total equivalent oxide thickness for CPW lines*

The total RF losses (α_{tot}) of the CPW lines are extracted from the measured S-parameters with a Thru-Line-Reflect method [HSI 04]. They are reported at 10 GHz in Figure 13.2(a) as a function of V_a, where it is seen that α_{tot} may be significantly affected by V_a when the oxide thickness (t_{ox}) is in the several hundreds of nm range (techno C). Indeed, in that case highly positive or negative biases have a large impact on the free carrier concentration below the oxide, thereby strongly affecting substrate losses. This effect is attenuated for thicker oxides (techno A, B and D). The V_a value for which losses are minimum ($V_{a,min}$) corresponds to the state of deep depletion underneath the oxide. As shown in Figure 13.2, V_a depends on the flatband voltage of the structure and is therefore dependent on t_{ox} as well as on the oxide charge density (Q_{ox}).

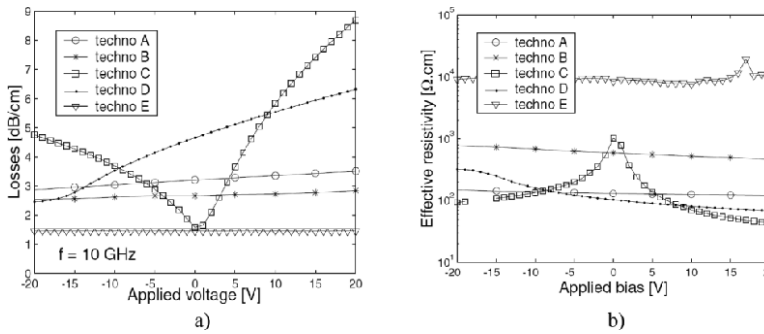

Figure 13.2. *a) CPW losses and b) effective substrate resistivity measured for different technologies described in Table 13.1 as a function of DC bias applied to the CPW central conductor*

To obtain more physical insight into the impact of PSC on the effective resistivity of the silicon substrate, numerical simulations have been run to extract the resistivity profile along the semiconductor depth for a p-type 5 kΩ.cm Si wafer. The results are shown in Figure 13.3. Because of the metal-semiconductor work-function difference and the fixed oxide charges (Qox = 10^11 /cm²), the inversion layer right underneath the oxide drastically decreases the resistivity of the substrate over a depth of approximately 3 μm [BEN 11]. Such parasitic conduction effects can be effectively reduced by introducing a high density of traps (Dit = 10^11/cm²) underneath the insulating oxide, as demonstrated in Figure 13.3. The presence of the metal-semiconductor work layer right underneath the oxide drastically decreases the resistivity of the substrate over a depth of approximately 3 μm.

The PSC can be reduced or even suppressed if the silicon substrate is passivated before oxidation with a trap-rich, highly resistive layer. Figure 13.4 illustrates the impact of trap density (D_{it}) at the HR-Si substrate–SiO_2 interface on the value of ρ_{eff} at 0 V for several Q_{ox} densities. It can be seen with no surprise that the minimum D_{it} level ($D_{it\,=\,10\,k}$), which is required to obtain lossless substrates (i.e., ρ_{eff} = 10 kΩ.cm), is an increasing function of the fixed charge density in the oxide. This is because for higher positive densities, a higher concentration of electrons is attracted near the substrate surface and a higher density of traps is required to absorb those mobile carriers.

As presented in Figure 13.3, because of the introduction of traps at the oxide/Si substrate interface, the HR properties underneath the oxide layer are conserved even at the proximity of the interface and the nominal substrate resistivity is recovered at the depth of approximately 20 μm. The Si substrate region presenting a resistivity higher than the nominal substrate resistivity (> 5 kΩ.cm) is related to the depletion region in the p-type Si substrate.

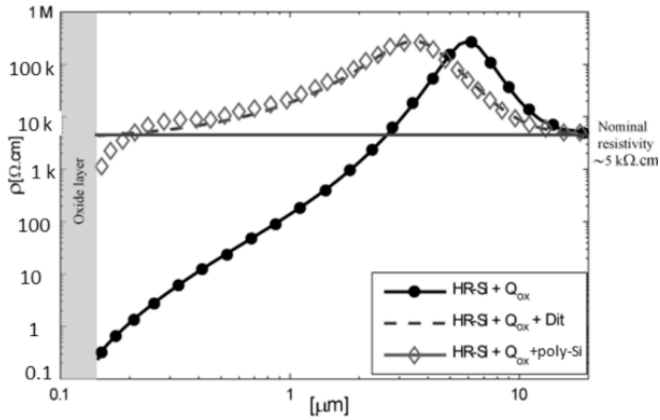

Figure 13.3. *Simulated resistivity vs. substrate depth for p-type 5 kΩ.cm HR-Si substrates, with and without a trap-rich layer (D_{it} introduced at the interface or simulation of an undoped polysilicon layer noted polySi). Q_{ox} = 10^{11}/cm^2 and D_{it}= 10^11/cm^2*

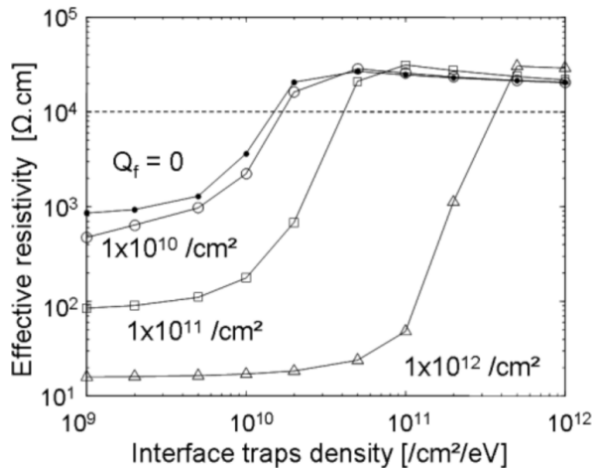

Figure 13.4. *Simulated effective resistivity values ρ_{eff} as a function of the trap density D_{it} for several fixed charges densities Q_{ox} at an applied bias value of 0 V*

The introduction of a high density of traps at the Si–SiO_2 interface has been successfully achieved using low-pressure chemical vapor-deposited (LPCVD) polysilicon (polySi) and amorphous silicon (α-Si) in [GAM 99] and [WON 04], respectively. In the context of SOI technology, substrate passivation could also be an efficient technique for reducing substrate losses. To be compatible with an HR-SOI wafer fabrication process, the passivation layer should be included within the SOI

structure by bonding an oxidized silicon wafer with a passivated HR substrate. In [LED 05b], the proposed method consists of the LPCVD-deposition of amorphous silicon followed by Si-crystallization at 900°C with RTA. This method was compared with previously published techniques (passivation with amorphous silicon in [WON 04] or LPCVD-polysilicon in [GAM 99]) and was demonstrated to perform better in terms of substrate loss reduction: effective resistivity values higher than 10 kΩ.cm were reported, compared with 3 and 6 kΩ.cm in the case of amorphous Si and LPCVD-polySi passivation, respectively. The new passivation method was also shown to present better rms surface roughness (σ = 0.37 nm) and to remain effective after long thermal annealing (4 hours at 900°C). A successful bonding of this layer with an oxidized substrate was achieved, showing that this new passivation technique could be introduced at reduced cost inside a Smartcut or BESOI process in order to fabricate SOI wafers with enhanced resistivity, i.e. higher than 10 kΩ.cm. Inspired by those theoretical and experimental results, SOITEC in collaboration with Université Catholique de Louvain (UCL) developed a new HR-SOI substrate, named eSI, which stands for enhanced signal integrity. eSI substrate is manufactured by SOITEC and is available on the market.

Figure 13.2(a) indicates that substrate passivation with polysilicon (techno E) significantly reduces RF losses while getting rid of the V_a influence. This is because traps present inside the polySi layer can absorb free carriers and pin the surface potential to a value independent of V_a [GAM 99]. Figure 13.2(b) presents the effective resistivity (ρ_{eff}) extracted according to a method depicted in [LED 05]. Not surprisingly, the highest ρ_{eff} value is observed for the passivated substrate, while at 0 V, the lowest value is obtained for the low-quality (Q_{ox}-rich) PECVD oxide. It should also be noted that due to the inverted layer underneath the BOX in techno A and B, the extracted values of ρ_{eff} do not exceed 130 and 580 Ω.cm, respectively. These values are both more than one order of magnitude lower than the nominal substrate resistivity.

The effective substrate resistivity of both HR-SOI and trap-rich HR-SOI wafers provided by SOITEC before and after UCL CMOS process, respectively, has been extracted. Figure 13.5 shows that the HR properties of HR-SOI are degraded after CMOS processing. It is actually four times lower than that on the initial HR-SOI substrate. This could be related to the different oxide stacks and thermal steps that are done during the CMOS process. The oxide charge density changes, as well as the interface traps, and the total net effect, give a degradation of the RF performance due to a stronger impact of the PSC effect. On the contrary, the effective resistivity remains the same and very high (nominal resistivity of the HR-Si substrate) before and after the CMOS process in the case of trap-rich HR-SOI wafers. We can see that the effective substrate resistivity of CPW on trap-rich HR-SOI is at least one order of magnitude higher than that of a similar CPW on

HR-SOI and that trap-rich HR-SOI can be considered lossless with and effective resistivity higher than 4 kΩ.cm. The trap-rich HR-SOI substrate reveals an excellent compatibility in terms of RF performance stability with the CMOS process.

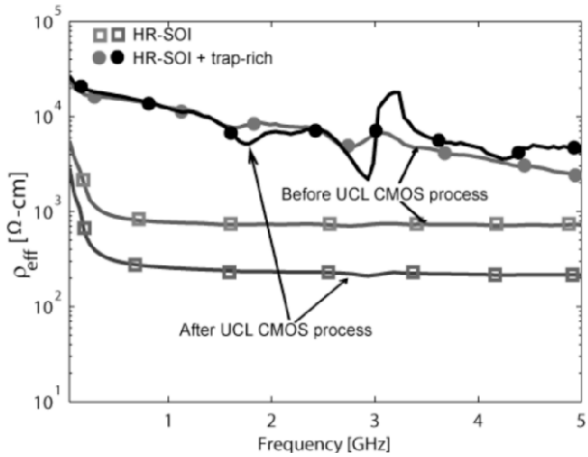

Figure 13.5. *Effective resistivity vs. frequency of CPWs on HR-SOI and trap-rich HR-SOI wafers*

13.2.2. *Crosstalk*

In recent years, the rapid progress of integrated circuit technology has made the co-integration of analog front-end and digital baseband-processing circuits of communication systems onto the same chip possible. Such mixed-signal SoCs have more functionality, higher performance, lower power and higher reliability than non-integrated solutions, where at least two chips are needed, one for digital and one for the analog applications. Moreover, because of CMOS technology scaling and its associated increasing integration level, SoCs have become the way to achieve cost effectiveness for demanding applications such as home entertainment and graphics, mobile consumer devices, networking and storage equipment. Such a rising integration level of mixed-signal ICs raises new issues for circuit designers. One of these issues is the substrate noise (see Figure 13.6) generated by switching digital circuits, called digital substrate noise (DSN), which may degrade the behavior of adjacent analog circuits [CAL 06a]. DSN issues become more and more important with IC evolution as (1) digital parts become more noisy due to increasing complexity and clock frequencies, (2) digital and analog parts closer and (3) analog parts more sensitive because of V_{dd} scaling for power concern issues.

High-performance SoC applications impose stringent requirements on the substrate characteristics. An ideal substrate should be a good thermal conductor and provide good isolation for digital switching noise (preferably <–100 dB). Among the numerous wireless standards, ultra wideband (UWB) systems face many design and technological challenges since they operate at high frequencies and over a wide frequency band (3.1 to 10.6 GHz). Such systems are more sensitive to substrate noise, which mostly originates from the synchronization clock (3, 10, 26, 100 MHz, etc.) and the high-speed digital circuits. Switching noise of such digital circuits propagates through the substrate and affects the different parts of the wideband system, such as the low-noise amplifier (LNA) [FAN 07], UWB RF filters [GIA 06a] and voltage-controlled oscillator (VCO) [CAL 06b]. Among the many applications enabled by SoC, building blocks are reconfigurable RF systems that benefit from co-integration of RF MEMS devices with CMOS-integrated circuits. Although they offer high performance in a modular fashion, they still suffer from substrate coupling and crosstalk effect [CLA 07].

In general, substrate noise can be decomposed in three different mechanisms: noise generation, injection/propagation into the substrate and reception by the analog part [VAN 00a]. Improvement in the reduction of any of these three mechanisms, or in all of them, will lead to a reduction in the DSN and a relaxation in the design requirements. Typically, guard rings and overdesigned structures are adopted to limit the effect of substrate noise, thereby reducing the advantages of the introduction of new technologies. It is thus a major issue for the semiconductor industry to find area-efficient design/technology solutions to reduce the impact of substrate noise in mixed-signal ICs.

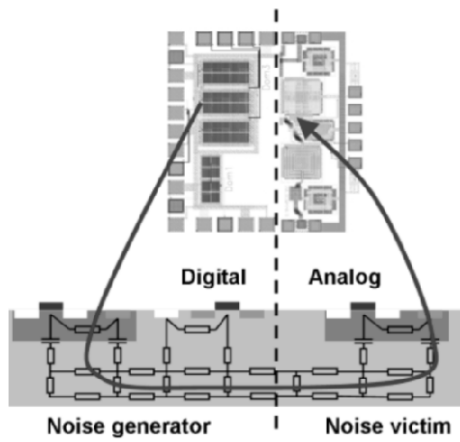

Figure 13.6. *Schematic representation of the substrate crosstalk between digital and analog parts of an SoC. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Over the last decade, several publications have theoretically and experimentally demonstrated the interest of HR-SOI substrates to greatly reduce the crosstalk level between integrated circuits [RAS 97]. Figure 13.7 shows how the crosstalk between two 50 µm-spaced metal pads is affected by ρ_{eff} and indicates that ρ_{eff} must be at least in the several kΩ.cm range to get rid of conductive coupling inside the substrate for frequencies around 100 MHz and lower. The result of the substrate crosstalk measurements using a classical double-pad structure in which both pads are connected to separate RF probing pads [RAS 97] is shown in Figure 13.8 in the form of $|S_{21}|$ versus frequency curves. The measurements are performed by using the low-frequency VNA up to 4 GHz and by applying various bias conditions on the coupling pads. The figure shows significantly higher (~13 dB at 0 V) crosstalk level below 1 GHz for the standard HR-SOI wafer, due to conductive effects in the substrate associated with PSC [LED 06]. It also highlights a significant dependence with respect to the applied bias. The crosstalk level is strongly reduced for negative bias and when deep depletion is formed below the BOX, whereas it is enhanced and exhibits higher cut-off frequencies for positive bias and increased inversion below the oxide. On the other hand, the passivated wafer exhibits (1) no effect of the applied bias due to the presence of the trap-rich polysilicon layer below the BOX [LED 05a] and (2) a perfect 20-dB/dec slope which shows that purely capacitive coupling occurs in the measurable frequency range (i.e. above the VNA noise floor). A reduction in crosstalk below 1 GHz is of particular interest for mixed-signal applications, since it is known from previous studies that the frequency spectrum of the noise generated by digital logic typically expands to several hundreds of megahertz, corresponding to multiples of the clock signal [VAN 00a, VAN 00b, VAN 02] or circuit internal resonance frequencies [BAD 03]. The generation of noise in that frequency range has also been shown to strongly increase the jitter in phase-locked loops (PLLs), which seem to be particularly sensitive to substrate noise injected at the PLL reference frequency, i.e. in the few hundreds of megahertz range [JEN 06]. It is further believed that in terms of crosstalk, the benefits gained by substrate passivation will even increase in the future. Indeed, a reduction in the BOX thickness for the next generations of active SOI devices will be required to reduce short channel effects and self-heating [ITR 05]. In [ROD 08], experimental DSN characterizations of CMOS circuits lying on SOI and bulk Si substrates are compared. Current injected into the substrate creates substrate voltage fluctuations (substrate noise). It is mainly created by two mechanisms [CAL 06]: coupling from the noisy digital power supply circuit and from switching drains. The DSN for eight switching inverter trees biased at either 0.8 or 1.2 V and for an input clock frequency of 225 MHz in the case of SOI and Si bulk substrates has been measured in [ROD 08, BOL 07]. For the 1.2 V supply voltage, the SOI technology causes a significant reduction in DSN up to 1 GHz. At higher frequency, the noise due to ringing on supply rail becomes dominant, and the bulk circuit shows a lower DSN level. This conclusion is in agreement with the results of studies on the supply

noise, showing that special attention should be paid to the rail for SOI technology, due to lower intrinsic decoupling capacitances [CHE 97]. At lower power supplies (0.8 V), as for the bulk, high-frequency noise generation decreases. The ringing supply noise thus tends to be negligible. In this case, the SOI technology presents better DSN results than the bulk substrates for frequencies up to 2 GHz, and similar DSN level for upper frequencies.

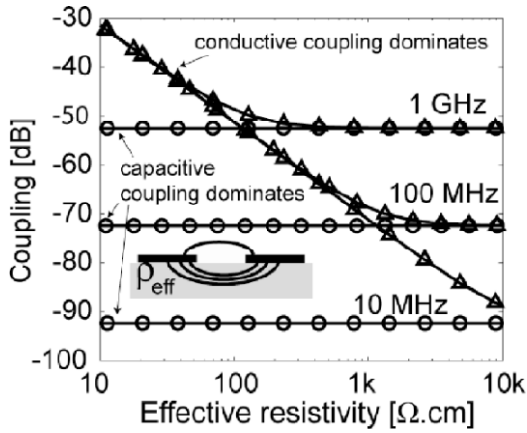

Figure 13.7. *Simulated crosstalk level at 10 MHz, 100 MHz and 1 GHz as a function of ρ_{eff} according to model presented in [RAS 97]*

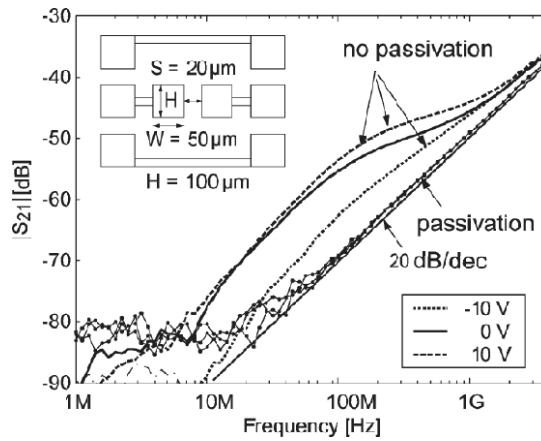

Figure 13.8. *Crosstalk measured as a function of frequency and under distinct bias conditions on the unpassivated and passivated HR-Si wafers*

13.2.3. *Nonlinearities along CPW lines*

HR silicon substrates are promising for RF applications due to their reduced substrate loss and coupling, as presented in the two previous paragraphs, which helps to facilitate RF cellular transmit switches on SOI using HR-Si handle wafers [TIN 06, MCK 07]. RF switches have high linearity requirements: for instance, a recent III-V RF switch product specifies less than –45 and –40 dBm for 2nd and 3rd harmonic power (H2 and H3), respectively, at +35 dBm input power [SIN]. As requirements become even more stringent for advanced multimode phones and 3G and 4G standards, it is important to investigate even small contributions to harmonic distortion (HD).

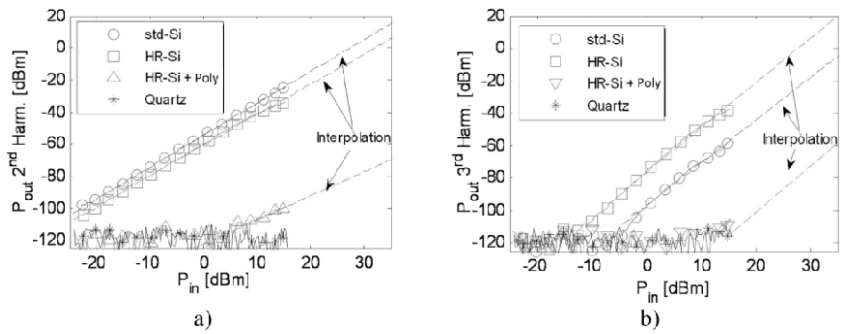

Figure 13.9. *a) 2nd and b) 3rd harmonic power of a 3,385 µm-long CPW line lying on different substrates. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

As explained above, when the CPW line is biased, the distribution of potential and free carriers inside the Si substrate changes as in the case of a classical MOS capacitor. The variation of carrier distribution in the Si substrate with the applied bias or large RF signal will thus lead to the existence of nonlinear capacitance (C) and conductance (G) associated with the Si substrate. These variables, C and G, are at the origin of the harmonics formation inside the Si substrate.

Figure 13.9 shows the HD of CPW Al metal lines on Si p-type substrates of different resistivities with 50 nm of top SiO_2. HR-Si substrate presents lower HD than the 20 Ω.cm (std-Si) substrate over most of the power sweeps. Measurements are made up to +15 dBm input power, and linearly interpolated up to +35 dBm. It can be observed that non-passivated Si substrates have HD levels higher than 45 dBc at +15 dBm, already 25 dB higher than the switch specifications at +35 dBm. The introduction of a 300-nm polysilicon (polySi) layer reduces HD levels by more than 60 dB, compared with the non-passivated HR-Si. As explained above, because of the high density of traps in the polycrystalline silicon or

as-deposited amorphous silicon layer located at the Si–SiO_2 interface, the surface potential at this interface is nearly fixed, and the external DC bias or large amplitude RF signal applied to the line does not impact the distribution of carriers inside the Si substrate.

Figure 13.10 clearly shows that the presence of a trap-rich layer has almost no impact on the measured distortion levels for low-resistivity substrates (ρ = 10 and 100 Ω-cm), as predicted by the simulations presented in [ROD 12]. On the contrary, for substrates with higher resistivities, it considerably reduces the nonlinearities. Measurements done for substrates with identical high resistivity but different oxides, not presented here, show that the minimum distortion is obtained when a polySi layer is introduced, and it is only limited by the final effective resistivity. The introduction of a thin polySi layer helps in the reduction of PSC effects but cannot totally reduce the harmonic levels. Only the combination of both the Si substrate characterized by a high resistivity (>3 kΩ-cm) and a trap-rich layer provides a viable solution to obtain a quasi-linear Si substrate.

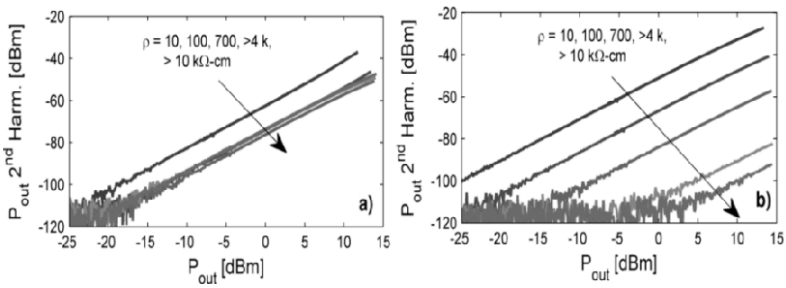

Figure 13.10. *Measured 2nd harmonic output power of a 2,146 µm-long CPW line on n-type Si with different resistivities a) without and b) with a trap-rich polySi layer. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

13.3. Porous Si substrate technology

As described in the introduction (section 13.1), a thick porous Si layer locally formed on the Si wafer can provide an effective RF shielding from the Si substrate for the integration of RF passive devices. The porous Si layer can be formed on the low-resistivity CMOS Si substrate, using CMOS-compatible processing. This is the only technology implemented on the low-resistivity Si substrate and it is thus the only viable solution investigated so far for the co-integration of CMOS logic and RF analog ICs on the same chip, paving the way toward the logic/RF SoC of the future.

Monolithic microwave integrated circuits (MMIC) are intensively investigated toward achieving higher frequencies of operation to cover the millimeter-wave

frequency bands [GIA 06b, DOA 04, RIE 04, KUH 04]. Passive elements, particularly transmission lines (TLs) for matching networks, baluns, power splitters and filters, are indispensable in millimeter-wave (mmW) systems. Two topologies of TLs are currently used, the CPW and the microstrip (MS). Using CPW topology and CMOS process steps, high-performance silicon-integrated passive devices are currently developed on HR silicon and on silicon-on-insulator (SOI). However, the above substrates are not compatible with the low-resistivity CMOS logic Si substrate and have higher cost compared with the bulk low-resistivity Si wafers. Furthermore, the characteristic impedance of CPW TLines on these substrates is limited to a maximum of about 70 Ω. The state-of-the-art attenuation constant of CPW TLines achieved with SOI or HR substrates is ~0.4-0.5 dB/mm at 60 GHz [BEL 10, HEI 98, MON 05, GIA 07b, CAT 07, MOR 10, GIA 06c, QUE 10, MON 06, GIA 05, FRA 11, FRA 09, CHE 06, GAR 04]. MS TLines realized with a dedicated mm-wave technology having two thick metal layers of 3 μm show almost the same performance, with attenuation constant ~0.5 dB/mm at 60 GHz for 50-Ω characteristic impedance TLines [BEL 10, FRA 11]. Using the most advanced technology nodes, an attenuation constant of 0.9 dB/mm at 60 GHz has been recently obtained [MOR 10] using sub-32 nm CMOS technology, ~10 Ω.cm Si substrate and MS TLine topology. This result can be only achieved with MS TLines since the attenuation constant for CPW TLines would exceed 2–3 dB/mm at 60 GHz [GIA 06c] due to significant losses into the low-resistivity Si substrate. As already mentioned, another issue with the back-end-of-line stack thickness reduction is the technological difficulty to realize high-characteristic impedance TLines (>70 Ω) with low attenuation constant. Such TLines are important building blocks of baluns, filters, couplers and power splitters. The solution to this is given by the local porous Si substrate technology. The effectiveness of the RF isolation provided by porous Si for frequencies up to 20 GHz and 50-Ω characteristic impedance CPW TLines has been demonstrated in [CON 07, CON 08a, CON 08b and ZAC 09]. Within the EU NoE Nanofunction, the investigation was extended to frequencies up to 210 GHz and it was demonstrated that porous Si performs also well at these high frequencies.

In this section, the fabrication and general properties of porous Si is presented and discussed. The characteristics of different RF devices, including CPW TLines, inductors and antennas on porous Si are analyzed, demonstrating the effectiveness of porous Si as a local low loss RF substrate on Si.

13.3.1. *General properties of porous Si*

Porous Si shows many interesting properties that make it appropriate for this application. These include the following:

– The fabrication process is compatible with CMOS processing.

– Implementation of the fabrication process into CMOS fabrication process steps is possible [KIM 03, CON 08a, CON 08b, ZAC 09].

– There is near zero mismatch in the thermal expansion coefficient between porous Si and bulk Si. This is a major advantage of porous Si over Si oxide, since several hundred μm thick porous Si layers can be fabricated on Si. This is not possible with SiO_2.

– Porous Si layers of a desired surface area and thickness can be grown locally on the Si substrate in Si-compatible processing.

– The relative dielectric constant and loss tangent of porous Si are adjustable by changing the structure and morphology of the material. This is achieved by changing the electrochemical conditions of porous Si formation and the type and doping density of the Si substrate. This is important for the design of RF devices with the adequate characteristics.

Porous Si is formed by electrochemical dissolution of bulk crystalline Si in HF-containing electrolytes. Pore formation is based on the existence of free holes in the Si substrate that recombine with F^- ions from the electrolyte. Consequently, without sample illumination, porous Si can be formed on p, p^+ type Si. Porosification of n-type Si is made under illumination. The electrochemical process is performed in single- or double-tank Teflon cells, with the Si wafer surface to be anodized in contact with the electrolyte. Usually anodization takes place under constant current density. The resulting material on p-type Si is sponge-like with isotropically distributed pores, while on p^+ Si vertical pores with lateral dendritic branching are obtained. On n-type Si under illumination, large macropores are obtained. More information on porous Si formation is found in [CAN 97] data reviews.

The structure, morphology and porosity of porous Si layers depend on the electrochemical conditions used (electrochemical solution, current density and etching time) and the starting wafer type and resistivity [CAN 97].

The porosity is defined as the fraction of void within the porous Si layer and can be determined easily by weight measurements. The unused wafer is first weighed before anodization (m1), then just after anodization (m2) and finally after dissolution of the whole porous Si layer (m3). The porosity is given by

$$Porosity(\%) = 100 \times \frac{m1 - m2}{m1 - m3}$$

Depending on the porosity, the material is characterized as microporous (pore size <2nm, mesoporous (pore size 2–50 nm) and macroporous (pore size >50 nm). An example of a cross-sectional high-resolution SEM image of a porous Si layer

formed on p^+-Si is shown in Figure 13.11. The layer shows vertical pores with a dendrite branching structure. In general, by increasing the porosity the dendrite tends to disappear and the pore walls become smoother.

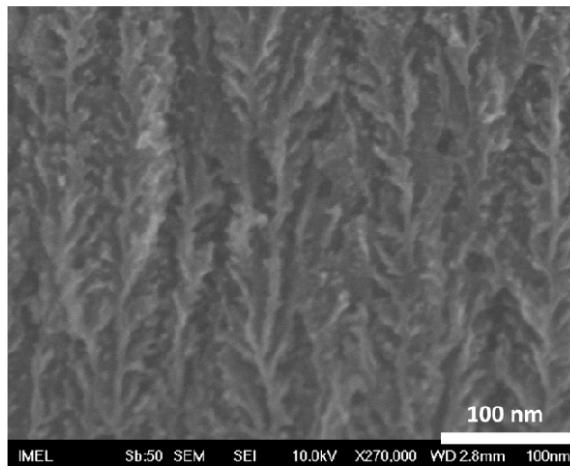

Figure 13.11. *Example of cross-sectional SEM image of a porous Si layer of 70% porosity on p^+-type Si*

Porous Si can be locally formed on Si by using adequate masking layers. Depending on the desired porous Si layer thickness, a different mask can be used. For thin porous Si layers (short anodization times), a conventional photoresist can be used, as for example the AZ 5214 photoresist. An SiO_2 or SiN3H4-masking layer can be used for slightly thicker layers. However, for very thick layers more robust masks should be used. A perfect mask is a bilayer of poly Si/SiO_2 [KAL 98]. This mask is totally resistant to the anodization solution and can be used for anodization times of several hours. The entire process is CMOS compatible and takes place at room temperature.

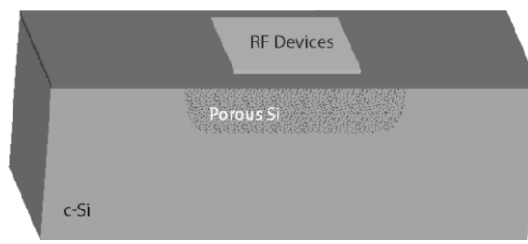

Figure 13.12. *Schematic representation of a locally formed porous Si layer on the Si substrate. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

13.3.2. *Dielectric properties of porous Si*

The dielectric properties of porous Si were investigated by fabricating thick layers of this material (150 μm thick) on the Si wafer and integrating Al CPW TLines on top of them [SAR 11]. The S-parameters of the TLines were measured, from which, in combination with electromagnetic simulations, the dielectric properties of the porous Si substrate were deduced.

Three different samples with porous Si layers of the same thickness (150 μm) and different porosity were fabricated [SAR 11]. The starting Si wafer was p+-type with a resistivity of 5 mΩ.cm. The electrolyte used was HF: ethanol 40:60 v.v. The current density used was 20, 40 and 60 mA/cm2 for a corresponding porosity of 70, 76 and 84%, respectively. Pore morphology was of a dendrite type with an average pore diameter of 30–35 nm.

Similar CPW TLines were fabricated on top of these layers by depositing a 1 μm thick Al layer and patterning it by photolithography and etching in order to form the CPW topology (see Figure 13.13). The signal line width (*W*) of the CPW TLine was 80 μm, the ground width (*Wg*) was 780 μm and the gap (*G*) between signal and ground was 35 μm. The length of the lines was 5 mm.

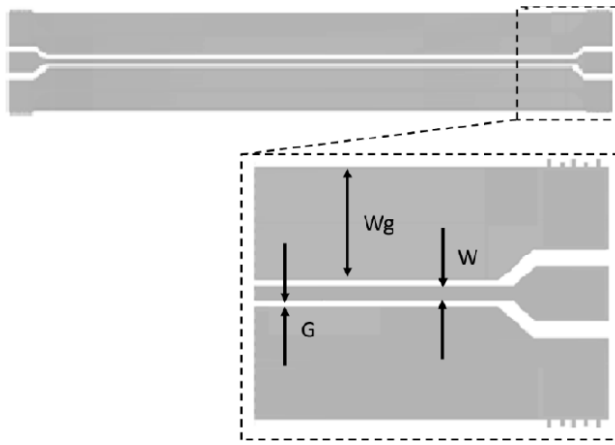

Figure 13.13. *Schematic representation of a CPW transmission line. The signal line (W) is separated from the two grounds (Wg) by the spacing (G)*

Figure 13.14 shows the measured S_{11} parameters for all three samples. It can be easily seen that the frequency position of the resonance is different for each sample. This is attributed to the difference in the dielectric constant of the PSi layer, since all other parameters are nominally the same in all three samples. Moreover, a right shift

in the resonance by increasing the current density, and hence the porosity, is indicative of a reduction in the value of the dielectric constant.

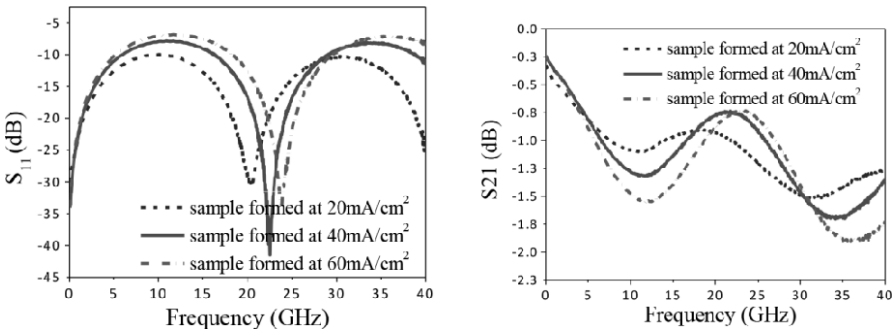

Figure 13.14. *S_{11} (left) and S_{21} (right) parameter measured for the CPW TLines on the three different porous Si layers*

Using the S_{11} and S_{21} parameters, the power loss can be extracted for each sample using:

$$Power\ \ Loss = 1 - \left|S_{11}\right|^2 - \left|S_{21}\right|^2$$

Figure 13.15 shows the calculated power loss as a function of frequency for all three samples. The sample with 70% porosity shows the largest power loss, while the two other samples show the similar power loss and lower than that of the 70% porosity sample. These results can be explained by considering both porosity and DC conductivity of the samples. The sample formed at 20 mA/cm^2 not only has the lowest porosity but also the maximum DC conductivity between all samples. This is why it shows the largest power loss. On the other hand, the two other samples have values of porosity that are very close to each other. Also, their DC conductivity for small bias voltages is similar and lower than that of the 70% porosity sample.

A methodology was developed to extract the dielectric parameters of the porous Si layers from the broadband electrical measurements of the CPW TLines on top of these layers [SAR 13a, SAR 13b]. From the S-parameters, $\varepsilon_{r,\mathrm{PSi}}$ is extracted by calculations [SAR 13a] and a simulation of the CPW TLine on an ideal substrate with permittivity equal to $\varepsilon_{r,\mathrm{PSi}}$ and loss tangent equal to zero ($tan\delta$ = 0) is performed. With the simulation result and the initial measurements, one can finally extract the loss tangent of PSi through straightforward calculations [SAR 13a].

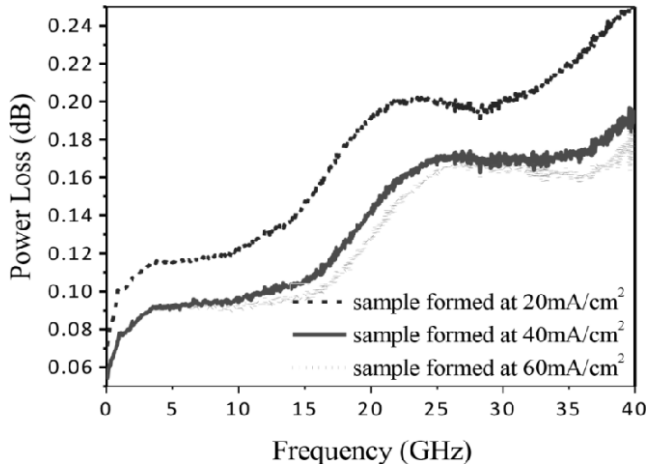

Figure 13.15. *Power loss of the CPWs on the three different PSi layers*

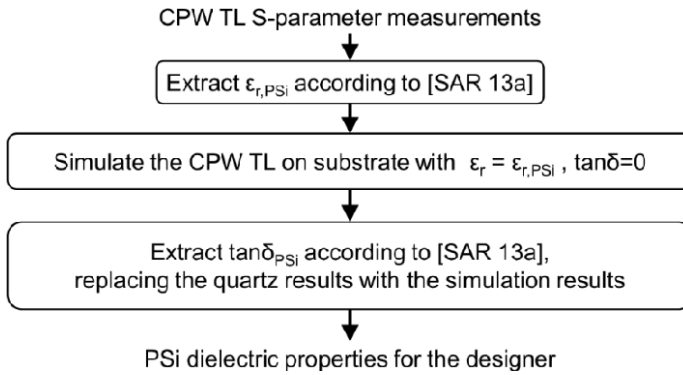

Figure 13.16. *Successive steps of the extraction method used to extract the dielectric parameters of PSi*

An example of the real part of dielectric permittivity for the three samples described is shown in Figure 13.17. This value decreases with increasing porosity and it becomes as low as ~2 for the 84% porosity layer. This gives a real advantage to designers for the design of devices of different characteristic impedance that is necessary in a number of applications. This is not possible with other RF substrate materials, as for example with a HR-Si substrate.

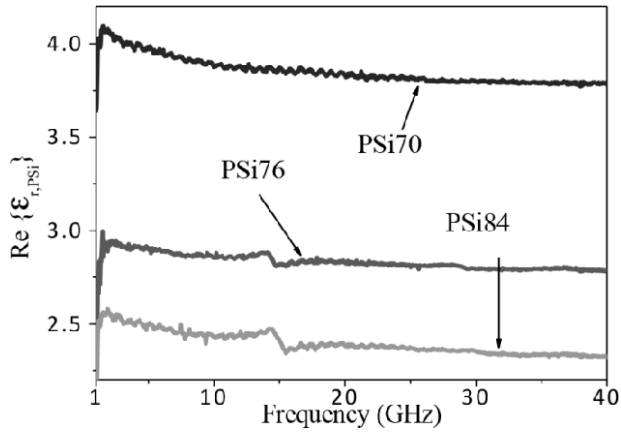

Figure 13.17. *Real part of the relative permittivity over the 0–40 GHz frequency range for three porous Si layers of different porosity (70%, 76% and 84%)*

Figure 13.18 shows the polarization loss (imaginary part of dielectric permittivity) for the three different samples studied. We expected a decrease in the polarization loss with increasing material porosity. However, the result is slightly different. PSi 84 shows slightly higher values than sample PSi76. This can be attributed to a possibly different material morphology in the case of sample PSi76, that is in favor of reducing dielectric losses.

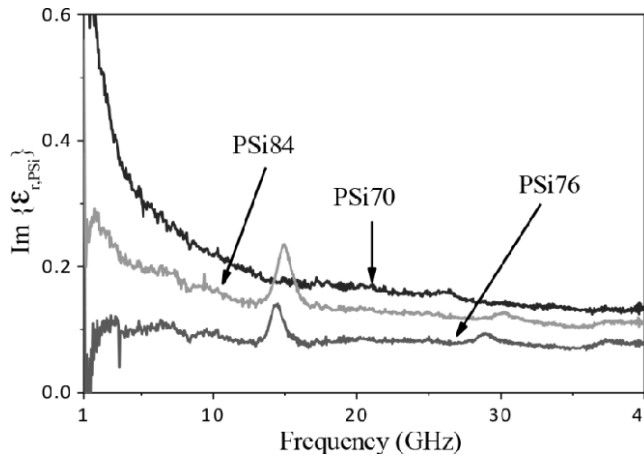

Figure 13.18. *Imaginary part of the relative permittivity over the frequency range 0–40 GHz for the three porous Si layers of different porosity (70%, 76% and 84%)*

13.3.3. *Broadband electrical characterization of CPWT Lines on porous Si*

13.3.3.1. *Frequency range 0–110 GHz*

Coplanar waveguides of two different characteristic impedances, namely 50 Ω (CPW1) and 145 Ω (CPW2), were fabricated on porous Si [ISS 11]. The porous Si layers were fabricated using a current density of 20 mA/cm^2 and the resulting layer thickness was 150 μm. This thickness was selected as sufficient to provide effective shielding from the Si substrate [ZAC 09].

The Al CPW TLines were realized using 1 μm thick Al layer, deposited by electron gun evaporation and patterned by standard photolithography and etching. The CPW TLines were measured from DC up to 110 GHz. In order to extract the electrical parameters using the measured scattering parameters of the TLines, several methods were compared and used [FER 94, MAN 06].

Figure 13.19 shows the extracted values of the characteristic impedance of both TLs, from DC up to 110 GHz. Simulations with Ansys HFSS [HFS 12] are in very good agreement with measurements. The resonance of both transmission lines appears at ~40 GHz. Also, the ripples that appear beyond 65 GHz are attributed to the dynamic range of the measurement system used in the 65–110 GHz band, and some inaccuracies in the de-embedding procedure [MAN 06]. Figure 13.20 shows the extracted and the simulated effective relative permittivity and phase velocity versus frequency. Excellent agreement is obtained between simulated and measured values.

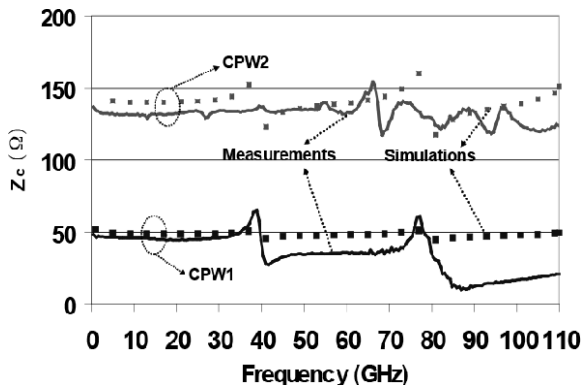

Figure 13.19. *Measured (solid lines) and simulated (dotted lines) characteristic impedance versus frequency [ISS 11]*

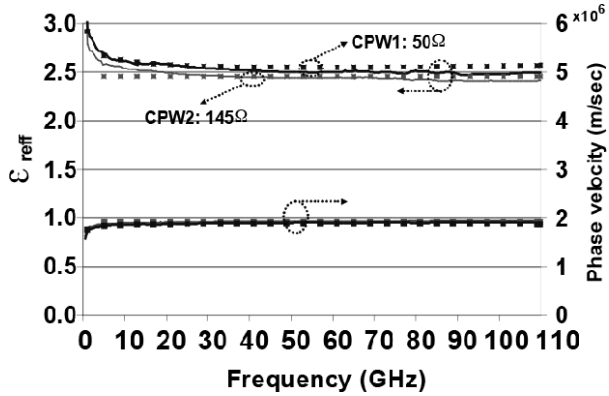

Figure 13.20. *Extracted (solid lines) and simulated (dotted lines) effective relative permittivity (right axis) and phase velocity (left axis) versus frequency [ISS 11]*

Figure 13.21 shows the extracted attenuation constant versus frequency. The measured attenuation constant is as low as 0.32–0.35 dB/mm at 60 GHz and ~0.55 dB/mm at 110 GHz for both TLines. These values are very competitive as compared with the present state of art of CMOS TLines. In order to clarify this, the CPW1 (Zc = 50 Ω) attenuation constant is compared with other 50-Ω TLines realized using different technologies. The comparison was carried out at 60 GHz and 110 GHz. Figure 13.23 shows the measured attenuation constants (in dB/mm) for the considered 50-Ω TLines. For a fair comparison, the topology, the metallization layer, material (Cu or Al), total thickness of the metal layers and the resistivity (ρ) of the substrate were specified for each case of the corresponding technology.

In Figure 13.23 it is depicted that the attenuation constant obtained for TLines on porous Si is lower than all addressed CMOS-compatible technologies. Lower attenuation constant can be obtained with non-CMOS solutions, for example with a thick BCB dielectric.

Figure 13.22 shows the extracted quality factor of the two TLines. The measured quality factor is between 20 and 30 from 50 to 110 GHz for both TLines. Figure 13.24 compares the quality factor of the CPW1 with that of the 50-Ω TLines considered in Figure 13.24, at 60 GHz. We see that the value of the quality factor obtained with CPW TLines on porous Si not only is much better than the conventional CPWs on p-type silicon (Q ~ 3 at 60 GHz in CMOS 65 nm technology), but also is comparable with the best existing TLines using more

complex topologies [FRA 11, FRA 09, CHE 06, CAR 04]. It is worth recalling that the above results were obtained using only a single 1 µm-thick Al metal layer. Hence, these results could be further improved if a thick copper metal strip is used.

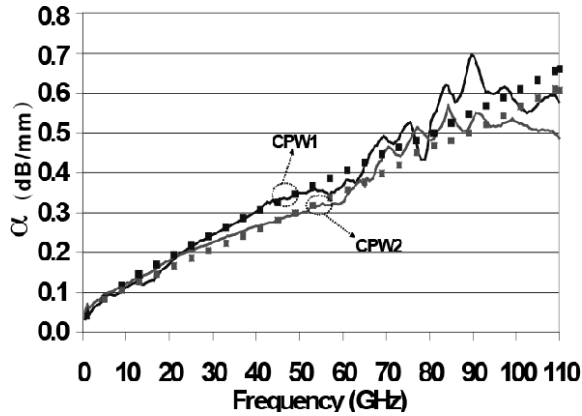

Figure 13.21. *Measured attenuation constant of the TLs investigated in this work, versus frequency [ISS 11]*

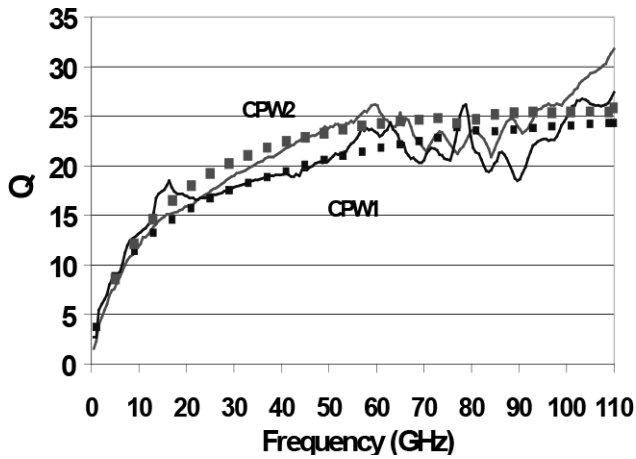

Figure 13.22. *Measured (solid lines) and simulated (dots) quality factor of the two transmission lines CPW1 and CPW2 investigated in this work, versus frequency [ISS 11]*

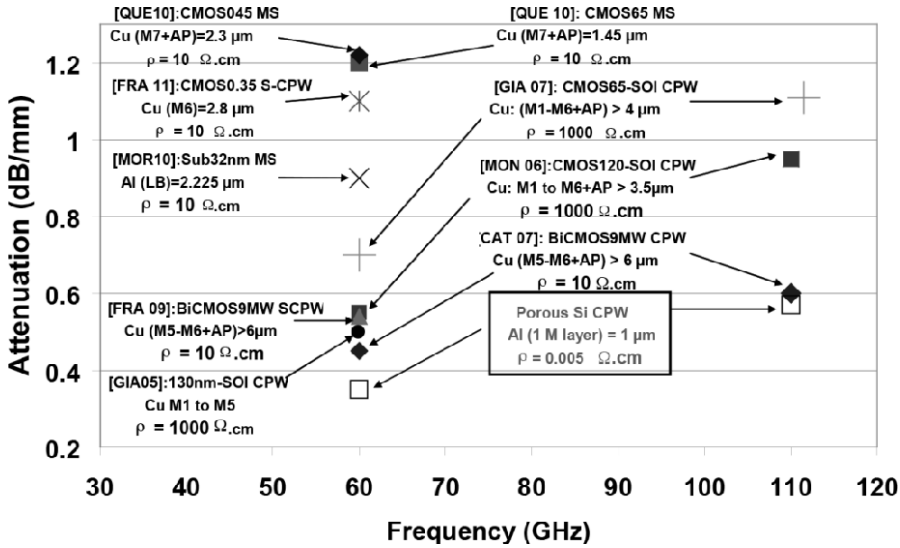

Figure 13.23. *Published (state of the art, see references in brackets) attenuation constant values of 50-Ω TLines realized using different technologies and topologies [ISS 11]*

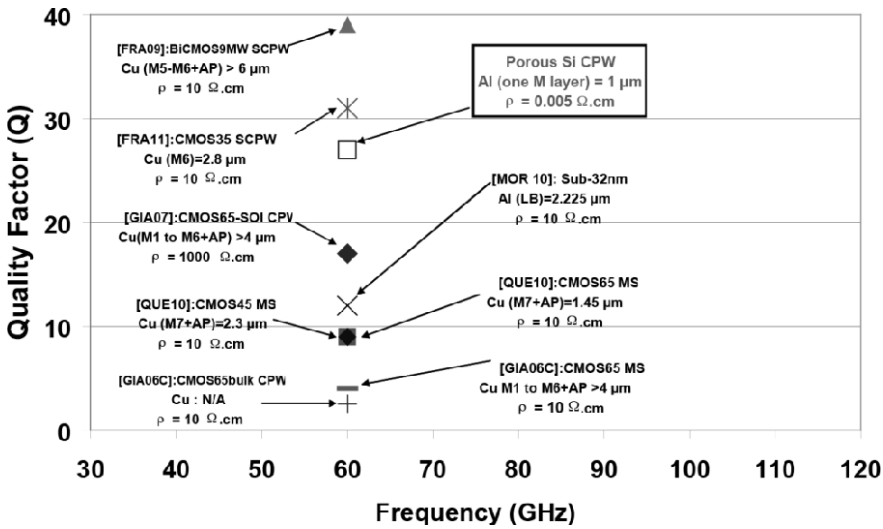

Figure 13.24. *Published (state of the art) quality factor values of 50-Ω TLines realized using different technologies and topologies. The empty square point indicates the quality factor of CPW1 realized on porous Si [ISS 11]*

13.3.3.2. *Frequency range 140–210 GHz*

Further characterization was conducted on CPW TLines in the frequency range 140–210 GHz [SAR 14]. In order to be able to characterize CPW TLines in this frequency range, one should use shorter lines. This was imposed by the fact that at 200 GHz structures that are larger than 500 μm operate as antennas. The lines that were used were designed to have a Zc =100 Ω on porous Si and ~50 Ω on Si. The dimensions were W = 25 μm, G = 8 μm and W_g = 208 μm. The Al thickness was 1 μm. In order to outline the high performance of porous Si, we have included in Figure 13.25 the measurements of the same CPW TLines on standard CMOS Si (1–10 Ω.cm) and on quartz.

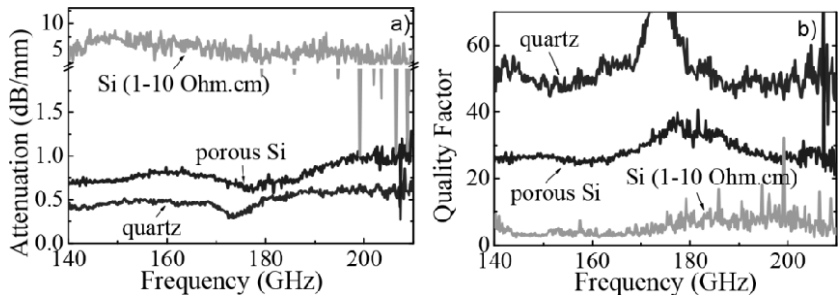

Figure 13.25. *Attenuation a) and quality factor b) of the porous Si layer in the frequency range 140–210 GHz [SAR 14]*

13.3.4. *Inductors on porous Si*

The on-chip integration of good quality, high inductance and high operating frequency inductors is one of the most challenging parts of the CMOS logic/RF analog SoC. In this section, we compare three different substrates for RF inductors, namely two Si-based substrates (porous Si with 70% porosity, $\varepsilon_{r,\mathrm{Psi}} = 4.1$ and standard CMOS Si with resistivity 1–10 Ω.cm) and quartz [SAR 13c]. Similar test inductors were fabricated on the three substrates using 1.3 μm thick Al metal with signal line width of 20 μm and spacing between the spires of 10 μm. The inter-metal dielectric was a 650 nm thick low temperature silicon oxide. The test inductors had a rectangular shape occupying a total area of 280 x 250 μm^2, 370 × 310 μm^2 and 400 × 370 μm^2 for 1.5, 2.5 and 3.5 turns, respectively (see Figure 13.26).

The inductors were characterized up to 18 GHz. As an example, the inductance and the quality factor of the 2.5 turn inductor are depicted in Figure 13.27.

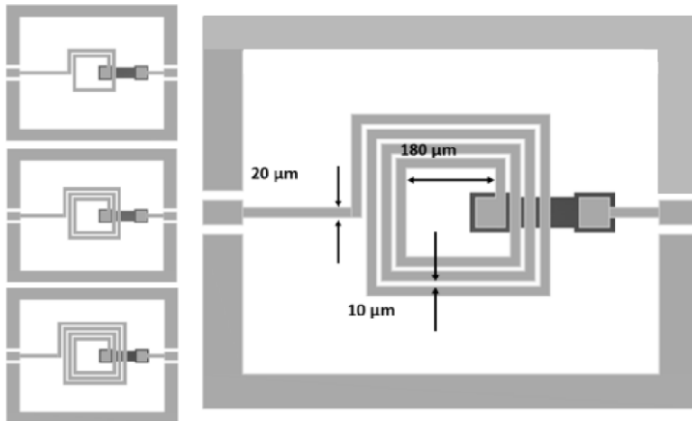

Figure 13.26. *Layout and dimensions of the test inductors fabricated on the four different substrates under test*

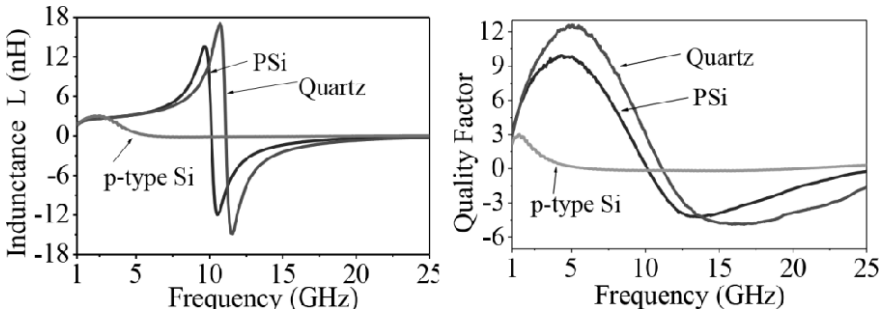

Figure 13.27. *Inductance and quality factor of the 2.5-turn inductor as a function of frequency on three different substrates, porous Si (PSi), p-type Si (resistivity 1–10 Ω.cm) and quartz*

It can be seen that the inductance remains almost constant (~3.2 nH) for all the substrates. It is also worth mentioning that, as expected, the resonance frequency is shifted to higher values as the permittivity of the substrate decreases (here $\varepsilon_{r,\mathrm{Si}}$ = 11.7, $\varepsilon_{r,\mathrm{Psi}}$ = 4.1, $\varepsilon_{r,\mathrm{quartz}}$ = 3.9). This is one of the advantages of porous Si, for which the real part of permittivity is tunable between 2 and 7, thus offering the possibility of designing inductors operating at different frequencies. It is also shown in Figure 13.27 that the quality factor of the inductors on porous Si is close to that of inductors on quartz and is more than 300% better than on low-resistivity Si.

13.3.5. *Antennas on porous Si*

Today the main bottlenecks toward the on-chip antenna integration are the low resistivity and the high-dielectric constant (ε_r = 11.7) of the standard CMOS Si substrate [CHE 13]. The low-substrate resistivity increases losses into the substrate and greatly reduces the antenna efficiency. The high-dielectric constant causes most of the power to be consumed into the substrate instead of being radiated to the free space. As described before, depending on its structure and morphology, porous Si can have a low ε_r ($\varepsilon_{r,\mathrm{PSi}} \sim 2$) and low-dielectric losses. Furthermore, it can be locally formed on the low-resistivity CMOS substrate, thus adding more functionality to this Si substrate by opening the possibility of integrating RF devices on it, including high-performance antennas. The improved performance of a dipole antenna on porous Si compared with a similar antenna on low-resistivity Si is illustrated in Figure 13.28. This figure presents the radiation pattern of a dipole antenna centered at (0,0,0) of the x-y-z axes, with the substrate at $z = -500$ μm and $z = 0$. On the left, the radiation pattern of the antenna on bulk low-resistivity Si is depicted, while on the right, the pattern of the antenna on porous Si is depicted, considered to be within the Si substrate and covering an area of 500 μm around the antenna. The directionality of the antenna on porous Si is clearly illustrated, which is the important advantage of porous Si substrate for the antenna integration. However, we have to mention here that there is also a drawback, and this is the increased size of the antenna due to the low permittivity of porous Si. This drawback is less important as the operating frequency of the antennas increases.

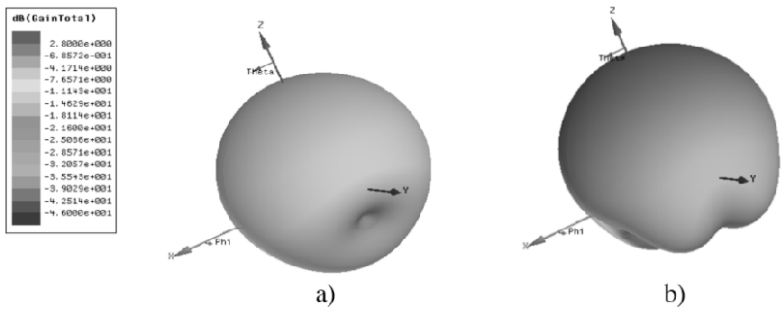

Figure 13.28. *3D representation of the dipole's radiating pattern for low-resistivity Si substrate a) and for porous Si b). The antenna center seats on (0,0,0) and the substrate extends between z=–500 um and z = 0. The results were obtained by HFSS simulations [SAR 13e]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

More results on antennas on porous Si can be found in Chapter 14 of this book and in [SAR 13e].

13.4. Comparison between HR Si and local porous Si substrate technologies

The two substrates that are extensively described in the previous sections are the trap-rich HR-Si and porous Si. Trap-rich HR-Si is the state-of-the-art, commercially available Si-based substrate for RF, which, however, is not compatible with the CMOS Si substrate. On the other hand, porous Si is a promising new substrate that can be combined with the low-resistivity CMOS Si substrate, thus paving the way toward the digital/RF analog SoC of the future. In this section, we provide a fair comparison between the two substrates by integrating on them similar CPW TLines, inductors and crosstalk structures, and comparing their experimental performance [SAR 13c, ROD 13].

The samples used in this study had the following characteristics: the trap-rich HR Si wafer had a resistivity of 10 KΩ.cm and a 300-nm trap-rich polysilicon layer on top. Two porous Si layers were used, one with 74% porosity and a relative dielectric constant of $\varepsilon_{r,\mathrm{Psi}} = 3.3$ that was used for the CPW TLines comparison and other with 70% porosity and $\varepsilon_{r,\mathrm{Psi}} = 4.1$, which was used in the comparison of the inductors [SAR 13a]. The above substrates were also compared with two other substrates, namely standard CMOS Si (1–10 Ω.cm) and quartz. All studied substrates apart from quartz were covered with a 500 nm thick SiO_2 layer.

13.4.1. *Comparison of similar CPW TLines on different substrates*

Similar CPW TLines were fabricated on top of the different substrates under comparison, described above. Their topology is described in section 13.2.1). The metal lines were composed of 1 μm thick Al, deposited on the different substrates using an electron gun evaporator and patterned using photolithography and Al etching. In Figures 13.29–13.32, the different transmission characteristics as a function of frequency in the range (0–40 GHz) are presented.

By design, the CPW TLines on trap-rich HR-Si have a characteristic impedance $Zc = 60\ \Omega$ on porous Si $Zc = 98\ \Omega$ and on quartz $Zc = 80\ \Omega$. The corresponding values as a function of frequency are shown in Figure 13.29. The effective permittivity of porous Si (see Figure 13.30) is the lowest of all studied substrates and it agrees well with the expected one ($\varepsilon_{r,\mathrm{eff,Psi}} = 2.2$). In Figure 13.31, the attenuation loss is presented. It is low for all studied substrates excluding the low-resistivity Si substrates. Porous Si shows an attenuation constant lower than that of the trap-rich HR-Si and comparable with that of quartz. This is partly attributed to the low losses in the substrate and partly to the higher Zc of the CPW TLine on porous Si compared with those on the other substrates. The quality factor (Q) of the lines is presented in Figure 13.32. We see that for all low loss substrates, $Q = 23$–25, whereas the line on low-ρ Si hardly achieves $Q = 1$.

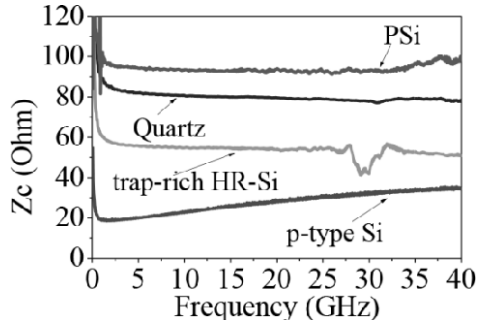

Figure 13.29. *Characteristic impedance (Zc) as a function of frequency of the CPW transmission lines on the four different substrates: porous Si (PSi) with 74% porosity, trap-rich HR-Si, quartz and p-type Si (1–10 Ω.cm) substrates [SAR 13c]*

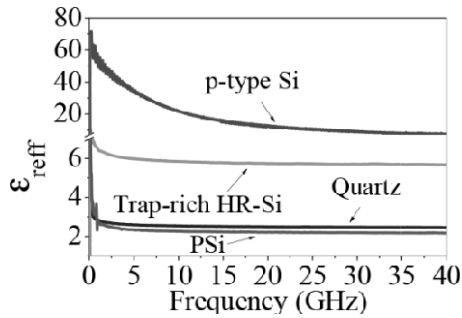

Figure 13.30. *Effective permittivity (ε_{reff}) as a function of frequency of the CPW transmission lines on porous Si with 74% porosity, trap-rich HR-Si, quartz and p-type Si (1–10 Ω.cm) substrates [SAR 13c]*

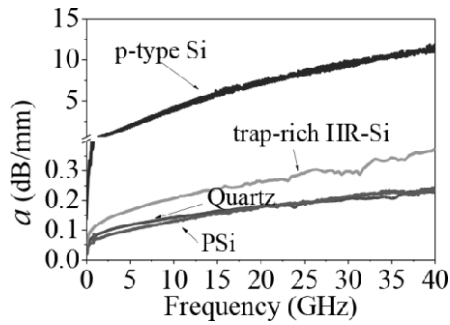

Figure 13.31. *Attenuation constant (a) as a function of frequency of the CPW transmission lines on porous Si with 74% porosity, trap-rich HR-Si, quartz and p-type Si (1–10 Ω.cm) substrates [SAR 13c]*

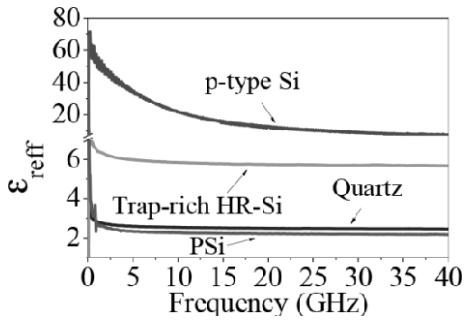

Figure 13.32. *Quality factor (Q) as a function of frequency of the CPW transmission lines on porous Si with 74% porosity, trap-rich HR-Si, quartz and p-type Si (1–10 Ω.cm) substrates [SAR 13c]*

Another parameter to compare is the effective resistivity (ρ_{eff}) of the substrate as this is defined in [LED 05]. The effective resistivity corresponds to the resistivity of an Si substrate with homogenous substrate losses, hence uniform resistivity within the material, which would lead to the same substrate losses with the obtained physical ones. The permittivity used for the extraction of ρ_{eff} was taken as 3.3 and 11.9 for the PSi layer and the trap-rich HR-Si substrate, respectively. In the effective resistivity parameter, not only the resistivity profile is taken into account, but also the field penetration inside the substrate. The obtained results are shown in Figure 13.33(a). We can see that the extracted effective resistivity of the PSi layer is much higher than that of the trap-rich HR-Si, with the last being limited by the nominal resistivity of the initial HR-Si.

The nonlinear behavior of the substrate is described by the total harmonic distortion (THD) of the CPW TLine and is shown in Figure 13.33(b). The THD in our case corresponds to the detected second harmonic component at the output of a 2,146 μm-long CPW TLine when a signal at 900 MHz is injected at the input. It is worth noticing that it has been experimentally proven that the harmonic distortion due to nonlinearities coming from the Si substrate is governed by the second harmonic component [ROD 12]. As expected, the distortion observed for the standard-Si is extremely high (THD > –40 dBm at P_{out} = 15 dBm). On the other hand, both porous Si and trap-rich HR-Si have much lower distortion levels and are well suited for the integration on them of RF transmitter modules for today's multi-standard cellular applications [RAS 97]. More specifically, the investigated porous Si substrate presents an even better response than trap-rich HR-Si in its linear performance, since it has a THD of at least 20 dB lower than the trap-rich HR-Si substrate. Both PSi and quartz substrates present THD levels lower than the noise floor of the measuring system (NF < –110 dBm) and they can be considered equivalent in terms of substrate linearity.

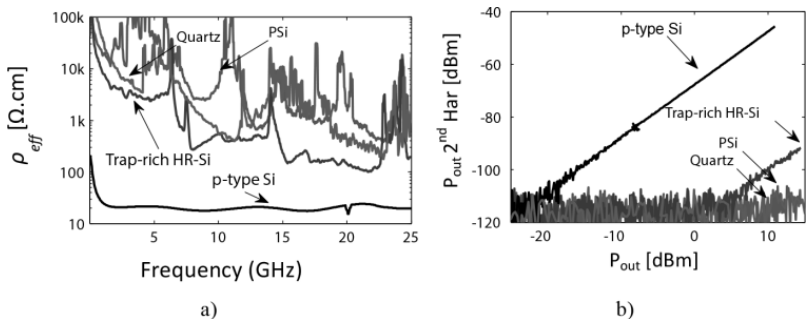

Figure 13.33. *Effective resistivity and second harmonic distortion of CPW TLines on the four substrates under comparison [SAR 13c]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

13.4.1.1. *Crosstalk characterization*

The crosstalk characterization was performed with some specially-designed structures as is shown in the inset of Figure 13.34. The dimensions of the metallic taps are 100 μm × 150 μm, bearing a gap of 30 μm.

The crosstalk as a function of frequency is shown in Figure 13.34 for the investigated substrates. It is depicted that, due to their HR characteristics, in all three substrates (trap-rich HR-Si, porous Si and quartz), the crosstalk presents a typical 20 dB/dec slope over the whole frequency range [RAS 97]. This typical slope of 20 dB/dec for the crosstalk versus frequency demonstrates that the conductive parasitic coupling into the substrate is negligible. In that case, the crosstalk is only governed by the capacitive coupling into the substrate. The very low relative permittivity of porous Si ($\varepsilon_{r,PSi}$ = 3.3), in combination with its high effective resistivity, results in a crosstalk that is respectively 10 dB and 4 dB lower than that of the trap-rich HR-Si and the quartz substrates.

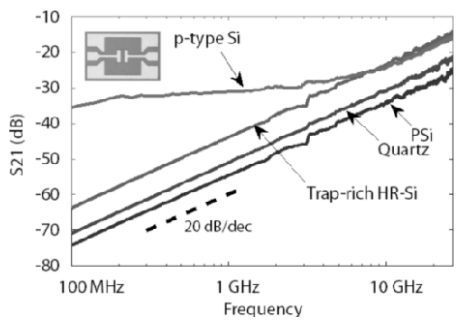

Figure 13.34. *Crosstalk characterization of porous Si, trap-rich HR-Si, quartz and p-type Si (1–10 Ω.cm) substrates*

13.4.2. *Comparison of inductors on different RF substrates*

The rectangular spiral inductors that are described in section 13.2.2 were also integrated on trap-rich HR-Si in order to have a full comparison of the substrates. The porous Si layer used in this comparison was slightly different from the one used for CPW TLine comparison. It had a 70% porosity and a dielectric constant εr,Psi = 4.1.

The inductance and the quality factor of the inductors over the studied frequency range are presented in Figure 13.35. The quality factor of the inductor on porous Si is similar to that on the trap-rich HR-Si and on quartz. It has to be mentioned that the inductors were designed for integration on a Si substrate and not specifically on PSi, a point that supports the assumption that there can be further improvement on the performance of the inductors on porous Si. The present results boost the conclusions of the CPW TLine structures measurements, i.e. a local PSi layer on a Si substrate is slightly better for RF shielding than the trap-rich HR-Si.

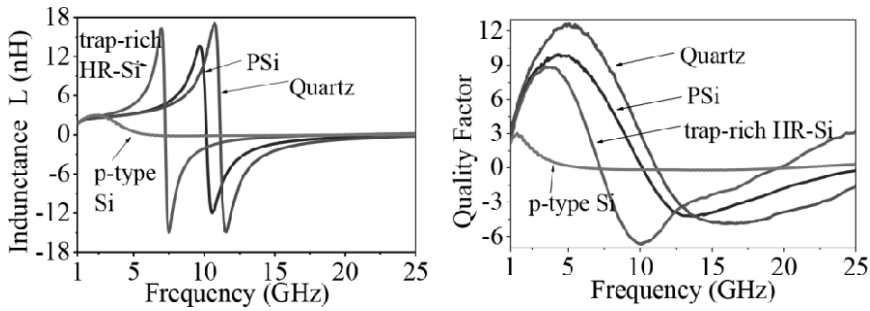

Figure 13.35. *Inductance (L) of the 2.5-turn inductor as a function of frequency on porous Si, trap-rich HR-Si, quartz and p-type Si (1–10 Ω.cm) substrates*

The analytical characteristics of the inductors on all four substrates can be seen in Table 13.2.

13.5. Design of slow-wave CPWs and filters on porous silicon

Slow-wave CPWs (S-CPWs) and filters on a locally grown porous silicon layer, with dielectric parameters $\varepsilon_{r,\mathrm{Psi}} = 3.85$ and $tan\delta = 0.029$, were designed. Low and high-characteristic impedance transmission lines were targeted. The idea of these designs was to assess the interest of using porous Si as a local substrate on the low-resistivity Si wafer to improve their performance.

No. of turns	Substrate	*De-embedded characteristics*			
		L (nH)	Q	f_{res} (GHz)	f_{Qmax} (GHz)
1.5	Quartz	1.29	13.5	22.4	8.5
	Porous Si	1.23	11.2	20.4	7.7
	Trap-rich HR-Si	1.32	12.7	18.8	7.7
	p-type Si (1–10 Ω.cm)	1.1	4.0	12.7	2.4
2.5	Quartz	3.24	12.6	11.1	5.0
	Porous Si	3.2	9.8	10.16	4.8
	Trap-rich HR-Si	3.4	8.8	7.23	3.6
	p-type Si (1–10 Ω.cm)	2.6	3.0	6.1	1.5
3.5	Quartz	6.5	10.6	7.1	3.5
	Porous Si	5.8	8.1	6.17	2.7
	Trap-rich HR-Si	6.3	8.1	5.49	2.7
	p-type Si (1–10 Ω.cm)	5.2	2.6	2.8	1.1

Table 13.2. *Inductor characteristics for the four substrates under test*

13.5.1. *Slow-wave CPW TLines on porous Si*

The slow-wave topology of CPW TLines was tested on a porous Si substrate by designing different S-CPW TLines on this substrate and comparing their characteristics. Figure 13.36 shows the different vertical dimensions (heights and thicknesses) of the considered fabrication technology along with the topology of the S-CPW TLines. The different dimensional parameters are shown in the figure. The shield consisted of strips of width SL separated by a gap SS.

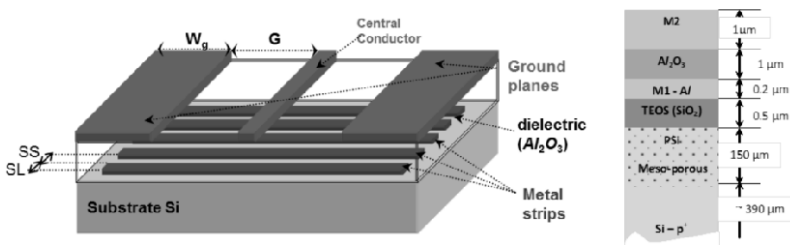

Figure 13.36. *(Left) 3D view of the S-CPW TLines with its dimensional parameters (right) description of the fabrication technology considered in the simulations. The inter-metal dielectric was considered to be a 1-µm thick alumina (Al_2O_3) layer. A 500 nm thick TEOS Si oxide was considered on top of the porous Si layer. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

13.5.2. *Simulation results for S-CPW TLines*

In this section, we present the simulation results of the different S-CPW TLines on porous Si that have been investigated. A very advanced process is considered for their fabrication.

Table 13.3 summarizes the characteristics of the designed S-CPW TLines at 30 GHz and 60 GHz. The dimensions of the shielding plane are fixed at SL = 1μm and SS = 2μm. The reason of choosing these values is twofold: (1) to show the obtained slow-wave effect of this type of TLines and (2) to show the importance of the presence of the PSi membrane. The presence of the shielding strips assures small size and high Q-factor, because of the transmission lines, due to the high slow-wave ratio defined as the ratio between the phase velocity of an S-CPW TLine and that of a CPW TLine on the same substrate.

Table 13.3 summarizes all the physical dimensions (in μm) of some of the designed transmission lines and their extracted electrical parameters, i.e. the characteristic impedance Zc in Ω, the effective relative permittivity $\varepsilon_{\text{reff}}$, the attenuation constant α in dB/mm and the quality factor Q.

Figure 13.37 shows the extracted effective relative permittivity ($\varepsilon_{r,\text{eff}}$) versus Zc (in Ω). For a fixed electrical length, a higher value of $\varepsilon_{r,\text{eff}}$ means smaller physical transmission line length. It can be observed that the transmission line HH has the highest value of $\varepsilon_{r,\text{eff}}$, exceeding 60 at 60 GHz. Increasing the value of the characteristic impedance of the S-CPW TLine while keeping a constant value of the gap G, decreases the value of $\varepsilon_{r,\text{eff}}$. We can also notice that reducing the width of the ground planes (W_g) decreases the value of the effective relative permittivity. However, the change in this value is less remarkable as the characteristic impedance of the transmission line increases (W decreases). On the other hand, by decreasing the value of the gap G, the value of $\varepsilon_{r,\text{eff}}$ decreases, as expected.

Figure 13.38 shows the corresponding quality factor values at 60 GHz versus the characteristic impedance of the same S-CPW TLines as shown in Figure 13.37. The highest value of Q was obtained for the S-CPW HH. The S-CPW OO on the other hand has a relatively small quality factor.

It can be noticed that by increasing the value of Zc (for a fixed value of G), the value of the quality factor of the transmission line decreases. By decreasing the value of W_g, both the value of the characteristic impedance and the quality factor of the S-CPW TLines increase.

Name	W_g	W	G	Zc	ε_{reff}	At 60 GHz		At 30 GHz	
						a(dB/mm)	Q	a(dB/mm)	Q
A	10	2.5	50	73.9	19.6	1.08	22.4	0.73	16.5
B	10	2.5	100	80.7	24.2	1.02	26.3	0.79	17.07
C	10	5	50	57.8	25.6	0.99	27.9	0.65	21.4
D	10	5	100	63.6	32.2	0.95	32.7	0.64	24.1
E	10	10	50	44.2	34.2	0.94	34	0.61	26.1
F	10	10	100	48.9	43.5	0.9	40.1	0.6	29.7
H	10	15	100	41.4	51.2	0.88	44.3	0.54	35.7
L	10	30	10	22.5	27.4	1.21	23.6	0.8	18.1
N	10	50	10	19.5	31.1	1.26	24.3	0.8	19.2
P	10	100	10	17.7	32.4	1.2	25.8	0.79	19.9
AA	20	2.5	50	69.1	20.5	1.1	22.5	0.75	16.5
BB	20	2.5	100	75.5	25.5	1.05	26.3	0.84	16.3
CC	20	5	50	53	27.9	1.01	28.6	0.66	22
DD	20	5	100	58.6	34.9	0.96	33.5	0.67	23.9
EE	20	10	50	39	39	0.95	35.9	0.6	28.5
FF	20	10	100	43.1	50	0.92	42	0.56	33.6
GG	20	15	50	32.1	47.4	0.93	40.5	0.58	32.3
HH	20	15	100	34.2	61	0.91	47	0.53	32.2
II	20	20	5	19.1	24.7	1.57	17.3	1.01	13.6
JJ	20	20	10						
KK	20	30	5	16.3	28.8	1.56	18.7	1.01	14.7
LL	20	30	10	17.8	37.2	1.33	25	0.86	19.6
MM	20	50	5	13.4	35	1.66	19.4	1.06	15.3
NN	20	50	10	14.8	44	1.36	26.6	0.85	21.3
OO	20	100	5	11.6	42	1.08	16.3		
PP	20	100	10	12.8	48.2	1.27	29.7	0.81	23.3

Table 13.3. *Extracted electrical parameters of the simulated S-CPW TLines at 30 and 60 GHz*

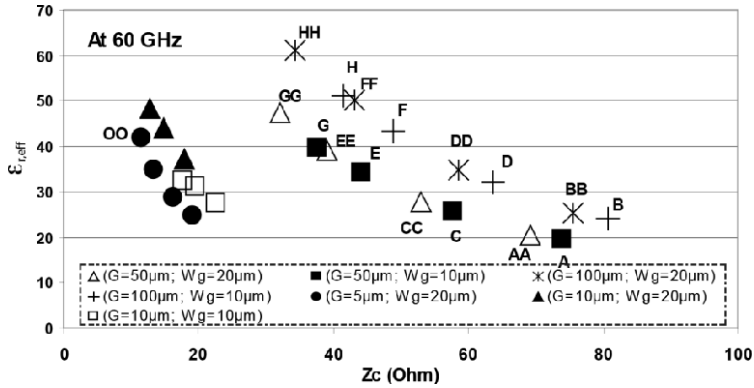

Figure 13.37. *Effective relative permittivity versus characteristic impedance of the S-CPW transmission lines at 60 GHz. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

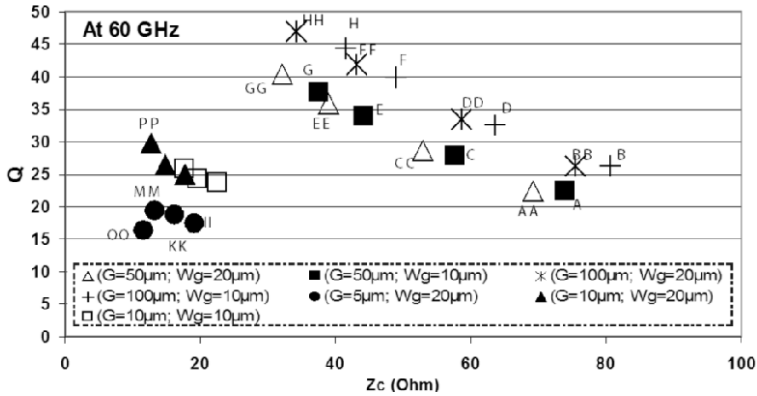

Figure 13.38. *Quality factor of the simulated lines at 60 GHz versus their characteristic impedance. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

In the next section, these transmission lines as well as the transmission lines presented in the previous section are considered in the design of low-pass stepped impedance filters (LPSIF).

13.5.3. *Stepped impedance low-pass filter on porous silicon*

The reason behind choosing the stepped impedance filter (SIF) topology is its simplicity. The idea is to cascade low- and high-characteristic impedance

transmission lines. The higher the value of *Zc*, the better the performance of the TLine, as will be shown in the following sections.

The filters were designed to have a cut-off frequency of 30 or 60 GHz, with a return loss better than 20 dB in the pass-band. The design was carried out for two different filter orders (5 and 7). The out-of-band response must have a good rejection with as high as possible spurious pushed away. Several different transmission lines were designed. They use CPW and S-CPW topologies and different technology parameters (varying for example the thickness of the alumina layer). Below, we present only simulation results of filters having a cut-off frequency of 30 GHz.

In order to obtain the best performance (from the point of view of selectivity and stop-band), S-CPW and CPW with the lowest- and highest-characteristic impedances were considered.

13.5.4. *Simulation results for filters*

We designed here filters using only S-CPW TLines. Three low-pass filters were designed with different thickness of the alumina layer (t_{Al2O3}), varying as follows: t_{Al2O3} = 1 μm (Filter1), 1.5 μm (Filter2) and 2 μm (Filter3).

The transmission lines B and OO from Table 13.3 were used in the filter design. The filter was designed using respectively five and seven TLine elements. By increasing the order of the filter, its physical length increases, but its selectivity and out-of-band rejection level increase as well. Table 13.4 summarizes the characteristics of the transmission lines used for the filter design. The table shows the name of the S-CPW TLine used, its electrical length at 30 GHz, its physical length (L) in μm and the total dimensions of the filter (taking into account the ground planes). For the remaining parameters (electrical and physical), we can refer to Table 13.3.

Figure 13.39 shows the circuit simulation of both types of filters using ideal transmission lines. In all cases, the cut-off frequency is at 30 GHz. We see that, as expected, the increase in the order of the filter induces an increase in its selectivity and out-of-band rejection. The first secondary lobe (spurious: $|S_{21}| > -20$ dB) appears around 60 GHz for the 5th-order SIF. On the other hand, the 7th-order SIF has stop-band rejection that extends up to 77 GHz.

Figure 13.40 shows the layout of the two types of filters drawn using Agilent's ADS. The length and the spacing between the strips remain constant for all the lines.

Filter order	Lines used	β at 30 GHz	L (μm)	Total dimensions (W × L) in μm^2
5	Line 1: B	37°	207	150 × 972
	Line 2: OO	18.3°	78	
	Line 3: B	71.6°	402	
7	Line 1: B	31°	174	150 × 1032
	Line 2: OO	17.8°	75	
	Line 3: B	20.3°	114	
	Line 4: OO	72	306	

Table 13.4. *Optimized values of the SIF filters of order 5 and 7*

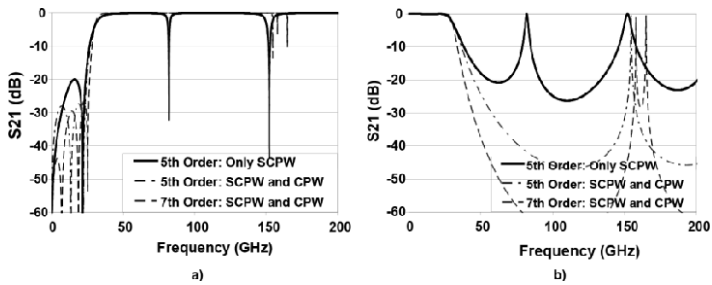

Figure 13.39. *Ideal simulation response of the two types of SIF: a) transmission and b) reflection S-parameters. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

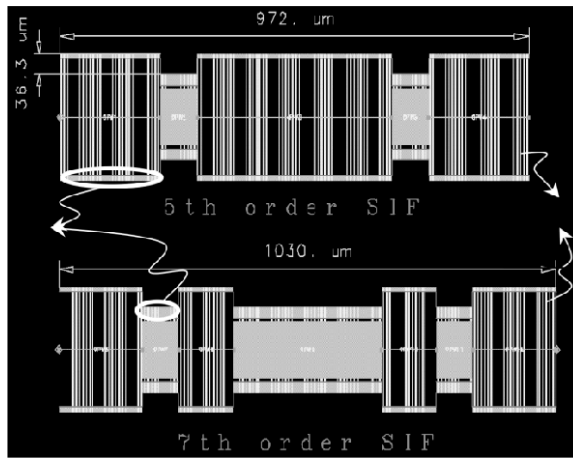

Figure 13.40. *Layout of the two types of SIF. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

13.6. Conclusion

In this chapter, we presented the properties of two different substrates for their use in RF, trap-rich HR-Si and porous Si. The general properties of the trap-rich HR-Si as an RF substrate were first presented in this study. The dielectric properties of porous Si at RF were discussed and high-performance passive devices were demonstrated on this substrate in the frequency range 0–210 GHz. CPW and S-CPW TLines as well as inductors and dipole antennas were investigated and a fair comparison between trap-rich Si and porous Si was made. This comparison showed the superiority of porous Si for the following reasons: devices with comparable quality factor than on trap-rich Si can be obtained on porous Si. In addition, porous Si offers flexibility to design devices with high-characteristic impedance, due to its tunable dielectric constant that can be as low as ~2. This is also an advantage for the antennas, since it offers better directionality of the radiation pattern that does not go into the substrate. LPSIFs on porous Si were designed and their characteristics were presented. The idea is to cascade CPW TLines, with high-characteristic impedance and low loss achieved with the porous Si substrate, with S-CPW TLines with low impedance. These filters show great potential in different applications.

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14

Metal Nanolines and Antennas for RF and mm-wave Applications

14.1. Introduction

As the continuous scaling of the transistor extends its capability well into the mm-wave frequency range, there is a need to develop high-quality passive components to improve both circuitry performance and system integration density [ZHA 09]. In current CMOS technology, the transmission lines for the RF circuits are fabricated on the top metal layer of the back-end-of-line (BEOL). The thickness of this metal is in the order of few microns and therefore the designers can benefit from the lower conductor losses. However, the feasibility to use lower-level metal layers in BEOL, with smaller thickness, is rarely investigated, but it is of great interest as the size of the active devices approaches the nanometer dimension. Interconnects in this case must be developed to be suitable for the circuit speed expected from miniaturization. Nanotubes and metal nanowires (nanolines) are expected to play an important role as high-frequency interconnects in future nanoelectronics, for transmitting signals between nano-components and connecting the nano-devices. Additionally, in wireless communications, nano-antennas based on nanotubes and nanowires can be investigated for use in connecting nanoelectronic devices to the macroscopic world and making potential high-density circuitry possible.

Only few works are found in the literature on this topic. In [STE 05, HAN 02, HIN 01], the authors have studied Cu nanolines realized using standard processes. The width of the smallest structure was 40 nm and of the largest 1,000 nm, and their thickness was 50, 155 or 230 nm. Line resistivity was measured and was found to

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Chapter written by Philippe BENECH, Chuan-Lun HSU, Gustavo ARDILA, Panagiotis SARAFIS and Androula G. NASSIOPOULOU. The presented results were obtained within the EU FP7 NoE Nanofunction.

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increase as the width of the line decreases. In [KIM 11, RIC 10], RF characterization up to 50 GHz of Pt NWs with 100 and 300 nm width was performed by combining a full-wave finite element method modeling and RF measurements. In previous studies, the measured conductivities of Au [SMI 00] and Cu [MOL 03] nanowires (NWs) were found to be lower than their bulk values, this being attributed partly to the effect of the contact resistance between the pad and the nanowire. In addition to metal nanowires, a lot of research is devoted to carbon nanotubes (CNTs) for electronic applications [MAD 10], some of them dealing also with RF applications [WAL 11].

Today, the on-chip transmission lines for silicon monolithic-integrated millimeter-wave (mm-wave) circuits are made of metals like copper and aluminum. Their line width and thickness is not less than 1 μm in the most advanced back-end-of-line (BEOL) CMOS technology for RF and mm-wave applications, thereby ensuring a low insertion loss and a good impedance matching [QUE 10]. As in all technology-scaling scenarios, metal losses increase significantly with decreasing size, especially when the line width and thickness come close to 100 nm. The DC metal conductivity degrades due to surface and grain-boundary scattering. Wires are also more vulnerable to electromigration [DUR 00] than thicker lines. From this point of view, metallic carbon nanotubes outperform metal nanowires. They exhibit ballistic flow of electrons with an electron mean free path of several microns and are capable of carrying large current densities [WHI 01]. On the other hand, due to the lack of sufficient control over geometry during CNT fabrication, metal nanowires can be advantageous over carbon nanotubes in this respect. So far, CNTs and solid metal nanowires have received equal attention regarding their RF interconnect applications and they are studied in parallel.

In this chapter, we will describe some recent advances in the above field, performed within the EU FP7 NoENanofunction network of excellence.

14.2. Metal nanowires (nanolines)

14.2.1. *General properties*

14.2.1.1. *Fabrication*

Nanolines can be fabricated either by metal deposition and patterning using e-beam lithography or by chemical synthesis. As this chapter focuses on nanolines that are horizontal to the Si wafer surface, the fabrication description is limited to the first case of metal deposition and patterning. In general, a two-lithography-step process is used, one to pattern the nanolines (using electron beam lithography) and the other to form the pads (using optical lithography). In this way, different metal thicknesses can be used for the nanolines and the pads (using thicker metal layers for

the pads to reduce series resistance). The different fabrication steps are illustrated in Figure 14.1, where cross-sectional schematic images of the different layers on Si during the successive fabrication steps are shown.

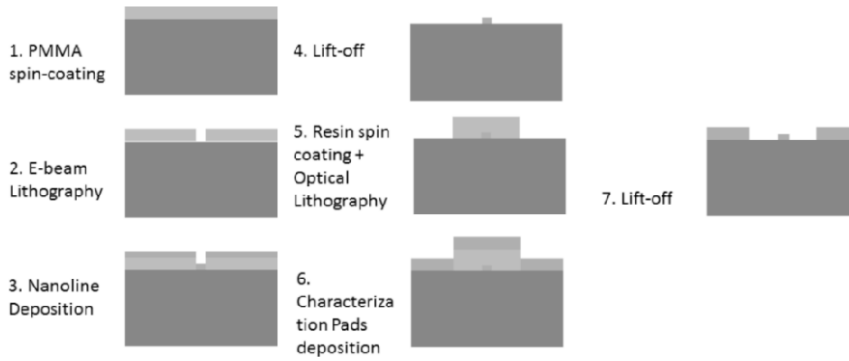

Figure 14.1. *A typical two-step process for fabricating horizontal metal nanolines and their characterization pads. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

In this study, metal nanolines from aluminum, gold and copper, in single and multiple-line configuration, are examined. These materials were chosen either because they are standard in CMOS processing (Al, Cu) or because they are not oxidized in air (Au), and thus constitute model materials for elucidating the mechanisms involved in the nanolines' electrical behavior. In Figure 14.2, an example of parallel copper nanolines fabricated by electron beam lithography is shown.

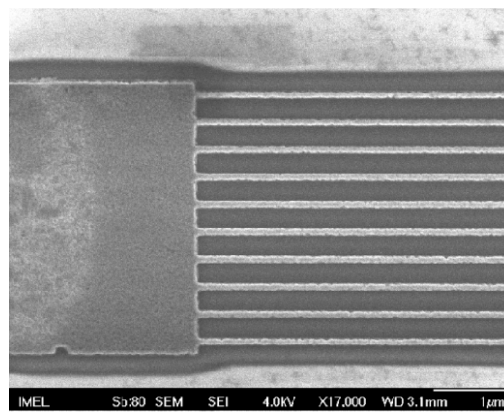

Figure 14.2. *SEM image of parallel copper nanolines on a porous Si substrate, fabricated using e-beam lithography and lift-off. The nanoline width is 150 nm [SAR 12]*

14.2.1.2. *Electrical properties*

While research in metal nanolines at high frequencies is still in its infancy, their DC properties were largely investigated for their use in CMOS circuits. Copper has been used as an interconnect metal in CMOS technology since the late 1990s. It is the material with the highest conductivity among all the metals. However, with the continuous CMOS scaling down to the nm range, copper interconnect technology is currently facing performance limitations due to the increasing interconnect wire resistance. The nanolines fabricated by physical vapor deposition are typically polycrystalline and have rough surfaces. Such nanolines suffer from surface and grain-boundary scattering, which leads to high resistivity [DUR 00]. This resistivity at the nanoscale is much higher than the bulk value, as is illustrated in Figure 14.3 [STE 02, ITR 07]. On the other hand, chemically synthesized nanolines exhibit much lower resistivity than that of polycrystalline NWs, fabricated by physical deposition. This is due to their almost single crystalline nature. Studies on the fabrication and characterization of single crystal silver, gold and copper nanolines with diameters of the order of 10 nm have been reported recently [WAN 08, KHA 11]. These nanoliness show a resistivity only two times higher than that of the corresponding bulk metal. They are also free of energy dissipation and void diffusion and have high failure current densities. Hence, in the domain of interconnects they are quite attractive.

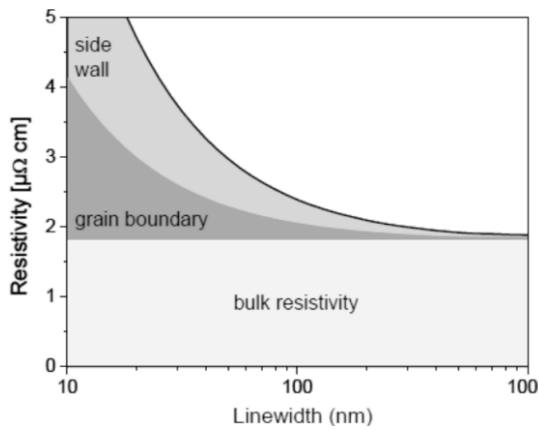

Figure 14.3. *Cu resistivity as a function of line width, taking into account the grain-boundary and interface electron scattering [ITR 07]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Different transport mechanisms are discussed in the literature to estimate the conductance, capacitance and inductance of metal nanolines [SAL 05]. It is shown

that the quantum capacitance (Q_c) and kinetic inductance (L_k) play an equally critical role in metal nanolines, as in CNTs, if their cross-section is reduced to the same size as that of CNTs. Q_c and L_k are in fact intrinsic to any conductor. They become important at the nanoscale because of the limited number of current-carrying modes.

14.2.1.3. *High-frequency characterization*

An established approach to study integrated RF passive components, such as transmission lines, inductors and antennas, is to measure the scattering parameters (S-parameters). Most of the high-frequency metallic nanowire measurements in the literature deal with CNTs and use mainly two-port S-parameter measurements. The RF test structure is either an RF microstrip line or a coplanar waveguide [GOM 07, JUN 07, KIM 10]. Appropriate procedures are applied to de-embed the contribution of the measurement platform and the RF pads and move the reference plane just before the test device [WAL 11]. Such a measurement setup makes the extraction of transmission characteristics of nanometer-scale devices possible. However, given the small dimensions of nanolines, it is difficult to obtain a reliable measurement. New issues emerge, such as the impedance matching, reliability of the contacts and the small signal level from the nanolines. All the above have a strong influence on the interpretation of the results.

14.2.1.4. *Contact and interface effect*

Among the most important problems in the RF measurements of nanolines and other nanoscale RF passive devices are the contact and interface effects. Metal nanolines and nanotubes are usually contacted by RF pads that are fabricated in an extra metallization step. Consequently, there is inevitably a parasitic impedance between the first and the second metal layers, that is called contact impedance, and which may have a significant contribution to the total nanoline impedance.

The interface effect is related to the physical discontinuity between the pad and the nanoline. The typical width of an RF pad, compatible with on-wafer probes, is 100 or 50 μm, which is at least three orders of magnitude higher than the nanoline width. This results in a discontinuity step in signal transmission. Its effect on the overall RF response depends on the characteristics of the line. In general, for a low-loss transmission line, it is important to accurately determine this interface contribution [POS 05], but also use appropriate designs of the RF pads to avoid it. The pads should exhibit minimum loss and maximum signal transmission [MAD 09a]. In addition, the abrupt steps in the connection between the nanolines and the pads should be avoided. A common solution is to use a tapered design, in which the width of the pad decreases gradually when approaching the nanoline [JUN 07, KIM 10].

14.2.1.5. *Removal of the RF pads' effect*

The main challenge with metal nanoline or nanotube characterization is the impedance mismatching [DEM 08]. Nanolines and nanotubes exhibit very high impedance compared to the 50 Ω impedance of all RF test equipment. This leads to high reflectance, reducing the RF energy fed to the test structure. Moreover, due to the high losses, the transmission signal is limited, resulting in a significant inaccuracy in the measurement and in the de-embedding of the pad parasitics.

Today a vast literature exists on the de-embedding methods for transmission line characterization. These methods use either equivalent two-port analysis or lumped-component approximations. Some of them have proved to be more accurate than others at frequencies up to the mm-wave frequencies [MAN 06, TRE 04, ITO 08], and they are in general adopted by the RF community. However, it is an open question whether they are reliable for de-embedding nanometer-scale devices up to frequencies of few hundred gigahertz.

Early works from a number of groups employed the "open" de-embedding method to remove pad parasitics [GU 11, RIC 07]. The open de-embedding method can be expressed in a simple algebraic form:

$$Y_{dut} = Y_{mea} - Y_{open}$$

where Y_{dut} denotes the intrinsic admittance parameters (Y-parameters) of the device under test (DUT), which is the nanoline in the present case. Y_{mea} denotes the measured admittance of the whole device (including the platform and the nanoline). Y_{open} is the admittance of the open device. The admittance parameters can be extracted from S-parameters. The concept of the method is based on a circuit model where the parasitics can be described by a parallel admittance Y_{open}, which represents the capacitive coupling between the input and the output pad, determined by the measured admittance of the "open" device.

Other de-embedding methods can also be applied, including the two-line method [MAN 06] based on the measurement of the signal from two lines which differ only in their length. Using simple mathematical formulas, one can extract the properties of an isolated transmission line with a length equal to the difference of the lengths of the two lines. This method can be very helpful for the de-embedding of the interface effect, as well as of the contact impedance effect, when this is identical in each contact point.

Another technique to extract the intrinsic response of a nanoline is to build a circuit model that describes the S-parameters of the "open" device. Adding new elements step by step to the above circuit, the measured S-parameters of the

nanoline can be fitted [MAD 09b]. The advantage of this approach is a better understanding of the designed RF pads, avoiding the errors that might be introduced by the de-embedding methods. The drawback of this method is the number of unknown circuit elements involved in the fitting process, as demonstrated in Figure 14.4 [JUN 07]. To reduce the amount of unknown lumped elements, Kim *et al*. [KIM 10] applied a full-wave model based on Agilent's ADS Momentum to simulate the "open" device. The capacitance due to the coupling effect can be extracted by fitting to the S-parameters of the "open" device. Note that there are many variations of circuit models that describe a metal nanoline in contact with the RF pads, and each one can lead to a different interpretation of the characteristics of the line. Clearly, more tests on different samples are needed for full assessment of the model.

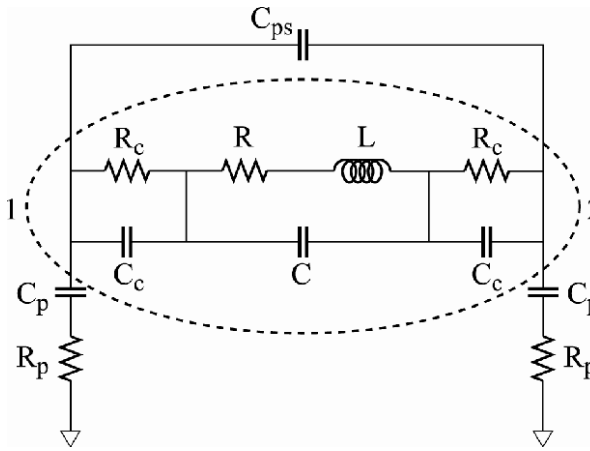

Figure 14.4. *Equivalent-circuit model for a sample with a CNT. The dotted circle represents the CNT part. C_p and R_p denote the capacitance and resistance of the RF pads, C_{ps} denotes the parasitic capacitance of the gap, R_c and C_c denote the contact resistance and capacitance between the CNT and the pads, and R, L,C are the resistance, inductance and capacitance of the CNT [JUN 07]*

14.2.1.6. *Circuit modeling for a wave transmission nanoline*

Once the effect of RF pads is removed from the signal, it is then possible to estimate the electrical properties of the nanoline. What remains includes segments of the contact impedance, and capacitance due to coupling between the pads and the nanoline. As the literature on the RF performance of metal nanolines is limited, we present CNTs' modeling, as an example of nanowire RF modeling.

The contact impedance of a CNT is often simulated by many authors by a parallel RC model [JUN 07, PLO 07, NOU 10], in which the circuit elements for the

CNT itself are the kinetic inductance along with an intrinsic resistance. The quantum capacitance is sufficiently small so as not expected to be measurable [RUT 08]. Based on an individual single-wall CNT measurement, Plombon *et al*. [PLO 07] have demonstrated that the resistance of a single CNT ranges between 10 and 30 KΩ/μm and the kinetic inductance is in the range of 8–43 nH/μm. Because of the much larger impedance than 50 Ω, it is difficult to obtain an accurate imaginary impedance extraction. For this reason, measurements of parallel arrays of CNTs are performed, which yield more stable and consistent results. The impedance of a single CNT can then be estimated from scaling the total impedance by the number of CNTs.

High-frequency characterization of metal nanolines remains quite unexplored. From the results presented in [KIM 11], the contact resistance and the conductivity of a single 300-nm-diameter platinum nanowire are extracted for frequencies up to 50 GHz. Quantum effects are neglected and the contact is assumed to be purely metal to metal. These measurements leave open the possibility of extracting physical transmission properties of the nanolines. The major issues are primarily the accuracy of the calibration and the measurement noise at high frequencies.

14.2.1.7. *Simulations of nano-transmission lines*

Commercial simulation software was used to predict the theoretical response of the nanolines, namely the Agilent's Advanced Design System (ADS) for circuit simulation and the Agilent's Momentum and Ansys's High Frequency Structural Simulator (HFSS) for device simulation.

14.2.2. *Transmission nanolines in microstrip configuration: characterization and modeling*

A simple RF structure to embed a metal nanoline is the microstrip line configuration. During the Nanofunction project, we investigated Al nanolines in microstrip configuration [HSU 12]. Two-line lengths were used in this study in order to facilitate different de-embedding schemes. The first one consisted of measuring Open, Short and Thru devices, realized on the same wafer with the nanolines. The second was the two-line method [MAN 06] to remove pad, contact and interface parasitics. Tapered signal pads were designed to minimize the parasitic effects, although they were not optimized for 50 Ω. The accurate thickness of the different layers of the thin film microstrip line (TFML) was measured by SEM and the results are presented in Figure 14.5, along with the cross-sectional view of the structure. The measured line width was 1.28 μm. A top-view optical microscopy image is shown in Figure 14.6.

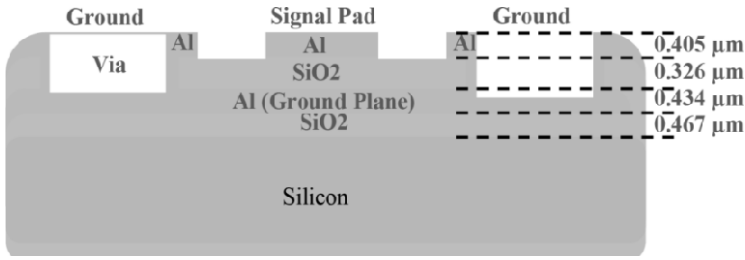

Figure 14.5. *Cross-sectional view of the TFML [HSU 12]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

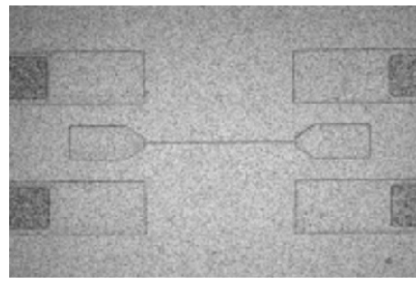

Figure 14.6. *Optical image of the fabricated 200 μm-long TFML and the GSG pads [HSU 12]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

A model proposed by F. Schnieder and W. Heinrich was used to describe the TFML [HAN 11]. According to this model, the TFML is described by an equivalent-circuit model (R, L, C, G), assuming quasi-TEM mode propagation. The individual circuit elements R, L, C and G per unit length are determined by using closed-form formulas, with input parameters derived from the dimensions and the material properties of the nanoline. There are two reasons for choosing this model: first for design purposes, since the close-form formulas used provide an understanding of the impact of the physical parameters to the electrical properties of the nanoline and second because the model is valid for a broad frequency range, from DC up to the beginning of the skin-effect region. To verify the model, the calculation result was compared with the measured one. The nanoline circuit elements R, L, C and G were extracted using the method described in [WAL 11]. Also, results from Agilent's Momentum were included in Figures 14.7 and 14.8 for comparison. In these figures, the inductance L and the capacitance C per unit length are presented for frequencies up to 60 GHz. The results clearly show that there is good agreement between measurements and simulations in the case of the inductance. However, a large mismatch is observed in the capacitance.

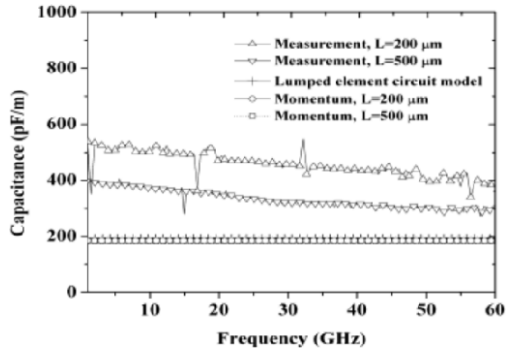

Figure 14.7. *Measured and simulated capacitance per unit length as a function of frequency for TFMLs with a length shown in the figure [HSU 12]*

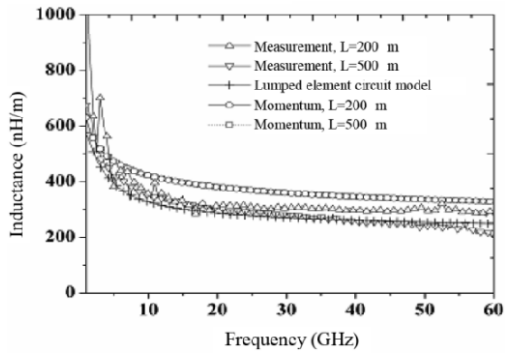

Figure 14.8. *Measured and simulated inductance per unit length as a function of frequency for TFMLs with a length shown in the figure [HSU 12]*

The deviation in circuit elements between the simulated and experimental data is also reflected in the transmission line parameters, namely the complex characteristic impedance (Zc) and the propagation constant (γ).

Since the capacitance is clearly underestimated, one reasonable explanation could be the influence of the step discontinuity between the pad and the line in the model. Although the de-embedding procedure applied has been proved to provide accurate results up to 40 GHz for a microstrip line, at higher frequencies the open end of the pad leads to scattered electrical field. This results in an increase in the effective length of the line. Trying to solve the problem, the step discontinuity was taken into account in the model. This effect was described by a circuit structure with two equivalent series inductances and one parallel capacitance [WAL 11,

HAN 11], with the assumption that the inductance closer to the pad side was removed during the de-embedding. A final circuit model was thus constructed and is shown in Figure 14.9, assuming that the above discontinuity effect exists at both sides of the line. The proposed electrical equivalent circuit was simulated using Agilent's ADS software. Assuming that the discontinuity model accurately describes the physical situation, the sets of values of *Ld* and *Cd* that fit the S-parameters between measurement data and the full-circuit model throughout the whole frequency range were obtained.

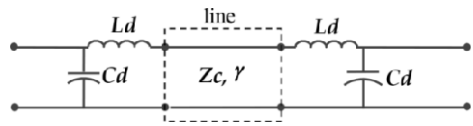

Figure 14.9. *Full-circuit model including the step discontinuity*

By using the method described above, the real and imaginary parts of the characteristic impedance *Zc* along with the attenuation (α) and the phase constant (β) were obtained as a function of frequency. A comparison between the measured data and those obtained from the simulations is shown in Figures 14.10 and 14.11. In the case of the lumped element circuit model for the 200 μm-long line, a capacitance *Cd* = 14 fF and an inductance *Ld* ≈ 0 were obtained. The model demonstrates a reasonable fitting to the measured data. A significant correction in *Zc* was obtained with the addition of *Cd* across the whole frequency range. The attenuation constant α, therefore, starts to show a similar trend and approaches the experimental value. This means that the discontinuity model can adequately describe the behavior of the step change and take into account the impedance mismatch between the line and the pad.

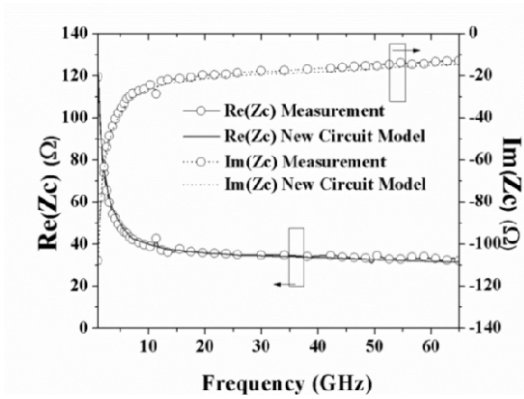

Figure 14.10. *Real (left) and imaginary (right) parts of Zc for the measured and simulated 500 μm-long TFML*

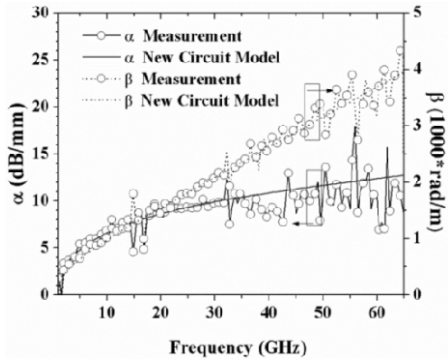

Figure 14.11. *Parameters α (left) and β (right) for the measured and simulated 500 µm-long TFML*

The above results obtained with TFMLs demonstrate that the contact between thin lines and pads has an influence on the RF behavior of a nanoline and must be analyzed and taken into account when designing such a line.

14.2.3. *Transmission nanolines in CPW configuration: fabrication, characterization and modeling*

In the CPW (ground-signal-ground) configuration, both the transmission line and the ground metal layers are on the same layer. The transmission line can be either a single nanoline or an assembly of parallel nanolines. Three types of nanolines are analyzed below, namely single Al nanolines on oxidized low-resistivity Si, single and multiple Au nanolines on oxidized low-resistivity Si and single and multiple Cu nanolines on a thick porous silicon layer, locally grown on the Si wafer.

14.2.3.1. *Aluminum single lines on low-resistivity Si*

In the following, the RF properties of Al nanolines in CPW configuration [HSU 13] are analyzed. The substrate used was a low-resistivity (5–10 Ω.cm) Si substrate, on which a 500 nm thick SiO_2 layer was deposited by low-pressure chemical vapor deposition. Five different nanoline lengths were used (L = 17, 42, 92, 192 and 492 µm). The other dimensions of the realized lines are given in Table 14.1.

Sample	Line width (nm)	Thickness (nm)	Gap (µm)
Al1	8,000	500	20
Al2	100	100	20
Al3	500	100	20

Table 14.1. *Geometric parameters of the studied Al lines in CPW configuration [HSU 13]*

As described in section 14.2.2, two de-embedding methods were investigated to remove parasitics from the measured results. The first method was based on an assumption that the measurement is a combination of the transmission characteristics of the pads, the pad–nanoline contact and the nanoline itself (Figure 14.12). To perform this de-embedding, it is necessary to evaluate the contact impedance, which is only possible for very low frequencies (<10 MHz). The second method was the well-known two-line method described above. This method was supplemented by a preliminary de-embedding of the two lines by using a "Thru" method to remove pad parasitics. The second method was less sensitive to the contact impedance between the line and pads. However, the two-line method assumes identical contact impedances and it cannot provide data for the contact.

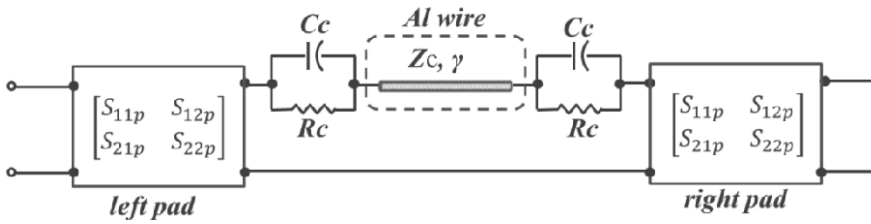

Figure 14.12. *Equivalent electrical circuit describing the model used for the de-embedding procedure, based on the low-frequency measurement of contact impedance*

Using all measurement results from the different lines (Al1, Al2, Al3), the main parameters were extracted using the first de-embedding method, as it helps in the direct study of the contact impedance. The extracted parameters are the characteristic impedance, the attenuation (α) and the phase constant (β). Figures 14.13 to 14.15 represent these parameters for the 192 μm long line.

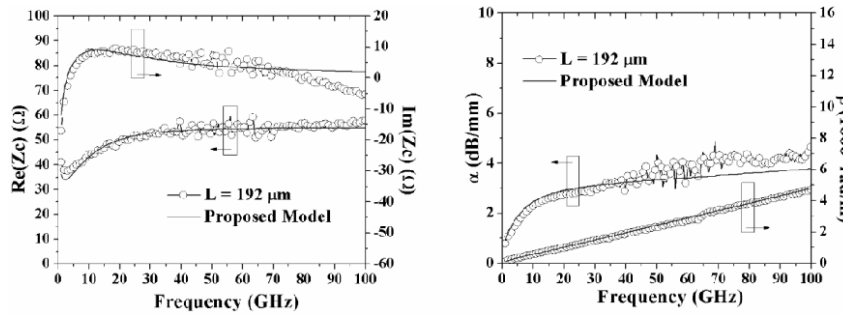

Figure 14.13. *Characteristics of the Al1 line with an Al line width of 8 μm. The real and imaginary parts of the characteristic impedance Zc and the parameters α and β as a function of frequency up to 100 GHz are shown*

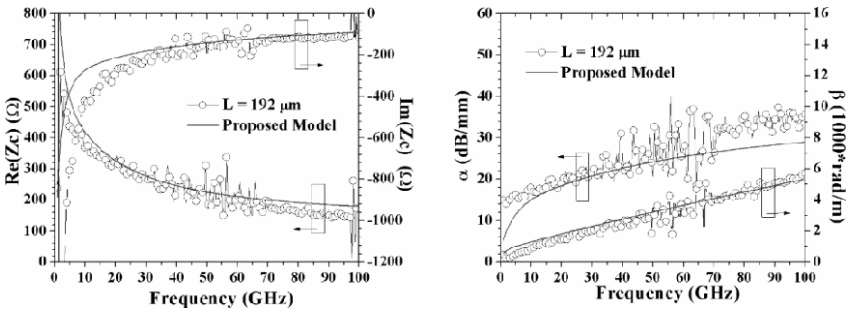

Figure 14.14. *Characteristics of the Al2 line with an Al line width of 100 nm. The real and imaginary parts of the characteristic impedance Zc and the parameters α and β as a function of frequency up to 100 GHz are shown*

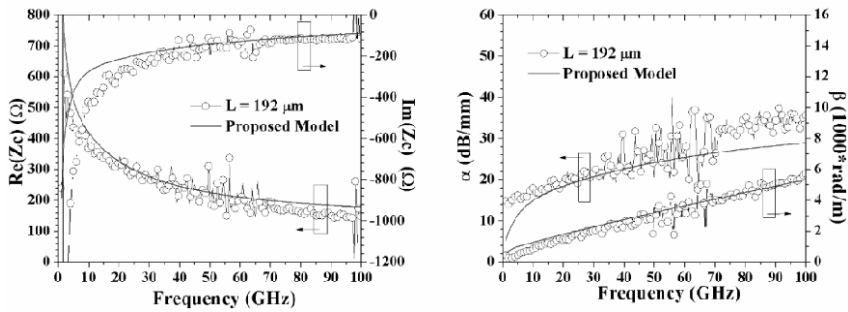

Figure 14.15. *Characteristics of the Al3 line with an Al line width of 500 nm. The real and imaginary parts of the characteristic impedance Zc and the parameters α and β as a function of frequency up to 100 GHz are shown*

For the widest line of Table 14.1 (Al1), the extracted characteristics are close to those of large lines, as expected. This line is not at nanometric dimensions, and it was designed to be used as a reference line. The second and third lines (Al1 and Al3) exhibit an increased characteristic impedance (*Zc*) compared to the wide line. The characteristic impedance increases with the decrease in the line cross-section. Similarly, the attenuation of the three lines, expressed by the parameter α, increases when the cross-section of the line decreases. The above is known and it was expected. On the other hand, by analyzing the phase constant β, we see that it increases with the reduction of the line cross-section. As β is inversely proportional to the phase velocity, the above result describes a slow-wave effect, which depends on the cross-section of the nanoline. Between Al1 and Al3, there is a reduction in phase velocity by a factor of 1.8. This slow-wave effect was also obtained for CNTs [NAE 05]. This effect can be interesting for different applications, for example in

phase shifters. However, the main problem with the nanolines is the considerable attenuation, which is more than ten times larger than in micrometer scale lines. Multiple nanolines in parallel can be envisaged to overcome this problem.

14.2.3.2. *Au single and multiple lines on low-resistivity Si*

Au is not compatible with CMOS processing. However, as mentioned above, it was used as a model nanoline material because it does not oxidize in air. Thus, the influence of contact impedance and of changes in the nanoline cross-section due to oxidation are avoided. The Au nanolines were also integrated on oxidized low-resistivity Si as Al nanolines. In order to avoid an impedance mismatch, observed in single Al nanolines, in these experiments multiple nanolines were used. The RF pads' pitch was reduced to 50 μm, which leads to a reduced pad area and improves the measurement accuracy. The effects of the distance between the two grounds and between nanolines (interline distance) in multiple line configurations were also studied. The dimensions of the realized structures are given in Table 14.2. Figure 14.16 shows an SEM image of two parallel Au nanolines between the corresponding pads in CPW configuration.

Sample	Line width (nm)	Thickness (nm)	Number of lines	Interline distance (nm)	Gap (μm)
B1	200	100	1		20
B1'	200	100	1		12
B2a	200	100	2	200	20
B2b	200	100	2	1,000	20
B5a	200	100	5	200	20
B5b	200	100	5	1,000	20

Table 14.2. *Different dimensions of the gold CPW lines*

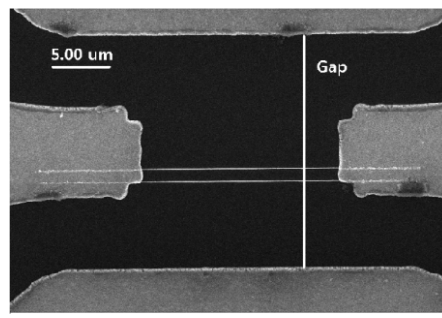

Figure 14.16. *SEM image of two parallel Au nanolines in CPW configuration*

The selected dimensions of nanolines allow us to investigate the influence of the main RF parameters. In Figures 14.17–14.20, the extracted parameters for lines B1, B2a and B5a are depicted. From these characteristics, we see that the characteristic impedance *Zc* of the nanolines decreases with increasing the number of parallel lines, as expected. The same trend is observed for the attenuation α. At 110 GHz, the attenuation for B1 is 49 dB/mm and for B5a is 20 dB/mm. The phase constant β for B1 is 7,000 rad/s and 5,200 for B5a. This corresponds to an increase of 20% in the phase velocity for B5a compared to B1; however, this value is still lower than that of large micrometer-width lines. By comparing the different lines, we see that the slow-wave effect is obtained in all cases. Both the attenuation and the slow-wave effect are adjustable by changing the cross-section of the nanoline and the number of parallel nanolines.

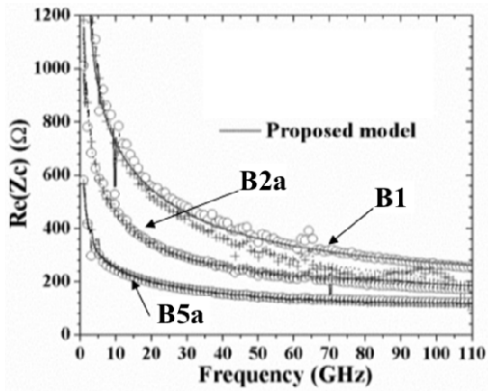

Figure 14.17. *Measured and simulated Re(Zc) of samples B1, B2a and B5a*

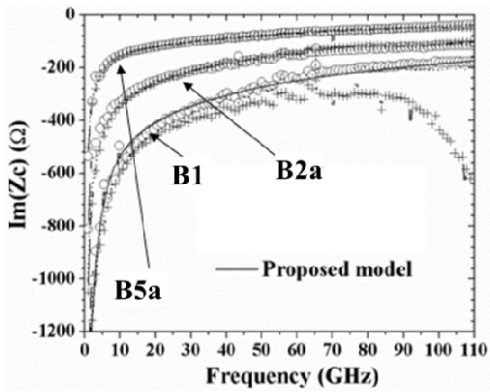

Figure 14.18. *Measured and simulated Im(Zc) of samples B1, B2a and B5a*

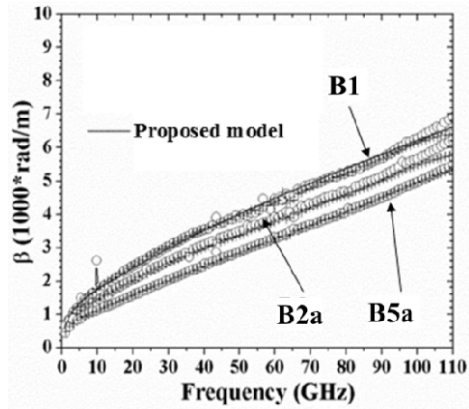

Figure 14.19. *Measured and simulated α of samples B1, B2a and B5a*

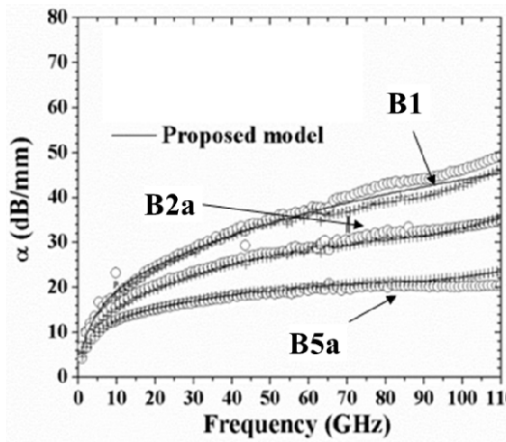

Figure 14.20. *Measured and simulated β of samples B1, B2a and B5a*

The interline effect can be observed on the extracted parameters of Figures 14.21 to 14.24, where the characteristics of samples B2a, B2b, B5a and B5b are analyzed. Their only difference is in the interline distance; for "a" lines it is 200 nm and for "b" lines it is 1,000 nm. As it can be seen in the aforementioned figures, the characteristic impedance is only slightly affected by the interline distance. The phase constant also exhibits very small variations, attributed to the measurement accuracy. By close examination of the characteristics, we see that Re(*Zc*) and Im(*Zc*) slightly decrease across the frequency range when the interline distance increases. At 30 GHz, the difference is approximately 12% and it becomes smaller and smaller at

higher frequencies. Considering the resistance-inductance-capacitance-conductance (RLCG) model parameters of the nanolines, the observed increase in α with the increase in the interline distance can be attributed to the increase in the dielectric loss (G), which is associated with the comparatively higher effective capacitance. The effective inductance has dropped substantially, but this has little effect on Zc and β, since R is dominant ($R > \omega L$) even at high frequencies. In fact, at low frequencies, Zc can be approximated by $\sqrt{R/G}$. At higher frequencies, the expression for Zc becomes $\sqrt{R/(G + i\omega C)}$. This explains the variation in Zc with the interline distance.

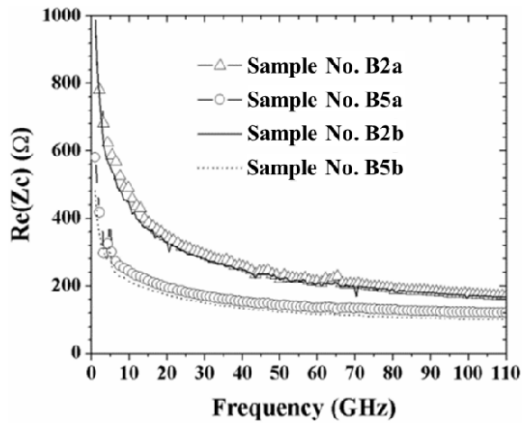

Figure 14.21. *Measured Re(Zc) of samples B2a, B2b, B2a and B5b*

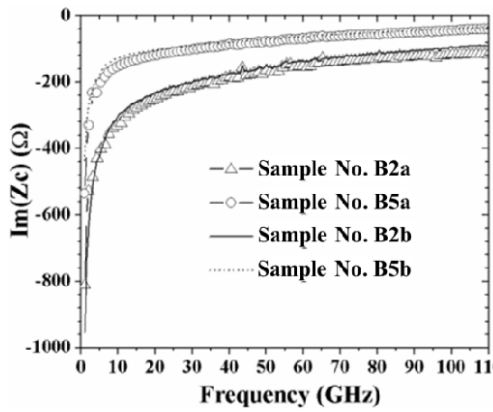

Figure 14.22. *Measured Im(Zc) of samples B2a, B2b, B2a and B5b*

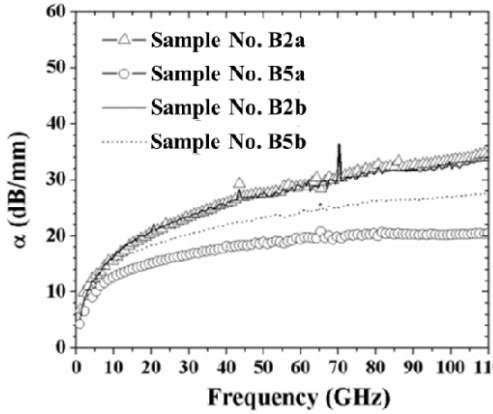

Figure 14.23. *Measured α of samples B2a, B2b, B2a and B5b*

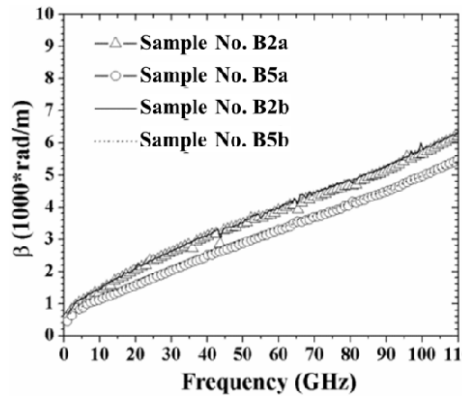

Figure 14.24. *Measured β of samples B2a, B2b, B2a and B5b*

The effect of the gap between ground pads is small and it mainly affects the characteristic impedance. On reducing the gap, the characteristic impedance decreases, as in large CPW lines.

14.2.3.3. *Copper single and multiple lines on porous silicon*

Today, copper is the most widely used metal in microelectronics as it is very conductive. In addition, thick porous Si layers were demonstrated to provide effective RF shielding from the Si substrate (see Chapter 13). In the following, the obtained results of the investigated RF properties of Cu nanolines on porous Si are presented. The porous Si substrate used had a porosity of 76%, and a thickness of

150 μm. Single and multiple Cu nanolines in CPW configuration were fabricated on porous silicon as described at the beginning of the chapter. The two-step metallization process was used, in which the nanoline is first deposited and patterned using electron beam lithography and lift-off, while the metal pads (250 nm thick evaporated Al) are subsequently added and patterned by optical lithography. SEM images of the nanolines in CPW configuration, with a zoom on the area between nanolines and pads, can be seen in Figure 14.25. The dimensions of the fabricated lines are given in Table 14.3.

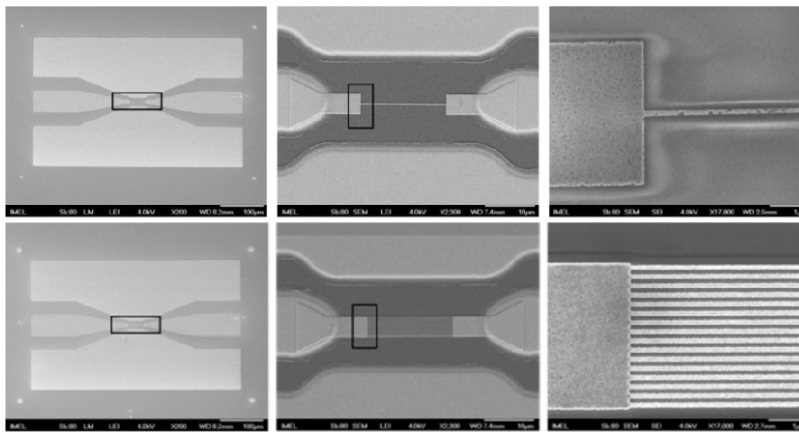

Figure 14.25. *SEM images of copper nanolines on porous Si substrate, fabricated with a two-step metallization process. The nanoline width is 100 nm [SAR 12]*

Sample	Line width (nm)	Thickness (nm)	Number of lines	Interline distance (nm)	Gap (μm)
PS1	200	100	1		20
PS2	200	100	4	700	20
PS3	200	100	5	650	20
PS4	200	100	8	1,000	20
PS5	200	100	10	900	20

Table 14.3. *Dimensions of the nanolines on porous silicon*

The extracted results from S-parameters measurements are represented in Figure 14.26. The measurements were performed up to 40 GHz and the two-line de-embedding method was followed, which was found to be an adequate one.

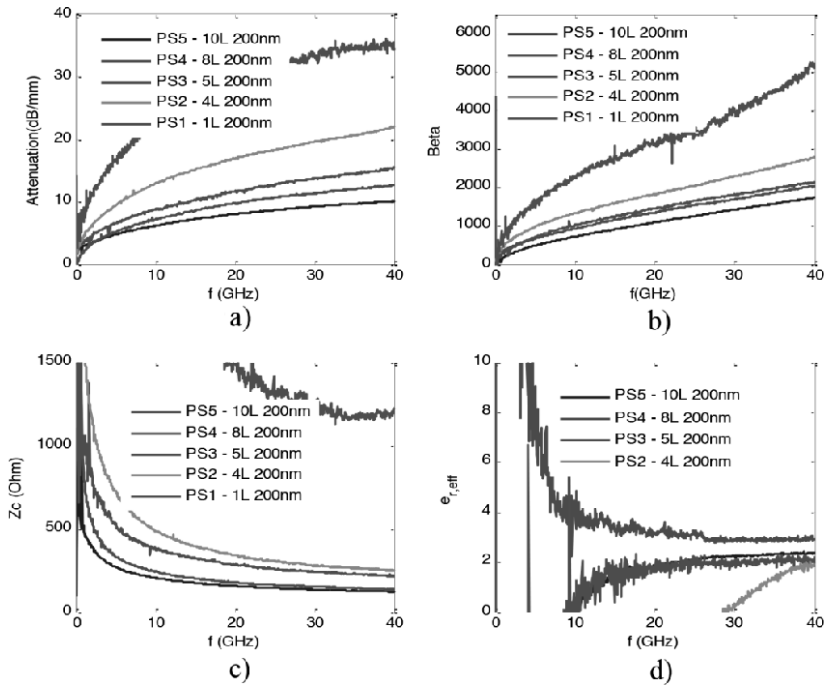

Figure 14.26. *Comparison of effective attenuation a), phase constant b), characteristic impedance c) and permittivity d) between 1, 4, 5, 8 and 10 lines of 200 nm width [SAR 12]. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The trend is the same as in the case of Au nanolines. The attenuation of the multiple lines (PS5) is more than 25 dB lower than that of a single line. The variation in the phase constant between different multiple nanolines is small but observable. Compared to the case of the single lines, the phase constant β of the multiple lines is lower (by ~70% at 40 GHz) for sample PS5 compared to PS1. However, the slow-wave effect remains. The attenuation of the nanolines on porous Si is lower than that of the Au lines on silicon oxide. This result was expected as the losses on porous Si are greatly reduced. Further experiments were conducted with Cu nanolines of several widths (100–1000 nm). The attenuation and the phase constant (at 40 GHz) as a function of the number of lines are presented in Figure 14.27.

A clear trend can be observed in Figure 14.27. As the number of nanolines increases, the attenuation and the phase constant decrease. Also, narrower nanolines lead to increased attenuation and phase constant. The changes seem to be exponential with the number of lines. These observations are quite crucial for

choosing the right combination of line width and number of lines in the design of CPWs with nanolines used as signal lines.

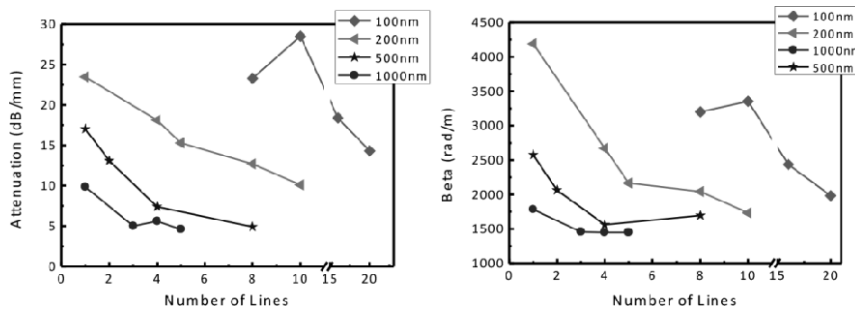

Figure 14.27. *Experimental values of the attenuation and the phase constant as a function of the number of lines. The values correspond to 40 GHz [SAR 12]*

14.2.4. *Characterization up to 200 GHz*

As deduced from the above experiments, the slow-wave effect is the main effect observed in all nanolines. To verify that this effect is not due to a shape factor, some nanolines were characterized up to 200 GHz. Figure 14.28 shows the attenuation and the phase constant of an aluminum line as a function of frequency in the frequency range 140–200 GHz, compared to the corresponding characteristics in the 0–100 GHz range. These two parameters show that the behavior of the line is the same for the whole frequency range.

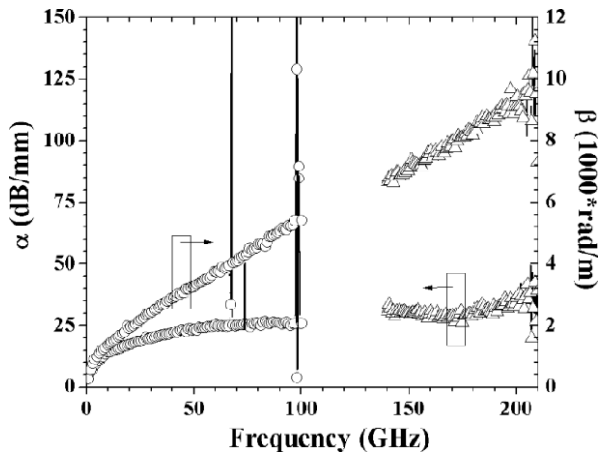

Figure 14.28. *Attenuation and phase constant of an Al line, sample 2, up to 200 GHz*

14.3. Antennas

To our knowledge, there are no results in the literature on metal nanoscale on-chip antennas for millimeter waves, since such antennas are considered intuitively as bad antennas. However, as the CMOS device dimensions continue to scale down, operating speeds and cut-off frequencies of CMOS devices tend to exceed 100 GHz. The frequency increase results in reduced antenna dimensions and is expected to facilitate the on-chip integration of the antennas. There are many possible applications in intra-chip or chip-to-chip communications, extensively described in [RUS 10a, RUS 10b].

In the EU project "Nanofunction", small integrated antennas were fabricated on different substrates and tested. The effect of antenna metal line width and the substrate material on wireless signal transmission were examined. Dipoles and planar inverted-F antennas (PIFAs) were investigated in the frequency range 1–110 GHz and 140–210 GHz.

14.3.1. *On-chip antennas: general*

14.3.1.1. *Antenna substrate materials*

The antenna characteristics are strongly dependent on the substrate. To evaluate the influence of the substrate on antenna characteristics and power transmission (from emitter to receiver), three kinds of substrates were used, namely low-resistivity (10 Ω.cm) bulk Si, high-resistivity Si (1 KΩ.cm) and porous Si locally formed on a low-resistivity Si wafer [ZAC 09, ISS 11]. The thickness of the porous Si layer was 150 μm and its measured relative permittivity was 3.5 [SAR 13a]. A 500 nm thick TEOS SiO_2 layer was deposited on top of the porous Si layer.

14.3.1.2. *Antenna design*

A common antenna design is that of the planar dipole antenna. Figure 14.29 shows the geometry of the designed on-chip antenna in the form of a planar dipole fed by a slot line. The different characteristic dimensions of the dipole antenna are also shown in the same figure. The total dipole length ($L = 2 \cdot Ld + Ls$) is about half its operating wavelength. The gap (Ls) between dipoles, the length (Lt) and the width (Wt) of the feed line have a strong influence on the impedance of the antenna [RUS 10b, RUS 10c]. On the other hand, the above parameters should have a negligible effect on the antenna resonant frequency. In the tested samples, two identical antennas were arranged opposite to one another, as represented in Figure 14.29. Therefore, all the characteristics that are analyzed below correspond to $\varphi = 90^o$ and $\theta = 0^o$.

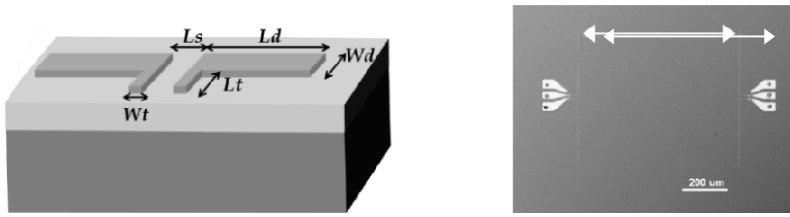

Figure 14.29. *Schematic representation of the dipole antennas structure design in 3D (left) and plane view (right). For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Several antennas with different dimensions were realized. The dimensions were chosen in acordance with the silicon substrate properties. In Table 14.4, the different dimensions of the realized dipole antennas are given.

Sample name	*Ld* (μm)	*Wd* (μm)	*Lt* (μm)	*Wt* (μm)	Thickness (nm)	*Ls* (μm)	*D* (μm)	Substrate
1A	1,000	4	20	5	250	50	1,000	PSi/low-ρ Si
1B	1,000	3	250	50	250	50	1,000	PSi/low-ρ Si
1C	500	2	80	50	250	50	1,000	PSi/low-ρ Si
1D	400	2	93	5	250	50	7,000	PSi/low-ρ Si
2A1	400	2	40	2	100	14	700	HR-Si
2A2	300	2	40	2	100	14	700	HR-Si
2B	300	2	90	2	100	14	700	HR-Si
2C	300/100	2	40	2	100	14	700	HR-Si

Table 14.4. *Different dimensions of the investigated dipole antennas*

Another popular on-chip antenna design is the PIFA, currently widely used in mobile phone antenna technology. The physical length of the PIFA is about one-quarter the operating wavelength, which is half the length of the dipole antenna. The layout of the designed PIFA is presented in Figure 14.30. Basically, the PIFA consists of a single line, connected to a short-circuiting line. The feed line is also illustrated in Figure 14.30. Similar designs were used by other authors in the literature [GUO 08]. Such configuration is compatible with GSG probes, while at the same time it minimizes the radiation loss and the coupling between the ground pads. It is noted that the distance *Ldg* between the feed line and the shorted line and

the line length (*Lt*) both have an important role on impedance matching. Finally, for the transmission characterization, the distance (*D*) between the two PIFAs, used as transmitter and receiver, is also important.

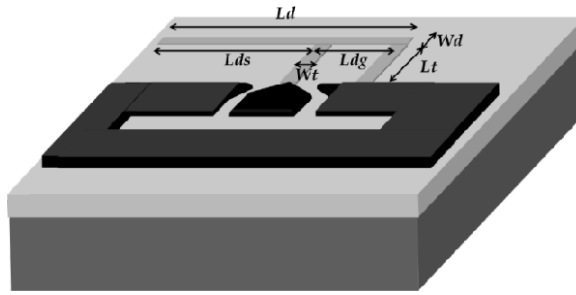

Figure 14.30. *Layout of the designed inverted-F antenna*

The dimensions of the designed PIFAs are given in Table 14.5.

Sample name	*Ld* (µm)	*Lds* (µm)	*Ldg* (µm)	*Wd* (µm)	*Lt* (µm)	*Wt* (µm)	Thickness (µm)	*D* (µm)
4B1	500	300	200	2	100	2	0.1	700
4B2	400	200	200	2	100	2	0.1	700
4B3	300	100	200	2	100	2	0.1	700

Table 14.5. *Different dimensions in µm of PIF antennas*

14.3.2. *On-chip antenna characterization method*

An on-chip communication system with a multilayer structure is known to have different channels of wave propagation, including the free-space waves, which propagate in air, and the surface waves, which propagate in-between the layers and are also bounded by the air-wafer surfaces [OKK 05]. As the operating frequency increases, the propagation by surface waves is expected to be preponderant and channels through the surface and the intermediate layers are expected to be the most critical. The propagation of these surface waves is also enhanced by using a thick shielding substrate.

The excitation of surface waves can be either advantageous or negative, depending whether it can contribute to the main beam radiation. In some

applications, such as in chip-to-chip communications or free-space applications (WLAN, WPAN, mobile phone networks, etc.), surface wave power is treated as wave propagation loss. On the other hand, in applications such as intra-chip communications, the surface waves are a useful channel of signal transmission, greatly influenced by the substrate. Through optimization of the dielectric properties and the thickness of the substrate, propagation by surface waves can be optimized. However, special attention needs to be paid in order to avoid destructive interferences between the multiple wave components [OKK 05]. As the frequency increases, different modes of surface waves can be excited, namely different orders of transverse electric and transverse magnetic modes. The cut-off frequencies of these modes depend on the thickness and the dielectric constant of the substrate and can be roughly evaluated using the following equations [TRI 08]:

$$f_c = \frac{nc}{2d\sqrt{\varepsilon_r - 1}} \qquad \text{n=0,1,2,... for } \mathrm{TM}_n \text{ modes}$$

$$f_c = \frac{(2n-1)c}{4d\sqrt{\varepsilon_r - 1}} \qquad \text{n=1,2,... for } \mathrm{TE}_n \text{ modes}$$

In the characterization setup, one antenna is used as a transmitting antenna and the other one as a receiving antenna. Typically, the figure of merit used to evaluate intra-chip antenna transmission characteristics is the antenna transmission gain G_a. It is calculated from two-port S-parameters as [TRI 08]:

$$G_a = \frac{\left|S_{21}\right|^2}{\left(1-\left|S_{11}\right|^2\right)\left(1-\left|S_{22}\right|^2\right)} = G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2 e^{-2aR}$$

14.3.3. *Measurement results*

14.3.3.1. *Dipole antennas on low-resistivity Si and porous Si substrates*

Figures 14.31 and 14.32 show the measured S-parameters as a function of frequency for similar dipole antennas realized on porous Si and on standard CMOS Si (1–10 Ω.cm). The dimensions of the investigated antennas 1A, 1B, 1C and 1D are presented in Table 14.4. The S-parameters were de-embedded with an "open" de-embedding method. From Figures 14.31 and 14.32, it can be seen that for the same antenna design the resonance frequency (denoted as f_0) is significantly higher on the porous silicon substrate than on the low-resistivity Si substrate. This is mainly attributed to the lower permittivity of porous silicon.

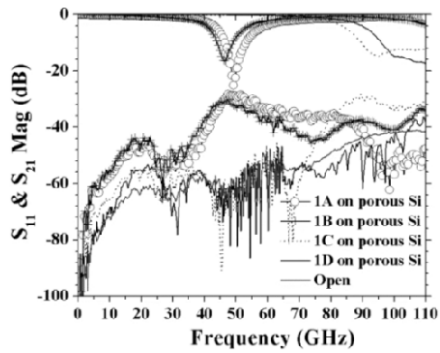

Figure 14.31. *Experimental S-parameters of the dipoles on porous silicon substrate. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

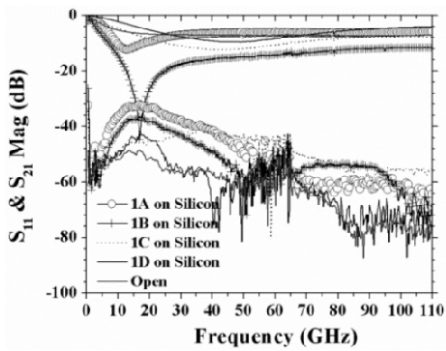

Figure 14.32. *Experimental S-parameters of the dipoles on low-R silicon substrate. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

A simple estimation of f_0 for an integrated dipole can be obtained from [BAL 12]:

$$f_0 = 0.47 \frac{c}{L\sqrt{\varepsilon_{eff}}}$$

where c is the speed of light, L is the total length of the dipole and ε_{eff} is the effective permittivity of the path. We know that the electromagnetic wave generated from the dipole travels both within the substrate and in air. The relationship between the effective permittivity, the antenna geometry and the material dielectric parameters for a single layer-printed radiator can be found in [BAL 12] and is the following:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + 12\frac{h}{w}\right)^{-1/2} + 0.04\left(1 - \frac{w}{h}\right)^2\right]$$

where ε_r is the relative dielectric constant of the substrate, w is the width of the conductor and h is the thickness of the substrate. Using this equation, the effective permittivity in the case of sample 1A on porous Si is ~2.2 and the relative dielectric constant of porous Si is found to be 3.4. This is close to the value of 3.5 extracted by the method described in [SAR 13a]. In the case of sample 1A on the low-resistivity Si substrate, the estimated ε_{eff} is over 30. Compared to the effective permittivity of bulk crystalline Si (which is equal to11.9), the above obtained value has no physical significance and the resonance frequency is largely underestimated. This is due to the eddy currents that circulate inside the low-resistivity Si substrate and which result in a shift of the resonance peak toward lower frequencies. The obtained shift after de-embedding with an open device is about 6 GHz, while in the case of porous Si this shift is reduced to 1 GHz. This suggests that the uncertainty introduced by the de-embedding is more pronounced in the case of a lossy substrate.

The extracted results for the dipole antennas are presented in Table 14.6. Compared to sample 1A, sample 1B has a larger feed line. Thus, it is expected to yield better impedance matching. However, from the calculated input impedance (Z_{in}), we only observe this improvement on the low-resistivity silicon substrate. In addition, f_0 is slightly different in sample 1B compared to sample 1A. It can be also seen that a decrease in the dipole width from 4 to 3 μm has resulted in a drop of 10 dB in the insertion loss on the porous silicon substrate, but a less significant decrease of 3 dB on the low-resistivity silicon substrate.

Sample name	1A-PSi	1A-Si	1B-PSi	1B-Si	1C-PSi	1C-Si	1D-PSi	1D-Si
f_0 (GHz)	49.2	12.8	46.2	16.9	105.9	42.9	>110	46.8
$\lvert S_{11}\rvert$ (dB)	–25.2	–12.3	–16.6	–44.7	–12.6	–12.5		–9.5
$\lvert S_{21}\rvert$ (dB)	–29.1	–33.7	–38.8	–36.4	–33.2	–42.5		–62
BW (>10 dB)	6.6	8.5	4.9	>100	>20.3	40.5		—
Zin (Ω)	55.8	82.0	67.4	50.6	80.6	81.1		100.4
e_{cd} (%)	44.8	66.5	40.8	26.7	61.9	65.5		75.6
R_L (Ω)	30.8	27.5	39.9	37.1	30.7	28.0		24.51
Ga (dBi)	–27.5	–31	–29.5	–36.5	–27.5	–37.5		–61.0

Table 14.6. *Summary of the experimental results derived from the two-port S-parameter measurements of dipole antennas on porous silicon (PSi) and on low-resistivity silicon (Si)*

Concerning the resonance frequency, samples of the 1C series, with dipole length equal to half that of samples 1A, showed, as expected, a resonance frequency two times higher than samples 1A, i.e. f_0 = 49.2 for 1A on PSi and 105.9 for 1C also

on PSi. The antenna 1D on PSi with even shorter length (L = 850 μm), had the highest resonance frequency of all other samples, that was above the measured frequency range of 110 GHz.

Concerning the dipole line width, we found that its scaling down led to an increase in conduction losses. This was somehow compensated by the reduction in the dipole length. If loss resistance (RL) and input impedance (Zin) are reduced, while Zin is increased, an increase in resonance efficiency is obtained.

The estimated radiation resistance of the antennas was about 61.9% of the total impedance for the 1C-PSi series, whereas for the 1B-PSi series it was 40.8%. However, although the 1B-PSi antennas had better reflection efficiency, their overall efficiency was lower than that of the 1C-PSi antennas. It is thus reasonable to say that at the same separation distance D, the transmission gain of 1C-PSi antennas is higher than that of 1B-PSi antennas, despite their occupied area being much lower (wd = 2 μm, L = 1050 μm). We can conclude that size reduction in the dipole antennas is achievable without compromising their gain, if both the geometry of the dipole and the feeding line are optimized.

Finally, as it can be seen in Figure 14.33, the transmission gain (Ga) is increased by few dBi (3 to 7 dBi) with the use of porous Si as a substrate [SAR 13b].

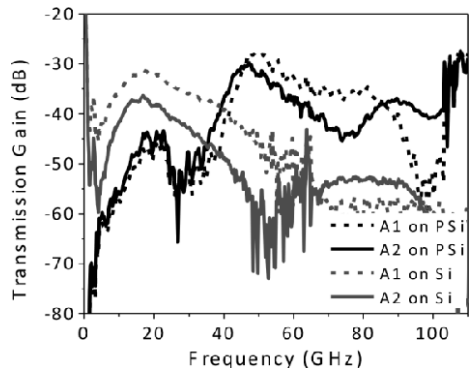

Figure 14.33. *Measured transmission gain (G_a) for A1 antennas (dots) and A2 antennas (solid line). Two different substrates are compared: porous Si (black) and low-resistivity Si (dotted) characteristics. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Figure 14.34 shows the measured and simulated S-parameters for samples 1A and 1D on porous silicon for frequencies up to 210 GHz. Besides the primary resonance peak at 49.2 GHz, another sharp resonance peak is observed at 145 GHz. The performance of the antennas is reasonably good. The return loss and insertion

loss are –14.9 and –30.0 dB, respectively. The resonance frequency of the 1D-PSi antenna is expected to occur in the frequency range 110–140 GHz that is not shown. Both measured and simulated data (using Ansys's HFSS) show similar trends, although there is a discrepancy in the magnitude of the S-parameters and f_0 is a slightly underestimated.

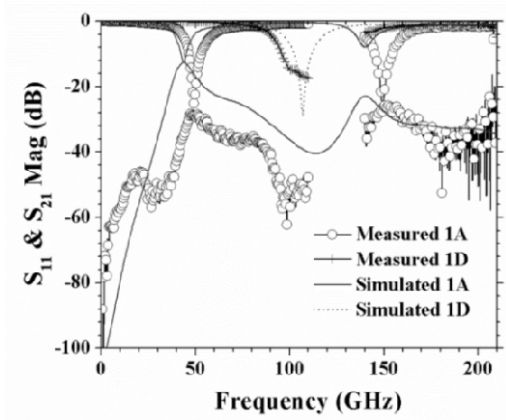

Figure 14.34. *Measured and simulated S-parameters for samples 1A and 1D on porous silicon for frequencies in the ranges (0–110) GHz and (140–210) GHz. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

14.3.3.2. *Dipole antennas on high-resistivity silicon*

Similar ultra narrow dipole antennas, such as those integrated on porous Si, were also integrated on a high-resistivity Si (HR-Si) substrate (2A1, 2A2, 2B and 2C from Table 14.4). Figure 14.35 shows the measured S-parameters of the tested dipoles. It can be seen that the transmission gain increases slowly in the frequency range between 30 and 60 GHz for all the dipoles. This shows that by increasing the frequency, the surface waves begin to dominate the field. The wave mode could be TE1, since its cut-off frequency is at 43 GHz. Above this range, a high S21 window can be seen, which favors signal transmission [KK 05]. Table 14.7 lists the experimental results of the dipoles, calculated from the measured S-parameters. The effective permittivity was estimated as in section 14.3.3.1. For sample 2A2, we obtained εeff equal to 6, which corresponds to a dielectric constant of the HR silicon of ~11. This is not far from the known value of 11.7.

Sample 2A1 has the highest gain among all the tested samples. Radiation loss accounts for 37.9% of the total input impedance. It is obvious that the conduction losses are significant in all samples due to the small antenna metal layer thickness (0.1 μm). By decreasing the dipole length (down to 614 μm for sample 2A2), f0 is

increased and reached the value of 93.7 GHz in sample 2A2. The gain degraded by 13.4 dB inspite of the better impedance matching at the resonance frequency. Only 31.3% of the total impedance takes parts in the radiation. In addition, it appears that the feeding line should be made as short as possible in order to achieve a better matching. Sample 2B has a feeding line twice as long as that of sample 2A2. It can be noticed that the impedance is slightly worse and the resonance frequency has shifted. Sample 2C is an asymmetric dipole, having one arm 300 μm long and the other one 100 μm long. It has a similar performance as sample 2A, if not better. This type of design is in favor of size reduction without sacrificing performance.

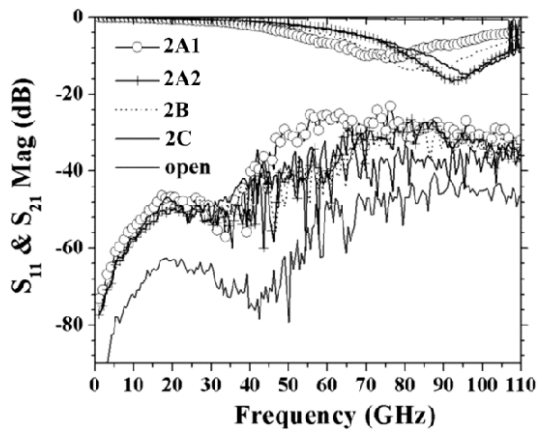

Figure 14.35. *Experimental S-parameters of the dipoles on a high-resistivity silicon substrate. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Sample name	2A1	2A2	2B	2C	3A1	3A2	3B
f_0 (GHz)	77.8	93.7	86.6	96.8	100.5	>110	98.6
$\|S_{11}\|$ (dB)	–10.0	–16.4	–13.8	–14.5	–9.9		–8.8
$\|S_{21}\|$ (dB)	–25.9	–31.9	–33.9	–33.7	–41.3		–40.2
BW (>10 dB)		23.5	22.9	21.5			
*Z*in (Ω)	96.2	67.8	75.7	73.2	97.0		107.0
e_r (%)	90.0	97.7	95.8	96.5	89.8		86.8
R_L (Ω)	59.7	46.6	53.2	46.7	85.8		91.0
e_{cd} (%)	37.9	31.3	29.7	36.2	11.5		15.0
Ga (dBi)	–25.0	–31.7	–33.5	–33.4	–40.3		–39

Table 14.7. *Summary of the experimental results from the two-port S-parameter measurements on high-resistivity silicon*

14.3.3.3. *PIFA antennas on high-resistivity silicon*

Figure 14.36 shows the experimental S-parameters up to 210 GHz of the PIFAs with different dimensions. It is important to emphasize that no de-embedding procedure was applied, since the ground plane was the same as that of the RF pads. It would be better if we could isolate the probing pads from the ground planes; however, no such test structure was available in our experiment. Hence, the analysis refers to the performance of the CPW line, the ground plane and the PIFA itself in a single device. Similarly to the case of the on-chip dipoles, a significant increase in the transmission coefficient S_{21} was observed from 30 to 50 GHz, which corresponds to the excitation of the TE_1 mode. Above 50 GHz, S_{21} remains high up to 210 GHz. As it can be seen from the results, there are significant fluctuations in the S_{21} characteristics, possibly due to the fixed charges in the oxide, which lead to unstable distribution of carriers inside the Si substrate. This effect becomes more pronounced in large areas of the devices, such as the ground plane. Despite this, we can identify the contribution of the antenna by comparing its signal level with that of the open structure. One can see that above 140 GHz, S_{21} of the antennas resemble the S_{21} of the open structure, which means that signal transmission is mainly attributed to pad–pad coupling.

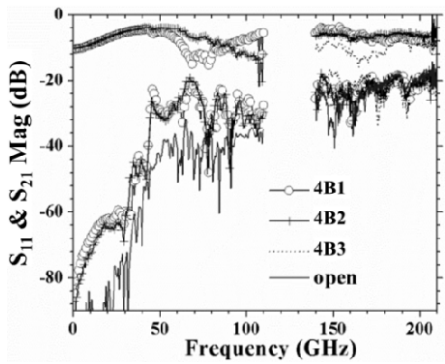

Figure 14.36. *Experimental S-parameters of PIFA antennas on high-resistivity silicon. For a color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

In general, the transmission gain of the PIFAs is relatively good, taking into account their limited size. Table 14.8 lists the results of the tested PIFAs. If we examine sample 4B1, we see that by increasing the distance between feed and shorting lines from 100 to 200 μm, the reflection coefficient has been reduced slightly. However, by doing so, the gain is sacrificed and the resonance frequency is also affected. The dependence of the transmission gain on the different features is difficult. Instabilities of the electromagnetic field, probably built up by the charges, result in a rapid fluctuation of the signal with frequency.

Sample No.	4B1	4B2	4B3
f_0 (GHz)	78.4	110–140	170.4
$\|S_{11}\|$ (dB)	–14.5		–14.8
$\|S_{21}\|$ (dB)	–35.6		–19.6
Bandwidth (>10 dB, GHz)	26.7		25.6
*Z*in (Ω)	73.2		72.2
Ga (dB)	–35		–19.3

Table 14.8. *Extracted characteristics of the PIFA antenna and the transmission link*

14.3.4. *Discussion on antenna results*

Different antenna designs were analyzed, i.e. symmetric dipole antennas, asymmetric dipole antennas and PIFAs. Asymmetric dipoles are proved to reduce the size of the antenna without too much sacrificing its performance. PIFAs are even shorter antennas and their performance remains very good.

Different substrates were also tested. The low-resistivity Si is a substrate with high losses and its limitation is mainly the attenuation of the propagated signal. High-resistivity Si has lower losses and improves the gain of the antennas. Both substrates have the same relative dielectric constant of bulk crystalline Si ($\varepsilon_{r,Si}$ = 11.7), which is high enough to be advantageous for antenna size reduction. However, a high-dielectric constant leads to lower cut-off frequencies of the surface waves and more energy stored inside the substrate, which is a drawback in free-space applications. Compared to bulk crystalline Si, porous Si is a low-dielectric constant material. In our experiments, a value of $\varepsilon_{r,porous\text{-}Si}$ = 3.5 was used, but this value can be engineered to be as low as 2 [SAR 13a]. Moreover, porous Si is a very low-loss material. These two properties constitute a very good combination for the integration of on-chip antennas [CHE 13, SAR 13b]. The only problem is the increase in the antenna dimensions due to the low ε_r; however, this can be solved by optimizing the antenna design.

14.4. Conclusion

From the presented results on the investigation of nanolines and antennas at RF and mm-wave frequencies, the following conclusions can be drawn:

– When measuring a nanoline, care should be taken to correctly choose the adequate de-embedding method, since this is an important source of inaccuracy,

mainly at high frequencies, due to the small signal level from the nanolines, which can be comparable to the parasitic signal.

– In single and multiple CPW nanolines, a slow-wave effect was observed. This effect depends on the line dimensions. Size reduction of nanolines leads to an increase in attenuation, which is less significant in multiple parallel nanolines. Multiples nanolines are more adequate RF for transmission. They show less metal losses and better impedance matching compared to single nanolines. They provide more freedom in design, because their transmission characteristics can be controlled by changing the number of nanolines, the distance between nanolines, and their line width. They, thus, constitute an attractive alternative to conventional CPW lines. It is noticeable that modeling can be performed by using conventional models or software, adjusted with the addition of a capacitive component.

– Antennas based on results obtained for nanolines were also designed and realized. The first goal was to analyze the electrical properties and transmission ability of a pair of antennas on silicon in a frequency range up to 200 GHz. Two main characteristics of the antennas have to be taken into consideration. The first one is the occupied surface and the second the antenna efficiency. Two types of antennas were investigated: dipole and PIFAs. The dipole is a half-wavelength antenna, while PIFA is a quarter-wavelength antenna and occupies less space. The obtained results were in good agreement with simulations and demonstrate that it is possible to transmit energy inside the Si substrate in the mm-wave range using small integrated antennas.

14.5. Acknowledgments

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15

Nanostructured Magnetic Materials for High-Frequency Applications

15.1. Introduction

Miniaturization, with increasing functionality, while maintaining or improving performance, is the key trend in many information and communications technology (ICT) products. These trends are forcing the electronic components that comprise the building blocks of larger systems to operate at higher frequencies, become more integrated and more suitable for automated, batch fabrication. Components using soft-magnetic materials are central to the operation of many ICT products. The functions for which magnetic components are utilized include energy management (e.g. inductors and transformers), radio frequency (RF) communications, electromagnetic interference (EMI) noise reduction and micromechanical components such as switches, read/write heads and sensors. Conventional magnetic component technology, which is mostly dominated by wire wound discrete/sintered cores, is not fully compatible with the current trends toward miniaturization and integration. Recently, magnetic cores integrated onto silicon microchips or printed circuit board (PCB) as a part of microelectronic modules have received increased attention from the scientific/engineering community. The focus of research on such cores can be divided into two major categories: (1) a quest for improved magnetic materials capable of operating at high frequency and (2) a quest for suitable integration techniques.

15.2. Power conversion and integration

Unlike data-processing circuits, power conversion circuitry has not achieved the same level of miniaturization or adherence to Moore's law. This is mostly due to the

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fact that energy processing circuits, such as DC-DC converters, generally require significant energy storage in the form of inductors and capacitors. These energy storage elements generally comprise the largest part of the volume of a converter and can only be reduced in size by increasing the switching frequency of the converter. It is well known that the size of energy storage elements required is inversely proportional to frequency. This is due to higher switching frequencies reducing the duration of time for which energy must be supplied from the passive energy storage elements (e.g. inductors) and hence reducing their required size (inductance in henries). Presently, most power converters have a switching frequency in the sub 1 MHz range (higher switching frequencies of several MHz (<4 MHz) are used for some low power non-isolated converters). Consequently, the passive components required are not within the range that can be effectively integrated onto a chip. It is only by increasing the switching frequency to the tens or hundreds of megahertz range, or higher, that the passive component values become suitable for complete integration as, shown in Figure 15.1, and huge advances in power converter integration and miniaturization can be achieved.

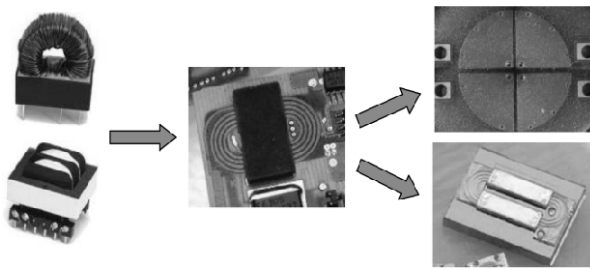

Figure 15.1. *Evolution of magnetic component technology: conventional technology a) wire wound discrete cores and bobbins b) planar magnetics – integrated windings and discrete core: current research c) full PCB integration integrated windings and integrated cores (top); integration onto silicon winding and core fabrication by MEMS technique (bottom)*

There has been a significant trend toward miniaturization in power converters over the last 20–30 years driven mainly by the moves to distributed powering schemes that require many, preferably small, point of load power supplies. This miniaturization has been achieved by increasing the switching frequency from kilohertz in the 1970s to hundreds of kilohertz and low megahertz today [HUL 00]. In recent years, this miniaturization has led to increased integration, in particular in the area of active circuitry integration onto silicon.

In the microprocessor world, continuing scaling of CMOS manufacturing technology according to Moore's law enabled an increase in processor clock frequency almost by three orders of magnitude in a decade. From the introduction of

Pentium by INTEL on 0.8 μm process in 1993 until the Pentium 4 on 90 nm process, the clock frequency increased from 66 MHz to 3.4 GHz with power consumption up from 8 to 103 W. Again, according to the projection of power requirement for future microprocessors, more than 100 A current is to be supplied with voltages less than 1 V. The challenge in this power supply application is that while the microprossor's load current steps from near zero to full load or vice versa within nanoseconds, the voltage must be held throughout the step with a tolerance of a few millivolts. The combination of high current, transient response and tight tolerance levels requires a voltage regulator module to be located adjacent to the load, small in size, operating at high frequency with high efficiency. In a paper from INTEL, a multiphase interleaved buck DC-DC converter with hysteretic control has been reported [SCH 04], which operates at 480 MHz with efficiency of 72%, thus enabling a dramatic reduction in the size of the passive components. The paper also reported that the only impediment for realization of this technology is the lack of suitable integratable core materials for inductors in high-frequency operation.

With the use of today's magnetic materials, the size reduction of the magnetic components with frequency hits a limit due to frequency-dependent losses such as hysteresis loss, eddy current loss and ferromagnetic resonance (FMR) loss in the material. It is also the case that the market for higher frequency magnetic materials presently used for power conversion is dominated by ferrite materials, which due to the high-sintering temperature required for fabrication are typically not compatible with on-chip integration. To take full advantage of miniaturization and integration at increased frequency, clearly improved magnetic materials, which are fully CMOS integration compatible, are required.

15.3. Materials and integration

The operating frequency of present-day discrete soft magnetic cores of transformers/inductors varies from the quasi-static (50–60 Hz), right up into approximately the hundreds of megahertz region. Over the years, different core materials (cores) have been developed to meet the specific needs of a variety of operating conditions and environments. Different cores have been optimized for power density, cost, weight, volume, etc. The field of ferromagnetic (FM) core research was considered a well-established one, where only a few material types are dominant in terms of their overall percentage use. Main-stream, "off the shelf" cores can be broadly subdivided into five main categories: (1) steel/iron-based materials that are mainly based on iron with additives such as phosphorous (P), nickel (Ni) and silicon (Si); (2) ferrite cores that find use in higher frequency applications and are based on oxides of metals [WIL 92]; (3) powder-based cores created by compacting individual FM particles coated in an inorganic insulating layer and held together with an organic resin as a binder [ASA 05]; (4) amorphous alloys that are

non-crystalline in nature and can be created by electroplating or melt spinning; and (5) more recently developed different nanocrystalline alloys, prepared primarily by providing suitable heat treatment to the melt spun amorphous alloys or by RF magnetron sputtering of different constituent elements. Figure 15.2(a) displays the different "families" of conventional soft magnetic materials, while Figure 15.2(b) shows that nanocrystalline soft magnetic materials possess both high saturation flux density and high permeability.

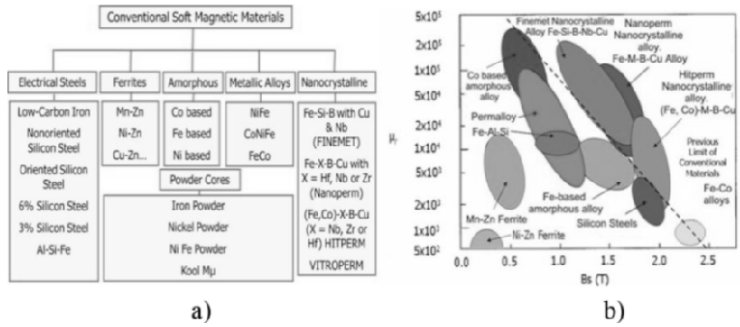

Figure 15.2. *a) Conventional magnetic material "families" and b) B_{sat} versus μ_r for conventional and nanocrystalline soft magnetic materials. For color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

Nanocomposite (metal/ceramic) materials produced by sputtering techniques show an interesting range of magnetic properties, not achievable by more conventional magnetic material synthesis techniques. In particular, because of their high resistivity and high FMR frequency (i.e. when the frequency of the applied microwave field matches the characteristic precessional frequency of the atomic magnetic spins), these materials show promise for use in future miniaturized RF components operating at gigahertz frequencies. Examples of such materials include (Co1-xFex)-Al-O granular thin films (nanocrystalline FeCo with 5 nm grains in an Al + O amorphous matrix) prepared by Ohnuma *et al.* [OHN 96, OHN 99] RF reactive magnetron sputtering in an O_2 atmosphere and achieved a saturation flux density (Bs) of 2.0 T, resistivity (ρ) of 200 μΩ-cm and coercivity (Hc) less than 397A/m at around x = 0.7. Sato *et al.* [SAT 00] developed a thin amorphous film of N7 the film by $Fe_{59}Co_{20}B_{14}N_7$ by dc magnetron sputtering, which upon magnetic field annealing transformed to nanocrystalline grains of FeCo embedded in a BN-rich matrix giving Bs = −1.7 T, ρ = 300 μΩ-cm, Hc = 19.9 A/m and a permeability of 900 maintained up to 300 MHz. Other notable research includes Sassaki *et al*. [SAS 97], who developed $Co_{44}Fe_{19}Hf_{15}O_{22}$ and $Fe_{61}Hf_{13}O_{26}$ by RF reactive sputtering. Among other significant efforts, Sullivan and coworkers [MEH 99, PRA 00] achieved nanocrystalline Co/Al_2O_3 deposition by O_2 atmosphere reactive sputtering.

Figures 15.3 and 15.4 show some of the materials and properties that were reported by Hatakawa *et al*. [HAT 97] and Makino *et al*. [MAK 99], respectively. These figures show the quality factor and the real part of the complex permeability. The relative complex permeability of a sample is given by

$$\mu_r = \mu_r' + j\mu_r'' \qquad [15.1]$$

where μ_r' is the real part of permeability and represents the non-dissipative processes within the system, whereas μ_r'' is the imaginary part of permeability and represents the dissipative processes (typically the conversion of energy to heat within the material). When there are no losses in the system, then $\mu_r = \mu_r'$ while conversely at the point where all of the energy is converted to heat, then $\mu r = j\mu r''$. In this chapter, the material properties of Bs > 0.9 T, $\rho > 4$ μΩm and Hc < 400 A/m were reported in the sputtered state for Fe-Hf-O. The structure of the film was composed of ultrafine grained bcc phases less than 10 nm situated in an amorphous phase reminiscent of the nanocrystalline materials described in previous sections. Hayakawa also discovered that by sputtering under a uniaxial magnetic field, a Bs of 1.3 T with μ′ of 1,400 up to 0.1 GHz was attainable for $Fe_{62}Hf_{11}O_{27}$ film, as deposited. With the addition of Co, a flat μ′ of 170 up to 1 GHz was reported with Qs as high as 61 at 0.1 GHz.

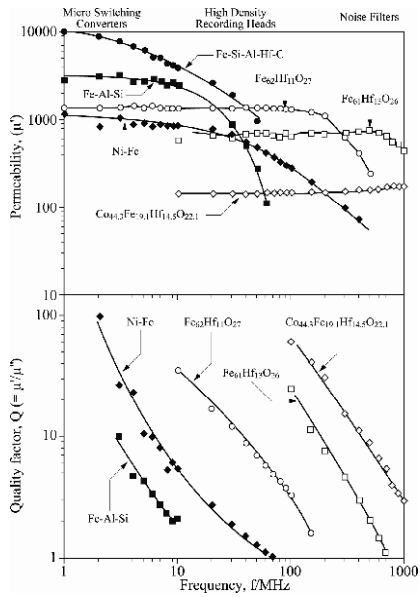

Figure 15.3. *Frequency dependence of the real part of initial permeability μ' and the quality factor Q for a number of materials [HAT 97]*

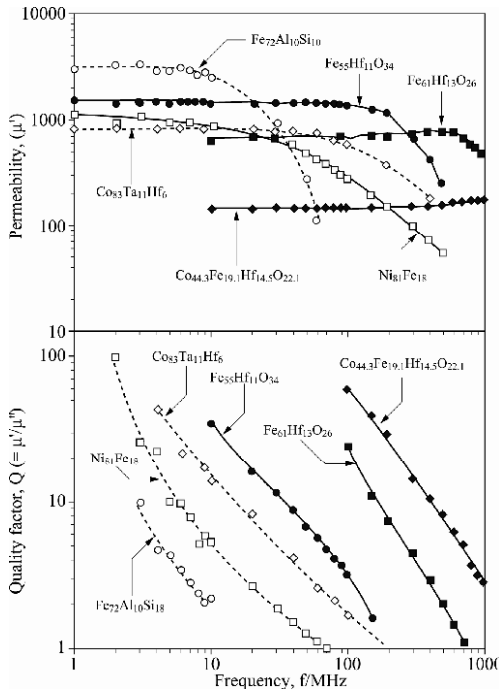

Figure 15.4. *Frequency dependence of permeability and quality factor for Fe-Hf-O and Co-Fe-Hf-O films compared with other materials [MAK 99]*

Although new generations of sputtered films have recently been used in thin film recording heads and integrated inductor structures for their high-frequency operation, power devices typically would require a thicker overall layer of magnetic material with an in-plane magnetic anisotropy to achieve high permeability and power density. As an example, inductor application of these materials has been demonstrated [MEH 99] at low power density in an otherwise efficient high-frequency DC-DC converter. To minimize eddy current loss, thick films can of course be built up from multiple thin metallic layers isolated from one another by an insulator, i.e. laminated films. However, lamination of the layers only controls the eddy current loss in the film's cross-section, but does not control the loss in the in-plane direction unless extra patterning is introduced. In-plane eddy currents can be a significant problem in common inductor geometries where the conductors are sandwiched between the magnetic layers. This problem has led to the significant interest in the use of granular films [SHI 03] to increase resistivity as opposed to the use of laminated metallic films. Several attempts to produce thicker nanocomposite materials by sputtering have resulted in striped domains with perpendicular

anisotropy. The occurrence of strong perpendicular anisotropy is suggested to originate from columnar structure with columns perpendicular to the film.

15.4. Controlling the magnetic properties

To target a good soft magnetic material, which will work in the high/very high frequency range, the following properties must be controllable and their relationship to the material structure is understood:

– coercivity (H_C);

– permeability (μ);

– saturation flux density (Bs);

– resistivity (ρ);

– cut-off frequency for eddy current loss (f_{ed});

– anisotropy field (H_K);

– natural FMR frequency (f_{FMR}).

1) *The material must have a low coercivity (H_c)*: to minimize the hysteresis loss with increasing frequency (hysteresis loss $\propto$ frequency), either the flux density or coercivity can be reduced. While the former is not a viable option in most applications, reducing the width of the hysteresis loop by reducing the coercivity is desirable. Coercivity has for some time being known to be related to grain size. When the grain size (D) is less than the FM exchange length (L_{ex} see [15.9]), coercivity is found to be related to the effective (or net) anisotropy <K> [HER 90], irrespective of the different mechanisms (domain displacement or rotation) of magnetization reversal, as:

$$H_C = b\,[<K>/M_S] \qquad [15.2]$$

where b is a constant close to unity and M_S is the saturation magnetization. Again effective anisotropy can be written in terms of the FM exchange length as:

$$<K> \approx K_1\,(D/L_{ex})^6 \qquad [15.3]$$

where K_1 is the first magnetocrystalline anisotropy constant. Now substitution of [15.3] into [15.2] results in:

$$H_C \approx b\,[K_1/M_S]\,(D/L_{ex})^6 \qquad [15.4]$$

which clearly shows that by restricting crystalline (different metals and metallic alloys) growth below the FM exchange length, we can reduce coercivity drastically. Since the effective anisotropy <K> results from the mean fluctuation amplitude of the anisotropy energy within the volume of the FM exchange length, an effective cancellation of the magnetocrystalline anisotropies will occur by the exchange interaction between the grains with magnetocrystalline anisotropies K_1 orientated randomly.

2) *The material must have a high resistivity (ρ)*: a high resistivity will allow for a control of eddy current effects. These eddy currents represent a dissipative loss of energy within a material and an increase in the temperature of the core; hence high resistivity is desirable. In addition, a high resistivity will increase the skin depth of the material. Skin depth should be suitably high to ensure that the magnetic field intensity does not change as a function of depth into the magnetic film. A high resistivity also minimizes the need for core laminations, thus maximizing the saturation magnetization of the core while simplifying the fabrication steps and associated cost.

Assuming the magnetic material to be deposited as a film, the cut-off frequency for eddy current loss, where due to the skin effect the real part of the permeability drops to two-thirds of its initial value, is given by:

$$f_{ed} = (4\pi)(\rho/\mu_0\mu t^2) \qquad [15.5]$$

where t is the film thickness. This means that for a given moderate permeability, we have to increase the resistivity of the film or decrease the film thickness to increase the value of f_{ed}. Consequently, laminated layers of alternating magnetic and insulating material have been used where thick films are required at high frequency. Generally, oxides are known to have very high resistivity and nanocrystalline alloys embedded in amorphous ceramic matrices are expected to give higher resistivity than pure crystalline alloys.

3) *The material must have a high saturation magnetization (M_s)*: this will maximize the permeability of the FM core as:

$$\mu_r = (4\pi M_s/H_k) + 1 \qquad [15.6]$$

where H_k is the anisotropy field. The anisotropy field relates to the anisotropy forces (crystal anisotropy, magnetoelastic anisotropy, shape anisotropy, etc), which hold a domain's magnetization in the easy axis direction (i.e. axis of easy magnetization). For a rotation in the magnetization away from the easy axis direction, the anisotropy acts like a magnetic field trying to hold the magnetization parallel to the easy axis and hence is called the anisotropy field. High M_s will also reduce the requirement

for an air gap (used to prevent core saturation) in the core, which would reduce the effective permeability (by increasing the magnetic reluctance of the core). In addition, according to Snoek's law [ACH 08] for soft magnetic thin films with uniform uniaxial in plane anisotropy ($\mu'_{f=0}F_{fmr}{}^2 \propto M_s{}^2$), where $\mu'_{f=0}$ is the permeability at low frequency and F is the FMR frequency. This shows how a high saturation magnetization will lead to a higher resulting product of permeability multiplied by FMR.

4) *The material must have a large real permeability (μ' or μ_r') that will hold up to high frequencies*: as the operating frequency of the magnetic material increases, then the material's quality factor ($Q = \mu_r'/\mu_r''$) will begin to decrease as the dissipative loss mechanism's within the material as represented by μ_r'' will also increase. With complex permeability $\mu_r = \mu_r' + j\mu_r''$, a large magnitude of μ_r' will necessitate a small value of μ_r'' ($\int_0^\infty \mu''(f).f.df = k(\pi/2)(2\gamma M_s)^2$) across the operating frequency range of interest.

5) *The material must also be integration compatible*: this necessitates a processing temperature low enough that it does not damage adjacent integrated circuitry (maximum CMOS processing temperature ~ 450ºC).

6) The *Curie temperature* of the material should also be above the intended operating temperature, so the material is not driven from an FM to a paramagnetic state.

7) *Low anomalous loss*, where this loss has reportedly been attributed to complicated distributions of eddy currents caused by the domain wall motion at higher frequency.

8) *A high FMR frequency* for very high frequency operation. The natural FMR frequency f_{FMR}, which plays a greater role in the gigahertz range, should be as high as possible.

The FMR frequency for thin films along the hard axis can be derived from the Landau–Lifshitz–Gilbert equation [GIL 55] as:

$$f_{FMR} = (\gamma/2\pi)(M_S H_K) \qquad [15.7]$$

where γ is the gyromagnetic constant (which relates the angular momentum of the electron (spinning around the nucleus) L and the magnetic moment m using the equation $m = \gamma L$) and H_K is the uniaxial anisotropy field. Again the real part of the permeability in the hard axis direction can be approximated for pure rotation as:

$$\mu = 4\pi M_S/H_K \qquad [15.8]$$

9) *The material must have a controllable anisotropy field*, which affects FMR and permeability. The concept of anisotropy here refers to the dependence of the energy within the system on the direction of the magnetization. The anisotropy field relates to the crystal anisotropy forces, which hold a domain's magnetization in the easy axis direction. If a material's anisotropy energy is minimized when the magnetization is aligned along one particular axis (easy axis), then the sample is said to have uniaxial (or hexagonal) anisotropy (an example of a material with uniaxial anisotropy is cobalt). For a uniaxial crystal, $H_k = 2K_1/M_s$ (cgs) or $2K_1/\mu_o M_s$ (SI) where K_1 is the first anisotropy constant.

Hence, from equations [15.7] and [15.8] described above, it can be concluded that for a higher anisotropy field, the permeability is reduced and for a lower anisotropy field, the f_{FMR} is reduced. For this trade-off relationship, a controllable anisotropy within, e.g. 800–4,000 A/m is needed. To produce a uniaxial anisotropy during deposition, a suitable magnetic field may be applied in the in-plane direction of the film to generate the magnetically easy axis along the direction of the magnetic field with the hard axis orthogonal to that. Other anisotropies may also be tailored for magnetic property tuning, for example shape anisotropy.

10) The material's deposition process must also be *low cost* to facilitate mass production and compete with existing and conventional low-cost fabrication technologies.

11) The material should also possess suitable *corrosion resistance* properties to ensure the longevity of the finish product.

Although it is clear that certain parameters such as coercivity should be minimized while other parameters such as saturation magnetization and resistivity should be maximized, in reality these parameters cannot be independently tailored owing to the fact that they are interrelated through the micro-/nanostructure of the material. Thus, for example, while it is always desirable to increase resistivity, this is usually achieved at the cost of a reduced saturation magnetization by the addition of extra non-magnetic elements into the material composition. For a high-frequency application, the increase in resistivity and hence also the reduction in associated losses is typically considered an improvement despite the trade-off of low saturation magnetization (e.g. ferrites). Similarly, there is a trade-off between the permeability and anisotropy field, and for many applications (e.g. those involving dc bias currents), a modest permeability is often acceptable in order to prevent saturation. Finally, the case for what constitutes improved parameters for any magnetic material needs to be evaluated in the light of the specific application scenario.

15.5. Magnetic properties of nanocomposite materials

In relation to magnetic properties, historically, fine particle/granular systems have long been studied, particularly for increasing hard magnetic properties [LUB 61]. As the size of each individual particle gets reduced and approaches single domain size, coercivity increases (see Figure 15.5). This happens because of the reduction in cancellation of spins by different domains in a single grain. Accordingly, the approach in conventional soft magnetic material engineering has been to make the grain size as large as possible to obtain low coercivities and high permeabilities [PFE 80].

In the last two decades, significant advances in soft magnetic material properties have been achieved with the advent of new classes of materials with nanosized grains. By melt spinning and subsequent annealing, it was found to be possible to prepare multicomponent (i.e. nanocrystals in an amorphous matrix) nanocrystalline alloys such as VITROPERM ($Fe_{73.5}Cu_1Nb_3Si_{13.5}B_9$) [YOS 88, HER 93, PET 02] or NANOPERM ($Fe_{85.6}Cu_1Nb_{3.3}Zr_{3.3}B_{6.8}$) [MAK 97] with substantially improved soft magnetic properties (Bs = 1.3–1.7 T, ρ = 50–115 $\mu\Omega$-cm, H_C = 0.01 Oe). Typical behavior of soft magnetic materials in relation to coercivity and grain size is shown in Figure 15.5. It is evident from the figure that for large grain sizes (D >~ 100 nm), coercivity varies with 1/D reflecting the classical rule: good soft magnetic properties require very large grains. For smaller grains (D <~ 20nm), coercivity varies with D^6 signifying the role of ultrafine crystallites in achieving good soft magnetic properties. The latter D^6 variation with coercivity occurs because (1) nanocrystallites being much smaller in size (10–15 nm) than the FM exchange length (~35 nm), L_{ex}:

$$L_{ex} = (A/K_1)^{1/2} \qquad [15.9]$$

where A is the exchange stiffness, K_1 is the first magnetocrystalline anisotropy constant; the effective magnetocrystalline anisotropy gets reduced by the exchange interaction between the randomly distributed smaller grains as in the random anisotropy model [ALB 78]; (2) the large positive magnetostriction of the amorphous matrix gets cancelled with the negative magnetostriction summed over the total nanocrystalline bcc phases resulting in almost zero magnetoelastic anisotropy.

One of the other reasons for the superior soft magnetic properties in the nanocrystallized glassy alloys [PET 02] (e.g. Nanoperm) over the nanocrystalline materials produced by methods, such as compaction of nanometer-sized powders [BIR 88], is the difference in configuration of interfacial layers. In the case of compacted nanometer-sized powders, there is a wide distribution of interparticle spaces with almost no short-range order, whereas in nanocrystallized glassy alloys,

the interfacial layer is in a well-relaxed amorphous state with relatively pronounced short-range order.

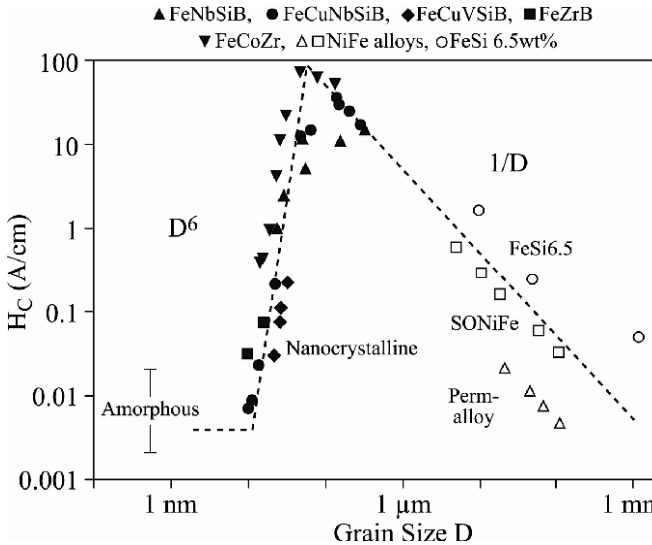

Figure 15.5. *Coercivity versus grain size for various soft magnetic alloys. The nanocrystalline materials shown are ▲, FeNbSiB; ●, FeCuNbSiB; ◆, FeCuVSiB; ■, FeZrB; ▼, FeCoZr; △□, NiFe alloys and O, FeSi 6.5 wt% [HER 93]*

As a result, many researchers have attempted to develop thin film nanosized soft materials using the sputtering technique. Among them, $Co_{44}Fe_{19}Hf_{15}O_{22}$, $Fe_{61}Hf_{13}O_{26}$ by RF reactive sputtering, $Co_{1-x}Fe_x$-Al-O granular thin films by RF reactive magnetron sputtering in oxygen atmosphere, and thin amorphous and nanocrystalline films of $Fe_{59}Co_{20}B_{14}N_7$ (FeCo nanocrystalline grains in BN-rich amorphous matrix) by dc magnetron sputtering are important to cite for their technological relevance. It was inferred that due to the high resistivity of the amorphous matrices, the overall resistivity of the films became higher and the nanocrystalline phase gave rise to the low coercivity. However, until relatively recently [PET 04, SOU 04], it was unclear both in theoretical understanding and experimental evidences (as briefly outlined below) why and how even a highly resistive, structurally nonpercolative, configuration of the sputtered nanocrystalline/amorphous materials show such a long-range FM order. This phenomenon, which has been investigated by a number of authors, is expounded in the following.

The macroscopic properties of nanostructured composite magnetic materials are determined by the size, morphology, and structure of the constituent phases and by the type and strength of magnetic coupling between them. For an assembly of noninteracting particles and with decreasing particle size, the magnetic anisotropy energy (which is proportional to particle volume) per particle responsible for holding the magnetic moment along certain directions becomes comparable to the thermal energy. As a result, the thermal fluctuations induce random flipping of the magnetic moment and the nanoparticles lose their stable magnetic order to become superparamagnetic (SPM) [CHI 97]. Thus, the demand for further reduction in the size of each individual non-interacting particle encounters the so-called "superparamagnetic limit" [WEL 99, THO 00]. This phenomenon has serious implications for theoretical maximum storage densities on magnetic storage media. However, when those non-interacting individual particles are brought close to each other, interparticle interactions (dipole–dipole or exchange interactions) compete with the anisotropy energy in determining the orientation of the particle moments. If strong enough, these interactions may turn the collection of individual SPM relaxation processes into a collective dynamical behavior [MAM 98, DOR 96] with domain wall motion or magnetization rotation as the reversal mechanism. Recently, this has been termed as superferromagnetism (SFM) in granular structures. So far, it has been established that a crossover from pure Néel–Brown-type SPM to superspin glass (SSG) behavior (i.e. spin frozen state out of competing interactions) takes place at low temperature for three-dimensional (3D) randomly distributed nanoparticle systems with high enough density and sufficiently narrow size distribution [JON 98, DJU 97, DOR 99]. However, transitions from SPM to SFM long-range order have been observed only in one-dimensional (1D) and two-dimensional (2D) self-organized [SUG 97, SHE 97, HAU 98] or regularly structured arrays of FM nanoparticles [COW 99b] with mainly dipolar interactions [HAU 98, LUT 46] and in a specific case, exchange coupling of supermoments [SCH 96] as the prevailing mechanism. Indeed, the coupling of point dipoles in 3D systems was predicted to form antiferromagnetic domain states [LUT 46, KRE 79]. Only recently has it been suggested that dipolar stray fields between finite size granules (superspins) can produce FM coupling (superexchange) to give rise to SFM order in disordered nanoparticle systems within discontinuous metal–insulator multilayers (DMIM) [DOR 99, SUG 97, CHE 03, KLE 01, KAK 03, BED 07] of $[Co_{80}Fe_{20}(t)/Al_2O_3(3\ nm)]_{10}$ as shown in Figure 15.6.

In a typical case, the nominal thickness of CoFe layer (t) has varied from 1 to 2.5 nm. It was found that at structural percolation t = 1.8 nm, electronic transport changed from activated to metallic conduction, whereas at t = 1.7 nm, the magnetic domain structure changes from dipolar (long range) coupled to exchange (short range) coupled domains leading to SFM to FM transition and way below at t = 1.1 nm, SPM to SFM transition was reported.

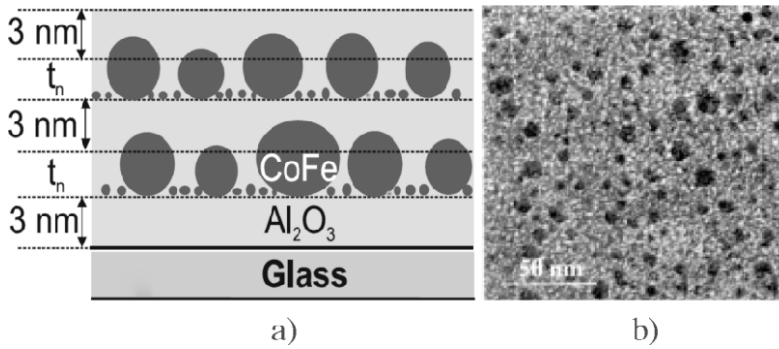

Figure 15.6. *a) Pictorial illustration of the structure of the $Co_{80}Fe_{20}/Al_2O_3$ discontinuous metal–insulator multilayers and b) TEM image of metallic composite layer [BED 07]*

15.6. Magnetic properties of nanomodulated continuous films

Anisotropy control through surface topographic manipulation has been demonstrated as a facile means of tailoring high-frequency performance. The film's anisotropy is a key parameter in determining the high-frequency response while the other parameters are fixed. This can be achieved simply by manipulating local in-plane and out-of-plane dipolar stray field in a nanomodulated soft FM continuous film without forming the vortices. This was demonstrated through novel fabrication processes that include the combination of nanoimprint lithography and electroplating of magnetic films. The experimental results were validated by developing associated theory and micromagnetic modeling.

One of the most significant challenges in patterned FM films is to configure their magnetization directions. In polycrystalline materials due to insufficient long-range microscopic crystalline order, this is mainly determined by external environmental effects or geometry [BRI 10]. Greater application of these materials relies on the ability to control the magnetic anisotropy based on spin configuration and pattern geometry. This phenomenon has been studied and demonstrated for patterned isolated magnetic structures [SKO 98, LI 01, COW 99a] and continuous magnetic films [LI 10, CHA 98] (Figure 15.7) to manipulate different magnetic properties. While patterned isolated magnetic structures have been extensively studied [CHA 98, CHO 97, COW 99b], structured continuous magnetic films have also drawn considerable attention in recent years [LI 01, NGU 97, TWI 02, BRI, LI 02]. Furthermore, the optimization of magnetic parameters, such as pattern geometry, film thickness, intrinsic anisotropy and coercivity, is essential for obtaining

controlled magnetic properties in a film by nanomodulation (see Figure 15.8) in a cost-effective way. Magnetostatic energy induced by strong nanomodulation forces the spins into local vortices, which is unfavorable for many applications. An optimized modulation of continuous thin film can overcome these drawbacks in applications such as in micromagnetic devices. Several methods have been used to control magnetization configuration in magnetic films without breaking the film continuity, such as ion irradiation through mask [CHA 98], selective epitaxy and surface modulation [NGU 97, BRI 09]. Surface nanomodulation by nanoimprint lithography is attractive because it provides potentially a low cost, simple method to engineer spin configuration locally in magnetic films, which is essential for many magnetic devices, such as high-precision bidimensional magnetic sensors and magnetoresistive devices [BRI 09, OEP 96].

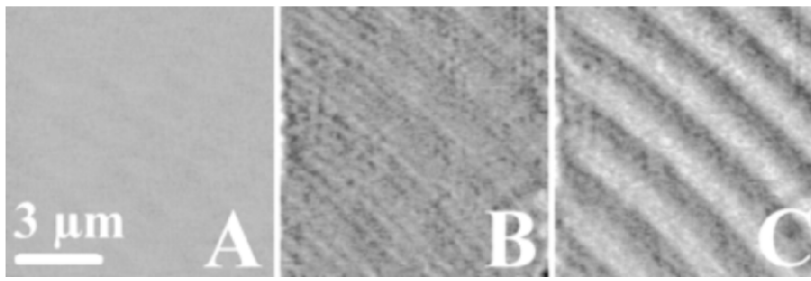

Figure 15.7. *Images in near-field magneto-optical microscopy of an array of stripes 1 µm wide, separated by 1 µm, magnetically patterned in a Pt-[Pt (1.4 nm)-Co (0.3 nm)]$_6$-Pt-Herasil multilayer. a) Optical transmission image (without polarization analysis). b) Magneto-optical image of the magnetically saturated array. The faint contrast is due to residual PMMA before exposure to oxygen plasma. c) Magneto-optical image of the array after reversal of the magnetization in the irradiated area only (white stripes). Magnetic resolution of the experiment was about 200 nm [CHA 98]*

Electrodeposition is widely used to deposit magnetic thin films, especially for industrial applications due to its cost effectiveness compared to other methods. The nanopatterned substrates for electroplating [LIS 11] are prepared by nanoimprint lithography followed by planarization and metallization. A silicon stamp fabricated by exposing twice in each of the perpendicular directions using optical interference lithography and subsequent ion reactive etching is used as an imprinting tool to print the PMMA layer with a nanohole array of different geometry (Figure 15.8(a)). The hole structure in PMMA is partially planarized by the spin coating of polystyrene solution in toluene (Figure 15.8(b)). A 10 nm Ti adhesion layer with a subsequent 200 nm layer of Au is sputter deposited to form a seed layer for electrodeposition

(Figure 15.8(c)). During the electrodeposition of $Ni_{45}Fe_{55}$ thin film (Figure 15.8(d)), an external magnetic field is applied along the direction of the square pattern to induce a uniaxial anisotropy (henceforth referred as induced anisotropy).

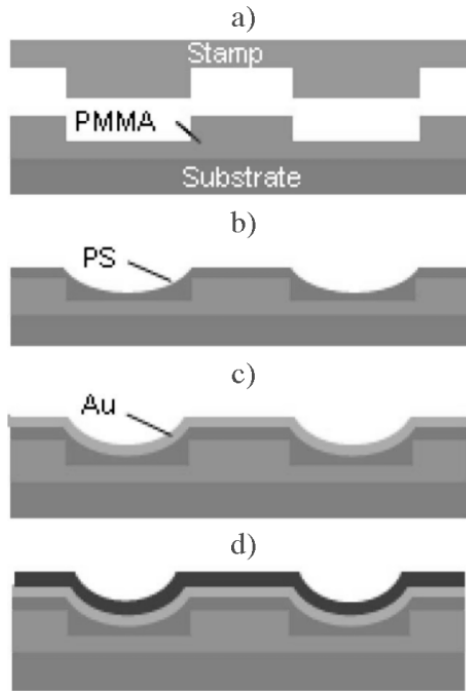

Figure 15.8. *Schematic illustration of the sample preparation process. a) Nanoimprinting PMMA; b) polystyrene (PS) coating; c) gold deposition; d) magnetic layer plating [LIS 11]*

It is observed that the remanent magnetization (Mr) and coercivity (Hc) of patterned continuous film both vary as a function of angle due to magnetic anisotropy created by nanomodulation [MAI 12]. In Figures 15.9(d) and (e), normalized remanent magnetization (Mr) for such patterned continuous film is shown as a function of sample rotation angles with respect to applied in-plane field direction for two different patterns. Both patterns show four-fold symmetry, whereas satellite maxima of the higher order are prominent in a 400 nm pattern (Figure 15.9(d)). The anisotropy based on nanomodulation is so strong that it could dominate over the film's uniaxial anisotropy, which is induced by plating in the presence of a magnetic field. There is a very minute difference between the remanence magnetization at 0º and 90º, which is due to the influence of uniaxial anisotropy of the film. A phase shift is observed in a 200 nm pattern (Figure 15.9(e)) for higher aspect ratio (diameter/separation (D/S) = 3:1).

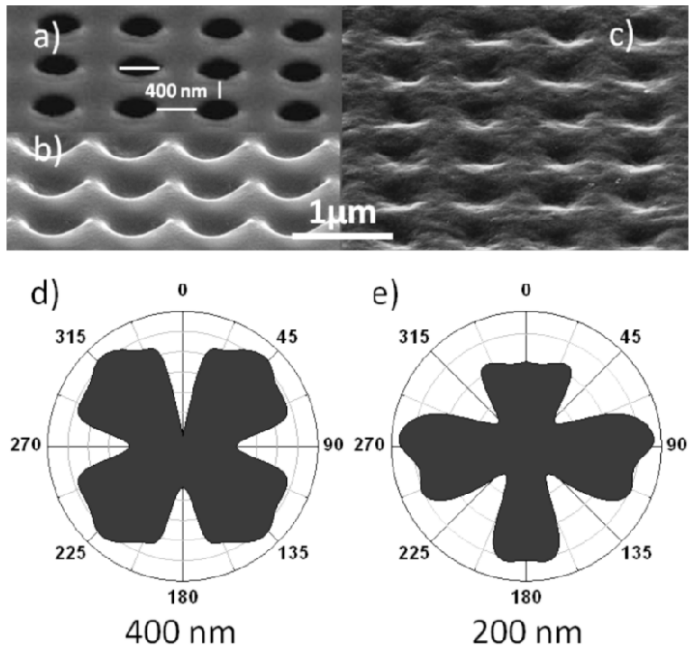

Figure 15.9. *a) SEM image of nanohole array on PMMA on Si. b) Gold seed layer on patterned substrate. c) Electroplated continuous $Ni_{45}Fe_{55}$ on nanomodulated substrate. d) and e) Angle-dependent remanent magnetization (Mr vs. θ) measured from 3D nanomodulated film with 400 nm and 200 nm element diameter, respectively [MAI 12]*

It is found that the nanomodulated film requires a very high field to reach saturation magnetization due to the formation of magnetic dipoles and their strong coupling. With the change of external magnetic field, the magnetic dipole goes through a transition from a stable to a metastable state (Figure 15.10). At near-zero field, the remanence Mr suddenly jumps from positive magnetization to negative, which indicates the existence of magnetic dipoles with non-zero Mr. Thus, a complete vortex cannot be achieved in such structure. For a square array pattern of 400 nm diameter and 100 nm modulation amplitude (D/S is 1), the calculated energy densities are 0.49×10^4 and 1.33×10^4 J/m^3 for vortex and near-single-domain state, respectively. Since the energy of a vortex state is less than that of a near-single-domain remanent state, there should be a strong inclination to adopt vortex states in the nanomodulated continuous FM thin films. On the other hand, it is necessary that the demagnetization processes needs to overcome the higher energy barrier to create a local vortex in nanomodulated continuous FM thin films, where spins are strongly

exchanged in parallel due to dipole–dipole interaction. Thus, these dipole interactions in this patterned matrix try to resist the formation of vortices, which is analogous to closely packed magnetic dots [ZHA 01]. As a result, a near-single domain state originates at the remanence magnetization state with an intention to become a vortex state.

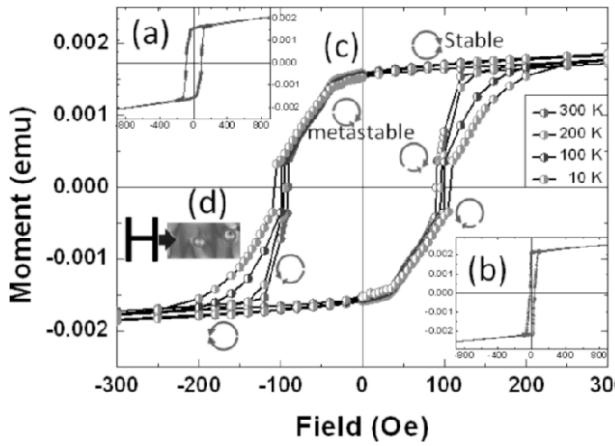

Figure 15.10. *Hysteresis loop measure from thin nanomodulated sample, a) 150 nm and b) 50 nm, shows metastable state. c) Step-like MH curve (zoomed of 150 nm thickness) in various temperatures shows existence of metastable dipoles throughout the temperature range. Near-zero remanence, the dipoles suddenly jump from positive to negative value. d) OOMMF simulated picture of magnetization configuration near remanent shows incomplete vortex formation [MAI 12]. For color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

However, thick films show uniaxial anisotropy since dipolar anisotropy is weaker compared to induced uniaxial anisotropy. Very thin films only show fourfold anisotropy symmetry, where dipoles are too weak for higher order dipolar interaction.

Thus, thickness t near modulation amplitude A shows maximum anisotropy variation in easy and hard directions (Figure 15.11). The results have been explained by recently developed power law for a magnetic film with a roughness-induced demagnetizing effect $H_K \sim \tilde{N}M_S \sim A^2 / t$ ($\tilde{N}$ is demagnetizing tensor) [CHO 99, ZHA 99]. Since the power law was derived using a demagnetizing tensor ($\tilde{N}$) for demagnetizing field H_d in a magnetostatic phenomenon, it supports the argument that the symmetry of magnetic anisotropy comes from 3D nanomodulation, which has been shown by means of variation of remanent magnetization. The symmetry is based on alignment of the pattern-induced magnetic dipoles and their interactions.

The direction of effective dipole interaction depends on the direction of applied field. In the MFM image (Figure 15.12), the dipoles are aligned in <110> direction as an external field (1,000 Oe) was applied in that direction before imaging. In case of an allignment in a certain direction by an external field depending upon the pattern symmetry, dipoles across each patterned elements are coupled with their neighbors and the demagnetization energy decreases with an increase in remanent magnetization due to strong dipole–dipole interactions. Furthermore, the linear density of the dipoles changes as a function of directional angle and hence the net dipole interaction varies.

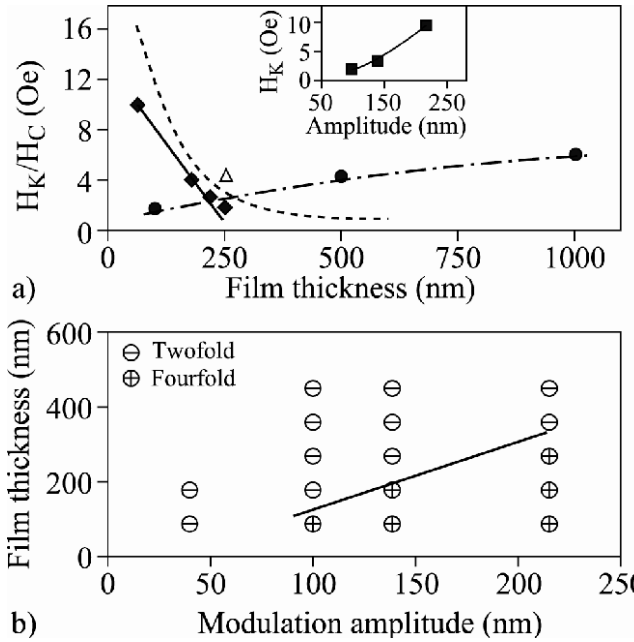

Figure 15.11. *a) Thickness dependence of anisotropy field taken from both patterned (diamond) and unpatterned films (solid circle), and together with coercivities measured from unpatterned films (open triangle). The anisotropy fields of unpatterned films were taken from hard axes. Inset shows a modulation amplitude dependence of topographic anisotropy. b) An experimental phase diagram that defines a transition from fourfold topographic anisotropy to twofold-induced anisotropy with increasing film thickness and reducing surface modulation [LI 10]*

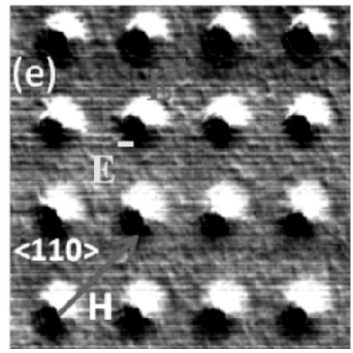

Figure 15.12. *MFM phase images of dipoles. An external field of 1,000 Oe was applied in <110> direction before imaging. The images were taken at a 50 nm distance from sample surface [MAI]. For color version of this figure, see www.iste.co.uk/balestra/nanodevices1.zip*

The pattern gives both in-plane and out-of-plane modulation (Figure 15.12), which allows dipoles to rotate. The effective dipole–dipole interaction strength is based on three different parameters: out-of-plane modulation amplitude, in-plane modulation amplitude and direction, based on modulation geometry and their arrangements.

The angularly dependent magnetic anisotropy is written by an equation in the following way:

$$H_K(r,\phi,\theta) = \frac{2}{\mu_0 M_S}\left[\frac{K_S \bullet V}{2}\sum_{i\neq j}\cos(i)\bullet\cos(j) + K_I\sin^2\theta + \sum_n K_n\cos^2(n.2\theta) + K_0\right] \quad [15.10]$$

where the elements in the square bracket are in the following order: (1) global shape anisotropy of the sample, (2) induced uniaxial anisotropy, (3) anisotropy due to patterning and (4) any other anisotropy. Except for the second and third part, the others remain the same for comparison as a function of angle. For patterned structure, the simplified equation is written as follows:

$$H_K(\theta) = \frac{2}{\mu_0 M_S}\left[K_I\sin^2\theta + \sum_n K_n\cos^2(n.2\theta)\right] \quad [15.11]$$

The expression has been generalized by a possible directional symmetry where $n = \beta/\alpha$; α is a number representing a minimum geometrical symmetry (i.e. four for square and three for equilateral triangle/hexagon) and β is a positive integer. K_n denotes the anisotropy constant for the corresponding symmetries. In nanomodulated films, the magnetization follows a wave-like path due to modulation

geometry and creates two types of magnetic charge dipoles [ZHA 99]. Since magnetic induction $\mathbf{B} = \mu_0 (\mathbf{H} + \mathbf{M})$ do not have divergence, the points where lines of magnetization originate or terminate can be considered as magnetic charge poles with opposite polarity. Because of the wave-like modulation, two different types of dipoles are created. These dipoles can interact with each other strongly only when there is a chain of elements in the applied field directions, creating an anisotropic magnetization throughout the whole film. Considering all types of magnetic interactions in different regions and by using the sum rules given by Yafet *et al.* [YAF 86] (considering two different layers of the pattern such as magnetic and nonmagnetic) for an externally applied field H, we can write the magnetostatic energy in the following way for a patterned structure:

$$E_{mag} = \sum_{n,m} \int -\frac{1}{2} \vec{M}_{i\ n,m}^{j} \cdot \vec{H}_{n,m} dv \qquad [15.12]$$

where the distribution of magnetization can be expanded in Fourier series as follows:

$$M(x, y) = \sum_{n=0}^{+\infty} \sum_{m=0}^{+\infty} M_{i\ n,m}^{j} \sin(k_n x)\sin(k_m y) \qquad [15.13]$$

and the field that corresponds to each magnetization will be $\mathrm{div}H_i^j = -4\pi \mathrm{div}M_i^j$.

The interlayer interaction gives perpendicular anisotropy and the remaining effects give in-plane anisotropy. Rewienski [REW 95] found magnetic anisotropy of FM thin films due to surface roughness. Using the same principle, we have calculated the anisotropy energy due to each single element as

$$\mathbf{E}_{mag}^{\parallel} = \mathbf{C}_i \left(\frac{1}{2}\right) \mathbf{M}_S^2 \left(\frac{1}{4}\right) \left[\mathbf{A}\left\{\mathbf{1} - \mathbf{f}(2\ \boldsymbol{\pi}\ \frac{\mathbf{A}}{\mathbf{D}}\right\}\right]$$

and

$$\mathbf{E}_{mag}^{\perp} = \mathbf{C}_i \left(\frac{1}{2}\right) \mathbf{M}_S^2 \left(\frac{1}{2}\right) \left[-\mathbf{A}\left\{\mathbf{1} - \mathbf{f}(2\ \boldsymbol{\pi}\ \frac{\mathbf{A}}{\mathbf{D}}\right\}\right],$$

where C_i is a constant that depends on pattern geometry and aspect ratio, A is the amplitude of modulation and D is the diameter of each pattern. The function [HAU 98] f is 0 at A/D = 1 and 1 at A/D = 0. The dipolar anisotropy is given by $\mathbf{E}_{da} = \mathbf{E}_{mag}^{\parallel} - \mathbf{E}_{mag}^{\perp} \neq \mathbf{0}$, which gives a finite dipolar anisotropy energy depending

upon the modulation geometry. Considering up to second-order harmonics, we can rewrite the dipolar anisotropy for anisotropy energy as

$$K^S = C_i \cdot \left(\frac{1}{2}\right) 4\pi M_S^2 \left(\frac{3}{4}\right) A \left[1 - f\left\{2\pi \frac{A}{D}\right\}\right]$$

where A is the amplitude of modulation and D is the diameter of the element. The dipole–dipole interaction strength depends on the density of elements in a particular direction. Hence, one can add another term sin (90°/β) for patterned-induced magnetic anisotropy.

Using the expression for K^S, we can then rewrite [15.10]:

$$H_K(\theta) = \frac{2}{\mu_0 M_S} \sum_n .C \bullet A \left[1 - f\left\{2\pi \frac{A}{D}\right\}\right] \left\{\sin\left(\frac{90^\circ}{\beta}\right)\right\} \cos^2\left(\beta \bullet \frac{2\theta}{\alpha}\right) \qquad [15.14]$$

where $n = \beta/\alpha$ and the constant C depends upon single element geometry and diameter/separation (D/S). The above equation provides the theoretical foundation and describes how one can vary anisotropy by varying the geometry of nanomodulation for different FM films. The methodology adopted can open a new path to manipulate/obtain good high-frequency properties from a given soft magnetic core material in micromagnetic devices such as microinductors/transformers.

15.7. Conclusion

In the case of microfabricated and integrated inductors, the inductance values may be expected to be of the order of nanohenry or tens of nanohenry at switching frequencies of several hundred megahertz. It might be considered that with such small inductance values, magnetic material is not required to achieve the inductance. However, the use of a suitable magnetic material almost always increases the inductance achievable per unit area. This increase in inductance per unit area has been verified by many other researchers and has been shown to be as much as an eightfold increase at 200 MHz [ZHU 03], 30–50% increase at 2 GHz and a 19% increase at 2 GHz [YAM 01] for RF inductors. For any application that requires an integrated inductor of a specific value, the inductance enhancement can be directly translated to a saving in silicon area, which is of huge importance in any IC implementation. In general, size reduction also results in the reduction of parasitic resistance and capacitance, thus leading to an increase in self-resonant frequency. It is also worth noting that inductors required for power conversion applications require very low resistance compared to inductors designed for RF signal

applications. This requirement demands much larger conductor cross-sections and hence a larger inductor size. Thus, for power inductors, the size reduction achievable by the incorporation of magnetic material is even more critical than for RF inductors. For power inductors, the reduction of EMI through the shielding effect of certain magnetic core configurations may also be a very important consideration. The level of inductance enhancement is only possible, however, if the resistivity of the magnetic material is sufficiently high so that relatively thick layers of the material can be used at the frequency of interest.

It is also worth noting that a core of magnetic material is essential if coupled inductors or transformers are to be achieved, as good coupling between windings can only be achieved by the use of a magnetic core. In addition, the materials must be patternable, have reasonably good adhesion properties and have material properties that remain unaltered during subsequent process steps.

Published work to date has focused on the use of sputtering deposition for layers of different granular materials and nanomodulated electrodeposited films as discussed in the previous sections. The key requirements for such a material are medium permeability, high resistivity and high anisotropy field. There is definitely further scope for developing new generations of integratable, nanocomposite magnetic materials so as to have high Q-factor and power density, simultaneously, for next-generation power electronic and RF applications.

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