CMOS VLSI ENGINEERING
Silicon-on-Insulator (SOI)

CMOS VLSI ENGINEERING
Silicon-on-Insulator (SOI)

by

JAMES B. KUO
and
KER-WEI SU

National Taiwan University

Springer-Science+Business Media, B.V.

Library of Congress Cataloging-in-Publication Data

ISBN 978-1-4419-5057-4 ISBN 978-1-4757-2823-1 (eBook)
DOI 10.1007/978-1-4757-2823-1

Printed on acid-free paper

Originally published by Kluwer Academic Publishers in 1998.
Softcover reprint of the hardcover 1st edition 1998

Acknowledgements

The authors would like to thanks colleagues in Taiwan and professors at Stanford for their support during the past 11 years. Without their encouragements, this work is not possible. The author would like to thank J. H. Lou, S. C. Lin, C. H. Hsu, C. K. Huang, C. Y. Huang, Y. M. Huang, J. Y. Lai, R. J. Liu, J. C. Su, H. K. Sui, and K. H. Yuan, for their help on drawing. The author would like to thank Ms. Cindy Lufting, Mr. James Finlay, and Mr. Mike Casey of Kluwer for their help such that this book could be published.

Preface

Silicon-On-Insulator (SOI) CMOS VLSI technology has been regarded as another major technology for VLSI in addition to bulk CMOS technology. Owing to the buried oxide isolation structure, SOI technology offers superior CMOS devices with higher speed, higher density, and reduced second order effects for deep-submicron low-voltage, low-power VLSI circuit applications. In addition to VLSI applications, SOI technology has also been used to realize communication circuits, microwave devices, BiCMOS devices, and even fiber optics applications for its superior properties. There are three key factors in engineering SOI CMOS VLSI— processing technology, device modeling, and circuit designs. The mutual influences from three factors are important in developing a creative SOI CMOS VLSI technology. Improvements in the processing technology and understanding of the device behaviors lead to progresses in the SOI circuit designs. Requirements for low-voltage low-power high-performance SOI circuits in the world-wide portable systems serve as an incentive to further evolve the SOI CMOS processing technology. Understanding of the SOI CMOS device behaviors can provide new ideas for development of the next-generation SOI CMOS technology. In addition, the developed SOI CMOS device models can provide CAD tools for circuit simulation. In this book, these three key factors in engineering SOI CMOS VLSI are covered. Starting from the SOI CMOS processing technology and the SOI CMOS digital and analog circuits, behaviors of the SOI CMOS devices are presented. In addition, a CAD program—ST-SPICE, which incorporates models for deep-submicron fully-depleted mesa-isolated SOI CMOS devices, is described. This book is written for undergraduate senior students and first-year graduate students interested in CMOS VLSI. The arrangement of the book is designed for a 3 semester-unit course. This book is also suitable for electrical engineering professionals interested in microelectronics.

James B. Kuo and Ker-Wei Su
Taipei, Taiwan
November 1998

About the Authors

Prof. James B. Kuo received BSEE from National Taiwan University in 1977, MSEE from Ohio State University in 1978, and PhDEE from Stanford University in 1985. Since 1987, he has been with National Taiwan University, and currently is a professor. He has published numerous international journal papers. He serves as an associate editor for the IEEE Circuits and Devices Magazine and an AdCom member for the IEEE Electron Devices Society.

Dr. Ker-Wei Su received BSEE and PhDEE from National Taiwan University in 1994 and 1998, respectively. His research specialty is modeling of SOI CMOS devices.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

SOI CMOS technology has been becoming another major technology for next-generation VLSI[1]-[6]. In this chapter, starting from the fundamentals of SOI, the advantages of the SOI CMOS technology are described. The applications of SOI CMOS technology for realizing VLSI digital circuits are introduced. The objectives of this book in terms of processing technology, device modeling, and circuit designs for SOI CMOS VLSI are outlined.

1.1 What is SOI?

SOI is Silicon On Insulator— on the top of an insulator layer, a layer of silicon thin-film is used to build active devices and circuits. In the early stage of SOI technology, this insulator is made from silicon nitride or sapphire—silicon on sapphire (SOS). Nowadays, the insulator in the SOI is based on the oxide layer— the buried oxide layer is used to isolate the active device thin-film region from the substrate. Fig. 1.1 shows the cross section of an SOI CMOS device. As shown in the figure, on the bulk silicon substrate, a buried oxide layer is formed. On the top of the buried oxide layer there is a silicon thin-film, where active MOS devices and circuits are located.

At the beginning, the motivation of the development of the SOI technology is from the radiation hard properties of the SOI devices. Owing to the excellent isolation provided by the buried oxide, immunity of the SOI devices against high-energy particle illumination is excellent. Fig. 1.2 shows the radiation effects on bulk and SOI MOS devices. As shown in the figure, the radiation effects on bulk and SOI MOS devices are quite different. When illuminated by a ray of the α-particles, in the silicon region where the high-energy particles pass, electron-hole pairs are generated. As a result, a large amount of current is produced. For the SOI MOS device, the ac-

J. B. Kuo et al., *CMOS VLSI Engineering*

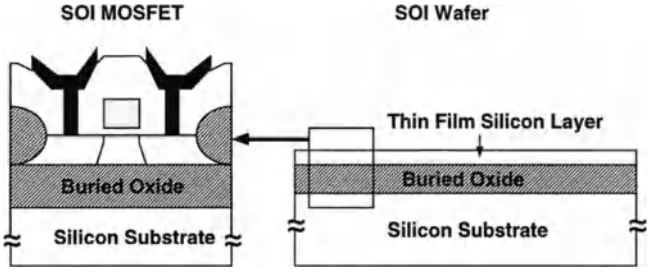


Figure 1.1: Cross section of an MOS device built on an SOI wafer.

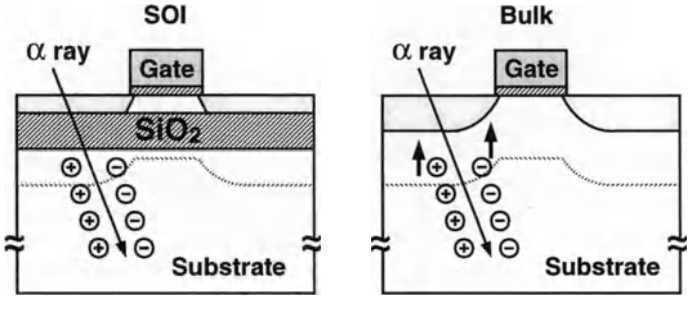


Figure 1.2: Radiation effect on bulk and SOI MOS devices.

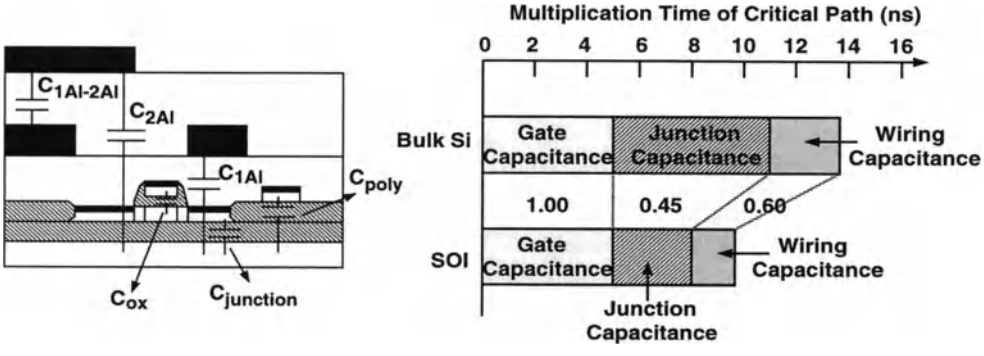


Figure 1.3: Comparison of the parasitic capacitances between bulk and SOI CMOS devices and the multiplication time of a 16bit x 16bit multiplier circuit built on a 0.6μm CMOS gate array in bulk and SOI technologies.

tive thin-film region is totally isolated from the substrate. Therefore, the α-particle induced current has little influence in the device performance. In contrast, for the bulk MOS device, this α-particle induced current may flow to the active region. As a result, the operation of the bulk MOS device is seriously affected. Therefore, compared to the conventional bulk MOS devices, the SOI MOS devices are more suitable for operation in the environment with high energy radiation. Hence, at the beginning, the applications of the SOI technology are toward space or military oriented purposes.

In addition to the radiation hard property, owing to the buried oxide layer, the parasitic capacitances of SOI MOS devices are smaller than those of bulk ones. Fig. 1.3 shows the comparison of the parasitic capacitances between bulk and SOI CMOS devices and the multiplication time of a 16bit x 16bit multiplier circuit built on a 0.6μm CMOS gate array in bulk and SOI technologies[4]. As shown in the figure, except the gate-related delay, other delays of the multiplier circuit due to the junction capacitances and the wiring capacitances of the SOI CMOS have been improved substantially as compared to the bulk CMOS. As a result, the speed of the multiplier circuit using the SOI CMOS technology has been enhanced. This is

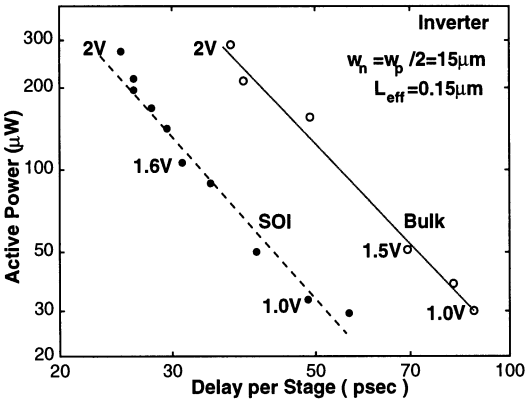


Figure 1.4: Power versus delay of the inverter circuit using 0.15μm bulk and SOI CMOS devices.

why the SOI CMOS technology has been receiving lots of attention.

Fig. 1.4 shows the power versus delay characteristics of the CMOS inverter circuit using SOI and bulk CMOS devices with a channel length of 0.15μm[5]. The channel width of the devices used in the inverter is 15μm for the NMOS and 30μm for the PMOS. Various power supply voltages have been used. From this figure, owing to smaller parasitic capacitances in the SOI MOS devices, the power-delay product of the SOI inverter circuit is much smaller as compared to the bulk one. From this figure, SOI CMOS technology has high-speed and low-power properties.

For SOI CMOS devices, buried oxide has been used for isolation. For bulk CMOS devices, between devices and between device and substrate, depletion regions of the reverse-biased pn-junction have been used for isolation. Therefore, device density of the bulk CMOS technology cannot be high. As shown in Fig. 1.5, for a deep-submicron down-scaled bulk CMOS technology based on n-well or p-well, the increased substrate doping density may degrade the device performance. In addition, the parasitic npn and pnp BJTs in the well and the substrate may be accidentally turned on to cause latch-up. In contrast, in the SOI technology, owing to the buried oxide isolation, no latch-up exists. In addition, device isolation is much simpler for

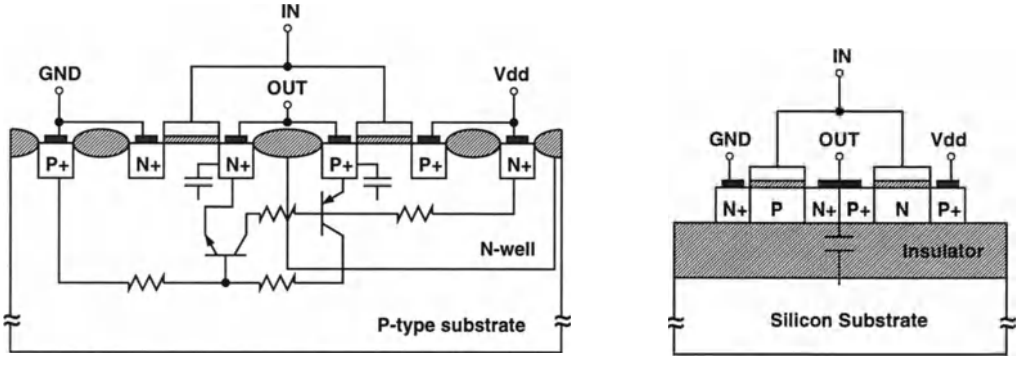


Figure 1.5: Cross section of bulk and SOI CMOS devices.

the SOI CMOS technology. Therefore, from processing point of view, SOI CMOS technology has a higher device density and an easier device isolation structure.

Owing to the superior properties, in addition to space and military applications, SOI CMOS technology has been gradually recognized as another major VLSI technology. Fig. 1.6 shows the technologies for high-speed digital circuits[7]-[13]. As shown in the figure, in addition to VLSI applications, SOI technology has also been used to realize communication circuits, microwave devices, BiCMOS devices, and even fiber optics applications for its superior performance.

Recently, due to the rapid progress in VLSI, CMOS devices have been scaled down continuously and the size of the CMOS circuits has been expanding. In addition, meeting the needs in the portable systems, low-voltage and low-power designs have become indispensable. In this aspect, SOI technology is suitable for integration of the low-voltage and low-power VLSI circuits. Fig. 1.7 shows the scaling of CMOS threshold voltages [14]. For down scaling CMOS devices and for reducing power consumption, power supply voltage for a VLSI circuit has been shrunk. In order to maintain the driving current at a certain level, the threshold voltage of the CMOS devices should also be scaled down. For bulk CMOS devices, since the

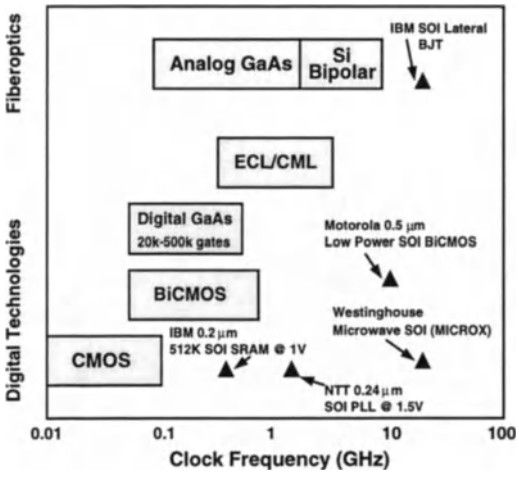


Figure 1.6: Technologies for high-speed digital circuits.

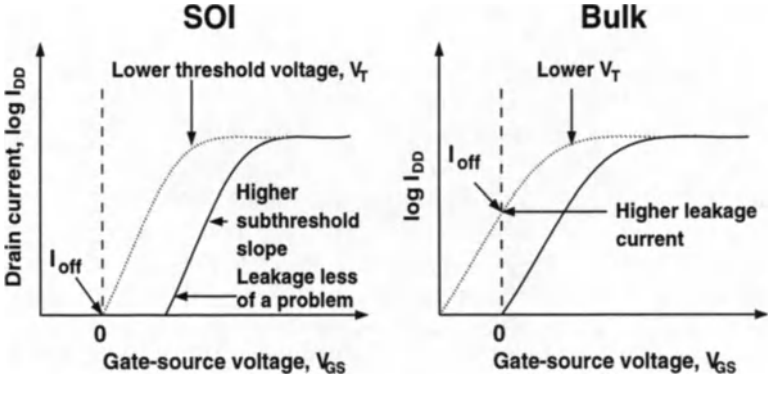


Figure 1.7: Scaling of CMOS threshold voltages: bulk versus SOI.

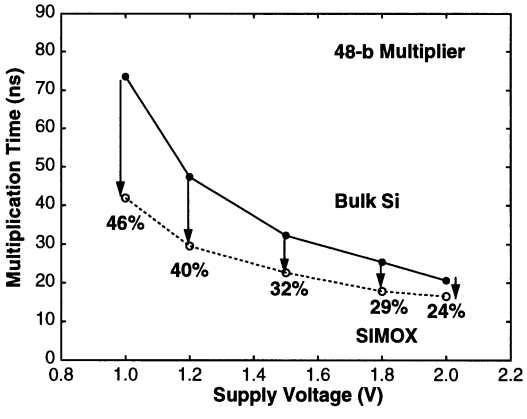


Figure 1.8: Multiplication time versus supply voltage of a 48-bit multiplier circuit using bulk and SOI CMOS technologies.

subthreshold slope is not steep enough, a reduction in the threshold voltage may cause an increase in the leakage current. As a result, standby power consumption is increased. On the other hand, for SOI CMOS devices, their subthreshold slope is steeper. Hence, their threshold voltage can be scaled down more easily. Under an identical situation, their leakage current is much smaller as compared to the bulk CMOS devices. Therefore, SOI CMOS devices are more suitable to be scaled down in deep-submicron VLSI technology for low-voltage low-power system applications.

Recently, many semiconductor companies have been devoted to development of SOI CMOS VLSI circuits. Table 1.1 shows the SOI circuits recently published[15]. As listed in the table, SOI CMOS technology has been used to realize low-voltage low-power high-speed VLSI circuits from portable communication electronics, to gate array, DRAM, SRAM, and other system circuits. Fig. 1.8 shows the multiplication time versus supply voltage of a 48-bit multiplier circuit using bulk and SOI CMOS technologies[15]. As shown in the figure, at an identical off leakage current, the SOI multiplier circuit is faster. In addition, when the power supply voltage is scaled down, the advantage of the SOI circuit is even more noticeable.

Generally speaking, manufacturing cost of the SOI wafer is more expensive than

Circuits	Gate Length	Speed	Supply	Company	Conference
Portable					
Prescaler	0.4μm	2GHz	2V	NTT	92 VLSI
PLL	0.24μm	2.2GHz	1.5V	NTT	93IEDM
μcontroller	0.5μm	5.7MHz	0.9V	Motorola	95IEDM
Communication					
I/O	0.25μm	2.5GHz	2V	NTT	96ISSCC
4:1 MUX	0.25μm	2.98GHz	2.2V	NTT	96ISSCC
8x8ATM sw	0.25μm	40Gb/s	2V	NTT	97ISSCC
Gate Array					
16KG	0.6μm	11.4ns	3V	Mitsubishi	91IEDM
300KG	0.25μm	70MHz	2V	NTT	96ISSCC
220KG	0.35μm	2.5ns	2V	Mitsubishi	97VLSI
250KG	0.25μm	18MHz	0.5V	NTT	97ASIC
SRAM					
512Kb	0.2μm	3.5ns	1V	IBM	93IEDM
DRAM					
16Mb	0.6 – 0.7μm	50ns	3V	Samsung	95VLSI
16Mb	0.5μm	46ns	1V	Mitsubishi	97ISSCC
Others					
ALU	0.25μm	40MHz	0.5V	NTT	96ISSCC
16x16multiplier	0.4μm	18ns	0.5V	Toshiba	96ISSCC
ALU	0.3μm	200MHz	0.5V	Toshiba	97ISSCC

Table 1.1: SOI circuits.

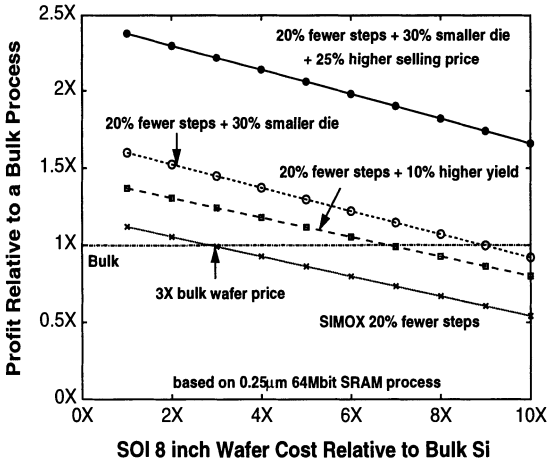


Figure 1.9: Profit factor versus 8-in wafer cost factor for SOI relative to bulk.

that of the bulk one, which is a bottleneck for development. Fig. 1.9 shows the profit factor versus 8-in wafer cost factor for SOI relative to bulk[16]. As shown in the figure, although the wafer cost is more expensive, due to fewer steps and fewer masks needed in the SOI CMOS technology and due to a higher integration density, a smaller die area and a better performance, SOI CMOS technology can produce more profits. Therefore, in the future commercial VLSI circuits, the potentials of SOI CMOS technology are yet to be utilized.

Along with development of new techniques, the cost of the SOI wafers is continuously falling. Fig. 1.10 shows the trend on the SOI wafer production[17]. Due to the continuously growing demands on low-voltage low-power high-performance VLSI wafers, the demands for the SOI wafers are continuously growing. Therefore, the potentials of the SOI CMOS technology are high.

1.2 Objectives

Fig. 1.11 shows three key factors in engineering SOI CMOS VLSI. Processing technology, device modeling, and circuit designs are comparably important. Mutual impacts among three factors are important in developing a creative SOI CMOS

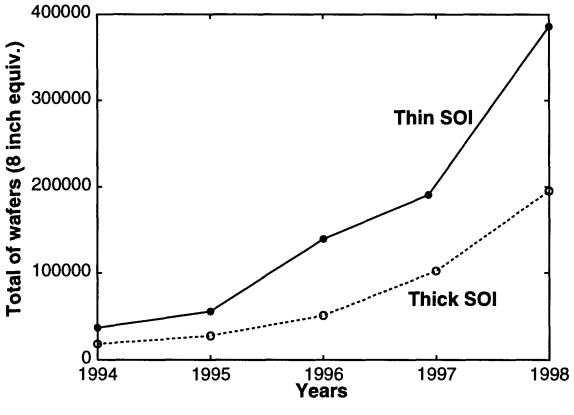


Figure 1.10: Trend on SOI wafer production.

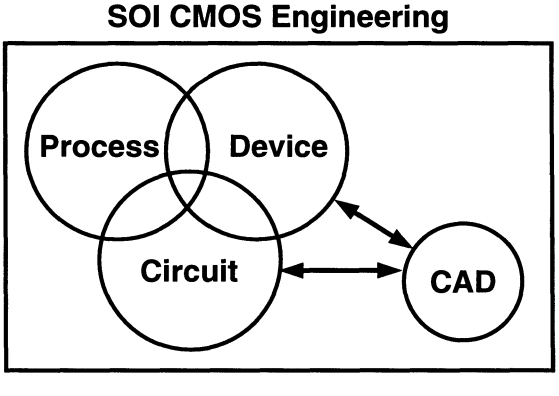


Figure 1.11: Three key factors in engineering SOI CMOS VLSI.

VLSI technology. Improvement in the processing technology and understanding of device behaviors lead to progresses in the SOI circuit designs. The requirements for low-voltage low-power high-performance SOI circuits in the world-wide market serve as an incentive to further evolve processing technology. Understanding of device behaviors can provide new ideas for development of next-generation SOI CMOS technology. In addition, developed device models can provide CAD tools for circuit simulation. In this book, most of the three key factors in engineering SOI CMOS VLSI will be covered. Starting from SOI CMOS processing technology and SOI CMOS VLSI circuits, device behaviors of the SOI CMOS devices are presented in the following chapters. In addition, a SPICE program—ST-SPICE, which incorporates device models for deep-submicron fully-depleted mesa-isolated SOI CMOS devices, is described.

References

[1] J.-P. Colinge, "Silicon-on-Insulator Technology: Materials to VLSI, 2nd ed." *Kluwer Academic: Boston*, 1997.

[2] M. Yoshimi, M. Takahashi, S. Kambayashi, M. Kemmochi, H. Hazama, T. Wada, K. Kato, H. Tango, and K. Natori, "Electrical Properties and Technological Perspectives of Thin-Film SOI MOSFETs," *IEICE Trans. Elec.*, Vol. 74, No. 2, pp. 337-351, Feb. 1991.

[3] S. Kawamura, "Ultra-Thin-Film SOI Technology and Its Application to Next Generation CMOS Devices," *SOI Conf. Dig.*, pp. 6-7, 1993.

[4] Y. Inoue and Y. Yamaguchi, "Trends in Research and Development of SOI Technology," *Applied Physics*, Vol. 64, No. 11, pp. 1104-1110, 1995 (in Japanese).

[5] B. Davari, R. H. Dennard, and G. G. Shahidi, "CMOS Scaling for High Performance and Low Power—The Next Ten Years," *IEEE Proc.*, Vol. 83, No. 4, pp. 595-606, Apr. 1995.

[6] S. Cristoloveanu and S. Li, "Electrical Characterization of Silicon-on-Insulator Materials and Devices," *Kluwer Academic: Boston*, 1995.

[7] S. Ohr, "GaAs Finds Home in Wireless & High-Speed Data-Communications Applications," *Computer Design*, pp. 59-68, March 1994.

[8] G. G. Shahidi, T. H. Ning, T. I. Chappell, J. H. Comfort, B. A. Chappell, R. Franch, C. J. Anderson, P. W. Cook, S. E. Schuster, M. G. Rosenfield, M. R. Polcari, R. H. Dennard, and B. Davari, "SOI for a 1-Volt CMOS Technology and Application to a 512Kb SRAM with 3.5ns Access Time," *IEDM Dig.*, pp. 813-816, 1993.

[9] Y. Kado, T. Ohno, M. Harada, K. Deguchi and T. Tsuchiya, "Enhanced Performance of Multi-GHz PLL LSIs Using Sub-1/4-Micron Gate Ultrathin Film CMOS/SIMOX Technology with Synchrotron X-Ray Lithography," *IEDM Dig.*, pp. 243-246, 1993.

[10] M. H. Hanes, A. K. Agarwal, T. W. O'Keeffe, H. M. Hobgood, J. R. Szedon, T. J. Smith, R. R. Siergiej, P. G. McMullin, H. C. Nathanson, M. C. Driver, and R. N. Thomas, "MICROX^{TM}— An All-Silicon Technology for Monolithic Microwave Integrated Circuits," *IEEE Elec. Dev. Let.*, Vol. 14, No. 5, pp. 219-221, May 1993.

[11] R. Dekker, W. T. A. v.d. Einden, and H. G. R. Maas, "An Ultra Low Power Lateral Bipolar Polysilicon Emitter Technology on SOI," *IEDM Dig.*, pp. 75-78, 1993.

[12] W. M. Huang, K. Klein, M. Grimaldi, M. Racanelli, S. Ramaswami, J. Tsao, J. Foerstner, and B. Y. Hwang, "TFSOI BiCMOS Technology for Low Power Applications," *IEDM Dig.*, pp. 449-452, 1993.

[13] G. G. Shahidi, D. D. Tang, B. Davari, Y. Taur, P. McFarland, K. Jenkins, D. Danner, M. Rodriguez, A. Megdanis, E. Petrillo, M. Polcari and T. H. Ning, "A Novel High-Performance Lateral Bipolar on SOI," *IEDM Dig.*, pp. 663-666, 1991.

[14] M. L. Alles, "Thin-Film SOI Emerges," *IEEE Spectrum*, pp. 37-45, June 1997.

[15] T. Tsuchiya, "Prospect of SOI Devices," *Applied Physics*, Vol. 66, No. 11, pp. 1191-1198, 1997 (in Japanese).

[16] T. Stanley, "Semiconductor Wafer Bonding: Science, Technology and Applications," *Elec. Chem. Soc. Proc.*, Vol. 93-29, p. 303, 1993.

[17] A. J. Auberton-Herve, "SOI: Materials to Systems," *IEDM Dig.*, pp. 3-10, 1996.

Chapter 2

SOI CMOS Technology

In this chapter, SOI CMOS technology is described. Starting from the evolution of SOI technology, various SOI substrate and isolation techniques are introduced. Then, a 0.25μm SOI CMOS fabrication processing sequence is described, followed by major SOI CMOS device structures. In the final portion of this chapter, special-purpose SOI technologies including DRAM, BiCMOS, and power are described.

2.1 Evolution of SOI

Table 2.1 shows the evolution of the mainstream SOI technology. As shown in the table, the CMOS industry began to be interested in the SOI technology in late 1970s. Initially, it was based on silicon-on-sapphire (SOS) wafers[1]. Since early 1980s, SOS technology has been replaced by SIMOX (separation by implantation of oxygen) and ZMR (zone-melting-and-recrystallization) SOI technologies [2]-[5]. Owing to the progress in bond-and-etch-back SOI (BESOI), ZMR SOI technology has been replaced[6][7]. As a result, SIMOX and BESOI have become the mainstream SOI technologies. SIMOX technology is suitable for realizing ultra-thin SOI devices. However, the quality of the silicon thin-film is inferior. In contrast, the quality of the silicon thin-film in BESOI technology is better but uniformity control of the thin-film is inferior. Therefore, SIMOX and BESOI technologies have their own strengths[9]. Recently, smart-cut SOI technology has emerged[10]. In the following sections, each of the major SOI technologies is described one by one in details.

J. B. Kuo et al., *CMOS VLSI Engineering*

Evolution of the mainstream SOI Technology.

Year	First Author	Technique
1978	Maurits[1]	SOS (silicon-on-sapphire)
1983	Lam[2]	SIMOX (separation by implantation of oxygen) SOI ZMR (zone-melting-and-recrystallization) SOI
1986	Partridge[3]	SOS, SIMOX, ZMR SOI
1989	Colinge[4]	SIMOX, ZMR SOI, BESOI (bond-and-etch-back SOI)
1990	Auberton-Herve[5]	SIMOX, ZMR SOI, BESOI
1991	Vogt[6]	SIMOX, BESOI, ZMR SOI
1991	Colinge[7]	SIMOX, BESOI
1993	Feijoo[8]	SIMOX, BESOI
1993	Kawamura[9]	SIMOX, BESOI
1996	Auberton-Herve[10]	SIMOX, BESOI, Smart-Cut SOI

Table 2.1: Evolution of the mainstream SOI Technology.

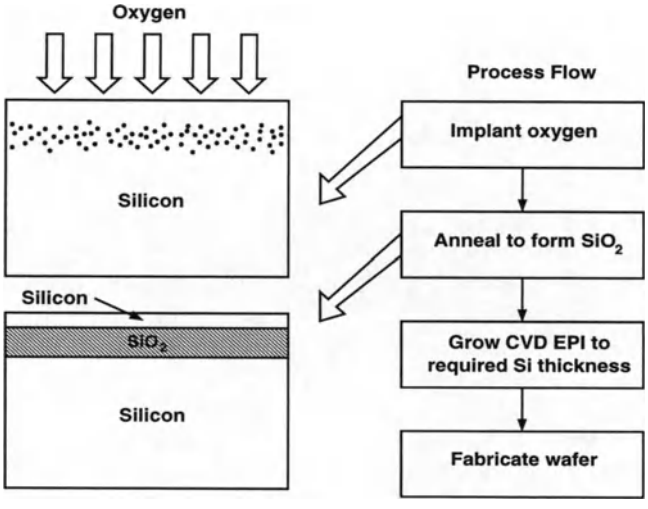


Figure 2.1: Basic steps of implant, anneal, and epitaxial silicon deposition in SIMOX wafer fabrication.

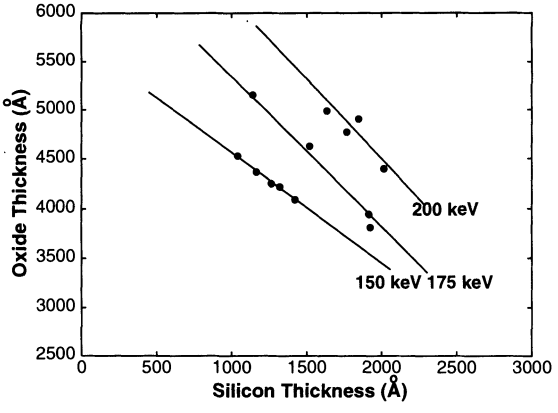


Figure 2.2: Buried oxide thickness versus the superficial silicon thickness for SIMOX produced at implant energies of 150keV, 175keV, and 200keV and oxygen doses of $1 - 2 \times 10^{18}\text{cm}^{-2}$.

2.2 SIMOX SOI Substrate

Implanted buried oxide layers for SOI were initially discussed in the late 1960s. Intensive work on Separation by Implantation of Oxygen (SIMOX) technology was begun in early 1980s. Fig. 2.1 shows the basic steps of implant, anneal, and epitaxial silicon deposition in SIMOX wafer fabrication[11]. As shown in the figure, first, oxygen is implanted into the silicon wafer. The profile of the implanted oxygen dopants is Gaussian-shape with its peak at some distance below the surface. Then, with a high-temperature anneal, the oxygen dopants react with silicon to form a buried oxide layer around the peak of the oxygen profile. During the high-temperature anneal, the oxygen dopants above the buried oxide move to gather at the peak region, thus react with silicon to form silicon dioxide. As a result, a single-crystal silicon thin-film above the buried oxide layer can be formed. If necessary, the thickness of the single-crystal silicon thin-film can be increased by epitaxy. Fig. 2.2 shows the buried oxide thickness versus the superficial silicon thin-film thickness for SIMOX produced at implant energies of 150keV, 175keV, and 200keV and oxygen doses of $1-2\times10^{18}\text{cm}^{-2}$[11]. As shown in the figure, when the buried oxide produced by the SIMOX technology becomes thicker, the top single-crystal silicon thin-film becomes thinner. The thickness of the top single-crystal silicon thin-film is related to the energy of the oxygen implant. A higher energy leads to a deeper distribution of the oxygen dopants. As a result, the buried oxide layer is formed at a deeper loca-

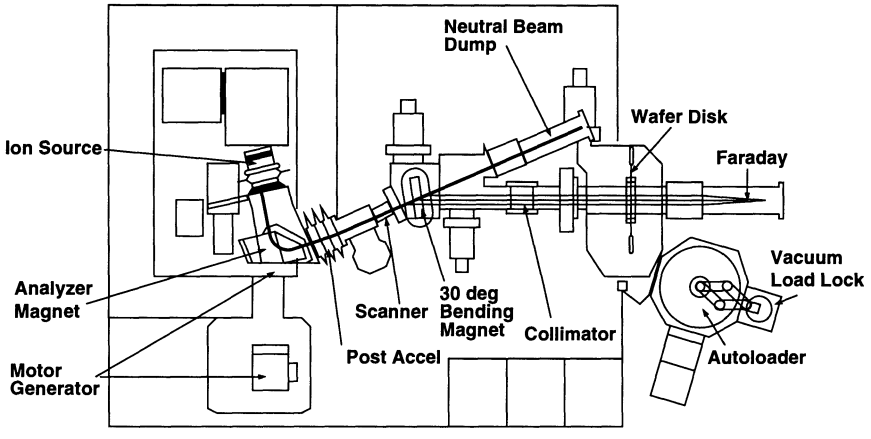


Figure 2.3: Schematic illustration of an oxygen implanter.

tion from the surface. Consequently, the thickness of the silicon thin-film becomes greater.

Fig. 2.3 shows the schematic illustration of an oxygen implanter[12]. The O^+ ions, which are excited from the ion source, travel through the analyzer magnet. During this time, the unwanted molecular ion beam is dissipated. Then, the O^+ ions are accelerated by the post accelerator. After passing through the scanner and the bending magnet, the O^+ ions hit the target wafer, which is heated to 600C to suppress the generation of defects in the top silicon layers and to prevent silicon sublimation at the surface[14].

Fig. 2.4 shows Auger spectroscopy of an oxygen-ion-implanted silicon substrate[13]. The oxygen implant is at an energy of 150keV and a dose of $1.2 \times 10^{18}\text{cm}^{-2}$. After the oxygen implant, the wafer is annealed in the N_2 environment at 1150C for two hours. As shown in the figure, the distribution of the oxygen dopants is below the surface at a certain depth in the wafer. In addition, after the anneal procedure, the oxygen dopants react with silicon to form silicon dioxide.

Fig. 2.5 shows the breakdown electric field of the buried oxide versus the dose of the oxygen implant[14] in a SIMOX process. The oxygen ions were implanted at 180keV and 550C. Subsequent anneal was performed at 1350C for 4 hours. The breakdown field was calculated by dividing the breakdown voltage by the mean

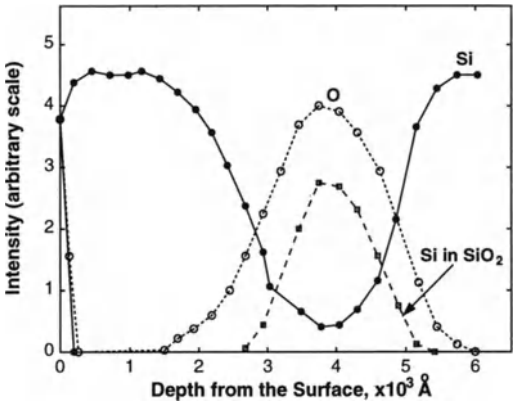


Figure 2.4: Auger spectroscopy of an oxygen-ion-implanted silicon substrate.

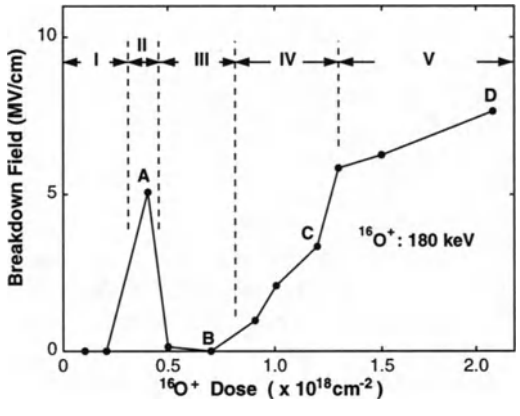


Figure 2.5: Breakdown electric field of the buried oxide versus the dose of the oxygen implant.

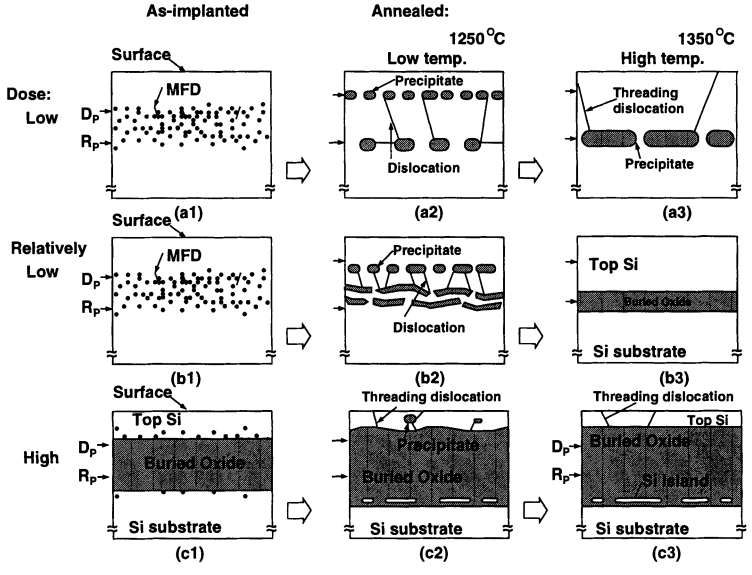


Figure 2.6: Schematic diagram illustrating the cross-sectional view of SIMOX wafers to explain the dose dependence of threading dislocation generation.

value of the buried oxide thickness, which was estimated from an XTEM observation. The doses identified by A, B, C, and D are 0.4, 0.7, 1.2, and 2.0 $\times$ $10^{18}cm^{-2}$, respectively. As shown in the figure, the dose of the oxygen implant affects not only the thickness of the buried oxide but also the quality of the buried oxide. In Region I, since no continuous buried oxide layer is formed yet, the breakdown field is 0MV/cm. In Region II, some improvement in the breakdown electric field can be seen. However, as compared to the thermal oxide, the breakdown electric field is still inferior due to the wavy interface. In Region III, due to high-density silicon pipes, the breakdown electric field becomes 0 again. After Region IV, when the dose of the oxygen implant increases, the quality of the buried oxide layer increases. In Region IV, many silicon-islands are present, hence the breakdown electric field is still not good enough. In Region V, silicon-islands almost disappear. Instead, they are present at the bottom of the buried oxide layer. Therefore, the breakdown electric field is the highest. From this figure, Region II provides a dose window often used for the low-dose implant, which offers low-cost, high through-put production. In addition, using the low-dose implant, the buried-oxide layer is thinner, which improves the self-heating of the device and the short-channel effects. Fig. 2.6

shows the schematic diagram illustrating the cross-sectional view of SIMOX wafers to explain the dose dependence of threading dislocation generation[14]. The doses of the oxygen implants in (a), (b), and (c) are $0.2 \times 10^{18}\text{cm}^{-2}$, $0.4 \times 10^{18}\text{cm}^{-2}$, and $2 \times 10^{18}\text{cm}^{-2}$, respectively. At a low dose of $0.2 \times 10^{18}\text{cm}^{-2}$ (a), the implanted oxygen ions are distributed at depths between D_p and R_p. After a low-temperature anneal at 1250C, oxide precipitates begin to form at a depth between D_p and R_p. Since at each depth, these oxide precipitates are still not continuous, a large stress leads to dislocations. After the high-temperature anneal, the oxide at the depth D_p disappears and the oxygen dopants follow the dislocation path to join the precipitates at the depth R_p to form larger buried oxide layer regions. At this time, the buried oxide regions are not continuous. Therefore, there exists a larger stress, which results in threading dislocations. With a relatively higher dose (b), the situation is similar to (a). However, due to a higher dose, the buried oxide structure is more solid with the threading dislocations. With a high dose (c), before anneal, a buried oxide layer is already formed. Under a low-temperature anneal, below and above the buried oxide layer, there exist oxide precipitates. The bottom precipitates are connected to the buried oxide layer. Therefore, silicon-islands are formed. The number of the precipitates above the buried oxide layer is much smaller. Hence, in the silicon thin-film, there are threading dislocations to the surface. After a high-temperature anneal at 1350C, the threading dislocations still exist. Note that precipitates can prevent dislocations from spreading to surface. MFD is multiple faulted defects, which exist in the silicon wafer before the process.

Fig. 2.7 shows the formation mechanisms of the threading dislocation [15]. When the high-temperature anneal starts, buried oxide is gradually formed. The excess silicon interstitials migrate toward surface to form the new epi-layer. If the anneal process is too fast, silicon atoms are easily accumulated in the location with an uneven stress. As a result, a large amount of precipitates with irregular crystal structures are formed. In addition, these precipitates grow continuously with the threading dislocations throughout the silicon thin-film. The threading dislocations affect the quality of the thin-film. The threading dislocations can be reduced by improving the annealing process. Fig. 2.8 shows the schematic diagram of an improved annealing sequence [15] to reduce dislocations. As shown in the figure, the ramp-up period from 1050C to 1300C in the annealing sequence has been intentionally lengthen to suppress the accumulation of the excess amount of the silicon interstitials for forming dislocations.

Fig. 2.9 shows the microstructure evolution of low-dose SIMOX wafers during a high-temperature anneal[16]. As shown in the figure, during the annealing pro-

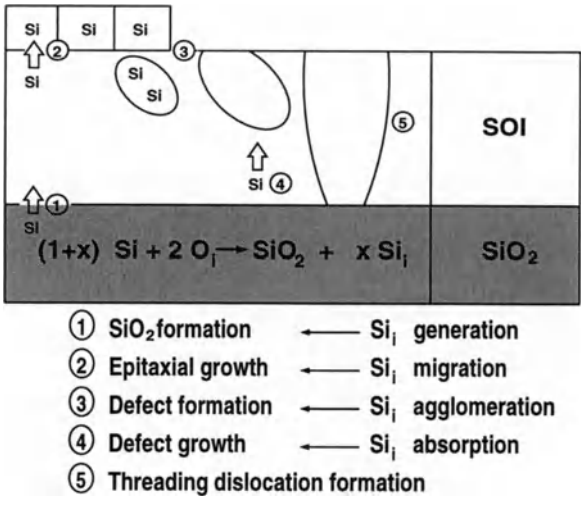


Figure 2.7: Formation mechanisms of the threading dislocation.

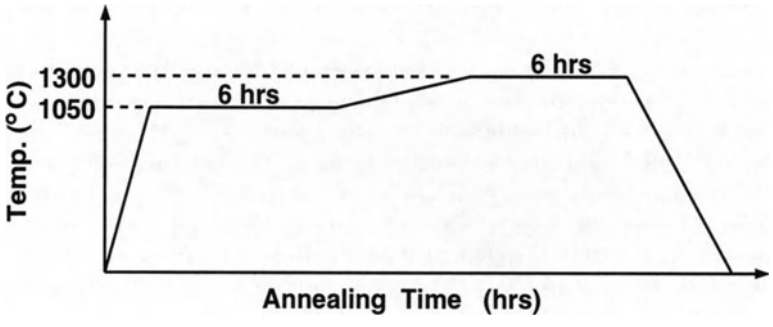


Figure 2.8: Schematic diagram of an improved annealing sequence.

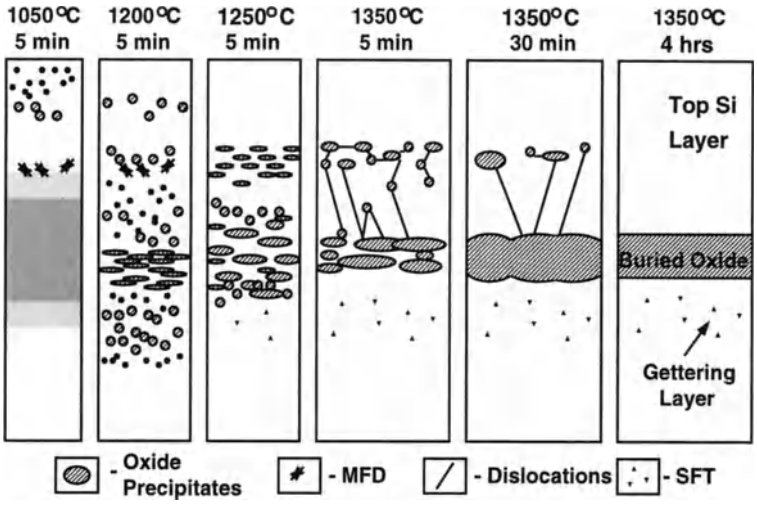


Figure 2.9: The microstructure evolution of low-dose SIMOX wafers during a high-temperature anneal.

cess, due to the multiple faulted defects (MFD) at the top of the buried oxide in the silicon thin-film, large oxide precipitates and dislocations are generated. After the high-temperature anneal, these precipitates dissolve and move along the path of dislocations to join the buried oxide layer. As a result, not many vacancies are produced. In contrast, the situation under the buried oxide is different, where no multiple faulted defects exist. Therefore, most of the oxide precipitates under the buried oxide are small. During the high-temperature anneal, most of the oxide precipitates dissolve quickly, thus a large quantity of vacancies—stacking faults are generated. Therefore, for low-dose oxygen-implanted SIMOX wafers, the quality of the silicon thin-film is good. However, below the buried oxide, there are lattice defects in the substrate. The lattice defects beneath the buried oxide also provide advantages—impurity gettering. Fig. 2.10 shows the schematic representation of the gettering option for SIMOX wafers at lattice defects formed inside the thin silicon substrate located just beneath the buried oxide[16]. As shown in the figure, these defects can absorb some heavy-metal atoms at surface such that the quality of the thin-film can be raised.

In order to further improve the quality of the buried oxide and the microroughness of interface, a high-temperature oxidation technique has been used for the

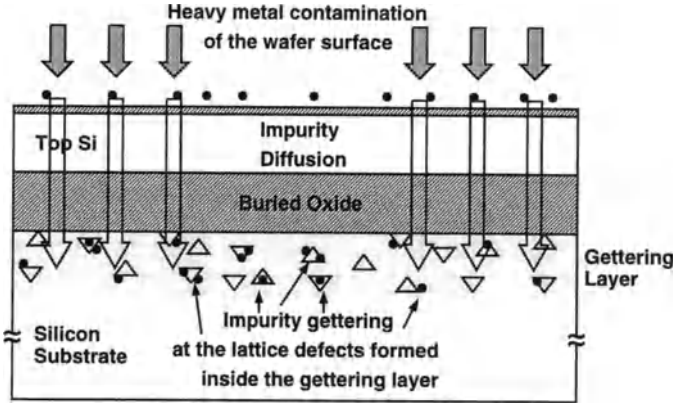


Figure 2.10: Schematic representation of the gettering option for SIMOX wafers at lattice defects formed inside the silicon substrate located just beneath the buried oxide.

SIMOX wafers. Fig. 2.11 shows the thickness of the internal thermal oxide (ITOX) versus the reciprocal of the oxidation temperature in a SIMOX wafer implanted with an oxygen dose of $4 \times 10^{17}\text{cm}^{-2}$ at 180keV[17]. As shown in the figure, after a high temperature oxidation, thermal oxide is grown at the surface. In addition, some oxygen atoms diffuse to the interface between the silicon thin-film and the buried-oxide, where reaction takes place. As a result, buried oxide thickens with an improved quality. Besides, the microroughness of interface has been improved. As shown in the figure, at a higher oxidation temperature, the oxygen atoms diffuse to the interface between the silicon thin-film and the buried oxide more easily. Therefore, its internal thermal oxide becomes thicker.

As for general silicon wafers, the surface roughness of SIMOX wafers can be improved by the hydrogen anneal. Fig. 2.12 shows the dependence of roughness on scale for the samples without a hydrogen anneal and with hydrogen anneals at 1000C/30min, 1100/30min, and 1100/2hours[18]. As shown in the figure, with a longer anneal time, the surface roughness improves more.

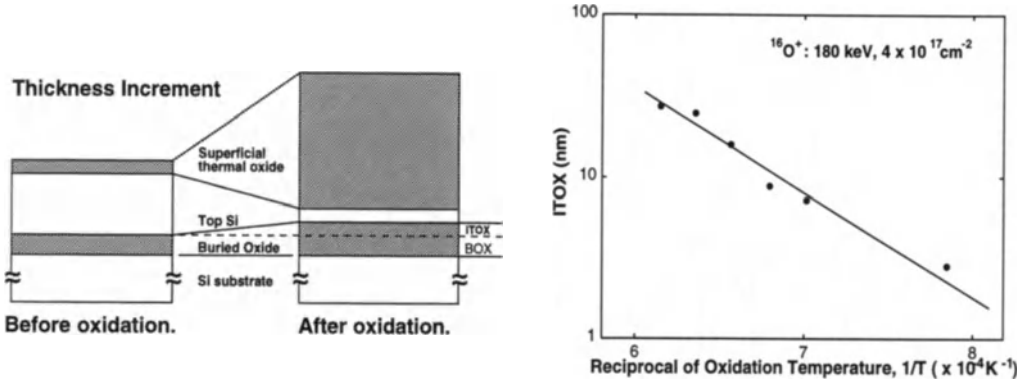


Figure 2.11: Thickness of the internal thermal oxide (ITOX) versus the reciprocal of the oxidation temperature in a SIMOX wafer implanted with an oxygen dose of $4 \times 10^{17}\text{cm}^{-2}$ at 180keV.

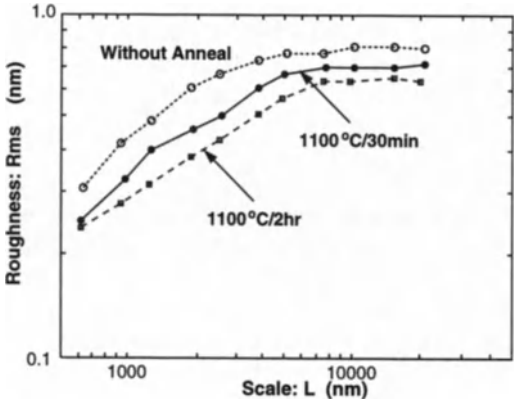


Figure 2.12: Dependence of roughness on scale for the samples without a hydrogen anneal and with hydrogen anneals at 1100/30min, and 1100/2hours.

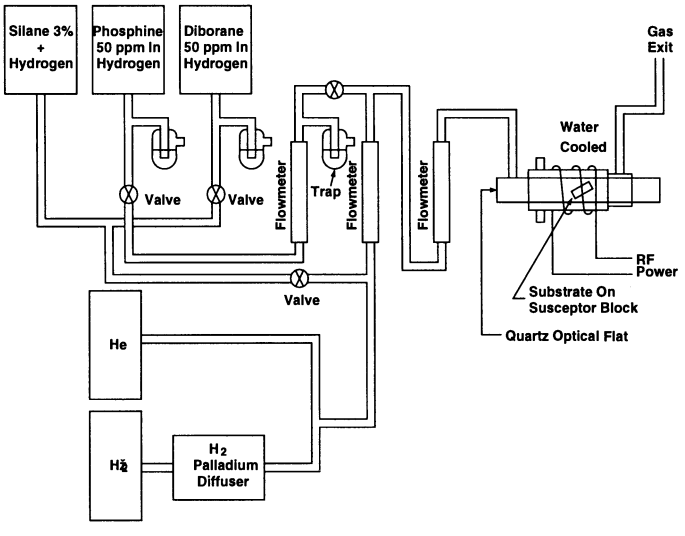


Figure 2.13: The CVD reaction chamber for silicon-on-sapphire deposition.

2.3 Other SOI Substrates

In the previous section, SIMOX technology has been described. In addition to SIMOX technology, there are several other technologies available for SOI. In this section, silicon-on-sapphire (SOS), zone-melting-recrystallization (ZMR SOI), bond-and-etch-back (BESOI), and smart-cut technologies are described.

2.3.1 SOS Substrate

The deposition of single crystal layers of silicon onto sapphire surfaces is called SOS technology. In preparing SOS substrate, single crystal sapphire substrates are cut approximately 60 degrees to the c axis and then polished carefully and ultrasonically cleaned in chloroform before being placed in the growth apparatus. As shown in Fig. 2.13, single crystal sapphire substrates are placed in the chemical vapor deposition (CVD) chamber, which is flushed with hydrogen, and heated to 1050-1200C by an RF generator. After thermal equilibrium has been established, the silane (SiH_4) flow is started for the silicon deposition process[19]. After the designated thickness of the silicon thin-film has been obtained, the silane flow is stopped. Then, the wafers are slowly cooled in hydrogen such that annealing and crystallization can be taken place. The quality of the silicon thin-film near sapphire

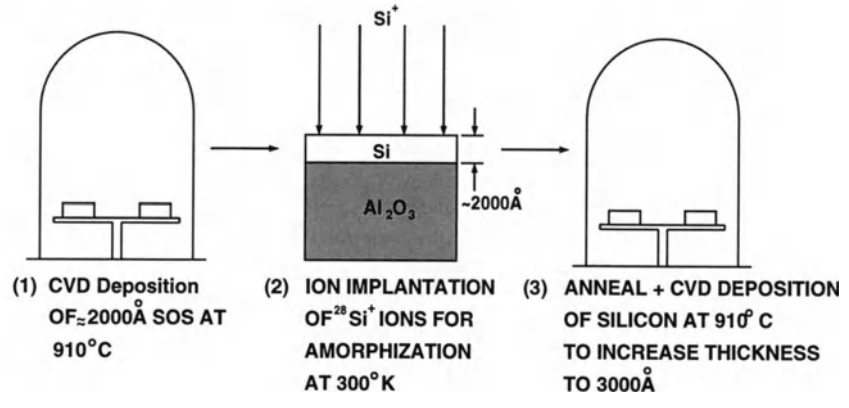


Figure 2.14: Solid phase epitaxy and regrowth (SPEAR) recrystallization process.

in the epitaxial SOS wafers may not be good, which can be improved by solid phase epitaxy and regrowth (SPEAR) technique as shown in Fig. 2.14 [20]. As shown in the figure, the starting SOS material has a 0.2μm silicon thin-film grown using silane. Silicon is implanted into the SOS wafers at an energy such that the surface crystal structure of the silicon thin-film is not seriously damaged. Due to the silicon implant, at the bottom of the silicon thin-film near the sapphire, the silicon has been damaged to become amorphous. At a high-temperature anneal at 910C, using the top single-crystal silicon thin-film as the seed, the bottom amorphous silicon layer is recrystallized. Thus, the whole silicon thin-film is recovered to be single-crystal silicon. This technique is called solid phase epitaxy (SPE). During SPE process, CVD can be taken place simultaneously such that the thickness of the single-crystal silicon thin-film can reach the designated value.

2.3.2 ZMR SOI Substrate

Fig. 2.15 shows the cross section of a typical zone-melting-and-recrystallization (ZMR) starting wafer and the process showing a wafer being scanned across by a wire heater, which sits on a heated lower platen[21]. A thermal oxide layer of 1μm is grown on the top of the wafer as the buried oxide. Then the thermal oxide at the edge of the wafer is etched off such that silicon is exposed as the seed during recrystallization. A layer of the polysilicon of $0.75 - 3\mu$m is deposited by LPCVD (low-pressure CVD). Then another layer of oxide, which is deposited by low-temperature CVD, is used as the capping oxide to isolate the wafer from contamination. In addition, this capping oxide layer can be used to reduce the thickness

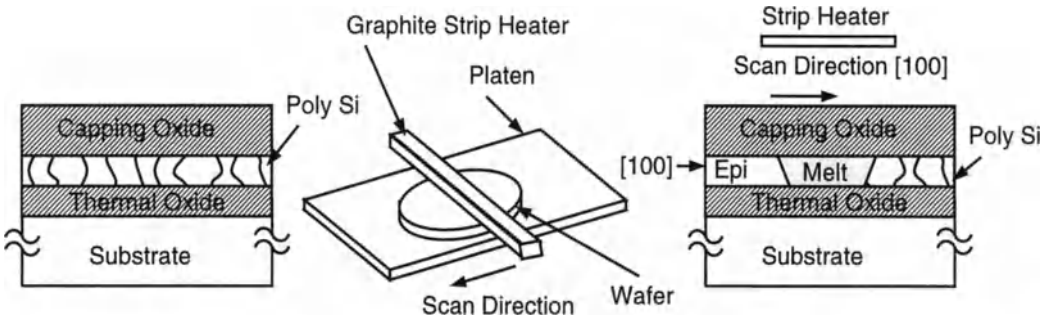


Figure 2.15: Cross section of a typical zone-melting-and-recrystallization(ZMR) starting wafer and the process showing a wafer being scanned across by a wire heater, which sits on a heated lower platen.

variation of the single-crystal silicon thin-film after zone-melting recrystallization. Then, the wafer is heated to 1200C. At an appropriate distance from the top of the wafer, a 2200 C graphite stripe heater is used to scan the wafer back and forth at a moving speed of $0.1 - 1.1$mm/sec. As shown in the figure, the polysilicon layer under the graphite stripe heater is melted. When the heater moves away, this portion of the polysilicon layer is cooled down to be recrystallized to become single-crystal silicon thin-film. Since the scan of the graphite heater is started from the edge of the wafer, the exposed silicon substrate functions as the seed during the recrystallization process.

In addition to the graphite stripe heater, arc lamp can also be used as the scanning heater for the zone melting recrystallization process. As shown in Fig. 2.16[22], on the top of the scanning arc lamp heater, an elliptical reflector is added such that the thermal energy can be concentrated on the surface of the wafer for the zone melting recrystallization process. Fig. 2.17 shows the schematic diagram of the RF-heated micro-zone-melting method[23]. The wafer is moved across the surface of the carbon susceptor, which is heated to a high temperature by the RF coil. Due to the thermal buffer plate between the wafer and the susceptor, the temperature of the wafer is about 1370C. In the portion of the wafer where the thermal buffer plate is open, it is exposed to the heat of the susceptor. As a result, the temperature at this portion of the wafer is 1450C, which is higher than the melting point of the silicon (1412C). Consequently, only the portion of the polysilicon thin-film above

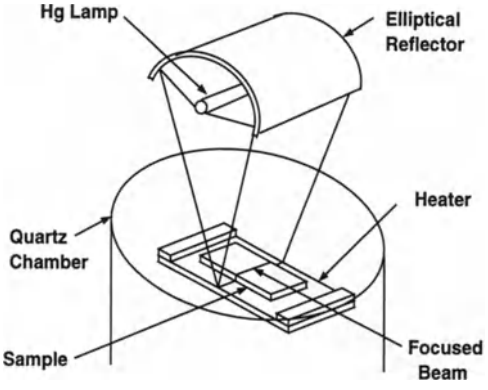


Figure 2.16: Schematic representation of scanning arc lamp system.

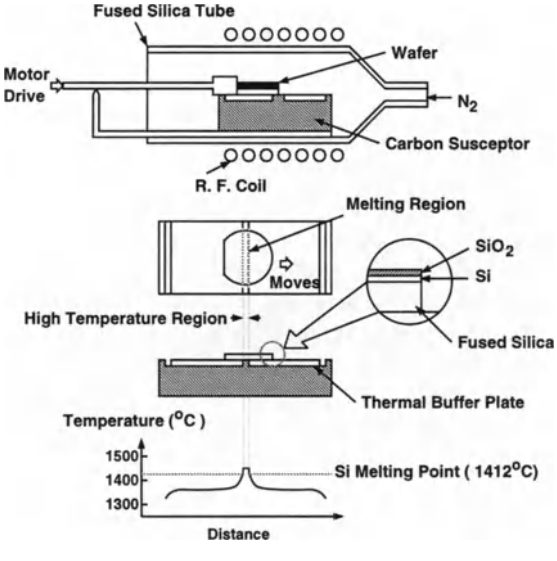


Figure 2.17: Schematic diagram of the RF-heated micro-zone-melting method.

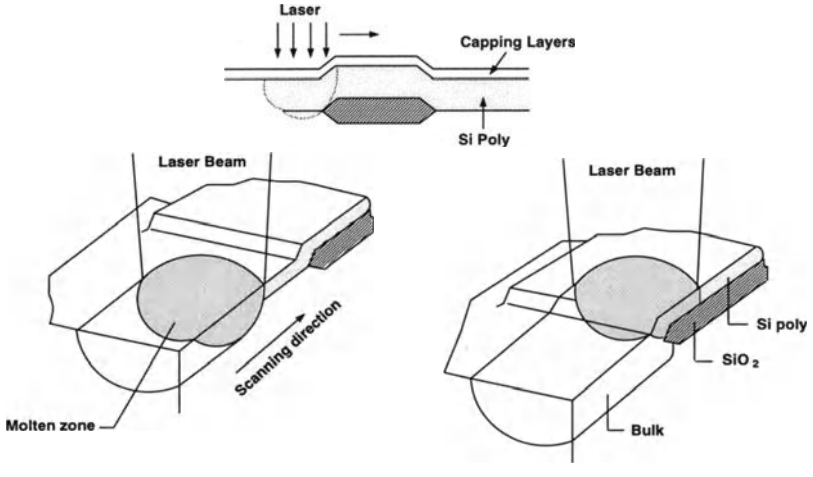


Figure 2.18: Principle of the laser-beam seeding technique for lateral epitaxy.

this opening of the thermal buffer plate is in the melting zone. Other procedures are similar as the one described above.

In addition to the techniques described above, laser and electron beam techniques are also effective heat sources. Fig. 2.18 shows the principle of the laser-beam seeding technique for lateral epitaxy[24]. The wafer is heated by a 9W Ar^+ C-W laser. The laser beam is concentrated on an area of $20 \times 100\mu m^2$ of the wafer, which is heated to 500C. Only at the area exposed to the laser beam, the polysilicon is melted. The scanning speed of the laser beam is 10-30 cm/sec. In addition, the scan of the laser beam starts from the area with an opening in the underlying oxide to the silicon substrate used as the seed during the process.

Zone melting recrystallization technique is especially suitable for 3D integration. Fig. 2.19 shows the stacked CMOS SOI structure using seeding lateral epitaxy technique[25]. When the CMOS devices at the surface of the bulk silicon substrate are accomplished, an oxide layer is added to be used for planarization. A $2\mu m$ opening in the oxide layer is used as the seed area. A polysilicon layer followed by a Si_3N_4 layer and a tungsten of 2000Å is deposited. The heat source is the 12KeV 2mA electron beam, which has an effective exposed area with a radius of $100\mu m$ on the wafer. The electron beam scans the wafer at a speed of 10cm/sec. The purpose of the tungsten layer is used to limit the temperature variations in the wafer

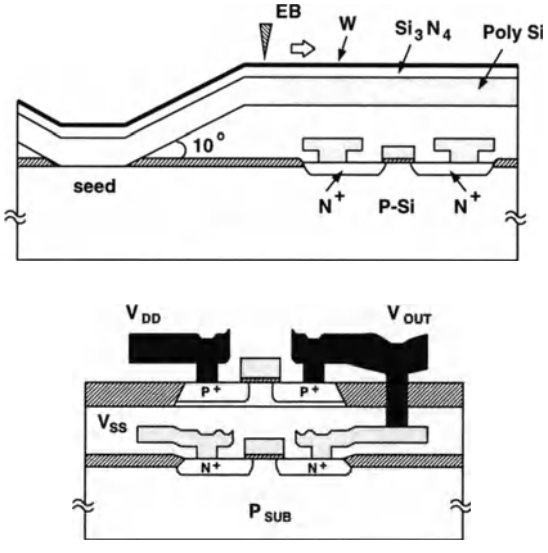


Figure 2.19: Stacked CMOS SOI structure using seeding lateral epitaxy technique.

such that a steady recrystallization process can be obtained— the quality of the single-crystal silicon thin-film can be enhanced. The single-crystal silicon thin-film after zone melting recrystallization can be used to build other devices. As shown in the figure, using this technique, a 3D integration of CMOS devices has been obtained. The top and the bottom layers of the devices are separated by an oxide layer of 0.9μm such that during the zone melting recrystallization process, the doping profile of the bottom layer device is not affected. In addition, the temperature of the fabrication process of the top layer device should be kept under 900C to avoid the influence in the bottom layer. Therefore, LOCOS isolation technique based on thermal oxidation can not be used for the top-layer devices.

2.3.3 BESOI Substrate

Fig. 2.20 shows the fabrication procedure of bond-and-etch-back SOI (BESOI) technology. In the BESOI process, two wafers—the device wafer and the handle wafer are needed. First, a special epitaxial layer is grown on the top of the device wafer, which is used as the etch-stop layer. For various techniques, the contents of this etch-stop layer may be different. Another epitaxial layer is grown for the device thin-film region. Then a thermal oxide layer is grown on both the device wafer

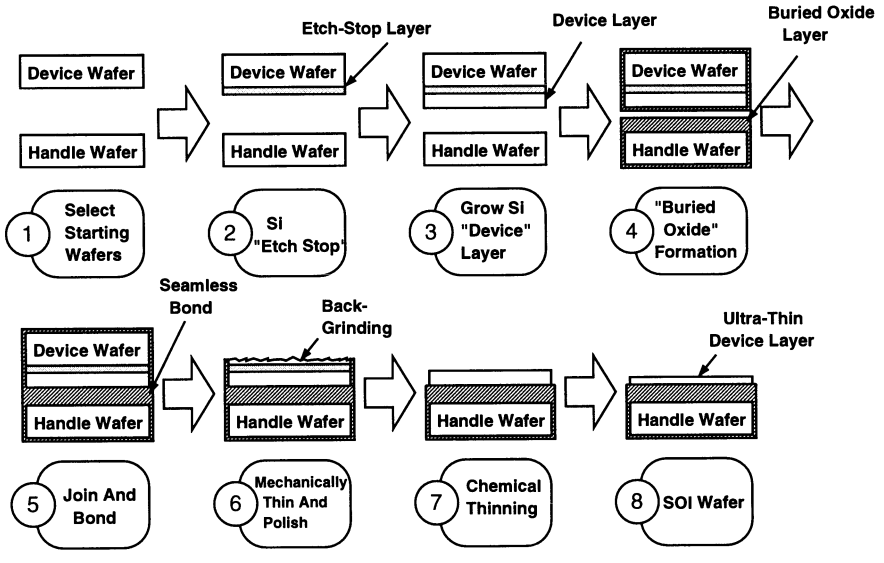


Figure 2.20: The fabrication procedure of bond-and-etch-back (BESOI) technology.

and the handle wafer. The oxide layer on the handle wafer is used as the buried oxide. The device wafer and the handle wafer are bonded together with the device wafer upside down at a raised temperature. The front surface of the device wafer is now in the center portion of the bonded wafer. The back surface of the device wafer is ground until only 10μm left, followed by a high selective etch to remove the remaining silicon on the top of the etch-stop layer. Another highly selective etch is used to remove the etch-stop layer such that only the device thin-film layer is left at the device wafer side. The thickness of the device thin-film layer can be further reduced by thermal oxidation or etch. A hydrogen anneal is used to improve the surface roughness of the wafer.

The mechanism of the bonding in the bond-and-etch-back SOI (BESOI) process is explained here. When two wafers covered with oxide are in close contact with each other in an oxidizing environment at 700C, the oxygen in the two wafers will penetrate through the oxide and react with silicon to form silicon dioxide. As a result, two wafers are connected more firmly. Fig. 2.21 shows the surface of the silicon dioxide prior to bonding, which is composed of Si-OH bonds[26]. When two

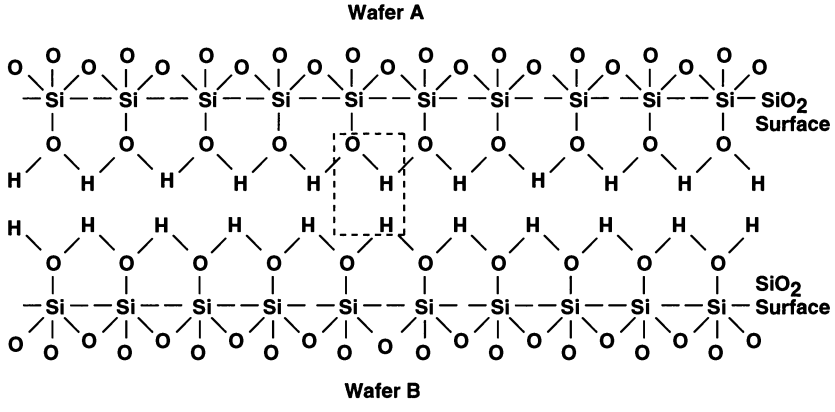


Figure 2.21: Surface of the silicon dioxide prior to bonding. Si-OH bonds on opposing wafer surfaces react to form Si-O-Si.

wafers are in contact, Si-OH reacts with each other to form

$$Si - OH + Si - OH \rightarrow O - Si - O + H_2O.$$

This implies that the previous oxide surface disappears. Instead, the structure has been reorganized to form a siloxane network– a block of oxide. At this step, the bonding procedure has been accomplished. This bonding can be further strengthened by heat.

For the BESOI technology, the key processing step is the etch-stop layer. Fig. 2.22 shows the schematic of the silicon-on-quartz approach using an etch-stop layer[27]. A P^{++} epi-layer followed by a P^- epi-layer is grown on the top of the p-type device wafer. The P^{++} layer is used as the etch-stop layer, while the P^- layer is the thin-film device region. Following the processing procedure described before, this device wafer and the handle wafer are bonded together with the device wafer upside down. The redundant top portion of the silicon layer and the etch-stop layer are etched off by the ethylene diamine pyrocatechol and $HF + HNO_3 + CH_3COOH$, respectively. Since these etches are impurity sensitive, finally only the p^- thin-film device region is left for the subsequent processing procedure.

Fig. 2.23 shows a BESOI wafer fabrication flow diagram with SiGe-layer as the etch-stop layer[28]. The fabrication procedure of this BESOI technology is similar to

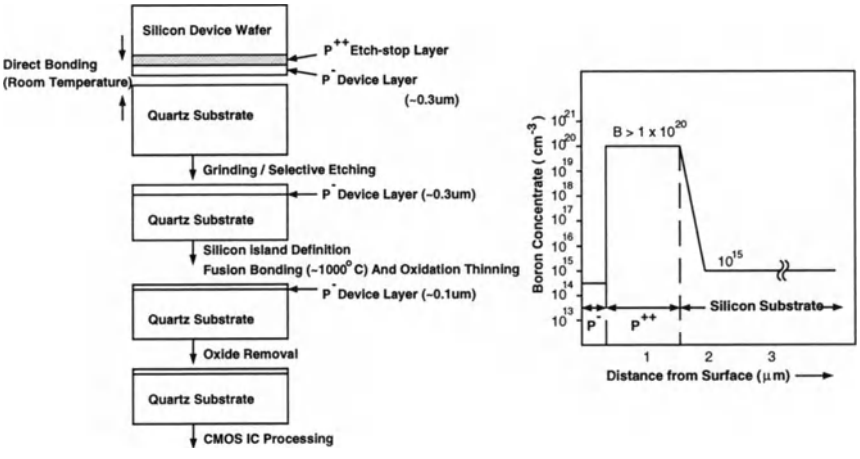


Figure 2.22: Schematic of the silicon-on-quartz approach using an etch-stop layer.

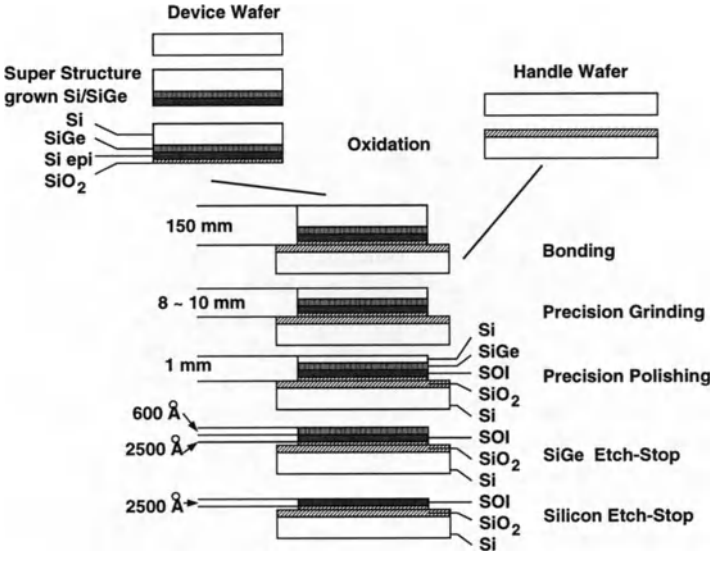


Figure 2.23: BESOI wafer fabrication flow diagram with SiGe-layer as the etch-stop layer.

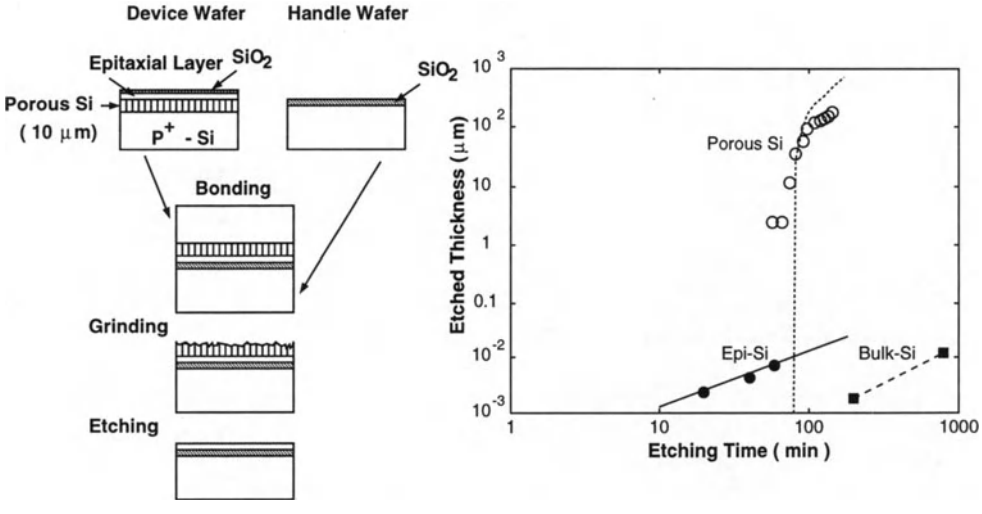


Figure 2.24: Schematic process flow of epitaxial layer transfer (ELTRAN) technique.

the one described before. After bonding is accomplished, via grinding and polishing, a selective etch is used to remove the SiGe etch-stop layer and the remaining silicon layer above it. Finally, only the silicon thin-film device layer is left for building the SOI device.

Fig. 2.24 shows the schematic process flow of epitaxial layer transfer (ELTRAN) technique[29]. In this process, a 10μm porous silicon layer is used as the etch-stop layer. The etchant for the etch-stop layer is $HF(3\%) + H_2O_2(25\%)$. As shown in the figure, due to the effective penetration of the etchant into the porous silicon layer, compared to other etch-stop layers, a high selectivity exists for this etchant. As described in the figure, the surface of the silicon wafer is first transformed into a $10\mu m$ porous silicon layer, followed by a silicon epitaxy step to grow a silicon thin-film device region. After similar procedures for bonding, grinding, and selective etch, the fabrication process of the SOI wafers is accomplished.

Fig. 2.25 shows the fabrication procedure of BESOI wafer without epitaxy and using LOCOS as the etch-stop layer[30]. As shown in the figure, a non-uniform oxide layer is grown on the wafer using LOCOS process. Then a thermal oxide used as the buried oxide is grown, followed by chemical mechanical polishing (CMP) to planarize the surface of the oxide-layer. After bonding the device wafer with the handle

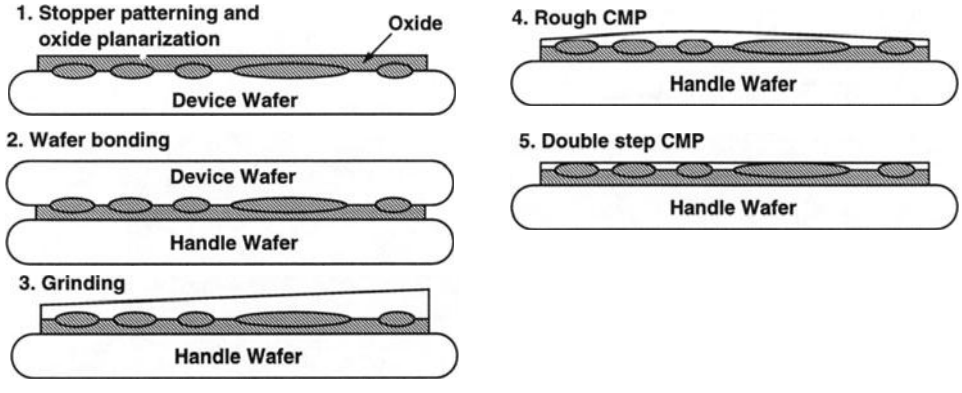


Figure 2.25: Fabrication procedure of BESOI wafer without epitaxy and using LOCOS as the etch-stop layer.

wafer, most of the silicon portion of the device wafer has been removed. Then a rough CMP is used to further grind the remaining silicon such that some of the local oxide is exposed. Next, a double-step CMP is used to remove all of the redundant silicon layer. Since this double-step CMP can remove silicon only, when it touches the polishing-stopper oxide, the etch stops. Therefore, the thin-film device region with a thickness identical to the polishing-stopper oxide is automatically left. In this processing technique, no epi-layer is needed— production throughput is high. However, device density may be low.

In the BESOI fabrication process, if the environment is not sufficiently clean during bonding or if the surface of the oxide layer is not even, dust or gas bubbles may exist between the bonded oxide layer. As a result, voids as shown in Fig. 2.26 may be formed[31]. As a result, the bonded wafers can't sustain the following high-temperature procedures. The thickness of the device thin-film region can't be uniform. Therefore, voids should be avoided during the BESOI process. In addition, polishing is commonly used in the BESOI technology. After grinding or polishing, the microscratch may further complicate the problem.

2.3.4 Smart-Cut SOI Technology

Smart-cut SOI technology is derived from BESOI. Two wafers are needed. As shown in Fig. 2.27, the device wafer is grown with a thick thermal oxide layer to be used

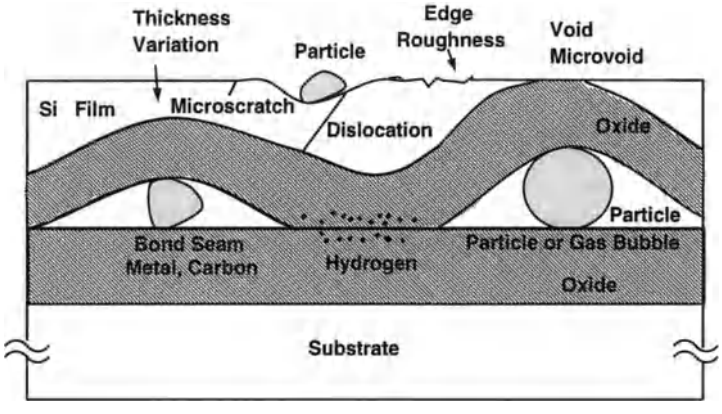


Figure 2.26: Potential defects in BESOI.

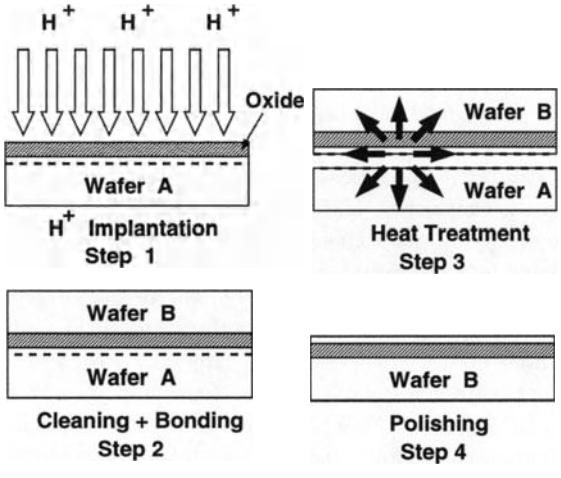


Figure 2.27: Principle of smart-cut SOI process.

as the buried oxide in the final SOI structure[32]. A hydrogen ion (H^+) implant at a dose of $2 \times 10^{16} - 1 \times 10^{17}\text{cm}^{-2}$ is carried out. After cleaning the device wafer and the handle wafer, they are bonded together at a temperature slighter than the room temperature. Then wafers are heated at 400-600C. The implanted hydrogen atoms at a depth under the oxide layer gather to form blistering. If the amount of the implanted hydrogen atoms is sufficient, this blistering will cause flaking of the whole silicon layer. As a result, a thin-film silicon layer with a thickness identical to the depth of the hydrogen implant is left at the top of the buried oxide. Then, a 1000C heat cycle strengthens the bonding of the two wafers. Due to the blistering, the microroughness of the wafer surface may not be acceptable. Application of CMP (chemical mechanical polishing) to smooth the wafer surface finalizes the smart-cut SOI procedure. The removed portion of the device wafer after flaking by blistering can be reused as wafers. In addition, no epitaxy is required for the smart-cut technology. Therefore, production throughput is high. Since the hydrogen profile after the H^+ implant is sharp, the thickness variation of the produced thin-film is small. Therefore, production cost and quality of the smart-cut technology are good.

2.4 Isolation Technology

In this section, three isolation technologies for SOI CMOS devices are described. They are mesa-isolation, LOCOS isolation, and shallow trench isolation. Mesa-isolation is frequently used for SOI devices. Fig. 2.28 shows the mesa-isolation of the SOI MOS devices[33]. During fabrication, the active thin-film region is masked and the thin-film in the field region is etched off. As a result, the active thin-film region of an SOI MOS device becomes a mesa. Using mesa-isolation, device density of the SOI MOS devices is high. However, there are problems associated with mesa isolation. In a mesa-isolated SOI MOS device, the edge of the mesa has a sharp profile, hence the stress is large. Therefore, the gate oxide at the edge of the mesa is thinner, which leads to a poor quality—easy to breakdown. If the edge of the mesa sidewall is steep, gate material residues may remain at the corner, which is not good for wiring since short circuit may occur. If the sidewall is also covered with the gate polysilicon, due to the existence of the steep edge at the sidewall of the mesa, 2D charge sharing effects and defects may be especially serious. Consequently, the threshold voltage at the sidewall of the mesa region of the MOS device is lower than that at the center channel region. Therefore, a subthreshold current hump as shown in the figure may occur for a mesa-isolated SOI MOS device.

Due to the edge effect from the mesa isolation, performance of the SOI MOS device is not good. Improvement of the mesa-isolation has been carried out. Fig. 2.29

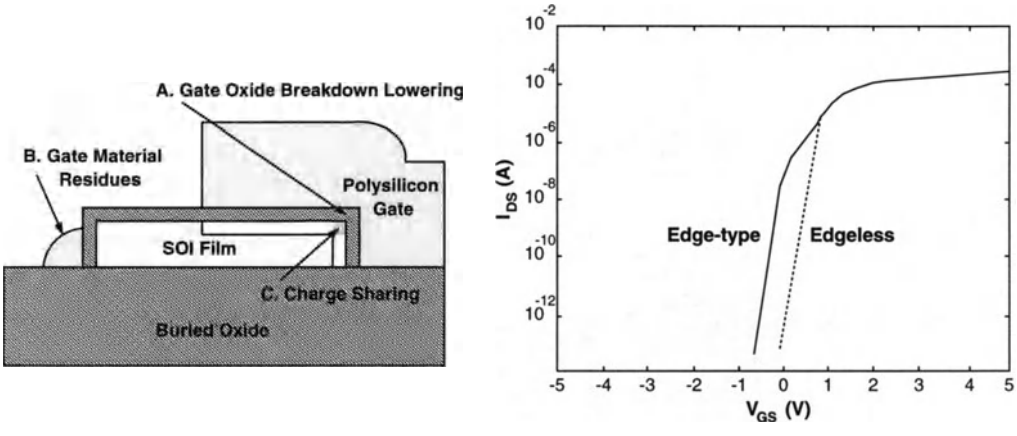


Figure 2.28: Mesa-isolation of the SOI MOS device and its subthreshold characteristics.

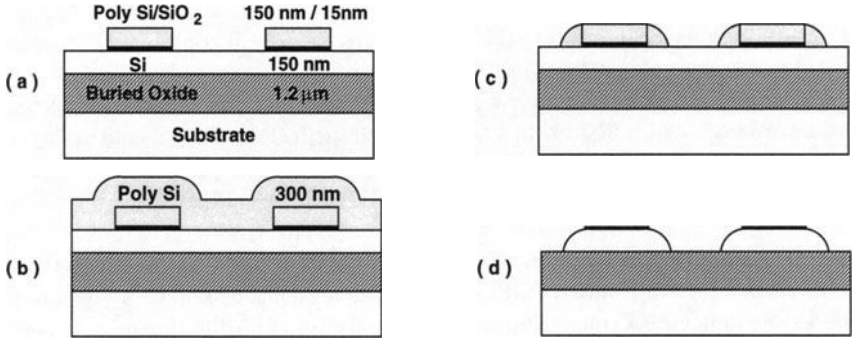


Figure 2.29: Rounded edge mesa (REM) formation procedure.

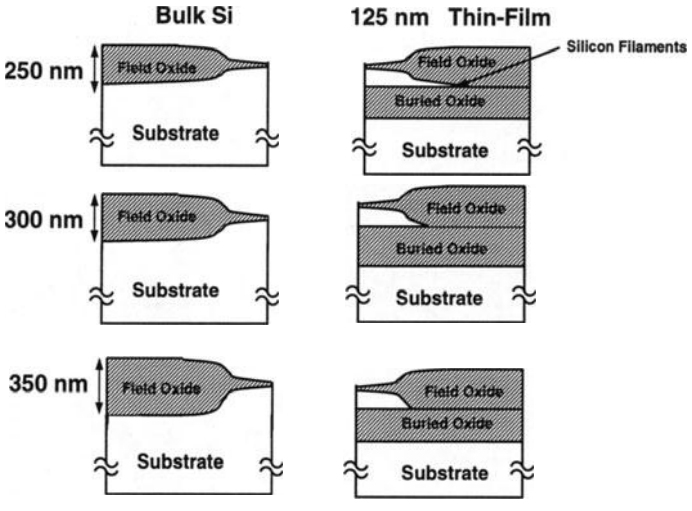


Figure 2.30: Cross section of LOCOS on bulk and SOI wafers.

shows the rounded edge mesa (REM) formation procedure[34]. As shown in the figure, over the active device thin-film region, a pad oxide layer and a polysilicon layer with an identical thickness as the thin-film region have been formed. Then the whole wafer is covered with a 300nm polysilicon layer. An anisotropic etch using reactive ion etching (RIE) technique is used to etch polysilicon. The RIE etch is carried on until the pad oxide and the buried oxide are exposed. Then, the RIE etch is stopped. At this moment, all polysilicon layer and the thin-film in the field region have been removed. Owing to the buffering effect of the polysilicon layer at the corner, the edge of the sidewall region becomes rounded instead of square-shape as described above. This completes the rounded edge mesa procedure.

In addition to mesa isolation, SOI CMOS devices can also be isolated using LOCOS. The LOCOS-isolated SOI CMOS technology has a similar processing procedure as the bulk CMOS one. Above the active device thin-film region, it is masked by a layer of the silicon nitride (Si_3N_4) layer, which is used to inhibit oxidation locally. During the thermal oxidation period, in the field region, local field oxide is grown. As for the bulk devices, bird's beaks are formed at the edge of the field oxide region. Compared to the bulk device, the consumption of silicon during the LOCOS process for SOI is different. For the bulk MOS devices, when a field oxide

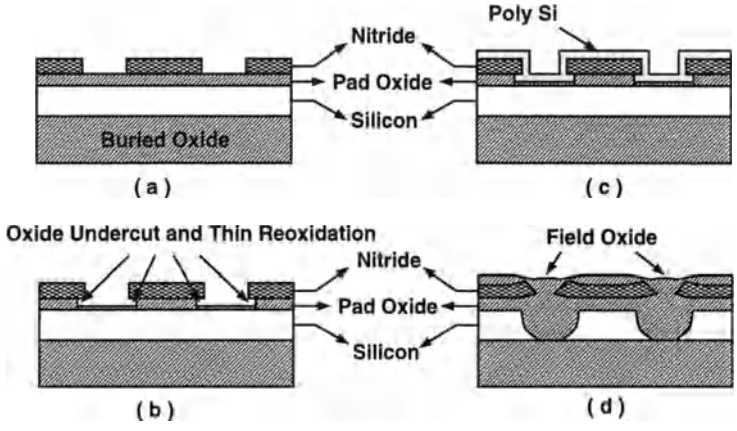


Figure 2.31: Main fabrication steps of SOI poly-encapsulated LOCOS (PELOX) isolation structure.

layer is formed, a silicon layer with a thickness equal to 1/2.2 times the thickness of the field oxide layer is consumed. In contrast, for the SOI MOS devices, a silicon layer with a thickness equal to 1/3 times the thickness of the field oxide layer is consumed. In an SOI technology, if the LOCOS process is used to oxidize the whole silicon thin-film, the time needed for oxidation is equal to the time required to grow a thermal oxide with a thickness 3 times the thickness of the silicon thin-film for a bulk device. If the oxidation time is shorter than this required amount, LOCOS is incomplete—silicon filaments as shown in Fig. 2.30 may exist, which leads to failure of device isolation[33]. With an equal thickness of the silicon layer, as compared to the bulk case, in the SOI structure, the longer time to fully oxidize the silicon thin-film is due to a larger stress.

In order to reduce bird's beaks and the silicon filaments at the edge of the field oxide in an SOI device, LOCOS technique can be improved. Fig. 2.31 shows the main fabrication steps of SOI poly-encapsulated (PELOX) isolation structure [35]. As shown in the figure, a pad oxide layer is grown over the thin-film. A patterned silicon nitride layer is used to mask the active device region during the thermal oxidation. After local oxidation, the pad oxide in the field region is etched off. Then a thin oxide is grown. The whole wafer is covered by a 300Å polysilicon layer. After field oxidation, the polysilicon region and the field region are fully oxidized. A wet etch is used to remove the oxidized polysilicon layer and the nitride layer. Using this PELOX isolation technique, with a 1000Å thin-film, the beak encroachment is

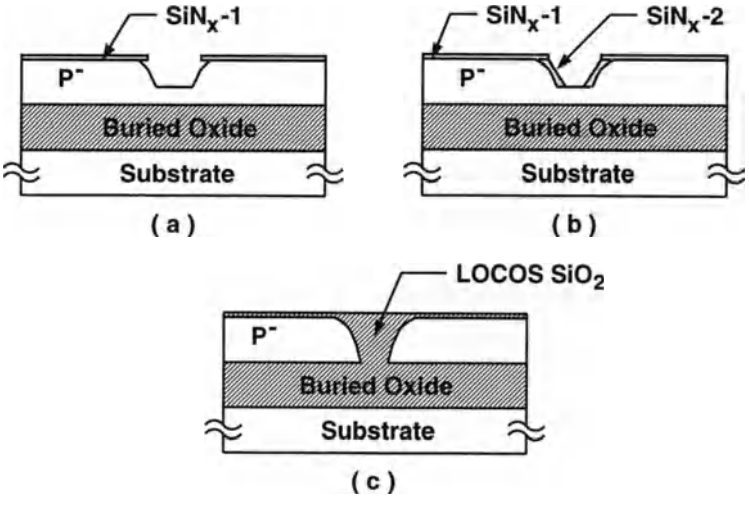


Figure 2.32: Two-step LOCOS isolation technique.

reduced to about 700Å.

Using the PELOX isolation technique, the planarization problem has not been resolved. Fig. 2.32 shows a two-step LOCOS isolation technique without the planarization problem[36]. At the beginning of the process, the thickness of the silicon thin-film is 560Å. During local oxidation, the active region is masked by a nitride layer. Field oxide is grown in the field region. Then the LOCOS oxide is etched away as shown in the figure. A 23-nm-thick silicon thin-film is left in the field region. At this moment, the corner of the thin-film region is rounded. Then, the wafer is covered with a 70Å nitride layer. A reactive ion etch (RIE) is used to remove the nitride on the wafer. As a result, the nitride in the field region is completely removed. In contrast, at the sidewall of the silicon islands, nitride still exists. The nitride at the sidewall can prevent the occurrence of the bird's beak encroachment. Another local oxidation is used to form the field oxide with a thickness identical to the thin-film. After local oxidation, the surface is planar. After etching away the nitride layer, the procedure is complete.

In addition to LOCOS, shallow trench isolation (STI) technique has also been used to provide isolation for SOI technology. Fig. 2.33 shows the cross section of a shallow-trench-isolated SOI MOS device with a channel width of 1μm, a silicon

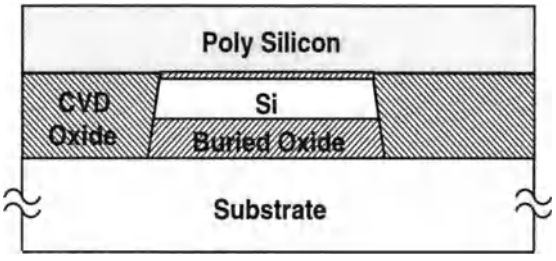


Figure 2.33: Cross section of a shallow-trench-isolated SOI MOS device with a channel width of 1μm, a silicon thin-film of 1500Å, and a buried oxide of 2000Å.

thin-film of 1500Å, and a buried oxide of 2000Å[37]. As shown in the figure, the silicon thin-film and the buried oxide layers in the field region are etched off. Then the trench is covered with CVD oxide. A chemical mechanical polishing (CMP) step is used to remove the surplus CVD oxide at the top such that the a planar surface can be obtained. When the trench is formed, the buried oxide below the silicon thin-film is also removed. By forming the trench with such a depth, the defects at the sidewall of the silicon thin-film are fewer. In addition, a more planar surface can be obtained when the trench is covered with the CVD oxide.

2.5 0.25μm SOI CMOS Processing Sequence

In this section, the processing sequence of a 0.25μm SOI CMOS technology based on SIMOX wafers to generate enhancement-type inversion-mode CMOS devices, using a two-step LOCOS isolation technique described in the previous section[36], is described. The starting material of the 0.25μm SOI CMOS technology is the SIMOX wafer with a p-type silicon substrate and a 90nm buried oxide. Atop the buried oxide is a silicon thin-film of 320nm. The thickness of the top silicon thin-film is reduced to 56nm by a sacrificial oxidation and a subsequent oxide etch as shown in step (3) in Fig. 2.34. On the top of the 56nm silicon thin-film, a pad oxide layer of 7nm is grown thermally— step (4). In step (5), a silicon nitride layer of 50nm on the pad oxide layer is deposited by LPCVD. In step (6), a photolithography procedure is used to define the field oxide region, followed by an RIE etch to remove the nitride layer over the field oxide region.

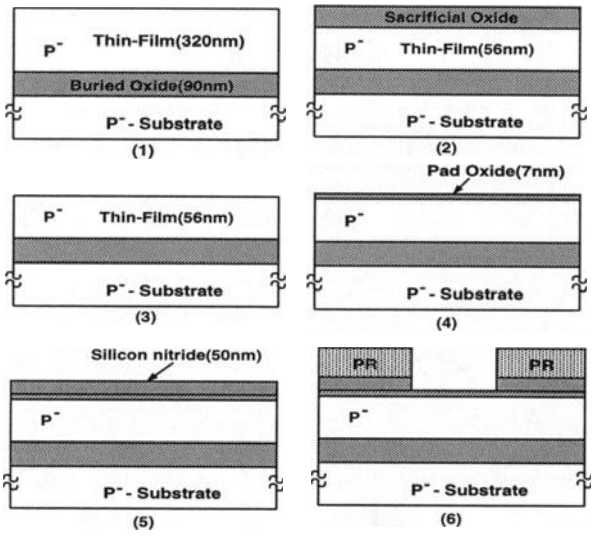


Figure 2.34: Step 1-6 of the 0.25μm SOI CMOS processing sequence.

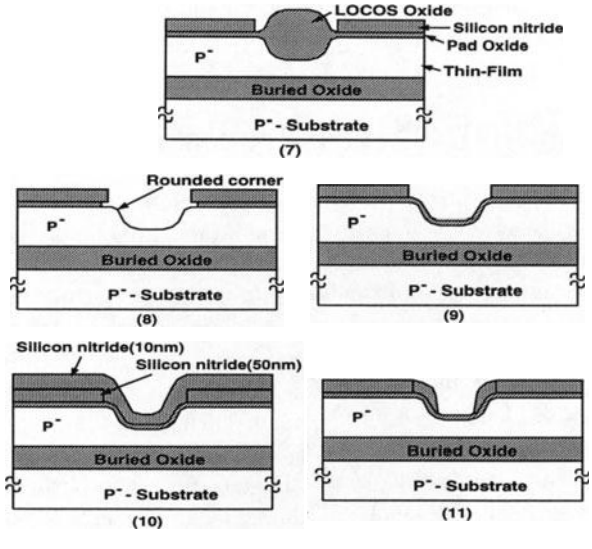


Figure 2.35: Step 7-11 of the 0.25μm SOI CMOS processing sequence.

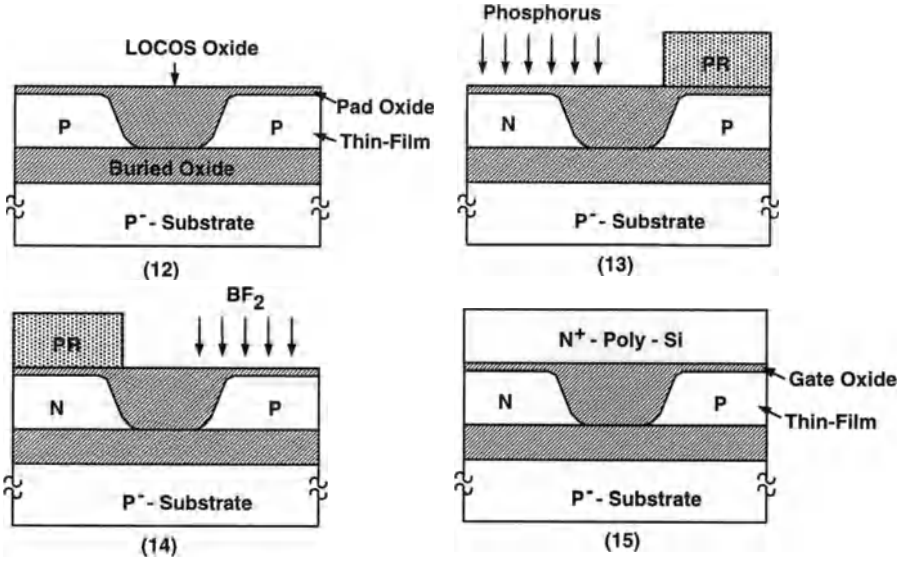


Figure 2.36: Step (12)-(15) of the 0.25μm SOI CMOS processing sequence.

Then a dry oxidation step at 1100C is carried out to generate the LOCOS field oxide region. After the LOCOS step, the thickness of the silicon thin-film below the field oxide is 23nm—step (7) as shown in Fig. 2.35. In step (8), the LOCOS oxide is removed by a wet etch. After this step, the corner of the silicon island is rounded. In step (9), a pad oxide layer of 70nm is grown on the top of the field region. Another silicon nitride layer of 10nm is deposited by CVD—step (10). In step (11), the 10nm silicon nitride layer over the field oxide region is removed by an RIE etch. Only the nitride layer over the active device region and the sidewall of the silicon island is left due to a larger thickness before the nitride etch.

In step (12), the field oxide is produced by the second LOCOS step at 1100C. Due to the existence of the nitride layer at the sidewall of the silicon island, the bird's beak has been substantially minimized. After the second LOCOS step, the thickness of the field oxide is about identical to the thickness of the silicon thin-film. Therefore, a planar surface can be expected. The remaining nitride layer is removed by a wet etch. In step (13), doping the silicon thin-film regions in the NMOS device and the PMOS device by implants is done. The PMOS thin-film region is implanted with phosphorus at a density of 10^{17}cm^{-3}, while the NMOS

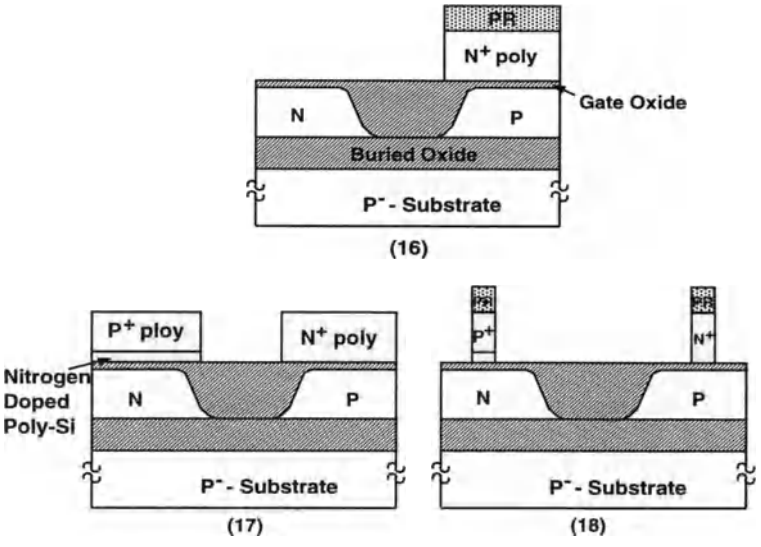


Figure 2.37: Step (16)-(18) of the 0.25μm SOI CMOS processing sequence.

thin-film region is masked by a patterned photoresist layer. The NMOS thin-film region is implanted with the BF_2 dopants at a density of $10^{17}cm^{-3}$. In step (15), the pad oxide is etched off. Then a 7nm gate oxide is grown by thermal oxidation, followed by a 0.3μm phosphorus-doped polysilicon layer is deposited by LPCVD as shown in step (15).

In step (16), the NMOS active device region is masked by photoresist. An ECR (electron cyclotron resonance) etch is used to remove the N^+ polysilicon layer except over the NMOS active device region. In step (17), after the photoresist layer is etched off, a thin nitrogen-doped CVD polysilicon layer is deposited, followed by a 0.3μm P^+ polysilicon layer. The purpose of the nitrogen-doped polysilicon layer is used to prevent the boron atoms in the P^+ polysilicon from penetrating through the gate oxide into the silicon thin-film during the subsequent high-temperature cycles. In step (18), an ECR etch is used to remove the N^+/P^+ layers except over the poly-gate region, which is masked by the patterned photoresist. Thus, the N^+ poly-gate for the NMOS device and the P^+ poly-gate for the PMOS device with a channel length of 0.25μm have been done.

In step (19), after stripping the photoresist, the wafer surface is covered by a

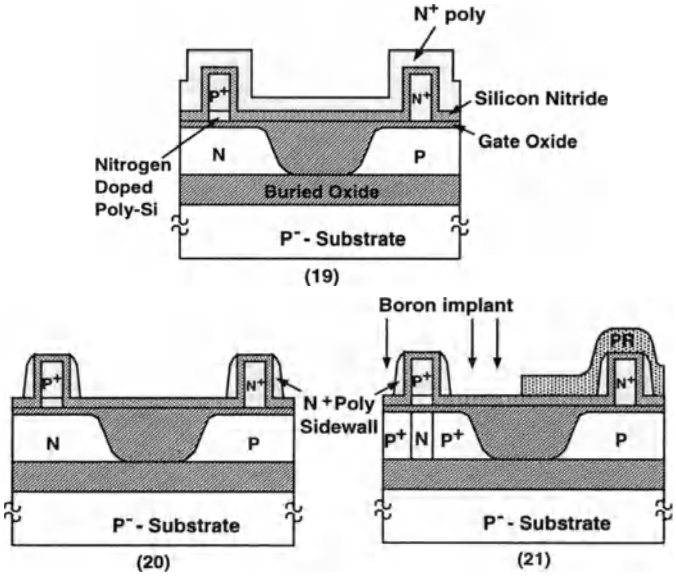


Figure 2.38: Step (19)-(21) of the 0.25μm SOI CMOS processing sequence.

silicon nitride layer, which is deposited by CVD, and an N^+ polysilicon layer. In step (20), the top N^+ polysilicon layer is removed by an ECR etch except some remaining at the sidewalls of the poly-gates, which becomes the polysilicon sidewall spacer. In step (21), a boron implant into the PMOS region generates its source/drain region, while the NMOS region is masked by a patterned photoresist. The use of the polysilicon sidewall spacer is to prevent the influence of the implant lateral straggle in the channel region during the source/drain implant. Similarly, in step (22) the NMOS source/drain regions are formed by the phosphorus implant while the PMOS region is masked by the patterned photoresist. In step (23), the photoresist is removed. The polysilicon sidewall spacers are etched off by a wet etch. Then the wafer is annealed by RTA (rapid thermal anneal) at 1000C such that the implanted dopants can be activated. In step (24), a low-temperature oxide (LTO) layer is deposited over the wafer by CVD. After planarization, contact areas are defined by the patterned photoresist.

In step (25), an RIE etch is used to remove the LTO and the silicon nitride in the contact areas. Then the wafer is deposited with a layer of Ti and TiN film by sputtering, followed by a tungsten film by CVD. The contact areas are masked

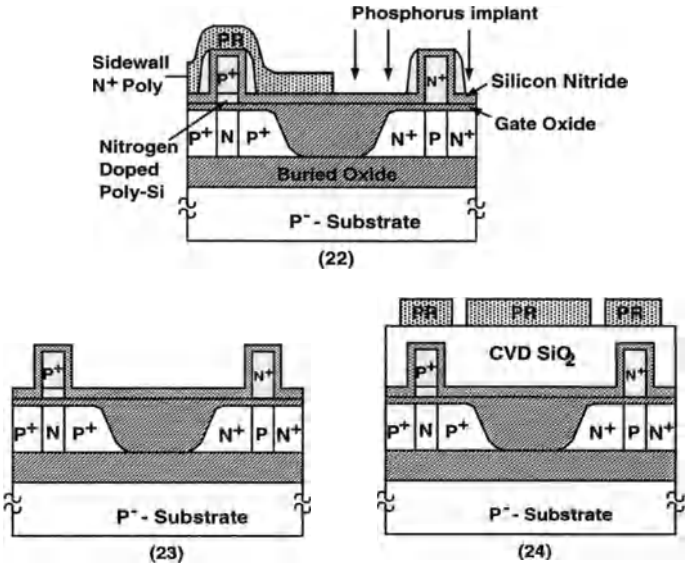


Figure 2.39: Step (22)-(24) of the 0.25μm SOI CMOS processing sequence.

by a patterned photoresist. In step (26), the W/TiN/Ti film outside the contact area is removed. Then the photoresist is stripped, followed by the deposition of the AlSiCu/Ti/TiN film. The interconnect metal lines are defined by patterning the photoresist over the AlSiCu/Ti/TiN layer. In step (27), the AlSiCu/Ti/TiN layer is etched off except the interconnect metal line areas. Then the wafer is deposited with a CVD LTO layer, followed by planarization of the surface. The via areas between interconnects are defined by the patterned photoresist.

In step (28), after the LTO in the via areas is etched off, the via areas are filled with Al. Then the wafer is covered with an Al/Ti layer, which is patterned by photolithography to define the second metal interconnect area. In step (29), the unwanted Al/Ti is removed by an Al etch. After stripping photoresist, the wafer is covered with a layer of silicon nitride for passivation, followed by the electrode pad opening and the post-metallization anneal. This completes the processing sequence of the 0.25μm SOI CMOS technology.

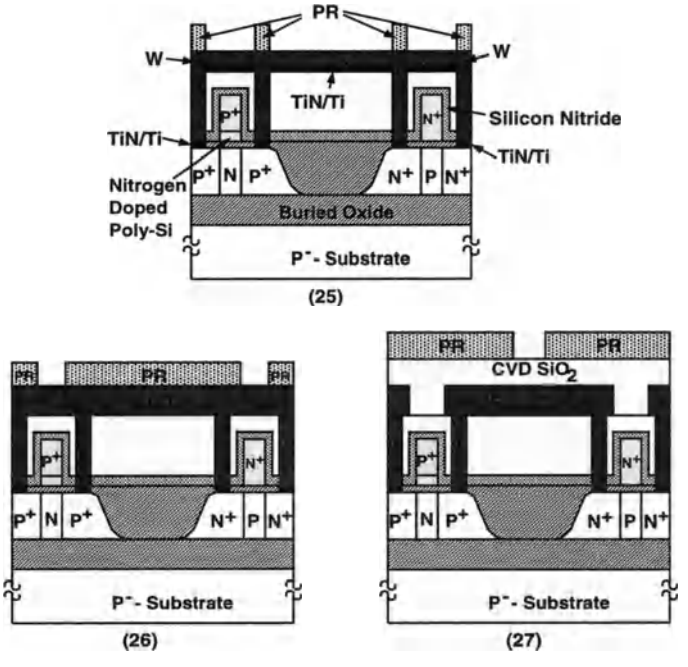


Figure 2.40: Step (25)-(27) of the 0.25μm SOI CMOS processing sequence.

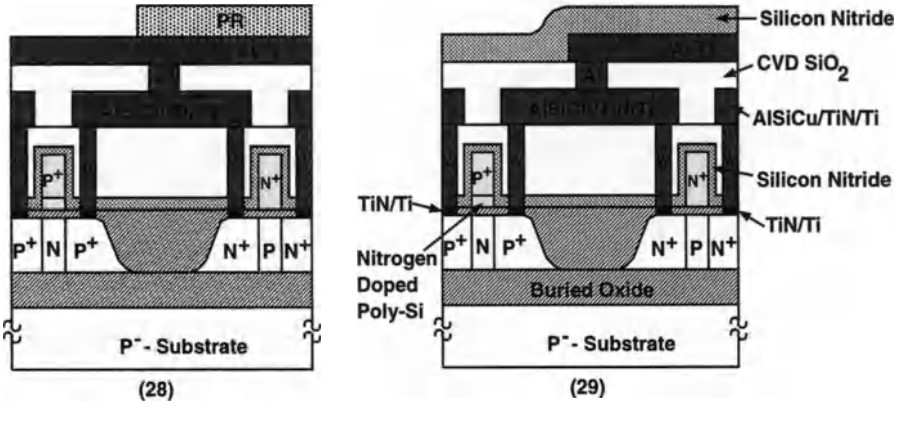


Figure 2.41: Step (28)-(29) of the 0.25μm SOI CMOS processing sequence.

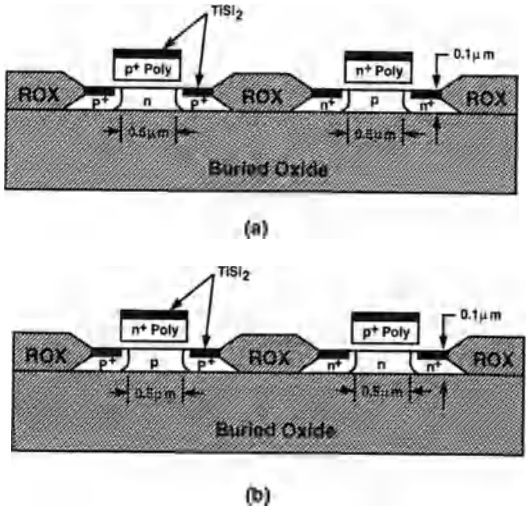


Figure 2.42: Inversion-mode and accumulation-mode SOI CMOS devices.

2.6 SOI CMOS Structures

In this section, different SOI CMOS structures including accumulation-mode, inversion-mode, partially-depleted, fully-depleted, double-gate, DELTA, and quasi-SOI devices are described.

2.6.1 Accumulation-mode versus Inversion-mode

In the bulk CMOS, no accumulation-mode device is possible due to the device isolation considerations. Thanks to the buried oxide isolation structure, in addition to the inversion-mode devices, accumulation-mode devices are also possible in the SOI CMOS structure as shown in Fig. 2.42[38]. For an inversion-mode NMOS device, from the source via the channel to the drain, the doping structure is $N^+ - P - N^+$, where the channel region is p-type, which is a different type from the source/drain region. For an inversion-mode SOI PMOS device, the device structure is $P^+ - N - P^+$, where the type of the dopants in the channel region is different from that in the source/drain region. For an accumulation-mode SOI PMOS device, the device structure is $P^+ - P - P^+$, where the type of the dopants in the channel region is same as that in the source/drain region. As for bulk CMOS, due to the work function difference, using the N^+ polysilicon gate, if an enhancement-

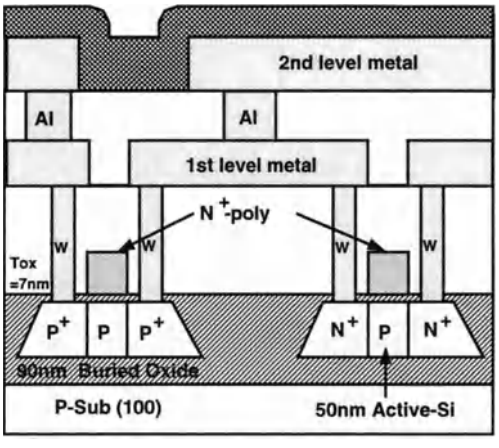


Figure 2.43: Cross section of an ultrathin 0.24μm polysilicon-gate CMOS/SIMOX structure with double metallization.

type PMOS device is needed ($V_T < 0$), an accumulation-mode SOI PMOS device, which has a $P^+ - P - P^+$ structure, can be used. The inversion-mode NMOS device ($N^+ - P - N^+$) can be enhancement-type (with a positive threshold voltage) by using the N^+ poly-gate. Using the P^+ polysilicon gate, if an enhancement-type NMOS device is needed, the accumulation-mode NMOS, which has an $N^+ - N - N^+$ structure, can be used. In order to have an enhancement-type PMOS device, the inversion-mode PMOS device ($P^+ - N - P^+$) can be used.

For an accumulation-mode SOI PMOS device, the doping structure in the thin-film is $P^+ - P - P^+$, which is similar to the surface doping structure used in a buried-channel bulk PMOS device with an N^+ polysilicon gate using bulk CMOS technology. When the hole channel exists in the accumulation-mode SOI PMOS device, the channel may not be located at the front Si/SiO_2 interface. Instead, it may be located above the buried oxide— the buried channel. Therefore, with a buried channel and a lower doping density, a higher mobility and thus a larger drain current can be expected from a buried-channel device. However, short channel effect of the accumulation-mode device is also larger. In addition, the subthreshold slope is poorer.

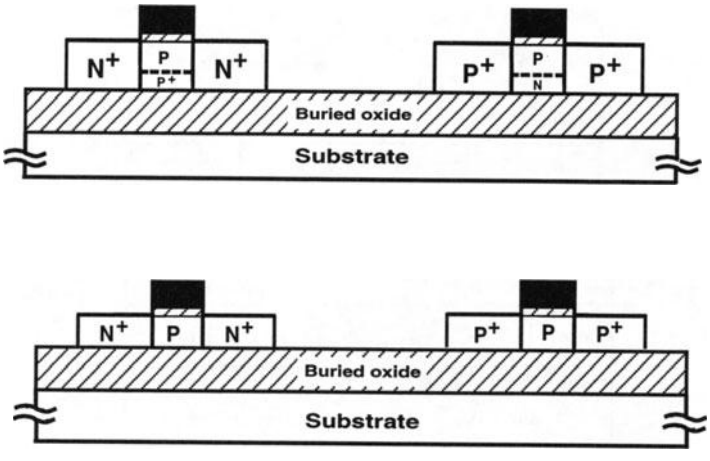


Figure 2.44: SOI CMOS devices: partially-depleted versus fully depleted.

For an SOI CMOS technology using an N^+ polysilicon gate, for enhancement-type devices, its NMOS device can be inversion-mode and its PMOS device can be accumulation-mode as shown in Fig. 2.43. Since the PMOS device is accumulation-mode, a larger mobility in the PMOS device leads to a smaller difference in the mobilities between PMOS and NMOS devices [39].

2.6.2 Partially Depleted versus Fully Depleted

Depending on the thickness of the silicon thin-film, the SOI CMOS devices can be divided into thick-film and thin-film. As shown in Fig. 2.44, if the silicon thin-film is thick, only the top portion of the silicon thin-film is depleted and the bottom portion is neutral. This type of SOI CMOS devices is called partially-depleted SOI CMOS devices. If the silicon thin-film is fully depleted, this type of the SOI CMOS devices is called fully-depleted SOI CMOS devices.

In a partially-depleted SOI CMOS device, the threshold voltage is insensitive to the thin-film thickness since the depletion region is independent of the film thickness. Therefore, for the partially-depleted thin-film SOI CMOS devices, the threshold voltage variation due to manufacturing factors is smaller. However, due to the neutral region in the thin-film in a partially-depleted SOI CMOS device, the floating body

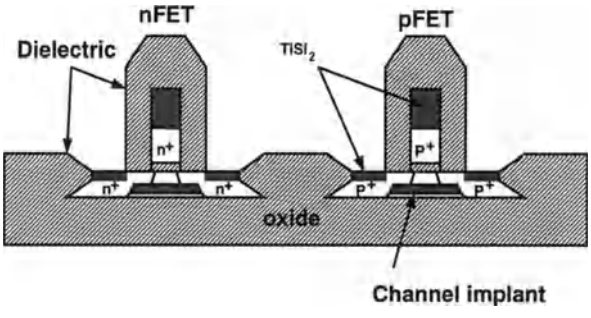


Figure 2.45: Cross section of partially-depleted SOI CMOS devices with a channel length of 0.08μm, a silicon thin-film of 1000Å, and a gate oxide of 42Å, with a non-uniform channel doping.

effect due to the parasitic bipolar device structure is more serious. In addition, the depletion region is more susceptible to the influence from the source and the drain regions. Therefore the device second order effects are more serious. Furthermore, in some partially-depleted silicon thin-film SOI CMOS devices, due to the neutral region, an unsmooth transition in the drain current characteristics—kink effect can be identified.

In a fully-depleted thin-film SOI CMOS device, regardless of the biasing condition, the silicon thin-film is fully depleted. In addition, a larger transconductance can be expected due to the larger gate control capability over the silicon thin-film. Therefore, the device second order effects including the short channel effect and the narrow channel effect are smaller. In addition, the subthreshold slope is improved. However, in a fully-depleted device, the threshold voltage may be sensitive to the thickness of the silicon thin-film, which may vary due to the fabrication process. Therefore, uniformity of the threshold voltage of the fully-depleted SOI CMOS devices may be poorer.

In order to have a device with a smaller sensitivity to the silicon thin-film thickness, partially-depleted devices are required. Fig. 2.45 shows the cross section of partially-depleted SOI CMOS devices with a channel length of 0.08μm, a silicon thin-film of 1000Å, and a gate oxide of 42μm, with a non-uniform channel doping[40]. As shown in the figure, in the bottom portion of the silicon thin-film, the doping

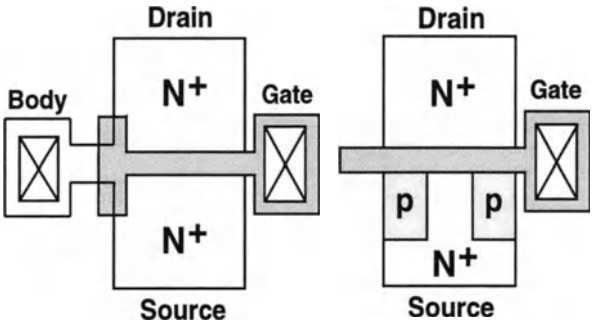


Figure 2.46: Body-fixed structures for SOI MOS devices .

density is higher. Using the non-uniform doping structure, kink effect and drain-induced-barrier-lowering effect (DIBL) can be suppressed. During the operation of the devices, the more highly-doped bottom portion of the silicon thin-film remains neutral.

For a partially-depleted SOI MOS device, due to the existence of the neutral region in the silicon thin-film, when the neutral region is floating, floating body effects may degrade its performance. Therefore, the silicon thin-film region needs to be contacted. As shown in Fig. 2.46, body contact to a partially-depleted SOI NMOS device can be implemented via an extended silicon thin-film region—T-gate type[41]. Using the T-gate type body contact, the gate capacitance increases since the gate overlap area increases. The body contact to the SOI MOS device can also be implemented via the body-tied-to-source (BTS) structure where the body contact is in the source region with the metal interconnect touching the P^+ body contact and the N^+ source region simultaneously. Using BTS structure, source and drain cannot exchange— less flexibility for circuit design. In addition, the smaller source region leads to a smaller effective channel width, which is disadvantageous for circuit operation. There is another body contact technique— field-shielded isolation as shown in Fig. 2.47[41]. As shown in the figure, the active device region is surrounded by the field-shield gate, which is connected to ground, such that the thin-film region can be protected against the influence from the front gate (transfer gate) when crossing this region. In addition, the oxide is thick between the field-shielded gate

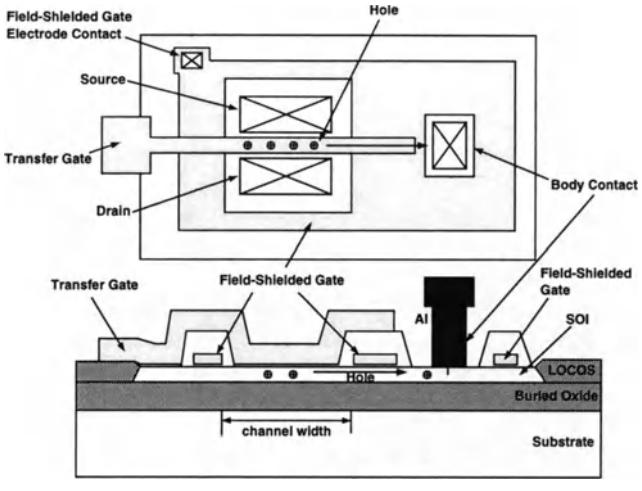


Figure 2.47: Schematic diagram of hole extraction using field-shielded isolation.

and the transfer gate, hence, the front gate capacitance is not changed substantially. The body of the device is connected to the body contact via the thin-film region under the field-shielded gate. Fig. 2.48 shows the schematic diagram of the sea of gates (SOG) gate array for practical use[41]. As shown in the figure, the doping density in the thin-film region under the field-shielded gate has been enhanced by an implant to reduce the resistance between the thin-film body and the body contact.

2.6.3 Double Gate & DELTA

The gate of most MOS devices is at the front surface—single-gate device. For SOI devices, their silicon thin-film region is surrounded by buried oxide. During the fabrication process, under the silicon thin-film region in the buried oxide, another gate—back gate can be arranged. Therefore, in addition to the channel at the front surface, a back channel controlled by the back gate can also function. Since both top and bottom gates can control the channels in the silicon thin-film, thus this kind of structure is called double-gate. Fig. 2.49 shows the cross section of a double-gate SOI MOS structure[42]. In a double-gate SOI MOS device, the polysilicon gate is surrounding the silicon thin-film. The key step in forming the double-gate SOI technology is described. After the silicon thin-film is etched off to become a mesa-isolated structure for the active region, an isotropic etch is used to remove

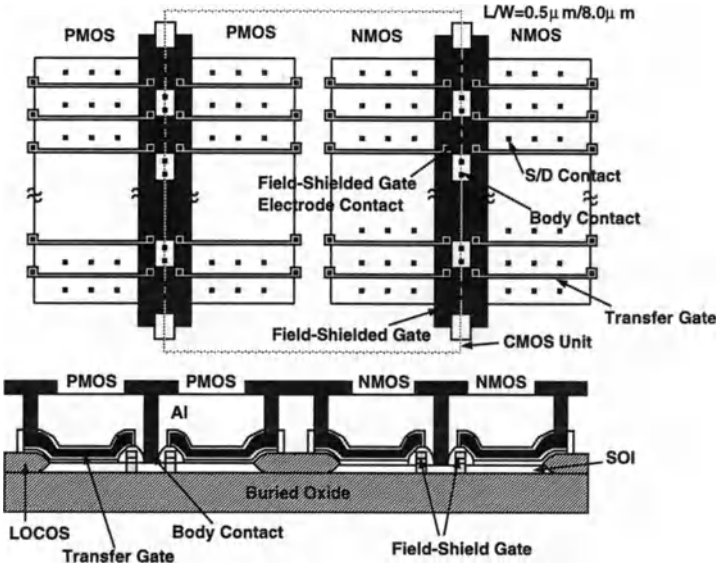


Figure 2.48: Schematic diagram of the sea of gates (SOG) gate array fabricated on an SOI substrate.

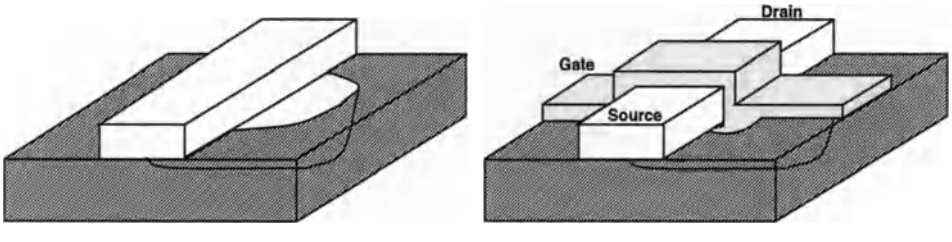


Figure 2.49: Double-gate SOI MOS structure.

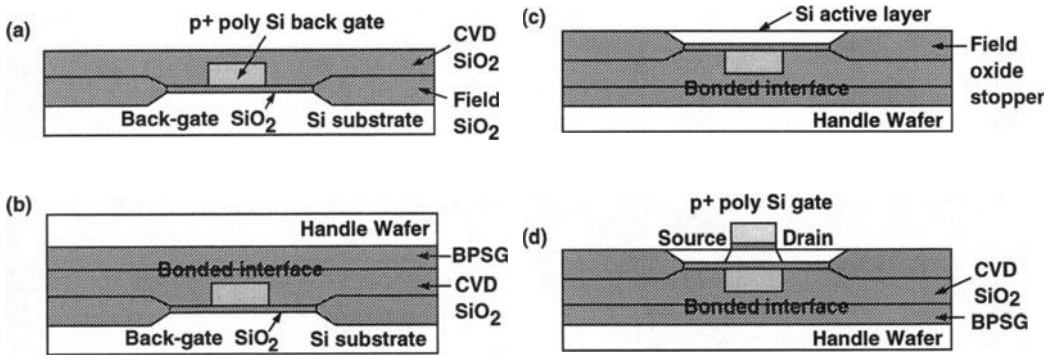


Figure 2.50: Key fabrication processing steps for producing double-gate BESOI MOS devices.

the oxide layer of the channel region. Since it's an isotropic etch, the buried oxide layer under the silicon thin-film is also etched off to become a cave. Then the silicon island area becomes like a bridge across this cave. After gate oxidation, a layer of polysilicon is deposited over the whole wafer by CVD. Thus this cave is filled up with the CVD polysilicon. Then, the polysilicon layer is etched off except the gate areas. After the poly etch, the double-gate structure as shown in Fig. 2.49 is completed. After the source/drain implant and metallization procedures, the fabrication processing procedure for double-gate is done. As shown in the figure, since the gate is surrounding the silicon thin-film channel region, therefore it's also called gate-all-around (GAA) device. Due to a much better control capability over the silicon thin-film, the double-gate SOI CMOS device has a larger transconductance, and reduced second-order effects. Specifically, the short channel effect and the narrow channel effect are reduced. In addition, the subthreshold slope is improved.

Double-gate SOI devices can also be built using BESOI technology. As shown in Fig. 2.50, the device wafer is processed using the processing sequence as for regular bulk MOS devices[43]. After accomplishing the field oxide, the gate oxide, and the poly-gate, the top surface is covered by a layer of CVD oxide. A CMP (chemical-mechanical polishing) procedure is used for planarization of the surface. Then, using the BESOI procedure, the device wafer is bonded with the handle wafer, which is covered with a layer of BPSG (boro-phoso-silicate glass). Then the redundant silicon layer in the device wafer is further ground by CMP using the field oxide as

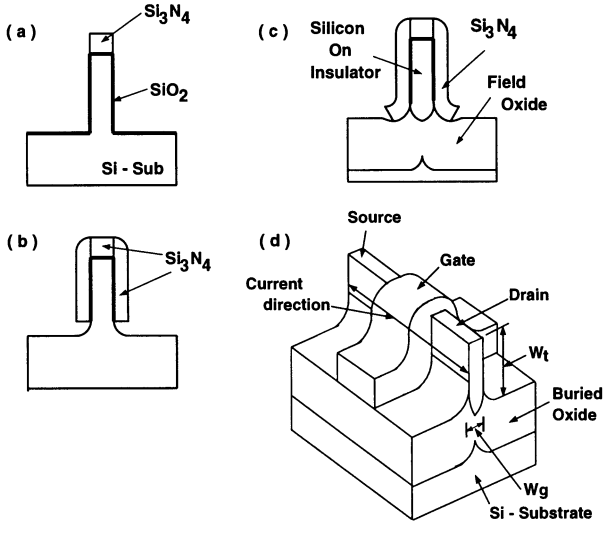


Figure 2.51: Process flow of the selective oxidation for the fully-depleted lean-channel transistor(DELTA).

the polishing stopper. After the CMP step, only the silicon thin-film layer, which is used as the device region, is left. Thus the gate in the device wafer becomes bottom gate in the double-gate structure. After the regular MOS processing procedure to accomplish the front gate oxide, the front poly-gate, the implanted source/drain, and the metallization steps, the double-gate structure is accomplished.

The other kind of double-gate SOI MOS device is called the fully-depleted lean-channel transistor (DELTA) as shown in Fig. 2.51[44]. As shown in the figure, on the top of a regular silicon wafer, a pad oxide layer is grown. Then, a silicon nitride layer is deposited, followed by an RIE etch to remove the nitride layer and a layer of the silicon except the active device region. Thus, the silicon-island structure is formed (a). Another pad oxide layer is grown. Then, a layer of CVD nitride followed by an RIE etch is used to cover the top and the sidewall of the silicon-island with nitride (b). A dry oxidation at 1100C is used to grow the field oxide. After this dry oxidation, the silicon island is totally isolated by the buried oxide (c). After the regular MOS fabrication procedure to finish the poly-gate, the source/drain implant, and the metallization, the DELTA structure is done. In the DELTA structure, the poly-gate surrounds most of the bottom portion of the thin-film region— alike the

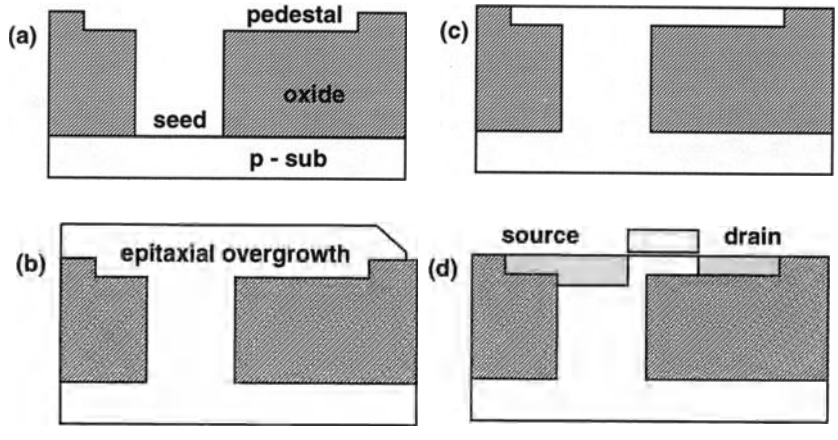


Figure 2.52: Processing sequence of quasi-SOI.

double-gate SOI structure.

2.6.4 Quasi-SOI

For SOI MOS devices, owing to fully surrounding of the silicon thin-film by the buried oxide, there are advantages in low parasitic capacitances and small second-order effects. However, self-heating is also a problem due to the isolation of the buried oxide. In addition, body contact is difficult to place. Innovations have been done to resolve these difficulties. As shown in Fig. 2.52, by having a small opening in the buried oxide, the above problems can be lessened. As shown in Fig. 2.52, a layer of thick field oxide is grown on the top of the silicon wafer[45]. Then the field oxide is etched off partially to form a pedestal. Then a further etch is used to form a seed hole through the field oxide (a). A selective epitaxy and a lateral overgrowth are used to fill the hole and the pedestal with single-crystal silicon (b). A CMP procedure is used to remove the redundant silicon layer. Thus, the single-crystal silicon and the remaining become the thin-film active region (c). Gate oxidation, poly-gate, source/drain implants, and metallization are accomplished following a regular CMOS fabrication procedure to accomplish the fabrication procedure. Owing to the hole in the buried oxide, heat dissipation problems can be removed (d). In addition, holes generated from impact ionization when the device is biased with a high lateral electric field can be removed. Thus impact ionization effects can be

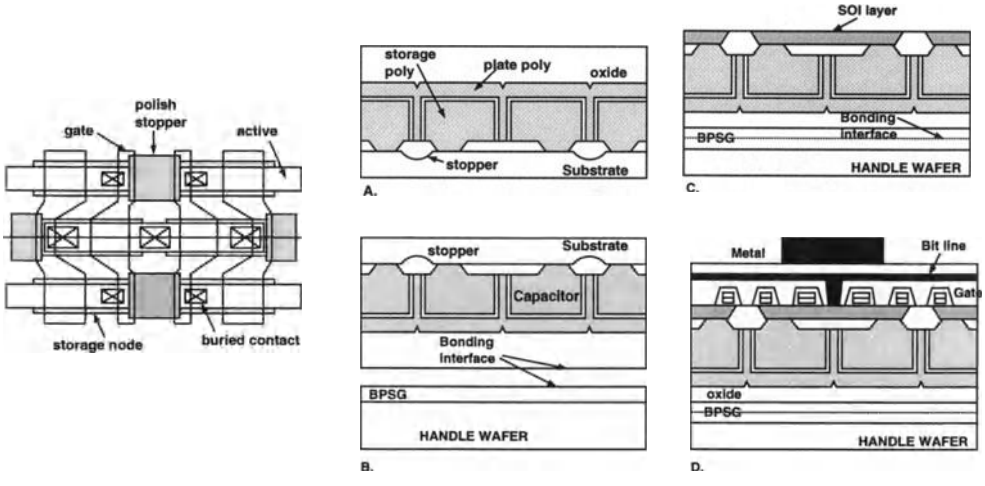


Figure 2.53: Process sequence of an SOI DRAM technology.

substantially reduced. Since most region is still covered with the buried oxide, the advantages of SOI structure still exist.

2.7 Special-purpose SOI Technologies

In addition to CMOS technology, SOI technology has also been used to implement other technologies. In this section, special-purpose SOI technologies including DRAM, BiCMOS, and power are described.

2.7.1 SOI DRAM

Owing to the low parasitic capacitance and good radiation hardness properties, SOI technology has been regarded suitable for integrating DRAMs. The SOI DRAM technology is slightly different from the SOI CMOS technology. Fig. 2.53 shows the process sequence of an advanced SOI DRAM technology with the memory cell layout[46]. As shown in the figure, on the device wafer, localized field oxide is grown by the LOCOS technique, followed by a thermal oxidation step to grow buried oxide. Then, contact-hole etching, polysilicon deposition, and another thermal oxidation are carried out to form the storage capacitor in the memory cell. Next, the top of the device wafer is covered with a layer of oxide, followed by planarization of the

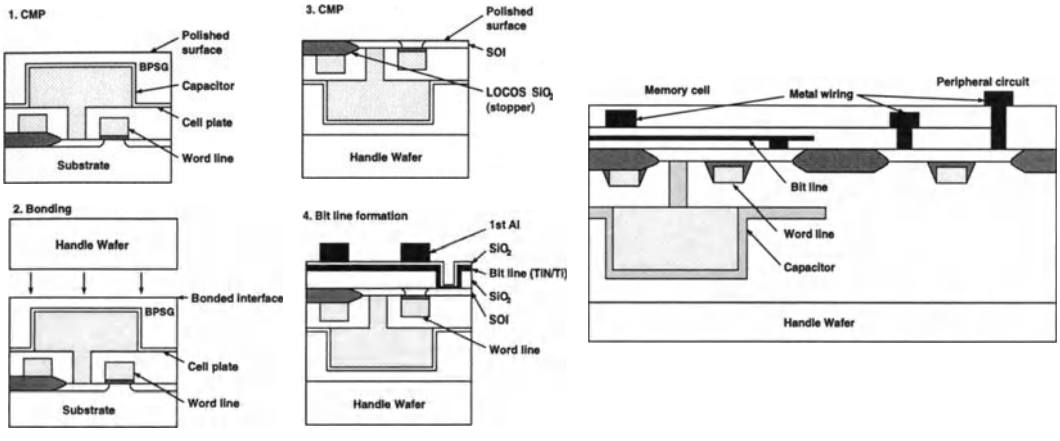


Figure 2.54: Processing sequence of an SOI DRAM technology.

surface. Using BESOI technology, the device wafer is bonded with the handle wafer, which is covered with BPSG (boro-phoso-silicate glass). The redundant silicon layer on the top of the device wafer is removed by grinding and CMP. At this step, the field oxide is used as the polishing stopper. After CMP, only the thin-film stays. The shallow trench isolation can be used to isolate thin-film regions. Then, poly-gate, source/drain implant, and metallization as for a the regular CMOS fabrication procedure are completed.

In the above SOI DRAM processing procedure, after finishing the storage capacitor, wafer bonding is initiated, followed by fabrication of the MOS transistors. In another SOI DRAM technology, wafer bonding is not initiated only until the storage capacitance and MOS transistors are done. As shown in Fig. 2.54, after the storage capacitor and MOS transistors are done, bonding with the other handle wafer is done[47]. The redundant silicon on the device wafer is removed by grinding and CMP. Then the bonded wafers are covered with an oxide layer for metallization. The advantages of this SOI DRAM technology are that bit lines are crossing a planarized region. In addition, bit lines and word lines (poly-gate) are located at the top and the bottom of the thin-film active device region. Therefore, the distance between the bit line and the source/drain region is smaller than that as for the conventional structure. Therefore, contact holes do not need to be large. Therefore, device density can be increased. Furthermore, after wafer bonding, no high-temperature steps

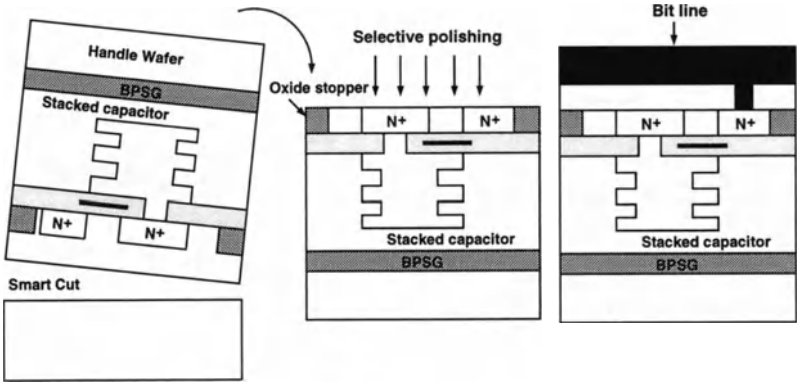


Figure 2.55: Application of smart-cut SOI technology to realize the DRAM buried capacitor structure.

exist. Therefore, low-cost glass substrate can be used as the handle wafer.

Smart-cut SOI technology has also been used to realize DRAMs such that high efficiency and low cost can be reached. As shown in Fig. 2.55, after completing the storage capacitor and the MOS devices, a hydrogen implant is initiated, followed by wafer bonding and wafer splitting as described in the smart-cut SOI technology[10]. Using smart-cut SOI technology, the time needed for grinding and CMP can be substantially reduced. In addition, the split wafer can be re-used.

In addition to BESOI, quasi-SOI technology has also been used to integrate DRAMs. As described before, quasi-SOI technology can be used to reduce the floating body effects. As shown in Fig. 2.56, a thermal oxidation procedure is carried out, followed by an RIE etch to generate the pedestal area and the seed hole in the oxide[48]. Then, using an epitaxial lateral overgrowth technique, the seed hole and the pedestal area are filled with single-crystal silicon. A preferential polishing step is used to remove the redundant silicon layer. After completing the MOS devices in the thin-film and the storage capacitor, the process is complete.

2.7.2 SOI BiCMOS

BiCMOS devices can be integrated using SOI technology. Fig. 2.57 shows the fabrication processing sequence of a 0.5μm complementary BiCMOS SOI technology,

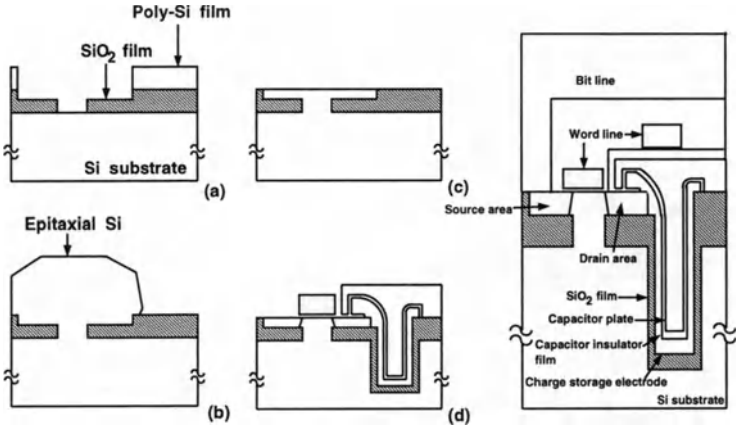


Figure 2.56: Transistor on a lateral epitaxial silicon layer (TOLE) DRAM cell fabrication steps.

which has lateral npn and pnp bipolar devices using polyemitter, poly-base, and silicide techniques[49]. At the beginning of the processing sequence, on the SIMOX or BESOI wafers, an oxide layer is grown. After a wet etch to remove oxide, the thickness of the silicon thin-film is reduced to 2000Å, followed by the LOCOS isolation procedure to produce a 4000Å field oxide for device isolation. Then a sacrificial oxide of $1000 - 2000$Å is grown. Next, channel implants for CMOS devices (n-type for PMOS and p-type for NMOS) and well implants for BJT (n-type for npn and p-type for pnp) are done. The sacrificial oxide outside the BJT area is etched off, followed by the 105Å gate oxidation. A polysilicon layer of 3000Å is deposited, followed by a short oxidation cycle to grow a thin oxide layer on polysilicon. For NMOS and PNP BJT, the polysilicon layer is implanted with phosphorus. For NPN BJT, it is doped with boron. For PMOS device, the polysilicon layer is not doped at this moment to prevent the boron dopants from penetration through the gate oxide into the channel region. At the next step, the whole wafer is deposited with a nitride layer and TEOS (tetraethylorthosilicate— $Si(OC_2H_5)_4$) oxide layer. The base/emitter edge of the BJT area is defined by photolithography. An RIE etch is used to remove the polysilicon and the oxide layers on the emitter, followed by a CVD poly-layer deposition and implants (P^+ for NPN, N^+ for PNP). Then, an RIE etch is used to remove this poly-layer. After this etch, some polysilicon is left at the edge of the base/emitter edge to become poly sidewall. Next, base im-

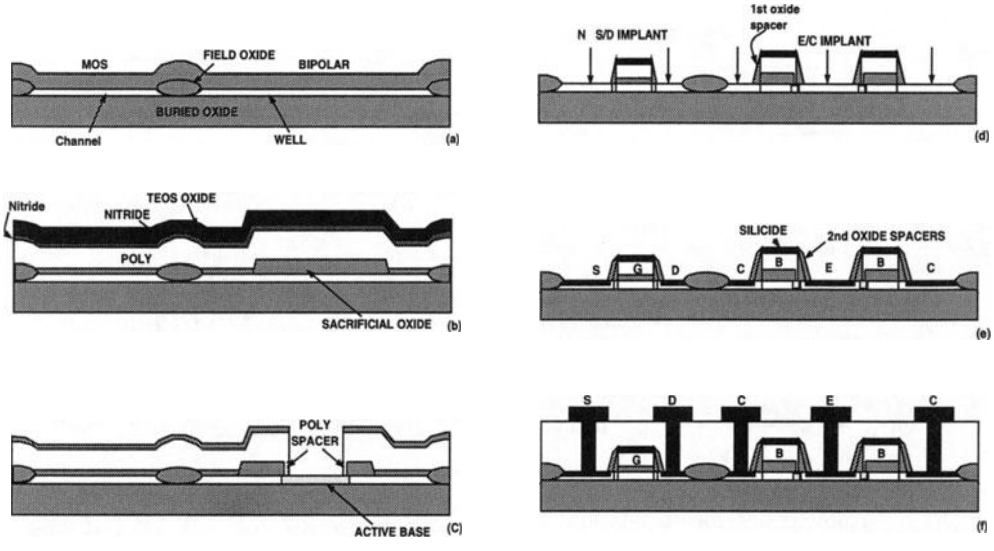


Figure 2.57: 0.5μm SOI BiCMOS fabrication processing sequence.

plants for BJT (p-type for npn and n-type for pnp) are carried out. Note that the poly sidewall spacer links the extrinsic poly-base contact and the intrinsic base region. BJT collector edge and the MOS gate area are patterned by photolithography.

When the BJT collector edge and the MOS poly-gate are done, lightly-doped drain (LDD) implants for CMOS are carried out (N^- type for NMOS and P^- for PMOS). Following a similar procedure for forming the poly spacer, thin-oxide spacers are formed at the emitter/base edge of the BJT and the poly-gate sidewall of the MOS. Note that this thin-oxide spacer defines the base region for the BJT and the LDD region for the MOS. Then, an arsenic implant defines the source/drain doping profile of the NMOS and the emitter/collector doping profile of the NPN, followed by a BF_2 implant to define the doping profile of the pnp emitter/collector. The nitride on the poly-layer is etched off. Note that this nitride is used to prevent the poly-base from the influence of the emitter/collector implant. A boron implant is used to dope the poly-gate and source/drain of the PMOS.

At the edge of the polysilicon layer, a second oxide spacer with a larger thickness is formed. Then, at the exposed silicon thin-film surface, a self-aligned silicide layer is formed. At the poly-layer surface, polycide is formed. Note that the second oxide

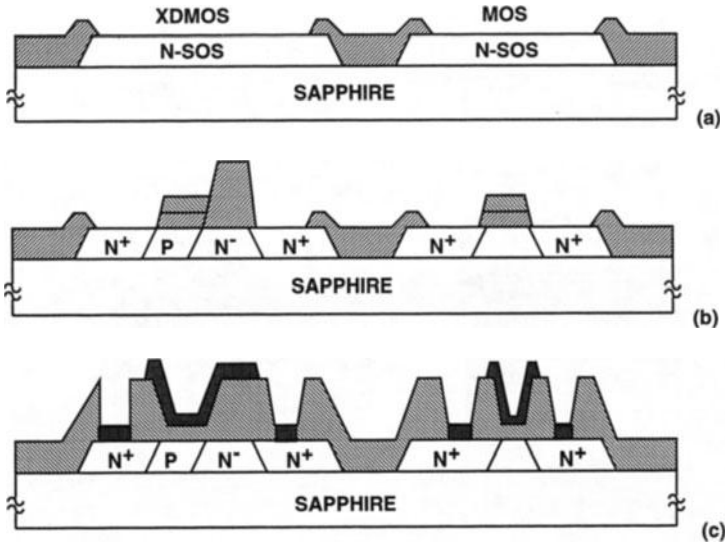


Figure 2.58: Fabrication sequence for lateral double-diffused MOS (DMOS)/SOS.

spacer is used to keep the emitter contact away from the emitter/base junction such that extra leakage can be prevented. Finally, an oxide layer is deposited, followed by planarization, contact hole formation, and two-layer metallization.

2.7.3 SOI Power

SOI technology has also been used to integrate high-voltage power devices with the control circuits. Fig. 2.58 shows the fabrication sequence for double-diffused MOS DMOS/SOS[50]. As shown in the figure, after the silicon thin-film is formed, the field region of the silicon thin-film is etched off, and then filled with oxide. The source/drain, channel, and the n- drift regions are defined by implants, followed by gate oxidation. The drift region is used for sustaining high voltages. Next, a thicker oxide layer (5000Å) is grown on the top of the drift region, followed by contact formation and metallization. In addition to high-voltage DMOS devices, low-voltage CMOS devices used for control circuits can also be integrated together. Due to the insulating substrate, interference between the high-voltage DMOS devices and the CMOS control circuits can be minimized.

BESOI technology has been used to integrate high-voltage power devices. Fig. 2.59

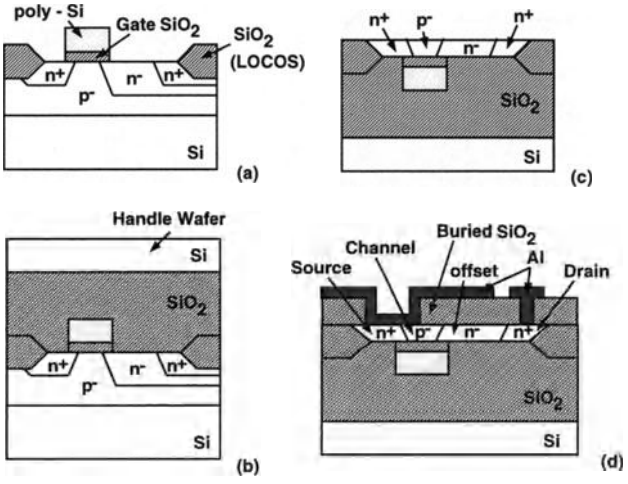


Figure 2.59: Processing steps of a quasi-SOI power lateral DMOS device using reversed silicon wafer direct bonding technique.

shows the processing steps of a quasi-SOI DMOS device using reversed silicon wafer direct bonding technique[51]. As shown in the figure, on the device wafer, doping of the p-channel of the DMOS device is done first, followed by the LOCOS isolation, gate oxidation, poly-gate formation, n- drift region doping, and n^+ source/drain doping. Then, the wafer is deposited with a CVD oxide layer, followed by planarization. Next, using BESOI technology, the device wafer is bonded with the handle wafer. The redundant silicon layer of the device wafer is etched off by grinding and CMP, where the LOCOS field oxide is used as the polishing stopper. After CMP, only the silicon thin-film is left. After oxide depositions, contact formation and metallization, the fabrication procedure is done. In this technology, the source contact is placed directly on the source region and the p-channel region, which functions as the body contact. Thus, floating body effects have been avoided.

2.8 Summary

In this chapter, different SOI technologies have been described. Starting from the evolution of SOI technology, different SOI substrates are described. A 0.25μm SOI CMOS fabrication processing sequence has also been presented, followed by various SOI CMOS device structures. Special-purpose SOI technologies including DRAM, BiCMOS and power have been described in the final portion of this chapter.

References

[1] J. E. A. Maurits, "SOS Wafers— Some Comparisons to Silicon Wafers," *IEEE Trans. Elec. Dev.*, Vol. 25, No. 8, pp. 859-863, Aug. 1978.

[2] H. W. Lam, "Silicon on Insulating Substrates— Recent Advances," *IEDM Dig.*, pp. 348-351, 1983.

[3] S. L. Partridge, "The Current Status of Silicon-On-Insulator Technologies— A Comparison," *IEDM Dig.*, pp. 428-430, 1986.

[4] J.-P. Colinge, "Thin-Film SOI Technology: The Solution to Many Submicron CMOS Problems," *IEDM Dig.*, pp. 817-820, 1989.

[5] A. J. Auberton-Herve, "SOI Technologies Applications: Trends in VLSI," *SOI Conf. Dig.*, pp. 149-150, 1990.

[6] H. Vogt, G. Burbach, J. Belz, and G. Zimmer, "Silicon-on-Insulator Development in Europe," *Sol. St. Tech.*, pp. 79-83, Feb. 1991.

[7] J.-P. Colinge, "Problems and Issues in SOI CMOS Technology," *SOI Conf. Dig.*, pp. 126-127, 1991.

[8] D. Feijoo, A. P. Mills, A. R. Kortan, J. B. Sapjeta, C. M. Hsieh and G. E. Carver, "Comparative Materials Characterization of SOI Wafers Produced by Competing Technologies," *SOI Conf. Dig.*, pp. 38-39, 1993.

[9] S. Kawamura, "Ultra-Thin-Film SOI Technology and its Application to Next Generation CMOS Devices," *SOI Conf. Dig.*, pp. 6-7, 1993.

[10] A. J. Auberton-Herve, "SOI: Materials to Systems," *IEDM Dig.*, pp. 3-10, 1996.

[11] H. H. Hosack, T. W. Houston, and G. P. Pollack, "SIMOX Silicon-on-Insulator: Materials and Devices," *Sol. St. Tech.*, pp. 61-66, Dec. 1990.

[12] G. Ryding, T. H. Smick, M. Farley, B. F. Cordts, R. P. Dolan, L. P. Allen, B. Mathews, W. Wray, B. Amundsen, and M. J. Anc, "The Ibis 1000 SIMOX Production Implanter," *SOI Conf. Dig.*, pp. 436-439, 1997.

[13] K. Izumi, M. Doken, and H. Ariyoshi, "C.M.O.S. Devices Fabricated on Buried SiO_2 Layers Formed by Oxygen Implantation into Silicon," *Elec. Let.*, Vol. 14, No. 18, pp. 593-594, Aug. 1978.

[14] S. Nakashima and K. Izumi, "Analysis of Buried Oxide Layer Formation and Mechanism of Threading Dislocation Generation in the Substoichiometric Oxygen Dose Region," *J. Mater. Res.*, Vol. 8, No. 3, pp. 523-534, March 1993.

[15] T. Nakai, H. Shinyashiki, T. Shingyouji, Y. Yamaguchi, T. Nishimura, and Y. Akasaka, "Reduction of Dislocations in a SIMOX Film by Controlling the Annealing Sequence," *SOI Conf. Dig.*, pp. 120-121, 1991.

[16] J. Jablonski, M. Saito, M. Imai, and S. Nakashima, "Gettering Layer Formation in Low-Dose SIMOX Wafers," *SOI Conf. Dig.*, pp. 34-35, 1995.

[17] S. Nakashima, T. Katayama, Y. Miyamura, A. Matsuzaki, M. Imai, K. Izumi, and N. Ohwada, "Thickness Increment of Buried Oxide in a SIMOX Wafer by High-Temperature Oxidation," *SOI Conf. Dig.*, pp. 71-72, 1994.

[18] Y. Kunii, S. Nanashima, M. Nagase, and K. Izumi, "Reduction in Surface Roughness of SIMOX Substrate by H_2 Annealing," *SOI Conf. Dig.*, pp.42-43, 1996.

[19] C. W. Mueller, and P. H. Robinson, "Grown-Film Silicon Transistors on Sapphire," *IEEE Proc.*, pp.1487-1490, Dec. 1964.

[20] D. C. Mayer, P. K. Vasudev, A. E. Schmitz and R. E. Kastris, "A High-Speed Submicrometer CMOS/SOS Process in Spear Material," *IEDM Dig.*, pp.676-679, 1985.

[21] P. M. Zavracky, D.-P. Vu, and M. Batty, "Silicon-on-Insulator Wafers by Zone Melting Recrystallization," *Sol. St. Tech.*, pp.55-57, Apr. 1991.

[22] T. J. Stultz and J. F. Gibbons, "Arc Lamp Zone Melting and Recrystallization of Si Films on Oxidized Silicon Substrates," *Appl. Phys. Let.*, Vol. 41, No. 9, pp. 824-826, Nov. 1982.

[23] Y. Kobayashi, A. Fukami and T. Suzuki, "Zone-Melting Recrystallization of Polycrystalline Silicon Films on Fused Silica Substrates Using RF-Heated Carbon Susceptor," *IEEE Elec. Dev. Let.*, Vol. 4, No. 5, pp. 132-134, May 1983.

[24] A. J. Auberton-Herve, J. P. Joly, P. Jeuch, J. Gautier, and J. M. Hode, "Device Performances of a Submicron SOI Technology," *IEDM Dig.*, pp. 808-811, 1984.

[25] M. Yoshimi, K. Suguro, M. Takahashi, T. Hamasaki, T. Inoue, T. Yoshii, K. Taniguchi and H. Tango, "Stacked SOI CMOS Fabricated with Seeding Lateral Epitaxy," *Symp. VLSI Tech. Dig.*, pp. 26-27, 1985.

[26] J. B. Lasky, S. R. Stiffler, F. R. White, and J. R. Abernathey, "Silicon-on-Insulator (SOI) by Bonding and Etch-Back," *IEDM Dig.*, pp. 684-687, 1985.

[27] K. R. Sarma, and S. T. Liu, "Silicon-on-Quartz for Low Power Electronic Applications," *SOI Conf. Dig.*, pp. 117-118, 1994.

[28] E. E. King, D. H. Huang, P. Leonov, L. J. Palkuti, G. J. Campisi, H. L. Hughes, and D. J. Godbey, "CMOS on Bonded Wafers Fabricated using a Novel Si-Ge Etch Stop," *SOI Conf. Dig.*, pp. 112-113, 1991.

[29] N. Sato, K. Sakaguchi, K. Yamagata, T. Atoji, Y. Fujiyama, J. Nakayama and T. Yonehara, "High-Quality Epitaxial Layer Transfer (ELTRAN) by Bond and Etch-Back of Porous Si," *SOI Conf. Dig.*, pp. 176-177, 1995.

[30] B. H. Lee, C. J. Kang, J. H. Lee, S. I. Yu, K. W. Lee, K. C. Park and T. E. Shim, "A Novel CMP Method for Cost-Effective Bonded SOI Wafer Fabrication," *SOI Conf. Dig.*, pp. 60-61, 1995.

[31] H. J. Hovel, "Silicon-on-Insulator Substrates: Status and Prognosis," *SOI Conf. Dig.*, pp. 1-3, 1996.

[32] M. Bruel, "Silicon on Insulator Material Technology," *Elec. Let.*, Vol. 31, No. 14, pp. 1201-1202, July 1995.

[33] M. Haond, and O. Le Neel, "Lateral Isolation in SOI CMOS Technology," *Sol. St. Tech.*, pp. 47-52, July 1991.

[34] M. Haond and O. Le Neel, "Rounded Edge Mesa for Submicron SOI CMOS Process," *SOI Conf. Dig.*, pp. 132-133, 1990.

[35] P. V. Gilbert and S.-W. Sun, "A PELOX Isolated Sub-0.5Micron Thin-Film SOI Technology," *Sym. VLSI Tech. Dig.*, pp.37-38, 1995.

[36] T. Ohno, Y. Kado, M. Harada, and T. Tsuchiya, "Experimental 0.25μm Gate Fully Depleted CMOS/SIMOX Process Using a New Two-Step LOCOS Isolation Technique," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 8, pp.1481-1486, Aug. 1995.

[37] C.-L. Huang, and G. J. Grula, "Degradation Characteristics of STI and MESA-Isolated Thin-Film SOI CMOS," *IEEE Elec. Dev. Let.*, Vol. 18, No. 10, pp. 474-476, Oct. 1997.

[38] L. K. Wang, J. Seliskar, T. Bucelot, A. Edenfeld, and N. Haddad, "Enhanced Performance of Accumulation Mode 0.5μm CMOS/SOI Operated at 300K and 85K," *IEDM Dig.*, pp. 679-682, 1991.

[39] Y. Kado, T. Ohno, M. Harada, K. Deguchi and T. Tsuchiya, "Enhanced Performance of Multi-GHz PLL LSIs Using Sub-1/4-micron Gate Ultrathin Film CMOS/SIMOX Technology with Synchrotron X-ray Lithography," *IEDM Dig.*, pp. 243-246, 1993.

[40] G. G. Shahidi, C. Blair, K. Beyer, T. Bucelot, T. Buti, P. N. Chang, S. Chu, P. Coane, J. Comfort, B. Davari, R. Dennard, S. Furkay, H. Hovel, J. Johnson, D. Klaus, K. Kiewtniack, R. Logan, T. Lii, P. A. McFarland, N. Mazzeo, D. Moy, S. Neely, T. Ning, M. Rodriguez, D. Sadana, S. Stiffler, J. Sun, F. Swell, and J. Warnock, "A Room Temperature 0.1μm CMOS on SOI," *Symp. VLSI Tech. Dig.*, pp. 27-28, 1993.

[41] T. Iwamatsu, Y. Yamaguchi, Y. Inoue, T. Nishimura, and N. Tsubouchi, "CAD-Compatible High-Speed CMOS/SIMOX Gate Array Using Field-Shield Isolation," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 11, pp. 1934-1939, Nov. 1995.

[42] J.-P. Colinge, M.-H. Gao, A. Romano, H. Maes and C. Claeys, "Silicon-on-Insulator Gate-All-Around MOS Device," *SOI Conf. Dig.*, pp. 137-138, 1990.

[43] T. Tanaka, H. Horie, S. Ando and S. Hijiya, "Analysis of P^+ Poly Si Double-Gate Thin-Film SOI MOSFETs," *IEDM Dig.*, pp. 683-686, 1991.

[44] D. Hisamoto, T. Kaga, Y. Kawamoto and E. Takeda, "A Fully Depleted Lean-Channel Transistor (DELTA)–A Novel Vertical Ultrathin SOI MOSFET," *IEEE Elec. Dev. Let.*, Vol. 11, No. 1, pp. 36-38, Jan. 1990.

[45] C. T. Nguyen, S. C. Kuehne, P. Renteln, and S. S. Wong, "Quasi-SOI MOSFETs Using Selective Epitaxy and Polishing," *IEDM Dig.*, pp. 341-344, 1992.

[46] I.-K. Kim, W. -T. Kang, J.-H. Lee, S. Yu, S.-C. Lee, K. Yeom, Y.-G. Kim, D.-H. Lee, G. Cha, B. H. Lee, S.-I. Lee, K.-C. Park, T.-E. Shim and C.-G. Hwang, "Advanced Integration Technology for a Highly Scalable SOI DRAM with SOC (Silicon-On-Capacitors)," *IEDM Dig.*, pp. 605-608, 1996.

[47] S. Nakamura, H. Horie, K. Asano, Y. Nara, T. Fukano, and N. Sasaki, "Giga-bit DRAM Cells with Low Capacitance and Low Resistance Bit-Lines on Buried MOSFET's and Capacitors by Using Bonded SOI Technology– Reversed-Stacked-Capacitor (RSTC) Cell-," *IEDM Dig.*, pp. 889-892, 1995.

[48] K. Terada, T. Ishijima, T. Kubota, and M. Sakao, "A New DRAM Cell with a Transistor on a Lateral Epitaxial Silicon Layer (TOLE Cell)," *IEEE Trans. Elec. Dev.*, Vol. 37, No. 9, pp. 2052-2057, Sept. 1990.

[49] W.-L. M. Huang, K. M. Klein, M. Grimaldi, M. Racanelli, S. Ramaswami, J. Tsao, J. Foerstner, and B.-Y. C. Hwang, "TFSOI Complementary BiCMOS Technology for Low Power Applications," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 3, pp. 506-512, March 1995.

[50] R. S. Ronen, M. R. Splinter, and R. E. Tremain, "High-Voltage SOS/MOS Devices and Circuit Elements: Design, Fabrication, and Performance," *IEEE J. Sol. St. Ckts*, Vol. 11, No. 4, pp. 431-442, Aug. 1976.

[51] S. Matsumoto, T. Yachi, H. Horie, and Y. Arimoto, "A Novel High-Speed Quasi-SOI Power MOSFET with Suppressed Parasitic Bipolar Effect Fabricated by Reversed Silicon Wafer Direct Bonding," *IEDM Dig.*, pp. 949-951, 1996.

Problems

1. In the SIMOX process, during the thermal anneal step, for forming the buried oxide with incorporating different oxygen doses, what are the differences? In a general SIMOX wafer, what behaviors may change the quality of the silicon thin-film and the buried oxide? How to improve them?

2. In ZMR SOI technology, how the seeds for recrystallization are formed? What is the purpose of capping oxide? What are the heat sources to melt the polysilicon layer?

3. Compare the differences in the processing sequences between BESOI and smart-cut SOI. Which technique has a better performance in throughput and cost?

4. Compare the tradeoffs between LOCOS and mesa isolation for SOI technology. How to improve them?

5. What is the purpose of the nitrogen-doped polysilicon layer in the 0.25μm SOI CMOS technology described in this chapter?

6. What are methods to provide body contacts for partially-depleted devices? What are the tradeoffs?

7. In the BiCMOS technology, what is the purpose of the sacrificial oxide? What are the purposes of the polysilicon spacer and the oxide spacers? In the lateral BJT, what factors control the formation of the base profile?

Chapter 3

SOI CMOS Circuits

In the previous chapter, SOI technology has been described. Due to the unique oxide isolation structure, SOI CMOS devices are latchup-free. In addition, parasitic capacitances are small. Better subthreshold characteristics and transconductance characteristics can be expected from SOI CMOS devices. Furthermore, reduced leakage currents and good radiation hardness are strong points of SOI CMOS devices. As shown in Fig. 3.1, due to the unique structure, device density of an SOI CMOS circuit can be enhanced substantially, as compared to the bulk CMOS circuit[1]. As shown in the figure, NMOS and PMOS SOI devices can be placed adjacent to each other. Therefore, in the future of the circuit design for VLSI, SOI is an important technology. In this chapter, SOI CMOS circuits are described.

3.1 Floating Body Effects

SOI CMOS devices are especially suitable for designing low-voltage CMOS circuits. However, there are some peculiar behaviors in the circuits using SOI CMOS devices. For partially-depleted SOI CMOS devices, the floating body induced parasitic BJT effects may cause substantial influences in the circuit performance. Fig. 3.2 shows a static three-way OR-AND logic circuit using partially-depleted SOI CMOS devices with a channel length of 0.25μm, a front gate oxide of 50Å, a buried oxide of 3500Å, and a silicon thin-film of 1400Å, at $V_{DD} = 2.5V$[2]. As shown in the figure, the inputs V_{in2}, V_{in3}, V_{in4} are maintained at 0V and the input V_{in1} is at 2.5V. At $t = 0.5ns$, when V_{in1} changes from 2.5V to 0V, due to gate/source capacitance coupling of N_1, the voltage at the internal node V_1 drops from $2.31V$ $(2.5V - V_{TH})$ to 1.79V. The body voltage of N_1 ($V_{B,N1}$) changes from 2.33V to 0.98V. At this time, the body voltage of N_2 ($V_{B,N2}$) maintains at 2.3V. After $t = 1.0ns$, V_{in4} switches from 0V to 2.5V, hence, N_4 is on. Therefore, V_1 is pulled low to 0V. Due to source/body

J. B. Kuo et al., *CMOS VLSI Engineering*

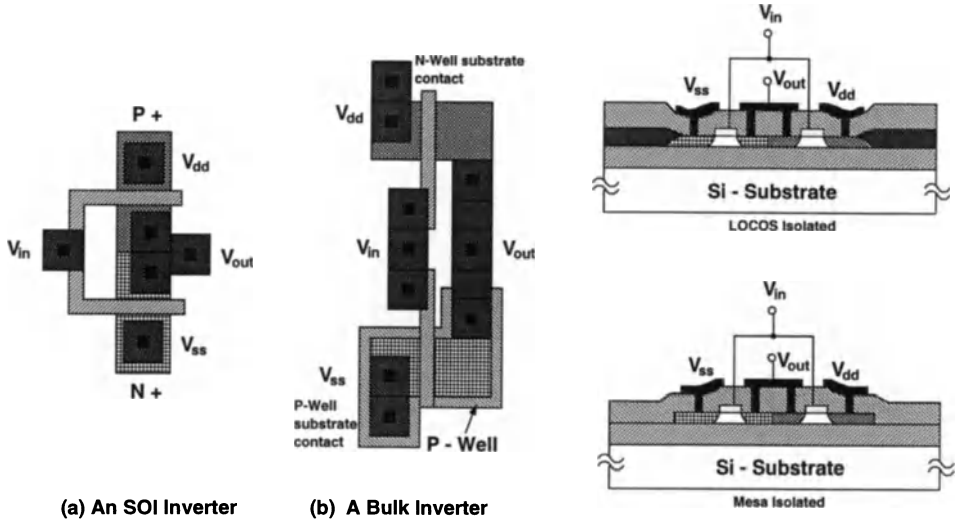


Figure 3.1: CMOS inverters based on SOI and bulk CMOS technologies.

capacitance coupling, the body voltage of N_1 ($V_{B,N1}$) changes from 0.98V to below 0.7V. Similarly, the body voltage of N_2 ($V_{B,N2}$) also drops from 2.3V due to source/body capacitance coupling. However, the final value of $V_{B,N2}$ is still high enough to turn on the body/source diode ($V_{B,N2} - V_1 > 0.7V$). Therefore, the parasitic BJT is triggered. Although the gate voltage of N_2 is low, a substantially large leakage current exists in N_2 ($I_{BIP,N2}$), which has a peak value of 0.4mA at 1.0ns and gradually decreases until the surplus holes in N_2 are used up. N_3, which is similar to N_2, also has a substantial amount of leakage current. On the other hand, for N_1, its body voltage becomes very small at $t = 0.5ns$. Hence, at $t = 1.0ns$, the body voltage of N_1 ($V_{B,N1}$) is not big enough to turn on its body/source diode. Therefore, no substantial amount of leakage current due to the parasitic BJT effect as for N_2 and N_3 exists in N_1. At the output node of the circuit, due to the existence of the DC path for this static circuit, the transient leakage currents such as $I_{BIP,N2}$, $I_{BIP,N3}$ do not affect its output transient waveform substantially. Instead, the transient leakage currents only raise its power consumption during the transient.

For any dynamic logic circuit, transient leakage current may cause serious effects. Fig.3.3 shows Manchester carry chain circuit and its switching transients for the input generate signals (G_4, G_3, G_2, G_1)=(0,0,0,0), the propagate signals (P_4, P_3, P_2,

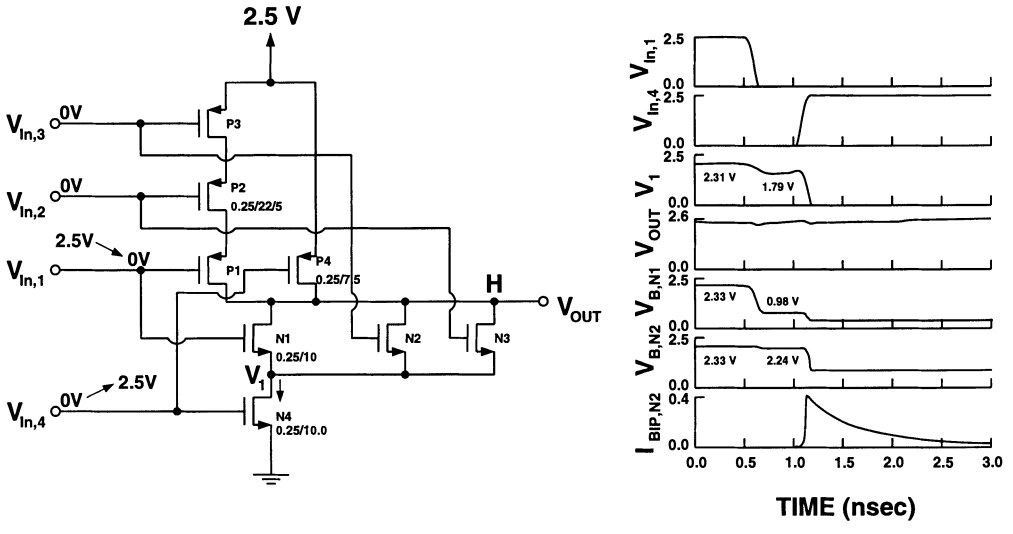


Figure 3.2: Static three-way OR-AND logic circuit and its switching transient, which uses SOI CMOS devices with a channel length of 0.25μm, a front gate oxide of 50Å, a buried oxide of 3500Å, and a silicon thin-film of 1400Å, at $V_{DD} = 2.5V$.

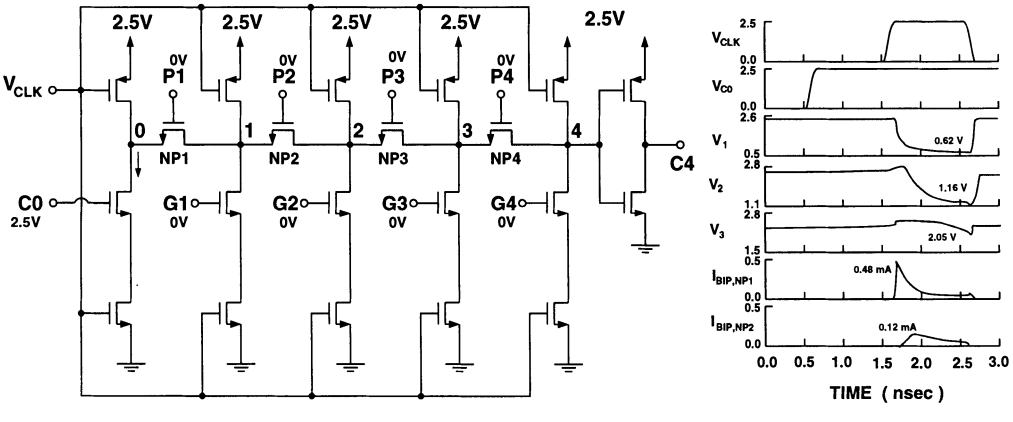


Figure 3.3: Manchester carry chain circuit and its switching transients for the input generate signals (G_4, G_3, G_2, G_1)=(0,0,0,0) and the propagate signals (P_4, P_3, P_2, P_1)=(0,0,0,0), and the input carry signal ($C_0 = 1$) using SOI CMOS devices.

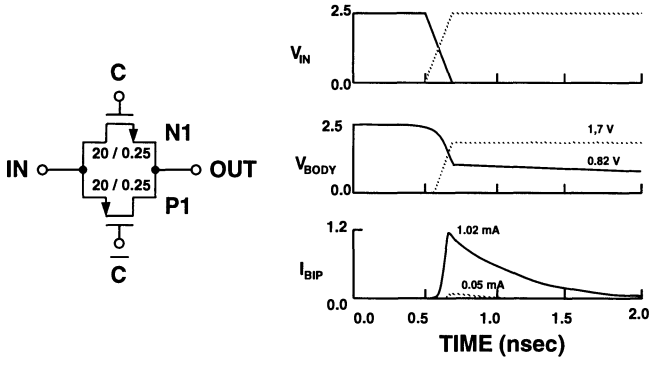


Figure 3.4: SOI CMOS pass-gate with its pertinent switching waveforms.

P_1)=(0,0,0,0), and the input carry signal ($C_0 = 1$) using SOI CMOS devices[2]. As shown in the figure, when clock is low at 0V, it is the precharge period. When clock is 2.5V, it is the evaluation period. Before clock becomes high, P_1, P_2, P_3, P_4 and G_1, G_2, G_3, G_4 maintain at 0V and the input carry signal C_0 is 2.5V. When clock becomes 2.5V, the voltage at node 0 (V_0) is pulled low to 0V. For the pass transistor N_{p1}, the sudden fall in the source voltage may turn on the body/source diode. As a result, the leakage current due to the parasitic BJT effect in N_{p1} (I_{BIP}, N_{p1}) may rise substantially. Therefore, the voltage of node 1 (V_1), which was precharged to 2.5V, may be pulled low to 0.62V, which represents $\overline{C_1}$. Hence, this leakage current already causes an error in $\overline{C_1}$. Similarly, the drop in V_1 may cause a non-negligible leakage current ($I_{BIP,N2}$) due to the parasitic BJT effect in N_{P2}. As a result, V_2 falls from 2.5V to 1.16V, which also causes an error in $\overline{C_2}$. Consequently, the leakage current effect propagates from one bit to the other. However, its effect becomes smaller as it propagates. When it reaches N_{p3}, its effect becomes much smaller. Therefore, the change in V_3 ($\overline{C_3}$) becomes much less drastic.

Similar floating body effect also exists in SOI CMOS pass-gates. As shown in Fig. 3.4[2], when C is low, $\overline{C}$ is high. The transmission gate is off. However, if V_{in} switches from high to low, the body/source diode of the NMOS device may turn on. Due to the parasitic BJT effect, a large leakage current (I_{BIP}) exists in the NMOS device. Similarly, when V_{in} changes from low to high, a large leakage current due to the parasitic BJT effect may exist in the PMOS device. This leakage current can

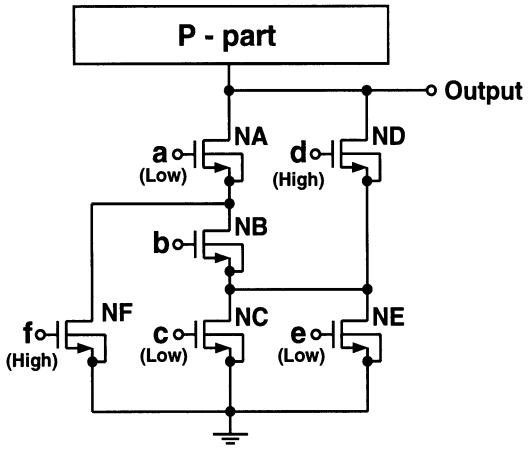


Figure 3.5: A switch network logic with inputs (a,b,c,d,e,f)=(0,0,0,1,0,1).

not be overlooked when designing circuits using SOI CMOS devices. Comparing NMOS with PMOS, the leakage current in the SOI PMOS device is smaller since the parasitic PNP BJT effect in the PMOS device is smaller than the parasitic NPN BJT effect in the SOI NMOS device.

The leakage current caused by the floating body effect can be overcome by tying the body to the source. Fig. 3.5 shows a switch network logic with body/source connected to inhibit the floating body effect[3]. However, when the inputs a, c, e are low and d, f are high, no matter what the potential of b is, the current path of ND-NB-NF is formed since NB can be regarded as a forward biased drain/body diode. When designing circuits using SOI CMOS devices, this phenomena should be avoided.

3.2 Low-Voltage SOI Circuits

Fig. 3.6 shows the dynamic threshold voltage MOS (DTMOS) technique[4]. As shown in the figure, the body of the NMOS device is connected to the gate. As shown in Fig. 3.7, the threshold voltage of the SOI NMOS device is lowered when a positive body bias is applied. Specifically, if the body is tied to the gate, its

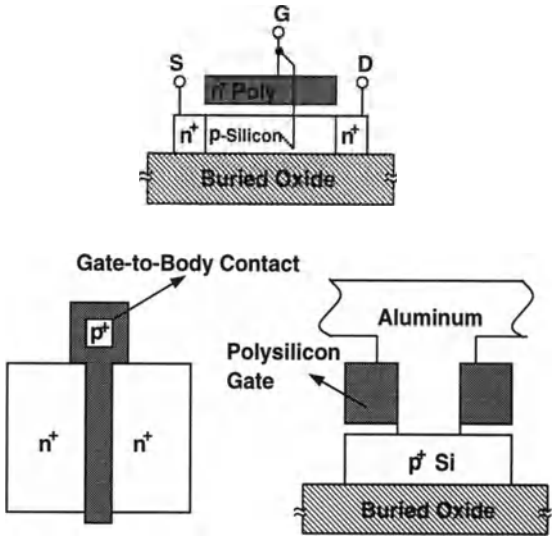


Figure 3.6: The SOI NMOS device with its body tied to gate.

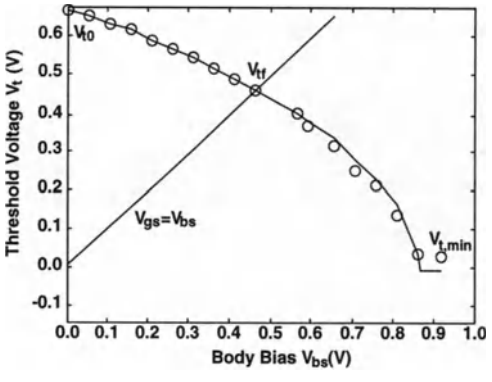


Figure 3.7: Threshold voltage versus body-source voltage of an SOI NMOS device.

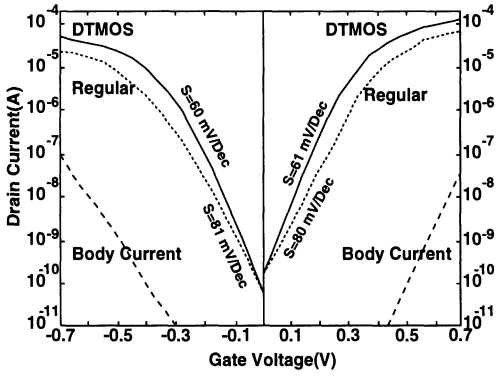


Figure 3.8: Subthreshold characteristics of SOI NMOS and PMOS devices (DTMOS and standard) operating with body grounded and body tied to the gate.

threshold voltage can be lowered by about 0.15V, which can provide a larger gate overdrive voltage. As shown in Fig. 3.7, by tying the body to the gate, due to a drop in the threshold voltage, the gate overdrive voltage becomes larger[4]. During the turn-on period, its threshold voltage becomes smaller. During the turn-off period ($V_G = 0$), its threshold voltage maintains its value— the leakage current is small and the overall subthreshold slope is steep as shown in the following figure. Fig. 3.8 shows the subthreshold characteristics of SOI NMOS and PMOS devices operating with body grounded and body tied to the gate[4]. As shown in the figure, for the standard NMOS device, its body is grounded. Compared with standard devices, at a low gate voltage, the leakage current of the DTMOS device is about identical. At a high gate voltage, the drain current of the DTMOS device is 2x the value of that for the standard device due to a smaller threshold voltage and a smaller vertical electric field at a high gate voltage—the mobility can be enhanced. In addition, the subthreshold slope of the DTMOS device is improved. However, at a small gate voltage, the diode leakage cannot be overlooked— the operating voltage of the DTMOS device cannot be high. In order to improve the operation region for the DTMOS device, as shown in Fig. 3.9, a limiter device is placed between the body and the gate to provide forward bias for the DTMOS device[5]. When the input voltage (V_{in}) is high, the voltage drop of the body/source diode is smaller than 0.6V. Other voltage drops are absorbed by the limiter device.

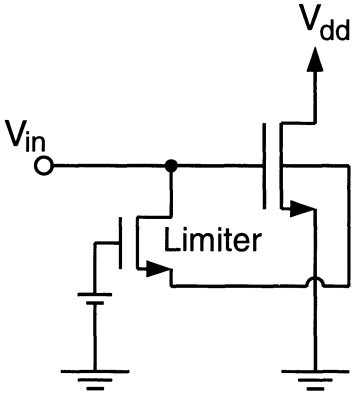


Figure 3.9: A limiter device is used to provide a forward bias for the DTMOS device.

In general, speed performance of the circuit using the DTMOS technique can be enhanced. In addition, owing to lowering of the threshold voltage during the transient, this SOI CMOS inverter circuit is suitable for low voltage operation. On the other hand, this SOI circuit also has weaknesses. Since body is connected to gate, therefore, the previous stage, which drives the gate, needs to absorb the extra body leakage current. In addition, if no limiter device is used in the DTMOS structure, the supply voltage is limited to below 0.6V such that the forward bias of the body-source junction can be avoided. Otherwise, when the body-source junction is forward biased, a large current may flow through the source contact.

In order to overcome the weakness of the SOI CMOS inverter with its body tied to gate as shown in Fig. 3.9, Fig. 3.10 shows an SOI CMOS inverter with the dynamic threshold voltage[6]. As shown in the figure, two auxiliary transistors driven by the input gate voltage are added to connect the bodies to the drain. With this circuit configuration, the previous stage circuit, which drives the gate, does not need to absorb the body leakage current any more. The operation of this SOI CMOS inverter is described here. During the pull-down transient, the input switches from low to high. Under this situation, both main and auxiliary NMOS devices turn on. If the output load capacitance is much larger than the body capacitance of the main transistor, the body potential of the main transistor will be pulled to high by the auxiliary transistor (Note that at the time the output node is not pulled low yet). Therefore, the threshold voltage of the main transistor drops. As a result, a larger

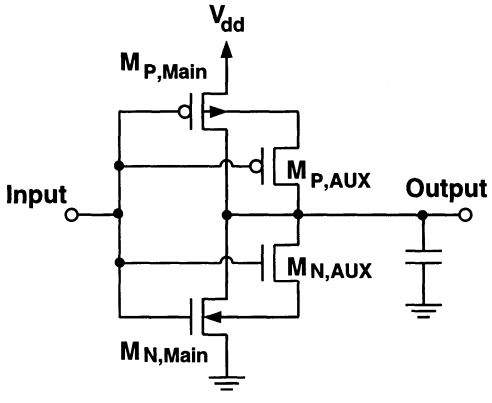


Figure 3.10: An SOI CMOS inverter with the dynamic threshold voltage.

drain current of the main transistor pulls the output to low faster. Owing to the turn-on of the auxiliary transistor, the body potential of the main transistor will also drop in accordance with the fall of the output voltage. Therefore, the threshold voltage of the main transistor rises again. When the output voltage reaches the ground level, the body potential is also 0V. At this time, the threshold voltage is restored to its zero-body-bias value. When the input switches to low, both main and auxiliary NMOS transistors turn off. Under this situation, body potential of the main NMOS transistor remains at ground and its threshold maintains its maximum value— minimum leakage current. The internal potential distribution in the body of the main transistor depends on the distance from the body contact. Due to the RC effect, at a location farther away from the body contact in the silicon thin-film of the main transistor, its body potential is less influenced by the auxiliary transistor. Therefore, a main transistor with a smaller equivalent RC time constant of the thin-film region can receive more benefits from the dynamic threshold effect. In addition, the body potential is also influenced by the coupling via the gate-body capacitance and the clock feedthrough via the auxiliary transistor. This SOI CMOS inverter circuit with dynamic threshold voltage is especially suitable for driving a large capacitive load.

The previous SOI CMOS inverter can be further improved. Fig. 3.11 shows an SOI CMOS buffer[7]. For the SOI CMOS inverter used in a large VLSI system, there may be a chain of cascading inverters involved. The propagation delay be-

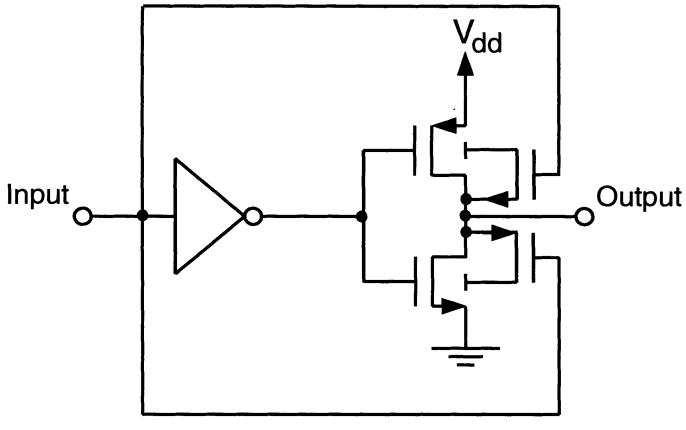


Figure 3.11: An SOI CMOS buffer.

tween inverters may be substantial. As shown in Fig. 3.10, the auxiliary transistors, which are used to lower the threshold voltage of the main transistors, are driven by the input voltage. The propagation delay may defer the function of the auxiliary transistor. As a result, the speed enhancement of the SOI CMOS inverter as shown in Fig. 3.10 is not fully utilized. As shown in Fig. 3.11, if the gates of the auxiliary transistors are controlled by the input signal to the previous stage instead of the present stage, the auxiliary transistor can function in time to shrink the threshold voltage of the main transistor during the transient of the present stage[7]. As a result, the dynamic threshold voltage technique can be fully utilized. In order to accommodate this new technique, the SOI circuit also needs to be modified accordingly. First, the NMOS and the PMOS auxiliary devices should be reversed such that the inverting function of the previous state can be taken into account. Therefore, including the function of the inverter of the previous stage, the whole circuit becomes the SOI CMOS buffer with dynamic threshold voltage.

Fig. 3.12 shows a 0.5V multi-threshold SOI CMOS logic circuit[8]. As shown in the figure, this SOI CMOS circuit is composed of two portions— the power switch transistor and the logic block. In the logic block, all transistors are fully-depleted SOI CMOS devices with a smaller magnitude in the threshold voltage. The supply to the logic block is called virtual V_{DD}, which is connected to V_{DD} of 0.5V via the power switch transistor. The power switch transistor is a partially-depleted

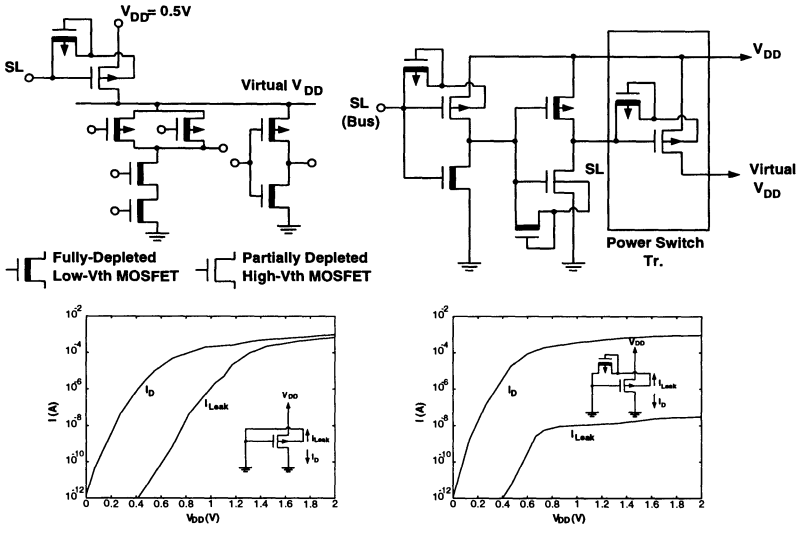


Figure 3.12: 0.5V multi-threshold CMOS logic circuit.

SOI MOS device with a larger threshold voltage. During the sleep mode, the power switch transistor is turned off to save power. The larger threshold voltage guarantees a smaller leakage current in the turned-off power switch transistor. As shown in the figure, a diode-connected auxiliary fully-depleted SOI MOS device based on the dynamic threshold voltage technique has been used to tie the body of the partially-depleted power switch transistor to gate. As a result, during the turn-on period its threshold voltage can be lowered. When the virtual V_{DD} is connected to V_{DD}, its voltage difference between V_{DD} and virtual V_{DD} can be small. In addition, as shown in the figure, this diode connected auxiliary MOS device can be used to reduce the leakage current of the DTMOS device at a large V_{DD}. In the driver circuit for the power switch, in order to increase the driving capability and to reduce the leakage current, the improved DTMOS structure has also been used.

3.3 SOI Gate Arrays

As described in the previous section, for partially-depleted SOI CMOS devices, floating body effect may cause serious degradation in circuit performance. By applying body contact to the partially-depleted SOI CMOS devices, the floating body problems can be lessened. For fully-depleted SOI CMOS devices, no body contacts are

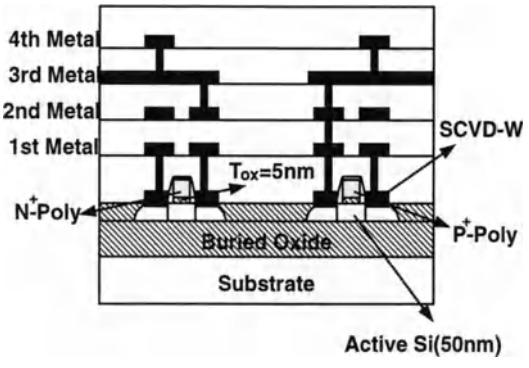


Figure 3.13: Cross section of the device structure of a gate array using fully-depleted SOI CMOS devices.

required. As a result, device density can be high, which is especially advantageous for gate array applications. Fig. 3.13 shows the cross section of the device structure of a gate array using fully-depleted SOI CMOS devices[9]. It is based on a 0.25μm SOI CMOS technology, which has a silicon thin-film thickness of 500Å, four layer metal interconnects, N^+ poly for NMOS and P^+ poly for PMOS.

Fig. 3.14 shows the basic cell structures used in SIMOX and bulk CMOS gate arrays using a 0.25μm fully-depleted SIMOX SOI CMOS technology[10]. As shown in the figure, the basic cells contain 10 normal-sized and small-sized CMOS devices. The normal-sized devices are used for logic gates. The small-sized PMOS devices are used as the load transistor in SRAMs. The small-sized NMOS devices are used as the transmission gate transistors. Using this basic cell, a 2-input NAND gate or a 2-port 6T SRAM cell can be realized.

Fig. 3.15 shows the basic cell and its arrangement in the sea of gates (SOG) configuration using a fully-depleted SOI CMOS technology[11], where a 400Å silicon thin-film, and two-layer metal interconnects have been used. The arrangement of the cells is via the sea of gates (SOG), where the sizes of both NMOS and PMOS are identical. NMOS and PMOS devices are located in different silicon islands. Between silicon islands, LOCOS is used for isolation. In the same silicon island, between active devices, isolation is via gate isolation— the devices next to the active devices are turned off. Fig. 3.16 shows the propagation delay time as a function of

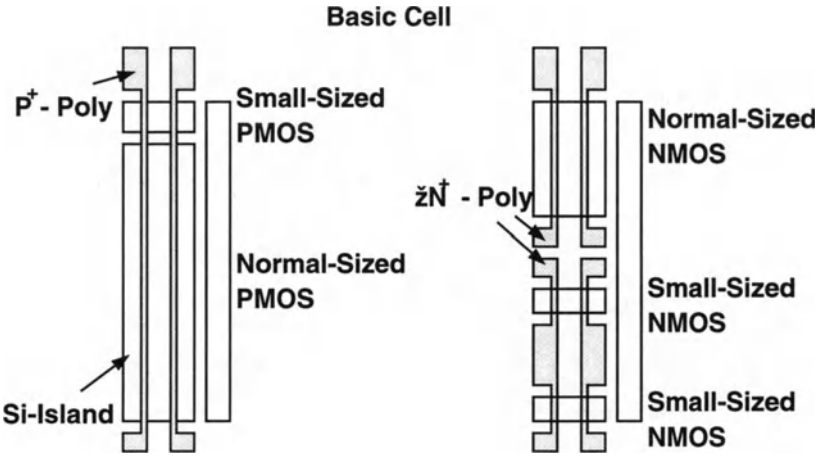


Figure 3.14: Basic cell structures used in SIMOX and bulk CMOS gate arrays.

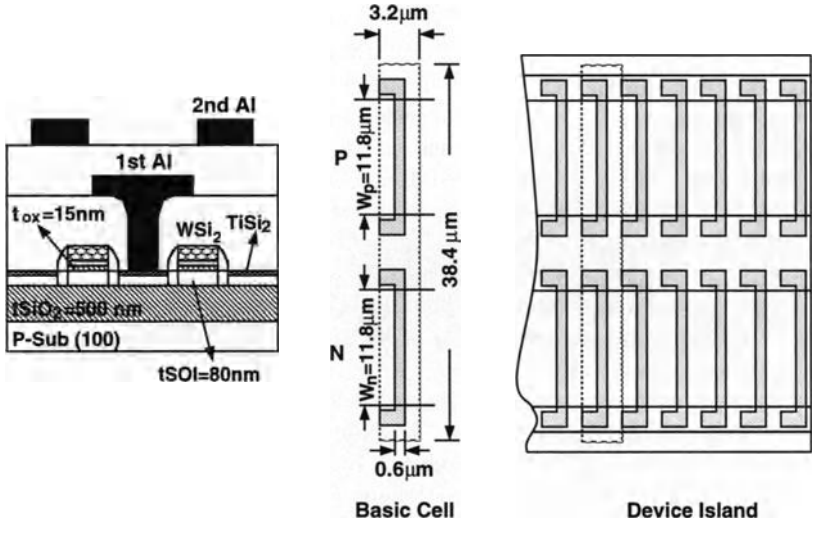
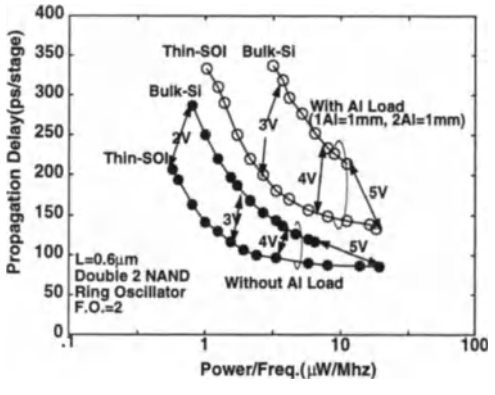


Figure 3.15: The basic cell and its arrangement in the sea of gates (SOG) configuration using a fully-depleted SOI CMOS technology.



	C (SOI)	C (bulk)	C(SOI)/C(bulk)
Active Gate (F.O.=1) C_{ox}	36.6fF	37.6fF	0.97
N^+Junction (1 drain) $C_{J(n)}$	9.5fF	18.9fF	0.50
P^+ Junction (1 drain) $C_{J(p)}$	7.6fF	21.6fF	0.35
Polysilicon (10μm²) C_{Poly}	0.43fF	0.98fF	0.44
1st Aluminum (1mm) C_{1Al}	72.6fF	123.2fF	0.59
2nd Aluminum (1mm) C_{2Al}	63.9fF	98.4fF	0.65

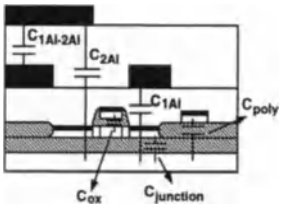


Figure 3.16: Propagation delay time as a function of power consumption of each gate in fully-depleted SOI and bulk-silicon 2-NAND ring oscillators with and without Al load capacitance, in which the power consumption is normalized by the oscillation frequencies of the ring oscillators.

power consumption of each gate in fully-depleted SOI and bulk-silicon 2-NAND ring oscillators with and without Al load capacitance, in which the power consumption is normalized by the oscillation frequencies of the ring oscillators[11]. As shown in the figure, at the same power, the speed of the SOI circuit is 1.4 times faster since the parasitic capacitance of the SOI circuit is one half of the bulk one.

Although fully-depleted SOI CMOS devices have many advantages, especially a much smaller floating-body effect, partially-depleted SOI CMOS devices have been gaining a lot of attention owing to their much smaller threshold voltage sensitivity to the silicon thin-film thickness and source/drain resistance. Therefore, they have also been used to realize gate arrays. Fig. 3.17 shows the basic-cell structures for a gate array using a 0.35μm partially-depleted SOI CMOS technology[12]. As shown in the figure, the sea-of-gate arrangement has been adopted. In addition, it adopts the field-shielded isolation technique with the neutral body of the partially-depleted SOI CMOS devices connected to the ground or V_{DD} via the silicon thin-film region under the field-shielded gate. As shown in the figure, from the layout arrangement point of view, this partially-depleted SOI CMOS gate array is similar to the bulk CMOS one. Therefore, the circuits designed for the bulk CMOS gate arrays can be

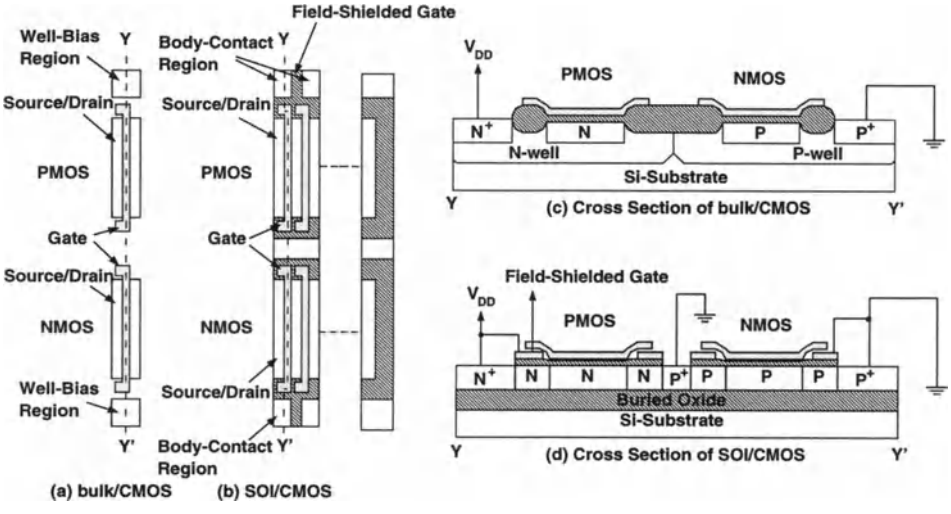


Figure 3.17: Basic-cell structures for a gate array using a 0.35μm partially-depleted SOI CMOS technology.

transferred directly for use in the SOI CMOS gate arrays. As shown in the figure, since impact ionization is quite serious for the fully-depleted SOI NMOS devices, hence, body contacts have been arranged at the two sides of the NMOS devices. In contrast, in the SOI PMOS devices, there are body contacts only at one side.

Fig. 3.18 shows the macro-cell placement for a partially-depleted SOI CMOS gate array[12]. As shown in the figure, metal interconnect lines have been placed vertically and horizontally. In the enlarged portion of this figure, the layout for an inverter has been shown. As shown in the figure, at both sides of the active MOS devices there are inactive MOS devices— the gate of the PMOS device is connected to V_{DD} and the gate of the NMOS device is connected to ground. The bodies of PMOS and NMOS devices are connected to V_{DD} and ground, respectively.

For partially-depleted SOI CMOS gate arrays, body-contacts are necessary. With body contacts, the high-density advantages may have been sacrificed a little bit. On the other hand, with body contacted, the unstable performance of the circuits can be improved. Fig. 3.19 shows the frequency dependence of the delay time of a circuit using a gate array with its body floating and tied, operating at 1V and -50C[13]. As shown in the figure, with body contacts, the speed performance has been improved

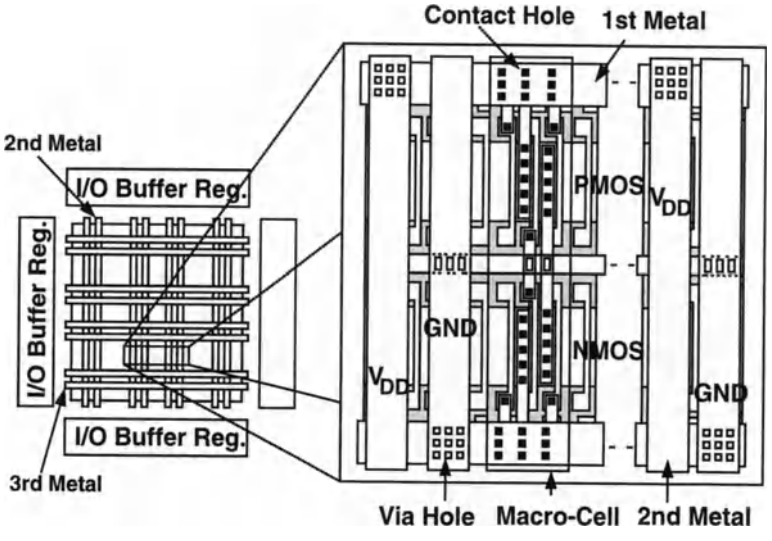


Figure 3.18: Macro-cell placement for a partially-depleted SOI CMOS gate array.

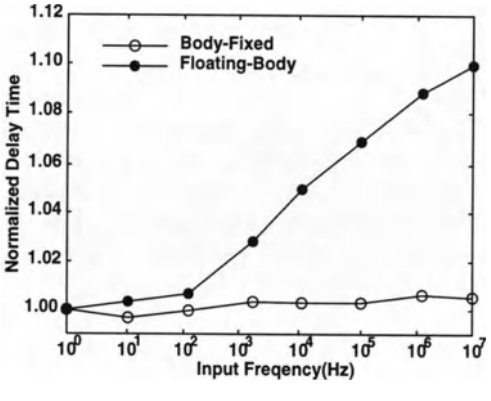


Figure 3.19: Frequency dependence of the delay time of a circuit using a gate array with its body floating and tied, operating at 1V and -50C.

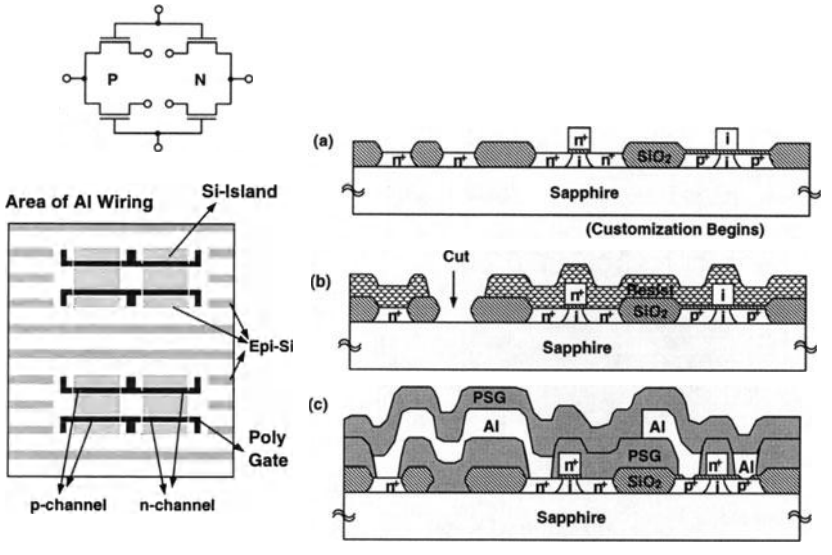


Figure 3.20: A CMOS/SOS gate array with a customization technique of cutting.

substantially.

Due to the excellent isolation property of the SOI CMOS devices, the silicon thin-film itself can be used for wiring. Fig. 3.20 shows a CMOS/SOS gate array with a customization technique of cutting[14]. As shown in the figure, in addition to the active device region, the silicon thin-films have also been used as the lateral interconnect lines. Via proper wire cutting, contact opening and aluminum patterning, the N^+ silicon thin-film lines are used for interconnects. Also shown in the figure is the detailed cutting procedure. After patterning the photoresist, the exposed oxide layer of the N^+ silicon thin-film lines are removed, followed by etching of the silicon thin-film layer. The wire cutting procedure does not complicate the processing sequence substantially.

3.4 SOI SRAM

Owing to its superior capabilities in radiation hardness, parasitic capacitances, and device isolation, SOI CMOS technology has been used to implement SRAMs. As shown in Fig. 3.21, in the SOI SRAM cell, PMOS and NMOS devices can be placed

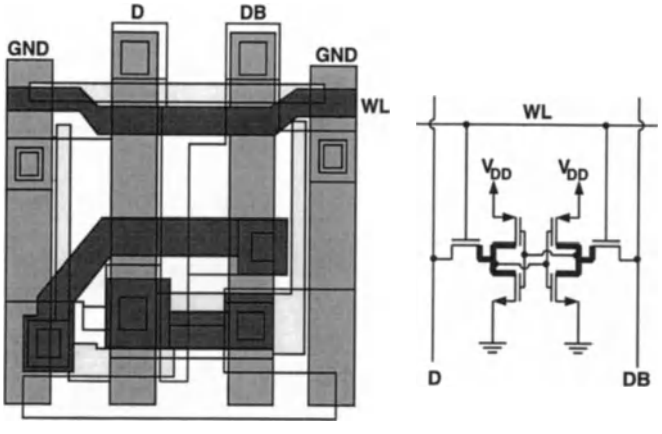


Figure 3.21: Layout of an SOI SRAM cell.

against one another without isolation problems[15]. The drain of the NMOS device can be placed adjacent to that of the PMOS device in the inverter. Therefore, the memory cell of the SOI SRAM can be much smaller than that of the bulk one.

As shown in Fig. 3.22, at a large V_{DS}, the subthreshold slope of a partially-depleted SOI NMOS device becomes better due to floating body effect. Therefore, its threshold voltage can be scaled down more easily[16]. Under low-voltage low-power requirements, SOI technology is especially suitable for SRAM cells. However, due to the kink effect from the floating body structure, its output conductance may be degraded. In order to lessen the kink effect, body contact should be arranged for the partially-depleted SOI CMOS devices. This figure also shows the access time versus supply voltage of a 512Kb SRAM using 0.2μm partially-depleted SOI CMOS technology. At 1V, the access time is 3.5ns at a power consumption much smaller than bulk SRAM with a comparable size. From this figure, the potentials of the SOI technology for low-voltage low-power SRAM applications can be seen.

Fig. 3.23 shows the schematic diagram of an SRAM cell, column, and main sense amplifier circuits in a typical SOI CMOS SRAM[17]. As shown in the figure, in order to save the cell area, no body contacts are available for the memory cell. In the bit-line related circuits, the body of the pass transistor is grounded. In the sense amplifier and other biasing circuits, the body-tied-to-source configuration has been

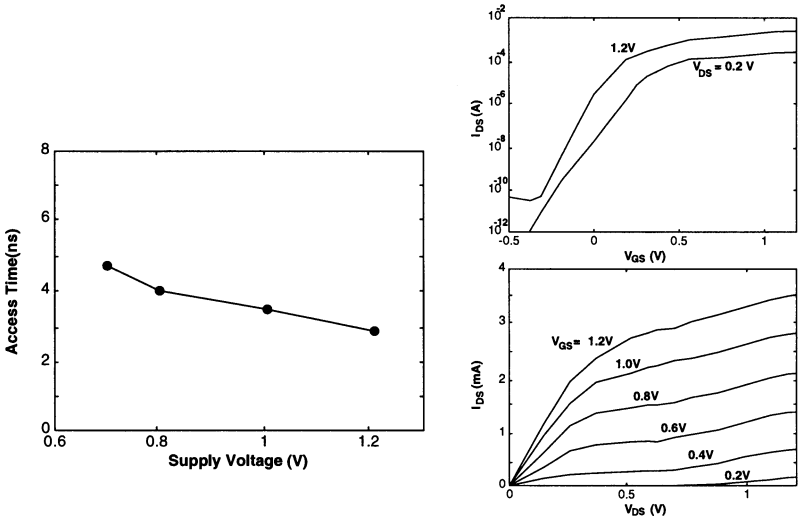


Figure 3.22: Access time versus supply voltage of a 512Kb SRAM using 0.2μm partially-depleted SOI CMOS technology.

used such that its output conductance hence the gain can be maintained at a high value without the influence from the kink effect.

The parasitic BJT effect due to the floating body structure in the memory cell can degrade the performance of an SRAM. For the memory cell and the column structure as shown in Fig. 3.24, its 'write 0' transient for the memory cell 0 is shown in Fig. 3.25[18]. In the figure, 'max' is referred to 'data 1' stored in cell 1-511 such that node A in the memory cell is high. 'min' is referred to 'data 0' stored in cell 1-511 such that node A in the memory cell is low. When the 'write 0' procedure is initiated, word line LWL becomes high. At this time, via the read/write switch, the input data (DIN=0) forces the bit line (BL) to pull low. The pass transistor of cell 0 is turned on. Therefore, node A is pulled low. The 'write 0' function is accomplished. Comparing the transient waveforms referred to 'min' and 'max', for the max case 'write 0' takes a longer time. This is due to the fact that for the 'max' case, the drain node (A) of the pass transistor (T1) in cell 1-511 maintains high. When the source end (at BL) of T1 becomes from high to low, the substantial leakage current due to the parasitic BJT results in an increased load at the bit line (BL). Consequently, the pull-down of the bit line (BL) becomes slower. Therefore,

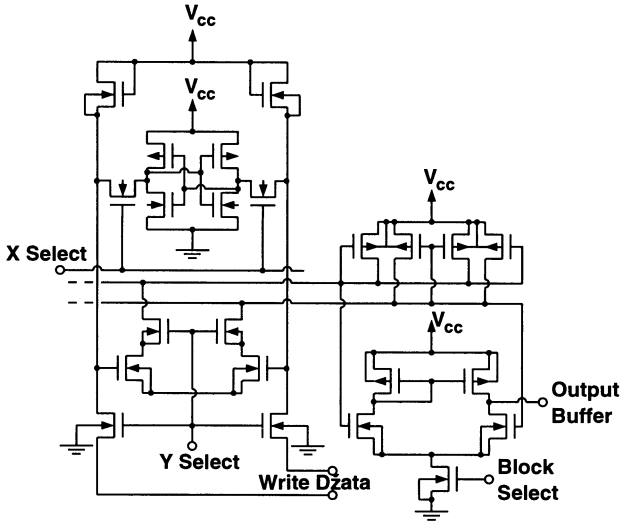


Figure 3.23: Schematic diagram of SRAM cell, column, and main sense amplifier circuits in a CMOS SOI 4K SRAM.

'write 0' is slower. For the 'min' case, no such situation occurs. Since for the 'min' case, node A in cell 1-511 maintains low. No leakage as in the 'max' case exists. Therefore, speed is faster. Fig. 3.25 also shows the transient voltage and currents of a single unselected cell for the 'max' case of the unselected cell disturb during a write cycle at $V_{DD} = 1.95V$ and 105C[18]. As shown in the figure, when 'write 0' is initiated, a leakage current indicated by i_e is injected into BL. In contrast, a leakage current indicated by i_c is flowing out of node A. As a result, node A is pulled low a little bit. Due to the DC path of the memory cell, the extent of the voltage perturbation at node A is not large. However, when designing the memory cell, the aspect ratio of the PMOS devices should be arranged carefully such that the leakage current from the parasitic BJT does not change the potentials at the storage nodes.

In some SRAM designs, SOI devices and bulk devices are simultaneously used. Fig. 3.26 shows the memory cell of an SRAM using laser-recrystallized SOI PMOS load[19]. As shown in the figure, in the memory cell, bulk NMOS devices and SOI PMOS load are used. The SOI PMOS load is realized by the laser recrystallization of the CVD deposited polysilicon layer. In this memory cell, the P^+ poly-gate of the PMOS device is connected directly to the drain of the NMOS device, which has

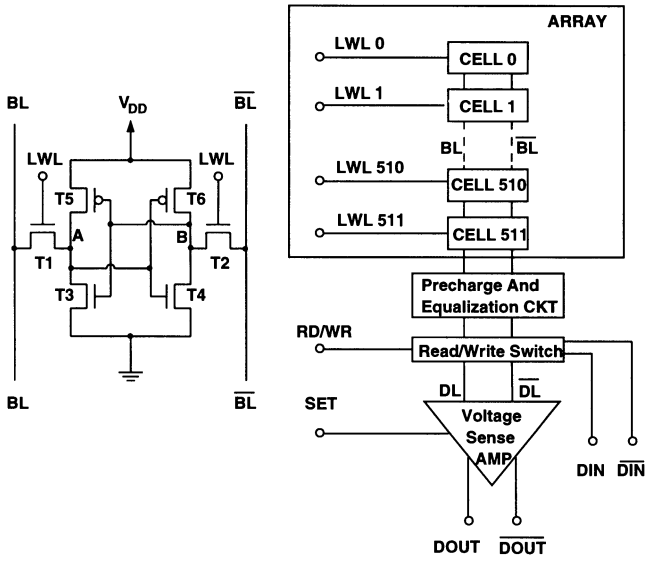


Figure 3.24: Block diagram of an SOI SRAM column and its memory-cell.

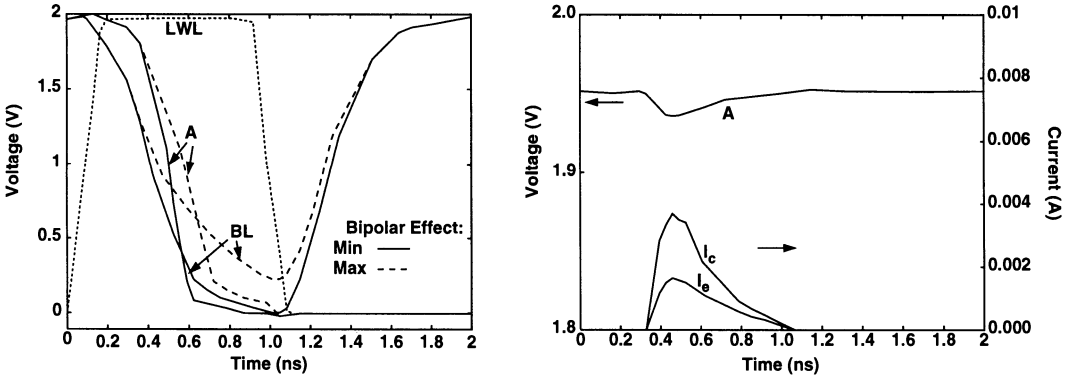


Figure 3.25: Transients of a selected and an unselected cell disturb during a write cycle at $V_{DD} = 1.95V$ and 105C.

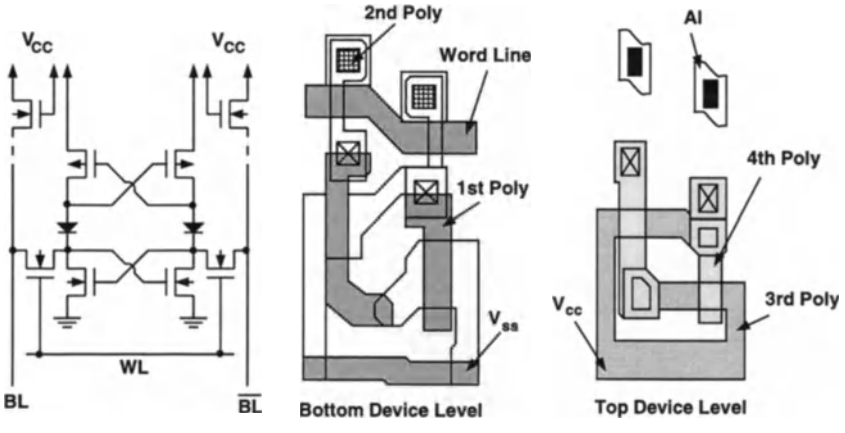


Figure 3.26: The memory cell of an SRAM using laser-recrystallized SOI PMOS load.

an N^+ poly-gate. As a result, effective diodes exist in the memory cell. As shown in Fig. 3.27, bulk NMOS devices are at the bottom level[20]. At the top level is the SOI PMOS load. Compared to the SRAM cell using polysilicon TFT as the load, the SOI PMOS load has a much smaller leakage current and a much larger turn-on current. Therefore, its performance is much better.

Three-dimensional IC technology has been used to realize SRAM. Fig. 3.28 shows the circuit diagram of a 3D SRAM[21]. As shown in the figure, at the bottom layer bulk MOS devices are used to integrate memory cells. At the top layer, the SOI devices realized by ZMR are used to implement address decoders, sense amplifiers, I/O buffers, and chip controllers.

3.5 SOI DRAM

Due to the properties in high density, low parasitic capacitances, low leakage current, and good radiation hardness[22], SOI technology has been regarded as a good candidate for realizing low-voltage low-power large-size high-speed DRAMs in the future.

Fig. 3.29 shows the schematic diagram representing the soft error immunity ef-

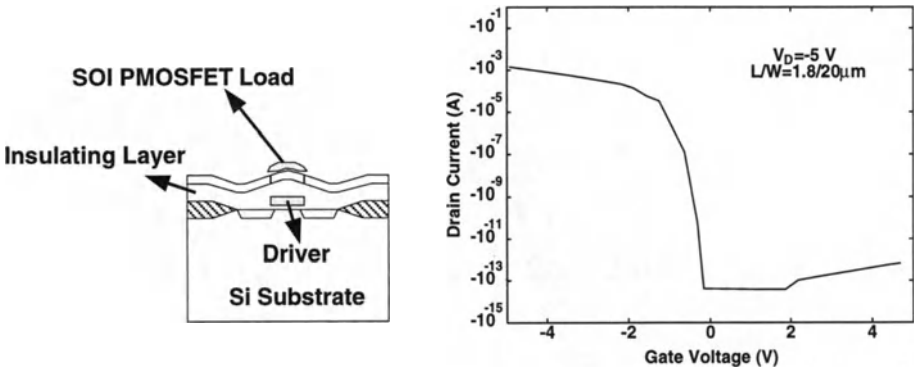


Figure 3.27: Cross section of the SOI PMOS load in an SRAM memory cell.

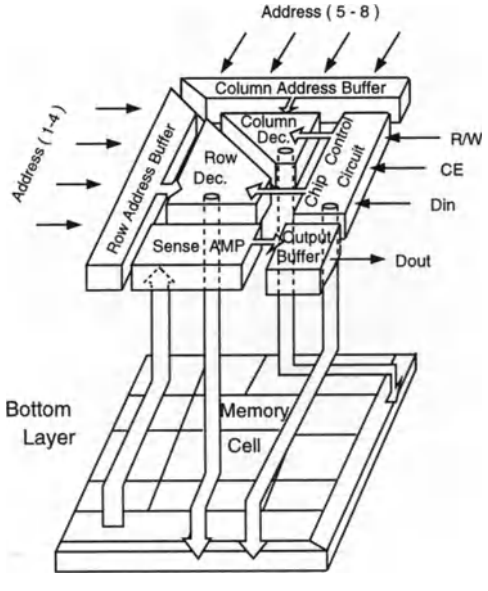


Figure 3.28: Circuit diagram of a 3D SRAM.

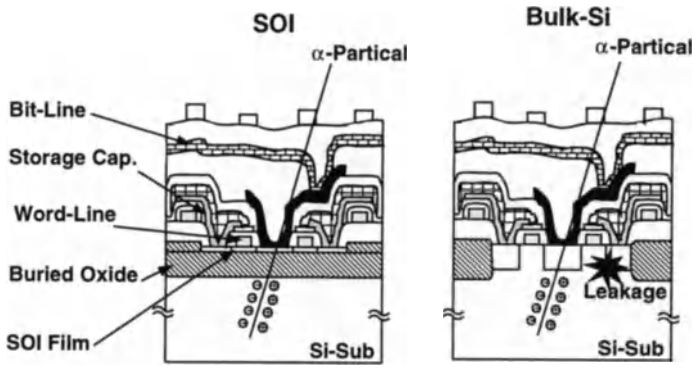


Figure 3.29: Schematic diagram representing the soft error immunity effect in an SOI DRAM.

fect in an SOI DRAM. As shown in the figure, when the DRAMs are susceptible to the alpha particles, owing to the buried oxide, which provides the isolation from the substrate, a large amount of electron-hole pairs produced by the alpha particles do not affect the storage nodes of the memory cell. Hence, a good soft error immunity can be obtained. In contrast, for the bulk DRAM, the electron-hole pairs produced by the alpha particles may be absorbed by the source/drain of the devices. Therefore, the potential of the storage nodes may change. Hence, the soft-error immunity is inferior.

Fig. 3.30 shows the processing sequence of an SOI-DRAM with LOCOS isolation using a 0.6μm SOI CMOS technology based on SIMOX or BESOI wafers, which has a silicon thin-film of 1000Å, and a front gate oxide of 110Å[23]. In this SOI CMOS technology, LOCOS isolation, 2-level metal interconnects, and semiconductor fin capacitors have been used. Using this SOI technology, a 16Mb DRAM has been integrated. At a supply voltage of 3V, the access time is 50ns, which is 20% faster as compared to the bulk one with a comparable size.

The parasitic BJT leakage current due to the floating body effect in a partially-depleted SOI CMOS device may affect the performance of a DRAM. Fig. 3.31 shows the illustration of the transient leakage mechanism in the SOI DRAM array device[24]. As shown in the figure, during the write cycle, when write is high, storage node is pushed high to 1.5V. During the latency period— cells of the same

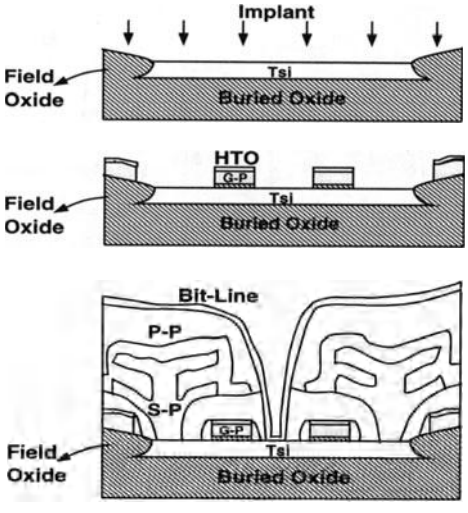


Figure 3.30: Processing sequence of an SOI-DRAM with LOCOS isolation.

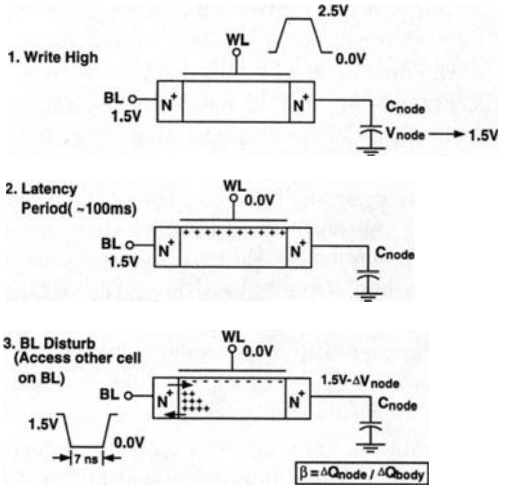


Figure 3.31: Illustration of the transient leakage mechanism in the SOI DRAM array device.

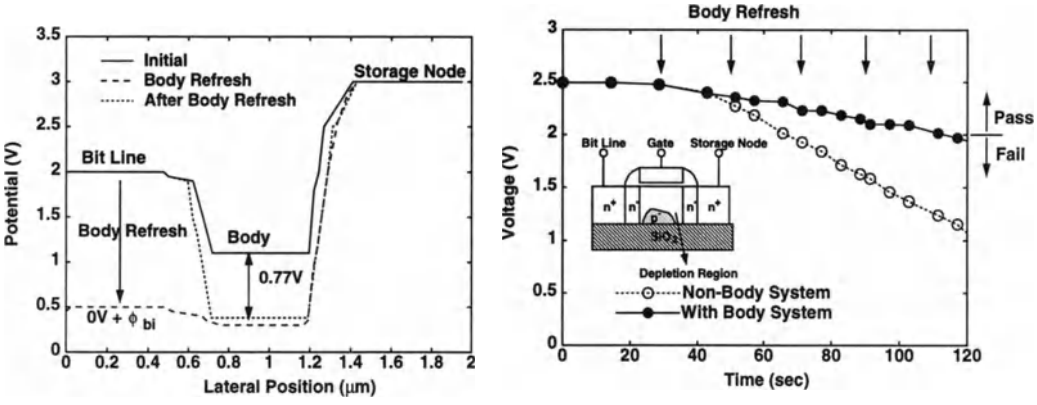


Figure 3.32: Potential distribution in an SOI DRAM memory cell and the transient behavior of the storage node during the latency period.

column are not accessed, due to the diode leakage current and the thermal generation effects, in the body, a substantial amount of holes are piled. As a result, the body potential rises. If a cell of the same column is accessed and the 'write 0' operation is initiated, the bit line will be pulled low. As a result, although the pass transistor of this unaccessed cell is off, the sudden drop in the source voltage may lead to the turn-on of the body-to-source diode. Hence, the holes in the body will be expelled. In addition, the parasitic BJT is triggered. Consequently, a large leakage current is injected from the drain end (the storage node). This leakage current will continue until the holes in the body are used up. Then, the body potential falls. This leakage causes the change in the potential at the storage node. Sometimes, errors may occur. In addition, if the latency period is too long, the subthreshold leakage current of the pass transistor becomes larger due to the increase in the body voltage. Therefore, the data retention time is degraded, which should be taken care of by the circuit designer.

The above leakage problems in an SOI DRAM memory cell can be improved by the body refresh operation. When the body potential of the pass transistor in an SOI DRAM memory cell does not reach a designated value, the bit line is pulled low intentionally such that the piled holes are expelled from the body. As a result, the body potential is maintained at a low value as shown in Fig. 3.32 [25]. Therefore, the parasitic BJT cannot be turned on. By this technique, the body voltage is

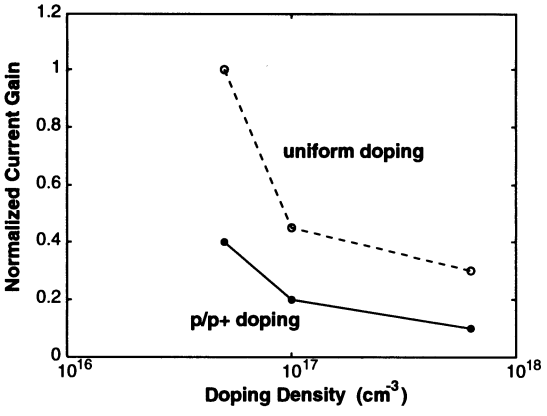


Figure 3.33: Current gain versus the thin-film doping density of the SOI MOS device with uniform and non-uniform p/p^+ doping structures used in the DRAM memory cell.

maintained at a low value. Therefore, during the latency period, the leakage current is smaller— a better data retention time can be obtained.

The leakage current problem in an SOI DRAM can be improved by another technique. By using partially-depleted SOI CMOS devices with a non-uniformly doped profile—at the bottom of the silicon thin-film, a more heavily doped P^+ region is formed, the current gain of the parasitic BJT can be effectively reduced. As a result, the influence of the parasitic BJT in the storage node can be lessened. Fig. 3.33 shows the current gain versus the thin-film doping density of the SOI MOS device with uniform and non-uniform P/P^+ doping structures used in the DRAM memory cell [26]. As shown in the figure, a non-uniform P/P^+ doping structure in the silicon thin-film with a high doping density at the bottom of the silicon thin-film provides an effective way to reduce the current gain of the parasitic bipolar device.

The leakage current effect can be suppressed by using body contacts. As shown in Fig. 3.34, the field oxide does not provide total isolation for the silicon thin-films [27]. Instead, a space is left for connecting the body contacts to the silicon thin-film body. The synchronous operation period of this 64Mb SOI DRAM is 5.8ns, which is 10% faster as compared to the bulk DRAM of the comparable size. Although

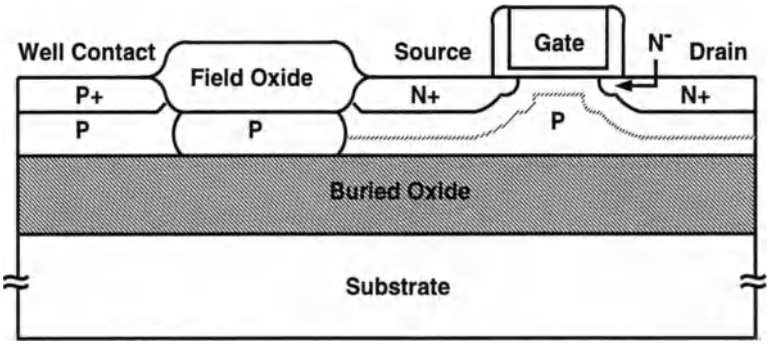


Figure 3.34: Schematic diagram of body-contacted (BC) SOI MOS devices used in a 64Mb SOI DRAM.

adding body contacts may lower the device density, using the body-tied SOI CMOS technology, the circuit design can be borrowed directly from the bulk CMOS technology.

Fig. 3.35 shows another way to add body contacts for SOI DRAM circuit applications [28]. As shown in the figure, only in the driver, the buffer, and the sense amplifier, body contacts are used, because the performance of these circuits is susceptible to the floating body effect. On the other hand, in the memory cell and logic gate, floating body configuration is still adopted since other techniques as described in the previous paragraphs have been used to avoid floating body effects. In addition, without using the body contact configuration, the density of these circuits can be enhanced. The overall arrangement of partial body-tied and partial body-floating strategy is used to optimize the circuit performance.

In addition to suppressing floating body effects, body contacts can be utilized for low-voltage operation. Fig. 3.36 shows the body-pulsed sense amplifier (BPS) circuit and its waveforms[29]. As shown in the figure, it is based on adjusting the body potential of some circuits dynamically such that the conducting capability of these devices can be enhanced in some appropriate time. In other time, their original states are maintained. By this arrangement, the power consumption does not increase substantially. As shown in the figure, in period (1), word line (WL) becomes high and the bit line (BL) starts to change. In period (2), SON becomes

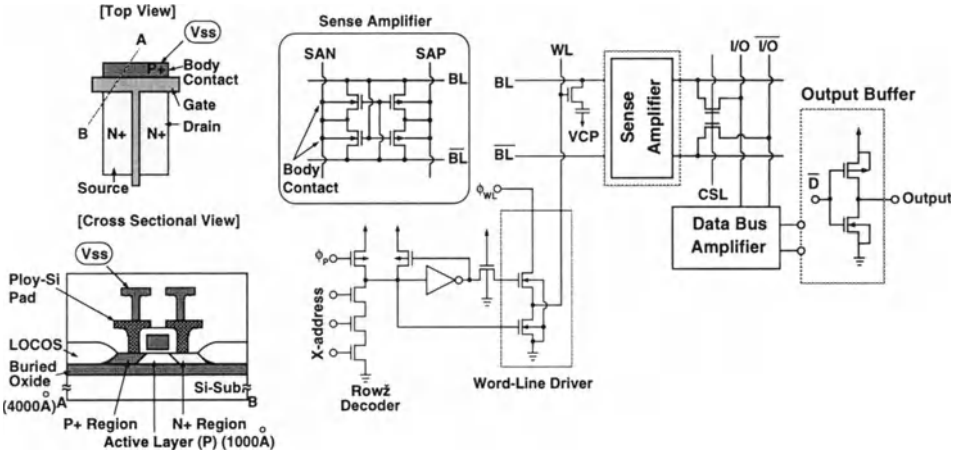


Figure 3.35: Data path of read operation in an SOI DRAM with body contacts for their devices using 0.5μm SOI CMOS technology.

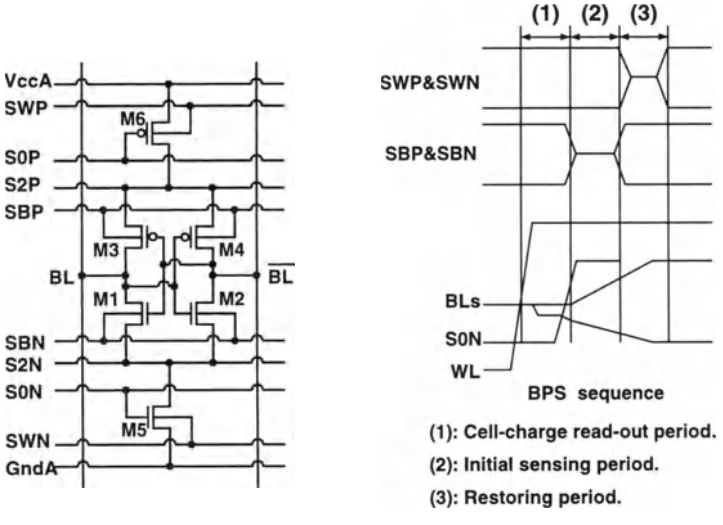


Figure 3.36: Body-pulsed sense amplifier (BPS) circuit.

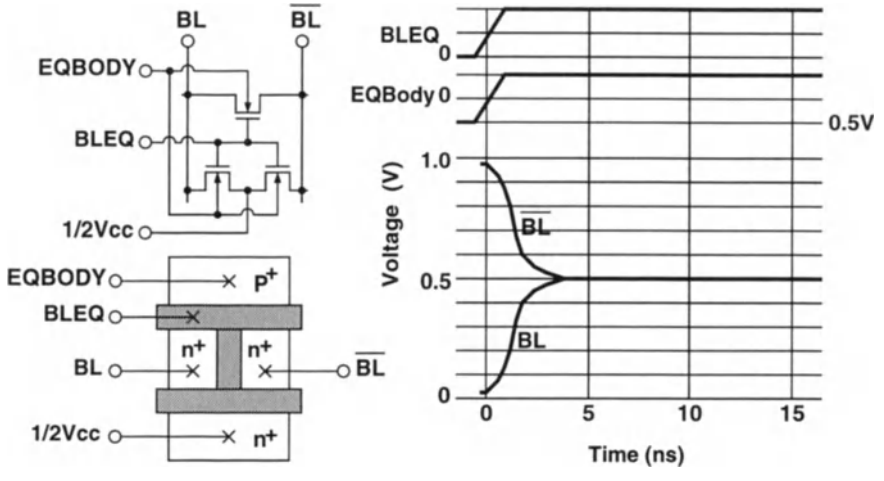


Figure 3.37: Body-driven equalizer (BDEQ) circuit and its related transients.

high and the sense amplifier begins to become active. At this time, the body voltage (SBN) of M1 and M2 is raised and the body voltage (SBP) of M3 and M4 is lowered temporarily. As a result, the magnitude of the threshold voltage of M_1-M_4 becomes smaller. Hence, the speed performance of the sense amplifier becomes faster. In period (3)— the restoring period, the body voltage (SWP & SWN) of M5 and M6 is changed accordingly such that the conducting capability of M5 & M6 can be upgraded. This results in a faster restoring process.

Based on a similar body-driven principle, Fig. 3.37 shows the body-driven equalizer (BDEQ) circuit and its related transient[29]. Similarly, when the equalizer becomes active (BLEQ is high), the body voltage of the NMOS device is raised simultaneously. Hence, the threshold voltage of the NMOS device is reduced, consequently the conducting capability is enhanced. Thus, the equalizing time is reduced. Fig. 3.38 shows the body current clamper (BCC) circuit[29]. The motivation of this circuit is to adjust the body voltage of the sense amplifier. If the body voltage is too high for the NMOS or too low for the PMOS, the body-source diode turns on, which may result in a large amount current flowing through V_{ccA} and Gnd_A. Therefore, some voltage perturbation exists on V_{ccA} and Gnd_A, which may affect the precise operation of the sense amplifier. This drawback can be improved by inserting diodes between body-bias line and V_{ccB}/Gnd_B. By this arrangement, the body voltage can

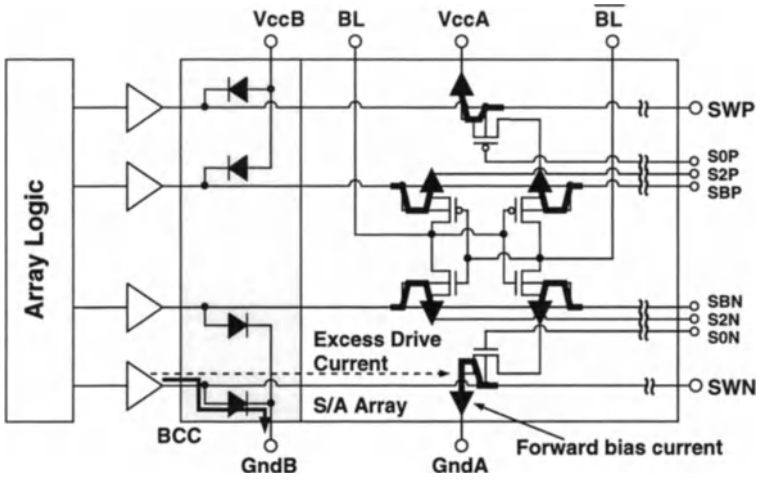


Figure 3.38: Body current clamper (BCC) circuit.

be clamped to within an appropriate value to reduce the voltage perturbation on V_{ccA} and Gnd_A.

Fig. 3.39 shows the body-pulsed transistor logic (BPTL) circuit to be used in the peripheral circuit[29]. BPTL circuit is also based on adjusting the body potential of the active logic gates such that a temporary enhancement in speed can be obtained. The active signal CLK arrives at various blocks at different times. In addition, the operation time for each block is limited. Therefore, the body bias (BP) should be adjusted only between the start and the end of the operation of each block. As shown in the figure, using AND gates and appropriate delay lines, the required BP signal can be obtained. When BP is high, it is the operation period of the block. Fig. 3.40 shows the performance of a 16Mb SOI DRAM using body control circuits based on a 0.5μm SIMOX SOI technology[29]. At a supply voltage of 1V, the access time is 46ns, which is much faster compared to the case without the body control.

In the previous section, 3D techniques for SRAMs have been described. Similarly, the 3D techniques have been used to integrate DRAM. As shown in Fig. 3.41, in a stacked SOI DRAM memory cell[30], there are three device layers. The bulk devices are at the bottom layer. The SOI devices are at the other two layers. Between device layers, doped polysilicon layers have been used to function as shielding such

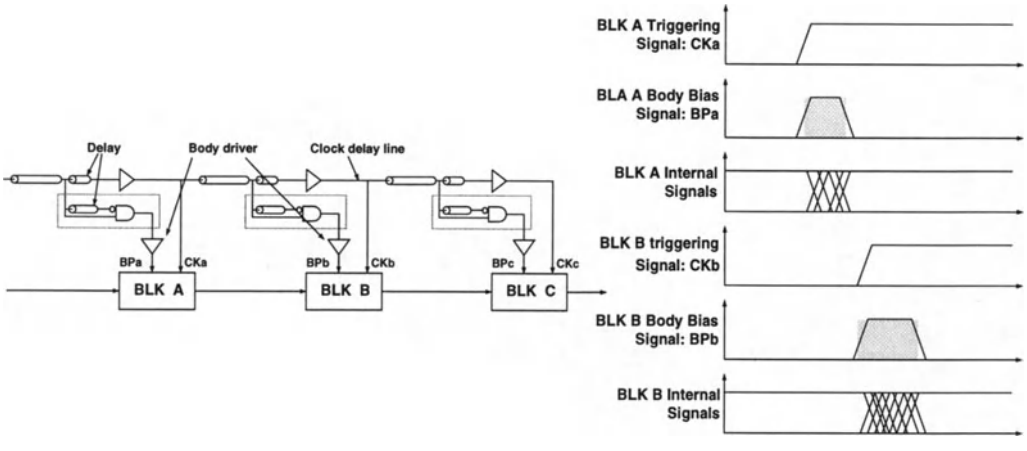
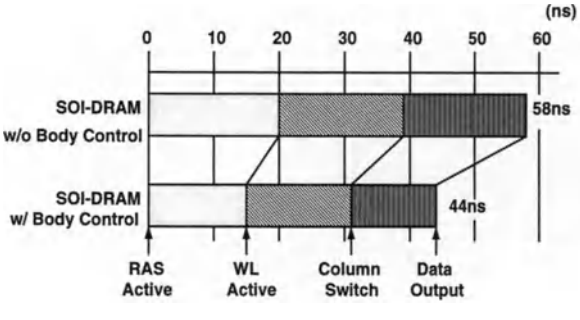


Figure 3.39: Body-pulsed transistor logic (BPTL) circuit.



Technology	0.5 μm CMOS/SIMOX, Dual gate, Modified MESA isolation
Thickness (tox/SOI/BOX)	10nm / 100nm / 400nm
Cell size	1.35 x 2.8 = 3.78 μm^2
Chip size	17.5 x 8.8 = 154mm
RAS access time	46ns @ 1.0V
Active current	11.5mA @1.0V, Tc=100ns
Standby current	4.4 μA @1.0V

Figure 3.40: Performance of a 16Mb SOI DRAM using the body control circuits based on a 0.5μm SIMOX SOI technology.

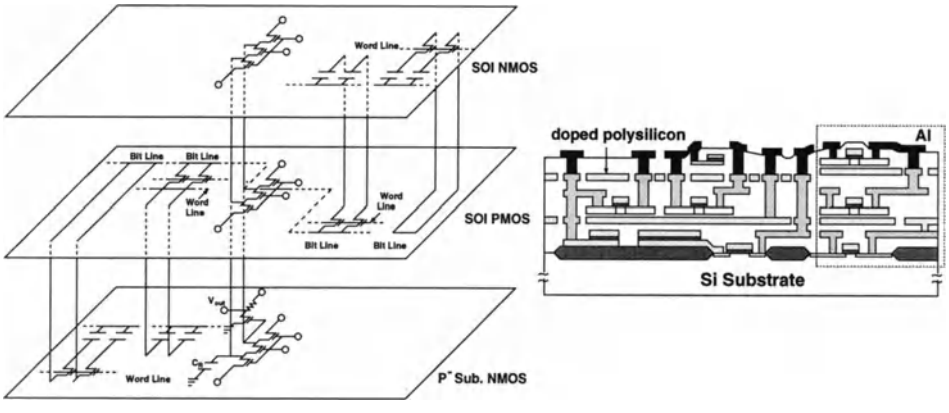


Figure 3.41: Structure of a stacked SOI DRAM memory cell.

that interference can be reduced. The planar capacitors are with the pass transistors located at the same layer or two adjacent layers to increase density and to reduce parasitic capacitances.

3.6 SOI CPU

Due to the advantages in radiation hardness, SOI CPUs have been used for special-purpose environments. The trends on SOI CPU are toward low-voltage and low-power. Based on a 0.5μm SOI CMOS technology, a microprocessor operating at below 1V has been integrated. As shown in Fig. 3.42, at 0.9V, the operation speed is 5.7MHz, which is 1.9 times faster as compared to the bulk one[31]. Fig. 3.43 shows the core frequency performance as a function of the operating temperature over a supply voltage of 0.9V to 2.5V of the SOI CPU [31]. At a larger V_{DD}, when the operating temperature is increased, due to a degraded mobility, the maximum operating frequency is reduced since the driving capability of the devices is decreased. On the other hand, at a smaller V_{DD}, the maximum operating frequency, which is sensitive to the threshold voltage, does not decrease when the temperature is increased. Instead, the speed increases slightly owing to the decreased magnitude in the threshold voltage when the operating temperature is raised.

Fig. 3.44 shows the multi-threshold CMOS/SIMOX circuit scheme[8]. As shown

CMOS		NMOS	PMOS
SOI silicon	μm	0.1	0.1
Buried Oxide	μm	0.4	0.4
Gate Oxide	Å	105	105
Leff	μm	0.41	0.50
Threshold Voltage	mV	530	460
I_{DSAT} @ 1.2V	μA/μm	65	22
sub-Vt slope	mV/dec	70	73
BVDSS	V	3.2	6.3

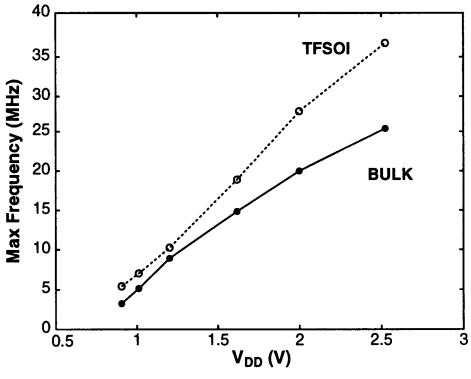


Figure 3.42: Microcontroller CPU core frequency performance comparison between SOI and bulk CMOS.

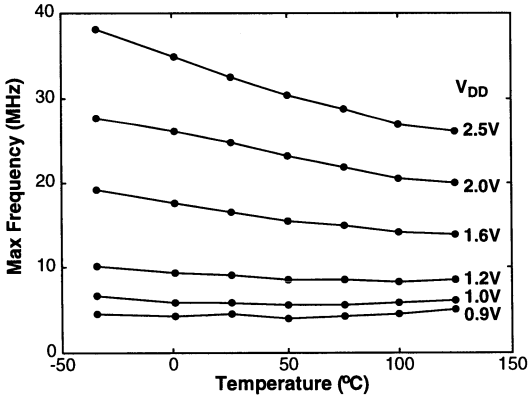
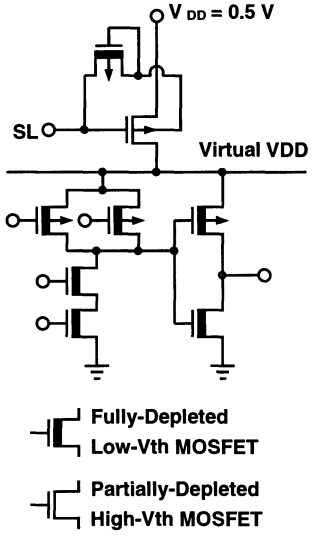


Figure 3.43: Core frequency performance as a function of the operating temperature over a supply voltage of 0.9V to 2.5V of the SOI CPU.



Supply Voltage	0.5 V
Operating Frequency	40 MHz
Power Dissipation	0.35 mW (at 40 MHz)
	< 5 nW (sleep mode)
Turn-on Time	0.4μs
Turn-off Time	8.0μs
Gate counts	8K gates

Figure 3.44: Multi-threshold CMOS/SIMOX circuit scheme.

in the figure, this SOI CMOS circuit is composed of two portions— the power switch transistor and the logic block. Their functions have been described in Sec. 3.2. Based on the multi-threshold CMOS/SIMOX circuit scheme, a 16bit arithmetic logic unit (ALU) based on a 0.25μm CMOS technology has been integrated. At a supply voltage of 0.5V, a speed of 40MHz has been reached. The power consumption is only 0.35mW. During the sleep mode, the power consumption is less than 5nW.

Using DTMOS technique, which is based on the dynamic threshold voltage MOS device with body tied to gate, the speed performance of a pass-gate logic can be faster. Fig. 3.45 shows the body-contact (BCSOI) pass-gate logic circuits. As shown in the figure, the first type of the BCSOI circuit is for driving loads with long wiring and large fan-out[32]. The second type of BCSOI circuit is for driving local connected circuits. As shown in Fig. 3.46, using the BCSOI pass gate logic circuits based on a 0.3μm SOI technology, a 32-bit ALU has been integrated[32]. At 0.5V, the maximum operating frequency is 200MHz. However, the power consumption is 20mW. Due to the restraints on turn-on of the body/source diode, this BCSOI CPU can only work at a supply voltage smaller than 0.8V.

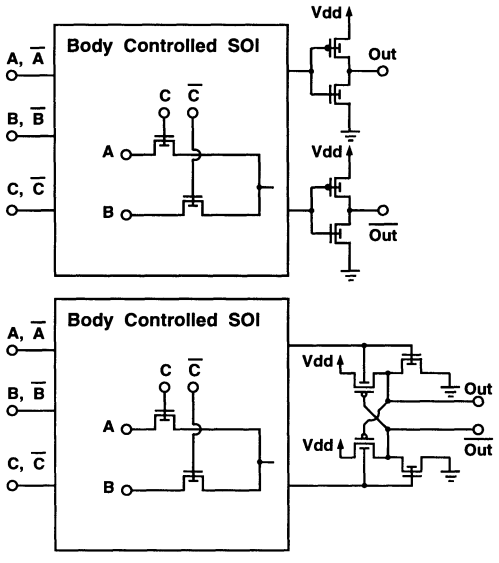


Figure 3.45: Body contact (BCSOI) pass-gate logic circuits.

3.7 SOI Analog Circuits

Until now in this chapter, SOI CMOS technology has been used for digital circuit designs. For SOI CMOS devices, their parasitic junction area is much smaller as compared to the bulk ones. SOI devices are especially suitable for operation at an elevated temperature. Bulk CMOS devices can work at an operating temperature until 150C. Bulk BJT can work until 200C. SOI CMOS devices can work until 300C[33]. Therefore, for analog circuits, SOI technology can also be useful. In this section, analog circuits using SOI CMOS technology are described. Fig. 3.47 shows the schematic cross section of a 0.35μm fully-depleted SOI/SIMOX CMOS technology for analog/digital mixed-mode circuits[34]. In this SOI technology, the CMOS devices have a front gate oxide of 70Å, a silicon thin-film of 500Å, and a buried oxide of 1000Å. As shown in the figure, in addition to the CMOS devices and two-level metal layers for interconnects, capacitors and resistors have been realized. The capacitor device is made of the N^+ top poly plate and the n-type silicon thin-film region with gate oxide as the dielectric, which is realized by an extra buried n-type layer diffusion before the forming the gate electrode. The doping density of this n-type silicon thin-film region has been optimized such that the capacitance volt-

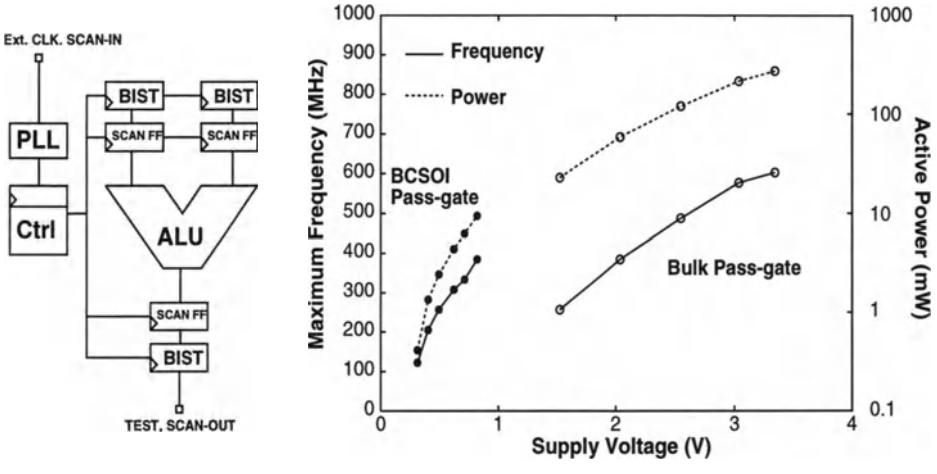


Figure 3.46: Maximum operating frequency and active power versus supply voltage of bulk pass-gate and BCSOI pass-gate logic.

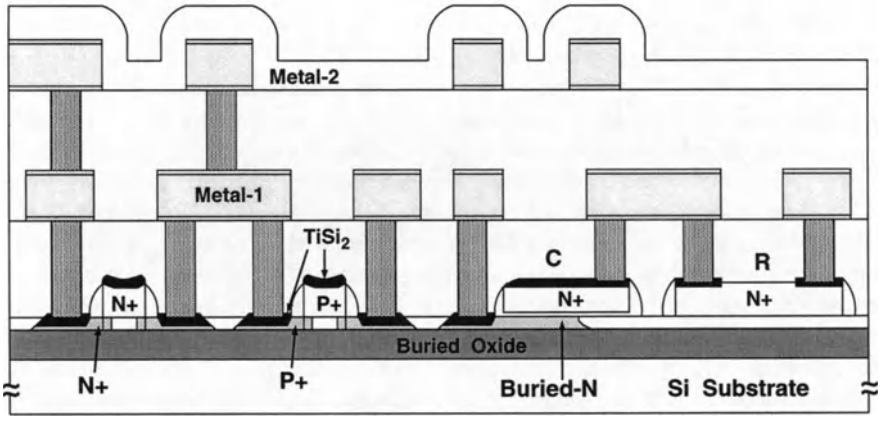
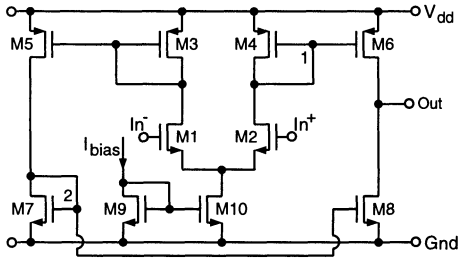


Figure 3.47: Schematic cross section of a 0.35μm fully-depleted SOI/SIMOX CMOS technology for analog/digital mixed-mode circuits.



	Micropower	High Gain	HF 3μm	HF 2μm
M 1-2	30 / 3	300 / 6	600 / 3	400 / 2
M 3-4	33 / 3	150 / 6	300 / 3	60 / 2
M 5-6	66 / 3	100 / 12	300 / 3	120 / 2
M 7-8	30 / 3	100 / 20	200 / 5	100 / 3
C_L(pF)	10	10	10	10
Vdd - Vss (V)	1.2	2	4	4
Pss (W)	3.6μ	100μ	29 m	12 m
f_T (MHz)	0.350	1.8	93	97
A_{vo} (dB)	44	65	35	37
f_{p1} (MHz)	8.9	12.4	209	211
f_{p2} (MHz)	12.4	2.7	243	546
Φ_M (^{o})	87	66	55	59
Area (μm^2)	9500	96000	82800	45700

Figure 3.48: An SOI operational transconductance amplifier.

age coefficient is smaller than 3%/V, which is sufficient for a 10bit analog-to-digital converter (ADC) design. The resistor device is realized by the N^+ polysilicon layer.

Fig. 3.48 shows an operational transconductance amplifier based on fully-depleted inversion-mode SOI CMOS technology, which has a front gate oxide of 300Å, a buried oxide of 4000Å, and a silicon thin-film of 800Å[35]. As shown in the figure, M_1 and M_2 are the input differential pair, which is used to sense the input signals. Via three current mirrors, which are made of M_3-M_8, the sensed input signal is transformed into the high-impedance output. As shown in the figure, the power consumption of this SOI operational transconductance amplifier is 3.6μW. A gain of 65dB and a maximum bandwidth of 200MHz have been reached. Fig. 3.49 shows gain and frequency versus operating temperature of the SOI operational transconductance amplifier[35]. Due to the superior isolation structure, the SOI operational transconductance amplifier can work up to 300C, where individual devices are biased at the ZTC (zero temperature coefficient) area. Consequently, the performance of the devices does not vary substantially as the operating temperature rises. Fig. 3.50 shows the drain current characteristics of SOI CMOS devices at different temperatures[36]. As shown in the figure, when the operating temperature is changed, the drain current changes. In spite of the temperature dependence, there is a zero-temperature-coefficient (ZTC) point, where the drain current behavior is insensitive to the operating temperature. Owing to the ZTC characteristics, it has

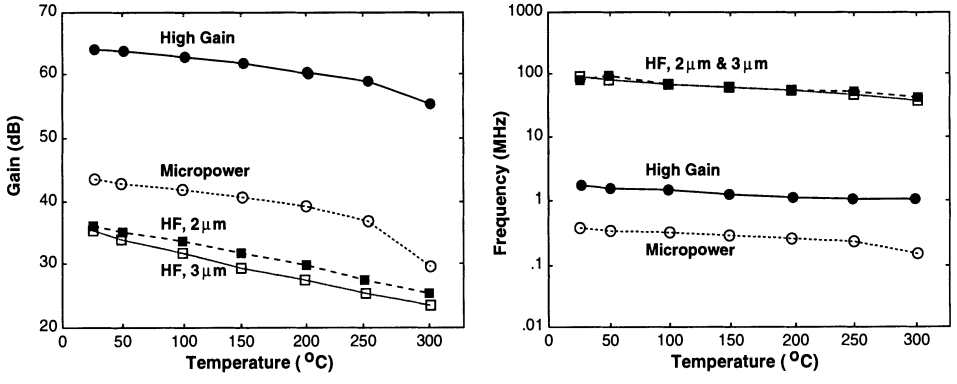


Figure 3.49: Gain and frequency versus operating temperature of the SOI operational transconductance amplifier.

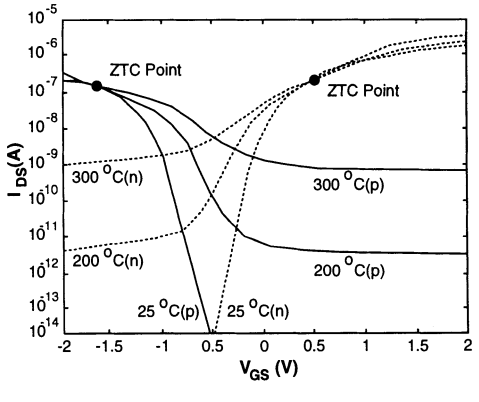


Figure 3.50: Drain current characteristics of SOI CMOS devices at different temperatures.

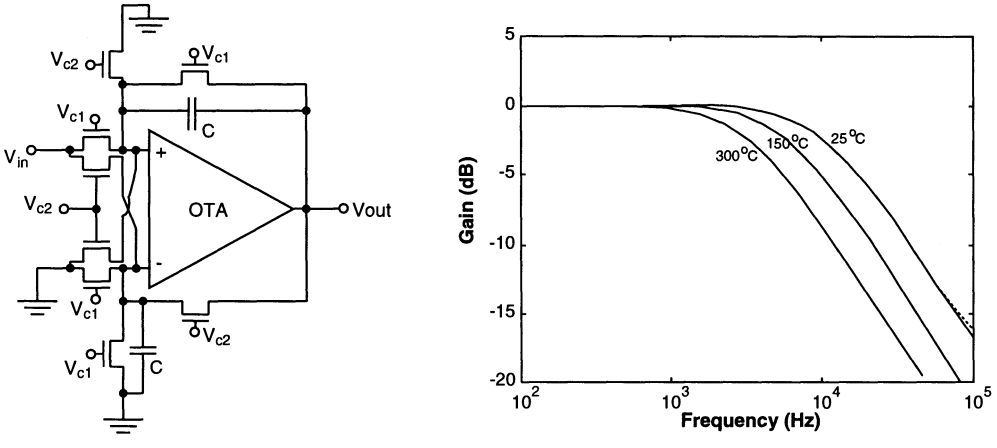


Figure 3.51: Schematic view of a first-order filter realized by SOI CMOS devices.

been often taken advantage to reduce the temperature sensitivity of the analog circuit.

Based on the operational transconductance amplifiers (OTA) and the highly-linear 4-MOSFET structure, an SOI first-order filter as shown in Fig. 3.51 has been implemented[37]. As shown in the figure, this SOI first-order filter can work at an operating temperature up to 300C. When the operating temperature is raised, the bandwidth becomes smaller. This is due to the increased effective resistance of the 4-MOSFET structure at an elevated temperature. In this circuit, V_{c1} is fixed. In contrast, V_{c2} is adjustable. Therefore, V_{c2} can be adjusted by using an on-chip automatic tuning circuit to compensate for the performance due to the temperature effect.

Based on the SOI operational transconductance amplifiers, pass transistors, latch, and comparator, a sigma-delta modulator for the sigma-delta analog-to-digital converter as shown in Fig. 3.52 has been done[38]. As shown in the figure, at an operating temperature of 300C, the modulator can still work, although the signal-to-noise ratio (SNR) performance is degraded a little bit due to harmonic distortion. At 300C, the leakage current of the pass transistors is substantial, which may affect the performance of the integrator. Due to the leakage current in the pass transis-

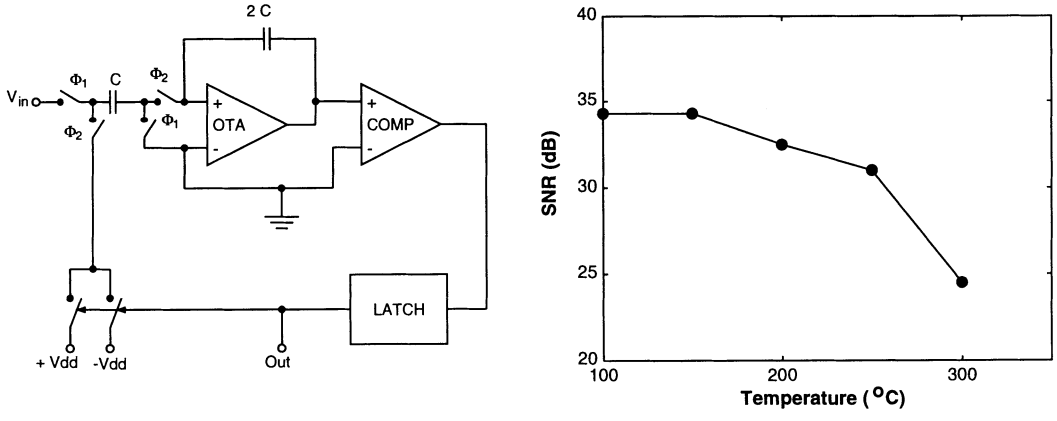


Figure 3.52: Schematic of the SOI first-order modulator.

tors, the charge in the capacitor is lost quickly. As a result, the minimum sampling frequency should be raised.

Fig. 3.53 shows a voltage reference circuit using accumulation-mode and inversion-mode SOI MOS devices, which have a similar doping density in the silicon thin-films[39]. As shown in the figure, M_3 and M_4, which are accumulation-mode, provide the biasing current for M_1 and M_2, which are inversion-mode. The reference voltage is generated by the difference in the threshold voltages of M_1 and M_2. M_5-M_8 form an output buffer. The accumulation-mode and the inversion-mode SOI MOS devices have an identical doping density. In addition, both the accumulation-mode and the inversion-mode SOI MOS devices are biased at a back gate bias of -5V. As a result, the threshold voltage and the drain current of both devices have almost identical temperature coefficients. Consequently, the reference voltage has an excellent temperature coefficient since the temperature coefficients of both devices are cancelled out by each other.

In addition to fully-depleted SOI devices, partially-depleted SOI CMOS devices have been used to design analog circuits. In order to avoid the kink effect due to the floating body structure, the body-tied-to-source structure has been adopted. Fig. 3.54 shows a two-stage operational amplifier with a class AB-output stage and a quiescent current control using partially-depleted SOI CMOS devices [33]. Fig. 3.55

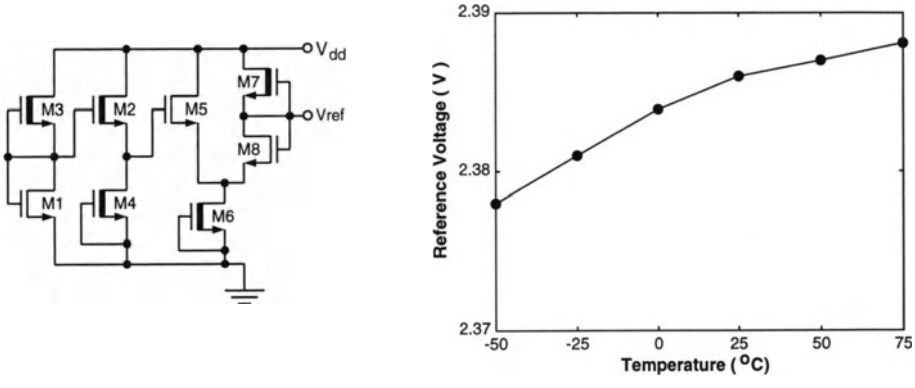


Figure 3.53: A voltage reference circuit using accumulation-mode and inversion-mode SOI MOS devices.

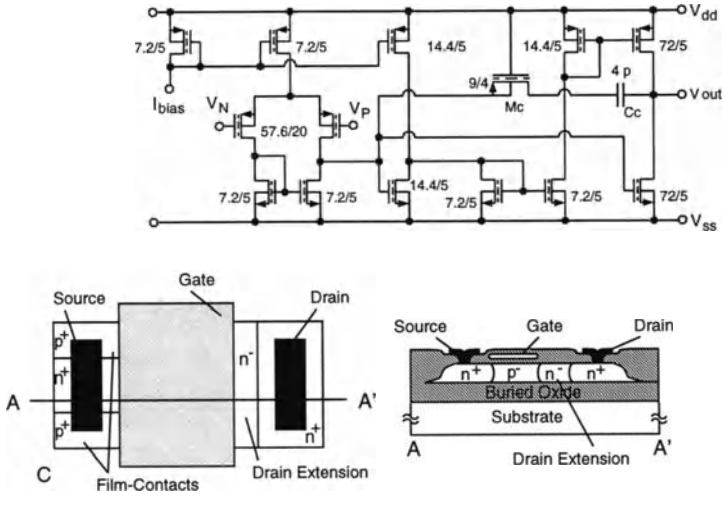


Figure 3.54: Two-stage operational amplifier with a class AB-output stage and a quiescent current control using partially-depleted SOI CMOS technology.

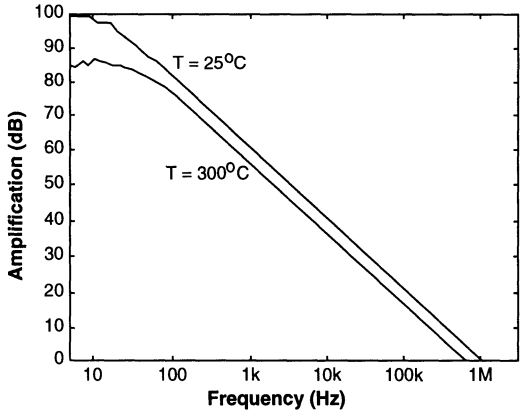


Figure 3.55: Open loop gain versus frequency of the SOI two-stage operational amplifier with a capacitive load of 50pF.

shows the open loop gain versus frequency of the SOI two-stage operational amplifier with a capacitive load of 50pF. As shown in the figure, at a higher temperature, the op amp still works although the frequency response becomes worse[33]. Fig. 3.56 shows the transmission gates realized by partially-depleted SOI MOS devices. As shown in the figure, the body of the partially-depleted SOI MOS device is connected to V_{SS} for NMOS or V_{DD} for PMOS. An H-shaped gate structure has been used to avoid the leakage current caused by the edge channel[33]. Fig. 3.57 shows the schematic and the frequency response at 300C of the switched-capacitor seventh-order low pass ladder filter using SOI MOS devices[33]. Owing to the utilization of the SOI devices, this circuit has a good performance until 300C. At 350C, it cannot function properly since the intrinsic carrier concentration is in the order of the silicon thin-film doping density.

Fig. 3.58 shows the block diagram of focused-ion-beam (FIB) 4-bit flash analog-to-digital converter (ADC) implemented by 0.25μm partially-depleted SOI CMOS devices[40]. Owing to the 0.25μm partially-depleted SOI CMOS devices, the sampling rate can be as high as 1GHz. On the other hand, the power dissipation is under 100mW. This SOI flash ADC uses the one-input comparators, which are composed of inverters having various transfer curves. The threshold voltage of the SOI devices in each inverter is individually adjusted by focus-ion-beam (FIB) such that the

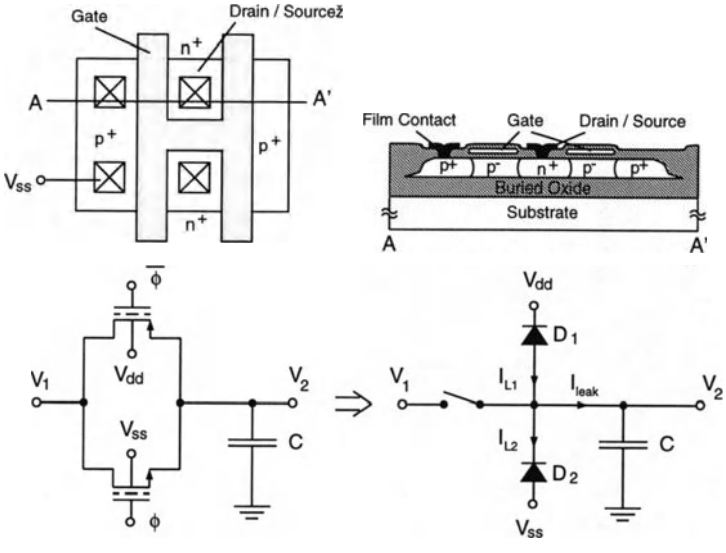


Figure 3.56: Transmission gates realized by partially-depleted SOI devices.

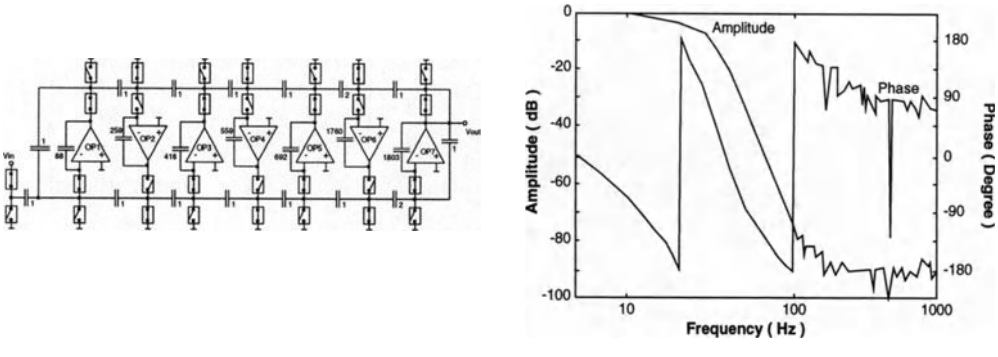


Figure 3.57: Schematic of the switched-capacitor seventh-order low pass ladder filter using SOI MOS devices.

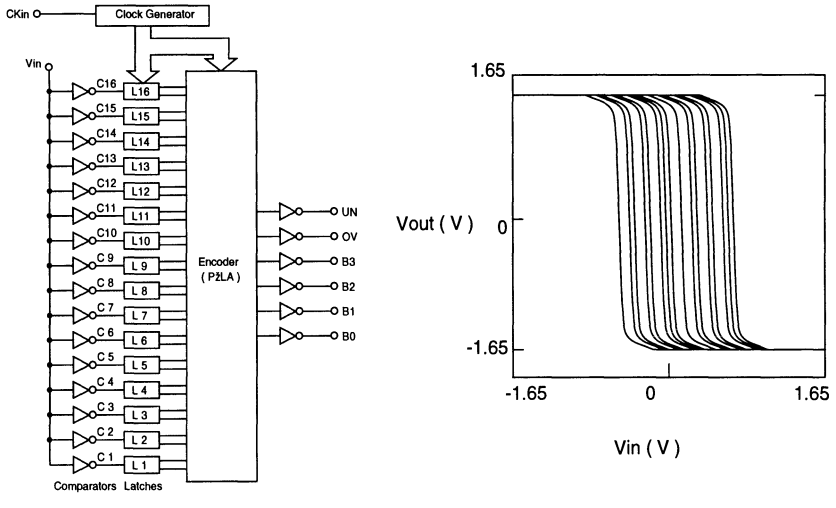


Figure 3.58: Block diagram of focused-ion-beam (FIB) 4-bit flash analog-to-digital converter (ADC) implemented by 0.25μm partially-depleted SOI CMOS devices.

transition point of each inverter can be located at its designated location. By this method, the speed performance can be enhanced at a reduced power dissipation. Fig. 3.59 shows the circuit schematic with the signal path through a comparator and a latch used in an SOI analog-to-digital converter (ADC) circuit[40]. Due to the partially-depleted SOI devices adopted in this circuit, body contacts to all devices are needed. Fig. 3.60 shows a portion of a 7-bit ADC circuit using a 0.7μm partially-depleted SOI CMOS technology[41]. As shown in the figure, in order to reduce the floating body effect, body-tied-to-source structure has been adopted.

3.8 Summary

In this chapter, the influence of the floating body effect in the circuit performance of SOI CMOS devices has been described, followed by the low-voltage circuit designs using SOI CMOS devices. SOI gate array, SRAM, DRAM, and CPU have been introduced. In addition to these digital circuits, SOI analog circuits including OTA, filters, modulators, and ADC have been presented in the final portion of the chapter.

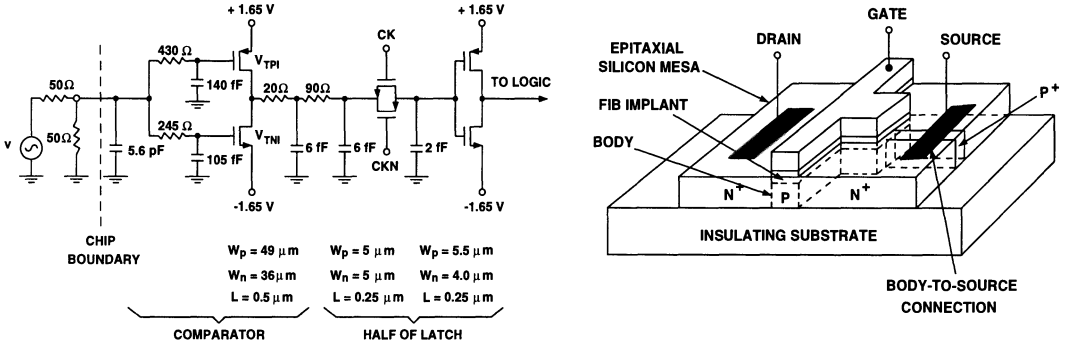


Figure 3.59: Circuit schematic showing the signal path through a comparator and a latch used in an SOI analog-to-digital converter (ADC) circuit.

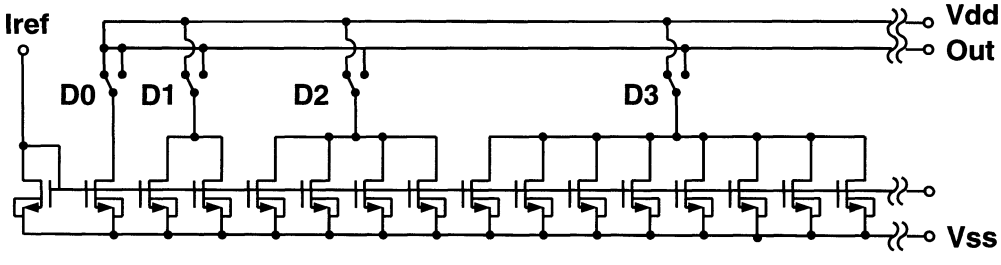


Figure 3.60: Portion of a 7-bit ADC circuit using a 0.7μm partially-depleted SOI CMOS technology.

References

[1] J. M. Stern, P. A. Ivey, S. Davidson and S. N. Walker, "Silicon-on-Insulator (SOI): A High Performance ASIC Technology," *CICC Dig.*, pp.9.2.1-4, 1992.

[2] P.-F. Lu, C.-T. Chuang, J. Ji, L. F. Wagner, C.-M. Hsieh, J. B. Kuang, L. L. Hsu, M. M. Pelella, S.-F. S. Chu, and C. J. Anderson, "Floating-Body Effects in Partially Depleted SOI CMOS Circuits," *IEEE J. Sol. St. Ckt*, Vol. 32, No. 8, pp. 1241-1253, Aug. 1997.

[3] R. Rajsuman, "Implementation of Switch Network Logic in SOI," *IEEE J. Sol. St. Ckt*, Vol. 25, No. 3, pp. 874-877, June 1990.

[4] F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P. K. Ko, and C. Hu, "A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Operation," *IEEE Elec. Dev. Let.*, Vol. 15, No. 12, pp. 510-512, Dec. 1994.

[5] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko, and C. Hu, "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," *IEEE Trans. Elec. Dev.*, Vol. 44, No. 3, pp. 414-422, March 1997.

[6] I.-Y. Chung, Y. J. Park, and H. S. Min, "A New SOI Inverter using Dynamic Threshold for Low-Power Applications," *IEEE Elec. Dev. Let.*, Vol. 18, No. 6, pp. 248-250, June 1997.

[7] T. W. Houston, "A Novel Dynamic Vt Circuit Configuration," *SOI Conf. Dig.*, pp. 154-155, 1997.

[8] T. Douseki, S. Shigematsu, J. Yamada, M. Harada, H. Inokawa, and T. Tsuchiya, "A 0.5-V MTCMOS/SIMOX Logic Gate," *IEEE J. Sol. St. Ckt*, Vol. 32, No. 10, pp. 1604-1609, Oct. 1997.

[9] Y. Sato, Y. Kado, T. Tsuchiya, T. Kosugi, H. Ishii, and K. Nishimura, "300KG Gate-Array LSI using 0.25μm Ultra-Thin-Film Fully-Depleted CMOS/SIMOX with Tungsten-Deposited Source/Drain," *SOI Conf. Dig.*, pp. 168-169, 1997.

[10] Y. Kado, H. Inokawa, Y. Okazaki, T. Tsuchiya, Y. Kawai, M. Sato, Y. Sakakibara, S. Nakayama, H. Yamada, M. Kitamura, S. Nakashima, K. Nishimura, S. Date, M. Ino, K. Takeya, and T. Sakai, "Substantial Advantages of Fully-Depleted CMOS/SIMOX Devices as Low-Power High-Performance VLSI Components Compared with its Bulk-CMOS Counterpart," *IEDM Dig.*, pp. 635-638, 1995.

[11] Y. Yamaguchi, A. Ishibashi, M. Shimizu, T. Nishimura, K. Tsukamoto, K. Horie, and Y. Akasaka, "A High-Speed 0.6 – μm 16K CMOS Gate Array on a Thin SIMOX Film," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 1, pp. 179-186, Jan. 1993.

[12] K. Ueda, K. Nii, Y. Wada, I. Takimoto, S. Maeda, T. Iwamatsu, Y. Yamaguchi, S. Maegawa, K. Mashiko, and H. Hamano, "A CAD-Compatible SOI/CMOS Gate Array having Body-Fixed Partially-Depleted Transistors," *ISSCC Dig.*, pp. 288-289, 1997.

[13] K. Mashiko, K. Ueda, K. Nii, Y. Wada, T. Hirota, S. Maeda, T. Iwamatsu, Y. Yamaguchi, T. Ipposhi, S. Maegawa, and H. Hamano, "A 0.35μm 560KG SOI/CMOS Gate Array using Field-Shield Isolation Technique," *SOI Conf. Dig.*, pp. 166-167, 1997.

[14] N. Sasaki and M. Nakano, "A CMOS/SOS Gate Array with a New Customization Technique of Cutting," *IEEE Trans. Elec. Dev.*, Vol. 29, No. 10, pp. 1535-1541, Oct. 1982.

[15] K. Kumagai, T. Yamada, H. Iwaki, H. Nakamura, H. Onishi, Y. Matsubara, K. Imai and S. Kurosawa, "A New SRAM Cell Design using 0.35μm CMOS/SIMOX Technology," *SOI Conf. Dig.*, pp. 174-175, 1997.

[16] G. G. Shahidi, T. H. Ning, T. I. Chappell, J. H. Comfort, B. A. Chappell, R. Franch, C. J. Anderson, P. W. Cook, S. E. Schuster, M. G. Rosenfield, M. R. Polcari, R. H. Dennard, and B. Davari, "SOI for a 1-Volt CMOS Technology and Application to a 512Kb SRAM with 3.5ns Access Time," *IEDM Dig.*, pp. 813-816, 1993.

[17] M. Isobe, Y. Uchida, K. Maeguchi, T. Mochizuki, M. Kimura, H. Hatano, Y. Mizutani, and H. Tango, "An 18ns CMOS/SOS 4K Static RAM," *IEEE J. Sol. St. Ckt*, Vol. 16, No. 5, pp. 460-465, Oct. 1981.

[18] J. B. Kuang, S. Ratanaphanyarat, M. J. Saccamango, L. L.-C. Hsu, R. C. Flaker, L. F. Wagner, S.-F. S. Chu, and G. G. Shahidi, "SRAM Bitline Circuits on PD SOI: Advantages and Concerns," *IEEE J. Sol. St. Ckt*, Vol. 32, No. 6, pp. 837-844, June 1997.

[19] Y. Takao, H. Shimada, N. Suzuki, Y. Matsukawa, Y. Kobayashi and N. Sasaki, "A Low-Power SRAM Utilizing High On/Off Ratio Laser-Recrystallized SOI PMOSFET Load," *Symp. VLSI Ckt Dig.*, pp. 95-96, 1991.

[20] Y. Takao, H. Shimada, N. Suzuki, Y. Matsukawa and N. Sasaki, "Low-Power and High-Stability SRAM Technology using a Laser-Recrystallized p-Channel SOI MOSFET," *IEEE Trans. Elec. Dev.*, Vol. 39, No. 9, pp. 2147-2152, Sept. 1992.

[21] T. Nishimura, Y. Inoue, K. Sugahara, M. Nakaya, Y. Horiba and Y. Akasaka, "A Three Dimensional Static RAM," *Symp. VLSI Tech. Dig.*, pp. 30-31, 1985.

[22] Y. Yamaguchi and Y. Inoue, "SOI DRAM: Its Features and Possibility," *SOI Conf. Dig.*, pp. 122-124, 1995.

[23] H.-S. Kim, S.-B. Lee, D.-U. Choi, J.-H. Shim, K.-C. Lee, K.-P. Lee, K.-N. Kim, and J.-W. Park, "A High Performance 16M DRAM on a Thin Film SOI," *Symp. VLSI Tech. Dig.*, pp. 143-144, 1995.

[24] J. A. Mandelman, J. E. Barth, J. K. DeBrosse, R. H. Dennard, H. L. Kalter, J. Gautier and H. I. Hanafi, "Floating-Body Concerns for SOI Dynamic Random Access Memory (DRAM)," *SOI Conf. Dig.*, pp. 136-137, 1996.

[25] S. Tomishima, F. Morishita, M. Tsukude, T. Yamagata, and K. Arimoto, "A Long Data Retention SOI-DRAM with the Body Refresh Function," *Symp. VLSI Ckt. Dig.*, pp. 198-199, 1996.

[26] H.-S. Kim, D.-U. Choi, S.-H. Lee, S.-K. Lee, J.-K. Park, K.-N. Kim and J.-W. Park, "Data Retention Times in SOI-DRAMs," *Symp. VLSI Tech. Dig.*, pp. 126-127, 1996.

[27] Y.-H. Koh, J.-H. Choi, J.-W. Yang, M.-H. Nam, W.-C. Lee, J.-W. Lee and M.-R. Oh, "64Mbit SOI-DRAM Technologies using Body-Contacted (BC) Structure," *SOI Conf. Dig.*, pp. 170-171, 1997.

[28] K. Suma, T. Tsuruda, H. Hidaka, T. Eimori, T. Oashi, Y. Yamaguchi, T. Iwamatsu, M. Hirose, F. Morishita, K. Arimoto, K. Fujishima, Y. Inoue, T. Nishimura, and T. Yoshihara, "An SOI-DRAM with Wide Operating Voltage Range by CMOS/SIMOX Technology," *IEEE J. Sol. St. Ckt*, Vol. 29, No. 11, pp. 1323-1329, Nov. 1994.

[29] K. Shimomura, H. Shimano, N. Sakashita, F. Okuda, T. Oashi, Y. Yamaguchi, T. Eimori, M. Inuishi, K. Arimoto, S. Maegawa, Y. Inoue, S. Komori, and K. Kyuma, "A 1-V 46-ns 16-Mb SOI-DRAM with Body Control Technique," *IEEE J. Sol. St. Ckt*, Vol. 32, No. 11, pp. 1712-1720, Nov. 1997.

[30] K. Ohtake, K. Shirakawa, M. Koba, K. Awane, Y. Ohta, D. Azuma and S. Miyata, "Triple Layered SOI Dynamic Memory," *IEDM Dig.*, pp. 148-151, 1986.

[31] W. M. Huang, K. Papworth, M. Racanelli, J. P. John, J. Foerstner, H. C. Shin, H. Park, B. Y. Hwang, T. Wetteroth, S. Hong, H. Shin, S. Wilson and S. Cheng, "TFSOI CMOS Technology for Sub-1V Microcontroller Circuits," *IEDM Dig.*, pp. 59-62, 1995.

[32] T. Fuse, Y. Oowaki, T. Yamada, M. Kamoshida, M. Ohta, T. Shino, S. Kawanaka, M. Terauchi, T. Yoshida, G. Matsubara, S. Yoshioka, S. Watanabe, M. Yoshimi, K. Ohuchi, and S. Manabe, "A 0.5V 200MHz 1-Stage 32b ALU using a Body Bias Controlled SOI Pass-Gate Logic," *ISSCC Dig.*, pp.286-287, 1997.

[33] M. Verbeck, C. Zimmermann, and H-L. Fiedler, "A MOS Switched-Capacitor Ladder Filter in SIMOX Technology for High Temperature Applications up to 300C," *IEEE J. Sol. St. Ckt*, Vol. 31, No. 7, pp. 908-914, July 1996.

[34] A. O. Adan, T. Naka, S. Kaneko, D. Urabe, K. Higashi, and A. Kagisawa, "Low-Voltage 0.35μm CMOS/SOI Technology for High-Performance ASIC's," *CICC Dig.*, pp. 427-430, 1997.

[35] J.-P. Eggermont, D. D. Ceuster, D. Flandre, B. Gentinne, P. G. A. Jespers, and J.-P. Colinge, "Design of SOI CMOS Operational Amplifiers for Applications up to 300C," *IEEE J. Sol. St. Ckt*, Vol. 31, No. 2, pp. 179-186, Feb. 1996.

[36] P. Francis, A. Terao, B. Gentinne, D. Flandre and J.-P. Colinge, "SOI Technology for High-Temperature Applications," *IEDM Dig.*, pp. 353-356, 1992.

[37] V. Dessard, D. Baldwin, L. Demeus, B. Gentinne and D. Flandre, "SOI Implementation of Low-Voltage and High-Temperature MOSFET-C Continuous-Time Filters," *SOI Conf. Dig.*, pp. 24-25, 1996.

[38] A. Viviani, D. Flandre and P. Jespers, "A SOI-CMOS Micro-Power First-Order Sigma-Delta Modulator," *SOI Conf. Dig.*, pp. 110-111, 1996.

[39] H.-J. Song and C.-K. Kim, "A Temperature-Stabilized SOI Voltage Reference Based on Threshold Voltage Difference Between Enhancement and Depletion NMOSFET's," *IEEE J. Sol. St. Ckt*, Vol. 28, No. 6, pp. 671-677, June 1993.

[40] R. H. Walden, A. E. Schmitz, A. R. Kramer, L. E. Larson, and J. Pasiecznik, "A Deep-Submicrometer Analog-to-Digital Converter Using Focused-Ion-Beam Implants," *IEEE J. Sol. St. Ckt*, Vol. 25, No. 2, pp. 562-571, Apr. 1990.

[41] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, C. F. Edwards, R. J. T. Bunyan and M. J. Uren, "Measurement and Simulation of Self-Heating in SOI CMOS Analogue Circuits," *SOI Conf. Dig.*, pp. 156-157, 1997.

Problems

1. What are the influences of the parasitic BJT leakage from the floating body effects in the performance of the dynamic and pass-transistor based circuits using SOI devices?

2. Based on the three dynamic-threshold-voltage MOS structures in Figs. 3.6, 3.10, & 3.11, design AND and OR logic circuits. Discuss the restraints on the application of the DTMOS techniques for the dynamic circuits. Based on the three dynamic-threshold-voltage MOS structures, design a 4-bit carry look-ahead circuit using domino logic.

3. Why the DTMOS structure in Fig.3.12 can be used to reduce the gate leakage current while its performance is not affected? As shown in the figure, in the driver circuit for the power switch transistor, why some devices use DTMOS? why some not?

4. What is the influence of the parasitic BJT leakage from the floating body effect in SRAM and DRAM using SOI devices? Which circuit is more affected? Why? How can the problems be overcome from the processing technology and circuit designs?

5. When the operating temperature is changed, what are changes in the subthreshold and the strong-inversion currents of SOI MOS devices? From Figs.3.43 and 3.50, discuss the temperature effect of the SOI digital and analog circuits.

Chapter 4

SOI CMOS Devices—Basic

In the previous chapters, processing technology and properties of SOI CMOS devices and VLSI circuits using SOI CMOS devices are introduced. Compared to bulk CMOS devices, SOI CMOS devices have been reknown for their superior performance in smaller second order effects, no latchup, and higher speed. Due to their unique structure, SOI CMOS devices have performance quite different from the bulk ones. In this chapter, fundamental behaviors of SOI CMOS devices are described. Starting from the back gate bias effect, one-dimensional threshold voltage models of SOI CMOS devices are presented. Then, short and narrow channel effects of SOI CMOS devices are described. Considering both short and narrow channel effects, three-dimensional small-geometry effects on the threshold voltage are depicted. After considering the threshold voltage, the mobility model of an SOI CMOS device is analyzed. Carrier mobilities in SOI CMOS devices are complicated especially for small-geometry SOI CMOS devices. In a short-channel SOI CMOS device, the internal electric field may be high. As a result, carriers in the channel may be traveling with a large energy. Therefore, carrier temperature may be much higher than the lattice temperature. Hence, the carrier temperature effect on the mobility can not be neglected. Sometimes, carriers may be travelling at a velocity even higher than the saturated velocity—velocity overshoot. Considering carrier temperature effect, the carrier-temperature dependent mobility model has been used to derive the drain current model of the SOI CMOS devices. In the final portion of this chapter, considering the lattice temperature and the non-local high electric field effects, a comprehensive DC drain current model for a small-geometry SOI CMOS device biased in the subthreshold and strong inversion regions is described.

J. B. Kuo et al., *CMOS VLSI Engineering*

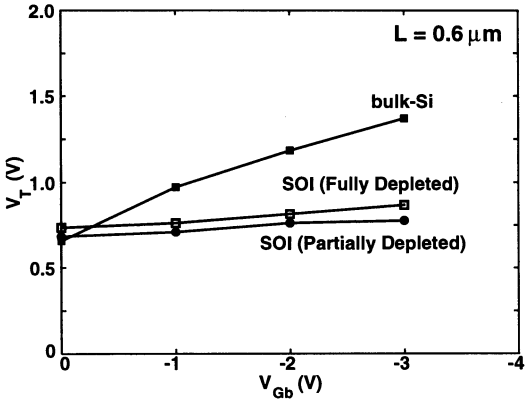


Figure 4.1: Threshold voltage versus back gate bias of an SOI NMOS device with a gate oxide of 150Å and a channel length of 0.6μm.

4.1 Back Gate Bias Effect

For an SOI CMOS device, owing to the buried oxide below the silicon thin-film, the back gate bias induced depletion region below the insulator in the substrate cannot be neglected [1]-[5]. As a result, the back gate bias effect of SOI CMOS devices is quite different from that of bulk ones. Fig. 4.1 shows the threshold voltage variation versus back gate bias of an SOI NMOS device with a gate oxide of 150Å and a channel length of 0.6μm[6]. As shown in the figure, due to the buried oxide between the silicon thin-film and the substrate, the back gate bias effect of the SOI NMOS device is smaller than that of the bulk one. From the figure, the back gate bias effect of the partially-depleted SOI device is smaller than that of the fully-depleted SOI device. For the partially-depleted SOI NMOS device, its threshold voltage is almost independent of the back gate bias due to the existence of the neutral region in the silicon thin-film— the influence of the back gate is shielded. Thus, when discussing the back gate bias effect, it is most often referred to fully-depleted devices. As shown in Fig. 4.2, the back gate bias effect on the threshold voltage can be divided into three regions[7]. For the back gate bias of between -30V and 30V, the threshold voltage is linearly proportional to the back gate bias. An increase in the back gate bias leads to a decrease in the threshold voltage. When the back gate bias is greater than 30V, the back-gate bias curve is saturated. A change in the back gate bias does not lead to a substantial deviation in the threshold voltage. Under this situation, hole accumulation at the substrate surface or strong inversion above the buried

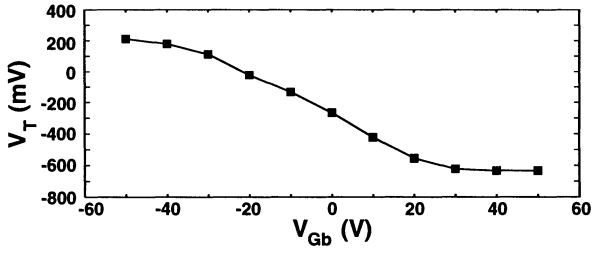


Figure 4.2: Threshold voltage versus back gate bias of an SOI NMOS device with a front gate oxide of 250Å, a buried oxide of 20000Å, a silicon thin-film of 1800Å and a p-type substrate.

oxide in the silicon thin-film may exist. As a result, the back gate bias is prevented from affecting the threshold voltage. Similarly, when the back gate bias is smaller than -30V, the curve is also saturated. Under this situation, strong inversion at the substrate surface or hole accumulation at the bottom of the silicon thin-film may occur. From the above analysis, back-gate bias effect on the threshold voltage of an SOI CMOS device is complicated. As for bulk CMOS devices, back gate bias effect is important in determining the performance of a circuit using SOI CMOS devices. In the remaining portion of this section, analytical back gate bias effect models for ultra-thin SOI CMOS devices[8] are described. First, back gate bias models for the SOI NMOS devices are analyzed, followed by those for the SOI PMOS devices.

4.1.1 NMOS device

Consider an SOI inversion-mode NMOS device using an N^+ polysilicon gate as shown in Fig. 4.3. The doping structure of the silicon thin-film in the inversion-mode SOI NMOS device is n^+-p-n^+. When the front gate is biased at its threshold voltage, at the front surface of the silicon thin-film, an electron inversion layer exists. Depending on the back gate bias, the surface of the p-type substrate under the buried oxide may be depleted— only the ionized space charge N_A^- left. In addition, an electron inversion layer may also exist at the back substrate surface. As shown in Fig.4.3, when the front gate is biased at the threshold voltage, by applying a back gate bias of -3V, there is an inversion layer under the buried oxide in the substrate[8]. Therefore, the back gate bias affects the generation of the front channel in the silicon thin-film— the threshold voltage may be affected by the back gate bias, which is the body effect of the SOI NMOS device.

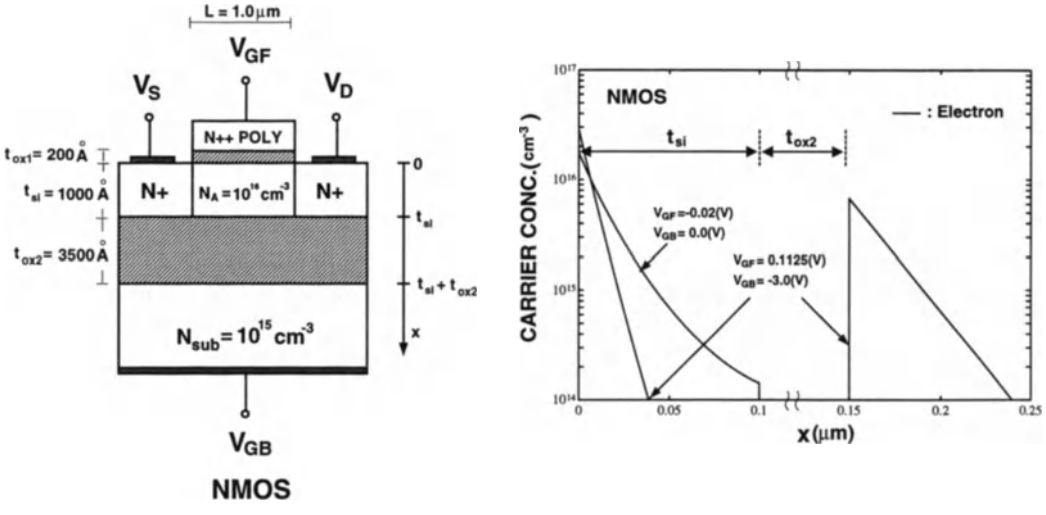


Figure 4.3: The internal carrier distributions of an inversion-mode SOI NMOS device biased without an inversion in the substrate and with an inversion in the substrate. The origin of the x axis is at the $Si - SiO_2$ interface below the front gate.

Consider the SOI NMOS device as shown in Fig. 4.3. Applying Gauss' law at the Si/SiO_2 interface under the front gate, one obtains: $C_{ox1}(\Psi_{GF} - \Psi_{s1}) = \epsilon_{si}E_{s1}$, where C_{ox1} is the unit area front gate oxide capacitance, $\Psi_{GF}(= -\phi_{F(POLY)} + V_{GF})$ is the electrostatic potential of the front polysilicon gate, Ψ_{s1} is the electrostatic potential at the Si/SiO_2 interface under the front gate, and E_{s1} is the electric field at the surface of the silicon thin-film under the front gate. From Kirchoff's voltage law, the electrostatic potential at the substrate surface under the buried oxide is: $\Psi_{s3} = \Psi_{s2} - \frac{\epsilon_{si}}{C_{ox2}}E_{s2}$, where Ψ_{s2} ad E_{s2} are the electrostatic potential and the electric field at the back surface of the silicon thin-film above the buried oxide, respectively. C_{ox2} is the unit area buried oxide capacitance.

Assuming no interface charge at the Si/SiO_2 interface, the electric field at the back surface of the silicon thin-film above the buried oxide is equal to the electric field below the buried oxide at the substrate surface: $E_{s2} = E_{s3}$, where E_{s3} is the electric field at the surface of the substrate surface below the buried oxide. When the device is biased at the threshold voltage, the silicon thin-film is fully depleted,

the Poisson's equation becomes:

$$\frac{\partial^2\Psi}{\partial x^2} = \frac{q}{\epsilon_{si}}(N_A + n - p) \cong \frac{q}{\epsilon_{si}}N_A. \tag{4.1}$$

Integrating Eq.(4.1), the electric field and the electrostatic potential above the buried oxide in the silicon thin-film are: $E_{s2} = E_{s1} - \frac{qN_A}{C_s}$, $\Psi_{s2} = \Psi_{s1} - E_{s1}t_{si} + \frac{qN_A}{2\epsilon_{si}}{t_{si}}^2$, where C_s is the unit area thin-film capacitance ($C_s = \epsilon_{si}/t_{si}$). Below the buried oxide in the p-type substrate, the Poisson's equation is:

$$\frac{\partial^2\Psi}{\partial x^2} = \frac{q}{\epsilon_{si}}(N_{sub} + n - p) = \frac{q}{\epsilon_{si}}(N_{sub} + n_0 e^{\Psi(x)/\frac{kT}{q}} - p_0 e^{-\Psi(x)/\frac{kT}{q}}), \tag{4.2}$$

where N_{sub} is the substrate doping density, $\Psi(x)$ is the electrostatic potential, and n_o and p_o are the electron and hole densities in the neutral substrate region, respectively.

From Eq.(4.2) and the relationship: $2\frac{\partial\Psi}{\partial x}\frac{\partial^2\Psi}{\partial x^2} = \frac{\partial}{\partial x}((\frac{\partial\Psi}{\partial x})^2)$, the electric field under the buried oxide in the substrate is:

$$\begin{aligned} E_{s3} &= \pm\sqrt{2\frac{q}{\epsilon_{si}}\int_{\Psi_{sub}}^{\Psi_{s3}}(N_{sub} + n_0 e^{\Psi/\frac{kT}{q}} - p_0 e^{-\Psi/\frac{kT}{q}})\partial\Psi} \qquad (4.3)\\ &= \pm\sqrt{2q[N_{sub}(\Psi_{s3} - \Psi_{sub}) + \frac{kT}{q}n_0(e^{\frac{\Psi_{s3}}{\frac{kT}{q}}} - e^{\frac{\Psi_{sub}}{\frac{kT}{q}}}) + \frac{kT}{q}\frac{p_0}{\epsilon_{si}}(e^{\frac{-\Psi_{s3}}{\frac{kT}{q}}} - e^{\frac{-\Psi_{sub}}{\frac{kT}{q}}})]}, \end{aligned}$$

where $\Psi_{sub}(= V_{GB} - \phi_{Fsub})$ is the electrostatic potential in the neutral substrate, and $\phi_{Fsub} = \frac{kT}{q}ln(\frac{N_{sub}}{n_i})$. If $\Psi_{s3} < \Psi_{sub}$, holes are accumulated at the surface of the substrate, therefore, the negative sign should be chosen in the above equation. From Eq. (4.3), two equations in terms of Ψ_{s3} and Ψ_{s1} can be obtained:

$$\Psi_{s3} = (1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox1}}{C_{ox2}})\Psi_{s1} + \frac{qN_A}{2\epsilon_{si}}{t_{si}}^2 + \frac{q\epsilon_{si}N_A}{C_{ox2}C_s} - (\frac{C_{ox1}}{C_s} + \frac{C_{ox1}}{C_{ox2}})\Psi_{GF}, \tag{4.4}$$

$$\begin{aligned} \frac{C_{ox1}}{\epsilon_{si}}(\Psi_{GF} - \Psi_{s1}) - \frac{qN_A}{C_s} &= \sqrt{2q[N_{sub}(\Psi_{s3} - \Psi_{sub}) + \frac{kT}{q}n_0 e^{\frac{\Psi_{s3}}{\frac{kT}{q}}}]/\epsilon_{si}} \quad \Psi_{s3} > \Psi_{sub},\\ &= -\sqrt{2q[N_{s\cdot b}(\Psi_{s3} - \Psi_{sub}) + \frac{kT}{q}p_0 e^{\frac{-\Psi_{s3}}{\frac{kT}{q}}}]/\epsilon_{si}} \quad \Psi_{s3} < \Psi_{sub}. \end{aligned} \tag{4.5}$$

From Eqs.(4.4)&(4.5), Ψ_{s1} and Ψ_{s3} can be obtained. When strong inversion does not exist at the surface of the substrate ($\Psi_{sub} < \Psi_{s3} < \Psi_{sub} + 2\phi_{Fsub}$), Eq.(4.5) is simplified to $\frac{C_{ox1}}{\epsilon_{si}}(\Psi_{GF} - \Psi_{s1}) - \frac{qN_A}{C_s} \cong \sqrt{\frac{2qN_{sub}(\Psi_{s3}-\Psi_{sub})}{\epsilon_{si}}}$. From Eq.(4.4), the electrostatic potential and the electric field at the surface of the silicon thin-film under the front gate are: $\Psi_{s1} = \frac{B}{2A} - \frac{1}{2A}\sqrt{B^2 - 4AC}$, $E_{s1} = \alpha + \sqrt{\beta + \frac{2qN_{sub}}{\epsilon_{si}}\Psi_{s1}}$, where $A = (\frac{C_{ox1}}{\epsilon_{si}})^2$, $B = 2(\frac{C_{ox1}}{\epsilon_{si}}\Psi_{GF} - \alpha)\frac{C_{ox1}}{\epsilon_{si}} + \frac{2qN_{sub}}{\epsilon_{si}}$, $C = (\frac{C_{ox1}}{\epsilon_{si}}\Psi_{GF} - \alpha)^2 - \beta$, $\alpha = \frac{qN_A}{C_s} - qN_{sub}(\frac{1}{C_s} + \frac{1}{C_{ox2}})$, and $\beta = (qN_{sub})^2(\frac{1}{C_s} + \frac{1}{C_{ox2}})^2 - (\frac{q}{C_s})^2 N_A N_{sub} + \frac{2qN_{sub}}{\epsilon_{si}}(-\Psi_{sub})$. The channel of an SOI NMOS device can be located at the top or at the bottom of the silicon thin-film. Therefore, the threshold voltage is defined as the front gate voltage when at a specific back gate bias the elecrostatic potential at the top of the silicon thin-film under the front gate (Ψ_{s1}) or the electrostatic potential at the top of the buried oxide in the silicon thin-film (Ψ_{s2}) reaches ϕ_F, where $\phi_F = \frac{kT}{q}(\frac{N_A}{n_i})$ is for the inversion-mode SOI NMOS devices, and n_i is the intrinsic carrier density. For an inversion-mode SOI NMOS device, strong inversion always occurs at the front surface. Therefore, the threshold voltage is defined as the front gate voltage when the electrostatic potential at the surface of the silicon thin-film under the gate (Ψ_{s1}) reaches ϕ_F: $E_{s1}(\Psi_{s1} = \phi_F) = \sqrt{\beta + \frac{2qN_{sub}}{\epsilon_{si}}\phi_F}$. Therefore, the threshold voltage is:

$$V_{TH} = \phi_F + \frac{\epsilon_{si}}{C_{ox1}}(\alpha + \sqrt{\beta + \frac{2qN_{sub}}{\epsilon_{si}}\phi_F}) + \phi_{F(POLY)}, \tag{4.6}$$

where $\phi_{F(POLY)}$ is the quasi-Fermi potential of the N^+ poly gate. Eq.(4.6) is applicable when strong inversion does not exist at the substrate surface under the buried oxide ($\Psi_{s3} < 2\phi_{Fsub} + \Psi_{sub}$). When strong inversion does occur at the substrate surface under the buried oxide ($\Psi_{s3} = 2\phi_{Fsub} + \Psi_{sub}$), the threshold voltage formula becomes:

$$V_{TH} = (\frac{C_{ox1}}{C_s} + \frac{C_{ox1}}{C_{ox2}})^{-1}[(1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox1}}{C_{ox2}})\phi_F + \frac{qN_A}{2\epsilon_{si}}t_{si}^2 + \frac{q\epsilon_{si}N_A}{C_{ox2}C_s} - (2\phi_{Fsub} + \Psi_{sub})] + \phi_{F(POLY)}. \tag{4.7}$$

Eqs.(4.6)(4.7) are the threshold voltage formulas for the SOI NMOS device. When V_{GB} is greater than the back gate voltage such that $\Psi_{s3} = 2\phi_{Fsub} + \Psi_{sub}$ and $\Psi_{s1} = \phi_F$, no strong inversion exists at the substrate surface, hence Eq.(4.6) should be used. Otherwise, Eq.(4.7) should be used. Based on Eqs.(4.6)(4.7), Fig. 4.4 shows the threshold voltage versus back gate bias for the SOI NMOS device. A more negative V_{GB} leads to a larger V_{TH}[8].

4.1.2 PMOS device

Using an N^+ polysilicon gate, the enhancement-type SOI PMOS device can be inversion-mode or accumulation-mode. The doping structure in the silicon thin-

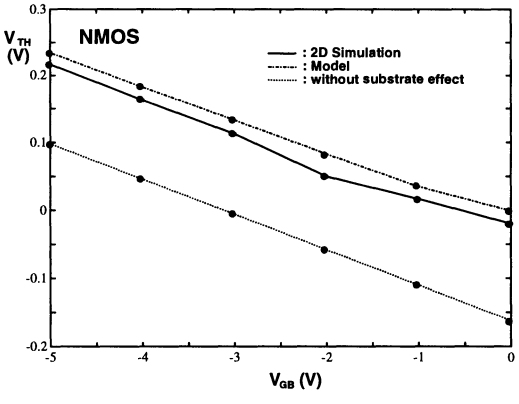


Figure 4.4: Threshold voltage of the SOI NMOS device biased at V_{GB} from 0 to -5V.

film of the inversion-mode SOI PMOS device is p^+-n-p^+. In the accumulation-mode SOI PMOS device, it is p^+-p-p^+. As shown in Fig. 4.5, at the threshold voltage, depending on the back gate bias, the channel with strong inversion may be at the top or at the bottom of the silicon thin-film of the inversion-mode PMOS device[8]. In addition, at the substrate surface under the buried oxide, strong inversion may also exist. At $V_{GB} = 0$, the influence of the back gate is small. When the front gate voltage is at the threshold voltage ($V_{GF} = V_{TH}$), the surface channel exists at the top of the silicon thin-film. At $V_{GB} = -1.6V$, at the threshold voltage ($V_{GF} = V_{TH}$), the buried channel exists at the bottom of the silicon thin-film. When the back gate bias is very negative ($V_{GB} = -3V$), at the threshold voltage ($V_{GF} = V_{TH}$), in addition to the buried channel in the silicon thin-film, strong inversion exists at the substrate surface.

When an accumulation-mode SOI PMOS device is biased at the threshold voltage, a buried channel exists in the silicon thin-film. At a back gate bias of $V_{GB} = 0$, at the threshold voltage ($V_{GF} = V_{TH}$), the buried channel in the silicon thin-film widens. In addition, hole accumulation exists at the substrate surface under the buried oxide. When the back gate bias is $V_{GB} = -1V$, at the threshold voltage ($V_{GF} = V_{TH}$), the buried channel in the silicon thin-film becomes narrower. In addition, the substrate surface is depleted. When the back gate bias is $V_{GB} = -3V$, at the threshold voltage ($V_{GF} = V_{TH}$), in addition to the buried channel in the silicon thin-film, strong inversion exists at the substrate surface.

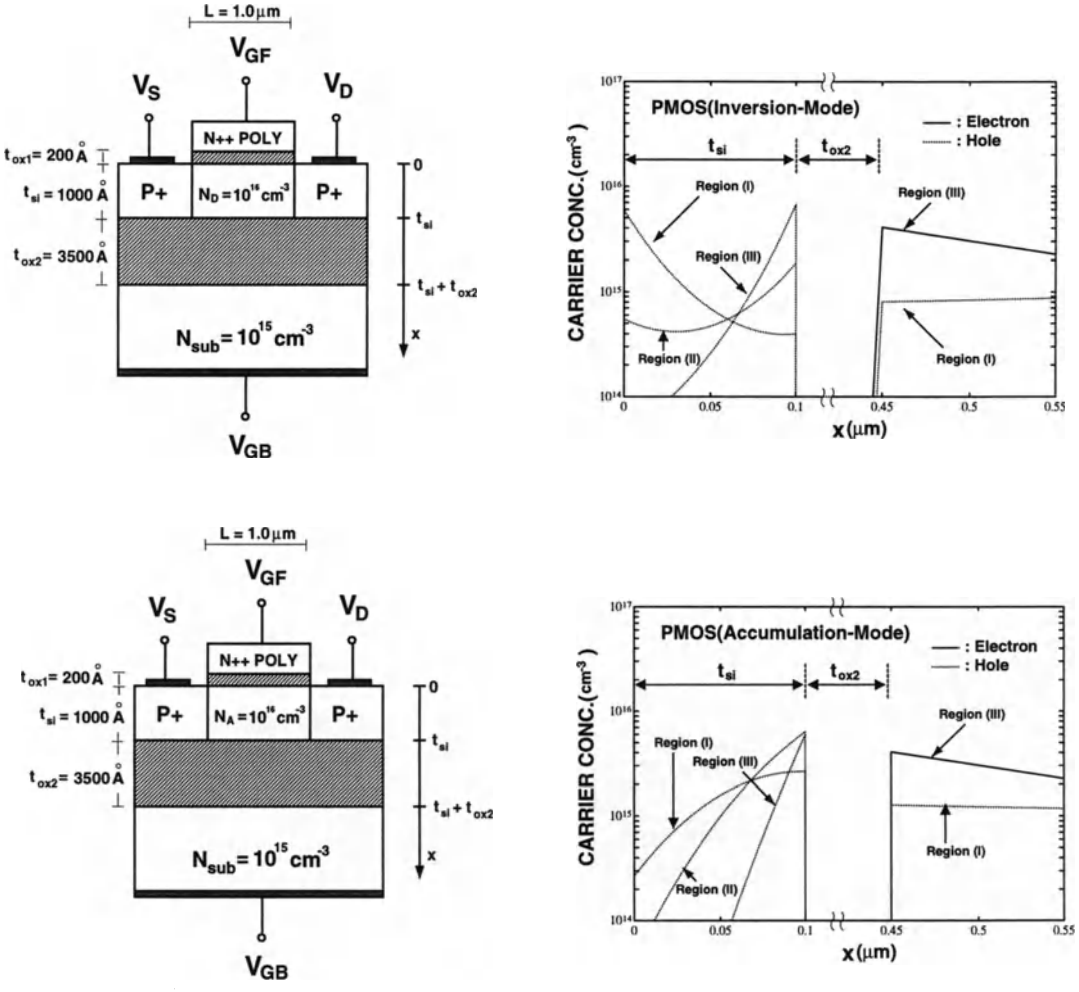


Figure 4.5: The internal carrier distributions in the inversion-mode and the accumulation-mode SOI PMOS devices.

For the inversion-mode SOI PMOS device as shown in Fig. 4.5, at the threshold voltage ($V_{GF} = V_{TH}$), in the silicon thin-film, a surface channel or a buried channel may exist. With a surface channel, the electrostatic potential at the surface of the silicon thin-film under the front gate is less than the electrostatic potential above the buried oxide in the silicon thin-film ($\Psi_{s1} < \Psi_{s2}$). Therefore, $E_{s2} < \frac{qN_D}{2C_s}$. From Eq.(4.3), one obtains: $N_{sub}(\Psi_{s3} - \Psi_{sub}) + \frac{kT}{q} n_0 e^{\Psi_{s3}/\frac{kT}{q}} < \frac{q\epsilon_{si}N_D^2}{8C_s^2}$. Since $\frac{q\epsilon_{si}N_D^2}{8C_s^2} \ll 2\phi_{Fsub}N_{sub}$, therefore, when a surface channel exists ($\Psi_{s1} < \Psi_{s2}$), there is no inversion at the substrate surface ($\Psi_{s3} - \Psi_{sub} < 2\phi_{Fsub}$). Thus, the threshold voltage formula for the SOI PMOS device is:

$$V_{TH} \equiv V_{GF}(\Psi_{s1} = \phi_F) = \phi_F + \frac{\epsilon_{si}}{C_{ox1}}(\alpha + \sqrt{\beta + \frac{2qN_{sub}}{\epsilon_{si}}\phi_F}) + \phi_{F(POLY)}, \quad (4.8)$$

where $\phi_F = \frac{kT}{q} ln \frac{n_i}{N_D}$ for the inversion-mode SOI PMOS devices. In contrast to Eq. (4.8), when $E_{s2} > (qN_D/2C_s)$, a buried channel dominates in the silicon thin-film. Under this situation, the threshold voltage formula is:

$$\begin{aligned} V_{TH} &\equiv V_{GF}(\Psi_{s2} = \phi_F), \\ &= \phi_F + [E_{s2}(\Psi_{s2} = \phi_F) - \frac{qN_D}{C_s}]t_{si} + \frac{q}{2\epsilon_{si}}N_D t_{si}^2 \\ &\quad + \frac{\epsilon_{si}}{C_{ox1}}[E_{s2}(\Psi_{s2} = \phi_F) - \frac{qN_D}{C_s}] + \phi_{F(POLY)}, \end{aligned} \quad (4.9)$$

where $E_{s2}(\Psi_{s2} = \phi_F) = -\frac{qN_{sub}}{C_{ox2}} + \sqrt{(\frac{qN_{sub}}{C_{ox2}})^2 + \frac{2qN_{sub}}{\epsilon_{si}}(\phi_F - \Psi_{sub})}$. Define V_{TR} as the back gate bias (V_{GB}) at the threshold voltage ($V_{GF} = V_{TH}$) when the electric field in the buried channel reaches $qN_D/2C_s$:

$$V_{TR} = \frac{\epsilon_{si}}{2qN_{sub}}[(\frac{qN_{sub}}{C_{ox2}})^2 + \frac{2qN_{sub}}{\epsilon_{si}}\phi_F - (\frac{qN_D}{2C_s} + \frac{qN_{sub}}{C_{ox2}})^2] + \phi_{F,sub}. \quad (4.10)$$

When $V_{GB} > V_{TR}$, Eq.(4.8) is the threshold voltage formula. When $V_{GB} < V_{TR}$, Eq.(4.9) is the threshold voltage formula. When $V_{GB} < V_{TR}$, if V_{GB} becomes more negative, inversion may exist at the substrate surface. With an inversion at the substrate surface, at the threshold voltage ($V_{GF} = V_{TH}$), the back gate bias voltage is defined as V_{BP}:

$$V_{BP} = \phi_F - \frac{1}{C_{ox2}}\sqrt{2q\epsilon_{si}N_{sub}(2\phi_{F,sub})} - \phi_{F,sub}. \quad (4.11)$$

Under this situation, for $V_{GB} < V_{BP}$, the threshold voltage is:

$$\begin{aligned} V_{TH} &= V_{GF}(\Psi_{s2} = \phi_F, \Psi_{s3} \cong \Psi_{sub} + 2\phi_{F,sub}) \\ &= \phi_F + \frac{q}{2\epsilon_{si}} N_D t_{si}^2 + \frac{\epsilon_{si}}{C_{ox1}}(1 + \frac{C_{ox1}}{C_s})[\frac{C_{ox2}}{\epsilon_{si}}(\phi_F - 2\phi_{F,sub} - \Psi_{sub}) - \frac{qN_D}{C_s}] + \phi_{f(poly)}. \end{aligned} \tag{4.12}$$

When the accumulation-mode SOI PMOS device is biased at the threshold voltage, a buried channel exists in the silicon thin-film. Under this situation, depending on the back gate bias, at the substrate surface, accumulation, depletion, or inversion may exist. At the threshold voltage, if accumulation exists at the substrate surface, the electrostatic potential at the substrate surface is $\Psi_{s3} = \Psi_{sub}$. The buried channel in the silicon thin-film is not on the buried oxide. Instead, it is at $x = x_{ch}$, where the electric field is zero ($E(x = x_{ch}) = 0$). Integrating the Poisson's equation from the front oxide interface to $x = x_{ch}$, one obtains $x_{ch} = \frac{\epsilon_{si} E_{s1}}{qN_A}$ and $\Psi(x = x_{ch}) = \Psi_{s1} - \frac{\epsilon_{si}}{2qN_A} E_{s1}^2$. From Eq.(4.4), the threshold voltage is defined as the front gate voltage when the potential in the buried channel reaches $\Psi_{ch} = -\phi_F$: $V_{TH} = -a_1 - \sqrt{a_1^2 - a_2} + \phi_{F(POLY)}$, where $a_1 = L - \frac{C_{ox1}^2}{q\epsilon_{si}N_A} M^2$, $a_2 = L^2 - M^2 + \frac{2C_{ox1}^2}{q\epsilon_{si}N_A} M^2(-\phi_F)$, $L = \frac{qN_A}{2\epsilon_{si}} t_{si}^2 + \frac{q\epsilon_{si}N_A}{C_{ox2}C_s} + (1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox1}}{C_{ox2}}) \frac{q\epsilon_{si}N_A'}{C_{ox1}^2} - \Psi_{sub}$, and $M = (1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox1}}{C_{ox2}})(\frac{q\epsilon_{si}N_A}{C_{ox1}^2})$, where $\phi_F = \frac{kT}{q} ln \frac{N_A}{n_i}$ for the accumulation-mode SOI PMOS devices. At the threshold voltage, if a depletion region exists at the substrate surface and the buried channel exists on the top of the buried oxide, then the potential at the substrate surface is $\Psi_{s2} = -\phi_F$. From Eq. (4.3), the threshold voltage formula is:

$$\begin{aligned} V_{TH} = -\phi_F - \frac{qN_A}{2\epsilon_{si}} t_{si}^2 &+ (1 + \frac{C_{ox1}}{C_s}) \frac{1}{C_{ox1}} (qN_A t_{si} - \frac{q\epsilon_{si}N_{sub}}{C_{ox2}} \\ &+ \sqrt{2q\epsilon_{si}N_{sub}(-\phi_F - \Psi_{sub}) + (\frac{q\epsilon_{si}N_{sub}}{C_{ox2}})^2}) + \phi_{F(POLY)}. \end{aligned} \tag{4.13}$$

When inversion exists at the substrate surface ($\Psi_{s3} = 2\phi_{Fsub} + \Psi_{sub}$), the threshold voltage formula is:

$$V_{TH} = (1 + \frac{C_{ox2}}{C_s} + \frac{C_{ox2}}{C_{ox1}})(-\phi_F) - (\frac{C_{ox2}}{C_s} + \frac{C_{ox2}}{C_{ox1}})(\phi_{F,sub} + V_{GB}) + \frac{qN_A}{2\epsilon_{si}} t_{si}^2 + \frac{qN_A t_{si}}{C_{ox1}} + \phi_{F(POLY)}. \tag{4.14}$$

At the threshold voltage, if accumulation exists at the substrate surface, the back gate bias is: $V_{TR} \equiv -\phi_F + \phi_{F,sub}$. At the threshold voltage, when $V_{GB} > V_{TR}$, hole accumulation exists at the substrate surface. When $V_{GB} < V_{TR}$, the substrate surface is depleted. At the threshold voltage, when the potential of the substrate surface reaches $\Psi_{s3} = 2\phi_{Fsub} + \Psi_{sub}$, the back gate bias is:

$$V_{BP} = -\phi_F - \frac{1}{C_{ox2}} \sqrt{2\epsilon_{si}N_{sub}(2\phi_{F,sub})} - \phi_{F,sub}. \tag{4.15}$$

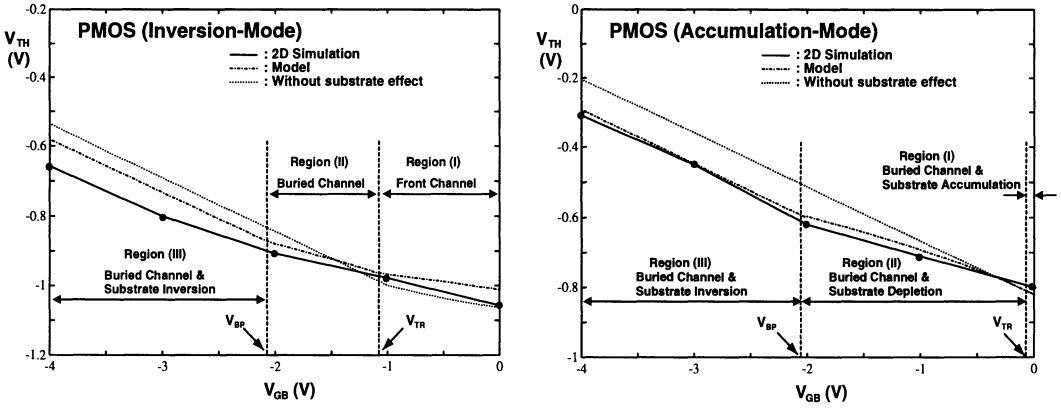


Figure 4.6: Threshold voltage versus V_{GB} of the SOI PMOS devices.

When $V_{GB} < V_{BP}$, inversion exists at the substrate surface. Fig. 4.6 shows the threshold voltage versus the back gate bias of the inversion-mode and the accumulation-mode SOI PMOS devices [8]. In contrast to the bulk PMOS devices, the back gate bias effect of the SOI PMOS devices is complicated.

4.2 Short-Channel Effect

For small-geometry SOI CMOS devices, short-channel effects are important[9]-[13][15]-[17]. The short channel effect of an SOI CMOS device is similar to that of the bulk CMOS device. Fig. 4.7 shows the threshold voltage versus effective channel length of an SOI PMOS device with a front gate oxide of 150Å, a silicon thin-film of 2200Å, and a buried oxide of 4000Å[9]. As shown in the figure, the SOI MOS device has a similar trend in the short channel effect on the threshold voltage as for bulk devices. When the channel length of a SOI PMOS device is shrunk, its threshold voltage is decreased. Compared to the bulk device, the short channel effect of the SOI MOS device is smaller—the change in the threshold voltage is smaller. Fig. 4.8 shows the short channel effect of two SOI NMOS devices with the double-gate and the single-gate structures. When the channel length becomes smaller, the threshold voltage for both devices becomes smaller [10]. Compared to the single-gate ones, double-gate (DG) fully-depleted SOI MOS devices have been known for their advantages in enhanced current density, and reduced second-order effects [10]-[12]. Compared to single-gate devices, the threshold voltage of the double-gate devices may be difficult to define due to the co-existence of the front and the back channels. For a

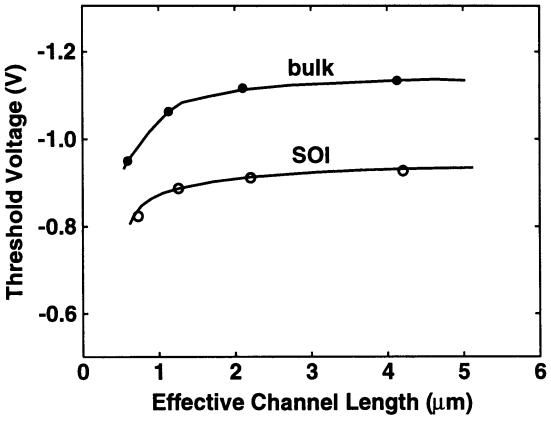


Figure 4.7: Threshold voltage versus effective channel length of an SOI PMOS device with a front gate oxide of 150Å, a silicon thin-film of 2200Å, and a buried oxide of 4000Å.

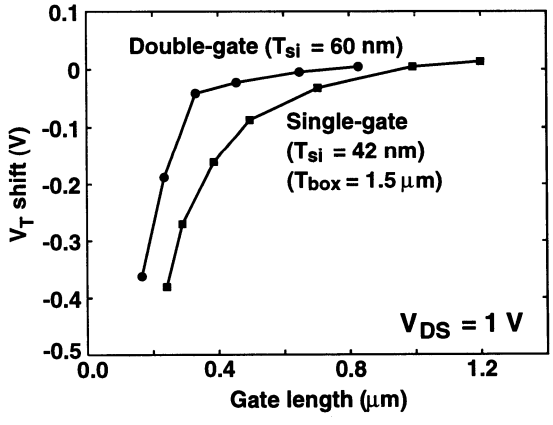


Figure 4.8: Threshold voltage versus channel length of a double-gate and a single-gate SOI NMOS device with a front gate oxide of 110Å. The double-gate one has a silicon thin-film of 600Å. The single-gate one has a silicon thin-film of 420Å and a buried oxide of 1.5μm.

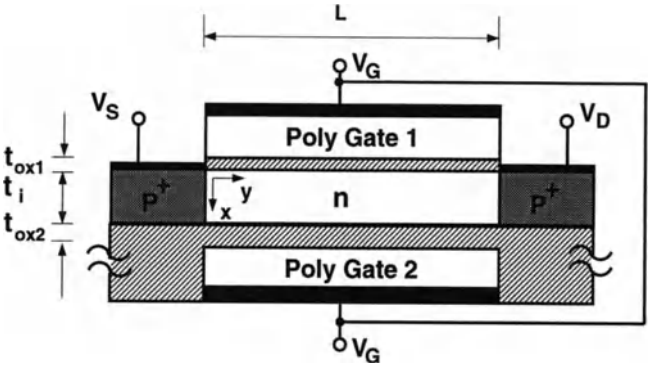


Figure 4.9: Cross section of double-gate fully-depleted SOI PMOS device.

single-gate SOI PMOS device, depending on the back gate bias, surface channel or buried channel may dominate. If surface channel dominates, the threshold voltage of the single-gate SOI PMOS device is defined in the previous section as the surface electrostatic potential at the Si/SiO_2 interface reaches $\Psi_{s1} = -\phi_{fn}$, where $\phi_{fn} = \frac{kT}{q} \ln \frac{N_D}{n_i}$, n_i is the intrinsic carrier concentration, N_D is the doping density of the silicon thin-film, k is Boltzmann constant, T is temperature in Kelvin, and q is the electronic charge. If the buried channel dominates, the threshold voltage is defined as the gate voltage when the electrostatic potential above the buried oxide reaches $\Psi_{s2} = -\phi_{fn}$. For the double-gate SOI MOS devices, there is no body effect. However, due to the double poly-gate structure, the front channel and the back channel may co-exist. Therefore, the threshold voltage model of the double-gate SOI MOS devices is more difficult to define. As for the bulk MOS devices [14], the short-channel effect threshold voltage is important for assessing device performance and gaining insights into device designs. In this section, a concise short-channel effect threshold voltage model for short-channel double-gate SOI PMOS devices [13] is described.

Fig. 4.9 shows the cross section of the double-gate fully-depleted SOI PMOS device under study[13]. In the following derivation, it is divided into the 1D long-channel and the quasi-2D short-channel analysis. Assuming that the silicon thin-film is fully depleted, solving Poisson's equation in the substrate direction as in the previous section ($x = 0$ is at the front $Si - SiO_2$ interface), the electrostatic potential at the back interface ($x = t_i$) is: $\Psi_{s2} = -\frac{qN_D}{2C_s} t_i - E_{s1} t_i + \Psi_{s1}$, where t_i is silicon thin-film thickness, $C_s = \frac{\epsilon_{si}}{t_i}$, ϵ_{si} is the silicon permittivity, E_{s1} is the electric field at the front Si/SiO_2 interface in the silicon thin-film: $E_{s1} = \frac{-\frac{qN_D}{2C_s} C_{ox2} t_i + C_{ox2}(\Psi_{s1} - \phi_{f2(poly)}) - \frac{qN_D}{C_s}\epsilon_{si}}{\epsilon_{si} + C_{ox2} t_i} -$

$\frac{C_{ox2}}{\epsilon_{si}+C_{ox2}t_i}V_G$, V_G is the gate voltage, $\phi_{f1(poly)}$ and $\phi_{f2(poly)}$ are the quasi-Fermi potential of the front and the back poly gates, respectively. For an N^+ poly gate, the quasi-Fermi potential is 0.465V. For a P^+ poly gate, the quasi-Fermi potential is -0.517V. $C_{ox2} = \frac{\epsilon_{ox}}{t_{ox2}}$. t_{ox2} is the thickness of the back oxide. ϵ_{ox} is oxide permittivity. Applying Gauss' law at the front $Si - SiO_2$ interface in the silicon thin-film, one obtains: $V_G = \frac{-\frac{qN_D}{2C_s}C_{ox2}t_i - \frac{qN_D}{C_s}\epsilon_{si} - C_{ox2}\phi_{f2(poly)} - (1+\frac{C_{ox2}}{C_s})C_{ox1}\phi_{f1(poly)}}{C_{ox1}+C_{ox2}+C_{ox1}C_{ox2}C_s^{-1}} + \Psi_{s1}$, which is referred to the front surface electrostatic potential (Ψ_{s1}). $C_{ox1} = \frac{\epsilon_{ox}}{t_{ox1}}$. t_{ox1} is the thickness of the front oxide. Owing to the symmetry of the double-gate structure, by exchanging "1" with "2", one obtains: $V_G = \frac{-\frac{qN_D}{2C_s}C_{ox1}t_i - \frac{qN_D}{C_s}\epsilon_{si} - C_{ox1}\phi_{f1(poly)} - (1+\frac{C_{ox1}}{C_s})C_{ox2}\phi_{f2(poly)}}{C_{ox1}+C_{ox2}+C_{ox1}C_{ox2}C_s^{-1}} + \Psi_{s2}$, which is referred to the back surface electrostatic potential (Ψ_{s2}).

If the front channel dominates, Ψ_{s1} is the dominant factor in determining the threshold voltage. If the back channel dominates, Ψ_{s2} is the dominant factor. Therefore, a concise threshold voltage model is difficult to obtain. In order to overcome the difficulties, the threshold voltage is defined as the gate voltage when sum of hole densities at the back and the front surfaces reaches the doping density of the silicon thin-film: $n_i e^{-\frac{\Psi_{s1}}{kT/q}} + n_i e^{-\frac{\Psi_{s2}}{kT/q}} = N_D$. At the threshold voltage, the electrostatic potential at the front surface (Ψ_{s1t}) and the back surface (Ψ_{s2t}) for the long channel devices can be obtained. Therefore, the threshold voltage is defined as the gate voltage when its front surface electrostatic potential reaches ($\Psi_{s1} = \Psi_{s1t}$) or its back surface electrostatic potential reaches ($\Psi_{s2} = \Psi_{s2t}$): $V_{TH(L)} \equiv V_G|_{\Psi_{s1}=\Psi_{s1t}, or \Psi_{s2}=\Psi_{s2t}}$. So far, the long-channel threshold voltage model has been described. In the following portion of this section, the short-channel threshold voltage model is derived.

For a short-channel double-gate SOI PMOS device, the 2D Poisson's equation is required:

$$\frac{d^2\Psi(x,y)}{dx^2} + \frac{d^2\Psi(x,y)}{dy^2} = -\frac{qN_D}{\epsilon_{si}}, \tag{4.16}$$

where y is in the lateral channel direction, and $\Psi(x, y)$ is the electrostatic potential at location (x,y) in the silicon thin-film. Using a parabolic approximation approach for the device [15]-[17], from the 2D Poisson's equation, the electrostatic potential is:

$$\Psi(x,y) = P_0(y) + P_1(y)x + P_2(y)x^2. \tag{4.17}$$

The boundary conditions for Eq. (4.16) are: at the front and the back silicon thin-film interfaces, the displacement is continuous:

$$-\frac{d\Psi(x,y)}{dx}|_{(x=0)} = \frac{C_{ox1}}{\epsilon_{si}}(V_G + \phi_{f1(poly)} - \Psi_s(y)), \tag{4.18}$$

$$-\frac{d\Psi(x,y)}{dx}|_{(x=t_i)} = \frac{C_{ox2}}{\epsilon_{si}}(\Psi_b(y) - V_G - \phi_{f2(poly)}),$$

where $\Psi_s(y)$ and $\Psi_b(y)$ are the lateral electrostatic potential at the front surface ($\Psi(0,y) = \Psi_s(y)$), and at the back surface ($\Psi(t_i,y) = \Psi_b(y)$), respectively. From Eqs. (4.17)-(4.18), one obtains:

$$\begin{aligned} P_0(y) &= \Psi_s(y), \\ P_1(y) &= \frac{C_{ox1}}{\epsilon_{si}}(\Psi_s(y) - V_G - \phi_{f1(poly)}), \\ P_2(y) &= \frac{-(1+\frac{C_{ox1}}{C_s}+\frac{C_{ox1}}{C_{ox2}})\Psi_s(y) + (1+\frac{C_{ox1}}{C_s}+\frac{C_{ox1}}{C_{ox2}})V_G + (\frac{C_{ox1}}{C_s}+\frac{C_{ox1}}{C_{ox2}})\phi_{f1(poly)} + \phi_{f2(poly)}}{t_i^2(1+\frac{2C_s}{C_{ox2}})}. \end{aligned} \tag{4.19}$$

Using a similar approach as in Refs.[15]-[17] to assume that at any depth in the silicon thin-film the derivative of the lateral electric field can be related to the derivative of the lateral electric field at the front $Si - SiO_2$ surface as:

$$\frac{d^2\Psi(x,y)}{dy^2} \cong \frac{1}{k_s}\frac{d^2\Psi_s(y)}{dy^2}, \tag{4.20}$$

where k_s is a parameter to account for the correlation between the derivative of the lateral electric field at any depth in the silicon thin-film and the derivative of the lateral electric field at the front $Si - SiO_2$ surface. Note that for a silicon thin-film with a very small thickness or with a lightly doping density, k_s is 1 [15]. Here, for general cases, k_s may be smaller than 1. From Eqs. (4.16)(4.17)(4.19)(4.20), one obtains a differential equation in terms of $\Psi_s(y)$:

$$\begin{aligned} \frac{d^2\Psi_s(y)}{dy^2} &- k_s\frac{(1+\frac{C_{ox1}}{C_s}+\frac{C_{ox1}}{C_{ox2}})}{\frac{1}{2}t_i^2(1+\frac{2C_s}{C_{ox2}})}\Psi_s(y) \\ &= k_s(-\frac{qN_D}{\epsilon_{si}} - \frac{(1+\frac{C_{ox1}}{C_s}+\frac{C_{ox1}}{C_{ox2}})V_G + (\frac{C_{ox1}}{C_s}+\frac{C_{ox1}}{C_{ox2}})\phi_{f1(poly)} + \phi_{f2(poly)}}{\frac{1}{2}t_i^2(1+\frac{2C_s}{C_{ox2}})}). \end{aligned} \tag{4.21}$$

Solving Eq. (4.21) with boundary conditions: at the source/drain, $\Psi_s(0) = \Psi_s(L) = -\frac{kT}{q}\ln\frac{N_A}{n_i}$ (at $V_S = V_D = 0V$), where L is the channel length, and N_A is the doping density in the source/drain, one obtains the electrostatic potential at the front surface:

$$\Psi_s(y) = \Psi_{s1} + C_1 e^{\sqrt{a}y} + C_2 e^{-\sqrt{a}y}, \tag{4.22}$$

where $a = \frac{(1+\frac{C_{ox1}}{C_s}+\frac{C_{ox1}}{C_{ox2}})}{\frac{1}{2}t_i^2(1+\frac{2C_s}{C_{ox2}})}k_s$, $C_1 = (\frac{(\Psi_s(0)-\Psi_{s1})(1-e^{-\sqrt{a}L})}{1-e^{-2\sqrt{a}L}})e^{-\sqrt{a}L}$, and $C_2 = \frac{(\Psi_s(0)-\Psi_{s1})(1-e^{-\sqrt{a}L})}{1-e^{-2\sqrt{a}L}}$. From Eq. (4.22), the front surface electrostatic potential has a maximum value in the center of the channel ($\Psi_{s1(max)} = \Psi_s(y = \frac{L}{2})$): $\Psi_{s1(max)} = \Psi_{s1} + (\Psi_s(0) - \Psi_{s1})A$, where $A = (1 - e^{-\sqrt{a}L})\frac{e^{-\frac{\sqrt{a}}{2}L}}{1-e^{-2\sqrt{a}L}}$. Using a similar approach as for Eqs. (4.21)(4.22), the maximum value of the electrostatic potential at the back surface is: $\Psi_{s2(max)} = \Psi_{s2} + (\Psi_s(0) - \Psi_{s2})B$, where $B = (1 - e^{-\sqrt{b}L})\frac{e^{-\frac{\sqrt{b}}{2}L}}{1-e^{-2\sqrt{b}L}}$, $b = \frac{(1+\frac{C_{ox2}}{C_s}+\frac{C_{ox2}}{C_{ox1}})}{\frac{1}{2}t_i^2(1+\frac{2C_s}{C_{ox1}})}k_s$.

The threshold voltage of a short-channel double-gate SOI PMOS device is defined as the gate voltage when the sum of hole densities in the center of channel at the back and the front surfaces reaches the doping density of the silicon thin-film: $n_i e^{-\frac{\Psi_{s1(max)}}{kT/q}} + n_i e^{-\frac{\Psi_{s2(max)}}{kT/q}} = N_D$. Therefore, $\Psi_{s2(max)}$ is: $\Psi_{s2(max)} = (\frac{1-B}{1-A})\Psi_{s1(max)} + \Psi_s(0)B + (C - \frac{A}{1-A}\Psi_s(0))(1 - B)$, where

$$C = -\frac{qN_D}{2C_s}t_i + \frac{\frac{qN_D}{2C_s}C_{ox1}(C_{ox2}t_i + 2\epsilon_{si}) + C_{ox1}C_{ox2}(\phi_{f2(poly)} - \phi_{f1(poly)})}{C_sC_{ox1} + C_sC_{ox2} + C_{ox1}C_{ox2}}.$$

Hence, an equation in terms of $\Psi_{s1(max)}$ has been obtained:

$$n_i e^{\frac{-\Psi_{s1(max)}}{kT/q}}(1 + e^{\frac{-D}{kT/q}}e^{\frac{(\frac{B-A}{1-A})\Psi_{s1(max)}}{kT/q}}) = N_D,$$

where $D = \Psi_s(0)B + (C - \frac{A}{1-A}\Psi_s(0))(1 - B)$. $\Psi_{s1(max)}$ has been approximated by substituting the $\Psi_{s1(max)}$ in the bracket in the above equation. Therefore, the short-channel effect threshold voltage model is:

$$\begin{aligned} V_{TH(S)} &= \frac{-\frac{qN_D}{2C_s}C_{ox2}t_i - \frac{qN_D}{C_s}\epsilon_{si} - C_{ox2}\phi_{f2(poly)} - (1 + \frac{C_{ox2}}{C_s})C_{ox1}\phi_{f1(poly)}}{C_{ox1} + C_{ox2} + C_{ox1}C_{ox2}C_s^{-1}} \\ &\quad + \frac{\Psi_{sm} - \Psi_s(0)A}{1 - A}, \\ \Psi_{sm} &= -\frac{kT}{q}(\ln\frac{N_D}{n_i} - \ln(1 + e^{\frac{-D}{kT/q}}e^{\frac{(\frac{B-A}{1-A})\Psi_{s1t}}{kT/q}})). \end{aligned} \tag{4.23}$$

Eq. (4.23) is an analytical short-channel effect threshold voltage model for double-gate short-channel SOI PMOS devices. Fig. 4.10 shows the threshold voltage versus the channel length of the double-gate fully-depleted SOI PMOS device using N^+ front and back poly gates, with a silicon thin-film of 1000Å, and a back thin-oxide thickness of 100Å, for front thin-oxide thicknesses of 50Å, 100Å, 150Å, and 200Å, based on the 2D simulation results and the analytical model results[13]. In the analytical model, $k_s = 0.4$. Fig. 4.11 shows the threshold voltage versus the channel

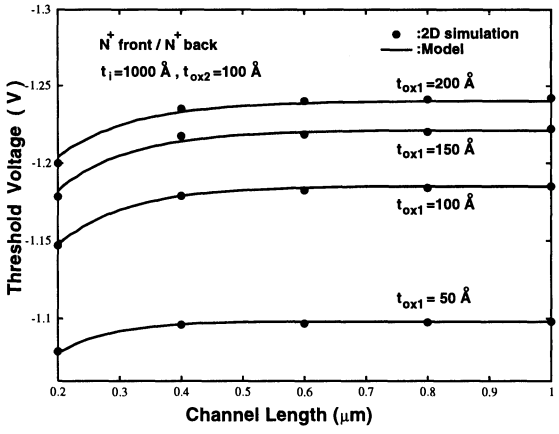


Figure 4.10: The threshold voltage versus the channel length of the double-gate fully-depleted SOI PMOS device using N^+ front and back poly gates, with a silicon thin-film of 1000Å, and a back thin-oxide thickness of 100Å, for front thin-oxide thicknesses of 50Å, 100Å, 150Å, and 200Å, based on the 2D simulation results and the analytical model results.

length of the double-gate fully-depleted SOI PMOS device using N^+ front and back poly gates, with a front and back thin-oxide thickness of 100Å, and silicon thin-film thicknesses of 400Å, 600Å, 800Å, 1000Å, based on the 2D simulation results and the analytical model results[13]. In the analytical model, $k_s = 0.4$ for $t_i = 1000$Å, $k_s = 0.48$ for $t_i = 800$Å, $k_s = 0.58$ for $t_i = 600$Å, $k_s = 0.615$ for $t_i = 400$Å. The deviation between the model and the 2D simulation results for the $t_i = 400$Å case is due to non-applicability of the fully-depleted approximation used in the analytical model. With a silicon thin-film of 400Å, holes above the field oxide can not be neglected. Compared to the long-channel threshold voltage formula, the shrinkage in the threshold voltage for the short-channel double-gate SOI PMOS device is: $\Delta V_{TH} = V_{TH(S)} - V_{TH(L)}$. Fig. 4.12 shows the shrinkage in threshold voltage versus the channel length of the double-gate fully-depleted SOI PMOS device using N^+ front and back poly gates, with a front and a back thin-oxide thicknesses of 100Å, and a silicon thin-film of 1000Å doped with donor densities of $10^{16}cm^{-3}$, $5 \times 10^{16}cm^{-3}$, and $10^{17}cm^{-3}$[13]. In the model derived in the previous section, k_s is dependent on the doping density and the thickness of the silicon thin-film. Here, $k_s = 0.92$ for $N_D = 10^{16}cm^{-3}$; $k_s = 0.69$ for $N_D = 5 \times 10^{16}cm^{-3}$; $k_s = 0.4$ for $N_D = 10^{17}cm^{-3}$. Also shown in the figure is the shrinkage in threshold voltage for

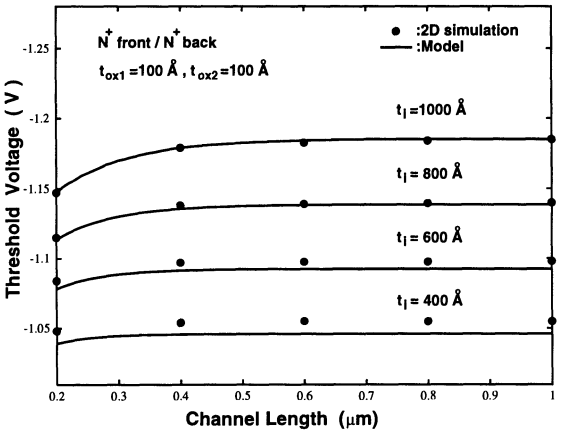


Figure 4.11: The threshold voltage versus the channel length of the double-gate fully-depleted SOI PMOS device using N^+ front and back poly gates, with a front and back thin-oxide thickness of 100Å, and silicon thin-film thicknesses of 400Å, 600Å, 800Å, 1000Å, based on the 2D simulation results and the analytical model results.

the single-gate SOI PMOS device, which has an identical structure except without the back poly gate. In the single-gate SOI PMOS device, the thickness of the buried oxide is 3500Å. For the single-gate SOI PMOS device, it's biased with a back gate bias of 0V. As shown in the figure, for both the single-gate and the double-gate cases, with a more heavily doped silicon thin-film, the threshold voltage is more sensitive to its channel length. Compared to the single-gate device, the double-gate device is less sensitive to its silicon thin-film doping density as a result of the better control of the channel by the front and the back gates.

Until now in this section, short channel effects have been analyzed. In fact, short channel effects are also influenced by the drain voltage. Fig. 4.13 shows the threshold voltage versus effective channel length of a fully-depleted SOI NMOS device with a front gate oxide of 92Å, a p-type silicon thin-film of 800Å doped with a density of $10^{17}cm^3$, and a buried oxide of 4000Å[19]. As shown in the figure, when V_D increases from 0.05V to 1V, the short channel effect becomes more serious. When the drain voltage increases, the potential distribution in the whole channel region is affected—the drain induced barrier lowering (DIBL) effect.

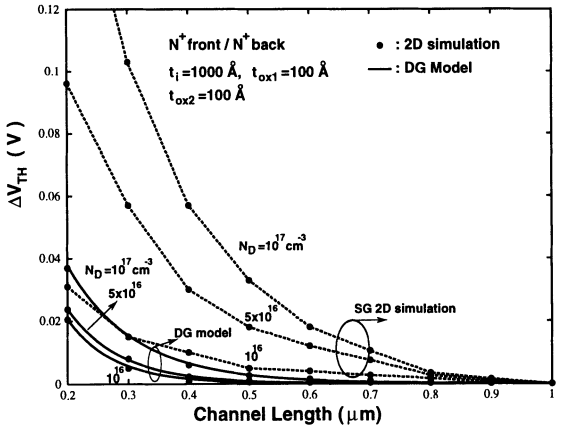


Figure 4.12: The shrinkage in threshold voltage versus the channel length of the double-gate fully-depleted SOI PMOS device using N^+ front and back poly gates, with a front and back thin-oxide thickness of 100Å, and a silicon thin-film of 1000Å doped with donor densities of $10^{16}cm^{-3}$, $5 \times 10^{16}cm^{-3}$, and $10^{17}cm^{-3}$. The single-gate SOI PMOS device has identical parameters except without the back poly gate. The thickness of the buried oxide in the single-gate SOI PMOS device is 3500Å.

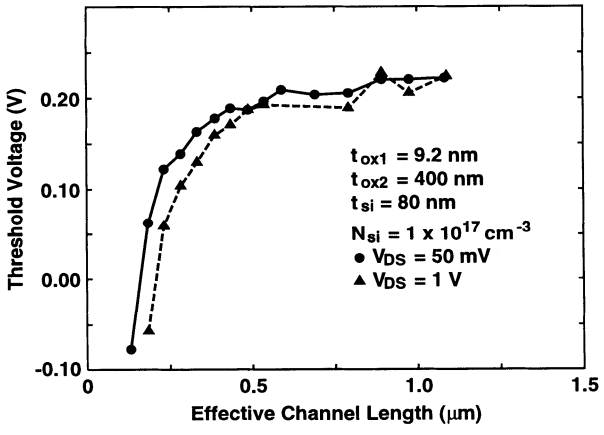


Figure 4.13: Threshold voltage versus effective channel length of a fully-depleted SOI NMOS device with a front gate oxide of 92Å, a p-type silicon thin-film of 800Å doped with a density of $10^{17}cm^{-3}$, and a buried oxide of 4000Å.

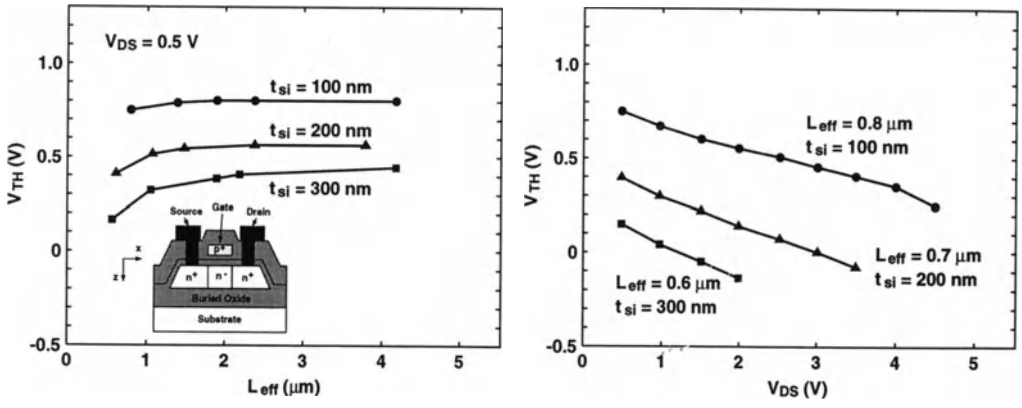


Figure 4.14: (a) Threshold voltage versus the effective channel length of an accumulation-mode SOI NMOS device with a front gate oxide of 550Å, a buried oxide of 4700Å,and an n-type silicon thin-film doped with a density of $1.5 \times 10^{15}\text{cm}^{-3}$, with various thin-film thicknesses. (b) Threshold voltage versus the drain voltage of the accumulation-mode SOI NMOS device with the parameters described in (a).

Until now in this section, the analysis of the short-channel effects of SOI MOS devices are for the inversion-mode fully-depleted devices. Here, the short-channel effects for the accumulation-mode SOI MOS devices are described. Fig. 4.14 shows (a) threshold voltage versus the effective channel length of an accumulation-mode SOI NMOS device with a front gate oxide of 550Å, a buried oxide of 4700Å,and an n-type silicon thin-film doped with a density of $1.5 \times 10^{15}\text{cm}^{-3}$, with various silicon thin-film thicknesses, and (b) threshold voltage versus the drain voltage of the accumulation-mode SOI NMOS device with the parameters described in (a)[20]. As shown in Fig. 4.14(a), the short channel effects of the accumulation-mode and inversion-mode devices are similar— a smaller effective channel length leads to a decrease in the threshold voltage. As shown in Fig. 4.14(b), as for the inversion-mode devices, when the drain voltage increases, the short channel effects become worse.

The short channel effect of an SOI MOS device is also dependent on the silicon thin-film thickness. Fig. 4.15 shows threshold voltage shift due to short channel effect versus the silicon thin-film thickness of an SOI NMOS device with a front gate oxide of 50Å, and a buried oxide of 3600Å, for various channel doping densities [21]. (a) $V_D = 0.05V$, (b) $V_D = 1.5V$. The threshold voltage shift is defined as the change in the threshold voltage for the device with a channel length of 0.1μm from the value

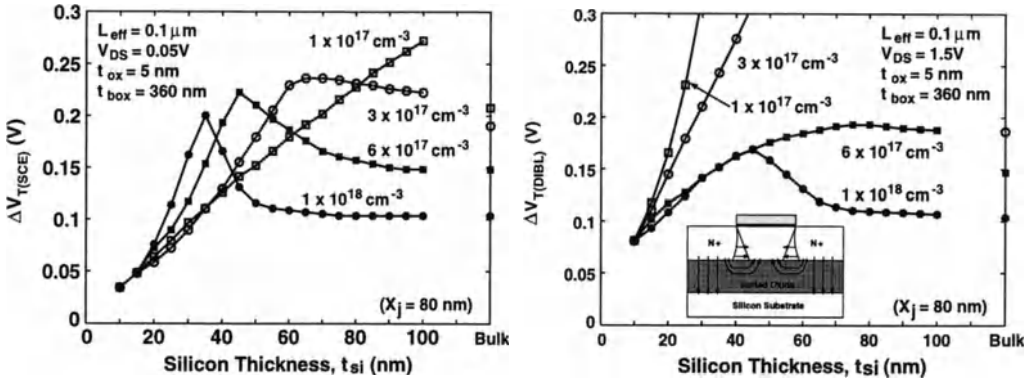


Figure 4.15: Threshold voltage shift due to short channel effect ($\delta V_{T(SCE)} = V_T(L_{eff} = 1\mu m) - V_T(L_{eff} = 0.1\mu m)$) versus the silicon thin-film thickness of the an SOI NMOS device with a front gate oxide of 50Å, and a buried oxide of 3600Å, for various channel doping densities. (a) $V_D = 0.05V$, (b) $V_D = 1.5V$.

at a channel length of 1μm ($\delta V_{T(SCE)} = V_T(L_{eff} = 1\mu m - V_T(L_{eff} = 0.1\mu m)$). As shown in Fig. 4.15(a), when the drain voltage is small, the threshold voltage shift becomes smaller when the silicon thin-film thickness decreases. In addition, a decrease in the doping density of the silicon thin-film leads to a smaller threshold voltage shift. This trend is true when the silicon thin-film thickness is small—full-depleted devices. When the silicon thin-film thickness is not small—partially-depleted devices, the threshold voltage shift is not sensitive to the silicon thin-film thickness. On the contrary, for the partially-depleted devices, an increase in the silicon thin-film doping density leads to an increase in the threshold voltage shift. Generally speaking, the magnitude of the threshold voltage shift in the partially-depleted SOI MOS devices is similar to that in the bulk MOS devices. The threshold voltage shifts in both the partially-depleted SOI and bulk MOS devices are larger than those in the fully-depleted SOI MOS devices. As shown in the figure, at the boundary between the partially-depleted and the fully-depleted SOI devices, there are peaks in the threshold voltage shift curves. At the boundary, the channel region in the SOI MOS devices is especially susceptible to the influence from the source and the drain regions via the buried oxide as shown in the figure. When the drain voltage is large as shown in Fig. 4.15(b), it has a similar trend as for the case in Fig. 4.15(a). As shown in Fig. 4.15(b), for both fully-depleted and partially-depleted devices, only when the silicon thin-film doping density is high, the DIBL effect can be effectively suppressed to decrease the threshold voltage shift. From Fig. 4.15(a)&(b), in order

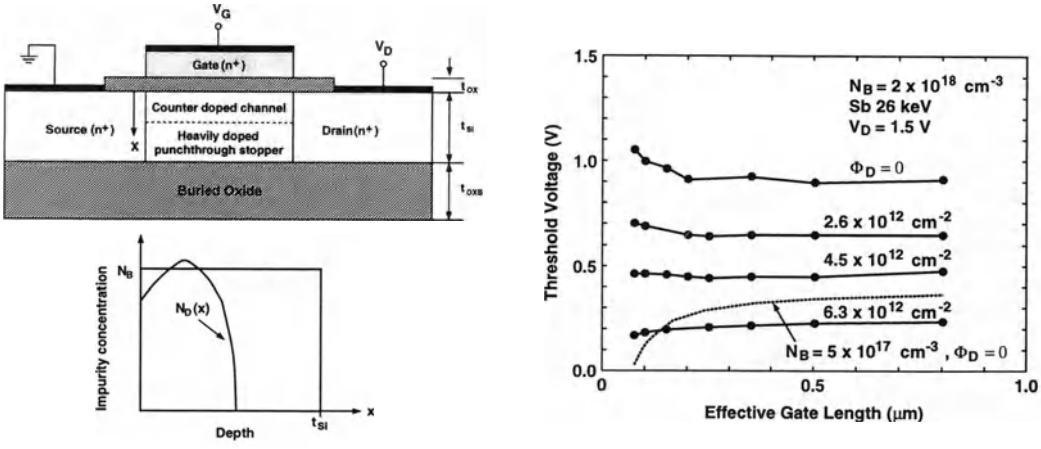


Figure 4.16: Short channel effect of a partially-depleted SOI NMOS device with a non-uniform doping profile in the silicon thin-film—heavily-doped p^+ region at the bottom of the silicon thin-film above the buried oxide and a counter-doped n-type channel region. The front oxide is 40Å thick. The silicon thin-film thickness is 1000Å.

to reduce the short channel effect, the silicon thin-film of the fully-depleted devices should be as thin as possible. In contrast, in order to reduce the short channel effect, the doping density of the silicon thin-film in the partially-depleted devices should be as high as possible. In addition, the device should be designed to avoid the partially-depleted/fully-depleted boundary region.

Although by raising the silicon thin-film doping density, the short channel effect of a partially-depleted SOI MOS device can be reduced, a high doping density in the silicon thin-film may lead to a high threshold voltage, which may not be appropriate for low-voltage operation. In addition, impurity scattering due to the heavy doping in the silicon thin-film may degrade the carrier mobility. Fig. 4.16 shows the short channel effect of a partially-depleted SOI NMOS device with a non-uniform doping profile in the silicon thin-film— heavily-doped p^+ region at the bottom of the silicon thin-film above the buried oxide and a counter-doped n-type channel region[22]. As shown in the figure, with the counter doped approach, its threshold voltage can be adjusted to an appropriate value. In addition, the DIBL effect can be controlled. In contrast, as shown in dashed lines in the figure, with the uniform doping method, in order to have an appropriate threshold voltage, the silicon thin-film doping density

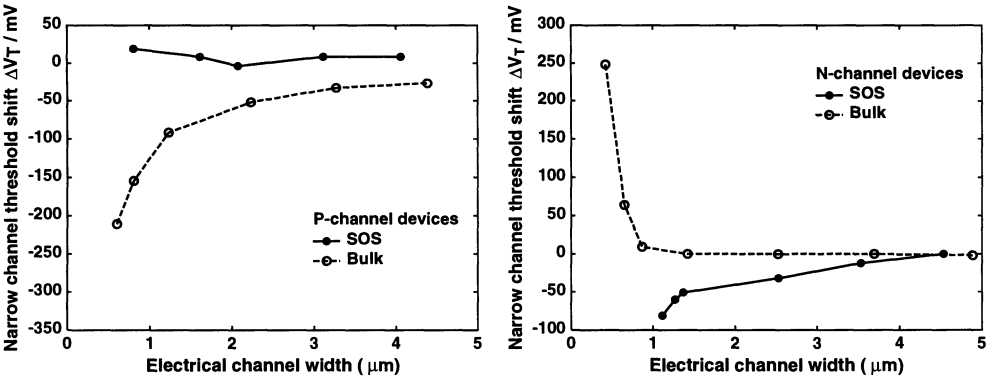


Figure 4.17: Threshold voltage shift versus channel width of SOI PMOS and NMOS devices using mesa isolation with a gate oxide thickness of 300Å.

cannot be too high. Otherwise, the DIBL can be serious. With the non-uniform doping technique, the threshold voltage of a partially-depleted SOI MOS device can be effectively designed.

4.3 Narrow-Channel Effect

For small-geometry SOI CMOS devices, in addition to short-channel effect, narrow-channel effect is also important [18][13][23]-[25]. Compared to short-channel effect, narrow-channel effect of small-geometry SOI CMOS devices is more complicated because of isolation technology. Mesa isolation technology offers advantages of high integration densities [18][23][26][27] for small-geometry SOI CMOS devices. However, narrow-channel effects of ultrathin SOI CMOS devices using mesa isolation are quite different from those of LOCOS-isolated bulk CMOS devices [18][23][28]-[30]. As shown in Fig. 4.17[23], the narrow channel effect on the threshold voltage of SOI CMOS devices using mesa isolation is contrary to that of bulk ones. For bulk NMOS devices using the LOCOS structure, due to the bird's beak of the field oxide and the channel stop implant under the field oxide, when the channel width is scaled down, the magnitude of the threshold voltage increases[28]-[30]. For SOI inversion-mode NMOS devices, the situation is reverse. Due to the 2D effect around the sidewall of the mesa isolation structure, when the channel width is shrunk, the magnitude of the threshold voltage also decreases. A threshold voltage model considering narrow-channel effect is important for providing insights into the device design of an SOI CMOS device. In this section, an analytical threshold voltage formula considering

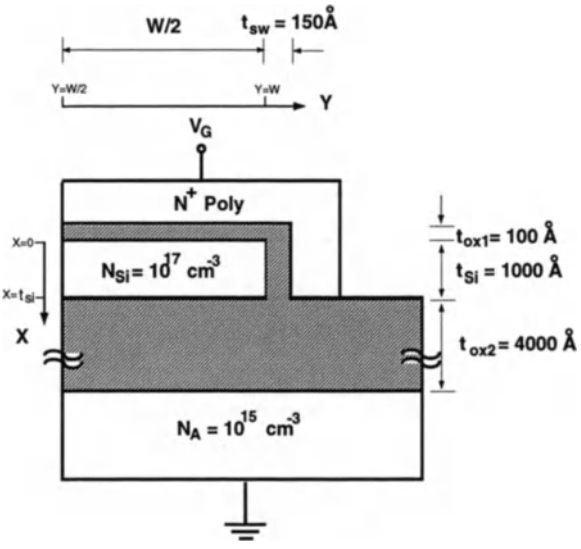


Figure 4.18: Mesa-isolated inversion-mode fully-depleted SOI NMOS device.

the sidewall-related narrow-channel effect for VLSI mesa-isolated fully-depleted ultrathin SOI NMOS devices is described.

Due to the buried oxide structure, device isolation in the SOI CMOS technology is much easier than that in the bulk CMOS technology. In the mesa-isolated SOI MOS device structure as shown in Fig.4.18 [31][32], the isolation between devices can be accomplished by etching off the silicon thin-film between the active region. Due to the mesa-isolated structure, the narrow channel effect of the SOI MOS device is different from that of the bulk MOS device.

As shown in Fig. 4.18, this mesa-isolated SOI NMOS device has an N^+ polysilicon gate. The doping density of the 1000Å p-type silicon thin-film is $10^{17}cm^{-3}$. The buried oxide is 4000Å. The front oxide is 100Å. Due to the mesa-isolated structure, to the right end of the silicon thin-film, there is an oxide sidewall of 150Å. Due to the symmetry, only half of the device is shown.

Consider the mesa-isolated fully-depleted inversion-mode SOI NMOS device as shown in Fig.4.18. When the channel width is small, the 1D analysis for the wide

channel case is not applicable. Instead, 2D Poisson's equation is required:

$$\frac{\partial^2\Psi}{\partial x^2}+\frac{\partial^2\Psi}{\partial y^2}=\frac{qN_{si}}{\epsilon_{si}}, \tag{4.24}$$

where N_{si} is the doping density of the silicon thin-film. Usually, the thickness of the silicon thin-film is much smaller than the channel width ($t_{si} << W$), therefore, the change in $\frac{d^2\Psi}{dy^2}$ in the lateral direction is much larger than that in the vertical direction. Hence, $\frac{d^2\Psi}{dy^2}$ is mainly related to the lateral direction:

$$\begin{aligned}\frac{\partial^2\Psi}{\partial y^2} &= \frac{qN_{si}k(y)}{\epsilon_{si}},\\ \frac{\partial^2\Psi}{\partial x^2} &= \frac{qN_{si}(1-k(y))}{\epsilon_{si}},\end{aligned} \tag{4.25}$$

where $k(y)$ is a function y. The boundary conditions for the above differential equations are that at the silicon thin-film surface under the front gate and at the bottom of the silicon thin-film above the buried oxide:

$$\begin{aligned}\Psi(0,y) &= \Psi_G+\frac{\partial\Psi}{\partial x}|_{0,y}\cdot\frac{\epsilon_{si}}{\epsilon_{ox}}t_{ox1},\\ \Psi(t_{si},y) &= \Psi_{s3}-\frac{\partial\Psi}{\partial x}|_{t_{si},y}\cdot\frac{\epsilon_{si}}{\epsilon_{ox}}t_{ox2},\end{aligned} \tag{4.26}$$

where Ψ_G is the electrostatic potential of the gate electrode, Ψ_{s3} is the substrate surface potential obtained from the previous section; t_{ox1} and t_{ox2} are thicknesses of the front and buried oxides, respectively. Solving the differential equations with these boundary conditions, the potential in the silicon thin-film is:

$$\Psi(x,y)=\frac{qN_{si}t_{si}^2}{2\epsilon_{si}}(1-k(y))\frac{x^2}{t_{si}^2}+\frac{\Psi_{s3}-\Psi_G-\frac{qN_{si}t_{si}^2}{2\epsilon_{si}}(1-k(y))(1+2\frac{C_{si}}{C_{ox2}})}{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}}(\frac{x}{t_{si}}+\frac{C_{si}}{C_{ox1}})+\Psi_G, \tag{4.27}$$

where $C_{ox1}=\frac{\epsilon_{ox}}{t_{ox1}}$, $C_{ox2}=\frac{\epsilon_{ox}}{t_{ox2}}$, $C_{si}=\frac{\epsilon_{si}}{t_{si}}$, and t_{si} is the silicon thin-film thickness. From the above equation, at a depth in the silicon thin-film ($x=\gamma t_{si}$, $0<\gamma<1$), k(y) is: $k(y)=1-\frac{2\epsilon_{si}}{qN_{si}t_{si}^2}\frac{(1-\gamma+\frac{C_{si}}{C_{ox2}})\Psi_G+(\gamma+\frac{C_{si}}{C_{ox1}})\Psi_{s3}-(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})\Psi(\gamma t_{si},y)}{(\gamma-\gamma^2)+(1-\gamma^2)\frac{C_{si}}{C_{ox1}}+(2\gamma-\gamma^2)\frac{C_{si}}{C_{ox2}}+2\frac{C_{si}}{C_{ox1}}\frac{C_{si}}{C_{ox2}}}$, where γ is used to measure the mean interaction point between the lateral direction and the vertical direction. From Eq. (4.25), the lateral direction differential equation at a depth ($x=\gamma t_{si}$) in the silicon thin-film is:

$$\frac{\partial^2\Psi(\gamma t_{si},y)}{\partial y^2} = \frac{\Psi(\gamma t_{si},y)}{l_1^2}+c_1, \tag{4.28}$$

where $l_1 = t_{si}\sqrt{\frac{(\gamma-\gamma^2)+(1-\gamma^2)\frac{C_{si}}{C_{ox1}}+(2\gamma-\gamma^2)\frac{C_{si}}{C_{ox2}}+2\frac{C_{si}}{C_{ox1}}\frac{C_{si}}{C_{ox2}}}{2(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})}}$, and

$$c_1 = \frac{qN_{si}}{\epsilon_{si}} - \frac{1}{l_1^2}\frac{(1-\gamma+\frac{C_{si}}{C_{ox2}})\Psi_G + (\gamma+\frac{C_{si}}{C_{ox1}})\Psi_{s3}}{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}}.$$

The boundary conditions for the above differential equation are that (1) in the center of the channel, the lateral electric field is zero and (2) at sidewall, the electrostatic potential is related to Ψ_G:

$$\frac{\partial\Psi(\gamma t_{si},y)}{\partial y}|_{y=W/2} = 0, \tag{4.29}$$

$$\Psi(\gamma t_{si},W) = \Psi_G - \frac{\partial\Psi(\gamma t_{si},y)}{\partial y}|_{y=W}.\frac{\epsilon_{si}}{\epsilon_{ox}}t_{sw},$$

where t_{sw} is the sidewall thickness. From the above equations, the electrostatic potential distribution at $x = \gamma t_{si}$ is:

$$\Psi(\gamma t_{si},y) = -c_1 l_1^2 + 2cosh((y-\frac{W}{2})/l_1).\alpha_1.(\Psi_G + c_1 l_1^2), \tag{4.30}$$

where $\alpha_1 = \frac{1}{(1-\frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_1})e^{-W/2l_1}+(1+\frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_1})e^{W/2l_1}}$, $C_{sw} = \frac{\epsilon_{ox}}{t_{sw}}$. From Eq.(4.27), in the center of the channel at the silicon thin-film surface under the gate, the electrostatic potential is:

$$\Psi(0,\frac{W}{2}) = \frac{C_{si}}{C_{ox1}}\frac{\Psi_{s3}-\Psi_G-\frac{qN_{si}t_{si}^2}{2\epsilon_{si}}(1-k(\frac{W}{2}))(1+2\frac{C_{si}}{C_{ox2}})}{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}} + \Psi_G, \tag{4.31}$$

where $k(\frac{W}{2}) = 1 - \frac{2\epsilon_{si}}{qN_{si}t_{si}^2}\frac{(1-\gamma+\frac{C_{si}}{C_{ox2}})\Psi_G+(\gamma+\frac{C_{si}}{C_{ox1}})\Psi_{s3}-(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})\Psi(\gamma t_{si},\frac{W}{2})}{(\gamma-\gamma^2)+(1-\gamma^2)\frac{C_{si}}{C_{ox1}}+(2\gamma-\gamma^2)\frac{C_{si}}{C_{ox2}}+2\frac{C_{si}}{C_{ox1}}\frac{C_{si}}{C_{ox2}}}$. When the device is biased at the threshold voltage, the electrostatic potential in the center of the channel at the silicon thin-film surface under the front gate is: where $\Psi(0,\frac{W}{2}) = -\phi_{si}$, and $\phi_{si} = \frac{kT}{q}ln\frac{n_i}{n_{si}}$. From Eqs.(4.30)(4.31), the narrow-channel effect threshold voltage formula is:

$$V_{TH} = V_{FB} + \Psi_G - \phi_{si}, \tag{4.32}$$

$$\Psi_G = \frac{-\phi_{si}(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}) - \Psi_{s3}\frac{C_{si}}{C_{ox1}}(1-\alpha_1') + \frac{qN_{si}t_{si}^2}{2\epsilon_{si}}\frac{C_{si}}{C_{ox1}}(1+2\frac{C_{si}}{C_{ox2}})(1-2\alpha_1)}{1+\alpha_1'\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}},$$

where $\alpha_1' = \alpha_1 \cdot \frac{t_{si}^2}{l_1^2}\frac{(\gamma+\frac{C_{si}}{C_{ox1}})(1+2\frac{C_{si}}{C_{ox2}})}{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}}$, and V_{FB} is the flat-band voltage of the front gate. Comparing Eq. (4.32) with the threshold voltage formula for the wide channel

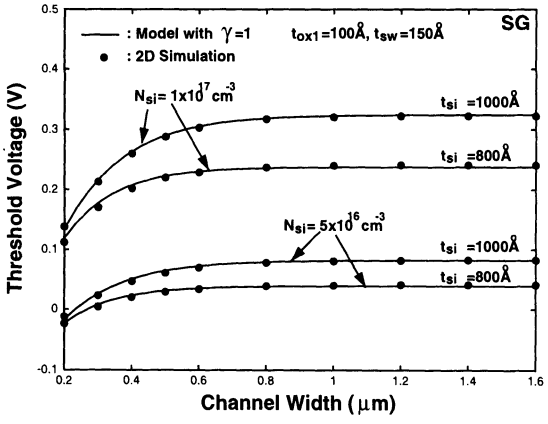


Figure 4.19: Threshold voltage versus channel width of the mesa-isolated SOI NMOS device with a front gate oxide of 100Å and a sidewall oxide of 150Å and silicon thin-films of 800Å and 1000Å, with acceptor densities of $10^{17}cm^{-3}$ and $5 \times 10^{16}cm^{-3}$.

case, the narrow channel effect is reflected on α_1 and α_1'. When the channel is wide, α_1 and α_1' are close to 0. From Eq. (4.32), as shown in Fig. 4.19, when the silicon thin-film is thinner and the doping density of the silicon thin-film is lighter, the narrow channel effect is smaller[33].

The analytical threshold voltage formula considering the narrow-channel effect is valid not just for single-gate SOI MOS devices but also for double-gate SOI MOS devices[11][35][24]. For the double-gate fully-depleted ultrathin SOI NMOS device as shown in Fig. 4.20[33], the differential equation Eq. (4.25) is still applicable but its boundary conditions are different:

$$\begin{aligned} \Psi(0,y) &= \Psi_G + \frac{\partial \Psi}{\partial y}|_{0,y} \cdot \frac{\epsilon_{si}}{\epsilon_{ox}} t_{ox}, \\ \Psi(t_{si},y) &= \Psi_G - \frac{\partial \Psi}{\partial y}|_{t_{si},y} \cdot \frac{\epsilon_{si}}{\epsilon_{ox}} t_{ox}, \end{aligned} \tag{4.33}$$

where the bottom boundary condition has been replaced. Solving Eq. (4.25) using Eq. (4.33), the electrostatic potential in the vertical direction is

$$\Psi(x,y) = \frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}}[1-k(y)](\frac{x^2}{{t_{si}}^2} - \frac{x}{t_{si}} - \frac{C_{si}}{C_{ox}}) + \Psi_G. \tag{4.34}$$

Compared to Eq. (4.27), Eq. (4.34) is much simpler due to the symmetry in the

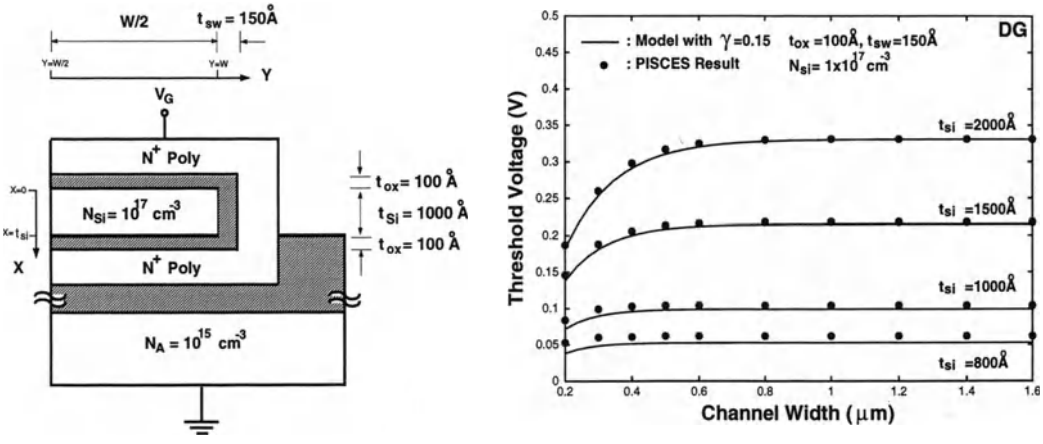


Figure 4.20: Cross section and threshold voltage versus channel width of the double polysilicon gate SOI CMOS device with a gate oxide of 100Å, a sidewall oxide of 150Å, and an acceptor density of $10^{17}cm^{-3}$ in the silicon thin-films of 800Å, 1000Å, 1500Å and 2000Å.

vertical structure for the double-gate SOI MOS device. Similarly, considering the lateral direction at a location ($x = \gamma t_{si}$, $0 \leq \gamma \leq 0.5$) in the silicon thin-film, from Eq. (4.34), one obtains $k(y) = 1 - \frac{2\epsilon_{si}}{qN_{si}{t_{si}}^2} \frac{\Psi_G - \Psi(\gamma t_{si}, y)}{\gamma - \gamma^2 + \frac{C_{si}}{C_{ox}}}$. From Eq. (4.25), the differential equation becomes

$$\frac{\partial^2 \Psi(\gamma t_{si}, y)}{\partial y^2} = \frac{\Psi(\gamma t_{si}, y)}{{l_2}^2} + c_2, \tag{4.35}$$

where $l_2 = t_{si}\sqrt{\frac{1}{2}(\gamma - \gamma^2 + \frac{C_{si}}{C_{ox}})}$, and $c_2 = \frac{qN_{si}}{\epsilon_{si}} - \frac{\Psi_G}{{l_2}^2}$. The boundary conditions for the lateral differential equation (Eq. (4.35)) are identical to Eq. (4.29). Solving Eq. (4.35), the lateral electrostatic potential distribution is

$$\Psi(\gamma t_{si}, y) = -c_2{l_2}^2 + 2\cosh[(y - \frac{W}{2})/l_2] \cdot \alpha_2 \cdot (\Psi_G + c_2{l_2}^2), \tag{4.36}$$

where $\alpha_2 = \frac{1}{(1 - \frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_2})e^{-W/2l_2} + (1 + \frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_2})e^{W/2l_2}}$. From Eq. (4.34), the vertical electrostatic potential, the surface electrostatic potential at the center of the channel is

$$\Psi(0, \frac{W}{2}) = \Psi_G - \frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}} \frac{C_{si}}{C_{ox}}[1 - k(\frac{W}{2})], \tag{4.37}$$

where $k(\frac{W}{2}) = 1 - \frac{2\epsilon_{si}}{qN_{si}{t_{si}}^2} \frac{\Psi_G - \Psi(\gamma t_{si}, \frac{W}{2})}{\gamma - \gamma^2 + \frac{C_{si}}{C_{ox}}}$. By defining that at the threshold voltage the surface electrostatic potential at the center of the channel is $\Psi(0, \frac{W}{2}) = -\phi_{si}$. using Eqs. (4.36)&(4.37), the threshold voltage is

$$\begin{aligned} V_{TH} &= V_{FB} + \Psi_G - \phi_{si} = V_{FB} - 2\phi_{si} + \frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}} \frac{C_{si}}{C_{ox}}(1 - 2\alpha_2), \\ \Psi_G &= -\phi_{si} + \frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}} \frac{C_{si}}{C_{ox}}(1 - 2\alpha_2). \end{aligned} \tag{4.38}$$

Eq. (4.38) is the analytical threshold voltage formula considering the narrow-channel effect for double-gate SOI NMOS devices. Fig. 4.20 shows the threshold voltage versus channel width of the double polysilicon gate fully-depleted ultrathin SOI NMOS device with a gate oxide of 100Å, a sidewall oxide of 150Å, and an acceptor density of $1 \times 10^{17}\text{cm}^{-3}$ in the silicon thin-films of 800Å, 1000Å, 1500Å and 2000Å, based on the analytical formula and the 2D simulation results[33]. The analytical formula results shown in this figure are for $\gamma = 0.15$. Considering the symmetry in the vertical structure of the double-gate SOI NMOS device, the smaller γ indicates a much better narrow-channel threshold voltage behavior as compared to the single-gate one. Compared to the interaction point in Fig. 4.19, $\gamma = 0.15$ in Fig. 4.20 is much smaller — the interaction point between the lateral direction and the vertical direction is inside the silicon thin-film as a result of the double-gate structure instead of a buried-oxide structure.

In this section until now, the narrow channel effect of mesa-isolated SOI MOS devices is different from that of the bulk MOS devices using field oxide. Due to the channel stop implant under the field oxide, when the channel width is small, the narrow channel effect increases the magnitude of the threshold voltage of a bulk device. However, in the mesa-isolated inversion-mode SOI NMOS device, narrow-channel effect shrinks the threshold voltage. This is one of the basic differences between SOI and bulk MOS devices. On the other hand, for the accumulation-mode SOI NMOS devices, the narrow-channel effect on the threshold voltage is similar to that for the bulk devices.

Fig. 4.21 shows the threshold voltage variations versus channel width of a mesa-isolated SOI PMOS device: (a) with a buried oxide of 4000Å, a silicon thin-film doping density of 10^{17}cm^{-3} at various silicon thin-film thicknesses of 1000Å, 800Å and 500Å; (b) with a silicon thin-film thickness of 1000Å, a silicon thin-film doping density of 10^{17}cm^{-3} and various buried-oxide thicknesses of 4000Å, 2000Å, and 1000Å [34]. As shown in the figure, when the channel width is reduced, the magnitude of the threshold voltage of the inversion-mode SOI PMOS device becomes

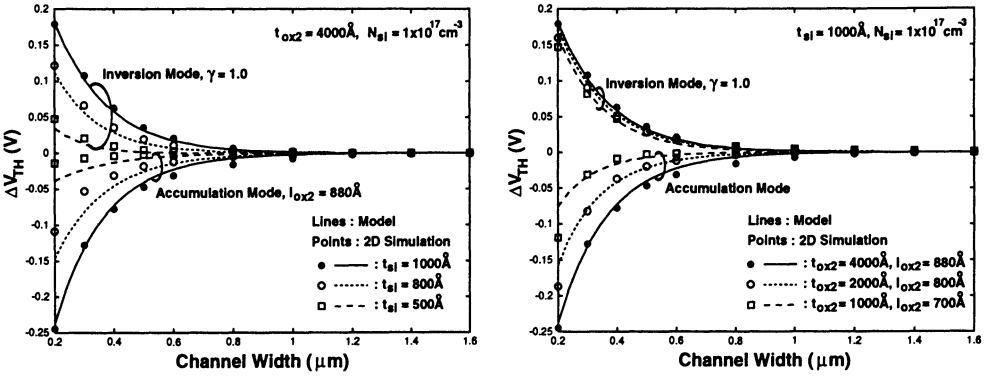


Figure 4.21: Threshold voltage variations versus channel width of a mesa-isolated SOI PMOS device: (a) with a buried oxide of 4000Å, a silicon thin-film doping density of $10^{17}cm^{-3}$ at various silicon thin-film thickness of 1000Å, 800Å and 500Å; (b)with a silicon thin-film thickness of 1000Å, a silicon thin-film doping density of $10^{17}cm^{-3}$ and various buried-oxide thicknesses of 4000Å, 2000Å, and 1000Å.

smaller but that of the accumulation-mode SOI PMOS device becomes larger. As indicated in the figure, with a thinner silicon thin-film, the narrow-channel effect is less. With a thicker buried oxide, the narrow-channel effect is more serious for the accumulation-mode SOI PMOS device. In contrast, for the inversion-mode SOI PMOS device, the narrow-channel effect is not sensitive to the thickness of the buried oxide. The larger sensitivity of the narrow-channel effect for the accumulation-mode SOI PMOS device is because of the buried-channel structure and its influence from the buried oxide.

4.4 Three-Dimensional effect

In the previous setions, short and narrow channel effects have been individually considered for small-geometry SOI CMOS devices. However, they are not considered at the same time. Due to the progress in the SOI CMOS processing technology, both the channel length and the channel width of a deep-submicron SOI CMOS device are scaled down simultaneously [36]-[38]. Therefore, short and narrow channel effects occur at the same time[37][39]. As a result, the analytical short-channel and narrow-channel effects models based on the 2D analysis are not sufficient for

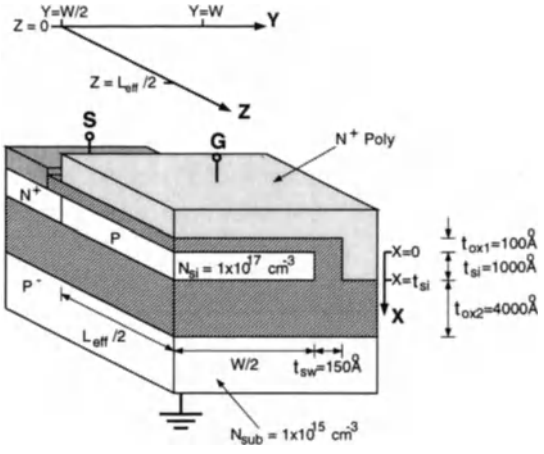


Figure 4.22: Cross section of a small-geometry mesa-isolated ultrathin SOI NMOS device under study.

accurate modeling of the small-geometry effects. In order to analyze the behavior of a small-geometry SOI CMOS device, the 3D geometrical effects should also be included in the analytical model. The 3D geometrical effects of bulk and SOI CMOS devices have been analyzed [40][45][46]. In this section, 3D geometrical effects models of the SOI CMOS are organized.

Fig.4.22 shows the cross section of a small-geometry mesa-isolated ultrathin SOI NMOS device under study[45]. This device has an N^+ polysilicon gate, a front oxide of 100Å, a sidewall oxide of 150Å, a buried oxide of 4000Å, and a p-type silicon thin-film of 1000Å. The doping density of the silicon thin-film and the p-type substrate is $1 \times 10^{17}\text{cm}^{-3}$ and $1 \times 10^{15}\text{cm}^{-3}$, respectively. Fig. 4.22 shows one quarter of the device under study. As shown in the figure, L_{eff} and W represent the channel length and the channel width, respectively. The x-axis is in the substrate direction. The y-axis is in the channel width direction. The z-axis is in the channel length direction. The threshold voltage of this device is defined as the gate voltage when the front surface of the silicon thin-film in the center of the device with a minimum potential ($x = 0$, $y = L_{eff}/2$, $z = W/2$) reaches strong inversion. Consider the SOI NMOS device as shown in Fig. 4.22, the analytical threshold voltage model based on 1D analysis is not applicable. Under this situation, 3D Poisson's equation should

be considered:

$$\frac{\partial^2\Psi}{\partial x^2}+\frac{\partial^2\Psi}{\partial y^2}+\frac{\partial^2\Psi}{\partial z^2}=\frac{qN_{si}}{\epsilon_{si}}, \tag{4.39}$$

where x is in the substrate direction, y is in the channel width direction, z is in the channel length direction, and N_{si} is the doping density of the silicon thin-film. Since, for ultrathin SOI NMOS devices, usually, the thickness of the silicon thin-film (t_{si}) is much smaller than the channel length (L_{eff}) and the channel width (W), therefore, in the silicon thin-film, the change in $\frac{\partial^2\Psi}{\partial x^2}$, $\frac{\partial^2\Psi}{\partial y^2}$, and $\frac{\partial^2\Psi}{\partial z^2}$ in the x-direction can be neglected. Hence, Eq. (4.39) can be simplified as:

$$\frac{\partial^2\Psi}{\partial y^2}+\frac{\partial^2\Psi}{\partial z^2} = \frac{qN_{si}k(y,z)}{\epsilon_{si}}, \tag{4.40}$$

$$\frac{\partial^2\Psi}{\partial x^2} = \frac{qN_{si}[1-k(y,z)]}{\epsilon_{si}}, \tag{4.41}$$

where $k(y,z)$ is a function independent of x. Considering Eq. (4.40), its boundary conditions are that at the front oxide/silicon thin-film interface and at the buried oxide/silicon thin-film interface the electrostatic potentials are similar to Eq. (4.26): $\Psi(0,y,z)=\Psi_G+\frac{\partial\Psi(x,y,z)}{\partial x}|_{x=0}\cdot\frac{\epsilon_{si}}{\epsilon_{ox}}t_{ox1}$, $\Psi(t_{si},y,z)=\Psi_{s3}-\frac{\partial\Psi(x,y,z)}{\partial x}|_{x=t_{si}}\cdot\frac{\epsilon_{si}}{\epsilon_{ox}}t_{ox2}$. From Eq. (4.40), one obtains the electrostatic potential:

$$\Psi(x,y,z) = \frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}}[1-k(y,z)]\frac{x^2}{{t_{si}}^2}+ \tag{4.42}$$
$$\frac{\Psi_{s3}-\Psi_G-\frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}}[1-k(y,z)](1+2\frac{C_{si}}{C_{ox2}})}{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}}(\frac{x}{t_{si}}+\frac{C_{si}}{C_{ox1}})+\Psi_G.$$

In the middle of the silicon thin-film ($x=t_{si}/2$), the electrostatic potential is $\Psi(t_{si}/2,y,z)$. Therefore, $k(y,z)$ becomes:

$$k(y,z)=1-\frac{2\epsilon_{si}}{qN_{si}{t_{si}}^2}\frac{(\frac{1}{2}+\frac{C_{si}}{C_{ox2}})\Psi_G+(\frac{1}{2}+\frac{C_{si}}{C_{ox1}})\Psi_{s3}-(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})\Psi(\frac{t_{si}}{2},y,z)}{\frac{1}{4}+\frac{3}{4}\frac{C_{si}}{C_{ox1}}+\frac{3}{4}\frac{C_{si}}{C_{ox2}}+2\frac{C_{si}}{C_{ox1}}\frac{C_{si}}{C_{ox2}}}.$$

From Eq. (4.40), in the middle of the silicon thin-film ($x=t_{si}/2$), one obtains:

$$\frac{\partial^2\Psi(\frac{t_{si}}{2},y,z)}{\partial y^2}+\frac{\partial^2\Psi(\frac{t_{si}}{2},y,z)}{\partial z^2}=\frac{\Psi(\frac{t_{si}}{2},y,z)}{{l_0}^2}+c_0, \tag{4.43}$$

where $l_0=t_{si}\sqrt{\frac{\frac{1}{4}+\frac{3}{4}\frac{C_{si}}{C_{ox1}}+\frac{3}{4}\frac{C_{si}}{C_{ox2}}+2\frac{C_{si}}{C_{ox1}}\frac{C_{si}}{C_{ox2}}}{2(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})}}$, and $c_0=\frac{qN_{si}}{\epsilon_{si}}-\frac{1}{{l_0}^2}\frac{(\frac{1}{2}+\frac{C_{si}}{C_{ox2}})\Psi_G+(\frac{1}{2}+\frac{C_{si}}{C_{ox1}})\Psi_{s3}}{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}}$.
In the middle of the channel length ($z=L_{eff}/2$), at a location near the sidewall, the

influence of the sidewall oxide is larger than that of the source/drain. Therefore, at a location closer to the sidewall, the value of its $\frac{\partial^2\Psi(\frac{t_{si}}{2},y,z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}}$ becomes smaller. Owing to the symmetry of the device with respect to $y=\frac{W}{2}$, one can assumes that $\frac{\partial^2\Psi(\frac{t_{si}}{2},y,z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}} \cong \frac{\partial^2\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}} \cdot (1-(\frac{2y}{W}-1)^2)$. Consequently, from Eq. (4.43), one obtains:

$$\begin{aligned}\frac{\partial^2\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{\partial y^2} &= \frac{\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{{l_0}^2}+c_0-\frac{\partial^2\Psi(\frac{t_{si}}{2},y,z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}}, \\ &\simeq \frac{\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{{l_0}^2}+c_0-\frac{\partial^2\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}}\cdot[1-(\frac{2y}{W}-1)^2].\end{aligned} \tag{4.44}$$

The boundary conditions in the channel width direction (y direction) for Eq. (4.44) are (1) in the center of the channel, the electric field in the channel width direction is zero, (2) at the sidewall, the electrostatic potential is related to Ψ_G: $\frac{\partial\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{\partial y}|_{y=\frac{W}{2}}=0$, and $\Psi(\frac{t_{si}}{2},W,\frac{L_{eff}}{2})=\Psi_G-\frac{\partial\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{\partial y}|_{y=W}\cdot\frac{\epsilon_{si}}{\epsilon_{ox}}t_{sw}$, where t_{sw} is the thickness of the sidewall oxide. Solving Eq. (4.44) with boundary conditions, the distribution of the electrostatic potential in the channel width direction (y direction) at $x=t_{si}/2$, $z=L_{eff}/2$ is:

$$\begin{aligned}\Psi\ (\ \frac{t_{si}}{2},y,\frac{L_{eff}}{2}) &= -c_0{l_0}^2+\frac{\partial^2\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}}\cdot{l_0}^2\cdot[1-\frac{8{l_0}^2}{W^2}-(\frac{2y}{W}-1)^2] \\ &+cosh[(y-\frac{W}{2})/l_0]\cdot\alpha\cdot[\Psi_G+c_0{l_0}^2+\frac{\partial^2\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}}\cdot{l_0}^2\cdot(\frac{8{l_0}^2}{W^2}+\frac{4t_{si}}{W}\frac{C_{si}}{C_{sw}})],\end{aligned} \tag{4.45}$$

where $\alpha=\frac{1}{cosh(W/2l_0)+\frac{t_{si}}{l_0}\frac{C_{si}}{C_{sw}}sinh(W/2l_0)}$, and $C_{sw}=\frac{\epsilon_{ox}}{t_{sw}}$. From Eq. (4.45), one obtains:

$$\frac{\partial^2\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{\partial y^2}|_{y=\frac{W}{2}} = \frac{\alpha}{{l_0}^2}\cdot(\Psi_G+c_0{l_0}^2)-\alpha'\cdot\frac{\partial^2\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}}, \tag{4.46}$$

where $\alpha'=(1-\alpha)\cdot\frac{8{l_0}^2}{W^2}-\alpha\cdot\frac{4t_{si}}{W}\frac{C_{si}}{C_{sw}}$. Similarly, from Eq. (4.43), in the middle of the channel width ($y=W/2$), assuming that $\frac{\partial^2\Psi(t_{si}/2,y,z)}{\partial y^2}|_{y=W/2}\simeq\frac{\partial^2\Psi(t_{si}/2,y,L_{eff}/2)}{\partial y^2}|_{y=W/2}(1-(\frac{2z}{L_{eff}}-1)^2)$, one obtains:

$$\begin{aligned}\frac{\partial^2\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{\partial z^2} &= \frac{\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{{l_0}^2}+c_0-\frac{\partial^2\Psi(\frac{t_{si}}{2},y,z)}{\partial y^2}|_{y=\frac{W}{2}}, \\ &\simeq \frac{\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{{l_0}^2}+c_0-\frac{\partial^2\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{\partial y^2}|_{y=\frac{W}{2}}\cdot[1-(\frac{2z}{L_{eff}}-1)^2].\end{aligned} \tag{4.47}$$

The boundary conditions for the above equation are that (1) at the center of the channel, the lateral electric field is zero, (2) at the source end, the electrostatic potential is a finite value: $\frac{\partial\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{\partial z}|_{z=\frac{L_{eff}}{2}} = 0$, and $\Psi(\frac{t_{si}}{2},\frac{W}{2},0) \simeq \frac{E_g}{2q}$, where E_g is the silicon energy bandgap. Solving Eq. (4.47) with boundary conditions, the distribution of the electrostatic potential in the channel length direction (z direction) in the middle of the silicon thin-film ($x = t_{si}/2$, $y = W/2$) is:

$$\Psi(\frac{t_{si}}{2},\frac{W}{2},z) = -c_0{l_0}^2 + \frac{\partial^2\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{\partial y^2}|_{y=\frac{W}{2}} \cdot {l_0}^2 \cdot [1 - \frac{8{l_0}^2}{L_{eff}^2} - (\frac{2z}{L_{eff}} - 1)^2] + \quad (4.48)$$
$$cosh[(z - \frac{L_{eff}}{2})/l_0] \cdot \beta \cdot [\frac{E_g}{2q} + c_0{l_0}^2 + \frac{\partial^2\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{\partial y^2}|_{y=\frac{W}{2}} \cdot {l_0}^2 \cdot \frac{8{l_0}^2}{L_{eff}^2}],$$

where $\beta = \frac{1}{cosh(L_{eff}/2l_0)}$. From Eq. (4.48), one obtains:

$$\frac{\partial^2\Psi(\frac{t_{si}}{2},\frac{W}{2},z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}} = \frac{\beta}{{l_0}^2} \cdot (\frac{E_g}{2q} + c_0{l_0}^2) - \beta' \cdot \frac{\partial^2\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{\partial y^2}|_{y=\frac{W}{2}}, \quad (4.49)$$

where $\beta' = (1-\beta) \cdot \frac{8{l_0}^2}{L_{eff}^2}$. From Eq. (4.46)(4.49), one obtains:

$$\frac{\partial^2\Psi(\frac{t_{si}}{2},y,\frac{L_{eff}}{2})}{\partial y^2}|_{y=\frac{W}{2}} = \frac{\alpha}{1-\alpha'\beta'} \cdot \frac{1}{{l_0}^2} \cdot (\Psi_G + c_0{l_0}^2) - \frac{\alpha'\beta}{1-\alpha'\beta'} \cdot \frac{1}{{l_0}^2} \cdot (\frac{E_g}{2q} + c_0{l_0}^2). \quad (4.50)$$

From Eqs. (4.48)(4.50), at $z = L_{eff}/2$, one obtains the electrostatic potential in the middle of the silicon thin-film:

$$\Psi(\frac{t_{si}}{2},\frac{W}{2},\frac{L_{eff}}{2}) = -[1 - \frac{\alpha(1-\beta')}{1-\alpha'\beta'} - \frac{\beta(1-\alpha')}{1-\alpha'\beta'}] \cdot c_0{l_0}^2 + \frac{\alpha(1-\beta')}{1-\alpha'\beta'} \cdot \Psi_G + \frac{\beta(1-\alpha')}{1-\alpha'\beta'} \cdot \frac{E_g}{2q}. \quad (4.51)$$

From Eqs. (4.51)(4.42), at the center of the surface channel ($x = 0$, $y = W/2$, $z = L_{eff}/2$), the electrostatic potential is:

$$\Psi(0,\frac{W}{2},\frac{L_{eff}}{2}) = \frac{C_{si}}{C_{ox1}} \frac{\Psi_{s3} - \Psi_G - \frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}}[1 - k(\frac{W}{2},\frac{L_{eff}}{2})](1 + 2\frac{C_{si}}{C_{ox2}})}{1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}}} + \Psi_G, \quad (4.52)$$

$$k(\frac{W}{2},\frac{L_{eff}}{2}) = 1 - \frac{2\epsilon_{si}}{qN_{si}{t_{si}}^2} \frac{(\frac{1}{2} + \frac{C_{si}}{C_{ox2}})\Psi_G + (\frac{1}{2} + \frac{C_{si}}{C_{ox1}})\Psi_{s3} - (1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}})\Psi(\frac{t_{si}}{2},\frac{W}{2},\frac{L_{eff}}{2})}{\frac{1}{4} + \frac{3}{4}\frac{C_{si}}{C_{ox1}} + \frac{3}{4}\frac{C_{si}}{C_{ox2}} + 2\frac{C_{si}}{C_{ox1}}\frac{C_{si}}{C_{ox2}}}.$$

When the front gate is biased at the threshold voltage of the center channel, the center of the surface channel enters strong inversion with an electrostatic potential: $\Psi(0, \frac{W}{2}, \frac{L_{eff}}{2}) = -\phi_{si}$. From Eqs. (4.51)&(4.52), the threshold voltage is:

$$V_{TH} = V_{FB} - \phi_{si} + \frac{-\phi_{si}(1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}}) - \Psi_{s3}\frac{C_{si}}{C_{ox1}}(1-\delta_2) - \frac{E_g}{2q}\frac{C_{si}}{C_{ox1}} \cdot \delta_3 + \frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}}\frac{C_{si}}{C_{ox1}}(1 + 2\frac{C_{si}}{C_{ox2}})(1-\delta_1)}{1 + \frac{C_{si}}{C_{ox1}}(\delta_2 - \delta_3) + \frac{C_{si}}{C_{ox2}}}, \quad (4.53)$$

where $\delta_1 = \frac{\alpha(1-\beta')}{1-\alpha'\beta'} + \frac{\beta(1-\alpha')}{1-\alpha'\beta'}$, $\delta_2 = \frac{1}{4}\frac{{t_{si}}^2}{{l_0}^2}\frac{(1+2\frac{C_{si}}{C_{ox1}})(1+2\frac{C_{si}}{C_{ox2}})}{(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})} \cdot \delta_1$, $\delta_3 = \frac{1}{2}\frac{{t_{si}}^2}{{l_0}^2}(1 + 2\frac{C_{si}}{C_{ox2}}) \cdot \frac{\beta(1-\alpha')}{1-\alpha'\beta'}$, and V_{FB} is the flat-band voltage of the front gate. Eq. (4.53) is the analytical threshold voltage model for the center channel considering 3D geometrical effects for small-geometry mesa-isolated fully-depleted ultrathin SOI NMOS devices derived from a quasi-3D approach. From Eqs. (4.45)(4.48), when L_{eff} and W are very large, α and β approach zero. Under this situation, δ_1, δ_2, and δ_3 in Eq. (4.53) also approach zero. Therefore, Eq. (4.53) is simplified to a model for the large-geometry case. Since Eq. (4.53) is applicable for fully-depleted devices, therefore, N_{si} and t_{si} should be restricted in the region: $N_{si} \leq \frac{-2\phi_{si}2\epsilon_{si}}{qt_{si}^2}$. In addition, since while deriving Eq. (4.39) there is an assumption that the silicon thin-film thickness is much smaller than the channel length and the channel width, therefore, the applicability of Eq.(4.53) is also limited. When the channel length and channel width (L_{eff}, W) are smaller than two times the silicon thin-film thickness ($2t_{si}$), the inaccuracy of the Eq. (4.53) becomes large.

Considering current conduction in a small-geometry SOI MOS device, in addition to the center channel, the sidewall channel cannot be overlooked. Therefore, the threshold voltage of the sidewall channel is also important. The threshold voltage of the sidewall channel is defined as the electrostatic potential at the sidewall equal to: $\Psi(\frac{t_{si}}{2}, W, \frac{L_{eff}}{2}) = -\phi_{si}$. From Eqs.(4.49)(4.50), one obtains: $\frac{\partial^2\Psi(\frac{t_{si}}{2}, \frac{W}{2}, z)}{\partial z^2}|_{z=\frac{L_{eff}}{2}}$. Then, from Eq. (4.45), the relationship between $\Psi(\frac{t_{si}}{2}, y, \frac{L_{eff}}{2})$ and y can be obtained. At y=W, one obtains the sidewall electrostatic potential:

$$\begin{aligned}\Psi(\frac{t_{si}}{2}, W, \frac{L_{eff}}{2}) &= -(1 - \alpha_s + \frac{\alpha_s'\beta}{1-\alpha'\beta'} - \frac{\alpha_s'\alpha\beta'}{1-\alpha'\beta'}) \cdot c_0{l_0}^2 + \\ &\quad (\alpha_s + \frac{\alpha_s'\alpha\beta'}{1-\alpha'\beta'}) \cdot \Psi_G - \frac{\alpha_s'\beta}{1-\alpha'\beta'} \cdot \frac{E_g}{2q},\end{aligned} \quad (4.54)$$

where $\alpha_s = \alpha \cdot cosh(W/2l_0)$, and $\alpha_s' = (1 - \alpha_s) \cdot \frac{8{l_0}^2}{W^2} - \alpha_s \cdot \frac{4t_{si}}{W}\frac{C_{si}}{C_{sw}}$. From Eq. (4.54),

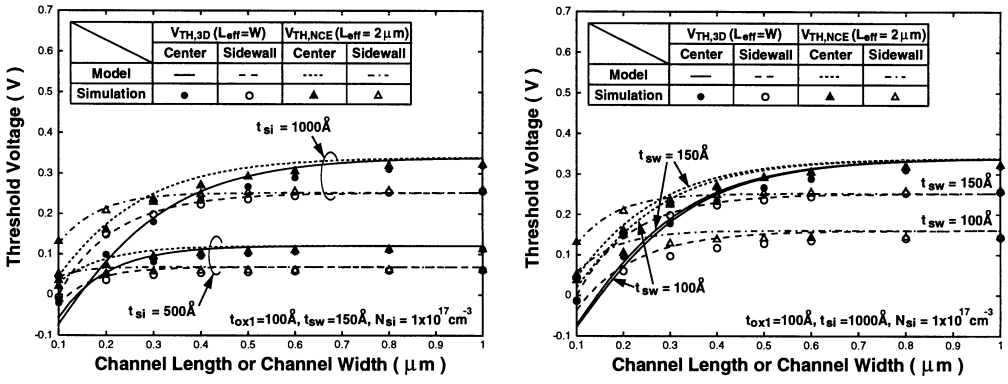


Figure 4.23: Threshold voltage versus channel width or channel length of the center and the sidewall portions in the SOI NMOS device with a front oxide of 100Å, a silicon thin-film doping density of $1 \times 10^{17}\text{cm}^{-3}$ and (a) with a sidewall oxide of 150Å and silicon thin-film thicknesses of 1000Å and 500Å (b) with a silicon thin-film thickness of 1000Å and sidewall oxide thicknesses of 100Å and 150Å based on the 3D simulation and the analytical model results.

the threshold voltage of the sidewall channel is:

$$V_{TH,s} = V_{FB} - \phi_{si} + \frac{-\phi_{si} + \delta_{1,s} \cdot \frac{qN_{si}l_0^2}{\epsilon_{si}} - \delta_{2,s} \cdot \Psi_{s3} + \delta_{3,s} \cdot \frac{E_g}{2q}}{1 - \delta_{2,s} + \delta_{3,s}}, \tag{4.55}$$

where $\delta_{1,s} = 1 - \alpha_s + \frac{\alpha'_s\beta}{1-\alpha'\beta'} - \frac{\alpha'_s\alpha\beta'}{1-\alpha'\beta'}$, $\delta_{2,s} = \frac{1}{2}\frac{1+2\frac{C_{si}}{C_{ox1}}}{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}} \cdot \delta_{1,s}$, and $\delta_{3,s} = \frac{\alpha'_s\beta}{1-\alpha'\beta'}$. Figs. 4.23(a) &(b) show the threshold voltage versus channel width or channel length of the center and the sidewall portions in the SOI NMOS device with a front oxide of 100Å, a silicon thin-film doping density of $1 \times 10^{17}\text{cm}^{-3}$ and (a) with a sidewall oxide of 150Å and silicon thin-film thicknesses of 1000Å and 500Å (b) with a silicon thin-film thickness of 1000Å and sidewall oxide thicknesses of 100Å and 150Å based on the 3D simulation and the analytical model results[45]. $V_{TH,3D}$ represents the threshold voltage of the device with identical channel length and channel width, which vary simultaneously. $V_{TH,NCE}$ represents the threshold voltage of the device when its channel width varies as the channel length is fixed at $2\mu m$. As shown in Fig. 4.23(a), with a silicon thin-film thickness of 1000Å, when the channel length

and the channel width are large, the threshold voltage of the sidewall channel is smaller than that of the center channel. Therefore, the sidewall channel turns on earlier than the center channel. In addition, in the subthreshold region, the hump phenomenon exists. When the channel length and the channel width are scaled down to very small dimensions, the threshold voltage of both the center channel and the sidewall channel becomes smaller. However, the extent of the change in the threshold voltage of the sidewall channel is much lighter. As a result, with very small channel length and channel width, the threshold voltage of the sidewall channel on the contrary is larger than that of the center channel. When the silicon thin-film thickness is scaled down to 500Å, the rate of the decrease in the threshold voltage of both the center channel and the sidewall channel is reduced. In addition, the difference in the threshold voltage between the center channel and the sidewall channel is reduced. This can be reasoned as the reduced 3D geometrical effect—when the silicon thin-film thickness is decreased, the control capability of the gate over the vertical direction of the silicon thin-film increases. Fig. 4.23(b) shows the threshold voltage at various sidewall oxide thicknesses, As shown in the figure, the thickness of the sidewall oxide becomes smaller, the threshold voltage curve of the center channel stays almost unchanged. In contrast, for the sidewall channel, its threshold voltage curve is sensitive to the sidewall oxide thickness. For the sidewall channel, regardless of the channel length or the channel width, its threshold voltage is reduced noticeable. Different from the center channel case, when the sidewall oxide is reduced, the 3D geometrical effect in the sidewall channel is lighter since the influence of the y direction in the sidewall channel is stronger than that in the center channel.

In Figs. 4.23(a)&(b), in addition to $V_{TH,3D}$ with respect to changing L_{eff} and W simultaneously (3D effect), $V_{TH,NCE}$ with respect to changing W only (narrow channel effect) is also shown. As shown in the figure, the trends on $V_{TH,3D}$ and $V_{TH,NCE}$ are similar except that the change in $V_{TH,NCE}$ is smaller than that in $V_{TH,3D}$. In addition, when the channel width is decreased, the edge effects become more important since when the center channel becomes more narrow, the contribution from the sidewall channel to the overall current conduction becomes more important. Furthermore, since the threshold voltage of the sidewall channel is smaller than that of the center channel, in the subthreshold region, current conduction is dominated by the sidewall channel.

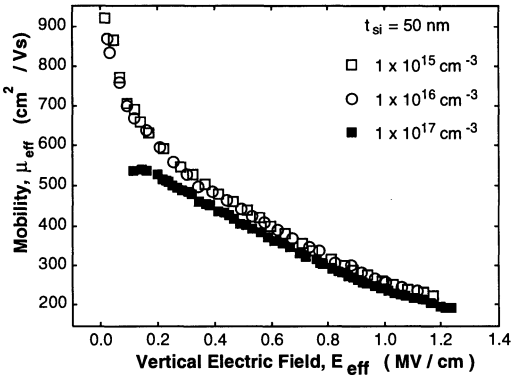


Figure 4.24: Electron mobility versus vertical electric field for an SOI NMOS device with a 500Å silicon thin-film as a function of the silicon thin-film doping density.

4.5 Mobility

In the previous sections, the threshold voltage of SOI CMOS devices has been analyzed. In addition to threshold voltage, mobility is another important parameter in determining the drain current of an SOI CMOS device. Mobility is dependent on impurity scattering and surface scattering . For an SOI NMOS device biased with a large electric field, the travelling carriers may possess a large amount of energy. As a result, the temperature of the travelling electrons may be much higher than the lattice temperature. The temperature of the travelling electrons also affects the electron mobility. In this section, analysis of the carrier mobility is divided into two portions. In the first portion, impurity-scattering and surface-scattering dependent mobility are described. In the second portion, the electron-temperature dependent mobility is analyzed.

4.5.1 Surface scattering mobility

Fig. 4.24 shows the electron mobility versus vertical electric field for an SOI NMOS device with a 500Å silicon thin-film as a function of the silicon thin-film doping density[47]. As shown in the figure, when the vertical electric field is low, the electron mobility varies when the silicon thin-film doping density changes. This implies that when the vertical electric field is small, impurity scattering dominates the electron mobility— the low-field mobility. On the other hand, when the vertical electric field is large, the electron mobility is independent of the silicon thin-film doping

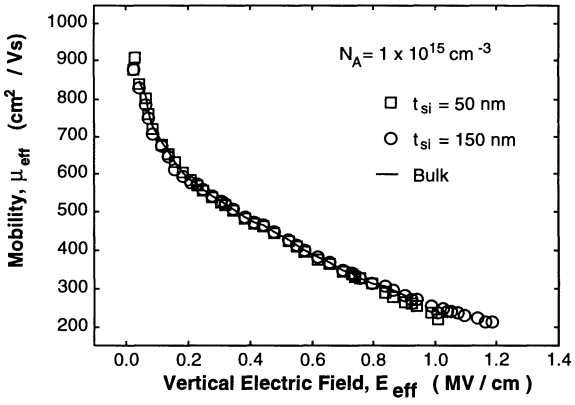


Figure 4.25: Electron mobility versus vertical electric field for an SOI NMOS device with a silicon thin-film doping density of $10^{15}cm^{-3}$ for two silicon thin-film thicknesses.

density. This means that at a large vertical electric field, impurity scattering is less important—surface scattering is more important. Fig. 4.25 shows the electron mobility versus vertical electric field for an SOI NMOS device with a silicon thin-film doping density of $10^{15}cm^{-3}$ for two silicon thin-film thicknesses [47]. Also shown in the figure is the case for the bulk NMOS device. As shown in the figure, regardless of the silicon thin-film thickness, the electron mobility curves are identical. In addition, the vertical-electric-field dependent electron mobility curves are similar for both bulk and SOI devices. Fig. 4.26 shows the electron mobility versus vertical electric field of an SOI NMOS device with the silicon thin-film thickness as a parameter[48]. Contrary to the case as shown in Fig. 4.25, the electron mobility curve in Fig. 4.26 is sensitive to the silicon thin-film thickness when the thickness is very smalll. As shown in the figure, when the silicon thin-film thickness is smaller than 100Å, the effective mobility is silicon thin-film thickness dependent due to the stress in the silicon thin-film, which is caused by the difference in the thermal expansion coefficients between the silicon thin-film and the oxide layers. Considering the impurity scattering and the vertical electric field dependent mobilities, the surface electron mobility is written as [49]:

$$\mu_{so} = \frac{\mu_o}{1 + \theta(V_G - V_T)}, \tag{4.56}$$

where μ_o is the low-field mobility considering impurity scattering, and θ is the surface mobility coefficient.

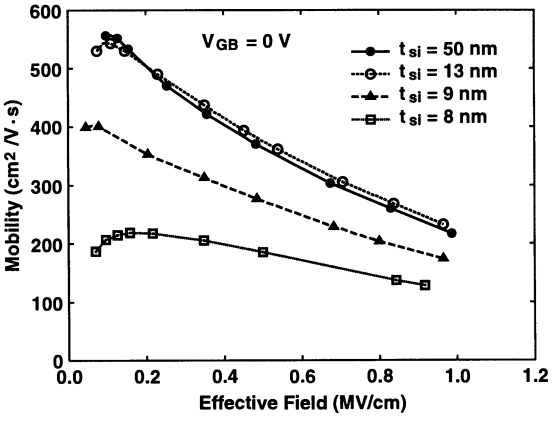


Figure 4.26: Electron mobility versus vertical electric field of an SOI NMOS device with the silicon thin-film thickness as a parameter.

4.5.2 Electron temperature

Sub-0.1μm MOS devices have been developed [50][51] for next generation VLSI. For deep-submicron MOS devices with a very small channel length, the lateral electric field in their lateral channel may be very high. Therefore, the carrier temperature can be much higher than the substrate temperature. As a result, the carrier mobility may be degraded due to the elevated carrier temperature[52][53]. A temperature-dependent electron mobility model, which is referred to the difference between the electron temperature (T_n) and the lattice temperature (T_l), is expressed as[52]:

$$\mu_n = \frac{\mu_s(T_l)}{1 + \alpha\frac{k}{q}(T_n - T_l)}, \tag{4.57}$$

where $\alpha = 3\mu_s(T_l)/2v_{sat}^2\tau_\epsilon$, v_{sat} is the saturation velocity , and τ_ϵ is the energy relaxation time. $\mu_s(T_l)$ is the electron surface mobility [54]:

$$\mu_s(T_l) = \mu_{so}(\frac{T_l}{T_o})^{-2}, \tag{4.58}$$

where μ_{so} is the electron surface mobility at the ambient temperature (T_o) as described in the previous subsection.

In addition to the influence in the carrier mobility, sometimes carrier temperature may cause peculiar phenomenon— velocity overshoot. For carriers travelling

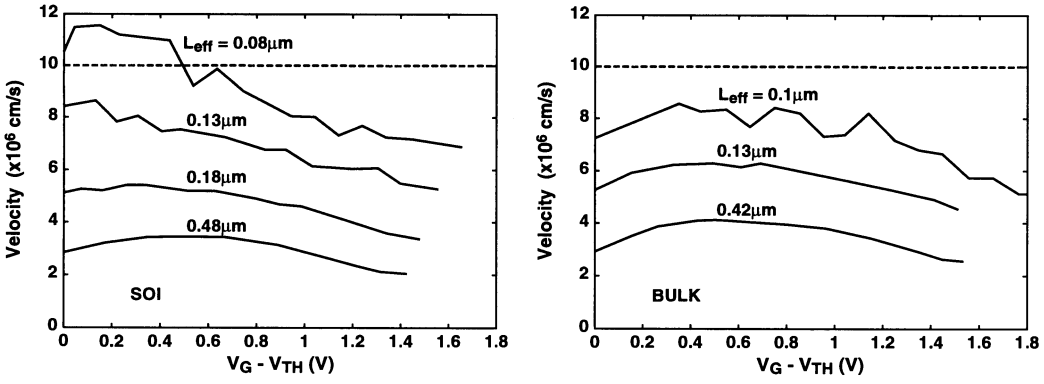


Figure 4.27: Electron velocity versus the gate over-drive voltage of an SOI NMOS device and a bulk NMOS device with the channel length as a parameter, biased at a drain voltage of 1V.

through the lateral channel region with a rapid change in electric field from low to high in a very short device, their speed may exceed steady-state saturation velocity – the velocity overshoot phenomenon[55]. Velocity overshoot is due to the nonequivalence of electron momentum and energy relaxation times [56]. For silicon, velocity overshoot phenomenon is not easy to identify because of its small energy relaxation time[57]. Velocity overshoot is noticeable when the channel length of an MOS device is shorter than 0.1μm. Fig. 4.27 shows the electron velocity versus the gate over-drive voltage of an SOI NMOS device and a bulk NMOS device with the channel length as a parameter, biased at a drain voltage of 1V[58]. As shown in the figures, for the SOI device, with a channel length of 0.08μm, when the gate over-drive voltage ($V_G - V_{TH}$) is smaller than 0.4V, there is velocity overshoot. Compared to SOI devices, for the bulk device, the electron velocity is smaller than that for the SOI device due to a larger impurity scattering from a higher silicon doping density. At a higher gate over-drive voltage, for both SOI and bulk devices, the electron velocity is smaller. Fig. 4.28 shows the electron velocity versus the channel length in SOI and bulk NMOS devices biased at a drain voltage of 1V and at a gate over-drive voltage of 0.1V and 1V[58]. At a smaller gate over-drive voltage, the electron mobility of the SOI device is 20% higher than that of the bulk device. At a larger gate over-drive voltage, the difference in the electron mobility between the SOI and the bulk devices disappears. This implies that when the vertical electric field is small, the electron velocity in the SOI device is larger than that in the bulk device due to a lighter doping density in the SOI device. When the gate over-drive voltage is large,

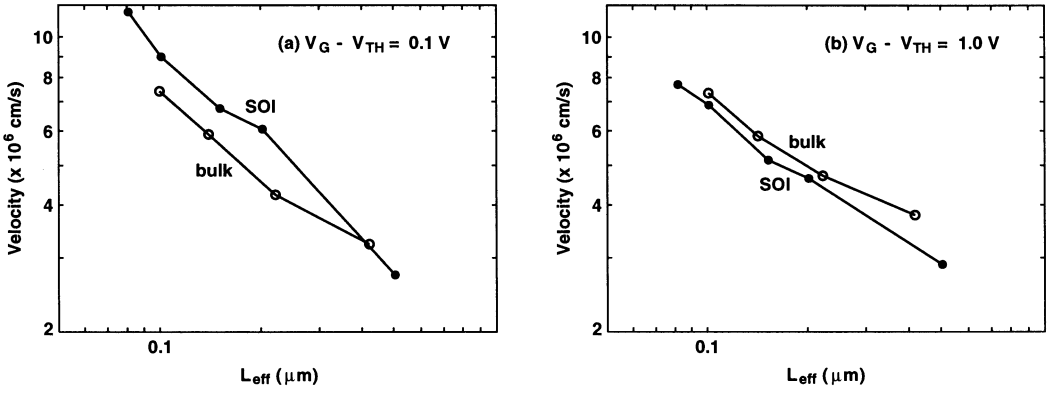


Figure 4.28: Electron velocity versus the channel length in SOI and bulk NMOS devices biased at a drain voltage of 1V and at a gate over-drive voltage of 0.1V and 1V.

impurity scattering is less important— the vertical electric field effect dominates the electron velocity.

In this section, carrier mobility of a deep-submicron SOI CMOS devices has been described. For a deep-submicron SOI CMOS device, its carrier mobility is related to impurity scattering, which is dependent on the doping density of the silicon thin-film, and surface scattering, which is determined by the vertical electric field. In addition, the carrier temperature and the lattice temperature are also important in determining the carrier mobility. When the channel length is close to 0.1μm, velocity overshoot of carriers in the SOI CMOS devices may exist.

4.6 Subthreshold Current

Until now in this chapter, the threshold voltage and the carrier mobility of the SOI CMOS devices have been described. In this section, the subthreshold conduction behavior of an SOI CMOS device is presented.

The subthreshold behavior of an SOI MOS device depends on the thickness of the silicon thin-film, the doping density of the silicon thin-film, and the channel length. Fig. 4.29 shows the inverse subthreshold slope versus silicon thin-film thickness of an SOI NMOS device with a front gate oxide of 250Å, a buried oxide of

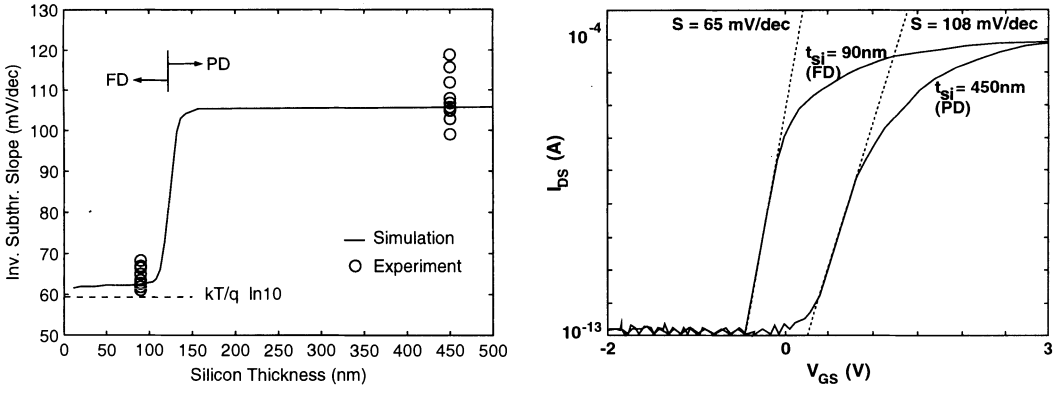


Figure 4.29: Inverse subthreshold slope versus silicon thin-film thickness of an SOI NMOS device with a front gate oxide of 250Å, a buried oxide of 1μm, a p-type doping density of 8×10^{16}cm^{-3}, an aspect ratio of W/L = 10μm/3μm, and interface state densities of 10^{11}cm^{-2} and 2×10^{11}cm^{-2} at the front and the back oxide interfaces in the silicon thin-film, respectively. The drain voltage is 1V.

1μm, a p-type doping density of 8×10^{16}cm^3, an aspect ratio of W/L = 10μm/3μm, interface state densities of 10^{11}cm^{-2} and 2×10^{11}cm^{-2} at the front and the back oxide interfaces in the silicon thin-film, respectively[59]. As shown in the figure, when the silicon thin-film is thick—partially-depleted, the subthreshold slope of the SOI NMOS device is similar to that of the bulk devices. When the silicon thin-film is thin—fully-depleted, its subthreshold slope is much better with its value close to the ideal case— (kT/q)(ln10)mV/dec due to the buried oxide isolation between the channel and the grounded substrate. Fig. 4.30 shows the inverse subthreshold slope of the partially-depleted and fully-depleted SOI NMOS devices with a buried oxide of 5000Å, a front gate oxide of 50Å, and a channel length of 10μm[60]. As shown in the figure, for a partially-depleted device, a higher silicon thin-film doping density leads to a worse inverse subthreshold slope—similar to the bulk device. In contrast, for a fully-depleted device, the inverse subthreshold slope is less sensitive to the silicon thin-film doping density. A higher silicon thin-film doping density leads to a better inverse subthreshold slope. For fully-depleted devices, its depletion width is fixed at the silicon thin-film thickness. Therefore, its inverse subthreshold slope is not sensitive to the silicon thin-film thickness. When the doping density of the silicon thin-film increases, its electric field increases. As a result, carriers tend to move close to the front surface. Consequently, a better front gate controllability leads to a slightly better inverse subthreshold slope. Fig. 4.31 shows the inverse

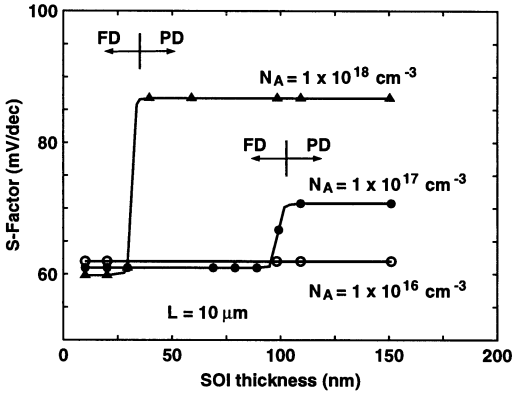


Figure 4.30: Inverse subthreshold slope of the partially-depleted (PD) and fully-depleted (FD) SOI NMOS devices with a buried oxide of 5000Å, a front gate oxide of 50Å, and a channel length of 10μm.

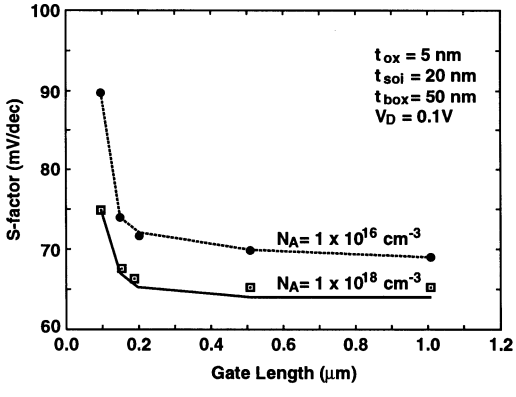


Figure 4.31: Inverse subthreshold slope versus gate length of an SOI NMOS device with a front gate oxide of 50Å, a silicon thin-film of 200Å, and a buried oxide of 500Å.

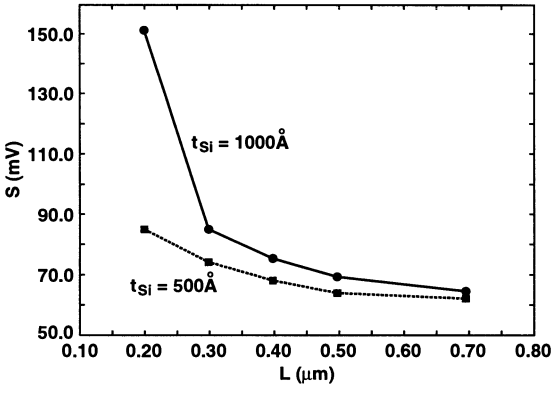


Figure 4.32: The inverse subthreshold slope versus channel length of an SOI NMOS device with a front gate oxide of 70Å, a buried oxide of 3300Å, and a p-type doping density of $2 \times 10^{16} cm^{-3}$ in the silicon thin-film.

subthreshold slope versus gate length of an SOI NMOS device with a front gate oxide of 50Å, a silicon thin-film of 200Å, and a buried oxide of 500Å[60]. As shown in the figure, when the channel length decreases, the 2D effect from the source/drain on the potential distribution influences the front gate controllability over the silicon thin-film—the inverse subthreshold slope becomes worse. From this figure, by raising the doping density of the silicon thin-film, the inverse subthreshold slope can be improved. Fig. 4.32 shows the inverse subthreshold slope versus channel length of an SOI NMOS device with a front gate oxide of 70Å, a buried oxide of 3300Å, and a p-type doping density of $2 \times 10^{16} cm^{-3}$ in the silicon thin-film[61]. As shown in the figure, when the channel length becomes smaller, the inverse subthreshold slope becomes worse. By decreasing the silicon thin-film thickness, the inverse subthreshold slope can be improved—when the thickness of the silicon thin-film becomes smaller, the front gate controllability becomes better.

Fig. 4.33 shows the subthreshold characteristics of a mesa-isolated SOI NMOS device[62]. As shown in the figure, a hump in the subthreshold characteristics can be seen. The hump is caused by the 2D effect, which results in a smaller threshold voltage for the sidewall channel as compared to the center channel. Here, analysis of the subthreshold behavior with a hump of a mesa-isolated SOI NMOS device is presented.

In order to simplify the analysis, a channel length of $1 \mu m$ has been used to

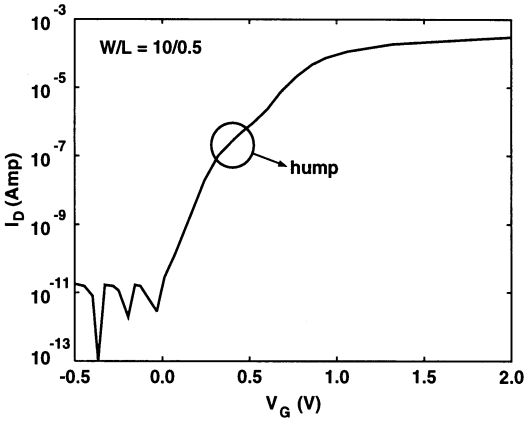


Figure 4.33: Subthreshold characteristics of a mesa-isolated SOI NMOS device.

avoid short channel effects. In the following analysis, the source and the substrate terminals are connected to ground. Fig. 4.34 shows the 3D electron density contours in the silicon thin-film of the ultrathin SOI NMOS devices with channel widths of $0.3\mu m$ and $1.2\mu m$, biased at $V_G = 0V$ and $V_D = 10mV$ ($V_S = 0V$, $V_B = 0V$) based on the 3D simulation results[64]. As shown in the figure, the distribution of the electron density is not uniform in the y-direction at the silicon thin-film surface. At the location near the sidewall, the electron density is higher— the sidewall induced electrons are important. With a narrower channel, the sidewall induced electrons are more important in affecting the current conduction. Therefore, the current conduction model assuming a uniform electron density profile in the y-direction for a wide-channel device is not applicable. In the analytical current conduction model presented in this section, the non-uniformity in the electron density profile due to the influence of the sidewall oxide is considered. In order to simplify the analysis, the y-direction of the channel is divided into two portions: (1) the center portion and (2) the sidewall portion. In the center portion, the electron profile is assumed to be uniform. In the sidewall portion, the electron density is higher than that in the center portion. In the following subsections, the current conduction models in the center and the sidewall portions are derived.

4.6.1 Center portion

The threshold voltage of the center portion ($V_{TH,center}$) is defined as the gate voltage when the electrostatic potential at the front Si/SiO_2 interface in the center of the

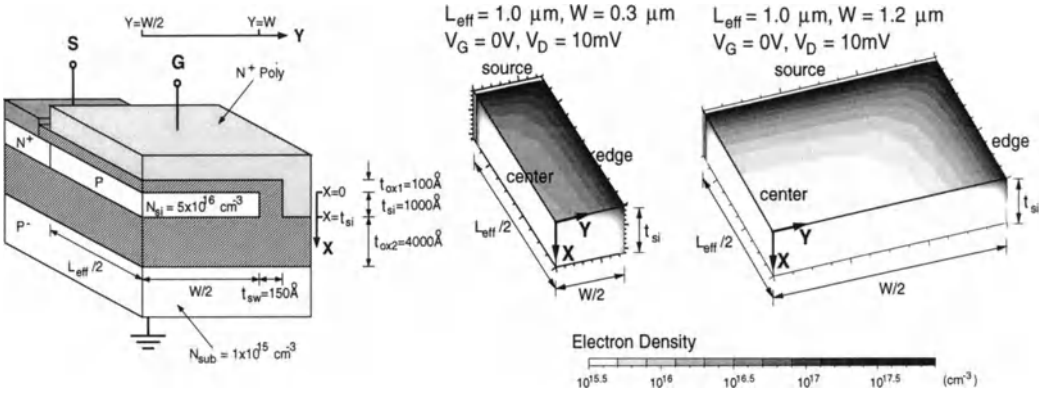


Figure 4.34: The 3D electron density contours of the ultrathin SOI NMOS devices with channel widths of 0.3μm and 1.2μm, biased at $V_G = 0V$ and $V_D = 10mV$ based on the 3D simulation results.

channel ($\Psi(x = 0, y = \frac{W}{2})$) reaches $-\phi_{si}$ ($\phi_{si} = \frac{kT}{q} ln \frac{n_i}{N_{si}}$), where N_{si} is the p-type doping density of the silicon thin-film and n_i is the intrinsic carrier density. From Ref. [33], considering the influence from the sidewall the threshold voltage is:

$$\begin{aligned} V_{TH,center} &= V_{FB} - \phi_{si} \\ &+ \frac{-\phi_{si}(1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}}) - \Psi_{s3}\frac{C_{si}}{C_{ox1}}(1 - \alpha') + \frac{qN_{si}t_{si}^2}{2\epsilon_{si}}\frac{C_{si}}{C_{ox1}}(1 + 2\frac{C_{si}}{C_{ox2}})(1 - 2\alpha)}{1 + \alpha'\frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}}}, \end{aligned} \tag{4.59}$$

where $\alpha = ((1 - \frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_0})e^{-W/2l_0} + (1 + \frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_0})e^{W/2l_0})^{-1}$, $\alpha' = \alpha \cdot \frac{t_{si}^2}{l_0^2}\frac{(\gamma + \frac{C_{si}}{C_{ox1}})(1 + 2\frac{C_{si}}{C_{ox2}})}{1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}}}$, $l_0 = t_{si}\sqrt{\frac{(\gamma - \gamma^2) + (1 - \gamma^2)\frac{C_{si}}{C_{ox1}} + (2\gamma - \gamma^2)\frac{C_{si}}{C_{ox2}} + 2\frac{C_{si}}{C_{ox1}}\frac{C_{si}}{C_{ox2}}}{2(1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}})}}$, $C_{si} = \frac{\epsilon_{si}}{t_{si}}$, $C_{ox1} = \frac{\epsilon_{ox}}{t_{ox1}}$, $C_{ox2} = \frac{\epsilon_{ox}}{t_{ox2}}$, and $C_{sw} = \frac{\epsilon_{ox}}{t_{sw}}$. Note that t_{ox1} and t_{ox2} are the thicknesses of the front and the buried oxides, respectively. t_{sw} is the thickness of the sidewall oxide. V_{FB} is the flatband voltage of the front gate. Ψ_G is the gate electrostatic potential when the center channel turns on. $\gamma = 1$. Ψ_{s3} is the electrostatic potential at the surface of the substrate below the buried oxide.

Using the value for the wide channel device for Ψ_{s3} and considering the 2D effect on the electrostatic potential distributions as explained before, the electrostatic

potential at the front oxide interface ($\Psi(0, \frac{W}{2})$) is such that :

$$V_G - V_{FB} + \phi_{si} = \frac{\Psi(0, \frac{W}{2}) \cdot (1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}}) - \Psi_{s3}\frac{C_{si}}{C_{ox1}}(1-\alpha') + \frac{qN_{si}t_{si}^2}{2\epsilon_{si}}\frac{C_{si}}{C_{ox1}}(1 + 2\frac{C_{si}}{C_{ox2}})(1-2\alpha)}{1 + \alpha'\frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}}}. \tag{4.60}$$

From the above equation, one obtains the following parameters:

$$n_{center} = (\frac{\partial\Psi(0, \frac{W}{2})}{\partial V_G})^{-1} = \frac{1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}}}{1 + \alpha'\frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}} + \frac{C_{si}}{C_{ox1}}(1-\alpha') \cdot \frac{\partial\Psi_{s3}}{\partial V_G}}, \tag{4.61}$$

where $\frac{\partial\Psi_{s3}}{\partial V_G}$ is the simplified result using the wide channel approximation. ϕ_{sub} is the Fermi potential of the substrate $\phi_{sub} = \frac{kT}{q} ln \frac{n_i}{N_{sub}}$. In order to simplify the analysis, by considering only the 1D situation, the depletion width in the substrate is $\sqrt{\frac{2\epsilon_{si}(\Psi_{s3} - \phi_{sub})}{qN_{sub}}}$. The corresponding effective depletion capacitance is $C_{sub} = \sqrt{\frac{\epsilon_{si} q N_{sub}}{2(\Psi_{s3} - \phi_{sub})}}$. Considering the 'capacitance divider' effect, $\frac{\partial\Psi_{s3}}{\partial V_G}$ is approximately $\frac{1/C_{sub}}{1/C_{ox1} + 1/C_{si} + 1/C_{ox2} + 1/C_{sub}}$. From Eq. (4.61), the diffusion current of the device is [63]:

$$I_{center,diff} = I_1 \cdot \frac{W}{L_{eff}} \cdot (1 - exp(-\frac{V_D}{\phi_t})) \cdot \frac{exp(\frac{V_G - V_{TH,center}}{n_{center} \cdot \phi_t})}{1 + exp(\frac{V_G - V_{TH,center}}{n_{center} \cdot \phi_t})}, \tag{4.62}$$

where I_1 is a constant and $\phi_t = kT/q$. When the device is biased at $V_G < V_{TH,center}$ the drift current of the center portion ($I_{center,drift}$) is zero. When $V_G > V_{TH,center}$, the center portion enters the strong inversion region. Hence, the drift current of the center portion is:

$$I_{center,drift} = \frac{\mu_{n0}}{1 + \theta \cdot (V_G - V_{TH,center})} \cdot \frac{V_D - V_J}{L_{eff}} \cdot (C_{ox1} \cdot W) \cdot (V_G - V_{TH,center}), \tag{4.63}$$

where μ_{n0} is the electron low-field mobility, θ is a parameter used to describe the influence of the vertical electric field in the mobility, and V_J is the extra voltage drop over the source/drain-channel junctions. The total drain current of the center portion is the sum of the drift current and the diffusion current:

$$I_{D,center} = I_{center,diff} + I_{center,drift}. \tag{4.64}$$

4.6.2 Sidewall portion

The current conduction in the sidewall portion of the ultrathin SOI NMOS device is due to the non-uniform electron profile in the lateral y-direction. The gate voltage for the surface at each location in the lateral y-direction to reach strong inversion is different. In order to simplify the analysis, the threshold voltage of the sidewall portion of the device is defined as the gate voltage when strong inversion starts to exist at the sidewall (x=0, y=W)— $\Psi(x=0, y=W) = -\phi_{si}$. From Ref. [33][64], the threshold voltage of the sidewall portion is:

$$V_{TH,edge} = V_{FB} - \phi_{si} + \frac{-\phi_{si}(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}) - \Psi_{s3}\frac{C_{si}}{C_{ox1}}(1-\beta') + \frac{qN_{si}t_{si}^2}{2\epsilon_{si}}\frac{C_{si}}{C_{ox1}}(1+2\frac{C_{si}}{C_{ox2}})(1-2\beta)}{1+\beta'\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}}, \tag{4.65}$$

where $\beta = \alpha \cdot cosh(\frac{W}{2l_0})$, and $\beta' = \alpha' \cdot cosh(\frac{W}{2l_0})$. Ψ'_G is the gate electrostatic potential when the edge channel region turns on. (Note Ψ'_G is different from Ψ_G.) Similarly, n_{edge} of the sidewall portion is:

$$n_{edge} = (\frac{\partial\Psi(0,W)}{\partial V_G})^{-1} = \frac{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}}{1+\beta'\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}+\frac{C_{si}}{C_{ox1}}(1-\beta')\cdot\frac{\partial\Psi_{s3}}{\partial V_G}}. \tag{4.66}$$

From Eq. (4.66), the diffusion current of the sidewall portion is:

$$I_{edge,diff} = \frac{I_2}{L_{eff}}\cdot(1-exp(-\frac{V_D}{\phi_t}))\cdot\frac{exp(\frac{V_G-V_{TH,edge}}{n_{edge}\cdot\phi_t})}{1+exp(\frac{V_G-V_{TH,edge}}{n_{edge}\cdot\phi_t})}, \tag{4.67}$$

where I_2 is a constant. As for the center portion, in the sidewall portion the drift current ($I_{edge,drift}$) is zero at $V_G < V_{TH,edge}$. At $V_G > V_{TH,edge}$, the sidewall portion enters strong inversion. Hence, the drift current of the sidewall portion is

$$I_{edge,drift} = \frac{\mu_{n0}}{1+\theta\cdot(V_G-V_{TH,edge})}\cdot\frac{V_D-V_J}{L_{eff}}\cdot(2C_e+2C_{sw}\cdot t_{si})\cdot(V_G-V_{TH,edge}), \tag{4.68}$$

where $C_{sw}t_{si}$ is used to describe the existence of the electrons in the inversion region at the sidewall, and C_e is a fitting parameter used to account for the increase in the electron density at the silicon thin-film surface near the sidewall region. The drain current of the sidewall portion is the sum of the diffusion current and the drift current:

$$I_{D,edge} = I_{edge,diff} + I_{edge,drift}. \tag{4.69}$$

Parameter	Value
L_{eff}	$1.0\mu m$
W	$1.2\mu m$
t_{ox1}	100Å
t_{sw}	150Å
t_{ox2}	4000Å
t_{si}	1000Å
N_{si}	$5.0 \times 10^{16} cm^{-3}$
N_{sub}	$1.0 \times 10^{15} cm^{-3}$
μ_{n0}	$408 cm^2/V \cdot sec$
θ	$0.25/V$
γ	1.0
V_{FB}	$-0.915V$
V_J	$0.006V$
I_1	$0.12\mu A$
I_2	$1.0pA \cdot cm$
C_e	$5.6pF/cm$

Table 4.1: Parameters of the device under study.

The total drain current of the mesa-isolated ultrathin SOI NMOS device is composed of the drain currents in the center and the sidewall portions:

$$I_{D,total} = I_{D,center} + I_{D,edge}. \tag{4.70}$$

The above equations are the analytical drain current model for the mesa-isolated fully-depleted SOI NMOS device considering the influence of the sidewall.

As listed in Table 4.1, the test device for studying the subthreshold behavior has a channel length of $1\mu m$. In the table, γ, I_1, I_2, and C_e are fitting parameters used in the compact model (they are not required in the 3D simulation). For the compact model and the 3D simulation, V_{FB} is identical in both the center and the sidewall portions. Fig. 4.35 shows the drain current versus the gate voltage of the ultrathin SOI NMOS device with a channel length of $1\mu m$ and a channel width of $1.2\mu m$ based on the analytical model and the 3D simulation results[64]. As shown in the figure, from the $I_{D,edge}$ and $I_{D,center}$ curves, the threshold voltage of the sidewall portion is smaller than that of the center portion. Therefore, in the subthreshold region, the drain current of the sidewall portion ($I_{D,edge}$) dominates. At a

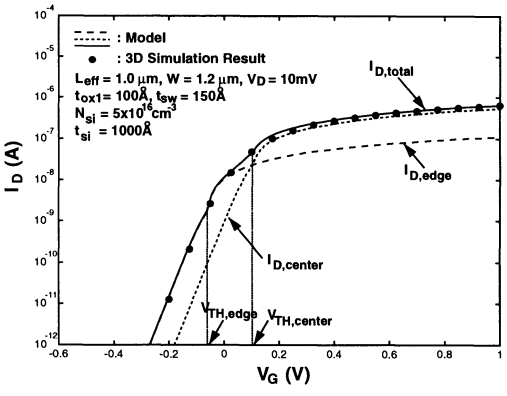


Figure 4.35: The drain current versus the gate voltage of the ultrathin SOI NMOS device with a channel length of 1μm and a channel width of 1.2μm.

large V_G in the strong inversion region, the dominance of the center portion drain current ($I_{D,center}$) can be identified. From this figure, the drain currents in both the center and the sidewall portions should be considered simultaneously, especially in the moderate inversion region when the gate voltage is near the threshold voltage.

Fig. 4.36 shows the drain current versus the gate voltage of the ultrathin SOI NMOS devices with channel widths of $2.4\mu m$ and $0.3\mu m$ and (a) gate oxide thicknesses of 100Å and 200Å; sidewall oxide thicknesses of 150Å and 300Å, (b) silicon thin-film thicknesses of 500Å and 1000Å, (c) silicon thin-film doping densities of $2 \times 10^{16} cm^{-3}$ and $5 \times 10^{16} cm^{-3}$ based on the analytical model and the 3D simulation results[64]. As shown in Fig. 4.36(a), when the front oxide (t_{ox1}) and the sidewall oxide (t_{sw}) become thicker, the subthreshold region with its drain current less sensitive to the channel width becomes larger. This implies that when the thickness of the front oxide (t_{ox1}) increases, the threshold voltages of both the center and the sidewall portions ($V_{TH,center}$, $V_{TH,edge}$) increase. However, the increase in the threshold voltage of the center portion ($V_{TH,center}$) is larger. Therefore, the difference between $V_{TH,center}$ and $V_{TH,edge}$ becomes wider. As a result, the drain current of the sidewall portion ($I_{D,edge}$) dominates in a wider subthreshold region. For the case with t_{ox1} = 200Å and t_{sw} = 300Å, the subthreshold current for $W = 2.4\mu m$ is a little bit smaller than that for $W = 0.3\mu m$. This is due to the fact that when the channel width is scaled down, the threshold voltage of the sidewall portion ($V_{TH,edge}$) drops slightly. As shown in Figs.4.36(b)&(c), when the thickness of the silicon thin-film (t_{si}) becomes thinner or the doping density of the silicon thin-film (N_{si}) becomes

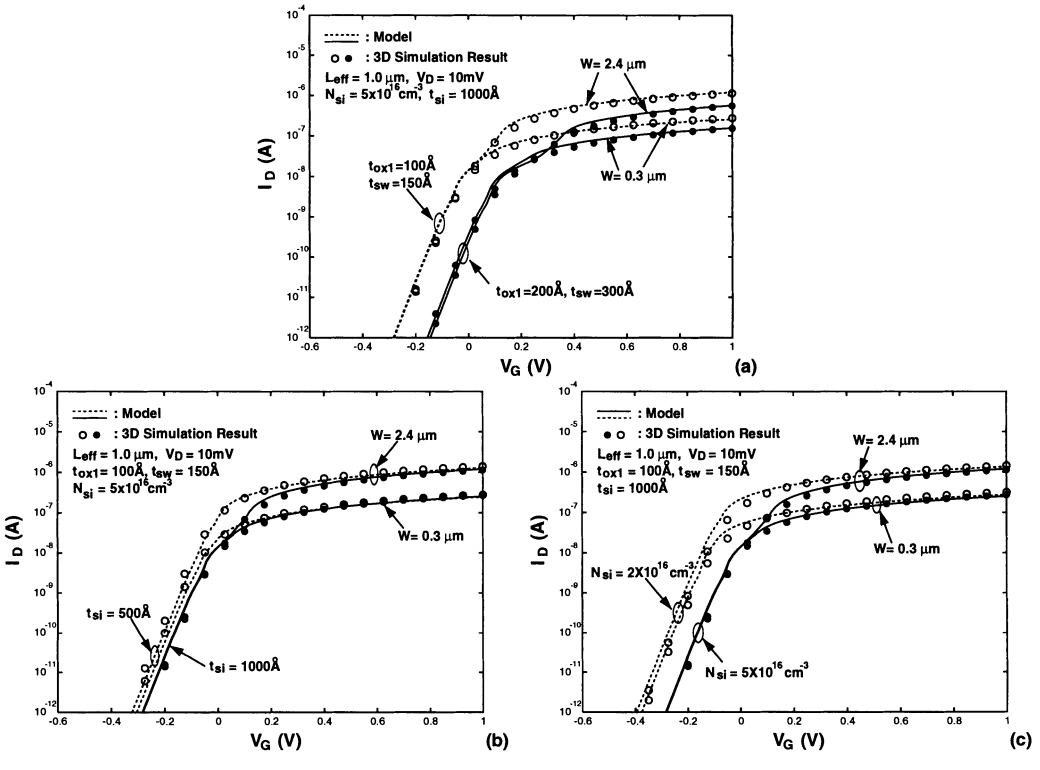


Figure 4.36: The drain current versus the gate voltage of the ultrathin SOI NMOS devices with channel widths of $2.4\mu m$ and $0.3\mu m$ and (a) gate oxide thicknesses of 100Å and 200Å; sidewall oxide thicknesses of 150Å and 300Å, (b) silicon thin-film thicknesses of 500Å and 1000Å, (c) silicon thin-film doping densities of $2 \times 10^{16} cm^{-3}$ and$5 \times 10^{16} cm^{-3}$ based on the analytical model and the 3D simulation results.

lighter, different from Fig. 4.36(a), their subthreshold curves are sensitive to the channel width. This implies that at a thinner silicon thin-film or at a more lightly doped silicon thin-film, the threshold voltages of both the center and the sidewall portions ($V_{TH,center}$, $V_{TH,edge}$) become smaller. In addition, the magnitude of the shrinkage in the threshold voltage of the center portion ($V_{TH,center}$) is larger, therefore, the difference between $V_{TH,center}$ and $V_{TH,edge}$ shrinks. Under this situation, the total subthreshold current is not dominated by the edge portion ($I_{D,edge}$). In this subthreshold region, its drain current curves are also influenced by the channel width.

In this section, analysis of the subthreshold drain current for a deep-submicron SOI NMOS device has been reported. Based on the analysis, in the subthreshold region the channel current near the sidewall dominates due to narrow channel effects.

4.7 Strong Inversion Drain Current

Until now in the chapter, the threshold voltage, the short channel effect, the narrow channel effect, the mobility, and the subthreshold current of the SOI CMOS devices have been reported. In this section, the drain current of the SOI CMOS devices biased in the strong inversion is described. When describing the strong inversion drain current, the threshold voltage, the small-geometry effects including the short and narrow channel effects and the mobility models are required. As reported in the previous section, the electron mobility in an SOI NMOS device is susceptible to the influence from the electron temperature and the lattice temperature. Due to the poor thermal conductivity of the buried oxide, which has a thermal conductivity 40 times larger than silicon, the deep-submicron SOI NMOS devices have self-heating problems [65][66][67]— the lattice temperature may rise at a large current. As a result, the electron mobility in the channel is degraded. Fig. 4.37 shows the IV characteristics of an SOI NMOS with a front gate oxide of 120Å and a silicon thin-film of 1200Å and two buried oxide thicknesses—1100Å and 3800Å[68]. As shown in the figure, due to the decreased power dissipation capability, when the thickness of the buried oxide is increased, the drain current is reduced in the saturation region. This is the result of the so-called self-heating, which is especially noticeable at the high current regime. As a result, at the high current regime, negative differential output resistance can be seen. When the thickness of the buried oxide is reduced, the self-heating phenomenon is lessened. In the following portion of this section, a drain current model for the small-geometry SOI CMOS devices biased in the strong inversion region considering small-geometry effects, electron temperature and lattice temperature effects is presented[65].

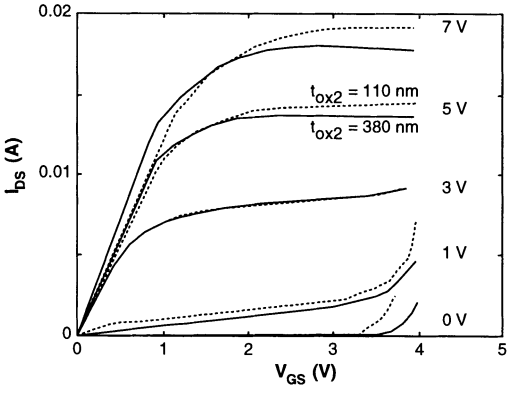


Figure 4.37: IV characteristics of an SOI NMOS device with a front gate oxide of 120Å and a thi-film of 1200Å and two buried oxide thicknesses—1100Å and 3800Å.

For NMOS devices with a deep submicron channel length, conventional drift-diffusion models are not sufficient [52]. The electron temperature may be much higher than the lattice temperature owing to the high electric field. As a result, energy transport is also important in determining the current conduction of the device [69]. In addition, due to self-heating, the lattice temperature also affects the current conduction in a deep submicron ultrathin SOI NMOS device. In order to obtain an accurate drain current model for the device, energy balance equation should also be solved simultaneously.

Consider a deep-submicron ultrathin SOI NMOS device with a very short channel. Due to its very small channel length, heat conduction in the silicon thin-film of the device is very quick. Therefore, the lattice temperature (T_l), which is assumed uniform, is linearly related to the power dissipated in the device [54]:

$$PR_{th} = T_l - T_o, \tag{4.71}$$

where T_o is the ambient temperature, and P is the dissipated power, which is expressed as the product of the drain current and the drain voltage: $P = I_D V_D$. R_{th} is the thermal resistance of the device. If the thermal healing length , which is $1/m_d = (\frac{K_d t_{si}}{h})^{\frac{1}{2}}$, where K_d is the silicon thermal conductivity, t_{si} is the silicon thin-film thickness, and h is the heat transfer coefficient, is smaller than gate-to-metal contact spacing (L_d), the thermal resistance can be approximated as[66]: $R_{th} \cong \frac{1}{2W}(\frac{t_{box}}{K_{ox} K_d t_{si}})^{\frac{1}{2}}$, where W is the channel width, t_{box} the thickness of the buried

oxide, and K_{ox} is the oxide thermal conductivity. For the ultrathin SOI NMOS device under study with its parameters as listed in the table in this section, its thermal resistance is $1.253 \times 10^4 K/W$.

Considering the electric field, the electron and the lattice temperature effects, the energy balance equation is:

$$q\mu_n E^2 = \frac{3}{2}k\frac{T_n - T_l}{\tau_\epsilon} - \frac{5}{2}k\mu_n E\frac{dT_n}{dy}, \tag{4.72}$$

where the second order term has been neglected [53], E is the electric field, T_n is the electron temperature, τ_ϵ is the energy relaxation time, y is the lateral channel direction, and k is Boltzmann constant.

A temperature-dependent electron mobility model [52] as described in the previous section is referred to the difference between the lattice temperature and the electron temperature as: $\mu_n = \frac{\mu_s(T_l)}{1+\alpha\frac{k}{q}(T_n - T_l)}$, where $\alpha = \frac{3\mu_s(T_l)}{2v_{\text{sat}}^2\tau_\epsilon}$, $\mu_s(T_l)$, which is the electron surface mobility considering lattice temperature. T_l is related to the lattice temperature as [54]: $\mu_s(T_l) = \mu_{so}(\frac{T_l}{T_o})^{-2}$, where μ_{so} is the electron surface mobility at ambient temperature, T_o: $\mu_{so} = \frac{\mu_0}{1+\theta(V_G - V_T)}$. θ is the surface mobility coefficient. From Eq. (4.72), one obtains

$$E^2 = \frac{3k}{2q} \cdot \frac{1+\alpha\frac{k}{q}(T_n - T_l)}{\mu_s(T_l)} \cdot \frac{T_n - T_l}{\tau_\epsilon} - \frac{5kE}{2q} \cdot \frac{dT_n}{dy}. \tag{4.73}$$

In order to solve the above differential equation, the electric field distribution in the device should be known. The drain current characteristics of a deep submicron NMOS device is divided into the triode region ($V_D < V_{DSAT}$) and the saturation region ($V_D > V_{DSAT}$).

4.7.1 Triode region ($V_D < V_{DSAT}$)

In the triode region, the lateral electric field distribution in the channel region is assumed to be linear: $E(y) = E_0 + ay$, where E_0 is the electric field at the source end: $E_0 = -\frac{\eta_1 V_D}{L_{\text{eff}}}$, where L_{eff} is the effective channel length, and η_1 is a fitting parameter. a is the slope of the electric field: $a = -\frac{2(1-\eta_1)V_D}{L_{\text{eff}}^2}$. Using a linear approximation formula: $T_n = A'y + B'$, from Eq. (4.73) with boundary conditions: at the source end the electron temperature is ambient temperature, one obtains:

$$(E_0 + ay)^2 = \frac{3k}{2q} \cdot \frac{1+\alpha\frac{k}{q}(A'y + B' - T_l)}{\mu_s(T_l)} \cdot \frac{A'y + B' - T_l}{\tau_\epsilon} - \frac{5k(E_0 + ay)}{2q}A'. \tag{4.74}$$

By equating the coefficient of the y^2 terms in Eq. (4.74), one obtains: $A' = -\frac{2qav_{\text{sat}}\tau_\epsilon}{3k}$. From Eq. (4.74) and considering the location at $y = L_{eff}$, one obtains: $B' = T_l - A'L_{\text{eff}} - \frac{q}{2\alpha k} + \frac{q\sqrt{1-\frac{20\mu_s^2(T_l)\tau_\epsilon}{3v_{\text{sat}}}(E_0+aL_{\text{eff}})+\frac{4\mu_s^2(T_l)}{v_{\text{sat}}^2}(E_0+aL_{\text{eff}})^2}}{2\alpha k}$. The drain current is expressed as:

$$I_D = \mu_{\text{eff}} C_{ox} \frac{W}{L_{\text{eff}}}[(V_G - V_{\text{T}})V_D - a_0 V_D^2], \tag{4.75}$$

where C_{ox} is the unit area gate oxide capacitance ($C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$), $a_0 = \frac{1}{2}(\frac{C_b+C_{ox}}{C_{ox}})$ [70], C_b is the silicon thin-film capacitance ($C_b = \frac{\epsilon_{si}}{t_{si}}$), V_T is the threshold voltage, and μ_{eff} is the effective electron mobility: $\mu_{\text{eff}} = \frac{L_{\text{eff}}}{\int_0^{L_{\text{eff}}} \frac{1}{\mu_n} dy}$. Using a simplified approach by taking values at both ends – at the source end ($\mu_n(0)$) and at the drain end ($\mu_n(L_{eff})$), the effective electron mobility becomes: $\mu_{\text{eff}} = \frac{L_{\text{eff}}}{\frac{L_{\text{eff}}}{2}(\frac{1}{\mu_n(0)}+\frac{1}{\mu_n(L_{\text{eff}})})} = \frac{2}{\frac{1}{\mu_n(0)}+\frac{1}{\mu_n(L_{\text{eff}})}}$, where the electron mobility at the source end is $\mu_n(0) = \mu_s(T_l)$. Therefore, the electron mobility at the drain end becomes:

$$\mu_n(L_{\text{eff}}) = \frac{\mu_s(T_l)}{1+\alpha\frac{k}{q}(T_n(L_{\text{eff}})-T_l)} = \frac{2\mu_s(T_l)}{1+\sqrt{1-\frac{20a\mu_s^2(T_l)\tau_\epsilon}{3v_{\text{sat}}}(E_0+aL_{\text{eff}})+\frac{4\mu_s^2(T_l)}{v_{\text{sat}}^2}(E_0+aL_{\text{eff}})^2}}. \tag{4.76}$$

Hence, the effective electron mobility becomes:

$$\mu_{\text{eff}} = \frac{4\mu_s(T_l)}{3+\sqrt{1+K\mu_s^2(T_l)}}, \tag{4.77}$$

where $K = (-\frac{40}{3}\frac{(1-\eta_1)(2-\eta_1)\tau_\epsilon}{v_{sat}L_{eff}^3}+\frac{4(2-\eta_1)^2}{v_{sat}^2L_{eff}^2})V_D^2$. From Eq. (4.77), as the effective channel length is in the order of $v_{sat}\tau_\epsilon$, the electron temperature effect cannot be neglected. Using Taylor's approximation formula, from Eq. (4.77), the effective mobility becomes:

$$\begin{aligned}
\mu_{eff} &\cong AT_l^2 + BT_l + C, \qquad (4.78)\\
\mu_{eff}|_{T_l=T_o} &= \frac{4\mu_{so}}{3+\sqrt{1+K\mu_{so}^2}},\\
\frac{\partial\mu_{eff}}{\partial T_l}|_{T_l=T_o} &= \frac{-8(3+(1+K\mu_{so}^2)^{\frac{-1}{2}})}{(3+(1+K\mu_{so}^2)^{\frac{1}{2}})^2}\frac{\mu_{so}}{T_o},\\
\frac{\partial^2\mu_{eff}}{\partial T_l^2}|_{T_l=T_o} &= \frac{-8\mu_{so}}{T_o^2(3+\sqrt{1+K\mu_{so}^2})^2}(3+\frac{1+3K\mu_{so}^2}{(1+K\mu_{so}^2)^{\frac{3}{2}}}+4\frac{(3+(1+K\mu_{so}^2)^{\frac{-1}{2}})^2}{3+(1+K\mu_{so}^2)^{\frac{1}{2}}}),
\end{aligned}$$

where $A = \frac{1}{2}\frac{\partial^2 \mu_{eff}}{\partial T_l^2}|_{T_l=T_o}$, $B = \frac{\partial \mu_{eff}}{\partial T_l}|_{T_l=T_o} - \frac{\partial^2 \mu_{eff}}{\partial T_l^2}|_{T_l=T_o} T_o$, $C = \mu_{eff}|_{T_l=T_o} - \frac{\partial \mu_{eff}}{\partial T_l}|_{T_l=T_o} T_o +$ $\frac{1}{2}\frac{\partial^2 \mu_{eff}}{\partial T_l^2}|_{T_l=T_o} T_o^2$. In the above equations, the higher order terms in the Taylor's series have been neglected. From Eqs. (4.71)(4.75)(4.78), the lattice temperature in terms of V_D and V_G can be obtained:

$$T_l(V_D, V_G) = \frac{-E - \sqrt{E^2 - 4DF}}{2D}, \tag{4.79}$$

where $D = Af$, $E = Bf - 1$, $F = Cf + T_o$, $f = C_{ox}\frac{W}{L_{eff}}((V_G - V_T)V_D - a_0 V_D^2)V_D R_{th}$. Eqs. (4.75)(4.78)(4.79) are the drain current formula for the ultrathin SOI NMOS device biased in the triode region considering electron and lattice temperatures simultaneously.

4.7.2 Saturation region ($V_D > V_{DSAT}$)

Using a similar approach as in the Refs. [71]-[73], the lateral channel of the NMOS device is divided into two sections — (1) the pre-saturation region and (2) the post-saturation region, separated by the "saturation point"($y = L_{eff} - \Delta L$), where its channel potential is V_{DSAT}. V_{DSAT} is defined as:

$$V_{DSAT} = V_{DSAT1} + V_p - \sqrt{V_{DSAT1}^2 + V_p^2}, \tag{4.80}$$

where V_p is the defined as the V_D when: $\frac{\partial I_D}{\partial V_D} = 0$. V_p is for the long channel case, where pinch-off dominates. The effective mobility formula is too complicated for deriving V_p. Using Taylor's approximation formula with respect to V_D at a reference: $V_D = \frac{V_G - V_T}{2a_0}$ for the square root term in the denominator of Eq. (4.77), one obtains:

$$\mu_{eff} = \frac{4\mu_{sp}}{Q + RV_D}, \tag{4.81}$$

where $\mu_{sp} = \mu_{so}(\frac{T_o}{T_l(V_p, V_G)})^2 \cong \mu_{so}(\frac{T_o}{T_l(\frac{V_G - V_T}{2a_0}, V_G)})^2$, $P = \frac{4(2-\eta_1)^2}{v_{sat}^2 L_{eff}^2} - \frac{40(1-\eta_1)(2-\eta_1)\tau_\epsilon}{3v_{sat}L_{eff}^3}$, $Q = 3 + (1 + P(\frac{V_G - V_T}{2a_0})^2 \mu_{sp}^2)^{\frac{-1}{2}}$, and $R = \frac{P(\frac{V_G - V_T}{2a_0})\mu_{sp}^2}{\sqrt{1 + P(\frac{V_G - V_T}{2a_0})^2 \mu_{sp}^2}}$. Therefore, from Eq. (4.75)(4.81), one obtains: $V_p = \frac{-a_0 Q + \sqrt{a_0^2 Q^2 + a_0 RQ(\frac{V_G - V_T}{2a_0})}}{a_0 R}$. $V_{\rm DSAT1}$ is the drain voltage when the velocity saturation occurs at drain: $-\mu_n(L_{\rm eff})(E_0 + aL_{\rm eff}) = \eta_2 v_{\rm sat}$, where $E_0 = -\eta_1 \frac{V_{\rm DSAT1}}{L_{\rm eff}}$, $a = -\frac{2(1-\eta_1)V_{\rm DSAT1}}{L_{\rm eff}^2}$, $\mu_n(L_{eff})$ is the electron mobility at drain,

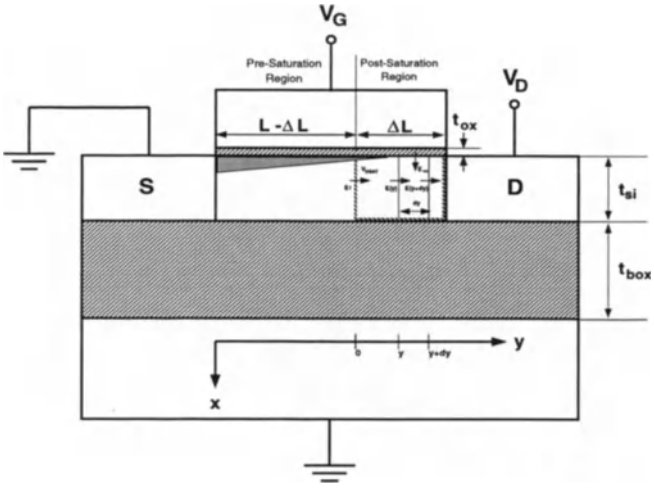


Figure 4.38: Cross section of the deep submicron ultrathin SOI NMOS device under study.

and η_2 is a fitting parameter. From Eq. (4.77), $V_{\rm DSAT1}$ becomes:

$$V_{\rm DSAT1} = \frac{\eta_2 v_{\rm sat} L_{\rm eff}^2}{(2-\eta_1)(1-\eta_2^2)\mu_s(T_l)L_{\rm eff} + \frac{10}{3}(1-\eta_1)\eta_2^2\mu_s(T_l)\tau_\epsilon v_{\rm sat}}. \tag{4.82}$$

As shown in Eq. (4.80), V_{DSAT} is determined by the smaller of V_{DSAT1} and V_p. V_{DSAT1} is determined by the electron velocity saturation behavior in short channel devices. V_p is determined by the pinchoff behavior in long channel devices. In order to be adaptable for both long and short channel cases, V_{DSAT} is determined by the smaller of the two — velocity saturation in short channel devices (V_{DSAT1}) and pinchoff in long channel devices (V_p).

(1)The pre-saturation region

In the pre-saturation region, Eq. (4.75) is the drain current formula except that L_{eff} should be replaced by $L_{eff} - \Delta L$ and V_D replaced by V_{DSAT}.

(2)The post-saturation region

Using a similar approach as in Ref.[74], in the post-saturation region, 2D Gauss' Law has been applied in the Gauss' box area as shown in Fig. 4.38[65]– from a loca-

tion y to a location $y + dy$ in the lateral channel direction and from oxide interface to the top of the buried oxide in the vertical direction. Integrating Gauss' box, one obtains an equation in terms of the potential $V(y)$ in the lateral channel region:

$$-\frac{\epsilon_{ox}}{\epsilon_{si}} \cdot \frac{V_G - V(y)}{t_{ox}} dy - t_{si}E(y) + t_{si}E(y+dy) = -\frac{q(N_A+n)}{\epsilon_{si}} t_{si} dy, \tag{4.83}$$

where N_A is the silicon thin-film doping density, ϵ_{si} is the silicon permittivity, ϵ_{ox} is the oxide permittivity, and n is the electron density. From Eq. (4.83), one obtains:

$$-\frac{\epsilon_{ox}}{\epsilon_{si}} \frac{V_G - V(y)}{t_{ox}} + t_{si}\frac{dE}{dy} = -qt_{si}\frac{N_A+n}{\epsilon_{si}}. \tag{4.84}$$

The boundary condition for Eq. (4.84) is that at the saturation location ($y = 0$):

$$-\frac{\epsilon_{ox}}{\epsilon_{si}} \frac{V_G - V_{\text{DSAT}}}{t_{ox}} + t_{si}a = -qt_{si}\frac{N_A+n}{\epsilon_{si}}. \tag{4.85}$$

From Eqs. (4.84)&(4.85), one obtains a differential equation in terms of the channel potential $V(y)$:

$$\frac{d^2V(y)}{dy^2} = \frac{1}{\lambda^2}(V(y) - V_{\text{DSAT}}) - a, \tag{4.86}$$

where λ is ($\lambda = \sqrt{\frac{\epsilon_{si}t_{si}t_{ox}}{\epsilon_{ox}}}$) [17]. Solving Eq. (4.86) with boundary conditions – at saturation point, the channel potential is V_{DSAT} and the electric field is E_1, the channel potential is:

$$V(y) = V_{\text{DSAT}} + a\lambda^2 + \frac{\lambda(E_1 - a\lambda)}{2} e^{-\frac{y}{\lambda}} - \frac{\lambda(E_1 + a\lambda)}{2} e^{\frac{y}{\lambda}}, \tag{4.87}$$

where $E_1 = -\frac{(2-\eta_1)V_{\text{DSAT}}}{L_{\text{eff}}-\Delta L}$. From Eq. (4.87), considering that at drain the potential is V_D, one obtains: $V_D = V_{\text{DSAT}} + a\lambda^2 + \frac{\lambda(E_1-a\lambda)}{2}e^{-\frac{\Delta L}{\lambda}} - \frac{\lambda(E_1+a\lambda)}{2}e^{\frac{\Delta L}{\lambda}}$, which is a nonlinear function of ΔL. Note that E_1 and a are also a function of ΔL. In order to simplify the equation, assume that $a = -\frac{2(1-\eta_1)V_{\text{DSAT}}}{L_{\text{eff}}^2}$, and $E_1 = -\frac{(2-\eta_1)V_{\text{DSAT}}}{L_{\text{eff}}}$.

ΔL has been obtained:

$$\Delta L = s\lambda \ln\left[\frac{-(V_D - V_{\text{DSAT}} - a\lambda^2) - \sqrt{(V_D - V_{\text{DSAT}} - a\lambda^2)^2 + \lambda^2(E_1^2 - a^2\lambda^2)}}{\lambda(E_1 + a\lambda)}\right], \tag{4.88}$$

where s is a correction factor, which is used to include the influence of ΔL in a and E_1. In addition, s can also be used to compensate for the velocity overshoot

Parameter	Value
W	9.5μm
L_{eff}	0.2μm
R_S	100Ω
V_T	0.25V
s	0.75
t_{ox}	70Å
v_{sat}	8×10^6cm/sec
t_{si}	800Å
η_1	0.5
η_2	0.85
μ_0	$400\text{cm}^2/\text{V} \cdot \text{sec}$
θ	0.32
τ_ϵ	0.2psec
t_{box}	4000Å
K_{ox}	$1.4\text{W/m} \cdot \text{K}$
K_d	$63\text{W/m} \cdot \text{K}$
T_o	300K

Table 4.2: Parameters of the SOI NMOS device under study.

effect, which is neglected in Eq. (4.88). Eqs.(4.75)(4.80)(4.82)(4.88) are the drain current formula for the ultrathin SOI NMOS device considering electron and lattice temperatures except that in Eq. (4.75), L_{eff} should be replaced by $L_{eff} - \Delta L$ and V_D replaced by V_{DSAT}.

The ultrathin SOI NMOS device under study here has an effective channel length of 0.2μm with a 800Å silicon thin-film atop a buried oxide of 4000Å.The gate oxide thickness is 70Å. The threshold voltage of the device is 0.25V. Table 4.2 shows the parameters of the $0.2\mu m$ ultrathin SOI NMOS device under study [67]. Fig. 4.39 shows the I_D versus V_D curves for the ultrathin SOI NMOS device based on the closed-form analytical model[65] (1) considering both the electron and the lattice temperatures (EB+LT), (2) considering the electron temperature and without considering the lattice temperature (EB), (3) considering the lattice temperature and without considering the electron temperature (LT), and the experimental data [67]. As shown in the figure, in the saturation region, at a large drain voltage, the drain current gets small – the negative differential output resistance phenomenon. For a

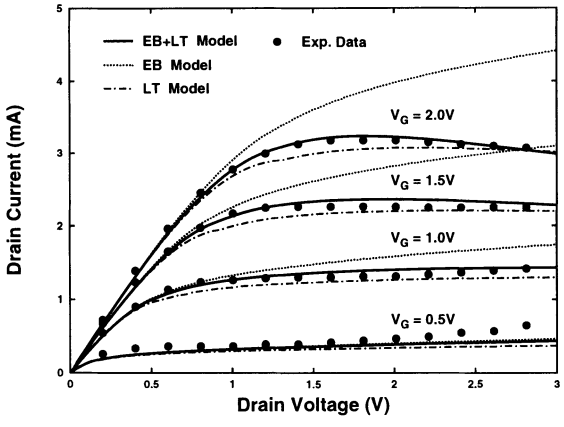


Figure 4.39: The I_D versus V_D curves for the 0.2μm ultrathin SOI NMOS device based on the model (1) considering both the electron and the lattice temperatures (EB+LT), (2) considering the electron temperature and without considering the lattice temperature (EB), (3) considering the lattice temperature and without considering the electron temperature (LT), and the experimental data.

larger V_G, the negative differential output resistance phenomenon is more serious. Without considering lattice temperature, no negative differential resistance can be seen. This verifies that the negative differential resistance phenomenon is indeed due to the self-heating of the lattice.

Fig. 4.40 shows the output conductance versus V_D curves of the 0.2μm ultrathin SOI NMOS device based on the analytical model (1) considering both the electron and the lattice temperature (EB+LT), (2) considering the electron temperature and without considering the lattice temperature (EB), (3) considering the lattice temperature and without considering the electron temperature (LT), and the experimental data[67]. As shown in the figure, the negative differential output conductance can be identified in some region. In addition, in the negative differential output conductance region, a larger gate voltage leads to a more negative differential output conductance. As shown in dotted lines, considering electron temperature only, the negative differential output conductance cannot be modeled. As shown in dashed lines, considering lattice temperature only, the dependence of the gate voltage in the negative differential output conductance region is not vivid. Considering both the electron and the lattice temperatures, the gate voltage dependence in the negative differential output conductance region is noticeable. Compared to two other models,

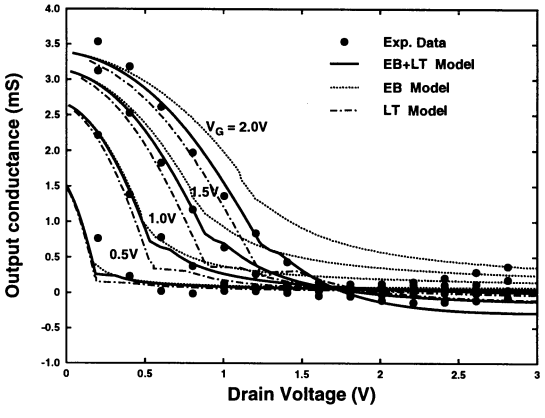


Figure 4.40: Output conductance versus V_D curves of the 0.2μm ultrathin SOI NMOS device based on the model (1) considering both the electron and the lattice temperatures ($EB + LT$), (2) considering the electron temperature and without considering the lattice temperature (EB), (3) considering the lattice temperature and without considering the electron temperature (LT), and the experimental data.

the analytical model results considering both electron and lattice temperature are more accurate. The deviation between the $EB + LT$ model and the experimental data is due to the parasitic bipolar device effects at a high drain voltage[75]. As shown in the figure, the transition between the triode region and the saturation region is smooth and continuous.

For an ultrathin SOI MOS device, power dissipation effect cannot be overlooked due to the existence of the buried oxide. As a result, self-heating of lattice can be serious. Fig. 4.41 shows the lattice temperature versus the drain voltage curves of the ultrathin SOI NMOS device biased at $V_G = 0.5V, 1.0V, 1.5V, 2.0V$ based on the analytical model (1) considering both the electron and the lattice temperatures (EB+LT), (2) considering the lattice temperature and without considering the electron temperature (LT)[65]. As shown in the figure, in the saturation region, the lattice temperature increases rapidly as the drain voltage gets high. For a large V_G, the lattice temperature is high. In the triode region, the lattice temperature is parabolically proportional to the drain voltage. In the saturation region, the lattice temperature is linearly proportional to the drain voltage. The difference in the slope of the lattice temperature between the triode and the saturation regions can be reasoned using Eq. (4.71). From Eq. (4.71), the increase in the lattice temperature can

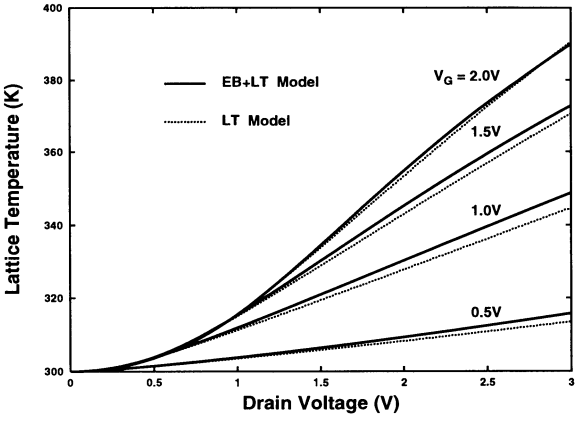


Figure 4.41: The lattice temperature versus the drain voltage curves of the ultrathin SOI NMOS device biased at $V_G = 0.5V, 1.0V, 1.5V, 2.0V$ based on the analytical model (1) considering both the electron and the lattice temperatures (EB+LT), (2) considering the lattice temperature and without considering the electron temperature (LT).

be expressed as: $\Delta T_l = (V_D \Delta I_D + I_D \Delta V_D) R_{th}$. In the triode region, both terms in the above equation are important. On the other hand, in the saturation region, ΔI_D is negligible, therefore, the equation is simplified as: $\Delta T_l \cong I_D \Delta V_D R_{th}$. Hence, in the saturation region, the slope of the lattice temperature is linearly proportional to V_D.

Fig. 4.42 shows the effective electron temperature versus the drain voltage curves of the ultrathin SOI NMOS device biased at $V_G = 0.5V, 1.0V, 1.5V, 2.0V$ based on the analytical model (1) considering both the electron and the lattice temperatures (EB+LT), (2) considering the electron temperature and without considering the lattice temperature (EB). Note that the effective electron temperature is defined as the average temperature in the presaturation region of the ultrathin SOI NMOS device. Without considering lattice temperature, the electron temperature is lower. As shown in Fig. 4.41, considering lattice temperature, although lattice temperature increases by only several tens of degrees, the electron temperature has been raised by over several hundred degrees. Since the effective mobility can be rewritten using the effective electron temperature: $\mu_{eff} = \frac{\mu_s(T_l)}{1+\alpha\frac{k}{q}(\overline{T_n}-T_l)}$, one obtains: $\overline{T_n} - T_l = \frac{q v_{sat}^2 \tau_\varepsilon}{6k}(\frac{\sqrt{1+K\mu_s^2}-1}{\mu_s})$. From Eq. (4.77), $K \propto V_{DSAT}^2$ at satura-

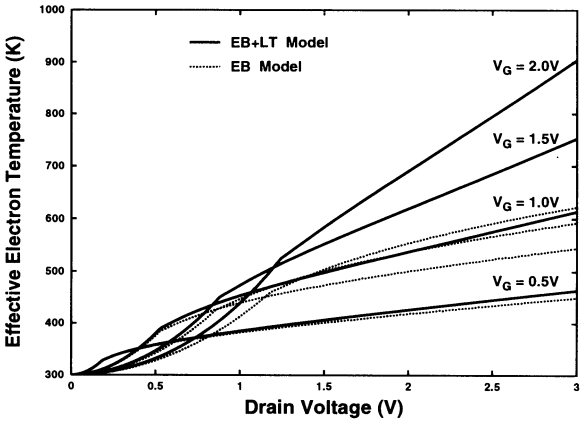


Figure 4.42: The effective electron temperature versus the drain voltage curves of the ultrathin SOI NMOS device biased at $V_G = 0.5V, 1.0V, 1.5V, 2.0V$ based on the analytical model (1) considering both the electron and the lattice temperatures (EB+LT), (2) considering the electron temperature and without considering the lattice temperature (EB).

tion. From Eq. (4.82), for a short channel device, since $V_{DSAT}^2 \propto \frac{1}{\mu_s^2}$, therefore, $\overline{T_n} - T_l \propto \frac{1}{\mu_s}$. Since μ_s is inversely proportional to T_l^2, considering lattice temperature, μ_s is smaller. A smaller μ_s leads to a larger $\overline{T_n} - T_l$. Consequently, considering lattice temperature, $\overline{T_n} - T_l$ is larger.

Fig. 4.43 shows the effective mobility, the effective electron temperature, and the lattice temperature versus the channel length of an ultrathin SOI NMOS device biased in the negative differential output resistance region ($V_G = V_D = 2V$) based on the analytical model (1) considering both the electron and the lattice temperatures (EB+LT), (2) considering the electron temperature and without considering the lattice temperature (EB), (3) considering the lattice temperature and without considering the electron temperature (LT)[65]. With a very short channel ($< 0.2\mu m$), the effective electron temperature increases rapidly inversely proportional to the channel length. Compared to the electron temperature, as shown in the figure, the lattice temperature increases slightly. However, a slight increase in the lattice temperature leads to a substantial decrease in μ_s. In addition, with a short channel, the influence of the effective electron temperature in the effective mobility is also important. Neglecting either the effective electron temperature or the lattice tem-

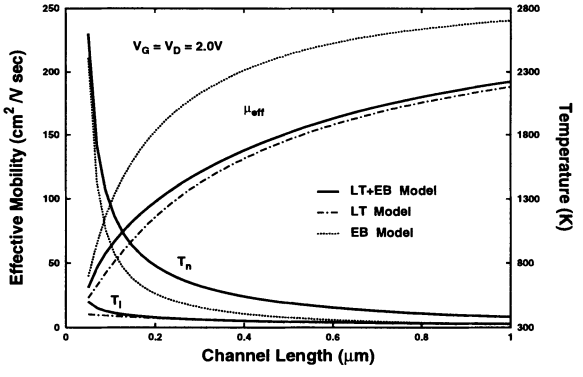


Figure 4.43: The effective mobility, the effective electron temperature, and the lattice temperature versus the channel length of an ultrathin SOI NMOS device biased in the negative differential resistance region ($V_G = V_D = 2V$) based on the analytical model (1) considering both the electron and the lattice temperatures (EB+LT), (2) considering the electron temperature and without considering the lattice temperature (EB), (3) considering the lattice temperature and without considering the electron temperature (LT).

perature may cause substantial deviations.

In this section, an analysis of the drain current for an SOI NMOS device biased in the strong inversion, considering both electron and lattice temperatures simultaneously using a quasi-two-dimensional approach for deep submicron SOI NMOS devices has been described. Based on the analysis, with a channel length of smaller than 0.2μm, both the effective electron temperature and lattice temperature are important in determining the negative differential resistance due to self-heating.

4.8 Source/Drain Resistance Effects

For fully-depleted SOI NMOS devices, a smaller silicon thin-film thickness leads to a smaller second order effects. In a fully-depleted SOI MOS device with a very small silicon thin-film thickness, the source/drain resistance is much larger as compared to the bulk devices. Therefore, the source/drain resistance cannot be overlooked. Fig. 4.44 shows the source/drain resistance versus silicon thin-film thickness of an SOI NMOS device[76]. As shown in the figure, when the silicon thin-film becomes thinner, the source/drain resistance becomes larger, which degrades its current driv-

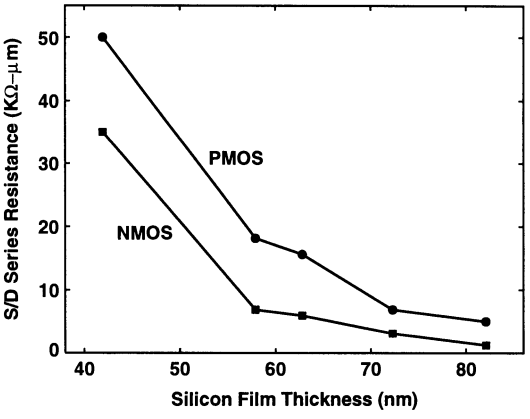


Figure 4.44: Source/drain resistance versus silicon thin-film thickness of an SOI NMOS device.

ing capability in the strong inversion region. Reducing the source/drain resistance has become an important issue for ultra-thin fully-depleted SOI MOS devices. In order to reduce source/drain resistance, an SOI MOS technology with a recessed channel structure as shown in Fig. 4.45 has been used[76]. In the figure, by using a patterned nitride layer, local oxidation has been used to reduce the silicon thin-film thickness in some regions in the silicon thin-film—the thickness of the silicon thin-film in the source/drain region is still large. Therefore, source/drain resistance is not too large. Using the recessed channel structure, the drain current has been improved substantially.

Source/drain resistance can be improved by using the self-aligned silicide (salicide) technique for the ultra-thin SOI MOS devices as shown in Fig. 4.46[77][78]. After patterning the polysilicon gate, LTO/nitride sidewall spacers are formed. Then, a thin Ti/Co layer is deposited, followed by a two-step RTA (rapid thermal anneal) is used to produce the salicide layer. As shown in the figure, with the salicide structure, the drain current has been substantially improved.

Due to the oxide isolated structure, SOI MOS devices may have two methods in contacting their source/drain region. Fig. 4.47 shows the surface and the lateral contacts to the source/drain region for SOI MOS devices with silicide[79]. As shown in the figure, the source/drain resistance is strongly correlated to the contact structures. When the contact resistance is greater than $1.3 \times 10^{-8} \Omega cm^{-2}$, using the

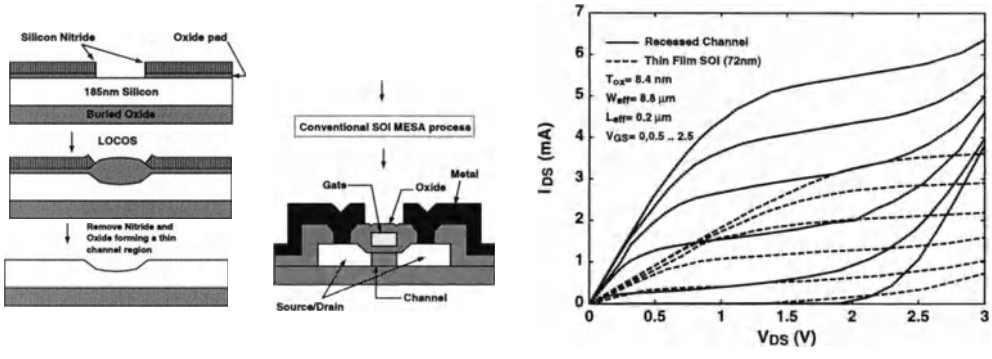


Figure 4.45: Processing steps of an SOI MOS technology with a recessed channel structure.

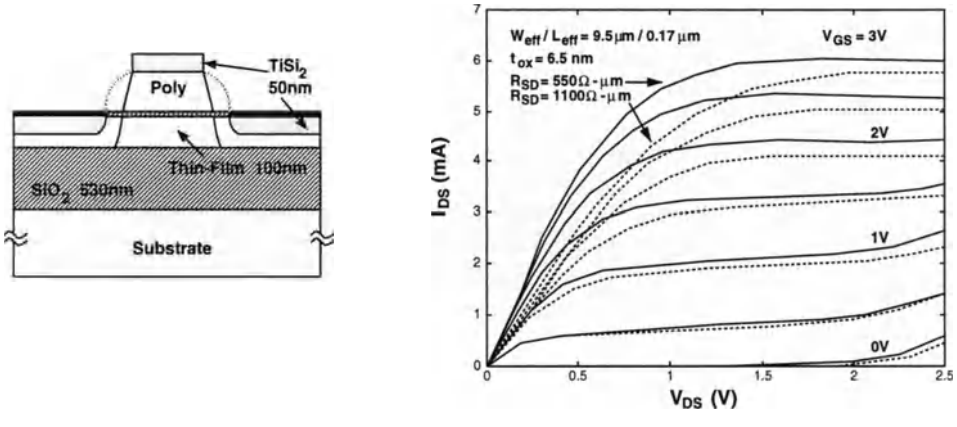


Figure 4.46: Cross section of an ultra-thin SOI MOS device with self-aligned silicide(salicide).

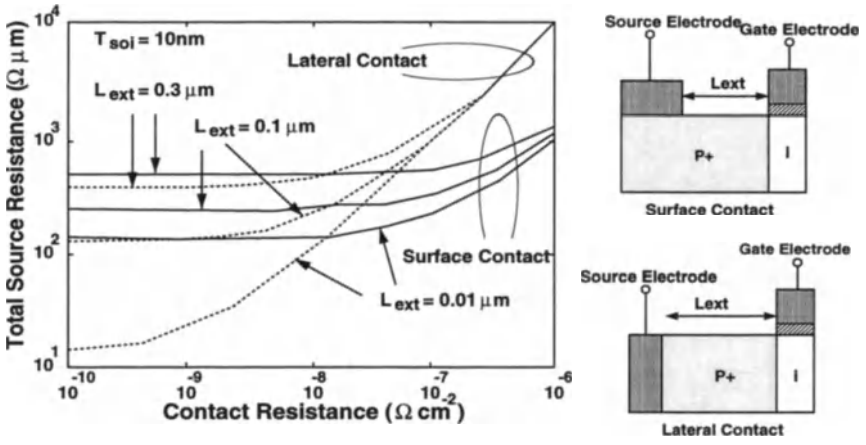


Figure 4.47: Surface and lateral contacts to the source/drain region for SOI MOS devices with silicide.

surface contact, the effective resistance is smaller. When the contact resistance is smaller than $1.3 \times 10^{-8}\Omega\text{cm}^{-2}$, using the lateral contact, its effective resistance is smaller. Therefore, in an advanced fully-depleted SOI MOS technology with silicide, lateral contact to the source/drain region is a good choice. As shown in the figure, when the distance between the source/drain contact and the channel region becomes smaller, its effective resistance becomes smaller.

4.9 Impact Ionization

As described in the previous section, for an SOI NMOS device with a very short channel length, the high electric field effect is very important. Specifically under a high electric field in the MOS device, the carrier temperature can be much higher than the ambient temperature. Conventional drift models are not sufficient to describe the drain current characteristics. Including an energy balance equation, improved models considering the carrier temperature for short-channel NMOS devices have been described [53]. In addition, for SOI CMOS devices biased at a high current level, self-heating of the silicon thin-film seriously degrades their performance. As a result of the elevated lattice temperature, the reduced carrier mobility leads to a negative differential output resistance at a high current level. Considering both the lattice thermal effect and the electron temperature effect, an analytical model for very short-channel SOI MOS devices has been described in the previous section.

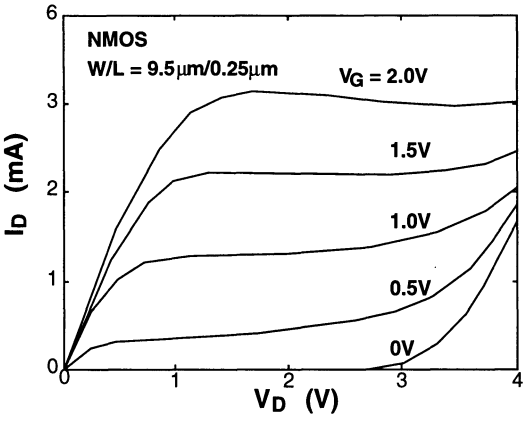


Figure 4.48: Impact ionization effect in an SOI NMOS device with an aspect ratio of W/L = 9.5μm/0.25μm.

Under a high electric field, the impact ionization effect, which may lead to breakdown of the device, is also very important [80]. For SOI MOS devices, due to their parasitic bipolar device structure above the buried oxide, the impact ionization is especially noticeable [81]-[86]. In this section by simultaneously considering impact ionization effect with carrier temperature effect and lattice thermal effect, an analytical drain current model for short-channel ultrathin SOI NMOS devices is described.

For a deep-submicron SOI NMOS device biased at a large V_{DS}, its internal electric field is large. Therefore, the high electric field effects can not be neglected [81]. As shown in Fig. 4.48, when V_{DS} is greater than a certain value, the drain current may increase suddenly. This is caused by impact ionization. As for the bulk CMOS devices, under a high electric field, a moving electron acquires a large amount of energy. Therefore, it may collide with the lattice. As a result, the electron/hole pair may be generated. The generated electron may acquire energy and collide with the lattice. The regeneration repeats itself to a become a positive feedback, hence the drain current increases drastically. Compared with bulk MOS devices, the impact ionization of the SOI MOS devices is different. In this section, the impact ionization of the SOI MOS device is analyzed[81].

As shown in Fig. 4.49[81], for an SOI NMOS device, the drain current due to the impact ionization effects is composed of the channel current (I_{ch}), the impact ionization current (I_h), and the collector current of the parasitic npn bipolar device.

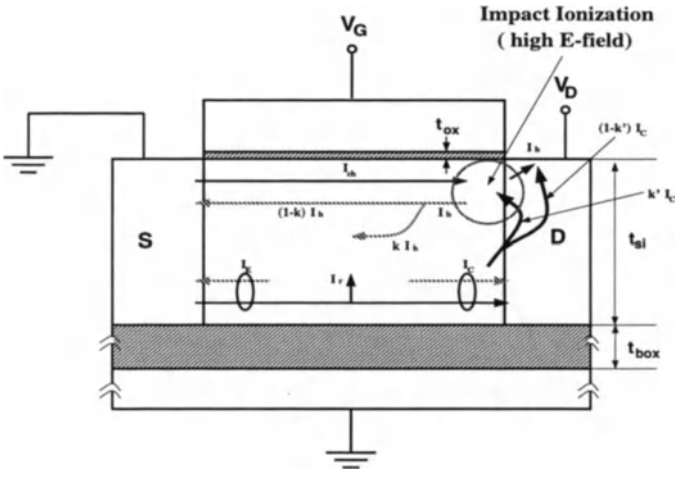


Figure 4.49: The mechanism of impact ionization in an SOI NMOS device.

The channel current has been analyzed in the previous section. In the parasitic npn bipolar device, the collector current is related to the emitter current as:

$$I_C = \alpha_0 I_E + I_{CBO}, \tag{4.89}$$

where I_{CBO} is the leakage current between the base and the collector when the emitter-base junction is open-circuited, and I_{CBO} is a function of the gate voltage. The source current is composed of the channel current (I_{ch}) and a partial portion of the impact ionization current ($(1-K)I_h$) and the emitter current (I_E):

$$I_S = I_{ch} + (1-K)I_h + I_E. \tag{4.90}$$

The impact ionization current is dependent on a portion of the collector current ($K'I_C$) flowing through the high electric field and the channel current:

$$I_h = (M-1)(I_{ch} + K'I_C), \tag{4.91}$$

where M is the multiplication factor[89], which is dependent on the drain voltage:

$$M - 1 = \alpha(V_D - V_{DSAT})exp(-\frac{\beta}{V_D - V_{DSAT}}), \tag{4.92}$$

where α and β are process-dependent parameters. From the above equation, at the onset of saturation ($V_D = V_{DSAT}$), M-1=0. By considering that the drain current is

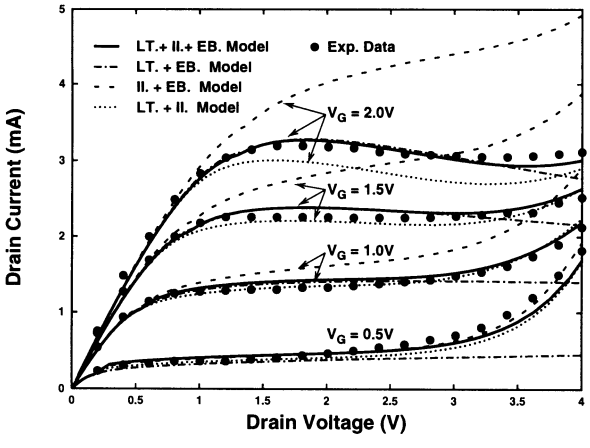


Figure 4.50: IV characteristics of a 0.25μm SOI NMOS device.

equal to the source current ($I_D = I_S$), the emitter current of the parasitic bipolar device and the impact ionization current become:

$$I_E = \frac{K(M-1)}{1-(1+KK'(M-1))\alpha_0} I_{ch} + \frac{1+KK'(M-1)}{1-(1+KK'(M-1))\alpha_0} I_{CBO}, \quad (4.93)$$

$$I_h = (M-1)\left(\frac{1-\alpha_0}{1-(1+KK'(M-1))\alpha_0} I_{ch} + \frac{K'}{1-(1+KK'(M-1))\alpha_0} I_{CBO}\right).$$

Since the drain current is compased of I_h and $(1-K')I_C$, the drain current is:

$$I_D = GI_{ch} + HI_{CBO}, \quad (4.94)$$

where $G = 1 + \frac{(M-1)(1-(1-K)\alpha_0)}{1-(1+KK'(M-1))\alpha_0}$, and $H = \frac{1+K'(M-1)}{1-(1+KK'(M-1))\alpha_0}$. Based on the above model considering the lattice temperature and the electron temperature as described in the last section, Fig. 4.50 shows the IV characteristics of a 0.25μm SOI NMOS device[81]. From Fig. 4.50, when V_{DS} is large, there is a kink in the drain current characteristics. When the drain current is small, the kink is produced by the impact ionization and the parasitic npn bipolar device. When the drain current is large, the kink is caused by the lattice temperature effect. Therefore, the kink in the drain current characteristics of an SOI CMOS device is caused by self-heating and the parasitic bipolar device.

The parasitic BJT induced breakdown voltage of an SOI MOS device can be improved using the LDD structure. Fig. 4.51 shows the gate-overlapped LDD structure in an ultra-thin SOI MOS device with a front gate oxide of 150Å, a buried oxide

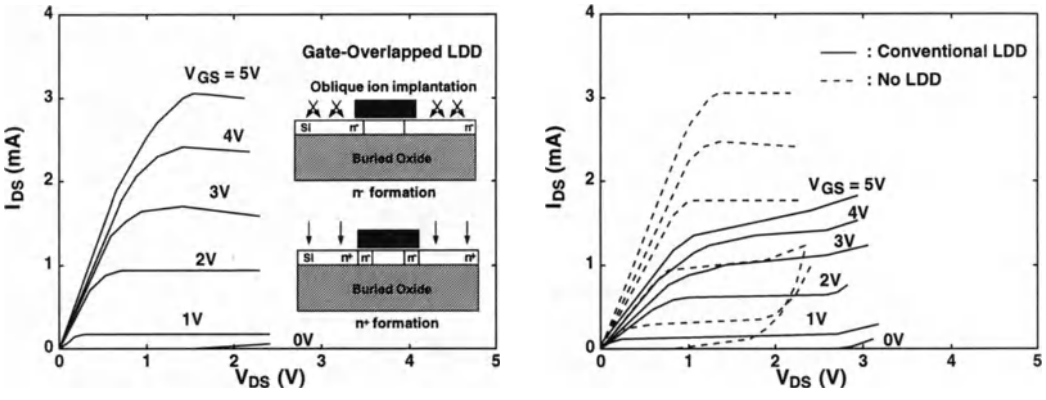


Figure 4.51: An ultra-thin SOI MOS device with a gate-overlapped LDD structure and a front gate oxide of 150Å, a buried oxide of 4600Å, and a silicon thin-film of 800Å.

of 4600Å, and a silicon thin-film of 800Å[87]. The gate-overlapped LDD structure was formed by a phosphorus ion-implant at an energy of 80keV and at an oblique angle of 60 degrees. Using the gate-overlapped LDD structure, the change in the electric field near the drain can be reduced— the impact ionization and the parasitic BJT effect can be lowered. As shown in the figure, without the LDD structure, its breakdown voltage is 2.3V. Using the conventional LDD structure without the overlap between the gate and n^- region, the breakdown voltage has been improved. However, due to the increased parasitic resistance, its drain current becomes smaller. Using the gate-overlapped LDD structure, its breakdown voltage can be improved. In addition, its drain current is not sacrificed.

The parasitic BJT effect also increases the gate-induced-drain-leakage (GIDL) current as shown in Fig. 4.52[88]. As shown in the figure, when V_G is very negative and V_D is positive, although the SOI NMOS device is off, the electric field in the gate-drain overlap region is large. As a result, electrons move from the silicon thin-film to the drain via tunneling from the valence band to the conduction band— GIDL. The holes in the silicon thin-film are amplified by the parasitic BJT— the leakage current is increased. As shown in the figure, when the channel length becomes smaller, the GIDL current is higher because of the parasitic BJT effect. Using the LDD structure, the GIDL current can be suppressed.

In this section, an analytical drain current model considering the impact ion-

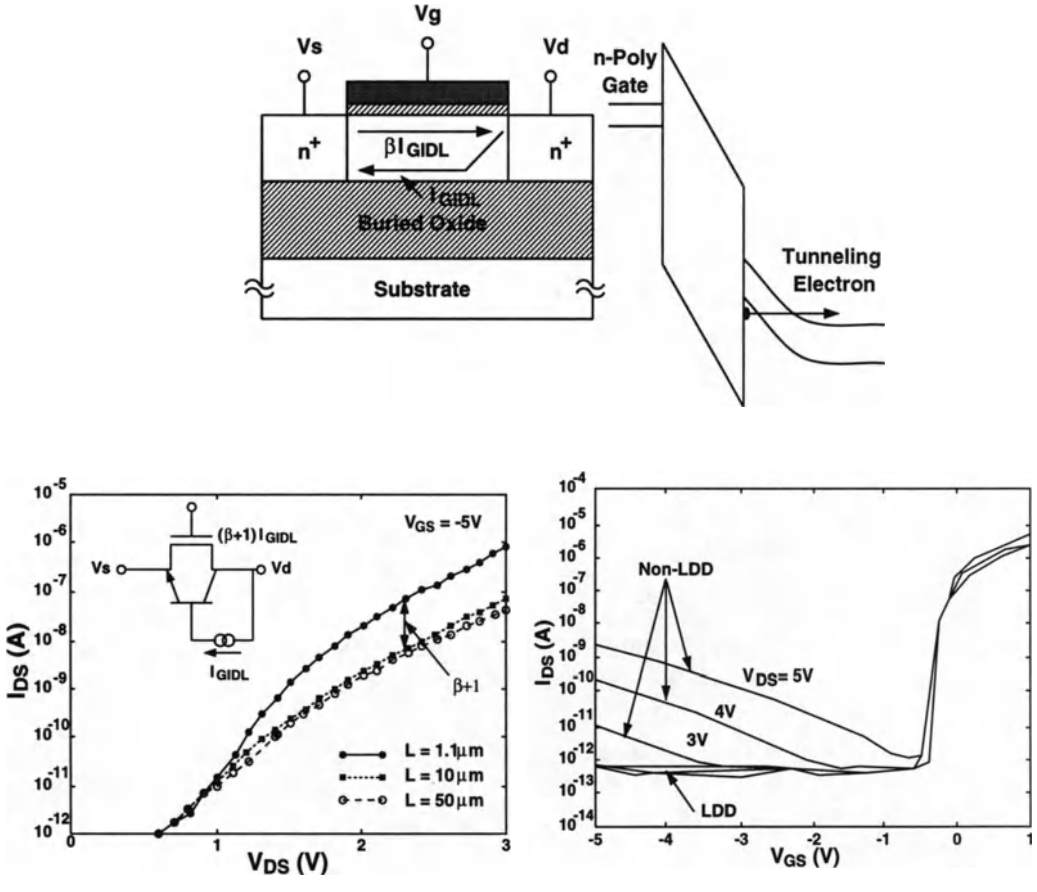


Figure 4.52: Gate-induced-drain-leakage (GIDL) current in an SOI NMOS device.

ization and parasitic BJT effects for short-channel SOI NMOS devices has been described. From the analysis, in the saturation region at a small gate voltage, the impact ionization and parasitic BJT effects are important. At a large gate voltage, lattice thermal effect is important. Finally, the improvement of breakdown voltage and the gate-induced drain leakage using an LDD structure has been described. GIDL can be reduced by the LDD structure— the change in the electric field near the drain can be reduced by the LDD structure.

4.10 Non-Local Effect

Until now, the electron temperature and the lattice temperature effects for SOI CMOS devices have been considered. In addition, the impact ionization and the parasitic BJT effect of a short-channel SOI CMOS have been described. For an SOI MOS device biased under a high electric field, the impact ionization effect, which may lead to breakdown of the device, is important. The impact ionization model described in the previous section is based on the conventional local impact ionization models for bulk MOS devices [80]-[86][89][90]. According to recent studies, in a VLSI MOS or bipolar device biased under a high electric field, the electron energy may not be in the equilibrium state. As a result, non-local effect is also very important [91]-[96]. Following the non-local effect on the breakdown voltage of bipolar devices[97][98], the non-local effect on the ultrathin SOI MOS devices is presented in this section. Here, a double-gate SOI NMOS device is used to describe the non-local effect.

In an NMOS device under an electric field, the ionization coefficient considering the local effect is exponentially related to its electric field [89] as:

$$\alpha(y) = A \cdot exp[\frac{-B}{E(y)}], \tag{4.95}$$

where $E(y)$, which is the electric field, can be expressed as:

$$E(y) = E_0 \cdot exp(\frac{y}{\lambda}). \tag{4.96}$$

Due to the rapid change in the electric field, energy equilibrium between the electrons and the lattice may not be reached. Under this situation, the non-local effect is very important— the ionization coefficient is not only related to the electric field but also dependent on the shape of the electric field, which can be characterized by λ as indicated in Eq. (4.96). From Refs.[91][92], the coefficients A and B are also

Parameter	Value
W	10μm[10]
t_{ox}	110Å[10]
t_{si}	600Å[10]
t_{box}	1.5μm[10]
N_{si}	1.5×10^{15}cm^{-3}[10]
R_S	60Ω[65]
T_o	300K[10]
υ_{sat}	8×10^6cm/sec[65]
θ	0.3[65]
τ_ϵ	0.2psec[65]
η_1	0.5[65]
η_2	1.0[65]
s	0.85[65]
γ	4.4×10^{10}cm^{-2}[91]
B_0	9×10^5V/cm[92]
λ_0	900Å[92]
α_o	0.997[81]
I_{S0}	10A/cm^2[81]
θ_I	1[81]
K	0.95[81]
K′	0.95[81]
λ	317Å(double-gate),448Å(single-gate)[65]

Table 4.3: Parameters of the double-gate ultrathin SOI NMOS device under study.

functions of λ. Therefore, α in Eq. (4.95) can be re-expressed as [99]:

$$\alpha(y) = \gamma\lambda \cdot exp[\frac{-B_0(1 + \frac{\lambda_0}{\lambda})}{E(y)}], \tag{4.97}$$

where γ, B_0 and λ_0 are constants. Eq. (4.97) is the ionization coefficient model considering the non-local impact ionization effect.

Based on the parameters listed in Table 4.3, Fig. 4.53 shows the drain current versus drain voltage curves of (a) the double-gate and (b) the single-gate ultrathin SOI NMOS device with an effective channel length of 0.33μm, a width of $10\mu m$, a thin-oxide thickness of 110Å, and a silicon thin-film thickness of 600Å, based on the analytical models[99] (1) considering lattice temperature and non-local impact ionization, (2) considering lattice temperature and local impact ionization, (3) con-

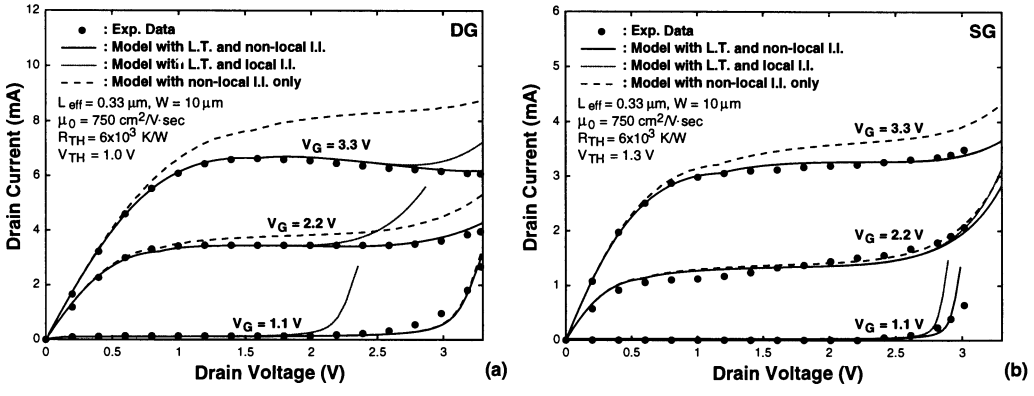


Figure 4.53: The drain current versus drain voltage curves of (a) the double-gate and (b) the single-gate ultrathin SOI NMOS devices with an effective channel length of $0.33\mu m$, a width of $10\mu m$, a thin-oxide thickness of 110Å, and a silicon thin-film thickness of 600Å, based on the analytical models (1) considering lattice temperature and non-local impact ionization, (2) considering lattice temperature and local impact ionization, (3) considering non-local impact ionization and without considering lattice temperature, and the experimental data. The thermal resistance is 6×10^3K/W. The threshold voltage is 1.0V for the double-gate device and 1.3V for the single-gate device.

sidering non-local impact ionization and without considering lattice temperature, and the experimental data [10]. The thermal resistance is 6×10^3K/W. The threshold voltage is 1.0V for the double-gate device and 1.3V for the single-gate device. As shown in the figure, the drain current of the double-gate device is much higher than that of the single-gate device. For both the double-gate and the single-gate devices, at a small V_G, as the drain voltage exceeds a certain value, the drain current increases rapidly due to the impact ionization in the high electric-field region. The generated holes as a result of impact ionization in the high electric-field region activate the parasitic bipolar device in the silicon thin-film. At a larger gate voltage, the rapid increase in the drain current occurs at a higher drain voltage. As the gate voltage increases further, this rapid increase in drain current disappears. At a high gate voltage, the lattice temperature in the silicon thin-film can be high. As a result, the electron mobility can be degraded. A region with a negative differential output conductance can be identified. In addition, the negative differential output resistance of the double-gate device due to self-heating is more serious—the difference between the double-gate cases with and without considering thermal

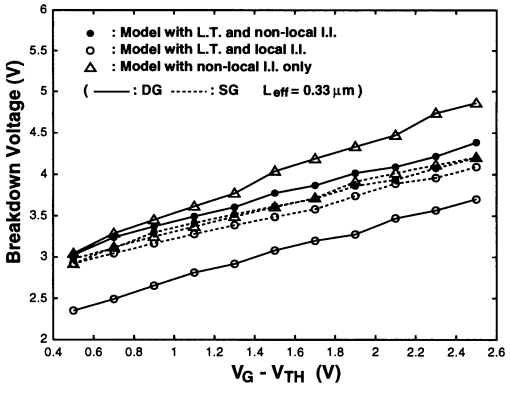


Figure 4.54: Breakdown voltage versus $V_G - V_{TH}$ of the double-gate and the single-gate ultrathin SOI NMOS devices with an effective channel length of 0.33μm based on the analytical models (1) considering lattice temperature and non-local impact ionization, (2) considering lattice temperature and local impact ionization, (3) considering non-local impact ionization and without considering lattice temperature.

effect is larger. However, channel length modulation of the double-gate device is less. For the double-gate device, considering the local impact ionization effect, the breakdown phenomenon occurs at a much smaller drain voltage. Only with considering the non-local impact ionization, the breakdown voltage of the double-gate device can be more accurately modeled. On the other hand, for the single-gate device, the necessity of the non-local effect is not so much as for the double-gate device.

As shown in Figs. 4.53(a)&(b), for the single-gate device, whether the non-local effect model is used or not does not seriously affect the accuracy in modeling the impact ionization phenomenon. However, for the double-gate device, the non-local effect model is necessary for accurately modeling the impact ionization. This can be understood by considering the electric-field profile in the post-saturation region. For the double-gate device, λ is smaller. The gradient of the electric field near the drain of the double-gate device is larger. As a result, the non-local effect is more influential in the double-gate device. Fig. 4.54 shows the breakdown voltage versus $V_G - V_{TH}$ of the double-gate and the single-gate ultrathin SOI NMOS devices with an effective channel length of 0.33μm based on the analytical models (1) considering lattice temperature and non-local impact ionization, (2) considering lattice temperature and local impact ionization, (3) considering non-local impact ionization and without considering lattice temperature[99]. As shown in the figure, the breakdown voltage

is a function of the gate voltage. As the gate voltage is small, its breakdown voltage is small— impact ionization is influential. As the gate voltage is large, its breakdown voltage becomes large. For the single-gate devices, among the three model results, their breakdown voltages are similar. However, for the double-gate device, the breakdown voltage is much more sensitive to the model adopted. Using the local impact ionization effect model, the breakdown voltage is the smallest— impact ionization has been overestimated. Considering the non-local impact ionization effect, the breakdown voltage is at least 0.7V higher as compared to the local impact ionization model result. Including the lattice temperature model in the non-local impact ionization model, the breakdown voltage is worse. From this figure, for the double-gate device, both the lattice temperature model and the non-local impact ionization model are important in characterizing the drain current behavior.

4.11 Summary

In this chapter, analysis of device performance for SOI CMOS devices has been done. Starting from the back gate bias effect, considering the small-geometry effect including the short-channel effect and the narrow-channel effect, a small-geometry threshold voltage model has been described for the SOI CMOS devices. Then, considering the impurity scattering effect, the surface scattering effect, and the electron temperature and the lattice temperature effects, a comprehensive mobility model has been described by simultaneously considering the energy transport equation. In addition, the velocity overshoot phenomenon of SOI CMOS devices has also been described. Then, analysis of the subthreshold current and the strong inversion current of SOI CMOS devices has also been reported by including the lattice temperature and the electron temperature effects. Negative differential output resistance of the SOI CMOS devices has been explained as due to self-heating effects. Then the breakdown of the SOI CMOS devices has been analyzed using the impact ionization, the parasitic BJT effects model, and the non-local effects. In the following chapter, capacitance and transient behavior of inversion-mode and accumulation-mode SOI CMOS devices will be described. In addition, sensitivity, partially-depleted SOI CMOS devices, hot electron effects, temperature effect, radiation hardness, and noise will be reported.

References

[1] H.-K. Lim and J. G. Fossum, "Threshold Voltage of Thin-Film Silicon-On-Insulator (SOI) MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 30, No. 10, pp.1244-1251, Oct. 1983.

[2] K. K. Young, "Analysis of Conduction in Fully Depleted SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 3, pp.504-506, March 1989.

[3] E. R. Worley, "Theory of the Fully Depleted SOS/MOS Transistor," *Sol. St. Elec.*, Vol. 23, pp.1107-1111, 1980.

[4] J. B. McKitterick, and A. L. Caviglia, "An Analytical Model for Thin SOI Transistors," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 6, pp.1133-1138, June 1989.

[5] F. Balestra, M. Benachir, J. Brini and G. Ghibaudo, "Analytical Models of Subthreshold Swing and Threshold Voltage for Thin- and Ultra-Thin-Film SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 37, No. 11, pp.2303-2311, Nov. 1990.

[6] Y. Inoue, Y. Yamaguchi, T. Yamaguchi, J. Takahashi, T. Iwamatsu, T. Wada, Y. Nishimura, T. Nishimura and N. Tsubouchi, "Selection of Operation Mode on SOI/MOSFET's for High-Resistivity Load Static Memory Cell," *SOI Conf. Dig.*, pp. 94-95, 1993.

[7] M. Haond and M. Tack, "Rapid Electrical Measurements of Back Oxide and Silicon Film Thickness in an SOI CMOS Process," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 3, pp. 674-676, March 1991.

[8] J.-H. Sim and J. B. Kuo, "An Analytical Back-Gate Bias Effect Model for Ultrathin SOI CMOS Devices," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 4, pp. 755-765, Apr. 1993.

[9] K. Hashimoto, T. I. Kamins, K. M. Cham and S. Y. Chiang, "Characteristics of Submicrometer CMOS Transistors in Implanted-Buried-Oxide SOI Films," *IEDM Dig.*, pp. 672-675, 1985.

[10] T. Tanaka, H. Horie, S. Ando, and S. Hijiya, "Analysis of P^+ Poly Si Double-Gate Thin-Film SOI MOSFETS," *IEDM Dig.*, pp.683-686, 1991.

[11] J.-P. Colinge, M.-H. Gao, A. Romano, H. Maes, and C. Claeys, "Silicon-on-Insulator "Gate-All-Around" MOS Device," *SOI Conf. Dig.*, pp.137-138, 1990.

[12] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-Gate Silicon-on-Insulator Transistor with Volume Inversion: A New Device with Greatly Enhanced Performance," *IEEE Elec. Dev. Let.*, Vol. 8, No. 9, pp. 410-412, Sept. 1987.

[13] S.-S. Chen and J. B. Kuo, "Deep Submicrometer Double-Gate Fully-Depleted SOI PMOS Devices: A Concise Short-Channel Effect Threshold Voltage Model using A Quasi-2D Approach," *IEEE Trans. Elec. Dev.*, Vol. 43, No. 9, pp. 1387-1393, Sept. 1996.

[14] L. D. Yau, "A Simple Theory to Predict the Threshold Voltage of Short-Channel IGFETs," *Sol. St. Elec.*, Vol. 17, pp. 1059-1063, 1974.

[15] K. K. Young, "Short-Channel Effect in Fully Depleted SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 2, pp. 399-402, Feb. 1989.

[16] V. Aggarwal, M. K. Khanna, R. Sood, S. Haldar and R. S. Gupta, "Analytical Two-Dimensional Modeling for Potential Distribution and Threshold Voltage of the Short-Channel Fully Depleted SOI (Silicon-on-Insulator) MOSFETs," *Sol. St. Elec.*, Vol. 37, No. 8, pp. 1537-1542, Aug. 1994.

[17] R.-H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From Bulk to SOI to Bulk," *IEEE Trans. Elec. Dev.*, Vol. 39, No. 7, pp. 1704-1710, July 1992.

[18] J. B. Kuo, Y. G. Chen and K. W. Su, "Sidewall-Related Narrow Channel Effect in Mesa-Isolated Fully-Depleted Ultra-Thin SOI NMOS Devices," *IEEE Elec. Dev. Let.* Vol. 16, No. 9., pp. 379-381, Sept. 1995.

[19] S. R. Banna, P. C. H. Chan, P. K. Ko, C. T. Nguyen, and M. Chan, "Threshold Voltage Model for Deep-Submicrometer Fully Depleted SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 11, pp. 1949-1955, Nov. 1995.

[20] Y. Omura, "A Simple Model for Short-Channel Effects of a Buried-Channel MOSFET on the Buried Insulator," *IEEE Trans. Elec. Dev.*, Vol. 29, No. 11, pp. 1749-1755, Nov. 1982.

[21] L. T. Su, J. B. Jacobs, J. E. Chung, and D. A. Antoniadis, "Deep-Submicrometer Channel Design in Silicon-on-Insulator (SOI) MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 15, No. 9, pp. 366-369, Sept. 1994.

[22] K. Suzuki, A. Satoh and T. Sugii, "Counter Doping into Uniformly and Heavily Doped Channel Region of Sub 0.1μm SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 17, No. 1, pp. 1-3, Jan. 1996.

[23] M. P. Brassington, A. G. Lewis, and S. L. Partridge, "A Comparison of Fine-Dimension Silicon-On-Sapphire and Bulk-Silicon Complementary MOS Devices and Circuits," *IEEE Trans. Elec. Dev.*, Vol. 32, No. 9, pp. 1858-1867, Sept. 1985.

[24] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling Theory for Double-Gate SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 12, pp. 2326-2329, Dec. 1993.

[25] T. Toyabe and S. Asai, "Analytical Models of Threshold Voltage and Breakdown Voltage of Short-Channel MOSFET's Derived from Two-Dimensional Analysis," *IEEE J. Sol. St. Ckt*, Vol. 14, No. 2, pp. 375-383, Apr., 1979.

[26] T. Elewa, B. Kleveland, S. Cristoloveanu, B. Boukriss, and A. Chovet, "Detailed Analysis of Edge Effects in SIMOX-MOS Transistors," *IEEE Trans. Elec. Dev.*, Vol. 39, No. 4, pp. 874-882, Apr. 1992.

[27] S. N. Lee, R. A. Kjar, and G. Kinoshita, "Island-Edge Effects in C-MOS/SOS Transistors," *IEEE Trans. Elec. Dev.*, Vol. 25, No. 8, pp. 971-978, Aug. 1978.

[28] G. Merckel, "A Simple Model of the Threshold Voltage of Short and Narrow Channel MOSFETs," *Sol. St. Elec.*, Vol. 23, No. 12, pp. 1207-1213, Dec. 1980.

[29] T. Yamaguchi and S. Morimoto, "Analytical Model and Characterization of Small Geometry MOSFETs," *IEEE Trans. Elec. Dev.*, Vol. 30, No. 6, pp. 559-566, June 1983.

[30] L. A. Akers, M. M. E. Beguwala, and F. Z. Custode, "A Model of a Narrow-Width MOSFET Including Tapered Oxide and Doping Encroachment," *IEEE Trans. Elec. Dev.*, Vol. 28, No. 12, pp. 1490-1495, Dec. 1981.

[31] T. Elewa, B. Kleveland, B. Boukriss, T. Ouisse, A. Chovet, S. Cristoloveanu, and J. Davis, "Novel Investigation of Edge Effects in SIMOX Transistors," *SOI Conf. Dig.*, pp. 35-36, 1989.

[32] M. Haond, "Lateral Isolation in SOI CMOS Technology," *SOI Conf. Dig.*, pp.117-118, 1990.

[33] K. W. Su and J. B. Kuo, "Analytical Threshold Voltage Formula Including Narrow-Channel Effects for VLSI Mesa-Isolated Fully Depleted Ultrathin Silicon-on-Insulator N-Channel Metal-Oxide-Silicon Devices," *Jpn. J. Appl. Phy.*, Vol. 34, No. 8A, pp. 4010-4019, Aug. 1995.

[34] K. W. Su and J. B. Kuo, "Modeling Narrow-Channel Effect in VLSI Mesa-Isolated SOI MOS Devices using a Quasi-Two-Dimensional Approach," *Sol. St. Elec.*, Vol. 39, No. 9, pp. 1321-1329, Sept. 1996.

[35] P. Francis, A. Terao, D. Flandre, and F. Van de Wiele, "Modeling of Ultrathin Double-Gate NMOS/SOI Transistors " *IEEE Trans. Elec. Dev.*, Vol. 41, No. 5, pp. 715-720, May 1994.

[36] Y. Hu, T. Houston, R. Rajgopal, K. Joyner and C. Teng, "Isolation Techniques for 256MBit SOI DRAM Application," *SOI Conf. Dig.*, pp. 26-27, 1995.

[37] K. Suma, T. Tsuruda, H. Hidaka, T. Eimori, T. Oashi, Y. Yamaguchi, T. Iwamatsu, M. Hirose, F. Morishita, K. Arimoto, K. Fujishima, Y. Inoue, T. Nishimura and T. Yoshihara, "An SOI-DRAM with Wide Operating Voltage Range by CMOS/SIMOX Technology," *IEEE J. Sol. St. Ckt*, Vol. 29, No. 11, pp. 1323-1328, Nov. 1994.

[38] D. Hisamoto, S. Kimura, T. Kaga, Y. Nakagome, M. Isoda, T. Nishida and E. Takeda, "A New Stacked Cell Structure for Giga-bit DRAMs using Vertical Ultra-Thin SOI (DELTA) MOSFETs," *IEDM Dig.*, pp. 959-961, 1991.

[39] K. Suma, T. Tsuruda, H. Hidaka, T. Eimori, T. Oashi, Y. Yamaguchi, T. Iwamatsu, M. Hirose, K. Fujishima, Y. Inoue, T. Nishimura, and T. Yoshihara, "An SOI-DRAM with Wide Operating Range by CMOS/SIMOX Technology," *ISSCC Dig.*, pp. 138-139, 1994.

[40] P. J. VanDerVoorn and J. P. Krusius, "Inversion Channel Edge in Trench-Isolated Sub-1/4-μm MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 43, No. 8, pp. 1274-1280, Aug. 1996.

[41] K. K. Hsueh, J. J. Sanchez, T. A. Demassa and L. A. Akers, "Inverse-Narrow-Width Effects and Small-Geometry MOSFET Threshold Voltage Model," *IEEE Trans. Elec. Dev.*, Vol. 35, No. 3, pp. 325-338, Mar. 1988.

[42] K. Shibahara, H. Mori, S. Ohnishi, R. Oikawa, K. Nakajima, Y. Kojima, H. Yamashita, K. Itoh, S. Kamiyama, H. Watanabe, T. Hamada and K. Koyama, "1GDRAM Cell with Diagonal Bit-Line(DBL) Configuration and Edge Operation MOS(EOS) FET," *IEDM Dig.*, pp. 639-642, 1994.

[43] S. Geissler, B. Porth, J. Lasky, J. Johnson and S. Voldman, "A New Three-Dimensional MOSFET Gate-Induced Drain Leakage Effect in Narrow Deep Submicron Devices," *IEDM Dig.*, pp. 839-842, 1991.

[44] N. Shigyo and R. Dang, "Analysis of an Anomalous Subthreshold Current in a Fully Recessed Oxide MOSFET Using a Three-Dimensional Device Simulator," *IEEE Trans. Elec. Dev.*, Vol. 32, No. 2, pp. 441-445, Feb. 1985.

[45] K. W. Su and J. B. Kuo, "Analytical Threshold Voltage Model Considering Small-Geometry Effects for VLSI Mesa-Isolated Fully-Depleted Ultrathin SOI NMOS Devices using a Quasi-3D Approach," *Private Communication.*

[46] M. Yoshimi, M. Terauchi, A. Murakoshi, M. Takahashi, K. Matsuzawa, N. Shigyo and Y. Ushiku, "Technology Trends of Silicon-On-Insulator - Its Advantages and Problems to be Solved -," *IEDM Dig.*, pp. 429-432, 1994.

[47] J. Wang, N. Kistler, J. Woo and C. R. Viswanathan, "Mobility-Field Behavior of Fully Depleted SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 15, No. 4, pp.117-119, Apr. 1994.

[48] J.-H. Choi, Y-J. Park and H.-S. Min, "Electron Mobility Behavior in Extremely Thin SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 16, No. 11, pp. 527-529, Nov. 1995.

[49] Y. P. Tsividis, "Operation and Modeling of the MOS Transistor," *McGraw-Hill: New York*, p. 146, 1987.

[50] Y. Omura, K. Kurihara, Y. Takahashi, T. Ishiyama, Y. Nakajima, and K. Izumi, "50-nm Channel nMOSFET/SIMOX with an Ultrathin 2- or 6-nm Thick Silicon Layer and Their Significant Features of Operations," *IEEE Trans. Elec. Dev.*, Vol. 18, No. 5, pp. 190-193, May 1997.

[51] K. Ohuchi, R. Ohba, H. Nhyama, K. Nakajima and T. Mizuno, "A High-Performance 0.05μm SOI MOSFET: Possibility of Velocity Overshoot," *Jpn. J. Appl. Phys.*, Vol. 35, No. 2B, pp. 960-964, Feb. 1996.

[52] B. Meinerzhagen and W. L. Engl, "The Influence of the Thermal Equilibrium Approximation on the Accuracy of Classical Two-Dimensional Numerical Modeling of Silicon Submicrometer MOS Transistors," *IEEE Trans. Elec. Dev.*, Vol. 35, No. 5, pp. 689-697, May 1988.

[53] S.-Y. Ma and J. B. Kuo, "Concise Analytical Model for Deep Submicron N-Channel Metal-Oxide-Semiconductor Devices with Consideration of Energy Trnasport," *Jpn. J. Appl. Phys.*, Vol. 33, No. 1B, pp. 550-553, Jan. 1994.

[54] D. Sharma, J. Gautier, and G. Merckel, "Negative Dynamic Resistance in MOS Devices," *IEEE J. Sol. St. Ckt*, Vol. 13, No. 3, pp. 378-380, June 1978.

[55] G. Baccarani and M. R. Wordeman, "An Investigation of Steady-State Velocity Overshoot in Silicon," *Sol. St. Elec.*, Vol. 28, No. 4, pp. 407-416, Apr. 1985.

[56] R. Stratton, "Diffusion of Hot and Cold Electrons in Semiconductor Barriers," *Phys. Rev.*, Vol. 126, No. 6, pp. 2002-2014, June 15, 1962.

[57] S. Y. Chou, D. A. Antoniadis, and H. I. Smith, "Observation of Electron Velocity Overshoot in Sub-100-nm-Channel MOSFET's in Silicon," *IEEE Elec. Dev. Let.*, Vol. 6, No. 12, pp. 665-667, Dec. 1985.

[58] T. Mizuno and R. Ohba, "Experimental Study of Carrier Velocity Overshoot in Sub-0.1μm Devices– Physical Limitation of MOS Structures," *IEDM Dig.*, pp. 109-112, 1996.

[59] J.-P. Colinge, "Subthreshold Slope of Thin-Film SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 7, No. 4, pp. 244-246, Apr. 1986.

[60] H.-O. Joachim, Y. Yamaguchi, K. Ishikawa, Y. Inoue, and T. Nishimura, "Simulation and Two-Dimensional Analytical Modeling of Subthreshold Slope in Ultrathin-Film SOI MOSFET's Down to 0.1μm Gate Length," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 10, pp. 1812-1817, Oct. 1993.

[61] P. C. Yeh and J. G. Fossum, "Physical Subthreshold MOSFET Modeling Applied to Viable Design of Deep-Submicrometer Fully-Depleted SOI Low-Voltage CMOS Technology," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 9, pp. 1605-1613, Sept. 1995.

[62] Y. C. Tseng, J. Collett, T. O. Vu, J. S. Cable, and J. C. S. Woo, "Analysis of Edge Effects in the Mesa Isolated NMOS SOI," *SOI Conf. Dig.*, pp.90-91, 1996.

[63] P. Antognetti, D. D. Caviglia and E. Profumo, "CAD Model for Threshold and Subthreshold Conduction in MOSFET's," *IEEE J. Sol. St. Ckt*, Vol. 17, No. 3, pp. 454-458, Jun. 1982.

[64] K. W. Su and J. B. Kuo, "Compact Current Model for Mesa-Isolated Fully-Depleted Ultrathin SOI NMOS Devices Considering Sidewall-Related Narrow Channel Effects," *SOI Conf. Dig.*, pp.84-85, 1997.

[65] Y.-G. Chen, S.-Y. Ma, J. B. Kuo, Z. Yu, and R. W. Dutton, "An Analytical Drain Current Model Considering Both Electron and Lattice Temperatures Simultaneously for Deep Submicron Ultrathin SOI NMOS Devices with Self-Heating," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 5, pp. 899-906, May 1995.

[66] L. T. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson, and M. I. Flik, "Measurement and Modeling of Self-Heating in SOI NMOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 1, pp. 69-75, Jan. 1994.

[67] J. Chen, S. Parke, J. King, F. Assaderaghi, P. K. Ko, and C. Hu, "A High Speed SOI Technology with 12ps/18ps Gate Delay Operating at 5V/1.5V," *IEDM Dig.*, pp. 35-38, 1992.

[68] C. Raynaud, O. Faynot, B. Giffard, and J. Gautier, "High Performance Submicron SOI Devices with Silicon Film Thickness Below 50nm," *SOI Conf. Dig.*, pp. 55-56, 1994.

[69] K. Sonoda, K. Taniguchi, and C. Hamaguchi, "Analytical Device Model for Submicrometer MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 12, pp. 2662-2668, Dec. 1991.

[70] H.-K. Lim and J. G. Fossum, "Current-Voltage Characteristics of Thin-Film SOI MOSFET's in Strong Inversion," *IEEE Trans. Elec. Dev.*, Vol. 31, No. 4, pp. 401-408, Apr. 1984.

[71] Y. A. El-Mansy and A. R. Boothroyd, "A Simple Two-Dimensional Model for IGFET Operation in the Saturation Region, " *IEEE Trans. Elec. Dev.*, Vol. 24, No. 3, pp. 254-262, March 1977.

[72] H.-C. Chow, W.-S. Feng, and J. B. Kuo, "An Improved Analytical Short-Channel MOSFET Model Valid in All Regions of Operation for Analog/Digital Circuit Simulation," *IEEE Trans. CAD of IC*, Vol. 11, No.12, pp.1522-1528, Dec. 1992.

[73] K. Mayaram, J. C. Lee and C. Hu, "A Model for the Electric Field in Lightly Doped Drain Structures," *IEEE Trans. Elec. Dev.*, Vol. ED-34, No. 7, pp.1509-1518, July 1987.

[74] N. G. Einspruch and G. Gildenblat, "Advanced MOS Device Physics," *Academic Press: New York*, Vol. 18, p.28, 1989.

[75] J.-Y. Choi and J. G. Fossum, "Analysis and Control of Floating-Body Bipolar Effects in Fully Depleted Submicrometer SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 6, pp. 1384-1391, June 1991.

[76] M. Chan, F. Assaderaghi, S. A. Parke, S. S. Yuen, C. Hu and P. K. Ko, "Recess Channel Structure for Reducing Source/Drain Series Resistance in Ultrathin SOI MOSFET," *SOI Conf. Dig.*, pp. 172-173, 1993.

[77] Y. Yamaguchi, Y. Inoue, T. Ipposhi, T. Nishimura, and Y. Akasaka, "Improved Characteristics of MOSFETs on Ultrathin Thin SIMOX," *IEDM Dig.*, pp. 825-827, 1989.

[78] L. T. Su, M. J. Sherony, H. Hu, J. E. Chung and D. A. Antoniadis, "Optimization of Series Resistance in Sub-0.2μm SOI MOSFETs," *IEDM Dig.*, pp. 723-726, 1993.

[79] H. Shimada and T. Ohmi, "Minimum Parasitic Resistance for Ultra-Thin SOI MOSFET with High-Permittivity Gate Insulator Peformed by Lateral Contact Structure," *SOI Conf. Dig.*, pp. 98-99, 1995.

[80] F.-C. Hsu, P.-K. Ko, S. Tam, C. Hu and R. S. Muller, "An Analytical Breakdown Model for Short-Channel MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 29, No. 11, pp. 1735-1740, Nov. 1982.

[81] Y. G. Chen, J. B. Kuo, Z. Yu, and R. W. Dutton, "An Analytical Drain Current Model for Short-Channel Fully-Depleted Ultrathin Silicon-on-Insulator NMOS Devices," *Sol. St. Elec.*, Vol. 38, No. 12, pp. 2051-2057, Dec. 1995.

[82] K. K. Young and J. A. Burns, "Avalanche-Induced Drain-Source Breakdown in Silicon-on-Insulator n-MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 35, No. 4, pp. 426-431, Apr. 1988.

[83] H.-T. H. Chen, and R.-S. Huang, "Modeling for Floating Body Effects in Fully Depleted SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 3, pp. 583-590, Mar. 1993.

[84] E. P. Ver Ploeg, C. T. Nguyen, S. S. Wong, and J. D. Plummer, "Parasitic Bipolar Gain in Fully Depleted n-Channel SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 6, pp. 970-976, June 1994.

[85] H.-K. Yu, J.-S. Lyu, S.-W. Kang, and C.-K. Kim, "A Physical Model of Floating Body Thin Film Silicon-On-Insulator nMOSFET with Parasitic Bipolar Transistor," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 5, pp. 726-732, May 1994.

[86] N. Kistler and J. Woo, "Detailed Characterization and Analysis of the Breakdown Voltage in Fully Depleted SOI n-MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 7, pp. 1217-1221, July 1994.

[87] Y. Yamaguchi, T. Iwamatsu, H. Joachim, H. Oda, Y. Inoue, T. Nishimura, and K. Tsukamoto, "Source-to-Drain Breakdown Voltage Improvement in Ultrathin-Film SOI MOSFET's Using a Gate-Overlapped LDD Structure," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 7, pp. 1222-1226, July 1994.

[88] J. Chen, F. Assaderaghi, P.-K. Ko and C. Hu, "The Enhancement of Gate-Induced-Drain-Leakage (GIDL) Current in SOI MOSFET and its Impact on SOI Device Scaling," *SOI Conf. Dig.*, pp. 84-85, 1992.

[89] T. Y. Chan, P. K. Ko and C. Hu, "A Simple Method to Characterize Substrate Current in MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 5, No. 12, pp. 505-507, Dec. 1984.

[90] W. N. Grant, "Electron and Hole Ionization Rates in Epitaxial Silicon at High Electric Fields," *Sol. St. Elec.*, Vol. 16, pp.1189-1203, 1973.

[91] J. M. Higman, I. C. Kizilyalli and K. Hess, "Nonlocality of the Electron Ionization Coefficient in n-MOSFET's: An Analytic Approach," *IEEE Elec. Dev. Let.*, Vol. 9, No. 8, pp. 399-401, Aug. 1988.

[92] K. Taniguchi, M. Yamaji, K. Sonoda, T. Kunikiyo and C. Hamaguchi, "Monte Carlo Study of Impact Ionization Phenomena in Small Geometry MOSFET's," *IEDM Dig.*, pp. 355-358, 1994.

[93] H. J. Peifer, B. Meinerzhagen, R. Thoma and W. L. Engl, "Evaluation of Impact Ionization Modeling in The Framework of Hydrodynamic Equations," *IEDM Dig.*, pp. 131-134, 1991.

[94] J. W. Slotboom, G. Streutker, M. J. v. Dort, P. H. Woerlee, A. Pruijmboom, and D. J. Gravesteijn, "Non-Local Impact Ionization in Silicon Devices," *IEDM Dig.*, pp. 127-130, 1991.

[95] S. Takagi and A. Toriumi, "New Experimental Findings on Hot Carrier Transport under Velocity Saturation Regime in Si MOSFETs," *IEDM Dig.*, pp. 711-714, 1992.

[96] Y. Omura and K. Izumi, "Physical Background of Substrate Current Characteristics and Hot-Carrier Immunity in Short-Channel Ultrathin-Film MOSFET's/SIMOX," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 3, pp. 352-358, Mar. 1994.

[97] G. Verzellesi, G. Baccarani, C. Canali, P. Pavan, L. Vendrame, and E. Zanoni, "Prediction of Impact-Ionization-Induced Snap-Back in Advanced Si n-p-n BJT's by Means of a Nonlocal Analytical Model for the Avalanche Multiplication Factor," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 12, pp. 2296-2300, Dec. 1993.

[98] G.-B. Hong and J. G. Fossum, "Implementation of Nonlocal Model for Impact-Ionization Current in Bipolar Circuit Simulation and Application to SiGe HBT Design Optimization," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 6, pp. 1166-1173, June 1995.

[99] K. W. Su and J. B. Kuo, "A Non-Local Impact Ionization/Lattice Temperature Model for VLSI Double-Gate Ultrathin SOI NMOS Devices," *IEEE Trans. Elec. Dev.*, Vol. 44, No. 2, pp. 324-330, Feb. 1997.

Problems

1. For an SOI NMOS device as shown in Fig. 4.3, the gate oxide is 50Å. The channel length is 0.1μm. The doping density of the p-type silicon thin-film is $10^{18}cm^{-3}$. The thickness of the silicon thin-film is 500Å. The buried oxide is 3000Å.

   (a) Calculate the threshold voltage without considering the short channel effect.

   (b) Calculate the body effect coefficient.

   (c) Calculate the subthreshold slope in terms of mV/decade.

   (d) Calculate the short-channel effect threshold voltage.

   (e) If the thickness of the sidewall oxide is 100Å, calculate the narrow channel effect threshold voltage if the channel width is 0.2μm.

2. For the SOI NMOS device as shown in Fig. 4.3, if the p-type dopants of the thin film are replaced by the n-type dopants. Other parameters are the same. Recalculate (a)-(e) in Prob. 1.

3. Consider the double-gate SOI device as shown in Fig. 4.9. Instead of PMOS, an NMOS using an N^+ poly gate, a thin-film of 1000Å doped with a p-type doping density of $5 \times 10^{16}\text{cm}^{-3}$, front and back gate oxide layers of 100Å, and channel width and length of 5μm.

   (a) Compute its threshold voltage.

   (b) If the back gate oxide becomes 200Å, what is the threshold voltage?

   (c) If the silicon thin-film thickness becomes 500Å, what is the threshold voltage?

   (d) If the channel length becomes 0.2μm, what is the threshold voltage?

   (e) If the channel width becomes 0.2μm, what is the threshold voltage? (f) If the thin-film doping density is switched to n-type $2 \times 10^{16}\text{cm}^{-3}$, repeat (a)-(c) to compute the threshold voltage.

4. Consider the single-gate SOI NMOS device as shown in Fig. 4.22.

   (a) If the channel width is 10μm, compute the change in the threshold voltage when the channel length is scaled down from 10μm to 0.2μm.

   (b) If the channel width is changed to 0.2μm, compute the change in the threshold voltage as in (a).

   (c) Based on (a) and (b), when the channel width is scaled down, discuss the effect on the short channel effect.

   (d) If the silicon thin-film thickness becomes 500Å, repeat (a)-(c). Discuss the effect on the short channel and narrow channel effects when the silicon thin-film thickness becomes smaller.

5. Consider an SOI NMOS device with its parameters listed in Table 4.2. If the device is biased at $V_{GS} = 2V$ and $V_{DS} = 2.5V$, compute the following items:

   (a) The drain current and its lattice temperature.

   (b) Repeat (a) if the thickness of the buried oxide is shrunk to 2000Å.

   (c) Repeat (a) if μ_o is 200cm^2/Vsec.

   (d) Repeat (a)-(c) if the device is working in an environment temperature of 80C.

6. In Prob. 5, if the biasing voltages are changed to $V_{GS} = 0.5V$ and $V_{DS} = 3V$, considering impact ionization, compute the following items:

   (a) If $\alpha = 0.15V^{-1}$, $\beta = 15.7V^{-1}$, $K = K' = 0.85$, $I_{CBO} \cong 0$, and current gain $\alpha_0 = 0.994$, repeat the questions in Prob. 5.

   (b) If α_0 becomes 0.98, repeat (a).

7. Consider a double-gate SOI NMOS device with its cross section as shown in Fig. 4.9. Using the approach associated with Fig. 4.38, analyze the lateral electric field (E_y) in the post-saturation region and compute $|\frac{dE_y}{dy}/E_y|$. If the back gate is removed to become a single-gate device, compute $|\frac{dE_y}{dy}/E_y|$. Which of the single-gate and double-gate devices has a more higher change in the electric field distribution? Which one has a higher non-local effect?

Chapter 5

SOI CMOS Devices—Advanced

In this chapter, further reports on the SOI CMOS devices are described. For SOI CMOS technology, in addition to the inversion-mode devices, owing to the buried oxide isolation structure, accumulation-mode devices are also important. In this chapter, first, the DC and the capacitance models for the accumulation-mode SOI MOS devices are presented. Recently, the trends on the fully-depleted SOI CMOS devices are toward using very thin silicon thin-films. With a very thin silicon thin-film, device second order effects can be further improved. However, when the silicon thin-film is too thin, the threshold voltage of the SOI CMOS devices may be very sensitive to the silicon thin-film thickness. As a result, fully-depleted SOI CMOS devices with a very thin silicon thin-film may not be practical for mass production from a manufacturing point of view. Therefore, SOI technology goes back for a thicker silicon thin-film. With a thicker silicon thin-film, the silicon thin-film may not be fully depleted— partially-depleted SOI CMOS devices. For partially-depleted SOI MOS devices, due to the floating body structure, impact ionization and parasitic BJT effects are important. As a result, the kink effect in the strong inversion and peculiar subthreshold characteristics have been observed. In addition, due to the floating body structure, the positive feedback in the device causes the single-transistor latch phenomenon. Furthermore, the breakdown voltage can also be affected by the floating body. In the next portion of this chapter, the kink effect and the subthreshold behavior of the partially-depleted SOI MOS devices are analyzed. A Ge-implanted source structure based on engineering bandgap narrowing has been used to reduce the parasitic BJT effect in the SOI device. In the later portion of this chapter, a SiGe-implanted SOI MOS device to reduce the floating body effect is also reported. Due to the floating body structure, transient performance of SOI CMOS devices may be quite different from that of bulk ones. Transient analysis of SOI CMOS devices is described. As for bulk CMOS devices, deep-submicron

J. B. Kuo et al., *CMOS VLSI Engineering*

SOI CMOS devices also have hot carrier effects due to the high electric field in the lateral channel. In the next portion of the chapter, hot carrier effects of the SOI CMOS devices are analyzed. Due to the poor heat dissipation capability from the buried oxide structure, the temperature effect is important in SOI CMOS devices. In the remaining portion of the chapter, thermal analysis of the SOI CMOS devices is presented. On the other hand, owing to the buried oxide structure, SOI CMOS devices also have superior properties in radiation hardness. In the final portion of this chapter, it is dedicated to radiation hardness of the SOI CMOS devices, followed by noise analysis.

5.1 Accumulation-mode – Drain Current

Due to the buried oxide isolation structure, in SOI CMOS technology, accumulation-mode devices are also available in addition to the inversion-mode devices. Owing to their unique structure, accumulation-mode SOI PMOS devices have advantages in high-temperature operation [1], breakdown voltage [2], hot electron effect [3], floating body effect [4], and mobility [5]. Short-channel accumulation-mode SOI PMOS devices and circuits have been reported [5]-[7]. For an accumulation-mode SOI PMOS device, the silicon thin-film is p-type. Therefore, from the source, via the silicon thin-film, to the drain, it is $P^+ - P - P^+$. In contrast, for an inversion-mode SOI PMOS device, it is $P^+ - N - P^+$. Fig. 5.1 shows the drain current characteristics of a typical accumulation-model SOI PMOS device [8]. Its current conduction mechanisms are shown in Fig. 5.2[8]. As shown in Fig. 5.2, the current conduction mechanisms in an accumulation-mode SOI PMOS device are complicated. Depending on the biasing conditions, various current conduction situations may exist in the accumulation-mode SOI PMOS device. In (a) of Fig. 5.2, when the device is turned off, the silicon thin-film is fully depleted. When the device gradually turns on in (b), buried channel exists in the silicon thin-film. In addition, near the drain, the buried channel is pinched off. In (c), buried and surface channels coexist in the silicon thin-film and the surface channel is pinched off. In (d), the device is with a buried channel without being pinched off. In (e), the device is with both buried and surface channels without being pinched off.

Fig. 5.3 shows the IV characteristics of an accumulation-mode SOI NMOS device with a front gate oxide of 125Å, a silicon thin-film of 1000Å, and a channel length of 0.8μm[3]. As shown in the figure, due to the n-type silicon thin-film region ($n^+ - n - n^+$), there is no parasitic BJT in the device. As a result, the breakdown voltage of the accumulation-mode SOI MOS devices is higher as compared to the inversion-mode devices.

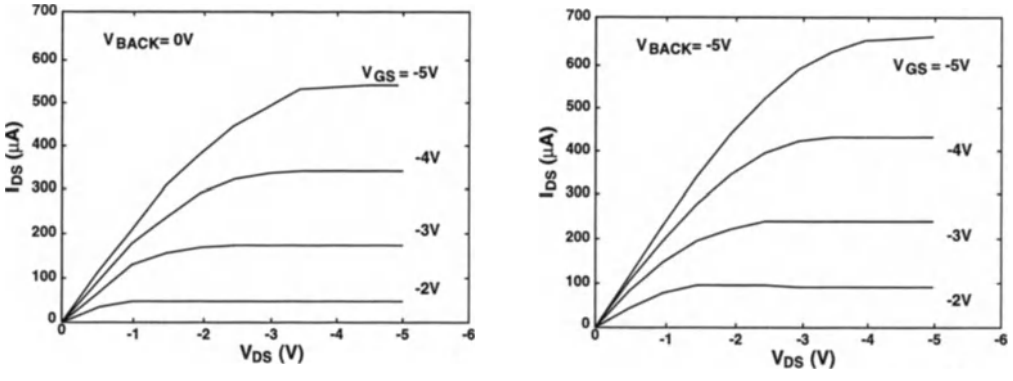


Figure 5.1: Drain current versus drain-source voltage characteristics of an accumulation-mode SOI PMOS device with an aspect ratio of W/L = 50μm/1.5μm, a front gate oxide of 230Å, a buried oxide of 3500Å, a silicon thin-film of 1000Å doped with a p-type doping density of $4 \times 10^{16}\text{cm}^{-3}$ biased at a back gate bias of 0V and -5V.

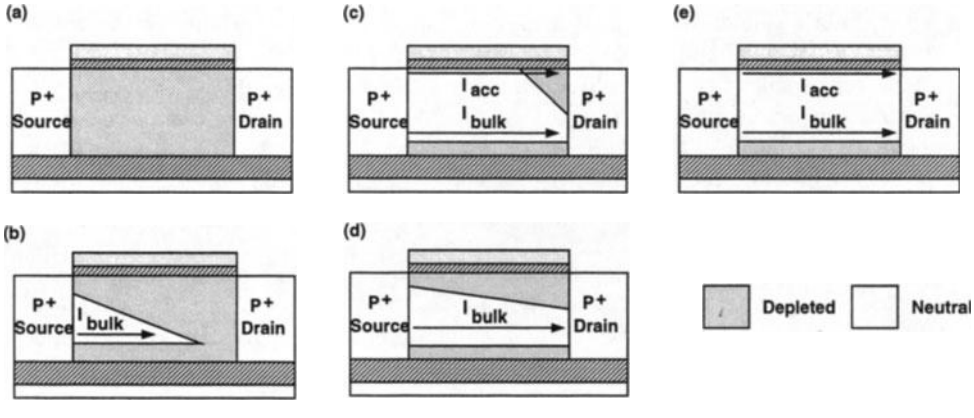


Figure 5.2: Conduction mechanisms in a long-channel accumulation-mode SOI PMOS device.

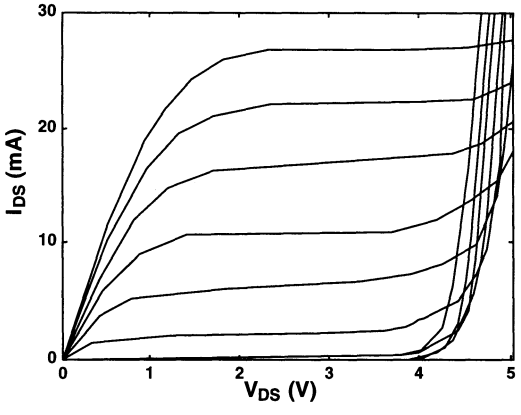


Figure 5.3: IV characteristics of an accumulation-mode SOI NMOS device with a front gate oxide of 125Å, a silicon thin-film of 1000Å, and a channel length of 0.8μm.

Due to the buried channel structure of the accumulation-mode SOI MOS devices, subthreshold characteristics may be influenced substantially by the silicon thin-film thickness and the back gate bias. Fig. 5.4 shows the inverse subthreshold slope versus silicon thin-film thickness of an accumulation-mode SOI NMOS device with a front gate oxide of 175Å, a buried oxide of 3800Å, and a channel length of 1μm[2]. As shown in the figure, when the silicon thin-film becomes thicker or the back gate bias becomes more positive, the inverse subthreshold slope becomes worse.

Short-channel accumulation-mode SOI PMOS devices and circuits have been reported [5]-[7]. Analysis of accumulation-mode SOI MOS devices has been reported [9]-[14]. Most of the analysis is for accumulation-mode SOI MOS devices operating at a certain condition[15]-[20]. In this section, an analytical drain current model considering channel length modulation and prepinchoff velocity saturation for short-channel accumulation-mode SOI PMOS devices is described[21]. The differences between the short-channel analytical model and the long-channel one for the accumulation-mode MOS devices will be described. In the following subsections, derivation of the analytical model is described.

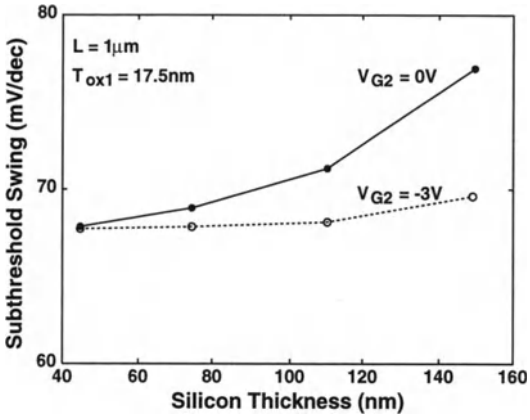


Figure 5.4: Inverse subthreshold slope versus silicon thin-film thickness of an accumulation-mode SOI NMOS device with a front gate oxide of 175Å, a buried oxide of 3800Å, and a channel length of 1μm.

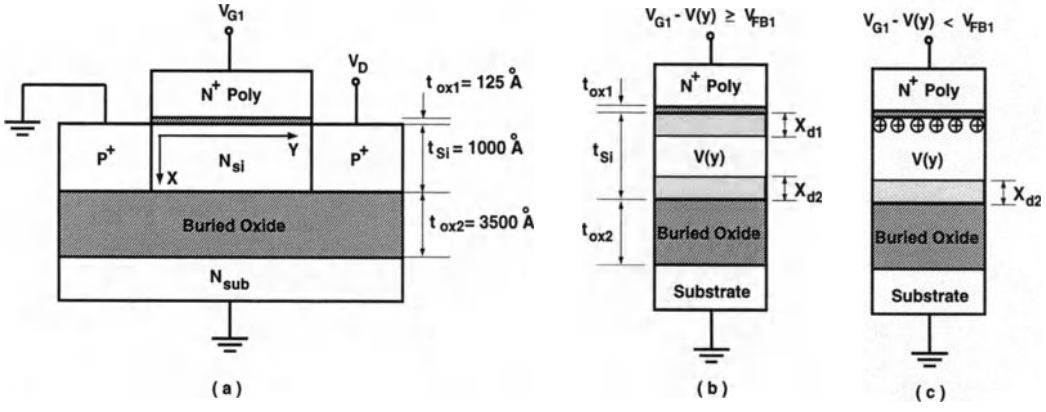


Figure 5.5: (a) Cross section of the accumulation-mode SOI PMOS device under study. (b) The upper and the lower portions of the silicon thin-film are depleted. (c) The lower portion of the silicon thin-film is depleted. The top surface is accumulated with holes.

5.1.1 Mobile Carriers

Fig. 5.5(a) shows the cross section of the accumulation-mode SOI PMOS device under study. It has a $2 \times 10^{16}\text{cm}^{-3}$ p-type silicon thin-film of 1000Å above a 3500Å buried oxide[21]. The p-type substrate doping density is $1 \times 10^{15}\text{cm}^{-3}$. A front thin oxide of 125Å is placed under an N+ polysilicon gate. Fig. 5.5(b) shows the cross section in the substrate direction at a location y in the channel as the device is biased at $V_{G1} - V(y) \geq V_{FB1}$, where V_{G1} is the front gate voltage, $V(y)$ is the channel potential at location y in the channel, and V_{FB1} is flat-band voltage of the front gate[21]. As shown in the figure, the upper and the lower portions of the silicon thin-film are depleted. Solving the Poisson's equation in the substrate direction, the widths of the upper and the lower depletion portions in the silicon thin-film are expressed as [8]:

$$X_{d1}(V(y)) = t_{si} \cdot [-\frac{C_{si}}{C_{ox1}} + \sqrt{(\frac{C_{si}}{C_{ox1}})^2 + \frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{G1} - V_{FB1} - V(y))}], \quad (5.1)$$

$$X_{d2}(V(y)) = t_{si} \cdot [-\frac{C_{si}}{C_{ox2}} + \sqrt{(\frac{C_{si}}{C_{ox2}})^2 + \frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{G2} - V_{FB2} - V(y))}], \quad (5.2)$$

where t_{si} is the silicon thin-film thickness, $C_{si} = \epsilon_{si}/t_{si}$, ϵ_{si} is the silicon permittivity, $C_{ox1} = \epsilon_{ox}/t_{ox1}$, ϵ_{ox} is the oxide permittivity, t_{ox1} is the oxide thickness under the front gate, $C_{ox2} = \epsilon_{ox}/t_{ox2}$, t_{ox2} is the thickness of the buried oxide, V_{G2} is the back gate voltage, and V_{FB2} is the flat-band voltage of the back gate. Under this condition, the conducting channel is in the center neutral portion of the silicon thin-film. The amount of total mobile carriers in the center channel is:

$$Q_{film} = qN_{si}(t_{si} - X_{d1} - X_{d2}). \quad (5.3)$$

As $V_{G1} - V(y) < V_{FB1}$, as indicated in Fig. 5.5(c)[21], the upper depletion region disappears. Holes are accumulated at the top surface. Under this situation, the amount of total mobile carriers in the channel, which includes the amount of total holes in the neutral silicon thin-film (Q_{film}) and in the accumulated holes at top (Q_{acc}), is

$$\begin{aligned} Q_{acc} &= -C_{ox1}(V_{G1} - V_{FB1} - V(y)), \\ Q_{film} &= qN_{si}(t_{si} - X_{d2}). \end{aligned} \quad (5.4)$$

For a short-channel accumulation-mode SOI PMOS device, in addition to the influence from the back gate, the lower depletion region in the silicon thin-film may

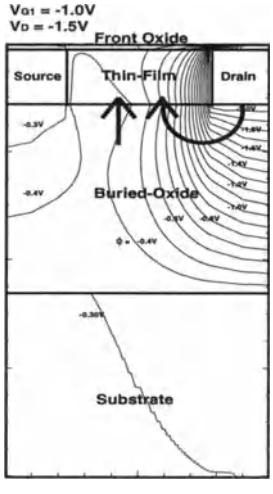


Figure 5.6: 2D electrostatic potential contours in the accumulation-mode SOI PMOS device biased at $V_{G1} = -1.0V$, and $V_D = -1.5V$.

also be influenced by the drain voltage via the buried oxide [10][16][22]. As shown in Fig. 5.6, from the 2D potential contours in the accumulation-mode SOI PMOS device biased at $V_{G1} = -1.0$V, and $V_D = -1.5$V, the influence from the drain is not negligible[21]. Since the vertical electric field under the silicon thin-film is affected by the drain voltage, X_{d2} is also influenced by the drain voltage. Therefore, an effective gate voltage V_{Geff2} has been used to describe the influence of V_D and V_{G2} in the vertical electric field. Considering the influence of the drain voltage, the width of the lower depletion region in the silicon thin-film can be modified as:

$$X_{d2}(V(y)) = t_{si} \cdot [-\frac{C_{si}}{C_{ox2}} + \sqrt{(\frac{C_{si}}{C_{ox2}})^2 + \frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{Geff2} - V_{FB2} - V(y))}], \quad (5.5)$$

where $V_{Geff2} \simeq V_{G2} + k_1 \cdot V_D$, and a similar approach [22] has been adopted to simplify the model. k_1 is a fitting parameter used to reflect the indirect influence of the drain voltage on the lower depletion region in the silicon thin-film. k_1 is related to the channel length and the thickness of the buried oxide.

For the mobile carriers in the neutral region of the silicon thin-film (Q_{film}), the hole mobility is [23]: $\mu_b = \frac{\mu_{b0}}{1+\frac{\mu_{b0}}{v_{sat}}E}$, where μ_{b0} is the low-field mobility, v_{sat} is the hole saturated velocity, and E is the lateral electric field. For the mobile carriers in the

Parameter	Value
L_{eff}	0.55μm
W	8.0μm
t_{ox1}	125Å
t_{ox2}	3500Å
t_{si}	1000Å
N_{si}	$2.0 \times 10^{16}\text{cm}^{-3}$
N_{sub}	$1.0 \times 10^{15}\text{cm}^{-3}$
μ_{b0}	$204\text{cm}^2/\text{V} \cdot \text{sec}$
v_{sat}	$9.5 \times 10^6\text{cm/sec}$
θ	0.22
k_1	1.0
k_2	0.9
k_3	0.7
n_d	$0.08V^{-1}$
R_S	200Ω
I_{b0}	2.0×10^{-8}A
V_{FB1}	−0.694V
V_{FB2}	−2.592V
V_{TH}	−0.7V

Table 5.1: Device parameters of the accumulation-mode SOI PMOS device under study.

accumulated hole region at top (Q_{acc}), holes are influenced by both the lateral and the vertical electric fields. Therefore, for Q_{acc}, its hole mobility is [24]: $\mu_s = \frac{\mu_{s0}}{1+\frac{\mu_{s0}}{v_{sat}}E}$, where $\mu_{s0} = \frac{k_2\mu_{b0}}{1-\theta\cdot(V_{G1}-V_{FB1})}$, k_2 and θ are fitting parameters used to account for the surface scattering effect.

5.1.2 Drain current

Depending on the biasing condition, the mechanism of the conducting current in an accumulation-mode SOI PMOS device can be complicated. The neutral silicon thin-film region may offer holes for current conduction. In addition, the accumulated holes at the top surface may also contribute to the mobile carriers for current conduction. Depending on the biasing conditions, the accumulation-mode SOI PMOS device may be working in the subthreshold, triode or saturation region. Depending on the biasing conditions, there are seven cases for the current conduction condition

in the accumulation-mode SOI PMOS device as shown in Fig. 5.7.

In Case 1 [21], at a small V_{G1}, the silicon thin-film is fully depleted for the device biased in the subthreshold region. In Case 2, as the magnitude of V_{G1} increases, the upper and the lower portions of the silicon thin-film are depleted. Only the center portion of the silicon thin-film is neutral, which can be provided for current conduction. In Case 3, the center conducting channel is pinched off. In Case 4, as the magnitude of V_{G1} further increases, the top depletion region disappears. The neutral region spreads from the center to the top. In addition, holes are accumulated at the top surface. The current conduction is via the neutral region and the accumulated hole region at top. If the magnitude of V_D increases, as shown in Case 5, the top hole-accumulated channel is pinched off. Beyond the top pinchoff point, the center neutral region is more important for current conduction. If the magnitude of V_D increases further, even the center neutral region may pinch off as shown in Case 6. It's worth pointing out that in Case 6, beyond the top pinch-off point, the current conduction is dominated by the center neutral region. In Case 7, the top and the center channels may reach the saturation point at the same lateral location. This means that both the top accumulated and the center neutral channels are equally important for current conduction at this location. Compared with the current conduction in the long-channel accumulation-mode SOI MOS devices [8] and bulk buried-channel MOS devices[25][26], Case 7 for the short-channel accumulation-mode SOI PMOS device is unique. As will be described in the following subsection, in Case 7, prepinchoff velocity saturation may exist in the top accumulated channel.

(a) Case 1

In Case 1, the accumulation-mode SOI PMOS device is biased in the subthreshold region. The threshold voltage of the device is defined as the front gate voltage $V_{G1} = V_{TH}$ when the fully-depleted condition is satisfied at the source end. Therefore at threshold voltage one obtains: $t_{si} = X_{d1}(0) + X_{d2}(0)$. From Eqs. (5.1)(5.2), the threshold voltage formula is obtained:

$$\begin{aligned} V_{TH} &= V_{FB1} + V_{Geff2} - V_{FB2} + \frac{qN_{si}t_{si}^2}{2\epsilon_{si}}[(1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}})^2 + (\frac{C_{si}}{C_{ox2}})^2 - \\ &\quad (\frac{C_{si}}{C_{ox1}})^2 - 2 \cdot (1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}})\sqrt{(\frac{C_{si}}{C_{ox2}})^2 + \frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{Geff2} - V_{FB2})}]. \end{aligned} \tag{5.6}$$

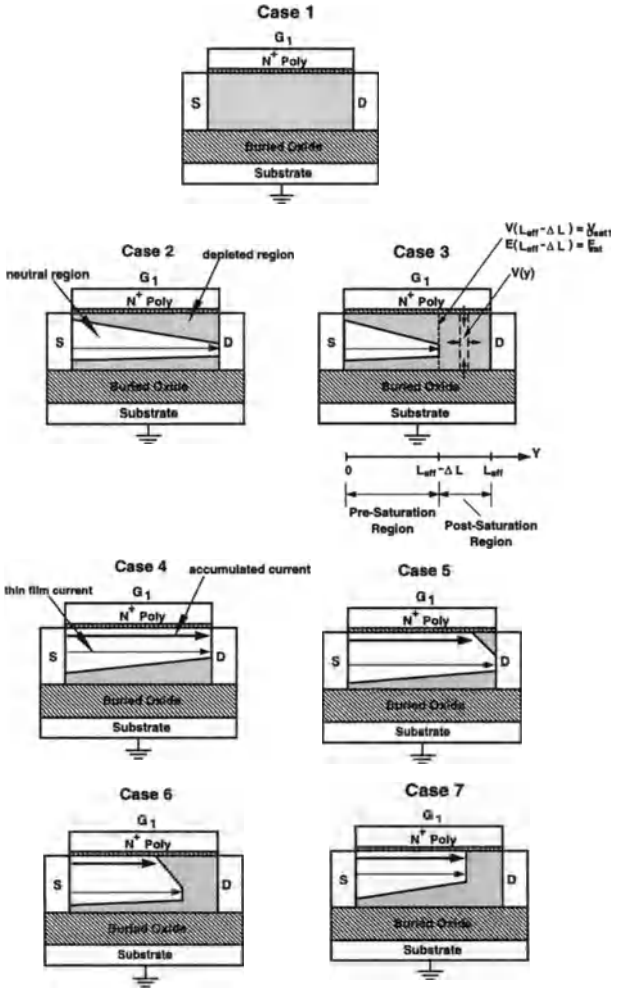


Figure 5.7: Various conditions in the accumulation-mode SOI PMOS device biased at various conditions. Case 1: fully depleted. Case 2: depleted at upper and lower. Case 3: depleted at upper and lower and pinched off at center. Case 4: depleted at lower and accumulated at top. Case 5: depleted at lower and pinched off at the top accumulated. Case 6: both top accumulated channel and the center neutral pinched off. Case 7: both top accumulated channel and the center neutral saturates at the same lateral location.

In the subthreshold region, diffusion current dominates. Therefore, from Ref. [27], the drain current is:

$$I_{D1} = -\frac{W}{L_{eff}} I_{b0} \cdot [1 - exp(\frac{V_D}{\phi_t})] \cdot \frac{exp[-\frac{(V_{G1}-V_{TH})}{n\phi_t}]}{1 + exp[-\frac{(V_{G1}-V_{TH})}{n\phi_t}]}, \tag{5.7}$$

where $n = 1 + \frac{C_{ox1}C_{ox2}+C_{ox2}C_{si}}{C_{ox1}C_{si}} + n_d|V_D|$. ϕ_t is 0.0259V, L_{eff} is the channel length, W is the channel width, I_{b0} is a fitting parameter, and n_d represents the influence of the two-dimensional effect from the drain voltage in the subthreshold slope [28].

(b) Case 2

As shown in Fig. 5.7, for Case 2, current conduction is via the center neutral region and the device is operating in the triode region. Since the drain end of the center channel is not pinched off, the drain current for Case 2 is expressed as:

$$I_{D2} = \frac{\mu_{b0}}{1 - \frac{\mu_{b0}}{v_{sat}}\frac{\partial V}{\partial y}} W Q_{film}(y) \cdot \frac{\partial V}{\partial y}. \tag{5.8}$$

Note that in the above equation, the positive direction of the drain current is defined as the current flowing into the drain contact. In Eq. (5.8), by moving the denominator to the left hand side and integrating from source to drain using Eq. (5.3), one obtains the drain current formula for Case 2 as:

$$I_{D2} = \frac{W}{L_{eff}} \frac{\mu_{b0}}{1 - \frac{\mu_{b0}}{v_{sat}}\frac{V_D}{L_{eff}}} qN_{si}t_{si}[V_D + F_1(V_D) - F_1(0) + F_2(V_D) - F_2(0)], \tag{5.9}$$

where $F_1(V) = \frac{C_{si}}{C_{ox1}}V + \frac{qN_{si}t_{si}^2}{3\epsilon_{si}}[(\frac{C_{si}}{C_{ox1}})^2 + \frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{G1} - V_{FB1} - V)]^{\frac{3}{2}}$, and $F_2(V) = \frac{C_{si}}{C_{ox2}}V + \frac{qN_{si}t_{si}^2}{3\epsilon_{si}}[(\frac{C_{si}}{C_{ox2}})^2 + \frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{Geff2} - V_{FB2} - V)]^{\frac{3}{2}}$.

(c) Case 3

In Case 3, if the magnitude of the drain voltage increases, holes in the center neutral region near the drain may be travelling at the saturated velocity. Defining the saturation point where holes are traveling just at the saturated velocity, the center neutral channel region is divided into two regions: the pre-saturation region and the post-saturation region. At the saturation point, the channel potential is V_{Dsat1}. Instead of finding the solution for V_{Dsat1}, the channel potential at the pinchoff point (V_p) where the center neutral channel pinches off is derived first. At the pinchoff

point, one obtains: $t_{si} = X_{d1}(V_p) + X_{d2}(V_p)$. From Eqs.(5.1)(5.2), the pinchoff potential is:

$$V_p = V_{G1} - V_{FB1} + \frac{qN_{si}t_{si}^2}{2\epsilon_{si}}(\frac{C_{si}}{C_{ox1}})^2 - \frac{qN_{si}t_{si}^2}{2\epsilon_{si}}\frac{1}{4(1+C_{si}/C_{ox1}+C_{si}/C_{ox2})^2}\cdot \quad (5.10)$$
$$[-(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})^2+(\frac{C_{si}}{C_{ox2}})^2-(\frac{C_{si}}{C_{ox1}})^2+\frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{Geff2}-V_{G1}-V_{FB2}+V_{FB1})]^2$$

At the saturation point, the hole velocity is equal to $k_3 v_{sat}$, where k_3 is a constant smaller than 1. (Note that the hole velocity: $v_p = \mu_b E = \frac{\mu_{b0}E}{1+\frac{\mu_{b0}E}{v_{sat}}}$ is equal to v_{sat} as the electric field E is approaching infinity. In the above equation, for a hole velocity above $k_3 v_{sat}(k_3 = 0.7)$, a further increase in E does not lead to a proportional increase in velocity. Therefore, $k_3 v_{sat}$ is regarded as the saturation point to simplify the model. k_3 can be regarded as a parameter to describe the effect of the length of the post-saturation region.) The drain current for Case 3 must satisfy the following condition: $I_{D2}|_{V_D=V_{Dsat1}} = -Wk_3v_{sat}\cdot qN_{si}[t_{si} - X_{d1}(V_{Dsat1}) - X_{d2}(V_{Dsat1})]$. This is an equation in terms of V_{Dsat1}, which is difficult to solve. Applying V_p as the initial guess for V_{Dsat1} in the Newton's method on the above equation, one obtains: $I_{D2}|_{V_D=V_p} \simeq -Wk_3v_{sat}\cdot qN_{si}(-\frac{\partial X_{d1}}{\partial V}|_{V_p} - \frac{\partial X_{d2}}{\partial V}|_{V_p})(V_{Dsat1}-V_p)$, where $\frac{\partial X_{d1}}{\partial V}|_{V_p} = -\frac{\frac{\epsilon_{si}}{qN_{si}t_{si}}}{\sqrt{(\frac{C_{si}}{C_{ox1}})^2+\frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{G1}-V_{FB1}-V_p)}}$, and $\frac{\partial X_{d2}}{\partial V}|_{V_p} = -\frac{\frac{\epsilon_{si}}{qN_{si}t_{si}}}{\sqrt{(\frac{C_{si}}{C_{ox2}})^2+\frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{Geff2}-V_{FB2}-V_p)}}$. Therefore, the V_{Dsat1} formula is:

$$V_{Dsat1} \simeq V_p + \frac{I_{D2}|_{V_D=V_p}}{Wk_3v_{sat}\cdot qN_{si}(\frac{\partial X_{d1}}{\partial V}|_{V_p}+\frac{\partial X_{d2}}{\partial V}|_{V_p})}. \quad (5.11)$$

At the saturation point, defining the lateral electric field as E_{sat}, one obtains: $k_3 v_{sat} = \frac{\mu_{b0}}{1+\frac{\mu_{b0}}{v_{sat}}E_{sat}}E_{sat}$. Therefore, E_{sat} is: $E_{sat} = \frac{k_3 v_{sat}}{\mu_{b0}(1-k_3)}$. From the above analysis, as $|V_D| > |V_{Dsat1}|$, the post-saturation region starts to exist in the device. Under this situation, gradual channel approximation is not applicable. 2D effects should be considered. As shown in Case 3 of Fig. 5.7, considering the Gauss' box in the post-saturation region $(L_{eff} - \Delta L \le y \le L_{eff})$ [24], the width of the post-saturation region formula is obtained as in the previous chapter: $\Delta L = \lambda \cdot ln[-\frac{V_D-V_{Dsat1}}{\lambda E_{sat}} + \sqrt{1+(\frac{V_D-V_{Dsat1}}{\lambda E_{sat}})^2}]$, where $\lambda = \sqrt{\frac{\epsilon_{si}t_{si}}{\epsilon_{ox}}\frac{t_{ox1}t_{ox2}}{t_{ox1}+t_{ox2}}}$. Therefore, the drain current formula for Case 3 can be obtained by modifying Case 2 formula (Eq. (5.9)) as:

$$I_{D3} = \frac{W}{L_{eff}-\Delta L}\cdot\frac{\mu_{b0}}{1-\frac{\mu_{b0}}{v_{sat}}\frac{V_{Dsat1}}{L_{eff}-\Delta L}}\cdot qN_{si}t_{si}[V_{Dsat1}+F_1(V_{Dsat1})-F_1(0)$$
$$+F_2(V_{Dsat1})-F_2(0)]. \quad (5.12)$$

(d) Case 4

As shown in Fig. 5.7, in Case 4, if V_{G1} is negative enough, the upper depletion region of the silicon thin-film may disappear. In addition, the top surface may have accumulated holes. The accumulated surface channel at top is not pinched off. In addition, the hole velocity in the center neutral channel does not reach the saturated velocity. Under this situation, current conduction is via both the top accumulated channel and the center neutral channel. Therefore, the drain current for Case 4 is:

$$I_{D4} = WQ_{film}\frac{\mu_{b0}}{1-\frac{\mu_{b0}}{v_{sat}}\frac{\partial V}{\partial y}}\cdot\frac{\partial V}{\partial y}+WQ_{acc}\frac{\mu_{s0}}{1-\frac{\mu_{s0}}{v_{sat}}\frac{\partial V}{\partial y}}\cdot\frac{\partial V}{\partial y}. \tag{5.13}$$

Approximating the $\frac{\partial V}{\partial y}$ portion in the denominator of the mobility in the above equation by $\frac{\partial V}{\partial y}\simeq\frac{V_D}{L_{eff}}$ and integrating from source to drain, the drain current formula for Case 4 is:

$$\begin{aligned} I_{D4} &= -\frac{W}{L_{eff}}C_{ox1}\frac{\mu_{s0}}{1-\frac{\mu_{s0}}{v_{sat}}\frac{V_D}{L_{eff}}}[(V_{G1}-V_{FB1})V_D-\frac{1}{2}{V_D}^2]+\frac{W}{L_{eff}}qN_{si}t_{si}\cdot \\ &\quad \frac{\mu_{b0}}{1-\frac{\mu_{b0}}{v_{sat}}\frac{V_D}{L_{eff}}}[V_D+F_2(V_D)-F_2(0)]. \end{aligned} \tag{5.14}$$

(e) Case 5

As shown in Fig. 5.7, in Case 5, the current conduction is via the top accumulated channel and the center neutral region. In addition, the top accumulated channel is pinched off and the center neutral channel does not have the post-saturation region yet. Therefore, using the similar method as for Case 4 except for the two-segments approach, one obtains the drain current formula for Case 5 as:

$$\begin{aligned} I_{D5} &= \frac{W}{L_{eff}}\frac{\mu_{s0}}{1-\frac{\mu_{s0}}{v_{sat}}\frac{V_D}{L_{eff}}}\int_0^{V_{G1}-V_{FB1}}-C_{ox1}[V_{G1}-V_{FB1}-V]\cdot dV+ \\ &\quad \frac{W}{L_{eff}}\frac{\mu_{b0}}{1-\frac{\mu_{b0}}{v_{sat}}\frac{V_D}{L_{eff}}}[\int_0^{V_{G1}-V_{FB1}}qN_{si}(t_{si}-X_{d2}(V))\cdot dV+ \\ &\quad \int_{V_{G1}-V_{FB1}}^{V_D}qN_{si}(t_{si}-X_{d1}(V)-X_{d2}(V))\cdot dV], \\ &= -\frac{W}{L_{eff}}\frac{\mu_{s0}}{1-\frac{\mu_{s0}}{v_{sat}}\frac{V_D}{L_{eff}}}\frac{1}{2}C_{ox1}(V_{G1}-V_{FB1})^2+\frac{W}{L_{eff}}\frac{\mu_{b0}}{1-\frac{\mu_{b0}}{v_{sat}}\frac{V_D}{L_{eff}}}qN_{si}t_{si}\cdot \\ &\quad [V_D+F_1(V_D)-F_1(V_{G1}-V_{FB1})+F_2(V_D)-F_2(0)]. \end{aligned} \tag{5.15}$$

(f) Case 6

As shown in Fig. 5.7, in Case 6, the top accumulated channel is pinched off. In addition, the center neutral channel is also pinched off. However, the top accumulated channel and the center neutral channel do not pinch off at the same lateral location. The accumulated channel pinches off earlier. Define V_{Dsat2} as the channel potential, at which travelling holes in the center neutral channel just reach the saturated velocity ($k_3 v_{sat}$), in the center neutral channel. The drain current for Case 6 must satisfy a condition by considering the drain current at the saturation point (V_{Dsat2}) in the center channel and the drain current formula for Case 5 using $V_D = V_{Dsat2}$ as:

$$I_{D5}|_{V_D=V_{Dsat2}} = -Wk_3 v_{sat} \cdot qN_{si}[t_{si} - X_{d1}(V_{Dsat2}) - X_{d2}(V_{Dsat2})]. \quad (5.16)$$

Using a similar method as for Case 3, the V_{Dsat2} formula is approximated as:

$$V_{Dsat2} \simeq V_p + \frac{I_{D5}|_{V_D=V_p}}{Wk_3 v_{sat} \cdot qN_{si}(\frac{\partial X_{d1}}{\partial V}|_{V_p} + \frac{\partial X_{d2}}{\partial V}|_{V_p})}. \quad (5.17)$$

Using Eq. (5.17)(5.15), the drain current formula for Case 6 can be obtained:

$$I_{D6} = -\frac{W}{L_{eff} - \Delta L} \frac{\mu_{s0}}{1 - \frac{\mu_{s0}}{v_{sat}} \frac{V_{Dsat2}}{L_{eff} - \Delta L}} \frac{1}{2} C_{ox1}(V_{G1} - V_{FB1})^2 + \frac{W}{L_{eff} - \Delta L} \frac{\mu_{b0}}{1 - \frac{\mu_{b0}}{v_{sat}} \frac{V_{Dsat2}}{L_{eff} - \Delta L}} \cdot qN_{si} t_{si} \cdot [V_{Dsat2} + F_1(V_{Dsat2}) - F_1(V_{G1} - V_{FB1}) + F_2(V_{Dsat2}) - F_2(0)], \quad (5.18)$$

where $\Delta L = \lambda \cdot ln[-\frac{V_D - V_{Dsat2}}{\lambda E_{sat}} + \sqrt{1 + (\frac{V_D - V_{Dsat2}}{\lambda E_{sat}})^2}]$.

(g) Case 7

Case 7 is similar to Case 6 except that the top accumulated channel has prepinchoff velocity saturation. In the center neutral channel, before the top accumulated channel pinches off, the hole velocity already reaches the saturated velocity ($k_3 v_{sat}$). Define V_{Dsat3} as the channel potential at which the hole velocity of the center channel just reaches the saturated velocity. Using the drain current formula for Case 4 and $V_D = V_{Dsat3}$, the drain current for Case 7 must satisfy the following condition: $I_{D4}|_{V_D=V_{Dsat3}} = \frac{\mu_{s0} E_{sat}}{1 + \frac{\mu_{s0}}{v_{sat}} E_{sat}} WC_{ox1}(V_{G1} - V_{FB1} - V_{Dsat3}) - Wk_3 v_{sat} \cdot qN_{si}[t_{si} - X_{d2}(V_{Dsat3})]$. Using a similar method as for Case 3, the above equation can be simplified as:

$$I_{D4}|_{V_D=V_p} \simeq \frac{\mu_{s0} E_{sat}}{1 + \frac{\mu_{s0}}{v_{sat}} E_{sat}} WC_{ox1}(V_{G1} - V_{FB1} - V_{Dsat3}) - Wk_3 v_{sat} \cdot qN_{si} \cdot [-\frac{\partial X_{d1}}{\partial V}|_{V_p} \cdot (V_{G1} - V_{FB1} - V_p) - \frac{\partial X_{d2}}{\partial V}|_{V_p} \cdot (V_{Dsat3} - V_p)]. \quad (5.19)$$

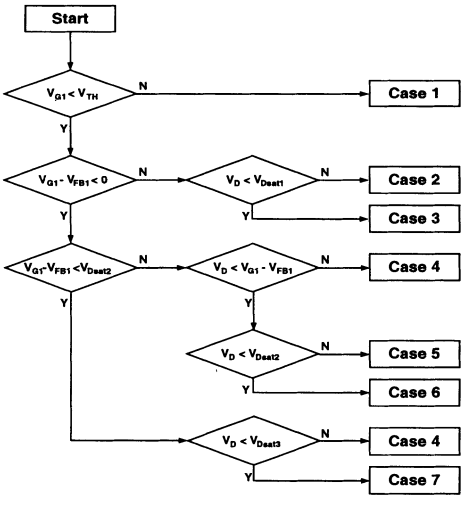


Figure 5.8: Judgment flowchart for determining which drain current formula should be used.

Therefore, V_{Dsat3} becomes:

$$V_{Dsat3} \simeq V_{G1} - V_{FB1} + \frac{I_{D4}|_{V_D=V_p} - Wk_3 v_{sat} \cdot qN_{si}(\frac{\partial X_{d1}}{\partial V}|_{V_p} + \frac{\partial X_{d2}}{\partial V}|_{V_p})(V_{G1} - V_{FB1} - V_p)}{Wk_3 v_{sat} \cdot qN_{si}\frac{\partial X_{d2}}{\partial V}|_{V_p} - WC_{ox1}\mu_{s0}E_{sat}/(1 + \frac{\mu_{s0}}{v_{sat}}E_{sat})}. \tag{5.20}$$

Therefore, the drain current formula for Case 7 may be obtained by modifying Eq. (5.14) and using Eq. (5.20) as:

$$\begin{aligned} I_{D7} = & -\frac{W}{L_{eff} - \Delta L} C_{ox1} \frac{\mu_{s0}}{1 - \frac{\mu_{s0}}{v_{sat}} \frac{V_{Dsat3}}{L_{eff} - \Delta L}} [(V_{G1} - V_{FB1})V_{Dsat3} - \frac{1}{2}{V_{Dsat3}}^2] \\ & + \frac{W}{L_{eff} - \Delta L} qN_{si}t_{si} \cdot \frac{\mu_{b0}}{1 - \frac{\mu_{b0}}{v_{sat}} \frac{V_{Dsat3}}{L_{eff} - \Delta L}} [V_{Dsat3} + F_2(V_{Dsat3}) - F_2(0)], \end{aligned} \tag{5.21}$$

where $\Delta L = \lambda \cdot ln[-\frac{V_D - V_{Dsat3}}{\lambda E_{sat}} + \sqrt{1 + (\frac{V_D - V_{Dsat3}}{\lambda E_{sat}})^2}]$.

Based on the above formula, Fig. 5.8 shows the judgment flowchart for determining which drain current formula should be used for the accumulation-mode SOI

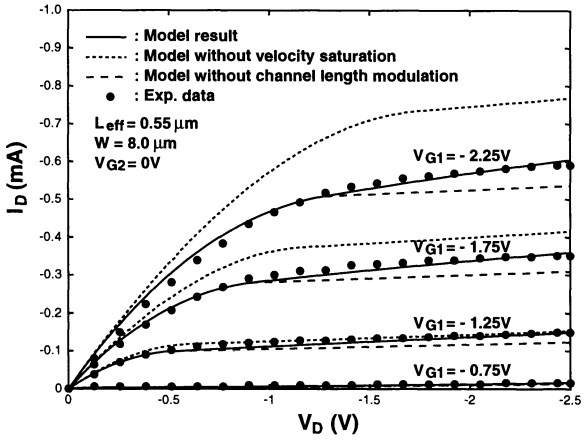


Figure 5.9: The drain current versus the drain voltage of the accumulation-mode SOI PMOS device based on the analytical model considering velocity saturation and channel length modulation and the experimental data.

PMOS device[21]. As shown in the figure, if $V_{G1} > V_{TH}$, the device is biased in the subthreshold region, Case 1 drain current formula should be used. If $V_{G1} < V_{TH}$, a further decision is necessary. If $V_{G1} - V_{FB1} > 0$, Case 2 and Case 3 formulas should be used. If $V_D > V_{Dsat1}$, Case 2 formula should be used. Otherwise, Case 3 formula is used. If $V_{G1} - V_{FB1} < 0$, a further decision is necessary. If $V_{G1} - V_{FB1} > V_{Dsat2}$, Cases 4,5,and 6 should be used. Otherwise, Cases 4 and 7 should be used.

As shown in Table 5.1, the test device for studying the IV characteristics has a channel length of 0.55μm. It has a $2 \times 10^{16}\text{cm}^{-3}$ p-type silicon thin-film of 1000Å above a 3500Å buried oxide[5]. The p-type substrate doping density is $1 \times 10^{15}\text{cm}^{-3}$. A front thin oxide of 125Å is placed under an N+ polysilicon gate.

Fig. 5.9 shows the drain current versus the drain voltage of the accumulation-mode SOI PMOS device based on the analytical model considering velocity saturation and channel length modulation and the experimental data [5]. The model result without considering velocity saturation ($v_{sat} \to \infty$) and the model result without considering channel length modulation ($\Delta L = 0$) have also been included. As shown in the figure, without considering channel length modulation, substantial deviations can be seen in the saturation region. Without considering velocity saturation, the drain current in both the triode and the saturation regions is overestimated. Fig. 5.10

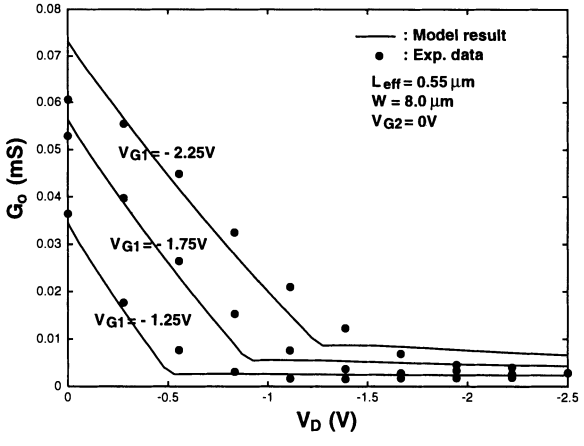


Figure 5.10: Output conductance versus drain voltage of the accumulation-mode SOI PMOS device based on the analytical model and the experimental data.

shows the output conductance versus the drain voltage of the accumulation-mode SOI PMOS device based on the analytical model and the experimental data[5][21]. As shown in the figure, the transition region from the triode region to the saturation region is smooth, which indicates that the technique in handling the saturation point is reasonable.

Fig. 5.11 shows the drain current versus the front gate voltage of the accumulation-mode SOI PMOS device based on the analytical model and the experimental data [5][21]. As shown in the figure, as $|V_{G1}|$ is large enough, the device is operating in Case 4 for a small $|V_D|$ and in Case 7 for a large $|V_D|$. As $|V_{G1}|$ is small, the device is operating in Case 1 (subthreshold). In transition, the device is operating in other cases. As shown in the figure, the transition region is more complicated for a small $|V_D|$. From the figure, for $V_D = -2.5V$, its threshold voltage becomes less negative as compared to the $V_D = -0.1V$ one.

5.2 Capacitance Model

For an SOI NMOS device, in addition to the DC model, the capacitance model is also important for transient analysis. The equivalent capacitance model of an NMOS device is shown in Fig. 5.12. The capacitance model of an SOI MOS device is composed of two intrinsic capacitances: the drain-gate capacitance (C_{DG}) and the

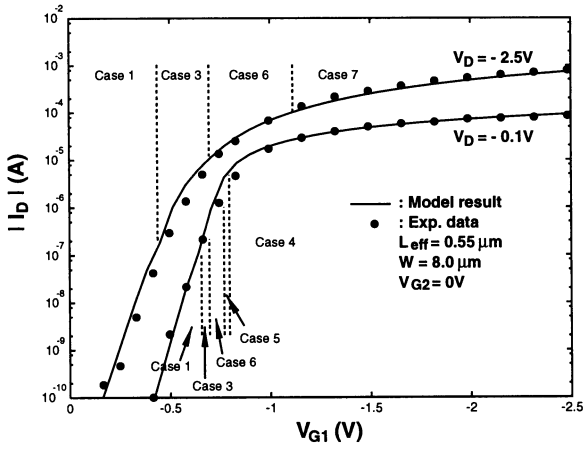


Figure 5.11: The drain current versus the front gate voltage of the accumulation-mode SOI PMOS device based on the analytical model and the experimental data.

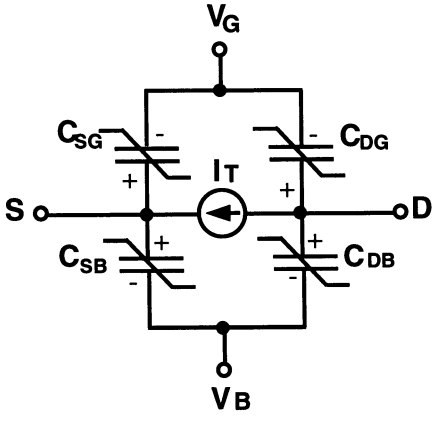


Figure 5.12: The capacitance model of an SOI NMOS device.

source-gate capacitance (C_{SG}) and the two extrinsic capacitances: the drain parasitic capacitance (C_{DB}) and the source parasitic capacitance (C_{SB}). The intrinsic capacitances affect the intrinsic performance of an MOS device. The extrinsic capacitances of the SOI MOS devices, which are much smaller than those of the bulk ones, are owing to the parasitic capacitances at the source/drain. The extrinsic parasitic capacitances also affect the speed performance of the device.

The drain-gate capacitance (C_{DG}) and the source-gate capacitance (C_{SG}) are defined as[29]:

$$\begin{aligned} C_{SG} &= \frac{\partial Q_S}{\partial V_G}, \\ C_{DG} &= \frac{\partial Q_D}{\partial V_G}, \end{aligned} \tag{5.22}$$

where Q_S/Q_D is the source/drain charge, which is the partitioned total charge under the gate. Definition of Q_S and Q_D was a difficult task for developing a consistent capacitance model for bulk MOS devices in 1970s. At the beginning, C_{SG} and C_{DG} were regarded as linear: $C_{SG} = C_{GS}$, $C_{DG} = C_{GD}$. Thus, C_{SG} and C_{DG} were obtained by $C_{SG} = \frac{\partial Q_G}{\partial V_S}$ and $C_{DG} = \frac{\partial Q_G}{\partial V_D}$. However, C_{DG} and C_{SG} are not linear, hence reciprocity does not hold. The above definitions of C_{DG} and C_{SG} assuming reciprocity are wrong. In this section, C_{DG} and C_{SG} are derived from the current continuity equation.

Consider an SOI NMOS device. At location y in the channel of the device (y is the lateral channel direction), the current is:

$$I(y,t) = W\mu_n(y,t)Q_I(y,t)\frac{\partial V(y,t)}{\partial y}. \tag{5.23}$$

From the current continuity equation, in a small region dy at location y in the channel, in a unit time, the change of the total electrons in this region is equal to the gradient of the current profile:

$$\frac{\partial Q_I(y,t)}{\partial t} = -\frac{1}{W}\frac{\partial I(y,t)}{\partial y}. \tag{5.24}$$

Integrating the above equation from source ($y = 0$) to y, an indefinite integral is obtained:

$$I(0,t) = W\mu_n Q_I(y,t)\frac{\partial V}{\partial y} + W\int_0^y \frac{\partial Q_I(y',t)}{\partial t}dy'. \tag{5.25}$$

Reintegrating this indefinite integral Eq.(5.25) from source ($y = 0$) to drain ($y = L$), one obtains:

$$I(0,t) = \mu_n \frac{W}{L} \int_0^{V_D} Q(V(y), V_G) dV(y) + \frac{W}{L} \int_0^L \int_0^y \frac{\partial Q_I(y',t)}{\partial t} dy' dy. \quad (5.26)$$

From the above equation, the transient current of the source terminal can be expressed in terms of the transport current and the derivative of the source charge with respect to time:

$$I_S(t) \equiv I(0,t) = I_T(t) - \frac{dQ_S(t)}{dt}, \quad (5.27)$$

where the transport current (I_T) is dependent on the terminal voltages, which is identical to the DC drain current:

$$I_T = \mu_n \frac{W}{L} \int_0^{V_D} Q_I dV(y). \quad (5.28)$$

From Eqs.(5.26)&(5.27), the source charge is composed of a double integral:

$$Q_S(t) = -\frac{W}{L} \int_0^L \int_0^y Q_I(y',t) dy' dy. \quad (5.29)$$

Using integration by parts, the double integral in the source charge can be simplified as:

$$Q_S(t) = -W \int_0^L (1 - \frac{y}{L}) Q_I(y,t) dy, \quad (5.30)$$

where dy in the above equation can be expressed as:

$$dy = \frac{\mu_n W C_{ox}(V_G - V_T - V(y))}{I} dV(y). \quad (5.31)$$

From Eqs.(5.30)(5.31), the source charge can be obtained. The source charge can be regarded as the weighted sum of the total electrons in the channel. From Eq.(5.30), at a location closer to the source, the weight of the electron is larger. At source, the weight is equal to 1. At drain, the weight is equal to 0.

Using a similar method, the drain transient current is:

$$\begin{aligned} I_D(t) &= I_T(t) + \frac{dQ_D(t)}{dt}, \quad (5.32) \\ Q_D(t) &= -W \int_0^L \frac{y}{L} Q_I(y) dy, \end{aligned}$$

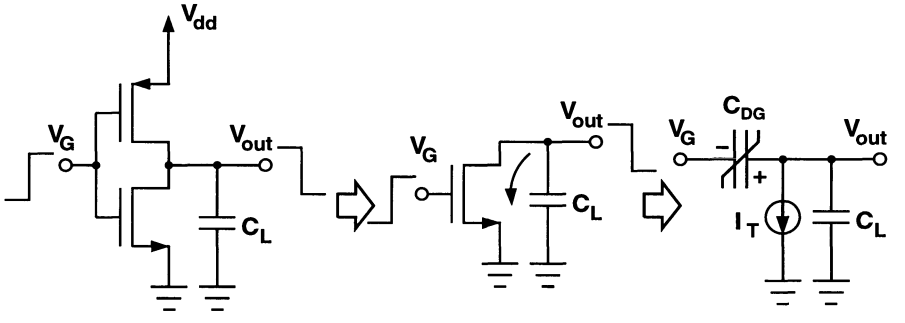


Figure 5.13: The equivalent circuit of the NMOS device for transient analysis.

where Q_D is the weighted total electrons in the channel. When computing Q_D, the electrons in the channel near the drain are weighted by a large factor and those far away from the drain are weighted by a small factor. The sum of Q_S and Q_D is equal to the quantity of the total electrons in the channel: $Q_S + Q_D = -W \int_0^L Q_I(y)dy$.

The gate-drain capacitance C_{GD} is defined as the derivative of the gate charge with respect to the drain voltage:

$$C_{GD} = \frac{\partial Q_G}{\partial V_D}, \tag{5.33}$$

where Q_G is the gate charge:

$$Q_G = C_{ox} W \int_0^L (V_G - V_T - V(y))dy. \tag{5.34}$$

C_{GD} is defined as the influence of the drain voltage in the gate charge. Due to the nonlinearity of the capacitances, C_{GD} is not equal to C_{DG}— the reciprocity does not hold. In analyzing the transient of a digital circuit, C_{DG} is more frequently used.

The capacitance model of an MOS device is used for transient analysis of an MOS circuit. As shown in Fig. 5.13, in a CMOS inverter circuit including an NMOS device and a PMOS device, the NMOS device is used to drive the output load during the pull-down transient. The input signal is usually imposed at the input gate electrode. The output voltage during the pull-down transient of the CMOS inverter circuit is to be calculated. Based on the equivalent circuit as shown in Fig. 5.13, writing the node equation at the output node, a differential equation in

terms of the output voltage is obtained:

$$\frac{dQ_D}{dt} + I_T(V_{out}, V_G) + C_L\frac{dV_{out}}{dt} = 0. \tag{5.35}$$

From the capacitance model, one obtains:

$$\frac{dQ_D}{dt} = \frac{\partial Q_D}{\partial V_G}\frac{dV_G}{dt} = C_{DG}\frac{dV_G}{dt}. \tag{5.36}$$

From Eqs.(5.37)&(5.35), one obtains a differential equation:

$$C_{DG}(V_{out}, V_G)\frac{dV_G}{dt} + I_T(V_{out}, V_G) + C_L\frac{dV_{out}}{dt} = 0. \tag{5.37}$$

Solving this differential equation, the transient waveform of the output voltage can be obtained.

5.3 Capacitance Model: Accumulation-Mode Devices

In this section, using the basic capacitance concept presented in the previous section, a capacitance model for the accumulation-mode SOI PMOS devices [30] is described. It will be shown that including the short-channel effect, velocity saturation, and channel-length modulation, the capacitance behavior of a submicron SOI accumulation-mode PMOS device is quite different from an inversion-mode one.

For an accumulation-mode SOI PMOS device, Fig. 5.14 shows the C_{GS} versus V_{GS} curves for various back gate biases[31]. As shown in the figure, when the back gate bias becomes more negative, the C_{GS} curve has two saturated portions with a two-step transition region, which is due to the buried channel in the silicon thin-film. With a positive back gate bias, the two-step transition region disappears. Instead, the transition region curve has a steeper slope.

Consider an accumulation-mode SOI PMOS device as shown in Fig. 5.15[30]. Before hole accumulation exists at the top silicon surface in the silicon thin-film– ($V_{G1} - V(y) \geq V_{FB1}$, where V_{G1} is the front gate voltage, V(y) is the potential at the top surface at location y, and V_{FB1} is the front-gate flat-band voltage), top and bottom surfaces are depleted. Solving the 1D Poisson's equation in the substrate

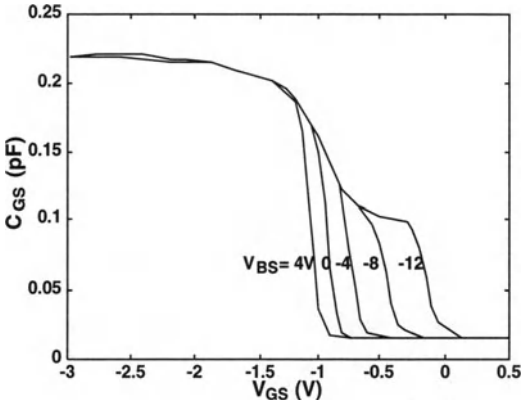


Figure 5.14: C_{GS} versus V_{GS} of an accumulation-mode SOI PMOS device with an aspect ratio of $W/L = 20\mu\text{m}/10\mu\text{m}$, biased at $V_{DS} = -50mV$.

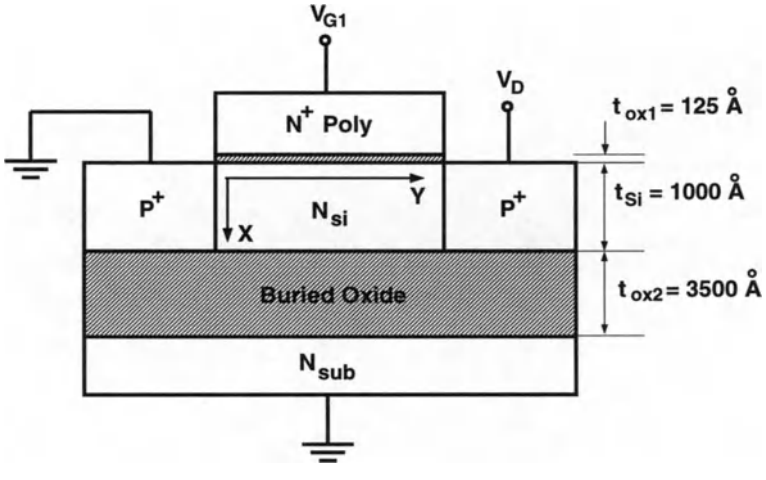


Figure 5.15: Cross section of the accumulation-mode SOI PMOS device under study.

direction, one obtains the depletion regions at the top and the bottom of the silicon thin-film [8] as:

$$X_{d1}(V(y)) = t_{si} \cdot [-\frac{C_{si}}{C_{ox1}} + \sqrt{(\frac{C_{si}}{C_{ox1}})^2 + \frac{2\epsilon_{si}}{qN_{si}t_{si}^2}(V_{G1} - V_{FB1} - V(y))}], \quad (5.38)$$

$$X_{d2}(V(y)) = t_{si} \cdot [-\frac{C_{si}}{C_{ox2}} + \sqrt{(\frac{C_{si}}{C_{ox2}})^2 + \frac{2\epsilon_{si}}{qN_{si}t_{si}^2}((V_{G2} + k_1 \cdot V_D) - V_{FB2} - V(y))}], \quad (5.39)$$

respectively. ($C_{ox1} = \epsilon_{ox}/t_{ox1}$, $C_{ox2} = \epsilon_{ox}/t_{ox2}$, $C_{si} = \epsilon_{si}/t_{si}$. t_{ox1} is the thickness of the front gate oxide. t_{ox2} is the thickness of the buried oxide. ϵ_{si} is the silicon permittivity. ϵ_{ox} is the oxide permittivity. V_{FB2} is the back-gate flat-band voltage.) Note that k_1 is used to reflect the influence of the drain voltage on the silicon thin-film via the buried oxide [22]. Since the thickness of the buried oxide is thick, the V(y) in Eq. (5.39) can be neglected. Therefore, $X_{d2} = X_{d2o} = X_{d2}(0)$. The amount of the total mobile charge, which is the holes in the neutral silicon thin-film, is

$$Q_{film} = qN_{si} \cdot (t_{si} - X_{d1} - X_{d2o}). \quad (5.40)$$

When $V_{G1} - V(y) < V_{FB1}$, the top depletion region disappears and holes are accumulated at the top surface. Therefore, the mobile charge contains the accumulated holes at the top surface (Q_{acc}) and the holes in the neutral silicon thin-film region (Q_{film}) as:

$$\begin{aligned} Q_{acc} &= -C_{ox1} \cdot [V_{G1} - V_{FB1} - V(y)], \\ Q_{film} &= qN_{si} \cdot (t_{si} - X_{d2o}). \end{aligned} \quad (5.41)$$

As described in the previous section, there are seven current conduction cases in the accumulation-mode SOI PMOS device biased at various conditions [21].

(a) Case 1

In Case 1, the silicon thin-film is fully depleted and the device is biased at subthreshold. Therefore, the charge on the front gate and the effective source and drain charges are

$$\begin{aligned} Q_{G1} &\simeq WL_{eff} \cdot qN_{si} \cdot t_{si}, \\ Q_{S1} &= 0, \\ Q_{D1} &= 0. \end{aligned} \quad (5.42)$$

In this case, although nearly no mobile charge exists in the channel, the fringing electric field may induce some additional charge, which will be described in (e).

(b) Case 2

In Case 2, current conduction is via the neutral region in the center. Therefore, considering the lateral electric field dependent mobility [23], the drain current is:

$$I_{D2} = \frac{\mu_{b0}}{1 - \frac{\mu_{b0}}{v_{sat}}\frac{\partial V}{\partial y}} \cdot W Q_{film}(y) \cdot \frac{\partial V}{\partial y}, \tag{5.43}$$

where μ_{b0} is the low-field mobility, v_{sat} is the hole saturated velocity, and Q_{film} is as described in Eq. (5.40). Multiplying both sides of Eq. (5.43) by $1 - \frac{\mu_{b0}}{v_{sat}}\frac{\partial V}{\partial y}$, from Eq. (5.40), and integrating the equation, one obtains: $I_{D2} = \frac{W}{L_{eff}} \frac{\mu_{b0}}{1 - \frac{\mu_{b0}}{v_{sat}}\frac{V_D}{L_{eff}}} \cdot qN_{si} \cdot [(t_{si} - X_{d2o}) \cdot V_D + t_{si} \cdot P(V_D) - t_{si} \cdot P(0)]$, where $P(V) = \frac{C_{si}}{C_{ox1}} V + \frac{qN_{si}t_{si}^2}{3\epsilon_{si}} \cdot [(\frac{C_{si}}{C_{ox1}})^2 + \frac{2\epsilon_{si}}{qN_{si}t_{si}^2} \cdot (V_{G1} - V_{FB1} - V)]^{\frac{3}{2}}$.

Similarly, from Eq. (5.43), using $\frac{\partial y}{\partial V} = (\frac{\partial V}{\partial y})^{-1}$, and integrating the equation, one obtains: $y = C + \frac{A}{b} \cdot (a + b \cdot V) + \frac{2B}{3b} \cdot (a + b \cdot V)^{\frac{3}{2}}$, where $A = \frac{\mu_{b0}}{v_{sat}} + \mu_{b0}\frac{W}{I_{D2}} \cdot qN_{si} \cdot (t_{si} - X_{d2o}) + \mu_{b0}\frac{W}{I_{D2}}\frac{C_{si}}{C_{ox1}} \cdot qN_{si} \cdot t_{si}$, $B = -\mu_{b0}\frac{W}{I_{D2}} \cdot qN_{si}$, $a = (\frac{C_{si}}{C_{ox1}}t_{si})^2 + \frac{2\epsilon_{si}}{qN_{si}} \cdot (V_{G1} - V_{FB1})$, $b = -\frac{2\epsilon_{si}}{qN_{si}}$, $C = -\frac{Aa}{b} - \frac{2B}{3b}a^{\frac{3}{2}}$.

The front gate charge can be computed by counting the total space charge in the top depletion region ($0 < x < X_{d1}$):

$$\begin{aligned} Q_{G2}(I_{D2}, V_D) &= \int_0^{L_{eff}} W \cdot qN_{si}X_{d1} \cdot dy = \int_0^{V_D} W \cdot qN_{si}X_{d1} \cdot (\frac{\partial V}{\partial y})^{-1} dV, \qquad (5.44) \\ &= W \cdot qN_{si} \cdot [-\frac{C_{si}}{C_{ox1}}t_{si}A \cdot V_D + (A - \frac{C_{si}}{C_{ox1}}t_{si}B)\frac{2}{3b}((a + b \cdot V_D)^{\frac{3}{2}} - \\ &\quad a^{\frac{3}{2}}) + \frac{B}{2b}((a + b \cdot V_D)^2 - a^2)]. \end{aligned}$$

Based on the partitioned-charge method [32][33], from Eq. (5.40), one obtains the source charge by integrating the weighted mobile charge in the lateral channel as:

$$\begin{aligned} Q_{S2}(I_{D2}, V_D) &= \int_0^{L_{eff}} W \cdot Q_{film}(y) \cdot (1 - \frac{y}{L_{eff}}) \cdot dy, \qquad (5.45) \\ &= \int_0^{V_D} W \cdot qN_{si} \cdot (t_{si} - X_{d2o} - X_{d1}) \cdot (1 - \frac{y}{L_{eff}}) \cdot (\frac{\partial V}{\partial y})^{-1} dV, \\ &= W \cdot qN_{si} \cdot [AD(1 - \frac{C}{L_{eff}}) \cdot V_D + (BD(1 - \frac{C}{L_{eff}}) - A(1 - \frac{C}{L_{eff}}))\frac{2}{3b} \cdot \end{aligned}$$

$$((a+b\cdot V_D)^{\frac{3}{2}}-a^{\frac{3}{2}})-(\frac{A^2D}{bL_{eff}}+B(1-\frac{C}{L_{eff}}))\cdot\frac{1}{2b}((a+b\cdot V_D)^2-a^2)+$$
$$(\frac{A^2}{bL_{eff}}-\frac{2ABD}{3bL_{eff}}-\frac{ABD}{bL_{eff}})\cdot\frac{2}{5b}((a+b\cdot V_D)^{\frac{5}{2}}-a^{\frac{5}{2}})+(\frac{2AB}{3bL_{eff}}+\frac{AB}{bL_{eff}}-$$
$$\frac{2B^2D}{3bL_{eff}})\frac{1}{3b}((a+b\cdot V_D)^3-a^3)+\frac{2B^2}{3bL_{eff}}\frac{2}{7b}((a+b\cdot V_D)^{\frac{7}{2}}-a^{\frac{7}{2}})],$$

where $D=t_{si}-X_{d2o}+\frac{C_{si}}{C_{ox1}}t_{si}$. Similarly, the drain charge is computed by integrating the weighted mobile charge in the lateral channel as:

$$\begin{aligned}
Q_{D2}(I_{D2},V_D) &= \int_0^{L_{eff}} W\cdot Q_{film}(y)\cdot\frac{y}{L_{eff}}\cdot dy, \qquad (5.46)\\
&= \int_0^{V_D} W\cdot qN_{si}(t_{si}-X_{d2o}-X_{d1})\cdot\frac{y}{L_{eff}}\cdot(\frac{\partial V}{\partial y})^{-1}dV,\\
&= W\cdot qN_{si}\cdot[\frac{ADC}{L_{eff}}V_D+(\frac{BDC}{L_{eff}}-\frac{AC}{L_{eff}})\frac{2}{3b}((a+b\cdot V_D)^{\frac{3}{2}}-a^{\frac{3}{2}})+\\
&\quad(\frac{A^2D}{bL_{eff}}-\frac{BC}{L_{eff}})\cdot\frac{1}{2b}((a+b\cdot V_D)^2-a^2)+(\frac{2ABD}{3bL_{eff}}-\frac{A^2}{bL_{eff}}+\frac{ABD}{bL_{eff}})\cdot\\
&\quad\frac{2}{5b}((a+b\cdot V_D)^{\frac{5}{2}}-a^{\frac{5}{2}})+(\frac{2B^2D}{3bL_{eff}}-\frac{2AB}{3bL_{eff}}-\frac{AB}{bL_{eff}})\frac{1}{3b}((a+b\cdot V_D)^3-\\
&\quad a^3)-\frac{2B^2}{3bL_{eff}}\frac{2}{7b}((a+b\cdot V_D)^{\frac{7}{2}}-a^{\frac{7}{2}})].
\end{aligned}$$

(c) Case 3

Case 3 is similar to Case 2 except that near the drain prepinchoff velocity saturation exists. Using a similar method in the previous section, at the onset of the prepinchoff velocity saturation, its potential is V_{Dsat1}. The length of the post-saturation region is ΔL. Using the method for Case 2, Q_{G3}, Q_{S3}, and Q_{D3} can be computed by considering both the pre-saturation ($0<y<L_{eff}-\Delta L$)and post-saturation ($L_{eff}-\Delta L<y<L_{eff}$) regions. In the post-saturation region, a uniform charge distribution is assumed [34].

$$\begin{aligned}
Q_{G3} &= \int_0^{L_{eff}-\Delta L} W\cdot qN_{si}X_{d1}\cdot dy+\int_{L_{eff}-\Delta L}^{L_{eff}} W\cdot qN_{si}X_{d1}(V_{Dsat1})\cdot dy, \qquad (5.47)\\
&= Q_{G2}(I_{D3},V_{Dsat1})+WqN_{si}\cdot X_{d1}(V_{Dsat1})\cdot\Delta L,\\
Q_{S3} &= \int_0^{L_{eff}-\Delta L} W\cdot Q_{film}(y)\cdot(1-\frac{y}{L_{eff}})\cdot dy+
\end{aligned}$$

$$\begin{aligned}
& \int_{L_{eff}-\Delta L}^{L_{eff}} W \cdot Q_{film}(L_{eff}-\Delta L)\cdot(1-\frac{y}{L_{eff}})\cdot dy, \\
= \; & Q_{S2}(I_{D3},V_{Dsat1}) + WqN_{si}\cdot[t_{si}-X_{d1}(V_{Dsat1})-X_{d2o}]\cdot\frac{\Delta L^2}{2L_{eff}}, \\
Q_{D3} = \; & \int_0^{L_{eff}-\Delta L} W\cdot Q_{film}(y)\cdot\frac{y}{L_{eff}}\cdot dy + \int_{L_{eff}-\Delta L}^{L_{eff}} W\cdot Q_{film}(L_{eff}-\Delta L)\cdot\frac{y}{L_{eff}}\cdot dy, \\
= \; & Q_{D2}(I_{D3},V_{Dsat1}) + WqN_{si}\cdot[t_{si}-X_{d1}(V_{Dsat1})-X_{d2o}]\cdot(1-\frac{\Delta L}{2L_{eff}})\Delta L.
\end{aligned}$$

(d) Case 4

In Case 4, the top depletion region disappears. In addition, hole accumulation exists at the top surface. Current conduction is via the neutral channel in the center and the hole-accumulated channel at top. Considering the surface scattering mobility for the top hole-accumulated channel [24], the drain current is:

$$\begin{aligned}
I_{D4} &= \frac{\mu_{b0}}{1-\frac{\mu_{b0}}{v_{sat}}\frac{\partial V}{\partial y}}\cdot WQ_{film}\cdot\frac{\partial V}{\partial y} + \frac{\mu_{s0}}{1-\frac{\mu_{s0}}{v_{sat}}\frac{\partial V}{\partial y}}\cdot WQ_{acc}\cdot\frac{\partial V}{\partial y}, \qquad (5.48)\\
&\simeq \frac{\mu_{b0}}{1-\frac{\mu_{s0}}{v_{sat}}\frac{\partial V}{\partial y}}\cdot\frac{1-\frac{\mu_{s0}}{v_{sat}}\frac{V_D}{L_{eff}}}{1-\frac{\mu_{b0}}{v_{sat}}\frac{V_D}{L_{eff}}}\cdot WQ_{film}\cdot\frac{\partial V}{\partial y} + \frac{\mu_{s0}}{1-\frac{\mu_{s0}}{v_{sat}}\frac{\partial V}{\partial y}}\cdot WQ_{acc}\cdot\frac{\partial V}{\partial y},
\end{aligned}$$

where μ_{s0} is the low-field surface mobility: $\mu_{s0}=k_2\mu_{b0}/(1-\theta(V_{G1}-V_{FB1}))$. Using a similar approach as for Case 2, one obtains: $y=G\cdot V+\frac{H}{2}\cdot V^2$, where $G=\frac{\mu_{s0}}{v_{sat}}+\frac{W}{I_{D4}}\cdot\mu_{b0}\frac{1-\frac{\mu_{s0}}{v_{sat}}\frac{V_D}{L_{eff}}}{1-\frac{\mu_{b0}}{v_{sat}}\frac{V_D}{L_{eff}}}\cdot qN_{si}\cdot(t_{si}-X_{d2o})+\frac{W}{I_{D4}}\cdot\mu_{s0}(-C_{ox1})\cdot(V_{G1}-V_{FB1})$, $H=\frac{W}{I_{D4}}\cdot\mu_{s0}\cdot C_{ox1}$. From Eqs.(5.40), in Case 4, the gate charge can be computed by counting the total accumulated holes at the top surface:

$$\begin{aligned}
Q_{G4}(I_{D4},V_D) &= \int_0^{L_{eff}} -W\cdot Q_{acc}(y)\cdot dy, \qquad (5.49)\\
&= \int_0^{V_D} W\cdot C_{ox1}\cdot[V_{G1}-V_{FB1}-V]\cdot(\frac{\partial V}{\partial y})^{-1}dV, \\
&= W\cdot C_{ox1}\cdot[(GV_{G1}-GV_{FB1})\cdot V_D+\frac{1}{2}(HV_{G1}-HV_{FB1}-G)\cdot V_D^2- \\
&\quad \frac{1}{3}H\cdot V_D^3].
\end{aligned}$$

Similarly, from Eqs.(5.40), the source charge in Case 4 is:

$$\begin{aligned} Q_{S4}(I_{D4}, V_D) &= \int_0^{L_{eff}} W \cdot [Q_{film}(y) + Q_{acc}(y)] \cdot (1 - \frac{y}{L_{eff}}) \cdot dy, \qquad (5.50) \\ &= \int_0^{V_D} W \cdot [qN_{si} \cdot (t_{si} - X_{d2o}) - C_{ox1} \cdot (V_{G1} - V_{FB1} - V)] \cdot (1 - \frac{y}{L_{eff}}) \cdot \\ &\quad \cdot (\frac{\partial V}{\partial y})^{-1} dV, \\ &= W \cdot [GM \cdot V_D + \frac{1}{2}(GC_{ox1} - \frac{G^2 M}{L_{eff}} + HM) \cdot V_D^2 + \frac{1}{3}(HC_{ox1} - \frac{3GHM}{2L_{eff}} \\ &\quad - \frac{G^2 C_{ox1}}{L_{eff}}) \cdot V_D^3 - \frac{1}{4}(\frac{3GHC_{ox1}}{2L_{eff}} + \frac{H^2 M}{2L_{eff}}) \cdot V_D^4 - \frac{H^2 C_{ox1}}{10L_{eff}} \cdot V_D^5], \end{aligned}$$

where $M = -C_{ox1} \cdot (V_{G1} - V_{FB1}) + qN_{si} \cdot (t_{si} - X_{d2o})$. Similarly, the drain charge for Case 4 is:

$$\begin{aligned} Q_{D4}(I_{D4}, V_D) &= \int_0^{L_{eff}} W \cdot [Q_{film}(y) + Q_{acc}(y)] \cdot \frac{y}{L_{eff}} \cdot dy, \qquad (5.51) \\ &= \int_0^{V_D} W \cdot [qN_{si} \cdot (t_{si} - X_{d2o}) - C_{ox1} \cdot (V_{G1} - V_{FB1} - V)] \cdot \frac{y}{L_{eff}} \cdot \\ &\quad (\frac{\partial V}{\partial y})^{-1} dV, \\ &= W \cdot [\frac{G^2 M}{2L_{eff}} \cdot V_D^2 + \frac{1}{3}(\frac{3GHM}{2L_{eff}} + \frac{G^2 C_{ox1}}{L_{eff}}) \cdot V_D^3 + \frac{1}{4}(\frac{3GHC_{ox1}}{2L_{eff}} + \\ &\quad \frac{H^2 M}{2L_{eff}}) \cdot V_D^4 + \frac{H^2 C_{ox1}}{10L_{eff}} \cdot V_D^5]. \end{aligned}$$

Cases 1-4 are the typical current conduction mechanisms in the accumulation-mode SOI PMOS device. Cases 5-7 can be regarded as extension from Cases 1-4. Specifically, in Case 5, the top accumulated channel is pinched off. Therefore, Case 5 is regarded as a combination of Cases 2 and 4. In Case 6, the surface accumulated channel is pinched off and the center channel has prepinchoff velocity saturation. Therefore, Case 6 can be regarded as a combination of Cases 3 and 4. In Case 7, both the top and the center channels have prepinchoff velocity saturation. Therefore, Case 7 can be regarded as extended from Case 4.

(e) Capacitance model

The capacitance of an MOS device can be regarded as the sum of the intrinsic capacitance and the fringing capacitance [34]:

$$C_{ij} = C_{ij}' + C_f \cdot (1 - 2 \cdot \frac{C_{ij}'}{C_{ox1} \cdot WL_{eff}}), \tag{5.52}$$

where C_{ij}' is the intrinsic capacitance, which is defined as:

$$C_{ij}' = -\frac{\partial Q_i}{\partial V_j}, \tag{5.53}$$

where i, j can be G,S,D. C_f is the fringing capacitance between source/drain and gate without considering the charge shield effect of mobile charge [35]:

$$C_f = \frac{2\epsilon_{si}W}{\pi} \cdot log[1 + \frac{1.5 \cdot t_{si}}{t_{ox1}} sin(\frac{\pi\epsilon_{ox}}{2\epsilon_{si}})]. \tag{5.54}$$

In this section, an analytical capacitance model for accumulation-mode SOI PMOS devices has been derived.

The accumulation-mode SOI PMOS device under study [5] has the parameters as shown in Table 5.1 of section 5.1. It has an effective channel length of 0.55μm, a front oxide of 125Å, a buried oxide of 3500Å. The doping density of the 1000Å silicon thin-film is $4 \times 10^{16}\text{cm}^{-3}$. Fig. 5.16 shows C_{GS},C_{GD},C_{SG},C_{DG} versus the front gate voltage V_{G1} of the accumulation-mode PMOS device with a channel length of 0.55μm (left) and 10μm (right)[30]. As shown in the figure, for the long-channel device, at $V_{G1} = 0$, the value of its capacitances is zero. On the other hand, for the short-channel device, the value of its capacitances at $V_{G1} = 0$ is not zero due to the fringing effect. As shown in the C_{GD} and C_{DG} figures, for the long-channel device, the transition from triode to saturation is sharp. Contrarily, for the short-channel device, the gradual transition from triode to saturation is owing to the velocity saturation and channel length modulation effects[36]. Fig. 5.17 shows the pull-up transient analysis of a CMOS inverter using the PMOS device described in this section and a capacitive load of 10fF [30]. Fig. 5.18 shows C_{GS}, C_{SG}, C_{GD}, and C_{DG} versus the front gate voltage of the short-channel accumulation-mode (a) and inversion-mode (b) PMOS devices. The donor density of the silicon thin-film in the inversion-mode device is $4 \times 10^{16}\text{cm}^{-3}$[30]. As shown in the figures, for the inversion-mode device, the transition from subthreshold to strong inversion is abrupt. On the other hand, for the accumulation-mode device, the transition is gradual (Case 3). In the inversion-mode device, the abrupt transition is due to

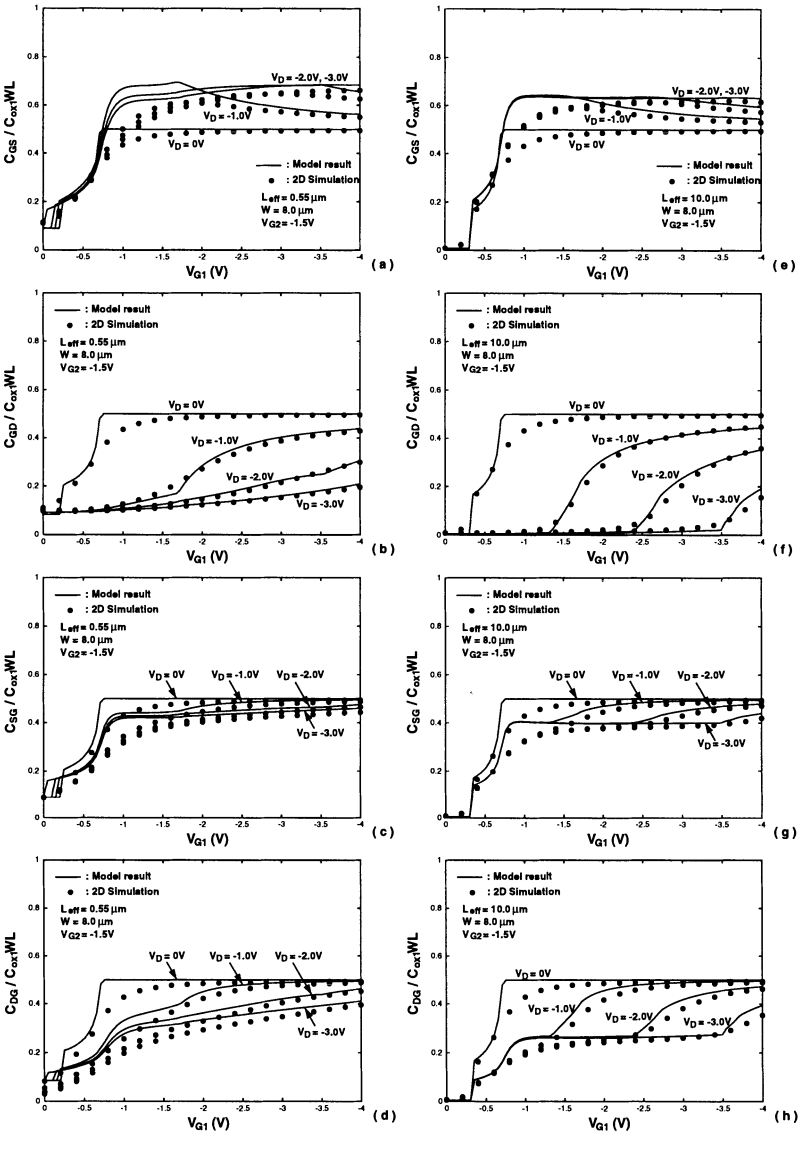


Figure 5.16: C_{GS}, C_{GD}, C_{SG}, C_{DG} versus front gate voltage of the SOI accumulation-mode PMOS device with a channel length of 0.55μm(a)-(d) and 10μm(e)-(h), biased at a back gate bias of $V_{G2} = -1.5V$, and a drain voltage of 0, -1V, -2V, -3V. The channel width is 8μm.

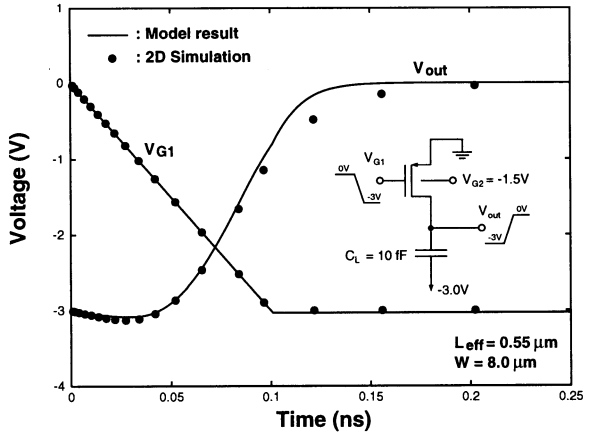


Figure 5.17: Pull-up transient analysis of a CMOS inverter using the PMOS device described in this section.

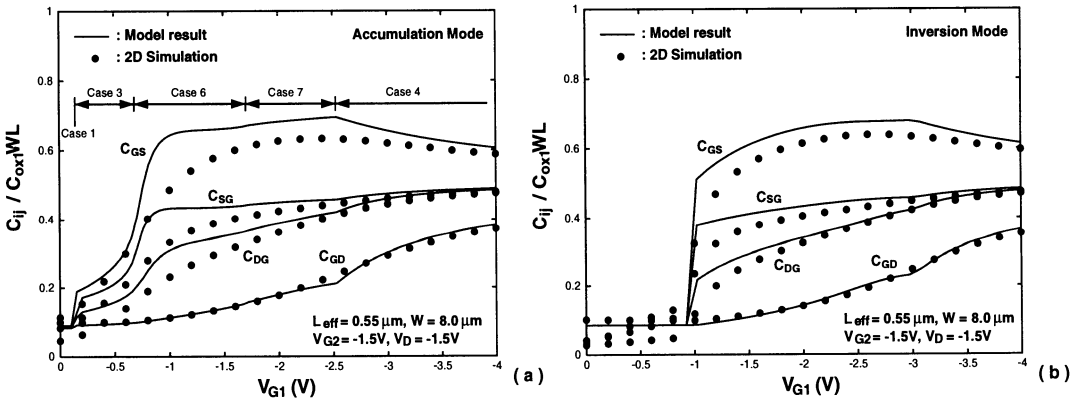


Figure 5.18: C_{GS}, C_{SG}, C_{GD}, C_{DG} versus the front gate voltage of the short-channel accumulation-mode (a) and inversion-mode (b) PMOS devices. The donor density of the silicon thin-film in the inversion-mode device is $4 \times 10^{16}\text{cm}^{-3}$.

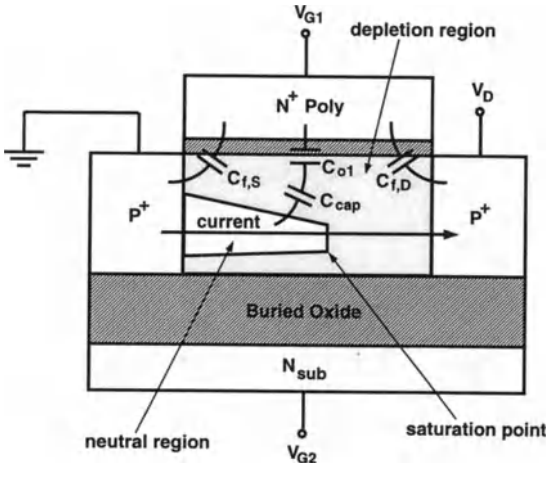


Figure 5.19: Description of the internal capacitances of the accumulation-mode SOI PMOS device biased in Case 3.

the surface channel effect. In the accumulation-mode device, the gradual transition is the result of the complicated buried channel effect. The gradual transition in Case 3 for the accumulation-mode device can be reasoned using Fig. 5.19[30]. As shown in the figure, in the accumulation-mode SOI PMOS device biased in Case 3, in addition to the fringing capacitances between the gate and the source/drain ($C_{f,S/D}$), there exists front gate oxide capacitance (C_{o1}) in series with the depletion capacitance between the front surface and the central neutral channel (C_{cap}). Due to the series connection of C_{o1} and C_{cap}, the effective capacitance is decreased. As V_{G1} becomes more positive for turning off the device, the depletion region between the top surface and the central channel region widens. Therefore, the equivalent capacitance becomes smaller. As a result, it leads to the gradual transition in Case 3.

5.4 Capacitance Model: Inversion-Mode Devices

In the previous section, a capacitance model for the accumulation-mode SOI PMOS device has been presented. In this section, a capacitance model for the inversion-mode SOI PMOS device is described. The derivation of the capacitance model for the inversion-mode SOI PMOS device is similar to the case for the accumulation-mode one.

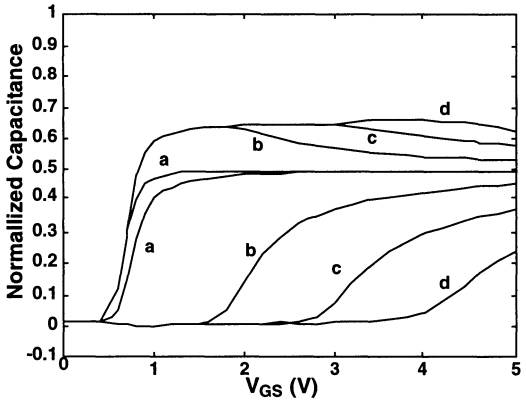


Figure 5.20: C_{GS} and C_{GD} versus V_{GS} of an inversion-mode SOI NMOS device with a front gate oxide of 340Å, a buried oxide of 4040Å, and a silicon thin-film of 839Å doped with a p-type doping density of $8 \times 10^{16}\text{cm}^{-3}$, biased at (a)$V_D = 0.05V$, (b) $V_D = 1.05V$, (c)$V_D = 2.05V$, (d)$V_D = 3.05V$, $V_S = 0$, $V_B = 0$.

Fig. 5.20 shows C_{GS} and C_{GD} versus V_{GS} of an inversion-mode SOI NMOS device with a front gate oxide of 340Å, a buried oxide of 4040Å, a silicon thin-film of 839Å doped with a p-type doping density of $8 \times 10^{16}\text{cm}^{-3}$, and an aspect ratio of $600\mu\text{m}/20\mu\text{m}$, biased at $V_D = 0.05, 1.05, 2.05, 3.05V$, $V_S = 0V$, $V_B = 0V$[37]. As shown in Fig. 5.20, the capacitance curves of the inversion-mode SOI NMOS device is similar to that of the bulk one. When the device turns on, the C_{GS} curve has a sudden rise. When the device enters the triode region, it has a gradual decay. In contrast, the C_{GD} curve has a non-zero value only when it enters the triode region.

In the following paragraphs, the capacitance model for the inversion-mode PMOS device is presented. The derivation of the inversion-mode capacitance model is similar to that of the accumulation-mode described in the previous section. The inversion-mode capacitance model can be divided into three regions—subthreshold, triode, and saturation regions.

(a) Subthreshold Region

In the subthreshold region ($V_G < V_T$), no mobile charge exists in the silicon thin-film—the channel is turned off. Therefore, the source charge and the drain charge

are: $Q_{S1} = Q_{D1} \cong 0$. On the other hand, the gate charge Q_{G1}, which is related to the space charge in the silicon thin-film, is equal to $Q_{G1} \cong -WL_{eff}qN_{si}t_{si}$.

(b) Triode Region

In the triode region ($V_{G1} > V_T$, $V_D < V_{DSAT}$), the channel turns on. However, near the drain region the channel does not pinch off. Following a similar approach as for the accumulation-mode device, the gate charge, the source charge, and the drain charge are:

$$\begin{aligned}
Q_{G2} \quad (I_{D2}, V_D) &= -WC_{ox1} \cdot \frac{\mu_{s0}}{v_{sat}} \cdot \frac{1}{2} \cdot [(V_{G1} - V_{TH} - V_D)^2 - (V_{G1} - V_{TH})^2] \quad (5.55) \\
&+ \frac{\mu_{s0} W^2 C_{ox1}^2}{I_{D2}} \cdot \frac{1}{3} \cdot [(V_{G1} - V_{TH} - V_D)^3 - (V_{G1} - V_{TH})^3] - WL_{eff}qN_{si}t_{si}, \\
Q_{S2} \quad (I_{D2}, V_D) &= WC_{ox1} \cdot [\frac{AD}{2} \cdot [(V_{G1} - V_{TH} - V_D)^2 - (V_{G1} - V_{TH})^2] + \\
&\frac{BD + AE}{3} \cdot [(V_{G1} - V_{TH} - V_D)^3 - (V_{G1} - V_{TH})^3] + \\
&\frac{CD + BE}{4} \cdot [(V_{G1} - V_{TH} - V_D)^4 - (V_{G1} - V_{TH})^4] + \\
&\frac{CE}{5} \cdot [(V_{G1} - V_{TH} - V_D)^5 - (V_{G1} - V_{TH})^5]], \\
Q_{D2} \quad (I_{D2}, V_D) &= WC_{ox1} \cdot [\frac{(1-A)D}{2} \cdot [(V_{G1} - V_{TH} - V_D)^2 - (V_{G1} - V_{TH})^2] + \\
&\frac{-BD + (1-A)E}{3} \cdot [(V_{G1} - V_{TH} - V_D)^3 - (V_{G1} - V_{TH})^3] - \\
&\frac{CD + BE}{4} \cdot [(V_{G1} - V_{TH} - V_D)^4 - (V_{G1} - V_{TH})^4] - \\
&\frac{CE}{5} \cdot [(V_{G1} - V_{TH} - V_D)^5 - (V_{G1} - V_{TH})^5]],
\end{aligned}$$

where $I_{D2} = -\frac{W}{L_{eff}} \frac{\mu_{s0}}{1 - \frac{\mu_{s0}}{v_{sat}} \frac{V_D}{L_{eff}}} \cdot C_{ox1} \cdot [(V_{G1} - V_{TH}) \cdot V_D - \frac{1}{2} V_D{}^2]$, $\mu_{s0} = \frac{k_2 \cdot \mu_{b0}}{1 - \theta \cdot (V_{G1} - V_{TH})}$, $A = 1 - \frac{\mu_{s0}}{L_{eff} v_{sat}} \cdot (V_{G1} - V_{TH}) + \frac{1}{2} \frac{\mu_{s0} W C_{ox1}}{L_{eff} I_{D2}} \cdot (V_{G1} - V_{TH})^2$, $B = \frac{\mu_{s0}}{v_{sat} L_{eff}}$, $C = -\frac{\mu_{s0} W C_{ox1}}{2 L_{eff} I_{D2}}$, $D = \frac{\mu_{s0}}{v_{sat}}$, and $E = -\frac{\mu_{s0} W C_{ox1}}{I_{D2}}$.

(c) Saturation Region

In the saturation region ($V_{G1} > V_T$, $V_D > V_{DSAT}$), the electrons in the channel near the drain travel at a saturated velocity. Therefore, the whole channel can

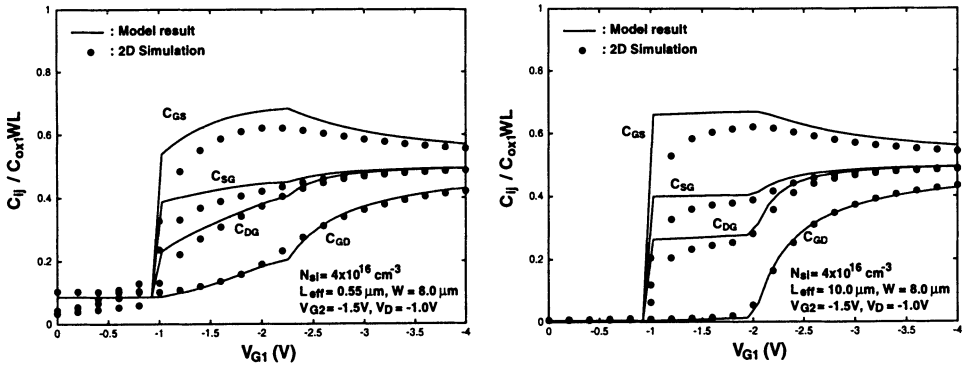


Figure 5.21: C_{GS}, C_{SG}, C_{DG}, C_{GD} versus the front gate voltage of an inversion-mode SOI PMOS device with a front gate oxide of 125Å, a buried oxide of 3500Å, a silicon thin-film of 1000Å doped with an n-type doping density of $4 \times 10^{16}\text{cm}^{-3}$, and aspect ratios of $8\mu\text{m}/10\mu\text{m}$ and $8\mu\text{m}/0.55\mu\text{m}$, biased at a back gate bias of -1.5V and $V_D = -1V$.

be divided into two regions—- the pre-saturation region and the post-saturation regions. The charge in these two regions should be considered simultaneously. For a similar approach as for the accumulation-mode devices, the gate charge, the source charge, and the drain charge are:

$$
\begin{aligned}
Q_{G3} &= Q_{G2}(I_{D3}, V_{Dsat}) + WC_{ox1} \cdot (V_{G1} - V_{TH} - V_{Dsat}) \cdot \Delta L, \\
Q_{S3} &= Q_{S2}(I_{D3}, V_{Dsat}) - WC_{ox1} \cdot (V_{G1} - V_{TH} - V_{Dsat}) \cdot \frac{\Delta L^2}{2L_{eff}}, \\
Q_{D3} &= Q_{D2}(I_{D3}, V_{Dsat}) - WC_{ox1} \cdot (V_{G1} - V_{TH} - V_{Dsat}) \cdot (1 - \frac{\Delta L}{2L_{eff}})\Delta L,
\end{aligned}
\tag{5.56}
$$

where $I_{D3} = -\frac{W}{L_{eff}-\Delta L}\frac{\mu_{s0}}{1-\frac{\mu_{s0}}{v_{sat}}\frac{V_{Dsat}}{L_{eff}-\Delta L}} \cdot C_{ox1} \cdot [(V_{G1} - V_{TH}) \cdot V_{Dsat} - \frac{1}{2}{V_{Dsat}}^2]$, $\Delta L = \lambda \cdot ln[-\frac{V_D - V_{Dsat}}{\lambda E_{sat}} + \sqrt{1 + (\frac{V_D - V_{Dsat}}{\lambda E_{sat}})^2}]$, $E_{sat} = \frac{k_3 v_{sat}}{\mu_{s0}(1-k_3)}$, $V_{Dsat} = \frac{1}{2k_3-1}[(k_3 - 1)(V_{G1} - V_{TH}) + \frac{k_3 v_{sat} L_{eff}}{\mu_{s0}} - \sqrt{[(k_3 - 1)(V_{G1} - V_{TH}) + \frac{k_3 v_{sat} L_{eff}}{\mu_{s0}}]^2 - (4k_3 - 2)\frac{k_3 v_{sat} L_{eff}}{\mu_{s0}} \cdot (V_{G1} - V_{TH})}]$.

Fig. 5.21 shows C_{GS}, C_{SG}, C_{DG}, C_{GD} versus the front gate voltage of an inversion-mode SOI PMOS device with a front gate oxide of 100Å, a buried oxide of 3500Å, a silicon thin-film of 1000Å doped with a p-type doping density of $4 \times 10^{16}\text{cm}^{-3}$ and

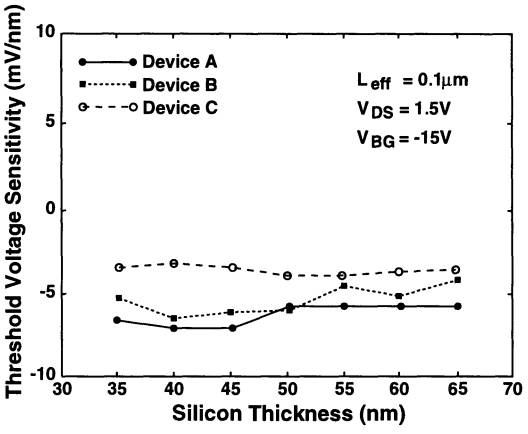


Figure 5.22: Threshold voltage sensitivity to the silicon thin-film thickness variation. Device A: $N_A = 3 \times 10^{15}cm^{-3}$ and $t_{ox} = 95Å$, Device B: $N_A = 5 \times 10^{16}cm^{-3}$ and $t_{ox} = 95Å$, Device C: $N_A = 3 \times 10^{15}cm^{-3}$ and $t_{ox} = 50Å$.

aspect ratios of $8\mu m/10\mu m$ and $8\mu m/0.55\mu m$, biased at a back gate bias of -1.5V and $V_D = -1V$. From Fig. 5.21, compared to the long-channel device, the capacitance curves of the short-channel device have a more gradual transition region from the triode region to the saturation region. In addition, when the device turns off, the capacitance curves have a non-zero value due to the fringing effect for the short-channel device. Compared to the accumulation-mode device, in the inversion-mode device its capacitance curves have a sudden jump in the transition region from turn-off to turn-on, instead of the gradual change as for the accumulation-mode case. This difference can be explained from the current conduction mechanism. In the inversion-mode device, the current conduction is via the surface channel only. However, in the accumulation-mode device, it is via the buried channel in addition to the surface channel.

5.5 Sensitivity

The trends on the fully-depleted SOI CMOS devices are toward using very thin silicon thin-films. With a very thin silicon thin-film, device second order effects can be further reduced. However, when the silicon thin-film is too thin, the threshold voltage of the SOI CMOS devices may be very sensitive to the silicon thin-film thickness. Fig. 5.22 shows the threshold voltage sensitivity to the silicon thin-film

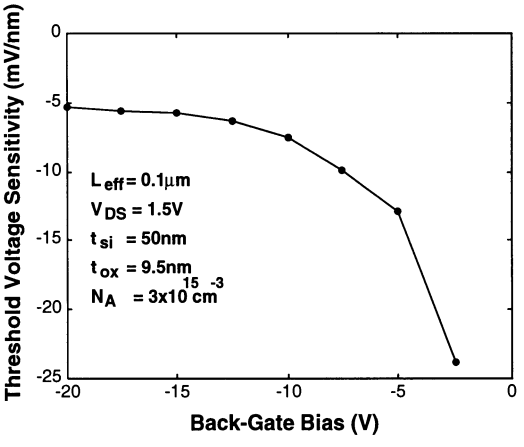


Figure 5.23: Threshold voltage sensitivity to the silicon thin-film thickness variation versus the back gate bias of an SOI NMOS device with a channel length of 0.1μm, a silicon thin-film of 500Å doped with an n-type doping density of $3 \times 10^{16}\text{cm}^{-3}$, a front gate oxide of 95Å, and a buried oxide of 3750Å, biased at $V_{DS} = 1.5V$.

thickness variation of three devices with different silicon thin-film doping densities and front gate oxide thicknesses[38]. Note that the applied back gate bias is -15V. As shown in the figure, when the front gate oxide thickness is reduced, the threshold voltage sensitivity with respect to the silicon thin-film thickness is decreased. On the other hand, a change in the silicon thin-film doping density does not alter the threshold voltage sensitivity substantially because of the negative back gate bias in this case. Fig. 5.23 shows the threshold voltage sensitivity to the silicon thin-film thickness variation versus the back gate bias of an SOI NMOS device with a channel length of 0.1μm, a silicon thin-film of 500Å doped with a p-type doping density of $3 \times 10^{15}\text{cm}^{-3}$, a front gate oxide of 95Å, and a buried oxide of 3750Å, biased at $V_{DS} = 1.5V$[38]. As shown in the figure, when the back gate bias becomes more negative, the threshold voltage sensitivity improves. When the back gate bias becomes more negative, the vertical electric field may increase. Hence, short-channel effect is reduced. Therefore, the threshold voltage sensitivity is reduced. When the back gate bias is smaller than -15V ($V_{GS} < -15V$), the threshold voltage sensitivity does not improve if the back gate bias is decreased further. This is due to the fact that at a very negative back gate bias, strong inversion may already exist at the substrate surface or hole accumulation may exist at the bottom of the silicon thin-film— back gate bias effect is saturated. Fig. 5.24 shows the threshold voltage

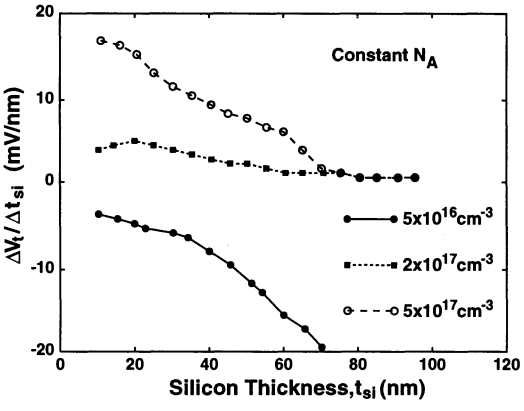


Figure 5.24: Threshold voltage sensitivity of a 0.2μm SOI NMOS device with a front gate oxide of 80Å, and a buried oxide of 3800Å, biased at $V_{DS} = 2.5V$ and $V_{BS} = 0V$.

sensitivity of a 0.2μm SOI NMOS device with a front gate oxide of 80Å, and a buried oxide of 3800Å, biased at $V_{DS} = 2.5V$ and $V_{BS} = 0V$[39]. At silicon thin-film doping densities of 5×10^{17}cm^3 and 2×10^{17}cm^{-3}, a higher silicon thin-film doping density leads to a higher threshold voltage sensitivity to the silicon thin-film thickness. At a silicon thin-film doping density of $5 \times 10^{16} cm^{-3}$, due to the drain-induced barrier lowering (DIBL), its threshold voltage sensitivity is even higher but in the negative direction. Therefore, if the silicon thin-film doping density is not too light, a thinner silicon thin-film leads to a higher threshold voltage sensitivity. If the silicon thin-film doping density is too light, a reverse trend on the threshold voltage sensitivity can be seen. Without a negative back gate bias, a change in the silicon thin-film doping density will alter the sensitivity substantially.

5.6 Floating Body Effects(I)

For an SOI MOS device, if its silicon thin-film is not fully depleted under a biasing condition, it is called partially-depleted SOI CMOS devices. Compared to the fully-depleted SOI MOS devices, partially-depleted devices usually have a thicker silicon thin-film. Due to the neutral region in the bottom portion of the silicon thin-film, floating body effect on the performance of a partially-depleted SOI CMOS devices is more serious, as compared to the fully-depleted device. Due to the floating body

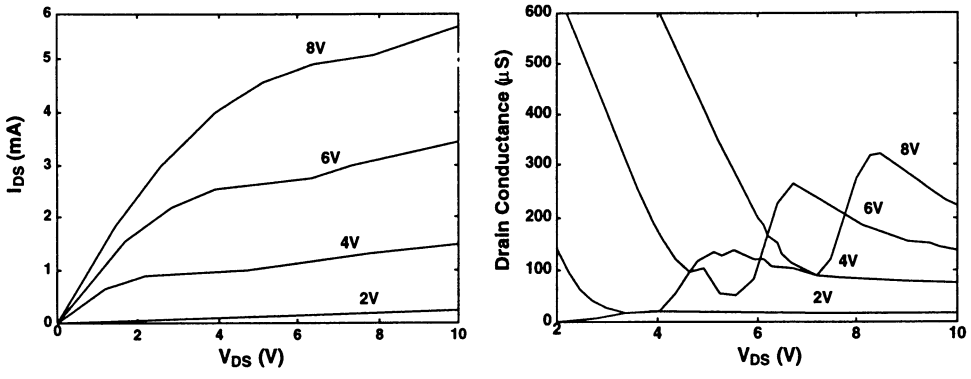


Figure 5.25: IV and output conductance characteristics of a partially-depleted SOI NMOS device.

effect, the parasitic bipolar device affects the performance of a partially-depleted SOI MOS device.

One of the floating body effects in a partially-depleted SOI MOS device is the kink effect. As shown in Fig. 5.25, an unsmooth transition in the saturation region can be identified[40]—kink effect, which is due to the floating body of the partially-depleted SOI NMOS device. A sudden rise in the output conductance can be seen. The kink effect is due to the hole current caused by the turn-on of the parasitic bipolar device, triggered by the accumulated holes, which are generated by impact ionization in the depletion region near the drain. As shown in the figure, when the gate voltage is small, the kink effect occurs at a low drain voltage[40]. Fig. 5.26 shows I_D versus V_{DS} characteristics of a partially-depleted NMOS device with a front gate oxide of 250Å, a buried oxide of 4500Å, and a silicon thin-film of 1000Å doped with a p-type doping density of $1.2 \times 10^{17}\text{cm}^{-3}$, biased at a front gate bias of $3V$[41]. As shown in Fig. 5.26(a), at a back gate bias of -5V, the kink effect is related to the channel length. A smaller channel length leads to an earlier occurrence of the kink effect. This is due to the fact, that when channel length becomes smaller, the electric field becomes larger. Hence, impact ionization becomes more serious. In addition, a smaller channel length also makes the parasitic BJT perform better. Therefore, the kink effect occurs at a smaller V_{DS}. As shown in Fig. 5.26(b), the kink effect is also related to the back gate bias. When the back gate bias becomes more negative, the kink effect is more visible since more holes can be accumulated

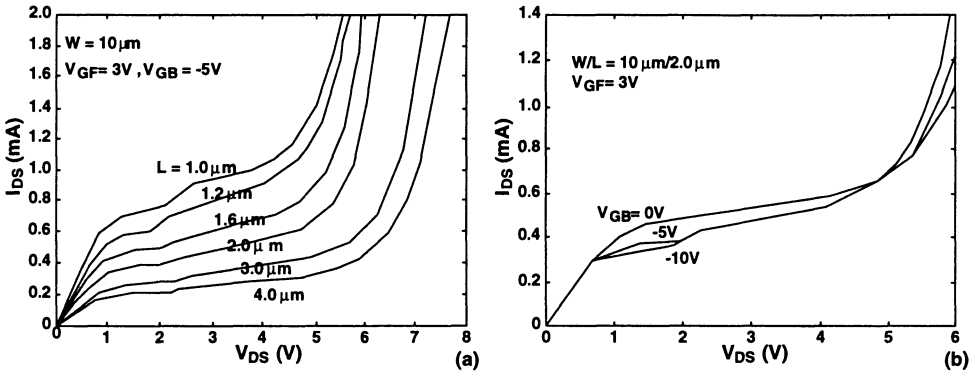


Figure 5.26: I_D versus V_{DS} characteristics of a partially-depleted NMOS device with a front gate oxide of 250Å, a buried oxide of 4500Å, and a silicon thin-film of 1000Å doped with a p-type doping density of $1.2 \times 10^{17}\text{cm}^{-3}$.

at the bottom of the silicon thin-film.

The sudden increase in the output conductance due to kink effect may degrade the performance of a circuit. Fig. 5.27 shows the I/O transfer curve and the small-signal gain versus the output voltage of an inverter using partially-depleted SOI MOS devices with body floating or grounded [42]. As shown in the figure, with floating body, the I/O transfer curve and the gain are worse due to the floating body induced kink effect. As shown in the figure, when the output voltage is high, the circuit performance is worse. With the body tied to ground, the performance is better—the kink effect has been suppressed.

In the next portion of this section, an analysis of the kink effect for partially-depleted SOI NMOS devices operating in strong inversion is presented. It will be shown that with a lighter doping density in the silicon thin-film and a thicker gate oxide, the onset of the kink effect occurs at a larger V_{DS}.

Due to the floating body structure and the parasitic BJT effect, the impact ionization effect of SOI NMOS devices is much more important than that of bulk NMOS devices [43]-[51]. Due to full depletion of the silicon thin-film, the source-bulk potential barrier is always small in a fully-depleted SOI device[52]. Therefore, accumulation of holes cannot take place in the body. As a result, the influence of the

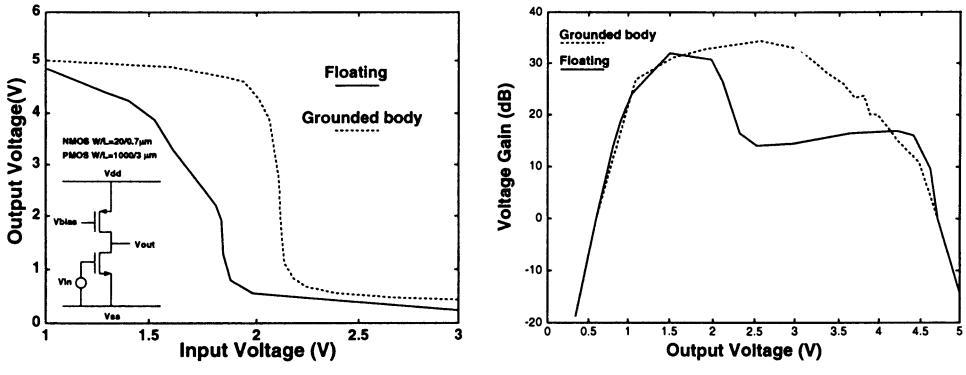


Figure 5.27: I/O transfer curve and small-signal gain versus output voltage of an inverter using partially-depleted SOI MOS devices with body floating or grounded.

body potential on the device behavior is small. In partially-depleted SOI NMOS devices, owing to the existence of the neutral region in the bulk, the source-bulk potential barrier is large. Therefore the generated holes due to impact ionization are easily trapped in the bulk. As a result, the potential barrier between the source and the bulk decreases. The hole current generated by impact ionization flows from bulk to source. Due to the increase in the bulk potential, the threshold voltage changes depending on the drain bias. This is the so-called kink effect [53]-[55]. In this section, an analytical kink effect model for partially-depleted SOI NMOS devices operating in strong inversion is derived[43].

Fig. 5.28 shows the cross section of a partially-depleted SOI NMOS device with a gate oxide thickness of $t_{ox1} = 250$Å, a silicon thin-film thickness of $t_{si} = 4500$Å, and a buried-oxide thickness of $t_{ox2} = 1\mu$m[43]. The silicon thin-film is doped with a p-type doping density of $N_A = 8 \times 10^{16}\text{cm}^{-3}$. The channel length is $L = 3\mu$m and the channel width is $W = 10\mu$m. Shaded area shows the neutral region in the bulk.

Fig. 5.29(a) shows the experimental drain current versus the drain voltage [56] of the partially-depleted SOI NMOS device as described in Fig. 5.28, biased at a gate voltage from 1V to 5V and a drain voltage from 0V to 6V. As shown in the figure, in the saturation region there are unsmooth transitions in the drain current due to impact ionization. This is the so-called kink effect. Fig. 5.29(b) shows the corresponding bulk-emitter voltage versus the drain voltage of this device[43].

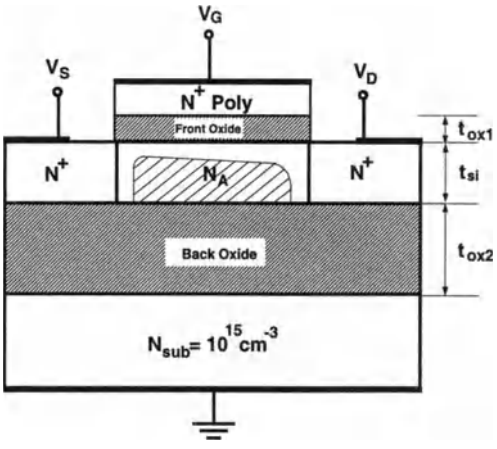


Figure 5.28: Cross section of the partially-depleted SOI NMOS device under study. It has a channel length 3μm, a gate-oxide thickness of 250Å, a buried-oxide thickness of 1μm and a silicon thin-film thickness of 4500Å doped with $8 \times 10^{16}\text{cm}^{-3}$.

From Figs.5.29(a)(b) we can identify that at the kink the bulk-emitter voltage of the parasitic bipolar device has an abrupt change. The bulk-emitter voltage can be expressed as the difference in the quasi-Fermi potential across the bulk-emitter junction: $V_{BE} = \phi_p - \phi_n$, where ϕ_p and ϕ_n are the hole and the electron quasi-Fermi potentials at the bulk-emitter junction, respectively. The sudden increase in the bulk-emitter voltage at the kink in the saturation region is due to accumulated holes caused by the injection of the hole current generated by impact ionization.

When imposing an external bias on the drain terminal, the emitter-bulk junction is forward biased. Most of the voltage drop is across the collector-bulk junction. The emitter current of the parasitic bipolar device is a combination of the recombination current and the electron diffusion current[57][58]:

$$I_E = I_{reco} exp(\frac{V_{BE}}{2kT/q}) + I_{ES} exp(\frac{V_{BE}}{kT/q}), \tag{5.57}$$

where $I_{reco} = \frac{qn_i A W_{be}}{2\tau_r}$, and $I_{ES} = \frac{qAD_{eB}n_i^2}{N_A W_B}$, q is the electron charge, k is Boltzmann constant, T is the temperature in Kelvin, n_i is the intrinsic concentration, τ_r is the recombination life time, $A = W(t_{si} - \sqrt{\frac{2\epsilon_{si}2\phi_f}{qN_A}})$ is the area of the cross section, ϵ_{si} is the silicon permittivity, $\phi_f = \frac{kT}{q} ln \frac{N_A}{n_i}$ is Fermi potential, $D_{eB} = \frac{kT}{q}\mu_{eff}$ is

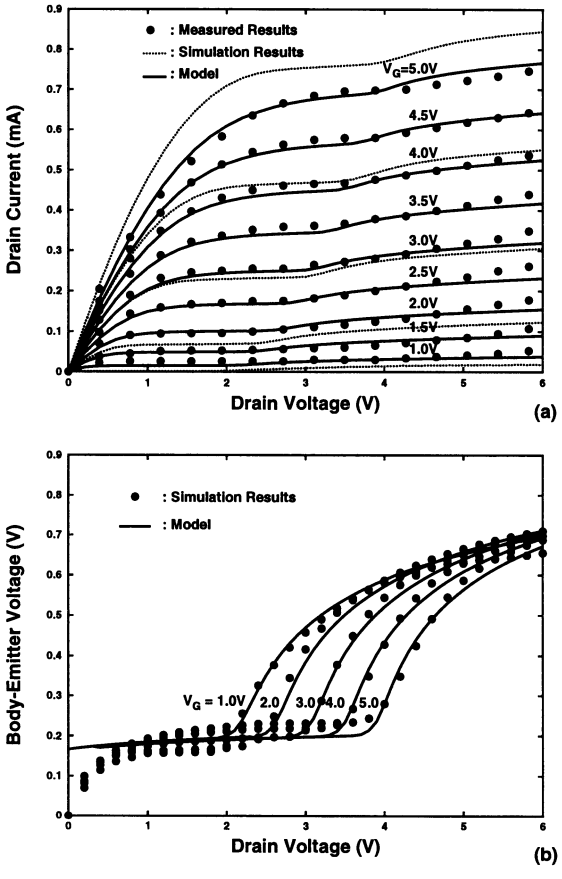


Figure 5.29: (a) The drain current versus the drain voltage of the partially-depleted SOI NMOS device, which has an aspect ratio of $10\mu m/3\mu m$, a front gate oxide of 250Å, a buried oxide of 10000Å, and a silicon thin-film of 4500Å doped with a p-type density of $8 \times 10^{16} cm^{-3}$. (b) The bulk-emitter voltage versus the drain voltage of the device.

the electron diffusion constant in the bulk, μ_{eff} is the electron effective mobility, $W_{be} \cong \sqrt{\frac{2\epsilon_{si}\phi_{bi}}{qN_A}}$ is the bulk-emitter junction width, $\phi_{bi} = \frac{kT}{q} ln \frac{N_A N_D}{n_i^2}$ is the built-in potential, N_D is the doping density of the source/drain region, $W_B = L - W_{be} - W_{bc}$ is the base width, and $W_{bc} \cong \sqrt{\frac{2\epsilon_{si}(\phi_{bi}+V_{DS})}{qN_A}}$ is the bulk-collector junction width.

Considering the effect from V_{BE}, the threshold voltage formula is:

$$V_T = V_{fb} + 2\phi_f + \gamma\sqrt{2\phi_f - V_{BE}}, \tag{5.58}$$

where $\gamma = \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}}$, and V_{fb} is the flat-band voltage. The channel current at the front surface is [25][59]:

$$I_{CH} = \frac{W}{L} \frac{\mu_{eff}}{1 + \theta(V_G - V_T) - \theta_B V_{BE}} C_{ox}((V_G - V_T)V_{dm} - \frac{1}{2}(1+\delta)V_{dm}^2), \tag{5.59}$$

where $\theta = \frac{\beta_\theta}{t_{ox1}}$, $V_{dm} = V_{DS} + V_{DSAT} - (V_{DS}^4 + V_{DSAT}^4)^{\frac{1}{4}}$, $V_{DSAT} = \frac{E_c L \frac{V_G - V_T}{(1+\delta)}}{E_c L + \frac{V_G - V_T}{(1+\delta)}}$, $\delta = \frac{\gamma}{2\sqrt{\phi_a + 2\phi_f - V_{BE}}}$, V_G is the gate voltage, β_θ and θ_B are empirical constants, and ϕ_a is used to compensate for the deviation caused by Taylor's expansion [25]. In deriving the analytical kink effect model, the analysis is divided into two sections: (1) $V_{DS} \leq V_{DSAT}$, and (2) $V_{DS} > V_{DSAT}$ (V_{DSAT} is the saturation drain voltage).

5.6.1 Triode Region ($V_{DS} \leq V_{DSAT}$)

For the partially-depleted SOI NMOS device biased in the triode region ($V_{DS} \leq V_{DSAT}$), there is no impact ionization existing in the silicon thin-film as shown in Fig. 5.30(a)[43]. Therefore, the floating body region can be regarded as two diodes connected back-to-back and the operation of the parasitic n-p-n bipolar device is weak. As shown in Fig. 5.30(a), since the collector-base junction is reverse biased, the collector current is due to generation current. Considering the avalanche effect in the collector-bulk junction, the collector current is [57][58]:

$$I_C = I_{gen} M_B, \tag{5.60}$$

where $I_{gen} = \frac{qn_i A W_{bc}}{2\tau_g}$, $M_B = 1/(1 - (\frac{V_{DS}}{V_{br}})^n)$, $V_{br} = \frac{\epsilon_{si} E_{br}^2}{2qN_A}$, $E_{br} = 2.5 \times 10^5 \times \frac{1+(logN_A - 14)^3}{14}$, τ_g is the generation lifetime, and n is a constant. At $V_{DS} \leq V_{DSAT}$, from Fig. 5.29(b), V_{BE} is small. Therefore, at the bulk-emitter junction, the emitter

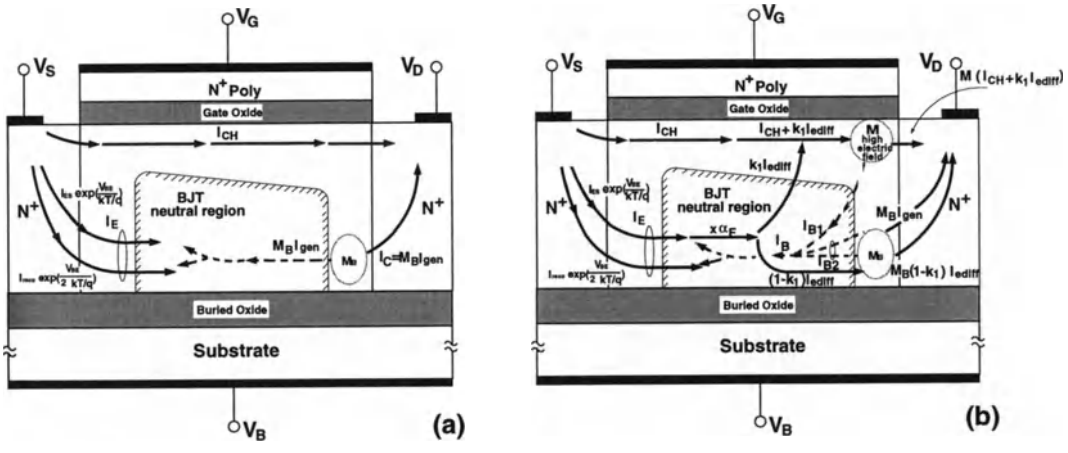


Figure 5.30: Cross section of the partially-depleted SOI NMOS device biased at (a) $V_{DS} \leq V_{DSAT}$, and (b) $V_{DS} > V_{DSAT}$.

current is dominated by recombination. From Eqs.(5.57)(5.60) and $I_E = I_C$, one obtains the bulk-emitter voltage as:

$$V_{BE} = 2\frac{kT}{q} ln(\frac{M_B I_{gen}}{I_{reco}}). \tag{5.61}$$

5.6.2 Saturation Region ($V_{DS} > V_{DSAT}$)

In the saturation region ($V_{DS} > V_{DSAT}$), as shown in Fig. 5.30(b), due to the impact ionization effect at the front surface near the drain in the silicon thin-film, hole current is injected into the body. At this moment, the floating body is like an active BJT. The hole current generated by impact ionization can function as the base current. Due to the high doping density of the emitter, the forward alpha α_F of the BJT connected in common base configuration is [57][60]: $\alpha_F = \frac{1}{cosh(W_B/L_{eB})}$, $L_{eB} = \sqrt{D_{eB}\tau_{eB}}$, $\tau_{eB} = \frac{\tau_0}{1+N_A/5\times10^{16}}$, where τ_0 is the hole lifetime. The electron diffusion current in the base is expressed as:

$$I_{ediff} = \alpha_F I_{ES} e^{\frac{V_{BE}}{kT/q}}, \tag{5.62}$$

which can be divided into two portions. k_1 portion of it is attracted by the front gate. $1-k_1$ portion of it is injected into the collector [48]. Therefore, from Eqs.(5.59)(5.62), and the hole current generated by the impact ionization in the front channel is:

$$I_{B1} = (M-1)(I_{CH} + k_1 I_{ediff}), \tag{5.63}$$

where M is the avalanche multiplication factor, which can be expressed as [61][62]: $M = 1 + \frac{\alpha}{\beta}(V_{DS} - V_{DSAT})exp(\frac{-\beta}{\sqrt{\frac{\epsilon_{ox}/\epsilon_{si}}{t_{ox1}X_c}(V_{DS}-V_{DSAT})}})$, where α and β are process-dependent parameters [48], ϵ_{ox} is the oxide permittivity, and $X_c = \sqrt{\frac{2\epsilon_{si}2\phi_f}{qN_A}}$ is the depth of depletion region. From Eqs.(5.60)(5.62), the hole current generated by the impact ionization at the collector-base junction is:

$$I_{B2} = M_B I_{gen} + (M_B - 1)(1 - k_1)I_{ediff}. \tag{5.64}$$

The base current(I_B) is the sum of I_{B1} and I_{B2}. The emitter current is composed of the base current and the electron diffusion current ($I_E = I_B + I_{ediff}$). Therefore, from Eqs.(5.63)(5.64)(5.57), V_{BE} can be obtained from the following equation:

$$\begin{aligned} I_{reco} \cdot & exp(\frac{V_{BE}}{2kT/q}) + (1 - \alpha_F - (M-1)k_1\alpha_F - (M_B - 1)(1-k_1)\alpha_F)I_{ES}exp(\frac{V_{BE}}{kT/q}) \\ & = M_B I_{gen} + (M-1)I_{CH}. \end{aligned} \tag{5.65}$$

Note that V_{DS} increases, V_{BE} may be larger than $2\phi_f$. Under this condition, the threshold voltage formula of Eq. (5.58) is not applicable. The threshold voltage formula should be modified as [63]:

$$V_T = V_{fb} + 2\phi_f - k_2(V_{BE} - 2\phi_f), \tag{5.66}$$

where k_2 is a fitting parameter [41][63]. The drain current is expressed as:

$$I_D = \begin{cases} I_{CH} + M_B I_{gen} & \text{for } V_{DS} \le V_{DSAT}, \\ (I_{CH} + k_1\alpha_F I_{ES}e^{(\frac{V_{BE}}{kT/q})})M + M_B(I_{gen} + (1-k_1)\alpha_F I_{ES}e^{(\frac{V_{BE}}{kT/q})}) & \text{for } V_{DS} > V_{DSAT}, \end{cases} \tag{5.67}$$

where generation and recombination effects have been neglected for the $V_{DS} \le V_{DSAT}$ case. Eq.(5.67) is the analytical kink effect model for the partially-depleted SOI NMOS devices.

The partially-depleted SOI NMOS device under study has a channel length of 3μm, a gate-oxide thickness of 250Å, a buried-oxide thickness of 1μm, a silicon thin-film thickness of 4500Å doped with a p-type doping density of $8 \times 10^{16}\text{cm}^{-3}$. τ_0, τ_g and τ_r depend on the trap density in the silicon thin-film. For a higher trap density in the silicon thin-film, $\tau_0 = 10ns$, $\tau_g = 10ns$ and $\tau_r = 250ns$ are smaller. $E_c = 3.6 \times 10^4 V/cm$ is the critical electric field related to the mobility model[25]. $\alpha = 1.4 \times 10^6\text{cm}^{-1}$ and $\beta = 3.773 \times 10^6\text{V/cm}$ are process-dependent parameters [48]. There are seven fitting parameters used in the analytical model. $\phi_a = 0.5$ is

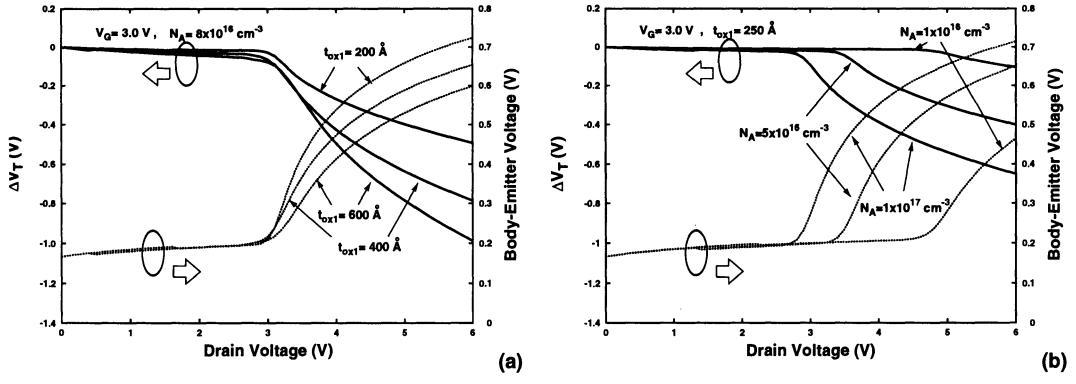


Figure 5.31: The deviation in the threshold voltage and the bulk-emitter voltage versus the drain voltage of the partially-depleted SOI NMOS device biased at V_G = 3V based on the analytical model. (a) The silicon thin-film doping density is $8 \times 10^{16}\text{cm}^{-3}$. The thickness of the gate-oxide varies from 200Å to 600Å. (b) The thickness of the gate oxide is 250Å. The silicon thin-film doping density varies from $1 \times 10^{16}\text{cm}^{-3}$ to $1 \times 10^{17}\text{cm}^{-3}$.

used to compensate for the deviation caused by Taylor's approximation [25]. $n = 6$ is a constant [57][58]. m is a constant [59]. $\beta_\theta = 0.00125$ and $\theta_B = 0.02$ are as in Ref.[25]. $k_1 = 0.8$. $k_2 = 0.5$.

The kink effect of the partially-depleted SOI NMOS device is also sensitive to the gate-oxide thickness and the silicon thin-film doping density. Fig. 5.31(a) shows the deviation in the threshold voltage and the bulk-emitter voltage as a function of the drain voltage at $V_G = 3\text{V}$ for a silicon thin-film doping density of $8 \times 10^{16}\text{cm}^{-3}$ and based on the analytical model[43]. The thickness of the gate oxide varies from 200Å to 600Å. As shown in the figure, for a thinner gate oxide, the bulk-emitter voltage becomes larger. This can be reasoned as follows. The avalanche multiplication factor is a function of the gate oxide thickness. For a thinner gate oxide, since the lateral field in the saturation region increases, the multiplication factor becomes larger. In the mean time, as the gate oxide becomes thinner according to Eq. (5.59), I_{CH} becomes larger. Due to the increase in the avalanche effect and the channel current, the influence of the impact ionization effect in the bulk increases. Therefore, for a thinner oxide, the bulk-emitter voltage becomes larger. Despite the increase in the bulk-emitter voltage for a thinner gate oxide, the change in the threshold voltage due to the kink effect is smaller. This can be understood using Eq. (5.58). For

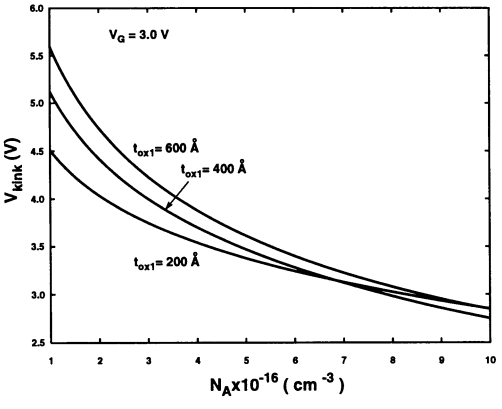


Figure 5.32: The triggering V_{DS} (V_{kink}) at the onset of the kink effect versus the silicon thin-film doping density of the partially-depleted SOI NMOS device for various gate-oxide thicknesses, based on the analytical model .

a thinner gate oxide, although the bulk-emitter voltage increases, the body effect coefficient ($\gamma = \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}}$) decreases. Therefore, as the gate oxide becomes thinner, the change in the threshold voltage due to the kink effect becomes smaller. As described before, the bulk-emitter voltage can be used to monitor the kink effect. As shown in Fig. 5.31(a), regardless of the thickness of the gate oxide, the onset of the kink effect seems to be triggered at the same V_{DS}. This means that the variation in the gate oxide thickness does not influence the triggering V_{DS} at the onset of the kink effect when the silicon thin-film doping density is high. Fig. 5.31(b) shows the deviation in the threshold voltage and the bulk-emitter voltage as a function of the drain voltage at $V_G = 3$V, based on the analytical model[43]. The silicon thin-film doping density varies from 1×10^{16}cm^{-3} to 1×10^{17}cm^{-3}. Different from the case described in Fig. 5.31(a), according to Fig.5.31(b), the triggering V_{DS} at the onset of the kink effect is strongly dependent on the silicon thin-film doping density. For a more heavily doped silicon thin-film, the onset of the kink effect occurs at a smaller triggering V_{DS}. In addition, for a more heavily doped silicon thin-film, the change in the threshold voltage due to the kink effect is larger.

The triggering V_{DS} formula at the onset of the kink effect can be found. Defining that at the triggering V_{DS} the bulk-emitter voltage is $V_{BE} = V_{BES} + \frac{1}{2}\frac{kT}{q}$, where V_{BES} is V_{BE} at $V_{DS} = V_{DSAT}$. Using Eqs. (5.59) (5.65), the triggering V_{DS} can be found. Based on the analytical model, Fig. 5.32 shows the triggering V_{DS} (V_{kink}) at

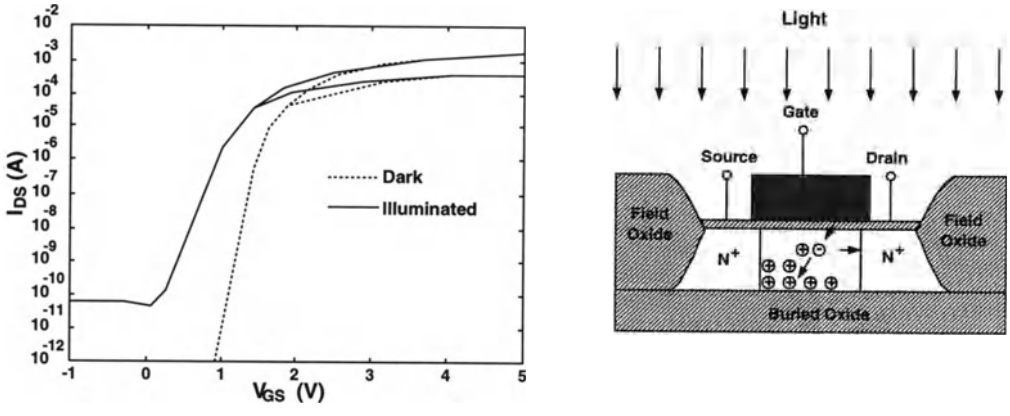


Figure 5.33: Turn-on characteristics for an illuminated and a nonilluminated partially-depleted SOI NMOS device with an aspect ratio of W/L = 50μm/3.2μm, biased at $V_{DS} = 0.1V$ and 1.5V.

the onset of the kink effect as a function of the silicon thin-film doping density at various gate-oxide thicknesses[43]. As shown in the figure, V_{kink} is inversely proportional to the silicon thin-film doping density. A more heavily doped silicon thin-film leads to a smaller triggering V_{kink}. As the doping density is high, the thickness of the gate oxide has little effect on the triggering V_{kink}. On the other hand, as the silicon thin-film is less heavily doped, the triggering V_{kink} is sensitive to the thickness of the gate oxide. A thinner gate oxide makes the kink effect to occur at a smaller V_{DS}.

In this section, the kink effect of partially-depleted SOI NMOS devices operating in strong inversion has been described. With a lighter doping density in the silicon thin-film and a thicker gate oxide, the onset of the kink effect occurs at a larger V_{DS}.

5.7 Floating Body Effects(II)

Due to the floating body, the subthreshold characteristics of the partially-depleted SOI MOS device is sensitive to the light illumination. Fig. 5.33 shows the turn-on characteristics for an illuminated and a non-illuminated partially-depleted SOI NMOS device with an aspect ratio of W/L = 50μm/3.2μm, biased at $V_{DS} = 0.1V$ and 1.5V[64]. As shown in the figure, when the partially-depleted SOI NMOS device with the floating body is illuminated with light, electron-hole pairs are generated in the silicon thin-film. The generated electrons move to drain to become

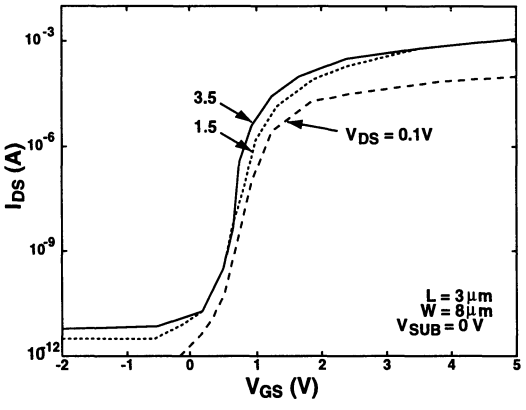


Figure 5.34: Subthreshold characteristics of a partially-depleted SOI NMOS device with an aspect ratio of $8\mu m/3\mu m$, a front gate oxide of 270Å, a buried oxide of 3500Å, and a silicon thin-film of 2800Å doped with a p-type density of of $5 \times 10^{16} cm^{-3}$.

the leakage current. The generated holes are accumulated at the bottom of the silicon thin-film. As a result, the potential of the floating body increases. Consequently, its threshold voltage is decreased and the subthreshold slope becomes worse.

Fig. 5.34 shows the subthreshold characteristics of a partially-depleted SOI NMOS device with an aspect ratio of $8\mu m/3\mu m$, a front gate oxide of 270Å, a buried oxide of 3500Å, and a silicon thin-film of 2800Å doped with a p-type density of $5 \times 10^{16} cm^{-3}$[65]. As shown in the figure, when the drain voltage exceeds 1.5V, the subthreshold slope becomes steeper as V_D becomes larger, which is contrary to the trend on the subthreshold slope for the bulk NMOS devices. For bulk NMOS devices, when the drain voltage becomes larger, due to the increased DIBL effect, the subthreshold slope becomes less steep. For partially-depleted NMOS devices, the situation is reverse due to the floating body effect. The subthreshold slope of a partially-depleted SOI NMOS device is also dependent on the gate length. Fig. 5.35 shows the subthreshold characteristics of a partially-depleted SOI NMOS device with various gate lengths[65]. As shown in the figure, due to the floating body, with a smaller gate length, its subthreshold slope becomes better, which is contrary to the short-channel effect case— when the channel length becomes smaller, its subthreshold slope becomes worse. With a smaller channel length, the electric field becomes larger, thus impact ionization becomes more serious. In addition, the parasitic BJT performs better when the channel length is shrunk. Thus, a better subthreshold

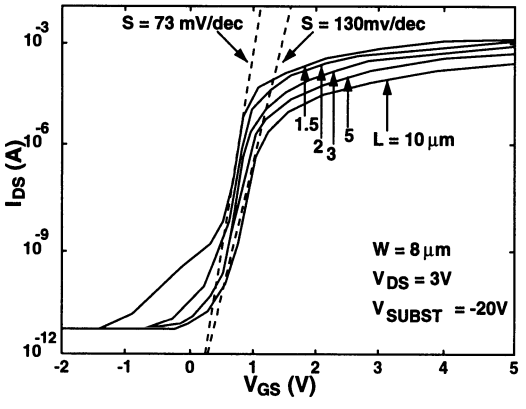


Figure 5.35: Subthreshold characteristics of a partially-depleted SOI NMOS device with various gate lengths.

slope can be seen when the channel length of a partially-depleted SOI NMOS device is shrunk.

Fig. 5.36 shows the drain current versus gate voltage characteristics of a partially-depleted SOI NMOS device with a front gate oxide of 250Å, a buried oxide of 5200Å, a silicon thin-film of 3400Å doped with a p-type density of $10^{17}cm^{-3}$, and a channel length of 1.2μm[66]. As shown in the figure, with a low leakage current, the kink effect dominates the subthreshold region. At a low-current level the leakage current dominates. As shown in Fig.5.37, leakage current is mainly due to the generation process of the traps near the buried oxide interface, which are produced by incorporation of the metal impurities into the silicon thin-film during the oxygen implantation for forming the buried oxide[66]. Combining the impact ionization effect in the high-electric field region, the leakage current may dominate in the partially-depleted SOI NMOS device. In a partially-depleted SOI NMOS device with a low leakage current, its subthreshold slope is dominated by the parasitic BJT effect and the impact ionization effect. Therefore, a higher drain voltage leads to a steeper subthreshold slope since the diffusion current of the parasitic BJT effect is more important.

For a partially-depleted SOI NMOS device, when the drain voltage is too large, the device cannot turn off. Fig. 5.38 shows the subthreshold characteristics of a partially-depleted SOI NMOS device with a front gate oxide 260Å, a silicon thin-

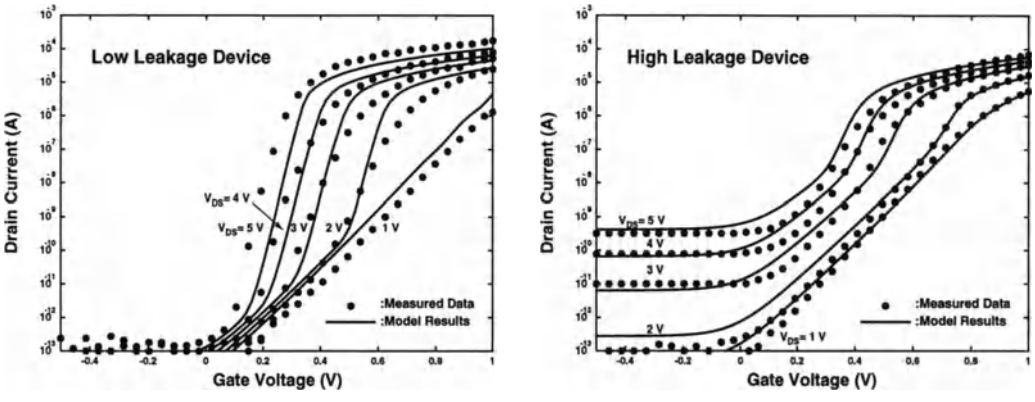


Figure 5.36: Drain current versus gate voltage characteristics of a partially-depleted SOI NMOS device with a front gate oxide of 250Å, a buried oxide of 5200Å, a silicon thin-film of 3400Å doped with a p-type density of $10^{17}cm^{-3}$, and a channel length of 1.2μm.

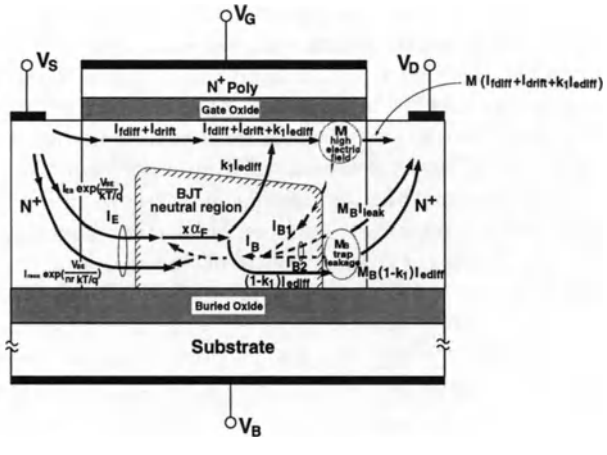


Figure 5.37: Current conduction mechanism in the partially-depleted SOI NMOS device biased in the subthreshold region.

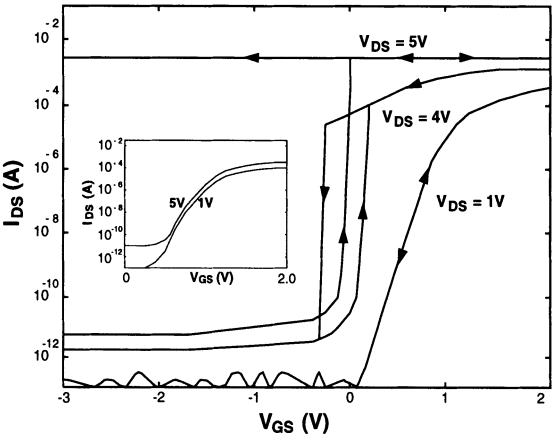


Figure 5.38: Subthreshold characteristics of a partially-depleted SOI NMOS device with a floating body, a front gate oxide of 260Å, a silicon thin-film doped with a p-type density of $10^{17}cm^{-3}$, and an aspect ratio of W/L = $7.2\mu m/1\mu m$. Inset shows the subthreshold characteristics with body grounded.

film doped with a p-type density of $10^{17}cm^{-3}$, and an aspect ratio of W/L = $7.2\mu m/1\mu m$[67]. As shown in the figure, at $V_D = 1V$, its subthreshold curve is normal. At $V_D = 4V$, a hysteresis may occur. When V_D becomes larger, the window of the hysteresis widens. At $V_D = 5V$, even when V_G switches from 2V to -3V, the device cannot be turned off due to the turn-on of the parasitic BJT. Once the device is latched, only by lowering V_D or by grounding the silicon thin-film body, the device can be recovered. This is the so-called single-transistor latch phenomenon, which occurs at high drain biases. The floating body results in a positive feedback between the impact ionization current, the body-to-source diode forward bias, and the transistor currents. At large drain voltages, this positive feedback can maintain a high drain-to-source current even when V_G is smaller than the threshold voltage.

Floating body effects of SOI MOS devices bring in lowering of the drain breakdown voltage, the kink effect, abnormal subthreshold slopes, current instability in switching, and enhanced leakage current. Using the bandgap engineering technique to implant germanium into the source region, the parasitic BJT effect can be reduced, hence the floating body effect can be lowered. Fig. 5.39 shows the $Si_{1-x}Ge_x$ source structure in an SOI NMOS device[68]. Germanium is implanted to form a Si-Ge structure as a narrow bandgapped material in the source area, which is about

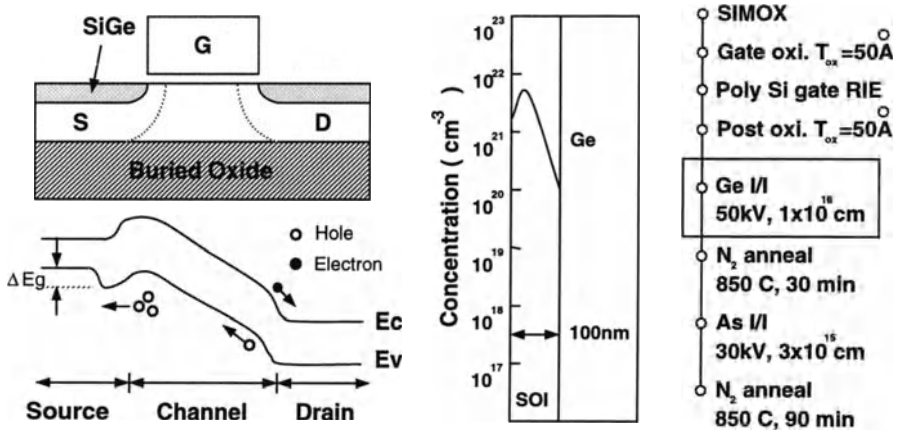


Figure 5.39: $Si_{1-x}Ge_x$ source structure in an SOI NMOS device.

one tenth of a volt smaller than the silicon bandgap. Due to a narrower bandgap in the Si-Ge source area, the hole current in the emitter is enhanced. The built-in potential barrier between the source and the body is lowered. Consequently, the accumulated holes in the silicon thin-film can be more easily expelled. As a result, the parasitic BJT effect is reduced. Fig. 5.40 shows the comparison of the IV characteristics between a conventional SOI-MOSFET and a Ge-implanted SOI-MOSFET, which have a front gate oxide of 50Å, a silicon thin-film of 1000Å, and an aspect ratio of W/L = 10μm/0.15μm[68]. As shown in the figure, owing to the Ge implant to the source region, the parasitic BJT effect is lowered. Therefore, the kink effect is lessened, hence, the breakdown voltage is improved for the device with the Si-Ge source structure. Fig. 5.41 shows the subthreshold characteristics of conventional and Ge-implanted SOI NMOS devices with aspect ratios of 10μm/0.15μm and 10μm/0.25μm[68]. As shown in the figure, in the Ge-implanted SOI NMOS device, the onset of the single-transistor latch behavior is due to the positive feedback phenomenon described in the previous paragraph, is improved from $V_D = 2.55V$ to $V_D = 3.75V$ ($V_G = -1V$). Also shown in the figure, the peculiar subthreshold slope behavior—at a larger drain voltage the subthreshold slope is steeper due to the parasitic BJT effect, is reduced substantially.

In addition to the Ge-implanted source structure, other techniques have also been figured out for reducing the nonideal effects of the partially-depleted SOI MOS devices due to floating body effects. Fig. 5.42 shows the cross section of a 0.1μm

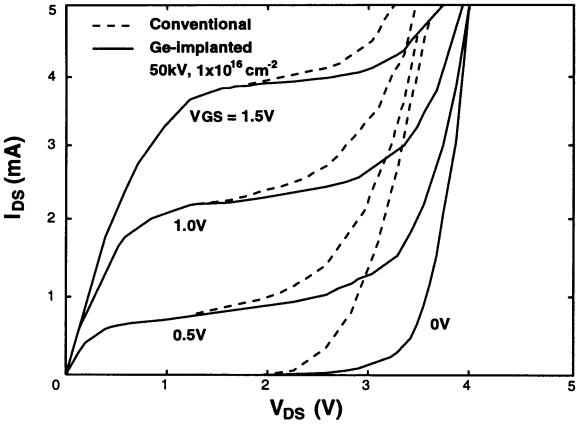


Figure 5.40: Comparison of the IV characteristics between a conventional SOI-MOSFET and a Ge-implanted SOI-MOSFET, which have a front gate oxide of 50Å, a silicon thin-film of 1000Å, and an aspect ratio of W/L = 10μm/0.15μm.

partially-depleted SOI NMOS device with a nonuniformly doped silicon thin-film structure[69]. By having a heavily-doped region at the bottom of the silicon thin-film, the short-channel effect of the partially-depleted SOI NMOS devices can be reduced. In addition, due to the heavily doped region in the silicon thin-film, the performance of the parasitic BJT worsens. Therefore, the kink effect and the breakdown voltage can be improved.

In the past two sections, floating body effects in SOI CMOS devices have been discussed. The impact ionization effect and the parasitic BJT effect due to the floating body structure cause the kink effect in the strong inversion, the peculiar subthreshold behavior, the single-transistor latch phenomenon, and the reduction in the drain breakdown voltage in partially-depleted SOI MOS devices. By using a SiGe-source structure and a nonuniformly doped silicon thin-film, the function of the parasitic BJT can be reduced. As a result, those unique behaviors related to the floating body structure can be lessened. In the following section, transient analysis of the SOI MOS devices is described.

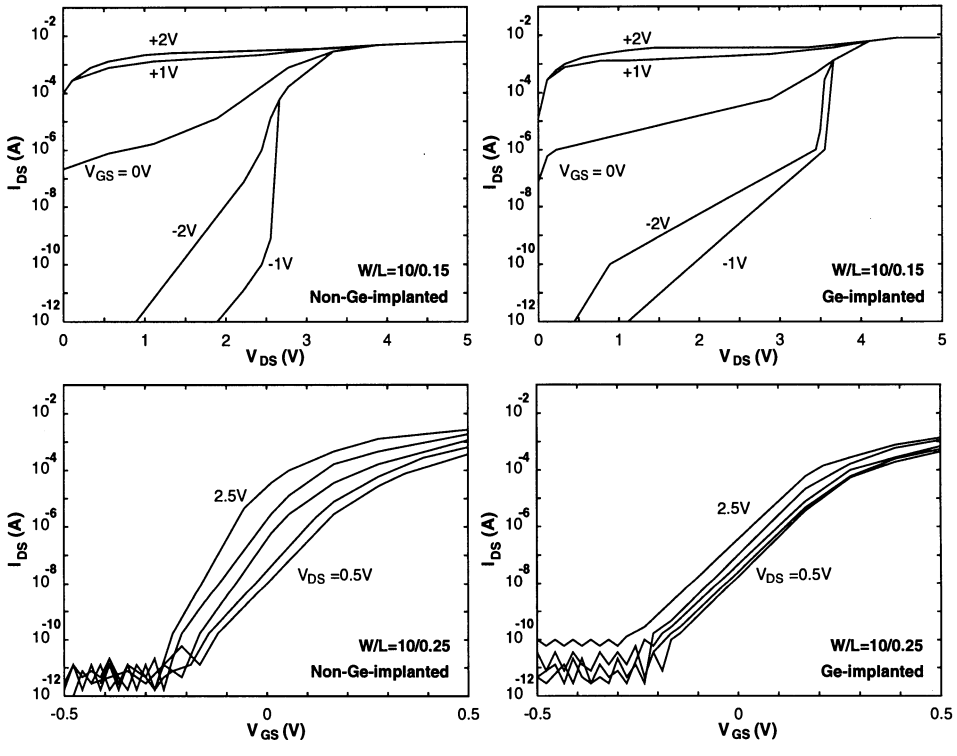


Figure 5.41: Subthreshold characteristics of conventional and Ge-implanted SOI NMOS device with aspect ratios of $10\mu m/0.15\mu m$ and $10\mu m/0.25\mu m$.

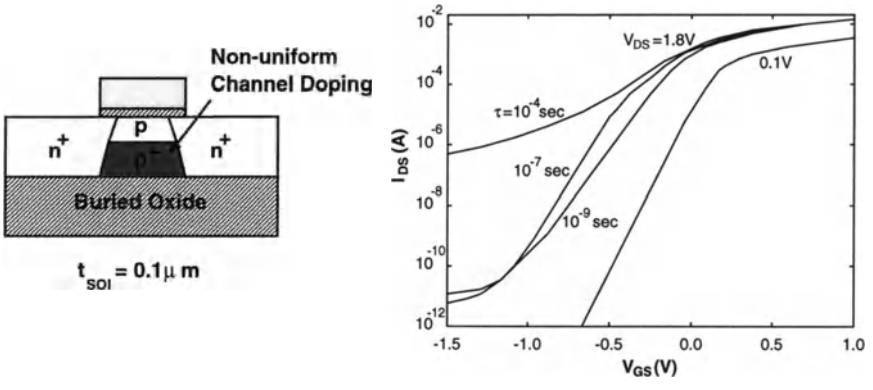


Figure 5.42: Cross section of a 0.1μm partially-depleted SOI NMOS device with a non-uniformly doped silicon thin-film structure for various carrier lifetimes.

5.8 Transient Analysis

This section is dedicated to the analysis of the transient behaviors in SOI MOS devices. Due to the floating body structure, the internal mechanisms in the SOI MOS devices during the transient are complicated. Especially, for the partially-depleted SOI MOS devices, the parasitic BJT effect and the impact ionization effect further complicate the internal mechanism during the transient. In this section, influence of the floating body structure in the transient performance is introduced first. Then, the influences of the drain voltage and the gate voltage in the transient behavior are analyzed. The operating frequency and the duty cycle of the clocks imposed on the SOI MOS devices also affect the transient behaviors. In the next portion of this section, the influence of the operating frequency in the transient performance of the SOI MOS devices is described.

The floating body structure affects the transient behavior in a partially-depleted SOI NMOS device. Fig. 5.43 shows the transient drain current characteristics of a 25μm/25μm partially-depleted SOI NMOS devices with a floating body structure and the body tied to the source, respectively. These devices have a front gate oxide of 105Å, a buried oxide of 4000Å, and a silicon thin-film of 1000Å doped with a p-type density of $2.2 \times 10^{17}\text{cm}^{-3}$. Imposing a voltage step from 0V to 1.8V at the front gate, the devices with the floating body and with the body-tied to ground show different transient characteristics[70]. The device with the body tied to ground does not have any overshoot in the drain current. The drain current settles to its final DC

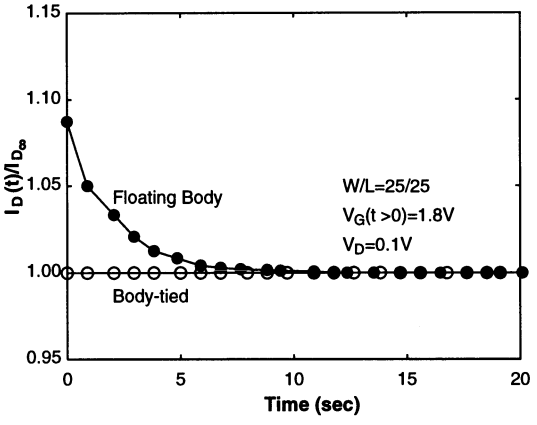


Figure 5.43: Transient drain current characteristics of a 25μm/25μm partially-depleted SOI NMOS devices with a floating body structure and a body tied to source, respectively. These devices have a front gate oxide of 105Å, a buried oxide of 4000Å, and a silicon thin-film of 1000Å doped with a p-type density of $2.2 \times 10^{17}\text{cm}^{-3}$. The source and the back gate are grounded.

value from the very beginning. In contrast, for the device with the floating body, when the gate voltage switches to positive, the device suddenly turns on. At the beginning, the holes in the p-type silicon thin-film cannot be evacuated immediately. Therefore, at the beginning, compared to the device with the body tied to ground, the device with the floating body has more holes in its silicon thin-film. As a result, at the beginning of the transient, the threshold voltage of the device with the floating body is smaller than that of the device with the body tied to ground. Consequently, a larger drain current can be seen at the beginning of the transient. For the device with its body tied to ground, when the gate voltage switches to a positive value, the holes in the silicon thin-film can be evacuated immediately. Therefore, its threshold voltage will not change. Therefore, no overshoot in the drain current can be observed.

Drain voltage affects the internal transient behavior of a partially-depleted SOI NMOS device. Fig. 5.44 shows the transient drain current of a partially-depleted NMOS device with a front gate oxide of 50Å, a buried oxide of 3800Å, a silicon thin-film of 750Å, and an aspect ratio of 25μm/0.15μm. Its gate is imposed by a pulse from -0.2V to 0.5V with an on-cycle of 35ns[71]. As shown in the figure, when the drain voltage is larger, the drain current switches to its final steady state

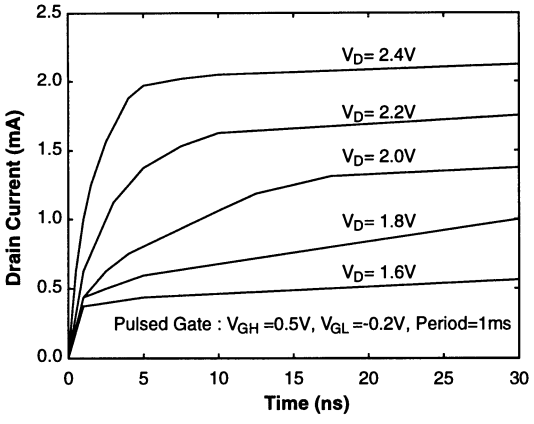


Figure 5.44: Transient drain current of a partially-depleted SOI NMOS device with a front gate oxide of 50Å, a buried oxide of 3800Å, a silicon thin-film of 750Å, and an aspect ratio of $25\mu m/0.15\mu m$. Its gate is imposed by a pulse from -0.2V to 0.5V with an on-cycle of 35ns.

more quickly. At a larger V_D, impact ionization is more serious. Therefore, a larger hole current is generated. Hence, the speed of the hole accumulation in the silicon thin-film is faster. Consequently, the parasitic BJT turns on faster and the device reaches its final steady state earlier.

In addition to the drain voltage, the gate voltage also affects the internal transient behavior in a partially-depleted SOI NMOS device. Fig. 5.45 shows the drain current characteristics of a partially-depleted SOI NMOS device with an aspect ratio of $50\mu m/0.2\mu m$, biased at $V_{DS} = 1.5V$. Its gate is imposed by a clock, which switches from 0V to V_{GS}. The pulse width is $8\mu s$. The pulse frequency is 50Hz[72]. As shown in the figure, for a smaller gate voltage, the drain current reaches its final steady state value more slowly. At a smaller gate voltage, its drain current is smaller. The hole current generated by impact ionization is also smaller. Therefore, the process of the hole accumulation in the silicon thin-film is slower. Therefore, it takes a longer period of time for the device to reaches its final steady state. Fig. 5.46 shows the subthreshold characteristics of a partially-depleted SOI NMOS device with its parameters and transient measurements same as for the previous figure[72]. Solid lines show the DC results. As shown in the figure, when $V_D > 1V$, the transient value is smaller than the DC value. Since the holes produced by impact ionization during the transient cannot be accumulated in time, the parasitic BJT does not

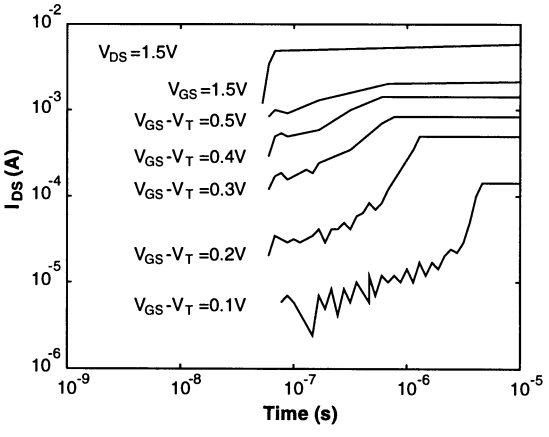


Figure 5.45: Drain current characteristics of a partially-depleted SOI NMOS device with an aspect ratio of $50\mu m/0.2\mu m$, biased at $V_{DS} = 1.5V$. Its gate is imposed by a clock, which switches from 0V to V_{GS}. The pulse width is $8\mu s$. The pulse frequency is 50Hz.

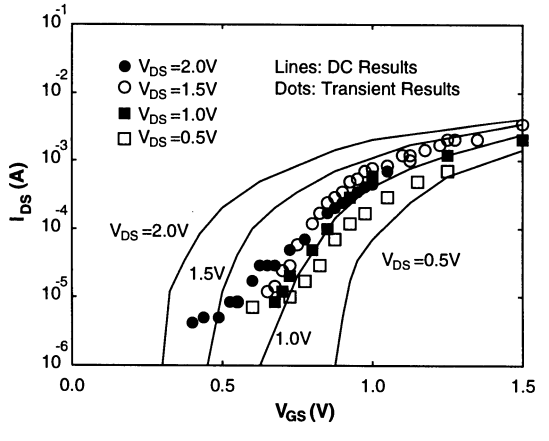


Figure 5.46: Subthreshold characteristics of a partially-depleted SOI NMOS device with its parameters and transient measurements same as for the previous figure. Solid lines show the DC results.

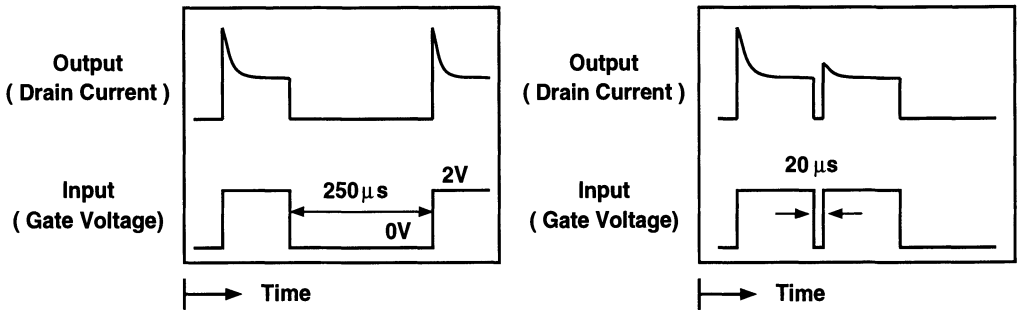


Figure 5.47: Switching characteristics of a partially-depleted SOI NMOS device with an aspect ratio of $20\mu m/2\mu m$, a front gate oxide of 700Å, a buried oxide of $1\mu m$, and a silicon thin-film of 5000Å doped with a p-type density of $5 \times 10^{16} cm^{-3}$, biased with an input clock of 2V imposed at the gate with intervals of $250\mu s$ and $20\mu s$.

turn on yet. Therefore, its threshold voltage during the transient is larger than that at DC. Consequently, the subthreshold current during the transient is smaller than its DC value at $V_D > 1V$. On the other hand, at $V_D < 1V$, the situation is reverse. At $V_D < 1V$, the transient value is larger than the DC value. At $V_D < 1V$, when the device suddenly turns on, the holes in the silicon thin-film cannot be evacuated quickly. As a result, the threshold voltage of the transient one at V_D is smaller than its DC value. Therefore, at $V_D < 1V$, its subthreshold current during transient is larger than its DC value. From the above reasoning, two mechanisms during transient exist. For $V_D > 1$, the transient behavior is dominated by the impact ionization and the parasitic BJT effects. For $V_D < 1$, the impact ionization and the parasitic BJT effects are not so important as compared to the hole evacuation effect. For $V_D < 1V$, the transient behavior is dominated by the change in the threshold voltage due to the hole evacuation condition.

The transient behavior in a partially-depleted SOI NMOS device is also dependent on the interval between consecutive turn-on cycles. Fig. 5.47 shows the switching characteristics of a partially-depleted SOI NMOS device with an aspect ratio of $20\mu m/2\mu m$, a front gate oxide of 700Å, a buried oxide of $1\mu m$, and a silicon thin-film of 5000Å doped with a p-type density of $5 \times 10^{16} cm^{-3}$, biased with an input clock of 2V imposed at the gate with intervals of $250\mu s$ and $20\mu s$[73]. As shown in the figure, the overshoot in the drain current is due to a lag in the hole evacuation process during the sudden turn-on of the device as described before. With a long interval between consecutive turn-on cycles ($250\mu s$), before the turn-on of the second

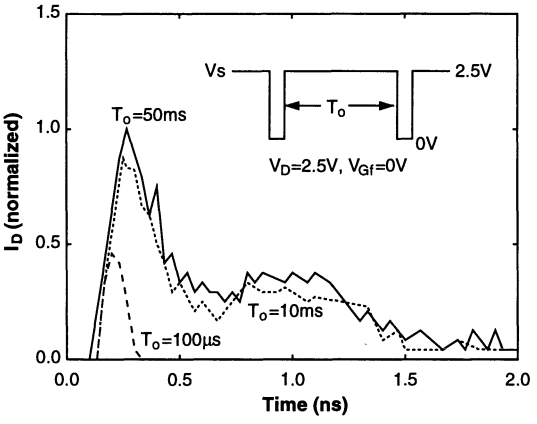


Figure 5.48: Transient drain current of the partially-depleted NMOS device with a front gate oxide of 70Å, a silicon thin-film of 1400Å, and an aspect ratio of $10\mu m/0.3\mu m$, biased at $V_G = 0V$. A clock as shown is imposed at the source.

turn-on cycle, the device has reached its stable state. Therefore, the drain current overshoot of the second turn-on period is identical to that of the first one. On the other hand, if the interval between turn-on cycles is short ($20\mu s$), after the first turn-on cycle, the device has not reached its stable off-state yet— the evacuated holes during turn-on have not been fully recovered to the silicon thin-film region for the turn-off cycle. At this time, the second turn-on cycle starts— the device suddenly turns on. At this time, the amount of holes in the silicon thin-film is smaller than that in the case with a longer interval ($250\mu s$). Therefore, the threshold voltage is larger for the $20\mu s$ case. Consequently, the drain current overshoot during the second turn-on period of the $20\mu s$ case is smaller as compared to the $250\mu s$ case.

The leakage current in a partially-depleted SOI NMOS device is important in determining the transient performance. The leakage current is related to the function of the parasitic BJT. Fig. 5.48 shows the transient drain current of the partially-depleted NMOS device with a front gate oxide of 70Å, a silicon thin-film of 1400Å, and an aspect ratio of $10\mu m/0.3\mu m$, biased at $V_G = 0V$. A clock from 0V to 2.5V is imposed at the source[74]. In this experiment, the device is turned off such that it can be concentrated on the leakage current effect. When the source voltage is 2.5V, the base-emitter junction of the parasitic BJT is reverse biased. When the source voltage is 0V, the base-emitter junction is forward biased. When the clock switches from 2.5V to 0V, the base-emitter junction turns on. A sudden rise in the

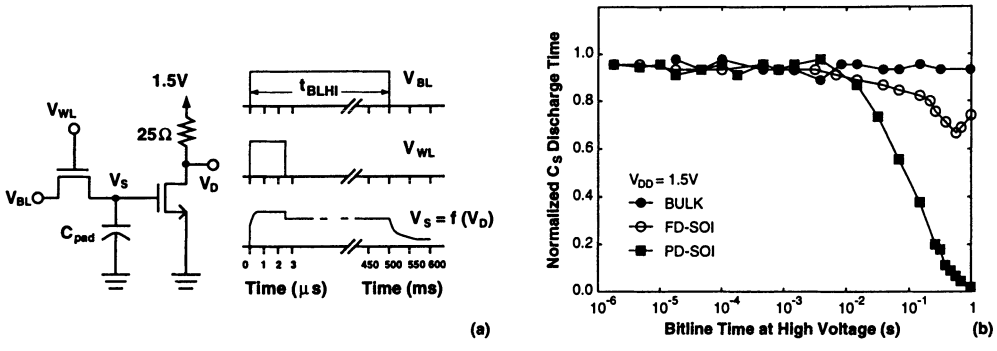


Figure 5.49: (a) A simplified circuit used to measure bitline-induced transient effect of a DRAM circuit built by partially-depleted SOI MOS devices. The device on the left represents the access transistor and the device on the right senses the voltage on the storage node V_S. Clocks to drive the world line and the bit line are shown.(b) Normalized discharge time to discharge the storage capacitance versus time interval between consecutive turn-low of the bit lines.

leakage current can be seen. After the base-emitter junction turns on, the holes in the silicon thin-film are being evacuated. Therefore, the drain current decays. The interval between consecutive turn-on periods of the base-emitter junction is also important for the leakage current. If the interval is long ($50ms$), the evacuated holes during the turn-on of the base-emitter junction have been fully returned to the silicon thin-film region. During the next turn-on, the leakage current is larger due to the fully forward bias of the base-emitter junction. On the other hand, if the interval between turn-ons is short ($100\mu s$), during the interval the silicon thin-film has not been fully recovered with all its holes. Then, during the next turn-on the leakage current is smaller. The leakage current can determine the time to discharge the storage capacitance. Fig. 5.49 shows a simplified circuit used to measure bitline-induced transient effect of a DRAM circuit built by partially-depleted SOI MOS devices. The device on the left represents the access transistor and the device on the right senses the voltage on the storage node V_s. Clocks to drive the word line and the bit line are shown[75]. Also shown in the figure are the discharge times for the DRAM circuit using bulk CMOS, fully-depleted and partially-depleted CMOS devices. As shown in the figure, if the time for the bitline at a high voltage is short, the leakage current is small as described before. Therefore, the time to discharge the storage capacitance is long. If the bitline time at the high voltage is long, the

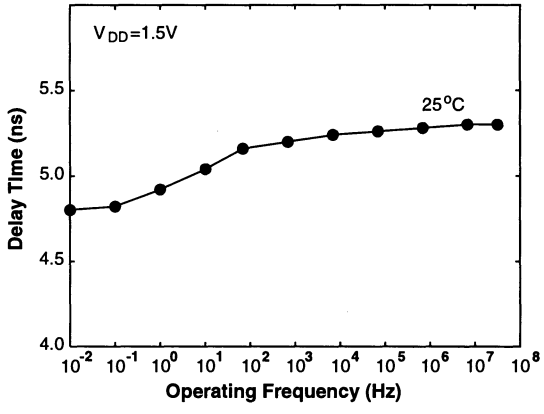


Figure 5.50: Delay time versus operating clock frequency of a 64-bit adder built by partially-depleted SOI MOS devices.

discharge time decreases since the leakage current increases. If the bitline time at the high voltage is short, regardless of the device type, the discharge time is about identical. If the bitline time at the high voltage is long, the partially-depleted case shows the worst discharge time since the leakage current is largest among three cases.

The internal transient behavior decides the speed performance of a circuit built by partially-depleted SOI MOS devices. Fig. 5.50 shows the delay time versus operating clock frequency of a 64-bit adder built by partially-depleted SOI MOS devices[76]. As shown in the figure, at a high operating frequency, the delay time of the adder built by partially-depleted SOI MOS devices is longer since the interval between two consecutive on periods is shorter. Therefore, before the beginning of the on cycle, the silicon thin-film does not have enough time to recover its evacuated holes. Consequently, the threshold voltage of the devices at the beginning of the on cycle is larger as compared to the case with a lower operating frequency. As a result, a smaller driving drain current is expected at a higher operating frequency. Hence, the propagation delay time is longer.

5.9 Hot Carrier Effects

For deep-submicron CMOS devices with a very small channel length, due to a large lateral electric field, the hot carrier effects are important. Due to the floating body structure, for deep-submicron SOI CMOS devices, the hot carrier effects may be

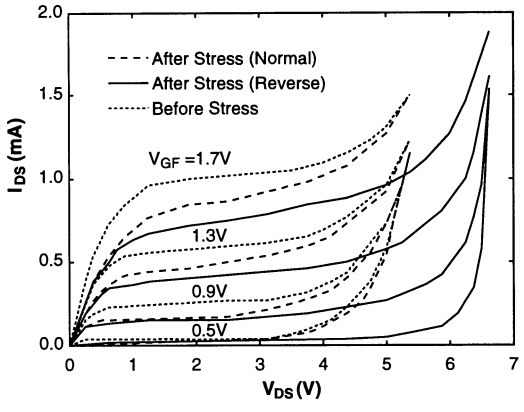


Figure 5.51: IV characteristics of an SOI NMOS device with an aspect ratio of $25\mu m/2\mu m$, a front gate oxide of 250Å, a buried oxide of 3600Å, and a silicon thin-film of 850Å, before and after stress for a period of 1500 seconds. The stress conditions are $V_G = 1V$, $V_S = V_B = 0$, $V_D = 6.5V$.

different from those for bulk CMOS ones. In this section, hot carrier effects of SOI CMOS devices are analyzed. Starting from the hot carrier effect on the strong inversion drain current of SOI NMOS and PMOS devices, the hot carrier effect on the subthreshold characteristics is analyzed. Then, the hot carrier degradation of fully-depleted and partially-depleted SOI CMOS devices is analyzed in terms of stress time. Comparison of the hot carrier degradation between SOI and bulk MOS devices is also included. In the final portion of this section, following the technique in studying the hot carriers for the bulk devices, monitoring the hot carrier degradation in terms of the body current is presented. Differences in the body current between the bulk and SOI devices are explained.

Fig. 5.51 shows the IV characteristics of an SOI NMOS device with an aspect ratio of $25\mu m/2\mu m$, a front gate oxide of 250Å, a buried oxide of 3600Å, and a silicon thin-film of 850Å, before and after stress for a period of 1500 seconds. The stress conditions are $V_G = 1V$, $V_S = V_B = 0V$, $V_D = 6.5V$[77]. As shown in the figure, after stress, the drain current decreases. After stress, the hot electrons in the high electric field near the drain are trapped at the front oxide. Therefore, the threshold voltage shifts toward the positive direction. Hence, the drain current is decreased after stress. If the source and the drain are reversed—reverse mode, after stress, the degradation in the drain current is even more as compared to the

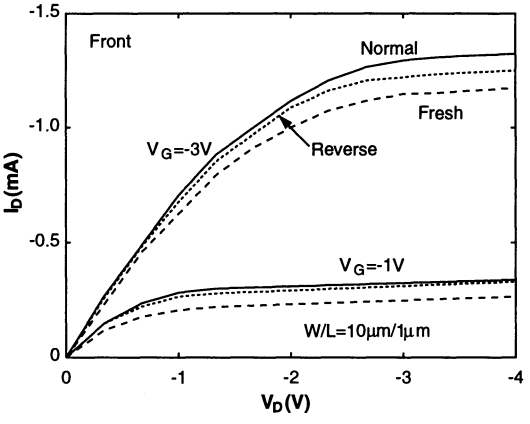


Figure 5.52: Drain current versus drain voltage of an SOI PMOS device with an aspect ratio of $10\mu m/1\mu m$, a silicon thin-film of 916Å, and a front gate oxide of 118Å, before and after stress.

normal mode without reversing the source and the drain. After stress, in the reverse mode, the breakdown voltage becomes larger. This is due to the fact, in the reverse mode, near the source end there exist a lot of interface traps after stress. When impact ionization occurs, the generated holes, which are supposed to be gathered by the source end, are attracted by the interface traps near the source. Thus, these holes recombine with the traps. As a result, the parasitic BJT effect is suppressed. Therefore, the breakdown voltage of the reverse mode after stress is higher.

In the previous paragraph, hot carrier effects of an SOI NMOS device have been reported. Here, hot carrier effects of an SOI PMOS device are described. Fig. 5.52 shows the drain current versus drain voltage of an SOI PMOS device with an aspect ratio of $10\mu m/1\mu m$, a thin-film of 916Å, and a front gate oxide of 118Å, before and after stress[78]. As shown in the figure, contrary to the NMOS case, the drain current decreases after stress. In addition, the generated hot electrons are injected into the front oxide. Therefore, the threshold voltage is shifted toward the positive direction. Thus, for a PMOS device its drain current increases after stress. If the source and the drain are reversed after stress, the enhancement in the drain current is smaller as compared to the normal mode— the source and the drain are not reversed after stress.

Until now in this section, hot carrier effects on the strong inversion drain current

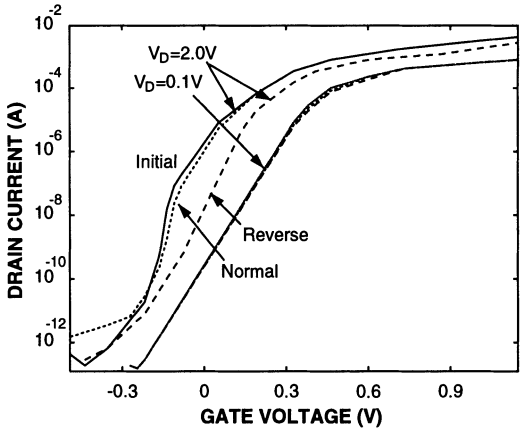


Figure 5.53: Subthreshold characteristics of a partially-depleted SOI NMOS device with an aspect ratio of $10\mu m/0.17\mu m$, a front gate oxide of 50Å, a buried oxide of 900Å, and a silicon thin-film of 500Å, before and after stress at $V_G = 0.2V$ and $V_D = 3V$ for three minutes.

characteristics have been analyzed. Here, hot carrier effects on the subthreshold characteristics are described. Fig. 5.53 shows the subthreshold characteristics of a partially-depleted SOI NMOS device with an aspect ratio of $10\mu m/0.17\mu m$, a front gate oxide of 50Å, a buried oxide of 900Å, and a silicon thin-film of 500Å, before and after stress at $V_G = 0.2V$ and $V_D = 3V$ for three minutes [79]. As shown in the figure, before stress, owing to the parasitic BJT effect, the subthreshold slope is steep for $V_D = 2V$. After stress, for the normal mode (without reversing the source and the drain) the characteristics does not change substantially. However, for the reverse mode (reversing the source and the drain) after stress, the subthreshold slope becomes less steep. This can be reasoned as follows. Under reverse mode after stress, a lot of traps gather near the source. Therefore, the holes, which are generated by impact ionization in the high electric field region near the drain, are attracted by the traps and thus recombined. Therefore, the parasitic BJT effect has been suppressed. As a result, the subthreshold slope becomes less steep.

The hot carrier effects in SOI MOS devices are dependent on the stress time. Fig. 5.54 shows the drain current degradation versus stress time of an SOI NMOS device with a channel length of $0.8\mu m$, a front gate oxide of 108Å, a buried oxide of 3600Å, and a silicon thin-film of 700Å doped with a p-type density of $5 \times 10^{16} cm^{-3}$,

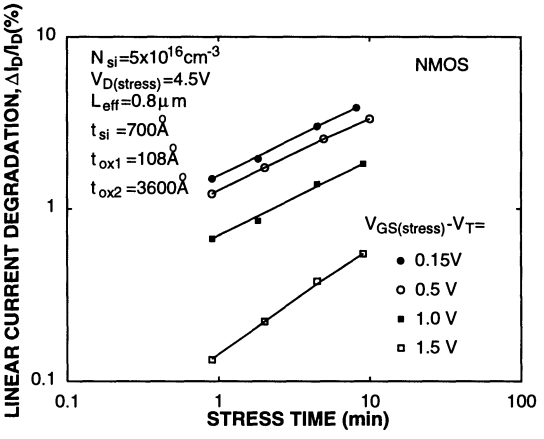


Figure 5.54: Drain current degradation versus stress time of an SOI NMOS device with a channel length of 0.8μm, a front gate oxide of 108Å, a buried oxide of 3600Å, and a silicon thin-film of 700Å doped with a p-type density of $5 \times 10^{16}\text{cm}^{-3}$, stressed at $V_D = 4.5V$.

stressed at $V_D = 4.5V$[80]. From this figure, in general, a longer stress time leads to a larger degradation in the drain current. When $V_{GS} - V_{TH}$ for stressing becomes smaller, the current degradation becomes worse. The worst current degradation occurs at a stress condition at $V_{GS} = V_{TH}$ for the SOI NMOS device. In contrast, for the bulk NMOS device, the worst current degradation after stress occurs at a stress condition of $V_{GS} = V_{DS}/2$. The difference in the condition when the worst current degradation occurs after stress between the SOI and the bulk NMOS devices is probably due to the parasitic BJT effects. Fig. 5.55 shows the drain current degradation versus stress time for a partially-depleted SOI NMOS device with a silicon thin-film of 1000Å doped with a p-type density of $3 \times 10^{17}\text{cm}^{-3}$ and two fully-depleted SOI NMOS devices with a silicon thin-film doping density of $5 \times 10^{16}\text{cm}^{-3}$, and a channel length of 0.7μm, stressed at $V_{GS} - V_T = 0.15V$ and $V_{DS} = 3.8V$. [80]. As shown in the figure, the partially-depleted SOI NMOS device has the worst hot carrier effects— the degradation is the worst among three cases. In addition, between two fully-depleted SOI NMOS devices, the silicon thin-film thickness does not substantially affect the hot carrier degradation.

Fig. 5.56 shows the transconductance degradation versus stress time of a fully-depleted SOI NMOS device with an aspect ratio of 25μm/0.48μm, a front gate oxide

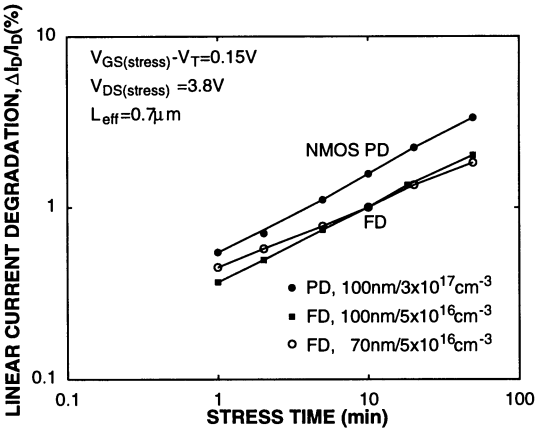


Figure 5.55: Drain current degradation versus stress time for a partially-depleted SOI NMOS device with a silicon thin-film of 1000Å doped with a p-type density of $3 \times 10^{17}\text{cm}^{-3}$ and two fully-depleted SOI NMOS devices with a silicon thin-film doping density of $5 \times 10^{16}\text{cm}^{-3}$, and a channel length of 0.7μm, stressed at $V_{GS} - V_T = 0.15V$ and $V_{DS} = 3.8V$.

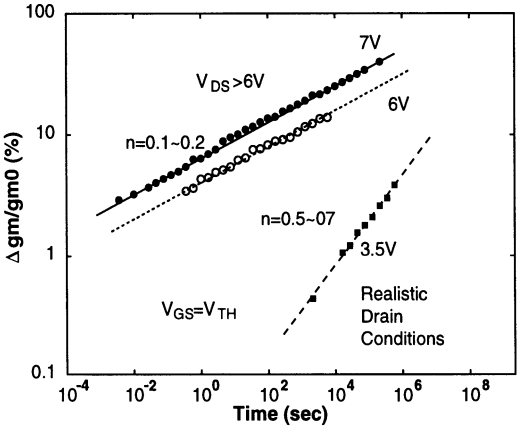


Figure 5.56: Transconductance degradation versus stress time of a fully-depleted SOI NMOS device with an aspect ratio of $25\mu\text{m}/0.48\mu\text{m}$, a front gate oxide of 105Å, a buried oxide of 4000Å, and a silicon thin-film of 900Å doped with a p-type density of $1.7 \times 10^{17}\text{cm}^{-3}$, stressed at $V_{GS} = V_{TH}$.

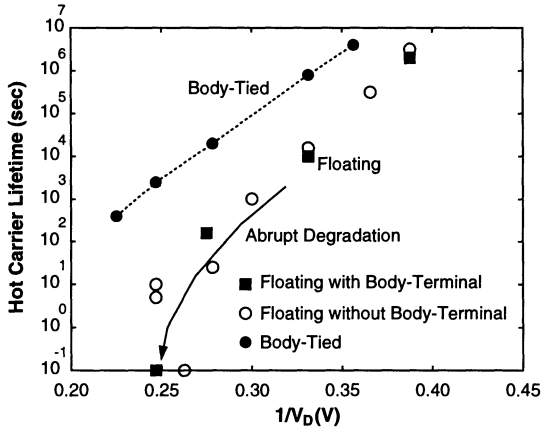


Figure 5.57: Hot carrier lifetime versus $1/V_D$ of two partially-depleted SOI NMOS devices with a channel length of 0.3μm, a front gate oxide of 70Å, a buried oxide of 4000Å, and a silicon thin-film of 2000Å, stressed at $V_{GS} = V_T$. One device is with its body tied to ground. The other is with its body floating.

of 105Å, a buried oxide of 4000Å, and a silicon thin-film of 900Å doped with a p-type density of $1.7 \times 10^{17}\text{cm}^{-3}$, stressed at $V_{GS} \cong V_{TH}$[81]. As shown in the figure, at different drain voltages the degradation mechanisms may be different. For $V_D < 5$, the degradation is a function of (stress time)$^{-\text{n}}$, where n is between 0.5 and 0.7. For $V_D > 6V$, n is between 0.1 and 0.2.

Fig. 5.57 shows the hot carrier lifetime versus $1/V_D$ of two partially-depleted SOI NMOS devices with a channel length of 0.3μm, a front gate oxide of 70Å, a buried oxide of 4000Å, and a silicon thin-film of 2000Å, stressed at $V_{GS} = 0.7V$. One device is with its body tied to ground. The other is with its body floating[82]. As shown in the figure, the hot carrier lifetime is defined as the elapsed time when the measured drain current in the saturation region is degraded by 15%, which is measured in reverse mode (with source and drain reversed) after stress. For a partially-depleted SOI NMOS device, the floating body structure affects the hot carrier performance substantially. With its body tied to ground, the hot carrier lifetime is longer. On the other hand, with its body floating, the hot carrier lifetime is shorter. Especially, after the onset of the kink effect, its lifetime decreases sharply due to the parasitic BJT effect.

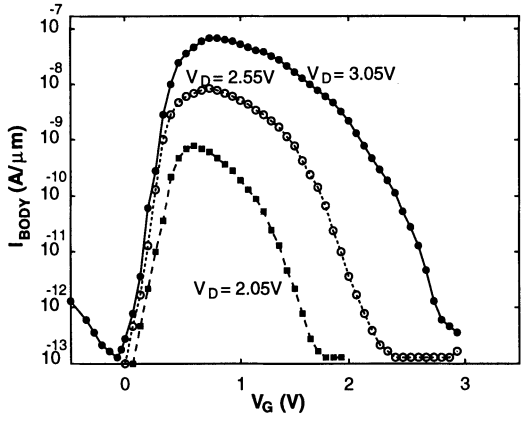


Figure 5.58: Body current versus gate voltage of a fully-depleted SOI NMOS device with a front gate oxide of 70Å, and a silicon thin-film of 560Å under stress.

As for the bulk CMOS devices, hot carrier degradation can be monitored by measuring the body current of the SOI device under stress. By adding a body contact to the silicon thin-film area, the body current of the SOI NMOS device under stress can be measured. Fig. 5.58 shows the body current versus gate voltage of a fully-depleted SOI NMOS device with a front gate oxide of 70Å, and a silicon thin-film of 560Å under stress[83]. A higher body current means that impact ionization is more serious, hence a higher hot carrier degradation can be expected. As shown in the figure, the peak in the body current is related to the peak in the hot carrier degradation. From the peak in the body current, the worst hot carrier degradation occurs at $V_{GS} = V_{TH}$, which is different from the bulk CMOS devices, where the worst hot carrier degradation occurs at $V_{GS} \cong V_{DS}/2$.

Fig.5.59 shows $I_{sub}/I_D(V_D - V_{DSAT})$ versus $1/(V_D - V_{DSDAT})$ of SOI and bulk NMOS devices with an aspect ratio of 9.5μm/1.4μm under stress [84]. The bulk device has a gate oxide of 86Å, and a source/drain junction depth of 2000Å. The SOI device has a front gate oxide of 90Å. From this figure, the hot carrier degradation in the SOI devices is much smaller than that in the bulk. In addition, the hot carrier degradation is not sensitive to the silicon thin-film thickness of the SOI MOS devices.

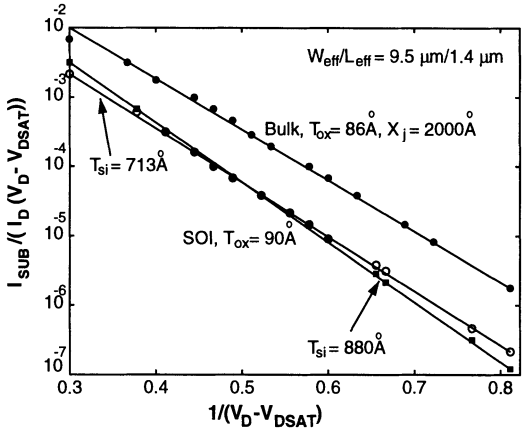


Figure 5.59: $I_{sub}/I_D(V_D - V_{DSAT})$ versus $1/(V_D - V_{DSAT})$ of SOI and bulk NMOS devices with an aspect ratio of $9.5\mu m/1.4\mu m$ under stress. The bulk device has a gate oxide of 86Å, and a source/drain junction depth of 2000Å. The SOI device has a front gate oxide of 90Å.

5.10 Thermal Analysis

Due to the buried oxide structure, SOI CMOS devices are sensitive to the thermal effect. In this section, thermal analysis of SOI CMOS devices is described. Specifically, starting from the effect of the ambient temperature on the carrier mobility, the influence of the ambient temperature in the threshold voltage, the leakage current, and the kink effect are presented. Then, the lattice temperature effect due to self-heating on the drain current and the transient behaviors is analyzed. In addition, the influence of the SOI structure in terms of the silicon thin-film and buried oxide thickness in the lattice temperature is discussed. In the final portion of the section, thermal coupling between devices for SOI circuits having various layouts is described.

When the ambient temperature is changed, the surface mobility in an SOI NMOS is affected. Fig. 5.60 shows the surface mobility versus ambient temperature of an SOI NMOS device[85]. When the ambient temperature is raised, the surface mobility is lowered. In addition, when the back gate bias becomes more negative, the surface mobility is also degraded due to the increased surface electric field. When the back gate bias is very negative, strong inversion at the substrate surface or hole accumulation at the bottom of the silicon thin-film may exist. Under this situation,

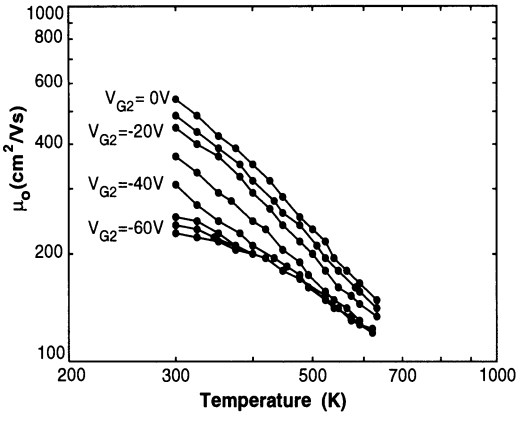


Figure 5.60: Surface mobility versus ambient temperature of an SOI NMOS device.

the back gate bias effect on the surface mobility becomes saturated.

In addition to mobility, threshold voltage of an SOI CMOS device is also sensitive to the ambient temperature. Fig. 5.61 shows the threshold voltage versus ambient temperature of an inversion-mode fully-depleted SOI NMOS device with a front gate oxide of 190Å, and a silicon thin-film of 1000Å doped with a p-type density of 1.6×10^{17}cm^3[86]. Also shown in the figure are the threshold voltages for partially-depleted SOI and bulk NMOS devices. As shown in the figure, the sensitivity of the threshold voltage to the ambient temperature of the partially-depleted SOI and bulk NMOS devices is about two to three times higher than that of the fully-depleted SOI NMOS devices since the depletion width under the channel in the partially-depleted SOI and bulk NMOS devices changes when the ambient temperature varies. However, for the fully-depleted devices, the fully-depleted silicon thin-film does not depend on the ambient temperature. It's worth pointing out that when the ambient temperature rises, the difference in the threshold voltage sensitivity to the ambient temperature between the partially-depleted and the fully-depleted SOI NMOS devices narrows.

Leakage current, which is important in determining the performance of an SOI MOS device, is sensitive to temperature variations. Fig. 5.62 shows the off leakage current versus ambient temperature of accumulation-mode SOI PMOS devices biased at $V_G = 0V$ and $V_D = -3V$ [1]. Also shown in the figure is the off leakage

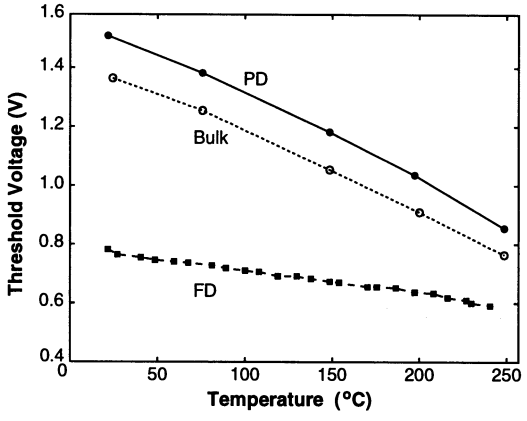


Figure 5.61: Threshold voltage versus ambient temperature of an inversion-mode fully-depleted SOI NMOS device with a front gate oxide of 190Å, and a silicon thin-film of 1000Å doped with a p-type density of $1.6 \times 10^{17}\text{cm}^{-3}$. Also shown are the threshold voltages for partially-depleted SOI and bulk NMOS devices.

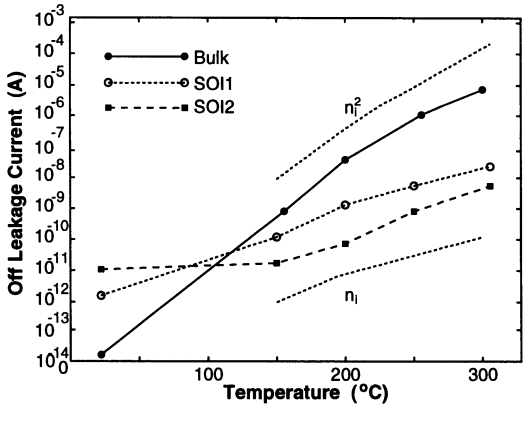


Figure 5.62: Off leakage current versus ambient temperature of accumulation-mode SOI PMOS devices biased at $V_G = 0V$ and $V_D = -3V$.

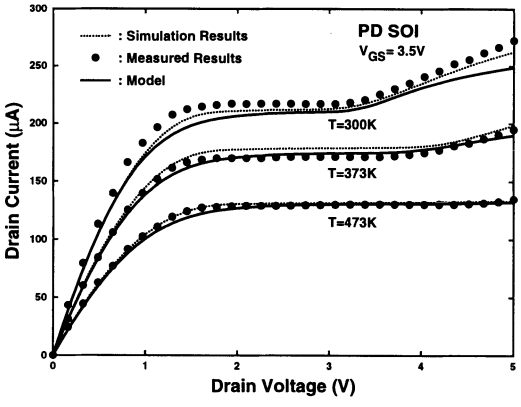


Figure 5.63: I_D versus V_{DS} of a partially-depleted SOI NMOS device with an aspect ratio of 50μm/20μm, a front gate oxide of 250Å, a buried oxide of 4500Å, and a silicon thin-film of 2500Å doped with a p-type density of $10^{17}cm^{-3}$.

current for the bulk device. As shown in the figure, the leakage of the bulk device is much more ambient-temperature dependent than that of the accumulation-mode SOI PMOS device since the leakage current in the bulk device is dominated by the reverse-biased diode current between the drain and substrate. Therefore, the leakage current of the bulk device is $\propto n_i^2$. On the other hand, for the SOI device, the drain is separated from the substrate by the buried oxide. Therefore, no diode current exists between the drain and the substrate. In the SOI device, the leakage current is mainly from the thermal generation current, which is linearly proportional to the intrinsic carrier concentration ($\propto n_i$). Therefore, the sensitivity of the SOI device to the temperature is much smaller than that of the bulk device.

In addition to the mobility, the threshold voltage, and the leakage current, the IV behavior of an SOI MOS device is also dependent on the ambient temperature. Fig. 5.63 shows I_D versus V_{DS} of a partially-depleted SOI NMOS device with an aspect ratio of 50μm/20μm, a front gate oxide of 250Å, a buried oxide of 4500Å, and a silicon thin-film of 2500Å doped with a p-type density of $10^{17}cm^{-3}$[87]. As shown in the figure, when the temperature rises, the mobility is degraded. Therefore, the drain current is reduced. When the temperature rises, the impact ionization rate is decreased. Therefore, the kink effect becomes smaller at a higher temperature.

Until now in this section, the temperature dependence is referred to raising the

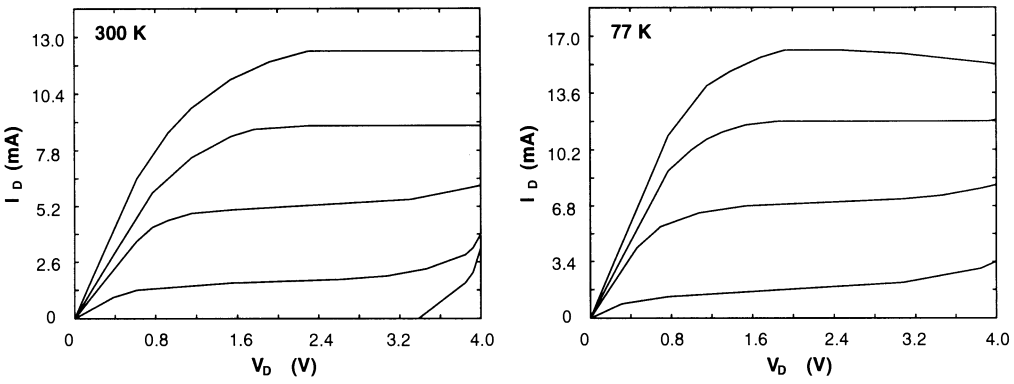


Figure 5.64: I_D versus V_{DS} characteristics of a fully-depleted SOI NMOS device with a front gate oxide of 175Å, a buried oxide of 3800Å, and a silicon thin-film of 800Å, operating at 300K and 77K.

ambient temperature. Here, self-heating of an SOI MOS device operating at 77K is described. Fig. 5.64 shows I_D versus V_{DS} characteristics of a fully-depleted SOI NMOS device with a front gate oxide of 175Å, a buried oxide of 3800Å, and a silicon thin-film of 800Å, operating at 300K and 77K[88]. As shown in the figure, at the low temperature, the negative differential output resistance is more noticeable. This is due to the fact that at the low temperature a higher mobility can be reached. Therefore, the drain current is larger at the low temperature, hence more power dissipation. As a result, self-heating is more noticeable at the low temperature. In addition, the thermal conductivity of the oxide is worse at the low temperature also contributes to the more noticeable negative output resistance behavior. Fig. 5.65 shows the thermal conductivity (K_{ox}) and thermal resistance (R_{th}) versus temperature with a silicon thin-film of 800Å[89]. From the figure, since the thermal conductivity of the oxide varies with the temperature, the thermal resistance of the device is not fixed. With an identical buried oxide thickness, the thermal resistance of the device drops when the temperature rises. With a thinner buried oxide, the thermal resistance becomes smaller.

As described before, due to the buried oxide structure, self heating of an SOI MOS device can not be overlooked. Due to self heating, the temperature in the silicon thin-film may rise above the ambient temperature— self-heating due to the lattice temperature. The lattice temperature of an SOI MOS device is dependent on two factors: the silicon thin-film thickness and the buried-oxide thickness. Fig. 5.66

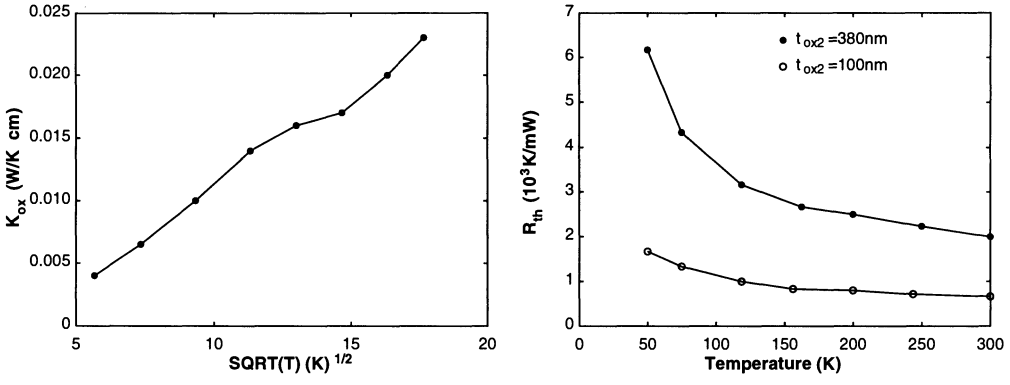


Figure 5.65: Thermal conductivity (K_{ox}) and thermal resistance (R_{th}) versus temperature of an SOI MOS device with a silicon thin-film of 800Å.

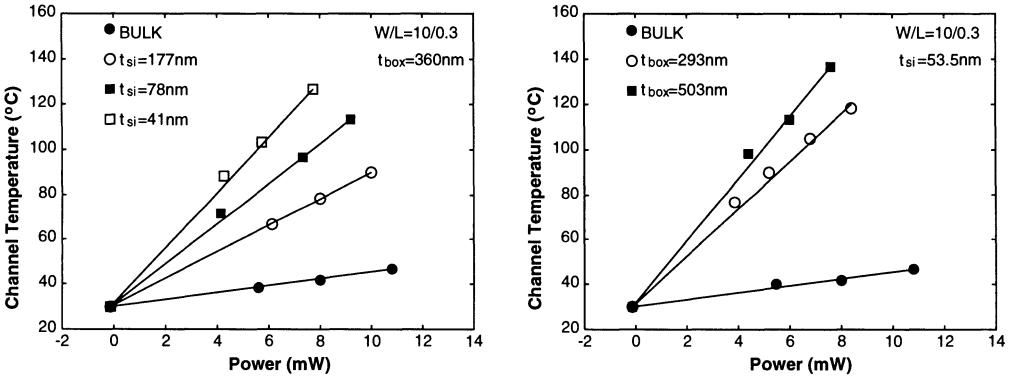


Figure 5.66: Lattice temperature versus power dissipation of an SOI NMOS device with an aspect ratio of 10μm/0.3μm, and a front gate oxide thickness of 55Å.

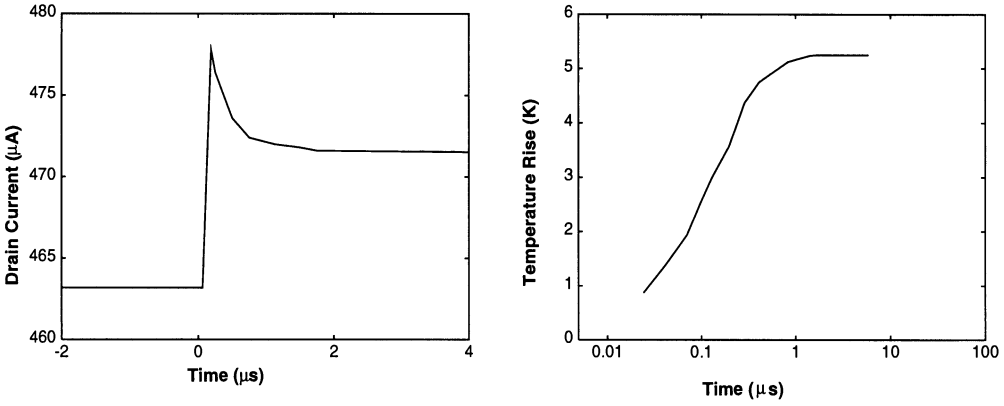


Figure 5.67: Drain current and the lattice temperature during the transient of a fully-depleted SOI MOS device with an aspect ratio of 2.4μm/1.8μm, a front gate oxide of 150Å, a buried oxide of 3300Å, and a silicon thin-film of 1700Å, with a sudden rise in the drain voltage.

shows the lattice temperature versus power dissipation of an SOI NMOS device with an aspect ratio of 10μm/0.3μm, and a front gate oxide thickness of 55Å[90]. As shown in the figure, when the power dissipation increases, the lattice temperature rises. In addition, a thinner silicon thin-film leads to a higher sensitivity to the power dissipation. Compared to the bulk device, from the silicon thin-film thickness point of view, the SOI device has a much higher lattice temperature sensitivity. On the other hand, the lattice temperature is also sensitive to the buried oxide thickness. As shown in the figure, a thicker buried oxide leads to a higher lattice temperature due to a poorer heat dissipation capability.

Until now in this section, the thermal analysis is on the DC performance of an SOI MOS device. In fact, self-heating also affects the transient behavior. Fig. 5.67 shows the drain current and the lattice temperature during the transient of a fully-depleted SOI MOS device with an aspect ratio of 2.4μm/1.8μm, a front gate oxide of 150Å, a buried oxide of 3300Å, and a silicon thin-film of 1700Å [91]. As shown in the figure, with a sudden rise in the drain voltage, the drain current rises suddenly to a peak. Along with an increase in the power consumption, the accumulated heat results in a gradual rise in the lattice temperature as shown in the figure. Note that the response time in the thermal effect is very slow. Therefore, due to the lattice temperature effect, the drain current falls accordingly to a stable DC value.

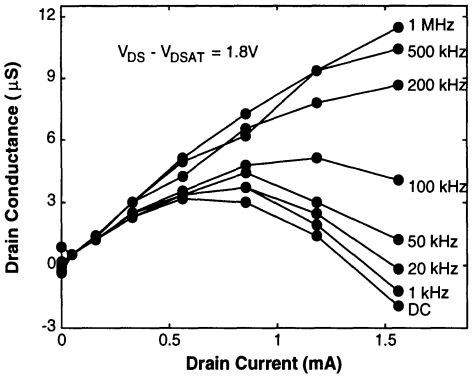


Figure 5.68: Small-signal output conductance of a partially-depleted SOI NMOS device with an aspect ratio of $20\mu m/5\mu m$, a front gate oxide of 250Å, a buried oxide of 4150Å, and a silicon thin-film of 1780Å, biased with $V_{DS} - V_{DSAT} = 1.8V$ and with its body tied to source. A sinusoidal signal with various frequencies is imposed at the drain.

As described in the previous paragraph, it takes some time for self heating of an SOI MOS device. Therefore, depending on the frequency of the imposed input signal to an SOI MOS device, the influence of self-heating varies. Fig. 5.68 shows the small-signal output conductance of a partially-depleted SOI NMOS device with an aspect ratio of $20\mu m/5\mu m$, a front gate oxide of 250Å, a buried oxide of 4150Å, and a silicon thin-film of 1780Å, biased with $V_{DS} - V_{DSAT} = 1.8V$ and with its body tied to source. A sinusoidal signal with various frequencies is imposed at the drain[92]. As shown in the figure, when a 1MHz sinusoidal signal is imposed at the drain, the response of self-heating is lagging behind. Therefore, its output conductance is identical to the one as for the bulk devices— the output conductance is linearly proportional to the drain current. When the frequency of the input sinusoidal signal falls, self-heating gradually affects the device operation. As a result, the output conductance decreases when the drain current rises. When the frequency is smaller than 20KHz, even a negative output conductance can be seen. Therefore, self-heating is most noticeable when the frequency of the imposed input signal is low.

In addition to self-heating, thermal coupling among devices in a circuit using SOI MOS devices is also important for thermal analysis. Here, a current mirror circuit is used to exemplify the thermal coupling effect. Fig. 5.69 shows the rise in V_{in} versus

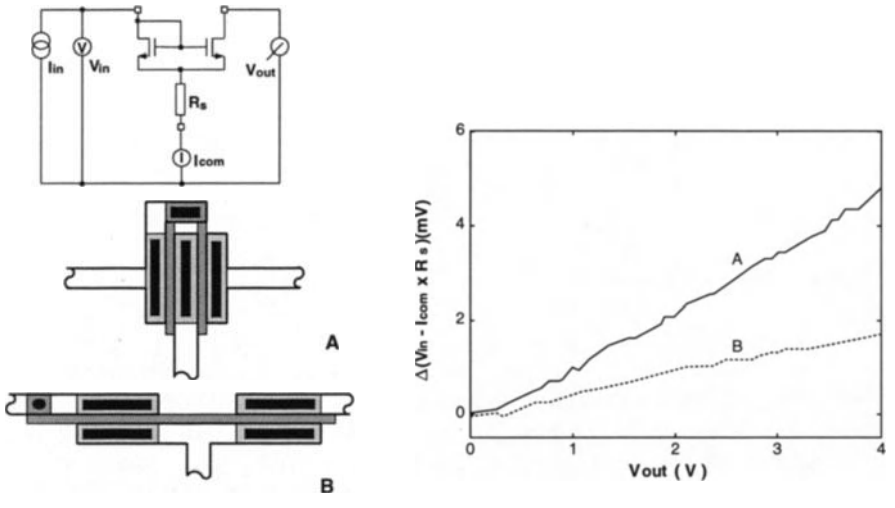


Figure 5.69: Rise in V_{in} versus V_{out} of a current mirror circuit with various layouts of fully-depleted SOI NMOS devices with an aspect ratio of $20\mu m/2\mu m$, a buried oxide of 3000Å, and a silicon thin-film of 1000Å.

V_{out} of a current mirror circuit with various layouts of full-depleted SOI NMOS devices with an aspect ratio of $20\mu m/2\mu m$, a buried oxide of 3000Å, and a silicon thin-film of 1000Å[93]. In layout A, the source terminals of the two devices in the current mirror circuit share the same region. Therefore, via the shared source silicon thin-film area, the heat from one device can affect the other. In layout B, except the polysilicon gate and the metal interconnect, two devices are separated from each other. During the measurement, at the diode-connected side of the current mirror circuit, a constant current source of I_{in} is imposed. By changing the voltage at the output end (V_{out}), the V_{GS} of the diode-connected device—V_{in} is measured. The purpose of this experiment is to see the thermal coupling from the output device to the diode-connected device. As shown in the figure, when the output voltage is changed, the input voltage is changed accordingly due to the thermal coupling effect. When V_{out} becomes higher, the power dissipation and thus the lattice temperature of the output device rise accordingly. Via thermal coupling between devices, the lattice temperature of the input diode-connected device also rises. Therefore, the carrier mobility of the input diode-connected device drops. Consequently, the input voltage needs to increase such that a constant current (I_{in}) can be maintained. Therefore, thermal coupling between two devices can be measured using this current mirror

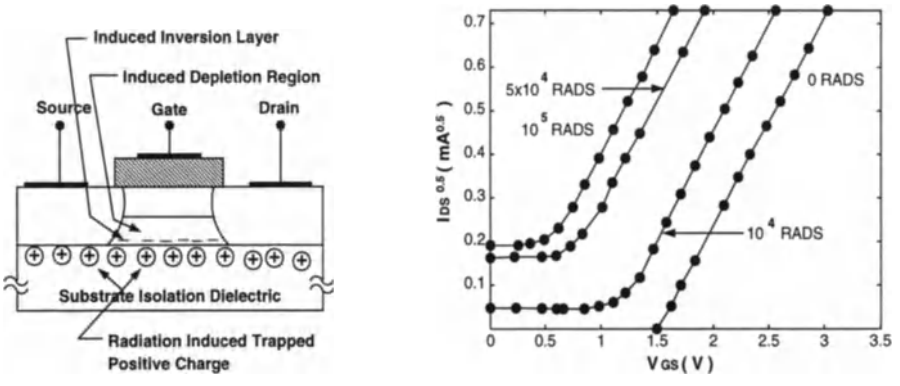


Figure 5.70: $\sqrt{I_D}$ versus V_G of an SOS(silicon-on-sapphire) NMOS device for various ionizing dose levels.

circuit. Compared to layout B, thermal coupling between two devices in the current mirror circuit using layout A is more noticeable. Depending on the layout of the circuit, thermal coupling between devices also takes time [94]. For example, for the current mirror circuit using layout A, the time for the thermal coupling from the output device to the input diode-connected device takes about 7μs, which is much longer than those observed for self-heating of individual devices. Therefore, the thermal effect in SOI MOS devices is also layout-dependent.

5.11 Radiation Hardness

Owing to isolation from the buried oxide, SOI MOS devices are known for their radiation hardness capability. With the buried oxide structure, the photo-current generated from radiation can be reduced in SOI MOS devices. However, when ionizing radiation penetrates through the oxide, electrons and holes are generated and move under the influence of the electric field. Some electrons may move out of the oxide. Holes move toward the negative electrode and may be trapped in the oxide. The most serious case is when the trapped positive charge exists at the oxide interface. Under this situation, device performance can be substantially affected. In this section, the radiation effect on the leakage current, the threshold voltage, the subthreshold slope, the strong-inversion drain current, and the transient performance of SOI MOS devices is analyzed sequentially.

This trapped positive charge may cause strong inversion at the bottom of the

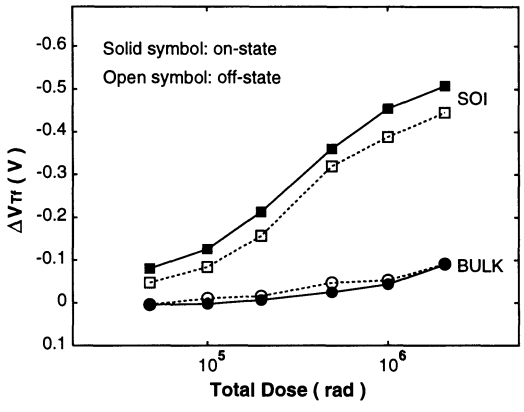


Figure 5.71: Threshold voltage shift versus total radiation dose of a fully-depleted SOI PMOS device with a channel length of 4.3μm, a front gate oxide of 109Å, a buried oxide of 3800Å, and a silicon thin-film of 450Å.

silicon thin-film. As a result, the front gate has no control over the back channel. Fig. 5.70 shows $\sqrt{I_D}$ versus V_G of an SOS(silicon-on-sapphire) NMOS device for various ionizing dose levels[95]. As shown in the figure, when the gate voltage is small, a substantial amount of leakage current exists. In addition, with a higher ionizing dose level, the amount of the leakage current is larger since the back channel at the bottom of the silicon thin-film caused by the trapped positive charge at the oxide interface turns stronger.

Fig. 5.71 shows the threshold voltage shift versus total radiation dose of a fully-depleted SOI PMOS device with a channel length of 4.3μm, a front gate oxide of 109Å, a buried oxide of 3800Å, and a silicon thin-film of 450Å [96]. The trapped charge caused by radiation depends on the biasing condition of the device when exposed to radiation. In the figure, on-state means that the device is exposed to radiation when the device is biased at $V_{G1} = -4V$ and $V_D = 0$. Off-state means that the device is exposed to radiation when the device is biased at $V_{G1} = 0V$ and $V_D = -4V$. Also shown in the figure is the result for a compatible bulk device. As shown in the figure, when the radiation dose increases, the threshold voltage shift rises due to the increased amount of trapped charge at the oxide interface. Compared to the bulk device, the SOI device shows a much worse threshold voltage shift from radiation because more holes are trapped in the buried oxide. Fig. 5.72 shows the subthreshold characteristics and the strong-inversion drain current degra-

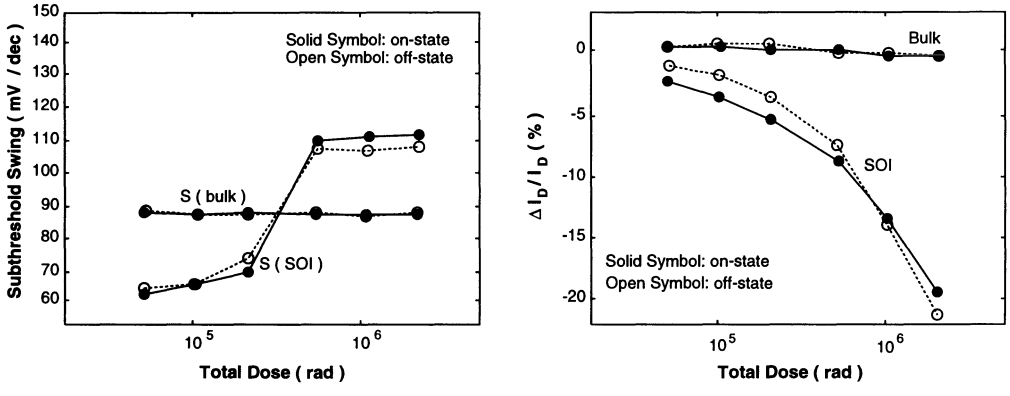


Figure 5.72: Subthreshold characteristics and the strong-inversion drain current degradation versus total radiation dose of the fully-depleted SOI PMOS device with its parameters as described in the previous figure.

dation versus total radiation dose of the fully-depleted SOI PMOS device with its parameters as described in the previous figure[96]. As shown in the figure, without radiation, the subthreshold slope of the SOI device is better than that of the bulk device. When the radiation dose increases, the difference in the subthreshold slope between the bulk and the SOI devices narrows. When the radiation dose exceeds 5×10^5rad, the subthreshold slope of the SOI device becomes worse than that of the bulk device due to the hole trapping in the buried oxide via electrostatic coupling between the front and the back oxide interfaces. On the other hand, the strong-inversion drain current of the bulk device is insensitive to the radiation dose. In contrast, the SOI device is quite sensitive to it. With a larger radiation dose, the strong-inversion drain current degrades more for the SOI device.

In addition to the effects described above, the transconductance of an SOI MOS device is strongly affected by the radiation. Fig. 5.73 shows the transconductance versus gate voltage of an SOI NMOS device with a silicon thin-film of 1500Å[97]. As shown in the figure, when the radiation dose increases, the transconductance curve shifts toward the negative direction. This implies that a large amount of trapped charge at the buried oxide interface makes the threshold voltage move left. In addition, with radiation, when the gate voltage decreases, the transconductance does not fall from its peak value directly. Instead, with radiation its transconductance falls from peak more slowly due to the back channel induced by the trapped positive charge at the buried oxide interface. From the figure, the peak value of transcon-

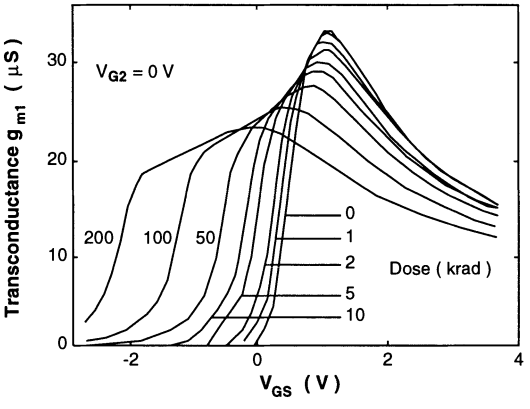


Figure 5.73: Transconductance versus gate voltage of an SOI NMOS device with a silicon thin-film of 1500Å.

ductance falls when the radiation dose increases—with a higher radiation dose, the quality of the silicon thin-film, the carrier mobility, and parasitic resistance become worse.

The damage caused by radiation can be recovered by an isothermal anneal at 140C. Fig. 5.74 shows the drain leakage current versus gate voltage of an SOI MOS device with various isothermal annealing times[98]. From this figure, when the annealing time becomes longer, the leakage current caused by the Co^{60} gamma irradiation becomes smaller, even back to the previous undamaged value.

Fig. 5.75 shows single-ion particle effects on an SOI NMOS device[99][100]. When a single-ion particle hits an SOI NMOS device accidentally, a large amount of electrons and holes are produced. Electrons are collected by the drain. The generated holes move to the silicon thin-film body. As a result, a pulse of the drain current, which is the ion current as shown in the figure, can be seen. Due to the remaining holes, the potential of the silicon thin-film body rises, which triggers the turn-on of the parasitic BJT. As a result, the leakage current with a long period can be seen.

5.12 Noise

In this section, noise behavior of the SOI CMOS devices is described. First, the noise spectrum of a partially-depleted SOI CMOS device is described. The noise

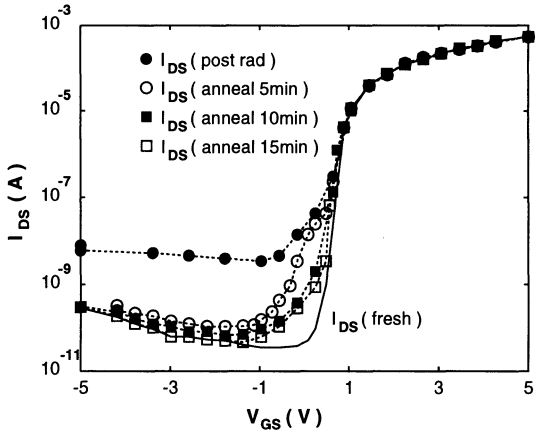


Figure 5.74: Drain leakage current versus gate voltage of an SOS MOS device with various isothermal annealing times.

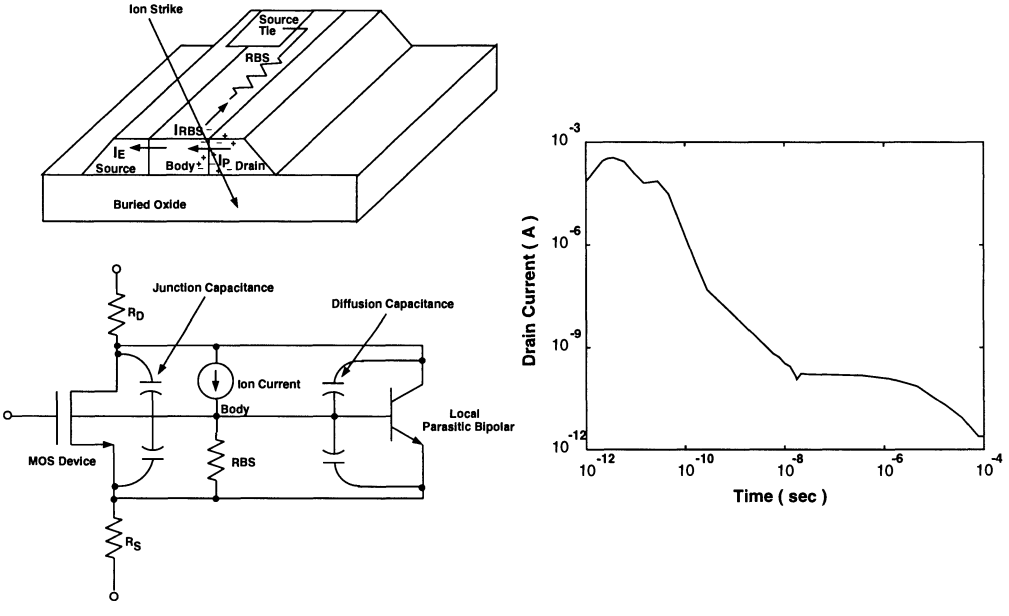


Figure 5.75: Single-ion particle effects on an SOI NMOS device.

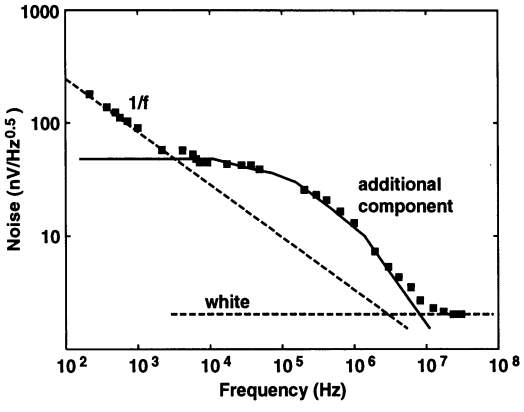


Figure 5.76: Noise spectrum of a partially-depleted SOI CMOS device with a front gate oxide of 230Å, a buried oxide of 3800Å, and a silicon thin-film of 1500Å.

in a partially-depleted CMOS device is also related to the kink effect. In the final portion of this section, the kink effect related noise is analyzed.

Fig. 5.76 shows the noise spectrum of a partially-depleted SOI CMOS device with a front gate oxide of 230Å, a buried oxide of 3800Å, and a silicon thin-film of 1500Å[101]. As shown in the figure, in the low frequency regime ($f < 1KHz$), it is dominated by the $1/f$ flicker noise. In the high frequency regime ($f > 10MHz$), it is dominated by white noise. As for the bulk CMOS devices, the flicker noise of the SOI CMOS devices is due to the surface scattering at the $Si - SiO_2$ interface. The white noise is due to random motion of the carriers at the operating temperature. As shown in the figure, between the flicker noise regime and the white noise regime, there is a hump in the noise characteristics, which is owing to the equivalent resistance of the neutral region in the silicon thin-film of the partially-depleted SOI MOS devices. This noise hump caused by the equivalent resistance of the neutral region, is filtered by a RC low-pass filter, where R is the equivalent resistance of the neutral region and C is made of the capacitances from the front and buried oxides.

In addition to the hump noise described above, for a partially-depleted MOS device, there is a noise overshoot, which is related to the kink effect. Fig. 5.77 shows the normalized drain current noise versus drain voltage of a partially-depleted SOI NMOS device with an aspect ratio of 9.5μm/1μm, a front gate oxide of 115Å, a buried oxide of 3000Å, a silicon thin-film of 1000Å, an aspect ratio of W/L =

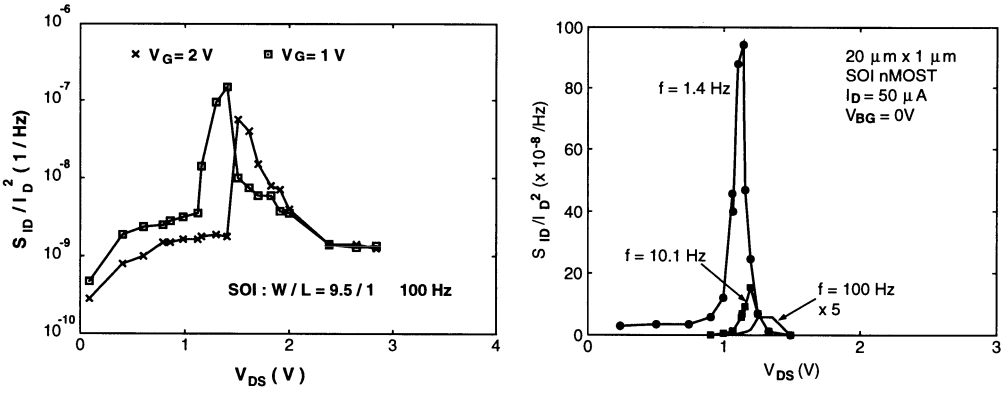


Figure 5.77: Normalized drain current noise versus drain voltage of a partially-depleted SOI NMOS device with an aspect ratio of 9.5μm/1μm, a front gate oxide of 115Å, a buried oxide of 3000Å, a silicon thin-film of 1000Å (left device), an aspect ratio of W/L = 20μm/1μm, a front gate oxide of 200Å, a buried oxide of 4000Å, and a silicon thin-film of 1800Å (right device).

20μm/1μm, a front oxide of 200Å, a buried oxide of 4000Å, and a silicon thin-film of 1800Å [102][103]. As shown in the figure, at certain frequencies, there exists a noise overshoot, which occurs at a biasing condition where the kink effect also happens. With the similar reasoning as for the kink effect, the noise overshoot is also due to impact ionization. The holes generated from impact ionization flow to the bottom of the silicon thin-film. As a result, trapping and detrapping between these holes and the interface states at the buried oxide interface lead to this extra noise source, which is further affected by the floating body and the parasitic BJT. At the onset of the kink effect, the conductance of the body-to-source diode is highest. Therefore, propagation of this extra noise source is the most at the onset of the kink effect— the kink-effect related noise overshoot. The kink-effect related noise overshoot, which is low-frequency noise[103], is especially noticeable at a frequency below 100Hz.

Fig. 5.78 shows the comparison of the low-frequency noise spectra in single-gate and double-gate SOI NMOS devices with various aspect ratios, a front gate oxide of 300Å, and a silicon thin-film of 1000Å for the double-gate and 1200Å for the single-gate doped with a density of $5 \times 10^{16} cm^{-3}$[104]. As shown in the figure, the double-gate device has a much lower noise level than the single-gate device. Fig. 5.79 shows the equivalent gate voltage noise versus drain voltage of the single-gate and

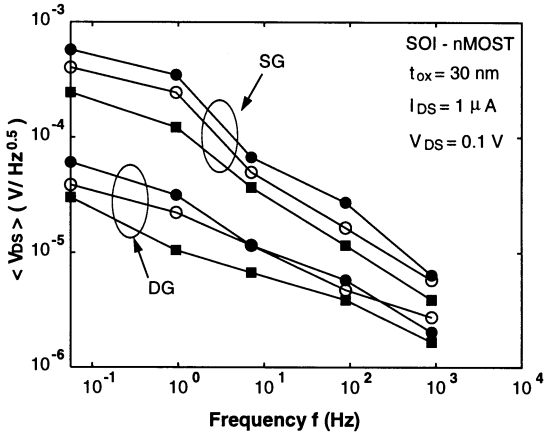


Figure 5.78: Comparison of the low-frequency noise spectra in single-gate and double-gate SOI NMOS devices with various aspect ratios, a front gate oxide of 300Å, and a silicon thin-film of 1000Å for the double-gate and 1200Å for the single-gate doped with a density of $5 \times 10^{16} cm^{-3}$.

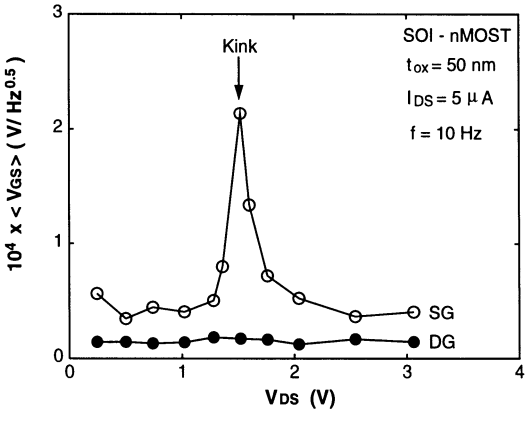


Figure 5.79: Equivalent gate voltage noise versus drain voltage of the single-gate and the double-gate SOI NMOS devices, with a front gate oxide of 500Å, biased at a drain current level of 5μA and operating at 10Hz.

the double-gate SOI NMOS devices, with a front gate oxide of 500Å, biased at a drain current level of 5μA and operating at 10Hz[104]. As shown in the figure, compared to the single-gate device, in addition to a lower noise level, the double-gate device does not have noise overshoot, which is due to the fact that the double-gate device is more easily fully-depleted. Besides, there are no interface states at the buried oxide interface in the double-gate devices.

5.13 Summary

In this chapter, DC and the capacitance models for the accumulation-mode SOI MOS devices have been presented. Sensitivity of the threshold voltage to the silicon thin-film thickness of SOI CMOS devices has been studied. When the silicon thin-film is too thin, the threshold voltage of the SOI CMOS devices may be very sensitive to the silicon thin-film thickness. For partially-depleted SOI MOS devices, due to the floating body structure, impact ionization and parasitic BJT effects are important. The kink effect in the strong inversion region and the peculiar subthreshold characteristics have been analyzed. Due to the floating body structure, the positive feedback in the device causes the single-transistor latch phenomenon. The drain breakdown voltage can also be affected by the floating body. The subthreshold behavior of the partially-depleted SOI MOS devices have been analyzed. A SiGe-implanted SOI MOS device to reduce the floating body effect has also been reported. Due to the floating body structure, transient performance of SOI CMOS devices may be quite different from that of bulk ones. Transient analysis of SOI CMOS devices has been described. As for bulk CMOS devices, deep-submicron SOI CMOS devices also have hot carrier effects due to the high electric field in the lateral channel. Hot carrier effects of the SOI CMOS devices have been analyzed. Due to the poor heat dissipation capability from the buried oxide structure, the temperature effect is important in SOI CMOS devices. Thermal analysis of the SOI CMOS devices has been presented. Owing to the buried oxide structure, SOI CMOS devices also have superior properties in radiation hardness. Radiation hardness and the noise analysis of SOI MOS devices have also been analyzed.

References

[1] D. Flandre, A. Terao, P. Francis, B. Gentinne and J.-P. Colinge, "Demonstration of The Potential of Accumulation-Mode MOS Transistors on SOI Substrates for High-Temperature Operation (150-300C)," *IEEE Elec. Dev. Let.*, Vol. 14, No. 1, pp. 10-12, Jan. 1993.

[2] O. Faynot, S. Cristoloveanu, A. J. Auberton-Herve and C. Raynaud, "Performance and Potential of Ultrathin Accumulation-Mode SIMOX MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 4, pp. 713-719, Apr. 1995.

[3] A. Acovic, L. K. Wang, F. Brady, and N. Haddad, "Hot-Carrier Reliability of Fully Depleted Accumulation Mode SOI MOSFETs," *SOI Conf. Dig.*, pp. 134-135, 1992.

[4] Q. Tong, X. Xu and H. Zhang, "Elimination of Kink Effect in Fully Depleted Complementary Buried-Channel SOI MOSFET (FD CBCMOS) Based on Silicon Direct Bonding Technology," *IEEE Elec. Dev. Let.*, Vol. 12, No. 3, pp. 101-103, Mar. 1991.

[5] L. K. Wang, J. Seliskar, T. Bucelot, A. Edenfeld and N. Haddad, "Enhanced Performance of Accumulation Mode 0.5um CMOS/SOI Operated at 300K and 85K," *IEDM Dig.*, pp. 679-682, 1991.

[6] Y. Kado, T. Ohno, M. Harada, K. Deguchi and T. Tsuchiya, "Enhanced Performance of Multi-GHz PLL LSIs Using Sub-1/4-micron Gate Ultrathin Film CMOS/SIMOX Technology with Synchrotron X-ray Lithography," *IEDM Dig.*, pp. 243-246, 1993.

[7] C. Raynaud, J. L. Pelloie, O. Faynot, B. Dunne and J. Hartmann, "Fully-Depleted Accumulation-Mode PMOSFET for 0.2um SOI Technology," *SOI Conf. Dig.*, pp. 12-13, 1995.

[8] J. Colinge, "Conduction Mechanisms in Thin-Film Accumulation-Mode SOI p-Channel MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 37, No. 3, pp. 718-723, Mar. 1990.

[9] A. Terao, D. Flandre, E. Lora-Tamayo and F. Van de Wiele, "Measurement of Threshold Voltages of Thin-Film Accumulation-Mode PMOS/SOI Transistors," *IEEE Elec. Dev. Lett.*, Vol. 12, No. 12, pp. 682-684, Dec. 1991.

[10] K. W. Su and J. B. Kuo, "Accumulation-type vs. Inversion-type: Narrow Channel Effect in VLSI Mesa-Isolated Fully-Depleted Ultra-thin SOI PMOS Devices," *SOI Conf. Dig.*, pp. 38-39, 1995.

[11] D. Flandre and S. Cristoloveanu, "Latch and Hot-Electron Gate Current in Accumulation-Mode SOI p-MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 15, No. 5, pp. 157-159, May 1994.

[12] J. A. Martino, A. L. P. Rotondaro, E. Simoen, U. Magnusson and C. Claeys, "Transient Effects in Accumulation Mode p-Channel SOI MOSFET's Operating at 77K," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 4, pp. 519-523, Apr. 1994.

[13] A. L. P. Rotondaro, U. K. Magnusson, C. Claeys, D. Flandre, A. Terao and J. Colinge, "Evidence of Different Conduction Mechanisms in Accumulation-Mode p-Channel SOI MOSFET's at Room and Liquid-Helium Temperatures," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 4, pp. 727-732, Apr. 1993.

[14] N. Lukyanchikova, M. Petrichuk and M. Garbar, "Results on Noise Examination of Fully-Depleted Accumulation Mode SOI pMOSFETs," *SOI Conf. Dig.*, pp. 36-37, 1995.

[15] D. Flandre and A. Terao, "Extended Theoretical Analysis of The Steady-State Linear Behaviour of Accumulation-Mode, Long-Channel p-MOSFETs on SOI Substrates," *Sol. St. Elec.*, Vol. 35, No. 8, pp. 1085-1092, Aug. 1992.

[16] H. Joachim, Y. Yamaguchi, Y. Inoue, T. Nishimura and N. Tsubouchi, "Analytical Modeling of Short-Channel Behavior of Accumulation-Mode Transistors on Silicon-on-Insulator Substrate," *Jpn J. Appl. Phys.*, Vol. 33, No. 1B, pp. 558-562, Jan. 1994.

[17] G. Niu and G. Ruan, "An Analytical Back Gate Bias Dependent Subthreshold Swing Model for Accumulation-Mode p-Channel SOI MOSFETs," *Sol. St. Elec.*, Vol. 38, No. 10, pp. 1805-1810, Oct. 1995.

[18] H. Haddara, T. Elewa and S. Cristoloveanu, "Static and Dynamic Transconductance Model for Depletion-Mode Transistors: A New Characterization Method for Silicon-on-Insulator Materials," *IEEE Elec. Dev. Let.*, Vol. 9, No. 1, pp. 35-37, Jan. 1988.

[19] J. Sim and J. B. Kuo, "An Analytical Back-Gate Bias Effect Model for Ultrathin SOI CMOS Devices," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 4, pp. 755-765. Apr. 1993.

[20] F. Balestra, J. Brini and G. Ghibaudo, "Analytical Modeling of Ultra-Thin Film Depletion-Mode SOI MOSFETs," *Sol. St. Elec.*, Vol. 34, No. 12, pp. 1361-1364, Dec. 1991.

[21] K. W. Su and J. B. Kuo, "Analysis of Current Conduction in Short-Channel Accumulation-Mode SOI PMOS Devices," *IEEE Trans. Elec. Dev.*, Vol. 44, No. 5, pp. 832-840, May 1997.

[22] P. C. Yeh and J. G. Fossum, "Physical Subthreshold MOSFET Modeling Applied to Viable Design of Deep-Submicrometer Fully Depleted SOI Low-Voltage CMOS Technology," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 9, pp. 1605-1613, Sep. 1995.

[23] D. M. Caughey and R. E. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Field," *Proc. IEEE*, Vol. 55, No. 12, pp. 2192-2193, Dec. 1967.

[24] Y.-G. Chen, S.-Y. Ma, J. B. Kuo, Z. Yu and R. W. Dutton, "An Analytical Drain Current Model Considering Both Electron and Lattice Temperatures Simultaneously for Deep Submicron Ultrathin SOI NMOS Devices with Self-Heating," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 5, pp. 899-906, May 1995.

[25] Y. P. Tsividis, "Operation and Modeling of The MOS Transistor," *McGraw-Hill: New York*, 1988.

[26] M. J. Van der Tol and S. G. Chamberlain, "Buried-Channel MOSFET Model for SPICE," *IEEE Trans. CAD of IC*, Vol. 10, No. 8, pp. 1015-1035, Aug. 1991.

[27] P. Antognetti, D. D. Caviglia and E. Profumo, "CAD Model for Threshold and Subthreshold Conduction in MOSFET's," *IEEE J. Sol. St. Ckts*, Vol. 17, No. 3, pp. 454-458, Jun. 1982.

[28] B. J. Sheu, D. L. Scharfetter, P.-K. Ko and M.-C. Jeng, "BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors," *IEEE J. Sol. St. Ckts*, Vol. 22, No. 4, pp. 558-566, Aug. 1987.

[29] J. B. Kuo, "CMOS Digital IC," *McGraw-Hill:Taipei*, 1996.

[30] K. W. Su and J. B. Kuo, "Analytical Capacitance Model for Submicron Accumulation-Mode SOI MOS Devices," *Sol. St. Elec.*, Vol. 42, No. 4, pp. 513-522, Apr. 1998.

[31] B. Gentinne, D. Flandre, A. Terao, and J.-P. Colinge, "Intrinsic Gate Capacitances and Large-Signal Transient Modeling of Thin-Film Accumulation-Mode P-Channel SOI MOSFETs," *SOI Conf. Dig.*, pp. 52-53, 1992.

[32] D. E. Ward and R. W. Dutton, "A Charge-Oriented Model for MOS Transistor Capacitances," *IEEE J. Sol. St. Ckts*, Vol. 13, No. 5, pp. 703-708, Oct. 1978.

[33] H. K. Lim and J. G. Fossum, "A Charge-Based Large-Signal Model for Thin-Film SOI MOSFET's," *IEEE J. Sol. St. Ckts*, Vol. 20, No. 1, pp. 366-377, Feb. 1985.

[34] B. J. Sheu and P. -K. Ko, "Measurement and Modeling of Short-Channel MOS Transistor Gate Capacitances," *IEEE J. Sol. St. Ckts*, Vol. 22, No. 3, pp. 464-472, Jun. 1987.

[35] R. Shrivastava and K. Fitzpatrick, "A Simple Model for the Overlap Capacitance of a VLSI MOS Device," *IEEE Trans. Elec. Dev.*, Vol. 29, No. 12, pp. 1870-1875, Dec. 1982.

[36] H. Iwai, M. R. Pinto, C. S. Rafferty, J. E. Oristian and R. W. Dutton, "Velocity Saturation Effect on Short-Channel MOS Transistor Capacitance," *IEEE Elec. Dev. Let.*, Vol. 6, No. 3, pp. 120-122, Mar. 1985.

[37] B. Iniguez, L. F. Ferreira, B. Gentinne, and D. Flandre, "A Physically-Based C_∞-Continuous Fully-Depleted SOI MOSFET Model for Analog Applications," *IEEE Trans. Elec. Dev.*, Vol. 43, No. 4, pp.568-575, April 1996.

[38] E. Leobandung and S. Y. Chou, "Threshold Voltage Sensitivity of 0.1μm Channel Length Fully-Depleted SOI NMOSFET's with Back-Gate Bias," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 9, pp.1707-1708, Sept. 1995.

[39] M. J. Sherony, L. T. Su, J. E. Chung, and D. A. Antoniadis, "Reduction of Threshold Voltage Sensitivity in SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 16, No. 3, pp. 100-102, March 1995.

[40] R. Howes and W. Redman-White, "A Small-Signal Model for the Frequency-Dependent Drain Admittance in Floating-Substrate MOSFET's," *IEEE J. Sol. St. Ckts*, Vol. 27, No. 8, pp. 1186-1193, Aug. 1992.

[41] H.-K. Yu, J.-S. Lyu, S.-W. Kang, and C.-K. Kim, "A Physical Model of Floating Body Thin Film Silicon-On-Insulator nMOSFET with Parasitic Bipolar Transistor," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 5, pp. 726-733, May 1994.

[42] C. F. Edwards, W. Redman-White, B. M. Tenbroek, M. S. L. Lee, and M. J. Uren, "The Effect of Body Contact Series Resistance on SOI CMOS Amplifier Stages," *IEEE Trans. Elec. Dev.*, Vol. 44, No. 12, pp. 2290-2294, Dec. 1997.

[43] S. S. Chen and J. B. Kuo, "An Analytical CAD Kink Effect Model of Partially-Depleted SOI NMOS Devices Operating in Strong Inversion," *Sol. St. Elec.*, Vol. 41, No. 3, pp. 447-458, March 1997.

[44] K. K. Young and J. A. Burns, "Avalanche-Induced Drain-Source Breakdown in Silicon-on-Insulator n-MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 35, No. 4, pp. 426-431, Apr. 1988.

[45] Y. G. Chen, J. B. Kuo, Z. Yu, and R. W. Dutton, "An Analytical Drain Current Model for Short-Channel Fully-Depleted Ultrathin Silicon-on-Insulator NMOS Devices," *Sol. St. Elec.*, Vol. 38, No. 12, pp. 2051-2057, Dec. 1995.

[46] Y. A. El-Mansy and D. M. Caughey, "Modeling Weak Avalanche Multplication Currents in IGFETs and SOS Transistors for CAD," *IEDM Dig.*, pp.31-34, 1975.

[47] T. Skotnicki, G. Merckel and A. Merrachi, "New Physcial Model of Multiplication-Induced Breakdown in MOSFET's," *Sol. St. Elec.*, Vol. 34, No. 11, pp.1297-1307, Nov. 1991.

[48] H.-T. H. Chen, and R.-S. Huang, "Modeling for Floating Body Effects in Fully Depleted SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 3, pp. 583-590, March 1993.

[49] E. P. Ver Ploeg, C. T. Nguyen, S. S. Wong, and J. D. Plummer, "Parasitic Bipolar Gain in Fully Depleted n-Channel SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 6, pp. 970-977, June 1994.

[50] J. Chen, F. Assaderaghi, H.-J. Wann, P.-K. Ko and C. Hu, "An Accurate Model of Thin Film SOI MOSFET Breakdown Voltage," *IEDM Dig.*, pp.671-674, 1991.

[51] J.-Y. Choi and J. G. Fossum, "Analysis and Control of Floating-Body Bipolar Effects in Fully Depleted Submicrometer SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 6, pp. 1384-1391, June 1991.

[52] J.-P. Colinge, "Reduction of Kink Effect in Thin-Film SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 9, No. 2, pp. 97-99, Feb. 1988.

[53] J. Tihanyi and H. Schlotterer, "Properties of ESFI MOS Transistors due to the Floating Substrate and the Finite Volume," *IEEE Trans. Elec. Dev.*, Vol. 22, No. 11, pp. 1017-1023, Nov. 1975.

[54] D. Suh and J. G. Fossum, "A Physical Charge-Based Model for Non-Fully Depleted SOI MOSFET's and its Use in Assessing Floating-Body Effects in SOI CMOS Circuits," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 4, pp.728-737, Apr. 1995.

[55] K. Kato, T. Wada and K. Taniguchi, "Analysis of Kink Characteristics in Silicon-on-Insulator MOSFET's using Two-Carrier Modeling," *IEEE Trans. Elec. Dev.*, Vol. 32, No. 2, pp. 458-462, Feb. 1985.

[56] J.-P. Colinge, "Reduction of Floating Substrate Effect in Thin-Film SOI MOSFET's," *Elec. Let.*, Vol. 22, No. 4, p.187, Feb. 1986.

[57] A. Bar-Lev, Semiconductors and Electronic Devices, Third Ed., *Prentice Hall:New York* (1993).

[58] D. J. Roulston, Bipolar Semiconductor Devices, *McGraw-Hill: New York* (1990).

[59] Y. G. Chen and J. B. Kuo, "A Unified Triode/Saturation Model with an Improved Continuity in the Output Conductance Suitable for CAD of VLSI Circuits Using Deep Sub-0.1μm NMOS Devices," *IEEE Trans. CAD of IC*, Vol. 15, No. 2, pp. 256-258, Feb. 1996.

[60] D. J. Roulston, N. D. Arora and S. G. Chamberlain, "Modeling and Measurement of Minority-Carrier Lifetime versus Doping in Diffused Layers of $n^+ - p$ Silicon Diodes," *IEEE Trans. Elect. Dev.*, Vol. 29, No. 2, pp. 284-291, Feb. 1982.

[61] F.-C. Hsu, P.-K. Ko, S. Tam, C. Hu and R. S. Muller, "An Analytical Breakdown Model for Short-Channel MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 29, No. 11, pp. 1735-1740, Nov. 1982.

[62] T. Y. Chan, P. K. Ko and C. Hu, "A Simple Method to Characterize Substrate Current in MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 5, No. 12, pp. 505-507, Dec. 1984.

[63] J. S. T. Huang, J. S. Kueng and T. Fabian, "An Analytical Model for Snapback in n-Channel SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 9, pp. 2082-2091, Sept. 1991.

[64] R. Werner, C. Zimmermann, and A. Kalz, "Light Dependence of Partially Depleted SOI-MOSFET's Using SIMOX Substrates," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 9, pp. 1653-1656, Sept. 1995.

[65] J. R. Davis, A. E. Glaccum, K. Reeson, and P. L. F. Hemment, "Improved Subthreshold Characteristics of n-Channel SOI Transistors," *IEEE Elec. Dev. Let.*, Vol. 7, No. 10, pp.570-572, Oct. 1986.

[66] S. S. Chen, S. C. Lin, and J. B. Kuo, "Kink Effect on Subthreshold Current Conduction Mechanism for n-Channel Metal-Oxide-Silicon Devices," *J. Appl. Phys.*, Vol. 80, No. 10, pp.5821-5827, Nov. 1996.

[67] C.-E. D. Chen, M. Matloubian, R. Sundaresan, B.-Y. Mao, C. C. Wei, and G. P. Pollack, "Single-Transistor Latch in SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 9, No. 12, pp.636-638, Dec. 1988.

[68] M. Yoshimi, M. Terauchi, A. Nishiyama, O. Arisumi, A. Murakoshi, K. Matsuzawa, N. Shigyo, S. Takeno, M. Tomita, K. Suzuki, Y. Ushiku, and H. Tango, "Suppression of the Floating-Body Effect in SOI MOSFET's by the Bandgap Engineering Method Using a $Si_{1-x}Ge_x$ Source Structure," *IEEE Trans. Elec. Dev.*, Vol. 44, No. 3, pp. 423-430, March 1997.

[69] G. G. Shahidi, C. A. Anderson, B. A. Chappell, T. I. Chappell, J. H. Comfort, B. Davari, R. H. Dennard, R. L. Franch, P. A. McFarland, J. S. Neely, T. H. Ning, M. R. Polcari, and J. D. Warnock, "A Room Temperature 0.1μm CMOS on SOI," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 12, pp. 2405-2412, Dec. 1994.

[70] H. C. Shin, I.-S. Lim, M. Racanelli, W.-L. M. Huang, J. Foerstner, and B.-Y. Hwang, "Analysis of Floating Body Induced Transient Behaviors in Partially Depleted Thin Film SOI Devices," *IEEE Trans. Elec. Dev.*, Vol. 43, No. 2, pp. 318-325, Feb. 1996.

[71] J. Gautier, K. A. Jenkins, and J. Y.-C. Sun, "Body Charge Related Transient Effects in Floating Body SOI NMOSFET's," *IEDM Dig.*, pp.623-626, 1995.

[72] A. Wei, M. J. Sherony, and D. A. Antoniadis, "Transient Behavior of the Kink Effect in Partially-Depleted SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 16, No. 11, pp. 494-496, Nov. 1995.

[73] K. Kato and K. Taniguchi, "Numerical Analysis of Switching Characteristics in SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 33, No. 1, pp. 133-139, Jan. 1986.

[74] M. M. Pelella, J. G. Fossum, D. Suh, S. Krishnan, K. A. Jenkins, and M. J. Hargrove, "Low-Voltage Transient Bipolar Effect Induced by Dynamic Floating-Body Charging in Scaled PD/SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 17, No. 5, pp. 196-198, May 1996.

[75] A. Wei and D. A. Antoniadis, "Measurement of Transient Effects in SOI DRAM/SRAM Access Transistors," *IEEE Elec. Dev. Let.*, Vol. 17, No. 5, pp. 193-195, May 1996.

[76] K. Ueda, H. Morinaka, Y. Yamaguchi, T. Iwamatsu, I. J. Kim, Y. Inoue, K. Mashiko, and T. Sumi, "Floating-Body Effects on Propagation Delay in SOI/CMOS LSIs," *SOI Conf. Dig.*, pp. 142-143, 1996.

[77] B. Zhang and T. P. Ma, "Front-Channel Hot-Carrier Effect on the Drain-Source Breakdown Voltage in Thin-Film SOI/NMOSFET's," *SOI Conf. Dig*, pp.126-127, 1992.

[78] J. Chen, K. Quader, R. Solomon, T. Chan, P. Ko, and C. Hu, "Hot Electron Gate Current and Degradation in P-Channel SOI MOSFET's," *SOI Conf. Dig.*, pp. 8-9, 1991.

[79] T. Tsuchiya and T. Ohno, "New Hot-Carrier-Degradation Mode in Thin-Film SOI nMOSFET's," *IEEE Elec. Dev. Let.*, Vol. 16, No. 10, pp.427-429, Oct. 1995.

[80] L. T. Su, H. Fang, J. E. Chung, and D. A. Antoniadis, "Hot-Carrier Effects in Fully-Depleted SOI NMOSFETs," *IEDM Dig.*, pp.349-352, 1992.

[81] J. Wang-Ratkovic, W. M. Huang, B. Y. Hwang, M. Racanelli, J. Forestner, and J. Woo, "Novel Device Lifetime Behavior and Hot-Carrier Degradation Mechanisms Under $V_{GS} \cong V_{TH}$ Stress for Thin-Film SOI nMOSFETs," *IEDM Dig.*, pp.639-642, 1995.

[82] S. Maeda, Y. Yamaguchi, I.-J. Kim, H.-O. Joachim, Y. Inoue, H. Miyoshi, and A. Yasuoka, "A Method for the Prediction of Hot-Carrier Lifetime in Floating SOI NMOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 44, No. 12, pp. 2200-2206, Dec. 1997.

[83] H.-J. Wann, J. Kim, J. Chen, P. K. Ko, and C. Hu, "Hot-Carrier Currents of SOI MOSFETs," *SOI Conf. Dig.*, pp. 118-119, 1993.

[84] Z. J. Ma, H. J. Wann, M. Chan, J. C. King, Y. C. Cheng, P. K. Ko, and C. Hu, "Hot-Carrier Effects in Thin-Film Fully Depleted SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 15, No. 6, pp. 218-220, June 1994.

[85] G. Reichert, T. Ouisse, J. L. Pelloie, and S. Cristoloveanu, "Surface Mobility of SOI MOSFET's in the High Temperature Range: Modeling and Experiment," *SOI Cong. Dig.*, pp.42-43, 1995.

[86] G. Groeseneken, J.-P. Colinge, H. E. Maes, J. C. Alderman, and S. Holt, "Temperature Dependence of Threshold Voltage in Thin-Film SOI MOSFET's," *IEEE Elec. Dev. Let.*, Vol. 11, No. 8, pp.329-331, Aug. 1990.

[87] D.-S. Jeon and D. E. Burk, "A Temperature-Dependent SOI MOSFET Model for High-Temperature Application (27C-300C)," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 9, pp. 2101-2111, Sept. 1991.

[88] J. Jomaah, F. Balestra, and G. Ghibaudo, "Self-Heating Effects in SOI MOSFET's Operated at Low Temperature," *SOI Conf. Dig.*, pp.82-83, 1993.

[89] J. Jomaah, G. Ghibaudo, F. Balestra, and J. L. Pelloie, "Impact of Self-Heating Effects on the Design of SOI Devices Versus Temperature," *SOI Conf. Dig.*, pp. 114-115, 1995.

[90] L. T. Su, J. E. Chung, D. A. Antoniadis, K. E. Goodson, and M. I. Flik, "Measurement and Modeling of Self-Heating in SOI NMOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 1, pp.69-75, Jan. 1994.

[91] T.-Y. Lee and R. M. Fox, "Extraction of Thermal Resistance for Fully-Depleted SOI MOSFETs," *SOI Conf. Dig.*, pp. 78-79, 1995.

[92] B. M. Tenbroek, M. S. L. Lee, W. Redman-White, R. J. T. Bunyan and M. J. Uren, "Self-Heating Effects in SOI MOSFET's and Their Measurement by Small Signal Conductance Techniques," *IEEE Trans. Elec. Dev.*, Vol. 43, No. 12, pp. 2240-2248, Dec. 1996.

[93] B. M. Tenbroek, W. Redman-White, M. S. L. Lee, R. J. T. Bunyan, M. J. Uren, and K. M. Brunson, "Characterization of Layout Dependent Thermal Coupling in SOI CMOS Current Mirrors," *IEEE Trans. Elec. Dev.*, Vol. 43, No. 12, pp. 2227-2232, Dec. 1996.

[94] B. M. Tenbroek, W. Redman-White, M. S. L. Lee, R. J. T. Bunyan and M. J. Uren, "Static and Dynamic Thermal Coupling in SOI NMOS Current Mirrors," *SOI Conf. Dig.*, pp. 26-27, 1996.

[95] B. L. Buchanan, D. A. Neamen, and W. M. Shedd, "SOS Device Radiation Effects and Hardening," *IEEE Trans. Elec. Dev.*, Vol. 25, No. 8, pp. 959-970, Aug. 1978.

[96] H.-F. Wei, J. E. Chung and N. K. Annamalai, "Buried-Oxide Charge Trapping Induced Performance Degradation in Fully-Depleted Ultra-Thin SOI p-MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 43, No. 8, pp. 1200-1205, Aug. 1996.

[97] T. Ouisse, S. Cristoloveanu, and G. Borel, "Investigation of Series Resistances, Interface Coupling and Irradiation Effects on the Transconductance of Fully-Depleted SOI-MOSFET's," *SOI Conf. Dig.*, pp. 50-51, 1991.

[98] E. Y. Chao, C. Hu, S. Wu, G. P. Li, P. Liu, J. White, and R. Kjar, "Annealing Characteristics of Radiation Induced Leakage in SOS MOSFETs," *SOI Conf. Dig.*, pp. 84-85, 1993.

[99] L. W. Massengill, D. V. Kerns, S. E. Kerns, and M. L. Alles, "Single-Event Charge Enhancement in SOI Devices," *IEEE Elec. Dev. Let.*, Vol. 11, No. 2, pp. 98-99, Feb. 1990.

[100] H. Iwata and T. Ohzone, "Numerical Analysis of Alpha-Particle-Induced Soft Errors in SOI MOS Devices," *IEEE Trans. Elec. Dev.*, Vol. 39, No. 5, pp.1184-1190, May 1992.

[101] F. Faccio, P. Aspell, P. Jarron and E. H. Heijne, "An Additional Contribution in the Noise Spectrum of SOI MOSFETs," *SOI Conf. Dig.*, pp. 9-10, 1996.

[102] J. Chen, P. Fang, P.-K. Ko, C. Hu, R. Solomon, T.-Y. Chan, and C. G. Sodini, "Noise Overshoot at Drain Current Kink in SOI MOSFET," *SOI Conf. Dig.*, pp. 40-41, 1990.

[103] E. Simoen, U. Magnusson, A. L. P. Rotondaro and C. Claeys, "The Kink-Related Excess Low-Frequency Noise in Silicon-on-Insulator MOST's," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 3, pp. 330-339, March 1994.

[104] E. Simoen, U. Magnusson, and C. Claeys, "A Low-Frequency Noise Study of Gate-All-Around SOI Transistors," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 11, pp. 2054-2059, Nov. 1993.

Problems

1. Consider an accumulation-mode SOI PMOS device with an N^+ poly-gate, a channel length of 0.5μm, a channel width of 10μm, a front gate oxide of 120Å, a buried oxide of 3500Å, and a silicon thin-film of 800Å doped with a p-type density of $5 \times 10^{16}\text{cm}^{-3}$. Other parameters are the same as listed in Sec. 5.1 and Table 5.1.

   (a) Compute the threshold voltages of the device if it is biased at $V_{DS} = -0.1V$ and $V_{DS} = -2V$.

   (b) Compute V_{Dsat1}, V_{Dsat2}, V_{Dsat3}.

   (c) When the device is biased at $V_{GS} = -1V$ and $V_{DS} = -2.5V$, based on Sec. 5.1, in which case the device operates? What is I_{DS}?

   (d) If the device is biased at $V_{GS} = -2.5V$ and $V_{DS} = -1V$, repeat (c).

2. Consider an accumulation-mode SOI PMOS device with an N^+ poly-gate, a channel length of 10μm, a channel width of 10μm, a front gate oxide of 120Å, a buried oxide of 4000Å, a silicon thin-film of 1000Å with a p-type density of $3 \times 10^{16}\text{cm}^{-3}$, and a p-type substrate doped with a density of $10^{15}cm^{-3}$, biased at $V_{DS} = -0.01V$.

(a) If the device is biased at $V_{G2} = 2.5V$ and $-2.5V$, what is the threshold voltage?

(b) At $V_{G2} = 2.5V$ and -2.5V, compute C_{GS} and plot C_{GS} versus V_{G1}.

(c) Analyze the C_{GS} versus V_{G1} plot to find out at what V_{G2} the two-step phenomenon is the most noticeable. At what V_{G2}, this two-step phenomenon disappears.

(d) Compute the maximum value of the fringing capacitance.

(e) If the channel length of the device is shrunk to 0.5μm, repeat (b). Compare the difference between considering the fringing effect and without.

3. Consider an inversion-mode SOI NMOS device with an N^+ poly-gate, a channel length of 5μm, a channel length of 10μm, a front gate oxide of 150Å, a buried oxide of 4000Å, a silicon thin-film of 1000Å doped with a p-type density of $5 \times 10^{16}\text{cm}^{-3}$, and a p-type substrate doped with a density of 10^{15}cm^{-3}. Mobility is $500\text{cm}^2/\text{Vsec}$. Based on Sec. 5.2 and Sec. 5.3,

   (a) Plot C_{DG} and C_{GD} versus V_{GS} if the device is biased at $V_{DS} = 0.1V$ and 1V.

   (b) Consider the circuit as shown in Fig.5.13. If the load capacitance is $C_L = 0.1pF$, V_{GS} switches from 0V to 3.3V in 0.1ns, compute the transient waveform at V_{out}. The initial value of the output is 3.3V.

   (c) If the channel length is shrunk to 0.5μm, considering velocity saturation ($v_{sat} = 10^7 cm/sec$), channel length modulation, and the fringing effect, repeat (a) and (b).

4. Considering a fully-depleted inversion-mode SOI NMOS device with an N^+ poly-gate, a channel length and a channel width of $10\mu\text{m}/10\mu\text{m}$, a front gate oxide of 80Å, a buried oxide of 4000Å, a p-type silicon thin-film, and a p-type substrate doped with a density of 10^{15}cm^{-3}. $V_{DS} = V_{BS} = 0V$.

   (a) If the silicon thin-film doping density is $5 \times 10^{16}\text{cm}^{-3}$ and $2 \times 10^{16} cm^{-3}$, compute $\frac{dV_{TH}}{dt_{si}}$ versus t_{si} (silicon thin-film thickness) when the silicon thin-film is fully-depleted.

   (b) If the dopant of the silicon thin-film is switched to n-type, the device becomes accumulation-mode. Repeat (a).

   (c) If the back gate is biased at -5V and the buried oxide is 2000Å, repeat (a) and (b).

(d) Consider a double-gate SOI NMOS device with a top gate oxide of 100Å and a bottom gate oxide of 200Å. Repeat (a) and (b).

(e) Analyze the sensitivity under all situations in (a)-(d).

5. Consider an SOI NMOS device with an N^+ poly-gate, a channel length of 2μm, a channel width of 10μm, a front gate oxide of 200Å, a buried oxide of 1μm, and a silicon thin-film thickness of 5000Å doped with a p-type density of $8 \times 10^{16}\text{cm}^{-3}$. Other parameters are as listed in Sec. 5.6.

(a) Before the onset of the kink effect, what is the threshold voltage?

(b) At $V_{GS} = 1.5V$ and 3V, compute V_{DS} at the onset of the kink effect.

(c) As in (b), at $V_{DS} = 6V$, compute the corresponding threshold voltages.

(d) If the silicon thin-film doping density is changed to $10^{17}cm^{-3}$ and $5\times10^{16}\text{cm}^{-3}$, repeat (a)-(c).

(e) If the device is stressed to generate a large amount of interface traps such that all the related lifetimes become 0.1x, repeat (a)-(d).

6. Consider an inversion-mode SOI NMOS device with an N^+ poly-gate, a channel length and a channel width of 10μm, a front gate oxide of 250Å, a buried oxide of 1μm, and a silicon thin-film thickness of 5000Å doped with a p-type density of $5 \times 10^{16}\text{cm}^{-3}$. If the device is biased at $V_{DS} = 0.1V$ and V_{GS} switches from 0V (turn-off) to 3V (turn-on) suddenly,

(a) What is the change in the electrostatic potential at the front oxide/silicon thin-film interface?

(b) If at the turn-on the device, holes can not be evacuated in time, the electrostatic potential in the silicon thin-film stays unchanged. At this moment, the potential difference between the body and the source is identical to the result in (a). Compute the effective threshold voltage at this moment.

(c) From (b), compute I_{DS} at the sudden turn-on with the floating body and with the body grounded.

(d) If the silicon thin-film doping density becomes $10^{17}cm^{-3}$ and $2 \times 10^{16}cm^{-3}$, repeat (a)-(c).

7. Consider two inversion-mode SOI NMOS devices with an N^+ poly-gate, a channel length and a channel width of 10μm, a front gate oxide of 150Å, a buried oxide of 3500Å, and a grounded substrate doped with a p-type density of $5 \times 10^{16}\text{cm}^{-3}$. The silicon thin-film thicknesses are 800Å and 5000Å. Consider the influence of the temperature-dependent intrinsic carrier concentration (n_i) and energy bandgap (E_g).

   (a) At room temperature, what is the thickness of silicon thin-film such that fully-depleted condition can be reached?

   (b) At 300C, repeat (a).

   (c) Compute the threshold voltages of these two devices from room temperature to 300C.

   (d) If the silicon thin-film doping density becomes $2 \times 10^{16}\text{cm}^{-3}$ and $10^{17}cm^{-3}$, repeat (a)-(c).

   (e) For accumulation-mode SOI NMOS devices with a n-type silicon thin-film doping density of $2 \times 10^{16}cm^{-3}$, repeat (a) and (b). If the silicon thin-film thickness is 800Å, repeat (c).

   (f) Consider a double-gate device with a front gate oxide of 100Å, a back gate oxide of 200Å, a silicon thin-film of 800Å doped with a p-type density of $5 \times 10^{16}cm^{-3}$. Repeat (a)-(d).

   (g) Compute the sensitivity of the threshold voltage with respect to temperature for the above cases.

Chapter 6

SOI-Technology ST-SPICE

As described in the previous chapters, SOI CMOS technology has been regarded as another major VLSI technology in addition to bulk CMOS technology. VLSI circuits using SOI CMOS technology have been reported increasingly. Since the performance of SOI CMOS devices is quite different from that of the bulk ones, SOI VLSI circuits have demonstrated unique phenomena as described in Chapter 3. When designing SOI VLSI circuits, the SPICE CAD program designed for bulk CMOS devices may not be sufficient for circuit simulation. In this chapter, by including the analytical device models of deep-submicron fully-depleted SOI CMOS devices described in the last two chapters, SOI-Technology— ST-SPICE [1] suitable for CAD of SOI CMOS VLSI circuits is described. Starting from the basic concepts of the SPICE program, analytical device models of deep-submicron fully-depleted SOI CMOS devices used in ST-SPICE for CAD of VLSI circuits are explained. In the final portion of this section, usage of the ST-SPICE CAD program for analyzing the steady state and transient behaviors of SOI CMOS circuits is presented.

6.1 Overview

SOI technology has been becoming an important technology for deep-submicron CMOS VLSI[1][2]. Using deep-submicron SOI technology, various VLSI circuits including DRAM, SRAM, logic circuits and gate arrays have been integrated [3]-[8]. As compared to the bulk CMOS circuits, SOI CMOS circuits have a better speed performance owing to smaller parasitic capacitances. As a result, higher-speed low-power applications can be obtained. The behaviors of deep-submicron SOI CMOS devices are quite different from those of bulk ones. In advanced deep-submicron

[1]ST-SPICE fully-depleted SOI CMOS device models are available at http://www.ee.ntu.edu.tw/www/faculty/jb-kuo/jb-kuo.htm

J. B. Kuo et al., *CMOS VLSI Engineering*

CMOS technologies [9]-[11] especially for integrating memory circuits [3]-[5][12], narrow-channel and short-channel effects [13]-[16] are important in determining the device performance [17][18]. In addition, sidewall conduction of narrow-channel SOI CMOS devices can not be neglected [19][20]. Furthermore, when channel length is very small, electron temperature effect is also important [21][22]. Therefore, related current and capacitance models should be adjusted to include these effects accordingly [23]. On the other hand, at a large drain voltage, the non-local impact ionization [24] and parasitic BJT effect [25] need to be considered. For SOI CMOS devices, heat dissipation capability is not good. Therefore, thermal effect can not be overlooked[26][27]. Under this situation, conventional SPICE programs [28], which are designed for bulk CMOS circuits, may not be applicable for simulation of deep-submicron SOI CMOS circuits. A SPICE program including these SOI device models suitable for simulation of SOI CMOS circuits is useful. In this chapter, analytical device models of deep-submicron fully-depleted SOI CMOS devices used in ST-SPICE for CAD of VLSI circuits are described. It will be shown that as verified by 3D device simulation and experimental results, inclusion of these models in the ST-SPICE program is important in providing a good prediction of DC and transient behaviors of fully-depleted mesa-isolated SOI CMOS circuits. In the following sections, description of the fundamentals of the SPICE program is introduced first. Then SOI CMOS models used in the ST-SPICE program are presented, followed by the usage and verification of the ST-SPICE program containing the SOI CMOS device models.

6.2 BSIM Models

Circuit simulation, which can be used to evaluate the performance of the proposed circuits before the IC is fabricated, is an indispensable tool for engineering VLSI circuits. SPICE circuit simulation is an important CAD tool for designing circuits. The contributions of SPICE to the progress of the ICs are well recognized.

In the SPICE program, the accuracy of the CMOS device models is critical for determining the precision of the results. SPICE CMOS device models have been continuously improved in the past. The SPICE MOS model was improved from Level 1 in 1970, to Level 2 & 3 in 1980s. In late 1980s, BSIM model was announced[28]. Level 1 model, which is also called Shichman-Hodges model, is suitable for MOS device with a channel length of greater than $2\mu m$. Level 2 model, which is suitable for MOS devices with a channel length of smaller than 2μm, already includes the second-order effects including the lateral and vertical electric field dependent mobility model. Level 3, which is a semi-empirical model, has a better mobility

model. Following these models are the second-generation models BSIM and BSIM2. The BSIM models are suitable for bulk CMOS devices with a channel length of less than 1μm. The BSIM models emphasize the influence of the process variations in the device models. Hot electron effects have also been considered. These models are arranged for efficient circuit simulation. However, these models are based on a semi-empirical approach. Sometimes, complicated polynomial equations are required. Therefore, sometimes physical meanings cannot be perceived. BSIM3 is the third-generation SPICE model. In BSIM3, models are with physical meanings such that a perceivable relationship between the model parameters and the actual device structures can be maintained. BSIM3 has also been evolved continuously for smooth model equations. In the future deep-submicron CMOS devices, there is an increasing need to have a more complete set of CMOS device models to be used for CAD of ULSI circuit design. In addition, for simulation of the ULSI circuits such as 16Gbit DRAM, due to a large number of transistors involved, during the transient analysis, to make the iterations converged is a challenging task. For the future deep-submicron CMOS devices used for ULSI circuits, the SPICE CMOS device models need to be compact and accurate—physical models with physical meanings are important.

Until now, the BSIM3 models developed for bulk CMOS devices cannot be used sufficiently for SOI. Due to the different device structures, most of the BSIM3 models are not applicable. For example, the back-gate bias effect on the threshold voltage is different from that for bulk ones. Small-geometry effects on the threshold voltage for SOI CMOS devices need to be reconstructed. Electron-temperature dependent mobility models are also required for deep-submicron SOI CMOS devices. Due to the mesa-isolated silicon thin-film structure above the buried oxide, the subthreshold current hump model needs to be included. In addition, the capacitance model is also different for the SOI CMOS devices. Specifically, the extrinsic parasitic capacitances due to the depletion regions between the source/drain and the substrate areas disappear. Instead, the parasitic capacitances are mostly due to the fringing electric field. In addition, owing to the electron temperature effect, the BSIM intrinsic capacitances models are not sufficient for the deep-submicron SOI CMOS devices.

In this chapter, physical models used in the ST-SPICE program for deep-submicron fully-depleted mesa-isolated SOI CMOS devices are described. Fig. 6.1 shows the flow chart of the SPICE program, which processes the input file containing the physical model parameters of the SOI CMOS devices, the circuit structure and the intended simulation objectives, to produce the output simulation results. From the input file, in the SPICE program, the input processing step is initiated. After the

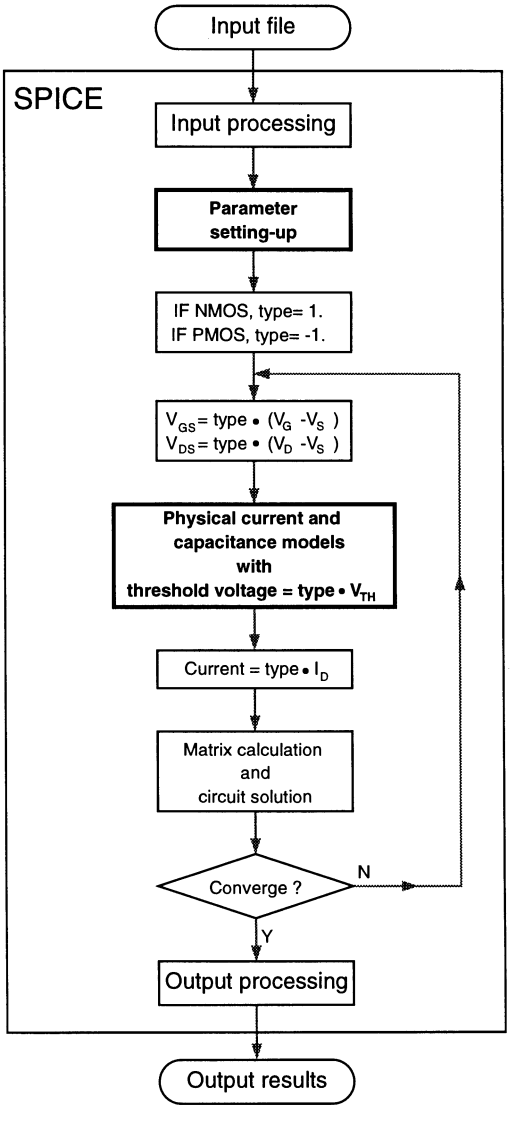


Figure 6.1: Flow chart of the SPICE program.

input processing step, parameters are set up in the parameter setting-up step. Then, identical physical models are used for the NMOS and PMOS devices by identifying the type. For NMOS, type is 1. For PMOS devices, type is -1. Then the gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}) for the NMOS and PMOS devices are individually defined. Using the SOI physical current and capacitance models with the threshold voltages for the NMOS and the PMOS devices, the drain currents are computed. Then, the modified nodal admittance matrix of the circuit is defined by writing the node equations at all nodes of the circuit based on the structure of the circuit using the physical models.

For transient analysis, at time t_0 the voltage at each node of the equivalent circuit is known: V_{x1}^0. If the input applied signal is known, the transient waveform of each node is to be computed. During the transient analysis, it's based on time increment method— from a time with all node voltages already known to compute the node voltages at the next time step. From the formula: $\int_{t_0}^{t_1} idt = Q(t_1) - Q_(t_0)$, all related equations can be built in an array:

$$\frac{h}{2}(i_{y1}^1 + i_{y0}) = (Q_{y1} - Q_{y0}) + \Sigma_x(\frac{dQ_y}{dV_x})|_{x1}^0(V_{x1}^1 - V_{x1}^0), \tag{6.1}$$

where $dQ_y/dV_x = C_{yx}$ is the capacitance of the related SOI MOS device, V_{x1}^0 is the estimated voltage value of the previous iteration at node x_1, V_{x1}^1 is the estimated voltage value of the current iteration at node x_1, h is the time step ($h = t_1 - t_0$), i_{y0} is the estimated current of the previous iteration, and i_{y0}^1 is the current to be estimated in this current iteration. After building all node equations, a node voltage vector can be obtained. Then based on the numerical implicit integration algorithm, iterations have been used to compute the node voltage vector. If the result of the current iteration has a change much smaller than the result of the previous iteration, the convergence of the computation has been reached— the voltage at each node has been successfully obtained at a time step. Then the iteration process for computing the node voltage for the next time step can be initiated. If the time step is too large, as compared to the change in the input waveform, the iterations of node equations cannot reach a convergence. Then a cutback in the next time step is required.

In the following sections, the physical deep-submicron fully-depleted mesa-isolated SOI CMOS device models including the back-gate-bias-dependent, small-geometry-effect threshold voltage model, the subthreshold current hump model, the electron temperature dependent mobility model, the strong-inversion current models, the electron-temperature dependent capacitance model, the non-local impact ionization and parasitic BJT effect model, and the thermal effect model, are described. Due to

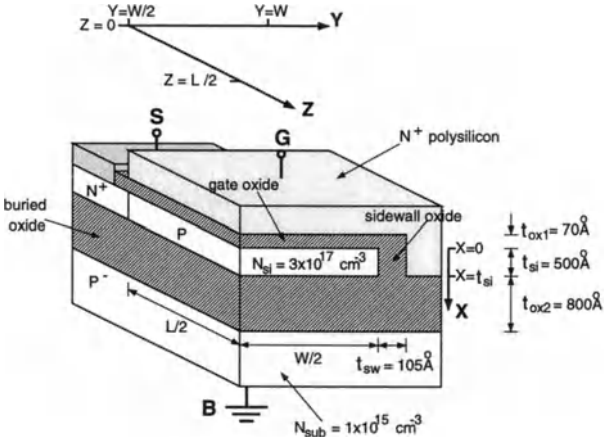


Figure 6.2: 3D cross section of of a fully-depleted mesa-isolated SOI CMOS device under study.

similarities of the NMOS and the PMOS devices, only the NMOS device models are described here. The models for the PMOS devices can be obtained systematically.

6.3 Threshold Voltage Model

For a small-geometry mesa-isolated fully-depleted SOI MOS device as shown in Fig. 6.2, considering the short-channel and narrow-channel effects, its threshold voltage of the center-channel region used in the ST-SPICE can be obtained by solving 3D Poisson's equation as [17]:

$$V_{TH,c} = V_{FB} + \phi_G - \phi_{si}, \tag{6.2}$$

$$\phi_G = \frac{-\phi_{si}(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}) - \phi_{s3}\frac{C_{si}}{C_{ox1}}(1-\delta_2) - \frac{E_g}{2q}\frac{C_{si}}{C_{ox1}}\cdot\delta_3 + \frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}}\frac{C_{si}}{C_{ox1}}(1+2\frac{C_{si}}{C_{ox2}})(1-\delta_1)}{1+\frac{C_{si}}{C_{ox1}}(\delta_2-\delta_3)+\frac{C_{si}}{C_{ox2}}},$$

$$\delta_1 = \frac{\alpha(1-\beta')}{1-\alpha'\beta'} + \frac{\beta(1-\alpha')}{1-\alpha'\beta'}, \quad \delta_2 = \frac{1}{4}\frac{{t_{si}}^2}{{l_0}^2}\frac{(1+2\frac{C_{si}}{C_{ox1}})(1+2\frac{C_{si}}{C_{ox2}})}{(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})}\cdot\delta_1,$$

$$\delta_3 = \frac{1}{2}\frac{{t_{si}}^2}{{l_0}^2}(1+2\frac{C_{si}}{C_{ox2}})\cdot\frac{\beta(1-\alpha')}{1-\alpha'\beta'},$$

$$\alpha = [cosh(W/2l_0) + \frac{t_{si}}{l_0}\frac{C_{si}}{C_{sw}}sinh(W/2l_0)]^{-1}, \quad \alpha' = (1-\alpha)\cdot\frac{8{l_0}^2}{W^2} - \alpha\cdot\frac{4t_{si}}{W}\frac{C_{si}}{C_{sw}},$$

$$\beta = \frac{1}{cosh(L/2l_0)}, \quad \beta' = (1-\beta)\cdot\frac{8{l_0}^2}{L^2}, \quad l_0 = t_{si}\sqrt{\frac{\frac{1}{4}+\frac{3}{4}\frac{C_{si}}{C_{ox1}}+\frac{3}{4}\frac{C_{si}}{C_{ox2}}+2\frac{C_{si}}{C_{ox1}}\frac{C_{si}}{C_{ox2}}}{2(1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}})}},$$

where V_{FB} is the flat-band voltage of the front gate, ϕ_G is the electrostatic potential at the front gate, ϕ_{s3} is the electrostatic potential at the buried oxide/substrate interface, E_g is the silicon energy bandgap, L is the channel length, W is the channel width, N_{si} is the silicon thin-film doping density, $\phi_{si} = \frac{kT}{q}ln\frac{n_i}{N_{si}}$, and n_i is the intrinsic carrier density. $C_{si} = \frac{\epsilon_{si}}{t_{si}}$. $C_{ox1} = \frac{\epsilon_{ox}}{t_{ox1}}$. $C_{ox2} = \frac{\epsilon_{ox}}{t_{ox2}}$. $C_{sw} = \frac{\epsilon_{ox}}{t_{sw}}$. t_{si}, t_{ox1}, t_{ox2}, t_{sw} are the thicknesses of the silicon thin-film, front oxide, buried oxide, and sidewall oxide, respectively. Considering the depletion region in the substrate, the electrostatic potential (ϕ_{s3}) and the electric field (E_0) at the buried oxide/substrate interface are [29]:

$$\begin{aligned} \phi_{s3} &= \phi_{sub} + V_{BS} + \frac{\epsilon_{si}}{2qN_{sub}}{E_0}^2, \qquad (6.3)\\ E_0 &= -\frac{qN_{sub}t_{si}}{\epsilon_{si}}(1+\frac{C_{si}}{C_{ox2}}) + \\ &\quad \sqrt{[\frac{qN_{sub}t_{si}}{\epsilon_{si}}(1+\frac{C_{si}}{C_{ox2}})]^2 - \frac{2qN_{sub}}{\epsilon_{si}}(\phi_{si}+\phi_{sub}+V_{BS}) - (\frac{qt_{si}}{\epsilon_{si}})^2 N_{si}N_{sub}}, \end{aligned}$$

respectively, where V_{BS} is the substrate-source voltage, N_{sub} is the substrate doping density, and $\phi_{sub} = \frac{kT}{q}ln\frac{n_i}{N_{sub}}$. For a small-geometry mesa-isolated SOI CMOS device, in addition to the center channel under the poly-gate, near the sidewall region, there is a parasitic transistor for current conduction [19][20]. Therefore, the threshold voltage of the sidewall parasitic transistor is also important. From Ref. [17], solving 3D Poisson's equation, the threshold voltage of the sidewall parasitic transistor is:

$$\begin{aligned} V_{TH,s} &= V_{FB} + \phi_G - \phi_{si}, \qquad (6.4)\\ \phi_G &= \frac{-\phi_{si} + \delta_{1,s}\cdot\frac{qN_{si}{l_0}^2}{\epsilon_{si}} - \delta_{2,s}\cdot\phi_{s3} + \delta_{3,s}\cdot\frac{E_g}{2q}}{1-\delta_{2,s}+\delta_{3,s}},\\ \delta_{1,s} &= 1-\alpha_s + \frac{\alpha_s'\beta}{1-\alpha'\beta'} - \frac{\alpha_s'\alpha\beta'}{1-\alpha'\beta'},\\ \delta_{2,s} &= \frac{1}{2}\frac{1+2\frac{C_{si}}{C_{ox1}}}{1+\frac{C_{si}}{C_{ox1}}+\frac{C_{si}}{C_{ox2}}}\cdot\delta_{1,s}, \quad \delta_{3,s} = \frac{\alpha_s'\beta}{1-\alpha'\beta'},\\ \alpha_s &= \alpha\cdot cosh(W/2l_0), \quad \alpha_s' = (1-\alpha_s)\cdot\frac{8{l_0}^2}{W^2} - \alpha_s\cdot\frac{4t_{si}}{W}\frac{C_{si}}{C_{sw}}. \end{aligned}$$

Fig. 6.3(a) shows the back gate bias effect: threshold voltage versus V_{BS} of the

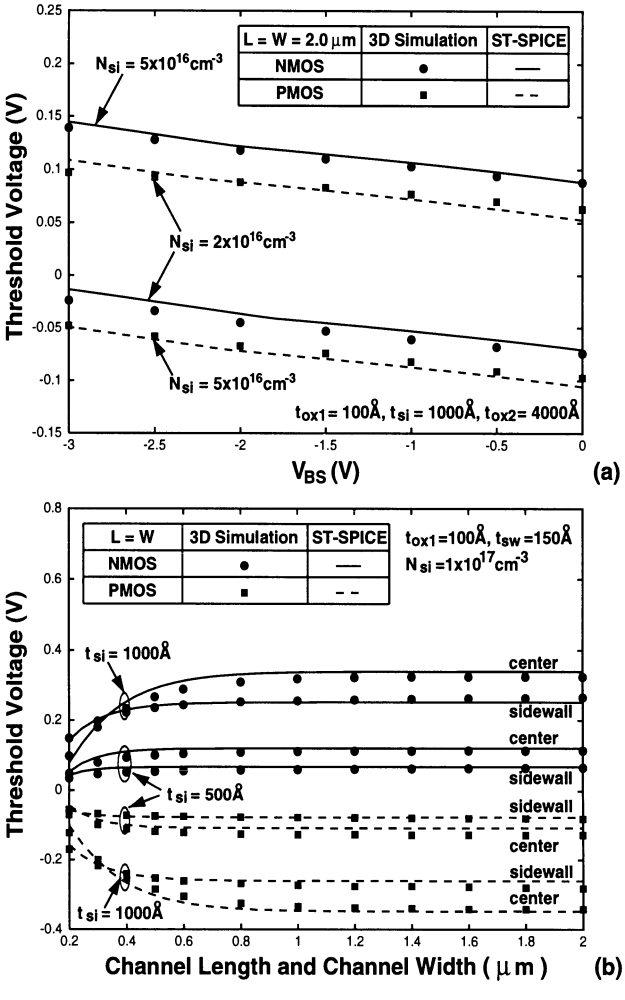


Figure 6.3: (a) Back gate bias effect: threshold voltage versus V_{BS} of the SOI CMOS devices with a gate oxide of t_{ox1} = 100Å, a 1000Å silicon thin-film doped with densities of (p-type for NMOS, n-type for PMOS) $2 \times 10^{16}\text{cm}^{-3}$ and $5 \times 10^{16}\text{cm}^{-3}$, a buried oxide of t_{ox2} = 4000Å, and channel length and width of 2μm, based on the ST-SPICE models and 3D simulation results. (b) Short channel and narrow channel effects: threshold voltage in the center and the sidewall channel regions versus channel length and channel width of the SOI CMOS devices with a gate oxide of t_{ox1} = 100Å, a sidewall oxide of 150Å, a silicon thin-film of 500Å and 1000Å doped with a density of (p-type for NMOS, n-type for PMOS) $1 \times 10^{17}\text{cm}^{-3}$, and a buried oxide of t_{ox2} = 4000Å, based on the ST-SPICE models and 3D simulation results.

SOI CMOS devices with a gate oxide of t_{ox1} = 100Å, a 1000Å silicon thin-film doped with densities of (p-type for NMOS, n-type for PMOS) $2 \times 10^{16}\text{cm}^{-3}$ and $5 \times 10^{16}\text{cm}^{-3}$, a buried oxide of t_{ox2} = 4000Å, and channel length and width of 2μm, based on the ST-SPICE models and 3D simulation results. As shown in the figure, at a more negative V_{BS}, the threshold voltages of both NMOS and PMOS devices are shifted toward the positive direction. Compared to the bulk CMOS devices, the body effect of SOI CMOS devices is much smaller. In addition, the influence of the silicon thin-film doping density in the body effect is small. Fig. 6.3(b) shows the short channel and narrow channel effects: threshold voltage in the center and the sidewall channel regions versus channel length and channel width of the SOI CMOS devices with a gate oxide of t_{ox1} = 100Å, a sidewall oxide of 150Å, a silicon thin-film of 500Å and 1000Å doped with a density of (p-type for NMOS, n-type for PMOS) $1 \times 10^{17}\text{cm}^{-3}$, and a buried oxide of t_{ox2} = 4000Å, based on the ST-SPICE models and 3D simulation results. As shown in the figure, when the size of the device is small, the magnitudes of the NMOS and PMOS threshold voltages decrease. When the silicon thin-film becomes thinner, the small-geometry effect becomes smaller. In addition, the trends on the small-geometry effect of the center and the sidewall channel regions are similar except that the magnitude of the threshold voltage of the sidewall channel region is smaller than that of the center channel region. Therefore, the sidewall channel region turns on earlier than the center channel region. In addition, the small-geometry effect of the sidewall channel region is smaller than that of the center channel region. As shown in Figs. 6.3(a)& (b), the threshold voltage model used in the ST-SPICE can well predict the body effect and the small geometry effect.

6.4 Subthreshold Current Model

When the gate-source voltage (V_{GS}) is smaller than the threshold voltage— the subthreshold region, diffusion current dominates in the device. Therefore, the diffusion current of the center channel used in the ST-SPICE is [30]-[32]:

$$\begin{aligned} I_{diff,c} &= I_1 \cdot \frac{W}{L} \cdot (1 - exp(-\frac{V'_{DS}}{kT/q})) \cdot \frac{exp(\frac{V'_{GS}-V_{TH,c}}{n_c \cdot kT/q})}{1 + exp(\frac{V'_{GS}-V_{TH,c}}{n_c \cdot KT/q})}, \\ V'_{DS} &= V_{DS} - I_D \cdot (R_S + R_D) - V_J, \quad V'_{GS} = V_{GS} - I_D \cdot R_S, \end{aligned} \tag{6.5}$$

where I_1 is a scaling coefficient, I_D is the total drain current, R_S and R_D are the parasitic resistances of the source and the drain, respectively. V_J is the slight potential barrier between the source/drain and the channel. $n_c = (\frac{\partial \phi(0, \frac{W}{2}, \frac{L}{2})}{\partial V_{GS}})^{-1}$, where

$\phi(0, \frac{W}{2}, \frac{L}{2})$ is the electrostatic potential at the center surface of the silicon thin-film. From Ref. [17], one obtains:

$$\begin{aligned} n_c &= \frac{1 + \frac{C_{si}}{C_{ox1}} + \frac{C_{si}}{C_{ox2}}}{1 + \frac{C_{si}}{C_{ox1}} \cdot (\delta_2 - \delta_3) + \frac{C_{si}}{C_{ox2}} + \frac{d\phi_{s3}}{dV_{GS}} \cdot \frac{C_{si}}{C_{ox1}} \cdot (1 - \delta_2)}, \\ \frac{d\phi_{s3}}{dV_{GS}} &= \frac{\frac{1}{C_d}}{\frac{1}{C_{ox1}} + \frac{1}{C_{ox2}} + \frac{1}{C_{si}} + \frac{1}{C_d}}, \quad C_d = \frac{\epsilon_{si}}{t_d}, \quad t_d = \frac{E_0 \epsilon_{si}}{qN_{sub}}, \end{aligned} \tag{6.6}$$

where t_d is the depletion width in the substrate [29]. Similarly, the diffusion current of the sidewal channel is:

$$\begin{aligned} I_{diff,s} &= I_2 \cdot \frac{1}{L} \cdot (1 - exp(-\frac{V'_{DS}}{kT/q})) \cdot \frac{exp(\frac{V'_{GS} - V_{TH,s}}{n_s \cdot kT/q})}{1 + exp(\frac{V'_{GS} - V_{TH,s}}{n_s \cdot KT/q})}, \\ n_s &= \frac{1}{1 - \delta_{2,s} + \delta_{3,s} + \delta_{2,s} \cdot \frac{d\phi_{s3}}{dV_{GS}}}, \end{aligned} \tag{6.7}$$

where I_2 is a scaling coefficient.

6.5 Mobility and Strong-Inversion Current Model

In this subsection, the mobility and the strong-inversion current models of an SOI CMOS device used in the ST-SPICE in terms of the triode and the saturation regions are described.

6.5.1 Triode Region

When the channel of a fully-depleted mesa-isolated SOI CMOS device is very short, the electron temperature effect can not be neglected [21][22]. An electron-temperature-dependent mobility model, which is referred to the difference between the electron temperature and the lattice temperature, is [23]:

$$\begin{aligned} \mu_n &= \frac{\mu_s(T_L)}{1 + \alpha \frac{k}{q}(T_n - T_L)}, \\ \alpha &= \frac{3\mu_s(T_L)}{2v_{sat}^2 \tau_\epsilon}, \end{aligned} \tag{6.8}$$

where T_L is the lattice temperature, $\mu_s(T_L)$ is the electron surface mobility considering lattice temperature, q is the electron charge, v_{sat} is the saturated velocity, τ_ϵ is

the energy relaxation time, and k is Boltzmann constant. Considering energy balance equation and the electron-temperature-dependent mobility model, the effective mobility of the center channel region is:

$$\begin{aligned}
\mu_{eff,c}(V'_{DS}) &= \frac{4\mu_{s,c}}{3+\sqrt{1+p\cdot {V'_{DS}}^2\cdot \mu_{s,c}^2}}, \\
\mu_{s,c} &= \frac{\mu_0(T_L)}{1+\theta(V'_{GS}-V_{TH,c})}, \quad \mu_0(T_L)=\mu_0(T_0)\cdot\frac{T_0^2}{T_L^2}, \\
p &= \frac{4(2-\eta_1)^2}{L^2 v_{sat}^2}-\frac{40}{3}\frac{(1-\eta_1)(2-\eta_1)\tau_\epsilon}{v_{sat}L^3},
\end{aligned} \tag{6.9}$$

where $\mu_{s,c}$ is the surface mobility in the center channel, μ_0 is the low-field mobility, T_0 is the ambient temperature, θ is used to describe the influence of the vertical electric field in the mobility, and η_1 is a fitting parameter related to the electric field distribution in the device. The drift current in the center channel of the SOI CMOS device biased in the triode region is:

$$\begin{aligned}
I_{drift,c} &= \mu_{eff,c}(V'_{DS})\cdot C_{ox1}\frac{W}{L}\cdot[(V'_{GS}-V_{TH,c})V'_{DS}-\frac{1}{2}a_{0,c}{V'_{DS}}^2], \\
a_{0,c} &= 1+\frac{C_{si}C'_{ox2}}{C_{ox1}(C_{si}+C'_{ox2})}, \quad C'_{ox2}=\frac{C_{ox2}C_d}{C_{ox2}+C_d},
\end{aligned} \tag{6.10}$$

where $a_{0,c}$ is related to the body effect of the device. Similarly, the drift current in the sidewall channel of the device biased in the triode region is:

$$\begin{aligned}
I_{drift,s} &= \mu_{eff,s}(V'_{DS})\cdot 2\cdot(C_e+C_{sw}\cdot t_{si})\frac{1}{L}\cdot[(V'_{GS}-V_{TH,s})V'_{DS}-\frac{1}{2}{V'_{DS}}^2], \\
\mu_{eff,s}(V'_{DS}) &= \frac{4\mu_{s,s}}{3+\sqrt{1+p\cdot {V'_{DS}}^2\cdot\mu_{s,s}^2}}, \quad \mu_{s,s}=\frac{\mu_0(T_L)}{1+\theta(V'_{GS}-V_{TH,s})},
\end{aligned} \tag{6.11}$$

where C_e is the parasitic capacitance at the corner of the sidewall.

6.5.2 Saturation Region

When the voltage drop over the channel of the device (V'_{DS}) is greater than a certain extent, the center channel starts to operate in the saturation region. At this time, $V'_{DS}=V_{Dsat,c}$:

$$\begin{aligned}
V_{Dsat,c} &= V_{Dsat1,c}+V_{p,c}-\sqrt{V_{Dsat1,c}^2+V_{p,c}^2}, \\
V_{Dsat1,c} &= \frac{\eta_2 v_{sat}L^2}{(2-\eta_1)(1-\eta_2^2)\mu_{s,c}L+\frac{10}{3}(1-\eta_1)\eta_2^2\mu_{s,c}\tau_\epsilon v_{sat}},
\end{aligned} \tag{6.12}$$

$$
\begin{aligned}
V_{p,c} &= \frac{-a_{0,c}Q_c + \sqrt{a_{0,c}^2 Q_c^2 + a_{0,c}R_c Q_c(\frac{V'_{GS}-V_{TH,c}}{2a_{0,c}})}}{a_{0,c}R_c}, \\
Q_c &= 3 + (1 + p \cdot (\frac{V'_{GS} - V_{TH,c}}{2a_{0,c}})^2 \cdot \mu_{s,c}^2)^{-0.5}, \\
R_c &= \frac{p \cdot (\frac{V'_{GS}-V_{TH,c}}{2a_{0,c}}) \cdot \mu_{s,c}^2}{\sqrt{1 + p \cdot (\frac{V'_{GS}-V_{TH,c}}{2a_{0,c}})^2 \cdot \mu_{s,c}^2}}.
\end{aligned}
$$

where η_2 is related to the electron velocity at the saturation point. The drift current in the center channel region of the device biased in the saturation region is:

$$
\begin{aligned}
I_{drift,c} &= \mu_{eff,c}(V_{Dsat,c}) \cdot C_{ox1}\frac{W}{L - \Delta L_c} \cdot [(V'_{GS} - V_{TH,c})V_{Dsat,c} - \frac{1}{2}a_{0,c}V_{Dsat,c}^2], \qquad (6. \\
\Delta L_c &= s \cdot \lambda_c \cdot ln[\frac{-(V'_{DS} - V_{Dsat,c} - a_c\lambda_c^2) - \sqrt{(V'_{DS} - V_{Dsat,c} - a_c\lambda_c^2)^2 + \lambda_c^2(E_{1,c}^2 - a_c^2\lambda_c^2}}{\lambda_c \cdot (E_{1,c} + a_c\lambda_c)} \\
\lambda_c &= (\frac{C_{ox1}}{t_{si}\epsilon_{si}} + \frac{C'_{ox2}}{t_{si}\epsilon_{si}})^{-0.5}, \quad a_c = -\frac{2(1-\eta_1)V_{Dsat,c}}{L^2}, \quad E_{1,c} = -\frac{(2-\eta_1)V_{Dsat,c}}{L},
\end{aligned}
$$

where s is a correction factor. ΔL_c, which is the length of the post-saturation region in the center channel region, can be obtained from 2D Gauss' Law. As for the sidewall channel, its saturation voltage can be obtained similarly as for the center channel:

$$
\begin{aligned}
V_{Dsat,s} &= V_{Dsat1,s} + V_{p,s} - \sqrt{V_{Dsat1,s}^2 + V_{p,s}^2}, \qquad (6.14) \\
V_{Dsat1,s} &= \frac{\eta_2 v_{sat} L^2}{(2-\eta_1)(1-\eta_2^2)\mu_{s,s}L + \frac{10}{3}(1-\eta_1)\eta_2^2\mu_{s,s}\tau_\epsilon v_{sat}}, \\
V_{p,s} &= \frac{-Q_s + \sqrt{Q_s^2 + 2R_sQ_s(V'_{GS} - V_{TH,s})}}{R_s}, \\
Q_s &= 3 + (1 + p \cdot (V'_{GS} - V_{TH,s})^2 \cdot \mu_{s,s}^2)^{-0.5}, \\
R_s &= \frac{p \cdot (V'_{GS} - V_{TH,s}) \cdot \mu_{s,s}^2}{\sqrt{1 + p \cdot (V'_{GS} - V_{TH,s})^2 \cdot \mu_{s,s}^2}}.
\end{aligned}
$$

When considering the length of the post-saturation region in the sidewall channel region (ΔL_s), the previous 2D Gauss' Law approach is not applicable due to the 3D effect as shown in Fig. 6.4— near the sidewall area, the 3D effect in the electron distribution can be identified. Therefore, 3D Gauss' Law should be considered. As

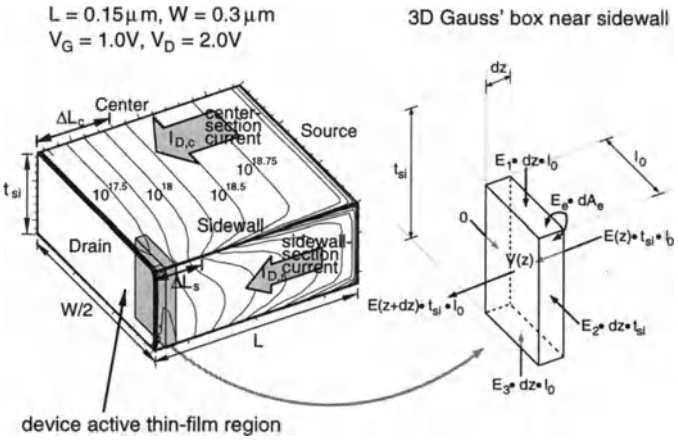


Figure 6.4: 3D Gauss' box near sidewall in the fully-depleted SOI NMOS device under study.

shown in Fig. 6.4, by considering the Gauss box in the space from z to $z+dz$ in the silicon thin-film, one obtains:

$$\begin{aligned} -E_1 \cdot dz \cdot l_0 - E_2 \cdot dz \cdot t_{si} &- E_3 \cdot dz \cdot l_0 - E_e \cdot dA_e + E(z+dz) \cdot l_0 \cdot t_{si} \\ -E(z) \cdot l_0 \cdot t_{si} &= -\frac{q(N_{si}+n)}{\epsilon_{si}} \cdot t_{si} \cdot l_0 \cdot dz, \qquad (6.15) \\ E_1 &= C_{ox1}(V'_{GS} - V(z))\frac{1}{\epsilon_{si}}, \quad E_2 = C_{sw}(V'_{GS} - V(z))\frac{1}{\epsilon_{si}}, \\ E_2 &= C'_{ox2}(V_{BS} - V(z))\frac{1}{\epsilon_{si}}, \quad E_e dA_e = C_e(V'_{GS} - V(z))\frac{1}{\epsilon_{si}}dz, \end{aligned}$$

where E_1, E_2, and E_3 represent the electric fields in the front oxide, sidewall oxide, and buried oxide, respectively. $E_e dA_e$ stands for the irregular electric field at the sidewall corner. l_0 is the sidewall characteristic length as shown in Eq.(6.2). n is the mobile carrier density. Using a similar approach in Ref. [23], Eq.(6.15) becomes:

$$\begin{aligned} \frac{d^2V(z)}{dz^2} &= \frac{1}{\lambda_s^2}(V(z) - V_{Dsat,s}) - a_s, \qquad (6.16) \\ \lambda_s &= (\frac{C_{ox1}}{\epsilon_{si}t_{si}} + \frac{C'_{ox2}}{\epsilon_{si}t_{si}} + \frac{C_{sw}}{\epsilon_{si}l_0} + \frac{C_e}{\epsilon_{si}t_{si}l_0})^{-0.5}, \\ a_s &= -\frac{2(1-\eta_1)V_{Dsat,s}}{L^2}. \end{aligned}$$

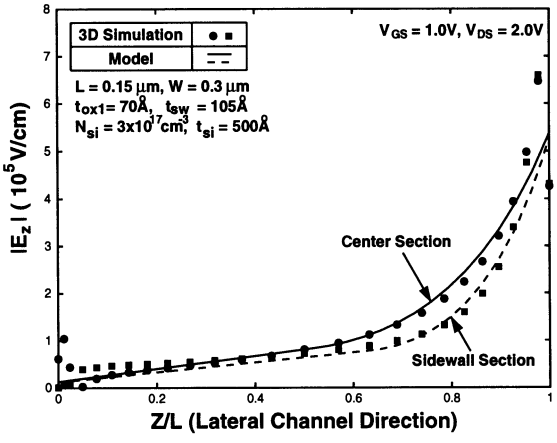


Figure 6.5: The magnitude of the electric field in the lateral channel of a fully-depleted mesa-isolated NMOS device with a gate oxide of 70Å, a sidewall oxide of 105Å, an p-type 500Å silicon thin-film doped with $3 \times 10^{17}\text{cm}^{-3}$, a channel length of 0.15μm and a channel width of 0.3μm, biased at $V_{GS} = 1V$, and $V_{DS} = 2V$, based on the analytical model and 3D simulation results.

Considering appropriate boundary conditions, one obtains:

$$\begin{aligned} V(z) &= V_{Dsat,s} + a_s\lambda_s^2 + \frac{\lambda_s(E_{1,s} - a_s\lambda_s)}{2} \cdot exp(-\frac{z-(L-\Delta L_s)}{\lambda_s}) \\ &\quad -\frac{\lambda_s(E_{1,s} + a_s\lambda_s)}{2} \cdot exp(\frac{z-(L-\Delta L_s)}{\lambda_s}), \\ E(z) &= -\frac{dV(z)}{dz}, \quad E_{1,s} = -\frac{(2-\eta_1)V_{Dsat,s}}{L}. \end{aligned} \tag{6.17}$$

Based on the analytical model and the 3D simulation results as shown in Fig. 6.5, the slope of the electric field profile in the sidewall channel region is larger than that in the center channel region. From Eq.(6.17) and considering $V(L) = V'_{DS}$, one obtains the length of the post-saturation region in the sidewall channel region:

$$\Delta L_s = s \cdot \lambda_s \cdot ln[\frac{-(V'_{DS} - V_{Dsat,s} - a_s\lambda_s^2) - \sqrt{(V'_{DS} - V_{Dsat,s} - a_s\lambda_s^2)^2 + \lambda_s^2(E_{1,s}^2 - a_s^2\lambda_s^2}}{\lambda_s \cdot (E_{1,s} + a_s\lambda_s)}$$

(6.

Therefore, the drift current in the sidewall channel region of the device biased in the saturation region is:

$$I_{drift,s} = \mu_{eff,s}(V_{Dsat,s}) \cdot 2 \cdot (C_e + C_{sw} \cdot t_{si}) \frac{1}{L - \Delta L_s} \cdot [(V'_{GS} - V_{TH,s}) V_{Dsat,s} - \frac{1}{2} V^2_{Dsat,s}]. \tag{6.19}$$

The total drain current is composed of the drift and the diffusion currents in both the center and the sidewall channel regions of the device:

$$I_D = I_{drift,c} + I_{diff,c} + I_{drift,s} + I_{diff,s}. \tag{6.20}$$

6.6 Capacitance Model

The capacitance model for an SOI CMOS device used in the ST-SPICE can be divided into three portions: the intrinsic capacitances in the device biased in (1) the triode region, (2) the saturation region, and (3) the fringing capacitance.

6.6.1 triode region

When a submicron SOI CMOS device biased in the triode region, in the center channel region, assuming that the electron temperature (T_n) is linearly proportional to the electric field ($\frac{dV(z)}{dz}$), from Ref. [23], one obtains

$$\begin{aligned} T_n(z) - T_L &\simeq \frac{T_n(L) - T_L}{\frac{dV}{dz}|_{z=L} - \frac{dV}{dz}|_{z=0}} \cdot (\frac{dV(z)}{dz} - \frac{dV}{dz}|_{z=0}), \\ &= \frac{q}{2\alpha k}[-1 + (1 + p \cdot \mu^2_{s,c} {V'_{DS}}^2)^{\frac{1}{2}}] \cdot \frac{\frac{dV(z)}{dz} + E_{0,c}}{-a_c L}, \\ E_{0,c} &= -\frac{\eta_1 V'_{DS}}{L}, \quad \alpha = \frac{3\mu_{s,c}}{2v^2_{sat}\tau_\epsilon}. \end{aligned} \tag{6.21}$$

From the electron-temperature related mobility model, one obtains:

$$I_{drift,c} = \frac{\mu_{s,c}}{1 + \alpha\frac{k}{q}(T_n(z) - T_L)} \cdot C_{ox1} W \cdot [V'_{GS} - V_{TH,c} - a_{0,c} V(y)]. \tag{6.22}$$

Multiplying Eq.(6.22) by $1 + \alpha\frac{k}{q}(T_n(z) - T_L)$, from Eq.(6.21), one obtains:

$$\frac{dV(Z)}{dz} = \frac{A_c}{C_c} + \frac{B_c}{C_c} V(z), \quad z = \frac{A_c}{C_c} V(z) + \frac{B_c}{2C_c} V(z)^2, \tag{6.23}$$

$$
\begin{aligned}
A_c &= \frac{\mu_{s,c}}{I_{drift,c}} \cdot WC_{ox1} \cdot (V'_{GS} - V_{TH,c}) + \frac{1}{2a_cL}[-1 + (1 + p \cdot \mu_{s,c}^2 \cdot {V'_{DS}}^2)^{\frac{1}{2}}], \\
B_c &= -\frac{\mu_{s,c}}{I_{drift,c}} \cdot WC_{ox1} \cdot a_{0,c}, \\
C_c &= 1 - \frac{E_{0,c}}{2a_cL}[-1 + (1 + p \cdot \mu_{s,c}^2 \cdot {V'_{DS}}^2)^{\frac{1}{2}}].
\end{aligned}
$$

From Ref [33] and Eq.(6.23), when the device is biased in the triode region, the intrinsic gate charge, the source charge, and the drain charge in the center channel region are

$$
\begin{aligned}
Q_{G,triode,c}(V'_{DS}) &= W\int_0^L C_{ox1}[V'_{GS} - V_{TH,c} - a_{0,c}V(z)]dz, \qquad (6.24) \\
&= W\int_0^{V'_{DS}} C_{ox1}[V'_{GS} - V_{TH,c} - a_{0,c}V](\frac{dV}{dz})^{-1}dV, \\
&= C_{ox1}W \cdot [\frac{A_c}{C_c}[V'_{GS} - V_{TH,c})V'_{DS} + (-\frac{a_{0,c}A_c}{C_c} + \\
&\quad \frac{B_c}{C_c}(V'_{GS} - V_{TH,c}))\frac{{V'_{DS}}^2}{2} - \frac{a_{0,c}B_c}{C_c}\frac{{V'_{DS}}^3}{3}], \\
Q_{S,triode,c}(V'_{DS}) &= W\int_0^L (1 - \frac{z}{L})(-C_{ox1})[V'_{GS} - V_{TH,c} - a_{0,c}V(z)]dz, \\
&= W\int_0^{V'_{DS}} (1 - \frac{A_c}{LC_c}V - \frac{B_c}{2LC_c}V^2)(-C_{ox1}) \times \\
&\quad [V'_{GS} - V_{TH,c} - a_{0,c}V](\frac{dV}{dz})^{-1}dV, \\
&= -C_{ox1}W \cdot [\frac{A_c}{C_c}(V'_{GS} - V_{TH,c})V'_{DS} + (-\frac{a_{0,c}A_c}{C_c} + (\frac{B_c}{C_c} - \\
&\quad \frac{A_c^2}{LC_c^2})(V'_{GS} - V_{TH,c}))\frac{{V'_{DS}}^2}{2} + (\frac{a_{0,c}A_c^2}{LC_c^2} - \frac{a_{0,c}B_c}{C_c} - \frac{3A_cB_c}{2LC_c^2} \times \\
&\quad (V'_{GS} - V_{TH,c}))\frac{{V'_{DS}}^3}{3} + (\frac{3a_{0,c}A_cB_c}{2LC_c^2} - \frac{B_c^2}{2LC_c^2}(V'_{GS} - V_{TH,c})) \times \\
&\quad \frac{{V'_{DS}}^4}{4} + \frac{a_{0,c}B_c^2}{2LC_c^2}\frac{{V'_{DS}}^5}{5}], \\
Q_{D,triode,c}(V'_{DS}) &= W\int_0^L \frac{z}{L}(-C_{ox1})[V'_{GS} - V_{TH,c} - a_{0,c}V(z)]dz, \\
&= W\int_0^{V'_{DS}} (\frac{A_c}{LC_c}V + \frac{B_c}{2LC_c}V^2)(-C_{ox1}) \times
\end{aligned}
$$

$$
\begin{aligned}
& [V'_{GS} - V_{TH,c} - a_{0,c}V](\frac{dV}{dz})^{-1}dV, \\
= \; & -C_{ox1}W \cdot [\frac{A_c^2}{LC_c^2}(V'_{GS} - V_{TH,c})\frac{{V'_{DS}}^2}{2} + (-\frac{a_{0,c}A_c^2}{LC_c^2} + \\
& \frac{3A_cB_c}{2LC_c^2}(V'_{GS} - V_{TH,c}))\frac{{V'_{DS}}^3}{3} + (-\frac{3a_{0,c}A_cB_c}{2LC_c^2} + \\
& \frac{B_c^2}{2LC_c^2}(V'_{GS} - V_{TH,c}))\frac{{V'_{DS}}^4}{4} - \frac{a_{0,c}B_c^2}{2LC_c^2}\frac{{V'_{DS}}^5}{5}],
\end{aligned}
$$

respectively. Similarly, in the sidewall channel region, the gate charge, the source charge, and the drain charge of the SOI MOS device, biased in the triode region are

$$
\begin{aligned}
Q_{G,triode,s}(V'_{DS}) &= 2 \cdot (C_e + C_{sw} \cdot t_{si}) \cdot [\frac{A_s}{C_s}[V'_{GS} - V_{TH,s}]V'_{DS} + (-\frac{A_s}{C_s} + \frac{B_s}{C_s} \times \\
& (V'_{GS} - V_{TH,s}))\frac{{V'_{DS}}^2}{2} - \frac{B_s}{C_s}\frac{{V'_{DS}}^3}{3}], \qquad (6.25) \\
Q_{S,triode,s}(V'_{DS}) &= -2 \cdot (C_e + C_{sw} \cdot t_{si}) \cdot [\frac{A_s}{C_s}(V'_{GS} - V_{TH,s})V'_{DS} + (-\frac{A_s}{C_s} + \\
& (\frac{B_s}{C_s} - \frac{A_s^2}{LC_s^2}) \times (V'_{GS} - V_{TH,s})) \cdot \frac{{V'_{DS}}^2}{2} + (\frac{A_s^2}{LC_s^2} - \frac{B_s}{C_s} - \\
& \frac{3A_sB_s}{2LC_s^2}(V'_{GS} - V_{TH,s}))\frac{{V'_{DS}}^3}{3} + (\frac{3A_sB_s}{2LC_s^2} - \\
& \frac{B_s^2}{2LC_s^2}(V'_{GS} - V_{TH,s})) \cdot \frac{{V'_{DS}}^4}{4} + \frac{B_s^2}{2LC_s^2}\frac{{V'_{DS}}^5}{5}], \\
Q_{D,triode,s}(V'_{DS}) &= -2 \cdot (C_e + C_{sw} \cdot t_{si}) \cdot [\frac{A_s^2}{LC_s^2}(V'_{GS} - V_{TH,s})\frac{{V'_{DS}}^2}{2} + (-\frac{A_s^2}{LC_s^2} + \\
& \frac{3A_sB_s}{2LC_s^2}(V'_{GS} - V_{TH,s})) \cdot \frac{{V'_{DS}}^3}{3} + (-\frac{3A_sB_s}{2LC_s^2} + \frac{B_s^2}{2LC_s^2} \times \\
& (V'_{GS} - V_{TH,s}))\frac{{V'_{DS}}^4}{4} - \frac{B_s^2}{2LC_s^2}\frac{{V'_{DS}}^5}{5}], \\
A_s &= \frac{\mu_{s,s}}{I_{drift,s}} \cdot 2(C_e + C_{sw} \cdot t_{si}) \cdot (V'_{GS} - V_{TH,s}) + \\
& \frac{1}{2a_sL}[-1 + (1 + p \cdot \mu_{s,s}^2 \cdot {V'_{DS}}^2)^{\frac{1}{2}}], \\
B_s &= -\frac{\mu_{s,s}}{I_{drift,s}} \cdot 2(C_e + C_{sw} \cdot t_{si}),
\end{aligned}
$$

$$C_s = 1 - \frac{E_{0,s}}{2a_s L}[-1 + (1 + p \cdot \mu_{s,s}^2 \cdot {V'_{DS}}^2)^{\frac{1}{2}}],$$

respectively.

6.6.2 saturation region

When an SOI MOS device biased in the saturation region, the charge in the pre-saturation and the post-saturation regions should be considered [34]. Therefore, the gate charge, the source charge, and the drain charge in the center channel region are

$$\begin{aligned}
Q_{G,sat,c} &= W\int_0^{L-\Delta L_c} C_{ox1}[V'_{GS} - V_{TH,c} - a_{0,c}V(z)]dz + \\
&\quad W\int_{L-\Delta L_c}^{L} C_{ox1}[V'_{GS} - V_{TH,c} - a_{0,c}V_{Dsat,c}]dz, \\
&= Q_{G,triode,c}(V_{Dsat,c}) + C_{ox1}W(V'_{GS} - V_{TH,c} - a_{0,c}V_{Dsat,c})\Delta L_c, \\
Q_{S,sat,c} &= W\int_0^{L-\Delta L_c} (1 - \frac{z}{L})(-C_{ox1})[V'_{GS} - V_{TH,c} - a_{0,c}V(z)]dz + \\
&\quad W\int_{L-\Delta L_c}^{L} (1 - \frac{z}{L})(-C_{ox1})[V'_{GS} - V_{TH,c} - a_{0,c}V_{Dsat,c}]dz, \\
&= Q_{S,troide,c}(V_{Dsat,c}) - C_{ox1}W(V'_{GS} - V_{TH,c} - a_{0,c}V_{Dsat,c})\frac{\Delta L_c^2}{2L}, \\
Q_{D,sat,c} &= W\int_0^{L-\Delta L_c} \frac{z}{L}(-C_{ox1})[V'_{GS} - V_{TH,c} - a_{0,c}V(z)]dz + \\
&\quad W\int_{L-\Delta L_c}^{L} \frac{z}{L}(-C_{ox1})[V'_{GS} - V_{TH,c} - a_{0,c}V_{Dsat,c}]dz, \\
&= Q_{D,troide,c}(V_{Dsat,c}) - C_{ox1}W(V'_{GS} - V_{TH,c} - a_{0,c}V_{Dsat,c})(1 - \frac{\Delta L_c}{2L})\Delta L_c,
\end{aligned} \tag{6.26}$$

respectively. Similarly, in the sidewall channel region, the gate charge, the source charge, and the drain charge are:

$$\begin{aligned}
Q_{G,sat,s} &= Q_{G,triode,s}(V_{Dsat,s}) + 2(C_e + C_{sw} \cdot t_{si})(V'_{GS} - V_{TH,s} - V_{Dsat,s})\Delta L_s, \\
Q_{S,sat,s} &= Q_{S,troide,s}(V_{Dsat,s}) - 2(C_e + C_{sw} \cdot t_{si})(V'_{GS} - V_{TH,s} - V_{Dsat,s})\frac{\Delta L_s^2}{2L}, \\
Q_{D,sat,s} &= Q_{D,troide,s}(V_{Dsat,s}) - 2(C_e + C_{sw} \cdot t_{si})(V'_{GS} - V_{TH,s} - V_{Dsat,s})(1 - \frac{\Delta L_s}{2L})\Delta L_s,
\end{aligned} \tag{6.27}$$

respectively.

6.6.3 fringing capacitance

In an SOI MOS device , the fringing capacitances between source/drain and front gate in the center channel region and in the sidewall channel region are also important. From Ref. [35], the fringing capacitances in the center and the sidewall channel regions are

$$\begin{aligned} C_{f,c} &= \frac{2\epsilon_{si}W}{\pi} ln[1 + \frac{1.5t_{si}}{t_{ox1}} \cdot sin(\frac{\pi\epsilon_{ox}}{2\epsilon_{si}})], \\ C_{f,s} &= \frac{4\epsilon_{si}t_{si}}{\pi} ln[1 + \frac{W}{2t_{sw}} \cdot sin(\frac{\pi\epsilon_{ox}}{2\epsilon_{si}})], \end{aligned} \tag{6.28}$$

respectively.

Considering the gate charge, the source charge, and the drain charge of both the center and sidewall channel regions of an SOI CMOS device biased in the triode and the saturation regions, one obtains the capacitance model:

$$\begin{aligned} C_{ij} = {} & (-1)^m \frac{dQ_{i,c}}{dV_j} + C_{f,c}[1 - 2 \cdot \frac{(-1)^m \frac{dQ_{i,c}}{dV_j}}{C_{ox1}WL}] + \\ & (-1)^m \frac{dQ_{i,s}}{dV_j} + C_{f,s}[1 - \frac{(-1)^m \frac{dQ_{i,s}}{dV_j}}{(C_e + C_{sw} \cdot t_{si})L}], \end{aligned} \tag{6.29}$$

where i, j can be G, S, or D. When $i \neq j$, $m = 1$. When $i = j$, $m = 0$.

6.7 Non-Local Impact Ionization & Parasitic BJT Effects Model

For a submicron SOI CMOS device biased at a large V_{DS}, impact ionization in the post-saturation region is important. Therefore, the drain current may increase abruptly. Considering the non-local effect [36][37], the multiplication factors in the both center and the sidewall channel regions are

$$\begin{aligned} M_c &= 1 + \frac{\gamma\lambda_c^2}{B_0(\lambda_c + \lambda_0)}(V'_{DS} - V_{Dsat,c}) \cdot exp[-\frac{B_0(\lambda_c + \lambda_0)}{V'_{DS} - V_{Dsat,c}}], \\ M_s &= 1 + \frac{\gamma\lambda_s^2}{B_0(\lambda_s + \lambda_0)}(V'_{DS} - V_{Dsat,s}) \cdot exp[-\frac{B_0(\lambda_s + \lambda_0)}{V'_{DS} - V_{Dsat,s}}], \end{aligned} \tag{6.30}$$

respectively. γ, B_0, and λ_0 are the parameters related to non-local impact ionization. λ_c and λ_s, which are the parameters related to the slope of the internal electric field

profile, can be obtained from Eqs.(6.13)&(6.16). When impact ionization occurs, the parasitic BJT in the silicon thin-film is activated. As a result, the conducting current is magnified [24][25]. By considering the non-local impact ionization and parasitic BJT effect, the drain current as shown in Eq.(6.20) is modified as:

$$
\begin{aligned}
I_D &= G_c I_{drift,c} + I_{diff,c} + H_c I_{CBO,c} + G_s I_{drift,s} + I_{diff,s} + H_s I_{CBO,s}, \quad (6.31)\\
G_c &= 1 + \frac{(M_c - 1)[1 - (1 - K)\alpha_0]}{1 - [1 + KK'(M_c - 1)]\alpha_0},\\
H_c &= \frac{1 + K'(M_c - 1)}{1 - [1 + KK'(M_c - 1)]\alpha_0}, \quad I_{CBO,c} = \frac{W t_{si} I_{s0}}{1 + \theta_I (V'_{GS} - V_{TH,c})},\\
G_s &= 1 + \frac{(M_s - 1)[1 - (1 - K)\alpha_0]}{1 - [1 + KK'(M_s - 1)]\alpha_0},\\
H_s &= \frac{1 + K'(M_s - 1)}{1 - [1 + KK'(M_s - 1)]\alpha_0}, \quad I_{CBO,s} = \frac{l_0 t_{si} I_{s0}}{1 + \theta_I (V'_{GS} - V_{TH,s})},
\end{aligned}
$$

where α_0 is the common-base current gain of the parasitic BJT. K and K' are the fitting parameters referred to the conducting current distribution in the silicon thin-film. $I_{CBO,c}$ and $I_{CBO,s}$, which are leakage currents caused by the parasitic BJT near the center and sidewall channel regions, respectively, are important only when V'_{DS} is large enough. I_{s0} and θ_I are the parameters related to the leakage current.

6.8 Thermal Effect Model

Between the silicon thin-film and the substrate in the SOI CMOS devices, there is a buried oxide layer. A thick buried oxide may prevent the SOI device from dissipating the heat generated in the active region of the silicon thin-film. As a result, the lattice temperature may increase. Under this situation, thermal effect is important in determining the performance of the device [23][26][27]. As indicated in Eq.(6.9), the low-field mobility is inversely proportional to the lattice temperature—$\mu_0(T_L) \propto T_L^{-2}$. Therefore, the lattice temperature (T_L) may affect the mobility, hence the drain current of the device. Lattice temperature can be computed by considering the equivalent circuit, which is composed of a current source, R_{TH} and C_{TH} as shown in Fig. 6.6[27]. The current source is made by the power of the device—$I_D V_{DS}$. R_{TH}, which is the thermal resistance between the device and the ambient, is closely correlated to the thickness of the buried oxide. A thicker buried oxide leads to a larger thermal resistance. C_{TH} is the thermal capacitance between the device and the ambient. From Fig. 6.6, the lattice temperature can be obtained

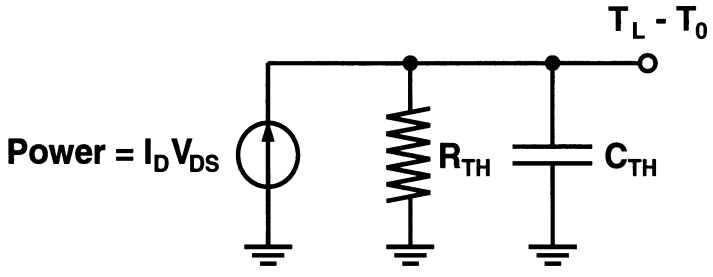


Figure 6.6: The equivalent circuit model of the SOI CMOS device considering thermal effect.

from the following equations:

$$-power + \frac{1}{R_{th}}(T_L - T_0) + C_{th} \cdot \frac{d}{dt}(T_L - T_0) = 0, \qquad (6.32)$$
$$power = I_D(T_L) \cdot V_{DS}.$$

6.9 Usage of ST-SPICE

The device models of deep-submicron fully-depleted SOI CMOS devices described in the previous section have been incorporated in the ST-SPICE program. In the ST-SPICE, only inversion-mode fully-depleted SOI CMOS devices are considered. For inversion-mode SOI NMOS devices, the N^+ poly gate is used with the p-type silicon thin-film. For inversion-mode SOI PMOS devices, the P^+ poly gate is used with the n-type silicon thin-film.

Table 6.1 lists the device parameters and their corresponding names in the ST-SPICE. In addition, the default values for all parameters have been included in the table. Shown in Fig. 6.7 are a set of model cards for SOI CMOS devices used in the ST-SPICE. Except channel length and width (L, W), thermal resistance (R_{TH}), and thermal capacitance (C_{TH}), all other parameters need to be defined in the model cards. L, W, R_{TH}, and C_{TH} are needed to be defined for all transistors in their individual transistor cards. In addition, only when the thermal resistance is not zero ($R_{TH} \neq 0$), thermal effect will be included. Similarly, only when the thickness of the sidewall oxide (t_{sw}) is defined, ST-SPICE will consider the sidewall-channel-related current and capacitances. Furthermore, ST-SPICE provides capabilities to inspect internal physical parameters such as lattice temperature, capacitances, and effective mobility etc. In the following paragraphs, steady state and transient results from

Symbol	ST-SPICE parameter	Default value	Unit
L	l	5×10^{-6}	m
W	w	5×10^{-6}	m
R_{th}	rth	0	K/W
C_{th}	cth	0	J/K
t_{si}	tsi	1000×10^{-10}	m
t_{ox1}	tox1	100×10^{-10}	m
t_{ox2}	tox2	4000×10^{-10}	m
t_{sw}	tsw	$t_{ox1} \cdot 1.5$	m
N_{si}	nsi	5×10^{16}	cm^{-3}
N_{sub}	nsubo	1×10^{15}	cm^{-3}
$\mu_0(T_0)$	mu0	440	$cm^2/Vsec$
θ	theta	1.05	$1/V$
s	s	0.75	–
η_1	eta1	0.27	–
η_2	eta2	1.0	–
τ_ϵ	taue	0.48×10^{-12}	sec
v_{sat}	vsato	1.5×10^5	m/sec
C_e	ce	0.5×10^{-10}	F/m
γ	gamma	4.4×10^{14}	m^{-2}
B_0	bo	9×10^7	V/m
λ_0	lambda0	900×10^{-10}	m
α_0	alphao	0.997	–
I_{s0}	is0	0	A/m^2
θ_I	thetai	1.0	$1/V$
K	k	0.95	–
K'	kprime	0.95	–
I_1	i1	0.12×10^{-6}	A
I_2	i2	1×10^{-11}	$A \cdot m$
V_J	vj	0.006	V
V_{FB}	vfb	$-(E_g/2 - \phi_{si})$	V

Table 6.1: Model parameters used in ST-SPICE.

```
****ST-SPICE Model Cards
*model=SOI Technology CMOS
.MODEL N1 NMOS
+Level=8
+Tsi=500e-10 Tox1=70e-10 Tox2=800e-10
+Tsw=105e-10 Nsi=3e17 Nsubo=1e15 Ce=0.5e-10
+mu0=440 theta=1.05 s=0.75 eta1=0.27 eta2=1.0
+taue=0.48e-12 vsato=1.5e5

.MODEL P1 PMOS
+Level=8
+Tsi=500e-10 Tox1=70e-10 Tox2=800e-10
+Tsw=105e-10 Nsi=3e17 Nsubo=1e15 Ce=0.5e-10
+Rsh=350 Vfb=0.89 mu0=100 theta=0.5 s=0.7
+eta1=0.01 eta2=1.0 taue=0.48e-12 vsato=1.5e5
```

Figure 6.7: A set of ST-SPICE device model cards.

the ST-SPICE models are compared with the 3D simulation results [38] and experimental data.

6.9.1 Steady State Analysis

Figs. 6.8 show the drain current versus V_{DS} of the SOI CMOS devices with a gate oxide of t_{ox1} = 70Å, a sidewall oxide of 105Å, a 500Å silicon thin-film doped with a density of (p-type for NMOS, n-type for PMOS) $3 \times 10^{17}\text{cm}^{-3}$, a buried oxide of t_{ox2} = 800Å, a channel length of 0.15μm, and a channel width of (a) 3μm PMOS, (b) 3μm NMOS, (c) 0.3μm PMOS, (d)0.3μm NMOS, based on the ST-SPICE models and 3D simulation results. From the figures, the IV curves of the PMOS and NMOS devices are symmetric to each other. When the channel width of the CMOS devices is scaled down from 3μm to 0.3μm, the drain current is not scaled down accordingly due to the relatively more importance of the sidewall channel region at a smaller channel width.

Figs. 6.9 show C_{GS}—(a) PMOS (b) NMOS and C_{GD}—(c) PMOS (d) NMOS versus V_{GS} of the SOI CMOS devices with a gate oxide of t_{ox1} = 70Å, a sidewall oxide of 105Å, a 500Å silicon thin-film doped with a density of (p-type for NMOS, n-type

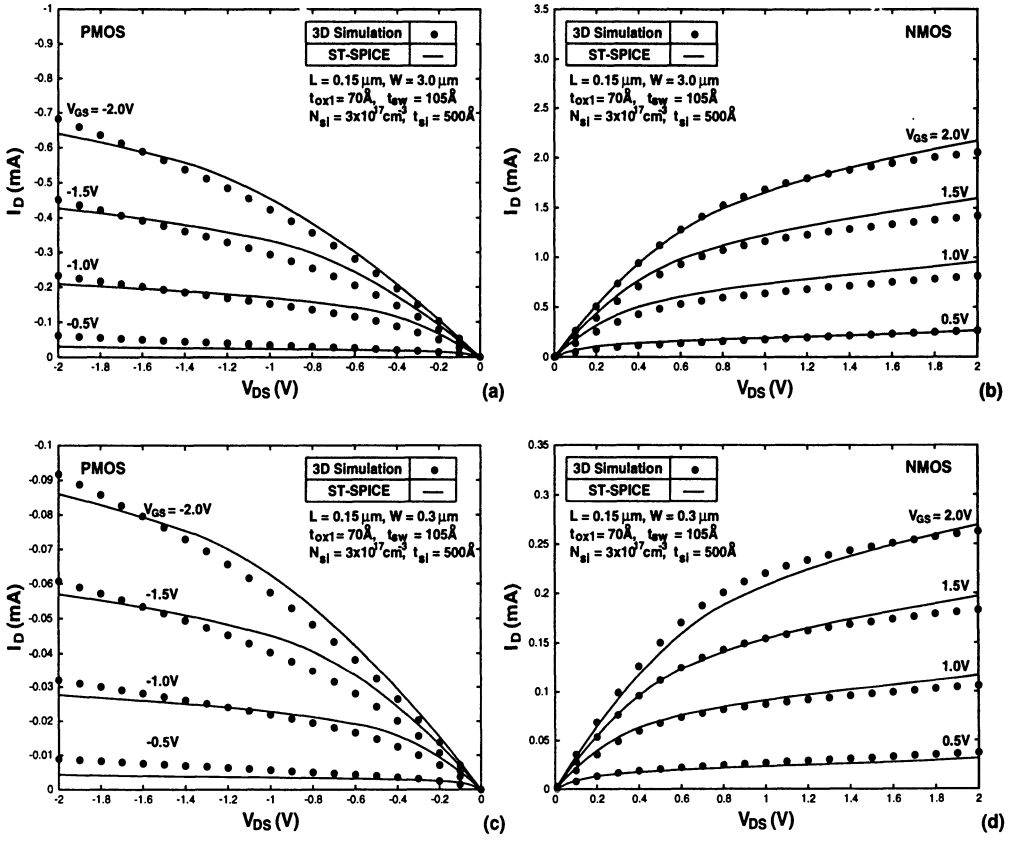


Figure 6.8: Drain current versus V_{DS} of the SOI CMOS devices with a gate oxide of t_{ox1} = 70Å, a sidewall oxide of 105Å, a 500Å silicon thin-film doped with a density of (p-type for NMOS, n-type for PMOS) $3 \times 10^{17}\text{cm}^{-3}$, a buried oxide of t_{ox2} = 800Å, a channel length of 0.15μm, and a channel width of (a) 3μm PMOS, (b) 3μm NMOS, (c) 0.3μm PMOS, (d)0.3μm NMOS, based on the ST-SPICE models and 3D simulation results.

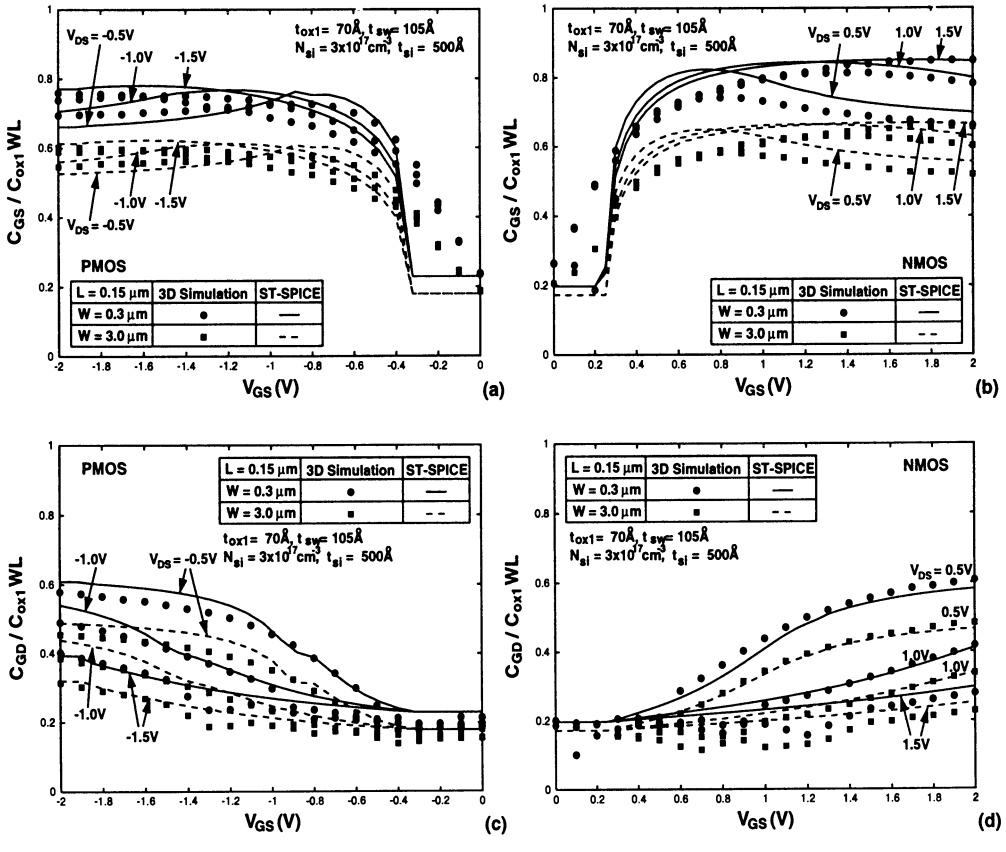


Figure 6.9: C_{GS}—(a) PMOS (b) NMOS and C_{GD}—(c) PMOS (d) NMOS versus V_{GS} of the SOI CMOS devices with a gate oxide of $t_{ox1} = 70$Å, a sidewall oxide of 105Å, a 500Å silicon thin-film doped with a density of (p-type for NMOS, n-type for PMOS) $3 \times 10^{17}\text{cm}^{-3}$, a buried oxide of $t_{ox2} = 800$Å, a channel length of 0.15μm, and channel widths of 0.3μm and $3\mu m$, biased at V_{DS} from $0.5V$ to $1.5V$, based on the ST-SPICE models and 3D simulation results.

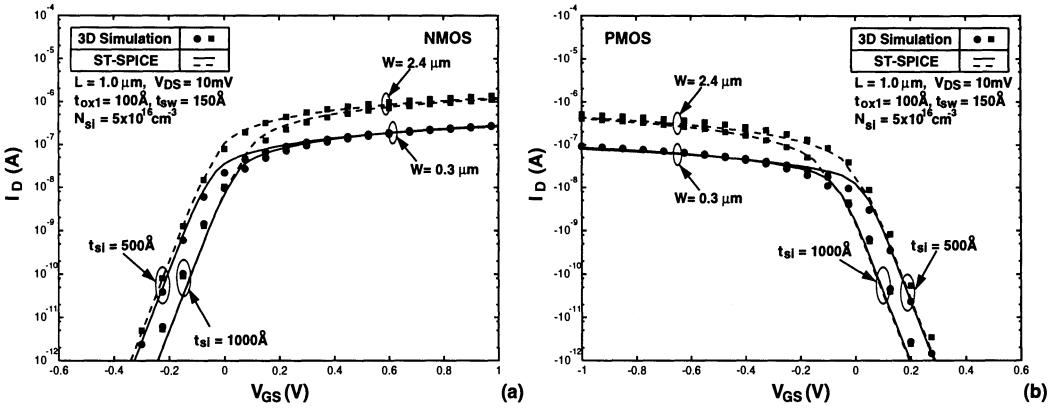


Figure 6.10: Subthreshold characteristics: drain current versus V_{GS} of the SOI (a) NMOS (b) PMOS devices with a gate oxide of $t_{ox1} = 100$Å, a sidewall oxide of 150Å, a silicon thin-film of 500Å and 1000Å doped with a density of (p-type for NMOS, n-type for PMOS) $5 \times 10^{16}\text{cm}^{-3}$, a buried oxide of $t_{ox2} = 4000$Å, and a channel length of 1μm, and channel widths of 0.3μm and $2.4\mu m$, biased at V_{DS} of $10mV$, based on the ST-SPICE models and 3D simulation results.

for PMOS) $3 \times 10^{17}\text{cm}^{-3}$, a buried oxide of $t_{ox2} = 800$Å, a channel length of 0.15μm, and channel widths of 0.3μm and $3\mu m$, biased at V_{DS} from $0.5V$ to $1.5V$, based on the ST-SPICE models and 3D simulation results. As shown in the figures, due to the sidewall channel, at a channel width of 0.3μm, the normalized capacitances are larger than those at a channel width of 3μm. In addition, due to the fringing effect, the capacitances are not zero when the device is turned off.

Figs. 6.10 show the subthreshold characteristics: drain current versus V_{GS} of the SOI (a) NMOS (b) PMOS devices with a gate oxide of $t_{ox1} = 100$Å, a sidewall oxide of 150Å, a silicon thin-film of 500Å and 1000Å doped with a density of (p-type for NMOS, n-type for PMOS) $5 \times 10^{16}\text{cm}^{-3}$, a buried oxide of $t_{ox2} = 4000$Å, and a channel length of 1μm, and channel widths of 0.3μm and $2.4\mu m$, biased at V_{DS} of $10mV$, based on the ST-SPICE models and 3D simulation results. As shown in the figures, in the subthreshold region, the drain current is not affected by the channel width due to the sidewall channel. Since the magnitude of the threshold voltage of the sidewall channel region is smaller than that of the center channel region, subthreshold current is dominated by the sidewall channel, which is valid for both PMOS and NMOS devices regardless of channel width and silicon thin-film

thickness.

Figs. 6.11 show the non-local impact ionization & parasitic BJT effect and the thermal effect—(a) drain current (b) lattice temperature (c) effective electron temperature and effective mobility versus V_{DS} of the SOI NMOS device with a gate oxide of t_{ox1} = 70Å, a p-type doped silicon thin-film of 800Å, a buried oxide of t_{ox2} = 4000Å, a channel length of 0.25μm, and a channel width of 9.5μm, biased at V_{GS} from 0.5V to 2V, based on the ST-SPICE models and experimental data [39]. Note that the effective electron temperature is defined as the average temperature in the presaturation region of the device. As shown in Fig. 6.11(a), at $V_{GS} = 2V$ and $V_{DS} = 2.5V$, due to the large power consumption, the elevation of the lattice temperature is noticeable. As a result, a higher V_{DS} leads to a smaller I_D— a negative differential output resistance. If V_{DS} is further increased, the drain current increases abruptly due to the non-local impact ionization and parasitic BJT effect. In addition, the non-local impact ionization and parasitic BJT effect is more noticeable at a smaller V_{GS}. As shown in Fig. 6.11(b), when V_{DS} or V_{GS} gets higher, the power consumption of the device gets larger, hence the lattice temperature becomes higher. As shown in Figs. 6.11(b)&(c), although the lattice temperature increases by only several tens of degrees, the effective electron temperature has been raised by over several hundred degrees, which is strongly correlated to the results in Ref. [23] As shown in Fig. 6.11(c), the effective mobility reflects the trends on lattice and effective electron temperatures.

6.9.2 Transient Analysis

After verifying steady state performance of the SOI CMOS devices, transient performance is verified. Figs. 6.12 show (a) pull-down (b) pull-up transients of a CMOS inverter using SOI CMOS devices with a gate oxide of t_{ox1} = 70Å, a sidewall oxide of 105Å, a 500Å silicon thin-film doped with a density of (p-type for NMOS, n-type for PMOS) $3 \times 10^{17}\text{cm}^{-3}$, a buried oxide of t_{ox2} = 800Å, a channel length of 0.15μm, and channel widths of 0.3μm and 3μm, based on the ST-SPICE results and 3D simulation results. The output load capacitance is 10fF. As shown in Figs. 6.12(a)&(b), due to inclusion of the sidewall channel region model in ST-SPICE, regardless of the channel width, the model results can predict well the transient performance as verified by the 3D simulation results. Using ST-SPICE, the transient analysis took about 0.6 seconds CPU time on a 200MIPs workstation. In contrast, using 3D device-level simulation, it took about 160 hours CPU time. The advantages of ST-SPICE can be seen.

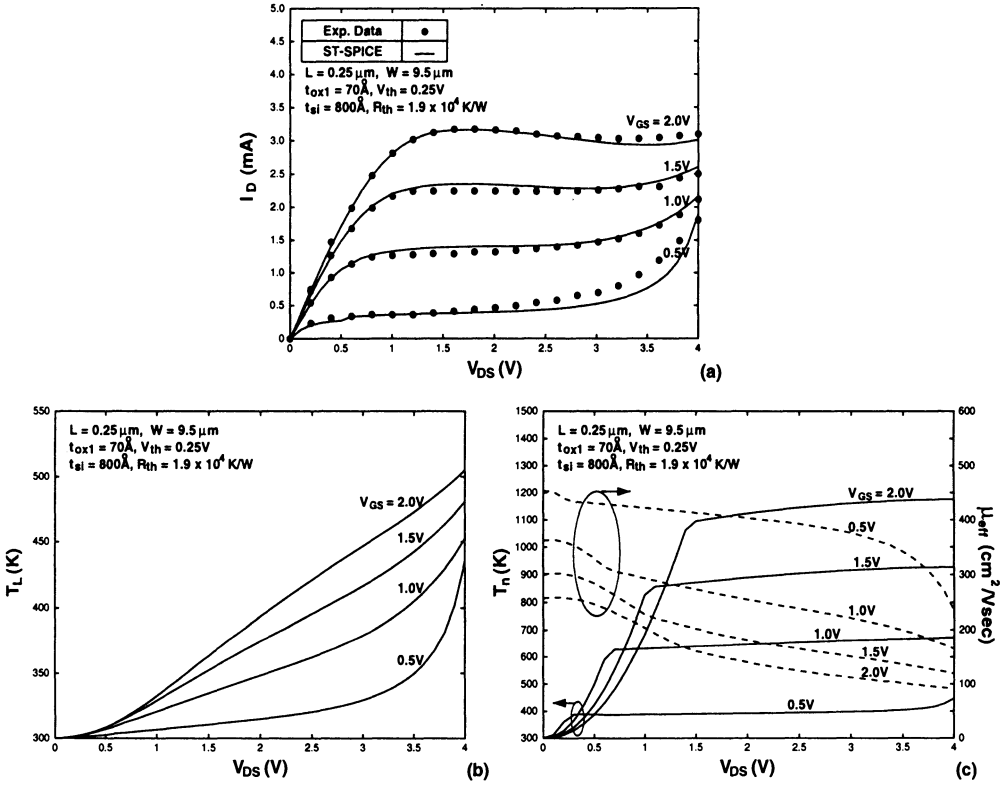


Figure 6.11: The non-local impact ionization & parasitic BJT effect and the thermal effect—(a) drain current (b) lattice temperature (c) effective electron temperature and effective mobility versus V_{DS} of the SOI NMOS device with a gate oxide of $t_{ox1} = 70$Å, a p-type doped silicon thin-film of 800Å, a buried oxide of $t_{ox2} = 4000$Å, a channel length of 0.25μm, and a channel width of $9.5\mu m$, biased at V_{GS} from 0.5V to 2V, based on the ST-SPICE models and experimental data .

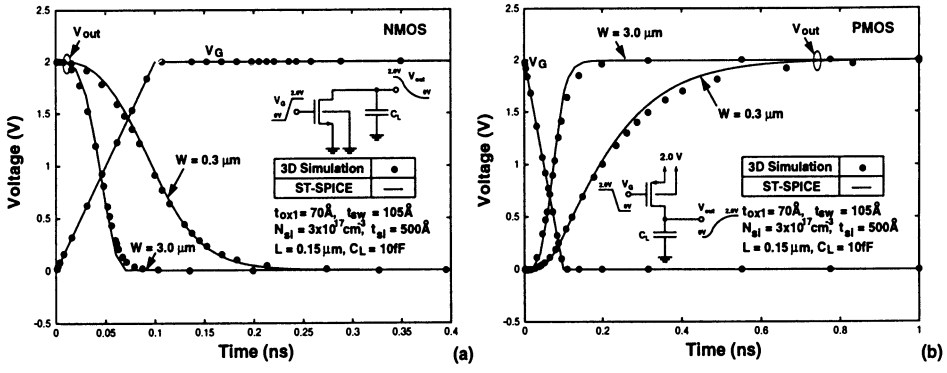


Figure 6.12: (a) Pull-down (b) pull-up transients of a CMOS inverter using SOI CMOS devices with a gate oxide of $t_{ox1} = 70$Å, a sidewall oxide of 105Å, a 500Å silicon thin-film doped with a density of (p-type for NMOS, n-type for PMOS) $3 \times 10^{17}\text{cm}^{-3}$, a buried oxide of $t_{ox2} = 800$Å, a channel length of 0.15μm, and channel widths of 0.3μm and $3\mu m$, based on the ST-SPICE results and 3D simulation results. The output load capacitance is 10fF.

Figs. 6.13&6.14 show a user program for simulating the transient performance of an SOI CMOS inverter using ST-SPICE, and (a) drain current versus V_{DS} of the SOI NMOS and PMOS devices with a gate oxide of $t_{ox1} = 80$Å, a 450Å silicon thin-film, a buried oxide of $t_{ox2} = 1100$Å, a channel length of 0.35μm, and a channel width of 10μm based on the ST-SPICE models and experimental data [40], (b) transient waveforms of the inverter and the NAND circuits using the SOI CMOS devices at a supply voltage of 2V and an output load capacitance of 25fF, (c) propagation delay versus supply voltage of the CMOS inverter using the SOI CMOS devices and an output capacitive load of 25fF, based on the ST-SPICE results and experimental data [39]. As shown in Figs. 6.14(a), due to larger power consumption, the NMOS device shows a negative differential output resistance at $V_{GS} = 3V$ and $V_{DS} = 3V$. For the NMOS device, at a smaller V_{GS}, an abrupt change in the drain current due to the non-local impact ionization & parasitic BJT effect can be identified. On the other hand, for the PMOS device, the negative differential output resistance and the non-local impact ionization & parasitic BJT effects can not be seen. From Fig. 6.14(c), at a lower supply voltage, the propagation delay of the inverter and the NAND circuits is longer. The propagation delay of the NAND circuit is longer than that of the inverter circuit. As verified by the experimental data [40], ST-SPICE

```
*** CMOS inverter for SOI-Technology (ST) SPICE general purpose check ***

m1 1 in out 0 p1 L=0.35u W=10u rth=0.8e4 cth=5e-10 display=lt
m2 out in 0 0 n1 L=0.35u W=10u rth=0.8e4 cth=5e-10 display=lt

*vdd 1 0 2.0
*vin in 0 1.0
*.dc vin 0 2.0 0.1
*.print dc m1#lt

c1 out 0 25fF
vdd 1 0 2.0
vin in 0 dc 0.0V pulse 0.0 2.0 0.2ns 0.1ns 0.1ns 0.3ns 10ns
.tran 1ps 1.0ns

*** Model Card ***
*model = SOI Technology
*ST-SPICE compatibility

.model N1 NMOS
+Level=8
+Tsi=450e-10 Tox1=80e-10 Tox2=1100e-10 Rsh=70 Vfb=-0.6
+mu0=450 theta=0.28 s=0.6 eta1=0.01 eta2=1.0 taue=0.48e-12
+vsato=1.5e5 alphao=0.9958 k=0.95 kprime=0.95
+gamma=4.0e14 bo=8.8e7 lambda0=900e-10

.model P1 PMOS
+Level=8
+Tsi=450e-10 Tox1=80e-10 Tox2=1100e-10 Rsh=300 Vfb=0.6
+mu0=100 theta=0.08 s=0.6 eta1=0.01 eta2=0.8 taue=0.48e-12
+vsato=1.5e5 gamma=0
```

Figure 6.13: A user program for simulating the transient performance of an SOI CMOS inverter using ST-SPICE.

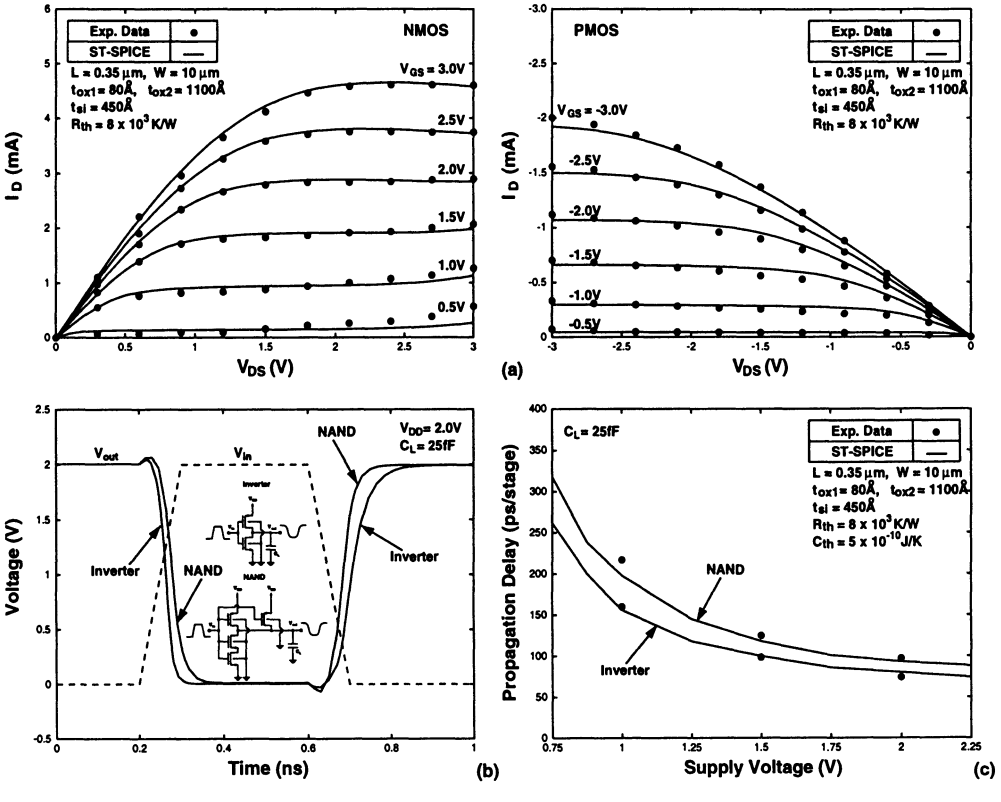


Figure 6.14: (a) Drain current versus V_{DS} of the SOI NMOS and PMOS devices with a gate oxide of $t_{ox1} = 80$Å, a 450Å silicon thin-film, a buried oxide of $t_{ox2} = 1100$Å, a channel length of 0.35μm, and a channel width of 10μm based on the ST-SPICE models and experimental data [40]. (b) Transient waveforms of the inverter and the NAND circuits using the SOI CMOS devices. (c) Propagation delay versus supply voltage of the CMOS inverter using the SOI CMOS devices and an output load capacitance of 25fF, based on the ST-SPICE results and experimental data [40].

can predict the performance of the inverter and the NAND circuits.

6.10 Implications from ST-SPICE

Different from conventional SPICE programs, the ST-SPICE program has incorporated the SOI CMOS device models considering electron and lattice temperatures, which are important in determining the steady state and transient characteristics of deep-submicron SOI CMOS devices.

In order to show the importance of the thermal effect on the transient behavior, Figs. 6.15 show the transient performance in terms of drain current, lattice temperature, electron temperature, and effective mobility of an SOI NMOS device with parameters as indicated in Fig. 6.11, considering the thermal effect: a thermal capacitance of $C_{TH} = 7 \times 10^{-10} J/K$ and a thermal resistance of $R_{TH} = 1.9 \times 10^4 K/W$ and $8.5 \times 10^3 K/W$ based on the ST-SPICE results. A pulse from 0V to 2V with a rise/fall time of 0.1ns is imposed on the input of the SOI NMOS device, which is biased at $V_{DS} = 2V$. As shown in Fig. 6.15, when the gate voltage rises from 0V to 2V, the drain current rises to the maximum value. However, due to the heat generated by the power consumption, the lattice temperature increases gradually. During turn-on of the device, the electron temperature almost keeps at a constant value. When the lattice temperature increases, the electron temperature also increases slightly. Therefore, the effective mobility, which is related to the electron and the lattice temperatures, reacts accordingly. Consequently, the drain current decays gradually. When V_G switches from 2V to 0V, the device turns off. The lattice temperature decreases slowly. When the lattice temperature is not back to the room temperature, if V_G turns high again, the peak drain current will be lower than the previous peak value. With a larger thermal resistance, the decrease in the drain current due to thermal effect is more noticeable. In addition, due to a longer thermal time constant ($R_{TH}C_{TH}$) at a larger R_{TH}, the time for the lattice temperature to reach thermal equilibrium is longer.

6.11 Summary

In this chapter, the SOI-Technology ST-SPICE CAD program has been described. Starting from the fundamentals of the SPICE CAD program, the analytical device models of deep-submicron fully-depleted SOI CMOS devices used in ST-SPICE for CAD of VLSI circuits have been reported. The analytical models include the drain current and the capacitance models in the subthreshold, the triode and the satura-

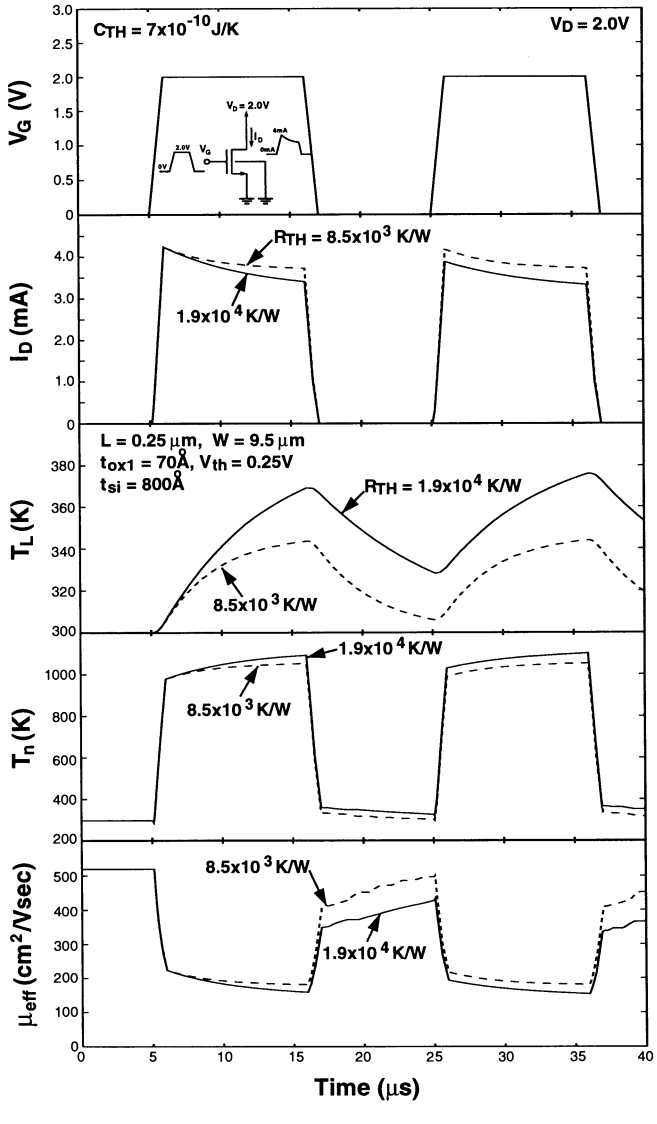


Figure 6.15: Transient performance in terms of drain current, lattice temperature, electron temperature, and effective mobility of an SOI NMOS device with parameters as indicated in Fig. 6.11, considering the thermal effect: a thermal capacitance of $C_{TH} = 7 \times 10^{-10} J/K$ and a thermal resistance of $R_{TH} = 1.9 \times 10^4 K/W$ and $8.5 \times 10^3 K/W$ based on the ST-SPICE results.

tion regions. In addition, the analytical models contain the small-geometry effect, the electron-temperature dependent mobility effect, the sidewall conduction effect , the non-local impact ionization effect & parasitic BJT effect, and the thermal effect. Usage of the SOI-Technology ST-SPICE CAD program has been described in terms of the circuit simulation examples for steady state and transient behaviors of SOI CMOS circuits.

References

[1] A. J. Auberton-Herve, "SOI: Materials to Systems," *IEDM Dig.*, pp. 3-10, 1996.

[2] Y. Yamaguchi and Y. Inoue, "SOI DRAM: Its Features and Possibility," *SOI Conf. Dig.*, pp. 122-124, 1995.

[3] H.-S. Kim, S.-B. Lee, D.-U. Choi, J.-H. Shim, K.-C. Lee, K.-P. Lee, K.-N. Kim, and J.-W. Park, "A High Performance 16M DRAM on a Thin Film SOI," *Symp. VLSI Tech. Dig.*, pp. 143-144, 1995.

[4] K. Suma, T. Tsuruda, H. Hidaka, T. Eimori, T. Oashi, Y. Yamaguchi, T. Iwamatsu, M. Hirose, K. Fujishima, Y. Inoue, T. Nishimura, and T. Yoshihara, "An SOI-DRAM with Wide Operating Voltage Range by CMOS/SIMOX Technology," *ISSCC Dig.*, pp. 138-139, 1994.

[5] H. Lu, E. Yee, L. Hite, T. Houston, Y.-D. Sheu, R. Rajgopal, C. C. Shen, J.-M. Hwang, and G. Pollack, "A 1-M Bit SRAM on SIMOX Material," *SOI Conf. Dig.*, pp. 182-183, 1993.

[6] T. Iwamatsu, Y. Yamaguchi, Y. Inoue, T. Nishimura, and N. Tsubouchi, "CAD-Compatible High-Speed CMOS/SIMOX Technology Using Field-Shield Isolation for 1M Gate Array," *IEDM Dig.*, pp. 475-478, 1993.

[7] Y. Kado, T. Ohno, M. Harada, K. Deguchi, and T. Tsuchiya, "Enhanced Performance of Multi-GHz PLL LSIs Using Sub-1/4-micron Gate Ultrathin Film CMOS/SIMOX Technology with Synchrotron X-Ray Lithography," *IEDM Dig.*, pp. 243-246, 1993.

[8] R. Rajsuman, "Implementation of Switch Network Logic in SOI," *IEEE J. Sol. St. Ckts*, Vol. 25, No. 3, pp. 874-877, June 1990.

[9] Y. Omura, S. Nakashima, K. Izumi, and T. Ishii, "0.1-μm-Gate, Ultrathin-Film CMOS Devices Using SIMOX Substrate with 80-nm-Thick Buried Oxide Layer," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 5, pp. 1019-1022, May 1993.

[10] M. Fujishima, K. Asada, Y. Omura, and K. Izumi, "Low-Power 1/2 Frequency Dividers Using 0.1-μm CMOS Circuits Built with Ultrathin SIMOX Substrates," *IEEE J. Sol. St. Ckts*, Vol. 28, No. 4, pp. 510-512, Apr. 1993.

[11] K. Ohuchi, R. Ohba, H. Nhyama, K. Nakajima, and T. Mizuno, "A High-Performance 0.05μm SOI MOS FET: Possibility of Velocity Overshoot," *Jpn. J. Appl. Phys.*, Vol. 35, No. 2B, pp. 960-964, Feb. 1996.

[12] Y. Hu, T. Houston, R. Rajgopal, K. Joyner, and C. Teng, "Isolation Techniques for 256MBit SOI DRAM Application," *SOI Conf. Dig.*, pp. 26-27, 1995.

[13] J. B. Kuo, Y. G. Chen, and K. W. Su, "Sidewall-Related Narrow Channel Effect in Mesa-Isolated Fully-Depleted Ultra-Thin SOI NMOS Devices," *IEEE Elec. Dev. Let.*, Vol. 16, No. 9, pp. 379-381, Sept. 1995.

[14] K. W. Su and J. B. Kuo, "Modeling Narrow-Channel Effect in VLSI Mesa-Isolated SOI MOS Devices Using a Quasi-Two-Dimensional Approach," *Sol. St. Elec.*, Vol. 39, No. 9, pp. 1321-1329, Sept. 1996.

[15] K. K. Young, "Short-Channel Effect in Fully Depleted SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 2, pp. 399-402, Feb. 1989.

[16] J. B. Kuo, K. W. Su, Y. G. Chen, and S. S. Chen, "Short-Channel Effect on the Threshold Voltage of Accumulation-Type, Inversion-Type and Intrinsic-Type SOI PMOS Devices," *Sol. St. Elec.*, Vol. 38, No. 10, pp. 1845-1847, Oct. 1995.

[17] K. W. Su and J. B. Kuo, "Analytical Threshold Voltage Model Considering Small-Geometry Effects for VLSI Mesa-Isolated Fully-Depleted Ultrathin SOI NMOS Devices Using a Quasi-3D Approach," private communication.

[18] P. J. VanDerVoorn and J. P. Krusius, "Inversion Channel Edge in Trench-Isolated Sub-1/4-μm MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 43, No. 8, pp. 1274-1280, Aug. 1996.

[19] M. Matloubian, R. Sundaresan, and H. Lu, "Measurement and Modeling of the Sidewall Threshold Voltage of Mesa-Isolated SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 5, pp. 938-942, May 1989.

[20] T. Elewa, B. Kleveland, S. Cristoloveanu, B. Boukriss, and A. Chovet, "Detailed Analysis of Edge Effects in SIMOX-MOS Transistors," *IEEE Trans. Elec. Dev.*, Vol. 39, No. 4, pp. 874-882, Apr. 1992.

[21] D. Chen, E. C. Kan, U. Ravaioli, C.-W. Shu, and R. W. Dutton, "An Improved Energy Transport Model Including Nonparabolicity and Non-Maxwellian Distribution Effects," *IEEE Elec. Dev. Let.*, Vol. 13, No. 1, pp. 26-28, Jan. 1992.

[22] S. Y. Ma and J. B. Kuo, "Concise Analytical Model for Deep Submicron N-Channel Metal-Oxide-Semiconductor Devices with Consideration of Energy Transport," *Jpn. J. Appl. Phys.*, Vol. 33, No. 1B, pp. 550-553, Jan. 1994.

[23] Y.-G. Chen, S.-Y. Ma, J. B. Kuo, Z. Yu, and R. W. Dutton, "An Analytical Drain Current Model Considering both Electron and Lattice Temperatures Simultaneously for Deep Submicron Ultrathin SOI NMOS Devices with Self-Heating," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 5, pp. 899-906, May 1995.

[24] K. W. Su and J. B. Kuo, "A Non-Local Impact Ionization/Lattice Temperature Model for VLSI Double-Gate Ultrathin SOI NMOS Devices," *IEEE Trans. Elec. Dev.*, Vol. 44, No. 2, pp. 324-330, Feb. 1997.

[25] Y. G. Chen, J. B. Kuo, Z. Yu, and R. W. Dutton, "An Analytical Drain Current Model for Short-Channel Fully-Depleted Ultrathin Silicon-on-Insulator NMOS Devices," *Sol. St. Elec.*, Vol. 38, No. 12, pp. 2051-2057, Dec. 1995.

[26] M. Berger and Z. Chai, "Estimation of Heat Transfer in SOI-MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 4, pp. 871-875, Apr. 1991.

[27] J. Bielefeld, G. Pelz, H. B. Abel, and G. Zimmer, "Dynamic SPICE-Simulation of the Electrothermal Behavior of SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 42, No. 11, pp. 1968-1974, Nov. 1995.

[28] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng, "BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors," *IEEE J. Sol. St. Ckts*, Vol. 22, No. 4, pp. 558-566, Aug. 1987.

[29] J.-H. Sim and J. B. Kuo, "An Analytical Back-Gate Bias Effect Model for Ultrathin SOI CMOS Devices," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 4, pp. 755-765, Apr. 1993.

[30] P. Antognetti, D. D. Caviglia, and E. Profumo, "CAD Model for Threshold and Subthreshold Conduction in MOSFET's," *IEEE J. Sol. St. Ckts*, Vol. 17, No. 3, pp. 454-458, Jun. 1982.

[31] K. K. Young, "Analysis of Conduction in Fully Depleted SOI MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 3, pp. 504-506, Mar. 1989.

[32] J. B. Kuo and K. W. Su, "Compact Current Model for Mesa-Isolated Fully-Depleted Ultrathin SOI NMOS Devices Considering Sidewall-Related Narrow Channel Effects," *SOI Conf. Dig.*, pp. 84-85, 1997.

[33] D. E. Ward and R. W. Dutton, "A Charge-Oriented Model for MOS Transistor Capacitances," *IEEE J. Sol. St. Ckts*, Vol. 13, No. 5, pp. 703-708, Oct. 1978.

[34] B. J. Sheu and P.-K Ko, "Measurement and Modeling of Short-Channel MOS Transistor Gate Capacitances," *IEEE J. Sol. St. Ckts*, Vol. 22, No. 3, pp. 464-472, June 1987.

[35] R. Shrivastava and K. Fitzpatrick, "A Simple Model for the Overlap Capacitance of a VLSI MOS Device," *IEEE Trans. Elec. Dev.*, Vol. 29, No. 12, pp. 1870-1875, Dec. 1982.

[36] J. M. Higman, I. C. Kizilyalli, and K. Hess, "Nonlocality of the Electron Ionization Coefficient in n-MOSFET's: An Analytic Approach," *IEEE Elec. Dev. Let.*, Vol. 9, No. 8, pp. 399-401, Aug. 1988.

[37] K. Taniguchi, M. Yamaji, K. Sonoda, T. Kunikiyo, and C. Hamaguchi, "Monte Carlo Study of Impact Ionization Phenomena in Small Geometry MOSFET's," *IEDM Dig.*, pp. 355-358, 1994.

[38] DAVINCI: Three-Dimensional Device Simulation Program, *Technology Modeling Associates, Inc.*, 1996.

[39] J. Chen, S. Parke, J. King, F. Assaderaghi, P. K. Ko, and C. Hu, "A High Speed SOI Technology with 12ps/18ps Gate Delay Operating at 5V/1.5V," *IEDM Dig.*, pp. 35-38, 1992.

[40] H. Nakamura, K. Imai, H. Onishi, K. Kumagai, T. Yamada, K. Iwaki, Y. Matsubara, T. Ishigami, S. Kurosawa, and T. Horiuchi, "High Performance Dual-Gate FD-SOI CMOS Process with an Ultra Thin $TiSi_2$," *SOI Conf. Dig.*, pp. 24-25, 1997.

Problems

1. Consider a mesa-isolated SOI NMOS device using an N^+ poly-gate, a front gate oxide of 70Å, a sidewall oxide of 105Å, a silicon thin-film of 500Å doped with a p-type density of $3 \times 10^{17}\text{cm}^{-3}$, a channel length of 0.15μm, and a channel width of 0.3μm. Other parameters are as shown in Table 6.1.

   (a) What are the threshold voltages in the center channel and in the sidewall channel?

   (b) At $V_{GS} = 1V$, $V_{DS} = 0.5V$, what are C_{GD} and the drain current? What are the proportions of C_{GD} and the drain current in the center channel and the sidewall channel?

(c) At $V_{GS} = 1V$, $V_{DS} = 2V$, repeat (a) and (b). In which region (triode or saturation), the relative importance of the sidewall portion is higher? Why?

(d) As for (c), what are the lateral electric field in the channel direction in the sidewall channel and the center channel? In the post-saturation region, which channel (center or sidewall) has a more noticeable non-local effect? Why?

2. Based on the parameters and the circuits in Fig.6.13, analyze the following problems.

(a) At $R_{th} = 0, 0.8 \times 10^4, 1.6 \times 10^4 K/W$, what happens to the DC transfer curve of the circuit?

(b) Consider a ring oscillator made of a 11-stage inverter. At $R_{th} = 0, 0.8 \times 10^4, 1.6 \times 10^4 K/W$ and $C_{th} = 0, 7 \times 10^{-10} J/K$, what is the oscillation frequency at the beginning? When the thermal equilibrium is reached, what is the oscillation frequency? How much time does it take to reach thermal equilibrium?

(c) If the inverter is changed to a 2-input NAND or NOR gate, repeat (a) and (b). Which logic gate (NAND or NOR) is more sensitive to the self-heating effect?

(d) If the load capacitance is 2pF, repeat (a)-(c). Discuss the self-heating effect on the performance of the circuit operating at high and low speeds.

Chapter 7

Special-Purpose SOI

In this chapter, special-purpose SOI devices are described. Fully-Depleted Lean-Channel Transistors (DELTA), which are similar to double-gate SOI CMOS devices, are vertical SOI transistors. In the beginning of this chapter, DELTAs are presented. In order to improve the surface-scattering mobility of SOI PMOS devices, SiGe-channel SOI PMOS devices were reported. The SiGe-channel is assuming the concept from the heterojunction bipolar transistors (HBT) based on engineering bandgap narrowing. However, due to the SiGe quantum well introduced, the body effect is much more complicated than conventional SOI CMOS devices. In the following portion of this chapter, SiGe-channel SOI PMOS devices are described. SOI technology has also been used to integrate power devices. Owing to the buried oxide structure, SOI power devices are suitable for high-temperature operations. In this chapter, SOI DMOS devices are described. Recently, SOI technology has also been used to integrate BiCMOS devices. SOI MESFET and JFETs have also been created. In addition, single-electron transistors (SET) built on SOI SIMOX substrates have been realized. Amorphous and polysilicon thin-film transistors built on insulators have been used for LCD. In this chapter, these special-purpose SOI devices are described sequentially.

7.1 Fully-Depleted Lean-Channel Transistors (DELTA)

Fig. 7.1 shows the cross section of the Fully-Depleted Lean-Channel Transistor (DELTA)[1], which is similar to the double-gate SOI MOS structure shown in the previous chapter except that the device has been rotated by 90 degrees. In the DELTA structure, one sidewall oxide is at the top and the other is replaced by the buried oxide at the bottom. The channel in DELTA is formed on a vertical surface, therefore the channel width depends on the height of the silicon island. DELTA

J. B. Kuo et al., *CMOS VLSI Engineering*

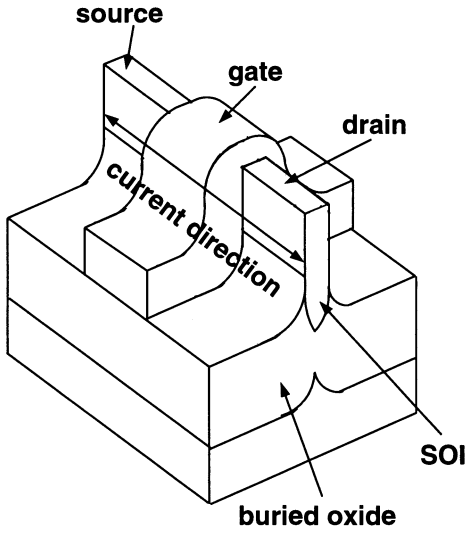


Figure 7.1: Device structure of the fully-depleted lean-channel transistors (DELTA).

provides superior device characteristics in reduced short channel effects, minimized subthreshold swing and high transconductance[2]. Fig.7.2 shows (a) the subthreshold and (b) the strong inversion characteristics of DELTA[2]. In (a) subthreshold characteristics, the DELTA has a gate width of 0.2μm and a channel length of 0.2μm. In (b) strong inversion IV, the DELTA has a channel length of 0.57μm and a gate width of 0.15μm. As shown in the figure, healthy subthreshold and strong inversion IV curves can be seen. Fig. 7.3 shows the threshold voltage versus channel length of DELTA and bulk NMOS devices[1]. As shown in the figure, DELTA demonstrates a smaller short channel effect as compared to the bulk NMOS devices.

In addition to the short channel effect, when the size of a DELTA is scaled down, it also demonstrates narrow channel effect[3]. In the following portion, the narrow channel effect of the DELTA is described. As shown in Fig. 7.4(a), by exchanging the x axis with the y axis, the equations for double-gate case can still be applicable[3]. Considering the vertical direction at $x = (1-\gamma)t_{si}$, most equations for the double-gate devices in the previous chapter are still valid upon replacing $\Psi(\gamma t_{si}, y)$ by $\Psi((1-\gamma)t_{si}, y)$:

$$\frac{\partial^2 \Psi[(1-\gamma)t_{si}, y]}{\partial y^2} = \frac{\Psi[(1-\gamma)t_{si}, y]}{{l_2}^2} + c_2, \tag{7.1}$$

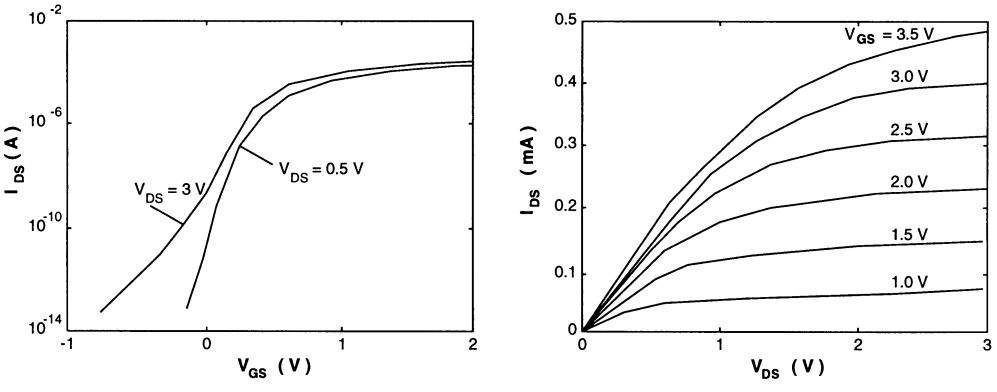


Figure 7.2: (a) Subthreshold and (b) strong inversion characteristics of DELTA. In (a) subthreshold characteristics, the DELTA has a gate width of 0.2μm and a channel length of 0.2μm. In (b) strong inversion IV, the DELTA has a channel length of 0.57μm and a gate width of 0.15μm.

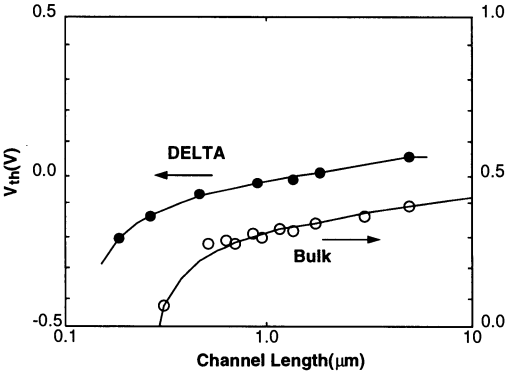


Figure 7.3: Threshold voltage versus channel length of DELTA and bulk NMOS devices.

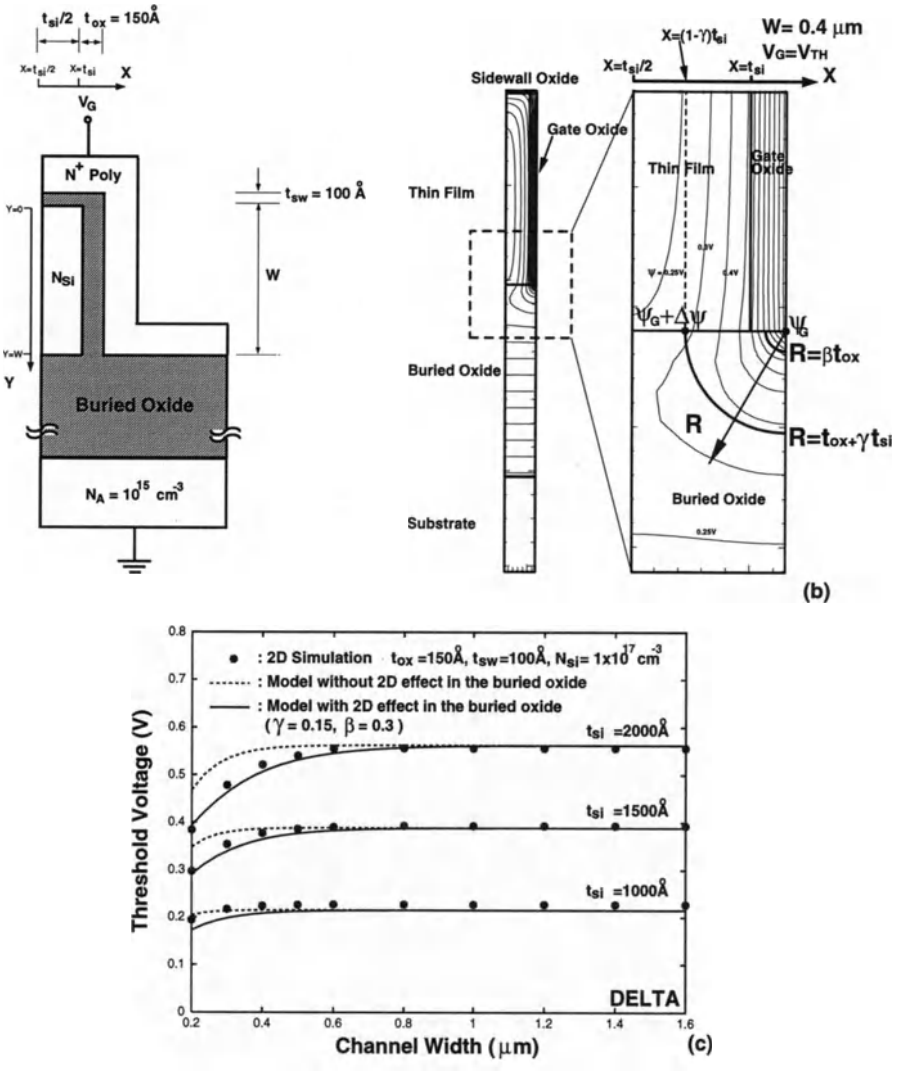


Figure 7.4: (a) Cross section and (b) 2D electrostatic potential contours near the edge of the gate oxide. (c) Threshold voltage versus channel width of the fully-depleted lean-channel transistor (DELTA), with a gate oxide of 150Å, a sidewall oxide of 100Å, and an acceptor density of $1 \times 10^{17}\text{cm}^{-3}$ in silicon thin-films of 1000Å, 1500Å and 2000Å.

where $l_2 = t_{si}\sqrt{\frac{1}{2}(\gamma - \gamma^2 + \frac{C_{si}}{C_{ox}})}$, and $c_2 = \frac{qN_{si}}{\epsilon_{si}} - \frac{\Psi_G}{l_2{}^2}$.

The boundary conditions of the above differential equation are below.
(i) One boundary condition for the above differential equation is that the surface electrostatic potential at the top sidewall oxide interface is derived by applying Gauss' Law at the oxide interface:

$$\Psi[(1-\gamma)t_{si}, 0] = \Psi_G + \frac{\partial \Psi[(1-\gamma)t_{si}, y]}{\partial y}\Big|_{y=0} \cdot \frac{\epsilon_{si}}{\epsilon_{ox}} t_{sw}, \tag{7.2}$$

where $\frac{\partial \Psi[(1-\gamma)t_{si}, y]}{\partial y}$ is the derivative of the electrostatic potential at the oxide interface in the silicon thin-film.

(ii) The other boundary condition is that above the buried oxide in the silicon thin-film:

$$\Psi[(1-\gamma)t_{si}, W] = \Psi_G + \Delta\Psi, \tag{7.3}$$

where $\Delta\Psi$ can be determined by considering the 2D electrostatic potential contours in the bottom silicon thin-film region surrounded by the gate electrode and the buried oxide [3], as shown in the enlarged portion in Fig. 7.4(b). Applying Poisson's equation in cylindrical coordinates with the origin at the corner of the silicon thin-film surrounded by the buried oxide and the gate electrode, one obtains $\frac{1}{R}\frac{\partial}{\partial R}(R\frac{\partial \Psi}{\partial R}) + \frac{1}{R^2}\frac{\partial^2 \Psi}{\partial \theta^2} = 0$. In the region in the buried oxide near the origin of the cylindrical coordinate, $\frac{\partial^2 \Psi}{\partial \theta^2} \cong 0$, the Poisson's equation is simplified as

$$\frac{\partial}{\partial R}(R\frac{\partial \Psi}{\partial R}) \simeq 0. \tag{7.4}$$

The boundary conditions for the above differential equation are that the electric field and the electrostatic potential are continuous from the thin oxide region:

$$\begin{aligned} \frac{\partial \Psi}{\partial R}\Big|_{R=\beta t_{ox}} &\simeq -\frac{qN_{si}t_{si}}{2\epsilon_{ox}}, \\ \Psi(R=\beta t_{ox}) &\simeq \Psi_G - \frac{qN_{si}t_{si}}{2\epsilon_{ox}}\beta t_{ox}, \end{aligned} \tag{7.5}$$

where β is a parameter which can be used to monitor the electrostatic relationship between the buried oxide and the gate oxide. From Eqs. (7.4) and (7.5), $\Delta\Psi$, which is the voltage drop between Ψ_G and the electrostatic potential at $R = \gamma t_{si} + t_{ox}$, is

$$\Delta\Psi = -\frac{qN_{si}t_{si}}{2C_{ox}} \cdot \beta \cdot [1 + ln(\frac{t_{ox} + \gamma t_{si}}{\beta t_{ox}})]. \tag{7.6}$$

From Eqs. (7.1)-(7.3)& (7.6), the electrostatic potential at $x = (1-\gamma)t_{si}$ is

$$\Psi[(1-\gamma)t_{si}, y] = -c_2 {l_2}^2 + A_1 e^{-y/l_2} + A_2 e^{y/l_2}, \quad (7.7)$$

where $A_1 = \frac{\frac{qN_{si}{l_2}^2}{\epsilon_{si}}(e^{W/l_2} - 1 + \frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_2}) - \Delta\Psi(1 - \frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_2})}{(1+\frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_2})e^{W/l_2} - (1-\frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_2})e^{-W/l_2}}$, and $A_2 = \frac{\frac{qN_{si}{l_2}^2}{\epsilon_{si}}(1 + \frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_2} - e^{-W/l_2}) + \Delta\Psi(1 + \frac{C_{si}}{C_{sw}}\frac{t_{si}}{l}$

The threshold voltage formula considering the narrow-channel effect for DELTA can be derived by considering that at a location ($y = \frac{W_{eff}}{2}$) with the minimum electrostatic potential in the vertical direction in the silicon thin-film at $x = t_{si}$ where strong inversion has just been reached:

$$\Psi[x = t_{si}, y = \frac{W_{eff}}{2}] = -\phi_{si}. \quad (7.8)$$

At a location ($x = (1-\gamma)t_{si}$, $y = \frac{W_{eff}}{2}$) in the silicon thin-film, $\frac{\partial\Psi((1-\gamma)t_{si}, y)}{\partial y}|_{y=\frac{W_{eff}}{2}} = 0$. From Eq. (7.7), W_{eff} is $W_{eff} = l_2 \ln(\frac{A_1}{A_2})$, where l_2 is as shown in Eq. (7.1) and A_1 and A_2 are as shown in Eq. (7.7). Using W_{eff}, Eq. (7.7) can be further simplified to

$$\Psi[(1-\gamma)t_{si}, y] = -c_2 {l_2}^2 + 2cosh[(y - \frac{W_{eff}}{2})/l_2] \cdot \alpha_3 \cdot (\Psi_G + c_2 {l_2}^2), \quad (7.9)$$

where $\alpha_3 = \frac{1}{(1-\frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_2})e^{-W_{eff}/2l_2} + (1+\frac{C_{si}}{C_{sw}}\frac{t_{si}}{l_2})e^{W_{eff}/2l_2}}$. Considering Eqs. (7.8) & (7.9), the threshold voltage can be obtained:

$$V_{TH} = V_{FB} - \Psi_G - \phi_{si} = V_{FB} - 2\phi_{si} + \frac{qN_{si}{t_{si}}^2}{2\epsilon_{si}}\frac{C_{si}}{C_{ox}}(1 - 2\alpha_3). \quad (7.10)$$

Fig. 7.4(c) shows threshold voltage versus channel width of DELTA, with a gate oxide of 150Å, a sidewall oxide of 100Å, and an acceptor density of $1 \times 10^{17}\text{cm}^{-3}$ in the silicon thin-films of 1000Å, 1500Å and 2000Å, based on the 2D simulation data and the analytical formula considering the 2D effect in the buried oxide near the corner of the silicon thin-film with $\gamma = 0.15$ and $\beta = 0.3$ (solid lines)[3]. (Note: $\beta = 0.3$ is used to show that at a distance of $0.3t_{ox}$ from the corner in the buried oxide, the electric field and the electrostatic potential become scattered in the cylindrical shape.) Also shown in the figure are the curves for the analytical formula without considering the 2D effect in the buried oxide (dashed lines). As indicated by solid lines, considering the 2D effect in the buried oxide, the narrow-channel behavior in terms of threshold voltage can be predicted.

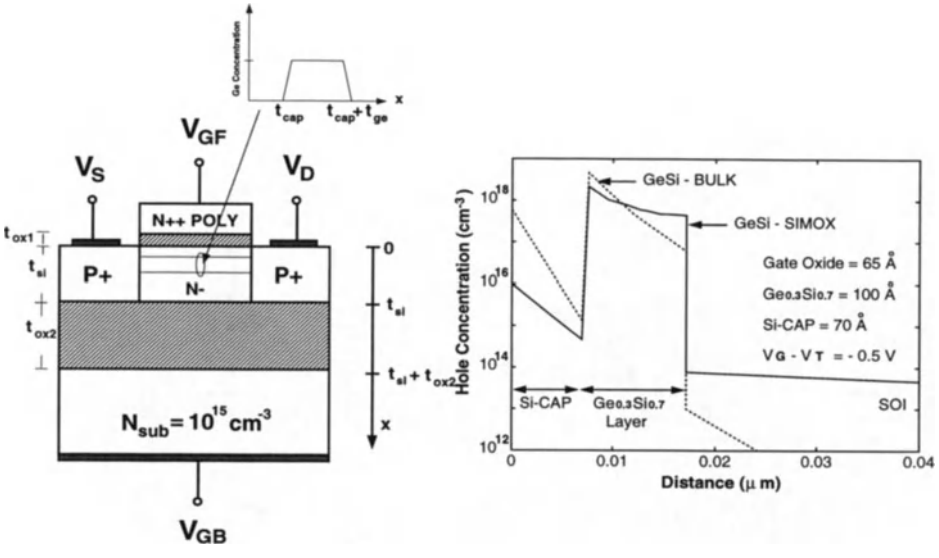


Figure 7.5: Cross section of a SiGe-channel SOI PMOS device.

7.2 SiGe SOI PMOS Devices

Based on the bandgap narrowing concept borrowing from the heterojunction bipolar transistors (HBT), SiGe-channel PMOS devices have been receiving lots of attention owing to their potentials in achieving high performance [5]-[6]. As shown in Fig. 7.5, using a SiGe heterostructure, a quantum well has been built in the PMOS device for improving its transconductance [4] since the conducting channel, which is in the quantum well, can be kept away from the $Si - SiO_2$ interface. As a result, surface scattering effect on reducing the effective mobility can be reduced. Furthermore, the hole mobility in a strained SiGe layer is higher than that in a bulk silicon. High performance SiGe-channel PMOS devices built on SOI structure using SIMOX technology were created [7]. Fig. 7.6 shows the IV characteristics of a SiGe-channel SOI PMOS and a conventional SOI PMOS device with an aspect ratio of $25\mu m/10\mu m$, a front gate oxide of 65Å, a buried oxide of 4100Å, a silicon thin-film of 1800Å, and a $Si_{0.7}Ge_{0.3}$ layer of 100Å, and a silicon cap of 100Å below the front gate oxide[4]. From this figure, the current driving capability of the SiGe-channel SOI PMOS device is much larger than the conventional SOI PMOS device.

SiGe-channel SOI PMOS devices have limitations. In addition to the compli-

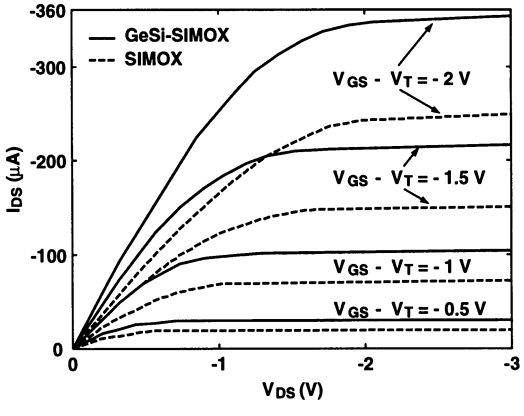


Figure 7.6: IV characteristics of a SiGe-channel SOI PMOS device and a conventional SOI PMOS device with an aspect ratio of $25\mu m/10\mu m$, a front gate oxide of 65Å, a buried oxide of 4100Å, a silicon thin-film of 1800Å, and a $Si_{0.7}Ge_{0.3}$ layer of 100Å, and a silicon cap of 100Å below the front gate oxide.

cated processing steps required, SiGe-channel SOI PMOS devices have complicated back-gate bias effect. In the remaining portion of this section, comparison of an SOI PMOS device with and without SiGe-channel in terms of internal hole distribution and back gate bias effects is described.

As shown in Fig. 7.5, the SiGe-channel SOI PMOS device structure is based on a SIMOX process [9]. The ultra-thin SOI PMOS device using an $N+$ polysilicon gate, has a front gate oxide of 120Å (t_{ox1}). Below the gate oxide, a silicon thin-film of 1000Å ($t_{cap} + t_{ge} + t_s$) is sitting on a field oxide of 3500Å (t_{ox2}). In the silicon thin-film an undoped silicon cap of 60Å (t_{cap}) below the gate oxide is placed atop the undoped SiGe-channel of 200Å (t_{ge}), where the germanium density is 0.25. Below the SiGe-channel, an n-type silicon thin-film of 740Å (t_s) doped with $1 \times 10^{16} cm^{-3}$ is used. Below the field oxide, a p-type substrate region with a doping concentration of $1 \times 10^{15} cm^{-3}$ has been used in the study. In order to show the uniqueness of the SiGe-channel SOI PMOS device in terms of the back gate bias effect on the subthreshold behavior, a standard SOI PMOS device without a SiGe-channel has been also studied – a silicon thin-film doped with $1 \times 10^{16} cm^{-3}$ n-type dopants has been used.

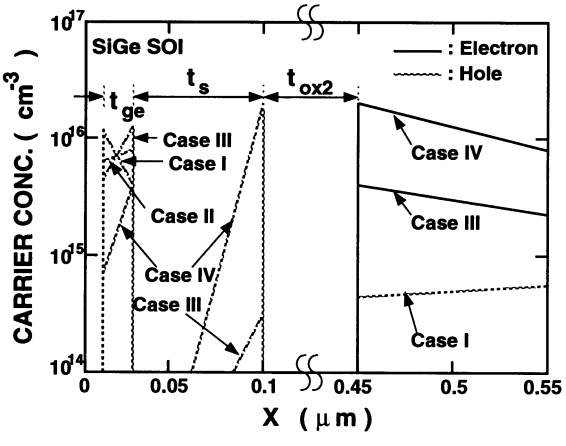


Figure 7.7: The internal carrier density distribution in the center of the SOI device biased at various back gate biases and a drain current of $10^{-7}A/\mu m$ with SiGe-channel.

Fig. 7.7 shows the internal carrier density distribution in the center of the SiGe-channel PMOS SOI device for various back gate biases and biased at a drain current of $I_D = 0.1\mu A/\mu m$ and $V_{DS} = -0.1V$[10]. Depending on the back gate bias, classified by the carrier distributions, there are four cases – Case I: a conduction channel at the top of the SiGe-channel and no inversion in the substrate, Case II: a conduction channel at the bottom of the SiGe-channel and no inversion in the substrate, Case III: a conduction channel at the bottom of the SiGe-channel and an inversion in the substrate, Case IV: a conduction channel at the top of the field oxide and an inversion in the substrate. Thanks to the existence of SiGe quantum well, the conduction channel is always present first in the SiGe region and the charge in the silicon cap can be neglected.

As shown in Fig. 7.5, consider the device in the substrate direction[8][10]. In Case I: without substrate inversion, with a conduction channel at the top of the SiGe channel, the threshold voltage of the device is defined as the gate voltage when the electrostatic potential at the top of the SiGe channel reaches $\Psi(t_1) = \phi_{fn(Ge)}$: $\phi_{fn(Ge)} = \frac{kT}{q} ln \frac{n_{i(Si)}}{N_D} + \frac{\Delta E_v}{q}$, where ΔE_v is the SiGe induced bandgap narrowing [11]-

[13]: $\Delta E_v = 0.0087y\ eV$ where y is the germanium content in percentage. The threshold voltage for Case I is:

$$V_{TH} = \phi_{fn(Ge)} + \phi_{poly} + \frac{\epsilon_{si} + C_{ox1}t_{cap}}{C_{ox1}}(-D + \sqrt{E + 2\frac{q}{\epsilon_{si}}N_{sub}\phi_{fn(Ge)}}), \quad (7.11)$$

where $D = q(N_{sub}(\frac{1}{C_{ge}}+\frac{1}{C_s}+\frac{1}{C_{ox2}})+\frac{N_D}{C_s})$, and $E = D^2 - 2\frac{qN_{sub}}{\epsilon_{si}}(qN_Dt_s(\frac{1}{2C_s+\frac{1}{C_{ox2}}})+\Psi_{sub}) - (\frac{qN_D}{C_s})^2$. In Case II: without substrate inversion and with a bottom SiGe channel, with a buried channel at the bottom of the SiGe channel, the threshold voltage of the device is defined as the gate voltage when the electrostatic potential at the bottom of the SiGe channel reaches $\Psi(t_2) = \phi_{fn(Ge)}$. The threshold voltage is:

$$V_{TH} = \phi_{fn(Ge)} + \phi_{poly} + \epsilon_{si}(\frac{1}{C_{ox1}} + \frac{1}{C_{ge}} + \frac{1}{C_{cap}})(-D + \sqrt{E + 2\frac{q}{\epsilon_{si}}N_{sub}\phi_{fn(Ge)}}), \quad (7.12)$$

where $C_{cap} = \epsilon_{si}/t_{cap}$. In Case III: with substrate inversion and with a bottom SiGe channel, the threshold voltage is defined as:

$$V_{TH} \equiv V_G(\Psi(t_2) = \phi_{fn(Ge)}, \Psi(t_4) = \Psi_{sub} + 2\phi_{f(sub)}).$$

The threshold voltage is

$$V_{TH} = \phi_{fn(Ge)} + \phi_{poly} + (\frac{1}{C_{ox1}} + \frac{1}{C_{cap}} + \frac{1}{C_{ge}})(\frac{C_{ox2}(\phi_{fn(Ge)} - 2\phi_{f(sub)} - \Psi_{sub} - \frac{qN_D}{2\epsilon_{si}}t_s^2) - qN_Dt_s}{1 + \frac{C_{ox2}}{C_s}}). \quad (7.13)$$

In Case IV: with surface inversion in the substrate and with a back channel at the top of the field oxide, the threshold voltage is defined as:

$V_{TH} \equiv V_G(\Psi(t_3) = \phi_{fn}, \Psi(t_4) = \Psi_{sub} + 2\phi_{f(sub)})$. The threshold voltage is:

$$V_{TH} = \phi_{poly} + \phi_{fn} - qN_Dt_s(\frac{1}{2C_s} + \frac{1}{C_{ox1}} + \frac{1}{C_{ge}} + \frac{1}{C_{cap}}) + C_{ox2}(\frac{1}{C_{ox1}} + \frac{1}{C_s} + \frac{1}{C_{ge}} + \frac{1}{C_{cap}})(\phi_{fn} - \Psi_{sub} - 2\phi_{f(sub)}). \quad (7.14)$$

Fig. 7.8 shows the threshold voltage versus back-gate bias voltage curves for the SOI PMOS device using the analytical model and 2D simulation results[10]. As

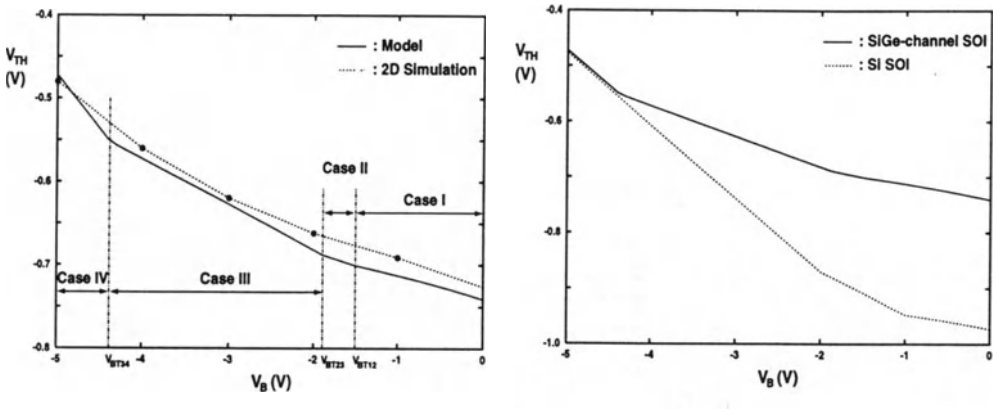


Figure 7.8: Threshold voltage versus back-gate bias of the SiGe-channel SOI PMOS device.

shown in the figure, four cases – Case I, II,III,IV can be identified. In each case, the slope of the threshold voltage curve with respect to the back gate bias is different. Fig. 7.8 also shows the difference between the SiGe-channel and the conventional SOI PMOS devices. When the back gate bias shifts toward the positive direction, the difference between the two devices gets larger. This can be understood by the equivalent capacitance models as shown in Fig. 7.9[10].

For the SiGe-channel PMOS device biased in Case I & II, the equivalent capacitance model as shown in Fig. 7.9(a), is composed of C_{ox1}, C_{cap}, C_{ge}, C_s and C_{ox2}, and C_{sub}. C_{sub} accounts for the depletion capacitance in the substrate. C_{cap}, C_{ge}, and C_s account for the capacitances of the silicon cap, the SiGe channel, and the silicon thin-film below the SiGe channel, respectively. Therefore, the threshold voltage slope can be expressed as the product of two terms: $\frac{\partial V_{TH}}{\partial \Psi_{sub}} = (\frac{\partial \Psi_{ch}}{\partial \Psi_{sub}} |_{\Psi_{ch}=\phi_F})(\frac{\partial \Psi_G}{\partial \Psi_{ch}} |_{\Psi_{ch}=\phi_F})$. As $V_B > -1.5V$ (Case I), the channel is located at the top of the SiGe channel, therefore, $\frac{\partial V_{TH}}{\partial \Psi_{sub}} = -\frac{(\frac{1}{C_{ox1}}+\frac{1}{C_{cap}})}{(\frac{1}{C_{ge}}+\frac{1}{C_s}+\frac{1}{C_{ox2}}+\frac{1}{C_{sub}})}$. For $-1.5V > V_B > -1.9V$ (Case II), the channel is located at the bottom of the SiGe channel, therefore, one obtains: $\frac{\partial V_{TH}}{\partial \Psi_{sub}} = -\frac{(\frac{1}{C_{ox1}}+\frac{1}{C_{cap}}+\frac{1}{C_{ge}})}{(\frac{1}{C_s}+\frac{1}{C_{ox2}}+\frac{1}{C_{sub}})}$. For the device operating in Case III & IV, as shown in Fig. 7.9(b), the equivalent capacitance model is without C_{sub}. Its threshold voltage slope is: $\frac{\partial V_{TH}}{\partial \Psi_{sub}} = (\frac{\partial \Psi_{ch}}{\partial \Psi_{sub}} |_{\Psi_{ch}=\phi_F})(\frac{\partial \Psi_G}{\partial \Psi_{ch}} |_{\Psi_{ch}=\phi_F})$. For $-4.4V < V_B < -1.9V$ (Case

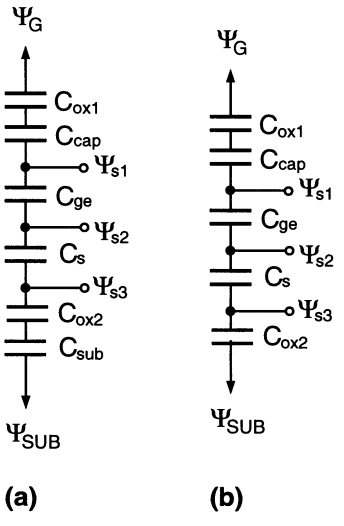


Figure 7.9: The equivalent capacitance model of the SiGe-channel SOI PMOS device.

III), the channel is located at the bottom of the SiGe channel and inversion exists at the substrate surface, therefore, $\frac{\partial V_{TH}}{\partial \Psi_{sub}} = -\frac{(\frac{1}{C_{ox1}}+\frac{1}{C_{cap}}+\frac{1}{C_{ge}})}{(\frac{1}{C_s}+\frac{1}{C_{ox2}})}$. For $V_B < -4.4V$ (Case IV), the channel is located at the top of the field oxide and inversion exists at the substrate surface, therefore, $\frac{\partial V_{TH}}{\partial \Psi_{sub}} = -\frac{(\frac{1}{C_{ox1}}+\frac{1}{C_{cap}}+\frac{1}{C_{ge}}+\frac{1}{C_s})}{(\frac{1}{C_{ox2}})}$. From the above analysis, the difference in the threshold voltage slope can be understood.

7.3 SOI Power Devices

High-voltage integrated circuits (HVIC's) have been gaining a lot of attention owing to their applications in telecommunication, display drivers, and electrostatic printers[14][15]. SOI technology for high-voltage MOS devices has been reported for its advantages in speed performance owing to smaller parasitic capacitances[14]. Owing to the buried oxide isolation structure, SOI structures are suitable for high-temperature operation. Therefore, SOI technology has been used to implement power devices. For an SOI LDMOS device as shown in Fig. 7.10, a silicon thin-film of 1.5μm has been used[16]. It has a 50μm long drift region with a silicon thin-film

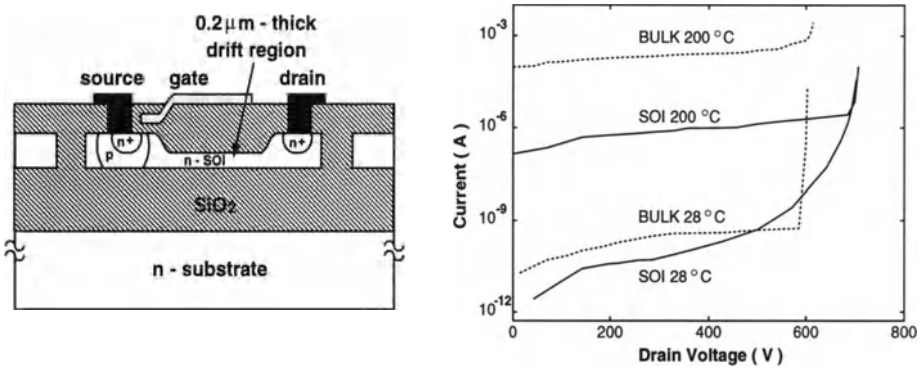


Figure 7.10: Cross section and leakage current of an SOI high-voltage LDMOS device.

thickness of 0.2μm, which is implemented using selective oxidation technique. Below the active region, there is a buried oxide of $3\mu\text{m} - 4\mu$m. The breakdown voltage of this device with a channel width of 8mm is 600-700V and its on-resistance is 19Ω at room temperature. Also shown in the figure is the leakage current versus drain voltage of the device. From this figure, the breakdown voltage of the SOI LDMOS device is much better than the bulk one. In addition, the leakage current sensitivity to the temperature of the SOI LDMOS device is much smaller than that of the bulk one owing to a less than 1.5μm silicon thin-film and the buried oxide isolation. Therefore, SOI LDMOS devices are more suitable for high-temperature operation.

Fig. 7.11 shows the drain current characteristics of an SOI LDMOS device with a drift region of 50μm, a silicon thin-film thickness of 0.2μm, a buried oxide of 1.2μm, and a device area of 0.3mm^2[17], measured at DC and after applying the bias for 2μs and 100μs. As for SOI MOS devices, self-heating is also noticeable in SOI LDMOS. The negative differential output resistance can also be seen at the high drain voltage regime. At a high drain voltage, carriers are travelling at the saturated velocity in the drift region. When the drain voltage is raised, power dissipation increases. Hence, the lattice temperature rises— the travelling velocity is degraded. As a result, the drain current drops. As shown in the figure, when the measurement is carried out in a shorter period of operation, the self-heating behavior is less. Fig. 7.12 shows the temperature rise versus time of SOI and bulk LDMOS devices following an application of a $90W/mm^2$, 100μs power pulse[17]. As

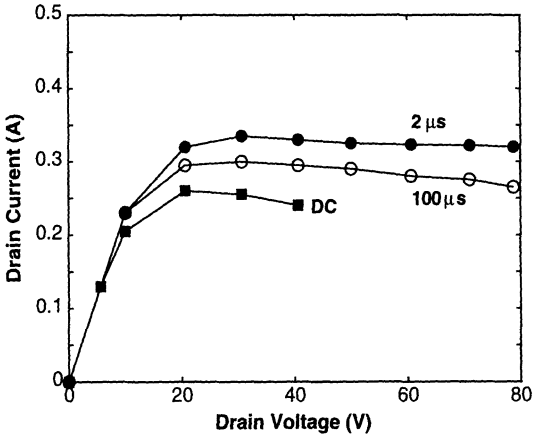


Figure 7.11: Drain current characteristics of an SOI LDMOS device with a drift region length of 50μm, a silicon thin-film thickness of 0.2μm, a buried oxide of 1.2μm, and a device area of 0.3mm^2, measured at DC, and after applying the bias for 2μs and 100μs.

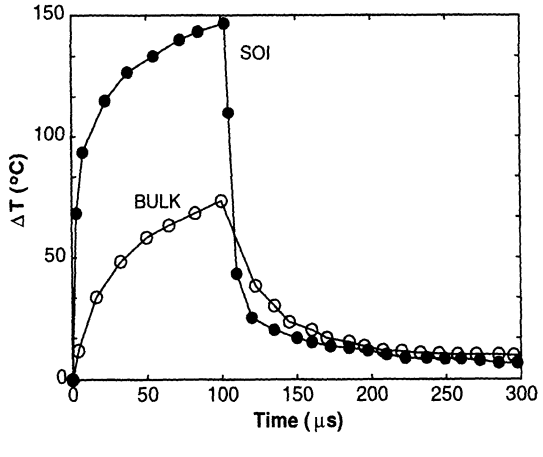
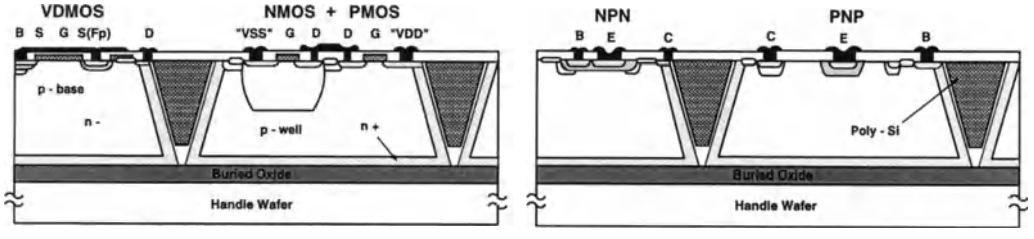


Figure 7.12: Temperature rise versus time of SOI and bulk LDMOS devices following an application of a $90W/mm^2$, 100μs power pulse.



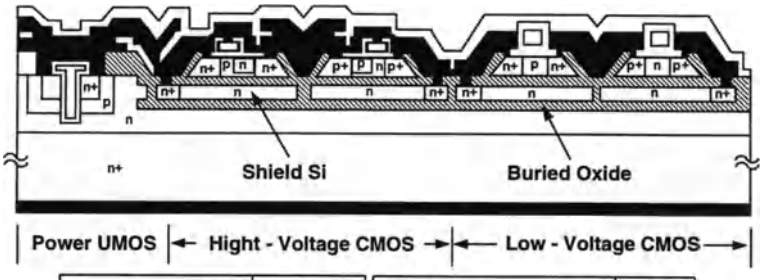
	VDMOS	NMOS	PMOS	NPN	PNP
Breakdown Voltage	150V	10V	15V	60V	75V
Threshold Voltage	1.4V	1.0V	- 1.0V		
On-resistance	$2\Omega \cdot mm^2$				
Gate/ base length	0.7 μm	2 μm	2 μm	1.5 μm	≥ 10 μm
Current gain at 100 μ A				80	80

Figure 7.13: Cross section of a merged SOI technology, which combines VDMOS, CMOS, and bipolar devices.

shown in the figure, due to the buried oxide, the temperature rise in the SOI device is much higher than that in the bulk device. In addition, when the pulse is over, the temperature in the SOI device drops to the final stable value much faster due to a much smaller thermal capacitance of the silicon thin-film.

Owing to the excellent isolation capability of the buried oxide structure, simultaneous integration of the power devices with CMOS control logic circuits becomes feasible. Fig.7.13 shows the cross section of an SOI technology, which combines VDMOS, CMOS and bipolar devices[18]. As shown in the figure, it has a buried oxide of 1μm, a silicon thin-film of 15μm, a front gate oxide of 400Å, and a CMOS gate length of 2μm. An isolating V-Groove surrounded by an n^+ sidewall has been adopted to provide a current path.

The previous merged SOI technology is based on a thick silicon film ($t_{si} = 15\mu m$). Here a merged SOI technology using a silicon thin-film is described. Fig. 7.14 shows the cross section of an intelligent power LSI SOI technology with double buried-oxide layers. All components are individually and completely isolated by the oxide layers[19]. Due to the 0.4μm silicon thin-film, a structure with double buried oxide layers separated by another silicon thin-film has been used to enhance the shielding



Parameters (Power UMOS)	Values
U - Groove Opening	1.5μm
U - Groove Layout Pitch	7.5μm
Gate Oxide Thickness	70nm
Substrate Thickness	520μm
Source Junction Depth	0.94μm
Body Junction Depth	3.4μm
Drain - Buffer Thickness	6.6μm

Parameter (CMOS)	Values
Gate Oxide Thickness	50nm
Gate Length (Low - Length)	2μm
Gate Length (Hight - Length)	5μm
Offset Length	5μm
Active Si Thickness	0.4μm
Upper Buried - Oxide Thickness	0.46μm
Lower Buried - Oxide Thickness	0.44μm

Figure 7.14: Cross section of an intelligent power LSI SOI technology with double buried-oxide layers. All components are individually and completely isolated by the oxide layers.

capability. The double buried-oxide layer structure is formed by an oxygen implant with an epitaxial growth, followed by another oxygen implant. The power DMOS device in this technology can sustain up to 60V. In addition, 5V and 12V CMOS devices are also available. The 5V CMOS devices are designed for controlling the 12V CMOS devices. The 12V CMOS devices are used to control the 60V DMOS power devices.

For a power DMOS device built by SOI technology, the back gate bias effect on the power DMOS device cannot be overlooked. Fig.7.15 shows the cross section and IV characteristics of an N-channel LDMOS device with a front gate oxide of 400Å, a buried oxide of 1.2μm, a silicon thin-film of 1μm, an aspect ratio of 200μm/0.4μm, and a drift region of 15μm[20]. As shown in the figure, at a more positive back gate bias, the drain current becomes larger since the resistance of the n-drift region becomes smaller.

For a bulk DMOS device, quasi-saturation behavior is important [15]. As described before, for an ultra-thin SOI MOS device, the back gate bias effect on its device performance is complicated. In the final portion of this section, the back gate

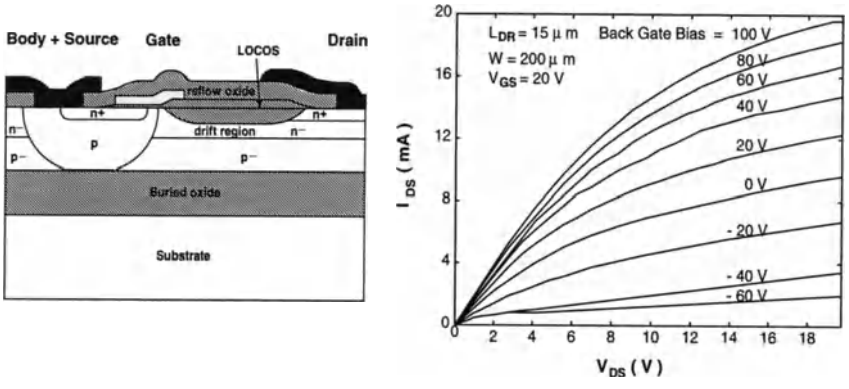


Figure 7.15: Cross section and IV characteristics of an N-channel LDMOS device with a front gate oxide of 400Å, a buried oxide of 1.2μm, a silicon thin-film of 1μm, an aspect ratio of 200μm/0.4μm, and a drift region of 15μm.

bias effect on the quasi-saturation behavior in a high-voltage SOI MOSFET[21] is described. Fig. 7.16 shows the cross section and IV characteristics of the high-voltage SOI DMOS device used in this study [21]. The high-voltage SOI DMOS device has an n+ polysilicon gate and a front gate oxide of 500Å and a 1μm silicon thin-film above an oxide insulator of 1.2μm. Below the oxide insulator, the p-type substrate is doped with 10^{16}cm^{-3}. There is an n- region of $40\mu m$ with a doping density of $10^{16}cm^{-3}$. As shown in the figure, when V_{GS} is greater than a certain value, the drain current stays almost unchanged regardless of V_{GS}. For a back gate bias of $0V$, as V_{DS} increases, the drain current at quasi-saturation increases. On the other hand, for a negative back gate bias of $-40V$, the drain current at quasi-saturation stays almost unchanged regardless of V_{DS}. Different from the bulk vertical DMOS device, the quasi-saturation behavior of the high-voltage SOI MOS device is also influenced by the back gate bias. Figs. 7.17 show the 2D electron concentration contours in the silicon thin-film region of the high-voltage SOI MOSFET biased at quasi-saturation ($V_{DS} = 40V$, $V_{GS} = 20V$) with $V_{BS} = 0V$ and $-40V$ from $10^{14}cm^{-3}$ to $10^{16}cm^{-3}$ at an interval of $10^{0.4}cm^{-3}$[21]. As in the bulk vertical DMOS device, the drain current of a high-voltage SOI MOSFET biased at quasi-saturation is determined by the current conduction in the n- region. For a back gate bias of $0V$, most of the n- region is for current conduction. For a back gate bias of $-40V$, the depletion edge moves upward. A more negative back gate bias leads to a smaller channel depth in the n- region. For $V_{BS} = 0V$, the shape of the depletion edge is linear. For $V_{BS} = -40V$, the shape of it is two-region piece-wise linear due to the hole inversion above the

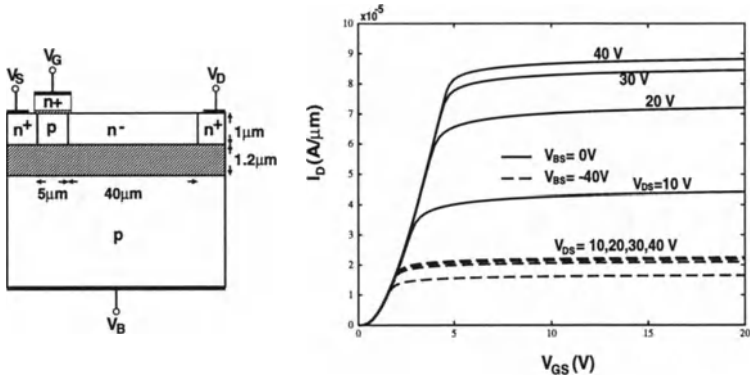


Figure 7.16: Cross section and IV characteristics of the high-voltage SOI DMOS device.

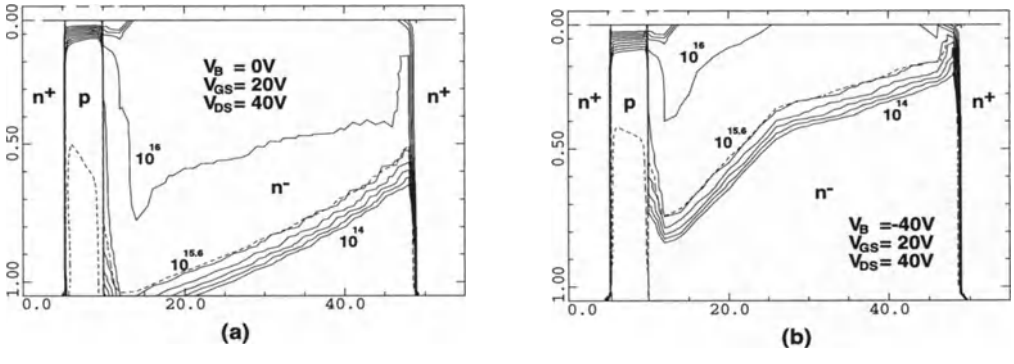


Figure 7.17: 2D electron concentration contours in the high-voltage SOI MOSFET biased at quasi-saturation ($V_{DS} = 40V$, $V_{GS} = 20V$) (a) $V_{BS} = 0V$ and (b) $-40V$.

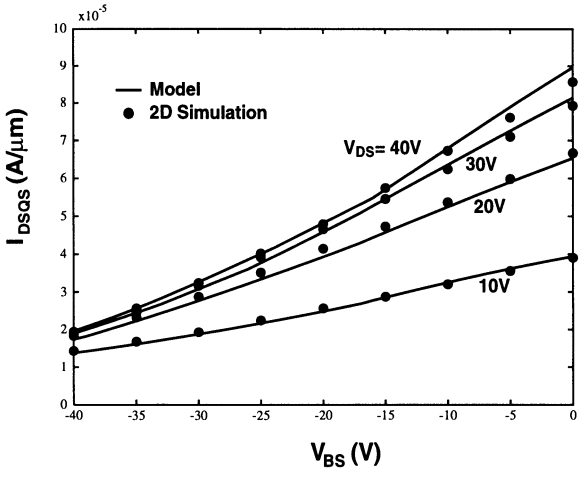


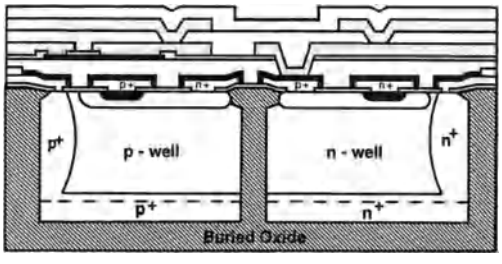
Figure 7.18: The drain current versus V_{BS} curves for the high-voltage SOI MOSFET biased at quasi-saturation ($V_{DS} = 10V - 40V$) based on the analytical model and the 2D simulation results.

field oxide at $V_{BS} = -40V$.

Fig. 7.18 shows the drain current versus V_{BS} curves for the high-voltage SOI MOSFET biased at quasi-saturation ($V_{DS} = 10V - 40V$)[21]. A more negative back gate bias makes the drain current at quasi-saturation smaller. In addition, a higher drain voltage leads to a higher drain current at quasi-saturation. However, the increase in the drain current is not linearly proportional to that in the drain voltage.

7.4 SOI BJT & BiCMOS

Due to an excellent α-particle immunity and low parasitic capacitances, SOI technology has also been used to implement BJTs. Fig. 7.19 shows the cross section of an SOI bipolar technology[22]. Except the buried oxide, LOCOS, and the trench isolation, it's identical to a bulk BJT technology. Each well has its own active BJT region above the buried layer and epi-layer. As shown in the figure, due to the buried oxide structure, the parasitic capacitance at the collector node of the SOI BJTs is much smaller than that of the bulk BJTs.



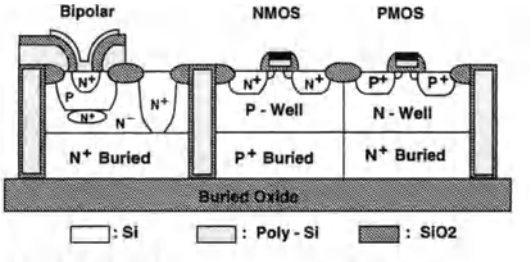
Parameter	NPN	PNP
Current gain	120	60
Early Voltage [V]	300	50
BVceo [V]	>35	>35
BVebo [V]	>4.0	>5.0
Re [Ω]	<1.5	<2.0
Rc [Ω]	70	120
Cje [fF]	160	86
Cjc [fF]	87	197
Cjs [fF]	65	65
f_t [GHz]	3	3
Vbe matching [μV]	< ± 300	< ± 300

Figure 7.19: Cross section of an SOI bipolar technology.

In addition to BJT, SOI technology has also been used to integrate BiCMOS devices. Fig. 7.20 shows the cross section of a 0.6μm SOI BiCMOS technology[23] using LOCOS and trench isolation. In this SOI BiCMOS technology, the structure of the CMOS devices is similar to that in bulk twin-tub technology. The bipolar devices benefit from the SOI structure— the parasitic capacitances can be much smaller as compared to the bulk devices.

Fig. 7.21 shows the cross section of a vertical SOI bipolar transistor [24] using mesa-isolation. The basic structure of this bipolar transistor is similar to that of the bulk one except the mesa-isolation and the buried oxide structures. Owing to the mesa-isolation structure, the processing sequence is less complicated. In addition, the device density can be higher.

In addition to the bipolar device, mesa isolation can also provide advantages for BiCMOS devices. Fig. 7.22 shows the cross section of a BiCMOS technology using mesa isolation[25]. As shown in the figure, the requirements on the thicknesses of the silicon thin-films for the bipolar and CMOS devices are different. For the bipolar device, the thickness of the silicon thin-film is 1.0μm. For CMOS devices, it is 0.3μm. At the beginning of the fabrication process, the silicon thin-film of the CMOS device region should be etched off more. Due to the difference in the silicon thin-film thickness between the bipolar and CMOS device regions, planarization may be much more difficult as compared to other planar processing technologies. As



Bipolar Transistor

Emitter size	0.5 x 20 μm^2
hFE	100
fT(Vce=1V)	27 GHz
BVceo	6V
BVcbo	18V
BVebo	4.7V
CTE	6fF
CTC	3.5fF
CTS	8fF
rbb'	250Ω

CMOS Devices

NMOS gate length Leff	0.60 μm
PMOS gate length Leff	0.62 μm
Gate oxide thickness tox	12 nm
NMOS Vth	0.45 V
NMOS Ids (Vd=Vds=3.3V)	0.30 mA/μm
PMOS Vth	- 0.55V
PMOS Ids (Vd=Vds=3.3V)	- 0.15 mA/μm
Memory cell size	58 μm^2

Figure 7.20: Cross section of a 0.6μm SOI BiCMOS technology.

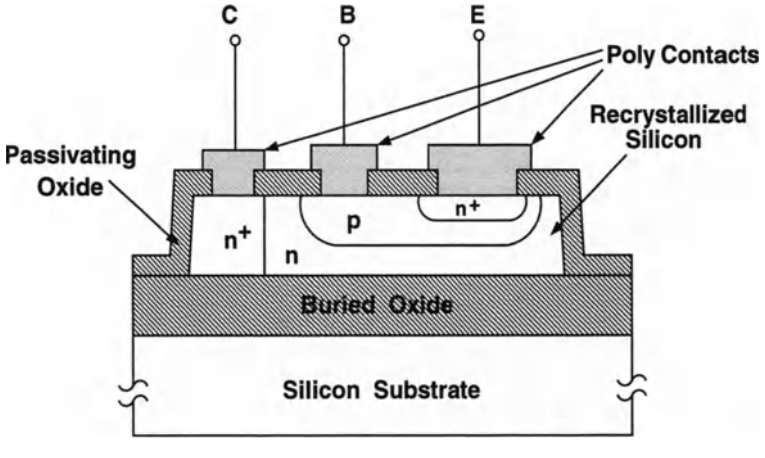


Figure 7.21: Cross section of a vertical SOI bipolar transistor.

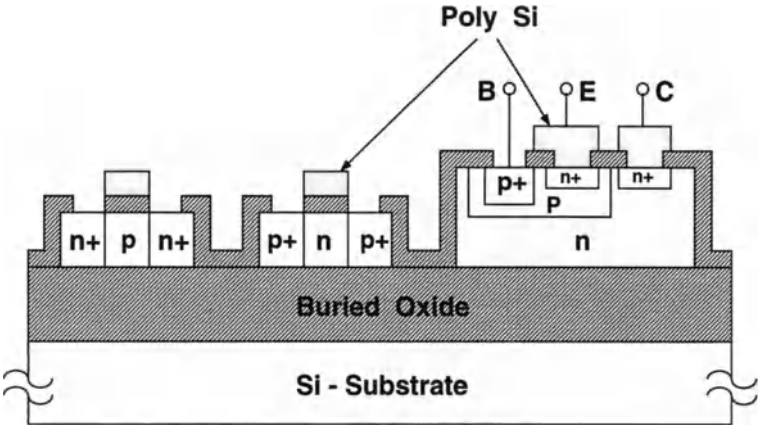


Figure 7.22: Cross section of a BiCMOS technology.

for the trench-isolated SOI BiCMOS technology, this mesa-isolated SOI BiCMOS also provides advantages in low parasitic capacitances.

Along with the development with the ultra-thin-film SOI technology, lateral bipolar devices have been receiving attention. Fig. 7.23 shows the cross section of the lateral bipolar device[26]. As shown in the figure, a silicon thin-film of 0.15μm is built on a buried oxide of 0.225μm. The base profile and the base contact of this lateral SOI bipolar device are based on a p^+ polysilicon layer and oxide sidewall. As a result, a great deal of improvement can be found for the parasitic capacitances of the base and the emitter in addition to the collector. The difficulties of this lateral SOI bipolar device is on forming the base profile and the base contact—if not properly done, the leakage between the base-emitter junction and the base resistance may not be acceptable.

Fig. 7.24 shows the cross section of an SOI BiCMOS technology with lateral bipolar devices[27] with a front gate oxide of 105Å, a buried oxide of 4000Å, a silicon thin-film of 1000Å, and a channel length of 0.5μm. As shown in the figure, lateral bipolar devices are made directly on the top of the silicon thin-film. As a result, the bipolar devices can be easily integrated with the CMOS devices. The base profile is determined by the sidewall oxide spacer, which is also used for the LDD structure in the CMOS devices, during the fabrication of the bipolar device.

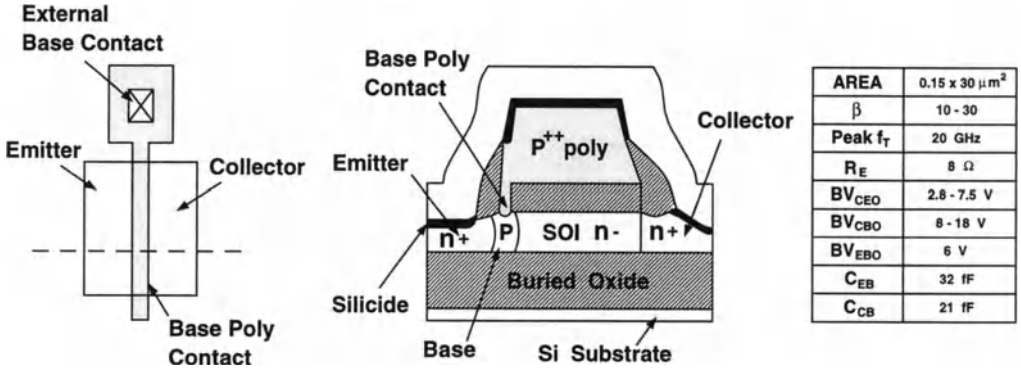


Figure 7.23: Cross section of the lateral SOI bipolar device.

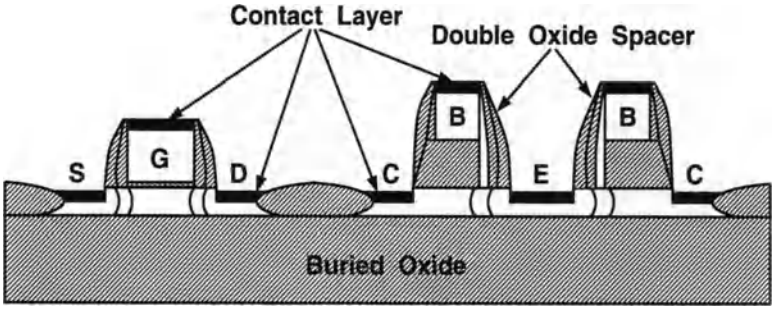


Figure 7.24: Cross section of an SOI BiCMOS technology with lateral bipolar devices with a front gate oxide of 105Å, a buried oxide of 4000Å, a silicon thin-film of 1000Å, and a channel length of 0.5μm.

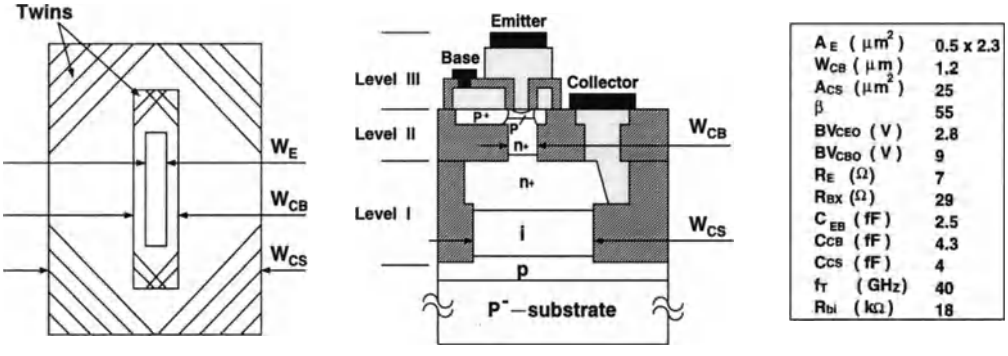


Figure 7.25: Cross section of a partial-SOI BJT technology using the sequentially planarized interlevel isolation technology (SPIRIT) structure.

Although the bipolar devices built by SOI technology can have smaller parasitic capacitances, which lead to a higher speed performance, self-heating problems can be serious. In order to optimize the tradeoffs between parasitic capacitances and self-heating, a partial-SOI structure, which is based on the sequentially planarized inter-level isolation technology (SPIRIT) has been used to build the double-poly self-aligned bipolar devices[28] as shown in Fig. 7.25, where the emitter, the base, and most of the collector area are surrounded by oxide. Under some portion of the collector, there is an opening in the oxide layer, which is used to help expedite heat dissipation. By using this partial-SOI structure, the advantages of the low parasitic capacitances can be maintained. However, the partially-SOI BJT technology needs several times of the selective epitaxial growth and oxide deposition during the process.

The vertical bipolar device built by the partial-SOI technology is also suitable for integration in the BiCMOS structure. Fig. 7.26 shows the cross section of the partial-SOI BiCMOS technology[29]. As shown in the figure, CMOS devices are at the top of the epi-layer, which has a thickness of less than 0.2μm. Only the bipolar devices, which dissipate more heat, are using the partial-SOI structure. In contrast, CMOS devices are still using the full-SOI structure.

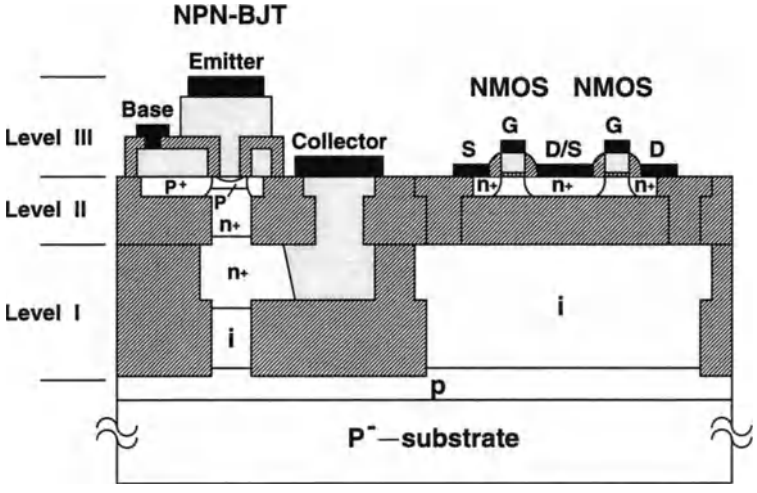


Figure 7.26: Cross section of the partial-SOI BiCMOS technology.

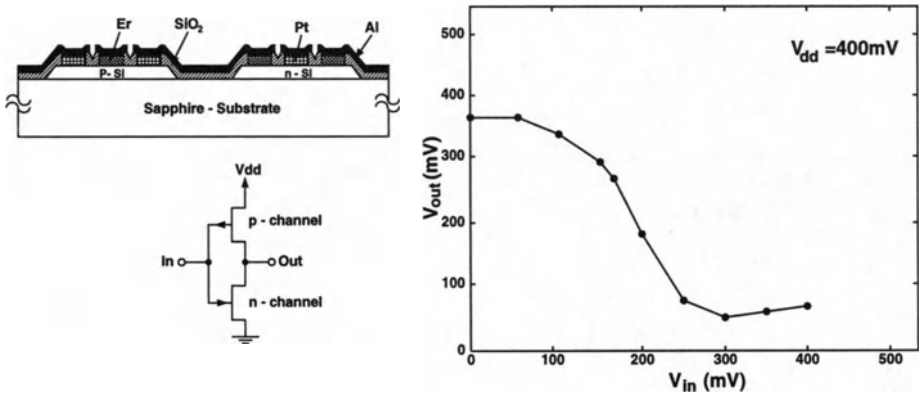


Figure 7.27: Cross section of complementary MESFET's on SOS.

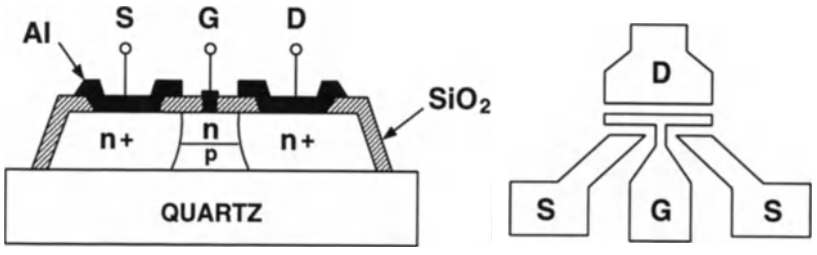


Figure 7.28: Si-on-quartz microwave MESFET has a gate length of 1.4μm and a channel thickness of 0.15μm.

7.5 SOI MESFET & JFET

Since there is no front oxide layer, MESFET's have better radiation hardness than MOSFET's. MESFET's have been integrated using SOI technology. Fig. 7.27 shows the cross section of complementary MESFET's on SOS[30]. For the n-type MESFET's, Pt has been used for the gate and Er has been used for the source and the drain. For p-type MESFET's, they are reverse. For the gate, it is Er. For the source/drain, it is Pt. From this figure, the device structure of SOI MESFET's is much simpler than that of the SOI MOSFET's. Therefore, the processing technology is also easier. The structure of an inverter circuit using MESFET's is similar to that using MOSFET's. However, in order to avoid a large current when the gate-channel diode is turned on, the supply voltage is limited to below 0.5V. In addition, no full-swing can be reached for the SOI MESFET inverter. As a result, noise immunity can be worse as compared to the MOS one.

In addition to applications for the digital logic circuits, SOI MESFETs have also been used for microwave circuits. As shown in Fig.7.28, a Si-on-quartz microwave MESFET has a gate length of 1.4μm, a channel thickness of 0.15μm[31]. In addition to MESFETs, JFETs can also be integrated on SOI. Fig. 7.29 shows the cross section of the SOI complementary JFET technology[32], which has a gate length of 4μm. The channel region is formed by ion implantation. Fig. 7.30 shows the cross section of a p-channel JFET on SIMOX substrate[33]. As shown in the figure, double gates at the top and the bottom of the channel region are used to improve the control capability. During the fabrication process, the bottom gates are formed by implanting to the specified silicon thin-film region, followed by an epi-layer formation for the channel region and the top gate.

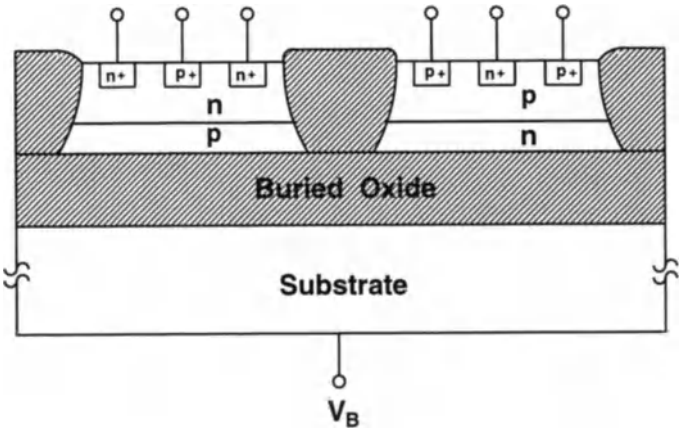


Figure 7.29: Cross section of the SOI complementary JFET technology.

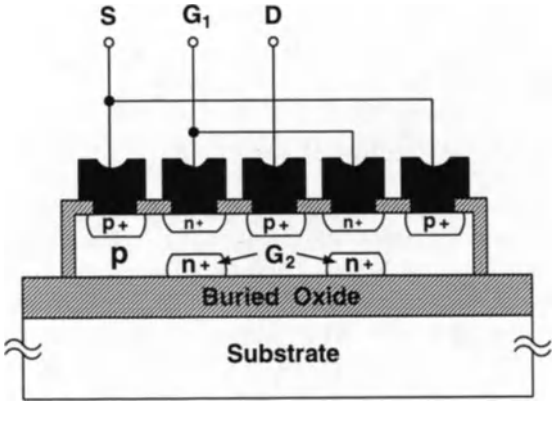


Figure 7.30: Cross section of the p-channel JFET on SIMOX substrate.

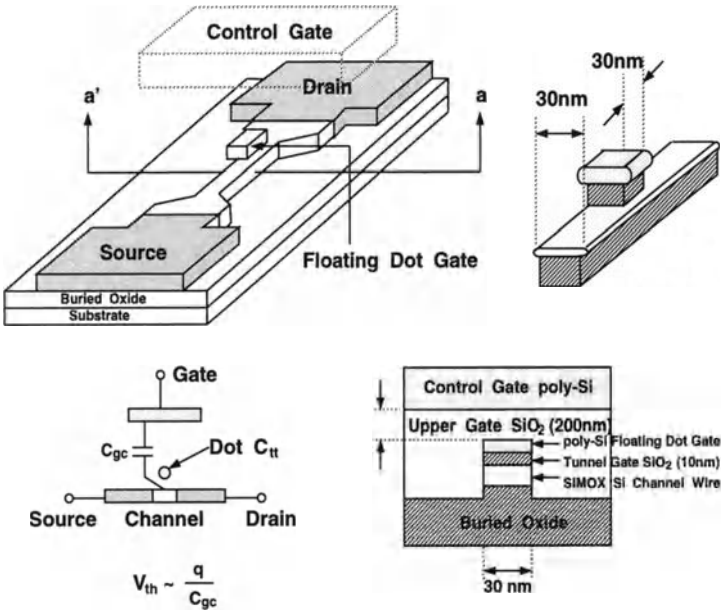


Figure 7.31: Cross section of a silicon single-electron transistor (SET) memory with the self-aligned floating dot gate.

7.6 Single-Electron Transistor(SET)

Nowadays, deep-submicron MOS devices with a channel length/width of much smaller than 1000Å has been reported. Along with down scaling of MOS devices, the supply voltage needs to decrease too. As a result, the number of conducting electrons in a down-scaled deep-submicron NMOS device decreases quickly. When the size of a very deep-submicron MOS device is shrunk further, what the limit is has been investigated. In a very small NMOS device, under the requirement on low power for VLSI, single electron transistors (SET), which mean that only one electron in the conducting channel, may be the limit in down scaling CMOS technology.

The so-called single-electron transistors (SET) are referred to the devices, which can control the transfer of a single electron. Fig. 7.31 shows the cross section of a single-electron transistor built on SIMOX substrate [34]. The key structure is the floating dot gate, which is below the control gate. The floating dot gate needs to be very small such that a very small capacitance of 3.3aF(a = 10^{-18}) to restrict the

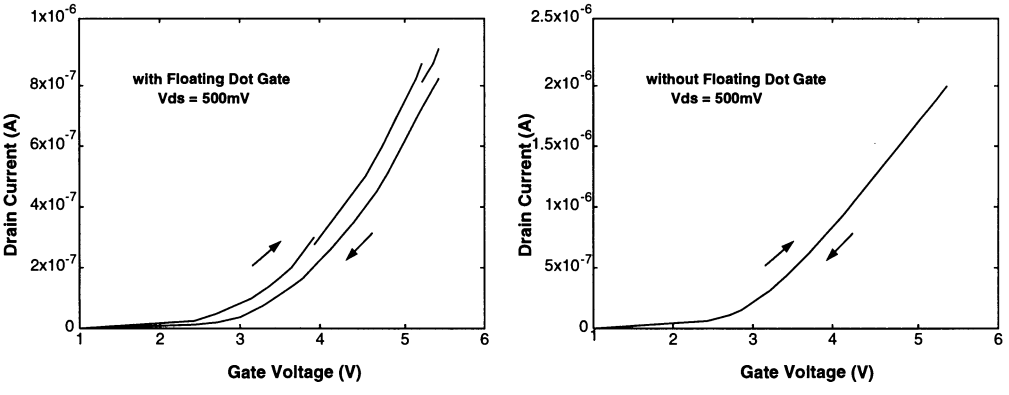


Figure 7.32: Drain current versus control gate voltage at room temperature for the single-electron FET with the floating dot gate.

quantity of the accommodated electrons. Fig. 7.32 shows the drain current versus control gate voltage at room temperature for the single-electron FET with the floating dot gate [34]. As shown in the figure, from the measured drain current curve, there exists a discontinuous transition point, which is due to the 0.1V threshold voltage shift caused by the trapping of a single electron at the floating dot gate. The trapped electron stays in the floating dot gate. As a result, there is a hysteresis in the drain current characteristics. Fig. 7.33 shows the energy diagram and the drain current characteristics of the single-electron memory device[35]. As shown in the figure, when the control gate voltage is positive enough such that a single electron is induced to move from the channel to the floating dot gate by tunneling through the oxide, the potential of the floating dot gate will change to prevent more electrons from entering—-this is Coulomb blockade effect. Therefore, the trapped electron changes the threshold voltage of the device substantially. As a result, the drain current curve is shifted. From this reasoning, in the single electron FET, the capacitance of the storage floating dot gate needs to be very small to produce a sufficient change in the potential, which can blockade the transfer of other electrons. From considering the electrostatic energy and the thermal energy of an electron, the capacitance of the floating dot gate needs to be as small as $q^2/2kT$ to guarantee the operation of a single electron at room temperature.

Fig. 7.34 shows the cross section of another silicon single-electron transistor on SOI SIMOX substrate[36]. The silicon island is surrounded by the gate electrode, the substrate silicon across the oxide layer, and the source/drain region. The final

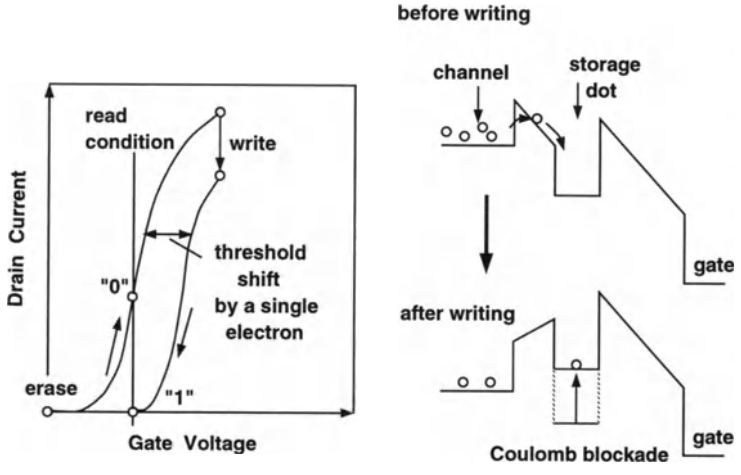


Figure 7.33: Energy diagram and drain current characteristics of the single-electron memory device.

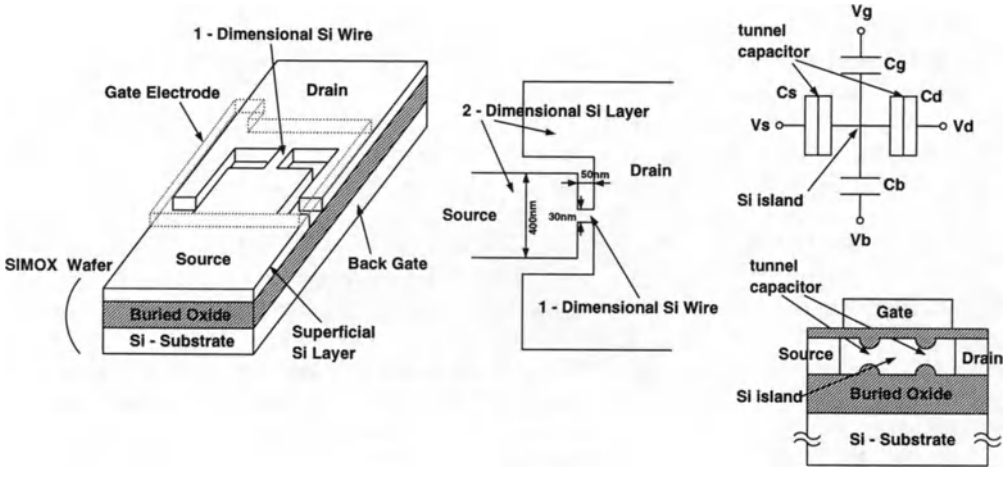


Figure 7.34: Cross section of a silicon single-electron transistor on SOI SIMOX substrate. The silicon island is surrounded by the gate electrode, the substrate silicon across the oxide layer, and the source/drain region.

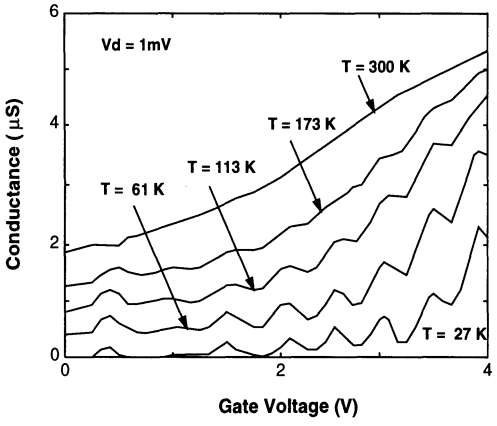


Figure 7.35: Conductance oscillation as a function of the gate voltage when the temperature is varied.

dimensions of the silicon island, which are defined by electron beam lithography and thermal oxidation, are several nm to generate a capacitance of $2aF$ such that Coulomb blockade effect can occur. Fig. 7.35 shows the conductance oscillation as a function of the gate voltage when the temperature is varied[36]. As shown in the figure, the conductance oscillation behavior is due to the Coulomb blockade effect from the silicon island, which is a strong evidence of the effect from a single-electron device. Also shown in the figure, when the temperature is lowered, the quantum effect is more noticeable.

7.7 Amorphous TFT

Hydrogenated amorphous thin-film transistors (a-Si:H TFT) built on an insulator, which can be regarded as an SOI structure, have been used for active matrix LCDs, complex arrays of electronic devices and large-area microelectronics using amorphous material [37]. Using a-Si:H TFTs, digital control switches can be integrated on-chip with complex arrays of a-Si:H LCD's [38]-[43] to reduce off-chip interconnects required. Fig. 7.36 shows the process sequence of an amorphous TFT technology[44]. As shown in the figure, in the amorphous TFT process, on the glass substrate, a layer of Cr (chromium) is deposited by sputtering. Then the gate electrode of the amorphous TFT is done by patterning the Cr layer using photolithography and etching. A layer of 3000Å SiNx, followed by a layer of 2000Å i-a-Si:H and a layer of 500Å

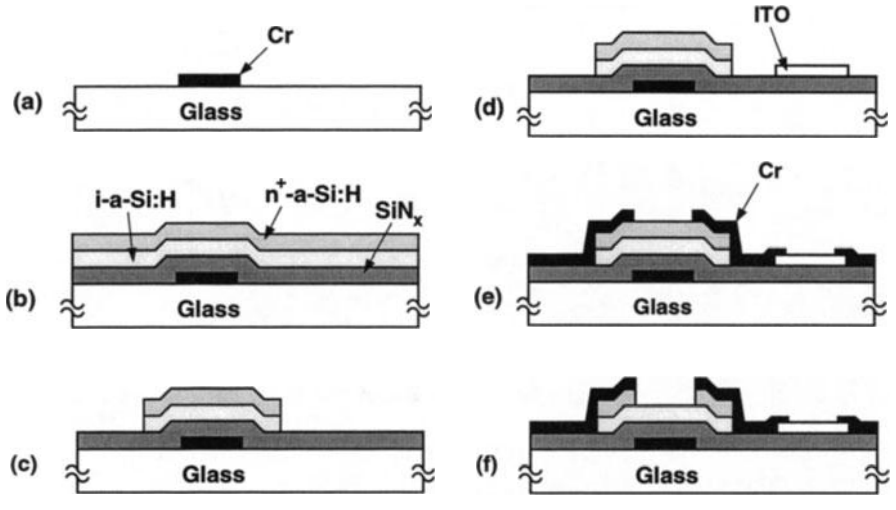


Figure 7.36: Process sequence of an amorphous TFT technology.

n^+ a-Si:H is deposited by CVD. Then the deposited i-a-Si:H and n^+ a-Si:H layers outside the TFT region are removed by photography and etching. An indium tin oxide (ITO) layer is deposited and patterned to form the transparent electrode for the TFT. After covering the whole wafer with Cr, the Cr above the TFT channel region and most of the ITO region is etched off. After etching off the n^+ a-Si layer above the TFT channel region, the process sequence is accomplished. Fig. 7.37 shows the cross section of an a-Si TFT/LCD pixel with the driving transient waveforms[45]. As shown in the figure, the a-Si TFT is located between two transparent display electrodes made of ITO. The switching of the amorphous TFT controls the charge and the discharge of the common electrodes and the pixel electrode. When the TFT turns on, the electric field between the two electrodes changes the polarization of light in the LCD pixel. As a result, the transmission of light through the pixel can be controlled.

Fig. 7.38 shows the cross section and IV characteristics of a thin-channel a-Si:H TFT[46]. As shown in the figure, an amorphous silicon thin-film is on an insulator. Below the insulator, there is a gate electrode. Source and drain contacts are at the top of the amorphous silicon thin-film. Under the source/drain electrodes, an N^+ implant to the amorphous silicon thin-film region has been used for the source/drain region. The thickness of the amorphous thin-film strongly affects the performance.

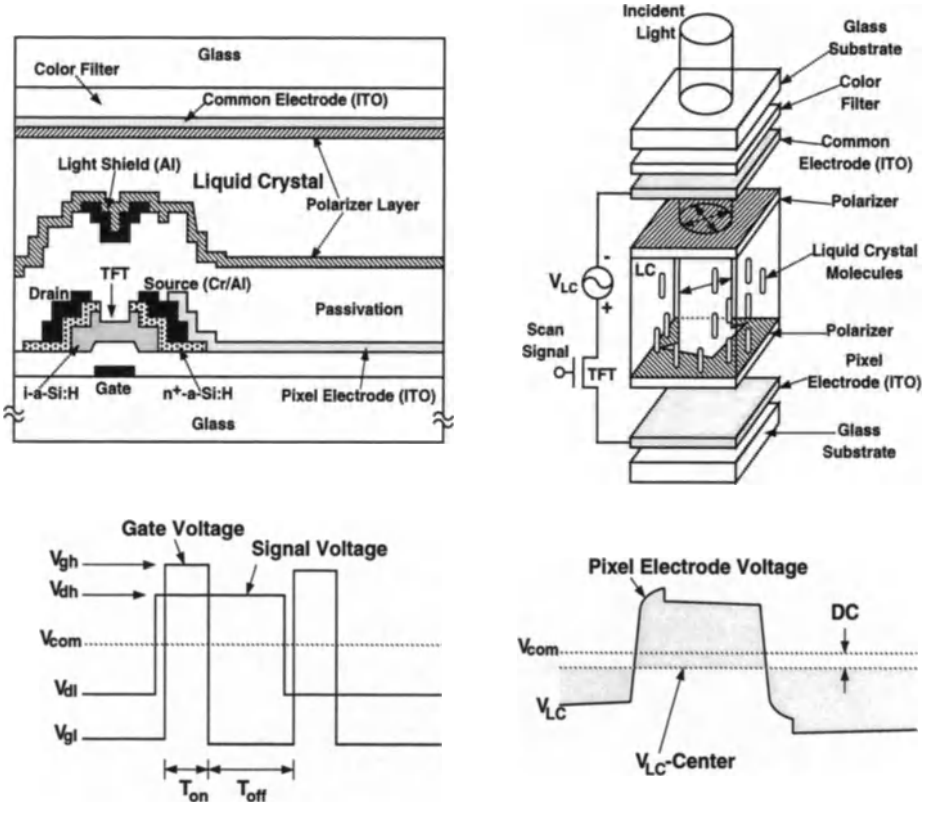


Figure 7.37: Cross section of an a-Si TFT/LCD pixel with the driving transient waveforms.

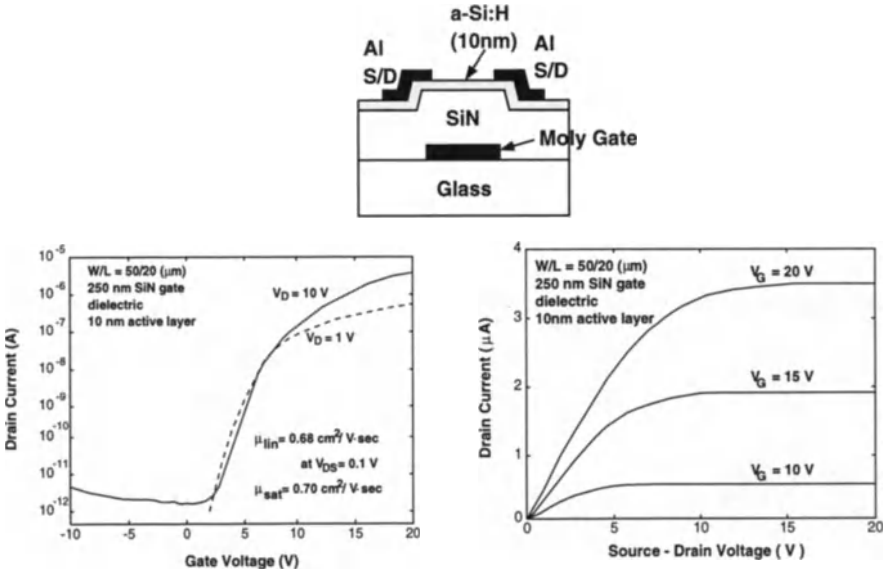


Figure 7.38: Cross section and IV characteristics of a thin-channel a-Si:H TFT.

When the channel of an a-Si:H TFT is thinner, the throughput of mass production of it will be better. In addition, the drain current in the linear region can be larger. When the thickness of the a-Si:H is thin enough (100Å), the 2D effect between the source/drain contact and the channel region can be reduced. Furthermore, with a very thin amorphous silicon thin-film carriers can move from channel to the metal contact via tunneling— doping the source/drain region can be skipped.

Analysis of a-Si:H TFTs have been reported [47]-[56]. Due to the complicated distribution of localized acceptor states in the energy gap of amorphous silicon, analytical models are difficult to derive [47][57]-[60]. The analytical models of the free and trapped charges in the channel of the a-Si:H TFT are difficult to obtain. In an analytical saturation region model based on an 'n-i-n diode' approach, in the region after pinchoff, it is regarded as an intrinsic region [53][54][61]. A capacitance model for a-Si:H TFTs based on a field-dependent mobility has been reported[54][55]. A capacitance model using numerical iteration for a-Si:H TFTS has been derived[56]. In the next portion of this section, analysis of the behaviors of a-Si:H TFTs is described[62].

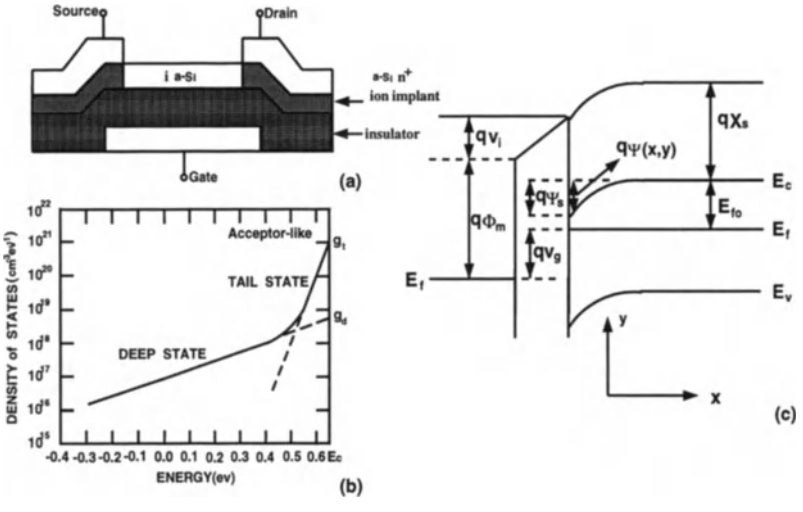


Figure 7.39: (a) The a-Si:H TFT under study. (b) Distribution of localized acceptor states in the energy gap of amorphous silicon. (c) Band diagram of the a-Si:H TFT.

Fig. 7.39(a) shows the cross section of a typical a-Si:H TFT. The majority of the induced charges in the channel is trapped in the localized states [62]. As a result, the density of free mobile carriers in the conduction band is small and the field-related mobility is small as compared to the single crystal MOS devices. Fig. 7.39(b) shows the distribution of localized acceptor states in the energy gap of amorphous silicon. The localized acceptor-like states, which are important for the n-channel device operation, can be roughly divided into two groups: deep localized acceptor states and tail localized acceptor states. The distribution of localized acceptor states ($g(E)$) can be expressed as:

$$g(E) = g_d e^{\frac{E-E_c}{kT_d}} + g_t e^{\frac{E-E_c}{kT_t}}, \tag{7.15}$$

where g_d and g_t are the deep states density and the tail states density at the conduction band edge, respectively. T_d and T_t are the characteristic temperatures of the deep states and tail states, respectively. E_c is the conduction band level. The localized trapped charge density in a-Si:H can be expressed as [63]:

$$n_{loc} = \int_{E_v}^{E_c} g(E)f(E)dE, \tag{7.16}$$

where $f(E)$ is the Fermi-Dirac occupation function, which can be approximated by

$$\begin{cases} f(E) = 1 - e^{\frac{E-E_{fn}}{kT}}, & E_v < E < E_{fn}, \\ f(E) = e^{\frac{-(E-E_{fn})}{kT}}, & E_{fn} \leq E < E_c, \end{cases} \tag{7.17}$$

where E_v is the valence band level, k is the Boltzmann constant, and T is the temperature in Kelvin. Using the Boltzmann distribution, the free electron density in the conduction band is:

$$n_{free} = N_c e^{\frac{E_{fn}-E_c}{kT}}, \tag{7.18}$$

where N_c is the effective density of states in the a-Si, and E_{fn} is the electron quasi-Fermi level. From Eqs.(7.15)&(7.16), the density of localized trapped charge is expressed as:

$$n_{loc} = \int_{E_v}^{E_{fn}} (1 - e^{\frac{E-E_{fn}}{kT}})(g_d e^{\frac{E-E_c}{kT_d}} + g_t e^{\frac{E-E_c}{kT_t}})dE + \int_{E_{fn}}^{E_c} \frac{g_d e^{\frac{E-E_c}{kT_d}} + g_t e^{\frac{E-E_c}{kT_t}}}{e^{\frac{E-E_{fn}}{kT}}} dE. \tag{7.19}$$

Using the relationship: $E_{fn} - E_c = q\Psi - E_{fo}$, where E_{fo} is the difference between E_c and the Fermi level in the bulk, as indicated in Fig. 7.39(c), Eq. (7.19) is rewritten as:

$$\begin{aligned} n_{loc} &= (g_d kT_d - \frac{g_d}{(\frac{1}{kT} + \frac{1}{kT_d})} + \frac{g_d}{(\frac{1}{kT} - \frac{1}{kT_d})}) e^{\frac{q\Psi - E_{fo}}{kT_d}} \\ &+ (g_t kT_t - \frac{g_t}{(\frac{1}{kT} + \frac{1}{kT_t})} - \frac{g_t}{(\frac{1}{kT_t} - \frac{1}{kT})}) e^{\frac{q\Psi - E_{fo}}{kT_t}} + (g_t \frac{1}{(\frac{1}{kT_t} - \frac{1}{kT})} - \frac{g_d}{(\frac{1}{kT} - \frac{1}{kT_d})}) e^{\frac{q\Psi - E_{fo}}{kT}}. \end{aligned} \tag{7.20}$$

Eq. (7.21) is the analytical model for computing the density of localized trapped charges in the a-Si:H TFT.

Applying Poisson's equation in the a-Si:H TFT, one obtains:

$$\frac{d^2\Psi}{dx^2} = -\frac{dE}{dx} = \frac{q}{\epsilon}(n_{loc} + n_{free}), \tag{7.21}$$

where E is the electric field in the vertical direction. Using the relationship: $2\frac{d\Psi}{dx}(\frac{d^2\Psi}{dx^2}) = \frac{d}{dx}(\frac{d\Psi}{dx})^2$, from Eqs. (7.18)(7.21)(7.21), the electric field is expressed as:

$$E(\Psi) = \sqrt{\frac{2}{\epsilon}(kT_d n_A e^{\frac{q\Psi - E_{fo}}{kT_d}} + kT_t n_B e^{\frac{q\Psi - E_{fo}}{kT_t}} + kT n_C e^{\frac{q\Psi - E_{fo}}{kT}})}, \tag{7.22}$$

where $n_A = g_d kT_d - \frac{g_d}{(\frac{1}{kT}+\frac{1}{kT_d})} + \frac{g_d}{(\frac{1}{kT}-\frac{1}{kT_d})}$, $n_B = g_t kT_t - \frac{g_t}{(\frac{1}{kT_t}+\frac{1}{kT})} - \frac{g_t}{(\frac{1}{kT_t}-\frac{1}{kT})}$, and $n_C = g_d \frac{1}{(\frac{1}{kT_d}-\frac{1}{kT})} + g_t \frac{1}{(\frac{1}{kT_t}-\frac{1}{kT})} + N_c$. Integrating the free carrier density as shown in Eq. (7.18) in the vertical direction of the a-Si:H TFT from the oxide/a-Si interface ($x = 0$) to the end of the channel in the a-Si thin film ($x = t_i$), total free carriers in the a-Si:H TFT are:

$$N_{free} = \int_o^{t_i} N_c e^{\frac{q\Psi - E_{fo}}{kT}} dx, \tag{7.23}$$

Using the relationship: $dx = -\frac{d\Psi}{E(\Psi)}$, Eq. (7.23) becomes:

$$N_{free} = \int_o^{\Psi_s} \frac{N_c e^{\frac{q\Psi - E_{fo}}{kT}}}{E(\Psi)} d\Psi. \tag{7.24}$$

Define an "effective temperature"as:

$$T_{ef}(\Psi) = \frac{q\Psi - E_{fo}}{kln\frac{E(\Psi)}{A}}, \tag{7.25}$$

where $A = \sqrt{\frac{2}{\epsilon}(kT_d n_A + kT_t n_B + kT n_C)}$. Note that in Eq. (7.25), no surface states have been considered. If surface states are considered, Eqs. (7.21)(7.22)&(7.25) will be with surface state terms. Using the effective temperature as expressed in Eq. (7.25), Eq. (7.24) becomes:

$$N_{free} = \frac{N_c}{qA} \frac{1}{(\frac{1}{kT} - \frac{1}{kT_{ef}(\Psi_s)})} e^{(q\Psi_s - E_{fo})(\frac{1}{kT} - \frac{1}{kT_{ef}(\Psi_s)})}. \tag{7.26}$$

From Gauss' Law, the total charges in the a-Si:H TFT, which include the localized trapped charges and the free electrons can be related to the electric field at the oxide/a-Si interface as:

$$N_{free} + N_{loc} = \frac{\epsilon}{q} E(\Psi_s). \tag{7.27}$$

Using the effective temperature approach, the assumptions that $n_{loc} \gg n_{free}$ and the separate consideration of the deep states and tail states as required in other analytical models [48][49][51] are not needed in deriving the N_{free} formula any more.

The effective temperature defined in Eq. (7.25) reflects the effects of the trapped charges in the deep and tail states and the mobile carriers. As shown in Eq. (7.25), the effective temperature is a function of characteristic temperatures of deep and tail states (T_d, T_t), deep and tail state density at conduction band (g_d, g_t) and the operation temperature.

Band mobility	μ_0	**17**	**cm^2/ Vs**
Gate Length	**L**	**8**	**μm**
Gate Width	**W**	**80**	**μm**
Conduction-band effective	**N_c**	**7×10^{19}**	**cm^{-3}**
Deep localized state	**g_d**	**8.8×10^{18}**	**$cm^{-3} ev^{-1}$**
Tail localized state	**g_t**	**2.1×10^{22}**	**$cm^{-3} ev^{-1}$**
Deep state characteristic temperature	**T_d**	**997**	**K**
Tail state characteristic temperature	**T_t**	**243**	**K**
Bulk Fermi level	**E_{f0}**	**0.65**	**eV**
a-Si active layer thickness	**T_i**	**500**	**Å**
Insulator thickness	**T_{ox}**	**3000**	**Å**
a-Si permittivity	**ε**	**1×10^{10}**	**F/m**
Insulator permittivity	**ε_{ox}**	**6×10^{10}**	**F/m**
Flatband voltage	**V_{FB}**	**0.7**	**V**
a-Si bandgap	**E_g**	**1.72**	**eV**

Table 7.1: Device parameters of the a-Si:H TFT under study.

Applying Gauss' Law at the oxide/a-Si interface and considering the voltage drop in the oxide region, one obtains:

$$V_g = V_{fb} + \Psi_s + \frac{q(N_{free} + N_{loc})}{C_{ox}} = V_{fb} + \Psi_s + \frac{\epsilon}{C_{ox}} A e^{\frac{q\Psi_s - E_{fo}}{kT_{ef}(\Psi_s)}}, \tag{7.28}$$

where C_{ox} is the unit area oxide capacitance, and V_{fb} is the flat-band voltage [49][52]: $V_{fb} = \frac{q^2 N_{ss}}{C_{ox}} \frac{E_{fo}}{q} - \frac{Q_f}{C_{ox}} + \phi_m + x_s$, where N_{ss} is the density of the oxide/a-Si interface charge, Q_f is the fixed charge per unit area in the oxide, ϕ_m is the work function of the gate metal, and x_s is the electron affinity of a-Si. From Eqs. (7.22)(7.25)(7.28), the electrostatic potential at the oxide/a-Si:H interface as a function of the gate voltage can be found. From Eqs. (7.22)(7.25)(7.26), the total mobile carriers in the a-Si:H TFT can be obtained. Using these equations, the drain current and capacitance models of a-Si:H TFT's can be derived [62]. Typical device parameters are shown in Table 7.1[53].

7.8 Polysilicon TFT

Polysilicon thin-film transistors(TFTs) built on an insulator, which can be regarded as an SOI structure, have been receiving attention owing to their advantages in liquid

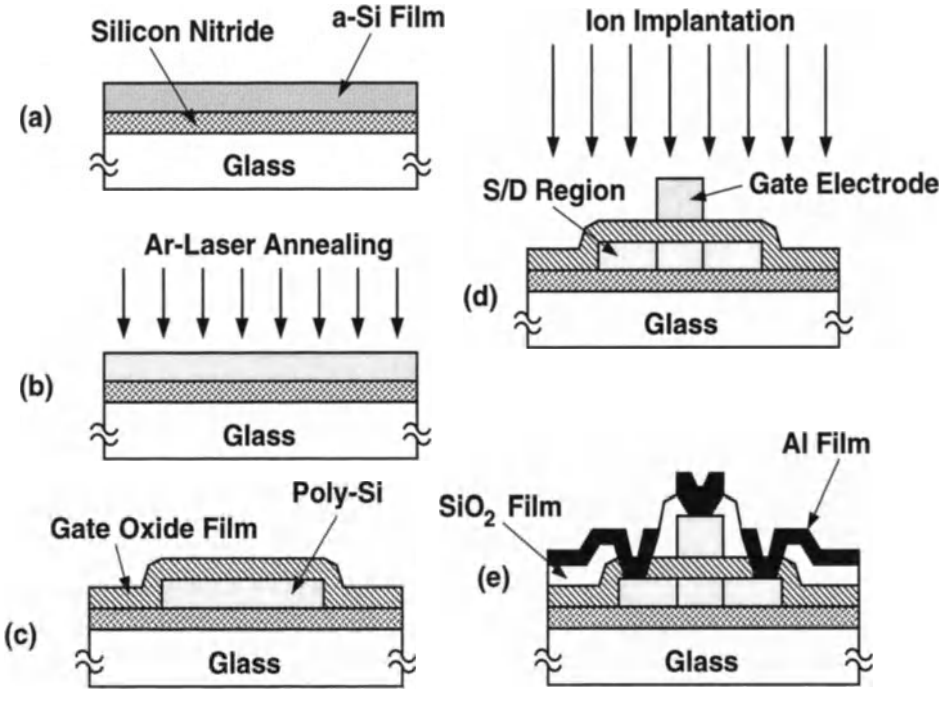


Figure 7.40: Fabrication process of a polysilicon TFT technology.

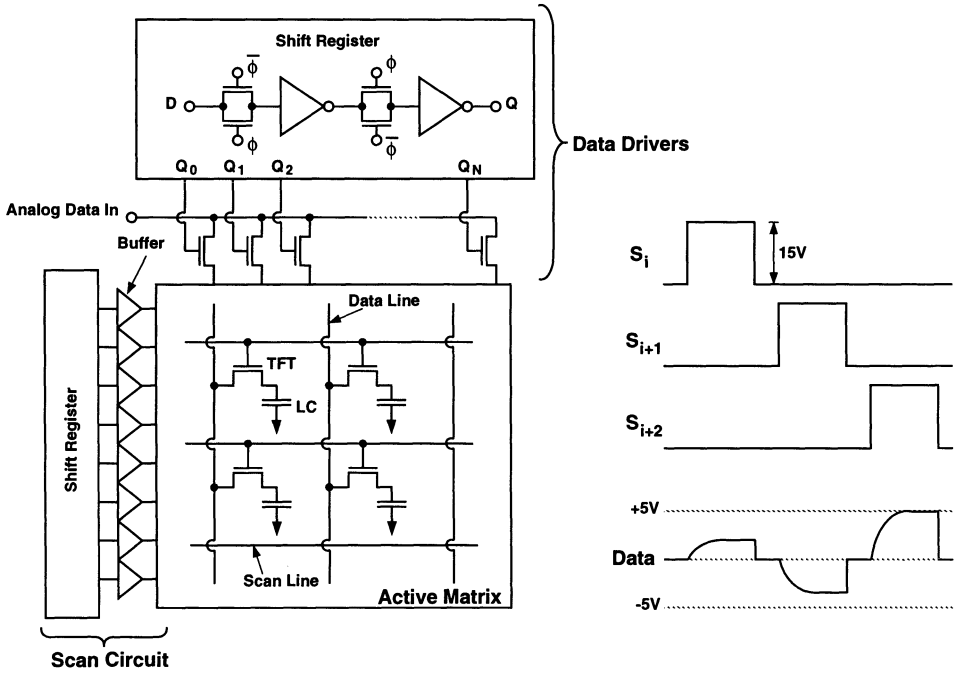


Figure 7.41: Active matrix liquid-crystal display (AMLCD) driving circuits using polysilicon TFTs.

crystal display (LCD)-related[65][66], and memory[67][74] applications. Fig. 7.40 shows the fabrication process of a polysilicon TFT technology[75]. As shown in the figure, on the glass substrate, a 100nm silicon nitride is deposited as the buffer layer. On the top of the nitride buffer layer, a 150nm amorphous layer is deposited by RF magnetron sputtering. Then polycrystallization of this amorphous silicon layer is carried out by an Ar-laser—the polysilicon layer is formed. After the polysilicon layer outside the TFT region is etched off, an oxide layer used as the gate oxide is deposited, followed by deposition of another phosphorus-doped silicon film, which is patterned to form the gate electrode by photolithography and etching. The source/drain region is done by ion implantation. After depositing another oxide layer for passivation, contact hole formation and metallization finalize the whole fabrication procedure. Fig. 7.41 shows the active matrix liquid-crystal display (AMLCD) driver circuits using polysilicon TFTs[76]. As shown in the figure, the main circuit element of the AMLCD is composed of the LCD pixels, scan lines, data lines, scan

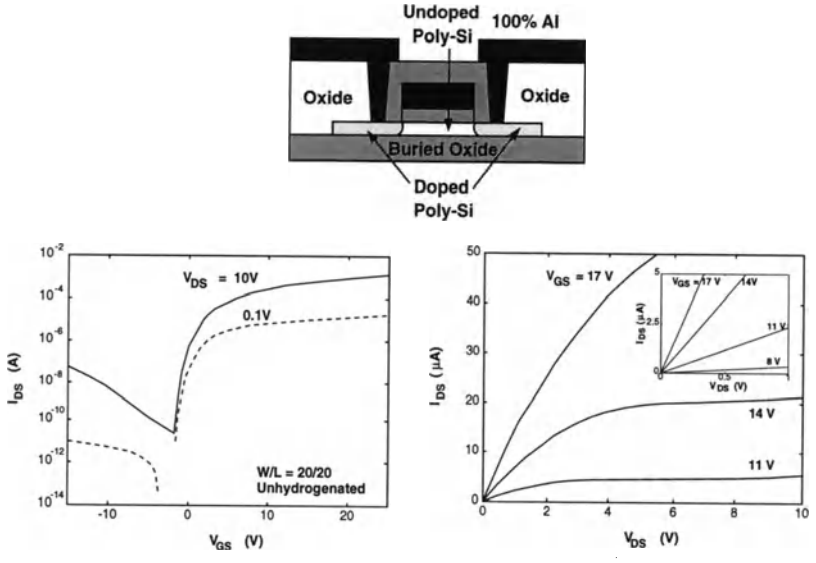


Figure 7.42: Cross section of a polysilicon thin-film transistor (TFT) and its IV characteristics.

circuits, and the data driver circuit. The pixel is made of a polysilicon TFT and a liquid crystal capacitor, which is composed of the liquid crystal and two transparent electrodes. The scan circuit provides appropriate signals to drive the scan lines. Each time only a row of pixels can accept the signals from the data driver, which provides the charge for the liquid crystal capacitor. As a result, the transmission of light through liquid crystals is controlled. As shown in the figure, there is a digital control circuit made of polysilicon TFTs. In general, the performance of the polysilicon TFTs is much worse than that of the single-crystal MOS devices. Therefore, the control circuits realized by polysilicon TFTs are more difficult to design.

Fig. 7.42 shows the cross section of a polysilicon thin-film transistor (TFT) and its IV characteristics.[68]. Polysilicon TFTs are similar to single-crystal SOI MOS devices except that their thin-films are derived from LPCVD amorphous silicon after recrystallization. In a polysilicon TFT, there exists several single-crystal silicon grains. Due to the effect from the grain boundary, the carrier mobility of polysilicon TFTs is between a-Si:H TFTs and single-crystal MOS devices. As shown in the figure, in the subthreshold region of a polysilicon TFT, there is a peculiar leakage behavior. Fig.7.43 shows the cross section of a p-type polysilicon TFT with its sub-

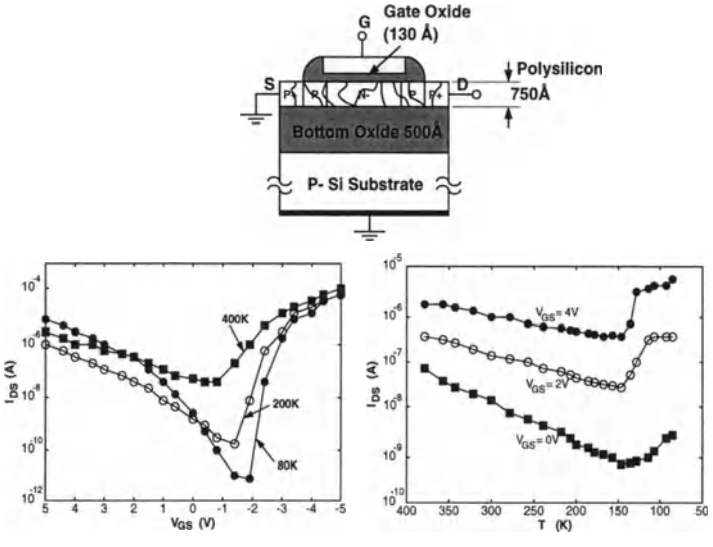


Figure 7.43: Cross section of a p-type polysilicon TFT with its subthreshold IV characteristics.

threshold IV characteristics[69]. From this figure, the leakage current of the device is large. In addition, the leakage current is sensitive to the operating temperature. When the temperature is above 150K, the leakage current decreases as the temperature is lowered. This is due to the thermal field emission via grain boundary traps—the mechanism of tunneling of trapped electrons and holes from the grain boundary traps to the conduction and valence bands, respectively, due to a large electric field. Under 150K, the leakage current increases when the temperature is decreased due to the impact ionization effects.

Fig. 7.44 shows the short channel effect of an n-channel polysilicon TFT[70]. As shown in the figure, as for the single-crystal SOI NMOS devices, when the channel length is scaled down, the threshold voltage becomes smaller. In addition, a larger drain voltage leads to a more noticeable short channel effect due to the 2D effect from the source/drain region to the channel region. Fig. 7.45 shows the narrow channel effect on the threshold voltage of an n-channel polysilicon TFT, which has a channel length of 20μm[71]. Similar to the case for the single-crystal SOI MOS devices, when the channel width is scaled down, its threshold voltage decreases. Compared to the single-crystal SOI MOS devices, the narrow channel effect of a

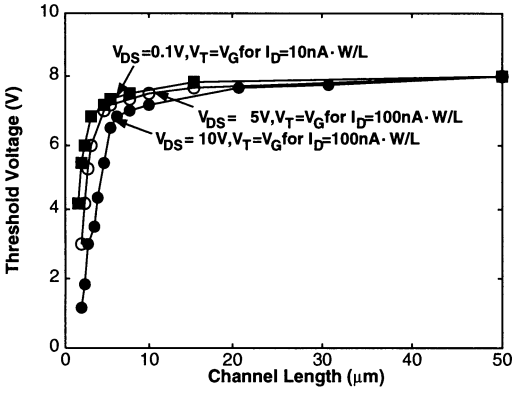


Figure 7.44: Short channel effect of an n-channel polysilicon TFT.

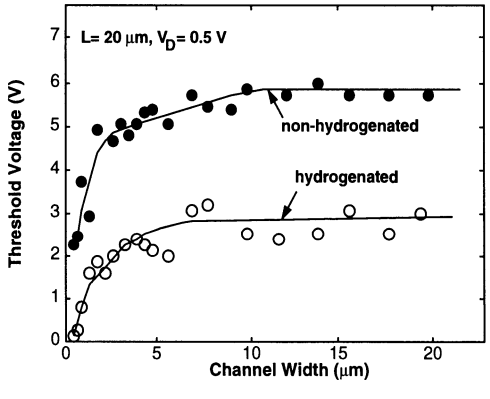


Figure 7.45: Narrow channel effect on the threshold voltage of an n-channel polysilicon TFT, which has a channel length of 20μm.

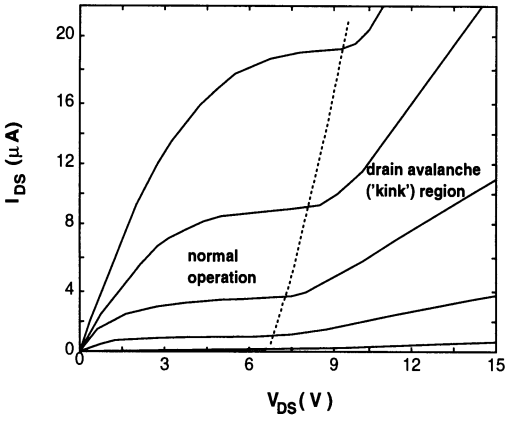


Figure 7.46: Drain current characteristics of an n-channel poly TFT showing kink effect.

polysilicon TFT is due to the decrease in the trap density at the grain boundary when the channel width decreases, which is the result of the different stress between the edge and the center of the channel. When the channel width is scaled down, the relative importance of the edge region of the channel increases. Therefore, the average trap density throughout the channel region falls. As a result, the threshold voltage is lowered.

As for the single-crystal SOI MOS devices, poly TFTs also have kink effect. Fig. 7.46 shows the drain current characteristics of an n-channel poly TFT[72]. When the drain voltage is large, impact ionization occurs in the region near the drain. The generated electrons are collected by the drain terminal. The generated holes are accumulated in the device island until the diode between the source and the island is turned on. As a result, the drain current increases abruptly—kink effect. Due to kink effect, the output impedance of the device becomes worse.

In addition to the driving device for the LCD, polysilicon TFTs have also been used to replace the load resistor in the SRAM memory cell. Fig. 7.47 shows the cross section of the polysilicon PMOS TFT load used in an SRAM cell [73]. The use of polysilicon TFTs to replace the load resistor in the SRAM memory cell provides a lower stand-by current and a higher pull-up speed. In addition, a much better soft-error immunity can be obtained. Furthermore, owing to the 3D capability of

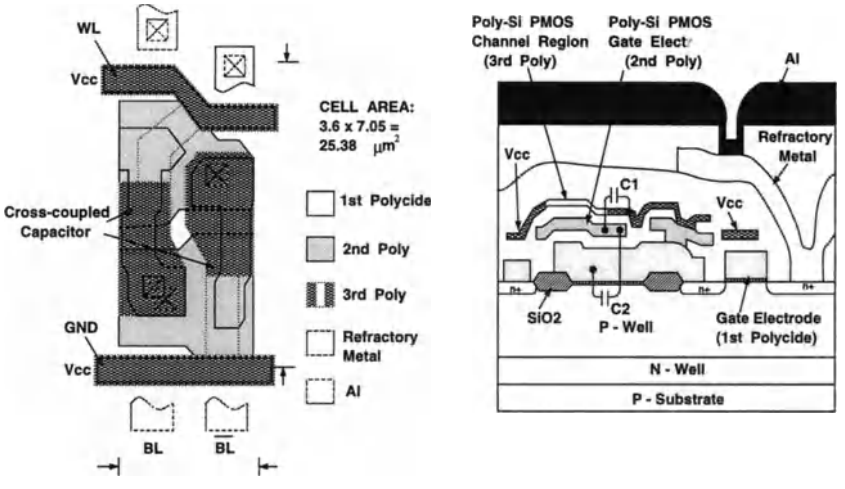


Figure 7.47: Cross section of a polysilicon PMOS TFT load used in an SRAM cell.

the polysilicon TFT structure, the area of the SRAM memory cell does not change substantially when the polysilicon TFT is used as the load resistor. However, a triple-poly process is required.

7.8.1 Moderate Inversion

In this sub-section, moderate inversion drain current behaviors are described. The current conduction of a polysilicon TFT has been explained as related to the grain-boundary-induced potential barrier lowering with influences from the gate voltage [77]-[85]. For polysilicon TFTs, prior to strong inversion, its drain current versus gate voltage curve has a less steep slope as compared to the subthreshold slope in bulk Si MOS devices[85]. Conventionally, the moderate inversion curve has been explained using a monoenergetic trap level model with average trap density concept and an effective channel depth for the effect of the grain boundary in polysilicon TFTs[81]. The moderate inversion curve of polysilicon TFTs has also been explained using a diffusion current model similar to the one for subthreshold region of bulk Si MOS devices[77]-[79]. However, the less steepness in the moderate inversion characteristics is difficult to explain. In polysilicon TFTs, the distribution of localized states in the energy gap of grain boundary is similar to that in hydrogenated

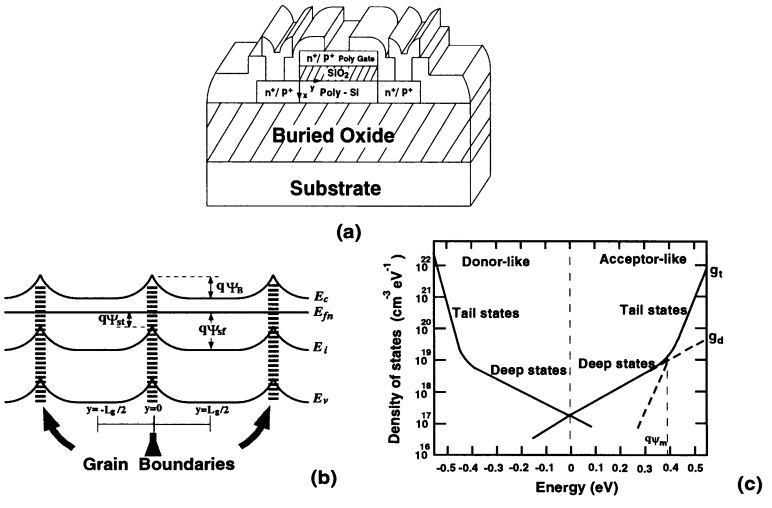


Figure 7.48: (a) Cross section (b) energy band diagram in the lateral direction at the surface (c) distribution of localized acceptor/donor states in the energy gap at the grain boundary of an n-channel polysilicon TFT.

amorphous silicon TFTs [86]-[90]. Considering the distribution of localized deep and tail states, analysis of current conduction in hydrogenated amorphous silicon TFTs has been described in the previous section. In this section, considering the distribution of localized states in the energy gap of grain boundary, an analytical current conduction model is described[87]. It will be shown that prior to strong inversion, the drain current is strongly influenced by the deep and tail states. As compared to the subthreshold region in the bulk Si MOS devices, the less steep slope of the moderate inversion region is due to the lowering in the potential barrier height.

Consider the cross section of a typical n-channel polysilicon TFT with coordinates as shown in Fig. 7.48(a)[87]. The polysilicon thin-film is above the buried oxide. In the channel region, the polysilicon thin-film is undoped. (Note that if no intentional dopant impurities are added into the polysilicon film, the energy band is relatively uniform throughout the film; therefore, other than grain-boundary effect, its behavior is similar to that of a uniform intrinsic single-crystal silicon.) In the source/drain region and the gate electrode, the polysilicon is doped with N^+ and P^+ dopants for n-channel and p-channel devices, respectively. Assume that the polycrystalline material is composed of a linear chain of identical crystallites having

a grain size L_g. The channel length of the device is assumed to be much larger than the grain size. In order to simplify the analysis, grain boundary is assumed to be perpendicular to the lateral channel and of negligible thickness as compared to the channel length (L).

Fig. 7.48(b) shows the energy band diagram in the lateral direction at the surface of an n-channel polysilicon TFT[87]. As shown in Fig. 7.48(b), free carriers are trapped at grain boundary. Consequently, in the region near grain boundary, no free carriers exist. A potential barrier height exists for the inversion electrons. Therefore, electron transport through grain boundary is assumed to be predominantly by thermionic emission over the barrier height (ψ_B). The barrier height is defined as:

$$\psi_B = \psi_{sf} - \psi_{st}, \tag{7.29}$$

where ψ_{st} is the surface electrostatic potential at the grain boundary, and ψ_{sf} is the surface electrostatic potential at the center of the grain.

At grain boundary, the distribution of localized acceptor/donor trap states in the energy gap of a polysilicon TFT is shown in Fig. 7.48(c)[86][90]. The localized acceptor-like trap states, which are important for the n-channel device operation, can be roughly divided into two groups: deep localized acceptor states and tail localized acceptor states. The distribution of localized acceptor states ($g(E)$) can be expressed as:

$$g(E) = g_d e^{\frac{E-E_c}{kT_d}} + g_t e^{\frac{E-E_c}{kT_t}}, \tag{7.30}$$

where g_d and g_t are the deep and tail state density at the conduction-band edge, respectively; T_d and T_t are the characteristic temperatures of the deep and tail states, respectively; E_c is the conduction-band level, E is the energy level, and k is Boltzmann constant. As shown in Fig. 7.48(c), at an energy level ($q\psi_m$), $g_d e^{\frac{q\psi_m - E_c}{kT_d}} = g_t e^{\frac{q\psi_m - E_c}{kT_t}}$, hence, $\psi_m = \frac{E_g}{2q} + \frac{1}{q(\frac{1}{kT_t} - \frac{1}{kT_d})} ln \frac{g_d}{g_t}$. The localized trapped charge density at the grain boundary can be expressed as[62][49]:

$$n_{loc} = \int_{E_v}^{E_c} g(E) f(E) dE, \tag{7.31}$$

where E_v is the valence-band level, $f(E)$ is the Fermi-Dirac occupation function: $f(E) = \frac{1}{1+e^{\frac{E-E_{fn}}{kT}}}$, E_{fn} is the electron quasi-Fermi level, and T is the temperature in Kelvin. From Eqs. (7.30)-(7.31) and using the relationship: $E_{fn} - E_c = q\psi - \frac{E_g}{2}$ (E_g is the bandgap $\cong 1.08eV$)), ψ is the electrostatic potential, the localized trapped

charge density at grain boundary becomes[49]:

$$n_{loc} = \begin{cases} g_d \pi kT \frac{1}{sin(\pi \frac{T}{T_d})} e^{\frac{q\psi - E_g/2}{kT_d}}, & \psi \leq \psi_m, \\ g_t mkT_t e^{(n\frac{q\psi - E_g/2}{kT})}, & \psi > \psi_m, \end{cases} \tag{7.32}$$

where $m = \frac{2\pi-4}{3}(\frac{T}{T_t})^2 + (6-2\pi)(\frac{T}{T_t}) + \frac{4\pi-8}{3}$, and $n = (-\frac{4}{15}(\frac{T}{T_t})^2 + (\frac{T}{T_t}) + \frac{1}{15})$. At the center of each grain in the lateral channel ($y = \frac{L_g}{2}$), from Boltzmann distribution, the free electron density in the conduction band is:

$$n_{free} = N_c e^{\frac{E_{fn} - E_c}{kT}}, \tag{7.33}$$

where N_c is the effective density of states in the conduction band in the grain region of the polysilicon thin-film.

From the 1D Poisson's equation in the vertical direction, the electrostatic potentials at the grain boundary and at the center for each grain are derived.

(a) At grain boundary

At grain boundary, the vertical-direction Poisson's equation is: $\frac{\partial^2 \psi}{\partial x^2} = \frac{q}{\epsilon_{si}} n_{loc}$, where q is the electronic charge, ϵ_{si} is the silicon permittivity, and x is the substrate direction.

(i)deep-state dominated ($\psi_{st} \leq \psi_m$)

If the surface electrostatic potential at grain boundary is smaller than or equal to ψ_m ($\psi_{st} \leq \psi_m$), deep states are more important since E_{fn} is in deep states region as shown in Fig. 7.48(c). Therefore, from Eq. (7.32) and the relationship $2\frac{d\psi}{dx}\frac{d^2\psi}{dx^2} = \frac{d}{dx}(\frac{d\psi}{dx})^2$, one obtains the derivative of the electrostatic potential at the surface of grain boundary: $\frac{\partial \psi}{\partial x}(x=0) = \sqrt{A_d(e^{\frac{q\psi_{st} - E_g/2}{kT_d}} - e^{\frac{-E_g/2}{kT_d}})}$, where $A_d = \frac{2}{\epsilon_{si}} kT_d g_d \pi kT \frac{1}{sin(\pi \frac{T}{T_d})}$. From Gauss' Law, the surface electrostatic potential at grain boundary is related to the gate voltage as:

$$V_G = V_{fb} + \psi_{st} + \frac{\epsilon_{si}}{C_{ox}} \sqrt{A_d(e^{\frac{q\psi_{st} - E_g/2}{kT_d}} - e^{\frac{-E_g/2}{kT_d}})}, \tag{7.34}$$

where V_G is the gate voltage, V_{fb} is the flat-band voltage, and C_{ox} is the unit area oxide capacitance. From Eq. (7.34), the surface electrostatic potential at

grain boundary is: $\psi_{st} = \frac{\frac{E_g/2}{kT_d}+B_d}{C_d+\frac{q}{kT_d}}$, where $B_d = ln((V_G - V_{fb})^2 \frac{C_{ox}^2}{\epsilon_{si}^2 A_d} + e^{\frac{-E_g/2}{kT_d}})$, $C_d = \frac{2(V_G-V_{fb})\frac{C_{ox}^2}{\epsilon_{si}^2 A_d}}{(V_G-V_{fb})^2\frac{C_{ox}^2}{\epsilon_{si}^2 A_d}+e^{\frac{-E_g/2}{kT_d}}}$.

(ii)tail-state dominated ($\psi_{st} > \psi_m$)

If the surface electrostatic potential at grain boundary is larger than ψ_m ($\psi_{st} > \psi_m$), tail states are more important since E_{fn} is in tail state region as shown in Fig. 7.48(c). From Eqs. (7.32) and the relationship: $2\frac{d\psi}{dx}\frac{d^2\psi}{dx^2} = \frac{d}{dx}(\frac{d\psi}{dx})^2$, one obtains the derivative of the electrostatic potential at the grain boundary surface:

$$\begin{aligned}\frac{\partial\psi}{\partial x}(x=0) &= \sqrt{\frac{2q}{\epsilon_{si}}(\int_0^{\psi_m} g_d\pi kT\frac{1}{sin(\pi\frac{T}{T_d})}e^{\frac{q\psi-E_g/2}{kT_d}}d\psi + \int_{\psi_m}^{\psi_{st}} g_t kT_t m e^{n\frac{q\psi-E_g/2}{kT}}d\psi)} \\ &= \sqrt{A_d(e^{\frac{q\psi_m-E_g/2}{kT_d}} - e^{\frac{-E_g/2}{kT_d}}) + A_t(e^{\frac{n(q\psi_{st}-E_g/2)}{kT}} - e^{\frac{n(q\psi_m-E_g/2)}{kT}})}, \quad (7.35)\end{aligned}$$

where $A_t = \frac{2kTg_tkT_t(\frac{2\pi-4}{3}(\frac{T}{T_t})^2+(6-2\pi)(\frac{T}{T_t})+\frac{4\pi-8}{3})}{\epsilon_{si}(-\frac{4}{15}(\frac{T}{T_t})^2+(\frac{T}{T_t})+\frac{1}{15})}$. Similarly as for Eq. (7.34), from Eq. (7.35), the surface electrostatic potential at grain boundary is: $\psi_{st} = \frac{\frac{nE_g/2}{kT}+B_t}{C_t+\frac{qn}{kT}}$, where $B_t = ln((V_G - V_{fb})^2\frac{C_{ox}^2}{\epsilon_{si}^2 A_t} + e^{\frac{n(q\psi_m-E_g/2)}{kT}} - \frac{A_d}{A_t}(e^{\frac{q\psi_m-E_g/2}{kT_d}} - e^{\frac{-E_g/2}{kT_d}}))$, $C_t = \frac{2(V_G-V_{fb})\frac{C_{ox}^2}{\epsilon_{si}^2 A_t}}{(V_G-V_{fb})^2\frac{C_{ox}^2}{\epsilon_{si}^2 A_t}+e^{\frac{n(q\psi_m-E_g/2)}{kT}}-\frac{A_d}{A_t}(e^{\frac{q\psi_m-E_g/2}{kT_d}}-e^{\frac{-E_g/2}{kT_d}})}$.

(b) At grain center

At the center of each grain in the lateral channel of an n-channel polysilicon TFT, the Poisson's equation is: $\frac{\partial^2\psi}{\partial x^2} = \frac{q}{\epsilon_{si}}n_{free}$. From Eq. (7.33) and the relationship: $2\frac{d\psi}{dx}\frac{d^2\psi}{dx^2} = \frac{d}{dx}(\frac{d\psi}{dx})^2$, the derivative of the surface electrostatic potential in the center of each grain is: $\frac{\partial\psi}{\partial x}(x=0) = \sqrt{A_f(e^{\frac{q\psi_{sf}-E_g/2}{kT}} - e^{\frac{-E_g/2}{kT}})}$, $A_f = \frac{2N_ckT}{\epsilon_{si}}$. From Gauss' law, the surface electrostatic potential in the center of the grain in the lateral channel of polysilicon TFT is: $\psi_{sf} = \frac{\frac{E_g/2}{kT}+B_f}{C_f+\frac{q}{kT}}$, where $B_f = ln((V_G - V_{fb})^2\frac{C_{ox}^2}{\epsilon_{si}^2 A_f} + e^{\frac{-E_g/2}{kT}})$, $C_f = \frac{2(V_G-V_{fb})\frac{C_{ox}^2}{\epsilon_{si}^2 A_f}}{(V_G-V_{fb})^2\frac{C_{ox}^2}{\epsilon_{si}^2 A_f}+e^{\frac{-E_g/2}{kT}}}$.

The drain current of a polysilicon TFT is determined by its threshold voltage and its mobility. The threshold voltage is dependent on the barrier height, which

is a function of the gate voltage. The maximum of the barrier height as shown in Eq. (7.29) strongly influences the threshold voltage of the device, which is defined as the gate voltage when its barrier height is at maximum. At the threshold voltage ($V_G = V_T$), the electron quasi-Fermi level is in the deep state region. Therefore, by taking the derivative of barrier height as shown in Eq. (7.29) to zero ($\frac{\partial \psi_B}{\partial V_G} = 0$), the threshold voltage is obtained:

$$V_T = V_{fb} - \frac{E_g/(2q)}{2(1-\frac{T_d}{T})} + \sqrt{\frac{E_g^2}{16(1-\frac{T_d}{T})^2 q^2} - \frac{2\epsilon_{si}k^2 T T_d g_d \pi e^{\frac{-E_g/2}{kT_d}}}{C_{ox}^2(1-\frac{T_d}{T})sin(\pi\frac{T}{T_d})}}. \tag{7.36}$$

As shown in Eq. (7.36), the threshold voltage is strongly influenced by the deep state density and the characteristic temperature of the deep states.

The current conduction in the lateral channel of a polysilicon TFT is via thermionic emission over grain boundary. From the threshold voltage formula (Eq. (7.36)), the drain current is:

$$I_D = \begin{cases} \frac{W}{L}\mu_n C_{ox}((V_G - V_T)V_D - \frac{1}{2}(1+\delta)V_D^2) + I_{leak} & \text{for } V_G - V_T > (1+\delta)V_D, \\ \frac{W}{L}\mu_n C_{ox}\frac{(V_G - V_T)^2}{2(1+\delta)} + I_{leak} & \text{for } V_G - V_T \leq (1+\delta)V_D, \end{cases} \tag{7.37}$$

where W is the channel width, V_D is the drain voltage, I_{leak} is the leakage current at $V_G = V_T$, δ is a fitting parameter, and μ_n is the effective electron mobility[80], which is affected by the barrier height as: $\mu_n = \mu_b e^{-\frac{q\psi_B}{kT}}$, where μ_b is the grain boundary mobility. The above equations are the analytical drain current model for the moderate inversion in an n-channel polysilicon TFT.

The test poly TFT under study [90] has a channel width of 40μm, a channel length of $10\mu m$. It has an undoped thin-film of 600Å and a gate oxide of 300Å. For the n-channel device, its flat-band voltage is $V_{fb} = 1.2$V and the density of states in the conduction band is $N_c = 2.8 \times 10^{19}\text{cm}^{-3}$. For the p-channel device, $V_{fb} = 0.3$V and the density of states in the valence band is $N_v = 1.04 \times 10^{19}\text{cm}^{-3}$. As listed in Tables 7.2 and 7.3, the polysilicon TFT with and without the fluorine contents: $2\times10^{13}\text{cm}^{-2}$ and $2\times10^{15}\text{cm}^{-2}$ affect g_d, g_t, T_d, T_t, and I_{leak}. (Note that as indicated in Eq. (7.37), δ is a parameter to account for the difference between the threshold voltage defined by the maximum in ψ_B in Eq. (7.36) and the actual threshold voltage data. In the moderate inversion region, the influence of δ on the threshold voltage is not easy to identified.) Based on the parameters on Tables 7.2 and 7.3, Fig. 7.49 shows the distribution of localized acceptor/donor states in the energy gap at the grain boundary of a polysilicon TFT [90]. (Note that the fluorine states tie up the grain boundary states.) As shown in Fig. 7.49, with $2 \times 10^{15} cm^{-2} F^+$, the distribution of localized acceptor/donor states in the energy gap at the grain boundary

Parameter	Unpassivated	Passivated: $2 \times 10^{13}\text{cm}^{-2}\text{F}^{+}$	Passivated: $2 \times 10^{15}\text{cm}^{-2}\text{F}^{+}$
$g_t(\text{cm}^{-3}\text{eV}^{-1})$	10^{22}	5×10^{21}	2.5×10^{21}
$g_d(\text{cm}^{-3}\text{eV}^{-1})$	7×10^{20}	6×10^{20}	5×10^{20}
$T_t(\text{K})$	300	335	380
$T_d(\text{K})$	1200	1060	1007
$I_{leak}(\text{A})$	2.63×10^{-11}	5.75×10^{-11}	1.18×10^{-10}
δ	0.05	0.05	0.05
$V_T(V)$	1.915	1.716	1.643

Table 7.2: n-channel TFT device parameters.

Parameter	Unpassivated	Passivated: $2 \times 10^{13}\text{cm}^{-2}\text{F}^{+}$	Passivated: $2 \times 10^{15}\text{cm}^{-2}\text{F}^{+}$
$g_t(\text{cm}^{-3}\text{eV}^{-1})$	5×10^{21}	3.5×10^{21}	2.5×10^{21}
$g_d(\text{cm}^{-3}\text{eV}^{-1})$	2.57×10^{20}	5.38×10^{20}	4.12×10^{20}
$T_t(\text{K})$	480	500	500
$T_d(\text{K})$	1560	1080	1050
$I_{leak}(\text{A})$	6.3×10^{-11}	1.05×10^{-10}	1.76×10^{-10}
δ	0.1	0.1	0.1
$V_T(V)$	-0.503	-0.215	-0.144

Table 7.3: p-channel TFT device parameters.

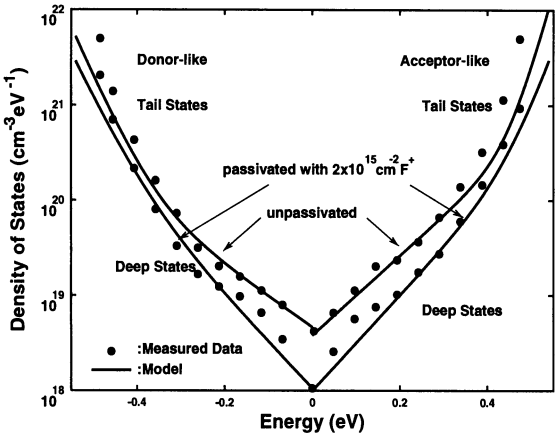


Figure 7.49: Distribution of localized acceptor/donor states in the energy gap at the grain boundary of a polysilicon TFT based on the model results, and the experimental data.

changes.

Figs. 7.50 show the drain current versus gate voltage of (a) the n-channel and (b) the p-channel polysilicon TFTs with and without the fluorine contents of $2 \times 10^{13}\text{cm}^{-2}$ and $2 \times 10^{15}\text{cm}^{-2}$ [90]. The drain voltage is biased at 5V and -5V for n-channel and p-channel devices, respectively. For the n-channel device, $\mu_b = 37\text{cm}^2/\text{Vsec}$. For the p-channel device, $\mu_b = 170\text{cm}^2/\text{Vsec}$. (Note that the grain boundary mobility (μ_b) may be related to grain size[80].) As shown in the figures, compared to the subthreshold region for bulk Si MOS devices, the slope of the moderate inversion region of the n-channel and p-channel polysilicon TFTs is less steep. This is due to a different mechanism involved in the moderate inversion region. In the bulk Si MOS devices, the subthreshold current is exponentially proportional to its gate voltage. In the moderate inversion region of the polysilicon TFT, its slope is determined predominantly by its effective mobility (μ_n), which is exponentially related to the potential barrier height (ψ_B). From the relationship between ψ_B and V_G as indicated in this subsection, due to the deep and tail state densities and the characteristic temperatures of the deep and tail states in the grain boundary, the slope of the moderate inversion region in the polysilicon TFT is less steep as compared to the subthreshold slope in bulk Si MOS devices.

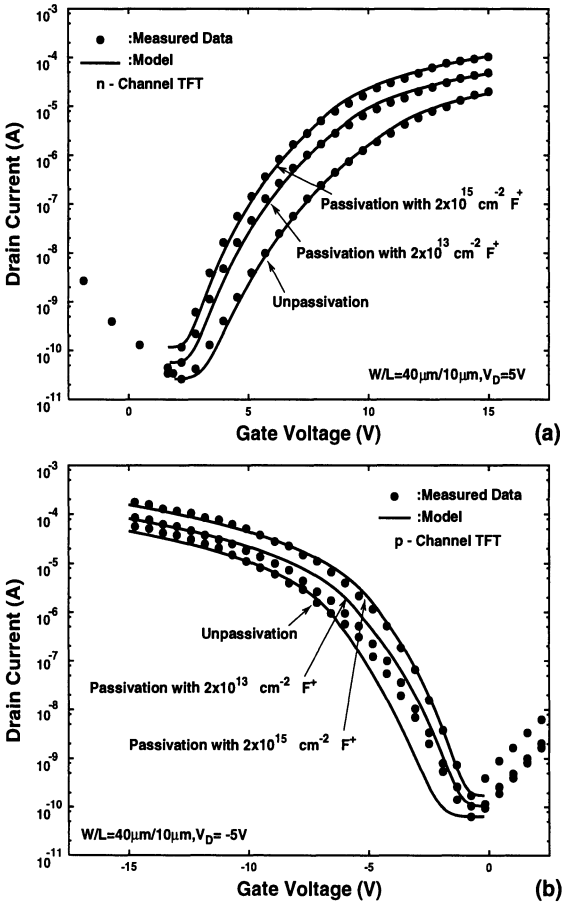


Figure 7.50: Drain current versus gate voltage of (a) n-channel and (c) p-channel polysilicon TFTs with and without the fluorine contents of $2 \times 10^{13}\text{cm}^{-2}$ and $2 \times 10^{15}\text{cm}^{-2}$ based the model result and the experimental data.

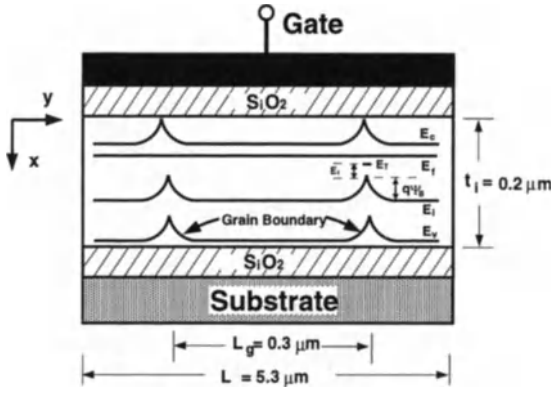


Figure 7.51: Cross section of the inversion-type TFT and its energy band diagram in the lateral channel direction.

7.8.2 Strong Inversion

In the above analysis, the subthreshold current conduction of the polysilicon TFT has been analyzed. The strong inversion current conduction and the capacitance behaviors of inversion-type polysilicon thin-film transistor are described next.

For a poly-silicon TFT biased in the saturation region at a high V_{DS}, the electric field near the drain region can be high such that impact ionization— avalanche multiplication creating electron-hole pairs occurs[86][91]. The impact ionization effect in the polysilicon TFT, which is strongly influenced by the grain boundary, makes the analytical model even more difficult to obtain[92]. This subsection presents analytical inversion-type poly-Si TFTs model considering kink effect suitable for circuit simulation [93].

Consider an inversion-type poly-Si TFT as shown in Fig. 7.51 [93]. (Note that in Fig. 7.51, the band diagram at the oxide interface is at the inverted mode.) Assume that the polycrystalline material is composed of a linear chain of identical crystallites having a grain size L_g, doped uniformly with an acceptor density of N_A. In order to simplify the analysis, grain boundary is assumed to be perpendicular to the lateral channel and of negligible thickness as compared to the channel length (L) such that the thickness of the grain boundary can be neglected. At grain boundary,

it contains $N_T(cm^{-2})$ traps located at energy E_T. In the poly-Si TFT, the trapped electrons are assumed to be uniformly distributed over the whole grain. The total charge density in the poly-Si TFT is the sum of the ionized acceptor density N_A, the trapped electron density, and the mobile electron density. In the substrate direction, Poisson's equation is:

$$\frac{\partial^2\Psi}{\partial x^2} = \frac{q}{\epsilon_s}\left(\frac{N_T/L_g}{1+\frac{1}{2}exp(\frac{E_T-E_f}{kT})} + n_o e^{\frac{\Psi}{\phi_t}} + N_A\right), \tag{7.38}$$

where x is in the substrate direction, q is the electron charge, ϵ_s is the silicon permittivity, Ψ is the electrostatic potential, E_f is the Fermi-level energy, ϕ_t is $\frac{kT}{q}$, k is Boltzmann constant, T is the temperature in Kelvin, and n_o is the intrinsic carrier concentration in the bulk ($n_o = N_A e^{\frac{-2\phi_f}{\phi_t}}$). Note that Eq. (7.38) is valid only when V_{DS} is small. Φ_f is Fermi potential: $\phi_f = \frac{kT}{q} ln\frac{N_A}{n_i}$. Since $E_T - E_f = (E_T - E_i) - q\Psi + q\phi_f = E_t - q\Psi + q\phi_f$, where E_i is the intrinsic energy level, $E_t = E_T - E_i$, Poisson's equation as shown in Eq. (7.38) is rewritten as:

$$\frac{\partial^2\Psi}{\partial x^2} = \frac{q}{\epsilon_s}\left(\frac{N_T/L_g}{1+K_m e^{-\Psi/\phi_t}} + n_o e^{\frac{\Psi}{\phi_t}} + N_A\right), \tag{7.39}$$

where $K_m = \frac{1}{2}e^{\frac{E_t+q\phi_f}{kT}}$. Using the relationship: $2\frac{\partial\Psi}{\partial x}(\frac{\partial^2\Psi}{\partial x^2}) = \frac{\partial}{\partial x}(\frac{\partial\Psi}{\partial x})^2$, from Eq. (7.39), the electric field becomes: $E(\Psi) = \sqrt{\frac{2q}{\epsilon_s}\left(N_A\Psi + \phi_t n_o(e^{\Psi/\phi_t}-1) + \frac{N_T}{L_g}(\Psi + \phi_t ln\frac{1+K_m e^{-\Psi/\phi_t}}{1+K_m})\right)}$. Considering the voltage drop in the gate oxide and using Gauss' Law at the poly-Si/oxide interface, an equation in terms of surface electrostatic potential (Ψ_s) is:

$$V_G = V_{fb} + \Psi_s + \frac{\epsilon_s\sqrt{\frac{2q}{\epsilon_s}\left(\phi_t n_o(e^{\Psi_s/\phi_t}) + (\frac{N_T}{L_g}+N_A)\Psi_s - \frac{N_T}{L_g}\phi_t ln(1+K_m)\right)}}{C_{ox}}, \tag{7.40}$$

where V_{fb} is the flat-band voltage, C_{ox} is the unit area gate oxide capacitance, and V_G is the gate voltage.

Current conduction in the lateral channel of a poly-Si TFT is influenced by the poly-Si grain boundary. As shown in Fig. 7.51, free carriers are trapped at grain boundary. Consequently, in the region near grain boundary, no free carriers exist. A potential barrier height (Ψ_B), which is related to the occupation function in the grain boundary from Ref.[95] and Fig. 7.51: $f = 1/(1+(n_i/2n_s)e^{(E_t/kT)}e^{\Psi_b/\phi_t})$, where n_s is the surface electron concentration ($n_s = N_A e^{\frac{\Psi_s-2\phi_f}{\phi_t}}$), exists for the inversion electrons. (Note that electron capture rate in the grain boundary is proportional to

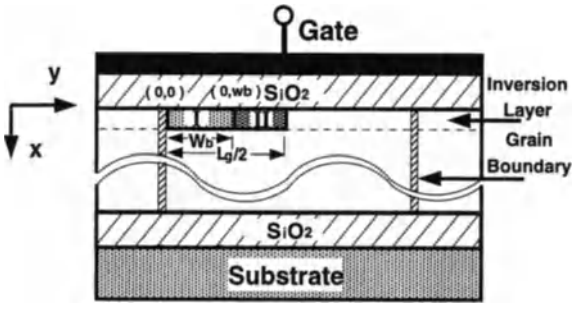


Figure 7.52: Cross section of the inversion-type poly-Si TFT showing I. the depleted region and II. the inverted region in a grain of the poly-Si TFT.

(1-f) [95].) Therefore, electron transport through grain boundary is assumed to be predominantly by thermionic emission over the barrier height (Ψ_B). Depending on the gate voltage, due to the influence of the grain boundary, each grain in the lateral channel region may be (a) fully depleted or (b) partially inverted.

(a) with fully-depleted grain

As the channel of the poly-Si TFT is fully depleted, all electrons in the channel are trapped in grain boundary. Therefore, one obtains: $L_g n_s = \frac{N_T}{1+K_n e^{\frac{\Psi_B}{\phi_t}}}$, where $K_n = \frac{n_i}{2n_s} e^{\frac{E_t}{kT}}$. The potential barrier height is: $\Psi_B = \phi_t ln\left(\frac{2N_T}{n_i L_g} e^{-E_t/kT}\right)$. The potential barrier height is due to effects of the trapped electrons in grain boundary, which are supposed to be existent in the surface channel region.

(b) with partially-inverted grain

Due to trapping at grain boundary, each grain in the lateral channel of the poly-Si TFT may be partially inverted as shown in Fig. 7.52[93]. As shown in the figure, each grain in the channel region is divided into region (I) the depleted region and region (II) the inverted region. The width of the depleted region, which is dependent on the gate voltage and the trap state density, determines the potential barrier height.

Applying Poisson's equation along the poly-Si/oxide interface, i.e., $x = 0$, in the

depleted region of each grain, one obtains:

$$\frac{\partial^2\Psi(x,y)}{\partial x^2}+\frac{\partial^2\Psi(x,y)}{\partial y^2}=\frac{q}{\epsilon_s}(N_A+\frac{N_T/L_g}{1+K_m e^{-\Psi(x,y)/\phi_t}}), \tag{7.41}$$

At the boundary between the depleted and inverted regions (y = W_b), Poisson's equation is:

$$\frac{\partial^2\Psi(x,W_b)}{\partial x^2}+\frac{\partial^2\Psi(x,W_b)}{\partial y^2}=\frac{q}{\epsilon_s}(N_A+n_s+\frac{N_T/L_g}{1+K_m e^{-\Psi(x,y)/\phi_t}}). \tag{7.42}$$

Considering the effect of grain boundary and using gradual channel approximation: $|\frac{\partial^2\Psi(x,y)}{\partial x^2}-\frac{\partial^2\Psi(x,W_b)}{\partial x^2}| \ll |\frac{\partial^2\Psi(x,y)}{\partial y^2}|$, from Eqs. (7.41) &(7.42), one obtains: $\frac{\partial^2\Delta\Psi(y)}{\partial y^2}=\frac{q}{\epsilon_s}n_s \quad for \quad 0\le y\le W_b$, where W_b has a maximum value equal to half of grain size. In the above equation, n_s is independent of y since V_{DS} has been assumed to be 0. $\Delta\Psi(y)$ is defined as the potential difference between the depleted/inverted boundary and a location in the depleted region of each grain ($\Delta\Psi(y)=\Psi(x,W_b)-\Psi(x,y)$). The boundary conditions for the above differential equation are: at the depleted/inverted boundary of each grain both the potential difference and the gradient of the potential are zero ($\Delta\Psi(y)|_{y=W_b}=0$, $\frac{\partial\Delta\Psi(y)}{\partial y}|_{y=W_b}=0$). Integrating the differential equation with the boundary conditions, the potential barrier height, which is equal to the potential drop in the depleted region, is: $\Psi_B=\frac{q}{2\epsilon_s}n_sW_b^2$. In the above equation, W_b is not a function of y since V_{DS} is assumed to be 0.

With partially-inverted grains in the channel, all electrons in the depleted region are trapped in the grain boundary. Thus, $2W_bn_s=\frac{N_T}{1+K_n e^{\frac{\Psi_B}{\phi_t}}}$. Therefore, the potential barrier height under the partially inverted situation becomes: $\Psi_B=-\frac{1}{2}(1+\phi_t-m)+\frac{1}{2}\sqrt{(1+\phi_t-m)^2+4(m+\phi_t)}$, where $m=\phi_t ln\sqrt{\frac{q}{2\epsilon_s n_s}\frac{N_T}{2K_n}}$. When all traps in grain boundary are fully occupied by electrons, thus $\frac{N_T}{1+K_n e^{\Psi_B/\phi_t}}\cong N_T$, therefore $\Psi_B=\frac{qN_T^2}{8\epsilon_s n_s}$. Ψ_B is a function of the surface electron density (n_s), which is the most important as compared to other locations in the x direction in the thin film. The potential barrier height (Ψ_B) and the surface electron density (n_s) can be found. From V_G, its corresponding Ψ_s can be calculated. From Ψ_s, the related surface electron density n_s can be found.

When the gate voltage increases, n_s increases. Due to trapping at grain boundary, electrons may be trapped in grain boundary. Therefore, each grain in the channel region may remain fully depleted, even though from the above formula, the channel

should be with mobile electrons. As V_G increases further, in spite of the trapping effect at grain boundary, the inversion region starts to occur at a location far from grain boundary – the center of each grain. The threshold voltage of a poly-Si TFT is defined as the gate voltage when an inversion region is about to happen at the center of each grain in the channel. At $V_G < V_T$, each grain in the lateral channel is fully depleted. At $V_G > V_T$, each grain in the lateral channel is partially inverted.

At threshold voltage, the depletion width is equal to half of the grain size ($W_b = \frac{L_g}{2}$). Therefore, from the barrier height formula, one obtains: $\Psi_B = \frac{q}{2\epsilon_s} n_s (\frac{L_g}{2})^2$. From $\Psi_B = \phi_t ln(\frac{2N_T}{n_i L_g} e^{-E_t/kT})$ with the fully-depleted grain and from $n_s = N_A e^{(\Psi_s - 2\phi_f)/\phi_t}$, the surface electrostatic potential becomes: $\Psi_s = 2\phi_f + \phi_t ln\left(\frac{8\epsilon_s \phi_t}{qL_g^2 N_A} ln\left(\frac{2N_T}{L_g n_i} e^{-E_t/kT}\right)\right)$. A simplified threshold voltage formula is obtained from Eq. (7.40):

$$V_T = V_{fb} + \Psi_s + \frac{\epsilon_s}{C_{ox}} \sqrt{\frac{2q}{\epsilon_s}\left(N_A \Psi_s + \phi_t n_o (e^{\Psi_s/\phi_t} - 1) + \frac{N_T}{L_g}(\Psi_s + \phi_t ln \frac{1 + K_m e^{-\Psi_s/\phi_t}}{1 + K_m})\right)}. \tag{7.43}$$

For a poly-Si TFT with a small grain size, the threshold voltage formula can be further simplified. For a poly-Si TFT with a small grain size, at the threshold voltage, all traps in grain boundary are fully loaded with electrons. As a result, $L_g n_s = N_T$. Therefore, the surface electrostatic potential becomes: $\Psi_s = 2\phi_f + \phi_t ln \frac{N_T}{L_g N_A}$. From Eq. (7.40), the threshold voltage can be obtained.

At $V_G < V_T$, each grain in the lateral channel of a poly-Si TFT is fully depleted. At threshold voltage, each grain in the lateral channel of a poly-Si TFT is about to have an inverted region. In addition, at the threshold voltage, the situation at grain boundary varies. For a poly-Si TFT with a small grain size, at the threshold voltage, all traps in grain boundary are filled with electrons. On the other hand, with a large grain size, traps in grain boundary are not totally filled. At $V_G > V_T$, no matter what the grain size is, each grain in the lateral channel is partially inverted – the depleted region in each grain is shrunk to W_b ($W_b < \frac{L_g}{2}$). When $V_G > V_T$, traps in grain boundary in a poly-Si TFT with a small grain size are totally filled. On the other hand, with a large grain size, when $V_G > V_T$, traps in grain boundary may be or may not be totally filled with electrons.

For $V_{DS} \leq V_{DSAT}$, the drain current of the poly-Si TFT is: $I_D = \frac{1}{2}\frac{W}{L} C_{ox} \mu_n (2(V_{GS} - V_T)V_{DS} - V_{DS}^2)$. The electron mobility in the channel of a poly-Si TFT is determined by the potential barrier height[84]. $\mu_n = \mu_b exp(-\Psi_B/\phi_t)$, where μ_b is the electron

grain boundary mobility.

Following a similar approach as for the SOI MOS device as described in Chapter 4 and from Ref.[93], for $V_{DS} > V_{DSAT}$, the length of the post-saturation region is:

$$\Delta L = \frac{1}{\lambda} \times \tag{7.44}$$
$$ln\left(\frac{(V_{DS} + \frac{\eta t_i q}{C_{ox}}(\frac{N_T}{L_g} + N_A) - V_{DSAT}) + \sqrt{(V_{DS} + \frac{\eta t_i q}{C_{ox}}(\frac{N_T}{L_g} + N_A) - V_{DSAT})^2 - 4C_1C_2}}{2C_1}\right).$$

The drain current as $V_{DS} \geq V_{DSAT}$ is: $I_{DSAT} = \frac{I_D(V_{DS}=V_{DSAT})}{1-\frac{\Delta L}{L}}$.

For a poly-Si TFT biased in the saturation region at a high V_{DS}, the electric field near the drain region can be very high such that impact ionization – avalanche multiplication creating electron-hole pairs occurs[86][91][92]. As a result, the generated electrons move to the drain. On the other hand, the generated holes move toward the source side. The impact ionization effect in the poly-Si TFT is strongly influenced by the grain boundary.

The current as a result of impact ionization (avalanche) is [96] $I_{aval} = I_{DSAT}(M_{aval} - 1)$, where M_{aval} is the avalanche multiplication factor, which is related to the lateral electric field in the device by the electron impact ionization coefficient $(\alpha exp(\frac{-\beta}{E_y}))$. By integrating the electron impact ionization factor throughout the post-saturation region, the avalanche multiplication factor is obtained: $M_{aval} = \int_0^{\Delta L} \alpha e^{\frac{-\beta}{|E_y|}} dy = \int_{V_{DSAT}}^{V_{DS}} \alpha e^{\frac{-\beta}{|E_y|}} \frac{1}{|E_y|} dv$. The drain current, which is composed of the avalanche current (I_{aval}) and I_{DSAT}, with kink effect becomes: $I_D = M_{aval} I_{DSAT}$. As V_{DS} is small, kink effect is negligible. Therefore, M_{aval} is equal to 1.

Fig. 7.53[93] shows the IV characteristics of the polysilicon TFT with its parameter as shown in Table 7.4 [94]. The electron saturated velocity used in the model for this device is $v_{sat} = 6 \times 10^6 cm/s$. The critical electric field is $E_c = 9 \times 10^4 V/cm$, $\eta = 0.9$, $\alpha = 2 \times 10^6 cm^{-1}$, $\beta = 1.46 \times 10^6 V/cm$.

7.8.3 Capacitance Model

From the MOS capacitance model, the gate-drain capacitance and the gate-source capacitance are defined as: $C_{GD} = \frac{\partial Q_G}{\partial V_D}$, $C_{GS} = \frac{\partial Q_G}{\partial V_S}$, where Q_G is the total charges

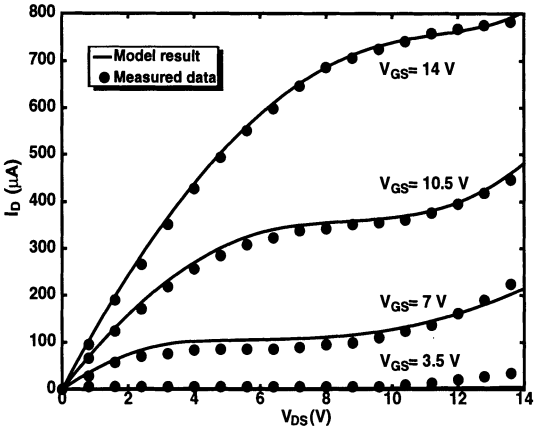


Figure 7.53: The drain current versus V_{DS} plot of the polysilicon TFT.

Parameter	Symbol	Value	Unit
Grain boundary mobility	μ_b	70	cm^2/Vs
Gate length	L	5.3	μm
Gate width	W	20	μm
Trap state density	N_T	5×10^{11}	cm^{-2}
Grain size	L_g	3000	Å
Acceptor doping density	N_A	1×10^{16}	cm^{-3}
Thin film thickness	t_i	2000	Å
Insulator thickness	t_{ox}	760	Å
Flat band voltage	V_{fb}	0.3	V
Trap level energy	E_t	-0.05	eV

Table 7.4: Important parameters of the poly-silicon TFT under study.

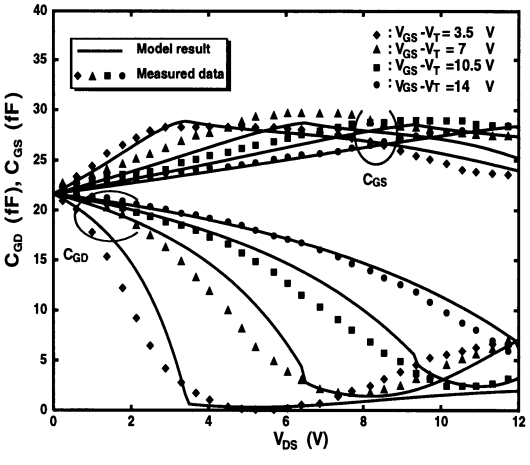


Figure 7.54: C_{GD} and C_{GS} versus V_{DS} of the inversion-type TFT.

in the channel:

$$Q_G = \begin{cases} -\frac{2}{3}WLC_{ox}s\frac{(V_{GD}-V_T)^3-(V_{GS}-V_T)^3}{(V_{GD}-V_T)^2-(V_{GS}-V_T)^2} & \text{for } V_{DS} \le V_{DSAT} \\ -\frac{2}{3}W(L-\Delta L)C_{ox}s(\frac{(V_{GS}-V_T-V_{DSAT})^3-(V_{GS}-V_T)^3}{(V_{GS}-V_T-V_{DSAT})^2-(V_{GS}-V_T)^2}) - W\Delta L(C_{ox}(V_{GS}-V_T \\ -V_{DSAT}) + \eta t_i q(\frac{N_T}{L_g}+N_A)) + (M_{aval}-1)I_{DSAT}\frac{L^2}{\mu_{peff}V_{DS}} & \text{for } V_{DS} > V_{DSAT} \end{cases} \tag{7.45}$$

where s is a fitting parameter, which is defined as when $V_{DS} = 0$, $s \equiv \frac{C_{GS}}{\frac{1}{2}WLC_{OX}}$. As $V_{DS} > V_{DSAT}$, the $(M_{aval}-1)I_{DSAT}\frac{L^2}{\mu_{peff}V_{DS}}$ term accounts for the kink effect as impact ionization is important. μ_{peff} is the hole effective mobility in the bulk. From Eqs. (7.45), C_{GD} and C_{GS} are:

$$C_{GD} = \begin{cases} \frac{2}{3}WLC_{ox}s(1-\frac{(V_{GS}-V_T)^2}{(V_{GS}+V_{GD}-2V_T)^2}) & \text{for } V_{DS} \le V_{DSAT} \\ (\frac{2}{3}Ws\frac{(V_{GS}-V_T-V_{DSAT})^3-(V_{GS}-V_T)^3}{(V_{GS}-V_T-V_{DSAT})^2-(V_{GS}-V_T)^2} - W(C_{ox}(V_{GS}-V_T-V_{DSAT}) \\ +\eta t_i q(\frac{N_T}{L_g}+N_A)))\frac{\partial\Delta L}{\partial V_D} + \frac{L^2}{\mu_{peff}} \cdot \frac{\partial((M_{aval}-1)I_{DSAT}V_{DS}^{-1})}{\partial V_D} & \text{for } V_{DS} > V_{DSAT} \end{cases} \tag{7.46}$$

$$C_{GS} = \begin{cases} \frac{2}{3}WLC_{ox}s(1 - \frac{(V_{GD}-V_T)^2}{(V_{GS}+V_{GD}-2V_T)^2}) & \text{for } V_{DS} \leq V_{DSAT} \\ \frac{2}{3}W(L-\Delta L)C_{ox}s(1 - \frac{(V_{GS}-V_T-V_{DSAT})^2}{(2(V_{GS}-V_T)-V_{DSAT})^2} + \frac{L^2}{\mu_{peff}}(M_{aval}-1)(\frac{I_{DSAT}}{V_{DS}^2} \\ -\frac{W}{V_{DS}(L-\Delta L)}\mu_n C_{ox}(V_{GS}-V_T)) & \text{for } V_{DS} > V_{DSAT} \end{cases} \tag{7.47}$$

Fig. 7.54 shows the C_{GD} and C_{GS} versus V_{DS} plot of the poly-Si TFT under study based on the analytical model[93] and the experimental data [94]. $s = 0.9$. $\mu_{peff} = 85cm^2/Vsec$. For a large V_{DS}, the C_{GD} increases and the C_{GS} decreases as a result of the kink effect.

7.9 Summary

Special-purposes SOI devices have been described. Starting from Fully-Depleted Lean-Channel Transistors (DELTA), which are similar to double-gate SOI CMOS devices, SiGe-channel SOI PMOS devices have been reported. Owing to the buried oxide structure, SOI power devices are suitable for high-temperature operations. SOI bipolar and BiCMOS have also been described. Single-electron transistors built on SOI SIMOX substrates have been analyzed. Amorphous and polysilicon thin-film transistors built on insulators used for LCD have been described.

References

[1] D. Hisamoto, S. Kimura, T. Kaga, Y. Nakagome, M. Isoda, T. Nishida, and E. Takeda, "A New Stacked Cell Structure for Giga-Bit DRAMs using Vertical Ultra-Thin SOI (DELTA) MOSFETs," *IEDM Dig.*, pp. 959-961, 1991.

[2] D. Hisamoto, T. Kaga, Y. Kawamoto and E. Takeda, "A Fully Depleted Lean-Channel Transistor(DELTA)—A Novel Vertical Ultra Thin SOI MOSFET," *IEDM Dig.*, pp.833-836, 1989.

[3] K. W. Su and J. B. Kuo, "Analytical Threshold Voltage Formula Including Narrow-Channel Effects for VLSI Mesa-Isolated Fully Depleted Ultrathin Silicon-on-Insulator N-Channel Metal-Oxide-Silicon Devices," *Jpn. J. Appl. Phys.*, Vol. 34, No. 8A, pp. 4010-4019, Aug. 1995.

[4] D. K. Nayak, J. C. S. Woo, G. K. Yabiku, K. P. MacWilliams, J. S. Park, and K. L. Wang, "High-Mobility GeSi PMOS on SIMOX," *IEEE Elec. Dev. Let.*, Vol. 14, No. 11, pp. 520-522, Nov. 1993.

[5] D. K. Nayak, J. C. S. Woo, J. S. Park, K. L. Wang, and K. P. MacWilliams, "Channel Mobility of GeSi Quantum-Well P-MOSFET's," *Symp. VLSI Tech. Dig.*, pp.107-108, 1991.

[6] P. M. Garone, V. Venkataraman, and J. C. Sturm, "Hole Confinement in MOS-Gated Ge_xSi_{1-x}/Si Heterostructures," *IEEE Elec. Dev. Let.*, Vol. 12, No. 5, pp. 230-232, May 1991.

[7] D. K. Nayak, J. S. Park, J. C. S. Woo, K. L. Wang, G. K. Yabiku, and K. P. MacWilliams, "High Performance GeSi Quantum-Well PMOS on SIMOX," *IEDM Dig.*, pp.777-780, 1992.

[8] J. H. Sim and J. B. Kuo, "An Analytical Back-Gate Bias Effect Model for Ultra-Thin SOI CMOS Devices," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 4, pp. 755-765, Apr. 1993.

[9] T. W. MacElwee, I. D. Calder, R. A. Bruce and F. R. Shepherd, "High-Performance Fully Depleted Silicon-on-Insulator Transistors," *IEEE Trans. Elec. Dev.*, Vol. 37, No. 6, pp.1444-1451, June 1990.

[10] J. B. Kuo, M. C. Tang and J. H. Sim, "An Analytical Back Gate Bias Dependent Threshold Voltage Model for SiGe-Channel Ultrathin SOI PMOS Devices," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 12, pp. 2237-2244, Dec. 1993.

[11] B. Pejcinovic, L. E. Kay, T.-W. Tang, and D. H. Navon, "Numerical Simulation and Comparison of Si BJT's and $Si_{1-x}Ge_x$ HBT's," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 10, pp.2129-2137, Oct. 1989.

[12] R. People, "Indirect Band Gap of Coherently Strained Ge_xSi_{1-x} Bulk Alloys on (100) Silicon Substrates," *Phys. Rev.* B., Vol. 32, No. 2, pp.1405-1408, July 1985.

[13] D. V. Lang, R. People, J. C. Bean, and A. M. Sergent, "Measurement of the Bandgap of Ge_xSi_{1-x}/Si Strained-Layer Heterostructures," Appl. Phys. Let., Vol. 47, No. 12, pp. 1333-1335, Dec. 1985.

[14] B. J. Baliga, "High Voltage Integrated Circuits," *IEEE Press*, 1988.

[15] C. M. Liu, K. H. Lou and J. B. Kuo, "$77K$ versus $300K$ Operation: The Quasi-Saturation Behavior of a DMOS Device and its Fully Analytical Model," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 9, pp. 1636-1644, Sept. 1993.

[16] E. Arnold, T. Letavic, and H. Bhimnathwala, "High-Temperature Off-State Characteristics of Thin-SOI Power Devices," *IEEE Elec. Dev. Let.*, Vol. 17, No. 12, pp.557-559, Dec. 1996.

[17] E. Arnold, H. Pein and S. P. Herko, "Comparison of Self-Heating Effects in Bulk-Silicon and SOI High-Voltage Devices," *IEDM Dig.*, pp. 813-816, 1994.

[18] T. Ifstrom, U. Apel, H.-G. Graf, C. Harendt, and B. Hofflinger, "A 150-V Multiple Up-Drain VDMOS, CMOS, and Bipolar Process in Directed-Bonded Silicon on Insulator on Silicon," *IEEE Elec. Dev. Let.*, Vol. 13, No. 9, pp. 460-461, Sept. 1992.

[19] T. Ohno, S. Matsumoto, and K. Izumi, "An Intelligent Power IC with Double Buried-Oxide Layers Formed by SIMOX Technology," *IEEE Trans. Elec. Dev.*, Vol. 40, No. 11, pp. 2074-2080, Nov. 1993.

[20] U. Apel, H. G. Graf, C. Harendt, B. Hofflinger, and T. Ifstrom, "A 100-V Lateral DMOS Transistor with a 0.3-Micrometer Channel in a 1-Micrometer Silicon-Film-on-Insulator-on-Silicon," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 7, pp.1655-1659, July 1991.

[21] C. M. Liu and J. B. Kuo, "Back Gate Bias Dependent Quasi-Saturation in a High-Voltage SOI MOSFET: 2D Analysis and Closed-form Analytical Model," *SOI Conf. Dig.*, pp. 25-26, 1994.

[22] R. C. Jerome, I. R. C. Post, P. G. Travnicek, G. M. Wodek, K. E. Huffstater, and D. R. Williams, "ACUTE:A High Performance Analog Complementary Polysilicon Emitter Bipolar Technology Utilizing SOI/Trench Full Dielectric Isolation," *SOI Conf. Dig.*, pp.100-101, 1993.

[23] T. Hiramoto, N. Tamba, M. Yoshida, T. Hashimoto, T. Fujiwara, K. Watanabe, M. Odaka, M. Usami, and T. Ikeda, "A 27GHz Double Polysilicon Bipolar Technology on Bonded SOI with Embedded $58\mu m^2$ CMOS Memory Cells for ECL-CMOS SRAM Applications," *IEDM Dig.*, pp.39-42, 1992.

[24] J. C. Sturm and J. F. Gibbons, "Vertical Bipolar Transistors in Laser-Recrystallized Polysilicon", *IEEE Elec. Dev. Let.*, Vol. 6, No. 8, pp. 400-402, Aug. 1985.

[25] B.-Y. Tsaur, R. W. Mountain, C. K. Chen and J. C. C. Fan, "Merged CMOS/Bipolar Technologies utilizing Zone-Melting-Recrystallized SOI Films," *IEEE Elec. Dev. Let.*, Vol. 5, No. 11, pp. 461-463, Nov. 1984.

[26] G. G. Shahidi, D. D. Tang, B. Davari, Y. Taur, P. McFarland, K. Jenkins, D. Danner, M. Rodriguez, A. Megdanis, E. Petrillo, M. Polcari and T. H. Ning, "A Novel High-Performance Lateral Bipolar on SOI," *IEDM Dig.*, pp. 663-666, 1991.

[27] M. Racanelli, W. M. Huang, S. Kuehne, J. Foerstner, S. Wong, and B.-Y. Hwang, "Contact Technology for High Performance Scalable BiCMOS on TFSOI," *IEEE Elec. Dev. Let.*, Vol. 16, No. 10, pp.424-426, Oct. 1995.

[28] J. N. Burghartz, A. O. Cifuentes, and J. D. Warnock, "A Low-Capacitance Bipolar/BiCMOS Isolation Technology, Part II— Circuit Performance and Device Self-Heating," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 8, pp. 1388-1395, Aug. 1994.

[29] J. N. Burghartz, R. C. McIntosh and C. L. Stanis, "A Low-Capacitance Bipolar/BiCMOS Isolation Technology, Part I—Concept, Fabrication Process, and Characterization," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 8, pp. 1379-1387, Aug. 1994.

[30] P. A. Tove, K. Bohlin, F. Masszi, H. Norde, J. Nylander, J. Tiren, and U. Magnusson, "Complementary Si MESFET Concept Using Silicon-on-Sapphire Technology," *IEEE Elec. Dev. Let.*, Vol. 9, No. 1, pp.47-49, Jan. 1988.

[31] B.-Y. Tsaur, H. K. Choi, C. K. Chen, C. L. Chen, R. W. Mountain and J. C. C. Fan, "Merged CMOS/Bipolar Technologies and Microwave MESFETs utilizing Zone-Melting-Recrystallized SOI Films," *IEDM Dig.*, pp.812-815, 1984.

[32] B.-Y. Tsaur, and H. K. Choi, "Radiation-Hardened Silicon-on-Insulator Complementary Junction Field-Effect Transistors," *IEEE Elec. Dev. Let.*, Vol. 7, No. 5, pp.324-326, May 1986.

[33] J. P. Blanc, J. Bonaime, E. Delevoye, J. Gautier, J. de Pontcharra, R. Truche, E. Dupont-Nivet, J. L. Martin, and J. Montaron, "P-JFET on SIMOX for Rad-Hard Analog Devices," *IEEE SOI Conf. Dig.*, pp. 85-86, 1990.

[34] A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, "Room Temperature Operation of Si Single-Electron Memory with Self-Aligned Floating Dot Gate," *IEDM Dig.*, pp. 952-954, 1996.

[35] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, "Room-Temperature Single-Electron Memory," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 9, pp.1628-1638, Sept. 1994.

[36] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwdate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, "Conductance Oscillations of a Si Single Electron Transistor at Room Temperature," *IEDM Dig.*, pp. 938-940, 1994.

[37] M. J. Thompson and H. C. Tuan, "Amorphous Si Electronic Devices and Their Applications," *IEDM Dig.*, pp. 192-195, 1986.

[38] F. Okumura and S. Kaneko, "Amorphous Si:H TFT Array," *Proc. Materials Res. Soc. Symp.*, Vol. 33, M. J. Thompson, Ed., North-Holland: New York, pp. 275-288, 1984.

[39] A. H. Firester, "Active-matrix Addressing for TFT-LCDs," *Soc. Inform. Disp.*, Vol. 3, No. 10, pp.11-14, Nov. 1987.

[40] H. Miki, S. Dawamoto, T. Horikawa, H. Maejima, H. Sakamoto, M. Hayama, and Y. Onishi, "Large Scale and Large Area Amorphous Silicon Thin Film Transistor Arrays for Active Matrix Liquid Crystal Displays," *Mat. Res. Soc. Symp. Proc.* Vol. 95, 1987, pp.431-436.

[41] T. L. Credelle, "Recent Trends in Color Avionic LCD's," *Soc. Inform. Disp.*, Vol. 3, No. 10, pp.15-18, Nov. 1987.

[42] A. R. Kmetz, "Flat-Panel Displays," *IEDM Dig.*, pp. 12-17, 1986.

[43] Y. Nara, Y. Kudou, and M. Matsumura, "Application of Amorphous Field Effect Transistor in 3-Dimensional Integrated Circuits," *Jpn J. Appl. Phys.*, Vol.22, No. 6, pp. L370-372, June 1983.

[44] F. Okumura, K. Sera, H. Asada, S. Kaneko, H. Ichinose, K. Tanaka, T. Yokoi, and C. Tani, "Ferroelectric Liquid-Crystal Shutter Array with a-Si:H TFT Driver," *IEEE Trans. Elec. Dev.*, Vol. 37, No. 10, pp. 2201-2206, Oct. 1990.

[45] Y. Kaneko, A. Sasano, and T. Tsukada, "Analysis and Design of a-Si TFT/LCD Panels with a Pixel Model," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 12, pp. 2953-2958, Dec. 1989.

[46] D. B. Thomasson, M. Dayawansa, J. H. Chang and T. N. Jackson, "Thin Active Layer a-Si:H Thin-Film Transistors," *IEEE Elec. Dev. Let.*, Vol. 18, No. 3, pp.117-119, March 1997.

[47] K. Y. Chung, G. W. Neudeck, and H. F. Bare "Analytical Modeling of the CMOS-like a-Si:H TFT Inverter Circuit," *IEEE J. Sol. St. Ckts*, Vol.23, No. 2, pp.566-572, Apr. 1988.

[48] M. Shur and M. Hack, "Physics of Amorphous Silicon Based Alloy Field-Effect Transistors," *J. Appl. Phys.*, Vol. 55, No. 10, pp.3831-3842, May 1984.

[49] K. Khakzar and E. H. Lueder, "Modeling of Amorphous-Silicon Thin-Film Transistors for Circuit Simulations with SPICE," *IEEE Trans. Elec. Dev.*, Vol. 39, No. 6, pp.1428-1434, June 1992.

[50] M. Shur, C. Hyun, and M. Hack "New High Field-Effect Mobility Regimes of Amorphous Silicon Alloy Thin-Film Transistor Operation," *J. Appl. Phys.*, Vol. 59, No. 7, pp. 2488-2497, April 1986.

[51] G. W. Neudeck, K. Y. Chung, H. F. Bare, and Z. Li "A Simplified Model for the Static Characteristics of Amorphous Silicon Thin-Film Transistor," *Sol. St. Elec.*, Vol. 29, No. 6, pp.639-645, June 1986.

[52] T. Leroux, "Static and Dynamic Analysis of Amorphous-Silicon Field-Effect Transistors," *Sol. St. Elec.*, Vol. 29, No. 1, pp.47-58, Jan. 1986.

[53] M. Shur, M. Hack, and J. G. Shaw, "A New Analytic Model for Amorphous Silicon Thin-Film Transistors," *J. Appl. Phys.*, Vol. 66, No. 7, pp. 3371-3380, Oct. 1989.

[54] M. Hack, M. S. Shur and J. G. Shaw, "Physical Models for Amorphous-Silicon Thin-Film Transistors and Their Implementation in a Circuit Simulation Program," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 12, pp.2764-2769, Dec. 1989.

[55] M. Shur, M. Hack, J. G. Shaw and R. A. Martin, "Capacitance-Voltage Characteristics of Amorphous Silicon Thin-Film Transistors," *J. Appl. Phys.*, Vol. 66, No. 7, pp. 3381-3385, Oct. 1989.

[56] J. S. Choi, G. W. Neudeck and S. Luan, "A Computer Model for Inter-Electrode Capacitance-Voltage Characteristics of an a-Si:H TFT," *Sol. St. Elec.*, Vol. 36, No. 2, pp. 223-228, Feb. 1993.

[57] K. Y. Chung, and G. W. Neudeck, "Transient Analysis of the CMOS-like a-Si:H TFT Inverter Circuit," *IEEE J. Sol. St. Ckts*, Vol.24, No. 3, pp.822-829, June 1989.

[58] M. Matsumura and H. Hayama, "Amorphous-Silicon Integrated Circuit," *Proc. IEEE*, Vol. 68, No. 10, pp. 1349-1350, Oct. 1980.

[59] Y. Nara and M. Matsumara, "An Amorphous Silicon Integrated Inverter," *IEEE Trans. Elec. Dev.*, Vol. 29, No.10, pp.1646-1649, Oct. 1982.

[60] G. W. Neudeck and K. Y. Chung, "A CMOS-Like Amorphous Silicon Ambipolar Thin-Film Transistor," *Proc. Inform. Disp.*, pp. 151-154, May 1987.

[61] M. Shur and M. Hack, "Determination of Density of Localized States in Amorphous Silicon Alloys Form the Low Field Conductance of Thin n-i-n Diodes," *Material Res. Soc. Symp. Proc.*, Vol. 49, pp.69-76, 1985.

[62] S. S. Chen and J. B. Kuo, "An Analytical a-Si:H TFT DC/Capacitance Model using an Effective Temperature Approach for Deriving a Switching Time Model for an Inverter Circuit Considering Deep and Tail States," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 7, pp. 1169-1178, July 1994.

[63] J. G. Shaw and M. Hack, "An Analytic Model for Calculating Trapped Charge in Amorphous Silicon," *J. Appl. Phys.*, Vol. 64, No. 9, pp.4562-4566, Nov. 1988.

[64] M. S. Shur, M. Hack, and C. Hyun, "Flat-band Voltage and Surface States in Amorphous Silicon-Based Alloy Field-Effect Transistors," *J. Appl. Phys.*, Vol. 56, No. 2, pp.382-386, July 1984.

[65] M. Takabatake, J. Ohwada, Y. A. Ono, K. Ono, A. Mimura, and N. Konishi, "CMOS Circuits for Peripheral Circuit Integrated Poly-Si TFT LCD Fabricated at Low Temperature Below 600C," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 6, pp. 1303-1309, June 1991.

[66] A. G. Lewis, I.-W. Wu, T. Y. Huang, A. Chiang, and R. H. Bruce, "Active Matrix Liquid Crystal Display Design using Low and High Temperature Processed Polysilicon TFT's," *IEDM Dig.*, pp. 843-846, 1990.

[67] M. Cao, T. Zhao, K. C. Saraswat, and J. D. Plummer, "A Simple EEPROM Cell Using Twin Polysilicon Thin Film Transistors," *IEEE Elec. Dev. Let.*, Vol. 15, No. 8, pp. 304-306, Aug. 1994.

[68] G. K. Giust and T. W. Sigmon, "Self-Aligned Aluminum Top-Gate Polysilicon Thin-Film Transistors Fabricated Using Laser Recrystallization and Gas-Immersion Laser Doping," *IEEE Elec. Dev. Let.*, Vol. 18, No. 8, pp.394-396, Aug. 1997.

[69] S. S. Bhattacharya, S. K. Banerjee, B.-Y. Nguyen, and P. J. Tobin, "Temperature Dependence of the Anomalous Leakage Current in Polysilicon-on-Insulator MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 2, pp. 221-227, Feb. 1994.

[70] A. G. Lewis, I.-W. Wu, T. Y. Huang, M. Koyanagi, A. Chiang and R. H. Bruce, "Small Geometry Effects in N- and P- Channel Polysilicon Thin Film Transistors," *IEDM Dig.*, pp. 260-263, 1988.

[71] N. Yamauchi, J.-J. J. Hajjar, R. Reif, K. Nakazawa, and K. Tanaka, "Characteristics of Narrow-Channel Polysilicon Thin-Film Transistors," *IEEE Trans. Elec. Dev.*, Vol. 38, No. 8, pp. 1967-1968, Aug. 1991.

[72] A. G. Lewis, T. Y. Huang, R. H. Bruce, M. Koyanagi, A. Chiang and I.-W. Wu, "Polysilicon Thin Film Transistors for Analogue Circuit Applications," *IEDM Dig.*, pp. 264-267, 1988.

[73] T. Yamanaka, T. Hashimoto, N. Hashimoto, T. Nishida, A. Shimizu, K. Ishibashi, Y. Sakai, K. Shimohigashi and E. Takeda, "A 25μm^2 New Poly-Si PMOS Load (PPL) SRAM Cell Having Excellent Soft Error Immunity," *IEDM Dig.*, pp.48-51, 1988.

[74] S. Koyama, "A Novel Cell Structure for Giga-bit EPROMs and Flash Memories Using Polysilicon Thin Film Transistors," *Symp. VLSI Tech. Dig.*, pp. 44-45, 1992.

[75] T. Serikawa, S. Shirai, A. Okamoto, and S. Suyama, "Low-Temperature Fabrication of High-Mobility Poly-Si TFT's for Large-Area LCD's," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 9, pp. 1929-1933, Sept. 1989.

[76] A. G. Lewis, D. D. Lee, and R. H. Bruce, "Polysilicon TFT Circuit Design and Performance," *IEEE J. Sol. St. Ckt*, Vol. 27, No. 12, pp. 1833-1842, Dec. 1992.

[77] H. Hayama and W. I. Milne, "A New Polysilicon MOS Transistor Model Which Includes The Effects of Bulk Trap States in Grain Boundary Regions," *Sol. St. Elec.*, Vol. 33, No. 2, pp.279-286, Feb. 1990.

[78] S. D. S. Malhi, H. Shichijo, S. K. Banerjee, R. Sundaresan, M. Elahy, G. P. Pollack, W. F. Richardson, A. H. Shah, L. R. Hite, R. H. Womack, P. K. Chatterjee and H. W. Lam, "Characteristics and Three-Dimensional Integration of MOSFET's in Small-Grain LPCVD Polycrystalline Silicon," *IEEE Trans. Elec. Dev.*, Vol.32, No. 2, pp.258-281, Feb. 1985.

[79] A. Ortiz-Conde and J. G. Fossum, "Subthreshold Behavior of Thin-Film LPCVD Polysilicon MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 33, No. 10, pp.1563-1571, Oct. 1986.

[80] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, "Conductivity Behavior in Polycrystalline Semiconductor Thin Film Transistors," *J. Appl. Phys.*, Vol. 53, No. 2, pp.1193-1202, Feb. 1982.

[81] T. Serikawa, S. Shirai, A. Okamoto, and S. Suyama, "A Model of Current-Voltage Characteristics in Polycrystalline Silicon Thin-Film Transistors," *IEEE Trans. Elec. Dev.*, Vol. 34, No. 2, pp.321-324, Feb. 1987.

[82] P.-S. Lin, J.-Y. Guo and C.-Y. Wu, "A Quasi-Two-Dimensional Analytical Model for the Turn-on Characteristics of Polysilicon Thin-Film Transistors," *IEEE Trans. Elec. Dev.*, Vol. 37, No. 3, pp. 666-674, March 1990.

[83] R. E. Proano, R. S. Misage and D. G. Ast, "Development and Electrical Properties of Undoped Polycrystalline Silicon Thin-Film Transistors," *IEEE Trans. Elec. Dev.*, Vol. 36, No. 9, pp.1915-1922, Sept. 1989.

[84] B. Faughnan, "Subthreshold Model of a Polycrystalline Silicon Thin-Film Field Effect Transistor," *Appl. Phys. Lett.*, Vol. 50, No. 5, pp. 290-292, Feb. 1987.

[85] T.-S. Li and P.-S. Lin, "On the Pseudo-Subthreshold Characteristics of Polycrystalline-Silicon Thin-Film Transistors with Large Grain Size," *IEEE Elec. Dev. Let.*, Vol. 14, No. 5, pp.240-242, May 1993.

[86] M. Hack, J. G. Shaw, P. G. LeComber and M. Willums, "Numerical Simulation of Amorphous and Polycrystalline Silicon Thin-Film Transistors," *Jpn. J. Appl. Phys.*, Vol. 29, No. 12, L-2360-2362, Dec. 1990.

[87] S. S. Chen and J. B. Kuo, "An Analytical Moderate Inversion Drain Current Model for Polycrystalline Silicon Thin-Film Transistors Considering Deep and Tail States in the Grain Boundary," *J. Appl. Phys.*, Vol. 79, No. 4, pp. 1961-1967, Feb. 1996.

[88] J. G. Shaw and M. Hack, "Amorphous and Polysilicon Device Simulations," *IEDM Dig.*, pp. 915-918, 1992.

[89] G. Fortunato and P. Migliorato, "Determination of Gap State Density in Polycrystalline Silicon by Field-Effect Conductance," *Appl. Phys. Let.*, Vol.49, No. 16, pp.1025-1027, Oct., 1986.

[90] H. N. Chern, C. L. Lee and T. F. Lei, "The Effects of Fluorine Passivation on Polysilicon Thin-Film Transistors," *IEEE Trans. Elec. Dev.*, Vol. 41, No. 5, pp.698-702, May 1994.

[91] M. Hack and A. G. Lewis, "Avalanche-Induced Effects in Polysilicon Thin-Film Transistors," *IEEE Elec. Dev. Let.*, Vol. 12, No. 5, pp. 203-205, May 1991.

[92] Y. H. Byun, M. Shur, M. Hack and K. Lee, "New Analytical Polycrystalline-Silicon Thin-Film Transistor Model for Computer Aided Design and Parameter Extraction," *Sol. St. Elec.*, Vol. 35, No. 5, pp. 655-663, May 1992.

[93] S. S. Chen, F. C. Shone, and J. B. Kuo, "A Closed-Form Inversion-Type Polysilicon Thin-Film Transistor DC/AC Model Considering the Kink Effect," *J. Appl. Phys.*, Vol. 77, No. 4, pp. 1776-1784, Feb. 1995.

[94] C. C. Li, H. Ikeda, T. Inoue, and P. K. Ko, "A Physical Polysilicon Thin Film Transistors Model for Circuit Simulations," *IEDM Dig.*, pp.497-500, 1993.

[95] S. M. Sze, "Physics of Semiconductor Devices," *Wiley: New York*, 1991.

[96] F.-C. Hsu, P.-K. Ko, S. Tam, C. Hu, and R. S. Muller, "An Analytical Breakdown Model for Short-Channel MOSFET's," *IEEE Trans. Elec. Dev.*, Vol. 29, No. 11, pp.1735-1740, Nov. 1982.

Problems

1. Consider the DELTA NMOS device as shown in Fig. 7.4, which has an N^+ poly-gate, a sidewall oxide and a front oxide of 120Å, a channel length of 1μm, and a p-type silicon thin-film doping density of $8 \times 10^{16}\text{cm}^{-3}$.

   (a) How thin the silicon thin-film should be such that fully-depleted of the silicon thin-film during the turn-on of the device can be assumed? At $V_{GS} = 0$, how thin the silicon thin-film should be to ensure the fully-depleted of the silicon thin-film?

   (b) If the channel width (Si-island height) is 0.7μm and the silicon thin-film is 1500Å, what is the threshold voltage?

   (c) If the channel width becomes 0.35μm, from (b), what is the threshold voltage?

   (d) If the silicon thin-film doping density becomes $2 \times 10^{17}\text{cm}^{-3}$, repeat (a)-(c).

2. Consider the SiGe-channel SOI PMOS device as shown in Fig. 7.5, which has an N^+ poly-gate, a front gate oxide of 100Å, an undoped Si-cap of 80Å, an undoped Si-Ge channel of 180Å with a Ge of 25%, a silicon thin-film of 740Å doped with an n-type density of $3 \times 10^{16}cm^{-3}$ under the Si-Ge channel, a buried oxide of 4000Å, and a p-type substrate doped with a density of $10^{15}cm^{-3}$. Analyze its back gate bias effect.

   (a) Compute the back gate biases at the boundaries between Case I and Case II; between Case II and Case III; between Case III and Case IV.

   (b) Plot the threshold voltage and subthreshold slope versus back gate bias.

   (c) If the thickness of the Si-cap layer becomes 50Å and the thickness of the SiGe-channel becomes 210Å, repeat (a) and (b).

   (d) If the silicon thin-film doping density becomes $8 \times 10^{16}\text{cm}^{-3}$, repeat (a)-(c).

3. Consider Fig.7.16. The LDMOS in Fig.7.16 has a silicon thin-film of 0.8μm, a drift region with an n-type doping density of $2 \times 10^{16}\text{cm}^{-3}$, a buried oxide of 1.5$\mu$m, and a p-type substrate doping density of $10^{15}cm^{-3}$.

(a) At $V_{DS} = 40V$, at what back gate bias (V_{BS}) the 2-segment depletion region as shown in Fig. 7.18(b) exists in the drift region of the device?

(b) At $V_{BS} = -50V$, at what V_{DS}, the 2-segment depletion region as shown in Fig. 7.17(b) exists in the drift region of the device?

(c) If the doping density of the drift region becomes 10^{16}cm^{-3} and $4 \times 10^{16}\text{cm}^{-3}$, repeat (a) and (b).

4. Consider an amorphous TFT as shown in Fig. 7.39 with its parameters listed in Table 7.1.

(a) At $V_{DS} = 0.01V$, $V_{GS} = 25V$, compute the intrinsic C_{GD}.

(b) At $V_{DS} = 10V$, $V_{GS} = 25V$, compute the drain current and the intrinsic C_{GD}.

(c) If the trapping density in the silicon thin-film becomes 2x and 5x, repeat (a) and (b). Discuss the influence of the trap density in the intrinsic capacitances.

5. Consider a poly-TFT as shown in Fig. 7.48 with the parameters for the unpassivated in Table 7.2 and 7.3. The device is biased at $V_{DS} = 5V$.

(a) At what V_G, what is the minimum value of the drain current? What is the best value in its subthreshold slope?

(b) If the trap density at the grain boundary becomes 2x and 0.5x, repeat (a). Discuss the influence of the trap density in the subthreshold slope.

6. Consider a poly-TFT as shown in Fig. 7.51. with the parameters listed in Table 7.4.

(a) Compute the threshold voltage.

(b) At $V_{GS} = 15V$, $V_{DS} = 1V$, what are the drain current and the intrinsic C_{gd}?

(c) At $V_{GS} = V_{GD} = 5V$, repeat (b).

(d) If the grain size becomes 0.5x and 2x, repeat (a)-(c). Discuss the influence of the grain size in the threshold voltage and the intrinsic C_{gd}.

(e) If the trap density at the grain boundary becomes 2x and 0.5x, repeat (a)-(c). Compared to an amorphous TFT, what is the influence of the trap density in the capacitance of a poly-TFT?

Index