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Preface

This is a book about the design and implementation details of high-speed analog-to-digital converters (ADCs) in advanced digital CMOS processes that achieve lower power consumption for a given speed and resolution than conventional designs, through architectural and circuit innovations that take advantage of unique features in nanometer CMOS processes. It includes a chapter for a phase lock loop (PLL) clock multiplier which has also been designed using innovative circuit techniques and successfully tested. It has been integrated for generating sampling clock to one ADC.

Chapter 1 analyzes the obstacles and opportunities involved in developing ADCs and necessary clocking circuits in nanometer digital CMOS processes, such as reduced transistor gain and linearity, increased switching speed, and increased silicon area. Five most commonly used ADC architectures are reviewed. Chapter 2 describes a 1.2 V 52 mW 210 MS/s 10-bit ADC in 130 nm digital CMOS for application to digital (low) IF receivers, whose advantage over the direct-conversion as a highly integrated receiver architecture has been shown [33, 35]. Using a proposed capacitor network implemented with small value interconnect capacitors which replaces the power hungry resistor ladder in conventional sub-ranging ADCs, and proposed offset canceling comparators, it achieves $>$70 dBc SFDR up to 100 MHz input frequency while consuming only 52 mW, which is the lowest reported to date for $>$200 MS/s 10-bit ADCs. The active area is 0.38 mm^2 including decoupling caps which is also competitive with other existing 10-bit pipeline ADCs. Chapter 3 presents a 1.2 V 32 mW 1.25 GS/s 6-bit ADC (applications include serial links, disk drives and UWB receivers) implemented in 130 nm digital CMOS [5]. This ADC uses a new type of architecture that combines flash and SAR to achieve the lowest power consumption, 6-bit $>$1 GS/s ADC implementation reported in open literature to date. The SAR internal clock frequency is 2.5 GHz, which is the fastest ever used for a SAR ADC. Because it does not require any calibration step or post processing, and has the same latency as most flash ADC, it can be a direct drop-in replacement of 6-bit flash ADCs in existing application to lower power by more than 5 times [30]. Chapter 4 details the integrated clock-multiplier PLL to generate sampling and internal clock for the 1.25 GS/s ADC. Measurement shows 0.4-ps-rms jitter (integrated

from 3 kHz to 300 MHz offset) for $\geq$2.5 GHz outputs and tuning range from below 1 GHz up to 3 GHz. A new loop filter structure based on a sample-reset phase to voltage converter and a Gm-C filter enables phase error preamplification to lower PLL in-band noise without increasing loop filter capacitor size.

This book is based upon my Ph.D. dissertation; it includes more details and measurement results for each project, and a completely new chapter which describes the 10-bit two-step ADC whose measurement finished only after I received my Ph.D. degree, and is not included in my dissertation. Because this book focuses on high-speed ADCs, it does not include a chapter for an early project of my Ph.D. research — a 14 mW 125 MS/s 1.25 MHz signal bandwidth 84 dB dynamic range $\Delta\Sigma$ modulator in 0.25 µm CMOS [4].

These projects I finished during my Ph.D. study in the University of Texas at Austin would never have been possible without the help and kindness of many individuals. First of all, I would like to express my gratitude to my Ph.D. advisor, Professor Shouli Yan for his confidence in me and enthusiasm for the results of my work. He gave me countless insightful suggestions and guidance, and at the same time also allowed me freedom to pursue my own ideas. I am grateful to Marco Corsi for giving me the opportunity to do a six-month intern at Texas Instruments in 2007. I sincerely thank Bob Payne for his guidance during my intern. The high standard in robustness of a design which he keeps and demands was very inspirational. I was educated that designing even the simplest circuit is not a trivial task. I would also like to thank Yunchu Li, Richard Schreier, Steve Rose, Will Yang and other engineers at Analog Devices for their guidance and discussions during my internship in 2006. I learned many important principles and fundamental concepts about analog/mixed-signal design through taking Mr. Eric Swanson's course at UT in a very early stage of my study, to which I am intensely grateful. I benefited a lot from my fellow students, especially Tongyu Song and Chaoming Zhang. Their attention to detail and willingness to share information allowed me to spot several catastrophic mistakes in my layout design which would certainly have lead to failure of the test chips. Their friendship made my stay at UT enjoyable. The projects included in this book would never have been completed in a timely manner without the kindness and help of Ken Agee and Kenneth Hodson at Texas Instruments who allowed me to use the labs they manage, and spent their time helping me with the test setup and soldering the tiny chip onto the board after my failed attempts. I appreciate the help from the staffs in the computer engineering research center, especially Andrew Kieschnick who as our system administrator maintained a primitive but very comfortable CAD environment (Windows XP + VNC to Linux servers, Cadence custom flow with UMC foundry design kit + spectreRF + Calibre) with virtually no down time which enabled efficient chip development (in fact, faster and less stressful than many proprietary CAD systems I used during my internship in industry) and other computing tasks. Finally I would like to thank my parents who encouraged and supported me during my study.

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Introduction

1.1 Motivations

The proliferation of digital technology has benefited our society greatly over the last several decades. Digital signal processing allowed virtually infinitely large time constant and dynamic range to be realized with very little space using very little energy. This enabled sound and images with higher quality than ever before to be generated, detected, recorded and transmitted with devices that are light and small enough to be carried around (e.g. CD, DVD, hard-disks, MP3 players, cell phones). It also revolutionized the communication industry by allowing more information to be transmitted through the efficient use of limited frequency spectrum (e.g. DSL, CDMA, WiFi, Satellite radio). To further reap benefit from digital signal processing, not only is it important to develop low power, high performance CMOS digital circuits through innovations in processing technology, computer architecture, circuits and testing methodology, but also it is important to realize high performance and low power analog interface that can be easily integrated in the latest CMOS processes needed for high performance digital VLSI.

1.1.1 Analog-to-Digital Converters

There is a constant drive in consumer electronic products toward single-chip integration in standard digital CMOS. Integration not only reduces system production cost but also increases performance, features and reliability. Nanometer CMOS technology benefits tremendously digital circuits in terms of speed, silicon area and power efficiency. Analog-to-digital converter (ADC) circuits also benefit a lot from scaling, due to the reduced parasitic capacitances and increased element matching for same physical dimension because of improved lithography accuracy [29].

On the other hand, the intrinsic gain (g_m/g_{ds}) , as well as the linearity of transistors have reduced (Fig. 1.1 [1]). The high speed of scaled-down CMOS transistors

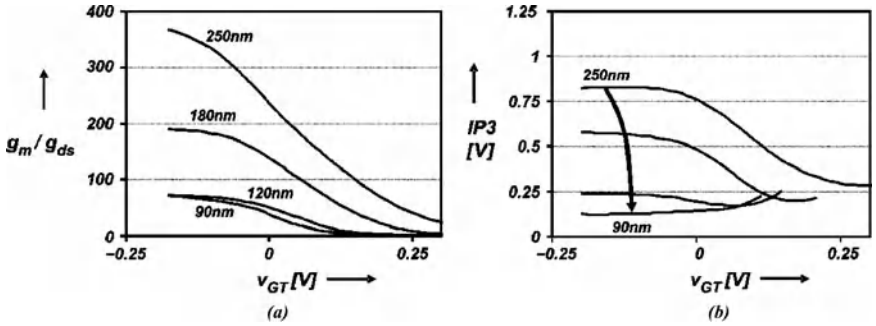

Fig. 1.1 Intrinsic gain (**a**) and output-referred third order intermodulation intercept point (IP3) (**b**) vs. gate-overdrive voltage for various CMOS technology nodes with L = 1μm [1]

depends on thin gate oxide, which however limits the maximum voltage that can be applied on the gate oxide. The reduced power supply voltage makes it difficult to use traditional analog structures such as cascode to increase amplifier gain with little impact on stability. We are now forced to cascade multiple stages of amplifiers to obtain enough open-loop gain. However, cascading introduces more poles or more signal delay, necessitating complicated compensation schemes to make the amplifier stable in feedback. These frequency compensation schemes often require large compensation capacitors hence die area, increase power consumption, and sacrifice circuit speed.

For the above reasons, many traditional analog circuits which rely on analog feedback to achieve accuracy no longer perform as well in scaled processes, necessitating change of ADC architectures toward those that are more amenable to nanometer CMOS. ADC architectures such as two-step subranging and successive approximation (SAR) are being given renewed attention in recent years ([15], [6], [28], [32]). These architectures do not rely on accuracy of feedback based analog signal processing to achieve accuracy of A/D conversion.

Chapter 2 presents a 10-bit two-step ADC that takes advantage of small value but well-matched interconnect capacitor and faster switch available in nanometer CMOS to achieve higher SFDR and lower power than most 10-bit pipeline ADCs. It does not require high transistor DC gain (g_m/g_{ds}) at all, it even deliberately lowers this gain to achieve higher speed in the preamps. In Chapter 3, the SAR architecture is extended to cover high speed applications where only flash ADCs could be used until now. A new architecture has been proposed and successfully demonstrated that exploits highly accurate matching of very small interconnect capacitors and fast digital logic in nanometer CMOS, to achieve the lowest power $>$1 GS/s 6-bit ADC ever published to date.

As process scales down, the problems facing medium $\sim$ high resolution ADCs are power consumption and die area. Since conversion error due to element mismatch can be reduced by various circuit techniques, signal-to-noise ratio (SNR) in high resolution ADCs are usually limited by thermal noise. If signal swing reduces by half due to voltage headroom limitation, signal power reduces by four times.

To keep the same SNR, four times as large capacitance is needed to reduce kT/C noise by the same amount. This requires four times large opamps transconductance to keep the same operation speed, which means the size of the op-amp, as well as its bias current must be increased four times. While the rest of the chip scales down, capacitors, whose size is limited by the kT/C noise requirement cannot be reduced. Therefore, the relative size of analog circuits in SoCs has kept increasing. On the other hand, nanometer CMOS offers high speed transistors. This favors oversampling ADCs with high sampling frequency because capacitor size can be reduced as oversampling ratio (OSR) increases. Even for medium resolution ($10 \sim 13$ bit) applications, $\Delta\Sigma$ ADCs with high OSR are becoming the preferred choice for integration in recent years [16], [21]. In [4], new circuit techniques have been used to achieve the highest SNR to power consumption ratio (84 dB at 14 mW) among $1 \sim 1.25$ MHz signal bandwidth $\Delta\Sigma$ ADCs in open literature, while using a very high sampling frequency (125 MHz) to relax anti-aliasing filter requirement.

1.1.2 Clock Generation

The trend toward high frequency and broadband digital communication increased the demand for low jitter, low phase noise clock generation circuits. Due to limited bandwidth on the printed-circuit board it is necessary to generate and route the high frequency clock signal on-chip. In conventional low jitter clock designs, LC-VCO based PLLs have been dominantly used. However, LC-VCOs suffer from narrow tuning range and large layout area. In this research a ring-oscillator based PLL has been designed. Using a wide PLL bandwidth to lower oscillator noise and a phase noise pre-amplification technique to lower PLL-inband noise, similar levels of jitter performance as LC-VCO has been achieved with 3:1 tuning range and much smaller layout area (Chapter 4).

1.2 A Review of Existing ADC Architectures

1.2.1 Flash

The simplest ADC architecture is the flash ADC. For N bit resolution 2^N comparators are placed in parallel and compares the input voltage with reference voltages generated by a resistor ladder (Fig. 1.2).

Two major drawbacks of flash ADCs are their large silicon area and input capacitance, the latter also limits the signal bandwidth. To increase N by 1, not only must the number of comparators be doubled, but also the size of each comparator must be quadrupled in order to reduce its input referred offset voltage by half to maintain the same DNL/INL. Techniques such as preamplification, offset averaging and

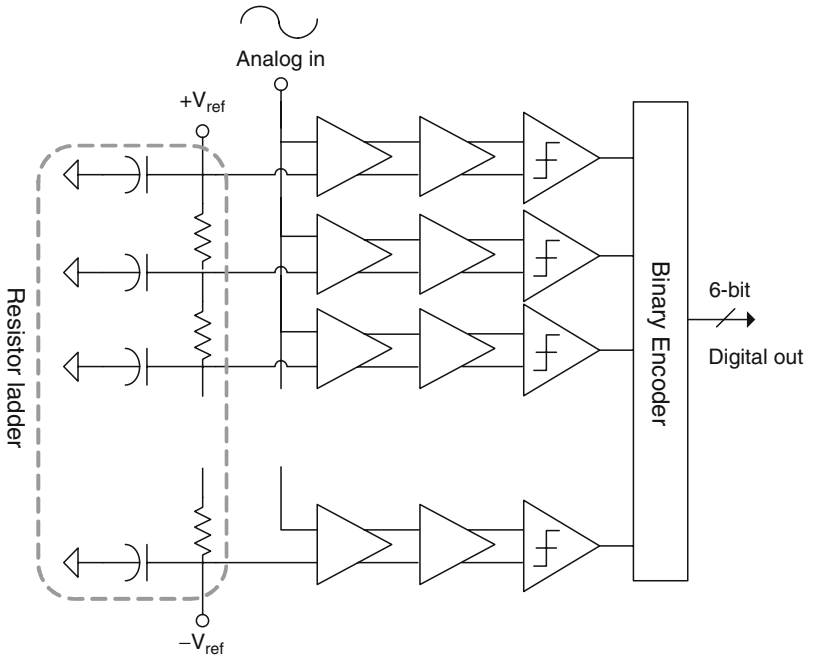

Fig. 1.2 Basic structure of a flash ADC

interpolation greatly help reducing both silicon area and input capacitance, but they are still much larger when compared with other architectures. However, the flash architecture has been exclusively used for high-speed ADCs with conversion rate above 500 MHz.

For 6-bit CMOS ADCs, conversion rate as high as 2 GHz, and for 4-bit, 4 GHz have been reported with power consumption of several hundreds of mW. The high power consumption is due to the large number of preamplifiers and comparators, and the static power consumption of the reference resistor ladder that must also "drive" the ADC input. The input capacitance of a 6-bit flash ADC is typically more than 1 pF, limiting the input bandwidth, and making time-interleaving multiple flash ADCs to obtain higher sampling frequency impractical.

1.2.2 Pipeline

Pipeline is the most widely used architecture for high performance Nyquist-rate ADCs. Instead of digitizing all the bits at once, in the first stage, the most significant bits are digitized with a small flash ADC, then a feedback DAC is used to subtract in analog domain the digitized bits from the input signal, producing the residue voltage, which is amplified and digitized by subsequent stages while the first stage

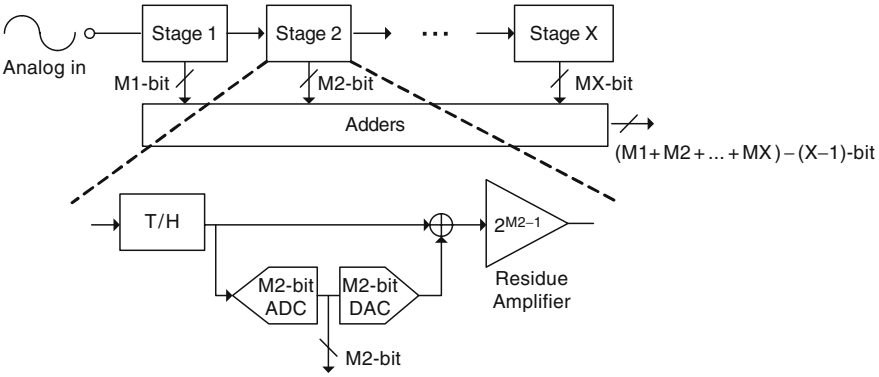

Fig. 1.3 Block diagram of a typical 10-bit pipelined ADC

handles the next sample (Fig. 1.3). If each stage digitizes 1 bit, only N comparators are required rather than 2^N comparators (in reality redundancy is provided and each stage digitize 1.5 bit or more, leading to at least $2N$ comparators.) Because of the pipelining, the sampling frequency can also be high.

The precision of pipelined ADC relies on accurate amplification of the residue, therefore, high DC gain op-amp is necessary. The accuracy requirement on the op-amp can be relaxed by digitizing more bits in the first stage, but the area of the flash ADC and the DAC increases. Also, the op-amp must provide larger closed-loop gain, therefore its bandwidth reduces. Various digital calibration methods that correct for inaccurate op-amp gain or non-linearity in the feedback DAC have been actively researched in recent years and good results are obtained. By using these techniques the op-amp DC gain requirements can be relaxed, and even open loop residue amplification becomes possible [29].

With digital calibration to compensate for analog inaccuracy, combined with the speed of deep submicron CMOS, pipelined ADC with both high sampling frequency and high resolution can be realized [2]. However, the system dynamic range now starts to be limited by front-end circuits. There are also attempts to use pipelined ADC for low resolution, high speed applications [47]. The advantage is the much reduced input capacitance compared with flash ADCs, hence the possibility of time-interleave multiple ADCs to digitize even wider bandwidth [19].

Drawbacks of pipelined ADC are its complexity and power consumption since either accurate residue amplification or complicated digital calibration is necessary. However, it is the most common Nyquist ADC architecture for resolution above 8-bit.

1.2.3 Subranging

Subranging is an architecture that was developed to reduce the number of comparators compared with flash ADC (Fig. 1.4).

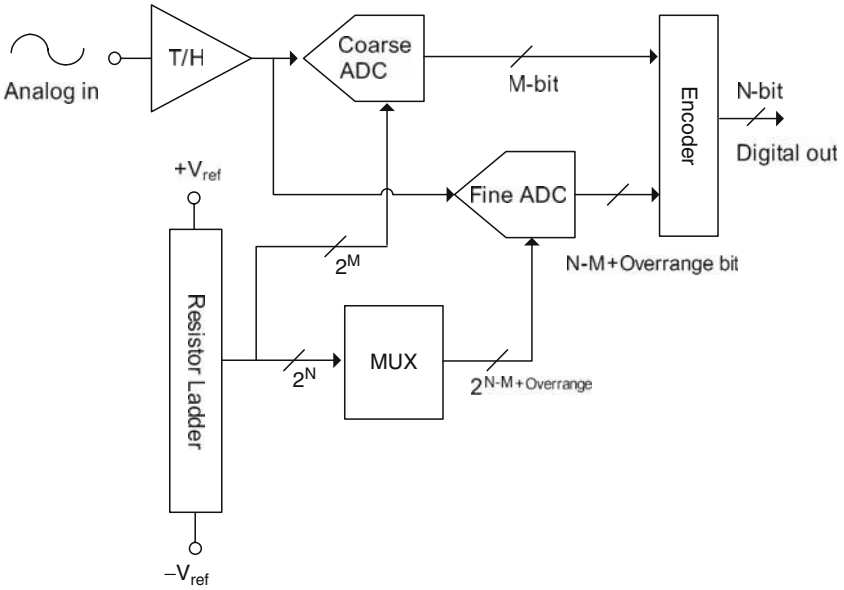

Fig. 1.4 Basic structure of a two-step subranging ADC

A coarse flash ADC first determines a "rough" range of the input voltage, then a "fine" flash ADC digitizes the input voltage using reference voltages that are chosen to enclose the rough range. Although the "fine" ADC needs to have an LSB that is the same as the whole ADC (e.g. 1/256 for an 8-bit ADC), it only needs to digitize the chosen range, therefore the number of comparators is greatly reduced (e.g. flash ADC would require 256 comparators, but around 32 comparators are required for the fine ADC.)

Unlike pipelined ADC, there is no residue signal amplification involved. Analog amplification by the preamp before the comparators of the fine ADC need not be linear and accurate, since only the zero crossing matters. Therefore, open loop amplification by cascading multiple stages of low-gain amplifiers can be used. This property made sub-ranging increasingly popular for fine-line CMOS with gate length $\leq$0.13 μm ([28], [15], [32].)

Since a large number of preamps are required for the fine ADC when the resolution exceeds 8-bit, large die area is still a problem in such case. A 12-bit sub-ranging ADC in 90 nm CMOS reported in [32] has an active area of 4.7 mm^2. When the area of digital portion of the chip shrink to half for every technology node, this kind of area becomes prohibitive in terms of cost.

1.2.4 Successive Approximation

Successive approximation (SA) is one of the earliest ADC architecture. It was used by the first complete ADC commercially became available in 1954. Figure 1.5

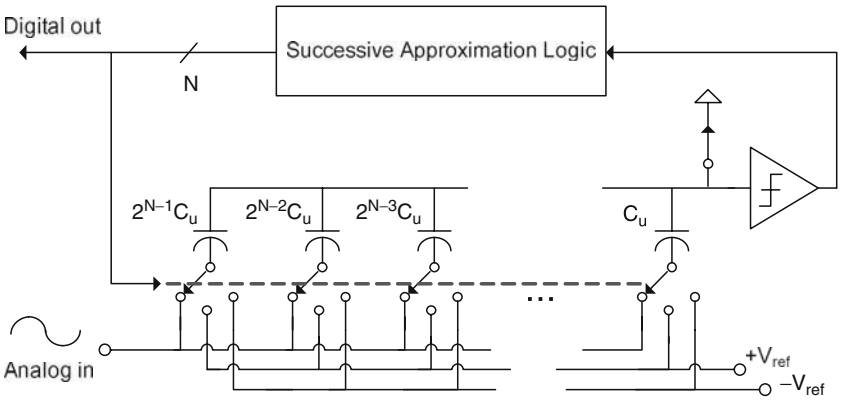

Fig. 1.5 Basic structure of a conventional N-bit successive approximation ADC

shows the basic structure of a conventional N-bit SA ADC. First the input voltage Vin is sampled on all the N capacitors. Next, the bottom plate of the first capacitor ($2^{N-1}C_u$) is connected to $+V_{ref}$ while the rest to $-V_{ref}$, and the top plate switch turns off. The comparator determines sign of the voltage on the top plate, if positive, then the MSB of V_{in} is determined to be zero, and in the next clock cycle, the first capacitor is connected to $-V_{ref}$ and the second one to $+V_{ref}$. The same process continues until all the N bits is determined. In the end, the digital output will switch each capacitor in such a way that the voltage on the capacitor top plate will be very close to zero.

The SA is a very hardware efficient architecture. Although N clock cycles are required to convert N-bit, only one comparator is needed and the rest is "all-passive", i.e. only switches and capacitors, without any linear amplifier. The conversion process can be seen as "digital feedback" as opposed to analog feedback to achieve desired accuracy. All the problems associated with analog feedback, such as phase margin, gain margin and linearity do not exist in "digital feedback", since we have complete control over the process to avoid any oscillation.

The settling of the passive switch-capacitor network can be made much faster than that in OTA-based switched-capacitor circuits, which are used to implement residue amplifiers in CMOS pipelined ADCs and analog loop filters in ΔΣ ADCs.

Figure 1.6 compares the settling time constant τ for the two cases. Except for the sampling switches, all switches are connected to reference voltages that are close to the supply rails. Therefore the gate overdrive voltages of these switches are very large ($V_{dd} - V_t$ is around 1.0 V if low-V_t transistors are used,) making their f_T very close to the maximum value (close to 100 GHz in 0.13 μm CMOS) available for the process. On the other hand, due to signal swing constraints, the speed of settling that involves operational amplifiers is much slower because the gate overdrive of the op-amp input devices must be set to $0.1 \sim 0.2$ V. Other than settling, another delay that limits the speed of "digital feedback" is the SA logic delay. However, in 0.13 μm CMOS a FO4 inverter delay is close to 30 ps and will further improve in finer technologies.

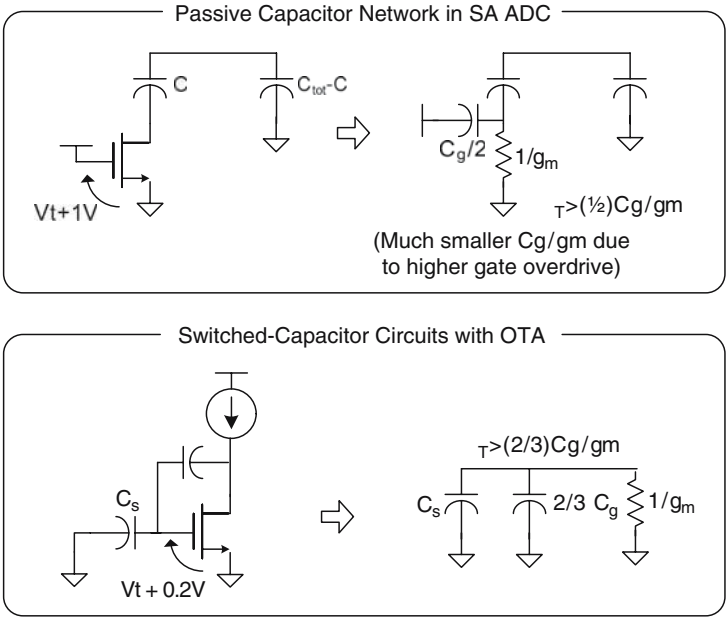

Fig. 1.6 Settling time-constant comparison between passive switched-capacitor network and conventional OTA-based switched-capacitor circuits

One problem with successive approximation is the large size of the capacitor network when the number of bit is large, because the ratio between the largest capacitor and the smallest one becomes so huge. C-2C ladder can be used to reduce the ratio, but it introduces errors due to the parasitic capacitances. SA ADCs that do not use preamplifiers expose the offset of the comparator as the offset of the ADC itself, which is not a problem unless time-interleaving is used. But if time-interleaving is used to increase the sampling frequency as in [14], preamplifiers must be used to reduce the offset mismatch among channels.

1.2.5 ΔΣ ADCs

For medium ∼ high resolution, low speed applications, ΔΣ ADC (Fig. 1.7) is probably the best solution for nanometer CMOS integration. More than 14-bit resolution can be easily achieved in nanometer CMOS processes whereas complicated digital calibration techniques must be used for other ADC architectures such as pipeline. The over-sampling nature of ΔΣ ADCs reduces anti-aliasing filter requirement and capacitors sizes.

Compared with other ADCs, ΔΣ ADCs require a rather massive digital decimation filter with many taps to filter out the shaped quantization noise. This causes more signal delay than other architectures which is unacceptable for some applications.

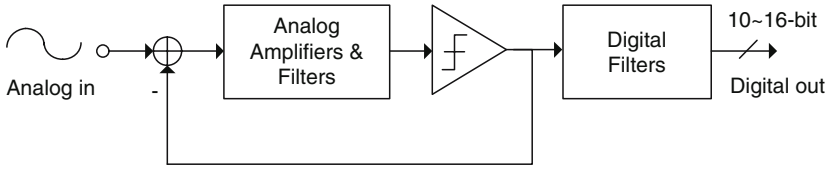

Fig. 1.7 Block diagram of a single-bit ΔΣ ADC

ΔΣ ADCs and SA ADCs are similar in principle because they both use "digital feedback", but the difference is that more analog signal processing is involved in the loop filter for ΔΣ ADCs. When multi-bit feedback and single-loop feed-forward architecture are used, the signal swing inside the loop filter can be reduced and the loop filter linearity requirement becomes much more relaxed. Therefore, nanometer CMOS devices with poor DC gain can be used to obtain high linearity and SNR without any digital calibration. In fact, recent years have seen a steady trend of ΔΣ ADC design moving from single-bit feedback architecture to multi-bit ones, and from high order (5 and even 7 [24]) analog loop filters to lower order, simpler ones such as [21]. The SA ADC can be seen as an ultimate form of this trend, where the digital feedback covers the entire ADC resolution and the analog loop filter disappears completely.

Chapter 2
A 52 mW 10 b 210 MS/s Two-Step ADC for Digital IF Receivers in 130 nm CMOS

2.1 Background

Pipeline ADCs with 10-bit resolution and tens to more than 100 MHz sampling frequency find applications in digital cameras, flat panel displays (to digitize incoming analog video signal) and recently in wireless receivers that employ the digital IF architecture, and in power amplifier linearization.

The digital IF architecture eliminates DC offset and flicker noise problem in direct-conversion architecture. Therefore it enables the use of discrete step automatic gain control (AGC) circuits which are generally more linear than AGC circuits with analog gain control signal that are often used in direct-conversion receivers since the DC offset correction/AC coupling schemes needed in direct-conversion receivers have long settling time [33].

Another benefit of the digital IF architecture is that both the frequency synthesizer and analog channel selection filter can be simplified since fine channel tuning and filtering can be done in digital domain. It eliminates the need for frequency synthesizers with fine frequency steps, which would require fractional-N PLLs to achieve full integration of the loop filter and the VCO, adding complexity to the entire system. Since the fine frequency tuning is done in digital domain and wide-bandwidth PLLs can be used, channel switching can be made much faster [33]. It also eliminates low-pass filters with large time-constants that are difficult to integrate in digital CMOS processes without consuming large die-area.

Digital IF receivers require ADCs with high sampling frequency and high spurious free dynamic range (SFDR)[1] at high input frequencies, such that digital filtering can be used to extract desired signal in the presence of large interferers. If such ADCs can be integrated with the DSP in standard nanometer digital CMOS processes with low power consumption and small die area become available, the overhead of implementing the digital IF architecture can be much reduced. With

[1] Since the desired signal is usually only in a fraction of the Nyquist bandwidth and the digital filtering removes most of the noise power, but certain distortion component of strong interferers may still fall in-band, the SFDR is a more important spec than SNR for this type of ADC

sufficient resolution in the ADC, digital I/Q mismatch calibration algorithms such as [36] also becomes available, making it possible to use a higher IF frequency hence less sensitivity degradation by flicker noise and second-order nonlinearity products. In addition, with high sampling frequencies in the ADC, the requirements of the analog filter stages can be much relaxed, reducing their power consumption and die area. In [33, 35] it was demonstrated that a digital IF receiver achieves better sensitivity and no BER degradation at high input power compared with competing direct-conversion solutions.

2.2 Architecture and Circuits

The pipeline architecture, which has been widely used for high sampling frequency $\geq$8 b ADCs, is difficult to implement in nanometer CMOS processes due to reduced transistor linearity, voltage gain and headroom. This is mainly because accurate residue amplification is needed. Techniques such as multi-stage amplifiers and nested gain boosting must be used for the op-amp, which limit the sampling frequency. On the other hand, as described in Chapter 1, two-step ADCs do not require linear residue amplification,[2] and is an attractive architecture for nanometer CMOS processes. Combined with well-matched small value interconnect capacitors available in these processes and offset cancellation techniques to realize low-power flash ADCs, they can achieve higher speed and lower power consumption for 10 b resolution ADCs, which is demonstrated in this chapter.

Two-step subranging ADCs generally consist of a "coarse" flash ADC that determines a rough range of the input analog level and switches reference levels used by a "fine" ADC (FADC). The FADC amplifies the input signal minus reference signal to find the point at which the sign changes with sufficient accuracy.

Figure 2.1 shows a block diagram of the proposed ADC. The difference from a conventional subranging ADC is that the 6 b FADC, which determines the performance of the entire converter, does not use resistor reference ladder and that there is no multiplexer that chooses a sub-range in the reference ladder to be used by the FADC. Instead, two SAR-like 5-bit feedback capacitor DACs that work also as passive S/Hs are used to generate Vin-(CADC output)-1 and Vin-(CADC output)+1. The FADC uses further capacitive interpolation to resolve 64 levels out of these two input boundary voltages, converting the 6 LSB (Fig. 2.2).

These boundary voltages are generated by the appropriate DAC input codes and an additional LSB capacitor in the DAC which shifts the boundary in such a way that in the presence of smaller than $\pm$0.5 LSB comparator offset in the 5-bit CADC, the two boundaries still have opposite sign, i.e. the FADC output does not clip, enabling correct 10-bit conversion after adding the capacitor DAC input with the FADC output.

[2] As described in section 2.2.4 if aggressive interpolation is used amplifier linearity still matters

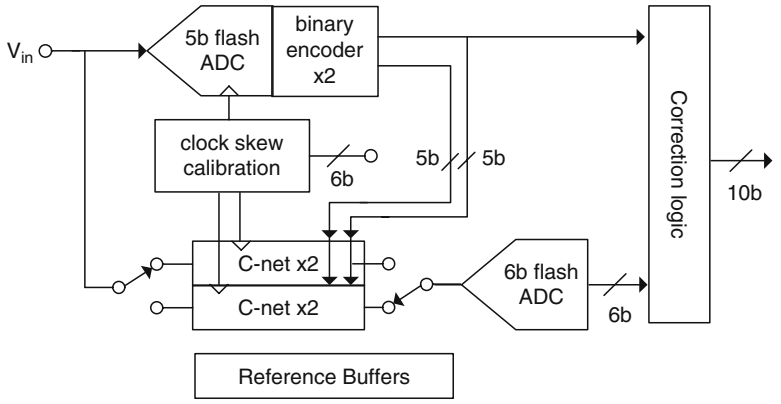

Fig. 2.1 Overall block diagram of the two-step ADC

Obvious advantages compared with conventional resistor ladder + multiplexer subranging ADC are (1) faster setting due to high turn-on voltages of the switches and (2) no reference resistor ladder which drives the FADC. Since the FADC determines the noise floor of the entire ADC, they require large sampling capacitors or preamplifiers to lower noise and/or offset. Therefore they typically present significant input capacitance, and much power must be used in the resistor ladder to satisfy DC bowing as well as settling speed requirement. Whereas in the proposed scheme, essentially only two reference voltages, i.e. $V_{ref}+$ and $V_{ref}-$ are used to drive the FADC through capacitive interpolation. These reference voltages are generated using gain-boosted source follower with large MOS capacitors at the output (the same circuit used in the SAR ADC described in Chapter 3, Fig. 3.6). The gain boosting allows orders of magnitude smaller current than what would be required in a resistor ladder to generate $\sim 2\Omega$ impedance at low frequencies. Sufficient capacitance is connected at the output to ground to provide similar impedance at high frequencies above the gain-boosting loop bandwidth. Unlike resistor ladder, since there are only two voltage levels, die area consumed by these large capacitors can be tolerated.

Another advantage (which generally applies to FADC with aggressive interpolation) is the kT/C noise. In conventional subranging ADCs, the FADC would often use more than two inputs, such as in [8]. The benefit is that a less aggressive interpolation can be used, which is more tolerant of preamp nonlinearity. For instance, if only $2\times$ interpolation is used, ignoring preamp offset, then the interpolated voltage is always linear regardless of preamp linearity. With many FADC inputs, one of FADC's many sampling capacitor that happens to handle the zero-crossing must produce sufficiently low kT/C noise which becomes the thermal noise floor of the entire ADC. Because each must be sized this way, the FADC presents large total load to the input and the reference ladder — in [8] each FADC unit sampling capacitor is 200 fF, resulting in 5 pF total FADC sampling capacitance and large ladder power consumption. In the proposed scheme, kT/C noise of each 5-bit binary weighted capacitor network's total capacitance determines the thermal noise floor

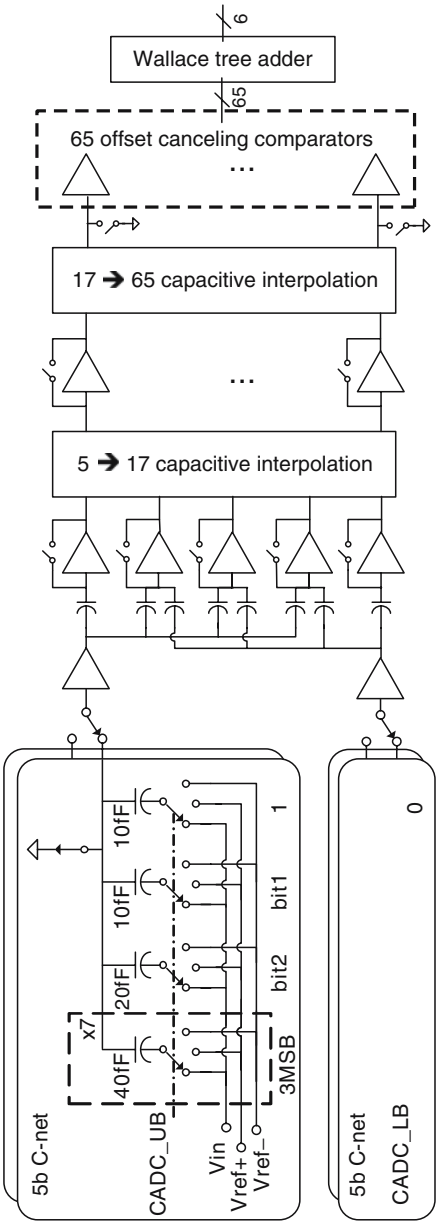

Fig. 2.2 Block diagram of the capacitor-sampling-network/5 b-DAC and the 6 b FADC

of the ADC,[3] assuming sufficient gain in the 1st stage preamps (so that kT/C noise of the interpolation capacitors can be negligible compared with that of the sampling capacitors.) Therefore, the FADC input load is much less (10 fF LSB for the 5 b C-DAC, 320 fF sampling capacitor in total vs. 5 pF with less kT/C noise).

2.2.1 Capacitor Sampling Network / 5b-DAC

Figure 2.3 is provided to give a more detailed illustration than by Fig. 2.2 of the critical signal path from the 10 b two-step ADC input to the 6 b Fine ADC input. It shows one side of a fully differential circuit, which further has two identical instances, P and Q, that are time-interleaved to allow CADC regeneration and encoder settling (see Fig. 2.4). Conventional bootstrapped switch is used to bootstrap the gate as well as the bulk (thanks to availability of deep-N-well in this process) of the NMOS sampling switches connected to the bottom plate of the C-array, to ideally Vdd+Vin and Vin respectively, such that there is no signal dependent g_m (g_{on}) and g_{mb}. Both gate and bulk are pulled down to ground when Φ1d goes low.

Note that although there are multiple bottom plate sampling switches, each connecting to different capacitors in the 5 b C-DAC, only one bootstrap circuit is necessary. Since the gate-to-source and drain capacitance C_g of the switch has some voltage coefficient ($C_{ox}WL$ is an approximation), a linear metal-metal capacitor C_0 that is much larger than C_g should be used by the bootstrap circuit to ensure that despite charge sharing between C_0 and C_g when C_0 connects between Vin and the gate, V_{gs} is substantially signal independent and remains close to Vdd. PSS simulations were run while sweeping the value of C_0. It was found distortion improves until C_0 reaches $2 \sim 3$ pF, therefore C_0 was chosen to be 3 pF, becoming the biggest capacitor except for MOS decoupling caps in this design.

It is a well know technique ("bottom-plate sampling") to turn off the bottom-plate switch slightly after the top-plate switch is turned off. This way, the top-plate switch decides the sampling instant. Although the charge injected by the top-plate switch will add upon sampled signal, since the top plate stays substantially at *vicm* all the time,[4] the charge injected when it turns off has little signal dependency.[5] Therefore it can be cancelled as common-mode by subsequent stages. When we try to reduce something through cancellation, it's natural to also try to reduce its absolute value — the top plate switch should be made as small as possible to reduce the amount of charge injection.

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[3] This is the worse case, if the zero crossing falls in the middle, then the kT/C noise is actually 3 dB less because the sampled noise of the upper and lower bounds are not correlated while the signal is

[4] In this design, which uses small common-mode switches, we must assume that the input has limited common mode movement for this to be true

[5] The only dependency comes from the difference of impedance looking into either side of the switch which decides what percentage of channel charge is injected to the sampling cap

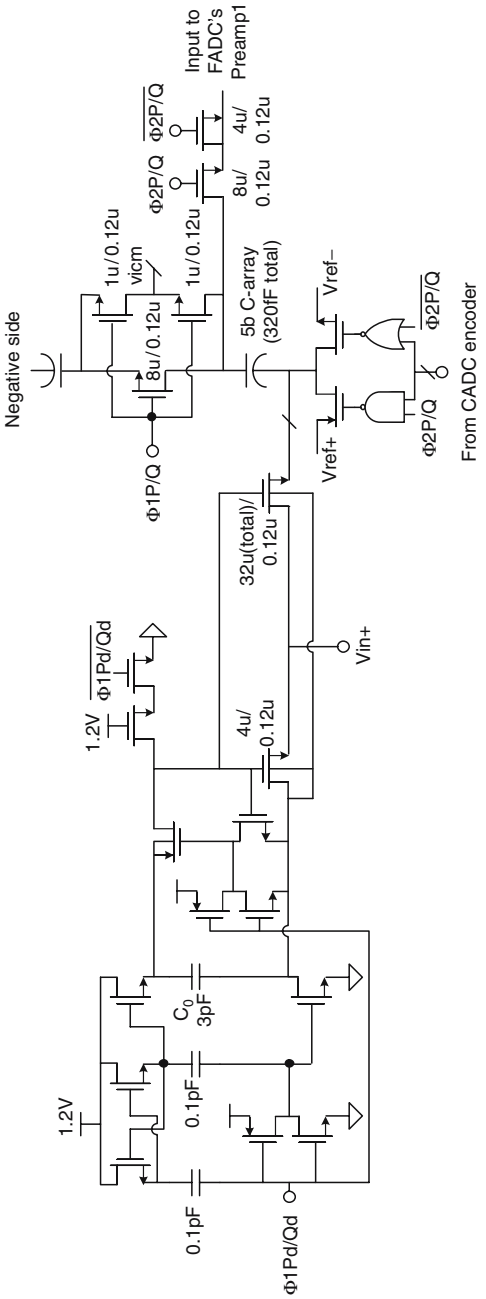

Fig. 2.3 Simplified schematic of the FADC sampling network (fully differential, one side shown)

However, the large on-resistance of a small switch presents two problems. One is long settling time constant, which will affect linearity if the settling is not completely linear because of nonlinear switch on-resistance. This problem improves with lower sampling frequency. Another, potentially more serious problem for sub-sampling application is that the current $2\pi f_{in} C_s vin$ will generate a voltage drop (as much as ~5 mV for f_{in} at 150 MHz) on the top-plate switch which will never settle. This not only limits the bandwidth of the ADC but also eats into the allowed ±0.5 CADC LSB (8 mV) correction range if $C_s R_{on}$ of the FADC and CADC does not match, because FADC and CADC would be sampling two signals with different amplitude and phase.

To achieve a favorable trade-off between R_{on} and charge injection, the top plate switch consists of a single low-Vt NMOS connecting between the positive and negative capacitor top-plates, and two 8× smaller common-mode switches connecting to *vicm*. Compared with having one switch per each side connecting to vicm, for the same amount of charge injection R_{on} is halved. The price paid is slower common-mode settling, which means charge injected by top-plate switch will have dependency on signal common-mode if it changes too fast.

Since the top-plate switch has already been turned off when the bottom plate switch turns off, charge injection by the bottom plate switch will not be sampled and is usually ignored in conventional CMOS S/H designs. However, for the proposed type of two-step ADC, the bottom plate switch charge injection also matters. This is because even tough the top-plate switch is already off, a part of injected charge by the bottom-plate switch will charge the parasitic capacitor (to ground) at the top-plate, such as the C_{db} of the top-plate switch. When the capacitor is connected to the input of FADC, this charge will share with the input capacitor of the first stage FADC preamps and adds on top of the FADC input. This has not been a problem in conventional CMOS S/H, because sampling capacitor top-plate connects to a virtual ground at the OTA input, hence the charge held by parasitic cap at the sampling cap top-plate will simply be removed and the state just before the top-plate switch turns off restored when the OTA settles. However, the top-plate will be floating during Φ_2 in the proposed architecture and does not always settle to ground (it only settles to the quantization error of the CADC). For this reason (1) the bottom plate switch should use low-Vt to reduce its size per on-conductance, and (2) bootstrap circuit should be designed with big C_0 to reduce signal dependency of charge injected by the bottom plate switch.

2.2.2 Conversion Timing Diagram

Figure 2.4 shows the timing diagram in order to give a better idea how the input is converted. To allow high SFDR at high input frequencies over Nyquist frequency (sub-sampling), it is best to use all-passive sampling network. That is to say, the preamp should not be involved during the tracking phase. This means that the CADC needs an extra half-clock-cycle for the reference ladder to settle before it can latch

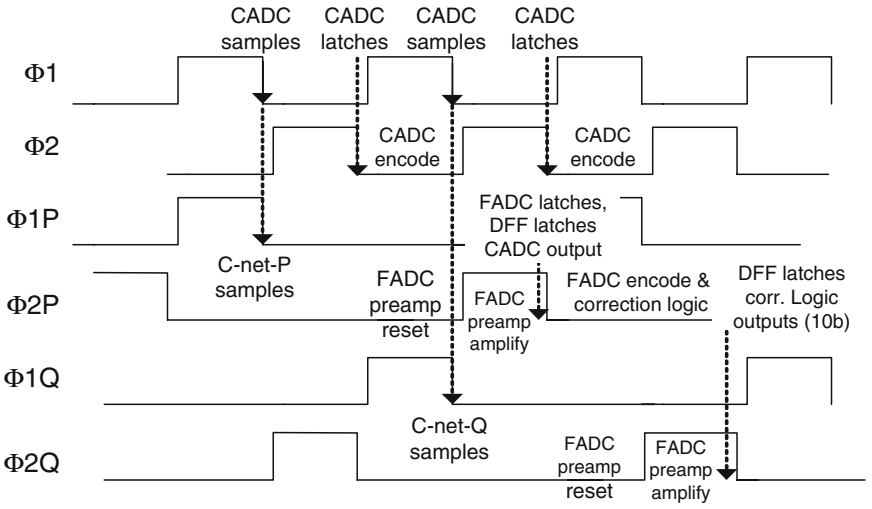

Fig. 2.4 Timing diagram of the two-step ADC

and starts to regenerate. Then the thermometer-to-binary encoder must convert the 30 comparator's output to 5 b binary code, and subsequently the 3 MSB to 7 b thermometer-code for the 5 b feedback C-DAC (thermometer-coding the MSBs in the C-DAC achieves less discontinuity at MSB transition (e.g. 011 to 100) in the presence of capacitor mismatch, hence better linearity for the entire ADC).

To allow time for the CADC regeneration and these thermometer-to/from-binary converters, the FADC input is held by 1 clock cycle. This is accomplished by time-interleaving two S/H (P and Q), each one samples input at the same time when CADC samples the input, and is connected to FADC input only after the other one finishes sampling input (1 clock cycle later), as shown in Fig. 2.4. As a result, half clock cycle is allowed for the CADC latch to regenerate and the binary encoder to settle. As shown later in experimental results, there has been a critical mistake in this design not to put a latch stage at the output of the CADC binary encoder which is opaque when $\Phi 1$ is high and transparent when $\Phi 1$ goes low. With the small added clk-Q delay this latch would have isolated the CADC binary encoder during its settling, and reduced both digital switching power and coupling of switching noise to sensitive analog signals such as ADC input and reference (although reference is only used during $\Phi 2$ so it is less a problem.) This mistake prevented the ADC to achieve sufficient performance for > -40 dBFS input (when the CADC output starts to toggle) at 300 MS/s, which is the sampling speed for which the ADC was originally designed.

2.2.3 Sampling Clock Skew Calibration

The problem with time-interleaving two S/H is that sampling clock timing skew between the two will cause tones to appear at $f_s/2 - f_{in}$. Also, the slightest gain and

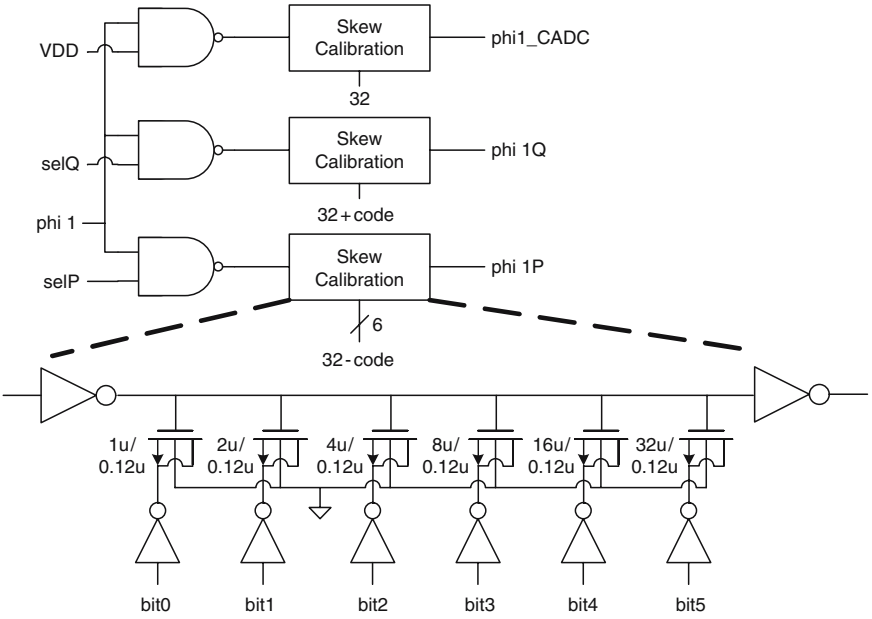

Fig. 2.5 Clock skew calibration circuits

offset mismatches generate tones at $f_s/2$ and $f_s/2 - f_{in}$, which can easily be much larger than tones from harmonic distortions, which are measured below -70 dBc in this ADC. There are known simple digital methods based on ADC output statistics to continuously correct gain and offset mismatch between time-interleaved channels, such as [22]. Correcting sampling timing error by digital post processing, however, involves much more complicated signal processing. Therefore, an analog means for calibrating out sampling timing mismatch is provided in this design.

As shown in Fig. 2.5, there are three 6-bit digitally controlled delay lines (0.2 ps LSB, FS of $\pm$14ps according to simulation) that delay sampling clock to FADC P/Q paths S/Hs and CADC's S/H. The delay line is implemented by turning on and off MOS channel capacitors that load the inverter output. It allows more compact layout and smaller, more controllable adjustment steps than switching in and out metal-metal capacitors.

According to simulation, the relationship between tuning code and delay has much 2nd order nonlinearity, i.e. when the code is small the adjustment step is also small, and vice versa. By applying differential tuning codes to P and Q channel delay line, this nonlinearity can be cancelled in terms of the timing difference. Measurement result verifies this prediction (section 2.3.2).

Since the application is digital IF receivers, we can expect that powerful DSP is available to process the ADC output. At start up, a sine wave (or any periodic waveform that is not in harmonic relation with the sampling clock) is applied to the ADC input and FFT is performed on even and odd ADC outputs to find the phase

difference of applied tone in each output. The FFT will also find the frequency of the applied tone and hence the ideal phase difference when there is no sampling timing error. A SAR state machine can then find the right tuning code.

Since the delay of the skew calibration circuit varies as much as 60 ps (larger than adjustment full-scale) over fast and slow process corners, a third delay line with fixed input (32) is used for the sampling clock to CADC. This allows CADC sampling clock to substantially track the FADC sampling clock over process variation, as shown in Fig. 2.6.

2.2.4 6 b Fine ADC

As shown in Fig. 2.2, the FADC receives two (differential) inputs from the capacitor network, one being positive the other negative, and finds where the zero crossing occurs with 6-bit resolution. It uses capacitive interpolation [30] rather than resistive interlation as in conventional flash ADCs because (1) there is no need to worry about edge effect, and (2) interpolation capacitors also function as input and output offset storage capacitors to completely cancel offset of the preamps.

Figure 2.7 shows schematic of preamps used in each stage. For stage 1, since there is no input capacitor to store the offset, output offset storage is used where the input is shorted during reset phase and the offset is stored solely on the output capacitor. To improve settling speed during reset phase, when the interpolation capacitor is charged, it's preferable that the output impedance is low, but during signal amplification phase, where the next stage's input capacitor, which is much smaller than the interpolation capacitor (otherwise gain will be lost by capacitive voltage division) is charged, it's preferable that the impedance is high to get more gain. To achieve this, a switch is used to diode-connect a PMOS only during reset phase, and the PMOS becomes current source in amplification phase. Proper gate bias of this PMOS is established during reset phase.

The kT/C noise of capacitor C_1 referred to input is

$$\frac{kT}{C_1}\left(\frac{g_{mp}}{g_{mn}}\right)^2.$$

Therefore, g_m of the PMOS should be made much smaller than the input g_m, otherwise C_1 that is much larger than the 320 fF sampling capacitor is needed to avoid degrading SNR much. Small PMOS g_m is however in conflict with the purpose of the design, i.e. to improve settling speed during reset phase, so a trade-off is made. To reduce noise, in addition to C_{gs} of the PMOS itself, a large PMOS capacitor has been added. When C_1 is large, large switch must also be used, otherwise the impedance becomes too much inductive. This can be said for reset switches for stage 2 and 3 preamp as well, and the 2nd pole caused by the on-resistance of the reset switch and C_{gs} is a cause of ringing during reset phase. Simulation is run to determine the right switch size that still allows complete settling (Fig. 2.8).

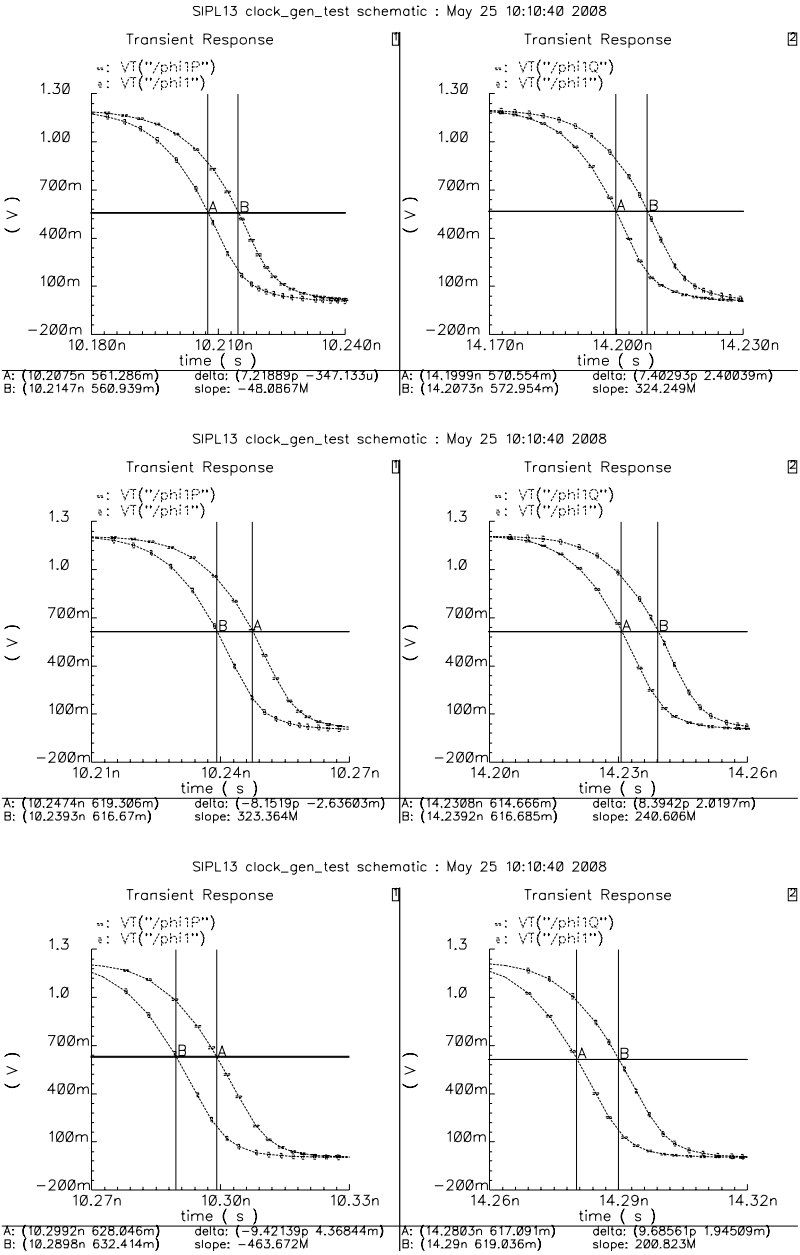

Fig. 2.6 Simulated clock edges of ϕ_1, ϕ_{1P} and ϕ_{1Q} for fast, nominal and slow process corner with code at full-scale

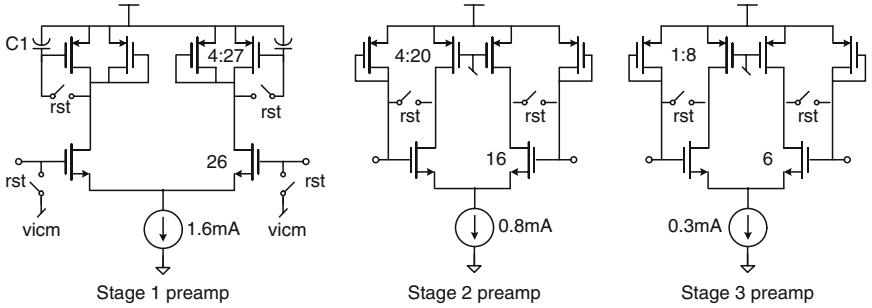

Fig. 2.7 FADC's preamplifiers

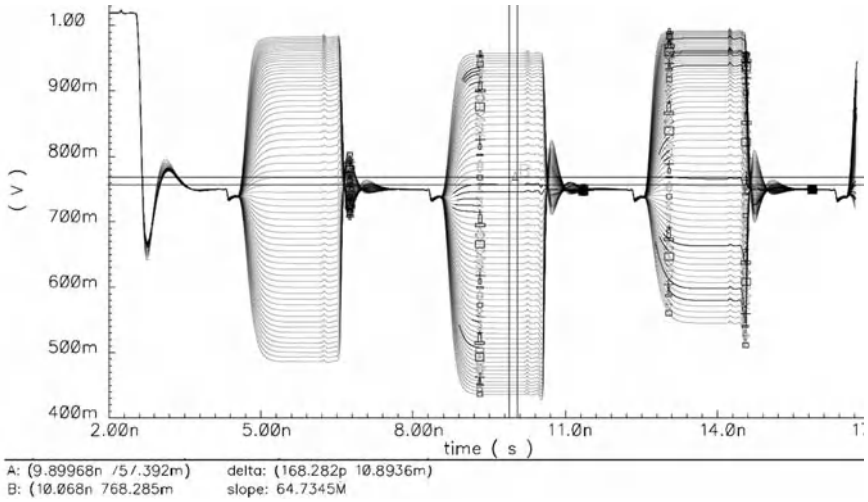

Fig. 2.8 Simulated 65 input waveforms to each stage-4 preamp

The design of stage 2 and 3 preamp is simpler, because offset storage capacitors are available at both input and output, so by simply connecting the input and the output during reset phase, the offset is stored and cancelled completely. A common misconception is that while output offset storage can completely cancel offset, input offset storage is only effective when the amplifier has high gain. However, if there are offset-storage capacitors connected at both input and output, each capacitor would store the voltage x calculated as follows:

$$-A(x-V_{os}) = x \rightarrow x = \frac{A}{A+1}V_{os},$$

where A is the amplifier's gain and V_{os} is the input referred offset. In amplification phase, assuming both the input and output offset storage capacitors are much larger than amplifiers' input capacitances C_{gs}, signal appearing at next stage's input is

$$-A[(V_{in}+x)-V_{os}]+x = -AV_{in},$$

therefore the offset is completely cancelled regardless of preamp gain. The advantage of input/output offset storage over output offset storage is power efficiency. During reset, when the interpolation capacitors are charged, the impedance is low (1/gm), and during amplification, when the next stages' input capacitances, which is much smaller than the interpolation capacitor are charged, the impedance can be higher, hence less current / larger load resistance can be used to reduce power.

Although aggressive interpolation (with more than one interpolated points per section) has benefits such as low kT/C noise per ADC total input capacitance as mentioned previously and smaller number of stages necessary to reach 65 outputs, a caveat is that the interpolated outputs are not guaranteed to be evenly spaced when the amplifier is not perfectly linear. For example, if the amplifier's transfer function has 3rd order nonlinearity (assuming 2nd order nonlinearity is largely cancelled by the fully differential circuit), i.e.

$$V_{out} = a_1 V_{in} - a_3 V_{in}^3$$

then with 2→5 interpolation and the inputs being 3 and -1, the 4th interpolated point should ideally be at 0 but would be at

$$V_{out,4} = (3a_1 - 9a_3) \times (1/4) + (-1a_1 + a_3) \times (3/4) = -1.5a_3.$$

The more unbalanced the positive and negative inputs are, the bigger the error becomes for 3rd order nonlinearity. Fortunately, unlike pure flash ADCs, in the proposed two-step ADC the linearity requirement of the FADC is greatly relaxed by the 5-bit feedback C-DAC which reduces the FADC input signal swing by ideally 32 times. This is the same principle as multi-bit ΔΣ ADCs or pipeline ADCs with multi-bit first stage, where the amplifier linearity is relaxed due to reduced signal swing. However, it is necessary to quantitatively verify how much linear the FADC must be, in order to properly set the gain and apply open-loop linearization to the preamps if necessary.

Figure 2.9 shows a design procedure used to verify if the FADC preamp design is sufficiently linear with a given input full-scale, without lengthly transistor level transient simulations. Firstly preamps in stage 1–3 whose linearity is a concern are simulated with DC sweep. The results are captured with sufficient resolution and imported into Matlab, where a behavioral model of the two-step ADC is run with a ramp input. The matlab program uses the captured DC simulation result to calculate the voltage at each internal node of the multi-stage interpolation FADC, and finds the 10-bit ADC output. The code density histogram is taken of the output to find DNL, which is further integrated to find INL of the 10-bit ADC. Although transient simulation with ramp input can obtain the same result, it would take much longer time to simulate, lengthening FADC design cycle.

As shown in the figure, assuming zero CADC offset and zero offset of the FADC preamps (although the offsets are cancelled, they will still affect preamp transfer function), with 1 Vpp differential ADC input full-scale the INL can be ±0.1 LSB. But when the FS increases to 1.6 Vpp, differential, the INL degrades to ±0.5 LSB.

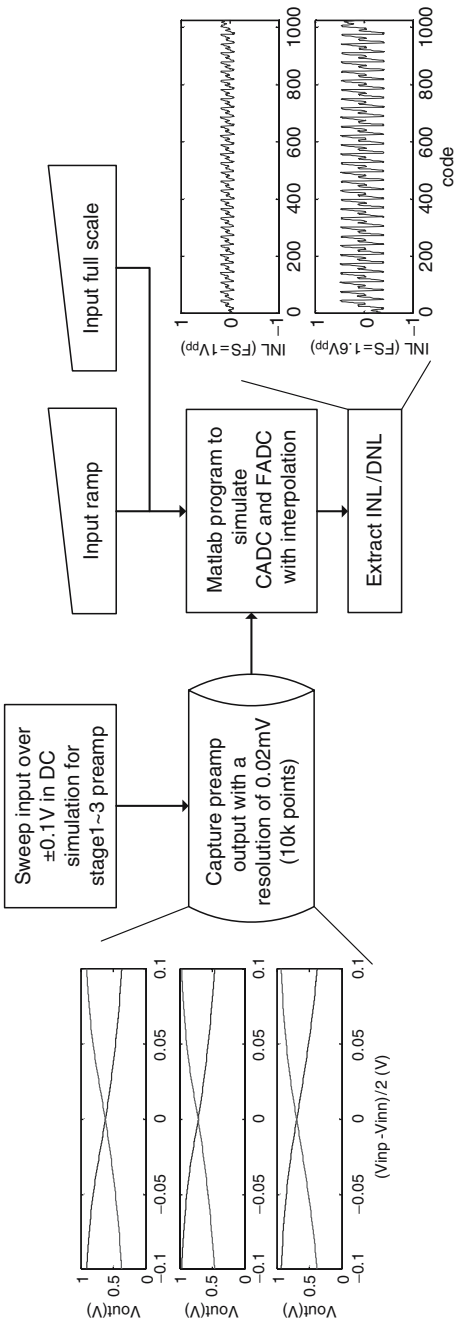

Fig. 2.9 A scheme used to verify if FADC preamps have sufficient linearity

2.2.5 Offset Canceling Comparator

The use of positive feedback to boost the gain of a preamp has become a popular technique in flash-type ADCs in recent years [32], [37]. Because of this technique, less number of preamp stages, and/or smaller comparators can be used, resulting in much power reduction. However, since the comparator itself already uses postive feedback, it seems redundant to have both a preamp with positive feedback and a conventional comparator. In this design, an "offset canceling comparator" is proposed which combines the function of the two. The output is connected to inverters and a slave latch to hold the decision when the comparator resets.

Figure 2.10 shows the proposed offset canceling comparator together with the stage 4 preamp. When "rst" is high, the offset of the preamp is stored, while the comparator regenerates. When "rst" goes low, the preamp starts to amplify the signal and settles before "latch" goes high, at which point the signal is applied to the regenerative comparator. While "latch" was low, the offset of the comparator is also stored and subsequently cancelled when "latch" goes high. The signal input to the regenerative comparator is a pulse rather than a step asis the case with conventional comparator. The regeneration time domain waveform is given by

$$\begin{aligned} & L^{-1}[\frac{1}{\tau s-1}(\frac{1}{s}-\frac{1}{s}e^{-sT})] \\ & = [(e^{t/\tau}-1)-(e^{(t-T)/\tau}-1)]u(t) \\ & = (1-e^{-T/\tau})e^{t/\tau}u(t), \end{aligned}$$

where T is the pulse width and τ is the regeneration time constant. We can see $T \sim \tau$ is enough not to slow down the regeneration much compared with conventional comparators where the input is a step.

The stage 4 preamp differs from stage 2 and 3 preamp in that it uses entirely PMOS current source load rather than diode connected load to increase voltage gain. Since there is no more interpolation after stage 4, there is no worry about linearity so the design is mainly focused on achieving high gain.

2.2.6 5 b Coarse ADC

The purpose of the 5 b coarse ADC is to reduce the signal swing at the input to the FADC to relax its linearity requirement. As long as the 5 b C-DAC code is such that the two FADC inputs are not both positive or both negative (in which case the FADC cannot find zero crossing and clips,) then the noise/mismatch of the CADC does not affect the accuracy of the entire ADC at all.

Figure 2.11 shows simplified schematic of the CADC. The allowed error for the FADC not to clip is ± 0.5 LSB of CADC. This is about 8 mV. kT/C noise of the 10 fF sampling capacitor is 0.64 mVrms so it should not affect performance most of the time. Each sampling capacitor is only 10 fF, and the input capacitance ($C_{gs}+C_{gd}$) of

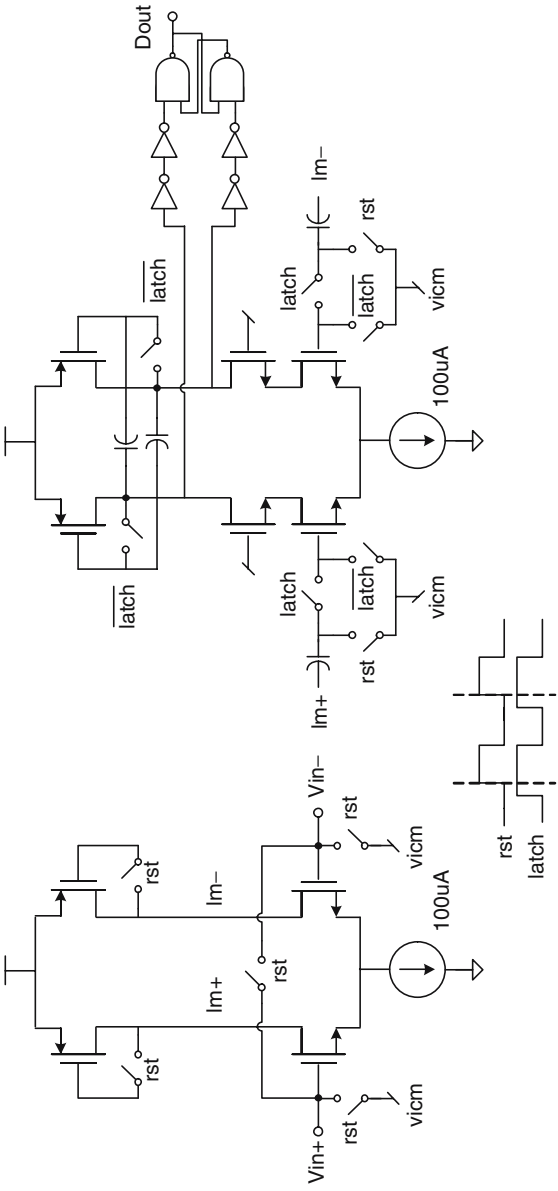

Fig. 2.10 Simplified schematic of the proposed offset canceling comparator used by both FADC and CADC

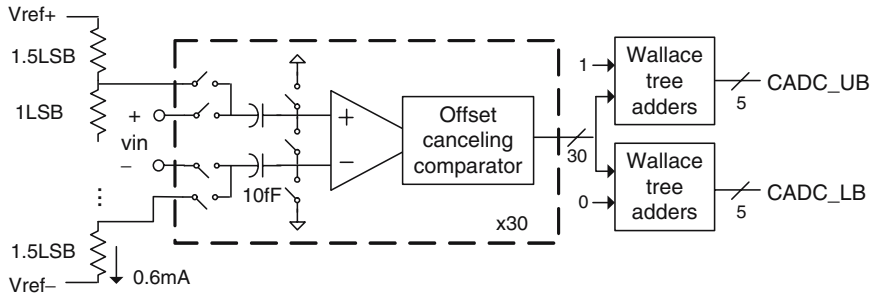

Fig. 2.11 Simplified schematic of the 5 b CADC (fully differential, one side shown)

the offset canceling comparator in reset which the resistor ladder eventually drives is even less (∼2 fF according to simulation). The very small load on the ladder not only speeds up its settling but also reduces long-term / DC error generated by bowing due to static current drawn from the ladder. The ladder consumes only 0.6 mA (each section is 27 Ω), much less current than those in conventional subranging ADCs that drive FADC, for example 15 mA is used in [37].

Since the input of the offset canceling comparator is reset to *vicm* each time, and subsequently driven up to $V_{ref}[n] - vin$, there is a finite amount of DC current drawn from the *nth* reference point of the ladder, which can be approximated as $(V_{ref}[n] - vin - vicm) f_s (C_{gs} + C_{gd})$, where f_s is the ADC sampling frequency (designed for 300 MHz). The situation is equivalent to have 1/300 MHz/2 fF ∼ 1.7 MΩ resistors connecting from each ladder node to $+vin - vicm$ and $-vin - vicm$. if we assume ADC input *vin* is entirely differential mode, then it can be shown that the ladder bowing caused by $+vin$ will cancel with bowing caused by $-vin$, so we can disregard the *vin* term. Simulation shows the worst case ladder bowing caused by these 1.7 MΩ resistors connecting to *vicm* is about 69 μV. Although much smaller current could be used to make ladder bowing small enough, the 0.6 mA current is designed to enable complete settling. It is only when very large decoupling capacitors are connected at each ladder node that bowing alone is the concern.

2.3 Experimental Results

The ADC is fabricated in UMC 1P8M high-speed digital 0.13 μm CMOS process without MIM capacitors. All capacitors are either interconnect capacitors or MOS gate capacitor. It uses only thin-oxide, 1.2 V devices. Figure 2.12 shows the layout. At the top of the layout there are 65 offset canceling comparators, followed by capacitors for interpolation and offset storage and 4 stages of preamps, among which are MOS capacitors for various bias signals. At the middle of the layout are the capacitors for the two S/H and 5 b feedback DAC (SAR capacitor network), below which are the switches and clock buffers. At both sides of the switches are large

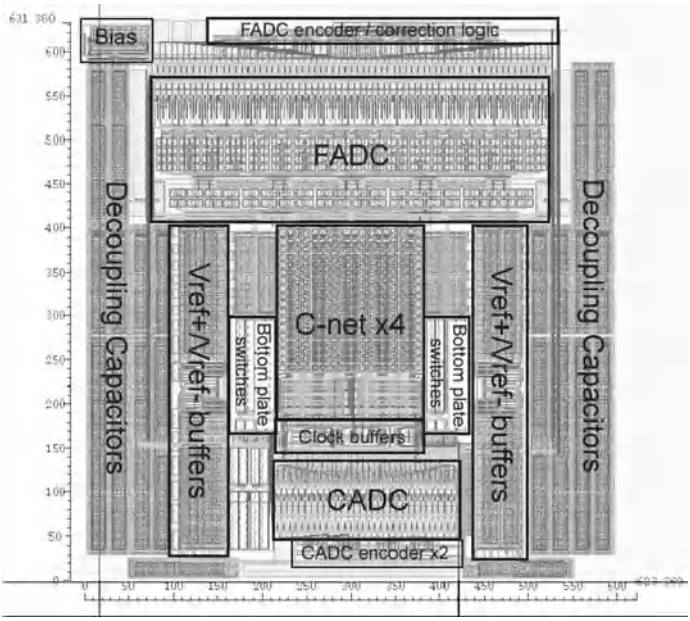

Fig. 2.12 Layout of the two-step ADC

(>2 pF) metal-metal fringe capacitors to drive the bootstrapped bottom plate sampling switch. At the bottom part are the 5 b coarse ADC and the resistor ladder. At both sides of the DAC/CADC are the reference buffers generating $V_{ref}+$ and $V_{ref}-$. The rest of the layout area is filled with MOS capacitor used for supply decoupling.

A die photo graph is shown in Fig. 2.13. The two-step ADC occupies 0.38 mm^2 including decoupling caps on either side. Despite the use of two 5 b and 6 b flash ADCs, the die area is very competitive with existing 10 b pipeline ADCs which uses multiple residue amplifications to save the number of comparators (see Table 2.2). This is largely because of the use of offset-canceling comparator and capacitive interpolation which minimized the size and number of preamp stage of each flash ADC.

2.3.1 Test Setup

Figure 2.14 illustrates the test setup. It uses off-chip baluns to convert clock and signal input to differential and directly applies to the ADC. For clock input, the ADC uses the same receiver amplifier circuit as the PLL described in Chapter 4 section 3.3. This receiver amplifier integrates 50 Ω matching resistor and provides common-mode rejection as well as sharpens the clock edges to CMOS square-wave.

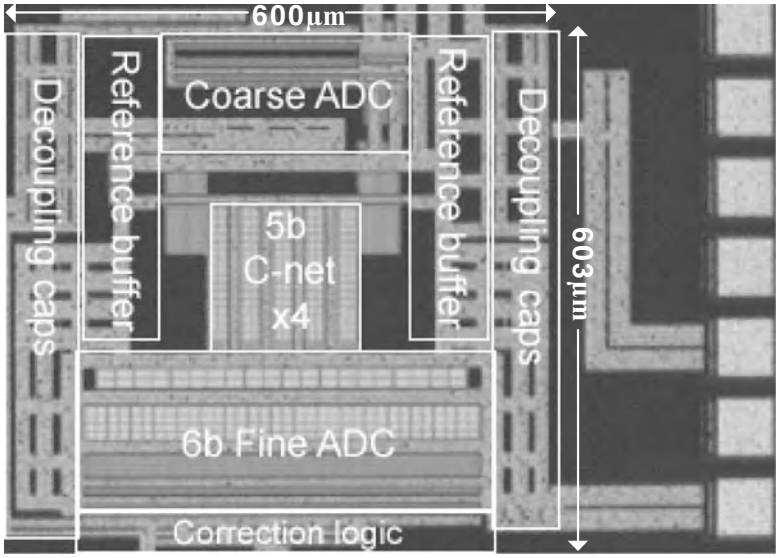

Fig. 2.13 Die photograph

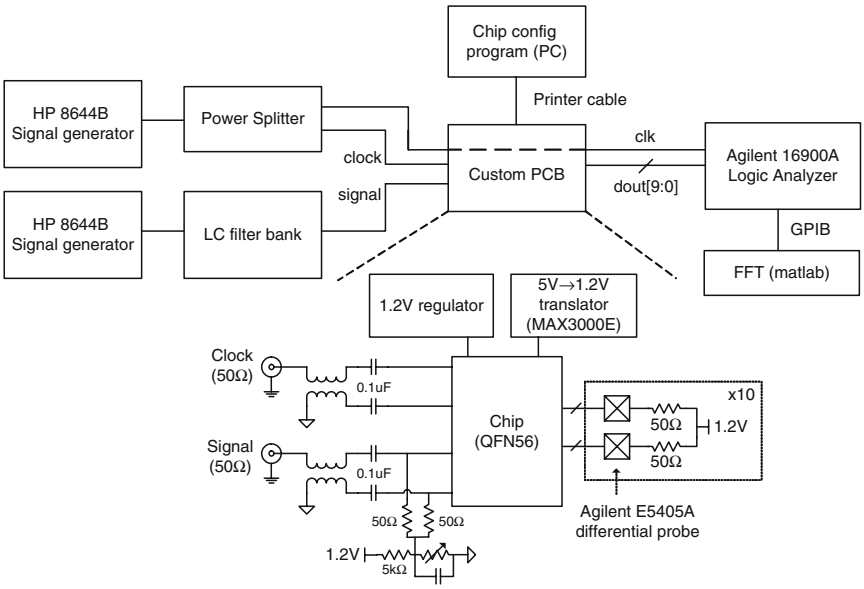

Fig. 2.14 Simplified block diagram of the test setup

For signal input, the ADC has relatively high effective impedance of around 5 kΩ (CADC and FADC's S/H each contributes 10 kΩ) at 300 MS/s. A driver amplifier is not used and 50 Ω 0603 chip resistors are placed on PCB for termination. The input

common-mode can be adjusted, desirably to the common-mode of on-chip reference voltages, so as to avoid any DC current from/to the on-chip reference buffers. However no difference in performance was observed while varying common-modes between 0.4 V to 0.8 V.

Unlike the SAR ADC in Chapter 3, capturing ADC output has been very straightforward, thanks to the availability of a logic analyzer with differential probe that can handle up to 600 MHz state data capture, and provides features such as eye finder which can correct skew and offset among the output bits and clock. The ADC output is double terminated by 50 Ω on-chip and off-chip resistors, and driven by NMOS differential pairs with 10 mA bias current each.

Figure 2.15 shows the evaluation PC board, which measures 3 inch by 3 inch. The PCB was greatly simplified thanks to the serial configuration interface described in Chapter 3 section 4.2, and ADC is directly connected to the 50 Ω termination resistors and no driver op-amp has been used. The die (1.5 mm × 1.5 mm) is packaged in a 7 mm × 7 mm 56 pin QFN package which was directly soldered on to the PCB to minimize package parasitics. Nevertheless, because the die is very small compared with the package, long bonding wire cannot be avoided which could have limited the SFDR for high input frequency.

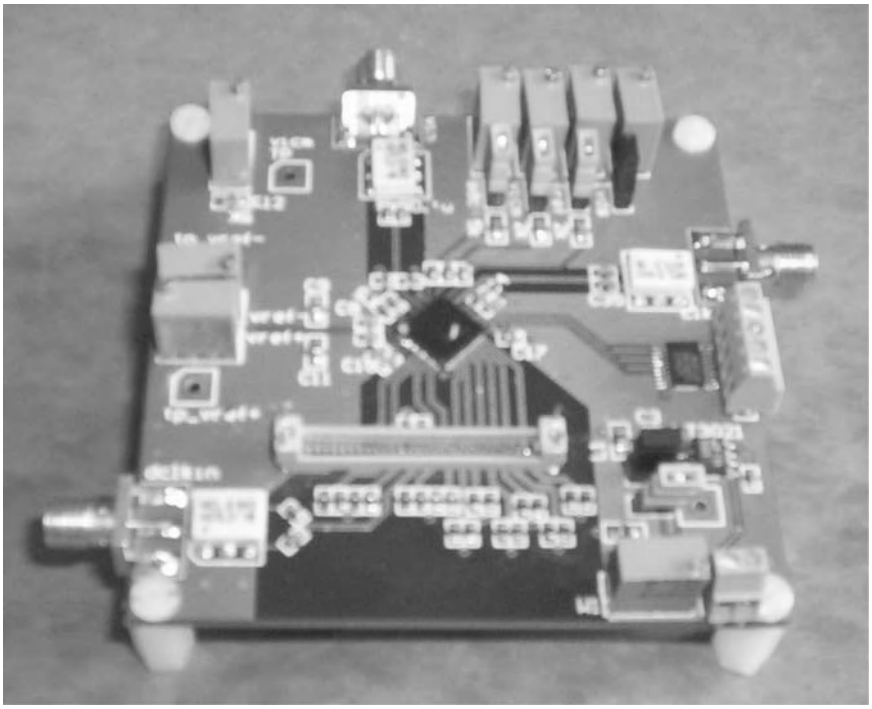

Fig. 2.15 Photograph of the evaluation PCB

2.3.2 Characterization of the Clock Delay Line

Before measuring the ADC, we need to characterize the clock delay line (cf. section 2.2.3) that corrects for sampling timing skew between the two S/H, in order to find the right delay line code. Measurement results show that the same code ($10 \sim 14$ for the tested part) can be used for different sampling and input frequencies, and changed little if at all, over days of measurement and temperature variation (after applying cooling spray). It can be concluded that the majority of the timing skew is caused by component mismatch and layout asymmetry, and is affected very little by operating conditions and temperature variations. This means for most applications timing calibration can be performed at power up and fixed thereafter.

To characterize the delay line, a high frequency (230 MHz) near full-scale input is applied (such that a small difference in sampling instant translates to larger voltage difference, making the measurement less sensitive to quantization and other noise) to the ADC input and FFT is performed on the even and odd ADC outputs to find phase difference of the applied tone. The more points the FFT uses, the more accurate the measurement becomes becasue FFT inherently averages and filters out quantization and other noise.

Figure 2.16 shows measured sampling timing error converted from phase to time (picosecond) vs. delay line code using 16 k point FFTs. Because extremely small load capacitors (cf. Fig. 2.5) are used and the C-DAC is all binary, DNL is very large. However, it is still meaningful to use 6-bits rather than for example 5-bits, because it is necessary to make the quantization error negligible compared with mismatch error, considering that adding 1-bit to the digital bus costs much less than reducing

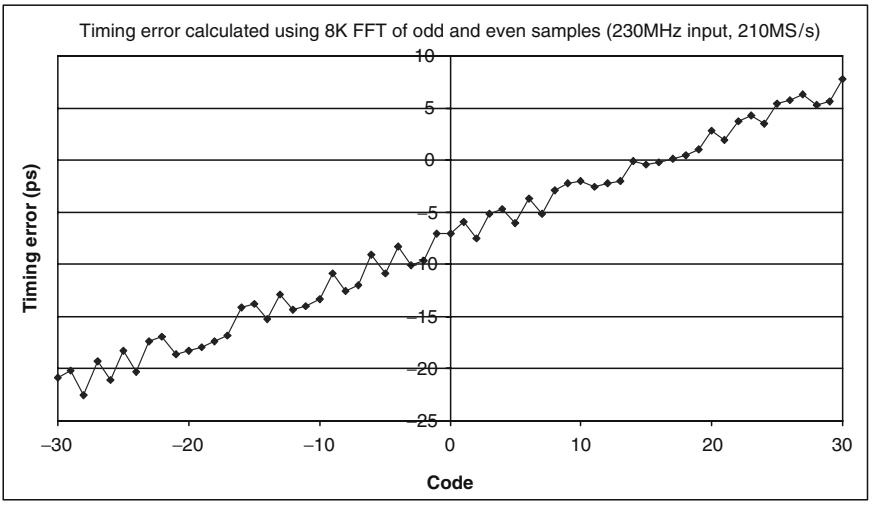

Fig. 2.16 Delay vs. delay control code (measured using output FFT phase of an applied 230 MHz signal input at 210 MS/s)

the mismatch by using larger capacitors. As seen in the results, the mismatch-limited resolution of the timing calibration is about 2 ps. As predicted by simulation, due to the differential way in which the codes are applied to the two delay lines, the delay difference vs. code relationship is very linear due to cancellation of 2nd order nonlinearity.

In addition to sampling timing skew (important for high f_{in}) correction between the two S/H, offset and gain mismatch also generate tones, regardless of f_{in}. As explained in detail in [22], they can be corrected by digital post-processing by taking statistics of the amplitude and mean of the odd and even outputs, and applying an opposite offset and gain.

Even though the passive S/Hs are separate, the ADC uses a single 6-bit FADC, therefore there is no offset and gain mismatch caused by amplifier input referred offset. Since capacitor mismatch of the 5-bit C-array would have caused harmonic distortion tones before it could result in offset and gain mismatch tones, the main source of gain/offset mismatch is the mismatch of on-resistance (causes gain error) and charge-injection (causes offset) of the (top-plate) sampling switches.

Figure 2.17 shows measured ADC output FFT (16,384 point with hanning window) spectra at 210 MS/s with a −3 dBFS 100.3 MHz single tone applied at the input. The first plot does not have any post-processing except DC removal and the code to clock delay line is 0 (p = 32, q = 32). The tone at $f_s/2 - f_{in}$ is about −55 dBc. The FFT after correcting offset and gain is shown in the 2nd plot. The tone at $f_s/2 - f_{in}$ reduces about 2 dB to −57 dBc. On the other hand, with timing skew correction alone, the tone reduces 6 dB to −61 dBc (3rd plot). The offset tone at $f_s/2$ also disappears without requiring correction. This result indicates that timing skew dominates over gain/offset mismatch with this f_{in}. With gain/offset and timing skew correction (last plot) all channel mismatch related tones become less than harmonic distortion terms and the SFDR becomes 71.7 dBc. SFDR changes with measurement but is typically better than 71 dBc for 100 MHz signal input at 210 MS/s.

2.3.3 ADC Measurement Results

As mentioned in section 2.2.2, measurement results show a rise in noise floor and spurs for > -40 dBFS input, which was most likely because the CADC encoder's outputs are directly routed to the 5 b feedback DAC input without using latches to contain the thermometer-to-binary encoder's switching activity locally, resulting in interference coupled to mainly the analog input signal, which does not completely settle before the sampling instant. Figures 2.18 and 2.19 show the actual measurement results (16,384 pt FFT with hanning window) for 210 MS/s and 300 MS/s. We can see and also calculate from the resulting SNDR that the noise floor rises when the signal becomes large enough to trigger change in the CADC output.

At 210 MS/s this noise floor degradation is less than 3 dB (because there was still enough time for the analog input to settle to a certain extent before the sampling

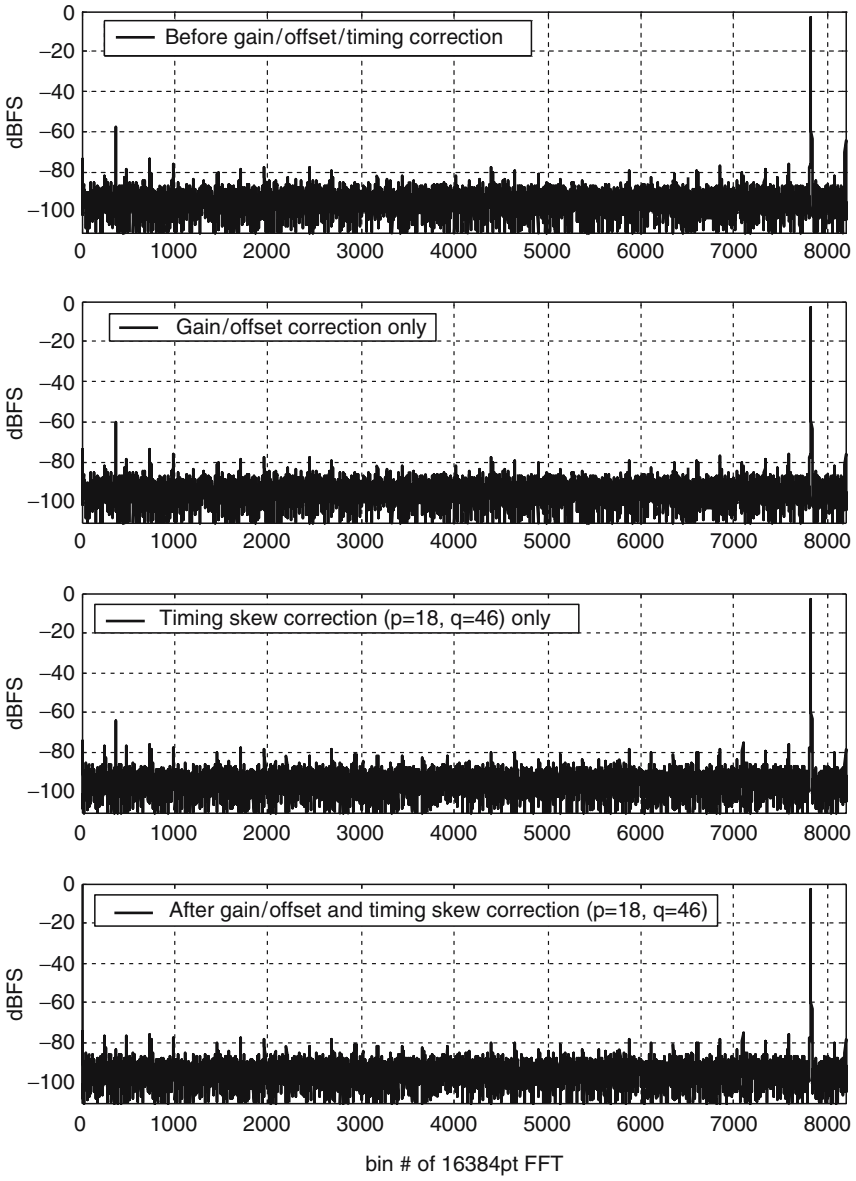

Fig. 2.17 Output FFT of 100.3 MHz −3 dBFS signal input at 210 MS/s with/without gain/offset/timing corrections

instant after the CADC encoder settles/finishes switching) but at 300 MS/s for which this design was originally intended, the degradation is almost 8 dB which must be considered a failure. Without the rise of noise floor, the maximum SNR could be around 57.4 $\sim$ 57.7 dB at 0 dBFS as calculated from the measurement with

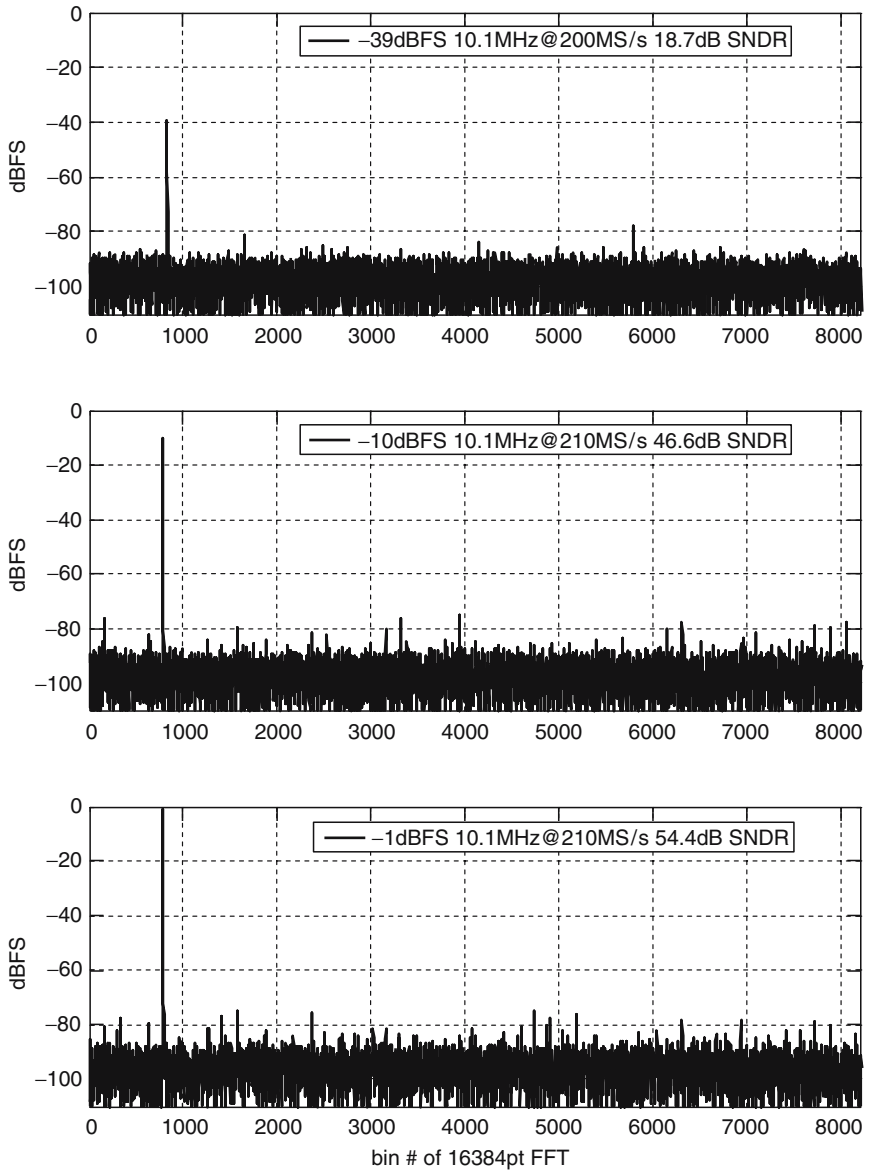

Fig. 2.18 Output FFT spectra for 10.1 MHz input (Notice the rise of noise floor and spurs as signal amplitude increases due to CADC encoder interference. Without this problem, higher maximum SNDR and up to 300 MHz sampling frequency could have been achieved.)

−40 dBFS input, while it is only 55 dB at 0 dBFS for 10 MHz signal. The noise floor for < -40 dBFS input however demonstrates the effectiveness of the proposed offset canceling comparator in the FADC.

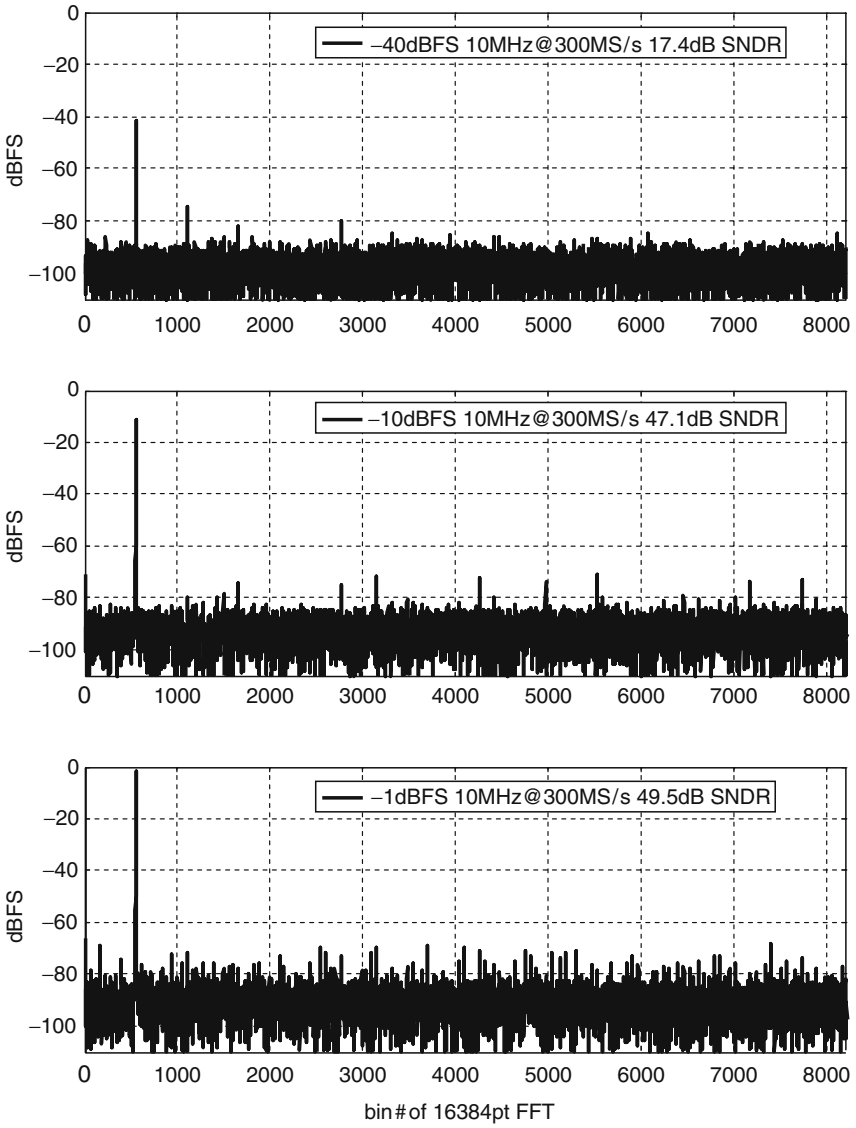

Fig. 2.19 Output FFT spectra at 300 MS/s for 10.3 MHz input (the rise of noise floor and spurs for >-40 dBFS signal is more serious)

Figure 2.20 summarizes measured SNDR/SFDR vs. input signal amplitude for 200 MS/s and 300 MS/s.

Figure 2.21 shows measured maximum SFDR/SNDR for different signal frequencies and sampling frequencies, after digital correction of gain/offset and timing mismatch between the two S/Hs.

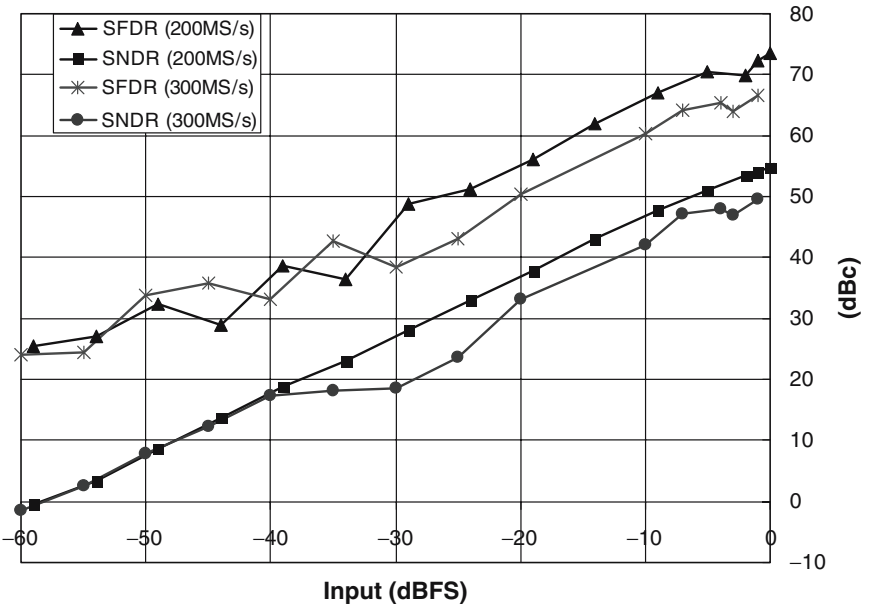

Fig. 2.20 SFDR and SNDR vs. input amplitude for 10 MHz signal at 210 MS/s and 300 MS/s

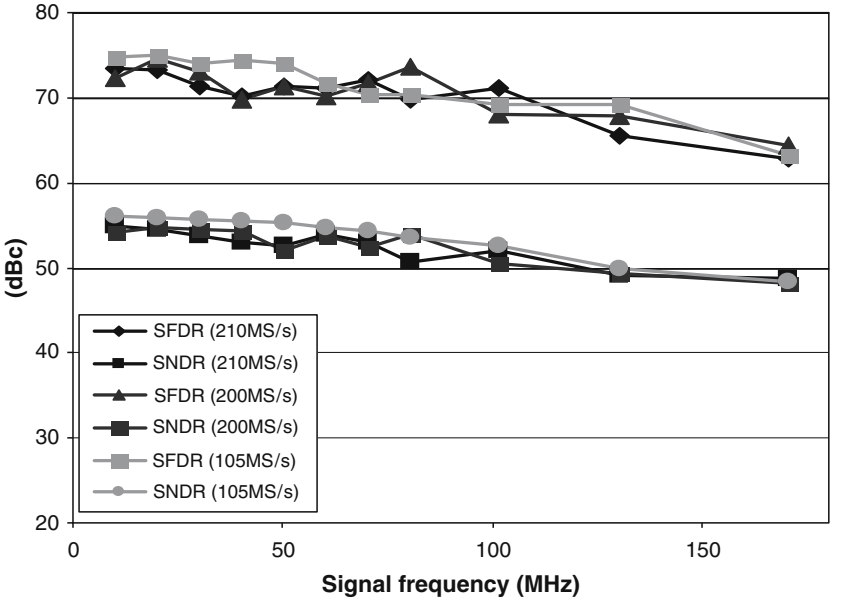

Fig. 2.21 Maximum SFDR/SNDR vs. input signal frequency

For high performance IF-sampling pipeline ADCs that require high SFDR for high frequency input signal, it is common place to use an on-chip signal buffer/active track-and-hold, with better dynamic range than the ADC itself, before the sampling capacitor network. The signal buffer can be sized such that complete settling is guaranteed for the ADC sampling network and we only have to consider charge injection linearity. However, such signal buffers are increasingly difficult to design as process scales down, because it requires transistors with both high DC gain and high f_T to achieve high loop gain from DC up to very high frequency to get as good high frequency linearity as the ADC. They also consume significant power to achieve high dynamic range over wide bandwidth, especially under low supply voltage.

This ADC does not use such an integrated signal buffer, but maintains >70 dBc SFDR up to 100 MHz signal frequency at 210 MS/s with the passive capacitor sampling network (Fig. 2.3). Thanks to the high f_T transistors available in scaled CMOS, the sampling network can use smaller switches with less charge-injection while satisfying settling and bandwidth requirements, resulting in better linearity compared with the same circuit implemented in order CMOS technologies. Another important reason behind the high SFDR is the high linearity of the 5 b capacitor DAC. Despite the fact that each unit capacitor is only 10 fF, linearity of the 5 b C-DAC surpasses that of cascaded residue amplifier stages used in conventional 10-bit pipeline ADCs to achieve the same function (cf. Table 2.2). This is because the improved lithography accuracy in nanometer CMOS process makes it possible to realize very small but well-matched interconnect capacitors [48], [5].

When the shortcomings of these scaled CMOS processes, namely the reduced amplifier voltage gain and linearity are overcome by using architectures that do not require op-amps in analog feedback, and their advantages exploited, we can expect higher analog dynamic range using these "digital" processes rather than lower dynamic range as generally perceived.

Figure 2.22 shows the INL and DNL measured using the histogram method by applying a full-scale sine wave. Again, due to the CADC binary encoder interference problem, the DNL at the codes where the CADC switches is much larger than what would otherwise have been without said interference issue. This results in reduced maximum SNDR. Nevertheless, the INL is still quite linear, confirming the high measured SFDR and demonstrating the linearity advantage of the proposed two-step architecture over conventional pipeline architectures.

The ADC draws 40 mA from a 1.2 V AVDD and 3 mA at 210 MS/s from a 1.2 V DVDD, including reference buffers, bias and clock buffers, but excluding output drivers. Table 2.1 summarizes performance measured of this chip.

Table 2.2 provides a comparison with other high speed 10-bit ADCs based on the conventional pipeline architecture. Even with the interference problem, the ADC still provides comparable performance with recently published 10-bit pipeline ADCs and better SFDR, with less silicon area and power consumption. If output latches were used at the CADC binary encoder to resolve this problem, up to 3 dB

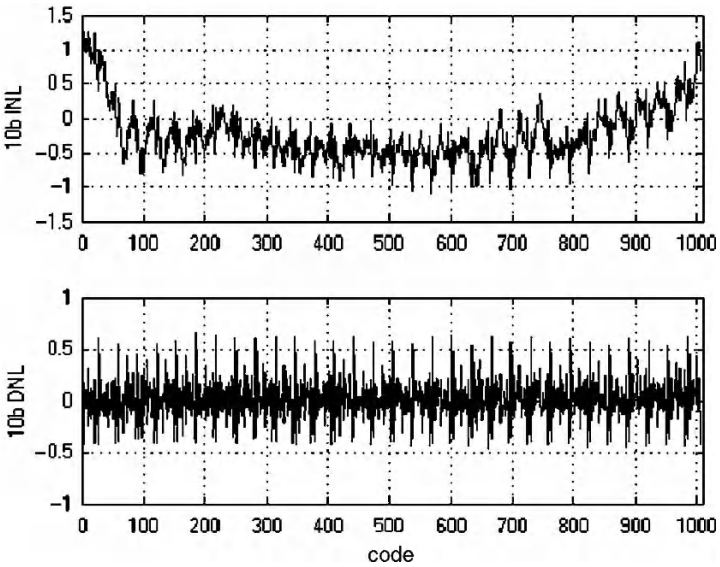

Fig. 2.22 INL/DNL measured with histogram method

Table 2.1 Performance summary

Technology	UMC 0.13 μm CMOS
Resolution	10 bits
Input range	0.9 Vpp differential
Power supply	1.2 V analog, 1.2 V digital
Sampling frequency	210 MHz
Power consumption	48 mW analog, 4 mW digital@210 MS/s
SFDR/SNDR	74 dB/55 dB, f_{in} = 10.1 MHz
	71 dB/52 dB, f_{in} = 100.3 MHz
Active area	0.38 mm^2 including decoupling caps
Die size	1,525 μm × 1,525 μm
Package	QFN 56 pin, 7 mm × 7 mm

Table 2.2 Comparison with other recently published 10-bit CMOS pipeline ADCs

Year	Fs (MS/s)	SFDR (DC)	SFDR (100 MHz)	SNDR	Power (mW)	Area (mm^2)	CMOS process	FOM (pJ/conv)	Ref.
2004	220	62 dBc	N/A	54.3 dB	135	1.3	130 nm	1.44	[20]
2005	200	66.5 dBc	N/A	54.4 dB	55	1.26	90 nm	0.63	[38]
2006	400	70.5 dBc	60 dBc	56 dB	160	4.2	130 nm	0.77	[42]
2006	50	70 dBc	N/A	56 dB	18	1.43	180 nm	0.8	[45]
2007	205	73 dBc	71 dBc	55 dB	61	1.0	90 nm	0.64	[43]
2008	210	74 dBc	71 dBc	54.7 dB	52	0.38	130 nm	0.56	This work

higher SNDR and SFDR could have been expected, and with a little increase of analog bias currents the ADC could have achieved 300 MS/s with good performance as originally designed.

2.4 Summary

A 10-bit 210 MS/s two-step ADC has been designed in 130 nm digital CMOS using only 1.2 V devices. It achieved 55 dB/74 dB SNDR/SFDR for DC and 52 dB/71 dB for 100 MHz 0.9 Vpp differential input signal, while consuming 52 mW from 1.2 V analog and digital supplies. Highlights of the proposed techniques include: (i) the use of 5-bit capacitor networks + efficient regulated reference buffers instead of power-hungry resistor ladders + multiplexers as in conventional subranging ADC to achieve higher linearity and less power consumption; (ii) the use of aggressive interpolation in the FADC to reduce FADC input capacitance for a given thermal noise level; (iii) the use of input/output offset storage in the FADC preamps which allow faster settling during reset phase, where the interpolation capacitors, rather than the next stage input capacitor, must be charged (hence less bias current needed for preamplifiers); and (iv) the use of offset canceling comparators which reduces the number of preamplifier stages and over-all die area of the FADC and the 5-bit CADC.

Chapter 3
A 32 mW 1.25 GS/s 6 b 2 b/Step SAR ADC in 130 nm Digital CMOS

3.1 Background

When we look at telecommunication standards of the past, present and the future, we notice a continued trend from narrow band specifications to wide band ones, with higher carrier frequency (Fig. 3.1.) While the AM radio used only 10 kHz for each channel with a carrier frequency of several hundred kHz, UWB (ultra wide band) would use 500 MHz per each channel with a carrier frequency of 3∼10 GHz.

As bandwidth widens, more thermal noise falls in-band, and since transmission power is limited to around 1∼3 W by power consumption constraints, inevitably the SNR reduces. The fact that phase noise of local oscillators degrades as carrier frequency increases is another reason that the SNR of transmitted or received signal continue to decrease for newer standards.

Shannon's theory tells us that the capacity C of a band-limited AWGN channel is given by

$$C = B\log(1+S/N). \tag{3.1}$$

Since the capacity only decreases logarithmically with more noise, but it increases linearly with bandwidth, even though the SNR inevitably reduces, newer wireless standards which use wider signal bandwidth can be developed that enables higher bit-rate transmission, hence accommodating more users and more advanced services.

Digital signal processing is also proliferating in wireline communications. To increase system flexibility and reliability against process and temperature variations, more and more functionality is being implemented in digital domain. 6-bit high-speed ADCs have long been used in HDD read channels to implement the partial response maximum likelihood (PRML) detection. In the near future, applications will broaden to include giga-bit ethernet interface and fiber optic network, where high speed ADCs are being used to digitize incoming signal before functions such as equalization or clock and data recovery can be performed reliably with much flexibility in digital domain.

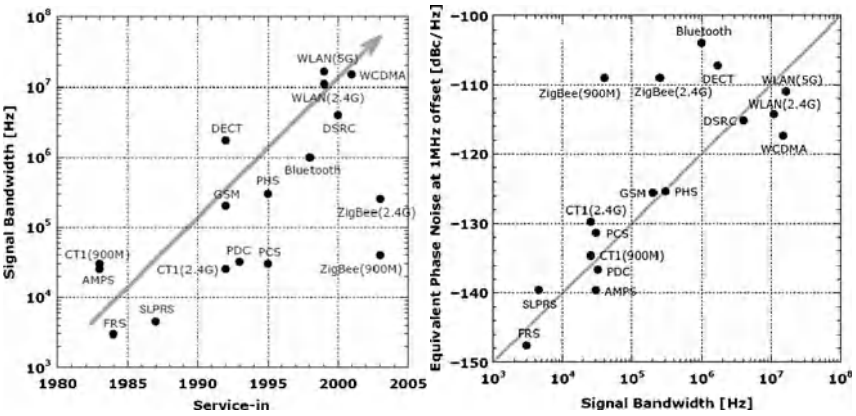

Fig. 3.1 Signal bandwidth and local oscillator phase noise requirement of various wireless standards

For the above reasons, it is predicted that the demand of high-speed, medium$\sim$low resolution ADCs for telecommunication applications will increase in the future. The flash architecture has been dominantly used for these ADCs. However, due to the requirement of many parallel comparators and preceding pre-amplifiers to reduce offset and input capacitance, the lowest reported power consumption for 6-bit $>$1 GS/s flash ADC is about 160 mW [30].

This paper presents a new type of ADC that takes advantage of the high speed digital logic and highly matched small capacitors [48] in standard nanometer digital CMOS processes to achieve 1.25 GS/s, 6-bit performance but with much lower power consumptions and smaller die area than flash ADCs. Unlike many previously published low-power high-speed ADCs such as [14], [13] and [6], this ADC achieves 6-bit accuracy without any complex digital post-processing or off-line calibration, making it a plug-in replacement for flash ADCs in many applications.

3.2 Architecture

In Chapter 1 it was explained the advantages of the successive approximation (SA) architecture in nanometer CMOS. It is known that the energy per conversion of SAR ADCs is approximately linearly proportional to the resolution while that of flash ADC is exponentially proportional [18]. This implies that SAR is more energy efficient than flash only when the number of bits is larger than a certain threshold, below which flash becomes more efficient (Fig. 3.2). It is also known that when the clock frequency is close to the upper limit of a certain process, energy per operation increases dramatically and a little reduction of speed can be traded for large power savings. When these factors are considered, for small number of bits it may be less efficient to use SAR with a very high internal clock frequency than to use flash.

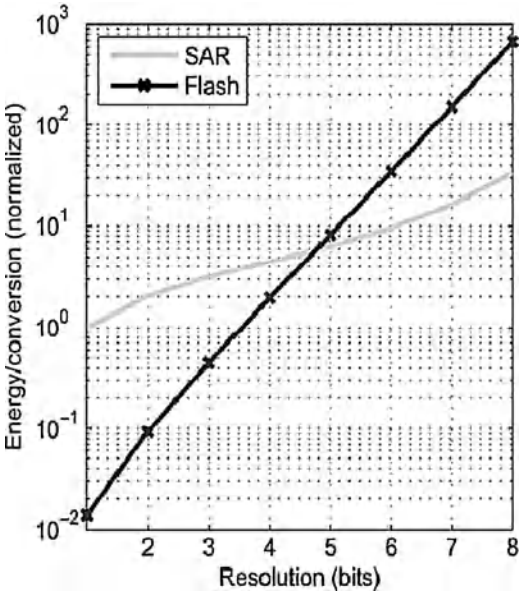

Fig. 3.2 Modeled SAR and flash ADC energies vs. resolution (Copy of Fig. 4a in [18])

If we view one SAR conversion process as a cascade of multiple SAR conversion processes with a smaller number of bits, we can see the possibility of increasing sampling frequency and/or power efficiency by replacing each sub-conversion process with the flash architecture.

Figure 3.3 illustrates an example conversion process of the proposed architecture that combines SAR and flash. Suppose analog input "39" was sampled on all capacitors. The next phase 3 reference levels for the flash are generated by (001), (011) and (111) inputs to the capacitors sized "16" (and (110), (100), (000) on the negative side). All the other capacitors are connected to 0 (and 1 on the negative side). As a result, the top 2 bits are converted by the 3 comparators. In the 2nd conversion step, the previous comparator outputs are connected to each "16" capacitor, and the 3 reference levels are generated by the "4" capacitors, converting the middle 2 bits. The continues and finally the 6-bit ADC output is obtained by simply using 3 full adders to convert each step's 3 comparators' outputs to 2-bit wide binary format, which is a much simpler process than in a traditional 6-bit flash ADC where 65 comparators' outputs need to be converted into binary format.

Implemented in UMC digital 0.13 μm CMOS, each SAR ADC is clocked at 2.5 GHz, and two bits are determined per each cycle. Including the sampling/autozeroing cycle, four cycles are required to convert 6 bits. two SAR ADCs are time-interleaved to sample at 1.25 GHz.

Figure 3.4 shows the block diagram of the proposed architecture. It achieves 6-bit resolution and 1.25 GS/s with only 6 comparators whereas 64 comparators are required in the flash architecture. Even though the clock frequency of each comparator

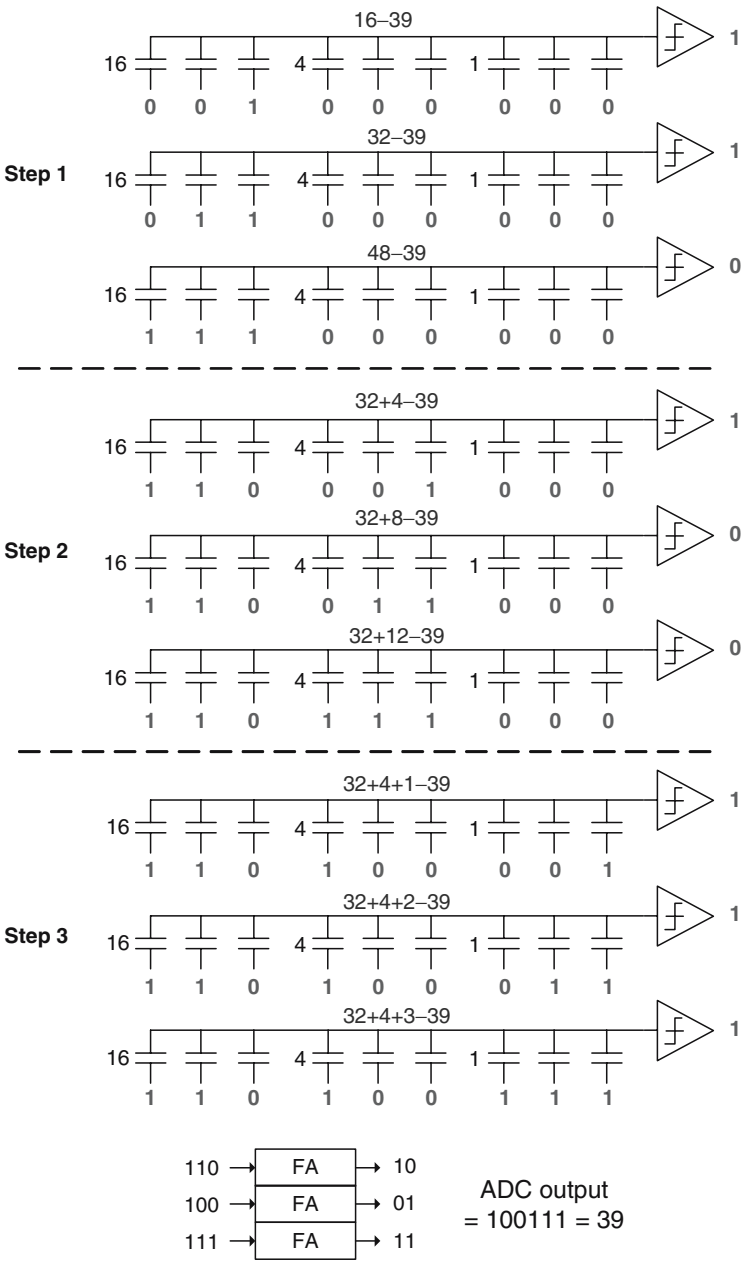

Fig. 3.3 An example conversion of analog input "39" by combined flash and SAR

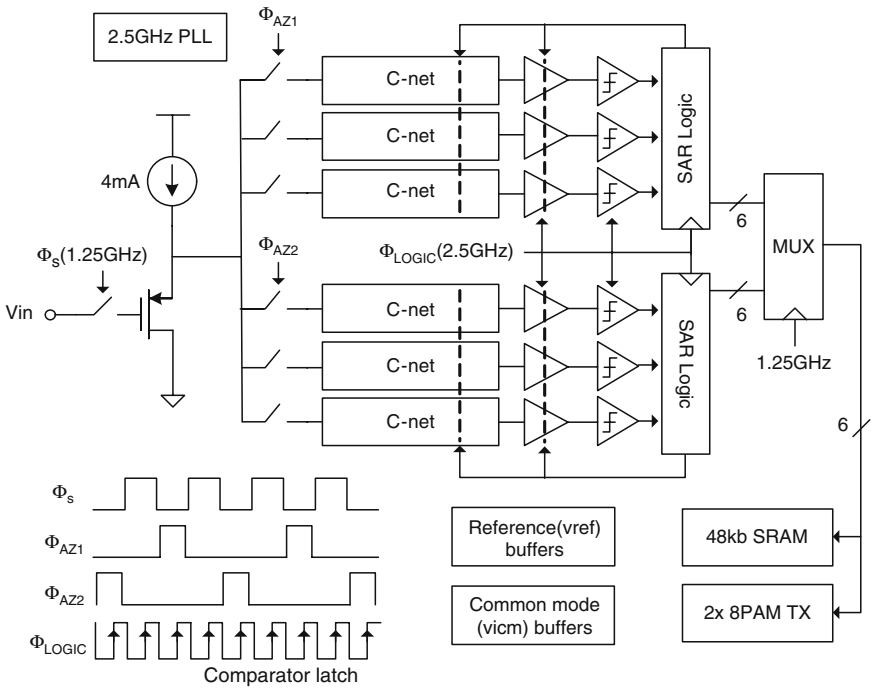

Fig. 3.4 Overall block diagram of the proposed 1.25 GS/s 6-bit SAR ADC

is doubled from 1.25 GHz to 2.5 GHz, the >10X reduction in number of comparators and the preceding preamps which consume static power results in much decrease in power consumption.

2X time-interleaving is used to double the sampling frequency. In theory more ADCs can be time-interleaved to obtain even higher sampling frequency [14]. However, offset, gain and sampling time mismatch create more tones and images of input signals, not to mention the increased area and input capacitance. The tones caused by offset mismatch among the channels are the largest error source, limiting the SNDR to 27 dB in [14]. These tones can be nulled by digitally adding offset until each channel's output has equal averaged value. This, however, also removes any input signal components at these tone frequencies. But for 2X time-interleaving, offset mismatch creates a tone at fs/2, which is tolerable since no signal exists near this frequency after anti-aliasing filter. Gain and offset mismatch can be relatively easily calibrated out using digital techniques proposed in [22]. Sampling time mismatch is much more difficult to correct using digital techniques. Therefore, a single track and hold (T/H) is used so that the sampling instant is determined by a single 1.25 GHz clock.

3.3 Enabling Circuits

The above architecture sounds promising but without several circuit level innovations described in this section it would not have been practical, i.e. actually realizing lower power consumption than flash with the same speed and resolution, or to achieve 1.25 GS/s to begin with.

3.3.1 Fast Settling Capacitor-Network

Rather than separating the 2-bit quantizer with the capacitor network, this design uses three capacitor networks (c-net), each of which is connected to a comparator (Fig. 3.4). This is to avoid the use of resistor ladder which draws much static power. In a way, each reference level is generated "digitally" by the feedback DAC, while only requiring two analog reference voltages $+V_{ref}$ and $-V_{ref}$ (Fig. 3.5).

Both in the flash and SAR architecture, to achieve high sampling speed the reference must provide low output impedance. In this design, $+V_{ref}$ and $-V_{ref}$ are generated by regulated source followers (Fig. 3.6). The output impedance of this buffer can be calculated as

$$Z_{out} \approx \frac{sC_{gs3} + g_{ds2} + g_{ds3}}{sC_{gs3}(g_{m2} + g_{ds2} + g_{ds3}) + g_{m3}(g_{m2} + g_{ds2} + g_{ds3})}. \tag{3.2}$$

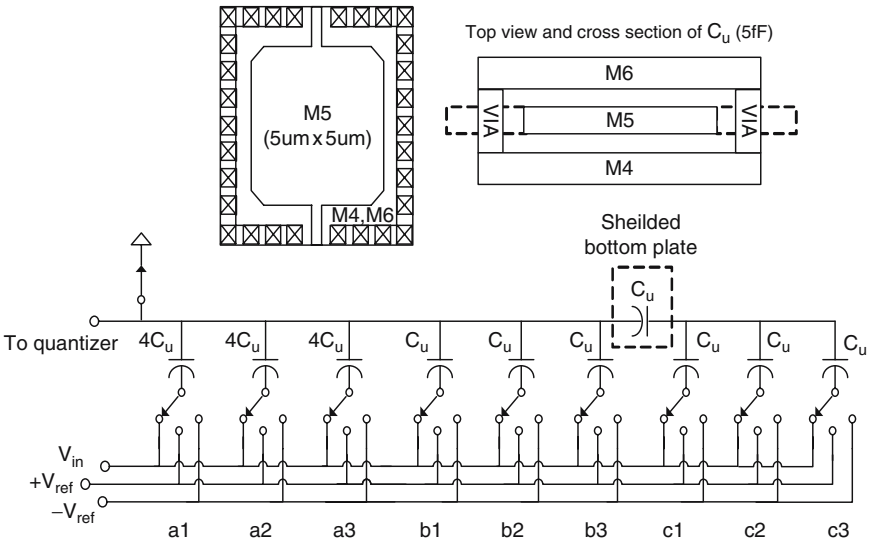

Fig. 3.5 Capacitor network

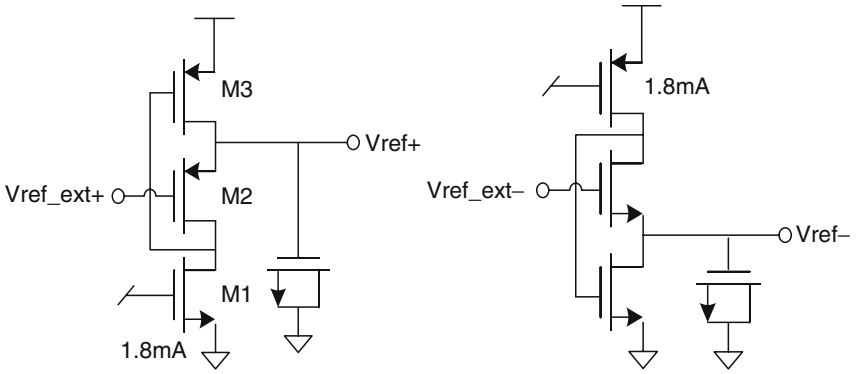

Fig. 3.6 Regulated source followers that generate $+V_{ref}$ and $-V_{ref}$

We can see at DC this is approximately

$$Z_0 \approx \frac{1}{g_{m3}(g_{m2}/(g_{ds2}+g_{ds3})+1)} \approx \frac{1}{I_{bias} \times 200}, \tag{3.3}$$

assuming reasonable V_{dsat} of 150 mV and M2's intrinsic gain of about 15. This output impedance is maintained until at a zero frequency

$$\omega_z \approx \frac{g_{ds2}+g_{ds3}}{C_{gs3}} \tag{3.4}$$

when it starts to increase 20 dB/dec until it reaches $1/\mathrm{gm}_2$ at a pole frequency

$$\omega_p \approx \frac{g_{m3}}{C_{gs3}}. \tag{3.5}$$

To keep output impedance around Z_0 for all frequency. the output capacitance size must then be

$$C_o \geq C_{gs3} \times \frac{g_{m2}}{g_{ds2}} \times \left(\frac{g_{m3}}{g_{ds3}+g_{ds2}} + 1 \right) \tag{3.6}$$

In this design, each reference buffer draws 2 mA, so about 2.5 Ω output impedance is generated at low frequencies. Similar impedance is generated at high frequencies by large NMOS gate capacitors (with gate area 200 times of that of M3) connected at the output to ground.

It should be noted that if reference resistor ladders, which are used in conventional flash ADCs, were used to generate this low impedance for each reference level, then the bias current would be VDD/2/2.5 = 240 mA, more than 100 times larger. The use of this type of reference buffering is only possible because there are only two analog voltage levels to generate, since these NMOS gate capacitors consume a lot of silicon area. In a way, the necessary 63 reference levels are generated by capacitor interpolation in this ADC rather than by a resistor ladder in conventional flash ADCs.

Another benefit of this design choice is that because closed switches have high over-drive voltages (VDD$-(-V_{ref})$ or $+V_{ref}-$VSS) during the comparison cycles, it becomes possible to achieve very fast settling speed, especially when low-Vt transistors are used for the switches.

The biggest disadvantage of using three c-net is the increased number of capacitors. Fortunately, as process scales the accuracy with which interconnect metal patterns can be defined improves, making it possible to realize highly matched, very small value capacitors using interconnect metals [48]. The 6-bit capacitor network uses ~5 fF unit capacitors realized by metal-456 sandwich with 5 μm × 5 μm top plate (Fig. 3.5). The top plate is almost completely encaged by the bottom plates to minimize parasitic coupling. A single bridging capacitor[1] has been used, resulting in a LSB capacitance of only 1.25 fF and a total capacitance of about 240 fF which is driven by the front-end T/H. The three capacitor networks occupy only 100 μm × 70 μm which is about 52% of the layout area.

3.3.2 Flip-Flop Bypass SAR Logic

To achieve the 400 ps cycle time, delay of the SAR logic must be reduced so that as much as possible time can be allocated for c-net and quantizer preamp settling.

Figure 3.7 shows block and timing diagrams of a conventional successive approximation control logic, which consists of a shift register and an array of DFF forming the successive approximation register (SAR). The comparator starts regeneration at the falling edge of the clock, and the SAR latches the comparator output at the rising edge of the clock. It is assumed that in the worst case (i.e., when the input differential signal is very small,) the comparator needs half clock cycle to regenerate. This results in large wasted cycle time for other cases when the comparator

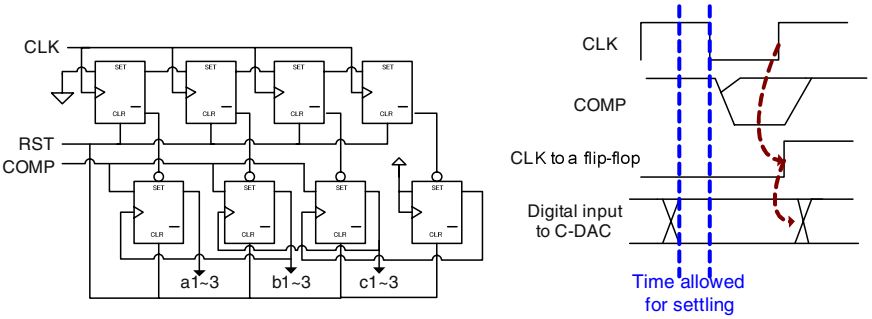

Fig. 3.7 Block and timing diagrams of conventional SA control logic

[1] The parasitic bottom plate capacitance of the bridging capacitor will not affect the bit weight ratio, because it will only reduce the impedance at the quantizer input which results in proportional signal attenuation

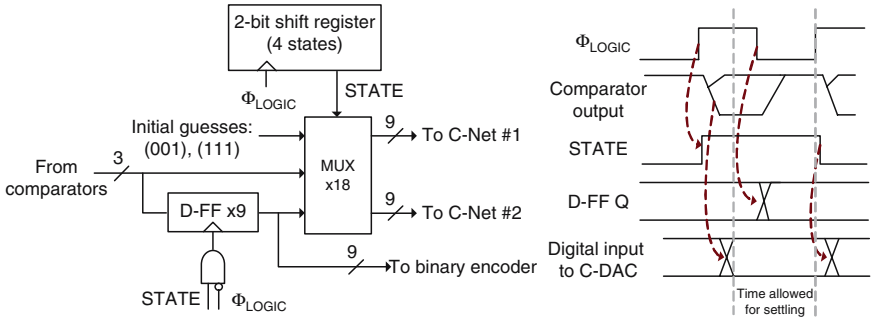

Fig. 3.8 Block and timing diagrams of the proposed SA control logic

Table 3.1 Multiplexer operation

	State 4 and 1	State 2	State 3
a1∼a3	(001)/(011)/(111)	Pass quantizer output	Pass D-FF output
b1∼b3	(000)	(001)/(011)/(111)	Pass quantizer output
c1∼c3	(000)	(000)	(001)/(011)/(111)

can regenerate more quickly. We also have a clk-to-Q delay after the rising edge of CLK, which eats away available cycle time for settling of the capacitor network. As a result, we have less than half clock cycle for the settling.

Figure 3.8 shows block and timing diagrams of the proposed "flip-flop bypass" control logic. The comparators in the quantizer starts regeneration at the rising edge of ϕ_{LOGIC}. The 3-bit thermometer coded output of the quantizer is directly passed to the C-Net through a multiplexer, without D-FF in between. The sooner the comparator regenerates, the sooner the output is applied to the C-Net and the settling of next bit cycle starts. It is only at the falling edge of ϕ_{LOGIC} that the comparator output is written to a D-flip-flop to be used by later SA cycles. If we are lucky at this time the next bit cycle may already have begun.

The c-net as shown in Fig. 3.5 enables the direct connection of the quantizer output. Nine bits (a1∼a3, b1∼b3 and c1∼c3) controls the effective feedback voltage.

All the additional logic such as binary encoding is placed outside of the digital feedback loop where pipelining can be used to increase clock frequency. The only logic delay inside the feedback loop is now from the multiplexer and a NAND gate that controls the c-net bottom-plate switch. Table 3.1 summarizes the operation of this multiplexer.

Figure 3.9 shows the simulated waveforms at one of the capacitor array's top plate (input to one of the preamp and quantizer), the clock that latches the comparator (master_clkb), comparator outputs, comparator slave latch's output (input to SAR logic) and the SAR logic output.

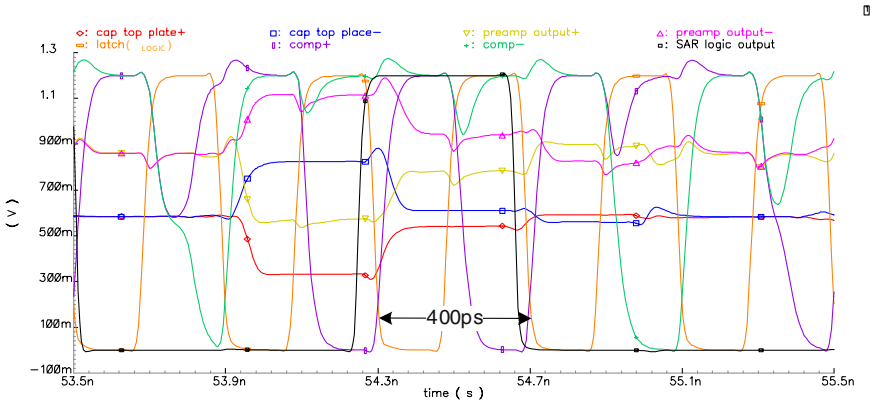

Fig. 3.9 Simulated internal waveforms of the SAR converter (after offset canceling loop settles)

The SAR logic is 100% static CMOS and uses low-Vt transistors for critical paths. Measured digital power consumption (SAR logic + clock buffers) is 8 mA at 2.5 GHz internal frequency.

3.3.3 Digital Background Offset Correction

Unlike pipeline ADC, since there is no residue amplification, and range-overlapping (redundancy) is not used for the sake of simplicity in this design, the 2-bit flash ADC must be 6-bit linear. Because a reasonably sized dynamic latching comparator would have several tens of mV (up to 10 LSB of the 6-bit ADC) of offset, preamplifiers must precede the comparators such that the error is small enough when referred to quantizer input, or offset reduction methods such as calibration or averaging must be used. Since each preamp must have very high bandwidth to obtain enough gain in limited amount of settling time, their DC gain must be low (2∼4) [7]. Interpolation are commonly used to reduce the number of preamps, but it also requires low gain so that large portions of the transfer curves of neighboring preamps overlap. In conventional 6-bit flash ADCs, cascade of many low gain preamps are used to provide a gain of more than 30 [30]. However, many stages of preamps not only increases power and die area, but also increases delay which is detrimental to the SAR scheme.

This problem is solved by reducing the number of preamp-stage to only 1 and using offset self-calibration through digital feedback to compensate for the lack of preamp gain. Comparator offset calibration has become a popular technique in recent years for Flash ADCs to reduce power consumption [13]. For example, if we use a 3-bit DAC to reduce maximum possible offset by 8 times, then the comparator size can be shrunk by 1/64, leading to 64X power reduction.

However, the flash ADC needs to be put off-line during calibration, and offset that changes during operation cannot be corrected. Unlike flash, where the comparator is always working during operation, the SAR conversion scheme allows the

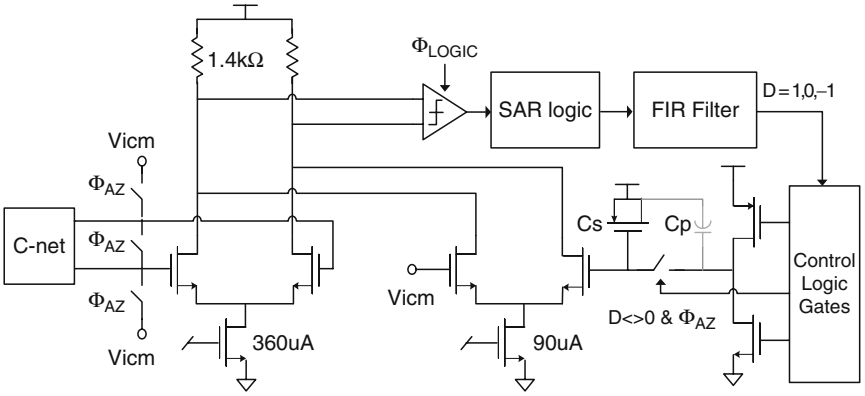

Fig. 3.10 Schematic diagram of proposed 2-bit quantizer

use of comparator output during the auto-zeroing phase when the c-net is sampling input and the top-plates are shorted, to measure the comparator offset, and then compensate during the next auto-zeroing phase (Fig. 3.10) while running the ADC at full speed.

Since the positive and negative inputs are shorted in this phase, offset of the preamp and the comparator will decide the digital output. The digital output is filtered by a FIR filter and applied to a passive switched-capacitor integrator. The resulting voltage controls an auxiliary amplifier to generate an opposite offset until the comparator outputs equal numbers of -1 and 1 in the auto-zeroing phase. This scheme is based on [15] where similar scheme has been used for two-step subranging ADC, in which two ADCs are time-interleaved so that each only process the input signal half of the time, while the outputs of the other half are used to calibrate offset. This results in 2X area and power penalty whereas in the proposed SAR ADC there is no additional cost.

Due to hysteresis and other non-idealities of the comparator, in steady state, we could see much unnecessary fluctuation at the comparator output even though the average is zero (e.g. $1, 1, -1, -1, 1, 1, -1, -1, ...$). Although the switched-capacitor integrator can filter out some of the fluctuations, further filtering is achieved by a simple two tap FIR filter without affecting stability of the loop. A block diagram of the loop is shown in Fig. 3.11. Cs/Cp is sized such that the compensation step size is about 0.02 LSB.

Figure 3.12 shows simulated settling waveform of the offset calibration loop, when each comparator is given an offset of -5 mV, 0 and 10 mV. Since the preamp's gain is about 2.5, these offsets are -2 mV, 0 and 4 mV referred to ADC input.

We can see that due to finite hysteresis in the comparators that makes their offset dependent on previous decision, the settling is not perfect and it is only when the ADC input referred offset becomes about 1mV that the comparator makes decision to move the correction to the opposite direction. However, since the LSB is about 10 mV, this error only amounts to 0.1 LSB and will be random rather than limit-cycle-oscillation-like in the figure because the simulation does not consider thermal noise and other random noise.

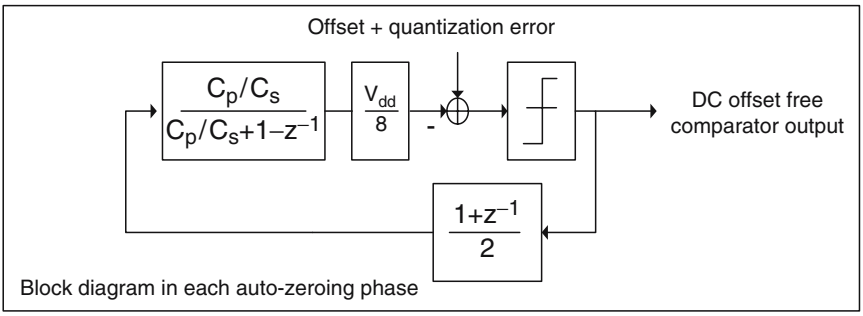

Fig. 3.11 Equivalent block diagram of proposed 2-bit quantizer

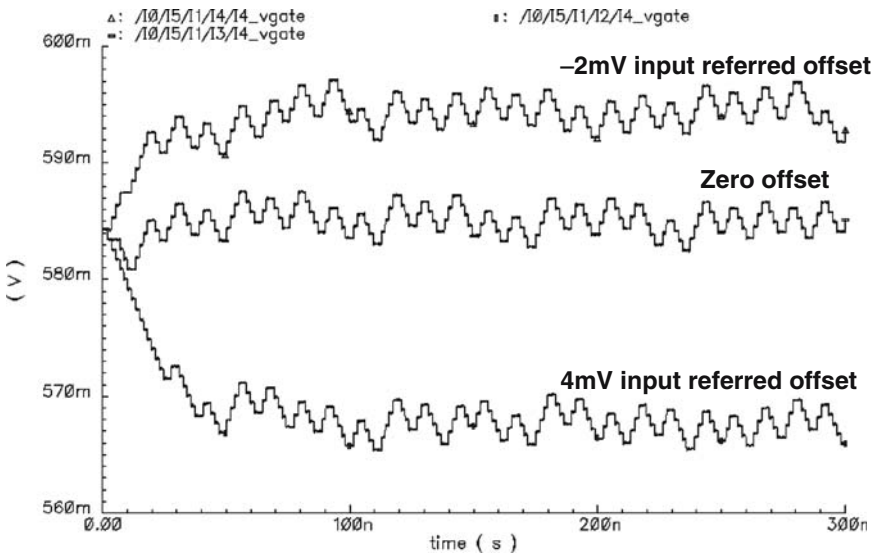

Fig. 3.12 Simulated settling waveforms of the offset calibration loop

3.3.4 High-Speed Low-Hysteresis Comparator

To enable the proposed architecture, the comparator must be both high speed, low latency and have very little hysteresis, i.e. its offset mostly being static and not affected by the previous decision. Even though the clock frequency is 2.5 GHz, to allow time for settling of the digital logic block and c-net, the latency of the comparator must be far less than 400 ps.

Figure 3.13 shows the schematic diagram of the comparator, which consists of a master dynamic comparator and slave static CMOS latch (cross coupled NAND). To reduce hysteresis, extra reset switches have been added to ensure every node in the master dynamic comparator is completely precharged to VDD before the latch signal goes high.

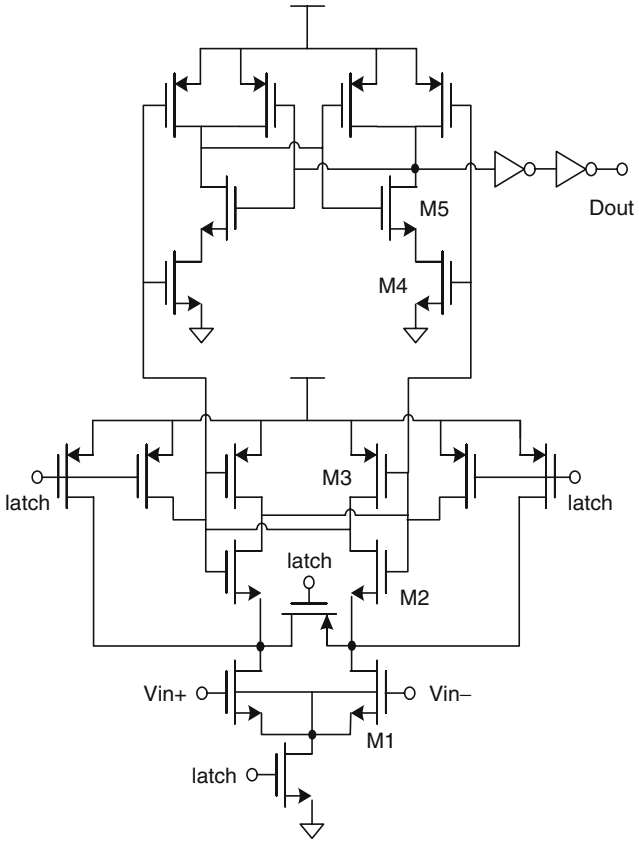

Fig. 3.13 Schematic diagram of the 2.5 GHz low hysteresis comparator

Because of the way the flip-flop bypass SA logic works, the comparator must hold the decision until the next latch edge, therefore a slave latch, typically realized by cross-coupled NAND gate for this type of comparator, must be used.

The outputs of the master dynamic comparator that goes directly to the slave latch were connected to the bottom NMOS rather than top NMOS that is exposed to NAND gate outputs. This is because depending on the NAND gate output being high or low (i.e. the previous comparator decision), the MOS channel is not completely formed (with drain = VDD and source = VDD-Vth) or formed (with drain/source = VSS), and hence presenting different load capacitance to the master dynamic comparator, resulting in much feared hysteresis. On the other hand, if they are connected to the bottom NMOS, the channel is always formed there regardless of the latched state, since drain/source are shorted to ground with the top NMOS turned off. The PMOS of the NAND gate is completely off hence does not present much data dependent load capacitance.

This kind of consideration was not necessary in conventional flash ADC since the comparator offset is being overcome by brute-force signal preamplification. It may even be preferable in terms of regeneration speed to use the top NMOS rather than the bottom one as the slave latch input in such case.

It may be argued that inverter buffer stages can be inserted between the comparator and slave latch to rid of hysteresis. However, with a single inverter, either cross coupled NOR gate or PMOS input comparator must be used instead, increasing propagation delay and power consumption. If two inverters are used, to maintain optimal fan-out, the cross-coupled NAND gates must be much larger and have to drive much larger load which would otherwise be driven much more efficiently by inverter buffers.

The comparator uses digital VDD/VSS. This is because the latch signal comes from the clock buffers and hence the charge current comes from digital VDD/VSS. If the comparator were connected to analog VDD/VSS, then every time the latch signal goes up or down, current must flow from digital VDD to analog VSS or digital VSS to analog VDD. This means the >2.5 GHz current must either pass through package bond wires or deep-n-well isolation which is basically a reverse biased p-n junction. The result is voltage bounce on the AVSS line, although periodic and signal independent, may slow down the comparator since the package inductance and PCB trace will come between the clock driver and the latch transistors (the AVSS will bounce up with "latch" signal goes up).

On the other hand, this problem is much less severe if the comparator uses digital VDD/VSS. This time, the comparator receives signal Vin+ and Vin- from the preamp which uses analog VDD/VSS. Since they are differential, only common-mode current goes between analog and digital supply. Figure 3.14 illustrates the two cases.

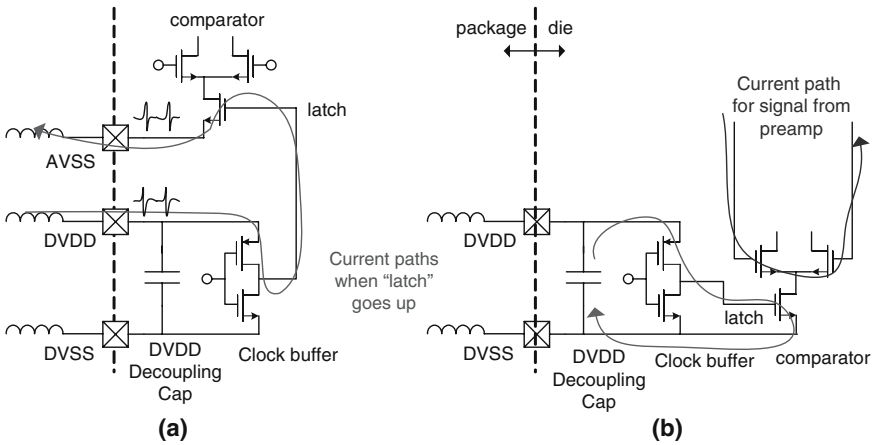

Fig. 3.14 Illustration of the current paths when the comparator uses analog supplies (**a**) and digital supplies (**b**)

The disadvantage of using digital VDD/VSS for comparator is that there are much signal dependent disturbances on digital VDD/VSS unless much decoupling capacitor is used for the digital supplies. These signal dependent disturbances result in time-varying offset in the comparator, which cannot be compensated by the background offset self-calibration loop. As can be seen in the die photo (Fig. 3.16) the digital VDD decoupling capacitor (realized by NMOS inversion mode gate capacitor) occupies almost twice as much area as the digital circuit block does.

3.3.5 Floor Plan and Layout Considerations

Figure 3.15 shows the layout excluding top metal and decoupling capacitors. To achieve 400 ps cycle time it is crucial to minimize layout parasitics, which requires the layout to be as compact as possible. Signals with the highest frequency components, in this case, clock signals, should have to go as little distance as possible to reduce loading and power consumption. Therefore, the clock buffer is placed at the center of two copies of the time-interleaved ADC, such that switches of both ADCs can be placed immediately next to it. Followed by the switches are the capacitor net-

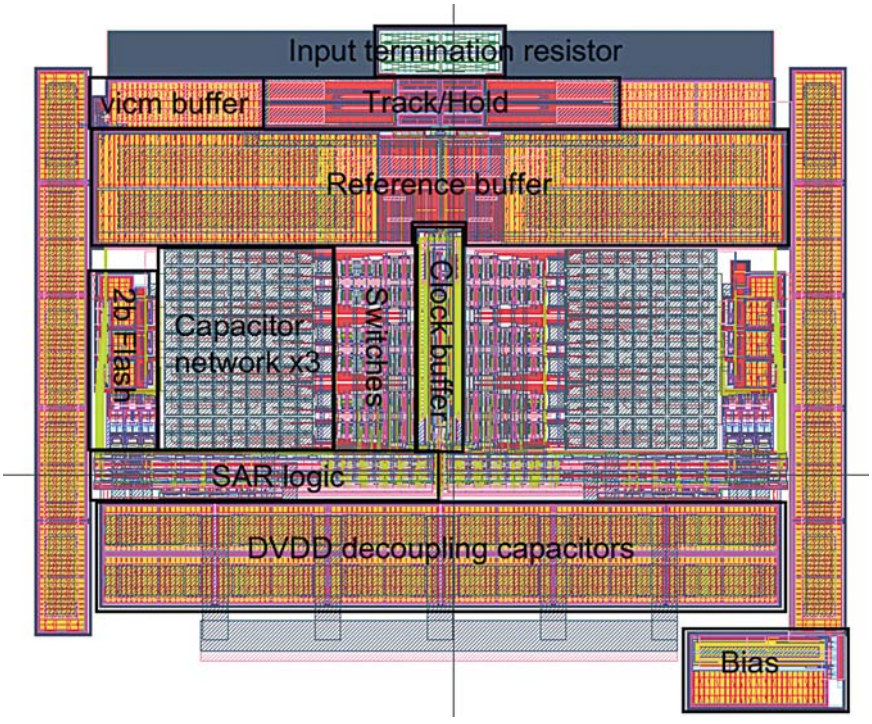

Fig. 3.15 Layout excluding decoupling capacitors

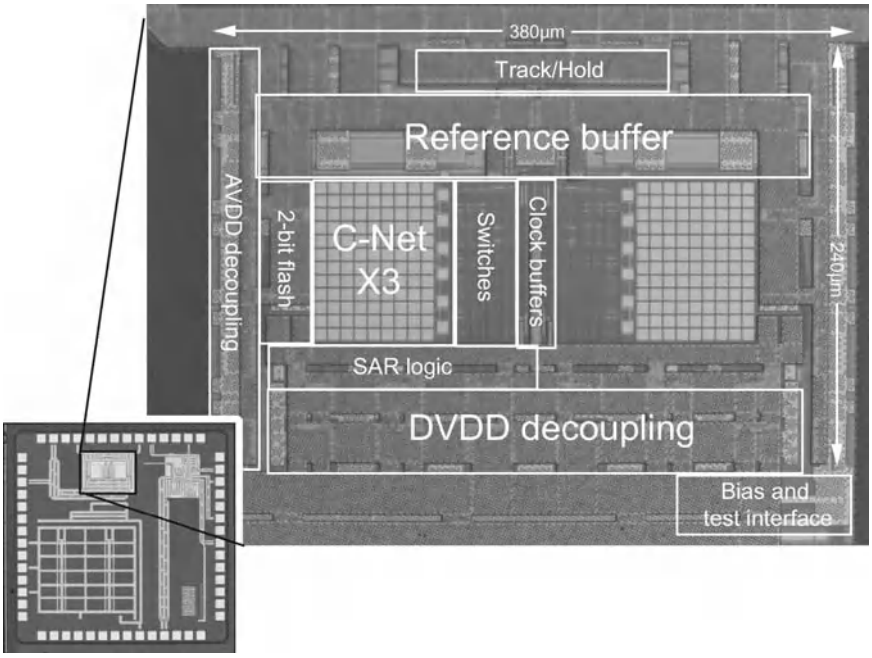

Fig. 3.16 Photograph of the entire die (including PLL and SRAM) with the ADC portion enlarged

works, beyond which lie the 3 preamps and comparators. The SAR logic lies across the comparator back to the switches, such that physical lengths of the digital signal paths are minimized.

Figure 3.16 shows die photographs of the chip. The ADC is placed at the upper center of the die, such that the signal and VDD/VSS bond wires can be as short as possible. The ADC's output travels downwards the die to the SRAM and two 8-PAM transmitter (essentially a 3-bit current steering DAC.) Inverter buffers are inserted every $\sim$300 μm to improve signal integrity. For every long single-ended signal wiring, metal-7 (DVSS) has been laid above the wiring to provide return path and reduce electromagnetic emission.

The PLL is placed at the upper-right corner of the die. The 2.5 GHz clock is routed from the PLL to ADC using differential metal-6 wiring with metal-1 (DVSS) shield. The shield increases isolation from substrate while adding little parasitic capacitance. To keep high edge-slope, the spacing between the plus and minus wiring must be large to reduce parasitic capacitance. However, parasitic inductance increases due to larger area enclosed by the current loop. To prevent magnetic interference, the wirings are twisted every 100 μm, such that the magnetically induced emf is reversed. This not only cancels mutual inductance hence injecting and receiving much less noise to/from the environment, but also reduces slightly the self inductance that leads to peaking.

3.4 Testing Issues

3.4.1 Capturing ADC Output Data

In real applications these high speed ADCs are almost always integrated with DSP, therefore there is no need to transmit the output data stream off-chip. However, we need to test the ADC by itself in this research. Capturing 1.25 GS/s 6-bit data directly poses a problem since very expensive logic analyzers would be needed. Even before this, assuming standard LVDS output for each bit, then 12 pads would be needed. These pads could otherwise be used to reduce package parasitics for important pins such as VDD/VSS.

To reduce the likelihood of unexpected problems involving circuits, PCB, lack of test equipments, any one of them could hamper successful testing of the ADC, two data capturing schemes have been integrated on the prototype chip, such that if one fails the other may work.

In the first scheme, 12 SRAM blocks, each with 4,096-bit are designed and placed on-chip. A 12-bit ripple-carry adder has also been designed to generate address. Each SRAM block takes 1-bit data and 12-bit address with 6-bit row and column decoder. The outputs of the two time-interleaved ADCs are written to the SRAM blocks (in capture mode) with a 625 MHz clock (at 1.25 GS/s).

Due to long wiring of the address buses to 12 SRAM blocks, post-layout simulation is a must to ensure write speed. The simulation showed that although the rise time increases to as much as 300 ps for the 12-bit address bus due to long and dense wiring, the write still works with clock up to 1 GHz.

In read mode, the SRAM is clocked by a parallel-to-serial converter consisting of a 16-bit shift-register and a divide-by-16 divider whose input is externally given. The SRAM is read every 16 cycles of the external clock to load 12 of the 16 DFFs. The output of the shift register is output and can be captured by low-speed logic analyzers.

In actual test, the serial SRAM output was as expected on the oscilloscope, but could not be captured by a logic analyzer due to unknown reason. The memory depth of the oscilloscope was too shallow to capture sufficient number of samples, so this scheme was not used.

The second scheme uses two 8-level Pulse Amplitude Modulation (PAM) transmitters which are simply two 3-bit DACs with 50 Ω output impedance. Figure 3.17 shows simplified schematics of each transmitter. To save pads, the transmitter outputs automatically become high-impedance when an externally given bias current is shut down, such that it can share the same pad with other high impedance CMOS input pads for the SRAM, which is shut down when the 8-PAM transmitter is enabled and vice versa. A large PMOS switch is used to connect and disconnect the 50 Ω on-chip load resistor and VDD.

Each transmitter output is routed on the PCB with 100 Ω differential controlled-impedance trace for about 3 inch before reaching SMA connectors. One side is terminated and the other side is connected to the oscilloscope. 0.1 μF 0603 capacitors

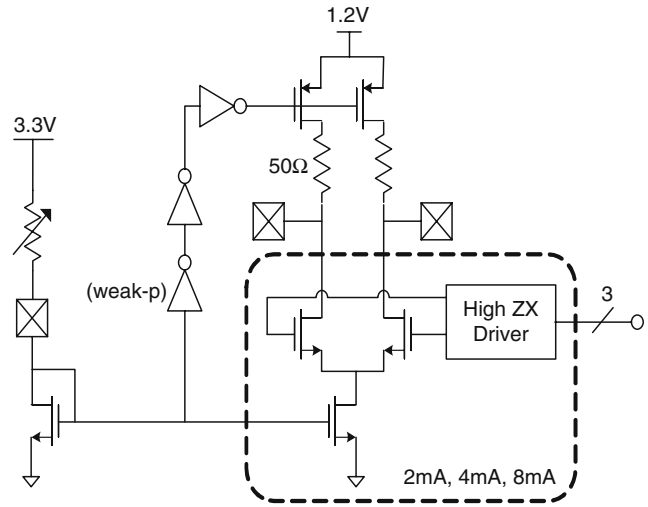

Fig. 3.17 Schematic diagram of the 8-PAM transmitter

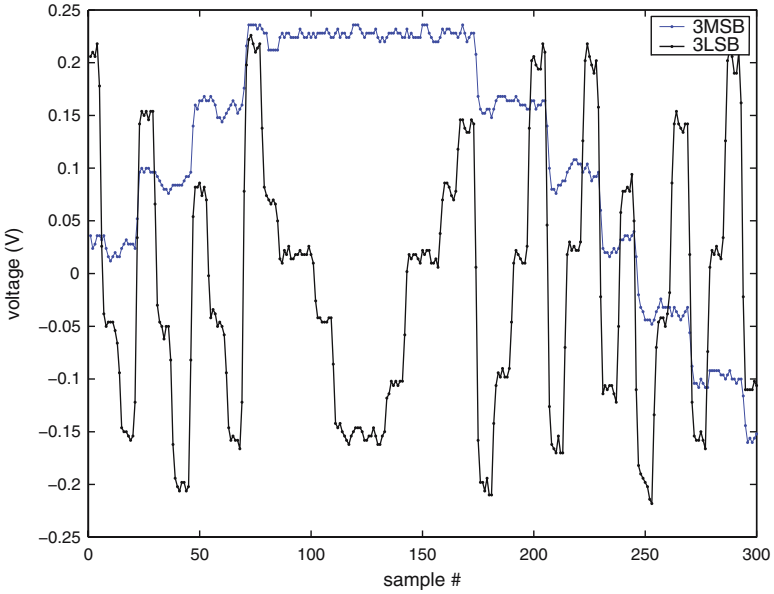

Fig. 3.18 Snippet of captured 8-PAM transmitter output by TDS694C (1.25 GS/s, 20 MHz input signal)

are used for obtain DC bias point that maximize signal swing. If PMOS current sources were used this would not have been necessary, but in turn we may get less clean waveform due to increased parasitics.

Figure 3.18 shows a captured transmitter output by Tektronics TDS694C, a 10 GS/s, 3 GHz bandwidth digital oscilloscope. The ADC is clocked at 1.25 GS/s

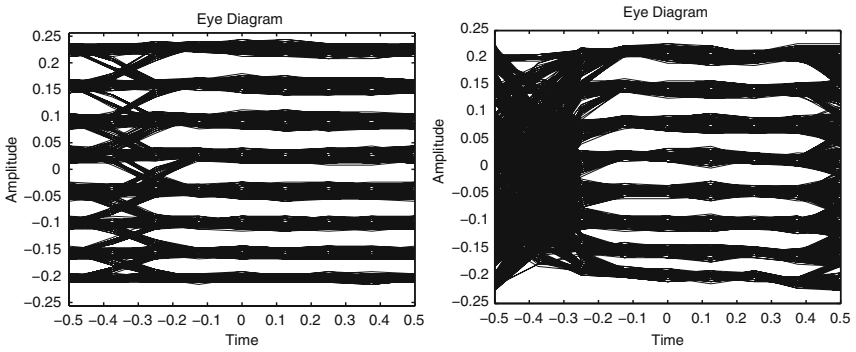

Fig. 3.19 Eye diagram of captured 8-PAM transmitter output (left: MSB, right: LSB, 1.25 GS/s, 20 MHz input signal)

so each symbol is oversampled by 8. Figure 3.19 show the eye diagrams of the MSB and LSB transmitter output. We can see that each level can be clearly identified. The record depth of TDS694C is 120 K so approximately 15,000 samples are captured each time for 1.25 GS/s.

3.4.2 Serial Configuration Interface

To enable better controllability, especially for the PLL described in Chapter 4 with power/phase-noise programmability, various circuit parameters (mainly bias currents for each block) need to be adjusted. Otherwise, many pads have to be devoted for this purpose. This not only reduces the available pads for VDD/VSS but also complicates the PCB, making it hard to design and assemble, especially in this chip which houses two major designs, the PCB may end up with many potentiometers all over.

To solve this issue, a simplified version of serial configuration interfaces which are widely used in industry has been integrated. Instead of using external potentiometers to control each bias current, each is generated on-chip by 3∼4-bit binary weighted current DAC. There is only a few master bias currents which are externally given. The inputs to these DACs comes from a shift register as shown in Fig. 3.20. Some bits are inverted such that the default bias currents are configured when the shift register resets.

A Windows application has been written that controls the printer port to generate the “reset”, “clk”, “din” and “load” signals with correct timing. Figure 3.21 shows a screenshot of the user interface.

Same scheme has been used for the 10-bit ADC described in the previous chapter, which require input of the 6-bit timing calibration code.

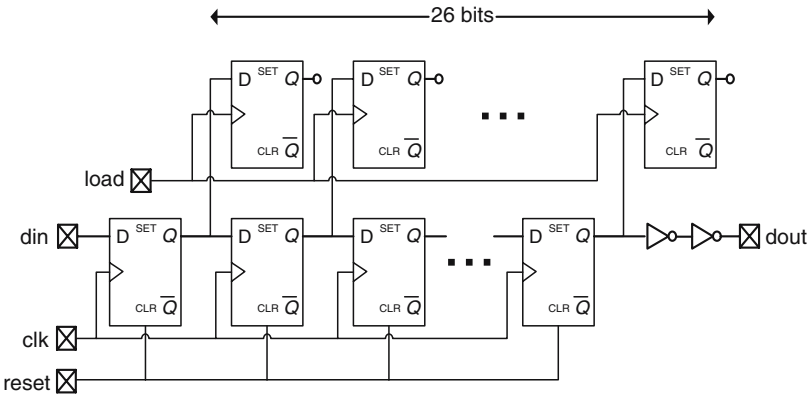

Fig. 3.20 Simplified schematic of the serial configuration interface

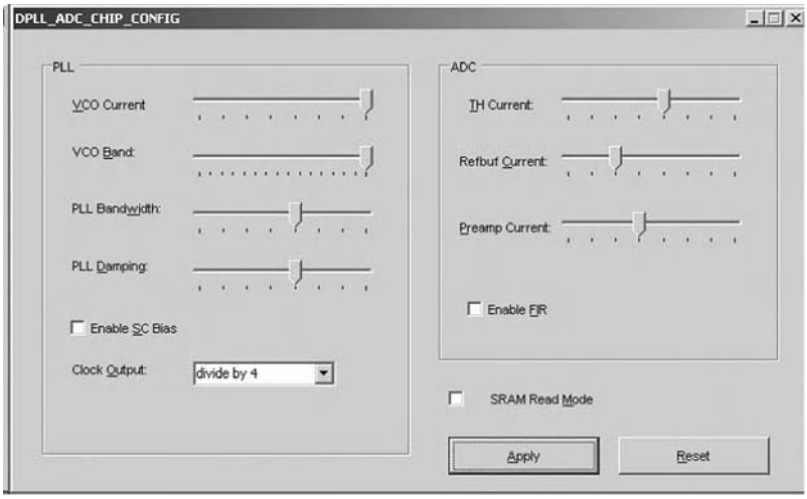

Fig. 3.21 Screen shot of the chip config program

3.4.3 Test Setup

Figure 3.22 shows a simplified block diagram of the test setup for the ADC. The pulse generator is triggered externally by a RF signal generator to get better quality clock. The square wave output of the pulse generator has higher edge slope than the sine wave output of the RF signal generator, thus lowering the jitter contribution of the clock receiver circuits (for detail see Chapter 4).

The transformer (ADTL-18 from minicircuits) has a bandwidth of 1.8 GHz. Above 2 GHz the attenuation becomes so large that the ADC no longer receives any clock. Therefore although the on-chip PLL can be disabled to allow clock given

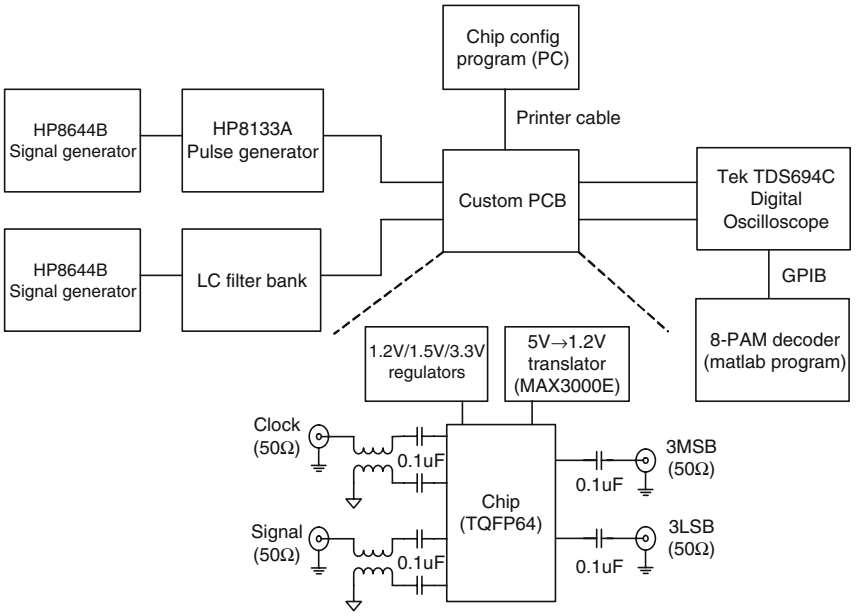

Fig. 3.22 Simplified block diagram of the test setup

externally for <1 GS/s, the multiply-by-8 PLL has been used for all measurements. The filter bank consists of LC bandpass filters from TTE and a low pass filter from minicircuits for >500 MHz.

3.4.4 Evaluation Board Design

Figure 3.23 is a picture of the custom evaluation PC board. It is a 4 layer PCB measuring 5 inch by 5 inch. The 2 internal layers are used for various VDDs and GND. The 50 Ω controlled impedance trace (microstrip line) has been designed according to thickness and dielectric constant of each PCB layer. The much thinner dielectric layers of a standard 4-layer PCB than a standard 2-layer PCB allows 50 Ω traces to be much narrower and more compact. Vias for shielding are placed around these high frequency traces.

The PCB includes three linear regulators to generate 1.2 V (used by ADC and digital part of PLL), 1.5 V (used by analog part of PLL) and 3.3 V (used to bias ESD protection diodes[2] and externally adjustable current sources). 0.22 μH SMT inductors have been used to isolate analog and digital supplies that come from the same regulator. Multiple 0.1 μF 0603 SMT capacitors are placed in parallel close to the DUT to reduce power supply noise.

[2] To reduce capacitance

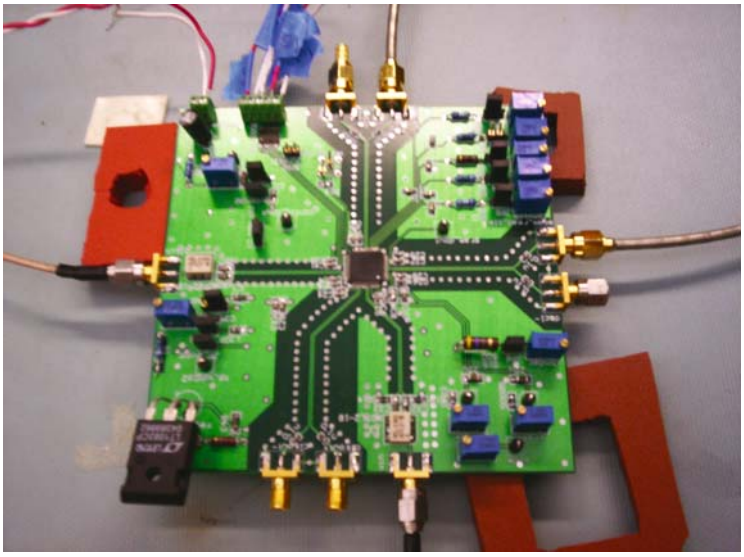

Fig. 3.23 Evaluation Board

3.5 Experimental Results

3.5.1 Summary of Results and Discussions

Figure 3.24 shows FFT of captured ADC output data at 60 MHz 0 dBFS input and 453 MHz −3 dBFS input.[3] The definition of "full-scale" is tricky in high speed ADC, because the signal experiences attenuation by the LC filter, the transformer, PCB trace etc before it reaches the ADC input. These attenuations are difficult to measure. Instead, the "full-scale" used here is based on the ADC digital output, i.e. 0 dBFS means when the maximum amplitude is 63. At DC, 0 dBFS corresponds to about 1.2 Vpp differential (0.3 V to 0.9 V each side) at ADC input.

Thanks to the single front-end T/H that removes the sampling timing mismatch between the 2 ADCs and good matching of the capacitor networks, tones at fs/2 and fs/2-fin are below −50 dBc and do not affect SNDR. Therefore, unlike many previous published experimental high-speed low-power ADCs ([14], [6], [13]) the proposed ADC does not require any external calibration procedures or digital correction, making it a very practical, plug-in replacement for flash ADCs to reduce power by more than 4 times. The only requirement is a 2X clock, which is readily available in many applications where the flash ADC blocks are themselves time-interleaved.

[3] These input amplitudes give the maximum SNDR

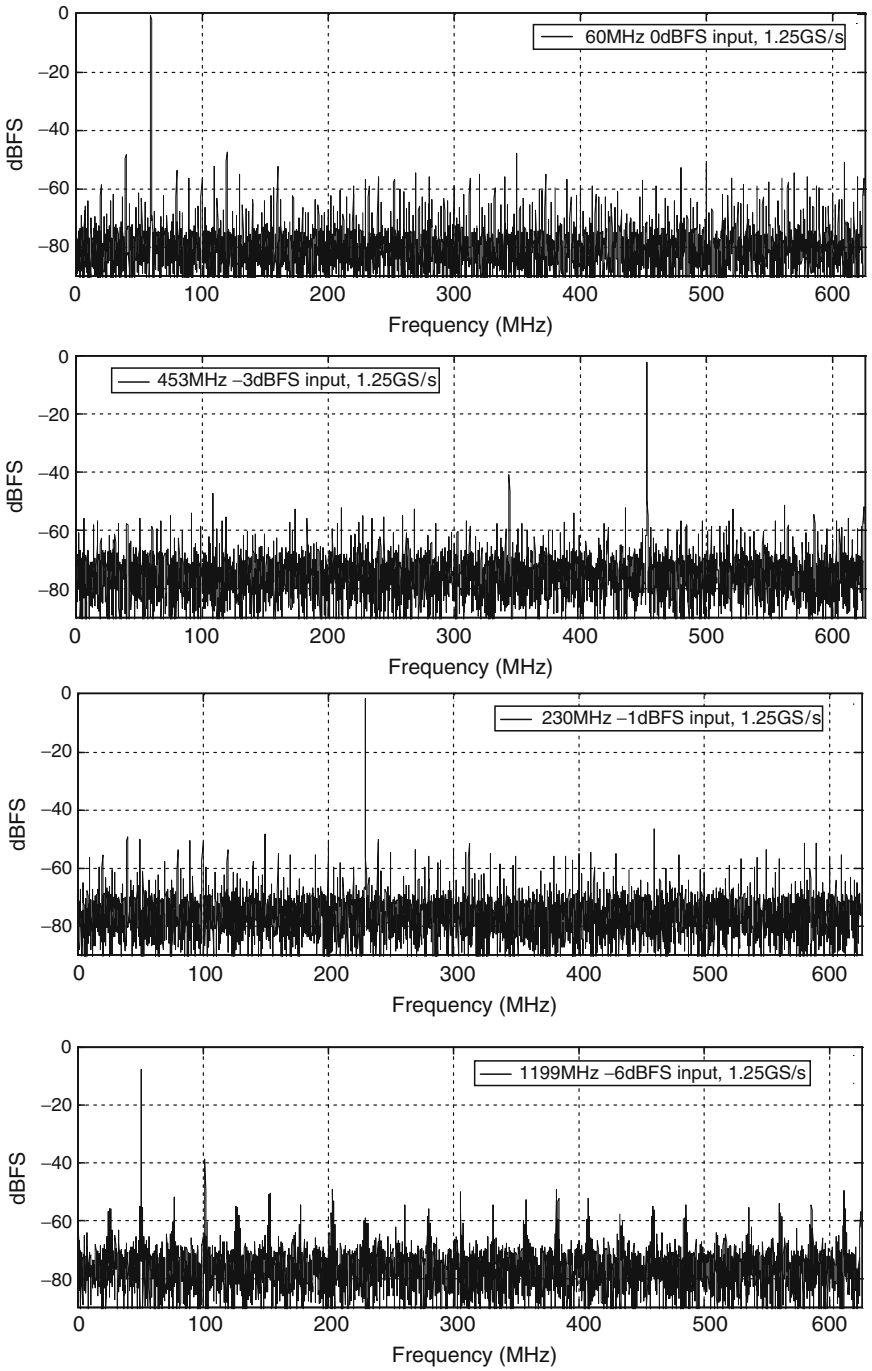

Fig. 3.24 ADC output FFT (14,800 pts) at 1.25 GS/s

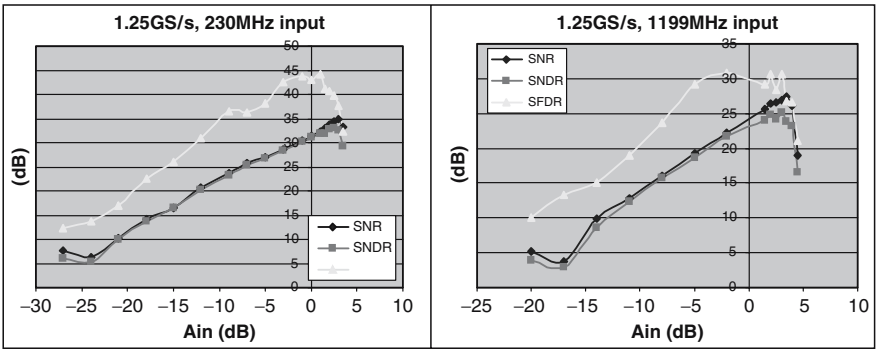

Fig. 3.25 Measured SNDR, SNR and SFDR vs. input signal power

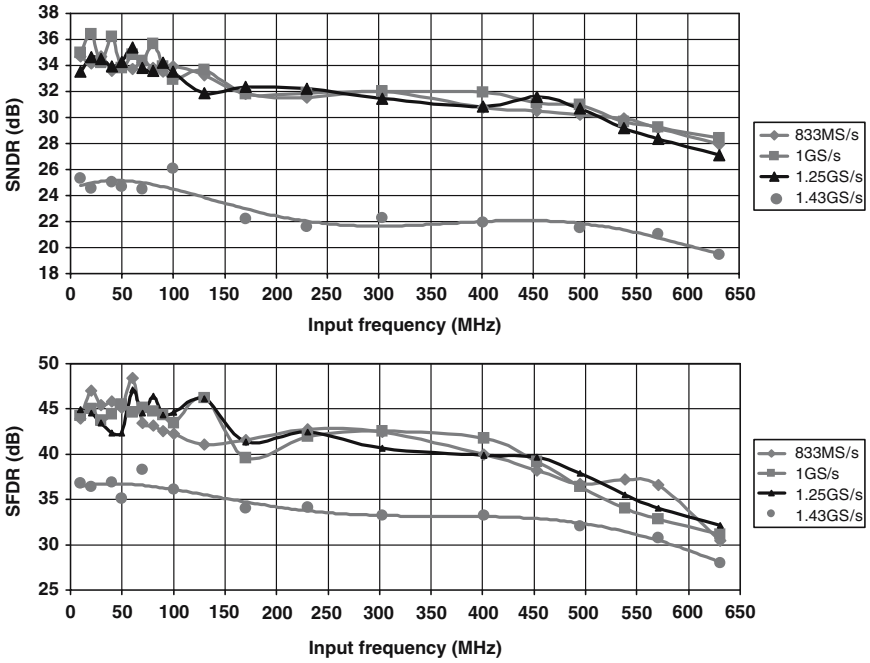

Fig. 3.26 Measured SNDR and SFDR vs. input signal frequency

Figure 3.25 shows SNDR, SFDR and SNR (calculated with the first 5 harmonics removed) vs. input signal power (arbitrary reference) for 230 MHz and 1.2 GHz input signals.

Figure 3.26 is a graph that summarizes the maximum SNDR and SFDR for each input signal frequency and different sampling clock frequency. As signal frequency increases, the signal amplitude that gives the maximum SNDR decreases due to the effect of nonlinear parasitic capacitances in the T/H circuit which degrade linearity. Two or three measurements are taken per each point with different input signal

amplitude close to where the SNDR is expected to peak, and SNDR/SFDR for the amplitude that gives the maximum SNDR are plotted.

Up to 48 dB SFDR and 36.4 dB SNDR for low frequency inputs demonstrate the level of capacitor matching and linearity of the 2 b quantizer with offset self-calibration; $\geq$32 dB SNDR is maintained up to 450 MHz input frequency.

The small unit capacitance (5 fF) of the capacitor network reduces power consumption and also improves linearity since smaller T/H can be used, presenting less nonlinear parasitic capacitance at the input. Nevertheless, due to the relatively large total capacitance (240 fF + bottom plate parasitics) the front-end T/H must drive, measured results (Fig. 3.26) show that linearity degrades when signal frequency f_{IN} is close to half the sampling frequency.

The measured SNDR and SFDR performance close to fs/2 are below 28 dB and 35 dB respectively, which is not as good as some of the state-of-art 6-bit flash ADCs. Interestingly, as f_{IN} is increased further to 1199 MHz, the SNDR and SFDR worsens but not as much as predicted from linear extrapolation of the SNDR, SFDR vs. f_{IN} curve between 500 $\sim$ 625 MHz (Figures 3.25 and 3.26). This can be explained by noting that the difference between the current and previous sample is smaller at 1,199 MHz than at 571 MHz, hence the charge T/H must deliver is actually less. This also partially verifies that the large load on the T/H is causing the performance degradation near fs/2. Improvements can be made by using larger T/H or by using a process with low-k dielectric such that even smaller unit capacitance (Cu) can be used without reducing the physical size of the capacitor (hence maintaining matching.)

3.6 Performance Summary and Comparison

The two time-interleaved ADCs, reference buffers and T/H draw 18.5 mA from a 1.2 V AVDD. The clock buffers and the SAR logic draw 8 mA at 1.25 GS/s from a 1.2 V DVDD. The total power consumption is 32 mW. Table. 3.2 provides a performance summary. The effective number of bits (ENOB) is calculated according to the following formula:

$$ENOB = (SNDR[dB] - 1.72)/6.02. \tag{3.7}$$

For an ideal 6-bit ADC with all the code boundary evenly spaced, the ENOB will be exactly 6. The effective resolution bandwidth (ERBW) refers to the signal frequency at which the SNR drops by 3 dB compared with the SNR at DC.

To give an objective view of these results, Table 3.3 gives a comparison with other 6-bit high-speed A/D converters published in recent years which are representative of the state of the art in CMOS. As technology advances, we can see that the sampling frequency increases and power tends to decrease. However, the lowest reported power for flash ADC is 160 mW. A two-step subranging ADC reports 55 mW power consumption, but this does not include the track-and-hold (ADC driver), hence presenting much larger ADC input capacitance.

Table 3.2 Performance summary

Technology	UMC 0.13 μm CMOS
Resolution	6 bits
Input range	1.2 Vpp differential
Power supply	1.2 V analog, 1.2 V digital
Sampling frequency	1.25 GHz
Latency	2 clock cycle (1.6 ns)
Power consumption	≤32 mW
ENOB	5.8@1 GS/s, f_{IN} = 20 MHz
	5.5@1.25 GS/s, f_{IN} = 20 MHz
	5.0@1.25 GS/s, f_{IN} = 453 MHz
Input capacitance	≤100 fF each side
Active area	0.09 mm^2 including decoupling caps
Die size	1525 μm × 1525 μm
Package	TQFP 64 pin, 10 mm × 10 mm

Table 3.3 Comparison with other published ≥1 GS/s 6-bit CMOS ADCs

Year	Fs (MS/s)	ENOB	ERBW (MHz)	Input capacitance	Power (mW)	Technology	Ref.
2001	1,100	5.3	450	N/A	300	0.35 μm	[17]
		5.7 (900 MS/s)					
2001	1,300	5.0	650	>1 pF	545	0.35 μm	[7]
2002	1,600	5.7	450	N/A	328	0.18 μm	[31]
2003	2,000	5.7	600	N/A	310	0.18 μm	[23]
2005	1,200	5.7	700	0.4 pF	160	0.13 μm	[30]
2006	1,000	5.5	500	>240 fF	55[1]	90 nm	[15]
2008	1,250	5.5	450	0.1 pF	32[2]	0.13 μm	This
		5.8 (1 GS/s)					work

[1] Does not include ADC driver
[2] Analog: 22 mW including ADC driver and reference buffers, digital: 9 mW

3.7 Summary

A new type of high-speed 6-bit ADC has been proposed by combining the successive approximation with the flash architecture. By taking advantage of small-value, highly-matched metal interconnect capacitor available in standard nanometer digital CMOS processes, a proto-type ADC achieved 6-bit resolution without calibration at 1.25 GS/s with 32 mW total power consumption, the lowest reported to date. Comparable dynamic performance as other published flash ADC has also been measured.

Low power consumption is the direct result of more than 10 times less comparators and much simpler thermometer-to- binary encoders than conventional 6 b flash architectures (3 full-adders vs. 57 full-adders in a 6 b Wallace-tree encoder).

The SAR ADC uses 2.5 GHz clock frequency, which is the highest reported for any switched-capacitor circuit to date. High sampling frequency is realized thanks to (i) the availability of small-size but highly matched metal-interconnect capacitors; (ii) low parasitic capacitances and on-resistance of the switches; (iii) reference

buffers with very low DC and AC output impedances; (iv) a proposed digital offset calibration scheme that removes the need for multi-stage preamplifiers; (v) a proposed flip-flop bypass SAR logic; and (vi) high speed digital logic available in nanometer CMOS process in general.

The potentials of passive switched-capacitor circuits for very high frequency applications in advanced digital CMOS processes, where the quality of switches and capacitors only improves every time the process scales down, has been demonstrated in this chapter.

Chapter 4
A 0.4 ps-RMS-Jitter 1–3 GHz Clock Multiplier PLL Using Phase-Noise Preamplification

4.1 Introduction

The trend toward high frequency and broadband digital communication has increased the demand for low jitter, low phase noise clock generation circuits. Due to limited bandwidth on the printed-circuit board, the high cost of high frequency clock source and excessive power dissipation caused by routing high speed clock off-chip, it is necessary to integrate clock multiplier PLLs on-chip.

For high performance DACs with GHz sampling frequency, the input date-rate is usually several times slower, and an on-chip digital interpolation filter is used to select the desired Nyquist zone before the signal is converted to analog domain, leading to relaxed requirements and reduced signal loss of the output anti-aliasing filter. These DACs require clock multiplier PLLs that can provide both low jitter and wide tuning range to satisfy a wide range of customer provided data-rates. Other applications such as multi-standard transceiver and multi-data-rate SERDES also require PLLs with both low jitter/phase-noise and wide tuning range.

The high speed SAR ADC described in the previous chapter requires a 2.5 GHz internal clock, from which the ADC sampling clock is also derived. This clock should have sufficiently low jitter (much less than 3 psrms to affect the SNR negligibly for input signal frequency up to the Nyquist) and the frequency should also be widely adjustable to facilitate debugging of the ADC.

In conventional low jitter clock designs, LC-VCO based PLLs have been dominantly used. The LC-oscillator itself features low phase-noise and low power-consumption if high-Q inductors and capacitors are available. However, LC-VCOs suffer from narrow tuning range and large layout area. Wide tuning range LC-VCOs require elaborate capacitor DACs and amplitude control loops, since the necessary amplifier g_m is roughly proportional to total capacitor in the tank, which quadruples when oscillation frequency is reduced by half. At high end of the frequency tuning range, nonlinear parasitic capacitors dominate the tank capacitance, resulting in much AM-PM conversion and up-converted bias flicker noise. On the other hand, it is easier to design ring-oscillators with wide tuning range, because the oscillation

frequency is determined by R and C, and the R is widely adjustable by controlling the bias current. Compared with LC-oscillators with the same power consumption using an integrated inductor (Q∼10), ring-oscillators have about 20∼30 dB worse phase noise/integrated jitter. To achieve low-jitter, the bandwidth of ring-oscillator based PLLs is usually chosen as wide as possible, and requires a low-jitter reference clock.

In this research a ring-oscillator based PLL has been designed using a wide PLL bandwidth to lower oscillator noise and a phase noise pre-amplification technique to lower PLL in-band noise. With a clean enough reference clock, similar levels of jitter performance as that of an LC-VCO has been achieved with 3:1 tuning range and much smaller layout area.

Deep-submicron/nanometer CMOS processes generally favor wideband PLLs. The PLL in-band noise sources such as divider and phase-frequency detector (PFD) improve because the edge-slope of CMOS swing signal becomes faster each time the process scales (with 2× edge slope and 2× noise bandwidth, jitter reduces by 2× for a given power consumption). On the other hand, the performance of PLL out-band noise source, i.e. VCO degrades because of reduced signal swing due to lower supply voltage.

Reference spur is a major issue when PLL bandwidth is increased as much as possible, because reference ripples on the VCO control line go through less filtering by the loop filter. One cause of the ripple in conventional PLLs is the leakage current, which increases in scaled CMOS processes. With wideband PLL, in-band noise is more important to overall jitter performance. While the noise of divider and PFD can be reduced by maintaining fast edge-slope, that of charge-pump (CP) currents and the loop filter resistor can only be reduced by either increasing the size of loop filter capacitor for a given PLL bandwidth, leading to increased die area, or reducing VCO gain, resulting in reduction of analog tuning range, which must be wide enough to cover temperature variation during continuous operation. A third issue for integrated PLLs is common mode noise coupling to the VCO control line, which becomes more sensitive for wide loop-bandwidth. Because complicated time-domain common mode feedback [39] is necessary to implement a fully differential version of the conventional charge-pump/RC loop-filter, most designs today still use single-ended VCO control schemes.

This paper proposed a new PLL loop filter structure to solve these major problems facing wideband PLLs. The proposed PLL uses fully-differential switched-capacitor based phase-to-voltage converter plus a GmC loop filter to replace the conventional charge-pump plus RC loop filter. Because the phase error is injected to the loop filter as voltage levels rather than as current pulses, leakage and charge-pump current mismatch only result in static phase error but not reference spur. This scheme also allows phase-error preamplification which enables reduction of PLL in-band phase noise floor without increasing loop filter capacitor size or sacrificing analog tuning range. Standard common-mode feedback can be applied to the fully-differential GmC loop filter integral path.

Another feature of this design the ability to program the trade-off between phase-noise/jitter performance and power consumption. In many communication

applications, the phase noise of local oscillator (LO) is specified considering the worst case interferer level. Depending on operating environment, actual interferer levels may be well below this value. In such case the proposed PLL can switch to a low power mode to reduce average power consumption.

4.2 Phase-Lock Loop (PLL)

4.2.1 Phase-to-Voltage Converter and Loop Filter

In the proposed PLL, phase error is converted to voltage by a phase-to-voltage converter (PVC) consisting of a fully-differential charge-pump and switched-capacitor (SC) resistors (Fig. 4.1). The PVC has a similar structure as the one used in [44], which is an improvement over the basic concept first proposed in [34].

When either the UP and DN signal is high, the charge-pump output current charges capacitor C_{PVC}. During this phase, the VCO control lines Vout+/− are isolated by switch SHARE from any disturbance caused by the charge pump switch charge injection or ripple due to up and down current mismatch. After both the UP and DN signal go low and disable the charge-pump, the SHARE switch turns on, allowing the capacitor C_{PVC} to charge share, transferring most of the voltage to Vout+/−. Finally (at the other edge of the reference clock) the SHARE switch turns off and the RST switch turns on in a non-overlapping fashion, resetting C_{PVC} to a common-mode voltage Vcm.

Since the charge-pump is fully differential, the total charge-pump output current is ideally zero. This means the Vcm buffer ideally do not have to provide any current, therefore only requires minimal amount of power even when the charge-pump current is large to achieve a low-noise wideband PLL. This is in contrast with conventional single-ended CP/LF designs where the buffer that precharges the other end of charge-pump may have to be biased with higher current than the charge-pump itself.

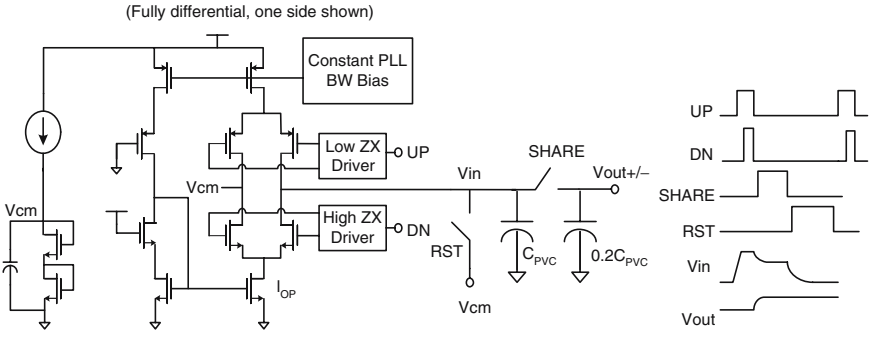

Fig. 4.1 Phase-to-voltage converter (PVC)

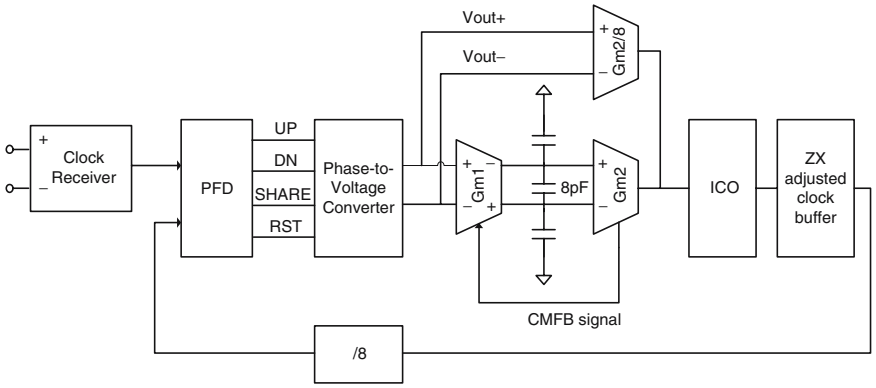

Fig. 4.2 Overall block diagram of the PLL

The resulting PVC output voltages Vout+/− are then integrated by a fully differential Gm-C loop filter to generate the integral path VCO control voltage, while the proportional path control comes directly from the PVC output. Figure 4.2 shows a block diagram of the PLL.

Since the loop filter is periodically reset the leakage in the charge-pump only causes slightly reduced gain. Similarly, leakage in the Gm cell and the capacitor only reduces its DC gain and does not cause ripples on the VCO control voltage. As process scales, smaller switches can be used for the SC resistor, leading to less spur due to switch charge-injection, which is further rejected as common-mode by the fully differential loop filter. Fully differential loop filters also enable 4× reduction in loop filter capacitor (realized by metal-metal fringe capacitance in this design) size by connecting between the positive and negative node, hence doubling the signal swing.

Figure 4.3 shows a simplified schematic diagram of the integral path (G_{m1}) and the common-mode feedback loop. The dominant pole of the loop is generated by the loop filter common-mode capacitors C2 and the high output impedance of G_{m1}. All the other nodes in the loop have low impedance to guarantee stability.

Figure 4.4 shows the proposed phase-frequency detector (PFD) circuit that also generates the SHARE/RST signals. The six-transistor dynamic DFF is a modified version of the "true-single-phase" flip-flop. Compared with standard static DFFs, the number of transistors, especially those loading the clock (F_{ref} and F_{vco}) inputs is greatly reduced, resulting in much less noise and jitter than a textbook PFD built with static logic gates. The edge movements of SHARE and RST do not generate jitter as long as the voltage settling during SHARE is complete. However, it must be guaranteed that SHARE and RST never overlaps, and that RST is off before either of UP and DOWN goes high, which means UP/DOWN signals must be delayed. To reduce flicker noise, the inverter chains that add delays to the UP/DOWN signals use non-minimum length (L = 0.3 μm) NMOS transistors.

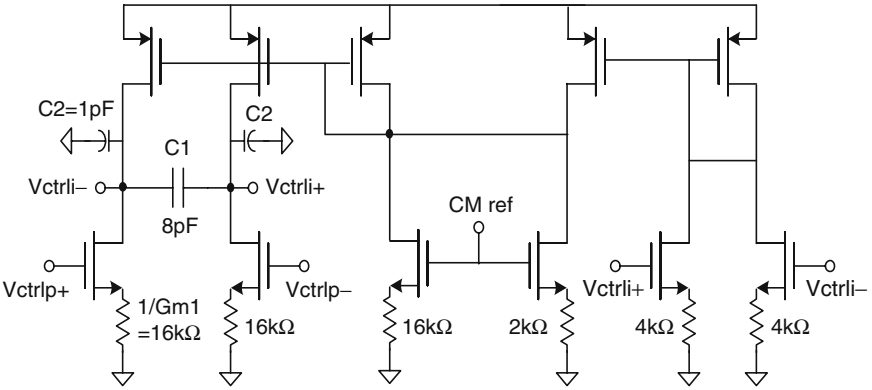

Fig. 4.3 Simplified schematic of G_{m1} and CMFB loop for the integral path

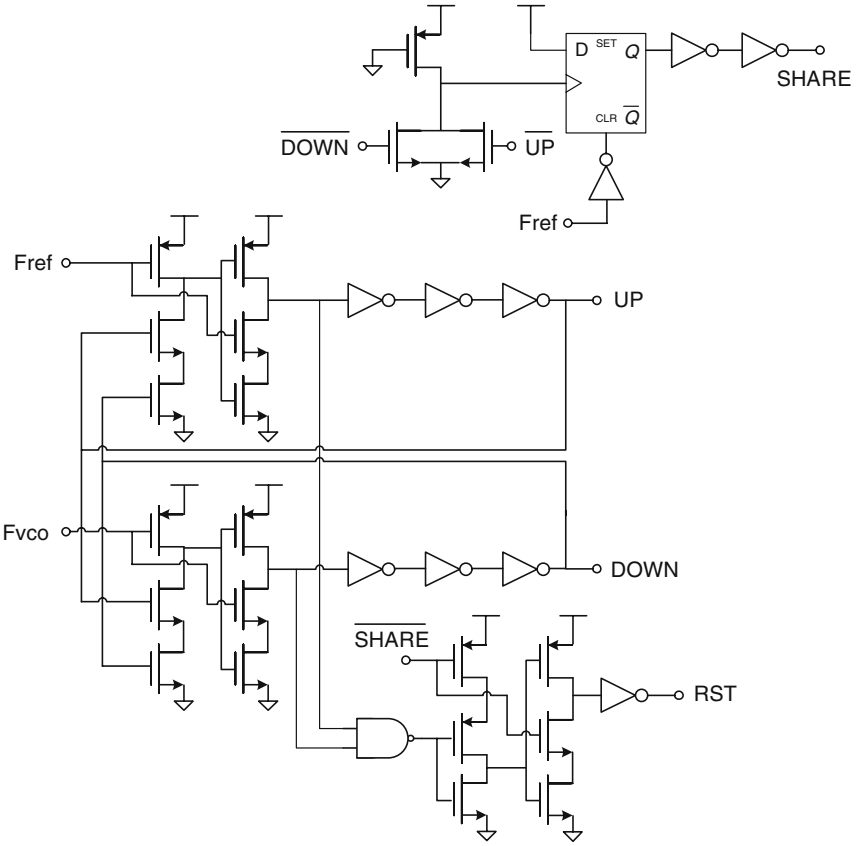

Fig. 4.4 Detailed schematic of the PFD and the SHARE/RST signal generator

4.2.2 Phase Error Preamplification

Because of the availability of high frequency references at 125 MHz ∼ 375 MHz, the PLL unity gain frequency is chosen to be about 70 MHz while the natural frequency is about 10 MHz. The drawback of wide PLL bandwidth is more noise coming from the PFD, divider and charge-pump/loop filter. Although noise from PFD and divider can be reduced by using fast edge-slope CMOS swing signals, large charge-pump currents are required to reduce charge-pump noise which eventually leads to increased size of the loop filter capacitor and die area of the PLL, given a minimum value of K_{VCO} to cover temperature variation during operation.

Unlike conventional PLLs, charge-pump outputs Vout+/- in the proposed scheme need not have swings wide enough to cover possible temperature variation during operation, since the integrator G_{m1}/C suppresses low frequency VCO control signal swing. Therefore, it becomes possible to increase the PVC gain a lot more which is ideally only limited by peak-to-peak high frequency jitter of the free-running VCO. In general, every doubling of PVC gain and halving of G_{m1} and the proportional path $G_{m2}/8$ results in 3 dB decrease in loop filter noise appearing at the PLL output without changing the size of loop filter capacitor.[1]

To understand this quantitatively, we define the SC resistance

$$R = \frac{T_{REF}}{C_{PVC}}, \tag{4.1}$$

where T_{REF} is the reference clock period and C_{PVC} is the capacitor size as shown in Fig. 4.2. For convenience, we also define

$$A = \frac{1}{G_{m1}R}. \tag{4.2}$$

We can see that charge pump current I_{CP} can be made A times larger without changing loop dynamics. If A is sufficiently large, noise of the charge pump current referred at PFD input becomes negligible.

The noise contribution of G_{m1} referred at PFD input is

$$\frac{4kT\gamma}{G_{m1} \times (A \times I_{CP} \times R)^2} = \frac{4kT\gamma}{I_{CP}^2 \times R \times A}. \tag{4.3}$$

The noise of the SC resistor and the proportional path G_{m2} is similarly inversely proportional to A. As A is made larger, the total PLL in-band noise eventually becomes less than that of the conventional design with same loop filter capacitance, despite the additional noise sources. In this design, A $\times I_{CP}$ is 1.8 mA, G_{m1} is 1/16 kΩ and R is 4 kΩ (for 250 MHz F_{ref}).

[1] In reality, parasitic capacitance of the charge-pump switching transistors limits the slew-rate at the charge-pump output to about 10 mV/ps in this process, setting the upper limit on the PVC gain

Similar active PLL loop-filter schemes have been previously proposed such as in [25]. The main advantage is that a virtual ground is maintained at the output of the charge-pump such that the up and down currents match better. The price paid is that the input referred noise of the op-amp gets integrated by the loop filter and appear as PLL in-band noise. These existing schemes do not provide a fundamental advantage over the conventional CP/LF design, because to reduce the PLL in-band noise one still needs to use larger charge-pump currents, an even larger op-amp, smaller loop filter resistors and larger loop filter capacitors.

4.2.3 Constant Loop-Bandwidth Biasing

Compared with a resistor, the sample-reset circuit distributes the charge pump current impulse over the entire reference period, and hence reduces reference spurs [34]. However, a problem with the sample-reset circuit is that its gain is proportional to reference period, so when the reference frequency is reduced, at some point the PVC gain becomes too large and the PLL becomes unstable.

To accommodate wide reference frequency range, the charge pump current is derived from bias circuitry that uses a replica sample-reset circuit to make the PVC plus the G_m cell gain equal to a given reference current I_{bias} regardless of reference frequency. As shown in Fig. 4.5, the charge-pump current I_{CP} is regulated to a value such that it charges the capacitor C_{PVC} up to the voltage I_{bias}/G_{m1} in $T_{REF}/2$ (the clock phase generator uses one divider to generate RST with period of $4 \times T_{REF}$). Therefore,

$$I_{CP}\frac{T_{REF}}{2C_{PVC}} = \frac{I_{bias}}{G_{m1}}. \tag{4.4}$$

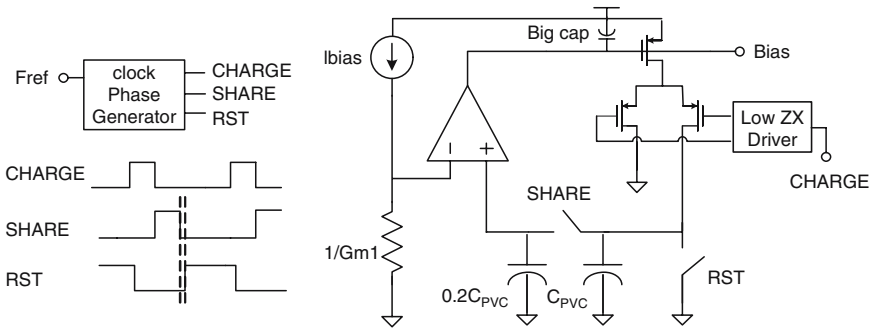

Fig. 4.5 Constant loop bandwidth biasing

The PLL loop gain is given by

$$LG_{PLL} = kI_{CP} \times \frac{T_{REF}}{C_{PVC}}\left(\frac{G_{m1}}{sC_{LF}} + 0.125\right)\frac{K_{VCO}}{N} \tag{4.5}$$

$$= \frac{k}{2}I_{bias}\left(\frac{1}{sC_{LF}} + \frac{1}{8G_{m1}}\right)\frac{K_{VCO}}{N}, \tag{4.6}$$

where k is the current mirror ratio of the charge-pump current, C_{LF} is the effective loop filter capacitor ($\sim$17 pF) and N is the feedback divide-by ratio.

As a result, the same loop characteristics as that of a conventional charge-pump PLL with RC loop filter (where R is 1/8 G_{m1}) is realized.

4.3 VCO and Clock Buffers

4.3.1 Phase Noise and Power Consumption Programmability

While in LC-VCOs only C can be efficiently adjusted, in ring-oscillators both C and R can be readily controlled to determine the oscillation frequency. For a given oscillation frequency we can use large C and small R to reduce noise or small C and large R to reduce power consumption. As shown in Fig. 4.6, the C and R of the current-controlled oscillator (ICO) is adjusted digitally by a 4-bit NMOS inversion mode capacitor DAC (CDAC) and by a 3-bit current DAC (IDAC). To switch modes, first the CDAC input is changed, and then the IDAC is adjusted according to a look-up table to enable the PLL to regain lock. To overcome process variation, standard digital frequency calibration procedures such as [41] can be repeated for each CDAC code at power-on to determine the values in the look-up table. As shown in Fig. 4.7, the analog tuning range is wide enough (>2 LSB of the IDAC) which is more than enough to cover temperature variation during operation.

An undesirable side-effect of adjusting VCO phase-noise performance is the change in VCO gain, which decreases as more capacitors are switched on. The decrease in PLL bandwidth is compensated by increasing I_{bias} in Fig. 4.5, which is digitally controlled by 3 b code at the same time CDAC code is increased.

The VCO is a 3-stage current starved CMOS ring-oscillator. Small cross-coupled inverters are used in each stage to prevent common-mode oscillation. By using a single combined current source to supply the three stages, higher supply rejection is achieved because the current source always stays in saturation [26]. To provide additional 10$\sim$20 dB of supply rejection a RC supply filter [27] has been used.

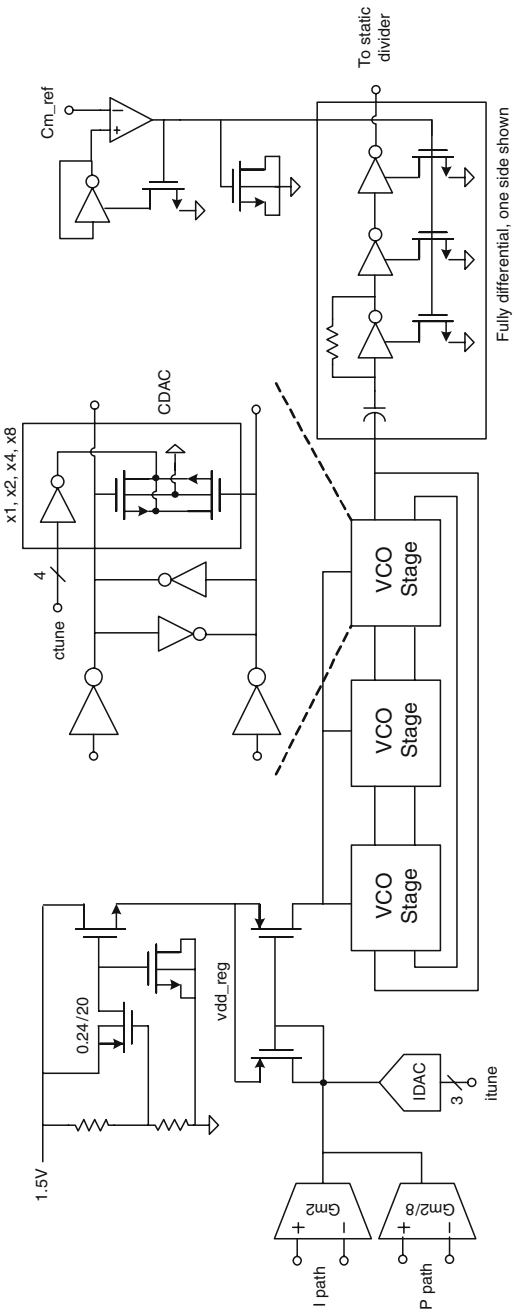

Fig. 4.6 VCO with C and R control

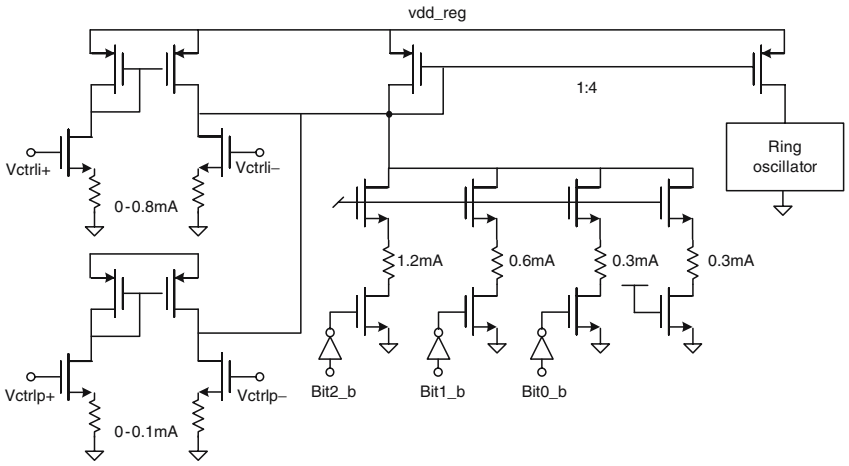

Fig. 4.7 Simplified schematic of Gm2s and the IDAC

4.3.2 VCO Buffer with 50% Duty Cycle Output

One circuit worth mentioning in Fig. 4.6 is the VCO output buffer with zero-crossing (ZX) control through replica biasing. The function of the VCO output buffer is to convert the sine wave like waveform inside the ring-oscillator with frequency dependent amplitude, to a 50% duty cycle, high edge slope (40 ps rise time) ideally square-wave 1.2 V CMOS swing clock.

Fifty percent duty cycle is desirable since it is only with 50% duty cycle that the plus and minus clock in a differential clock path switch at the same instant, causing the smallest amount of common mode disturbance. High edge slope is needed to reduce voltage noise to time-domain noise (jitter) conversion gain. Without high edge slope, large power consumption must be used to lower the input referred voltage noise of each transistor that handles the clock signal to achieve low jitter. But when the edge slope is made as high as possible, only the first few stages in the clock buffer that amplify the low edge slope clock to high edge slope need to be low noise.

A 150 fF metal-metal fringe capacitor is used each side to AC couple the signal. The DC level is set to the "trip-point" of the CMOS inverter, such that the duty cycle of amplified clock is close to 50%. This is achieved by generating the DC bias using an inverter with input connected to output through a large (10 kΩ) resistor, such that the same inverter can be used for both DC bias and signal amplification. This is a standard technique that has been used in numerous other VCO buffer designs.

However, this alone is not enough to obtain an exactly 50% duty cycle, when several more inverter stages must follow to further sharpen up the edge slope. When the signal swing is small, and with the AC coupling capacitor (which enables the waveform to go above VDD or below VSS) the input waveform can be reasonably

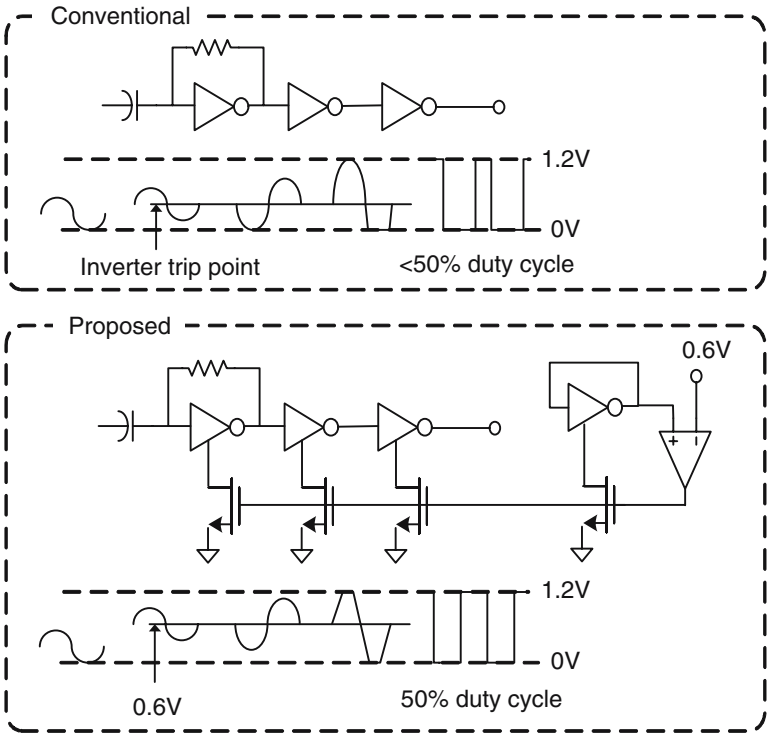

Fig. 4.8 Conventional vs. proposed 50% duty-cycle VCO output buffer

symmetric around the trip-point, then at the inverter output the waveform may also be symmetric around the trip-point. However, eventually the waveform will be clipped by either supply rail (e.g. if NMOS is stronger than PMOS, then the trip-point will be less than VDD/2 and the waveform will be clipped by VSS first,) and lose its symmetry. This common-mode asymmetry will be amplified by the succeeding inverter stages, i.e. if the waveform is clipped by VSS, then at the next output the zero-crossing (ZX) will go slightly below the trip-point (duty cycle $<50\%$), and the ZX will go a lot more above the trip-point (duty cycle $>50\%$) at the output of the following inverter stage (Fig. 4.8).

To avoid this "duty-cycle distortion" as called in [27], multiple AC coupled stages are used in a previous work [27]. This can only correct small ZX errors and comes at the cost of increased layout area due to the large AC coupling capacitor.

This work proposes another approach to solve this problem. Each inverter in the VCO buffer has two NMOS connected in series, the bottom one controlled by a feedback loop to control the pull-down strength such that the "trip-point" is at VDD/2. This way, the waveform will stay symmetric much longer, even after being clipped by VDD and VSS, until the edge-slope becomes so sharp at the VCO buffer output that it doesn't matter if NMOS is a little stronger than PMOS, after which

point simple CMOS logic gates without ZX control are used (Fig. 4.8). The replica biasing loop approach cancels process variations that make it impractical to try to size NMOS and PMOS to set the trip-point at mid-supply.

4.3.3 Reference Clock Receiver

The reference clock receiver is very important to realize low-jitter wideband PLLs. The wide bandwidth allows much more noise coming from the reference path to affect the PLL output. According to PNOISE simulation, 6 mA bias current has been used in the first stage amplifier such that its noise contribution is negligible.

Figure 4.9 shows a simplified schematic of the clock receiver. Differential pair is used as the first and second stage to remove common mode noise and disturbance that the PCB traces and bond-wires may pick up. The DC level of the first stage is generated on-chip by connecting to the common-mode of the 100 Ω differential on-chip termination resistor. The second stage uses a standard technique where current mirrors are used to shift the DC levels such that the low swing differential waveform is converted to 1.2 V CMOS swing clock signal. The common mode is also cancelled. The edge slope is higher than input due to the amplification by the first stage, so less current can be used for the second stage.

4.4 Experimental Results

4.4.1 Test Setup

Figure 4.10 illustrates the PLL test setup. The reference clock is given as a sine wave by HP8644B (on a lab bench with Agilent E5052A signal source analyzer) and by Rhode&Schwartz SMHU (on a lab bench with Agilent E4443A PSA spectrum analyzer). The difference of signal generator appears in measured phase noise at low offset frequency (<100 kHz). Although E5052A has lower internal noise floor, therefore can make higher accuracy measurements, it can only measure phase noise up to 40 MHz offset, which is too narrow for this wideband PLL. To measure rms jitter integrated to an offset frequency well beyond the PLL bandwidth, E4443A PSA spectrum analyzer is used.

The output buffer is a NMOS differential pair with 8 mA tail current loaded with 50 Ω on-chip resistor. One side of the differential output is AC coupled to spectrum analyzers for phase noise measurement with the other side terminated with 50 Ω.

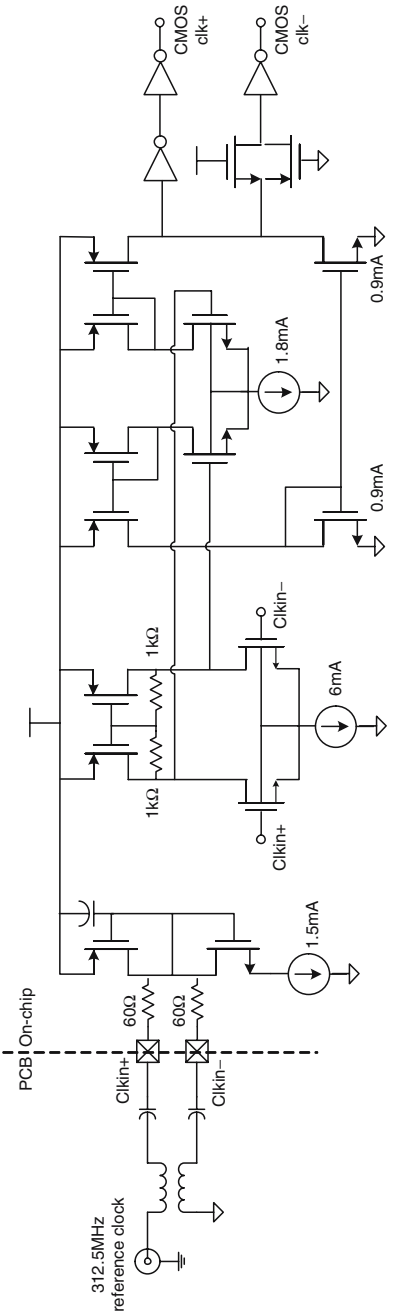

Fig. 4.9 Simplified schematic of the reference clock receiver

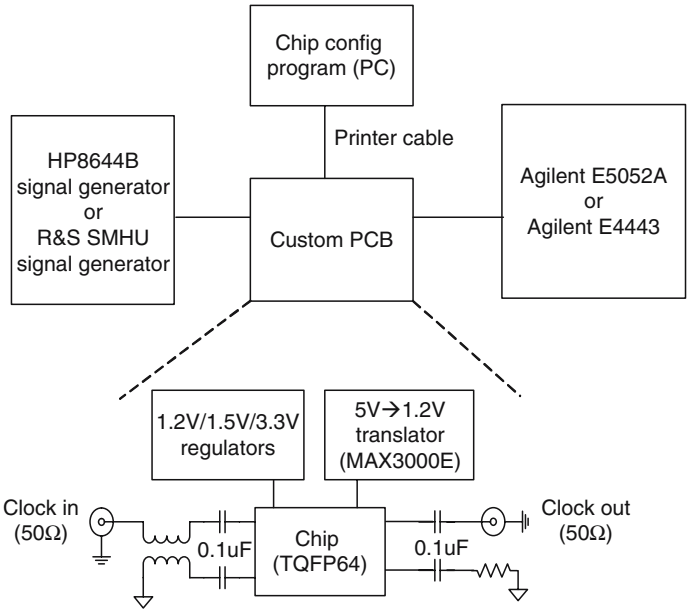

Fig. 4.10 Simplified block diagram of the PLL test setup

4.4.2 Measurement Results and Discussions

Figure 4.11 shows the measured PLL in-band phase noise using Agilent E5052A signal source analyzer with HP8644B signal generator as the 250 MHz reference. Less than −118 dBc/Hz PLL in-band phase noise is maintained for >100 kHz offset. Figure 4.12 shows the RMS jitter integrated from 3 kHz to 300 MHz offset at 2.5 GHz output at the highest power mode. Figure 4.13 compares the phase noise difference at the highest and lowest power modes at 2 GHz (after charge-pump current adjustment to compensate for change in VCO gain). In the frequency ranges where VCO noise dominates, spot phase noise changes by approximately 10 dB. Figure 4.14 summarizes measured performance and VCO currents over several frequencies of interest. Above 2.4 GHz, the power/performance tuning range decreases mainly because the maximum CDAC setting can no longer be used. As process scales down, however, the proposed scheme can be used to achieve wider power/performance tuning at higher output frequencies due to reduced unswitchable parasitic capacitances.

Figure 4.15 shows measured spur performance. At 900 MHz output (112.5 MHz reference) the spur is −68.5 dBc, even with very wide PLL bandwidth evident from the spectrum. This demonstrates the effectiveness of proposed scheme in reducing reference spurs. However, at 2.7 GHz output (337.5 MHz reference) the spur (at 3.0375 GHz) increases to −48.3 dBc despite the PLL bandwidth being the same. The spur at 2.3625 GHz is about 10 dB lower. These results indicate that the spurs

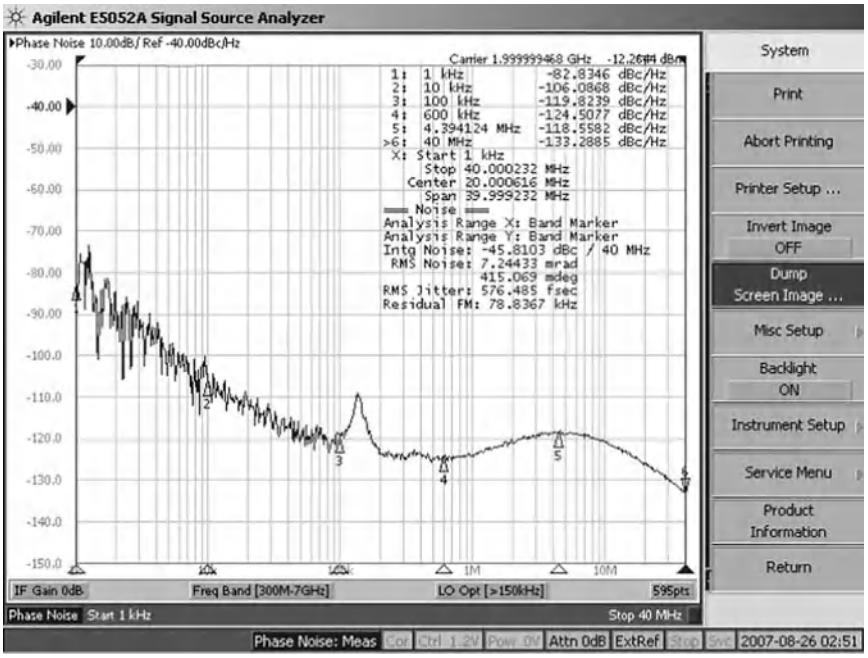

Fig. 4.11 PLL in-band phase noise at 2 GHz output

at high output frequencies are caused by reactive coupling paths to the VCO other than the loop filter, such as substrate and VCO supply bond-wire coupling. The PLL floorplan (Fig. 4.16) may be improved by placing the PFD, which is a major source of spurs, away from VCO supply filter.

Figure 4.16 shows the die photo with the PLL portion enlarged. The PLL occupies only 0.07 mm^2 where the 8 pF differential loop filter capacitor takes up less than 20% of the layout area. Much of the layout area is filled with MOS decoupling capacitors for DVDD (supplies divider/PFD/charge-pump) and AVDD (supplies the G_ms and the VCO). The measured DVDD current is 6.2 mA at 2 GHz and 7.1 mA at 2.4 GHz.

4.4.3 Comparison with Existing PLLs with Similar Output Frequency Range

It is difficult to make a fair comparison among different PLLs. This is because there are many parameters such as divider ratio (which is sometimes not even disclosed,) PLL bandwidth required by the application, flicker noise coefficient of the process, and measurement setup (some authors use oscilloscope to measure jitter while others give phase noise results without specifying jitter.) For example, a multiply-by-16 PLL has 6 dB higher gain of noise from divider, PFD and charge-pump to output

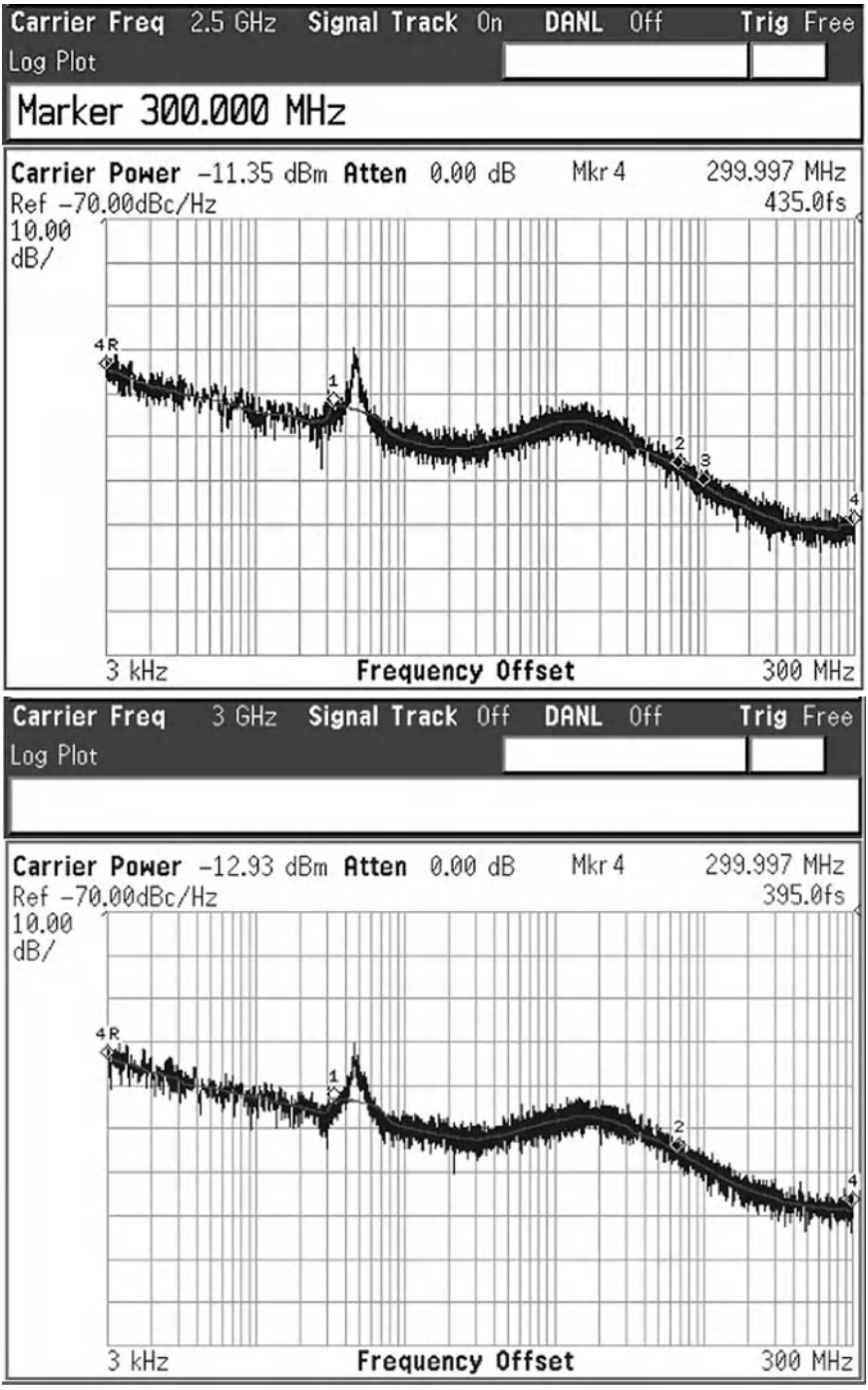

Fig. 4.12 Integrated jitter from 3 kHz to 300 MHz at 2.5 GHz and 3 GHz outputs measured using Agilent E4443A

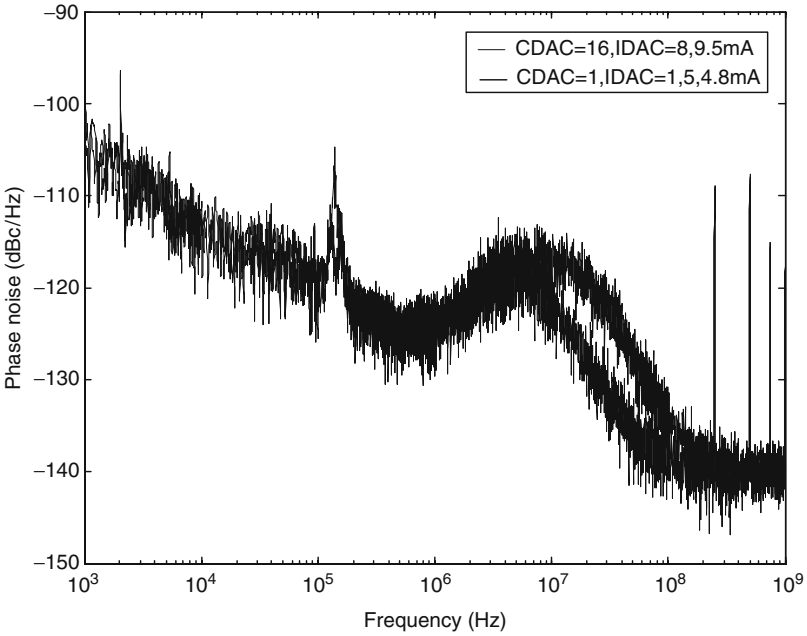

Fig. 4.13 Phase noise at 2 GHz for the lowest and highest power modes measured using Agilent E4443A

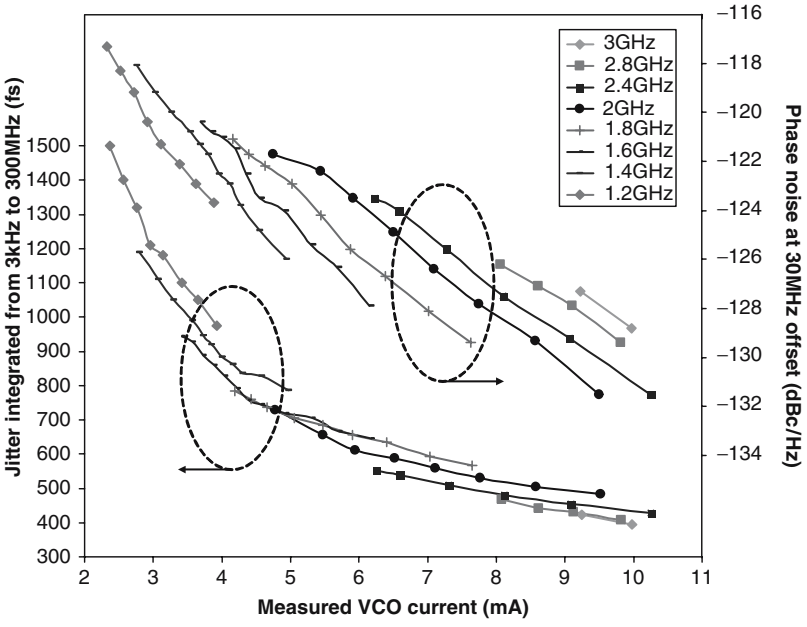

Fig. 4.14 Summary of measured rms jitter and phase noise at 30 MHz offset vs. VCO current

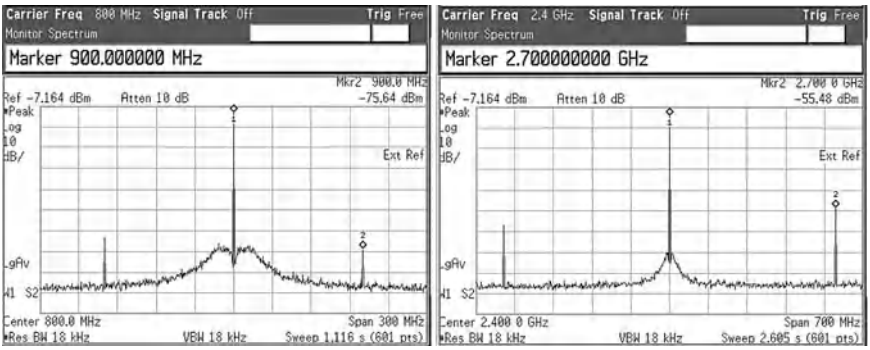

Fig. 4.15 Spurs at 800 MHz and 2.4 GHz output

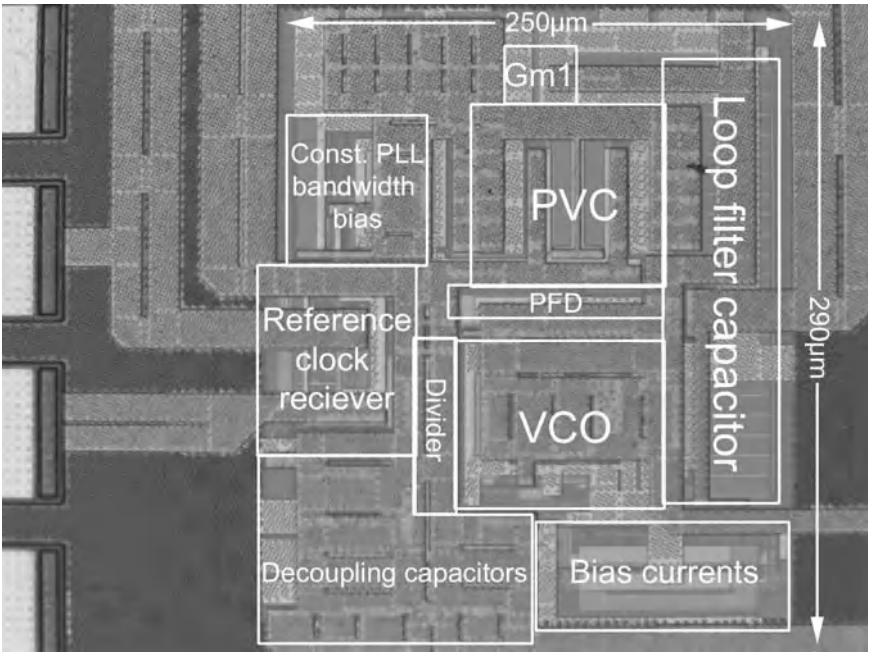

Fig. 4.16 Die photograph of the PLL

PLL in-band phase noise than a multiply-by-8 PLL, however the update frequency is half, making the injected noise power 3 dB less, resulting in net 3 dB higher in-band phase noise if everything else is the same. Table 4.1 nevertheless gives a best effort comparison with PLLs published in recent years with similar output frequency range. The jitter results are best case reported RMS jitter at room temperature. Reference [12] is an LC-VCO based PLL intended to generate a single frequency. The jitter result for reference [40] is a 5 GHz while the that for this work is at 2.5 GHz. We can see that the proposed design demonstrates state-of-art performance in terms of tuning range and random jitter.

Table 4.1 Comparison with other published PLLs with similar output frequency range

Technology	Range	Power	Jitter[1]	Die area	Ref
0.18 μm CMOS	0.125−1.25 GHz	90 mW	9 ps	0.24 mm^2	[34]
0.12 μm CMOS	2.488 GHz[2]	35 mW	0.86 ps	0.7 mm^2	[12]
0.18 μm CMOS	0.5−2.5 GHz	25 mW	2.36 ps	0.15 mm^2	[3]
90 nm CMOS	1−3 GHz	20 mW	0.94 ps	0.016 mm^2	[46]
90 nm CMOS	4.3−7.4 GHz	150 mW	0.7 ps[3]	0.49 mm^2	[40]
0.13 μm CMOS	1−3 GHz	23 mW	0.43 ps[4]	0.07 mm^2	This work

[1] Best case reported RMS jitter at room temperature
[2] This is an LC-VCO based PLL intended to generate a single frequency
[3] At 5 GHz
[4] At 2.5 GHz

4.5 Summary

A 1–3 GHz tunable, low jitter multiply-by-8 ring-oscillator based PLL achieving $<$0.5 ps rms jitter (for output frequency $>$2 GHz) integrated from 3 kHz to 300 MHz offset has been designed and implemented in a standard 0.13 μm digital CMOS technology. Highlights of the proposed techniques include: (i) a phase error preamplification technique is used to lower charge-pump noise without increasing loop filter capacitor size; (ii) a new biasing scheme for switched-capacitor based phase-to-voltage converters makes PLL bandwidth constant independent of reference frequency; (iii) a ring-oscillator with programmable resistor and capacitor enables adjustable power/noise trade-offs for a given output frequency; and (iv) a VCO output buffer replica biasing scheme stabilizes output duty cycle at 50% without using multiple AC coupling stages.

Chapter 5
Conclusions and Future Directions

Three analog functional blocks incorporating numerous architecture and circuit level innovations have been designed, laid out, fabricated in standard a 130 nm digital CMOS process and successfully tested. This chapter makes conclusions that apply to the entire book, while avoiding repeating conclusions specific to each project which can be found in the "Summary" section of each previous chapter.

No engineering research is meaningful unless it meets the changing demand of our society. As far as I understand, there are two main market segments for advanced integrated circuits.[1] One is for high performance analog/mixed-signal ICs, the other is for high volume consumer ICs. The former includes high resolution, high speed data converters, high speed and/or high linearity, low noise and offset op-amp, or high voltage, high power amplifiers and other discrete analog components, which are often used in expensive, specialized measurement equipments, professional audio, medical or in military applications. In this segment, the trend is for each company to develop its own analog IC processes (both silicon and compound semiconductor) optimized for analog performance, but not level of integration [10]. Circuits and architectures are very mature with little room for innovation, which is often specific to each process if there is any, and the process technologies themselves are developed to make conventional analog circuit and architecture work better, hence removing the need for their innovation.

The high volume consumer IC segment includes VLSIs such as microprocessors, graphics chips, cell phone processors, chips used in PCs and other consumer products such as those for USB, HDD, DVD, Ethernet interface and WLAN, and more recently chips in HDTVs. These are the so called "system-on-chip" (SoC). We can see a very different picture here than in the high performance segment. The technologies used are the latest, standardized nanometer digital CMOS that follow the Moore's Law. Industry standards set specifications for the analog interface and it does not make as much sense to exceed the standards as in the high performance market. In this segment, the trend is toward higher level of integration (to lower

[1] Integrated circuits that do not fall into this category can be considered "commodity" and brings minimal reward for designers

cost and form factor) and lower power consumption. Analog interface circuits that are needed in this segment are faced with lower supply voltage and smaller low frequency voltage gain which limits the use of many transistor-level circuit techniques, and only a few basic, proven transistor-level circuit topology can be used and proves to be effective. It is then required to innovate in architecture level such that the same function can be implemented robustly with small power consumption and silicon area.

Architecture level innovations involve the following aspects, most of which have been explored in this research. Further exploration is suggested as the future direction of a similar research:

1. To use higher sampling frequency and smaller sampling capacitor to over-sample analog signal, such that more signal processing move from continuous-time analog domain to discrete-time or digital domain, where they can be performed with higher dynamic range and less power and silicon area, not to mention higher flexibility, robustness against process/temperature variation and testability.
2. Replacement of analog feedback with digital feedback, which does not take large area to realize large time constants, provides higher dynamic range, and can be better controlled for stability without complicated compensation schemes. The use of digital feedback is rapidly expanding, including, but is not limited to delta-sigma modulators, SAR ADCs, digital amplitude control loop for LC-VCOs, DC offset auto-calibration in direct-conversion receivers, "all-digital PLLs" with digital loop filters and digitally controlled switching regulators. As logic speed increases digital feedback control can replace analog feedback for more applications.
3. Increase of programmability of analog functional blocks which are to be controlled by back-end DSP. Today SoCs are required to support multiple standards and data-rates. The solution is to provide an increased level of digital programmability which may also allow dynamically making trade-offs between gain, noise, linearity, bandwidth and power consumption, which leads to lower average power consumption in a changing operating environment [11].
4. Digital calibration to correct analog error. Some can be considered as a special case of "digital feedback", but we don't have to close a loop. A current-steering DAC implemented in 0.13 μm CMOS used an on-chip sigma-delta ADC to measure mismatch of each unit current cell in a calibration mode and then used an error DAC to cancel the mismatch during operation [9]. Low power and higher AC linearity has been achieved as a result of not having have to use large current cells to achieve DC matching. The same technique can be applied to ADC to build a high resolution, high speed A/D converter in deep-submicron CMOS that lacks DC accuracy. We can put a sigma-delta DAC on-chip to generate a slow, but very linear ramp as the input and measure the ADC output code in a calibration mode. Then we can correct the ADC output during operation using a look-up table built during the calibration mode. The only requirement for the analog part is that one ADC output code corresponds to only one ADC input voltage, which may necessitate additional calibration of residue gain or getting rid of residue amplification by using two-step subranging architecture.

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