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Electrical Variability due to Layout Dependent Effects: Analysis, Quantification, and Mitigation on 40 and 28nm SOC Designs

Mark Zwolinski
mz@ecs.soton.ac.uk

Agenda

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1. Introduction
2. Stress Effects
3. Variability Analysis Flow
4. Results and Discussions – 40nm CMOS Technology
    a) Transistor variations: Vth, Idsat, Ioff
    b) Cell timing and leakage variations
5. 28nm Results
6. Mitigation Strategies
7. Conclusions

1. Introduction

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- **Layout dependent variations (context dependent):**
  - **A. Variation in poly pitch.**
  - **B. Well-proximity effects.**
  - **C. Intentional and unintentional Stress: LOD, STI, DSL and SiGe.**
  - **D. Pattern dependent dishing and oxide erosion.**
  - **E. Rapid thermal anneal (RTA) process.**
- **We focus on stress effects including Diffusion Spacing Effects (OSE) and Well Proximity Effects (WPE).**
- Cadence tool LEA is used to analyze stress effects as results of layout context.
- Device and cell variability due to stress are analysed.
- Mitigation strategies for lower systematic variability are discussed.

2. Stress Effects

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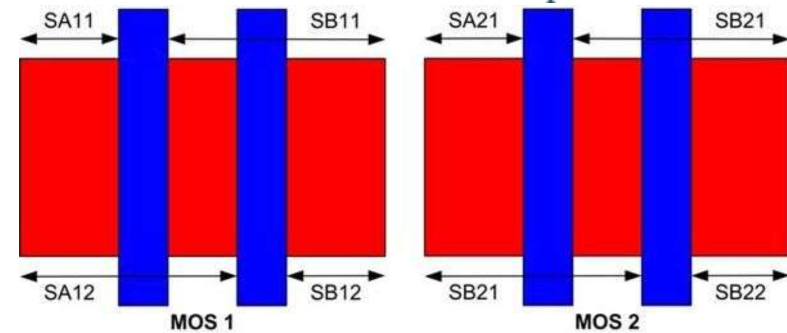
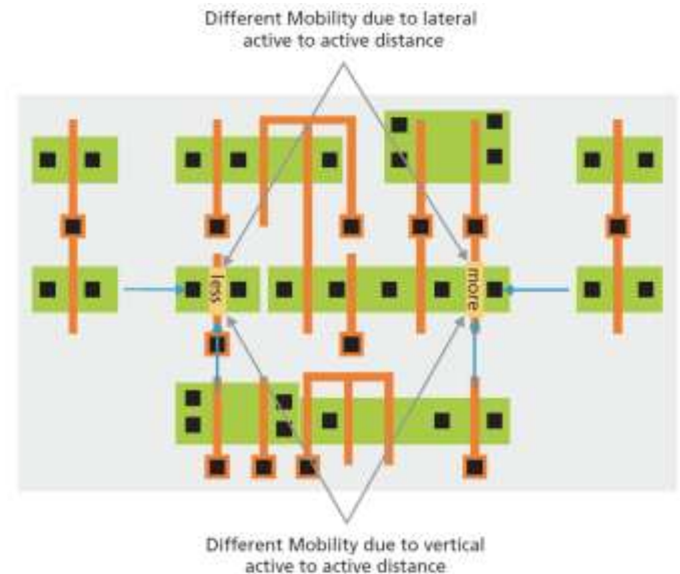
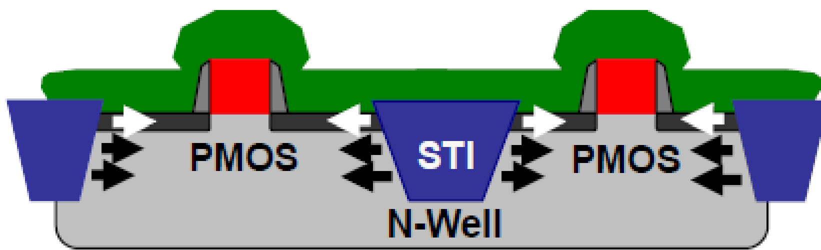
- **Unintentional stress: LOD and STI:**

➢**LOD** effect is due to mechanical compressive stress induced at boundary of OD.
➢Proportional to the distance to OD boundary.
➢Layout dependent but not context dependent.



➢**STI** becomes compressive as the wafer cools down.
➢The wider STI the higher the stress.
➢Width of STI (Active to Active Spacing) has a strong role in determining the stress.
➢Context dependent.





2. Stress Effects (Cont.)

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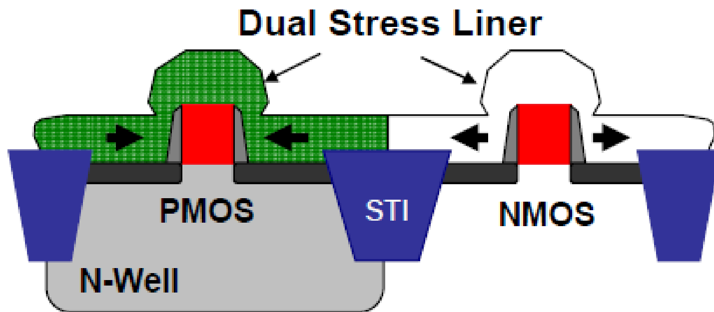
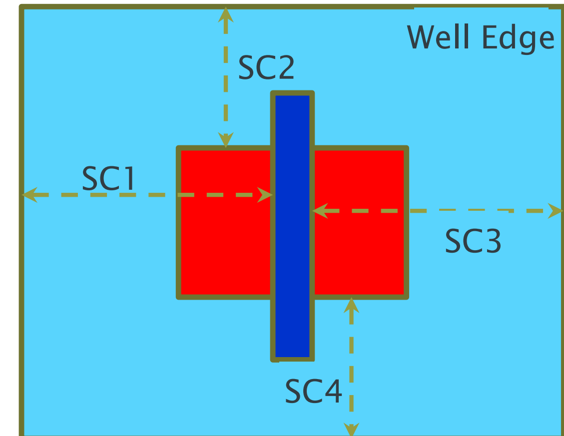
- **Intentional stress: DSL and e-SiGe:**



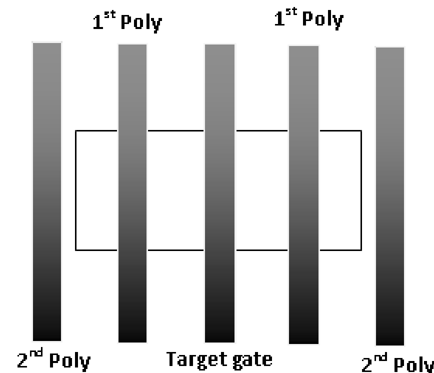
- DSL applies a SiN film to create tensile stress on n- and compressive stress on p-MOS.
- The boundaries of compressive and tensile are synthesized from the well layer.
- Context dependent.

- **Well Proximity Effects: WPE →**
  - MOS close to well edge exhibits a difference in Vth and Ids from that of the device located remotely from well edge.



- **Poly Space Effects (PSE)**

not context dependent if cells have dummy polys (1st polys have same dimensions as poly gate), and effects of 2nd polys are less.



3. Variability analysis flow

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- **Library Variability analysis**
  - Understand and quantify context variability
  - Perform quantified area/timing variability architectural and layout tradeoffs
  - Prioritize various layout optimizations or mitigation strategies
  - Optimize selection of context for characterization
- **Device Variability analysis**
  - Vth characterisation.
  - Idsat characterization.
  - Ioff characterization.
- **Path Variability analysis**
  - Analysis of critical paths, Clock Trees, etc
  - More accurate timing analysis and reduce margins

3. Path Variability

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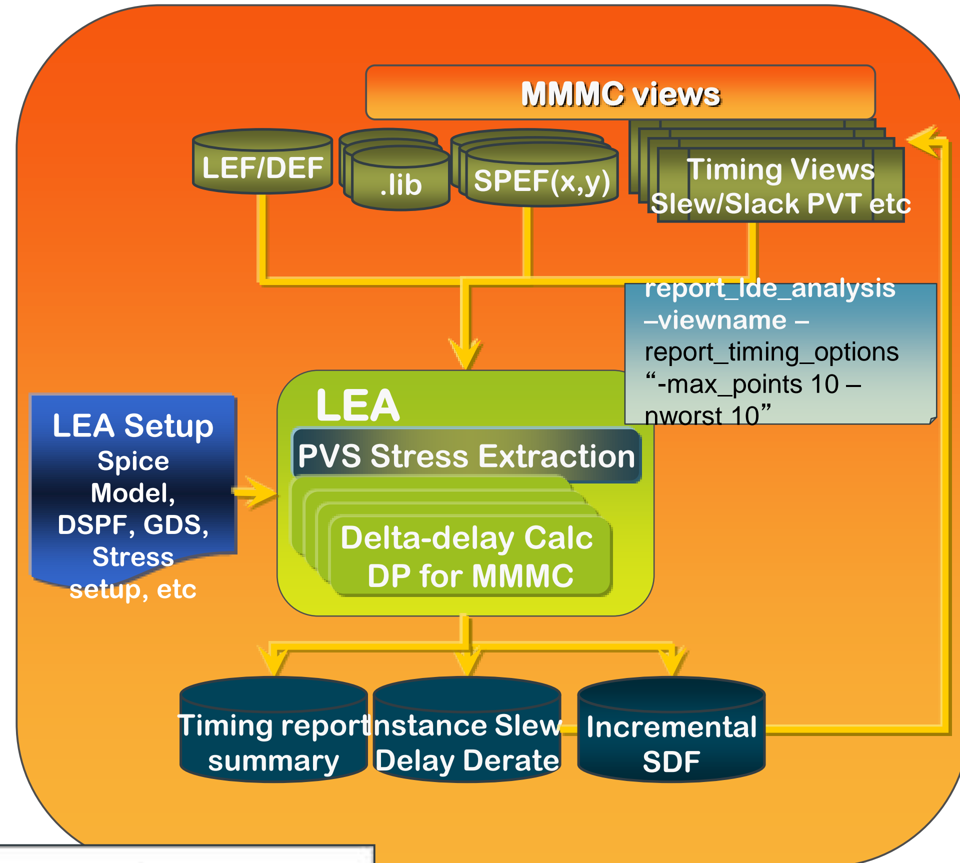
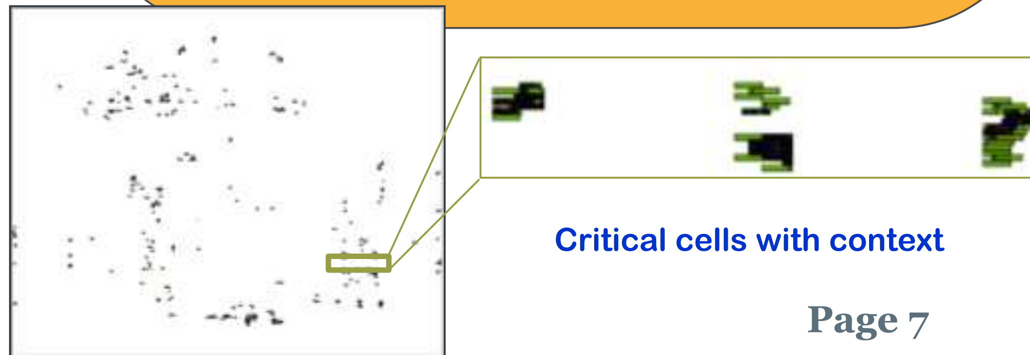
- LEA path variability flow:
  - Create data from Encounter
  - Extracts critical cells with context
  - Launch LVS to extract stress effects due to contexts on critical cells
  - Compute delay difference and back-annotate timing
- LEA path variability flow is used:
  - To run analysis on critical paths, Clock Trees, etc
  - To provide more accurate timing analysis and reduce margins
  - In Standalone mode or from Encounter





Critical cells with context

4. Results : Vth variability, 40 nm

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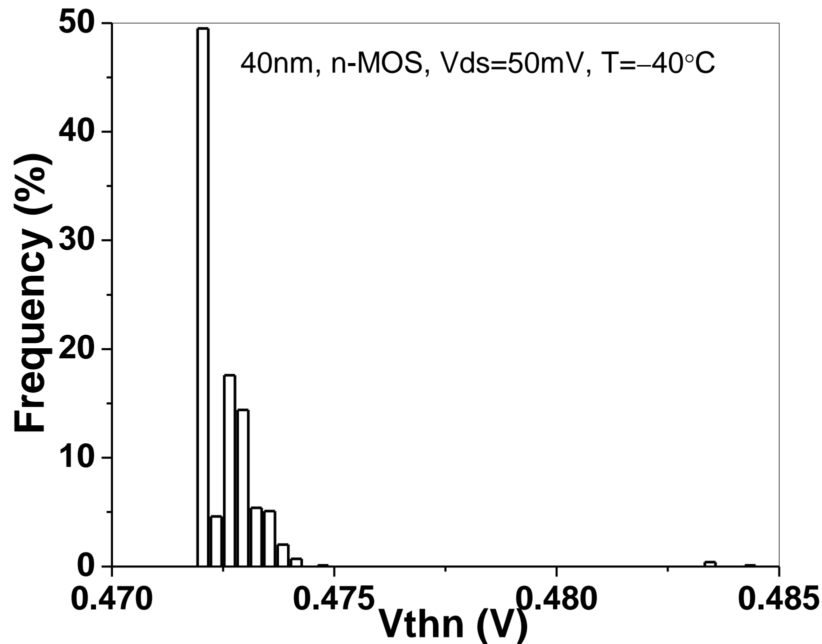
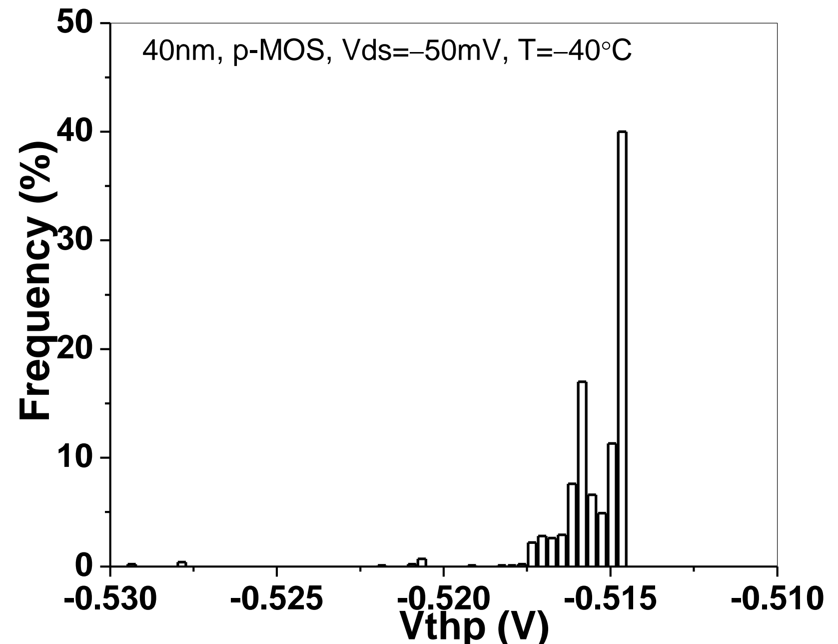
Small logic cell: Inverter consists of 1 n-MOS and 1 p-MOS
1000 random contexts,
Top and Bottom: Regular Layout (Filler Cells),
Left and Right: Random cells from the library.





Vth	Spread (mV)	Relative Variation (%)
NMOS	13.4	2.84
PMOS	14.8	2.88

4. Results: Idsatn, Ioffn variability, 40 nm

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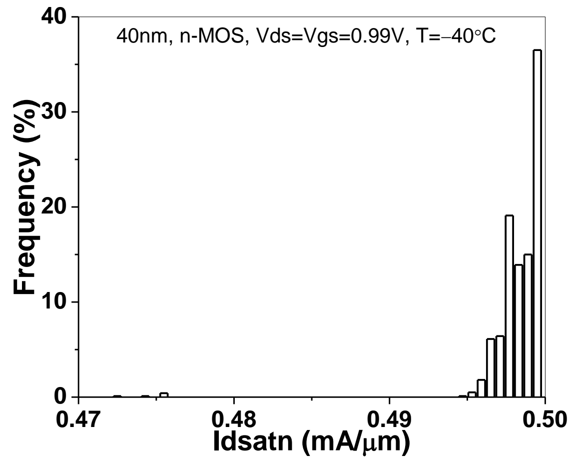

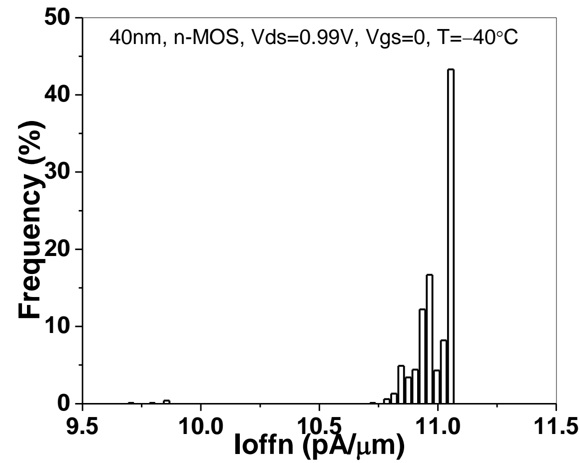

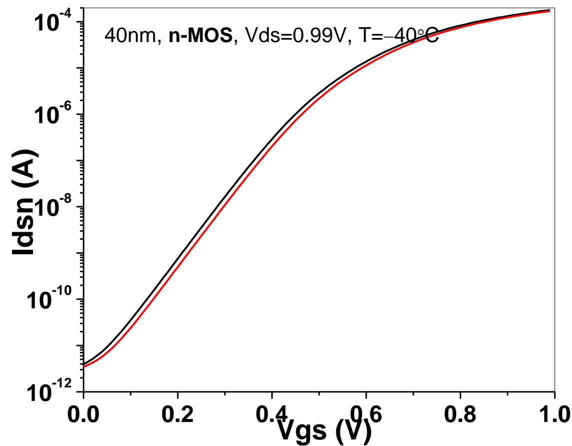

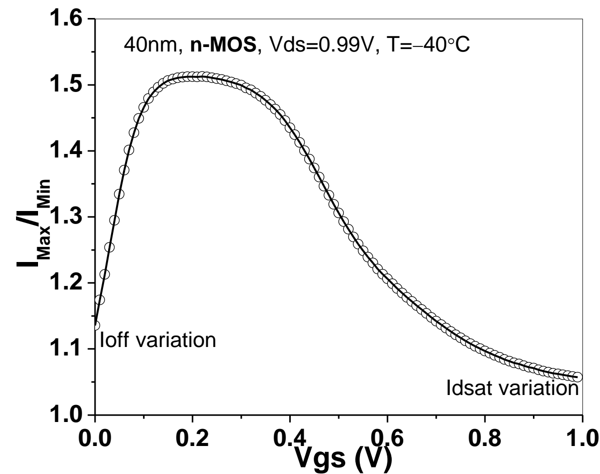

NMOS	Spread	Relative Variation (%)
Idsat	0.0268 (mA/μm)	5.7
Ioff	1.35 (pA/μm)	13.9

4. Results: Idsatp, Ioffp variability, 40 nm

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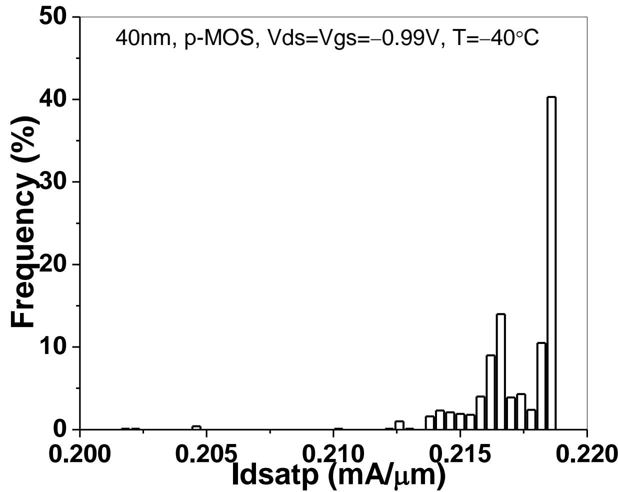

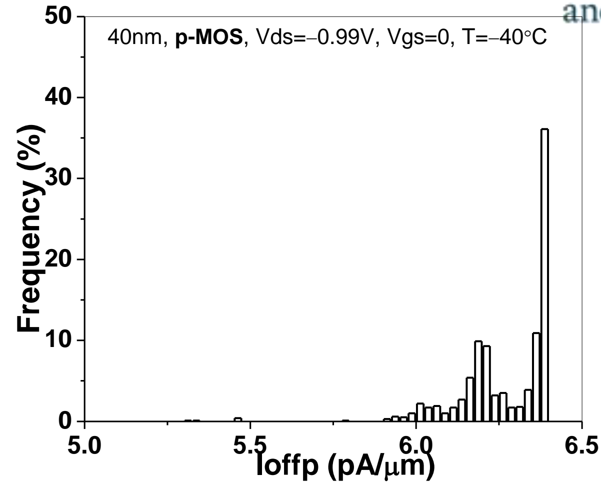

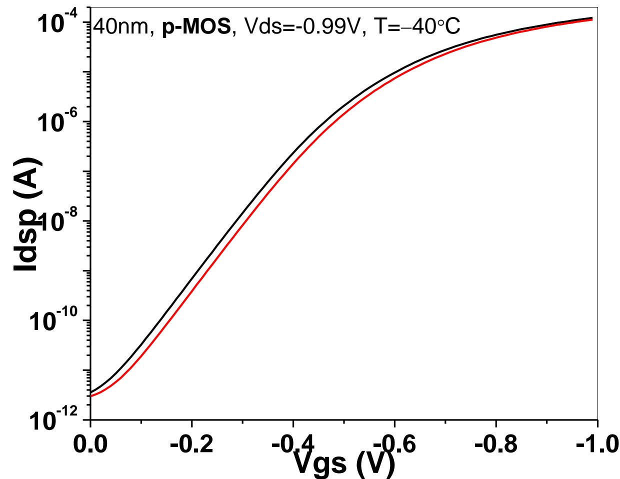

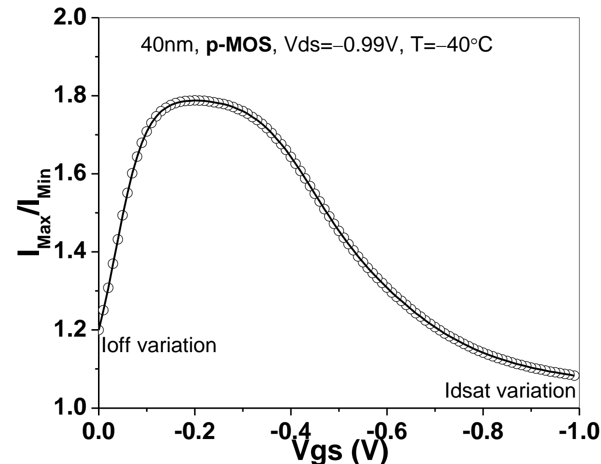

PMOS	Spread	Relative Variation (%)
Idsat	0.0168 (mA/µm)	8.3
Ioff	1.06 (pA/µm)	20.0

4. Results: Cell variability, 40 nm

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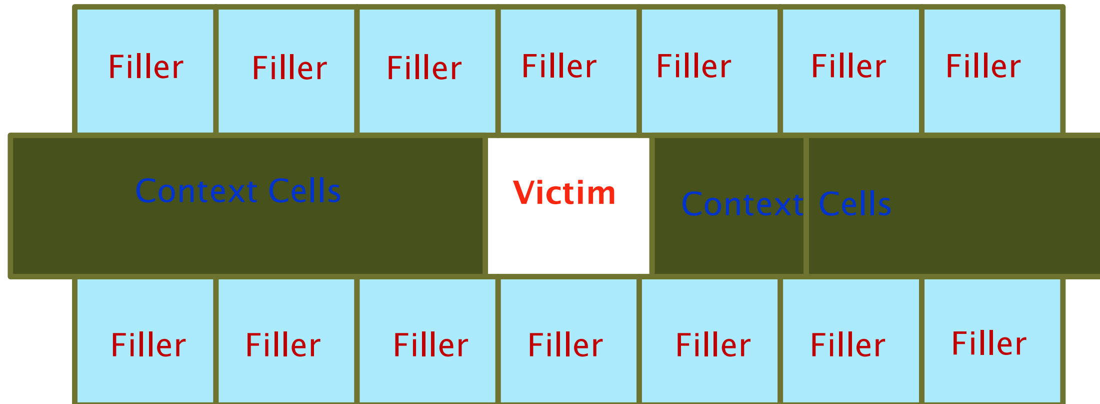

Context configuration

CELLS	Drive Strength	Max delay spread (%)	CELLS	Drive Strength	Max Output slew spread (%)	CELLS	Drive Strength	Max Leakage spread (%)
Inverter	2	15.39	Buffer	1	13.53	Inverter	1	30.48
Inverter	1	11.74	Inverter	2	13.25	Inverter	2	28.25
Inverter	0.5	10.90	Inverter	1	12.79	Inverter	0.5	26.83
Inverter	4	10.49	Buffer	0.5	12.57	Buffer	1	24.19
Buffer	1	9.86	Buffer	2	10.56	Inverter	4	22.16
Buffer	8	4.75	Inverter	32	6.70	Buffer	6	12.97
Buffer	20	4.40	Inverter	20	6.62	Buffer	12	12.96
Buffer	16	3.65	Buffer	8	6.20	Buffer	8	11.60
Buffer	24	3.18	Inverter	16	5.88	Buffer	32	11.28
Buffer	32	2.97	Inverter	24	5.54	Buffer	24	10.41

Worst and best 5 clock tree cells variability from 40 nm cell library

4. Discussion: Cell variability, 40 nm

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Smaller cells demonstrate higher variability and bigger cells have lower variability as shown in the above table.

Cell variability is affected mostly by:

1. Devices at the border of the cell because they have higher variability.

2. The proportion (Percentage) of devices along the cell border affects the whole variability.

3. The left and right context cells (WPE and OSE at lateral effects).

4. And top and bottom contexts cells have negligible effects because of the Dummy diffusions (smaller OSE Vertical effects).

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5. 28nm devices

- **28nm MOSFETs variability due to stress.**
  - Vth and Idsat Variability of n-MOS increase with technology scaling.
  - Ioff variability is much smaller.
  - Variability of p-MOS is about half of 40nm devices, which may be because of DSL and SiGe technologies.
  - Up to 4% of timing and 0.2% of leakage variability of cells' are found.
  - The 28nm technology is better than 40nm according to context dependent variability.

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5. Results of 28nm devices – Cell variability

CELLS	Drive Strength	Max delay spread (%)	CELLS	Drive Strength	Max Output slew spread (%)	CELLS	Drive Strength	Max Leakage spread (%)
Inverter	20	1.6103	Inverter	24	3.7275	Inverter	1	0.1631
Inverter	24	1.4437	Buffer	1	3.5992	Inverter	0	0.1631
Inverter	3	1.2694	Buffer	2	3.4314	Inverter	2	0.1321
Buffer	4	1.1821	Buffer	8	3.2862	Inverter	3	0.1296
Inverter	2	1.1562	Buffer	4	3.1377	Buffer	2	0.1037
Inverter	8	0.728	Inverter	20	1.2376	Buffer	16	0.0128
Inverter	12	0.69	Inverter	16	1.2306	Buffer	20	0.0103
Buffer	32	0.653	Buffer	6	1.2293	Inverter	32	0.0095
Buffer	24	0.528	Inverter	12	1.1215	Buffer	24	0.0086
Inverter	16	0.091	Inverter	32	1.0738	Buffer	32	0.0063

Worst and best 5 clock tree cells' timing and leakage variations from 28 nm cell library

Cell variability at 28nm technology is smaller than that of 40nm's.

6. Possible Mitigation Strategies

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1. Effects of diffusion spacing (OSE)

✓ We found that the context dependent systematic variability does not become worse by removing the dummy diffusion.

Strategy 1: Remove top and bottom dummy diffusions in future generations.

I_{DSAT}	Dummy OD	Min (mA/µm)	Max (mA/µm)	Variation (%)
NMOS	With	0.48520	0.51371	5.88
	W/O	0.47707	0.50599	6.06
PMOS	With	0.20345	0.22089	8.57
	W/O	0.20663	0.22479	8.79

✓ Bigger vertical diffusion spacing is good for p-MOS current, bigger spacing is suggested to trade-off n and p-MOS current.

Strategy 2: Making the top context cells a little farther from the victim.

✓ Device performance benefits from smaller horizontal diffusion spacing:

Strategy 3: Making the left and right context cells closer to the victim.

6. Possible Mitigation Strategies (Cont.)

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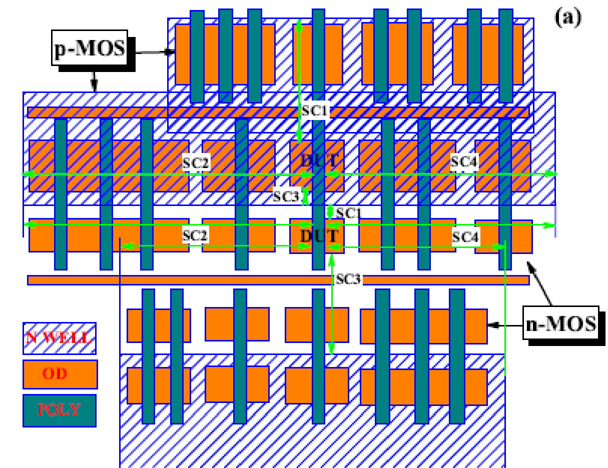
2. Effects of Well Proximity (WPE)

✓ The smaller distance from gate to well edges, the higher WPE.

Strategy 4: Try to place bigger cells at the left and right of the victim.



Schematic diagram of physical distances between gate to well edges

3. Effects of Poly Spacing (PSE)

✓ Stress Variability is not obviously affected by removing dummy polys.

I_{DSAT}	Dummy Poly	Min (mA/µm)	Max (mA/µm)	Variation (%)
NMOS	With	0.48520	0.51371	5.88
	W/O	0.487635	0.516094	5.84
PMOS	With	0.20345	0.22089	8.57
	W/O	0.20417	0.22154	8.51

7. Conclusions

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1. Context dependent stress effects (Oxide Spacing, Well Proximity Effects) are significant for nano devices and cell variability.
2. LEA is used for device, cell, circuit variability analysis due to stress.
3. 40nm MOSFET variability due to stress are reported.
4. Cell variability of 40nm due to stress are affecting SOC designs.
5. Mitigation strategies to reduce context dependent variability.
6. 28nm MOSFETs variability due to stress.
7. Maximum context dependent variability at 40 and 28nm technologies.

Process	Vth	Idsat	Ioff	Delay/Slew	Leakage
40nm	2.88%	8.3%	20.0%	15.39%	30.48%
28nm	3.91%	11.5%	2.18%	3.73%	0.163%

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