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Title

TSMC 65 NM/ 55 NM CMOS LOGIC/MS_RF DESIGN RULE (CLN65 G/GP/LP/LPG/ULP, CLN55 GP/LP, CMN65 GP/LP, CMN55LP)

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Title

TSMC 65 NM/ 55 NM CMOS LOGIC/MS_RF DESIGN RULE (CLN65 G/GP/LP/LPG/ULP, CLN55 GP/LP, CMN65 GP/LP, CMN55LP)

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TSMC 65 NM/ 55 NM CMOS LOGIC/MS_RF DESIGN RULE (CLN65 G/GP/LP/LPG/ULP, CLN55 GP/LP, CMN65 GP/LP, CMN55LP)

Table of Contents

1 INTRODUCTION 11

1.1 OVERVIEW 11
1.2 REFERENCE DOCUMENT 12

2 TECHNOLOGY OVERVIEW 16

2.1 SEMICONDUCTOR PROCESS 16
2.1.1 Front-End Features 16
2.1.2 Back-End Features 17
2.2 DEVICES 19
2.3 POWER SUPPLY AND OPERATION TEMPERATURE RANGES 20
2.4 CROSS-SECTION 22
2.5 METALLIZATION OPTIONS 27

3 GENERAL LAYOUT INFORMATION 36

3.1 MASK INFORMATION, KEY PROCESS SEQUENCE, AND CAD LAYERS 36
3.2 METAL/VIA CAD LAYER INFORMATION FOR METALLIZATION OPTIONS 64
3.3 DUMMY PATTERN FILL CAD LAYERS 65
3.4 SPECIAL RECOGNITION CAD LAYER SUMMARY 66
3.5 DEVICE TRUTH TABLES 70
3.5.1 CLN65 General Purpose (G): 71
3.5.2 CLN65 General Purpose Plus (GP): 73
3.5.3 CLN65 Low Power (LP): 75
3.5.4 CLN65 LP-based Triple Gate Oxide (LPG) Design 77
3.5.5 CLN65 Ultar Low Power (ULP) Design 79
3.5.6 CLN55 General Purpose Plus (GP): 80
3.5.7 CLN55 Low Power (LP): 82
3.5.8 CMN65 MIM 83
3.5.9 CLN65/CLN55/CMN65/CMN55 MOM 83
3.5.10 CMN65/CMN55 Inductor 84
3.5.11 CMN65 LP High Current Diode (HIA_DIO): 85
3.6 MASK REQUIREMENTS FOR DEVICE OPTIONS (HIGH/STD/LOW VT) 86
3.7 DESIGN GEOMETRY RESTRICTIONS 88
3.7.1 Design Geometry Rules 88
3.7.2 OPC Recommendations and Guidelines 89
3.8 DESIGN HIERARCHY GUIDELINES 91
3.9 CHIP IMPLEMENTATION AND TAPE OUT CHECKLIST 92

4 LAYOUT RULES AND RECOMMENDATIONS 93

4.1 LAYOUT RULE CONVENTIONS 93
4.2 SPECIAL GEOMETRIES USED IN PHYSICAL DESIGN RULES 94
4.2.1 Derived Geometries 94
4.2.2 Special Definition 95
4.3 DEFINITION OF LAYOUT GEOMETRICAL TERMINOLOGY 96
4.4 MINIMUM PITCHES 101

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4.5 CLN65(LOGIC) LAYOUT RULES AND GUIDELINES....102
4.5.1 Deep N-Well (DNW) Layout Rules (Mask ID: 119) [Optional]....102
4.5.2 Gate Oxide and Diffusion (OD) Layout Rules (Mask ID: 120)....104
4.5.3 N-Well (NW) Layout Rules....106
4.5.4 N-Well Resistor Within OD (NWROD) Layout Rules....108
4.5.5 N-Well Resistor Under STI (NWRSTI) Layout Rules....110
4.5.6 Native Device (NT_N) Layout Rules....111
4.5.7 Thick Oxide (OD2) Layout Rules (Mask ID: 152)....113
4.5.8 Dual Core Oxide (DCO) Rules Layout Rules (MASK ID:153)....115
4.5.9 OD25_33 Layout Rules....117
4.5.10 OD25_18 Layout Rules....118
4.5.11 Poly (PO) Layout Rules (Mask ID: 130)....119
4.5.12 High Vt NMOS (VTH_N) Layout Rules (Mask ID: 128)....126
4.5.13 High Vt PMOS (VTH_P) Layout Rules (Mask ID: 127)....127
4.5.14 Low Vt NMOS (VTL_N) Layout Rules (Mask ID: 118)....128
4.5.15 Low Vt PMOS (VTL_P) Layout Rules (Mask ID: 117)....129
4.5.16 m-Low Vt (mVTL) Layout Rules....130
4.5.17 N65 HVD_N Layout Rules....131
4.5.18 N65 HVD_P Layout Rules....134
4.5.19 N65 5V HVMOS Layout Rules and Guidelines....137
4.5.20 P+ Source/Drain Ion Implantation (PP) Layout Rules (Mask ID: 197)....142
4.5.21 N+ Source/Drain Ion Implantation (NP) Rules (Mask ID: 198)....144
4.5.22 Layout Rules for LDD Mask Logical Operations....146
4.5.23 Resist Protection Oxide (RPO) Layout Rules (Mask ID: 155)....148
4.5.24 OD and Poly Resistor Recommendations and Guidelines....149
4.5.25 MOS Varactor Layout Rules (VAR)....152
4.5.26 Contact (CO) Layout Rules (Mask ID: 156)....154
4.5.27 Metal-1 (M1) Layout Rules (Mask ID: 360)....158
4.5.28 VIAx Layout Rules (Mask ID: 378, 378, 373, 374, 375, 376)....162
4.5.29 Mx Layout Rules (Mask ID:380, 381, 384, 385, 386, 387)....168
4.5.30 VIAy Layout Rules (Mask ID: 379, 373, 374, 375, 376, 377, 372)....172
4.5.31 My Layout Rules (Mask ID: 381, 384, 385, 386, 387, 388, 389)....176
4.5.32 Top VIAz Layout Rules (Mask ID: 379, 373, 374, 375, 376, 377, 372)....180
4.5.33 Top Mz Layout Rules (Mask ID: 381, 384, 385, 386, 387, 388, 389)....184
4.5.34 Top VIAr Layout Rules (Mask ID: 375, 356, 377, 372)....186
4.5.35 Top Mr Layout Rules (Mask ID:386, 387, 388, 389)....190
4.5.36 MOM Layout Rules....192
4.5.37 Via Layout Recommendations....198
4.5.38 Product Labels and Logo Rules....199
4.5.39 SRAM Rules....200
4.5.40 SRAM Periphery (Word Line Decoder) Rules....203
4.5.41 Fuse Rules....204
4.5.42 Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns....204
4.5.43 Chip Corner Stress Relief Pattern (CSR)....210
4.5.44 Seal Ring Layout Rules....215
4.5.45 Sealring CDU (Critical Dimension Uniformity) Rules....223
4.5.46 Antenna Effect Prevention (A) Layout Rules....224
4.6 CMN65 (MIXED SIGNAL, RF) LAYOUT RULES AND GUIDELINES....228
4.6.1 Capacitor Top Metal (CTM) Layout Rules (Mask ID: 182)....228
4.6.2 Capacitor Bottom Metal (CBM) Layout Rules (Mask ID: 183)....229
4.6.3 MIM Capacitor PDK Guidelines....231
4.6.4 VIAz and VIAu Layout Rule for MIM Capacitor and Mu....233
4.6.5 Mz Layout Rule (Mask ID: 384, 385, 386, 387, 388, 389) for MIM Capacitor....234
4.6.6 Antenna Effect Prevention Design Rules for MIM Capacitor....235
4.6.7 Ultra Thick Metal (Mu) Layout Rules (Mask ID: 384, 385, 386, 387, 388, 389)....241
4.6.8 INDDMY Rule Overview....242
4.6.9 Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns....254
4.6.10 Seal-Ring Rule....254
4.7 RV LAYOUT RULES (CB VIA HOLE)....259
4.7.1 RV Layout Rules (CB VIA hole) for Wire Bond....259
4.7.2 RV Layout Rules (Passivation-1 VIA Hole) for Flip Chip....260

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4.8 AP-MD LAYOUT RULES 261
4.8.1 AP-MD Layout Rules for Wire Bond 261
4.8.2 AP-MD Layout Rules for Flip Chip 262

5 WIRE BOND, FLIP CHIP AND INTERCONNECTION DESIGN RULES 263

6 N55 DESIGN INFORMATION 264

6.1 OVERVIEW 264
6.1.1 General Logic Design Specifications 264
6.1.2 SRAM Design Specifications 265
6.2 NON-SHRINKABLE LAYOUT RULES 265
6.2.1 Purpose: 265
6.2.2 Stress Migration and Wide Metal Spacing Rules Adjustment 266
6.2.3 SRAM Rules 268
6.2.4 Pad Rule for Wire Bond 268
6.2.5 Flip Chip Bump Rules 268
6.2.6 AP Metal Fuse Rules 269
6.3 ANTENNA EFFECT PREVENTION LAYOUT RULES 270
6.4 LAYOUT GUIDELINE FOR LATCH-UP AND I/O ESD 270
6.5 DESIGN FLOW FOR TAPE-OUT 270
6.5.1 How to shrink the existing N65 design 270
6.5.2 How to prepare a new design of N55 272
6.5.3 110% size-up 273
6.5.4 Layout check and post simulation 275

7 LAYOUT RULES AND RECOMMENDATION FOR ANALOG CIRCUITS 279

7.1 USER GUIDES 279
7.2 LAYOUT RULES FOR THE WPE (WELL PROXIMITY EFFECT) 280
7.3 LAYOUT GUIDELINES FOR LOD (LENGTH OF THE OD REGION) EFFECT 282
7.3.1 What is LOD? 282
7.3.2 Id change due to different SA 282
7.3.3 How to have a precise LOD Simulation 283
7.4 LAYOUT RULES, RECOMMENDATIONS AND GUIDELNIES FOR THE ANALOG DESIGNS 284
7.4.1 General Guidelines 284
7.4.2 MOS Recommendations and Guidelines 284
7.4.3 Parasitic Bipolar Transist or (BJT) Rules and Recommendations 285
7.4.4 Resistor Rules and Recommendations 287
7.4.5 Capacitor Guidelines 288
7.5 LAYOUT RULES AND GUIDELINES FOR DEVICE PLACEMENT 289
7.5.1 General Rules and Guidelines 289
7.5.2 Matching Rules and Guidelines 290
7.5.3 Electrical Performance Rules and Guidelines 292
7.5.4 Noise 295
7.6 BURN-IN GUIDELINES FOR ANALOG CIRCUITS 299

8 DUMMY PATTERN RULE AND FILLING GUIDELINE 300

8.1 DUMMY OD (DOD) RULES 300
8.2 DUMMY POLY (DPO) RULES 303
8.3 DUMMY TCD RULES AND FILLING GUIDELINES 306
8.3.1 Dummy TCD Rules (DTCD) 306
8.3.2 Dummy TCD layout Summary 307
8.4 DUMMY METAL (DM) RULES 308
8.5 DUMMY PATTERN FILL USAGE SUMMARY 312
8.5.1 Dummy Pattern Filling Requirements 312
8.5.2 Recommended Flow for Dummy Pattern Filling 313
8.5.3 Blockage Layer (ODBLK/POBLK/DMxEXCL) Requirements and Recommendations 314
8.5.4 Dummy Pattern Filling Guidelines 315
8.5.5 Mask Revision Guidelines 316
8.5.6 Dummy Pattern Re-fill Evaluation Flow Chart 317

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9 DESIGN FOR MANUFACTURING (DFM) 320

9.1 LAYOUT GUIDELINES FOR YIELD ENHANCEMENT 320
9.1.1 Layout Tips for Minimizing Critical Areas 320
9.1.2 Guidelines for Optimal Electrical Model and Silicon Correlation 322
9.1.3 Electrical Wiring 327
9.1.4 Guidelines for Mask Making Efficiency 327
9.2 DFM RECOMMENDATIONS AND GUIDELINES SUMMARY 328
9.2.1 Action-Required Rules 328
9.2.2 Recommendations 329
9.2.3 Guidelines 332
9.2.4 Grouping Table of DFM Action-Required Rules, Recommendations and Guidelines 334
9.3 GDA DIE SIZE OPTIMIZATION KIT 336
9.3.1 What is MFU? 336
9.3.2 Recommended GDA criteria MFU>80% 336

10 LAYOUT GUIDELINES FOR LATCH-UP AND I/O ESD 337

10.1 LAYOUT RULES AND GUIDELINES FOR LATCH-UP PREVENTION 337
10.1.1 Latch-up Introduction 337
10.1.2 Layout Rules and Guidelines for Latch-up Prevention 341
10.1.3 Test Specification and Requirements 353
10.2 I/O ESD PROTECTION CIRCUIT DESIGN AND LAYOUT GUIDELINES 354
10.2.1 ESD introduction 354
10.2.2 TSMC IO ESD layout style introduction 356
10.2.3 ESD Implant (ESDIMP) Layout Rules (MASK ID: 111) 358
10.2.4 ESD Dummy Layers Summary 359
10.2.5 ESD circuits Definition 360
10.2.6 Requirements for ESD Implant Masks 361
10.2.7 DRC methodology for ESD guidelines 361
10.2.8 ESD Guidelines 366
10.2.9 CDM Protection for Cross Domain Interface 382
10.2.10 High Current Diode (HIA_DIO) 383
10.2.11 Tips for the ESD/LU Design 387
10.2.12 Tips for the Power ESD Protection 388
10.2.13 ESD test methodology 388

11 RELIABILITY RULES 389

11.1 TERMINOLOGY 389
11.2 FRONT-END PROCESS RELIABILITY RULES AND MODELS 389
11.2.1 Guidelines for I/O Over Drive Voltage 389
11.2.2 Guidelines for Gate Oxide Integrity 389
11.2.3 Guideines for Hot Carrier Injection Effect 392
11.2.4 Guidelines for Negative Bias Temperature Instability (NBTI) 394
11.3 BACK-END PROCESS RELIABILITY RULES 397
11.3.1 Guidelines for Stress Migration(SM) 397
11.3.2 Guidelines for Low-k Dielectric Integrity 397
11.3.3 DC Cu Metal Current Density (EM) Specifications 399
11.3.4 Cu Metal AC Operation 406
11.3.5 AP RDL Current Density (EM) Specification 417
11.3.6 N65/N55 AP RDL AC Operation 418
11.3.7 Poly Current Density Specifications 418
11.3.8 N65 Poly EM Joule heating Guidelines 419
11.3.9 OD Current Density Specifications 419
11.4 PRODUCT EARLY FAILURE RATE SCREENING GUIDELINES 420
11.4.1 Wafer Level Screening 420
11.4.2 Package-Level Screening – Product Burn-In 421
11.4.3 Soft Error Rate 421
11.5 E-RELIABILITY MODEL SYSTEM INTRODUCTION 430
11.5.1 What is the e-Reliability Model System? 430
11.5.2 Why the e-Reliability Model System? 430
11.5.3 Where to access the e-Reliability Model System? 430

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12 ELECTRICAL PARAMETERS SUMMARY 431

12.1 AVAILABLE MOS TRANSISTORS 432
12.1.1 CLN65LP (1.2V) 432
12.1.2 CLN65LPHV (2.5V) 432
12.1.3 CLN65G (1.0V) 432
12.1.4 CLN65GP (1.0V_2.5V) 433
12.1.5 CLN65LPG (LP:1.2V, G:1.0V) 433
12.1.6 CLN65ULP (1.0V) 434
12.1.7 CLN55GP (1.0V_2.5V) 434
12.1.8 CLN55LP (1.2V) 435
12.2 KEY PARAMETERS OF MOS TRANSISTORS IN CLN65LP & CLN65LPHV 436
12.2.1 1.2V Standard Vt MOS 436
12.2.2 1.2V High V_t MOS 437
12.2.3 1.2V mLow MOS 438
12.2.4 1.2V Low V_t MOS 439
12.2.5 1.8V I/O MOS (2.5V underdrive to 1.8V) 440
12.2.6 2.5V I/O MOS 441
12.2.7 3.3V I/O MOS (2.5V overdrive to 3.3V) 442
12.2.8 3.3V I/O MOS 443
12.2.9 1.2V Native MOS 444
12.2.10 2.5V Native I/O MOS 445
12.2.11 2.5V Native Over-drive 3.3V I/O MOS 446
12.2.12 2.5/5.5V High Voltage MOS 447
12.2.13 2.50V MOS 448
12.3 KEY PARAMETERS OF MOS TRANSISTORS IN CLN65G 449
12.3.1 1.0V Standard Vt MOS 449
12.3.2 1.0V High Vt MOS 450
12.3.3 1.8V I/O MOS 451
12.3.4 2.5V I/O MOS 452
12.3.5 1.0V Native MOS 453
12.3.6 1.8V Native MOS 454
12.3.7 2.5V Native MOS 455
12.4 KEY PARAMETERS OF MOS TRANSISTORS IN CLN65GP 456
12.4.1 1.0V Standard Vt MOS 456
12.4.2 1.0V High Vt MOS 457
12.4.3 1.0V Low Vt MOS 458
12.4.4 1.8V I/O MOS 459
12.4.5 2.5V I/O MOS 460
12.4.6 1.8V I/O MOS (2.5V underdrive to 1.8V) 461
12.4.7 3.3V I/O MOS (2.5V overdrive to 3.3V) 462
12.4.8 1.0V Native MOS 463
12.4.9 1.8V Native I/O MOS 464
12.4.10 2.5V Native I/O MOS 465
12.4.11 3.3V Native I/O MOS 466
12.5 KEY PARAMETERS OF MOS TRANSISTORS IN CLN65LPG 467
12.5.1 1.0V LPG/G Standard Vt MOS 467
12.5.2 1.0V LPG/G High Vt MOS 468
12.5.3 2.5V IO MOS 469
12.5.4 1.8V I/O MOS (2.5V underdrive to 1.8V) 470
12.5.5 3.3V I/O MOS (2.5V overdrive to 3.3V) 471
12.5.6 1.0V LPG/G Native MOS 472
12.5.7 2.5V Native MOS 473

TSMC Confidential Information 833462 USCVISIVMOSIS 12/16/2016

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12.6 KEY PARAMETERS OF MOS TRANSISTORS IN CLN65ULP 474
12.6.1 1.0V Standard Vt MOS 474
12.6.2 1.0V High V_t MOS 475
12.6.3 1.0V mLow MOS 476
12.6.4 1.0V Low V_t MOS 477
12.6.5 1.8V I/O MOS 478
12.6.6 2.5V I/O MOS 479
12.6.7 3.3V I/O MOS 480
12.6.8 1.0V Native MOS 481
12.6.9 2.5V Native I/O MOS 482
12.6.10 2.5V Native Over-drive 3.3V I/O MOS 483
12.6.11 2.5/5.5V High Voltage MOS 484
12.7 KEY PARAMETERS OF MOS TRANSISTORS IN CLN55GP 485
12.7.1 1.0V Standard Vt MOS 485
12.7.2 1.0V High Vt MOS 486
12.7.3 1.0V Low Vt MOS 487
12.7.4 1.0V Ultra High Vt MOS 488
12.7.5 1.8V I/O MOS 489
12.7.6 2.5V I/O MOS 490
12.7.7 3.3V I/O MOS (2.5V Overdrive to 3.3V) 491
12.7.8 1.0V Native MOS 492
12.7.9 1.8V Native MOS 493
12.7.10 2.5V Native MOS 494
12.7.11 3.3V Native MOS 495
12.7.12 2.5V Over-drive 3.3V Native MOS 495
12.8 KEY PARAMETERS OF MOS TRANSISTORS IN CLN55LP 496
12.8.1 1.2V Standard Vt MOS 496
12.8.2 1.2V High V_t MOS 497
12.8.3 1.2V Low V_t MOS 498
12.8.4 1.8V I/O MOS 499
12.8.5 2.5V I/O MOS 500
12.8.6 3.3V I/O MOS 501
12.8.7 2.5V under drive 1.8V I/O MOS 502
12.8.8 2.5V over drive 3.3V I/O MOS 503
12.8.9 1.2V Native MOS 504
12.8.10 2.5V Native I/O MOS 505
12.8.11 2.5V Native Over-drive 3.3V I/O MOS 506
12.9 KEY PARAMETERS FOR BIPOLAR 507
12.9.1 CLN65LP 507
12.9.2 CLN65G 508
12.9.3 CLN65GP 508
12.9.4 CLN65LPG 509
12.9.5 CLN65ULP 510
12.9.6 CLN55GP 511
12.9.7 CLN55LP 511
12.10 KEY PARAMETERS FOR JUNCTION DIODES 512
12.10.1 CLN65LP 512
12.10.2 CLN65G 513
12.10.3 CLN65GP 514
12.10.4 CLN65LPG 515
12.10.5 CLN65ULP 516
12.10.6 CLN55GP 517
12.10.7 CLN55LP 518
12.11 RESISTOR MODELS 519
12.11.1 CLN65LP 520
12.11.2 CLN65G (M1MxMz process, no My/Mr, x=2~7, z=8~9) 522
12.11.3 CLN65GP (M1MxMz process, no My/Mr, x=2~7, z=8~9) 524
12.11.4 CLN65LPG (M1MxMz process, no My/Mr, x=2~7, z=8~9) 526
12.11.5 CLN65ULP 528
12.11.6 CLN55GP (M1MxMz process, no My/Mr, x=2~7, z=8~9) 530
12.11.7 CLN55LP (M1MxMz process, no MyMr, x=2~7, z=8~9) 532

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12.12 UNSILICIDED N+/P+ POLY RESISTORS MODELS 534
12.12.1 Resistor Model Equations 535
12.13 UNSILICIDED N+/P+ DIFFUSION RESISTORS MODELS 540
12.14 INTERCONNECT MODEL 545
12.14.1 Conductor Layers 545
12.14.2 Dielectric Layers 547
12.14.3 Interconnect line-to-line capacitance 551
12.15 MIM CAPACITOR MODEL 592
12.15.1 Model Usage Guide 592
12.15.2 Test Structure and Measurement Procedures 592
12.15.3 Equivalent Circuit Model 593
12.15.4 Model Details 594
12.15.5 Corner Model Table 599
12.15.6 Temperature Effect Model 600
12.15.7 TCC and VCC 602
12.15.8 Mismatch Model 603
12.15.9 Statistical Model 603
12.16 MOM CAPACITOR MODEL 604
12.16.1 RF Model Usage Guide 604
12.16.2 RF Test Structure and Measurement Procedures 604
12.16.3 RF Equivalent Circuit Model 605
12.16.4 RF Model Details 606
12.16.5 RF Corner Model Table 609
12.16.6 RF Temperature Effect Model 609
12.17 INDUCTOR MODEL 610
12.17.1 Model Usage Guide 610
12.17.2 Test Structure and Measurement Procedures 611
12.17.3 Equivalent Circuit Model 611
12.17.4 Model Details 613
12.17.5 Corner Model Table 620
12.17.6 Temperature Effect Model 620
12.17.7 Variable Metal Layer Model 621
12.17.8 Statistical Model 621
12.18 RF I/O PAD MODEL 622
12.18.1 Model Usage Guide 622
12.18.2 Test Structure and Measurement Procedure 622
12.18.3 Equivalent Circuit and Model Scaling Rule 623
12.18.4 Modeled Capacitance and Model Error Table 623

APPENDIX A REVISION HISTORY 624

A.1 T-N65-CL-DR-001 (LOGIC) 624
A.1.1 From Version 0.1 to Version 0.2 624
A.1.2 From Version 0.2 to Version 0.3 626
A.1.3 From Version 0.3 to Version 1.0 627
A.1.4 From Version 1.0 to Version 1.1 628
A.1.5 From Version 1.1 to Version 1.2 632
A.1.6 From Version 1.2 to Version 1.3 633
A.1.7 From Version 1.3 to Version 1.4 638
A.1.8 From Version 1.4 to Version 1.4_1 642
A.1.9 From Version 1.4_1 to Version 2.0 643
A.1.10 From Version 2.0 to Version 2.1 648
A.1.11 From Version 2.1 to Version 2.2 655
A.1.12 From Version 2.2 to Version 2.3 657
A.2 REVISION HISTORY OF T-N65-CM-DR-001 (MS_RF) 658
A.2.1 New (Version 0.1): only for Mu and MIM 658
A.2.2 From Version 0.1 to Version 0.2 658
A.2.3 From Version 0.2 to Version 1.0 659
A.2.4 Rule Mapping from MS_RF Rule to Logic Rule 662
A.3 REVISION HISTORY OF T-N55-CL-DR-001 (N55 LOGIC) 663
A.3.1 From Version 0.1 to Version 0.2 663
A.3.2 From Version 0.2 to Version 1.0 664

TSMC Confidential Information 833462 USCVISIVMOSIS 12/16/2016

A.4 REVISION HISTORY OF T-000-CL-DR-002 (PAD) 665
A.4.1 Change from Each Document to Version 1.0 ..... *665*
A.4.2 Change from Version 1.0 to 1.1 ..... *667*
A.4.3 Change from Version 1.1 to 1.2 ..... *668*
A.4.4 Change from Version 1.2 to 1.3 ..... *670*
A.4.5 Change from Version 1.3 to 1.4 ..... *673*
A.5 REVISION HISTORY OF T-N65-CL-DR-029 (5V HV CMOS) 674
A.5.1 Change from Version 0.1 to 1.0 ..... *674*

TSMC Confidential Information
833462
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12/16/2016

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1 Introduction

This chapter has been divided into the following topics:

1.1 Overview
1.2 Reference documentation

1.1 Overview

This document provides all the rules and reference information for the design and layout of integration circuits using the TSMC 65 nm and 55nm CMOS LOGIC/MS_RF 1P9M (single poly, 9 metal layers), salicide, Cu technology.

- ***CLN65G*** is a general-purpose product for applications with a 1.0V core design, and with 1.8V or 2.5V capable I/O's.
- ***CLN65GP*** provides lower leakage or higher performance transistors for multiple applications with core 1.0V voltage and 1.8V or 2.5V IO options.
- ***CLN65LP*** is a low-power product for applications with a 1.2V core design, and with 2.5V or 3.3V capable I/O's, and 5V HVMOS fabricated with 2.5V IO gate oxide.
- ***CLN65LPG*** provides both low active power and low standby power applications with 1.0V (G) and 1.2V (LP) core design, and with 2.5V capable I/O.
- ***CLN65ULP*** provides lowest power solution for both active power and standby power with similar low cost as 65LP. Core voltage is 1.0V with 2.5V IO.
- ***CLN55GP*** provides CLN65G/GP products with 90% linear shrinkage for the die area saving purpose. CLN55GP offers dual-gate oxide process for 1.0V core and, 1.8V, 2.5V or 3.3V I/O devices. You must complete all GDS and DRC related efforts in N65 level, i.e. follow CLN65 design rules and CLN55 non-shrinkable rules to tape out. TSMC will shrink the GDS to CLN55 while mask making.
- ***CLN55LP*** provides CLN65LP products with 90% linear shrinkage for the die area saving purpose. CLN55LP offers dual-gate oxide process for 1.2V core and 2.5V I/O devices. You must complete all GDS and DRC related efforts in N65 level, i.e. follow CLN65 design rules and CLN55 non-shrinkable rules to tape out. TSMC will shrink the GDS to CLN55 while mask making.
- ***CMN65*** is based on CLN65 process (LP/GP) with extra process steps for mixed signal/RF applications. It includes metal-insulator-metal (MIM) capacitor and ultra thick metal (Mu=UTM; 34KA) for inductor.
  CMN65LP is a low-power product for RF and mixed signal applications with a 1.2V core design, and with 2.5V or 3.3V I/O option, and 5V HVMOS fabricated with 2.5V IO gate oxide.
  CMN65GP provides lower leakage or higher performance transistors for RF and mixed signal applications with core 1.0V voltage and 2.5V IO options.
- ***CMN55LP*** is based on CLN55LP process with extra process steps for mixed signal/ RF application. It includeds metal-oxide-metal (MOM) capacitor and ultra thick metal (Mu=UTM; 34KA) for inductor. CMN55LP is a low-power product for RF and mixed signal applications with a 1.2V core design, and with 2.5V I/O option.

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1.2 Reference Document

Table 1.2.1 Reference Documents

Content	Reference Document
Reference Flow	• *Please download it from TSMC on-line*
Pad rule	• *T-000-CL-DR-017* *TSMC 0.13UM ~ 55NM WIRE BOND, EUTECTIC FLIP CHIP, LEAD FREE (LF) BUMP FLIP CHIP AND INTERCONNECTION DESIGN RULE*
Metal fuse rule	• *T-000-CL-DR-005:* *TSMC AL FUSE (AP FUSE) DESIGN RULE FOR CU PROCESS*
X-metal rule	• *T-N65-CL-DR-009:* *TSMC 65NM X-METAL (XMX) DESIGN RULE*
WCLSP rule	• *T-000-BP-DR-005* *TSMC BUMPING POST PASSIVATION INTERCONNECT DESIGN RULE* • *Q-RAS-02-02-083* *BUMP EM IMAX RULE (FOR TSMC'S BUMP LINE PROCESS ONLY)*
WCLCSP DRC deck	• *T-000-BP-DR-005-X1 (X is the code of EDA tool, please refer to TSMC-Online for the details)* *TSMC BUMPING POST PASSIVATION INTERCONNECT DRC (CALIBRE) COMMAND FILE*
N55 5V HVMOS rules	• *T-N55-CL-DR-006* *TSMC 55 NM 5V HV CMOS DESIGN RULE (CLN55LP/CMN55LP)*
Schottky Barrier Diode rule	• *T-N65-CM-DR-015* *TSMC 65 NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SCHOTTKY BARRIER DIODE (SBD) DESIGN RULE*
P+/PW Varactor design rule	• *T-N65-CM-DR-012* *TSMC 65 NM LOW POWER CMOS 1.2V/2.5V N+/NW AND P+/PW MOS VARACTOR DESIGN RULE (CMN65LP FOR RF)*
GDS layer usage	• *T-N65-CL-LE-001* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE GDS LAYER USAGE DESCRIPTION FILE*
DRC deck	• *T-N65-CL-DR-001-X1 (X is the code of EDA tool, please refer to TSMC-Online for the details)* *TSMC 65NM/55NM CMOS LOGIC/MS_RF DRC COMMAND FILE*
Dummy pattern generation utility	• *T-N65-CL-DR-001-X2 (X is the code of EDA tool, please refer to TSMC-Online for the details)* *TSMC 65NM CMOS LOGIC DUMMY OD/PO GENERATION UTILITY* • *T-N65-CL-DR-001-X3 (X is the code of EDA tool, please refer to TSMC-Online for the details)* *TSMC 65NM CMOS LOGIC DUMMY METAL GENERATION UTILITY*
DFM utility	• *T-N65-CL-DR-001-X4 (X is the code of EDA tool, please refer to TSMC-Online for the details)* *TSMC 65NM CMOS LOGIC DFM LAYOUT ENHANCEMENT UTILITY*
SPICE	• *T-N65-CL-SP-009* *TSMC 65 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2V&2.5V HD BEOL SPICE MODEL (CLN65LP)* • *T-N65-CL-SP-020* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M+AL_RDL SALICIDE CU_LOWK 1.0&2.5V HD BEOL SPICE MODEL* • *T-N65-CL-SP-023* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&1.8V HD BEOL SPICE MODEL* • *T-N65-CL-SP-031* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M+AL_RDL SALICIDE CU_LOWK 1.0&1.8V SPICE MODEL (CLN65G+)* • *T-N65-CL-SP-034* *TSMC 65 NM CMOS LOGIC LP-BASED TRIPLE GATE OXIDE WITH DUAL CORE 1P9M SALICIDE CU_LOWK 1/1.2/2.5V SPICE MODEL* • *T-N65-CL-SP-040* *TSMC 65NM CMOS LOGIC LOW POWER 1P9M+AL_RDL SALICIDE CU_LOWK 1.2V/3.3V SPICE MODELS (CLN65LP)* • *T-N65-CL-SP-041* *TSMC 65 NM LOGIC SALICIDE Low-K IMD (1.0V/2.5V) (CLN65GPLUS)*

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Content	Reference Document
	• *T-N55-CL-SP-007* *TSMC 55 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M+AL_RDL SALICIDE CU_LOWK 1.0&1.8V SPICE MODEL* • *T-N55-CL-SP-010* *TSMC 55 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M+AL_RDL SALICIDE CU_LOWK 1.0/2.5V SPICE MODEL* • *T-N55-CL-SP-013* *TSMC 55 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M+AL_RDL SALICIDE CU_LOWK 1.0&3.3V SPICE MODEL* • *T-N65-CM-SP-002* *TSMC 65 NM CMOS MIXED SIGNAL MS LOW POWER 1P9M+AL_RDL SALICIDE CU_LOWK 1.2&2.5V HD BEOL SPICE MODEL (CMN65LP)* • *T-N65-CM-SP-006* *TSMC 65 NM CMOS MIXED-SIGNAL GENERAL PURPOSE PLUS 1P9M+AL_RDL SALICIDE CU_LOWK 1.0&2.5V SPICE MODEL (CMN65GP)* • *T-N65-CM-SP-007* *TSMC 65 NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SALICIDE CU_LOWK 1.2&2.5V SPICE MODEL* • *T-N65-CM-SP-012* *TSMC 65 NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SALICIDE CU_LOWK 1.2&3.3V SPICE MODEL* • *T-N65-CM-SP-014* *TSMC 65NM CMOS MIXED-SIGNAL LOW POWER 1P9M+AL_RDL SALICIDE CU_LOWK 1.2V/3.3V SPICE MODELS (CMN65LP)* • *T-N65-CL-SP-070* *TSMC 65NM CMOS LOGIC LOW POWER HIGH VOLTAGE 1P9M+AL_RDL SALICIDE CU_LOWK 2.5V SPICE MODEL(PRE RELEASE)* • *T-N65-CM-SP-026-P1* *TSMC 65 NM CMOS MIXED SIGNAL LOW POWER HIGH VOLTAGE 1P9M+AL_RDL SALICIDE CU_LOWK 2.5V SPICE MODEL (PRE RELEASE)* • *T-N55-CM-SP-009-P1* *TSMC 55NM CMOS MIXED SIGNAL LOW POWER 1P9M+AL_RDL SALICIDE CU_LOWK 1.2V/2.5V SPICE MODELS 55LP* • *T-N55-CL-SP-021* *TSMC 55 NM CMOS LOGIC LOW POWER 1P9M+AL_RDL SALICIDE CU_LOWK 1.2&2.5V SPICE MODELS 55LP* • *T-N65-CE-SP-002* *TSMC 65 NM CMOS EMBEDDED DRAM LOW POWER 1P8MT2 (2XTM: M7-M8) SALICIDE CU_LOWK 1.2V&2.5V/ 1.2V&3.3V SPICE MODELS (CLN65LP EDRAM)* • *T-N65-CE-SP-003* *TSMC 65 NM CMOS EMBEDDED DRAM GENERAL PURPOSE PLUS 1P8MT2_Mz(M8_as_CuRDL) SALICIDE CU_LOWK 1.0V&1.8V SPICE MODELS (CLN65G+eDRAM)*
Device formation examples and LVS properties	• *T-N65-CL-LS-001* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE DEVICE FORMATION EXAMPLES AND LVS PROPERTIES*
LVS	• *T-N65-CL-LS-001-X1 (X is the code of EDA tool, please refer to TSMC-Online for the details)* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE DEVICE FORMATION EXAMPLES AND LVS PROPERTIES LVS COMMAND FILE* • *T-N55-CL-LS-001-X1 (X is the code of EDA tool, please refer to TSMC-Online for the details)* *TSMC 55 NM CMOS LOGIC LOW POWER DEVICE FORMATION EXAMPLES AND LVS PROPERTIES LVS COMMAND FILE*
PDK	• *T-N65-CL-SP-031-K1* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M+AL_RDL SALICIDE CU_LOWK 1.0&1.8V PDK (CLN65GP)* • *T-N65-CM-SP-006-K1* *TSMC 65 NM CMOS MIXED-SIGNAL GENERAL PURPOSE PLUS 1P9M AL_RDL SALICIDE CU_LOWK 1.0&2.5V PDK (CMN65GP)* • *T-N65-CM-SP-012-K1* *TSMC 65 NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SALICIDE CU_LOWK 1.2&3.3V PDK (CRN65LP)*

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Content	Reference Document
	• *T-N55-CL-SP-010-K1* *TSMC 55 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M+AL_RDL SALICIDE CU_LOWK 1.0/2.5V PDK (CLN55GP) (INCLUDED: CLN55GP 1.0V/1.8V, CLN55GP 1.0V/2.5V)* • *T-N55-CM-SP-009-P1-K1:* *TSMC 55NM CMOS MIXED SIGNAL LOW POWER 1P9M+AL_RDL SALICIDE CU_LOWK 1.2V/2.5V PDK*
SRAM	• *T-N65-CL-CL-001* *TSMC 65 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2V 6T SRAM CELL LAYOUT & MODEL* • *T-N65-CL-CL-002* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0V 6T SRAM CELL LAYOUT & MODEL* • *T-N65-CL-CL-003* *TSMC 65 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2V 8T SRAM CELL LAYOUT & MODEL* • *T-N65-CL-CL-004* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0V 8T DP SRAM CELL LAYOUT & MODEL* • *T-N65-CL-CL-005* *TSMC 65 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2V 8T DP_HC SRAM CELL LAYOUT & MODEL* • *T-N65-CL-CL-006* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0V 8T DP_HC SRAM CELL LAYOUT & MODEL* • *T-N65-CL-CL-007* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M SALICIDE CU_LOWK 1.0V 6T and 8T SRAM CELL LAYOUT & MODEL* • *T-N65-CL-CL-012* *TSMC 65 NM CMOS LOGIC ULTRA LOW POWER 1P9M SALICIDE CU_LOWK 1.0V 6T and 8T SRAM CELL LAYOUT & MODEL* • *T-N55-CL-CL-001* *TSMC 55 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M SALICIDE CU_LOWK 6T/8T SRAM CELL LAYOUT & MODEL*
Latch up	• *T-N65-CL-CR-001* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&2.5V CHARACTERIZATION REPORT*
Qualification report	• *T-N65-CL-QR-002* *TSMC 65NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOW K 1.2&2.5V PROCESS QUALIFICATION REPORT -- FAB12* • *T-N65-CL-QR-003* *TSMC 65NM 2XTM PROCESS QUALIFICATION REPORT --FAB12* • *T-N65-CL-QR-004* *TSMC 65NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOW K 1.0&1.8V PROCESS QUALIFICATION REPORT -FAB12* • *T-N65-CL-QR-009* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&2.5V QUALIFICATION REPORT-FAB12* • *T-N65-CL-QR-010* *TSMC 65 NM SECOND INTER-LAYER METAL (MY) PROCESS QUALIFICATION REPORT -FAB12* • *T-N65-CL-QR-011* *TSMC 65NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2V/2.5V SERIAL INTERFACE ELECTRICAL FUSE IP QUALIFICATION REPORT* • *T-N65-CL-QR-012* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0V/1.8V HIGH DENSITY(1K BITS) ELECTRICAL FUSE IP QUALIFICATION REPORT* • *T-N65-CL-QR-016* *TSMC 65NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M SALICIDE CU_LOW K 1.0&1.8V PROCESS QUALIFICATION REPORT - FAB12* • *T-N65-CL-QR-017* *TSMC 65NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M SALICIDE CU_LOW K 1.0&2.5V*

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Content	Reference Document
	PROCESS QUALIFICATION REPORT - FAB12 • *T-N65-CL-QR-035* *TSMC 65NM CMOS LOGIC ULTRA LOW POWER 1P9M SALICIDE CU_LOW K 1.0&2.5V PRODUCT QUALIFICATION REPORT - FAB12* • *S-QCS-04-03-005* *POST CP WAFER QUALITY ASSURANCE SPECIFICATION (BUMP & NON-BUMP WAFER)* • *T-N65-CL-QR-008* *TSMC 65NM CUP WIRE BOND PBGA PACKAGE QUALIFICATION REPORT (DUAL PASSIVATION)-FAB12* • *T-N65-CM-QR-001* *TSMC 65NM MSRF CMOS LOGIC 1P9M SALICIDE CU_LOW K 1.2&2.5V PROCESS QUALIFICATION REPORT - FAB12* • *S-QCS-04-03-005* *POST CP WAFER QUALITY ASSURANCE SPECIFICATION (BUMP & NON-BUMP WAFER)* • *T-N65-BP-QR-001* *TSMC 65NM FLIP CHIP PACKAGE WITH EUTECTIC BUMP QUALIFICATION REPORT (TSMC BUMP + TSMC ASSEMBLY)* • *T-N65-BP-QR-002* *TSMC 65NM FLIP CHIP PACKAGE WITH HIGH LEAD BUMP QUALIFICATION REPORT (TSMC BUMP + TSMC ASSEMBLY)* • *T-N65-CV-QR-001* *TSMC 65 NM CMOS LOGIC LOW POWER HVMOS 1P9M SALICIDE CU_LOW K 1.2&2.5V AND HVMOS (D5G2.5) PROCESS QUALIFICATION REPORT- FAB12* • *T-N65-CL-QR-051* *TSMC 65NM 28K AlCu RDL QUALIFICATION REPORT-FAB14* • *T-N55-CL-QR-016* *TSMC 55 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWER K 1.2&2.5V QUALIFICATION REPORT-FAB14*
Brief process flow	• *T-N65-CL-PF-001* *TSMC 65 NM CMOS LOGIC LOW POWER 1P9M SILICIDE CU_LOWK 1.2&2.5V BRIEF PROCESS FLOW* • *T-N65-CL-PF-005* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SILICIDE CU_LOWK 1.0&1.8&2.5V BRIEF PROCESS FLOW* • *T-N65-CL-PF-006* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&1.8V BRIEF PROCESS FLOW* • *T-N65-CL-PF-010* *TSMC 65 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M SALICIDE CU_LOWK 1.0&1.8V BRIEF PROCESS FLOW* • *T-N65-CL-PF-011* *TSMC 65 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2&3.3V BRIEF PROCESS FLOW* • *T-N65-CL-PF-013* *TSMC 65 NM CMOS LOGIC LP-BASED TRIPLE GATE OXIDE WITH DUAL CORE 1P9M SILICIDE CU_LOWK 1/1.2/2.5V BRIEF PROCESS FLOW* • *T-N65-CL-PF-018* *TSMC 65 NM CMOS LOGIC ULTRA LOW POWER 1P9M SALICIDE NBL/PBL EPI 1.0&2.5V BRIEF PROCESS FLOW* • *T-N55-CL-PF-001* *TSMC 55 NM CMOS LOGIC GENERAL PURPOSE PLUS 1P9M SALICIDE CU_LOWK 1.0&1.8&2.5V BRIEF PROCESS FLOW* • *T-N55-CL-PF-012* *TSMC 55 NM CMOS LOGIC LOW POWER 1P9M SALICIDE NBL/PBL EPI CU_LOWK 1.2&2.5V BRIEF PROCESS FLOW*
Testline Layout Guideline	• *E-MSS-02-02-024* *TSMC TEST LINE LAYOUT USER GUIDELINE*

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2 Technology Overview

This chapter provides information about the following:

2.1 Semiconductor process (including front-end and back-end features)
2.2 Devices
2.3 Power supply and operation temperature ranges
2.4 Cross-section
2.5 Metallization options

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2.1 Semiconductor Process

The process consists of the front-end features and the back-end features.

2.1.1 Front-End Features

- **Shallow trench isolation (STI)**

  Used for active isolation to reduce active pitch (OD pitch)
- **Retrograde twin well CMOS technology on <100> P- substrate (epitaxy wafer) (subtrate resistivity of 8-12 Ω-cm)**

  For a low well sheet resistance and enhancement of latch-up behavior (compared to conventionally diffused wells). Also provides for a good control of short parasitic field transistors.
- **Triple well, Deep N-Well (optional)**

  For isolating P-Well from the substrate
- **Dual gate oxide process**

  CLN55/CLN65 Logic Dual gate oxide (CLN65G: 1.0V/2.5V or 1.0V/1.8V, CLN65GP: 1.0V/2.5V or 1.0V/1.8V, CLN65LP: 1.2V/3.3V or 1.2V/2.5V, CLN65ULP: 1.0V/2.5V, CLN55GP: 1.0V/3.3V, 1.0V/2.5V or1.0V/1.8V, CLN55LP: 1.2V/2.5V)

  CMN55/CMN65 Dual gate oxide (CMN65GP: 1.0V/2.5V, CMN65LP: 1.2V/3.3V or 1.2V/2.5V, CMN55LP: 1.2V/2.5V)
- **Triple gate oxide process**

  CLN65LPG: 1.0V(G)/1.2V(LP)/2.5V
- **N+/P+ poly gate**

  Allows symmetrical design of NMOS and PMOS devices
- **Multiple V_t devices for low leakage or high performance requirements**

  These devices may be mixed on the same die.
- **Native devices with different gate oxide and application volatge**

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- **SRAM cells in different process**

Process Type	N65G/ N65GP	N65LP	N65LPG	N65ULP	N55GP
Cell Size	0.499 μm²/0.525 μm²/ 0.62 μm²/ 0.974 μm²/ 8T 1.158 μm²/ 10T 1.158 μm² (G only)	0.525μm²/ 0.62 μm²/ 0.974 μm²/ 8T 1.158 μm²/	0.525μm²(LP)/ 0.62 μm²(LP, G)/ 0.974 μm²(LP, G)/ 1.158 μm²(LP)	0.525μm²/ 0.62 μm²/ 0.974 μm²	0.525μm²/ 0.62 μm²/ 0.974 μm²

Process Type	N55LP
Cell Size	0.525μm²/ 0.62 μm²/ 0.974 μm²

- **Self-aligned Ni-silicided drain, source and gate**

  Nickel silicide is designed to connect N+ and P+ gates; furthermore, it drastically reduces gate and S/D serial resistance. Self-aligned silicide on source/drain structures allows butting straps with only one minimally sized contact.

- **Unsilicided N+/P+ poly and OD resistors**

  Silicide protectin (requires one additional mask, RPO) is used to prevent silicide formation over the active and poly area.

- **NW resistor**

  Two kinds of NW resistor: 1) NW resistor within OD, and 2) NW resistor under STI

- **Varactor**

  MOS varactor provides 1.0V/1.2V/1.8V/2.5V/3.3V NMOS-in-NW capacitor structure.

- **eDRAM**

  For eDRAM related IP/ Macro design or product with eDRAM IP/ Macro, please notice contact – contact capacitance and contact resistance are higher than those in pure logic process, Need to use eDRAM SPICE model (T-N65-CE-SP-002 and T-N65-CE-SP-003) and RC extraction deck (T-N65-CE-SP-002-B1 and T-N65-CE-SP-003-B1) to specially handle the extra CT-CT coupling capacitance and resistance from eDRAM process for both eDRAM and non-eDRAM portions.

2.1.2 Back-End Features

- **Tungsten contact connecting poly or OD to first metal level**
- **Three to nine Cu metal levels, plus last metal level in Al pad.**
- **Two kinds of inter-layer metal:**
  - Mx: First Inter-layer Metal, W/S=0.1μm/0.1μm, thickness=2200 Å.
  - My: Second Inter-layer Metal, W/S=0.2μm/0.2μm, thickness=5000 Å for CLN65 only, not for CLN55, CMN55 and CMN65
- **Four kinds of top-layer metal:**
  - Mz (4XTM): top metal pitch is four times of Mx pitch (W/S=0.4μm/0.4μm, thickness=9000 Å)
  - My (2XTM): top metal pitch is two times of Mx pitch (W/S=0.2μm/0.2μm, thickness=5000 Å) for CLN65 and CLN55, not for CMN65 and CMN55
  - Mr: top metal pitch is five times of Mx pitch (W/S=0.5μm/0.5μm, thickness=12500 Å) for CLN65 and CLN55, not for CMN65 and CMN55.
  - Mu: top metal for inductor metal, W/S=2μm/2μm, thickness=34000 Å.

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- **AP-MD layer can be used as a redistribution layer (AP RDL) option.**
- **AP-MD layer can be used as interconnection. Two kinds of AP-MD thickness, 14.5K and 28K, are offered. CAD layer (74;0) of both AP-MD is the same.**

	Mask ID	CAD Layer	Thickness (Å)	Remark
AP	307	74	14500	Cannot use for interconnection, RDL
			28000	
AP_MD	309	74	14500	Can use for interconnection, RDL
			28000	

- **Cu RDL is offered. No need extra mask (MD) and just use Cu metal for Cu RDL application.**
- **One or two thick last (top) Cu metal layers at a relaxed pitch for power, clock, busses, and major interconnect signal distribution**
- **Tight pitch levels for routing on thin Cu for the other metal levels below the thick level**
- **Chemical mechanical polishing (CMP) for enhanced planarization (STI, contact, metals, vias, passivation)**
- **Dual damascene copper interconnection, for metal-2 to the last (top) metal**
- **Low K (< 3.0) inter-metal dielectric for thin metal**
- **Metal oxide metal (MOM) capacitor**
  - Use metal lines to design metal capacitor.
- **Metal-insulator-metal (MIM) capacitor for N65 Mixed Signal and RF process:**
  - Use the PEOX USG film as the dielectric film of MiM capacitors and use TaN/AlCu as the capacitor metal plate. 3 kinds of MiM process are supported:1.0fF/μm2, 1.5fF/μm2, 2.0fF/μm2. Only one kind of MIM capacitor can be used in the chip.
- **High-Q copper inductor for CMN65GP/LP and CMN55LP Mixed Signal and RF process:**
  - Have ultra thick Cu (Mu, 34 KÅ) process for inductor metal.
- **TSMC N55 generation does not support MIM capacitor.**
- **Wire bond or flip chip terminals**
- **Laser fuse**

  AP fuse is available. Please refer to T-000-CL-DR-005: TSMC AL FUSE (AP FUSE) DESIGN RULE FOR CU PROCESS
- **Electrical fuse**

  The IP of electrical fuse is provided. Please contact your account manager to get the related information. Besides, the IP can't be shrunk at N55.

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2.2 Devices

The technology provides multiple V_t devices, thin and thick gate oxide native devices, MOM, MIM, and inductor

Table 2.2.1 Available Vt/ MOM/ MIM/ Inductor in each technology

Core	CLN65						CLN55	
	G (1.0V)	GP (1.0V)	LP (1.2V)	ULP (1.0V)	LPG		GP (1.0V)	LP (1.2V)
					LP (1.2V)	G (1.0V)		
High Vt	V	V	V	V	V	V	V	V
STD Vt	V	V	V	V	V	V	V	V
Low Vt	-	V	V	V	V	-	V	V
Native	V	V	V	V	V	V	V	V
m-low Vt	-	-	V	V	-	-	-	
MOM	V	V	V	V	V	V	V	V
MIM	-	-	-	-	-	-	-	-
Inductor	-	-	-	-	-	-	-	-

Core	CMN65 for MS		CMN65 for RF		CMN55 for MS	CMN55 for RF
	GP (1.0V)	LP (1.2V)	GP (1.0V)	LP (1.2V)	LP (1.2V)	LP (1.2V)
High Vt	V	V	V	V	V	V
STD Vt	V	V	V	V	V	V
Low Vt	V	V	V	V	V	V
Native	V	V	-*	-*	V	-
m-low Vt	-	V	-	-	-	-
MOM	V	V	V	V	V	V
MIM	V	V	V	V	-	-
Inductor	-	-	V	V	-	V

* : For RF process, TSMC provides Native device, but don't provide the SPICE model.

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2.3 Power Supply and Operation Temperature Ranges

Table 2.3.1 Power Supplies

	CLN65									
	G		GP		LP		ULP		LPG	
	Normal power supply	*Max power supply	Normal power supply	*Max power supply	Normal power supply	*Max power supply	Normal power supply	*Max power supply	Normal power supply	*Max power supply
Core (thin oxide)	1.0V	1.1V	1.0V	1.1V	1.2V	1.32V	1.0V	1.1V	1.0V(G) 1.2V (LP)	1.1V 1.32V
I/O (thick oxide)	1.8V	1.98V	1.8V	1.98V	-	-	-	-	-	
	2.5V	2.75V	2.5V	2.75V	2.5V	2.75V	2.5V	2.75V	2.5V	2.75V
	-	-	-	-	3.3V	3.63V	-	-	-	-
2.5V overdrive to 3.3V	3.3V	3.63V	3.3V	3.63V	3.3V	3.63V	3.3V	3.63V	3.3V	3.63V
2.5V underdrive to 1.8V	1.8V	1.98V	1.8V	1.98V	1.8V	1.98V	1.8V	1.98V	1.8V	1.98V
**5V HVMOS only for LP 2.5V IO	-	-	-	-	5V (drain)/ 2.5V (G/S/B)	5.5V (drain)/ 2.75V (G/S/B)	-	-	-	-
	CLN55				CMN65				CMN55	
	GP		LP		GP		LP		LP	
	Normal power supply	*Max power supply	Normal power supply	*Max power supply	Normal power supply	*Max power supply	Normal power supply	*Max power supply	Normal power supply	*Max power supply
Core (thin oxide)	1.0V	1.1V	1.2V	1.32V	1.0V	1.1V	1.2V	1.32V	1.2V	1.32V
I/O (thick oxide)	1.8V	1.98V	-	-	-	-	-	-	-	-
	2.5V	2.75V	2.5V	2.75V	2.5V	2.75V	2.5V	2.75V	2.5V	2.75V
	3.3V	3.63V	-	-	-	-	3.3V	3.63V	-	-
2.5V overdrive to 3.3V	3.3V	3.63V	3.3V	3.63V	3.3V	3.63V	3.3V	3.63V	3.3V	3.63V
2.5V underdrive to 1.8V	-	-	1.8V	1.98V	1.8V	1.98V	1.8V	1.98V	1.8V	1.98V
**5V HVMOS only for LP 2.5V IO	-	-	5V (drain)/ 2.5V (G/S/B)	5.5V (drain)/ 2.75V (G/S/B)	-	-	5V (drain)/ 2.5V (G/S/B)	5.5V (drain)/ 2.75V (G/S/B)	-	-

** Only drain side can be applied. The other terminals can only be applied to 2.5V.
The operation temperature range is -40°C to 125°C (junction temperature).

For the detail information of both 2.5V overdrive to 3.3V, and 2.5V underdrive to 1.8V, please refer to section 4.5.9 and 4.5.10. 2.5V underdrive to 1.8V is not offered in 2.5V native device.

* Maximum power supply voltage means variation upper limit of product operation voltage.

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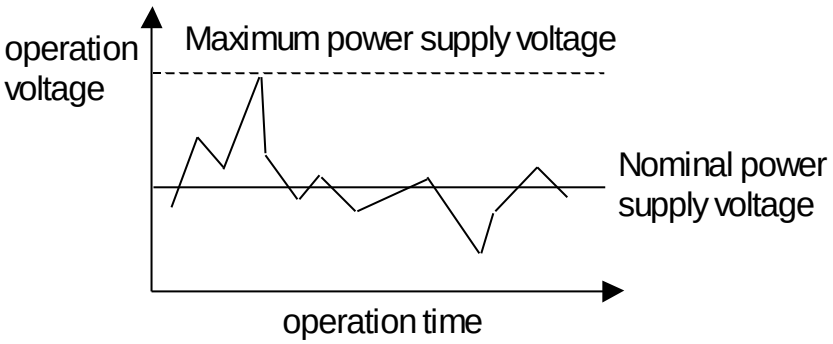

Beside regular 1.2V core MOS and 2.5V IO MOS in N65LP 1.2/2.5V logic process, there is additional 5V HVMOS including NMOS/PMOS are offered and the bias condition of the four terminals (Gate/ Drain/ Source/ Bulk) are as the following table 2.3.2 HVMOS device list and spec.

Table 2.3.2 HVMOS deive list and spec

Device	|Vgs|	|Vds|	|Vbs|
HV NMOS (5V)	0~2.5V	0~5V	0~2.5V
HV PMOS (5V)	0~2.5V	0~5V	0~2.5V

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12/16/2016
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2.4 Cross-section

Cross section (1-9M as inter Mx, top My(2XTM))

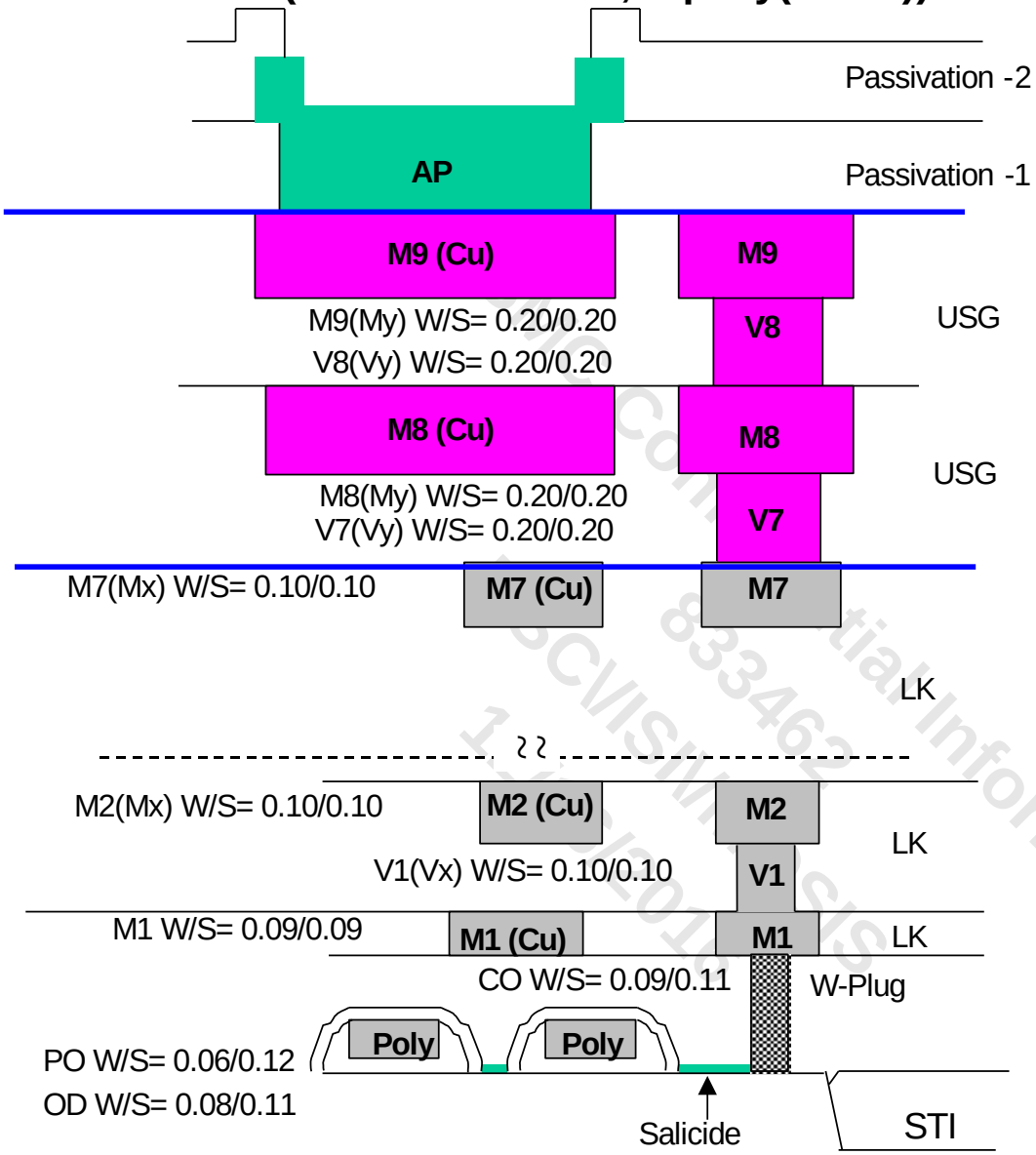

Figure 2.4.1 Cross-section for 1P9M_6x2y

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Cross section (1P9M as intex Mx, top Mz(4XTM))

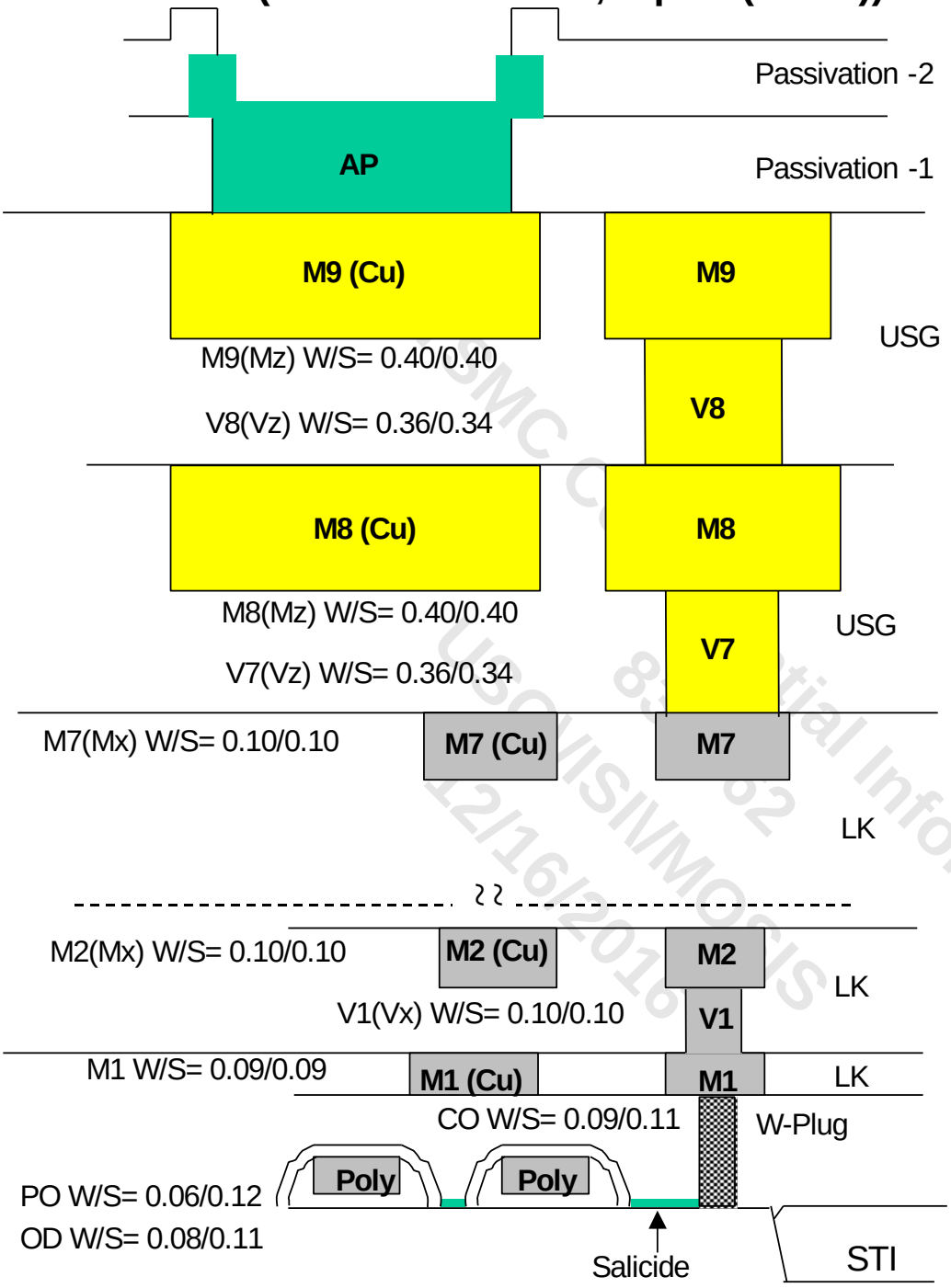

Figure 2.4.2 Cross-section for 1P9M_6x2z

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Cross section (1P9M as intex Mx/My, top Mz(4XTM))

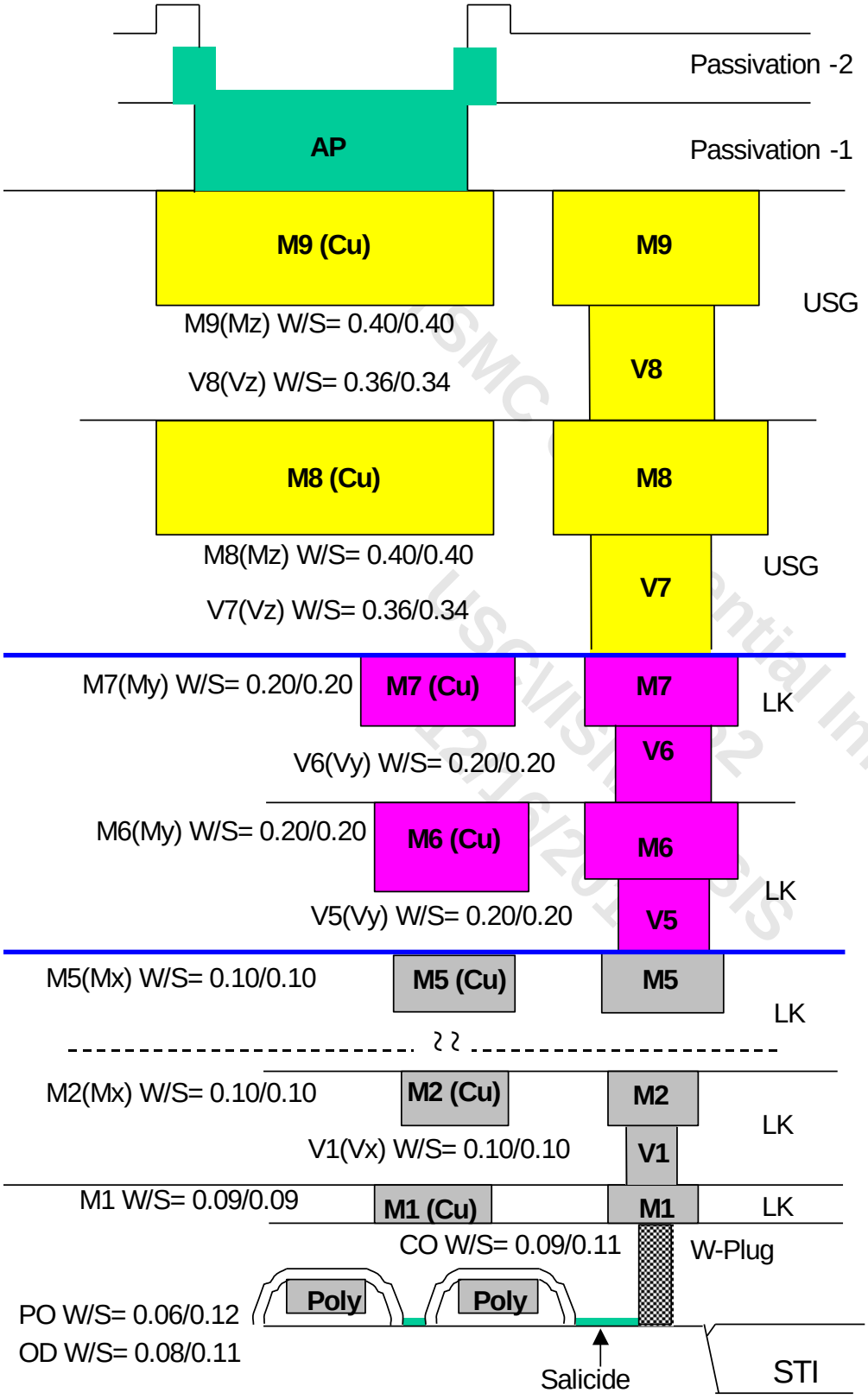

Figure 2.4.3 Cross-section for 1P9M_4x2y2z

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Cross section (1P9M as intex Mx, top Mr)

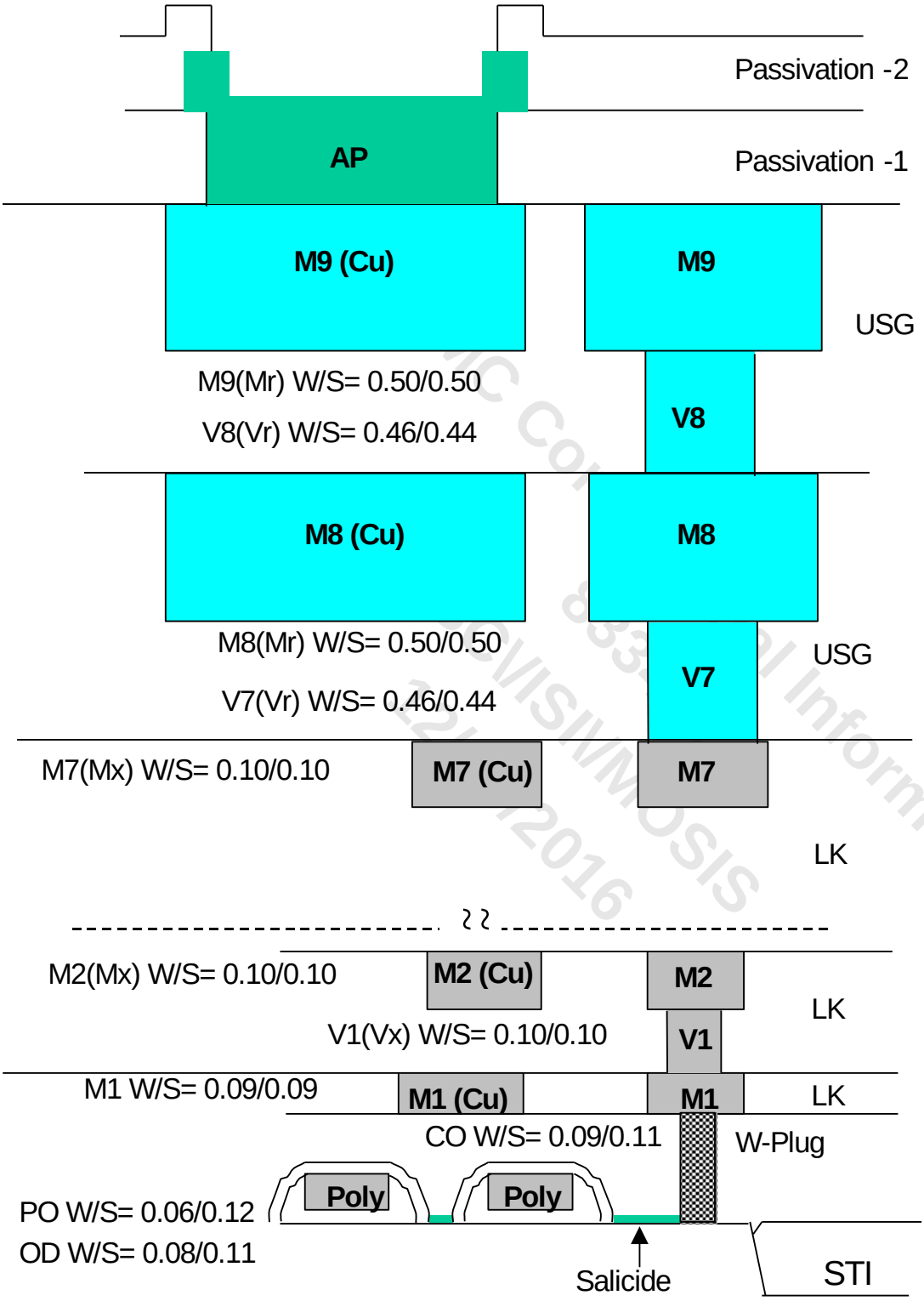

Figure 2.4.4 Cross-section for 1P9M_6x2r

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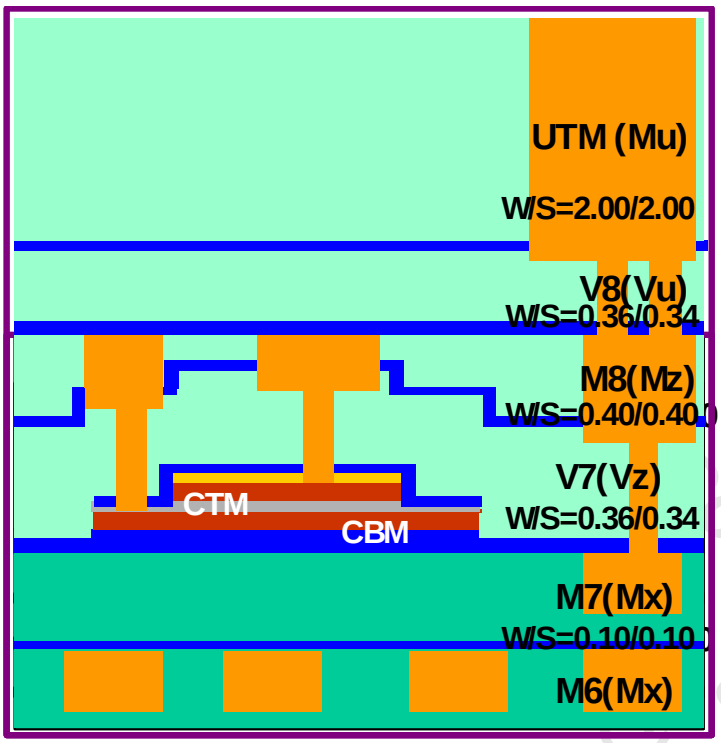
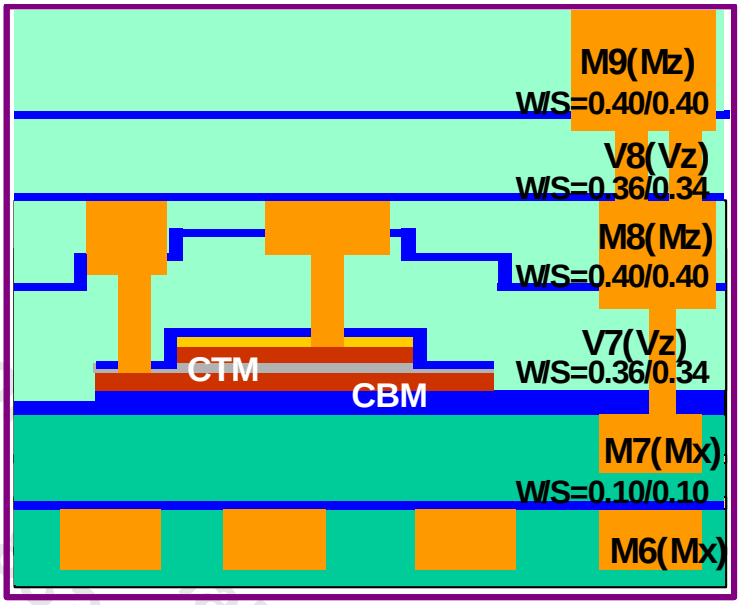
Cross section for CMN65

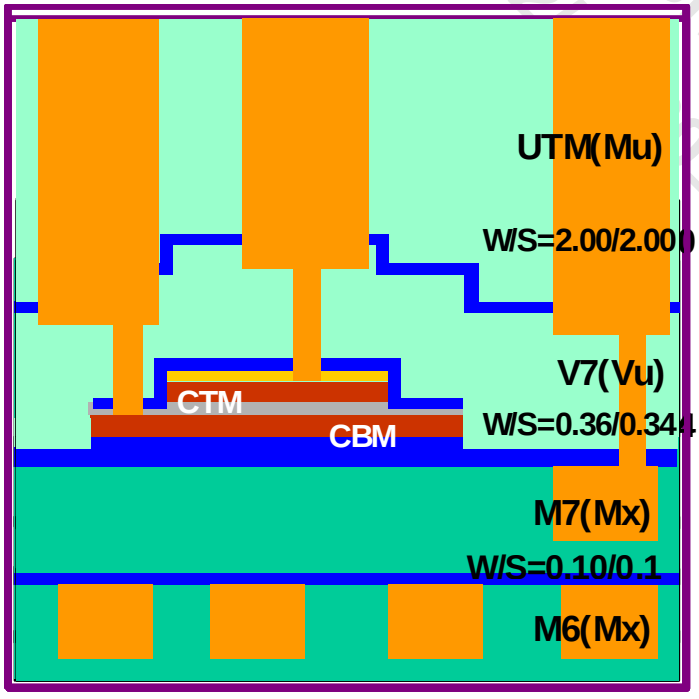
(1) 1P9M: MIM between M7 and M8 with Mu (34KÅ)



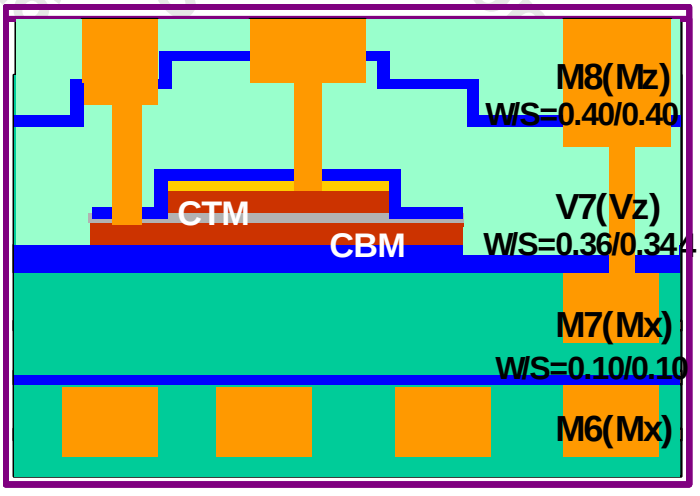
(2) 1P9M: MIM between M7 and M8, without Mu



(3) 1P8M: MIM between M7 and M8 (M8 is Mu)



(4) 1P8M: MIM between M7and M8, without Mu



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2.5 Metallization Options

The general 65 nm and 55nm are offered with a single poly and nine metal layers (1P9M). In addition to 1P9M, please refer to the following tables for the other metallization options.

Table 2.5.1 Naming for Different Metal Thicknesses

Metal type	Code	W/S (μm)				Thickness (Å).				Mask layers
		CLN65	CLN55	CMN65	CMN55	CLN65	CLN55	CMN65	CMN55	
M1	M1	0.09/0.09	0.09/0.09	0.09/0.09	0.09/0.09	1800	1600	1800	1600	M1 (360) only
First Inter-layer Metal	Mx	0.1/0.1	0.1/0.1	0.1/0.1	0.1/0.1	2200	2000	2200	2000	M2~M7 (380, 381, 384, 385, 386, 387), max : six layers
Second Inter-layer Metal	My	0.2/0.2	Not offer	Not offer	Not offer	5000	Not offer	Not offer	Not offer	M5~M7 (385, 386, 387), max : two layers
Top Metal (2XTM)	My	0.2/0.2	0.2/0.2	Not offer	Not offer	5000	5000	Not offer	Not offer	M3~M9 (381, 384, 385, 386, 387, 388, 389), max : two layers
Top Metal (4XTM)	Mz	0.4/0.4	0.4/0.4	0.4/0.4	0.4/0.4	9000	9000	9000	9000	M3~M9 (381, 384, 385, 386, 387, 388, 389), max : two layers
Top Metal	Mr	0.5/0.5	0.5/0.5	Not offer	Not offer	12500	12500	Not offer	Not offer	M6~M9 (386, 387, 388, 389), max: two layers
Top Metal (UTM)	Mu	Not offer	Not offer	2/2	2/2	Not offer	Not offer	34000	34000	M4~M9 (384, 385, 386, 387, 388, 389), max : one layer
AP-MD*	AP-MD	3/2	3/2	3/2	3/2	14500	14500	14500	14500	AP-MD(307 or 309) Max: one layer. 14.5K and 28KÅ are offered.
						28000	28000	28000	28000	

Table 2.5.2 Naming for Different Via Types

Via type	Code	W/S(μm)				Mask layers
		CLN65	CLN55	CMN65	CMN55	
First Inter-layer Via	Vx	0.1/0.1	0.1/0.1	0.1/0.1	0.1/0.1	VIA1~VIA6 (378, 379, 373, 374, 375, 376), max : six layers
Second Inter-layer Via	Vy	0.2/0.2	Not offer	Not offer	Not offer	VIA4~VIA6 (374, 375, 376), max : two layers
Top Via (2XTM)	Vy	0.2/0.2	0.2/0.2	Not offer	Not offer	VIA2~VIA8 (379, 373, 374, 375, 376, 377, 372), max : two layers
Top Via (4XTM)	Vz	0.36/0.34	0.36/0.34	0.36/0.34	0.36/0.34	VIA2~VIA8 (379, 373, 374, 375, 376, 377, 372), max : two layers
Top Via	Vr	0.46/0.44	0.46/0.44	Not offer	Not offer	VIA5~VIA8 (375, 376, 377, 372), max: two layers
Top Via (UTM)	Vu	Not offer	Not offer	0.36/0.34	0.36/0.34	VIA3~VIA8 (373, 374, 375, 376, 377, 372),max : one layer
RV*	RV	3/3	3/3	3/3	3/3	RV (306), max: one layer

*: 1. With AP-MD process, CBD (mask 306)/ AP-MD (mask 309)/ CB2 (mask 308) are used. RV is needed to connect AP-MD and Mtop when AP-MD is an additional interconnection layer.
2. Without AP-MD process, CB (CBD) (mask 107)/ AP (mask 307)/ CB(CBD) (mask 107) are used and no RV layer is used. CB layer is for interconnection usage.

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Table 2.5.3 CLN65/CLN55 Metallization Options (My/Vy are used as second inter-layer Metal/Via)

Metal /Via	Total Number of Metal Layers																	
	3	4	5		6			7				8				9		
CLN65	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**
CLN55	**V**	**V**	**V**	**V**	**V**	**V**	**X**	**V**	**V**	**X**	**X**	**V**	**V**	**X**	**X**	**V**	**X**	**X**
M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
VIA1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1
M2	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1
VIA2	**Vz1**	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2
M3	**Mz1**	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2
VIA3		**Vz1**	Vx3	**Vz1**	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3
M4		**Mz1**	Mx3	**Mz1**	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3
VIA4			**Vz1**	**Vz2**	Vx4	**Vz1**	Vy1	Vx4	Vx4	Vx4	Vy1	Vx4	Vx4	Vx4	Vx4	Vx4	Vx4	Vx4
M5			**Mz1**	**Mz2**	Mx4	**Mz1**	My1	Mx4	Mx4	Mx4	My1	Mx4	Mx4	Mx4	Mx4	Mx4	Mx4	Mx4
VIA5					**Vz1**	**Vz2**	**Vz1**	Vx5	**Vz1**	Vy1	Vy2	Vx5	Vx5	Vy1	Vy1	Vx5	Vx5	Vy1
M6					**Mz1**	**Mz2**	**Mz1**	Mx5	**Mz1**	My1	My2	Mx5	Mx5	My1	My1	Mx5	Mx5	My1
VIA6								**Vz1**	**Vz2**	**Vz1**	**Vz1**	Vx6	**Vz1**	Vy2	**Vz1**	Vx6	Vy1	Vy2
M7								**Mz1**	**Mz2**	**Mz1**	**Mz1**	Mx6	**Mz1**	My2	**Mz1**	Mx6	My1	My2
VIA7												**Vz1**	**Vz2**	**Vz1**	**Vz2**	**Vz1**	**Vz1**	**Vz1**
M8												**Mz1**	**Mz2**	**Mz1**	**Mz2**	**Mz1**	**Mz1**	**Mz1**
VIA8																**Vz2**	**Vz2**	**Vz2**
M9																**Mz2**	**Mz2**	**Mz2**
RV	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
AP-MD	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V

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Table 2.5.4 CLN65/CLN55 Metallization Options (My/Vy are used as 2X top Metal/Via)

Metal /Via	Total Number of Metal Layers										
	3	**4**	**5**		**6**		**7**		**8**		**9**
CLN65	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**
CLN55	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**	**V**
M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
VIA1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1
M2	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1
VIA2	**Vy1**	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2
M3	**My1**	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2
VIA3		**Vy1**	Vx3	**Vy1**	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3
M4		**My1**	Mx3	**My1**	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3
VIA4			**Vy1**	**Vy2**	Vx4	**Vy1**	Vx4	Vx4	Vx4	Vx4	Vx4
M5			**My1**	**My2**	Mx4	**My1**	Mx4	Mx4	Mx4	Mx4	Mx4
VIA5					**Vy1**	**Vy2**	Vx5	**Vy1**	Vx5	Vx5	Vx5
M6					**My1**	**My2**	Mx5	**My1**	Mx5	Mx5	Mx5
VIA6							**Vy1**	**Vy2**	Vx6	**Vy1**	Vx6
M7							**My1**	**My2**	Mx6	**My1**	Mx6
VIA7									**Vy1**	**Vy2**	**Vy1**
M8									**My1**	**My2**	**My1**
VIA8											**Vy2**
M9											**My2**
RV	V	V	V	V	V	V	V	V	V	V	V
AP-MD	V	V	V	V	V	V	V	V	V	V	V

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Table 2.5.5 CLN65/CLN55 Metallization Options for Mr

Metal /Via	Total Number of Metal Layers					
	6	7		8		9
CLN65	**V**	**V**	**V**	**V**	**V**	**V**
CLN55	**V**	**V**	**V**	**V**	**V**	**V**
M1	M1	M1	M1	M1	M1	M1
VIA1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1
M2	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1
VIA2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2
M3	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2
VIA3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3
M4	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3
VIA4	Vx4	Vx4	Vx4	Vx4	Vx4	Vx4
M5	Mx4	Mx4	Mx4	Mx4	Mx4	Mx4
VIA5	**Vr1**	Vx5	**Vr1**	Vx5	Vx5	Vx5
M6	**Mr1**	Mx5	**Mr1**	Mx5	Mx5	Mx5
VIA6		**Vr1**	**Vr2**	Vx6	**Vr1**	Vx6
M7		**Mr1**	**Mr2**	Mx6	**Mr1**	Mx6
VIA7				**Vr1**	**Vr2**	**Vr1**
M8				**Mr1**	**Mr2**	**Mr1**
VIA8						**Vr2**
M9						**Mr2**
RV	V	V	V	V	V	V
AP-MD	V	V	V	V	V	V

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833462
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12/16/2016

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Table 2.5.6 CM65 metallization options for Mz or Mu (one Mz or Mu layer above MIM, Figure (3) and (4)of Crossection)

Metal /Via	Total Number of Metal Layers									
	4		5		6		7		8	
M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
VIA1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1
M2	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1
VIA2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2
M3	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2
VIA3	**Vz1**	**Vu1**	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3
M4	**Mz1**	**Mu1**	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3
VIA4			**Vz1**	**Vu1**	Vx4	Vx4	Vx4	Vx4	Vx4	Vx4
M5			**Mz1**	**Mu1**	Mx4	Mx4	Mx4	Mx4	Mx4	Mx4
VIA5					**Vz1**	**Vu1**	Vx5	Vx5	Vx5	Vx5
M6					**Mz1**	**Mu1**	Mx5	Mx5	Mx5	Mx5
VIA6							**Vz1**	**Vu1**	Vx6	Vx6
M7							**Mz1**	**Mu1**	Mx6	Mx6
VIA7									**Vz1**	**Vu1**
M8									**Mz1**	**Mu1**
RV	V	V	V	V	V	V	V	V	V	V
AP-MD	V	V	V	V	V	V	V	V	V	V
MIM location	M3~M4		M4~M5		M5~M6		M6~M7		M7~M8	

Note:

1. The mark " ═══ " in the above table stands for MIM layer.
2. MIM must be placed between Mx and Mz, or between Mx and Mu.

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Table 2.5.7 CMN65 metallization options for Mz without Mu (two Mz layers above MIM, Figure (2) of Crossection):

Metal /Via	Total Number of Metal Layers				
	5	**6**	**7**	**8**	**9**
M1	M1	M1	M1	M1	M1
VIA1	Vx1	Vx1	Vx1	Vx1	Vx1
M2	Mx1	Mx1	Mx1	Mx1	Mx1
VIA2	Vx2	Vx2	Vx2	Vx2	Vx2
M3	Mx2	Mx2	Mx2	Mx2	Mx2
VIA3	**Vz1**	Vx3	Vx3	Vx3	Vx3
M4	**Mz1**	Mx3	Mx3	Mx3	Mx3
VIA4	**Vz2**	**Vz1**	Vx4	Vx4	Vx4
M5	**Mz2**	**Mz1**	Mx4	Mx4	Mx4
VIA5		**Vz2**	**Vz1**	Vx5	Vx5
M6		**Mz2**	**Mz1**	Mx5	Mx5
VIA6			**Vz2**	**Vz1**	Vx6
M7			**Mz2**	**Mz1**	Mx6
VIA7				**Vz2**	**Vz1**
M8				**Mz2**	**Mz1**
VIA8					**Vz2**
M9					**Mz2**
RV	V	V	V	V	V
AP-MD	V	V	V	V	V
MIM location	M3~M4	M4~M5	M5~M6	M6-M7	M7~M8

Note:

1. The mark " ═══ " in the above table stands for MIM layer.
2. MIM must be placed between Mx and Mz. MIM can not be located between Mz and Mz.

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Table 2.5.8 CMN65 metallization for Mz with Mu (Mz+Mu layers above MIM, Figure (1) of Crossection):

Metal /Via	Total Number of Metal Layers				
	5	**6**	**7**	**8**	**9**
M1	M1	M1	M1	M1	M1
VIA1	Vx1	Vx1	Vx1	Vx1	Vx1
M2	Mx1	Mx1	Mx1	Mx1	Mx1
VIA2	Vx2	Vx2	Vx2	Vx2	Vx2
M3	Mx2	Mx2	Mx2	Mx2	Mx2
VIA3	**Vz1**	Vx3	Vx3	Vx3	Vx3
M4	**Mz1**	Mx3	Mx3	Mx3	Mx3
VIA4	**Vu1**	**Vz1**	Vx4	Vx4	Vx4
M5	**Mu1**	**Mz1**	Mx4	Mx4	Mx4
VIA5		**Vu1**	**Vz1**	Vx5	Vx5
M6		**Mu1**	**Mz1**	Mx5	Mx5
VIA6			**Vu1**	**Vz1**	Vx6
M7			**Mu1**	**Mz1**	Mx6
VIA7				**Vu1**	**Vz1**
M8				**Mu1**	**Mz1**
VIA8					**Vu1**
M9					**Mu1**
RV	V	V	V	V	V
AP-MD	V	V	V	V	V
MIM location	M3~M4	M4~M5	M5~M6	M6-M7	M7~M8

Note:

1. The mark " ═══ " in the above table stands for MIM layer.
2. MIM must be placed between Mx and Mz. MIM can not be located between Mz and Mu.

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Table 2.5.9 CMN55LP metallization options for Mz or Mu

Metal /Via	Total Number of Metal Layers									
	4		5		6		7		8	
M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
VIA1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1	Vx1
M2	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1	Mx1
VIA2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2	Vx2
M3	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2	Mx2
VIA3	**Vz1**	**Vu1**	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3	Vx3
M4	**Mz1**	**Mu1**	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3	Mx3
VIA4			**Vz1**	**Vu1**	Vx4	Vx4	Vx4	Vx4	Vx4	Vx4
M5			**Mz1**	**Mu1**	Mx4	Mx4	Mx4	Mx4	Mx4	Mx4
VIA5					**Vz1**	**Vu1**	Vx5	Vx5	Vx5	Vx5
M6					**Mz1**	**Mu1**	Mx5	Mx5	Mx5	Mx5
VIA6							**Vz1**	**Vu1**	Vx6	Vx6
M7							**Mz1**	**Mu1**	Mx6	Mx6
VIA7									**Vz1**	**Vu1**
M8									**Mz1**	**Mu1**
RV	V	V	V	V	V	V	V	V	V	V
AP-MD	V	V	V	V	V	V	V	V	V	V

Table 2.5.10 CMN55LP metallization options for Mz without Mu

Metal /Via	Total Number of Metal Layers				
	5	6	7	8	9
M1	M1	M1	M1	M1	M1
VIA1	Vx1	Vx1	Vx1	Vx1	Vx1
M2	Mx1	Mx1	Mx1	Mx1	Mx1
VIA2	Vx2	Vx2	Vx2	Vx2	Vx2
M3	Mx2	Mx2	Mx2	Mx2	Mx2
VIA3	**Vz1**	Vx3	Vx3	Vx3	Vx3
M4	**Mz1**	Mx3	Mx3	Mx3	Mx3
VIA4	**Vz2**	**Vz1**	Vx4	Vx4	Vx4
M5	**Mz2**	**Mz1**	Mx4	Mx4	Mx4
VIA5		**Vz2**	**Vz1**	Vx5	Vx5
M6		**Mz2**	**Mz1**	Mx5	Mx5
VIA6			**Vz2**	**Vz1**	Vx6
M7			**Mz2**	**Mz1**	Mx6
VIA7				**Vz2**	**Vz1**
M8				**Mz2**	**Mz1**
VIA8					**Vz2**
M9					**Mz2**
RV	V	V	V	V	V
AP-MD	V	V	V	V	V

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Table 2.5.11 CMN55LP metallization for Mz with Mu:

Metal /Via	Total Number of Metal Layers				
	5	**6**	**7**	**8**	**9**
M1	M1	M1	M1	M1	M1
VIA1	Vx1	Vx1	Vx1	Vx1	Vx1
M2	Mx1	Mx1	Mx1	Mx1	Mx1
VIA2	Vx2	Vx2	Vx2	Vx2	Vx2
M3	Mx2	Mx2	Mx2	Mx2	Mx2
VIA3	**Vz1**	Vx3	Vx3	Vx3	Vx3
M4	**Mz1**	Mx3	Mx3	Mx3	Mx3
VIA4	**Vu1**	**Vz1**	Vx4	Vx4	Vx4
M5	**Mu1**	**Mz1**	Mx4	Mx4	Mx4
VIA5		**Vu1**	**Vz1**	Vx5	Vx5
M6		**Mu1**	**Mz1**	Mx5	Mx5
VIA6			**Vu1**	**Vz1**	Vx6
M7			**Mu1**	**Mz1**	Mx6
VIA7				**Vu1**	**Vz1**
M8				**Mu1**	**Mz1**
VIA8					**Vu1**
M9					**Mu1**
RV	V	V	V	V	V
AP-MD	V	V	V	V	V

Table 2.5.12 Top metal numbers My, Mz, Mr, or Mu for wire bond and flip chip.

	My	**Mz**	**Mr**	**Mu**
Wire bond	1 or 2 layers of My	1 or 2 layers of Mz	1or 2 layers of Mr	1 layer of Mu
Flip Chip	2 layers of My	1 or 2 layers of Mz	1 or 2 layers of Mr	1 layer of Mu

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12/16/2016

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3 General Layout Information

This chapter provides the following general layout information:

3.1 Mask information, key process sequence, and CAD layers
3.2 Metal/via CAD layer information for metallization options
3.3 Dummy pattern fill CAD Layers
3.4 Special recognition CAD layers summary
3.5 Device truth tables
3.6 Mask requirement for device options (High/STD/Low Vt)
3.7 Design geometry restrictions
3.8 Design hierarchy guidelines

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3.1 Mask Information, Key Process Sequence, and CAD Layers

Tables in the section 3.1 lists masks and corresponding masking steps.

1. The **VTC_N/VTC_P** mask is a default mask generated from a logic operation (SRM NOT NW) for those you who use certain SRAM cell IP. Please see the "Special Recognition CAD Layer Summary" section in this chapter for information about the SRM layer.
2. TSMC uses NW and OD2 (OD_18, OD_25, OD_33) to generate **NW1V, PW1V, and PW2V** masks by logical operations. Designers can draw NW only.
3. TSMC uses NP, PP, and other layers to generate **N1V, N2V, P1V, and P2V** masks by logical operations. Designers do not need to draw these masks.
4. SEALRING layer (CAD layer: 162) is a must for VIAx if either you add seal ring by themselves or metal fuse is used. SEALRING layer (CAD layer: 162) is only allowed in seal ring and fuse protection ring.
5. An **Al pad** is a reverse tone of CB with bias. However, in a flip-chip product, Al pad is a drawn layer.

The **Mask Name column** lists names that are reserved for standard mask steps. These names should not be used for another purpose in tape out files without prior authorization from TSMC.

The **CAD Layer column** lists CAD layer numbers. To obtain all related CAD layer usage information, please refer to TSMC Document, T-N65-CL-LE-001

6. In the tabe of section 3.1, " * " means optional mask. " # " means non-design level mask which is no need to draw (or design) this layer. This non-design level mask is generated by logical operation from other drawn layers.

Warning: A CAD layer number must be less than, or equal to, 255. If the number is greater than 255, the mask making will fail.

Warning:

For N65:

1. Need to re-tapeout 124 mask if 112, 113, 152, or 199 GDS are changed.
2. Need to re-tapeout 14A mask if 112, 113 or 199 GDS are changed.

For N55:

1. Need to re-tapeout 124 mask if 112, 113 or 152 GDS are changed.
2. Need to re-tapeout 14A mask if 112 or 113 GDS are changed.

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Table 3.1.1 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN65LP2.5V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	OD_25, NW, NT_N, HVD_P	Core device P-Well.
4*#	VTC_N	112	C	Derived	SRM, SRM_11, SRM_12, SRM_13, SRM_14, NW, VTH_N	It's a must for std Vt SRAM cell (0.525 μm²). High Vt SRAM cell and std Vt SRAM cell (0.62 μm², 0.97um², 1.15um²) don't need VTC_N.
5#	PW2V	193	C	Derived	OD_25, NW, NT_N, HVD_N, OD, PO	2.5V P-Well.
6*	VTL_N	118	C	Derived	OD_25, NW, NT_N, VTL_N, HVD_P	Low Vt NMOS implantation for LP only.
7*	VTH_N	128	C	67	-	High Vt NMOS implantation.
8#	NW1V	192	C	Derived	NW, NT_N	Core device and 2.5V N-Well.
9*	VTL_P	117	C	Derived	OD_25, NW, NT_N, VTL_P, HVD_N	Low Vt PMOS implantation for LP only.
10*	VTH_P	127	C	68	-	High Vt PMOS implantation.
11	OD2	152	D	18	-	2.5V thick oxide for DGO process.
12#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
13	PO	130	D	Derived	PO, OD, OD_25, NP, PP, SRM, mVTL, DPO	Poly-Si.
14#	N2V	116	C	Derived	NP, NW, OD_25, RH, VAR, NT_N, POFUSE, PO, OD, RPO, HVD_N	2.5V NLDD implantation.
15#	P2V	115	C	Derived	PP, NW, OD_25, RH, VAR, PO, OD, RPO, HVD_P	2.5V PLDD implantation.
16#	N1V	114	C	Derived	NP, NW, OD_25, RH, VAR, POFUSE, BJTDMY, PO, OD, RPO	Core device NLDD implantation.
17#	P1V	113	C	Derived	PP, NW, OD_25, RH, VAR, BJTDMY, PO, OD, RPO	Core device PLDD implantation.
18	NP	198	C	Derived	NP, SRM	N+ implantation.
19	PP	197	C	Derived	PP, SRM	P+ implantation.
20*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3, ESDIMP	ESD implantation.
21	RPO	155	D	29	-	Silicide protection.
22	CO	156	C	Derived	CO, CO_11, OD, SRAMDMY_4.	Contact window from M1 to OD or PO.
23	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
24	VIA1	378	C	51	-	Via1 hole between M2 and M1.
25	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
26	VIA2	379	C	52	-	Via2 hole between M3 and M2.
27	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
28	VIA3	373	C	53	-	Via3 hole between M4 and M3.
29	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
30	VIA4	374	C	54	-	Via4 hole between M5 and M4.
31	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
32	VIA5	375	C	55	-	Via5 hole between M6 and M5.
33	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
34	VIA6	376	C	56	-	Via6 hole between M7 and M6.
35	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
36	VIA7	377	C	57	-	Via7 hole between M8 and M7.
37	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
38	VIA8	372	C	58	-	Via8 hole between M9 and M8.
39	M9	389	C	Derived	M9, DM9	9th metal for interconnection.
FBEOL option1 (Wire bond without (AP Fuse or AP RDL))						
40	CB	107	C	76	-	Passivation-1 open for bond pad.
41#	AP	307	D	Derived	CB	Al pad.
42	CB	107	C	76	-	Passivation-2 open for bond pad.
FBEOL option2 (Flip chip without (AP Fuse or AP RDL))						
40	CB	107	C	169	-	Passivation-1 open for bond pad.
41	AP	307	D	74	-	Al pad.
42	CB	107	C	169	-	Passivation-2 open for bond pad.
FBEOL option3 (Wire bond with (AP Fuse or AP RDL))						
40	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
41	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
42*	FW_AP	30A	C	95;20	-	AP fuse window.
43	CB2	308	C	86	-	Passivation-2 open.
FBEOL option4 (Flip chip with (AP Fuse or AP RDL))						
40	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
41	AP-MD	309	D	74	-	Al pad, AP RDL, Al fuse.
42*	FW_AP	30A	C	95;20	-	AP fuse window.
43	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.2 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN65LP3.3V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	OD_33, NW, NT_N	Core device P-Well.
4*#	VTC_N	112	C	Derived	SRM, SRM_11, SRM_12, SRM_13, SRM_14,NW, VTH_N	It's a must for std Vt SRAM cell (0.525 μm²). High Vt SRAM cell and std Vt SRAM cell (0.62 μm², 0.97um², 1.15um²) don't need VTC_N.
5#	PW2V	193	C	Derived	OD_33, NW, NT_N	3.3V P-Well.
6*	VTL_N	118	C	Derived	OD_33, NW, NT_N, VTL_N	Low Vt NMOS implantation for LP only.
7*	VTH_N	128	C	67	-	High Vt NMOS implantation.
8#	NW1V	192	C	Derived	NW, NT_N	Core device and 3.3V N-Well.
9#	NW2V	194	C	Derived	OD_33, NW, NT_N	3.3V N-Well.
10*	VTL_P	117	C	Derived	OD_33, NW, NT_N, VTL_P	Low Vt PMOS implantation for LP only.
11*	VTH_P	127	C	68	-	High Vt PMOS implantation.
12	OD2	152	D	15	-	3.3V thick oxide for DGO process.
13#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
14	PO	130	D	Derived	PO, OD, OD_33, NP, PP, SRM, mVTL, DPO	Poly-Si.
15#	N2V	116	C	Derived	NP, NW, OD_33, RH, VAR, NT_N, POFUSE, PO, OD, RPO	3.3V NLDD implantation.
16#	P2V	115	C	Derived	PP, NW, OD_33, RH, VAR, PO, OD, RPO	3.3V PLDD implantation.
17#	N1V	114	C	Derived	NP, NW, OD_33, RH, VAR, POFUSE, BJTDMY, PO, OD, RPO	Core device NLDD implantation.
18#	P1V	113	C	Derived	PP, NW, OD_33, RH, VAR, BJTDMY, PO, OD, RPO	Core device PLDD implantation.
19	NP	198	C	Derived	NP, SRM	N+ implantation.
20	PP	197	C	Derived	PP, SRM	P+ implantation.
21*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
22	RPO	155	D	29	-	Silicide protection.
23	CO	156	C	Derived	CO, CO_11, OD, SRAMDMY_4.	Contact window from M1 to OD or PO.
24	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
25	VIA1	378	C	51	-	Via1 hole between M2 and M1.
26	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
27	VIA2	379	C	52	-	Via2 hole between M3 and M2.
28	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
29	VIA3	373	C	53	-	Via3 hole between M4 and M3.
30	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
31	VIA4	374	C	54	-	Via4 hole between M5 and M4.
32	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
33	VIA5	375	C	55	-	Via5 hole between M6 and M5.
34	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
35	VIA6	376	C	56	-	Via6 hole between M7 and M6.
36	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
37	VIA7	377	C	57	-	Via7 hole between M8 and M7.
38	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
39	VIA8	372	C	58	-	Via8 hole between M9 and M8.
40	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

41	CB	107	C	76	-	Passivation-1 open for bond pad.
42#	AP	307	D	Derived	CB	AP pad.
43	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

41	CB	107	C	169	-	Passivation-1 open for bond pad.
42	AP	307	D	74	-	Al pad.
43	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

41	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
42	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
43*	FW_AP	30A	C	95;20	-	AP fuse window.
44	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

41	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
42	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
43*	FW_AP	30A	C	95;20	-	AP fuse window.
44	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.3 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN65G1.8V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	NW, NT_N	Core device and 1.8V P-Well.
4#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
5*	VTH_N	128	C	67	-	High Vt NMOS implantation.
6#	NW1V	192	C	Derived	NW, NT_N	Core device and 1.8V N-Well.
7#	VTC_P	199	C	Derived	SRM, NW	SRAM cell PMOS Vt.
8*	VTH_P	127	C	68	-	High Vt PMOS implantation.
9	OD2	152	D	16	-	1.8V thick oxide for DGO process.
10#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
11	PO	130	D	Derived	PO, OD, OD_18, NP, PP, SRM, FUSELINK, DPO	Poly-Si.
12#	N2V	116	C	Derived	NP, NW, OD_18, RH, VAR, NT_N, POFUSE, PO, RPO, OD	1.8V NLDD implantation.
13#	P2V	115	C	Derived	PP, NW, OD_18, RH, VAR, PO, RPO, OD	1.8V PLDD implantation.
14#	N1V	114	C	Derived	NP, NW, OD_18, RH, VAR, POFUSE, BJTDMY, PO, RPO, OD	Core device NLDD implantation.
15#	P1V	113	C	Derived	PP, NW, OD_18, RH, VAR, BJTDMY, PO, RPO, OD	Core device PLDD implantation.
16	NP	198	C	Derived	NP, SRM	N+ implantation.
17	PP	197	C	Derived	PP, SRM	P+ implantation.
18*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
19	RPO	155	D	29	-	Silicide protection.
20	CO	156	C	Derived	CO, CO_11, OD, SRAMDMY_5, SRAMDMY_5.	Contact window from M1 to OD or PO.
21	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
22	VIA1	378	C	51	-	Via1 hole between M2 and M1.
23	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
24	VIA2	379	C	52	-	Via2 hole between M3 and M2.
25	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
26	VIA3	373	C	53	-	Via3 hole between M4 and M3.
27	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
28	VIA4	374	C	54	-	Via4 hole between M5 and M4.
29	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
30	VIA5	375	C	55	-	Via5 hole between M6 and M5.
31	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
32	VIA6	376	C	56	-	Via6 hole between M7 and M6.
33	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
34	VIA7	377	C	57	-	Via7 hole between M8 and M7.
35	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
36	VIA8	372	C	58	-	Via8 hole between M9 and M8.
37	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

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FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

38	CB	107	C	76	-	Passivation-1 open for bond pad.
39#	AP	307	D	Derived	CB	Al pad.
40	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

38	CB	107	C	169	-	Passivation-1 open for bond pad.
39	AP	307	D	74	-	Al pad.
40	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

38	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, Al RDL via and Al fuse trench.
39	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
40*	FW_AP	30A	C	95;20	-	AP fuse window.
41	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

38	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
39	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
40*	FW_AP	30A	C	95;20	-	AP fuse window.
41	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.4 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN65G2.5V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	OD_25, NW, NT_N	Core device P-Well.
4#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
5#	PW2V	193	C	Derived	OD_25, NW, NT_N	2.5V P-Well.
6*	VTH_N	128	C	67	-	High Vt NMOS implantation.
7#	NW1V	192	C	Derived	NW, NT_N	Core device and 2.5V N-Well.
8#	VTC_P	199	C	Derived	SRM, NW	SRAM cell PMOS Vt.
9*	VTH_P	127	C	68	-	High Vt PMOS implantation.
10	OD2	152	D	18	-	2.5V thick oxide for DGO process.
11#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
12	PO	130	D	Derived	PO, OD, OD_25, NP, PP, SRM, FUSELINK, DPO	Poly-Si.
13#	N2V	116	C	Derived	NP, NW, OD_25, RH, VAR, NT_N, POFUSE, PO, RPO, OD	2.5V NLDD implantation.
14#	P2V	115	C	Derived	PP, NW, OD_25, RH, VAR, PO, RPO, OD	2.5V PLDD implantation.
15#	N1V	114	C	Derived	NP, NW, OD_25, RH, VAR, POFUSE, BJTDMY, PO, RPO, OD	Core device NLDD implantation.
16#	P1V	113	C	Derived	PP, NW, OD_25, RH, VAR, BJTDMY, PO, RPO, OD	Core device PLDD implantation.
17	NP	198	C	Derived	NP, SRM	N+ implantation.
18	PP	197	C	Derived	PP, SRM	P+ implantation.
19*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
20	RPO	155	D	29	-	Silicide protection.
21	CO	156	C	Derived	CO, CO_11, OD, SRAMDMY_4 SRAMDMY_5.	Contact window from M1 to OD or PO.
22	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
23	VIA1	378	C	51	-	Via1 hole between M2 and M1.
24	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
25	VIA2	379	C	52	-	Via2 hole between M3 and M2.
26	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
27	VIA3	373	C	53	-	Via3 hole between M4 and M3.
28	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
29	VIA4	374	C	54	-	Via4 hole between M5 and M4.
30	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
31	VIA5	375	C	55	-	Via5 hole between M6 and M5.
32	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
33	VIA6	376	C	56	-	Via6 hole between M7 and M6.
34	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
35	VIA7	377	C	57	-	Via7 hole between M8 and M7.
36	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
37	VIA8	372	C	58	-	Via8 hole between M9 and M8.
38	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

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FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

39	CB	107	C	76	-	Passivation-1 open for bond pad.
40#	AP	307	D	Derived	CB	Al pad.
41	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

39	CB	107	C	169	-	Passivation-1 open for bond pad.
40	AP	307	D	74	-	Al pad.
41	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

39	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, Al RDL via and Al fuse trench.
40	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
41*	FW_AP	30A	C	95;20	-	AP fuse window.
42	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

39	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and Al fuse trench.
40	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
41*	FW_AP	30A	C	95;20	-	AP fuse window.
42	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.5 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN65GP1.8V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	OD_18, NW, NT_N	Core device and 1.8V P-Well.
4#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
5*	VTL_N	118	C	Derived	OD_18, NW, NT_N, VTL_N	Low Vt NMOS implantation
6#	PW2V	193	C	Derived	OD_18, NW, NT_N	1.8V P-Well
7*	VTH_N	128	C	67	-	High Vt NMOS implantation.
8#	NW1V	192	C	Derived	NW, NT_N	Core device and 1.8 N-Well.
9#	VTC_P	199	C	Derived	SRM, NW	SRAM cell PMOS Vt.
10*	VTL_P	117	C	Derived	OD_18, NW, NT_N, VTL_P	Low Vt PMOS implantation
11*	VTH_P	127	C	68	-	High Vt PMOS implantation.
12	OD2	152	D	16	-	1.8V thick oxide for DGO process.
13#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
14#	NPO2	14A	C	Derived	PP, NW, OD_18, RH, VAR, SRM, BJTDMY, PO, RPO, OD	NPO2 process
15	PO	130	D	Derived	PO, OD, OD_18, NP, PP, SRM, FUSELINK DPO	Poly-Si.
16#	N2V	116	C	Derived	NP, NW, OD_18, RH, VAR, NT_N, POFUSE, PO, RPO, OD, BJTDMY	1.8V NLDD implantation.
17#	P2V	115	C	Derived	PP, NW, OD_18, RH, VAR, PO, RPO, OD, POFUSE, BJTDMY	1.8V PLDD implantation.
18#	N1V	114	C	Derived	NP, NW, OD_18, RH, VAR, POFUSE, PO, RPO, OD	Core device NLDD implantation.
19#	P1V	113	C	Derived	PP, NW, OD_18, RH, VAR, BJTDMY, PO, RPO, OD	Core device PLDD implantation.
20	PP	197	C	Derived	PP, SRM	P+ implantation.
21#	VTC_N	112	C	Derived	NW, SRM	DSD implantation.
22	NP	198	C	Derived	NP, SRM	N+ implantation.
23*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
24#	RPO2	124	C	Derived	PP, SRM, NW, OD_18,RH, VAR, BJTDMY, PP, RPO	RPO2 process
25	RPO	155	D	29	-	Silicide protection.
26	CO	156	C	Derived	CO, CO_11, OD, SRAMDMY_4.	Contact window from M1 to OD or PO.
27	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
28	VIA1	378	C	51	-	Via1 hole between M2 and M1.
29	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
30	VIA2	379	C	52	-	Via2 hole between M3 and M2.
31	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
32	VIA3	373	C	53	-	Via3 hole between M4 and M3.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
33	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
34	VIA4	374	C	54	-	Via4 hole between M5 and M4.
35	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
36	VIA5	375	C	55	-	Via5 hole between M6 and M5.
37	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
38	VIA6	376	C	56	-	Via6 hole between M7 and M6.
39	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
40	VIA7	377	C	57	-	Via7 hole between M8 and M7.
41	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
42	VIA8	372	C	58	-	Via8 hole between M9 and M8.
43	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

42	CB	107	C	76	-	Passivation-1 open for bond pad.
43#	AP	307	D	Derived	CB	Al pad.
44	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

42	CB	107	C	169	-	Passivation-1 open for bond pad.
43	AP	307	D	74	-	AP pad.
44	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

42	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
43	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
44*	FW_AP	30A	C	95;20	-	AP fuse window.
45	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

42	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
43	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
44*	FW_AP	30A	C	95;20	-	AP fuse window.
45	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.6 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN65GP2.5V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	OD_25, NW, NT_N	Core device P-Well.
4#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
5*	VTL_N	118	C	Derived	OD_25, NW, NT_N, VTL_N	Low Vt NMOS implantation for LP only.
6#	PW2V	193	C	Derived	OD_25, NW, NT_N	2.5V P-Well.
7*	VTH_N	128	C	67	-	High Vt NMOS implantation.
8#	NW1V	192	C	Derived	NW, NT_N	Core device and 2.5V N-Well.
9#	VTC_P	199	C	Derived	SRM, NW	SRAM cell PMOS Vt.
10*	VTL_P	117	C	Derived	OD_25, NW, NT_N, VTL_P	Low Vt PMOS implantation for LP only.
11*	VTH_P	127	C	68	-	High Vt PMOS implantation.
12	OD2	152	D	18	-	2.5V thick oxide for DGO process.
13#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
14#	NPO2	14A	C	Derived	PP, NW, OD_25, RH, VAR, SRM, BJTDMY, PO, RPO, OD	NPO2 process
15	PO	130	D	Derived	PO, OD, OD_25, NP, PP, SRM, FUSELINK, DPO	Poly-Si.
16#	N2V	116	C	Derived	NP, NW, OD_25, RH, PO, RPO, OD, VAR, NT_N, POFUSE, BJTDMY	2.5V NLDD implantation.
17#	P2V	115	C	Derived	PP, NW, OD_25, RH, PO, RPO, OD, VAR, BJTDMY, POFUSE	2.5V PLDD implantation.
18#	N1V	114	C	Derived	NP, NW, OD_25, RH, PO, RPO, OD, VAR, POFUSE , BJTDMY	Core device NLDD implantation.
19#	P1V	113	C	Derived	PP, NW, OD_25, RH, PO, RPO, OD, VAR, BJTDMY	Core device PLDD implantation.
20	PP	197	C	Derived	PP, SRM	P+ implantation.
21#	VTC_N	112	C	Derived	SRM, NW	DSD implantation.
22	NP	198	C	Derived	NP, SRM	N+ implantation.
23*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
24#	RPO2	124	C	Derived	PP, SRM, NW, OD_25, RH, VAR, BJTDMY, PO, RPO	RPO2 process
25	RPO	155	D	29	-	Silicide protection.
26	CO	156	C	Derived	CO, CO_11, OD, SRAMDMY_4, SRAMDMY_5.	Contact window from M1 to OD or PO.
27	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
28	VIA1	378	C	51	-	Via1 hole between M2 and M1.
29	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
30	VIA2	379	C	52	-	Via2 hole between M3 and M2.
31	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
32	VIA3	373	C	53	-	Via3 hole between M4 and M3.
33	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
34	VIA4	374	C	54	-	Via4 hole between M5 and M4.
35	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
36	VIA5	375	C	55	-	Via5 hole between M6 and M5.
37	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
38	VIA6	376	C	56	-	Via6 hole between M7 and M6.
39	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
40	VIA7	377	C	57	-	Via7 hole between M8 and M7.
41	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
42	VIA8	372	C	58	-	Via8 hole between M9 and M8.
43	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

44	CB	107	C	76	-	Passivation-1 open for bond pad.
45#	AP	307	D	Derived	CB	Al pad.
46	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

44	CB	107	C	169	-	Passivation-1 open for bond pad.
45	AP	307	D	74	-	Al pad.
46	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

44	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
45	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
46*	FW_AP	30A	C	95;20	-	AP fuse window.
47	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

44	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
45	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
46*	FW_AP	30A	C	95;20	-	AP fuse window.
47	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.7 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN65LPG 2.5V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, NW, SRM	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	DNW	Deep N-Well.
3#	PW1V	191	D	Derived	OD_25, NW, NT_N, DCO	LP cCore device P-Well.
4#	PW1V_DCO	11J	C	Derived	OD_25, NW, NT_N, DCO	LP NMOS Vt
5*#	VTC_N	112	C	Derived	SRM, NW, DCO, VTH_N	LP SRAM cell NMOS Vt.
6#	PW2V	193	C	Derived	OD_25, NW, NT_N, DCO	2.5V P-Well.
7*	VTH_N	128	C	Derived	VTH_N, NW, SRM, DCO	High Vt NMOS and G SRAM cell NMOS implantation.
8#	NW1V	192	C	Derived	OD_25, NW, NT_N	2.5V and cCore device N-Well..
9*	VTH_P	127	C	Derived	VTH_P, NW, SRM, DCO	High Vt PMOS and G SRAM cell PMOS implantation..
10	OD2	152	D	Derived	OD_25, DCO	2.5V thick oxide and G core oxide
11	OD3	153	C	90	DCO	G core oxide
12#	NPO	196	C	Derived	NP, SRM, POFUSE	Pre-doped N+ poly.
13	PO	130	D	Derived	PO, OD, OD_25, NP, PP, SRM, DCO, DPO, SRAMDMY;1, MVTL, FUSELINK	Poly-Si.
14#	N2V	116	C	Derived	NP, NW, OD_25, RH, VAR, NT_N, POFUSE, DCO, PO, OD, RPO	2.5V NLDD implantation.
15#	P2V	115	C	Derived	PP, NW, OD_25, RH, VAR, DCO, PO, OD, RPO	2.5V PLDD implantation.
16#	N1V	114	C	Derived	NP, NW, OD_25, RH, VAR, POFUSE, PO, OD, RPO, BJTDMY	LP Core device NLDD implantation.
17#	N1V_DCO	106	C	Derived	NP, NW, OD_25, RH, VAR, DCO, PO, OD, RPO, BJTDMY	G core device NLDD implantation.
18#	P1V_DCO	105	C	Derived	PP, NW, OD_25, RH, VAR, DCO, PO, OD, RPO, BJTDMY	G core device PLDD implantation.
19#	P1V	113	C	Derived	PP, NW, OD_25, RH, VAR, DCO, PO, OD, RPO, BJTDMY	LP core device PLDD implantation.
20	NP	198	C	Derived	NP, SRM	N+ implantation.
21	PP	197	C	Derived	PP, SRM	P+ implantation.
22*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
23	RPO	155	D	29	RPO	Silicide protection.
24	CO	156	C	Derived	CO, CO_;11, SRAMDMY_;4.	Contact window from M1 to OD or PO.
25	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
26	V1	378	C	51	V1	Via1 hole between M2 and M1.
27	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
28	V2	379	C	52	V2	Via2 hole between M3 and M2.
29	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
30	V3	373	C	53	V3	Via3 hole between M4 and M3.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
31	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
32	V4	374	C	54	V4	Via4 hole between M5 and M4.
33	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
34	V5	375	C	55	V5	Via5 hole between M6 and M5.
35	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
36	V6	376	C	56	V6	Via6 hole between M7 and M6.
37	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
38	V7	377	C	57	V7	Via7 hole between M8 and M7.
39	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
40	V8	372	C	58	V8	Via8 hole between M9 and M8.
41	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

42	CB	107	C	76	-	Passivation-1 open for bond pad.
43#	AP	307	D	Derived	CB	AP pad.
44	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

42	CB	107	C	169	-	Passivation-1 open for bond pad.
43	AP	307	D	74	-	AP pad.
44	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

42	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
43	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
44*	FW_AP	30A	C	95;20	-	AP fuse window.
45	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

42	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
43	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
44*	FW_AP	30A	C	95;20	-	AP fuse window.
45	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.8 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN65ULP2.5V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	OD_25, NW, NT_N	Core device P-Well.
4#	PW2V	193	C	Derived	OD_25, NW, NT_N	2.5V P-Well.
5*	VTL_N	118	C	Derived	OD_25, NW, NT_N, VTL_N	Low Vt NMOS implantation
6*	VTH_N	128	C	67	-	High Vt NMOS implantation.
7#	NW1V	192	C	Derived	NW, NT_N	Core device and 2.5V N-Well.
8*	VTL_P	117	C	Derived	OD_25, NW, NT_N, VTL_P	Low Vt PMOS implantation
9*	VTH_P	127	C	68	-	High Vt PMOS implantation.
10	OD2	152	D	18	-	2.5V thick oxide for DGO process.
11#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
12	PO	130	D	Derived	PO, OD, OD_25, NP, PP, SRM, mVTL, DPO	Poly-Si.
13#	N2V	116	C	Derived	NP, NW, OD_25, RH, VAR, NT_N, POFUSE, PO, OD, RPO	2.5V NLDD implantation.
14#	P2V	115	C	Derived	PP, NW, OD_25, RH, VAR, PO, OD, RPO	2.5V PLDD implantation.
15#	N1V	114	C	Derived	NP, NW, OD_25, RH, VAR, POFUSE, BJTDMY, PO, OD, RPO, SRM	Core device NLDD implantation.
16*#	VTC_N	112	C	Derived	NP, NW, OD_18, RH, VAR, POFUSE, BJTDMY, OD, PO, RPO, SRM	ULP SRAM Device NLDD implantation.
17#	P1V	113	C	Derived	PP, NW, OD_25, RH, VAR, BJTDMY, PO, OD, RPO	Core device PLDD implantation.
18	NP	198	C	Derived	NP, SRM	N+ implantation.
19	PP	197	C	Derived	PP, SRM	P+ implantation.
20*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
21	RPO	155	D	29	-	Silicide protection.
22	CO	156	C	Derived	CO, CO_11, OD, SRAMDMY_4.	Contact window from M1 to OD or PO.
23	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
24	VIA1	378	C	51	-	Via1 hole between M2 and M1.
25	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
26	VIA2	379	C	52	-	Via2 hole between M3 and M2.
27	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
28	VIA3	373	C	53	-	Via3 hole between M4 and M3.
29	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
30	VIA4	374	C	54	-	Via4 hole between M5 and M4.
31	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
32	VIA5	375	C	55	-	Via5 hole between M6 and M5.
33	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
34	VIA6	376	C	56	-	Via6 hole between M7 and M6.
35	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
36	VIA7	377	C	57	-	Via7 hole between M8 and M7.
37	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
38	VIA8	372	C	58	-	Via8 hole between M9 and M8.
39	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

40	CB	107	C	76	-	Passivation-1 open for bond pad.
41#	AP	307	D	Derived	CB	Al pad.
42	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

40	CB	107	C	169	-	Passivation-1 open for bond pad.
41	AP	307	D	74	-	Al pad.
42	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

40	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
41	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
42*	FW_AP	30A	C	95;20	-	AP fuse window.
43	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

40	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
41	AP-MD	309	D	74	-	Al pad, AP RDL, Al fuse.
42*	FW_AP	30A	C	95;20	-	AP fuse window.
43	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.9 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN55GP1.8V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	OD_18, NW, NT_N	Core device P-Well.
4#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
5#	PW2V	193	C	Derived	OD_18, NW, NT_N	1.8V P-Well.
6*	VTL_N	118	C	Derived	OD_18, NW, NT_N, VTL_N	Low Vt NMOS implantation
7*	VTH_N	128	C	67	-	High Vt NMOS implantation.
8#	NW1V	192	C	Derived	NW, NT_N	Core device and 1.8 N-Well.
9*	VTL_P	117	C	Derived	OD_18, NW, NT_N, VTL_P	Low Vt PMOS implantation
10*	VTH_P	127	C	68	-	High Vt PMOS implantation.
11	OD2	152	D	16	-	1.8V thick oxide for DGO process.
12#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
13	PO	130	D	Derived	PO, OD, OD_18, NP, PP, SRM, DPO SRAMDMY_1	Poly-Si.
14#	N2V	116	C	Derived	NP, NW, OD_18, RH, VAR, NT_N, POFUSE, BJTDMY	1.8V NLDD implantation.
15#	P2V	115	C	Derived	PP, NW, OD_18, RH, VAR, BJTDMY	1.8V PLDD implantation.
16#	N1V	114	C	Derived	NP, NW, OD_18, RH, VAR, POFUSE, BJTDMY	Core device NLDD implantation.
17#	P1V	113	C	Derived	PP, NW, OD_18, RH, VAR, BJTDMY	Core device PLDD implantation.
18	NP	198	C	Derived	NP, SRM	N+ implantation.
19	PP	197	C	Derived	PP, SRM	P+ implantation.
20*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
21#	NPO2	14A	C	Derived	PP, NW, OD_18, RH, VAR, SRM, BJTDMY	Device tuning implantation
22#	RPO2	124	C	Derived	SRM, NW, OD_18,RH, VAR, BJTDMY	RPO2 etch
23	RPO	155	D	Derived	PO, RPO, OD	Silicide protection.
24	CO	156	C	Derived	CO, CO_11, OD, SRAMDMY_4.	Contact window from M1 to OD or PO.
25	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
26	VIA1	378	C	51	-	Via1 hole between M2 and M1.
27	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
28	VIA2	379	C	52	-	Via2 hole between M3 and M2.
29	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
30	VIA3	373	C	53	-	Via3 hole between M4 and M3.
31	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
32	VIA4	374	C	54	-	Via4 hole between M5 and M4.
33	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
34	VIA5	375	C	55	-	Via5 hole between M6 and M5.
35	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
36	VIA6	376	C	56	-	Via6 hole between M7 and M6.
37	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
38	VIA7	377	C	57	-	Via7 hole between M8 and M7.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
39	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
40	VIA8	372	C	58	-	Via8 hole between M9 and M8.
41	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

42	CB	107	C	76	-	Passivation-1 open for bond pad.
43#	AP	307	D	Derived	CB	Al pad.
44	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

42	CB	107	C	169	-	Passivation-1 open for bond pad.
43	AP	307	D	74	-	Al pad.
44	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

42	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
43	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
44*	FW_AP	30A	C	95;20	-	AP fuse window.
45	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

42	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
43	AP-MD	309	D	74	-	Al pad, AP RDL, Al fuse.
44*	FW_AP	30A	C	95;20	-	AP fuse window.
45	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.10 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN55GP2.5V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	OD_25, NW, NT_N	Core device P-Well.
4#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
5#	PW2V	193	C	Derived	OD_25, NW, NT_N	2.5V P-Well.
6*	VTL_N	118	C	Derived	OD_25, NW, NT_N, VTL_N	Low Vt NMOS implantation
7*	VTH_N	128	C	67	-	High Vt NMOS implantation.
8#	NW1V	192	C	Derived	NW, NT_N	Core device and 2.5V N-Well.
9*	VTL_P	117	C	Derived	OD_25, NW, NT_N, VTL_P	Low Vt PMOS implantation
10*	VTH_P	127	C	68	-	High Vt PMOS implantation.
11	OD2	152	D	18	-	2.5V thick oxide for DGO process.
12#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
13	PO	130	D	Derived	PO, OD, OD_25, NP, PP, SRM, DPO SRAMDMY_1, OD25_33	Poly-Si.
14#	N2V	116	C	Derived	NP, NW, OD_25, RH, VAR, NT_N, POFUSE, BJTDMY	2.5V NLDD implantation.
15#	P2V	115	C	Derived	PP, NW, OD_25, RH, VAR, BJTDMY	2.5V PLDD implantation.
16#	N1V	114	C	Derived	NP, NW, OD_25, RH, VAR, POFUSE, BJTDMY	Core device NLDD implantation.
17#	P1V	113	C	Derived	PP, NW, OD_25, RH, VAR, BJTDMY	Core device PLDD implantation.
18	NP	198	C	Derived	NP, SRM	N+ implantation.
19	PP	197	C	Derived	PP, SRM	P+ implantation.
20*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
21#	NPO2	14A	C	Derived	PP, NW, OD_25, RH, VAR, SRM, BJTDMY	Device tuning implantation
22#	RPO2	124	C	Derived	SRM, NW, OD_25,RH, VAR, BJTDMY	RPO2 etch
23	RPO	155	D	Derived	RPO, OD, PO	Silicide protection.
24	CO	156	C	Derived	CO, CO_11, SRAMDMY_4.	Contact window from M1 to OD or PO.
25	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
26	VIA1	378	C	51	-	Via1 hole between M2 and M1.
27	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
28	VIA2	379	C	52	-	Via2 hole between M3 and M2.
29	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
30	VIA3	373	C	53	-	Via3 hole between M4 and M3.
31	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
32	VIA4	374	C	54	-	Via4 hole between M5 and M4.
33	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
34	VIA5	375	C	55	-	Via5 hole between M6 and M5.
35	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
36	VIA6	376	C	56	-	Via6 hole between M7 and M6.
37	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
38	VIA7	377	C	57	-	Via7 hole between M8 and M7.
39	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
40	VIA8	372	C	58	-	Via8 hole between M9 and M8.
41	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

42	CB	107	C	76	-	Passivation-1 open for bond pad.
43#	AP	307	D	Derived	CB	Al pad.
44	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

42	CB	107	C	169	-	Passivation-1 open for bond pad.
43	AP	307	D	74	-	Al pad.
44	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

42	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
43	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
44*	FW_AP	30A	C	95;20	-	AP fuse window.
45	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

42	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
43	AP-MD	309	D	74	-	Al pad, AP RDL, Al fuse.
44*	FW_AP	30A	C	95;20	-	AP fuse window.
45	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.11 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN55GP3.3V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, SRM, NP, NW, PP, DOD	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	NW, SRM, NT_N, OD_33,	Core device P-Well.
4#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
5*	VTL_N	118	C	Derived	NW, OD_33, NT_N, VTL_N	Low Vt NMOS implantation
6#	PW2V	193	C	Derived	OD_33, NW, NT_N	3.3V P-Well.
7*	VTH_N	128	C	67	-	High Vt NMOS implantation.
8#	NW1V	192	C	Derived	NW, NT_N, OD_33, SRM,	Core device NW
9*	VTL_P	117	C	Derived	OD_33, NW, NT_N, VTL_P	Low Vt PMOS implantation
10#	NW2V	194	C	Derived	NW, OD_33, SRM	3.3V N-Well.
11*	VTH_P	127	C	68	-	High Vt PMOS implantation.
12	OD2	152	D	15	-	2.5V thick oxide for DGO process.
13#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
14	PO	130	D	Derived	PO, OD, OD_33, NP, PP, SRM, FUSELINK, DPO SRAMDMY_1,	Poly-Si.
15#	N2V	116	C	Derived	NP, NW, OD_33, RH, PO, RPO, OD, VAR, NT_N, POFUSE, BJTDMY	2.5V NLDD implantation.
16#	P2V	115	C	Derived	PP, NW, OD_33, RH, PO, RPO, OD, VAR, NT_N, POFUSE, BJTDMY	2.5V PLDD implantation.
17#	N1V	114	C	Derived	NP, NW, OD_33, RH, PO, RPO, OD, VAR, POFUSE, BJTDMY, SRM	Core device NLDD implantation.
18#	P1V	113	C	Derived	PP, NW, OD_33, RH, PO, RPO, OD, VAR, POFUSE, BJTDMY, SRM	Core device PLDD implantation.
19	NP	198	C	Derived	NP, SRM	N+ implantation.
20	PP	197	C	Derived	PP, SRM	P+ implantation.
21*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
22#	NPO2	14A	C	Derived	NP, NW, OD_33, RH, PO, RPO, OD, VAR, BJTDMY, SRM	Device tuning implantation
23#	RPO2	124	C	Derived	PP, NW, OD_33, RH, PO, RPO, OD, VAR, BJTDMY, SRM	RPO2 etch
24	RPO	155	D	Derived	PO, RPO, OD	Silicide protection.
25	CO	156	C	Derived	CO, SRM, CO_11, SRAMDMY_4, NW, NP, PP, SRM_12, SRM_13, SRM_14,	Contact window from M1 to OD or PO.
26	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
27	VIA1	378	C	51	-	Via1 hole between M2 and M1.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
28	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
29	VIA2	379	C	52	-	Via2 hole between M3 and M2.
30	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
31	VIA3	373	C	53	-	Via3 hole between M4 and M3.
32	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
33	VIA4	374	C	54	-	Via4 hole between M5 and M4.
34	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
35	VIA5	375	C	55	-	Via5 hole between M6 and M5.
36	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
37	VIA6	376	C	56	-	Via6 hole between M7 and M6.
38	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
39	VIA7	377	C	57	-	Via7 hole between M8 and M7.
40	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
41	VIA8	372	C	58	-	Via8 hole between M9 and M8.
42	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

43	CB	107	C	76	-	Passivation-1 open for bond pad.
44#	AP	307	D	Derived	CB	Al pad.
45	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

43	CB	107	C	169	-	Passivation-1 open for bond pad.
44	AP	307	D	74	-	Al pad.
45	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

43	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
44	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
45*	FW_AP	30A	C	95;20	-	AP fuse window.
46	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

43	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
44	AP-MD	309	D	74	-	Al pad, AP RDL, Al fuse.
45*	FW_AP	30A	C	95;20	-	AP fuse window.
46	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.12 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN55LP2.5V

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD, SRM, NW	Device, ACTIVE, STRAP and interconnection regions.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	OD_25, NW, NT_N	Core device P-Well.
4#	PW2V	193	C	Derived	OD_25, NW, NT_N	2.5V P-Well.
5*	VTL_N	118	C	Derived	OD_25, NW, NT_N, VTL_N	Low Vt NMOS implantation for LP only.
6*	VTH_N	128	C	67	-	High Vt NMOS implantation.
7#	NW1V	192	C	Derived	NW, NT_N	Core device and 2.5V N-Well.
8*	VTL_P	117	C	Derived	OD_25, NW, NT_N, VTL_P	Low Vt PMOS implantation for LP only.
9*	VTH_P	127	C	68	-	High Vt PMOS implantation.
10	OD2	152	D	18	-	2.5V thick oxide for DGO process.
11#	NPO	196	C	Derived	NP, SRM, POFUSE, NW	Pre-doped N+ poly.
12	PO	130	D	Derived	PO, OD, OD_25, NP, PP, SRM, mVTL, DPO	Poly-Si.
13#	N2V	116	C	Derived	NP, NW, OD_25, RH, VAR, NT_N, POFUSE, PO, OD, RPO	2.5V NLDD implantation.
14#	P2V	115	C	Derived	PP, NW, OD_25, RH, VAR, PO, OD, RPO	2.5V PLDD implantation.
15*#	VTC_N	112	C	Derived	SRM, SRM_11, SRM_12, NW, VTH_N	SRAM NLDD implantation
16#	N1V	114	C	Derived	NP, NW, OD_25, RH, VAR, POFUSE, BJTDMY, PO, OD, RPO	Core device NLDD implantation.
17#	P1V	113	C	Derived	PP, NW, OD_25, RH, VAR, BJTDMY, PO, OD, RPO	Core device PLDD implantation.
18	NP	198	C	Derived	NP, SRM	N+ implantation.
19	PP	197	C	Derived	PP, SRM	P+ implantation.
20*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
21	RPO	155	D	29	-	Silicide protection.
22	CO	156	C	Derived	CO, CO_11, OD, SRAMDMY_4.	Contact window from M1 to OD or PO.
23	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
24	VIA1	378	C	51	-	Via1 hole between M2 and M1.
25	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
26	VIA2	379	C	52	-	Via2 hole between M3 and M2.
27	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
28	VIA3	373	C	53	-	Via3 hole between M4 and M3.
29	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
30	VIA4	374	C	54	-	Via4 hole between M5 and M4.
31	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
32	VIA5	375	C	55	-	Via5 hole between M6 and M5.
33	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
34	VIA6	376	C	56	-	Via6 hole between M7 and M6.
35	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
36	VIA7	377	C	57	-	Via7 hole between M8 and M7.
37	M8	388	C	Derived	M8, DM8	8th metal for interconnection.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
38	VIA8	372	C	58	-	Via8 hole between M9 and M8.
39	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

40	CB	107	C	76	-	Passivation-1 open for bond pad.
41#	AP	307	D	Derived	CB	Al pad.
42	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

40	CB	107	C	169	-	Passivation-1 open for bond pad.
41	AP	307	D	74	-	Al pad.
42	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

40	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
41	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
42*	FW_AP	30A	C	95;20	-	AP fuse window.
43	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

40	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
41	AP-MD	309	D	74	-	Al pad, AP RDL, Al fuse.
42*	FW_AP	30A	C	95;20	-	AP fuse window.
43	CB2	308	C	86	-	Passivation-2 open.

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Table 3.1.13 Mask Name and ID, Key Process Sequence, and CAD Layer for CMN65/CMN55:

- The following tables provide the N65/N55 backend process mask sequence with additional information regarding CTM/CBM of N65 or Mu mask of N65/N55.
- **Mu (UTM: 34KÅ) is only allowed as the most top metal layer. (Only one Mu layer is allowed in a chip.) Mu cannot co-exist with other different thickness top metal layer(s) (such as Mz, My or Mr) on the same metal layer.**
- **For the Mu adopted INDDMY inductor design, please refer to the section 4.6.7**

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	M1	360	C	Derived	M1, DM1, DM1_O	1st metal for interconnection.
2	VIA1	378	C	51	-	Via1 hole between M2 and M1.
3	M2	380	C	Derived	M2, DM2, DM2_O	2nd metal for interconnection.
4	VIA2	379	C	52	-	Via2 hole between M3 and M2.
5	M3	381	C	Derived	M3, DM3, DM3_O	3rd metal for interconnection.
6	VIA3	373	C	53	-	Via3 hole between M4 and M3.
7	M4	384	C	Derived	M4, DM4, DM4_O	4th metal for interconnection.
8	VIA4	374	C	54	-	Via4 hole between M5 and M4.
9	M5	385	C	Derived	M5, DM5, DM5_O	5th metal for interconnection.
10	VIA5	375	C	55	-	Via5 hole between M6 and M5.
11	M6	386	C	Derived	M6, DM6, DM6_O	6th metal for interconnection.
12	VIA6	376	C	56	-	Via6 hole between M7 and M6.
13	M7	387	C	Derived	M7, DM7, DM7_O	7th metal for interconnection.
14	CTM@	182	D	77	-	CAPACITOR TOP METAL
15	CBM@	183	D	88	-	CAPACITOR BOTTOM METAL
16	VIA7	377	C	57	-	Via7 hole between M8 and M7.
17	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
18	VIA8	372	C	58	-	Via8 hole between M9 and M8.
19	M9	389	C	Derived	M9, DM9	9th metal for interconnection.
				Derived	Mu, DMu	Ultra thick metal for inductor/ interconnection

FBEOL option1 (Wire bond without (AP Fuse or AP RDL))

20	CB	107	C	76	-	Passivation-1 open for bond pad.
21#	AP	307	D	Derived	CB	Al pad.
22	CB	107	C	76	-	Passivation-2 open for bond pad.

FBEOL option2 (Flip chip without (AP Fuse or AP RDL))

20	CB	107	C	169	-	Passivation-1 open for bond pad.
21	AP	307	D	74	-	Al pad.
22	CB	107	C	169	-	Passivation-2 open for bond pad.

FBEOL option3 (Wire bond with (AP Fuse or AP RDL))

20	CB-VD	306	C	Derived	CB, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
21	AP-MD	309	D	74	-	Al pad, AP RDL, AP fuse.
22*	FW_AP	30A	C	95;20	-	AP fuse window.
23	CB2	308	C	86	-	Passivation-2 open.

FBEOL option4 (Flip chip with (AP Fuse or AP RDL))

20	CB-VD	306	C	Derived	CBD, RV, FW	Passivation-1 open for bond pad, AP RDL via and AP fuse trench.
21	AP-MD	309	D	74	-	Al pad, AP RDL, Al fuse.
22*	FW_AP	30A	C	95;20	-	AP fuse window.
23	CB2	308	C	86	-	Passivation-2 open.

Note: The mark " @ " is for CTM/CBM placement of CMN65 and can refer to Table 2.5.6, 2.5.7 and 2.5.8

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Table 3.1.14 Mask Name/ID/Grade/Type, OPC, and PSM Information.

Mask Name	Mask ID	Mask Grade	Mask Type	OPC	PSM	Group	Non-design level mask
OD	120	K	ASF	A	C		
DNW	119	E	DSF	B	B		
PW1V	191	G	DSF	B	B		Yes
PW1V_DCO	11J	H	DSF	A	B		Yes
VTC_N	112	G	DSF	B	B		Yes
PW2V	193	G	DSF	B	B		Yes
VTL_N	118	H	DSF	A	B		
VTH_N	128	H	DSF	A	B		
NW1V	192	G	DSF	B	B		Yes
NW2V	194	G	DSF	B	B		Yes
VTC_P	199	G	DSF	B	B		Yes
VTL_P	117	H	DSF	A	B		
VTH_P	127	H	DSF	A	B		
OD2	152	E	DSF	B	B		
OD3	153	E	DSF	B	B		
NPO	196	H	DSF	A	B		Yes
NPO2	14A	H	DSF	A	B		Yes
PO	130	L	ASF	A	C		
N2V	116	H	DSF	A	B		Yes
P2V	115	H	DSF	A	B		Yes
VTC_N	112	G	DSF	B	B		Yes
N1V	114	H	DSF	A	B		Yes
N1V_DCO	106	H	DSF	A	B		Yes
P1V_DCO	105	H	DSF	A	B		Yes
P1V	113	H	DSF	A	B		Yes
NP	198	H	DSF	A	B		
PP	197	H	DSF	A	B		
ESD	111	E	DSF	B	B		Yes
RPO2	124	G	DSF	A	B		Yes
RPO	155	E (N65) F (N55)	DSF	B	B		
CO	156	K	ASF	A	C		
M1	360	K	ASF	A	C		
VIA1	378	J	ASF	A	C		
M2	380	J	ASF	A	B		
VIA2	379	J	ASF	A	C	VIAx	
		H	DSF	B	C	VIAy	
		F	DSF	B	B	VIAz	
M3	381	J	ASF	A	B	Mx	
		H	DSF	A	B	My	
		F	DSF	B	B	Mz	
VIA3	373	J	ASF	A	C	VIAx	
		H	DSF	B	C	VIAy	
		F	DSF	B	B	VIAz	
		F	DSF	B	B	VIAu	
M4	384	J	ASF	A	B	Mx	
		H	DSF	A	B	My	
		F	DSF	B	B	Mz	
		F	DSF	B	B	Mu	
VIA4	374	J	ASF	A	C	VIAx	
		H	DSF	B	C	VIAy	
		F	DSF	B	B	VIAz	
		F	DSF	B	B	VIAu	

TSMC Confidential Information
TSMC Confidential Information 833462 USCVISIVMOSIS 12/16/2016

Mask Name	Mask ID	Mask Grade	Mask Type	OPC	PSM	Group	Non-design level mask
M5	385	J	ASF	A	B	Mx	
		H	DSF	A	B	My	
		F	DSF	B	B	Mz	
		F	DSF	B	B	Mu	
VIA5	375	J	ASF	A	C	VIAx	
		H	DSF	B	C	VIAy	
		F	DSF	B	B	VIAz	
		F	DSF	B	B	VIAr	
		F	DSF	B	B	VIAu	
M6	386	J	ASF	A	B	Mx	
		H	DSF	A	B	My	
		F	DSF	B	B	Mz	
		F	DSF	B	B	Mr	
		F	DSF	B	B	Mu	
VIA6	376	J	ASF	A	C	VIAx	
		H	DSF	B	C	VIAy	
		F	DSF	B	B	VIAz	
		F	DSF	B	B	VIAr	
		F	DSF	B	B	VIAu	
M7	387	J	ASF	A	B	Mx	
		H	DSF	A	B	My	
		F	DSF	B	B	Mz	
		F	DSF	B	B	Mr	
		F	DSF	B	B	Mu	
VIA7	377	F	DSF	B	B	VIAz	
		H	DSF	B	C	VIAy	
		F	DSF	B	B	VIAr	
		F	DSF	B	B	VIAu	
CTM	182	G	DSF	B	B		
CBM	183	E	DSF	B	B		
M8	388	F	DSF	B	B	Mz	
		H	DSF	A	B	My	
		F	DSF	B	B	Mr	
		F	DSF	B	B	Mu	
VIA8	372	F	DSF	B	B	VIAz	
		H	DSF	B	C	VIAy	
		F	DSF	B	B	VIAr	
		F	DSF	B	B	VIAu	
M9	389	F	DSF	B	B	Mz	
		H	DSF	A	B	My	
		F	DSF	B	B	Mr	
		F	DSF	B	B	Mu	
CB	107	A	DSF	B	B		
CB-VD	306	D	DSF	B	B		
AP	307	A	DSF	B	B		Yes
AP-MD	309	D	DSF	B	B		
CB2	308	A	DSF	B	B		
FW_AP	30A	A	DSF	B	B		

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TSMC Confidential Information 833462 USCVISIVMOSIS 12/16/2016
833462 USCVISIVMOSIS 12/16/2016

Table 3.1.15

Category	Abbreviation	Description
Mask type:	DSF	DUV scanner
	ASF	193nm scanner
OPC:	B	Non-OPC (Binary)
	A	OPC
PSM:	B	Non-PSM (Binary)
	C	PSM

3.2 Metal/Via CAD Layer Information for Metallization Options

- **Due to the complexity of metallization schemes, Table 3.2.1 is the summary of TSMC metal/via CAD layer number, name, and datatype.**

  The labels “x”, "y", “z”, “r” denote different metal schemes and minimum pitches. “x” using datatype “0” is first inter-layer metal (Mx) with minimum pitch 0.2 μm. “y” using datatype “20” is second inter-layer metal (My) or 2x top layer metal (My) with minimum pitch 0.4 μm. “z” using datatype “40” is top layer metal (Mz) with minimum pitch 0.8 μm. “r” using datatype “80” is top layer metal (Mr) with minimum pitch 1.0 μm. The via datatype is the same as the metal right upon the via.

- **For any metal combination, a marker (1+A+B+C) M_AxByCz or (1+A+D)M_AxDr can be used to represent the metal combination of Mx, My, Mz, and Mr.**

  The marker is interpreted as one layer of M1, A layers of Mx, B layers of My, C layers of Mz and D layers of Mr. The total metal layer number is 1+A+B+C or 1+A+D. For example, a 7 metal layer process with one M1 layer, three Mx layers, one My layer and two Mz layers, can be denoted as 7M_3x1y2z.

Table 3.2.1 Metal CAD Layer Number, Name, and Datatype

Layer Name	CAD Layer #	Datatype				
		x	y	z	r	u
M1	31	0	-	-	-	
VIA1	51	0	-	-	-	
M2	32	0	-	-	-	
VIA2	52	0	20	40	-	
M3	33	0	20	40	-	
VIA3	53	0	20	40	-	40
M4	34	0	20	40	-	60
VIA4	54	0	20	40	-	40
M5	35	0	20	40	-	60
VIA5	55	0	20	40	80	40
M6	36	0	20	40	80	60
VIA6	56	0	20	40	80	40
M7	37	0	20	40	80	60
VIA7	57	-	20	40	80	40
M8	38	-	20	40	80	60
VIA8	58	-	20	40	80	40
M9	39	-	20	40	80	60

The following is the CAD layer/datatype example of a 7 metal layer process with one M1 layer, three Mx layers, one My layer and two Mz layers, which can be denoted as 7M_3x1y2z. The CAD layer designators are specified according to the format of GDS layer #; datatype.

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Table 3.2.2 CAD Layer/Datatype Example for 7M_3x1y2z

Process Sequence	CAD Layer #/Datatype
Metal-1	31; 0
Via-1	51; 0
Metal-2	32; 0
Via-2	52; 0
Metal-3	33; 0
Via-3	53; 0
Metal-4	34; 0
Via-4	54; 20
Metal-5	35; 20
Via-5	55; 40
Metal-6	36; 40
Via-6	56; 40
Metal-7	37; 40

3.3 Dummy Pattern Fill CAD Layers

The layers in Table 3.3.1 are for planarization (dummy fill) geometry, referring to Table 3.2.1

Table 3.3.1 Dummy Pattern CAD Layer Number, Name, and Datatype

Layer Name	CAD Layer #	Dummy Datatype				
		x	y	z	r	u
DOD	6	1	-	-	-	-
DPO	17	1	-	-	-	-
DM1	31	1, 7	-	-	-	-
DM2	32	1, 7	21	-	-	-
DM3	33	1, 7	21	41	-	-
DM4	34	1, 7	21	41	-	61
DM5	35	1, 7	21	41	-	61
DM6	36	1, 7	21	41	81	61
DM7	37	1, 7	21	41	81	61
DM8	38	-	21	41	81	61
DM9	39	-	21	41	81	61

Table notes:

Metal datatypes 1 (DMx) & 41 (DMz) are the dummy metals without receiving OPC. Datatypes 7 (DMx_O), which will be generated from TSMC metal dummy utility, will receive OPC same as main metal pattern. Please refer to the section 8.3 Dummy Metal Rules.

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3.4 Special Recognition CAD Layer Summary

Table 3.4.1 lists special layers used in CLN65 design rules and in DRC command files. These layers are used for CAD device recognition, and DRC waivers. Some CAD layer designators include a GDS datatype according to the GDS *layer;datatype* format.

The column "Tape out required layer" indicates that this layer must be noted on the mask tapeout to provide information for mask making.

Table 3.4.1 Special Layer Summary

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape out required layer
General					
NWDMY	114	NW resistor dummy layer for DRC and LVS. The NW region covered by both NWDMY and RPO layers is the "NW within OD resistor." The NW region covered by only NWDMY is the "NW under STI resistor."	NWROD and NWRSTI rules	✓	
Ncap_NTN	11;20	DRC needs NCap_NTN to waive the NMOS capacitors with same potential.	NT_N rules	✓	
OD25_33	18;3	DRC dummy layer for 2.5V thick oxide (second gate oxide) overdrive to 3.3V	OD25_33 rules	✓	
OD25_18	18;4	DRC dummy layer for 2.5V thick oxide (second gate oxide) underdrive to 1.8V	OD25_18 rules	✓	
RH	117	For OD, PO resistors	OD and PO resistor guidelines	✓	✓
VAR	143	This layer is for MOS type varactors.	MOS varactor rules	✓	✓
RPDMY	115	Poly/OD resistors dummy layer for LVS and DRC	OD and Poly Resistor Layout Rules	✓	
SEALRING	162	Covers the seal ring region and metal fuse protection ring region.	Seal ring rules	✓	✓ (For N55 use)
CSRDMY	166	For stress relief pattern rule check.	Chip corner rules	✓	
CDUDMY	165	DRC dummy layer to recognize CDU pattern	Seal ring rules	✓	
LOGO	158	LOGO and product labels layer for DRC	Logo rules	✓	
BJTDMY	110;0	Cover BJT device	Analog layout rule	✓	✓
BJTDMY (drawing 1)	110;1	LVS dummy layer for small BJT	Analog layout rule		
HVD_N	91;3	Define HV NMOS drain side where sustains high voltage	HVD_N rules	✓	✓
HVD_P	91;2	Define HV PMOS drain side where sustains high voltage	HVD_P rules	✓	✓
MOM					
MOMDMY_1	155;1	Dummy layer for M1 MOM region	MOM rules	✓	
MOMDMY_2	155;2	Dummy layer for M2 MOM region	MOM rules	✓	
MOMDMY_3	155;3	Dummy layer for M3 MOM region	MOM rules	✓	
MOMDMY_4	155;4	Dummy layer for M4 MOM region	MOM rules	✓	
MOMDMY_5	155;5	Dummy layer for M5 MOM region	MOM rules	✓	
MOMDMY_6	155;6	Dummy layer for M6 MOM region	MOM rules	✓	
MOMDMY_7	155;7	Dummy layer for M7 MOM region	MOM rules	✓	
MOMDMY_8	155;8	Dummy layer for M8 MOM region	MOM rules	✓	
MOMDMY_9	155;9	Dummy layer for M9 MOM region	MOM rules	✓	
MOMDMY_AP	155;20	Dummy layer for AP MOM region	MOM rules	✓	
RTMOMDMY	155;21	Dummy layer for RTMOM	PO.R.4/ PO.L.1	✓	

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Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape out required layer
MS RF					
CTMDMY	148;0	Dummy marker layer for MIM capacitor. Use for DRC. Its size is equal to CBM layer sizes up +10 µm per side.	CTM and CBM rules	✓	
CTMDMY (drawing 1)	148;10	LVS dummy layer for putting BB/RF devices under 2T BB MIMCAPs.			
CTMDMY	148;110	Dummy marker layer for MIM capacitor 1.0fF/um^2. Use for DRC. Its size is equal to CBM layer sizes up +10 µm per side.	CTM and CBM rules	✓	
CTMDMY	148;115	Dummy marker layer for MIM capacitor 1.5fF/um^2. Use for DRC. Its size is equal to CBM layer sizes up +10 µm per side.	CTM and CBM rules	✓	
CTMDMY	148;120	Dummy marker layer for MIM capacitor 2.0fF/um^2. Use for DRC. Its size is equal to CBM layer sizes up+10 µm per side.	CTM and CBM rules	✓	
INDDMY_MD	144;37	Dummy layer for medium metal density inductor	INDDMY_MD rules	✓	
INDDMY_COIL	144;36	This dummy layer is drawn over metal coil region within INDDMY_MD.	INDDMY_MD rules	✓	
INDDMY_HD	144;38	Dummy layer for high metal density (logic) inductor	INDDMY_HD rules	✓	
INDDMY	144;0 ~ 144;14	Dummy layer for low metal density inductor	IND rules and Dummy OD/PO/metal rules	✓	
RFDMY	161	RFDMY is a required dummy layer for LVS/DRC device recognition and SPICE simulation. RFDMY should completely cover the RF devices that require a TSMC RF model.	VAR rules	✓	
RFDMY (drawing 1)	161;10	LVS dummy layer for putting BB/RF devices under RF MIMCAPs with shielding.			
SRAM					
SRM	50;0	SRM is used to generate the VTC_N/VT_P masks for all SRAM cell sizes. Covers the SRAM cell array. The edge of the SRM layer should be aligned to the boundary of the SRAM cell array, which may include storage, strapping, and dummy edge cells. If you have SRAM in your chip, and then you have OPC mask to tape out, you need to include the 50;0 in your GDS.	SRAM rules	✓	✓
SRM_11	50;11	SRM_11 is used to cover 0.62 µm² SRAM cell array.	SRAM rules	✓	✓
SRM_12	50;12	SRM_12 is used to cover 0.974 µm² SRAM cell array.	SRAM rules	✓	✓
SRM_13	50;13	SRM_13 is used to cover 8T 1.158 µm² SRAM cell array.	SRAM rules	✓	✓
SRM_14	50;14	SRM_14 is used to cover 10T 1.158 µm² SRAM cell array.	SRAM rules	✓	✓
SRAMDMY_0	186;0	SRAM DRC violation waiver layer. It can waive SRAM DRC violations under VIA1 as well as the rules, M2.S.5, M2.A.1, VIA2.EN.2, and M3.EN.2. If you have SRAM in your chip, and then you have OPC masks to tape out, you need to include the 186;0 in your GDS.	SRAM rules	✓	✓

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Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape out required layer
		Before using SRAMDMY, please make sure that TSMC has reviewed the SRAM library to avoid real violations that are automatically waived by the SRAMDMY marker layer.			
SRAMDMY_1	186;1	Cover the pass-gate transistor of SRAM cells. If N55 SRAM cell is used, 186;1 is a must for tape-out.	SRAM rules	✓	✓
SRAMDMY_4	186;4	SRAM periphery DRC layer can only be used in the word decoder of TSMC SRAM (0.525 μm², 0.62 μm², 0.974μm², 1.158μm²). This layer is only to waive CO.S.3 and G.1. And the SRAM must be reviewed by TSMC's R&D and PE even if you uses TSMC cell. In addition, 186;4 will be referred for CO mask tape-out. It is a must for any SRAM decoder with rule pushed layout. SRAMDMY_4 (186;4) overlap of SRAMDMY_0 (186;0) is not allowed.	SRAM rules	✓	✓
SRAMDMY_5	186;5	Same usage as 186;4 but is used for 0.499 μm²	SRAM rules	✓	✓
CO_11	30;11	It is a must layer for CO mask tape-out. The CO_11 is square CO in bit cell except butted CO.	SRAM rules	✓	✓
Latch up and ESD					
LUPWDMY	255;1	Some design structure may fail the DRC check in LUP.1, LUP.2, LUP.3.1, LUP.3.2, LUP.3.3, LUP.3.4, LUP.3.5, LUP.4, LUP.5.1, LUP.5.2, LUP.5.3, LUP.5.4, LUP.5.5. You can use LUPWDMY to waive these violations as they are silicon proven at package level. Don't use this layer before silicon proven, and consult tsmc if you have any DRC violation.	Latch up rules	✓	
LUPWDMY_2	255;18	A DRC dummy layer to trigger the area I/O latch-up rules check	AAIO latch up rules	✓	
SDI	122	SDI is a required DRC dummy (marker) layer to check I/O ESD and latch-up guidelines. The SDI layer must cover all I/O MOS (OD) regions that are connected to pads.	Latch up rules and ESD guidelines	✓	
AP (pin)	126;0	AP pin for text layer	Latch up rules	✓	
ESDIMP	189;0	A drawing layer for ESD implant	ESDIMP rules	✓	✓
ESD3	147	This layer is required for ESD implant mask generation.	ESD guidelines		✓
VDDDMY	255;4	Dummy Layer for Power(Vdd) PAD	Latch up rules	✓	
VSSDMY	255;5	Dummy Layer for Ground(Vss) PAD	Latch up rules	✓	
HIA_DUMMY	168;0	Dummy Layer for high current diode	HIA_DIO guideline	✓	
M1(pin)	131;0	Metal1 pin for text layer	Latch up rules	✓	
M2(pin)	132;0	Metal2 pin for text layer	Latch up rules	✓	
M3(pin)	133;0	Metal3 pin for text layer	Latch up rules	✓	
M4(pin)	134;0	Metal4 pin for text layer	Latch up rules	✓	
M5(pin)	135;0	Metal5 pin for text layer	Latch up rules	✓	
M6(pin)	136;0	Metal6 pin for text layer	Latch up rules	✓	
M7(pin)	137;0	Metal7 pin for text layer	Latch up rules	✓	
M8(pin)	138;0	Metal8 pin for text layer	Latch up rules	✓	
M9(pin)	139;0	Metal9 pin for text layer	Latch up rules	✓	

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Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape out required layer
Dummy utility					
ODBLK	150;20	Dummy OD exclusion marker layer	DOD rules	✓	
POBLK	150;21	Dummy PO exclusion marker layer	DPO rules	✓	
DMxEXCL	150;x	Dummy Mx exclusion marker layer and redundant via	DMx rules	✓	
TCDDMY	165;1	Dummy TCD layer	DTCD Rules	✓	
DFM					
RRuleRequire	182;1	Dummy layer for DFM Action-Required recommendation	DFM Action-Required	✓	
RRuleRecommend	182;2	Dummy layer for DFM Recommended recommendation	DFM Recommended	✓	
RRuleAnalog	182;3	Dummy layer for Rules, Recommendations, and Guidelines. for Analog Designs	Rules and Recommendations for Analog Designs	✓	
RRuleGuideline	182;4	Dummy layer for DFM guideline check	DFM guideline	✓	
excludeRRuleRequire	182;11	DRC dummy layer for excluding DFM Action-Required recommendation check.	DFM Action-Required	✓	
excludeRRuleRecommended	182;12	DRC dummy layer for excluding DFM DFM Recommended recommendation check	DFM Recommended	✓	
excludeRRuleAnalog	182;13	DRC dummy layer for excluding DFM Recommended Dimension check for Analog Designs	Rules and Recommendations for Analog Designs	✓	
excludeRRuleGuidelines	182;14	DRC dummy layer for excluding DFM guideline check	DFM guideline	✓	
Fuse					
PMDMY	106	Dummy layer to cover metal fuse protection ring structure for DRC. For details, please refer to Doc.: T-00-CL-DR-005 (Al Fuse Rule).	Fuse rules	✓	
POFUSE	156;0	Poly fuse implant layer, cover all poly fuse regions.	PO rule	✓	✓
FUSELINK	156;1	A layer to cover poly fuse neck region	PO rule	✓	✓
LMARK	109	This layer is for laser repair alignment mark opening. For details, please refer to Doc.: T-00-CL-DR-005 (Al Fuse Rule).	Fuse rules	✓	✓
Pad					
WBDMY	157;0	CUP pad region marker layer for N65 CUP relative rule check	CUP rules	✓	

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3.5 Device Truth Tables

This section contains the device truth tables for.

- CLN65 Logic General Purpose (G) technology
- CLN65 Logic General Purpose Plus (GP) technology
- CLN65 Logic Low Power (LP) technology
- CLN65 Logic LP-based Triple Gate Oxide (LPG) technology
- CLN65 Logic Ultra Low Power (ULP) technology
- CLN55 Logic General Purpose Plus (GP) technology
- CLN55 Logic Low Power (LP) technology
- CMN65 MIM
- CLN65/LCN55/CMN65/CMN55 MOM
- CMN65 Inductor
- CMN65 LP High Current Diode (HIA_DIO)

The following provides a legend for the following device truth tables.

Table 3.5.1 Table Legend for Device Truth Tables

0	Does not cover the structures
1	Covers or matches the structures
*****	Don't care

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3.5.1 CLN65 General Purpose (G):

Table 3.5.2

Device	SPICE Name	Design Levels												Special Layer				
		DNW	OD	NW	NT_N	OD_25	OD_18	POLY	VTH_N	VTH_P	N+	P+	RPO	RH	NWDMY	VAR	BJTDMY	ESD3
NMOS (1.0V)	nch	*	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
PMOS (1.0V)	pch	*	1	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0
High Vt NMOS (1.0V)	nch_hvt	*	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0
High Vt PMOS (1.0V)	pch_hvt	*	1	1	0	0	0	1	0	1	0	1	0	0	0	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	0	1	0	0	0	1	0	0	0	0	0	0
I/O NMOS (1.8V)	nch_18	*	1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0
I/O PMOS (1.8V)	pch_18	*	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0
Native NMOS (1.0V)	nch_na	0	1	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0
Native I/O NMOS (1.8V)	nch_na18	0	1	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	0	0	0	1	0	0	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	0	0	0	0	1	0	0	0	0	0	0
High Vt N+/PW Junction Diode (1.0V)	NDIO_hvt	*	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
High Vt P+/NW Junction Diode (1.0V)	PDIO_hvt	*	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0
I/O N+/PW Junction Diode (1.8V)	NDIO_18	*	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (1.8V)	PDIO_18	*	1	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0
I/O N+/PW Junction Diode (2.5V)	NDIO_25	*	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (2.5V)	PDIO_25	*	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0
Native N+/PW Junction Diode (1.0V)	NDIO_na	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (2.5V)	NDIO_na25	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (1.8V)	NDIO_na18	0	1	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0
PW/DNW Junction Diode	PWDNW	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
DNW/PSUB Junction Diode	DNWPSUB	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
ESD Junction Diode	NDIO_ESD	*	1	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1
NW/PSUB Junction Diode	NWDIO	*	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
P-Well Contact		*	1	0	0	*	*	0	0	0	0	1	0	0	0	0	0	0
N-Well Contact		*	1	1	0	*	*	0	0	0	1	0	0	0	0	0	0	0
Silicided N+ PO Resistor	rnpoly	*	0	*	0	0	0	1	0	0	1	0	0	0	0	0	0	0
Silicided P+ PO Resistor	rppoly	*	0	*	0	0	0	1	0	0	0	1	0	0	0	0	0	0
Silicided N+ OD Resistor	rnod	*	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Silicided P+ OD Resistor	rpod	*	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Unsilicided N+ PO Resistor	rnpolywo	*	0	*	0	0	0	1	0	0	1	0	1	1	0	0	0	0
Unsilicided P+ PO Resistor	rppolywo	*	0	*	0	0	0	1	0	0	0	1	1	1	0	0	0	0
Unsilicided N+ OD Resistor	rnodwo	*	1	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0
Unsilicided P+ OD Resistor	rpodwo	*	1	1	0	0	0	0	0	0	0	1	1	1	0	0	0	0
NW Resistor (under STI)	rnwsti	0	1	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0
NW Resistor (under OD)	rnwod	0	1	1	0	0	0	0	0	0	1	0	1	0	1	0	0	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 μm^2) pnp5 (5x5 μm^2) pnp10 (10x10 μm^2)	0	1	1	0	0	0	0	0	0	1	1	1	*	0	0	1	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 μm^2) npn5 (5x5 μm^2) npn10 (10x10 μm^2)	1	1	1	0	0	0	0	0	0	1	1	1	*	0	0	1	0

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Device	SPICE Name	Design Levels												Special Layer				
		DNW	OD	NW	NT_N	OD_25	OD_18	POLY	VTH_N	VTH_P	N+	P+	RPO	RH	NWDMY	VAR	BJTDMY	ESD3
1.0V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0
1.8V Varactor (NMOS Capacitor)	nmoscap18	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0	0
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	1	0	1	0	0	1	0	0	0	0	1	0	0

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3.5.2 CLN65 General Purpose Plus (GP):

Table 3.5.3

Device	SPICE Name	Design Levels														Special Layer				
		DNW	OD	NW	NT_N	OD_25	OD_18	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	RH	NWDMY	VAR	BJTDMY	ESD3
NMOS (1.0V)	nch	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
PMOS (1.0V)	pch	*	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
High Vt NMOS (1.0V)	nch_hvt	*	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0
High Vt PMOS (1.0V)	pch_hvt	*	1	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0
Low Vt NMOS (1.0V)	nch_lvt	*	1	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0
Low Vt PMOS (1.0V)	pch_lvt	*	1	1	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0
I/O NMOS (1.8V)	nch_18	*	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0
I/O PMOS (1.8V)	pch_18	*	1	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0
Native NMOS (1.0V)	nch_na	0	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O NMOS (1.8V)	nch_na18	0	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	0	0	0	0	0	1	0	0	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	0	0	0	0	0	0	1	0	0	0	0	0	0
High Vt N+/PW Junction Diode (1.0V)	NDIO_hvt	*	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
High Vt P+/NW Junction Diode (1.0V)	PDIO_hvt	*	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0
Low Vt N+/PW Junction Diode (1.0V)	NDIO_lvt	*	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
Low Vt P+/NW Junction Diode (1.0V)	PDIO_lvt	*	1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
I/O N+/PW Junction Diode (1.8V)	NDIO_18	*	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (1.8V)	PDIO_18	*	1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
I/O N+/PW Junction Diode (2.5V)	NDIO_25	*	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (2.5V)	PDIO_25	*	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Native N+/PW Junction Diode (1.0V)	NDIO_na	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (2.5V)	NDIO_na25	0	1	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (1.8V)	NDIO_na18	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0
PW/DNW Junction Diode	PWDNW	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
DNW/PSUB Junction Diode	DNWPSUB	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
ESD Junction Diode	NDIO_ESD	*	1	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	1
NW/PSUB Junction Diode	NWDIO	*	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
P-Well Contact		*	1	0	0	*	*	0	0	0	0	0	0	1	0	0	0	0	0	0
N-Well Contact		*	1	1	0	*	*	0	0	0	0	0	1	0	0	0	0	0	0	0
Silicided N+ PO Resistor	rnpoly	*	0	*	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
Silicided P+ PO Resistor	rppoly	*	0	*	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
Silicided N+ OD Resistor	rnod	*	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Silicided P+ OD Resistor	rpod	*	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Unsilicided N+ PO Resistor	rnpolywo	*	0	*	0	0	0	1	0	0	0	0	1	0	1	1	0	0	0	0
Unsilicided P+ PO Resistor	rppolywo	*	0	*	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0
Unsilicided N+ OD Resistor	rnodwo	*	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0
Unsilicided P+ OD Resistor	rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
NW Resistor (under STI)	rnwsti	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
NW Resistor (under OD)	rnwod	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0

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Device	SPICE Name	Design Levels														Special Layer				
		DNW	OD	NW	NT_N	OD_25	OD_18	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	RH	NWDMY	VAR	BJTDMY	ESD3
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 μm^2) pnp5 (5x5 μm^2) pnp10 (10x10 μm^2)	0	1	1	0	0	0	0	0	0	0	0	1	1	1	*	0	0	1	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 μm^2) npn5 (5x5 μm^2) npn10 (10x10 μm^2)	1	1	1	0	0	0	0	0	0	0	0	1	1	1	*	0	0	1	0
1.0V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0
1.8V Varactor (NMOS Capacitor)	nmoscap18	0	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0	0
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	1	0	1	0	0	0	0	1	0	0	0	0	1	0	0

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3.5.3 CLN65 Low Power (LP):

Table 3.5.4

Device	SPICE Name	Design Levels															Special Layer						
		DNW	OD	NW	NT_N	OD_18	OD_25	OD_33	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	mVTL	RH	NWDMY	VAR	BJTDMY	ESD3	HVD_N	HVD_P
NMOS (1.2V)	nch	*	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
PMOS (1.2V)	pch	*	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
High Vt NMOS (1.2V)	nch_hvt	*	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
High Vt PMOS (1.2V)	pch_hvt	*	1	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
Low Vt NMOS (1.2V)	nch_lvt	*	1	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
Low Vt PMOS (1.2V)	pch_lvt	*	1	1	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
m Low Vt NMOS (1.2V)	nch_mlvt	*	1	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
m Low Vt PMOS (1.2V)	pch_mlvt	*	1	1	0	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
HV NMOS (5V)	nch_hv25_snw	0	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0
HV PMOS (5V)	pch_hv25_spw	0	1	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
I/O NMOS (2.5V)	nch_25	*	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
I/O NMOS (3.3V)	nch_33	*	1	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
I/O PMOS (3.3V)	pch_33	*	1	1	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Native NMOS (1.2V)	nch_na	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Native I/O NMOS (3.3V)	nch_na33	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	*	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
High Vt N+/PW Junction Diode (1.2V)	NDIO_hvt	*	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
High Vt P+/NW Junction Diode (1.2V)	PDIO_hvt	*	1	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
Low Vt N+/PW Junction Diode (1.2V)	NDIO_lvt	*	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
Low Vt P+/NW Junction Diode (1.2V)	PDIO_lvt	*	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
m Low Vt N+/PW Junction Diode (1.2V)	NDIO_mlvt	*	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
m Low Vt P+/NW Junction Diode (1.2V)	PDIO_mlvt	*	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
I/O N+/PW Junction Diode (2.5V)	NDIO_25	*	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (2.5V)	PDIO_25	*	1	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
I/O N+/PW Junction Diode (3.3V)	NDIO_33	*	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (3.3V)	PDIO_33	*	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Native N+/PW Junction Diode (1.2V)	NDIO_na	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (2.5V)	NDIO_na25	0	1	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (3.3V)	NDIO_na33	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
PW/DNW Junction Diode	PWDNW	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
DNW/PSUB Junction Diode	DNWPSUB	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
ESD Junction Diode	NDIO_ESD	*	1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0
NW/PSUB Junction Diode	NWDIO	*	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
P-Well Contact		*	1	0	0	*	*	*	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
N-Well Contact		*	1	1	0	*	*	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Silicided N+ PO Resistor	Rnpoly	*	0	*	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Silicided P+ PO Resistor	Rppoly	*	0	*	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Silicided N+ OD Resistor	Rnod	*	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Silicided P+ OD Resistor	Rpod	*	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Unsilicided N+ PO Resistor	Rnpolywo	*	0	*	0	0	0	0	1	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0
Unsilicided P+ PO Resistor	Rppolywo	*	0	*	0	0	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0

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Device	SPICE Name	Design Levels																Special Layer						
		DNW	OD	NW	NT_N	OD_18	OD_25	OD_33	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	mVTL	RH	NWDMY	VAR	BJTDMY	ESD3	HVD_N	HVD_P
Unsilicided N+ OD Resistor	Rnodwo	*	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0
Unsilicided P+ OD Resistor	Rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0
NW Resistor (under STI)	Rnwsti	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
NW Resistor (under OD)	Rnwod	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 um^2) pnp5 (5x5 um^2) pnp10 (10x10 um^2)	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	*	0	0	1	0	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 um^2) npn5 (5x5 um^2) npn10 (10x10 um^2)	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	*	0	0	1	0	0	0
1.2V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
3.3V Varactor (NMOS Capacitor)	nmoscap33	0	1	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0

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3.5.4 CLN65 LP-based Triple Gate Oxide (LPG) Design

Table 3.5.5

Device	SPICE Name	Design Levels															Special Layer							
		DNW	OD	NW	NT_N	OD_25	DCO	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	MVTL	OD25_18	OD25_33	SRAM	RH	NWDMY	VAR	BJTDMY	ESD3
NMOS (1.0V)	nch_lpg	*	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
PMOS (1.0V)	pch_lpg	*	1	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
NMOS (1.2V)	nch	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
PMOS (1.2V)	pch	*	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
High Vt NMOS (1.0V)	nch_lpghvt	*	1	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
High Vt PMOS (1.0V)	pch_lpghvt	*	1	1	0	0	1	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
High Vt NMOS (1.2V)	nch_hvt	*	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
High Vt PMOS (1.2V)	pch_hvt	*	1	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
I/O NMOS (2.5V under-drive 1.8V)	nch_25ud18	*	1	0	0	1	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
I/O PMOS (2.5V under-drive 1.8V)	pch_25ud18	*	1	1	0	1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
I/O NMOS (2.5V over-drive 3.3V)	nch_25od33	*	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0
I/O PMOS (2.5V over-drive 3.3V)	pch_25od33	*	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Native NMOS (1.0V)	nch_lpgna	0	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Native NMOS (1.2V)	nch_na	0	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
SRAM PD MOS (1.0V)	nchpd_lpgsr	*	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
SRAM PG MOS (1.0V)	nchpg_lpgsr	*	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
SRAM PU MOS (1.0V)	nchpu_lpgsr	*	1	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
SRAM PD MOS (1.2V)	nchpd_sr	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
SRAM PG MOS (1.2V)	nchpg_sr	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
SRAM PU MOS (1.2V)	nchpu_sr	*	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
High Vt SRAM PD MOS (1.2V)	nchpd_hvtsr	*	1	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0
High Vt SRAM PG MOS (1.2V)	nchpg_hvtsr	*	1	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0
High Vt SRAM PU MOS (1.2V)	nchpu_hvtsr	*	1	1	0	0	0	1	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0
DP SRAM PD MOS (1.2V)	nchpd_dpsr	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
DP SRAM PG MOS (1.2V)	nchpg_dpsr	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
DP SRAM PU MOS (1.2V)	nchpu_dpsr	*	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
DP High Vt SRAM PD MOS (1.2V)	nchpd_dphvtsr	*	1	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0
DP High Vt SRAM PG MOS (1.2V)	nchpg_dphvtsr	*	1	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0
DP High Vt SRAM PU MOS (1.2V)	nchpu_dphvtsr	*	1	1	0	0	0	1	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0
N+/PW Junction Diode (1.0V)	ndio_lpg	*	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
P+/NW Junction Diode (1.0V)	pdio_lpg	*	1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
N+/PW Junction Diode (1.2V)	ndio	*	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
P+/NW Junction Diode (1.2V)	pdio	*	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
High Vt N+/PW Junction Diode (1.0V)	ndio_lpghvt	*	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
High Vt P+/NW Junction Diode (1.0V)	pdio_lpghvt	*	1	1	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
High Vt N+/PW Junction Diode (1.2V)	ndio_hvt	*	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

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Device	SPICE Name	Design Levels															Special Layer							
		DNW	OD	NW	NT_N	OD_25	DCO	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	MVTL	OD25_18	OD25_33	SRAM	RH	NWDMY	VAR	BJTDMY	ESD3
High Vt P+/NW Junction Diode (1.2V)	pdio_hvt	*	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0
I/O N+/PW Junction Diode (2.5V)	ndio_25	*	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (2.5V)	pdio_25	*	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
I/O N+/PW Junction Diode (2.5V under-drive 1.8V)	ndio_25ud18	*	1	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (2.5V under-drive 1.8V)	pdio_25ud18	*	1	1	0	1	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0
I/O N+/PW Junction Diode (2.5V over-drive 3.3V)	ndio_25od33	*	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0
I/O P+/NW Junction Diode (2.5V over-drive 3.3V)	pdio_25od33	*	1	1	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0
Native N+/PW Junction Diode (1.2V)	NDIO_na	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Native N+/PW Junction Diode (1.0V)	NDIO_lpgna	0	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (2.5V)	NDIO_na25	0	1	0	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
PW/DNW Junction Diode	PWDNW	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
DNW/PSUB Junction Diode	DNWPSUB	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
ESD Junction Diode	NDIO_ESD	*	1	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1
NW/PSUB Junction Diode	NWDIO	*	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
P-Well Contact		*	1	0	0	*	*	0	0	0	0	0	0	1	0	0	*	*	0	0	0	0	0	0
N-Well Contact		*	1	1	0	*	*	0	0	0	0	0	1	0	0	0	*	*	0	0	0	0	0	0
Unsilicided N+ PO Resistor	rnpolywo	*	0	*	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0
Unsilicided P+ PO Resistor	rppolywo	*	0	*	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0
Unsilicided N+ OD Resistor	rnodwo	*	1	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0
Unsilicided P+ OD Resistor	rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0
NW Resistor (under OD)	rnwod	0	1	1	0	0	*	0	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 um^2) pnp5 (5x5 um^2) pnp10 (10x10 um^2)	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	1	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 um^2) npn5 (5x5 um^2) npn10 (10x10 um^2)	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	1	0
1.0V Varactor (NMOS Capacitor)	nmoscap_lpg	0	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
1.2V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0
2.5V Varactor (NMOS Capacitor)	nmoscap_25	0	1	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0

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3.5.5 CLN65 Ultar Low Power (ULP) Design

Table 3.5.6

Device	SPICE Name	Design Levels														Special Layer				
		DNW	OD	NW	NT_N	OD_25	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	mVTL	RH	NWDMY	VAR	BJTDMY	ESD3
NMOS (1.0V)	nch	*	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
PMOS (1.0V)	pch	*	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0
High Vt NMOS (1.0V)	nch_hvt	*	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
High Vt PMOS (1.0V)	pch_hvt	*	1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0
Low Vt NMOS (1.0V)	nch_lvt	*	1	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0
Low Vt PMOS (1.0V)	pch_lvt	*	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0
m Low Vt NMOS (1.0V)	nch_mlvt	*	1	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0
m Low Vt PMOS (1.0V)	pch_mlvt	*	1	1	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
Native NMOS (1.0V)	nch_na	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0
N+/PW Junction Diode (1.0V)	NDIO	*	1	0	0	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0
P+/NW Junction Diode (1.0V)	PDIO	*	1	1	0	*	0	0	0	0	0	0	1	0	0	0	0	0	0	0
High Vt N+/PW Junction Diode (1.0V)	NDIO_hvt	*	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
High Vt P+/NW Junction Diode (1.0V)	PDIO_hvt	*	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
Low Vt N+/PW Junction Diode (1.0V)	NDIO_lvt	*	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
Low Vt P+/NW Junction Diode (1.0V)	PDIO_lvt	*	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
I/O N+/PW Junction Diode (2.5V)	NDIO_25	*	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (2.5V)	PDIO_25	*	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Native N+/PW Junction Diode (1.0V)	NDIO_na	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (2.5V)	NDIO_na25	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
PW/DNW Junction Diode	PWDNW	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
DNW/PSUB Junction Diode	DNWPSUB	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
ESD Junction Diode	NDIO_ESD	*	1	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	1
NW/PSUB Junction Diode	NWDIO	*	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
P-Well Contact		*	1	0	0	*	0	0	0	0	0	0	1	0	0	0	0	0	0	0
N-Well Contact		*	1	1	0	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Silicided N+ PO Resistor	Rnpoly	*	0	*	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
Silicided P+ PO Resistor	Rppoly	*	0	*	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0
Silicided N+ OD Resistor	Rnod	*	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Silicided P+ OD Resistor	Rpod	*	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Unsilicided N+ PO Resistor	Rnpolywo	*	0	*	0	0	1	0	0	0	0	1	0	1	0	1	0	0	0	0
Unsilicided P+ PO Resistor	Rppolywo	*	0	*	0	0	1	0	0	0	0	0	1	1	0	1	0	0	0	0
Unsilicided N+ OD Resistor	Rnodwo	*	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0
Unsilicided P+ OD Resistor	Rpodwo	*	1	1	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0
NW Resistor (under STI)	Rnwsti	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0
NW Resistor (under OD)	Rnwod	0	1	1	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 um^2) pnp5 (5x5 um^2) pnp10 (10x10 um^2)	0	1	1	0	0	0	0	0	0	0	1	1	1	0	*	0	0	1	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 um^2) npn5 (5x5 um^2) npn10 (10x10 um^2)	1	1	1	0	0	0	0	0	0	0	1	1	1	0	*	0	0	1	0
1.0V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0

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3.5.6 CLN55 General Purpose Plus (GP):

Table 3.5.7

Device	SPICE Name	Design Levels															Special Layer				
		DNW	OD	NW	NT_N	OD_33	OD_25	OD_18	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	RH	NWDMY	VAR	BJTDMY	ESD3
NMOS (1.0V)	nch	*	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
PMOS (1.0V)	pch	*	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
High Vt NMOS (1.0V)	nch_hvt	*	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0
High Vt PMOS (1.0V)	pch_hvt	*	1	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0
Low Vt NMOS (1.0V)	nch_lvt	*	1	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0
Low Vt PMOS (1.0V)	pch_lvt	*	1	1	0	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0
I/O NMOS (3.3V)	nch_33	*	*	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
I/O PMOS (3.3V)	pch_33	*	*	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0
I/O NMOS (1.8V)	nch_18	*	1	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0
I/O PMOS (1.8V)	pch_18	*	1	1	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0
Native NMOS (1.0V)	nch_na	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O NMOS (3.3V)	nch_na33	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O NMOS (1.8V)	nch_na18	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
High Vt N+/PW Junction Diode (1.0V)	NDIO_hvt	*	1	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0
High Vt P+/NW Junction Diode (1.0V)	PDIO_hvt	*	1	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0
Low Vt N+/PW Junction Diode (1.0V)	NDIO_lvt	*	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0
Low Vt P+/NW Junction Diode (1.0V)	PDIO_lvt	*	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
I/O N+/PW Junction Diode (1.8V)	NDIO_18	*	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (1.8V)	PDIO_18	*	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
I/O N+/PW Junction Diode (2.5V)	NDIO_25	*	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (2.5V)	PDIO_25	*	1	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
I/O N+/PW Junction Diode (3.3V)	NDIO_33	*	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (3.3V)	PDIO_33	*	1	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Native N+/PW Junction Diode (1.0V)	NDIO_na	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (3.3V)	NDIO_na33	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (2.5V)	NDIO_na25	0	1	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (1.8V)	NDIO_na18	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0
PW/DNW Junction Diode	PWDNW	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
DNW/PSUB Junction Diode	DNWPSUB	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
ESD Junction Diode	NDIO_ESD	*	1	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	1
NW/PSUB Junction Diode	NWDIO	*	1	0	0	*	*	*	0	0	0	0	0	1	0	0	0	0	0	0	0
P-Well Contact		*	1	0	0	*	*	*	0	0	0	0	0	0	1	0	0	0	0	0	0
N-Well Contact		*	1	1	0	*	*	*	0	0	0	0	0	1	0	0	0	0	0	0	0
Silicided N+ PO Resistor	rnpoly	*	0	*	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0
Silicided P+ PO Resistor	rppoly	*	0	*	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
Silicided N+ OD Resistor	rnod	*	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Silicided P+ OD Resistor	rpod	*	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Unsilicided N+ PO Resistor	rnpolywo	*	0	*	0	0	0	0	1	0	0	0	0	1	0	1	1	0	0	0	0
Unsilicided P+ PO Resistor	rppolywo	*	0	*	0	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0
Unsilicided N+ OD Resistor	rnodwo	*	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0

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Device	SPICE Name	Design Levels															Special Layer				
		DNW	OD	NW	NT_N	OD_33	OD_25	OD_18	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	RH	NWDMY	VAR	BJTDMY	ESD3
Unsilicided P+ OD Resistor	rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0
NW Resistor (under STI)	rnwsti	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
NW Resistor (under OD)	rnwod	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 μm^2) pnp5 (5x5 μm^2) pnp10 (10x10 μm^2)	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	*	0	0	1	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 μm^2) npn5 (5x5 μm^2) npn10 (10x10 μm^2)	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	*	0	0	1	0
1.0V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0
1.8V Varactor (NMOS Capacitor)	nmoscap18	0	1	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	1	0	0
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	1	0	0
3.3V Varactor (NMOS Capacitor)	nmoscap33	0	1	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0

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3.5.7 CLN55 Low Power (LP):

Table 3.5.8

Device	SPICE Name	Design Levels													Special Layer						
		DNW	OD	NW	NT_N	OD_25	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	RH	NWDMY	VAR	BJTDMY	ESD3	HVD_N	HVD_P
NMOS (1.2V)	nch	*	1	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
PMOS (1.2V)	pch	*	1	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
High Vt NMOS (1.2V)	nch_hvt	*	1	0	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
High Vt PMOS (1.2V)	pch_hvt	*	1	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0
Low Vt NMOS (1.2V)	nch_lvt	*	1	0	0	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
Low Vt PMOS (1.2V)	pch_lvt	*	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Native NMOS (1.2V)	nch_na	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
High Vt N+/PW Junction Diode (1.2V)	NDIO_hvt	*	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
High Vt P+/NW Junction Diode (1.2V)	PDIO_hvt	*	1	1	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
Low Vt N+/PW Junction Diode (1.2V)	NDIO_lvt	*	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
Low Vt P+/NW Junction Diode (1.2V)	PDIO_lvt	*	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
I/O N+/PW Junction Diode (2.5V)	NDIO_25	*	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
I/O P+/NW Junction Diode (2.5V)	PDIO_25	*	1	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Native N+/PW Junction Diode (1.2V)	NDIO_na	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Native I/O N+/PW Junction Diode (2.5V)	NDIO_na25	0	1	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
PW/DNW Junction Diode	PWDNW	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
DNW/PSUB Junction Diode	DNWPSUB	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
ESD Junction Diode	NDIO_ESD	*	1	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	1	0	0
NW/PSUB Junction Diode	NWDIO	*	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
P-Well Contact		*	1	0	0	*	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
N-Well Contact		*	1	1	0	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Silicided N+ PO Resistor	rnpoly	*	0	*	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Silicided P+ PO Resistor	rppoly	*	0	*	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Silicided N+ OD Resistor	rnod	*	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Silicided P+ OD Resistor	rpod	*	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Unsilicided N+ PO Resistor	rnpolywo	*	0	*	0	0	1	0	0	0	0	1	0	1	1	0	0	0	0	0	0
Unsilicided P+ PO Resistor	rppolywo	*	0	*	0	0	1	0	0	0	0	0	1	1	1	0	0	0	0	0	0
Unsilicided N+ OD Resistor	rnodwo	*	1	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0
Unsilicided P+ OD Resistor	rpodwo	*	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
NW Resistor (under STI)	rnwsti	0	1	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0
NW Resistor (under OD)	rnwod	0	1	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 μm^2) pnp5 (5x5 μm2) pnp10 (10x10 μm2)	0	1	1	0	0	0	0	0	0	0	1	1	1	*	0	0	1	0	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 μm^2) npn5 (5x5 μm2) npn10 (10x10 μm2)	1	1	1	0	0	0	0	0	0	0	1	1	1	*	0	0	1	0	0	0
1.2V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	1	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0

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3.5.8 CMN65 MIM

Table 3.5.9

Device	SPICE Name	Design Levels														Special Layer																				
		DNW	NP/PP	OD	NW/PW	CO	M1	M5	M6	M8	VIA5	VIA7	CTM	CBM	CTMDMY	M1(pin)	M6(pin)	M8(pin)	RFDMY	CTMDMY(148;110)	CTMDMY(148;115)	CTMDMY(148;120)	POBLK	ODBLK	DMEXCL(d1)	DMEXCL(d2)	DMEXCL(d3)	DMEXCL(d4)	DMEXCL(d5)	DMEXCL(d6)	DMEXCL(d7)	DMEXCL(d8)	DMEXCL(d9)			
MIM(Type-a)	mimcap_um_sin_rf	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	*	*	*	0	0	0	0	0	0	1	1	1	1	1			
MIM(Type-b)	NA	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	0	*	*	*	0	0	0	0	0	0	1	1	1	0	0			
MIM(Type-c)	mimcap_woum_sin_rf	*	*	1	*	1	1	0	0	1	0	1	1	1	1	1	0	1	1	*	*	*	1	1	1	1	1	1	1	1	1	1	1			
MIM(Type-d)	mimcap_sin_3t	*	*	1	*	1	1	0	0	1	0	1	1	1	1	1	0	1	0	*	*	*	1	1	1	1	1	1	1	1	1	0	0			
MIM(Type-e)	mimcap_sin	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	0	1	0	*	*	*	0	0	0	0	0	0	0	0	1	0	0			

3.5.9 CLN65/CLN55/CMN65/CMN55 MOM

Table 3.5.10

Node	SPICE Name	Design Levels																																		
		DNW	NW	NT_N	OD	OD_18	OD_25	OD_33	POLY	N+	P+	RPO	CO	M1	VIA1	M2	VIA2	M3	VIA3	M4	VIA4	M5	VIA5	M6	VIA6	M7	VIA7	M8	VIA8	M9	RV	AP				
N65/N55	crtmom	0	1	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0				
N65/N55	crtmom_rf	0	1	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0				
N65/N55	crtmom_mx	0	1	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0				

Node	SPICE Name	Special Layers																																		
		RFDMY(161;0)	MOMDMY(155;0)	MOMDMY(155;1)	MOMDMY(155;2)	MOMDMY(155;3)	MOMDMY(155;4)	MOMDMY(155;5)	MOMDMY(155;6)	MOMDMY(155;7)	MOMDMY(155;21)	MOMDMY(155;22)	MOMDMY(155;23)	MOMDMY(155;24)	MOMDMY(155;25)	MOMDMY(155;27)	ODBLK(150;20)	POBLK(150;21)	DM1EXCL(150;1)	DM2EXCL(150;2)	DM3EXCL(150;3)	DM4EXCL(150;4)	DM5EXCL(150;5)	DM6EXCL(150;6)	DM7EXCL(150;7)	DM8EXCL(150;8)	DM9EXCL(150;9)								
N65/N55	crtmom	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1									
N65/N55	crtmom_rf	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1									
N65/N55	crtmom_mx	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1									

Note:
1. MOMDMY(155;0) dummy layer RTMOM device
2. MOMDMY(155;21) dummy layer to waive violations in MOM region
3. MOMDMY(155;22) denotes MX MOM recogition.
4. MOMDMY(155;23) to recognize pin plus 1, minus 1 for MX MOM.
5. MOMDMY(155;24) to recognize pin plus 2, minus 2 for MX MOM.
6. MOMDMY(155;25) to recognize for cross-coupled mom pin.
7. RFDMY(161;0) dummy layer for RF devices.

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3.5.10 CMN65/CMN55 Inductor

Table 3.5.11

PDK Inductor Scheme [Mtop-2+Mtop-1+Mtop+(AP-RDL)]	Inductor type Device / SPICE		Design Levels																												
			DNW	NW	NT_N	OD	POLY	N+	P+	RPO	CO	M1	VIA1	M2	VIA2	M3	VIA3	M4	VIA4	M5	VIA5	M6	VIA6	M7	VIA7	M8	VIA8	M9	RV	AP
Mx+Mz+Mu (Top Metal: M5 ~ M9)	standard	spiral_std_mu_z	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	0	0
	symmetric	spiral_sym_mu_z	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	0	0
	center-tap	spiral_ct_mu_z	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1	1	1	0	0
Mx+Mu+AP-RDL (Top Metal: M5 ~ M8)	standard	spiral_std_mu_a	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1			1	1
	symmetric	spiral_sym_mu_a	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1			1	1
	center-tap	spiral_ct_mu_a	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1			1	1
Mx+Mz+AP-RDL (Top Metal: M5 ~ M8)	standard	spiral_std_mza_a	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1			1	1
	symmetric	spiral_sym_mza_a	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1			1	1
	center-tap	spiral_ct_mza_a	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1			1	1

PDK Inductor Scheme [Mtop-2+Mtop-1+Mtop+(AP-RDL)]	Inductor type Device / SPICE		Special Layer														
			INDDMY(144;0)	INDDMY(144;1)	INDDMY(144;2)	INDDMY(144;3)	INDDMY(144;4)	INDDMY(144;5)	INDDMY(144;6)	INDDMY(144;7)	INDDMY(144;8)	INDDMY(144;9)	INDDMY(144;10)	INDDMY(144;11)	INDDMY(144;30)	DMYDIS(144;31)	INDDMY(144;32)
Mx+Mz+Mu (Top Metal: M5 ~ M9)	standard	spiral_std_mu_z	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1
	symmetric	spiral_sym_mu_z	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1
	center-tap	spiral_ct_mu_z	0	0	1	0	0	0	0	0	0	0	0	0	1	1	1
Mx+Mu+AP-RDL (Top Metal: M5 ~ M8)	standard	spiral_std_mu_a	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1
	symmetric	spiral_sym_mu_a	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1
	center-tap	spiral_ct_mu_a	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1
Mx+Mz+AP-RDL (Top Metal: M5 ~ M8)	standard	spiral_std_mza_a	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1
	symmetric	spiral_sym_mza_a	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1
	center-tap	spiral_ct_mza_a	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

1. The inductor with most metal layers scheme (1P9M for two top metal layers scheme & 1P8M for one top metal layer scheme) is illustrated for the truth table.
2. INDDMY(144;30) denotes the inductor inner radius.
3. DMYDIS(144;31) denotes the distance from INDDMY to spiral outer edge.
4. INDDMY(144;32) denotes the inductor turn numbers.

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3.5.11 CMN65 LP High Current Diode (HIA_DIO):

Table 3.5.12

Device	SPICE Name	Design Levels																Special Layer							
		DNW	OD	NW	NT_N	OD_18	OD_25	OD_33	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	mVTL	RH	NWDMY	VAR	BJTDMY	ESD3	HVD_N	HVD_P	HIA_DUMMY
N+/PW Junction Diode for ESD protection#	NDIO_HIA_rf	*	1	0	0	*	*	*	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1
P+/NW Junction Diode for ESD protection#	PDIO_HIA_rf	*	1	1	0	*	*	*	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1

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3.6 Mask Requirements for Device Options (High/STD/Low VT)

Table 3.6.1

Device	Mask Requirements			
	Well			
	CLN65LP	CLN65G	CLN65GP	CLN65ULP
STD Vt+ I/O (1.8V)	-	2 masks PW1V/ NW1V	3 masks PW1V/ NW1V/ PW2V	-
STD Vt+ High Vt+ I/O (1.8V)	-	4 masks PW1V/ NW1V/ VTH_N/ VTH_P	5 masks PW1V/ NW1V/ PW2V/ VTH_N/ VTH_P	-
STD Vt+ Low Vt+ I/O (1.8V)	-	4 masks PW1V/ NW1V/ VTL_N/ VTL_P	5 masks PW1V/ NW1V/ PW2V/ VTL_N/ VTL_P	-
STD Vt+ High Vt+ Low Vt+ I/O (1.8V)	-	6 masks PW1V/ NW1V/ VTH_N/ VTH_P/ VTL_N/ VTL_P	7 masks PW1V/ PW2V/ NW1V/ VTH_N/ VTH_P/ VTL_N/ VTL_P	-
STD Vt+ I/O (2.5V)	3 masks PW1V/ PW2V/ NW1V			
STD Vt+ High Vt+ I/O (2.5V)	5 masks PW1V/ PW2V/ NW1V/ VTH_N/ VTH_P			
STD Vt+ Low Vt+ I/O (2.5V)	5 masks PW1V/ PW2V/ NW1V/ VTL_N/ VTL_P			
STD Vt+ High Vt+ Low Vt+ I/O (2.5V)	7 masks PW1V/ PW2V/ NW1V/ VTH_N/ VTH_P / VTL_N/ VTL_P			
STD Vt+ I/O (3.3V)	4 masks PW1V/ PW2V/ NW1V/ NW2V	-	-	-
STD Vt+ High Vt+ I/O (3.3V)	6 masks PW1V/ PW2V/ NW1V/ NW2V/ VTH_N/ VTH_P	-	-	-
STD Vt+ Low Vt+ I/O (3.3V)	6 masks PW1V/ PW2V/ NW1V/ NW2V/ VTL_N/ VTL_P	-	-	-
STD Vt+ High Vt+ Low Vt+ I/O (3.3V)	8 masks PW1V/ PW2V/ NW1V/ NW2V/ VTH_N/ VTH_P/ VTL_N/ VTL_P	-	-	-

CLN65LPG	Mask Requirements
Device	Well
LP STD Vt + G STD Vt + LP High Vt + G High Vt + I/O (2.5V)	6 masks PW1V/ PW1V_DCO/ PW2V/ NW1V/ VTH_N/ VTH_P
LP STD Vt + G STD Vt + I/O (2.5V)	4 masks PW1V/ PW1V_DCO/ PW2V/ NW1V

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CLN55GP	Mask Requirements
Device	**Well**
STD Vt+ I/O (1.8V or 2.5V)	3 masks PW1V/PW2V/NW1V
STD Vt+ High Vt+ I/O (1.8V or 2.5V)	5 masks PW1V/PW2V/NW1V/VTH_N/VTH_P
STD Vt+ Low Vt+ I/O (1.8V or 2.5V)	5 masks PW1V/PW2V/NW1V/VTL_N/VTL_P
STD Vt+ High Vt+ Low Vt+ I/O (1.8V or 2.5V)	7 masks PW1V/PW2V/NW1V/ VTH_N/ VTH_P /VTL_N/VTL_P
STD Vt+ I/O (3.3V)	4 masks PW1V/ PW2V/ NW1V/ NW2V
STD Vt+ High Vt+ I/O (3.3V)	6 masks PW1V/ PW2V/ NW1V/ NW2V/ VTH_N/ VTH_P
STD Vt+ Low Vt+ I/O (3.3V)	6 masks PW1V/ PW2V/ NW1V/ NW2V/ VTL_N/ VTL_P
STD Vt+ High Vt+ Low Vt+ I/O (3.3V)	8 masks PW1V/ PW2V/ NW1V/ NW2V/ VTH_N/ VTH_P/ VTL_N/ VTL_P

CLN55LP/CMN55LP	Mask Requirements
Device	**Well**
STD Vt+ I/O (2.5V)	3 masks PW1V/PW2V/NW1V
STD Vt+ High Vt+ I/O (2.5V)	5 masks PW1V/PW2V/NW1V/VTH_N/VTH_P
STD Vt+ Low Vt+ I/O (2.5V)	5 masks PW1V/PW2V/NW1V/VTL_N/VTL_P
STD Vt+ High Vt+ Low Vt+ I/O (2.5V)	7 masks PW1V/PW2V/NW1V/ VTH_N/ VTH_P /VTL_N/VTL_P

CMN65	Mask Requirements	
Device	**Well**	
	CMN65LP	CMN65GP
STD Vt+ I/O (2.5V)	3 masks PW1V/ PW2V/ NW1V	
STD Vt+ High Vt+ I/O (2.5V)	5 masks PW1V/ PW2V/ NW1V/ VTH_N/ VTH_P	
STD Vt+ Low Vt+ I/O (2.5V)	5 masks PW1V/ PW2V/ NW1V/ VTL_N/ VTL_P	
STD Vt+ High Vt+ Low Vt+ I/O (2.5V)	7 masks PW1V/ PW2V/ NW1V/ VTH_N/ VTH_P / VTL_N/ VTL_P	
STD Vt+ I/O (3.3V)	4 masks PW1V/ PW2V/ NW1V/ NW2V	-
STD Vt+ High Vt+ I/O (3.3V)	6 masks PW1V/ PW2V/ NW1V/ NW2V/ VTH_N/ VTH_P	-
STD Vt+ Low Vt+ I/O (3.3V)	6 masks PW1V/ PW2V/ NW1V/ NW2V/ VTL_N/ VTL_P	-
STD Vt+ High Vt+ Low Vt+ I/O (3.3V)	8 masks PW1V/ PW2V/ NW1V/ NW2V/ VTH_N/ VTH_P/ VTL_N/ VTL_P	-

For the related CAD layer, please refer to section 3.1 and T-N65-CL-LE-001.

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3.7 Design Geometry Restrictions

3.7.1 Design Geometry Rules

Table 3.7.1

Rule No.	Description
G.1	The design grid must be an integer multiple of 0.005 μm except PO & CO layers inside the layer 186;5. 0.005 μm deviation is allowed for 45-degree polygon dimensions. DRC will not flag UBM/ CBD/PM/PM1/CB2/PM2/PPI layers
G.2	Shapes with acute angles between line segments are not allowed.
G.3	Only shapes that are orthogonal or on a 45-degree angle are allowed.
G.4	For the OPC layers, any edge of length < 1.0 x minimum width cannot have another adjacent edge of length < 1.0 x minimum width (Figure 3.7.1). The OPC layers: OD, PO, VTL_N, VTL_P, VTH_N, VTH_P, NP, PP, CO, M1, VIAx, Mx, My
G.5	Don't use the following GDS layer;datatype. They are reserved for tsmc internal mask making. Layer / Datatype / Example 6 / 161~165 / 6;161 17 / 161~165 / 17;161 31~40 / 161~165 / 31;161
G.6g[U]	For OD, PO, VTL_N, VTL_P, VTH_N, VTH_P, NP, PP, M1, Mx, My, all vertices and intersections of 45-degree polygon must be on an integer multiple of 0.005 μm except PO inside the layer 186;5.

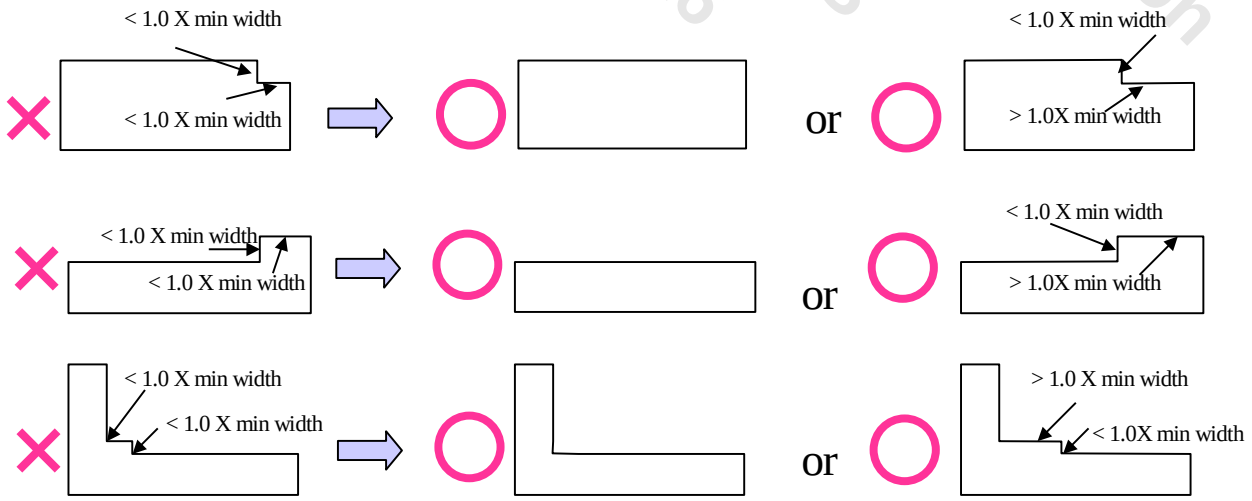

Figure 3.7.1 Illustration for G.4.

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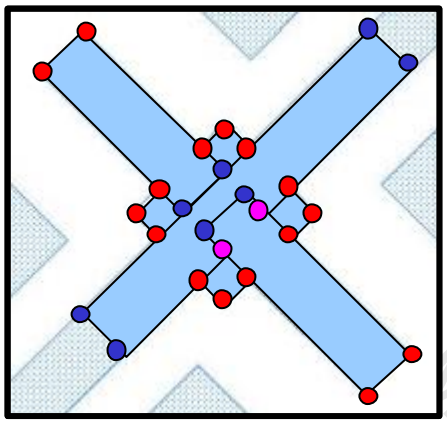

Figure 3.7.2 Illustration for G.6g.

3.7.1.1 DBU guideline

Recommend to use 1nm as layout database unit (DBU) when streaming out GDS. TSMC's technology files adopt 1nm DBU by default. If further DBU setting is considered, please consult it with TSMC for guidelines to modify default setting of TSMC's technology files.

3.7.2 OPC Recommendations and Guidelines

The following OPC recommendations are very important tips to reduce OPC and mask-making cycle time (or physical verification) and ensure the best silicon performance:

- **Make certain that the design is DRC clean (free of all DRC violations).**
- **Do not use circles, oval shapes, or logos of arbitrary geometry (Figure 3.7.3).** Use rectangular or 45-degree polygons to write words, logos, and other marks that are not part of the circuit.
- **Verify that all line ends are rectangular.**
- **Limit cell names to 64 or fewer characters.**
- **Use a well-organized, hierarchical layout structure.**

  Avoid redundant or excessive overlaps of polygons from two, or more than two, different cells or cell placements. For example, avoid forming a straight line from numerous cell placements, with each one contributing a little piece. Refer to the “Design Hierarchy Guidelines” section in this chapter.
- **Worse performance in the simulation of contour for the layout with small jog/zigzag (Figure 3.7.5).**
- **Using the commercial LPC tools or tsmc DFM LPC service, to identify the potential patterening marginalities (such as pinch or bridge) with process window, and then modify the layout.**

Rule No.	Description			Rule
OPC.R.1®	Recommended 45-degree edge length (Figure 3.7.4) for OPC friendly layout..	A	≥	0.27
OPC.R.2g	Avoid small jogs (Figure 3.7.5). It is recommended to use greater than, or equal to, half of the minimum width of each layer for each segment of a jog.			

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Figure 3.7.3 Logo Geometry Example

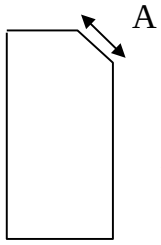

Figure 3.7.4 Illustration for OPC.R.1®

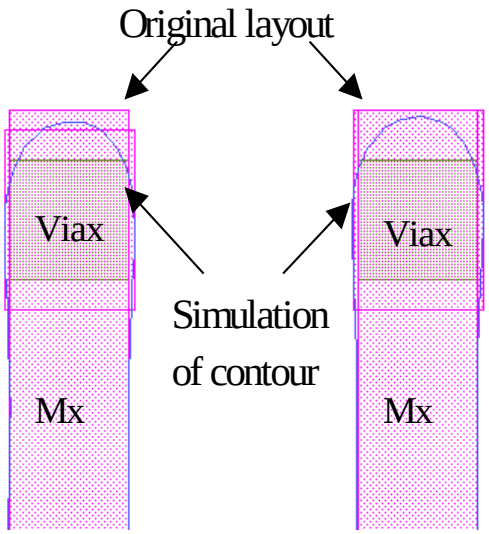

Figure 3.7.5 Simulation contour for the layout with and without small jog/zigzag. The simulation is Mx line and not well treated due to small jog/zigzag, and cause smaller Viax overlap.

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3.8 Design Hierarchy Guidelines

The style of the cell hierarchy in a design can significantly affect the following:

- OPC and mask-making cycle time
- Run time and memory usage of physical verification.

Following are the recommended practices:

- **Re-use design blocks as much as possible.**
  Do not create two different cells for the same device.
- **Whenever possible, avoid using *L*, *U*, or *ring* shapes.**
  For inevitable *ring* structures such as seal rings and power rings, use cells for holding each ring segment instead of drawing the whole ring at once. The same method applies to the *L* and *U* shapes.
- **Put everything as low in the cell hierarchy as possible.** Here are some examples:
  - Put all shapes required for defining a device or circuit into the same cell. An inverter cell, for example, should include NW, OD, PO, NP, and PP, as well as CO and M1 (for pins).
  - Avoid drawing a large shape to cover a whole circuit.
  - Place texts at the lowermost cell where devices can be formed.
  - For layout patches/revisions/ECOs, avoid changing device properties or metal connections at upper cells in the design hierarchy.
  - Draw within the cell the shapes required in TSMC's logic operations.
    Please consider all independent layers used in each rule logic operations and derived layer logic operations. For example, LDN.EX.1 applies to NP and OD2; therefore, NP should reside in the same cell as OD2.
- **Make certain each cell is DRC clean in a bottom-up construction of the cell hierarchy.**
  For example, when placing a contact in a cell, place M1 in that cell as well, with the required amount of M1.
- **Keep dummy fill geometry in a separate hierarchy from the main patterns and reduce the count of flattened dummy fill geometry as much as possible.**

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3.9 Chip Implementation and Tape Out Checklist

The following checklist is required to be completed prior to the tape out:

- **IP are correctly utilized in the design**
  - ✓ Pay attentions to the special orientation/direction (e.g. SRAM), guard ring or space keep-out requirements of placement.
  - ✓ Pay attentions to routing constrains in resistance matching, power net spacing, layers available for over block routing, layers allowed for dummy fill, and power connection/width.
  - ✓ To avoid using non-silicon proven library and IP, please pay attentions to the available library/IP validation status from TSMC Online (Design Portal → Library/IP).
  - ✓ It is highly recommended that do not modify or remove the IP (CAD 63;63) in the design.
- **The design passes signal/power/IR/ESD integrity analysis**
  - ✓ Simulations of all CKTs in setup time, hold time, and noise analysis under design operating corners or sign-off corners.
  - ✓ Analyses in leakage with considering statistical factor, total power consumption, power network robustness, static/dynamic IR, IO SSO meet design specifics over all operating corners.
  - ✓ Ensure all COs/Vias and metal lines meet EM lifetime requirement.
  - ✓ ESD/latch-up layout and design requirements have been met.
- **The design passes DRC**
  - ✓ Use the most update DRC command file version corresponding to the design rule document.
  - ✓ Need to choose the DRC options carefully & correctly.
  - ✓ Need to cover all the DRC, including latch-up, ESD, antenna, assembly check.
  - ✓ It is recommended to run full chip DRC if there is any layout change in cell level.
  - ✓ Any DRC violation needs to be reviewed by TSMC, to make sure no production concern.
- **The design passes LVS/ERC checks**
  - ✓ Use the most update LVS/ERC command file version corresponding to the SPICE document.
- **DFM services & requirements are recommended**
  - ✓ Utilize TSMC DFM layout enhancement utility to insert double vias and enlarge via enclosure.
  - ✓ Utilize TSMC dummy OD/PO/metal generation utilities to insert dummy patterns to meet pattern density requirements.
  - ✓ RC extraction by DFM-LPE to have accurate SPICE simulations in IP design.
  - ✓ The section 3.8 Design Hierarchy Guidelines have been considered.
- **Tape out information**
  - ✓ Make sure to have every “tape out required CAD layer” filled correctly in the TSMC i-tapeout system. Additionally, to correctly fill DRC-only CAD layers of the design is welcome.
  - ✓ It is highly recommended that the GDSII file taped out to TSMC contains IP information (CAD 63;63).

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4 Layout Rules and Recommendations

This chapter provides the following general layout information:

4.1 Layout Rule Conventions
4.2 Special Geometries Used in Physical Design Rules
4.3 Definition of Layout Geometrical Terminology
4.4 Minimum Pitches
4.5 CLN65 (Logic) Layout Rules and Guidelines

4.1 Layout Rule Conventions

Layout rules follow these conventions:

- Unless otherwise specified, all rules are of minimum dimension.
- The basic unit of measure is μm; the basic unit of area is μm^2.
- Process, product, and reliability yields are expected to be improved when designs are relaxed from minimum dimensions. Minimum dimensions showed only to be used to shrink the chip size or to improve the circuit performance.
- Design rules requiring exact dimensions ("=" in the rule tables) are not to be relaxed.
- Guideline is grouped by a separate table.
- DFM recommendations and guidelines are designated by a registered symbol ® or "g" after the rule number.
- A registered symbol "U" is marked after the rule number as the rule is not checked by DRC.
- Bracket usage in the rules should be noted carefully:
  - Parentheses ( ) are used for explanation.
  - Square brackets [ ] are used for certain conditions.
  - Curved brackets { } are used to indicate that an operation is performed.

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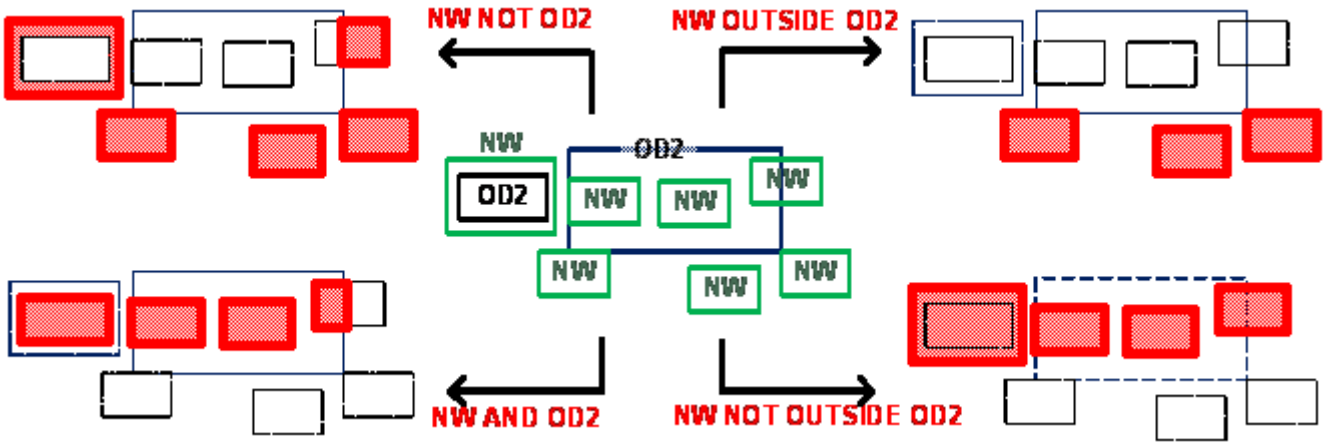
4.2 Special Geometries Used in Physical Design Rules

4.2.1 Derived Geometries

Term	Definition
ACTIVE	N+ACTIVE OR P+ACTIVE
ALLOD	OD OR DOD
Butted_STRAP	STRAP TOUCH ACTIVE
FIELD	NOT OD
FIELD PO	PO NOT OD
GATE	PO AND OD
N+ACTIVE	(NP AND OD) NOT NW
N+OD	NP AND OD
NW STRAP	(NP AND OD) AND NW
NW1V	1.NW NOT OD2 (Note 1) 2.NW OUTSIDE OD2 (Note 1~2)
NW2V	1.NW AND OD2(Note 1) 2.NW NOT OUTSIDE OD2 (Note 1~2)
NWROD	(NW INTERACT NWDMY) INTERACT RPO
NWRSTI	(NW INTERACT NWDMY) NOT INTERACT RPO
PW	NOT NW
OD2	OD_18, OD_25, OD_33
P+ACTIVE	(PP AND OD) AND NW
P+OD	PP AND OD
PW STRAP	(PP AND OD) NOT NW
STRAP	NW STRAP OR PW STRAP

Table note:

1. For DRC recognition purpose, NW covered by OD2 is necessary for NW applied by voltage greater than core voltage. It is very important to manually take care of NW to NW space ≥ 1.2um if NW cannot be covered by OD2 and at least one NW is applied by voltage greater than core voltage.
2. If the switch, NW_SUGGESTED, turns ON (default), DRC will not only run NW.S.3 and NW.S.4 but also additionally check “SUGGESTED.NW.S.3_NW.S.4” by recognizing NW1V by {NW OUTSIDE OD2} and NW2V by {NW NOT OUTSIDE OD2}. If it turns OFF, DRC only checks NW.S.3 and NW.S.4.



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4.2.2 Special Definition

Term	Definition
NW	N-WELL
RW	PW inside DNW
MOS	Transistor structure consisting of a source, a drain, and a gate.
NMOS	N type MOS
PMOS	P type MOS
HV NMOS	N type HVMOS
HV PMOS	P type HVMOS
DOD	Dummy OD
DPO	Dummy PO
DMx	Dummy Metal
DMx_O	OPC dummy metal. The rules of DMx_O are the same as real metal, Mx.
Chip edge	“Chip” doesn’t include seal ring and assembly isolation.
Assembly isolation	The region between the seal ring and chip edge
End-cap	The PO extension of a transistor gate in the width direction onto the field.
CUP	Wire bond pad design for Circuit Under Pad
Guard ring	Complete un-broken ring-type OD and M1 with CO as many as possible, connected to Vdd or Vss.
N+ guard-ring	Complete un-broken ring-type (NP AND OD) and M1 with CO as many as possible, connected to Vdd.
P+ guard-ring	Complete un-broken ring-type (PP AND OD) and M1 with CO as many as possible, connected to Vss.
HV NMOS cluster	A group of HV NMOSs
HV PMOS cluster	A group of HV PMOSs

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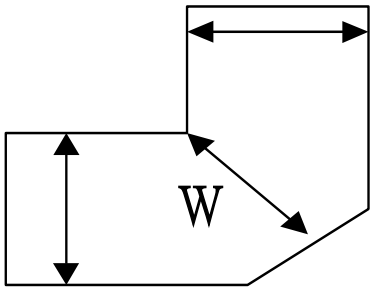
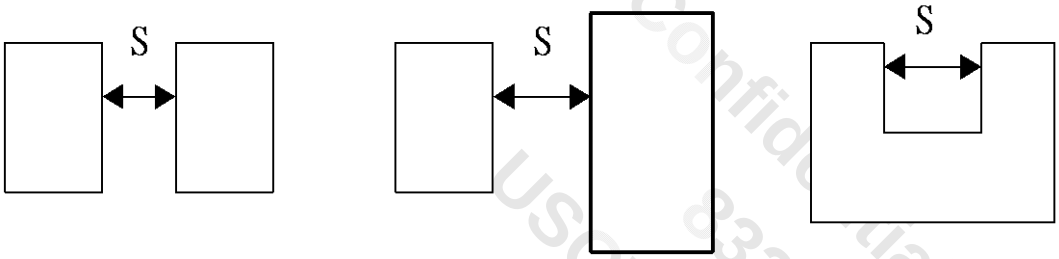
4.3 Definition of Layout Geometrical Terminology

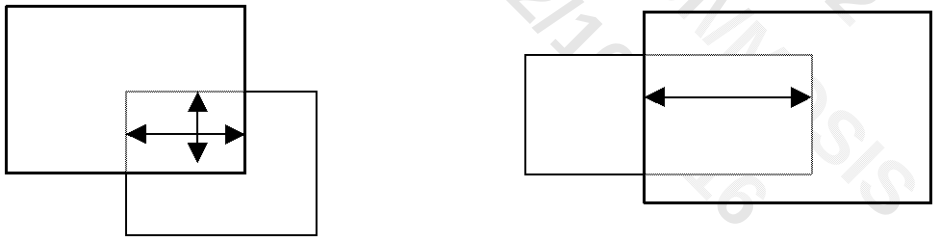
Width: Distance of interior-facing edge for single layer. (W)



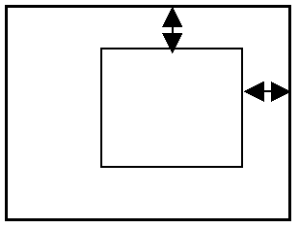
Space: Distance of exterior-facing edge for one or two layer (S)



Overlap: Distance of interior-facing edge for two layers (O)



Enclosure: Distance of inside edge to outside edge (Fully inside) (EN)



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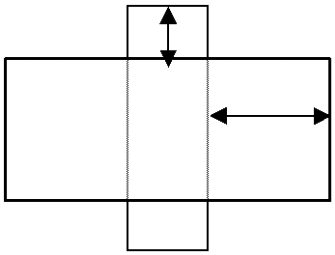
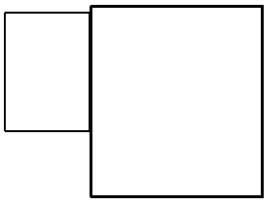
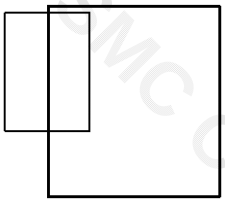
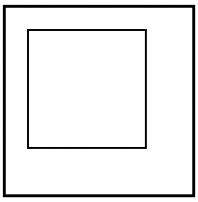
Extension: Distance of inside edge to outside edge (EX)



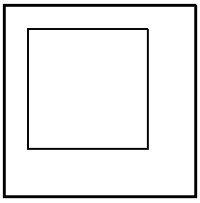
Interact with:



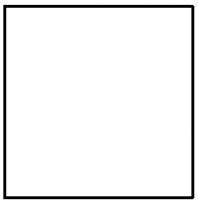




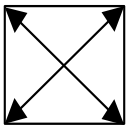
Inside:



Outside:



AREA (A):



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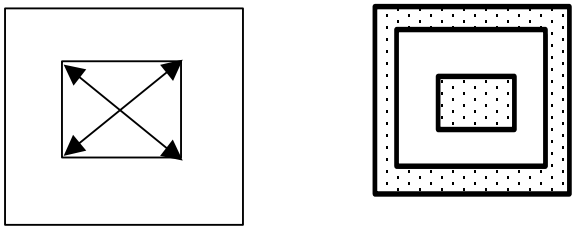
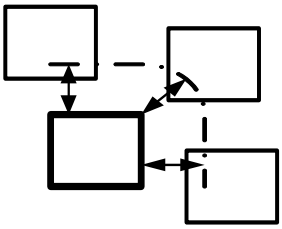
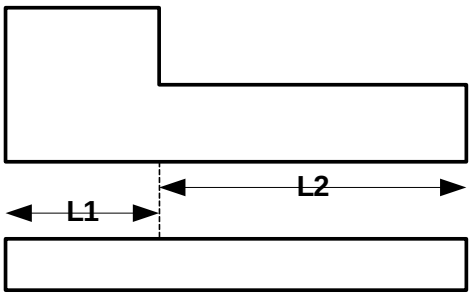
ENCLOSED Area (A):



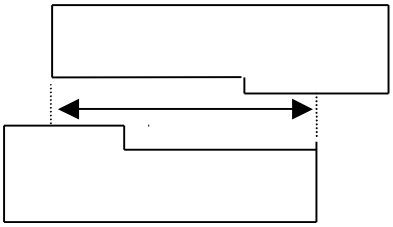
3-Neighboring:



Projection:
Individual projection (L1, L2)
Union projection (L1 + L2)



Parallel run length:



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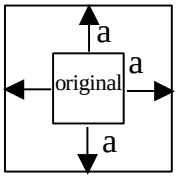
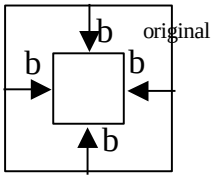
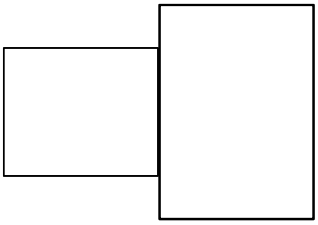
Size up a



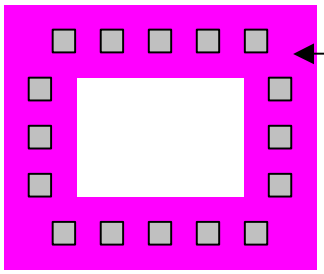
Size down b



Butted

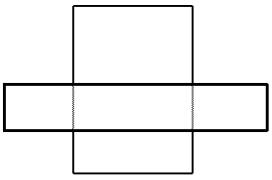


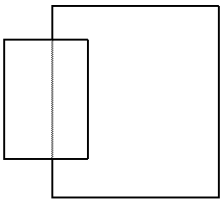
Guardring

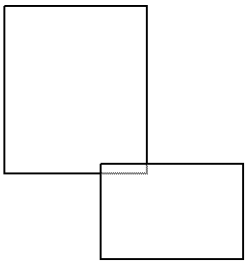


Ring-type OD and M1 with CO
as many as possible

Cut







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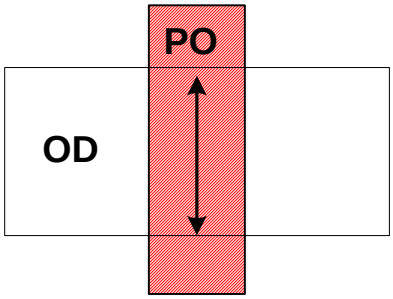
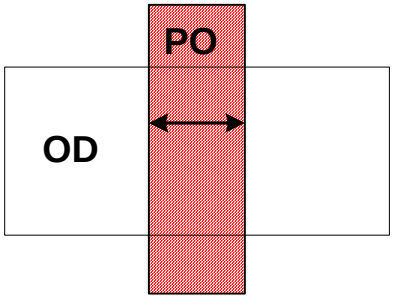
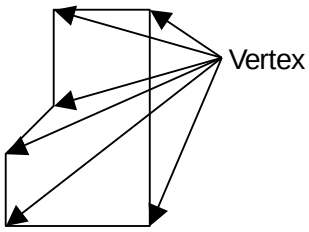
Channel width



Channel length



Vertex: Polygon whose edge form an angle



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4.4 Minimum Pitches

Layer	CLN65G/LP/HS (Unit: µm)
OD interconnect pitch	0.19 (W/S=0.08/0.11)
OD interconnect width	0.08
OD transistor pitch	0.23 (W/S=0.12/0.11)
PO interconnect pitch (on STI)	0.18 (W/S=0.06/0.12)
PO interconnect width	0.06
PO transistor pitch (on OD)	0.19 (W/S=0.06/0.13)
Minimum length of a transistor	0.06
Minimum width of a transistor	0.12
N+/P+ spacing	0.32
M1 pitch	0.18 (W/S=0.09/0.09)
Mx pitch	0.20 (W/S=0.10/0.10)
My pitch	0.40 (W/S=0.20/0.20)
Mz pitch	0.80 (W/S=0.40/0.40)
Mr pitch	1.0 (W/S=0.5/0.5)
Mu pitch	4.0 (W/S=2.0/2.0)
CTM pitch	2.8 (W/S=2.0/0.8)
CBM pitch	4.8 (W/S=2.8/2.0)
CO pitch	0.20 (W/S=0.09/0.11)
CO pitch in different net	0.21 (W/S=0.09/0.12)
CO pitch in different net & parallel	0.23 (W/S=0.09/0.14)
CO ≥ 3 neighboring pitch	0.23 (W/S=0.09/0.14)
VIAx pitch	0.20 (W/S=0.10/0.10)
VIAx pitch in different net	0.23 (W/S=0.10/0.13)
VIAx ≥ 3 neighboring pitch	0.23 (W/S=0.10/0.13)
VIAy pitch	0.40 (W/S=0.20/0.20)
VIAy ≥ 3 neighboring pitch	0.45 (W/S=0.20/0.25)
VIAz pitch	0.70 (W/S=0.36/0.34)
VIAz ≥ 3 neighboring Pitch	0.90 (W/S=0.36/0.54)
VIAr pitch	0.90 (W/S=0.46/0.44)
VIAr ≥ 3 neighboring pitch	1.12 (W/S=0.46/0.66)
VIAu pitch	0.70 (W/S=0.36/0.34)
VIAu ≥ 3 neighboring Pitch	0.90 (W/S=0.36/0.54)

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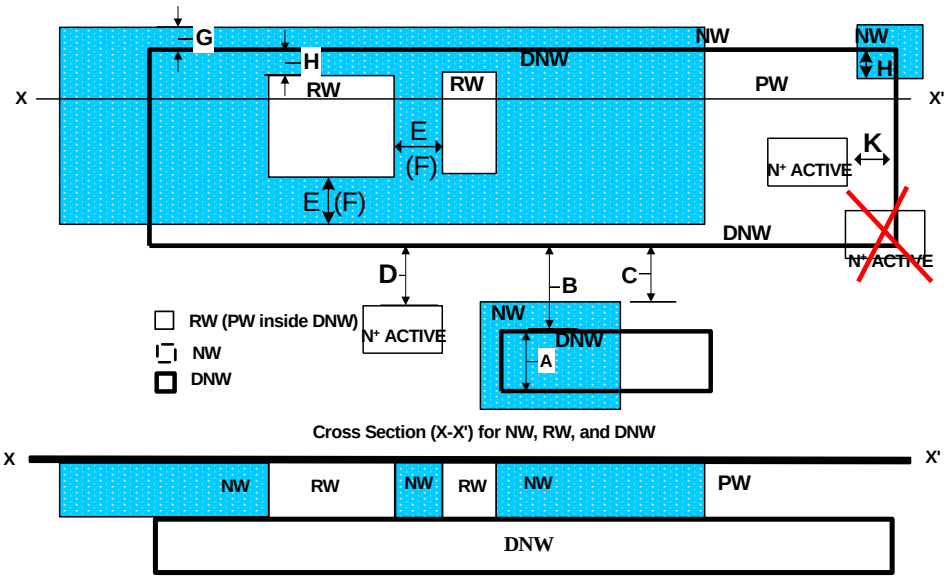
4.5 CLN65(Logic) Layout Rules and Guidelines

4.5.1 Deep N-Well (DNW) Layout Rules (Mask ID: 119) [Optional]

The purpose of DNW is to get PW isolated from substrate. DNW should also be drawn under NW for better latch-up immunity.

Rule No.	Description	Label		Rule
DNW.W.1	Width	A	≥	3.0
DNW.S.1	Space	B	≥	3.5
DNW.S.2	Space to NW with different potential	C	≥	2.5
DNW.S.3	Space to {N+ACTIVE outside DNW} except dummy TCD region (TCDDMY)	D	≥	1.65
DNW.S.4	RW space to {RW OR PW} with different potential	E	≥	1.0
DNW.S.5	{RW OR PW} space to {RW INTERACT OD2} with different potential	F	≥	1.2
DNW.EN.1®	Recommended enclosure by NW for better noise isolation	G	≥	1.0
DNW.EN.3	Enclosure of N+ACTIVE	K	≥	0.56
DNW.O.1	Overlap of NW	H	≥	0.4
DNW.R.2	RW is the PW in DNW			
DNW.R.3 U	Keep {NW INTERACT DNW} and PW in reverse bias			
DNW.R.4U	{NW INTERACT DNW} must be at the same potential			
DNW.R.5	DNW cut N+ACTIVE is not allowed			
DNW.R.6g	Recommend not using floating RW unless necessary, to avoid unstable device performance. DRC can flag RW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.			
DNW.R.7	Maximum cumulative area ratio of DNW to {(NMOS/P-VAR core gates) OUTSIDE DNW} [connects to {P+ ACTIVE INSIDE {NW INTERACT DNW}}] This rule is checked by the ANTENNA DRC command file.		≤	500000

DNW



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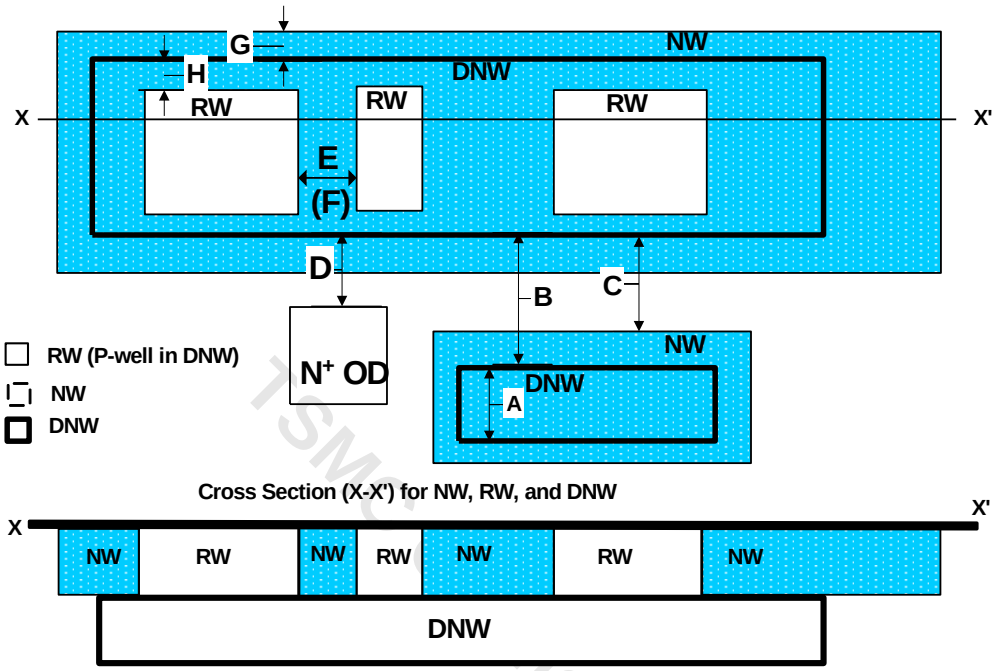
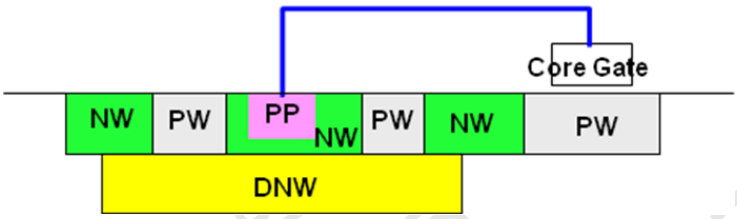


DNW.R.7



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4.5.2 Gate Oxide and Diffusion (OD) Layout Rules (Mask ID: 120)

Rule No.	Description	Label		Rule
OD.W.1	Width	A	≥	0.08
OD.W.2	Width of MOS (≤ 1.2V) [for core device]	B	≥	0.12
OD.W.2®	Recommended width of MOS (≤ 1.2V) [for core device]	B	≥	0.15
OD.W.3	Width of MOS (> 1.2V to ≤ 3.3V) [for I/O device]	C	≥	0.4
OD.W.4	Width of 45-degree bent OD Please make sure the vertex of 45-degree pattern is on 5nm grid (refer to the guideline, G.6g^{U}, in section 3.7)	D	≥	0.18
OD.S.1	Space	E	≥	0.11
OD.S.1®	Recommended minimum OD space to reduce the short possibility caused by particle	E	≥	0.14
OD.S.2	Space (inside OD2)	F	≥	0.18
OD.S.3	Space of two ODs (width (W) > 0.15 µm), if the parallel run length (L) ≥ 0.2 µm	G	≥	0.13
OD.S.3.1	Space to OD (width (W) > 0.15 µm), if the parallel run length (L) ≥ 0.2 µm	G1	≥	0.125
OD.S.4	Space to 45-degree bent OD	H	≥	0.18
OD.S.5	Space between two segments of a U-shape or an O-shape OD (notch only)	I	≥	0.18
OD.S.6®	Recommended space to OD [OD area > 4,000,000 µm²].	N	≥	0.35
OD.A.1	Area	J	≥	0.054
OD.A.2	Enclosed area	K	≥	0.085
OD.L.1	Maximum length of {ACTIVE (source) [width < 0.15 µm] interacts with butted_STRAP}	O	≤	0.5
OD.L.2	Maximum OD length [OD width is < 0.15 µm] between two contacts as well as between one contact and the OD line end	M	≤	25
OD.DN.1	{OD OR DOD} density across full chip		≥	25%
			≤	75%
OD.DN.2	{OD OR DOD} local density		≥	20%
			≤	80% (outside OD2)
			≤	90%
OD.DN.3	{OD OR DOD} local density inside ODBLK		≥	20%
			≤	80% (outside OD2)
			≤	90%
	1. OD.DN.2 and OD.DN.3 are checked over any 150 µm x 150 µm window (stepping in 75 µm increments). 2. (outside OD2) means the overlapped width between the checking window and OD2 layer is smaller than 37.5 µm. 3. For OD.DN.2/OD.DN.3, the following regions can be excluded: o (CB sizing 2) for high speed/RF products for 20% rule o NWDMY/FW/LMARK/LOGO/INDDMY for 20% rule o Chip corner stress relief and seal ring for 20%/80%/90% rule 4. OD.DN.2 is applied while the width of ((checking window NOT the item 3) ≥ 37.5 µm. 5. OD.DN.3 must be followed for every defined ODBLK region. This rule is only applied while the width of ((checking window AND ODBLK) NOT item 3) ≥ 37.5 µm.			
OD.R.1	OD must be fully covered by {NP OR PP} except for {DOD OR NWDMY}			
DOD.R.1*	DOD is a must. DOD CAD layer (TSMC default, 6;1) must be different from OD's.			
OD.L.2g^{U}	It is strongly suggested to limit the max interconnect length (M) to be as short as possible to avoid high Rs variation by salicidation.			

Table Notes:

* In order to meet the extremely tight requirement in terms of process control for STI etch, polish as well as channel length definition (inter-level dielectric (ILD) planarization), you must fill the DOD globally and uniformly even if the originally drawn OD already satisfies the required OD density rule (OD.DN.1~OD.DN.3). It is recommended to manually add DOD uniformly inside regions covered by the ODBLK layer, to gain better process window and electrical performance.

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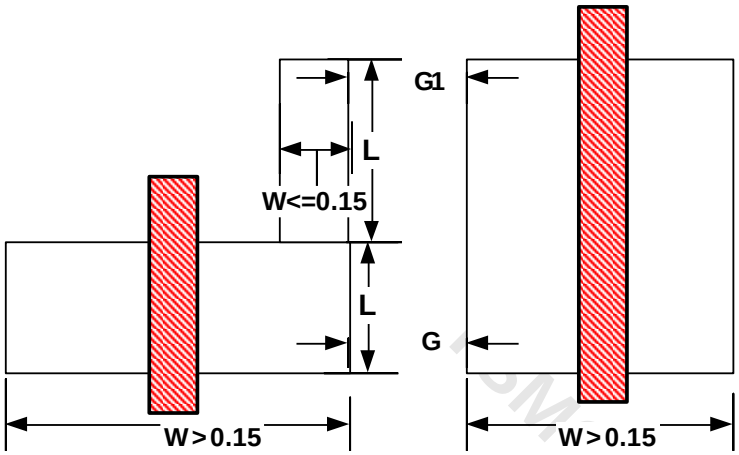
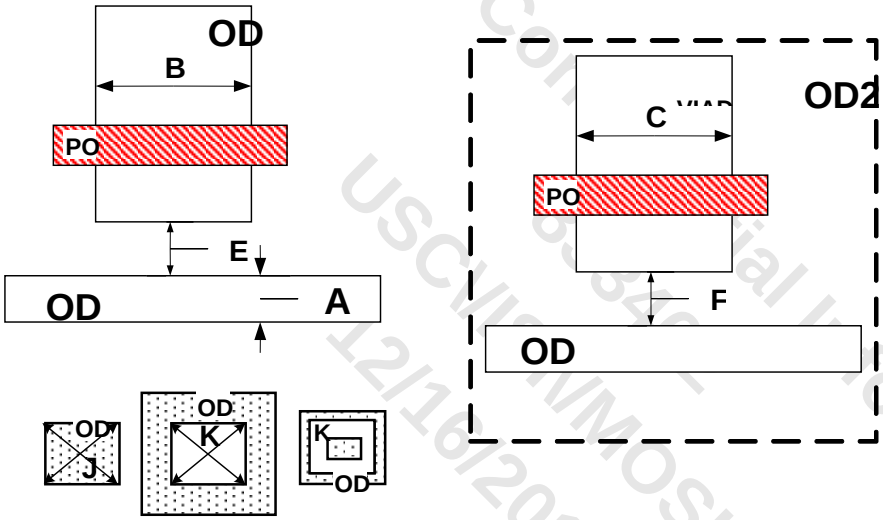
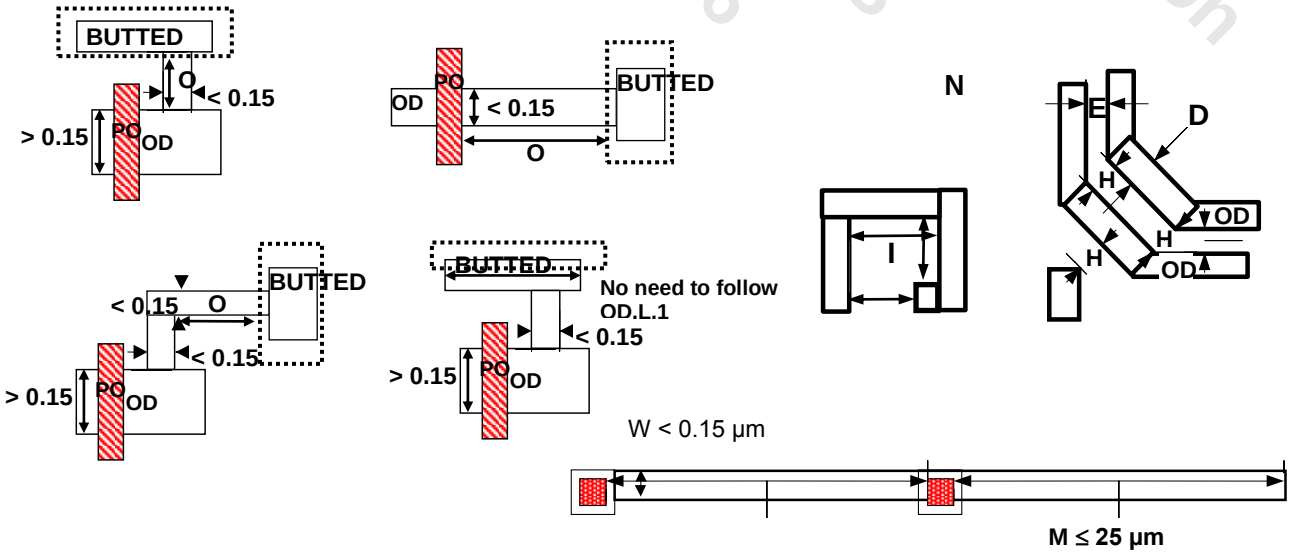
OD





OD (>4,000,000 μm^2)



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4.5.3 N-Well (NW) Layout Rules

Rule No.	Description	Label		Rule
NW.W.1	Width	A	≥	0.47
NW.S.1	Space	C	≥	0.47
NW.S.2	Space of two NW1V with different potentials (*)	D	≥	1.00
NW.S.3	NW1V space to NW2V with different potentials (*)	E	≥	1.20
NW.S.4	Space of two NW2V with different potentials (*)	F	≥	1.20
NW.S.5	Space to PW STRAP	G	≥	0.16
NW.S.6	Space to N+ACTIVE except dummy TCD region (TCDDMY)	H	≥	0.16
NW.S.7	Space to {N+ACTIVE INTERACT OD2}	I	≥	0.31
NW.EN.1	Enclosure of NW STRAP	K	≥	0.16
NW.EN.2	Enclosure of P+ACTIVE	L	≥	0.16
NW.EN.3	Enclosure of {P+ACTIVE INTERACT OD2}	M	≥	0.31
NW.A.1	Area	O	≥	0.64
NW.A.3	Area [one of the edge length < 0.8μm]	Q	≥	1
NW.A.2	Enclosed area	P	≥	0.64
NW.A.4	Enclosed area [one of the enclosed edge length < 0.8μm]	R	≥	1
NW.R.1g	Recommended not using floating well unless necessary, to avoid unstable device performance. DRC can flag both NW is not with CO in NPOD and PW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.			
NW.R.2^{U}	OD2 must overlap NW [applied by voltage greater than core voltage]			

Table notes:

1. (*): DRC implementation is on different nets.
2. For DRC recognition purpose, NW covered by OD2 is necessary for NW applied by voltage greater than core voltage. It is very important to manually take care of NW to NW space ≥ 1.2um if NW cannot be covered by OD2 and at least one NW is applied by voltage greater than core voltage.
3. If the switch, NW_SUGGESTED, turns ON (default), DRC will not only run NW.S.3 and NW.S.4 but also additionally check “SUGGESTED.NW.S.3_NW.S.4” by recognizing NW1V by {NW OUTSIDE OD2} and NW2V by {NW NOT OUTSIDE OD2}. If it turns OFF, DRC only checks NW.S.3 and NW.S.4.

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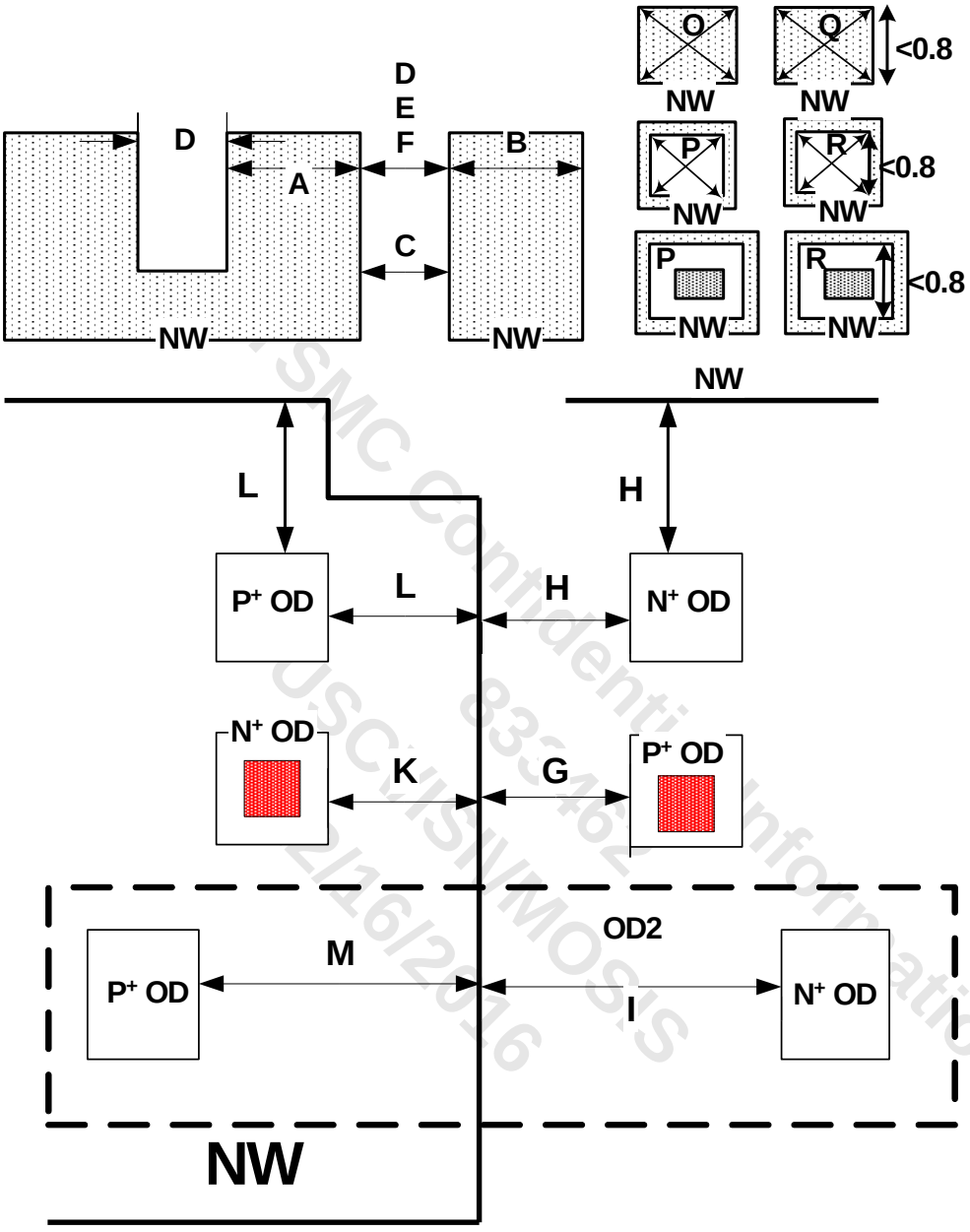
NW



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4.5.4 N-Well Resistor Within OD (NWROD) Layout Rules

Rule No.	Description	Label		Rule
NWROD.W.1	Width	A	≥	1.8
NWROD.S.1	Space to NWROD or to NW	B	≥	1.2
NWROD.S.2	Space to RPO	C	≥	0.3
NWROD.S.3®	Recommended RPO space to CO in NW resistor within OD for SPICE simulation accuracy	G	=	0.3
NWROD.EN.1	Enclosure by OD	D	≥	1.0
NWROD.EN.2	Enclosure of CO	E	≥	0.3
NWROD.O.1	RPO overlap of NP. Use exact value (0.4um) on sides touching NWDMY.	F	=	0.4
NWROD.O.2	{OD AND NWDMY} overlap of {NP, PP, VTH_N, VTH_P, VTL_N, or VTL_P} (all implant layers except NW) is not allowed.			
NWROD.R.1®	Recommended length/width ≥ 5, length ≥ 20 in NW resistor within OD for SPICE simulation accuracy (length/width is un-checkable).			
NWROD.R.3g	Recommended to use rectangle shape resistor for the SPICE simulation accuracy. DRC can flag {NWDMY AND NW} is not a rectangle.			
NWROD.R.4	Only one NW in NWROD is allowed in one OD.			
NWROD.R.5	Only two NPs in NWROD is allowed in one OD.			
NWROD.R.6	Only two RPO holes (Sailcide) in NWROD are allowed in same OD			
NWROD.R.7	For U-shape or S-shape NWROD, both OD and NW must be U-shape or S-shape and the OD edge must be parallel to the NW edge. DRC can only flag the pattern without OD space while 2 edges of NW [NW space or notch <= 5 um] parallel run length > 0 um.			

Table Notes:

The mean value and deviation of an N-Well resistor will depend on the layout and dimension.

Dummy layer NWDMY is needed for DRC and LVS.

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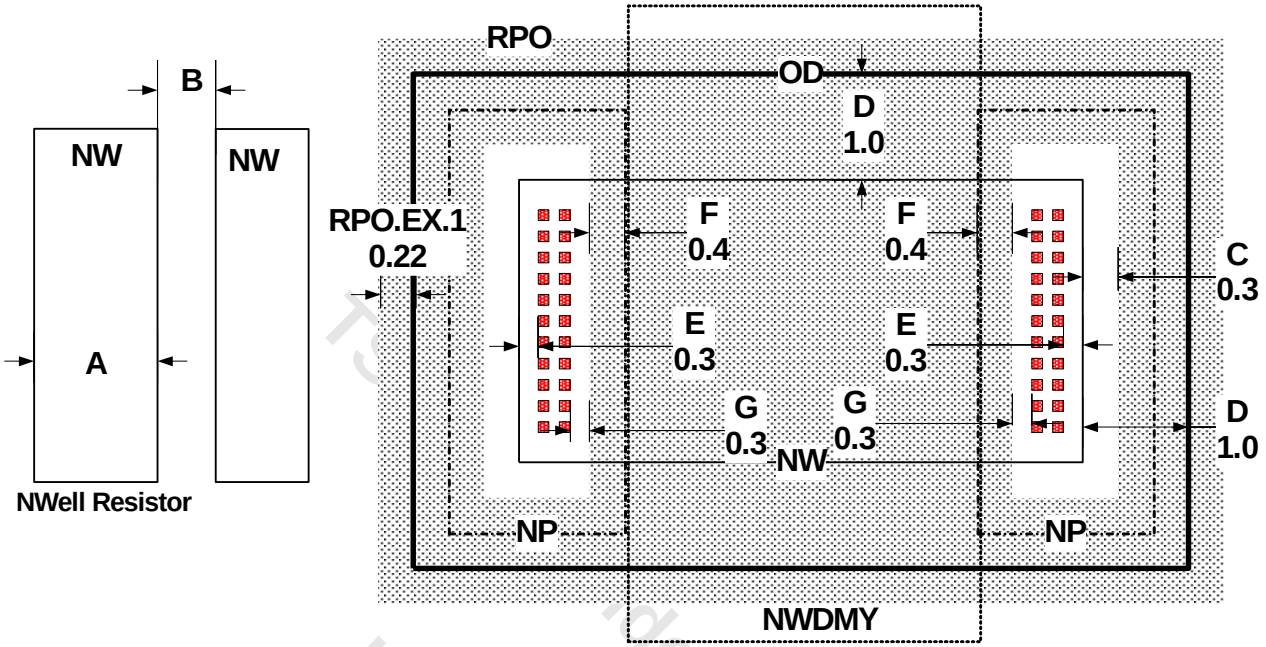
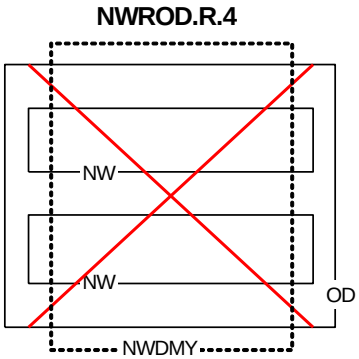
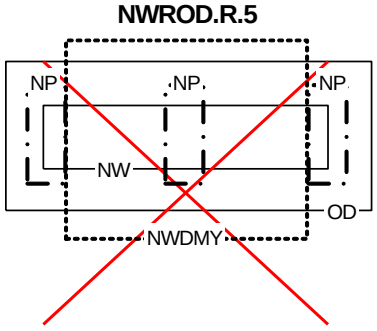
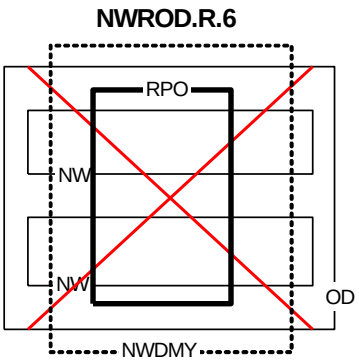
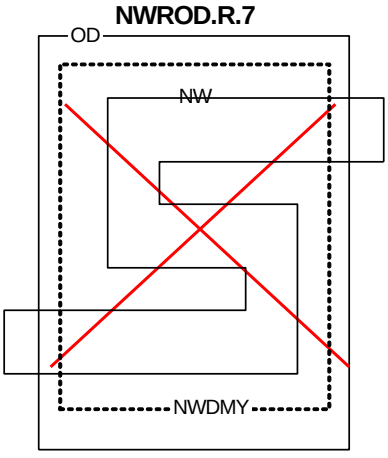
NWROD

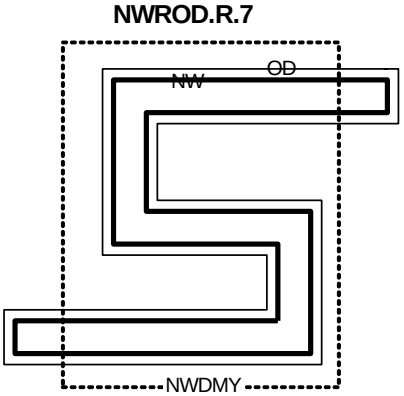


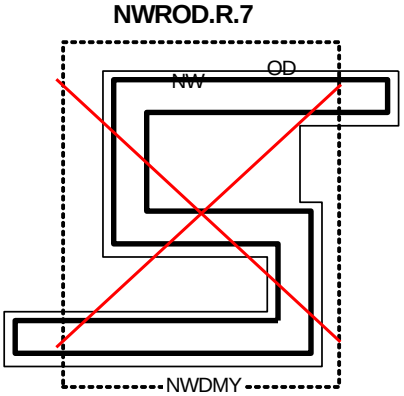












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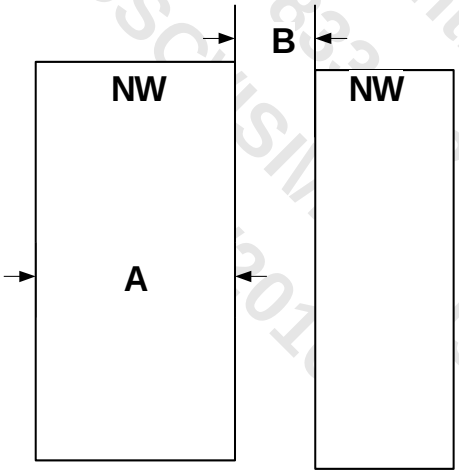
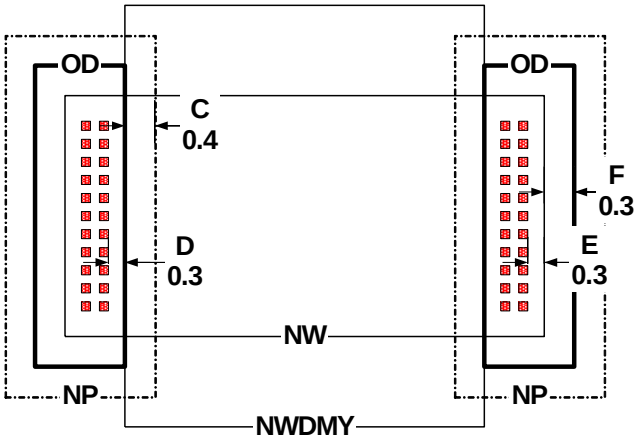
4.5.5 N-Well Resistor Under STI (NWRSTI) Layout Rules

Rule No.	Description	Label		Rule
NWRSTI.W.1	Width	A	≥	1.8
NWRSTI.S.1	Space to NWRSTI or to NW	B	≥	1.2
NWRSTI.EN.1	NP enclosure of OD	C	≥	0.4
NWRSTI.EN.2	OD enclosure of CO	D	≥	0.3
NWRSTI.EN.2®	Recommended OD enclosure of CO in NW resistor under STI for SPICE simulation accuracy	D	=	0.3
NWRSTI.EN.3	Enclosure of CO	E	≥	0.3
NWRSTI.EX.1	OD extension on NWRSTI	F	≥	0.3
NWRSTI.O.1	{NP INTERACT NWDMY} overlap of {PP, VTH_P, or VTL_P} (all p-type implant layers) is not allowed			
NWRSTI.R.1®	Recommended length/width ≥ 5, length ≥ 20 in NW resistor within OD for SPICE simulation accuracy (length/width is un-checkable).			
NWRSTI.R.3g	Recommended to use rectangle shape resistor for the SPICE simulation accuracy. DRC can flag {NWDMY AND NW} is not a rectangle.			

NWRSTI



NWell Resistor



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4.5.6 Native Device (NT_N) Layout Rules

NT_N, Native NMOS Blocked Implant Definition

This layer is used to block NW and PW implant. If you use native NMOS devices in a circuit design, use this drawn layer with NW to generate PW.

Rule No.	Description	Label		Rule
NT_N.W.1	Width	A	≥	0.47
NT_N.W.2	Channel length of core native device [for G/GP/(G in N65LPG process)]	B	≥	0.20
NT_N.W.2.1	Channel length of core native device [for N65LP/N65ULP/(LP in N65LPG process)]	B	≥	0.30
NT_N.W.2.2	Channel length of core native device [for N65LP/N65ULP/(LP in N65LPG process) with limited E and M (E<=1um, M<=0.5um)]	B	≥	0.20
NT_N.W.2.3	Channel length of core native device [Only for N55LP]	B	≥	0.20
NT_N.W.3	Channel length of 2.5V or 3.3V native device	C	≥	1.20
NT_N.W.4	Channel length of 1.8V native device	D	≥	0.8
NT_N.W.5	Channel width	E	≥	0.5
NT_N.S.1	Space	F	≥	0.47
NT_N.S.2	Space to [Active outside NT_N]	G	≥	0.38
NT_N.S.3	Space to NW	H	≥	1.20
NT_N.EN.1	Enclosure of N+OD.	I	≥	0.26
			≤	0.285
NT_N.EX.1	PO extension on {OD inside NT_N} (PO endcap)	J	≥	0.35
NT_N.A.1	Area	K	≥	0.64
NT_N.A.3	Area [one of the edge length < 0.8μm]	N	≥	1.0
NT_N.A.2	Enclosed area	L	≥	0.64
NT_N.A.4	Enclosed area [one of the enclosed edge length < 0.8μm]	O	≥	1.0
NT_N.R.1	Overlap of {NW OR DNW} is not allowed			
NT_N.R.2	P+ Gate is not allowed in NT_N			
NT_N.R.3	Only one OD region is allowed in NT_N ● except NMOS capacitors with the same potential. ● You have to draw a NCap_NTN layer to cover the NMOS capacitors. The NCap_NTN enclosure of OD have to be ≥ 0um. ● DRC also flags NCap_NTN and OD, which is outside of the NCap_NTN, in the same NT_N.			

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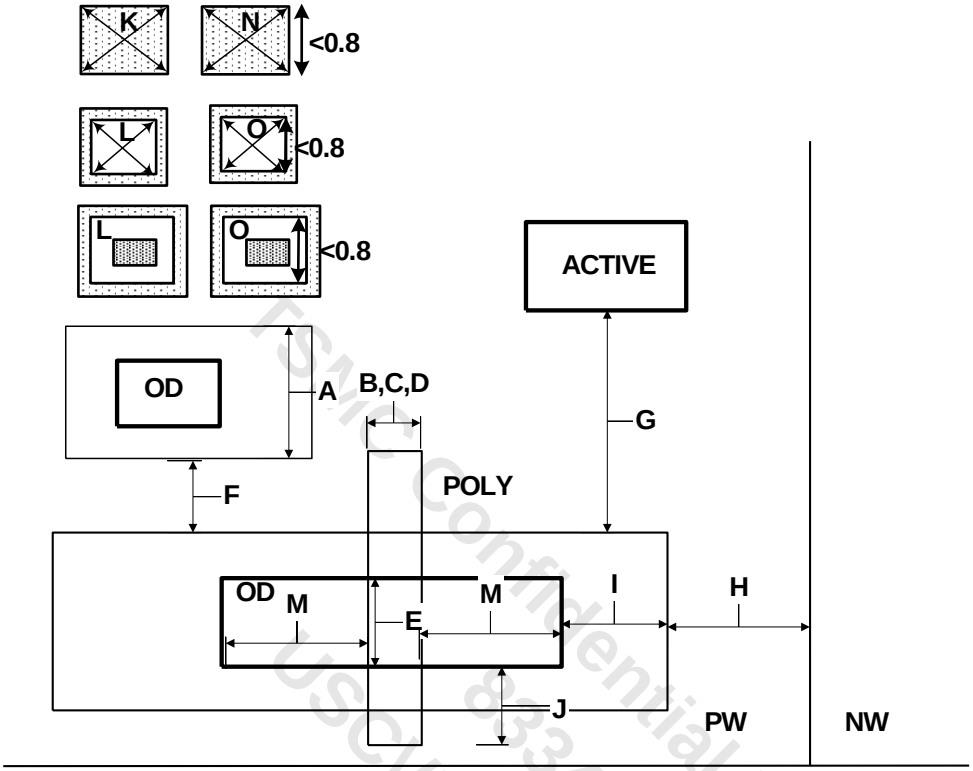
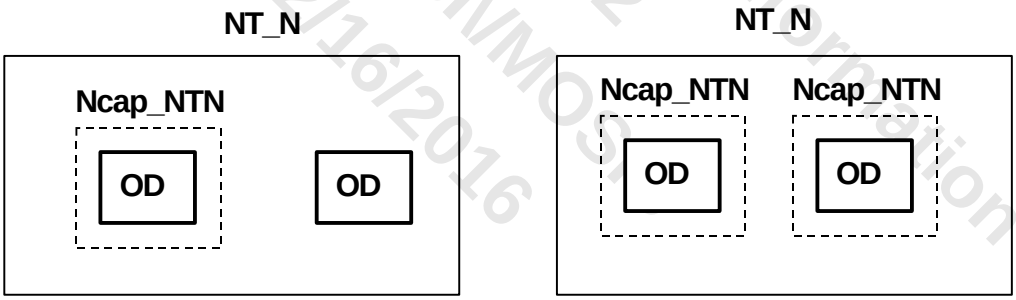
NT_N



NT_N.R.3



Prohibited **Allowed**

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4.5.7 Thick Oxide (OD2) Layout Rules (Mask ID: 152)

Define thick oxide area of 1.8V or 2.5V or 3.3V I/O transistors.

The OD_33 layer (CAD layer: 15) is used for 3.3V gate oxide area.

The OD_25 layer (CAD layer: 18) is used for 2.5V gate oxide area.

The OD_18 layer (CAD layer: 16) is used for 1.8V gate oxide area.

OD2 refers to any thick oxide device, for example, OD2 = OD_18, OD_25, OD_33.

Rule No.	Description	Label		Rule
OD2.W.1	Width	A	≥	0.47
OD2.W.2	Width of {OD2 OR (NW OR NT_N)}	L	≥	0.47
OD2.S.1	Space	B	≥	0.47
OD2.S.2	Space to {ACTIVE OR GATE}	C	≥	0.27
OD2.S.3	Space to 1.0V or 1.2V GATE in S/D direction.	D	≥	0.34
OD2.S.4	Space to NW. Space = 0 is allowed.	E	≥	0.47
OD2.S.5	Space of {NW NOT OD2}	M	≥	0.47
OD2.S.6	Space of {NW AND OD2}	O	≥	0.47
OD2.S.7	Space of {OD2 NOT (NW OR NT_N)}	N	≥	0.47
OD2.EN.1	Enclosure of 1.8V or 2.5V or 3.3V Gate in S/D direction.	G	≥	0.34
OD2.EX.1	NW extension on OD2. Extension = 0 is allowed.	H	≥	0.47
OD2.EX.2	Extension on NW. Extension = 0 is allowed.	I	≥	0.47
OD2.EX.3	Extension on {ACTIVE OR GATE}	J	≥	0.27
OD2.O.1	Overlap of NW. Overlap = 0 is allowed.	K	≥	0.47
OD2.R.1	OD_18, OD_25 and OD_33 cannot be used on same die.			
OD2.R.2[U]	If the OD is shared by core and IO, the OD must be same potential			

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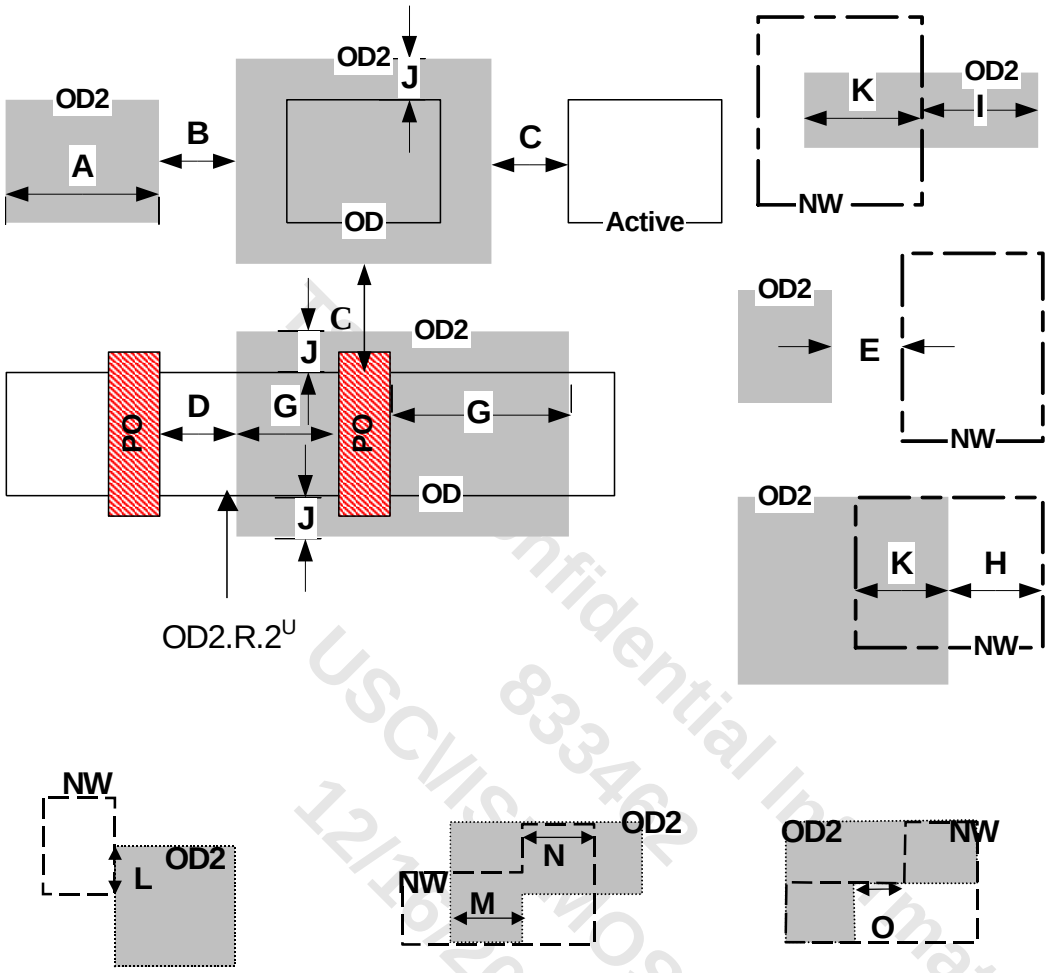
OD2



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4.5.8 Dual Core Oxide (DCO) Rules Layout Rules (MASK ID:153)

DCO is a layer to cover G core device in N65LPG process.

Rule No.	Description	Label		Rule
DCO.W.1	Width	A	≥	0.4
DCO.S.1	Space	B	≥	0.4
DCO.S.2	Space to ACTIVE	C	≥	0.055
DCO.S.3	Space to LP (core 1.2V) Gate in S/D direction.	D	≥	0.185
DCO.S.4	Space to LP (core 1.2V) Gate in end-cap direction.	D1	≥	0.16
DCO.S.5	Space to NW. Space = 0 is allowed.	E	≥	0.18
DCO.S.6	Space to OD2. Space = 0 is allowed.	F	≥	0.4
DCO.EN.1	Enclosure of G (core 1.0V) Gate in S/D direction.	G	≥	0.185
DCO.EN.2	Enclosure of G (core 1.0V) Gate in end-cap direction.	G1	≥	0.16
DCO.EX.1	NW extension on DCO. Extension = 0 is allowed.	H	≥	0.18
DCO.EX.2	Extension on NW. Extension = 0 is allowed.	I	≥	0.18
DCO.EX.3	Extension on ACTIVE [without Gate]	J	≥	0.055
DCO.A.1	Area	M	≥	1.2
DCO.A.2	Enclosed area	N	≥	1.2
DCO.O.1	Overlap of NW. Overlap = 0 is allowed.	K	≥	0.18
DCO.R.1[U]	If the OD is shared by G and LP, the OD must be the same potential.			
DCO.R.2	Overlap of OD2 is not allowed			
DCO.R.3	RH cut DCO is not allowed			
DCO.R.4	Point touch of corners is allowed [width ≥ 0.4μm].			
DCO.R.5	One-track (0.2μm) overlap / space are allowed [width ≥ 0.4μm].			

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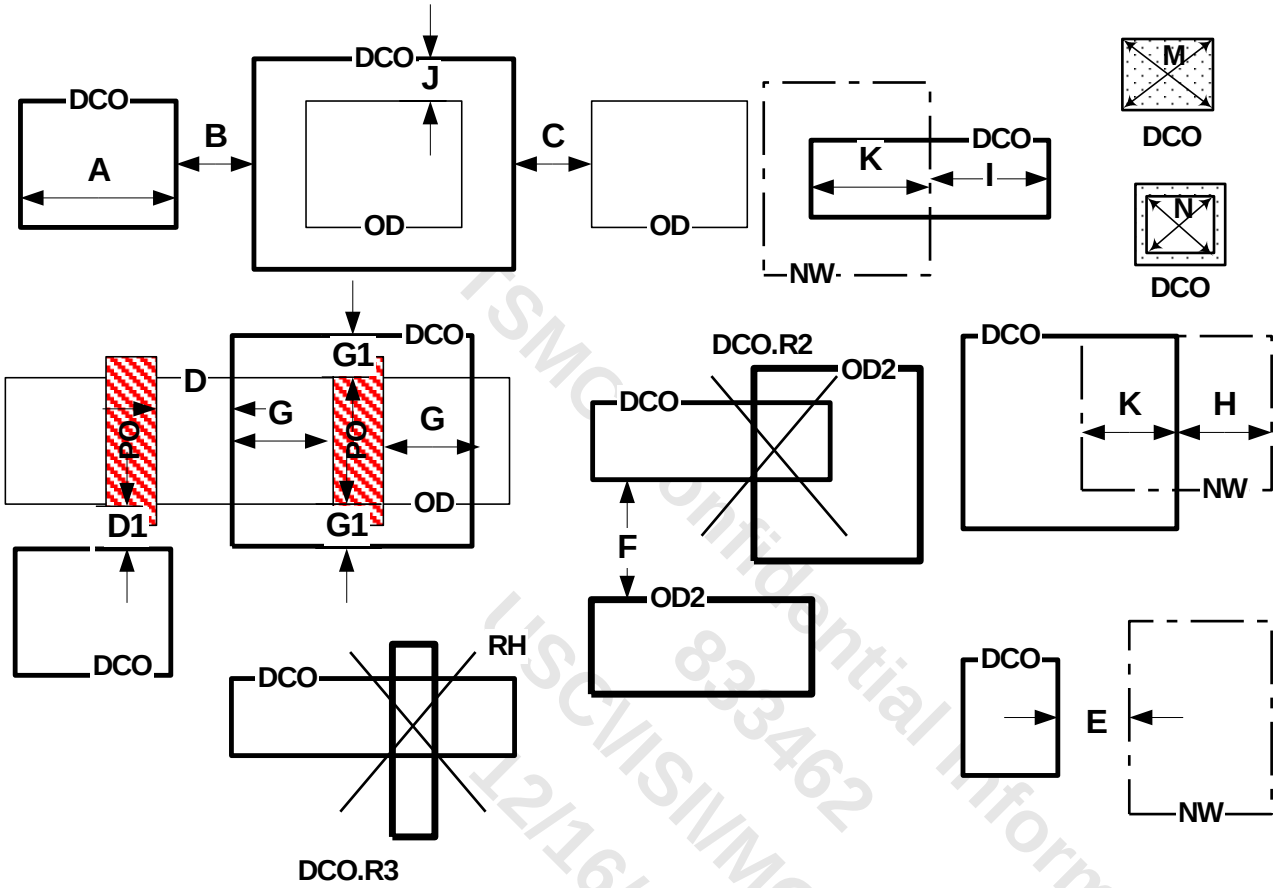
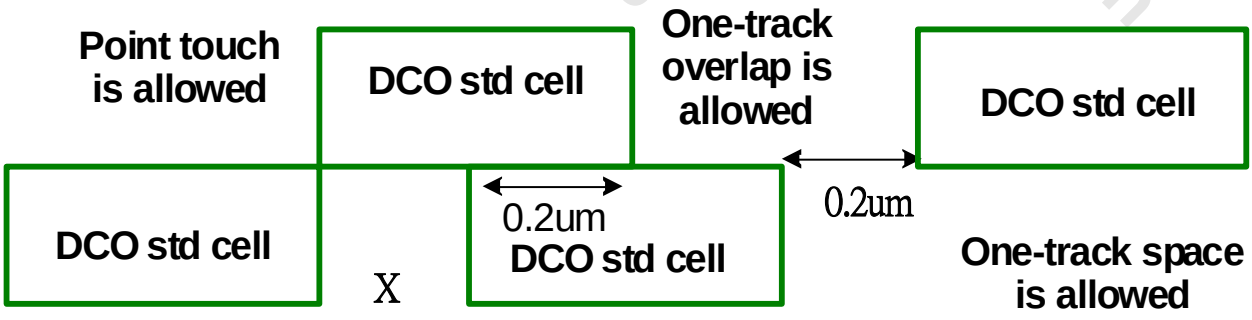
DCO



DCO.R.4/DCO.R.5



Not allowed if space<0.4um

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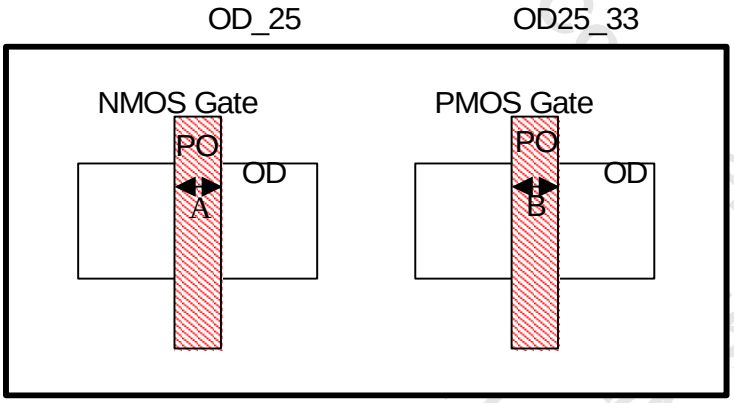
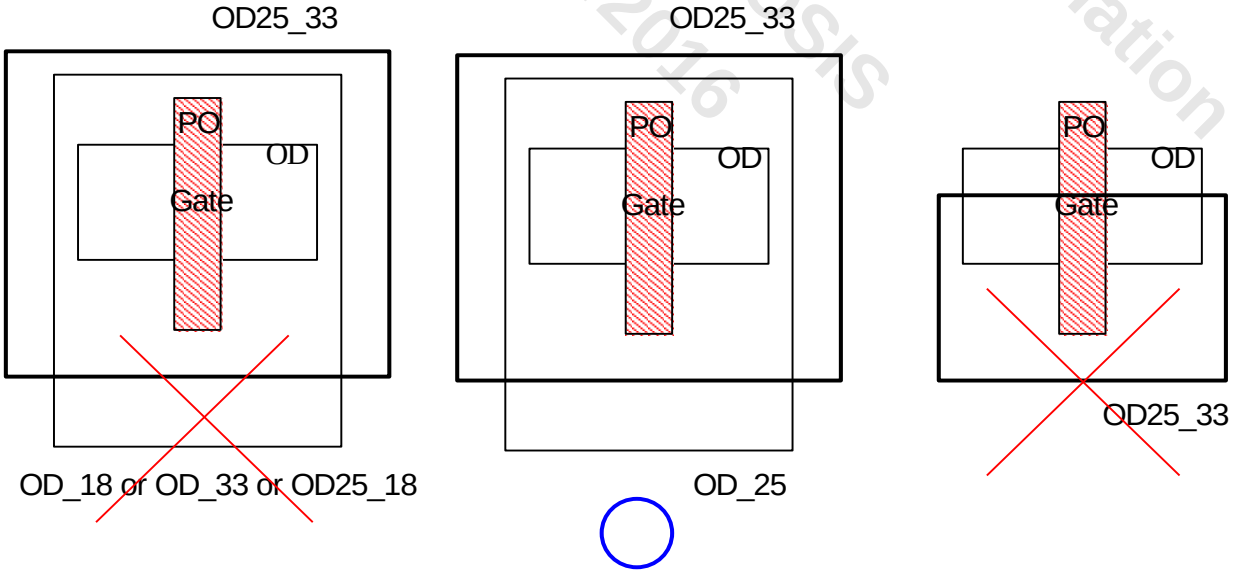
4.5.9 OD25_33 Layout Rules

OD25_33 (CAD layer: 18;3) is used for 2.5V overdrive to 3.3V in N65G/GP/LP/LPG/ULP process and N55 GP/LP process.

Rule No.	Description	Label		Rule
OD25_33.W.1	Channel length of 2.5V NMOS overdrive to 3.3V (NMOS Gate AND OD25_33) except gate without PO CO in RFDMY	A	≥	0.5
OD25_33.W.2	Channel length of 2.5V PMOS overdrive to 3.3V (PMOS Gate AND OD25_33) except gate without PO CO in RFDMY	B	≥	0.4
OD25_33.R.1	(Gate AND OD25_33) can't overlap OD_18 or OD_33 or OD25_18. (Gate AND OD25_33) must be covered by OD_25. OD25_33 can't cut GATE.			



OD25_33.R.1



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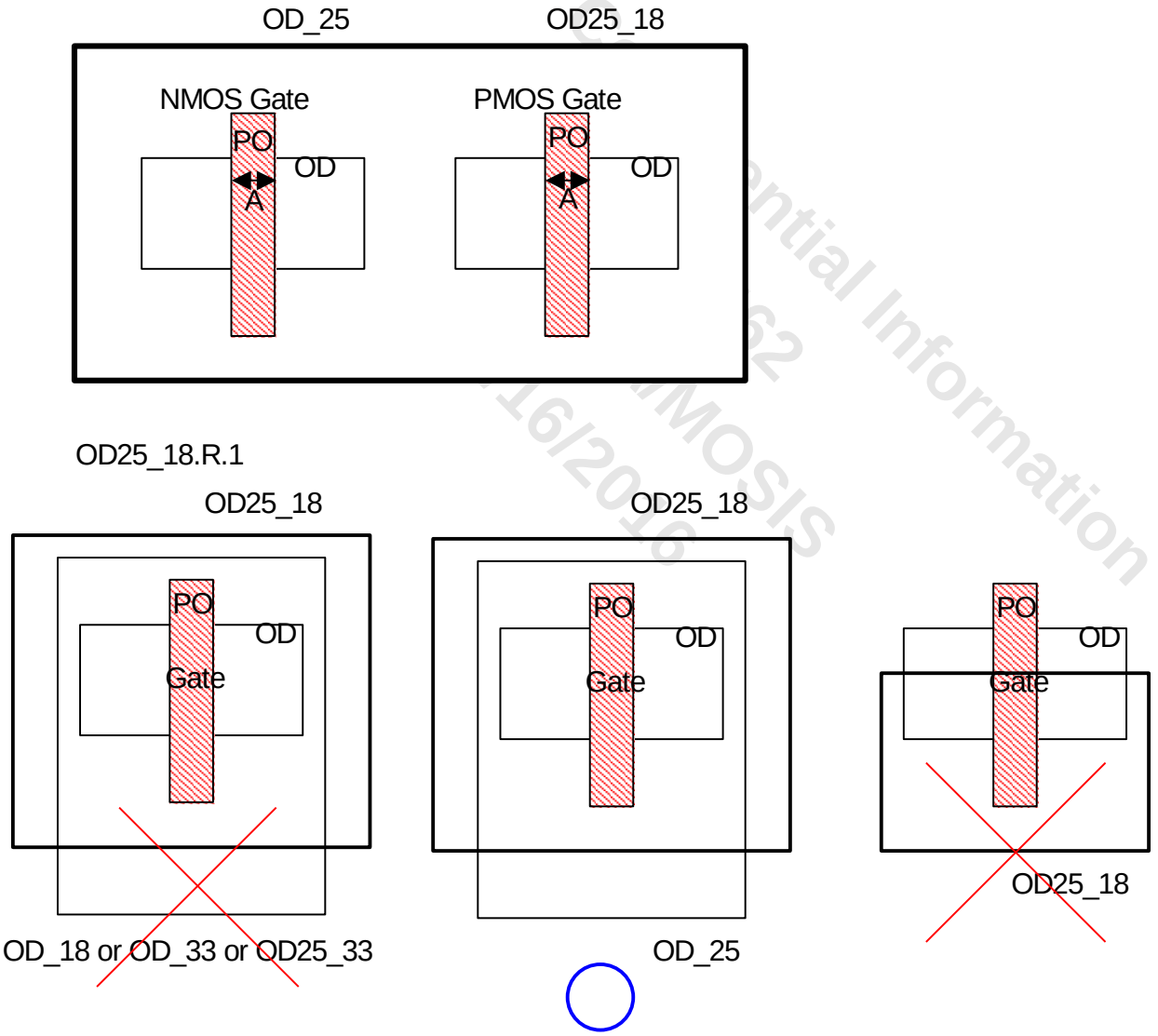
4.5.10 OD25_18 Layout Rules

OD25_18 (CAD layer: 18;4) is only used for 2.5V underdrive to 1.8V in N65 G/GP/LP/LPG/ULP process and N55LP, not in N55 GP process .

2.5V underdrive to 1.8V is not offered in 2.5V native device.

Rule No.	Description	Label		Rule
OD25_18.W.1	Channel length of 2.5V MOS underdrive to 1.8V (Gate AND OD25_18)	A	≥	0.26
OD25_18.R.1	(Gate AND OD25_18) can't overlap OD_18 or OD_33 or OD25_33. (Gate AND OD25_18) must be covered by OD_25. OD25_18 can't cut GATE.			



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4.5.11 Poly (PO) Layout Rules (Mask ID: 130)

Rule No.	Description	Label		Rule
PO.W.1	Width	A	≥	0.06
PO.W.2	Channel length of 2.5V MOS	B	≥	0.28
PO.W.3	Channel length of 3.3V MOS except gate without PO CO in RFDMY (for 2.5V overdrive to 3.3V, please refer to section 4.5.9)	C	≥	0.38
PO.W.4	Channel length of 1.8 V MOS (for 2.5V underdrive to 1.8V, please refer to section 4.5.10)	D	≥	0.20
PO.W.5	Width of 45-degree FIELD PO (except PO fuse element, POFUSE, 156;0). DRC will also flag the width <0.08um in the POFUSE. Please make sure the vertex of 45-degree pattern is on 5nm grid (refer to the guideline, G.6g^{U}, in section 3.7)	E	≥	0.19
PO.S.1	Space	F	≥	0.12
PO.S.1®	Recommended minimum interconnect PO space to reduce the short possibility caused by particle	F	≥	0.15
PO.S.2	GATE space in the same OD	G	≥	0.13
PO.S.2®	Recommended GATE space in the same OD in LP/GP/LPG/ULP process to avoid Isat degradation	G	≥	0.2
PO.S.2.1	Gate space [either one channel length > 0.09 μm]	G1	≥	0.15
PO.S.3	{GATE inside OD2} space in the same OD	H	≥	0.25
PO.S.4	FIELD PO space to OD	I	≥	0.05
PO.S.4.1	Gate space when the area enclosed by L-shape OD and L-shape PO< 0.0121 μm2	I1	≥	0.15
PO.S.4.1®	Recommended gate space when the area enclosed by L-shape OD and L-shape PO< 0.0196 μm^2 for PO/OD rounding effect	I2	≥	0.20
PO.S.5	Space to L-shape OD when PO and OD are in the same MOS [channel width (W) < 0.15 μm]	J	≥	0.10
PO.S.5®	Recommended space to L-shape OD when PO and OD are in the same MOS [channel width (W) ≥ 0.15 μm] for stable Isat (avoid corner rounding effect)	J	≥	0.10
	Recommended max. L-leg length when PO and OD are in the same MOS [channel width (W) ≥ 0.15 μm] , if J<0.1. The recommendation is for stable Isat (avoid corner rounding effect)	J1	≤	0.21
PO.S.6	L-shape PO space to OD when PO and OD are in the same MOS [channel width (W) < 0.15 μm]	K	≥	0.10
PO.S.7	Space if at least one PO width is > 0.13 μm, and the PO parallel run length is > 0.18 μm (individual projection).	L	≥	0.18
PO.S.9	Space of {PO AND RPO}	N	≥	0.25
PO.S.10	Space at PO line-end (W<Q1=0.090) in a dense-line-end configuration: If PO has parallel run length with opposite PO (measured with T1=0.035 extension) along 2 adjacent edges of PO [any one edge <Q1 distance from the corner of the two edges], then one of the space (S1 or S2) needs to be at least this value (except for small jog with edge length < 0.06 um(R))	S1/S2	≥	0.14
PO.S.11®	Recommended space of gate poly [channel length ≤ 0.08um] to neighboring poly for PO gate CDU control.	Z	<	1.0
PO.S.13®	Recommended using the space ranges of gate poly to neighboring poly for sensitive circuit with minimum PO width = 0.06 μm. For space < 0.19 μm, extend the space whenever possible. The recommendation is for PO gate CDU control.	Z2	=	0.19~0.27/ 0.295~0.39/ 0.455~0.94
PO.S.15	Large PO to gate [channel length <=0.08um] space. The large PO is defined as PO area >=630um² and interact with regions of density > 70% flagged by 30um x 30um (stepping 15um) window density check. DPO will be excluded from density check.		≥	1.0
PO.S.16	Space to 45-degree FIELD PO	M	≥	0.19
	For sensitive circuit which needs precisely device parameter control, e.g. constant current source or differential input pair, please follow the subsequent four recommendations, PO.S.14®, PO.EN.1®, PO.EN.2®, and PO.EN.3®. Please refer to the section 5.2.			

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Rule No.	Description	Label		Rule
PO.S.14®	Recommended 1.0V or 1.2V NMOS gate space to {OD2 OR (NW OR NT_N)}, to reduce the impact by well proximity effect.	a	≥	1.0
PO.EN.1®	Recommended 1.0V or 1.2V PMOS gate enclosure by {(NW NOT OD2) NOT NT_N} for 3.3V IO process, to reduce the impact by well proximity effect.	b	≥	1.0
	Recommended 1.0V or 1.2V PMOS gate enclosure by (NW NOT NT_N) for1.8V or 2.5V IO process, to reduce the impact by well proximity effect.	b	≥	1.0
PO.EN.2®	Recommended 1.8V or 2.5V or 3.3V NMOS gate enclosure by {OD2 NOT (NW OR NT_N)}, to reduce the impact by well proximity effect.	c	≥	2.0
PO.EN.3®	Recommended 3.3V PMOS gate enclosure by {(NW AND OD2) NOT NT_N}, to reduce the impact by well proximity effect.	d	≥	1.5
	Recommended 1.8V or 2.5V PMOS gate enclosure by (NW NOT NT_N), to reduce the impact by well proximity effect.	d	≥	1.5
PO.EX.1	Extension on OD (end-cap)	O	≥	0.14
PO.EX.2	OD extension on PO	P	≥	0.115
PO.EX.2®	Recommended OD extension on PO (full and symmetrical contact placement are recommended at both source and drain side) to avoid Isat degradation, especially for channel width>1μm.	P	≥	0.18
PO.EX.3	Extension on OD (end-cap) when the PO space to L-shape OD (in the same MOS) is < 0.1 μm, and the channel width (W) is ≥ 0.15 μm.	Q	≥	0.16
PO.L.1	Maximum PO length between two contacts without gate, as well as the length from any point inside PO gate to nearest CO, when the PO width is < 0.13 μm. (except RTMOM region (RTMOMDMY, CAD layer: 155;21))	R	≤	25
PO.A.1	Area	S	≥	0.042
PO.A.1.1	Area {PO not interacting with Gate}	S3	≥	0.051
PO.A.2	Enclosed area	T	≥	0.094
PO.DN.1	{PO OR DPO} density across full chip		≥	14 %
			≤	40%
PO.DN.2	{OD OR DOD OR PO OR DPO} local density		≥	0.1%
	1. PO.DN.2 rules are checked over any 20 μm x 20 μm area. (stepping in 10 μm increments). 2. For PO.DN.2 rules, the following regions can be excluded: o (CB sizing 2) for high speed/RF products o ODBLK/POBLK/NWDMY/FW/LMARK/LOGO/INDDMY as default o Chip corner stress relief area if seal ring and stress relief pattern added by TSMC. 3. Even in areas covered by {ODBLK OR POBLK}, this pattern density that follows the PO.DN.2 rules is recommended. 4. The rule is applied while width of (checking window NOT item 2) ≥ 5 μm.			
PO.DN.3	PO density within POBLK except {TCDDMY OR RFDMY}		≥	14 %
PO.R.1	GATE must be a rectangle orthogonal to grid. (Both bent GATE and Gate to have jog are not allowed).			
PO.R.2[U]	PO line-end must be rectangular. Other shapes are not allowed.			
PO.R.4	PO intersecting OD must form two or more diffusions except RTMOM region (RTMOMDMY, CAD layer: 155;21).			
PO.R.6	H-gate forbidden with channel length (V) < 0.11 μm, PO center bar length (U) < 0.425 μm, all four H-legs length (X) > 0.065 μm, and all four H-legs width (Y) < 0.255 μm.			
DPO.R.1	DPO is a must. DPO CAD layer (TSMC default, 17;1) must be a different layer from the PO CAD layer.			
PO.R.8	It is prohibited for floating gate if the effective source/drain is not connected together. Floating gate in the DRC: (1) Gate without Poly CO (2) Gate with Poly CO but not connect to MOS OD, STRAP or PAD. (3) It is not a floating gate if the Gate is connected to OD by Butted CO in SRAM bit cell.			

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Rule No.	Description	Label		Rule
	The effective source/drain in DRC: Source/drain is connected to different {MOSOD NOT PO}, STRAP, Gate, or PAD. This rule is only checked in whole chip, not in IP level.			
PO.FU.R.8	FUSELINK layer must exist and be inside POFUSE if POFUSE exists (only for N65GP/ N55GP/ N55LP)			
PO.L.1g^{U}	Recommend to limit the max interconnect PO length (R) as short as possible to avoid high Rs variation by salicidation.			

Table Notes:

Good poly uniformity is the key to meet the PO CD as well as circuit performance requirement. You must fill the DPO globally and uniformly even if the original drawn poly already satisfies the required poly density rule (PO.DN.1). The designer may wish to add dummy poly to improve the stability of the poly line dimension on silicon. It is recommended to manually add DPO uniformly inside regions covered by the dummy fill blocking layer POBLK, to gain better process window and electrical performance.

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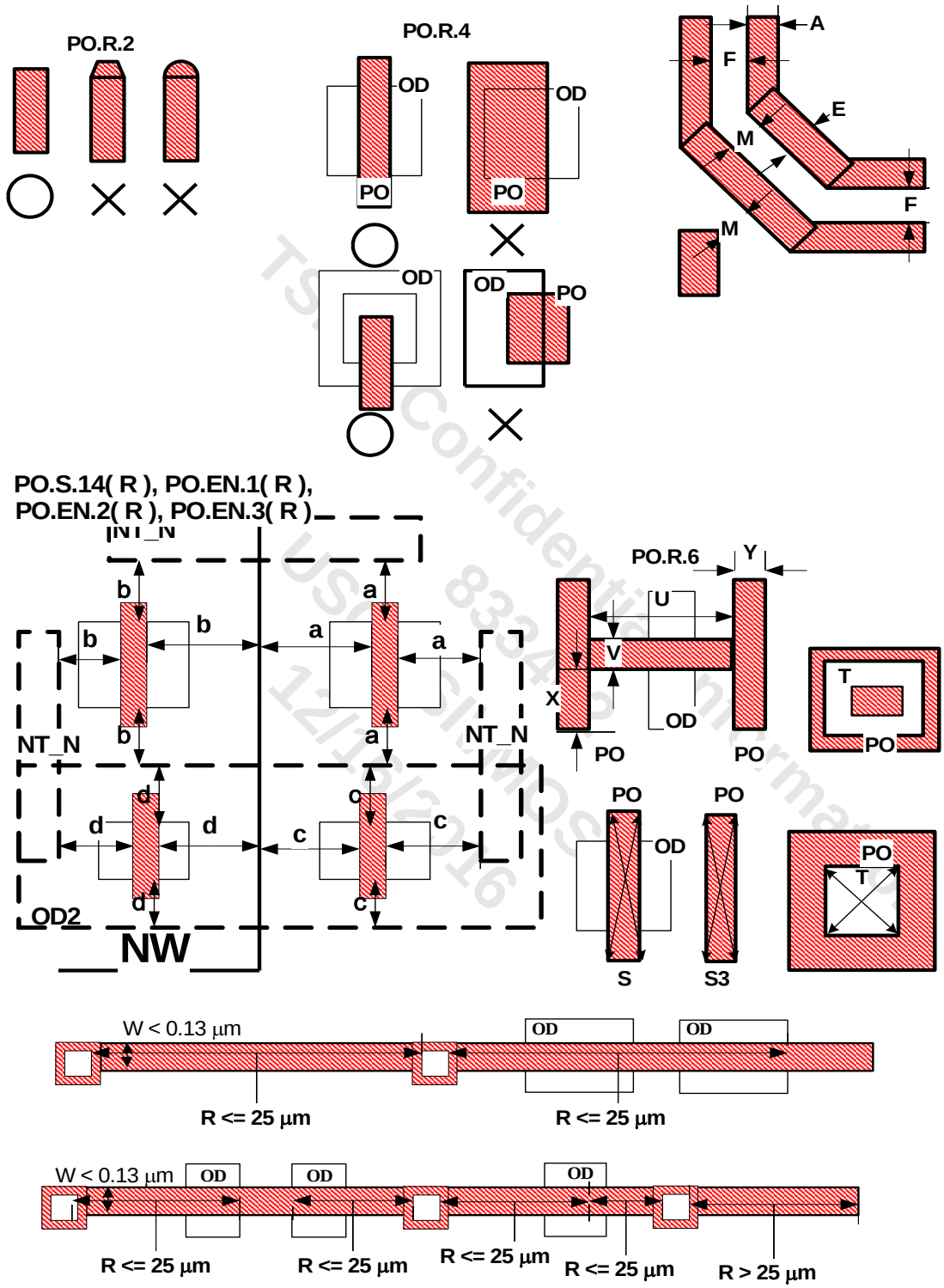
PO



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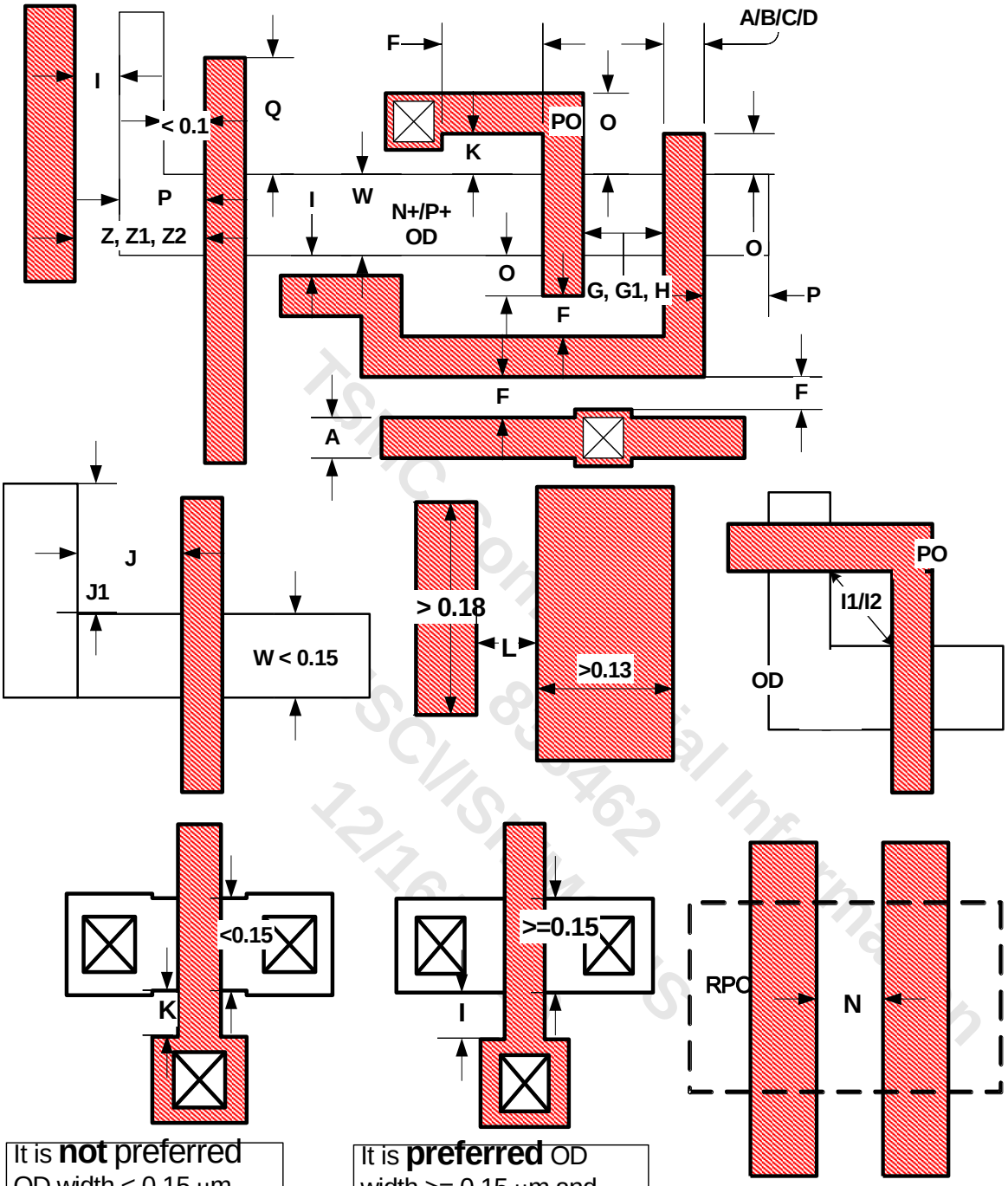

It is **not** preferred OD width < 0.15 μm and with dogbone.

It is **preferred** OD width >= 0.15 μm and without dogbone.

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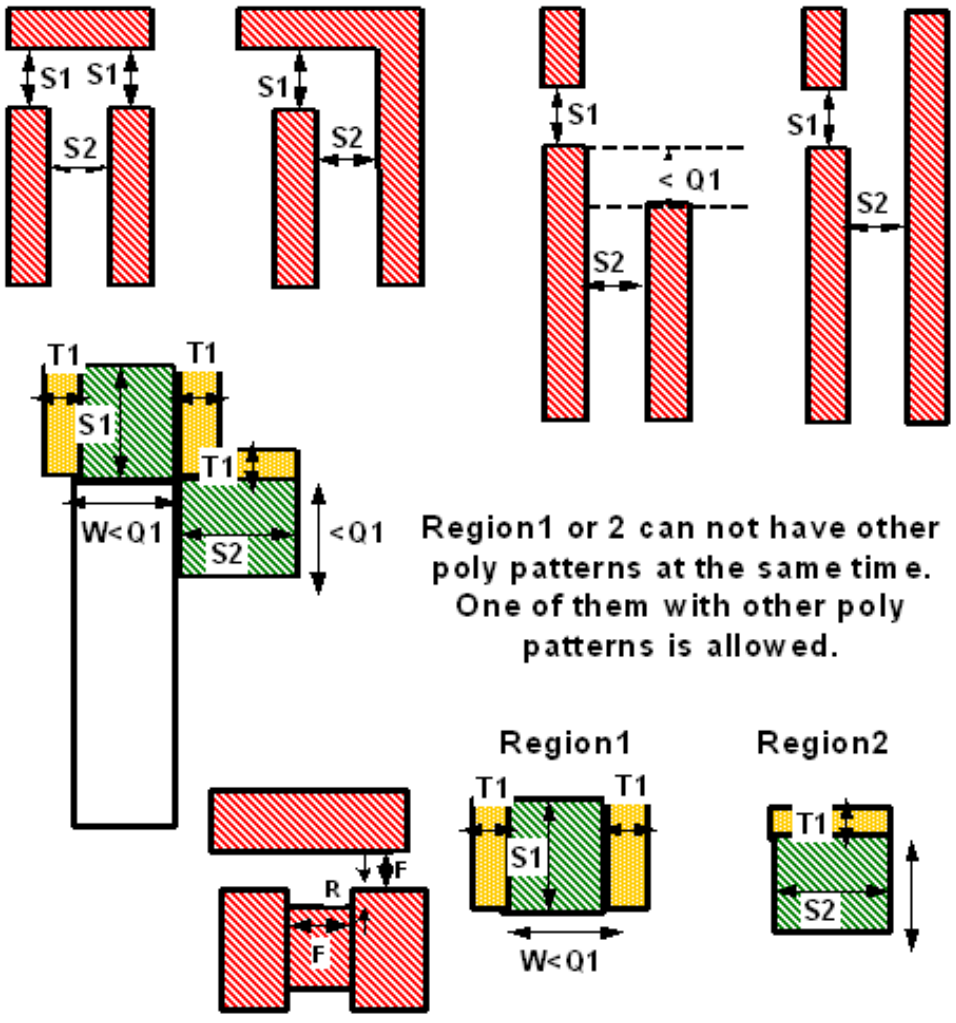
PO.S.10



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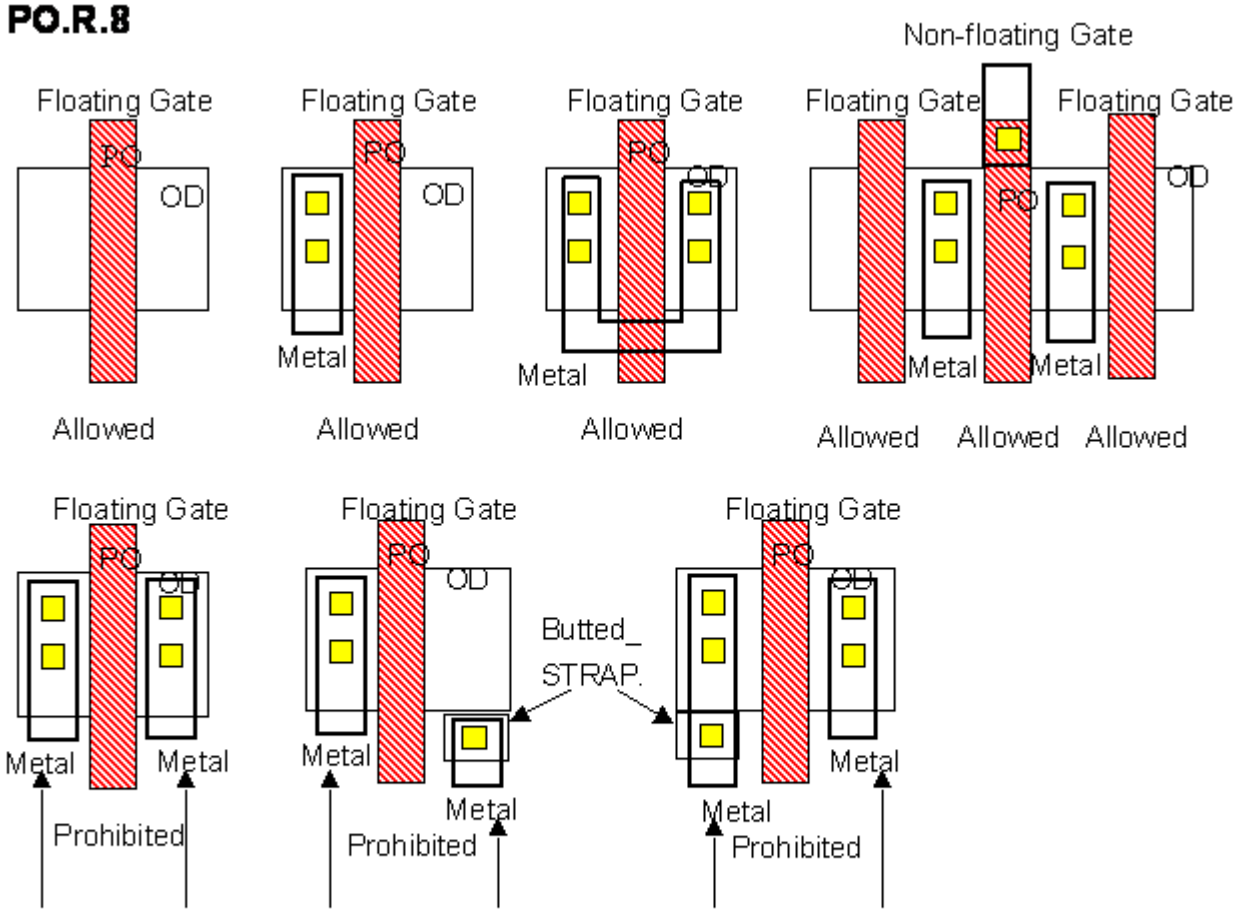
PO.R.8



Source/drain is connected to different {MOS OD NOT PO}, STRAP, Gate, or PAD.

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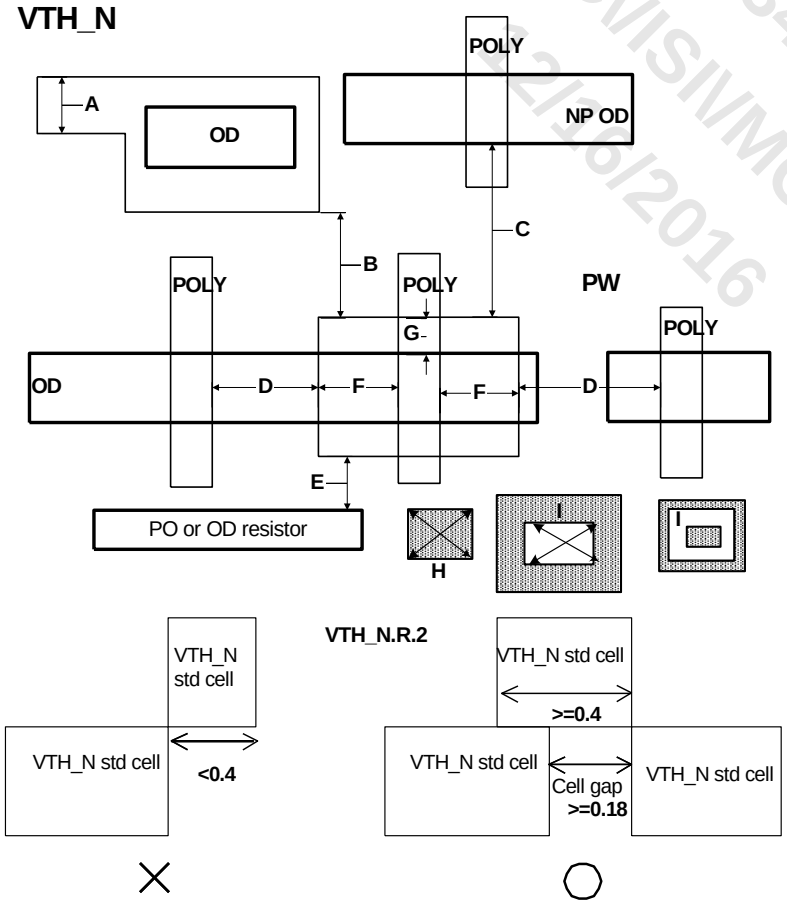
4.5.12 High Vt NMOS (VTH_N) Layout Rules (Mask ID: 128)

VTH_N, 1.0V or 1.2V high Vt NMOS Implant Definition

VTH_N is only used for core devices (1.0V, 1.2V). It is not allowed in I/O devices (1.8V, 2.5V, and 3.3V).

Rule No.	Description	Label		Rule
VTH_N.W.1	Width	A	≥	0.18
VTH_N.S.1	Space	B	≥	0.18
VTH_N.S.2	Space to gate in PO endcap direction	C	≥	0.16
VTH_N.S.2.1	Space to gate in S/D direction	D	≥	0.185
VTH_N.S.3	Space to unsilicided OD	E	≥	0.22
VTH_N.EN.1	Enclosure of gate in S/D direction	F	≥	0.185
VTH_N.EN.2	Enclosure of gate in PO endcap direction	G	≥	0.16
VTH_N.A.1	Area	H	≥	0.27
VTH_N.A.2	Enclosed area	I	≥	0.27
VTH_N.R.1	Overlap of P+ACTIVE, VTL_N, NT_N, or OD2 is not allowed.			
VTH_N.R.2	Point touch of corners are allowed. [width ≥ 0.4 μm]			

VTH_N



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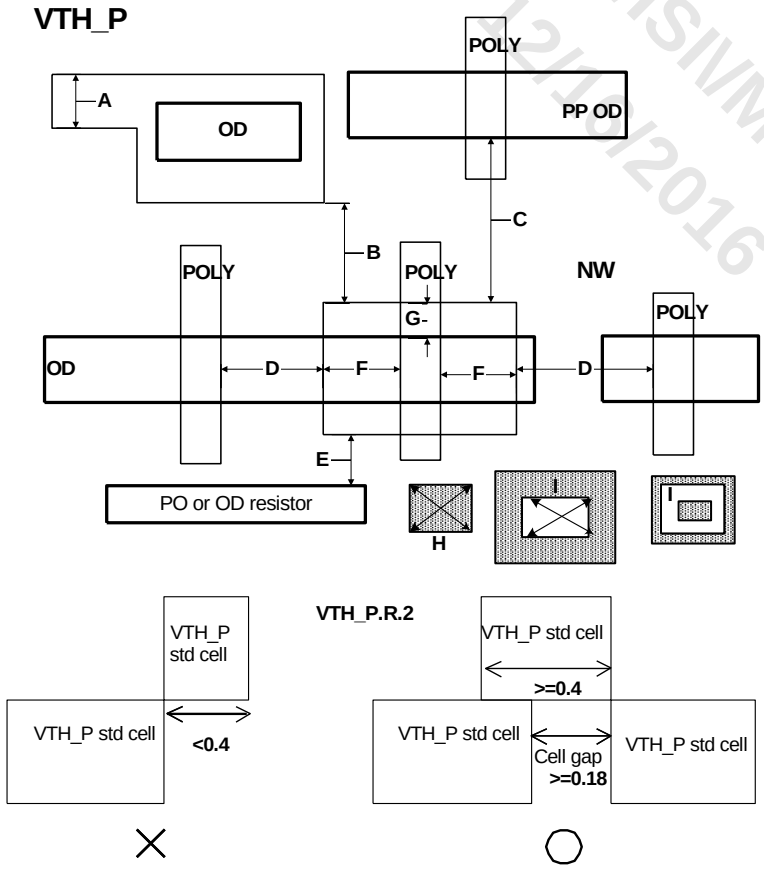
4.5.13 High Vt PMOS (VTH_P) Layout Rules (Mask ID: 127)

VTH_P, 1.0V or 1.2V High Vt PMOS Implant Definition

VTH_P is only used for core devices (1.0V, 1.2V). It is not allowed in I/O devices (1.8V, 2.5V, and 3.3V).

Rule No.	Description	Label		Rule
VTH_P.W.1	Width	A	≥	0.18
VTH_P.S.1	Space	B	≥	0.18
VTH_P.S.2	Space to gate in PO endcap direction	C	≥	0.16
VTH_P.S.2.1	Space to gate in S/D direction	D	≥	0.185
VTH_P.S.3	Space to unsilicided OD	E	≥	0.22
VTH_P.EN.1	Enclosure of gate in S/D direction	F	≥	0.185
VTH_P.EN.2	Enclosure of gate in PO endcap direction	G	≥	0.16
VTH_P.A.1	Area	H	≥	0.27
VTH_P.A.2	Enclosed area	I	≥	0.27
VTH_P.R.1	Overlap of N+ACTIVE (including varactor gate), VTL_P, NT_N, or OD2 is not allowed.			
VTH_P.R.2	Point touch of corners are allowed. [width ≥ 0.4 μm]			

VTH_P



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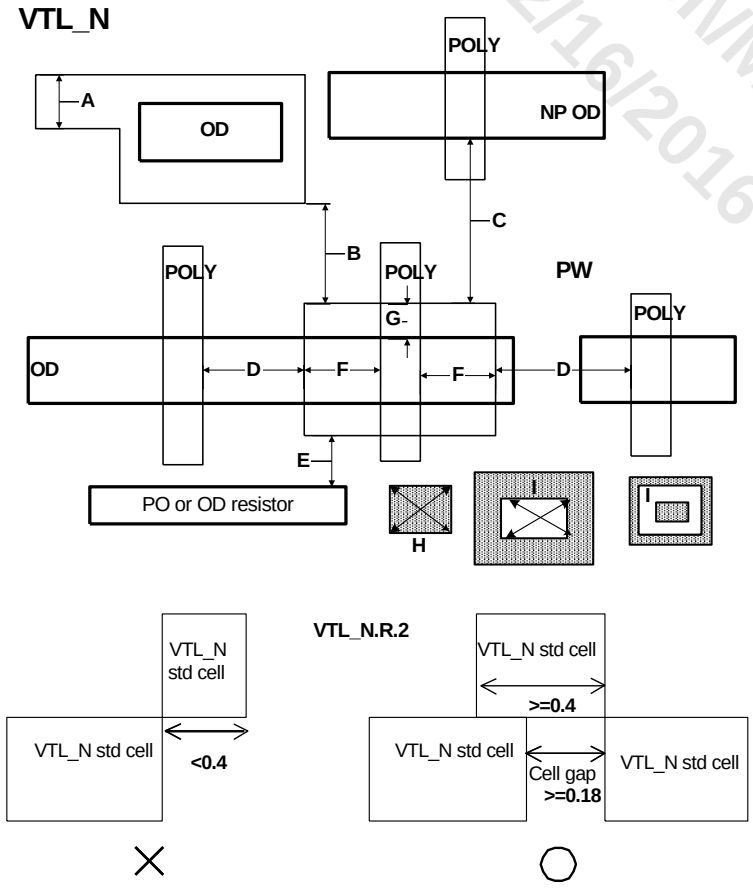
4.5.14 Low Vt NMOS (VTL_N) Layout Rules (Mask ID: 118)

VTL_N, 1.0V(GP) or 1.2V Low Vt NMOS Implant Definition

VTL_N is only used for core devices (1.0V(GP), 1.2V). It is not allowed in core devices (1.0V(G)) or I/O devices (1.8V, 2.5V, and 3.3V).

Rule No.	Description	Label		Rule
VTL_N.W.1	Width	A	≥	0.18
VTL_N.S.1	Space	B	≥	0.18
VTL_N.S.2	Space to gate in PO endcap direction	C	≥	0.16
VTL_N.S.2.1	Space to gate in S/D direction	D	≥	0.185
VTL_N.S.3	Space to unsilicided OD	E	≥	0.22
VTL_N.EN.1	Enclosure of gate in S/D direction	F	≥	0.185
VTL_N.EN.2	Enclosure of gate in PO endcap direction	G	≥	0.16
VTL_N.A.1	Area	H	≥	0.27
VTL_N.A.2	Enclosed area	I	≥	0.27
VTL_N.R.1	Overlap of P+ACTIVE, VTH_N, NT_N, or OD2 is not allowed.			
VTL_N.R.2	Point touch of corners are allowed. [width ≥ 0.4 μm]			

VTL_N



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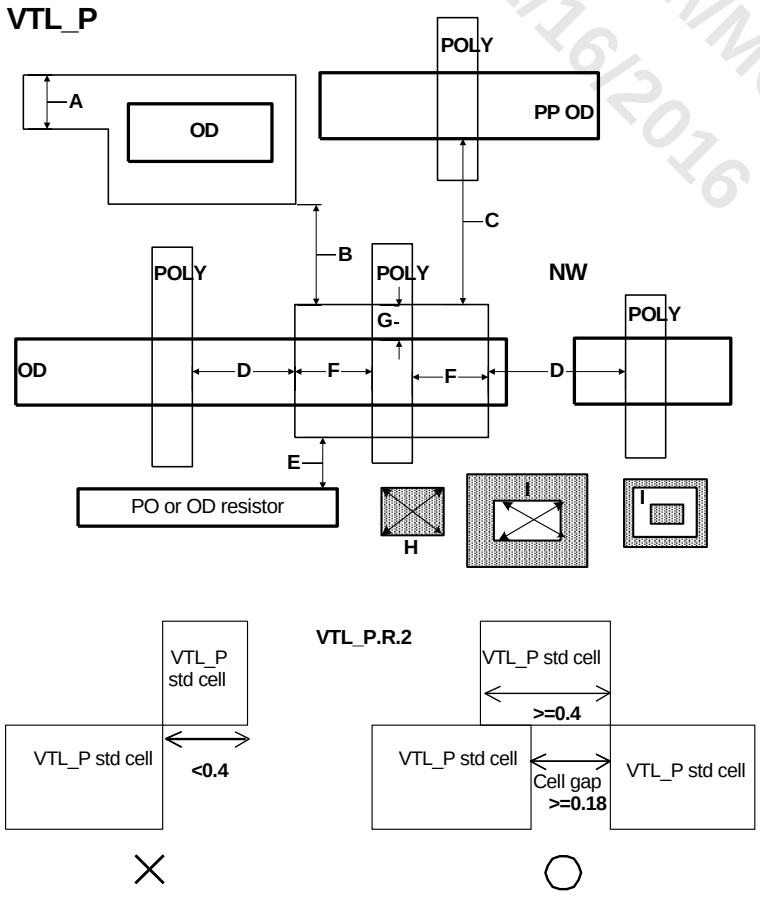
4.5.15 Low Vt PMOS (VTL_P) Layout Rules (Mask ID: 117)

VTL_P, 1.0V(GP) or 1.2V Low Vt PMOS Implant Definition

VTL_P is only used for core devices (1.0V(GP), 1.2V). It is not allowed in core devices (1.0V(G)) or I/O devices (1.8V, 2.5V, and 3.3V)

Rule No.	Description	Label		Rule
VTL_P.W.1	Width	A	≥	0.18
VTL_P.S.1	Space	B	≥	0.18
VTL_P.S.2	Space to gate in PO endcap direction	C	≥	0.16
VTL_P.S.2.1	Space to gate in S/D direction	D	≥	0.185
VTL_P.S.3	Space to unsilicided OD	E	≥	0.22
VTL_P.EN.1	Enclosure of gate in S/D direction	F	≥	0.185
VTL_P.EN.2	Enclosure of gate in PO endcap direction	G	≥	0.16
VTL_P.A.1	Area	H	≥	0.27
VTL_P.A.2	Enclosed area	I	≥	0.27
VTL_P.R.1	Overlap of N+ACTIVE (including varactor gate), VTH_P, NT_N, or OD2 is not allowed.			
VTL_P.R.2	Point touch of corners are allowed. [width ≥ 0.4 µm]			

VTL_P



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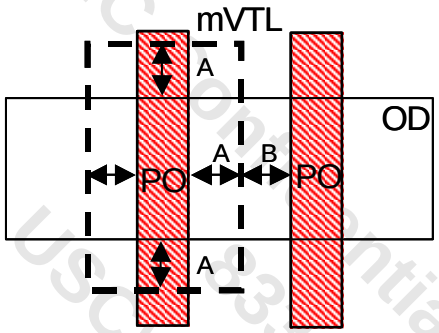
4.5.16 m-Low Vt (mVTL) Layout Rules

mVTL is only used for core LP/ULP devices (LP, ULP). It is not allowed in core G/GP/LPG devices or I/O devices (1.8V, 2.5V, and 3.3V).

mVTL: You must provide this layer (CAD layer: 17;51) to generate poly logical operation in LP/ULP process with standard Vt implant so that there is no additional mask requirement.

Rule No.	Description	Label		Rule
mVTL.EN.1	Enclosure of gate	A	≥	0.05
mVTL.S.1	Space to gate	B	≥	0.05
mVTL.R.1	Overlap of VTH_N, VTH_P, VTL_N, VTL_P, NT_N, or OD2 is not allowed.			



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4.5.17 N65 HVD_N Layout Rules

HVD_N (CAD layer 91;3) is only used for 5V HV NMOS to define drain side where high voltage will be sustained. The following rules are for N65 LP 5V HV NMOS. For N55 5V HVMOS, please refer to T-N55-CL-DR-006.

Rule No.	Description	Label		Rule
HVD_N.L.1	Channel length of {gate INTERACT HVD_N}	M	≥	0.85
HVD_N.W.2	Channel width of {gate INTERACT HVD_N}	N	≥	0.6
HVD_N.W.1	Width	A	≥	0.47
HVD_N.S.1	Space	B	≥	0.47
HVD_N.S.2	Space of two HVD_N with different potentials (*)	C	≥	1.37
HVD_N.S.3	Space to NW	D	≥	1.6
HVD_N.S.4	Space to PW STRAP (overlap is not allowed)	E	≥	0.3
HVD_N.S.5	Space to N+ ACTIVE	F	≥	0.6
HVD_N.S.6	Space to DNW (overlap is not allowed)	G	≥	3.0
HVD_N.EX.1	Extension on N+ ACTIVE (Drian side must be fully inside HVD_N)	I	≥	0.24
HVD_N.O.1	Overlap of {I/O NMOS GATE}	J	=	0.30
HVD_N.A.1	Area	K	≥	0.64
HVD_N.A.2	Enclosed area	L	≥	0.64
HVD_N.R.1	Overlap of NW is not allowed.			
HVD_N.R.2	HVD_N edge landing on OD without landing on GATE is not allowed.			
HVD_N.R.3	HVD_N must be fully inside OD_25.			
HVD_N.R.4	{(OD NOT PO) inside one HVD_N} must be same potential (**)			
HVD_N.R.5®^{U}	For better Idsat uniformity with single finger gate, HVD_N is recommended to be located at the same side of the gate.			
HVD_N.R.6	{(HVD_N interact OD) AND PO} must be a rectangle. A concave {(HVD_N interact OD) AND PO} is not allowed.			

(*) DRC implementation is on different nets
(**) DRC implementation is on same nets

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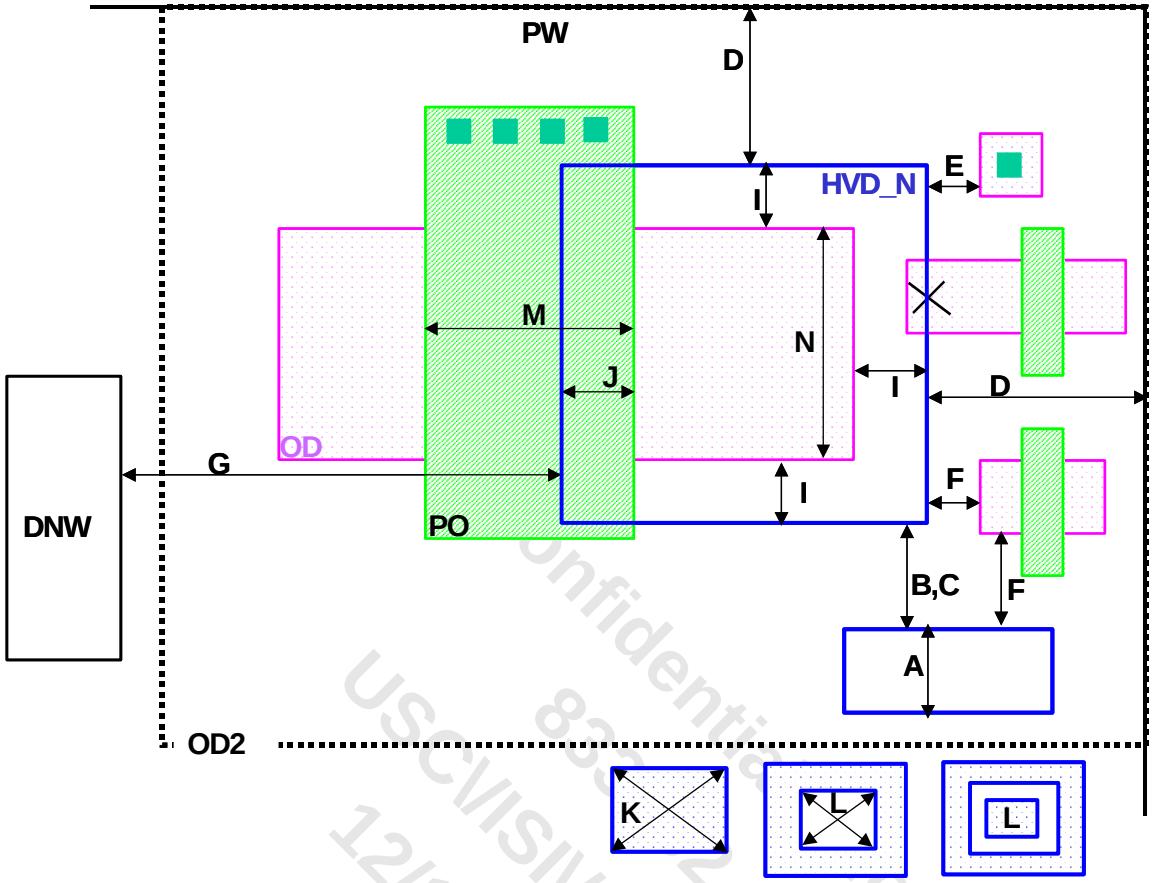
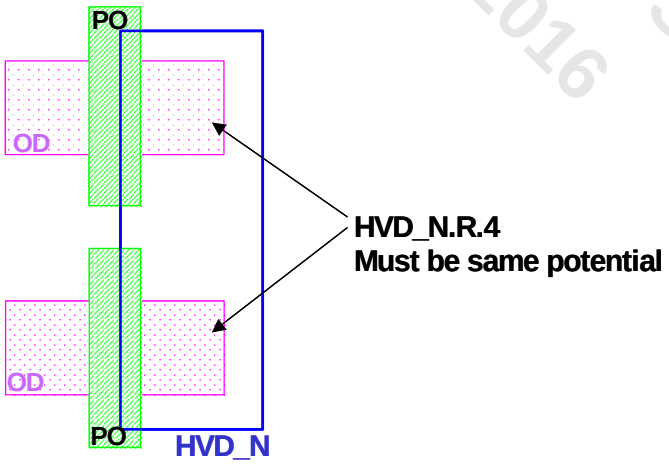
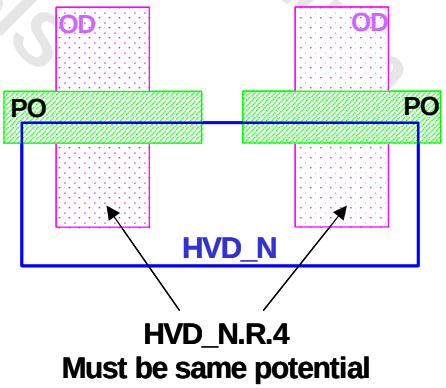
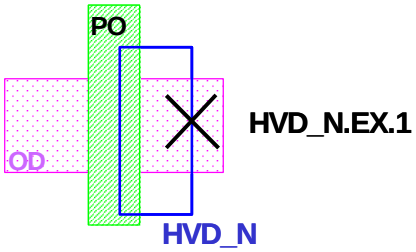
HVD_N









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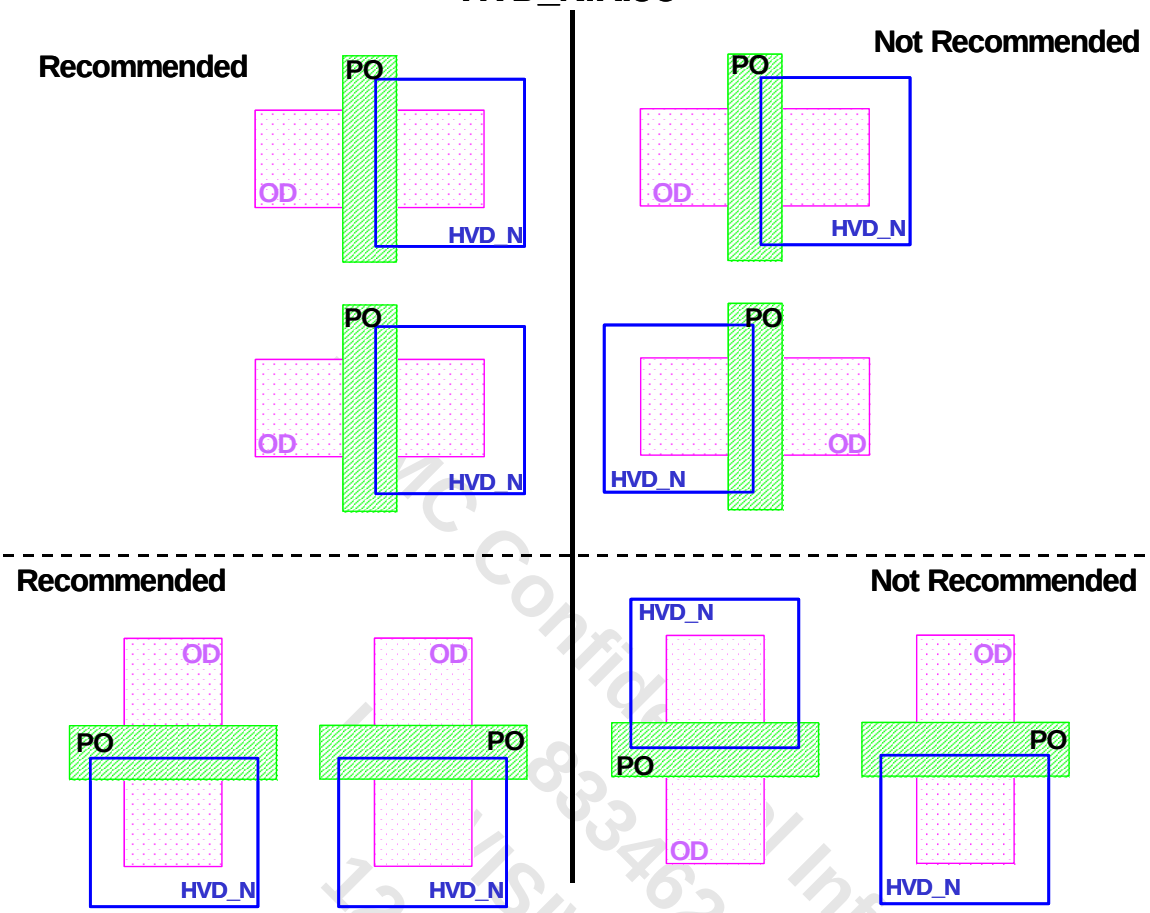
HVD_N.R.5®



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4.5.18 N65 HVD_P Layout Rules

HVD_P (CAD layer 91;2) is only used for 5V HV PMOS to define drain side where high voltage will be sustained. The following rules are for N65 LP 5V HV PMOS. For N55 5V HVMOS, please refer to T-N55-CL-DR-006.

Rule No.	Description	Label		Rule
HVD_P.L.1	Channel length of {gate INTERACT HVD_P}	M	≥	0.6
HVD_P.W.2	Channel width of {gate INTERACT HVD_P}	N	≥	0.6
HVD_P.W.1	Width	A	≥	0.47
HVD_P.S.1	Space	B	≥	0.47
HVD_P.S.2	Space of two HVD_P with different potentials(*)	C	≥	1.2
HVD_P.S.4	Space to NW STRAP (overlap is not allowed)	E	≥	0.24
HVD_P.S.5	Space to P+ ACTIVE	F	≥	0.48
HVD_P.EX.1	Extension on P+ ACTIVE (Drian side must be fully inside HVD_P)	I	≥	0.24
HVD_P.EN.1	Enclosure by NW	D	≥	1.6
HVD_P.O.1	Overlap of {I/O PMOS GATE}	J	=	0.25
HVD_P.A.1	Area	K	≥	0.64
HVD_P.A.2	Enclosed area	L	≥	0.64
HVD_P.R.1	HVD_P must be inside {NW NOT INTERACT DNW}			
HVD_P.R.2	HVD_P edge landing on OD without landing on GATE is not allowed.			
HVD_P.R.3	HVD_P must be fully inside OD_25.			
HVD_P.R.4	{(OD NOT PO) inside same HVD_P} must be same potential (**)			
HVD_P.R.5®^{U}	For better Idsat uniformity with single gate, HVD_P is recommended to be located at the same side of the gate.			
HVD_P.R.6	{(HVD_P interact OD) AND PO} must be a rectangle. A concave {(HVD_P interact OD) AND PO} is not allowed.			

(*) DRC implementation is on different nets
(**) DRC implementation is on same nets

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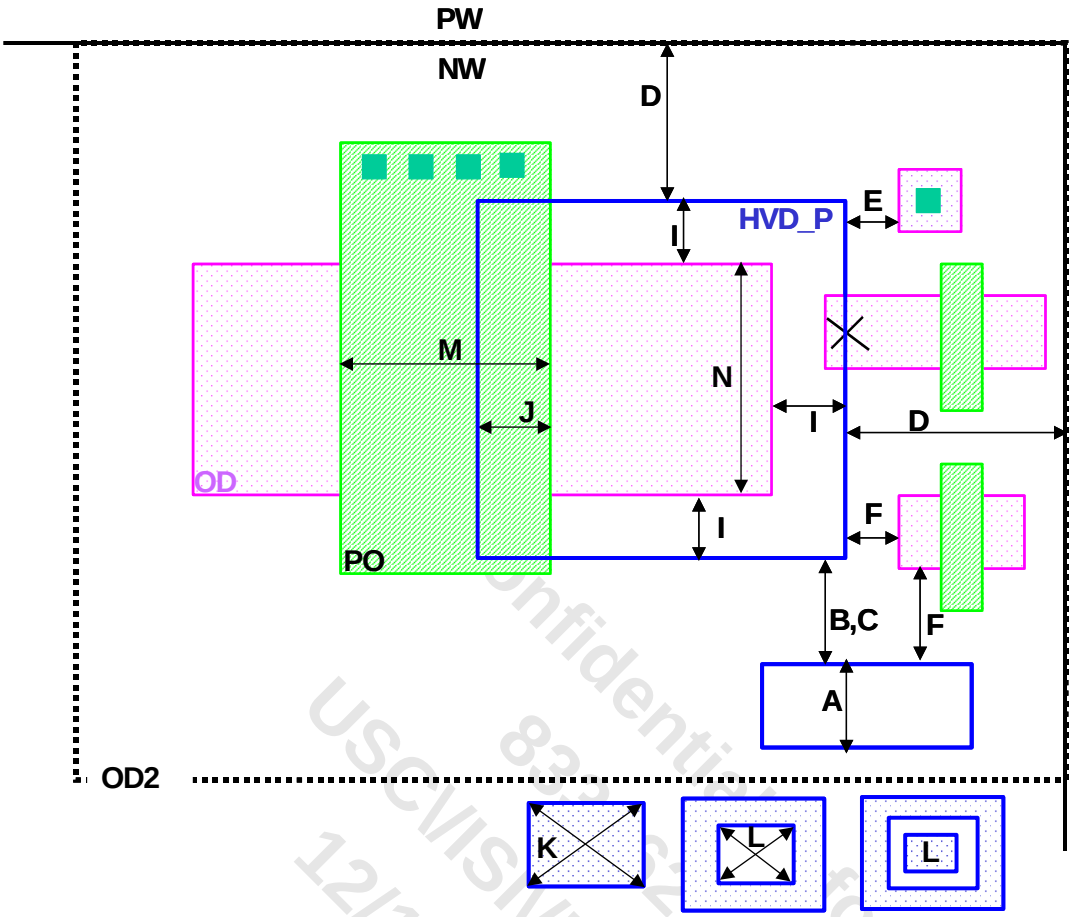
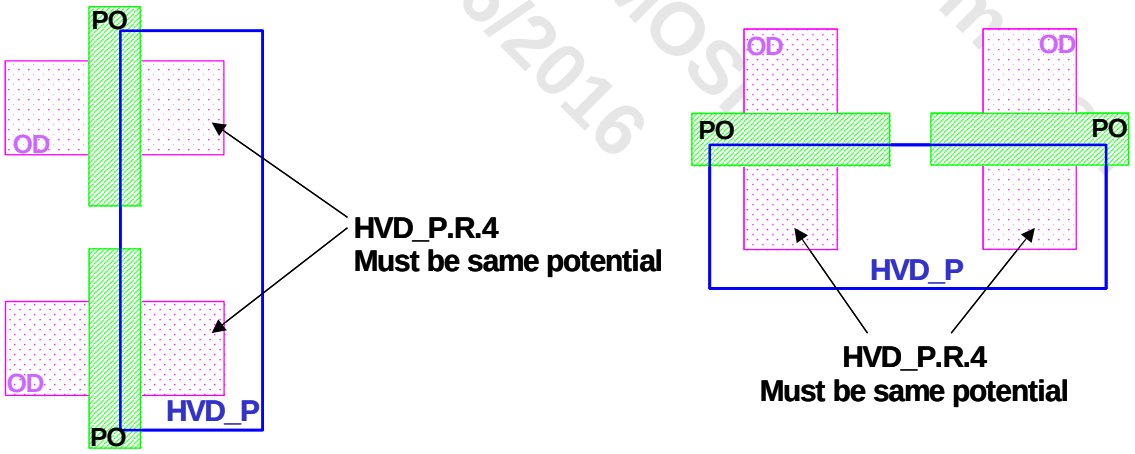
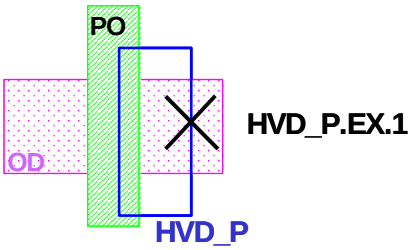
HVD_P







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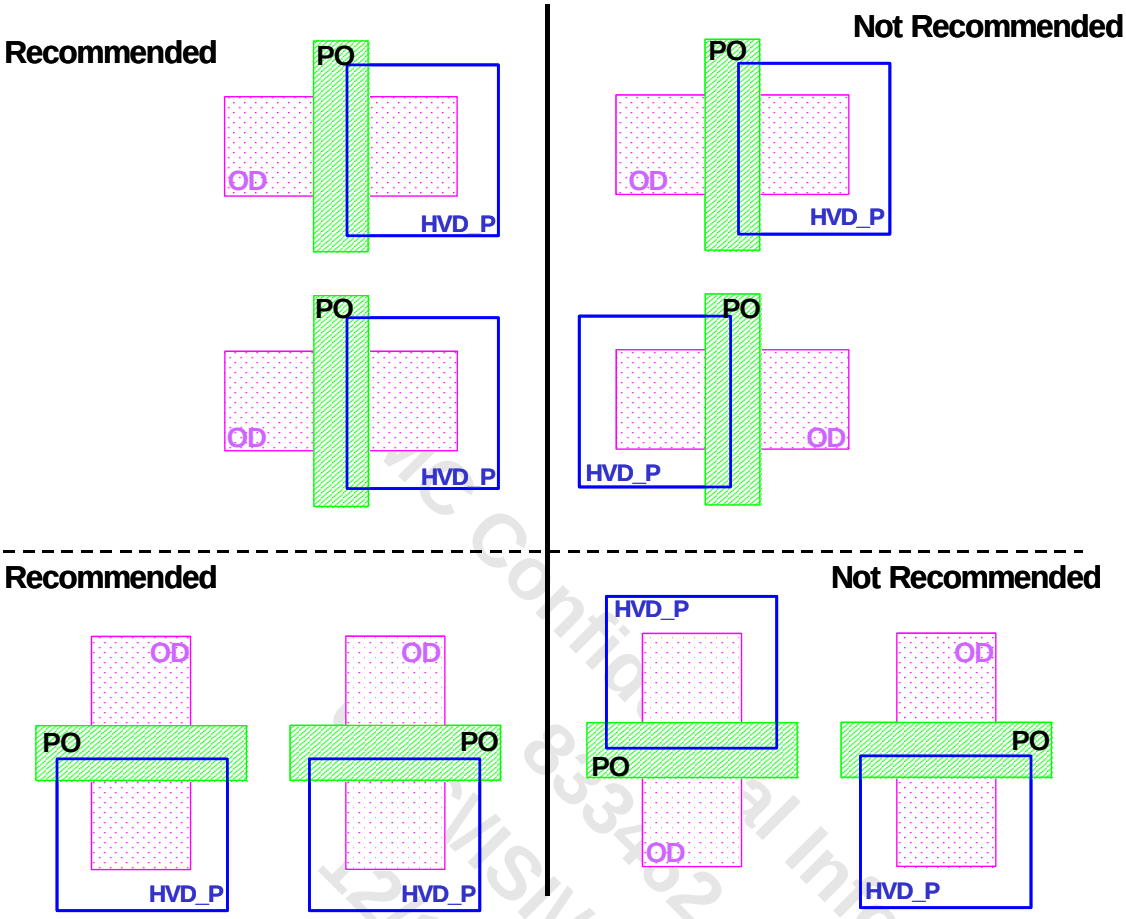
HVD_P.R.5 ®



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4.5.19 N65 5V HVMOS Layout Rules and Guidelines

The following rules and guidelines are particularly for N65 LP 5V HVMOS with multi-finger gate. The following rules are for N65 LP 5V HVMOS guard ring. For N55 5V HVMOS, please refer to T-N55-CL-DR-006.

4.5.19.1 Guard Ring Rules and Guidelines

Rule No.	Description	Label		Rule
GR.R.1	It is not allowed to place HV NMOS and HV PMOS inside the same guard ring (Either P+ or N+ OD guard ring)			
GR.R.2[U]	HV NMOS must be surrounded by the P+ guard ring as PW strap, the P+ guard ring must to be connected to Vss (*).			
GR.R.3[U]	HV PMOS must be surrounded by the N+ guard ring as NW strap, the N+ guard ring must to be connected to Vdd (*).			
GR.R.4®[U]	If there is a set of cluster 5V HVMOS, it is highly recommended that please use the guard ring at the outer edge of the cluster and to partition each of the HVMOS. ● Every HV NMOS cluster has to be surrended by P+ guard ring (PW strap). (please refer to Fig.4.5.19.1.1(a)) ● Every HV PMOS cluster has to be surrended by N+ guard ring (NW strap). (please refer to Fig.4.5.19.1.1(b))			
GR.R.5[U]	Please put Contact (CO) as many as possible in the P+ or N+ guard ring (PW strap or NW strap).			
GR.R.6[U]	For the design of cluster HV PMOS in the same N+ guard-ring(NW strap), only one row or two rows of multi-OD (in the S/D direction) are allowed (Fig.4.5.19.1.2).			
GR.R.7	For one row and two rows of multi-OD in the same guard-ring The outer edge of OD in the poly endcap direction of each HV PMOS space to the N+ guard-ring(NW strap) (Fig.4.5.19.1.3)	A	≤	2
GR.R.8	The OD space in the poly endcap direction between two adjacent rows of each HV PMOS in the same N+ guard-ring(NW strap) (Fig.4.5.19.1.3)	B	≤	4
GR.R.9[U]	The space of inner OD edge of the nearest N+ guard-ring(NW strap) in the poly endcap direction of HV PMOS (Fig.4.5.19.1.3)	C	≤	28
GR.R.10	For one row and two rows multi-OD in the same guard-ring The outer edge of OD in the S/D direction for HV PMOS space to the N+ guard-ring(NW strap) (Fig.4.5.19.1.4)	D	≤	2
GR.R.11	The OD space in the S/D direction between two adjacent HV PMOS in the same N+ guard-ring(NW strap) (Fig.4.5.19.1.4)	E	≤	2
GR.R.12[U]	The space of inner OD edge of the nearest N+ guard-ring(NW strap) in the S/D direction of HV PMOS (Fig.4.5.19.1.4)	F	≤	65
GR.R.13	The OD width of two-rows multi-OD HV PMOS within the same N+ guard-ring(NW strap)	G, G1	≤	10
GR.R.14	HV N/PMOS enclosed by P+ guard-ring(PW strap) or N+ guard-ring(NW strap) with RPO is not allowed.			
GR.R.15®[U]	Recommend to reduce the breach region of M1 on P+ guard-ring(PW strap) or N+ guard-ring(NW strap) if using M1 to connect HV N/PMOS to outside circuit.			

Table Notes:

(*)Regarding the other Guard-ring rules of HVMOS, please follow Section 10.1.2 Layout Rules and Guidelines for Latch-up prevention".

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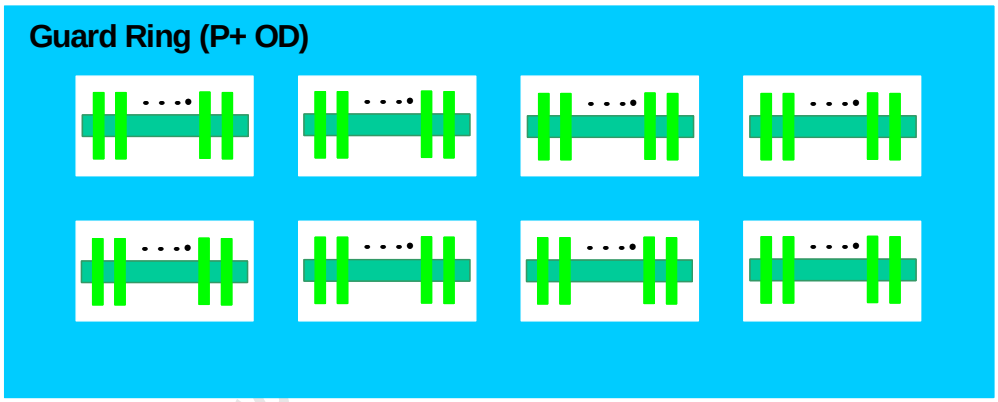

Fig.4.5.19.1.1(a)

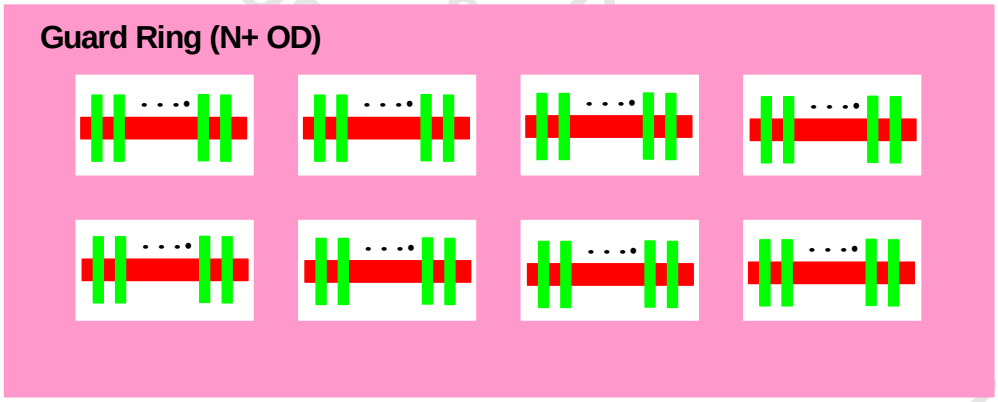

Fig.4.5.19.1.1(b)

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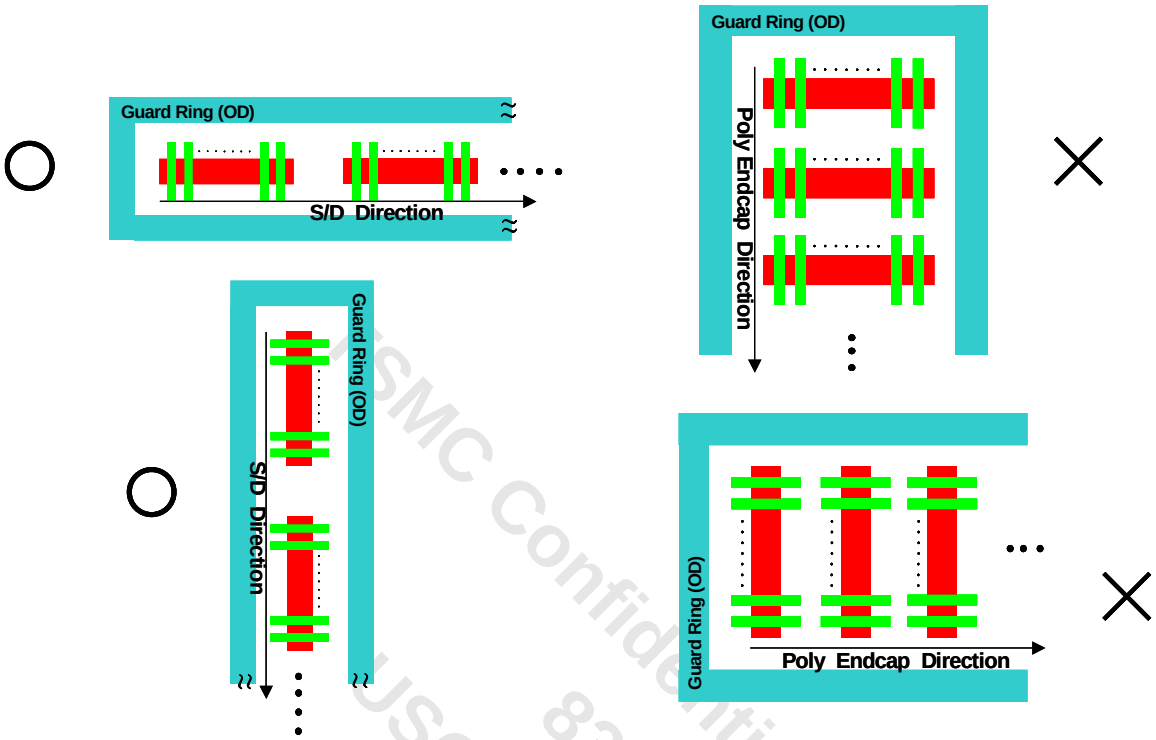
One-Row HV PMOS



Two-Row HV PMOS

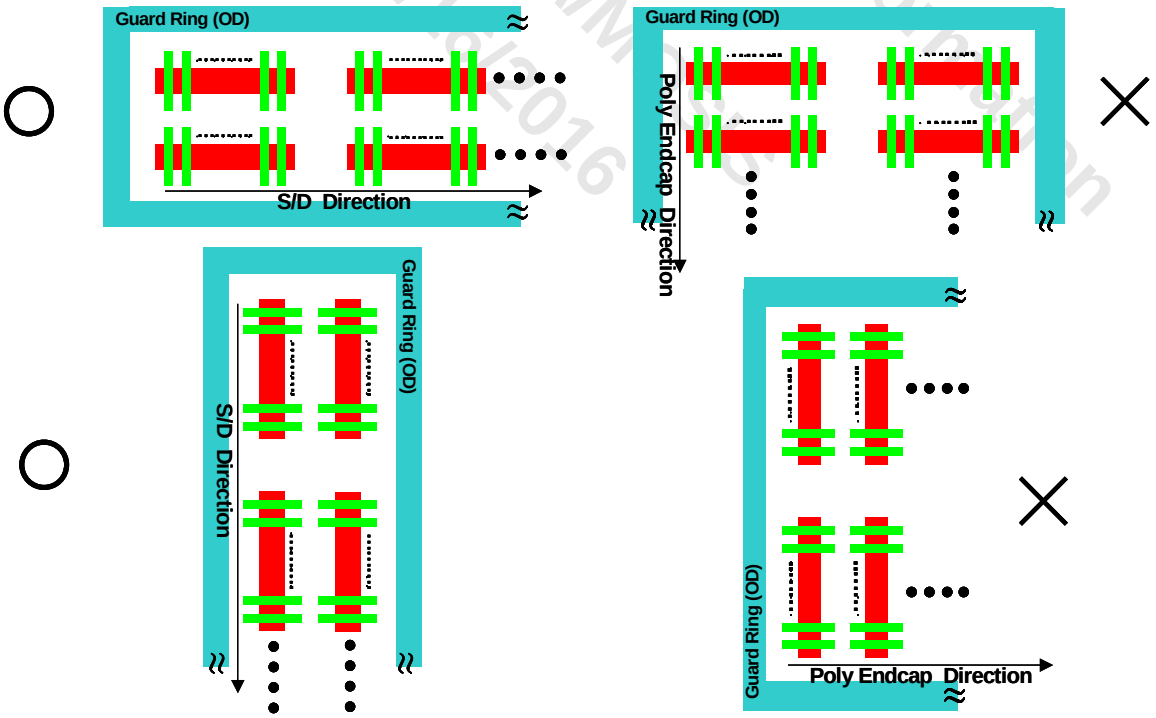


Figure 4.5.19.1.2

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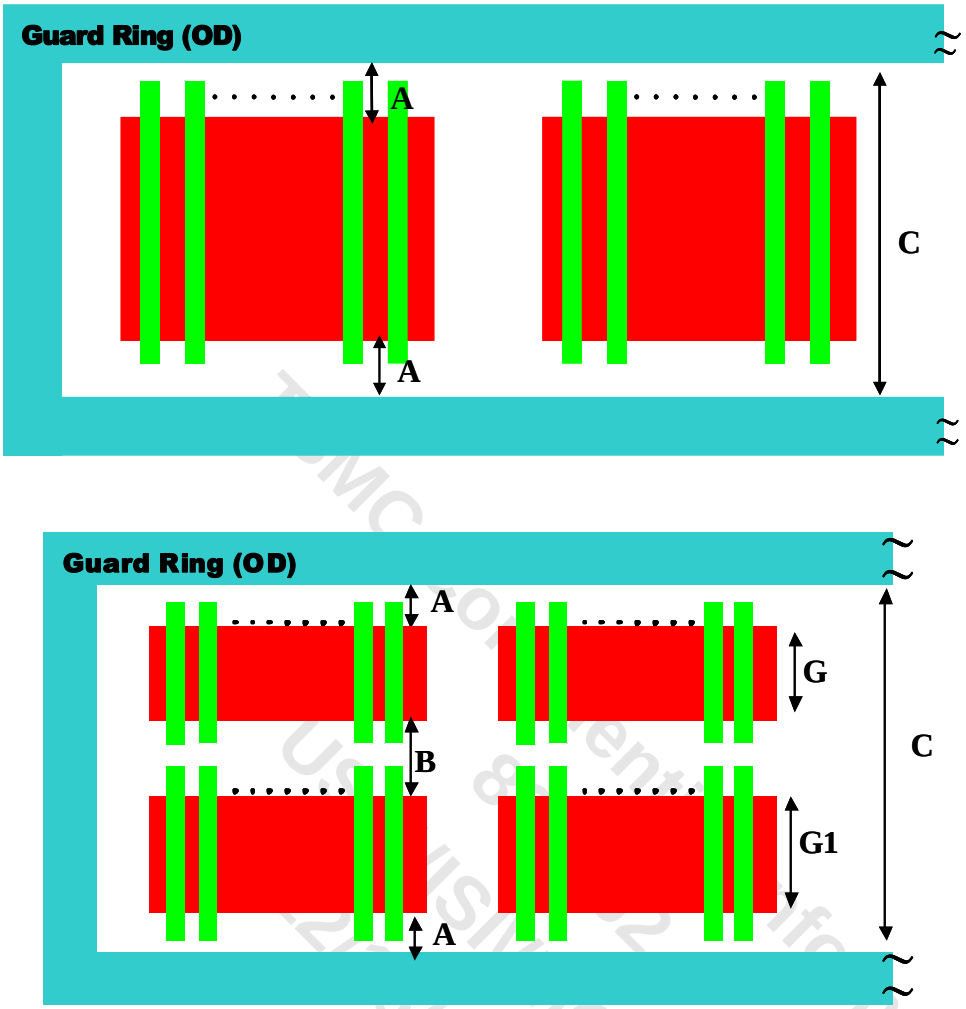

Figure 4.5.19.1.3

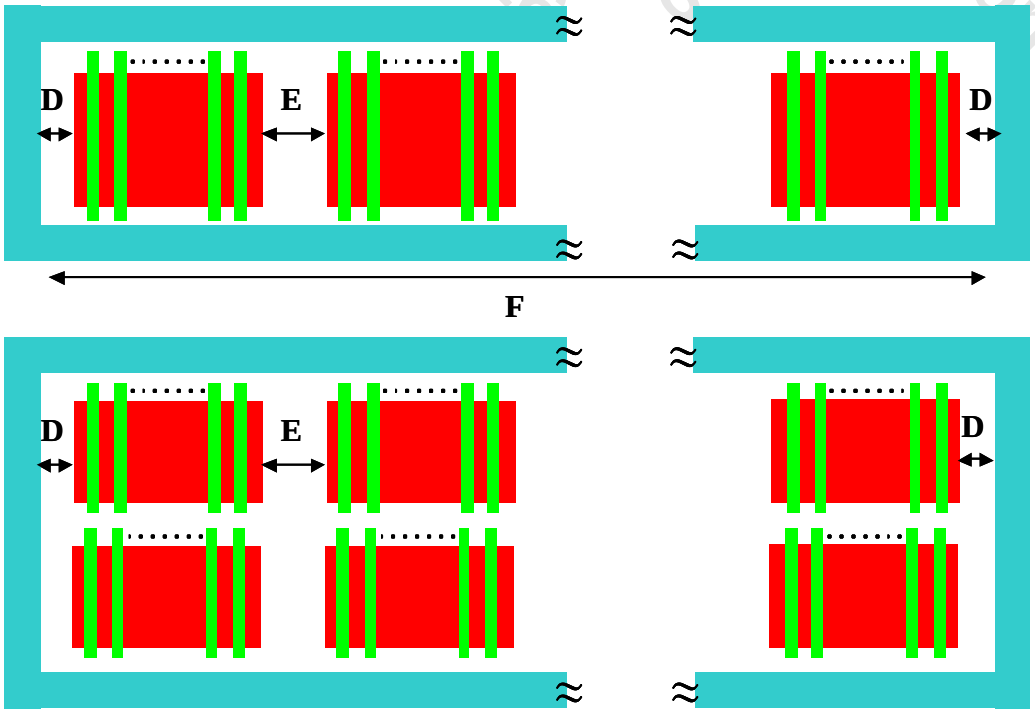

Figure 4.5.19.1.4

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4.5.19.2 Breakdown Characterization Guidelines

The breakdown characterization of HVMOS is checked by Id-Vd with different active OD width and finger number of PO gate. The rules defined here are based on 2um OD to OD spacing between active region and well pick-up ring (Fig.4.5.19.2.2), and the finger number of PO gate is ranged from 1 to 64.

Rule No.	Description	Label		Rule
BV.W.1g	Recommended Maxium HV NMOS channel width	A	≤	10
BV.W.2g	Recommended Maxium HV PMOS channel width	B	≤	50
BV.R.1g	Recommended Maximum finger number of PO gate in the same OD.	C	≤	64

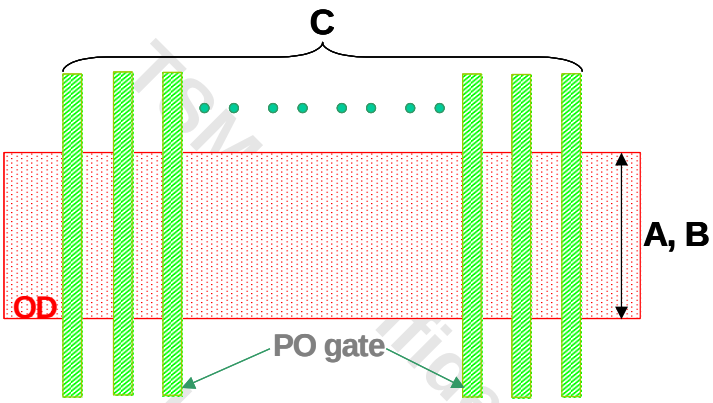

Fig.4.5.19.2.1

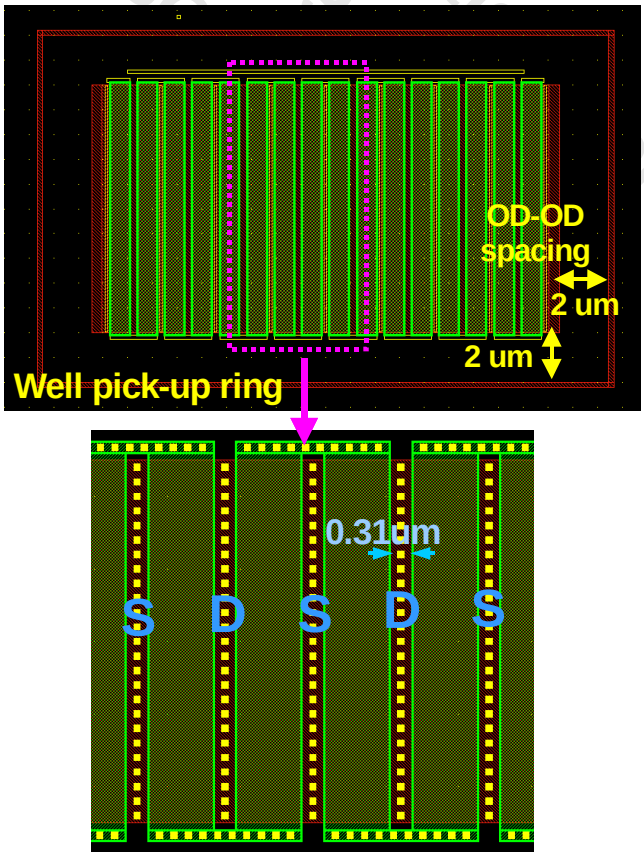

Fig.4.5.19.2.2

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4.5.20 P+ Source/Drain Ion Implantation (PP) Layout Rules (Mask ID: 197)

Rule No.	Description	Label		Rule
PP.W.1	Width	A	≥	0.18
PP.S.1	Space	B	≥	0.18
PP.S.2	Space to N+ACTIVE (non-butted)	C	≥	0.13
PP.S.3	Space to {N+ACTIVE OR NW STRAP} (butted)	D	=	0.00
PP.S.4	Space to NW STRAP (non-butted)	E	≥	0.02
PP.S.5	{PP edge on OD} space to NMOS GATE	F	≥	0.32
PP.S.6	Butted PW STRAP space to PO in the same OD [the butted N+ACTIVE extending 0 < J1 < 0.16 μm]	G	≥	0.32
PP.S.7	Space to N-type unsilicided OD/PO	H	≥	0.20
PP.EN.1	{NP OR PP} enclosure of PO (except DPO)	I	≥	0.15
PP.EX.1	Extension on P+ACTIVE	J	≥	0.13
PP.EX.2	Extension on PW STRAP	K	≥	0.02
PP.EX.3	Extension on P-type unsilicided OD/PO	L	≥	0.20
PP.EX.4	{PP edge on OD} extension on PMOS GATE	M	≥	0.32
PP.O.1	Overlap of OD	N	≥	0.13
PP.A.1	Area	O	≥	0.122
PP.A.2	Enclosed area	P	≥	0.122
PP.A.3	Area of butted PW STRAP	Q	≥	0.04
PP.R.1	PP must fully cover {PMOS GATE SIZING 0.16 μm}	R	≥	0.16
PP.R.2	Overlap of NP is not allowed			
PP.R.3	OD must be fully covered by {NP OR PP} (except DOD)			
PP.R.4	PO must be fully covered by {NP OR PP} (except DPO)			

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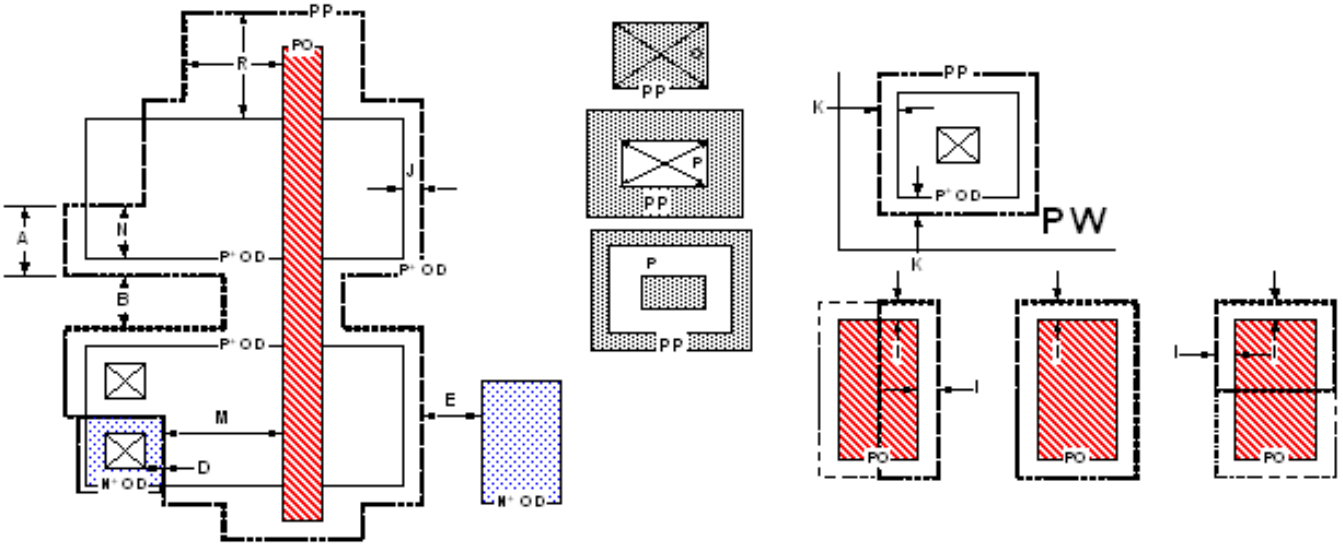
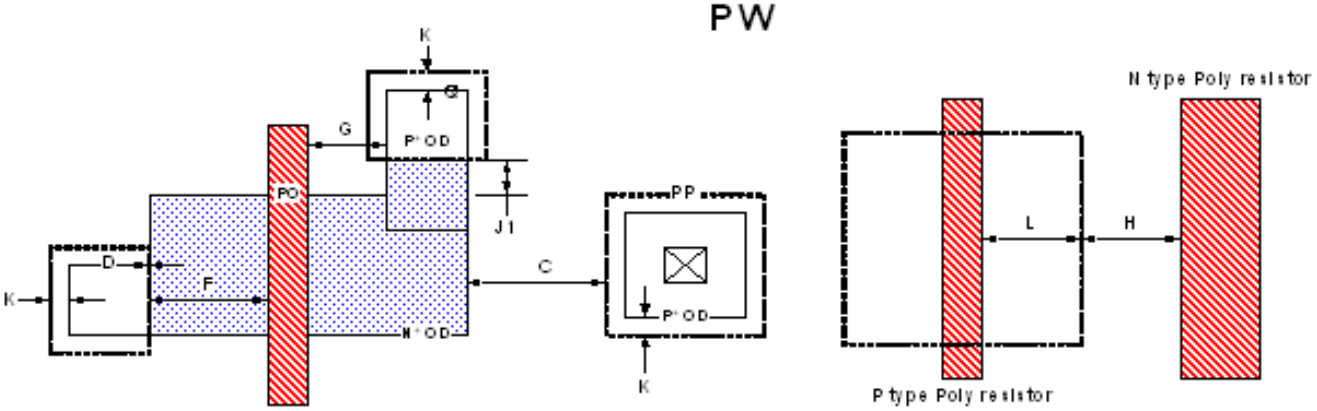
PP



NW

PW



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4.5.21 N+ Source/Drain Ion Implantation (NP) Rules (Mask ID: 198)

Rule No.	Description	Label		Rule
NP.W.1	Width	A	≥	0.18
NP.S.1	Space	B	≥	0.18
NP.S.2	Space to P+ACTIVE (non-butted)	C	≥	0.13
NP.S.3	Space to {P+ACTIVE OR PW STRAP} (butted)	D	=	0.00
NP.S.4	Space to PW STRAP (non-butted)	E	≥	0.02
NP.S.5	{NP edge on OD} space to PMOS GATE	F	≥	0.32
NP.S.6	Butted NW STRAP space to PO in the same OD [the butted P+ACTIVE extending 0 < J1 < 0.16 µm]	G	≥	0.32
NP.S.7	Space to P-type unsilicided OD/PO	H	≥	0.20
NP.EN.1	{NP OR PP} enclosure of PO (except DPO)	I	≥	0.15
NP.EX.1	Extension on N+ACTIVE	J	≥	0.13
NP.EX.2	Extension on NW STRAP	K	≥	0.02
NP.EX.3	Extension on N-type unsilicided OD/PO	L	≥	0.20
NP.EX.4	{NP edge on OD} extension on NMOS GATE	M	≥	0.32
NP.O.1	Overlap of OD	N	≥	0.13
NP.A.1	Area	O	≥	0.122
NP.A.2	Enclosed area	P	≥	0.122
NP.A.3	Area of butted NW STRAP	Q	≥	0.04
NP.R.1	NP must fully cover {NMOS GATE SIZING 0.16 µm}	R	≥	0.16
NP.R.2	Overlap of PP is not allowed			
NP.R.3	OD must be fully covered by {NP OR PP} (except DOD)			
NP.R.4	PO must be fully covered by {NP OR PP} (except DPO)			

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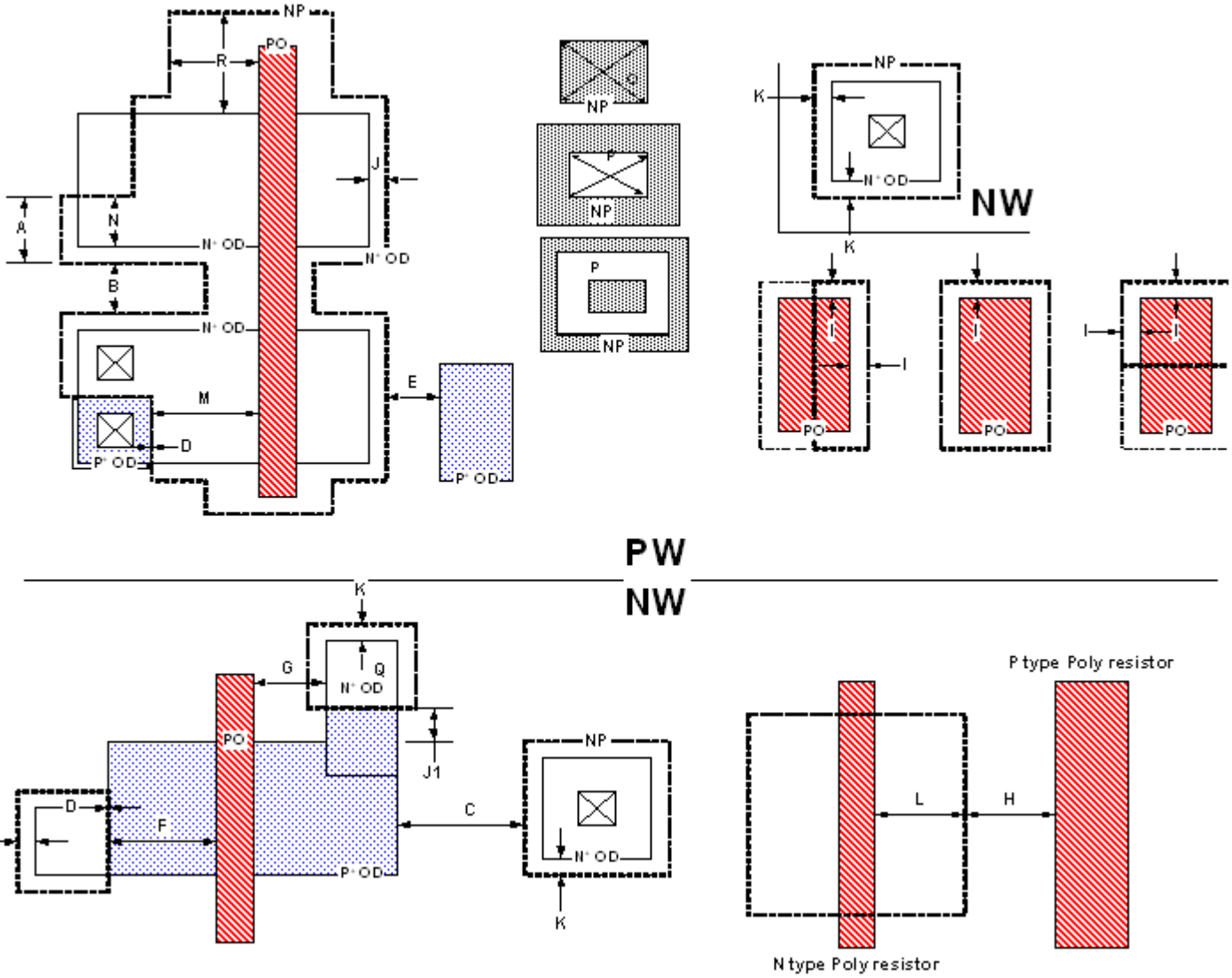
NP



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4.5.22 Layout Rules for LDD Mask Logical Operations

N1V/N2V/P1V/P2V and VTC_N/VTC_P/VTL_N/VTL_P

As a default, TSMC generates some masking layers from drawn layers by logical operations. By default, these include N1V/N2V/P1V/P2V and VTC_N/VTC_P/VTL_N/VTL_P masks. The following rules and recommendations (Fig. 1 - Fig. 6) are defined to avoid small patterns during mask making.

Warning:

If the rules is not followed, the mask making cycle time will be seriously impacted.

The following are special requirements.

d ≥ 0.18 μm	The minimum extension/clearance between two corners of two layers
X/Y (the extension/space between two edges of two layers in an X/Y)	If either dimension X or Y < 0.18 μm (including 0, 2 edges aligned), the other dimension must be ≥ 0.18 μm.

Rule No.	Description			Rule
LDN.EX.1	NP extension on NW	Fig.1	≥	0.18
LDN.EX.2	NP extension on {OD2 OR DCO}	Fig.2	≥	0.18
LDN.EX.3	NP extension on {RH OR BJTDMY}	Fig.1	≥	0.18
LDN.EX.4	NP extension on VAR	Fig.1	≥	0.18
LDN.O.1	NP overlap of {OD2 OR DCO}	Fig.3	≥	0.18
LDP.EX.1	PP extension on {OD2 OR DCO}	Fig.2	≥	0.18
LDP.EX.2	PP extension on {RH OR BJTDMY}	Fig.1	≥	0.18
LDP.EX.3	PP extension on VAR	Fig.1	≥	0.18
LDP.O.1	PP overlap of NW	Fig.3	≥	0.18
LDP.O.2	PP overlap of {OD2 OR DCO}	Fig.3	≥	0.18
VT.S.1	VTL_N space to {(OD2 OR NW) OR DCO }	Fig.5	≥	0.18
VT.EX.2	NW extension on {(OD2 OR VTL_P) OR DCO }	Fig.6	≥	0.18

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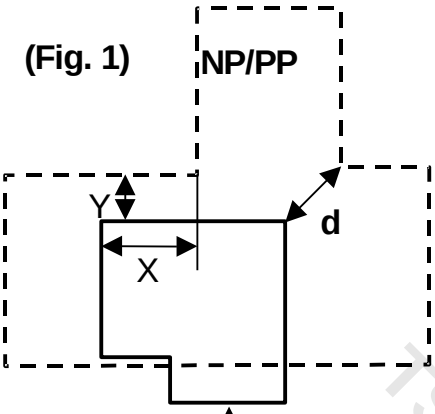
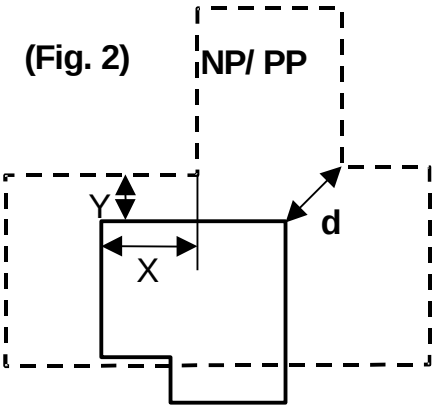
(Fig. 1) NP/PP



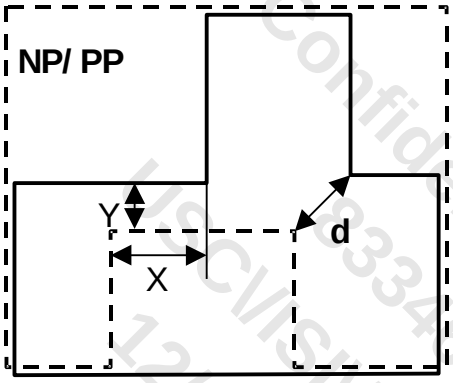
NW/RH/BJTDMY/VAR

(Fig. 2) NP/ PP



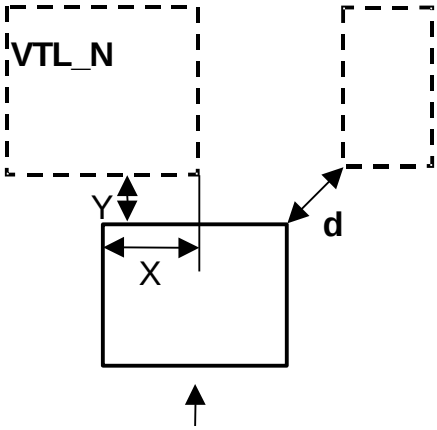
(OD2 OR DCO)

(Fig. 3) NP/ PP



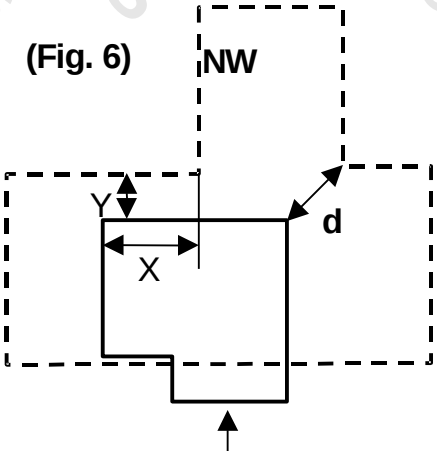
NW/ (OD2 OR DCO)

(Fig. 5) VTL_N



((OD2 OR NW) OR DCO)

(Fig. 6) NW



((OD2 OR VTL_P) OR DCO)

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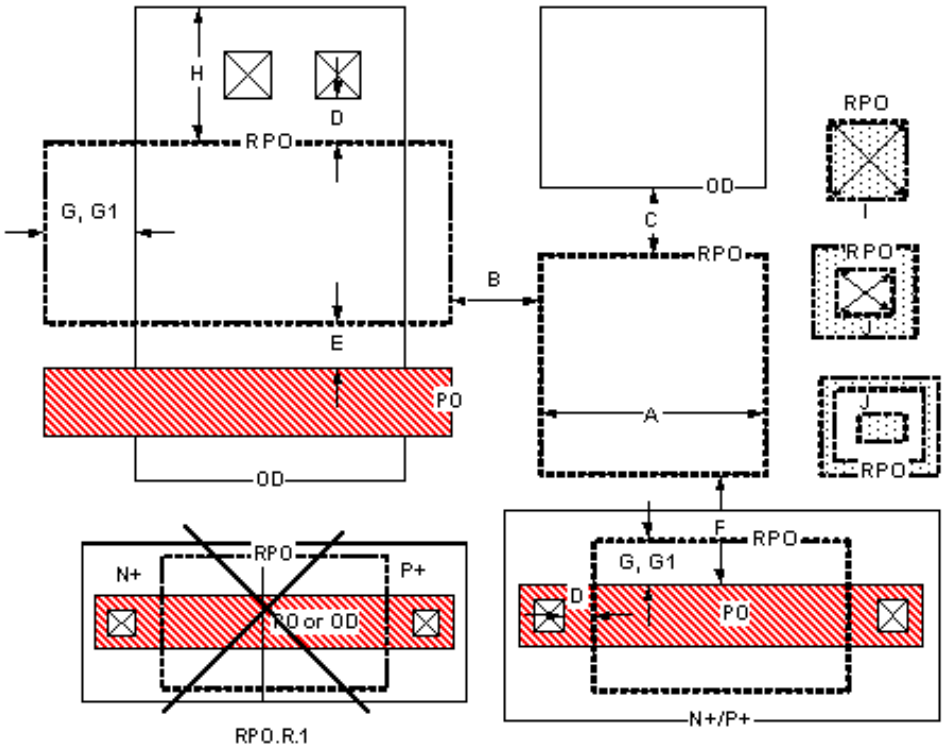
4.5.23 Resist Protection Oxide (RPO) Layout Rules (Mask ID: 155)

Rule No.	Description	Label		Rule
RPO.W.1	Width	A	≥	0.43
RPO.S.1	Space	B	≥	0.43
RPO.S.2	Space to OD	C	≥	0.22
RPO.S.3	Space to CO (overlap of CO is not allowed.)	D	≥	0.22
RPO.S.4	Space to GATE (overlap of GATE is not allowed except ESD circuit.)	E	≥	0.38
RPO.S.5	Space to PO	F	≥	0.30
RPO.EX.1	Extension on unsilicided OD/PO	G	≥	0.22
RPO.EX.1.1	Extension on unsilicided OD/PO [RPO width >10 μm]	G1	≥	0.30
RPO.EX.2	OD extension on RPO	H	≥	0.22
RPO.A.1	Area	I	≥	1.00
RPO.A.2	Enclosed area	J	≥	1.00
RPO.R.1	Butted NP/PP on unsilicided OD/PO is not allowed.			

RPO



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4.5.24 OD and Poly Resistor Recommendations and Guidelines

RH layer is required for OD and poly resistors. RH layer is a dummy layer that blocks NLDD or PLDD implants in the logic operations that generate N1V, N2V, P1V, and P2V.

Unsilicided OD resistor: {RH AND (RPO AND OD)}

Unsilicided PO resistor: {RH AND (RPO AND PO)}

Rule No.	Description	Label		Rule
RES.2®	Recommended minimum width(W), length(L) and square number (L/W) for unsilicided OD/PO resistor for SPICE simulation accuracy. Square number can not be checked by DRC Width ≥ 0.4 μm (Checked by DRC) Length ≥ 0.4 μm (Checked by DRC) Square number ≥ 1 (Not checked by DRC)		≥	0.4(width) 0.4(length) 1 (L/W)
RES.8®	**For unsilicided OD resistor in the source or drain of MOS** Recommended RH space to Gate of unsilicided OD resistor in the source or drain of MOS for SPICE simulation accuracy.		≥	0.185
RES.9®	**For unsilicided OD/PO resistor** Recommended RH enclosure of unsilicided OD/PO resistor for SPICE simulation accuracy.		≥	0.13
RES.8	**For unsilicided OD/PO resistor** RH space to Gate ≥ 0.16. (Overlap is not allowed)			
RES.10	**For unsilicided PO resistor** RPO intersecting (PO AND RH) must form two or more POs (except BJT or ESD circuits)			
RES.11	**For unsilicided OD resistor** RPO intersecting (OD AND RH) must form two or more ODs (except BJT or ESD circuits)			
RES.21	**For unsilicided OD resistors** NP OD resistor is not allowed interacting with NW. DRC will flag {(((OD AND NP) AND RH) AND RPDMY) INTERACT NW}			
RES.22	**For unsilicided OD resistors** PP OD resistor is only allowed inside NW. DRC will flag {(((OD AND PP) AND RH) AND RPDMY) NOT INSIDE NW}			
RES.12g	**For unsilicided PO resistor** {RPO AND PO} must be fully covered by RH (except BJT or ESD circuits)			
RES.13g	**For unsilicided OD resistor** {RPO AND OD} must be fully covered by RH (except BJT or ESD circuits)			
RES.15g^{U}	Recommended to use rectangle shape resistor for the SPICE simulation accuracy			

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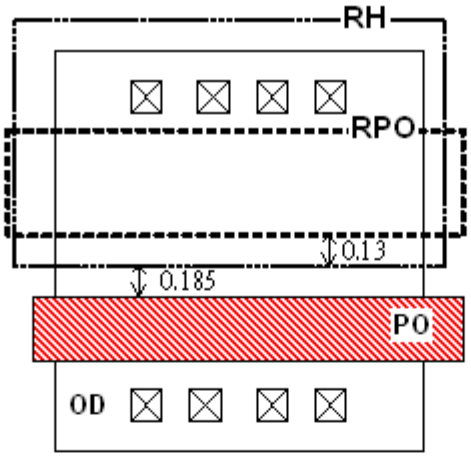
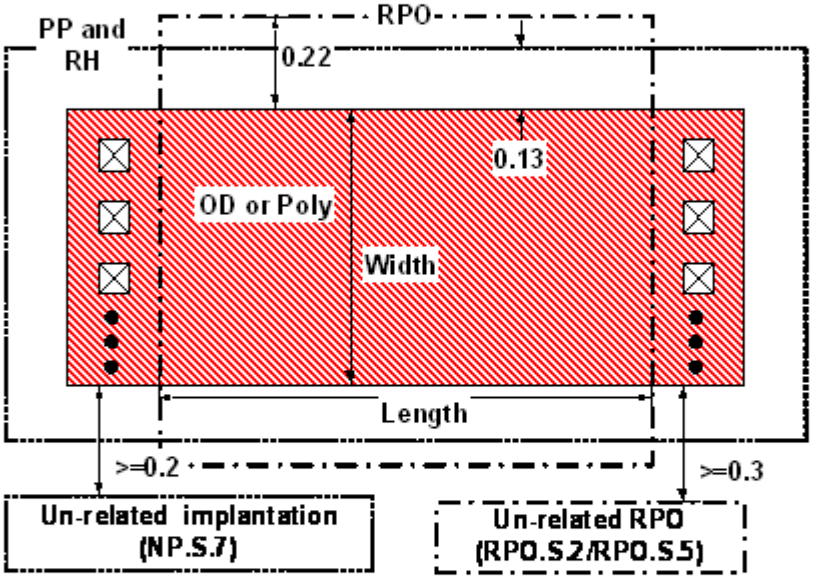
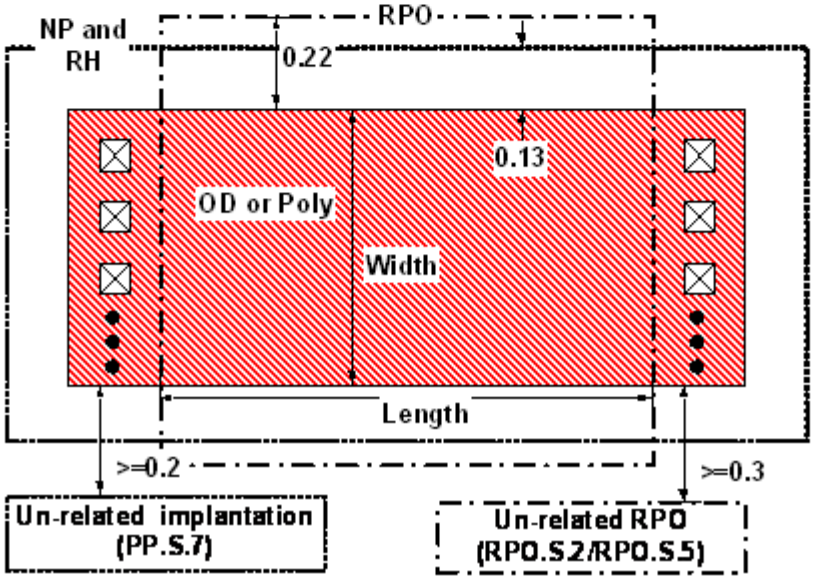


* P+ OD/Poly resistor with RPO



* N+ OD/Poly resistor with RPO



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- **The Following table describes the resistance performance and variation with sampled width/legnth:**

  The data is an example based on CLN65LP SPICE model: T-N65-CL-SP-009 (V1.2) with the bias condition of 0.01V. It contains one typical case (TT) and two corner cases, slow (SS) and fast (FF). Make sure to refer to the most updated SPICE model version of each different technology to design your resistor.

Resistor	W(um)	L(um)	SQ (L/W)	TT (ohm)	SS (ohm)	FF (ohm)	TT/SS Diff	TT/FF Diff
Unsilicided N+OD resistor	2.00	4.00	2.0	245.8	298.4	193.5	21.41%	-21.26%
	1.00	2.00	2.0	251.4	310.3	192.7	23.44%	-23.33%
	0.70	1.40	2.0	256.2	320.6	192.1	25.13%	-24.99%
	0.40	0.80	2.0	267.9	346.3	190.9	29.23%	-28.74%
	2.00	10.00	5.0	605.8	733.2	479.4	21.02%	-20.86%
	1.00	5.00	5.0	611.6	750.6	473.2	22.74%	-22.63%
	0.70	3.50	5.0	616.4	765.7	468.1	24.21%	-24.06%
	0.40	2.00	5.0	628.4	803.9	456.3	27.91%	-27.39%
Unsilicided P+OD resistor	2.00	4.00	2.0	493.7	595.1	392.1	20.54%	-20.58%
	1.00	2.00	2.0	496.9	617.3	374.3	24.24%	-24.67%
	0.70	1.40	2.0	499.5	637.1	360.4	27.55%	-27.85%
	0.40	0.80	2.0	506.1	690.8	330.5	36.49%	-34.69%
	2.00	10.00	5.0	1230.0	1481.4	978.1	20.44%	-20.48%
	1.00	5.00	5.0	1233.9	1530.9	931.5	24.07%	-24.51%
	0.70	3.50	5.0	1237.1	1575.5	895.1	27.35%	-27.65%
	0.40	2.00	5.0	1245.3	1697.2	816.2	36.29%	-34.45%
Unsilicided N+PO resistor	2.00	4.00	2.0	320.3	386.7	252.6	20.75%	-21.12%
	1.00	2.00	2.0	333.9	413.0	253.4	23.68%	-24.12%
	0.70	1.40	2.0	345.9	437.3	253.8	26.41%	-26.63%
	0.40	0.80	2.0	378.1	507.9	254.6	34.34%	-32.66%
	2.00	10.00	5.0	795.2	958.9	628.5	20.59%	-20.97%
	1.00	5.00	5.0	824.6	1017.9	627.8	23.44%	-23.87%
	0.70	3.50	5.0	851.1	1073.3	627.1	26.11%	-26.32%
	0.40	2.00	5.0	923.3	1237.5	625.1	34.02%	-32.30%
Unsilicided P+PO resistor	2.00	4.00	2.0	1406.9	1606.0	1202.1	14.15%	-14.56%
	1.00	2.00	2.0	1434.7	1704.4	1141.5	18.80%	-20.44%
	0.70	1.40	2.0	1459.4	1798.5	1094.2	23.24%	-25.02%
	0.40	0.80	2.0	1524.5	2085.2	991.9	36.77%	-34.94%
	2.00	10.00	5.0	3515.8	4012.9	3004.6	14.14%	-14.54%
	1.00	5.00	5.0	3584.0	4256.8	2852.4	18.77%	-20.41%
	0.70	3.50	5.0	3644.5	4490.4	2733.7	23.21%	-24.99%
	0.40	2.00	5.0	3804.8	5203.1	2476.5	36.75%	-34.91%

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4.5.25 MOS Varactor Layout Rules (VAR)

MOS varactor provides NMOS in NW capacitor structure for core and IO region

VAR: You must provide this layer (CAD layer: 143) to generate LDD logical operation, if the MOS varactor is used.

Rule No.	Description	Label		Rule
VAR.W.1	Length of {gate AND VAR} Please follow table 4.5.25.1 for SPICE model valid range.	A	≥	0.2
VAR.W.4	Channel width of {gate AND VAR} Please follow table 4.5.25.1 for SPICE model valid range.	G	≥	0.4
VAR.S.1	Space to ACTIVE	B	≥	0.13
VAR.EN.1	Enclosure of OD	D	≥	0.16
VAR.R.1	VAR layer must be drawn to fully cover the varactor devices.			
VAR.R.2	Overlap of VTL_N, VTL_P, VTH_N, VTH_P, NT_N, mVTL, PW, or RPO is not allowed.			
VAR.R.3	PP overlap of {gate AND VAR} is not allowed.			
VAR.R.4	Overlap to {(PO AND ACTIVE) SIZING 0.16 μm} is not allowed			
VAR.R.5	NP must fully cover {(((VAR AND GATE) sizing 0.19) AND OD) sizing 0.13}			

Table note:

Due to the intrinsic gate leakage, you need to do SPICE simulation carefully while large area of MOS varactor is designed in the thin oxide area.

The follow table is the width/length of baseband and RF model in SPCIE model. Please refer the below table with W/L for varactor application.

Table 4.5.25.1 minimum W/L of baseband and RF model for SPICE valid range

	Technology	Core & I/O	Baseband (W/L = G/A)	RF model (W/L = G/A)
			N+/NW VAR	N+/NW VAR
N65 & N55	N65G	Core 1.0V	1.0/1.0	
		IO (1.8V, 2.5V)	1.0/1.0	
	N65GP	Core 1.0V	1.0/1.0	
		IO (1.8V, 2.5V) -CLN65	1.0/1.0	
		IO (2.5V) -CMN65	1.0/1.0	
	CLN65LP/CMN65LP	Core 1.2V	1.0/1.0	0.4/0.2
		IO (2.5V, 3.3V)	1.0/1.0	0.4/0.4
	N65ULP	Core 1.0V	1.0/1.0	
		IO (2.5V)	1.0/1.0	
	N65LPG	Core 1.2V or 1.0V	1.0/1.0	
		IO (2.5V)	1.0/1.0	
	CLN55GP	Core 1.0V	0.9*(1.0/1.0)	
		IO (1.8V, 2.5V, 3.3V)	0.9*(1.0/1.0)	
	N55LP	Core 1.2V	0.9*(1.0/1.0)	0.4/0.2
		IO (2.5V)	0.9*(1.0/1.0)	0.4/0.4

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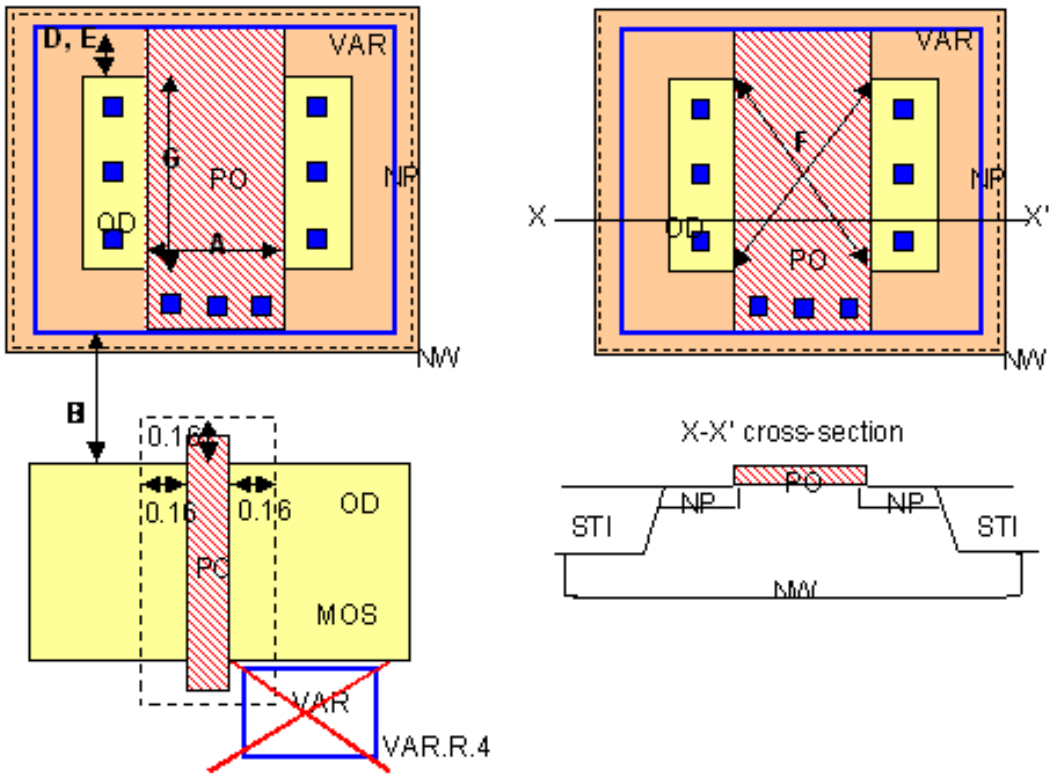
VAR



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4.5.26 Contact (CO) Layout Rules (Mask ID: 156)

Rule No.	Description	Label		Rule
CO.W.1	Width (maximum = minimum except for seal-ring and fuse protection ring)	A	=	0.09
CO.W.2	Width of CO bar. CO bar is only allowed in seal ring. CO bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover CO bar if CO bar is used.		=	0.09
CO.S.1	Space	B	≥	0.11
CO.S.2	Space to 3-neighboring CO (< 0.15 µm distance)	C	≥	0.14
CO.S.2.1	Space to neighboring CO [different net and common parallel run length > 0]	B1	≥	0.14
CO.S.2.2	Space to neighboring CO [different net]	B3	≥	0.12
CO.S.3	Space to GATE (Overlap of GATE is not allowed) [space can be ≥ 0.05 µm inside SRAM word line decoder covered by layer 186;4, and space ≥ 0.043 µm covered by 186;5]	D	≥	0.055
CO.S.3®	Recommended CO space to GATE to reduce the short possibility caused by particle	D	≥	0.065
CO.S.4	{CO inside PO} space to OD	E	≥	0.07
CO.S.5	{CO inside OD} space to 1.8V or 2.5V or 3.3V GATE	F	≥	0.09
CO.S.6	Space to butted PP/NP edge on OD (overlap of NP/PP boundary on OD is not allowed.)	G	≥	0.06
CO.EN.0	Enclosure by PO is defined by either {CO.EN.2 and CO.EN.3} or CO.EN.4.			
CO.EN.1	Enclosure by OD	H	≥	0.015
CO.EN.1®	Recommended CO enclosure by OD to avoid high Rc.	H	≥	0.04
CO.EN.1.1	Enclosure by OD [at least two opposite sides]	H1	≥	0.03
CO.EN.2	Enclosure by PO	J	≥	0.01
CO.EN.3	Enclosure by PO [at least two opposite sides]	K	≥	0.04
CO.EN.3®	Recommended CO enclosure by PO [at least two opposite sides] to avoid high Rc.	K	≥	0.06
CO.EN.4	Enclosure by PO [all sides].	L	≥	0.03
CO.R.2	Overlap of RPO is not allowed.			
CO.R.3	45-degree rotated CO is not allowed.			
CO.R.4	CO must be fully covered by M1 and {OD OR PO}.			
CO.S.6g	Recommended to put contacts at both source side and butted well pickup side to avoid high Rs. DRC can flag if the STRAP is butted on source, one of STRAP and source is without CO.			
CO.R.1g^{U}	Recommended to put {CO inside PO} space to GATE as close as possible to avoid high Rs.			
CO.R.5g	Recommend using redundant CO to avoid high Rc wherever layout allows 1. Recommended to use double CO or more on the resistor connection. 2. Double CO on Poly gate to reduce the probability of high Rc 3. Recommend putting multiple and symmetrical source/drain CO for SPICE simulation accuracy. 4. If it is hard to increase the CO to gate spacing (CO.S.3®) for the large transitor, limit the number of source/drain CO: to have the necessary CO number for the current, and then distribute the CO evenly on the Source/Drain area. If possible, also increase the CO to gate spacing (to reduce the short possibility by particle) 5. DRC can flag single CO.			

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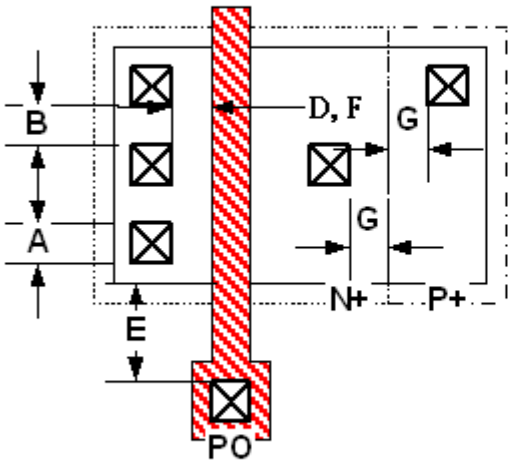
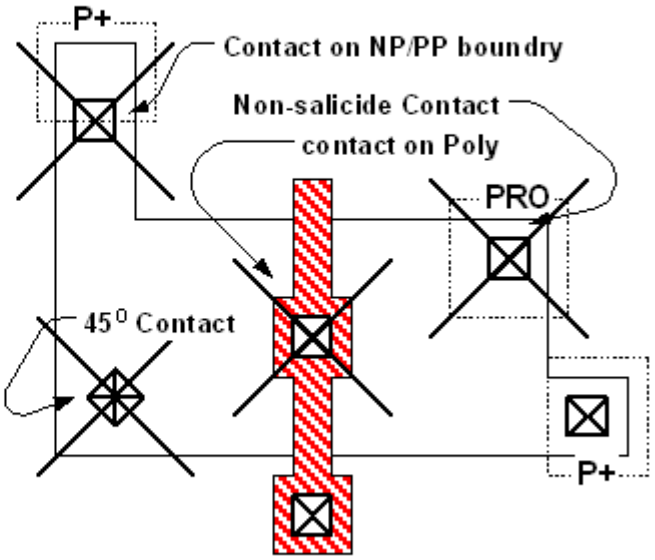
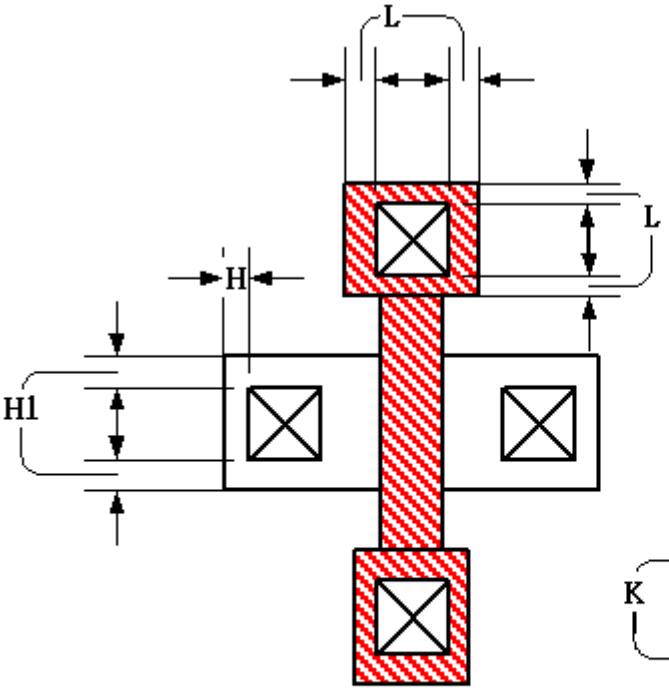
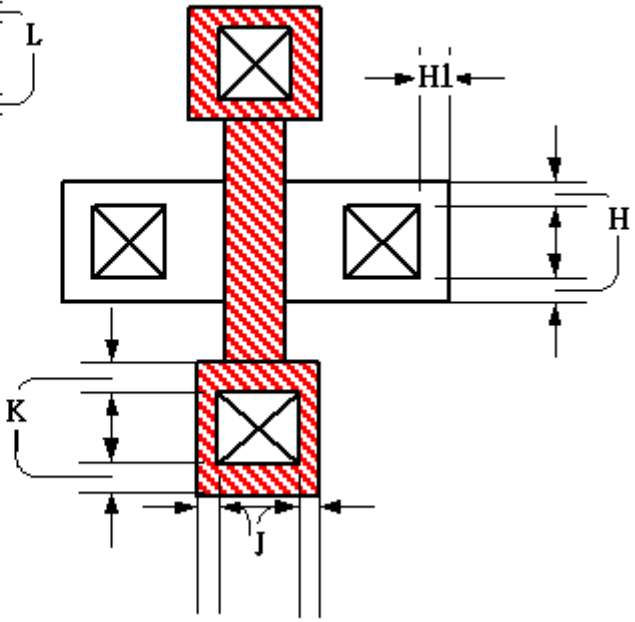
CO









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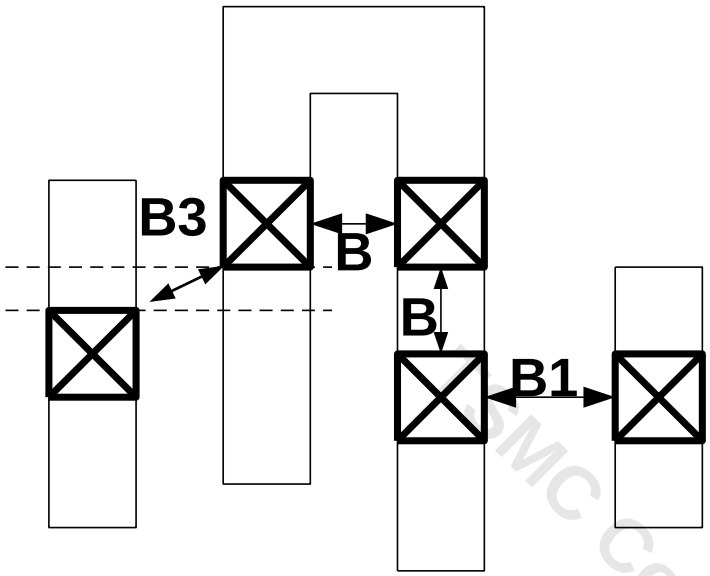
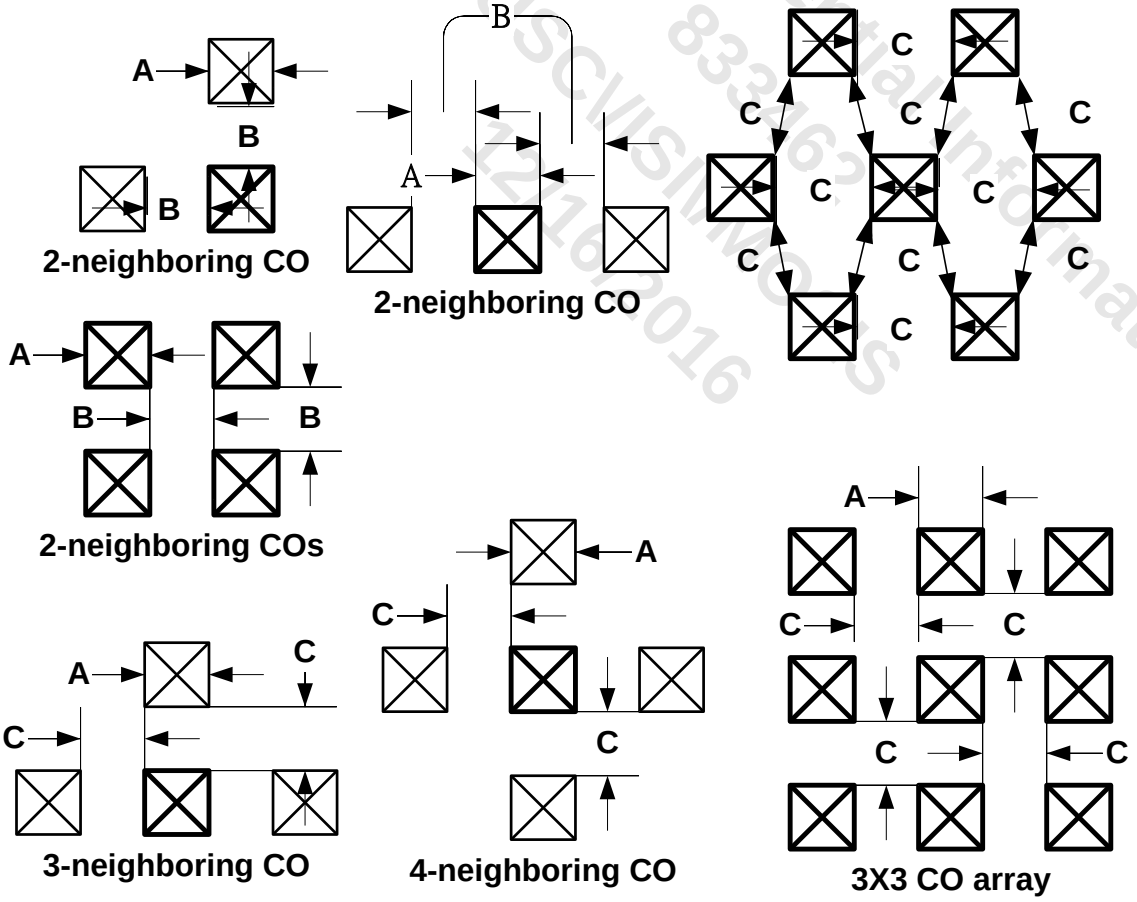


CO space to neighboring CO in the same net or in the different net



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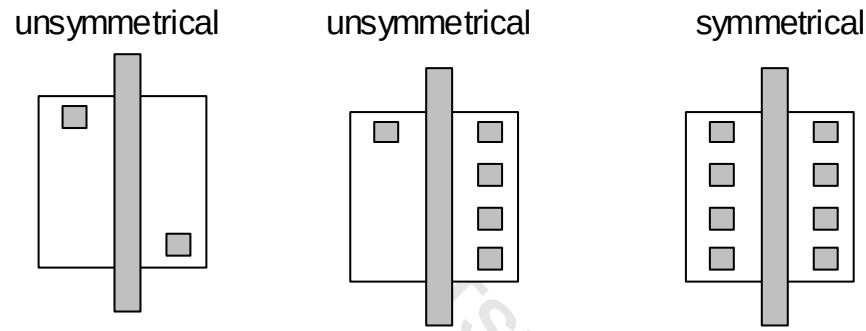
Item 3 in CO.R.5g



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4.5.27 Metal-1 (M1) Layout Rules (Mask ID: 360)

Rule No.	Description	Label		Rule
M1.W.1	Width	A	≥	0.09
M1.W.2	Width of 45-degree bent M1 Please make sure the vertex of 45-degree pattern is on 5nm grid (refer to the guideline, G.6g^{U}, in section 3.7)	B	≥	0.19
M1.W.3	Maximum width	C	≤	12.00
M1.S.1	Space	D	≥	0.09
M1.S.1®	Recommended M1 space to reduce the short possibility caused by particle	D	≥	0.12
M1.S.2	Space [at least one metal line width > 0.20 µm (W1) and the parallel metal run length > 0.38 µm (L1)] (union projection)	E	≥	0.11
M1.S.2.1	Space [at least one metal line width > 0.42 µm (W2) and the parallel metal run length > 0.42 µm (L2)] (union projection)	E1	≥	0.16
M1.S.3	Space [at least one metal line width > 1.5 µm (W3) and the parallel metal run length > 1.5 µm (L3)] (union projection)	F	≥	0.50
M1.S.4	Space [at least one metal line width > 4.5 µm (W4) and the parallel metal run length > 4.5 µm (L4)] (union projection)	G	≥	1.50
	Note: When M1 width > 9um is used, please take care of the M1.DN.2 rule by using larger space. For example, if two M1 with width 12um and space 1.5um, it will get 94% density violation on M1.DN.2; either enlarger the M1 space (like 2um) or reduce the M1 width (like 9um) to meet M1.DN.2.			
M1.S.5	Space at M1 line-end (W<Q=0.110) in a dense-line-end configuration: If M1 has parallel run length with opposite M1 (measured with T=0.035 extension) along 2 adjacent edges of M1 [any one edge <Q distance from the corner of the two edges], then one of the space (S1 or S2) needs to be at least this value (except for small jog with edge length < 0.09um (R))	S1/S2	≥	0.11
M1.S.6	Space to 45-degree bent M1	H	≥	0.19
M1.S.7®	Recommended space between two non-M1 regions [one of the non-M1 area > 4,000,000µm²] for mask ESD concern. Non-M1 region is defined as {NOT (M1 OR DM1)} e.g. enlarge the metal width ≥ 0.35 for the guard-ring design.	N	≥	0.35
M1.EN.0	Enclosure of CO is defined by either {M1.EN.1 and M1.EN.2} or M1.EN.3.			
M1.EN.0®	Recommended enclosure of CO is defined by either M1.EN.1® or M1.EN.2®.			
M1.EN.1	Enclosure of CO	I	≥	0.00
M1.EN.1®	Recommended M1 enclosure of CO to avoid high Rc	I	≥	0.04
M1.EN.2	Enclosure of CO [at least two opposite sides]	J	≥	0.04
M1.EN.2®	Recommended M1 enclosure of CO [at least two opposite sides] to avoid high Rc.	J	≥	0.06
M1.EN.3	Enclosure of CO	K	≥	0.025
M1.EN.4	Enclosure of CO [M1 width > 1µm]	K	≥	0.04
M1.A.1	Area	L	≥	0.042
M1.A.2	Enclosed area	M	≥	0.2
	For the following M1.DN.1, M1.DN.1.1, M1.DN.2, M1.DN.4, and DM1.R.1, please refer to the "Dummy Metal Rules" section in Chapter 8 for the details.			
M1.DN.1	Minimum metal density in window 75 µm x 75 µm, stepping 37.5 µm		≥	10%
M1.DN.1.1	Maximum metal density in window 100 µm x 100 µm, stepping 50 µm		≤	80%
M1.DN.2	Maximum metal density over any 20 µm x 20 µm area (checked by stepping in 10 µm increments). The rule is applied while width of (checking window NOT Bond pad) ≥ 5		≤	90%

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Rule No.	Description	Label		Rule
	μm. M1.DN.2 would exclude the following regions: 1. Both wire bond pad and flip chip bump pad 2. Mz in {INDDMY SIZING 18 μm} 3. LMARK			
M1.DN.4	The metal density difference between any two 250 μm x 250 μm neighboring checking windows including DMxEXCL (stepping in 250 μm increments) Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient)		≤	40%
DM1.R.1	DM1 is a must. The DM1 CAD layer (TSMC default, 31;1 for DM1) must be different from the M1 CAD layer.			
M1.R.1[U]	M1 line-end must be rectangular. Other shapes are not allowed.			

Table Notes:

- To improve the metal CMP process window, you must fill the DMx globally and uniformly even if the originally drawn M1 has already met the density rule (M1.DN.1/M1.DN.2). For sensitive areas with auto-fill operations blocked by the DM1EXCL layer, it is recommended filling dummy pattern evenly by manual operations to gain a better process window and electrical performance.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations (M1.DN.1, M1.DN.2) during placement. It may have unexpected violation during the IP/macro placement due to the environment, even if the IP/macro already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.

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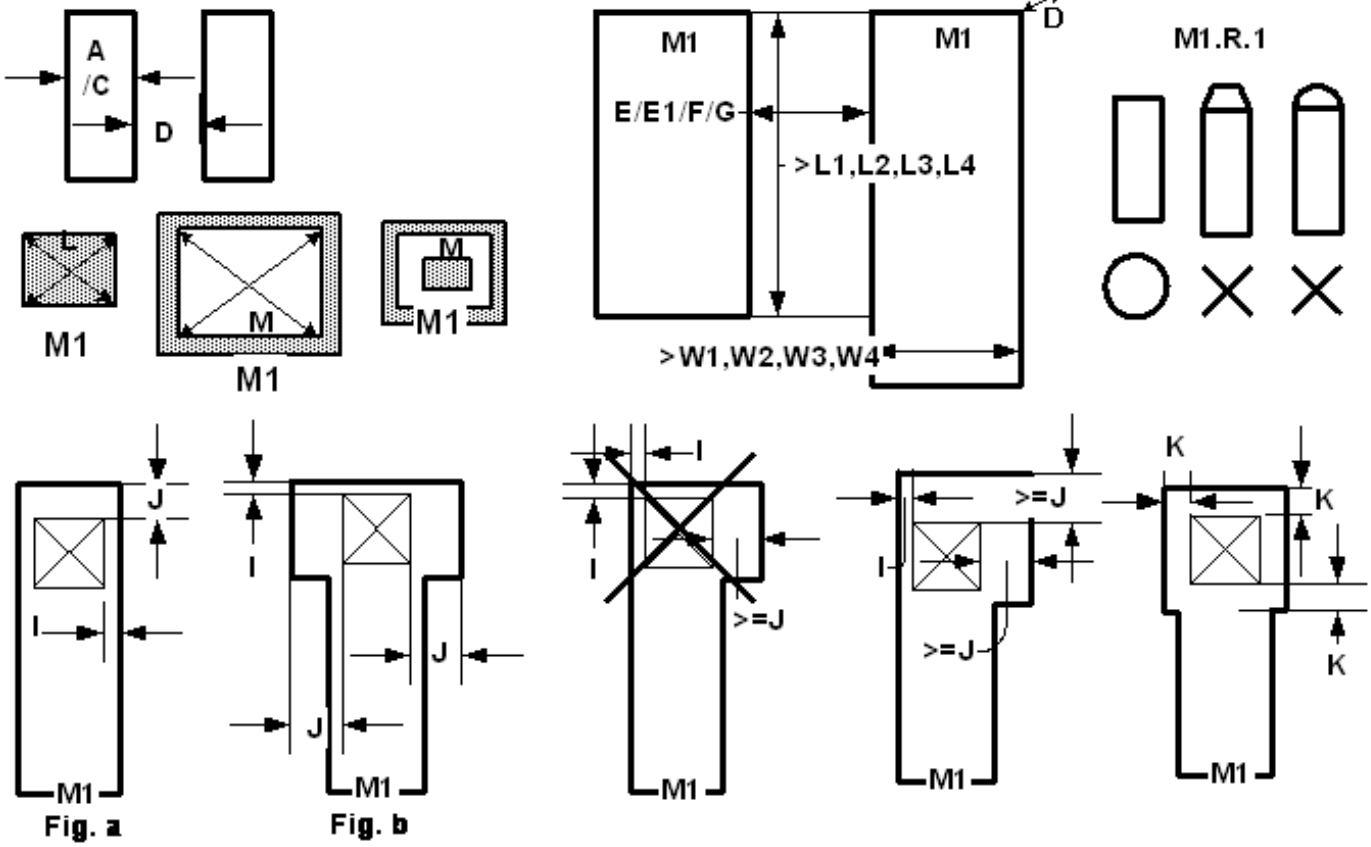
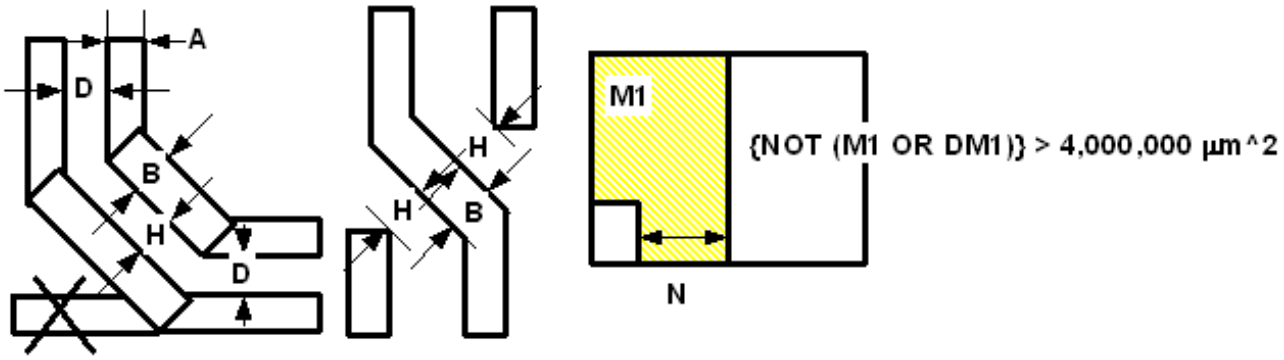
M1





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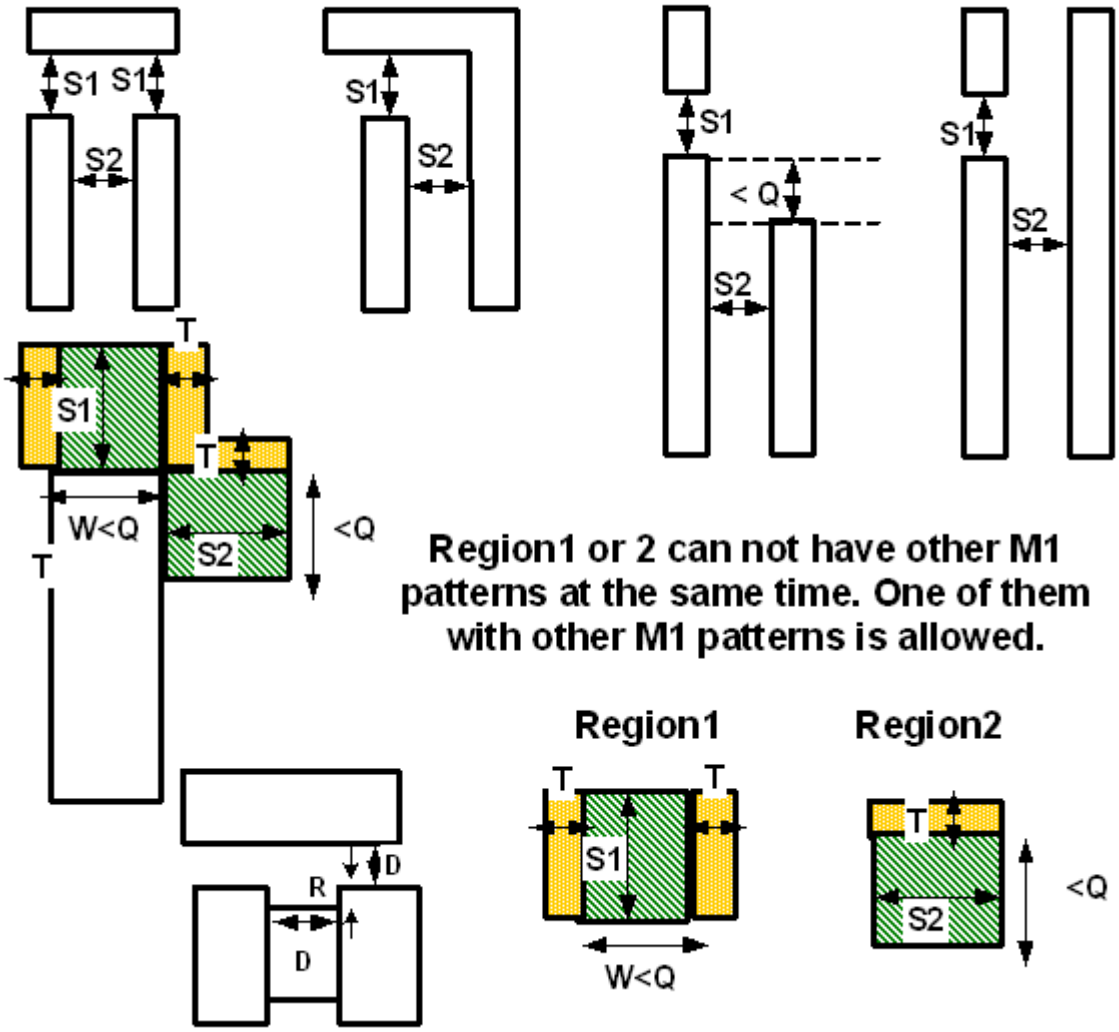
M1.S.5



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4.5.28 VIAx Layout Rules (Mask ID: 378, 378, 373, 374, 375, 376)

For the specification of metals/vias stacking sequence and associated mask id, please refer to section 2.5.

Rule No.	Description	Label		Rule
VIAx.W.1	Width (maximum = minimum except for seal-ring and fuse protection ring)	A	=	0.10
VIAx.W.2	Width of VIAx bar. VIAx bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover VIAx bar if VIAx bar is used.		=	0.10
VIAx.S.1	Space	B	≥	0.10
VIAx.S.2	Space to 3-neighboring VIAx (< 0.14 µm distance)	C	≥	0.13
VIAx.S.3	Space to neighboring VIAx [different net and common parallel run length > 0]	B1	≥	0.13
VIAx.EN.0	Enclosure by Mx or M1 is defined by either {VIAx.EN.1 and VIAx.EN.2} or VIAx.EN.3.			
VIAx.EN.0®	Recommended enclosure by Mx or M1 is defined by either VIAx.EN.1® or VIAx.EN.2®.			
VIAx.EN.1	Enclosure by Mx or M1	D	≥	0.00
VIAx.EN.1®	Recommended VIAx enclosure by Mx or M1 to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.37.	D	≥	0.04
VIAx.EN.2	Enclosure by Mx or M1 [at least two opposite sides]	E	≥	0.04
VIAx.EN.2®	Recommended VIAx enclosure by Mx or M1 [at least two opposite sides] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.37.	E	≥	0.07
VIAx.EN.3	Enclosure by Mx or M1 [all sides]	D	≥	0.03
VIAx.R.1	45-degree rotated VIAx is not allowed.			
VIAx.R.2	At least two VIAx with space ≤ 0.20 µm (S1), or at least four VIAx with space ≤ 0.25 µm (S1') are required to connect Mx and Mx+1 when one of these two metals has width and length (W1) > 0.30 µm.			
VIAx.R.3	At least four VIAx with space ≤ 0.20 µm (S2), or at least nine VIAx with space ≤ 0.35 µm (S2') are required to connect Mx and Mx+1 when one of these two metals has width and length (W2) > 0.70 µm.			
VIAx.R.4	At least two VIAx must be used for a connection that is ≤ 0.8 µm (D) away from a metal plate (either Mx or Mx+1) with length > 0.3 µm (L) and width > 0.3 µm (W). (It is allowed to use one VIAx for a connection that is > 0.8 µm (D) away from a metal plate (either Mx or Mx+1) with length > 0.3 µm (L) and width > 0.3 µm (W).)			
VIAx.R.5	At least two VIAx must be used for a connection that is ≤ 2 µm (D) away from a metal plate (either Mx or Mx+1) with length > 2 µm (L) and width > 2 µm (W). (It is allowed to use one VIAx for a connection that is > 2 µm (D) away from a metal plate (either Mx or Mx+1) with length > 2 µm (L) and width > 2 µm (W).)			
VIAx.R.6	At least two VIAx must be used for a connection that is ≤ 5 µm (D) away from a metal plate (either Mx or Mx+1) with length > 10 µm (L) and width > 3 µm (W). (It is allowed to use one VIAx for a connection that is > 5 µm (D) away from a metal plate (either Mx or Mx+1) with length > 10 µm (L) and width > 3 µm (W)).			
VIAx.R.7	VIAx must be fully covered by Mx and Mx+1.			
VIAx.R.8®	Recommended maximum consecutive stacked VIAx layer, which has only one via for each VIAx layer to avoid high Rc. (Example: VIA1~VIA4, VIA2~VIA5, VIA3~VIA6. This rule does not apply to top via. It is allowed to stack from VIA3 to VIA8 because VIA7 and VIA8 are top via. It is allowed to stack more than four VIAx layers if two or more vias in each VIAx layer are on the same metal.)		≤	4
VIAx.R.11	Single VIAx is not allowed in "H-shape" Mx+1 when all of the following conditions come into existence: (1) The Mx+1 has "H-shape" metal interact with two metal holes: both two metal hole length(L2) ≤ 5um and two metal hole area ≤ $5um^2$ (2) The VIAx overlaps on the center metal bar of this "H-shape" Mx+1 (3) The length (L) of the center metal bar ≤1um and the width of metal bar is ≤			

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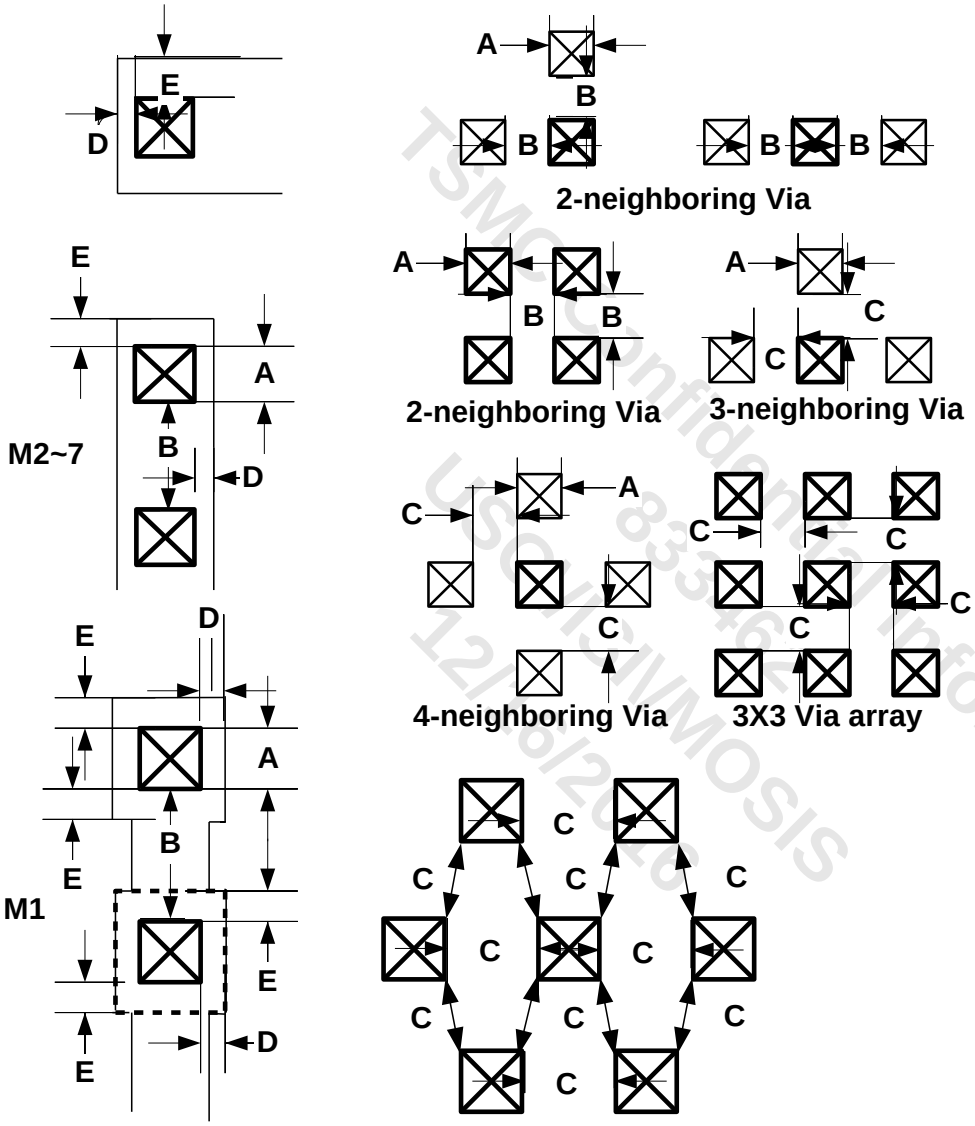
Rule No.	Description	Label		Rule
	0.3um.			
VIAx.R.9g	Recommend using redundant vias to avoid high Rc wherever layout allows. Please refer to the “Via Layout Recommendations” in the section 4.5.37. DRC can flag single via.			



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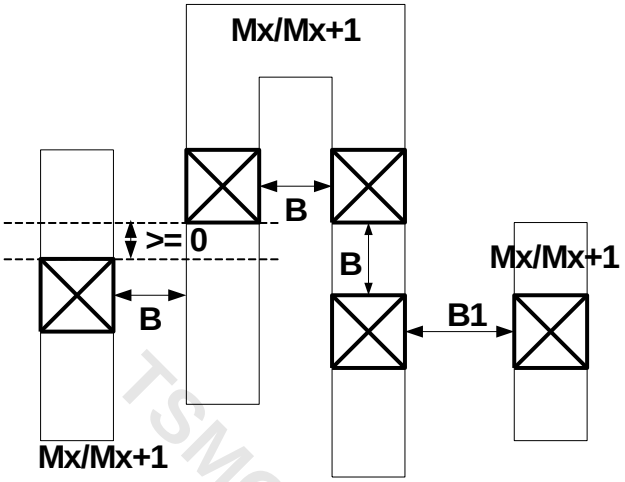

Via space to neighboring via in the same net or in the different net

Illustration of VIAx.R.8(R)

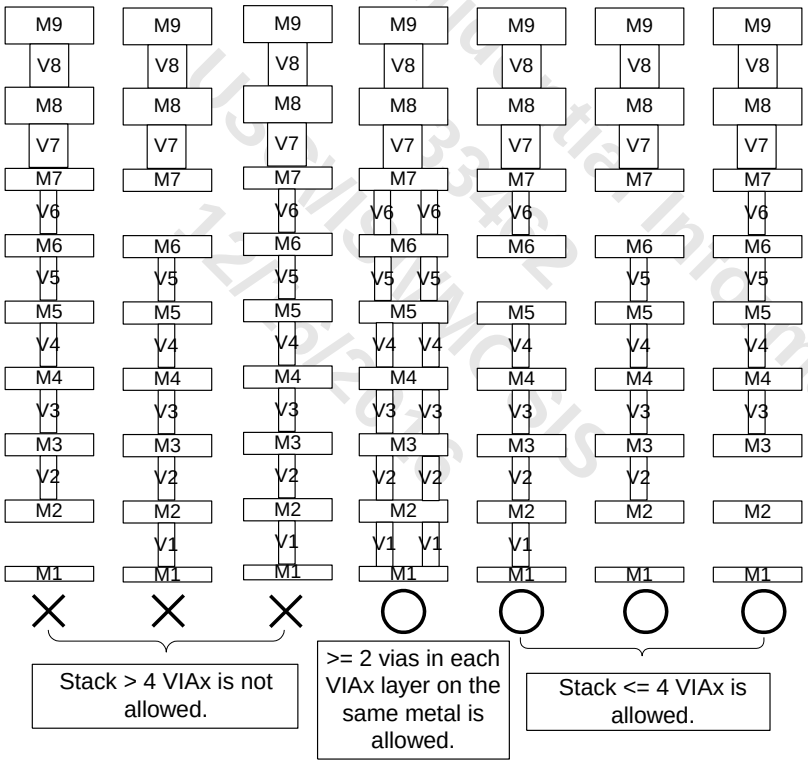

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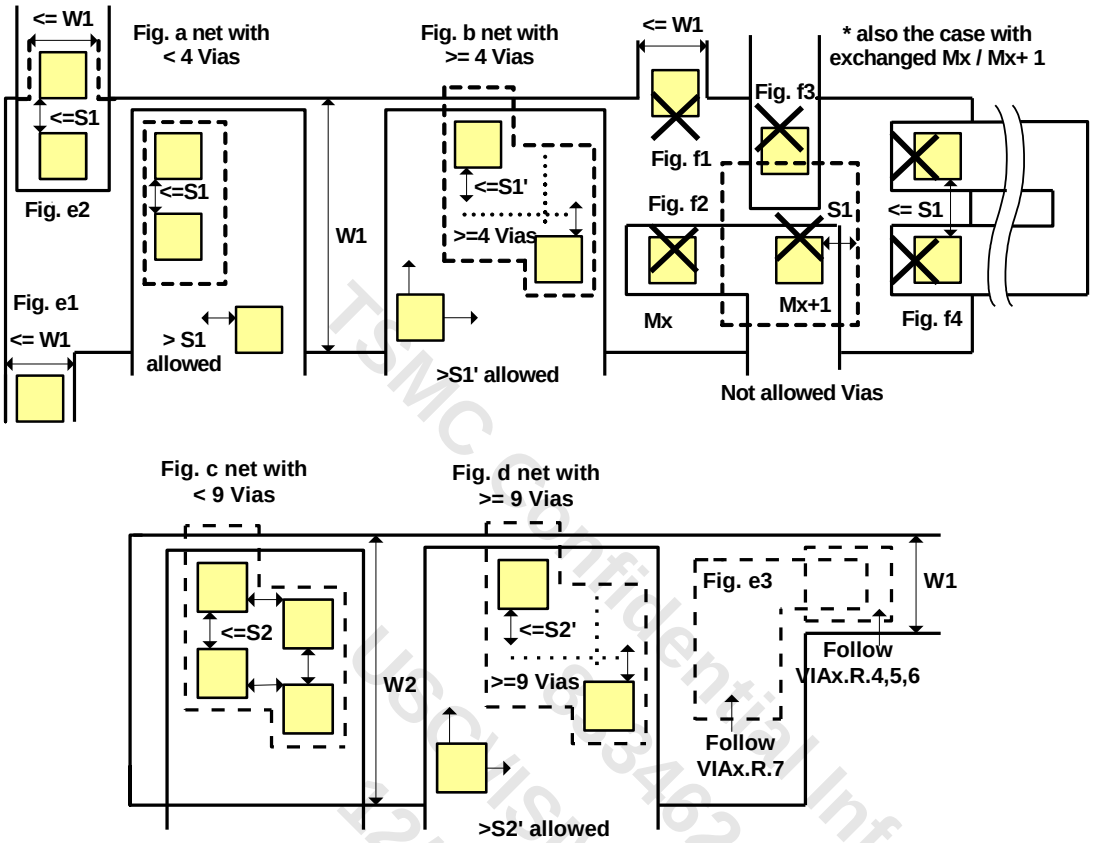
Illustration of VIAx.R.2, VIAx.R.3 Rules



Rule VIAx.R.2 0.30 µm < W1 ≤ 0.70 µm		Rule VIAx.R.3 W2 µm > 0.70 µm	
Fig. a < 4 vias	Fig. b ≥ 4 vias	Fig. c <9 vias	Fig. d ≥ 9 vias
S1 = 0.20 µm	S1’ = 0.25 µm	S2 = 0.20 µm	S2’ = 0.35 µm

Fig a. At least two vias with spacing ≤ S1 µm inside the same overlapped metal region (Mx AND Mx+1).

Fig. b At least four vias with spacing ≤ S1’ µm.

Fig. c. At least four vias with spacing ≤ S2 µm inside the same overlapped metal region (Mx AND Mx+1).

Fig. d At least nine vias with spacing ≤ S2’ µm.

Fig. e1 A single via is allowed inside metal of width ≤ W1 µm. However, it is a violation if the via is located on the boundary between metal segments of width ≤ W1 µm and width > W1 µm as shown in fig f1.

Fig. e2 A via or vias located on ≤ W1 (W2) metal but near > W1 (W2) metal can be counted in for the rule.

Fig. e3 A via or vias located on ≤ W1 (W2) metal but near > W1 (W2) metal can be counted in for the rule.

Fig. e3 Indicates the rules that the areas within the vias should follow.

Layout violation examples:

Fig. f2. Two vias with spacing > S1 µm.

Fig. f3. Two vias with spacing ≤ S1 µm but belonging to different nets.

Fig. f4. Two vias with spacing ≤ S1 µm on the same net but not inside the same overlapped metal region (Mx AND Mx+1).

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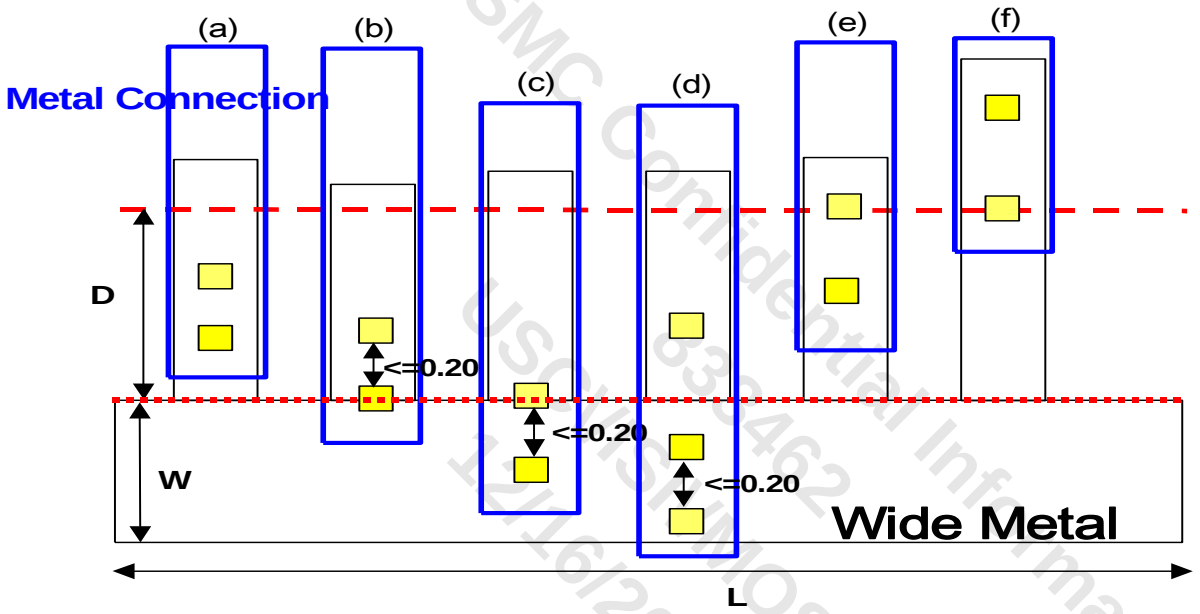
Illustration of VIAx.R.4/VIAx.R.5/VIAx.R.6 Rules

Rule No	VIAx.R.4	VIAx.R.5	VIAx.R.6
Wide Metal	Mx or Mx+1	Mx or Mx+1	Mx or Mx+1
Metal connection	Mx+1 or Mx	Mx+1 or Mx	Mx+1 or Mx
W	> 0.3 μm	> 2 μm	> 3 μm
L	> 0.3 μm	> 2 μm	> 10 μm
D	> 0.8 μm	> 2 μm	> 5 μm

(a) ~ (f) is ok but (g) ~ (j) is not allowed



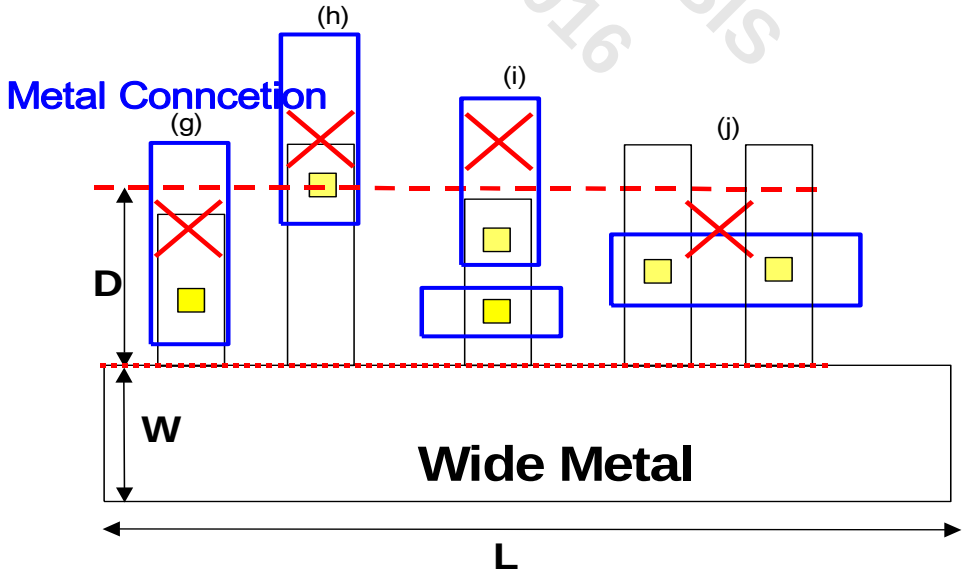


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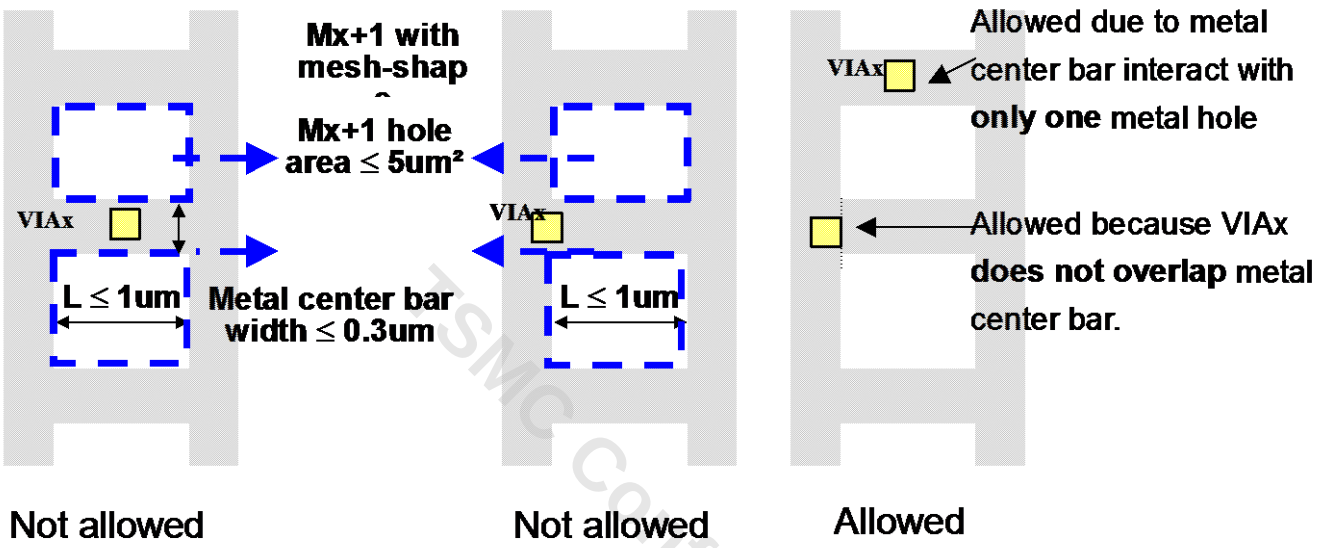
Illustration of VIAx.R.11 Rules



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4.5.29 Mx Layout Rules (Mask ID:380, 381, 384, 385, 386, 387)

For the specification of metals/vias stacking sequence and associated mask id, please refer to section 2.5.

Rule No.	Description	Label		Rule
Mx.W.1	Width	A	≥	0.10
Mx.W.2	Width of 45-degree bent Mx Please make sure the vertex of 45-degree pattern is on 5nm grid (refer to the guideline, G.6g^{U}, in section 3.7)	B	≥	0.19
Mx.W.3	Maximum width [except bond pad, if Mx is Mtop-1 layer]	C	≤	12.00
Mx.S.1	Space	D	≥	0.10
Mx.S.1®	Recommended Mx space to reduce the short possibility caused by particle	D	≥	0.13
Mx.S.2	Space [at least one metal line width > 0.20 µm (W1) and the parallel metal run length > 0.38 µm (L1)] (union projection)	E	≥	0.12
Mx.S.2.1	Space [at least one metal line width > 0.4 µm (W2) and the parallel metal run length > 0.4 µm (L2)] (union projection)	E1	≥	0.16
Mx.S.3	Space [at least one metal line width > 1.5 µm (W3) and the parallel metal run length > 1.5 µm (L3)] (union projection)	F	≥	0.50
Mx.S.4	Space [at least one metal line width > 4.5 µm (W4) and the parallel metal run length > 4.5 µm (L4)] (union projection)	G	≥	1.50
	Note: When Mx width > 9um is used, please take care of the Mx.DN.2 rule by using larger space. For example, if two Mx with width 12um and space 1.5um, it will get 94% density violation on Mx.DN.2; either enlarger the Mx space (like 2um) or reduce the Mx width (like 9um) to meet Mx.DN.2.			
Mx.S.5	Space at Mx line-end (W<Q=0.120) in a dense-line-end configuration: If Mx has parallel run length with opposite Mx (measured with T=0.035 extension) along 2 adjacent edges of Mx [any one edge <Q distance from the corner of the two edges], then one of the space (S1 or S2) needs to be at least this value (except for small jog with edge length < 0.10um (R))	S1/S2	≥	0.12
Mx.S.6	Space to 45-degree bent Mx	H	≥	0.19
Mx.S.7®	Recommended space between two non-Mx regions [one of the non-Mx area > 4,000,000µm²]. Non-Mx region is defined as {NOT (Mx OR DMx)} e.g. enlarge the metal width ≥ 0.35 for guard-ring design.	N	≥	0.35
Mx.EN.0	Enclosure of VIAx-1 is defined by either {Mx.EN.1 and Mx.EN.2} or Mx.EN.3.			
Mx.EN.0®	Recommended enclosure of VIAx-1 is defined by either Mx.EN.1® or Mx.EN.2®.			
Mx.EN.1	Enclosure of VIAx-1	I	≥	0.00
Mx.EN.1®	Recommended Mx enclosure of VIAx-1 to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	I	≥	0.04
Mx.EN.2	Enclosure of VIAx-1 [at least two opposite sides]	J	≥	0.04
Mx.EN.2®	Recommended Mx enclosure of VIAx-1 [at least two opposite sides] to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	J	≥	0.07
Mx.EN.3	Enclosure of VIAx-1 [all sides].	I	≥	0.03
Mx.A.1	Area	K	≥	0.052
Mx.A.2	Enclosed area	L	≥	0.20
	For the following Mx.DN.1/ Mx.DN.1.1, Mx.DN.2, Mx.DN.4, Mx.R.3, and DMx.R.1, please refer to the "Dummy Metal Rules" in Chapter 8 for the details.			

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Rule No.	Description	Label		Rule
Mx.DN.1	Minimum metal density in window 75 µm x 75 µm, stepping 37.5 µm		≥	10%
Mx.DN.1.1	Maximum metal density in window 100 µm x 100 µm, stepping 50 µm		≤	80%
Mx.DN.2	Maximum metal density over any 20 µm x 20 µm area (checked by stepping in 10 µm increments). The rule is applied while width of (checking window NOT Bond pad) ≥ 5 µm. Mx.DN.2 would exclude the following regions: 1. Both wire bond pad and flip chip bump pad 2. Mz in {INDDMY SIZING 18 µm} 3. LMARK		≤	90%
Mx.DN.4	The metal density difference between any two 250 µm x 250 µm neighboring checking windows including DMxEXCL (stepping in 250 µm increments) Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient.)		≤	40%
Mx.DN.5	It is not allowed to have local density > 80% of all 3 consecutive metal (Mx, Mx+1 and Mx+2) over any 50um x 50um (stepping 25), i.e. it is allowed for either one of Mx, Mx+1, or Mx+2 to have a local density ≤ 80%. 1. The metal layers include M1/Mx and dummy metals. 2. The check does not include chip corner stress relief pattern,seal ring and top2 metals at CUP area.			
DMx.R.1	DMx is a must. The DMx CAD layer (TSMC default, 32;1 for DM2) must be different from the Mx CAD layer.			
Mx.R.1^{U}	Mx line-end must be rectangular. Other shapes are not allowed.			
Mx.R.2g^{U}	For the small space, recommended to enlarge the metal space by using Wire Spreading function of EDA tool to reduce the wire capacitance and the possibility of metal short. Please refer to section 9.1.1 and TSMC Reference Flow.			

Table Notes:

- To improve the metal CMP process window, you must fill the DMx globally and uniformly even if the originally drawn Mx has already met the density rule (Mx.DN.1/ Mx.DN.1.1/Mx.DN.2). For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, it is recommended filling dummy pattern evenly by manual operations to gain a better process window and electrical performance.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations (Mx.DN.1/ Mx.DN.1.1, Mx.DN.2, Mx.DN.5) during placement. It may have unexpected violation during the IP/macro placement due to the environment, even if the IP/macro already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.

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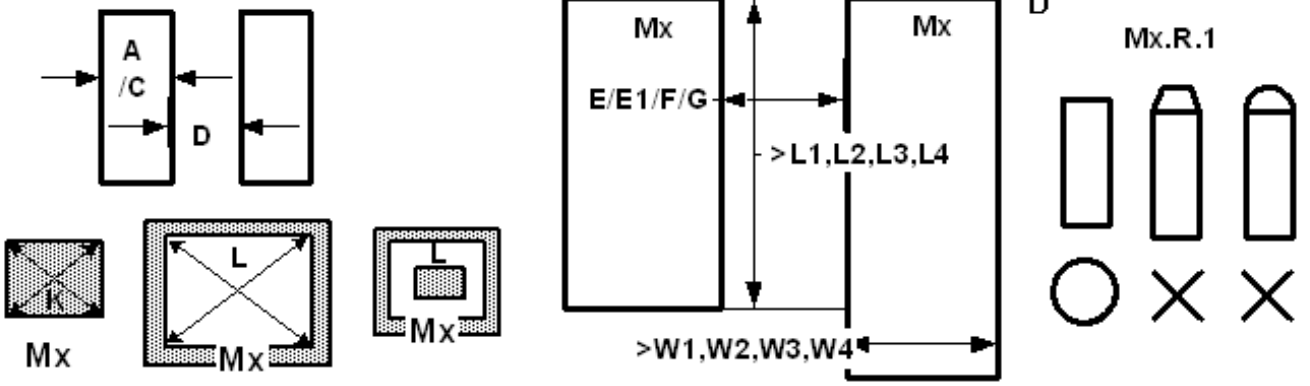
Mx



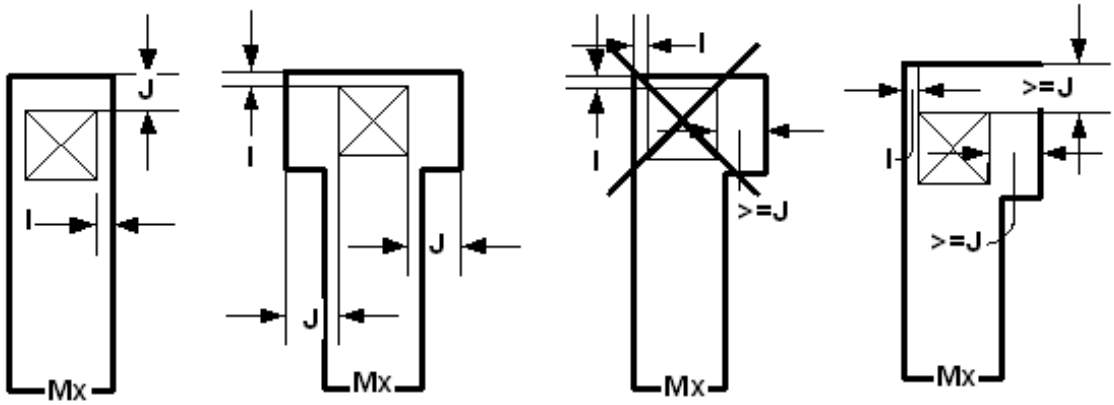
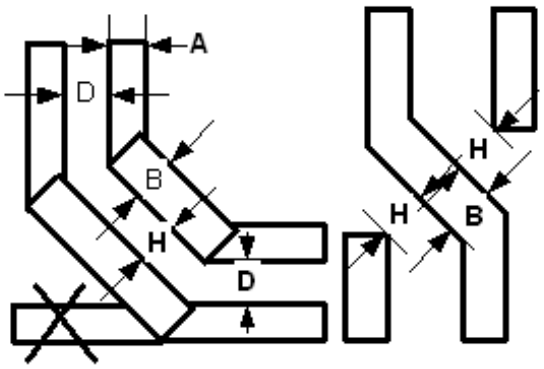
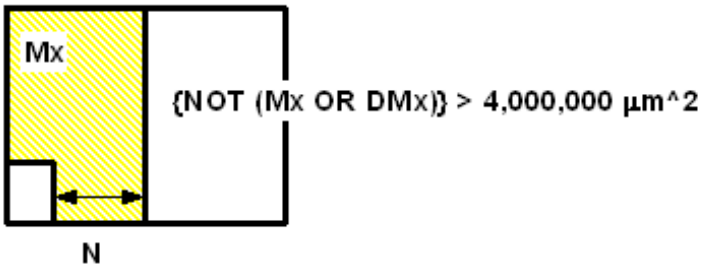


Fig. a Fig. b





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Mx.S.5

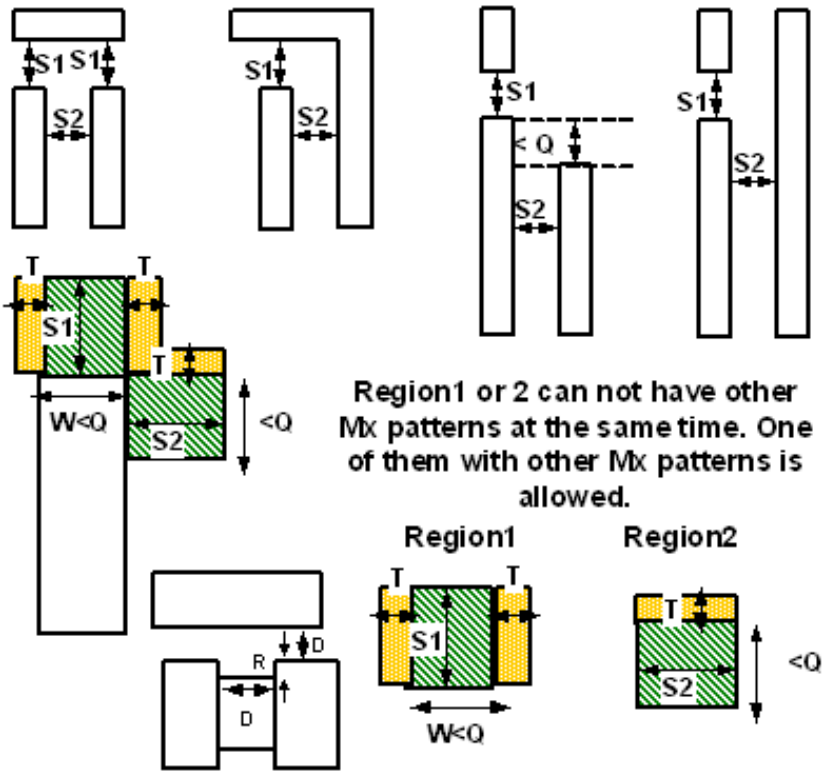
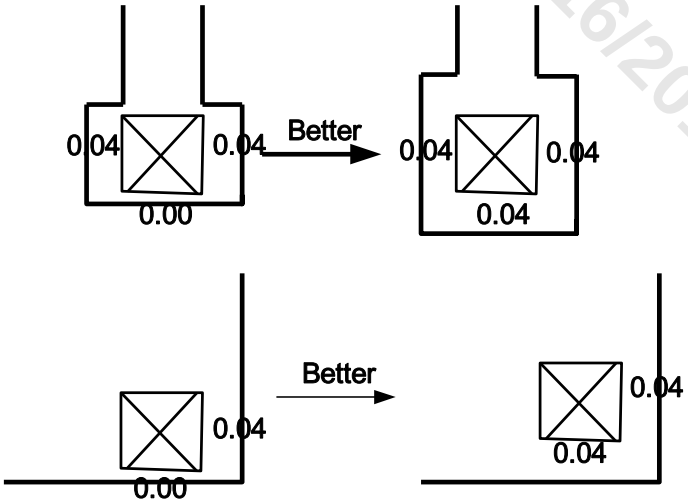


Illustration of Mx.EN.1®



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4.5.30 VIAy Layout Rules (Mask ID: 379, 373, 374, 375, 376, 377, 372)

For a specification of the stacking sequence of metals and vias see section 2.5.

Table 2.5.3 is for second inter-layer via.

Table 2.5.4 is for 2X top via.

Rule No.	Description	Label		Rule
VIAy.W.1	Width (maximum = minimum except for seal-ring and fuse protection ring)	A	=	0.20
VIAy.W.2	Width of VIAy bar. VIAy bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover VIAy bar if VIAy bar is used.		=	0.20
VIAy.S.1	Space	B	≥	0.20
VIAy.S.2	Space to 3-neighboring VIAy (< 0.28 µm distance)	C	≥	0.25
VIAy.EN.0®	Recommended enclosure by Mx or My is defined by either VIAy.EN.1® or VIAy.EN.2®.			
VIAy.EN.1	Enclosure by Mx or My	D	≥	0.00
VIAy.EN.1®	Recommended enclosure by Mx or My to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	D	≥	0.05
VIAy.EN.2	Enclosure by Mx or My [at least two opposite sides]	E	≥	0.05
VIAy.EN.2®	Recommended enclosure by Mx or My [at least two opposite sides] to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	E	≥	0.08
VIAy.R.1	45-degree rotated VIAy is not allowed.			
VIAy.R.2	At least two VIAy with space ≤ 0.40 µm (S1), or at least four VIAy with space ≤ 0.50 µm (S1’) are required to connect My and My+1 when one of these two metals has width and length (W1) > 0.60 µm.			
VIAy.R.3	At least four VIAy with space ≤ 0.40 µm (S2) are required to connect My and My+1 when one of these two metals has width and length (W2) > 1.40 µm.			
VIAy.R.4	At least two VIAy must be used for a connection that is ≤ 1.6 µm (D) away from a metal plate (either My or My+1) with length > 0.6 µm (L) and width > 0.6 µm (W). (It is allowed to use one VIAy for a connection that is > 1.6 µm (D) away from a metal plate (either My or My+1) with length > 0.6 µm (L) and width > 0.6 µm (W).)			
VIAy.R.5	At least two VIAy must be used for a connection that is ≤ 2 µm (D) away from a metal plate (either My or My+1) with length > 2 µm (L) and width > 2 µm (W). (It is allowed to use one VIAy for a connection that is > 2 µm (D) away from a metal plate (either My or My+1) with length > 2 µm (L) and width > 2 µm (W).)			
VIAy.R.6	At least two VIAy must be used for a connection that is ≤ 5 µm (D) away from a metal plate (either My or My+1) with length > 10 µm (L) and width > 3 µm (W). (It is allowed to use one VIAy for a connection that is > 5 µm (D) away from a metal plate (either My or My+1) with length > 10 µm (L) and width > 3 µm (W)).			
VIAy.R.7	VIAy must be fully covered by {Mx AND My+1} or {My AND My+1}.			
VIAy.R.9g	Recommend using redundant vias to avoid high Rc wherever layout allows. Please refer to the “Via Layout Recommendations” in the section 4.5.37. DRC can flag single via.			

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VIAy

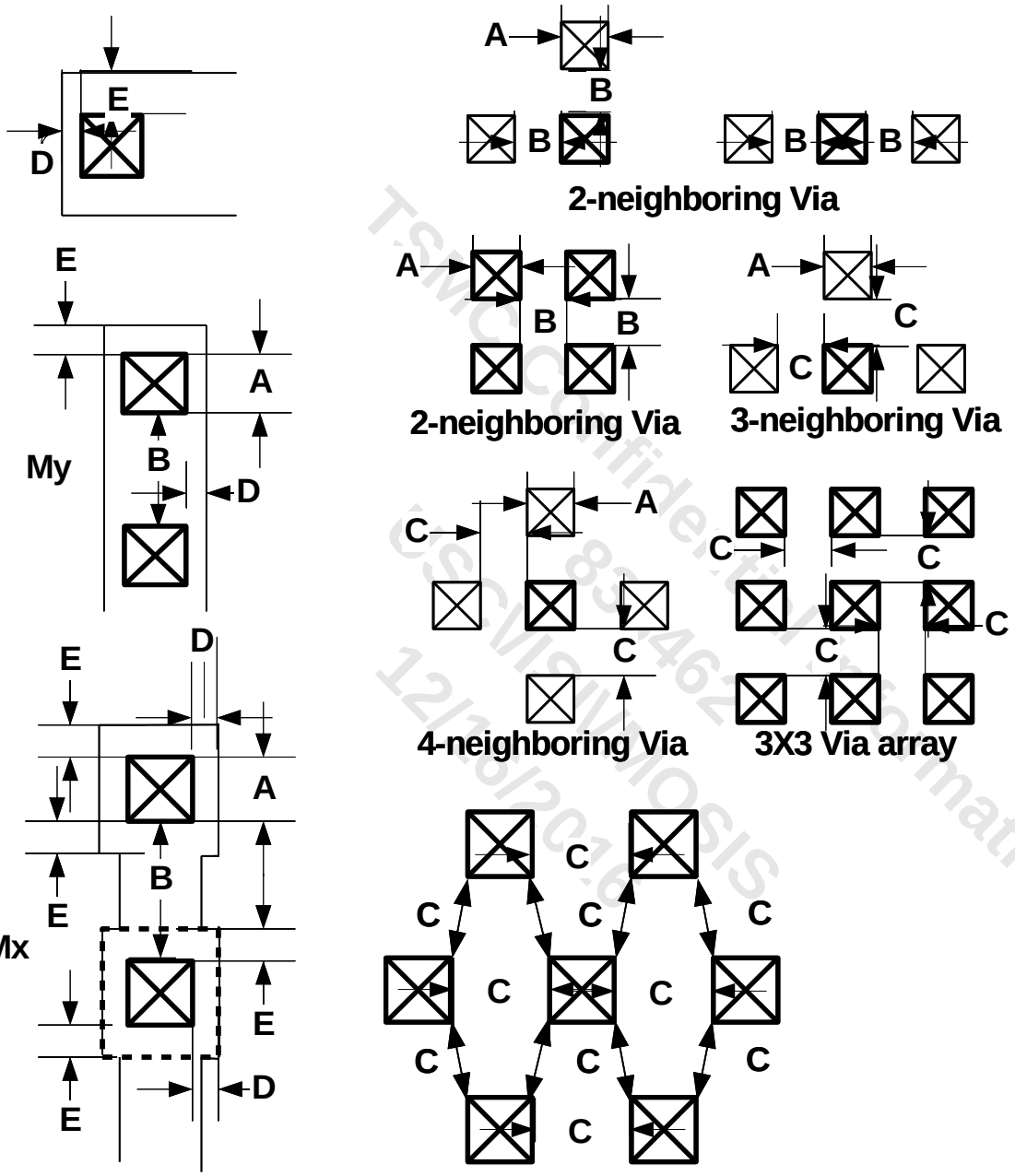

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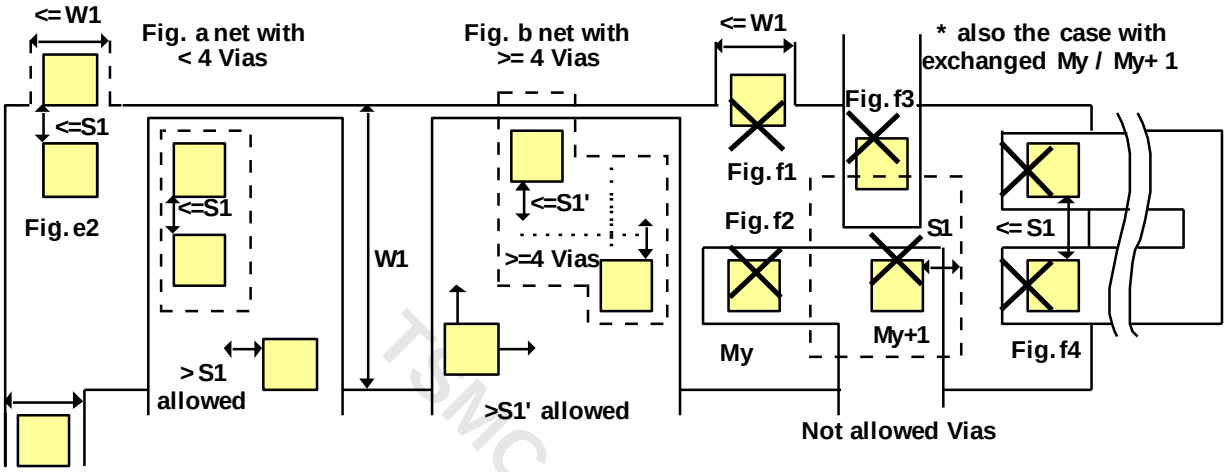
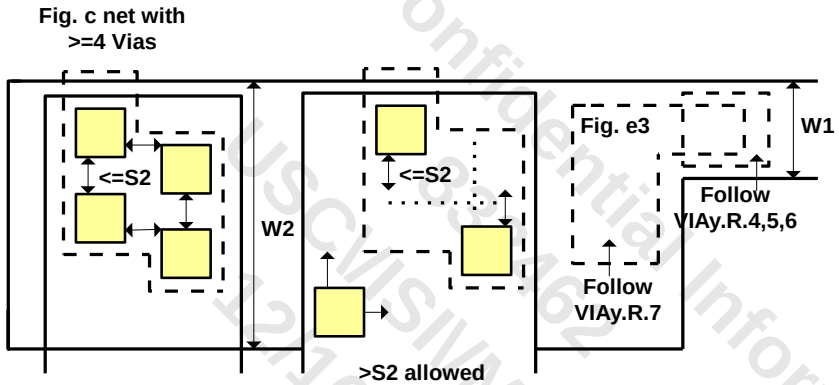
Illustration of VIAy.R.2, VIAy.R.3 Rules





Rule VIAy.R.2 0.60 µm < W1 ≤ 1.4 µm		Rule VIAy.R.3 W2 µm > 1.4 µm
Fig. a < 4 vias	Fig. b ≥ 4 vias	Fig. c ≥ 4 vias
S1 = 0.40 µm	S1' = 0.50 µm	S2 = 0.40 µm

Fig a. At least two vias with spacing ≤ S1 µm inside the same overlapped metal region (My AND My+1).

Fig. b At least four vias with spacing ≤ S1' µm.

Fig. c. At least four vias with spacing ≤ S2 µm inside the same overlapped metal region (My AND My+1).

Fig. d At least nine vias with spacing ≤ S2' µm.

Fig. e1 A single via is allowed inside metal of width ≤ W1 µm. However, it is a violation if the via is located on the boundary between metal segments of width ≤ W1 µm and width > W1 µm as shown in fig f1.

Fig. e2 A via or vias located on ≤ W1 (W2) metal but near > W1 (W2) metal can be counted in for the rule.

Fig. e3 A via or vias located on ≤ W1 (W2) metal but near > W1 (W2) metal can be counted in for the rule.

Fig. e3 Indicates the rules that the areas within the vias should follow.

Layout violation examples:

Fig. f2. Two vias with spacing > S1 µm.

Fig. f3. Two vias with spacing ≤ S1 µm but belonging to different nets.

Fig. f4. Two vias with spacing ≤ S1 µm on the same net but not inside the same overlapped metal region (My AND My+1).

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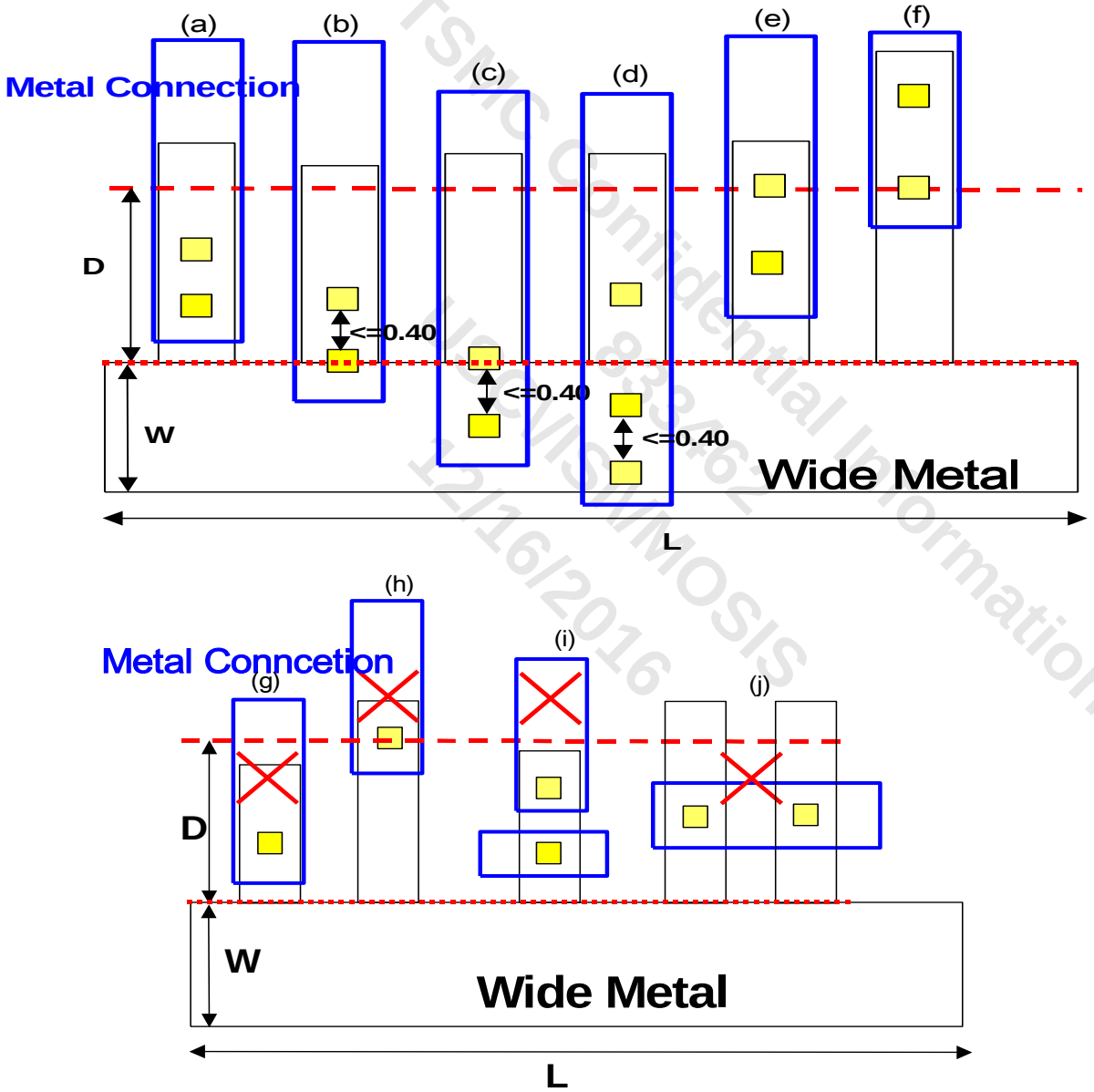
Illustration of VIAy.R.4/VIAy.R.5/VIAy.R.6 Rules

Rule No	VIAy.R.4	VIAy.R.5	VIAy.R.6
Wide Metal	My or My+1	My or My+1	My or My+1
Metal connection	My+1 or My	My+1 or My	My+1 or My
W	> 0.6 µm	> 2 µm	> 3 µm
L	> 0.6 µm	> 2 µm	> 10 µm
D	> 1.6 µm	> 2 µm	> 5 µm

(a) ~ (f) is ok but (g) ~ (j) is not allowed



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4.5.31 My Layout Rules (Mask ID: 381, 384, 385, 386, 387, 388, 389)

For the specification of metals/vias stacking sequence and associated mask id, please refer to section 2.5.
Table 2.5.3 is for second inter-layer metal.
Table 2.5.4 is for 2X top metal.

Rule No.	Description	Label		Rule
My.W.1	Width	A	≥	0.20
My.W.2	Width of 45-degree bent My. Please make sure the vertex of 45-degree pattern is on 5nm grid (refer to the guideline, G.6g^{U}, in section 3.7)	B	≥	0.39
My.W.3	Maximum width	C	≤	12.00
My.S.1	Space	D	≥	0.20
My.S.2	Space [at least one metal line width > 0.39 µm (W1) and the parallel metal run length > 1.0 µm (L1)] (union projection)	E	≥	0.24
My.S.3	Space [at least one metal line width > 1.5 µm (W2) and the parallel metal run length > 1.5 µm (L2)] (union projection)	F	≥	0.50
My.S.4	Space [at least one metal line width > 4.5 µm (W3) and the parallel metal run length > 4.5 µm (L3)] (union projection)	G	≥	1.50
	Note: When My width > 9um is used, please take care of the My.DN.2 rule by using larger space. For example, if two My with width 12um and space 1.5um, it will get 94% density violation on My.DN.2; either enlarger the My space (like 2um) or reduce the My width (like 9um) to meet My.DN.2.			
My.S.5	Space to 45-degree bent My	H	≥	0.39
My.S.6®	Recommended space between two non-My regions [one of the non-My area > 4,000,000µm²]. Non-My region is defined as {NOT (My OR DMy)}. e.g. enlarge the metal width ≥ 0.35 for the guard-ring design.	M	≥	0.35
My.EN.0®	Recommended enclosure of VIAy-1 is defined by either My.EN.1® or My.EN.2®.			
My.EN.1	Enclosure of VIAy-1	I	≥	0.00
My.EN.1®	Recommended enclosure of VIAy-1 to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	I	≥	0.05
My.EN.2	Enclosure of VIAy-1 [at least two opposite sides]	J	≥	0.05
My.EN.2®	Recommended enclosure of VIAy-1 [at least two opposite sides] to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	J	≥	0.08
My.A.1	Area	K	≥	0.144
My.A.2	Enclosed area	L	≥	0.265
	For the following My.DN.1, My.DN.1.1, My.DN.2, My.DN.3, My.DN.4, and DMy.R.1, please refer to the "Dummy Metal Rules" in Chapter 8 for the details.			
My.DN.1	Minimum metal density in window 75 µm x 75 µm, stepping 37.5 µm		≥	10%
My.DN.1.1	Maximum metal density in window 100 µm x 100 µm, stepping 50 µm		≤	80%
My.DN.2	Maximum metal density over any 20 µm x 20 µm area (checked by stepping in 10 µm increments).		≤	90%
My.DN.4	The metal density difference between any two 250 µm x 250 µm neighboring checking windows (stepping in 250 µm increments) Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient).		≤	40%

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Rule No.	Description	Label		Rule
DMy.R.1	DMy is a must. The DMy CAD layer (TSMC default, 36;21 for DM6) must be different from the My CAD layer.			
My.R.1[U]	My line-end must be rectangular. Other shapes are not allowed.			
My.R.2g[U]	For the small space, recommended to enlarge the metal space, by using Wire Spreading function of EDA tool, to reduce the wire capacitance. Please refer to section 9.1.1 and TSMC Reference Flow.			

Table Notes:

- To improve the metal CMP process window, you must fill the DMy globally and uniformly even if the originally drawn My has already met the density rule (My.DN.1/ My.DN.1.1/My.DN.2). For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, it is recommended filling dummy pattern evenly by manual operations to gain a better process window and electrical performance.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations (My.DN.1/ My.DN.1.1/My.DN.2) during placement. It may have unexpected violation during the IP/macro placement due to the environment, even if the IP/macro already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.

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My

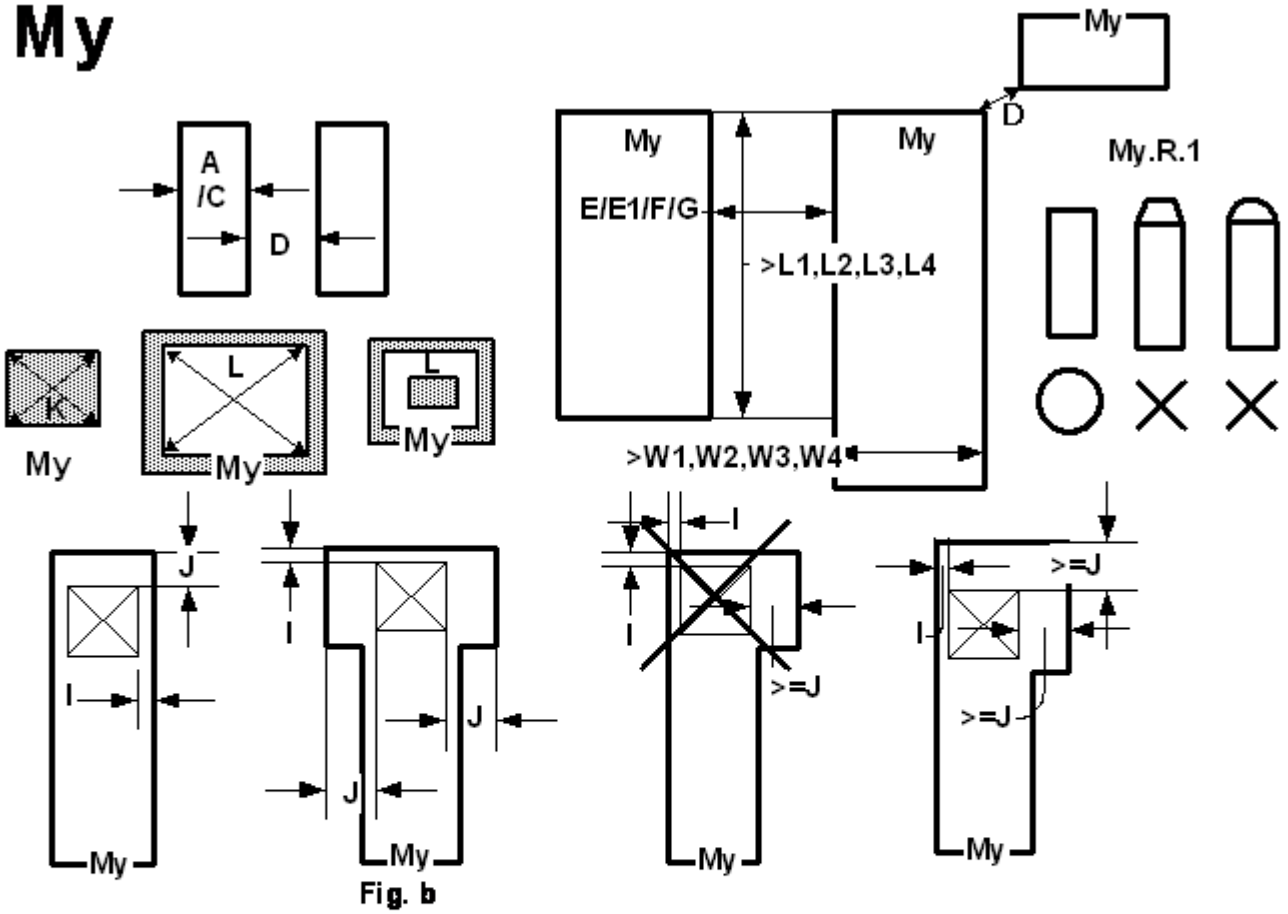

Fig. b

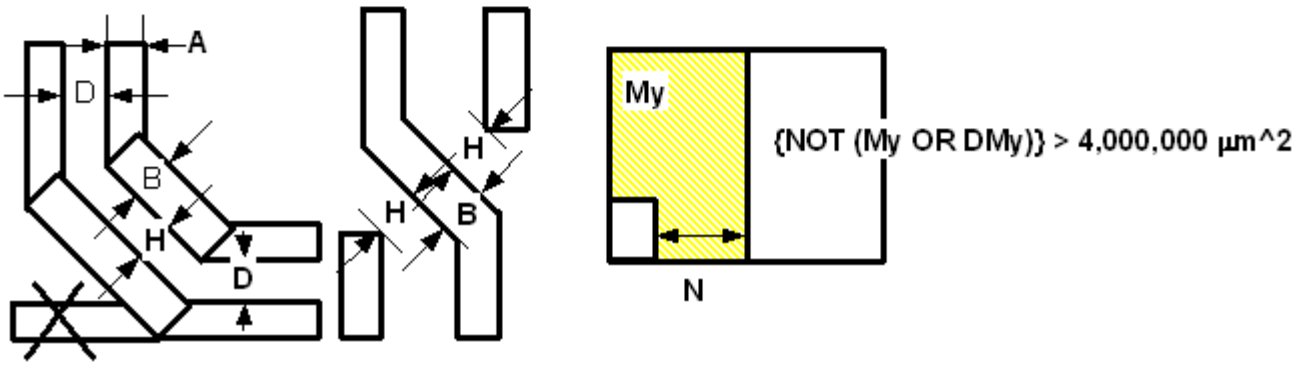

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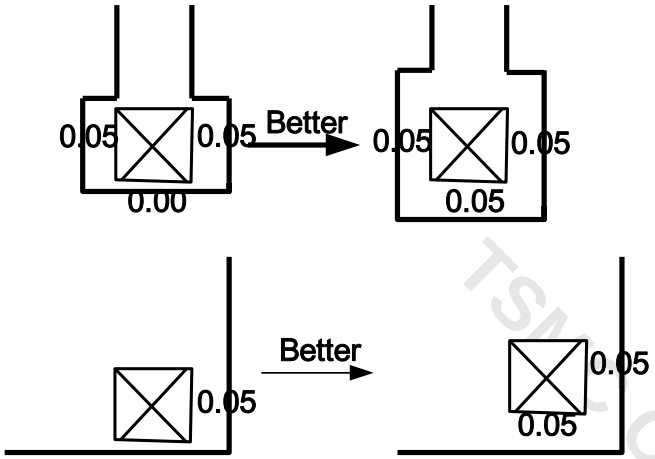
Illustration of My.EN.1®



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4.5.32 Top VIAz Layout Rules (Mask ID: 379, 373, 374, 375, 376, 377, 372)

For the specification of metals/vias stacking sequence and associated mask id, please refer to section 2.5.

Rule No.	Description	Label		Rule
VIAz.W.1	Width (maximum = minimum except for seal-ring and fuse protection ring)	A	=	0.36
VIAz.W.2	Width of VIAz bar. VIAz bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover VIAz bar if VIAz bar is used.		=	0.36
VIAz.S.1	Space	B	≥	0.34
VIAz.S.2	Space to 3-neighboring VIAz (<0.56 µm distance)	C	≥	0.54
VIAz.EN.1	Enclosure by Mx or My or Mz	D	≥	0.02
VIAz.EN.2	Enclosure by Mx or My or Mz [at least two opposite sides]	E	≥	0.08
VIAz.R.1	45-degree rotated VIAz is not allowed.			
VIAz.R.2	At least two VIAz with spacing ≤ 1.7 µm are required to connect Mz and Mz+1 when one of these metals has a width and length > 1.8 µm.			
VIAz.R.3	At least two VIAz must be used for a connection that is ≤ 5 µm (D) away from a metal plate (either Mz or Mz+1) with length > 10 µm (L) and width > 3 µm (W). (It is allowed to use one VIAz for a connection that is > 5 µm (D) away from a metal plate (either Mz or Mz+1) with length > 10 µm (L) and width > 3 µm (W)).			
VIAz.R.4	VIAz must be fully covered by Mz and Mz+1.			
VIAz.R.5g	Recommend using redundant vias to avoid high Rc wherever layout allows. DRC can flag single via.			

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VIAz

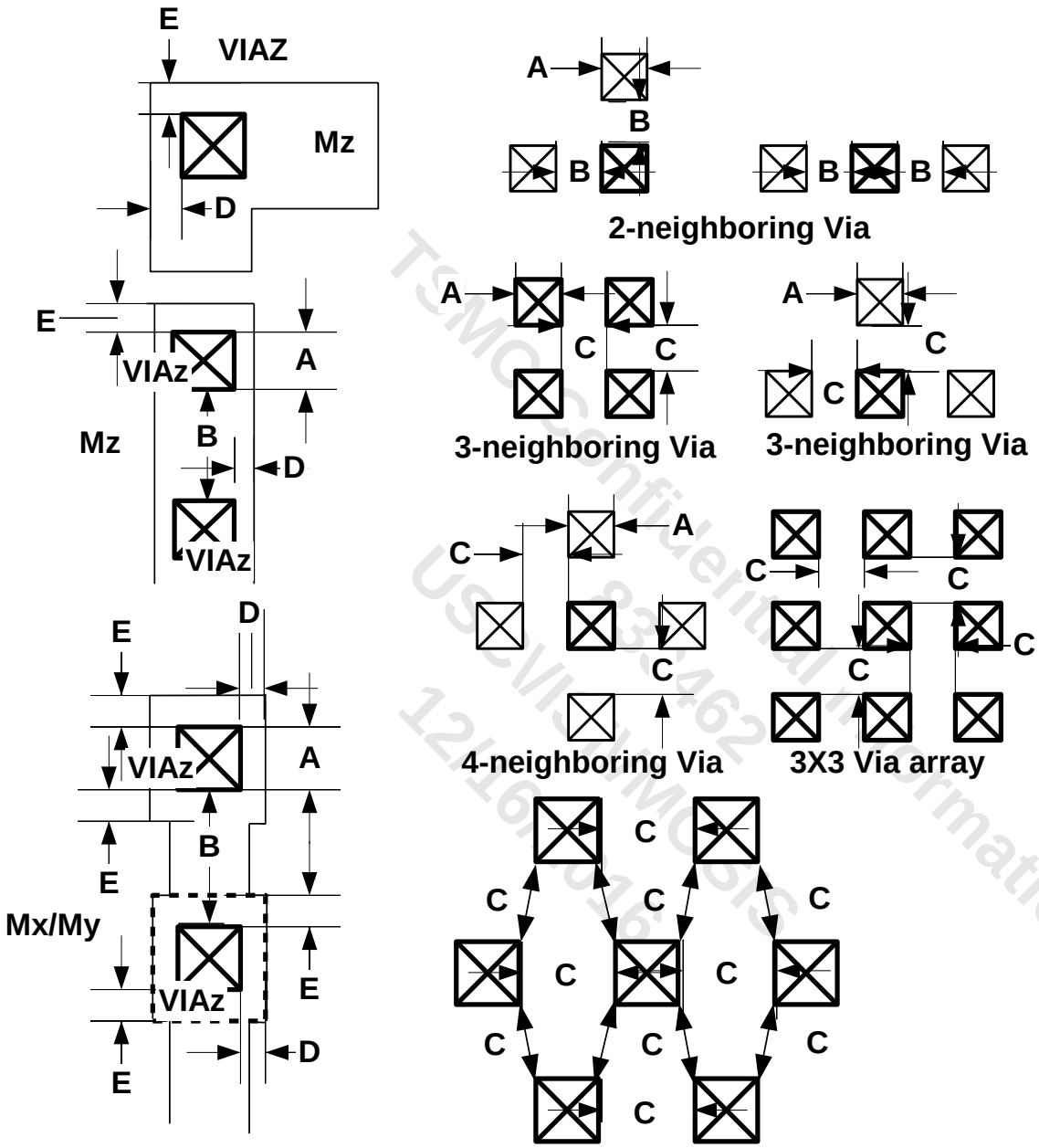

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Illustration of VIAz.R.2 Rule

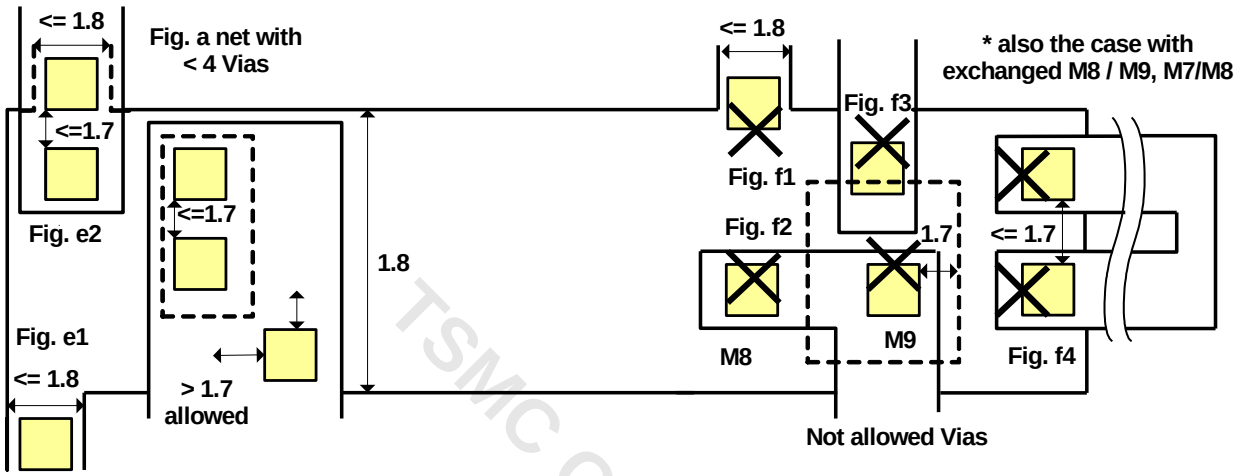

Fig. a At least two vias with spacing ≤ 1.7 µm inside the same overlapped metal region (M7 AND M8) or (M8 AND M9).

Fig. e1 A single via is allowed inside metal of width ≤ 1.8 µm. However, it is a violation if the via is located on the boundary between a metal segment of width ≤ 1.8 µm and a segment of width > 1.8 µm as in Fig. f1.

Fig. e2 A via or vias that are located on ≤ 1.8 metal but near >1.8 metal can be counted in for the rule.

Violated layout examples:

Fig. f2 Two vias with spacing > 1.7 µm.

Fig. f3 Two vias with spacing ≤ 1.7 µm but belonging to different nets.

Fig. f4 Two vias with spacing ≤ 1.7 µm on the same net but not inside the same overlapped metal region (M7 AND M8) or (M8 AND M9).

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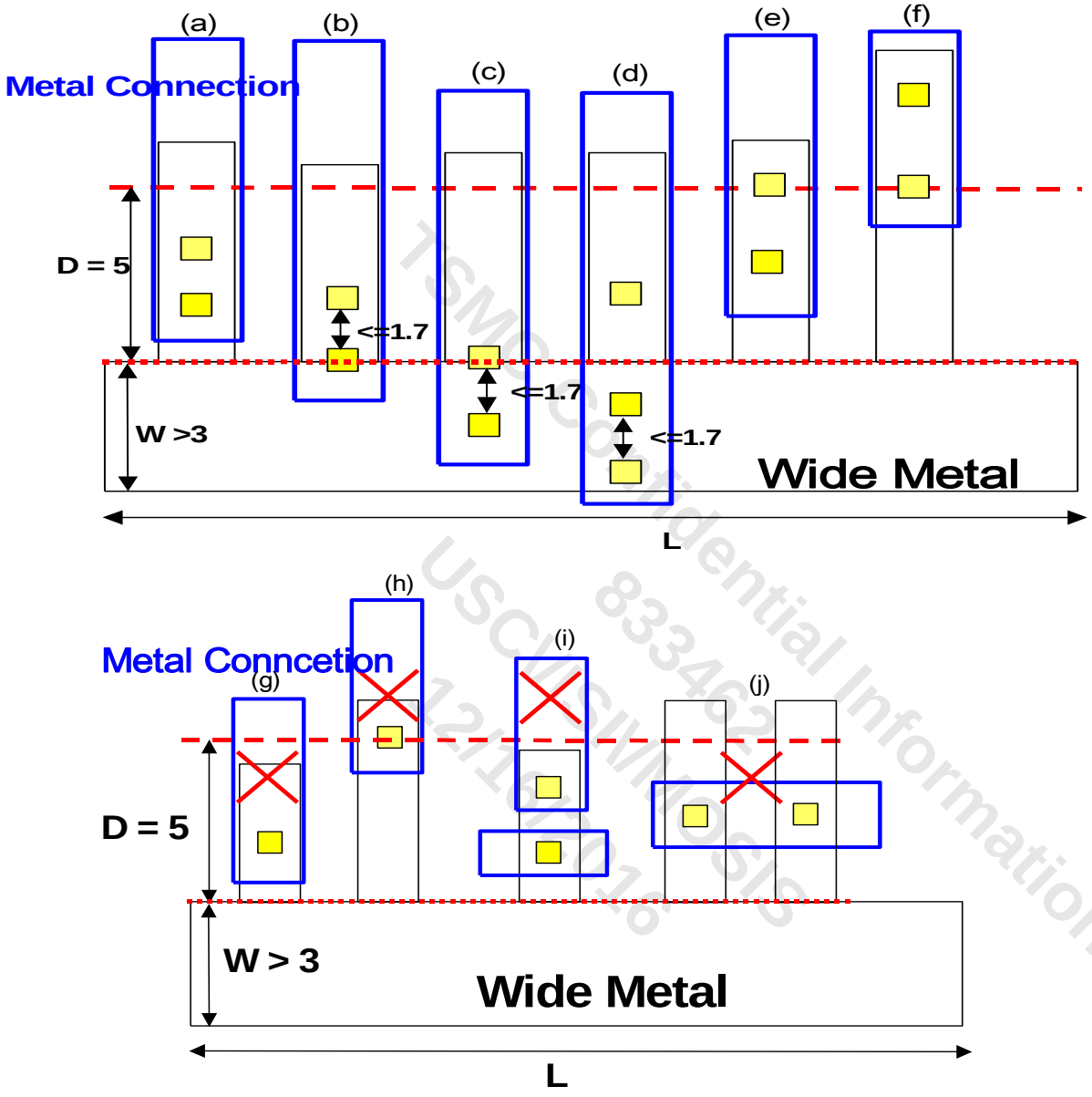
Illustration of VIAz.R.3 Rule

(a) ~ (f) is ok but (g) ~ (j) is not allowed



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4.5.33 Top Mz Layout Rules (Mask ID: 381, 384, 385, 386, 387, 388, 389)

For the specification of metals/vias stacking sequence and associated mask id, please refer to section 2.5.

Rule No.	Description	Label		Rule
Mz.W.1	Width	A	≥	0.40
Mz.W.2	Maximum width [except bond pad]	B	≤	12.00
Mz.S.1	Space	C	≥	0.40
Mz.S.2	Space [at least one metal line width > 1.5 µm (W1) and the parallel metal run length > 1.5 µm (L1)]	D	≥	0.50
Mz.S.3	Space [at least one metal line width > 4.5 µm (W2) and the parallel metal run length > 4.5 µm (L2)]	E	≥	1.50
	Note: When Mz width > 9um is used, please take care of the Mz.DN.2 rule by using larger space. For example, if two Mz with width 12um and space 1.5um, it will get 94% density violation on Mz.DN.2; either enlarger the Mz space (like 2um) or reduce the Mz width (like 9um) to meet Mz.DN.2.			
Mz.EN.1	Enclosure of VIAz-1	F	≥	0.02
Mz.EN.2	Enclosure of VIAz-1 [at least two opposite sides]	G	≥	0.08
Mz.A.1	Area	H	≥	0.565
Mz.A.2	Enclosed area	I	≥	0.565
	For the following Mz.DN.1, Mz.DN.1.1, Mz.DN.2, Mz.DN.3, Mz.DN.4, and DMz.R.1, please refer to the "Dummy Metal Rules" in Chapter 8 for the details.			
Mz.DN.1	Minimum metal density in window 75 µm x 75 µm, stepping 37.5 µm. Both wire bond pad and flip chup bump are excluded from 80% density check.		≥	10%
Mz.DN.1.1	Maximum metal density in window 100 µm x 100 µm, stepping 50 µm. Both wire bond pad and flip chup bump are excluded from 80% density check.		≤	80%
Mz.DN.2	Maximum metal density over any 20um x 20um area (checked by stepping in 10um increments). Both wire bond pad and flip chup bump are excluded from 90% density check.		≤	90%
Mz.DN.4	The metal density difference between any two 250 µm x 250 µm neighboring checking windows including DMxEXCL (stepping in 250 µm increments) Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient).		≤	40%
DMz.R.1	DMz is a must. The DMz CAD layer (TSMC default, 38;41 for DM8) must be different from the Mz CAD layer.			
Mz.R.1^{U}	Mz line-end must be rectangular. Other shapes are not allowed.			

Table Notes:

- For RF/Mixed-signal applications, some metal rules are different from Logic rules. Please refer to RF/Mixed-signal design rules for details.
- To improve the metal CMP process window, you must fill the DMz globally and uniformly even if the originally drawn Mn has already met the density rule (Mz.DN.1/Mz.DN.2). For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, it is recommended filling dummy pattern evenly by manual operations to gain a better process window and electrical performance.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations (Mz.DN.1, Mz.DN.2) during placement. It may have unexpected violation during the IP/macro placement due to the environment, even if the IP/macro already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.

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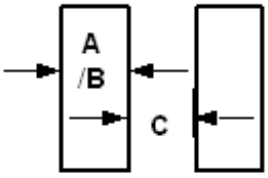
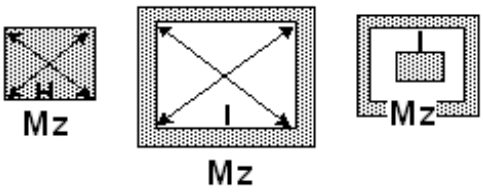
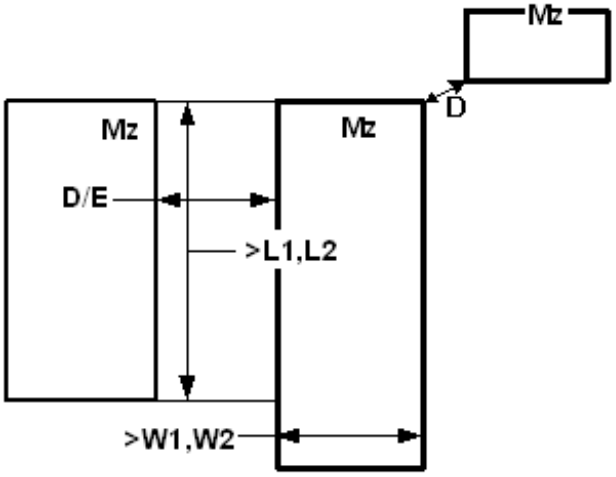
Mz







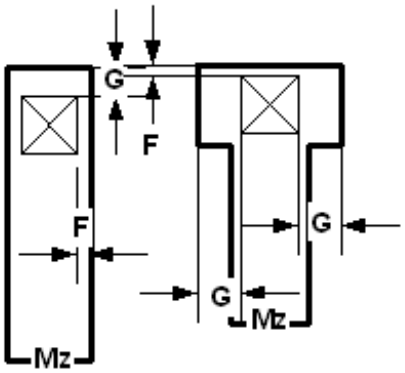
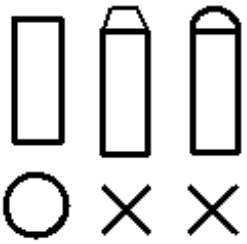


Fig. a

Fig. b

Mz.R.1



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4.5.34 Top VIAr Layout Rules (Mask ID: 375, 356, 377, 372)

For the specification of metals/vias stacking sequence and associated mask id, please refer to section 2.5.

Rule No.	Description	Label		Rule
VIAr.0[U]	VIAr is only allowed to start from VIA5 and the maximum layer count is two.			
VIAr.W.1	Width (square)(maximum = minimum)	A	=	0.46
VIAr.W.2	Width of VIAr bar. VIAr bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover VIAr bar if VIAr bar is used.		=	0.29
VIAr.S.1	Space	B	≥	0.44
VIAr.S.2	Space to 3-neighboring VIAr (≤0.66 µm distance)	C	≥	0.66
	[Space of 2*2 array on same net]	C1	≥	0.54
VIAr.EN.1	Enclosure by Mx or Mr	D	≥	0.02
VIAr.EN.2	Enclosure by Mx or Mr [at least two opposite sides]	E	≥	0.08
VIAr.R.1	45-degree rotated VIAr is not allowed.			
VIAr.R.2	At least two VIAr with spacing ≤ 1.7 µm are required to connect Mr and Mr+1 when one of these metals has a width and length > 1.8 µm.			
VIAr.R.3	At least two VIAr must be used for a connection that is ≤ 5 µm (D) away from a metal plate (either Mr or Mr+1) with length > 10 µm (L) and width > 3 µm (W). (It is allowed to use one VIAr for a connection that is > 5 µm (D) away from a metal plate (either Mr or Mr+1) with length > 10 µm (L) and width > 3 µm (W)).			
VIAr.R.4	VIAr must be fully covered by Mx and Mr.			
VIAr.R.5g	Recommend using redundant vias to avoid high Rc wherever layout allows. DRC can flag single via.			

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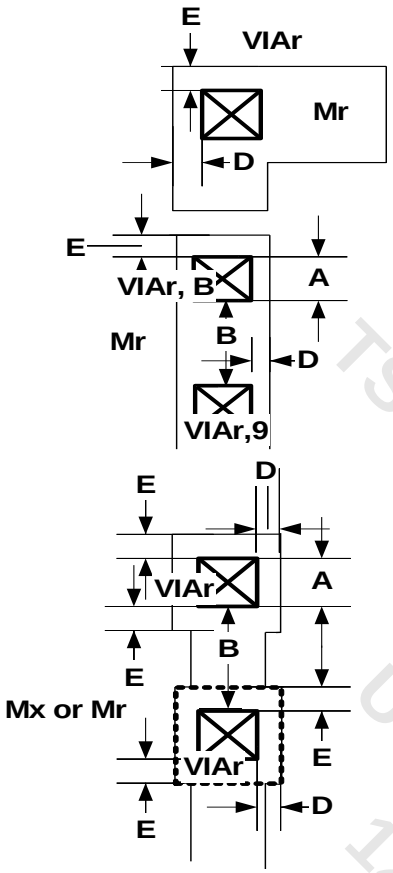

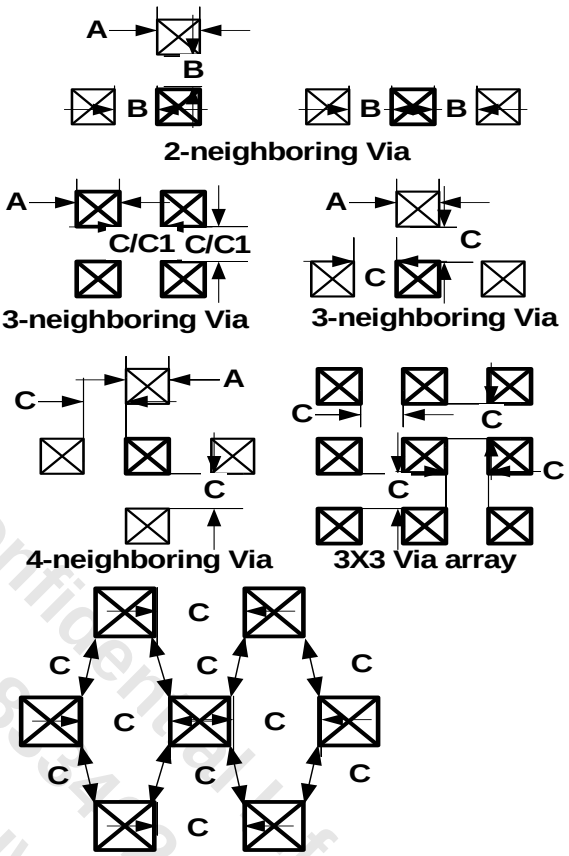

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Illustration of VIAr.R.2 Rule

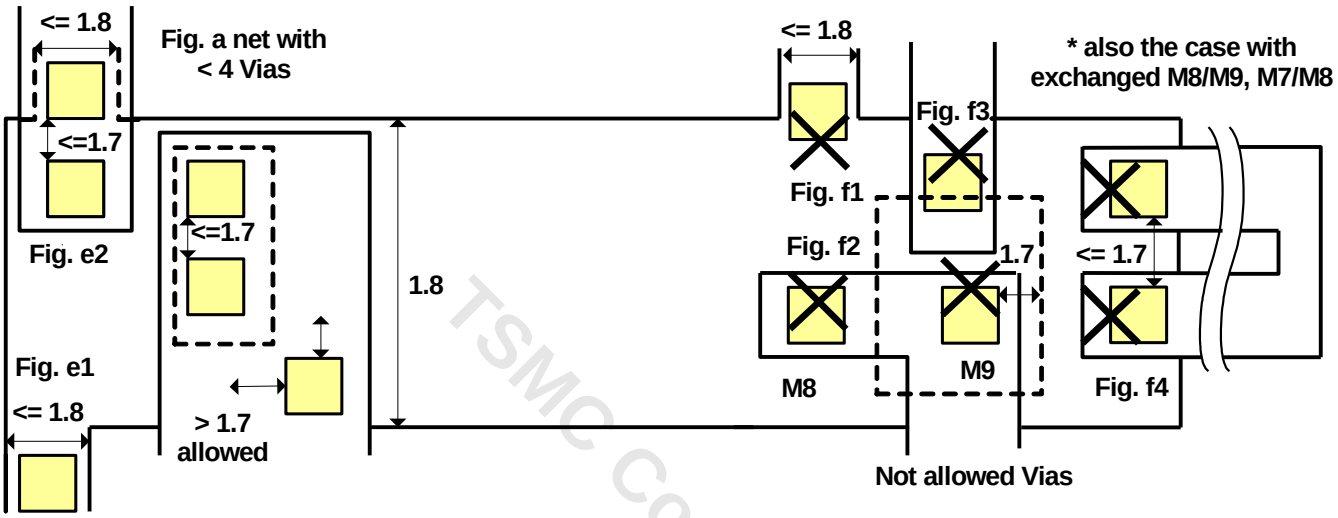

Fig. a At least two vias with spacing ≤ 1.7 µm inside the same overlapped metal region (M7 AND M8) or (M8 AND M9).

Fig. e1 A single via is allowed inside metal of width ≤ 1.8 µm. However, it is a violation if the via is located on the boundary between a metal segment of width ≤ 1.8 µm and a segment of width > 1.8 µm as in Fig. f1.

Fig. e2 A via or vias that are located on ≤ 1.8 metal but near >1.8 metal can be counted in for the rule.

Violated layout examples:

Fig. f2 Two vias with spacing > 1.7 µm.

Fig. f3/f4 Two vias with spacing ≤ 1.7 µm on the same net but not inside the same overlapped metal region (M7 AND M8) or (M8 AND M9).

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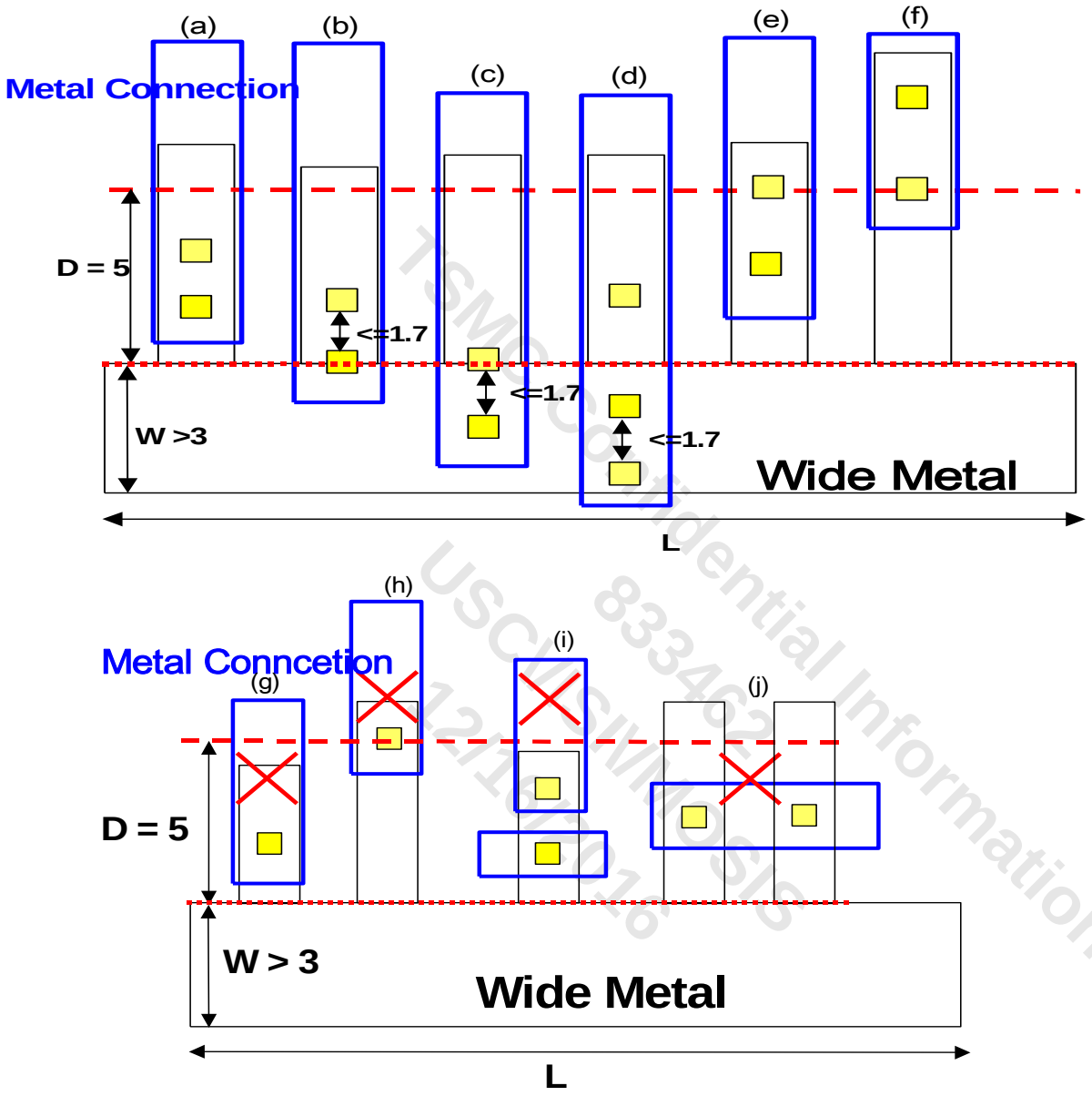
Illustration of VIAr.R.3 Rule

(a) ~ (f) is ok but (g) ~ (j) is not allowed



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4.5.35 Top Mr Layout Rules (Mask ID:386, 387, 388, 389)

For the specification of metals/vias stacking sequence and associated mask id, please refer to section 2.5.

Rule No.	Description	Label		Rule
Mr.0[U]	Mr is only allowed to start from M6 and the maximum layer count is two.			
Mr.W.1	Width	A	≥	0.50
Mr.W.2	Maximum width [except bond pad]	B	≤	12.00
Mr.S.1	Space	C	≥	0.50
Mr.S.2	Space [at least one metal line width > 1.5 µm (W1) and the parallel metal run length > 1.5 µm (L1)]	D	≥	0.65
Mr.S.3	Space [at least one metal line width > 4.5 µm (W2) and the parallel metal run length > 4.5 µm (L2)]	E	≥	1.50
	Note: When Mr width > 9um is used, please take care of the Mr.DN.2 rule by using larger space. For example, if two Mr with width 12um and space 1.5um, it will get 94% density violation on Mr.DN.2; either enlarger the Mr space (like 2um) or reduce the Mr width (like 9um) to meet Mr.DN.2.			
Mr.EN.1	Enclosure of VIAr-1	F	≥	0.02
Mr.EN.2	Enclosure of VIAr-1 [at least two opposite sides]	G	≥	0.08
Mr.A.1	Area	H	≥	1.0
Mr.A.2	Enclosed area	I	≥	1.0
	For the following Mr.DN.1, Mr.DN.1.1, Mr.DN.2, Mr.DN.3, Mr.DN.4, and DMr.R.1, please refer to the "Dummy Metal Rules" in Chapter 8 for the details.			
Mr.DN.1	Minimum metal density in window 75 µm x 75 µm, stepping 37.5 µm. Both wire bond pad and flip chup bump are excluded from 80% density check.		≥	10%
Mr.DN.1.1	Maximum metal density in window 100 µm x 100 µm, stepping 50 µm. Both wire bond pad and flip chup bump are excluded from 80% density check.		≤	80%
Mr.DN.2	Maximum metal density over any 20um x 20um area (checked by stepping in 10um increments). Both wire bond pad and flip chip bump pad are excluded from 90% density check.		≤	90%
Mr.DN.4	The metal density difference between any two 250 µm x 250 µm neighboring checking windows including DMrEXCL (stepping in 250 µm increments) Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient).		≤	40%
Mr.R.1[U]	Mr line-end must be rectangular. Other shapes are not allowed.			
DMr.R.1	DMr is a must. The DMr CAD layer (TSMC default, 38;81 for DM8) must be different from the Mr CAD layer.			

Table Notes:

- To improve the metal CMP process window, you must fill the DMr globally and uniformly even if the originally drawn Mr has already met the density rule (Mr.DN.1/Mr.DN.2). For sensitive areas with auto-fill operations blocked by the DMrEXCL layer, it is recommended filling dummy pattern evenly by manual operations to gain a better process window and electrical performance.
- During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations (Mr.DN.1, Mr.DN.2) during placement. It may have unexpected violation during the IP/macro placement due to the environment, even if the IP/macro already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.

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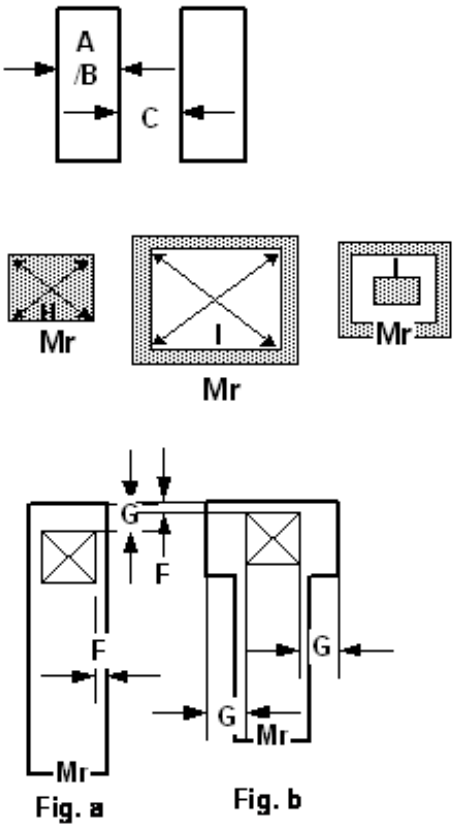
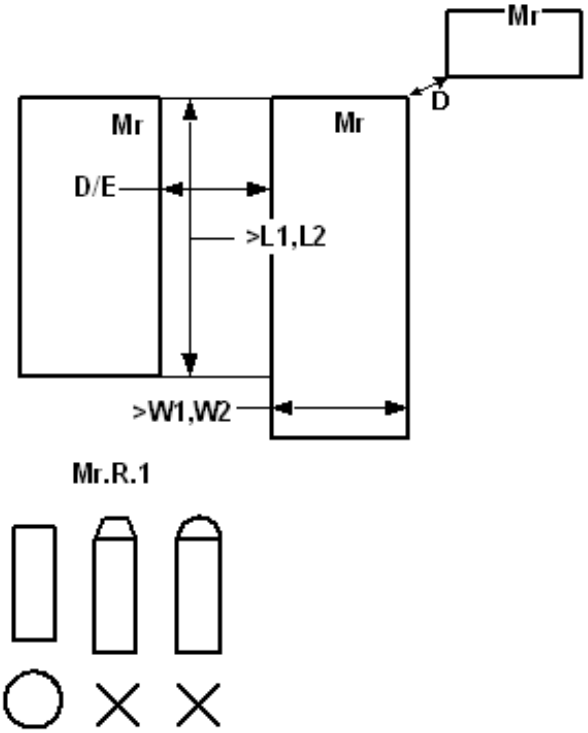


Fig. a Fig. b



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4.5.36 MOM Layout Rules

- MOM is a fringe Metal-Oxide-Metal capacitor. It is based on the capacitance between parallel metal lines separated by the inter-level dielectric. The device does not require any additional masks.
- Although any kind of metal combination, M1/Mx/My/Mz/Mr/Mu/AP, is allowed to build a MOM element in terms of process, TSMC only provides a specific MOM SPICE model and the associated PDK cell named RTMOM which is covered by MOMDMY (CAD layer: 155;0) (see section 4.5.36.1)

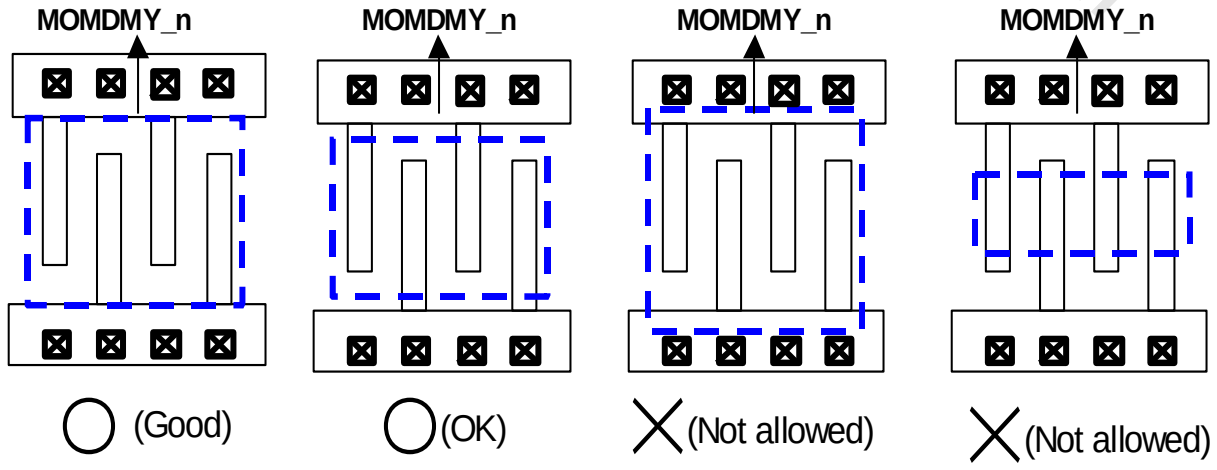
	Non-RTMOM structure			RTMOM structure		
	SPICE	PDK	Process	SPICE	PDK	Process
M1	X	X	O	O	O	O
Mx	X	X	O	O	O	O
My/Mz/Mr/Mu/AP	X	X	O	X	X	O
O: available X: not available						

*Mu is the ultra thick metal (34K Å) for the interconnection and inductor in the MS/RF process.

- MOMDMY_n (n=1~9/AP) is a dummy layer for DRC/LVS to recognize the MOM region.

Layer name	CAD layer	Description	Non-RTMOM structure	RTMOM structure
MOMDMY_1	155;1	M1 MOM region	O	O
MOMDMY_2	155;2	M2 MOM region	O	O for Mx
MOMDMY_3	155;3	M3 MOM region	O	O for Mx
MOMDMY_4	155;4	M4 MOM region	O	O for Mx
MOMDMY_5	155;5	M5 MOM region	O	O for Mx
MOMDMY_6	155;6	M6 MOM region	O	O for Mx
MOMDMY_7	155;7	M7 MOM region	O	O for Mx
MOMDMY_8	155;8	M8 MOM region	O	
MOMDMY_9	155;9	M9 MOM region	O	
MOMDMY_AP	155;20	AP MOM region	O	

- In order to have a good DRC check, you need to draw the MOMDMY_n carefully. The following examples are for your reference.



- You need to pay attention to meet the metal local density rule above/under the MOM element. Therefore, if you want to design a RF MOM circuit with a large area, it is recommended to connect several smaller MOM elements. And each element should be surrounded with dummy metals.

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- The Multi-X Couple layout is recommended for large pair capacitors design to improve the matching performance (see section 4.5.36.1).
- Use symmetrical dummy metals around the matched pairs instead of automatically generated dummy metals.
- Carefully design wire access to capacitor terminals, and consider acess to external metal lines to ensure an optimal symmetry of the device environment.
- MOM can be used for N55.
- TSMC RTMOM PDK cell is without Via.

Rule No.	Description	Label		Rule
MOM.S.1	Space of M1 in MOMDMY_1	A	≥	0.1
MOM.S.2	Space of metal (M1/Mx) line-end in MOMDMY_n	B	≥	0.12
	Definition of MOM without Via Count of {VIAn inside (Mn AND MOMDMY_n) AND (Mn+1 AND MOMDMY_n+1)} ≤ 4, (n=1~9/AP)			
MOM.A.1**	Maximum sidewall area of total metals in MOM without Via. For the definition of the sidewall area of total metals, please refer to the figure 4.5.36.1.	C	≤	7.01E7
	Definition of MOM with Via Count of {VIAn inside (Mn AND MOMDMY_n) AND (Mn+1 AND MOMDMY_n+1)} > 4, (n=1~9/AP)		≥	
MOM.S.3	Space of Metal (M1/Mx) in MOM with Via [excluding the region of metal line end]	D	≥	0.13
MOM.S.4	Space of VIAx in MOM with Via in different net	E	≥	0.13
MOM.A.2**	Maximum sidewall area of {total metals+ total Vias} in MOM with Via. For the definition of the sidewall area of {total metals+ total Vias}, please refer to the figure 4.5.36.2.	F	≤	1.72E5

****The rule value of MOM.A.1 and MOM.A.2 is based on the 3.3V operation voltage. If your layout violates these two rules and you don't apply 3.3V on the MOM application, please refer to the following table to waive the rules.**

	Applied voltage				
Maximum sidewall area	**3.3V**	**2.5V**	**1.8V**	**1.2V**	**1.0V**
MOM without Via	7.01E7	1.82E8	4.27E8	8.94E8	1.14E9
MOM with Via	1.72E5	4.45E5	1.05E6	2.19E6	2.80E6

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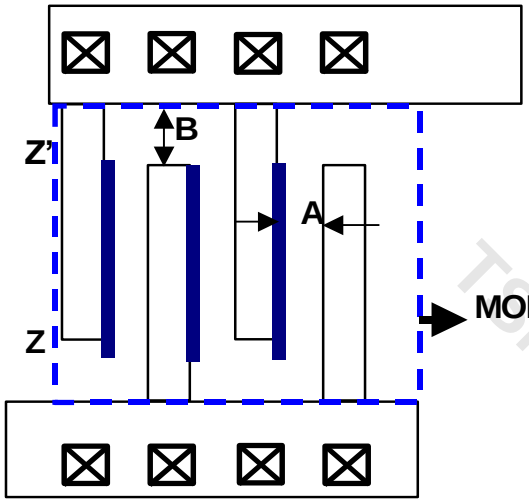
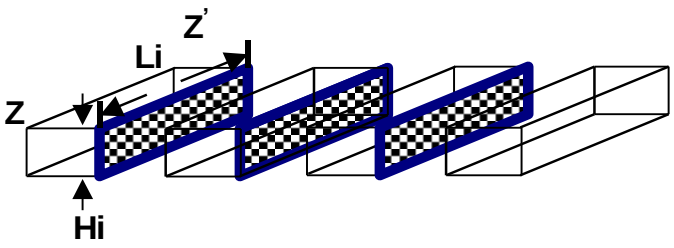
MOM without Via



MOM.A.1



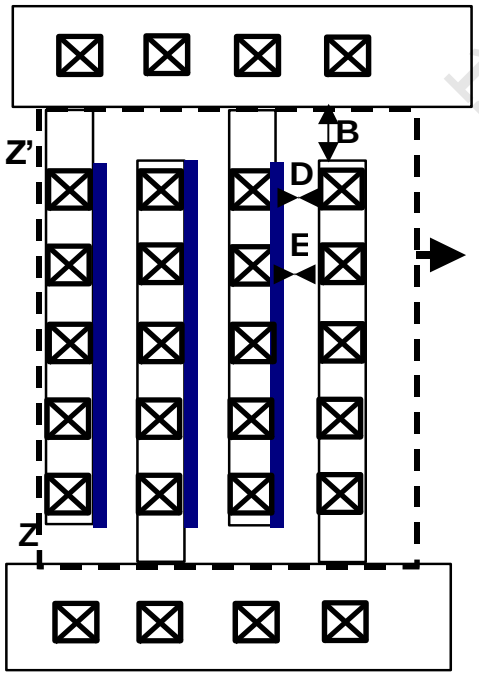
C= Total metal sidewall area

$$= \sum_{i=1}^{n} Hi \times Li$$

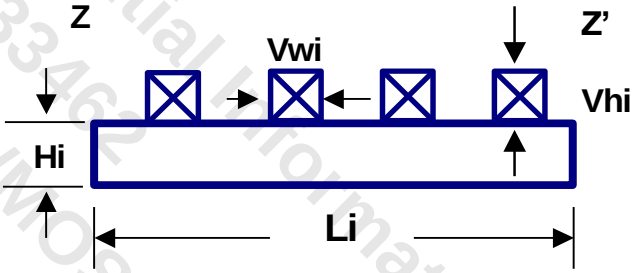
Li= finger length
Hi= metal thickness
n=total metal finger number-1

Figure 4.5.36.1

MOM with Via



MOM.A.2



F= Via total sidewall area + Metal total sidewall area

$$= \sum_{i=1}^{n} Vwi \times Vhi \times m + \sum_{i=1}^{n} Hi \times Li$$

Vwi= via width
Vhi= via height
Hi= metal thickness
Li= metal length
m= total via number per finger
n= total metal finger number-1

Figure 4.5.36.2

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4.5.36.1 RTMOM (Rotated Metal Oxide Metal) Capacitor Guidelines

This section lists the guidelines for TSMC offered RTMOM. The offered RTMOM is a fringe Metal-Oxide-Metal capacitor. It is based on the capacitor between parallel metal lines separated by the inter-level dielectric. The device does not require any additional mask.

1. Although any kind of metal combination, M1/Mx/My/Mz/Mr/Mu/AP, is allowed to build a MOM element in terms of process, TSMC only provides a specific MOM SPICE model and the associated PDK cell named RTMOM which is covered by MOMDMY (CAD layer: 155;0). (The TSMC offered PDK RTMOM is implemented by “Mx” or “Mx/M1”, at least three layers are required).

Metal Layer	RTMOM structure		
	SPICE	PDK	Process
M1	O	O	O
Mx	O	O	O
My/Mz/Mr/Mu/AP(Al-RDL)	X	X	O
O: available X: not available			

2. The poly-shielded layer is adopted to avoid RF performance degradation.
3. For layout flexibility at I/O region, an option of OD2 enclosing floating dummy OD is also available in RTMOM PDK cell..
4. The Multi-X Couple layout is recommended for large-pair capacitor design, which can improve the matching performance. The Parallel and Multi-X Couple layout for match pairs is illustrated in Figure 4.5.36.1.1 and Figure 4.5.36.1.2.
   - The unit cell C1 and the unit cell C2 of the Multi-X Couple RTMOM are placed in an array with alternate pattern placement in each row and each column.
   - If the total capacitance C>400fF is required, it is recommended to use Multi-X Couple layout type with unit cell <200fF, to improve the matching performance. It is not recommended to use 2x200fF Parallel RTMOM design.
5. TSMC RTMOM PDK cell with pre-inserted dummy OD meets all required OD/Poly density rules. If you design your own RTMOM cell, you have to take care the OD/Poly density rules carefully.

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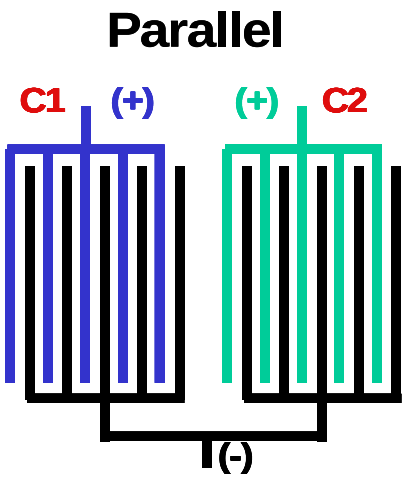

Figure 4.5.36.1.1

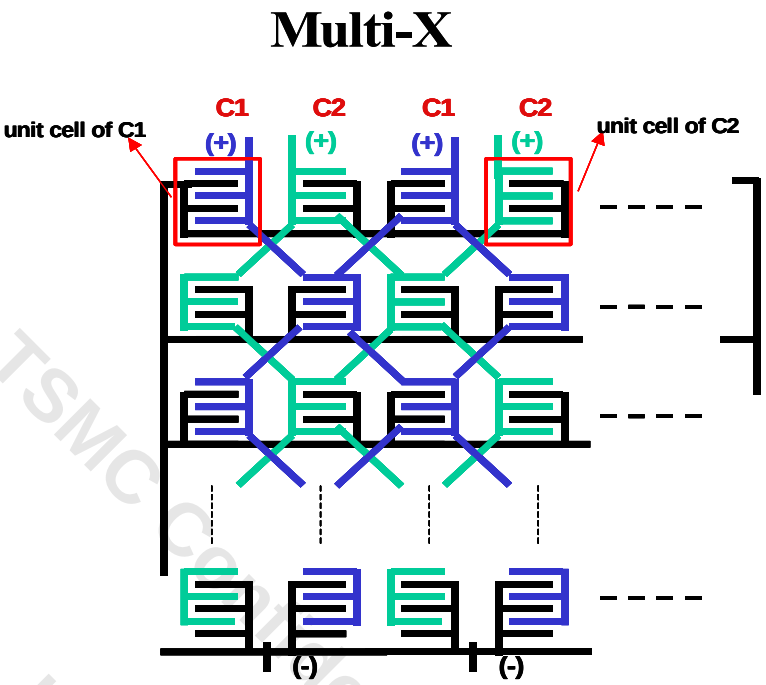

Figure 4.5.36.1.2

6. In order to make sure the SPICE simulation accuracy, and avoid the density rule violation, the following guidelines are recommended.
   - The dummy metal exclusive layers (DMxEXCL) are adopted under RTMOM to avoid dummy pattern insertion. It is not recommended to place below/above the RTMOM any dummy metal patterns or routing. If dummy metal or routing (not generated by PDK itself) are added into the region below/above the RTMOM generated by PDK, the resulting extra parasitic and model inaccuracy must be taken into consideration by designers.
   - If the metal density rule is violated due to the large area of RTMOM, parallel connected small RTMOMs array with dummy metals between individual RTMOM is recommended, as shown in Figure 4.5.36.1.3.

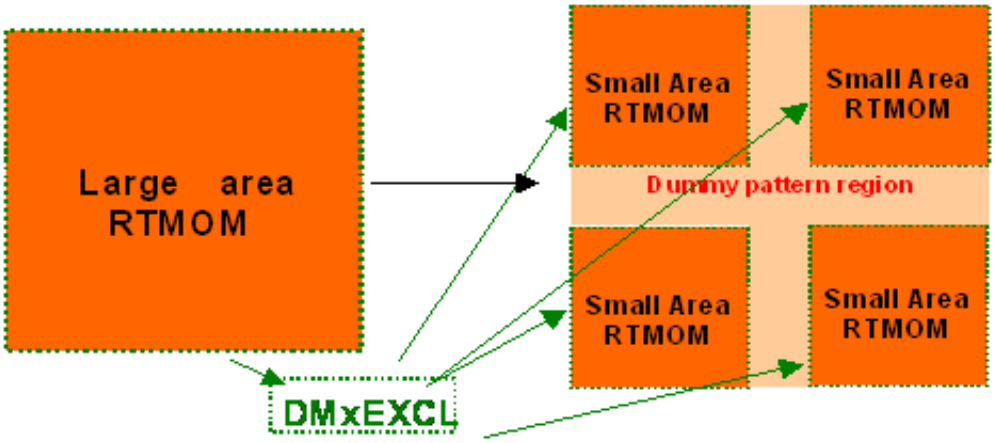

Figure 4.5.36.1.3

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7. Figure 4.5.36.1.4 shows the mismatching (one sigma of delta capacitance) versus $1/C^{0.5}$ of parallel RTMOM pair with 2um fixed distance. SPICE model shot on median value of lots and will be optimistic compared to process variation, it is recommended to reserve enough design margin to cover process variation. Figure 4.5.36.1.4 is for reference only, please refer to the SPICE document, "T-N65-CM-SP-007" for most updated figure.

8. The parallel RTMOM mismatching will increase dramatically as the distance between RTMOM pair larger than 200um, as shown in Figure 4.5.36.1.5. It is recommended to use the RTMOM pair with distance less than 200um for optimized mismatching performance.

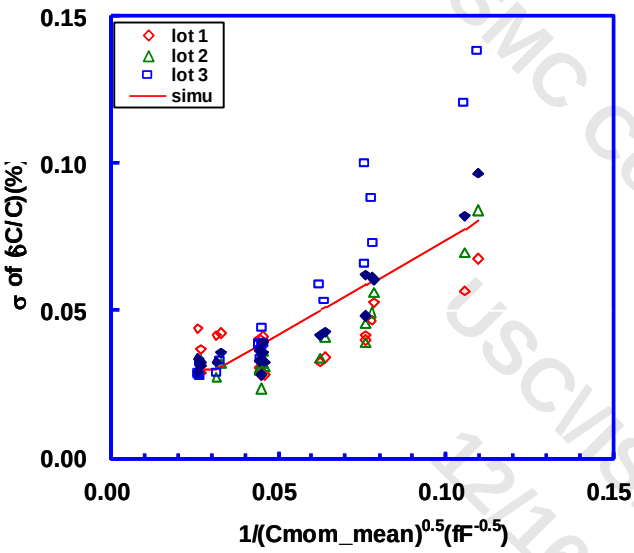

Figure 4.5.36.1.4

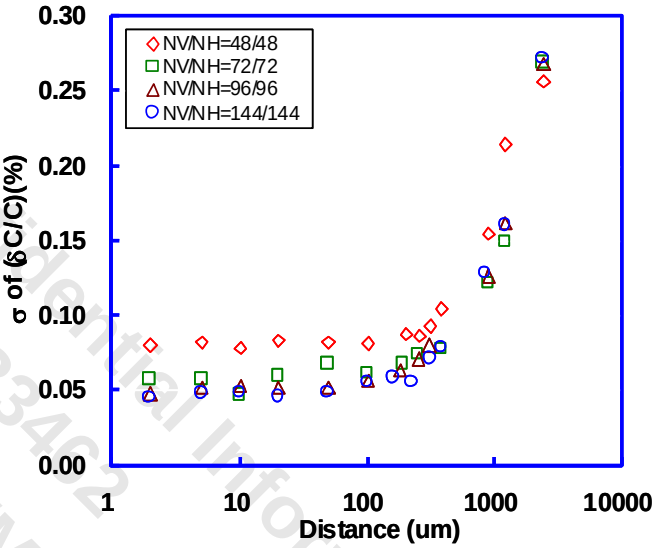

Figure 4.5.36.1.5

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4.5.37 Via Layout Recommendations

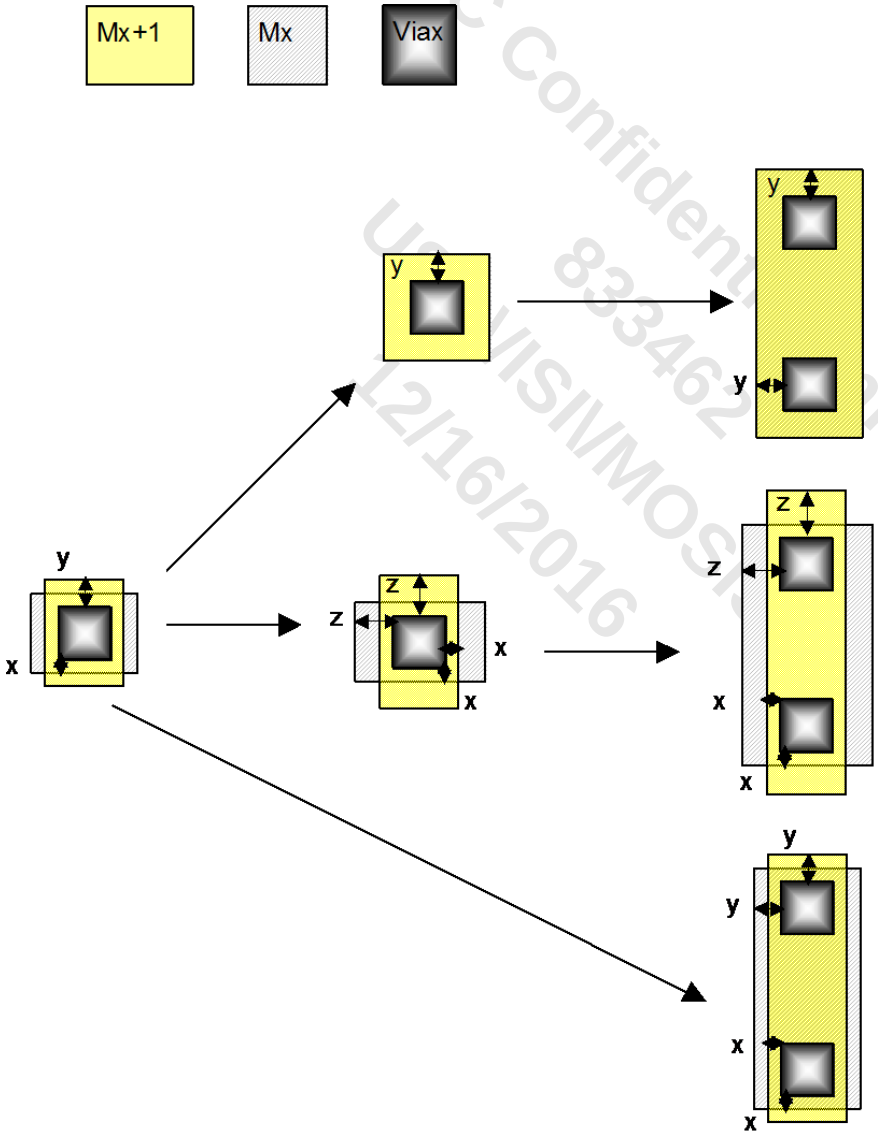
For better yield and reliability, use of a commercial auto router or TSMC utility is recommended to add redundant vias and bigger metal enclosures wherever the layout allows. Please refer to the most updated "T-N65-CL-DR-001-X4, TSMC 65NM CMOS LOGIC DFM LAYOUT ENHANCEMENT UTILITY". You can also download the document from TSMC Online (Design Portal—Reference Flow) for the reference of redundant vias insertion at auto router.

Annotation:

x: value of minimum extension rule (0 nm) (VIAx.EN.1 and Mx.EN.1) or (0 nm)(VIAy.EN.1 and My.EN.1)

y: value of recommended extension (40 nm) (VIAx.EN.1® and Mx.EN.1®) or (50 nm) (VIAy.EN.1® and My.EN.1®), same as line-end extension rule (VIAx.EN.2 and Mx.EN.2) or (VIAy.EN.2 and My.EN.2)

z: value of recommended line-end extension value (70 nm) (VIAx.EN.2® and Mx.EN.2®) or (80 nm) (VIAy.EN.2® and My.EN.2®)



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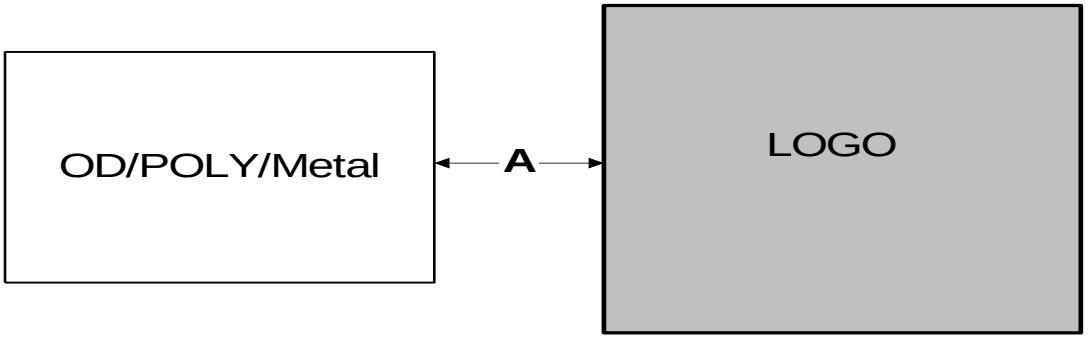
4.5.38 Product Labels and Logo Rules

1. **Use any of the following product labels:**
   - Copyright and year
   - Company logo
   - Part number
   - Mask level names
   - Other similar labels
2. **Make sure there is a dummy layer LOGO (CAD layer no. 158) to do DRC for product labels.**
   Product labels must be fully covered by LOGO dummy layer.
3. **Form the product labels for the CO/Via layer by using squares with minimum width.**
   A big CO/Via polygon for a character (or a numeral) is not allowed.
4. **Don't use minimum rules for the product labels, except for CO/Vias.**
   It is best to have greater than, or equal to, 1 μm of width and space. If the minimum width and space is greater than 1 μm in the rule (for example, 30K thick metal) please use at least the minimum width and space.
5. **To protect the product labels, do not use a dummy OD/Poly/Metal in the LOGO demarcated regions.**
   For process uniformity, keep the LOGO layer and the corresponding product labels at least 10 μm distant from the OD/PO/Metal geometry. Add dummy fill in this 10 μm border region. (The TSMC dummy pattern utility will insert dummy pattern geometry in the 10 μm LOGO border region to minimize the process impact on the circuit OD/PO/Metal geometry that is near the LOGO.)

Rule No.	Description	Label		Rule
LOGO.S.1	Space to OD, PO, or Metals (non-dummy patterns, and non-dummy TCD)	A	≥	10
LOGO.O.1	Overlap of CB, CBD, FW, PM, UBM, DOD, DPO, or DMx is not allowed.			
LOGO.R.1 [U]	A circuit in the LOGO is not allowed.			
LOGO.R.2	The rules of PO.EX.1, PO.EX.2, PO.EX.2®, PO.EX.3, PO.R.1, and PO.R.4 can be exempted from DRC in LOGO area.			



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4.5.39 SRAM Rules

Rule No.	Description			
SRAM.W.1	SRM width (interact with OD). The SRM edge should be aligned to the boundary of the cell array, which may include storage, strapping, and dummy edge cells.	A	≥	0.28
SRAM.S.1	SRM space (interact with OD)	B	≥	0.28
SRAM.S.2	SRM space to {GATE NOT INTERACT SRM}	C	≥	0.12
SRAM.EN.1	SRM enclosure of GATE.	E	≥	0.12
SRAM.EX.1	SRM extension on NW (interact with OD). Extension = 0 is allowed.	D	≥	0.28
SRAM.O.1	SRM Overlap of NW (interact with OD) (for VTC_N, VTC_P). Extension = 0 is allowed.	F	≥	0.28
SRAM.A.1	Enclosed area of donut-type OD (Enclosed area of OD > 0) interact with poly is not allowed in SRM region.	G	≥	0.6
SRAM.R.1^{U}	**Customer-designed SRAM bit cell**: Review by TSMC's R&D and PE before use a customer-designed SRAM bit cell. It is recommended to use the standard TSMC SRAM cells including core, edge, and strap cells. If non-standard cells are used, TSMC requires customers to submit a layout at least one month before tape-out for TSMC to review and approve the use of SRAM cells.			
SRAM.R.2^{U}	**Logic SPICE model**: Don't use TSMC logic SPICE model to design SRAM unless the layout strictly follows the logic design rule for designing SRAM. TSMC's R&D and PE must review the SRAM layout.			
SRAM.R.3^{U}	**Redundancy**: If the accumulated SRAM density is greater than 8.0M bits, redundancy is needed. The accumulated SRAM density is normalized density of **0.525um^2** cell size. Please refer to the most current version of the TSMC Embedded SRAM Redundancy Implementation Rule *(T-000-CL-RP-002*).			
SRAM.R.4^{U}	**SRAM cell implant:** TSMC provides the following V_t implants in SRAM cells (see the table 4.5.39.1): **Cell implant for NMOS (VTC_N), PMOS (VTC_P):** You must provide a special layer SRM. The VTC_N, VTC_P layers are derived from logical operations using "SRM" marker layer**.**			
SRAM.R.5^{U}	**Array delay-tracking bit cells:** This kind of bit cell should be embedded inside an array. If a delay-tracking cell is to be placed outside an array, it should be fully surrounded by dummy bit cells.			
SRAM.R.6^{U}	**Dummy layouts for embedded SRAM**: To minimize proximity and loading effects during processing, you must add dummy layouts to provide a similar surrounding for every cell. To add dummy layouts, please refer to SRAM cell layout documents for guidelines and GDS examples. These documents provide instructions for adding dummy layouts in both columns and rows, at array edges, and at the connection/tap in-between arrays.			
SRAM.R.7^{U}	**SRAMDMY (186;4 & 186;5):** Can only use in the word-line decoder of TSMC SRAM. This layer is only to waive CO.S.3 and G.1. And it must be reviewed by TSMC's R&D and PE even if you uses TSMC cell. SRAMDMY (186;4 & 186;5) is a must for CO mask tape-out if SRAM decoder is rule pushed.			
SRAM.R.12	SRAMDMY (186;4 & 186;5) overlap of SRAMDMY_0 (186;0) is not allowed.			
SRAM.R.13	SRM must fully cover GATE.			
SRAM.R.14	SRAMDMY_0 (186;0) is a must for any SRAM cell with rule pushed layout. It can waive SRAM DRC violations under VIA1 as well as the rules, M2.S.5, M2.A.1, VIA2.EN.2, and M3.EN.2.			
SRAM.R.15	**CO_11 (30;11) is a must for CO mask tape-out in SRAM**. 1. If CO_11 exists, it must cover CO 2. CO_11 must be 0.09um x 0.09um 3. CO_11 must be exactly the same as CO 4. CO_11 must be fully covered by SRM (50;0) and SRAMDMY_0 (186;0)			
SRAM.R.17	SRAMDMY_0 (186;0) must fully cover OD, CO, VIA1.			

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Rule No.	Description
SRAM.R.8g[U]	**SRAM device length/width:** To avoid Pass Gate (PG) leakage impact on SRAM cell electrical performance, the PG channel length should be ≥ 0.07 µm. The PG channel width should be ≥ 0.08 µm. Consult with TSMC regarding the SRAM cell's electrical performance and the suppression of accumulated pass-gate leakage on a bit line.
SRAM.R.9g[U]	**Sense-amp and decoder redundancy**: In addition to bit-row and/or bit-column redundancy design, redundancy in peripheral array elements, such as sense amplifiers and decoders, is recommended. Architectural efficiency can minimize the added overhead area entailed by this additional redundancy. Peripheral element redundancy is especially important for high-density memory blocks.
SRAM.R.10g[U]	**Bit cell orientation**: It is recommended to place the bit cells of related SRAM blocks in the same orientation.
SRAM.R.11g[U]	**Guardring:** It is recommended to have an additional VSS (PW) guardring around the memory circuit block.
SRAM.R.20g[U]	Avoid placing SRAM at the chip corner and chip edge. (Please refer Figure 7.5.7 in Chapter 7)

Table 4.5.39.1 65 nm/ 55nm TSMC SRAM Cells Mask Requirement Summary

	Process Type	N65G/N65GP	N65LP		N65ULP
SRAM Cells Type	**Cell Size**	0.499 um²/ 0.525 um²/ 0.62 um²/ 0.974 um²/ 8T 1.158 um²/ 10T 1.158 um²(G only)	0.525 um²	0.62 um²/ 0.974 um²/ 8T 1.158 um²/	0.525 um²/ 0.62 um² 0.974 um²
std VT	NMOS	PW1V+ VTC_N	PW1V+ VTC_N	PW1V	NA
	PMOS	NW1V+ VTC_P	NW1V		NA
high VT	NMOS	NA	PW1V+ VTH_N		PW1V+ VTH_N + VTC_N
	PMOS	NA	NW1V+ VTH_P		NW1V+ VTH_P

	Process Type	N65LPG			N55GP
		G	LP		
SRAM Cells Type	**Cell Size**	0.62 um²/ 0.974 um²/	0.525 um²	0.62 um²/ 0.974 um²/ 8T 1.158 um²/	0.525 um²/ 0.62 um²/ 0.974 um²/
std VT	NMOS	PW1V+VTH_N(LP)	PW1V+ VTC_N	PW1V	PW1V+ VTC_N
	PMOS	NW1V+VTH_P(LP)	NW1V		NW1V
high VT	NMOS	NA	PW1V+ VTH_N		NA
	PMOS	NA	NW1V+ VTH_P		NA

	Process Type	N55LP	
SRAM Cells Type	**Cell Siz**	0.62 um²/ 0.974 um²/	0.525 um²
std VT	NMOS	PW1V+ VTC_N	NA
	PMOS	NW1V	NA
high VT	NMOS	PW1V+ VTH_N+ VTC_N	
	PMOS	NW1V+ VTH_P	

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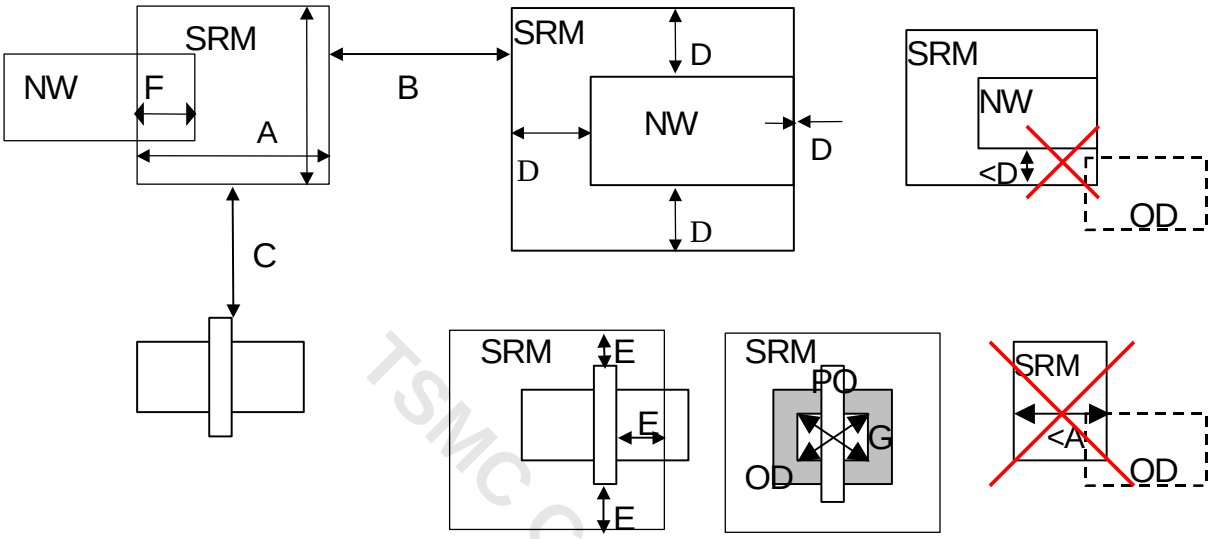

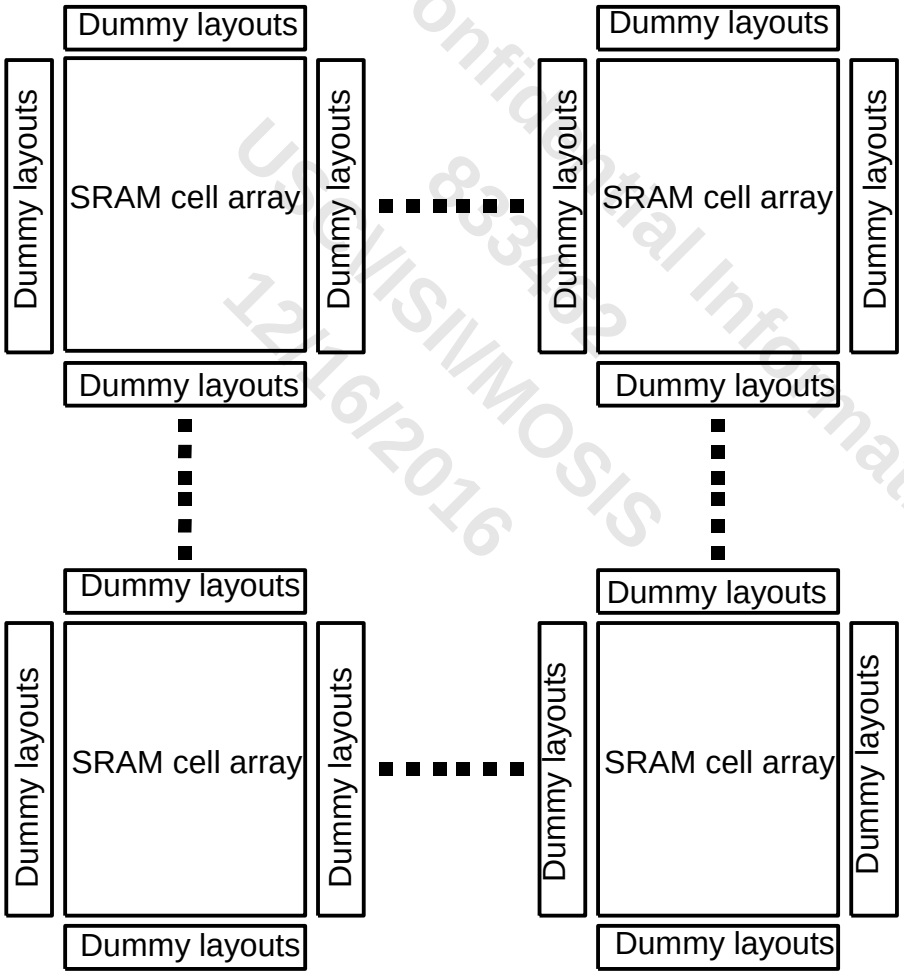

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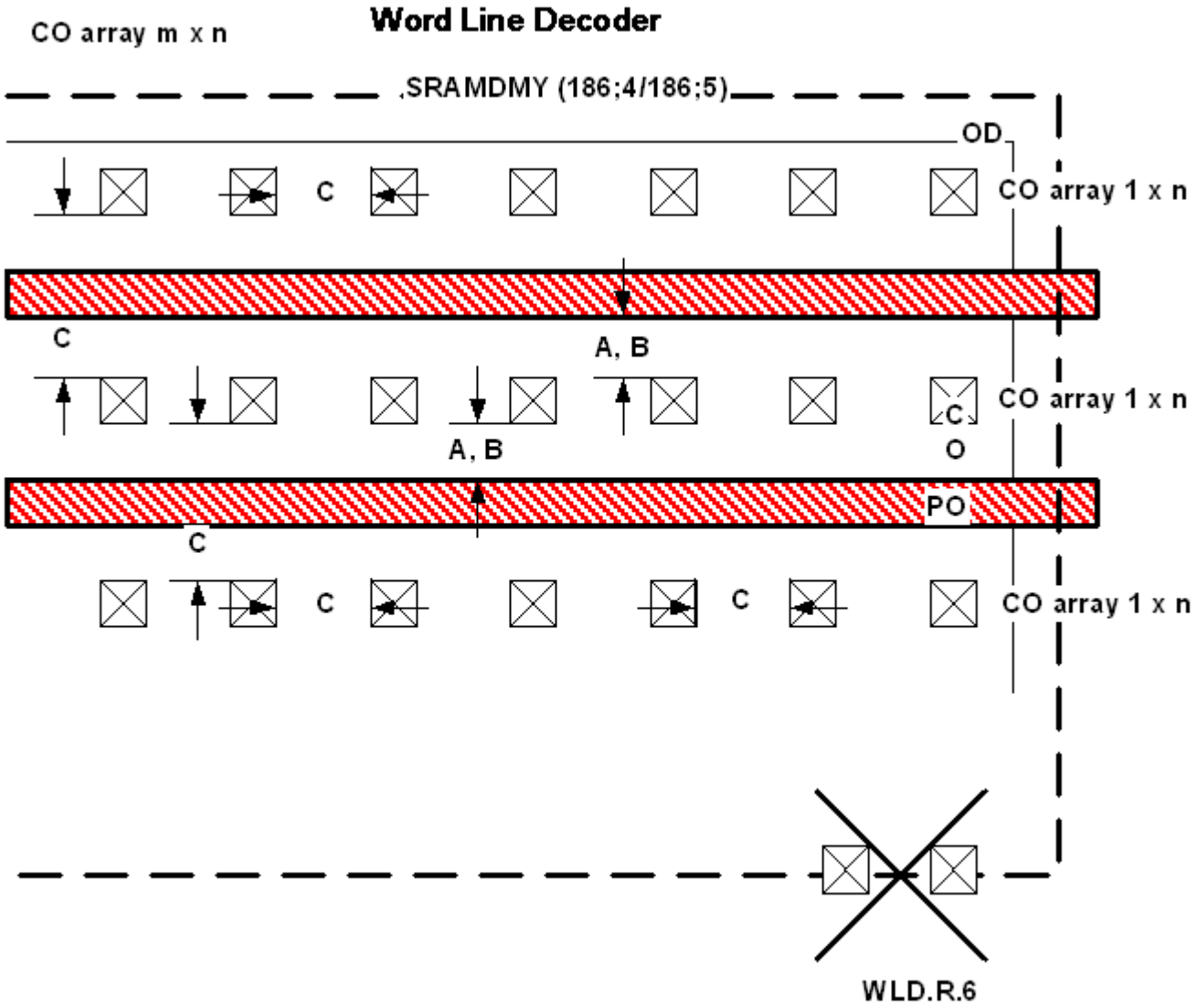
4.5.40 SRAM Periphery (Word Line Decoder) Rules

The following rules only apply to word line decoder covered by SRAMDMY (186;4 & 186;5). 186;5 is used for 0.499μm² cell and 186;4 is used for 0.525 μm², 0.62 μm², 0.974μm², 1.158μm² cell.

Rule No.	Description	Label		Rule
WLD.R.1	{CO AND SRAMDMY_4 (186;4)} space to PO .	A	≥	0.05
WLD.R.2	{CO SRAMDMY_5 (186;5)} space to PO	B	≥	0.043
WLD.R.3	CO space on the same OD [inside SRAMDMY (186;4 & 186;5)]	C	≥	0.14
WLD.R.6	SRAMDMY (186;4 & 186;5) edge cut CO is not allowed.			
WLD.R.7	SRAMDMY_0 (186;0) upsized 200μm must cover SRAMDMY_4 (186;4) or SRAMDMY_5 (186;5)			



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4.5.41 Fuse Rules

- **Laser fuse**

  AP fuse is available. Please refer to T-000-CL-DR-005: TSMC AL FUSE (AP FUSE) DESIGN RULE FOR CU PROCESS

- **Electrical fuse**

  The IP of electrical fuse is provided. Please contact your account manager to get the related information. Besides, the IP can't be shrunk at N55.

4.5.42 Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns

- **The seal ring and chip corner stress relief (CSR) pattern can reduce the impact of damage induced by thermal stress during packaging and field applications.**
- **There are two ways to mount the seal ring and CSR structures in your design:**
  1. **Added by TSMC:** You can request that the seal ring and CSR pattern add by TSMC during post tape out data preparation. Please follow CSR.R.1 in the following table if this option is selected.
  2. **Added by You:** You can choose to add the seal ring and CSR patterns before tape out. Two sample GDS files (archived along with this document) are prepared for this purpose. Please select the proper gds layers matching with the metal scheme of your design by following the seal ring and CSR rules in this section (except CSR.R.1).
     - ***1P9M sample Gds file for using Mz as top metal :*** N65_SR_topMz.gds
     - ***1P9M sample Gds file for using My as top metal:*** N65_SR_topMy.gds
     - ***1P9M sample Gds file for using Mr as top metal:*** N65_SR_1P9M6X2R_20061120_C.gds
     - The following CAD layers are required for seal ring and CSR structure, please keep these layers in the sample gds file: OD (6), PP (25), CO (30), CB (76), CB2 (86), LMARK (109), SEALRING (162), and CSRDMY (166). In addition, please keep CDU (165), PO (17), and NP (26) for CD uniformity patterns for TSMC process monitor purpose.
     - An alignment mark (L-mark) is drawn at seal ring corner. You can use this L-mark for the laser alignment of ID number verification or the metal fuse cutting purpose.
- **TSMC offers new sealring structures can be used in WLCSP/Flip chip/Wire bond packages.**
     - ***1P9M sample Gds file for using Mz as top metal :*** N65_SR_topMz_ 12022016_WLCSP.gds
     - ***1P9M sample Gds file for using My as top metal:*** N65_SR_topMy_ 12022016_WLCSP.gds
     - ***1P9M sample Gds file for using Mr as top metal:*** N65_SR_1P9M6X2R_ 12022016_WLCSP.gds
- **Mask combination CB (mask ID:107)/ AP (mask ID: 307)/ CB (mask ID:107) is not allowed for WLCSP process.**

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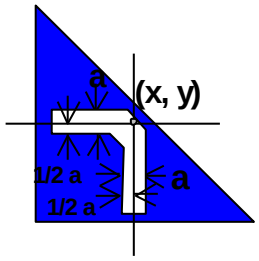
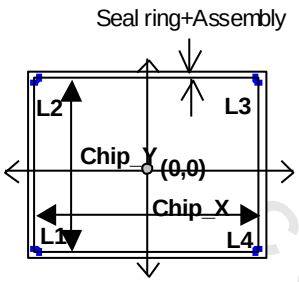
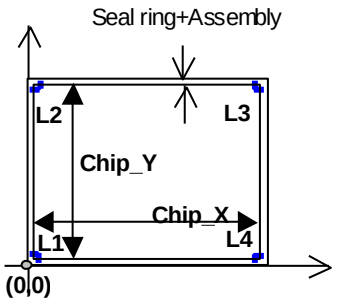
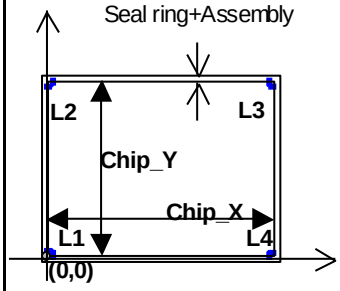
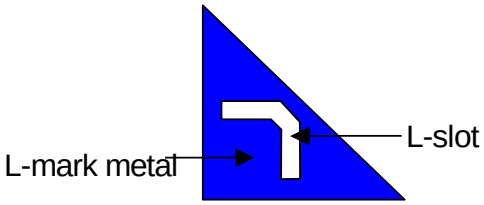
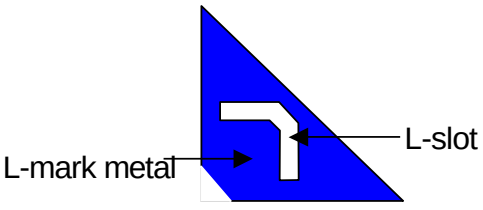
The Reference coordinates of L-mark: You can calculate the coordinates of L-mark by yourself, or follow the coordinates of the below table.

(Chip_X, Chip_Y) are the dimensions of the chip (without sealring and assembly isolation)

L-Mark Coordinates (μm)	Coordinate A	Coordinate B	Coordinate C
			
	(0, 0) is at the center of the chip	(0, 0) is at bottem-left of the chip with sealring (10um) and assembly isolation (10um)	(0, 0) is at bottem-left of the chip without sealring (10um) and assembly isolation (10um)
L1	(-0.5X+14.25, -0.5Y+14.25)	(34.25, 34.25)	(14.25, 14.25)
L2	(-0.5X+14.25, 0.5Y-14.25)	(34.25, Y+5.75)	(14.25, Y-14.25)
L3	(0.5X-14.25, 0.5Y-14.25)	(X+5.75, Y+5.75)	(X-14.25, Y-14.25)
L4	(0.5X-14.25, -0.5Y+14.25)	(X+5.75, 34.25)	(X-14.25, 14.25)

- **L-mark metal:** a solid metal (top Cu metal) with an L shaped slot in LMARK.
- **L-mark metal in CSR:** L-mark metal in a CSR pattern.
- **L-slot**: L shaped hole in the L-mark metal
- **L-mark metal layer:** Only top Cu metal is required for L-mark metal, and AP for L-mark metal is not allowed.





WLCSP L-mark

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4.5.42.1 Metallization Options

The general 65 nm logic process is offered with a single poly and nine metal layers (1P9M). In addition to 1P9M, please refer to the following tables for the other metallization options.

For any metal combination, a marker (1+A+B+C)M_AxByCz or (1+A+D)M_AxDr can be used to represent the metal combination of Mx, My, Mz, and Mr.

The marker is interpreted as one layer of M1, A layers of Mx, B layers of My, C layers of Mz, and D layers of Mr. The total metal layer number is 1+A+B+C or 1+A+D.

Naming for Different Metal Thicknesses

Metal type	Code	W/S (μm)	Thickness (Å).	Mask layers
M1	M1	0.09/0.09	1800	M1 (360) only
First Inter-layer Metal	Mx	0.1/0.1	2200	M2~M7 (380, 381, 384, 385, 386, 387), max : six layers
Second Inter-layer Metal	My	0.2/0.2	5000	M5~M7 (385, 386, 387), max : two layers
Top Metal (2XTM)	My	0.2/0.2	5000	M3~M9 (381, 384, 385, 386, 387, 388, 389), max : two layers
Top Metal (4XTM)	Mz	0.4/0.4	9000	M3~M9 (381, 384, 385, 386, 387, 388, 389), max : two layers
Top Metal	Mr	0.5/0.5	12500	M6~M9 (386, 387, 388, 389), max: two layers

Naming for Different Via Types

Via type	Code	W/S(μm)	Mask layers
First Inter-layer Via	Vx	0.1/0.1	VIA1~VIA6 (378, 379, 373, 374, 375, 376), max : six layers
Second Inter-layer Via	Vy	0.2/0.2	VIA4~VIA6 (374, 375, 376), max : two layers
Top Via (2XTM)	Vy	0.2/0.2	VIA2~VIA8 (379, 373, 374, 375, 376, 377, 372), max : two layers
Top Via (4XTM)	Vz	0.36/0.34	VIA2~VIA8 (379, 373, 374, 375, 376, 377, 372), max : two layers
Top Via	Vr	0.46/0.44	VIA5~VIA8 (375, 376, 377, 372), max: two layers

Metallization CAD Layers

Layer	CAD Layer ID
Metal-1	31
Via-1	51
Metal-2	32
Via-2	52
Metal-3	33
Via-3	53
Metal-4	34
Via-4	54
Metal-5	35
Via-5	55
Metal-6	36
Via-6	56
Metal-7	37
Via-7	57
Metal-8	38
Via-8	58
Metal-9	39

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For example, in a 9M_4x2y2z scheme, the Via-5, Metal-6, Via-6, and Metal-7 should use layer (55;20), (36;20), (56;20), and (37;20), respectively, for My and Vy layers. The Via-7, Metal-8, Via-8, and Metal-9 should use layer (57;40), (38;40), (58;40), and (39;40), respectively for Mz and Vz layers. The Metal-1 through Metal-5 should follow their respective CAD layer ID with data type 0.

If you want to add the CSR patterns and the seal ring before tape out (option 2), please use TSMC sample GDS file for seal ring and CSR as a starting file, and follow the descriptions below to select the related metal and via layers for your design.

4.5.42.1.1 Metallization Options Using Mz as the Top Metal

1. **Start with "N65_SR_topMz .gds" sample gds file. Select the metallization layers from the table below based on the target metallization scheme. Delete from the sample gds any metal and via layers that are not listed in the column.**

	Metallization Options using Mz as Top Metal																	
Metal Scheme	**1P3M**	**1P4M**	**1P5M**		**1P6M**			**1P7M**				**1P8M**				**1P9M**		
	1x1z	**2x1z**	**3x1z**	**2x2z**	**4x1z**	**3x2z**	**3x1y1z**	**5x1z**	**4x2z**	**4x1y1z**	**3x2y1z**	**6x1z**	**5x2z**	**4x2y1z**	**4x1y2z**	**6x2z**	**5x1y2z**	**4x2y2z**
M1	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0
VIA1	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0
M2	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0
VIA2	**58:40***	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0
M3	**39:40***	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0
VIA3		**58:40***	53:0	**57:40***	53:0	53:0	53:0	53:0	53:0	53:0	53:0	53:0	53:0	53:0	53:0	53:0	53:0	53:0
M4		**39:40***	34:0	**38:40***	34:0	34:0	34:0	34:0	34:0	34:0	34:0	34:0	34:0	34:0	34:0	34:0	34:0	34:0
VIA4			**58:40***	**58:40***	54:0	**57:40***	*56:20**	54:0	54:0	54:0	*55:20**	54:0	54:0	54:0	54:0	54:0	54:0	54:0
M5			**39:40***	**39:40***	35:0	**38:40***	*37:20**	35:0	35:0	35:0	*36:20**	35:0	35:0	35:0	35:0	35:0	35:0	35:0
VIA5					**58:40***	**58:40***	**58:40***	55:0	**57:40***	*56:20**	*56:20**	55:0	55:0	*55:20*	*56:20**	55:0	55:0	*55:20*
M6					**39:40***	**39:40***	**39:40***	36:0	**38:40***	*37:20**	*37:20**	36:0	36:0	*36:20*	*37:20**	36:0	36:0	*36:20*
VIA6								**58:40***	**58:40***	**58:40***	**58:40***	56:0	**57:40***	*56:20*	**57:40***	56:0	*56:20*	*56:20*
M7								**39:40***	**39:40***	**39:40***	**39:40***	37:0	**38:40***	*37:20*	**38:40***	37:0	*37:20*	*37:20*
VIA7												**58:40***	**58:40***	**58:40***	**58:40***	**57:40**	**57:40**	**57:40**
M8												**39:40***	**39:40***	**39:40***	**39:40***	**38:40**	**38:40**	**38:40**
VIA8																**58:40**	**58:40**	**58:40**
M9																**39:40**	**39:40**	**39:40**

2. **Re-assign the layers marked with "*" by the appropriate CAD layers to match with the CAD ID for that layer.**

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Example: For a design with 6M_3x1y1z.

Step 1: Locate the "3x1y1z" column under "1P6M" in the metallization options table above. Delete unused metal and via layers: (54;0), (35; 0), (55;0),(36;0),(56;0),(37;0), (55;20) (36;20), (57;40) and (38;40) .

Step 2: Re-assign CAD ID for the layers denoted with "", from (56;20), (37;20), (58;40) and (39;40), respectively, to (54;20), (35:20), (55:40) and (36:40) to match with your metallization scheme.*

4.5.42.1.2 Metallization Options Using My as the Top Metal

1. **Start with "N65_SR_topMy .gds" sample gds file. Select the metallization layers from the table below based on the target metallization scheme. Delete from the sample gds any metal and via layers that are not listed in the column.**

	Metallization Options using My as Top Metal										
Meta	**1P3M**	**1P4M**	**1P5M**		**1P6M**		**1P7M**		**1P8M**		**1P9M**
ISchem	**1x1y**	**2x1y**	**3x1y**	**2x2y**	**4x1y**	**3x2y**	**5x1y**	**4x2y**	**6x1y**	**5x2y**	**6x2y**
M1	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0	31:0
VIA1	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0	51:0
M2	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0	32:0
VIA2	***58:20****	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0	52:0
M3	***39:20****	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0	33:0
VIA3		***58:20****	53:0	***57:20****	53:0	53:0	53:0	53:0	53:0	53:0	53:0
M4		***39:20****	34:0	***38:20****	34:0	34:0	34:0	34:0	34:0	34:0	34:0
VIA4			***58:20****	***58:20****	54:0	***57:20****	54:0	54:0	54:0	54:0	54:0
M5			***39:20****	***39:20****	35:0	***38:20****	35:0	35:0	35:0	35:0	35:0
VIA5					***58:20****	***58:20****	55:0	***57:20****	55:0	55:0	55:0
M6					***39:20****	***39:20****	36:0	***38:20****	36:0	36:0	36:0
VIA6							***58:20****	***58:20****	56:0	***57:20****	56:0
M7							***39:20****	***39:20****	37:0	***38:20****	37:0
VIA7									***58:20****	***58:20****	***57:20***
M8									***39:20****	***39:20****	***38:20***
VIA8											***58:20***
M9											***39:20***

2. **Re-assign the layers marked with "*" by the appropriate CAD layers to match with the CAD ID for that layer.**

Example: For a design with 6M_3x2y.

Step 1: Locate the "3x2y" column under "1P6M" in the metallization options table above. Delete unused metal and via layers: (54;0), (35; 0), (55;0) (36;0), (56;0) and (37;0).

Step 2: Re-assign CAD ID for the layers denoted with "", from (57;20), (38;20), (58;20) and (39;20), respectively, to (54;20), (35;20), (55;20) and (36;20) to match with your metallization scheme.*

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4.5.42.1.3 Metallization Options Using Mr as the Top Metal

1. **Start with "N65_SR_1P9M6X2R_20061120_C.gds" sample gds file. Select the metallization layers from the table below based on the target metallization scheme. Delete from the sample gds any metal and via layers that are not listed in the column.**

	Metallization Options using Mr as Top Metal					
Metal Scheme	**1P6M**	**1P7M**		**1P8M**		**1P9M**
	4x1r	**5x1r**	**4x2r**	**6x1r**	**5x2r**	**6x2r**
M1	31:0	31:0	31:0	31:0	31:0	31:0
VIA1	51:0	51:0	51:0	51:0	51:0	51:0
M2	32:0	32:0	32:0	32:0	32:0	32:0
VIA2	52:0	52:0	52:0	52:0	52:0	52:0
M3	33:0	33:0	33:0	33:0	33:0	33:0
VIA3	53:0	53:0	53:0	53:0	53:0	53:0
M4	34:0	34:0	34:0	34:0	34:0	34:0
VIA4	54:0	54:0	54:0	54:0	54:0	54:0
M5	35:0	35:0	35:0	35:0	35:0	35:0
VIA5	***58:80****	55:0	***57:80****	55:0	55:0	55:0
M6	***39:80****	36:0	***38:80****	36:0	36:0	36:0
VIA6		***58:80****	***58:80****	56:0	***57:80****	56:0
M7		***39:80****	***39:80****	37:0	***38:80****	37:0
VIA7				***58:80****	***58:80****	***57:80***
M8				***39:80****	***39:80****	***38:80***
VIA8						***58:80***
M9						***39:80***

2. **Re-assign the layers marked with "*" by the appropriate CAD layers to match with the CAD ID for that layer.**

Example: For a design with 7M_4x2r.

Step 1: Locate the "4x2r" column under "1P7M" in the metallization options table above. Delete unused metal and via layers: (55;0) (36;0), (56;0) and (37;0).

Step 2: Re-assign CAD ID for the layers denoted with "", from (57;80), (38;80), (58;80) and (39;80), respectively, to (55;80), (36;80), (56;80) and (37;80) to match with your metallization scheme.*

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4.5.43 Chip Corner Stress Relief Pattern (CSR)

Rule No.	Description		Layout Rule (um)
CSR.R.1	If the you requests TSMC to add CSR and seal ring, triangle empty areas (74 um) at 4 chip corners must be reserved and no layout is allowed inside, as shown in Fig.1a		

Warning: Violation of this rule may result in serious layout mistake thus the corrections of many masks may be required! Please jobview the mask data after adding CSR and seal ring by tsmc.

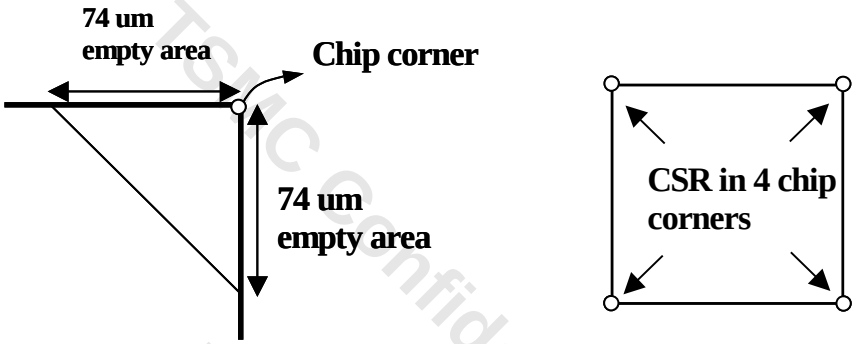

Fig.1a

Warning: A "L-Slot" is an alignment mark structure for the purpose of laser repair alignment. L-slot is an L-shape opening at the top metal level .

CSR.R.2	The CSR structure must include M9/M8 (top metal), VIA8/VIA7 (top via), M7, VIA6…VIA1, M1, CO, PP, OD layers. CSR is a fence type formed by crossed 2.5 µm metals with CO/Via located at the metal crossing, except M9. The CSR patterns are fully covered by a solid M9, as shown in Fig.2b. Therefore, fully overlapped vias and metals of all levels (except top vias) are formed.			
CSR.S.1	CO space	A1	≥	0.36
CSR.EN.1	CO enclosure by metal [crossing area]	B1	≥	0.53
CSR.S.2	VIAx space	A2	≥	0.35
CSR.EN.2	VIAx enclosure by metal [crossing area]	B2	≥	0.525
CSR.S.3	VIAy space	A4	≥	0.34
CSR.EN.3	VIAy enclosure by metal [crossing area]	B4	≥	0.61
CSR.S.4	VIAz space	A3	≥	0.56
CSR.EN.4	VIAz enclosure by metal [crossing area]	B3	≥	0.61
CSR.S.5	VIAr space	A5	≥	0.89
CSR.EN.9	VIAr enclosure by metal [crossing area]	B5	≥	0.345
CSR.R.3	(CO/VIAx, VIAy, VIAz/Viar) number at metal crossing area	D	=	(16, 9,4)
CSR.W.1	Width of L-slot	a	=	10
CSR.L.1	Minimum length of L-slot	b	≥	20
	Maximum length of L-slot		≤	25
CSR.EN.5	Top metal enclosure of L-slot [in the direction of the L-slot length] (Except WLCSP sealring region)	c	≥	4
			≤	8
CSR.EN.5.1	Top metal enclosure of L-slot [in the direction of the L-slot length] for WLCSP	c	≥	5
			≤	9
CSR.EN.6	Top metal enclosure of L-slot [perpendicular to the direction of the L-slot length] (Except WLCSP sealring region)	c'	≥	28
			≤	29

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CSR.EN.6.1	Metal layers of sealring corners can only exist isosceles triangle for WLCSP sealring region. An empty isosceles triangle area must exist butted to the WLCSP sealring outside corner.			
	Minimum length of isosceles triangle(except AP)	c'	≥	19
	Maximum length of isosceles triangle(except AP)		≤	20
CSR.EN.6.2	Minimum length of AP layer isosceles triangle for WLCSP sealring region	c'	≥	19.2
	Maximum length of AP layer isosceles triangle for WLCSP sealring region		≤	20.3
CSR.W.2	Width of 45-degree corner of L-slot	d	≥	6
			≤	10
CSR.W.3	Width of Via ring (VIAx/VIAy/VIAz/VIAr) around CSR pattern and L-slot	e	=	0.1/0.2/0.36/0.29
CSR.EN.7	Metal enclosure of (VIAx/VIAy/VIAz/VIAr) around L-slot	f	≥	0.52/0.47/0.58/0.345
CSR.EN.8	Mx/inter My enclosure by MT around the L-slot	g	≥	0.25

Remark:

Chip corner stress relief pattern and seal ring structures are based on 1P9M process:

*CSRDMY is a dummy layer aligned to the boundary of stress relief pattern in region I for DRC. Please refer to Fig. 1.b in the next page.

*Square CO/Via must follow each layer's width rule.

*For more than 2 top metal layers (My/Mz/Mr) with generic top metal thickness, the Via (Vy-1/Vz-1/Vr-1) below the thick metal (My/Mz/Mr) must follow CSR.S.3/4/5, CSR.EN.3/4/5, and other VIA7/VIA8 rules.

*Please be careful with the non-generic logical operation, CAD bias, and shrinkage effects on the drawn dimensions of stress relief pattern and seal ring.

For flip-chip product,

CBD (mask code 107) layout is same as CB.

* Do not draw UBM (mask code 020) layout on chip corner stress relief pattern, seal ring and assembly isolation. No UBM metal is left on these regions.

* Please draw AP (mask 307) on seal ring as shown in next 3 pages.

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Chip Corner Stress Relief pattern

Chip corner stress relief pattern can reduce the impact of damage induced by thermal stress during packaging and field application. Please refer to region I in Fig. 1 as an example.

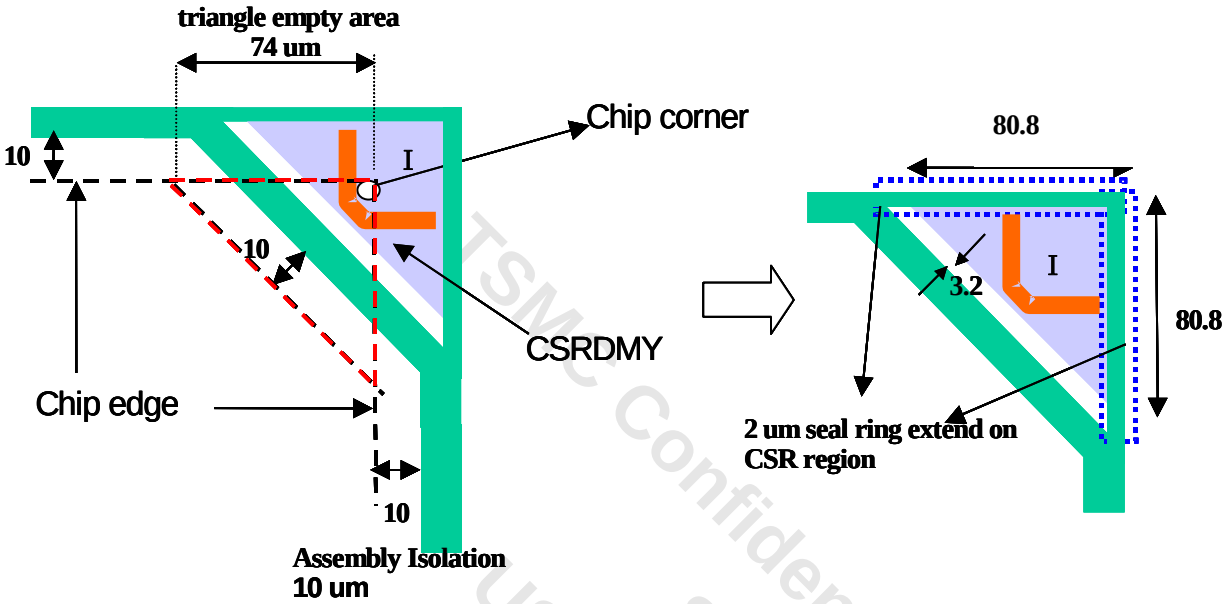
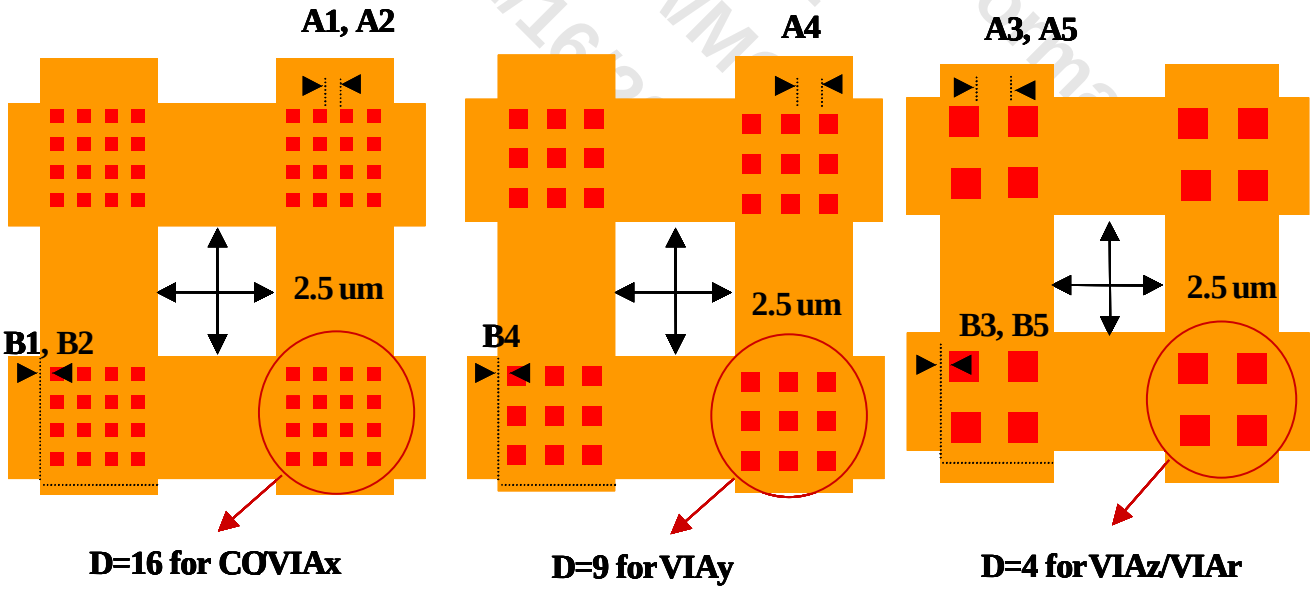


Fig. 1.b, the shape of seal ring and CSR

Within the region I, user must add dummy pattern for Chip Corner Stress Relief



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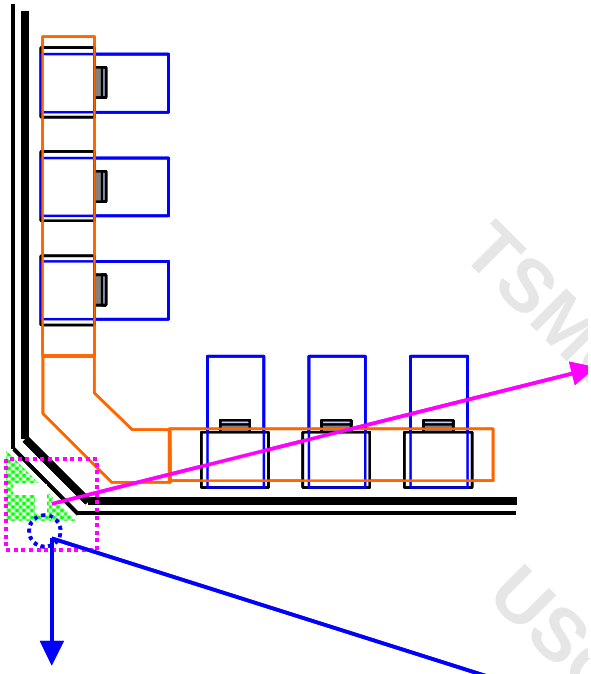
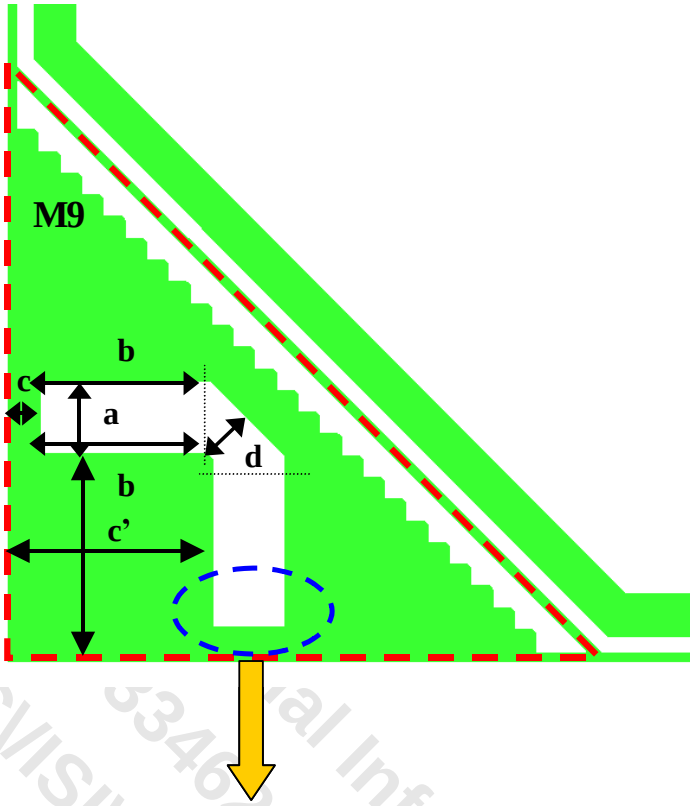
Chip Corner Stress Relief Pattern (Fig. 2)

Top View Fig. 2a

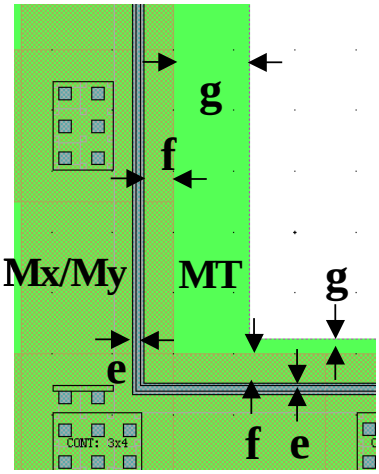


M9 Layout Fig. 2b

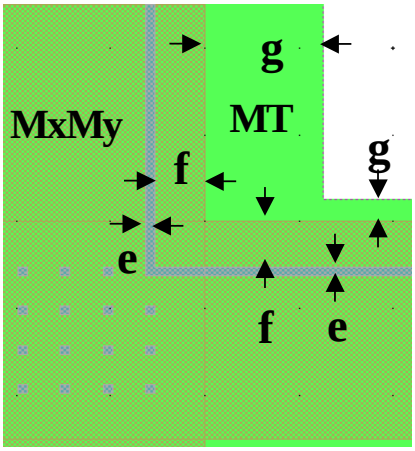


CO/Viax/Viay/Viaz/Viar layout in L-Mark area Fig.2c.

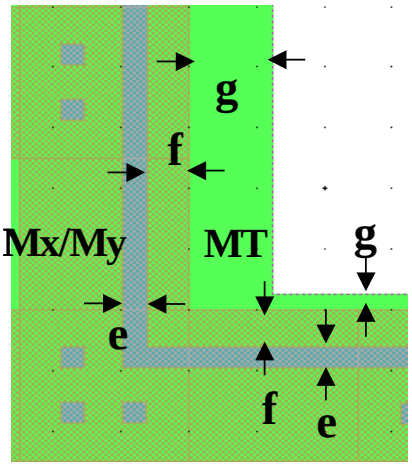
CO/Viax



Viay



Viaz/Viar



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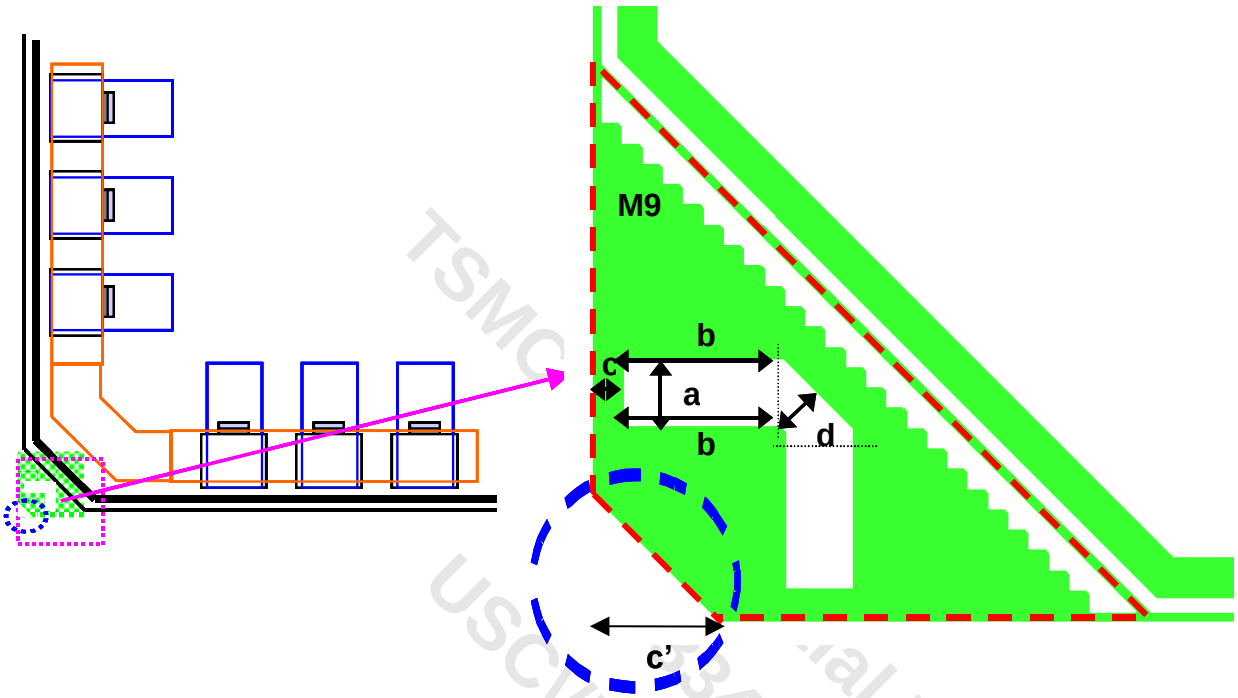
Chip Corner Stress Relief Pattern for WLCSP:



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4.5.44 Seal Ring Layout Rules

Please follow exactly the schematic diagram below (as in the GDS example) for seal-ring layout. Now, DRC cannot fully check these dimensions. If you do not use these dimensions as below, please consult with TSMC.
In the following Figure, the 10 μm measure for assembly isolation is for reference only. Assembly isolation depends on the capability of assembly house. If seal ring is added by TSMC, TSMC will add assembly isolation and seal-ring structure at the same time.
Al pad (AP)/Polyimide (PM) can be generated by logic operation only for non-flip-chip product.

Rule No.	Description		Rule
SR.S.1	Width of Assembly isolation Only M1~Mtop and CDU allowed in assembly isolation region. [For non-WLCSP seal ring] (1) Connect circuit to seal ring through M1~Mtop if needed. (2) Connect circuit to seal ring through AP is not allowed. [For WLCSP seal ring] (1) Connect circuit to seal ring through M1~Mtop if needed. (2) For connecting circuit to seal ring through AP, it is only allowed connecting to the most inner seal ring (AP overlaps with CB2 is not allowed).	≥	10
SR.R.1	SEALRING layer is a must if either you add sealring by themselves, or metal fuse is used.		
SR.EN.1	(OD interact seal ring) enclosure of metal with the outer edge of seal ring.	≥	0.5
CO.W.2	Width of CO bar. CO bar is only allowed in seal ring. CO bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover CO bar if CO bar is used.	=	0.09
VIAx.W.2	Width of VIAx bar. VIAx bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover VIAx bar if VIAx bar is used.	=	0.1
VIAy.W.2	Width of VIAy bar. VIAy bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover VIAy bar if VIAy bar is used.	=	0.2
VIAz.W.2	Width of VIAz bar. VIAz bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover VIAz bar if VIAz bar is used.	=	0.36
VIAr.W.2	Width of VIAr bar. VIAr bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover VIAr bar if VIAr bar is used.	=	0.29

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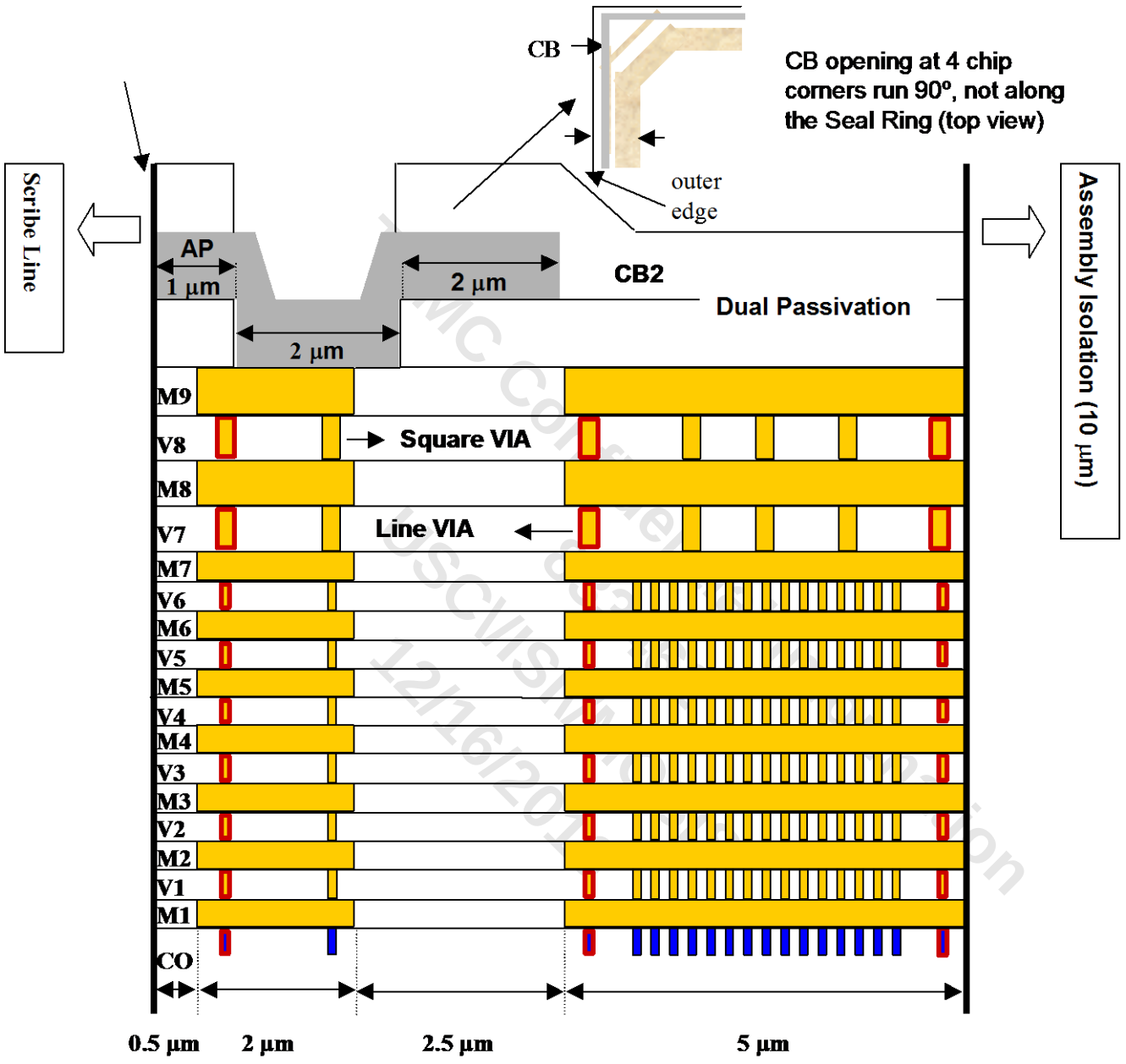
Cross-sectional view of seal ring



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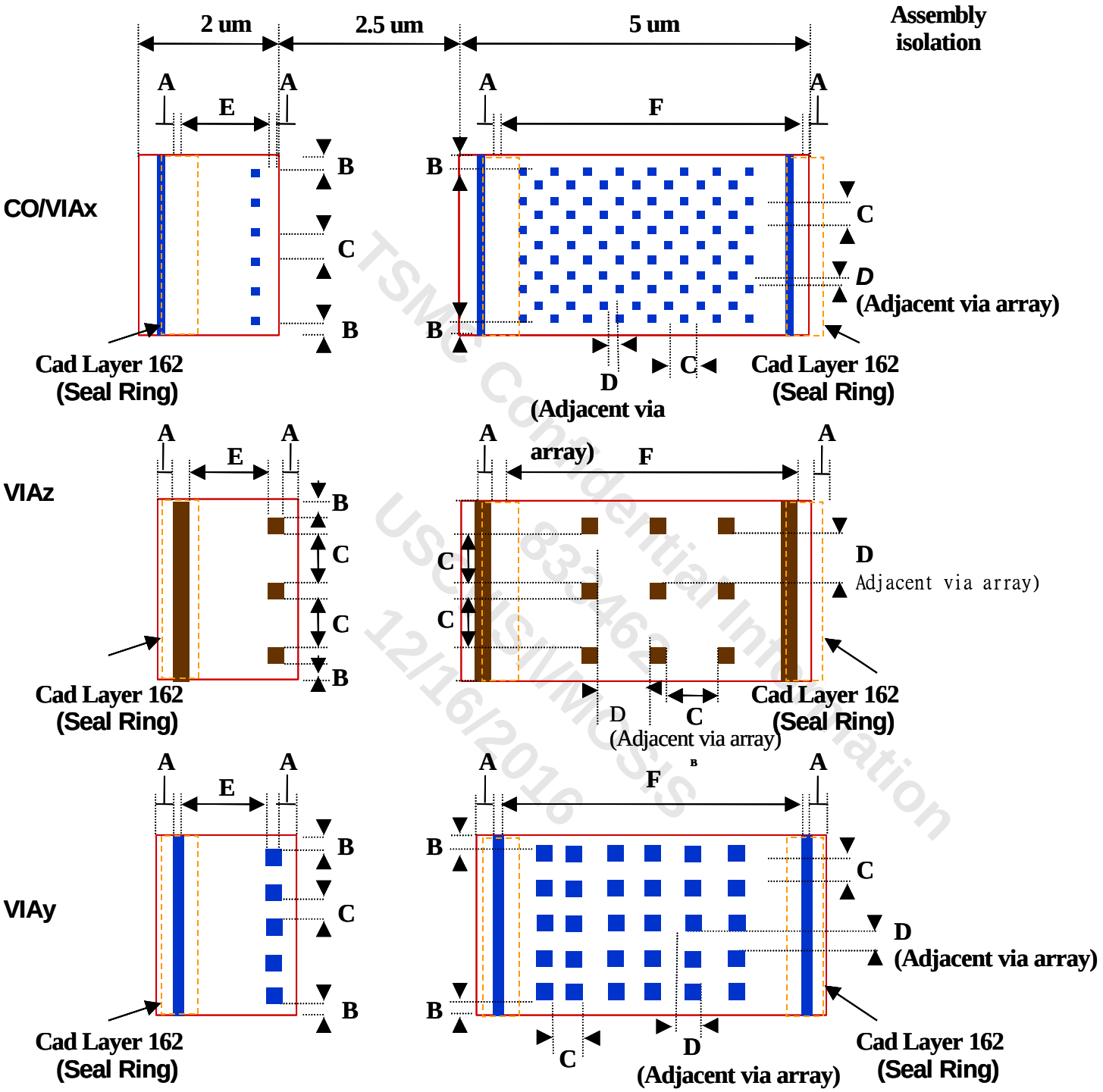
Top view of seal ring



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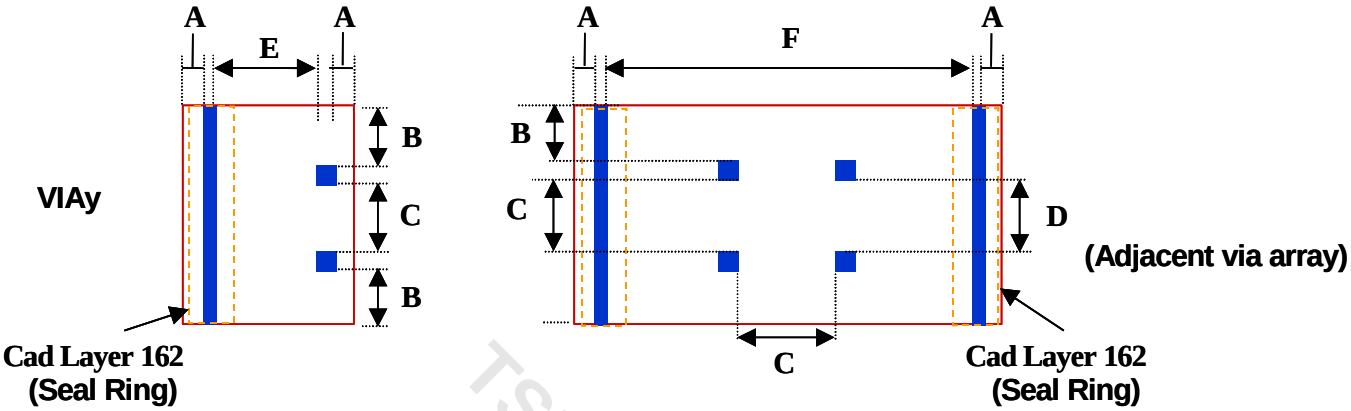

Layer	Width		A	B	C	D	E	F
	Bar	square						
CO	0.09	0.09	0.275	0.18	0.36	0.135	1.27	4.27
VIAx (VIA1~VIA6)	0.1	0.1	0.27	0.175	0.35	0.125	1.26	4.26
VIAy (VIA2~VIA8)	0.2	0.2	0.22	0.17	0.34	0.34	1.16	4.16
VIAz (VIA2~VIA8)	0.36	0.36	0.14	0.27	0.54	0.54	1	4
VIAr (VIA5~VIA8)	0.29	0.46	0.21	0.445	0.89	0.89	0.83	4

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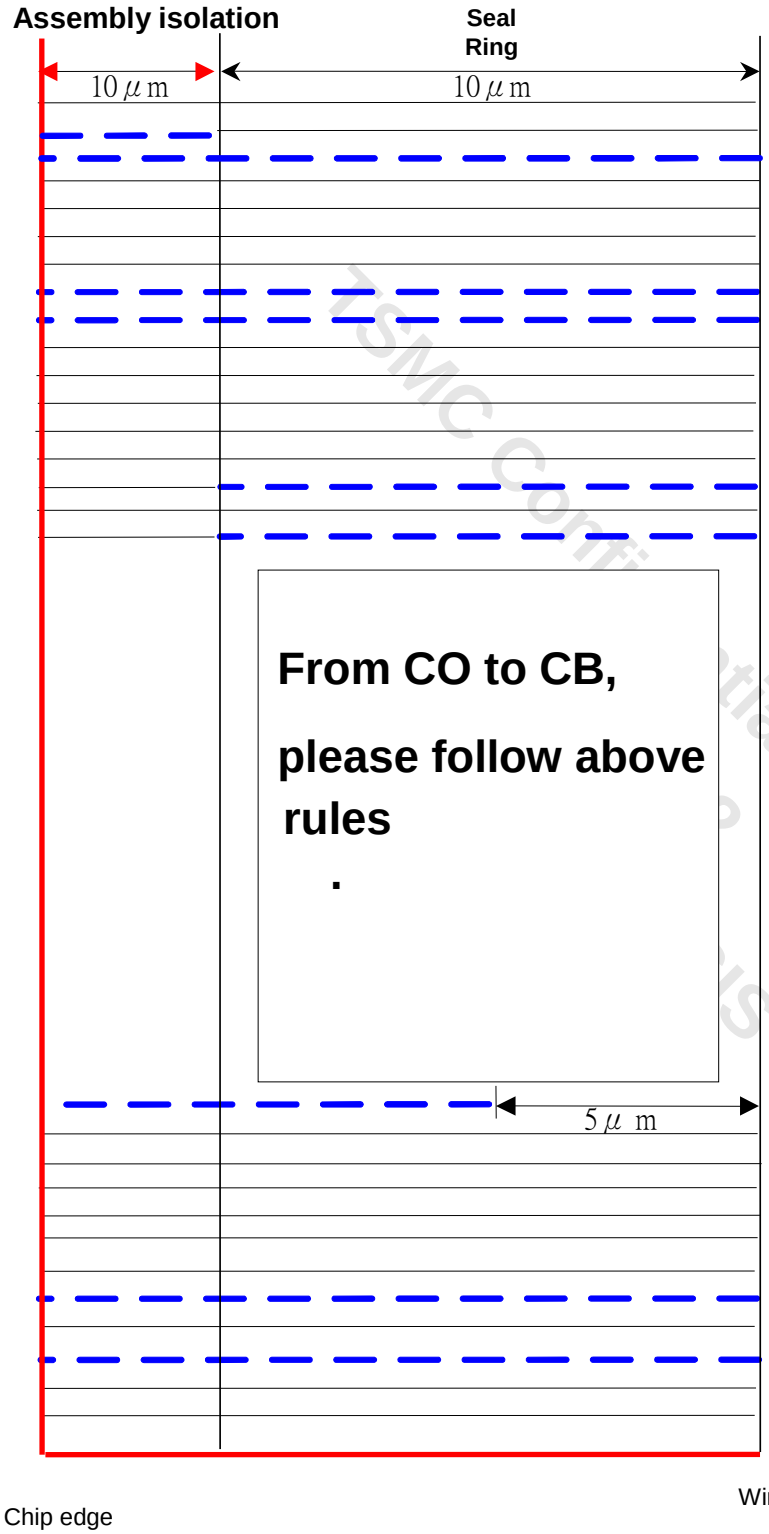
For other layers:

: Digitized area is clear on mask. ——: Digitized area is dark on mask.



Layer	Scribe line tone
DNW (119)	D
OD (120)	D
PW1V (191)	D
NW1V (192)	D
PW2V(193)	D
NW2V (194)	D
VTC_N(112)	D
OD2 (152)	C
Poly (130)	C
N1V (114)	D
P1V (113)	D
N2V (116)	D
P2V (115)	D
NP (198)	D
PP (197)	D
ESD (111)	D
RPO (155)	D
CO (156)	D
M1 (360)	D
VIA1 (378)	D
M2 (380)	D
VIA2 (379)	D
M3 (381)	D
VIA3 (373)	D
M4 (384)	D
VIA4 (374)	D
M5 (385)	D
VIA5 (375)	D
M6 (386)	D
VIA6 (376)	D
M7 (387)	D
VIA7 (377)	D
M8 (388)	D
VIA8 (372)	D
M9(389)	D
CB (107) (306)	D
AP (307) (309)	C
FUSE (30A)	D
PM (009)	D
VTH_P(127)	D
VTH_N(128)	D
VTL_P(117)	D
VTL_N(118)	D
PW1V_DCO (195)	D
NW1V_DCO (19E)	D
OD3 (153)	C
N1V_DCO (106)	D
P1V_DCO (105)	D

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4.5.44.1 WLCSP Seal Ring Layout Rules

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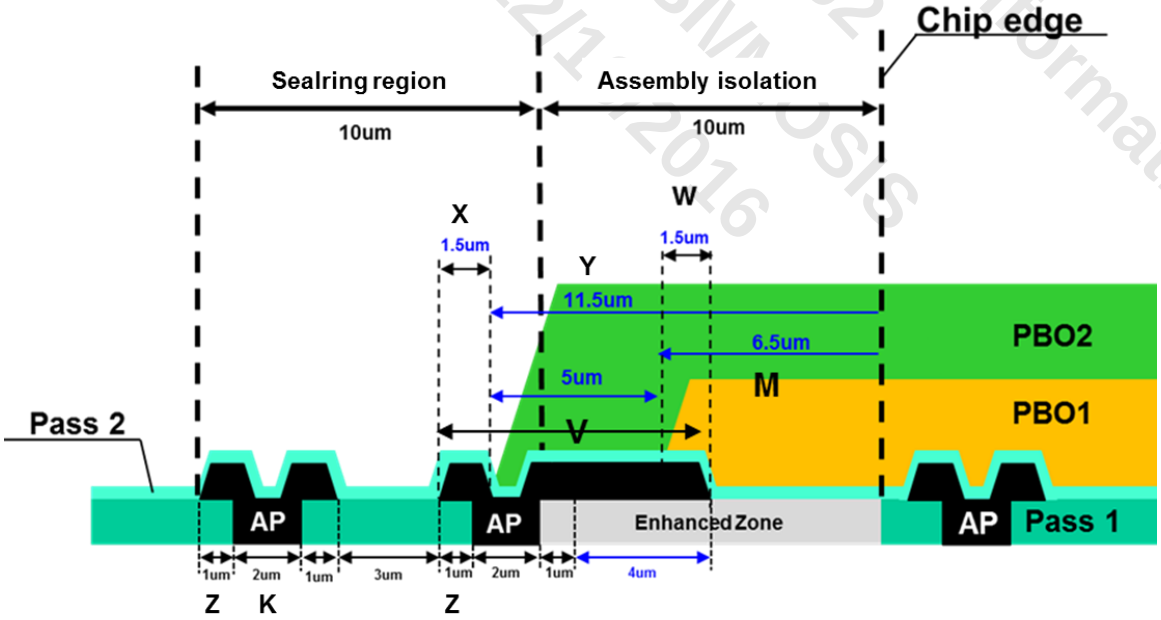
Rule No.	Description	Label		Value
AP.W.4	Width of {AP INTERACT ASSEMBLY ISOLATION } (DRC tolerance at 45 degree turning 0.02 um)	V	>=	8
AP.W.5	Width of {{AP NOT PM1} interact ASSEMBLY ISOLATION} (DRC tolerance at 45 degree turning 0.02 um)	W	>=	1.5
AP.W.6	Width of {AP INTERACT ASSEMBLY ISOLATION AND PM2 } (DRC tolerance at 45 degree turning 0.02 um)	X	=	1.5

Rule No.	Description	Label		Value
AP.EN.3	AP enclosure of CB/CBD/RV in sealring region (DRC tolerance at 45 degree turning 0.02 um)	Z	=	1
CB.W.7	Width of CB/CBD/RV opening inside sealring region (DRC tolerance at 45 degree turning 0.02 um)	K	=	2

Rule No.	Description	Label		Value
PM.R.1	Region of {ASSEMBLY ISOLATION NOT PM1} must abut chip edge			V
PM.W.5	Width of {ASSEMBLY ISOLATION NOT PM1} (DRC tolerance at 45 degree turning 0.02 um)	M	=	6.5
PM.W.6	Width of {SEALRING OR ASSEMBLY ISOLATION NOT PM2 } (DRC tolerance at 45 degree turning 0.02 um)	Y	=	11.5



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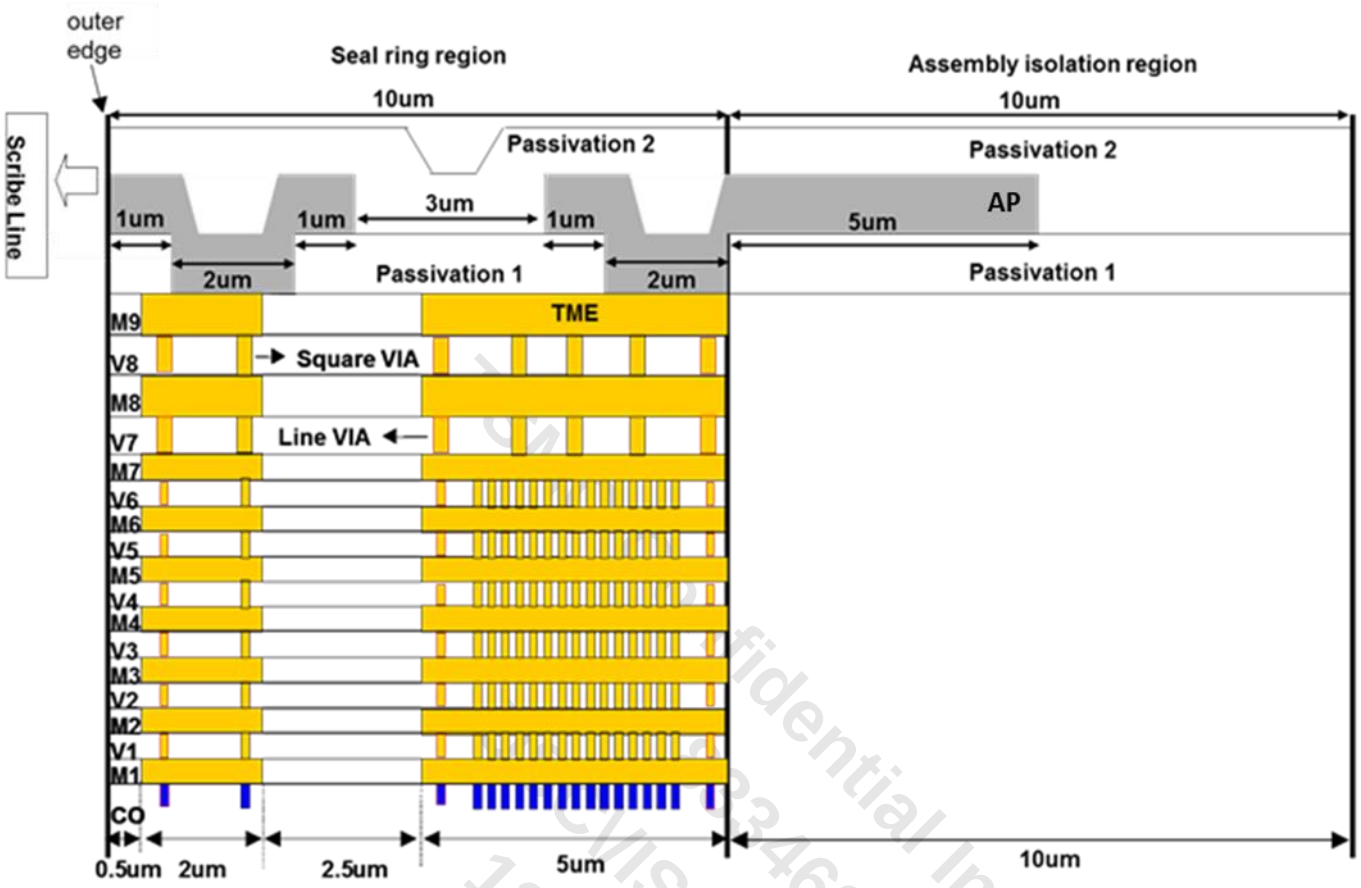
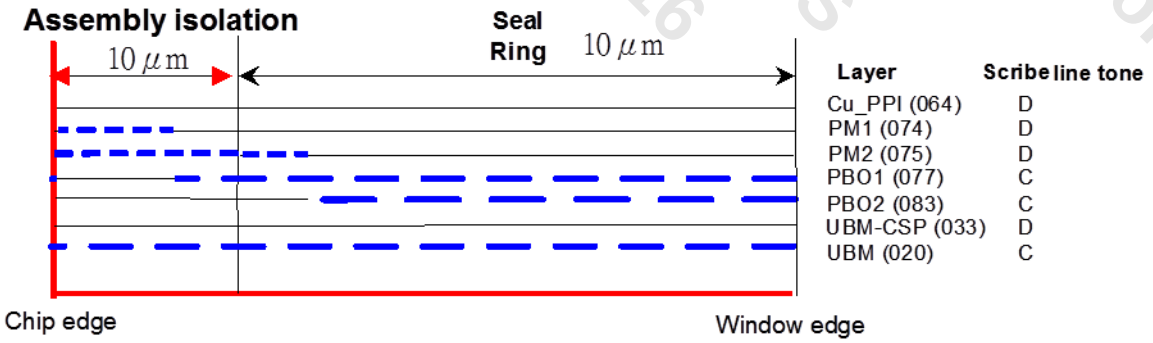


For WLCSP layers:

: Digitized area is clear on mask. : Digitized area is dark on mask.



Layer	Scribe line tone
Cu_PPI (064)	D
PM1 (074)	D
PM2 (075)	D
PBO1 (077)	C
PBO2 (083)	C
UBM-CSP (033)	D
UBM (020)	C

Remark: Please refer the layout of PM to draw PM1.

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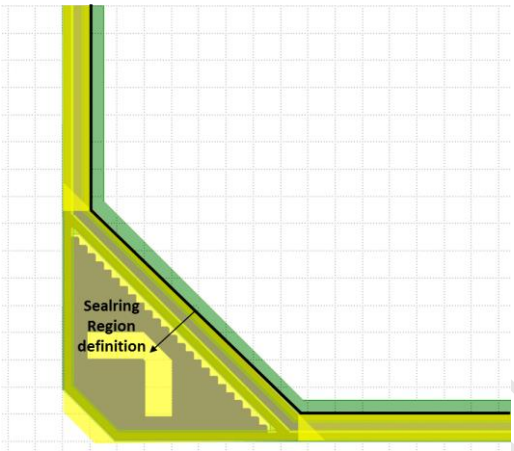

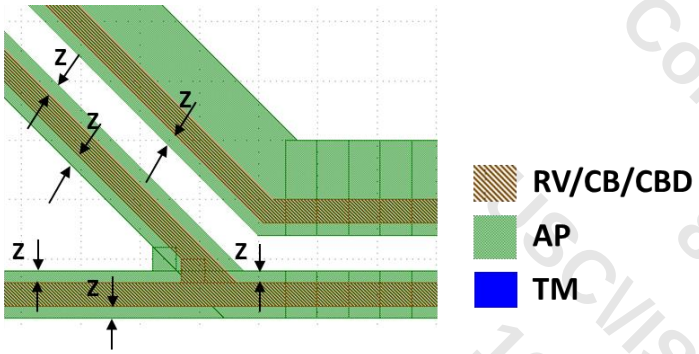

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4.5.45 Sealring CDU (Critical Dimension Uniformity) Rules

1. **CD uniformity**: It is required that you add a CDU pattern in a 10 µm assembly isolation beside a seal ring. The CDU must include OD/Poly/CO/M1/NP with isolated/dense pitches for different proximity monitoring.

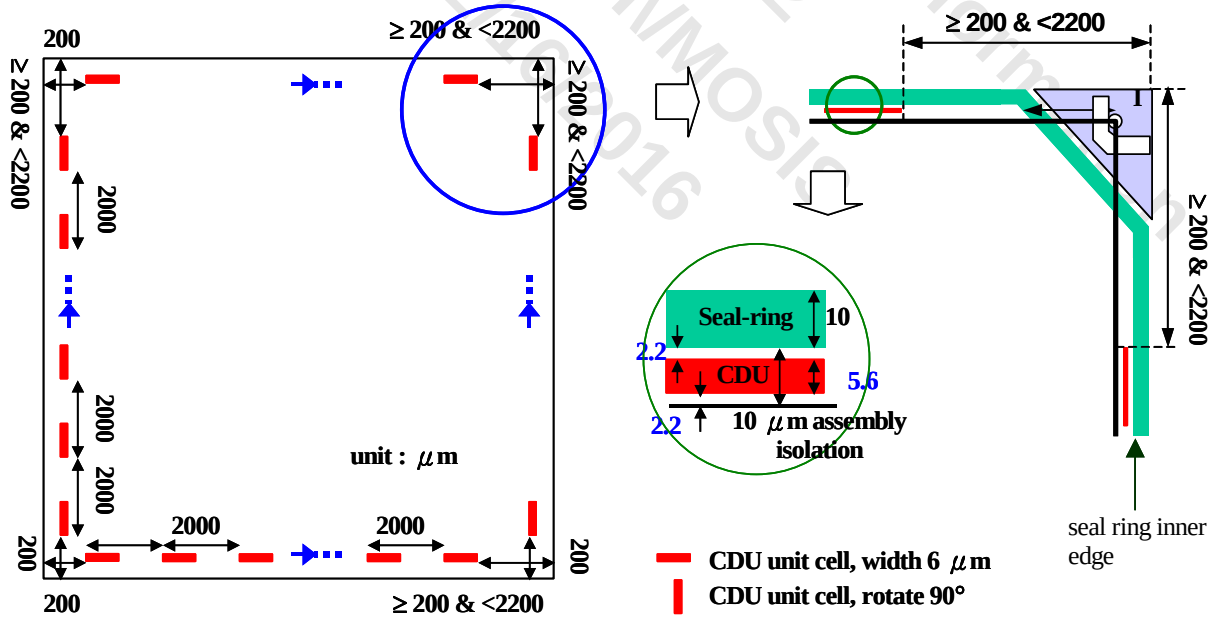
   If you request that TSMC add a chip corner stress relief pattern and seal ring, TSMC will add CDU.

2. **Customer-added CDU**: If you add the stress relief pattern, seal ring, and CDU by yourself, you need to know the following:
   - GDS example: ***same as seal-ring GDS***
   - You need a dummy layer CDUDMY (CAD layer:165) to align to the CDU cell edge.
   - The DRC will only check the CDU rules in the 2 following rules.

Rule No.	Description
CDU.R.1	CDUDMY must be inside the assembly isolation, beside the seal ring.
CDU.R.2	OD/Poly/CO/M1/NP must be inside the CDUDMY.

3. **CDU Clearance:** The assembly isolation must be equal to, or greater than, 10 µm. If the assembly isolation is less than 10 µm, the space is not enough for CDU.

   Example: A CDU cell that is 5.6 µm wide is placed in a chip from the left to the right and from the bottom to the top. This occurs every 2000 µm. The space from the left-bottom edge to the short edge of the first CDU cell is 200 µm. The space from the short edge of the last CDU cell to the top-right edge is greater than, or equal to 200 µm and less than 2200 µm. The space from the CDU long edge to the seal ring inner edge is 2.2 µm.



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4.5.46 Antenna Effect Prevention (A) Layout Rules

A protection OD means diode, STRAP, source, drain and so on.

Rule No.	Description		Ratio	
	Prevention without protection OD (A.R.1~6, 10,11)		In OD2 (GATE AND OD2)	Not in OD2 (GATE NOT OD2)
A.R.1	Drawn ratio of the poly top area to the active poly gate area that is connected directly to it	≤	250	250
A.R.2	Drawn ratio of the poly sidewall area to the active poly gate area that is connected directly to it	≤	500	500
A.R.3	Drawn ratio of the poly contact area to the active poly gate area that is connected directly to it	≤	10	10
A.R.4	Single-layer drawn ratio of a via area to the active poly gate area that is connected directly to it	≤	20	20
A.R.6	Ratio of cumulative metal top area (from M1 to M9) to an active poly gate area	≤	1000 (1.8V IO) 5000(except 1.8V IO)	5000
A.R.9	Ratio of cumulative via area (from V1 to V8) to an active poly gate area	≤	50	
A.R.10	Drawn ratio of RV area to the active poly gate area that is connected directly to it	≤	20	200
A.R.11	Drawn ratio of AP-MD sidewall area to the active poly gate area that is connected directly to it	≤	1000	2000
	Prevention with protection OD (A.R.7~8, 12, 13)			
A.R.7	Drawn ratio of cumulative via area (from Via1 to Via8) to the active poly gate area with a protection OD	≤	OD area x 210 + 900, for cumulative layers	
A.R.8	Drawn ratio of the cumulative metal top area (from M1 to Last Matal-1) to the active poly gate area with a protection OD	≤	OD area x 456 + 43000, for cumulative layers	
		≤	OD area x 8000 + 50000, for last metal alone	
A.R.12	Drawn ratio of RV area to the active poly gate area, when a protection OD with an area larger than, or equal to, 0.06 μm2 (0.2 μm X 0.3 μm) is used	≤	OD area x 83 + 400	
A.R.13	Drawn ratio of AP-MD sidewall area to the active poly gate area, when a protection OD with an area larger than, or equal to, 0.06 μm2 (0.2 μm X 0.3 μm) is used	≤	OD area x 8000 + 30000	

Table Notes:

1. It is recommended to have OD connection to the poly gate through metal lines for all devices.
2. All N+ OD and P+ OD areas connected to metal or via do contribute to the OD area. (Including source or drain diffusion of MOSFET and Strap areas)
3. If a large OD is needed, it is recommended to have one big diffusion area with multiple contacts. Avoid covering the entire diode area with metal.
4. Gate poly thickness is 1000 angstrom (Å) for both core and I/O gates.
5. For all of the protection ODs in the same net, if the summation of their areas is larger than 0.06 μm^2, they can be treated as effective protection ODs against plasma charging.
6. In order to avoid the antenna ratio mismatch between the paired devices, metal lines need to be as symmetry as possible.
7. The transistors in mismatch sensitive configurations shall be tied to an active region by M1 to prevent process- induced damage.

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8. When an error is detected at DRC, antenna ratio can be reduced by the following suggestion; connect the node to a protection OD, connect the gate to the highest metal level as close to the gate as possible, or connect the node to the output of the driver with a lower metal level.
9. DRC implementation for calculations of metal to gate area ratio in cumulative antenna rules,
   - "Cumulated Ratio" of A.R.4 and A.R.6 rules is defined as:
     Area(Mx(n))/Area(GATE(n)) + Area(Mx-1(n-1))/Area(GATE(n-1)) + ... + Area(M1(1))/Area(GATE(1))
     - Where GATE(n) is the total GATE area in a particular net constructed by the increment connections up to current n^{th} stage.
     - Mx(n) is the whole area of metal x (x = 1~ top) in the same net.
   - Definition of the protection OD for antenna rules:
     Total area of (OD NOT POLY) INTERACT CONTACT on the same net
10. Failure Criterion
    - Tailing percentage of 20% changes in gate current in Log-normal distribution (which is expressed with the following equation) is less than 5%.

$$\Delta \mathrm{Ig}(\%) \equiv \left| \frac{\mathrm{Ig(n)} - \mathrm{Ig(n-1)}}{\mathrm{Ig(n-1)}} \right| \times 100\%$$

4.5.46.1 Poly Antenna Ratio

The definition of the **poly top area antenna ratio** for each layer is:

ratio = (Lp x Ld + Lpe x Wpe) / (Wd x Ld)

The definition of the **poly sidewall area antenna ratio** for each layer is:

ratio = 2 x [(Lpe +Wpe + Lp) x t] / (Wd x Ld)

- Lp: length of field poly connected to gate
- Wp: width of field poly connected to gate
- Lpe: length of field poly extension connected to gate
- Wpe: width of field poly extension connected to gate
- t: poly thickness
- Wd: transistor channel width
- Ld: transistor channel length

4.5.46.2 M1-M9 Antenn Ratio

The definition of the M1-M9 antenna ratio for each layer is:

ratio = (Wm x Lm) / (Wd x Ld)

- Lm: length of metal line connected to gate
- Wm: width of metal line connected to gate
- Wd: transistor channel width
- Ld: transistor channel length

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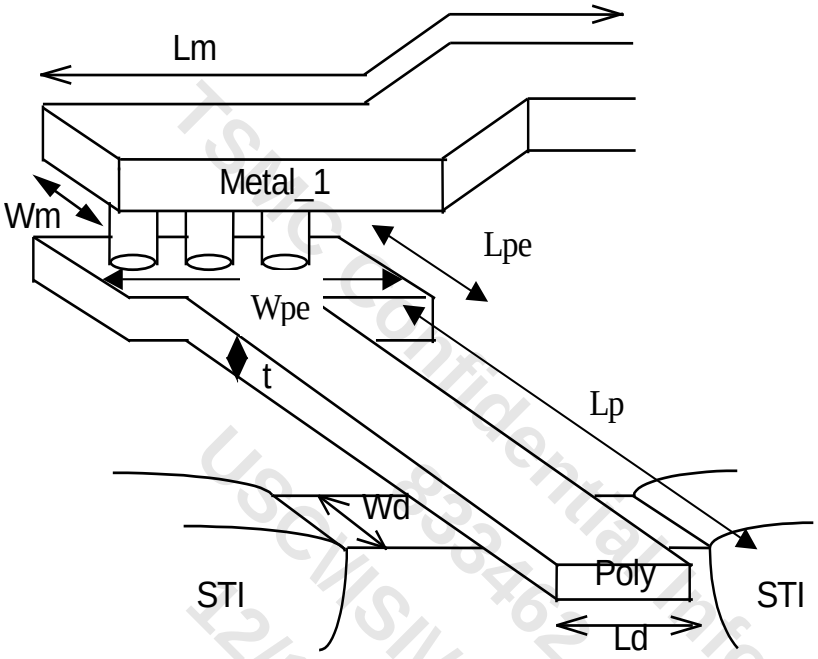
4.5.46.3 CO Via1 – Via8 Antenna Ratio

The definition of CO, VIA1-VIA7 antenna ratio is:

ratio = {total contact (via) area}/ Wd x Ld

Wd: transistor channel width

Ld: transistor channel length



4.5.46.4 AP-MD Antenna Ratio

The definition of the AP-MD antenna ratio is:

ratio = 2 x [(Wm + Lm) x t1] / (Wd x Ld)

Lm: length of metal line connected to gate

Wm: width of metal line connected to gate

t1: thickness of metal line connected to gate

Wd: transistor channel width

Ld: transistor channel length

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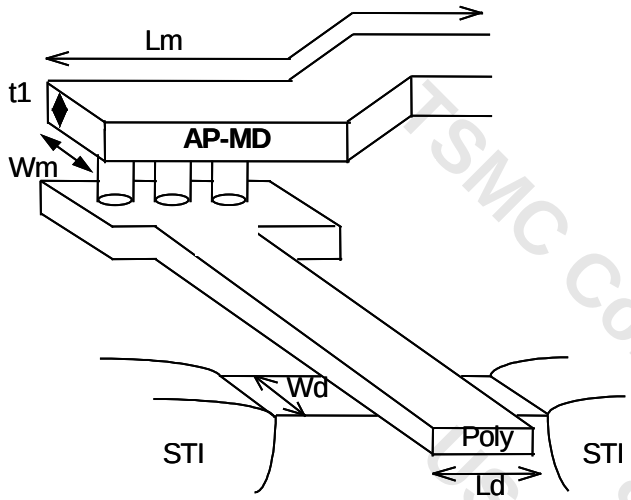
4.5.46.5 RV (Passivation-1 VIA Hole) Antenna Ratio

The definition of RV antenna ratio is:

ratio = {total RV area}/ Wd x Ld

Wd: transistor channel width

Ld: transistor channel length



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4.6 CMN65 (Mixed Signal, RF) Layout Rules and Guidelines

4.6.1 Capacitor Top Metal (CTM) Layout Rules (Mask ID: 182)

The MiM capacitance is defined by the CTM and CBM area. Individual CTM or CBM (i.e, dummy CTM or CBM) is not allowed. It is important to define the correct CAD layer name for the different capacitor application in the following table.

CTMDMY	148;0	Dummy marker layer for MIM capacitor. Use for DRC. Its size is equal to CBM layer sizes up +10 µm per side.
CTMDMY	148;110	Dummy marker layer for MIM capacitor 1.0fF/um^2. Use for DRC. Its size is equal to CBM layer sizes up +10 µm per side.
CTMDMY	148;115	Dummy marker layer for MIM capacitor 1.5fF/um^2. Use for DRC. Its size is equal to CBM layer sizes up +10 µm per side.
CTMDMY	148;120	Dummy marker layer for MIM capacitor 2.0fF/um^2. Use for DRC. Its size is equal to CBM layer sizes up+10 µm per side.

Rule No.	Description	Label		Rule
CTM.W.1	Width	A	≥	2
CTM.W.2	Maximum length and width For example, 10 µm x 101 µm CTM is not allowed.	A1	≤	100
CTM.S.1	Space	B	≥	0.8
CTM.EN.1	Enclosure by CBM (CTM must be fully inside CBM).	E	≥	0.4
CTM.R.1	The different unit capacitance can't co-exist on same product.			
CTM.R.2	It is prohibitive to have My, VIAy, Mr, and VIAr in your MIM design.			
CTM.R.3*	CTM/ CBM are not allowed in N55 technology. DRC will flag CTM layer.			

*: The MIM capacitance is not offered N55 generation.

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4.6.2 Capacitor Bottom Metal (CBM) Layout Rules (Mask ID: 183)

Rule No.	Description	Label		Rule
CBM.W.1	Width	C	≥	2.8
CBM.W.2	Maximum length and width For example, 10 µm x 211 µm CBM is not allowed.	C_1	≤	210
CBM.S.1	Space (For CTMDMY area ≤ 40,000 µm^2)	D	≥	2.0
CBM.S.2	Space (For CTMDMY area > 40,000 µm^2)	D1	≥	2.6
CBM.S.3	Space to the top Mx	F	≥	0.5
CBM.EN.2	CTMDMY is equal to CBM layer sizing up 10 µm for each side. DRC checking layer (CTMDMY, GDS layer 148) is needed to specify the MIM capacitor region; special Mz or Mu and VIAz/VIAu design rules will be defined inside this area	G	=	10
CBM.R.1	The top Mx layer (including the top dummy Mx) interacting with CBM is not allowed. (Mx pattern density rule check will exclude CTMDMY region; the other density rules for metal layers must still comply with the *Logic Design Rule Manual)*			
CBM.R.2g^U	Circuits under MIM are allowed from process point of view. But the parasitic and signal coupling effects should be considered by designers. It is recommended to add metal shielding between MIM capacitor and underneath routing or circuits. One can refer to section 4.6.3 for circuit under MIM layout options.			
Mx.DN.6	It is not allowed to have local density < 15% of all 3 consecutive metal (Mx, Mx+1 and Mx+2) under ((CBM SIZEING 25) SIZING -25) whose size is >= 200um X 200um			
Mx.R.3g^U	It's recommended to use 1) PDK cell with metal shielding option, 2) Don't put a lot of MIM together, 3) To design small MIM region to meet Mx.DN.1 and Mx.DN.4.			

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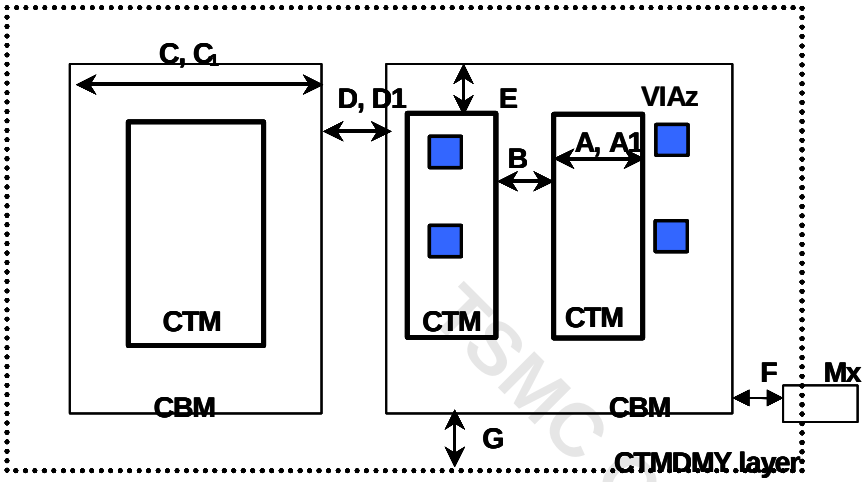
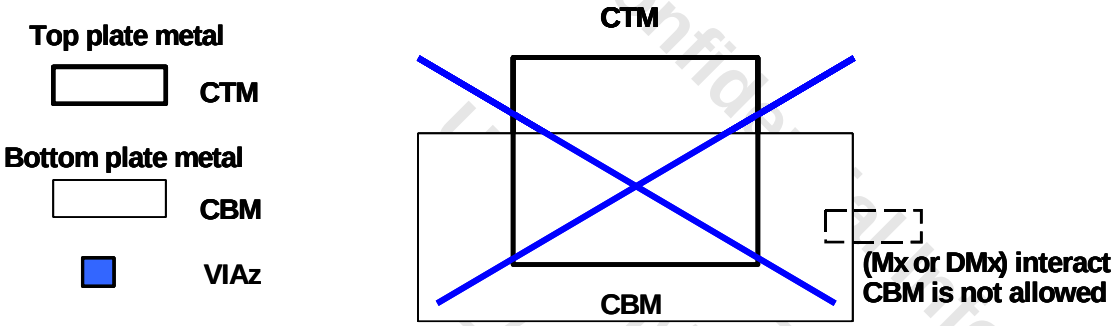
CTM and CBM





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4.6.3 MIM Capacitor PDK Guidelines

The TSMC offered MIM spice model includes both RF and BB (base band) model, the user guideline of the model are shown as following for better product yield, performance to achieve mixed-signal and RF circuit design:

- The offered MIM model has 3T (three terminals) and 2T types. In the 3T case, the terminals are CTM, CBM and ground terminal. In the 2T case, the terminals are CTM and CBM only.
- In the 3T case, it offers MIM with metal shielding layers and without metal shielding layers.
- The with shield MIM and without shield MIM both include RF and BB models respectively.
- In order to keep the offered model accuracy, the model type of MIM device is defined by “start” and “end” layers. Users cannot draw/generate any metal routing or dummy metal into the region between the start and end layer region. The dummy exclusion layers (EXCL) are used in the MIM layout to ensure this region dummy patterns clean. The size of used exclusion layers is equal to the size of CBM region.

The following table is the coverage of tsmc CMN65 for RF SPICE model and PDK offerings

MIM combination/ Coverage Function		MIM			Inductor		
		Spice	PDK	Process	Spice	PDK	Process
1	Mx+MIM+Mz+Mu (A)	O	O	O	O	O	O
2	Mx+MIM+Mz+Mz (B)	O	O	O	O	O	O
3	Mx+MIM+Mu (C)	O	O	O	O	O	O
4	Mx+MIM+Mz (D)	O	O	O	O	O	O
O : available X : not available (Mx:2.2 KÅ, Mz:9KÅ, Mu:34KÅ)							

The following is the illustration of model covering range for different MIM type.

Model type				Spice name	Model start layer	Model end layer
3T	w/i shield	RF	Type-a	mimcap_um_sin_rf	Mx,top-2	Mz or Mu
		BB	Type-b	NA	Mx,top-2	CTM
	w/o shield	RF	Type-c	mimcap_woum_sin_rf	Substrate	Mz or Mu
		BB	Type-d	mimcap_sin_3t	Substrate	CTM
2T			Type-e	mimcap_sin	CBM	CTM

Mx layer (including dummy Mx) interacting with CBM are not allowed (CBM.R.2). The special attention below are needed for the five MIM model types to enable MS/RF circuit design:

1. Type-a and Type-b allow metal routing under the shielding metal layers.
2. Type-c and type-d do not allow metal routing under Mx region. In the without shield MIM type (type-c and type-d), the substrate can be flexible such as: NW, PW, DNW or NTN.
3. Type-e allows metal routing under the Mx layer.

Type-a. In the RF 3T with shield MIM type, the model constructs from shield metal layer (Mx,top-2) to end layer at Mz (1P8M) or Mz (1P9M) or Mu (if Mu used). Under the shield metal layers of MIM, metal routing is allowed, but metal routing above the end layer is not allowed.

Type-b. In the BB 3T with shield MIM type, the model constructs from shield inter metal layer (Mx,top-2) to end at CTM layer. Metal routing under the shield metal layers or above the CTM layer is allowed.

Type-c. In the RF 3T without shield MIM type, the model constructs from substrate to end layer at Mz (1P9M) or Mz (1P9M) or Mu (if Mu used). Between the start and end layer region, user cannot draw any metal routing or dummy metal to keep model accuracy.

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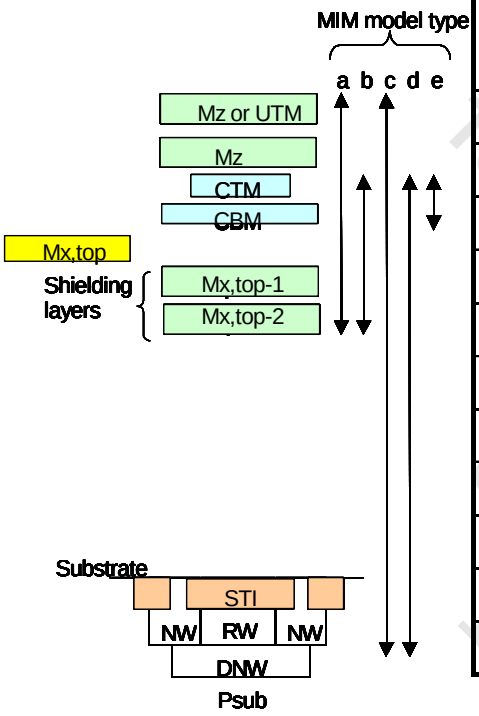
Type-d. In the BB 3T without shield MIM type, the model constructs from substrate to end at CTM layer. Between the start and end layer region, user cannot draw any metal routing or dummy metal. Above the CTM layer, the metal routing is allowed.

Type-e. In the 2T MIM type, the model constructs from CBM to end at CTM layer. Metal routing under the Mcap-1 layer or above the CTM layer is allowed.



Layer	EXCL layer	Type-a	Type-b	Type-c	Type-d	Type-e
		RF-3T-w/i-shield	BB-3T-w/i-shield	RF-3T-w/o-shield	BB-3T-w/o-shield	BB-2T
M9	(150;9)	O		O		
M8	(150;8)	O		O		
M7	(150;7)	O	O	O	O	O
M6	(150;6)	O	O	O	O	
M5	(150;5)	O	O	O	O	
M4	(150;4)			O	O	
M3	(150;3)			O	O	
M2	(150;2)			O	O	
M1	(150;1)			O	O	
Poly	(150;21)			O	O	
OD	(150;20)			O	O	

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4.6.4 VIAz and VIAu Layout Rule for MIM Capacitor and Mu

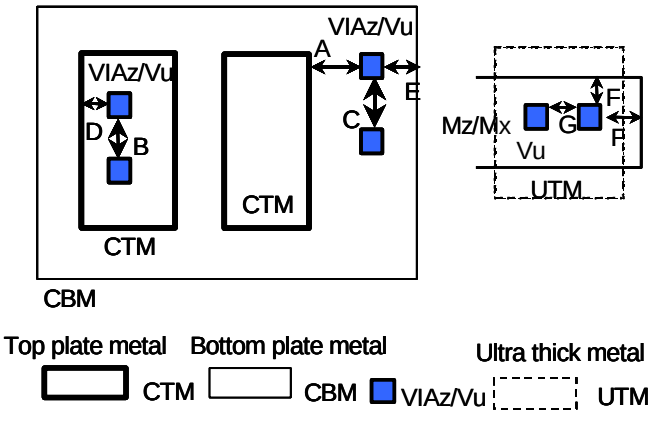
In this section, VIAz/VIAu layer is the top VIA (size=0.36um) above CTM or CBM capacitors. Except to follow the VIAz rules in the section 4.5, you also need to meet the following specific rules are related to the MIM or Mu connection.

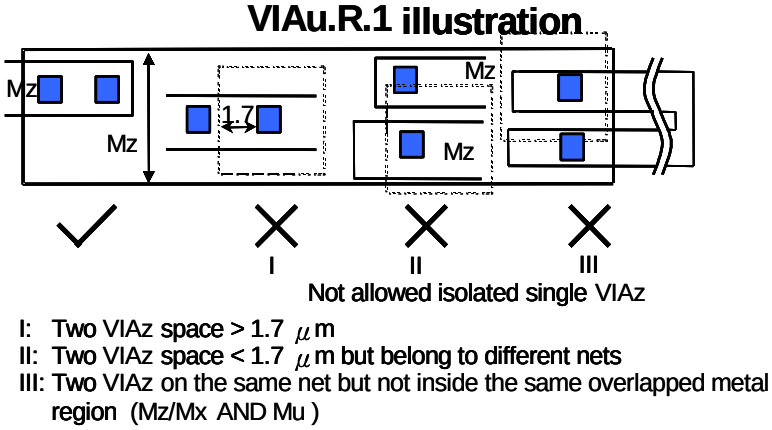
4.6.4.1 VIAz(u) Layout Rule (Mask ID: 373, 374, 375, 376, 377, 372) for CTM/CBM

Rule No.	Description	Label		Rule
VIAz(u).EN.3	Enclosure by CTM (cut is not allowed)	D	≥	0.24
VIAz(u).EN.4	Enclosure by CBM (cut is not allowed)	E	≥	0.20
VIAz(u).S.3	[VIAz(u) inside CBM but outside CTM] space to CTM	A	≥	0.30
VIAz(u).S.4	Space of VIAz(u) inside CTM.	C	≥	0.54
VIAz(u).S.5	Space of VIAz(u) inside CBM	B	≥	0.54
VIAz(u).R.6g[U]	For MIM application, please put as many VIAz(u) as possible for both CTM and CBM connections.			
VIAz(u).R.7	Single VIAz(u) for in a CTM or [CBM NOT CTM] or connect to (the top Mx layer inside CTMDMY*) is not allowed.			

4.6.4.2 VIAu Layout (Mask ID: 373, 374, 375, 376, 377, 372) Rule for Mu

Rule No.	Description	Label		Rule
VIAu.EN.5	[VIAu inside Mu] enclosure by [Mz or Mx] .	F	≥	0.08
VIAu.R.8	At least two [VIAu under Mu], with space (G) ≤ 1.7 μm, are required to connect [Mx or Mz] and Mu. One via for Mu or connect to (the top Mx layer inside CTMDMY) is not allowed.	G	≤	1.7





I: Two VIAz space > 1.7 μm
II: Two VIAz space < 1.7 μm but belong to different nets
III: Two VIAz on the same net but not inside the same overlapped metal region (Mz/Mx AND Mu)

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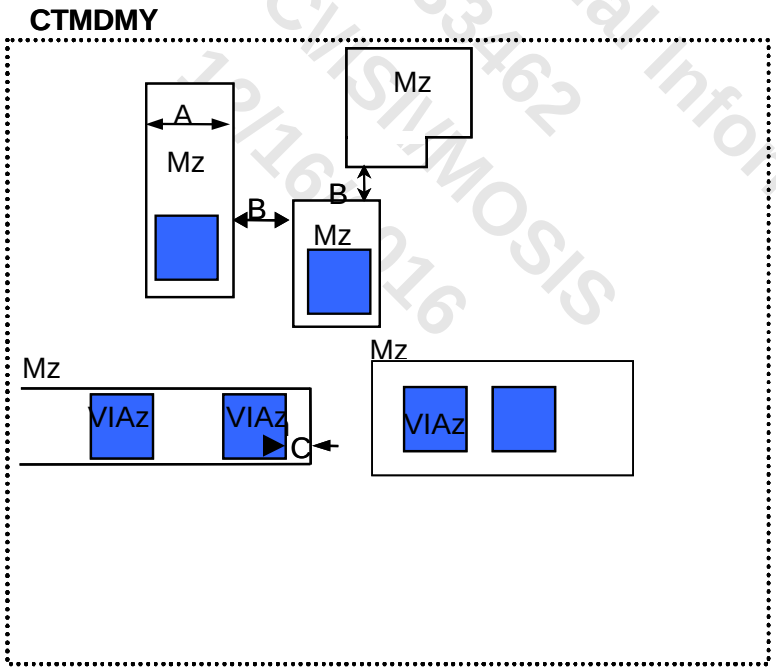
4.6.5 Mz Layout Rule (Mask ID: 384, 385, 386, 387, 388, 389) for MIM Capacitor

Mz layer means the first metal layer above the MIM capacitor and connect to CTM or CBM. Except to follow the Mz (4XTM) rules in the section 4.5, you also need to meet the following specific rules which are related to the MIM.

Rule No.	Description	Label		Rule
Mz.EN.3	Mz [1st metal above MIM capacitor connect to CTM or CBM] enclosure of [VIAz inside CTMDMY] inside CTMDMY*.	C	≥	0.10
Mz.DN.5	Mz [1st metal above MIM capacitor connect to CTM or CBM] density range inside a CTMDMY* [the overlapped area of {checking window AND CTMDMY}≥ 2500μm^2] Note: TSMC PDK cells have taken this rule into layout consideration. If you do not use TSMC PDK cells, please pay attention on the Mz layout while you design the MM_RF device.		≥ ≤	50% by 200x200 80% by 100x100
Mz.W.4	Width of Mz [1st metal above MIM capacitor connect to CTM or CBM] inside CTMDMY	A	≥	0.84
Mz.S.4	Space of Mz [1st metal above MIM capacitor connect to CTM or CBM] inside CTMDMY	B	≥	0.84

Rules for Mz and VIAz inside a CTMDMY



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4.6.6 Antenna Effect Prevention Design Rules for MIM Capacitor

4.6.6.1 MIM structures with the Antenna Effect

The antenna effect should be taken into consideration for the MIM capacitor design. The layout style of the MIM capacitor routing will impact its immunity to antenna effect during fab process. Antenna rules are defined separately for the following metallization options:

Table 4.6.6.1 Metallization Options for Metal Layers above MIM

Metallization Options	Metal Layers above MIM			
	1st Mz	2nd Mz	Mu	AP-MD
A	V			
B			V	
C	V	V		
D	V		V	
E	V			V
F			V	V
G	V	V		V
H	V		V	V

4.6.6.1.1 Terminology

- "**Floating**" defines as below:

  CTM or CBM node is not connected to any OD or poly gate region.

- "**Grounded**" defines as below:

  CTM or CBM node is connected to OD region.

- **"Balanced structures"** defines as below:

  Both CTM and CBM nodes are floating or connected to ground (including protection OD) through the same metal path (i.e. Mz, Mu or AP-MD) after MIM structure is formed. Please refer to Fig 4.6.6.1.1.

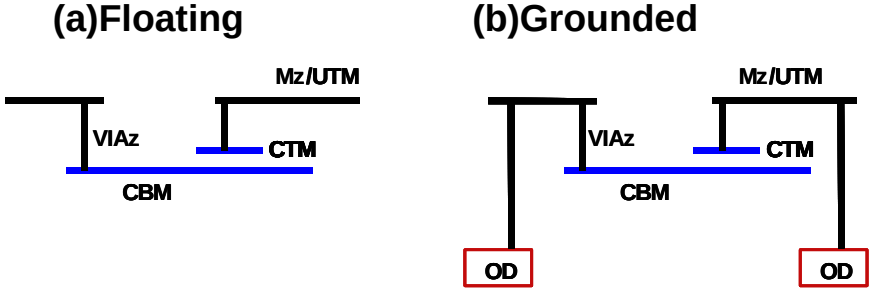

Fig.4.6.6.1.1 Examples of balanced structures

- **"Unbalanced structures"** defines as below:
  - If one node of the MIM capacitor is connected to OD or poly gate, but the other node is not connected to OD at the same metal layer. Please refer to Fig 4.6.6.1.2.
  - If any node of the MIM capacitor is connected to gate but without protection OD.
  - Unbalanced structures are not allowed.

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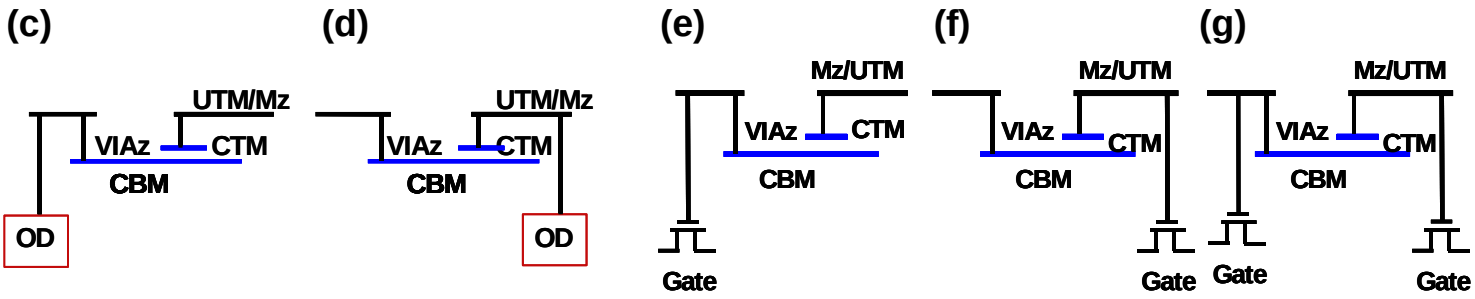

Fig. 4.6.6.1.2 Examples of unbalanced structures

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4.6.6.1.2 MIM Structure Recognition Methodology

Below tables are for clear definition of balanced & unbalanced MIM structure.
A, B: Two terminals of MIM
All structure = balanced (float) + balanced (OD) + unbalanced
Unbalanced (A-OD): Unbalanced structure. Terminal A connected to OD and terminal B not connected to OD.
Unbalanced (B-OD): Unbalanced structure. Terminal B connected to OD and terminal A not connected to OD.

Table 4.6.6.1.2.1 One metal layer above MIM

1st A, B	1st metal Structure	In TSMC
Both A, B floating	Balanced (float)	**Allowed**
Both A, B connect to OD	Balanced (OD)	**Allowed**
Other combinations		**Not allowed**

Table 4.6.6.1.2.2 Two metal layers above MIM

1st A,B	2nd A,B	2nd metal Structure	In TSMC
Balanced (float)	Balanced (float)	Balanced	**Allowed**
Balanced (float)	Balanced (OD)	Balanced	**Allowed**
Balanced (OD)	All structures	Balanced	**Allowed**
Other combinations			**Not allowed**

Table 4.6.6.1.2.3 Three metal layers above MIM

1st A,B	2nd A,B	3rd A,B	3rd metal Structure	In TSMC
Balanced(OD)	All structure	All structure	Balanced	**Allowed**
Balanced(float)	Balanced(float)	Balanced(float)	Balanced	**Allowed**
Balanced(float)	Balanced(float)	Balanced(OD)	Balanced	**Allowed**
Balanced(float)	Balanced(OD)	All structure	Balanced	**Allowed**
Other combinations				**Not allowed**

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4.6.6.1.3 Check Methods:

- If there is only one Metal (Mz or Mu) above the MIM capacitor:

  Refer to Fig. 4.6.6.1.1 and Fig. 4.6.6.1.2 to check MIM structure is balanced or unbalanced.

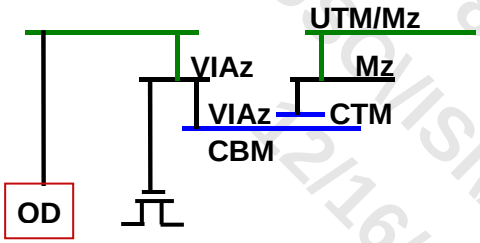
- If there are at least two Metal layers (Table 4.6.6.1 option C~H) above the MIM capacitor:

  1. Each metal layers above MIM capacitor must follow the antenna rule. (Please refer to section 4.6.6.2).
  2. DRC first check the 1st metal layer right above the MIM capacitor. It is the same as only one Metal above the MIM capacitor.
  3. Then DRC following check the 2nd metal layer above the MIM capacitor (for two or more metal layers above MIM capacitor use):

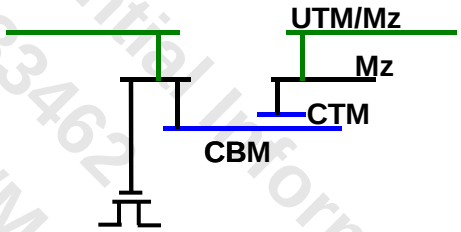
     3-1. If the 1st metal layer above the MIM capacitor is balanced, then to check the 2nd metal scheme.

     3-2. If the 1st metal layer above the MIM capacitor is unbalanced, it needs to check the all metal schemes above MIM capacitor as below, then to judge whether the 2nd metal layer is balanced or unbalanced. But unbalanced structures are not allowed.

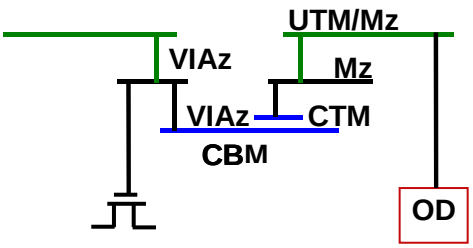
(h)Unbalanced



(i)Unbalanced

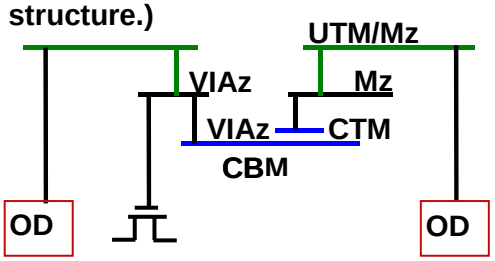


(j)Unbalanced



(k) Unbalanced

(But 1st Mz above MIM capacitor is unbalanced structure. It is not allowed to use unbalanced structure.)



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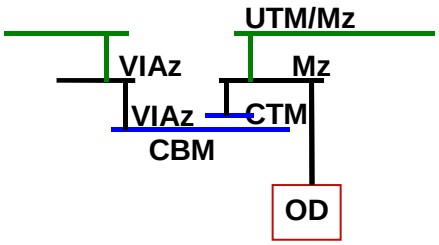
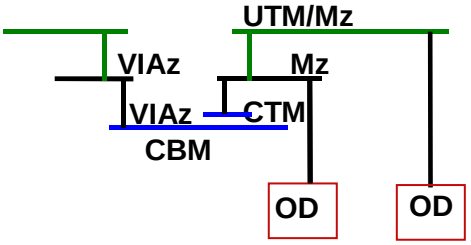
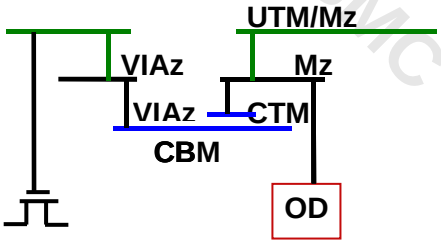
(l)Unbalanced



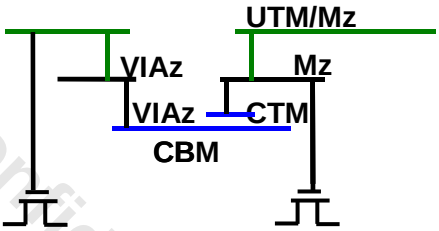
(m)Unbalanced



(n)Unbalanced

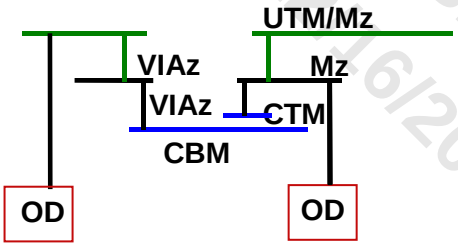


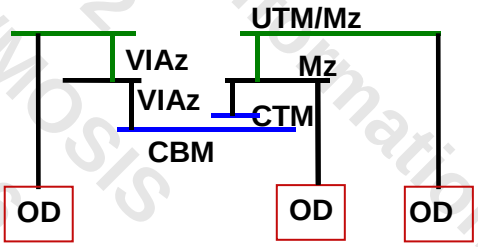
(o)Unbalanced



(p)Unbalanced **(q)Unbalanced**

(But 1st Mz above MIM capacitor is unbalanced structure. It is not allowed to use unbalanced structure for picture p and q.)





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4.6.6.2 Antenna Effect Prevention Layout Rules

The rules are for the metal layers and VIA layers above the CTM and CBM as in Table 4.6.6.1. Take 1P9M where M9 is Mu as an example, the antenna effect of VIA7 / M8 / VIA8 / M9 to the MIM capacitors needs to be considered.

Rule No.	**Description**		**Antenna Ratio**	
			CTM Node	CBM Node
A.R.MIM.1	Unbalanced structure is not allowed.			
A.R.MIM.2	Maximum ratio of the cumulative metal area and AP-MD sidewall area to the MIM capacitor for balanced structure when both CTM and CBM are floating.	≦	1000	1000
A.R.MIM.3	Maximum ratio of the cumulative metal area and AP-MD sidewall area to the MIM capacitor for balanced structure when both CTM and CBM are connected to OD.	≦	OD area x 8000 + 1000	
A.R.MIM.4	Maximum ratio of the cumulative VIA and RV area to the MIM capacitor for balanced structure when both CTM and CBM are floating.	≦	20	20
A.R.MIM.5	Maximum ratio of the cumulative VIA and RV area to the MIM capacitor for balanced structure when both CTM and CBM are connected to OD.	≦	OD area x 210 + 20	

Definition of Antenna Ratio

Different antenna ratio formulas are defined for Cu and AP-MD due to the process differences.

Metal Layer	MIM node	Drawn Ratio Formula	Definition
Cu Antenna (Mz, Mu, MD)	CTM node	(L1 x W1) / (W2 x L2)	L1: metal length connected to CTM W1: metal width connected to CTM W2: connected CTM width L2: connected CTM length
	CBM node	(L1 x W1) / (W2 x L2)	L1: metal length connected to CBM W1 : metal width connected to CBM W2 : connected CTM width L2 : connected CTM length
VIA Antenna	CTM node	{ total VIA area } / (W2 x L2)	total VIA area connected to CTM W2: connected CTM width L2 : connected CTM length
	CBM node	{ total VIA area } / (W2 x L2)	total VIA area connected to CBM W2 : connected CTM width L2 : connected CTM length
AP-MD Antenna	CTM node	2 [(L1 +W1) x t] / (W2 x L2)	L1: metal length connected to CTM W1 : metal width connected to CTM t : metal thickness of AP-MD W2: connected CTM width L2 : connected CTM length
	CBM node	2 [(L1 +W1) x t] / (W2 x L2)	L1: metal length connected to CBM W1 : metal width connected to CBM t : metal thickness of AP-MD W2: connected CTM width L2 : connected CTM length
RV Antenna	CTM node	{ total RV area } / (W2 x L2)	total RV area connected to CTM W2 : connected CTM width L2 : connected CTM length
	CBM node	{ total RV area } / (W2 x L2)	total RV area connected to CBM W2 : connected CTM width L2 : connected CTM length

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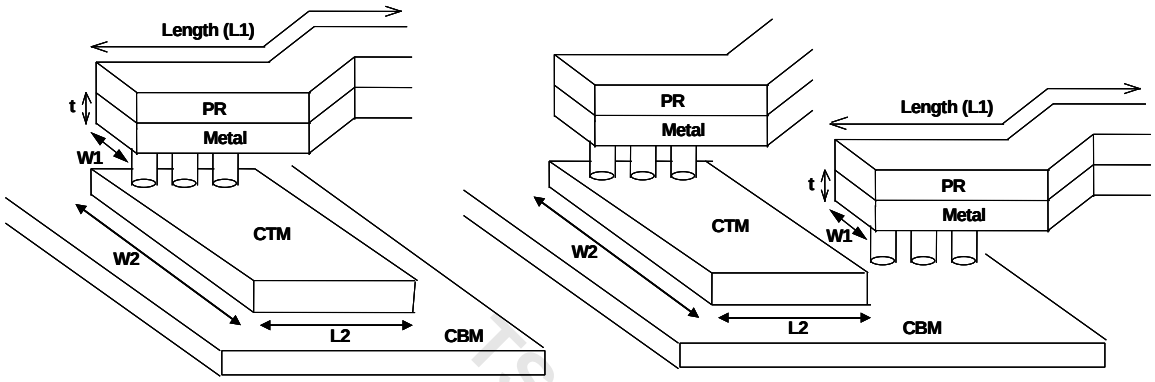

CTM Node **CBM Node**

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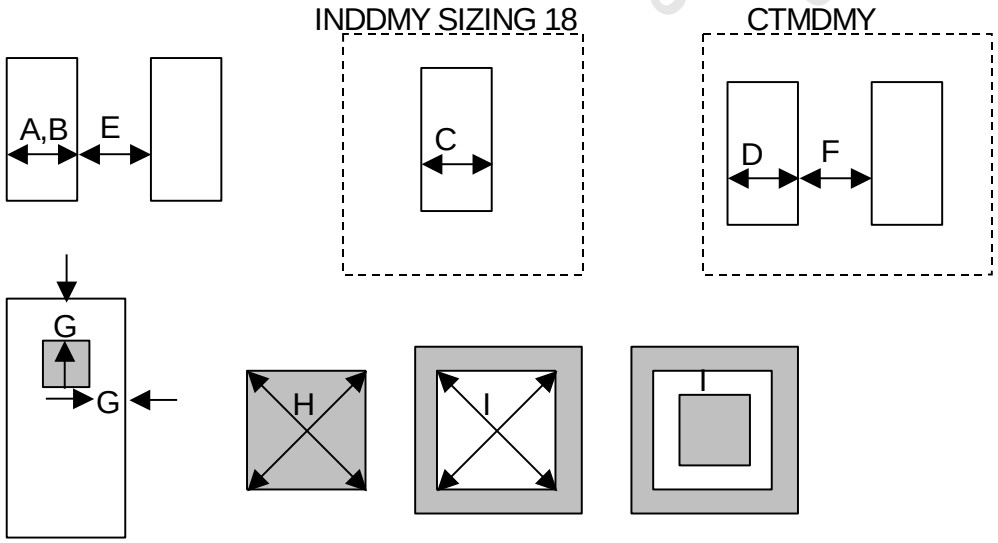
4.6.7 Ultra Thick Metal (Mu) Layout Rules (Mask ID: 384, 385, 386, 387, 388, 389)

Mu (34KÅ) and Mz (9 KÅ) can not co-exist on the same metal layer.

Rule No.	Description	Label		Rule
Mu.W.1	Width	A	≥	2
Mu.W.2	Maximum width [outside (INDDMY SIZING 18 µm) and (except bond pad)]	B	≤	12
Mu.W.3	Maximum width [inside (INDDMY SIZING 18 µm)] for inductor application only.	C	≤	30
Mu.S.1	Space	E	≥	2
Mu.EN.1	Enclosure of VIAu	G	≥	0.3
Mu.A.1	Area	H	≥	9
Mu.A.2	Enclosed area	I	≥	9
Mu.R.2^{U}	Mu line-end must be rectangular. Other shapes are not allowed.			
Mu.DN.1	Mu metal density over the whole chip (include INDDMY)		≥	20%
			≤	70%
Mu.DN.2	Mu density range in whole chip.		≥	10% in 75x75
			≤	80% in 100x100
Mu.DN.3	Mu [1st metal above MIM capacitor connect to CTM or CBM] density range inside a CTMDMY* [the overlapped area of {checking window AND CTMDMY}≥ 2500µm^2] Note: TSMC PDK cells have taken this rule into layout consideration. If you do not use TSMC PDK cells, please pay attention on the Mu layout while you design the MM_RF device.		≥	50% by 200x200
			≤	80% by 100x100



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4.6.8 INDDMY Rule Overview

TSMC offered 3 kinds of INDDMY rule options according to different device/circuit applications. But TSMC only provided a specific inductor device SPICE model /PDK for Low-density INDDMY design.

Different INDDMY dummy layers are defined to recognize the three types inductors: Low-density, Medium-density and High-density. In order to have a correct DRC check, you need to draw the corresponding INDDMY (144;x) carefully. Please refer section 3.4 for detailed INDDMY layer definitions.

1. Low-density INDDMY (INDDMY): INDDMY is offered to allow very low metal density within an inductor to achieve better inductor performance. Except the Mx layer directly below [Mz or Mu], any other inter-metal layer (Mx), inter-via (Vx) and DOD/DPO/DMx are not allowed to be inserted inside INDDMY (INDDMY).
2. Medium-density INDDMY (INDDMY_MD): Conditioned inter-via/inter-metal are allowed within INDDMY_MD region on the premise that INDDMY_MD rules has been followed. The inductor performance impact by the extra-added dummy pattern must be taken care by designers. When other devices, patterns or metal routing are put within IMDDMY_MD, the extra parasitic, device coupling and model accuracy issue also must be taken into consideration by designers.
3. High-density INDDMY (INDDMY_HD): All the inter-vias/inter-metals are allowed within INDDMY_HD region on the premise that all the related logic design rules has been followed well, especially for the inter-layer metal density rules. The inductor performance impact by the extra-added dummy pattern must be taken care by designers. When other devices, patterns, metal routing are put within IMDDMY_HD, the extra parasitic, device coupling and model accuracy issue also must be taken into consideration by designers.

Rule Type	SPICE	PDK	LVS	Process
Low-density INDDMY (INDDMY)	○	○	○	○
Medium-density INDDMY (INDDMY_MD)	╳	╳	╳	○
High-density INDDMY (INDDMY_HD)	╳	╳	╳	○
○: available ╳: not available				

Table 4.6.8.1 INDDMY Rule Summary

Rule Type	**INDDMY**	**INDDMY_MD**	**INDDMY_HD**
DMx	Not Allowed	Allowed inside (INDDMY_MD NOT (INDDMY_COIL AND INDDMY_MD))	Allowed
DOD/DPO	Not Allowed	Allowed	Allowed
Inter-Metal (Mx)	Not Allowed except the Mx layer directly below [Mz or Mu]	Allowed	Allowed
Inter-Via (Vx)	Not Allowed	Allowed	Allowed

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4.6.8.1 Layout Rules for Inductors with INDDMY Layer

For eddy current reduction, a special metal (and OD/PO) dummy block layer called “INDDMY” (CAD layer:144,) is offered to allow very low metal density within the inductor, provided a proper surrounding (dummy) metal scheme requirement is satisfied. Inductors could be implemented by either 9KA thick top metal layer(s) (Mz) or 34KA ultra thick top metal layer (Mu). Please be noted that “INDDMY” can only be used for inductor devices, TSMC does not support for non-inductor devices constructed with “INDDMY”.Inductor devices offered in TSMC PDK can fit the design rule listed below.

Rule No.	Description	Label		Rule
IND.W.1	M1 width in (INDDMY SIZING 12 µm)	A1	≥	0.40
IND.W.2	Mx width in (INDDMY SIZING 12 µm)	A2	≥	0.60
IND.W.3	Mz width in (INDDMY SIZING 12 µm)	A3	≥	0.80
IND.W.4	M1/Mx maximum width in (INDDMY SIZING 12 µm)	B1	≤	12.00
IND.W.5	Mz/Mu maximum width [outside (INDDMY SIZING 18 µm) and except bond pad]	B2	≤	12.00
IND.W.6	Mz/Mu maximum width for inductor application only [inside (INDDMY SIZING 18 µm)]	B3	≤	30.00
IND.W.7	Maximum dimension (either width or length) of an INDDMY region	C	≤	600.00
IND.S.1	M1 space in (INDDMY SIZING 12 µm)	D1	≥	0.40
IND.S.2	Mx space in (INDDMY SIZING 12 µm)	D2	≥	0.60
IND.S.3	Mz space in (INDDMY SIZING 12 µm)	D3	≥	0.80
IND.S.4	M1/Mx/Mz space in (INDDMY SIZING 12 µm) [at least one metal line width > 1.5 µm (W1) and the parallel metal run length > 1.5 µm (L1)]	E	≥	1.00
IND.S.5	M1/Mx/Mz space in (INDDMY SIZING 12 µm) [at least one metal line width > 4.5 µm (W2) and the parallel metal run length > 4.5 µm (L2)]	F	≥	2.00
IND.R.1	In the region of (INDDMY SIZING 12 µm), inter-via (Vx) is not allowed.			
IND.R.2	At least 4 VIAz with space <= 1.7 µm are required to connect [two Mz layers] or [Mz to Mx] in (INDDMY SIZING 12 µm), (Please put as many vias as possible for reliability and RF applications).	I1	≤	1.70
IND.R.3	At least 4 VIAu with space <= 1.7 µm are required to connect [Mu to Mz] or [Mu to Mx] in (INDDMY SIZING 12 µm), (Please put as many vias as possible for reliability and RF applications).	I2	≤	1.70
The following inductor rule description is based on the concept of different regions (“a”, ”b”, ”c” and “d”) from center to edge to achieve the flexibility of design easiness and maintaining density for uniformity.				
IND.R.4	In the region “a” of (INDDMY SIZING -4 µm), except the Mx layer directly below [Mz or Mu], any other inter-metal layer (Mx) is not allowed. (E.g. for a 1P6M process with 9KA of M6 (Mz), then Mx of M5 is allowed, but other lower Mx metal layers are not allowed for the inductor.)			
IND.R.5[U]	In the region “a” of (INDDMY SIZING -4 µm), except the needed patterns for inductor structure itself (such as OD, PO, PP, CO, M1, Vz, Mz,…), any active device, active OD/PO, interconnection OD/PO or metal routing is not allowed. (This rule cannot be checked by DRC.)			
IND.R.6	In the ring region “b” of {INDDMY NOT (INDDMY SIZING -4 µm)} with 4 µm in width, 3 µm x 3 µm dummy metal islands with 3 µm space for metal layers from metal 2 to the top metal layer (Mz or Mu) are required to maintain CMP uniformity. Metal 1 in the ring region “b” can be designed for guard-ring, but its corresponding metal density must be followed (IND.DN.1).			
IND.R.7[U]	In the ring region “b” of {INDDMY NOT (INDDMY SIZING -4 µm)} with 4 µm in width, except the 3 µm x 3 µm metal islands (IND.R.6), the straight metal line that connects the inductor to the circuits outside INDDMY region and the needed patterns for inductor structure itself (such as OD, PP, CO & M1 for guard-ring…), any active device, active OD/PO, interconnection OD/PO or metal routing is not allowed in this region. (This rule cannot be checked by DRC.)			
IND.R.8	In the 4um wide ring region “b” defined as {INDDMY NOT (INDDMY SIZING –4 µm)}, empty (no pattern) area larger than either (4 µm x 12			

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Rule No.	Description	Label		Rule
	µm) or (12 µm x 4 µm) is not allowed for all metal layers. This rule check is excluded for all metal layers within the 20um extension region next to the so called “metal port leading”. “Metal port leading” is defined as a metal line that goes through the 16 um wide ring regions “b”, ”c” and “d” for interconnect.			
IND.DN.1	Metal density within ring region “b” of {INDDMY NOT (INDDMY SIZING -4 µm)} with 4 µm in width. This rule check is excluded for all metal layers within the 20um extension region next to the so called “metal port leading”. “Metal port leading” is defined as a metal line that goes through the 16 um wide ring regions “b”, ”c” and “d” for interconnect.		≥ ≤	10% 80%
IND.R.13	INDDMY enclosure of inductor metal spirals. 1. The larger distance (such as 50 µm) from inductor metal spirals to guarding-ring would make better inductor electrical performance and reduce the coupling on/between components nearby. Please take the impact of the INDDMY enclosure of inductor metal spirals into consideration. 2. Keep the INDDMY regions of separate inductors located as uniform as possible over the whole chip area to maintain CMP uniformity.	G	≥	4.00
IND.R.14	It is prohibitive to have My, VIAy, Mr, and VIAr in your Inductor design.			
IND.DN.6	Maximum density of INDDMY in whole chip		≤	5%
IND.DN.7	Maximum M1/Mx/Mz density within (INDDMY SIZING 12 µm) over any 50 µm x 50 µm area (stepping in 25 µm increments) except Mz which is used as top metal layer		≤	90%
IND.DN.8	Maximum M1/Mx/Mz density within (INDDMY SIZING 12 µm) over any 100 µm x 100 µm area (stepping in 50 µm increments) except Mz which is used as top metal layer.		≤	80%
IND.DN.9	M1/Mx/Mz metal density over the whole chip (include INDDMY) if you have INDDMY.		≥	20%
IND.R.15	A 0.01um checking tolerance is allowed for the rules: IND.W.1, IND.W.2, IND.W.3, IND.W.4, IND.W.6, IND.W.7, IND.S.1, IND.S.2, IND.S.3, IND.S.4, and IND.S.5.			
IND.R.16	A 0.01 µm checking tolerance in the region of [(INDDMY) SIZING 18 µm] is allowed for the listed regular logic rules in “T-N65-CL-DR-001”: RV.S.1, RV.EN.1, AP.W.1, AP.W.2, AP.S.1 and AP.EN.1. Note: DRC implement 0.01µm tolerance on Vertical, Horizontal and 45-degree bent.			
IND.R.17g^{U}	Recommend putting NT_N to fully cover the inductor (metal) to achieve high quality factor.			
Waive items	Tsmc waive following items for inductor by INDDMY layer: OD.DN.2, OD.DN.3, PO.DN.2, Mu.W.2, Mz.W.2, Mu.DN.2, Mx.DN.1, Mx.DN.1.1, Mx.DN.2, Mz.DN.1, Mz.DN.2, M1.DN.1 and M1.DN.2			

Notes:

1. The INDDMY blocks the automated dummy generation.
2. The dummy generation utility inserts floating dummy OD/PO/metal patterns into the region outside (INDDMY SIZING 2.5 µm).
3. Due to the layout on-grid requirement, a 0.005µm rule check tolerance is applied to the 45-degree patterns within the region of (INDDMY SIZING 12 µm).
4. For TSMC PDK offered inductor, a native substrate region is created under the inductor coil to minimize eddy currents. This region is specified/implemented by the implant blocking NT_N layer (CAD layer:11). The NT_N drawn layer adds no process cost and no extra mask.
5. TSMC offered PDK Inductor does not support the inductors implemented by 5KA (My) or 12.5KA (Mr) thick top metal layer(s). If designers want to design the inductors with inter-layer metal and/or inter-layer via, users need to implement the dummy layers INDDMY_MD , INDDMY_COIL, or INDDMY_HD to define the inductor region with inter-layer metal and/or inter-layer via and follow the design rules in section 4.6.8.1 or 4.6.8.2. Besides, users need to take care the potential Inductor performance deviation (e.g.: Q-factor) introduced by the additional inter-layer metal using the qualified EM simulator. For an inductor to be with dummy OD/PO/Metal patterns inserted into, the INDDMY dummy layer should be removed to allow dummy deck’s dummy pattern generation.

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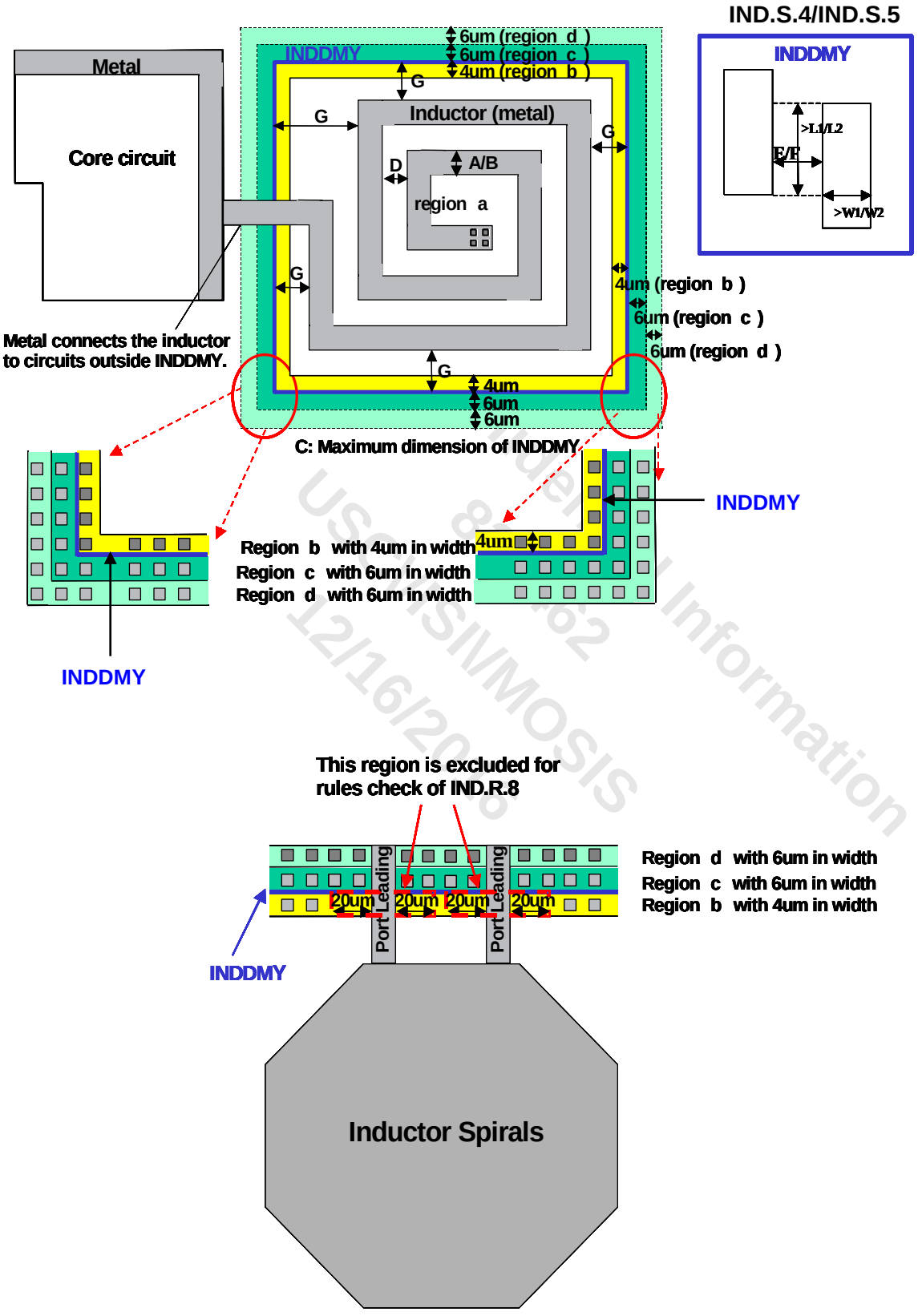
6. TSMC offered PDK inductor is octagonal type, the square type inductor in the following picture is only for rule illustrations.



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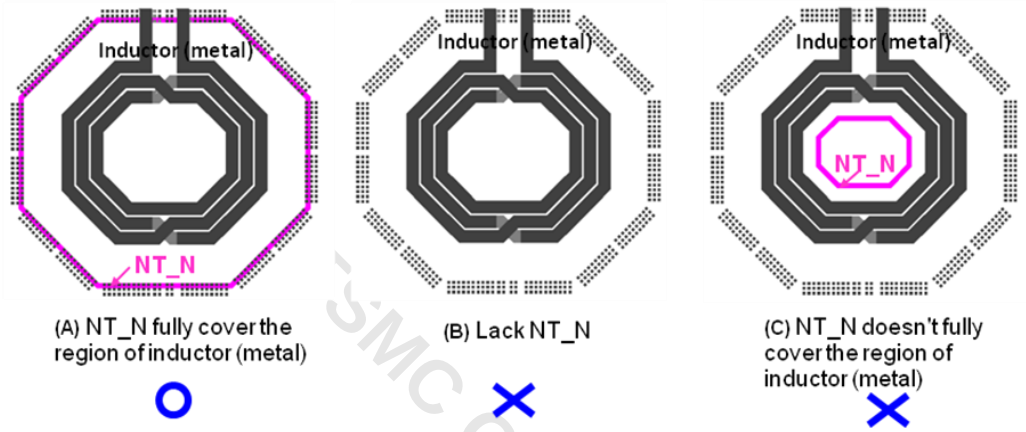
IND.R.17g^{U}



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4.6.8.2 Layout Rules for Inductors with INDDMY_MD Layer

For better process uniformity, a special dummy layer called “INDDMY_MD” (CAD layer: 144;37) is offered to allow conditioned inter-metal/inter-via within the inductor under the condition of proper dummy metal scheme requirement is satisfied. Please be noted that “INDDMY_MD and INDDMY_COIL” can only be used for inductor devices, and TSMC does not support for non-inductor devices constructed with “INDDMY_MD and INDDMY_COIL”.

(1) INDDMY_MD layer (144;37): This layer is only drawn over inductor region for medium metal density inductor.

(2) INDDMY_COIL layer (144;36): This layer is drawn over metal coil within INDDMY_MD for DRC checking purpose.

Please take care the SPICE model /LVS flow by yourselves when using INDDMY_MD layer to design inductor.

Rule No.	Description	Label		Rule
IND_MD.DN.11	Metal density in the region of (INDDMY_MD NOT (INDDMY_COIL AND INDDMY_MD))		≥	15% in 75x75
			≤	80% in 100x100
IND_MD.DN.10	For the region of (INDDMY_MD SIZING 12 µm) with VIAx adopted, minimum metal density over any 15 µm x 15 µm area for all lower metal layers that below VIAx in the region of {[(((Inter-VIA AND (INDDMY_MD SIZING 12µm)) SIZING 5 µm) SIZING -5 µm) SIZING 5 µm] AND (INDDMY_MD SIZING 12µm)}. E.g. If V3 and V4 as Vx are the adopted inter via within (INDDMY_MD SIZING 12 µm) region, then the metal density within the check region for the M4, M3, M2 and M1 must be followed.		≥	15%
IND_MD.R.17	At least 100 VIAx with space ≤ 0.20 µm are required to connect [two Mx layers] or [Mx to M1] in (INDDMY_MD SIZING 12 µm)	I3	≤	0.20
IND_MD.R.18®[U]	VIAx counts in metal line need to follow item (A) and (B): (See figure 1.6.2) (A) At least 6 column or row array are required in non-45 degree metal line (B) At least 4 column or row array are required in 45-degree metal line.			
IND_MD.W.1	M1, DM1, DM1_O width in (INDDMY_COIL SIZING 16 µm)	A1	≥	0.40
IND_MD.W.2	Mx , DMx , DMx_O width in (INDDMY_COIL SIZING 16 µm)	A2	≥	0.60
IND_MD.W.3	Mz , DMz width in (INDDMY_COIL SIZING 16 µm)	A3	≥	0.80
IND_MD.W.4	M1, DM1, DM1_O/Mx, DMx, DMx_O maximum width in (INDDMY_COIL SIZING 16 µm)	B1	≤	12.00
IND_MD.W.7	Maximum dimension (either width or length) of an INDDMY_MD region	C	≤	600.00
IND_MD.S.1	M1, DM1,DM1_O space in (INDDMY_COIL SIZING 16 µm)	D1	≥	0.40
IND_MD.S.2	Mx, DMx, DMx_O space in (INDDMY_COIL SIZING 16 µm)	D2	≥	0.60
IND_MD.S.3	Mz, DMz space in (INDDMY_COIL SIZING 16 µm)	D3	≥	0.80
IND_MD.S.4	M1, DM1, DM1_O/Mx, DMx, DMx_O/Mz, DMz space in (INDDMY_COIL SIZING 16 µm) [at least one metal line width > 1.5 µm (W1) and the parallel metal run length > 1.5 µm (L1)]	E	≥	1.00
IND_MD.S.5	M1, DM1, DM1_O/Mx, DMx, DMx_O/Mz, DMz space in (INDDMY_COIL SIZING 16 µm) [at least one metal line width > 4.5 µm (W2) and the parallel metal run length > 4.5 µm (L2)]	F	≥	2.00
IND_MD.R.2	At least 4 VIAz with space ≤ 1.7 µm are required to connect [two Mz layers] or [Mz to Mx] in (INDDMY_MD SIZING 12 µm), (Please put as many vias as possible for reliability and RF applications).	I1	≤	1.70
IND_MD.R.3	At least 4 VIAu with space ≤ 1.7 µm are required to connect [Mu to Mz] or [Mu to Mx] in (INDDMY_MD SIZING 12 µm), (Please put as many vias as possible for reliability and RF applications).	I2	≤	1.70

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Rule No.	Description	Label		Rule
IND_MD.R.13	INDDMY_MD enclosure of {inductor metal spirals AND INDDMY_COIL}. Keep the INDDMY_MD regions of separate inductors located as uniform as possible over the whole chip area to maintain CMP uniformity.	G	≥	4.00
IND_MD.R.20 U	INDDMY_COIL enclosure of inductor metal spirals. INDDMY_COIL must fully cover and fully abutted the region of {inductor metal spiral OR {metal port leading AND INDDMY_MD}}. INDDMY_COIL must be fully inside INDDMY_MD. (See figure 1.6.4) Keep the area of INDDMY_COIL as smaller as possible over the whole INDDMY_MD area to maintain CMP uniformity.		=	0
IND_MD.R.14	It is prohibitive to have My, VIAy, Mr, and VIAr in your Inductor design.			
IND_MD.DN.6	Maximum density of INDDMY_MD in whole chip		≤	5%
IND_MD.DN.7	Maximum M1/Mx/Mz density within (INDDMY_MD SIZING 12µm) over any 50 µm x 50 µm area (stepping in 25 µm increments) except Mz which is used as top metal layer		≤	90%
IND_MD.DN.8	Maximum M1/Mx/Mz density within (INDDMY_MD SIZING 12µm) over any 100 µm x 100 µm area (stepping in 50 µm increments) except Mz which is used as top metal layer.		≤	80%
IND_MD.DN.9	M1/Mx/Mz metal density over the whole chip (include INDDMY_MD) if you have INDDMY_MD.		≥	20%
IND_MD.R.15	A 0.01um checking tolerance is allowed for the rules: IND_MD.W.1, IND_MD.W.2, IND_MD.W.3, IND_MD.W.4, IND_MD.W.7, IND_MD.S.1, IND_MD.S.2, IND_MD.S.3, IND_MD.S.4, IND_MD.S.5 and IND_MD.R.20			
IND_MD.R.16	A 0.01 µm checking tolerance in the region of [(INDDMY_MD) SIZING 18µm] is allowed for the listed regular logic rules in “T-N65-CL-DR-001”:, RV.S.1, RV.EN.1, AP.W.1, AP.W.2, AP.S.1 and AP.EN.1. Note: DRC implement 0.01µm tolerance on Vertical, Horizontal and 45-degree bent.			
IND_MD.R.21®U	The inductor performance impact by the extra-added dummy pattern must be taken care by designers. When other devices, patterns or metal routing are put within IMDDMY_MD, the extra parasitic, device couplings and model accuracy issue also must be taken into consideration by designers.			
Waive items	Tsmc waive following items for inductor by INDDMY_MD layer:, Mu.DN.2L, Mx.DN.1L, Mz.DN.1L and M1.DN.1L			

Notes:

1. Logic rules are applied in the region of (INDDMY_MD NOT (INDDMY_COIL SIZING16um))
2. Special inductor dummy utility provides an option to auto-generate specific dummy metal within (INDDMY_MD NOT INDDMY_COIL) to lower the inductor performance degradation caused by dummy fill. But the real inductor performance impact by these extra-added dummy metal patterns still must be taken care by designer.
3. The dummy generation utility inserts floating dummy metal patterns into the region outside (INDDMY_MD SIZING 2.5 µm) and dummy OD/PO inside and outside INDDMY_MD
4. Due to the layout on-grid requirement, a 0.005µm rule check tolerance is applied to the 45-degree patterns within the region of (INDDMY_MD SIZING 12 µm).

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Figure 4.6.8.2.1

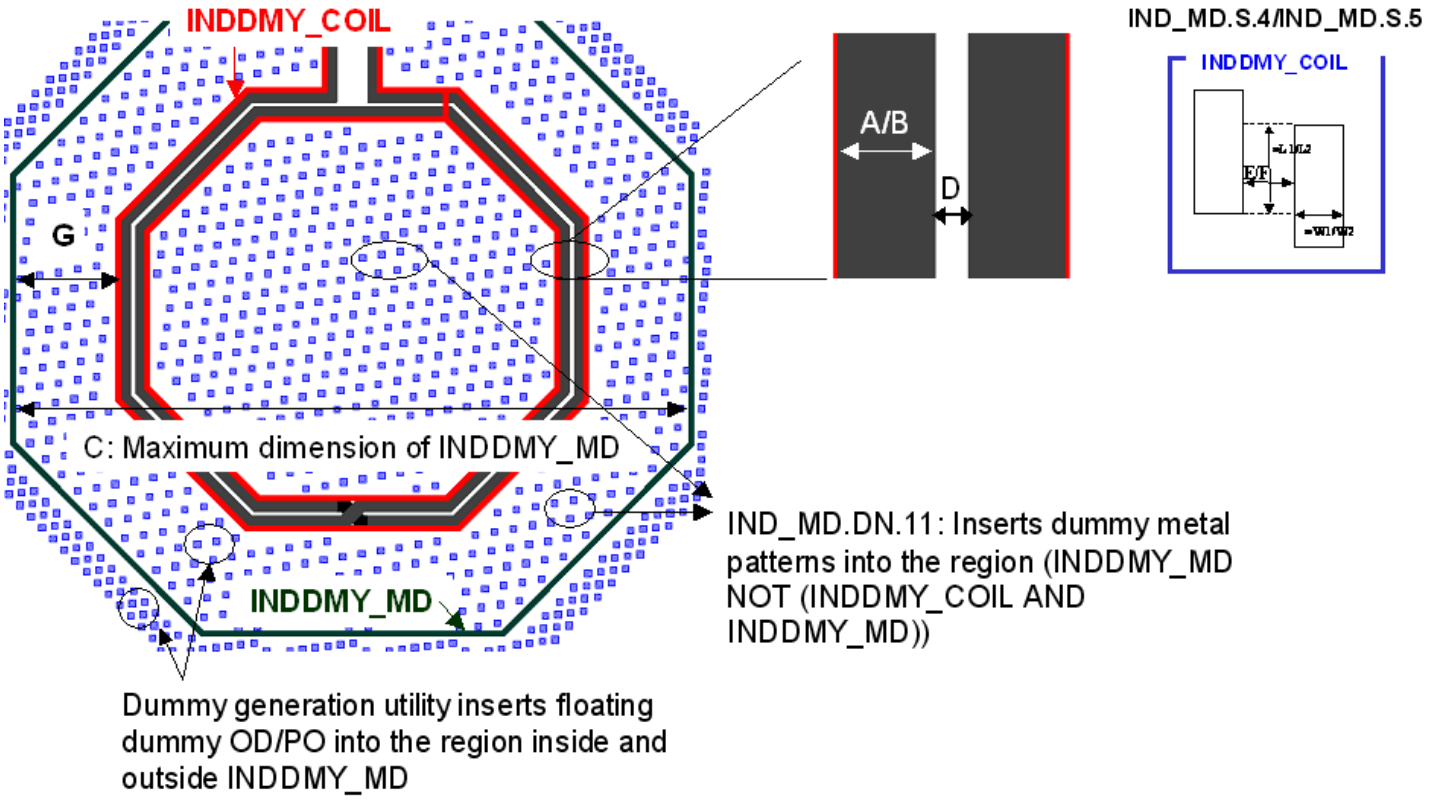

Figure 4.6.8.2.2

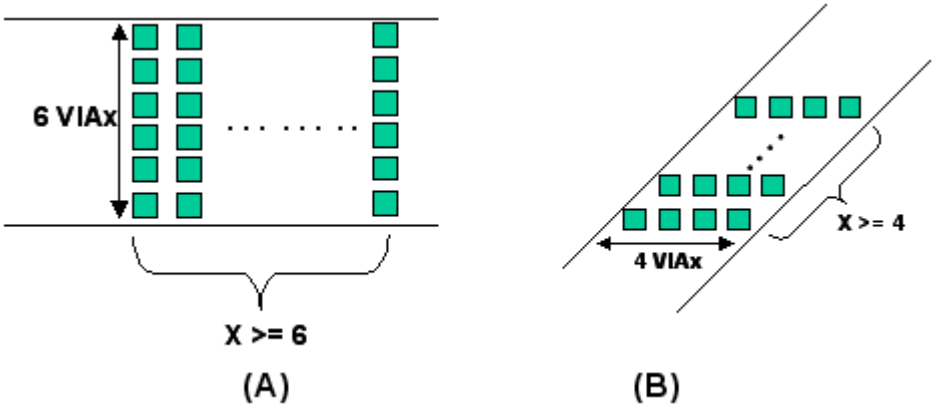

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Figure 4.6.8.2.3

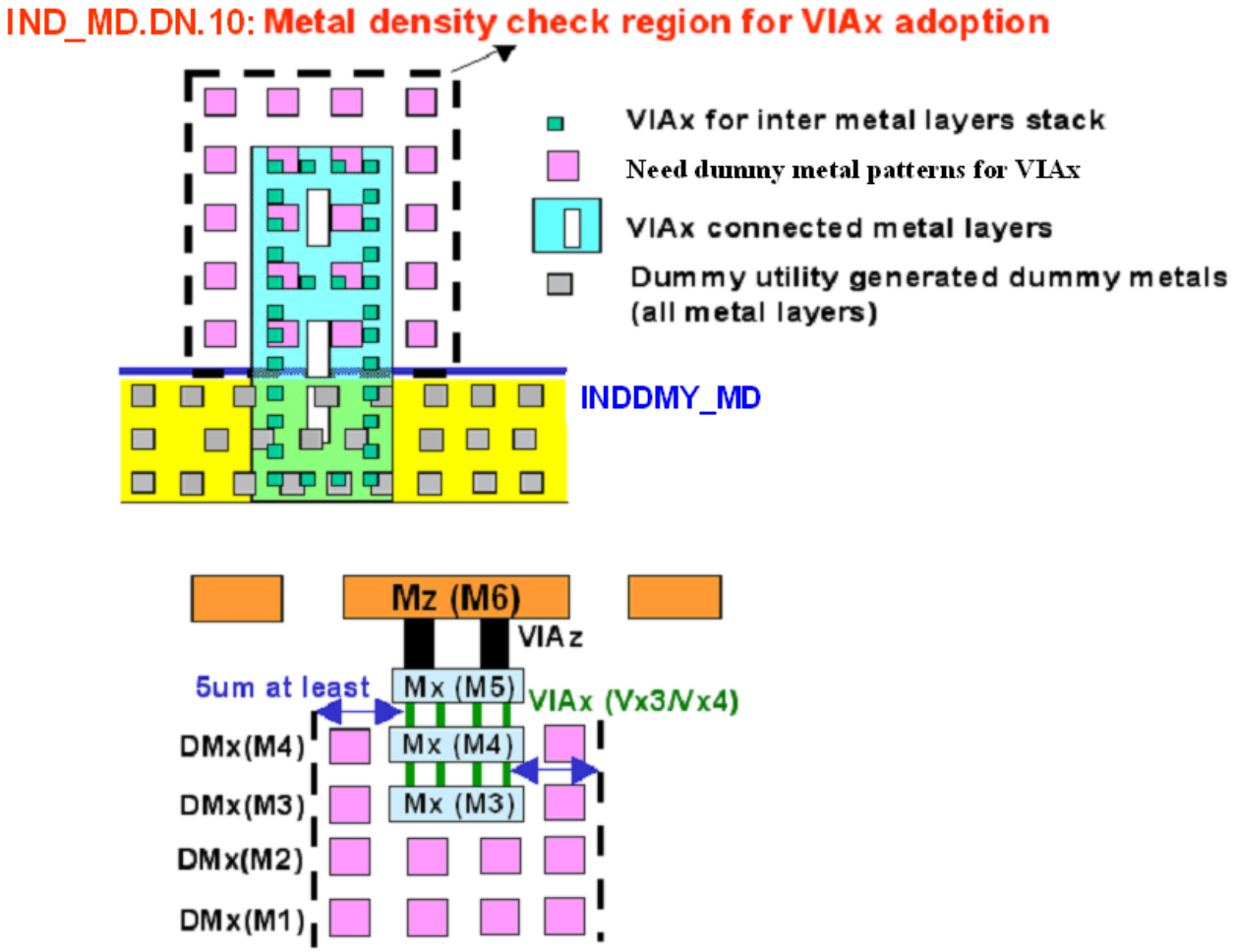
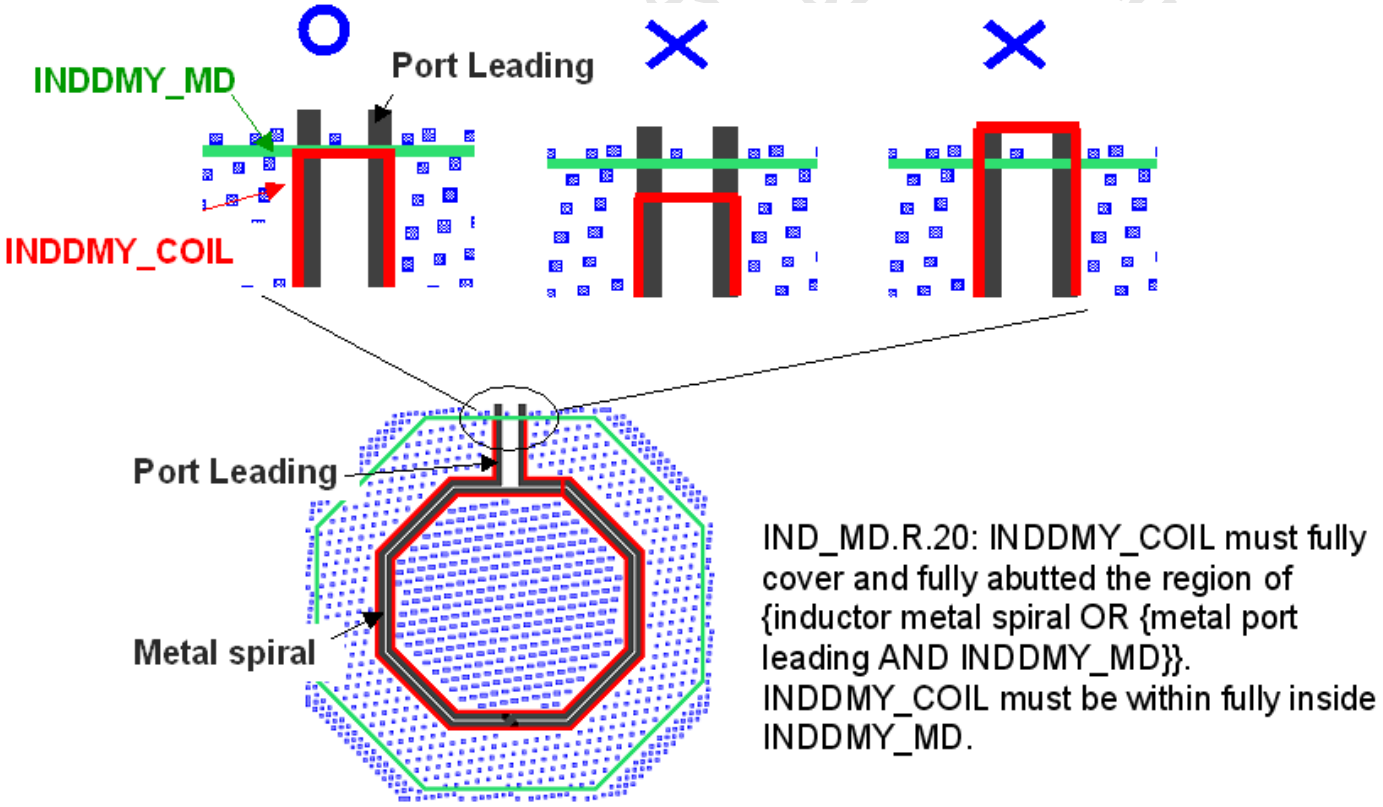


Figure 4.6.8.2.4



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4.6.8.3 Layout Rules for Inductors with INDDMY_HD Layer

For better process uniformity, a special dummy layer called “INDDMY_HD” (CAD layer: 144;38) is offered to define logic inductor region.

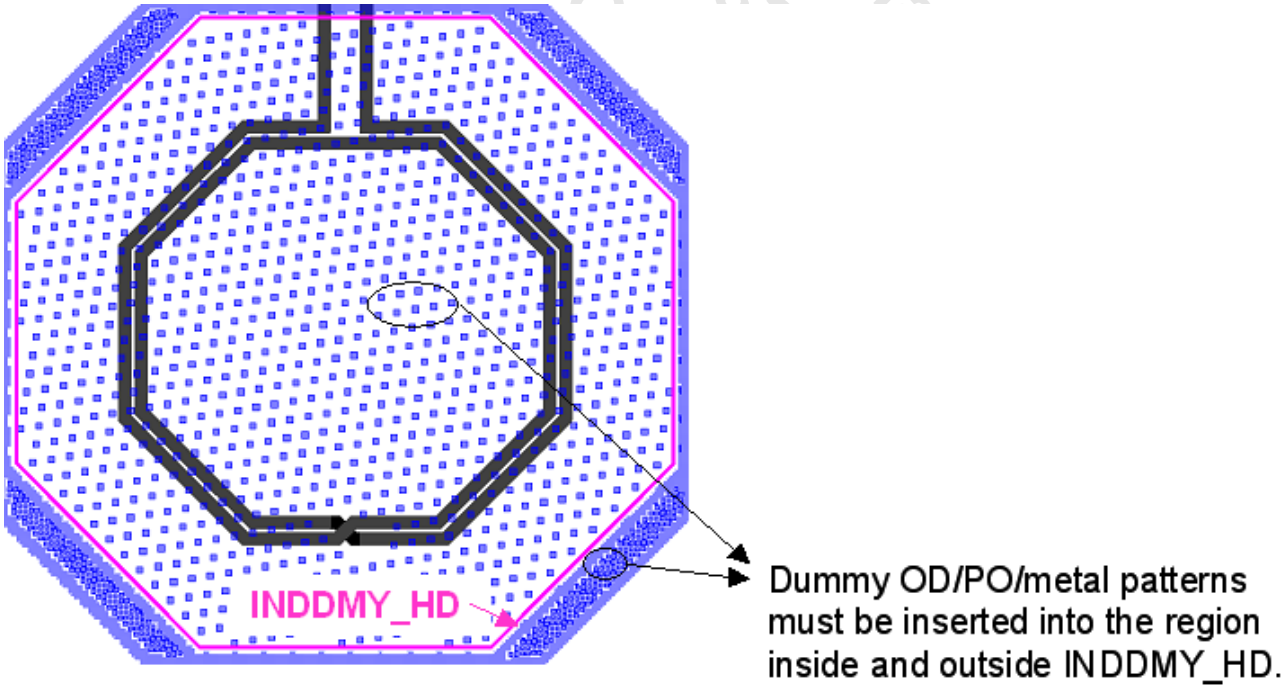
All the inter-vias/inter-metals are allowed within INDDMY_HD region on the premise that all the related logic design rules has been followed well, especially for the inter-layer metal density rules. All the rules within INDDMY_HD follow general logical rules.

Please be noted “INDDMY_HD” can only be used for inductor devices,

Notes:

1. Special inductor dummy utility provides an option to auto-generate specific dummy metal within INDDMY_HD to lower the inductor performance degradation caused by dummy fill. But the real inductor performance impact by these extra-added dummy metal patterns still must be taken care by designer.
2. The dummy generation utility inserts floating dummy metal patterns into the region outside (INDDMY_HD SIZING 2.5 µm) and dummy OD/PO inside and outside INDDMY_HD.
3. INDDMY_HD rules are allowed to build an inductor element in terms of process, customers need to take care the SPICE model /LVS flow by themselves when using INDDMY_HD layer to design inductor.
4. The inductor performance impact by the extra-added dummy pattern must be taken care by designer. When other device, patterns or metal routing are put within IMDDMY_HD, the extra parasitic, device couplings and model accuracy issue also must be taken into consideration by designers.

Figure 4.6.8.3.1



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4.6.8.4 Inductor Guidelines

TSMC offered a variety of ways to construct inductor devices for MS/RF circuit design need:

1. To achieve lower inductor series resistance, a >3um ultra thick Cu metal (Mu) process is offered and its associated process design rule is listed in section 4.6.8.

2. In section 4.6.9.1 below, we used the inductor offered in TSMC PDK as examples to briefly illustrate the basic guidelines and elements for constructing various inductors such as standard (simple spiral), symmetric and central-tap inductors.

4.6.8.5 Introduction to PDK Inductor

1. TSMC PDK offered octagonal inductors in the 65nm technology node apply to the top metal scheme of regular thick metal layer(s) (Mz) or ultra thick metal layer (Mu). As summarized in the Table 4.6.9.1, four kinds of top metal scheme inductors are provided, and the offerings for each top metal scheme option include three different layout configurations: standard (STD), symmetric (SYM) and center-tap (CT).
2. The symmetric type inductor can be used both as single-ended mode or differential mode.
3. Inductors implemented by 5KA (My) and 12.5KA (Mr) thick metal layer(s) are not supported by the TSMC PDK.
4. The offered inductors are fabricated on top of P-substrate that specified/implemented by an NT_N implantation-blocking layer (CAD layer:11, that adds no extra mask/process cost). The offered inductor is 3-Terminal including two signal terminals and the third terminal for grounded guard-ring (CT type inductor has the fourth terminal for center-tap connection).
5. The INDDMY dummy layer(s) (CAD layer:144) is needed to identify the inductor with very low metal density within the inductor, the DRC (design rule check) deck will check the INDDMY identified region by inductor related/specific rules. The INDDMY layer cannot be used for other applications (for inductor only), and allowed maximum density of INDDMY in whole chip is 5% (rule IND.DN.6). The inductor with different kinds of metal scheme and configuration type has its corresponding INDDMY dummy layer for LVS purpose (Table 4.6.9.1).
6. The INDDMY dummy layer blocks the automated generation of dummy OD/PO/Metal patterns (dummy Al-RDL patterns will not be generated).
7. The dummy OD/PO/Metal patterns make better pattern uniformity and better metal CMP uniformity over the silicon wafer.
8. Table 3.5.11 shows the PDK inductor truth table (where the inductor with most metal layers scheme is illustrated).
9. From the inductor model accuracy point of view, other devices or metal patterns is not allowed to be placed below/above the offered inductors, as the magnetic flux and the resulted inductor performance will be affected by the extra-added parts. If other devices, patterns or metal routing (not generated by PDK itself) are added into the region below/above the PDK inductor, the resulted extra parasitic and model inaccuracy must be taken into consideration by designers.
10. The PDK inductor layout parameters in 65nm node are listed in Table 4.6.9.2. The corresponding temperature effect and corner cases are also included; please refer to the model documents for model scope and other details.

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Table 4.6.8.5.1 Summary of inductor metal scheme option and corresponding INDDMY layer

PDK Inductor Scheme [M_{top-2}+M_{top-1}+M_{top}+(AP-RDL)]	Inductor Type		INDDMY (CAD layer;datatype)	Layer Usage			
				M_{top-2}	M_{top-1}	M_{top}	AP-RDL
Mx+Mz+Mu (Top Metal: M5 ~ M9)	standard	spiral_std_mu_z	INDDMY (144;0)		v	v	
	symmetric	spiral_sym_mu_z	INDDMY (144;1)		v	v	
	center-tap	spiral_ct_mu_z	INDDMY (144;2)	v	v	v	
Mx+Mu+Al-RDL (Top Metal: M5 ~ M8)	standard	spiral_std_mu_a	INDDMY (144;6)			v	v
	symmetric	spiral_sym_mu_a	INDDMY (144;7)			v	v
	center-tap	spiral_ct_mu_a	INDDMY (144;8)		v	v	v
Mx+Mz+Al-RDL (Top Metal: M5 ~ M8)	standard	spiral_std_mza_a	INDDMY (144;9)			v	v
	symmetric	spiral_sym_mza_a	INDDMY (144;10)			v	v
	center-tap	spiral_ct_mza_a	INDDMY (144;11)		v	v	v

1. Thickness of Mx/Mz/Mu/Al-RDL=0.22um/0.9um/3.4um/1.45um.
2. When Al-RDL adopted, allowed min width in 45-degree is around 7.5um {>[3*(2^0.5)+1.5*2]} due to 3umx3um RV size.
3. The naming in "Inductor Type" column illustrates the individual inductor structures, e.g. "spiral_std_mu_z" means "inductor", "standard type", "Mu layer spiral" and "Mz layer underpass", respectively.

Table 4.6.8.5.2 PDK inductor layout parameters

W(w)(um)	spiral track width
N(nr)	number of turns
R(rad)(um)	inner radius
GDIS(gdis)(um)	distance from guard-ring to spiral
1PxM(lay)	top metal layer

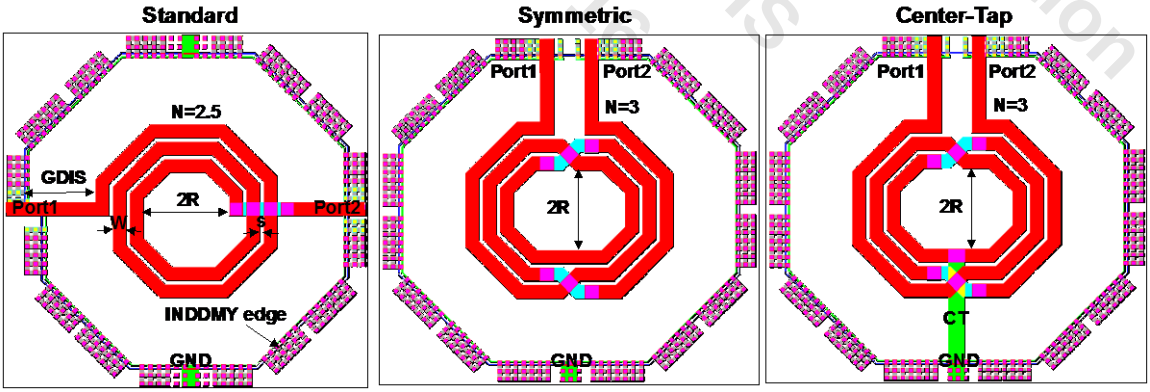

Figure 4.6.8.5.1 PDK inductor top-view illustration

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4.6.9 Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns

Please follow most updated logic rule in the section 4.5 for CSR placing guidelines and rules for non-Mu design.
For Mu design, some CSR design rules need to be revised as the following.

Rule No.	Description	Label		Rule
TSMC provide some sample gds files for different metal options. For non-Mu process, please refer to most updated logic rule in the section 4.5 archived sample gds files. For Mu process, two gds examples are archived along with this document: "*N65_Mu_SR_03152013.gds" and "N65_Mu_SR_ 12022016_WLCSP.gds".*				
All of rules and guidelines defined in most updated logic rule in the section 4.5 are still valid except below rules:				
CSR.EN.10	Top metal enclosure of L-slot [perpendicular to the direction of the L-slot length] (Except WLCSP sealring region). (This is for Mu design)	C'	≥	27
			≤	29
CSR.EN.10.1	Metal layers of sealring corners can only exist isosceles triangle for WLCSP sealring region. An empty isosceles triangle area must exist butted to the WLCSP sealring outside corner.			
	Minimum length of isosceles triangle (except AP)	C'	≥	17
	Maximum length of isosceles triangle (except AP)		≤	18
CSR.EN.10.2	Minimum length of AP layer isosceles triangle for WLCSP sealring region	C'	≥	18.1
	Maximum length of AP layer isosceles triangle for WLCSP sealring region		≤	19.2

Example: For a design with 6M: 3x1z1u.
Step 1: Locate the "3x1z1u" column under "1P6M" in the metallization options table above. Delete unused metal and via layers: (54;0), (35;0), (55;0),(36;0),(56;0),(37;0) .
Step 2: Re-assign CAD ID for the layers denoted with "", from VIA7(57;40), (38;40), (58;40) and (39;60), respectively, to VIA4(z)(54;40), (35:40), (55:40) and (36:60) to match with your metallization scheme.*

4.6.10 Seal-Ring Rule

Please follow exactly the schematic diagram below for seal-ring layout (as in the GDS example "*N65_Mu_SR_03152013.gds" and "N65_Mu_SR_ 12022016_WLCSP.gds"*). Now, DRC cannot fully check these pattern dimensions in the Mu seal-ring sample layout. If you do not use these dimensions as the schematic diagram below, please consult with TSMC.

In the following figure, the 10 μm region for assembly isolation is for reference only. The mentioned assembly isolation region depends on the capability of assembly house. If seal ring is added by TSMC, TSMC will add assembly isolation and seal-ring structure at the same time.

AlCu pad (AP)/Polyimide (PM) can be generated by logic operation only for non-flip-chip product.

Rule No.	Description		Rule
VIAu.W.2	Width of VIAu connect to Mu bar. VIAu bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a Must to cover VIAu bar if VIAu bar is used.	=	0.36
SR.EN.2	(OD interact seal ring) enclosure of metal with the outer edge of seal ring. (Only for Mu seal-ring)	≥	2.0

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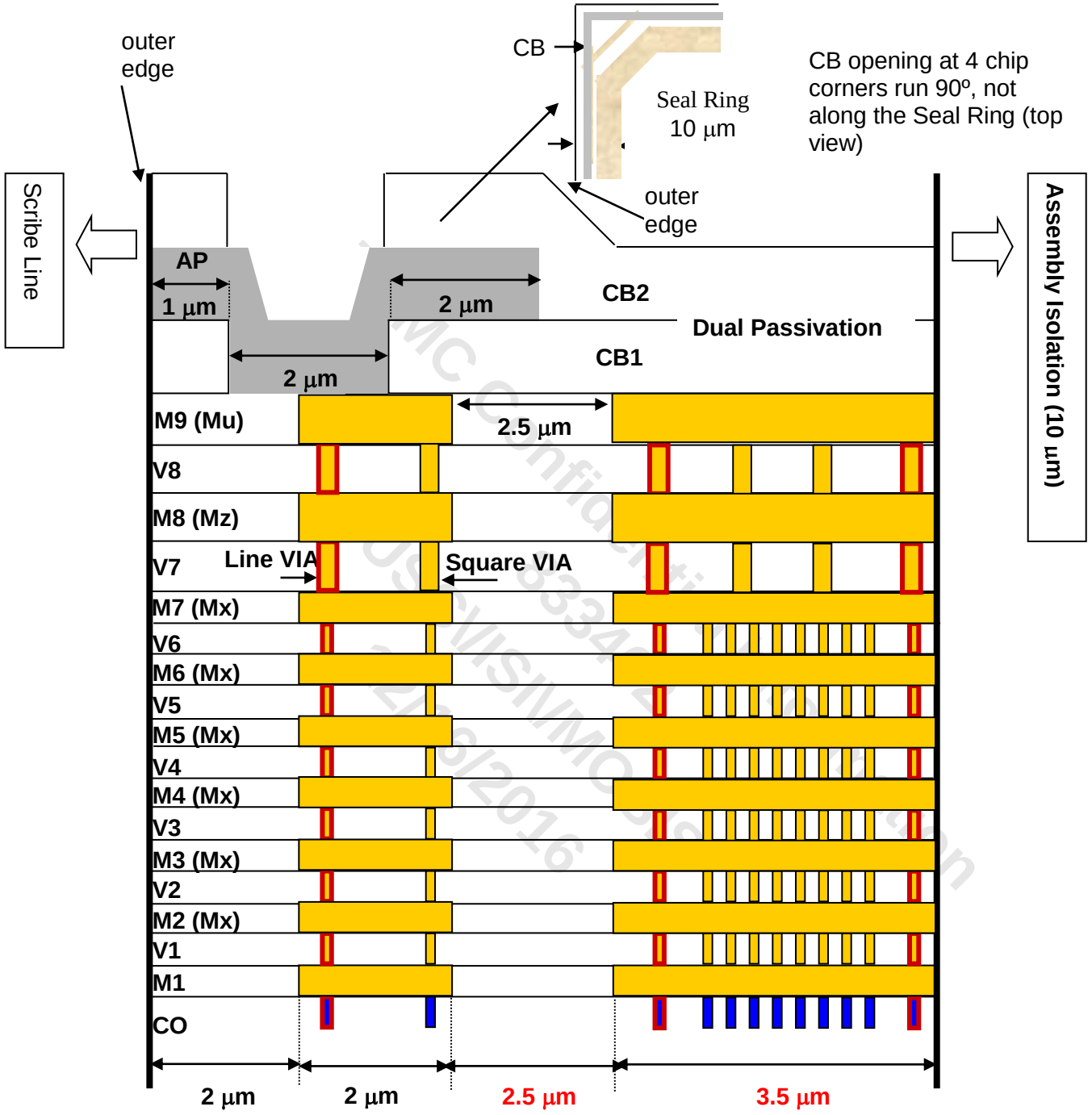
Cross-sectional view of seal ring



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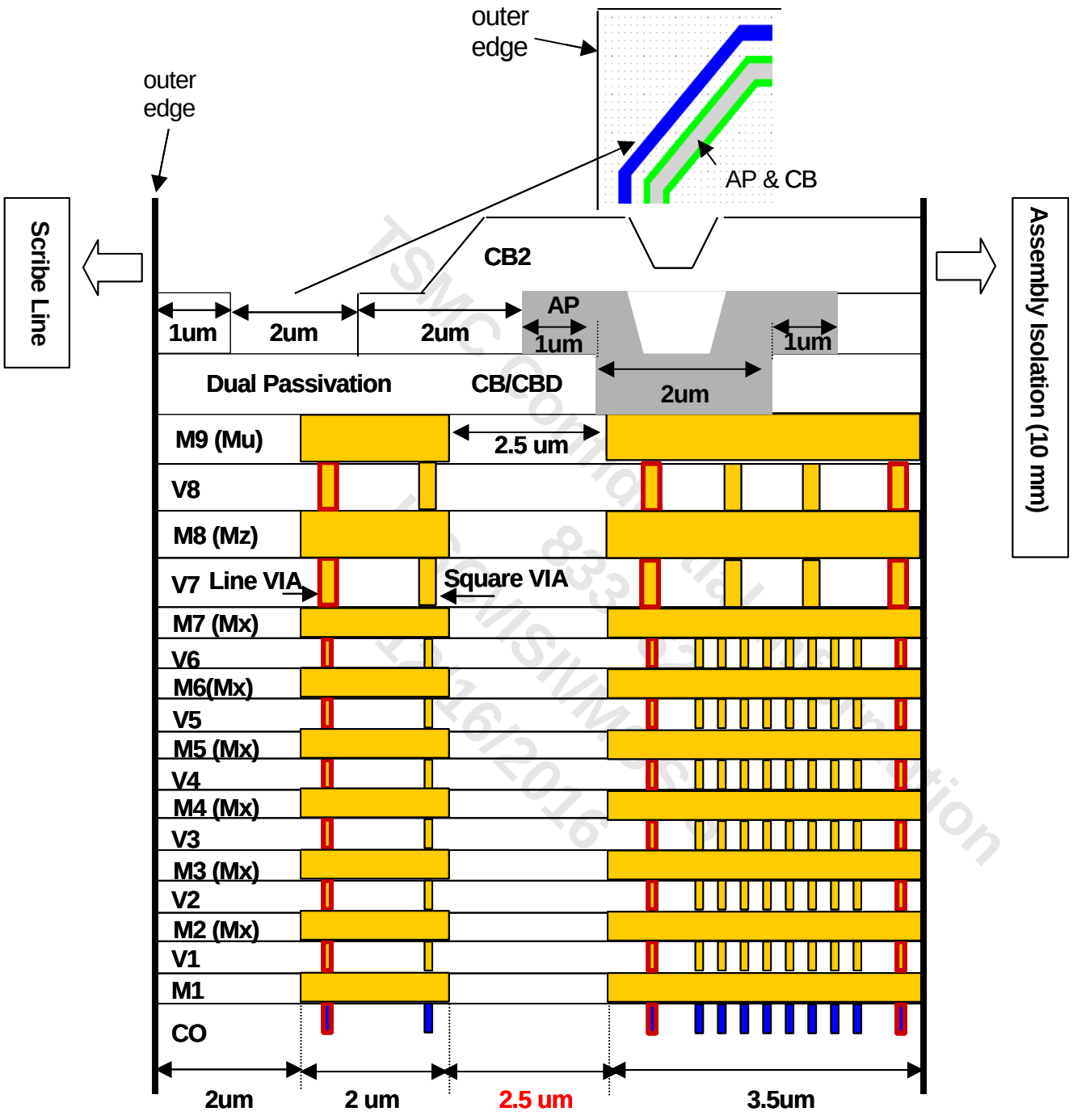
Cross-sectional view of seal ring for WLCSP



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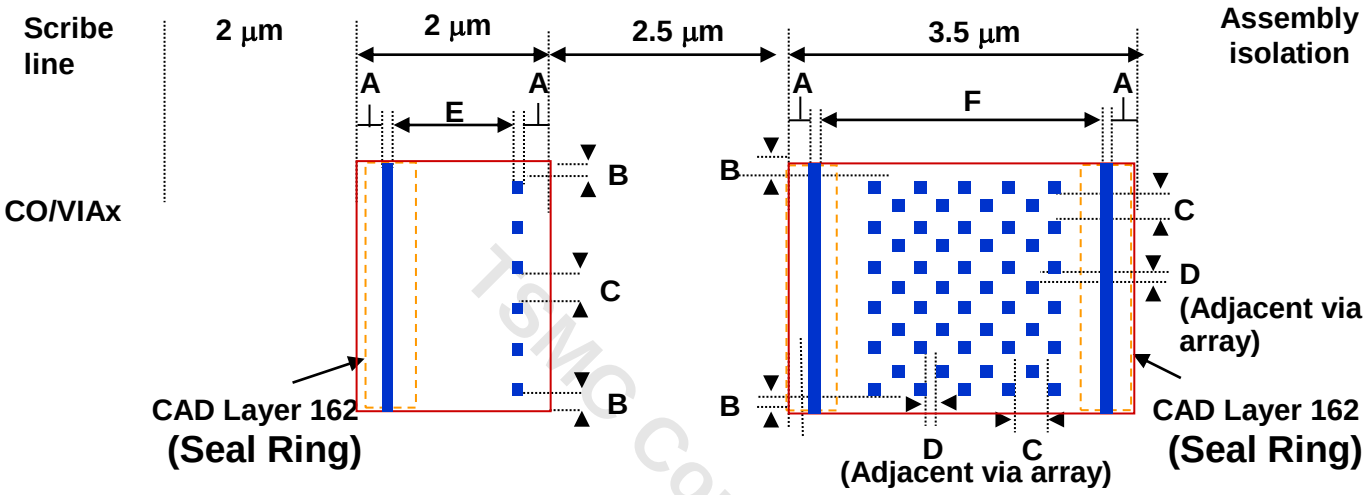
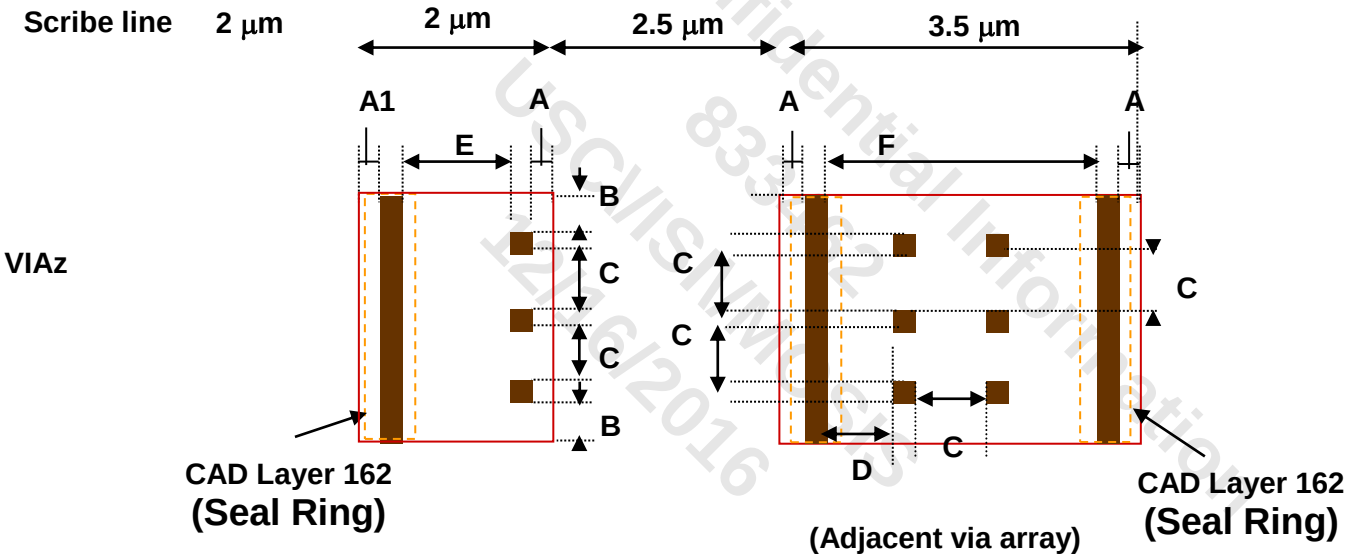
Top view of seal ring





Top view for Seal-Ring structure

Layer	Width	A/A1	B	C/C1	D	E	F
CO	0.09	0.275/NA	0.185	0.37/NA	0.14	1.27	2.77
VIAx (VIA1~VIA6)	0.1	0.27/NA	0.18	0.36/NA	0.13	1.26	2.76
VIAz/VIAu (VIA7, VIA8)	0.36	0.38/0.30	0.28	0.56/0.54	0.38	0.68	2.02

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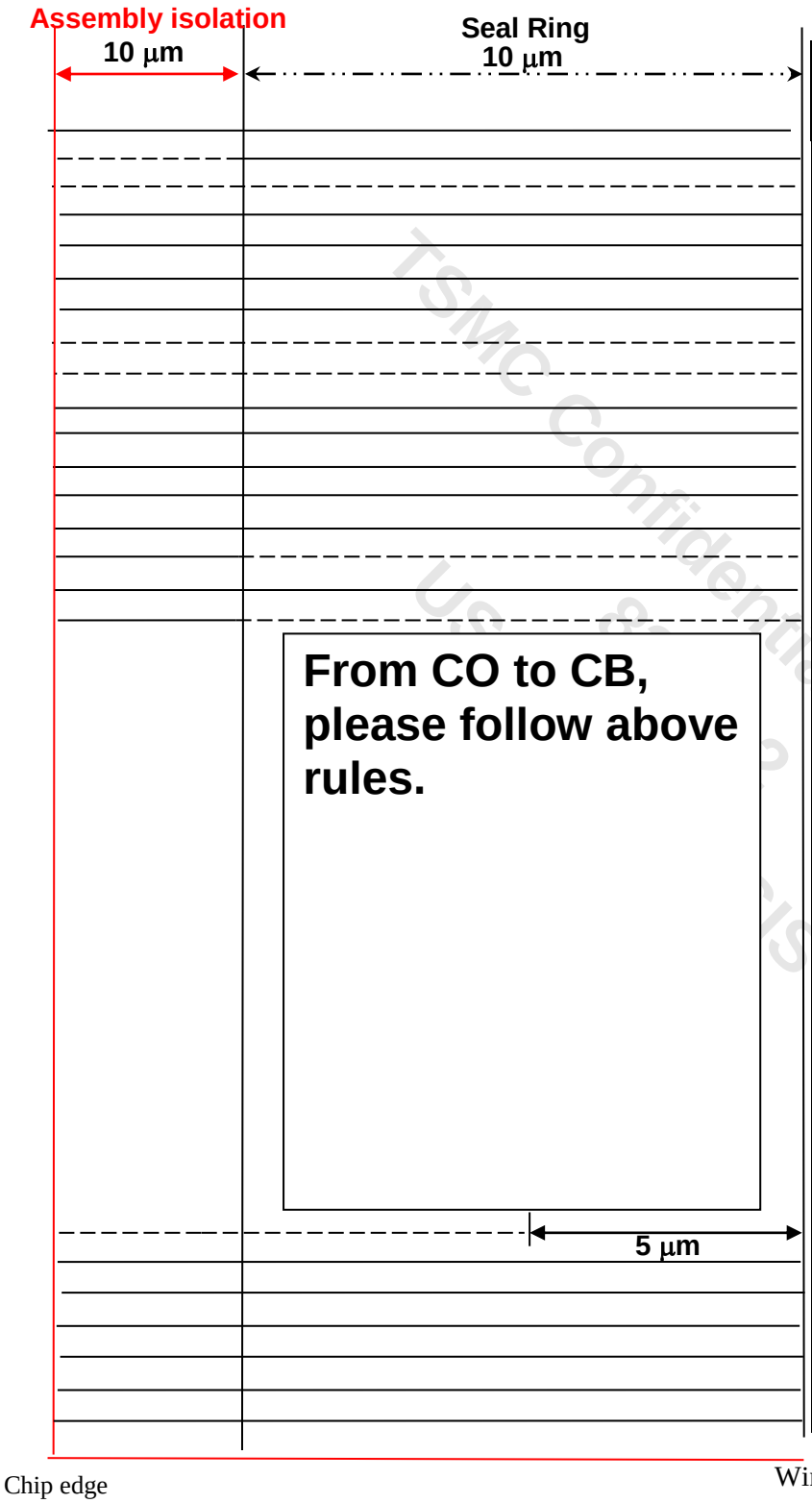
For other layers:

_ _ _ _ : Digitized area is clear on mask. ____ : Digitized area is dark on mask.



Layer	Scribe line
DNW (119)	D
OD (120)	D
PW1V (191)	D
NW1V (192)	D
PW2V(193)	D
NW2V (194)	D
VTC N(112	D
OD2 (132)	C
Poly (130)	C
N1V (114)	D
P1V (113)	D
N2V (116)	D
P2V (115)	D
NP (198)	D
PP (197)	D
ESD (111)	D
RPO (155)	D
CO (156)	D
M1 (360)	D
VIA1 (378)	D
M2 (380)	D
VIA2 (379)	D
M3 (381)	D
VIA3 (373)	D
M4 (384)	D
VIA4 (374)	D
M5 (385)	D
VIA5 (375)	D
M6 (386)	D
VIA6 (376)	D
M7 (387)	D
VIA7 (377)	D
M8 (388)	D
VIA8 (372)	D
M9(389)	D
CB (107)	D
AP (307)	C
FUSE (395)	D
PM (009)	D
VTH P(127)	D
VTH N(128	D
VTL P(117)	D
VTL N(118)	D

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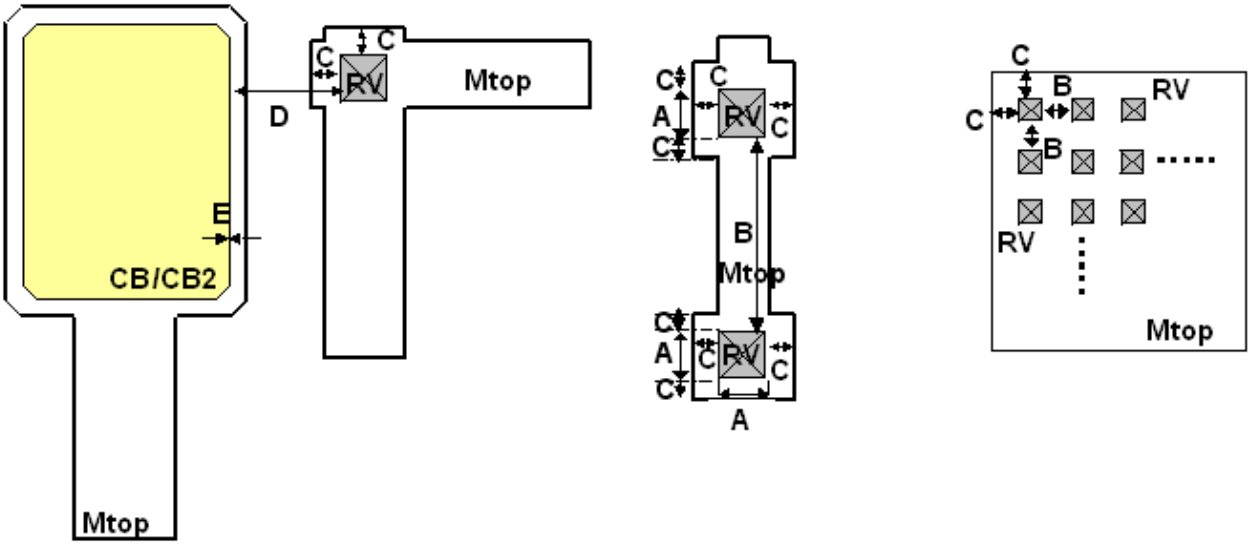
4.7 RV Layout Rules (CB VIA hole)

4.7.1 RV Layout Rules (CB VIA hole) for Wire Bond

- CB-VD mask (306) is generated by the logical operation of CB (CAD layer: 76) and RV (CAD layer: 85).
- You must consider the RV counts to provide enough current for ESD requirements. Therefore, it's recommended to make as many RV holes as possible.

Rule No.	Description	Label		Rule
RV.W.1.WB	Width (Square) (maximum =minimum) {Not inside seal ring}	A	=	3
RV.S.1.WB	Space	B	≥	3
RV.S.3.WB	Space to CB/CB2/FW/FW(AP) [Overlap is prohibited]	D	≥	6
RV.EN.1.WB	Enclosure by Mtop {Not inside seal ring}	C	≥	1.5
RV.R.1.WB	A 45-degree rotated RV is prohibited. (Except WLCSP seal ring region)			
RV.R.2.WB	{CB inside CB2} enclosure by CB2 (CB and CB2 must draw same size and identical shape)	E	=	0

RV:



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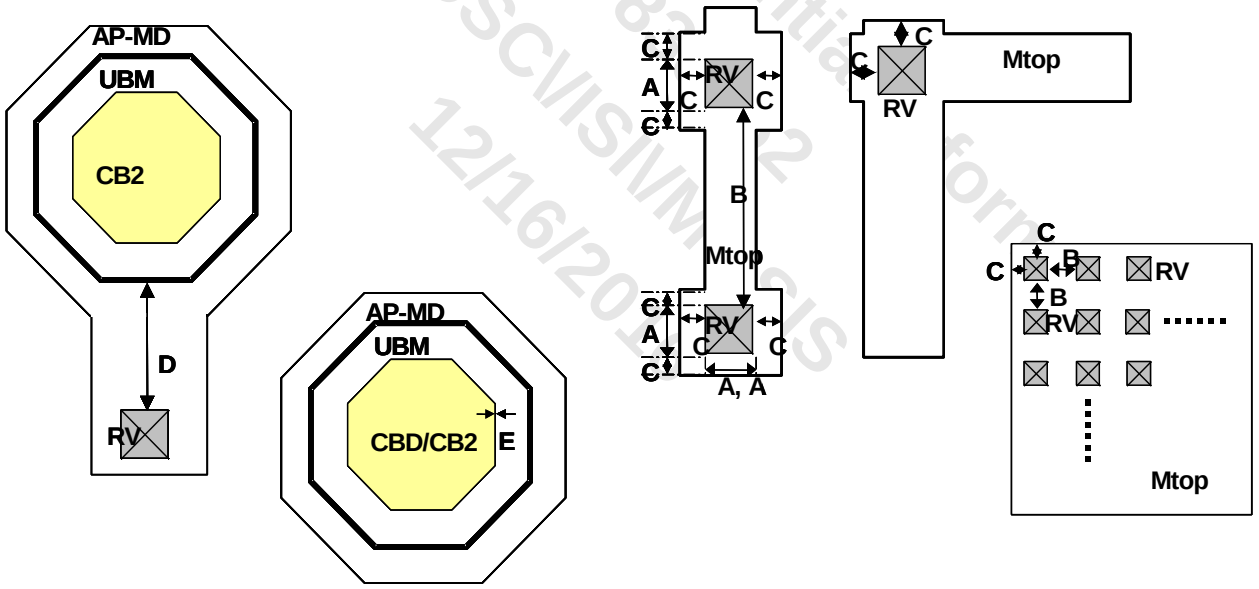
4.7.2 RV Layout Rules (Passivation-1 VIA Hole) for Flip Chip

- CB-VD mask (306) is generated by the logical operation of CBD (CAD layer: 169) or RV (CAD layer: 85).
- You must consider that RV counts can provide enough current for ESD requirements. Therefore, it is recommended to make as many RV holes as possible.

Rule No.	Description	Label		Rule
RV.W.1.FC	Width (Square) (maximum =minimum) {NOT INSIDE FW(AP) or seal ring}	A	=	3
RV.S.1.FC	Space	B	≥	3
RV.S.2.FC	Space to UBM [Overlap is prohibited]	D	≥	0
RV.EN.1.FC	Enclosure by Mtop {Not inside seal ring}	C	≥	1.5
RV.R.1.FC	A 45-degree rotated RV is prohibited. (Except WLCSP seal ring region)			
RV.R.3.FC	{CBD inside CB2} enclosure by CB2 (For ground-up design, CBD and CB2 must draw same size, and identical shape.)	E	=	0

RV:



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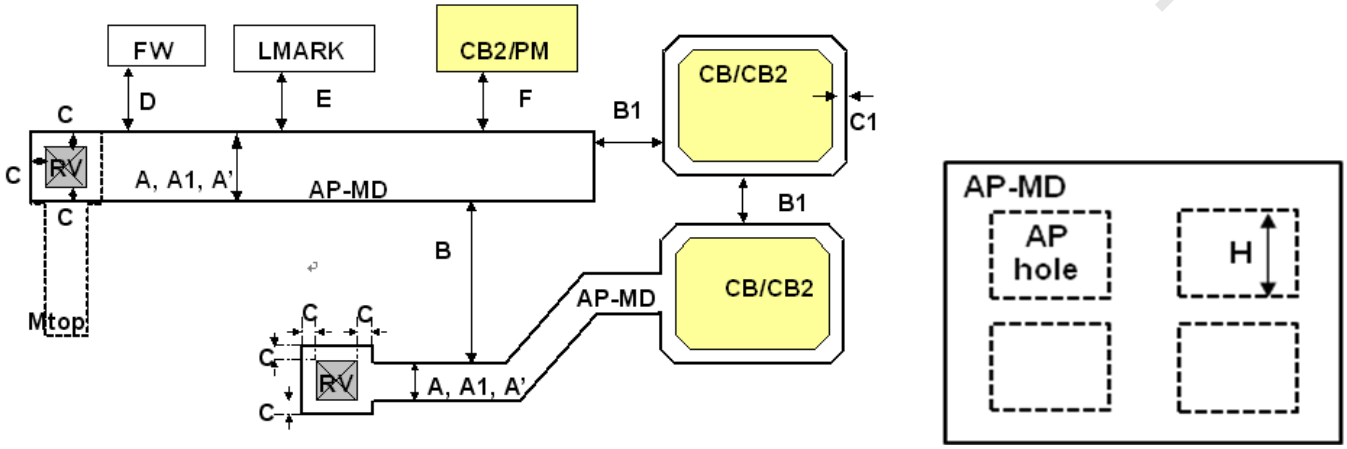
4.8 AP-MD Layout Rules

4.8.1 AP-MD Layout Rules for Wire Bond

Rule No.	Description	Label		Rule
AP.W.1.WB	Width {Interconnection only} {NOT INSIDE FW(AP) or seal ring}	A	≥	3
AP.W.2.WB	Maximum width {Interconnection only} {NOT INSIDE CB OR CB2}	A1	≤	35
AP.W.2.WB®U	Recommended total width of BUS line [Connect with bond pad]	A'	≥	10
AP.W.3.WB	AP hole width for 28KÅ AP, except < 100 inner 90-degrees vertex of AP holes [width < 3μm] within window 100μm x 100μm, stepping 50μm.	H	≥	3
AP.S.1.WB	Space (except space in the same polygon and in {CB2 SIZING 5um} region)	B	≥	2
AP.S.1.1.WB	{AP AND [CB2 sizing 3]} space to {AP AND [CB2 sizing 3]}, or space to AP routing (Except spacing in the same polygon)	B1	≥	2.5
AP.S.2.WB	Space to FW_CU/FW_AP [(Overlap FW_CU)/ (Cut FW_AP) is prohibited]	D	≥	5
AP.S.3.WB	Space to LMARK [Overlap is prohibited, except seal-ring]	E	≥	5
AP.S.4.WB	Space to CB2/PM [Overlap is prohibited, except bond pad region and seal ring]	F	≥	3.5
AP.EN.1.WB	Enclosure of RV {NOT INSIDE seal ring}	C	≥	1.5
AP.EN.2.WB	Enclosure of CB/CB2	C1	≥	1
AP.DN.1.WB	AP density across full chip		≥	10%
			≤	70%
AP.R.1.WB U	Maximum chip size for wire bond using AP-MD routing. Need to add polyimide layer for wirebond using AP-MD routing for die size >= 100mm^2.		≤	100 mm^2

AP-MD:



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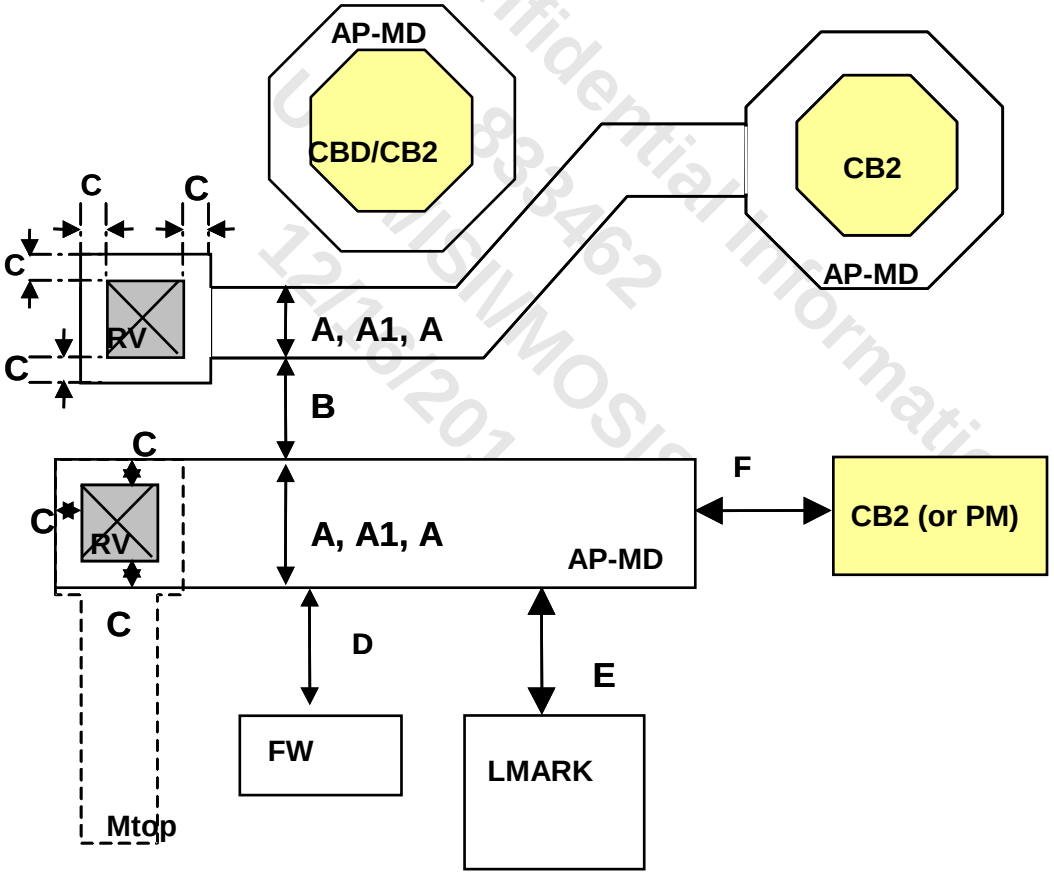
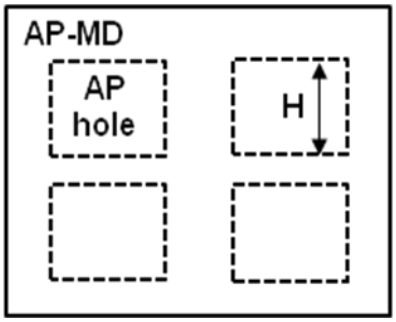
4.8.2 AP-MD Layout Rules for Flip Chip

Rule No.	Description	Label		Rule
AP.W.1.FC	Width {Interconnection only} {NOT INSIDE FW(AP) or seal ring}	A	≥	3
AP.W.2.FC	Maximum width {Interconnection only} {NOT INSIDE UBM, CBD or CB2}	A1	≤	35
AP.W.2.FC®U	Recommended total width of BUS line [Connect with bump pad]	A'	≥	10
AP.W.3.FC	AP hole width for 28KÅ AP, except < 100 inner 90-degrees vertex of AP holes [width < 3μm] within window 100μm x 100μm, stepping 50μm.	H	≥	3
AP.S.1.FC	Space (except space in the same polygon and in {UBM SIZING 5um} region)	B	≥	2
AP.S.2.FC	Space to FW_CU/FW_AP [(Overlap FW_CU)/ (Cut FW_AP) is prohibited]	D	≥	5
AP.S.3.FC	Space to LMARK [Overlap is prohibited, except seal-ring]	E	≥	5
AP.S.4.FC	Space to CB2/PM [Overlap is prohibited, except UBM region and seal ring]	F	≥	3.5
AP.EN.1.FC	Enclosure of RV {Not inside seal ring}	C	≥	1.5
AP.DN.1.FC	AP density across full chip		≥	10%
			≤	70%

AP-MD:





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5 Wire Bond, Flip Chip and Interconnection Design Rules

Please refer to T-000-CL-DR-017.

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6 N55 Design Information

6.1 Overview

This chapter provides all the rules and reference information for the design and layout of integration circuits using TSMC 55 nm CMOS LOGIC 1P9M (single poly, 9 metal layers), salicide, Cu technology.

- **TSMC offers N55 process** – 90% linear shrinkage from N65 layout dimension.
  - **CLN55GP:** Provides N65G/GP products with 90% linear shrinkage for the die area saving purpose. N55GP offers dual-gate oxide process for 1.0V core and, 1.8V, 2.5V, 3.3V I/O devices.
  - **CLN55LP:** Provides CLN65LP products with 90% linear shrinkage for the die area saving purpose. CLN55LP offers dual-gate oxide process for 1.2V core and 2.5V I/O devices.
  - **CMN55LP:** Based on CLN55LP process with extra process steps for mixed signal/ RF application. It includeds metal-oxide-metal (MOM) capacitor and ultra thick metal (Mu=UTM; 34KA) for inductor. CMN55LP is a low-power product for RF and mixed signal applications with a 1.2V core design, and with 2.5V I/O option.
- **TSMC offers one kind of inter-layer metal (Mx) and four kinds of top-layer metal (Mz/ My/ Mr/ Mu):**
  - Mx: Inter-layer Metal, W/S=0.1μm/0.1μm.
  - Mz (4XTM): top metal pitch is four times of Mx pitch (W/S=0.4μm/0.4μm).
  - My (2XTM): top metal pitch is two times of Mx pitch (W/S=0.2μm/0.2μm) for CLN55, not for CMN55.
  - Mr: top metal pitch is five times of Mx pitch (W/S=0.5μm/0.5μm) for CLN55, not for CMN55.
  - Mu: top metal for inductor metal of CMN55.
- **X-metal and second Inter-layer Metal (My) are not offered.**
- **TSMC N55 generation does not support MIM capacitor.**
- **You must complete all GDS and DRC related efforts in N65 level,** i.e. follow N65 design rules and N55 non-shrinkable rules to tape out. TSMC will shrink the GDS to N55 while mask making.

6.1.1 General Logic Design Specifications

- **The drawn dimension in N55** tape-out needs to follow N65 rules and the non-shrinkable rules of this chapter, then TSMC will have a 90% linear shrinkage during mask making.
- **Designers must assess the shrinkage impact** on critical circuits, such as PLL, analog and IO circuits.
- **Seal ring and chip corner stress relief pattern (CSR) are shrinkable.** If you want to draw your own seal ring and CSR, you need to follow the CLN65 seal ring and CSR rules in chapter 4.
- **Designers may consider a direct 110% size-up at the CLN65 level** to maintain the circuit performance (for example: matching circuits, current-driving at IO circuits).
- **It's recommended to use 1 nm design grid on 110% size-up IP layout to minimize the device layout mismatch due to data truncation or grid snapping.** It may occur 5nm layout mismatch when snapping the design grid to 5nm on 110% size-up circuit. You should pay attention on the performance impact on the size-up circuits, especially on OD and PO layout. Please refer to the " 110% Size-up" section 6.5.3 for details. You could also consult with the TSMC Design Support Department about the size-up procedure.
- **For newly developed IP, a compatible design for N65 and N55 is recommended. Please consider the following guidelines besides non-shrinkable rules**
  - 10nm design grid for critical device layout for both device parameters and device coordinates. Thus, avoid the device mismatch caused by grid snapping (no matter for 110% size-up or direct shrink flow).
  - Avoid using 45◦ lines. If 45◦ shape is necessary, use 10nm grid for both endpoints of 45◦ lines. Thus, avoid skewed lines no matter for size-up or direct shrink flow.

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6.1.2 SRAM Design Specifications

- **You can prepare SRAM by**
  1. **Consult with 3rd party venders; or**
  2. **Use TSMC's silicon proven SRAM bit cells (N55) to build the configuration; or**
  3. **Use self-own SRAM cell. Please contact TSMC to perform a mandatory bit cell review.**
- **The following SRAM cells are silicon proven in TSMC.**

Process Type	N55		
Cell Size (before shrunk) (N65 drawn dimension)	0.525um^2	0.62um^2	0.974um^2

- **Please follow SRAM rules and recommendations in the chapter 4.**

6.2 Non-shrinkable Layout Rules

6.2.1 Purpose:

A set of non-shrinkable rules are defined to meet the below requirements:

1. The limitation of the silicon process step, testing probing, laser repair and assembly.
2. Prevent DRC false errors from 110% size up steps.
3. Except the non-shrinkable rules in the following section, other rules (please refer to chapter 4) are shrinkable.

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6.2.2 Stress Migration and Wide Metal Spacing Rules Adjustment

- The rules listed in the below table are adjusted to avoid DRC false alarm on 110% size-up circuits.
- Except 110% size-up circuits, other circuits have to follow the stress migration and wide metal spacing rules in chapter 4. However, the following rules will be met automatically as long as rules in Chpater 4 are met.

Rule No	Description	Label		Rule
M1.S.2.S	Space [at least one metal line width > 0.22 µm (W1) and the parallel metal run length > 0.42 µm (L1)] (union projection)		≥	0.11
M1.S.2.1.S	Space [at least one metal line width > 0.465 µm (W2) and the parallel metal run length > 0.465 µm (L2)] (union projection)		≥	0.16
M1.S.2.2.S	Space [at least one metal line width > 0.20 µm (W1) and the parallel metal run length > 0.42 µm (L1)] (union projection)		≥	0.10
M1.S.2.3.S	Space [at least one metal line width > 0.42 µm (W2) and the parallel metal run length > 0.465 µm (L2)] (union projection)		≥	0.12
M1.S.3.S	Space [at least one metal line width > 1.65 µm (W3) and the parallel metal run length > 1.65 µm (L3)] (union projection)		≥	0.5
M1.S.4.S	Space [at least one metal line width > 4.95 µm (W4) and the parallel metal run length > 4.95 µm (L4)] (union projection)		≥	1.5
VIAx.R.2.S	At least two VIAx with space ≤ 0.22 µm (S1), or at least four VIAx with space ≤ 0.275 µm (S1') are required to connect Mx and Mx+1 when one of these two metals has width and length (W1) > 0.33 µm.			
VIAx.R.3.S	At least four VIAx with space ≤ 0.22 µm (S2), or at least nine VIAx with space ≤ 0.385 µm (S2') are required to connect Mx and Mx+1 when one of these two metals has width and length (W2) > 0.77 µm.			
VIAx.R.4.S	At least two VIAx must be used for a connection that is ≤ 0.8 µm (D) away from a metal plate (either Mx or Mx+1) with length > 0.33 µm (L) and width > 0.33 µm (W). (It is allowed to use one VIAx for a connection that is > 0.8 µm (D) away from a metal plate (either Mx or Mx+1) with length > 0.33 µm (L) and width > 0.33 µm (W).)			
VIAx.R.5.S	At least two VIAx must be used for a connection that is ≤ 2 µm (D) away from a metal plate (either Mx or Mx+1) with length > 2.2 µm (L) and width > 2.2 µm (W). (It is allowed to use one VIAx for a connection that is > 2 µm (D) away from a metal plate (either Mx or Mx+1) with length > 2.2 µm (L) and width > 2.2 µm (W).)			
VIAx.R.6.S	At least two VIAx must be used for a connection that is ≤ 5 µm (D) away from a metal plate (either Mx or Mx+1) with length > 11 µm (L) and width > 3.3 µm (W). (It is allowed to use one VIAx for a connection that is > 5 µm (D) away from a metal plate (either Mx or Mx+1) with length > 11 µm (L) and width > 3.3 µm (W)).			
Mx.S.2.S	Space [at least one metal line width > 0.22 µm (W1) and the parallel metal run length > 0.42 µm (L1)] (union projection)		≥	0.12
Mx.S.2.1.S	Space [at least one metal line width > 0.44 µm (W2) and the parallel metal run length > 0.44 µm (L2)] (union projection)		≥	0.16
Mx.S.2.2.S	Space [at least one metal line width > 0.2 µm (W1) and the parallel metal run length > 0.42 µm (L1)] (union projection)		≥	0.11
Mx.S.2.3.S	Space [at least one metal line width > 0.4 µm (W2) and the parallel metal run length > 0.44 µm (L2)] (union projection)		≥	0.13
Mx.S.3.S	Space [at least one metal line width > 1.65 µm (W3) and the parallel metal run length > 1.65 µm (L3)] (union projection)		≥	0.5
Mx.S.4.S	Space [at least one metal line width > 4.95 µm (W4) and the parallel metal run length > 4.95 µm (L4)] (union projection)		≥	1.5
VIAy.R.2.S	At least two VIAy with space ≤ 0.44 µm (S1), or at least four VIAy with space ≤ 0.55 µm (S1') are required to connect My and My+1 when one of these two metals has width and length (W1) > 0.66 µm.			

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Rule No	Description	Label		Rule
VIAy.R.3.S	At least four VIAy with space ≤ 0.44 µm (S2) are required to connect My and My+1 when one of these two metals has width and length (W2) > 1.54 µm.			
VIAy.R.4.S	At least two VIAy must be used for a connection that is ≤ 1.6 µm (D) away from a metal plate (either My or My+1) with length > 0.66 µm (L) and width > 0.66 µm (W). (It is allowed to use one VIAy for a connection that is > 1.6 µm (D) away from a metal plate (either My or My+1) with length > 0.66 µm (L) and width > 0.66 µm (W).)			
VIAy.R.5.S	At least two VIAy must be used for a connection that is ≤ 2 µm (D) away from a metal plate (either My or My+1) with length > 2.2 µm (L) and width > 2.2 µm (W). (It is allowed to use one VIAy for a connection that is > 2 µm (D) away from a metal plate (either My or My+1) with length > 2.2 µm (L) and width > 2.2 µm (W).)			
VIAy.R.6.S	At least two VIAy must be used for a connection that is ≤ 5 µm (D) away from a metal plate (either My or My+1) with length > 11 µm (L) and width > 3.3 µm (W). (It is allowed to use one VIAy for a connection that is > 5 µm (D) away from a metal plate (either My or My+1) with length > 11 µm (L) and width > 3.3 µm (W)).			
My.S.2.S	Space [at least one metal line width > 0.43 µm (W1) and the parallel metal run length > 1.1 µm (L1)] (union projection)		≥	0.24
My.S.3.S	Space [at least one metal line width > 1.65 µm (W2) and the parallel metal run length > 1.65 µm (L2)] (union projection)		≥	0.50
My.S.4.S	Space [at least one metal line width > 4.95 µm (W3) and the parallel metal run length > 4.95 µm (L3)] (union projection)		≥	1.50
VIAz.R.2.S	At least two VIAz with spacing ≤ 1.87 µm are required to connect Mz and Mz+1 when one of these metals has a width and length > 1.98 µm.			
VIAz.R.3.S	At least two VIAz must be used for a connection that is ≤ 5 µm (D) away from a metal plate (either Mz or Mz+1) with length > 11 µm (L) and width > 3.3 µm (W). (It is allowed to use one VIAz for a connection that is > 5 µm (D) away from a metal plate (either Mz or Mz+1) with length > 11 µm (L) and width > 3.3 µm (W)).			
Mz.S.2.S	Space [at least one metal line width > 1.65 µm (W1) and the parallel metal run length > 1.65 µm (L1)]		≥	0.5
Mz.S.3.S	Space [at least one metal line width > 4.95 µm (W2) and the parallel metal run length > 4.95 µm (L2)]		≥	1.5
VIAr.R.2.S	At least two VIAr with spacing ≤ 1.87 µm are required to connect Mr and Mr+1 when one of these metals has a width and length > 1.98 µm.			
VIAr.R.3.S	At least two VIAr must be used for a connection that is ≤ 5 µm (D) away from a metal plate (either Mr or Mr+1) with length > 11 µm (L) and width > 3.3 µm (W). (It is allowed to use one VIAr for a connection that is > 5 µm (D) away from a metal plate (either Mr or Mr+1) with length > 11 µm (L) and width > 3.3 µm (W)).			
Mr.S.2.S	Space [at least one metal line width > 1.65 µm (W1) and the parallel metal run length > 1.65 µm (L1)]		≥	0.65
Mr.S.3.S	Space [at least one metal line width > 4.95 µm (W2) and the parallel metal run length > 4.95 µm (L2)]		≥	1.50
DMx.S.3.S	Space to Mx (Overlap is not allowed) [Mx width > 4.95 µm and the parallel metal run length > 4.95 µm]		≥	1.5
DMx.S.3.1.S	Space to Mx (Overlap is not allowed) [Mx width > 1.65 µm and the parallel metal run length > 1.65 µm]		≥	0.5

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6.2.3 SRAM Rules

- Please refer to all the SRAM rules in the section “SRAM Rules” in chapter 4, except the rule listing in the following table.

Rule No	Description
SRAM.R.15	**CO_11 (30;11) is a must for CO mask tape-out in SRAM**. 1. If CO_11 exists, it must cover CO 2. CO_11 must be 0.09um x 0.09um 3. CO_11 must be exactly the same as CO 4. CO_11 must be fully covered by SRM (50;0) and SRAMDMY_0 (186;0)
SRAM.R.18	SRAMDMY_0 (186;0) must fully cover SRAMDMY_1(186;1).

6.2.4 Pad Rule for Wire Bond

- Since the pad rule is limited by testing and assembly capability, you has to check the layout dimension before 90% linear shrink.
- Single in-line and Staggered pad rule is non-shrinkable. The design rules Tri-tiers pad structure are shrinkable.
- Please refer to T-000-CL-DR-017.

6.2.5 Flip Chip Bump Rules

- The bumping rules for flip-chip design are critical on the bumping ball formation. You must meet the non-shrinkable rules before 90% linear shrink.
- The bump height and diameter would decrease due to UBM shrinking. You must evaluate this bump height change carefully.
- Please refer to T-000-CL-DR-017.

*** Warning:** For the design with a bump pitch 150~175um (after shrink), please consult with your assembly house in advance. Make sure that your assembly house is able to provide such substrates and the associated service for your smaller bump pitch design.

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6.2.6 AP Metal Fuse Rules

- Reference document: *T-000-CL-DR-005"TSMC AL FUSE (AP FUSE) DESIGN RULE FOR CU PROCESS"*
- "Long-length AP fuse" can allow 90% shrinking.
- "Short-length AP fuse" is non-shrinkable. Please follow the rule in the following table.
- L-mark is non-shrinkable. Please follow the rule in the following table.

6.2.6.1 Non-shrinkable Rules:

Rule No	Description		Rule
FU.L.1.1	Length of AP fuse between dog bone (Short-length AP fuse only)	≥	6.6
FU.S.1	Space of AP fuse (Short-length AP fuse only)	≥	4.18
LW.W.1	Minimum width of L-slot (11 um is recommended)	≥	11
	Maximum width of L-slot	≤	22
LW.L.1	Minimum length of L-slot (33 um is recommended)	≥	33
	Maximum length of L-slot	≤	55
LW.EN.1	LMARK enclosure of L-slot [in the direction of the L-slot length]	≥	13.2
LW.EN.2	LMARK enclosure of L-slot [perpendicular to the direction of the L-slot length]	≥	33

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6.3 Antenna Effect Prevention Layout Rules

Please refer to Antenna Effect Prevention Layout Rules in chapter 4.

6.4 Layout Guideline for Latch-up and I/O ESD

Please refer to chapter 10.

6.5 Design Flow For Tape-Out

6.5.1 How to shrink the existing N65 design

- **Designers must evaluate the following items when applying 90% linear shrinkage from an existing N65 design:**
  - All IP libraries require timing simulation and characterization with N55 spice models.
  - Perform full-chip timing, leakage simulation and characterization to ensure chip functionality and robustness (with enough design margin).
  - Assess the BEOL RC delay impact (by sec. 6.5.4.2 “RC Extraction Guidelines”), because the resistance of via-hole and sheet resistance (Rs) of metal line is higher in N55 as compared to N65.
- **SRAM replacement:** Designers must replace the N65 SRAM cell to N55 one. The following SRAM cells are proven by TSMC.

Process Type	N55		
Cell Size (Before shrunk) (N65 drawn dimension)	0.525um^2	0.62um^2	0.974um^2

  It is reminding to replace theSRAM cells with the N55 unit-cells, which also includes the dummy, strapping, boundary and twist cells. Please refer to the section 6.1.2 for the detail.
- **110% size-up:** For some analog circuits (for example: matching circuits, current-driving at I/O circuits), designers may consider 110% size-up at the N65 level in order to keep the circuit performance when shrink to N55.
- **It’s recommended to use 1 nm design grid on 110% size-up IP layout to minimize the device layout mismatch due to the data truncation or grid snapping.** It may occur 5nm layout mismatch when snapping to 5nm design grid on the 110% size-up circuit. You should pay attention on the performance impact on the size-up circuits, especially on OD and PO layout. Please refer to the “ 110% Size-up” section 6.5.3 for the details. You could also consult with the TSMC Design Methodology about the size-up procedure.
- **The layouts for N55 must follow non-shrinkable rules.** (Please refer to section 6.2 “Non-shrinkable Layout Rules”.)

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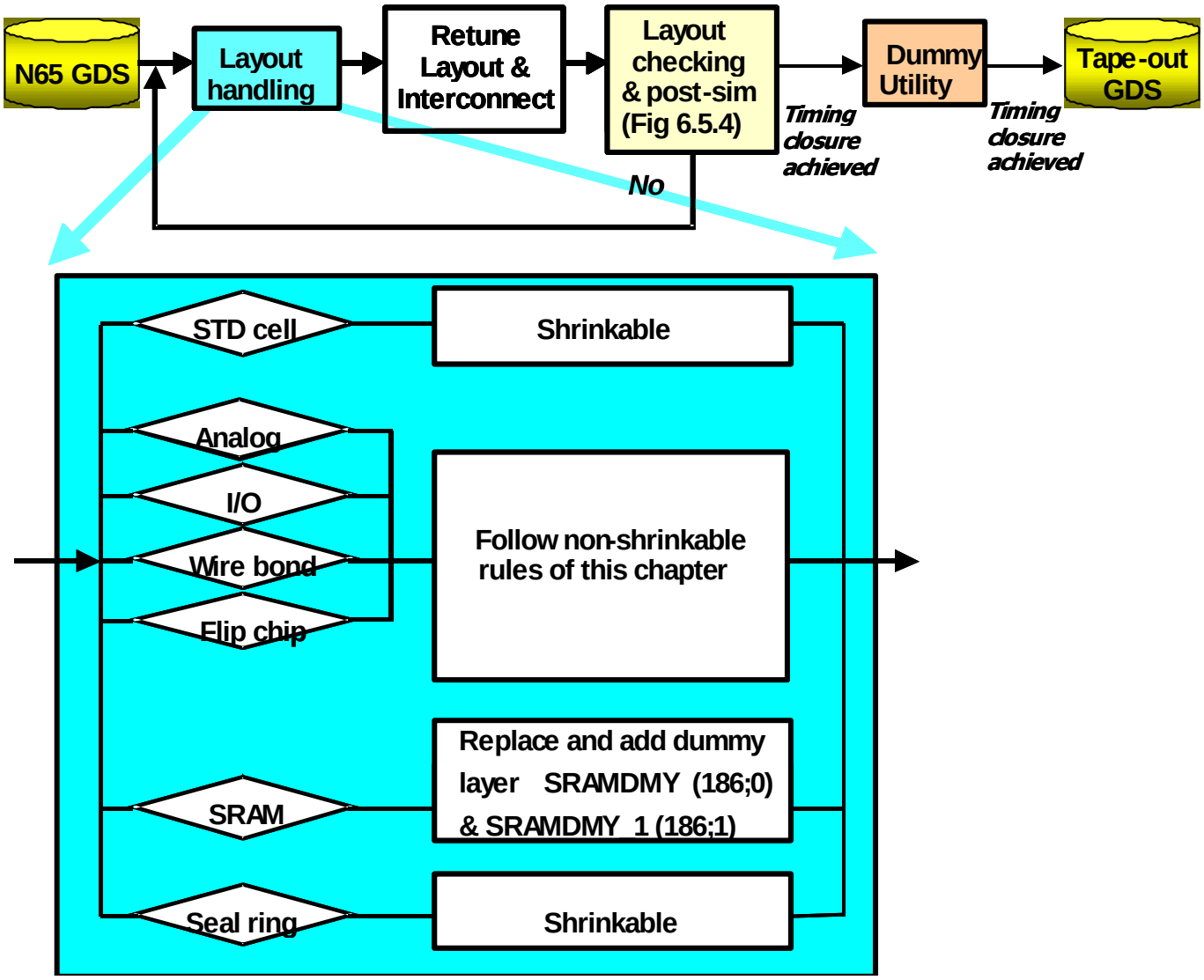
Figure 6.5.1 Shrink an existing N65 design to N55



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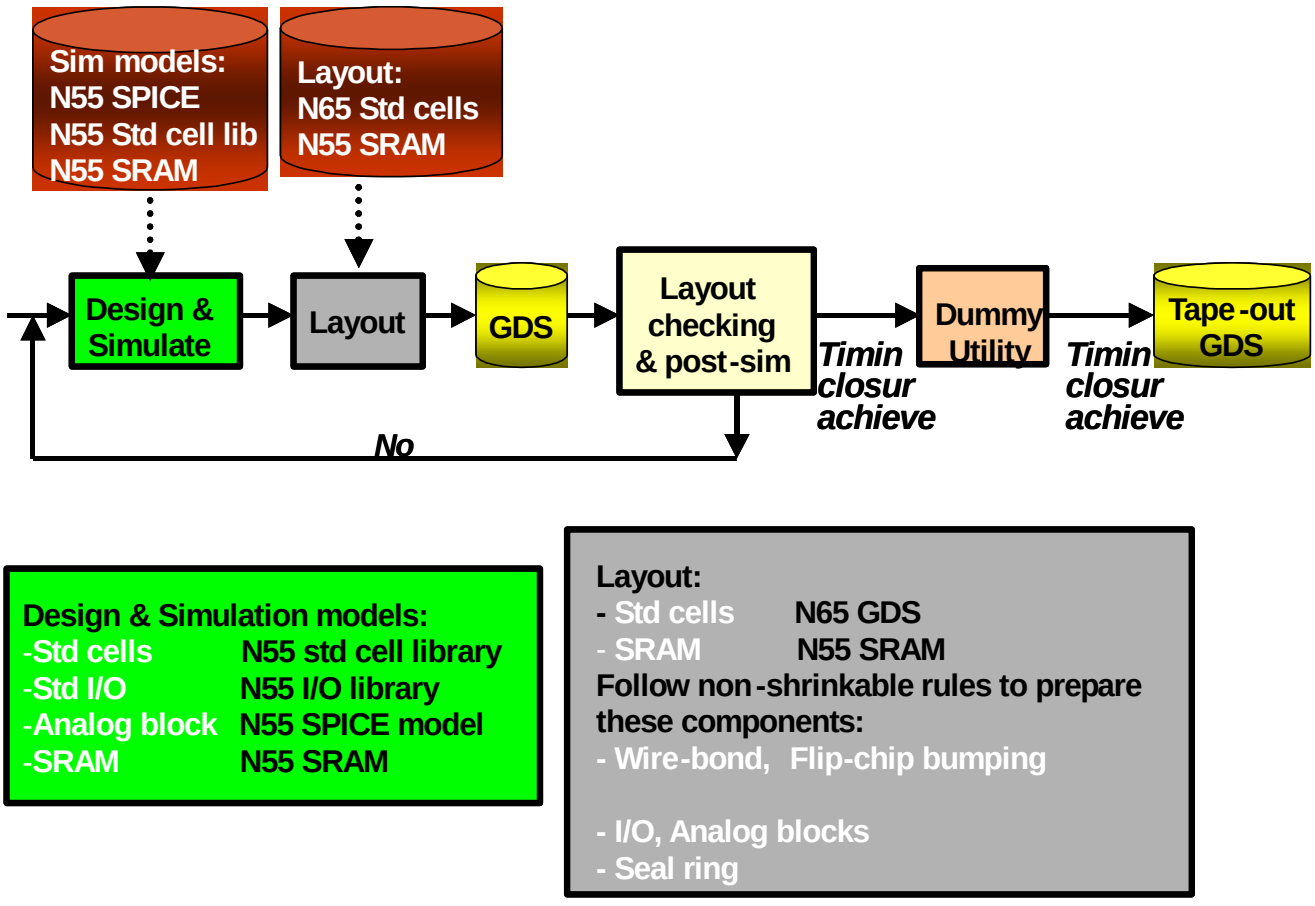
6.5.2 How to prepare a new design of N55

To start a whole new N55 design (that is, there is no existing N65 product to shrink from), please follow the design flow in Figure 6.5.2.

- **TSMC provides SPICE models, standard cell libraries, I/Os, and SRAM models in N55.**
- **Chip designers should follow the same timing sign-off flow as N65. Circuit designers should simulate their IP as described in section 6.5.4, paying attention critical circuits.**

Figure 6.5.2 Start a N55 new tape-out.



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6.5.3 110% size-up

- **If you have difficult to solve the data truncation or grid snapping problem by 5nm grid at the design stage, you can snap the design grid size to 1nm to minimize the device layout mismatch risk.**
- **Snap to 1nm grid size is only especially for the matching device.You still have to use 5nm grid for the 110% size-up on other circuit.**
- **If you snap the design grid size to 5nm in the size-up circuits, the device layout may occur 5nm mismatch.** You should pay attention to the performance impact on the size-up circuits, especially on OD and PO layout. Please refer to the mismatch impact ratio in the following table.

Design grid size	Mismatch after grid snapping	Mismatch after mask making	OD/PO layout dimension				
			0.06um	0.08um	0.1um	0.5um	1.0um
10nm	0 nm	0.5 nm	0.83%	0.63%	0.5%	0.1%	0.05%
5nm	1 nm	1 nm	1.67%	1.25%	1.00%	0.2%	0.1%

- **110% size-up procedure:**
  - **Prepare N65 IP:** Given N65 layout GDSII, which is clean on N65 DRC/LVS check.
  - **Stream-in:** Stream into layout editor database with precision 0.1nm (adding 1 more digit for database precision)
  - **Size-up 110%:** Size up layout by 110% in layout database
  - **Size-down CO/VIA:** Size down all CO/VIA layers to make CO/VIA size to be the same as before size-up. Thus, CO/VIA sizes comply with DRC.
  - **Flatten and merge polygons:** Flatten and merge polygons for avoiding gaps or jogs happening after grid snapping.
  - **Stream-out:** If you have the critical devices in the size-up circuits, please stream out and snap all co-ordinates to 1nm design grid.
  - **Fill dummy pattern manually or by using tsmc's utility.**
  - **Run N55 DRC/LVS check:** Check the size-up circuits by 1nm grid size in DRC command file†. If there are any DRC violations, modify layout to fix these violations.

    † Fill the cell name of size-up circuits behind the 1nm grid check variable in DRC command file. (Don't need to fill the cell name, if you snap to 5nm design grid). The variable of cell selection for 1nm grid check is listed below:

    CellsFor1nmGrid "cell1 name" "cell2 name" "cell3 name"…
- **Chip integration for size-up and direct-shrink circuits:**
  - **Direct-shrink part:** Circuits of direct-shrink part keeps 5nm design grid, same as N65 requirement.
  - **110% Size-up part:** Circuits of 110% size-up part use 1nm design grid.
  - **Run N55 DRC/LVS check:** Please fill the cell name of 110% size-up circuits behind the 1nm grid check variable in DRC command file (Don't need to fill the cell name, if you use 5nm design grid in 110% size-up circuits). Then, 110% size-up circuits will be checked by 1nm grid size and the other direct shrink circuits will be checked by 5nm grid size. If there are any DRC violations, modify the layout to fix these violations.
- **Please refer to Figure 6.5.3 for the 110% size-up flow chart**

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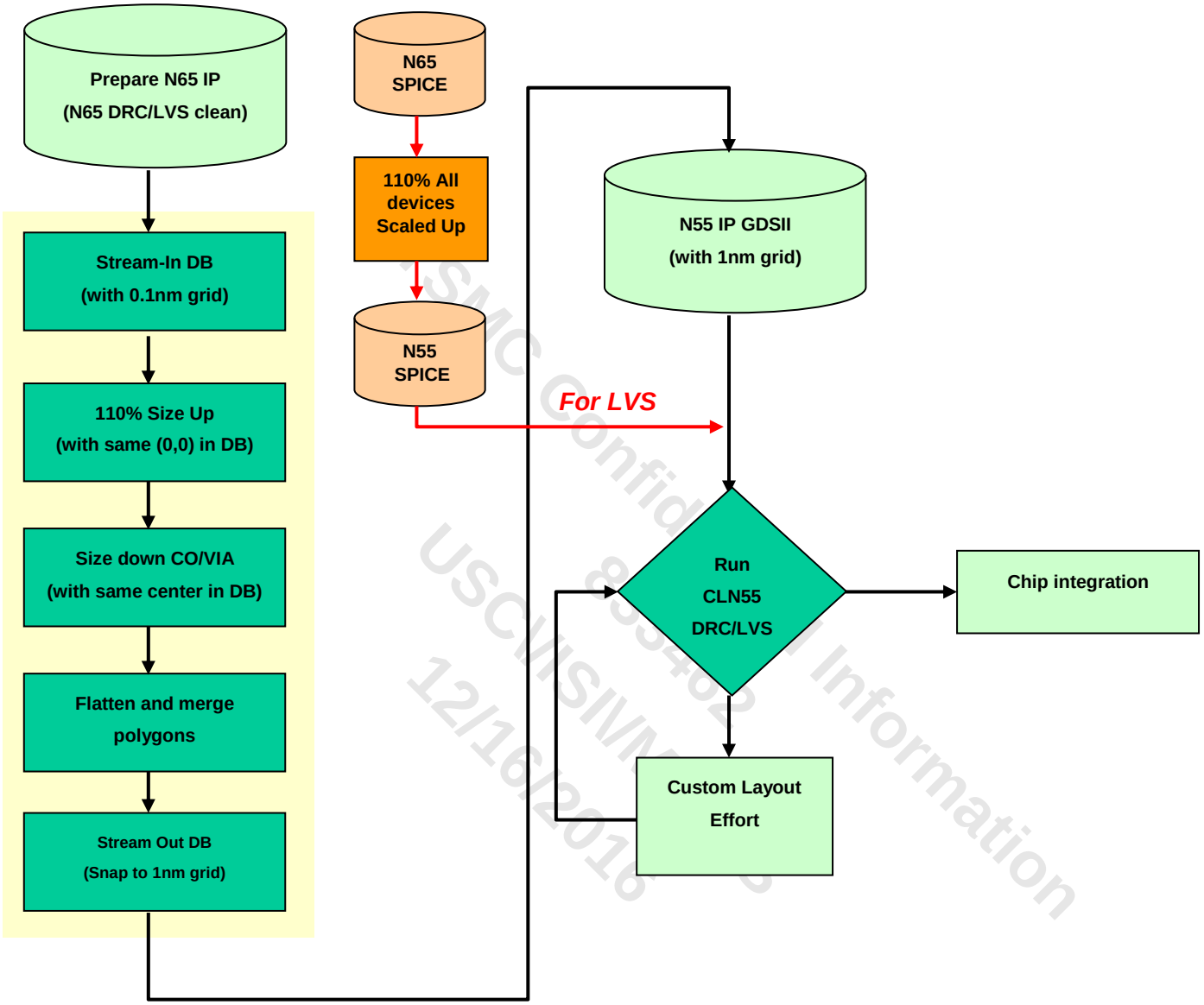
Figure 6.5.3 Flow Chart of Size-up Procedure



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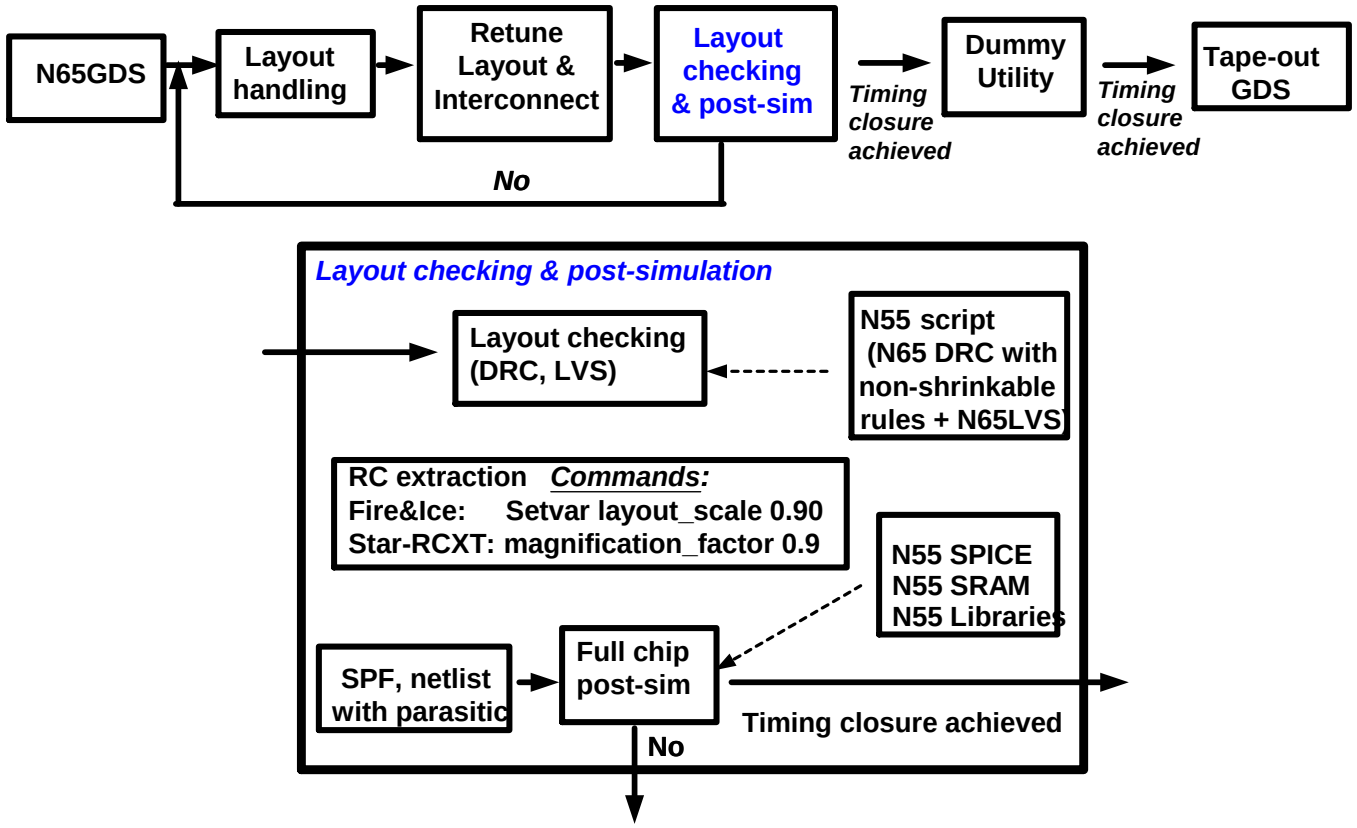
6.5.4 Layout check and post simulation

When the layout is ready, the designer should look for possible DRC violation and do an LVS check. Figure 6.5.4 shows the sequence.

- **If it passes DRC & LVS, perform the RC extraction by the commands given. Perform full-chip simulation on the extracted net-list (with parasitic).**
- **If timing closure is achieved, it is ready for tape-out. Otherwise, re-design, re-layout or make other adjustments as needed to meet the timing goals.**

By enabling the option of the scale factor (0.9) in RC extractor, the output of the **N55 RC extractor** will be N55 parasitics. Please refer 6.5.4.2 for RC extraction setting of IP-level and chip-level extraction.

Figure 6.5.4. Layout check and post simulation.



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6.5.4.1 SPICE Guidelines for Library IP Development

- **TSMC provides N55 logic and SRAM models, which designers can use to do pre-sim and post-sim for the circuits.**
- **Outline for both existing N65 design migration and new N55 design**
  1. At pre-sim stage, scale=0.9 must be added in the net-list if the device size is in N65 dimension.
  2. At post-sim stage, LPE will extract device size based on layout dimension and RC extractor will take care of parasitic extraction scaling. The device size is still in N65 dimension but parasitics is extracted based on 90% shrunk layout. As a result, scale=0.9 should be added in net-list for N55 simulation since it only impacts MOS, DIO geometry but not on parasitics With this extraction flow, pre-sim and post-sim environments are the same. Thus, it's easier for design integration and LVS back-annotation for debugging. .
- **Simulation Syntax for scaling (HSPICE only):**

1. The Following is an example for MOS and DIODE lib.

```
.option post tnom=25 ingold=2 numdgt=6 scale=0.9
```

2. For the part of resistors and varactors, scale factor is put in spice model header. It's suitable for both pre-layout and post-layout simulation. Please refer to the example below.

```
***** Macro Model Resistor & Capacitor (or Varactor) *****
.LIB scale_option_res
.param scale_res= 0.9
.ENDL scale_option_res

.LIB scale_option_cap
.param scale_cap=0.9
.ENDL scale_option_cap

.LIB scale_option_cap25
.param scale_cap25=0.9
.ENDL scale_option_cap25
```

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3. There are also flags in SPICE model header for contact to poly gate resistance estimation in pre-layout stage.

```
***** Contact-to-poly parasitics *****
.LIB CCO_pre_simu
.param ccoflag=1
.ENDL CCO_pre_simu

.LIB CCO_pre_simu_hvt
.param ccoflag_hvt=1
.ENDL CCO_pre_simu_hvt

.LIB CCO_pre_simu_25
.param ccoflag_25=1
.ENDL CCO_pre_simu_25

.LIB CCO_pre_simu_na
.param ccoflag_na=1
.ENDL CCO_pre_simu_na

.LIB CCO_pre_simu_na25
.param ccoflag_na25=1
.ENDL CCO_pre_simu_na25
```

4. BJT model is not a scalable model, so users can't specify "area" in the net-list. The model is not affected by value of scale and has already been extracted from a shrunk size.

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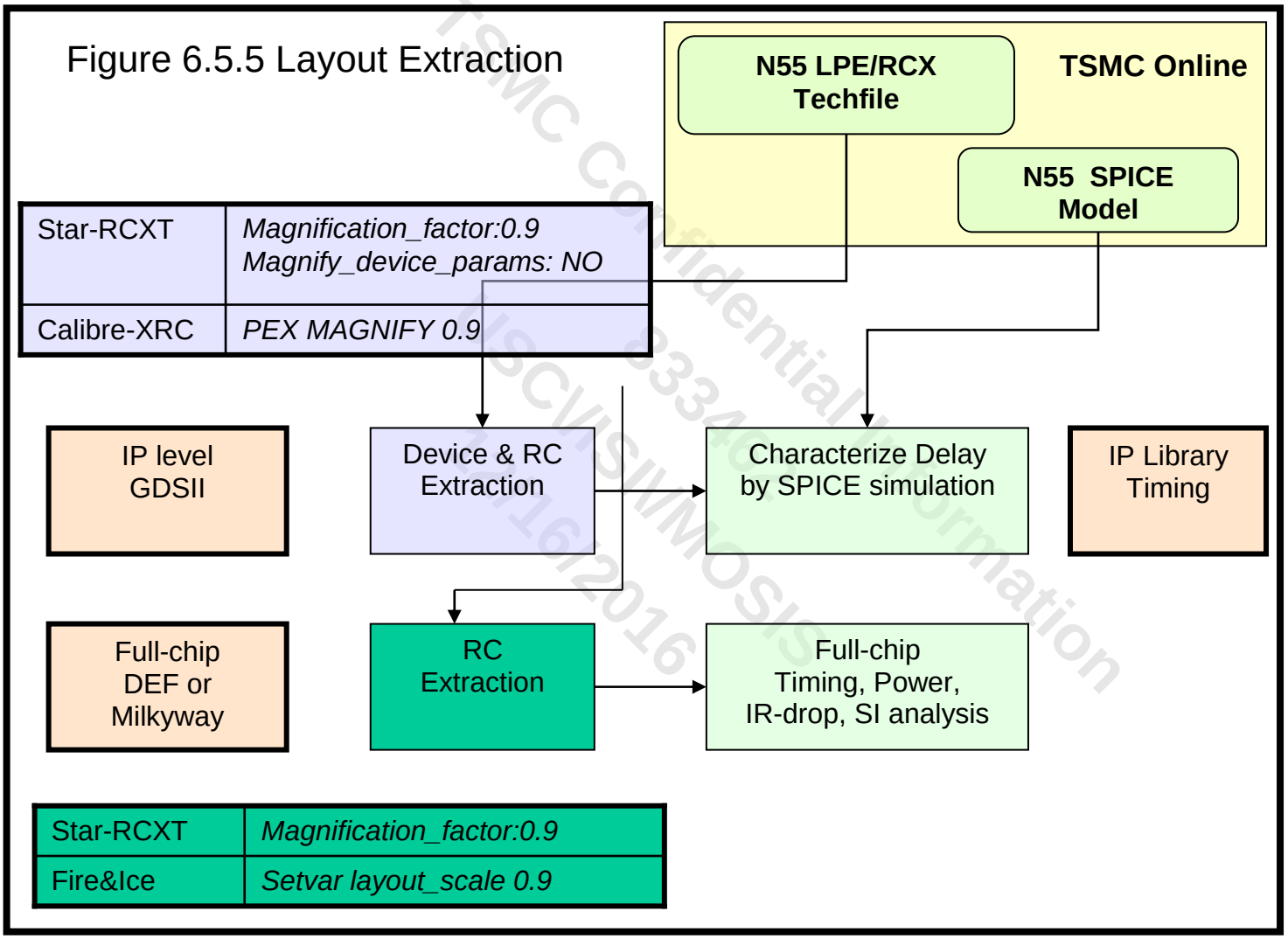
6.5.4.2 RC Extraction Guidelines

- **Designers must assess RC delay impact (by N55 RC layout extraction) since the via resistance and metal Rs are higher than N65.**
- **For IP libraries extraction, there are WPE , DFM switches on transistors parameters for more accurate circuit simulation**
- **Full-chip timing and leakage simulation/characterization are required to ensure chip functionality and robust yields.**
- **Layout extraction procedure (Figure 6.5.5):**

Figure 6.5.5 Layout Extraction



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7 Layout Rules and Recommendation for Analog Circuits

This chapter provides information about the following topics:

7.1 User guides

7.2 Layout rules for the WPE (well proximity effect)

7.3 Layout guidelines or LOD (length of the OD region) effect

7.4 Layout rules, recommendations and guidelines for the analog design

7.5 Layout rules and guidelines for device placement

7.6 Burn-in guidelines for analog circuits

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7.1 User Guides

1. Use these rules, recommendations, and guidelines to achieve better analog device performance and matching. In analog circuits, good device matching provides good performance margin and production yield.
2. The examples of analog circuits:
   - **Operational Amplifier:** includes differential input pair, bias circuit and current mirror.
   - **DAC:** includes constant current source, amplifier using external Rset to adjust full range current and bias circuit.
   - **ADC:** includes comparator, amplifier, sample/hold switches, switching capacitor, and reference voltage resistor ladder.
   - **PLL:** includes VCO (delay stage) and charge pump (current mirror, buffer/opamp)
   - **Bandgap:** BJT, current mirror, bias circuit, differential amplifier and ratioed resistor.
   - **LNA and mixer**
   - **Sense amplifiers in memories.**
   - **Matching pair** includes active and passive devices.
3. If your circuit has concern about the rules, recommendations, and guidelines, TSMC DRC deck can help you to flag the violations. Analog DRC deck is bundled in the TSMC logic DRC deck. The following two methods can specify the region to run analog part. Please also refer to the user guide in the DRC deck.
   - **Dummy layer:**
     - RRuleAnalog (CAD layer: 182;3): for the layout rules, recommendations, and guidelines of the analog designs.
   - **Cell selection based on the following variable:**
     - CellsForRRuleAnalog: only check the cells in the variable
     - ExclCellsForRRuleAnalog: don't check the cells in the variable
4. A registered symbol "^{U}" is marked after the rule number as the rule is not checked by DRC.

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7.2 Layout Rules for the WPE (Well Proximity Effect)

NMOS or PMOS very close to well edge will exhibit a difference in threshold and Id from that of the device located remotely from well edge.
For the sensitive circuit, e.g. constant current source or differential input pair, which needs precise device parameter control like △Vt <5mV and △Id<2%, please follow the subsequent four layout rules for WPE.

Rule No.	Device		Dimension
PO.S.14m	Gate space to (OD2 OR (NW OR NT_N)) in Core NMOS	≥	1.0
PO.EN.1m	Gate enclosure by ((NW NOT OD2) NOT NT_N) in Core PMOS for 3.3V IO process.	≥	1.0
	Gate enclosure by (NW NOT NT_N) in Core PMOS for 1.8V/2.5V IO process.	≥	1.0
PO.EN.2m	Gate enclosure by (OD2 NOT (NW OR NT_N)) in IO NMOS.	≥	2
PO.EN.3m	Gate enclosure by ((NW AND OD2) NOT NT_N) in IO PMOS for 3.3V IO process.	≥	1.5
	Gate enclosure by (NW NOT NT_N) in IO PMOS for 1.8V/2.5V IO process.	≥	1.5

1. For the dimension smaller than the above rules, the V_t of MOS device is raised as well as the Id is degraded. This effect increases with the reduction of the space or enclosure dimension.
2. The WPE phenomenon occurs to every MOS: standard V_t, high V_t, low V_t , thin oxide MOS and thick oxide MOS.
3. If the above dimension is impossible to comply in the critical circuit requiring tight matching in threshold voltage or Id, identical layouts with identical well enclosure dimension should be kept. (Figure 7.2.1)
4. If the distance between gate and well is the same, the WPE impact from the poly end cap direction is smaller than that from the source/drain direction.
5. SPICE model has included the WPE effect. Users need to input SC in the netlist to activate these new features during pre-simulation. During post-simulation LPE will automatically extract the SC from layout, and add the extracted SC to the netlist, then activate the model properly. (SC is the distance between gate and Well edge, please refer to the Appendix in the SPICE document).
6. The detailed information regarding the device parameter impact by one side neighboring Well, or two sides or four sides is as the following.

	Core N/PMOS		IO N/PMOS	
	△Vt <5mV	△Id<2%	△Vt <5mV	△Id<2%
1 side	≥ 0.8um	≥ 1.0um	≥ 2.0um/ ≥ 1.5um	≥ 1.2um/ ≥1.0um
2 sides	≥ 1.2um	≥1.5um	≥2.5um	≥ 1.5um
4 sides	≥ 2.0um	≥ 2.5um	≥ 3.5um/ ≥3.0um	≥ 2.5um

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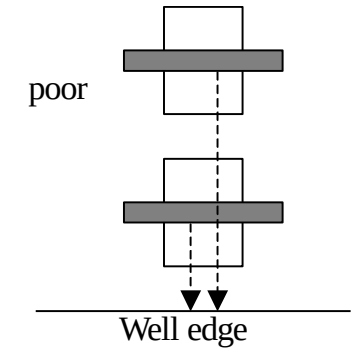

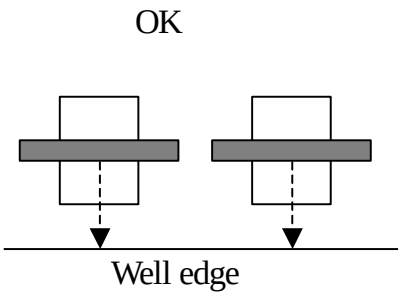

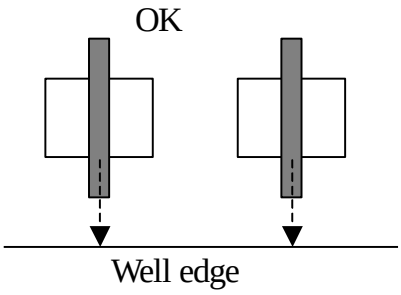

For example, to meet ΔVt <5mV in core N/PMOS,
please keep gate space to well edge ≥ 2.0um in 4 sides.

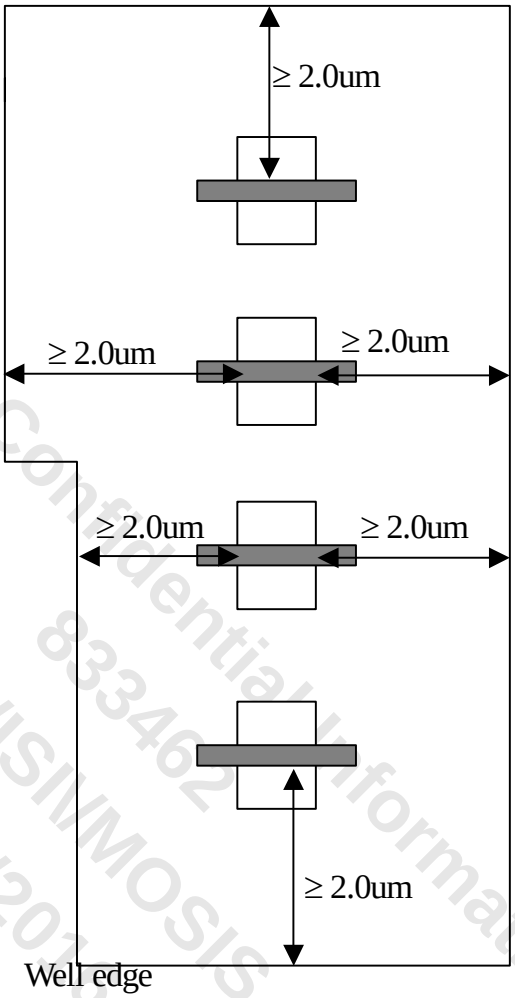

Figure 7.2.1 Device Placement for Matching Pairs

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7.3 Layout Guidelines for LOD (Length of the OD region) Effect

7.3.1 What is LOD?

1. The device performance (Vt or Id) will be impacted by LOD effect. It is due to the different mechanical stress induced by the different OD length.
2. SPICE model has included the LOD effect. Users need to input SA and SB in the netlist to activate these new features. (SA and SB are the distance between gate to OD edge). (Figure 7.3.1)

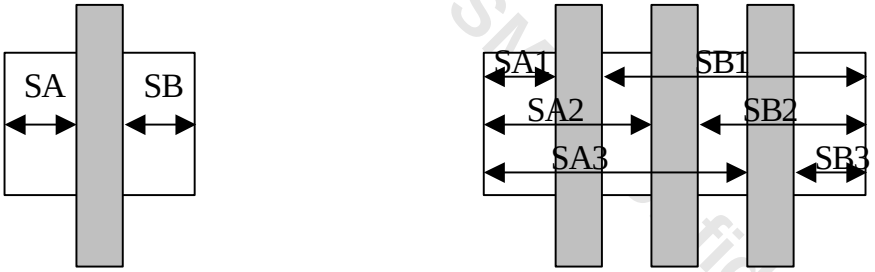

Figure 7.3.1 Example of SA and SB

7.3.2 Id change due to different SA

1. The drain current of MOS core or IO device shows complex SA (or SB) dependence. (Figure 7.3.2)

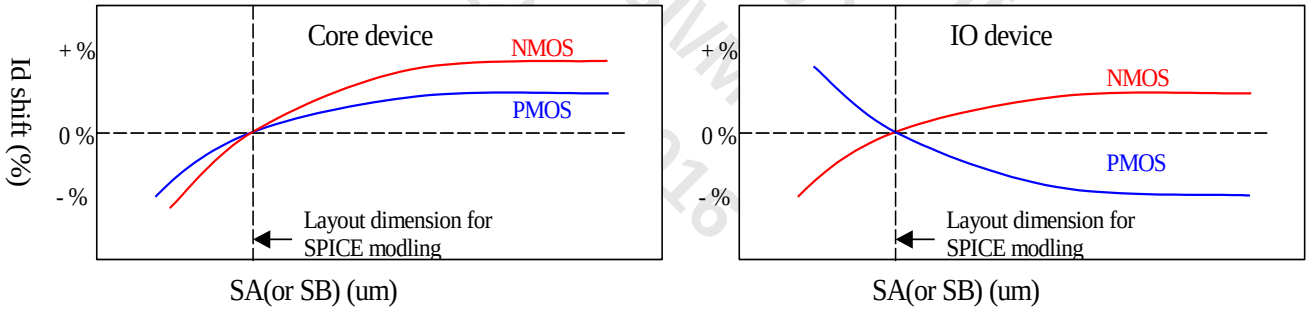

Figure 7.3.2 Id shift (%) due to different SA in NMOS/PMOS

2. Based on item 1, the Id of core device and IO NMOS of a multi-finger device is higher than that of a series of single gate. (Figure 7.3.3)

	SB	Id of Core device	Id of IO NMOS	Id of IO PMOS
Multi-finger device	larger	larger	larger	smaller
Single-gate device	smaller	smaller	smaller	larger

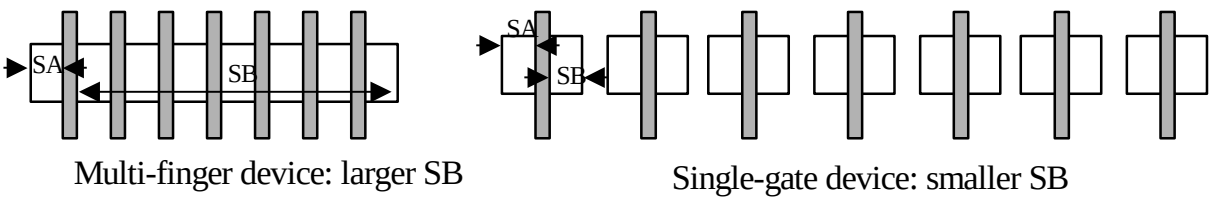

Figure 7.3.3 Id difference between multi-finger device and single-gate device in NMOS/PMOS

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7.3.3 How to have a precise LOD Simulation

1. For pre-sim cases
   - PDK: Every MOS device in PDK has a layout view. So, when you use TSMC PDK to do design, the corresponding pcell layouts are also ready. TSMC PDK includes Skill code which can estimate the SA and SB values from the corresponding pcell before real layouts. The pre-sim netlist will include the accurate SA and SB parameters.
   - If you do not use PDK cell, you need to estimate the SA and SB first, and put them into the netlists as transistor instance parameters.

   SA and SB are 0.405μm for core device and 0.46μm for IO device in the layout of test structure for TSMC SPICE model generation. If you use the above dimension precisely during layout design, the LPE will not do any LOD correction.
2. For post-sim cases (layouts are ready), designers need to use TSMC LPE deck to extract the SA and SB directly from layouts. The LPE will automatically add the extracted SA and SB to the netlists and thus the simulators will then activate the models properly.
3. Avoid the irregular OD layout for the model simulation accuracy concern. (Figure 7.3.4)

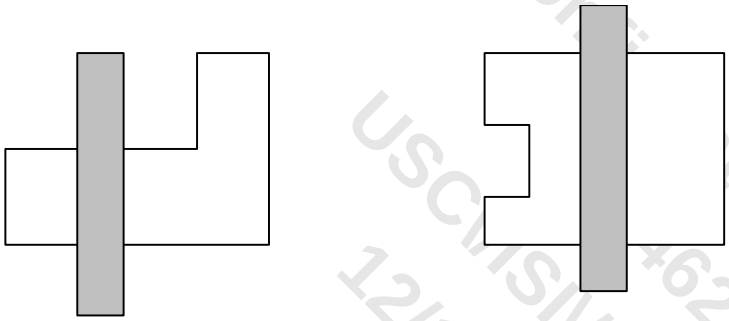

Figure 7.3.4 Irregular OD

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7.4 Layout Rules, Recommendations and Guidelnies for the Analog Designs

7.4.1 General Guidelines

Guideline No.	Description
AN.R.1mg^{U}	If possible, use devices with large widths. Do not use minimum widths and lengths for performance-critical device. Using current source device as an example, designer should refer to the device I-V curve to check at which W/L range, the drain saturation current reaches constant.
AN.R.2mg^{U}	Use larger areas for transistors, resistors, and capacitor devices for better mismatch..
AN.R.34mg^{U}	It is recommended to adopt all the advisory number of the DFM Action-Required Rules, and also adopt all the parametric/systematic related DFM Recommendations/Guidelines.
AN.R.35mg^{U}	Prefer simple shapes (rectangles) of OD and Poly.
AN.R.36mg^{U}	Avoid OD routing (prefer using metals and Co) to limit the number of corner OD (risk of OD rounding), and to limit the number of narrow OD connections (risk of OD Rs variation)

7.4.2 MOS Recommendations and Guidelines

Recommendation No.	Description			Recommended	Min. Rule
PO.S.5m®	Recommended PO space to L-shape OD when PO and OD are in the same MOS for model simulation accuracy	J	≥	0.2 (all dimension).	0.1 (channel width < 0.15)
PO.S.6.m®	Recommended L-shape PO space to OD when PO and OD are in the same MOS	E	≥	0.1 (all dimension).	0.1 (channel width < 0.15)
PO.EX.2mg^{U}	For current mirror devices using common OD, please pay attention to LOD effect (please refer to section 5.3), eg. when using common OD, please follow the following items: • Keep the same SA/SB • Enlarger extension (F1) to put dummy gate at both source/drain sides with the same channel width, length, pitch and count, as possible.				
AN.R.45mg^{U}	It is recommended not to use a very long channel device in the design. In order to ensure the channel relaxation time of the MOS device is enough to build up charge to the steady state, it is recommended to use <10 times of minimum channel length at the high operation frequency range. The operating frequency shall be below 0.2 * gm / Cgate, where gm is the transconductance of the transistor and Cgate is the gate-oxide capacitance.				

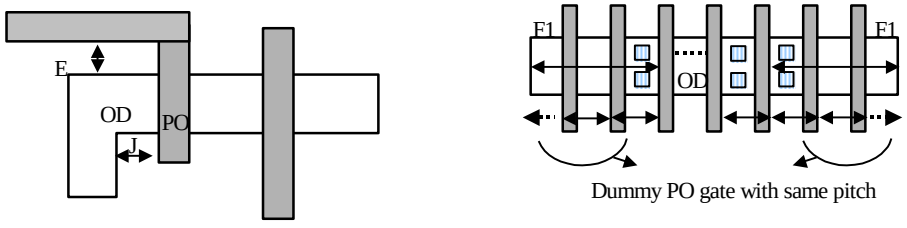

Figure 7.4.2 Analog Circuit Layout

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7.4.3 Parasitic Bipolar Transist or (BJT) Rules and Recommendations

1. Two kinds of vertical bipolar are provided, PNP bipolar (P+/NW/PSUB) and NPN bipolar (N+/PW/DNW).
2. TSMC offer two set of BJT models. Refer to below table:

(1) Model-1 with traditional layout (previously generation layout like)

Model name	PNP10 and NPN10	PNP5 and NPN5	PNP2 and NPN2
Emitter size	10x10	5x5	2x2
Base size	16x16	11x11	8x8
BJT dummy layer CAD number	BJTDMY (110;0)	BJTDMY (110;0)	BJTDMY (110;0)

(2) Model-2 with small BJT for CLN65LP process only. (keep emitter size, minimize collector and base layout area)

Model name	PNP10_S and NPN10_S	PNP5_S and NPN5_S	PNP2_S and NPN2_S
Emitter size	10x10	5x5	2x2
Base size	11.8x11.8	6.8x6.8	3.8x3.8
BJT dummy layer CAD number	BJTDMY (110;0+110;1)	BJTDMY (110;0+110;1)	BJTDMY (110;0+110;1)

3. In order to have precise SPICE model prediction, it is strongly recommended that users should apply the standard TSMC bipolar layouts in their designs. The layout could be accessed from tsmc SPICE model document or tsmc PDK.
4. The entire device needs to be covered with an BJTDMY (CAD layer: 110) which is used for DRC and LVS check.

Rule No.	Description	Label		Rule
BJT.R.1	RPO needs to cover 0.3um on the Emitter OD edge for both OD and STI sides, i.e. RPO= ((Emitter OD sizing 0.3) NOT (Emitter OD sizing -0.3))	F	=	0.6
BJT.R.8	{RH OR BJTDMY} enclosure of Emitter OD	G	≥	0.13
BJT.R.2®	OD (Emitter size) is 2μm x 2μm, 5μm x 5μm, 10μm x 10μm,	A	=	

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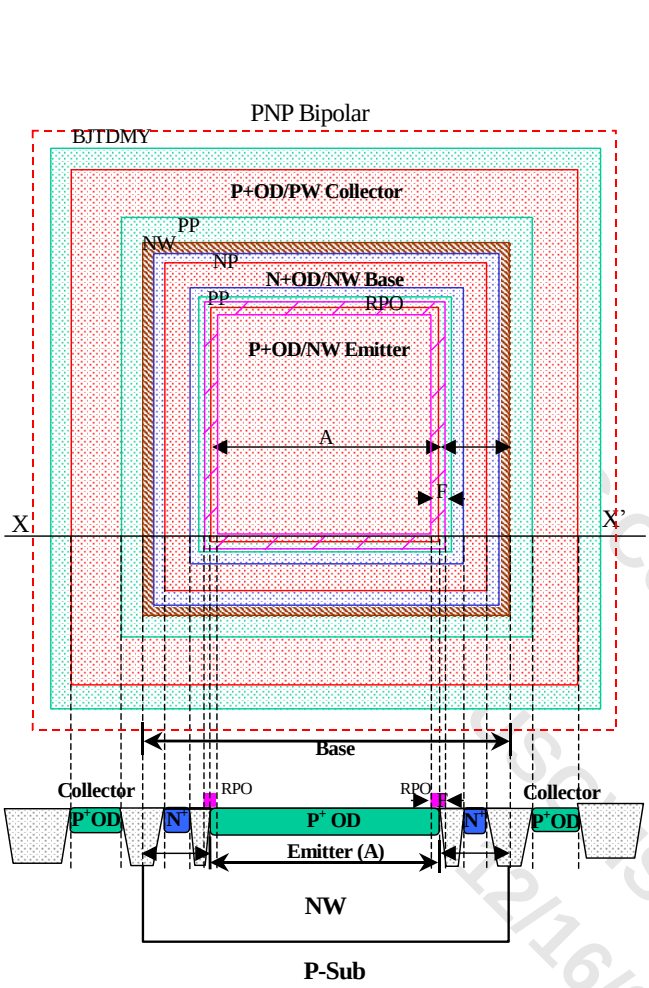

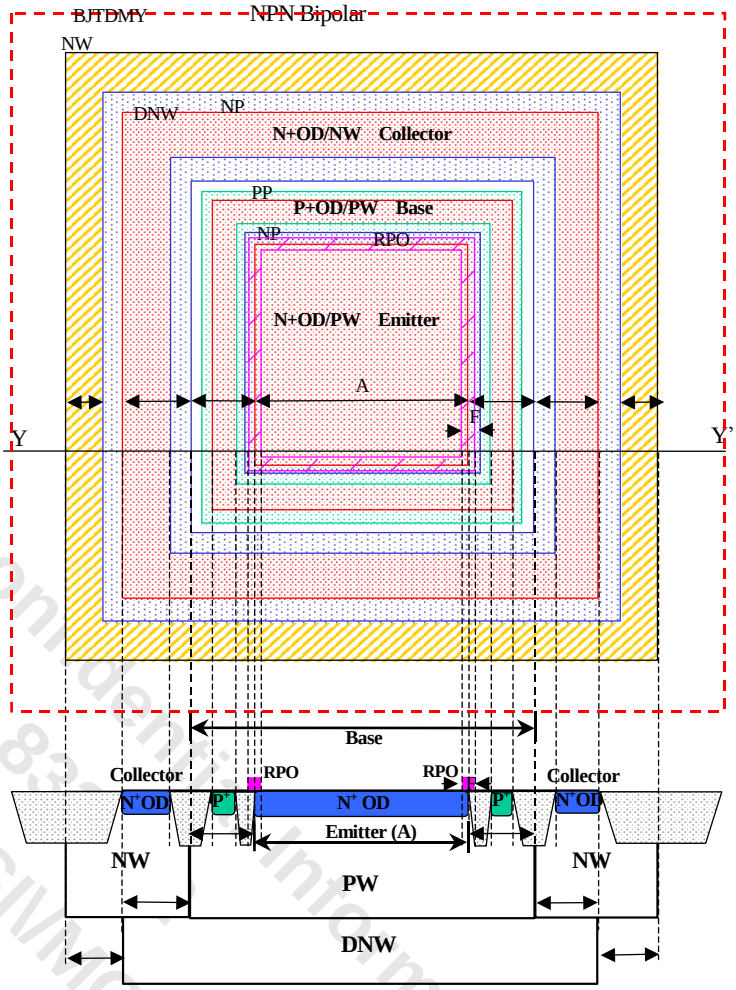

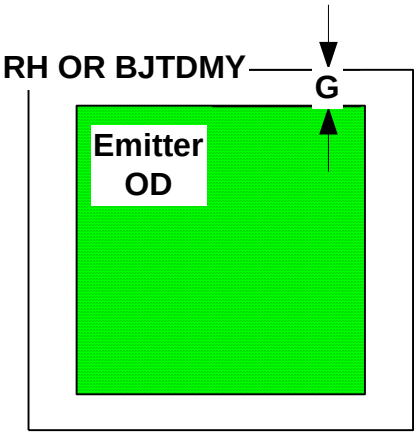

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7.4.4 Resistor Rules and Recommendations

Rule No.	Description	Label		Rule
RES.2m	Width (W) ≥ 0.4um, length (L) ≥ 0.4um, and square number (L/W) ≥ 1 for unsilicided OD/PO resistor. DRC can't check the square number.			
RES.5m®	Recommended CO space to unsilicided OD/PO resistor = 0.22 (S) for SPICE simulation accuracy.			
NWROD.R.1m	Width (W') ≥ 1.8um, length (L') ≥ 20um, and square number (L'/W') ≥ 5 for NW resistor within OD. DRC can't check the square number.			
NWRSTI.R.1m	Width (W") ≥ 1.8um, length (L") ≥ 20um, and square number (L"/W") ≥ 5 for NW resistor under STI. DRC can't check the square number.			

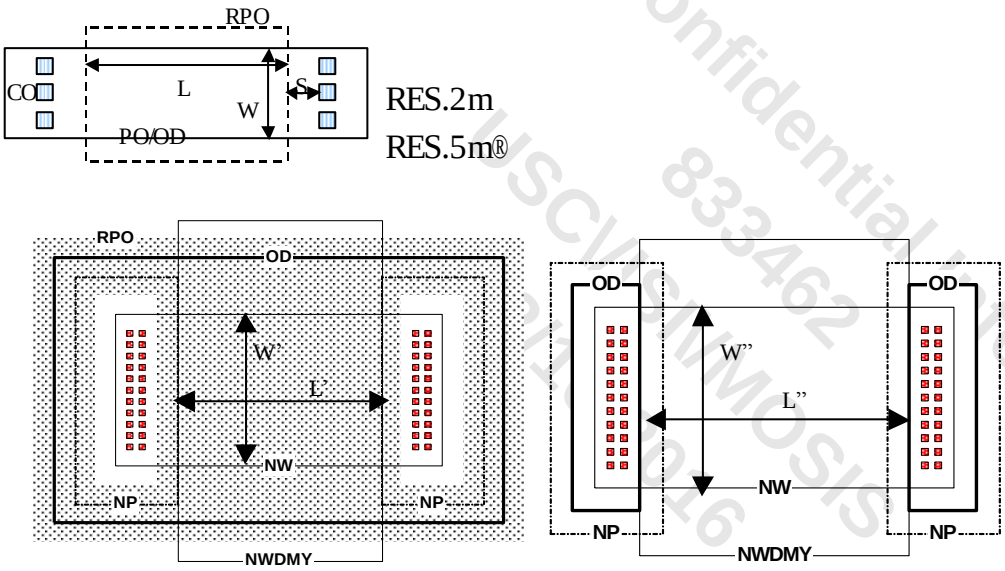

Figure 7.4.4 Resistor layout

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7.4.5 Capacitor Guidelines

Guideline No.	Description
AN.R.37mg^{U}	It is recommended not to use a very long channel device in the design. In order to ensure the channel relaxation time of the MOS capacitor (excluding varactor) is enough to build up charge to the steady state, it is recommended to use proper channel length at the high operation frequency range. The operating frequency shall be below 0.2 * gm / Cgate, where gm is the transconductance of the transistor and Cgate is the gate-oxide capacitance.
AN.R.38mg^{U}	Varactor (NMOS capacitor in NW) is the best choice as MOS capacitor. And the NW should have a P-type guard-ring tied to ground.

7.4.5.1 Design Guidelines for Capacitor Connections – for the Estimation of Minimum Metal Width and Minimum Via Number

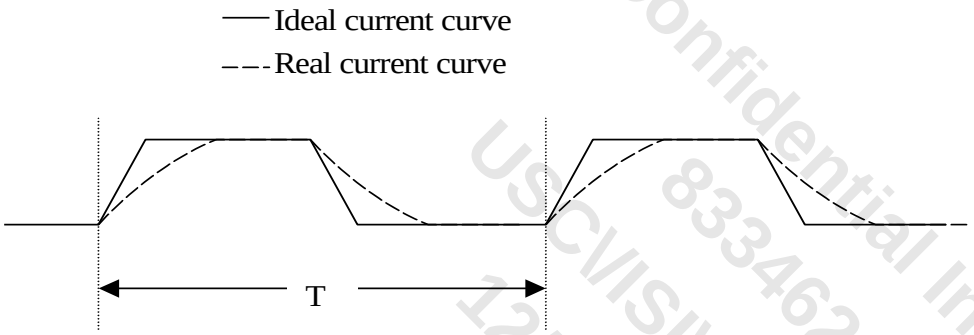

Figure 7.4.5 Transient peak current

For the estimation of minimum metal line width and minimum number of via connecting to capacitor terminals, we assume that the charging up or discharge time is a quarter of clock period T.

In calculation:

△t=T/4 to charge up to VDD or discharge from VDD to ground.

T=1/f, f is the clock frequency.

The current to charge or discharge capacitor is

Imax=Cdv/dt=C* VDD/(1/4f)=4f*VDD*C

C is the capacitance extracted from layout

f (is the clock frequency) and VDD are provided by designer.

The minimum metal line width is

W(metal width in um)= Imax/Jmax, where Jmax= EM current density for metal line per um.

The minimum number of via is

N(Via number)= Imax/Jvia, Jvia= EM current density for each Via.

Both Jmax and Jvia are provided by process specifications to avoid EM (electro migration)

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7.5 Layout Rules and Guidelines for Device Placement

7.5.1 General Rules and Guidelines

Rule No.	Description
AN.R.3m[U]	You need to insert the dummy patterns in the empty area, even if the OD, PO, metal density has already met the density rules. Insert the dummy patterns properly. The recommendation steps for this AN.R.3m: 1st Insert same geometric dummy cells manually to minimize the proximity effec (Figure 7.5.1) 2nd Using TSMC's utility to fill dummy patterns on the rest of the empty space. 3rd In TSMC's utility, Analog (CAD layer: 182;3) layer can't avoid DOD, DPO, or DMx insertion in the region. Please use ODBLK, POBLK, or DMxEXCL layer to cover your analog circuit, which will exclude DOD, DPO or DMx insertion during chip level. 4th Do electrical or silicon characterization
AN.R.4mg[U]	Avoid to have sparse poly gate. Please refer to the item 3 in the section 9.1.2.1.1

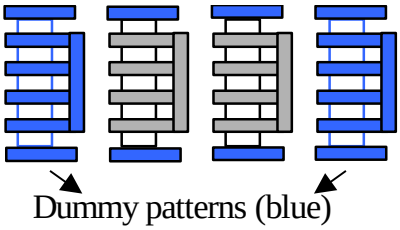

Figure 7.5.1 Example of manual DOD, DPD, or unit cell

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7.5.2 Matching Rules and Guidelines

Rule No.	Description
AN.R.5m^{U}	Make certain that the areas and shapes of matching pairs are identical. Do not use matching pairs with different proximities (iso/dense), nor with different widths, direction and areas, and different shape of equal area.
AN.R.39m^{U}	Make certain that the local pattern density of, and nearby, the matching pair should be identical as much as possible. Use enough dummy cells surrounding the matching pair is highly recommended.
AN.R.6m^{U}	Elements of the matching pair should have the same orientation (Figure 7.5.2).
AN.R.7m^{U}	Avoid routing metal over a matching pair. M1 is the most critical. If it is unavoidable, then use identical routing metal with same potential, over the matching pair. (Figure 7.5.3).
AN.R.8mg^{U}	Place the matching devices close together and, if possible, use “common-centroid” or “inter-digitated” placement for better matching. “Common-centroid” architecture is recommended for those devices that cannot be placed close together (Figure 7.5.4).
AN.R.9mg^{U}	Regardless of any device dimensions of matching pairs with consistent resistance concerns, use the symmetrical number of contacts (please refer to the CO.R.6g) and the same CO to PO gate space. (Figure 7.5.9). The layout of interconnection routing should be symmetrical with respect to each branch.
AN.R.10mg^{U}	Pay attention on the associated routing layout, as well as the associated pattern density, of the matching pair, to minimize the Rs difference. (Figure 7.5.5)
AN.R.11mg^{U}	Pay attention on the matching topology of the resistor layout (Figure 7.5.6)
AN.R.12mg^{U}	PO gate must connect to a protection OD by M1 to reduce the antenna effects in current mirror and matching pairs.
AN.R.40.mg^{U}	In order to avoid the drift of electrical parameter matching, it is important to maintain identical DC bias on the each matching-transistor (NMOS or PMOS) at all operation conditions (eg, standby conditions). If the DC bias is not identical, please evaluate the impact of matching performance.

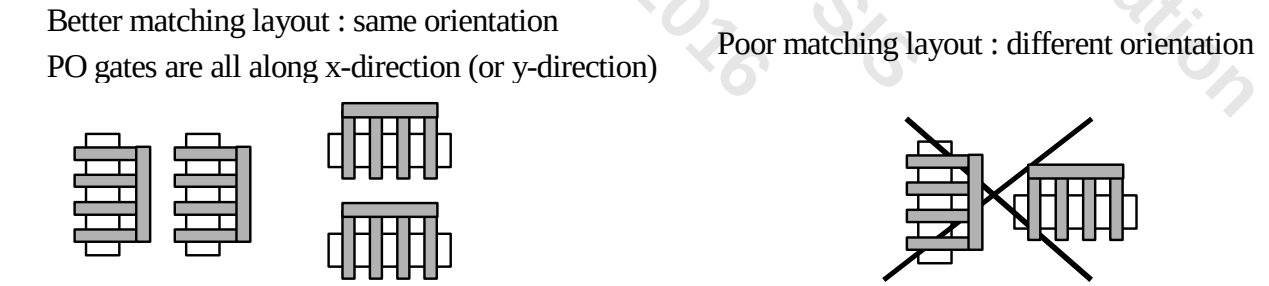

Figure 7.5.2 Example of same or different orientation for matching pairs

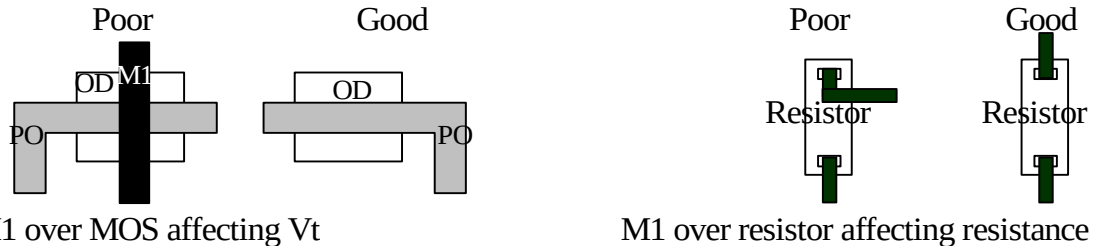

Figure 7.5.3 Example of avoiding routing metal over a matching pair

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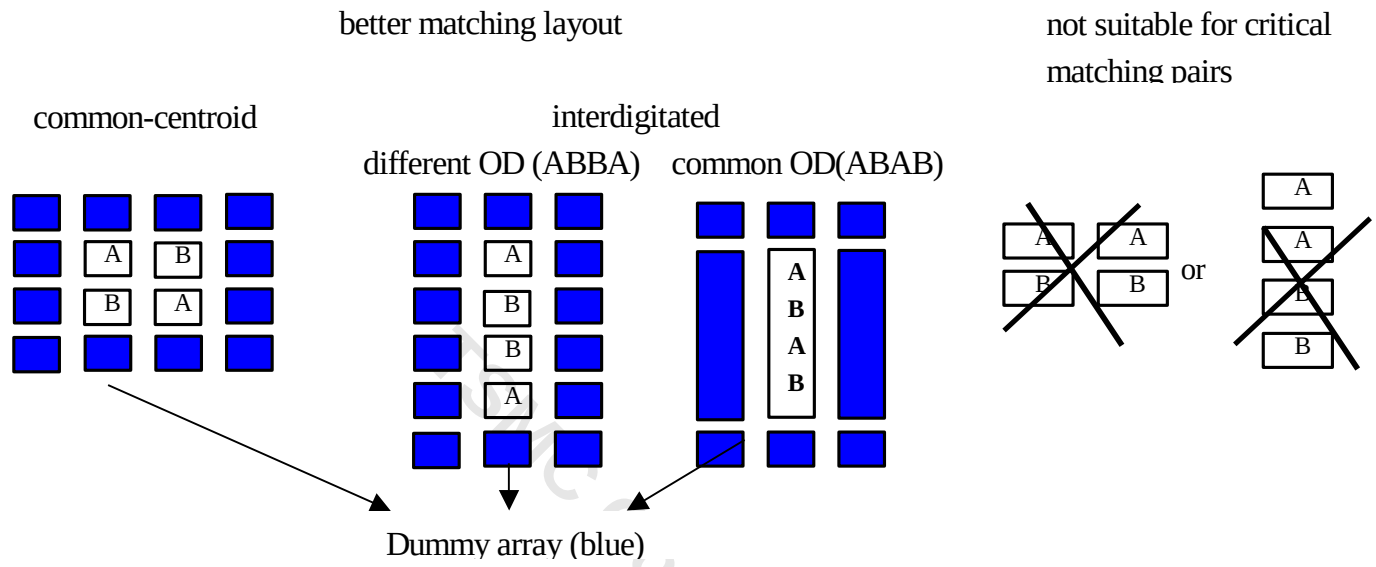

Figure 7.5.4 Example of common-centroid or inter-digitated layout for matching pairs

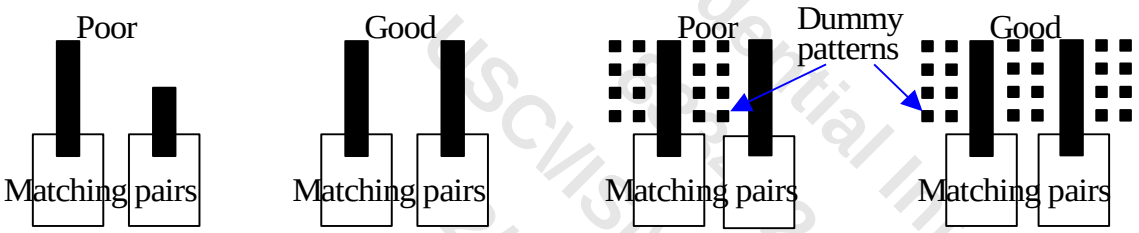

Figure 7.5.5 Example of the associated routing layout of the matching pair

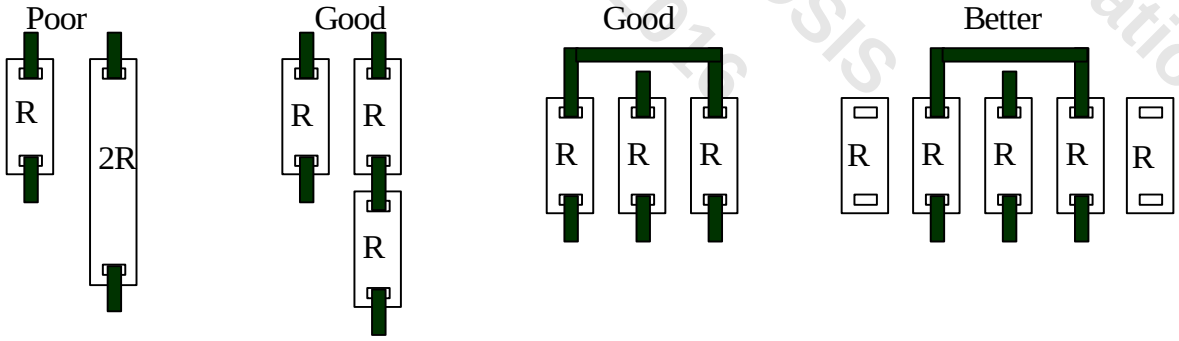

Figure 7.5.6 Example of matching topology of resistor layout for matching pairs

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7.5.3 Electrical Performance Rules and Guidelines

Rule No.	Description
AN.R.13m[U]	Avoid placing the matching pairs or performance-critical devices at the chip corner and chip edge. (Figure 7.5.7)
AN.R.14mg[U]	Avoid using silicided-OD connected between well strap and the MOS source node (butted junction) in analog, matching and performance-critical devices. (Figure 7.5.8)
AN.R.15mg[U]	Optimize the CO number at both source and drain sides of performance-critical devices. (Figure 7.5.9)
AN.R.16mg[U]	Do not use maximum latch-up rule near narrow ravine between wells. (Figure 7.5.10)
AN.R.17mg	Place unsilicided PO resistor on an N-well for better noise immunity. A P+ PO resistor is recommended for overall performance.
AN.R.18mg[U]	Do not use single via for high current or resistance sensitive wire. (Figure 7.5.11)
AN.R.20mg	Use thick oxide (OD2) MOS varactor and capacitor to reduce gate oxide leakage. DRC can not check capacitor.
AN.R.21mg[U]	CB and CBD are not recommended to put on the top of matching pairs or performance-critical devices.
AN.R.41.mg[U]	For the matching sensitive circuits with DC bias at low Vgs regions; the layout style effects (such as LOD, WPE and device orientation) should be carefully reviewed.

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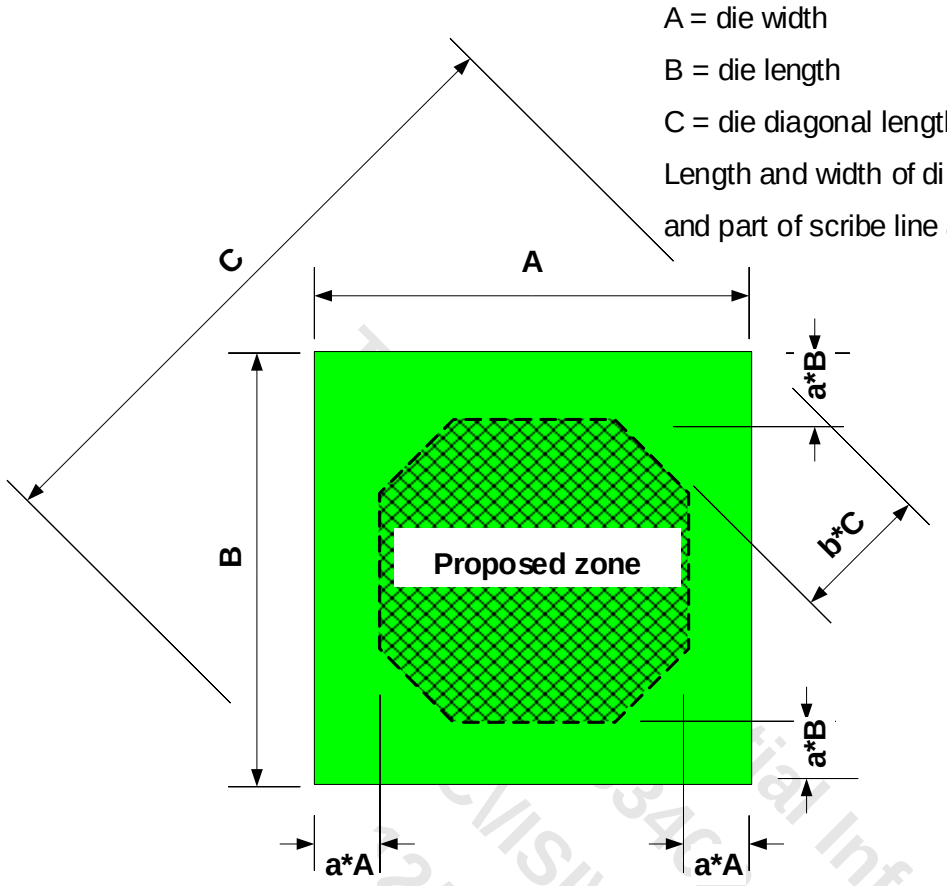

For the bottom/upper die in a stacked-die wirebond PBGA package
1) a: away from die edge ≥ 10% of the chip edge length
2) b: away from die corner ≥ 15% of the chip diagonal dimension

For a single-die wirebond PBGA package
1) a: away from die edge ≥ 3% of the chip edge length
2) b: away from die corner ≥ 5% of the chip diagonal dimension

For a single-die flip chip PBGA package
1) a: away from die edge ≥ 1% of the chip edge length
2) b: away from die corner ≥ 3% of the chip diagonal dimension

The above numbers may be changed by several factors, e.g. die size, die thickness, package type, package material, package size, and circuit design margin, please contact TSMC for more details.

Figure 7.5.7 The proposed zone for matching pairs or performance-critical devices

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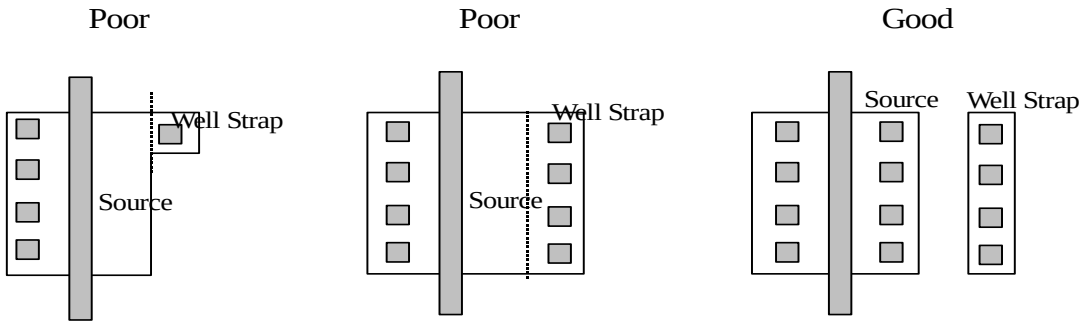

Figure 7.5.8 Example of avoiding using silicided-OD connected between well strap and the MOS source node

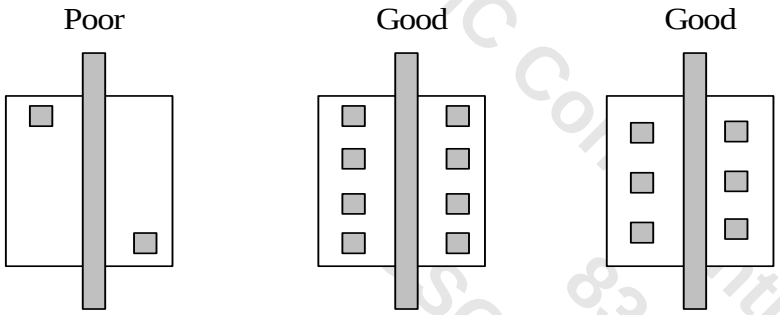

Figure 7.5.9 Optimize theCO number at both source and drain sides

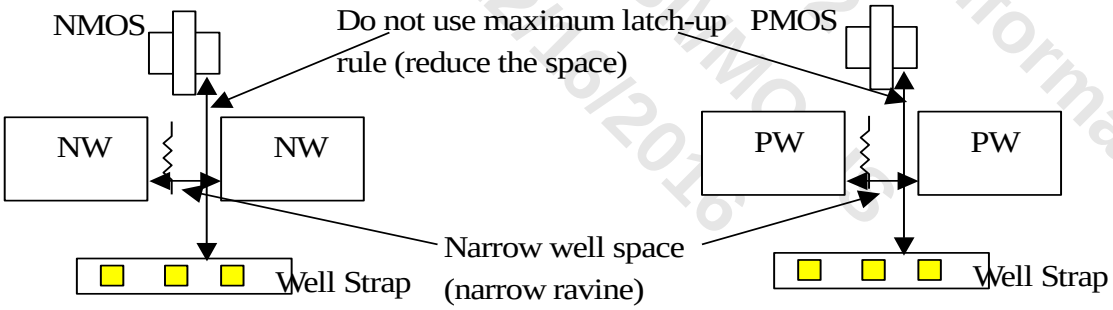

Figure 7.5.10 Example of maximum latch-up rule near narrow ravine between wells

Figure 7.5.11 Example of not using single via for high current or resistance sensitive wire

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7.5.4 Noise

7.5.4.1 Power and Ground

Guideline No.	Description
AN.R.22mg^{U}	For the low noise circuit, a P-Well ring, which is tied to VSS, is recommended to surround all PMOS devices in each analog circuit block.
AN.R.23mg^{U}	For the low noise circuit, a N-Well ring, which is tied to VDD, is recommended to surround all NMOS devices in each analog circuit block.
AN.R.24mg^{U}	Put NMOS in RW (PW in DNW) is a good practice of isolating critical circuit from substrate noise (Figure 7.5.13). Make sure every NW connected to DNW must be same potential (refer to DNW.R.4).
AN.R.25mg^{U}	Use NT_N layer (width >=1um), as a high resistance region, to isolate two high frequency circuit, to reduce the noise or signal coupling from substrate (Figure 7.5.14). ■ minimize the signal lines crossing the high resistance NT_N region. ■ maximize the distance between metal lines from the substrate above the NT_N region (use upper level metal).
AN.R.26mg^{U}	Use separate power supplies and ground buses for the noisy and sensitive circuit and also for the analog and digital circuits. (Figure 7.5.15)
AN.R.27mg^{U}	Keep enough distance between the noisy and sensitive area.
AN.R.28mg^{U}	Use wide guard-ring to stabilize substrate and well potential.
AN.R.29mg^{U}	If transistors within sensitive circuit must be tied together with source and body, do not tie them in the local area by shorter metal line. (Figure 7.5.16)

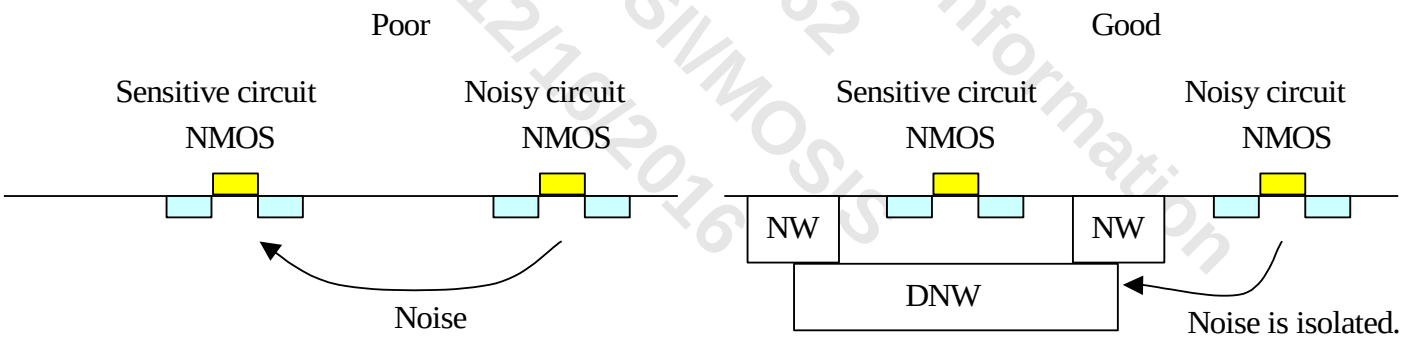

Figure 7.5.13 Example of NMOS is RW.

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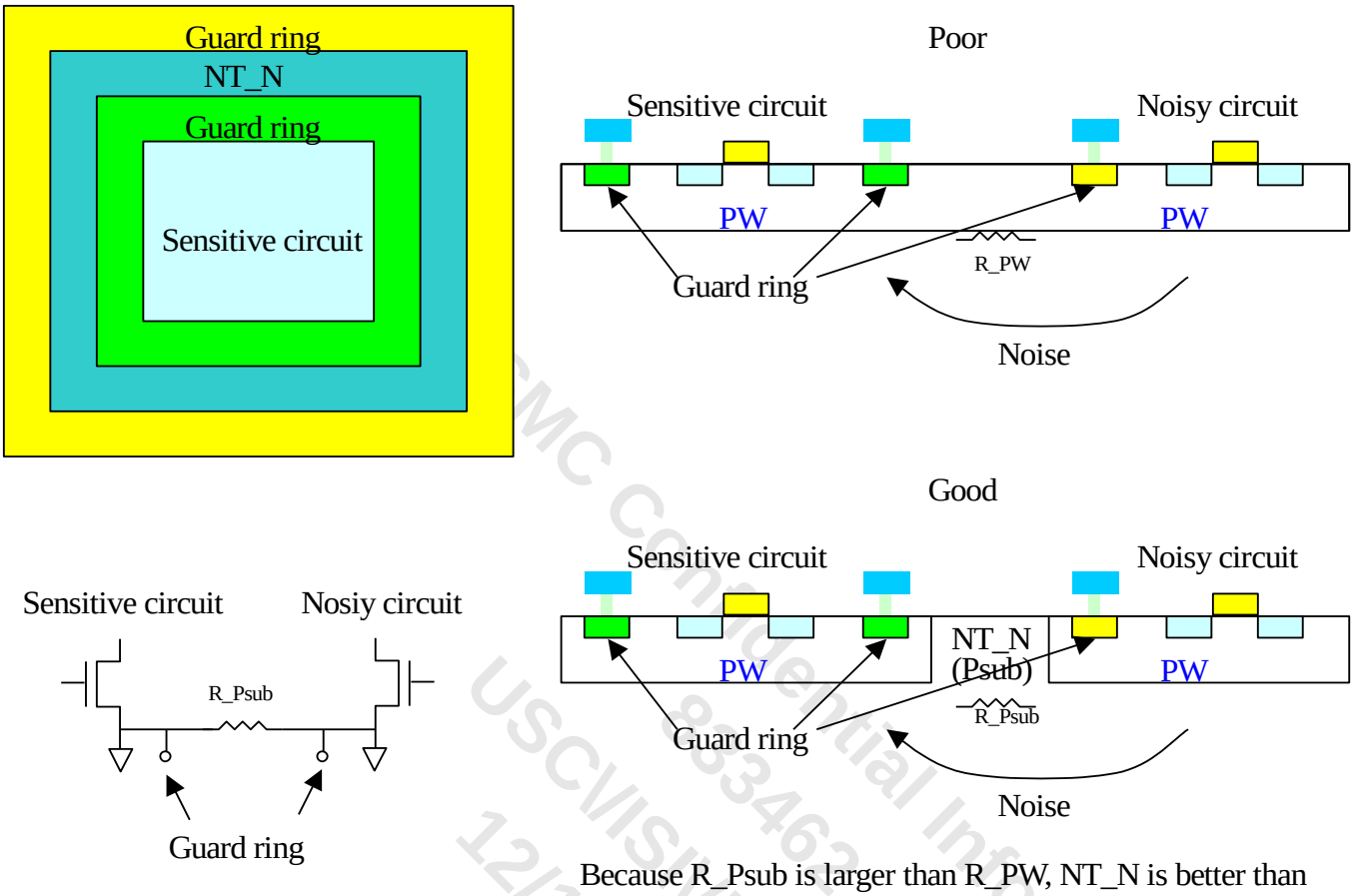

Because R_Psub is larger than R_PW, NT_N is better than PW in the noise isolation.

Figure 7.5.14 Example of NT_N layer as a high resistance region

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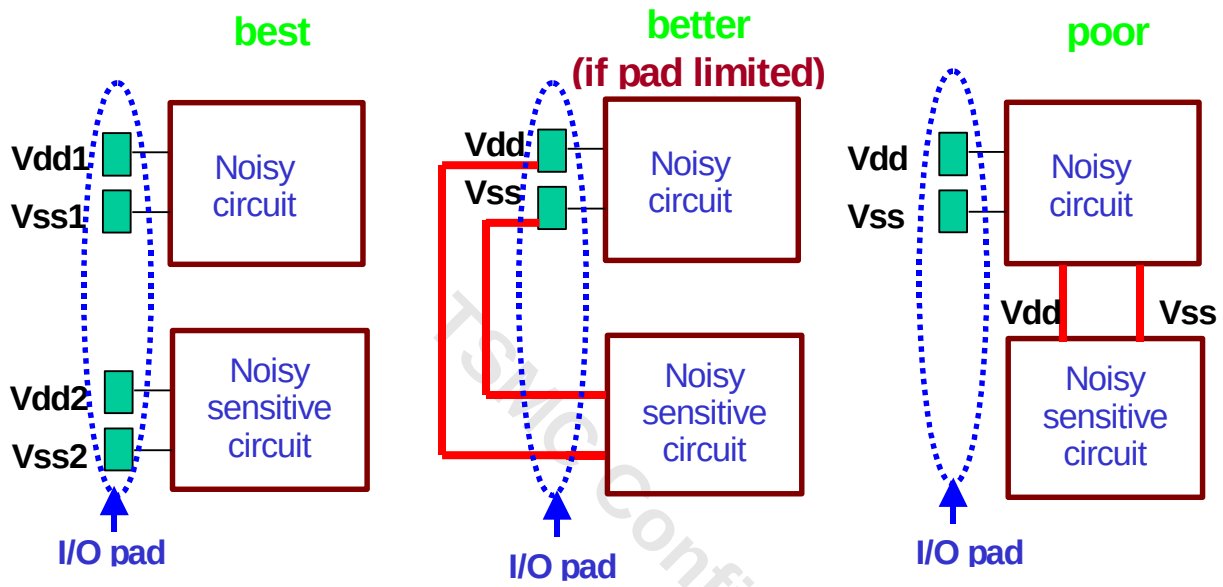

Figure 7.5.15 Example of separated power supplies and ground buses for the noisy and sensitive circuit

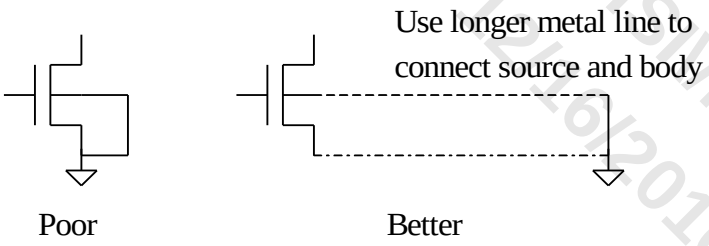

Figure 7.5.16 Example of transistors within sensitive circuit tied together with source and body

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7.5.4.2 Signal

Guideline No.	Description
AN.R.30mg[U]	Keep high frequency signal in high level metal layer.
AN.R.31mg[U]	Use metal shield for victim line that is noise sensitive.
AN.R.32mg[U]	Use metal and poly shield for attacker line that travels through long distance.
AN.R.33mg[U]	Prevent from feedback path through chip seal ring between critical input and output. Use additional guard-ring to isolate the coupling. (Figure 7.5.17)

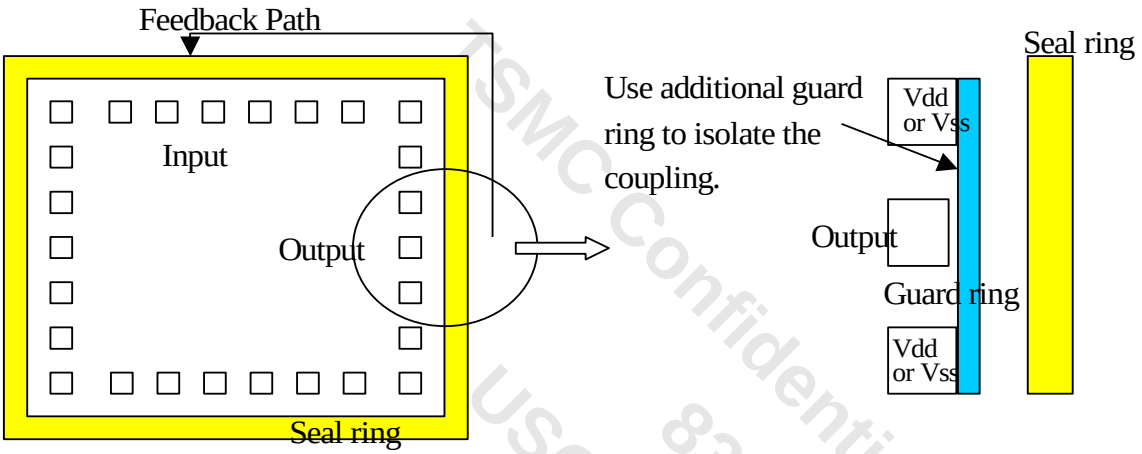

Figure 7.5.17 Example of prevention from feedback path through chip seal ring

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7.6 Burn-in Guidelines for Analog Circuits

Guideline No.	Description
AN.R.42mg^{U}	For the sensitive circuit, e.g. differential input pair, which needs precise device mismatching parameter control such as △Vt and △Isat, it must avoid unbalanced DC bias stress during burn-in period. For example, V_A=Vdd or GND & VB=1/2Vdd, which causes current supplied from current source flowing differently on the differential input pair ($I_A \neq I_B$). This will make differential pair matching become worse after burn-in stress. (Figure 7.6.1)
AN.R.43mg^{U}	Be sure that the analog circuit operates at normal operational condition during burn-in. For example, avoid P1 floating (when R is external) and make it be biased at the normal condition during burn-in. (Figure 7.6.2)
AN.R.44mg^{U}	With the protection OD connection in the sensitive circuit to reduce plasma induced damage during wafer processing.

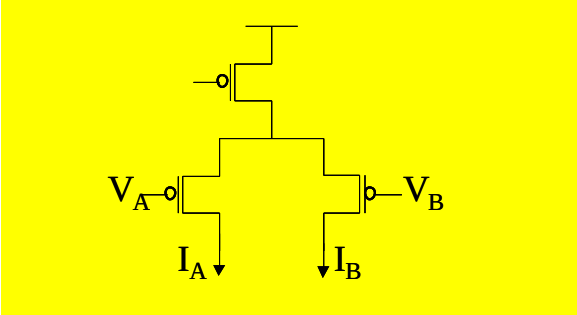

Figure 7.6.1 Example of differential input pair

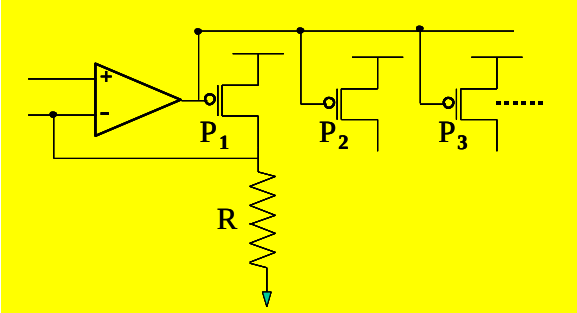

Figure 7.6.2 Example of analog circuit

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8 Dummy Pattern rule and Filling Guideline

This chapter contains the following topics:

8.1 Dummy OD rules
8.2 Dummy poly rules
8.3 Dummy TCD rules and filling guidelines
8.4 Dummy metal rules
8.5 Dummy pattern fill usage summary

8.1 Dummy OD (DOD) Rules

1. **In order to meet the extremely tight requirement in terms of process control for STI etch, polish as well as channel length definition (inter-level dielectric (ILD) planarization), you must fill the DOD globally and uniformly** even if the originally drawn OD already satisfies the required OD density rule (OD.DN.1~OD.DN.3).
2. **It is recommended to use TSMC's auto-fill utilities** (documents: *T-N65-CL-DR-001-C2* and *T-N65-CL-DR-001-H2*).

   It is important to perform the utility on the whole chip GDS. It is dangerous to perform the utility only on the local density violation blocks in terms of the process requirement.
3. **It is recommended to use filler cells with OD/PO to fill a large empty area in the standard-cell-based block during the P&R stage.** Current TSMC DOD/DPO utility is difficult to insert DOD shapes into a standard-cell placed area. For the better PO and OD CD control requirement, it is suggested to layout both OD and PO into filler cell (treat OD/PO as dummy filling, need to follow OD/PO and related rules, and use the GDS layer of OD/PO).
4. **Evaluate the impact on OD masks carefully** when any one of the following layouts is revised:
   - PO/ DPO (poly and dummy poly)
   - NW/ ODBLK/NWDMY/ FW/LMARK/ LOGO/ INDDMY
5. **Use the dummy layer ODBLK properly**. This layer (CAD layer no. 150;20) directs TSMC utility that the area covered should be blocked from DOD fill operations. ODBLK is for excluding DOD, not for excluding dummy Poly (DPO).
6. **It is suggested to make sure that the ODBLK layer covers sensitive circuits**, such as:
   - Pad areas for high frequency signals
   - SRAM sensitive functional blocks and bit cell arrays
   - Analog/RF circuits (DAC/ADC, PLL, Inductor, MiM capacitor) and so on
7. **It is recommended to manually add DOD uniformly inside regions covered by the ODBLK layer,** to gain better process window and electrical performance.
8. **Don't put DOD in areas covered by the following marker layers**:
   - Metal fuse (FW)/L target region (LMARK)
   - Well resistor under STI (NWDMY)
   - Inductor (INDDMY)
   - LOGO
   - Region of chip corner stress relief pattern, seal ring, and CDU pattern

   TSMC's fill generation utility will not add DOD into these regions, as these layers are well defined. The ODBLK covered areas should not cover or overlap the above areas for DRC reasons.
9. **Please refer to the "Dummy Pattern Fill Usage Summary" section in this chapter for additional information.**
10. **Please consult with TSMC first before you use your own DOD rules.**

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Rule No.	Description	Label		Rule
DOD.W.1	Width	A	≥	0.5
DOD.S.1	Space	B	≥	0.4
DOD.S.2	Space to OD (Overlap is not allowed)	C	≥	0.34
DOD.S.3	Space to PO (Overlap is not allowed)	D	≥	0.3
DOD.S.5	Space to NW	F	≥	0.3
DOD.S.6	Space to FW (Overlap is not allowed)	G	≥	1.2
DOD.S.7.0	Space to LMARK or L-slot is defined by either DOD.S.7 or DOD.S.7.1.			
DOD.S.7	Space to LMARK (Overlap is not allowed)	H	≥	1.2
DOD.S.7.1	Space to L-slot (Overlap is not allowed)	H'	≥	5.0
DOD.S.8	Space to NWDMY (Overlap is not allowed)	I	≥	0.6
DOD.S.9	Space to LOGO (Overlap is not allowed)	J	≥	0.0
DOD.S.10	Space to INDDMY (Overlap is not allowed)	K	≥	1.2
DOD.EN.1	Enclosure by NW (fully outside is allowed)	L	≥	0.3
DOD.EN.2	Enclosure by chip edge	M	≥	0.6
OD.DN.1	{OD OR DOD} density across full chip		≥	25%
			≤	75%
OD.DN.2	{OD OR DOD} local density		≥	20%
			≤	80% (outside OD2)
			≤	90%
OD.DN.3	{OD OR DOD} local density inside ODBLK		≥	20%
			≤	80% (outside OD2)
			≤	90%
	1. OD.DN.2 and OD.DN.3 are checked over any 150 µm x 150 µm window (stepping in 75 µm increments). 2. (outside OD2) means the overlapped width between the checking window and OD2 layer is smaller than 37.5 µm. 3. For OD.DN.2/OD.DN.3, the following regions can be excluded: o (CB sizing 2) for high speed/RF products for 20% rule o NWDMY/FW/LMARK/LOGO/INDDMY for 20% rule o Chip corner stress relief and seal ring for 20%/80%/90% rule 4. OD.DN.2 is applied while the width of ((checking window NOT the item 3) ≥ 37.5 µm. 5. OD.DN.3 must be followed for every defined ODBLK region. This rule is only applied while the width of ((checking window AND ODBLK) NOT item 3) ≥ 37.5 µm.			
DOD.R.1	DOD is a must. DOD CAD layer (TSMC default, 6;1) must be different from OD's.			
DOD.R.2	DOD inside chip corner stress relief area is not allowed [except seal ring and stress relief patterns drawn by you].			
DOD.R.3	Only square (or rectangular) and solid shapes are allowed. A 45-degree shape is not allowed.			
DOD.S.2g^{U}	Recommended space to OD (C = 0.6)			
DOD.S.4g^{U}	Recommended space to ODBLK (E ≥ 0.6) (Overlap is not recommended)			

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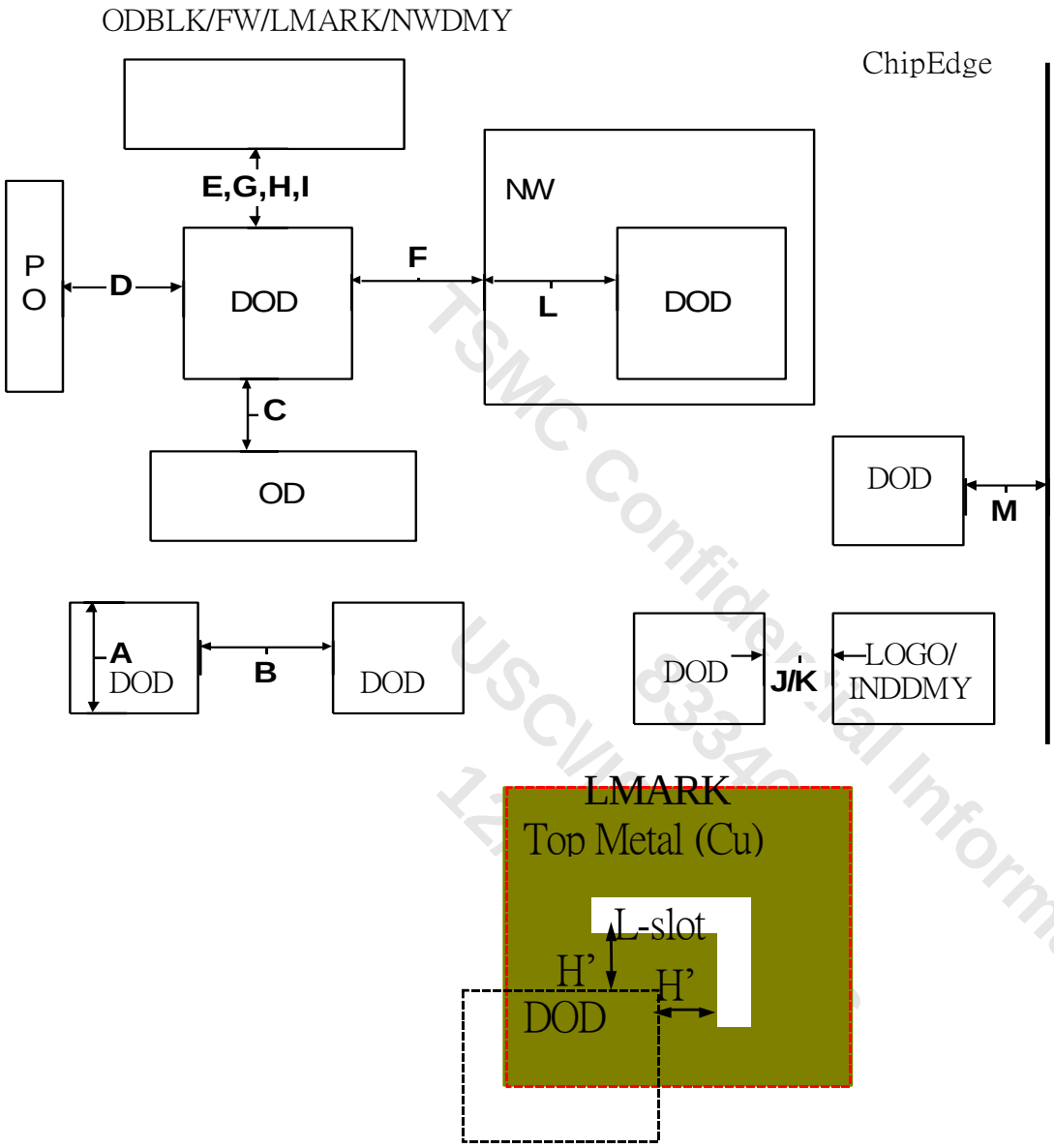
DOD



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8.2 Dummy Poly (DPO) Rules

1. **Good Poly uniformity is the key to meet the PO CD as well as circuit performance requirement. You must fill the DPO globally and uniformly** even if the original drawn poly already satisfies the required poly density rule (PO.DN.1). The designer may wish to add dummy poly to improve the stability of the poly line dimension on silicon.
2. **It is recommended to use TSMC's auto-fill utilities** (documents *T-N65-CL-DR-001-C2* and *T-N65-CL-DR-001-H2*).
3. **It is recommended to use filler cells with OD/PO to fill a large empty area in the standard-cell-based block during the P&R stage.** Current TSMC DOD/DPO utility is difficult to insert DOD shapes into a standard-cell placed area. For the better PO and OD CD control requirement, it is suggested to layout both OD and PO into filler cell (treat OD/PO as dummy filling, need to follow OD/PO and related rules, and use the GDS layer of OD/PO).
4. **Evaluate the impact on the poly mask carefully** when there is DPO in the mask and any one of the following layouts is revised:
   - OD/DOD
   - POBLK/FW/LMARK/LOGO/INDDMY
5. **Use the dummy layer POBLK properly**. This layer (CAD layer no. 150;21) directs the TSMC utility that the area covered should be blocked from DPO fill operations. POBLK is for excluding DPO, not for excluding dummy OD (DOD).
6. **It is suggested to make sure that the POBLK layer covers sensitive circuits**, such as:
   - Pad areas for high frequency signals
   - SRAM sensitive functional blocks and bit cell arrays
   - Analog/RF circuits (DAC/ADC, PLL, Inductor, MiM capacitor) and so on
7. **It is recommended to manually add DPO uniformly inside regions covered by the dummy fill blocking layer POBLK,** to gain better process window and electrical performance.
8. **Don't put DPO in areas covered by the following marker layers** to avoid DRC problems.
   - Metal fuse (FW)/L target region (LMARK)
   - Inductor (INDDMY)
   - LOGO
   - Region of chip corner stress relief pattern, seal ring, and CDU pattern

   TSMC's fill generation utility will not add DPO into these regions because these layers are well defined.

   The POBLK covered areas should not cover or overlap the above areas for DRC reasons.
9. **Please refer to the "Dummy Pattern Fill Usage Summary" section in this chapter for additional information.**
10. **Please consult with TSMC first before you use your own DPO rules.**

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Rule No.	Description	Label		Rule
DPO.W.1	Width	A	≥	0.4
DPO.S.1	Space	B	≥	0.3
DPO.S.2	Space to OD (Overlap is not allowed)	C	≥	0.2
DPO.S.3	Space to PO (Overlap is not allowed)	D	≥	0.5
DPO.S.5	Space to FW (Overlap is not allowed)	F	≥	1.2
DPO.S.6.0	Space to LMARK or L-slot is defined by either DPO.S.6 or DPO.S.6.1.			
DPO.S.6	Space to LMARK (Overlap is not allowed)	G	≥	1.2
DPO.S.6.1	Space to L-slot (Overlap is not allowed)	G'	≥	5.0
DPO.S.8	Space to LOGO (Overlap is not allowed)	I	≥	0.0
DPO.S.9	Space to INDDMY (Overlap is not allowed)	J	≥	1.2
DPO.EN.1	Enclosure by chip edge	K	≥	0.6
PO.DN.1	{PO OR DPO} density across full chip		≥	14%
			≤	40%
PO.DN.2	{OD OR DOD OR PO OR DPO} local density		≥	0.1%
	1. PO.DN.2 rules are checked over any 20 µm x 20 µm area. (stepping in 10 µm increments). 2. For PO.DN.2 rules, the following regions can be excluded: o (CB sizing 2) for high speed/RF products o ODBLK/POBLK/NWDMY/FW/LMARK/LOGO/INDDMY as default o Chip corner stress relief area if seal ring and stress relief pattern added by TSMC. 3. Even in areas covered by {ODBLK OR POBLK}, this pattern density that follows the PO.DN.2 rules is recommended. 4. The rule is applied while width of (checking window NOT item 2) ≥ 5 µm.			
DPO.R.1	DPO is a must. DPO CAD layer (TSMC default, 17;1) must be a different layer from the PO CAD layer.			
DPO.R.2	DPO inside chip corner stress relief area is not allowed [except seal ring and stress relief patterns drawn by you].			
DPO.R.3	Only square (or rectangular) and solid shapes are allowed. A 45-degree shape is not allowed.			
DPO.S.3g^{U}	Recommended space to PO (D = 0.5)			
DPO.S.4g^{U}	Recommended space to POBLK (E ≥ 0.4) (Overlap is not recommended)			
DPO.R.4g^{U}	DPO cut DOD is not recommended			

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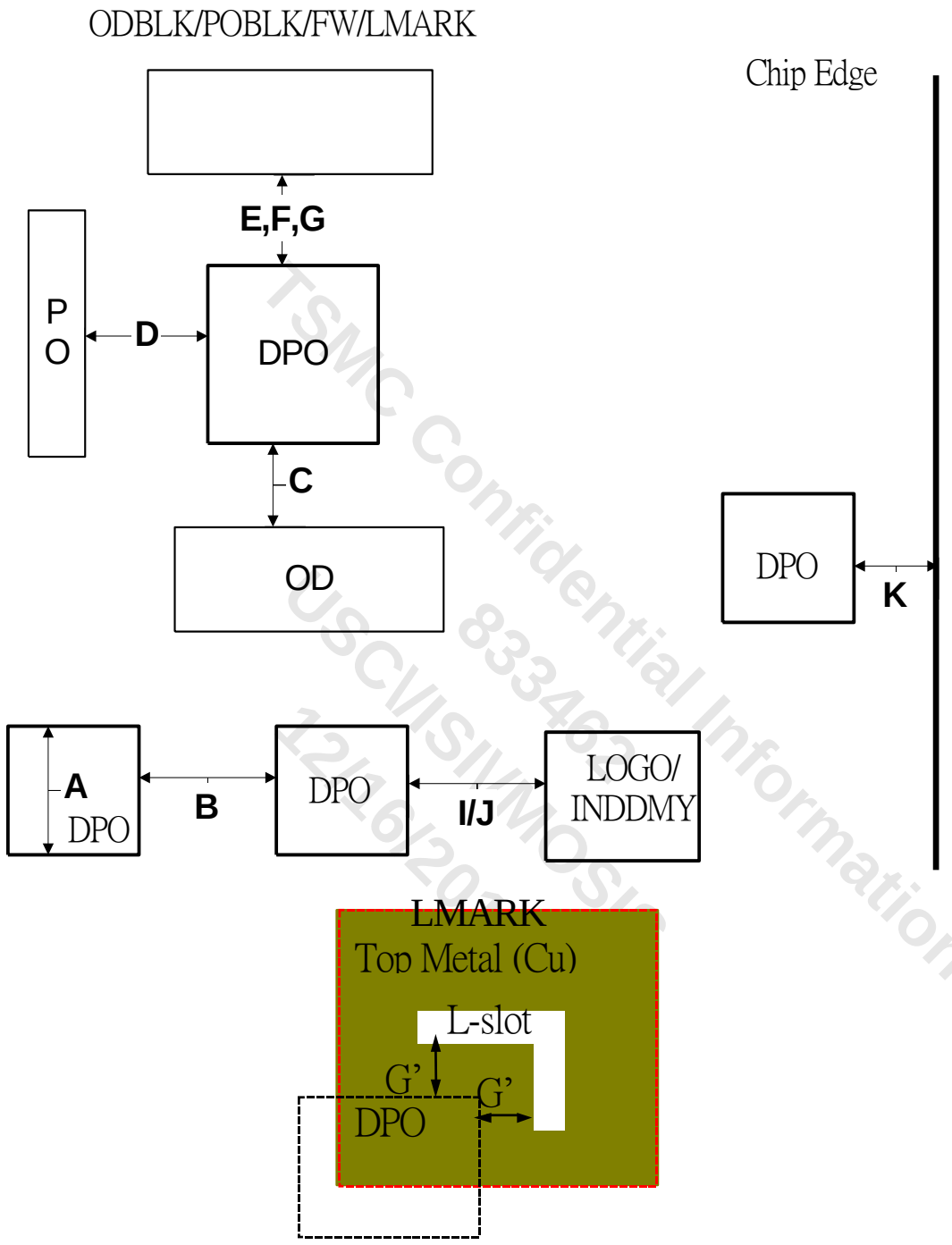
DPO



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8.3 Dummy TCD Rules and Filling Guidelines

8.3.1 Dummy TCD Rules (DTCD)

1. **In order to meet the extremely tight requirement in terms of process control for Poly CD, the Dummy TCD is required within 2mmX2mm area.**
2. **It is recommended to use TSMC's auto-fill utilities** (documents *T-N65-CL-DR-001-C2* and *T-N65-CL-DR-001-H2*). It is important to perform the utility on the whole chip GDS. It is not recommended to perform the utility only on the single IP.
3. **Evaluate the impact on OD/PO/NPO/NPO2/RPO2/P+/N+/NLDD/PLDD masks carefully** when any one of the following layouts is revised:
   - PO/OD/NP/PP
4. **Use the dummy layer POBLK/ODBLK properly**. Theses layers (CAD layer no. 150;20/150;21) directs TSMC utility that the area covered should be blocked from Dummy TCD fill operations.
5. **If you do not use tsmc's dummy utility,** please ask for the dummy TCD layout and insert it in your design flow:
   - It is suggested to make sure that the POBLK/ODBLK layer covers sensitive circuits.
   - TCDDMY overlaps DOD, DPO NW, OD2, DCO, NT_N, POFUSE, RPO, RH, VAR, mVTL, VTH_P, VTH_N, VTL_P, VTL_N, SRM, SRAMDMY, FW, LMARK, INDDMY, LOGO, or MOMDMY which is not allowed.

Rule No.	Description	Label		Rule
DTCD.W.1	Width of TCDDMY		=	12 or 9.245
DTCD.DN.1®	Density of DummyTCD (2mmX2mm is one unit, see next page for more information)	A	≧	80%
DTCD.R.1	TCDDMY must contain OD/PO/PP/NP/POBLK/ODBLK layer			
DTCD.R.2	OD/PO/PP/NP/POBLK/ODBLK layout in the TCDDMY must exactly same as them in tsmc's utility.			
DTCD.R.3	TCDDMY overlap of DOD, DPO, NW, OD2, DCO, NT_N, POFUSE, RPO, RH, VAR, mVTL, VTH_P, VTH_N, VTL_P, VTL_N, SRM, SRAMDMY, FW, LMARK, INDDMY, LOGO, or MOMDMY is not allowed.			

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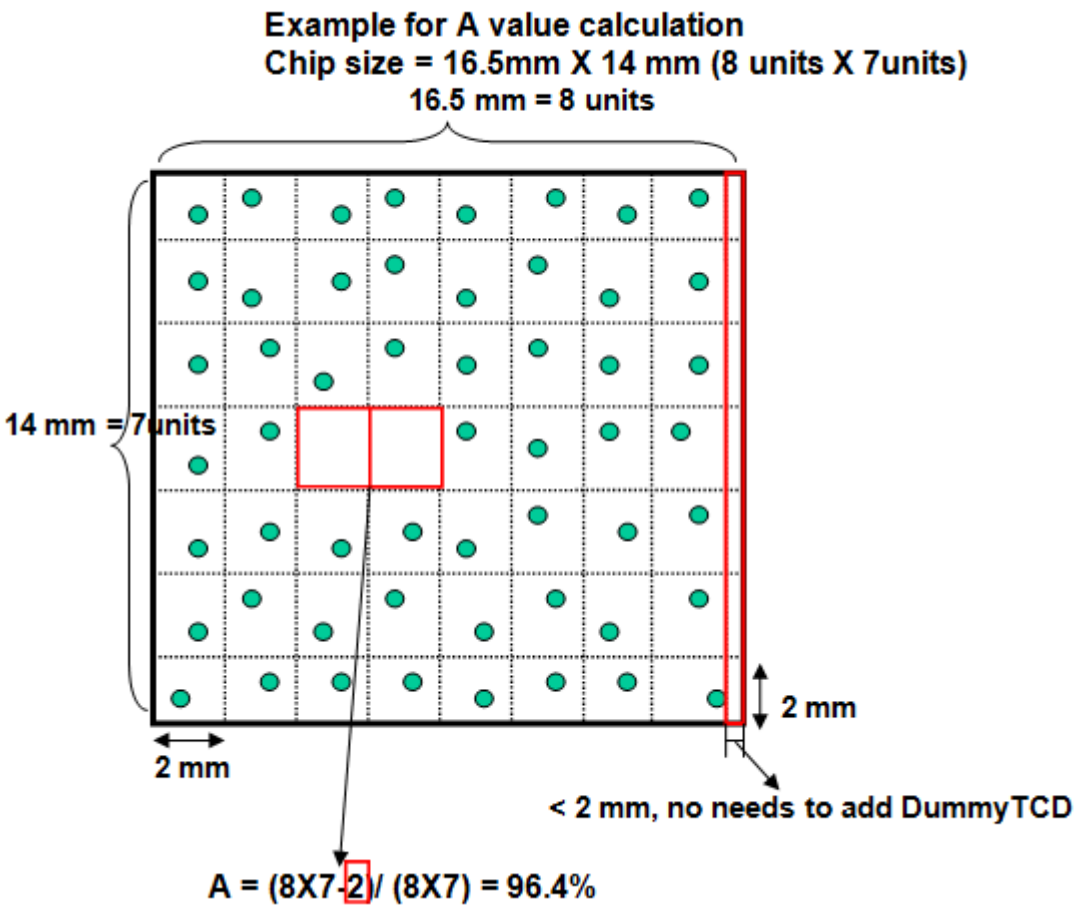
Dummy TCD



8.3.2 Dummy TCD layout Summary

1. The DummyTCD cell should include layers as below.

Layer	CAD
OD	6;0
PO	17;0
PP	25;0
NP	26;0
ODBLK	150;20
POBLK	150;21
* TCDDMY	165;1

2. The Dummy TCD cell is located at P-well area.
3. The Dummy TCD cell can neighbor on the main circuit.
4. PO.DN.3 will exclude TCDDMY area.

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8.4 Dummy Metal (DM) Rules

(DMx, x = 1,2,3,4,5,6,7,8,9)

1. To improve the metal CMP process window, **you must fill the dummy metal globally and uniformly** even if the originally drawn Mx has already met the density rule (Mx.DN.1/ Mx.DN.1.1/Mx.DN.2).
2. **Use either the P&R dummy fill or the utility dummy fill as a method for inserting dummy metal**. Two methods are available for automated dummy metal insertion: commercial P&R tools and a utility from TSMC:
   - The P&R dummy fill is better for dummy metal insertion at the chip level.
   - The utility dummy fill is better for IP blocks, library cells, and full custom cells.
   - Commercial P&R software inserts rectangular DMx geometry. TSMC also provides P&R settings for DMx insertion. Please refer to Reference Flow in *TSMC-Online*.
   - The TSMC utility can insert square DMx uniformly within the original layout.
   - If you use TSMC's auto-fill utility to fill the DMx on the whole chip GDS, TSMC will waive the low local density violation (15% and 20%). If you do not use TSMC's utility to perform the dummy metal generation, you must meet the local density rule (Mx.DN.1).
3. **In the TSMC utility, 2 kinds of dummy metal are generated, DMx and DMx_O.**
   - DMx_O: OPC dummy of inter-metal. DMx_O is the same as real metal, Mx.
   - DMx_O receive OPC. In the MT form, you need to combine DMx_O into the real metal, like (Mx OR DMx_O). My and Mz dummy won't receive OPC.
   - DMx_O needs to meet all Mx rules.
   - The distinction between Mx, DMx, and DMx_O

	Mx	DMx	DMx_O
GDS datatype	0	1	7 for dummy M1 and inter-metals Mx
Do OPC modification on it	Yes	No	Yes
Refer to it during OPC	Yes	Yes	Yes
Follow Mx rule	Yes	No	Yes

4. Use the dummy layer DMxEXCL properly. This layer directs TSMC's utility that the area covered should be blocked from DM fill operations.
5. **It is suggested to make sure that DMxEXCL is drawn over the following:**
   - Sensitive circuits (such as SRAM sensitive function blocks and bit cell array) and analog circuits (such as DAV/ADC, and PLL)
   - RF application circuits
   - Pad areas for high frequency signals
   - MIM capacitors for mixed-signal circuits

     At a minimum, the first metal layer immediately beneath CBM is required. For example, if the capacitor is located between M8 and M7, then M7 under the CBM regions must be blocked.

   For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, careful manual uniform fill addition is still recommended so as to gain a better process window and electrical performance.
6. **For DMxEXCL, use the GDS layer numbers 150;n** (n = 1,2,3,4,5,6,7,8,9).
7. Revision of the following layers may necessitate re-filling of DMx. Because of this, **evaluate the impact on the metal layer mask carefully** when any one of the following layouts is revised:
   - Mx and DMxEXCL layers. This layout revision impacts the Mx mask only.
   - FW/LMARK/LOGO/INDDMY. This revision impacts all the metal layer masks.
   - CBM (between Mx and Mx+1). This revision impacts the Mx mask only if there are no DM problems at the other metal layers. (CBM is a capacitor bottom-plate metal for an MIM capacitor in the MS/RF process.)

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8. In order to have an accurate interconnect RC for timing and power analysis, it is important to extract RC after dummy metal insertion, and extract RC with density based metal thickness variation feature enabled.
9. **Don't put DMx in areas covered by the following marker layers**:
   - Metal fuse (FW)/L target region (LMARK)
   - MIM capacitor region (CBM)
   - Inductor region (INDDMY)
   - LOGO
   - Regions of chip corner stress relief pattern, seal ring, and CDU pattern.

   TSMC's fill generation utility will not add DMx into these regions because these layers are well defined.

   The DMxEXCL covered areas should not cover or overlap the above areas for DRC reasons.
10. **Please refer to the "Dummy Pattern Fill Usage Summary" section in this chapter for additional information**.
11. **Please consult with TSMC first before you use your own DMx rules.**

Rule No.	Description	Label		Rule
DMx.W.1	Width (minimum)	A	≥	
DMx.W.2	Width (maximum) (checked by sizing down 1.5 µm)	B	≤	3.0
DMx.S.1	Space	C	≥	
DMx.S.2	Space to Mx (Overlap is not allowed)	D	≥	
DMx.S.3	Space to Mx (Overlap is not allowed) [Mx width > 4.5 µm and the parallel metal run length > 4.5 µm]	E	≥	1.5
DMx.S.3.1	Space to Mx (Overlap is not allowed) [Mx width > 1.5 µm and the parallel metal run length > 1.5 µm]	E1	≥	0.5
DMx.S.4	Space to FW (Overlap is not allowed)	F	≥	5.0
DMx.S.5.0	Space to LMARK or L-slot is defined by either DMx.S.6 or DMx.S.5.1.			
DMx.S.5	Space to LMARK (Overlap is not allowed)	G	≥	5.0
DMx.S.5.1	Space to L-slot (Overlap is not allowed)	G'	≥	5.0
DMx.S.7	Space to LOGO (Overlap is not allowed)	I	≥	0.0
DMx.S.8	Space to INDDMY (Overlap is not allowed)	J	≥	2.5
DMx.S.9	Space to CBM [CBM between Mx and Mx+1] (Overlap is not allowed)	K	≥	1.5
DMx.S.10	Space to 45-degree bent Mx	O	≥	0.4
DMx.EN.1	Enclosure by chip edge	L	≥	2.5
DMx.A.1	Area (minimum)	M	≥	
DMx.A.2	Area (maximum)	N	≤	

Layer	Dimension				
	A	C	D	M	N
M1and Mx	0.3	0.3	0.3	0.24	80
My	0.4	0.4	0.6	0.565	160
Mz	0.4	0.4	0.6	0.565	160
Mr	0.8	0.8	0.8	1.44	160
Mu (ultra thick metal)	3.0	3.0	3.0	9.00	600

Table Notes:

Mu is the ultra thick metal (34K Å) for the interconnection and inductor in the MS/RF process.

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Mx.DN.1	Minimum metal density in window 75 µm x 75 µm, stepping 37.5 µm	≥	10%
Mx.DN.1.1	Maximum metal density in window 100 µm x 100 µm, stepping 50 µm	≤	80%
	1. Mx.DN.1 ≥10% rule is checked over any 75 µm x 75 µm area (stepping in 37.5 µm increments). 2. Mx.DN.1.1 ≤80% rule is checked over any 100 µm x 100 µm area (stepping in 50 µm increments). 3. Mx.DN.1 and Mx.DN.1.1 would exclude the following regions: o FW /LOGO/INDDMY for 10% rule o LMARK for 10%/80% rule o Chip corner stress relief area and seal ring o CBM of MIM capacitor for 10% rule. For example, if the capacitor is constructed between M8 and M7, then the M7 density check would exclude the CBM region. 4. Mx.DN.1 ≥ 10% rule is applied while the width of (checking window NOT item 3) >= 18.75 µm. 5. Mx.DN.1.1 ≤ 80% rule is applied while the width of (checking window NOT item 3) ≥ 25 µm. 6. Both wire bond pad and flip chip bump pad are excluded from 80% density check.		
Mx.DN.2	Maximum metal density over any 20 µm x 20 µm area (checked by stepping in 10 µm increments). The rule is applied while width of (checking window NOT Bond pad) ≥ 5 µm. Mx.DN.2 would exclude the following regions: 1. Both wire bond pad and flip chip bump pad 2. Mz in {INDDMY SIZING 18 µm} 3. LMARK	≤	90%
Mx.DN.4	The metal density difference between any two 250 µm x 250 µm neighboring checking windows including DMxEXCL (stepping in 250 µm increments) Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient.)	≤	40%
Mx.DN.5	It is not allowed to have local density > 80% of all 3 consecutive metal (Mx, Mx+1 and Mx+2) over any 50um x 50um (stepping 25), i.e. it is allowed for either one of Mx, Mx+1, or Mx+2 to have a local density ≤ 80%. 1. The metal layers include M1/Mx and dummy metals. 2. The check does not include chip corner stress relief pattern,seal ring and top2 metals at CUP area.		
DMx.R.1	DMx is a must. The DMx CAD layer (TSMC default, 32;1 for DM2) must be different from the Mx CAD layer.		
DMx.R.2	DMx inside chip corner stress relief area is not allowed [except seal ring and stress relief patterns drawn by you].		
DMx.R.3	0 or 45-degree solid shapes are allowed		
DMx_O.R.1	DMx_O INTERACT Mx is not allowed.		
DMx.S.6g^{U}	Recommended space to DMxEXCL (H ≥ 0.6) (Overlap is not recommended)		
DMx.W.1g^{U}	Recommended DMx size (width x length)		

	Square (Utility Fill)
	Width x Length
M1 and Mx	0.5x0.5~2x2
My	1x1~2x2
Mz	1x1~2x2
Mr	1.2x1.2~3x3
Mu	3x3

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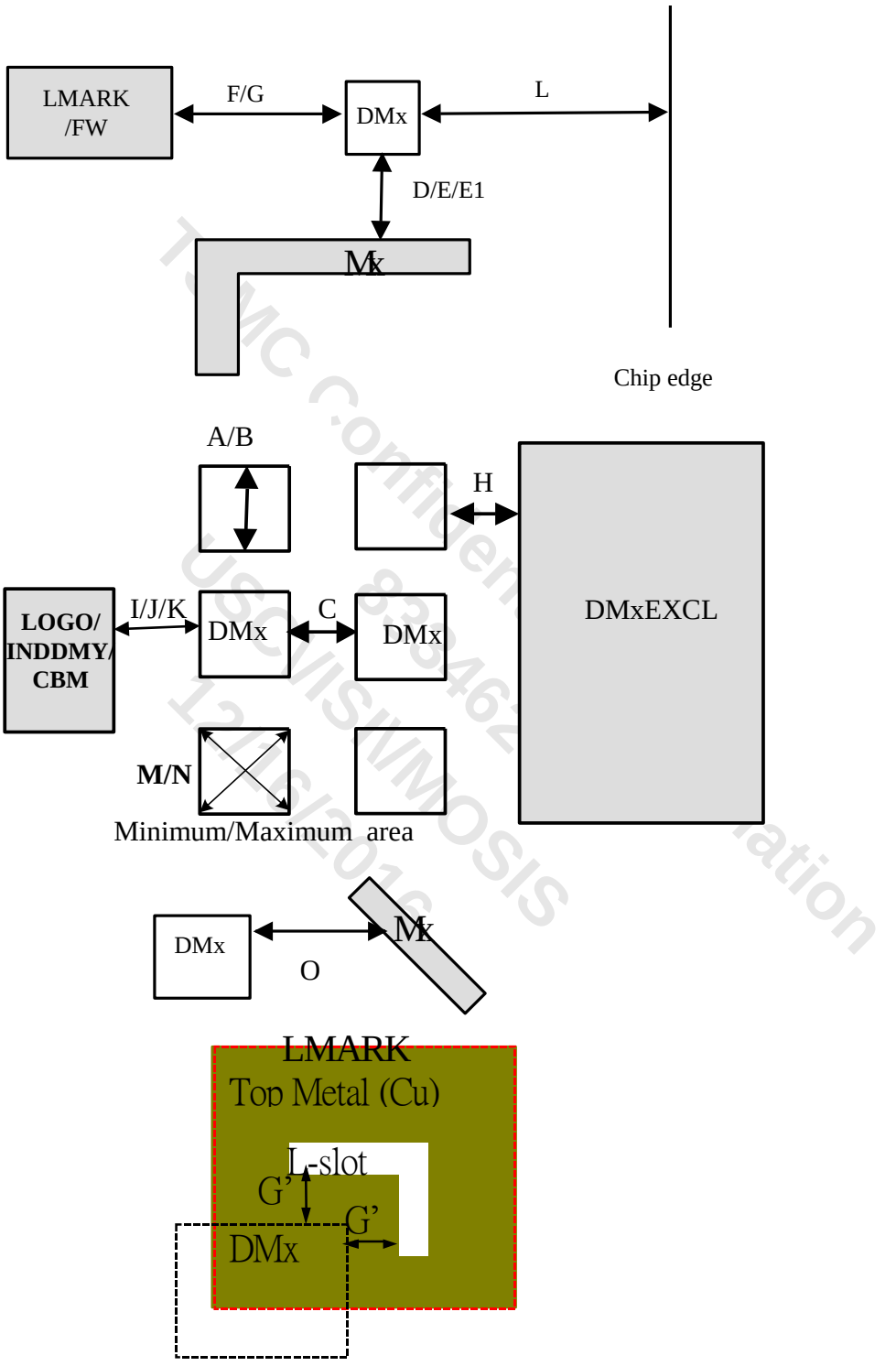
DMx



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8.5 Dummy Pattern Fill Usage Summary

This section is divided into the following sections:

- Dummy pattern filling requirements
- Recommended flow for dummy pattern filling
- Blockage layer (ODBLK/POBLK/DMxEXCL) requirements and recommendations
- Dummy pattern filling guidelines
- Mask revision guidelines
- Dummy pattern re-fill evaluation flow chart

8.5.1 Dummy Pattern Filling Requirements

1. **OD/PO/Metal pattern density requirements**

	Local Density Range	Window check size	Whole Chip Density Range
OD	20%~80% for Core region 20%~90% for I/O region	150 µm * 150 µm	25%~75%
Poly	≥0.1% for OD or PO	20 µm * 20 µm for 0.1%	14%~40%
Metal	≤ 90% for M1/Mx/My/Mz/Mr	20 µm * 20 µm	NA
	10~80% for M1/Mx/My/Mz/Mr/Mu	75 µm * 75 µm for 10% 100 µm * 100 µm for 80%	NA

2. **DOD/DPO/DMx requirement**: The DOD/DPO/DMx must be filled, even if the local or chip density has already met the density rules (OD.DN.1/OD.DN.2/OD.DN.3/PO.DN.1/PO.DN.2/PO.DN.3/ Mx.DN.1 /Mx.DN.1.1/Mx.DN.2/ Mx.DN.4/Mx.DN.5) (x=1~9).
3. **Density requirement**: It is recommended that you use the TSMC auto-fill utility to generate dummy fill patterns.

   If you use TSMC's auto-fill utility to fill DOD and DMx, TSMC will waive the low density rule violations (OD.DN.2, Mx.DN.1, Mx.DN.1.1) (x=1~9). Both the local density rules and chip density rules must be met if TSMC's auto-fill utility is not used to generate the DOD/DPO/DMx fill.
4. **Tool recommendation:** It is recommended to fill dummy patterns using P&R dummy fill (for DMx only) with TSMC provided settings or using the TSMC's auto-fill utility.

   The TSMC auto-fill utility can fill patterns uniformly. It is structurally and hierarchically optimized to provide maximum yield and manufacturability improvement with minimum perturbation to the circuit.

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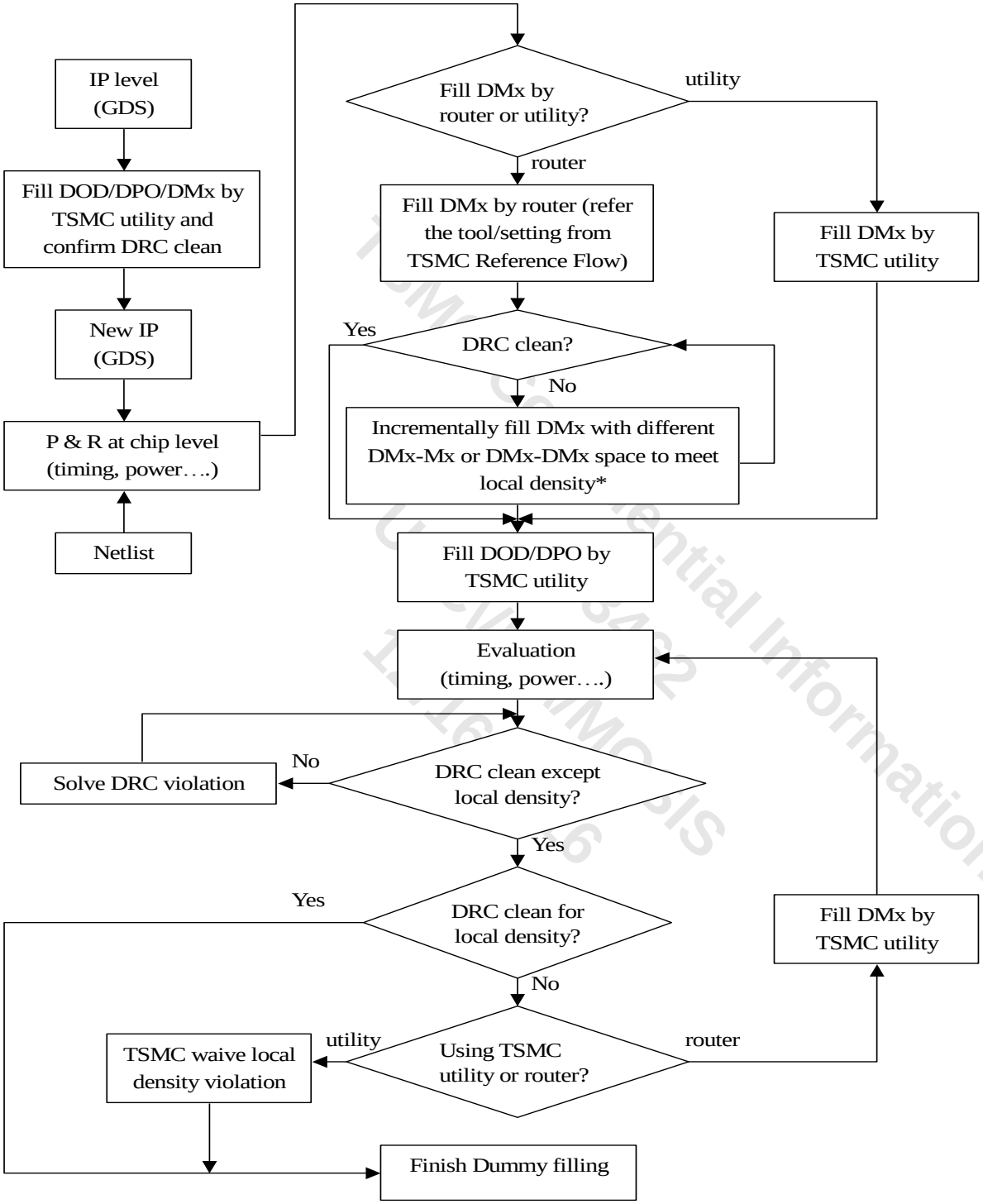
8.5.2 Recommended Flow for Dummy Pattern Filling



* If incrementally fill DMx is done many times, it still can't meet local density, please fill DMx by TSMC utility.

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8.5.3 Blockage Layer (ODBLK/POBLK/DMxEXCL) Requirements and Recommendations

1. **Density requirement**: For any area covered by a blockage layer, it is especially critical to meet the local density rules.

   Blockage layers specify sensitive regions (by recommendation or requirement), and P&R dummy fill(for DMx only) or the TSMC auto-fill utility does not fill dummy patterns for these regions. For details, please refer to the following sections in this chapter: "Dummy OD Rules," Dummy Poly Rules," and "Dummy Metal Rules."

Circuit	Blockage Layer		
	ODBLK	POBLK	DMxEXCL
RF application circuit	Must	Must	Must
Pad metal area for high frequency signals	Must	Must	Must
SRAM block and bit cell area	Recommended	Recommended	Must (M1 at least)
Analog block (ADC/DAC/PLL, and so on)	Must	Must	Recommended

   - **RF circuits**: Draw a blockage layer that covers the entire RF circuit. Designers should consider the signal coupling impact and keep a suitable distance between the RF circuits and the blockage layer edge.
   - **High frequency signal pads**: Draw blockage **layers** that are coincident with the outer edge of the metal pads.
   - **Other sensitive regions**: Draw a blockage layer that covers the other sensitive regions, including the SRAM function block and bit cell array, analog circuits (DAC/ADC/PLL), and so on.

2. **Areas excluded from certain dummy fill**: Don't put any dummy patterns into the following regions:
   - Metal fuse (FW)/L target region (LMARK): DOD/DPO/DMx
   - Well resistor under STI region (NWDMY): DOD
   - CBM region: DMx (if CBM between Mx+1 and Mx)
   - INDDMY region: DOD/DPO/DMx
   - LOGO region: DOD/DPO/DMx
   - Seal ring /CDU /chip corner stress relief pattern region: DOD/DPO/DMx

The TSMC utility will not add dummy patterns into these regions unless the correct dummy layer is specified, or the correct option is turned on (for CBM and chip corner).

The ODBLK/POBLK/DMxEXCL covered areas should not cover or overlap the above areas for DRC reasons.

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8.5.4 Dummy Pattern Filling Guidelines

1. **Dummy pattern filled by P&R dummy fill (for DMx only) or TSMC's dummy fill utility**.

   Put all relevant layers (MUST and OPTION listed in the following table) into one GDS file. If the OPTION layers are not ready to tape out, draw the blockage layer to avoid dummy pattern fill. (For example, if FW is not ready to tape out when making an OD mask, draw FW into ODBLK to exclude DOD filling.)

Layer ID	Description	Dummy Pattern		
		DOD	DPO	DMx (x=1,2,3,4,5,6,7,8,9)
OD	Diffusion	MUST	MUST	
PO	Poly	MUST	MUST	
NW	N-well	MUST		
Mx	x=1,2,3,4,5,6,7,8,9			MUST
FW	Fuse window	OPTION	OPTION	OPTION
LMARK	L-mark	OPTION	OPTION	OPTION
CBM	Capacitor bottom metal			OPTION
NWDMY	N-Well resistor	OPTION		
INDDMY	Inductor dummy layer	OPTION	OPTION	OPTION
ODBLK	DOD blockage layer	OPTION		
POBLK	DPO blockage layer		OPTION	
DMxEXCL	DMx blockage layer			OPTION
LOGO	Product labels	OPTION	OPTION	OPTION

2. **Dummy pattern geometry (DOD/DPO/DMx) generated by P&R tool or TSMC utility**: You must place this fill geometry in a reserved layer (data type 1 as default).
3. **Dummy pattern generated by a non-TSMC utility**: If the auto-fill utility is not provided by TSMC, it must meet the DOD/DPO/DMx rule. Also, keep this fill geometry in a reserved layer (data type 1 as default).
4. **CAD layer usage**: If dummy patterns and active patterns have different GDS layers and data types (such as data type 0 and 1), the dummy patterns should follow the DOD/DPO/DMx rules.

   If dummy geometry and active circuit geometry are placed on the same GDS layers and data types (such as data type 0), the dummy patterns should follow the appropriate OD/PO/Mx rules. Please note that placement of dummy geometry on the same CAD layer as circuit geometry will result in longer mask making cycle times.

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8.5.5 Mask Revision Guidelines

When masks or layouts are revised, re-evaluate to modify the filled dummy patterns.

Layer ID		Dummy Pattern		
		DOD	DPO	DMx (x=1,2,3,4,5,6,7,8,9)
1	OD	○	✓	×
2	PO	✓	○	×
3	NW	✓	×	×
4	Mx (x=1,2,3,4,5,6,7,8,9)	×	×	○
5	FW	✓	✓	✓
6	LMARK	✓	✓	✓
7	CBM	×	×	✓
8	NWDMY	✓	×	×
9	INDDMY	✓	✓	✓
10	ODBLK	✓	×	×
11	POBLK	×	✓	×
12	DMxEXCL (x=1,2,3,4,5,6,7,8,9)	×	×	✓
13	LOGO	✓	✓	✓
14	DOD	○	✓	×
15	DPO	✓	○	×

○ : Needs mask revision

✓ : Evaluate mask revision

× : Doesn't need mask revision

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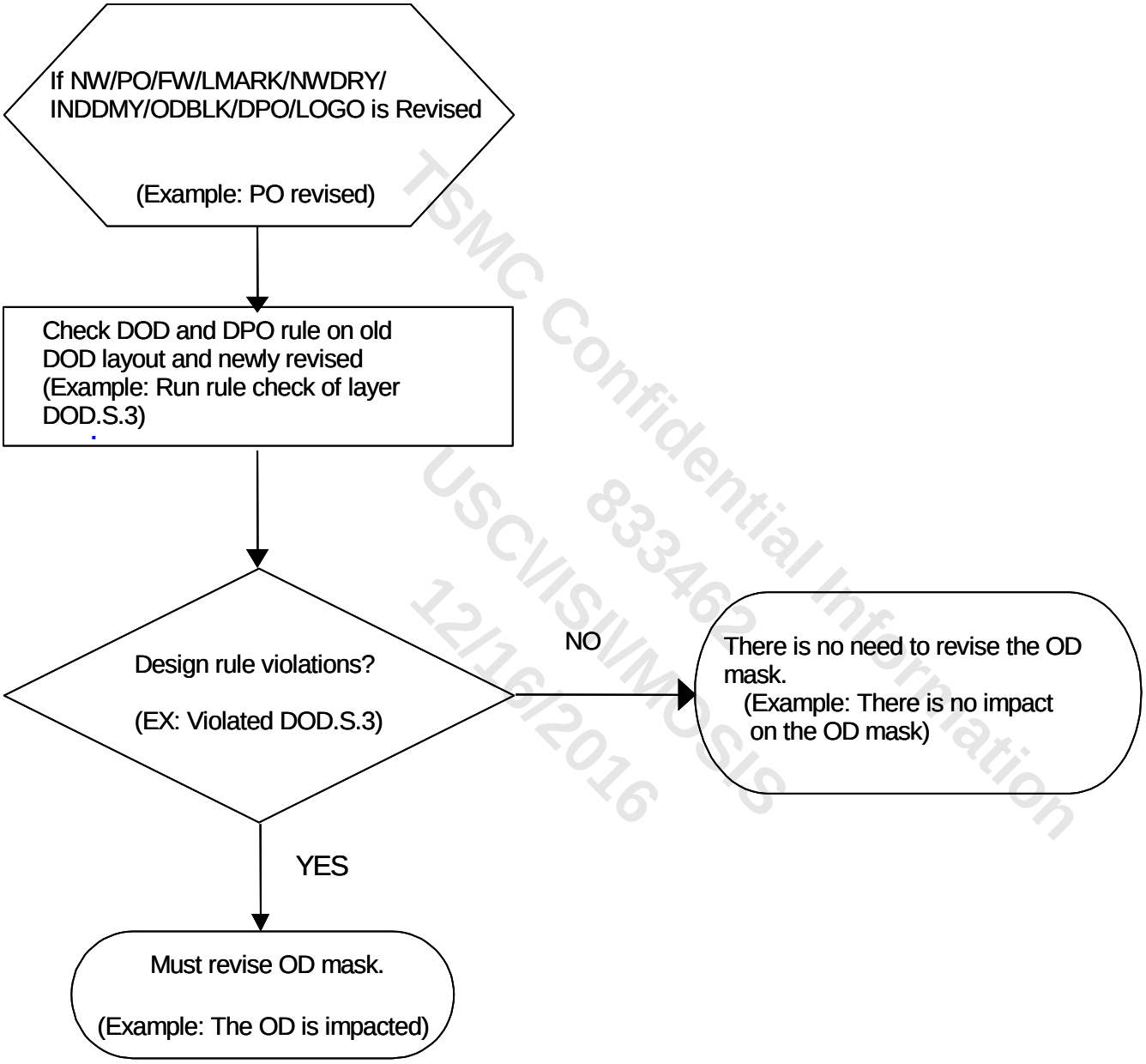
8.5.6 Dummy Pattern Re-fill Evaluation Flow Chart

OD Mask Revision Decision Flow



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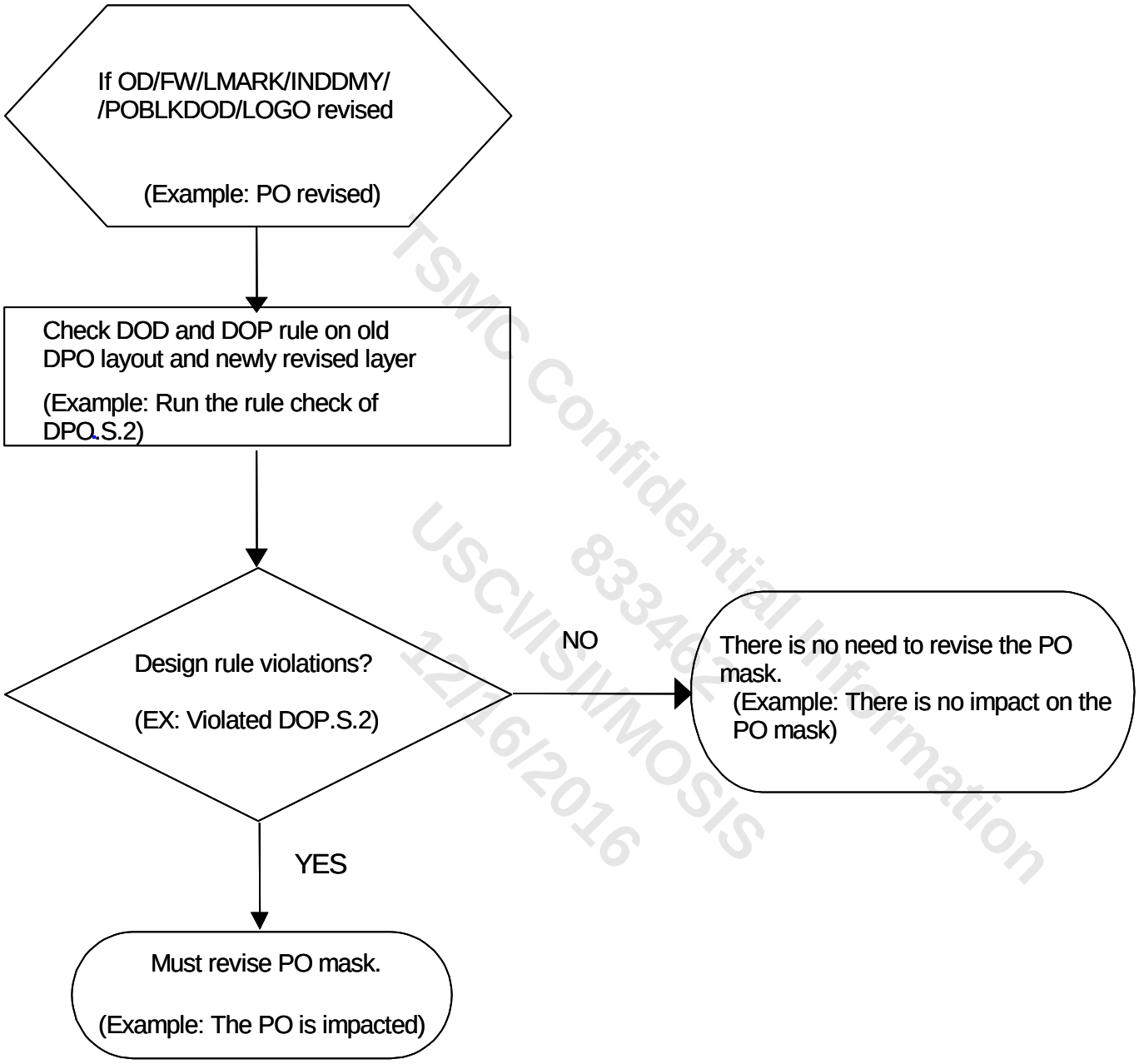
PO Mask Revision Decision Flow



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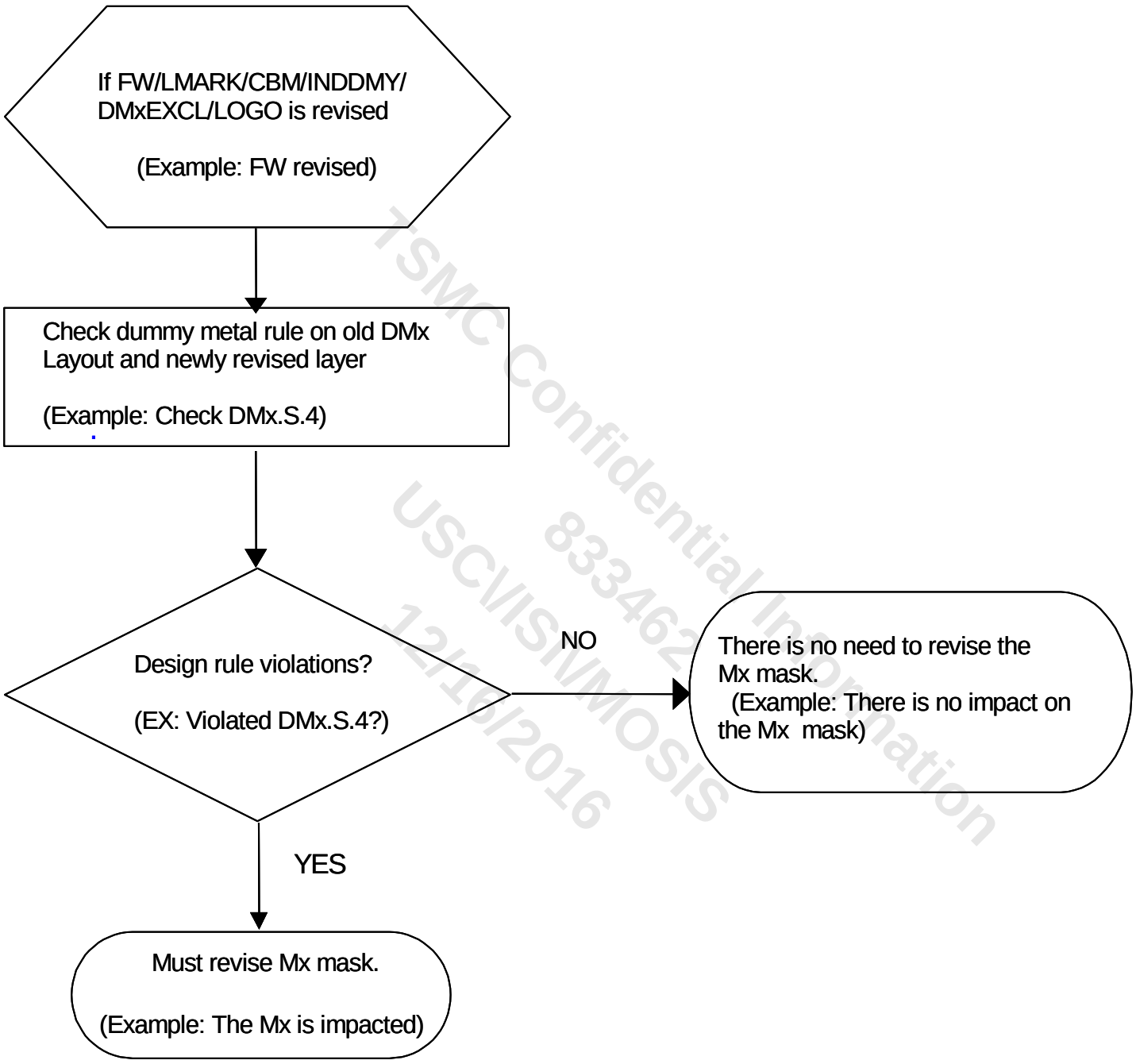
Mx Mask Revision Flow



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9 Design For Manufacturing (DFM)

This chapter provides information about the following topics:

9.1 Layout guidelines for yield enhancement

9.2 DFM recommendations and guidelines summary

9.3 MFU optimization kit

9.1 Layout Guidelines for Yield Enhancement

This section provides guidelines for layout optimization to minimize certain potential and unnecessary yield or timing loss under the condition that they introduce no area penalty.

For a given chip design, first and foremost, efforts should be made to achieve as small a die size as possible. The guidelines should not be used indiscriminately, which could result in unnecessarily large chip sizes.

This section is divided into the following topics:

- Layout tips for minimizing critical areas
- Guidelines for optimal electrical model and silicon correlation
- Guidelines for mask making efficiency

9.1.1 Layout Tips for Minimizing Critical Areas

Defects are variable in size and therefore follow a size distribution. A *critical area* of a given layout is an accumulative area that is susceptible to certain failures (shorts or opens) caused by defects of a certain size. For example, although the total occupied areas are the same in panels A and B of Figure 9.1.1, the wires in layout A are more vulnerable to defect-induced shorts because they have a larger critical area.

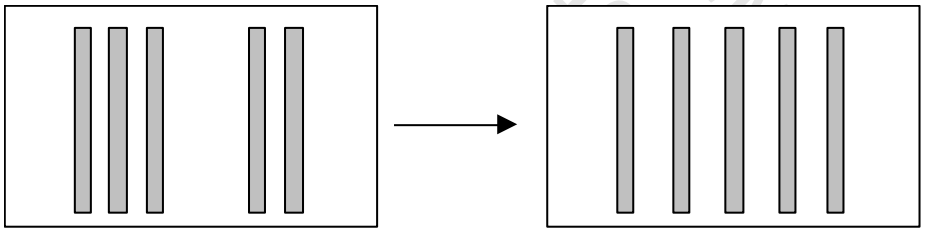

Figure 9.1.1 Layout Examples of Critical Areas

1. **Space out the wiring**.

   Spacing out the wiring, either using Wire Spreading at P&R stage or manually layout modification at cell level, to take advantage of an empty space can reduce the critical area. This practice has additional benefits:

   - It can reduce wire cross coupling.
   - It can reduce the possibility of pattern short.
   - It can evenly distribute the local pattern density, thereby creating less variation in wire Rs.

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2. **Reduce the probability of wiring shorts**.

   The critical area plays a role in the yield of a given design, but so does the rate of failure that corresponds to the critical area. Manufacturing experience indicates that a wiring short circuit is a more frequent problem than an open circuit.

   - Give priority to increasing wiring space for conductors of non-minimum wiring pitch, second only to wire resistance or EM considerations. Refer to Figure 9.1.2.

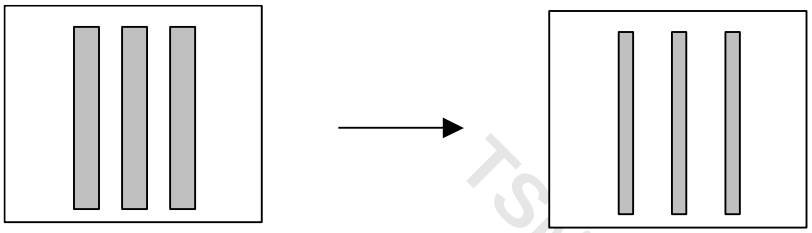

Figure 9.1.2 Reduced Probability of Wiring Shorts

   - For long and parallel metal or poly lines use a larger space.
   - Avoid the use of redundant wiring, except for reliability or performance considerations.
   - Draw wires in an orthogonal fashion.
   - Avoid leaving small jogs, especially in the corner areas where metal spacing is at a minimum.
   - Avoid using 45-degree turns, except for very wide metal buses, where the length of the 45-degree portion should be sufficiently large. X-metal uses more advanced E-beam writer to generate mask and no need to consider this recommendation.

3. **Reduce the risk of open silicided wire or high resistance silicided wire**.

   To avoid a potential silicide break related to an open circuit or high resistance in narrow lines of poly or OD:

   - Do not use a long narrow width poly conductor, if possible, as a means of local interconnection. The length of un-contacted narrow width poly should be kept to a minimum.
   - If possible, do not use a narrow width OD conductor as a means of interconnection.
   - Avoid a butted N+OD/P+OD interface in a narrow OD.
   - Use a sufficient number of contacts when a narrow OD strip is used for substrate tapping.

4. **Reduce the probability of a contact or via open circuit.**

   Open and soft open (excessively high Rc) of a single contact or via are usually a yield bottleneck, given their sheer number in a chip. While the manufacturer strives to bring down the failure rate as low as possible, a designer can contribute to further reduction of the probability.

   Whenever possible, include redundant vias and contacts for the following benefits:

   - Reduces the probability of an open circuit
   - Reduces via and contacts resistance and potential variation.
   - Potentially increases via stress migration immunity

5. **Reduce the probability of open vias in a single-via stack**.

   Whenever possible, use a larger than minimum sized island metal for stacking a single via. This reduces the risk of via resistance variation or open vias.

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9.1.2 Guidelines for Optimal Electrical Model and Silicon Correlation

The following sections offer recommended practices to minimize the deviation of processed hardware from electrical models.

9.1.2.1 Transistors

1. **Avoid layout styles that may contribute to silicon-to-model deviation**.
   - Avoid using narrow-width devices and short channel device if they require high precision, such as current source device
     - Due to critical dimension variations in channel length and channel width, the electrical properties of narrow-width devices and short channel devices vary more than those of larger devices.
     - Poly or OD corner rounding may impact the device length or width critical dimension, primarily in narrow width devices (W < 0.15 µm). These DFM Action Required Rules, PO.S.5®, should be followed to eliminate this effect while W ≥ 0.15 µm.
   - Source or drain contacts should be placed symmetrically wherever possible. Avoid using single source or drain contacts on large width devices. Please refer to CO.R.6g.
   - Use the recommendation from DFM recommendation CO.EN.1® regarding sufficient OD-to-contact overlap.

     The benefits of sufficient OD-to-contact overlap are less variation of contact resistance and the avoidance of potentially excessive drain or source leakage.
   - Use uniform poly and OD densities across a design.

     The poly and OD densities in the neighboring area could affect the gate critical dimension. Although the post-layout insertion of dummy OD, or dummy poly, or both, may patch some empty spaces, it is best to avoid the problem with careful planning and space filling at the macro levels of layout design initially. Please refer to these rules in Chapter 5: "DOD Rule," "DPO Rule," "Dummy Pattern Fill Usage Summary" and also 9.1.2.1.1: "Improvement of poly CD uniformity."
2. **Be aware that thin oxide gate leakage of the 65nm process is higher than that of previous generations.** Its impact on the functionality of a circuit, which uses thin oxide transistors and/or capacitors and/or MOS varactors, must be taken into account by using a proper SPICE model that contains the leakage components.
3. **Pay attention to the leakage current for narrow-width devices with a low-V_t option.**

   Please consult the SPICE model for detailed information.
4. **Device behavior is influenced by layout style possibly due to stress distribution induced by STI/OD edge.** Designer should take this length of OD (LOD) effect into consideration during device or cell level design. Please refer to section 5.3.
5. **Avoid using asymmetrical or single source/drain CO placement on large device (CO.R.5g)..**
6. **For PMOS device, if the NWELL is tied to the source used as an internal AC node, the NWELL total area junction capacitance should be included in the circuit simulation by adding the Well capacitance at the source node.**
7. **Take NWELL sheet resistance into consideration during simulation, to reflect the transient bias variation by adding the Well resistance between source node and substrate node.**

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9.1.2.1.1 Improvement of poly CD uniformity

Further recommendation for improvement of poly CD uniformity (3-sigma) at small channel length:

- **Uni-directional poly lines are suggested**. The overall CD uniformity improvement is 0.3nm. The vertical and horizontal poly CD may have 1.5nm difference in worse case as the poly orientation is different.
- **For sensitive circuit with minimum poly width = 0.06 µm, it is recommended using the following space ranges of gate poly to neighboring poly, 0.19 µm ~ 0.27 µm, 0.295 µm ~ 0.39 µm, and 0.455 µm ~ 0.94 µm.** 0.3nm CD improvement can be achieved. Please refer to DFM recommendation PO.S.13®. Fixed PO space equal to 0.2um or 0.49um is highly recommended.
- **Reduce sparse poly gate count. Avoid to draw a core device PO gate > 1.0 µm away from nearby PO or dummy PO** (S2, S3 in figure 9.1.3). Please refer to DFM recommendation PO.S.11®.
- **Insert dummy PO surrounding existing PO gate if this PO gate is the nearest one to cell edge and is > 0.5 µm away from cell edge.** (S1, S3 in figure 9.1.3)
- **Recommend to insert dummy PO (or PO) with same parallel run length as of the surrounded PO gate.**
  - Hard macro cells are sometimes with placement blockages. However, this blockage would degrade DOD/DPO insertion performance and cause a wide open area.
  - IP designers have to own the responsibility of reducing isolated PO/OD by inserting dummy PO/OD inside the hard macro layout.
  - Either extend hard macro boundary to align with blockage area, or minimize the distance (recommended < 3 µm) from the blockage edge to the macro cell boundary. Also embed this blockage area in macro cell.
  - Have dummy patterns in the blockage area as default and being verified with library characterization process.
  - Avoid any open area ≥ 10 µm x 10 µm without any OD/PO patterns inside in the macro cell area.

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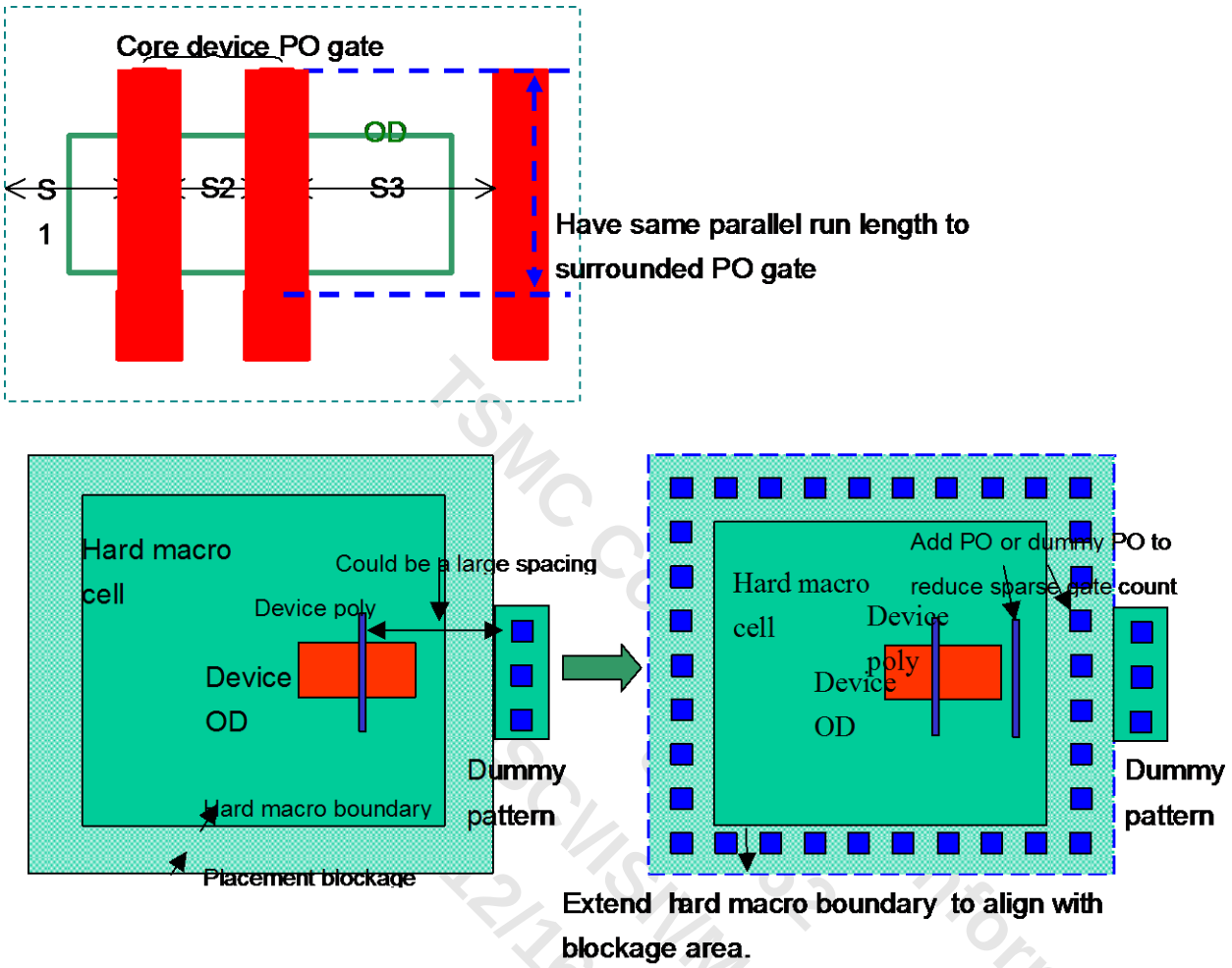

Figure 9.1.3 Reduce sparse poly count

- **Empty area in the standard cell array is not allowed. You needs to use patterned filler cell to insert the empty area of the standard cell array by P&R.**
  - It is requested to have OD and PO patterns in the filler cell, which provides better gate CD uniformity.
  - Need to put dummy PO firstly on sides of both cell edges with < 0.5 μm space to nearby cell edge. A space (≥ 0.1 μm) to nearby cell edge is recommended.
  - Need to follow the layout rules in DRM
  - Use larger PO width in the filler cell. Width ≥ 0.09 μm is recommended.
  - Put OD and PO uniformly across the whole filler cell. Maximized the length of the OD and PO as much as you can (to match the cell height). If the space was not enough, put PO first.
  - Rectangular PO pattern is recommended in the filler cell.
  - Dummy fillers of floating and fixed voltage are both acceptable from process point of view. However, the associated implant layers are must if the filler cell is connected to a fixed voltage.
  - It is also recommended to put filler cell at the edges of standard cell arrays during P&R.

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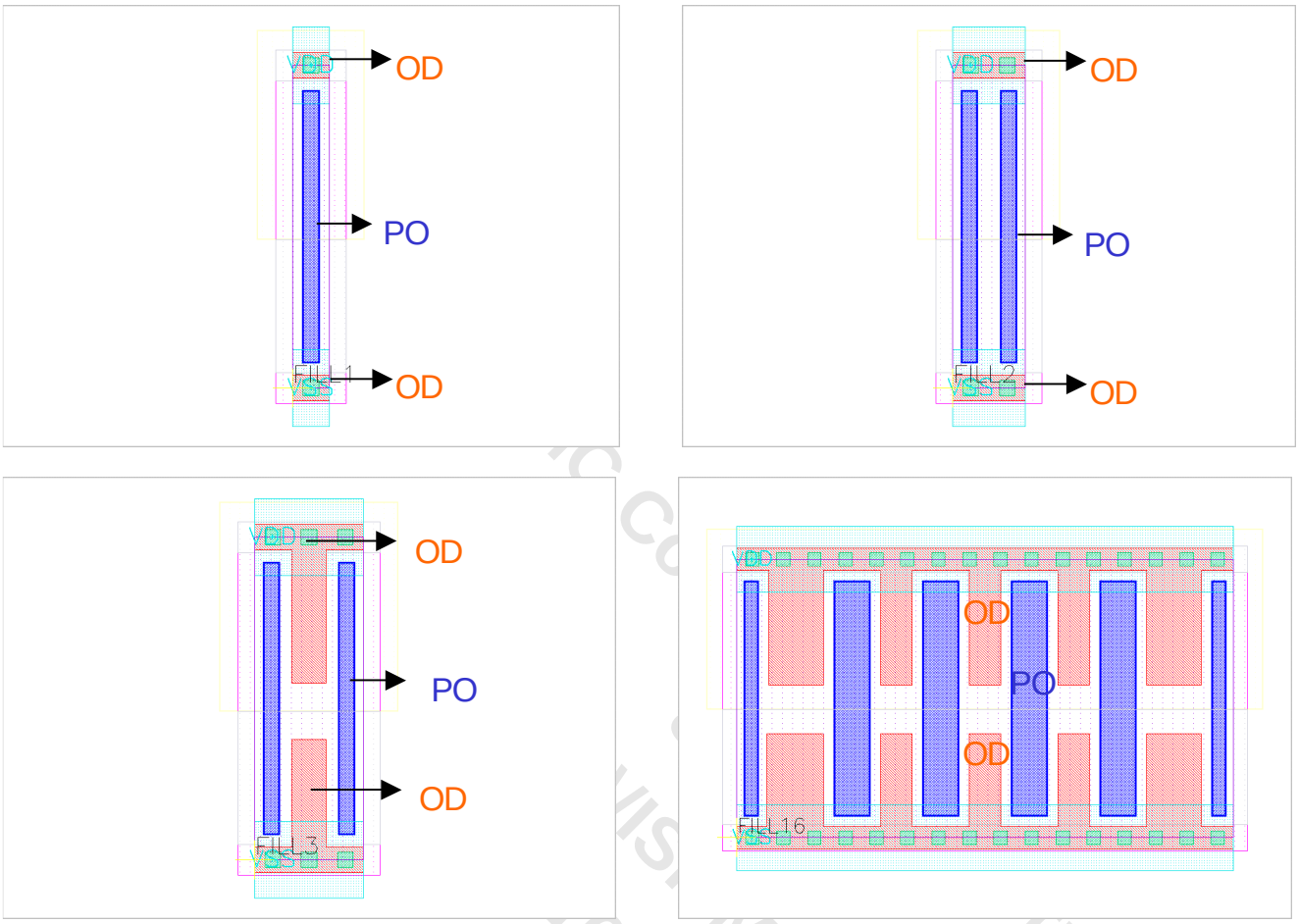
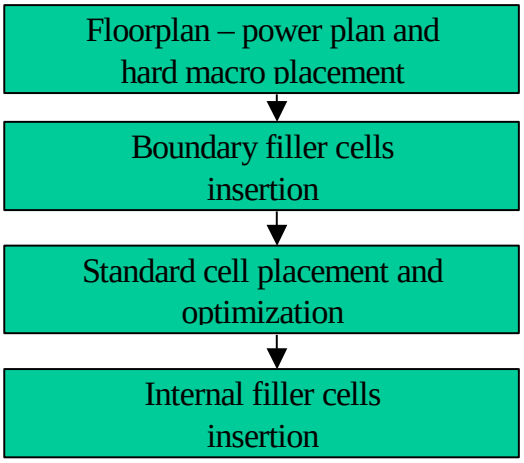


Figure 9.1.4 Example of filler cell

- Guidelines for P&R during filler cell insertion at P&R:
  - Flow:



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- Layout with filler cells
  - Boundary filler cells
    - Before standard cell placement, inserting fillers on block boundary and macro boundary for occupying the placement locations.
  - Internal filler cells
    - After standard cell placement, using original filler insertion command.

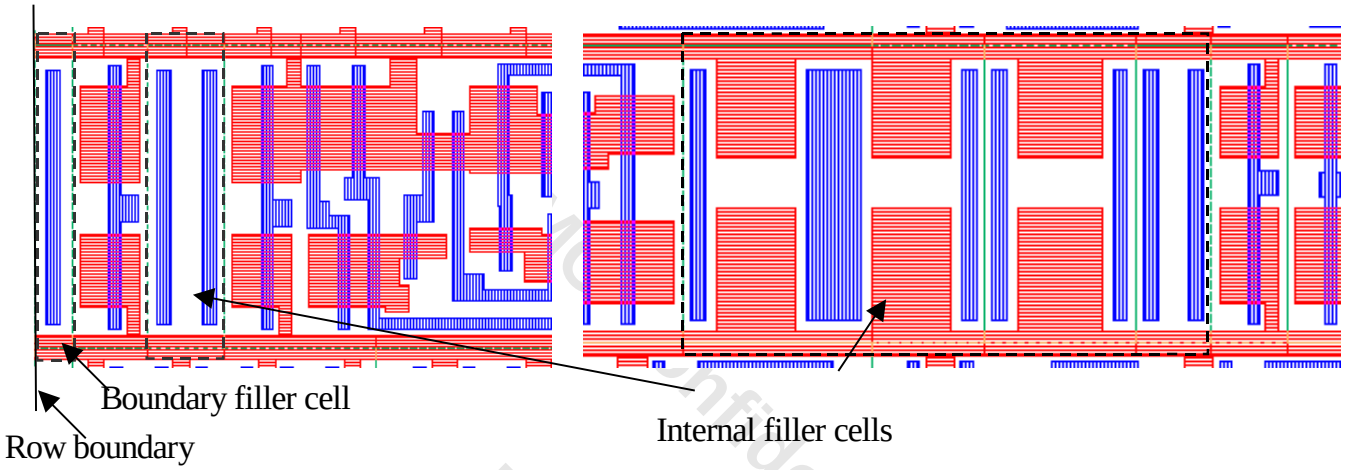

Figure 9.1.5 Layout with filler cells

9.1.2.2 Resistors

1. **For SPICE simulation accuracy it is strongly recommended to put each OD/poly resistor in a dense area.**
2. **Avoid using small width/length of the poly and OD resistor that is critical in performance.**
3. **In order to have accurate interconnect RC for timing and power analysis,** it is important to extract RC after dummy metal insertion and extract RC with density based metal thickness variation feature enabled.

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9.1.3 Electrical Wiring

1. **Avoid using minimum-width poly or OD where resistance is critical to the circuit performance**.
2. During IP/macro design, it is important to put certain density margin to avoid the possibility of high density violations (Mx.DN.1/ Mx.DN.1.1, Mx.DN.2, Mx.DN.4, and Mx.DN.5) during placement. It may have unexpected violation during the IP/macro placement due to the environment, even if the IP/macro already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.
3. **Wherever possible, use two or more narrower metal buses to replace a single bus that uses the maximum width**.
4. **Maintain uniform metal density to minimize wire sheet resistance variation and maximize the associated photo process window. Target the local density to the middle range of the specification, avoiding the two extreme ends**.
5. **Need dummy insertion in the library/IP/Macro blockage area:**
   - Either extend hard macro boundary to align with blockage area or minimize the distance (recommended ≤ 3 μm) from the blockage edge to the macro cell boundary. Also embed this blockage region in macro cell.
   - Have dummy patterns in the blockage area as default and being verified with library characterization process.
   - Need to re-define I/O pin for P&R at new macro cell boundary if you push out hard macro boundary to align with blockage area.

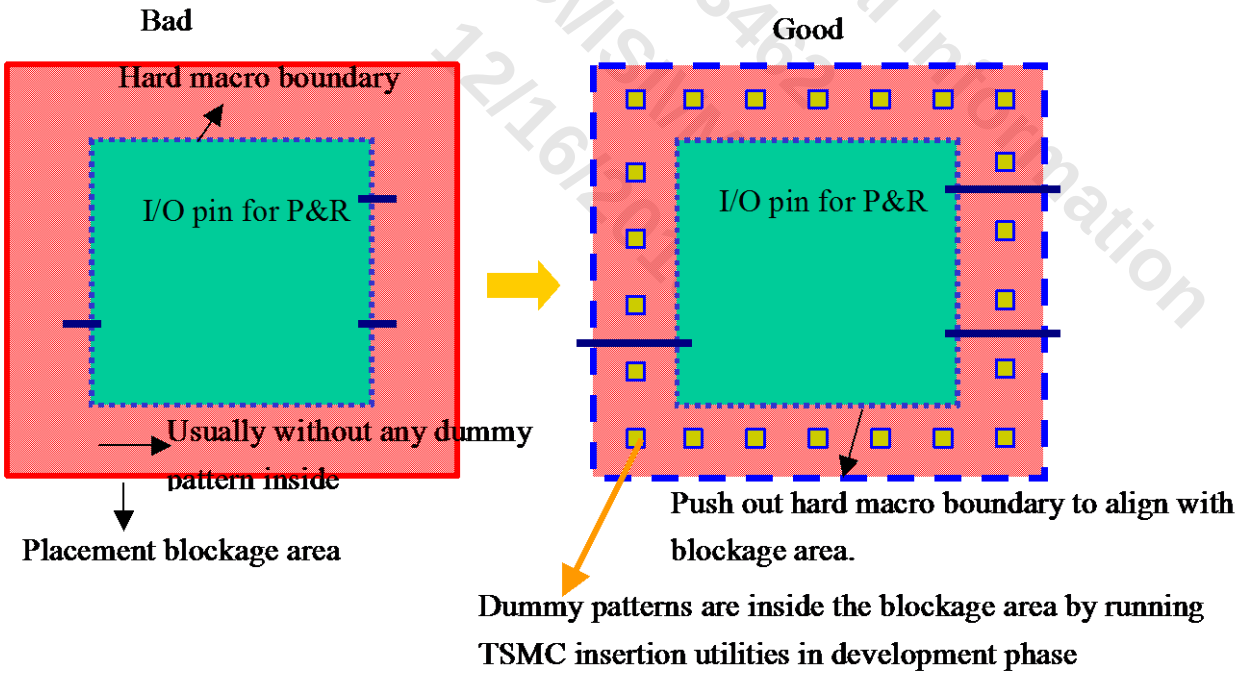

Figure 9.1.6 Dummy insertion for library/IP/Macro blockage area

9.1.4 Guidelines for Mask Making Efficiency

Please refer to these Chapter 3 sections:

- "Design Geometry Restrictions"
- "Design Hierarchy Guidelines"

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9.2 DFM Recommendations and Guidelines Summary

- Please use the following advisory/recommended dimensions and guidelines whenever possible, unless doing so impacts chip size or performance.
- DFM does not have to comply to the advisory/recommendation value completely. Any change even by one grid helps.
- By using DFM recommendations and guidelines, higher precision of models, better reliability, lower timing, process or yield variation may be expected.
- If your circuit has concern about the DFM Action-Required rules (9.2.1) and Recommendations (9.2.2) TSMC DRC deck can help you to flag the violations. DFM DRC deck is bundled in the TSMC logic DRC deck. The following 2 methods can specify the region to run DFM recommendations in DFM DRC deck. Please also refer to the "User Guide" in the DFM deck
  1. Dummy layer:
     - RRuleRequire(CAD layer: 182;1): for the DFM Action Required recommendations.
     - RRuleRecommend(CAD layer: 182;2): for the DFM Recommended recommendations
  2. Cell selection based on the following variables:
     - CellsForRRuleRequired.
     - CellsForRRuleRecommended

9.2.1 Action-Required Rules

Using minimum dimension of the following rules may have influence on the electrical characteristics (e.g. Idsat) of a related device. It is required that either the concerned influence be taken into account in a circuit electrical design if a dimension is less than the advisory point, or the advisory value be used. In order to have precisely CKT simulation, user needs to turn on the DFM-LPE (RC extraction tool, builded in TSMC LVS released package under the directory "DFM") option for PO.S.2®, PO.EX.2®, PO.S.5®, to get the optimized device parameter.

No.	Description		Advisory	Min. Rule
PO.S.2®	Recommended GATE space in the same OD in LP/GP/LPG/ULP process to avoid Isat degradation.	≥	0.2	0.13
PO.EX.2®	Recommended OD extension on PO (full and symmetrical contact placement are recommended at both source and drain side) to avoid Isat degradation, especially for channel width > 1μm.	≥	0.18	0.115
PO.S.5®	Recommended space to L-shape OD when PO and OD are in the same MOS [channel width (W) ≥ 0.15 μm] for stable Isat (avoid corner rounding effect)	≥	0.1	0.05 (PO.S.4)
	Recommended max. L-leg length when PO and OD are in the same MOS [channel width (W) ≥ 0.15 μm], if J<0.1. The recommendation is for stable Isat (avoid corner rounding effect)	≤	0.21	-

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9.2.2 Recommendations

Using minimum dimension of the following rules is okay. If a non-minimum recommendation is used, however, the variation of the related electrical parameter (e.g. contact or via Rc) can be minimized and yield benefit may be expected. It is recommended that the Recommendations be used wherever possible.

No.	Description	Recommended		Min Rule
OPC.R.1®	Recommended 45-degree edge length (Figure 3.7.3) for OPC friendly layout	≥	0.27	-
DNW.EN.1®	Recommended enclosure by NW for better noise isolation	≥	1.0	-
OD.W.2®	Recommended width of MOS(≤ 1.2V) [for core device]	≥	0.15	0.12
OD.S.1®	Recommended minimum OD space to reduce the short possibility caused by particle	≥	0.14	0.11
OD.S.6®	Recommended space to OD [OD area > 4,000,000 μm²].	≥	0.35	-
NWROD.S.3®	Recommended RPO space to CO in NW resistor within OD for SPICE simulation accuracy	=	0.3	-
NWROD.R.1®	Recommended length/width ≥ 5, length ≥ 20 in NW resistor within OD for SPICE simulation accuracy (length/width is un-checkable).			
NWRSTI.EN.2®	Recommended OD enclosure of CO in NW resistor under STI for SPICE simulation accuracy	=	0.3	-
NWRSTI.R.1®	Recommended length/width ≥ 5, length ≥ 20 in NW resistor within OD for SPICE simulation accuracy (length/width is un-checkable).			
PO.S.1®	Recommended minimum interconnect PO space to reduce the short possibility caused by particle	≥	0.15	0.12
PO.S.4.1®	Recommended gate space when the area enclosed by L-shape OD and L-shape PO< 0.0196 μm² for PO/OD rounding effect	≥	0.2	0.15
PO.S.11®	Recommended space of gate poly [channel length ≤ 0.08um] to neighboring poly for PO gate CDU control.	<	1.0	0.13
PO.S.13®	Recommended using the space ranges of gate poly to neighboring poly for sensitive circuit with minimum PO width = 0.06 μm. For space < 0.19 μm, extend the space whenever possible. The recommendation is for PO gate CDU control	=	0.19~0.27/ 0.295~0.39/ 0.455~0.94	0.13
	For sensitive circuit which needs precisely device parameter control, e.g. constant current source or differential input pair, please follow the subsequent four recommendations, PO.S.14®, PO.EN.1®, PO.EN.2®, and PO.EN.3®. The recommendations are for well proximity effect. Please refer to the section 7.2.			
PO.S.14®	Recommended 1.0V or 1.2V NMOS gate space to {OD2 OR (NW OR NT_N)}, to reduce the impact by well proximity effect.	≥	1.0	-
PO.EN.1®	Recommended 1.0V or 1.2V PMOS gate enclosure by {(NW NOT OD2) NOT NT_N} for 3.3V IO process, to reduce the impact by well proximity effect.	≥	1.0	-
	Recommended 1.0V or 1.2V PMOS gate enclosure by (NW NOT NT_N) for 1.8V or 2.5V IO process, to reduce the impact by well proximity effect.	≥	1.0	-
PO.EN.2®	Recommended 1.8V or 2.5V or 3.3V NMOS gate enclosure by {OD2 NOT (NW OR NT_N)}, to reduce the impact by well proximity effect.	≥	2.0	-
PO.EN.3®	Recommended 3.3V PMOS gate enclosure by {(NW AND OD2) NOT NT_N}, to reduce the impact by well proximity effect.	≥	1.5	-

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No.	Description	Recommended		Min Rule
	Recommended 1.8V or 2.5V PMOS gate enclosure by (NW NOT NT_N), to reduce the impact by well proximity effect.	≥	1.5	-
RES.2®	Recommended minimum width(W), length(L) and square number (L/W) for unsilicided OD/PO resistor for SPICE simulation accuracy. Square number can not be checked by DRC Width ≥ 0.4 μm (Checked by DRC) Length ≥ 0.4 μm (Checked by DRC) Square number ≥ 1 (Not checked by DRC)	≥	0.4(width) 0.4(length) 1 (L/W)	-
RES.5m®	Recommended CO space to unsilicided OD/PO resistor = 0.22 (S) for SPICE simulation accuracy.			
RES.8®	**For unsilicided OD resistor in the source or drain of MOS** Recommended RH space to Gate of unsilicided OD resistor in the source or drain of MOS for SPICE simulation accuracy.	≥	0.185	-
RES.9®	**For unsilicided OD/PO resistor** Recommended RH enclosure of unsilicided OD/PO resistor for SPICE simulation accuracy.	≥	0.13	-
CO.S.3®	Recommended CO space to GATE to reduce the short possibility caused by particle	≥	0.065	0.055
CO.EN.1®	Recommended CO enclosure by OD to avoid high Rc.	≥	0.04	0.015
CO.EN.3®	Recommended CO enclosure by PO [at least two opposite sides] to avoid high Rc.	≥	0.06	0.04
M1.S.1®	Recommended M1 space to reduce the short possibility caused by particle	≥	0.12	0.09
M1.S.7®	Recommended space between two non-M1 regions [one of the non-M1 area > 4,000,000μm²] for mask ESD concern. Non-M1 region is defined as {NOT (M1 OR DM1)} e.g. enlarge the metal width ≥ 0.35 for the guard-ring design.	≥	0.35	-
M1.EN.1®	Recommended M1 enclosure of CO to avoid high Rc	≥	0.04	0.00
M1.EN.2®	Recommended M1 enclosure of CO [at least two opposite sides] to avoid high Rc	≥	0.06	0.04
VIAx.EN.1®	Recommended VIAx enclosure by Mx or M1 to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	≥	0.04	0.00
VIAx.EN.2®	Recommended VIAx enclosure by Mx or M1 [at least two opposite sides] to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	≥	0.07	0.04
VIAx.R.8®	Recommended maximum consecutive stacked VIAx layer, which has only one via for each VIAx layer to avoid high Rc. (Example: VIA1~VIA4, VIA2~VIA5, VIA3~VIA6. This rule does not apply to top via. It is allowed to stack from VIA3 to VIA8 because VIA7 and VIA8 are top via. It is allowed to stack more than four VIAx layers if two or more vias in each VIAx layer are on the same metal.)	≤	4	-
Mx.S.1®	Recommended Mx space to reduce the short possibility caused by particle	≥	0.13	0.10
Mx.S.7®	Recommended space between two non-Mx regions [one of the non-Mx area > 4,000,000μm²]. Non-Mx region is defined as {NOT (Mx OR DMx)} e.g. enlarge the metal width ≥ 0.35 for guard-ring design.	≥	0.35	-
Mx.EN.1®	Recommended Mx enclosure of VIAx-1 to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	≥	0.04	0.00
Mx.EN.2®	Recommended Mx enclosure of VIAx-1 [at least two opposite sides] to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	≥	0.07	0.04

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No.	Description	Recommended		Min Rule
VIAy.EN.1®	Recommended enclosure by Mx or My to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	≥	0.05	0.00
VIAy.EN.2®	Recommended enclosure by Mx or My [at least two opposite sides] to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	≥	0.08	0.05
My.S.6®	Recommended space between two non-My regions [one of the non-My area > 4,000,000μm²]. Non-My region is defined as {NOT (My OR DMy)}. e.g. enlarge the metal width ≥ 0.35 for the guard-ring design.	≥	0.35	-
My.EN.1®	Recommended enclosure of VIAy-1 to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	≥	0.05	0.00
My.EN.2®	Recommended enclosure of VIAy-1 [at least two opposite sides] to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.37.	≥	0.08	0.05
AP.W.2®^{U}	Recommended total width of BUS line [Connect with bond pad]	≥	15	-

M1.EN.0®: Recommended enclosure of CO is defined by either M1.EN.1® or M1.EN.2®.

VIAx.EN.0®: Recommended enclosure by Mx or M1 is defined by either VIAx.EN.1® or VIAx.EN.2®.

Mx.EN.0®: Recommended enclosure of VIAx-1 is defined by either Mx.EN.1® or Mx.EN.2®.

VIAy.EN.0®: Recommended enclosure by Mx or My is defined by either VIAy.EN.1® or VIAy.EN.2®.

My.EN.0®: Recommended enclosure of VIAy-1 is defined by either My.EN.1® or My.EN.2®.

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9.2.3 Guidelines

The followings are guidelines regarding layout design practice, although they cannot be quantified. These guidelines should be observed to their maximum in any circuit designs.

Rule No.	Description	Label		Rule
G.6g[U]	For OD, PO, VTL_N, VTL_P, VTH_N, VTH_P, NP, PP, M1, Mx, My, all vertices and intersections of 45-degree polygon must be on an integer multiple of 0.005 μm except PO inside the layer 186;5.			
OPC.R.2g	Avoid small jogs (Figure 3.7.5). It is recommended to use greater than, or equal to, half of the minimum width of each layer for each segment of a jog.			
OD.L.2g[U]	Recommended to limit the maximum interconnect OD length as short as possible to avoid high Rs variation by salicidation.			
NW.R.1g	Recommended not using floating well unless necessary, to avoid unstable device performance. DRC can flag both NW is not with CO in NPOD and PW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.			
DNW.R.6g	Recommend not using floating RW unless necessary, to avoid unstable device performance. DRC can flag RW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.			
NWROD.R.3g	Recommended to use rectangle shape resistor for the SPICE simulation accuracy. DRC can flag {NWDMY AND NW} is not a rectangle.			
NWRSTI.R.3g	Recommended to use rectangle shape resistor for the SPICE simulation accuracy. DRC can flag {NWDMY AND NW} is not a rectangle.			
PO.L.1g[U]	Recommended to limit the maximum interconnect PO length as short as possible to avoid high Rs variation by salicidation.			
CO.S.6g	Recommended to put contacts at both source side and butted well pickup side to avoid high Rs. DRC can flag if the STRAP is butted on source, one of STRAP and source is without CO.			
CO.R.1g[U]	Recommend to put {CO inside PO} space to GATE as close as possible to avoid high Rs			
CO.R.5g	Recommend using redundant CO to avoid high Rc wherever layout allows 1. Recommended to use double CO or more on the resistor connection. 2. Double CO on Poly gate to reduce the probability of high Rc 3. Recommend putting multiple and symmetrical source/drain CO for SPICE simulation accuracy. 4. If it is hard to increase the CO to gate spacing (CO.S.3®) for the large transitor, limit the number of source/drain CO: to have the necessary CO number for the current, and then distribute the CO evenly on the Source/Drain area. If possible, also increase the CO to gate spacing (to reduce the short possibility by particle) 5. DRC can flag single CO.			
VIAx.R.9g	Recommend using redundant vias to avoid high Rc wherever layout allows. Please refer to the “Via Layout Recommendations” in the section 4.5.37. DRC can flag single via.			
VIAy.R.9g	Recommend using redundant vias to avoid high Rc wherever layout allows. Please refer to the “Via Layout Recommendations” in the section 4.5.37. DRC can flag single via.			

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Rule No.	Description	Label		Rule
VIAz.R.5g	Recommend using redundant vias to avoid high Rc wherever layout allows. DRC can flag single via.			
VIAr.R.5g	Recommend using redundant vias to avoid high Rc wherever layout allows. DRC can flag single via.			
Mx.R.2g[U]	For the small space, recommended to enlarge the metal space, by using Wire Spreading function of EDA tool, to reduce the wire capacitance and the possibility of metal short. Please refer to section 9.1.1 and TSMC Reference flow.			
My.R.2g[U]	For the small space, recommended to enlarge the metal space, by using Wire Spreading function of EDA tool, to reduce the wire capacitance. Please refer to section 9.1.1 and TSMC Reference Flow.			
CBM.R.2g [U]	Circuits under MIM are allowed from process point of view. But the parasitic and signal coupling effects should be considered by designers. It is recommended to add metal shielding between MIM capacitor and underneath routing or circuits. One can refer to section 4.6.3 for circuit under MIM layout options.			
VIAz.R.6g[U]	For MIM application, please put as many VIAz as possible for both CTM and CBM connections.			
UBM.R.4g [u]	• It is recommended not to put any bump on the top of SRAM, analog, sensitive circuits, and the matching pairs. o The circuits should be located at a minimum distance of 60 µm from the bump pad's PM or CBD edge. o It is also recommended to consider UBM.S.4® at the same time. o If bump over SRAM, analog, or sensitive circuit areas is needed, it is recommended to use the ultra-low alpha particle materials in the bump and assembly processes (solder bump, under-fill, pre-solder bump…) to avoid a high Soft Error Rate (SER). o TSMC uses ultra-low alpha particle materials in the solder bump process. If you could not meet UBM.S.4® and UBM.R.4g at the same time, you can consult TSMC for the layout suggestions.			
UBM.R.5g [u]	It is recommended not to place the IO bump pads in the 2nd and 3rd row in the bump array corner, but put Vss, Vdd, or dummy bump pads.			

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9.2.4 Grouping Table of DFM Action-Required Rules, Recommendations and Guidelines

No.	1st priority to implement for yield and performance enhancement	Systematic			Defect	SPICE
		CMP	Litho/OPC	Others		
PO.S.2®			v	v		v
PO.S.14®				v		v
PO.EN.1®				v		v
PO.EN.2®				v		v
PO.EN.3®				v		v
PO.EX.2®				v		v
PO.S.5®			v			v
OPC.R.1®			v			
DNW.EN.1®				v		
OD.W.2®						v
OD.S.1®					v	
OD.S.6®				v		
NWROD.S.3®						v
NWROD.R.1®						v
NWRSTI.EN.2®						v
NWRSTI.R.1®						v
PO.S.1®					v	
PO.S.4.1®						v
PO.S.11®			v			
PO.S.13®			v			
PO.S.5m®						v
PO.S.6.m®						v
RES.2®						v
RES.5m®						v
RES.8®						v
RES.9®						v
CO.S.3®	v			v	v	
CO.EN.1®			v			v
CO.EN.3®			v			v
M1.S.1®					v	
M1.S.7®				v		
M1.EN.0®	v			v		
M1.EN.1®	v		v			v
M1.EN.2®	v		v			v
VIAx.EN.0®	v			v		
VIAx.EN.1®	v		v			v
VIAx.EN.2®	v		v			v
VIAx.R.8®		v				
Mx.S.1®					v	
Mx.S.7®				v		
Mx.EN.0®	v			v		
Mx.EN.1®	v		v			v

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No.	1st priority to implement for yield and performance enhancement	Systematic			Defect	SPICE
		CMP	Litho/OPC	Others		
Mx.EN.2®	v		v			v
VIAy.EN.0®	v			v		
VIAy.EN.1®	v		v			v
VIAy.EN.2®	v		v			v
My.S.6®				v		
My.EN.0®	v			v		
My.EN.1®	v		v			v
My.EN.2®	v		v			v
AP.W.2®^{U}				v		
DTCD.DN.1®			v			
G.6g^{U}			v			
OPC.R.2g			v			
OD.L.2g^{U}					v	
NW.R.1g				v		v
DNW.R.6g				v		v
NWROD.R.3g						v
NWRSTI.R.3g						v
PO.L.1g^{U}					v	
CO.S.6g						v
CO.R.1g^{U}						v
CO.R.5g	v				v	v
VIAx.R.9g	v				v	v
VIAy.R.9g	v				v	v
VIAz.R.5g	v				v	v
VIAr.R.5g	v				v	v
Mx.R.2g^{U}				v	v	
My.R.2g^{U}				v	v	
VIAz.R.6g^{U}				v		
BJT.R.2®						v
ESDIMP.EN.1®				v		

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9.3 GDA die size optimization kit

- Gross Die Advisor (GDA) is to optimize die size x-y for both mask field allocation and gross die maximization.
- The function of GDA is based on user input die size, target gross die and TSMC generic fabrication condition to estimate gross die count, and recommend a list of the other die size combination (X / Y) with higher gross die and MFU>80% criterion. Based on GDA result, user can choose the best combination of die size and gross die to meet the project need in the early design phase.
- Use GDA function from TSMC on-line
  - TSMC On-line Directory: Home/Design Porotal 2.0/Technology Selection (GDA)/Gross Die Advisor (GDA)

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9.3.1 What is MFU?

- Mask Field Utilization (MFU) is a ratio of mask utilized region which is calculated by (multiple die area+ scribe_line area) / (scanner maximum field area). (Fig.9.3.1.1)
- Low MFU implies low scanner productivity at whole lithography layers. It is important to improve MFU as possible as you can. MFU>80% is strong recommended.

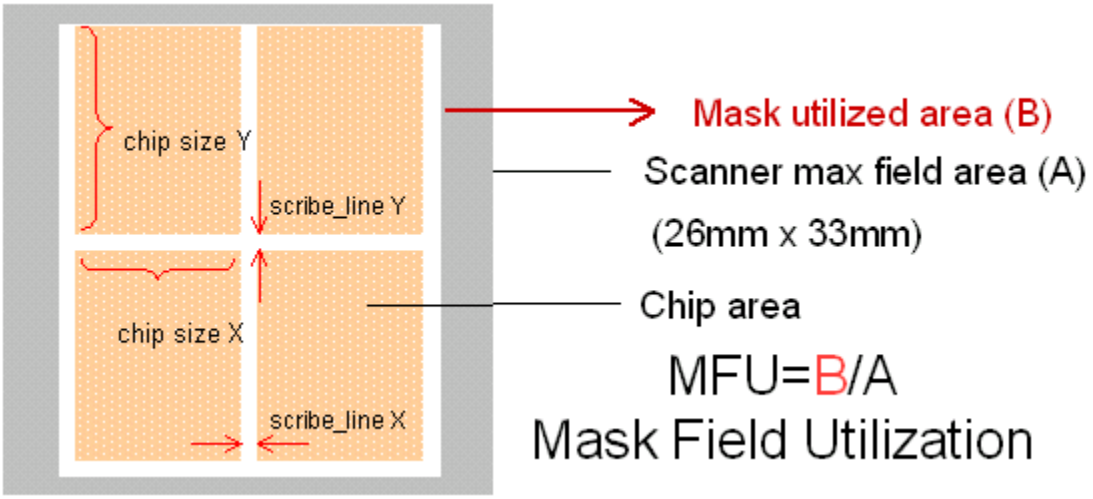

Figure 9.3.1.1 Example of MFU

9.3.2 Recommended GDA criteria MFU>80%

- The benefits from GDA:
  - Simulate gross die count base on initial die size x-y at the early design stage.
  - Advise die size x-y for better gross die count and MFU>80% simultaneously.
- The MFU ratio is calculated by (die size+assembly isolation +sealring+ scribe-line Area) / (maximum scanner field size).

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10 Layout Guidelines for Latch-Up and I/O ESD

This chapter consists of the following 2 Sections:

10.1 Layout rules and guidelines for latch-up prevention

10.2 I/O ESD protection circuit design and layout guideline

10.1 Layout Rules and Guidelines for Latch-up Prevention

10.1.1 Latch-up Introduction

Before latch-up, the parasitic components of an inverter can be modeled as the equivalent circuit in Figure 10.1.1. As the output signal is higher than Vdd+0.7V (overshooting), the bipolar VT2 turns on first. As the output signal is lower than –0.7V (undershooting), the bipolar LT2 turns on first. The collector of each BJT is connected to the base of the other transistor and can inject the minority carriers to the well to induce a potential difference between PW and Vss, or NW and Vdd, to forward the base to emitter junction of the other transistor (LT1 or VT1), resulting in the other transistor turning on. When both BJT's, which connect to Vdd (VT1) and Vss (LT1), turn on, the injected minority carrier concentrations are increased higher than the doping concentrations of NW and PW (Figure 10.1.2). Subsequently, NW and PW disappear and a heavy conductivity region creates a low resistance path between Vdd and Vss (please refer to JH Lee et. al, “The positive trigger lowering effect for latch-up,” in IPFA, p. 85, 2004). This may induce a circuit malfunction, and destroy the device in the worst case.

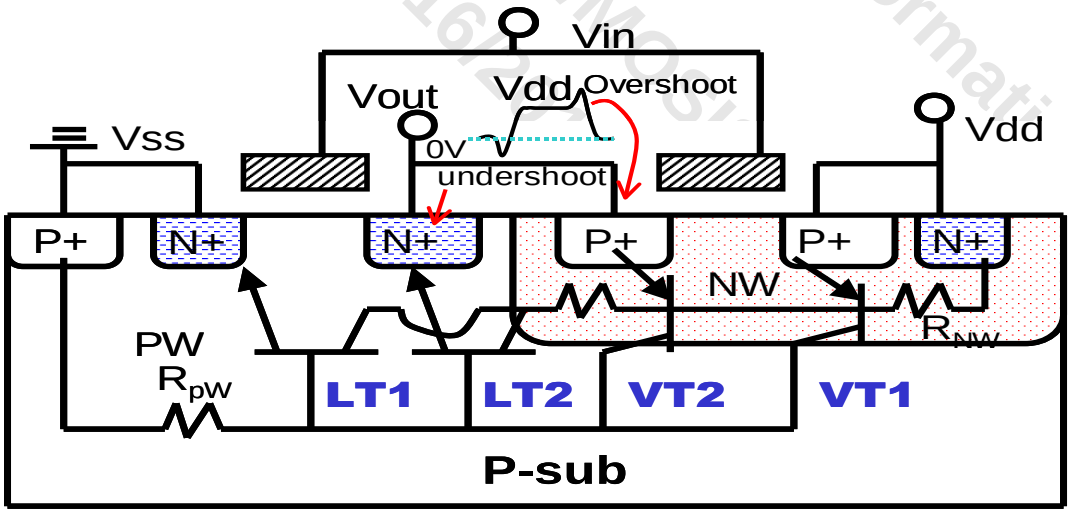

Fig. 10.1.1 Lump element model for an inverter before latch-up

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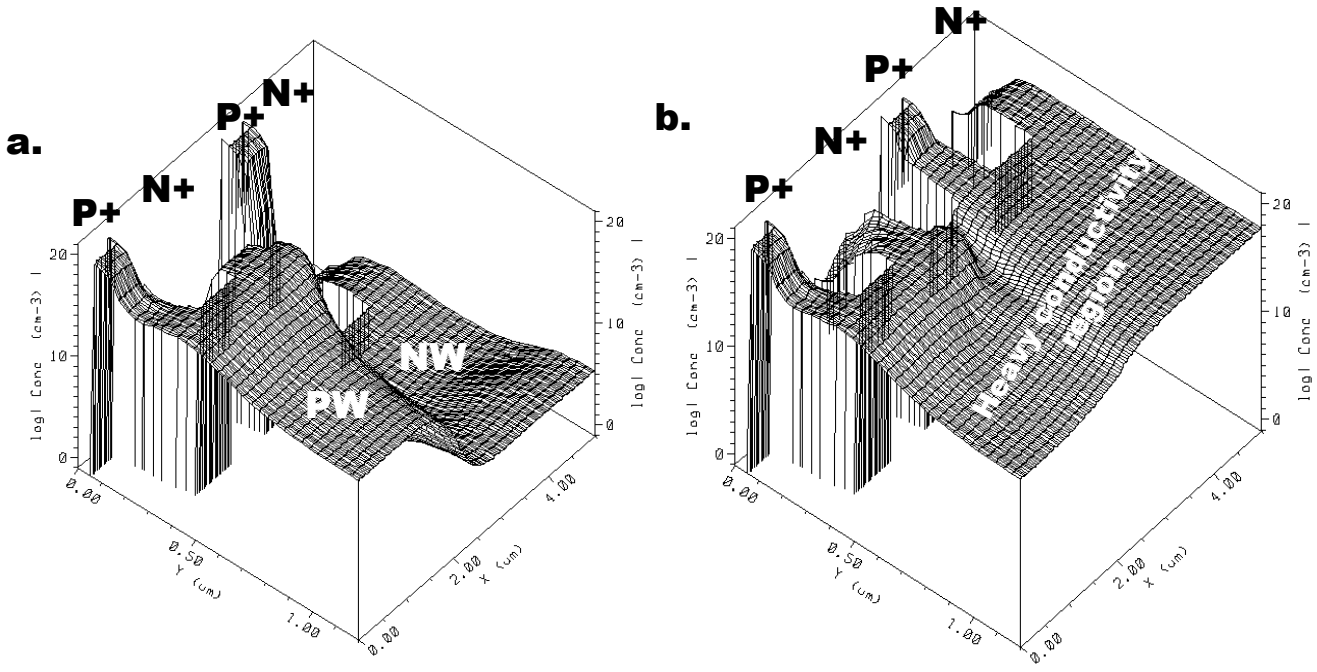

Fig. 10.1. 2 Hole concentrations (a) before latch-up, (b) after latch-up

The latch-up trigger sources often come from the IO Pad, but both IO circuits and internal circuits might cause a latch-up if the layout does not follow the latch-up design rules. The following lists the latch-up failure cases caused by layout rule violations.

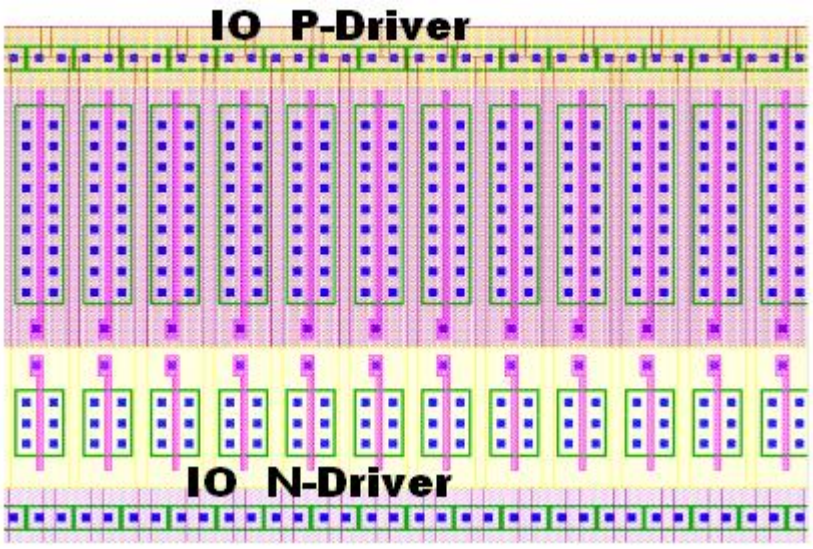

Fig. 10.1.3 LUP. 1 rule violation: (IO without guard-ring)

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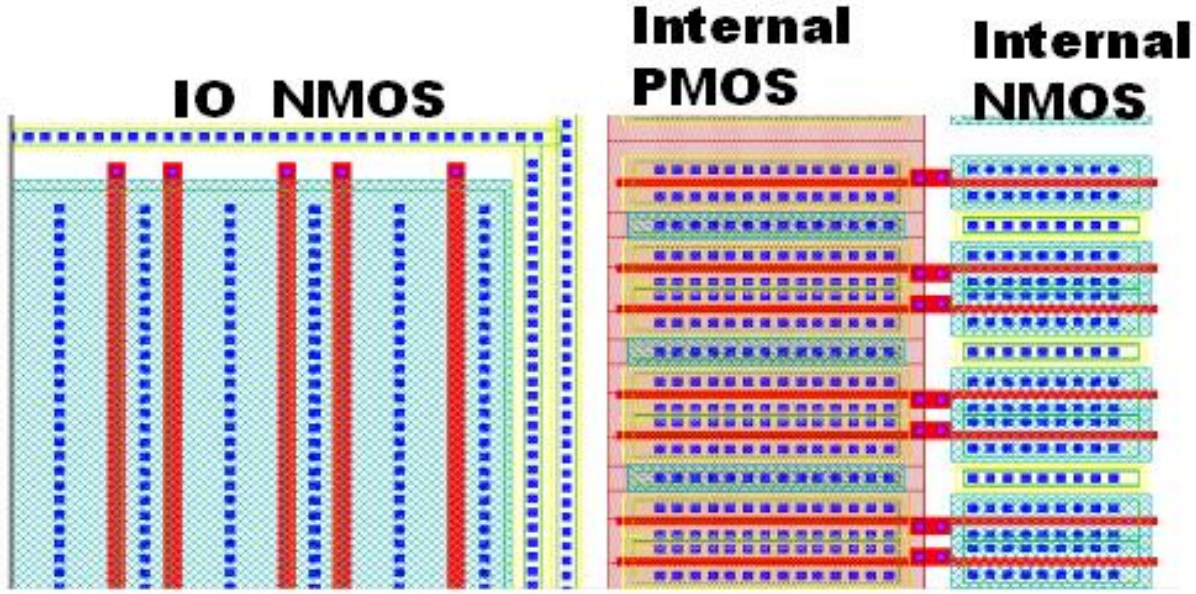

Fig. 10.1.4 LUP. 2 rule violation:
(Within 20um from IO, N/PMOS in the internal circuit without the guard-ring)

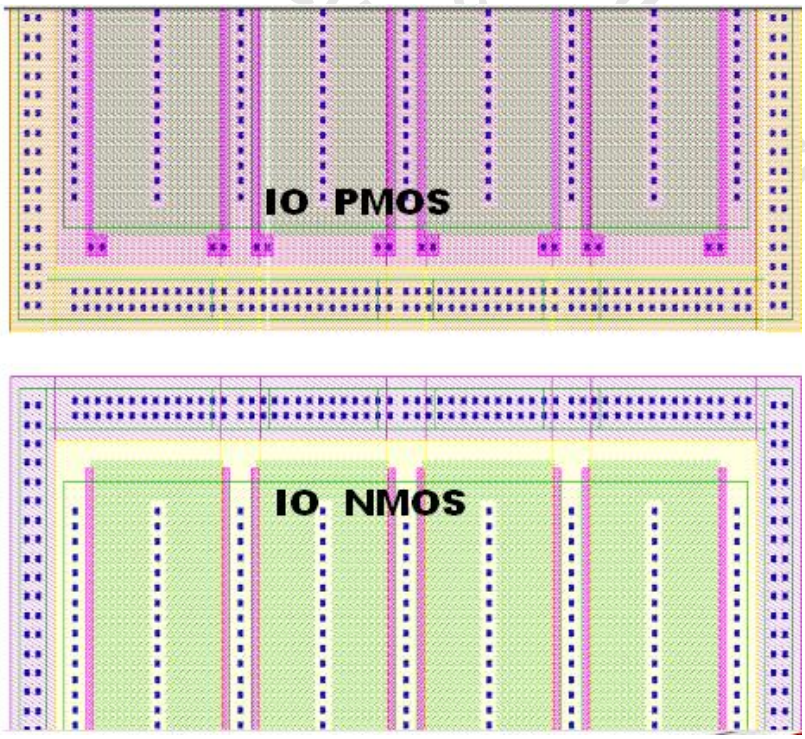

Fig. 10.1.5 LUP. 3 rule violation: (too short IO N/PMOS space)

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The following figure shows the latch-up failure if the layout does not violate any latch-up design rule. The displacement current (Cdv/dt) may induce the internal circuit latch-up if the internal circuit is nearby the capacitors and is not separated by a P+ strap. Please separate the internal circuit and capacitor by a P+ strap to inhibit the displacement current to induce the latch-up.

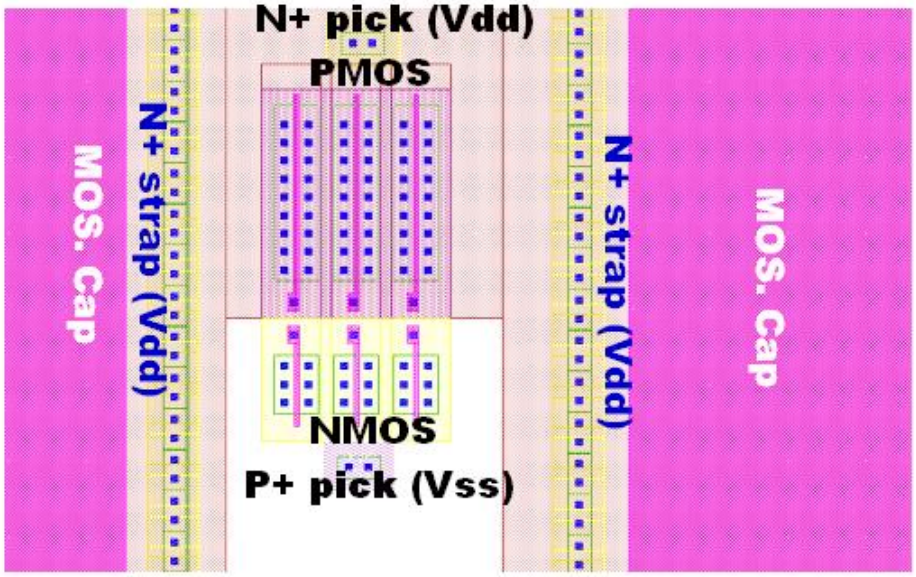

Fig. 10.1.6 LUP.8g violation, but DRC can not flag it:
(Inverter and capacitor are not separated by P+ guard-ring)

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10.1.2 Layout Rules and Guidelines for Latch-up Prevention

10.1.2.1 Special Definition in Latch-up Prevention

Term	Definition
I/O pads	Do not include Vdd pad and Vss pad.
Internal circuit	Include NMOS, PMOS, de-coupling capacitors and varactor that do not connect to an IO pad.
Guard-ring	Complete un-broken ring-type OD and M1 with CO as many as possible, connected to Vdd or Vss.
N+ guard-ring	Complete un-broken ring-type (NP AND OD) and M1 with CO as many as possible, connected to Vdd.
P+ guard-ring	Complete un-broken ring-type (PP AND OD) and M1 with CO as many as possible, connected to Vss.
NMOS cluster	A group of NMOSs
PMOS cluster	A group of PMOSs
OD injector	Any OD directly connected to I/O pad. Ex. MOS, HIA diode, diode string (DRC uncheckable), OD resistor, and well resistor directly connected to I/O PAD. N+ OD directly connected to I/O pad is N+ OD injector. P+ OD directly connected to I/O pad is P+ OD injector.

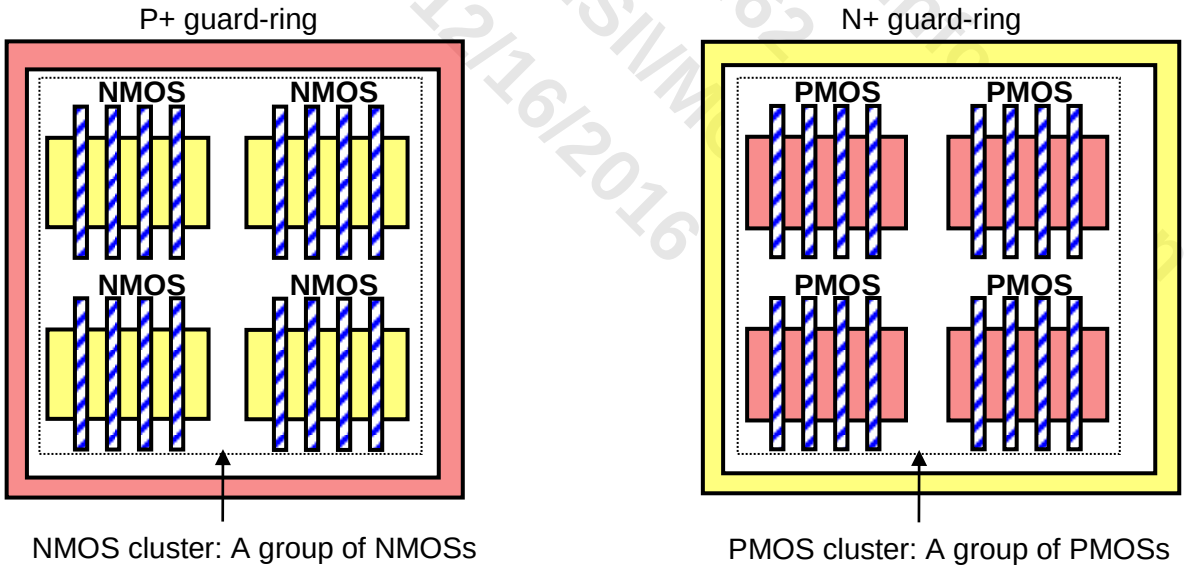

Fig. 10.1.7 Example of an NMOS cluster and a PMOS cluster

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10.1.2.2 Latch-up Dummy Layers Summary

10.1.2.2.1 LUPWDMY Dummy Layer (CAD layer: 255;1)

LUPWDMY is a dummy layer to waive these guidelines, LUP.1g, LUP.2g, LUP.3.1.1~2g, LUP.3.2.1~2g, LUP.3.3.1~2g, LUP.3.4.1~2g, LUP.3.5.1~2g, LUP.4, LUP.5.1.1~2g, LUP.5.2.1~2g, LUP.5.3.1~2g, LUP.5.4.1~2g and LUP.5.5.1~2g.

- Condition:
  - It is not recommended to use this layer before silicon is proven at the package.
  - Please consult TSMC if you would like to follow it as rules and have DRC violations before tapeout.
- Usage:
  - Draw LUPWDMY to fully cover MOS/ACTIVE OD/ Diode regions that are connected to I/O pads, including the source, gate, drain, and diode, but not necessarily to cover Well STRAP, guard-ring.
  - It is for DRC usage but not a tapeout required CAD layer.

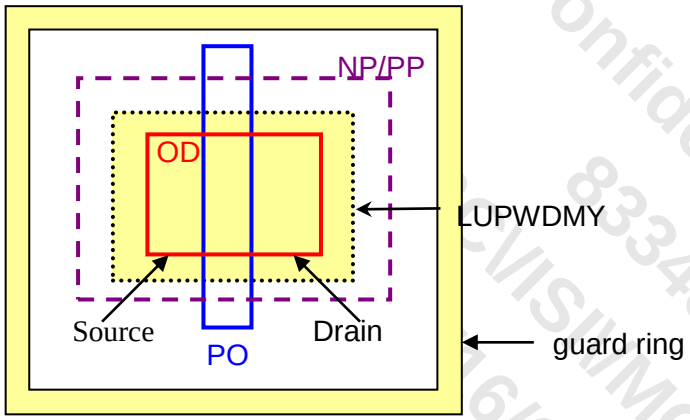

Fig. 10.1.8 Example of LUPWDMY

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10.1.2.3 DRC methodology for Latch-up Rules

10.1.2.3.1 DRC methodology for LUP.1

- OD injector is defined by any OD directly connected to I/O pad.
- Ex. MOS, STI diode (STI bonded), OD resistor, and well resistor directly connected I/O PAD.
    1. When an OD injector is covered by LUPWDMY (255;1), it is excluded by DRC from LUP.1 check.
    2. The guard ring can not be shared by different type devices

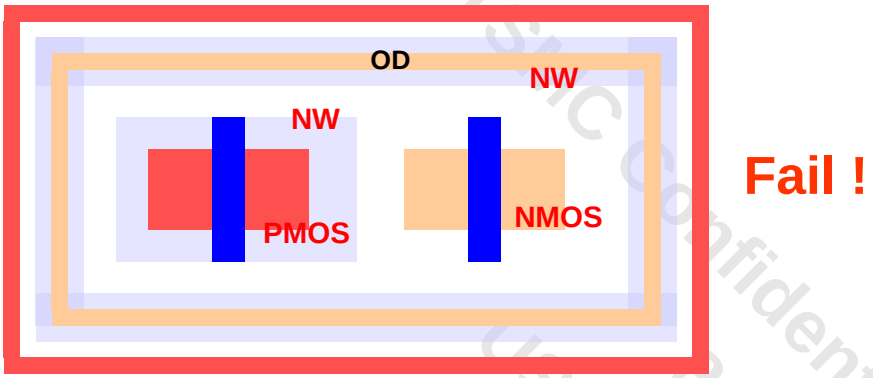

Fig. 10.1.9 example of illegal guard ring

10.1.2.3.2 DRC methodology for LUP.2

- DRC use the following features to find out the devices for LUP.2:
    1. The MOS OD within 15um space from the OD injector for LUP.1 check
    2. The following cases are excluded:
        - I. The MOS OD is floating without any contact over gate and S/D.
        - II. The OD injector is covered by LUPWDMY (255;1)
        - III. The NMOS is inside DNW, and the NW over DNW is not the same as the NW of relative PMOS, but these two NWs are connected.

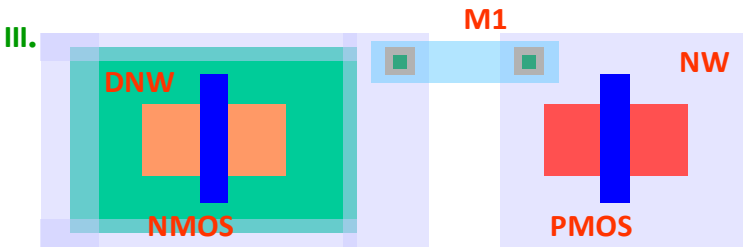

Fig. 10.1.10 example of LUP.2 III and IV

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10.1.2.3.3 DRC methodology for LUP.3 group

- DRC use the following features to find out the devices for LUP.3 group:
  1. Find out the OD injector for LUP.1 check
  2. The following cases are excluded:
     I. The excluded case in LUP.1.
     II. The NMOS is inside DNW, and the NW over DNW is not the same as the NW of relative PMOS, but these two NWs are connected.

10.1.2.3.4 DRC methodology for LUP.4

- DRC use the following features to check the guard-ring width.
  1. Find out the OD injectorfor LUP.1 & LUP.2 check.
  2. The devices should be placed inside a complete guard-ring with width >= 0.12um.

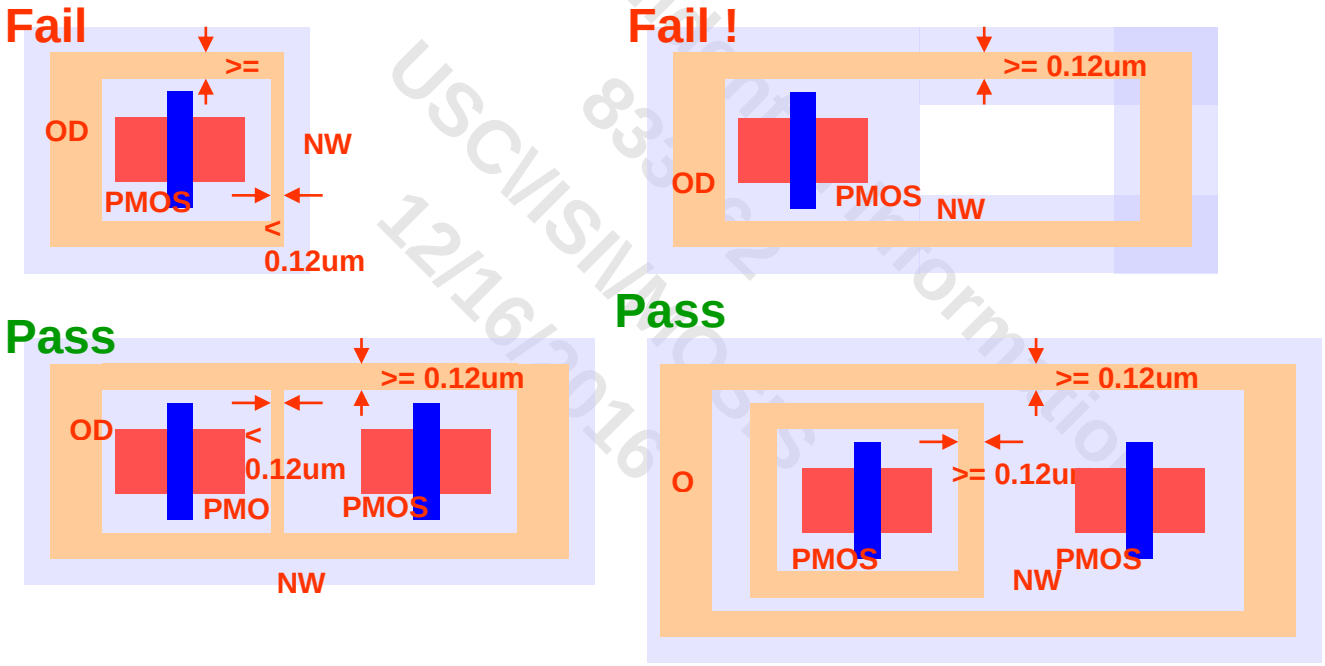

Fig. 10.1.11 example of LUP.4

10.1.2.3.5 DRC methodology for LUP.5 group

- DRC use the following features to find out the devices for LUP.3 group:
  1. Find out the OD injector for LUP.1 & LUP.2 check.
  2. The excluded cases are “I”, “II”, and “IV” in LUP.2.

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10.1.2.4 Layout Rules and Guidelines for Latch-up Prevention

The LUP rules are for design reference to achieve the specifications proposed by TSMC. They are extracted by the standard digital I/O and Area I/O test structures. Note that Latch-up free can not be guaranteed for all applications such as substrate bias condition, floating body circuits, SCR ESD IPs, etc.

The following latch-up rules are only for 2.5V, 3.3V, and 5V HVMOS device.

Table 10.1.1 Layout Rules and Guidelines for Latch-up Prevention

Rule No.	Description	Label		Dimension (um)
LUP.1g	Any N+ OD injector or an N+ OD injector cluster connected to an I/O pad must be surrounded by a P+ guard-ring. (Figure 10.1.12) Any P+ OD injector or a P+ OD injector cluster connected to an I/O pad must be surrounded by a N+ guard-ring. (Figure 10.1.12) Please also refer to LUP.9g for further information.			
LUP.2g	Within 15um space from the OD injector, a P+ guard-ring is required to surround an NMOS or an NMOS cluster. And an N+ guard-ring is required to surround a PMOS or a PMOS cluster. (Figure 10.1.14) NMOS guard-ring are exempt from the following conditions (Figure 10.1.13): If the NMOS is enclosed by a DNW, the NW of the checked PMOS does not interact with the DNW,and the voltage (Va) of the NW INTERACT DNW is ≥ the voltage (Vb) of the NW of the checked PMOS. However, DRC can only flag the different connection.			
LUP.3.0	LUP.3.1.1~2g, LUP.3.2.1~2g, LUP.3.3.1~2g, LUP.3.4.1~2g, LUP.3.5.1~2g, LUP.5.1.1~2g, LUP.5.2.1~2g, LUP.5.3.1~2g, LUP.5.4.1~2g can be exempt from if the NMOS meets the following conditions (Figure 10.1.13): If the NMOS is enclosed by a DNW, the NW of the checked PMOS does not interacte with the DNW, and the voltage (Va) of the NW INTERACT DNW is ≥ the voltage (Vb) of the NW of the checked PMOS. However, DRC can only flag the different connection.			
LUP.3.1.0	In LUP.3.1.1g and LUP.3.1.2g for the 1.2V or 1.0V N/PMOS which connects to an I/O pad, space between the NMOS and the PMOS. (Figure 10.1.12),			
LUP.3.1.1g	if all of guard-ring width ≥ 0.2um (e. g. width of guard-ring of LUP.1g)	A	≥	2
LUP.3.1.2g	if one of guard-ring width < 0.2um (e. g. width of guard-ring of LUP.1g)	A	≥	3
LUP.3.2.0	In LUP.3.2.1g and LUP.3.2.2g, for the 1.8V N/PMOS which connects to an I/O pad directly, (Figure 10.1.12) (1) space between the 1.8V NMOS and the 1.8V/1.2V/1.0V PMOS (2) space between the 1.8V PMOS and the 1.8V/1.2V/1.0V NMOS			
LUP.3.2.1g	if all of guard-ring width ≥ 0.2um (e. g. width of guard-ring of LUP.1g)	A	≥	2.3
LUP.3.2.2g	if one of guard-ring width < 0.2um (e. g. width of guard-ring of LUP.1g)	A	≥	4
LUP.3.3.0	In LUP.3.3.1 and LUP.3.3.2, for the 2.5V N/PMOS which connects to an I/O pad directly, (Figure 10.1.12) (1) space between the 2.5V NMOS and the 2.5V/1.2V/1.0V PMOS (2) space between the 2.5V PMOS and the 2.5V/1.2V/1.0V NMOS			
LUP.3.3.1g	if all of guard-ring width ≥ 0.2um (e. g. width of guard-ring of LUP.1g)	A	≥	2.6
LUP.3.3.2g	if one of guard-ring width < 0.2um (e. g. width of guard-ring of LUP.1g)	A	≥	5

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Rule No.	Description	Label		Dimension (um)
LUP.3.4.0	In LUP.3.4.1g and LUP.3.4.2g for the 3.3V N/PMOS which connects to an I/O pad directly, (Figure 10.1.12) (1) space between the 3.3V NMOS and the 3.3V/1.2V/1.0V PMOS (2) space between the 3.3V PMOS and the 3.3V/1.2V/1.0V NMOS			
LUP.3.4.1g	if all of guard-ring width ≥ 0.2um (e. g. width of guard-ring of LUP.1g)	A	≥	4
LUP.3.4.2g	if one of guard-ring width < 0.2um (e. g. width of guard-ring of LUP.1g)	A	≥	8
LUP.3.5.0	In LUP.3.5.1g and LUP.3.5.2g for the 5.0V HV N/PMOS which connects to an I/O pad, space between the NMOS and the PMOS (Figure 10.1.12). (1)space between the 5.0V/2.5V/1.2V PMOS. (2)space between the 5.0V/2.5V/1.2V NMOS			
LUP.3.5.1g	If all of guard-ring width ≥ 0.2um (e.g. width of guard-ring of LUP.1g)	A	≥	10
LUP.3.5.2g	If all of guard-ring width < 0.2um (e.g. width of guard-ring of LUP.1g)	A	≥	15
LUP.4g	Width of the N+ guard-ring and P+ guard-ring for the OD injector, and also MOS within 15um space from OD injector. (e. g. width of guard-ring of LUP.1g and LUP.2g)	B	≥	0.12
LUP.5.1.0	In LUP.5.1.1g and LUP.5.1.2g for the internal circuits within 15um space from 1.2V or 1.0V OD injector, (1) space between the 1.2V or 1.0V N+ OD injector connected to an I/O pad and the PMOS in the internal circuit (Figure 10.1.14) (2) space between the 1.2V or 1.0V P+ OD injector and the NMOS in the internal circuit (Figure 10.1.14)			
LUP.5.1.1g	if all of guard-ring width ≥ 0.2um (e. g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	2
LUP.5.1.2g	if one of guard-ring width < 0.2um (e. g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	3
LUP.5.2.0	In LUP.5.2.1g and LUP.5.2.2g for the internal circuits within 15um space from 1.8V OD injector, (1) space between the 1.8V N+ OD injector and the PMOS in the internal circuit (Figure 10.1.14) (2) space between the 1.8V P+ OD injector and the NMOS in the internal circuit (Figure 10.1.14)			
LUP.5.2.1g	if all of guard-ring width ≥ 0.2um (e. g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	2.3
LUP.5.2.2g	if one of guard-ring width < 0.2um (e. g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	4
LUP.5.3.0	In LUP.5.3.1g and LUP.5.3.2g for the internal circuits within 15um space from 2.5V OD injector, (1) space between the 2.5V N+ OD injector and the PMOS in the internal circuit (Figure 10.1.14) (2) space between the 2.5V P+ OD injector and the NMOS in the internal circuit (Figure 10.1.14)			
LUP.5.3.1g	if all of guard-ring width ≥ 0.2um (e. g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	2.6
LUP.5.3.2g	if one of guard-ring width < 0.2um (e. g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	5

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Rule No.	Description	Label		Dimension (um)
LUP.5.4.0	In LUP.5.4.1g and LUP.5.4.2g for the internal circuits within 15um space from 3.3V OD injector, (1) space between the 3.3V N+ OD injectorand the PMOS in the internal circuit (Figure 10.1.14) (2) space between the 3.3V P+ OD injector and the NMOS in the internal circuit (Figure 10.1.14)			
LUP.5.4.1g	if all of guard-ring width ≥ 0.2um (e. g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	4
LUP.5.4.2g	if one of guard-ring width < 0.2um (e. g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	8
LUP.5.5.0	In LUP.5.5.1g and LUP.5.5.2g for the internal circuits within 15um space from 5.0V OD injector. (1) space between the 5.0V N+ OD injector and the HV PMOS in the internal circuit. (Figure 10.1.14). (2) space between the 5.0V P+ OD injector and the HV NMOS in the internal circuit. (Figure 10.1.14)			
LUP.5.5.1g	If all of guard-ring width ≥ 0.2um (e.g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	10
LUP.5.5.2g	If all of guard-ring width < 0.2um (e.g. width of guard-ring of LUP.1g and LUP.2g)	C	≥	15
LUP.6	(1) Any point inside NMOS source/drain {(N+ACTIVE INTERACT PO) NOT PO} space to the nearest PW STRAP in the same PW. (Figure 10.1.15) (2) Any point inside PMOS source/drain {(P+ACTIVE INTERACT PO) NOT PO} space to the nearest NW STRAP in the same NW. (Figure 10.1.15) In SRAM bit cell region, the rule is relaxed from 30um to 40um.	D	≤	30
LUP.7g^{U}	All the guard-rings and STRAPs should be connected to VDD/VSS with very low series resistance. Use as many contacts and vias as possible.			
LUP.8g^{U}	A P+ guard-ring should separate a large capacitor and MOS.			
LUP.9g^{U}	Additional one N+ STRAP and one P+ STRAP are required to be inserted between the P+ guard-ring and N+ guard-ring for LUP.1 (Figure 10.1.12). And the N+ STRAP should isolate the P+ STRAP and the P+ guard-ring. And the P+ STRAP should isolate the N+ STRAP and the N+ guard-ring.			

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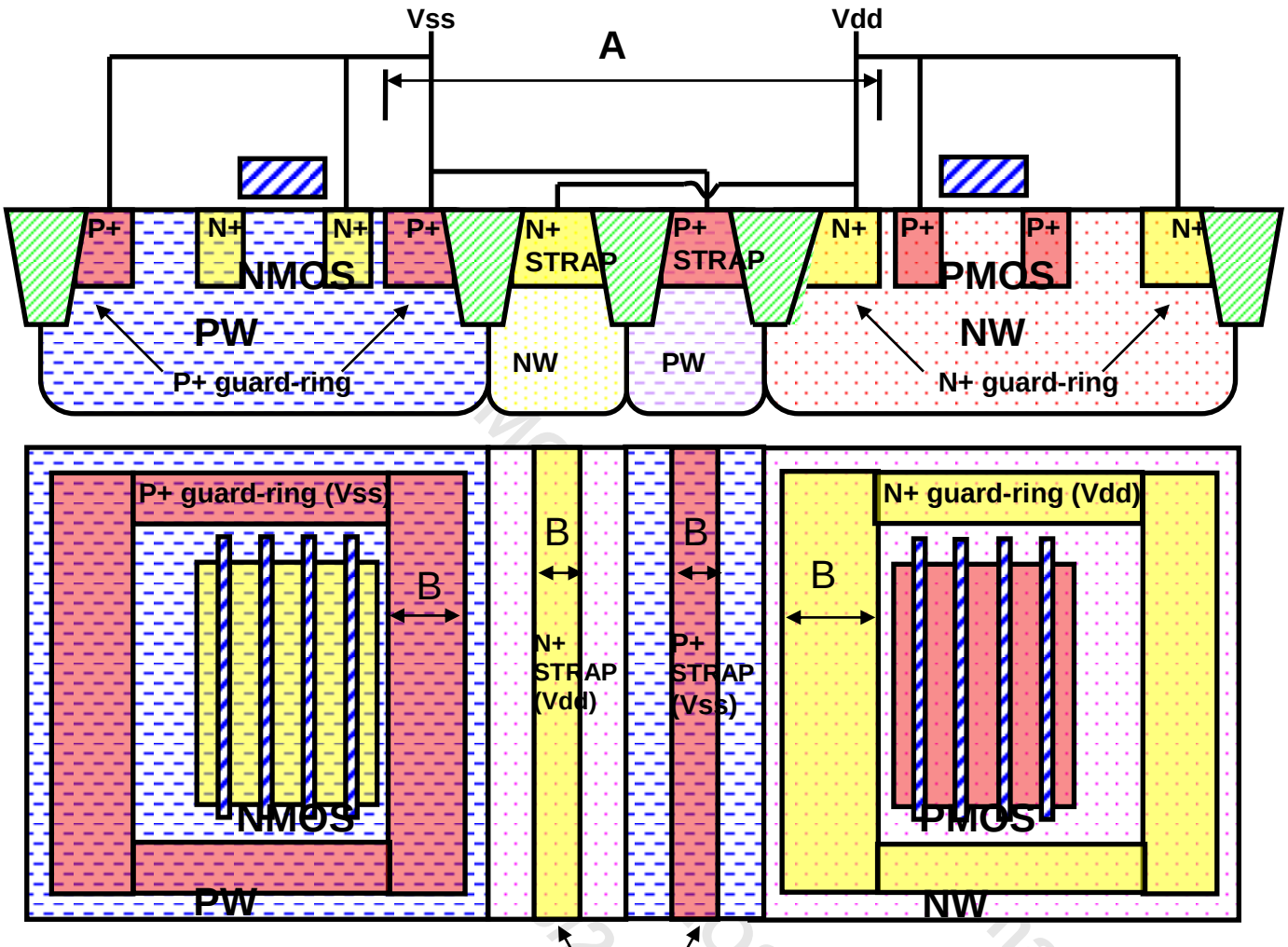

To exchange N+ STRAP and P+ STRAP not recommended (LUP.9g)

Figure 10.1.12

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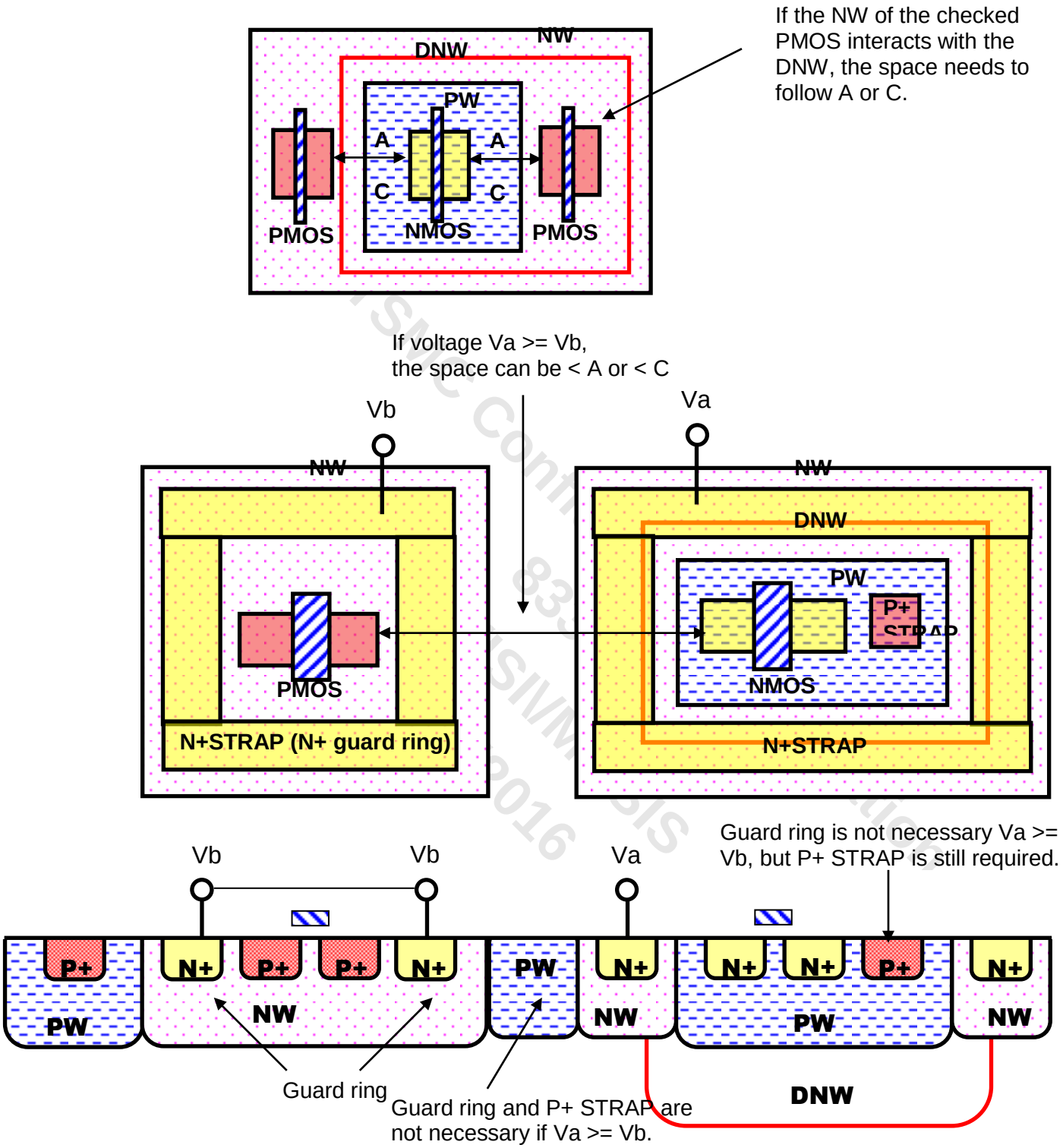

For LUP.2g, LUP.3.1.1~2g, LUP.3.2.1~2g, LUP.3.3.1~2g, LUP.3.4.1~2g, LUP.3.5.1~2g, LUP.5.1.1~2g, LUP.5.2.1~2g, LUP.5.3.1~2g, LUP.5.4.1~2g, LUP.5.5.1~2g,if voltage Va >= Vb, the above rules allow that the NMOS is enclosed by a DNW and the NW of the checked PMOS does not interact with the DNW. However, DRC can only flag the different connection.

Figure 10.1.13

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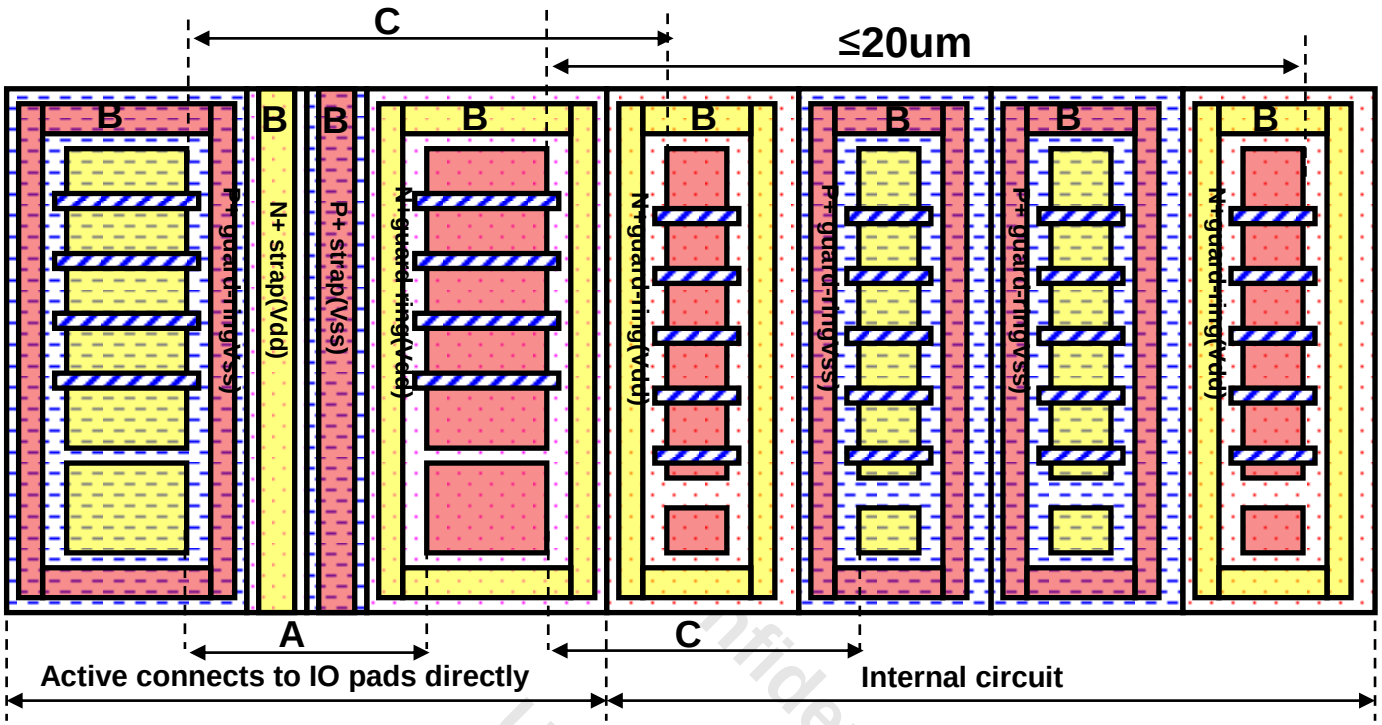

Figure 10.1.14

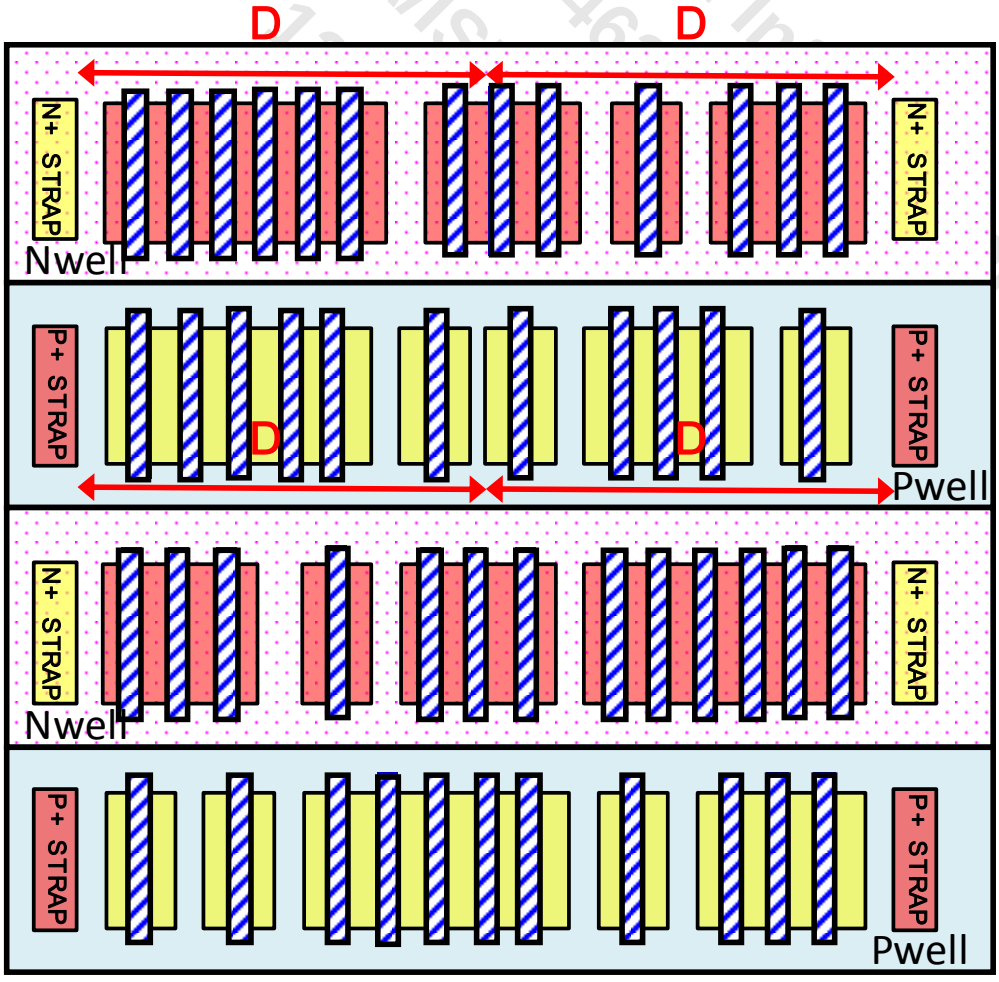

Figure 10.1.15

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10.1.2.5 Layout Rules and Guidelines for Area I/O Latch-up Prevention

To increase the number or density of I/Os in VLSI designs, the area-I/O is adopted to achieve a smaller package size (such as flip-chip), shorter wire length, better signal and power integrity. However, an external injection of minority carriers from an Area IO cell can trigger a latchup event easily in the parasitic pnpn path of the surrounding CMOS circuits in the chip's core area. The Area I/O cell is different from the peripheral type I/O ring, it does not have pre-driver structure between the post driver (carrier injector) and the core CMOS circuits, which can help absorb the substrate currents or carriers from an external injection. Fig 10.1.16 shows the schematic diagram of the Area I/O structure.

"LUPWDMY_2 (255;18)" is a DRC dummy layer to trigger the area I/O latch-up rules check. (Fig 10.1.17)

Table 10.1.2 Layout Rules and Guidelines for Area I/O Latch-up Prevention

Rule No.	Description	Label	Op.	Rule
LUP.10.g	For Area I/O, within 75 µm (≤ 75um, label "A" in Fig. 10.1.16) sizing of the OD injector (covered by LUPWDMY_2), specific guard rings/guard bands rules and N/P wells STRAP rules (LUP.11~LUP.14) should be followed to enhance latch up immunity. (Fig 10.1.16) Exclusive conditions: If the spacing between the N+ OD and P+ OD of the core CMOS circuits ≥ 3 µm (Label "F" in Fig 10.1.16).			
LUP.11.g[U]	For Area I/O, the minimum total width of the P+ guard band (Fig 10.1.16)	B	≥	2
LUP.12.g[U]	For Area I/O, the minimum total width of the N+ guard band (Fig 10.1.16)	C	≥	2
LUP.13.g	For Area I/O, 1. Any point inside NMOS source/drain {(N+ ACTIVE INTERACT PO) NOT PO} space to the nearest PW STRAP in the same PW. (Figure 10.1.18) 2. Any point inside PMOS source/drain {(P+ ACTIVE INTERACT PO) NOT PO} space to the nearest NW STRAP in the same NW. (Figure 10.1.18) 3. The height of pick-up OD is recommended to be equal to that of source/drain ODs.	D	≤	15
LUP.14.g	For Area I/O, must be surrounded two guard-ring for the OD injector. And all of the guard-ring widths must be ≥ 0.2um. N+OD injector must be surrounded by P+ guard-ring (P+ pick-up ring) P+OD injector must be surrounded by N+ guard-ring (N+ pick-up ring) The PW of N+OD injector must be surrounded by N+ guard-ring The NW of P+OD injector must be surrounded by P+ guard-ring	E	≥	0.2

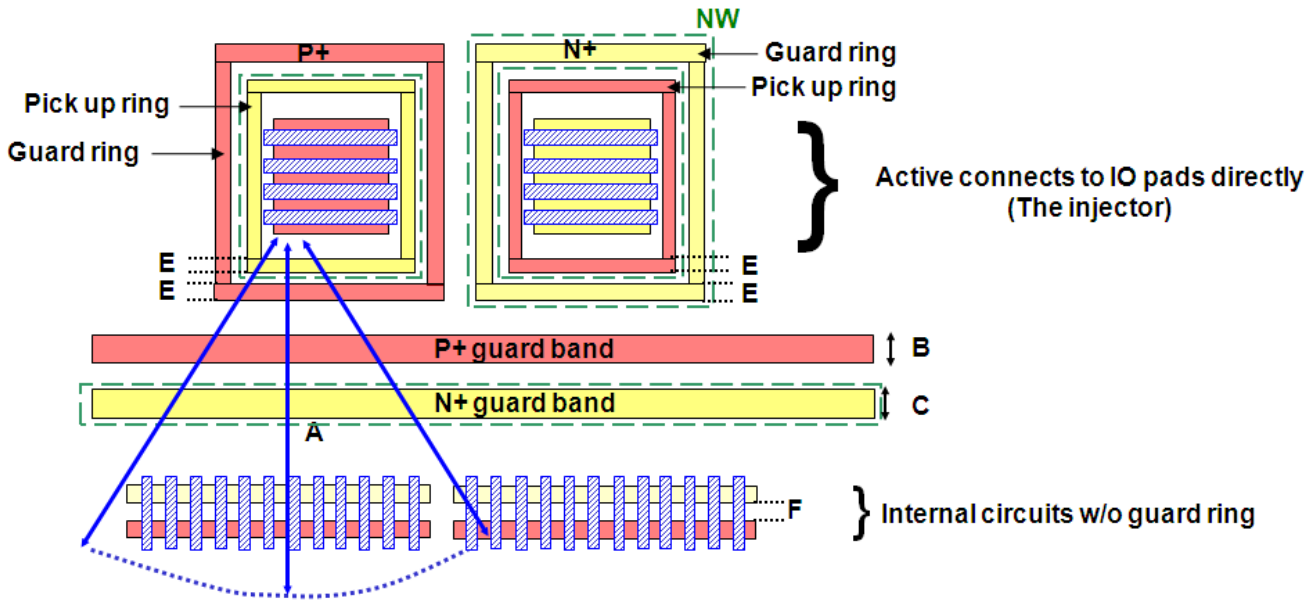

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Figure 10.1.16 Area I/O latchup prevention

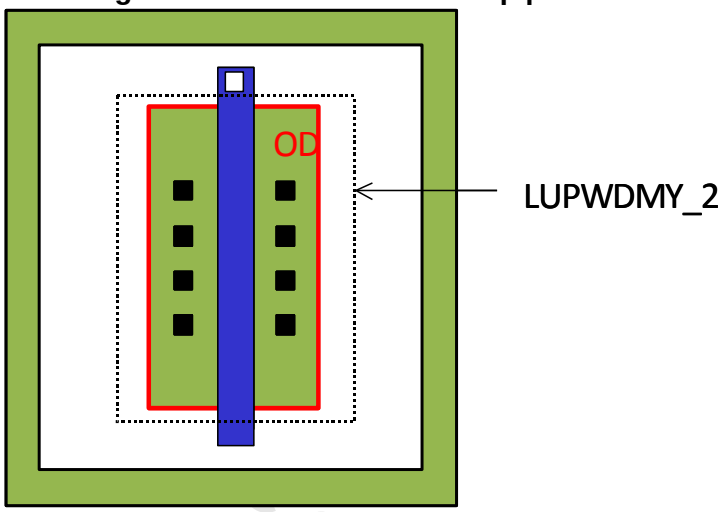

Figure 10.1.17 Example of LUPWDMY_2 Usage

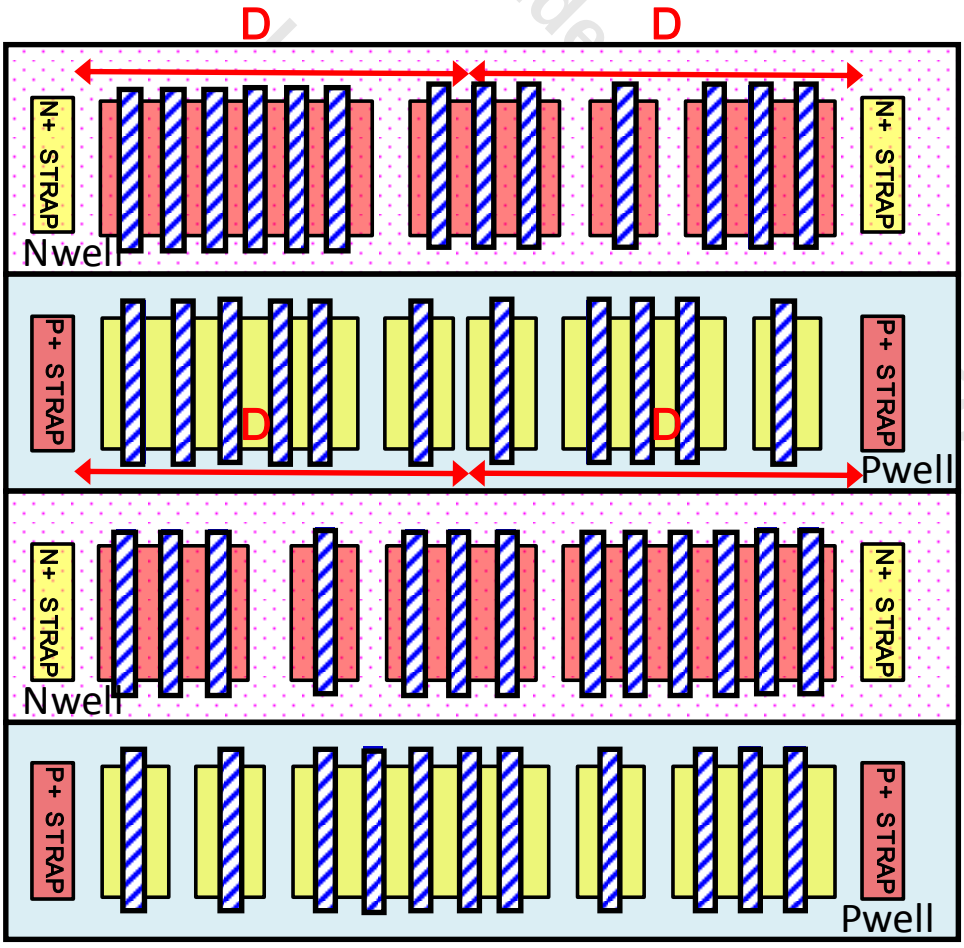

Figure 10.1.18

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10.1.3 Test Specification and Requirements

TSMC Latch-Up testing is performed at room temperature and 125°C by complying the Latch-up test methodology defined by JEDEC78. The test items include Input/Output over-voltage/ over-current test (Fig. 10.1.1.3.1) and supply over-voltage test (Fig. 10.1..3.2). It applies a stepped voltage/current to one pin per device with all other pins open except Vdd and Vss. Testing was started from Vdd/50mA (positive) or 0V/-50mA (negative), and the DUT was biased for 0.5 seconds. If the Icc current does not reach the predefined limit (Idd=200mA), then the voltage was increased by +/-0.1V or +/-50mA and the pin was tested again until +/-1.5Vdd or +/-100mA for Input/Output over-voltage/ over-current.

Notes:
1. DUT: Device under test.

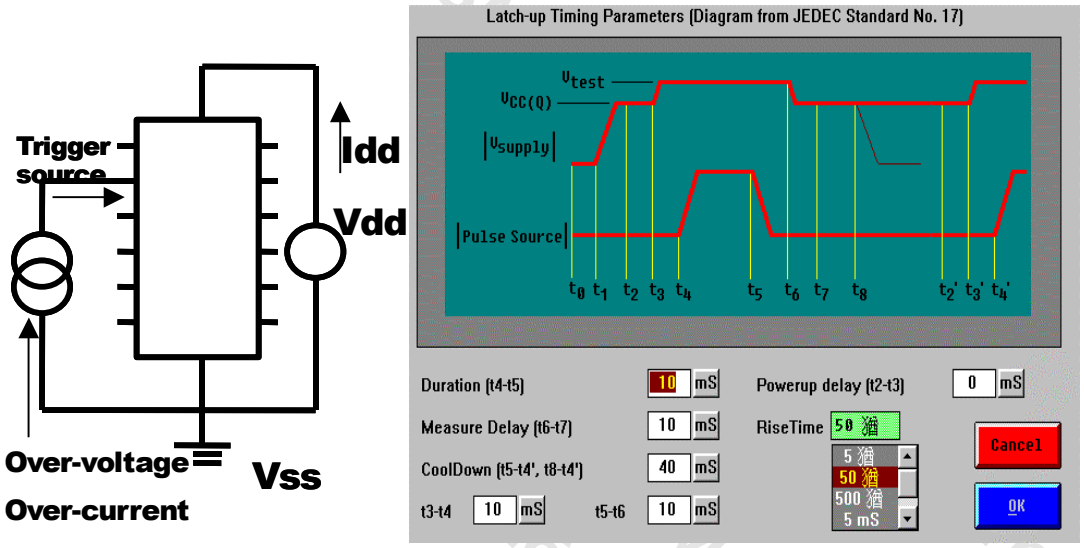

Fig. 10.1.3.1 Input/Output Over-Voltage/Current Test

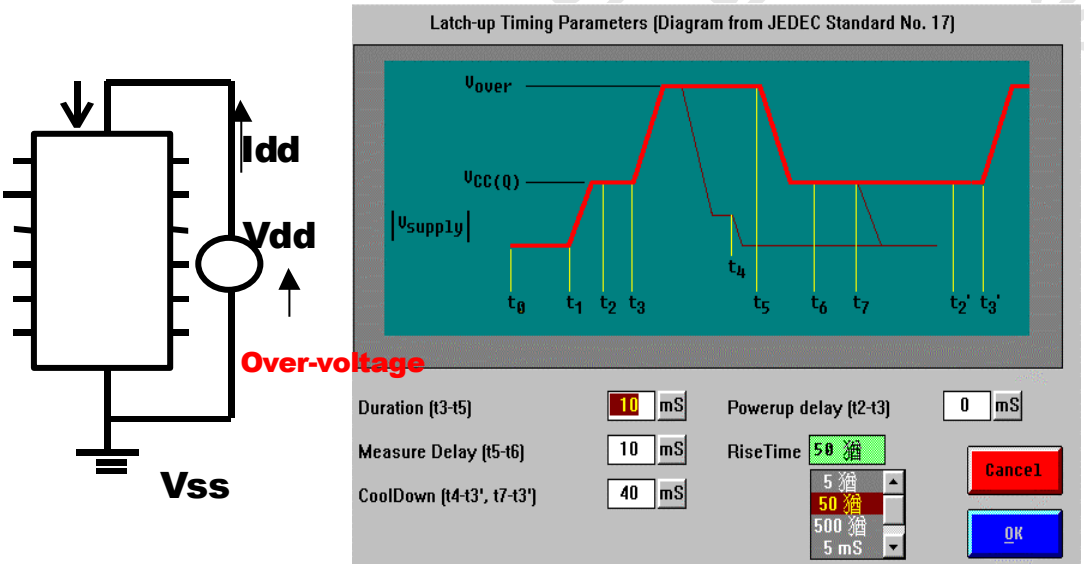

Fig. 10.1.3.1 Supply Over-voltage Test

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10.2 I/O ESD Protection Circuit Design and Layout Guidelines

10.2.1 ESD introduction

During manufacturing, it is inevitable the IC will suffer various kinds of Electrostatic-Discharge (ESD) damage. Different environments, wafer during CMOS process, package, testing and human handling, will generate different kinds of ESD's. Currently, the charge device model (CDM), Human-Body mode (HBM) and Machine model (MM) are the most common models used to simulate the ESD events generated from various environments. The main difference between CDM and HBM is that CDM charges come from the substrate through the internal circuit to the pad, while the ESD's for HBM and MM come from the external environment to the pad. So, most ESD protection devices only can be used to protect HBM and MM, but cannot be used to protect the CDM since the ESD protection device is at the pad and there is no direct current path between the internal circuit and the ESD protection device.

The discharging behaviors for the three ESD models all can be simplified by the equivalent circuit in Figure 10.2.1 and expressed by the equation :

$$I_{ESD} = V_{ESD} \frac{e^{(-\alpha+\beta)t} - e^{-(\alpha+\beta)t}}{2\beta L_o} \quad \textbf{(1)}.$$ where $\alpha = R_o/(2L_o)$, $\beta = \sqrt{(R_o C_o)^2 - 4L_o C_o}\,/(2L_o C_o)$

For HBM, the R_O , C_O and L_O is 1.5KΩ, 100pF and 7.4μH, respectively. For MM, the R_O , C_O and L_O is 10Ω, 200pF and 7.4μH, respectively. Substituting the above values into eq. (1), the measured and theoretical current waveforms for HBM and MM are shown in Figure 10.2.2. For HBM, the rise time is <10nsec, the decay time is 150nsec (R_OC_O=1.5KΩ×100pF) and the peak current is equal to V_{ESD}/R_O. The period for MM is nearly 90nsec and the peak current for 100V MM is nearly 1.7A.

Figure 10.2.3 shows the CDM discharging current waveforms vs. L_O and R_O based on eq. (1) for 500V CDM. The CDM period and peak current are varied with L_O, C_O, and R_O. Compared with HBM and MM, the CDM has a shorter period and a larger peak current.

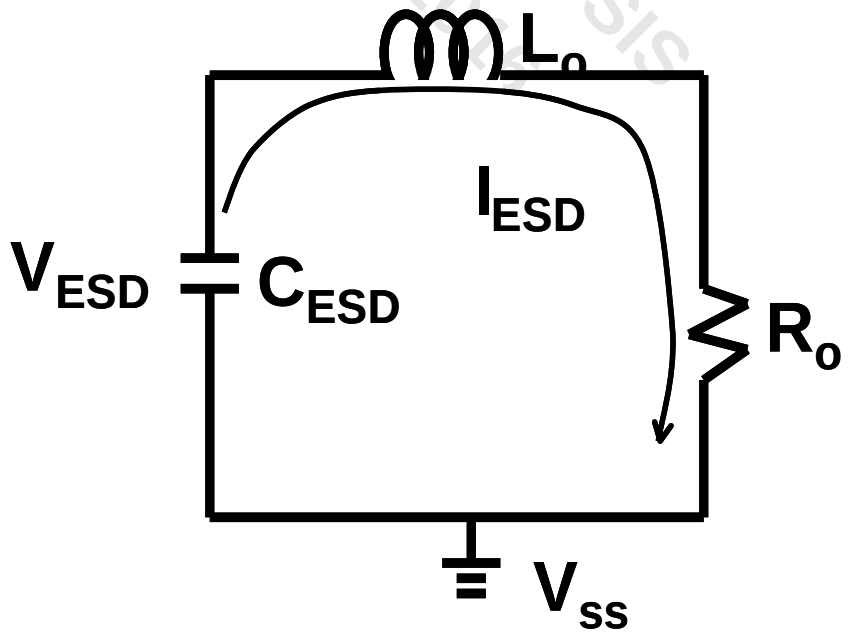

Fig. 10.2.1 The simplfied equivalent circuit for ESD

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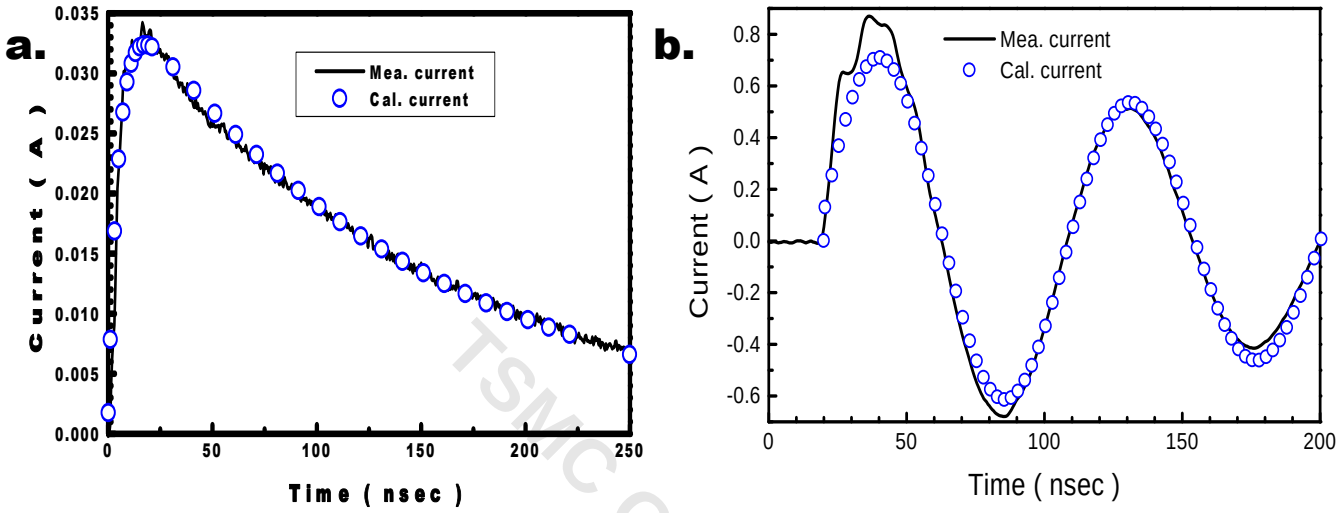

Fig. 10.2.2 The discharging current waveform for (a) HBM and (b) MM

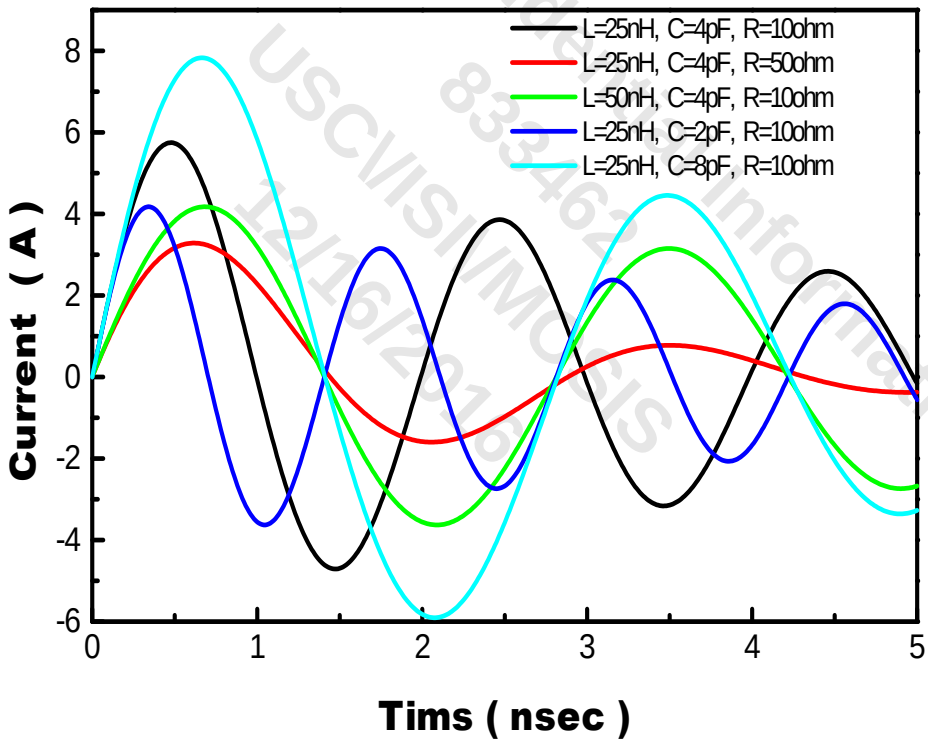

Fig. 10.2.3 The CDM discharging current waveforms vs. Lo, Ro, and Co

Besides the above three models, another kind of ESD, which occurrs during wire bonding, has been found. We call it ball-bonding ESD (BBE). The stress period of the BBE (~20nsec) is shorter than HBM and MM, but longer than CDM. The stress voltage (~13V) of BBE is much smaller than HBM, MM and CDM. The BBE came from the charged wire through the pad and device which connect the pad to the substrate. It might induce the reliability issue and degrade the device ESD performance if the ESD protection device is not robust enough or the pad is without the ESD protection device. (please refer to JH Lee et. al, “The impact of ball-bonding induced voltage transient on sub-90nm CMOS technology,” in IRPS, p. 97, 2007.)

Because the pad is the median used to interact with externals for an IC, all pads need ESD protection devices to protect the ESD coming from various environments to prevent internal circuit damage.

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10.2.2 TSMC IO ESD layout style introduction

TSMC IO ESD protection scheme is the self-protection scheme that IO is the ESD protection device. No matter NMOS or PMOS, they all have the snapback phenomena. The snapback mechanism can be described as the following: As the applied voltage is higher than the device trigger voltage (Vt1 in Fig. 10.2.4), a lot of holes are generated due to a drain junction occurrence Avalanche-breakdown. The hole current (Isub in Fig. 10.2.4) flows through the substrate (Rsub in Fig. 10.2.4) and raises up the substrate potential (Vsub in Fig. 10.2.4), and eventually forward bias the p-n junction (D1 in Fig. 10.2.4) between the P-substrate and the source when the potential becomes higher than 0.7V. Subsequently, a lot of electrons are injected from the source and flow to the p-n junction between the P-substrate and the drain, which generates more electron-hole pairs due to impact-ionizations at the high electrical field of the drain junction. The resulting carrier transport mechanism causes a positive feedback effect to turn on the parasitic n-p-n bipolar transistor (npn in Fig. 10.2.4). As the parasitic n-p-n is turned on, it can sink a much higher current level than the initial Avalanche-breakdown current and goes into a stable snapback region as shown in Fig. 10.2.4.

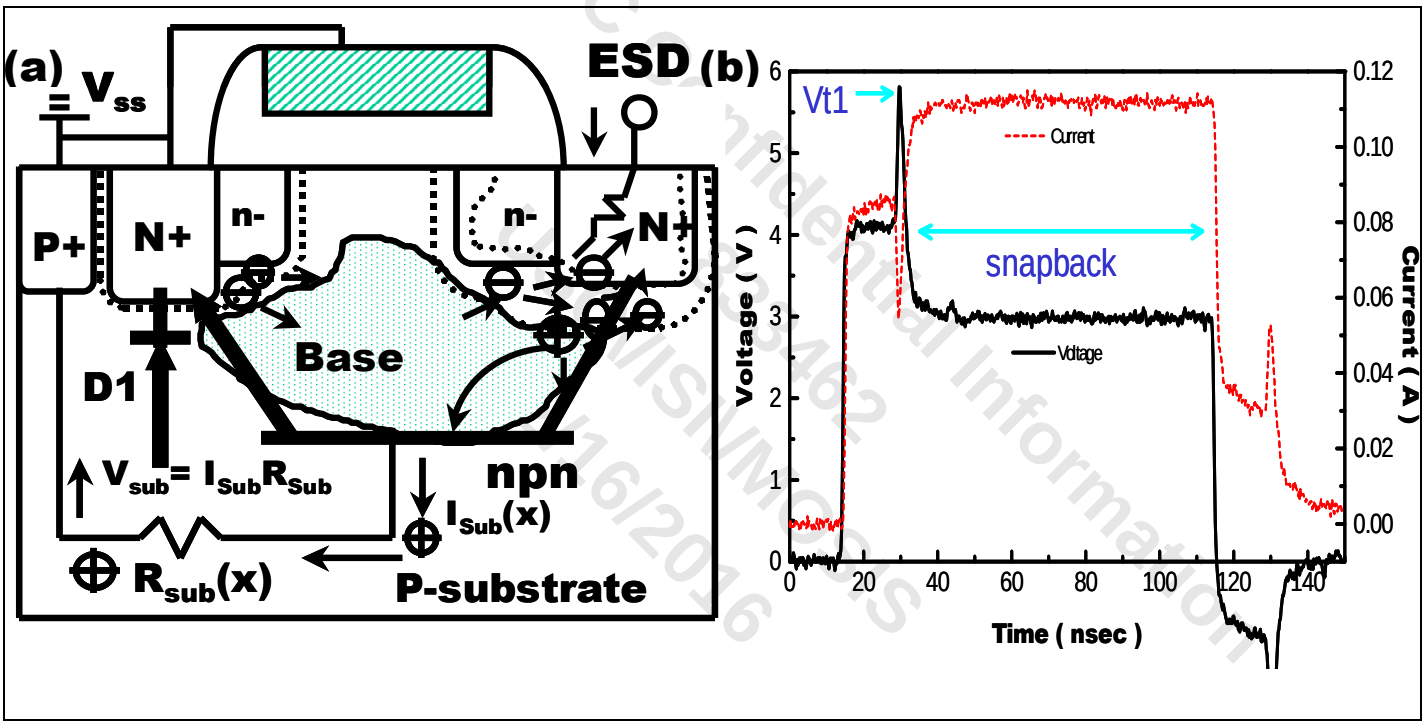

Fig. 10.2.4 (a) the parasitic components of a Grounded-gate NMOS (GGNMOS), (b). real time IV characteristics of a GGNMOS uder 100 nsec TLP pulse

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The RPO is the silicide blocking layer which is commonly used for an ESD protection device to forbid the silicide formation on the drain region. The RPO scheme might be not a good solution for IO design due to larger series resistance, but it can provide a stable ESD performance for an ESD protection device. So, the device ESD performance does not vary between technology generations or manufacturing fabs. Fig. 10.2.5 shows the high current IV characteristics of a RPO N+ OD resistor. The RPO N+ OD resistor has a saturation region. In the saturation region, the resistor becomes a high impedance resistor, so the increase in the applied voltage does not increase the stress current. From this characteristic, we can deduce that RPO can be used to clamp the current to prevent the current being localized in a given region. As a region enters the saturation point, it becomes a high impedance resistor. Then, the current of this region cannot be increased anymore. Subsequently, the current will be pushed to flow to other non-saturaed regions and the current can distribute along the junction uniformly.

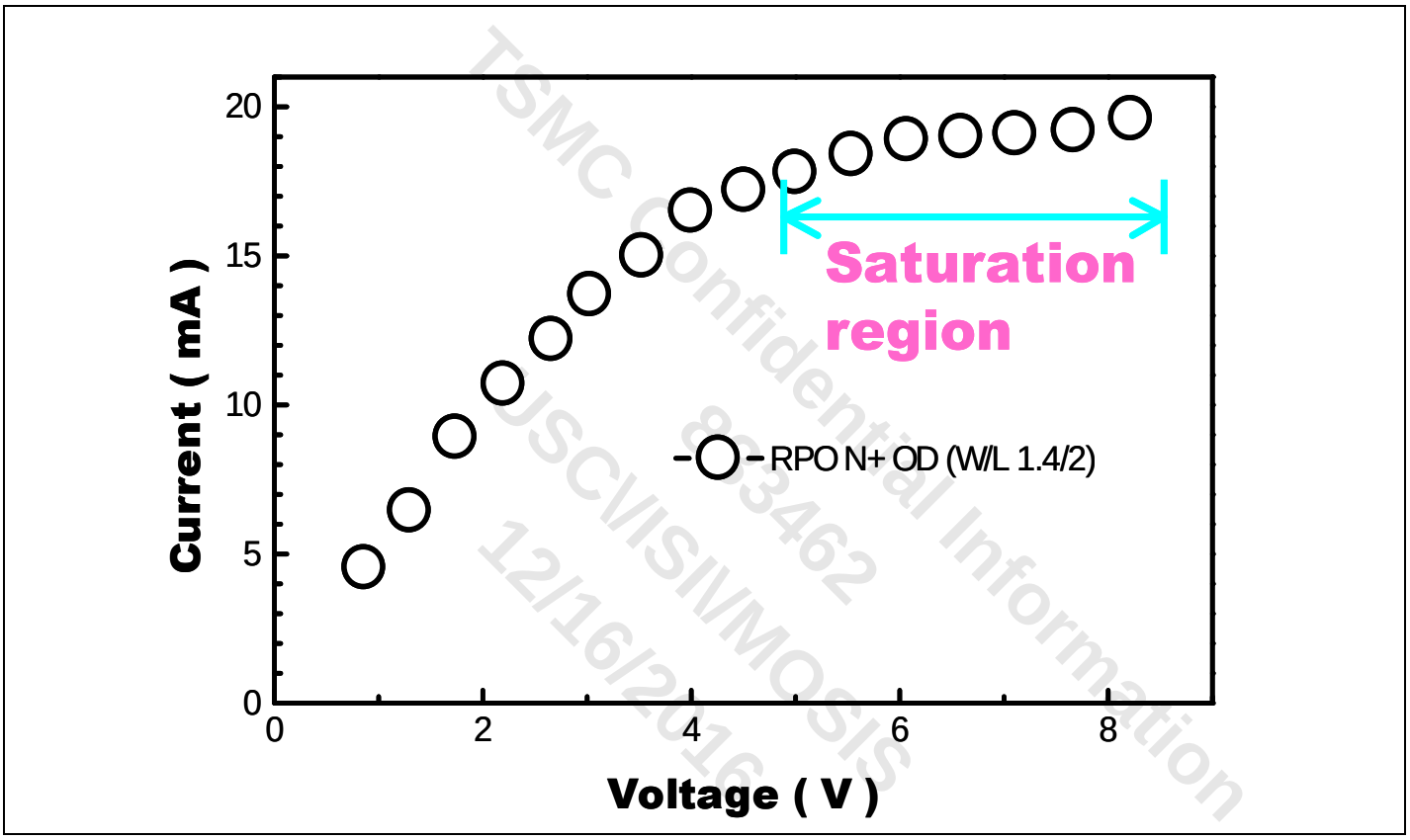

Fig. 10.2.5 High current IV charctertistics of a RPO N+ OD resistor

The ESD implant is a process scheme to enhance the device ESD performance without changing the device layout since it only covers the drain region and needs to have 0.4um space from the poly gate. The current ESD implant recipe is P-type ESD implant. It can reduce the device breakdown voltage and create the higher electrical field during the snapback region, resulting in better ESD performance. At TSMC, only one dosage exits for P-type ESD implants. The dosage for ESD implants is higher than the channel implant dosage for 3.3V and 2.5V devices, but lower than the channel implant dosage for 1.8V and 1.0V devices. So, the ESD implant is useful for 3.3V device, but is useless for 2.5V devices and of no use for devices below 1.8V.

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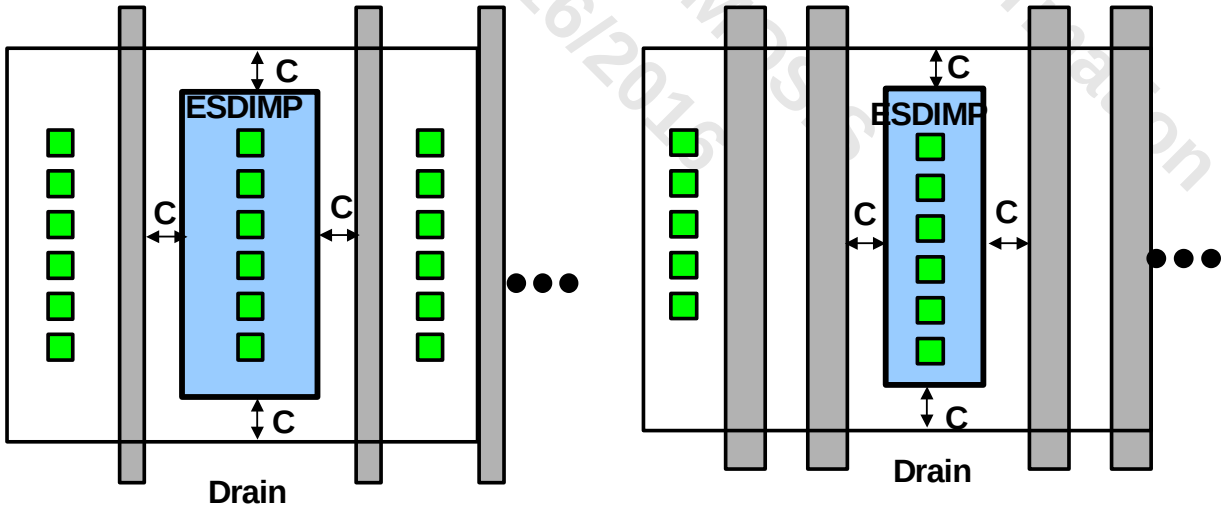
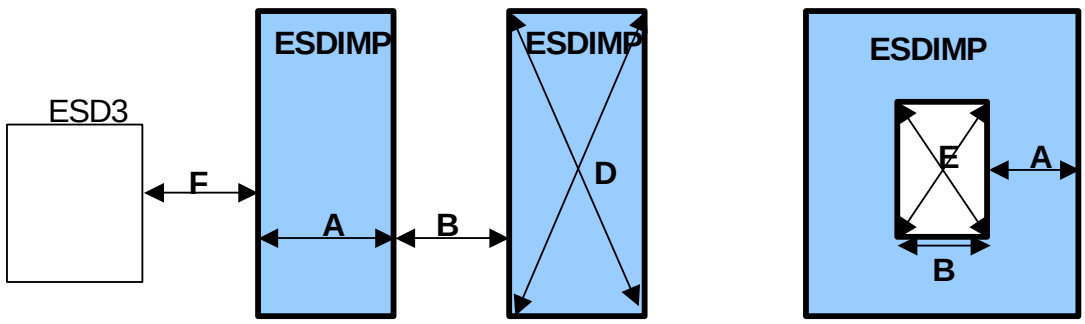
10.2.3 ESD Implant (ESDIMP) Layout Rules (MASK ID: 111)

ESDIMP (CAD layer: 189;0) is a drawn layer for ESD implant. ESDIMP (a drawn layer) and ESD3 (logical operation) can coexist.

The following width, space, area, and enclosed area are based on process concern. Please use larger dimension for ESD implant.

Rule No.	Description	Label		Rule
ESDIMP.W.1	Width	A	≥	0.6
ESDIMP.S.1	Space	B	≥	0.6
ESDIMP.S.2	Space to ESD3 (Overlap is prohibited)	F	≥	0.6
ESDIMP.EN.1	(OD NOT PO) enclosure of ESDIMP. ESDIMP must be fully inside (OD NOT PO).	C	≥	0.4
ESDIMP.EN.1®	Recommended (OD NOT PO) enclosure of ESDIMP.	C	=	0.4
ESDIMP.A.1	Area	D	≥	1.0
ESDIMP.A.2	Enclosed area	E	≥	1.0
ESDIMP.R.1	ESDIMP must be fully inside N+ ACTIVE			
ESDIMP.R.2®[U]	Recommended ESDIMP in the following NMOS drain side, 1) 5V tolerant I/O circuits using a 3.3V I/O device. A 5V tolerant I/O is defined by the V_{IN} criterion: $V_{IN} > V_{DD}$ but $V_{IN} \leq$ (5V +10%) 2) 3.3V tolerant I/O circuits using a 2.5V I/O device. A 3.3V tolerant I/O is defined by the V_{IN} criterion: $V_{IN} > V_{DD}$ but $V_{IN} \leq$ (3.3V +10%) 3) 2.5V tolerant I/O circuits using a 1.8V I/O device. A 2.5V tolerant I/O is defined by the V_{IN} criterion: $V_{IN} > V_{DD}$ but $V_{IN} \leq$ (2.5V +10%)			





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10.2.4 ESD Dummy Layers Summary

10.2.4.1 SDI Dummy Layer

- SDI (CAD layer: 122) is a DRC layer but not for mask making. It is required to cover all the OD regions of the ESD related circuits (Regular IO, high voltage tolerant I/O, Power Clamp), including MOS and diode, that are connected to the pads. SDI is not necessary to cover the Well STRAP or ESD guard-ring.

10.2.4.2 ESD3 Dummy Layer Description

- ESD3 (CAD layer: 147) a tape-out layer. It is required for cascode NMOS in high voltage tolerant I/O (N2 and N3 shown in Figure 10.2.15). ESD3 includes the source, gate, and drain, but does not necessarily cover the Well STRAP or the ESD guard-ring. So, ESD3 should enclosure of ACTIVE.

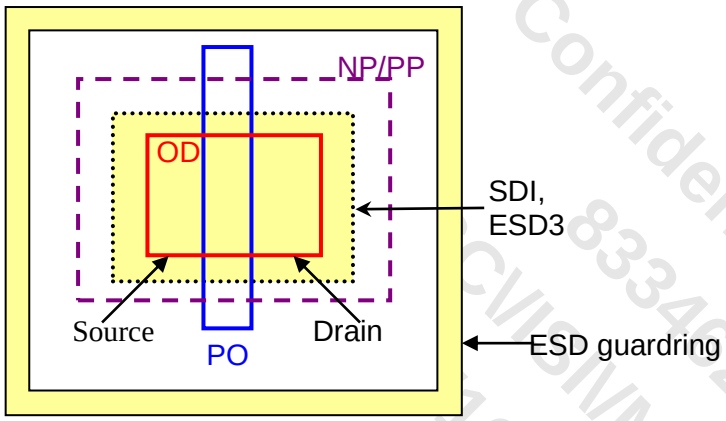

Figure 10.2.6 The SDI, ESD3 dummy layer layout

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10.2.5 ESD circuits Definition

10.2.5.1 Regular IO

Regular I/O is composed of the NMOS and PMOS and the drains of the NMOS and PMOS connect to the pad directly (N1/P1 in Figure 10.2.10).

10.2.5.2 HV tolerant IO

The HV tolerant I/O is composed of the PMOS in floating NW (P2 Figure 10.2.15) and cascode NMOS and the drains of the floating NW PMOS and cascode NMOS connect to the pad directly (P2/N2/N3 in Figure 10.2.15). There are three kinds of HV tolerant IO listed below.

10.2.5.2.1 5V tolerant I/O

5V tolerant I/O circuits using a 3.3V I/O device with V_{IN} criterion: $V_{IN} > 3.3V$ but $V_{IN} \leq (5V +10\%)$.

10.2.5.2.2 3.3V tolerant I/O

3.3V tolerant I/O circuits using a 2.5V I/O device with V_{IN} criterion: $V_{IN} > 2.5V$ but $V_{IN} \leq (3.3V +10\%)$.

10.2.5.2.3 2.5V tolerant I/O

2.5V tolerant I/O circuits using a 1.8V I/O device with V_{IN} criterion: $V_{IN} > 1.8V$ but $V_{IN} \leq (2.5V +10\%)$.

10.2.5.3 IO Buffer

The I/O Buffer includes regular I/O and HV tolerant I/O.

10.2.5.4 Power Clamp Device (Ncs)

The device is used for V_{DD} Pad to V_{SS} Pad protection (Ncs in Figure 10.2.10 and Figure 10.2.15). Please refer to section 10.2.6.4.

10.2.5.5 ESD Device

The ESD Device includes any device (NMOS, PMOS, I/O buffer, power clamp device, diodes, SCR and resistor) which connects to the pad directly and can be used to discharge the ESD current.

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10.2.6 Requirements for ESD Implant Masks

- ESD implant is required for HV tolerant(cascode) I/O NMOS unless TSMC approves. You have to draw ESD3 layer for mask making.
- For customers who use their own ESD design structure, or do not use HV tolerant NMOS, ESD implant is optional.

Table 10.2.1 ESD Implant Masks for HV Tolerant I/O Circuits

I/O Design Style	ESD3 (CAD layer 147)/ESD IMP (CAD laer 189;0) Requirement	ESD mask (no.111) Requirement
TSMC-style I/O withHV tolerant IO circuits	Drawing Required	Yes
TSMC-style I/O without HV tolerant I/O circuits	No need	No need
Non TSMC-style ESD	Depends	Depends

10.2.7 DRC methodology for ESD guidelines

10.2.7.1 DRC methodology to identify ESD MOSFET

1. The ESD MOS is defined by MOS covered by SDI (122;0).
2. The Regular ESD N/P MOS is defined in the following:
   - ESD N/P MOS with gate partially covered by RPO & without gate fully covered by RPO
3. The HV Tolerance ESD PMOS is defined in the following:
   - ESD PMOS with gate partially covered by RPO & without gate fully covered by RPO.(same as Regular ESD PMOS)
4. The HV Tolerance ESD NMOS is defined in the following:
   - ESD NMOS with gate partially covered by RPO & with gate fully covered by RPO
5. The Power Clamp ESD NMOS is defined in the following:
   - ESD NMOS without RPO overlap

 # Note: For Other non- TSMC standard ESD MOSFETs, there is no DRC ESD guidelines check.

Table 10.2.7.1.1 how to recognize ESD MOSFET

RPO Partially Cover Gate	RPO Fully Cover Gate	ESD MOS Type
Y	Y	HV Tolerance ESD NMOS
Y	N	Regular ESD N/P MOS or HV Tolerance ESD PMOS
N	Y	No support
N	N	Power Clamp ESD NMOS

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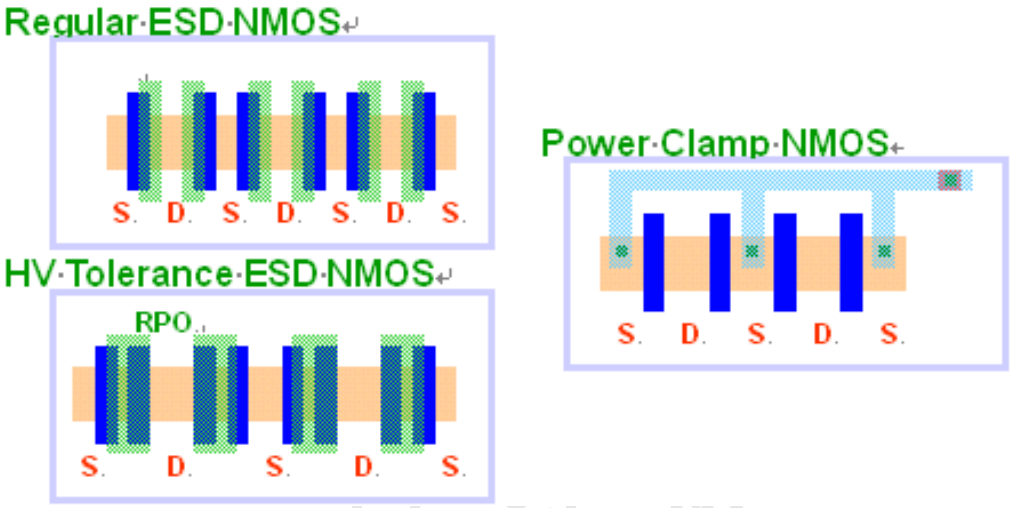
10.2.7.2 DRC methodology to identify ESD MOS Source and Drain

1. The S/D region is defined by {MOS_OD NOT POLY}
2. The S/D region which connected to well pick-up is Source.
   - The connectivity is not broken by resistor for this check.
3. The S/D region OUTSIDE RPO is Source. (except for Power Clamp)
4. Except for recognized Source, all the others are Drain.

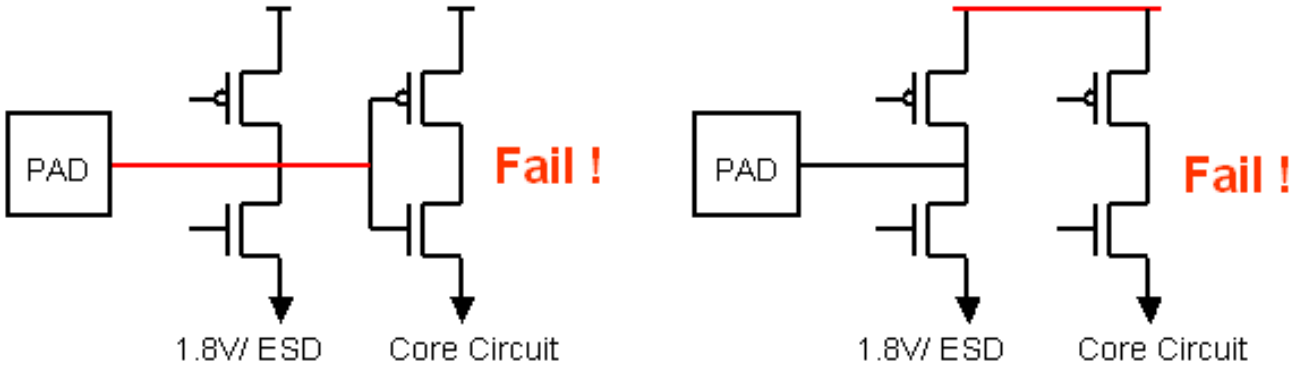
 # Note: If the ESD layout structure is not TSMC-standard, this approach will fail.



Example of S/D for ESD device

10.2.7.3 DRC methodology for ESD.1g

1. ESD S/D is covered by OD18, and connected to Core device S/D/G (without OD18).
2. If ESD S/D is connected to P-well pick-up, it is excluded from this rule check.
3. The connectivity is not broken by resistor for this check.



Example of ESD.1g

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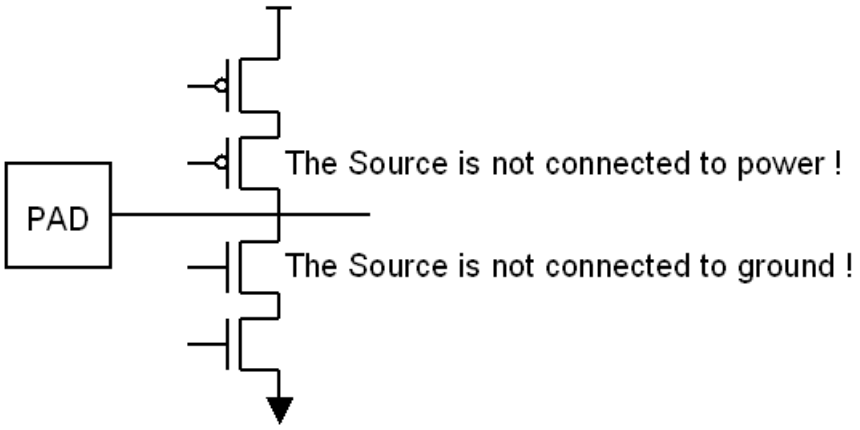
10.2.7.4 DRC methodology for ESD.4g

1. ESD S/D interact one gate only is defined as edge side OD.
2. The edge side OD is not connected relative well pick-up.
   - N-well pick-up works for NMOS, P-well pick-up works for PMOS.
   - The connectivity is not broken by resistor for this check.

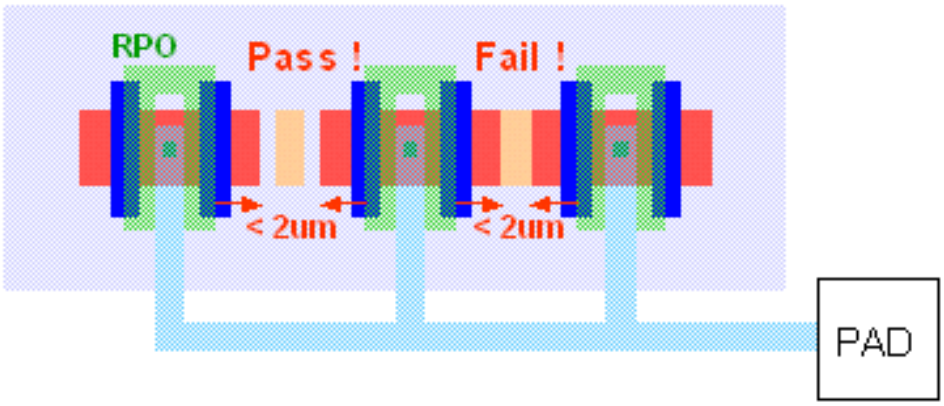
 # Note: This check will fail for stacked ESD circuit.



Example of ESD.4g

10.2.7.5 DRC methodology for ESD.6g

1. Check the space between two ESD MOS in same connection of Drain to PAD.
   - The connectivity is not broken by resistor for this check.
2. The space < 2μm, and there is a well pick-up between these two ESD MOSs



Example of ESD.6g

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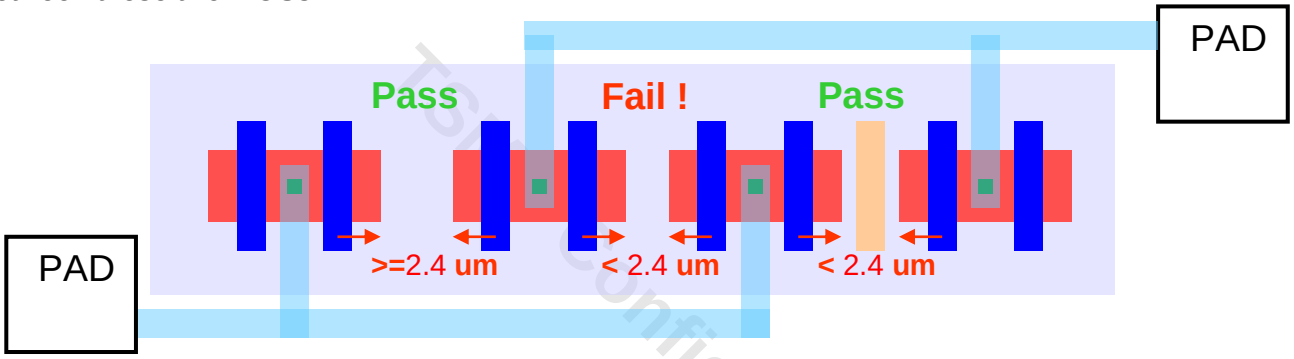
10.2.7.6 DRC methodology for ESD.7g

1. Check the space < 2.4μm between two same type Non-ESD MOSs connected to different PAD. (Non-ESD MOS: MOS not covered by SDI).
   - The connectivity depends on “DISCONNECT_AFTER_RESISTOR” is turned ON or OFF.
2. Check the space < 2.4μm between two same type Non-ESD MOSs in the same well, or these two wells are connected.
   - The connectivity is not broken by resistor for this check.
3. Find out the MOSs meet above two criteria at the same time, and there is no different type of OD placed between these two MOSs.



Example of ESD.7g

10.2.7.7 DRC methodology for finger width

1. This check is for ESD.16g, ESD.17g, ESD.24g, ESD.25g, ESD.36g, ESD.37g, ESD.44g, ESD.45g, ESD.53g, ESD.58, and ESD.59.
2. The total finger width is calculated by the ESD MOS (ESD.16g, ESD17g, ESD.24g, ESD.25g, ESD.36g, ,ESD.37g ESD.44g, ESD.45g, and ESD.53g) in same Drain connection.
3. The total width is calculated by the ESD Field Device (ESD.58g, ESD.59g) in same collector connection. The connectivity is not broken by resistor for this check.

Example of finger width

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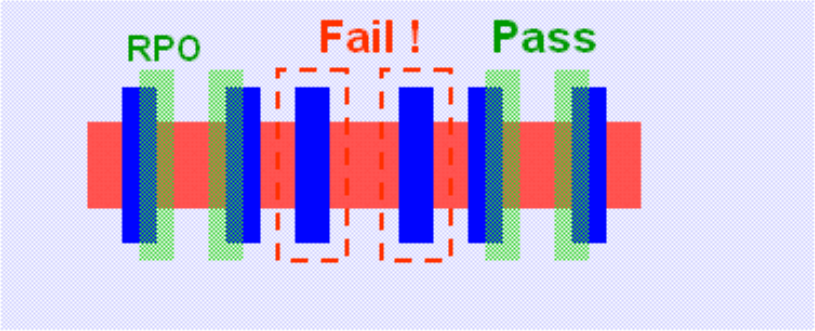
10.2.7.8 DRC methodology for ESD.19g and ESD.27g

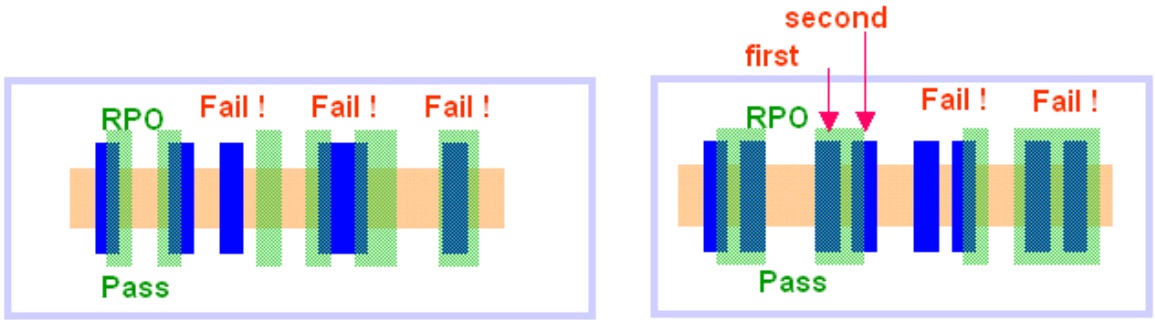
1. As mentioned in previous, the drain-side is recognized by S/D not OUTSIDE RPO, so that the check of drain-side OD without RPO would be meaningless.
2. DRC only highlight the gate without overlap with RPO.



Example of ESD.19g and ESD.27g

10.2.7.9 DRC methodology for ESD.20g, ESD.28g, ESD.29g, and ESD.40g

1. For Regular ESD N/P MOS & HV Tolerance ESD PMOS :
   - The overlap of RPO and Gate should exactly equal to 0.06μm.
   - The overlap should occur in one-side only
   - Without overlap is not allowed
2. For HV Tolerance ESD NMOS :
   - The RPO should fully cover the first Gate.
   - The overlap of RPO and second Gate should exactly equal to 0.06μm.
   - The overlap should occur in one-side only.
   - Without overlap is not allowed.



Example of ESD.20g, ESD.28g, ESD.29g and ESD40g

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10.2.8 ESD Guidelines

- TSMC's ESD spec is 2KV for Human Body Model (HBM) and 200V for Machine Model (MM)
- These design guidelines are designed to increase ESD protection levels to TSMC specifications.
- These guidelines are developed from our test chip silicon data. The test structures in these test chips include most of the failure cases we have studied. Yet, there might be other weak paths that are not captured by these guidelines. Thus, chip level ESD testing should be carried out.

10.2.8.1 General Guideline for ESD Protection

No.	Description	Label		Dimension
ESD.WARN.1	SDI is not in whole chip. If SDI does not exist, the ESD related DRC will not work well.			
ESD.WARN.2	SDI enclosure of ACTIVE		≥	0
ESD.1g	Use thin oxide transistor for thin oxide power clamp and thin oxide I/O buffers; use thick oxide transistor for the thick oxide Power Clamp and thick oxide I/O buffers (Figure 10.2.7). DRC will flag the following one condition: (1) ((MOS INTERACT OD2) INTERACT SDI) connected to (MOS NOT INTERACT OD2) DRC will exclude Drain/Source/Gate connected to PW STRAP. (For more ESD design Tips, please see the "Tips for ESD/LU design" section in this chapter.)			
ESD.2g^{U}	NMOS and PMOS for I/O buffer and Power Clamp follow finger type structure with unique finger dimension and layout style.			
ESD.3g	Unit finger width of NMOS and PMOS for I/O buffer and Power Clamp Device (Figure 10.2.8)	G	=	15-60
ESD.4g	The OD area of the edge side of I/O buffer and Power Clamp should be Source or Bulk rather than Drain (Figure 10.2.8), to avoid an unwanted parasitic bipolar effect or an abnormal discharge path in ESD zapping. DRC will flag (((OD INTERACT SDI) NOT PO) INTERACT one Gate) does not connect to STRAP.			
ESD.5g	Same type OD of the I/O buffer and Power Clamp should be surrounded by a guard-ring. All other type ODs should be placed outside this guard-ring. (Figure 10.2.8) DRC will flag the following two conditions, (1) Different type ODs in the most inner guard-ring. (2) OD not inside the most inner guard-ring			
ESD.6g	Butted STRAP and the STRAP which are between two sources of the N/PMOS in the same I/O buffer and Power Clamp are strictly prohibited. (Figure 10.2.9) DRC will flag Butted STRAP and the STRAP which is within 2um space of two sources of (MOS INTERACT SDI) connected to same pad.			
ESD.7g	Except the ESD device, either one of the following two conditions must be followed.			
	1) the space of two same type ODs		≥	2.4
	2) two same type ODs should be separated by different types of OD.			
	The same type ODs are N+OD and N+OD in the same PW, or P+OD and P+OD in the same NW, which connect to two different pads			
ESD.8g^{U}	Value of resistor R in Figure 10.2.10		≥	200 Ω

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No.	Description	Label		Dimension
ESD.9g[U]	N/PMOS (N4/P4) of ESD secondary protection in Figure 10.2.10 1) Channel width 2) Should be added after the resistor R (on the far side of R from the pad). 3) NOT in SDI 4) ESD implant and RPO are not needed in these secondary protection devices.		≥	20
ESD.10g[U]	Total width of metal lines connecting the bond pad and the ESD devices. (Figure 10.2.8)	I	≥	15
ESD.11g[U]	Via number for each layer in the ESD discharge current path.		≥	200
ESD.12g	It is not allowed to use OD RPO resistors or NW resistors connected to I/O PAD (Figure 10.2.10 and Figure 10.2.11). DRC will use (((RPDMY OR RH) AND OD) AND RPO) to recognize OD RPO resistor. DRC will use (NWDMY INTERACT NW) to recognize NW resistor.			
ESD.13g[U]	Total metal width for Power and Ground bus line (Figure 10.2.12)		≥	20
ESD.14g[U]	Resistance of the bus line from the V_{DD} or V_{SS} pad to any I/O pad (Figure 10.2.12)		≤	1Ω
ESD.15g[U]	Bypass discharge cells should be inserted between each separate V_{DD} and V_{SS} to avoid ESD damage to internal circuits. This preventative measure is of special importance to the isolated powers used only by a small circuit (< 5K gates). The connections are illustrated in Figure 10.2.13. (For more details, please see the "Tips for the Power Bus" section in this chapter.)			

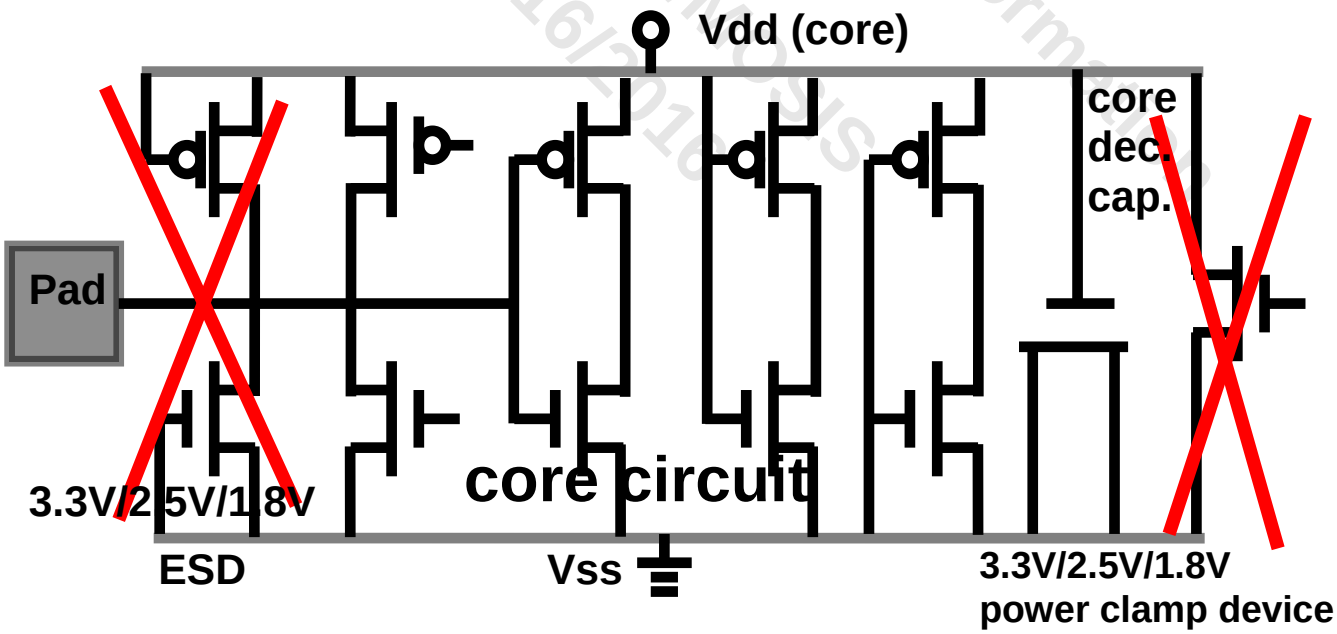

Figure 10.2.7 Use thin oxide transistor for the ESD protection of thin oxide circuits

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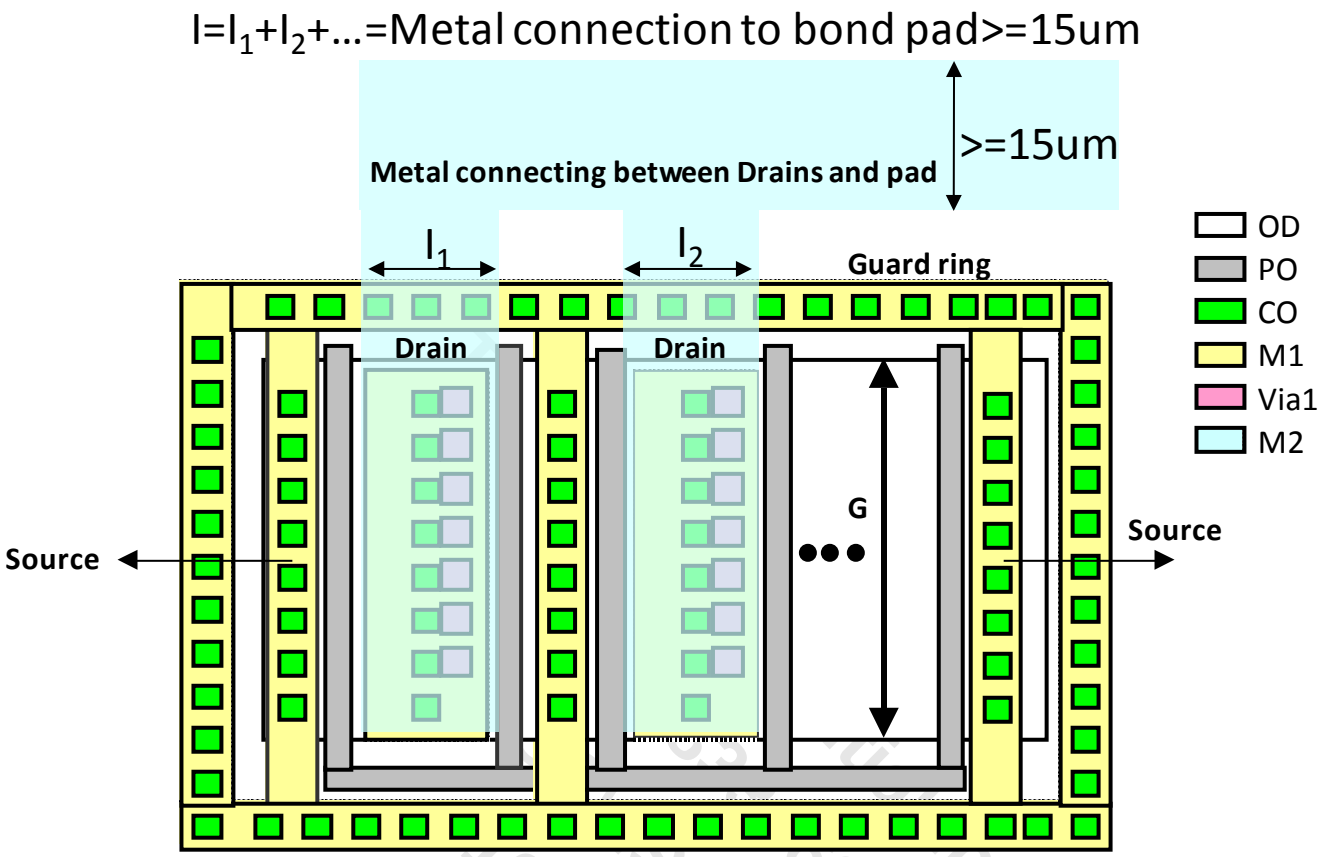

Figure 10.2.8 NMOS and PMOS Layouts for I/O Buffer

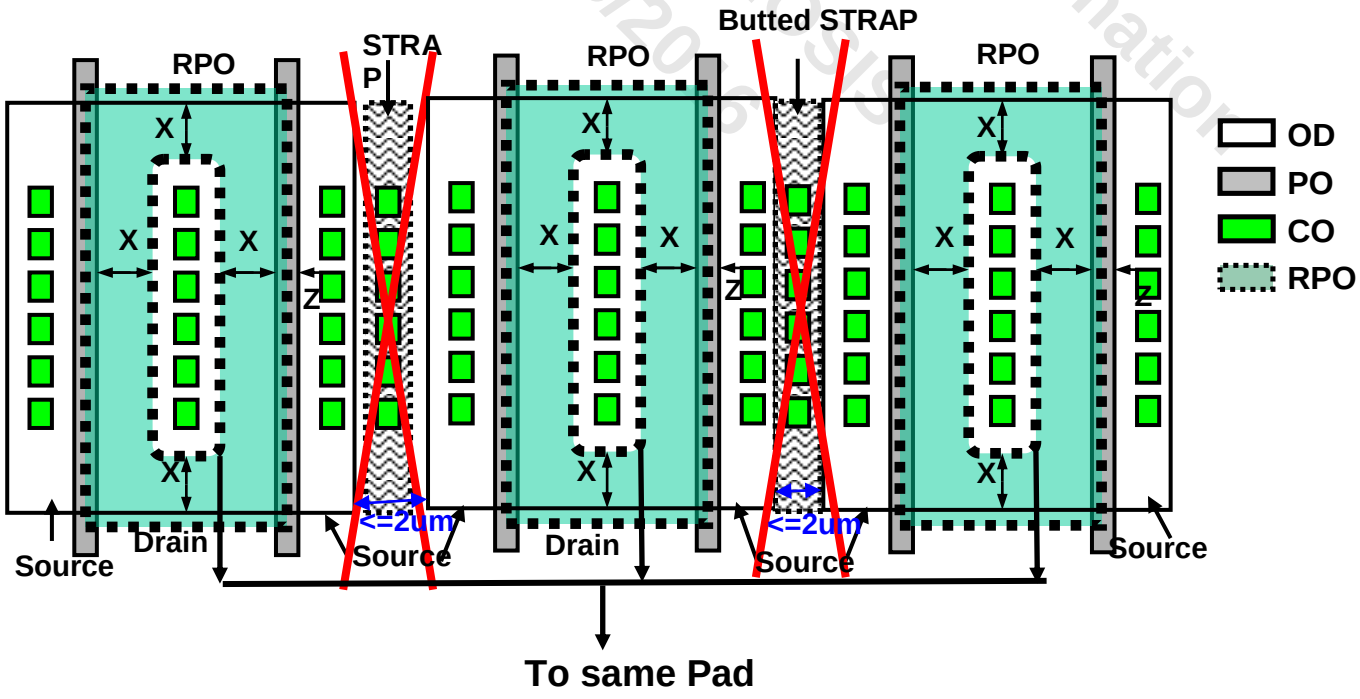

Figure 10.2.9 Butting or Inserted STRAP between two sources of I/O buffer is prohibited

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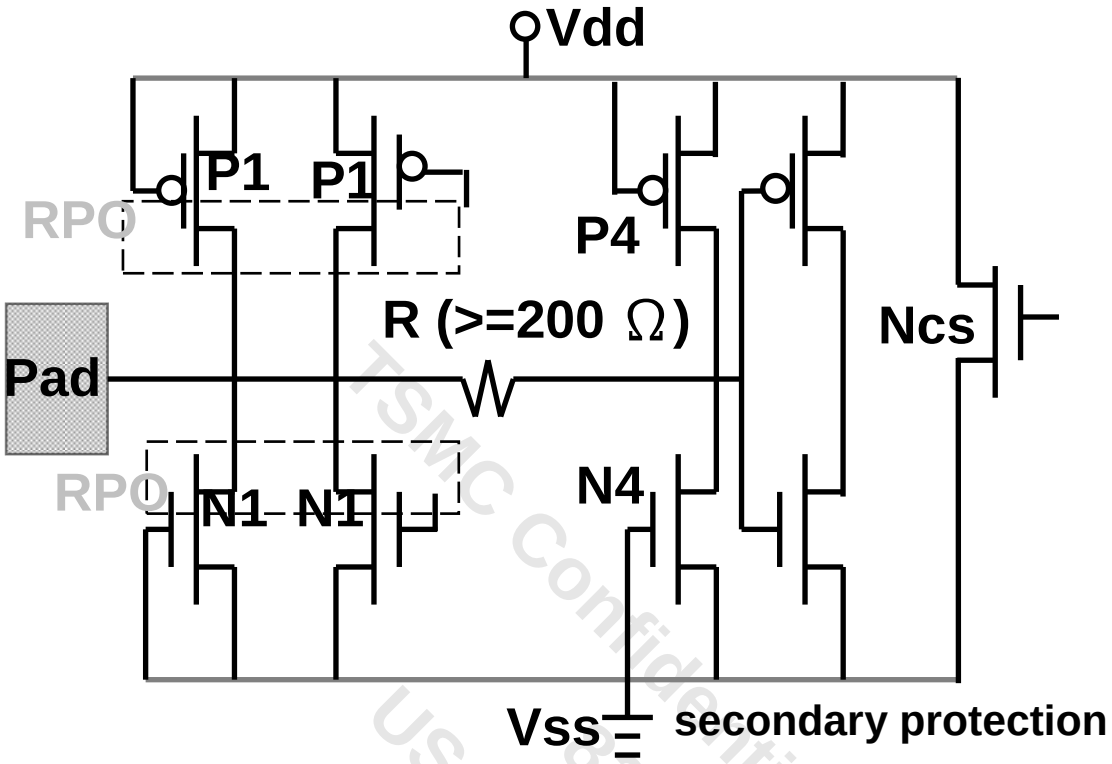

Figure 10.2.10 Regular I/O

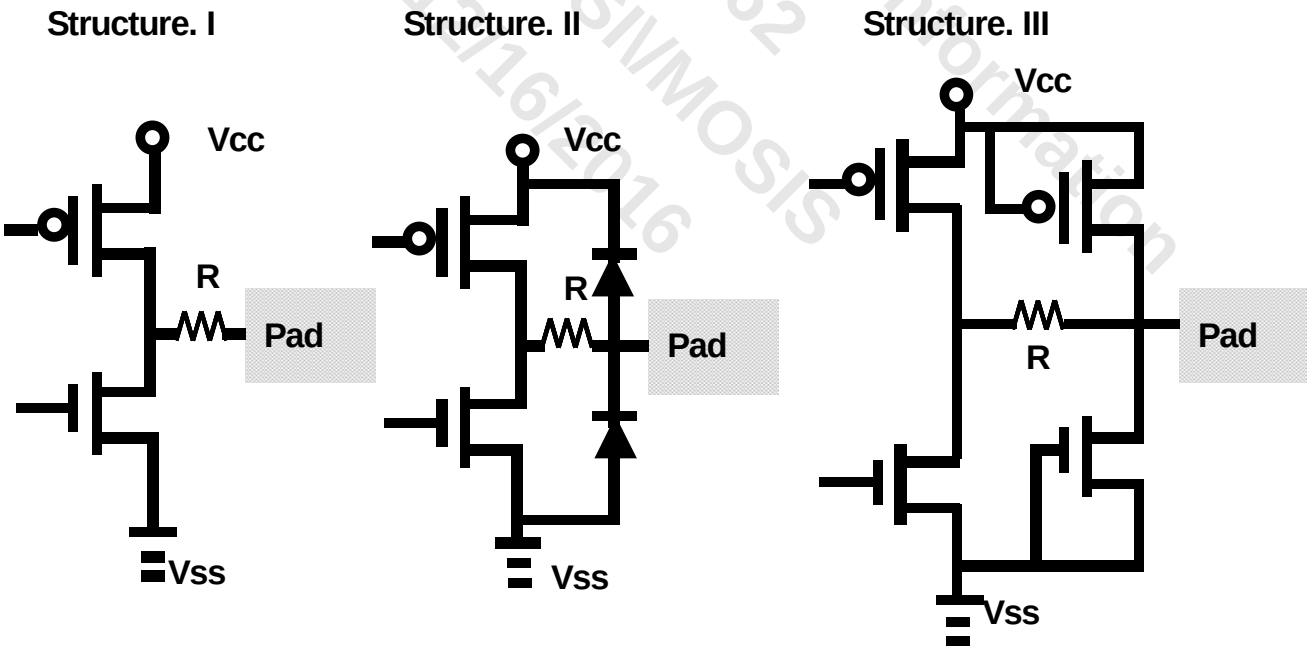

Figure 10.2.11 A resistor before the output transistor

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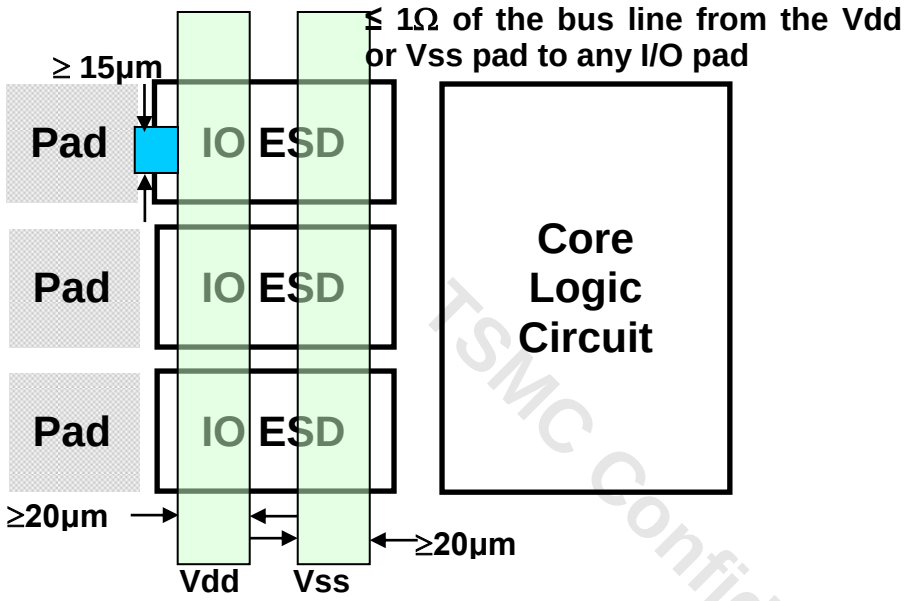

Figure 10.2.12 Bus-Lines Design

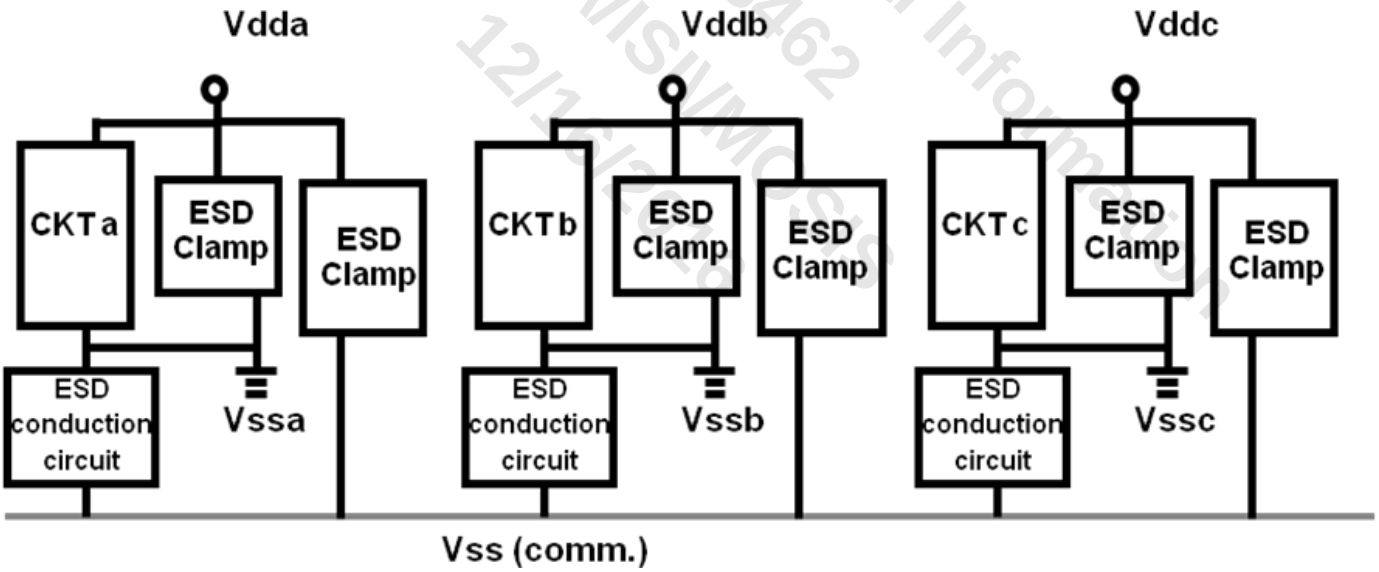

Figure 10.2.13 Schematic of a Multiple Power ESD Protection Design

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10.2.8.2 Regular I/O (3.3V/2.5V/1.8V/1.2V/1.0V RPO Device)

- DRC deck uses (N+ACTIVE AND SDI) AND (some of the related Gate partially overlap RPO but no related Gate fully inside RPO) to recognize NMOS of Regular I/O.
- DRC deck uses (P+ ACTIVE AND SDI) AND (some of the related Gate partially overlap RPO but no related Gate fully inside RPO) to recognize PMOS of Regular I/O.

No.	Description	Label		Dimension
ESD.16g	Total finger width for NMOS in same connection of gate or in same connection of drain.		≥	360
ESD.17g	Total finger width for PMOS in same connection of gate or in same connection of drain.		≥	360
ESD.18g	Channel length			
	3.3V Regular I/O (in OD33)	L	≥	0.4
	2.5V Regular I/O (in OD25)	L	≥	0.35
	1.8V Regular I/O (in OD18)	L	≥	0.2
	1.2V/1.0V Regular I/O (not in OD2)	L	≥	0.1
ESD.19g	The NMOS and PMOS should have an unsilicided area on the drain side. That is, the RPO mask should block the drain side of the device (except the contact region which should remain silicided). DRC only flags no RPO in this device.			
ESD.20g	Overlap of RPO on the drain side to the poly gate (N1/P1 in Figure 10.2.10 and Figure 10.2.14)	Z	=	0.06
ESD.21g	Width of the RPO on the drain side for NMOS. (Figure 10.2.14)	X	≥	1.0
ESD.22g	Width of the RPO on the drain side for PMOS. (Figure 10.2.14)	X	≥	1.0
ESD.23g	Space of poly to CO on the source side (Figure 10.2.14)	Y	≥	0.22

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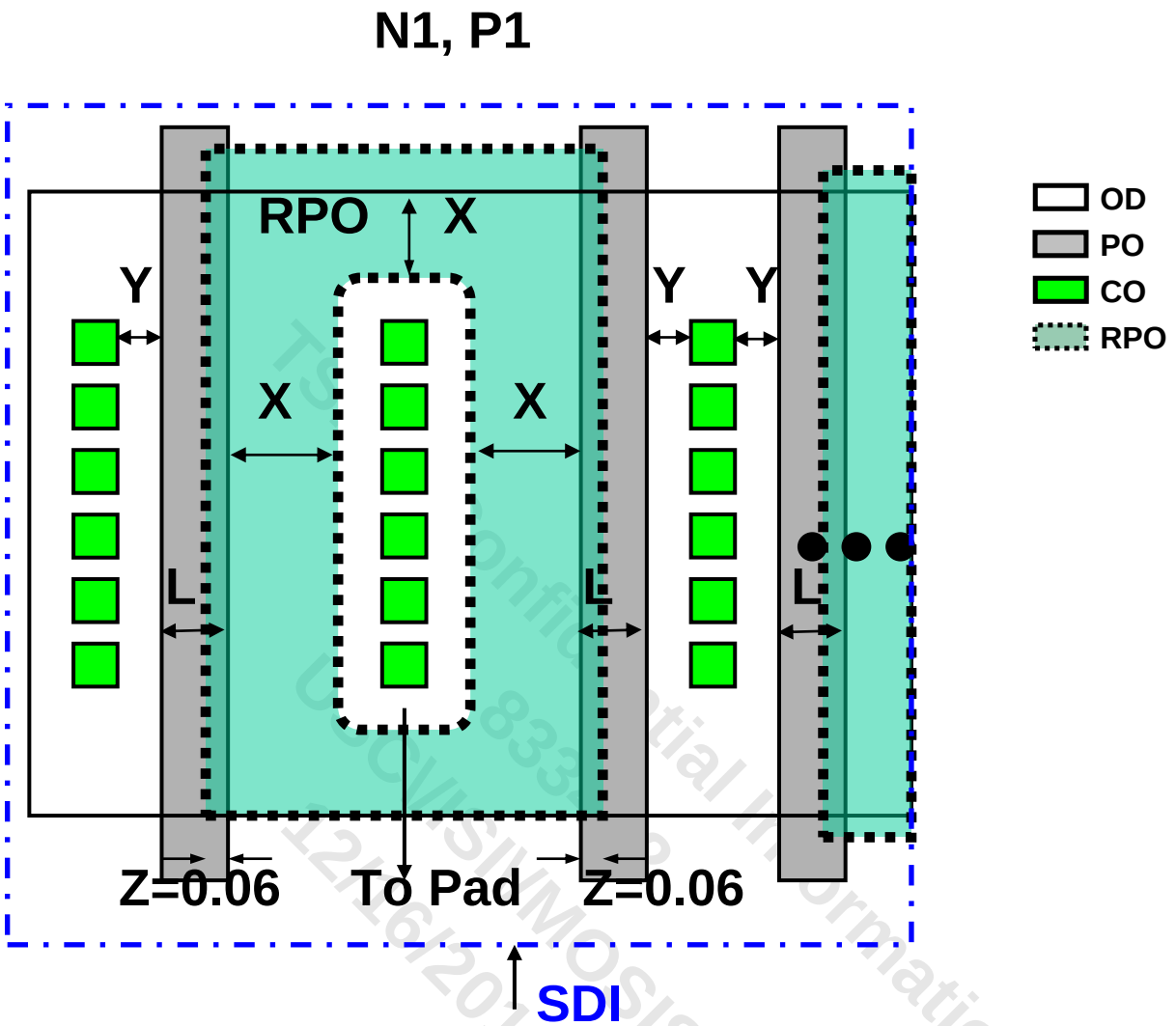

Figure 10.2.14 NMOS and PMOS (N1 and P1 in Figure 10.2.10) for regular I/O

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10.2.8.3 HV Tolerant I/O

- DRC deck uses (N+ACTIVE AND SDI) AND (some of the related Gate fully inside RPO and some of the related Gate partial overlap RPO) to recognize the NMOS of HV tolerant I/O.
- DRC deck uses (P+ ACTIVE AND SDI) AND (all of the related gates partially overlap RPO) to recognize PMOS of HV tolerant I/O, whose layout is same as PMOS of Regular I/O.
- You have to draw ESD3 or ESDIMP, which is identical to SDI, in the N2 and N3 transistors. The ESD3 or ESDIMP will be used to generate ESD mask.

No.	Description	Label		Dimension
ESD.24g	Total finger width for NMOS in same connection of gate or in same connection of drain. ESD.24g has been checked by ESD.16g.		≥	360
ESD.25g	Total finger width for PMOS in same connection of gate or in same connection of drain. ESD.25g has been checked by ESD.17g.		≥	360
ESD.26g	Channel length N2,N3, P2 in Figure 10.2.15, Figure 10.2.16 and Figure 10.2.17.			
	5V tolerant I/O (in OD33)	L	≥	0.4
	3.3V tolerant I/O (in OD25)	L	≥	0.35
	2.5V tolerant I/O (in OD18)	L	≥	0.2
	PMOS in ESD.26g has been checked by ESD.18g.			
ESD.27g	The NMOS and PMOS should have an unsilicided area on the drain side. That is, the RPO mask should block the drain side of the device (except the contact region which should remain silicided). DRC only flags no RPO in this device. PMOS in ESD.27g has been checked by ESD.19g.			
ESD.28g	For NMOS (N2 and N3 in Figure 10.2.15), the RPO needs to cover all inactive poly gates and extend to overlap the N3 gate by Z=0.06um. (Figure 10.2.15) (Figure 10.2.16)	Z	=	0.06
ESD.29g	For PMOS (P2 in Figure 10.2.15 and Figure 10.2.17), overlap of RPO on the drain side to the poly gate ESD.29g has been checked by ESD.20g.	Z	=	0.06
ESD.30g	Width of the RPO on the drain side for NMOS. (Figure 10.2.16)	X	≥	1
ESD.31g	Width of the RPO on the drain side for PMOS. (P2 in Figure 10.2.15) (Figure 10.2.17) ESD.31g has been checked by ESD.22g.	X	≥	1
ESD.32g	Space of poly to CO on the source side (Figure 10.2.16) (Figure 10.2.17) PMOS in ESD.32g has been checked by ESD.23g.	Y	≥	0.22
ESD.33g	For NMOS (N2 and N3 in Figure 10.2.15), space of the N2 gate to the N3 gate. (Figure 10.2.16)	S	=	0.25
ESD.34g	The NMOS should have ESD3 or ESDIMP DRC only flags (no ESD3/ESDIMP INTERACT N+ACTIVE) for the NMOS of HV tolerant I/O.			
ESD.35g[U]	In order to avoid turning on the diode of P+/NW (P2 in Figure 10.2.15), it is recommended to use floating NW, as your circuit design allows.			

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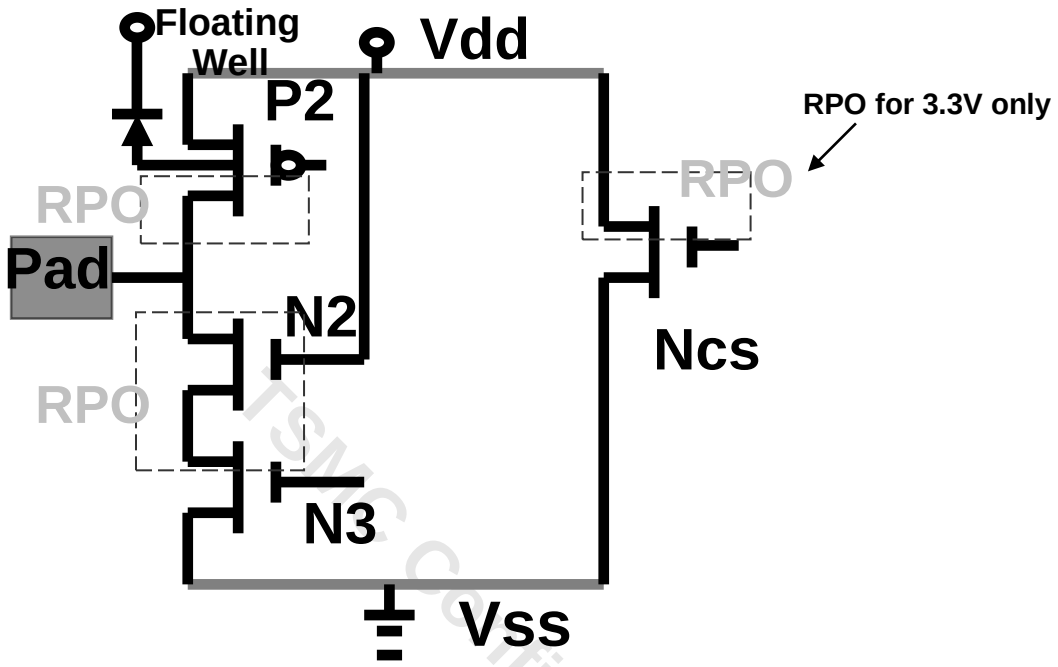

Figure 10.2.15 The schematic of HV Tolerant I/O buffer

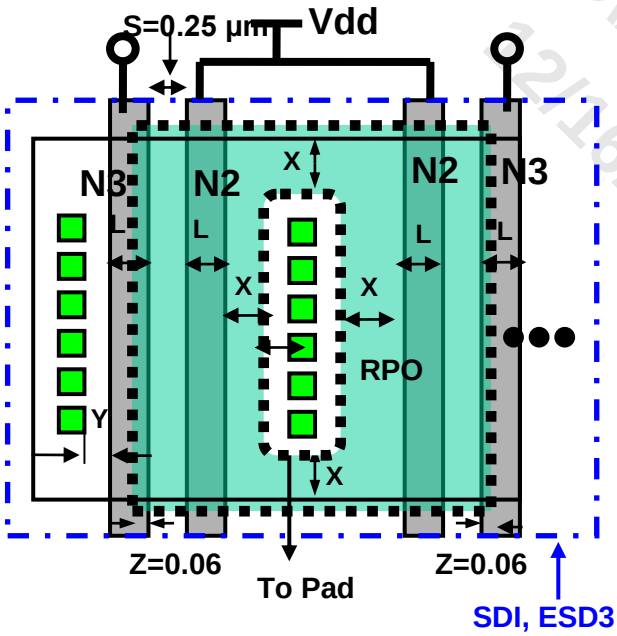

Figure 10.2.16 HV Tolerant NMOS (N2/N3 in Figure 10.2.15)

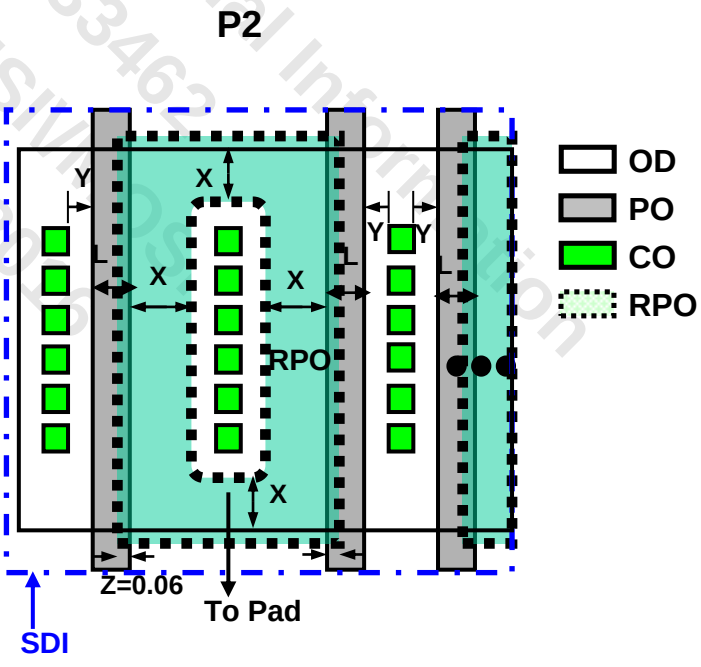

Figure 10.2.17 HV Tolerant PMOS (P2 in Figure 10.2.15)

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10.2.8.4 Power Clamp Device (Ncs)

- DRC deck uses (N+ ACTIVE AND SDI) AND (all of the related gates partially overlap RPO) to recognize 3.3V Power Clamp, whose layout is same as NMOS of Regular I/O.
- DRC deck uses ((N+ ACTIVE AND SDI) NOT INTERACT RPO) to recognize 2.5V/1.8V/1.2V/1.0V Power Clamp.
- For 2.5V/1.8V/1.2V/1.0V power clamp, the Active Power Clamp is required to put between power and ground buses. The Active Power Clamp is consisted of one trigger circuit and one big FET. The trigger circuit is designed to turn on the big FET during ESD events and keep the big FET in off state at normal operation.
- For more ESD design Tips, please see the “Tips for ESD power clamp design” section in this chapter.

No.	Description	Label		Dimension
ESD.36g	Total finger width for 3.3V Power Clamp in same connection of gate or in same connection of drain. (Ncs in Figure 10.2.18). ESD.36g has been checked by ESD.16g.		≥	360
ESD.37g	Total finger width for 2.5V/1.8V/1.2V/1.0V Power Clamp in same connection of gate or in same connection of drain. (Ncs in Figure 10.2.19)		≥	900
ESD.38g	Channel length			
	3.3V Power Clamp (in OD33) Has checked by ESD.16g.	L	≥	0.4
	2.5V Power Clamp (in OD25)	L	≥	0.35
	1.8V Power Clamp (in OD18)	L	≥	0.2
	1.2V/1.0V Power Clamp (not in OD2)	L	≥	0.1
ESD.39g	The 3.3V Power Clamp (Ncs in Figure 10.2.18) should have an unsilicided area on the drain side. That is, the RPO mask should block the drain side of the device (except the contact region which should remain silicided). DRC only flags no RPO in this device. 3.3V Power Clamp in ESD.39g has been checked by ESD.19g.			
ESD.40g	For 3.3V Power Clamp (Ncs in Figure 10.2.18), overlap of RPO on the drain side to the poly gate. ESD.40g has been checked by ESD.20g	Z	=	0.06
ESD.41g	Width of the RPO on the drain side for 3.3V Power Clamp (Ncs in Figure 10.2.18) ESD.41g has been checked by ESD.21g	X	≥	1
ESD.42g	Space of poly to CO on the source side for 3.3V Power Clamp (Ncs in Figure 10.2.18) ESD.42g has been checked by ESD.23g	Y	≥	0.22
ESD.43g^{U}	Space of poly to CO on the drain/source side for 2.5V/1.8V/1.2V/1.0V Power Clamp (Figure 10.2.19) except RC Power Clamp.	Y	≥	0.2

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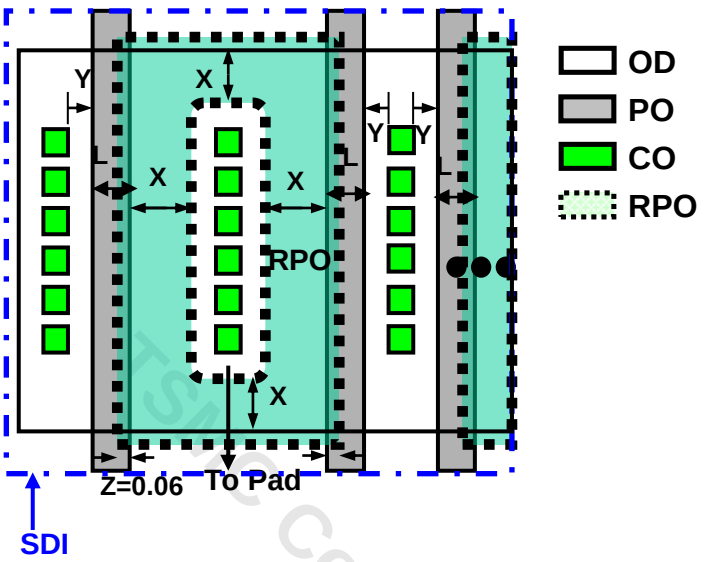

Figure 10.2.18 Ncs Layout for 3.3V in Figure 10.2.10 and Figure 10.2.15

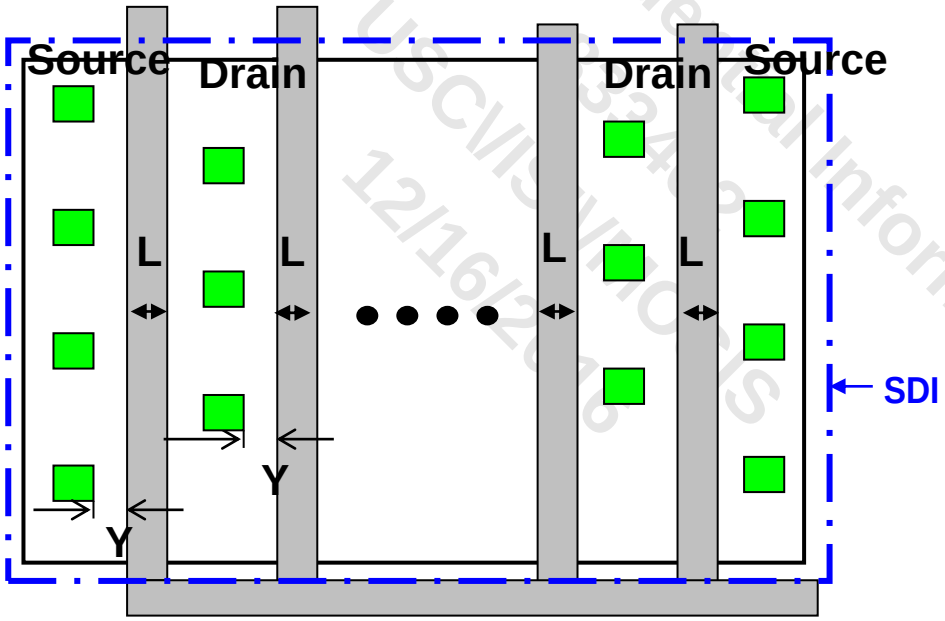

Figure 10.2.19 Ncs Layout for 2.5V, 1.8V,1.2V, and 1.0V in Figure 10.2.10 and Figure 10.2.15

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10.2.8.5 5V HVMOS protection (Field Device)

- DRC deck uses (((N+ACTIVE NOT INTERACT PO) NOT RPDMY) AND SDI) CUT RPO to recognize NFD of 5V HVMOS protection.
- DRC deck uses (((P+ACTIVE NOT INTERACT PO) NOT RPDMY) AND SDI) CUT RPO to recognize PFD of 5V HVMOS protection.
- DRC deck uses NFD connect to VSS net to recognize NFD Emitter
- DRC deck uses NFD NOT (NFD Emitter) to recognize NFD Collector
- DRC deck uses PFD connect to VDD net to recognize PFD Emitter

DRC deck uses PFD NOT (PFD Emitter) to recognize PFD Collector**.**

Rule No.	Description	Label	Op.	Rule
ESD.72g	The layer of OD2 (OD_25) is required for 5V protection (NFD and PFD)			
ESD.58g	Total width for NFD in same connection of collector. (Figure 10.2.20)		≥	360
ESD.59g	Total width for PFD in same connection of collector. (Figure 10.2.20)		≥	360
ESD.60g	STI spacing of the NFD and PFD	DL	=	0.44
ESD.61g	Unit collector width of NFD and PFD	CW	=	15-60
ESD.62g	Unit emitter width of NFD and PFD should be the same as unit collector width (EW=CW)			
ESD.63g	Unit emitter length of NFD and PFD	EL	≥	0.86
ESD.64g	Width of the RPO on the collector side for NFD and PFD	DX	≥	1.95
ESD.65g	Width of the RPO on the emitter side for NFD and PFD	DZ	=	0.1
ESD.66g	Space of RPO to CO on the collector and emitter side (Figure 10.2.20)	DY	≥	0.22

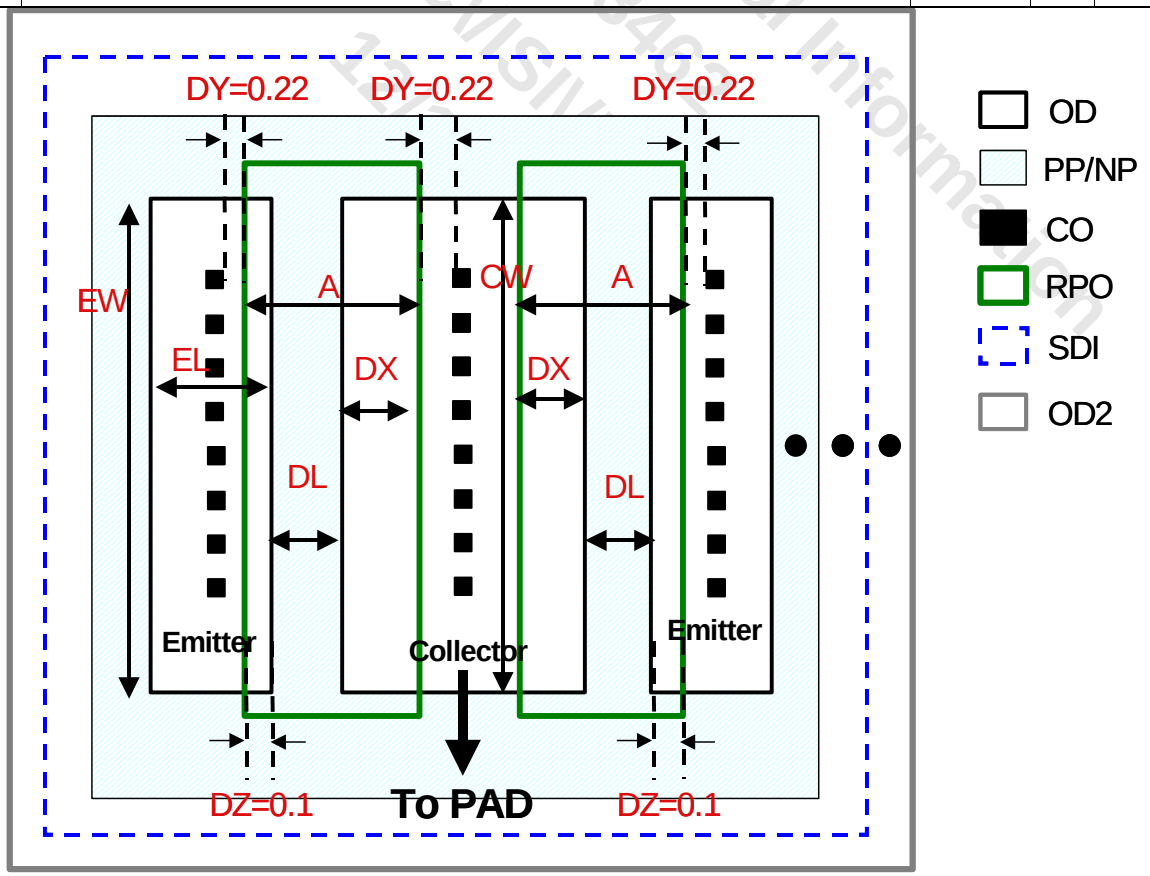

Figure 10.2.20 5V HVMOS protection layout

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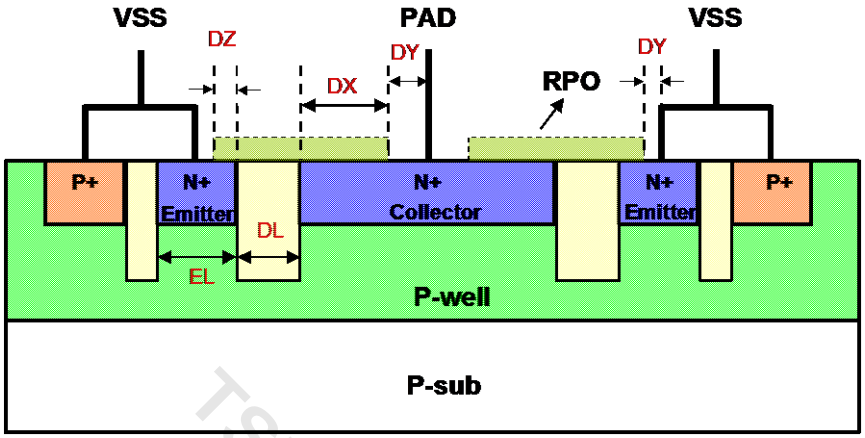

Figure 10.2.21 5V NFD HVMOS protection cross-section diagram

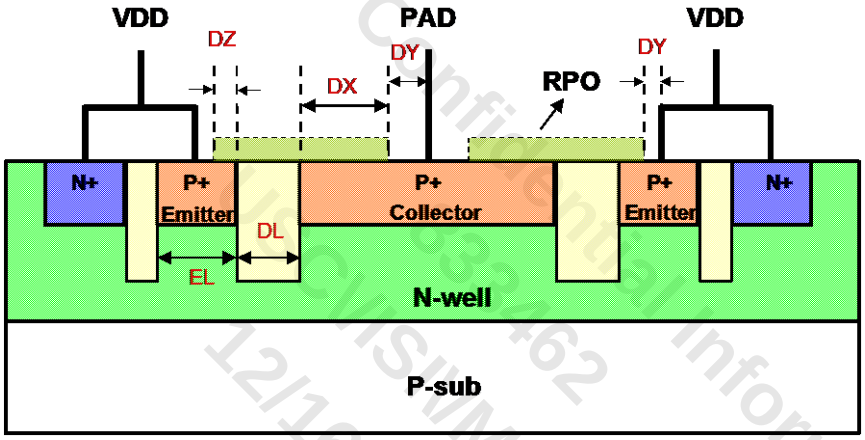

Figure 10.2.22 5V PFD HVMOS protection cross-section diagram

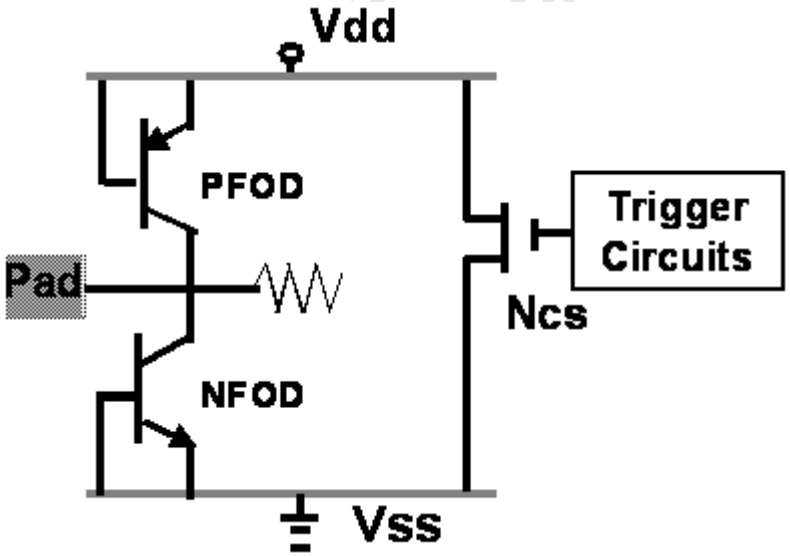

Figure 10.2.23 The schematic of 5V HVMOS protection

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10.2.8.6 RPO and ESD Implant Summary

I/O Device	3.3V/2.5V/1.8V/1.2V/1.0V NMOS for Regular IO	3.3V/2.5V/1.8V/1.2V/1.0V PMOS for Regular IO	NMOS of 5V/3.3V/2.5V HV Tolerant IO	PMOS of 5V/3.3V/2.5V HV Tolerant IO	3.3V NMOS for Power Clamp	2.5V/1.8V/1.2V/1.0V NMOS for Power Clamp
Minimum RPO width on drain side (X)	1.95	1.0	1.95	1.0	1.95	No need
RPO-to-N2(Z) =	Overlap poly by 0.06	Overlap poly by 0.06	Completely cover N2	Overlap poly by 0.06	Overlap poly by 0.06	No need
N2-to-N3 space =	NA	NA	0.25	NA	NA	No need
RPO coverage in the diffusion region between poly gates	NA	NA	Completely cover diffusion	NA	NA	No need
RPO-to-N3 (Z) =	NA	NA	Overlap N3 by 0.06	NA	NA	No need
ESD implant	3.3V/2.5V: Option 1.8V/1.2V/1.0V: No need	No	Yes	No	Option	No need
Dummy layer for DRC	SDI	SDI	SDI	SDI	SDI	SDI
Dummy layer for ESD mask making. ESD3 or ESDIMP	3.3V/2.5V: Option: ESD3 1.8V/1.2V/1.0V: No need	No	ESD3/ESDIMP	No	Option: ESD3/ESDIMP	No need
Illustration	Figure 10.2.14	Figure 10.2.14	Figure 10.2.15	Figure 10.2.17	Figure 10.2.18	Figure 10.2.19

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10.2.8.7 Additional Two ESD Structures

In this section, we keep supporting the two previous kinds of ESD structures (design rule before V1.3). However, it is recommended to use the updated structures (section 10.2.6.2~4) to simplify the ESD device structure.

10.2.8.7.1 1.8V Regular IO

- DRC deck uses ((N+ ACTIVE AND SDI) INTERACT RPO) AND (the related Gate NOT INTERACT RPO) to recognize 1.8V NMOS of Regular I/O.
- DRC deck uses ((P+ ACTIVE AND SDI) INTERACT RPO) AND (the related Gate NOT INTERACT RPO) to recognize 1.8V PMOS of Regular I/O.
- The ESD performance of this structure is worse than that in section 10.2.6.2, so recommend to use the structure of section 10.2.6.2 for 1.8V regular IO.

No.	Description	Label		Dimension
ESD.44g	Total finger width for NMOS in same connection of gate or in same connection of drain. ESD.44g has been checked by ESD.16g.		≥	360
ESD.45g	Total finger width for PMOS in same connection of gate or in same connection of drain. ESD.45g has been checked by ESD.17g.		≥	360
ESD.46g	Channel length (in OD18)	L	≥	0.2
ESD.47g	The NMOS and PMOS should have an unsilicided area on the drain side. That is, the RPO mask should be in the drain side of the device (except the contact region which should remain silicided). DRC only flags no RPO in this device.			
ESD.48g	RPO on the drain side space to the poly gate (N1/P1 in Figure 10.2.10) and (Figure 10.2.24).	S	=	0.45
ESD.49g	Width of the RPO on the drain side for NMOS. (Figure 10.2.24)	X	≥	1
ESD.50g	Width of the RPO on the drain side for PMOS. (Figure 10.2.24)	X	≥	1
ESD.51g	Space of poly to CO on the source side (Figure 10.2.24)	Y	≥	0.22
ESD.52g	1.8V regular IO INTERACT OD_25 or OD_33 is not recommended.			

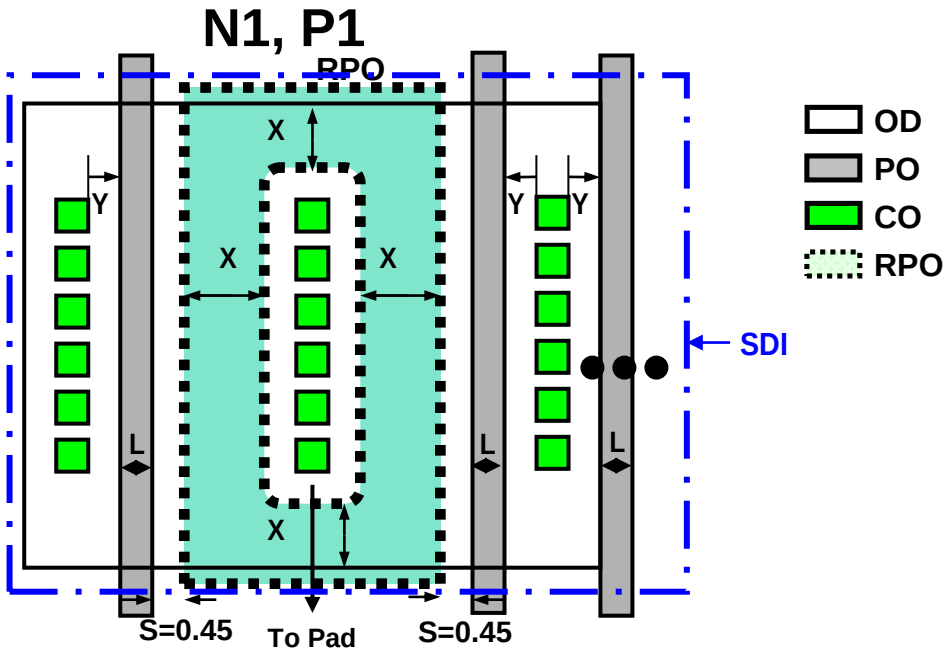

Figure 10.2.24 1.8V I/O NMOS and PMOS (N1 and P1 in Figure 10.2.10)

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10.2.8.7.2 3.3V, 2.5V Power Clamp (Ncs)

- DRC deck uses ((N+ ACTIVE AND SDI) INTERACT RPO) AND (the related Gate fully inside RPO) to recognize 3.3V, 2.5V Power Clamp.

No.	Description	Label		Dimension
ESD.53g	Total finger width in same connection of gate or in same connection of drain. ESD.53g has been checked by ESD.16g.		≥	360
ESD.54g	Channel length			
	3.3V Power Clamp (in OD33)	L	≥	0.4
	2.5V Power Clamp (in OD25)	L	≥	0.35
ESD.55g	The NMOS should have an unsilicided area on the drain/source side. That is, the RPO mask should be in the drain/source side of the device (except the contact region which should remain silicided). DRC only flags no RPO in this device.			
ESD.56g	Width of the RPO on the drain side for NMOS. (Figure 10.2.25). DRC recognizes the drain side by N+OD NOT connected to PW STRAP.	X	≥	1
ESD.57g	Space of poly to CO on the source side (Figure 10.2.25)	Y	≥	0.22

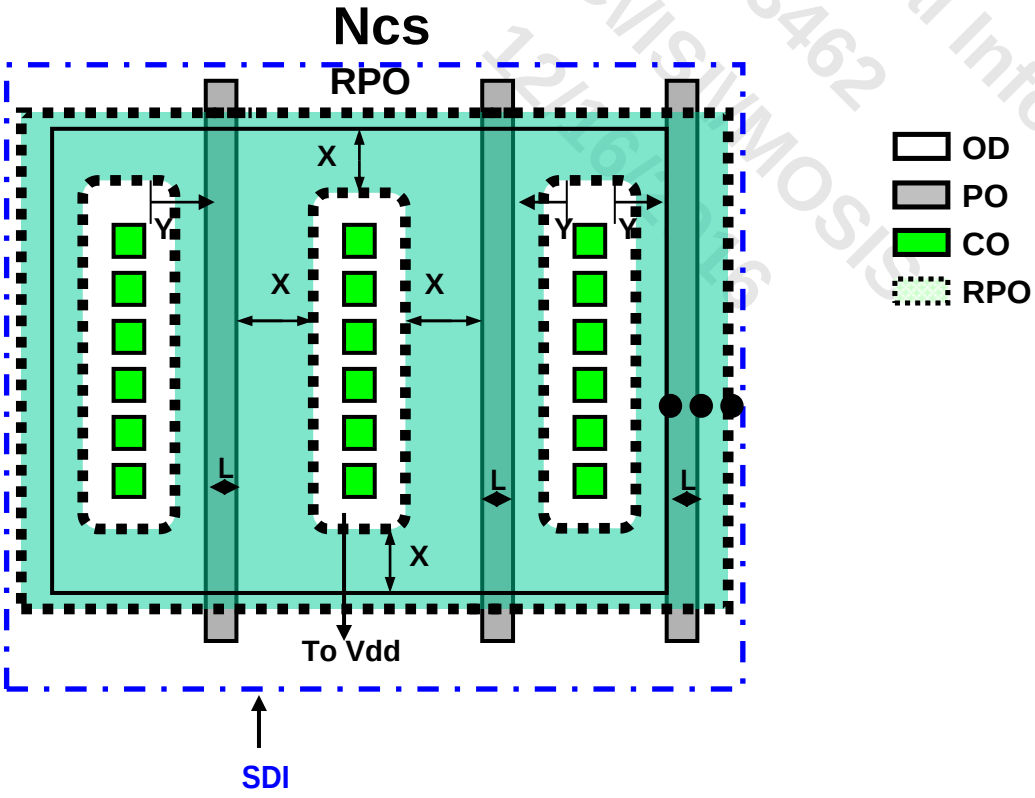

Figure 10.2.25 Ncs Layout for 3.3V or 2.5V in Figure 10.2.10 and Figure 10.2.15

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10.2.9 CDM Protection for Cross Domain Interface

CDM is an increasingly important issue for modern integrated circuits technology as the gate oxide thickness keeps on shrinking and the number of power domains continues increasing. With respect to the CDM protection, the cross-domain interface is the most crucial situation as compared with the I/O input gate (defined as ESD.9g in DRM), the gate directly connected to power/ground, and the long signal path without parasitic junction diode. It is because that the fatal CDM charges are mostly accumulated at the power/ground metal buses and easily damage the gate oxide at the interface when the discharge current path crosses the different power domains.

To prevent this kind of CDM damage for the complex power domains, the protection scheme is proposed as Figure 10.2.26 shown. The protection network consists of a resistor, a pair of gate-ground NMOS and gate-Vdd PMOS and active power clamp cells. The resistance and related device dimensions are listed in the following Table 1. Basically, the protection transistors have to be placed as close to the receiver gates as possible, and share the same power/ground and well of the receiver cell. A global active clamp cell should be placed near the cross-domain interface to help conducting the CDM currents. Additionally, the resistance of power bus between the global active power clamp cells is recommended to be smaller than 1Ω. The turn-on resistance of “current conducting element” should be as small as possible to minimize the voltage drop during CDM zapping.

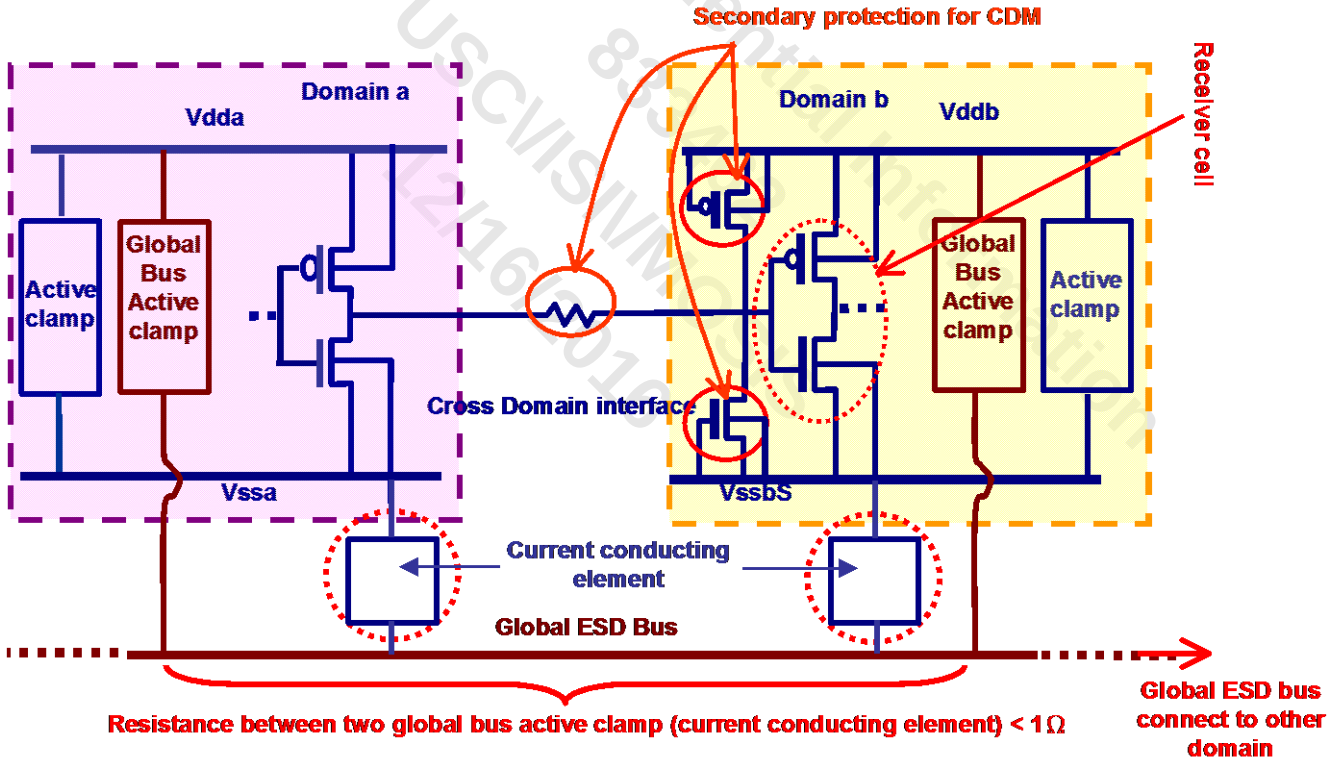

Figure 10.2.26 The protection scheme for cross-domain CDM

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Rule No.	Description	Label		Rule
ESD.67g^{U}	Total finger width of 3.3V/2.5V/1.8V/1.2V/1.0V cross-domain secondary protection. (GGN/PMOSFET in Figure 10.2.26)		≥	8
ESD.68g^{U}	Channel Length for 3.3V domain b secondary protection. (GGN/PMOSFET in Figure 10.2.26)		=	0.38
ESD.69g^{U}	Channel Length for 2.5V domain b secondary protection. (GGN/PMOSFET in Figure 10.2.26)		=	0.27
ESD.69.1g^{U}	Channel Length for 1.8V domain b secondary protection. (GGN/PMOSFET in Figure 10.2.26)		=	0.15
ESD.69.2g^{U}	Channel Length for 1.2V/1.0V domain b secondary protection. (GGN/PMOSFET in Figure 10.2.26)		≥	0.07~0.1
ESD.70g^{U}	RPO poly resistor is recommended for cross-domain protection (resistor in Figure 10.2.26)		≥	200Ω
ESD.71g^{U}	Bus resistance between two global bus active clamps		<	1Ω

10.2.10 High Current Diode (HIA_DIO)

10.2.10.1.1 Dual-Diode I/O Protection

HIA_DIO stands for the diode, which can be used for logic, low capacitance or high speed/frequency ESD protection. For diode-base ESD protection scheme, it should work together with low trigger power clamps, such as RC-gate driven clamp.

Fig. 10.2.30 shows the common dual-diode protection scheme. One diode is for pull-up path to the VDD and the other is for pull-down path to the VSS. There are four current discharge paths between the PAD, VDD and VSS. The brief descriptions are as follows:

1. For a positive pulse from PAD respect to VDD, the current passes through the pull-up diode to VDD.
2. For a negative pulse from PAD respect to VDD, the current enter the VDD pin, through the power clamp, and then passes through the pull-down diode,
3. For a positive pulse from PAD respect to VSS, the current passes through the pull-up diode, along the supply metal bus to through the power clamp and out the VSS.
4. For a negative pulse from PAD respect to VSS, the current passes through the pull-down diode and out the PAD.

Please note that excellent ESD performance is achieved when the discharge paths are confined to the design paths as mentioned above. It depends on the low turn-on resistance of the diode, wiring and power clamp devices. The designer should minimize the I-R drop effect as much as possible. The resistance of metal bus between the PAD and power clamp should be less than 1 ohm. Also, both the ESD level and parasitic capacitance are directly proportional to the diode's perimeter. Hence, the designer should consider the parasitic capacitance of the diodes on the I/O PAD and has to balance the ESD and circuit's performance.

10.2.10.1.2 Layout Guidelines for HIA_DIO

HIA_DIO is the diodes both can use for logic, high speed or low capacitance ESD clamp (Fig. 10.2.30).

The HBM level is proportional to the diode's perimeter, however the parasitic capacitance is increasing also.

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10.2.10.1.3 HIA_DIO Layout Guidelines

10.2.10.1.3.1 HIA_DUMMY Layer (CAD layer: 168:0)

DRC deck uses (N+ ACTIVE AND HIA_DUMMY NOT NW) to recognize N diodes for ESD protection.

DRC deck uses (P+ ACTIVE AND HIA_DUMMY AND NW) to recognize P diodes for ESD protection.

Draw HIA_DUMMY (CAD layer: 168:0) to fully cover diode's OD regions that are connected to I/O pads, including the anode, cathode, and guard-ring. Refer to Figure 10.2.27, and shown below. It is for DRC usage but not a tape out required CAD layer.

Diode's layout (all dimensions of width/length/spacing/overlap) should be exactly identical to the p_cell, or the RF model's accuracy will be impacted.

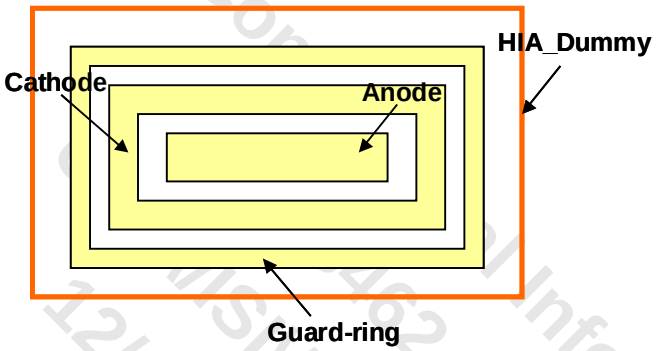

Fig. 10.2.27 Example of HIA_DUMMY

10.2.10.1.3.2 High current diodes protection

Rule No.	Description	Label	Op.	Rule
HIA.1g^{U}	Unit finger width of single and multi-finger diodes. (Figure 10.2.28 and Figure 10.2.29)	A	=	0.6-1.6
HIA.2g^{U}	Unit finger length of single and multi-finger diodes. (Figure 10.2.28 and Figure 10.2.29)	B	=	5-40
HIA.3g^{U}	Total perimeter of hia_diode. (Figure 10.2.28 and Figure 10.2.29)		≥	300
HIA.4g^{U}	The STI spacing of the longer side of anode (P-diode) between anode and cathode, and vice versa for N-diode. (Figure 10.2.28 and Figure 10.2.29)	C1	=	0.3-0.4
HIA.5g^{U}	The STI spacing of the shorter side of anode (P-diode) between anode and cathode, and vice versa for N-diode. (Figure 10.2.28 and Figure 10.2.29)	C2	=	0.6-0.8
HIA.6g^{U}	Cathode width should be larger than anode width for P-diode, and anode width should be larger than cathode width for N-diode (D≥A). (Figure 10.2.28 and Figure 10.2.29)	D		
HIA.7g^{U}	The sum of metal connections' width (all fingers and metal layers) of anode or cathode to the bond pad should be larger than 15um to handle high ESD current. (HBM/MM=2kV/200V) (Figure 10.2.28 and Figure 10.2.29)	I	≥	15
HIA.8g^{U}	Value of RPO poly resistor R (Ω) for input protection (Figure 10.2.30)	R	≥	200
HIA.9g^{U}	Protection scheme should include gate-driven power clamps (Figure 10.2.30), a trigger circuit (such as RC-trigger) is required.			

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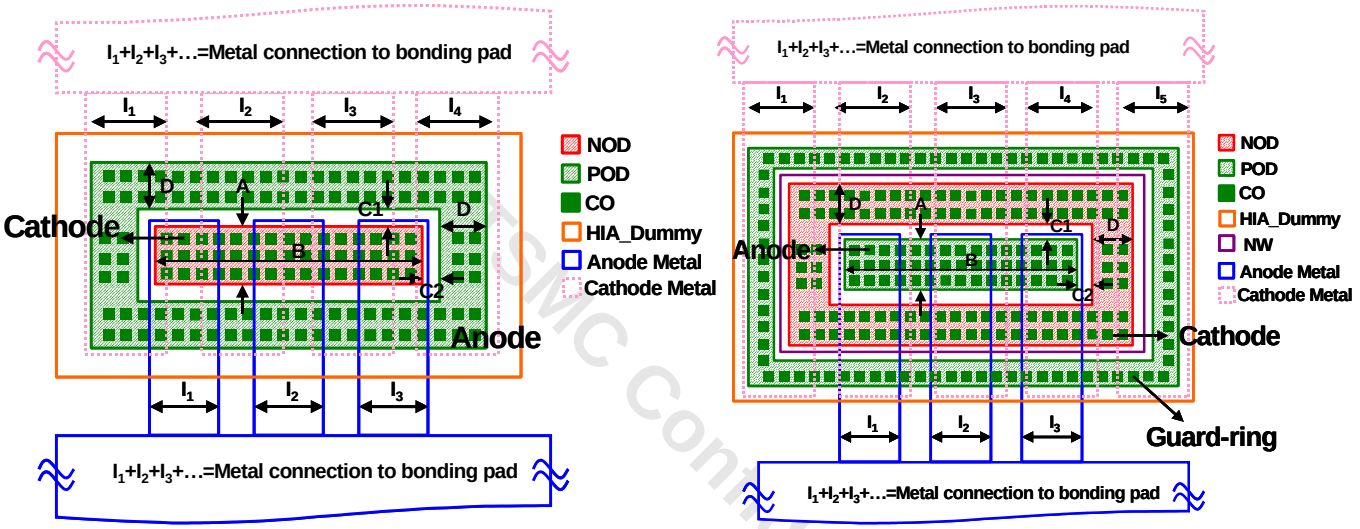

Figure 10.2.28 Single-finger type N-diode's and P-diode's layout

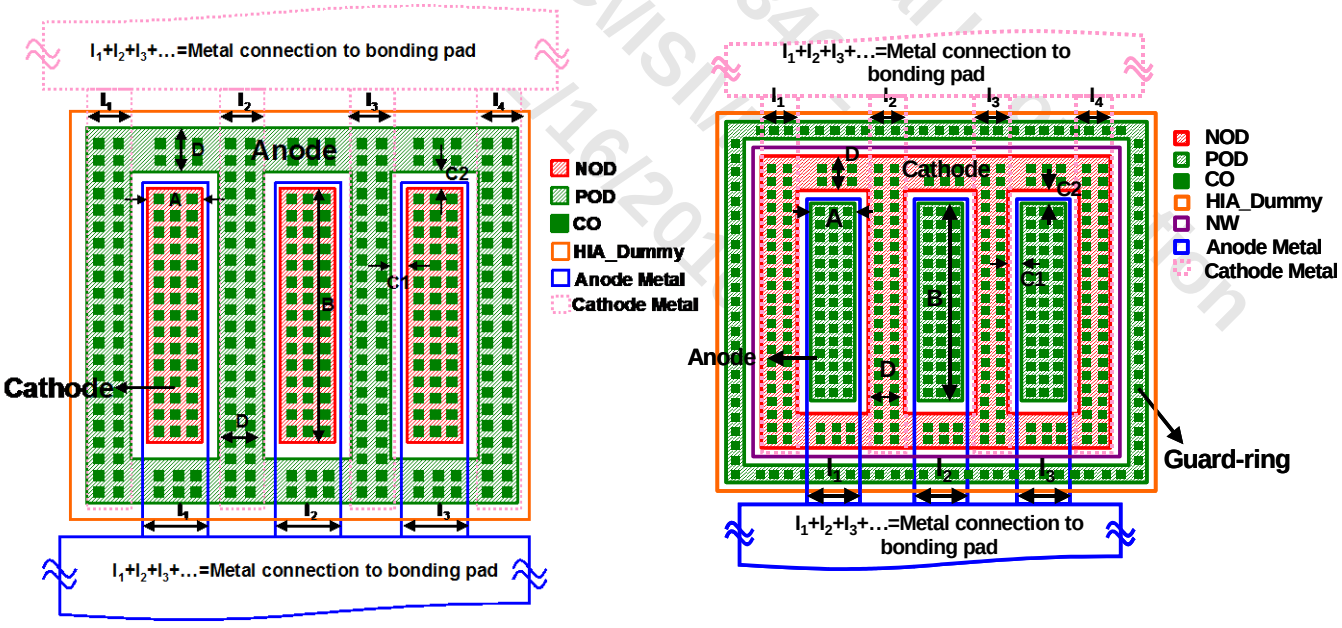

Figure 10.2.29 Multi-finger type N-diode's and P-diode's layout

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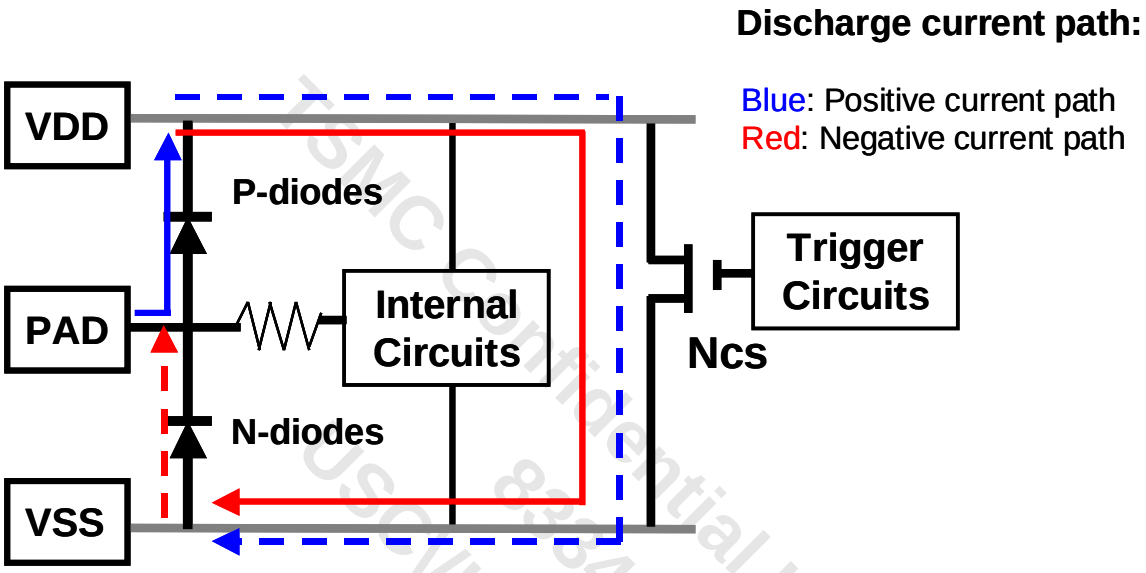

Figure 10.2.30 The schematic diagram for diode-base protection

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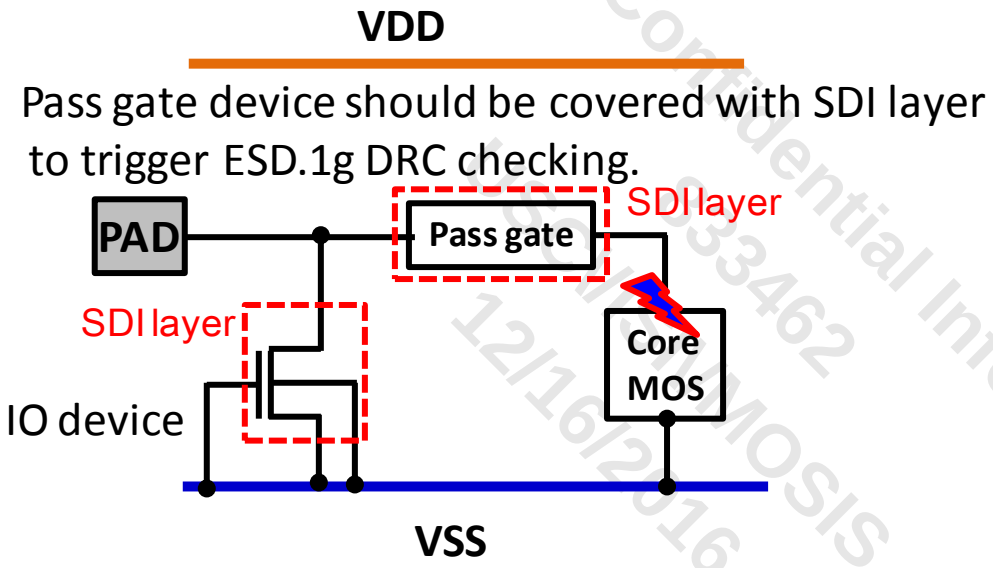
10.2.11 Tips for the ESD/LU Design

To enhance ESD/LU immunity, the following guidelines are recommended.

(1) If a gate is connected to VDD/VSS directly, a low-trigger power clamp is required. Also, the power bus resistance needs to be smaller than 1ohm between the pad and power clamp. Otherwise, please avoid it.
(2) Any Drain/Source/Gate of a transistor connected to a pad should have ESD protection.
(3) Contacts and vias should be as many as possible in all ESD devices and current paths, including the diode and metal connection.
(4) All the guard rings and STRAPs should be connected to VDD/VSS directly with very low parasitic resistance. Use as many contacts and vias as possible.
(5) When a pass-gate device is added between a PAD and a core device, please pay attention to the core device's ESD protection. Don't use an IO device to protect the core device (as below figure shown). It's recommended to cover the pass-gate device with an SDI layer to trigger the ESD.1g check.



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10.2.12 Tips for the Power ESD Protection

To avoid ESD damage to internal circuits, the ESD protection design is intended not only for the input, output, or power pins, but also for the whole chip. Of special concern are the digital and analog circuits. In the mixed-mode ICs, separate digital and analog powers are used, and the interface devices between the digital and analog circuits are especially sensitive to ESD damage.To achieve a better ESD immunity, add inter-power ESD protection circuits by using the following:

1. Add ESD clamping cells/circuits to provide discharge paths between V_{DD} and V_{SS} as many as possible. Each set of V_{DD} and V_{SS} must have its own power clamp cells.
2. Cross-couple power clamps between multi-power supplies are necessary including Vdd(x) to Vss(y) and Vdd(x) to Vdd(y). The x and y denote different power supply combination.
3. For power protection, if there is enough space, the larger total channel width the better ESD immunity.
4. Use at least one clamping and/or conduction cell for every 1.0Ω of power line resistance.
5. Power lines should keep ultra low resistance and avoid disconnect. For different powers or grounds with same potential, use bi-directional cell to link them such as back to back diodes.
6. Each component of power clamp and back to back diode cells must be surrounded by double guard rings to avoid latch up.
7. The turn-on detector circuits of active power clamp should be well designed to avoid mis-trigger subjected to power noise or glitch, for example the RC time constant and the junctions acting as minority collectors.
8. Guard rings directly connected to V_{DD} or V_{SS} power pad should be as wide as possible, to avoid silicon burnout on parasitic junction diode during ESD events.

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10.2.13 ESD test methodology

10.2.13.1 Stress condition and Measurement condition

The ESD test items include HBM and MM which need to meet MIL-STD 883 and EIAJ IC-121, or JEDEC standards. The rise time and decay time of HBM are within 10ns and 150ns, respectively. The rise time and period of MM are within 10ns and 80ns, respectively. The specification for HBM is 2KV and for MM is 200V. The peak currents for 2KV HBM is1.2A-1.48A and for MM 200V is 2.8A-3.8A.
The ESD test is performed at room temperature. The sample size for ESD test is three devices and each device are stressed three times at each voltage level. The DC parametric and functional testing at room temperature is performed on all devices before ESD testing. The test devices need to meet device data sheet requirements and the DC parameters.
The pin zapping combinations depend on the number of power pin groups like VDD1, VDD2, VSS1, VSS2, GND, etc. Please refer to MIL-STD 883 and EIAJ IC-121, or JEDEC standards.

10.2.13.2 Failure criteria

The DC parametric and functional testing of the device should be characterized after each voltage level to check the device ESD failure threshold. The device will be defined as a failure if, after exposure to ESD pulses, it no longer meets the device data sheet requirements using DC parameter and functional testing.

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11 Reliability Rules

This chapter provides information about the following:

11.1 Terminology
11.2 Front-end process reliability rules and models
11.3 Back-end process reliability rules
11.4 Product early failure rate screening guidelines
11.5 e-Reliability model system introduction

The information in this chapter is to help you meet their product application needs and their design-in reliability goals. The following sections include descriptions about gate oxide integrity, hot carrier effect injection (HCI), PMOS negative bias temperature instability (NBTI), EM, and SM specifications.

11.1 Terminology

This section provides definitions for key terms that are included in this chapter.

Table 11.1.1

Term	Definition
MTTF	The lifetime in which 50% of the population has failed
0.1% cumulative failure	The lifetime in which 0.1% of the population has failed

11.2 Front-End Process Reliability Rules and Models

This section provides information about overdrive voltage, gate oxide integrity, HCI degradation, and negative bias temperature instability.

11.2.1 Guidelines for I/O Over Drive Voltage

For 2.5V I/O device, it can be operated at 3.3V with 10% tolerance. The assumptions are:

1. The device concerns Idsat shift only, not Vt shift. The failure criterion is Idsat shift 10%, and an AC lifetime of 10 years.
2. Device operated at 3.3V only, and 10% Idsat shift is based on 3.3V Idsat value.
   And, to meet overdrive requirement, poly channel length must be extended to:
   NMOS Lg_minimum extend to 0.5um for 3.3V + 10%.
   PMOS Lg_minimum extend to 0.4um for 3.3V +10%

11.2.2 Guidelines for Gate Oxide Integrity

This section provides information to help you predict gate oxide reliability and prevent a time dependent dielectric breakdown (TDDB). TDDB is the breakdown of gate oxide induced by a combination of voltage, junction temperature, and oxide thickness.

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Warning: Following the guidelines in this section ensures a reliability performance of a 0.1% cumulative failure rate for reference conditions as a function of transistor type, oxide thickness and area, junction temperature, and applied gate voltage. Deviations from these guidelines could result in a potentially unreliable integrated circuit. For specific memory or analog capacitor applications, please consult with TSMC to ensure the required product level reliability specification can be met.

11.2.2.1 Gate Oxide Lifetime Prediction Model

For core thin gate oxide and I/O thick gate oxide:

Time to failure $\propto (V_{cc})^{-n} \times \exp(E_a/K_T) \times (A_{ox})^{-1/\beta}$ **equation (1)**

Where:

A_{ox} is the total gate oxide area on silicon (unit: μm^2)

T is the absolute junction temperature (unit: K)

V_{cc} is the gate voltage (unit: volt)

n is the power law exponent for core thin gate oxide (voltage acceleration factor)

E_a is the thermal activation energy

k is the Boltzmann's constant ((8.617×10^{-5}) cV/K)

β is the Weibull shape factor (distribution spread)

11.2.2.2 Failure Mechanism

When an electron current is passed through gate oxide, defects such as electron traps, interface states, positively charged donor-like traps, and so on, gradually build up in the gate oxide until a conduction path is formed, followed by thermal run away.

According to the anode hole injection model, injected electrons generate holes at the anode that can tunnel back into the oxide. Intrinsic breakdown occurs when a critical hole density is reached.

11.2.2.3 Test Methodology

11.2.2.3.1 Measurement conditions

1. **I_g** is the gate current with $V_b=V_s=V_d=GND$. T=125°C.
2. **V_g** is set to 5.5 ~ 7.6 volts for N65LP/N65LPG, or 3.4 ~ 4.1 volts for N65G/N65GP, for thick (I/O) gate oxide.
3. **V_g** is set to 3.1 ~ 4.1 volts for N65LP/N65LPG (LP oxide), or 2.7 ~3.2 volts for N65G/N65LPG (G oxide)/ N65GP, for thin (core) gate oxide.

11.2.2.3.2 Stress Conditions

At least 50 samples constitute a sample size for core.

At least 30 samples constitute a sample size for I/O.

1. To determine the **voltage acceleration factor (n)**, 3 stress voltages are used at each fixed stress temperature.
2. To determine the **thermal activation energy (E_a)**, 3 stress temperatures are used at each fixed stress voltage.

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11.2.2.3.3 Failure Criteria

The failure criterion for thin (core) gate oxide is an onset of the first soft breakdown when there is a gate current (I_g) progressively increasing in noise or variance. The failure criterion for thick (I/O) gate oxide is a hard breakdown.

The following table provides an example of maximum gate voltage (V_{ccmax}) calculations for 65nm LP core gate oxide applications. The reference conditions are a gate oxide area of 0.1 cm², a cumulative failure rate of 0.1%, and a duty factor of 100%.

Table 11.2.1 65nm LP/ LPG (LP oxide) Core Maximum Gate Voltage for Reference Condition with 0% Tolerance;

Area (Aox=0.1cm²); Failure Rate (Fref=0.1%) Duty Factor of 100%

NMOS					PMOS				
LifeTime (Years)	**T= 65°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**	**Lifetime (Years)**	**T= 65°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**
10	1.80	1.77	1.74	1.71	**10**	1.72	1.68	1.64	1.61
7	1.82	1.78	1.75	1.72	**7**	1.73	1.69	1.66	1.62
5	1.83	1.79	1.76	1.73	**5**	1.75	1.71	1.67	1.64

Table 11.2.2 65nm G/ LPG (LP oxide) Core Maximum Gate Voltage for Reference Condition with 0% Tolerance;

Area (Aox=0.1cm²); Failure Rate (Fref=0.1%) Duty Factor of 100%

NMOS					PMOS				
LifeTime (Years)	**T= 65°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**	**Lifetime (Years)**	**T= 65°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**
10	1.33	1.29	1.25	1.22	**10**	1.33	1.29	1.25	1.22
7	1.34	1.30	1.26	1.23	**7**	1.34	1.30	1.26	1.23
5	1.35	1.31	1.27	1.24	**5**	1.35	1.31	1.27	1.24

Table 11.2.3 65nm GP Core Maximum Gate Voltage for Reference Condition with 0% Tolerance;

Area (Aox=0.1cm²); Failure Rate (Fref=0.1%) Duty Factor of 100%

NMOS					PMOS				
LifeTime (Years)	**T= 65°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**	**Lifetime (Years)**	**T= 65°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**
10	1.26	1.23	1.21	1.19	**10**	1.44	1.36	1.30	1.24
7	1.27	1.24	1.22	1.20	**7**	1.46	1.39	1.32	1.26
5	1.28	1.25	1.23	1.21	**5**	1.49	1.41	1.34	1.28

Table 11.2.4 55nm LP (LP oxide) Core Maximum Gate Voltage for Reference Condition with 0% Tolerance; Area (Aox=0.1cm²); Failure Rate (Fref=0.1%) Duty Factor of 100%

Area (Aox=0.1cm²); Failure Rate (Fref=0.1%) Duty Factor of 100%

NMOS					PMOS				
LifeTime (Years)	**T= 55°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**	**Lifetime (Years)**	**T= 55°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**
10	1.85	1.80	1.77	1.74	**10**	1.79	1.72	1.68	1.65
7	1.86	1.81	1.78	1.75	**7**	1.81	1.74	1.70	1.66
5	1.88	1.82	1.79	1.76	**5**	1.82	1.75	1.71	1.68

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Table 11.2.5 55nm GP Core Maximum Gate Voltage for Reference Condition with 0% Tolerance;
Area (Aox=0.1cm²); Failure Rate (Fref=0.1%) Duty Factor of 100%

NMOS					PMOS				
LifeTime (Years)	**T= 55°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**	**Lifetime (Years)**	**T= 55°C**	**T= 85°C**	**T= 105°C**	**T= 125°C**
10	1.35	1.31	1.28	1.26	**10**	1.49	1.37	1.31	1.26
7	1.36	1.32	1.29	1.27	**7**	1.51	1.39	1.33	1.28
5	1.37	1.33	1.30	1.28	**5**	1.54	1.42	1.35	1.30

11.2.3 Guideines for Hot Carrier Injection Effect

Hot carriers are holes or electrons that have been accelerated to a high energy by a local electric field. Hot carrier degradation can significantly impact circuit performance and functionality. It is important for circuit designers to carefully check the lifetime degradation of their designs caused by hot carrier injection (HCI). Cumulative degradation and process variation must be taken into account for burn-in, field operation, and overdrive applications.

11.2.3.1 Lifetime Prediction Model for Device Degradation

Owing to the importance of hot carrier injection on circuit operation, you should employ detailed models to calculate device degradation during circuit operation and to simulate the impact on circuit operation. The following is a general model for the degradation of device characteristics:

$$MTTF = A \times f(L, W) \times (\Delta\%)^{1/n} \times \exp[B \times (1/V_{ds})] \times \exp[E_a/k\,(1/T)] \quad \textbf{equation (3)}$$

Where:

MTTF is the mean time to failure

L is the drawn channel length (unit: μm)

W is the drawn channel width (unit: μm)

Δ% is the percentage degradation of an electrical parameter (for example, 10% I_{dsat}, 10% G_m)

V_{ds} is the drain to source bias (unit: volt)

n is the power law factor of time dependent degradation

E_a is the activation energy

k is the Boltzmann constant ((8.617 × 10-5) cV/K)

T is the absolute junction temperature (unit: K)

A and **B** are empirical fitting parameters

11.2.3.2 Failure Mechanism

A percentage of the energetic hot carriers will impact the lattice and create electron-hole pairs. The created electron-hole pairs will create even more pairs later on. If the hot carriers have a kinetic energy larger than the silicon-insulator barrier height, some of the carriers may surmount the barrier and be propelled toward the insulator that has a moderate or higher gate bias. These carriers can either be trapped in the oxide region or at the Si-SiO2 interface. The trapped charges from HCI stress have the following effect on the transistors:

1. Shift in the V_t (threshold voltage) of the device
2. Reduced mobility of the conducting carriers
3. Reduced device drain current
4. Increased effective series resistance, from a charge trapped above the S/D extension region
5. Degraded sub-threshold slope

These transistor changes are dependent on the amount of HCI stress that is incurred. The HCI stress in the transistor is dependent on several factors: L_{gate}, V_{ds}, V_{gs}, V_{bs}, and temperature.

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11.2.3.3 Test Methodology

11.2.3.3.1 Measurement Conditions

1. **I_{dsat}** is the forward saturation region drain current with $V_d=V_g=V_{cc}$, $V_s=V_b$=GND.
2. **I_{dlin}** is the forward linear region drain current with $V_d=0.05 \times V_{cc}$, $V_g=V_{cc}$, $V_s=V_b$=GND.
3. **G_m** is the maximum transconductance with V_d=0.1V, $V_s=V_b$=GND.
4. **V_t** is the threshold voltage extrapolated at maximum transconductance.

11.2.3.3.2 Stress Conditions

1. **The core device is stressed at** $V_d=V_g$ < 90% device breakdown voltage; $V_s=V_b$=GND.
2. **The IO device is stressed at a given** given V_d < 90% device breakdown voltage; V_g is at the maximum substrate current for a given V_d; $V_s=V_b$=GND.

11.2.3.3.3 Dimension Ranges of Stress Devices

1. **Channel Length:** 0.05 µm ~ 0.07 µm for core N/PMOS devices,
   0.18 µm ~ 0.315 µm for 1.8V I/O N/PMOS devices,0.26 µm ~ 0.415 µm for 2.5V I/O N/PMOS devices,
2. **Channel Width:** 0.3 µm ~ 10 µm for core N/PMOS devices,
   0.6 µm ~ 10 µm for 1.8/2.5V I/O N/PMOS devices

11.2.3.3.4 Failure Criteria and Spec

The failure criterion for all devices are 10% degradation
Spec= DC 0.2 years, AC/DC factor=50 for core and IO.

11.2.3.3.5 DC Lifetime and Vmax

DC Lifetime definition: 0.1% cum
Criteria: Idsat shift 10%:
N65LP:
1.2V Core (STDVT): NMOS = 0.417yrs @ 1.32V , Vmax of NMOS= 1.353V for W/L=1/0.06, 25℃;
PMOS = 6.84yrs @ 1.32V, Vmax of PMOS= 1.447V for W/L=1/0.06, 125℃
2.5V IO: NMOS = 0.9yrs @ 2.75V; PMOS= 3.22yrs @ 2.75V for W/L=10/0.28, 25℃;

N65G
1.0V Core (STDVT): NMOS = 8.933yrs @ 1.1V , Vmax of NMOS= 1.208V for W/L=1/0.06, 25℃;
PMOS = 93.9yrs @ 1.1V, Vmax of PMOS= 1.283V for W/L=1/0.06, 125℃
1.8V IO: NMOS = 0.2384yrs @ 1.98V; PMOS= 26.4yrs @ 1.98V for W/L=10/0.20, 25℃;

N65GP
1.0V Core (STDVT): NMOS = 6.75yrs @ 1.1V , Vmax of NMOS= 1.195V for W/L=1/0.06, 25℃;
PMOS = 7.45yrs @ 1.1V, Vmax of PMOS= 1.212V for W/L=1/0.06, 125℃
1.8V IO: NMOS = 0.6663yrs @ 1.98V; PMOS= 10.2yrs @ 1.98V for W/L=10/0.20, 25℃

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N55LP:

1.2V Core (STDVT): NMOS = 1.8yrs @ 1.32V for W/L=0.9/0.054, 25℃;
PMOS = 14.1yrs @ 1.32V for W/L=0.9/0.054, 125℃

2.5V IO: NMOS = 0.37yrs @ 2.75V; PMOS= 1.21yrs @ 2.75V for W/L=9/0.252, 25℃;

N55GP

1.0V Core (STDVT): NMOS = 3.05yrs @ 1.1V for W/L=0.9/0.054, 25℃;
PMOS = 11.2yrs @ 1.1V for W/L=0.9/0.054, 125℃

1.8V IO: NMOS = 0.49yrs @ 1.98V; PMOS= 2.9yrs @ 1.98V for W/L=9/0.189, 25℃

11.2.4 Guidelines for Negative Bias Temperature Instability (NBTI)

Negative Bias Temperature Instability (NBTI) is a key reliability item below 65nm technology that is of newer aging issue in p-channel MOS devices stressed with negative gate voltages. The high temperature and bias on Gate terminal will cause significantly NBTI effect, which increase in the threshold voltage and decrease in drain current. It is significant for circuit designers to consider the lifetime degradation ratio of their designs caused by negative bias temperature instability (NBTI) and must be taken into account for burn-in, field operation, and overdrive applications from process variation.

11.2.4.1 Lifetime Prediction Model for Negative Bias Temperature Instability

The lifetime for the negative bias temperature instability (NBTI) is correlated with voltage, temperature, parametric failure criteria, device length, and device width.

$MTTF = A \times f(L, W) \times (I_{dsat}\%)^{1/n} \times \exp[-\gamma x V_g] \times \exp[E_a/k(1/T)]$ **equation (4)**

Where:

L is the drawn channel length (unit: um)

W is the drawn channel width (unit: um)

$\mathbf{I_{dsat}}$ is the criteria of I_{dsat} degradation percentage

n is the power law factor of time dependent degradation

$\mathbf{V_g}$ is the operation gate bias (unit: volt)

γ is the voltage acceleration factor

$\mathbf{E_a}$ is the activation energy

k is the Boltzmann constant ((8.617×10^{-5}) cV/K)

T is the absolute junction temperature (unit:K)

A is a constant

11.2.4.2 Lifetime Prediction Model for AC

For an acceptable specification, the AC lifetime must be considered. Currently, TSMC's proposed standard is an AC-to-DC factor of 2, based on the assumption that the off-state operation occupies half the product's operation time. The accepted AC lifetime is 10 years, with a DC lifetime of 5 years at temperature 125°C.

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11.2.4.3 Failure Mechanism

The PMOS device has a lower mobility than the NMOS device. Mobility for a PMOS device is decreased further, and significantly, by negative bias stress on the transistor gate under a high temperature environment. A hole injected under negative bias into the oxide-substrate interface increases interface states. The electrochemical reaction induces device instability that is enhanced by boron implanted in the gate poly engineering process. Logic circuits could suffer from the driving current decrease, and analog circuits could suffer from the mismatching or shift of threshold voltage.

Negative bias temperature stress under constant voltage (DC) causes the generation of interface trap (NIT) before the gate oxide & Si substrate, which translate to device Vt shift & Ion loss. The NBTI effect is more severe for PMOS than NMOS due to the process of holes in the PMOS inversion layer that are known to interact with oxide state.

11.2.4.4 Test Methodology

11.2.4.4.1 Measurement Condition

I_{dsat} is the saturation region of drain current with $V_d=V_g=V_{cc}$, $V_s=V_b$=GND at a stress temperature.

11.2.4.4.2 Stress Conditions

1. **Sample size** is at least 5 samples for each stress condition.
2. **Voltage range** is 6~ 10MV/cm for core devices and 6 ~ 10 MV/cm for I/O devices.
3. **Temperature range** is 125°C ~ 175°C.
4. **Channel length** is 0.05 um ~ 1.2 um for core devices, 0.18 um ~ 1.2 um for 1.8V I/O devices and 0.26 um ~ 1.2 um for 2.5V I/O devices.
5. **Channel width** is 0.3 um ~ 10 um for core devices and 0.5 um ~ 10 um for 1.8V/2.5V I/O devices.

11.2.4.4.3 Failure Criteria

The failure criterion for NBTI is Idsat 10% degradation.
Spec=DC 5 years, AC/DC factor=2

11.2.4.4.4 DC Lifetime and Vmax

DC Lifetime definition: 0.1% cum

N65LP

a) Criteria: Idsat shift 10%:

1.2V Core (STDV): PMOS = 10.5yrs @ 1.32V for W/L=1/0.06, 125℃
Vmax of PMOS= 1.38V for W/L=1/0.06, 125℃

2.5V IO: PMOS= 298yrs @ 2.75V for W/L=10/0.28, 125℃;
Vmax of PMOS= 3.67V for W/L=10/0.28, 125℃

b) Criteria: Vt shift 50mV

1.2V Core (STDV): PMOS =10.5 yrs @ 1.32V for W/L=1/0.06, 125℃
Vmax of PMOS= 1.38V for W/L=1/0.06, 125℃.

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N65G

a) Criteria: Idsat shift 10%:

1.0V Core (STDV): PMOS = 9.24yrs @ 1.1V for W/L=1/0.06, 125℃
Vmax of PMOS= 1.156V for W/L=1/0.06, 125℃

1.8V IO: PMOS= 23.6yrs @ 1.98V for W/L=10/0.20, 125℃;
Vmax of PMOS= 2.184V for W/L=10/0.20, 125℃

b) Criteria: Vt shift 50mV

1.0V Core (STDV): PMOS =7.66 yrs @ 1.1V for W/L=1/0.06, 125℃
Vmax of PMOS= 1.141V for W/L=1/0.06, 125℃.

N65GP

a) Criteria: Idsat shift 10%:

1.0V Core (STDV): PMOS = 9.6yrs @ 1.1V for W/L=1/0.06, 125℃
Vmax of PMOS= 1.147V for W/L=1/0.06, 125℃

1.8V IO: PMOS= 23.1yrs @ 1.98V for W/L=10/0.20, 125℃;
Vmax of PMOS= 2.17V for W/L=10/0.20, 125℃

b) Criteria: Vt shift 50mV

1.0V Core (STDV): PMOS =9.27 yrs @ 1.1V for W/L=1/0.06, 125℃
Vmax of PMOS= 1.149V for W/L=1/0.06, 125℃.

N55LP

a) Criteria: Idsat shift 10%:

1.2V Core (STDV): PMOS = 29.3yrs @ 1.32V for W/L=0.9/0.054, 125℃

2.5V IO: PMOS= 200yrs @ 2.75V for W/L=9/0.252, 125℃;

b) Criteria: Vt shift 50mV

1.2V Core (STDV): PMOS =29yrs @ 1.32V for W/L=0.9/0.054, 125℃

N55GP

a) Criteria: Idsat shift 10%:

1.0V Core (STDV): PMOS = 8.2yrs @ 1.1V for W/L=0.9/0.054, 125℃

1.8V IO: PMOS= 11yrs @ 1.98V for W/L=9/0.189, 125℃;

b) Criteria: Vt shift 50mV

1.0V Core (STDV): PMOS =6.5 yrs @ 1.1V for W/L=0.9/0.054, 125℃

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11.3 Back-End Process Reliability Rules

11.3.1 Guidelines for Stress Migration(SM)

The Cu vias are frequently subjected to significant stress. The stress frequently causes voids, commonly referred to stress migration (SM) or stress-induced voids (SIV).

11.3.1.1 Failure Mechanism

The stress result from the different coefficient of thermal expansion (CTE) between Cu and the surrounding material will drive micro-vacancy in Cu to diffuse and agglomerate through interfacial surface and grain boundary. Eventually the stressed-induced voids may significantly affect the electrical characteristics and may cause the semiconductor structure to fail.

11.3.1.2 Test Methodology

11.3.1.2.1 Measurement Condition

The measurement is performed under 25°C using wafer-level probing after oven bake. Stress Conditions

1. **Sample size** is >130die(2 wafers) per lot. Totally 3 lots are required.
2. **Temperature range** is 175°C.
3. **Stress time** is 500hr.
4. **Test structures** are:
    i. Vias chain-1 (single via with metal width = min. width under/above via).
    ii. Vias chain-2 (single via with metal width = 0.3um under/above via).
    iii. Vias chain-3 (single via with metal width = 0.42um under/above via).
    iv. Vias chain-4 (dual via with metal width = 0.7um under/above via).
    v. Stacked via chain (single via with metal width = 0.3um under/above via).

11.3.1.2.2 Failure Criteria

1. The failure criterion is resistance >10% shift in terms of wafer-level test.
2. Specification: No failure allowed within 3 lots.

11.3.1.3 SM design rule

Please refer to below rule codes of chapter4.

VIAx.R.2, VIAx.R.3, VIAx.R.4, VIAx.R.5, VIAx.R.6, VIAy.R.2, VIAy.R.3, VIAy.R.4, VIAy.R.5, VIAy.R.6, VIAz.R.2, VIAz.R.3, VIAr.R.2, VIAr.R.3.

11.3.2 Guidelines for Low-k Dielectric Integrity

This section provides information to help you predict LK dielectric reliability and prevent a time dependent dielectric breakdown (TDDB). IMD TDDB is the breakdown of LK dielectric induced by a combination of operation voltage, temperature, and oxide thickness.

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11.3.2.1 Low-k Dielectric Lifetime Prediction Model

TTF (Time to failure) $\propto$ **exp (-**γ**×E_d) × exp (E_a/KT) × (L_{ox})$^{-1/\beta}$**

Where:

L_{ox} is the total metal length in the same metal layer (unit: μm)

T is the absolute operation temperature (unit: K)

E_d is the induced electric field applied to LK dielectric (unit: MVolt/cm)

γ is the field acceleration factor for LK dielectric

E_a is the thermal activation energy

k is the Boltzmann's constant ((8.617×10^{-5}) cV/K)

β is the Weibull shape factor (distribution spread)

11.3.2.2 Failure Mechanism

While the current passed through LK dielectric and formed a conduction path, it would result in LK dielectric breakdown.

The possible failure mechanisms after IMD-TDDB test could be as followings.

1. Dielectric interface breakdown (ie: LK dielectric porosity, ESL integration, Cu ions residue…etc.)
2. Dielectric bulk breakdown (ie: trench barrier formation, LK dielectric porosity…etc.)

11.3.2.3 Test Methodology

11.3.2.3.1 Measurement Conditions

1. **I_g** is the leakage current between metal lines at T=125°C.
2. **E_d** (constant stress field) is set to 2 ~ 4 MV/cm for LK dielectric.

11.3.2.3.2 Stress Conditions

At least 16 samples constitute a sample size for each stress condition:

1. To determine the **field acceleration factor (γ)**, 3 stress voltages are used at each fixed stress temperature.
2. To determine the **thermal activation energy (E_a)**, 3 stress temperatures are used at each fixed stress voltage. Failure Criteria
3. Monitor parameter: **I_g** (leakage current) between metal lines.
4. A DUT is considered as failed if **I_g** (Tbd) > 100 * **I_g** (T0).
5. Specification: 0.1% cumulative DC lifetime at 1.1Vcc > 10 yrs @ 125C.

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11.3.3 DC Cu Metal Current Density (EM) Specifications

This section provides information to evaluate the quality of N65/N55 Cu process and to determine the EM lifetime of metal line, via, stack via, contact under normal operation condition.

11.3.3.1 Electromigration Lifetime Prediction Model

TTF = A x J^(-n) x exp(Ea/kT)

TTF : Time to Failure

A: a constant which contains a factor involving the cross-sectional area of the film

n: exponent of current density (n =1)

J: current density flowing in metal

Ea: activation energy (Ea =0.9eV)

k: Boltzman's constant

T: temperature

11.3.3.2 Failure Mechanism

When a stress current is applied, Cu ions move from cathode to anode under electromigration, vacancy will generate at cathode and it will cause resistance increasing.

11.3.3.3 Test Methodology

11.3.3.3.1 Measurement Conditions

R is the resistance of stress current at high temperature.

11.3.3.3.2 Stress Conditions

1. Sample size is at least 20 samples for each stress condition.
2. Stress temperature: @**300~350**℃
3. Stress current: 1.5 MA/cm^2 based on the cross-section area of metal line.

11.3.3.3.3 Failure Criteria

1. Monitor parameter: **R** (resistance)
2. A DUT is considered as failed if **dR** (Tbd) > 10%* **R0**.
3. Specification: 0.1% cumulative lifetime, 100k hours @ 110C.

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11.3.3.4 Rating factor for Maximum DC Current

I_{max} is the maximum DC current allowed for metal lines, vias, or contacts. I_{max} is based on 0.1% point of measurement data at a 10% resistance increase after 100K hours of continuous operation at 110°C. Use the following table to calculate I_{max} if the junction temperature differs from 110°C.

Table 11.3.1

Temperature	85°C	90°C	95°C	100°C	105°C	110°C	115°C	120°C	125°C
Rating factor of Imax	3.164	2.861	2.512	2.077	1.434	1.000	0.704	0.500	0.358

For example, I_{max} (at 125°C) = 0.358 × I_{max} (at 110°C).

If the junction temperature is below 85°C, please use the rating factor (3.164) at 85°C or contact with TSMC reliability.

11.3.3.5 Maximum DC Current for Metal Lines, Contacts and Vias (T_j = 110°C)

11.3.3.5.1 General

The table provides the maximum allowed DC current, I_{max} for each of the metals, contacts, and vias at junction temperature of 110°C. In the table, *w* (in μm) represents the width of the metal line.

Table 11.3.2

Metal Wiring Level / Interlevel connection	Metal Length, L (μm)	I_{max} (mA)
M1	Any length of metal	1.509 × *(w-0.016)*
Mx	Any length of metal	1.877 × *(w-0.016)*
My	Any length of metal	4.416 × *(w-0.02)*
Mz	Any length of metal	8.096 × *(w-0.02)*
Mr	Any length of metal	11.316 × *(w-0.02)*
Mu	Any length of metal	30.176 × *(w-0.02)*
Contact (size: 0.09x0.09 μm²)	Any length of metal	0.296 per contact
Vx (size : 0.10 × 0.10 μm²)	Any length of metal	0.158 per via
Vy (size : 0.20 × 0.20 μm²)	Any length of metal	0.795 per via
Vz (size : 0.36 × 0.36 μm²)	Any length of metal	3.077 per via
Vr (size : 0.46 × 0.46 μm²)	Any length of metal	5.432 per via
Vu (size : 0.36 × 0.36 μm²)	Any length of metal	3.077 per via

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11.3.3.5.2 Dependence of metal length (length<20μm)

For a metal line length less than 20 μm, an enhancement adjustment factor for the DC current limits of the following table must be obeyed. In this table, the junction temperature is 110°C, and w (in μm) represents the width of the metal line and L (in μm) represents the length of the metal line.

Table 11.3.3

Metal Wiring Level / Interlevel connection	Metal Length, L (μm)	I_{max} (mA)
M1	L ≧ 20	1.509 × (*w-0.016*)
	20 > L >5	(20/L) × 1.509 × (*w-0.016*)
	L ≦ 5	4 × 1.509 × (*w-0.016*)
Mx	L ≧ 20	1.877 × (*w-0.016*)
	20 > L >5	(20/L) × 1.877 × (*w-0.016*)
	L ≦ 5	4 × 1.877 × (*w-0.016*)
My	L ≧ 20	4.416 × (*w-0.02*)
	20 > L >5	(20/L) × 4.416 × (*w-0.02*)
	L ≦ 5	4 × 4.416 × (*w-0.02*)
Mz	L ≧ 20	8.096 × (*w-0.02*)
	20 > L >5	(20/L) × 8.096 × (*w-0.02*)
	L ≦ 5	4 × 8.096 × (*w-0.02*)
Mr	L ≧ 20	11.316 × (*w-0.02*)
	20 > L >5	(20/L) × 11.316 × (*w-0.02*)
	L ≦ 5	4 × 11.316 × (*w-0.02*)
Mu	L ≧ 20	30.176 × (*w-0.02*)
	20 > L >5	(20/L) × 30.176 × (*w-0.02*)
	L ≦ 5	4 × 30.176 × (*w-0.02*)
Vx (size : 0.10 × 0.10 μm^2)	L ≧ 20	0.158 per via
	20 > L >5	(20/L) × 0.158 per via
	L ≦ 5	4 × 0.158 per via
Vy (size : 0.20 × 0.20 μm^2)	L ≧ 20	0.795 per via
	20 > L >5	(20/L) × 0.795 per via
	L ≦ 5	4 × 0.795 per via
Vz (size : 0.36 × 0.36 μm^2)	L ≧ 20	3.077 per via
	20 > L >5	(20/L) × 3.077 per via
	L ≦ 5	4 × 3.077 per via
Vr (size : 0.46 × 0.46 μm^2)	L ≧ 20	5.432 per via
	20 > L >5	(20/L) × 5.432 per via
	L ≦ 5	4 × 5.432 per via
Vu (size : 0.36 × 0.36 μm^2)	L ≧ 20	3.077 per via
	20 > L >5	(20/L) × 3.077 per via
	L ≦ 5	4 × 3.077 per via

Note : Imax for short length rule and Imax of via array/CO array rule can't collateral at the same time

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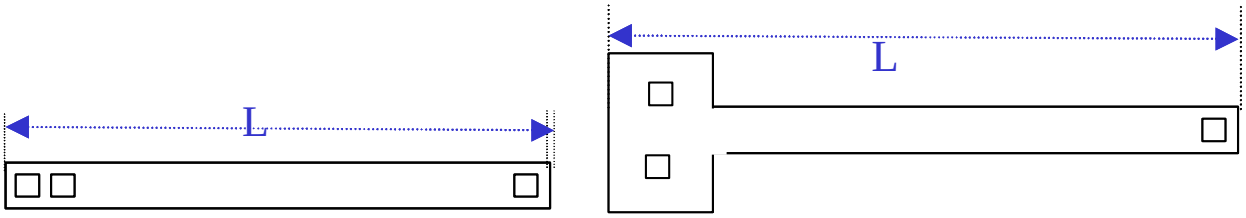
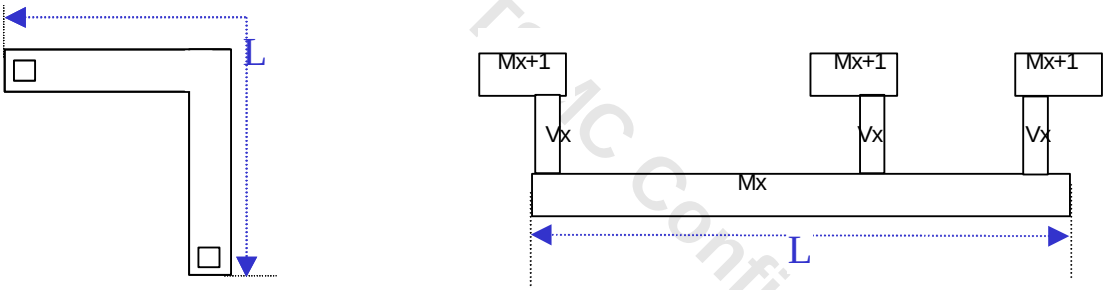
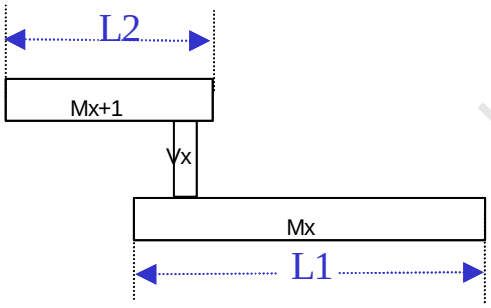
1. Metal Length Definition (L):
   The total length of metal wiring level is from one line-end site to another site line-end site of metal.



2. The higher of the upper_metal and lower_metal Length is used for Via length rule.



If L1 is larger than L2, Imax of via for short length is based on L1.
If L2 is larger than L1, Imax of via for short length is based on L2.



For example : Via1 connect to 10um-length M1 and 5um-length M2.
Imax of M1 = (20/10) x1.509 x (w-0.016)
Imax of M2 = 4x 1.877 x (w-0.016)
Imax of Via1= (20/10) x0.158

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11.3.3.5.3 Stacked Vias

The table provides the maximum allowed DC current, I_{max}, for stacked vias at junction temperature of 110°C.

Table 11.3.4

Interlevel Connection	Imax (mA)	
Vxx	0.158	per stack
Vxy	0.158	per stack
Vxz	0.158	per stack
Vxr	0.158	per stack
Vxu	0.158	per stack
Vxyz	0.158	per stack
Vxzu	0.158	per stack
Vyy	0.795	per stack
Vyz	0.795	per stack
Vzz	3.077	per stack
Vzu	3.077	per stack
Vrr	5.432	per stack

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11.3.3.5.4 Dependence of Via array/Contact array on DC current (T_j = 110℃)

For Via or Contact number exceeding 2 (including 2; Via array or Contact array structure), an adjustment factor for the line, Via and Contact DC current limits of the following table must be obeyed. In this table, the junction temperature is 110°C.

Table 11.3.5

Interlevel connection	Numbers of via	I_{max} (mA)
M1	Single via	1.509 × (*w-0.016)*
	Via array	2 × 1.509 × (*w-0.016)*
Mx	Single via	1.877 × (*w-0.016)*
	Via array	2 × 1.877 × (*w-0.016)*
My	Single via	4.416 × (*w-0.02)*
	Via array	2 × 4.416 × (*w-0.02)*
Mz	Single via	8.096 × (*w-0.02)*
	Via array	2 × 8.096 × (*w-0.02)*
Mr	Single via	11.316 × (*w-0.02)*
	Via array	2 × 11.316 × (*w-0.02)*
Mu	Single via	30.176 × (*w-0.02)*
	Via array	2 × 30.176 × (*w-0.02)*
Contact	Single contact	0.296 per contact
	Contact array	2 × 0.296 per contact
Vx (size : 0.10 × 0.10 μm²)	Single via	0.158 per via
	Via array	2 × 0.158 per via
Vy (size : 0.20 × 0.20 μm²)	Single via	0.795 per via
	Via array	2 × 0.795 per via
Vz (size : 0.36 × 0.36 μm²)	Single via	3.077 per via
	Via array	2 × 3.077 per via
Vr (size : 0.46 × 0.46 μm²)	Single via	5.432 per via
	Via array	2 × 5.432 per via
Vu (size : 0.36 × 0.36 μm²)	Single via	3.077 per via
	Via array	2 × 3.077 per via

Note : Imax for short length rule and Imax of via array/Contact array rule can't collateral at the same time.

1. In this table, Via array/ contact array is defined as via number/ contact number larger than 2 (including 2), including parallel and perpendicular to the direction of current flow via structure.
2. For the use of Via array / contact array structure, the allowable current values equal to the allowable current per via / contact (the above table) times the number of vias/ contacts.

If via size is 0.1umx0.1um, Imax of vias
Type A : Imax of vias (total vias) = 2 x 0.158 x 2 = 0.632 mA
Type B : Imax of vias (total vias) = 2 x 0.158 x 2 = 0.632 mA
Type C : Imax of vias (total vias) = 2 x 0.158 X 15= 4.74 mA

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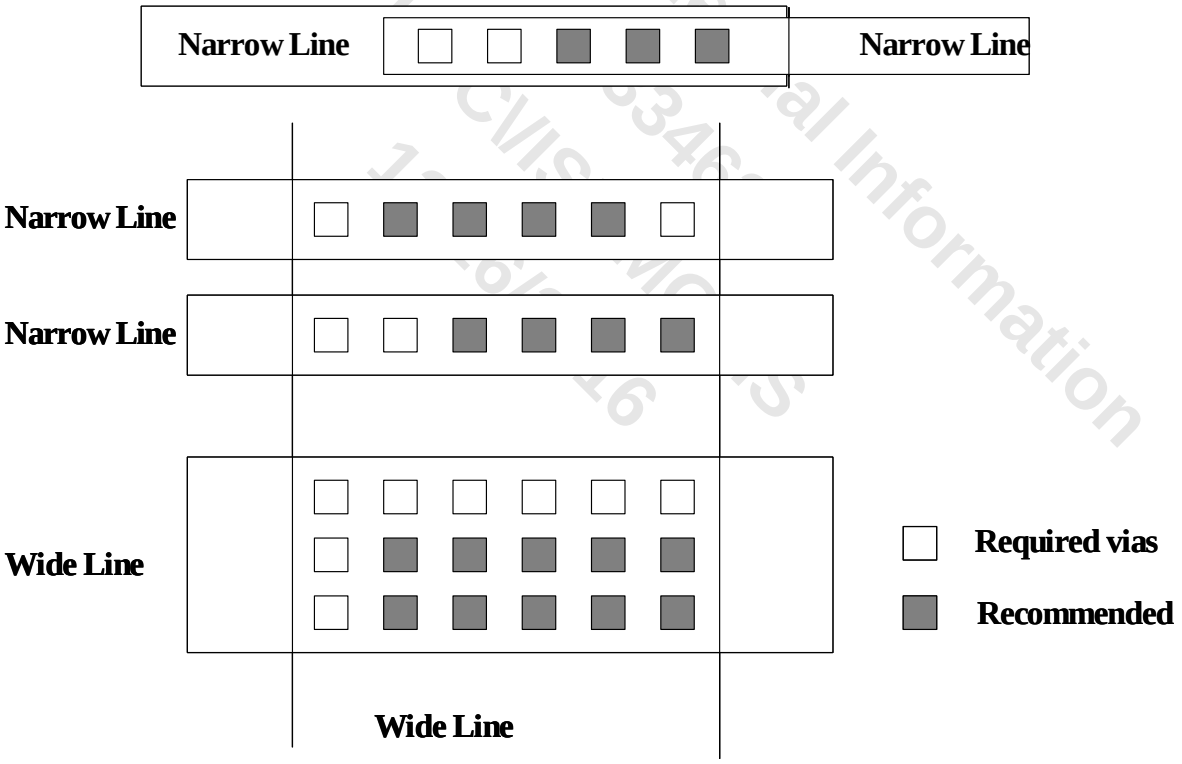
11.3.3.5.5 DC Operation, Required Number of Vias

1. If space permits, it is preferable to have more contacts or vias than the EM rules requie.
2. At a minimum rule, the EM current rules require one via.
   a. Example 1, if M1 is 0.09 μm and the current density is 1.509 mA/μm; that is, the current is 1.509*(0.09-0.016) = 0.112 mA, only one VIA1 is necessary to ensure the reliability margin.
   b. Example 2, if M2 is 0.10 μm and the current density is 1.877 mA/μm; that is, the current is 1.877*(0.10-0.016) = 0.158 mA, only one VIA1 and one VIA2 are necessary to ensure the reliability margin.
3. To determine the required number of vias, please proceed as follow:
   a. From the DC current given in &9.3.3.5, determine the necessary line width (W-line)
   b. Calculate the Maximum allowed Idc_line for the given line width (W-line).
   c. Calculate the required number of contacts or vias to carry line current Idc_line : Number of vias = Idc_line/ Idc_via.
4. Recommended Rule : The number of contacts and vias placed across a line (perpendicular to direction of current flow) must be maximized to increase reliability by providing redundancy in the case of blocked or resistive vias. (increases as much as the line width permits).



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11.3.4 Cu Metal AC Operation

11.3.4.1 Pulsed Signal Terminology

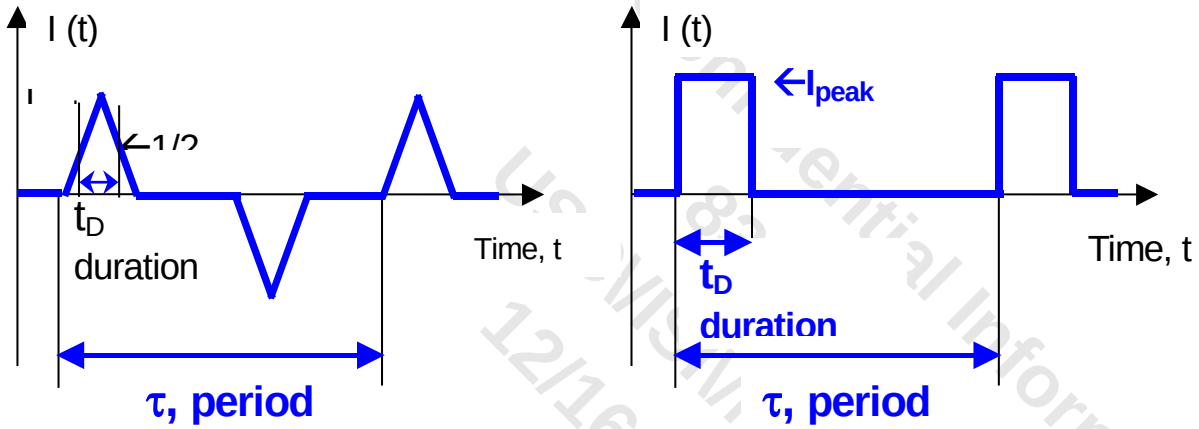
The general terminology for a pulsed DC or AC signal is:

Period (τ)

Duration (t_D)

For your convenience, you could measure the pulse width of I_{peak} at half the peak to define the duration (t_D). The definition of I_{peak} is:

$$I_{peak} = \max\left(\left|I(t)\right|\right)$$



11.3.4.2 Average Value of the Current

I_{avg} is the average value of the current, which is the effective DC current. Therefore, I_{avg} rules are identical to I_{max} rules. Please refer to the DC EM sections. The temperature de-rating table is also applicable to the I_{avg} rule for a junction temperature different from 110°C.

The definition of I_{avg} is:

$$I_{avg} = \left[\left(\int_0^{\tau} I(t)dt\right)/\tau\right]$$

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11.3.4.3 Root-Mean-Square Current

I_{rms} is the root-mean-square of the current through a metal line. The definition of I_{rms} is:

$$I_{rms} = \left[\left(\int_0^{\tau} I(t)^2 dt \right) / \tau \right]^{1/2}$$

The following tables provide the maximum I_{rms} allowed for each of the metal wiring levels at a junction temperature of 110°C. In the table, *w* (in μm) represents the width of the metal line and Δ T (°C) is the temperature rise due to Joule heating.

For M1MxMz combination, please refer to 11.3.4.3.1 and 11.3.4.3.2.

For M1MxMyMz and M1MxMy combinations, please refer to 11.3.4.3.3 and 11.3.4.3.4

For M1MxMy(2XTM) combination, please refer to 11.3.4.3.5 and 11.3.4.3.6

For M1MxMr combination, please refer to 11.3.4.3.7 and 11.3.4.3.8

For M1MxMu combination, please refer to 11.3.4.3.9 and 11.3.4.3.10

11.3.4.3.1 Maximum Root-Mean-Square Currnet for LK Dielectrics (1P9M M1MxMz process, no My)

Table 11.3.6

Metal level	I_{rms} (mA)		
M1	Sqrt [	18.33	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [	6.31	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [	3.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [	2.42	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [	1.85	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [	1.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mx6)	Sqrt [	1.26	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
M8 (Mz1)	Sqrt [	4.37	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M9 (Mz2)	Sqrt [	3.71	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.898) / (w - 0.020 + 0.0443)$]

Table 11.3.7 Example Root-Mean-Square Current for ΔT = 5°C

Metal level	I_{rms} (mA)		
M1	Sqrt [	91.63	$\times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [	31.55	$\times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [	17.50	$\times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [	12.11	$\times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [	9.26	$\times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [	7.49	$\times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mx6)	Sqrt [	6.29	$\times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
M8 (Mz1)	Sqrt [	21.87	$\times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M9 (Mz2)	Sqrt [	18.55	$\times (w - 0.020)^2 \times (w - 0.020 + 2.898) / (w - 0.020 + 0.0443)$]

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11.3.4.3.2 Maximum Root-Mean-Square Current for LK Dielectrics (other metallization options, M1MxMz process, no My)

Table 11.3.6 and 11.3.7 apply to 1P9M process. For other metallization options, please use Irms of M8 and M9 as the first and second Mz, respectively.

For example, 1P7M with M2 ~ M6 as Mx, and M7 as Mz, the Irms rules are:

Table 11.3.8

Metal level	I_{rms} (mA)		
M1	Sqrt [	18.33	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [	6.31	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [	3.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [	2.42	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [	1.85	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [	1.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mz1)	Sqrt [	4.37	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]

Another example, 1P7M with M2 ~ M5 as Mx, M6 and M7 as Mz, the Irms rules are:

Table 11.3.9

Metal level	I_{rms} (mA)		
M1	Sqrt [	18.33	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [	6.31	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [	3.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [	2.42	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [	1.85	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [	4.37	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M7 (Mz1)	Sqrt [	3.71	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.898) / (w - 0.020 + 0.0443)$]

11.3.4.3.3 Maximum Root-Mean-Square Current for LK Dielectrics (1P9M M1MxMyMz process)

Table 11.3.10

Metal level	I_{rms} (mA)		
M1	Sqrt [	18.33	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
Mx1	Sqrt [	6.31	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
Mx2	Sqrt [	3.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
Mx3	Sqrt [	2.42	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
Mx4	Sqrt [	1.85	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
Mx5	Sqrt [	1.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
Mx6	Sqrt [	1.26	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
My1	Sqrt [	2.35	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.546) / (w - 0.020 + 0.0443)$]
My2	Sqrt [	1.84	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 3.250) / (w - 0.020 + 0.0443)$]
Mz1	Sqrt [	2.78	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 3.866) / (w - 0.020 + 0.0443)$]
Mz2	Sqrt [	2.50	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 4.306) / (w - 0.020 + 0.0443)$]

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Table 11.3.11 Example Root-Mean-Square Current for ΔT = 5°C

Metal level	I_{rms} (mA)
M1	Sqrt [$91.63 \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
Mx1	Sqrt [$31.55 \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
Mx2	Sqrt [$17.50 \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
Mx3	Sqrt [$12.11 \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
Mx4	Sqrt [$9.26 \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
Mx5	Sqrt [$7.49 \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
Mx6	Sqrt [$6.29 \times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
My1	Sqrt [$11.73 \times (w - 0.020)^2 \times (w - 0.020 + 2.546) / (w - 0.020 + 0.0443)$]
My2	Sqrt [$9.19 \times (w - 0.020)^2 \times (w - 0.020 + 3.250) / (w - 0.020 + 0.0443)$]
Mz1	Sqrt [$13.90 \times (w - 0.020)^2 \times (w - 0.020 + 3.866) / (w - 0.020 + 0.0443)$]
Mz2	Sqrt [$12.48 \times (w - 0.020)^2 \times (w - 0.020 + 4.306) / (w - 0.020 + 0.0443)$]

If the metal scheme is 1P9M with M1 + 4x2y2z, then use Mx1 ~ Mx4, My1 ~ My2 and Mz1 ~ Mz2.

If the metal scheme is 1P9M with M1 + 5x1y2z, then use Mx1 ~ Mx5, My1 and Mz1 ~ Mz2

If the metal scheme is 1P8M with M1 + 4x2y1z, then use Mx1 ~ Mx4, My1 ~ My2, and Mz1.

11.3.4.3.4 Maximum Root-Mean-Square Current for LK Dielectrics (other metallization options, M1MxMyMz process)

Table 11.3.10 and 11.3.11 apply to 1P9M process. For other metallization options, please use Irms of M8 and M9 as the first and second Mz, respectively. Please refer to the section 2.5 of Metallization Options for allowed metal schemes.

For example, 1P9M with M1 + 4x2y2z (M2 ~ M5 as Mx, M6 ~ M7 as My, and M8 ~ M9 as Mz), the Irms rules are:

Table 11.3.12

Metal level	I_{rms} (mA)
M1	Sqrt [18.33 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [6.31 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [3.50 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [2.42 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [1.85 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (My1)	Sqrt [2.35 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.546) / (w - 0.020 + 0.0443)$]
M7 (My2)	Sqrt [1.84 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 3.250) / (w - 0.020 + 0.0443)$]
M8 (Mz1)	Sqrt [2.78 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 3.866) / (w - 0.020 + 0.0443)$]
M9 (Mz2)	Sqrt [2.50 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 4.306) / (w - 0.020 + 0.0443)$]

Another example, 1P9M with M1 + 5x1y2z (M2 ~ M6 as Mx, M7 as My, and M8 ~ M9 as Mz), the Irms rules are:

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Table 11.3.13

Metal level	I_{rms} (mA)		
M1	Sqrt [	18.33	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [	6.31	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [	3.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [	2.42	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [	1.85	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [	1.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (My1)	Sqrt [	2.35	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.546) / (w - 0.020 + 0.0443)$]
M8 (Mz1)	Sqrt [	2.78	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 3.866) / (w - 0.020 + 0.0443)$]
M9 (Mz2)	Sqrt [	2.50	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 4.306) / (w - 0.020 + 0.0443)$]

One more example, 1P8M with M1 + 4x2y1z (M2 ~ M5 as Mx, M6 ~ M7 as My, and M8 as Mz), the Irms rules are:

Table 11.3.14

Metal level	I_{rms} (mA)		
M1	Sqrt [	18.33	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [	6.31	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [	3.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [	2.42	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [	1.85	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (My1)	Sqrt [	2.35	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.546) / (w - 0.020 + 0.0443)$]
M7 (My2)	Sqrt [	1.84	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 3.250) / (w - 0.020 + 0.0443)$]
M8 (Mz1)	Sqrt [	2.78	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 3.866) / (w - 0.020 + 0.0443)$]

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11.3.4.3.5 Maximum Root-Mean-Square Current for LK Dielectrics (1P9M M1MxMy process, My as 2XTM)

Table 11.3.15

Metal level	I_{rms} (mA)
M1	Sqrt [18.33 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [6.31 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [3.50 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [2.42 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [1.85 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [1.50 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mx6)	Sqrt [1.26 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
M8 (My1)	Sqrt [2.52 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.370) / (w - 0.020 + 0.0443)$]
M9 (My2)	Sqrt [2.29 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.605) / (w - 0.020 + 0.0443)$]

Table 11.3.16 Example Root-Mean-Square Current for $\Delta T = 5°C$

Metal level	I_{rms} (mA)
M1	Sqrt [91.63 $\times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [31.55 $\times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [17.50 $\times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [12.11 $\times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [9.26 $\times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [7.49 $\times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mx6)	Sqrt [6.29 $\times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
M8 (My1)	Sqrt [12.60 $\times (w - 0.020)^2 \times (w - 0.020 + 2.370) / (w - 0.020 + 0.0443)$]
M9 (My2)	Sqrt [11.47 $\times (w - 0.020)^2 \times (w - 0.020 + 2.605) / (w - 0.020 + 0.0443)$]

11.3.4.3.6 Maximum Root-Mean-Square Current for LK Dielectrics (other metallization options, M1MxMy process, My as 2XTM)

Table 11.3.15 and 11.3.16 apply to 1P9M process. For other metallization options, please use Irms of M8 and M9 as the first and second My(2XTM), respectively.

For example, 1P7M with M2 ~ M6 as Mx, and M7 as My(2XTM), the Irms rules are:

Table 11.3.17

Metal level	I_{rms} (mA)
M1	Sqrt [18.33 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [6.31 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [3.50 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [2.42 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [1.85 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [1.50 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (My1)	Sqrt [2.52 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.370) / (w - 0.020 + 0.0443)$]

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Another example, 1P7M with M2 ~ M5 as Mx, M6 and M7 as My(2XTM), the Irms rules are:

Table 11.3.18

Metal level	I_{rms} (mA)
M1	Sqrt [18.33 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [6.31 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [3.50 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [2.42 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [1.85 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (My1)	Sqrt [2.52 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.370) / (w - 0.020 + 0.0443)$]
M7 (My2)	Sqrt [2.29 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.605) / (w - 0.020 + 0.0443)$]

11.3.4.3.7 Maximum Root-Mean-Square Current for LK Dielectrics (1P9M M1MxMr process)

Table 11.3.19

Metal level	I_{rms} (mA)
M1	Sqrt [18.33 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [6.31 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [3.50 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [2.42 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [1.85 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [1.50 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mx6)	Sqrt [1.26 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
M8 (Mr1)	Sqrt [6.07 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M9 (Mr2)	Sqrt [4.98 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 3.001) / (w - 0.020 + 0.0443)$]

Table 11.3.20 Example Root-Mean-Square Current for $\Delta T = 5°C$

Metal level	I_{rms} (mA)
M1	Sqrt [91.63 $\times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [31.55 $\times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [17.50 $\times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [12.11 $\times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [9.26 $\times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [7.49 $\times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mx6)	Sqrt [6.29 $\times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
M8 (Mr1)	Sqrt [30.37 $\times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M9 (Mr2)	Sqrt [24.88 $\times (w - 0.020)^2 \times (w - 0.020 + 3.001) / (w - 0.020 + 0.0443)$]

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11.3.4.3.8 Maximum Root-Mean-Square Current for LK Dielectrics (other metallization options, M1MxMr process)

Table 11.3.19 and 11.3.20 apply to 1P9M process. For other metallization options, please use Irms of M8 and M9 as the first and second Mr, respectively.

For example, 1P7M with M2 ~ M6 as Mx, and M7 as Mr, the Irms rules are:

Table 11.3.21

Metal level	I_{rms} (mA)		
M1	Sqrt [	18.33	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [	6.31	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [	3.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [	2.42	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [	1.85	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [	1.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mr1)	Sqrt [	6.07	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]

Another example, 1P7M with M2 ~ M5 as Mx, M6 and M7 as Mr, the Irms rules are:

Table 11.3.22

Metal level	I_{rms} (mA)		
M1	Sqrt [	18.33	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [	6.31	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [	3.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [	2.42	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [	1.85	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mr1)	Sqrt [	6.07	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M7 (Mr2)	Sqrt [	4.98	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 3.001) / (w - 0.020 + 0.0443)$]

11.3.4.3.9 Maximum Root-Mean-Square Current for LK Dielectrics (1P9M M1MxMzMu process)

Table 11.3.23

Metal level	I_{rms} (mA)		
M1	Sqrt [	18.33	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [	6.31	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [	3.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [	2.42	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [	1.85	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [	1.50	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mx6)	Sqrt [	1.26	$\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
M8 (Mz1)	Sqrt [	4.37	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M9 (Mu)	Sqrt [	13.60	$\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.898) / (w - 0.020 + 0.0443)$]

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Table 11.3.24 Example Root-Mean-Square Current for ΔT = 5°C

Metal level	I_{rms} (mA)
M1	Sqrt [$91.63 \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [$31.55 \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [$17.50 \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [$12.11 \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [$9.26 \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mx5)	Sqrt [$7.49 \times (w - 0.016)^2 \times (w - 0.016 + 1.754) / (w - 0.016 + 0.0443)$]
M7 (Mx6)	Sqrt [$6.29 \times (w - 0.016)^2 \times (w - 0.016 + 2.089) / (w - 0.016 + 0.0443)$]
M8 (Mz1)	Sqrt [$21.85 \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M9 (Mu)	Sqrt [$68.00 \times (w - 0.020)^2 \times (w - 0.020 + 2.898) / (w - 0.020 + 0.0443)$]

If the metal scheme is 1P6M with M1 + 3Mx+Mz+Mu, then useM1, Mx1 ~ Mx3, Mz1 and Mu.

11.3.4.3.10 Maximum Root-Mean-Square Current for LK Dielectrics (other metallization options, M1MxMzMu process)

Table 11.3.23 and 11.3.24 apply to 1P9M process. For other metallization options, please use Irms of M8 as Mz and M9 as Mu.

For example, 1P7M with M2 ~ M5 as Mx, M6 as Mz, and M7 as Mu, the Irms rules are:

Table 11.3.25

Metal level	I_{rms} (mA)
M1	Sqrt [18.33 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [6.31 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [3.50 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [2.42 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [1.85 $\times \Delta T \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mz1)	Sqrt [4.37 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M7 (Mu)	Sqrt [13.60 $\times \Delta T \times (w - 0.020)^2 \times (w - 0.020 + 2.898) / (w - 0.020 + 0.0443)$]

Table 11.3.26 Example Root-Mean-Square Current for ΔT = 5°C

Metal level	I_{rms} (mA)
M1	Sqrt [$91.63 \times (w - 0.016)^2 \times (w - 0.016 + 0.352) / (w - 0.016 + 0.0443)$]
M2 (Mx1)	Sqrt [$31.55 \times (w - 0.016)^2 \times (w - 0.016 + 0.417) / (w - 0.016 + 0.0443)$]
M3 (Mx2)	Sqrt [$17.50 \times (w - 0.016)^2 \times (w - 0.016 + 0.751) / (w - 0.016 + 0.0443)$]
M4 (Mx3)	Sqrt [$12.11 \times (w - 0.016)^2 \times (w - 0.016 + 1.085) / (w - 0.016 + 0.0443)$]
M5 (Mx4)	Sqrt [$9.26 \times (w - 0.016)^2 \times (w - 0.016 + 1.420) / (w - 0.016 + 0.0443)$]
M6 (Mz1)	Sqrt [$21.85 \times (w - 0.020)^2 \times (w - 0.020 + 2.458) / (w - 0.020 + 0.0443)$]
M7 (Mu)	Sqrt [$68.00 \times (w - 0.020)^2 \times (w - 0.020 + 2.898) / (w - 0.020 + 0.0443)$]

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11.3.4.3.11 Maximum Root-Mean-Square Current for LK Dielectrics (1P8M M1MxMu process)

Table 11.3.27

Metal level	I_{rms} (mA)
M1	Sqrt [18.33 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 0.352) / (*w* - 0.016 + 0.0443)]
M2 (Mx1)	Sqrt [6.31 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 0.417) / (*w* - 0.016 + 0.0443)]
M3 (Mx2)	Sqrt [3.50 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 0.751) / (*w* - 0.016 + 0.0443)]
M4 (Mx3)	Sqrt [2.42 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 1.085) / (*w* - 0.016 + 0.0443)]
M5 (Mx4)	Sqrt [1.85 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 1.420) / (*w* - 0.016 + 0.0443)]
M6 (Mx5)	Sqrt [1.50 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 1.754) / (*w* - 0.016 + 0.0443)]
M7 (Mx6)	Sqrt [1.26 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 2.089) / (*w* - 0.016 + 0.0443)]
M8 (Mu)	Sqrt [16.04 × ΔT × (*w* - 0.020)^2 × (*w* - 0.020 + 2.458) / (*w* - 0.020 + 0.0443)]

Table 11.3.28 Example Root-Mean-Square Current for ΔT = 5°C

Metal level	I_{rms} (mA)
M1	Sqrt [91.63 × (*w* – 0.016)^2 × (*w* - 0.016 + 0.352) / (*w* - 0.016 + 0.0443)]
M2 (Mx1)	Sqrt [31.55 × (*w* – 0.016)^2 × (*w* - 0.016 + 0.417) / (*w* - 0.016 + 0.0443)]
M3 (Mx2)	Sqrt [17.50 × (*w* – 0.016)^2 × (*w* - 0.016 + 0.751) / (*w* - 0.016 + 0.0443)]
M4 (Mx3)	Sqrt [12.11 × (*w* – 0.016)^2 × (*w* - 0.016 + 1.085) / (*w* - 0.016 + 0.0443)]
M5 (Mx4)	Sqrt [9.26 × (*w* – 0.016)^2 × (*w* - 0.016 + 1.420) / (*w* - 0.016 + 0.0443)]
M6 (Mx5)	Sqrt [7.49 × (*w* – 0.016)^2 × (*w* - 0.016 + 1.754) / (*w* - 0.016 + 0.0443)]
M7 (Mx6)	Sqrt [6.29 × (*w* – 0.016)^2 × (*w* - 0.016 + 2.089) / (*w* - 0.016 + 0.0443)]
M8 (Mu)	Sqrt [80.2 × (*w* – 0.020)^2 × (*w* - 0.020 + 2.458) / (*w* - 0.020 + 0.0443)]

11.3.4.3.12 Maximum Root-Mean-Square Current for LK Dielectrics (other metallization options, M1MxMu process)

Table 11.3.27 and 11.3.28 apply to 1P8M process. For other metallization options, please use Irms of M8 as Mu.

For example, 1P6M with M2 ~ M5 as Mx, and M6 as Mu, the Irms rules are:

Table 11.3.29

Metal level	I_{rms} (mA)
M1	Sqrt [18.33 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 0.352) / (*w* - 0.016 + 0.0443)]
M2 (Mx1)	Sqrt [6.31 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 0.417) / (*w* - 0.016 + 0.0443)]
M3 (Mx2)	Sqrt [3.50 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 0.751) / (*w* - 0.016 + 0.0443)]
M4 (Mx3)	Sqrt [2.42 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 1.085) / (*w* - 0.016 + 0.0443)]
M5 (Mx4)	Sqrt [1.85 × ΔT × (*w* - 0.016)^2 × (*w* - 0.016 + 1.420) / (*w* - 0.016 + 0.0443)]
M6 (Mu)	Sqrt [16.04 × ΔT × (*w* - 0.020)^2 × (*w* - 0.020 + 2.458) / (*w* - 0.020 + 0.0443)]

Table 11.3.30 Example Root-Mean-Square Current for ΔT = 5°C

Metal level	I_{rms} (mA)
M1	Sqrt [91.63 × (*w* – 0.016)^2 × (*w* - 0.016 + 0.352) / (*w* - 0.016 + 0.0443)]
M2 (Mx1)	Sqrt [31.55 × (*w* – 0.016)^2 × (*w* - 0.016 + 0.417) / (*w* - 0.016 + 0.0443)]
M3 (Mx2)	Sqrt [17.50 × (*w* – 0.016)^2 × (*w* - 0.016 + 0.751) / (*w* - 0.016 + 0.0443)]
M4 (Mx3)	Sqrt [12.11 × (*w* – 0.016)^2 × (*w* - 0.016 + 1.085) / (*w* - 0.016 + 0.0443)]
M5 (Mx4)	Sqrt [9.26 × (*w* – 0.016)^2 × (*w* - 0.016 + 1.420) / (*w* - 0.016 + 0.0443)]
M6 (Mu)	Sqrt [80.2 × (*w* – 0.020)^2 × (*w* - 0.020 + 2.458) / (*w* - 0.020 + 0.0443)]

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11.3.4.4 Peak Current

I_{peak} = max (| I (t) |)

I_{peak} is the current at which a metal line undergoes excessive Joule heating and can begin to melt. This current should be used infrequently.

The limit for the peak current, I_{peak}, can be calculated by using the following formula:

$$I_{peak} = \frac{I_{peak_DC}}{\sqrt{r}}$$

r is the duty ratio, which is equal to the pulse duration divided by the period,

$$r = \frac{t_D}{\tau}$$

where I_{peak_DC} is provided in the following table. In the table, w (in μm) represents the width of the metal line.

Note : the above equation is only applicable for frequency larger than 1 MHz and *r* larger than 0.05.

Table 11.3.31

Metal Level	Ipeak_DC (mA)
M1	36.0 × (*w*-0.016)
Mx	22.0 × (*w*-0.016)
My	35.0 × (*w*-0.020)
Mz	63.0 × (*w*-0.020)
Mr	87.5 × (*w*-0.020)
Mu	99.0 × (*w*-0.020)

The I_{peak} rule applies to the periodic AC or pulsed DC signals.

For a single event high current pulse or signals which cannot be specified by duty ratio, please follow the ESD guidelines in Chapter 10.

The I_{peak} rules provided in this section are applicable to signals with a pulse width (t_D) of less than 1μsec. No temperature adjustment factor for the I_{rms} and I_{peak} is given.

The I_{rms} and I_{peak} of contacts and vias do not include because the heating in contacts and vias is negligible and is usually determined by metal or substrate. If the metal width is increased to some extent and only one via is used in that metal, then the heating in the via cannot be considered negligible. However, if the design follows the SM rules, via heating can be negligible. Please follow the VIAx.R.2~VIAx.R.6, VIAy.R2~VIAy.R6, VIAz.R.2~VIAz.R.3, and VIAr.R.2~VIAr.R.3 rules to make sure that the via heating is not a problem.

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11.3.5 AP RDL Current Density (EM) Specification

11.3.5.1 Maximum DC Current

Jmax is maximum DC current allowed per um of AP RDL metal line width or per CB via. The number is based on 0.1% point of measurement data at 10% resistance increase after 100K hours of continuous operation at 110°C. Use the following table to calculate I_{max} if the junction temperature differs from 110°C.

Table 11.3.32

Temperature	85°C	90°C	95°C	100°C	105°C	110°C	115°C	120°C	125°C
Rating factor of Imax	1.800	1.623	1.466	1.329	1.151	1.000	0.872	0.764	0.671

For example, J_{max} (at 125°C) = 0.671 × J_{max} (at 110°C)

If the junction temperature is below 85°C, please use the rating factor (1.800) at 85°C or contact with TSMC reliability.

11.3.5.2 Maximum DC Current for AP RDL Metal (AP RDL) Lines (Tj = 110°C)

The table provides the maximum allowed DC current, I_{max} for each of the metal wiring levels at junction temperature of 110°C. In the table, *w* (in μm) represents the width of the metal line.

Table 11.3.33

Metal Wiring Level	Imax (mA)		RDL Thickness
AP RDL	2.7	× *w*	14.5K Å
AP RDL	5.21	× *w*	28K Å

11.3.5.3 Maximum DC Current for AP RDL (RV) Vias (Tj = 110°C)

The table provides the maximum allowed DC current, I_{max} for each of the contact and via at junction temperature of 110°C. In the table, the sizes of contact and via are also noted.

Table 11.3.34

Interlevel Connection	Imax (mA)		Size
RV	7	per RV	3 × 3 μm^2

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11.3.6 N65/N55 AP RDL AC Operation

The general terminology for AlCu RDL is the same as Cu interconnects.

The following table provides the maximum I_{rms} allowed for AlCu RDL at a junction temperature of 110°C. In the table, *w* (in µm) represents the width of the RDL line and Δ T (°C) is the temperature rise due to Joule heating.

Table 11.3.35

Metal level	Irms (mA)	RDL Thickness
AP RDL	Sqrt [2.62 × Δ T × *w* × (*w* + 3.397)]	14.5K Å
AP RDL	Sqrt [5.06 × Δ T × *w* × (*w* + 3.397)]	28K Å

The I_{peak} rule for AP RDL is 58 mA/um for RDL thickness = 14.5 KA.

The I_{peak} rule for AP RDL is 112 mA/um for RDL thickness = 28.0 KA.

11.3.7 Poly Current Density Specifications

The maximum current density for poly resistor (unsilicided) is 0.5 mA/µm at a junction temperature of 110°C. This density is calculated using 0.1% point of measurement data at a 5% resistance increase after 100K hours of continuous operation.

Use the following table to calculate I_{max} if the junction temperature differs from 110°C. For a junction temperature below 105°C, use the rule at 105°C.

Table 11.3.36

Junction temperature	105°C	110°C	125°C
Rating factor of Jmax	1.03	1.00	0.927

For example, I_{max} (at 125°C) = 0.927 × I_{max} (at 110°C).

This rule is applicable to N+, and P+ unsilicided poly resistors.

For silicided poly, the maximum DC current density is 6mA/um at a junction temperature of 110°C. This density is calculated using 0.1% point of measurement data at a 5% resistance increase after 100K hours of continuous operation.

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11.3.8 N65 Poly EM Joule heating Guidelines

11.3.8.1 Root-Mean-Square Current (Irms)

The following table(1.1.1.1) provides the root-mean-square current (I_{rms}) for poly. In this table, Wp (in μm) represents the drawn width of poly line and ∆ T (°C) is the temperature rise due to Joule heating effect.

Table 11.3.8.1.1 Wp: poly drawn width

poly	Root-Mean-Square current (mA)
unsilicided	Sqrt [0.003709 x ∆T x Wp x (Wp + 1.02)]
silicided	Sqrt [0.187 x ∆T x Wp x (Wp + 1.713)]

Table 11.3.8.1.2 Example for the relationships of Irms (mA), poly width(μm) and joule heating effect(ΔT)

Irms for unsilicided poly (mA), Sqrt [0.003709 x △T x Wp x (Wp + 1.02)]						
Poly width (μm)	ΔT=10 ℃	ΔT=20 ℃	ΔT=30 ℃	ΔT=40 ℃	ΔT=50 ℃	ΔT=60 ℃
0.5	0.168	0.237	0.291	0.336	0.375	0.411
1.0	0.274	0.387	0.474	0.547	0.612	0.670
2.0	0.473	0.669	0.820	0.947	1.058	1.159

Irms for silicided poly (mA), Sqrt [0.187 x △T x Wp x (Wp + 1.713)]						
Poly width (μm)	ΔT=10 ℃	ΔT=20 ℃	ΔT=30 ℃	ΔT=40 ℃	ΔT=50 ℃	ΔT=60 ℃
0.5	1.438	2.034	2.491	2.877	3.216	3.523
1.0	2.252	3.185	3.901	4.505	5.037	5.517
2.0	3.726	5.270	6.454	7.453	8.333	9.128

11.3.8.2 Ipeak

The following table(11.3.8.2.1) provides the maximum Ipeak allowed for poly, In the table, Wp (in μm) represents the drawn width of poly line.

Table 11.3.8.2.1

poly	I_{peak} (mA)
unsilicided	1.875 * Wp
silicided	9.36 * Wp

11.3.9 OD Current Density Specifications

For diffusion (OD) unsilicided resistors and/or silicided interconnect, no I_{max} rule is given. Since diffusion (OD) is crystalline silicon with implantation, no electromigration or Joule heating problems occur. If the design follows contact, metal, and via current density rules, there will be no reliability concern for diffusion (OD).

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11.4 Product Early Failure Rate Screening Guidelines

The guidelines in this section can help you to improve product Early Failure Rate (EFR) either in wafer level or package level. Dynamic Voltage Stress (DVS) testing or low noise margin (LNM) testing methods at the wafer level could be applied for AlCu and pure Cu processes.

11.4.1 Wafer Level Screening

TSMC's wafer level screening methodology includes DVS stress and LNM methods.

11.4.1.1 Wafer-Level Screening - DVS

TSMC recommend you to check the following items before DVS screening:

1. DVS stress voltage cannot apply on circuitry with voltage regulator to avoid unnecessary damage.
2. DVS stress voltage cannot apply on analog circuitry.
3. Try to avoid spiking noise signal during DVS stress.

11.4.1.1.1 Stress Voltaeg Setting

Schmoo plot verification prior to formal stress is recommended for stress voltage settings. You should avoid introducing any artificial damage (for example, latch-up, EOS, localized over-stress, and so on).

After the stress test, it is recommended that the you verify the correlation between product burn-in result and wafer level screening data.

11.4.1.1.2 Stress Time

A stress duration of 500 ms to 1000 ms has proven to be effective. You needs to compare that effectiveness against the costs of testing before finalizing the stress time.

11.4.1.1.3 Screening Criteria

You can choose any one of the following criteria. The following criteria should correlate to package level burn in failure rate and define the acceptance specification.

1. **Tightened I_{sb}**: Defined by the I_{sb} cumulated distribution plot from production lots.
2. **Delta I_{sb}**: Defined by the delta I_{sb} cumulated distribution plot
3. **Low voltage or high frequency functionality test:** Defined by V_{ccmin} or scan like test

11.4.1.2 Wafer-Level Screening - LNM

It has been demonstrated that devices with low noise margins (LNM) are reliably weaker parts. Reliably weaker parts can be identified successfully by comparing CP sort bin (speed, data retention, and V_{ccmin}) degradation between the ambient temperature and the high temperature (HT).

TSMC recommend you to check the following items before LNM screening:

1. Be sure of I_{sb} or I_{ddq} current specifications available at high temperature.
2. Be sure of product can be operated at a high temperature and have toggle test pattern.
3. Be sure of speed index or V_{ddmin} datalog could be extracted as a reliability assessment parameter.
4. Be sure of testing hardware setup like probe card and tester environment were stable and reliable for high temperature testing.

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11.4.1.2.1 HT Temperature Setting

HT screening without artificial damage greatly depends on the product design windows or margins at HT. These windows or margins need to be checked by wafer sorting

11.4.1.2.2 Stress Duration

A temperature of 85°C can increase device gate leakage (I_g) by 8% ~ 10% and, thus, narrow down the noise margin. You need to judge the reliability requirements and design a balanced test regime that avoids unnecessary over-stress to the product. Please consult TSMC before implementing this method.

11.4.1.2.3 Screening Criteria

1. **Tightened V_{ddmin}**: The tailing parts in a V_{ddmin} distribution are dice with the lowest LNM. A tight V_{ddmin} specification is defined by the V_{ddmin} distribution plot of the production lots. STD+3 sigma is recommended.
2. **Delta speed**: A delta of speed is defined by the delta speed distribution plot of the production lots.
3. **Functional test screening**: High temperature narrows the noise margin. Thus, the function test at HT directly screens out dice with the LNM.

11.4.2 Package-Level Screening – Product Burn-In

Recommendations:

1. **Voltage**: 1.4 × V_{cc} to core; 1.1 × V_{cc} to I/O and V_{ih}.
2. **Temperature**: Depends on the product transistor counts and burn-in patterns design. To avoid thermal run away, you should estimates the whole chip leakage by using a specific burn in pattern and check the thermal resistance of package material before setting this temperature.
3. **Pattern**: ATPG (Automatic Test Pattern Generation) or the scan pattern with the highest transistor coverage is recommended.
4. **Duration**: Less than 6 hours or judging from bathtub curve to meet specific product early failure rate criteria.

11.4.3 Soft Error Rate

TSMC follows JEDEC's JESD89 in the domain of SER. So the definition, test methodology, FIT calculation and so on will follow the description in JESD89.

Introduction

Soft errors are nondestructive functional errors induced by energetic ion strikes. Soft errors are a subset of single event effects (SEE), and include single-event upsets (SEU), multiple-bit upsets (MBU), single-event functional interrupts (SEFI), single-event transients (SET) that, if latched, become SEU, and single-event latch-up (SEL) where the formation of parasitic bipolar action in CMOS wells induce a low-impedance path between power and ground, producing a high current condition (SEL can also cause latent and hard errors).

In general, soft errors may be induced by alpha particles emitted from radioactive impurities in materials nearby the sensitive volume, such as packaging, solder bumps, etc., and by highly ionizing secondary particles produced from the reaction of both thermal and high-energy terrestrial neutrons with component materials.

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There are two fundamental methods to determine a product's SER. One is to test a large number of actual production devices for a long enough period of time (weeks or months) until enough soft errors have been accumulated to give a reasonably confident estimate of the SER. This is generally referred to as a real-time or unaccelerated SER testing. Real-time testing has the advantage of being a direct measurement of the actual product SER requiring no extrapolation, assumptions, or special experimental structures, equipment, etc. (provided the test is performed in a building location similar to the actual use environment). However, Real-time testing requires expensive systems monitoring hundreds or thousands of devices in parallel, for long periods of time.

The other method commonly employed to allow more rapid SER estimations and to clarify the source of errors is accelerated-SER (ASER) testing. In ASER testing, devices are exposed to a specific radiation source whose intensity is much higher than the ambient levels of radiation the device would normally encounter. ASER allows useful data to be obtained in a fraction of the time required by real-time, unaccelerated real-time testing. Only a few units are needed and complete evaluations can often be done in a few hours or days instead of weeks or months. The disadvantages of ASER are that the results must be extrapolated to use conditions and that several different radiation sources must be used to ensure that the estimation accounts for soft errors induced by both alpha particle and cosmic-ray-neutron events.

TSMC's soft errors measurement, including alpha and neutron, are ASER that follows JEDEC Standard (JESD89).

11.4.3.1 Alpha SER

Introduction

Uranium and thorium impurities found in trace amounts in the various production and packaging materials emit alpha particles. Alpha particles are strongly ionizing, so those that impinge on the active device create bursts of free electron-hole pairs in the silicon. This charge disruption can be collected at pn junctions (much like charge created by light), producing a current spike (noise pulse) in the circuit. These current spikes can be large enough to alter the data state on some circuits. The alpha flux is independent of altitude, and is only a function of the type, location, and amount radioactive impurities present in the component or its package.

11.4.3.1.1 Alpha Source

Different types of alpha sources can be used to simulate the alpha emission from uranium and thorium impurities. Here is the information of the alpha source used in TSMC.

Source : ^{241}Am

Energy : 5.4MeV

Activity : 3722.2 Bq (=0.1006uCi)

Area : 1320.25 mm^2

Alpha particle source Flux : 2.819/mm^2-sec (= Activity / Area)

Packaged component alpha Flux : 27.8E-10 /mm^2-sec or 0.001 c/cm^2-h

G factor : Calculated from the die size and DUT-to-alpha source space.

Acceleration factor : G * (Alpha particle source Flux / Packaged component alpha Flux)

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11.4.3.1.2 Test Condition

11.4.3.1.2.1 Packaging for alpha particle testing

Unlike real-time and accelerated neutron and proton test methods where the package type is not critical, for accelerated alpha particle testing the DUT's surface must be directly exposed to the isotope source without any intervening solid material and with a minimal air gap.

Recommended DUT package types are the ceramic dual-in-line (CERDIP) or pin-grid array (CERPGA) package. Certainly, other package types that offer access to the top surface of the chip can also be used but these types in particular are mechanically robust particularly when used with zero-insertion force (ZIF) sockets allowing reliable loading and unloading over many cycles.

The die should be mounted and wirebonded within the well or cavity such that the surface of the die is as close as possible to the top surface of the package without anything, such as the bond wires, projecting above this plane. This configuration is required to minimize the alpha source-to-die spacing, while providing a convenient indexing surface for the isotope source. The metal lid for the package should be installed with tape to protect the DUT between tests.

f the product to be tested is already encapsulated in a plastic package, the material over the die must be etched back to fully expose the active area. If the manufacturer's packaging includes an alpha shielding layer, typically polyimide, over the surface of the die, this must be left in place at full thickness for accurate testing. In this case it is best to have unpackaged, but coated, samples of the DUT provided by the manufacturer for alpha testing, rather than attempting to etch back the existing packaging material. Lead-over-chip (LOC) packages are not suitable since the lead frame shadows a large portion of the device. FC packages with solder bumps distributed over the face of the die are also not suitable for the same reason.

11.4.3.1.2.2 Test pattern

The basic test pattern for all memory circuits is a logical checkerboard, alternating by address and bit. If detailed layout information for the DUT is available, a physical checkerboard is also useful. A determination of the best test pattern is left to the discretion of the tester, but must be documented in the test report.

The use of physical data patterns, i.e. patterns that are related to the actual layout of the DUT, rather than the logical addressing are recommended where possible. These patterns may provide insight into the ionizing radiation sensitivity of the DUT. Because layout information is generally proprietary only DUT manufacturers would generally be expected to be able to meet this recommendation.

Some devices, particularly dynamic RAMs (DRAMS) and logic elements often have a "preferred" soft-error failure, either 0 → 1 or 1 → 0. The selected test pattern must consider this possibility in its design. For testing when there is no a priori knowledge of the device the test pattern should balance the number of 0's and 1's. If the relative failure rates are known, perhaps from previous test experience, the test pattern can be adjusted to improve statistics of the less likely transition. The use of an unbalanced test pattern must be described fully in the final report and data analysis.

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11.4.3.1.3 FIT Calculation

To determine the actual field product failure rate from soft errors requires extrapolating the accelerated test results to the nominal use conditions. The product SER under normal use conditions can be obtained by multiplying the observed SER (rate of soft errors) during the accelerated testing by the ratio of the alpha particle flux reaching the DUT active device area under normal use conditions and the alpha flux reaching the DUT active device areas during the test according to the following equation.

$$Unaccelerated\ Alpha\ Particle\ SER = \frac{ASER}{Acceleration_factor}$$

Where ASER is the soft error rate obtained from the DUT during accelerated testing, and Acceleration_factor is calculated in the section of 11.4.3.1.1. As mentioned earlier, since the accelerated source uses an alpha particle source with a flux that is significantly higher than the nominal package environment, this Acceleration_factor is in the range of 10^5 to 10^{14} and consequently the unaccelerated SER will be significantly lower than the ASER observed during accelerated testing. This equation and method is not part of the actual requirement However, all alpha particle SER data must include a description of the assumption made for geometry factor along with all experimental parameters (e.g. source size, DUT active area, source-to-DUT spacing, etc.) that would enable an outside observer to verify that the assumptions used were valid.

Finally, it is not uncommon to use dedicated test structures instead of the final product during accelerated testing. This is particularly true if in cases where a technology's alpha-particle SER sensitivity is being determined prior to actual qualified production. It is recommended that alpha testing of at least a few actual production components be done following test chip data to ensure that the test chip used is representative of the SER sensitivity in actual products.

11.4.3.2 Cosmic (Neutron) SER

Introduction

Terrestrial cosmic rays, at sea level up to moderate altitudes, are dominated by neutrons, with some contributions from other particles like protons and pions. Neutrons interact with Si and other nuclei via strong nuclear interactions. These processes produce a variety of secondary particles - protons, neutrons, alpha particles and heavy recoil nuclei. Some of these secondary particles are strongly ionizing, so those that impinge on the active device create bursts of free electron-hole pairs in the silicon. This charge disruption can be collected at pn junctions (much like charge created by light), producing a current spike (noise pulse) in the circuit. These current spikes can be large enough to alter the data state on some circuits. This section deals with the method of determining a component's sensitivity to high-energy neutron events from accelerated experiments.

This section deals strictly with SER induced by high-energy neutron events. The high energy neutron flux is dependent on altitude, latitude, and solar activity

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11.4.3.2.1 Neutron Beam Selection

A spallation neutron source, such as the ICE House (formerly known as the Weapons Neutron Research, WNR) facility at the Los Alamos National or the TRIUMF Neutron Facility allows one to measure the SEU rate and derive an *averaged* SEU cross section. Because the neutrons produced from a spallation source cover a wide energy spectrum, the user cannot extract a SEU cross section at a specific energy from such measurements, but rather obtains the contribution of SEU events from neutrons of all energies within the spectrum. The major reason that a spallation neutron source is widely used is that the shape of the energy spectrum from this beam is similar to the spectrum of the terrestrial neutrons on the ground. In Figure 9-1, we compare the neutron spectra from the beams at Los Alamos and TRIUMF with the scaled neutron spectrum at ground level.

The ICE House spectrum in Figure 9-1 is at the location of the LANL fission detector, which was at a point 19.97 meters down the flight path from the tungsten target. DUTs are located further down the flight path, so that the neutron flux will be reduced by the following ratio $r^2/(r+d)^2$, where r is the distance to the detector (19.97 m in this case) and d is the distance between the detector and the DUT. At TRIUMF the spectrum in Figure 9-1 also applies at the location of the DUT so no correction needs to be made.

When testing with a spallation neutron source, the SEUs recorded will be due primarily to the high energy (e.g. > 10 MeV) neutrons. The SEU contribution of the neutrons in the 1<E< 10 MeV range is small, < 10%, but these neutrons comprise ~40% of all neutrons > 1 MeV in the terrestrial spectrum (as can be seen in Fig. 11.4.1). Further, if a spallation neutron source is used that contains thermal neutrons, which is not true at Los Alamos, care must be taken to subtract out the SEUs that are caused by the thermal neutrons.

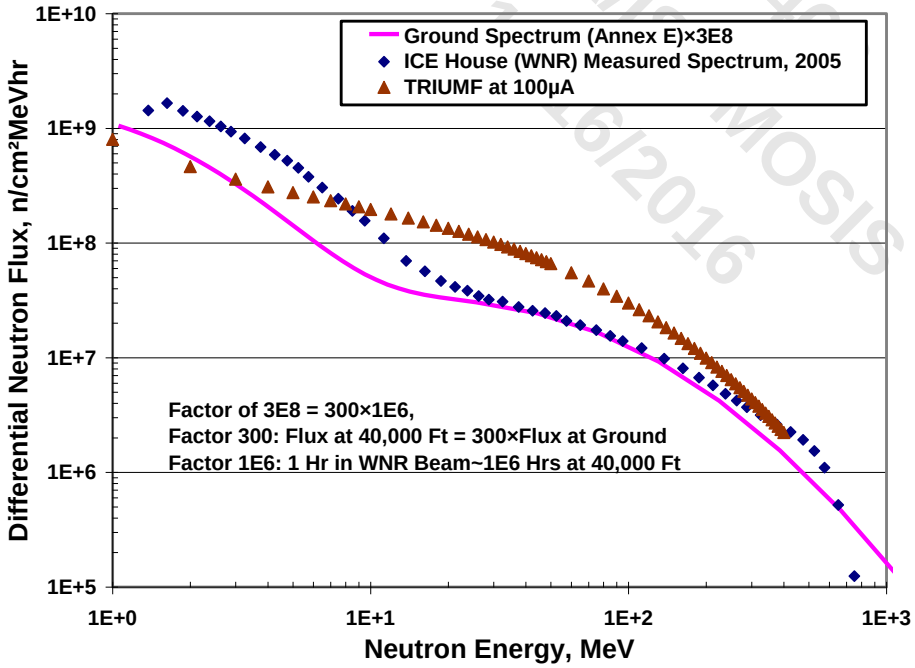

Figure 11.4.1: Comparison of Los Alamos and TRIUMF neutron beam spectra with terrestrial neutron spectrum

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11.4.3.2.2 Basic Test Methodology

The basic test methodology for memory arrays is storing a known data pattern in the array while the part is exposed to the accelerated beam and comparing the stored pattern that is present after the device has been irradiated. At some time during and/or after the exposure, the data is evaluated to identify the number of changes in the pattern as errors. Other circuits may have different tester requirements.

11.4.3.2.3 FIT Calculation

11.4.3.2.3.1 Cross-section and FIT calculation

The cross-section defines the sensitivity of a device. The cross-section per bit is defined as σ=N/(F*C) where N is the total number of errors, F is the fluence and C is the number of bits of the tested memory. In this document the cross-section is given in cm²/bit.

Since the WNR neutron beam has a neutron energy spectrum very similar to that of the terrestrial neutron energy spectrum, the cross-section per bit obtained at WNR can be used directly to estimate the terrestrial failure rate.

According to the JEDEC specification, the FIT rate is calculated using the value of neutron flux for New-York City, f_{NYC} =14 n/cm^2/hour for neutrons with energy above 10 MeV. The FIT is calculated in TSMC's report for a memory capacity of 1 Mbit. Thus, FIT is given by the following formula:

$FIT=\sigma*f_{NYC}*10^9*2^{20}$ (errors / 10^9 hour / 1 Mbit)

Where σ is the cross-section per bit given in cm²/bit, and f_{NYC} is the flux given in n/cm^2/hour.

The FIT is calculated using the neutron flux for New-York City, and for a memory capacity of 1 Mbit. The neutron flux depends on the altitude and location.

11.4.3.2.3.2 Accuracy of Result

The accuracy of the measured cross-section is the sum of the following components:

The error rate is generally described by a Poisson distribution, cf. appendix C.1 of JEDEC. The standard deviation depends on the number of errors observed. If N errors occur, the standard deviation is $\sqrt{N}$. Thus the cross-section accuracy is $1/\sqrt{N}$.

There are cases of interest where small numbers of events are observed (including the case where no events occur). The cross section can be bounded for such cases using the upper and lower counting events in the table below, extracted from appendix C.2 of JEDEC. In using this table, the first column is the actual number of events observed in the experiment. The upper and lower limits show how high (or low) the number of events could actually be if the experiment were continued for much longer time periods.

Accuracy of the fluence measurement for each run. This accuracy is better than 3% for the WNR facility.

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	95% confidence limit	
Events	Lower limit	Upper limit
0	0.0	3.7
1	0.1	5.6
2	0.2	7.2
3	0.6	8.8
4	1.0	10.2
5	1.6	11.7
6	2.2	13.1
7	2.8	14.4
8	3.4	15.8
9	4.0	17.1
10	4.7	18.4
20	12.2	30.9
50	37.1	65.9
100	81.4	121.6

11.4.3.3 Suggestion to Improve SER

11.4.3.3.1 SER Mitigation Options

Many papers discussed about SER mitigation options and some are experimented in TSMC. Here lists the SER mitigation options that have been published.

Error Correction Codes: By far, the most effective method of dealing with soft errors in memory components is by employing additional circuitry for error detection and/or correction. Typically, error correction is achieved by adding extra bits to each data vector encoding the data so that the “information distance” between any two possible data vectors is, at least, three. Lager information distances can be achieved with more parity bits and additional circuitry – but in general, the single error correctin double error detection (SECDED) schemes are favored. In these systems, if a single error occurs (a change of plus or minus one in information space), there is no chance that the corrupted vector will be mistaken for its nearest neighbors (since the information distance is three). In fact, if two errors occur in the same “correction word”, a valid error vector will still be produced. The only limitation is that with two errors the error vector will not be unique to a single data value, thus only detection of double-bit errors is supported. There are two suggestions to make the ECC more reliable. First, scramble and interleaving must be taken into consideration. Physical adjacent bits should not map to the same logic word. Second, memory scrubbing can correct latent errors before they build up to cause uncorrectable errors. The combination of ECC and scrubbing gives a very high-reliable framework only area penalty must be concerned.

Reduction of Alpha –Particle Upset: The effect of alpha-particle-induced upset in semiconductors has been know for over two decades due to trace contamination of Thorium and Uranium in the chip packaging materials and lead in the solder and flip-chip bumps. Unlike neutrons, the amount of alpha particles can be: 1) controlled by the process technology and 2) shielded from the sensitive areas of the chip. Low alpha particle mold compounds and thick polyimide coatings(>15 μm) are used to shield the chip from package-induced alpha particles. For flip-chip-mounted devices, “keep-out” designs are used where the sensitive memory arrays are maintained at a sufficient distance so that alpha particles generated from the lead bumps must traverse large angles through the top layers (and therefore, significant material thickness) before they arrive at the sensitive volume of the circuit. Low alpha count lead can also be used, but but there is a significant increase in material cost for this isotopic purity.

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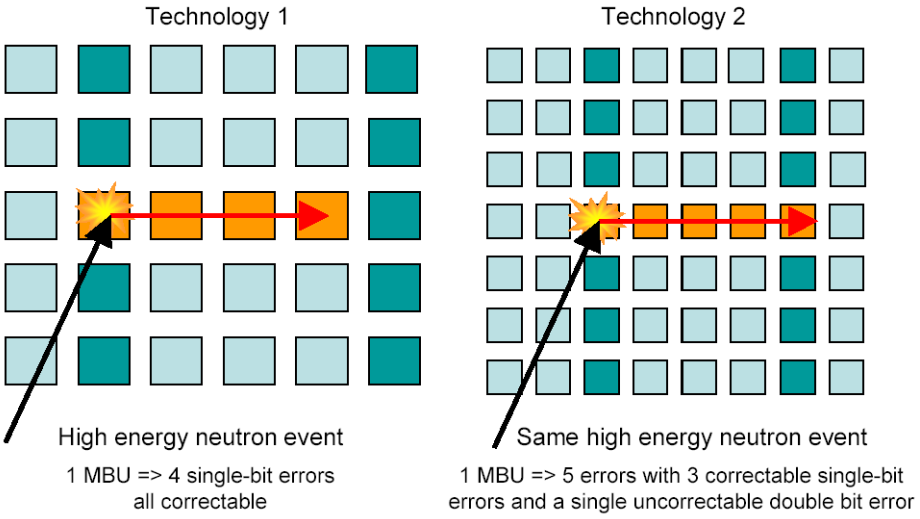
Elimination of Borophosphosilicate Glass (BPSG): BPSG is used as a planarization and gettering layer immediately about the transistors. However, the ^{10}B isotope has a large capture cross section for thermal neutrons, which leads to energetic fission byproducts (a ^{7}Li recoil, an alpha particle, and a gamma ray) and increased SERs. The development of chemmechanicl polishing (CMP) techniques for planarization in deep submicrometer designs have largely replaced the need for BPSG in logic and SRAM processes, so SER due to thermal neutrons can be eliminated.

Added SRAM Capacitance: Addition of a metal-insulator-metal (MIM) node capacitor can reduce the SRAM cell-upset rate from high-energy neutrons by roughly an order of magnitude, but not eliminate cell upset altogether. However, there can also be a penalty on the write cycle of ~20 ps/fF. In TSMC, the 1T-MiM reduces SER FIT over one order of magnitude than 6T-SRAM in the same technology generation.

Triple Well Structure: Triple well structures have been widely used for both a better electrical isolation and a reduction of the nois originating from the substrate. As most actural devices are processed in a p-substrate, triple well is usually designated as deep n-well (DNW) or also n+ buried layer. DNW theoretically reduces the SER sensitivity as the electrons generated deep inside the substrate are more efficiently collected by the extended n buried zone and then better evacuated through n-well ties. Practically, DNW shows no improvement in TSMC 65nm SRAM.

11.4.3.3.2 ECC & MBU

The Error Correcting Code(ECC) function is a very efficient way to reduce SER though the circuit area overhead is considerable. But there still is the limitation of ECC function. When the errors occur in the same multiplexer(MUX) under the same wordline(WL), it will become a uncorrectable error. As the bitcell area scales down, the occurence of uncorrectable error will increase due to the Multiple-Bit-Upset(MBU). The illustration below can explain this phenomenon.



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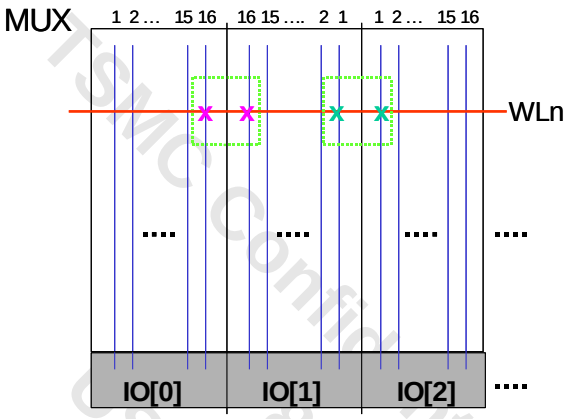
11.4.3.3.3 Design Suggestion for MBU

In order to avoid the uncorrectable error due to MBU, TSMC has two suggestions.

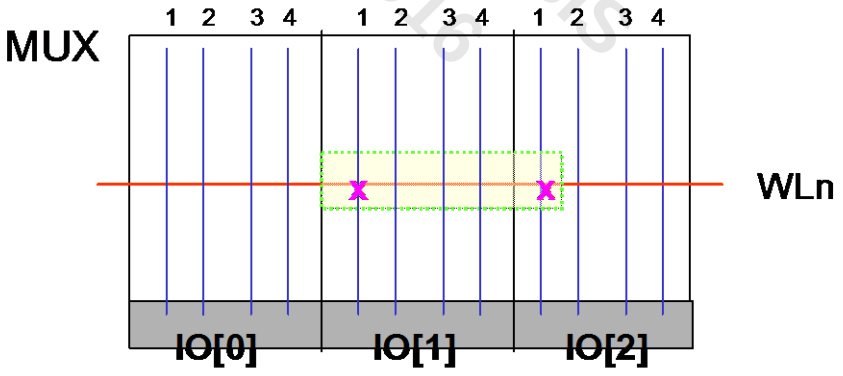
1. **Avoid Mirror type scramble layout.**

   Please refer to the illustration below as an example. If the I/O boundary is hit, it will make the word uncorrectable, because ECC can't correct 2(or more) errors in one word accessed. It's recommended to avoid this type design.



2. Use MUX-8 or higher design

   Please refer to the illustration below as an example. If one MBU possibly includes 5 adjacent fail bits, however, it happens in MUX-4 design. It will cause an uncorrectable error. For this issue, increasing the MUX number can raise the tolerance of MBU. Now the observed maximum adjacent bits number of one MBU due to neutron strike in N65 generation is 6. So it's recommended to use MUX-8 or higher design.



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11.5 e-Reliability Model System Introduction

The system objectives are to provide a simple, consistent and instant way to address your needs for reliability assessment in designing and production. TSMC provides a user-friendly reliability calculator on TSMC Online.

11.5.1 What is the e-Reliability Model System?

The system provides you reliability assessment for TSMC's process technologies, that includes intrinsic and product-level reliability.

A. Intrinsic reliability assessment:

   This includes gate oxide integrity (GOI), hot carrier injection (HCI), negative bias temperature instability (NBTI), electron migration (EM), and time depend dielectric breakdown of inter-metal dielectric (IMD-TDDB)

B. Product-level reliability assessment:

   This includes early failure rate (EFR), long term failure rate (LTFR), and estimates of voltage overdrive capability, the impact of voltage overshoot on circuit reliability, and allowable junction temperature.

11.5.2 Why the e-Reliability Model System?

The e-Reliability model system will help you achieve built-in reliability design and attain their business goals by using

1. A simple and instant way to do circuit lifetime prediction.
2. A model to predict production failure rate.
3. A solution provider to customize voltage/temperature/layout configurations.

11.5.3 Where to access the e-Reliability Model System?

The e-Reliability model system is built into TSMC Online on the Web in the Quality & Reliability section. There are two ways to use this system:

1. From overall Reliability Assessment, which provides an estimate of circuit lifetime for a user-defined set of circuit operating conditions and transistor and interconnect layout geometry.
2. From advanced Reliability Assessment, which provides (a) Reliability assessment for individual failure items under a given set of circuit operating conditions and layout geometry. (b) Product-level reliability (EFR, LTFR) or voltage/temperature estimates, resulting from user level-defined operating conditions and die size.

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12 Electrical Parameters Summary

12.1 Available MOS transistors
12.2 Key parameters of MOS transistors in CLN65LP and CLN65LPHV
12.3 Key parameters of MOS transistors in CLN65G
12.4 Key parameters of MOS transistors in CLN65GP
12.5 Key parameters of MOS transistors in CLN65LPG
12.6 Key parameters of MOS transistors in CLN65ULP
12.7 Key parameters of MOS transistors in CLN55GP
12.8 Key parameters of MOS transistors in CLN55LP
12.9 Key parameters of bipolar transistors
12.10 Key parameters of junction diodes
12.11 Resistor model
12.12 Unsilicided N+/P+ poly resistors models
12.13 Unsilicided N+/P+ diffusion resistors models
12.14 Interconnect model
12.15 MIM capacitor model
12.16 MOM capacitor model
12.17 Inductor model
12.18 RF I/O PAD model

All the dimensions in this chapter are wafer dimensions, unless specified otherwise. The electrical parameters are given for T=25°C, unless specified otherwise.

The electrical parameters in this chapter are dependent on the following documents. Please be sure to use the most update version for circuit design.

Technology		Core/IO	Doc NO.	Version
CLN65	LP	1.2V/2.5V	T-N65-CL-SP-009	V1.4
		1.2V/2.5V (HVMOS)	T-N65-CL-SP-070	V1.1
		1.2V/3.3V	T-N65-CL-SP-040	V1.1
	G	1.0V/1.8V	T-N65-CL-SP-023	V1.3
		1.0V/2.5V	T-N65-CL-SP-020	V1.3
	GP	1.0V/1.8V	T-N65-CL-SP-031	V1.3
		1.0V/2.5V	T-N65-CL-SP-041	V1.3
	LPG	1.0V(G), 1.2(LP)/ 2.5V	T-N65-CL-SP-034	V1.0
	ULP	1.0V/2.5V	T-N65-CL-SP-055	V1.2
CLN55	GP	1.0V/1.8V	T-N55-CL-SP-007	V1.2
		1.0V/2.5V	T-N55-CL-SP-010	V1.2
	LP	1.2V/2.5V	T-N55-CL-SP-021	V1.1
CMN65	LP for MS	1.2V/2.5V	T-N65-CM-SP-002	V1.4
		1.2V/2.5V (HVMOS)	T-N65-CL-SP-026-P1	V1.0P1
		1.2V/3.3V	T-N65-CM-SP-014	V1.0
	LP for RF	1.2V/2.5V	T-N65-CM-SP-007	V1.6
		1.2V/3.3V	T-N65-CM-SP-012	V1.4
	GP for MS	1.0V/2.5V	T-N65-CM-SP-006	V1.3

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12.1 Available MOS Transistors

12.1.1 CLN65LP (1.2V)

	Model Name		Electric_Tox (Å)		Minimum Length (μ m)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.20V_Standard_Vt_MOS	nch	pch	26	28	0.06	0.06
1.20V_High_Vt_MOS	nch_hvt	pch_hvt	26	28	0.06	0.06
1.20V_Low_Vt_MOS	nch_lvt	pch_lvt	26	28	0.06	0.06
1.20V_mLow_Vt_MOS	nch_mlvt	pch_mlvt	26	28	0.06	0.06
2.50V_MOS	nch_25	pch_25	56	59	0.28	0.28
1.80V_MOS	nch_18	pch_18	56	59	0.26	0.26
3.30V_MOS	nch_33	pch_33	73	75	0.38	0.38
2.5V over-drive 3.3V MOS	nch_25od33	pch_25od33	56	59	0.5	0.4
2.5V under-drive 1.8V MOS	nch_25ud18	pch_25ud18	56	59	0.26	0.26
1.20V_Native_MOS	nch_na	-	26	-	0.2	-
2.50V_Native_MOS	nch_na25	-	56	-	1.2	-
3.30V_Native_MOS	nch_na33	-	73	-	1.2	-
2.50V_Native_over-drive 3.3V_MOS	nch_na25od33	-	56	-	1.2	-
2.5/5.5V_High_Voltage_MOS	nch_hv25_snw	pch_hv25_spw	56	59	0.85	0.6

12.1.2 CLN65LPHV (2.5V)

	Model Name		Electric_Tox (Å)		Minimum Length (μ m)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
2.50V_MOS	nch_hv25_snw	pch_hv25_spw	56	59	0.85	0.6

12.1.3 CLN65G (1.0V)

	Model Name		Electric_Tox (Å)		Minimum Length (μ m)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.0V_Standard_Vt_MOS	nch	pch	20.7	23	0.06	0.06
1.0V_High_Vt_MOS	nch_hvt	pch_hvt	20.7	23	0.06	0.06
1.8V MOS	nch_18	nch_18	34.0	37.0	0.2	0.2
2.5V MOS	nch_25	pch_25	56	59	0.28	0.28
1.0V_Native_MOS	nch_na	-	20.7	-	0.2	-
1.8V Native MOS	nch_na18	-	34.0	-	0.8	-
2.5V_Native_MOS	nch_na25	-	56	-	1.2	-

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12.1.4 CLN65GP (1.0V_2.5V)

	Model Name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.0V Standard Vt MOS	nch	pch	20	22	0.06	0.06
1.0V High Vt MOS	nch_hvt	pch_hvt	20	22	0.06	0.06
1.0V Low Vt MOS	nch_lvt	pch_lvt	20	22	0.06	0.06
1.8V Under-drive MOS	nch_18	pch_18	56.0	59.0	0.26	0.26
2.5V MOS	nch_25	pch_25	56.0	59.0	0.28	0.28
3.3V Over-drive MOS	nch_33	pch_33	56	59	0.5	0.4
1.8V Under-drive MOS	nch_25ud18	pch_25ud18	56.0	59.0	0.26	0.26
3.3V MOS	nch_25od33	pch_25od33	56.0	59.0	0.26	0.26
1.0V Native MOS	nch_na	-	20	-	0.2	-
2.5V Native MOS	nch_na25	-	56.0	-	1.2	-
3.3V Over-drive Native MOS	nch_na33	-	56.0	-	1.2	-
3.3V Over-drive Native MOS	nch_na25od33	-	56.0	-	1.2	-

12.1.5 CLN65LPG (LP:1.2V, G:1.0V)

	Model Name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.0V Standard Vt MOS	nch_lpg	pch_lpg	20.5	23	0.06	0.06
1.0V High Vt MOS	nch_lpghvt	pch_lpghvt	20.5	23	0.06	0.06
1.8V Under-drive MOS (2.5V underdrive to 1.8V)	nch_25ud18	pch_25ud18	56	59	0.26	0.26
2.5V MOS	nch_25	pch_25	56	59	0.28	0.28
3.3V Over-drive MOS (2.5V overdrive to 3.3V)	nch_25od33	pch_25od33	56	59	0.5	0.4
1.0V Native MOS	nch_lpgna	-	20.5	-	0.2	-
2.5V Native MOS	nch_na25	-	56	-	1.2	-

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12.1.6 CLN65ULP (1.0V)

	Model Name		Electric_Tox (Å)		Minimum Length (μ m)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.20V_Standard_Vt_MOS	nch	pch	26	28	0.06	0.06
1.20V_High_Vt_MOS	nch_hvt	pch_hvt	26	28	0.06	0.06
1.20V_Low_Vt_MOS	nch_lvt	pch_lvt	26	28	0.06	0.06
1.20V_mLow_Vt_MOS	nch_mlvt	pch_mlvt	26	28	0.06	0.06
2.50V_MOS	nch_25	pch_25	56	59	0.28	0.28
1.80V_MOS	nch_18	pch_18	56	59	0.26	0.26
3.30V_MOS	nch_33	pch_33	56	59	0.5	0.4
1.20V_Native_MOS	nch_na	-	26	-	0.2	-
2.50V_Native_MOS	nch_na25	-	56	-	1.2	-
2.50V_Native_over-drive 3.3V_MOS	nch_na25od33	-	56	-	1.2	-
2.5/5.5V_High_Voltage_MOS	nch_hv25_snw	pch_hv25_spw	56	59	0.85	0.6

12.1.7 CLN55GP (1.0V_2.5V)

	Model Name		Electric_Tox (Å)		Minimum Length (μ m)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.0V_Standard_Vt_MOS	nch	pch	20.3	22.3	0.054	0.054
1.0V_High_Vt_MOS	nch_hvt	pch_hvt	20.3	22.3	0.054	0.054
1.0V_Low_Vt_MOS	nch_lvt	pch_lvt	20.3	22.3	0.054	0.054
1.00V_Ultra_High_Vt_MOS	nch_uhvt	pch_uhvt	20.3	22.3	0.054	0.054
1.8V_MOS	nch_18	pch_18	34	37	0.18	0.18
2.5V_MOS	nch_25	pch_25	56	59	0.252	0.252
3.3V Over-drive MOS (2.5V overdrive to 3.3V)	nch_33	pch_33	56	59	0.45	0.36
1.0V_Native_MOS	nch_na	-	20.3	-	0.18	-
1.8V_Native_MOS	nch_na18	-	34	-	0.72	-
2.5V_Native_MOS	nch_na25	-	56	-	1.08	-
3.30V_Native_MOS	nch_na33	-	56	-	1.08	-
2.5V over-drive 3.30V_Native MOS	nch_na25od33	-	56	-	1.08	-

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12.1.8 CLN55LP (1.2V)

	Model Name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.20V_Standard_Vt_MOS	nch	pch	26.9	28.1	0.054	0.054
1.20V_High_Vt_MOS	nch_hvt	pch_hvt	26.9	28.1	0.054	0.054
1.20V_Low_Vt_MOS	nch_lvt	pch_lvt	26.9	28.1	0.054	0.054
1.80V_MOS	nch_18	pch_18	60.69	63.75	0.234	0.252
2.50V_MOS	nch_25	pch_25	60.69	63.75	0.252	0.252
3.30V_MOS	nch_33	pch_33	60.69	63.75	0.45	0.36
2.50V_under-drive 1.8V MOS	nch_25ud18	pch_25ud18	60.69	63.75	0.234	0.252
2.50V_over-drive 3.3V MOS	nch_25od33	pch_25od33	60.69	63.75	0.45	0.36
1.20V_Native_MOS	nch_na	-	26.9	-	0.18	-
2.50V_Native_MOS	nch_na25	-	60.69	-	1.08	-
2.50V Native over-drive 3.3V MOS	nch_na25od33	-	60.69	-	1.08	-

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12.2 Key Parameters of MOS Transistors in CLN65LP & CLN65LPHV

12.2.1 1.2V Standard Vt MOS

The following table summarizes the key parameters for 1.2V standard V_t MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.001±0.005	0.002±0.005	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	26±0.670	28±0.670	
Vt_gm	1	1	V	0.450 0.033 -0.033	0.427 -0.036	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	0.3_0.6	0.06		0.519 0.067 -0.080	0.531 -0.054	
	0.12	0.06		0.493 0.091 -0.110	0.518 -0.090	
Vt_lin	1	1	V	0.340 0.034 -0.035	0.386 -0.036	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
	0.3_0.6	0.06		0.402 0.068 -0.082	0.475 -0.062	
	0.12	0.06		0.375 0.096 -0.116	0.442 -0.097	
Vt_sat	1	1	V	0.319	0.360	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	0.3_0.6	0.06		0.296	0.356	
	0.12	0.06		0.288	0.344	
DIBL	0.3_0.6	0.06	V	0.10591	-0.11893	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	92.677	42.347	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		104.36	56.715	
Id_sat	0.3_0.6	0.06	uA/um	603.34 -18.7% 21.9%	316.98 -17.3% 18.0%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.12	0.06		683.86 -24.7% 29.1%	410.47 -24.0% 27.6%	
Isoff	0.3_0.6	0.06	pA/um	211.29 0.055 19.336	128.51 0.110 15.884	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	0.3_0.6	0.06	mV/dec	88.809	101.66	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.35082	0.024836	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.043	0.060	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	4.176E-01	7.369E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.21E-01	2.14E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.251	1.077	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.06	ps/gate	9.312 1.874	-1.5539	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.2.2 1.2V High V_t MOS

The following table summarizes the key parameters for 1.20V_High_Vt MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.001±0.005	0.002±0.005	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	26±0.670	28±0.670	
Vt_gm	1	1	V	0.583 0.034 -0.036	0.607 -0.034	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	0.3_0.6	0.06		0.624 0.075 -0.085	0.644 -0.062	
	0.12	0.06		0.580 0.102 -0.113	0.620 -0.093	
Vt_lin	1	1	V	0.463 0.036 -0.038	0.559 -0.035	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
	0.3_0.6	0.06		0.502 0.076 -0.079	0.593 -0.065	
	0.12	0.06		0.467 0.114 -0.110	0.551 -0.096	
Vt_sat	1	1	V	0.450	0.545	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	0.3_0.6	0.06		0.406	0.492	
	0.12	0.06		0.385	0.460	
DIBL	0.3_0.6	0.06	V	0.096729	-0.10076	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	74.49	32.887	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		83.563	46.103	
Id_sat	0.3_0.6	0.06	uA/um	434.2 -19.4% 24.7%	216.99 -19.0% 21.2%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.12	0.06		509.06 -27.0% 33.2%	290.74 -26.3% 31.3%	
Isoff	0.3_0.6	0.06	pA/um	10.126 0.247 5.699	4.4026 0.240 4.966	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	0.3_0.6	0.06	mV/dec	98.661	108.52	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.34713	0.022115	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.075	0.091	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	3.262E-01	9.827E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.13E-01	1.92E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.472	1.091	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.06	ps/gate	14.51 3.153	-2.604	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.2.3 1.2V mLow MOS

The following table summarizes the key parameters for 1.20V_mLow_Vt MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.007±0.005	0.002±0	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	26±0.670	28±0.670	
Vt_gm	1	1	V	0.450 0.037 -0.037	0.427 -0.036	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	0.3_0.6	0.06		0.504 0.082 -0.093	0.535 -0.073	
	0.12	0.06		0.475 0.108 -0.124	0.527 -0.103	
Vt_lin	1	1	V	0.340 0.038 -0.038	0.386 -0.036	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
	0.3_0.6	0.06		0.372 0.085 -0.104	0.475 -0.085	
	0.12	0.06		0.371 0.110 -0.147	0.461 -0.118	
Vt_sat	1	1	V	0.319	0.360	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	0.3_0.6	0.06		0.268	0.332	
	0.12	0.06		0.260	0.344	
DIBL	0.3_0.6	0.06	V	0.10421	-0.14311	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	99.898	43.713	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		112.73	56.062	
Id_sat	0.3_0.6	0.06	uA/um	646.3 -20.4% 23.6%	342.25 -19.0% 21.7%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.12	0.06		728.37 -25.9% 31.6%	416.87 -26.3% 33.2%	
Isoff	0.3_0.6	0.06	pA/um	584.9 0.049 30.891	213.56 0.069 38.332	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	0.3_0.6	0.06	mV/dec	90.993	100.34	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.34858	0.024688	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.043	0.050	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	4.682E-01	9.163E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.21E-01	2.14E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.251	1.077	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.06	ps/gate	8.2501 2.0479	 -1.5904	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.2.4 1.2V Low V_t MOS

The following table summarizes the key parameters for 1.20V_Low_Vt MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.001±0.005	0.002±0.005	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	26±0.670	28±0.670	
Vt_gm	1	1	V	0.308 0.036 -0.036	0.308 -0.032	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	0.3_0.6	0.06		0.414 0.075 -0.084	0.464 -0.066	
	0.12	0.06		0.386 0.094 -0.108	0.448 -0.110	
Vt_lin	1	1	V	0.212 0.040 -0.040	0.266 -0.036	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
	0.3_0.6	0.06		0.314 0.082 -0.094	0.409 -0.075	
	0.12	0.06		0.296 0.104 -0.120	0.385 -0.114	
Vt_sat	1	1	V	0.189	0.226	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	0.3_0.6	0.06		0.189	0.267	
	0.12	0.06		0.177	0.262	
DIBL	0.3_0.6	0.06	V	0.12444	-0.14228	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	107.33	45.252	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		122.79	60.688	
Id_sat	0.3_0.6	0.06	uA/um	741.92 -19.6% 22.0%	381.69 -17.5% 19.0%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.12	0.06		844.5 -24.5% 29.4%	481.74 -23.8% 28.6%	
Isoff	0.3_0.6	0.06	pA/um	4256.4 0.040 34.045	854.88 0.058 21.846	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	0.3_0.6	0.06	mV/dec	91.26	99.881	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.34787	0.024602	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.036	0.036	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	4.766E-01	1.033E-02	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.32E-01	2.24E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.185	1.068	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.06	ps/gate	7.316 1.5033	-1.1826	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.2.5 1.8V I/O MOS (2.5V underdrive to 1.8V)

The following table summarizes the key parameters for 2.5V under-drive 1.80V MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS		PMOS		Definition
△L (xl +/-dxl)			um	-0.015±0.01		-0.015±0.01		
△W(xw+/-dxw)			um	0.007±0.012		0.007±0.012		
Electrical_ Tox			Å	56±3.000		59±3.000		
Vt_gm	10	10	V	0.579		0.642		Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.050	-0.050		-0.048	
	10	0.26		0.560		0.506		
				0.067	-0.069		-0.062	
	0.4	0.26		0.526		0.484		
				0.082	-0.088		-0.097	
Vt_lin	10	10	V	0.519		0.682		Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
				0.052	-0.052		-0.051	
	10	0.26		0.504		0.530		
				0.072	-0.074		-0.067	
	0.4	0.26		0.461		0.496		
				0.088	-0.094		-0.104	
Vt_sat	10	10	V	0.512		0.669		Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	0.26		0.416		0.431		
	0.4	0.26		0.386		0.400		
DIBL	10	0.26	V	0.087629		-0.0986		Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.26	uA/um	42.697		14.387		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.26		45.431		17.802		
Id_sat	10	0.26	uA/um	375.65		193.98		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-14.3%	15.5%	-15.1%	16.9%	
	0.4	0.26		398.32		229.05		
				-21.2%	22.8%	-20.5%	24.7%	
Ioff	10	0.26	pA/um	3.9411		3.5208		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.158	6.646	0.180	6.292	
Sub Vt slope	10	0.26	mV/dec	90.84		94.472		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.26	V	0.113		0.101		△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.26	nA/um	2.903E+00		3.405E-03		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.26	fF/um	2.66E-01		2.81E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.195		1.111		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.26	ps/gate	35.036				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				6.271		-5.159		

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12.2.6 2.5V I/O MOS

The following table summarizes the key parameters for 2.50V MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.01	-0.015±0.01	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.579 0.050 -0.050	0.642 -0.048	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	10	0.28		0.576 0.066 -0.068	0.515 -0.061	
	0.4	0.28		0.535 0.079 -0.084	0.493 -0.093	
Vt_lin	10	10	V	0.519 0.052 -0.052	0.682 -0.051	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
	10	0.28		0.525 0.070 -0.072	0.541 -0.066	
	0.4	0.28		0.466 0.085 -0.090	0.510 -0.099	
Vt_sat	10	10	V	0.512	0.669	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	0.28		0.430	0.432	
	0.4	0.28		0.391	0.404	
DIBL	10	0.28	V	0.094561	-0.10853	Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.28	uA/um	51.809	17.925	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.28		54.581	21.637	
Id_sat	10	0.28	uA/um	605.6 -11.5% 12.2%	342.64 -11.4% 12.7%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.4	0.28		644.25 -16.5% 17.2%	394.07 -15.8% 18.7%	
Ioff	10	0.28	pA/um	1.7285 0.169 6.205	2.4638 0.183 6.250	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	0.28	mV/dec	87.698	91.697	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.28	V	0.163	0.146	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.28	nA/um	1.897E+02	1.197E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.28	fF/um	2.55E-01	2.71E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.195	1.111	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.28	ps/gate	27.53 3.44	-2.948	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.2.7 3.3V I/O MOS (2.5V overdrive to 3.3V)

The following table summarizes the key parameters for 2.5V over-drive 3.30V MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.01	-0.015±0.01	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.579	0.642	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.050 -0.050	-0.048	
	10	N0.5 / P0.4		0.631	0.609	
				0.057 -0.058	-0.051	
	0.4	N0.5 / P0.4		0.563	0.580	
				0.065 -0.068	-0.074	
Vt_lin	10	10	V	0.519	0.682	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
				0.052 -0.052	-0.051	
	10	N0.5 / P0.4		0.578	0.641	
				0.060 -0.060	-0.056	
	0.4	N0.5 / P0.4		0.503	0.602	
				0.071 -0.073	-0.080	
Vt_sat	10	10	V	0.511	0.669	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	N0.5 / P0.4		0.550	0.604	
	0.4	N0.5 / P0.4		0.474	0.562	
DIBL	10	N0.5 / P0.4	V	0.028083	-0.037659	Vb=0, Vt_lin-Vt_sat
Id_lin	10	N0.5 / P0.4	uA/um	31.488	13.584	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	N0.5 / P0.4		33.379	17.015	
Id_sat	10	N0.5 / P0.4	uA/um	570.26	346.27	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-8.8% 9.2%	-8.0% 8.8%	
	0.4	N0.5 / P0.4		628.69	404.57	
				-13.3% 14.0%	-11.6% 13.3%	
Ioff	10	N0.5 / P0.4	pA/um	0.054651	0.47088	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.386 3.207	0.635 1.634	
Sub Vt slope	10	N0.5 / P0.4	mV/dec	91.849	94.158	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	N0.5 / P0.4	V	0.349	0.292	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	N0.5 / P0.4	nA/um	1.465E+03	3.501E+01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	N0.5 / P0.4	fF/um	2.48E-01	2.64E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.195	1.111	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	N0.5 / P0.4	ps/gate	49.567		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				3.583	-3.224	

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12.2.8 3.3V I/O MOS

The following table summarizes the key parameters for 3.3V I/O MOS in CLN65LP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			μm	-0.015 ± 0.012	-0.015 ± 0.012	
△W(xw+/-dxw)			μm	0.000 ± 0.012	0.000 ± 0.012	
Electrical_ Tox			Å	73.0 ± 3	75.0 ± 3	
Vt_lin	10	10	V	0.548	-0.666	Vg @Vd=0.05V, Vs=Vb=0
				0.045 -0.045	0.059 -0.060	
	10	0.38		0.595	-0.608	
				0.066 -0.067	0.065 -0.066	
	0	0.38		0.519	-0.565	
				0.072 -0.073	0.069 -0.070	
Vt_sat	10	10	V	0.536	-0.652	Vg @Vd=Vdd, Vs=Vb=0
				0.045 -0.044	0.058 -0.059	
	10	0.38		0.522	-0.563	
				0.069 -0.070	0.066 -0.067	
	0.4	0.38		0.457	-0.524	
				0.073 -0.074	0.069 -0.070	
DIBL	10	0.38	V	0.073	0.045	Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.38	μA/μm	39.6	12.8	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.38		43.1	16.2	
Id_sat	10	0.38	μA/μm	604	300	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				10.5% -9.8%	10.9% -10.1%	
	0.4	0.38		651	356	
				13.1% -11.9%	13.6% -12.1%	
Ioff	10	0.38	pA/μm	1.57E-01	2.01E-01	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				5.86E-01 -1.25E-01	6.28E-01 -1.25E-01	
Sub Vt slope	10	0.38	mV/dec	93	98	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.38	V	0.267	0.345	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.38	nA/um	9.74E+02	8.23E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl			fF/um	0.209	0.195	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.14	1.11	Vrev=0V
Inverter FO=1 Delay	Wn/Wp = 3.6/5	0.38	ps/gate	37.3702		RO_Td(ring oscillator delay time with rg,rc) @ V=Vdd (Fan_out=1)
				3.6612	-3.2277	

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12.2.9 1.2V Native MOS

The following table summarizes the key parameters for 1.20V_Native MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.001±0.005	
△W(xw+/-dxw)			um	0.02±0.008	
Electrical_ Tox			Å	26±0.670	
Vt_gm	1	1	V	0.050 0.045	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	1	0.2		0.115 0.068	
	0.5	0.2		0.121 0.071	
Vt_lin	1	1	V	-0.038 0.048	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
	1	0.2		-0.001 0.074	
	0.5	0.2		0.008 0.076	
Vt_sat	1	1	V	-0.092	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	1	0.2		-0.077	
	0.5	0.2		-0.069	
DIBL	1	0.2	V	0.075746	Vb=0, Vt_lin-Vt_sat
Id_lin	1	0.2	uA/um	77.175	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	0.2		78.701	
Id_sat	1	0.2	uA/um	706.43 -13.0% 13.7%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.5	0.2		741.78 -14.5% 15.5%	
Ioff	1	0.2	pA/um	1.41E+06 0.101 7.572	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	1	0.2	mV/dec	81.564	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.26848	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	1	0.2	V	0.018	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	1	0.2	nA/um	0.083	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.2	fF/um	4.00E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.155	Vrev=0V

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12.2.102.5V Native I/O MOS

The following table summarizes the key parameters for 2.50V_Native MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.03859±0.01	
△W(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	56±3.000	
Vt_gm	10	10	V	-0.066 0.053	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	10	1.2		-0.100 0.080	
	0.5	1.2		-0.076 0.084	
Vt_lin	10	10	V	-0.130 0.056	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
	10	1.2		-0.146 0.084	
	0.5	1.2		-0.118 0.088	
Vt_sat	10	10	V	-0.136	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	1.2		-0.178	
	0.5	1.2		-0.131	
DIBL	10	1.2	V	0.032093	Vb=0, Vt_lin-Vt_sat
Id_lin	10	1.2	uA/um	17.157	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	1.2		18.345	
Id_sat	10	1.2	uA/um	406.44 -10.2% 11.4%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.5	1.2		423.96 -13.2% 14.7%	
Ioff	10	1.2	pA/um	2.59E+06 0.270 2.689	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	1.2	mV/dec	82.6	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	1.2	V	0.047	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	1.2	nA/um	0.828	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	1.2	fF/um	3.31E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.145159	Vrev=0V

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12.2.11 2.5V Native Over-drive 3.3V I/O MOS

The following table summarizes the key parameters for 3.30V_Native MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.03859±0.01	
△W(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	56±3.000	
Vt_gm	10	10	V	-0.105 0.052	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	10	1.2		-0.123 0.078	
	0.5	1.2		-0.082 0.084	
Vt_lin	10	10	V	-0.128 0.055	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
	10	1.2		-0.145 0.081	
	0.5	1.2		-0.122 0.088	
Vt_sat	10	10	V	-0.138	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	1.2		-0.187	
	0.5	1.2		-0.143	
DIBL	10	1.2	V	0.042186	Vb=0, Vt_lin-Vt_sat
Id_lin	10	1.2	uA/um	18.292	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	1.2		20.173	
Id_sat	10	1.2	uA/um	557.11 -8.4% 8.6%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.5	1.2		593.82 -11.3% 11.9%	
Ioff	10	1.2	pA/um	3.44E+06 0.305 2.612	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	1.2	mV/dec	75.458	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	1.2	V	0.063	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	1.2	nA/um	13.229	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	1.2	fF/um	3.08E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.145159	Vrev=0V

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12.2.12 2.5/5.5V High Voltage MOS

The following table summarizes the key parameters for 2.50/5.5V HV MOS in CLN65LP process.

	W (um)	L (um)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	-0.015±0		-0.015±0		
ΔW(xw+/-dxw)			um	0.007±0		0.007±0		
Electrical_ Tox			Å	56±0.000		59±0.000		
Vt_gm	10	10	V	0.583		0.643		Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.032	-0.033	0.033	-0.033	
	10	N: 0.85 P: 0.6		0.598		0.507		
				0.075	-0.076	0.065	-0.065	
	0.6	N: 0.85 P: 0.6		0.562		0.506		
				0.105	-0.107	0.085	-0.085	
Vt_lin	10	10	V	0.534		0.682		Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
				0.035	-0.036	0.035	-0.036	
	10	N: 0.85 P: 0.6		0.527		0.513		
				0.080	-0.08	0.070	-0.070	
	0.6	N: 0.85 P: 0.6		0.486		0.509		
				0.111	-0.111	0.091	-0.090	
Vt_sat	10	10	V	0.528		0.670		Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=±5.5V, Vs=Vb=0
	10	N: 0.85 P: 0.6		0.513		0.462		
	0.6	N: 0.85 P: 0.6		0.472		0.458		
DIBL	10	N: 0.85 P: 0.6	V	0.01451		-0.05149		Vb=0, Vt_lin-Vt_sat
Id_lin	10	N: 0.85 P: 0.6	uA/um	26.350		10.430		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.6	N: 0.85 P: 0.6		28.480		11.770		
Id_sat	10	N: 0.85 P: 0.6	uA/um	474.20		277.30		Id @Vg=±2.5V, Vd=±5.5V, Vs=Vb=0
				-11.6%	11.6%	-17.9%	17.9%	
	0.6	N: 0.85 P: 0.6		514.10		300.90		
				-15.5%	15.5%	-18.3%	18.3%	
Ioff	10	N: 0.85 P: 0.6	pA/um	8.2660		12.730		Id @Vg=0, Vd=±5.5V, Vs=Vb=0
				0.100	10.452	0.110	10.094	
Sub Vt slope	10	N: 0.85 P: 0.6	mV/dec	91.298		90.186		Slope @Vd=±5.5V, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	N: 0.85 P: 0.6	V	0.413		0.211		ΔVt_sat @Vb=-(±5.5V)/2 and Vb=0
Isub	10	N: 0.85 P: 0.6	nA/um	9.030E-02		8.368E-04		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	N: 0.85 P: 0.6	fF/um	4.56E-01		3.66E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cjd			fF/um2	0.141		0.575		Vrev=0V
Cjs			fF/um2	1.195		1.111		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 6.4/6.8	N: 0.85 P: 0.6	ps/gate	94.8609				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				13.3291		-10.2616		

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12.2.13 2.50V MOS

The following table summarizes the key parameters for 2.50V MOS in CLN65LPHV process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
ΔL (xl +/-dxl)			um	-0.015±0	-0.015±0	
ΔW(xw+/-dxw)			um	0.007±0	0.007±0	
Electrical_ Tox			Å	56±0.000	59±0.000	
Vt_gm	10	10	V	0.583 0.032 -0.033	0.643 0.033 -0.033	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	10	N: 0.85 P: 0.6		0.598 0.075 -0.076	0.507 0.065 -0.065	
	0.6	N: 0.85 P: 0.6		0.562 0.105 -0.107	0.506 0.085 -0.085	
Vt_lin	10	10	V	0.534 0.035 -0.036	0.682 0.035 -0.036	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
	10	N: 0.85 P: 0.6		0.527 0.080 -0.08	0.513 0.070 -0.070	
	0.6	N: 0.85 P: 0.6		0.486 0.111 -0.111	0.509 0.091 -0.090	
Vt_sat	10	10	V	0.528	0.670	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=±5.5V, Vs=Vb=0
	10	N: 0.85 P: 0.6		0.513	0.462	
	0.6	N: 0.85 P: 0.6		0.472	0.458	
DIBL	10	N: 0.85 P: 0.6	V	0.01451	-0.05149	Vb=0, Vt_lin-Vt_sat
Id_lin	10	N: 0.85 P: 0.6	uA/um	26.350	10.430	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.6	N: 0.85 P: 0.6		28.480	11.770	
Id_sat	10	N: 0.85 P: 0.6	uA/um	474.20 -11.6% 11.6%	277.30 -17.9% 17.9%	Id @Vg=±2.5V, Vd=±5.5V, Vs=Vb=0
	0.6	N: 0.85 P: 0.6		514.10 -15.5% 15.5%	300.90 -18.3% 18.3%	
Ioff	10	N: 0.85 P: 0.6	pA/um	8.2660 0.100 10.452	12.730 0.110 10.094	Id @Vg=0, Vd=±5.5V, Vs=Vb=0
Sub Vt slope	10	N: 0.85 P: 0.6	mV/dec	91.298	90.186	Slope @Vd=±5.5V, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	N: 0.85 P: 0.6	V	0.413	0.211	ΔVt_sat @Vb=-(±5.5V)/2 and Vb=0
Isub	10	N: 0.85 P: 0.6	nA/um	9.030E-02	8.368E-04	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	N: 0.85 P: 0.6	fF/um	4.56E-01	3.66E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cjd			fF/um2	0.141	0.575	Vrev=0V
Cjs			fF/um2	1.195	1.111	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 6.4/6.8	N: 0.85 P: 0.6	ps/gate	97.829 14.03	-10.67	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.3 Key parameters of MOS Transistors in CLN65G

12.3.1 1.0V Standard Vt MOS

The following table summarizes the key parameters for 1.0V standard V_t MOS in CLN65G process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.013±0.004	-0.01±0.004	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	20.7±0.600	23±0.600	
Vt_gm	1	1	V	0.213	0.299	Vg @Vd=0.05V, Vs=Vb=0
				0.035 -0.035	0.036 -0.035	
	0.3_0.6	0.06		0.322	0.335	
				0.060 -0.063	0.060 -0.061	
	0.12	0.06		0.301	0.315	
				0.082 -0.088	0.093 -0.088	
Vt_lin	1	1	V	0.116	0.250	Vg @Vd=0.05V, Vs=Vb=0, Id=4e-8*Wdrawn/Ldrawn
				0.037 -0.038	0.038 -0.037	
	0.3_0.6	0.06		0.210	0.273	
				0.066 -0.070	0.067 -0.069	
	0.12	0.06		0.188	0.248	
				0.091 -0.096	0.104 -0.101	
Vt_sat	1	1	V	0.090	0.236	Vg @Vd=Vdd, Vs=Vb=0, Id=4e-8*Wdrawn/Ldrawn
	0.3_0.6	0.06		0.123	0.127	
	0.12	0.06		0.116	0.126	
DIBL	0.3_0.6	0.06	V	0.086777	-0.14511	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	141.46	51.038	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		156.89	65.855	
Id_sat	0.3_0.6	0.06	uA/um	807.26	409.12	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-18.7% 18.8%	-19.1% 19.3%	
	0.12	0.06		900.71	516.97	
				-25.9% 26.3%	-27.3% 28.7%	
Isoff	0.3_0.6	0.06	pA/um	29138	33017	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.109 10.464	0.105 9.293	
Sub Vt slope	0.3_0.6	0.06	mV/dec	91.559	98.719	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	59.958	12.025	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.050	0.032	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	6.085E-02	1.212E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.03E-01	2.01E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.273	1.076	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.5	0.06	ps/gate	5.76786		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				1.0826	-0.85588	

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12.3.2 1.0V High Vt MOS

The following table summarizes the key parameters for 1.0V high V_t MOS in CLN65G process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.013±0.004	-0.01±0.004	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	20.7±0.600	23±0.600	
Vt_gm	1	1	V	0.349	0.409	Vg @Vd=0.05V, Vs=Vb=0
				0.035 -0.035	0.037 -0.037	
	0.3_0.6	0.06		0.385	0.390	
				0.075 -0.077	0.054 -0.054	
	0.12	0.06		0.363	0.368	
				0.099 -0.106	0.095 -0.093	
Vt_lin	1	1	V	0.239	0.363	Vg @Vd=0.05V, Vs=Vb=0, Id=4e-8*Wdrawn/Ldrawn
				0.036 -0.037	0.039 -0.039	
	0.3_0.6	0.06		0.267	0.329	
				0.080 -0.082	0.061 -0.061	
	0.12	0.06		0.246	0.301	
				0.106 -0.112	0.104 -0.101	
Vt_sat	1	1	V	0.227	0.352	Vg @Vd=Vdd, Vs=Vb=0, Id=4e-8*Wdrawn/Ldrawn
	0.3_0.6	0.06		0.192	0.216	
	0.12	0.06		0.173	0.201	
DIBL	0.3_0.6	0.06	V	0.074629	-0.11351	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	132.8	46.241	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		146.44	62.745	
Id_sat	0.3_0.6	0.06	uA/um	705.88	337.92	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-21.8% 22.3%	-21.0% 21.9%	
	0.12	0.06		805.84	441.44	
				-28.3% 31.0%	-30.2% 32.0%	
Isoff	0.3_0.6	0.06	pA/um	4481.5	3551.6	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.088 14.350	0.113 10.637	
Sub Vt slope	0.3_0.6	0.06	mV/dec	90.322	100.85	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	60.011	12.041	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.051	0.054	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	1.005E-01	3.236E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.01E-01	1.85E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.3	1.083	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.5	0.06	ps/gate	7.47354		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				1.72253	-1.22558	

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12.3.3 1.8V I/O MOS

The following table summarizes the key parameters for 1.8V I/O MOS in CLN65G process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.055±0.008	-0.055±0.008	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	34±1.333	37±1.333	
Vt_gm	10	10	V	0.342	0.384	Vg @Vd=0.05V, Vs=Vb=0
				0.050 -0.048	0.052 -0.050	
	10	0.2		0.495	0.477	
				0.058 -0.058	0.051 -0.054	
	0.4	0.2		0.510	0.467	
				0.071 -0.066	0.064 -0.066	
Vt_lin	10	10	V	0.298	0.415	Vg @Vd=0.05V, Vs=Vb=0, Id=1e-7*Wdrawn/Ldrawn
				0.053 -0.053	0.055 -0.052	
	10	0.2		0.438	0.486	
				0.065 -0.064	0.056 -0.059	
	0.4	0.2		0.455	0.464	
				0.080 -0.074	0.070 -0.071	
Vt_sat	10	10	V	0.286	0.401	Vg @Vd=Vdd, Vs=Vb=0, Id=1e-7*Wdrawn/Ldrawn
	10	0.2		0.366	0.427	
	0.4	0.2		0.370	0.406	
DIBL	10	0.2	V	0.071056	-0.05863	Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.2	uA/um	79.037	23.04	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.2		78.88	29.112	
Id_sat	10	0.2	uA/um	679.07	298.53	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-13.4% 13.5%	-13.6% 15.1%	
	0.4	0.2		692.97	357.32	
				-19.2% 20.4%	-17.3% 19.7%	
Ioff	10	0.2	pA/um	13.334	7.1915	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.166 6.963	0.166 7.622	
Sub Vt slope	10	0.2	mV/dec	84.962	99.543	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.2	V	0.080	0.135	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.2	nA/um	7.437E+01	8.951E-01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.2	fF/um	2.30E-01	1.94E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.384	1.098	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.5	0.2	ps/gate	18.4834		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				3.2224	-2.5873	

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12.3.4 2.5V I/O MOS

The following table summarizes the key parameters for 2.5V I/O MOS in CLN65G process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
ΔL (xl +/-dxl)			um	-0.015±0.01	-0.015±0.01	
ΔW(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.593 0.057 -0.057	0.610 0.047 -0.048	Vg @Vd=0.05V, Vs=Vb=0
	10	0.28		0.601 0.053 -0.054	0.483 0.053 -0.051	
	0.4	0.28		0.551 0.072 -0.073	0.449 0.069 -0.061	
Vt_lin	10	10	V	0.534 0.059 -0.059	0.651 0.050 -0.051	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	0.28		0.519 0.061 -0.062	0.505 0.059 -0.056	
	0.4	0.28		0.476 0.080 -0.080	0.466 0.074 -0.065	
Vt_sat	10	10	V	0.525	0.637	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	0.28		0.409	0.383	
	0.4	0.28		0.383	0.348	
DIBL	10	0.28	V	0.10967	-0.12246	Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.28	uA/um	52.208	17.213	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.28		55.963	21.948	
Id_sat	10	0.28	uA/um	608.94 -11.1% 12.3%	345.09 -11.7% 14.0%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.4	0.28		651.21 -16.2% 17.3%	420.5 -15.1% 20.0%	
Ioff	10	0.28	pA/um	1.7546 0.209 5.326	9.179 0.195 4.391	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	0.28	mV/dec	83.042	93.552	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.28	V	0.134	0.150	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.28	nA/um	2.361E+02	7.862E-01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.28	fF/um	2.18E-01	2.44E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.184	1.099	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.5	0.28	ps/gate	26.9157 3.312	-2.9873	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.3.5 1.0V Native MOS

The following table summarizes the key parameters for 1.0V native MOS in CLN65G process.

	W (μ m)	L (μ m)	Unit	NMOS		Definition
△L (xl +/-dxl)			um	-0.013±0.005		
△W(xw+/-dxw)			um	0.02±0.008		
Electrical_ Tox			Å	20.7±0.600		
Vt_gm	1	1	V	0.113		Vg @Vd=0.05V, Vs=Vb=0
				0.042	-0.042	
	1	0.2		0.171		
				0.060	-0.060	
	0.5	0.2		0.172		
				0.061	-0.061	
Vt_lin	1	1	V	0.014		Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.044	-0.044	
	1	0.2		0.069		
				0.063	-0.065	
	0.5	0.2		0.063		
				0.065	-0.067	
Vt_sat	1	1	V	-0.033		Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	1	0.2		0.006		
	0.5	0.2		0.000		
DIBL	1	0.2	V	0.063105		Vb=0, Vt_lin-Vt_sat
Id_lin	1	0.2	uA/um	82.623		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	0.2		82.184		
Id_sat	1	0.2	uA/um	618.59		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-14.3%	16.1%	
	0.5	0.2		622.44		
				-15.2%	17.2%	
Ioff	1	0.2	pA/um	167240		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.154	6.054	
Sub Vt slope	1	0.2	mV/dec	76.787		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	60.028		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	1	0.2	V	0.022		△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	1	0.2	nA/um	0.011		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.2	fF/um	3.26E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.164087		Vrev=0V

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12.3.6 1.8V Native MOS

The following table summarizes the key parameters for 1.8V native MOS in CLN65G process.

	W (μm)	L (μm)	Unit	NMOS		Definition
ΔL (xl +/-dxl)			μm	-0.055 ± 0.008		
ΔW(xw+/-dxw)			μm	0.007 ± 0.012		
Electrical_ Tox			Å	34.0± 1.333		
Vt_gm	10	10	V	0.342		Vg @Vd=0.05V, Vs=Vb=0
				0.049	-0.049	
	10.0	0.2		0.495		
				0.060	-0.060	
	0.40	0.2		0.510		
				0.071	-0.067	
Vt_lin	10	10	V	0.298		Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
				0.053	-0.053	
	10.0	0.2		0.438		
				0.067	-0.067	
	0.40	0.2		0.455		
				0.080	-0.076	
Vt_sat	10	10	V	0.286		Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10.0	0.2		0.366		
	0.40	0.2		0.370		
DIBL	10.0	0.2	V	0.071		Vb=0, Vt_lin-Vt_sat
Id_lin	10.0	0.2	μA/μm	79.0		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.40	0.2		78.9		
Id_sat	10.0	0.2	μA/μm	679		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				13.8%	-13.4%	
	0.40	0.2		693		
				19.2%	-18.0%	
Idoff	10.0	0.2	pA/μm	13		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				7.1E+01	-12	
Sub Vt slope	10.0	0.2	mV/dec	85		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10.0	0.2	V	0.080		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10.0	0.2	nA/um	7.4E+01		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.2	fF/um	0.254		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.384		Vrev=0V

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12.3.7 2.5V Native MOS

The following table summarizes the key parameters for 2.5V native MOS in CLN65G process.

	W (μm)	L (μm)	Unit	NMOS		Definition
ΔL (xl +/-dxl)			um	-0.015±0.01		
ΔW(xw+/-dxw)			um	0.007±0.012		
Electrical_ Tox			Å	56±3.000		
Vt_gm	10	10	V	-0.102		Vg @Vd=0.05V, Vs=Vb=0
				0.053	-0.060	
	10	1.2		-0.120		
				0.078	-0.084	
	0.5	1.2		-0.096		
				0.082	-0.086	
Vt_lin	10	10	V	-0.126		Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
				0.056	-0.063	
	10	1.2		-0.140		
				0.081	-0.088	
	0.5	1.2		-0.119		
				0.086	-0.090	
Vt_sat	10	10	V	-0.132		Vg @Vd=Vdd, Vs=Vb=0
	10	1.2		-0.176		
	0.5	1.2		-0.142		
DIBL	10	1.2	V	0.036255		Vb=0, Vt_lin-Vt_sat
Id_lin	10	1.2	uA/um	18.241		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	1.2		19.375		
Id_sat	10	1.2	uA/um	407.25		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-11.6%	12.4%	
	0.5	1.2		426.2		
				-13.4%	14.6%	
Ioff	10	1.2	pA/um	3.40E+06		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.272	2.446	
Sub Vt slope	10	1.2	mV/dec	72.418		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	1.2	V	0.053		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	1.2	nA/um	0.808		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	1.2	fF/um	3.25E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.15305		Vrev=0V

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12.4 Key Parameters of MOS Transistors in CLN65GP

12.4.1 1.0V Standard Vt MOS

The following table summarizes the key parameters for 1.0V standard V_t MOS in CLN65GP process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition
△L (xl +/-dxl)			μm	-0.019 ± 0.004		-0.016 ± 0.004		
△W(xw+/-dxw)			μm	0.016 ± 0.008		0.016 ± 0.008		
Electrical_ Tox			Å	20 ± 0.6		22.0 ± 0.6		
Vt_gm	1	1	V	0.308		0.291		Vg @Vd=0.05V, Vs=Vb=0
				0.035	-0.034	0.038	-0.038	
	0.3_0.6	0.06		0.362		0.378		
				0.061	-0.064	0.057	-0.053	
	0.12	0.06		0.346		0.362		
				0.080	-0.082	0.085	-0.085	
Vt_lin	1	1	V	0.210		0.240		Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.036	-0.038	0.039	-0.040	
	0.3_0.6	0.06		0.271		0.317		
				0.065	-0.072	0.061	-0.058	
	0.12	0.06		0.256		0.296		
				0.086	-0.091	0.092	-0.092	
Vt_sat	1	1	V	0.197		0.224		Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.3_0.6	0.06		0.171		0.173		
	0.12	0.06		0.159		0.171		
DIBL	0.3_0.6	0.06	V	0.100		0.144		Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	μA/μm	142.2		51.7		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		154.8		66.5		
Id_sat	0.3_0.6	0.06	μA/μm	798		402		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				21.6%	-19.8%	19.9%	-20.2%	
	0.12	0.06		879		503		
				28.0%	-26.7%	30.2%	-28.4%	
Idoff	0.3_0.6	0.06	pA/μm	11060		13680		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				9.4E+04	-9.3E+03	8.2E+04	-1.2E+04	
Sub Vt slope	0.3_0.6	0.06	mV/dec	95		103		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1.00	nA/um2	121		30		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.069		0.031		△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	1.90E+00		5.31E-03		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.06	fF/um	2.54E-01		2.41E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.27		1.06		Vrev=0V
Inverter FO=1 Delay	Wn/Wp = 3.6/5	0.06	ps/gate	6.599				RO_Td(ring oscillator delay time) @ V=Vdd,ccoflag=1 (Fan_out=1)
				1.489		-1.139		

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12.4.2 1.0V High Vt MOS

The following table summarizes the key parameters for 1.0V high V_t MOS in CLN65GP process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition
△L (xl +/-dxl)			μm	-0.019 ± 0.004		-0.016 ± 0.004		
△W(xw+/-dxw)			μm	0.016 ± 0.008		0.016 ± 0.008		
Electrical_ Tox			Å	20 ± 0.6		22.0 ± 0.6		
Vt_gm	1	1	V	0.458		0.396		Vg @Vd=0.05V, Vs=Vb=0
				0.031	-0.032	0.043	-0.044	
	0.3_0.6	0.06		0.448		0.432		
				0.051	-0.072	0.058	-0.064	
	0.12	0.06		0.420		0.416		
				0.087	-0.109	0.106	-0.119	
Vt_lin	1	1	V	0.350		0.344		Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.033	-0.034	0.045	-0.046	
	0.3_0.6	0.06		0.328		0.369		
				0.058	-0.070	0.059	-0.061	
	0.12	0.06		0.309		0.351		
				0.092	-0.107	0.105	-0.109	
Vt_sat	1	1	V	0.340		0.331		Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.3_0.6	0.06		0.229		0.241		
	0.12	0.06		0.212		0.231		
DIBL	0.3_0.6	0.06	V	0.100		0.128		Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	μA/μm	126.4		46.2		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		137.1		60.2		
Id_sat	0.3_0.6	0.06	μA/μm	683		329		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				22.2%	-20.9%	20.5%	-20.4%	
	0.12	0.06		760		422		
				30.5%	-26.6%	30.9%	-28.6%	
Idoff	0.3_0.6	0.06	pA/μm	3478		3193		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				2.7E+04	-2639	1.6E+04	-2259	
Sub Vt slope	0.3_0.6	0.06	mV/dec	98		101		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1.00	nA/um2	121		30		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.073		0.068		△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	3.26E-01		1.40E-02		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.06	fF/um	2.50E-01		2.30E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.33E+00		1.08		Vrev=0V
Inverter FO=1 Delay	Wn/Wp = 3.6/5	0.06	ps/gate	8.237				RO_Td(ring oscillator delay time) @ V=Vdd,ccoflag=1 (Fan_out=1)
				1.996		-1.6		

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12.4.3 1.0V Low Vt MOS

The following table summarizes the key parameters for 1.0V low V_t MOS in CLN65GP process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition
△L (xl +/-dxl)			μm	-0.019 ± 0.004		-0.016 ± 0.004		
△W(xw+/-dxw)			μm	0.016 ± 0.008		0.016 ± 0.008		
Electrical_ Tox			Å	20 ± 0.6		22.0 ± 0.6		
Vt_gm	1	1	V	0.173		0.194		Vg @Vd=0.05V, Vs=Vb=0
				0.035	-0.036	0.038	-0.040	
	0.3_0.6	0.06		0.321		0.330		
				0.061	-0.059	0.052	-0.055	
	0.12	0.06		0.302		0.319		
				0.089	-0.092	0.088	-0.091	
Vt_lin	1	1	V	0.066		0.148		Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.037	-0.038	0.040	-0.042	
	0.3_0.6	0.06		0.214		0.272		
				0.065	-0.069	0.059	-0.061	
	0.12	0.06		0.188		0.256		
				0.093	-0.100	0.098	-0.100	
Vt_sat	1	1	V	0.036		0.125		Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.3_0.6	0.06		0.116		0.103		
	0.12	0.06		0.090		0.111		
DIBL	0.3_0.6	0.06	V	0.098		0.169		Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	μA/μm	155.6		54.4		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		170.5		71.2		
Id_sat	0.3_0.6	0.06	μA/μm	897		453		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				19.1%	-18.6%	18.2%	-18.0%	
	0.12	0.06		1013		558		
				28.3%	-24.8%	29.4%	-27.1%	
Idoff	0.3_0.6	0.06	pA/μm	39970		64540		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				3.8E+05	-4e4	4.5E+05	-6e4	
Sub Vt slope	0.3_0.6	0.06	mV/dec	95		101		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1.00	nA/um2	120		30		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.061		0.016		△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	1.01E-01		4.14E-04		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.06	fF/um	2.57E-01		2.51E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.207		1.02		Vrev=0V
Inverter FO=1 Delay	Wn/Wp = 3.6/5	0.06	ps/gate	5.686				RO_Td(ring oscillator delay time) @ V=Vdd,ccoflag=1 (Fan_out=1)
				1.168		-0.923		

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12.4.4 1.8V I/O MOS

The following table summarizes the key parameters for 1.8V I/O MOS in CLN65GP process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			μm	-0.055 ± 0.008		-0.055 ± 0.008		
ΔW(xw+/-dxw)			μm	0.007 ± 0.012		0.007 ± 0.012		
Electrical_ Tox			Å	34.0± 1.333		37.0 ± 1.333		
Vt_gm	10	10	V	0.370		0.384		Vg @Vd=0.05V, Vs=Vb=0
				0.051	-0.048	0.052	-0.050	
	10.0	0.2		0.522		0.477		
				0.061	-0.054	0.051	-0.054	
	0.40	0.2		0.528		0.467		
				0.078	-0.071	0.064	-0.066	
Vt_lin	10	10	V	0.317		0.415		Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
				0.055	-0.051	0.055	-0.052	
	10.0	0.2		0.452		0.486		
				0.068	-0.061	0.056	-0.059	
	0.40	0.2		0.458		0.464		
				0.087	-0.076	0.070	-0.071	
Vt_sat	10	10	V	0.304		0.401		Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10.0	0.2		0.368		0.427		
	0.40	0.2		0.371		0.406		
DIBL	10.0	0.2	V	0.084372		-0.05863		Vb=0, Vt_lin-Vt_sat
Id_lin	10.0	0.2	μA/μm	73.355		23.04		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.40	0.2		73.322		29.112		
Id_sat	10.0	0.2	μA/μm	682.57		298.53		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-13.4%	14.9%	-13.6%	15.1%	
	0.40	0.2		690.23		357.32		
				-18.2%	19.4%	-17.3%	19.7%	
Idoff	10.0	0.2	pA/μm	16.311		7.1915		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.117	7.320	0.166	7.622	
Sub Vt slope	10.0	0.2	mV/dec	90.092		99.543		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10.0	0.2	V	0.068		0.135		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10.0	0.2	nA/um	6.474E+01		8.951E-01		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.2	fF/um	2.53E-01		2.18E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.46		1.098		Vrev=0V
Inverter FO=1 Delay	Wn/Wp = 3.6/5	0.2	ps/gate	19.1516				RO_Td(ring oscillator delay time) @ V=Vdd,ccoflag=1 (Fan_out=1)
				3.3717		-2.7854		

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12.4.5 2.5V I/O MOS

The following table summarizes the key parameters for 2.5V I/O MOS in CLN65GP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.01	-0.015±0.01	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.565 0.058 -0.057	0.622 0.053 -0.049	Vg @Vd=0.05V, Vs=Vb=0
	10	0.28		0.544 0.057 -0.056	0.466 0.060 -0.061	
	0.4	0.28		0.518 0.075 -0.077	0.450 0.090 -0.093	
Vt_lin	10	10	V	0.515 0.060 -0.060	0.655 0.057 -0.052	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	0.28		0.522 0.061 -0.060	0.492 0.066 -0.068	
	0.4	0.28		0.474 0.081 -0.082	0.469 0.096 -0.099	
Vt_sat	10	10	V	0.506	0.639	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	0.28		0.434	0.364	
	0.4	0.28		0.385	0.352	
DIBL	10	0.28	V	0.088493	-0.12784	Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.28	uA/um	51.135	16.775	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.28		52.959	20.88	
Id_sat	10	0.28	uA/um	605.32 -11.2% 12.4%	345.66 -11.2% 12.7%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.4	0.28		637.87 -16% 17%	391.18 -14.3% 17.8%	
Ioff	10	0.28	pA/um	2.0132 0.204 5.248	15.514 0.092 11.759	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	0.28	mV/dec	87.229	93.642	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.28	V	0.143	0.154	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.28	nA/um	3.215E+02	4.439E-01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.28	fF/um	2.14E-01	2.32E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.051	1.12	Vrev=0V
Inverter FO=1 Delay	Wn/Wp=5/3.6	0.28	ps/gate	25.3811 2.94	 -2.614	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.4.6 1.8V I/O MOS (2.5V underdrive to 1.8V)

The following table summarizes the key parameters for 1.8V I/O MOS (2.5V underdrive to 1.8V) in CLN65GP process.

	W (μ m)	L (μ m)	Unit	NMOS		PMOS		Definition
△L (xl +/-dxl)			um	-0.015±0.01		-0.015±0.01		
△W(xw+/-dxw)			um	0.007±0.012		0.007±0.012		
Electrical_ Tox			Å	56±3.000		59±3.000		
Vt_gm	10	10	V	0.565		0.622		Vg @Vd=0.05V, Vs=Vb=0
				0.058	-0.057	0.053	-0.049	
	10	0.26		0.487		0.417		
				0.073	-0.073	0.070	-0.065	
	0.4	0.26		0.489		0.405		
				0.083	-0.085	0.100	-0.097	
Vt_lin	10	10	V	0.515		0.655		Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
				0.060	-0.060	0.057	-0.052	
	10	0.26		0.465		0.440		
				0.076	-0.077	0.077	-0.072	
	0.4	0.26		0.443		0.422		
				0.089	-0.091	0.108	-0.104	
Vt_sat	10	10	V	0.507		0.639		Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	0.26		0.370		0.307		
	0.4	0.26		0.352		0.304		
DIBL	10	0.26	V	0.095289		-0.13233		Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.26	uA/um	46.572		15.136		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.26		47.795		18.341		
Id_sat	10	0.26	uA/um	400.22		223.78		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-15.8%	17.8%	-17.4%	20.0%	
	0.4	0.26		419		250.28		
				-21.5%	24.4%	-25.4%	29.3%	
Ioff	10	0.26	pA/um	13.56		115.93		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.123	8.139	0.053	13.922	
Sub Vt slope	10	0.26	mV/dec	87.243		95.579		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.26	V	0.090		0.097		△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.26	nA/um	4.736E+00		1.651E-03		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.26	fF/um	2.00E-01		2.20E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.051		1.12		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.26	ps/gate	28.3246				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				5.5571		-4.4107		

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12.4.7 3.3V I/O MOS (2.5V overdrive to 3.3V)

The following table summarizes the key parameters for 3.3V I/O MOS (2.5V overdrive to 3.3V) in CLN65GP process.

	W (μ m)	L (μ m)	Unit	NMOS		PMOS		Definition
△L (xl +/-dxl)			um	-0.015±0.01		-0.015±0.01		
△W(xw+/-dxw)			um	0.007±0.012		0.007±0.012		
Electrical_ Tox			Å	56±3.000		59±3.000		
Vt_gm	10	10	V	0.565		0.622		Vg @Vd=0.05V, Vs=Vb=0
				0.058	-0.057	0.053	-0.049	
	10	N0.5 / P0.4		0.629		0.566		
				0.055	-0.055	0.054	-0.053	
	0.4	N0.5 / P0.4		0.551		0.555		
				0.065	-0.066	0.073	-0.079	
Vt_lin	10	10	V	0.515		0.655		Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
				0.060	-0.060	0.057	-0.052	
	10	N0.5 / P0.4		0.586		0.598		
				0.058	-0.058	0.058	-0.058	
	0.4	N0.5 / P0.4		0.509		0.568		
				0.072	-0.072	0.088	-0.09	
Vt_sat	10	10	V	0.505		0.639		Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	N0.5 / P0.4		0.556		0.553		
	0.4	N0.5 / P0.4		0.476		0.52		
DIBL	10	N0.5 / P0.4	V	0.030539		-0.04467		Vb=0, Vt_lin-Vt_sat
Id_lin	10	N0.5 / P0.4	uA/um	30.869		13.043		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	N0.5 / P0.4		31.701		16.298		
Id_sat	10	N0.5 / P0.4	uA/um	580.56		350.68		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-8.0%	8.5%	-8.5%	8.5%	
	0.4	N0.5 / P0.4		603.79		405.6		
				-12.5%	12.6%	-15.3%	15.3%	
Ioff	10	N0.5 / P0.4	pA/um	0.012734		0.106		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.252	4.253	0.394	3.653	
Sub Vt slope	10	N0.5 / P0.4	mV/dec	85.863		96.3		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	N0.5 / P0.4	V	0.346		0.304		△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	N0.5 / P0.4	nA/um	2.268E+03		8.478E+00		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	N0.5 / P0.4	fF/um	2.07E-01		2.24E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.051		1.12		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.5	ps/gate	46.425				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				3.277		-2.854		

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12.4.8 1.0V Native MOS

The following table summarizes the key parameters for 1.0V native MOS in CLN65GP process.

	W (μm)	L (μm)	Unit	NMOS	Definition
ΔL (xl +/-dxl)			μm	-0.019 ± 0.005	
ΔW(xw+/-dxw)			μm	0.016 ± 0.008	
Electrical_ Tox			Å	20.0 ± 0.6	
Vt_gm	1	1	V	0.158	Vg @Vd=0.05V, Vs=Vb=0
				0.040 / -0.039	
	1	0.2		0.216	
				0.059 / -0.058	
	0.5	0.2		0.221	
				0.060 / -0.060	
Vt_lin	1	1	V	0.053	Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.041 / -0.042	
	1	0.2		0.113	
				0.060 / -0.060	
	0.5	0.2		0.113	
				0.061 / -0.062	
Vt_sat	1	1	V	0.015	Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	1	0.2		0.066	
	0.5	0.2		0.064	
DIBL	1	0.2	V	0.047	Vb=0, Vt_lin-Vt_sat
Id_lin	1	0.2	μA/μm	81.7	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	0.2		81.8	
Id_sat	1	0.2	μA/μm	565	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				15.8% / -13.9%	
	0.5	0.2		566	
				17.0% / -14.6%	
Idoff	1	0.2	pA/μm	27140	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				1.4E+05 / -2.2E+04	
Sub Vt slope	1	0.2	mV/dec	76	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	122	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	1	0.2	V	0.044	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	1	0.2	nA/um	1.7E-02	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.2	fF/um	3.31E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.162	Vrev=0V

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12.4.9 1.8V Native I/O MOS

The following table summarizes the key parameters for 1.8V native I/O MOS in CLN65GP process.

	W (μm)	L (μm)	Unit	NMOS	Definition
△L (xl +/-dxl)			μm	-0.015 ± 0.008	
△W(xw+/-dxw)			μm	0.007 ± 0.012	
Electrical_ Tox			Å	34.0 ± 1.333	
Vt_gm	10	10	V	-0.115 0.051 / -0.051	Vg @Vd=0.05V, Vs=Vb=0
	10.0	0.8		-0.143 0.071 / -0.072	
	0.5	0.8		-0.113 0.081 / -0.083	
Vt_lin	10	10	V	-0.148 0.053 / -0.053	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10.0	0.8		-0.179 0.074 / -0.075	
	0.5	0.8		-0.144 0.084 / -0.086	
Vt_sat	10	10	V	-0.154	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10.0	0.8		-0.236	
	0.5	0.8		-0.165	
DIBL	10.0	0.8	V	0.056	Vb=0, Vt_lin-Vt_sat
Id_lin	10.0	0.8	μA/μm	27.5	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	0.8		28.2	
Id_sat	10.0	0.8	μA/μm	486 11.4% / -10.4%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.5	0.8		497 15.3% / -13.4%	
Idoff	10.0	0.8	pA/μm	10100000 9.5E+06 / -6.1E+06	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10.0	0.8	mV/dec	76	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10.0	0.8	V	0.057	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10.0	0.8	nA/um	1.22E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.8	fF/um	0.297	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.48E-01	Vrev=0V

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12.4.10 2.5V Native I/O MOS

The following table summarizes the key parameters for 2.5V native I/O MOS in CLN65GP process.

	W (μm)	L (μm)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.03859±0.01	
△W(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	56±3.000	
Vt_gm	10	10	V	-0.066 0.053 -0.055	Vg @Vd=0.05V, Vs=Vb=0
	10	1.2		-0.100 0.081 -0.073	
	0.5	1.2		-0.076 0.084 -0.066	
Vt_lin	10	10	V	-0.130 0.056 -0.060	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	1.2		-0.146 0.084 -0.090	
	0.5	1.2		-0.119 0.088 -0.090	
Vt_sat	10	10	V	-0.136	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	1.2		-0.178	
	0.5	1.2		-0.133	
DIBL	10	1.2	V	0.032358	Vb=0, Vt_lin-Vt_sat
Id_lin	10	1.2	uA/um	18.191	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	1.2		19.123	
Id_sat	10	1.2	uA/um	408.73 -10.6% 12.0%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.5	1.2		415.24 -13.3% 14.9%	
Ioff	10	1.2	pA/um	2.60E+06 0.271 2.686	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	1.2	mV/dec	82.591	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	1.2	V	0.048	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	1.2	nA/um	0.837	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	1.2	fF/um	3.55E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.145159	Vrev=0V

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12.4.113.3V Native I/O MOS

The following table summarizes the key parameters for 3.3V Over-drive Native MOS in CLN65GPLUS process.

	W (μm)	L (μm)	Unit	NMOS	Definition
ΔL (xl +/-dxl)			um	-0.03859±0.01	
ΔW(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	56±3.000	
Vt_gm	10	10	V	-0.067 0.053 -0.055	Vg @Vd=0.05V, Vs=Vb=0
	10	1.2		-0.105 0.081 -0.073	
	0.5	1.2		-0.070 0.084 -0.066	
Vt_lin	10	10	V	-0.131 0.056 -0.060	Vg @Vd=0.05V, Vs=Vb=0 Id=1E-07*W/L
	10	1.2		-0.153 0.084 -0.090	
	0.5	1.2		-0.114 0.088 -0.091	
Vt_sat	10	10	V	-0.137	Vg @Vd=Vdd, Vs=Vb=0 Id=1E-07*W/L
	10	1.2		-0.194	
	0.5	1.2		-0.128	
DIBL	10	1.2	V	0.040437	Vb=0, Vt_lin-Vt_sat
Id_lin	10	1.2	uA/um	19.786	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	1.2		20.823	
Id_sat	10	1.2	uA/um	568.47 -8.8% 9.8%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.5	1.2		585.49 -11.5% 12.7%	
Ioff	10	1.2	pA/um	3.22E+06 0.294 2.573	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	1.2	mV/dec	82.397	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	1.2	V	0.061	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	1.2	nA/um	17.190	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	1.2	fF/um	3.32E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.145159	Vrev=0V

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12.5 Key Parameters of MOS Transistors in CLN65LPG

12.5.1 1.0V LPG/G Standard Vt MOS

The following table summarizes the key parameters for 1.0V LPG/G standard V_t MOS in CLN65LPG process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	-0.013±0.0045		-0.01±0.0045		
ΔW(xw+/-dxw)			um	0.02±0.008		0.02±0.008		
Electrical_ Tox			Å	20.7±0.600		23±0.600		
Vt_gm	1	1	V	0.253		0.276		Vg @Vd=0.05V, Vs=Vb=0
				0.034	-0.034	0.035	-0.041	
	0.3_0.6	0.06		0.310		0.339		
				0.070	-0.073	0.062	-0.083	
	0.12	0.06		0.284		0.329		
				0.094	-0.099	0.094	-0.113	
Vt_lin	1	1	V	0.159		0.239		Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.036	-0.038	0.037	-0.043	
	0.3_0.6	0.06		0.209		0.272		
				0.074	-0.078	0.071	-0.092	
	0.12	0.06		0.182		0.257		
				0.102	-0.106	0.105	-0.124	
Vt_sat	1	1	V	0.144		0.226		Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.3_0.6	0.06		0.117		0.143		
	0.12	0.06		0.107		0.136		
DIBL	0.3_0.6	0.06	V	0.09243		-0.12813		Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	141.5		50.645		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		159.24		65.048		
Id_sat	0.3_0.6	0.06	uA/um	810.54		397.15		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-20.6%	20.8%	-20.7%	-19.8%	
	0.12	0.06		906.99		505.1		
				-27.9%	28.8%	-29.8%	-26.9%	
Isoff	0.3_0.6	0.06	pA/um	30237		22551		Is @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.069	15.176	0.076	12.029	
Sub Vt slope	0.3_0.6	0.06	mV/dec	87.078		100.72		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	59.574		12.083		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.051		0.031		Δ Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	5.182E-02		1.206E-03		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.06	fF/um	1.92E-01		1.88E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.253		1.059		Vrev=0V
Inverter FO=1 Delay	Wn/Wp=5/3.6	0.06	ps/gate	5.84244				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				1.33985		-0.97216		

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12.5.2 1.0V LPG/G High Vt MOS

The following table summarizes the key parameters for 1.0V LPG/G high V_t MOS in CLN65LPG process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.013±0.004	-0.01±0.004	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	20.7±0.600	23±0.600	
Vt_gm	1	1	V	0.402	0.423	Vg @Vd=0.05V, Vs=Vb=0
				0.039 -0.039	0.042 -0.043	
	0.3_0.6	0.06		0.382	0.427	
				0.076 -0.083	0.054 -0.053	
	0.12	0.06		0.356	0.407	
				0.100 -0.110	0.099 -0.091	
Vt_lin	1	1	V	0.293	0.383	Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.042 -0.042	0.042 -0.044	
	0.3_0.6	0.06		0.266	0.355	
				0.080 -0.085	0.067 -0.066	
	0.12	0.06		0.244	0.328	
				0.108 -0.117	0.127 -0.120	
Vt_sat	1	1	V	0.283	0.374	Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.3_0.6	0.06		0.184	0.249	
	0.12	0.06		0.174	0.237	
DIBL	0.3_0.6	0.06	V	0.081374	-0.10653	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	124.49	43.079	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		139.5	56.248	
Id_sat	0.3_0.6	0.06	uA/um	664.07	306.47	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-22.6% 24.2%	-22.8% 22.8%	
	0.12	0.06		760.63	390.12	
				-29.8% 32.8%	-33.5% 33.5%	
Isoff	0.3_0.6	0.06	pA/um	4337.4	1757.7	Is @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.073 15.651	0.069 15.095	
Sub Vt slope	0.3_0.6	0.06	mV/dec	86.084	110.62	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	60.093	12.055	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.069	0.070	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	1.176E-01	1.038E-02	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.06	fF/um	1.88E-01	1.66E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.449	1.084	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.06	ps/gate	8.20699		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				2.12501	-1.47782	

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12.5.3 2.5V IO MOS

The following table summarizes the key parameters for 2.5V IO MOS in CLN65LPG process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.01	-0.015±0.01	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.582	0.614	Vg @Vd=0.05V, Vs=Vb=0
				0.049 -0.049	0.048 -0.048	
	10	0.28		0.578	0.482	
				0.064 -0.064	0.059 -0.059	
	0.4	0.28		0.538	0.462	
				0.076 -0.080	0.090 -0.096	
Vt_lin	10	10	V	0.519	0.652	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
				0.051 -0.051	0.051 -0.051	
	10	0.28		0.522	0.508	
				0.069 -0.069	0.065 -0.066	
	0.4	0.28		0.471	0.473	
				0.084 -0.088	0.097 -0.102	
Vt_sat	10	10	V	0.512	0.638	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	0.28		0.450	0.399	
	0.4	0.28		0.404	0.381	
DIBL	10	0.28	V	0.071567	-0.10992	Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.28	uA/um	51.397	17.426	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.28		55.81	21.834	
Id_sat	10	0.28	uA/um	609.85	348.94	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-11.1% 12.2%	-12.5% 12.7%	
	0.4	0.28		649.7	402.12	
				-15.9% 17.1%	-15.9% 18.8%	
Ioff	10	0.28	pA/um	1.0895	5.1041	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.203 5.314	0.135 8.848	
Sub Vt slope	10	0.28	mV/dec	88.36	90.329	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.28	V	0.171	0.142	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.28	nA/um	2.065E+02	1.214E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.28	fF/um	2.28E-01	2.76E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.1971	1.11168	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.28	ps/gate	27.7184		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				3.5945	-3.0064	

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12.5.4 1.8V I/O MOS (2.5V underdrive to 1.8V)

The following table summarizes the key parameters for 1.8V IO MOS (2.5V underdrive to 3.3V) in CLN65LPG process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.01	-0.015±0.01	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.582 0.049 -0.049	0.614 0.048 -0.048	Vg @Vd=0.05V, Vs=Vb=0
	10	0.26		0.547 0.070 -0.082	0.451 0.060 -0.066	
	0.4	0.26		0.516 0.081 -0.086	0.438 0.092 -0.101	
Vt_lin	10	10	V	0.519 0.051 -0.051	0.652 0.051 -0.051	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	0.26		0.461 0.082 -0.088	0.467 0.075 -0.082	
	0.4	0.26		0.445 0.091 -0.097	0.448 0.099 -0.108	
Vt_sat	10	10	V	0.512	0.638	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	0.26		0.400	0.364	
	0.4	0.26		0.382	0.350	
DIBL	10	0.26	V	0.060776	-0.10226	Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.26	uA/um	45.474	14.953	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.26		49.311	18.918	
Id_sat	10	0.26	uA/um	407.14 -15.2% 19.5%	215.53 -18.1% 22.9%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.4	0.26		428.66 -22.1% 25.9%	257.33 -22.0% 26.3%	
Ioff	10	0.26	pA/um	2.6512 0.179 13.080	14.461 0.093 21.992	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	0.26	mV/dec	93.135	97.56	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.26	V	0.109	0.092	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.26	nA/um	3.585E+00	4.223E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.26	fF/um	2.39E-01	2.88E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.1971	1.11168	Vrev=0V
Inverter FO=1 Delay	Wn/Wp=5/3.6	0.26	ps/gate	32.8299 6.5958	-5.7636	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.5.5 3.3V I/O MOS (2.5V overdrive to 3.3V)

The following table summarizes the key parameters for 3.3V IO MOS (2.5V overdrive to 3.3V) in CLN65LPG process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
ΔL (xl +/- dxl)			um	-0.015±0.01	-0.015±0.01	
ΔW(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.582	0.614	Vg @Vd=0.05V, Vs=Vb=0
				0.049 0.048	-0.048	
	10	N0.5 / P0.4		0.631	0.573	
				0.055 0.054	-0.052	
	0.4	N0.5 / P0.4		0.565	0.552	
				0.063 0.074	-0.071	
Vt_lin	10	10	V	0.519	0.652	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
				0.051 0.051	-0.051	
	10	N0.5 / P0.4		0.576	0.599	
				0.059 0.058	-0.057	
	0.4	N0.5 / P0.4		0.502	0.568	
				0.071 0.080	-0.076	
Vt_sat	10	10	V	0.511	0.638	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	N0.5 / P0.4		0.550	0.559	
	0.4	N0.5 / P0.4		0.478	0.526	
DIBL	10	N0.5 / P0.4	V	0.025269	-0.040243	Vb=0, Vt_lin-Vt_sat
Id_lin	10	N0.5 / P0.4	uA/um	33.308	13.592	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	N0.5 / P0.4		35.493	16.952	
Id_sat	10	N0.5 / P0.4	uA/um	580.45	350.34	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-9.5% -7.7%	7.8%	
	0.4	N0.5 / P0.4		635.2	412.07	
				-16.3% -12.0%	11.8%	
Ioff	10	N0.5 / P0.4	pA/um	0.11914	0.28033	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.433 0.671	1.548	
Sub Vt slope	10	N0.5 / P0.4	mV/dec	96.319	97.722	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	N0.5 / P0.4	V	0.346	0.293	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	N0.5 / P0.4	nA/um	1.479E+03	4.048E+01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	N0.5 / P0.4	fF/um	2.21E-01	2.68E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.1971	1.11168	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	N0.5 / P0.4	ps/gate	47.73		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				6.72	-5.85	

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12.5.6 1.0V LPG/G Native MOS

The following table summarizes the key parameters for 1.0V LPG/G native MOS in CLN65LPG process.

	W (μm)	L (μm)	Unit	NMOS		Definition
△L (xl +/-dxl)			um	-0.013±0.0045		
△W(xw+/-dxw)			um	0.02±0.008		
Electrical_ Tox			Å	20.7±0.600		
Vt_gm	1	1	V	0.086		Vg @Vd=0.05V, Vs=Vb=0
				0.044	-0.045	
	1	0.2		0.155		
				0.072	-0.073	
	0.5	0.2		0.147		
				0.074	-0.074	
Vt_lin	1	1	V	-0.010		Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.046	-0.048	
	1	0.2		0.047		
				0.076	-0.078	
	0.5	0.2		0.045		
				0.077	-0.079	
Vt_sat	1	1	V	-0.048		Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	1	0.2		-0.024		
	0.5	0.2		-0.018		
DIBL	1	0.2	V	0.070807		Vb=0, Vt_lin-Vt_sat
Id_lin	1	0.2	uA/um	84.3		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	0.2		84.86		
Id_sat	1	0.2	uA/um	641.05		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-16.0%	18.6%	
	0.5	0.2		649.14		
				-16.6%	19.5%	
Ioff	1	0.2	pA/um	392210		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.108	7.447	
Sub Vt slope	1	0.2	mV/dec	75.598		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	60.353		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	1	0.2	V	0.024		△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	1	0.2	nA/um	0.009		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.2	fF/um	2.75E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.152		Vrev=0V

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12.5.7 2.5V Native MOS

The following table summarizes the key parameters for 2.5V native MOS in CLN65LPG process.

	W (μm)	L (μm)	Unit	NMOS		Definition
△L (xl +/-dxl)			um	-0.015±0.01		
△W(xw+/-dxw)			um	0.007±0.012		
Electrical_ Tox			Å	56±3.000		
Vt_gm	10	10	V	-0.104		Vg @Vd=0.05V, Vs=Vb=0
				0.053	-0.057	
	10	1.2		-0.120		
				0.082	-0.087	
	0.5	1.2		-0.078		
				0.085	-0.090	
Vt_lin	10	10	V	-0.129		Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
				0.055	-0.060	
	10	1.2		-0.144		
				0.085	-0.090	
	0.5	1.2		-0.098		
				0.088	-0.094	
Vt_sat	10	10	V	-0.136		Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	10	1.2		-0.183		
	0.5	1.2		-0.119		
DIBL	10	1.2	V	0.03899		Vb=0, Vt_lin-Vt_sat
Id_lin	10	1.2	uA/um	19.176		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	1.2		19.982		
Id_sat	10	1.2	uA/um	423.31		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-10.3%	11.4%	
	0.5	1.2		435.71		
				-13.1%	14.8%	
Ioff	10	1.2	pA/um	3.48E+06		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.262	2.483	
Sub Vt slope	10	1.2	mV/dec	76.607		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	1.2	V	0.052		△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	1.2	nA/um	0.718		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	1.2	fF/um	3.11E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.156		Vrev=0V

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12.6 Key Parameters of MOS Transistors in CLN65ULP

12.6.1 1.0V Standard Vt MOS

The following table summarizes the key parameters for 1.00V standard V_t MOS in CLN65ULP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
ΔL (xl +/-dxl)			um	-0.001±0.005	0.002±0.005	
ΔW(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	26±0.670	28±0.670	
Vt_gm	1	1	V	0.450	0.427	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.033 -0.033	-0.036	
	0.3_0.6	0.06		0.519	0.531	
				0.067 -0.080	-0.054	
	0.12	0.06		0.493	0.518	
				0.091 -0.110	-0.090	
Vt_lin	1	1	V	0.340	0.386	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
				0.034 -0.035	-0.036	
	0.3_0.6	0.06		0.402	0.475	
				0.068 -0.082	-0.062	
	0.12	0.06		0.375	0.442	
				0.096 -0.116	-0.097	
Vt_sat	1	1	V	0.322	0.362	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	0.3_0.6	0.06		0.310	0.372	
	0.12	0.06		0.298	0.356	
DIBL	0.3_0.6	0.06	V	0.092527	-0.10306	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	68.963	31.64	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		78.527	42.949	
Id_sat	0.3_0.6	0.06	uA/um	379.88	190.04	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-25.3% 31.9%	-23.9% 25.8%	
	0.12	0.06		438.01	248.79	
				-32.8% 41.7%	-32.9% 39.0%	
Isoff	0.3_0.6	0.06	pA/um	148.39	88.062	Is @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.058 18.374	0.119 15.009	
Sub Vt slope	0.3_0.6	0.06	mV/dec	89.195	102.08	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.12325	0.01092	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.040	0.054	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	1.160E-02	2.320E-04	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.21E-01	2.15E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.251	1.077	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.06	ps/gate	13.7018		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				3.8773	-2.9486	

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12.6.2 1.0V High V_t MOS

The following table summarizes the key parameters for 1.00V_High_Vt MOS in CLN65ULP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.001±0.005	0.002±0.005	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	26±0.670	28±0.670	
Vt_gm	1	1	V	0.583	0.607	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.034 -0.036	-0.034	
	0.3_0.6	0.06		0.624	0.644	
				0.075 -0.085	-0.062	
	0.12	0.06		0.580	0.620	
				0.102 -0.113	-0.093	
Vt_lin	1	1	V	0.463	0.559	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
				0.036 -0.038	-0.035	
	0.3_0.6	0.06		0.502	0.593	
				0.076 -0.079	-0.065	
	0.12	0.06		0.467	0.551	
				0.114 -0.110	-0.096	
Vt_sat	1	1	V	0.452	0.546	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	0.3_0.6	0.06		0.418	0.504	
	0.12	0.06		0.395	0.470	
DIBL	0.3_0.6	0.06	V	0.084343	-0.088833	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	48.968	21.553	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		57.961	30.919	
Id_sat	0.3_0.6	0.06	uA/um	240.75	111.79	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-29.4% 39.2%	-29.0% 35.4%	
	0.12	0.06		296.43	158.16	
				-39.1% 49.8%	-39.8% 50.7%	
Isoff	0.3_0.6	0.06	pA/um	7.2837	3.3001	Is @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.256 5.398	0.252 4.645	
Sub Vt slope	0.3_0.6	0.06	mV/dec	99.523	108.99	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.14203	0.0088854	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.066	0.082	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	1.052E-02	1.809E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.13E-01	1.94E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.472	1.091	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.06	ps/gate	24.9495		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				8.9283	-6.3505	

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12.6.3 1.0V mLow MOS

The following table summarizes the key parameters for 1.00V_mLow_Vt MOS in CLN65ULP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.007±0.005	0.002±0	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	26±0.670	28±0.670	
Vt_gm	1	1	V	0.450	0.427	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.037 -0.037	-0.036	
	0.3_0.6	0.06		0.504	0.535	
				0.082 -0.093	-0.073	
	0.12	0.06		0.475	0.527	
				0.108 -0.124	-0.103	
Vt_lin	1	1	V	0.340	0.386	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
				0.038 -0.038	-0.036	
	0.3_0.6	0.06		0.372	0.475	
				0.085 -0.104	-0.085	
	0.12	0.06		0.371	0.461	
				0.110 -0.147	-0.118	
Vt_sat	1	1	V	0.322	0.362	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	0.3_0.6	0.06		0.280	0.352	
	0.12	0.06		0.274	0.360	
DIBL	0.3_0.6	0.06	V	0.092068	-0.12314	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	75.467	32.702	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		85.715	42.568	
Id_sat	0.3_0.6	0.06	uA/um	417.92	206.94	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-27.5% 32.8%	-26.4% 31.8%	
	0.12	0.06		480.03	253.56	
				-33.6% 42.2%	-36.6% 47.3%	
Isoff	0.3_0.6	0.06	pA/um	428.92	131.46	Is @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.050 29.253	0.075 36.842	
Sub Vt slope	0.3_0.6	0.06	mV/dec	91.411	100.86	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.12246	0.010856	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.041	0.048	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	1.246E-02	2.672E-04	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.21E-01	2.14E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.251	1.077	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.06	ps/gate	12.0886		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				4.2645	-2.99668	

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12.6.4 1.0V Low V_t MOS

The following table summarizes the key parameters for 1.00V_Low_Vt MOS in CLN65ULP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.001±0.005	0.002±0.005	
△W(xw+/-dxw)			um	0.02±0.008	0.02±0.008	
Electrical_ Tox			Å	26±0.670	28±0.670	
Vt_gm	1	1	V	0.308	0.308	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.036 -0.036	-0.032	
	0.3_0.6	0.06		0.414	0.464	
				0.075 -0.084	-0.066	
	0.12	0.06		0.386	0.448	
				0.094 -0.108	-0.110	
Vt_lin	1	1	V	0.212	0.266	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
				0.040 -0.040	-0.036	
	0.3_0.6	0.06		0.314	0.409	
				0.082 -0.094	-0.075	
	0.12	0.06		0.296	0.385	
				0.104 -0.120	-0.114	
Vt_sat	1	1	V	0.192	0.230	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	0.3_0.6	0.06		0.207	0.286	
	0.12	0.06		0.193	0.278	
DIBL	0.3_0.6	0.06	V	0.10675	-0.12241	Vb=0, Vt_lin-Vt_sat
Id_lin	0.3_0.6	0.06	uA/um	85.68	35.276	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.12	0.06		100.34	47.698	
Id_sat	0.3_0.6	0.06	uA/um	504.49	243.15	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-24.1% 28.2%	-22.7% 26.3%	
	0.12	0.06		588.02	313.2	
				-29.1% 36.2%	-29.5% 38.5%	
Isoff	0.3_0.6	0.06	pA/um	2563.3	515.66	Is @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.045 31.949	0.062 21.712	
Sub Vt slope	0.3_0.6	0.06	mV/dec	91.931	100.78	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.14214	0.011068	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.3_0.6	0.06	V	0.032	0.032	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.3_0.6	0.06	nA/um	1.698E-02	3.293E-04	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.3_0.6	0.06	fF/um	2.33E-01	2.26E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.185	1.068	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.06	ps/gate	9.92691		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				2.68709	-1.98779	

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12.6.5 1.8V I/O MOS

The following table summarizes the key parameters for 1.80V MOS in CLN65ULP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.01	-0.015±0.01	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.579 0.050 -0.050	0.642 -0.048	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	10	0.26		0.560 0.067 -0.069	0.506 -0.062	
	0.4	0.26		0.526 0.082 -0.088	0.484 -0.097	
Vt_lin	10	10	V	0.519 0.052 -0.052	0.682 -0.051	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
	10	0.26		0.504 0.072 -0.074	0.530 -0.067	
	0.4	0.26		0.461 0.088 -0.094	0.496 -0.104	
Vt_sat	10	10	V	0.512	0.669	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	0.26		0.416	0.431	
	0.4	0.26		0.386	0.400	
DIBL	10	0.26	V	0.087629	-0.0986	Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.26	uA/um	42.697	14.387	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.26		45.431	17.802	
Id_sat	10	0.26	uA/um	375.65 -14.3% 15.5%	193.98 -15.1% 16.9%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.4	0.26		398.32 -21.2% 22.8%	229.05 -20.5% 24.7%	
Ioff	10	0.26	pA/um	3.9411 0.158 6.646	3.5208 0.180 6.292	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	0.26	mV/dec	90.84	94.472	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.26	V	0.113	0.101	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.26	nA/um	2.903E+00	3.405E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.26	fF/um	2.66E-01	2.81E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.195	1.111	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.26	ps/gate	35.0091 6.2689	-5.1563	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.6.6 2.5V I/O MOS

The following table summarizes the key parameters for 2.50V MOS in CLN65ULP process.

	W (μ m)	L (μ m)	Unit	NMOS	PMOS	Definition
∆L (xl +/-dxl)			um	-0.015±0.01	-0.015±0.01	
∆W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.579 0.050 -0.050	0.642 -0.048	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	10	0.28		0.576 0.066 -0.068	0.515 -0.061	
	0.4	0.28		0.535 0.079 -0.084	0.493 -0.093	
Vt_lin	10	10	V	0.519 0.052 -0.052	0.682 -0.051	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
	10	0.28		0.525 0.070 -0.072	0.541 -0.066	
	0.4	0.28		0.466 0.085 -0.090	0.510 -0.099	
Vt_sat	10	10	V	0.512	0.669	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	0.28		0.430	0.432	
	0.4	0.28		0.391	0.404	
DIBL	10	0.28	V	0.094561	-0.10853	Vb=0, Vt_lin-Vt_sat
Id_lin	10	0.28	uA/um	51.809	17.925	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	0.28		54.581	21.637	
Id_sat	10	0.28	uA/um	605.6 -11.5% 12.2%	342.64 -11.4% 12.7%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.4	0.28		644.25 -16.5% 17.2%	394.07 -15.8% 18.7%	
Ioff	10	0.28	pA/um	1.7285 0.169 6.205	2.4638 0.183 6.250	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	0.28	mV/dec	87.698	91.697	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	0.28	V	0.163	0.146	∆Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	0.28	nA/um	1.897E+02	1.197E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	0.28	fF/um	2.55E-01	2.71E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.195	1.111	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.28	ps/gate	27.5112 3.4405	-2.9534	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.6.7 3.3V I/O MOS

The following table summarizes the key parameters for 3.30V MOS in CLN65ULP process.

	W (μ m)	L (μ m)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.01	-0.015±0.01	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	10	10	V	0.579	0.642	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.050 -0.050	-0.048	
	10	N0.5 / P0.4		0.631	0.609	
				0.057 -0.058	-0.051	
	0.4	N0.5 / P0.4		0.563	0.580	
				0.065 -0.068	-0.074	
Vt_lin	10	10	V	0.519	0.682	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
				0.052 -0.052	-0.051	
	10	N0.5 / P0.4		0.578	0.641	
				0.060 -0.060	-0.056	
	0.4	N0.5 / P0.4		0.503	0.602	
				0.071 -0.073	-0.080	
Vt_sat	10	10	V	0.511	0.669	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	N0.5 / P0.4		0.550	0.604	
	0.4	N0.5 / P0.4		0.474	0.562	
DIBL	10	N0.5 / P0.4	V	0.028083	-0.037659	Vb=0, Vt_lin-Vt_sat
Id_lin	10	N0.5 / P0.4	uA/um	31.488	13.584	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.4	N0.5 / P0.4		33.379	17.015	
Id_sat	10	N0.5 / P0.4	uA/um	570.26	346.27	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-8.8% 9.2%	-8.0% 8.8%	
	0.4	N0.5 / P0.4		628.69	404.57	
				-13.3% 14.0%	-11.6% 13.3%	
Ioff	10	N0.5 / P0.4	pA/um	0.054651	0.47088	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.386 3.207	0.635 1.634	
Sub Vt slope	10	N0.5 / P0.4	mV/dec	91.849	94.158	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	N0.5 / P0.4	V	0.349	0.292	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	N0.5 / P0.4	nA/um	1.465E+03	3.501E+01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	N0.5 / P0.4	fF/um	2.48E-01	2.64E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.195	1.111	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.5	ps/gate	61.3912		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				4.1216	-3.7347	

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12.6.8 1.0V Native MOS

The following table summarizes the key parameters for 1.00V_Native MOS in CLN65ULP process.

	W (μm)	L (μm)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.001±0.005	
△W(xw+/-dxw)			um	0.02±0.008	
Electrical_ Tox			Å	26±0.670	
Vt_gm	1	1	V	0.050 0.045	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	1	0.2		0.115 0.068	
	0.5	0.2		0.121 0.071	
Vt_lin	1	1	V	-0.038 0.048	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
	1	0.2		-0.001 0.074	
	0.5	0.2		0.008 0.076	
Vt_sat	1	1	V	-0.087	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	1	0.2		-0.068	
	0.5	0.2		-0.060	
DIBL	1	0.2	V	0.067607	Vb=0, Vt_lin-Vt_sat
Id_lin	1	0.2	uA/um	69.534	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	0.2		71.091	
Id_sat	1	0.2	uA/um	546.51 -15.4% 16.5%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.5	0.2		575.98 -17.0% 18.6%	
Isoff	1	0.2	pA/um	1.16E+06 0.105 7.577	Is @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	1	0.2	mV/dec	81.673	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	1	1	nA/um2	0.10651	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	1	0.2	V	0.014	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	1	0.2	nA/um	0.005	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	1	0.2	fF/um	4.10E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.155	Vrev=0V

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12.6.9 2.5V Native I/O MOS

The following table summarizes the key parameters for 2.50V_Native MOS in CLN65ULP process.

	W (μ m)	L (μ m)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.03859±0.01	
△W(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	56±3.000	
Vt_gm	10	10	V	-0.066 0.053	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	10	1.2		-0.100 0.080	
	0.5	1.2		-0.076 0.084	
Vt_lin	10	10	V	-0.130 0.056	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
	10	1.2		-0.146 0.084	
	0.5	1.2		-0.118 0.088	
Vt_sat	10	10	V	-0.136	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	1.2		-0.178	
	0.5	1.2		-0.131	
DIBL	10	1.2	V	0.032093	Vb=0, Vt_lin-Vt_sat
Id_lin	10	1.2	uA/um	17.157	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	1.2		18.345	
Id_sat	10	1.2	uA/um	406.44 -10.2% 11.4%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.5	1.2		423.96 -13.2% 14.7%	
Ioff	10	1.2	pA/um	2.59E+06 0.270 2.689	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	1.2	mV/dec	82.6	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	1.2	V	0.047	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	1.2	nA/um	0.828	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	1.2	fF/um	3.31E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.145159	Vrev=0V

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12.6.10 2.5V Native Over-drive 3.3V I/O MOS

The following table summarizes the key parameters for 3.30V_Native MOS in CLN65LP process.

	W (μ m)	L (μ m)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.03859±0.01	
△W(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	56±3.000	
Vt_gm	10	10	V	-0.105 0.052	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	10	1.2		-0.123 0.078	
	0.5	1.2		-0.082 0.084	
Vt_lin	10	10	V	-0.128 0.055	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
	10	1.2		-0.145 0.081	
	0.5	1.2		-0.122 0.088	
Vt_sat	10	10	V	-0.138	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	10	1.2		-0.187	
	0.5	1.2		-0.143	
DIBL	10	1.2	V	0.042186	Vb=0, Vt_lin-Vt_sat
Id_lin	10	1.2	uA/um	18.292	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.5	1.2		20.173	
Id_sat	10	1.2	uA/um	557.11 -8.4% 8.6%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.5	1.2		593.82 -11.3% 11.9%	
Ioff	10	1.2	pA/um	3.44E+06 0.305 2.612	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	10	1.2	mV/dec	75.458	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	1.2	V	0.063	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	10	1.2	nA/um	13.229	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	1.2	fF/um	3.08E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.145159	Vrev=0V

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12.6.11 2.5/5.5V High Voltage MOS

The following table summarizes the key parameters for 2.50/5.5V HV MOS in CLN65LP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
ΔL (xl +/-dxl)			um	-0.015±0	-0.015±0	
ΔW(xw+/-dxw)			um	0.007±0	0.007±0	
Electrical_ Tox			Å	56±0.000	59±0.000	
Vt_gm	10	10	V	0.583	0.643	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.032 -0.033	0.033 -0.033	
	10	N: 0.85 P: 0.6		0.598	0.507	
				0.075 -0.076	0.065 -0.065	
	0.6	N: 0.85 P: 0.6		0.562	0.506	
				0.105 -0.107	0.085 -0.085	
Vt_lin	10	10	V	0.534	0.682	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
				0.035 -0.036	0.035 -0.036	
	10	N: 0.85 P: 0.6		0.527	0.513	
				0.080 -0.08	0.070 -0.070	
	0.6	N: 0.85 P: 0.6		0.486	0.509	
				0.111 -0.111	0.091 -0.090	
Vt_sat	10	10	V	0.528	0.670	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=±5.5V, Vs=Vb=0
	10	N: 0.85 P: 0.6		0.513	0.462	
	0.6	N: 0.85 P: 0.6		0.472	0.458	
DIBL	10	N: 0.85 P: 0.6	V	0.01451	-0.05149	Vb=0, Vt_lin-Vt_sat
Id_lin	10	N: 0.85 P: 0.6	uA/um	26.350	10.430	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.6	N: 0.85 P: 0.6		28.480	11.770	
Id_sat	10	N: 0.85 P: 0.6	uA/um	474.20	277.30	Id @Vg=±2.5V, Vd=±5.5V, Vs=Vb=0
				-11.6% 11.6%	-17.9% 17.9%	
	0.6	N: 0.85 P: 0.6		514.10	300.90	
				-15.5% 15.5%	-18.3% 18.3%	
Ioff	10	N: 0.85 P: 0.6	pA/um	8.2660	12.730	Id @Vg=0, Vd=±5.5V, Vs=Vb=0
				0.100 10.452	0.110 10.094	
Sub Vt slope	10	N: 0.85 P: 0.6	mV/dec	91.298	90.186	Slope @Vd=±5.5V, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	10	N: 0.85 P: 0.6	V	0.413	0.211	ΔVt_sat @Vb=-(±5.5V)/2 and Vb=0
Isub	10	N: 0.85 P: 0.6	nA/um	9.030E-02	8.368E-04	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	10	N: 0.85 P: 0.6	fF/um	4.56E-01	3.66E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cjd			fF/um2	0.141	0.575	Vrev=0V
Cjs			fF/um2	1.195	1.111	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 6.4/6.8	N: 0.85 P: 0.6	ps/gate	97.829		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				14.03	-10.67	

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12.7 Key Parameters of MOS Transistors in CLN55GP

12.7.1 1.0V Standard Vt MOS

The following table summarizes the key parameters for 1.0V standard V_t MOS in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.004	-0.013±0.004	
△W(xw+/-dxw)			um	0.016±0.008	0.016±0.008	
Electrical_ Tox			Å	20.3±0.600	22.3±0.600	
Vt_gm	0.9	0.9	V	0.323	0.286	Vg @Vd=0.05V, Vs=Vb=0
				0.030 -0.031	0.038 -0.039	
	0.27_0.54	0.054		0.386	0.349	
				0.072 -0.077	0.049 -0.055	
	0.108	0.054		0.368	0.345	
				0.099 -0.104	0.084 -0.099	
Vt_lin	0.9	0.9	V	0.224	0.236	Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.030 -0.031	0.040 -0.042	
	0.27_0.54	0.054		0.273	0.293	
				0.071 -0.073	0.054 -0.061	
	0.108	0.054		0.255	0.282	
				0.092 -0.094	0.092 -0.106	
Vt_sat	0.9	0.9	V	0.210	0.222	Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.27_0.54	0.054		0.158	0.171	
	0.108	0.054		0.151	0.180	
DIBL	0.27_0.54	0.054	V	0.11439	-0.12213	Vb=0, Vt_lin-Vt_sat
Id_lin	0.27_0.54	0.054	uA/um	145.58	51.447	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.108	0.054		165.02	67.649	
Id_sat	0.27_0.54	0.054	uA/um	807.09	396.86	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-18.8% 19.6%	-17.3% 19.5%	
	0.108	0.054		948.53	489.48	
				-26.9% 27.2%	-25.6% 30.0%	
Isoff	0.27_0.54	0.054	pA/um	11022	13400	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.079 13.492	0.161 6.798	
Sub Vt slope	0.27_0.54	0.054	mV/dec	87.415	101.15	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	0.9	0.9	nA/um2	89.966	28.008	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.27_0.54	0.054	V	0.056	0.037	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.27_0.54	0.054	nA/um	1.670E-01	6.605E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.27_0.54	0.054	fF/um	1.96E-01	1.61E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.207	1.06	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 4.5/3.24	0.054	ps/gate	5.49448		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				1.06868	-0.86412	

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12.7.2 1.0V High Vt MOS

The following table summarizes the key parameters for 1.0V high V_t MOS in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.004	-0.013±0.004	
△W(xw+/-dxw)			um	0.016±0.008	0.016±0.008	
Electrical_ Tox			Å	20.3±0.600	22.3±0.600	
Vt_gm	0.9	0.9	V	0.474 0.034 -0.037	0.397 0.039 -0.041	Vg @Vd=0.05V, Vs=Vb=0
	0.27_0.54	0.054		0.438 0.080 -0.085	0.408 0.057 -0.062	
	0.108	0.054		0.418 0.109 -0.112	0.408 0.100 -0.110	
Vt_lin	0.9	0.9	V	0.364 0.036 -0.037	0.346 0.041 -0.041	Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.27_0.54	0.054		0.318 0.079 -0.087	0.347 0.059 -0.061	
	0.108	0.054		0.304 0.106 -0.113	0.336 0.096 -0.101	
Vt_sat	0.9	0.9	V	0.354	0.335	Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.27_0.54	0.054		0.218	0.239	
	0.108	0.054		0.213	0.244	
DIBL	0.27_0.54	0.054	V	0.099244	-0.10726	Vb=0, Vt_lin-Vt_sat
Id_lin	0.27_0.54	0.054	uA/um	127.17	46.706	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.108	0.054		147.83	60.915	
Id_sat	0.27_0.54	0.054	uA/um	678.74 -21.3% 21.7%	328.52 -20.6% 20.9%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.108	0.054		815.91 -26.6% 29.5%	406.82 -29.3% 30.5%	
Isoff	0.27_0.54	0.054	pA/um	2694.4 0.095 11.463	1976.6 0.098 8.837	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	0.27_0.54	0.054	mV/dec	92.039	98.915	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	0.9	0.9	nA/um2	89.936	28.106	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.27_0.54	0.054	V	0.066	0.063	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.27_0.54	0.054	nA/um	5.315E-01	2.886E-02	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.27_0.54	0.054	fF/um	1.90E-01	1.50E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.22951	1.05944	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 4.5/3.24	0.054	ps/gate	6.80764 1.5765	 -1.23121	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.7.3 1.0V Low Vt MOS

The following table summarizes the key parameters for 1.0V low V_t MOS in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.004	-0.013±0.004	
△W(xw+/-dxw)			um	0.016±0.008	0.016±0.008	
Electrical_ Tox			Å	20.3±0.600	22.3±0.600	
Vt_gm	0.9	0.9	V	0.190	0.209	Vg @Vd=0.05V, Vs=Vb=0
				0.031 -0.031	0.041 -0.042	
	0.27_0.54	0.054		0.328	0.317	
				0.076 -0.076	0.063 -0.063	
	0.108	0.054		0.301	0.333	
				0.109 -0.120	0.089 -0.105	
Vt_lin	0.9	0.9	V	0.098	0.165	Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
				0.034 -0.034	0.043 -0.045	
	0.27_0.54	0.054		0.223	0.255	
				0.082 -0.082	0.070 -0.071	
	0.108	0.054		0.197	0.259	
				0.117 -0.129	0.098 -0.113	
Vt_sat	0.9	0.9	V	0.062	0.139	Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.27_0.54	0.054		0.104	0.118	
	0.108	0.054		0.089	0.148	
DIBL	0.27_0.54	0.054	V	0.11912	-0.13722	Vb=0, Vt_lin-Vt_sat
Id_lin	0.27_0.54	0.054	uA/um	166.06	55.627	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.108	0.054		183.68	70.437	
Id_sat	0.27_0.54	0.054	uA/um	925.65	449.92	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-18.9% 19.1%	-19.0% 18.6%	
	0.108	0.054		1080	528.41	
				-25.4% 27.7%	-25.9% 28.4%	
Isoff	0.27_0.54	0.054	pA/um	54421	49420	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.054 18.117	0.085 12.171	
Sub Vt slope	0.27_0.54	0.054	mV/dec	91.571	100.88	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	0.9	0.9	nA/um2	88.31	27.878	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.27_0.54	0.054	V	0.044	0.035	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.27_0.54	0.054	nA/um	1.581E-01	9.801E-04	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.27_0.54	0.054	fF/um	1.99E-01	1.66E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.175	1.05	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 4.5/3.24	0.054	ps/gate	4.44714		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				0.89469	-0.70217	

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12.7.4 1.0V Ultra High Vt MOS

The following table summarizes the key parameters for 2.50V MOS in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
ΔL (xl +/- dxl)			um	-0.015±0.004	-0.013±0.004	
ΔW(xw+/-dxw)			um	0.016±0.008	0.016±0.008	
Electrical_ Tox			Å	20.3±0.600	22.3±0.600	
Vt_gm	0.9	0.9	V	0.527	0.424	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
				0.039 -0.039	0.038 -0.040	
	n0.27_p0.54	0.054		0.481	0.416	
				0.083 -0.088	0.056 -0.060	
	0.108	0.054		0.430	0.397	
				0.110 -0.112	0.102 -0.101	
Vt_lin	0.9	0.9	V	0.410	0.369	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=0.05V, Vs=Vb=0
				0.042 -0.041	0.040 -0.041	
	n0.27_p0.54	0.054		0.353	0.357	
				0.082 -0.088	0.059 -0.062	
	0.108	0.054		0.311	0.331	
				0.112 -0.118	0.102 -0.097	
Vt_sat	0.9	0.9	V	0.401	0.358	Constant current method, search Vg @Id=Ith*W/L, Ith=4e-8A, Vd=Vdd, Vs=Vb=0
	n0.27_p0.54	0.054		0.256	0.269	
	0.108	0.054		0.206	0.249	
DIBL	n0.27_p0.54	0.054	V	0.096785	-0.088289	Vb=0, Vt_lin-Vt_sat
Id_lin	0.27_0.54	0.054	uA/um	114.97	44.628	Id @Vg=Vdd,Vd=0.05V, Vs=Vb=0
	0.108	0.054		142.45	63.293	
Id_sat	n0.27_p0.54	0.054	uA/um	612.6	301.34	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-22.0% 21.7%	-19.8% 20.4%	
	0.108	0.054		794.5	419.45	
				-26.7% 29.6%	-29.2% 29.8%	
Isoff	n0.27_p0.54	0.054	pA/um	1116.3	974.14	Is GVg=0 Vd=1Vdd, Vs=Vb=0
				0.101 12.778	0.118 9.092	
Sub Vt slope	n0.27_p0.54	0.054	mV/dec	95.744	99.6	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	0.9	0.9	nA/um2	89.945	28.143	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	n0.27_p0.54	0.054	V	0.081	0.069	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	n0.27_p0.54	0.054	nA/um	9.119E-01	3.351E-02	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	n0.27_p0.54	0.054	fF/um	1.84E-01	1.50E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.45776	1.07267	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.24/4.5	0.054	ps/gate	8.00672		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				1.92988	-1.46472	

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12.7.5 1.8V I/O MOS

The following table summarizes the key parameters for 1.8V I/O MOS in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	-0.044±0.008	-0.044±0.008	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	34±1.333	37±1.333	
Vt_gm	9	9	V	0.374	0.400	Vg @Vd=0.05V, Vs=Vb=0
				0.047 -0.046	0.050 -0.049	
	9	0.18		0.503	0.481	
				0.055 -0.056	0.061 -0.054	
	0.36	0.18		0.502	0.477	
				0.092 -0.096	0.084 -0.070	
Vt_lin	9	9	V	0.312	0.421	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
				0.050 -0.050	0.052 -0.052	
	9	0.18		0.435	0.478	
				0.059 -0.060	0.068 -0.060	
	0.36	0.18		0.419	0.461	
				0.101 -0.105	0.093 -0.078	
Vt_sat	9	9	V	0.297	0.406	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	9	0.18		0.327	0.415	
	0.36	0.18		0.322	0.400	
DIBL	9	0.18	V	0.10792	-0.063833	Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.18	uA/um	76.421	23.74	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	0.18		77.632	28.371	
Id_sat	9	0.18	uA/um	709.88	315.02	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-14.0% 15.4%	-14.3% 16.0%	
	0.36	0.18		742.86	356.9	
				-19.9% 20.4%	-17.8% 19.6%	
Ioff	9	0.18	pA/um	35.347	14.168	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.116 10.008	0.276 5.772	
Sub Vt slope	9	0.18	mV/dec	82.288	100.05	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.18	V	0.061	0.144	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.18	nA/um	5.226E+01	7.543E-01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	0.18	fF/um	1.98E-01	1.75E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.308	1.075	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 4.5/3.24	0.18	ps/gate	16.2243		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				2.9219	-2.4365	

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12.7.6 2.5V I/O MOS

The following table summarizes the key parameters for 2.5V I/O MOS in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	0.002±0.01	0.004±0.01	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	9	9	V	0.579 0.053 -0.054	0.615 0.048 -0.048	Vg @Vd=0.05V, Vs=Vb=0
	9	0.252		0.549 0.102 -0.110	0.438 0.056 -0.056	
	0.36	0.252		0.504 0.144 -0.150	0.428 0.094 -0.102	
Vt_lin	9	9	V	0.518 0.055 -0.056	0.652 0.051 -0.051	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	9	0.252		0.496 0.105 -0.112	0.469 0.062 -0.067	
	0.36	0.252		0.453 0.144 -0.150	0.446 0.101 -0.116	
Vt_sat	9	9	V	0.508	0.637	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	9	0.252		0.385	0.330	
	0.36	0.252		0.352	0.325	
DIBL	9	0.252	V	0.11142	-0.13834	Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.252	uA/um	54.304	17.644	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	0.252		57.388	21.282	
Id_sat	9	0.252	uA/um	627.13 -12.5% 13.3%	361.85 -10.6% 11.7%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.36	0.252		679.1 -15.3% 17.2%	411.4 -14.7% 16.8%	
Ioff	9	0.252	pA/um	8.119 0.007 89.427	55.245 0.076 20.382	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	9	0.252	mV/dec	88.745	95.52	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.252	V	0.124	0.124	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.252	nA/um	3.318E+02	1.209E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	0.252	fF/um	1.85E-01	2.01E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.072	1.2	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 4.5/3.24	0.252	ps/gate	23.0217 2.5574	 -2.3712	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.7.7 3.3V I/O MOS (2.5V Overdrive to 3.3V)

The following table summarizes the key parameters for 3.3V I/O MOS (2.5V overdrive to 3.3V) in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition
△L (xl +/-dxl)			um	0.002±0.01	0.004±0.01	
△W(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	56±3.000	59±3.000	
Vt_gm	9	9	V	0.579 0.053 0.048	0.613 -0.054	Vg @Vd=0.05V, Vs=Vb=0
	9	N0.45 / P0.36		0.654 0.076 0.047	0.581 -0.053	
	0.36	N0.45 / P0.36		0.554 0.116 0.079	0.559 -0.079	
Vt_lin	9	9	V	0.518 0.055 0.051	0.650 -0.052	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	9	N0.45 / P0.36		0.601 0.079 0.053	0.611 -0.058	
	0.36	N0.45 / P0.36		0.504 0.121 0.081	0.574 -0.09	
Vt_sat	9	9	V	0.508	0.634	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	9	N0.45 / P0.36		0.569	0.573	
	0.36	N0.45 / P0.36		0.473	0.533	
DIBL	9	N0.45 / P0.36	V	0.031562	-0.038751	Vb=0, Vt_lin-Vt_sat
Id_lin	9	N0.45 / P0.36	uA/um	34.25	10.997	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	N0.45 / P0.36		36.639	13.788	
Id_sat	9	N0.45 / P0.36	uA/um	583.95 -8.8% -6.9%	290.63 8.5%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.36	N0.45 / P0.36		648.45 -9.9% -8.1%	347.38 15.3%	
Ioff	9	N0.45 / P0.36	pA/um	0.085432 0.290 0.458	0.31438 3.653	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	9	N0.45 / P0.36	mV/dec	92.742	104.55	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	N0.45 / P0.36	V	0.328	0.318	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	N0.45 / P0.36	nA/um	2.225E+03	2.182E+01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	N0.45 / P0.36	fF/um	1.80E-01	1.94E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.072	1.2	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 5/3.6	0.45	ps/gate	52.0956 2.7916	 -2.8718	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.7.8 1.0V Native MOS

The following table summarizes the key parameters for 1.0V native MOS in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.015±0.005	
△W(xw+/-dxw)			um	0.016±0.008	
Electrical_ Tox			Å	20.3±0.600	
Vt_gm	0.9	0.9	V	0.169 0.041 -0.045	Vg @Vd=0.05V, Vs=Vb=0
	0.9	0.18		0.245 0.053 -0.063	
	0.45	0.18		0.243 0.062 -0.073	
Vt_lin	0.9	0.9	V	0.073 0.043 -0.050	Vg @Vd=0.05V, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.9	0.18		0.131 0.057 -0.068	
	0.45	0.18		0.128 0.066 -0.079	
Vt_sat	0.9	0.9	V	0.028	Vg @Vd=Vdd, Vs=Vb=0 Id=4e-8*Wdrawn/Ldrawn
	0.9	0.18		0.085	
	0.45	0.18		0.082	
DIBL	0.9	0.18	V	0.046155	Vb=0, Vt_lin-Vt_sat
Id_lin	0.9	0.18	uA/um	84.419	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.45	0.18		84.53	
Id_sat	0.9	0.18	uA/um	597.48 -16.1% 18.0%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.45	0.18		604.95 -16.9% 19.7%	
Ioff	0.9	0.18	pA/um	18465 0.132 17.656	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	0.9	0.18	mV/dec	77.423	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	0.9	0.9	nA/um2	89.627	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.9	0.18	V	0.020	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.9	0.18	nA/um	0.020	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.9	0.18	fF/um	2.84E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.16373	Vrev=0V

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12.7.9 1.8V Native MOS

The following table summarizes the key parameters for 1.8V native MOS in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.053±0.008	
△W(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	34±1.333	
Vt_gm	9	9	V	-0.109 0.049 -0.050	Vg @Vd=0.05V, Vs=Vb=0
	9	0.72		-0.137 0.053 -0.057	
	0.45	0.72		-0.123 0.052 -0.060	
Vt_lin	9	9	V	-0.139 0.052 -0.054	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	9	0.72		-0.181 0.060 -0.064	
	0.45	0.72		-0.155 0.061 -0.068	
Vt_sat	9	9	V	-0.147	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	9	0.72		-0.249	
	0.45	0.72		-0.191	
DIBL	9	0.72	V	0.067263	Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.72	uA/um	29.04	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.45	0.72		30.523	
Id_sat	9	0.72	uA/um	509.23 -11.1% 12.4%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.45	0.72		525.05 -14.0% 15.9%	
Ioff	9	0.72	pA/um	1.11E+07 0.462 1.909	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	9	0.72	mV/dec	86.336	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.72	V	0.038	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.72	nA/um	6.246	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	0.72	fF/um	2.86E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.14446	Vrev=0V

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12.7.102.5V Native MOS

The following table summarizes the key parameters for 2.5V native MOS in CLN55GP process.

	W (μm)	L (μm)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.014±0.01	
△W(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	56±3.000	
Vt_gm	9	9	V	-0.097 0.058 / -0.063	Vg @Vd=0.05V, Vs=Vb=0
	9	1.2		-0.114 0.079 / -0.092	
	0.45	1.2		-0.094 0.083 / -0.096	
Vt_lin	9	9	V	-0.119 0.060 / -0.066	Vg @Vd=0.05V, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	9	1.2		-0.134 0.082 / -0.095	
	0.45	1.2		-0.124 0.087 / -0.100	
Vt_sat	9	9	V	-0.126	Vg @Vd=Vdd, Vs=Vb=0 Id=1e-7*Wdrawn/Ldrawn
	9	1.2		-0.172	
	0.45	1.2		-0.141	
DIBL	9	1.2	V	0.037253	Vb=0, Vt_lin-Vt_sat
Id_lin	9	1.2	uA/um	18.49	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.45	1.2		20.358	
Id_sat	9	1.2	uA/um	404.57 -11.2% / 13.3%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.45	1.2		430.81 -13.1% / 16.0%	
Ioff	9	1.2	pA/um	3.32E+06 0.247 / 2.731	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	9	1.2	mV/dec	70.826	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	1.2	V	0.047	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	1.2	nA/um	34.992	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	1.2	fF/um	2.89E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.147	Vrev=0V

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12.7.11 3.3V Native MOS

The following table summarizes the key parameters for 3.30V Native MOS in CMN55GP process.

	W (μm)	L (μm)	Unit	NMOS	Definition
△L (xl +/-dxl)			um	-0.014±0.01	
△W(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	56±3.000	
Vt_gm	9	9	V	-0.106 0.058 -0.063	Gm_max method, Vg @Vd=0.05V, Vs=Vb=0
	9	1.08		-0.122 0.082 -0.096	
	0.45	1.08		-0.103 0.087 -0.100	
Vt_lin	9	9	V	-0.124 0.061 -0.065	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=0.05V, Vs=Vb=0
	9	1.08		-0.144 0.086 -0.100	
	0.45	1.08		-0.122 0.091 -0.104	
Vt_sat	9	9	V	-0.132	Constant current method, search Vg @Id=Ith*W/L, Ith=1e-7A, Vd=Vdd, Vs=Vb=0
	9	1.08		-0.197	
	0.45	1.08		-0.149	
DIBL	9	1.08	V	0.05288	Vb=0, Vt_lin-Vt_sat
Id_lin	9	1.08	uA/um	21.302	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.45	1.08		23.545	
Id_sat	9	1.08	uA/um	593.46 -9.6% 11.6%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.45	1.08		633.36 -12.1% 14.7%	
Ioff	9	1.08	pA/um	4.83E+06 0.266 2.584	Id @Vg=0 Vd=1Vdd, Vs=Vb=0
Sub Vt slope	9	1.08	mV/dec	74.342	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	1.08	V	0.069	△Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	1.08	nA/um	84.276	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	1.08	fF/um	2.87E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.147	Vrev=0V

12.7.122.5V Over-drive 3.3V Native MOS

Same as 12.7.11 3.3V Native MOS.

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12.8 Key Parameters of MOS Transistors in CLN55LP

12.8.1 1.2V Standard Vt MOS

The following table summarizes the key parameters for 1.2V standard V_t MOS in CLN55LP process.

	W (µm)	L (µm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	0.0033±0.005		0.0047±0.005		
ΔW(xw+/-dxw)			um	0.016±0.008		0.016±0.008		
Electrical_ Tox			Å	26.9±0.670		28.1±0.670		
Vt_gm	0.9	0.9	V	0.439		0.406		Vg @Vd=0.05V, Vs=Vb=0
				0.034	-0.034	0.038	-0.040	
	0.27_0.54	0.054		0.491		0.506		
				0.061	-0.073	0.056	-0.060	
	0.108	0.054		0.486		0.502		
				0.092	-0.097	0.093	-0.098	
Vt_lin	0.9	0.9	V	0.334		0.370		Vg @Vd=0.05V, Vs=Vb=0
				0.036	-0.035	0.039	-0.040	
	0.27_0.54	0.054		0.400		0.473		
				0.068	-0.077	0.059	-0.063	
	0.108	0.054		0.397		0.444		
				0.098	-0.100	0.090	-0.099	
Vt_sat	0.9	0.9	V	0.315		0.346		Vg @Vd=Vdd, Vs=Vb=0
	0.27_0.54	0.054		0.285		0.341		
	0.108	0.054		0.293		0.333		
DIBL	0.27_0.54	0.054	V	0.11437		-0.13179		Vb=0, Vt_lin-Vt_sat
Id_lin	0.27_0.54	0.054	uA/um	90.977		37.201		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.108	0.054		100.83		51.068		
Id_sat	0.27_0.54	0.054	uA/um	605.89		316.57		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-17.8%	18.0%	-17.6%	18.6%	
	0.108	0.054		669.98		398.83		
				-25.4%	29.2%	-24.2%	27.3%	
Ioff	0.27_0.54	0.054	pA/um	339.57		106.92		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.083	15.786	0.104	17.212	
Sub Vt slope	0.27_0.54	0.054	mV/dec	88.099		94.475		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	0.9	0.9	nA/um2	0.11242		0.019389		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.27_0.54	0.054	V	0.049		0.028		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.27_0.54	0.054	nA/um	4.154E-01		3.142E-03		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.27_0.54	0.054	fF/um	1.67E-01		1.49E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.759		1.074		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.24/4.5	0.054	ps/gate	8.06475				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				1.64936		-1.3724		

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12.8.2 1.2V High V_t MOS

The following table summarizes the key parameters for 1.20V_High_Vt MOS in CLN55LP process.

	W (µm)	L (µm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	0.0033±0.005		0.0047±0.005		
ΔW(xw+/-dxw)			um	0.016±0.008		0.016±0.008		
Electrical_ Tox			Å	26.9±0.670		28.1±0.670		
Vt_gm	0.9	0.9	V	0.608		0.581		Vg @Vd=0.05V, Vs=Vb=0
				0.036	-0.037	0.035	-0.036	
	0.27_0.54	0.054		0.603		0.622		
				0.070	-0.071	0.060	-0.063	
	0.108	0.054		0.592		0.618		
				0.091	-0.097	0.089	-0.090	
Vt_lin	0.9	0.9	V	0.493		0.528		Vg @Vd=0.05V, Vs=Vb=0
				0.038	-0.040	0.037	-0.037	
	0.27_0.54	0.054		0.503		0.585		
				0.079	-0.080	0.065	-0.070	
	0.108	0.054		0.490		0.557		
				0.106	-0.107	0.097	-0.098	
Vt_sat	0.9	0.9	V	0.482		0.513		Vg @Vd=Vdd, Vs=Vb=0
	0.27_0.54	0.054		0.392		0.489		
	0.108	0.054		0.395		0.485		
DIBL	0.27_0.54	0.054	V	0.11138		-0.09615		Vb=0, Vt_lin-Vt_sat
Id_lin	0.27_0.54	0.054	uA/um	73.459		29.88		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.108	0.054		83.092		41.75		
Id_sat	0.27_0.54	0.054	uA/um	449.93		208.93		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-19.0%	19.8%	-19.7%	22.0%	
	0.108	0.054		511.41		274.05		
				-27.7%	29.5%	-26.3%	30.0%	
Ioff	0.27_0.54	0.054	pA/um	23.846		4.3611		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.263	5.122	0.589	2.849	
Sub Vt slope	0.27_0.54	0.054	mV/dec	91.29		91.842		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	0.9	0.9	nA/um2	0.10542		0.017258		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.27_0.54	0.054	V	0.068		0.091		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.27_0.54	0.054	nA/um	2.967E-01		4.426E-03		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.27_0.54	0.054	fF/um	1.57E-01		1.22E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	2.072		1.082		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.24/4.5	0.054	ps/gate	12.2224				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				2.8607		-2.32079		

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12.8.3 1.2V Low V_t MOS

The following table summarizes the key parameters for 1.20V_Low_Vt MOS in CLN55LP process.

	W (µm)	L (µm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	0.0033±0.005		0.0047±0.005		
ΔW(xw+/-dxw)			um	0.016±0.008		0.016±0.008		
Electrical_ Tox			Å	26.9±0.670		28.1±0.670		
Vt_gm	0.9	0.9	V	0.294		0.302		Vg @Vd=0.05V, Vs=Vb=0
				0.039	-0.038	0.037	-0.038	
	0.27_0.54	0.054		0.391		0.429		
				0.075	-0.076	0.065	-0.071	
	0.108	0.054		0.408		0.429		
				0.093	-0.108	0.107	-0.095	
Vt_lin	0.9	0.9	V	0.199		0.265		Vg @Vd=0.05V, Vs=Vb=0
				0.040	-0.040	0.039	-0.040	
	0.27_0.54	0.054		0.296		0.400		
				0.082	-0.084	0.068	-0.077	
	0.108	0.054		0.314		0.382		
				0.101	-0.116	0.106	-0.106	
Vt_sat	0.9	0.9	V	0.168		0.234		Vg @Vd=Vdd, Vs=Vb=0
	0.27_0.54	0.054		0.174		0.248		
	0.108	0.054		0.198		0.254		
DIBL	0.27_0.54	0.054	V	0.12203		-0.15212		Vb=0, Vt_lin-Vt_sat
Id_lin	0.27_0.54	0.054	uA/um	103.3		41.225		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.108	0.054		113.18		56.048		
Id_sat	0.27_0.54	0.054	uA/um	741.08		380.27		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-18.4%	18.6%	-18.1%	18.5%	
	0.108	0.054		804.15		483.78		
				-25.3%	29.2%	-24.6%	27.9%	
Ioff	0.27_0.54	0.054	pA/um	7330.7		1502.2		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.073	13.298	0.087	13.012	
Sub Vt slope	0.27_0.54	0.054	mV/dec	88.471		96.51		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	0.9	0.9	nA/um2	0.12654		0.020271		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.27_0.54	0.054	V	0.030		0.019		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.27_0.54	0.054	nA/um	1.295E+00		4.471E-03		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.27_0.54	0.054	fF/um	1.73E-01		1.53E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.523		1.079		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.24/4.5	0.054	ps/gate	6.28757				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				1.3341		-1.07299		

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12.8.4 1.8V I/O MOS

The following table summarizes the key parameters for 1.80V MOS in CLN55LP process.

	W (µm)	L (µm)	Unit	NMOS	PMOS	Definition
ΔL (xl +/-dxl)			um	0.005±0.01	0.01±0.01	
ΔW(xw+/-dxw)			um	0.007±0.012	0.007±0.012	
Electrical_ Tox			Å	60.69±3.000	63.75±3.000	
Vt_gm	9	9	V	0.602 0.050 -0.050	0.637 0.048 -0.049	Vg @Vd=0.05V, Vs=Vb=0
	9	0.234		0.539 0.076 -0.078	0.473 0.062 -0.067	
	0.36	0.234		0.509 0.079 -0.084	0.467 0.087 -0.094	
Vt_lin	9	9	V	0.534 0.051 -0.051	0.671 0.051 -0.052	Vg @Vd=0.05V, Vs=Vb=0
	9	0.234		0.467 0.084 -0.086	0.490 0.072 -0.078	
	0.36	0.234		0.436 0.093 -0.098	0.472 0.102 -0.111	
Vt_sat	9	9	V	0.524	0.655	Vg @Vd=Vdd, Vs=Vb=0
	9	0.234		0.370	0.376	
	0.36	0.234		0.348	0.370	
DIBL	9	0.234	V	0.096604	-0.11322	Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.234	uA/um	43.796	14.887	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	0.234		46.532	17.499	
Id_sat	9	0.234	uA/um	395.41 -15.7% 16.9%	211.48 -14.5% 16.8%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.36	0.234		419.05 -20.9% 22.6%	236.65 -19.9% 25.3%	
Ioff	9	0.234	pA/um	15.564 0.080 12.522	13.183 0.088 13.106	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	9	0.234	mV/dec	87.565	92.778	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.234	V	0.094	0.094	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.234	nA/um	1.258E+01	1.979E-02	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	0.234	fF/um	2.36E-01	2.42E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.192	1.093	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.24/4.5	0.234	ps/gate	30.2773 5.6252	-4.7051	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

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12.8.5 2.5V I/O MOS

The following table summarizes the key parameters for 2.50V MOS in CLN55LP process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	0.005±0.01		0.01±0.01		
ΔW(xw+/-dxw)			um	0.007±0.012		0.007±0.012		
Electrical_ Tox			Å	60.69±3.000		63.75±3.000		
Vt_gm	9	9	V	0.602		0.637		Vg @Vd=0.05V, Vs=Vb=0
				0.050	-0.050	0.048	-0.049	
	9	0.252		0.585		0.503		
				0.066	-0.067	0.058	-0.062	
	0.36	0.252		0.532		0.484		
				0.077	-0.083	0.088	-0.094	
Vt_lin	9	9	V	0.534		0.671		Vg @Vd=0.05V, Vs=Vb=0
				0.051	-0.051	0.051	-0.052	
	9	0.252		0.520		0.528		
				0.071	-0.073	0.064	-0.067	
	0.36	0.252		0.471		0.503		
				0.084	-0.090	0.095	-0.101	
Vt_sat	9	9	V	0.524		0.655		Vg @Vd=Vdd, Vs=Vb=0
	9	0.252		0.426		0.413		
	0.36	0.252		0.386		0.394		
DIBL	9	0.252	V	0.09387		-0.11549		Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.252	uA/um	49.743		17.516		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	0.252		53.395		21.216		
Id_sat	9	0.252	uA/um	601.53		339.37		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-11.5%	12.2%	-11.1%	12.6%	
	0.36	0.252		644.09		388.36		
				-16.5%	17.2%	-15.9%	18.6%	
Ioff	9	0.252	pA/um	1.9799		2.5349		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.178	6.197	0.168	7.084	
Sub Vt slope	9	0.252	mV/dec	85.001		88.416		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.252	V	0.146		0.138		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.252	nA/um	2.930E+02		7.893E-01		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	0.252	fF/um	2.25E-01		2.30E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.192		1.093		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.24/4.5	0.252	ps/gate	26.0542				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				2.8744		-2.5745		

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12.8.6 3.3V I/O MOS

The following table summarizes the key parameters for 3.30V MOS in CLN55LP process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	0.005±0.01		0.01±0.01		
ΔW(xw+/-dxw)			um	0.007±0.012		0.007±0.012		
Electrical_ Tox			Å	60.69±3.000		63.75±3.000		
Vt_gm	9	9	V	0.602		0.637		Vg @Vd=0.05V, Vs=Vb=0
				0.050	-0.050	0.048	-0.049	
	9	0.45(n)/0.36(p)		0.642		0.584		
				0.057	-0.058	0.052	-0.054	
	0.36	0.45(n)/0.36(p)		0.575		0.561		
				0.065	-0.068	0.074	-0.077	
Vt_lin	9	9	V	0.534		0.671		Vg @Vd=0.05V, Vs=Vb=0
				0.051	-0.052	0.051	-0.052	
	9	0.45(n)/0.36(p)		0.590		0.617		
				0.059	-0.060	0.057	-0.059	
	0.36	0.45(n)/0.36(p)		0.513		0.580		
				0.071	-0.073	0.080	-0.084	
Vt_sat	9	9	V	0.523		0.655		Vg @Vd=Vdd, Vs=Vb=0
	9	0.45(n)/0.36(p)		0.559		0.568		
	0.36	0.45(n)/0.36(p)		0.481		0.534		
DIBL	9	0.45(n)/0.36(p)	V	0.030586		0.04919		Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.45(n)/0.36(p)	uA/um	33.277		14.54		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	0.45(n)/0.36(p)		36.468		18.2		
Id_sat	9	0.45(n)/0.36(p)	uA/um	588.88		370.9		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-8.1%	8.6%	-6.9%	8.5%	
	0.36	0.45(n)/0.36(p)		649.93		435.1		
				-13.1%	14.0%	-12.5%	14.3%	
Ioff	9	0.45(n)/0.36(p)	pA/um	0.065646		0.3706		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.521	2.607	0.653	1.782	
Sub Vt slope	9	0.45(n)/0.36(p)	mV/dec	90.514		93.56574		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.45(n)/0.36(p)	V	0.336		0.289		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.45(n)/0.36(p)	nA/um	1.325E+03		6.717E+00		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	0.45(n)/0.36(p)	fF/um	2.18E-01		2.22E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.192		1.093		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.24/4.5	0.45	ps/gate	51.7106				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				3.1824		-2.9458		

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12.8.7 2.5V under drive 1.8V I/O MOS

The following table summarizes the key parameters for 2.5V under drive 1.80V MOS in CLN55LP process.

	W (µm)	L (µm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	0.005±0.01		0.01±0.01		
ΔW(xw+/-dxw)			um	0.007±0.012		0.007±0.012		
Electrical_ Tox			Å	60.69±3.000		63.75±3.000		
Vt_gm	9	9	V	0.602		0.637		Vg @Vd=0.05V, Vs=Vb=0
				0.050	-0.050	0.048	-0.049	
	9	0.234		0.539		0.473		
				0.076	-0.078	0.062	-0.067	
	0.36	0.234		0.509		0.467		
				0.079	-0.084	0.087	-0.094	
Vt_lin	9	9	V	0.534		0.671		Vg @Vd=0.05V, Vs=Vb=0
				0.051	-0.051	0.051	-0.052	
	9	0.234		0.467		0.490		
				0.084	-0.086	0.072	-0.078	
	0.36	0.234		0.436		0.472		
				0.093	-0.098	0.102	-0.111	
Vt_sat	9	9	V	0.524		0.655		Vg @Vd=Vdd, Vs=Vb=0
	9	0.234		0.370		0.376		
	0.36	0.234		0.348		0.370		
DIBL	9	0.234	V	0.096604		-0.11322		Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.234	uA/um	43.796		14.887		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	0.234		46.532		17.499		
Id_sat	9	0.234	uA/um	395.41		211.48		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-15.7%	16.9%	-14.5%	16.8%	
	0.36	0.234		419.05		236.65		
				-20.9%	22.6%	-19.9%	25.3%	
Ioff	9	0.234	pA/um	15.564		13.183		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.080	12.522	0.088	13.106	
Sub Vt slope	9	0.234	mV/dec	87.565		92.778		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.234	V	0.094		0.094		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.234	nA/um	1.258E+01		1.979E-02		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	0.234	fF/um	2.36E-01		2.42E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.192		1.093		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.24/4.5	0.234	ps/gate	30.2773				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				5.6252		-4.7051		

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12.8.8 2.5V over drive 3.3V I/O MOS

The following table summarizes the key parameters for 2.5V over drive 3.30V MOS in CLN55LP process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition
ΔL (xl +/-dxl)			um	0.005±0.01		0.01±0.01		
ΔW(xw+/-dxw)			um	0.007±0.012		0.007±0.012		
Electrical_ Tox			Å	60.69±3.000		63.75±3.000		
Vt_gm	9	9	V	0.602		0.637		Vg @Vd=0.05V, Vs=Vb=0
				0.050	-0.050	0.048	-0.049	
	9	0.45(n)/0.36(p)		0.642		0.584		
				0.057	-0.058	0.052	-0.054	
	0.36	0.45(n)/0.36(p)		0.575		0.561		
				0.065	-0.068	0.074	-0.077	
Vt_lin	9	9	V	0.534		0.671		Vg @Vd=0.05V, Vs=Vb=0
				0.051	-0.052	0.051	-0.052	
	9	0.45(n)/0.36(p)		0.590		0.617		
				0.059	-0.060	0.057	-0.059	
	0.36	0.45(n)/0.36(p)		0.513		0.580		
				0.071	-0.073	0.080	-0.084	
Vt_sat	9	9	V	0.523		0.655		Vg @Vd=Vdd, Vs=Vb=0
	9	0.45(n)/0.36(p)		0.559		0.568		
	0.36	0.45(n)/0.36(p)		0.481		0.534		
DIBL	9	0.45(n)/0.36(p)	V	0.030586		0.04919		Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.45(n)/0.36(p)	uA/um	33.277		14.54		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	0.45(n)/0.36(p)		36.468		18.2		
Id_sat	9	0.45(n)/0.36(p)	uA/um	588.88		370.9		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-8.1%	8.6%	-6.9%	8.5%	
	0.36	0.45(n)/0.36(p)		649.93		435.1		
				-13.1%	14.0%	-12.5%	14.3%	
Ioff	9	0.45(n)/0.36(p)	pA/um	0.065646		0.3706		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.521	2.607	0.653	1.782	
Sub Vt slope	9	0.45(n)/0.36(p)	mV/dec	90.514		93.56574		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.45(n)/0.36(p)	V	0.336		0.289		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.45(n)/0.36(p)	nA/um	1.325E+03		6.717E+00		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	0.45(n)/0.36(p)	fF/um	2.18E-01		2.22E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	1.192		1.093		Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.24/4.5	0.45	ps/gate	51.7106				RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				3.1824		-2.9458		

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12.8.9 1.2V Native MOS

The following table summarizes the key parameters for 1.20V_Native MOS in CLN55LP process.

	W (µm)	L (µm)	Unit	NMOS	Definition
ΔL (xl +/-dxl)			um	0.0033±0.005	
ΔW(xw+/-dxw)			um	0.016±0.008	
Electrical_ Tox			Å	26.9±0.670	
Vt_gm	0.9	0.9	V	0.095 0.045 -0.051	Vg @Vd=0.05V, Vs=Vb=0
	0.9	0.18		0.179 0.070 -0.077	
	0.45	0.18		0.178 0.071 -0.080	
Vt_lin	0.9	0.9	V	0.002 0.048 -0.053	Vg @Vd=0.05V, Vs=Vb=0
	0.9	0.18		0.076 0.074 -0.081	
	0.45	0.18		0.071 0.076 -0.086	
Vt_sat	0.9	0.9	V	-0.034	Vg @Vd=Vdd, Vs=Vb=0
	0.9	0.18		0.016	
	0.45	0.18		0.013	
DIBL	0.9	0.18	V	0.060291	Vb=0, Vt_lin-Vt_sat
Id_lin	0.9	0.18	uA/um	75.773	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.45	0.18		76.713	
Id_sat	0.9	0.18	uA/um	645.81 -13.0% 13.6%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.45	0.18		665.82 -14.6% 15.6%	
Ioff	0.9	0.18	pA/um	141790 0.099 9.974	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	0.9	0.18	mV/dec	79.261	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	0.9	0.9	nA/um2	0.1326	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.9	0.18	V	0.013	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	0.9	0.18	nA/um	0.077	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.9	0.18	fF/um	2.50E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.1596	Vrev=0V

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12.8.10 2.5V Native I/O MOS

The following table summarizes the key parameters for 2.50V_Native MOS in CLN55LP process.

	W (µm)	L (µm)	Unit	NMOS	Definition
ΔL (xl +/-dxl)			um	0.005±0.01	
ΔW(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	60.69±3.000	
Vt_gm	9	9	V	-0.101 0.054 -0.058	Vg @Vd=0.05V, Vs=Vb=0
	9	1.08		-0.109 0.081 -0.087	
	0.45	1.08		-0.087 0.085 -0.087	
Vt_lin	9	9	V	-0.121 0.055 -0.060	Vg @Vd=0.05V, Vs=Vb=0
	9	1.08		-0.131 0.083 -0.089	
	0.45	1.08		-0.112 0.088 -0.090	
Vt_sat	9	9	V	-0.129	Vg @Vd=Vdd, Vs=Vb=0
	9	1.08		-0.174	
	0.45	1.08		-0.139	
DIBL	9	1.08	V	0.043521	Vb=0, Vt_lin-Vt_sat
Id_lin	9	1.08	uA/um	18.853	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.45	1.08		20.912	
Id_sat	9	1.08	uA/um	418.12 -10.1% 11.4%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.45	1.08		447.12 -13.2% 14.7%	
Ioff	9	1.08	pA/um	3.47E+06 0.277 2.420	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	9	1.08	mV/dec	68.94	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	1.08	V	0.052	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	1.08	nA/um	9.628	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	1.08	fF/um	3.17E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.154	Vrev=0V

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TSMC Confidential 833462 USCVISIVMOSIS 12/16/2016

12.8.11 2.5V Native Over-drive 3.3V I/O MOS

The following table summarizes the key parameters for 3.30V_Native MOS in CLN55LP process.

	W (µm)	L (µm)	Unit	NMOS	Definition
ΔL (xl +/-dxl)			um	0.005±0.01	
ΔW(xw+/-dxw)			um	0.007±0.012	
Electrical_ Tox			Å	60.69±3.000	
Vt_gm	9	9	V	-0.101 0.053 -0.056	Vg @Vd=0.05V, Vs=Vb=0
	9	1.08		-0.109 0.079 -0.085	
	0.45	1.08		-0.087 0.084 -0.086	
Vt_lin	9	9	V	-0.121 0.055 -0.058	Vg @Vd=0.05V, Vs=Vb=0
	9	1.08		-0.131 0.082 -0.088	
	0.45	1.08		-0.112 0.087 -0.089	
Vt_sat	9	9	V	-0.130	Vg @Vd=Vdd, Vs=Vb=0
	9	1.08		-0.185	
	0.45	1.08		-0.145	
DIBL	9	1.08	V	0.054015	Vb=0, Vt_lin-Vt_sat
Id_lin	9	1.08	uA/um	19.859	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.45	1.08		22.526	
Id_sat	9	1.08	uA/um	570.3 -8.4% 8.7%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.45	1.08		614.64 -11.3% 12.0%	
Ioff	9	1.08	pA/um	4.00E+06 0.311 2.287	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	9	1.08	mV/dec	68.695	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um2	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	1.08	V	0.070	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	1.08	nA/um	66.700	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9	1.08	fF/um	3.16E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um2	0.154	Vrev=0V

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12.9 Key Parameters for Bipolar

12.9.1 CLN65LP

The following table summarizes the key parameters for bipolar.

Device	Parameter	TT	SS	FF
PNP10	Vbe	0.6439	0.6492	0.6404
	beta	0.8859	0.7580	1.0115
PNP5	Vbe	0.6433	0.6490	0.6396
	beta	1.0064	0.8757	1.1285
PNP2	Vbe	0.6406	0.6465	0.6368
	beta	1.5012	1.2759	1.7266

Vbe : VB=VC=0, IE=1e-8*Area
Beta : VB=VC=0, IE=1e-8*Area

Device	Parameter	TT	SS	FF
NPN10	Vbe	0.6428	0.6497	0.6381
	beta	3.8741	3.4263	4.2718
NPN5	Vbe	0.6394	0.6463	0.6347
	beta	4.0429	3.5415	4.5021
NPN2	Vbe	0.6330	0.6402	0.6280
	beta	4.0751	3.7746	4.2968

Vbe : VB=VC=0, IE=-1e-8*Area
Beta : VB=VC=0, IE=-1e-8*Area

Device	Parameter	TT	SS	FF
PNP10_S	Vbe	0.6431	0.6484	0.6397
	beta	0.8923	0.7596	1.0244
PNP5_S	Vbe	0.6422	0.6477	0.6387
	beta	1.0251	0.8729	1.1765
PNP2_S	Vbe	0.6406	0.6466	0.6367
	beta	1.5663	1.3445	1.7821

Vbe : VB=VC=0,IE=1e-8*Area
Beta : VB=VC=0,IE=1e-8*Area

Device	Parameter	TT	SS	FF
NPN10_S	Vbe	0.6414	0.6482	0.6367
	beta	4.3467	3.7632	4.9004
NPN5_S	Vbe	0.6393	0.6464	0.6346
	beta	4.5343	4.0321	4.9727
NPN2_S	Vbe	0.6334	0.6407	0.6283
	beta	5.0697	4.7604	5.2793

Vbe : VB=VC=0, IE=-1e-8*Area
Beta : VB=VC=0, IE=-1e-8*Area

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12.9.2 CLN65G

The following table summarizes the key parameters for bipolar.

Device	Parameter	TT	SS	FF
PNP10	Vbe (V)	0.6465	0.6520	0.6429
	Beta	0.7502	0.6560	0.8370
PNP5	Vbe (V)	0.6445	0.6503	0.6407
	Beta	0.7635	0.6774	0.8393
PNP2	Vbe (V)	0.6402	0.6461	0.6363
	Beta	0.8561	0.7619	0.9382

Device	Parameter	TT	SS	FF
NPN10	Vbe (V)	0.6465	0.6533	0.6420
	Beta	4.3179	3.6891	4.9373
NPN5	Vbe (V)	0.6435	0.6503	0.6389
	Beta	4.1453	3.6185	4.6328
NPN2	Vbe (V)	0.6376	0.6446	0.6328
	Beta	3.6832	3.3365	3.9662

Vbe: VB=VC-0, IE= 1uA

Beta: VB=VC-0, IE= 1uA

12.9.3 CLN65GP

The following table summarizes the key parameters for bipolar.

Device	Parameter	TT	SS	FF
PNP10	Vbe (V)	0.6471	0.6524	0.6438
	Beta	0.8547	0.7282	0.9805
PNP5	Vbe (V)	0.6462	0.6516	0.6427
	Beta	0.9506	0.8117	1.0876
PNP2	Vbe (V)	0.6434	0.6494	0.6394
	Beta	1.3662	1.1922	1.5275

Device	Parameter	TT	SS	FF
NPN10	Vbe (V)	0.6462	0.6532	0.6416
	Beta	5.4414	4.6478	6.2238
NPN5	Vbe (V)	0.6435	0.6504	0.6388
	Beta	5.3740	4.6166	6.1084
NPN2	Vbe (V)	0.6374	0.6444	0.6325
	Beta	5.2936	4.6906	5.8263

Vbe: VB=VC-0, IE= 1uA

Beta: VB=VC-0, IE= 1uA

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12.9.4 CLN65LPG

The following table summarizes the key parameters for bipolar.

Device	Parameter	TT	SS	FF
PNP10	Vbe (V)	0.6439	0.6492	0.6404
	Beta	0.8859	0.7580	1.0115
PNP5	Vbe (V)	0.6433	0.6490	0.6396
	Beta	1.0064	0.8757	1.1285
PNP2	Vbe (V)	0.6406	0.6465	0.6368
	Beta	1.5012	1.2759	1.7266

Device	Parameter	TT	SS	FF
NPN10	Vbe (V)	0.6428	0.6497	0.6381
	Beta	3.8741	3.4263	4.2718
NPN5	Vbe (V)	0.6394	0.6463	0.6347
	Beta	4.0429	3.5415	4.5021
NPN2	Vbe (V)	0.6330	0.6402	0.6280
	Beta	4.0751	3.7746	4.2968

Vbe: VB=VC-0, IE= 1uA

Beta: VB=VC-0, IE= 1uA

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12/16/2016

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12.9.5 CLN65ULP

The following table summarizes the key parameters for bipolar.

Device	Parameter	TT	SS	FF
PNP10	Vbe	0.6439	0.6492	0.6404
	beta	0.8859	0.7580	1.0115
PNP5	Vbe	0.6433	0.6490	0.6396
	beta	1.0064	0.8757	1.1285
PNP2	Vbe	0.6406	0.6465	0.6368
	beta	1.5012	1.2759	1.7266

Vbe : VB=VC=0, IE=1E-8A*Area
Beta : VB=VC=0, IE=1E-8A*Area

Device	Parameter	TT	SS	FF
NPN10	Vbe	0.6428	0.6497	0.6381
	beta	3.8741	3.4263	4.2718
NPN5	Vbe	0.6394	0.6463	0.6347
	beta	4.0429	3.5415	4.5021
NPN2	Vbe	0.6330	0.6402	0.6280
	beta	4.0751	3.7746	4.2968

Vbe : VB=VC=0, IE=-1E-8A*Area
Beta : VB=VC=0, IE=-1E-8A*Area

Device	Parameter	TT	SS	FF
PNP10_S	Vbe	0.6431	0.6484	0.6397
	beta	0.8923	0.7596	1.0244
PNP5_S	Vbe	0.6422	0.6477	0.6387
	beta	1.0251	0.8729	1.1765
PNP2_S	Vbe	0.6406	0.6466	0.6367
	beta	1.5663	1.3445	1.7821

Vbe : VB=VC=0,IE=1e-8*Area
Beta : VB=VC=0,IE=1e-8*Area

Device	Parameter	TT	SS	FF
NPN10_S	Vbe	0.6414	0.6482	0.6367
	beta	4.3467	3.7632	4.9004
NPN5_S	Vbe	0.6393	0.6464	0.6346
	beta	4.5343	4.0321	4.9727
NPN2_S	Vbe	0.6334	0.6407	0.6283
	beta	5.0697	4.7604	5.2793

Vbe : VB=VC=0, IE=-1e-8*Area
Beta : VB=VC=0, IE=-1e-8*Area

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12.9.6 CLN55GP

The following table summarizes the key parameters for bipolar.

Device	Parameter	TT	SS	FF
PNP10	Vbe (V)	0.6488	0.6540	0.6455
	Beta	0.7968	0.6807	0.9113
PNP5	Vbe (V)	0.6484	0.6538	0.6449
	Beta	0.9278	0.7927	1.0609
PNP2	Vbe (V)	0.6462	0.6519	0.6425
	Beta	1.3951	1.1857	1.6045

Device	Parameter	TT	SS	FF
NPN10	Vbe (V)	0.6499	0.6569	0.6452
	Beta	4.8892	4.2750	5.4545
NPN5	Vbe (V)	0.6479	0.6548	0.6433
	Beta	4.9907	4.2940	5.6631
NPN2	Vbe (V)	0.6413	0.6482	0.6365
	Beta	4.9813	4.3502	5.5648

Vbe: VB=VC-0, IE= 1uA

Beta: VB=VC-0, IE= 1uA

12.9.7 CLN55LP

The following table summarizes the key parameters for bipolar.

Device	Parameter	TT	SS	FF
PNP10	Vbe	0.6507	0.6559	0.6475
	beta	0.8200	0.6970	0.9430
PNP5	Vbe	0.6492	0.6545	0.6459
	beta	0.9503	0.8077	1.0929
PNP2	Vbe	0.6470	0.6527	0.6432
	beta	1.4494	1.2318	1.6670

Vbe : VB=VC=0, IE=1e-8xArea

Beta : VB=VC=0, IE=1e-8xArea

Device	Parameter	TT	SS	FF
NPN10	Vbe	0.6503	0.6570	0.6459
	beta	3.7795	3.2258	4.3266
NPN5	Vbe	0.6479	0.6546	0.6433
	beta	4.0289	3.4815	4.5750
NPN2	Vbe	0.6409	0.6479	0.6362
	beta	4.6999	4.1330	5.2126

Vbe : VB=VC=0, IE=-1e-8xArea

Beta : VB=VC=0, IE=-1e-8xArea

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12.10 Key Parameters for Junction Diodes

12.10.1 CLN65LP

Device	Junction	CJ	CJSW	CJSWG	**BV**	**N**	**RS**	**IS**	**ISW**
		(F/m2)	(F/m)	(F/m)	**V**		**ohm/m2**	**A/m2**	**A/m**
1.20V_Standard_Vt	N+/PW	1.251E-03	7.90E-11	2.04E-10	9.1	1.02	1.00E-10	2.010E-07	4.17E-13
	P+/NW	1.077E-03	6.40E-11	2.20E-10	9.4	1	1.00E-10	1.820E-07	2.71E-13
	NW/Psub	1.370E-04	7.25E-10	NA	12	1.02	1.00E-10	3.410E-06	1.05E-12
1.20V_High_Vt	N+/PW	1.472E-03	9.50E-11	2.59E-10	8.85	1.02	1.00E-10	1.990E-07	5.10E-13
	P+/NW	1.091E-03	6.40E-11	2.90E-10	9.4	1	1.00E-10	2.010E-07	2.13E-13
1.20V_mLow_Vt	N+/PW	1.251E-03	7.90E-11	2.04E-10	9.1	1.02	1.00E-10	2.010E-07	4.17E-13
	P+/NW	1.077E-03	6.40E-11	2.20E-10	9.4	1	1.00E-10	1.820E-07	2.71E-13
1.20V_Low_Vt	N+/PW	1.185E-03	9.40E-11	1.60E-10	9.3	1.005	1.00E-10	1.700E-07	2.80E-13
	P+/NW	1.068E-03	7.60E-11	1.50E-10	9.4	1.005	1.00E-10	1.150E-07	1.70E-13
1.80V	N+/PW	1.195E-03	1.65E-10	2.08E-10	9	1.02	1.00E-10	1.399E-07	5.69E-13
	P+/NW	1.111E-03	9.70E-11	1.68E-10	9	1.005	1.00E-10	1.130E-07	2.70E-13
2.50V	N+/PW	1.195E-03	1.65E-10	2.08E-10	9	1.02	1.00E-10	1.399E-07	5.69E-13
	P+/NW	1.111E-03	9.70E-11	1.68E-10	9	1.005	1.00E-10	1.130E-07	2.70E-13
3.30V	N+/PW	1.195E-03	1.65E-10	2.08E-10	9	1.02	1.00E-10	1.399E-07	5.69E-13
	P+/NW	1.111E-03	9.70E-11	1.68E-10	9	1.005	1.00E-10	1.130E-07	2.70E-13
2.5V over-drive 3.3V	N+/PW	1.195E-03	1.65E-10	2.08E-10	9	1.02	1.00E-10	1.399E-07	5.69E-13
	P+/NW	1.111E-03	9.70E-11	1.68E-10	9	1.005	1.00E-10	1.130E-07	2.70E-13
2.5V under-drive 1.8V	N+/PW	1.195E-03	1.65E-10	2.08E-10	9	1.02	1.00E-10	1.399E-07	5.69E-13
	P+/NW	1.111E-03	9.70E-11	1.68E-10	9	1.005	1.00E-10	1.130E-07	2.70E-13
1.20V_Native	N+/PW	1.550E-04	1.82E-10	1.43E-10	19	1.02	1.00E-10	5.110E-06	5.46E-12
2.50V_Native	N+/PW	1.452E-04	1.94E-10	1.18E-10	17.8	1.02	1.00E-10	8.430E-07	1.36E-12
2.50V_Native over-drive 3.3V	N+/PW	1.452E-04	1.94E-10	1.18E-10	17.8	1.02	1.00E-10	8.430E-07	1.36E-12
DNW	DNWPSUB	1.150E-04	1.33E-09	NA	11.92	1.02	1.00E-10	3.680E-06	8.80E-12
	PWDNW	7.310E-04	6.46E-10	NA	12.31	1.02	1.00E-10	3.600E-06	1.30E-13
ESD	N+/PW	2.110E-03	1.15E-10	NA	6	1.02	1.00E-10	5.700E-07	6.50E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m2).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diode parameters.

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12.10.2 CLN65G

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m^2)	(F/m)	(F/m)	V		ohm/m^2	A/m^2	A/m
1.0V Standard Vt	N+/PW	1.273E-03	8.50E-11	2.68E-10	8.8	1.02	1.00E-10	1.317E-07	2.40E-13
	P+/NW	1.076E-03	7.30E-11	2.34E-10	9.4	1.005	1.00E-10	1.140E-07	1.48E-13
1.0V High Vt	N+/PW	1.330E-04	7.74E-10	NA	11.73	1.02	4.80E-10	1.349E-05	7.05E-12
	P+/NW	1.300E-03	8.30E-11	3.00E-10	8.8	1.04	1.00E-10	2.485E-07	2.96E-13
1.8V	N+/PW	1.38E-03	1.28E-10	1.66E-10	8.8	1.02	1.0E-10	2.65E-07	7.52E-13
	P+/NW	1.10E-03	7.80E-11	2.20E-10	9.2	1.02	1.0E-10	2.32E-07	4.69E-13
2.5V	N+/PW	1.184E-03	1.62E-10	1.95E-10	8.8	1.02	1.00E-10	1.299E-07	4.89E-13
	P+/NW	1.099E-03	9.60E-11	1.58E-10	9	1.005	1.00E-10	1.177E-07	3.83E-13
1.0V Native	N+/Psub	1.641E-04	1.48E-10	1.32E-10	18.9	1.02	1.00E-10	1.950E-06	2.10E-12
1.8V Native	N+/Psub	1.49E-04	1.82E-10	1.71E-10	18.3	1.02	1.0E-10	5.33E-07	6.59E-12
2.5V Native	N+/PW	1.531E-04	1.63E-10	1.73E-10	18.9	1.02	1.00E-10	8.430E-07	1.36E-12
NW	NW/Psub	1.33E-04	7.74E-10	NA	11.7	1.02	4.8E-10	1.35E-05	7.05E-12
DNW	DNWPSUB	1.10E-04	1.38E-09	NA	11.6	1.02	1.0E-10	1.19E-05	2.95E-11
	PWDNW	7.93E-04	7.05E-10	NA	12.0	1.02	1.0E-10	3.07E-07	1.86E-13
ESD	N+/PW	2.182E-03	1.37E-10	NA	5.82	1.02	1.00E-10	2.549E-07	1.19E-12

The area and perimeter components of junction capacitance listed in the table ara at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m2).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-B ounded Junction (V).
- N, RS, IS, and ISW are forward bias related diode parameters.

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12.10.3 CLN65GP

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m2)	(F/m)	(F/m)	V		ohm/m2	A/m2	A/m
1.0V_Standard_Vt	N+/PW	1.270E-03	6.40E-11	3.05E-10	9.03	1.02	1.00E-10	1.350E-07	2.50E-13
	P+/NW	1.060E-03	6.40E-11	2.55E-10	9.59	1.02	1.00E-10	1.730E-07	1.86E-13
	NW/Psub	1.388E-04	7.49E-10	NA	11.8	1.005	1.00E-10	2.490E-06	8.22E-13
1.0V_High_Vt	N+/PW	1.330E-03	6.69E-11	3.35E-10	8.92	1.005	1.00E-10	1.203E-07	1.67E-13
	P+/NW	1.080E-03	6.40E-11	3.05E-10	9.52	1.005	1.00E-10	1.450E-07	1.57E-13
1.0V_Low_Vt	N+/PW	1.207E-03	6.40E-11	2.97E-10	9.05	1.007	1.00E-10	1.368E-07	1.83E-13
	P+/NW	1.020E-03	6.40E-11	1.95E-10	9.68	1.005	1.00E-10	1.530E-07	4.96E-13
1.8V	N+/PW	1.460E-03	1.19E-10	1.22E-10	8.8	1.02	1.00E-10	5.470E-07	3.95E-12
	P+/NW	1.098E-03	7.80E-11	2.20E-10	9.2	1.02	1.00E-10	2.320E-07	4.69E-13
1.8V (2.5V underdrive to 1.8V)	N+/PW	1.161E-03	1.16E-10	1.62E-10	9.2	1.02	1.00E-10	1.320E-07	6.27E-13
	P+/NW	1.120E-03	9.00E-11	1.70E-10	9	1.02	1.00E-10	1.380E-07	4.11E-13
2.5V	N+/PW	1.161E-03	1.16E-10	1.62E-10	9.2	1.02	1.00E-10	1.320E-07	6.27E-13
	P+/NW	1.120E-03	9.00E-11	1.70E-10	9	1.02	1.00E-10	1.380E-07	4.11E-13
3.3V (2.5V overdrive to 3.3V)	N+/PW	1.161E-03	1.16E-10	1.62E-10	9.2	1.02	1.00E-10	1.320E-07	6.27E-13
	P+/NW	1.120E-03	9.00E-11	1.70E-10	9	1.02	1.00E-10	1.380E-07	4.11E-13
1.0V_Native	N+/PW	1.620E-04	1.27E-10	2.95E-10	19	1.005	1.00E-10	2.250E-06	2.22E-12
1.8V_Native	N+/PW	1.384E-03	1.28E-10	1.76E-10	8.8	1.02	1.00E-10	5.470E-07	3.95E-12
2.5V Native	N+/Psub	1.452E-04	1.69E-10	1.18E-10	19	1.02	1.00E-10	8.430E-07	1.36E-12
3.3V Native (2.5V overdrive to 3.3V)	N+/Psub	1.452E-04	1.69E-10	1.18E-10	19	1.02	1.00E-10	8.430E-07	1.36E-12
NW	NW/Psub	1.39E-04	7.5E-10	NA	11.8	1.01	1.E-10	2.49E-06	8.22E-13
DNW	DNWPSUB	1.150E-04	1.39E-09	NA	11.8	1.005	1.00E-10	2.440E-06	5.88E-12
	PWDNW	7.519E-04	6.68E-10	NA	12.2	1.005	1.00E-10	1.360E-07	2.07E-13
ESD	N+/PW	2.452E-03	1.55E-10	NA	5.4	1.007	1.00E-10	1.129E-07	9.39E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m2).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diodes parameters

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12.10.4 CLN65LPG

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m2)	(F/m)	(F/m)	V		ohm/m2	A/m2	A/m
LPG	N+/PW	1.253E-03	9.70E-11	2.99E-10	9.1	1.005	1.00E-10	5.888E-07	7.32E-13
	P+/NW	1.059E-03	7.47E-11	2.56E-10	9.35	1.005	1.00E-10	4.343E-07	2.37E-13
1.8V	N+/PW	1.197E-03	1.61E-10	1.85E-10	8.7	1.02	1.00E-10	3.705E-07	1.14E-12
	P+/NW	1.112E-03	9.83E-11	1.58E-10	9.4	1.005	1.00E-10	1.190E-07	4.73E-13
2.5V	N+/PW	1.197E-03	1.61E-10	1.85E-10	8.7	1.02	1.00E-10	3.705E-07	1.14E-12
	P+/NW	1.112E-03	9.83E-11	1.58E-10	9.4	1.005	1.00E-10	1.190E-07	4.73E-13
3.3V	N+/PW	1.197E-03	1.61E-10	1.85E-10	8.7	1.02	1.00E-10	3.705E-07	1.14E-12
	P+/NW	1.112E-03	9.83E-11	1.58E-10	9.4	1.005	1.00E-10	1.190E-07	4.73E-13
1.8V(2.5V underdrive to 1.8V)	N+/PW	1.197E-03	1.61E-10	1.85E-10	8.7	1.02	1.00E-10	3.705E-07	1.14E-12
	P+/NW	1.112E-03	9.83E-11	1.58E-10	9.4	1.005	1.00E-10	1.190E-07	4.73E-13
3.3V (2.5V overdrive to 3.3V)	N+/PW	1.197E-03	1.61E-10	1.85E-10	8.7	1.02	1.00E-10	3.705E-07	1.14E-12
	P+/NW	1.112E-03	9.83E-11	1.58E-10	9.4	1.005	1.00E-10	1.190E-07	4.73E-13
1.0V_LPG_Native	N+/PW	1.520E-04	1.78E-10	1.31E-10	18.6	1.005	1.00E-10	1.380E-05	9.50E-12
2.5V_Native	N+/PW	1.560E-04	1.77E-10	1.74E-10	17.8	1.02	1.00E-10	8.430E-07	1.36E-12
ESD	N+/PW	2.182E-03	1.37E-10	NA	5.82	1.02	1.00E-10	2.549E-07	1.19E-12

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m2).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diodes parameters

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12.10.5 CLN65ULP

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m2)	(F/m)	(F/m)	V		ohm/m2	A/m2	A/m
1. 0V_Standard_Vt	N+/PW	1.251E-03	7.90E-11	2.04E-10	9.1	1.02	1.00E-10	2.010E-07	4.17E-13
	P+/NW	1.077E-03	6.40E-11	2.20E-10	9.4	1	1.00E-10	1.820E-07	2.71E-13
	NW/Psub	1.370E-04	7.25E-10	NA	12	1.02	1.00E-10	3.410E-06	1.05E-12
1.0V_High_Vt	N+/PW	1.472E-03	9.50E-11	2.59E-10	8.85	1.02	1.00E-10	1.990E-07	5.10E-13
	P+/NW	1.091E-03	6.40E-11	2.90E-10	9.4	1	1.00E-10	2.010E-07	2.13E-13
1.0V_mLow_Vt	N+/PW	1.251E-03	7.90E-11	2.04E-10	9.1	1.02	1.00E-10	2.010E-07	4.17E-13
	P+/NW	1.077E-03	6.40E-11	2.20E-10	9.4	1	1.00E-10	1.820E-07	2.71E-13
1.0V_Low_Vt	N+/PW	1.185E-03	9.40E-11	1.60E-10	9.3	1.005	1.00E-10	1.700E-07	2.80E-13
	P+/NW	1.068E-03	7.60E-11	1.50E-10	9.4	1.005	1.00E-10	1.150E-07	1.70E-13
1.80V	N+/PW	1.195E-03	1.65E-10	2.08E-10	9	1.02	1.00E-10	1.399E-07	5.69E-13
	P+/NW	1.111E-03	9.70E-11	1.68E-10	9	1.005	1.00E-10	1.130E-07	2.70E-13
2.50V	N+/PW	1.195E-03	1.65E-10	2.08E-10	9	1.02	1.00E-10	1.399E-07	5.69E-13
	P+/NW	1.111E-03	9.70E-11	1.68E-10	9	1.005	1.00E-10	1.130E-07	2.70E-13
3.30V	N+/PW	1.195E-03	1.65E-10	2.08E-10	9	1.02	1.00E-10	1.399E-07	5.69E-13
	P+/NW	1.111E-03	9.70E-11	1.68E-10	9	1.005	1.00E-10	1.130E-07	2.70E-13
1.0V_Native	N+/PW	1.550E-04	1.82E-10	1.43E-10	19	1.02	1.00E-10	5.110E-06	5.46E-12
2.50V_Native	N+/PW	1.452E-04	1.94E-10	1.18E-10	17.8	1.02	1.00E-10	8.430E-07	1.36E-12
DNW	DNWPSUB	1.150E-04	1.33E-09	NA	11.92	1.02	1.00E-10	3.680E-06	8.80E-12
	PWDNW	7.310E-04	6.46E-10	NA	12.31	1.02	1.00E-10	3.600E-06	1.30E-13
ESD	N+/PW	2.110E-03	1.15E-10	NA	6	1.02	1.00E-10	5.700E-07	6.50E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m2).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diode parameters.

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12.10.6 CLN55GP

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m2)	(F/m)	(F/m)	V		ohm/m2	A/m2	A/m
1.0V_Standard_Vt	N+/PW	1.207E-03	6.50E-11	2.93E-10	9.1	1.02	1.00E-10	1.146E-07	1.88E-13
	P+/NW	1.061E-03	6.00E-11	2.78E-10	9.6	1.005	1.00E-10	1.369E-07	1.35E-13
	NW/Psub	1.427E-04	8.00E-10	NA	11.5	1.005	1.00E-10	1.145E-06	1.37E-12
1.0V_High_Vt	N+/PW	1.230E-03	6.52E-11	3.20E-10	9.07	1.005	1.00E-10	9.128E-08	1.49E-13
	P+/NW	1.059E-03	5.93E-11	3.24E-10	9.62	1.005	1.00E-10	1.340E-07	1.40E-13
1.0V_Low_Vt	N+/PW	1.175E-03	6.70E-11	2.71E-10	9.15	1.007	1.00E-10	9.040E-08	1.40E-13
	P+/NW	1.050E-03	6.00E-11	2.39E-10	9.53	1.005	1.00E-10	1.280E-07	1.19E-13
1.8V	N+/PW	1.318E-03	1.10E-10	1.41E-10	8.8	1.02	1.00E-10	9.272E-08	3.26E-13
	P+/NW	1.108E-03	7.10E-11	2.30E-10	9.05	1.02	1.00E-10	1.090E-07	2.25E-13
2.5V	N+/PW	1.077E-03	1.48E-10	1.82E-10	9.2	1.02	1.00E-10	1.240E-07	4.48E-13
	P+/NW	1.126E-03	8.80E-11	1.67E-10	8.8	1.02	1.00E-10	1.300E-07	3.49E-13
3.3V(2.5V overdrive to 3.3V)	N+/PW	1.077E-03	1.48E-10	1.82E-10	9.2	1.02	1.00E-10	1.240E-07	4.48E-13
	P+/NW	1.126E-03	8.80E-11	1.67E-10	8.8	1.02	1.00E-10	1.300E-07	3.49E-13
1.0V_Native	N+/PW	1.637E-04	1.55E-10	1.46E-10	18.4	1.005	1.00E-10	7.470E-07	8.31E-13
1.8V_Native	N+/PW	1.440E-04	2.03E-10	1.19E-10	18.32	1.02	1.00E-10	1.121E-06	1.19E-12
2.5V_Native	N+/PW	1.498E-04	2.00E-10	1.13E-10	17.7	1.04	1.00E-10	1.503E-06	1.75E-12
DNW	DNWPSUB	1.088E-04	1.37E-09	NA	11.45	1.03	1.00E-10	4.674E-06	1.08E-11
	PWDNW	7.752E-04	6.68E-10	NA	11.9	1.005	1.00E-10	1.600E-07	9.55E-14
ESD	N+/PW	1.082E-03	1.35E-10	NA	9.28	1.03	1.00E-10	1.583E-07	2.59E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m2).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diodes parameters

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12.10.7 CLN55LP

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m2)	(F/m)	(F/m)	V		ohm/m2	A/m2	A/m
1.20V_Standard_Vt	N+/PW	1.759E-03	1.30E-10	1.83E-10	8.6	1.02	1.00E-10	1.600E-07	6.00E-13
	P+/NW	1.074E-03	7.20E-11	1.61E-10	9.4	1.02	1.00E-10	1.600E-07	1.52E-12
	NW/Psub	1.579E-04	7.46E-10	NA	12	1.02	1.00E-10	1.110E-06	3.10E-13
1.20V_High_Vt	N+/PW	2.072E-03	1.54E-10	2.09E-10	8	1.02	1.00E-10	3.200E-07	1.30E-12
	P+/NW	1.082E-03	7.10E-11	2.33E-10	9.4	1.02	1.00E-10	2.100E-07	2.00E-12
1.20V_mLow_Vt	N+/PW	1.759E-03	1.30E-10	1.83E-10	8.6	1.02	1.00E-10	1.600E-07	6.00E-13
	P+/NW	1.074E-03	7.20E-11	1.61E-10	9.4	1.02	1.00E-10	1.600E-07	1.52E-12
1.20V_Low_Vt	N+/PW	1.523E-03	1.13E-10	1.56E-10	9	1.02	1.00E-10	3.200E-07	2.00E-15
	P+/NW	1.079E-03	7.10E-11	9.50E-11	9.6	1.02	1.00E-10	2.100E-07	1.80E-13
1.80V	N+/PW	1.192E-03	1.720E-10	1.47e-10	8.8	1.02	1.00E-10	7.000E-07	9.000E-12
	P+/NW	1.093E-03	9.600E-11	1.31E-10	9	1.02	1.00E-10	3.200E-07	4.300E-12
2.50V	N+/PW	1.192E-03	1.720E-10	1.47e-10	8.8	1.02	1.00E-10	7.000E-07	9.000E-12
	P+/NW	1.093E-03	9.600E-11	1.31E-10	9	1.02	1.00E-10	3.200E-07	4.300E-12
3.30V	N+/PW	1.192E-03	1.720E-10	1.47e-10	8.8	1.02	1.00E-10	7.000E-07	9.000E-12
	P+/NW	1.093E-03	9.600E-11	1.31E-10	9	1.02	1.00E-10	3.200E-07	4.300E-12
2.50V under drive 1.8V	N+/PW	1.192E-03	1.720E-10	1.47e-10	8.8	1.02	1.00E-10	7.000E-07	9.000E-12
	P+/NW	1.093E-03	9.600E-11	1.31E-10	9	1.02	1.00E-10	3.200E-07	4.300E-12
2.50V over drive 3.3V	N+/PW	1.192E-03	1.720E-10	1.47e-10	8.8	1.02	1.00E-10	7.000E-07	9.000E-12
	P+/NW	1.093E-03	9.600E-11	1.31E-10	9	1.02	1.00E-10	3.200E-07	4.300E-12
1.20V_Native	N+/PW	1.596E-04	1.60E-10	1.38E-10	17.8	1.02	1.00E-10	1.030E-06	1.10E-12
2.50V_Native	N+/PW	1.540E-04	1.880E-10	1.35E-10	17.75	1.02	1.00E-10	1.800E-06	5.000E-12
2.50V_Native over-drive 3.3V	N+/PW	1.540E-04	1.880E-10	1.35E-10	17.75	1.02	1.00E-10	1.800E-06	5.000E-12
DNW	DNWPSUB	1.309E-04	1.43E-09	NA	12	1.02	1.00E-10	1.100E-06	2.60E-12
	PWDNW	7.497E-04	6.44E-10	NA	12.4	1.02	1.00E-10	2.120E-07	4.00E-14
ESD	N+/PW	2.110E-03	1.15E-10	NA	6	1.02	1.00E-10	5.700E-07	6.50E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m2).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diode parameters.

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12.11 Resistor Models

Several resistor models are included in this model release. The model naming and valid dimension ranges are reported in the Table 12.11.1 and 12.11.2. The model nominal temperature is 25 °C, while the valid temperature range is from –40 to 125 °C. All models contain one typical case (TT_RES) and two corner ones, slow (SS_RES) and fast (FF_RES) corners each.

Most resistors were measured by applying voltages on one node, while grounding the other node and substrate (if connection is available). The voltage sweep was performed from 0 up to +/- 4 V (provided there is no reliability issue). Most of resistance data measured were modeled with the following equation (12.11.1):

$$R(T,V) = R_0 \cdot (1 + TC1 \cdot \delta T + TC2 \cdot \delta T^2) \cdot (1 + VC1 \cdot \delta(V/L) + VC2 \cdot \delta(V/L)^2)$$ **Equation (12-11-1)**

where

δT = T – 25 (in °C),

V (in volt) = the voltage drop across the resistor,

L = the length of the resistor.

R_0 of equation (12-10-1) is the resistance value at 25 °C and an infinitesimal voltage. R_0 is related to sheet resistance, R_{sh}:

where $R_0 = R_{sh} \cdot L/(W - \delta W)$ **Equation (12-11-2)**

W = the layout drawn width

L = the layout drawn length.

δW = the width offset.

The following tables list the median sheet resistance values and their corresponding variations, temperature coefficients, and voltage coefficients. The data was extracted based on the methodology described previously in this section.

Note: An NW diffusion resistor under STI is very subject to CMP variation. Users are recommended to use NW diffusion resistor under OD for their design.

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12.11.1 CLN65LP

Table 12.11.1: Resistor model table for CLN65LP

Film	Valid Width (in um)	Model Naming	Rsh Mean/Range		Unit	TC1	TC2	VC1	VC2
N+ Poly w/I silicide	W>=2.0	rnpolyl	15.06186	-	ohm/sq	0.0018874	-6.41E-07	6.54E-07	1.17E-11
N+ Poly w/I silicide	0.06<=W<2.0	rnpolys	15.06186	-	ohm/sq	0.0021624	-7.21E-07	2.63E-08	4.19E-12
P+ Poly w/I silicide	W>=2.0	rppolyl	14.92552	-	ohm/sq	0.0022507	-9.32E-07	8.25E-07	1.38E-11
P+ Poly w/I silicide	0.06<=W<2.0	rppolys	14.92552	-	ohm/sq	0.0023718	-6.16E-07	8.54E-08	4.18E-12
N+ diff. W/I silicide	W>=2.0	rnodl	15.52195	-	ohm/sq	0.0019054	-5.99E-07	-5.30E-08	3.23E-12
N+ diff. W/I silicide	0.08<=W<2.0	rnods	15.52195	-	ohm/sq	0.0021720	-5.47E-07	4.83E-08	9.73E-13
P+ diff. W/I silicide	W>=2.0	rpodl	14.55118	-	ohm/sq	0.0021324	-9.32E-07	-7.28E-09	3.46E-12
P+ diff. W/I silicide	0.08<=W<2.0	rpods	14.55118	-	ohm/sq	0.0023705	-7.40E-07	-4.25E-09	1.37E-12
N-well under OD	-	rnwod	326.8034	-	ohm/sq	2.43E-03	9.20E-06	0.0021189	0.0005158
N-well under STI	-	rnwsti	595.1748	-	ohm/sq	2.02E-03	9.94E-06	0.0038177	1.03E-04
M1	W/S=0.09/0.45	RM1L	0.0868	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.09/0.09	RM1S	0.16	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.27/0.135	RM1W	0.137	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M2	W/S=0.1/0.5	RM2L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.1/0.1	RM2S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.3/0.13	RM2W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.5	RM3L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.1	RM3S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.3/0.13	RM3W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.5	RM4L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.1	RM4S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.3/0.13	RM4W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.5	RM5L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.1	RM5S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.3/0.13	RM5W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.5	RM6L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.1	RM6S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.3/0.13	RM6W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.5	RM7L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.1	RM7S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.3/0.13	RM7W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M8	W/S=0.4/1.5	RM8L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=0.4/0.4	RM8S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=1.5/0.4	RM8W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/1.5	RM9L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/0.4	RM9S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=1.5/0.4	RM9W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M10 AL RDL	W/S=3/2	RM10	0.021	-	ohm/sq	3.89E-3	-1.50E-7	-	-
Mx	W/S=0.1/0.5	RMXL	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.1/0.1	RMXS	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.3/0.13	RMXW	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
My	W/S=0.2/1	RMYL	0.0326	-	ohm/sq	3.335e-3	-1.142e-7		
My	W/S=0.2/0.2	RMYS	0.0380	-	ohm/sq	3.335e-3	-1.142e-7		
My	W/S=0.6/0.3	RMYW	0.0365	-	ohm/sq	3.335e-3	-1.142e-7		
Mz	W/S=0.4/1.5	RMZL	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-

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Film	Valid Width (in um)	Model Naming	Rsh Mean/Range		Unit	TC1	TC2	VC1	VC2
Mz	W/S=0.4/0.4	RMZS	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mz	W/S=1.5/0.4	RMZW	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mr	W/S=0.5/1.2	RMRL	0.0145	-	ohm/sq	3.27E-03	-3.88E-06	-	-
Mr	W/S=0.5/0.5	RMRS	0.0147	-	ohm/sq	3.27E-03	-3.88E-06	-	-
Mr	W/S=1.2/0.5	RMRW	0.0178	-	ohm/sq	3.27E-03	-3.88E-06	-	-
MAP	W/S=3/2	RMAP	0.021		ohm/sq	3.89E-03	-1.5E-07		
MAP_UT	W/S=3/2	RMAP_UT	0.011		ohm/sq	3.89E-03	-1.5E-07		
Mt		RMT	0.005		ohm/sq	3.41E-03	3.69E-06		

Film	Valid Width (in um)	Model Naming	Rsh Mean/Range		Unit	TC1	TC2	VC1	VC2
M1	-		0.160	+0.0512 / -0.0352	Ohm/sq	2.65E-03	-2.64E-07	NA	NA
M2-7	-		0.140	+0.0420 / -0.0294	Ohm/sq	2.71E-03	-3.48E-07	NA	NA
M8-9	-		0.022	+0.0044 / -0.0035	Ohm/sq	3.63E-03	-1.39E-06	NA	NA
M10 (Al RDL)	-		0.021	+0.0042 / -0.0042	Ohm/sq	3.89E-03	-1.50E-07	NA	NA
RC_N+	-		26	10.4	Ohm/ct	9.49E-04	-4.47E-06	NA	NA
RC_P+	-		26	10.4	Ohm/ct	1.84E-03	6.70E-06	NA	NA
RC_PO(N+)	-		20	8.0	Ohm/ct	1.03E-03	1.63E-07	NA	NA
RC_PO(P+)	-		20	8.0	Ohm/ct	1.11E-03	4.23E-07	NA	NA
RC_VIA1	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA2	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA3	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA4	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA5	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA6	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA7	-		0.22	0.11	Ohm/ct	2.48E-03	1.03E-06	NA	NA
RC_VIA8	-		0.22	0.11	Ohm/ct	2.48E-03	1.03E-06	NA	NA
RC_VIA9	-		0.041	0.0205	Ohm/ct	3.37E-03	-7.91E-08	NA	NA

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12.11.2 CLN65G (M1MxMz process, no My/Mr, x=2~7, z=8~9)

Table 12.11.2: Resistor model table for CLN65G

Film	Valid Width (in μm)	Model Naming	Rsh Mean/Range		Unit	TC1	TC2	VC1	VC2
N+ Poly w/i silicide	W>=2.0	rnpolyl	15.40	-	ohm/sq	2.09E-3	-4.21E-6	3.39E-9	6.01E-14
N+ Poly w/i silicide	0.06<=W<2.0	rnpolys	15.40	-	ohm/sq	2.43E-3	-6.10E-6	4.04E-8	5.83E-13
P+ Poly w/i silicide	W>=2.0	rppolyl	14.82	-	ohm/sq	2.30E-3	-3.32E-6	3.53E-7	7.56E-12
P+ Poly w/i silicide	0.06<=W<2.0	rppolys	14.82	-	ohm/sq	2.61E-3	-5.37E-6	4.28E-8	7.04E-13
N+ diff. w/i silicide	W>=2.0	rnodl	15.25	-	ohm/sq	2.03E-3	-3.42E-6	4.20E-8	6.36E-13
N+ diff. w/i silicide	0.08<=W<2.0	rnods	15.25	-	ohm/sq	2.31E-3	-4.78E-6	2.72E-8	5.53E-14
P+ diff. w/i silicide	W>=2.0	rpodl	14.55	-	ohm/sq	2.19E-3	-2.37E-6	-1.23E-9	4.05E-13
P+ diff. w/i silicide	0.08<=W<2.0	rpods	14.55	-	ohm/sq	2.26E-3	-4.41E-7	2.39E-8	-3.99E-4
N-well under OD	-	rnwod	326.8	-	ohm/sq	2.43E-3	9.20E-6	2.12E-3	5.16E-4
N-well under STI	-	rnwsti	595.2	-	ohm/sq	2.02E-3	9.94E-6	3.82E-3	1.03E-4
M1	W/S=0.09/0.45	RM1L	0.0868	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.09/0.09	RM1S	0.16	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.27/0.135	RM1W	0.137	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M2	W/S=0.1/0.5	RM2L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.1/0.1	RM2S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.3/0.13	RM2W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.5	RM3L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.1	RM3S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.3/0.13	RM3W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.5	RM4L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.1	RM4S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.3/0.13	RM4W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.5	RM5L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.1	RM5S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.3/0.13	RM5W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.5	RM6L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.1	RM6S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.3/0.13	RM6W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.5	RM7L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.1	RM7S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.3/0.13	RM7W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M8	W/S=0.4/1.5	RM8L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=0.4/0.4	RM8S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=1.5/0.4	RM8W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/1.5	RM9L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/0.4	RM9S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=1.5/0.4	RM9W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M10 AP RDL	W/S=3/2	RM10	0.021	-	ohm/sq	3.89E-3	-1.50E-7	-	-
Mx	W/S=0.1/0.5	RMXL	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.1/0.1	RMXS	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.3/0.13	RMXW	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mz	W/S=0.4/1.5	RMZL	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mz	W/S=0.4/0.4	RMZS	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mz	W/S=1.5/0.4	RMZW	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-

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Film	Valid Width (in μm)	Model Naming	RshMean/Range		Unit	TC1	TC2	VC1	VC2
M1	-		0.160	`+0.0512 / -0.0352	W/sq	2.65E-03	-2.64E-07	NA	NA
M2-7	-		0.140	`+0.0420 / -0.0294	W/sq	2.71E-03	-3.48E-07	NA	NA
M8-9	-		0.022	`+0.0044 / -0.0035	W/sq	3.63E-03	-1.39E-06	NA	NA
M10 (AP RDL)	-		0.021	`+0.0042 / -0.0042	W/sq	3.89E-03	-1.50E-07	NA	NA
RC_N+	-		26	10.4	W/ct	9.49E-04	-4.47E-06	NA	NA
RC_P+	-		26	10.4	W/ct	1.84E-03	6.70E-06	NA	NA
RC_PO(N+)	-		20	8	W/ct	1.03E-03	1.63E-07	NA	NA
RC_PO(P+)	-		20	8	W/ct	1.11E-03	4.23E-07	NA	NA
RC_VIA1	-		1.5	`+1.5 / -1.05	W/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA2	-		1.5	`+1.5 / -1.05	W/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA3	-		1.5	`+1.5 / -1.05	W/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA4	-		1.5	`+1.5 / -1.05	W/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA5	-		1.5	`+1.5 / -1.05	W/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA6	-		1.5	`+1.5 / -1.05	W/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA7	-		0.22	0.11	W/ct	2.48E-03	1.03E-06	NA	NA
RC_VIA8	-		0.22	0.11	W/ct	2.48E-03	1.03E-06	NA	NA
RC_VIA9	-		0.041	0.0205	W/ct	3.37E-03	-7.91E-08	NA	NA

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12.11.3 CLN65GP (M1MxMz process, no My/Mr, x=2~7, z=8~9)

Table 12.11.3: Resistor model table for CLN65GP

Film	Valid Width (in m)	Model Naming	Rsh Mean/Range		Unit	TC1	TC2	VC1	VC2
N+ Poly w/i silicide	W>=2.0	rnpolyl	15.397	-	ohm/sq	2.09E-3	-4.21E-6	3.39E-9	6.01E-14
N+ Poly w/i silicide	0.06<=W<2.0	rnpolys	15.397	-	ohm/sq	2.43E-3	-6.10E-6	4.04E-8	5.83E-13
P+ Poly w/i silicide	W>=2.0	rppolyl	14.819	-	ohm/sq	2.30E-3	-3.32E-6	3.53E-7	7.56E-12
P+ Poly w/i silicide	0.06<=W<2.0	rppolys	14.819	-	ohm/sq	2.61E-3	-5.37E-6	4.28E-8	7.04E-13
N+ diff. w/i silicide	W>=2.0	rnodl	15.246	-	ohm/sq	2.03E-3	-3.42E-6	4.20E-8	6.36E-13
N+ diff. w/i silicide	0.08<=W<2.0	rnods	15.246	-	ohm/sq	2.31E-3	-4.78E-6	2.72E-8	5.53E-14
P+ diff. w/i silicide	W>=2.0	rpodl	14.552	-	ohm/sq	2.19E-3	-2.37E-6	-1.23E-9	4.05E-13
P+ diff. w/i silicide	0.08<=W<2.0	rpods	14.552	-	ohm/sq	2.26E-3	-4.41E-7	2.39E-8	-3.99E-14
N-well under OD	-	rnwod	316	-	ohm/sq	2.93E-3	9.99E-6	5.04E-3	1.67E-4
N-well under STI	-	rnwsti	605	-	ohm/sq	2.30E-3	9.34E-6	6.29E-3	-1.97E-4
M1	W/S=0.09/0.45	RM1L	0.0868	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.09/0.09	RM1S	0.16	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.27/0.135	RM1W	0.137	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M2	W/S=0.1/0.5	RM2L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.1/0.1	RM2S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.3/0.13	RM2W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.5	RM3L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.1	RM3S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.3/0.13	RM3W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.5	RM4L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.1	RM4S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.3/0.13	RM4W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.5	RM5L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.1	RM5S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.3/0.13	RM5W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.5	RM6L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.1	RM6S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.3/0.13	RM6W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.5	RM7L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.1	RM7S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.3/0.13	RM7W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M8	W/S=0.4/1.5	RM8L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=0.4/0.4	RM8S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=1.5/0.4	RM8W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/1.5	RM9L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/0.4	RM9S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=1.5/0.4	RM9W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M10 APRDL	W/S=3/2	RM10	0.021	-	ohm/sq	3.89E-3	-1.50E-7	-	-
Mx	W/S=0.1/0.5	RMXL	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.1/0.1	RMXS	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.3/0.13	RMXW	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mz	W/S=0.4/1.5	RMZL	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mz	W/S=0.4/0.4	RMZS	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mz	W/S=1.5/0.4	RMZW	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-

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Film	Valid Width (in μm)	Model Naming	RshMean/Range		Unit	TC1	TC2	VC1	VC2
M1	-		0.160	+0.0512 / -0.0352	Ω/sq	2.65E-03	-2.64E-07	NA	NA
M2-7	-		0.140	+0.0420 / -0.0294	Ω/sq	2.71E-03	-3.48E-07	NA	NA
M8-9	-		0.022	+0.0044 / -0.0035	Ω/sq	3.63E-03	-1.39E-06	NA	NA
M10 (Al RDL)	-		0.021	+0.0042 / -0.0042	Ω/sq	3.89E-03	-1.50E-07	NA	NA
RC_N+	-		26	10.4	Ω/ct	9.49E-04	-4.47E-06	NA	NA
RC_P+	-		26	10.4	Ω/ct	1.84E-03	6.70E-06	NA	NA
RC_PO(N+)	-		20	8	Ω/ct	1.03E-03	1.63E-07	NA	NA
RC_PO(P+)	-		20	8	Ω/ct	1.11E-03	4.23E-07	NA	NA
RC_VIA1	-		1.5	+1.5 / -1.05	Ω/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA2	-		1.5	+1.5 / -1.05	Ω/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA3	-		1.5	+1.5 / -1.05	Ω/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA4	-		1.5	+1.5 / -1.05	Ω/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA5	-		1.5	+1.5 / -1.05	Ω/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA6	-		1.5	+1.5 / -1.05	Ω/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA7	-		0.22	0.11	Ω/ct	2.48E-03	1.03E-06	NA	NA
RC_VIA8	-		0.22	0.11	Ω/ct	2.48E-03	1.03E-06	NA	NA
RC_VIA9	-		0.041	0.0205	Ω/ct	3.37E-03	-7.91E-08	NA	NA

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833462
12/16/2016
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12.11.4 CLN65LPG (M1MxMz process, no My/Mr, x=2~7, z=8~9)

Table 12.11.4: Resistor model table for CLN65LPG

Film	Valid Width (in μm)	Model Naming	Rsh Mean/Range		Unit	TC1	TC2	VC1	VC2
N+ Poly w/I silicide	W>=2.0	rnpolyl	15.0618623	-	ohm/sq	0.001887444	-6.41E-07	6.54E-07	1.17E-11
N+ Poly w/I silicide	0.06<=W<2.0	rnpolys	15.0618623	-	ohm/sq	0.002162497	-7.21E-07	2.63E-08	4.19E-12
P+ Poly w/I silicide	W>=2.0	rppolyl	14.9255297	-	ohm/sq	0.002250708	-9.32E-07	8.25E-07	1.38E-11
P+ Poly w/I silicide	0.06<=W<2.0	rppolys	14.9255297	-	ohm/sq	0.002371857	-6.16E-07	8.54E-08	4.18E-12
N+ diff. W/I silicide	W>=2.0	rnodl	15.52195217	-	ohm/sq	0.001905463	-5.99E-07	-5.30E-08	3.23E-12
N+ diff. W/I silicide	0.08<=W<2.0	rnods	15.52195217	-	ohm/sq	0.002172012	-5.47E-07	4.83E-08	9.73E-13
P+ diff. W/I silicide	W>=2.0	rpodl	14.55118032	-	ohm/sq	0.002132422	-9.32E-07	-7.28E-09	3.46E-12
P+ diff. W/I silicide	0.08<=W<2.0	rpods	14.55118032	-	ohm/sq	0.002370563	-7.40E-07	-4.25E-09	1.37E-12
N-well under OD	-	rnwod	326.8034772	-	ohm/sq	2.43E-03	9.20E-06	0.002118977	0.000515843
N-well under STI	-	rnwsti	595.1748005	-	ohm/sq	2.02E-03	9.94E-06	0.003817735	1.03E-04
M1	W/S=0.09/0.45	RM1L	0.0868	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.09/0.09	RM1S	0.16	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.27/0.135	RM1W	0.137	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M2	W/S=0.1/0.5	RM2L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.1/0.1	RM2S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.3/0.13	RM2W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.5	RM3L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.1	RM3S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.3/0.13	RM3W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.5	RM4L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.1	RM4S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.3/0.13	RM4W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.5	RM5L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.1	RM5S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.3/0.13	RM5W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.5	RM6L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.1	RM6S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.3/0.13	RM6W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.5	RM7L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.1	RM7S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.3/0.13	RM7W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M8	W/S=0.4/1.5	RM8L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=0.4/0.4	RM8S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=1.5/0.4	RM8W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/1.5	RM9L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/0.4	RM9S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=1.5/0.4	RM9W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M10 AP RDL	W/S=3/2	RM10	0.021	-	ohm/sq	3.89E-3	-1.50E-7	-	-
Mx	W/S=0.1/0.5	RMXL	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.1/0.1	RMXS	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.3/0.13	RMXW	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mz	W/S=0.4/1.5	RMZL	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mz	W/S=0.4/0.4	RMZS	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mz	W/S=1.5/0.4	RMZW	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-

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Film	Valid Width (in μm)	Model Naming	RshMean/Range		Unit	TC1	TC2	VC1	VC2
M1	-		0.160	+0.0512 / -0.0352	Ohm/sq	2.65E-03	-2.64E-07	NA	NA
M2-7	-		0.140	+0.0420 / -0.0294	Ohm/sq	2.71E-03	-3.48E-07	NA	NA
M8-9	-		0.022	+0.0044 / -0.0035	Ohm/sq	3.63E-03	-1.39E-06	NA	NA
M10 (AP RDL)	-		0.021	+0.0042 / -0.0042	Ohm/sq	3.89E-03	-1.50E-07	NA	NA
RC_N+	-		26	10.4	Ohm/ct	9.49E-04	-4.47E-06	NA	NA
RC_P+	-		26	10.4	Ohm/ct	1.84E-03	6.70E-06	NA	NA
RC_PO(N+)	-		20	8.0	Ohm/ct	1.03E-03	1.63E-07	NA	NA
RC_PO(P+)	-		20	8.0	Ohm/ct	1.11E-03	4.23E-07	NA	NA
RC_VIA1	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA2	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA3	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA4	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA5	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA6	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-04	-2.57E-06	NA	NA
RC_VIA7	-		0.22	0.11	Ohm/ct	2.48E-03	1.03E-06	NA	NA
RC_VIA8	-		0.22	0.11	Ohm/ct	2.48E-03	1.03E-06	NA	NA
RC_VIA9	-		0.041	0.0205	Ohm/ct	3.37E-03	-7.91E-08	NA	NA

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12.11.5 CLN65ULP

Table 12.11.5: Resistor model table for CLN65ULP

Film	Valid Width (in μm)	Model Naming	Rsh Mean/Range		Unit	TC1	TC2	VC1	VC2
N+ Poly w/l silicide	W>=2.0	rnpolyl	15.06186	-	ohm/sq	0.0018874	-6.41E-07	6.54E-07	1.17E-11
N+ Poly w/l silicide	0.06<=W<2.0	rnpolys	15.06186	-	ohm/sq	0.0021624	-7.21E-07	2.63E-08	4.19E-12
P+ Poly w/l silicide	W>=2.0	rppolyl	14.92552	-	ohm/sq	0.0022507	-9.32E-07	8.25E-07	1.38E-11
P+ Poly w/l silicide	0.06<=W<2.0	rppolys	14.92552	-	ohm/sq	0.0023718	-6.16E-07	8.54E-08	4.18E-12
N+ diff. W/l silicide	W>=2.0	rnodl	15.52195	-	ohm/sq	0.0019054	-5.99E-07	-5.30E-08	3.23E-12
N+ diff. W/l silicide	0.08<=W<2.0	rnods	15.52195	-	ohm/sq	0.0021720	-5.47E-07	4.83E-08	9.73E-13
P+ diff. W/l silicide	W>=2.0	rpodl	14.55118	-	ohm/sq	0.0021324	-9.32E-07	-7.28E-09	3.46E-12
P+ diff. W/l silicide	0.08<=W<2.0	rpods	14.55118	-	ohm/sq	0.0023705	-7.40E-07	-4.25E-09	1.37E-12
N-well under OD	-	rnwod	326.8034	-	ohm/sq	2.43E-03	9.20E-06	0.0021189	0.000515843
N-well under STI	-	rnwsti	595.1748	-	ohm/sq	2.02E-03	9.94E-06	0.0038177	1.03E-04
M1	W/S=0.09/0.45	RM1L	0.0868	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.09/0.09	RM1S	0.16	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M1	W/S=0.27/0.135	RM1W	0.137	-	ohm/sq	2.65E-3	-2.64E-7	-	-
M2	W/S=0.1/0.5	RM2L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.1/0.1	RM2S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M2	W/S=0.3/0.13	RM2W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.5	RM3L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.1/0.1	RM3S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M3	W/S=0.3/0.13	RM3W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.5	RM4L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.1/0.1	RM4S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M4	W/S=0.3/0.13	RM4W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.5	RM5L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.1/0.1	RM5S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M5	W/S=0.3/0.13	RM5W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.5	RM6L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.1/0.1	RM6S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M6	W/S=0.3/0.13	RM6W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.5	RM7L	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.1/0.1	RM7S	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M7	W/S=0.3/0.13	RM7W	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
M8	W/S=0.4/1.5	RM8L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=0.4/0.4	RM8S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M8	W/S=1.5/0.4	RM8W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/1.5	RM9L	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=0.4/0.4	RM9S	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M9	W/S=1.5/0.4	RM9W	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
M10 AL RDL	W/S=3/2	RM10	0.021	-	ohm/sq	3.89E-3	-1.50E-7	-	-
Mx	W/S=0.1/0.5	RMXL	0.0778	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.1/0.1	RMXS	0.1399	-	ohm/sq	2.71E-3	-3.48E-7	-	-
Mx	W/S=0.3/0.13	RMXW	0.119	-	ohm/sq	2.71E-3	-3.48E-7	-	-
My	W/S=0.2/1	RMYL	0.0326	-	ohm/sq	3.335e-3	-1.142e-7		
My	W/S=0.2/0.2	RMYS	0.0380	-	ohm/sq	3.335e-3	-1.142e-7		
My	W/S=0.6/0.3	RMYW	0.0365	-	ohm/sq	3.335e-3	-1.142e-7		
Mz	W/S=0.4/1.5	RMZL	0.0215	-	ohm/sq	3.63E-3	-1.39E-6	-	-

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Film	Valid Width (in μm)	Model Naming	Rsh Mean/Range		Unit	TC1	TC2	VC1	VC2
Mz	W/S=0.4/0.4	RMZS	0.0218	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mz	W/S=1.5/0.4	RMZW	0.0227	-	ohm/sq	3.63E-3	-1.39E-6	-	-
Mr	W/S=0.5/1.2	RMRL	0.0145	-	ohm/sq	3.27E-03	-3.88E-06	-	-
Mr	W/S=0.5/0.5	RMRS	0.0147	-	ohm/sq	3.27E-03	-3.88E-06	-	-
Mr	W/S=1.2/0.5	RMRW	0.0178	-	ohm/sq	3.27E-03	-3.88E-06	-	-
MAP	W/S=3/2	RMAP	0.021		ohm/sq	3.89E-03	-1.5E-07		
MAP_UT	W/S=3/2	RMAP_UT	0.011		ohm/sq	3.89E-03	-1.5E-07		
Mt		RMT	0.005		ohm/sq	3.41E-03	3.69E-06		

Film	Valid Width (in μm)	Model Naming	RshMean/Range		Unit	TC1	TC2	VC1	VC2
M1	-		0.160	+0.0512 / -0.0352	Ohm/sq	2.65E-	-2.64E-07	NA	NA
M2-7	-		0.140	+0.0420 / -0.0294	Ohm/sq	2.71E-	-3.48E-07	NA	NA
M8-9	-		0.022	+0.0044 / -0.0035	Ohm/sq	3.63E-	-1.39E-06	NA	NA
M10 (Al RDL)	-		0.021	+0.0042 / -0.0042	Ohm/sq	3.89E-	-1.50E-07	NA	NA
RC_N+	-		26	10.4	Ohm/ct	9.49E-	-4.47E-06	NA	NA
RC_P+	-		26	10.4	Ohm/ct	1.84E-	6.70E-06	NA	NA
RC_PO(N+)	-		20	8.0	Ohm/ct	1.03E-	1.63E-07	NA	NA
RC_PO(P+)	-		20	8.0	Ohm/ct	1.11E-	4.23E-07	NA	NA
RC_VIA1	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-	-2.57E-06	NA	NA
RC_VIA2	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-	-2.57E-06	NA	NA
RC_VIA3	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-	-2.57E-06	NA	NA
RC_VIA4	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-	-2.57E-06	NA	NA
RC_VIA5	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-	-2.57E-06	NA	NA
RC_VIA6	-		1.5	+1.5 / -1.05	Ohm/ct	7.82E-	-2.57E-06	NA	NA
RC_VIA7	-		0.22	0.11	Ohm/ct	2.48E-	1.03E-06	NA	NA
RC_VIA8	-		0.22	0.11	Ohm/ct	2.48E-	1.03E-06	NA	NA
RC_VIA9	-		0.041	0.0205	Ohm/ct	3.37E-	-7.91E-08	NA	NA

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12.11.6 CLN55GP (M1MxMz process, no My/Mr, x=2~7, z=8~9)

Table 12.11.6: Resistor model table for CLN55GP

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	107.87	ohm/sq	1.09E-09	5.09E-02	1.51E-06	-1.54E-06	1.66E-03	1.63E-06
		Rend0	3.03E-07	ohm.m	-	-0.0655	2.53E+03	0.427	-2.09E-04	2.58E-05
rpodwo	P+OD w/o silicide resistor	Rsh	262.16	ohm/sq	2.33E-09	0.011	1.05E-06	-4.95E-04	1.29E-03	3.50E-06
		Rend0	5.82E-07	ohm.m	-	-0.2064	1.43E+03	-0.9821	6.55E-03	1.97E-05
rnpolywo	N+POLY w/o silicide resistor	Rsh	139.16	ohm/sq	4.32E-08	0.7198	4.84E-05	2.9624	1.35E-04	1.43E-06
		Rend0	1.24E-06	ohm.m	-	-0.2757	1.24E+04	-0.4189	-1.19E-03	-7.31E-06
rppolywo	P+POLY w/o silicide resistor	Rsh	781.46	ohm/sq	5.01E-08	0.0489	-4.55E-06	2.3171	-4.23E-04	3.53E-06
		Rend0	1.08E-06	ohm.m	-	2.03E-01	20.6378	0.6691	-4.57E-04	8.24E-07
rppolyl	P+POLY silicide resistor (W>=1.8um)	Rsh	16.19	ohm/sq	-1.56E-08	5.99E-07	1.58E-11	-	0.002236	1.87E-07
rppolys	P+POLY silicide resistor (W<1.8um)	Rsh	16.19	ohm/sq	-1.56E-08	3.40E-06	-2.23E-11	-	0.003822	4.95E-06
rnpolyl	N+POLY silicide resistor (W>=1.8um)	Rsh	15.96	ohm/sq	-1.05E-08	6.92E-08	6.40E-12	-	0.001794	-1.93E-07
rnpolys	N+POLY silicide resistor (W<1.8um)	Rsh	15.96	ohm/sq	-1.05E-08	2.34E-06	-1.20E-11	-	0.002864	1.69E-06
rnodl	N+OD silicide resistor (W>=1.8um)	Rsh	16.48	ohm/sq	-3.80E-08	4.92E-08	2.59E-12	-	0.002056	-6.48E-07
rnods	N+OD silicide resistor (W<1.8um)	Rsh	16.48	ohm/sq	-3.80E-08	-3.28E-08	1.63E-12	-	0.015908	6.37E-05
rpodl	P+OD silicide resistor (W>=1.8um)	Rsh	15.73	ohm/sq	-3.92E-08	4.56E-08	3.09E-12	-	0.002355	-2.05E-06
rpods	P+OD silicide resistor (W<1.8um)	Rsh	15.73	ohm/sq	-3.92E-08	-2.01E-08	2.50E-12	-	0.008712	-5.57E-05
rnwod	N-Well under OD resistor	Rsh	330.6	ohm/sq	0.189u	0.003416	0.000291	-	2.82E-03	9.88E-06
rnwsti	N-well under STI resistor	Rsh	605	ohm/sq	0.27u	0.004694	8.15E-05	-	2.02E-03	1.02E-05
rm1l	Metal 1 with W/S=0.081/0.405	Rsh	0.0934	ohm/sq	0	0	0	-	2.47E-03	-2.55E-07
rm1s	Metal 1 with W/S=0.081/0.081	Rsh	0.1892	ohm/sq	0	0	0	-	2.47E-03	-2.55E-07
rm1w	Metal 1 with W/S=0.243/0.122	Rsh	0.1564	ohm/sq	0	0	0	-	2.47E-03	-2.55E-07
rm2l	Metal 2with W/S=0.09/0.45	Rsh	0.0851	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm2s	Metal 2 with W/S=0.09/0.09	Rsh	0.1667	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm2w	Metal 2 with W/S=0.27/0.117	Rsh	0.1272	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm3l	Metal 3 with W/S=0.09/0.45	Rsh	0.0851	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm3s	Metal 3 with W/S=0.09/0.09	Rsh	0.1667	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm3w	Metal 3 with W/S=0.27/0.117	Rsh	0.1272	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm4l	Metal 4 with W/S=0.09/0.45	Rsh	0.0851	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm4s	Metal 4 with W/S=0.09/0.09	Rsh	0.1667	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm4w	Metal 4 with W/S=0.27/0.117	Rsh	0.1272	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm5l	Metal 5 with W/S=0.09/0.45	Rsh	0.0851	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm5s	Metal 5 with W/S=0.09/0.09	Rsh	0.1667	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm5w	Metal 5 with W/S=0.27/0.117	Rsh	0.1272	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm6l	Metal 6 with W/S=0.09/0.45	Rsh	0.0851	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm6s	Metal 6 with W/S=0.09/0.09	Rsh	0.1667	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm6w	Metal 6 with W/S=0.27/0.117	Rsh	0.1272	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm7l	Metal 7 with W/S=0.09/0.45	Rsh	0.0851	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm7s	Metal 7 with W/S=0.09/0.09	Rsh	0.1667	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07

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Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rm7w	Metal 7 with W/S=0.27/0.117	Rsh	0.1272	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rm8l	Metal 8 with W/S=0.36/1.35	Rsh	0.022	ohm/sq	0	0	0	-	3.64E-03	-1.38E-06
rm8s	Metal 8 with W/S=0.36/0.36	Rsh	0.0221	ohm/sq	0	0	0	-	3.64E-03	-1.38E-06
rm8w	Metal 8 with W/S=1.35/0.36	Rsh	0.0237	ohm/sq	0	0	0	-	3.64E-03	-1.38E-06
rm9l	Metal 9 with W/S=0.36/1.35	Rsh	0.022	ohm/sq	0	0	0	-	3.64E-03	-1.38E-06
rm9s	Metal 9 with W/S=0.36/0.36	Rsh	0.0221	ohm/sq	0	0	0	-	3.64E-03	-1.38E-06
rm9w	Metal 9 with W/S=1.35/0.36	Rsh	0.0237	ohm/sq	0	0	0	-	3.64E-03	-1.38E-06
rm10	Metal 10 (AL_RDL) with W/S=2.7/1.8	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rmxl	Metal x with W/S=0.09/0.45	Rsh	0.0851	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rmxs	Metal x with W/S=0.09/0.09	Rsh	0.1667	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rmxw	Metal x with W/S=0.27/0.117	Rsh	0.1272	ohm/sq	0	0	0	-	2.54E-03	-2.75E-07
rmzl	Metal z with W/S=0.36/1.35	Rsh	0.022	ohm/sq	0	0	0	-	3.64E-03	-1.38E-06
rmzs	Metal z with W/S=0.36/0.36	Rsh	0.0221	ohm/sq	0	0	0	-	3.64E-03	-1.38E-06
rmzw	Metal z with W/S=1.35/0.36	Rsh	0.0237	ohm/sq	0	0	0	-	3.64E-03	-1.38E-06
-	RC_N+		30	ohm/ct	0	0	0	-	1.20E-03	-3.81E-07
-	RC_P+		30	ohm/ct	0	0	0	-	1.30E-03	-5.83E-07
-	RC_PO(N+)		22	ohm/ct	0	0	0	-	1.24E-03	-4.11E-07
-	RC_PO(P+)		22	ohm/ct	0	0	0	-	1.41E-03	-4.15E-07
-	RC_VIA9		0.041	ohm/ct	0	0	0	-	3.37E-03	-7.91E-08
-	RC_VIA8		0.24	ohm/ct	0	0	0	-	2.69E-03	-1.97E-06
-	RC_VIA7		0.24	ohm/ct	0	0	0	-	2.69E-03	-1.97E-06
-	RC_VIA6		2.5	ohm/ct	0	0	0	-	1.20E-03	-7.73E-06
-	RC_VIA5		2.5	ohm/ct	0	0	0	-	1.20E-03	-7.73E-06
-	RC_VIA4		2.5	ohm/ct	0	0	0	-	1.20E-03	-7.73E-06
-	RC_VIA3		2.5	ohm/ct	0	0	0	-	1.20E-03	-7.73E-06
-	RC_VIA2		2.5	ohm/ct	0	0	0	-	1.20E-03	-7.73E-06
-	RC_VIA1		2.5	ohm/ct	0	0	0	-	1.20E-03	-7.73E-06

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12.11.7 CLN55LP (M1MxMz process, no MyMr, x=2~7, z=8~9)

Table 12.11.7: Resistor model table for CLN55LP

Name	Structure	Type	TypeVal	Unit	dw(m)	dl(m)	VC1	VC2	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	119.5	ohm/sq	3.00E-03	0	function of W/L (pls refer to model card)			
		Rend0	7.90E-06	ohm.m	-	-	function of W/L (pls refer to model card)			
rpodwo	P+OD w/o silicide resistor	Rsh	251	ohm/sq	-1.23E-02	0	function of W/L (pls refer to model card)			
		Rend0	4.60E-06	ohm.m	-	-	function of W/L (pls refer to model card)			
rnpolywo	N+POLY w/o silicide resistor	Rsh	155.7	ohm/sq	6.00E-02	0	function of W/L (pls refer to model card)			
		Rend0	1.10E-05	ohm.m	-	-	function of W/L (pls refer to model card)			
rppolywo	P+POLY w/o silicide resistor	Rsh	726.5	ohm/sq	4.00E-02	0	function of W/L (pls refer to model card)			
		Rend0	1.00E-06	ohm.m	-	-	function of W/L (pls refer to model card)			
rppolyl	P+POLY silicide resistor (W>=2um)	Rsh	13.4598	ohm/sq	-2.49E-08	-	0	pls refer to model card	0.00233	-6.88E-07
rppolys	P+POLY silicide resistor (W<2um)	Rsh	13.4598	ohm/sq	-2.49E-08	-	0	pls refer to model card	0.00233	-6.88E-07
rnpolyl	N+POLY silicide resistor (W>=2um)	Rsh	13.3586	ohm/sq	-2.36E-08	-	0	pls refer to model card	0.00213	-1.24E-06
rnpolys	N+POLY silicide resistor (W<2um)	Rsh	13.3586	ohm/sq	-2.36E-08	-	0	pls refer to model card	0.00213	-1.24E-06
rnodl	N+OD silicide resistor (W>=2um)	Rsh	13.524	ohm/sq	-1.79E-08	-	0	pls refer to model card	0.00222	-1.15E-06
rnods	N+OD silicide resistor (W<2um)	Rsh	13.524	ohm/sq	-1.79E-08	-	0	pls refer to model card	0.00222	-1.15E-06
rpodl	P+OD silicide resistor (W>=2um)	Rsh	13.287	ohm/sq	-1.86E-08	-	0	pls refer to model card	0.00224	-1.31E-06
rpods	P+OD silicide resistor (W<2um)	Rsh	13.287	ohm/sq	-1.86E-08	-	0	pls refer to model card	0.00224	-1.31E-06
rnwod	N-Well under OD resistor	Rsh	342	ohm/sq	0.2241u	-	9.86E-03	1.01E-04	2.61E-03	9.58E-06
rnwsti	N-well under STI resistor	Rsh	589.5	ohm/sq	0.2812u	-	4.21E-03	1.69E-04	2.16E-03	9.58E-06
rm1l	Metal 1 with W/S=0.09/0.45	Rsh	0.0934	ohm/sq	0	-	0	0	2.47E-03	-2.55E-07
rm1s	Metal 1 with W/S=0.09/0.09	Rsh	0.1892	ohm/sq	0	-	0	0	2.47E-03	-2.55E-07
rm1w	Metal 1 with W/S=0.27/0.136	Rsh	0.1564	ohm/sq	0	-	0	0	2.47E-03	-2.55E-07
rm2l	Metal 2with W/S=0.1/0.5	Rsh	0.0851	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm2s	Metal 2 with W/S=0.1/0.1	Rsh	0.1667	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm2w	Metal 2 with W/S=0.3/0.13	Rsh	0.1272	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm3l	Metal 3 with W/S=0.1/0.5	Rsh	0.0851	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm3s	Metal 3 with W/S=0.1/0.1	Rsh	0.1667	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm3w	Metal 3 with W/S=0.3/0.13	Rsh	0.1272	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm4l	Metal 4 with W/S=0.1/0.5	Rsh	0.0851	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm4s	Metal 4 with W/S=0.1/0.1	Rsh	0.1667	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm4w	Metal 4 with W/S=0.3/0.13	Rsh	0.1272	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm5l	Metal 5 with W/S=0.1/0.5	Rsh	0.0851	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm5s	Metal 5 with W/S=0.1/0.1	Rsh	0.1667	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm5w	Metal 5 with	Rsh	0.1272	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07

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Name	Structure	Type	TypeVal	Unit	dw(m)	dl(m)	VC1	VC2	TC1	TC2
	W/S=0.3/0.13									
rm6l	Metal 6 with W/S=0.1/0.5	Rsh	0.0851	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm6s	Metal 6 with W/S=0.1/0.1	Rsh	0.1667	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm6w	Metal 6 with W/S=0.3/0.13	Rsh	0.1272	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm7l	Metal 7 with W/S=0.1/0.5	Rsh	0.0851	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm7s	Metal 7 with W/S=0.1/0.1	Rsh	0.1667	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm7w	Metal 7 with W/S=0.3/0.13	Rsh	0.1272	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rm8l	Metal 8 with W/S=0.4/1.5	Rsh	0.0299	ohm/sq	0	-	0	0	3.29E-03	-1.62E-06
rm8s	Metal 8 with W/S=0.4/0.4	Rsh	0.0402	ohm/sq	0	-	0	0	3.29E-03	-1.62E-06
rm8w	Metal 8 with W/S=1.5/0.4	Rsh	0.0413	ohm/sq	0	-	0	0	3.29E-03	-1.62E-06
rm9l	Metal 9 with W/S=0.4/1.5	Rsh	0.0299	ohm/sq	0	-	0	0	3.29E-03	-1.62E-06
rm9s	Metal 9 with W/S=0.4/0.4	Rsh	0.0402	ohm/sq	0	-	0	0	3.29E-03	-1.62E-06
rm9w	Metal 9 with W/S=1.5/0.4	Rsh	0.0413	ohm/sq	0	-	0	0	3.29E-03	-1.62E-06
rm10	Metal 10 (AL_RDL) with W/S=3/2	Rsh	0.021	ohm/sq	0	-	0	0	3.89E-03	-1.50E-07
rmxl	Metal x with W/S=0.1/0.5	Rsh	0.0851	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rmxs	Metal x with W/S=0.1/0.1	Rsh	0.1667	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rmxw	Metal x with W/S=0.3/0.13	Rsh	0.1272	ohm/sq	0	-	0	0	2.54E-03	-2.75E-07
rmyl	Metal y with W/S=0.2/1	Rsh	0.0299	ohm/sq	0	-	0	0	3.29E-03	-1.62E-06
rmys	Metal y with W/S=0.2/0.2	Rsh	0.0402	ohm/sq	0	-	0	0	3.29E-03	-1.62E-06
rmyw	Metal y with W/S=0.6/0.3	Rsh	0.0396	ohm/sq	0	-	0	0	3.29E-03	-1.62E-06
rmzl	Metal z with W/S=0.4/1.5	Rsh	0.022	ohm/sq	0	-	0	0	3.64E-03	-1.38E-06
rmzs	Metal z with W/S=0.4/0.4	Rsh	0.0221	ohm/sq	0	-	0	0	3.64E-03	-1.38E-06
rmzw	Metal z with W/S=1.5/0.4	Rsh	0.0237	ohm/sq	0	-	0	0	3.64E-03	-1.38E-06
-	RC_N+		29	ohm/ct	0	-	0	0	1.20E-03	-3.81E-07
-	RC_P+		29	ohm/ct	0	-	0	0	1.30E-03	-5.83E-07
-	RC_PO(N+)		24	ohm/ct	0	-	0	0	1.24E-03	-4.11E-07
-	RC_PO(P+)		24	ohm/ct	0	-	0	0	1.41E-03	-4.15E-07
-	RC_VIA9		0.041	ohm/ct	0	-	0	0	3.37E-03	-7.91E-08
-	RC_VIA8		0.24	ohm/ct	0	-	0	0	2.69E-03	-1.97E-06
-	RC_VIA7		0.24	ohm/ct	0	-	0	0	2.69E-03	-1.97E-06
-	RC_VIA6		2.5	ohm/ct	0	-	0	0	1.20E-03	-7.73E-06
-	RC_VIA5		2.5	ohm/ct	0	-	0	0	1.20E-03	-7.73E-06
-	RC_VIA4		2.5	ohm/ct	0	-	0	0	1.20E-03	-7.73E-06
-	RC_VIA3		2.5	ohm/ct	0	-	0	0	1.20E-03	-7.73E-06
-	RC_VIA2		2.5	ohm/ct	0	-	0	0	1.20E-03	-7.73E-06
-	RC_VIA1		2.5	ohm/ct	0	-	0	0	1.20E-03	-7.73E-06

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12.12 Unsilicided N+/P+ Poly Resistors Models

Two types of unsilicided poly resistor models are available; one is N+ type and the other is P+ type. A cross-section schematic of the resistor structure is shown in Fig. 12.12.1.These resistors were measured by sweeping current on one node, while grounding the other one. As suggested by TSMC's reliability team, these resistors might encounter a reliability issue if the current density applied is above 500 μA/μm width. Thus, the valid current density range for these models is between 0 and 500 μA/μm width. The corresponding voltage range can be obtained using the Ohm's law. TSMC further limits the application of these models only to resistors with width ≥ 0.4 μm and length ≥ 0.4 μm, and square number > 1. It is strongly recommended that all users should apply these models within valid current/voltage/dimension ranges. Application beyond the valid range will lead to a significant error.

These resistors were modeled with the equivalent circuit shown in Fig. 12.12.2. In this circuit, the R_{end} component represents the contributions from the interface resistance (R_{int}, due to the depletion of dopant near the interface between revered protection oxide (RPO) and silicide) but do not include the contact resistance R_c, while the R_p component represents the primary contribution of the poly resistor.

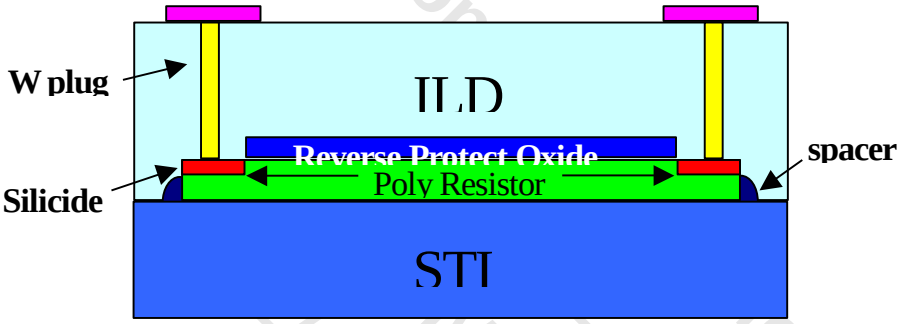

Fig. 12.12.1: Cross-section schematic of the unsilicided poly resistor.

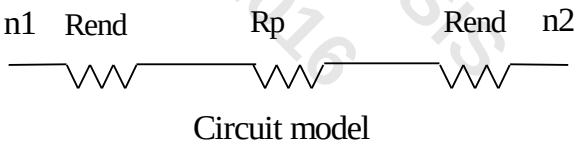

Fig. 12.12.2: Equivalent circuit used to model the unsilicided poly resistor.

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12.12.1 Resistor Model Equations

As shown in the equivalent circuit, the total resistance (R) measured is equal to the sum of the R_p plus two times of R_{end}, as in equation (12-12-1):

$$R = R_p + 2R_{end}$$ **Equation (12-12-1)**

In contrast to other resistor models, the voltage dependence of R_p and R_{end} components were modeled with the equations containing hyperbolic-tangent terms, as in equation (12-12-2) and (12-12-3):

$$R_{end} = R_{end0}/(W-\delta W)\cdot(1+tce1\cdot\delta T+tce2\cdot\delta T^2)\cdot\{1+vce1\cdot[\tanh(vce2\cdot|\delta V_e|+vce3)-\tanh(vce3)]\}$$ **Equation (12-12-2)**

$$R_p = R_{sh}\cdot(L-\delta L)/(W-\delta W)\cdot(1+tcp1\cdot\delta T+tcp2\cdot\delta T^2)\cdot \{1+vcp1\cdot[\tanh(vcp2\cdot|\delta V_p|/L+vcp3)-\tanh(vcp3)]\}$$ **Equation (12-12-3)**

where

δT = T - 25 (in °C),

δV_p and δV_e (in volt) = the voltage drops across R_p and R_{end} components, respectively.

R_{end0} = the R_{end} resistance value at 25 °C and an infinitesimal voltage.

δL = the length offset.

The use of the empirical hyper-tangent equation, instead of the second order polynomial one, is to avoid the occurrence of zero or negative resistance during the simulation iteration. For temperature dependence modeling, the second order polynomial equation used by other resistor models is also employed here. Finally, the median sheet resistance values and their corresponding variations, R_{end0}, temperature coefficients, voltage coefficients, δW, and δL extracted based on the methodology described above are reported in Table 12.12.1~10.

Table 12.12.1: Unsilicided poly resistor model parameter table for N65LP 1.2V/2.5V.

Resistor Parameters	N+ poly w/o silicide	P+ poly w/o silicide
Rsh (ohm/sq)	153.4133674	690.0226806
Range	+18.0%/-18.0%-	+17.5%/-17.5%--
Rend0(ohm.m)	3.03E-06	1.04E-06
Rp: Jc1_0	0.468910868642278	0.0695053510675811
Rp: Jc1_w	-0.112938447121681	0.0269845671346735
Rp: Jc1_n	0.00691776661634369	0.000714977117664719
Rp: Tc1_0	0.000146777758646609	0.000326161317630646
Rp: Tc1_w	-3.23409625208756E-05	3.10855059871834E-06
Rp: Tc2_0	1.89557340140836E-07	8.05172629127237E-07
Rp: Tc2_w	8.47296898658068E-08	-2.79415787596679E-08
Rp: Jct_0	0.00382604564786152	-0.00425159480565355
Rp: Jct_w	-0.00234776917199985	2.26507523320411E-05
Rend: Jc1end_0	21.876715834462	27.900361735252
Rend: Jc1end_w	0	0
Rend: Tc1end_0	0.000876816730930428	-0.00141906402431781
Rend: Tc1end_w	0.00036855776757363	1.51517802655145E-05
Rend: Tc2end_0	5.63556101704174E-07	1.19263050938459E-06
Rend: Tc2end_w	-3.50561057125037E-07	5.77755688915007E-07
Rend: Jctend_0	0.00297141058822875	-0.00141455931220154
Rend: Jctend_w	-0.00196020344135713	0.000920093941015092

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Table 12.12.2: Unsilicided poly resistor model parameter table for N65LP 1.2V/3.3V.

Resistor Parameters	N+ poly w/o silicide	P+ poly w/o silicide
Rsh (ohm/sq)	153.4133674	690.0226806
Range	+18.0%/-18.0%	+17.5%/-17.5%
Rend0(ohm.m)	3.03E-06	1.04E-06
Rp: tcp1	0.00015	-0.000309
Rp: tcp2	2.85E-07	7.50E-07
Rp: vcp1	-5.43E+00	2.00E+01
Rp: vcp2	-9.80E-05	-4.27E-08
Rp: vcp3	-3.66E+00	2.49E+00
Rend: tce1	0.00868707	-0.0006397
Rend: tce2	-2.88E-05	1.18E-06
Rend: vce1	3.97E+00	7.83E-01
Rend: vce2	-2.99E+03	-8.65E+03
Rend: vce3	-2.01E+00	-7.67E-01

Table 12.12.3: Unsilicided poly resistor model parameter table for N65G 1.0V/1.8V.

Resistor Parameters	N+ poly w/o silicide	P+ poly w/o silicide
Rsh (ohm/sq)	139.1	790.2
Range (ohm/sq)	---	---
Rend0(ohm.m)	4.800E-06	1.000E-06
Rp: tcp1	1.72E-04	-4.06E-04
Rp: tcp2	3.11E-07	8.27E-07
Rp: vcp1	0.0272	0.0875
Rp: vcp2	3.80E-05	-3.5096E-06
Rp: vcp3	1.1636	2.3563
Rend: tce1	4.720E-03	-2.469E-03
Rend: tce2	-1.814E-06	6.392E-06
Rend: vce1	0.66	-0.05
Rend: vce2	-2100	-339.2022
Rend: vce3	-1.1365	2.1995

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Table 12.12.4: Unsilicided poly resistor model parameter table for N65G 1.0V/2.5V.

Resistor Parameters	N+ poly w/o silicide	P+ poly w/o silicide
Rsh (ohm/sq)	139.1	790.2
Range	---	---
Rend0(ohm.m)	4.800E-06	1.000E-06
Rp: tcp1	1.72E-04	-4.06E-04
Rp: tcp2	3.11E-07	8.27E-07
Rp: vcp1	0.0272	0.0875
Rp: vcp2	3.80E-05	-3.5096E-06
Rp: vcp3	1.1636	2.3563
Rend: tce1	4.720E-03	-2.469E-03
Rend: tce2	-1.814E-06	6.392E-06
Rend: vce1	0.66	-0.05
Rend: vce2	-2100	-339.2022
Rend: vce3	-1.1365	2.1995

Table 12.12.5: Unsilicided poly resistor model parameter table for N65GP 1.0V/1.8V.

Resistor Parameters	N+ poly w/o silicide	P+ poly w/o silicide
Rsh (ohm/sq)	124.45	756.21
Range (ohm/sq)	---	---
Rend0(ohm.m)	4.27E-06	6.34E-07
Rp: tcp1	1.75E-04	-3.44E-04
Rp: tcp2	2.52E-07	7.32E-07
Rp: vcp1	-5.89	5.88E-02
Rp: vcp2	-6.64E-05	-5.46E-06
Rp: vcp3	-3.92	2.64
Rend: tce1	2.52E-03	-2.83E-03
Rend: tce2	9.92E-06	5.84E-06
Rend: vce1	1.76	2.18
Rend: vce2	-4.38E+03	-3.70E+2
Rend: vce3	-1.44	-2.78

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Table 12.12.6: Unsilicided poly resistor model parameter table for N65GP 1.0V/2.5V.

Resistor Parameters	N+ poly w/o silicide	P+ poly w/o silicide
Rsh (ohm/sq)	124.45	756.21
Range (ohm/sq)	---	---
Rend0(ohm.m)	4.27E-06	6.34E-07
Rp: tcp1	1.75E-04	-3.44E-04
Rp: tcp2	2.52E-07	7.32E-07
Rp: vcp1	-5.89	5.88E-02
Rp: vcp2	-6.64E-05	-5.46E-06
Rp: vcp3	-3.92	2.64
Rend: tce1	2.52E-03	-2.83E-03
Rend: tce2	9.92E-06	5.84E-06
Rend: vce1	1.76	2.18
Rend: vce2	-4.38E+03	-3.70E+2
Rend: vce3	-1.44	-2.78

Table 12.12.7: Unsilicided poly resistor model parameter table for N65LPG 1.0V(G),1.2(LP)/2.5V

Resistor Parameters	N+ poly w/o silicide	P+ poly w/o silicide
Rsh (ohm/sq)	153.4133674	690.0226806
Range	+18.0%/-18.0%	+17.5%/-17.5%
Rend0(ohm.m)	3.03E-06	1.04E-06
Rp: tcp1	0.00015	-0.000309
Rp: tcp2	2.85E-07	7.50E-07
Rp: vcp1	-5.43E+00	2.00E+01
Rp: vcp2	-9.80E-05	-4.27E-08
Rp: vcp3	-3.66E+00	2.49E+00
Rend: tce1	0.00868707	-0.0006397
Rend: tce2	-2.88E-05	1.18E-06
Rend: vce1	3.97E+00	7.83E-01
Rend: vce2	-2.99E+03	-8.65E+03
Rend: vce3	-2.01E+00	-7.67E-01

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Table 12.12.8: Unsilicided poly resistor model parameter table for N65ULP 1.0V/2.5V

Resistor Parameters	N+ poly w/o silicide	P+ poly w/o silicide
Rsh (ohm/sq)	153.4133674	690.0226806
Range	+18.0%/-18.0%-	+17.5%/-17.5%--
Rend0(ohm.m)	3.03E-06	1.04E-06
Rp: Jc1_0	0.468910868642278	0.0695053510675811
Rp: Jc1_w	-0.112938447121681	0.0269845671346735
Rp: Jc1_n	0.00691776661634369	0.000714977117664719
Rp: Tc1_0	0.000146777758646609	0.000326161317630646
Rp: Tc1_w	-3.23409625208756E-05	3.10855059871834E-06
Rp: Tc2_0	1.89557340140836E-07	8.05172629127237E-07
Rp: Tc2_w	8.47296898658068E-08	-2.79415787596679E-08
Rp: Jct_0	0.00382604564786152	-0.00425159480565355
Rp: Jct_w	-0.00234776917199985	2.26507523320411E-05
Rend: Jc1end_0	21.876715834462	27.900361735252
Rend: Jc1end_w	0	0
Rend: Tc1end_0	0.000876816730930428	-0.00141906402431781
Rend: Tc1end_w	0.00036855776757363	1.51517802655145E-05
Rend: Tc2end_0	5.63556101704174E-07	1.19263050938459E-06
Rend: Tc2end_w	-3.50561057125037E-07	5.77755688915007E-07
Rend: Jctend_0	0.00297141058822875	-0.00141455931220154
Rend: Jctend_w	-0.00196020344135713	0.000920093941015092

Table 12.12.9: Unsilicided poly resistor model parameter table for N55GP 1.0V/1.8V

Rs	W	L	PCM target	model (Rsh/corner)
N+PO(RPO)	0.45	36	-	154.0/29.8%/-30.4%
	1.8	36	-	142.7/19.7%/-20.5%
P+PO(RPO)	0.45	36	-	879.4/31.1%/-30.9%
	1.8	36	-	803.9/19.9%/-19.9%

Table 12.12.10: Unsilicided poly resistor model parameter table for N55GP 1.0V/2.5V

Rs	W	L	PCM target	model (Rsh/corner)
N+PO(RPO)	0.45	36	-	154.0/29.8%/-30.4%
	1.8	36	-	142.7/19.7%/-20.5%
P+PO(RPO)	0.45	36	-	879.4/31.1%/-30.9%
	1.8	36	-	803.9/19.9%/-19.9%

Table 12.12.10: Unsilicided poly resistor model parameter table for N55LP 1.2V/2.5V

Rs	W	L	PCM target	model (Rsh/corner)
N+PO(RPO)	0.5	40	-	179.87/30.4%/-30.8%
	2	40	-	161.35/19.8%/-20.6%
P+PO(RPO)	0.5	40	-	797.37/15.3%/-15.3%
	2	40	-	743/13.1%/-13.0%

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12.13 Unsilicided N+/P+ Diffusion Resistors Models

Both N+ and P+ type unsilicided diffusion resistor models are available in the current release. The cross-section schematic of this resistor structure is similar to what is shown in Fig. 12.13.1. The difference is that the poly resistor is replaced with diffusion resistor. These resistors were measured by sweeping current on one node, while grounding the other one. The back bias was kept at 0 volt during measurements. The valid current density range for these models is between 0 and 800 μA/μm width. TSMC further limits the application of these models only to resistors with width ≥ 0.4 μm and length ≥ 0.4 μm, and square number > 1. It is strongly recommended that all users should apply these models within valid current/voltage/dimension ranges. Application beyond the valid range will lead to a significant error.
The same equivalent circuit as the unsilicided poly resistor models was employed to model these diffusion resistors. The important model parameters are listed in Table 12.13.1~11.

Table 12.13.1: Unsilicided diffusion resistor model parameter table in N65LP 1.2V/2.5V.

Resistor Parameters	N+ diffusion w/o silicide	P+ diffusion w/o silicide
Rsh (ohm/sq)	120.0	245.2236546
Range	+19.3%/-19%-	+17.0%/-16%-
Rend0(ohm.m)	5.73E-06	2.88E-06
Rp: Jc1_0	0.106424864190149	0.111676986150315
Rp: Jc1_w	0.164977240163601	0.152379354165086
Rp: Jc1_n	0.0110803345857938	-0.00253193199710238
Rp: Tc1_0	0.0016375645345203	0.00134516723460811
Rp: Tc1_w	-1.06236946256314E-05	-1.93197505178018E-06
Rp: Tc2_0	5.58760711472759E-07	6.91556298384702E-07
Rp: Tc2_w	8.17454452868088E-08	5.99375320579376E-08
Rp: Jct_0	0.00244689689527551	0.00119863544617091
Rp: Jct_w	-0.00164118315706858	-0.00096981387975331
Rend: Jc1end_0	5.13022042122399	30.8120320049789
Rend: Jc1end_w	0	0
Rend: Tc1end_0	0.000858024695509284	7.97874855197876E-05
Rend: Tc1end_w	0.000108897460150394	4.99324114654573E-05
Rend: Tc2end_0	7.01952799620945E-07	-2.22863924323114E-07
Rend: Tc2end_w	-4.5518169088131E-07	-4.11818902290053E-08
Rend: Jctend_0	-0.00280558922243977	0.00951466816029306
Rend: Jctend_w	0.00230548862908327	-0.00277001356063046

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Table 12.13.2: Unsilicided diffusion resistor model parameter table in N65LP 1.2/3.3V.

Resistor Parameters	N+ diffusion w/o silicide	P+ diffusion w/o silicide
Rsh (ohm/sq)	120.0	245.2236546
Range	+19.3%/-19%	+17.0%/-16%
Rend0(ohm.m)	5.73E-06	2.88E-06
Rp: tcp1	0.0016257	0.0013736
Rp: tcp2	1.80E-06	4.71E-07
Rp: vcp1	-1.65	-0.0122
Rp: vcp2	-1.73E-05	-0.0000327
Rp: vcp3	-3.02	4.11
Rend: tce1	0.0014833	-0.000118905
Rend: tce2	-1.06E-05	-3.77E-06
Rend: vce1	3.43E-01	4.03E-01
Rend: vce2	-1.64E+03	-3.10E+03
Rend: vce3	-1.22E+00	-9.12E-01

Table 12.13.3: Unsilicided diffusion resistor model parameter table in N65G 1.0/1.8V.

Resistor Parameters	N+ diffusion w/o silicide	P+ diffusion W/o silicide
Rsh (ohm/sq)	113.3	260.6
Range (ohm/sq)	---	---
Rend0(ohm.m)	3.950E-06	8.976E-06
Rp: tcp1	1.645E-03	1.4E-03
Rp: tcp2	8.710E-07	7.9E-07
Rp: vcp1	0.1253	-0.0017
Rp: vcp2	2.16E-5	-9.3E-5
Rp: vcp3	1.6547	7.9378
Rend: tce1	2.239E-03	3.129E-05
Rend: tce2	1.513E-06	-1.107E-06
Rend: vce1	2.71	0.8333
Rend: vce2	-4180	-1630
Rend: vce3	-1.6823	-1.5743

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Table 12.13.4: Unsilicided diffusion resistor model parameter table in N65G 1.0/2.5V.

Resistor Parameters	N+ diffusion w/o silicide	P+ diffusion w/o silicide
Rsh (ohm/sq)	113.3	260.6
Range	---	---
Rend0(ohm.m)	3.950E-06	8.976E-06
Rp: tcp1	1.645E-03	1.4E-03
Rp: tcp2	8.710E-07	7.9E-07
Rp: vcp1	0.1253	-0.0017
Rp: vcp2	2.16E-5	-9.3E-5
Rp: vcp3	1.6547	7.9378
Rend: tce1	2.239E-03	3.129E-05
Rend: tce2	1.513E-06	-1.107E-06
Rend: vce1	2.71	0.8333
Rend: vce2	-4180	-1630
Rend: vce3	-1.6823	-1.5743

Table 12.13.5: Unsilicided diffusion resistor model parameter table in N65GP 1.0/1.8V.

Resistor Parameters	N+ diffusion w/o silicide	P+ diffusion w/o silicide
Rsh (ohm/sq)	104.14	257.35
Range (ohm/sq)	---	---
Rend0(ohm.m)	5.32E-06	4.98E-06
Rp: tcp1	1.58E-03	1.33E-03
Rp: tcp2	4.18E-07	5.71E-07
Rp: vcp1	1.12E-01	-1.37E-02
Rp: vcp2	1.17E-05	-5.50E-06
Rp: vcp3	1.58E+00	9.11E-01
Rend: tce1	2.51E-03	3.54E-04
Rend: tce2	-1.38E-06	1.59E-06
Rend: vce1	1.13E+00	7.68E-02
Rend: vce2	-2.31E+02	-1.34E+03
Rend: vce3	-1.35E+00	-4.98E-01

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Table 12.13.6: Unsilicided diffusion resistor model parameter table in N65GP 1.0/2.5V.

Resistor Parameters	N+ diffusion w/o silicide	P+ diffusion w/o silicide
Rsh (ohm/sq)	104.14	257.35
Range (ohm/sq)	---	---
Rend0(ohm.m)	5.32E-06	4.98E-06
Rp: tcp1	1.58E-03	1.33E-03
Rp: tcp2	4.18E-07	5.71E-07
Rp: vcp1	1.12E-01	-1.37E-02
Rp: vcp2	1.17E-05	-5.50E-06
Rp: vcp3	1.58E+00	9.11E-01
Rend: tce1	2.51E-03	3.54E-04
Rend: tce2	-1.38E-06	1.59E-06
Rend: vce1	1.13E+00	7.68E-02
Rend: vce2	-2.31E+02	-1.34E+03
Rend: vce3	-1.35E+00	-4.98E-01

Table 12.13.7: Unsilicided diffusion resistor model parameter table in N65LPG 1.0V(G),1.2(LP)/2.5V.

Resistor Parameters	N+ diffusion w/o silicide	P+ diffusion w/o silicide
Rsh (ohm/sq)	120.0	245.2236546
Range	+19.3%/-19%	+17.0%/-16%
Rend0(ohm.m)	5.73E-06	2.88E-06
Rp: tcp1	0.0016257	0.0013736
Rp: tcp2	1.80E-06	4.71E-07
Rp: vcp1	-1.65	-0.0122
Rp: vcp2	-1.73E-05	-0.0000327
Rp: vcp3	-3.02	4.11
Rend: tce1	0.0014833	-0.000118905
Rend: tce2	-1.06E-05	-3.77E-06
Rend: vce1	3.43E-01	4.03E-01
Rend: vce2	-1.64E+03	-3.10E+03
Rend: vce3	-1.22E+00	-9.12E-01

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Table 12.13.8: Unsilicided diffusion resistor model parameter table in N65ULP 1.0/2.5V.

Resistor Parameters	N+ diffusion w/o silicide	P+ diffusion w/o silicide
Rsh (ohm/sq)	120.0	245.2236546
Range	+19.3%/-19%-	+17.0%/-16%-
Rend0(ohm.m)	5.73E-06	2.88E-06
Rp: Jc1_0	0.106424864190149	0.111676986150315
Rp: Jc1_w	0.164977240163601	0.152379354165086
Rp: Jc1_n	0.0110803345857938	-0.00253193199710238
Rp: Tc1_0	0.0016375645345203	0.00134516723460811
Rp: Tc1_w	-1.06236946256314E-05	-1.93197505178018E-06
Rp: Tc2_0	5.58760711472759E-07	6.91556298384702E-07
Rp: Tc2_w	8.17454452868088E-08	5.99375320579376E-08
Rp: Jct_0	0.00244689689527551	0.00119863544617091
Rp: Jct_w	-0.00164118315706858	-0.00096981387975331
Rend: Jc1end_0	5.13022042122399	30.8120320049789
Rend: Jc1end_w	0	0
Rend: Tc1end_0	0.000858024695509284	7.97874855197876E-05
Rend: Tc1end_w	0.000108897460150394	4.99324114654573E-05
Rend: Tc2end_0	7.01952799620945E-07	-2.22863924323114E-07
Rend: Tc2end_w	-4.5518169088131E-07	-4.11818902290053E-08
Rend: Jctend_0	-0.00280558922243977	0.00951466816029306
Rend: Jctend_w	0.00230548862908327	-0.00277001356063046

Table 12.13.9: Unsilicided diffusion resistor model parameter table in N55GP 1.0/1.8V.

Rs	W	L	PCM target	model (Rsh/corner)
N+OD(PRO)	0.45	36	-	108.2/26.5%/-26.8%
	1.8	36	-	108.0/20.0%/-20.4%
P+OD(RPO)	0.45	36	-	263.6/32.6%/-32.4%
	1.8	36	-	262.5/19.7%/-20.1%

Table 12.13.10: Unsilicided diffusion resistor model parameter table in N55GP 1.0/2.5V.

Rs	W	L	PCM target	model (Rsh/corner)
N+OD(PRO)	0.45	36	-	108.2/26.5%/-26.8%
	1.8	36	-	108.0/20.0%/-20.4%
P+OD(RPO)	0.45	36	-	263.6/32.6%/-32.4%
	1.8	36	-	262.5/19.7%/-20.1%

Table 12.13.11: Unsilicided diffusion resistor model parameter table in N55LP 1.2/2.5V.

Rs	W	L	PCM target	model (Rsh/corner)
N+OD(PRO)	0.5	40	-	120.51/26.5%/-26.8%
	2	40	-	119.9/20.0%/-20.4%
P+OD(RPO)	0.5	40	-	244.37/32.0%/-31.9%
	2	40	-	249.4/19.7%/-20.1%

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12.14 Interconnect Model

12.14.1 Conductor Layers

tw = top width of metal
bw = bottom width of metal
ts = top space of metal
bs = bottom space of metal

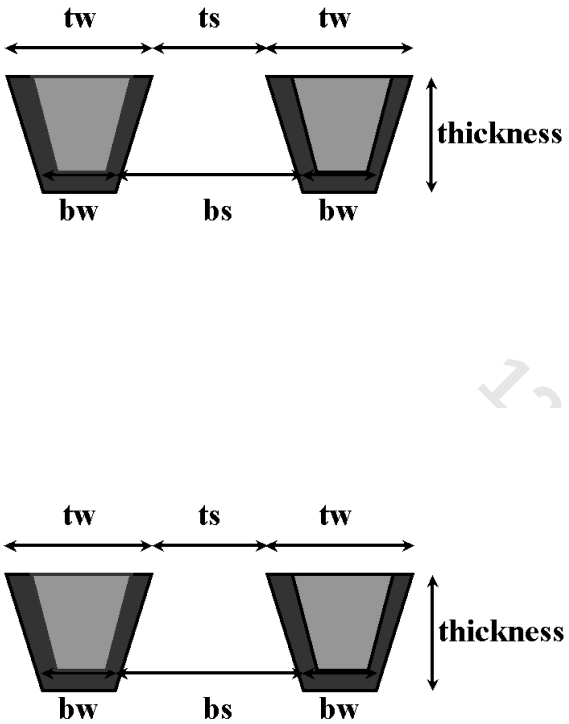

Figure12.14.1: Relations of trapezoidal width and spacing at top, and at bottom, respectively

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12.14.1.1M1MxMz process, no My/Mr, x=2~7, z=8~9

Table 12.14.1: Profiles of CLN65 metal layers

	Typical Thickness (Å)	Minimum Drawn Width (μm)	Minimum Drawn Spacing (μm)	On Silicon Width Bias At bottom (μm)	On Silicon Width bias At top (μm)	Maximum variation in thickness (%)	Maximum Variation in width (%)	Distance between conductor layer and substrate under STI (Å)
M10-AP RDL	14500	3	2	0.389	-0.034	+/-10	+/-10	69300
M9(Mz)	9000	0.4	0.4	0	0.1	+/-10	+/-10	52300
M8(Mz)	9000	0.4	0.4	0	0.1	+/-10	+/-10	37350
M7(Mx)	2200	0.1	0.1	-0.015	0.02	+/-15	+/-10	29200
M6(Mx)	2200	0.1	0.1	-0.015	0.02	+/-15	+/-10	25250
M5(Mx)	2200	0.1	0.1	-0.015	0.02	+/-15	+/-10	21300
M4(Mx)	2200	0.1	0.1	-0.015	0.02	+/-15	+/-10	17350
M3(Mx)	2200	0.1	0.1	-0.015	0.02	+/-15	+/-10	13400
M2(Mx)	2200	0.1	0.1	-0.015	0.02	+/-15	+/-10	9450
M1	1800	0.09	0.09	-0.005	0.02	+/-16.4	+/-10	5900
PO1(LP, LPG, ULP)	1000	0.06	0.12	-0.001	-0.001	+/-10	+/-7	3200
PO1(G)	1000	0.06	0.12	-0.013	-0.013	+/-10	+/-7	3200
PO1(GP)	1000	0.06	0.12	-0.019	-0.019	+/-10	+/-7	3200

Table 12.14.2: Profiles of CLN55 metal layers

	Typical Thickness (Å)	Minimum Drawn Width (μm)	Minimum Drawn Spacing (μm)	On Silicon Width Bias At bottom (m)	On Silicon Width bias At top (μm)	Maximum variation in thickness (%)	Maximum Variation in width (%)	Distance between conductor layer and substrate under FOX (Å)
M10-AP RDL	14500	2.7	1.8	0.35	-0.03	+/-10	+/-10	66050
M9(Mz)	9000	0.36	0.36	0.02	0.07	+/-10	+/-10	49800
M8(Mz)	9000	0.36	0.36	0.02	0.07	+/-10	+/-10	35400
M7(Mx)	2000	0.09	0.09	-0.015	0.015	+/-15	+/-10	28000
M6(Mx)	2000	0.09	0.09	-0.015	0.015	+/-15	+/-10	24250
M5(Mx)	2000	0.09	0.09	-0.015	0.015	+/-15	+/-10	20500
M4(Mx)	2000	0.09	0.09	-0.015	0.015	+/-15	+/-10	16750
M3(Mx)	2000	0.09	0.09	-0.015	0.015	+/-15	+/-10	13000
M2(Mx)	2000	0.09	0.09	-0.015	0.015	+/-15	+/-10	9250
M1	1600	0.081	0.081	-0.006	0.019	+/-16.4	+/-10	5900
PO1	1000	0.054	0.108	-0.015	-0.015	+/-10	+/-7	3200

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12.14.2 Dielectric Layers

12.14.2.1 M1MxMz process, no My/Mr, X=2~7, Z=8~9

Table 12.14.3: Profiles and properties of CLN65 each dielectric layer

Dielectric Name	Thickness (Å)	Variation +/- (%)	dielectric constant	Comments
PASS6	6,000	10	8.1	Side-wall thickness 4600A
PASS5	4,000	10	4.2	Side-wall thickness 3000A
PASS4	2,500	10	4.2	
PASS3	750	10	8.1	
PASS2	4,000	10	4.2	
PASS1	750	10	8.1	
IMD9c	7,750	10	4.2	
IMD9b	500	5	8.1	
IMD9a	6,200	7	4.2	IMD9a recess 750A after M9
IMD8d	500	5	5.0	
IMD8c	7,750	10	4.2	
IMD8b	500	5	8.1	
IMD8a	6,200	7	4.2	IMD8a recess 750A after M8
IMD7c	500	5	5.0	
IMD7b	2,200	15	2.9	
IMD7a	950	20	2.9	
IMD6d	300	5	4.2	
IMD6c	500	5	5.0	
IMD6b	2,200	15	2.9	
IMD6a	950	20	2.9	
IMD5d	300	5	4.2	
IMD5c	500	5	5.0	
IMD5b	2,200	15	2.9	
IMD5a	950	20	2.9	
IMD4d	300	5	4.2	
IMD4c	500	5	5.0	
IMD4b	2,200	15	2.9	
IMD4a	950	20	2.9	
IMD3d	300	5	4.2	
IMD3c	500	5	5.0	
IMD3b	2,200	15	2.9	
IMD3a	950	20	2.9	
IMD2d	300	5	4.2	
IMD2c	500	5	5.0	
IMD2b	2,200	15	2.9	
IMD2a	950	20	2.9	
IMD1d	300	5	4.2	
IMD1c	500	5	5.0	
IMD1b	1,300	16	2.9	
IMD1a	300	5	4.5	
ILD	3,100	15	4.2	ILD recess 200A after M1 etch
FOX	3,000	10	3.9	For spacer and liner, see Note: 1 and 2

NOTE 1: The depth of the STI is 3000 Å, while the final thickness of the FOX under PO1 is 3200 Å. This means that the FOX is about 200 Å higher than the OD.

NOTE 2: The spacer and liner around the Poly have been added to the schematic in Fig. 12.14.2 and are shown approximately. Their effective widths and dielectric constants are 370 Å and 6.25 for the dotted area and 200 Å and 7.5 for thick-lined area, respectively.

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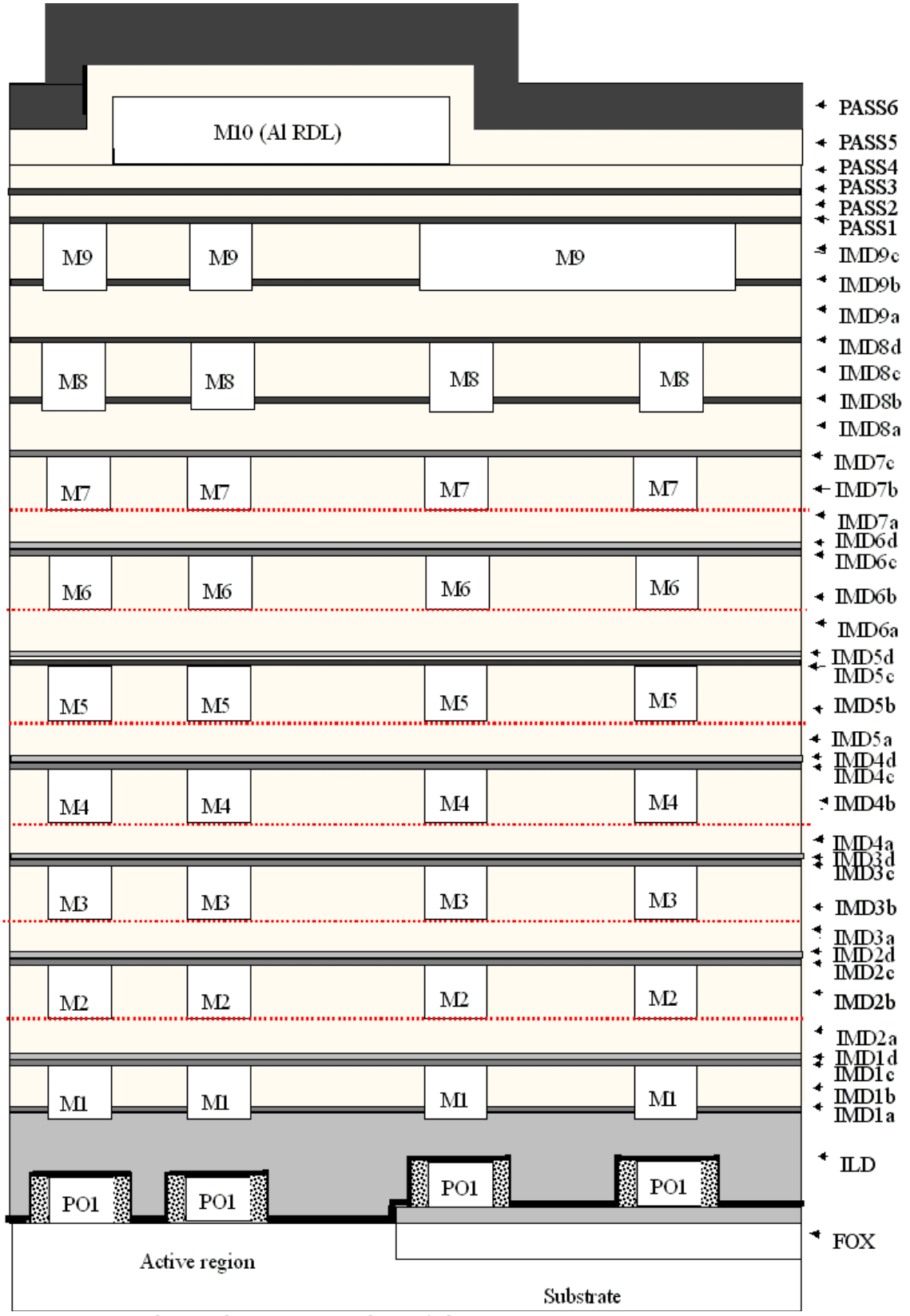

Figure12.14.2 A schematic cross-section of the CLN65 1P9M_AP_RDL process.

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Table 12.14.4: Profiles and properties of CLN55 each dielectric layer

Dielectric name	Thickness (Å)	Variation +/- (%)	Dielectric constant	Comments
PASS4	6,000	10	8.1	Side-wall thickness 4600A
PASS3	4,000	10	4.2	Side-wall thickness 3000A
PASS2	6,500	10	4.2	
PASS1	750	10	8.1	
IMD9c	7,750	10	4.2	
IMD9b	500	5	8.1	
IMD9a	5,650	7	4.2	IMD9a recess 750A after M9 etch
IMD8d	500	5	5.0	
IMD8c	7,750	10	4.2	
IMD8b	500	5	8.1	
IMD8a	5,650	7	4.2	IMD8a recess 750A after M8 etch
IMD7c	500	5	5.0	
IMD7b	2,000	15	2.9	
IMD7a	950	20	2.9	
IMD6d	300	5	4.2	
IMD6c	500	5	5.0	
IMD6b	2,000	15	2.9	
IMD6a	950	20	2.9	
IMD5d	300	5	4.2	
IMD5c	500	5	5.0	
IMD5b	2,000	15	2.9	
IMD5a	950	20	2.9	
IMD4d	300	5	4.2	
IMD4c	500	5	5.0	
IMD4b	2,000	15	2.9	
IMD4a	950	20	2.9	
IMD3d	300	5	4.2	
IMD3c	500	5	5.0	
IMD3b	2,000	15	2.9	
IMD3a	950	20	2.9	
IMD2d	300	5	4.2	
IMD2c	500	5	5.0	
IMD2b	2,000	15	2.9	
IMD2a	950	20	2.9	
IMD1d	300	5	4.2	
IMD1c	500	5	5.0	
IMD1b	1,100	16	2.9	
IMD1a	300	5	4.5	
ILD	3,100	15	4.2	ILD recess 200A after M1 etch
FOX	3,000	10	3.9	For **spacer and liner**, see Note: 1, 2 and 2

NOTE 1: The depth of the STI is 3000 Å, while the final thickness of the FOX under PO1 is 3200 Å. This means that the FOX is about 200 Å higher than the OD.

NOTE 2: The spacer and liner around the Poly have been added to the schematic in Fig. 12.14.3 and are shown approximately. Their effective widths and dielectric constants are 370 Å and 6.25 for the dotted area and 200 Å and 7.5 for thick-lined area, respectively.

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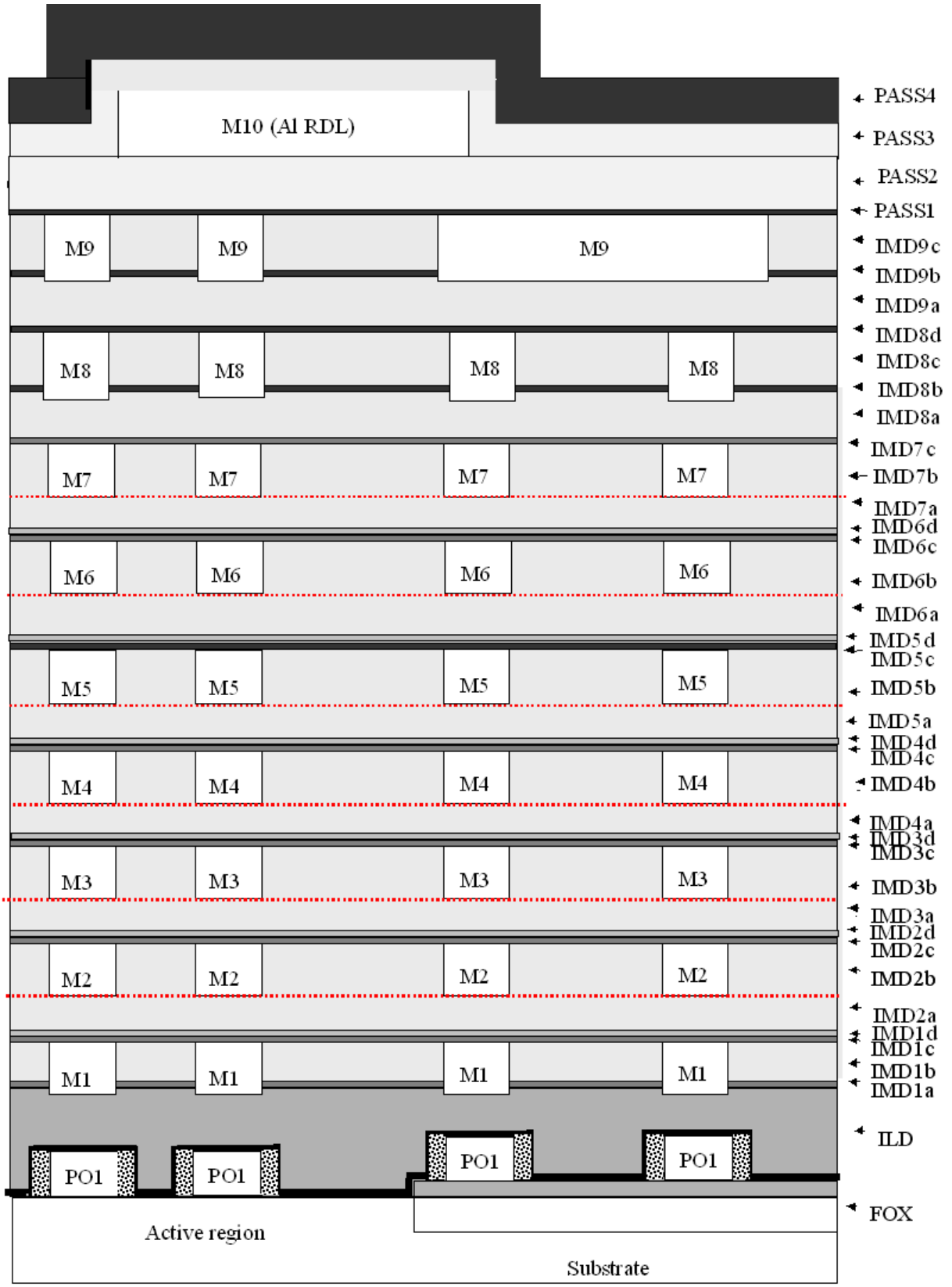

Figure12.14.2 A schematic cross-section of the CLN55 1P9M_AP_RDL process.

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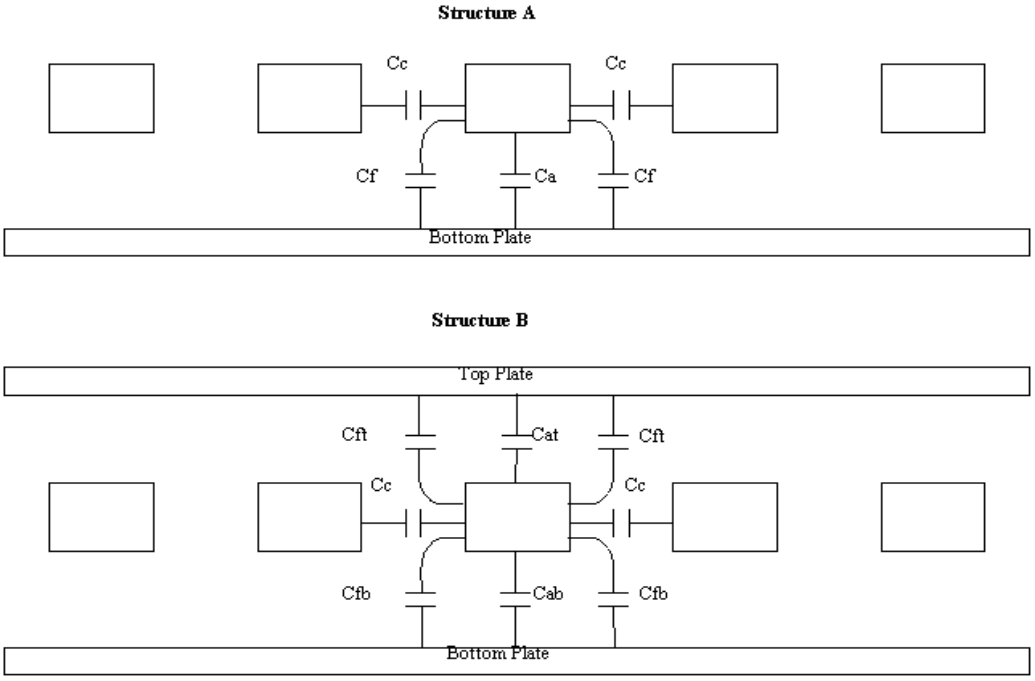
12.14.3 Interconnect line-to-line capacitance



The information in the following table applies to the structure in the preceding figure.

Structure A	
Cc	Coupling capacitance between top central trace and its neighboring traces
Ca	Area capacitance between top central trace and infinite bottom ground plate
Cf	Fringe capacitance per side between top central trace and infinite bottom ground plate
Cbottom	Ca + 2Cf
Csum	Ca + 2Cf + 2Cc
Ctotal	Total capacitance of the top central trace

Structure B	
Cc	Coupling capacitance between the middle central trace and its neighboring traces
Cat	Area capacitance between middle central trace and infinite top ground plate
Cab	Area capacitance between middle central trace and infinite bottom ground plate
Cft	Fringe capacitance per side between top central trace and infinite top ground plate
Cfb	Fringe capacitance per side between top central trace and infinite bottom ground plate
Ctop	Cat + 2Cft
Cbottom	Cab + 2Cfb
Csum	(Cat + 2Cft) + (Cab + 2Cfb) + 2Cc
Ctotal	Total capacitance of the middle central trace

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12.14.3.1M1MxMz process in CLN65LP 1.2V/2.5V, no My/Mr, x=2~7, z=8~9

12.14.3.1.1 Structure A 25 ℃

Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.98E-01	8.39E-02	2.99E-02	6.37E-03	1.17E-02	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.66E-02	1.74E-03	9.32E-02	6.37E-03	4.34E-02	100%
M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.39E-01	1.09E-01	2.03E-02	5.14E-03	7.58E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	8.44E-02	5.13E-03	7.41E-02	8.17E-03	3.30E-02	100%
M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.43E-01	1.06E-01	3.15E-02	1.09E-02	1.03E-02	100%
	0.09	2	0.1525	1.938	8.62E-02	1.11E-01	2.79E-03	1.06E-01	1.73E-02	4.41E-02	100%
M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.45E-01	1.01E-01	4.25E-02	1.66E-02	1.29E-02	100%
	0.09	2	0.1525	1.938	8.62E-02	1.32E-01	2.07E-03	1.28E-01	2.64E-02	5.06E-02	100%
M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.47E-01	1.00E-01	4.63E-02	1.86E-02	1.38E-02	100%
	0.09	2	0.1525	1.938	8.62E-02	1.38E-01	1.94E-03	1.34E-01	2.95E-02	5.24E-02	100%
M2-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.47E-02	1.62E-02	2.98E-03	6.59E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.90E-02	7.34E-03	5.43E-02	4.73E-03	2.48E-02	100%
M2-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.36E-02	1.90E-02	4.30E-03	7.34E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.66E-02	5.60E-03	6.54E-02	6.82E-03	2.93E-02	100%
M2-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.30E-02	2.04E-02	4.97E-03	7.72E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.02E-02	5.02E-03	7.02E-02	7.90E-03	3.11E-02	100%
M2-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.29E-02	2.07E-02	5.13E-03	7.81E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.10E-02	4.90E-03	7.12E-02	8.15E-03	3.15E-02	100%
M2-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.14E-01	8.65E-02	4.15E-02	1.51E-02	1.32E-02	100%
	0.1	2	0.1535	1.946	7.74E-02	1.21E-01	2.50E-03	1.16E-01	2.40E-02	4.58E-02	100%
M3-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.57E-02	1.36E-02	1.99E-03	5.78E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.22E-02	9.23E-03	4.37E-02	3.16E-03	2.03E-02	100%
M3-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.52E-02	1.48E-02	2.50E-03	6.15E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.55E-02	7.99E-03	4.95E-02	3.97E-03	2.28E-02	100%
M3-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.50E-02	1.53E-02	2.72E-03	6.29E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.69E-02	7.56E-03	5.18E-02	4.31E-03	2.37E-02	100%
M3-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.49E-02	1.54E-02	2.76E-03	6.32E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.72E-02	7.48E-03	5.23E-02	4.39E-03	2.39E-02	100%
M3-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.36E-02	1.88E-02	4.28E-03	7.27E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.63E-02	5.52E-03	6.52E-02	6.80E-03	2.92E-02	100%
M3-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.55E-02	4.14E-02	1.51E-02	1.32E-02	100%
	0.1	2	0.1535	1.946	7.74E-02	1.20E-01	2.43E-03	1.15E-01	2.40E-02	4.54E-02	100%
M4-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.62E-02	1.22E-02	1.49E-03	5.37E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.90E-02	1.07E-02	3.75E-02	2.37E-03	1.76E-02	100%
M4-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.59E-02	1.30E-02	1.76E-03	5.61E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.08E-02	9.83E-03	4.11E-02	2.80E-03	1.92E-02	100%
M4-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.58E-02	1.32E-02	1.87E-03	5.69E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.15E-02	9.52E-03	4.24E-02	2.97E-03	1.97E-02	100%
M4-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.58E-02	1.33E-02	1.89E-03	5.71E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.16E-02	9.46E-03	4.27E-02	3.00E-03	1.99E-02	100%
M4-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.52E-02	1.48E-02	2.50E-03	6.16E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.56E-02	7.98E-03	4.96E-02	3.97E-03	2.28E-02	100%
M4-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.26E-02	1.89E-02	4.28E-03	7.31E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.58E-02	5.42E-03	6.49E-02	6.80E-03	2.91E-02	100%
M4-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.55E-02	4.14E-02	1.51E-02	1.32E-02	100%
	0.1	2	0.1535	1.946	7.74E-02	1.20E-01	2.44E-03	1.15E-01	2.40E-02	4.54E-02	100%
M5-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.65E-02	1.15E-02	1.20E-03	5.13E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.74E-02	1.20E-02	3.35E-02	1.90E-03	1.58E-02	100%
M5-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.63E-02	1.20E-02	1.36E-03	5.30E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.85E-02	1.13E-02	3.59E-02	2.16E-03	1.69E-02	100%
M5-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.62E-02	1.21E-02	1.42E-03	5.35E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.89E-02	1.11E-02	3.68E-02	2.26E-03	1.73E-02	100%
M5-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.62E-02	1.22E-02	1.44E-03	5.37E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.90E-02	1.10E-02	3.70E-02	2.28E-03	1.74E-02	100%
M5-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.59E-02	1.31E-02	1.76E-03	5.65E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.11E-02	9.91E-03	4.13E-02	2.80E-03	1.93E-02	100%
M5-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.42E-02	1.49E-02	2.50E-03	6.23E-03	100%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.1	2	0.1535	1.946	7.74E-02	6.55E-02	7.95E-03	4.96E-02	3.97E-03	2.28E-02	100%
M5-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.26E-02	1.90E-02	4.28E-03	7.36E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.61E-02	5.50E-03	6.51E-02	6.80E-03	2.92E-02	100%
M5-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.55E-02	4.15E-02	1.51E-02	1.32E-02	100%
	0.1	2	0.1535	1.946	7.74E-02	1.20E-01	2.50E-03	1.15E-01	2.40E-02	4.54E-02	100%
M6-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.67E-02	1.10E-02	9.96E-04	5.02E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.72E-02	1.32E-02	3.07E-02	1.58E-03	1.46E-02	100%
M6-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.66E-02	1.14E-02	1.11E-03	5.15E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.79E-02	1.27E-02	3.25E-02	1.76E-03	1.54E-02	100%
M6-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.65E-02	1.15E-02	1.15E-03	5.20E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.82E-02	1.25E-02	3.31E-02	1.83E-03	1.56E-02	100%
M6-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.65E-02	1.16E-02	1.16E-03	5.21E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.82E-02	1.25E-02	3.32E-02	1.84E-03	1.57E-02	100%
M6-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.62E-02	1.22E-02	1.36E-03	5.42E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.95E-02	1.16E-02	3.62E-02	2.16E-03	1.70E-02	100%
M6-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.48E-02	1.34E-02	1.76E-03	5.80E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.17E-02	1.01E-02	4.14E-02	2.80E-03	1.93E-02	100%
M6-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.41E-02	1.52E-02	2.50E-03	6.37E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.65E-02	8.26E-03	4.99E-02	3.97E-03	2.30E-02	100%
M6-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.25E-02	1.93E-02	4.28E-03	7.49E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.69E-02	5.77E-03	6.54E-02	6.80E-03	2.93E-02	100%
M6-M5	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.53E-02	4.18E-02	1.51E-02	1.34E-02	100%
	0.1	2	0.1535	1.946	7.74E-02	1.19E-01	2.64E-03	1.14E-01	2.40E-02	4.50E-02	100%
M7-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.09E-01	9.86E-02	1.14E-02	8.54E-04	5.29E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.99E-02	1.56E-02	2.88E-02	1.36E-03	1.37E-02	100%
M7-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.08E-01	9.82E-02	1.17E-02	9.36E-04	5.39E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.05E-02	1.51E-02	3.02E-02	1.49E-03	1.43E-02	100%
M7-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.09E-01	9.84E-02	1.19E-02	9.65E-04	5.45E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.06E-02	1.50E-02	3.06E-02	1.53E-03	1.46E-02	100%
M7-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.09E-01	9.84E-02	1.19E-02	9.71E-04	5.46E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.07E-02	1.50E-02	3.07E-02	1.54E-03	1.46E-02	100%
M7-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.09E-01	9.82E-02	1.24E-02	1.11E-03	5.65E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.15E-02	1.43E-02	3.30E-02	1.76E-03	1.56E-02	100%
M7-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.65E-02	1.33E-02	1.36E-03	5.96E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.28E-02	1.30E-02	3.67E-02	2.16E-03	1.73E-02	100%
M7-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.60E-02	1.45E-02	1.76E-03	6.39E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.54E-02	1.16E-02	4.23E-02	2.80E-03	1.97E-02	100%
M7-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.51E-02	1.65E-02	2.50E-03	6.98E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.02E-02	9.59E-03	5.10E-02	3.97E-03	2.35E-02	100%
M7-M5	0.1	0.1	0.1025	0.0975	1.40E-01	2.08E-01	9.34E-02	2.08E-02	4.28E-03	8.24E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.03E-02	6.84E-03	6.66E-02	6.80E-03	2.99E-02	100%
M7-M6	0.1	0.1	0.1025	0.0975	1.40E-01	2.16E-01	8.61E-02	4.37E-02	1.51E-02	1.43E-02	100%
	0.1	2	0.1535	1.946	7.74E-02	1.24E-01	3.36E-03	1.17E-01	2.40E-02	4.65E-02	100%
M8-FOX	0.4	0.4	0.45	0.35	2.18E-02	3.07E-01	1.46E-01	1.55E-02	3.23E-03	6.15E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.09E-01	4.01E-02	2.85E-02	3.23E-03	1.26E-02	100%
M8-OD	0.4	0.4	0.45	0.35	2.18E-02	3.07E-01	1.46E-01	1.61E-02	3.47E-03	6.31E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.09E-01	3.97E-02	2.98E-02	3.47E-03	1.32E-02	100%
M8-PO1(OD)	0.4	0.4	0.45	0.35	2.18E-02	3.07E-01	1.45E-01	1.63E-02	3.56E-03	6.36E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.09E-01	3.96E-02	3.03E-02	3.56E-03	1.34E-02	100%
M8-PO1(FOX)	0.4	0.4	0.45	0.35	2.18E-02	3.07E-01	1.45E-01	1.63E-02	3.57E-03	6.37E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.09E-01	3.95E-02	3.04E-02	3.57E-03	1.34E-02	100%
M8-M1	0.4	0.4	0.45	0.35	2.18E-02	3.08E-01	1.45E-01	1.72E-02	3.96E-03	6.61E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.10E-01	3.89E-02	3.24E-02	3.96E-03	1.42E-02	100%
M8-M2	0.4	0.4	0.45	0.35	2.18E-02	3.08E-01	1.45E-01	1.86E-02	4.61E-03	6.98E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.12E-01	3.80E-02	3.58E-02	4.61E-03	1.56E-02	100%
M8-M3	0.4	0.4	0.45	0.35	2.18E-02	3.09E-01	1.44E-01	2.05E-02	5.51E-03	7.47E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.14E-01	3.68E-02	4.05E-02	5.51E-03	1.75E-02	100%
M8-M4	0.4	0.4	0.45	0.35	2.18E-02	3.03E-01	1.40E-01	2.32E-02	6.85E-03	8.20E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.17E-01	3.48E-02	4.70E-02	6.85E-03	2.01E-02	100%
M8-M5	0.4	0.4	0.45	0.35	2.18E-02	3.04E-01	1.38E-01	2.76E-02	9.05E-03	9.30E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.22E-01	3.25E-02	5.71E-02	9.05E-03	2.40E-02	100%
M8-M6	0.4	0.4	0.45	0.35	2.18E-02	3.08E-01	1.36E-01	3.59E-02	1.33E-02	1.13E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.32E-01	2.87E-02	7.46E-02	1.33E-02	3.06E-02	100%
M8-M7	0.4	0.4	0.45	0.35	2.18E-02	3.18E-01	1.30E-01	5.84E-02	2.53E-02	1.65E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.60E-01	2.33E-02	1.14E-01	2.53E-02	4.42E-02	100%
M9-FOX	0.4	0.4	0.45	0.35	2.18E-02	3.24E-01	1.55E-01	1.37E-02	2.45E-03	5.64E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.14E-01	4.50E-02	2.37E-02	2.45E-03	1.06E-02	100%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M9-OD	0.4	0.4	0.45	0.35	2.18E-02	3.25E-01	1.55E-01	1.41E-02	2.59E-03	5.75E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.14E-01	4.47E-02	2.45E-02	2.59E-03	1.09E-02	100%
M9-PO1(OD)	0.4	0.4	0.45	0.35	2.18E-02	3.25E-01	1.55E-01	1.42E-02	2.63E-03	5.78E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.14E-01	4.47E-02	2.47E-02	2.63E-03	1.10E-02	100%
M9-PO1(FOX)	0.4	0.4	0.45	0.35	2.18E-02	3.25E-01	1.55E-01	1.42E-02	2.64E-03	5.79E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.14E-01	4.46E-02	2.48E-02	2.64E-03	1.11E-02	100%
M9-M1	0.4	0.4	0.45	0.35	2.18E-02	3.25E-01	1.55E-01	1.47E-02	2.85E-03	5.94E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.14E-01	4.43E-02	2.59E-02	2.85E-03	1.15E-02	100%
M9-M2	0.4	0.4	0.45	0.35	2.18E-02	3.24E-01	1.54E-01	1.55E-02	3.17E-03	6.17E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.15E-01	4.38E-02	2.76E-02	3.17E-03	1.22E-02	100%
M9-M3	0.4	0.4	0.45	0.35	2.18E-02	3.25E-01	1.54E-01	1.64E-02	3.57E-03	6.43E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.16E-01	4.31E-02	2.98E-02	3.57E-03	1.31E-02	100%
M9-M4	0.4	0.4	0.45	0.35	2.18E-02	3.19E-01	1.51E-01	1.76E-02	4.09E-03	6.76E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.16E-01	4.19E-02	3.25E-02	4.09E-03	1.42E-02	100%
M9-M5	0.4	0.4	0.45	0.35	2.18E-02	3.18E-01	1.50E-01	1.91E-02	4.79E-03	7.17E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.18E-01	4.08E-02	3.60E-02	4.79E-03	1.56E-02	100%
M9-M6	0.4	0.4	0.45	0.35	2.18E-02	3.20E-01	1.49E-01	2.11E-02	5.77E-03	7.69E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.19E-01	3.90E-02	4.08E-02	5.77E-03	1.75E-02	100%
M9-M7	0.4	0.4	0.45	0.35	2.18E-02	3.20E-01	1.48E-01	2.40E-02	7.26E-03	8.38E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.22E-01	3.70E-02	4.78E-02	7.26E-03	2.03E-02	100%
M9-M8	0.4	0.4	0.45	0.35	2.18E-02	3.33E-01	1.37E-01	5.78E-02	2.53E-02	1.62E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.64E-01	2.56E-02	1.13E-01	2.53E-02	4.37E-02	100%
M10-FOX	3	2	3.178	1.822	2.10E-02	1.74E-01	7.29E-02	2.78E-02	1.64E-02	5.69E-03	100%
	3	8	3.178	7.822	2.10E-02	9.15E-02	2.06E-02	5.04E-02	1.64E-02	1.70E-02	100%
M10-OD	3	2	3.178	1.822	2.10E-02	1.74E-01	7.26E-02	2.88E-02	1.71E-02	5.83E-03	100%
	3	8	3.178	7.822	2.10E-02	9.26E-02	2.02E-02	5.23E-02	1.71E-02	1.76E-02	100%
M10-PO1(OD)	3	2	3.178	1.822	2.10E-02	1.74E-01	7.25E-02	2.91E-02	1.74E-02	5.88E-03	100%
	3	8	3.178	7.822	2.10E-02	9.30E-02	2.01E-02	5.29E-02	1.74E-02	1.77E-02	100%
M10-PO1(FOX)	3	2	3.178	1.822	2.10E-02	1.74E-01	7.25E-02	2.92E-02	1.74E-02	5.89E-03	100%
	3	8	3.178	7.822	2.10E-02	9.30E-02	2.00E-02	5.30E-02	1.74E-02	1.78E-02	100%
M10-M1	3	2	3.178	1.822	2.10E-02	1.74E-01	7.18E-02	3.06E-02	1.85E-02	6.07E-03	100%
	3	8	3.178	7.822	2.10E-02	9.46E-02	1.95E-02	5.55E-02	1.85E-02	1.85E-02	100%
M10-M2	3	2	3.178	1.822	2.10E-02	1.75E-01	7.10E-02	3.28E-02	2.00E-02	6.37E-03	100%
	3	8	3.178	7.822	2.10E-02	9.70E-02	1.88E-02	5.93E-02	2.00E-02	1.96E-02	100%
M10-M3	3	2	3.178	1.822	2.10E-02	1.78E-01	7.12E-02	3.53E-02	2.19E-02	6.73E-03	100%
	3	8	3.178	7.822	2.10E-02	9.97E-02	1.80E-02	6.36E-02	2.19E-02	2.09E-02	100%
M10-M4	3	2	3.178	1.822	2.10E-02	1.79E-01	7.01E-02	3.84E-02	2.41E-02	7.16E-03	100%
	3	8	3.178	7.822	2.10E-02	1.03E-01	1.70E-02	6.85E-02	2.41E-02	2.22E-02	100%
M10-M5	3	2	3.178	1.822	2.10E-02	1.79E-01	6.86E-02	4.21E-02	2.68E-02	7.69E-03	100%
	3	8	3.178	7.822	2.10E-02	1.07E-01	1.61E-02	7.47E-02	2.68E-02	2.39E-02	100%
M10-M6	3	2	3.178	1.822	2.10E-02	1.82E-01	6.74E-02	4.69E-02	3.01E-02	8.37E-03	100%
	3	8	3.178	7.822	2.10E-02	1.12E-01	1.50E-02	8.19E-02	3.01E-02	2.59E-02	100%
M10-M7	3	2	3.178	1.822	2.10E-02	1.85E-01	6.60E-02	5.29E-02	3.45E-02	9.22E-03	100%
	3	8	3.178	7.822	2.10E-02	1.18E-01	1.38E-02	9.09E-02	3.45E-02	2.82E-02	100%
M10-M8	3	2	3.178	1.822	2.10E-02	2.04E-01	5.97E-02	8.50E-02	5.75E-02	1.38E-02	100%
	3	8	3.178	7.822	2.10E-02	1.52E-01	9.78E-03	1.33E-01	5.75E-02	3.75E-02	100%
M10-M9	3	2	3.178	1.822	2.10E-02	3.30E-01	4.75E-02	2.35E-01	1.73E-01	3.09E-02	100%
	3	8	3.178	7.822	2.10E-02	3.01E-01	5.07E-03	2.91E-01	1.73E-01	5.89E-02	100%

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12.14.3.1.2 Structure B 25 ℃

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M1-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	2.01E-01	7.03E-02	1.99E-02	6.37E-03	6.76E-03	4.08E-02	4.77E-03	1.80E-02	100%
	0.06	2.4	0.059	2.401	1.49E+01	1.30E-01	4.01E-07	4.44E-02	6.37E-03	1.90E-02	8.53E-02	4.77E-03	4.03E-02	100%
M2-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.92E-01	7.82E-02	2.23E-02	6.37E-03	7.97E-03	1.32E-02	3.56E-03	4.80E-03	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.77E-02	3.93E-05	6.12E-02	6.37E-03	2.74E-02	3.64E-02	3.56E-03	1.64E-02	100%
M2-M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.39E-01	9.63E-02	1.27E-02	5.14E-03	3.78E-03	3.41E-02	1.95E-02	7.28E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.38E-01	1.31E-04	3.98E-02	8.17E-03	1.58E-02	9.75E-02	3.02E-02	3.37E-02	100%
M2-M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.42E-01	9.30E-02	2.37E-02	1.09E-02	6.42E-03	3.24E-02	1.95E-02	6.45E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.54E-01	8.81E-06	6.68E-02	1.73E-02	2.47E-02	8.76E-02	3.02E-02	2.87E-02	100%
M2-M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.46E-01	8.99E-02	3.45E-02	1.66E-02	8.95E-03	3.20E-02	1.95E-02	6.24E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.71E-01	1.65E-06	8.78E-02	2.64E-02	3.07E-02	8.29E-02	3.02E-02	2.63E-02	100%
M2-M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.48E-01	8.89E-02	3.82E-02	1.86E-02	9.82E-03	3.19E-02	1.95E-02	6.21E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.76E-01	1.10E-06	9.43E-02	2.95E-02	3.24E-02	8.18E-02	3.02E-02	2.58E-02	100%
M3-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.91E-01	7.96E-02	2.41E-02	6.37E-03	8.89E-03	7.82E-03	1.92E-03	2.95E-03	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.21E-02	1.90E-04	6.91E-02	6.37E-03	3.13E-02	2.27E-02	1.92E-03	1.04E-02	100%
M3-M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.32E-01	1.03E-01	1.41E-02	5.14E-03	4.46E-03	1.17E-02	5.54E-03	3.09E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	9.61E-02	7.39E-04	5.11E-02	8.17E-03	2.15E-02	4.35E-02	8.57E-03	1.75E-02	100%
M3-M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.35E-01	9.93E-02	2.52E-02	1.09E-02	7.17E-03	1.06E-02	5.54E-03	2.55E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.17E-01	1.76E-04	8.04E-02	1.73E-02	3.16E-02	3.66E-02	8.57E-03	1.40E-02	100%
M3-M2-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.13E-01	8.31E-02	8.56E-03	2.98E-03	2.79E-03	3.79E-02	2.13E-02	8.30E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.29E-01	3.73E-04	2.58E-02	4.73E-03	1.05E-02	1.02E-01	3.05E-02	3.58E-02	100%
M3-M2-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.13E-01	8.24E-02	1.15E-02	4.30E-03	3.59E-03	3.68E-02	2.13E-02	7.77E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.32E-01	1.29E-04	3.38E-02	6.82E-03	1.35E-02	9.80E-02	3.05E-02	3.37E-02	100%
M3-M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.39E-01	9.61E-02	3.62E-02	1.66E-02	9.77E-03	1.04E-02	5.54E-03	2.40E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.36E-01	8.46E-05	1.02E-01	2.64E-02	3.79E-02	3.35E-02	8.57E-03	1.25E-02	100%
M3-M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.40E-01	9.51E-02	3.99E-02	1.86E-02	1.07E-02	1.03E-02	5.54E-03	2.38E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.42E-01	7.16E-05	1.09E-01	2.95E-02	3.97E-02	3.28E-02	8.57E-03	1.21E-02	100%
M3-M2-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.13E-01	8.20E-02	1.29E-02	4.97E-03	3.98E-03	3.65E-02	2.13E-02	7.59E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.34E-01	7.80E-05	3.75E-02	7.90E-03	1.48E-02	9.63E-02	3.05E-02	3.29E-02	100%
M3-M2-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.14E-01	8.19E-02	1.33E-02	5.13E-03	4.07E-03	3.64E-02	2.13E-02	7.55E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.34E-01	6.99E-05	3.83E-02	8.15E-03	1.51E-02	9.59E-02	3.05E-02	3.27E-02	100%
M3-M2-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.21E-01	7.62E-02	3.35E-02	1.51E-02	9.20E-03	3.51E-02	2.13E-02	6.90E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.63E-01	2.01E-06	7.74E-02	2.40E-02	2.67E-02	8.53E-02	3.05E-02	2.74E-02	100%
M4-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.91E-01	8.01E-02	2.53E-02	6.37E-03	9.45E-03	5.64E-03	1.31E-03	2.17E-03	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.07E-02	4.00E-04	7.33E-02	6.37E-03	3.34E-02	1.66E-02	1.31E-03	7.66E-03	100%
M4-M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.31E-01	1.04E-01	1.52E-02	5.14E-03	5.03E-03	7.68E-03	3.23E-03	2.23E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	8.86E-02	1.54E-03	5.62E-02	8.17E-03	2.40E-02	2.93E-02	4.99E-03	1.22E-02	100%
M4-M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.34E-01	1.00E-01	2.65E-02	1.09E-02	7.81E-03	6.79E-03	3.23E-03	1.78E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.12E-01	5.57E-04	8.64E-02	1.73E-02	3.45E-02	2.41E-02	4.99E-03	9.54E-03	100%
M4-M2-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.04E-02	9.60E-03	2.98E-03	3.31E-03	1.33E-02	6.05E-03	3.61E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.46E-02	1.40E-03	3.38E-02	4.73E-03	1.45E-02	4.79E-02	8.67E-03	1.96E-02	100%
M4-M2-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	8.96E-02	1.26E-02	4.30E-03	4.13E-03	1.25E-02	6.05E-03	3.23E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.96E-02	7.62E-04	4.33E-02	6.82E-03	1.82E-02	4.48E-02	8.67E-03	1.81E-02	100%
M4-M3-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.38E-02	6.05E-03	1.99E-03	2.03E-03	3.88E-02	2.13E-02	8.74E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.26E-01	6.67E-04	1.86E-02	3.16E-03	7.72E-03	1.06E-01	3.05E-02	3.76E-02	100%
M4-M3-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.13E-01	8.36E-02	7.31E-03	2.50E-03	2.41E-03	3.81E-02	2.13E-02	8.42E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.27E-01	4.20E-04	2.24E-02	3.97E-03	9.20E-03	1.03E-01	3.05E-02	3.65E-02	100%
M4-M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.38E-01	9.70E-02	3.76E-02	1.66E-02	1.05E-02	6.54E-03	3.23E-03	1.66E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.31E-01	3.45E-04	1.08E-01	2.64E-02	4.10E-02	2.18E-02	4.99E-03	8.40E-03	100%
M4-M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.40E-01	9.60E-02	4.13E-02	1.86E-02	1.14E-02	6.50E-03	3.23E-03	1.63E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.37E-01	3.10E-04	1.15E-01	2.95E-02	4.28E-02	2.13E-02	4.99E-03	8.15E-03	100%
M4-M2-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	8.90E-02	1.40E-02	4.97E-03	4.52E-03	1.22E-02	6.05E-03	3.10E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	9.22E-02	5.92E-04	4.75E-02	7.90E-03	1.98E-02	4.35E-02	8.67E-03	1.74E-02	100%
M4-M2-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	8.89E-02	1.44E-02	5.13E-03	4.61E-03	1.22E-02	6.05E-03	3.07E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	9.29E-02	5.60E-04	4.85E-02	8.15E-03	2.02E-02	4.33E-02	8.67E-03	1.73E-02	100%
M4-M3-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.34E-02	7.83E-03	2.72E-03	2.55E-03	3.79E-02	2.13E-02	8.29E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.27E-01	3.49E-04	2.39E-02	4.31E-03	9.78E-03	1.03E-01	3.05E-02	3.61E-02	100%
M4-M3-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.33E-02	7.94E-03	2.76E-03	2.59E-03	3.78E-02	2.13E-02	8.27E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.27E-01	3.35E-04	2.42E-02	4.39E-03	9.91E-03	1.03E-01	3.05E-02	3.60E-02	100%
M4-M2-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.29E-02	3.48E-02	1.51E-02	9.87E-03	1.13E-02	6.05E-03	2.62E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.26E-01	1.17E-04	9.04E-02	2.40E-02	3.32E-02	3.56E-02	8.67E-03	1.35E-02	100%
M4-M3-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.13E-01	8.25E-02	1.14E-02	4.28E-03	3.54E-03	3.67E-02	2.13E-02	7.71E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.32E-01	1.08E-04	3.36E-02	6.80E-03	1.34E-02	9.79E-02	3.05E-02	3.37E-02	100%
M4-M3-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.21E-01	7.62E-02	3.35E-02	1.51E-02	9.20E-03	3.51E-02	2.13E-02	6.90E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.63E-01	1.97E-06	7.74E-02	2.40E-02	2.67E-02	8.53E-02	3.05E-02	2.74E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M5-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.91E-01	8.04E-02	2.60E-02	6.37E-03	9.82E-03	4.44E-03	9.97E-04	1.72E-03	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.06E-02	6.10E-04	7.62E-02	6.37E-03	3.49E-02	1.32E-02	9.97E-04	6.11E-03	100%
M5-M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.31E-01	1.04E-01	1.60E-02	5.14E-03	5.43E-03	5.83E-03	2.28E-03	1.77E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	8.58E-02	2.27E-03	5.90E-02	8.17E-03	2.54E-02	2.22E-02	3.52E-03	9.34E-03	100%
M5-M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.34E-01	1.01E-01	2.74E-02	1.09E-02	8.24E-03	5.06E-03	2.28E-03	1.39E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.10E-01	9.72E-04	8.96E-02	1.73E-02	3.62E-02	1.80E-02	3.52E-03	7.25E-03	100%
M5-M2-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.17E-02	1.05E-02	2.98E-03	3.78E-03	8.89E-03	3.52E-03	2.68E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.59E-02	2.57E-03	3.77E-02	4.73E-03	1.65E-02	3.30E-02	5.05E-03	1.40E-02	100%
M5-M2-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.08E-02	1.36E-02	4.30E-03	4.64E-03	8.23E-03	3.52E-03	2.35E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.17E-02	1.64E-03	4.79E-02	6.82E-03	2.05E-02	3.05E-02	5.05E-03	1.27E-02	100%
M5-M3-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.11E-02	6.96E-03	1.99E-03	2.49E-03	1.40E-02	6.05E-03	3.98E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.01E-02	2.10E-03	2.50E-02	3.16E-03	1.09E-02	5.09E-02	8.67E-03	2.11E-02	100%
M5-M3-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.08E-02	8.27E-03	2.50E-03	2.88E-03	1.35E-02	6.05E-03	3.71E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.20E-02	1.58E-03	2.97E-02	3.97E-03	1.28E-02	4.92E-02	8.67E-03	2.02E-02	100%
M5-M4-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.41E-02	4.73E-03	1.49E-03	1.62E-03	3.95E-02	2.13E-02	9.10E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.25E-01	9.64E-04	1.46E-02	2.37E-03	6.12E-03	1.08E-01	3.05E-02	3.87E-02	100%
M5-M4-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.39E-02	5.45E-03	1.76E-03	1.84E-03	3.90E-02	2.13E-02	8.88E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.25E-01	7.63E-04	1.68E-02	2.80E-03	7.01E-03	1.07E-01	3.05E-02	3.81E-02	100%
M5-M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.38E-01	9.73E-02	3.85E-02	1.66E-02	1.09E-02	4.84E-03	2.28E-03	1.28E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.29E-01	6.57E-04	1.12E-01	2.64E-02	4.27E-02	1.62E-02	3.52E-03	6.35E-03	100%
M5-M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.40E-01	9.63E-02	4.22E-02	1.86E-02	1.18E-02	4.80E-03	2.28E-03	1.26E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.35E-01	6.02E-04	1.18E-01	2.95E-02	4.45E-02	1.58E-02	3.52E-03	6.15E-03	100%
M5-M2-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.03E-02	1.51E-02	4.97E-03	5.04E-03	8.02E-03	3.52E-03	2.25E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.46E-02	1.37E-03	5.23E-02	7.90E-03	2.22E-02	2.96E-02	5.05E-03	1.23E-02	100%
M5-M2-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.02E-02	1.54E-02	5.13E-03	5.13E-03	7.97E-03	3.52E-03	2.22E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.53E-02	1.32E-03	5.33E-02	8.15E-03	2.26E-02	2.93E-02	5.05E-03	1.21E-02	100%
M5-M3-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.06E-02	8.80E-03	2.72E-03	3.04E-03	1.33E-02	6.05E-03	3.62E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.29E-02	1.41E-03	3.15E-02	4.31E-03	1.36E-02	4.85E-02	8.67E-03	1.99E-02	100%
M5-M3-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.06E-02	8.91E-03	2.76E-03	3.08E-03	1.33E-02	6.05E-03	3.60E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.30E-02	1.37E-03	3.19E-02	4.39E-03	1.38E-02	4.83E-02	8.67E-03	1.98E-02	100%
M5-M4-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.39E-02	5.73E-03	1.87E-03	1.93E-03	3.89E-02	2.13E-02	8.80E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.25E-01	6.98E-04	1.77E-02	2.97E-03	7.34E-03	1.06E-01	3.05E-02	3.78E-02	100%
M5-M4-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.39E-02	5.78E-03	1.89E-03	1.95E-03	3.89E-02	2.13E-02	8.78E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.25E-01	6.82E-04	1.78E-02	3.00E-03	7.41E-03	1.06E-01	3.05E-02	3.77E-02	100%
M5-M2-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.39E-02	3.61E-02	1.51E-02	1.05E-02	7.18E-03	3.52E-03	1.83E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.21E-01	4.48E-04	9.64E-02	2.40E-02	3.62E-02	2.35E-02	5.05E-03	9.21E-03	100%
M5-M3-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	8.95E-02	1.24E-02	4.28E-03	4.07E-03	1.24E-02	6.05E-03	3.19E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.93E-02	7.23E-04	4.31E-02	6.80E-03	1.82E-02	4.47E-02	8.67E-03	1.80E-02	100%
M5-M4-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.35E-02	7.29E-03	2.50E-03	2.40E-03	3.81E-02	2.13E-02	8.40E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.27E-01	4.12E-04	2.24E-02	3.97E-03	9.20E-03	1.04E-01	3.05E-02	3.65E-02	100%
M5-M3-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.29E-02	3.48E-02	1.51E-02	9.87E-03	1.13E-02	6.05E-03	2.62E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.26E-01	1.17E-04	9.04E-02	2.40E-02	3.32E-02	3.56E-02	8.67E-03	1.35E-02	100%
M5-M4-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.13E-01	8.25E-02	1.14E-02	4.28E-03	3.54E-03	3.67E-02	2.13E-02	7.71E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.32E-01	1.08E-04	3.36E-02	6.80E-03	1.34E-02	9.79E-02	3.05E-02	3.37E-02	100%
M5-M4-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.21E-01	7.62E-02	3.35E-02	1.51E-02	9.20E-03	3.51E-02	2.13E-02	6.90E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.63E-01	1.97E-06	7.74E-02	2.40E-02	2.67E-02	8.53E-02	3.05E-02	2.74E-02	100%
M6-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.92E-01	8.08E-02	2.65E-02	6.37E-03	1.01E-02	3.67E-03	8.04E-04	1.43E-03	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.07E-02	7.93E-04	7.81E-02	6.37E-03	3.59E-02	1.10E-02	8.04E-04	5.08E-03	100%
M6-M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.31E-01	1.05E-01	1.66E-02	5.14E-03	5.72E-03	4.73E-03	1.76E-03	1.48E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	8.46E-02	2.85E-03	6.10E-02	8.17E-03	2.64E-02	1.79E-02	2.72E-03	7.60E-03	100%
M6-M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.34E-01	1.01E-01	2.80E-02	1.09E-02	8.55E-03	4.06E-03	1.76E-03	1.15E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.09E-01	1.32E-03	9.17E-02	1.73E-02	3.72E-02	1.44E-02	2.72E-03	5.86E-03	100%
M6-M2-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.22E-02	1.13E-02	2.98E-03	4.14E-03	6.87E-03	2.49E-03	2.19E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.25E-02	3.56E-03	4.00E-02	4.73E-03	1.76E-02	2.53E-02	3.56E-03	1.09E-02	100%
M6-M2-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.13E-02	1.43E-02	4.30E-03	5.01E-03	6.29E-03	2.49E-03	1.90E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.88E-02	2.46E-03	5.05E-02	6.82E-03	2.19E-02	2.33E-02	3.56E-03	9.89E-03	100%
M6-M3-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.25E-02	7.79E-03	1.99E-03	2.90E-03	9.56E-03	3.52E-03	3.02E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.07E-02	3.58E-03	2.81E-02	3.16E-03	1.25E-02	3.54E-02	5.05E-03	1.52E-02	100%
M6-M3-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.21E-02	9.15E-03	2.50E-03	3.32E-03	9.09E-03	3.52E-03	2.78E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.31E-02	2.88E-03	3.33E-02	3.97E-03	1.47E-02	3.40E-02	5.05E-03	1.45E-02	100%
M6-M4-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.14E-02	5.56E-03	1.49E-03	2.03E-03	1.46E-02	6.05E-03	4.29E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.83E-02	2.74E-03	1.99E-02	2.37E-03	8.76E-03	5.29E-02	8.67E-03	2.21E-02	100%
M6-M4-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.13E-02	6.33E-03	1.76E-03	2.28E-03	1.42E-02	6.05E-03	4.09E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.93E-02	2.35E-03	2.28E-02	2.80E-03	9.98E-03	5.18E-02	8.67E-03	2.16E-02	100%
M6-M5-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.42E-02	3.90E-03	1.20E-03	1.35E-03	4.00E-02	2.13E-02	9.37E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.24E-01	1.22E-03	1.21E-02	1.90E-03	5.08E-03	1.10E-01	3.05E-02	3.96E-02	100%
M6-M5-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.41E-02	4.37E-03	1.36E-03	1.50E-03	3.97E-02	2.13E-02	9.20E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.25E-01	1.07E-03	1.35E-02	2.16E-03	5.68E-03	1.09E-01	3.05E-02	3.92E-02	100%
M6-M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.38E-01	9.75E-02	3.91E-02	1.66E-02	1.12E-02	3.86E-03	1.76E-03	1.05E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.29E-01	9.35E-04	1.14E-01	2.64E-02	4.38E-02	1.29E-02	2.72E-03	5.11E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M6-M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.40E-01	9.65E-02	4.29E-02	1.86E-02	1.21E-02	3.83E-03	1.76E-03	1.03E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	1.35E-01	8.59E-04	1.21E-01	2.95E-02	4.55E-02	1.26E-02	2.72E-03	4.94E-03	100%
M6-M2-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.08E-02	1.58E-02	4.97E-03	5.43E-03	6.10E-03	2.49E-03	1.81E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.18E-02	2.11E-03	5.51E-02	7.90E-03	2.36E-02	2.25E-02	3.56E-03	9.47E-03	100%
M6-M2-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.07E-02	1.62E-02	5.13E-03	5.52E-03	6.06E-03	2.49E-03	1.79E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.25E-02	2.04E-03	5.61E-02	8.15E-03	2.40E-02	2.23E-02	3.56E-03	9.39E-03	100%
M6-M3-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.20E-02	9.70E-03	2.72E-03	3.49E-03	8.93E-03	3.52E-03	2.70E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.40E-02	2.63E-03	3.53E-02	4.31E-03	1.55E-02	3.35E-02	5.05E-03	1.42E-02	100%
M6-M3-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.20E-02	9.82E-03	2.76E-03	3.53E-03	8.90E-03	3.52E-03	2.69E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.43E-02	2.58E-03	3.57E-02	4.39E-03	1.57E-02	3.34E-02	5.05E-03	1.42E-02	100%
M6-M4-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.12E-02	6.61E-03	1.87E-03	2.37E-03	1.41E-02	6.05E-03	4.03E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.95E-02	2.20E-03	2.38E-02	2.97E-03	1.04E-02	5.13E-02	8.67E-03	2.13E-02	100%
M6-M4-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.12E-02	6.68E-03	1.89E-03	2.39E-03	1.41E-02	6.05E-03	4.01E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.96E-02	2.17E-03	2.40E-02	3.00E-03	1.05E-02	5.13E-02	8.67E-03	2.13E-02	100%
M6-M5-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.41E-02	4.54E-03	1.42E-03	1.56E-03	3.96E-02	2.13E-02	9.15E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.24E-01	1.01E-03	1.40E-02	2.26E-03	5.89E-03	1.08E-01	3.05E-02	3.90E-02	100%
M6-M5-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.41E-02	4.58E-03	1.44E-03	1.57E-03	3.96E-02	2.13E-02	9.14E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.25E-01	1.00E-03	1.41E-02	2.28E-03	5.93E-03	1.08E-01	3.05E-02	3.89E-02	100%
M6-M2-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.44E-02	3.70E-02	1.51E-02	1.10E-02	5.35E-03	2.49E-03	1.43E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.19E-01	8.30E-04	9.96E-02	2.40E-02	3.78E-02	1.76E-02	3.56E-03	7.02E-03	100%
M6-M3-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.09E-02	1.34E-02	4.28E-03	4.57E-03	8.19E-03	3.52E-03	2.33E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.14E-02	1.60E-03	4.77E-02	6.80E-03	2.04E-02	3.05E-02	5.05E-03	1.27E-02	100%
M6-M4-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.08E-02	8.25E-03	2.50E-03	2.88E-03	1.35E-02	6.05E-03	3.71E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.20E-02	1.57E-03	2.97E-02	3.97E-03	1.28E-02	4.92E-02	8.67E-03	2.03E-02	100%
M6-M5-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.40E-02	5.45E-03	1.76E-03	1.84E-03	3.90E-02	2.13E-02	8.88E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.25E-01	7.64E-04	1.68E-02	2.80E-03	7.01E-03	1.07E-01	3.05E-02	3.81E-02	100%
M6-M3-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.39E-02	3.61E-02	1.51E-02	1.05E-02	7.18E-03	3.52E-03	1.83E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.21E-01	4.45E-04	9.62E-02	2.40E-02	3.61E-02	2.35E-02	5.05E-03	9.20E-03	100%
M6-M4-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	8.95E-02	1.24E-02	4.28E-03	4.07E-03	1.24E-02	6.05E-03	3.19E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.92E-02	7.19E-04	4.31E-02	6.80E-03	1.81E-02	4.47E-02	8.67E-03	1.80E-02	100%
M6-M5-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.35E-02	7.29E-03	2.50E-03	2.40E-03	3.81E-02	2.13E-02	8.40E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.27E-01	4.10E-04	2.23E-02	3.97E-03	9.18E-03	1.03E-01	3.05E-02	3.65E-02	100%
M6-M4-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.29E-02	3.48E-02	1.51E-02	9.87E-03	1.13E-02	6.05E-03	2.62E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.26E-01	1.17E-04	9.04E-02	2.40E-02	3.32E-02	3.56E-02	8.67E-03	1.35E-02	100%
M6-M5-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.13E-01	8.25E-02	1.14E-02	4.28E-03	3.54E-03	3.67E-02	2.13E-02	7.71E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.32E-01	1.08E-04	3.36E-02	6.80E-03	1.34E-02	9.79E-02	3.05E-02	3.37E-02	100%
M6-M5-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.21E-01	7.62E-02	3.35E-02	1.51E-02	9.20E-03	3.51E-02	2.13E-02	6.90E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.63E-01	1.97E-06	7.74E-02	2.40E-02	2.67E-02	8.53E-02	3.05E-02	2.74E-02	100%
M7-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.92E-01	8.08E-02	2.70E-02	6.37E-03	1.03E-02	3.13E-03	6.74E-04	1.23E-03	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.09E-02	9.37E-04	7.96E-02	6.37E-03	3.66E-02	9.38E-03	6.74E-04	4.35E-03	100%
M7-M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.32E-01	1.05E-01	1.70E-02	5.14E-03	5.94E-03	3.99E-03	1.43E-03	1.28E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	8.38E-02	3.26E-03	6.22E-02	8.17E-03	2.70E-02	1.50E-02	2.22E-03	6.40E-03	100%
M7-M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.35E-01	1.01E-01	2.84E-02	1.09E-02	8.77E-03	3.39E-03	1.43E-03	9.77E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.09E-01	1.60E-03	9.33E-02	1.73E-02	3.80E-02	1.21E-02	2.22E-03	4.92E-03	100%
M7-M2-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.26E-02	1.18E-02	2.98E-03	4.41E-03	5.65E-03	1.92E-03	1.86E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.06E-02	4.31E-03	4.15E-02	4.73E-03	1.84E-02	2.06E-02	2.75E-03	8.90E-03	100%
M7-M2-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.15E-02	1.49E-02	4.30E-03	5.30E-03	5.13E-03	1.92E-03	1.61E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.72E-02	3.07E-03	5.22E-02	6.82E-03	2.27E-02	1.89E-02	2.75E-03	8.06E-03	100%
M7-M3-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.32E-02	8.44E-03	1.99E-03	3.22E-03	7.48E-03	2.49E-03	2.50E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.67E-02	4.75E-03	3.00E-02	3.16E-03	1.34E-02	2.73E-02	3.56E-03	1.18E-02	100%
M7-M3-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.27E-02	9.83E-03	2.50E-03	3.67E-03	7.06E-03	2.49E-03	2.29E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.93E-02	3.93E-03	3.53E-02	3.97E-03	1.57E-02	2.61E-02	3.56E-03	1.13E-02	100%
M7-M4-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.30E-02	6.31E-03	1.49E-03	2.41E-03	1.01E-02	3.52E-03	3.30E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.83E-02	4.41E-03	2.25E-02	2.37E-03	1.01E-02	3.69E-02	5.05E-03	1.59E-02	100%
M7-M4-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.26E-02	7.12E-03	1.76E-03	2.68E-03	9.77E-03	3.52E-03	3.12E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.95E-02	3.89E-03	2.57E-02	2.80E-03	1.14E-02	3.60E-02	5.05E-03	1.55E-02	100%
M7-M5-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.17E-02	4.66E-03	1.20E-03	1.73E-03	1.51E-02	6.05E-03	4.53E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.72E-02	3.22E-03	1.65E-02	1.90E-03	7.32E-03	5.42E-02	8.67E-03	2.28E-02	100%
M7-M5-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.15E-02	5.17E-03	1.36E-03	1.90E-03	1.48E-02	6.05E-03	4.38E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.78E-02	2.93E-03	1.85E-02	2.16E-03	8.15E-03	5.34E-02	8.67E-03	2.24E-02	100%
M7-M6-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.13E-01	8.44E-02	3.32E-03	9.96E-04	1.16E-03	4.04E-02	2.13E-02	9.57E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.24E-01	1.41E-03	1.02E-02	1.58E-03	4.33E-03	1.11E-01	3.05E-02	4.02E-02	100%
M7-M6-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.42E-02	3.65E-03	1.11E-03	1.27E-03	4.02E-02	2.13E-02	9.45E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.24E-01	1.29E-03	1.13E-02	1.76E-03	4.76E-03	1.10E-01	3.05E-02	3.98E-02	100%
M7-M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.39E-01	9.81E-02	3.95E-02	1.66E-02	1.15E-02	3.22E-03	1.43E-03	8.90E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.29E-01	1.15E-03	1.16E-01	2.64E-02	4.46E-02	1.08E-02	2.22E-03	4.29E-03	100%
M7-M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.41E-01	9.70E-02	4.33E-02	1.86E-02	1.24E-02	3.18E-03	1.43E-03	8.74E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.35E-01	1.07E-03	1.22E-01	2.95E-02	4.64E-02	1.05E-02	2.22E-03	4.14E-03	100%
M7-M2-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.10E-02	1.64E-02	4.97E-03	5.72E-03	4.96E-03	1.92E-03	1.52E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.04E-02	2.68E-03	5.68E-02	7.90E-03	2.45E-02	1.82E-02	2.75E-03	7.73E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M7-M2-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.09E-02	1.68E-02	5.13E-03	5.82E-03	4.93E-03	1.92E-03	1.50E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.12E-02	2.61E-03	5.79E-02	8.15E-03	2.49E-02	1.81E-02	2.75E-03	7.65E-03	100%
M7-M3-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.25E-02	1.04E-02	2.72E-03	3.84E-03	6.92E-03	2.49E-03	2.21E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.05E-02	3.66E-03	3.74E-02	4.31E-03	1.66E-02	2.57E-02	3.56E-03	1.11E-02	100%
M7-M3-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.25E-02	1.05E-02	2.76E-03	3.87E-03	6.89E-03	2.49E-03	2.20E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.07E-02	3.60E-03	3.79E-02	4.39E-03	1.67E-02	2.56E-02	3.56E-03	1.10E-02	100%
M7-M4-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.26E-02	7.42E-03	1.87E-03	2.78E-03	9.65E-03	3.52E-03	3.06E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.00E-02	3.71E-03	2.68E-02	2.97E-03	1.19E-02	3.57E-02	5.05E-03	1.53E-02	100%
M7-M4-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.26E-02	7.49E-03	1.89E-03	2.80E-03	9.63E-03	3.52E-03	3.05E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.01E-02	3.67E-03	2.71E-02	3.00E-03	1.20E-02	3.56E-02	5.05E-03	1.53E-02	100%
M7-M5-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.14E-02	5.35E-03	1.42E-03	1.97E-03	1.47E-02	6.05E-03	4.33E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.80E-02	2.83E-03	1.91E-02	2.26E-03	8.44E-03	5.32E-02	8.67E-03	2.23E-02	100%
M7-M5-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.14E-02	5.39E-03	1.44E-03	1.98E-03	1.47E-02	6.05E-03	4.32E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.80E-02	2.81E-03	1.93E-02	2.28E-03	8.50E-03	5.31E-02	8.67E-03	2.22E-02	100%
M7-M6-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.42E-02	3.77E-03	1.15E-03	1.31E-03	4.01E-02	2.13E-02	9.41E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.24E-01	1.26E-03	1.17E-02	1.83E-03	4.92E-03	1.10E-01	3.05E-02	3.97E-02	100%
M7-M6-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.42E-02	3.80E-03	1.16E-03	1.32E-03	4.01E-02	2.13E-02	9.40E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.24E-01	1.25E-03	1.17E-02	1.84E-03	4.95E-03	1.10E-01	3.05E-02	3.97E-02	100%
M7-M2-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.46E-02	3.77E-02	1.51E-02	1.13E-02	4.28E-03	1.92E-03	1.18E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.16E-03	1.02E-01	2.40E-02	3.89E-02	1.41E-02	2.75E-03	5.68E-03	100%
M7-M3-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.13E-02	1.42E-02	4.28E-03	4.95E-03	6.25E-03	2.49E-03	1.88E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.84E-02	2.40E-03	5.03E-02	6.80E-03	2.18E-02	2.33E-02	3.56E-03	9.87E-03	100%
M7-M4-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.21E-02	9.13E-03	2.50E-03	3.31E-03	9.08E-03	3.52E-03	2.78E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.30E-02	2.86E-03	3.33E-02	3.97E-03	1.46E-02	3.40E-02	5.05E-03	1.45E-02	100%
M7-M5-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.12E-02	6.32E-03	1.76E-03	2.28E-03	1.42E-02	6.05E-03	4.09E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.92E-02	2.34E-03	2.27E-02	2.80E-03	9.97E-03	5.18E-02	8.67E-03	2.16E-02	100%
M7-M6-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.41E-02	4.37E-03	1.36E-03	1.50E-03	3.97E-02	2.13E-02	9.21E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.25E-01	1.07E-03	1.35E-02	2.16E-03	5.68E-03	1.09E-01	3.05E-02	3.92E-02	100%
M7-M3-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.44E-02	3.70E-02	1.51E-02	1.10E-02	5.35E-03	2.49E-03	1.43E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.19E-01	8.26E-04	9.95E-02	2.40E-02	3.78E-02	1.76E-02	3.56E-03	7.01E-03	100%
M7-M4-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.08E-02	1.34E-02	4.28E-03	4.57E-03	8.18E-03	3.52E-03	2.33E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.13E-02	1.59E-03	4.76E-02	6.80E-03	2.04E-02	3.05E-02	5.05E-03	1.27E-02	100%
M7-M5-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.08E-02	8.25E-03	2.50E-03	2.88E-03	1.35E-02	6.05E-03	3.71E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.19E-02	1.56E-03	2.96E-02	3.97E-03	1.28E-02	4.92E-02	8.67E-03	2.02E-02	100%
M7-M6-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.39E-02	5.45E-03	1.76E-03	1.84E-03	3.90E-02	2.13E-02	8.88E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.25E-01	7.60E-04	1.68E-02	2.80E-03	7.00E-03	1.07E-01	3.05E-02	3.81E-02	100%
M7-M4-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.39E-02	3.61E-02	1.51E-02	1.05E-02	7.18E-03	3.52E-03	1.83E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.21E-01	4.45E-04	9.62E-02	2.40E-02	3.61E-02	2.35E-02	5.05E-03	9.20E-03	100%
M7-M5-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	8.95E-02	1.24E-02	4.28E-03	4.07E-03	1.24E-02	6.05E-03	3.19E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.92E-02	7.19E-04	4.31E-02	6.80E-03	1.81E-02	4.47E-02	8.67E-03	1.80E-02	100%
M7-M6-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.35E-02	7.29E-03	2.50E-03	2.40E-03	3.81E-02	2.13E-02	8.40E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.27E-01	4.10E-04	2.23E-02	3.97E-03	9.18E-03	1.03E-01	3.05E-02	3.65E-02	100%
M7-M5-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.29E-02	3.48E-02	1.51E-02	9.87E-03	1.13E-02	6.05E-03	2.62E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.26E-01	1.17E-04	9.04E-02	2.40E-02	3.32E-02	3.56E-02	8.67E-03	1.35E-02	100%
M7-M6-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.13E-01	8.25E-02	1.14E-02	4.28E-03	3.54E-03	3.67E-02	2.13E-02	7.71E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.32E-01	1.08E-04	3.36E-02	6.80E-03	1.34E-02	9.79E-02	3.05E-02	3.37E-02	100%
M7-M6-M5	0.1	0.1	0.1025	0.0975	1.40E-01	2.21E-01	7.62E-02	3.35E-02	1.51E-02	9.20E-03	3.51E-02	2.13E-02	6.90E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.63E-01	1.97E-06	7.74E-02	2.40E-02	2.67E-02	8.53E-02	3.05E-02	2.74E-02	100%
M8-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.94E-01	8.18E-02	2.75E-02	6.37E-03	1.06E-02	2.50E-03	5.27E-04	9.87E-04	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.08E-02	1.09E-03	8.11E-02	6.37E-03	3.74E-02	7.48E-03	5.27E-04	3.48E-03	100%
M8-M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.32E-01	1.06E-01	1.76E-02	5.14E-03	6.22E-03	3.16E-03	1.09E-03	1.04E-03	100%
	0.09	2	0.1525	1.938	8.62E-02	8.32E-02	3.76E-03	6.38E-02	8.17E-03	2.78E-02	1.18E-02	1.68E-03	5.06E-03	100%
M8-M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.35E-01	1.02E-01	2.90E-02	1.09E-02	9.05E-03	2.65E-03	1.09E-03	7.80E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.08E-01	1.92E-03	9.50E-02	1.73E-02	3.89E-02	9.40E-03	1.68E-03	3.86E-03	100%
M8-M2-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.28E-02	1.25E-02	2.98E-03	4.77E-03	4.38E-03	1.38E-03	1.50E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.93E-02	5.19E-03	4.33E-02	4.73E-03	1.93E-02	1.56E-02	1.98E-03	6.83E-03	100%
M8-M2-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.18E-02	1.56E-02	4.30E-03	5.66E-03	3.93E-03	1.38E-03	1.27E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.61E-02	3.82E-03	5.42E-02	6.82E-03	2.37E-02	1.43E-02	1.98E-03	6.16E-03	100%
M8-M3-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.36E-02	9.27E-03	1.99E-03	3.64E-03	5.59E-03	1.65E-03	1.97E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.39E-02	6.15E-03	3.19E-02	3.16E-03	1.44E-02	1.97E-02	2.37E-03	8.66E-03	100%
M8-M3-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.32E-02	1.07E-02	2.50E-03	4.09E-03	5.21E-03	1.65E-03	1.78E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.67E-02	5.20E-03	3.75E-02	3.97E-03	1.68E-02	1.88E-02	2.37E-03	8.22E-03	100%
M8-M4-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.38E-02	7.28E-03	1.49E-03	2.89E-03	7.05E-03	2.05E-03	2.50E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.25E-02	6.48E-03	2.49E-02	2.37E-03	1.13E-02	2.47E-02	2.95E-03	1.09E-02	100%
M8-M4-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.36E-02	8.13E-03	1.76E-03	3.18E-03	6.73E-03	2.05E-03	2.34E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.39E-02	5.84E-03	2.83E-02	2.80E-03	1.27E-02	2.40E-02	2.95E-03	1.05E-02	100%
M8-M5-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.36E-02	5.77E-03	1.20E-03	2.29E-03	8.97E-03	2.72E-03	3.13E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.37E-02	6.15E-03	1.99E-02	1.90E-03	8.99E-03	3.15E-02	3.89E-03	1.38E-02	100%
M8-M5-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.35E-02	6.34E-03	1.36E-03	2.49E-03	8.69E-03	2.72E-03	2.99E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.45E-02	5.73E-03	2.21E-02	2.16E-03	9.96E-03	3.10E-02	3.89E-03	1.35E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M8-M6-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.30E-02	4.52E-03	9.96E-04	1.76E-03	1.20E-02	4.00E-03	3.98E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.86E-02	5.15E-03	1.58E-02	1.58E-03	7.10E-03	4.25E-02	5.74E-03	1.84E-02	100%
M8-M6-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.29E-02	4.91E-03	1.11E-03	1.90E-03	1.17E-02	4.00E-03	3.86E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.90E-02	4.88E-03	1.73E-02	1.76E-03	7.76E-03	4.20E-02	5.74E-03	1.81E-02	100%
M8-M7-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.20E-02	3.50E-03	8.54E-04	1.32E-03	1.96E-02	7.60E-03	5.98E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.52E-02	3.65E-03	1.19E-02	1.36E-03	5.29E-03	6.60E-02	1.09E-02	2.75E-02	100%
M8-M7-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.19E-02	3.78E-03	9.36E-04	1.42E-03	1.93E-02	7.60E-03	5.87E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.54E-02	3.50E-03	1.29E-02	1.49E-03	5.73E-03	6.55E-02	1.09E-02	2.73E-02	100%
M8-M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.39E-01	9.82E-02	4.01E-02	1.66E-02	1.17E-02	2.50E-03	1.09E-03	7.07E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.29E-01	1.40E-03	1.17E-01	2.64E-02	4.55E-02	8.39E-03	1.68E-03	3.35E-03	100%
M8-M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.41E-01	9.71E-02	4.39E-02	1.86E-02	1.26E-02	2.47E-03	1.09E-03	6.93E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.35E-01	1.31E-03	1.24E-01	2.95E-02	4.72E-02	8.16E-03	1.68E-03	3.24E-03	100%
M8-M2-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.13E-02	1.71E-02	4.97E-03	6.07E-03	3.79E-03	1.38E-03	1.20E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.94E-02	3.37E-03	5.89E-02	7.90E-03	2.55E-02	1.38E-02	1.98E-03	5.89E-03	100%
M8-M2-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.12E-02	1.75E-02	5.13E-03	6.17E-03	3.76E-03	1.38E-03	1.19E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.02E-02	3.28E-03	6.00E-02	8.15E-03	2.59E-02	1.37E-02	1.98E-03	5.84E-03	100%
M8-M3-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.30E-02	1.13E-02	2.72E-03	4.27E-03	5.09E-03	1.65E-03	1.72E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.80E-02	4.88E-03	3.97E-02	4.31E-03	1.77E-02	1.85E-02	2.37E-03	8.06E-03	100%
M8-M3-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.30E-02	1.14E-02	2.76E-03	4.31E-03	5.06E-03	1.65E-03	1.71E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.82E-02	4.82E-03	4.02E-02	4.39E-03	1.79E-02	1.84E-02	2.37E-03	8.03E-03	100%
M8-M4-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.35E-02	8.44E-03	1.87E-03	3.29E-03	6.63E-03	2.05E-03	2.29E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.45E-02	5.62E-03	2.95E-02	2.97E-03	1.33E-02	2.37E-02	2.95E-03	1.04E-02	100%
M8-M4-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.35E-02	8.51E-03	1.89E-03	3.31E-03	6.61E-03	2.05E-03	2.28E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.46E-02	5.58E-03	2.98E-02	3.00E-03	1.34E-02	2.37E-02	2.95E-03	1.04E-02	100%
M8-M5-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.35E-02	6.54E-03	1.42E-03	2.56E-03	8.60E-03	2.72E-03	2.94E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.48E-02	5.58E-03	2.29E-02	2.26E-03	1.03E-02	3.08E-02	3.89E-03	1.34E-02	100%
M8-M5-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.35E-02	6.58E-03	1.44E-03	2.57E-03	8.59E-03	2.72E-03	2.94E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.49E-02	5.55E-03	2.30E-02	2.28E-03	1.04E-02	3.07E-02	3.89E-03	1.34E-02	100%
M8-M6-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.29E-02	5.05E-03	1.15E-03	1.95E-03	1.16E-02	4.00E-03	3.82E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.92E-02	4.79E-03	1.78E-02	1.83E-03	7.99E-03	4.18E-02	5.74E-03	1.80E-02	100%
M8-M6-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.29E-02	5.08E-03	1.16E-03	1.96E-03	1.16E-02	4.00E-03	3.82E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.92E-02	4.77E-03	1.79E-02	1.84E-03	8.03E-03	4.18E-02	5.74E-03	1.80E-02	100%
M8-M7-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.19E-02	3.87E-03	9.65E-04	1.45E-03	1.93E-02	7.60E-03	5.84E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.55E-02	3.45E-03	1.33E-02	1.53E-03	5.88E-03	6.53E-02	1.09E-02	2.72E-02	100%
M8-M7-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.19E-02	3.89E-03	9.71E-04	1.46E-03	1.93E-02	7.60E-03	5.83E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.55E-02	3.44E-03	1.34E-02	1.54E-03	5.91E-03	6.53E-02	1.09E-02	2.72E-02	100%
M8-M2-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.48E-02	3.84E-02	1.51E-02	1.17E-02	3.20E-03	1.38E-03	9.10E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.56E-03	1.04E-01	2.40E-02	4.01E-02	1.06E-02	1.98E-03	4.29E-03	100%
M8-M3-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.18E-02	1.51E-02	4.28E-03	5.40E-03	4.52E-03	1.65E-03	1.43E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.64E-02	3.39E-03	5.30E-02	6.80E-03	2.31E-02	1.66E-02	2.37E-03	7.14E-03	100%
M8-M4-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.30E-02	1.02E-02	2.50E-03	3.86E-03	6.13E-03	2.05E-03	2.04E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.80E-02	4.55E-03	3.64E-02	3.97E-03	1.62E-02	2.25E-02	2.95E-03	9.77E-03	100%
M8-M5-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.32E-02	7.59E-03	1.76E-03	2.91E-03	8.18E-03	2.72E-03	2.73E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.65E-02	4.86E-03	2.70E-02	2.80E-03	1.21E-02	2.98E-02	3.89E-03	1.29E-02	100%
M8-M6-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.27E-02	5.74E-03	1.36E-03	2.19E-03	1.13E-02	4.00E-03	3.64E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.01E-02	4.34E-03	2.04E-02	2.16E-03	9.13E-03	4.09E-02	5.74E-03	1.76E-02	100%
M8-M7-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.18E-02	4.35E-03	1.11E-03	1.62E-03	1.90E-02	7.60E-03	5.68E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.59E-02	3.20E-03	1.50E-02	1.76E-03	6.61E-03	6.45E-02	1.09E-02	2.68E-02	100%
M8-M3-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.47E-02	3.80E-02	1.51E-02	1.15E-02	3.75E-03	1.65E-03	1.05E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.35E-03	1.03E-01	2.40E-02	3.94E-02	1.24E-02	2.37E-03	4.99E-03	100%
M8-M4-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.15E-02	1.46E-02	4.28E-03	5.16E-03	5.38E-03	2.05E-03	1.66E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.72E-02	2.87E-03	5.16E-02	6.80E-03	2.24E-02	1.99E-02	2.95E-03	8.49E-03	100%
M8-M5-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.25E-02	9.65E-03	2.50E-03	3.58E-03	7.53E-03	2.72E-03	2.41E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.02E-02	3.68E-03	3.48E-02	3.97E-03	1.54E-02	2.80E-02	3.89E-03	1.20E-02	100%
M8-M6-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.23E-02	6.95E-03	1.76E-03	2.59E-03	1.07E-02	4.00E-03	3.36E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.16E-02	3.58E-03	2.50E-02	2.80E-03	1.11E-02	3.94E-02	5.74E-03	1.69E-02	100%
M8-M7-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.16E-02	5.14E-03	1.36E-03	1.89E-03	1.85E-02	7.60E-03	5.44E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.64E-02	2.76E-03	1.78E-02	2.16E-03	7.80E-03	6.31E-02	1.09E-02	2.61E-02	100%
M8-M4-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.46E-02	3.75E-02	1.51E-02	1.12E-02	4.53E-03	2.05E-03	1.24E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.08E-03	1.01E-01	2.40E-02	3.86E-02	1.49E-02	2.95E-03	6.00E-03	100%
M8-M5-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.12E-02	1.40E-02	4.28E-03	4.86E-03	6.70E-03	2.72E-03	1.99E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.91E-02	2.21E-03	4.97E-02	6.80E-03	2.14E-02	2.49E-02	3.89E-03	1.05E-02	100%
M8-M6-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.19E-02	8.95E-03	2.50E-03	3.23E-03	1.00E-02	4.00E-03	3.01E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.50E-02	2.60E-03	3.25E-02	3.97E-03	1.43E-02	3.73E-02	5.74E-03	1.58E-02	100%
M8-M7-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.13E-02	6.32E-03	1.76E-03	2.28E-03	1.79E-02	7.60E-03	5.13E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.76E-02	2.21E-03	2.19E-02	2.80E-03	9.57E-03	6.13E-02	1.09E-02	2.52E-02	100%
M8-M5-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.44E-02	3.68E-02	1.51E-02	1.09E-02	5.76E-03	2.72E-03	1.52E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.19E-01	7.49E-04	9.89E-02	2.40E-02	3.75E-02	1.89E-02	3.89E-03	7.53E-03	100%
M8-M6-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.06E-02	1.32E-02	4.28E-03	4.48E-03	9.08E-03	4.00E-03	2.54E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.32E-02	1.44E-03	4.68E-02	6.80E-03	2.00E-02	3.36E-02	5.74E-03	1.39E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M8-M7-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.09E-02	8.30E-03	2.50E-03	2.90E-03	1.70E-02	7.60E-03	4.72E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	9.03E-02	1.50E-03	2.88E-02	3.97E-03	1.24E-02	5.86E-02	1.09E-02	2.38E-02	100%
M8-M6-M5	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.39E-02	3.59E-02	1.51E-02	1.04E-02	8.02E-03	4.00E-03	2.01E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.22E-01	3.95E-04	9.51E-02	2.40E-02	3.56E-02	2.60E-02	5.74E-03	1.01E-02	100%
M8-M7-M5	0.1	0.1	0.1025	0.0975	1.40E-01	2.08E-01	8.97E-02	1.26E-02	4.28E-03	4.14E-03	1.59E-02	7.60E-03	4.14E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	9.72E-02	7.17E-04	4.21E-02	6.80E-03	1.76E-02	5.37E-02	1.09E-02	2.14E-02	100%
M8-M7-M6	0.1	0.1	0.1025	0.0975	1.40E-01	2.16E-01	8.30E-02	3.52E-02	1.51E-02	1.01E-02	1.45E-02	7.60E-03	3.47E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.34E-01	1.46E-04	8.97E-02	2.40E-02	3.29E-02	4.36E-02	1.09E-02	1.64E-02	100%
M9-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.93E-01	8.16E-02	2.80E-02	6.37E-03	1.08E-02	1.89E-03	3.90E-04	7.51E-04	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.15E-02	1.28E-03	8.32E-02	6.37E-03	3.84E-02	5.70E-03	3.90E-04	2.65E-03	100%
M9-M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.32E-01	1.06E-01	1.82E-02	5.14E-03	6.54E-03	2.38E-03	7.84E-04	7.96E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	8.36E-02	4.29E-03	6.62E-02	8.17E-03	2.90E-02	8.87E-03	1.21E-03	3.83E-03	100%
M9-M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.35E-01	1.02E-01	2.96E-02	1.09E-02	9.34E-03	1.97E-03	7.84E-04	5.91E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.09E-01	2.21E-03	9.72E-02	1.73E-02	4.00E-02	6.98E-03	1.21E-03	2.88E-03	100%
M9-M2-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.30E-02	1.33E-02	2.98E-03	5.16E-03	3.25E-03	9.51E-04	1.15E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.90E-02	6.04E-03	4.55E-02	4.73E-03	2.04E-02	1.14E-02	1.36E-03	5.04E-03	100%
M9-M2-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.20E-02	1.64E-02	4.30E-03	6.04E-03	2.88E-03	9.51E-04	9.64E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	7.56E-02	4.47E-03	5.63E-02	6.82E-03	2.48E-02	1.04E-02	1.36E-03	4.50E-03	100%
M9-M3-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.39E-02	1.02E-02	1.99E-03	4.10E-03	4.05E-03	1.07E-03	1.49E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.28E-02	7.41E-03	3.41E-02	3.16E-03	1.55E-02	1.39E-02	1.54E-03	6.17E-03	100%
M9-M3-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.34E-02	1.16E-02	2.50E-03	4.56E-03	3.74E-03	1.07E-03	1.33E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.55E-02	6.29E-03	3.98E-02	3.97E-03	1.79E-02	1.31E-02	1.54E-03	5.80E-03	100%
M9-M4-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.42E-02	8.35E-03	1.49E-03	3.43E-03	4.95E-03	1.23E-03	1.86E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.03E-02	8.31E-03	2.73E-02	2.37E-03	1.24E-02	1.65E-02	1.76E-03	7.35E-03	100%
M9-M4-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.40E-02	9.22E-03	1.76E-03	3.73E-03	4.68E-03	1.23E-03	1.72E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.16E-02	7.51E-03	3.07E-02	2.80E-03	1.39E-02	1.59E-02	1.76E-03	7.06E-03	100%
M9-M5-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.44E-02	7.01E-03	1.20E-03	2.91E-03	5.98E-03	1.44E-03	2.27E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.96E-02	8.80E-03	2.25E-02	1.90E-03	1.03E-02	1.95E-02	2.06E-03	8.73E-03	100%
M9-M5-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.42E-02	7.62E-03	1.36E-03	3.13E-03	5.73E-03	1.44E-03	2.15E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.02E-02	8.22E-03	2.48E-02	2.16E-03	1.13E-02	1.90E-02	2.06E-03	8.47E-03	100%
M9-M6-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.43E-02	5.99E-03	9.96E-04	2.49E-03	7.26E-03	1.73E-03	2.76E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.05E-02	9.06E-03	1.90E-02	1.58E-03	8.70E-03	2.34E-02	2.48E-03	1.05E-02	100%
M9-M6-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.42E-02	6.44E-03	1.11E-03	2.66E-03	7.04E-03	1.73E-03	2.65E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.08E-02	8.63E-03	2.06E-02	1.76E-03	9.42E-03	2.29E-02	2.48E-03	1.02E-02	100%
M9-M7-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.52E-02	5.36E-03	8.54E-04	2.25E-03	9.52E-03	2.18E-03	3.67E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.51E-02	9.81E-03	1.63E-02	1.36E-03	7.49E-03	2.91E-02	3.12E-03	1.30E-02	100%
M9-M7-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.51E-02	5.73E-03	9.36E-04	2.40E-03	9.31E-03	2.18E-03	3.57E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.51E-02	9.47E-03	1.76E-02	1.49E-03	8.03E-03	2.86E-02	3.12E-03	1.28E-02	100%
M9-M8-FOX	0.4	0.4	0.45	0.35	2.18E-02	3.18E-01	1.29E-01	7.69E-03	3.23E-03	2.23E-03	5.29E-02	3.17E-02	1.06E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.62E-01	1.97E-02	1.71E-02	3.23E-03	6.94E-03	1.05E-01	3.17E-02	3.67E-02	100%
M9-M8-OD	0.4	0.4	0.45	0.35	2.18E-02	3.18E-01	1.29E-01	8.19E-03	3.47E-03	2.36E-03	5.27E-02	3.17E-02	1.05E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.62E-01	1.94E-02	1.83E-02	3.47E-03	7.41E-03	1.05E-01	3.17E-02	3.65E-02	100%
M9-M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.40E-01	9.85E-02	4.07E-02	1.66E-02	1.20E-02	1.85E-03	7.84E-04	5.32E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.29E-01	1.63E-03	1.19E-01	2.64E-02	4.64E-02	6.19E-03	1.21E-03	2.49E-03	100%
M9-M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.41E-01	9.74E-02	4.44E-02	1.86E-02	1.29E-02	1.83E-03	7.84E-04	5.21E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.35E-01	1.52E-03	1.26E-01	2.95E-02	4.82E-02	6.02E-03	1.21E-03	2.40E-03	100%
M9-M2-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.14E-02	1.79E-02	4.97E-03	6.46E-03	2.76E-03	9.51E-04	9.06E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	7.90E-02	3.97E-03	6.11E-02	7.90E-03	2.66E-02	9.94E-03	1.36E-03	4.29E-03	100%
M9-M2-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.13E-02	1.82E-02	5.13E-03	6.55E-03	2.74E-03	9.51E-04	8.94E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	7.97E-02	3.87E-03	6.22E-02	8.15E-03	2.70E-02	9.85E-03	1.36E-03	4.24E-03	100%
M9-M3-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.32E-02	1.22E-02	2.72E-03	4.73E-03	3.64E-03	1.07E-03	1.28E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.67E-02	5.92E-03	4.20E-02	4.31E-03	1.88E-02	1.29E-02	1.54E-03	5.67E-03	100%
M9-M3-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.32E-02	1.23E-02	2.76E-03	4.77E-03	3.62E-03	1.07E-03	1.27E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.70E-02	5.85E-03	4.25E-02	4.39E-03	1.90E-02	1.28E-02	1.54E-03	5.65E-03	100%
M9-M4-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.39E-02	9.54E-03	1.87E-03	3.84E-03	4.59E-03	1.23E-03	1.68E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.22E-02	7.24E-03	3.20E-02	2.97E-03	1.45E-02	1.57E-02	1.76E-03	6.97E-03	100%
M9-M4-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.39E-02	9.61E-03	1.89E-03	3.86E-03	4.57E-03	1.23E-03	1.67E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.23E-02	7.19E-03	3.23E-02	3.00E-03	1.46E-02	1.57E-02	1.76E-03	6.95E-03	100%
M9-M5-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.42E-02	7.84E-03	1.42E-03	3.21E-03	5.65E-03	1.44E-03	2.11E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.05E-02	8.02E-03	2.56E-02	2.26E-03	1.17E-02	1.88E-02	2.06E-03	8.39E-03	100%
M9-M5-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.42E-02	7.88E-03	1.44E-03	3.22E-03	5.64E-03	1.44E-03	2.10E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.06E-02	7.99E-03	2.58E-02	2.28E-03	1.18E-02	1.88E-02	2.06E-03	8.37E-03	100%
M9-M6-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.42E-02	6.59E-03	1.15E-03	2.72E-03	6.97E-03	1.73E-03	2.62E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.09E-02	8.49E-03	2.12E-02	1.83E-03	9.68E-03	2.28E-02	2.48E-03	1.01E-02	100%
M9-M6-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.41E-02	6.63E-03	1.16E-03	2.73E-03	6.95E-03	1.73E-03	2.61E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.10E-02	8.46E-03	2.13E-02	1.84E-03	9.73E-03	2.27E-02	2.48E-03	1.01E-02	100%
M9-M7-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.51E-02	5.86E-03	9.65E-04	2.45E-03	9.25E-03	2.18E-03	3.54E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.52E-02	9.37E-03	1.80E-02	1.53E-03	8.23E-03	2.85E-02	3.12E-03	1.27E-02	100%
M9-M7-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.51E-02	5.88E-03	9.71E-04	2.46E-03	9.23E-03	2.18E-03	3.53E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.53E-02	9.36E-03	1.81E-02	1.54E-03	8.27E-03	2.85E-02	3.12E-03	1.27E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M9-M8-PO1(OD)	0.4	0.4	0.45	0.35	2.18E-02	3.18E-01	1.29E-01	8.36E-03	3.56E-03	2.40E-03	5.26E-02	3.17E-02	1.05E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.62E-01	1.94E-02	1.87E-02	3.56E-03	7.57E-03	1.05E-01	3.17E-02	3.65E-02	100%
M9-M8-PO1(FOX)	0.4	0.4	0.45	0.35	2.18E-02	3.18E-01	1.29E-01	8.40E-03	3.57E-03	2.41E-03	5.26E-02	3.17E-02	1.04E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.62E-01	1.93E-02	1.88E-02	3.57E-03	7.60E-03	1.05E-01	3.17E-02	3.65E-02	100%
M9-M2-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.49E-02	3.92E-02	1.51E-02	1.20E-02	2.29E-03	9.51E-04	6.68E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.91E-03	1.06E-01	2.40E-02	4.13E-02	7.53E-03	1.36E-03	3.08E-03	100%
M9-M3-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.20E-02	1.60E-02	4.28E-03	5.86E-03	3.17E-03	1.07E-03	1.05E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.55E-02	4.23E-03	5.55E-02	6.80E-03	2.44E-02	1.15E-02	1.54E-03	4.98E-03	100%
M9-M4-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.34E-02	1.13E-02	2.50E-03	4.42E-03	4.17E-03	1.23E-03	1.47E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.59E-02	6.00E-03	3.91E-02	3.97E-03	1.76E-02	1.48E-02	1.76E-03	6.50E-03	100%
M9-M5-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.39E-02	8.95E-03	1.76E-03	3.59E-03	5.28E-03	1.44E-03	1.92E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.24E-02	7.14E-03	3.01E-02	2.80E-03	1.36E-02	1.81E-02	2.06E-03	8.03E-03	100%
M9-M6-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.40E-02	7.37E-03	1.36E-03	3.00E-03	6.64E-03	1.73E-03	2.45E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.20E-02	7.87E-03	2.41E-02	2.16E-03	1.10E-02	2.21E-02	2.48E-03	9.82E-03	100%
M9-M7-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.50E-02	6.46E-03	1.11E-03	2.68E-03	8.94E-03	2.18E-03	3.38E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.59E-02	8.93E-03	2.01E-02	1.76E-03	9.18E-03	2.79E-02	3.12E-03	1.24E-02	100%
M9-M8-M1	0.4	0.4	0.45	0.35	2.18E-02	3.17E-01	1.28E-01	9.18E-03	3.96E-03	2.61E-03	5.23E-02	3.17E-02	1.03E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.63E-01	1.89E-02	2.06E-02	3.96E-03	8.31E-03	1.04E-01	3.17E-02	3.63E-02	100%
M9-M3-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.49E-02	3.90E-02	1.51E-02	1.19E-02	2.55E-03	1.07E-03	7.39E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.80E-03	1.06E-01	2.40E-02	4.08E-02	8.38E-03	1.54E-03	3.42E-03	100%
M9-M4-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.19E-02	1.58E-02	4.28E-03	5.74E-03	3.56E-03	1.23E-03	1.17E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.56E-02	3.99E-03	5.47E-02	6.80E-03	2.40E-02	1.29E-02	1.76E-03	5.58E-03	100%
M9-M5-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.32E-02	1.11E-02	2.50E-03	4.28E-03	4.73E-03	1.44E-03	1.65E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.65E-02	5.67E-03	3.84E-02	3.97E-03	1.72E-02	1.68E-02	2.06E-03	7.39E-03	100%
M9-M6-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.36E-02	8.69E-03	1.76E-03	3.46E-03	6.15E-03	1.73E-03	2.21E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.40E-02	6.82E-03	2.93E-02	2.80E-03	1.32E-02	2.11E-02	2.48E-03	9.31E-03	100%
M9-M7-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.47E-02	7.43E-03	1.36E-03	3.04E-03	8.48E-03	2.18E-03	3.15E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.70E-02	8.15E-03	2.36E-02	2.16E-03	1.07E-02	2.70E-02	3.12E-03	1.20E-02	100%
M9-M8-M2	0.4	0.4	0.45	0.35	2.18E-02	3.18E-01	1.28E-01	1.05E-02	4.61E-03	2.93E-03	5.18E-02	3.17E-02	1.01E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.63E-01	1.81E-02	2.35E-02	4.61E-03	9.44E-03	1.03E-01	3.17E-02	3.58E-02	100%
M9-M4-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.49E-02	3.87E-02	1.51E-02	1.18E-02	2.88E-03	1.23E-03	8.28E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.70E-03	1.05E-01	2.40E-02	4.04E-02	9.49E-03	1.76E-03	3.86E-03	100%
M9-M5-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.18E-02	1.55E-02	4.28E-03	5.60E-03	4.07E-03	1.44E-03	1.32E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.63E-02	3.78E-03	5.39E-02	6.80E-03	2.36E-02	1.48E-02	2.06E-03	6.38E-03	100%
M9-M6-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.30E-02	1.08E-02	2.50E-03	4.17E-03	5.55E-03	1.73E-03	1.91E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.81E-02	5.44E-03	3.76E-02	3.97E-03	1.68E-02	1.97E-02	2.48E-03	8.62E-03	100%
M9-M7-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.43E-02	8.84E-03	1.76E-03	3.54E-03	7.92E-03	2.18E-03	2.87E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.91E-02	7.16E-03	2.88E-02	2.80E-03	1.30E-02	2.60E-02	3.12E-03	1.14E-02	100%
M9-M8-M3	0.4	0.4	0.45	0.35	2.18E-02	3.18E-01	1.27E-01	1.22E-02	5.51E-03	3.35E-03	5.14E-02	3.17E-02	9.84E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.64E-01	1.71E-02	2.75E-02	5.51E-03	1.10E-02	1.03E-01	3.17E-02	3.55E-02	100%
M9-M5-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.48E-02	3.85E-02	1.51E-02	1.17E-02	3.33E-03	1.44E-03	9.46E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.58E-03	1.04E-01	2.40E-02	3.99E-02	1.09E-02	2.06E-03	4.43E-03	100%
M9-M6-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.16E-02	1.53E-02	4.28E-03	5.50E-03	4.81E-03	1.73E-03	1.54E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.75E-02	3.61E-03	5.29E-02	6.80E-03	2.31E-02	1.74E-02	2.48E-03	7.45E-03	100%
M9-M7-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.38E-02	1.11E-02	2.50E-03	4.30E-03	7.23E-03	2.18E-03	2.52E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.30E-02	5.78E-03	3.71E-02	3.97E-03	1.66E-02	2.43E-02	3.12E-03	1.06E-02	100%
M9-M8-M4	0.4	0.4	0.45	0.35	2.18E-02	3.19E-01	1.27E-01	1.48E-02	6.85E-03	3.96E-03	5.09E-02	3.17E-02	9.59E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.67E-01	1.59E-02	3.33E-02	6.85E-03	1.32E-02	1.02E-01	3.17E-02	3.50E-02	100%
M9-M6-M5	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.45E-02	3.83E-02	1.51E-02	1.16E-02	3.97E-03	1.73E-03	1.12E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.19E-01	1.55E-03	1.03E-01	2.40E-02	3.93E-02	1.29E-02	2.48E-03	5.21E-03	100%
M9-M7-M5	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.21E-02	1.58E-02	4.28E-03	5.75E-03	6.34E-03	2.18E-03	2.08E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.23E-02	3.97E-03	5.27E-02	6.80E-03	2.29E-02	2.17E-02	3.12E-03	9.28E-03	100%
M9-M8-M5	0.4	0.4	0.45	0.35	2.18E-02	3.25E-01	1.28E-01	1.89E-02	9.05E-03	4.91E-03	5.03E-02	3.17E-02	9.31E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.71E-01	1.42E-02	4.23E-02	9.05E-03	1.66E-02	1.01E-01	3.17E-02	3.45E-02	100%
M9-M7-M6	0.1	0.1	0.1025	0.0975	1.40E-01	2.15E-01	8.51E-02	3.92E-02	1.51E-02	1.21E-02	5.27E-03	2.18E-03	1.54E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	1.23E-01	1.79E-03	1.03E-01	2.40E-02	3.97E-02	1.64E-02	3.12E-03	6.64E-03	100%
M9-M8-M6	0.4	0.4	0.45	0.35	2.18E-02	3.27E-01	1.25E-01	2.68E-02	1.33E-02	6.71E-03	4.98E-02	3.17E-02	9.06E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.81E-01	1.17E-02	5.81E-02	1.33E-02	2.24E-02	9.91E-02	3.17E-02	3.37E-02	100%
M9-M8-M7	0.4	0.4	0.45	0.35	2.18E-02	3.37E-01	1.19E-01	4.84E-02	2.53E-02	1.15E-02	4.94E-02	3.17E-02	8.87E-03	100%
	0.4	2	0.45	1.95	2.14E-02	2.06E-01	7.89E-03	9.41E-02	2.53E-02	3.44E-02	9.60E-02	3.17E-02	3.22E-02	100%
M10-PO1-FOX	0.06	0.12	0.059	0.121	1.49E+01	1.95E-01	8.26E-02	2.84E-02	6.37E-03	1.10E-02	1.50E-03	3.04E-04	5.97E-04	100%
	0.06	2.4	0.059	2.401	1.49E+01	9.11E-02	1.33E-03	8.39E-02	6.37E-03	3.88E-02	4.49E-03	3.04E-04	2.09E-03	100%
M10-M1-FOX	0.09	0.09	0.0975	0.0825	1.60E-01	2.32E-01	1.06E-01	1.86E-02	5.14E-03	6.75E-03	1.87E-03	6.00E-04	6.36E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	8.34E-02	4.50E-03	6.75E-02	8.17E-03	2.96E-02	6.95E-03	9.27E-04	3.01E-03	100%
M10-M1-OD	0.09	0.09	0.0975	0.0825	1.60E-01	2.34E-01	1.01E-01	3.00E-02	1.09E-02	9.54E-03	1.53E-03	6.00E-04	4.68E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.09E-01	2.39E-03	9.90E-02	1.73E-02	4.08E-02	5.47E-03	9.27E-04	2.27E-03	100%
M10-M2-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.35E-02	1.39E-02	2.98E-03	5.44E-03	2.54E-03	7.09E-04	9.17E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	6.86E-02	6.41E-03	4.69E-02	4.73E-03	2.11E-02	8.87E-03	1.02E-03	3.93E-03	100%
M10-M2-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.24E-02	1.69E-02	4.30E-03	6.31E-03	2.24E-03	7.09E-04	7.64E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	7.57E-02	4.83E-03	5.81E-02	6.82E-03	2.56E-02	8.02E-03	1.02E-03	3.50E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M10-M3-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.44E-02	1.09E-02	1.99E-03	4.43E-03	3.15E-03	7.74E-04	1.19E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.22E-02	7.97E-03	3.57E-02	3.16E-03	1.63E-02	1.06E-02	1.11E-03	4.74E-03	100%
M10-M3-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.40E-02	1.23E-02	2.50E-03	4.88E-03	2.88E-03	7.74E-04	1.05E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.53E-02	6.86E-03	4.16E-02	3.97E-03	1.88E-02	1.00E-02	1.11E-03	4.45E-03	100%
M10-M4-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.48E-02	9.11E-03	1.49E-03	3.81E-03	3.80E-03	8.52E-04	1.47E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.94E-02	9.11E-03	2.89E-02	2.37E-03	1.33E-02	1.23E-02	1.22E-03	5.53E-03	100%
M10-M4-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.46E-02	9.99E-03	1.76E-03	4.11E-03	3.56E-03	8.52E-04	1.35E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.11E-02	8.33E-03	3.26E-02	2.80E-03	1.49E-02	1.18E-02	1.22E-03	5.30E-03	100%
M10-M5-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.51E-02	7.90E-03	1.20E-03	3.35E-03	4.51E-03	9.47E-04	1.78E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.83E-02	9.92E-03	2.43E-02	1.90E-03	1.12E-02	1.41E-02	1.36E-03	6.38E-03	100%
M10-M5-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.49E-02	8.52E-03	1.36E-03	3.58E-03	4.29E-03	9.47E-04	1.67E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.93E-02	9.36E-03	2.68E-02	2.16E-03	1.23E-02	1.37E-02	1.36E-03	6.19E-03	100%
M10-M6-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.51E-02	7.00E-03	9.96E-04	3.00E-03	5.35E-03	1.07E-03	2.14E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.85E-02	1.07E-02	2.10E-02	1.58E-03	9.70E-03	1.62E-02	1.53E-03	7.36E-03	100%
M10-M6-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.50E-02	7.48E-03	1.11E-03	3.18E-03	5.15E-03	1.07E-03	2.04E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.91E-02	1.02E-02	2.28E-02	1.76E-03	1.05E-02	1.59E-02	1.53E-03	7.18E-03	100%
M10-M7-FOX	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.63E-02	6.61E-03	8.54E-04	2.88E-03	6.76E-03	1.22E-03	2.77E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.20E-02	1.22E-02	1.85E-02	1.36E-03	8.59E-03	1.90E-02	1.75E-03	8.62E-03	100%
M10-M7-OD	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.62E-02	7.01E-03	9.36E-04	3.04E-03	6.56E-03	1.22E-03	2.67E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.24E-02	1.19E-02	1.99E-02	1.49E-03	9.20E-03	1.87E-02	1.75E-03	8.46E-03	100%
M10-M8-FOX	0.4	0.4	0.45	0.35	2.18E-02	3.03E-01	1.38E-01	8.78E-03	3.23E-03	2.78E-03	1.78E-02	8.49E-03	4.66E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.19E-01	3.10E-02	1.88E-02	3.23E-03	7.77E-03	3.78E-02	8.49E-03	1.46E-02	100%
M10-M8-OD	0.4	0.4	0.45	0.35	2.18E-02	3.03E-01	1.38E-01	9.31E-03	3.47E-03	2.92E-03	1.76E-02	8.49E-03	4.57E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.19E-01	3.05E-02	2.00E-02	3.47E-03	8.26E-03	3.75E-02	8.49E-03	1.45E-02	100%
M10-M9-FOX	0.4	0.4	0.45	0.35	2.18E-02	3.29E-01	1.38E-01	6.40E-03	2.45E-03	1.97E-03	4.57E-02	2.55E-02	1.01E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.58E-01	2.44E-02	1.39E-02	2.45E-03	5.73E-03	9.52E-02	2.55E-02	3.48E-02	100%
M10-M9-OD	0.4	0.4	0.45	0.35	2.18E-02	3.29E-01	1.38E-01	6.71E-03	2.59E-03	2.06E-03	4.56E-02	2.55E-02	1.00E-02	100%
	0.4	2	0.45	1.95	2.14E-02	1.58E-01	2.41E-02	1.46E-02	2.59E-03	6.01E-03	9.48E-02	2.55E-02	3.46E-02	100%
M10-M1-PO1(OD)	0.09	0.09	0.0975	0.0825	1.60E-01	2.38E-01	9.79E-02	4.10E-02	1.66E-02	1.22E-02	1.44E-03	6.00E-04	4.19E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.30E-01	1.78E-03	1.22E-01	2.64E-02	4.77E-02	4.85E-03	9.27E-04	1.96E-03	100%
M10-M1-PO1(FOX)	0.09	0.09	0.0975	0.0825	1.60E-01	2.40E-01	9.67E-02	4.48E-02	1.86E-02	1.31E-02	1.42E-03	6.00E-04	4.10E-04	100%
	0.09	2	0.1525	1.938	8.62E-02	1.36E-01	1.66E-03	1.28E-01	2.95E-02	4.94E-02	4.72E-03	9.27E-04	1.89E-03	100%
M10-M2-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.19E-02	1.84E-02	4.97E-03	6.72E-03	2.14E-03	7.09E-04	7.15E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	7.92E-02	4.31E-03	6.29E-02	7.90E-03	2.75E-02	7.69E-03	1.02E-03	3.34E-03	100%
M10-M2-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.18E-02	1.88E-02	5.13E-03	6.82E-03	2.12E-03	7.09E-04	7.05E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	8.00E-02	4.21E-03	6.40E-02	8.15E-03	2.79E-02	7.62E-03	1.02E-03	3.30E-03	100%
M10-M3-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.38E-02	1.28E-02	2.72E-03	5.06E-03	2.79E-03	7.74E-04	1.01E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.66E-02	6.49E-03	4.38E-02	4.31E-03	1.98E-02	9.80E-03	1.11E-03	4.35E-03	100%
M10-M3-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.37E-02	1.30E-02	2.76E-03	5.09E-03	2.78E-03	7.74E-04	1.00E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.69E-02	6.41E-03	4.43E-02	4.39E-03	2.00E-02	9.76E-03	1.11E-03	4.32E-03	100%
M10-M4-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.45E-02	1.03E-02	1.87E-03	4.22E-03	3.48E-03	8.52E-04	1.32E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.17E-02	8.05E-03	3.39E-02	2.97E-03	1.55E-02	1.17E-02	1.22E-03	5.23E-03	100%
M10-M4-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.45E-02	1.04E-02	1.89E-03	4.24E-03	3.47E-03	8.52E-04	1.31E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.18E-02	8.00E-03	3.42E-02	3.00E-03	1.56E-02	1.16E-02	1.22E-03	5.21E-03	100%
M10-M5-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.48E-02	8.73E-03	1.42E-03	3.65E-03	4.22E-03	9.47E-04	1.64E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.96E-02	9.17E-03	2.77E-02	2.26E-03	1.27E-02	1.36E-02	1.36E-03	6.12E-03	100%
M10-M5-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.48E-02	8.78E-03	1.44E-03	3.67E-03	4.21E-03	9.47E-04	1.63E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.97E-02	9.13E-03	2.79E-02	2.28E-03	1.28E-02	1.36E-02	1.36E-03	6.11E-03	100%
M10-M6-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.49E-02	7.64E-03	1.15E-03	3.25E-03	5.08E-03	1.07E-03	2.01E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.94E-02	1.01E-02	2.34E-02	1.83E-03	1.08E-02	1.58E-02	1.53E-03	7.12E-03	100%
M10-M6-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.49E-02	7.67E-03	1.16E-03	3.26E-03	5.07E-03	1.07E-03	2.00E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	5.94E-02	1.01E-02	2.35E-02	1.84E-03	1.08E-02	1.58E-02	1.53E-03	7.11E-03	100%
M10-M7-PO1(OD)	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.62E-02	7.15E-03	9.65E-04	3.09E-03	6.50E-03	1.22E-03	2.64E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.25E-02	1.18E-02	2.04E-02	1.53E-03	9.42E-03	1.86E-02	1.75E-03	8.41E-03	100%
M10-M7-PO1(FOX)	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.62E-02	7.18E-03	9.71E-04	3.10E-03	6.49E-03	1.22E-03	2.63E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.25E-02	1.18E-02	2.05E-02	1.54E-03	9.46E-03	1.85E-02	1.75E-03	8.40E-03	100%
M10-M8-PO1(OD)	0.4	0.4	0.45	0.35	2.18E-02	3.03E-01	1.38E-01	9.49E-03	3.56E-03	2.97E-03	1.76E-02	8.49E-03	4.54E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.19E-01	3.04E-02	2.04E-02	3.56E-03	8.43E-03	3.75E-02	8.49E-03	1.45E-02	100%
M10-M8-PO1(FOX)	0.4	0.4	0.45	0.35	2.18E-02	3.03E-01	1.38E-01	9.53E-03	3.57E-03	2.98E-03	1.76E-02	8.49E-03	4.54E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.19E-01	3.04E-02	2.05E-02	3.57E-03	8.46E-03	3.74E-02	8.49E-03	1.45E-02	100%
M10-M9-PO1(OD)	0.4	0.4	0.45	0.35	2.18E-02	3.29E-01	1.38E-01	6.81E-03	2.63E-03	2.09E-03	4.55E-02	2.55E-02	9.99E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.58E-01	2.41E-02	1.48E-02	2.63E-03	6.10E-03	9.47E-02	2.55E-02	3.46E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M10-M9-PO1(FOX)	0.4	0.4	0.45	0.35	2.18E-02	3.29E-01	1.38E-01	6.83E-03	2.64E-03	2.09E-03	4.55E-02	2.55E-02	9.98E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.58E-01	2.41E-02	1.49E-02	2.64E-03	6.12E-03	9.47E-02	2.55E-02	3.46E-02	100%
M10-M2-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.54E-02	3.97E-02	1.51E-02	1.23E-02	1.74E-03	7.09E-04	5.17E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	2.11E-03	1.08E-01	2.40E-02	4.22E-02	5.77E-03	1.02E-03	2.38E-03	100%
M10-M3-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.25E-02	1.66E-02	4.28E-03	6.16E-03	2.40E-03	7.74E-04	8.14E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	7.56E-02	4.69E-03	5.75E-02	6.80E-03	2.54E-02	8.68E-03	1.11E-03	3.79E-03	100%
M10-M4-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.39E-02	1.21E-02	2.50E-03	4.79E-03	3.12E-03	8.52E-04	1.14E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.56E-02	6.73E-03	4.12E-02	3.97E-03	1.86E-02	1.09E-02	1.22E-03	4.84E-03	100%
M10-M5-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.45E-02	9.83E-03	1.76E-03	4.03E-03	3.89E-03	9.47E-04	1.47E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.16E-02	8.21E-03	3.22E-02	2.80E-03	1.47E-02	1.30E-02	1.36E-03	5.82E-03	100%
M10-M6-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.47E-02	8.42E-03	1.36E-03	3.53E-03	4.78E-03	1.07E-03	1.86E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.05E-02	9.40E-03	2.65E-02	2.16E-03	1.22E-02	1.53E-02	1.53E-03	6.86E-03	100%
M10-M7-M1	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.60E-02	7.78E-03	1.11E-03	3.34E-03	6.20E-03	1.22E-03	2.49E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.33E-02	1.13E-02	2.27E-02	1.76E-03	1.04E-02	1.81E-02	1.75E-03	8.18E-03	100%
M10-M8-M1	0.4	0.4	0.45	0.35	2.18E-02	3.05E-01	1.38E-01	1.03E-02	3.96E-03	3.19E-03	1.73E-02	8.49E-03	4.42E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.19E-01	2.99E-02	2.24E-02	3.96E-03	9.23E-03	3.72E-02	8.49E-03	1.43E-02	100%
M10-M9-M1	0.4	0.4	0.45	0.35	2.18E-02	3.30E-01	1.39E-01	7.29E-03	2.85E-03	2.22E-03	4.53E-02	2.55E-02	9.87E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.58E-01	2.38E-02	1.59E-02	2.85E-03	6.53E-03	9.43E-02	2.55E-02	3.44E-02	100%
M10-M3-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.12E-01	8.54E-02	3.95E-02	1.51E-02	1.22E-02	1.89E-03	7.74E-04	5.59E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.19E-01	2.07E-03	1.08E-01	2.40E-02	4.21E-02	6.27E-03	1.11E-03	2.58E-03	100%
M10-M4-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.04E-01	9.24E-02	1.65E-02	4.28E-03	6.09E-03	2.62E-03	8.52E-04	8.82E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	7.58E-02	4.60E-03	5.72E-02	6.80E-03	2.52E-02	9.47E-03	1.22E-03	4.13E-03	100%
M10-M5-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.39E-02	1.20E-02	2.50E-03	4.73E-03	3.43E-03	9.47E-04	1.24E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.61E-02	6.64E-03	4.08E-02	3.97E-03	1.84E-02	1.20E-02	1.36E-03	5.32E-03	100%
M10-M6-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.44E-02	9.77E-03	1.76E-03	4.01E-03	4.35E-03	1.07E-03	1.64E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.29E-02	8.27E-03	3.19E-02	2.80E-03	1.46E-02	1.44E-02	1.53E-03	6.46E-03	100%
M10-M7-M2	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.57E-02	8.81E-03	1.36E-03	3.72E-03	5.78E-03	1.22E-03	2.28E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.46E-02	1.04E-02	2.64E-02	2.16E-03	1.21E-02	1.74E-02	1.75E-03	7.82E-03	100%
M10-M8-M2	0.4	0.4	0.45	0.35	2.18E-02	3.04E-01	1.38E-01	1.17E-02	4.61E-03	3.53E-03	1.70E-02	8.49E-03	4.25E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.20E-01	2.90E-02	2.55E-02	4.61E-03	1.05E-02	3.68E-02	8.49E-03	1.41E-02	100%
M10-M9-M2	0.4	0.4	0.45	0.35	2.18E-02	3.30E-01	1.39E-01	7.97E-03	3.17E-03	2.40E-03	4.49E-02	2.55E-02	9.68E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.57E-01	2.33E-02	1.74E-02	3.17E-03	7.14E-03	9.34E-02	2.55E-02	3.39E-02	100%
M10-M4-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.49E-02	3.94E-02	1.51E-02	1.22E-02	2.07E-03	8.52E-04	6.10E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.99E-03	1.07E-01	2.40E-02	4.16E-02	6.81E-03	1.22E-03	2.80E-03	100%
M10-M5-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.19E-02	1.64E-02	4.28E-03	6.05E-03	2.89E-03	9.47E-04	9.70E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	7.58E-02	4.46E-03	5.65E-02	6.80E-03	2.48E-02	1.04E-02	1.36E-03	4.51E-03	100%
M10-M6-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.02E-01	9.33E-02	1.19E-02	2.50E-03	4.72E-03	3.85E-03	1.07E-03	1.39E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.69E-02	6.63E-03	4.03E-02	3.97E-03	1.82E-02	1.33E-02	1.53E-03	5.88E-03	100%
M10-M7-M3	0.1	0.1	0.1025	0.0975	1.40E-01	2.05E-01	9.49E-02	1.03E-02	1.76E-03	4.26E-03	5.31E-03	1.22E-03	2.04E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	6.66E-02	9.16E-03	3.18E-02	2.80E-03	1.45E-02	1.65E-02	1.75E-03	7.37E-03	100%
M10-M8-M3	0.4	0.4	0.45	0.35	2.18E-02	3.04E-01	1.37E-01	1.35E-02	5.51E-03	3.98E-03	1.66E-02	8.49E-03	4.07E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.22E-01	2.79E-02	2.98E-02	5.51E-03	1.21E-02	3.64E-02	8.49E-03	1.39E-02	100%
M10-M9-M3	0.4	0.4	0.45	0.35	2.18E-02	3.29E-01	1.38E-01	8.82E-03	3.57E-03	2.62E-03	4.45E-02	2.55E-02	9.49E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.58E-01	2.28E-02	1.94E-02	3.57E-03	7.90E-03	9.28E-02	2.55E-02	3.36E-02	100%
M10-M5-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.49E-02	3.93E-02	1.51E-02	1.21E-02	2.29E-03	9.47E-04	6.73E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.18E-01	1.95E-03	1.06E-01	2.40E-02	4.12E-02	7.50E-03	1.36E-03	3.07E-03	100%
M10-M6-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.03E-01	9.18E-02	1.64E-02	4.28E-03	6.06E-03	3.25E-03	1.07E-03	1.09E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.66E-02	4.53E-03	5.60E-02	6.80E-03	2.46E-02	1.16E-02	1.53E-03	5.01E-03	100%
M10-M7-M4	0.1	0.1	0.1025	0.0975	1.40E-01	2.06E-01	9.42E-02	1.26E-02	2.50E-03	5.05E-03	4.73E-03	1.22E-03	1.75E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	7.08E-02	7.53E-03	4.05E-02	3.97E-03	1.82E-02	1.53E-02	1.75E-03	6.77E-03	100%
M10-M8-M4	0.4	0.4	0.45	0.35	2.18E-02	3.04E-01	1.36E-01	1.61E-02	6.85E-03	4.63E-03	1.63E-02	8.49E-03	3.89E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.25E-01	2.65E-02	3.60E-02	6.85E-03	1.46E-02	3.60E-02	8.49E-03	1.37E-02	100%
M10-M9-M4	0.4	0.4	0.45	0.35	2.18E-02	3.29E-01	1.38E-01	9.89E-03	4.09E-03	2.90E-03	4.41E-02	2.55E-02	9.27E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.59E-01	2.23E-02	2.18E-02	4.09E-03	8.87E-03	9.22E-02	2.55E-02	3.33E-02	100%
M10-M6-M5	0.1	0.1	0.1025	0.0975	1.40E-01	2.11E-01	8.47E-02	3.94E-02	1.51E-02	1.22E-02	2.59E-03	1.07E-03	7.62E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.19E-01	2.06E-03	1.06E-01	2.40E-02	4.11E-02	8.40E-03	1.53E-03	3.44E-03	100%
M10-M7-M5	0.1	0.1	0.1025	0.0975	1.40E-01	2.07E-01	9.26E-02	1.73E-02	4.28E-03	6.52E-03	4.02E-03	1.22E-03	1.40E-03	100%
	0.1	2	0.1535	1.946	7.74E-02	8.07E-02	5.35E-03	5.66E-02	6.80E-03	2.49E-02	1.34E-02	1.75E-03	5.83E-03	100%
M10-M8-M5	0.4	0.4	0.45	0.35	2.18E-02	3.07E-01	1.35E-01	2.03E-02	9.05E-03	5.63E-03	1.59E-02	8.49E-03	3.69E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.30E-01	2.43E-02	4.54E-02	9.05E-03	1.82E-02	3.54E-02	8.49E-03	1.35E-02	100%
M10-M9-M5	0.4	0.4	0.45	0.35	2.18E-02	3.30E-01	1.38E-01	1.13E-02	4.79E-03	3.24E-03	4.36E-02	2.55E-02	9.01E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.59E-01	2.13E-02	2.50E-02	4.79E-03	1.01E-02	9.13E-02	2.55E-02	3.29E-02	100%
M10-M7-M6	0.1	0.1	0.1025	0.0975	1.40E-01	2.15E-01	8.54E-02	4.08E-02	1.51E-02	1.29E-02	3.19E-03	1.22E-03	9.83E-04	100%
	0.1	2	0.1535	1.946	7.74E-02	1.23E-01	2.56E-03	1.08E-01	2.40E-02	4.19E-02	9.88E-03	1.75E-03	4.06E-03	100%
M10-M8-M6	0.4	0.4	0.45	0.35	2.18E-02	3.09E-01	1.33E-01	2.84E-02	1.33E-02	7.52E-03	1.55E-02	8.49E-03	3.50E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.40E-01	2.13E-02	6.22E-02	1.33E-02	2.44E-02	3.47E-02	8.49E-03	1.31E-02	100%
M10-M9-M6	0.4	0.4	0.45	0.35	2.18E-02	3.31E-01	1.37E-01	1.32E-02	5.77E-03	3.70E-03	4.30E-02	2.55E-02	8.72E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.60E-01	2.02E-02	2.93E-02	5.77E-03	1.18E-02	9.04E-02	2.55E-02	3.24E-02	100%
M10-M8-M7	0.4	0.4	0.45	0.35	2.18E-02	3.23E-01	1.29E-01	5.04E-02	2.53E-02	1.25E-02	1.51E-02	8.49E-03	3.33E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.4	2	0.45	1.95	2.14E-02	1.67E-01	1.66E-02	1.00E-01	2.53E-02	3.73E-02	3.35E-02	8.49E-03	1.25E-02	100%
M10-M9-M7	0.4	0.4	0.45	0.35	2.18E-02	3.35E-01	1.38E-01	1.59E-02	7.26E-03	4.34E-03	4.23E-02	2.55E-02	8.40E-03	100%
	0.4	2	0.45	1.95	2.14E-02	1.63E-01	1.88E-02	3.57E-02	7.26E-03	1.42E-02	8.95E-02	2.55E-02	3.20E-02	100%
M10-M9-M8	0.4	0.4	0.45	0.35	2.18E-02	3.48E-01	1.29E-01	4.85E-02	2.53E-02	1.16E-02	4.07E-02	2.55E-02	7.60E-03	100%
	0.4	2	0.45	1.95	2.14E-02	2.01E-01	1.02E-02	9.57E-02	2.53E-02	3.52E-02	8.48E-02	2.55E-02	2.96E-02	100%

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12.14.3.2 M1MxMz process in CLN55GP 1.0V/2.5V, no My/Mr, x=2~7, z=8~9

12.14.3.2.1 Structure A 25 ℃

Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.78E-01	7.51E-02	2.80E-02	4.21E-03	1.19E-02	100%
	0.054	2.16	0.039	2.175	1.50E+01	8.36E-02	1.57E-03	8.05E-02	4.21E-03	3.82E-02	100%
M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.93E-02	4.54E-03	7.40E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.04E-02	7.20E-03	6.60E-02	7.93E-03	2.91E-02	100%
M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.93E-02	9.62E-03	9.85E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.04E-01	3.94E-03	9.64E-02	1.68E-02	3.98E-02	100%
M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.92E-02	3.92E-02	1.47E-02	1.23E-02	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.24E-01	2.91E-03	1.18E-01	2.56E-02	4.62E-02	100%
M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.82E-02	4.26E-02	1.64E-02	1.31E-02	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.30E-01	2.72E-03	1.25E-01	2.87E-02	4.80E-02	100%
M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.56E-02	2.70E-03	6.43E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.72E-02	9.54E-03	4.81E-02	4.51E-03	2.18E-02	100%
M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	1.83E-02	3.95E-03	7.19E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.37E-02	7.40E-03	5.89E-02	6.58E-03	2.62E-02	100%
M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	1.97E-02	4.60E-03	7.56E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.70E-02	6.65E-03	6.37E-02	7.66E-03	2.80E-02	100%
M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	2.01E-02	4.75E-03	7.65E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.78E-02	6.49E-03	6.48E-02	7.92E-03	2.84E-02	100%
M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.81E-02	1.33E-02	1.24E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.12E-01	3.45E-03	1.05E-01	2.22E-02	4.15E-02	100%
M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.32E-02	1.32E-02	1.82E-03	5.67E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.16E-02	1.15E-02	3.86E-02	3.04E-03	1.78E-02	100%
M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.27E-02	1.44E-02	2.31E-03	6.04E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.43E-02	1.01E-02	4.41E-02	3.85E-03	2.01E-02	100%
M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	1.49E-02	2.52E-03	6.19E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.55E-02	9.61E-03	4.63E-02	4.20E-03	2.10E-02	100%
M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	1.50E-02	2.57E-03	6.22E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.58E-02	9.51E-03	4.68E-02	4.28E-03	2.12E-02	100%
M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	1.82E-02	3.93E-03	7.11E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.34E-02	7.27E-03	5.88E-02	6.56E-03	2.61E-02	100%
M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.81E-02	1.33E-02	1.24E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.12E-01	3.44E-03	1.05E-01	2.22E-02	4.16E-02	100%
M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.37E-02	1.19E-02	1.37E-03	5.28E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.91E-02	1.30E-02	3.32E-02	2.29E-03	1.55E-02	100%
M4-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.34E-02	1.27E-02	1.64E-03	5.51E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.05E-02	1.20E-02	3.65E-02	2.73E-03	1.69E-02	100%
M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	1.29E-02	1.74E-03	5.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.11E-02	1.17E-02	3.78E-02	2.90E-03	1.74E-02	100%
M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.32E-02	1.30E-02	1.76E-03	5.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.12E-02	1.16E-02	3.80E-02	2.93E-03	1.75E-02	100%
M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.27E-02	1.44E-02	2.31E-03	6.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.44E-02	1.01E-02	4.42E-02	3.85E-03	2.02E-02	100%
M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	1.82E-02	3.93E-03	7.14E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.35E-02	7.26E-03	5.90E-02	6.56E-03	2.62E-02	100%
M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.81E-02	1.33E-02	1.24E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.12E-01	3.43E-03	1.05E-01	2.22E-02	4.16E-02	100%
M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.40E-02	1.12E-02	1.10E-03	5.04E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.80E-02	1.41E-02	2.98E-02	1.84E-03	1.40E-02	100%
M5-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.38E-02	1.17E-02	1.27E-03	5.21E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.88E-02	1.34E-02	3.20E-02	2.11E-03	1.49E-02	100%
M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.37E-02	1.19E-02	1.33E-03	5.27E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.92E-02	1.32E-02	3.28E-02	2.21E-03	1.53E-02	100%
M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.37E-02	1.19E-02	1.34E-03	5.28E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.92E-02	1.31E-02	3.30E-02	2.23E-03	1.54E-02	100%
M5-M1	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	1.28E-02	1.63E-03	5.56E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.09E-02	1.20E-02	3.68E-02	2.72E-03	1.70E-02	100%
M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	1.45E-02	2.31E-03	6.10E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.47E-02	1.01E-02	4.45E-02	3.85E-03	2.03E-02	100%
M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	1.83E-02	3.93E-03	7.19E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.38E-02	7.28E-03	5.93E-02	6.56E-03	2.64E-02	100%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.82E-02	1.33E-02	1.25E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.45E-03	1.06E-01	2.22E-02	4.17E-02	100%
M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.42E-02	1.08E-02	9.21E-04	4.93E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.79E-02	1.52E-02	2.75E-02	1.53E-03	1.30E-02	100%
M6-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.40E-02	1.12E-02	1.03E-03	5.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.85E-02	1.47E-02	2.91E-02	1.72E-03	1.37E-02	100%
M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.39E-02	1.13E-02	1.07E-03	5.11E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.87E-02	1.45E-02	2.97E-02	1.79E-03	1.39E-02	100%
M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.39E-02	1.13E-02	1.08E-03	5.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.87E-02	1.45E-02	2.98E-02	1.80E-03	1.40E-02	100%
M6-M1	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.37E-02	1.19E-02	1.26E-03	5.33E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.97E-02	1.37E-02	3.23E-02	2.11E-03	1.51E-02	100%
M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.33E-02	1.30E-02	1.63E-03	5.69E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.18E-02	1.23E-02	3.72E-02	2.72E-03	1.72E-02	100%
M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	1.48E-02	2.31E-03	6.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.56E-02	1.04E-02	4.49E-02	3.85E-03	2.05E-02	100%
M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.86E-02	3.93E-03	7.33E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.47E-02	7.51E-03	5.96E-02	6.56E-03	2.65E-02	100%
M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.85E-02	1.33E-02	1.26E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.64E-03	1.06E-01	2.22E-02	4.19E-02	100%
M7-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.53E-02	1.11E-02	7.91E-04	5.16E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.09E-02	1.75E-02	2.59E-02	1.32E-03	1.23E-02	100%
M7-OD	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.51E-02	1.15E-02	8.71E-04	5.29E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.14E-02	1.71E-02	2.71E-02	1.45E-03	1.28E-02	100%
M7-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.51E-02	1.16E-02	8.99E-04	5.34E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.15E-02	1.70E-02	2.76E-02	1.50E-03	1.30E-02	100%
M7-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.51E-02	1.16E-02	9.05E-04	5.35E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.15E-02	1.69E-02	2.77E-02	1.51E-03	1.31E-02	100%
M7-M1	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.49E-02	1.21E-02	1.03E-03	5.53E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.22E-02	1.63E-02	2.96E-02	1.72E-03	1.39E-02	100%
M7-M2	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.45E-02	1.29E-02	1.26E-03	5.83E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.35E-02	1.53E-02	3.29E-02	2.11E-03	1.54E-02	100%
M7-M3	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.41E-02	1.41E-02	1.63E-03	6.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.56E-02	1.39E-02	3.78E-02	2.72E-03	1.76E-02	100%
M7-M4	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.33E-02	1.60E-02	2.31E-03	6.86E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.95E-02	1.18E-02	4.58E-02	3.85E-03	2.10E-02	100%
M7-M5	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.17E-02	2.01E-02	3.93E-03	8.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.86E-02	8.85E-03	6.09E-02	6.56E-03	2.72E-02	100%
M7-M6	0.09	0.09	0.09	0.09	1.67E-01	2.11E-01	8.51E-02	4.04E-02	1.33E-02	1.36E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.17E-01	4.58E-03	1.08E-01	2.22E-02	4.30E-02	100%
M8-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.50E-02	3.25E-03	5.89E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.05E-01	3.83E-02	2.88E-02	3.25E-03	1.28E-02	100%
M8-OD	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.56E-02	3.51E-03	6.05E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.06E-01	3.78E-02	3.03E-02	3.51E-03	1.34E-02	100%
M8-PO1(OD)	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.58E-02	3.60E-03	6.10E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.06E-01	3.77E-02	3.08E-02	3.60E-03	1.36E-02	100%
M8-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.58E-02	3.62E-03	6.11E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.06E-01	3.76E-02	3.09E-02	3.62E-03	1.36E-02	100%
M8-M1	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.67E-02	4.01E-03	6.33E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.07E-01	3.70E-02	3.30E-02	4.01E-03	1.45E-02	100%
M8-M2	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.54E-01	1.80E-02	4.67E-03	6.68E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.08E-01	3.59E-02	3.65E-02	4.67E-03	1.59E-02	100%
M8-M3	0.36	0.36	0.405	0.315	2.21E-02	3.27E-01	1.53E-01	1.99E-02	5.59E-03	7.15E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.10E-01	3.46E-02	4.12E-02	5.59E-03	1.78E-02	100%
M8-M4	0.36	0.36	0.405	0.315	2.21E-02	3.27E-01	1.52E-01	2.26E-02	6.96E-03	7.79E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.14E-01	3.28E-02	4.80E-02	6.96E-03	2.05E-02	100%
M8-M5	0.36	0.36	0.405	0.315	2.21E-02	3.29E-01	1.51E-01	2.68E-02	9.23E-03	8.80E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.19E-01	3.04E-02	5.84E-02	9.23E-03	2.46E-02	100%
M8-M6	0.36	0.36	0.405	0.315	2.21E-02	3.31E-01	1.48E-01	3.51E-02	1.37E-02	1.07E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.30E-01	2.69E-02	7.66E-02	1.37E-02	3.14E-02	100%
M8-M7	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.42E-01	5.79E-02	2.66E-02	1.57E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.60E-01	2.15E-02	1.17E-01	2.66E-02	4.53E-02	100%
M9-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.32E-02	2.45E-03	5.36E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.09E-01	4.25E-02	2.39E-02	2.45E-03	1.07E-02	100%
M9-OD	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.35E-02	2.60E-03	5.46E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.09E-01	4.22E-02	2.47E-02	2.60E-03	1.11E-02	100%
M9-PO1(OD)	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.36E-02	2.65E-03	5.50E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.09E-01	4.21E-02	2.50E-02	2.65E-03	1.12E-02	100%
M9-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.37E-02	2.66E-03	5.50E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.09E-01	4.21E-02	2.51E-02	2.66E-03	1.12E-02	100%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M9-M1	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.41E-02	2.86E-03	5.64E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.10E-01	4.17E-02	2.62E-02	2.86E-03	1.17E-02	100%
M9-M2	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.49E-02	3.19E-03	5.85E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.10E-01	4.11E-02	2.80E-02	3.19E-03	1.24E-02	100%
M9-M3	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.63E-01	1.58E-02	3.59E-03	6.09E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.11E-01	4.03E-02	3.02E-02	3.59E-03	1.33E-02	100%
M9-M4	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.63E-01	1.69E-02	4.11E-03	6.38E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.12E-01	3.94E-02	3.29E-02	4.11E-03	1.44E-02	100%
M9-M5	0.36	0.36	0.405	0.315	2.21E-02	3.43E-01	1.62E-01	1.83E-02	4.81E-03	6.74E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.13E-01	3.83E-02	3.65E-02	4.81E-03	1.59E-02	100%
M9-M6	0.36	0.36	0.405	0.315	2.21E-02	3.43E-01	1.61E-01	2.02E-02	5.79E-03	7.20E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.15E-01	3.68E-02	4.14E-02	5.79E-03	1.78E-02	100%
M9-M7	0.36	0.36	0.405	0.315	2.21E-02	3.44E-01	1.60E-01	2.30E-02	7.28E-03	7.84E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.18E-01	3.48E-02	4.86E-02	7.28E-03	2.06E-02	100%
M9-M8	0.36	0.36	0.405	0.315	2.21E-02	3.57E-01	1.50E-01	5.71E-02	2.66E-02	1.53E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.63E-01	2.32E-02	1.16E-01	2.66E-02	4.49E-02	100%
M10-FOX	2.7	1.8	2.86	1.64	2.10E-02	1.78E-01	7.60E-02	2.63E-02	1.55E-02	5.39E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.07E-02	2.16E-02	4.74E-02	1.55E-02	1.60E-02	100%
M10-OD	2.7	1.8	2.86	1.64	2.10E-02	1.79E-01	7.57E-02	2.72E-02	1.62E-02	5.52E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.17E-02	2.12E-02	4.92E-02	1.62E-02	1.65E-02	100%
M10-PO1(OD)	2.7	1.8	2.86	1.64	2.10E-02	1.79E-01	7.56E-02	2.76E-02	1.64E-02	5.56E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.20E-02	2.11E-02	4.98E-02	1.64E-02	1.67E-02	100%
M10-PO1(FOX)	2.7	1.8	2.86	1.64	2.10E-02	1.79E-01	7.56E-02	2.76E-02	1.65E-02	5.57E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.21E-02	2.11E-02	4.99E-02	1.65E-02	1.67E-02	100%
M10-M1	2.7	1.8	2.86	1.64	2.10E-02	1.79E-01	7.51E-02	2.89E-02	1.74E-02	5.74E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.34E-02	2.06E-02	5.23E-02	1.74E-02	1.74E-02	100%
M10-M2	2.7	1.8	2.86	1.64	2.10E-02	1.80E-01	7.45E-02	3.09E-02	1.89E-02	6.02E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.55E-02	1.99E-02	5.58E-02	1.89E-02	1.85E-02	100%
M10-M3	2.7	1.8	2.86	1.64	2.10E-02	1.81E-01	7.38E-02	3.33E-02	2.06E-02	6.34E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.80E-02	1.91E-02	5.99E-02	2.06E-02	1.96E-02	100%
M10-M4	2.7	1.8	2.86	1.64	2.10E-02	1.82E-01	7.30E-02	3.62E-02	2.27E-02	6.74E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.01E-01	1.82E-02	6.47E-02	2.27E-02	2.10E-02	100%
M10-M5	2.7	1.8	2.86	1.64	2.10E-02	1.84E-01	7.20E-02	3.96E-02	2.52E-02	7.23E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.05E-01	1.72E-02	7.03E-02	2.52E-02	2.26E-02	100%
M10-M6	2.7	1.8	2.86	1.64	2.10E-02	1.86E-01	7.09E-02	4.40E-02	2.83E-02	7.85E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.09E-01	1.61E-02	7.72E-02	2.83E-02	2.44E-02	100%
M10-M7	2.7	1.8	2.86	1.64	2.10E-02	1.89E-01	6.95E-02	4.97E-02	3.24E-02	8.65E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.15E-01	1.49E-02	8.56E-02	3.24E-02	2.66E-02	100%
M10-M8	2.7	1.8	2.86	1.64	2.10E-02	2.07E-01	6.36E-02	7.99E-02	5.41E-02	1.29E-02	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.47E-01	1.08E-02	1.26E-01	5.41E-02	3.58E-02	100%
M10-M9	2.7	1.8	2.86	1.64	2.10E-02	3.25E-01	5.13E-02	2.23E-01	1.65E-01	2.91E-02	100%
	2.7	7.2	2.86	7.04	2.10E-02	2.90E-01	5.78E-03	2.79E-01	1.65E-01	5.71E-02	100%

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12.14.3.2.2 Structure B 25 ℃

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M1-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.87E-01	6.59E-02	1.81E-02	4.21E-03	6.94E-03	3.73E-02	3.15E-03	1.71E-02	100%
	0.054	2.16	0.039	2.175	1.50E+01	1.22E-01	1.12E-06	4.16E-02	4.21E-03	1.87E-02	8.02E-02	3.15E-03	3.85E-02	100%
M2-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.80E-01	7.30E-02	2.07E-02	4.21E-03	8.23E-03	1.29E-02	2.47E-03	5.21E-03	100%
	0.054	2.16	0.039	2.175	1.50E+01	9.34E-02	6.23E-05	5.74E-02	4.21E-03	2.66E-02	3.59E-02	2.47E-03	1.67E-02	100%
M2-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.79E-02	1.17E-02	4.54E-03	3.59E-03	3.14E-02	1.77E-02	6.84E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.34E-01	5.55E-04	3.81E-02	7.93E-03	1.51E-02	9.45E-02	2.86E-02	3.29E-02	100%
M2-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.41E-01	9.50E-02	2.17E-02	9.62E-03	6.06E-03	2.97E-02	1.77E-02	5.95E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.50E-01	7.82E-05	6.47E-02	1.68E-02	2.39E-02	8.49E-02	2.86E-02	2.82E-02	100%
M2-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.45E-01	9.20E-02	3.14E-02	1.47E-02	8.38E-03	2.91E-02	1.77E-02	5.70E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.65E-01	2.21E-05	8.53E-02	2.56E-02	2.98E-02	8.01E-02	2.86E-02	2.57E-02	100%
M2-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.46E-01	9.11E-02	3.48E-02	1.64E-02	9.18E-03	2.91E-02	1.77E-02	5.66E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.71E-01	1.61E-05	9.17E-02	2.87E-02	3.15E-02	7.89E-02	2.86E-02	2.52E-02	100%
M3-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.79E-01	7.43E-02	2.25E-02	4.21E-03	9.16E-03	7.74E-03	1.34E-03	3.20E-03	100%
	0.054	2.16	0.039	2.175	1.50E+01	8.78E-02	2.60E-04	6.48E-02	4.21E-03	3.03E-02	2.25E-02	1.34E-03	1.06E-02	100%
M3-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.32E-01	1.04E-01	1.32E-02	4.54E-03	4.32E-03	1.14E-02	5.25E-03	3.08E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	9.44E-02	2.07E-03	4.80E-02	7.93E-03	2.00E-02	4.23E-02	8.46E-03	1.69E-02	100%
M3-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.35E-01	1.01E-01	2.33E-02	9.62E-03	6.86E-03	1.02E-02	5.25E-03	2.49E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.15E-01	6.81E-04	7.75E-02	1.68E-02	3.03E-02	3.60E-02	8.46E-03	1.38E-02	100%
M3-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.32E-02	8.09E-03	2.70E-03	2.69E-03	3.47E-02	1.86E-02	8.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.24E-01	1.05E-03	2.48E-02	4.51E-03	1.02E-02	9.70E-02	2.79E-02	3.46E-02	100%
M3-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.25E-02	1.09E-02	3.95E-03	3.50E-03	3.36E-02	1.86E-02	7.51E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.88E-04	3.31E-02	6.58E-03	1.33E-02	9.34E-02	2.79E-02	3.28E-02	100%
M3-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.77E-02	3.32E-02	1.47E-02	9.26E-03	9.88E-03	5.25E-03	2.32E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.33E-01	3.72E-04	9.92E-02	2.56E-02	3.68E-02	3.30E-02	8.46E-03	1.23E-02	100%
M3-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.40E-01	9.67E-02	3.66E-02	1.64E-02	1.01E-02	9.82E-03	5.25E-03	2.29E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.39E-01	3.22E-04	1.06E-01	2.87E-02	3.85E-02	3.23E-02	8.46E-03	1.19E-02	100%
M3-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.22E-02	1.24E-02	4.60E-03	3.89E-03	3.33E-02	1.86E-02	7.31E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.29E-01	3.37E-04	3.69E-02	7.66E-03	1.46E-02	9.18E-02	2.79E-02	3.20E-02	100%
M3-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.21E-02	1.27E-02	4.75E-03	3.98E-03	3.32E-02	1.86E-02	7.27E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.30E-01	3.09E-04	3.78E-02	7.92E-03	1.50E-02	9.14E-02	2.79E-02	3.18E-02	100%
M3-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M4-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.79E-01	7.47E-02	2.36E-02	4.21E-03	9.72E-03	5.62E-03	9.15E-04	2.35E-03	100%
	0.054	2.16	0.039	2.175	1.50E+01	8.59E-02	4.99E-04	6.85E-02	4.21E-03	3.22E-02	1.64E-02	9.15E-04	7.76E-03	100%
M4-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.32E-01	1.05E-01	1.43E-02	4.54E-03	4.88E-03	7.55E-03	3.08E-03	2.23E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.71E-02	3.48E-03	5.20E-02	7.93E-03	2.20E-02	2.81E-02	4.96E-03	1.16E-02	100%
M4-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.46E-02	9.62E-03	7.50E-03	6.58E-03	3.08E-03	1.75E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.09E-01	1.50E-03	8.25E-02	1.68E-02	3.29E-02	2.35E-02	4.96E-03	9.29E-03	100%
M4-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.97E-02	9.19E-03	2.70E-03	3.24E-03	1.29E-02	5.51E-03	3.68E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.33E-02	3.08E-03	3.17E-02	4.51E-03	1.36E-02	4.55E-02	8.24E-03	1.86E-02	100%
M4-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.89E-02	1.21E-02	3.95E-03	4.07E-03	1.21E-02	5.51E-03	3.27E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.83E-02	1.96E-03	4.15E-02	6.58E-03	1.74E-02	4.29E-02	8.24E-03	1.73E-02	100%
M4-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.37E-02	5.76E-03	1.82E-03	1.97E-03	3.56E-02	1.86E-02	8.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.21E-01	1.52E-03	1.79E-02	3.04E-03	7.43E-03	1.00E-01	2.79E-02	3.61E-02	100%
M4-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.35E-02	7.02E-03	2.31E-03	2.35E-03	3.49E-02	1.86E-02	8.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	1.11E-03	2.18E-02	3.85E-03	8.98E-03	9.81E-02	2.79E-02	3.51E-02	100%
M4-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.85E-02	3.46E-02	1.47E-02	9.94E-03	6.29E-03	3.08E-03	1.61E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.28E-01	9.75E-04	1.05E-01	2.56E-02	3.95E-02	2.13E-02	4.96E-03	8.19E-03	100%
M4-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.76E-02	3.80E-02	1.64E-02	1.08E-02	6.24E-03	3.08E-03	1.58E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.34E-01	8.83E-04	1.11E-01	2.87E-02	4.13E-02	2.08E-02	4.96E-03	7.94E-03	100%
M4-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.85E-02	1.35E-02	4.60E-03	4.47E-03	1.18E-02	5.51E-03	3.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	9.09E-02	1.61E-03	4.59E-02	7.66E-03	1.91E-02	4.18E-02	8.24E-03	1.68E-02	100%
M4-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.84E-02	1.39E-02	4.75E-03	4.56E-03	1.17E-02	5.51E-03	3.11E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	9.15E-02	1.54E-03	4.70E-02	7.92E-03	1.95E-02	4.15E-02	8.24E-03	1.66E-02	100%
M4-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.34E-02	7.54E-03	2.52E-03	2.51E-03	3.47E-02	1.86E-02	8.01E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.23E-01	9.69E-04	2.34E-02	4.20E-03	9.60E-03	9.74E-02	2.79E-02	3.48E-02	100%
M4-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.34E-02	7.65E-03	2.57E-03	2.54E-03	3.46E-02	1.86E-02	7.99E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.23E-01	9.41E-04	2.37E-02	4.28E-03	9.73E-03	9.72E-02	2.79E-02	3.47E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M4-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.30E-02	3.19E-02	1.33E-02	9.28E-03	1.08E-02	5.51E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	4.62E-04	8.65E-02	2.22E-02	3.22E-02	3.48E-02	8.24E-03	1.33E-02	100%
M4-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.26E-02	1.08E-02	3.93E-03	3.45E-03	3.35E-02	1.86E-02	7.45E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.29E-04	3.29E-02	6.56E-03	1.32E-02	9.33E-02	2.79E-02	3.27E-02	100%
M4-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M5-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.78E-01	7.48E-02	2.44E-02	4.21E-03	1.01E-02	4.43E-03	6.96E-04	1.87E-03	100%
	0.054	2.16	0.039	2.175	1.50E+01	8.51E-02	7.13E-04	7.07E-02	4.21E-03	3.33E-02	1.30E-02	6.96E-04	6.13E-03	100%
M5-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.32E-01	1.05E-01	1.51E-02	4.54E-03	5.28E-03	5.75E-03	2.18E-03	1.79E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.43E-02	4.50E-03	5.42E-02	7.93E-03	2.31E-02	2.11E-02	3.51E-03	8.80E-03	100%
M5-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.55E-02	9.62E-03	7.93E-03	4.92E-03	2.18E-03	1.37E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.07E-01	2.16E-03	8.51E-02	1.68E-02	3.42E-02	1.75E-02	3.51E-03	7.01E-03	100%
M5-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	1.01E-02	2.70E-03	3.72E-03	8.71E-03	3.23E-03	2.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.51E-02	4.85E-03	3.46E-02	4.51E-03	1.51E-02	3.07E-02	4.83E-03	1.30E-02	100%
M5-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	1.31E-02	3.95E-03	4.59E-03	8.02E-03	3.23E-03	2.39E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.07E-02	3.43E-03	4.51E-02	6.58E-03	1.92E-02	2.88E-02	4.83E-03	1.20E-02	100%
M5-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	6.72E-03	1.82E-03	2.45E-03	1.36E-02	5.51E-03	4.04E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.90E-02	4.04E-03	2.32E-02	3.04E-03	1.01E-02	4.77E-02	8.24E-03	1.97E-02	100%
M5-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	8.03E-03	2.31E-03	2.86E-03	1.30E-02	5.51E-03	3.76E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.09E-02	3.29E-03	2.80E-02	3.85E-03	1.21E-02	4.63E-02	8.24E-03	1.90E-02	100%
M5-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.39E-02	4.53E-03	1.37E-03	1.58E-03	3.62E-02	1.86E-02	8.81E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.94E-03	1.40E-02	2.29E-03	5.87E-03	1.02E-01	2.79E-02	3.70E-02	100%
M5-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.25E-03	1.64E-03	1.81E-03	3.58E-02	1.86E-02	8.58E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.66E-03	1.63E-02	2.73E-03	6.80E-03	1.01E-01	2.79E-02	3.64E-02	100%
M5-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.88E-02	3.55E-02	1.47E-02	1.04E-02	4.67E-03	2.18E-03	1.24E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.26E-01	1.50E-03	1.07E-01	2.56E-02	4.08E-02	1.58E-02	3.51E-03	6.15E-03	100%
M5-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.79E-02	3.88E-02	1.64E-02	1.12E-02	4.62E-03	2.18E-03	1.22E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.32E-01	1.38E-03	1.14E-01	2.87E-02	4.26E-02	1.54E-02	3.51E-03	5.96E-03	100%
M5-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.96E-02	1.46E-02	4.60E-03	5.00E-03	7.78E-03	3.23E-03	2.27E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.36E-02	2.95E-03	4.98E-02	7.66E-03	2.11E-02	2.80E-02	4.83E-03	1.16E-02	100%
M5-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.95E-02	1.49E-02	4.75E-03	5.09E-03	7.74E-03	3.23E-03	2.25E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.43E-02	2.85E-03	5.08E-02	7.92E-03	2.15E-02	2.78E-02	4.83E-03	1.15E-02	100%
M5-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	8.99E-02	8.57E-03	2.52E-03	3.02E-03	1.28E-02	5.51E-03	3.66E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.18E-02	3.03E-03	3.00E-02	4.20E-03	1.29E-02	4.58E-02	8.24E-03	1.88E-02	100%
M5-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	8.99E-02	8.69E-03	2.57E-03	3.06E-03	1.28E-02	5.51E-03	3.64E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.20E-02	2.97E-03	3.04E-02	4.28E-03	1.30E-02	4.57E-02	8.24E-03	1.87E-02	100%
M5-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.53E-03	1.74E-03	1.89E-03	3.56E-02	1.86E-02	8.50E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.21E-01	1.56E-03	1.72E-02	2.90E-03	7.15E-03	1.00E-01	2.79E-02	3.62E-02	100%
M5-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.58E-03	1.76E-03	1.91E-03	3.56E-02	1.86E-02	8.49E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.21E-01	1.53E-03	1.74E-02	2.93E-03	7.22E-03	1.00E-01	2.79E-02	3.62E-02	100%
M5-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.40E-02	3.32E-02	1.33E-02	9.93E-03	6.91E-03	3.23E-03	1.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.17E-01	1.18E-03	9.15E-02	2.22E-02	3.47E-02	2.28E-02	4.83E-03	8.99E-03	100%
M5-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.90E-02	1.20E-02	3.93E-03	4.01E-03	1.20E-02	5.51E-03	3.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.79E-02	1.87E-03	4.13E-02	6.56E-03	1.74E-02	4.28E-02	8.24E-03	1.73E-02	100%
M5-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.35E-02	7.00E-03	2.31E-03	2.35E-03	3.49E-02	1.86E-02	8.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	1.09E-03	2.18E-02	3.85E-03	8.96E-03	9.81E-02	2.79E-02	3.51E-02	100%
M5-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.30E-02	3.19E-02	1.33E-02	9.28E-03	1.08E-02	5.51E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	4.62E-04	8.65E-02	2.22E-02	3.22E-02	3.48E-02	8.24E-03	1.33E-02	100%
M5-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.26E-02	1.08E-02	3.93E-03	3.45E-03	3.35E-02	1.86E-02	7.45E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.29E-04	3.29E-02	6.56E-03	1.32E-02	9.33E-02	2.79E-02	3.27E-02	100%
M5-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M6-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.78E-01	7.49E-02	2.49E-02	4.21E-03	1.04E-02	3.66E-03	5.61E-04	1.55E-03	100%
	0.054	2.16	0.039	2.175	1.50E+01	8.46E-02	8.86E-04	7.22E-02	4.21E-03	3.40E-02	1.07E-02	5.61E-04	5.07E-03	100%
M6-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.57E-02	4.54E-03	5.57E-03	4.68E-03	1.69E-03	1.49E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.29E-02	5.19E-03	5.56E-02	7.93E-03	2.38E-02	1.69E-02	2.72E-03	7.11E-03	100%
M6-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.61E-02	9.62E-03	8.23E-03	3.94E-03	1.69E-03	1.13E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.06E-01	2.63E-03	8.68E-02	1.68E-02	3.50E-02	1.40E-02	2.72E-03	5.63E-03	100%
M6-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.14E-02	1.09E-02	2.70E-03	4.08E-03	6.76E-03	2.29E-03	2.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.18E-02	6.11E-03	3.63E-02	4.51E-03	1.59E-02	2.33E-02	3.42E-03	9.96E-03	100%
M6-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	1.39E-02	3.95E-03	4.96E-03	6.14E-03	2.29E-03	1.93E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.78E-02	4.50E-03	4.70E-02	6.58E-03	2.02E-02	2.18E-02	3.42E-03	9.17E-03	100%
M6-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	7.55E-03	1.82E-03	2.87E-03	9.37E-03	3.23E-03	3.07E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.03E-02	6.10E-03	2.56E-02	3.04E-03	1.13E-02	3.25E-02	4.83E-03	1.38E-02	100%
M6-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.13E-02	8.92E-03	2.31E-03	3.30E-03	8.87E-03	3.23E-03	2.82E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.09	1.5	0.141	1.449	8.46E-02	7.25E-02	5.17E-03	3.07E-02	3.85E-03	1.34E-02	3.14E-02	4.83E-03	1.33E-02	100%
M6-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	5.39E-03	1.37E-03	2.01E-03	1.42E-02	5.51E-03	4.34E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.72E-02	4.80E-03	1.84E-02	2.29E-03	8.06E-03	4.92E-02	8.24E-03	2.05E-02	100%
M6-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	6.17E-03	1.64E-03	2.27E-03	1.38E-02	5.51E-03	4.14E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.81E-02	4.30E-03	2.13E-02	2.73E-03	9.27E-03	4.82E-02	8.24E-03	2.00E-02	100%
M6-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	3.74E-03	1.10E-03	1.32E-03	3.68E-02	1.86E-02	9.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.25E-03	1.16E-02	1.84E-03	4.86E-03	1.03E-01	2.79E-02	3.76E-02	100%
M6-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	4.21E-03	1.27E-03	1.47E-03	3.64E-02	1.86E-02	8.90E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.06E-03	1.31E-02	2.11E-03	5.48E-03	1.02E-01	2.79E-02	3.72E-02	100%
M6-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.89E-02	3.61E-02	1.47E-02	1.07E-02	3.72E-03	1.69E-03	1.02E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.25E-01	1.87E-03	1.09E-01	2.56E-02	4.17E-02	1.26E-02	2.72E-03	4.93E-03	100%
M6-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.80E-02	3.95E-02	1.64E-02	1.15E-02	3.68E-03	1.69E-03	1.00E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.31E-01	1.73E-03	1.16E-01	2.87E-02	4.35E-02	1.23E-02	2.72E-03	4.77E-03	100%
M6-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.00E-02	1.54E-02	4.60E-03	5.38E-03	5.94E-03	2.29E-03	1.83E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.08E-02	3.95E-03	5.18E-02	7.66E-03	2.21E-02	2.11E-02	3.42E-03	8.84E-03	100%
M6-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	8.99E-02	1.57E-02	4.75E-03	5.48E-03	5.90E-03	2.29E-03	1.81E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.16E-02	3.84E-03	5.29E-02	7.92E-03	2.25E-02	2.10E-02	3.42E-03	8.77E-03	100%
M6-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	9.48E-03	2.52E-03	3.48E-03	8.70E-03	3.23E-03	2.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.35E-02	4.84E-03	3.28E-02	4.20E-03	1.43E-02	3.10E-02	4.83E-03	1.31E-02	100%
M6-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	9.60E-03	2.57E-03	3.52E-03	8.67E-03	3.23E-03	2.72E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.37E-02	4.77E-03	3.33E-02	4.28E-03	1.45E-02	3.09E-02	4.83E-03	1.30E-02	100%
M6-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	6.46E-03	1.74E-03	2.36E-03	1.36E-02	5.51E-03	4.07E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.85E-02	4.12E-03	2.23E-02	2.90E-03	9.73E-03	4.79E-02	8.24E-03	1.98E-02	100%
M6-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	6.52E-03	1.76E-03	2.38E-03	1.36E-02	5.51E-03	4.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.86E-02	4.09E-03	2.26E-02	2.93E-03	9.82E-03	4.79E-02	8.24E-03	1.98E-02	100%
M6-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	4.39E-03	1.33E-03	1.53E-03	3.63E-02	1.86E-02	8.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.99E-03	1.36E-02	2.21E-03	5.70E-03	1.02E-01	2.79E-02	3.71E-02	100%
M6-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	4.42E-03	1.34E-03	1.54E-03	3.63E-02	1.86E-02	8.83E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.97E-03	1.37E-02	2.23E-03	5.75E-03	1.02E-01	2.79E-02	3.71E-02	100%
M6-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.43E-02	3.40E-02	1.33E-02	1.04E-02	5.16E-03	2.29E-03	1.44E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.15E-01	1.79E-03	9.41E-02	2.22E-02	3.60E-02	1.70E-02	3.42E-03	6.80E-03	100%
M6-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	1.30E-02	3.93E-03	4.51E-03	7.96E-03	3.23E-03	2.37E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.03E-02	3.33E-03	4.49E-02	6.56E-03	1.92E-02	2.88E-02	4.83E-03	1.20E-02	100%
M6-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	8.01E-03	2.31E-03	2.85E-03	1.30E-02	5.51E-03	3.75E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.08E-02	3.27E-03	2.80E-02	3.85E-03	1.21E-02	4.63E-02	8.24E-03	1.90E-02	100%
M6-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.24E-03	1.63E-03	1.80E-03	3.58E-02	1.86E-02	8.58E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.66E-03	1.63E-02	2.72E-03	6.79E-03	1.01E-01	2.79E-02	3.64E-02	100%
M6-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.40E-02	3.32E-02	1.33E-02	9.93E-03	6.91E-03	3.23E-03	1.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.17E-01	1.18E-03	9.15E-02	2.22E-02	3.47E-02	2.28E-02	4.83E-03	8.99E-03	100%
M6-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.90E-02	1.20E-02	3.93E-03	4.01E-03	1.20E-02	5.51E-03	3.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.79E-02	1.87E-03	4.13E-02	6.56E-03	1.74E-02	4.28E-02	8.24E-03	1.73E-02	100%
M6-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.35E-02	7.00E-03	2.31E-03	2.35E-03	3.49E-02	1.86E-02	8.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	1.09E-03	2.18E-02	3.85E-03	8.96E-03	9.81E-02	2.79E-02	3.51E-02	100%
M6-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.30E-02	3.19E-02	1.33E-02	9.28E-03	1.08E-02	5.51E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	4.62E-04	8.65E-02	2.22E-02	3.22E-02	3.48E-02	8.24E-03	1.33E-02	100%
M6-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.26E-02	1.08E-02	3.93E-03	3.45E-03	3.35E-02	1.86E-02	7.45E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.29E-04	3.29E-02	6.56E-03	1.32E-02	9.33E-02	2.79E-02	3.27E-02	100%
M6-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M7-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.78E-01	7.50E-02	2.53E-02	4.21E-03	1.05E-02	3.12E-03	4.70E-04	1.33E-03	100%
	0.054	2.16	0.039	2.175	1.50E+01	8.44E-02	1.02E-03	7.32E-02	4.21E-03	3.45E-02	9.13E-03	4.70E-04	4.33E-03	100%
M7-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.61E-02	4.54E-03	5.79E-03	3.95E-03	1.37E-03	1.29E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.22E-02	5.67E-03	5.67E-02	7.93E-03	2.44E-02	1.42E-02	2.22E-03	5.98E-03	100%
M7-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.65E-02	9.62E-03	8.44E-03	3.30E-03	1.37E-03	9.62E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.05E-01	2.95E-03	8.80E-02	1.68E-02	3.56E-02	1.16E-02	2.22E-03	4.71E-03	100%
M7-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	1.14E-02	2.70E-03	4.35E-03	5.58E-03	1.77E-03	1.90E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.02E-02	6.96E-03	3.74E-02	4.51E-03	1.65E-02	1.89E-02	2.65E-03	8.12E-03	100%
M7-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	1.44E-02	3.95E-03	5.25E-03	5.02E-03	1.77E-03	1.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.64E-02	5.24E-03	4.83E-02	6.58E-03	2.09E-02	1.75E-02	2.65E-03	7.45E-03	100%
M7-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.22E-02	8.20E-03	1.82E-03	3.19E-03	7.37E-03	2.29E-03	2.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.68E-02	7.52E-03	2.69E-02	3.04E-03	1.20E-02	2.48E-02	3.42E-03	1.07E-02	100%
M7-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	9.60E-03	2.31E-03	3.65E-03	6.92E-03	2.29E-03	2.32E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.91E-02	6.49E-03	3.23E-02	3.85E-03	1.42E-02	2.39E-02	3.42E-03	1.02E-02	100%
M7-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	6.14E-03	1.37E-03	2.39E-03	9.93E-03	3.23E-03	3.35E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.09	1.5	0.141	1.449	8.46E-02	6.81E-02	7.04E-03	2.04E-02	2.29E-03	9.05E-03	3.37E-02	4.83E-03	1.44E-02	100%
M7-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	6.97E-03	1.64E-03	2.67E-03	9.55E-03	3.23E-03	3.16E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.92E-02	6.43E-03	2.35E-02	2.73E-03	1.04E-02	3.29E-02	4.83E-03	1.40E-02	100%
M7-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.08E-02	4.52E-03	1.10E-03	1.71E-03	1.47E-02	5.51E-03	4.58E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.62E-02	5.34E-03	1.53E-02	1.84E-03	6.73E-03	5.02E-02	8.24E-03	2.10E-02	100%
M7-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	5.05E-03	1.27E-03	1.89E-03	1.44E-02	5.51E-03	4.42E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.68E-02	5.01E-03	1.72E-02	2.11E-03	7.54E-03	4.96E-02	8.24E-03	2.07E-02	100%
M7-M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.41E-02	3.19E-03	9.21E-04	1.13E-03	3.71E-02	1.86E-02	9.26E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.47E-03	9.84E-03	1.53E-03	4.15E-03	1.04E-01	2.79E-02	3.81E-02	100%
M7-M6-OD	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.41E-02	3.53E-03	1.03E-03	1.25E-03	3.69E-02	1.86E-02	9.14E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.33E-03	1.09E-02	1.72E-03	4.59E-03	1.03E-01	2.79E-02	3.78E-02	100%
M7-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.90E-02	3.65E-02	1.47E-02	1.09E-02	3.10E-03	1.37E-03	8.65E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.25E-01	2.13E-03	1.10E-01	2.56E-02	4.22E-02	1.04E-02	2.22E-03	4.11E-03	100%
M7-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.80E-02	3.99E-02	1.64E-02	1.17E-02	3.07E-03	1.37E-03	8.47E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.31E-01	1.97E-03	1.17E-01	2.87E-02	4.41E-02	1.02E-02	2.22E-03	3.98E-03	100%
M7-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.02E-02	1.59E-02	4.60E-03	5.67E-03	4.84E-03	1.77E-03	1.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.95E-02	4.64E-03	5.32E-02	7.66E-03	2.28E-02	1.70E-02	2.65E-03	7.17E-03	100%
M7-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	1.63E-02	4.75E-03	5.77E-03	4.80E-03	1.77E-03	1.52E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.02E-02	4.52E-03	5.43E-02	7.92E-03	2.32E-02	1.69E-02	2.65E-03	7.11E-03	100%
M7-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	1.02E-02	2.52E-03	3.83E-03	6.77E-03	2.29E-03	2.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.02E-02	6.12E-03	3.44E-02	4.20E-03	1.51E-02	2.35E-02	3.42E-03	1.01E-02	100%
M7-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.16E-02	1.03E-02	2.57E-03	3.86E-03	6.74E-03	2.29E-03	2.22E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.04E-02	6.04E-03	3.49E-02	4.28E-03	1.53E-02	2.35E-02	3.42E-03	1.00E-02	100%
M7-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	7.28E-03	1.74E-03	2.77E-03	9.43E-03	3.23E-03	3.10E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.97E-02	6.21E-03	2.46E-02	2.90E-03	1.09E-02	3.27E-02	4.83E-03	1.39E-02	100%
M7-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	7.34E-03	1.76E-03	2.79E-03	9.40E-03	3.23E-03	3.09E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.98E-02	6.16E-03	2.49E-02	2.93E-03	1.10E-02	3.26E-02	4.83E-03	1.39E-02	100%
M7-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	5.24E-03	1.33E-03	1.96E-03	1.42E-02	5.51E-03	4.37E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.70E-02	4.88E-03	1.79E-02	2.21E-03	7.83E-03	4.93E-02	8.24E-03	2.05E-02	100%
M7-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	5.27E-03	1.34E-03	1.97E-03	1.42E-02	5.51E-03	4.36E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.70E-02	4.86E-03	1.80E-02	2.23E-03	7.89E-03	4.93E-02	8.24E-03	2.05E-02	100%
M7-M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.41E-02	3.65E-03	1.07E-03	1.29E-03	3.68E-02	1.86E-02	9.09E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.28E-03	1.13E-02	1.79E-03	4.74E-03	1.03E-01	2.79E-02	3.77E-02	100%
M7-M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.41E-02	3.67E-03	1.08E-03	1.30E-03	3.68E-02	1.86E-02	9.08E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.27E-03	1.14E-02	1.80E-03	4.78E-03	1.03E-01	2.79E-02	3.77E-02	100%
M7-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.45E-02	3.47E-02	1.33E-02	1.07E-02	4.14E-03	1.77E-03	1.18E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.14E-01	2.23E-03	9.57E-02	2.22E-02	3.68E-02	1.36E-02	2.65E-03	5.48E-03	100%
M7-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.06E-02	1.37E-02	3.93E-03	4.89E-03	6.10E-03	2.29E-03	1.91E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.74E-02	4.40E-03	4.68E-02	6.56E-03	2.01E-02	2.17E-02	3.42E-03	9.16E-03	100%
M7-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.13E-02	8.90E-03	2.31E-03	3.29E-03	8.86E-03	3.23E-03	2.82E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.24E-02	5.15E-03	3.07E-02	3.85E-03	1.34E-02	3.14E-02	4.83E-03	1.33E-02	100%
M7-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	6.16E-03	1.63E-03	2.26E-03	1.38E-02	5.51E-03	4.14E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.81E-02	4.30E-03	2.12E-02	2.72E-03	9.26E-03	4.82E-02	8.24E-03	2.00E-02	100%
M7-M6-M1	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	4.21E-03	1.26E-03	1.47E-03	3.64E-02	1.86E-02	8.90E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.06E-03	1.31E-02	2.11E-03	5.47E-03	1.02E-01	2.79E-02	3.72E-02	100%
M7-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.43E-02	3.40E-02	1.33E-02	1.04E-02	5.16E-03	2.29E-03	1.44E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.15E-01	1.79E-03	9.41E-02	2.22E-02	3.60E-02	1.70E-02	3.42E-03	6.80E-03	100%
M7-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	1.30E-02	3.93E-03	4.51E-03	7.96E-03	3.23E-03	2.37E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.03E-02	3.33E-03	4.49E-02	6.56E-03	1.92E-02	2.88E-02	4.83E-03	1.20E-02	100%
M7-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	8.01E-03	2.31E-03	2.85E-03	1.30E-02	5.51E-03	3.75E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.08E-02	3.27E-03	2.80E-02	3.85E-03	1.21E-02	4.63E-02	8.24E-03	1.90E-02	100%
M7-M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.24E-03	1.63E-03	1.80E-03	3.58E-02	1.86E-02	8.58E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.66E-03	1.63E-02	2.72E-03	6.79E-03	1.01E-01	2.79E-02	3.64E-02	100%
M7-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.40E-02	3.32E-02	1.33E-02	9.93E-03	6.91E-03	3.23E-03	1.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.17E-01	1.18E-03	9.15E-02	2.22E-02	3.47E-02	2.28E-02	4.83E-03	8.99E-03	100%
M7-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.90E-02	1.20E-02	3.93E-03	4.01E-03	1.20E-02	5.51E-03	3.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.79E-02	1.87E-03	4.13E-02	6.56E-03	1.74E-02	4.28E-02	8.24E-03	1.73E-02	100%
M7-M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.35E-02	7.00E-03	2.31E-03	2.35E-03	3.49E-02	1.86E-02	8.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	1.09E-03	2.18E-02	3.85E-03	8.96E-03	9.81E-02	2.79E-02	3.51E-02	100%
M7-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.30E-02	3.19E-02	1.33E-02	9.28E-03	1.08E-02	5.51E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	4.62E-04	8.65E-02	2.22E-02	3.22E-02	3.48E-02	8.24E-03	1.33E-02	100%
M7-M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.26E-02	1.08E-02	3.93E-03	3.45E-03	3.35E-02	1.86E-02	7.45E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.29E-04	3.29E-02	6.56E-03	1.32E-02	9.33E-02	2.79E-02	3.27E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M7-M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M8-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.78E-01	7.50E-02	2.58E-02	4.21E-03	1.08E-02	2.52E-03	3.71E-04	1.07E-03	100%
	0.054	2.16	0.039	2.175	1.50E+01	8.41E-02	1.17E-03	7.44E-02	4.21E-03	3.51E-02	7.34E-03	3.71E-04	3.48E-03	100%
M8-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.66E-02	4.54E-03	6.06E-03	3.16E-03	1.05E-03	1.05E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.15E-02	6.16E-03	5.80E-02	7.93E-03	2.50E-02	1.12E-02	1.70E-03	4.76E-03	100%
M8-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.70E-02	9.62E-03	8.70E-03	2.60E-03	1.05E-03	7.74E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.05E-01	3.28E-03	8.93E-02	1.68E-02	3.63E-02	9.13E-03	1.70E-03	3.72E-03	100%
M8-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.19E-02	1.21E-02	2.70E-03	4.69E-03	4.37E-03	1.29E-03	1.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.90E-02	7.84E-03	3.88E-02	4.51E-03	1.72E-02	1.44E-02	1.93E-03	6.26E-03	100%
M8-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.09E-02	1.51E-02	3.95E-03	5.59E-03	3.89E-03	1.29E-03	1.30E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.52E-02	5.99E-03	4.99E-02	6.58E-03	2.17E-02	1.34E-02	1.93E-03	5.71E-03	100%
M8-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	9.00E-03	1.82E-03	3.59E-03	5.57E-03	1.54E-03	2.01E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.43E-02	8.95E-03	2.84E-02	3.04E-03	1.27E-02	1.80E-02	2.31E-03	7.84E-03	100%
M8-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.22E-02	1.04E-02	2.31E-03	4.05E-03	5.17E-03	1.54E-03	1.81E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.68E-02	7.81E-03	3.39E-02	3.85E-03	1.50E-02	1.73E-02	2.31E-03	7.47E-03	100%
M8-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.28E-02	7.07E-03	1.37E-03	2.85E-03	7.03E-03	1.92E-03	2.55E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.32E-02	9.30E-03	2.21E-02	2.29E-03	9.93E-03	2.25E-02	2.88E-03	9.79E-03	100%
M8-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	7.94E-03	1.64E-03	3.15E-03	6.70E-03	1.92E-03	2.39E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.44E-02	8.59E-03	2.54E-02	2.73E-03	1.13E-02	2.19E-02	2.88E-03	9.49E-03	100%
M8-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	5.60E-03	1.10E-03	2.25E-03	8.94E-03	2.55E-03	3.20E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.43E-02	8.85E-03	1.77E-02	1.84E-03	7.95E-03	2.89E-02	3.81E-03	1.25E-02	100%
M8-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	6.18E-03	1.27E-03	2.46E-03	8.66E-03	2.55E-03	3.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.50E-02	8.40E-03	1.98E-02	2.11E-03	8.87E-03	2.84E-02	3.81E-03	1.23E-02	100%
M8-M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.19E-02	4.36E-03	9.21E-04	1.72E-03	1.19E-02	3.79E-03	4.07E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.89E-02	7.54E-03	1.42E-02	1.53E-03	6.34E-03	3.96E-02	5.66E-03	1.70E-02	100%
M8-M6-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.19E-02	4.77E-03	1.03E-03	1.87E-03	1.17E-02	3.79E-03	3.95E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.92E-02	7.26E-03	1.57E-02	1.72E-03	6.97E-03	3.91E-02	5.66E-03	1.67E-02	100%
M8-M7-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.06E-02	3.34E-03	7.91E-04	1.28E-03	1.96E-02	7.34E-03	6.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.51E-02	5.46E-03	1.09E-02	1.32E-03	4.79E-03	6.32E-02	1.10E-02	2.61E-02	100%
M8-M7-OD	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.06E-02	3.63E-03	8.71E-04	1.38E-03	1.94E-02	7.34E-03	6.02E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.53E-02	5.30E-03	1.19E-02	1.45E-03	5.21E-03	6.28E-02	1.10E-02	2.59E-02	100%
M8-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.91E-02	3.70E-02	1.47E-02	1.12E-02	2.44E-03	1.05E-03	6.92E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.24E-01	2.40E-03	1.11E-01	2.56E-02	4.29E-02	8.17E-03	1.70E-03	3.24E-03	100%
M8-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.81E-02	4.04E-02	1.64E-02	1.20E-02	2.41E-03	1.05E-03	6.76E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.31E-01	2.23E-03	1.18E-01	2.87E-02	4.47E-02	7.96E-03	1.70E-03	3.13E-03	100%
M8-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	1.66E-02	4.60E-03	6.01E-03	3.73E-03	1.29E-03	1.22E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.84E-02	5.34E-03	5.48E-02	7.66E-03	2.36E-02	1.29E-02	1.93E-03	5.49E-03	100%
M8-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.03E-02	1.70E-02	4.75E-03	6.11E-03	3.70E-03	1.29E-03	1.21E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.92E-02	5.21E-03	5.59E-02	7.92E-03	2.40E-02	1.28E-02	1.93E-03	5.44E-03	100%
M8-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	1.10E-02	2.52E-03	4.24E-03	5.04E-03	1.54E-03	1.75E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.79E-02	7.40E-03	3.61E-02	4.20E-03	1.60E-02	1.70E-02	2.31E-03	7.34E-03	100%
M8-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	1.11E-02	2.57E-03	4.28E-03	5.02E-03	1.54E-03	1.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.82E-02	7.32E-03	3.66E-02	4.28E-03	1.62E-02	1.69E-02	2.31E-03	7.31E-03	100%
M8-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	8.26E-03	1.74E-03	3.26E-03	6.58E-03	1.92E-03	2.33E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.49E-02	8.33E-03	2.66E-02	2.90E-03	1.19E-02	2.17E-02	2.88E-03	9.39E-03	100%
M8-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	8.33E-03	1.76E-03	3.28E-03	6.56E-03	1.92E-03	2.32E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.50E-02	8.28E-03	2.69E-02	2.93E-03	1.20E-02	2.16E-02	2.88E-03	9.37E-03	100%
M8-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	6.39E-03	1.33E-03	2.53E-03	8.56E-03	2.55E-03	3.00E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.53E-02	8.24E-03	2.06E-02	2.21E-03	9.20E-03	2.82E-02	3.81E-03	1.22E-02	100%
M8-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	6.43E-03	1.34E-03	2.55E-03	8.54E-03	2.55E-03	2.99E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.53E-02	8.21E-03	2.08E-02	2.23E-03	9.27E-03	2.81E-02	3.81E-03	1.22E-02	100%
M8-M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	4.91E-03	1.07E-03	1.92E-03	1.16E-02	3.79E-03	3.91E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.94E-02	7.16E-03	1.62E-02	1.79E-03	7.18E-03	3.89E-02	5.66E-03	1.66E-02	100%
M8-M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	4.94E-03	1.08E-03	1.93E-03	1.16E-02	3.79E-03	3.90E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.94E-02	7.14E-03	1.63E-02	1.80E-03	7.23E-03	3.89E-02	5.66E-03	1.66E-02	100%
M8-M7-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.06E-02	3.73E-03	8.99E-04	1.41E-03	1.93E-02	7.34E-03	5.99E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.53E-02	5.25E-03	1.22E-02	1.50E-03	5.35E-03	6.26E-02	1.10E-02	2.58E-02	100%
M8-M7-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.06E-02	3.75E-03	9.05E-04	1.42E-03	1.93E-02	7.34E-03	5.98E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.53E-02	5.24E-03	1.23E-02	1.51E-03	5.38E-03	6.26E-02	1.10E-02	2.58E-02	100%
M8-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.54E-02	1.33E-02	1.10E-02	3.13E-03	1.29E-03	9.20E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.67E-03	9.75E-02	2.22E-02	3.77E-02	1.02E-02	1.93E-03	4.15E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M8-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.09E-02	1.46E-02	3.93E-03	5.32E-03	4.47E-03	1.54E-03	1.46E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.54E-02	5.48E-03	4.88E-02	6.56E-03	2.11E-02	1.56E-02	2.31E-03	6.64E-03	100%
M8-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	9.94E-03	2.31E-03	3.82E-03	6.09E-03	1.92E-03	2.08E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.79E-02	7.10E-03	3.30E-02	3.85E-03	1.46E-02	2.07E-02	2.88E-03	8.92E-03	100%
M8-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.22E-02	7.39E-03	1.63E-03	2.88E-03	8.14E-03	2.55E-03	2.79E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.67E-02	7.47E-03	2.43E-02	2.72E-03	1.08E-02	2.74E-02	3.81E-03	1.18E-02	100%
M8-M6-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	5.57E-03	1.26E-03	2.15E-03	1.12E-02	3.79E-03	3.73E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.01E-02	6.70E-03	1.85E-02	2.11E-03	8.22E-03	3.82E-02	5.66E-03	1.63E-02	100%
M8-M7-M1	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.05E-02	4.18E-03	1.03E-03	1.57E-03	1.90E-02	7.34E-03	5.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.57E-02	4.99E-03	1.37E-02	1.72E-03	6.01E-03	6.19E-02	1.10E-02	2.55E-02	100%
M8-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.45E-02	3.50E-02	1.33E-02	1.08E-02	3.67E-03	1.54E-03	1.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.44E-03	9.65E-02	2.22E-02	3.72E-02	1.20E-02	2.31E-03	4.86E-03	100%
M8-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	1.41E-02	3.93E-03	5.08E-03	5.33E-03	1.92E-03	1.70E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.64E-02	4.91E-03	4.77E-02	6.56E-03	2.06E-02	1.88E-02	2.88E-03	7.96E-03	100%
M8-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	9.37E-03	2.31E-03	3.53E-03	7.49E-03	2.55E-03	2.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.00E-02	6.09E-03	3.18E-02	3.85E-03	1.40E-02	2.61E-02	3.81E-03	1.11E-02	100%
M8-M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.15E-02	6.74E-03	1.63E-03	2.55E-03	1.07E-02	3.79E-03	3.46E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.16E-02	5.87E-03	2.29E-02	2.72E-03	1.01E-02	3.70E-02	5.66E-03	1.57E-02	100%
M8-M7-M2	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.04E-02	4.94E-03	1.26E-03	1.84E-03	1.86E-02	7.34E-03	5.61E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.64E-02	4.55E-03	1.64E-02	2.11E-03	7.14E-03	6.09E-02	1.10E-02	2.50E-02	100%
M8-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.44E-02	3.45E-02	1.33E-02	1.06E-02	4.44E-03	1.92E-03	1.26E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.14E-01	2.10E-03	9.52E-02	2.22E-02	3.65E-02	1.46E-02	2.88E-03	5.88E-03	100%
M8-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	1.35E-02	3.93E-03	4.78E-03	6.65E-03	2.55E-03	2.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.82E-02	4.09E-03	4.63E-02	6.56E-03	1.98E-02	2.38E-02	3.81E-03	9.98E-03	100%
M8-M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	8.66E-03	2.31E-03	3.17E-03	9.98E-03	3.79E-03	3.10E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.47E-02	4.67E-03	3.00E-02	3.85E-03	1.31E-02	3.54E-02	5.66E-03	1.49E-02	100%
M8-M7-M3	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.02E-02	6.07E-03	1.63E-03	2.22E-03	1.79E-02	7.34E-03	5.30E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.76E-02	3.91E-03	2.03E-02	2.72E-03	8.80E-03	5.95E-02	1.10E-02	2.43E-02	100%
M8-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.42E-02	3.38E-02	1.33E-02	1.02E-02	5.66E-03	2.55E-03	1.55E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.15E-01	1.62E-03	9.33E-02	2.22E-02	3.56E-02	1.87E-02	3.81E-03	7.44E-03	100%
M8-M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	8.98E-02	1.27E-02	3.93E-03	4.38E-03	9.03E-03	3.79E-03	2.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.23E-02	2.96E-03	4.39E-02	6.56E-03	1.87E-02	3.25E-02	5.66E-03	1.34E-02	100%
M8-M7-M4	0.09	0.09	0.09	0.09	1.67E-01	2.05E-01	8.98E-02	7.95E-03	2.31E-03	2.82E-03	1.71E-02	7.34E-03	4.89E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	9.02E-02	2.98E-03	2.69E-02	3.85E-03	1.15E-02	5.74E-02	1.10E-02	2.32E-02	100%
M8-M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.37E-02	3.29E-02	1.33E-02	9.77E-03	7.91E-03	3.79E-03	2.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.18E-01	1.01E-03	9.02E-02	2.22E-02	3.40E-02	2.60E-02	5.66E-03	1.01E-02	100%
M8-M7-M5	0.09	0.09	0.09	0.09	1.67E-01	2.05E-01	8.87E-02	1.20E-02	3.93E-03	4.02E-03	1.60E-02	7.34E-03	4.31E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	9.68E-02	1.72E-03	3.99E-02	6.56E-03	1.67E-02	5.35E-02	1.10E-02	2.12E-02	100%
M8-M7-M6	0.09	0.09	0.09	0.09	1.67E-01	2.12E-01	8.27E-02	3.21E-02	1.33E-02	9.40E-03	1.45E-02	7.34E-03	3.59E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.30E-01	4.67E-04	8.50E-02	2.22E-02	3.14E-02	4.43E-02	1.10E-02	1.67E-02	100%
M9-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.78E-01	7.51E-02	2.63E-02	4.21E-03	1.10E-02	1.89E-03	2.73E-04	8.10E-04	100%
	0.054	2.16	0.039	2.175	1.50E+01	8.39E-02	1.32E-03	7.58E-02	4.21E-03	3.58E-02	5.50E-03	2.73E-04	2.62E-03	100%
M9-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.73E-02	4.54E-03	6.36E-03	2.36E-03	7.53E-04	8.03E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.10E-02	6.59E-03	5.96E-02	7.93E-03	2.58E-02	8.29E-03	1.21E-03	3.54E-03	100%
M9-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.76E-02	9.62E-03	8.98E-03	1.92E-03	7.53E-04	5.81E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.05E-01	3.56E-03	9.09E-02	1.68E-02	3.70E-02	6.69E-03	1.21E-03	2.74E-03	100%
M9-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.21E-02	1.28E-02	2.70E-03	5.07E-03	3.21E-03	8.80E-04	1.17E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.81E-02	8.56E-03	4.06E-02	4.51E-03	1.80E-02	1.04E-02	1.32E-03	4.55E-03	100%
M9-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	1.59E-02	3.95E-03	5.96E-03	2.83E-03	8.80E-04	9.73E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.45E-02	6.60E-03	5.17E-02	6.58E-03	2.26E-02	9.56E-03	1.32E-03	4.12E-03	100%
M9-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	9.91E-03	1.82E-03	4.04E-03	4.01E-03	9.92E-04	1.51E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.29E-02	1.01E-02	3.03E-02	3.04E-03	1.36E-02	1.25E-02	1.48E-03	5.50E-03	100%
M9-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	1.13E-02	2.31E-03	4.51E-03	3.68E-03	9.92E-04	1.34E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.55E-02	8.86E-03	3.59E-02	3.85E-03	1.60E-02	1.19E-02	1.48E-03	5.21E-03	100%
M9-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.32E-02	8.14E-03	1.37E-03	3.38E-03	4.89E-03	1.14E-03	1.88E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.09E-02	1.10E-02	2.41E-02	2.29E-03	1.09E-02	1.47E-02	1.70E-03	6.52E-03	100%
M9-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.30E-02	9.03E-03	1.64E-03	3.70E-03	4.61E-03	1.14E-03	1.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.22E-02	1.02E-02	2.75E-02	2.73E-03	1.24E-02	1.43E-02	1.70E-03	6.29E-03	100%
M9-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	6.85E-03	1.10E-03	2.88E-03	5.90E-03	1.33E-03	2.29E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.04E-02	1.15E-02	2.00E-02	1.84E-03	9.06E-03	1.75E-02	1.99E-03	7.74E-03	100%
M9-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.32E-02	7.47E-03	1.27E-03	3.10E-03	5.65E-03	1.33E-03	2.16E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.11E-02	1.10E-02	2.22E-02	2.11E-03	1.00E-02	1.70E-02	1.99E-03	7.53E-03	100%
M9-M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.32E-02	5.85E-03	9.21E-04	2.46E-03	7.16E-03	1.60E-03	2.78E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.13E-02	1.17E-02	1.69E-02	1.53E-03	7.67E-03	2.10E-02	2.39E-03	9.28E-03	100%
M9-M6-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.32E-02	6.31E-03	1.03E-03	2.64E-03	6.93E-03	1.60E-03	2.66E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.17E-02	1.13E-02	1.85E-02	1.72E-03	8.37E-03	2.06E-02	2.39E-03	9.09E-03	100%
M9-M7-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.39E-02	5.23E-03	7.91E-04	2.22E-03	9.36E-03	2.01E-03	3.67E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.58E-02	1.26E-02	1.45E-02	1.32E-03	6.60E-03	2.60E-02	3.01E-03	1.15E-02	100%
M9-M7-OD	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.38E-02	5.61E-03	8.71E-04	2.37E-03	9.15E-03	2.01E-03	3.57E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.09	1.5	0.141	1.449	8.46E-02	6.61E-02	1.24E-02	1.57E-02	1.45E-03	7.13E-03	2.57E-02	3.01E-03	1.13E-02	100%
M9-M8-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.41E-01	1.41E-01	7.41E-03	3.25E-03	2.08E-03	5.21E-02	3.01E-02	1.10E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.60E-01	1.80E-02	1.74E-02	3.25E-03	7.09E-03	1.07E-01	3.01E-02	3.84E-02	100%
M9-M8-OD	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.41E-01	7.92E-03	3.51E-03	2.21E-03	5.19E-02	3.01E-02	1.09E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.61E-01	1.77E-02	1.87E-02	3.51E-03	7.59E-03	1.07E-01	3.01E-02	3.83E-02	100%
M9-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.91E-02	3.75E-02	1.47E-02	1.14E-02	1.79E-03	7.53E-04	5.16E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.24E-01	2.62E-03	1.13E-01	2.56E-02	4.37E-02	5.97E-03	1.21E-03	2.38E-03	100%
M9-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.82E-02	4.09E-02	1.64E-02	1.23E-02	1.76E-03	7.53E-04	5.04E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.30E-01	2.44E-03	1.20E-01	2.87E-02	4.55E-02	5.80E-03	1.21E-03	2.29E-03	100%
M9-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	1.74E-02	4.60E-03	6.38E-03	2.70E-03	8.80E-04	9.10E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.77E-02	5.92E-03	5.67E-02	7.66E-03	2.45E-02	9.22E-03	1.32E-03	3.95E-03	100%
M9-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	1.77E-02	4.75E-03	6.48E-03	2.67E-03	8.80E-04	8.97E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.85E-02	5.78E-03	5.78E-02	7.92E-03	2.49E-02	9.15E-03	1.32E-03	3.91E-03	100%
M9-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.19E-02	2.52E-03	4.70E-03	3.57E-03	9.92E-04	1.29E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.67E-02	8.41E-03	3.81E-02	4.20E-03	1.70E-02	1.17E-02	1.48E-03	5.11E-03	100%
M9-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.22E-02	1.20E-02	2.57E-03	4.74E-03	3.55E-03	9.92E-04	1.28E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.69E-02	8.32E-03	3.86E-02	4.28E-03	1.72E-02	1.17E-02	1.48E-03	5.09E-03	100%
M9-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	9.36E-03	1.74E-03	3.81E-03	4.51E-03	1.14E-03	1.69E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.28E-02	9.94E-03	2.88E-02	2.90E-03	1.29E-02	1.41E-02	1.70E-03	6.21E-03	100%
M9-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	9.43E-03	1.76E-03	3.84E-03	4.49E-03	1.14E-03	1.68E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.29E-02	9.88E-03	2.90E-02	2.93E-03	1.30E-02	1.41E-02	1.70E-03	6.19E-03	100%
M9-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	7.70E-03	1.33E-03	3.19E-03	5.56E-03	1.33E-03	2.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.14E-02	1.08E-02	2.30E-02	2.21E-03	1.04E-02	1.69E-02	1.99E-03	7.46E-03	100%
M9-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	7.74E-03	1.34E-03	3.20E-03	5.55E-03	1.33E-03	2.11E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.15E-02	1.07E-02	2.32E-02	2.23E-03	1.05E-02	1.69E-02	1.99E-03	7.45E-03	100%
M9-M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	6.47E-03	1.07E-03	2.70E-03	6.85E-03	1.60E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.19E-02	1.12E-02	1.90E-02	1.79E-03	8.62E-03	2.04E-02	2.39E-03	9.02E-03	100%
M9-M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	6.51E-03	1.08E-03	2.71E-03	6.84E-03	1.60E-03	2.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.19E-02	1.12E-02	1.91E-02	1.80E-03	8.67E-03	2.04E-02	2.39E-03	9.01E-03	100%
M9-M7-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.38E-02	5.74E-03	8.99E-04	2.42E-03	9.08E-03	2.01E-03	3.53E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.62E-02	1.23E-02	1.61E-02	1.50E-03	7.31E-03	2.55E-02	3.01E-03	1.13E-02	100%
M9-M7-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.38E-02	5.77E-03	9.05E-04	2.43E-03	9.06E-03	2.01E-03	3.53E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.62E-02	1.23E-02	1.62E-02	1.51E-03	7.35E-03	2.55E-02	3.01E-03	1.13E-02	100%
M9-M8-PO1(OD)	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.41E-01	8.10E-03	3.60E-03	2.25E-03	5.19E-02	3.01E-02	1.09E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.61E-01	1.76E-02	1.91E-02	3.60E-03	7.75E-03	1.07E-01	3.01E-02	3.82E-02	100%
M9-M8-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.41E-01	8.13E-03	3.62E-03	2.26E-03	5.18E-02	3.01E-02	1.09E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.61E-01	1.76E-02	1.92E-02	3.62E-03	7.79E-03	1.07E-01	3.01E-02	3.82E-02	100%
M9-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.61E-02	1.33E-02	1.14E-02	2.22E-03	8.80E-04	6.69E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.03E-03	9.93E-02	2.22E-02	3.86E-02	7.21E-03	1.32E-03	2.95E-03	100%
M9-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.55E-02	3.93E-03	5.78E-03	3.11E-03	9.92E-04	1.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.43E-02	6.33E-03	5.10E-02	6.56E-03	2.22E-02	1.06E-02	1.48E-03	4.57E-03	100%
M9-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	1.11E-02	2.31E-03	4.38E-03	4.10E-03	1.14E-03	1.48E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.59E-02	8.57E-03	3.53E-02	3.85E-03	1.57E-02	1.34E-02	1.70E-03	5.85E-03	100%
M9-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	8.76E-03	1.63E-03	3.56E-03	5.20E-03	1.33E-03	1.94E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.30E-02	9.86E-03	2.70E-02	2.72E-03	1.21E-02	1.63E-02	1.99E-03	7.16E-03	100%
M9-M6-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	7.22E-03	1.26E-03	2.98E-03	6.53E-03	1.60E-03	2.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.28E-02	1.06E-02	2.16E-02	2.11E-03	9.77E-03	1.99E-02	2.39E-03	8.76E-03	100%
M9-M7-M1	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.37E-02	6.33E-03	1.03E-03	2.65E-03	8.78E-03	2.01E-03	3.38E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.68E-02	1.19E-02	1.80E-02	1.72E-03	8.14E-03	2.51E-02	3.01E-03	1.10E-02	100%
M9-M8-M1	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.41E-01	8.88E-03	4.01E-03	2.44E-03	5.16E-02	3.01E-02	1.08E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.62E-01	1.72E-02	2.10E-02	4.01E-03	8.51E-03	1.06E-01	3.01E-02	3.80E-02	100%
M9-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.59E-02	1.33E-02	1.13E-02	2.47E-03	9.92E-04	7.41E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.93E-03	9.88E-02	2.22E-02	3.83E-02	8.05E-03	1.48E-03	3.28E-03	100%
M9-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	1.53E-02	3.93E-03	5.66E-03	3.49E-03	1.14E-03	1.18E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.47E-02	6.11E-03	5.05E-02	6.56E-03	2.20E-02	1.20E-02	1.70E-03	5.14E-03	100%
M9-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.08E-02	2.31E-03	4.25E-03	4.66E-03	1.33E-03	1.66E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.66E-02	8.24E-03	3.48E-02	3.85E-03	1.55E-02	1.53E-02	1.99E-03	6.67E-03	100%
M9-M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	8.51E-03	1.63E-03	3.44E-03	6.05E-03	1.60E-03	2.22E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.46E-02	9.54E-03	2.64E-02	2.72E-03	1.18E-02	1.91E-02	2.39E-03	8.35E-03	100%
M9-M7-M2	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.35E-02	7.28E-03	1.26E-03	3.01E-03	8.33E-03	2.01E-03	3.16E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.78E-02	1.11E-02	2.12E-02	2.11E-03	9.54E-03	2.43E-02	3.01E-03	1.07E-02	100%
M9-M8-M2	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.40E-01	1.01E-02	4.67E-03	2.73E-03	5.12E-02	3.01E-02	1.06E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.36	2	0.405	1.955	2.20E-02	1.63E-01	1.65E-02	2.41E-02	4.67E-03	9.71E-03	1.06E-01	3.01E-02	3.77E-02	100%
M9-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.57E-02	1.33E-02	1.12E-02	2.80E-03	1.14E-03	8.31E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.81E-03	9.83E-02	2.22E-02	3.80E-02	9.12E-03	1.70E-03	3.71E-03	100%
M9-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.09E-02	1.50E-02	3.93E-03	5.53E-03	3.99E-03	1.33E-03	1.33E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.53E-02	5.85E-03	4.98E-02	6.56E-03	2.16E-02	1.38E-02	1.99E-03	5.89E-03	100%
M9-M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	1.06E-02	2.31E-03	4.13E-03	5.46E-03	1.60E-03	1.93E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.81E-02	7.98E-03	3.41E-02	3.85E-03	1.51E-02	1.80E-02	2.39E-03	7.80E-03	100%
M9-M7-M3	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.31E-02	8.65E-03	1.63E-03	3.51E-03	7.79E-03	2.01E-03	2.89E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.96E-02	1.01E-02	2.59E-02	2.72E-03	1.16E-02	2.34E-02	3.01E-03	1.02E-02	100%
M9-M8-M3	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.40E-01	1.18E-02	5.59E-03	3.12E-03	5.07E-02	3.01E-02	1.03E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.64E-01	1.56E-02	2.82E-02	5.59E-03	1.13E-02	1.05E-01	3.01E-02	3.74E-02	100%
M9-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.45E-02	3.54E-02	1.33E-02	1.11E-02	3.23E-03	1.33E-03	9.50E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.67E-03	9.75E-02	2.22E-02	3.77E-02	1.05E-02	1.99E-03	4.27E-03	100%
M9-M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	1.48E-02	3.93E-03	5.43E-03	4.72E-03	1.60E-03	1.56E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.66E-02	5.67E-03	4.91E-02	6.56E-03	2.13E-02	1.62E-02	2.39E-03	6.91E-03	100%
M9-M7-M4	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.25E-02	1.08E-02	2.31E-03	4.26E-03	7.10E-03	2.01E-03	2.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.30E-02	8.56E-03	3.37E-02	3.85E-03	1.49E-02	2.22E-02	3.01E-03	9.60E-03	100%
M9-M8-M4	0.36	0.36	0.405	0.315	2.21E-02	3.43E-01	1.39E-01	1.43E-02	6.96E-03	3.68E-03	5.02E-02	3.01E-02	1.01E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.67E-01	1.44E-02	3.42E-02	6.96E-03	1.36E-02	1.04E-01	3.01E-02	3.70E-02	100%
M9-M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.44E-02	3.52E-02	1.33E-02	1.10E-02	3.85E-03	1.60E-03	1.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.14E-01	2.62E-03	9.67E-02	2.22E-02	3.72E-02	1.25E-02	2.39E-03	5.04E-03	100%
M9-M7-M5	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.12E-02	1.53E-02	3.93E-03	5.67E-03	6.21E-03	2.01E-03	2.10E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.15E-02	6.27E-03	4.88E-02	6.56E-03	2.11E-02	2.02E-02	3.01E-03	8.59E-03	100%
M9-M8-M5	0.36	0.36	0.405	0.315	2.21E-02	3.44E-01	1.38E-01	1.83E-02	9.23E-03	4.56E-03	4.97E-02	3.01E-02	9.83E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.72E-01	1.27E-02	4.35E-02	9.23E-03	1.71E-02	1.03E-01	3.01E-02	3.65E-02	100%
M9-M7-M6	0.09	0.09	0.09	0.09	1.67E-01	2.11E-01	8.47E-02	3.62E-02	1.33E-02	1.14E-02	5.10E-03	2.01E-03	1.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	3.10E-03	9.72E-02	2.22E-02	3.75E-02	1.58E-02	3.01E-03	6.39E-03	100%
M9-M8-M6	0.36	0.36	0.405	0.315	2.21E-02	3.47E-01	1.36E-01	2.62E-02	1.37E-02	6.23E-03	4.92E-02	3.01E-02	9.58E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.82E-01	1.03E-02	5.99E-02	1.37E-02	2.31E-02	1.01E-01	3.01E-02	3.56E-02	100%
M9-M8-M7	0.36	0.36	0.405	0.315	2.21E-02	3.57E-01	1.30E-01	4.83E-02	2.66E-02	1.09E-02	4.89E-02	3.01E-02	9.40E-03	100%
	0.36	2	0.405	1.955	2.20E-02	2.09E-01	6.65E-03	9.76E-02	2.66E-02	3.55E-02	9.79E-02	3.01E-02	3.39E-02	100%
M10-PO1-FOX	0.054	0.108	0.039	0.123	1.50E+01	1.78E-01	7.51E-02	2.66E-02	4.21E-03	1.12E-02	1.48E-03	2.11E-04	6.37E-04	100%
	0.054	2.16	0.039	2.175	1.50E+01	8.38E-02	1.40E-03	7.67E-02	4.21E-03	3.62E-02	4.31E-03	2.11E-04	2.05E-03	100%
M10-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.77E-02	4.54E-03	6.57E-03	1.85E-03	5.72E-04	6.37E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.08E-02	6.80E-03	6.08E-02	7.93E-03	2.64E-02	6.45E-03	9.22E-04	2.77E-03	100%
M10-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.79E-02	9.62E-03	9.16E-03	1.48E-03	5.72E-04	4.56E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.05E-01	3.69E-03	9.20E-02	1.68E-02	3.76E-02	5.17E-03	9.22E-04	2.12E-03	100%
M10-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.21E-02	1.34E-02	2.70E-03	5.34E-03	2.50E-03	6.51E-04	9.23E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.78E-02	8.91E-03	4.19E-02	4.51E-03	1.87E-02	8.02E-03	9.73E-04	3.52E-03	100%
M10-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.64E-02	3.95E-03	6.22E-03	2.18E-03	6.51E-04	7.62E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.42E-02	6.89E-03	5.31E-02	6.58E-03	2.33E-02	7.31E-03	9.73E-04	3.17E-03	100%
M10-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.30E-02	1.06E-02	1.82E-03	4.37E-03	3.09E-03	7.10E-04	1.19E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.24E-02	1.06E-02	3.18E-02	3.04E-03	1.44E-02	9.45E-03	1.06E-03	4.20E-03	100%
M10-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	1.20E-02	2.31E-03	4.83E-03	2.81E-03	7.10E-04	1.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.50E-02	9.33E-03	3.74E-02	3.85E-03	1.68E-02	8.96E-03	1.06E-03	3.95E-03	100%
M10-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.34E-02	8.90E-03	1.37E-03	3.76E-03	3.72E-03	7.81E-04	1.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.02E-02	1.18E-02	2.57E-02	2.29E-03	1.17E-02	1.09E-02	1.17E-03	4.88E-03	100%
M10-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	9.79E-03	1.64E-03	4.08E-03	3.47E-03	7.81E-04	1.35E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.15E-02	1.09E-02	2.91E-02	2.73E-03	1.32E-02	1.05E-02	1.17E-03	4.68E-03	100%
M10-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.36E-02	7.73E-03	1.10E-03	3.31E-03	4.41E-03	8.67E-04	1.77E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.93E-02	1.25E-02	2.17E-02	1.84E-03	9.92E-03	1.26E-02	1.30E-03	5.63E-03	100%
M10-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.34E-02	8.36E-03	1.27E-03	3.55E-03	4.19E-03	8.67E-04	1.66E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.01E-02	1.20E-02	2.40E-02	2.11E-03	1.09E-02	1.22E-02	1.30E-03	5.45E-03	100%
M10-M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.36E-02	6.86E-03	9.21E-04	2.97E-03	5.22E-03	9.75E-04	2.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.96E-02	1.32E-02	1.88E-02	1.53E-03	8.62E-03	1.45E-02	1.46E-03	6.50E-03	100%
M10-M6-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.35E-02	7.35E-03	1.03E-03	3.16E-03	5.02E-03	9.75E-04	2.02E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.01E-02	1.28E-02	2.04E-02	1.72E-03	9.36E-03	1.41E-02	1.46E-03	6.33E-03	100%
M10-M7-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.45E-02	6.48E-03	7.91E-04	2.85E-03	6.57E-03	1.11E-03	2.73E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.32E-02	1.49E-02	1.66E-02	1.32E-03	7.63E-03	1.69E-02	1.67E-03	7.60E-03	100%
M10-M7-OD	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.44E-02	6.90E-03	8.71E-04	3.01E-03	6.38E-03	1.11E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.36E-02	1.46E-02	1.79E-02	1.45E-03	8.20E-03	1.66E-02	1.67E-03	7.44E-03	100%
M10-M8-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	8.49E-03	3.25E-03	2.62E-03	1.69E-02	7.63E-03	4.66E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.15E-01	2.92E-02	1.92E-02	3.25E-03	7.98E-03	3.78E-02	7.63E-03	1.51E-02	100%
M10-M8-OD	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	9.04E-03	3.51E-03	2.76E-03	1.68E-02	7.63E-03	4.57E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.16E-01	2.88E-02	2.05E-02	3.51E-03	8.51E-03	3.76E-02	7.63E-03	1.50E-02	100%
M10-M9-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.52E-01	6.15E-03	2.45E-03	1.85E-03	4.33E-02	2.32E-02	1.00E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.25E-02	1.41E-02	2.45E-03	5.82E-03	9.39E-02	2.32E-02	3.53E-02	100%
M10-M9-OD	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.52E-01	6.46E-03	2.60E-03	1.93E-03	4.31E-02	2.32E-02	9.96E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.23E-02	1.48E-02	2.60E-03	6.12E-03	9.36E-02	2.32E-02	3.52E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M10-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.91E-02	3.79E-02	1.47E-02	1.16E-02	1.38E-03	5.72E-04	4.03E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.24E-01	2.73E-03	1.14E-01	2.56E-02	4.42E-02	4.60E-03	9.22E-04	1.84E-03	100%
M10-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.82E-02	4.13E-02	1.64E-02	1.24E-02	1.36E-03	5.72E-04	3.93E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.30E-01	2.54E-03	1.21E-01	2.87E-02	4.60E-02	4.47E-03	9.22E-04	1.77E-03	100%
M10-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.06E-02	1.79E-02	4.60E-03	6.63E-03	2.07E-03	6.51E-04	7.11E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.74E-02	6.18E-03	5.80E-02	7.66E-03	2.52E-02	7.03E-03	9.73E-04	3.03E-03	100%
M10-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	1.82E-02	4.75E-03	6.73E-03	2.05E-03	6.51E-04	7.00E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.82E-02	6.04E-03	5.92E-02	7.92E-03	2.56E-02	6.97E-03	9.73E-04	3.00E-03	100%
M10-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.25E-02	2.52E-03	5.01E-03	2.72E-03	7.10E-04	1.00E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.62E-02	8.87E-03	3.97E-02	4.20E-03	1.77E-02	8.79E-03	1.06E-03	3.86E-03	100%
M10-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.27E-02	2.57E-03	5.05E-03	2.70E-03	7.10E-04	9.95E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.64E-02	8.77E-03	4.02E-02	4.28E-03	1.79E-02	8.75E-03	1.06E-03	3.85E-03	100%
M10-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.30E-02	1.01E-02	1.74E-03	4.19E-03	3.39E-03	7.81E-04	1.31E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.21E-02	1.06E-02	3.04E-02	2.90E-03	1.38E-02	1.04E-02	1.17E-03	4.61E-03	100%
M10-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.30E-02	1.02E-02	1.76E-03	4.22E-03	3.38E-03	7.81E-04	1.30E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.22E-02	1.06E-02	3.07E-02	2.93E-03	1.39E-02	1.04E-02	1.17E-03	4.59E-03	100%
M10-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.34E-02	8.59E-03	1.33E-03	3.63E-03	4.11E-03	8.67E-04	1.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.04E-02	1.18E-02	2.48E-02	2.21E-03	1.13E-02	1.21E-02	1.30E-03	5.39E-03	100%
M10-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	8.63E-03	1.34E-03	3.65E-03	4.10E-03	8.67E-04	1.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.05E-02	1.17E-02	2.50E-02	2.23E-03	1.14E-02	1.20E-02	1.30E-03	5.38E-03	100%
M10-M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.35E-02	7.52E-03	1.07E-03	3.22E-03	4.95E-03	9.75E-04	1.99E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.03E-02	1.26E-02	2.10E-02	1.79E-03	9.61E-03	1.40E-02	1.46E-03	6.28E-03	100%
M10-M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.35E-02	7.55E-03	1.08E-03	3.24E-03	4.94E-03	9.75E-04	1.98E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.04E-02	1.26E-02	2.11E-02	1.80E-03	9.67E-03	1.40E-02	1.46E-03	6.27E-03	100%
M10-M7-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.44E-02	7.04E-03	8.99E-04	3.07E-03	6.31E-03	1.11E-03	2.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.37E-02	1.45E-02	1.83E-02	1.50E-03	8.40E-03	1.64E-02	1.67E-03	7.39E-03	100%
M10-M7-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.44E-02	7.07E-03	9.05E-04	3.08E-03	6.30E-03	1.11E-03	2.59E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.37E-02	1.44E-02	1.84E-02	1.51E-03	8.44E-03	1.64E-02	1.67E-03	7.38E-03	100%
M10-M8-PO1(OD)	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	9.22E-03	3.60E-03	2.81E-03	1.67E-02	7.63E-03	4.54E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.16E-01	2.87E-02	2.10E-02	3.60E-03	8.70E-03	3.75E-02	7.63E-03	1.49E-02	100%
M10-M8-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	9.26E-03	3.62E-03	2.82E-03	1.67E-02	7.63E-03	4.54E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.16E-01	2.87E-02	2.11E-02	3.62E-03	8.73E-03	3.75E-02	7.63E-03	1.49E-02	100%
M10-M9-PO1(OD)	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.52E-01	6.57E-03	2.65E-03	1.96E-03	4.31E-02	2.32E-02	9.93E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.22E-02	1.51E-02	2.65E-03	6.22E-03	9.35E-02	2.32E-02	3.52E-02	100%
M10-M9-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.52E-01	6.59E-03	2.66E-03	1.96E-03	4.31E-02	2.32E-02	9.92E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.22E-02	1.51E-02	2.66E-03	6.24E-03	9.35E-02	2.32E-02	3.52E-02	100%
M10-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.65E-02	1.33E-02	1.16E-02	1.68E-03	6.51E-04	5.14E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.12E-01	3.19E-03	1.01E-01	2.22E-02	3.92E-02	5.44E-03	9.73E-04	2.23E-03	100%
M10-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.61E-02	3.93E-03	6.08E-03	2.34E-03	7.10E-04	8.13E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.39E-02	6.70E-03	5.26E-02	6.56E-03	2.30E-02	7.92E-03	1.06E-03	3.43E-03	100%
M10-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	1.18E-02	2.31E-03	4.76E-03	3.05E-03	7.81E-04	1.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.52E-02	9.17E-03	3.71E-02	3.85E-03	1.66E-02	9.77E-03	1.17E-03	4.30E-03	100%
M10-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	9.66E-03	1.63E-03	4.01E-03	3.80E-03	8.67E-04	1.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.20E-02	1.08E-02	2.89E-02	2.72E-03	1.31E-02	1.16E-02	1.30E-03	5.13E-03	100%
M10-M6-M1	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	8.29E-03	1.26E-03	3.51E-03	4.66E-03	9.75E-04	1.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.13E-02	1.20E-02	2.38E-02	2.11E-03	1.08E-02	1.36E-02	1.46E-03	6.05E-03	100%
M10-M7-M1	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.42E-02	7.67E-03	1.03E-03	3.32E-03	6.04E-03	1.11E-03	2.46E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.43E-02	1.40E-02	2.03E-02	1.72E-03	9.29E-03	1.60E-02	1.67E-03	7.18E-03	100%
M10-M8-M1	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	1.00E-02	4.01E-03	3.02E-03	1.65E-02	7.63E-03	4.43E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.17E-01	2.82E-02	2.30E-02	4.01E-03	9.51E-03	3.72E-02	7.63E-03	1.48E-02	100%
M10-M9-M1	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	7.02E-03	2.86E-03	2.08E-03	4.28E-02	2.32E-02	9.82E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.20E-02	1.62E-02	2.86E-03	6.65E-03	9.32E-02	2.32E-02	3.50E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M10-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.64E-02	1.33E-02	1.16E-02	1.82E-03	7.10E-04	5.55E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.14E-03	1.00E-01	2.22E-02	3.91E-02	5.91E-03	1.06E-03	2.42E-03	100%
M10-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.60E-02	3.93E-03	6.02E-03	2.55E-03	7.81E-04	8.82E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.41E-02	6.59E-03	5.23E-02	6.56E-03	2.29E-02	8.64E-03	1.17E-03	3.74E-03	100%
M10-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	1.17E-02	2.31E-03	4.70E-03	3.35E-03	8.67E-04	1.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.57E-02	9.05E-03	3.69E-02	3.85E-03	1.65E-02	1.08E-02	1.30E-03	4.73E-03	100%
M10-M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	9.61E-03	1.63E-03	3.99E-03	4.25E-03	9.75E-04	1.64E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.31E-02	1.08E-02	2.87E-02	2.72E-03	1.30E-02	1.29E-02	1.46E-03	5.71E-03	100%
M10-M7-M2	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.40E-02	8.68E-03	1.26E-03	3.71E-03	5.64E-03	1.11E-03	2.26E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.54E-02	1.32E-02	2.37E-02	2.11E-03	1.08E-02	1.54E-02	1.67E-03	6.87E-03	100%
M10-M8-M2	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.50E-01	1.13E-02	4.67E-03	3.34E-03	1.62E-02	7.63E-03	4.27E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.18E-01	2.74E-02	2.63E-02	4.67E-03	1.08E-02	3.69E-02	7.63E-03	1.46E-02	100%
M10-M9-M2	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	7.68E-03	3.19E-03	2.25E-03	4.25E-02	2.32E-02	9.66E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.54E-01	2.17E-02	1.78E-02	3.19E-03	7.29E-03	9.27E-02	2.32E-02	3.48E-02	100%
M10-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.63E-02	1.33E-02	1.15E-02	1.99E-03	7.81E-04	6.05E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.08E-03	1.00E-01	2.22E-02	3.89E-02	6.47E-03	1.17E-03	2.65E-03	100%
M10-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	1.59E-02	3.93E-03	5.97E-03	2.80E-03	8.67E-04	9.68E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.46E-02	6.50E-03	5.21E-02	6.56E-03	2.27E-02	9.53E-03	1.30E-03	4.11E-03	100%
M10-M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.17E-02	2.31E-03	4.69E-03	3.75E-03	9.75E-04	1.39E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.68E-02	9.10E-03	3.66E-02	3.85E-03	1.64E-02	1.20E-02	1.46E-03	5.26E-03	100%
M10-M7-M3	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.36E-02	1.01E-02	1.63E-03	4.24E-03	5.16E-03	1.11E-03	2.02E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.73E-02	1.20E-02	2.86E-02	2.72E-03	1.30E-02	1.47E-02	1.67E-03	6.51E-03	100%
M10-M8-M3	0.36	0.36	0.405	0.315	2.21E-02	3.29E-01	1.50E-01	1.31E-02	5.59E-03	3.76E-03	1.58E-02	7.63E-03	4.10E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.20E-01	2.63E-02	3.07E-02	5.59E-03	1.26E-02	3.65E-02	7.63E-03	1.44E-02	100%
M10-M9-M3	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	8.50E-03	3.59E-03	2.46E-03	4.22E-02	2.32E-02	9.48E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.54E-01	2.12E-02	1.98E-02	3.59E-03	8.08E-03	9.22E-02	2.32E-02	3.45E-02	100%
M10-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.62E-02	1.33E-02	1.15E-02	2.20E-03	8.67E-04	6.67E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.04E-03	9.98E-02	2.22E-02	3.88E-02	7.14E-03	1.30E-03	2.92E-03	100%
M10-M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.09E-02	1.59E-02	3.93E-03	5.98E-03	3.16E-03	9.75E-04	1.09E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.56E-02	6.57E-03	5.18E-02	6.56E-03	2.26E-02	1.06E-02	1.46E-03	4.59E-03	100%
M10-M7-M4	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.29E-02	1.23E-02	2.31E-03	5.01E-03	4.59E-03	1.11E-03	1.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.10E-02	1.02E-02	3.67E-02	3.85E-03	1.64E-02	1.37E-02	1.67E-03	6.03E-03	100%
M10-M8-M4	0.36	0.36	0.405	0.315	2.21E-02	3.29E-01	1.49E-01	1.57E-02	6.96E-03	4.36E-03	1.55E-02	7.63E-03	3.92E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.23E-01	2.48E-02	3.71E-02	6.96E-03	1.51E-02	3.61E-02	7.63E-03	1.42E-02	100%
M10-M9-M4	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	9.52E-03	4.11E-03	2.71E-03	4.18E-02	2.32E-02	9.27E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.55E-01	2.06E-02	2.22E-02	4.11E-03	9.07E-03	9.16E-02	2.32E-02	3.42E-02	100%
M10-M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.45E-02	3.63E-02	1.33E-02	1.15E-02	2.48E-03	9.75E-04	7.53E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.14E-01	3.14E-03	9.95E-02	2.22E-02	3.86E-02	7.99E-03	1.46E-03	3.27E-03	100%
M10-M7-M5	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.15E-02	1.68E-02	3.93E-03	6.43E-03	3.89E-03	1.11E-03	1.39E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.97E-02	7.65E-03	5.22E-02	6.56E-03	2.28E-02	1.23E-02	1.67E-03	5.30E-03	100%
M10-M8-M5	0.36	0.36	0.405	0.315	2.21E-02	3.30E-01	1.48E-01	1.98E-02	9.23E-03	5.29E-03	1.51E-02	7.63E-03	3.73E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.28E-01	2.28E-02	4.70E-02	9.23E-03	1.89E-02	3.56E-02	7.63E-03	1.40E-02	100%
M10-M9-M5	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	1.09E-02	4.81E-03	3.02E-03	4.13E-02	2.32E-02	9.03E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.56E-01	1.99E-02	2.55E-02	4.81E-03	1.04E-02	9.09E-02	2.32E-02	3.39E-02	100%
M10-M7-M6	0.09	0.09	0.09	0.09	1.67E-01	2.11E-01	8.50E-02	3.77E-02	1.33E-02	1.22E-02	3.05E-03	1.11E-03	9.67E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.18E-01	3.93E-03	1.01E-01	2.22E-02	3.93E-02	9.33E-03	1.67E-03	3.83E-03	100%
M10-M8-M6	0.36	0.36	0.405	0.315	2.21E-02	3.33E-01	1.45E-01	2.78E-02	1.37E-02	7.06E-03	1.47E-02	7.63E-03	3.55E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.39E-01	1.98E-02	6.45E-02	1.37E-02	2.54E-02	3.49E-02	7.63E-03	1.36E-02	100%
M10-M9-M6	0.36	0.36	0.405	0.315	2.21E-02	3.54E-01	1.50E-01	1.27E-02	5.79E-03	3.44E-03	4.07E-02	2.32E-02	8.76E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.58E-01	1.88E-02	3.00E-02	5.79E-03	1.21E-02	9.02E-02	2.32E-02	3.35E-02	100%
M10-M8-M7	0.36	0.36	0.405	0.315	2.21E-02	3.43E-01	1.39E-01	5.03E-02	2.66E-02	1.19E-02	1.44E-02	7.63E-03	3.38E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.68E-01	1.52E-02	1.04E-01	2.66E-02	3.88E-02	3.35E-02	7.63E-03	1.29E-02	100%
M10-M9-M7	0.36	0.36	0.405	0.315	2.21E-02	3.54E-01	1.49E-01	1.53E-02	7.28E-03	4.01E-03	4.01E-02	2.32E-02	8.45E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.61E-01	1.74E-02	3.65E-02	7.28E-03	1.46E-02	8.93E-02	2.32E-02	3.30E-02	100%
M10-M9-M8	0.36	0.36	0.405	0.315	2.21E-02	3.67E-01	1.40E-01	4.84E-02	2.66E-02	1.09E-02	3.85E-02	2.32E-02	7.66E-03	100%
	0.36	2	0.405	1.955	2.20E-02	2.01E-01	8.81E-03	9.95E-02	2.66E-02	3.65E-02	8.41E-02	2.32E-02	3.04E-02	100%

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12.14.3.3 M1MxMz process in CLN55LP 1.2V/2.5V, no My/Mr, x=2~7, z=8~9

12.14.3.3.1 Structure A 25 ℃

Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
PO1-FOX	0.05	0.11	0.054	0.108	1.47E+01	2.05E-01	8.84E-02	2.79E-02	5.83E-03	1.10E-02	100%
	0.05	2.16	0.054	2.16	1.47E+01	8.79E-02	1.73E-03	8.44E-02	5.83E-03	3.93E-02	100%
M1-FOX	0.08	0.08	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.93E-02	4.54E-03	7.40E-03	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	8.04E-02	7.20E-03	6.60E-02	7.93E-03	2.91E-02	100%
M1-OD	0.08	0.08	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.93E-02	9.62E-03	9.85E-03	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.04E-01	3.94E-03	9.64E-02	1.68E-02	3.98E-02	100%
M1-PO1(OD)	0.08	0.08	0.0875	0.0745	1.89E-01	2.38E-01	9.92E-02	3.92E-02	1.47E-02	1.23E-02	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.24E-01	2.91E-03	1.18E-01	2.56E-02	4.62E-02	100%
M1-PO1(FOX)	0.08	0.08	0.0875	0.0745	1.89E-01	2.39E-01	9.82E-02	4.26E-02	1.64E-02	1.31E-02	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.30E-01	2.72E-03	1.25E-01	2.87E-02	4.80E-02	100%
M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.56E-02	2.70E-03	6.43E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.72E-02	9.54E-03	4.81E-02	4.51E-03	2.18E-02	100%
M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	1.83E-02	3.95E-03	7.19E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.37E-02	7.40E-03	5.89E-02	6.58E-03	2.62E-02	100%
M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	1.97E-02	4.60E-03	7.56E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.70E-02	6.65E-03	6.37E-02	7.66E-03	2.80E-02	100%
M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	2.01E-02	4.75E-03	7.65E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.78E-02	6.49E-03	6.48E-02	7.92E-03	2.84E-02	100%
M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.81E-02	1.33E-02	1.24E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.12E-01	3.45E-03	1.05E-01	2.22E-02	4.15E-02	100%
M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.32E-02	1.32E-02	1.82E-03	5.67E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.16E-02	1.15E-02	3.86E-02	3.04E-03	1.78E-02	100%
M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.27E-02	1.44E-02	2.31E-03	6.04E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.43E-02	1.01E-02	4.41E-02	3.85E-03	2.01E-02	100%
M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	1.49E-02	2.52E-03	6.19E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.55E-02	9.61E-03	4.63E-02	4.20E-03	2.10E-02	100%
M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	1.50E-02	2.57E-03	6.22E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.58E-02	9.51E-03	4.68E-02	4.28E-03	2.12E-02	100%
M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	1.82E-02	3.93E-03	7.11E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.34E-02	7.27E-03	5.88E-02	6.56E-03	2.61E-02	100%
M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.81E-02	1.33E-02	1.24E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.12E-01	3.44E-03	1.05E-01	2.22E-02	4.16E-02	100%
M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.37E-02	1.19E-02	1.37E-03	5.28E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.91E-02	1.30E-02	3.32E-02	2.29E-03	1.55E-02	100%
M4-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.34E-02	1.27E-02	1.64E-03	5.51E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.05E-02	1.20E-02	3.65E-02	2.73E-03	1.69E-02	100%
M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	1.29E-02	1.74E-03	5.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.11E-02	1.17E-02	3.78E-02	2.90E-03	1.74E-02	100%
M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.32E-02	1.30E-02	1.76E-03	5.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.12E-02	1.16E-02	3.80E-02	2.93E-03	1.75E-02	100%
M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.27E-02	1.44E-02	2.31E-03	6.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.44E-02	1.01E-02	4.42E-02	3.85E-03	2.02E-02	100%
M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	1.82E-02	3.93E-03	7.14E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.35E-02	7.26E-03	5.90E-02	6.56E-03	2.62E-02	100%
M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.81E-02	1.33E-02	1.24E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.12E-01	3.43E-03	1.05E-01	2.22E-02	4.16E-02	100%
M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.40E-02	1.12E-02	1.10E-03	5.04E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.80E-02	1.41E-02	2.98E-02	1.84E-03	1.40E-02	100%
M5-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.38E-02	1.17E-02	1.27E-03	5.21E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.88E-02	1.34E-02	3.20E-02	2.11E-03	1.49E-02	100%
M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.37E-02	1.19E-02	1.33E-03	5.27E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.92E-02	1.32E-02	3.28E-02	2.21E-03	1.53E-02	100%
M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.37E-02	1.19E-02	1.34E-03	5.28E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.92E-02	1.31E-02	3.30E-02	2.23E-03	1.54E-02	100%
M5-M1	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	1.28E-02	1.63E-03	5.56E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.09E-02	1.20E-02	3.68E-02	2.72E-03	1.70E-02	100%
M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	1.45E-02	2.31E-03	6.10E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.47E-02	1.01E-02	4.45E-02	3.85E-03	2.03E-02	100%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	1.83E-02	3.93E-03	7.19E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.38E-02	7.28E-03	5.93E-02	6.56E-03	2.64E-02	100%
M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.82E-02	1.33E-02	1.25E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.45E-03	1.06E-01	2.22E-02	4.17E-02	100%
M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.42E-02	1.08E-02	9.21E-04	4.93E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.79E-02	1.52E-02	2.75E-02	1.53E-03	1.30E-02	100%
M6-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.40E-02	1.12E-02	1.03E-03	5.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.85E-02	1.47E-02	2.91E-02	1.72E-03	1.37E-02	100%
M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.39E-02	1.13E-02	1.07E-03	5.11E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.87E-02	1.45E-02	2.97E-02	1.79E-03	1.39E-02	100%
M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.39E-02	1.13E-02	1.08E-03	5.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.87E-02	1.45E-02	2.98E-02	1.80E-03	1.40E-02	100%
M6-M1	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.37E-02	1.19E-02	1.26E-03	5.33E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.97E-02	1.37E-02	3.23E-02	2.11E-03	1.51E-02	100%
M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.33E-02	1.30E-02	1.63E-03	5.69E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.18E-02	1.23E-02	3.72E-02	2.72E-03	1.72E-02	100%
M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	1.48E-02	2.31E-03	6.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.56E-02	1.04E-02	4.49E-02	3.85E-03	2.05E-02	100%
M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.86E-02	3.93E-03	7.33E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.47E-02	7.51E-03	5.96E-02	6.56E-03	2.65E-02	100%
M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.85E-02	1.33E-02	1.26E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.64E-03	1.06E-01	2.22E-02	4.19E-02	100%
M7-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.53E-02	1.11E-02	7.91E-04	5.16E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.09E-02	1.75E-02	2.59E-02	1.32E-03	1.23E-02	100%
M7-OD	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.51E-02	1.15E-02	8.71E-04	5.29E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.14E-02	1.71E-02	2.71E-02	1.45E-03	1.28E-02	100%
M7-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.51E-02	1.16E-02	8.99E-04	5.34E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.15E-02	1.70E-02	2.76E-02	1.50E-03	1.30E-02	100%
M7-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.51E-02	1.16E-02	9.05E-04	5.35E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.15E-02	1.69E-02	2.77E-02	1.51E-03	1.31E-02	100%
M7-M1	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.49E-02	1.21E-02	1.03E-03	5.53E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.22E-02	1.63E-02	2.96E-02	1.72E-03	1.39E-02	100%
M7-M2	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.45E-02	1.29E-02	1.26E-03	5.83E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.35E-02	1.53E-02	3.29E-02	2.11E-03	1.54E-02	100%
M7-M3	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.41E-02	1.41E-02	1.63E-03	6.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.56E-02	1.39E-02	3.78E-02	2.72E-03	1.76E-02	100%
M7-M4	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.33E-02	1.60E-02	2.31E-03	6.86E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.95E-02	1.18E-02	4.58E-02	3.85E-03	2.10E-02	100%
M7-M5	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.17E-02	2.01E-02	3.93E-03	8.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.86E-02	8.85E-03	6.09E-02	6.56E-03	2.72E-02	100%
M7-M6	0.09	0.09	0.09	0.09	1.67E-01	2.11E-01	8.51E-02	4.04E-02	1.33E-02	1.36E-02	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.17E-01	4.58E-03	1.08E-01	2.22E-02	4.30E-02	100%
M8-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.50E-02	3.25E-03	5.89E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.05E-01	3.83E-02	2.88E-02	3.25E-03	1.28E-02	100%
M8-OD	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.56E-02	3.51E-03	6.05E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.06E-01	3.78E-02	3.03E-02	3.51E-03	1.34E-02	100%
M8-PO1(OD)	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.58E-02	3.60E-03	6.10E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.06E-01	3.77E-02	3.08E-02	3.60E-03	1.36E-02	100%
M8-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.58E-02	3.62E-03	6.11E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.06E-01	3.76E-02	3.09E-02	3.62E-03	1.36E-02	100%
M8-M1	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.55E-01	1.67E-02	4.01E-03	6.33E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.07E-01	3.70E-02	3.30E-02	4.01E-03	1.45E-02	100%
M8-M2	0.36	0.36	0.405	0.315	2.21E-02	3.26E-01	1.54E-01	1.80E-02	4.67E-03	6.68E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.08E-01	3.59E-02	3.65E-02	4.67E-03	1.59E-02	100%
M8-M3	0.36	0.36	0.405	0.315	2.21E-02	3.27E-01	1.53E-01	1.99E-02	5.59E-03	7.15E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.10E-01	3.46E-02	4.12E-02	5.59E-03	1.78E-02	100%
M8-M4	0.36	0.36	0.405	0.315	2.21E-02	3.27E-01	1.52E-01	2.26E-02	6.96E-03	7.79E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.14E-01	3.28E-02	4.80E-02	6.96E-03	2.05E-02	100%
M8-M5	0.36	0.36	0.405	0.315	2.21E-02	3.29E-01	1.51E-01	2.68E-02	9.23E-03	8.80E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.19E-01	3.04E-02	5.84E-02	9.23E-03	2.46E-02	100%
M8-M6	0.36	0.36	0.405	0.315	2.21E-02	3.31E-01	1.48E-01	3.51E-02	1.37E-02	1.07E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.30E-01	2.69E-02	7.66E-02	1.37E-02	3.14E-02	100%
M8-M7	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.42E-01	5.79E-02	2.66E-02	1.57E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.60E-01	2.15E-02	1.17E-01	2.66E-02	4.53E-02	100%
M9-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.32E-02	2.45E-03	5.36E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.09E-01	4.25E-02	2.39E-02	2.45E-03	1.07E-02	100%
M9-OD	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.35E-02	2.60E-03	5.46E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.09E-01	4.22E-02	2.47E-02	2.60E-03	1.11E-02	100%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M9-PO1(OD)	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.36E-02	2.65E-03	5.50E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.09E-01	4.21E-02	2.50E-02	2.65E-03	1.12E-02	100%
M9-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.37E-02	2.66E-03	5.50E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.09E-01	4.21E-02	2.51E-02	2.66E-03	1.12E-02	100%
M9-M1	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.41E-02	2.86E-03	5.64E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.10E-01	4.17E-02	2.62E-02	2.86E-03	1.17E-02	100%
M9-M2	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.64E-01	1.49E-02	3.19E-03	5.85E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.10E-01	4.11E-02	2.80E-02	3.19E-03	1.24E-02	100%
M9-M3	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.63E-01	1.58E-02	3.59E-03	6.09E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.11E-01	4.03E-02	3.02E-02	3.59E-03	1.33E-02	100%
M9-M4	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.63E-01	1.69E-02	4.11E-03	6.38E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.12E-01	3.94E-02	3.29E-02	4.11E-03	1.44E-02	100%
M9-M5	0.36	0.36	0.405	0.315	2.21E-02	3.43E-01	1.62E-01	1.83E-02	4.81E-03	6.74E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.13E-01	3.83E-02	3.65E-02	4.81E-03	1.59E-02	100%
M9-M6	0.36	0.36	0.405	0.315	2.21E-02	3.43E-01	1.61E-01	2.02E-02	5.79E-03	7.20E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.15E-01	3.68E-02	4.14E-02	5.79E-03	1.78E-02	100%
M9-M7	0.36	0.36	0.405	0.315	2.21E-02	3.44E-01	1.60E-01	2.30E-02	7.28E-03	7.84E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.18E-01	3.48E-02	4.86E-02	7.28E-03	2.06E-02	100%
M9-M8	0.36	0.36	0.405	0.315	2.21E-02	3.57E-01	1.50E-01	5.71E-02	2.66E-02	1.53E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.63E-01	2.32E-02	1.16E-01	2.66E-02	4.49E-02	100%
M10-FOX	2.7	1.8	2.86	1.64	2.10E-02	1.78E-01	7.60E-02	2.63E-02	1.55E-02	5.39E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.07E-02	2.16E-02	4.74E-02	1.55E-02	1.60E-02	100%
M10-OD	2.7	1.8	2.86	1.64	2.10E-02	1.79E-01	7.57E-02	2.72E-02	1.62E-02	5.52E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.17E-02	2.12E-02	4.92E-02	1.62E-02	1.65E-02	100%
M10-PO1(OD)	2.7	1.8	2.86	1.64	2.10E-02	1.79E-01	7.56E-02	2.76E-02	1.64E-02	5.56E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.20E-02	2.11E-02	4.98E-02	1.64E-02	1.67E-02	100%
M10-PO1(FOX)	2.7	1.8	2.86	1.64	2.10E-02	1.79E-01	7.56E-02	2.76E-02	1.65E-02	5.57E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.21E-02	2.11E-02	4.99E-02	1.65E-02	1.67E-02	100%
M10-M1	2.7	1.8	2.86	1.64	2.10E-02	1.79E-01	7.51E-02	2.89E-02	1.74E-02	5.74E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.34E-02	2.06E-02	5.23E-02	1.74E-02	1.74E-02	100%
M10-M2	2.7	1.8	2.86	1.64	2.10E-02	1.80E-01	7.45E-02	3.09E-02	1.89E-02	6.02E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.55E-02	1.99E-02	5.58E-02	1.89E-02	1.85E-02	100%
M10-M3	2.7	1.8	2.86	1.64	2.10E-02	1.81E-01	7.38E-02	3.33E-02	2.06E-02	6.34E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	9.80E-02	1.91E-02	5.99E-02	2.06E-02	1.96E-02	100%
M10-M4	2.7	1.8	2.86	1.64	2.10E-02	1.82E-01	7.30E-02	3.62E-02	2.27E-02	6.74E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.01E-01	1.82E-02	6.47E-02	2.27E-02	2.10E-02	100%
M10-M5	2.7	1.8	2.86	1.64	2.10E-02	1.84E-01	7.20E-02	3.96E-02	2.52E-02	7.23E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.05E-01	1.72E-02	7.03E-02	2.52E-02	2.26E-02	100%
M10-M6	2.7	1.8	2.86	1.64	2.10E-02	1.86E-01	7.09E-02	4.40E-02	2.83E-02	7.85E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.09E-01	1.61E-02	7.72E-02	2.83E-02	2.44E-02	100%
M10-M7	2.7	1.8	2.86	1.64	2.10E-02	1.89E-01	6.95E-02	4.97E-02	3.24E-02	8.65E-03	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.15E-01	1.49E-02	8.56E-02	3.24E-02	2.66E-02	100%
M10-M8	2.7	1.8	2.86	1.64	2.10E-02	2.07E-01	6.36E-02	7.99E-02	5.41E-02	1.29E-02	100%
	2.7	7.2	2.86	7.04	2.10E-02	1.47E-01	1.08E-02	1.26E-01	5.41E-02	3.58E-02	100%
M10-M9	2.7	1.8	2.86	1.64	2.10E-02	3.25E-01	5.13E-02	2.23E-01	1.65E-01	2.91E-02	100%
	2.7	7.2	2.86	7.04	2.10E-02	2.90E-01	5.78E-03	2.79E-01	1.65E-01	5.71E-02	100%

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12.14.3.3.2 Structure B 25 ℃

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M1-PO1-FOX	0.054	0.108	0.054	0.108	1.47E+01	2.14E-01	7.87E-02	1.83E-02	5.83E-03	6.21E-03	3.87E-02	4.37E-03	1.72E-02	100%
	0.054	2.16	0.054	2.16	1.47E+01	1.31E-01	1.41E-06	4.42E-02	5.83E-03	1.92E-02	8.69E-02	4.37E-03	4.12E-02	100%
M2-PO1-FOX	0.054	0.108	0.054	0.108	1.47E+01	2.06E-01	8.63E-02	2.07E-02	5.83E-03	7.41E-03	1.29E-02	3.42E-03	4.76E-03	100%
	0.054	2.16	0.054	2.16	1.47E+01	9.86E-02	7.23E-05	6.05E-02	5.83E-03	2.74E-02	3.79E-02	3.42E-03	1.73E-02	100%
M2-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.79E-02	1.17E-02	4.54E-03	3.59E-03	3.14E-02	1.77E-02	6.84E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.34E-01	5.55E-04	3.81E-02	7.93E-03	1.51E-02	9.45E-02	2.86E-02	3.29E-02	100%
M2-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.41E-01	9.50E-02	2.17E-02	9.62E-03	6.06E-03	2.97E-02	1.77E-02	5.95E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.50E-01	7.82E-05	6.47E-02	1.68E-02	2.39E-02	8.49E-02	2.86E-02	2.82E-02	100%
M2-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.45E-01	9.20E-02	3.14E-02	1.47E-02	8.38E-03	2.91E-02	1.77E-02	5.70E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.65E-01	2.21E-05	8.53E-02	2.56E-02	2.98E-02	8.01E-02	2.86E-02	2.57E-02	100%
M2-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.46E-01	9.11E-02	3.48E-02	1.64E-02	9.18E-03	2.91E-02	1.77E-02	5.66E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.71E-01	1.61E-05	9.17E-02	2.87E-02	3.15E-02	7.89E-02	2.86E-02	2.52E-02	100%
M3-PO1-FOX	0.054	0.108	0.054	0.108	1.47E+01	2.05E-01	8.75E-02	2.25E-02	5.83E-03	8.31E-03	7.72E-03	1.85E-03	2.93E-03	100%
	0.054	2.16	0.054	2.16	1.47E+01	9.24E-02	2.94E-04	6.82E-02	5.83E-03	3.12E-02	2.36E-02	1.85E-03	1.09E-02	100%
M3-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.32E-01	1.04E-01	1.32E-02	4.54E-03	4.32E-03	1.14E-02	5.25E-03	3.08E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	9.44E-02	2.07E-03	4.80E-02	7.93E-03	2.00E-02	4.23E-02	8.46E-03	1.69E-02	100%
M3-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.35E-01	1.01E-01	2.33E-02	9.62E-03	6.86E-03	1.02E-02	5.25E-03	2.49E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.15E-01	6.81E-04	7.75E-02	1.68E-02	3.03E-02	3.60E-02	8.46E-03	1.38E-02	100%
M3-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.32E-02	8.09E-03	2.70E-03	2.69E-03	3.47E-02	1.86E-02	8.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.24E-01	1.05E-03	2.48E-02	4.51E-03	1.02E-02	9.70E-02	2.79E-02	3.46E-02	100%
M3-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.25E-02	1.09E-02	3.95E-03	3.50E-03	3.36E-02	1.86E-02	7.51E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.88E-04	3.31E-02	6.58E-03	1.33E-02	9.34E-02	2.79E-02	3.28E-02	100%
M3-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.77E-02	3.32E-02	1.47E-02	9.26E-03	9.88E-03	5.25E-03	2.32E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.33E-01	3.72E-04	9.92E-02	2.56E-02	3.68E-02	3.30E-02	8.46E-03	1.23E-02	100%
M3-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.40E-01	9.67E-02	3.66E-02	1.64E-02	1.01E-02	9.82E-03	5.25E-03	2.29E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.39E-01	3.22E-04	1.06E-01	2.87E-02	3.85E-02	3.23E-02	8.46E-03	1.19E-02	100%
M3-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.22E-02	1.24E-02	4.60E-03	3.89E-03	3.33E-02	1.86E-02	7.31E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.29E-01	3.37E-04	3.69E-02	7.66E-03	1.46E-02	9.18E-02	2.79E-02	3.20E-02	100%
M3-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.21E-02	1.27E-02	4.75E-03	3.98E-03	3.32E-02	1.86E-02	7.27E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.30E-01	3.09E-04	3.78E-02	7.92E-03	1.50E-02	9.14E-02	2.79E-02	3.18E-02	100%
M3-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M4-PO1-FOX	0.054	0.108	0.054	0.108	1.47E+01	2.05E-01	8.80E-02	2.35E-02	5.83E-03	8.86E-03	5.59E-03	1.27E-03	2.16E-03	100%
	0.054	2.16	0.054	2.16	1.47E+01	9.04E-02	5.57E-04	7.20E-02	5.83E-03	3.31E-02	1.73E-02	1.27E-03	7.99E-03	100%
M4-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.32E-01	1.05E-01	1.43E-02	4.54E-03	4.88E-03	7.55E-03	3.08E-03	2.23E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.71E-02	3.48E-03	5.20E-02	7.93E-03	2.20E-02	2.81E-02	4.96E-03	1.16E-02	100%
M4-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.46E-02	9.62E-03	7.50E-03	6.58E-03	3.08E-03	1.75E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.09E-01	1.50E-03	8.25E-02	1.68E-02	3.29E-02	2.35E-02	4.96E-03	9.29E-03	100%
M4-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.97E-02	9.19E-03	2.70E-03	3.24E-03	1.29E-02	5.51E-03	3.68E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.33E-02	3.08E-03	3.17E-02	4.51E-03	1.36E-02	4.55E-02	8.24E-03	1.86E-02	100%
M4-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.89E-02	1.21E-02	3.95E-03	4.07E-03	1.21E-02	5.51E-03	3.27E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.83E-02	1.96E-03	4.15E-02	6.58E-03	1.74E-02	4.29E-02	8.24E-03	1.73E-02	100%
M4-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.37E-02	5.76E-03	1.82E-03	1.97E-03	3.56E-02	1.86E-02	8.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.21E-01	1.52E-03	1.79E-02	3.04E-03	7.43E-03	1.00E-01	2.79E-02	3.61E-02	100%
M4-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.35E-02	7.02E-03	2.31E-03	2.35E-03	3.49E-02	1.86E-02	8.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	1.11E-03	2.18E-02	3.85E-03	8.98E-03	9.81E-02	2.79E-02	3.51E-02	100%
M4-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.85E-02	3.46E-02	1.47E-02	9.94E-03	6.29E-03	3.08E-03	1.61E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.28E-01	9.75E-04	1.05E-01	2.56E-02	3.95E-02	2.13E-02	4.96E-03	8.19E-03	100%
M4-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.76E-02	3.80E-02	1.64E-02	1.08E-02	6.24E-03	3.08E-03	1.58E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.34E-01	8.83E-04	1.11E-01	2.87E-02	4.13E-02	2.08E-02	4.96E-03	7.94E-03	100%
M4-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.85E-02	1.35E-02	4.60E-03	4.47E-03	1.18E-02	5.51E-03	3.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	9.09E-02	1.61E-03	4.59E-02	7.66E-03	1.91E-02	4.18E-02	8.24E-03	1.68E-02	100%
M4-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.84E-02	1.39E-02	4.75E-03	4.56E-03	1.17E-02	5.51E-03	3.11E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	9.15E-02	1.54E-03	4.70E-02	7.92E-03	1.95E-02	4.15E-02	8.24E-03	1.66E-02	100%
M4-M3-	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.34E-02	7.54E-03	2.52E-03	2.51E-03	3.47E-02	1.86E-02	8.01E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
PO1(OD)														
	0.09	1.5	0.141	1.449	8.46E-02	1.23E-01	9.69E-04	2.34E-02	4.20E-03	9.60E-03	9.74E-02	2.79E-02	3.48E-02	100%
M4-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.34E-02	7.65E-03	2.57E-03	2.54E-03	3.46E-02	1.86E-02	7.99E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.23E-01	9.41E-04	2.37E-02	4.28E-03	9.73E-03	9.72E-02	2.79E-02	3.47E-02	100%
M4-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.30E-02	3.19E-02	1.33E-02	9.28E-03	1.08E-02	5.51E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	4.62E-04	8.65E-02	2.22E-02	3.22E-02	3.48E-02	8.24E-03	1.33E-02	100%
M4-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.26E-02	1.08E-02	3.93E-03	3.45E-03	3.35E-02	1.86E-02	7.45E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.29E-04	3.29E-02	6.56E-03	1.32E-02	9.33E-02	2.79E-02	3.27E-02	100%
M4-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M5-PO1-FOX	0.054	0.108	0.054	0.108	1.47E+01	2.05E-01	8.81E-02	2.43E-02	5.83E-03	9.22E-03	4.40E-03	9.63E-04	1.72E-03	100%
	0.054	2.16	0.054	2.16	1.47E+01	8.95E-02	7.93E-04	7.43E-02	5.83E-03	3.42E-02	1.36E-02	9.63E-04	6.32E-03	100%
M5-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.32E-01	1.05E-01	1.51E-02	4.54E-03	5.28E-03	5.75E-03	2.18E-03	1.79E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.43E-02	4.50E-03	5.42E-02	7.93E-03	2.31E-02	2.11E-02	3.51E-03	8.80E-03	100%
M5-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.55E-02	9.62E-03	7.93E-03	4.92E-03	2.18E-03	1.37E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.07E-01	2.16E-03	8.51E-02	1.68E-02	3.42E-02	1.75E-02	3.51E-03	7.01E-03	100%
M5-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	1.01E-02	2.70E-03	3.72E-03	8.71E-03	3.23E-03	2.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.51E-02	4.85E-03	3.46E-02	4.51E-03	1.51E-02	3.07E-02	4.83E-03	1.30E-02	100%
M5-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	1.31E-02	3.95E-03	4.59E-03	8.02E-03	3.23E-03	2.39E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.07E-02	3.43E-03	4.51E-02	6.58E-03	1.92E-02	2.88E-02	4.83E-03	1.20E-02	100%
M5-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	6.72E-03	1.82E-03	2.45E-03	1.36E-02	5.51E-03	4.04E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.90E-02	4.04E-03	2.32E-02	3.04E-03	1.01E-02	4.77E-02	8.24E-03	1.97E-02	100%
M5-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	8.03E-03	2.31E-03	2.86E-03	1.30E-02	5.51E-03	3.76E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.09E-02	3.29E-03	2.80E-02	3.85E-03	1.21E-02	4.63E-02	8.24E-03	1.90E-02	100%
M5-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.39E-02	4.53E-03	1.37E-03	1.58E-03	3.62E-02	1.86E-02	8.81E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.94E-03	1.40E-02	2.29E-03	5.87E-03	1.02E-01	2.79E-02	3.70E-02	100%
M5-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.25E-03	1.64E-03	1.81E-03	3.58E-02	1.86E-02	8.58E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.66E-03	1.63E-02	2.73E-03	6.80E-03	1.01E-01	2.79E-02	3.64E-02	100%
M5-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.88E-02	3.55E-02	1.47E-02	1.04E-02	4.67E-03	2.18E-03	1.24E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.26E-01	1.50E-03	1.07E-01	2.56E-02	4.08E-02	1.58E-02	3.51E-03	6.15E-03	100%
M5-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.79E-02	3.88E-02	1.64E-02	1.12E-02	4.62E-03	2.18E-03	1.22E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.32E-01	1.38E-03	1.14E-01	2.87E-02	4.26E-02	1.54E-02	3.51E-03	5.96E-03	100%
M5-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.96E-02	1.46E-02	4.60E-03	5.00E-03	7.78E-03	3.23E-03	2.27E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.36E-02	2.95E-03	4.98E-02	7.66E-03	2.11E-02	2.80E-02	4.83E-03	1.16E-02	100%
M5-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.95E-02	1.49E-02	4.75E-03	5.09E-03	7.74E-03	3.23E-03	2.25E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.43E-02	2.85E-03	5.08E-02	7.92E-03	2.15E-02	2.78E-02	4.83E-03	1.15E-02	100%
M5-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	8.99E-02	8.57E-03	2.52E-03	3.02E-03	1.28E-02	5.51E-03	3.66E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.18E-02	3.03E-03	3.00E-02	4.20E-03	1.29E-02	4.58E-02	8.24E-03	1.88E-02	100%
M5-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	8.99E-02	8.69E-03	2.57E-03	3.06E-03	1.28E-02	5.51E-03	3.64E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.20E-02	2.97E-03	3.04E-02	4.28E-03	1.30E-02	4.57E-02	8.24E-03	1.87E-02	100%
M5-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.53E-03	1.74E-03	1.89E-03	3.56E-02	1.86E-02	8.50E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.21E-01	1.56E-03	1.72E-02	2.90E-03	7.15E-03	1.00E-01	2.79E-02	3.62E-02	100%
M5-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.58E-03	1.76E-03	1.91E-03	3.56E-02	1.86E-02	8.49E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.21E-01	1.53E-03	1.74E-02	2.93E-03	7.22E-03	1.00E-01	2.79E-02	3.62E-02	100%
M5-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.40E-02	3.32E-02	1.33E-02	9.93E-03	6.91E-03	3.23E-03	1.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.17E-01	1.18E-03	9.15E-02	2.22E-02	3.47E-02	2.28E-02	4.83E-03	8.99E-03	100%
M5-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.90E-02	1.20E-02	3.93E-03	4.01E-03	1.20E-02	5.51E-03	3.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.79E-02	1.87E-03	4.13E-02	6.56E-03	1.74E-02	4.28E-02	8.24E-03	1.73E-02	100%
M5-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.35E-02	7.00E-03	2.31E-03	2.35E-03	3.49E-02	1.86E-02	8.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	1.09E-03	2.18E-02	3.85E-03	8.96E-03	9.81E-02	2.79E-02	3.51E-02	100%
M5-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.30E-02	3.19E-02	1.33E-02	9.28E-03	1.08E-02	5.51E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	4.62E-04	8.65E-02	2.22E-02	3.22E-02	3.48E-02	8.24E-03	1.33E-02	100%
M5-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.26E-02	1.08E-02	3.93E-03	3.45E-03	3.35E-02	1.86E-02	7.45E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.29E-04	3.29E-02	6.56E-03	1.32E-02	9.33E-02	2.79E-02	3.27E-02	100%
M5-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M6-PO1-FOX	0.054	0.108	0.054	0.108	1.47E+01	2.05E-01	8.82E-02	2.48E-02	5.83E-03	9.48E-03	3.64E-03	7.77E-04	1.43E-03	100%
	0.054	2.16	0.054	2.16	1.47E+01	8.90E-02	9.82E-04	7.58E-02	5.83E-03	3.50E-02	1.12E-02	7.77E-04	5.22E-03	100%
M6-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.57E-02	4.54E-03	5.57E-03	4.68E-03	1.69E-03	1.49E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	8.29E-02	5.19E-03	5.56E-02	7.93E-03	2.38E-02	1.69E-02	2.72E-03	7.11E-03	100%
M6-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.61E-02	9.62E-03	8.23E-03	3.94E-03	1.69E-03	1.13E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.081	1.5	0.1461	1.4349	9.26E-02	1.06E-01	2.63E-03	8.68E-02	1.68E-02	3.50E-02	1.40E-02	2.72E-03	5.63E-03	100%
M6-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.14E-02	1.09E-02	2.70E-03	4.08E-03	6.76E-03	2.29E-03	2.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.18E-02	6.11E-03	3.63E-02	4.51E-03	1.59E-02	2.33E-02	3.42E-03	9.96E-03	100%
M6-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	1.39E-02	3.95E-03	4.96E-03	6.14E-03	2.29E-03	1.93E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.78E-02	4.50E-03	4.70E-02	6.58E-03	2.02E-02	2.18E-02	3.42E-03	9.17E-03	100%
M6-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	7.55E-03	1.82E-03	2.87E-03	9.37E-03	3.23E-03	3.07E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.03E-02	6.10E-03	2.56E-02	3.04E-03	1.13E-02	3.25E-02	4.83E-03	1.38E-02	100%
M6-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.13E-02	8.92E-03	2.31E-03	3.30E-03	8.87E-03	3.23E-03	2.82E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.25E-02	5.17E-03	3.07E-02	3.85E-03	1.34E-02	3.14E-02	4.83E-03	1.33E-02	100%
M6-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	5.39E-03	1.37E-03	2.01E-03	1.42E-02	5.51E-03	4.34E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.72E-02	4.80E-03	1.84E-02	2.29E-03	8.06E-03	4.92E-02	8.24E-03	2.05E-02	100%
M6-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	6.17E-03	1.64E-03	2.27E-03	1.38E-02	5.51E-03	4.14E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.81E-02	4.30E-03	2.13E-02	2.73E-03	9.27E-03	4.82E-02	8.24E-03	2.00E-02	100%
M6-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	3.74E-03	1.10E-03	1.32E-03	3.68E-02	1.86E-02	9.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.25E-03	1.16E-02	1.84E-03	4.86E-03	1.03E-01	2.79E-02	3.76E-02	100%
M6-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	4.21E-03	1.27E-03	1.47E-03	3.64E-02	1.86E-02	8.90E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.06E-03	1.31E-02	2.11E-03	5.48E-03	1.02E-01	2.79E-02	3.72E-02	100%
M6-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.89E-02	3.61E-02	1.47E-02	1.07E-02	3.72E-03	1.69E-03	1.02E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.25E-01	1.87E-03	1.09E-01	2.56E-02	4.17E-02	1.26E-02	2.72E-03	4.93E-03	100%
M6-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.80E-02	3.95E-02	1.64E-02	1.15E-02	3.68E-03	1.69E-03	1.00E-03	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.31E-01	1.73E-03	1.16E-01	2.87E-02	4.35E-02	1.23E-02	2.72E-03	4.77E-03	100%
M6-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.00E-02	1.54E-02	4.60E-03	5.38E-03	5.94E-03	2.29E-03	1.83E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.08E-02	3.95E-03	5.18E-02	7.66E-03	2.21E-02	2.11E-02	3.42E-03	8.84E-03	100%
M6-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	8.99E-02	1.57E-02	4.75E-03	5.48E-03	5.90E-03	2.29E-03	1.81E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.16E-02	3.84E-03	5.29E-02	7.92E-03	2.25E-02	2.10E-02	3.42E-03	8.77E-03	100%
M6-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.12E-02	9.48E-03	2.52E-03	3.48E-03	8.70E-03	3.23E-03	2.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.35E-02	4.84E-03	3.28E-02	4.20E-03	1.43E-02	3.10E-02	4.83E-03	1.31E-02	100%
M6-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	9.60E-03	2.57E-03	3.52E-03	8.67E-03	3.23E-03	2.72E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.37E-02	4.77E-03	3.33E-02	4.28E-03	1.45E-02	3.09E-02	4.83E-03	1.30E-02	100%
M6-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	6.46E-03	1.74E-03	2.36E-03	1.36E-02	5.51E-03	4.07E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.85E-02	4.12E-03	2.23E-02	2.90E-03	9.73E-03	4.79E-02	8.24E-03	1.98E-02	100%
M6-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	6.52E-03	1.76E-03	2.38E-03	1.36E-02	5.51E-03	4.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.86E-02	4.09E-03	2.26E-02	2.93E-03	9.82E-03	4.79E-02	8.24E-03	1.98E-02	100%
M6-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	4.39E-03	1.33E-03	1.53E-03	3.63E-02	1.86E-02	8.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.99E-03	1.36E-02	2.21E-03	5.70E-03	1.02E-01	2.79E-02	3.71E-02	100%
M6-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	4.42E-03	1.34E-03	1.54E-03	3.63E-02	1.86E-02	8.83E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.97E-03	1.37E-02	2.23E-03	5.75E-03	1.02E-01	2.79E-02	3.71E-02	100%
M6-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.43E-02	3.40E-02	1.33E-02	1.04E-02	5.16E-03	2.29E-03	1.44E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.15E-01	1.79E-03	9.41E-02	2.22E-02	3.60E-02	1.70E-02	3.42E-03	6.80E-03	100%
M6-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	1.30E-02	3.93E-03	4.51E-03	7.96E-03	3.23E-03	2.37E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.03E-02	3.33E-03	4.49E-02	6.56E-03	1.92E-02	2.88E-02	4.83E-03	1.20E-02	100%
M6-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	8.01E-03	2.31E-03	2.85E-03	1.30E-02	5.51E-03	3.75E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.08E-02	3.27E-03	2.80E-02	3.85E-03	1.21E-02	4.63E-02	8.24E-03	1.90E-02	100%
M6-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.24E-03	1.63E-03	1.80E-03	3.58E-02	1.86E-02	8.58E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.66E-03	1.63E-02	2.72E-03	6.79E-03	1.01E-01	2.79E-02	3.64E-02	100%
M6-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.40E-02	3.32E-02	1.33E-02	9.93E-03	6.91E-03	3.23E-03	1.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.17E-01	1.18E-03	9.15E-02	2.22E-02	3.47E-02	2.28E-02	4.83E-03	8.99E-03	100%
M6-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.90E-02	1.20E-02	3.93E-03	4.01E-03	1.20E-02	5.51E-03	3.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.79E-02	1.87E-03	4.13E-02	6.56E-03	1.74E-02	4.28E-02	8.24E-03	1.73E-02	100%
M6-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.35E-02	7.00E-03	2.31E-03	2.35E-03	3.49E-02	1.86E-02	8.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	1.09E-03	2.18E-02	3.85E-03	8.96E-03	9.81E-02	2.79E-02	3.51E-02	100%
M6-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.30E-02	3.19E-02	1.33E-02	9.28E-03	1.08E-02	5.51E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	4.62E-04	8.65E-02	2.22E-02	3.22E-02	3.48E-02	8.24E-03	1.33E-02	100%
M6-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.26E-02	1.08E-02	3.93E-03	3.45E-03	3.35E-02	1.86E-02	7.45E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.29E-04	3.29E-02	6.56E-03	1.32E-02	9.33E-02	2.79E-02	3.27E-02	100%
M6-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M7-PO1-FOX	0.054	0.108	0.054	0.108	1.47E+01	2.05E-01	8.83E-02	2.52E-02	5.83E-03	9.67E-03	3.10E-03	6.51E-04	1.23E-03	100%
	0.054	2.16	0.054	2.16	1.47E+01	8.87E-02	1.13E-03	7.68E-02	5.83E-03	3.55E-02	9.56E-03	6.51E-04	4.45E-03	100%
M7-M1-FOX	0.081	0.081	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.61E-02	4.54E-03	5.79E-03	3.95E-03	1.37E-03	1.29E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.081	1.5	0.1461	1.4349	9.26E-02	8.22E-02	5.67E-03	5.67E-02	7.93E-03	2.44E-02	1.42E-02	2.22E-03	5.98E-03	100%
M7-M1-OD	0.081	0.081	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.65E-02	9.62E-03	8.44E-03	3.30E-03	1.37E-03	9.62E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.05E-01	2.95E-03	8.80E-02	1.68E-02	3.56E-02	1.16E-02	2.22E-03	4.71E-03	100%
M7-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	1.14E-02	2.70E-03	4.35E-03	5.58E-03	1.77E-03	1.90E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.02E-02	6.96E-03	3.74E-02	4.51E-03	1.65E-02	1.89E-02	2.65E-03	8.12E-03	100%
M7-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	1.44E-02	3.95E-03	5.25E-03	5.02E-03	1.77E-03	1.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.64E-02	5.24E-03	4.83E-02	6.58E-03	2.09E-02	1.75E-02	2.65E-03	7.45E-03	100%
M7-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.22E-02	8.20E-03	1.82E-03	3.19E-03	7.37E-03	2.29E-03	2.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.68E-02	7.52E-03	2.69E-02	3.04E-03	1.20E-02	2.48E-02	3.42E-03	1.07E-02	100%
M7-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	9.60E-03	2.31E-03	3.65E-03	6.92E-03	2.29E-03	2.32E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.91E-02	6.49E-03	3.23E-02	3.85E-03	1.42E-02	2.39E-02	3.42E-03	1.02E-02	100%
M7-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	6.14E-03	1.37E-03	2.39E-03	9.93E-03	3.23E-03	3.35E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.81E-02	7.04E-03	2.04E-02	2.29E-03	9.05E-03	3.37E-02	4.83E-03	1.44E-02	100%
M7-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	6.97E-03	1.64E-03	2.67E-03	9.55E-03	3.23E-03	3.16E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.92E-02	6.43E-03	2.35E-02	2.73E-03	1.04E-02	3.29E-02	4.83E-03	1.40E-02	100%
M7-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.08E-02	4.52E-03	1.10E-03	1.71E-03	1.47E-02	5.51E-03	4.58E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.62E-02	5.34E-03	1.53E-02	1.84E-03	6.73E-03	5.02E-02	8.24E-03	2.10E-02	100%
M7-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	5.05E-03	1.27E-03	1.89E-03	1.44E-02	5.51E-03	4.42E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.68E-02	5.01E-03	1.72E-02	2.11E-03	7.54E-03	4.96E-02	8.24E-03	2.07E-02	100%
M7-M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.41E-02	3.19E-03	9.21E-04	1.13E-03	3.71E-02	1.86E-02	9.26E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.47E-03	9.84E-03	1.53E-03	4.15E-03	1.04E-01	2.79E-02	3.81E-02	100%
M7-M6-OD	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.41E-02	3.53E-03	1.03E-03	1.25E-03	3.69E-02	1.86E-02	9.14E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.33E-03	1.09E-02	1.72E-03	4.59E-03	1.03E-01	2.79E-02	3.78E-02	100%
M7-M1-PO1(OD)	0.081	0.081	0.0875	0.0745	1.89E-01	2.38E-01	9.90E-02	3.65E-02	1.47E-02	1.09E-02	3.10E-03	1.37E-03	8.65E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.25E-01	2.13E-03	1.10E-01	2.56E-02	4.22E-02	1.04E-02	2.22E-03	4.11E-03	100%
M7-M1-PO1(FOX)	0.081	0.081	0.0875	0.0745	1.89E-01	2.39E-01	9.80E-02	3.99E-02	1.64E-02	1.17E-02	3.07E-03	1.37E-03	8.47E-04	100%
	0.081	1.5	0.1461	1.4349	9.26E-02	1.31E-01	1.97E-03	1.17E-01	2.87E-02	4.41E-02	1.02E-02	2.22E-03	3.98E-03	100%
M7-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.02E-02	1.59E-02	4.60E-03	5.67E-03	4.84E-03	1.77E-03	1.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.95E-02	4.64E-03	5.32E-02	7.66E-03	2.28E-02	1.70E-02	2.65E-03	7.17E-03	100%
M7-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	1.63E-02	4.75E-03	5.77E-03	4.80E-03	1.77E-03	1.52E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.02E-02	4.52E-03	5.43E-02	7.92E-03	2.32E-02	1.69E-02	2.65E-03	7.11E-03	100%
M7-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	1.02E-02	2.52E-03	3.83E-03	6.77E-03	2.29E-03	2.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.02E-02	6.12E-03	3.44E-02	4.20E-03	1.51E-02	2.35E-02	3.42E-03	1.01E-02	100%
M7-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.16E-02	1.03E-02	2.57E-03	3.86E-03	6.74E-03	2.29E-03	2.22E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.04E-02	6.04E-03	3.49E-02	4.28E-03	1.53E-02	2.35E-02	3.42E-03	1.00E-02	100%
M7-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	7.28E-03	1.74E-03	2.77E-03	9.43E-03	3.23E-03	3.10E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.97E-02	6.21E-03	2.46E-02	2.90E-03	1.09E-02	3.27E-02	4.83E-03	1.39E-02	100%
M7-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	7.34E-03	1.76E-03	2.79E-03	9.40E-03	3.23E-03	3.09E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.98E-02	6.16E-03	2.49E-02	2.93E-03	1.10E-02	3.26E-02	4.83E-03	1.39E-02	100%
M7-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	5.24E-03	1.33E-03	1.96E-03	1.42E-02	5.51E-03	4.37E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.70E-02	4.88E-03	1.79E-02	2.21E-03	7.83E-03	4.93E-02	8.24E-03	2.05E-02	100%
M7-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	5.27E-03	1.34E-03	1.97E-03	1.42E-02	5.51E-03	4.36E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.70E-02	4.86E-03	1.80E-02	2.23E-03	7.89E-03	4.93E-02	8.24E-03	2.05E-02	100%
M7-M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.41E-02	3.65E-03	1.07E-03	1.29E-03	3.68E-02	1.86E-02	9.09E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.28E-03	1.13E-02	1.79E-03	4.74E-03	1.03E-01	2.79E-02	3.77E-02	100%
M7-M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.41E-02	3.67E-03	1.08E-03	1.30E-03	3.68E-02	1.86E-02	9.08E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.27E-03	1.14E-02	1.80E-03	4.78E-03	1.03E-01	2.79E-02	3.77E-02	100%
M7-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.45E-02	3.47E-02	1.33E-02	1.07E-02	4.14E-03	1.77E-03	1.18E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.14E-01	2.23E-03	9.57E-02	2.22E-02	3.68E-02	1.36E-02	2.65E-03	5.48E-03	100%
M7-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.06E-02	1.37E-02	3.93E-03	4.89E-03	6.10E-03	2.29E-03	1.91E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.74E-02	4.40E-03	4.68E-02	6.56E-03	2.01E-02	2.17E-02	3.42E-03	9.16E-03	100%
M7-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.13E-02	8.90E-03	2.31E-03	3.29E-03	8.86E-03	3.23E-03	2.82E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.24E-02	5.15E-03	3.07E-02	3.85E-03	1.34E-02	3.14E-02	4.83E-03	1.33E-02	100%
M7-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	6.16E-03	1.63E-03	2.26E-03	1.38E-02	5.51E-03	4.14E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.81E-02	4.30E-03	2.12E-02	2.72E-03	9.26E-03	4.82E-02	8.24E-03	2.00E-02	100%
M7-M6-M1	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.40E-02	4.21E-03	1.26E-03	1.47E-03	3.64E-02	1.86E-02	8.90E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	2.06E-03	1.31E-02	2.11E-03	5.47E-03	1.02E-01	2.79E-02	3.72E-02	100%
M7-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.43E-02	3.40E-02	1.33E-02	1.04E-02	5.16E-03	2.29E-03	1.44E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.09	1.5	0.141	1.449	8.46E-02	1.15E-01	1.79E-03	9.41E-02	2.22E-02	3.60E-02	1.70E-02	3.42E-03	6.80E-03	100%
M7-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	1.30E-02	3.93E-03	4.51E-03	7.96E-03	3.23E-03	2.37E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.03E-02	3.33E-03	4.49E-02	6.56E-03	1.92E-02	2.88E-02	4.83E-03	1.20E-02	100%
M7-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.01E-02	8.01E-03	2.31E-03	2.85E-03	1.30E-02	5.51E-03	3.75E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.08E-02	3.27E-03	2.80E-02	3.85E-03	1.21E-02	4.63E-02	8.24E-03	1.90E-02	100%
M7-M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.38E-02	5.24E-03	1.63E-03	1.80E-03	3.58E-02	1.86E-02	8.58E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.20E-01	1.66E-03	1.63E-02	2.72E-03	6.79E-03	1.01E-01	2.79E-02	3.64E-02	100%
M7-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.40E-02	3.32E-02	1.33E-02	9.93E-03	6.91E-03	3.23E-03	1.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.17E-01	1.18E-03	9.15E-02	2.22E-02	3.47E-02	2.28E-02	4.83E-03	8.99E-03	100%
M7-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	8.90E-02	1.20E-02	3.93E-03	4.01E-03	1.20E-02	5.51E-03	3.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.79E-02	1.87E-03	4.13E-02	6.56E-03	1.74E-02	4.28E-02	8.24E-03	1.73E-02	100%
M7-M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.35E-02	7.00E-03	2.31E-03	2.35E-03	3.49E-02	1.86E-02	8.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	1.09E-03	2.18E-02	3.85E-03	8.96E-03	9.81E-02	2.79E-02	3.51E-02	100%
M7-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.09E-01	8.30E-02	3.19E-02	1.33E-02	9.28E-03	1.08E-02	5.51E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.22E-01	4.62E-04	8.65E-02	2.22E-02	3.22E-02	3.48E-02	8.24E-03	1.33E-02	100%
M7-M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.10E-01	8.26E-02	1.08E-02	3.93E-03	3.45E-03	3.35E-02	1.86E-02	7.45E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.27E-01	4.29E-04	3.29E-02	6.56E-03	1.32E-02	9.33E-02	2.79E-02	3.27E-02	100%
M7-M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.16E-01	7.70E-02	3.04E-02	1.33E-02	8.56E-03	3.18E-02	1.86E-02	6.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.56E-01	2.38E-05	7.43E-02	2.22E-02	2.60E-02	8.15E-02	2.79E-02	2.68E-02	100%
M8-PO1-FOX	0.05	0.11	0.054	0.108	1.47E+01	2.05E-01	8.83E-02	2.56E-02	5.83E-03	9.90E-03	2.50E-03	5.14E-04	9.92E-04	100%
	0.05	2.16	0.054	2.16	1.47E+01	8.84E-02	1.30E-03	7.81E-02	5.83E-03	3.61E-02	7.69E-03	5.14E-04	3.59E-03	100%
M8-M1-FOX	0.08	0.08	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.66E-02	4.54E-03	6.06E-03	3.16E-03	1.05E-03	1.05E-03	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	8.15E-02	6.16E-03	5.80E-02	7.93E-03	2.50E-02	1.12E-02	1.70E-03	4.76E-03	100%
M8-M1-OD	0.08	0.08	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.70E-02	9.62E-03	8.70E-03	2.60E-03	1.05E-03	7.74E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.05E-01	3.28E-03	8.93E-02	1.68E-02	3.63E-02	9.13E-03	1.70E-03	3.72E-03	100%
M8-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.19E-02	1.21E-02	2.70E-03	4.69E-03	4.37E-03	1.29E-03	1.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.90E-02	7.84E-03	3.88E-02	4.51E-03	1.72E-02	1.44E-02	1.93E-03	6.26E-03	100%
M8-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.09E-02	1.51E-02	3.95E-03	5.59E-03	3.89E-03	1.29E-03	1.30E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.52E-02	5.99E-03	4.99E-02	6.58E-03	2.17E-02	1.34E-02	1.93E-03	5.71E-03	100%
M8-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	9.00E-03	1.82E-03	3.59E-03	5.57E-03	1.54E-03	2.01E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.43E-02	8.95E-03	2.84E-02	3.04E-03	1.27E-02	1.80E-02	2.31E-03	7.84E-03	100%
M8-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.22E-02	1.04E-02	2.31E-03	4.05E-03	5.17E-03	1.54E-03	1.81E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.68E-02	7.81E-03	3.39E-02	3.85E-03	1.50E-02	1.73E-02	2.31E-03	7.47E-03	100%
M8-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.28E-02	7.07E-03	1.37E-03	2.85E-03	7.03E-03	1.92E-03	2.55E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.32E-02	9.30E-03	2.21E-02	2.29E-03	9.93E-03	2.25E-02	2.88E-03	9.79E-03	100%
M8-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	7.94E-03	1.64E-03	3.15E-03	6.70E-03	1.92E-03	2.39E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.44E-02	8.59E-03	2.54E-02	2.73E-03	1.13E-02	2.19E-02	2.88E-03	9.49E-03	100%
M8-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	5.60E-03	1.10E-03	2.25E-03	8.94E-03	2.55E-03	3.20E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.43E-02	8.85E-03	1.77E-02	1.84E-03	7.95E-03	2.89E-02	3.81E-03	1.25E-02	100%
M8-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	6.18E-03	1.27E-03	2.46E-03	8.66E-03	2.55E-03	3.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.50E-02	8.40E-03	1.98E-02	2.11E-03	8.87E-03	2.84E-02	3.81E-03	1.23E-02	100%
M8-M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.19E-02	4.36E-03	9.21E-04	1.72E-03	1.19E-02	3.79E-03	4.07E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.89E-02	7.54E-03	1.42E-02	1.53E-03	6.34E-03	3.96E-02	5.66E-03	1.70E-02	100%
M8-M6-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.19E-02	4.77E-03	1.03E-03	1.87E-03	1.17E-02	3.79E-03	3.95E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.92E-02	7.26E-03	1.57E-02	1.72E-03	6.97E-03	3.91E-02	5.66E-03	1.67E-02	100%
M8-M7-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.06E-02	3.34E-03	7.91E-04	1.28E-03	1.96E-02	7.34E-03	6.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.51E-02	5.46E-03	1.09E-02	1.32E-03	4.79E-03	6.32E-02	1.10E-02	2.61E-02	100%
M8-M7-OD	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.06E-02	3.63E-03	8.71E-04	1.38E-03	1.94E-02	7.34E-03	6.02E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.53E-02	5.30E-03	1.19E-02	1.45E-03	5.21E-03	6.28E-02	1.10E-02	2.59E-02	100%
M8-M1-PO1(OD)	0.08	0.08	0.0875	0.0745	1.89E-01	2.38E-01	9.91E-02	3.70E-02	1.47E-02	1.12E-02	2.44E-03	1.05E-03	6.92E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.24E-01	2.40E-03	1.11E-01	2.56E-02	4.29E-02	8.17E-03	1.70E-03	3.24E-03	100%
M8-M1-PO1(FOX)	0.08	0.08	0.0875	0.0745	1.89E-01	2.39E-01	9.81E-02	4.04E-02	1.64E-02	1.20E-02	2.41E-03	1.05E-03	6.76E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.31E-01	2.23E-03	1.18E-01	2.87E-02	4.47E-02	7.96E-03	1.70E-03	3.13E-03	100%
M8-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	1.66E-02	4.60E-03	6.01E-03	3.73E-03	1.29E-03	1.22E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.84E-02	5.34E-03	5.48E-02	7.66E-03	2.36E-02	1.29E-02	1.93E-03	5.49E-03	100%
M8-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.03E-02	1.70E-02	4.75E-03	6.11E-03	3.70E-03	1.29E-03	1.21E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.92E-02	5.21E-03	5.59E-02	7.92E-03	2.40E-02	1.28E-02	1.93E-03	5.44E-03	100%
M8-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	1.10E-02	2.52E-03	4.24E-03	5.04E-03	1.54E-03	1.75E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.79E-02	7.40E-03	3.61E-02	4.20E-03	1.60E-02	1.70E-02	2.31E-03	7.34E-03	100%
M8-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	1.11E-02	2.57E-03	4.28E-03	5.02E-03	1.54E-03	1.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.82E-02	7.32E-03	3.66E-02	4.28E-03	1.62E-02	1.69E-02	2.31E-03	7.31E-03	100%
M8-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	8.26E-03	1.74E-03	3.26E-03	6.58E-03	1.92E-03	2.33E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.49E-02	8.33E-03	2.66E-02	2.90E-03	1.19E-02	2.17E-02	2.88E-03	9.39E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M8-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	8.33E-03	1.76E-03	3.28E-03	6.56E-03	1.92E-03	2.32E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.50E-02	8.28E-03	2.69E-02	2.93E-03	1.20E-02	2.16E-02	2.88E-03	9.37E-03	100%
M8-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	6.39E-03	1.33E-03	2.53E-03	8.56E-03	2.55E-03	3.00E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.53E-02	8.24E-03	2.06E-02	2.21E-03	9.20E-03	2.82E-02	3.81E-03	1.22E-02	100%
M8-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	6.43E-03	1.34E-03	2.55E-03	8.54E-03	2.55E-03	2.99E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.53E-02	8.21E-03	2.08E-02	2.23E-03	9.27E-03	2.81E-02	3.81E-03	1.22E-02	100%
M8-M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	4.91E-03	1.07E-03	1.92E-03	1.16E-02	3.79E-03	3.91E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.94E-02	7.16E-03	1.62E-02	1.79E-03	7.18E-03	3.89E-02	5.66E-03	1.66E-02	100%
M8-M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.18E-02	4.94E-03	1.08E-03	1.93E-03	1.16E-02	3.79E-03	3.90E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.94E-02	7.14E-03	1.63E-02	1.80E-03	7.23E-03	3.89E-02	5.66E-03	1.66E-02	100%
M8-M7-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.06E-02	3.73E-03	8.99E-04	1.41E-03	1.93E-02	7.34E-03	5.99E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.53E-02	5.25E-03	1.22E-02	1.50E-03	5.35E-03	6.26E-02	1.10E-02	2.58E-02	100%
M8-M7-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.06E-02	3.75E-03	9.05E-04	1.42E-03	1.93E-02	7.34E-03	5.98E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.53E-02	5.24E-03	1.23E-02	1.51E-03	5.38E-03	6.26E-02	1.10E-02	2.58E-02	100%
M8-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.54E-02	1.33E-02	1.10E-02	3.13E-03	1.29E-03	9.20E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.67E-03	9.75E-02	2.22E-02	3.77E-02	1.02E-02	1.93E-03	4.15E-03	100%
M8-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.09E-02	1.46E-02	3.93E-03	5.32E-03	4.47E-03	1.54E-03	1.46E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.54E-02	5.48E-03	4.88E-02	6.56E-03	2.11E-02	1.56E-02	2.31E-03	6.64E-03	100%
M8-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	9.94E-03	2.31E-03	3.82E-03	6.09E-03	1.92E-03	2.08E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.79E-02	7.10E-03	3.30E-02	3.85E-03	1.46E-02	2.07E-02	2.88E-03	8.92E-03	100%
M8-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.22E-02	7.39E-03	1.63E-03	2.88E-03	8.14E-03	2.55E-03	2.79E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.67E-02	7.47E-03	2.43E-02	2.72E-03	1.08E-02	2.74E-02	3.81E-03	1.18E-02	100%
M8-M6-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	5.57E-03	1.26E-03	2.15E-03	1.12E-02	3.79E-03	3.73E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.01E-02	6.70E-03	1.85E-02	2.11E-03	8.22E-03	3.82E-02	5.66E-03	1.63E-02	100%
M8-M7-M1	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.05E-02	4.18E-03	1.03E-03	1.57E-03	1.90E-02	7.34E-03	5.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.57E-02	4.99E-03	1.37E-02	1.72E-03	6.01E-03	6.19E-02	1.10E-02	2.55E-02	100%
M8-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.45E-02	3.50E-02	1.33E-02	1.08E-02	3.67E-03	1.54E-03	1.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.44E-03	9.65E-02	2.22E-02	3.72E-02	1.20E-02	2.31E-03	4.86E-03	100%
M8-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	1.41E-02	3.93E-03	5.08E-03	5.33E-03	1.92E-03	1.70E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.64E-02	4.91E-03	4.77E-02	6.56E-03	2.06E-02	1.88E-02	2.88E-03	7.96E-03	100%
M8-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.17E-02	9.37E-03	2.31E-03	3.53E-03	7.49E-03	2.55E-03	2.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.00E-02	6.09E-03	3.18E-02	3.85E-03	1.40E-02	2.61E-02	3.81E-03	1.11E-02	100%
M8-M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.15E-02	6.74E-03	1.63E-03	2.55E-03	1.07E-02	3.79E-03	3.46E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.16E-02	5.87E-03	2.29E-02	2.72E-03	1.01E-02	3.70E-02	5.66E-03	1.57E-02	100%
M8-M7-M2	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.04E-02	4.94E-03	1.26E-03	1.84E-03	1.86E-02	7.34E-03	5.61E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.64E-02	4.55E-03	1.64E-02	2.11E-03	7.14E-03	6.09E-02	1.10E-02	2.50E-02	100%
M8-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.44E-02	3.45E-02	1.33E-02	1.06E-02	4.44E-03	1.92E-03	1.26E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.14E-01	2.10E-03	9.52E-02	2.22E-02	3.65E-02	1.46E-02	2.88E-03	5.88E-03	100%
M8-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	1.35E-02	3.93E-03	4.78E-03	6.65E-03	2.55E-03	2.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.82E-02	4.09E-03	4.63E-02	6.56E-03	1.98E-02	2.38E-02	3.81E-03	9.98E-03	100%
M8-M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	8.66E-03	2.31E-03	3.17E-03	9.98E-03	3.79E-03	3.10E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.47E-02	4.67E-03	3.00E-02	3.85E-03	1.31E-02	3.54E-02	5.66E-03	1.49E-02	100%
M8-M7-M3	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.02E-02	6.07E-03	1.63E-03	2.22E-03	1.79E-02	7.34E-03	5.30E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.76E-02	3.91E-03	2.03E-02	2.72E-03	8.80E-03	5.95E-02	1.10E-02	2.43E-02	100%
M8-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.42E-02	3.38E-02	1.33E-02	1.02E-02	5.66E-03	2.55E-03	1.55E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.15E-01	1.62E-03	9.33E-02	2.22E-02	3.56E-02	1.87E-02	3.81E-03	7.44E-03	100%
M8-M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	8.98E-02	1.27E-02	3.93E-03	4.38E-03	9.03E-03	3.79E-03	2.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.23E-02	2.96E-03	4.39E-02	6.56E-03	1.87E-02	3.25E-02	5.66E-03	1.34E-02	100%
M8-M7-M4	0.09	0.09	0.09	0.09	1.67E-01	2.05E-01	8.98E-02	7.95E-03	2.31E-03	2.82E-03	1.71E-02	7.34E-03	4.89E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	9.02E-02	2.98E-03	2.69E-02	3.85E-03	1.15E-02	5.74E-02	1.10E-02	2.32E-02	100%
M8-M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.37E-02	3.29E-02	1.33E-02	9.77E-03	7.91E-03	3.79E-03	2.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.18E-01	1.01E-03	9.02E-02	2.22E-02	3.40E-02	2.60E-02	5.66E-03	1.01E-02	100%
M8-M7-M5	0.09	0.09	0.09	0.09	1.67E-01	2.05E-01	8.87E-02	1.20E-02	3.93E-03	4.02E-03	1.60E-02	7.34E-03	4.31E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	9.68E-02	1.72E-03	3.99E-02	6.56E-03	1.67E-02	5.35E-02	1.10E-02	2.12E-02	100%
M8-M7-M6	0.09	0.09	0.09	0.09	1.67E-01	2.12E-01	8.27E-02	3.21E-02	1.33E-02	9.40E-03	1.45E-02	7.34E-03	3.59E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.30E-01	4.67E-04	8.50E-02	2.22E-02	3.14E-02	4.43E-02	1.10E-02	1.67E-02	100%
M9-PO1-FOX	0.05	0.11	0.054	0.108	1.47E+01	2.05E-01	8.84E-02	2.61E-02	5.83E-03	1.02E-02	1.88E-03	3.78E-04	7.50E-04	100%
	0.05	2.16	0.054	2.16	1.47E+01	8.81E-02	1.46E-03	7.95E-02	5.83E-03	3.68E-02	5.76E-03	3.78E-04	2.69E-03	100%
M9-M1-FOX	0.08	0.08	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.73E-02	4.54E-03	6.36E-03	2.36E-03	7.53E-04	8.03E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	8.10E-02	6.59E-03	5.96E-02	7.93E-03	2.58E-02	8.29E-03	1.21E-03	3.54E-03	100%
M9-M1-OD	0.08	0.08	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.76E-02	9.62E-03	8.98E-03	1.92E-03	7.53E-04	5.81E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.05E-01	3.56E-03	9.09E-02	1.68E-02	3.70E-02	6.69E-03	1.21E-03	2.74E-03	100%
M9-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.21E-02	1.28E-02	2.70E-03	5.07E-03	3.21E-03	8.80E-04	1.17E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.09	1.5	0.141	1.449	8.46E-02	6.81E-02	8.56E-03	4.06E-02	4.51E-03	1.80E-02	1.04E-02	1.32E-03	4.55E-03	100%
M9-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	1.59E-02	3.95E-03	5.96E-03	2.83E-03	8.80E-04	9.73E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.45E-02	6.60E-03	5.17E-02	6.58E-03	2.26E-02	9.56E-03	1.32E-03	4.12E-03	100%
M9-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	9.91E-03	1.82E-03	4.04E-03	4.01E-03	9.92E-04	1.51E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.29E-02	1.01E-02	3.03E-02	3.04E-03	1.36E-02	1.25E-02	1.48E-03	5.50E-03	100%
M9-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	1.13E-02	2.31E-03	4.51E-03	3.68E-03	9.92E-04	1.34E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.55E-02	8.86E-03	3.59E-02	3.85E-03	1.60E-02	1.19E-02	1.48E-03	5.21E-03	100%
M9-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.32E-02	8.14E-03	1.37E-03	3.38E-03	4.89E-03	1.14E-03	1.88E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.09E-02	1.10E-02	2.41E-02	2.29E-03	1.09E-02	1.47E-02	1.70E-03	6.52E-03	100%
M9-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.30E-02	9.03E-03	1.64E-03	3.70E-03	4.61E-03	1.14E-03	1.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.22E-02	1.02E-02	2.75E-02	2.73E-03	1.24E-02	1.43E-02	1.70E-03	6.29E-03	100%
M9-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	6.85E-03	1.10E-03	2.88E-03	5.90E-03	1.33E-03	2.29E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.04E-02	1.15E-02	2.00E-02	1.84E-03	9.06E-03	1.75E-02	1.99E-03	7.74E-03	100%
M9-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.32E-02	7.47E-03	1.27E-03	3.10E-03	5.65E-03	1.33E-03	2.16E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.11E-02	1.10E-02	2.22E-02	2.11E-03	1.00E-02	1.70E-02	1.99E-03	7.53E-03	100%
M9-M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.32E-02	5.85E-03	9.21E-04	2.46E-03	7.16E-03	1.60E-03	2.78E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.13E-02	1.17E-02	1.69E-02	1.53E-03	7.67E-03	2.10E-02	2.39E-03	9.28E-03	100%
M9-M6-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.32E-02	6.31E-03	1.03E-03	2.64E-03	6.93E-03	1.60E-03	2.66E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.17E-02	1.13E-02	1.85E-02	1.72E-03	8.37E-03	2.06E-02	2.39E-03	9.09E-03	100%
M9-M7-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.39E-02	5.23E-03	7.91E-04	2.22E-03	9.36E-03	2.01E-03	3.67E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.58E-02	1.26E-02	1.45E-02	1.32E-03	6.60E-03	2.60E-02	3.01E-03	1.15E-02	100%
M9-M7-OD	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.38E-02	5.61E-03	8.71E-04	2.37E-03	9.15E-03	2.01E-03	3.57E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.61E-02	1.24E-02	1.57E-02	1.45E-03	7.13E-03	2.57E-02	3.01E-03	1.13E-02	100%
M9-M8-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.41E-01	1.41E-01	7.41E-03	3.25E-03	2.08E-03	5.21E-02	3.01E-02	1.10E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.60E-01	1.80E-02	1.74E-02	3.25E-03	7.09E-03	1.07E-01	3.01E-02	3.84E-02	100%
M9-M8-OD	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.41E-01	7.92E-03	3.51E-03	2.21E-03	5.19E-02	3.01E-02	1.09E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.61E-01	1.77E-02	1.87E-02	3.51E-03	7.59E-03	1.07E-01	3.01E-02	3.83E-02	100%
M9-M1-PO1(OD)	0.08	0.08	0.0875	0.0745	1.89E-01	2.38E-01	9.91E-02	3.75E-02	1.47E-02	1.14E-02	1.79E-03	7.53E-04	5.16E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.24E-01	2.62E-03	1.13E-01	2.56E-02	4.37E-02	5.97E-03	1.21E-03	2.38E-03	100%
M9-M1-PO1(FOX)	0.08	0.08	0.0875	0.0745	1.89E-01	2.39E-01	9.82E-02	4.09E-02	1.64E-02	1.23E-02	1.76E-03	7.53E-04	5.04E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.30E-01	2.44E-03	1.20E-01	2.87E-02	4.55E-02	5.80E-03	1.21E-03	2.29E-03	100%
M9-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	1.74E-02	4.60E-03	6.38E-03	2.70E-03	8.80E-04	9.10E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.77E-02	5.92E-03	5.67E-02	7.66E-03	2.45E-02	9.22E-03	1.32E-03	3.95E-03	100%
M9-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.04E-02	1.77E-02	4.75E-03	6.48E-03	2.67E-03	8.80E-04	8.97E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.85E-02	5.78E-03	5.78E-02	7.92E-03	2.49E-02	9.15E-03	1.32E-03	3.91E-03	100%
M9-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.19E-02	2.52E-03	4.70E-03	3.57E-03	9.92E-04	1.29E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.67E-02	8.41E-03	3.81E-02	4.20E-03	1.70E-02	1.17E-02	1.48E-03	5.11E-03	100%
M9-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.22E-02	1.20E-02	2.57E-03	4.74E-03	3.55E-03	9.92E-04	1.28E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.69E-02	8.32E-03	3.86E-02	4.28E-03	1.72E-02	1.17E-02	1.48E-03	5.09E-03	100%
M9-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	9.36E-03	1.74E-03	3.81E-03	4.51E-03	1.14E-03	1.69E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.28E-02	9.94E-03	2.88E-02	2.90E-03	1.29E-02	1.41E-02	1.70E-03	6.21E-03	100%
M9-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	9.43E-03	1.76E-03	3.84E-03	4.49E-03	1.14E-03	1.68E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.29E-02	9.88E-03	2.90E-02	2.93E-03	1.30E-02	1.41E-02	1.70E-03	6.19E-03	100%
M9-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	7.70E-03	1.33E-03	3.19E-03	5.56E-03	1.33E-03	2.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.14E-02	1.08E-02	2.30E-02	2.21E-03	1.04E-02	1.69E-02	1.99E-03	7.46E-03	100%
M9-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	7.74E-03	1.34E-03	3.20E-03	5.55E-03	1.33E-03	2.11E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.15E-02	1.07E-02	2.32E-02	2.23E-03	1.05E-02	1.69E-02	1.99E-03	7.45E-03	100%
M9-M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	6.47E-03	1.07E-03	2.70E-03	6.85E-03	1.60E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.19E-02	1.12E-02	1.90E-02	1.79E-03	8.62E-03	2.04E-02	2.39E-03	9.02E-03	100%
M9-M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	6.51E-03	1.08E-03	2.71E-03	6.84E-03	1.60E-03	2.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.19E-02	1.12E-02	1.91E-02	1.80E-03	8.67E-03	2.04E-02	2.39E-03	9.01E-03	100%
M9-M7-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.38E-02	5.74E-03	8.99E-04	2.42E-03	9.08E-03	2.01E-03	3.53E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.62E-02	1.23E-02	1.61E-02	1.50E-03	7.31E-03	2.55E-02	3.01E-03	1.13E-02	100%
M9-M7-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.38E-02	5.77E-03	9.05E-04	2.43E-03	9.06E-03	2.01E-03	3.53E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.62E-02	1.23E-02	1.62E-02	1.51E-03	7.35E-03	2.55E-02	3.01E-03	1.13E-02	100%
M9-M8-PO1(OD)	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.41E-01	8.10E-03	3.60E-03	2.25E-03	5.19E-02	3.01E-02	1.09E-02	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.36	2	0.405	1.955	2.20E-02	1.61E-01	1.76E-02	1.91E-02	3.60E-03	7.75E-03	1.07E-01	3.01E-02	3.82E-02	100%
M9-M8-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.41E-01	8.13E-03	3.62E-03	2.26E-03	5.18E-02	3.01E-02	1.09E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.61E-01	1.76E-02	1.92E-02	3.62E-03	7.79E-03	1.07E-01	3.01E-02	3.82E-02	100%
M9-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.61E-02	1.33E-02	1.14E-02	2.22E-03	8.80E-04	6.69E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.03E-03	9.93E-02	2.22E-02	3.86E-02	7.21E-03	1.32E-03	2.95E-03	100%
M9-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.55E-02	3.93E-03	5.78E-03	3.11E-03	9.92E-04	1.06E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.43E-02	6.33E-03	5.10E-02	6.56E-03	2.22E-02	1.06E-02	1.48E-03	4.57E-03	100%
M9-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	1.11E-02	2.31E-03	4.38E-03	4.10E-03	1.14E-03	1.48E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.59E-02	8.57E-03	3.53E-02	3.85E-03	1.57E-02	1.34E-02	1.70E-03	5.85E-03	100%
M9-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	8.76E-03	1.63E-03	3.56E-03	5.20E-03	1.33E-03	1.94E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.30E-02	9.86E-03	2.70E-02	2.72E-03	1.21E-02	1.63E-02	1.99E-03	7.16E-03	100%
M9-M6-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	7.22E-03	1.26E-03	2.98E-03	6.53E-03	1.60E-03	2.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.28E-02	1.06E-02	2.16E-02	2.11E-03	9.77E-03	1.99E-02	2.39E-03	8.76E-03	100%
M9-M7-M1	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.37E-02	6.33E-03	1.03E-03	2.65E-03	8.78E-03	2.01E-03	3.38E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.68E-02	1.19E-02	1.80E-02	1.72E-03	8.14E-03	2.51E-02	3.01E-03	1.10E-02	100%
M9-M8-M1	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.41E-01	8.88E-03	4.01E-03	2.44E-03	5.16E-02	3.01E-02	1.08E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.62E-01	1.72E-02	2.10E-02	4.01E-03	8.51E-03	1.06E-01	3.01E-02	3.80E-02	100%
M9-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.59E-02	1.33E-02	1.13E-02	2.47E-03	9.92E-04	7.41E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.93E-03	9.88E-02	2.22E-02	3.83E-02	8.05E-03	1.48E-03	3.28E-03	100%
M9-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	1.53E-02	3.93E-03	5.66E-03	3.49E-03	1.14E-03	1.18E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.47E-02	6.11E-03	5.05E-02	6.56E-03	2.20E-02	1.20E-02	1.70E-03	5.14E-03	100%
M9-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.08E-02	2.31E-03	4.25E-03	4.66E-03	1.33E-03	1.66E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.66E-02	8.24E-03	3.48E-02	3.85E-03	1.55E-02	1.53E-02	1.99E-03	6.67E-03	100%
M9-M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.26E-02	8.51E-03	1.63E-03	3.44E-03	6.05E-03	1.60E-03	2.22E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.46E-02	9.54E-03	2.64E-02	2.72E-03	1.18E-02	1.91E-02	2.39E-03	8.35E-03	100%
M9-M7-M2	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.35E-02	7.28E-03	1.26E-03	3.01E-03	8.33E-03	2.01E-03	3.16E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.78E-02	1.11E-02	2.12E-02	2.11E-03	9.54E-03	2.43E-02	3.01E-03	1.07E-02	100%
M9-M8-M2	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.40E-01	1.01E-02	4.67E-03	2.73E-03	5.12E-02	3.01E-02	1.06E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.63E-01	1.65E-02	2.41E-02	4.67E-03	9.71E-03	1.06E-01	3.01E-02	3.77E-02	100%
M9-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.57E-02	1.33E-02	1.12E-02	2.80E-03	1.14E-03	8.31E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.81E-03	9.83E-02	2.22E-02	3.80E-02	9.12E-03	1.70E-03	3.71E-03	100%
M9-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.09E-02	1.50E-02	3.93E-03	5.53E-03	3.99E-03	1.33E-03	1.33E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.53E-02	5.85E-03	4.98E-02	6.56E-03	2.16E-02	1.38E-02	1.99E-03	5.89E-03	100%
M9-M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.20E-02	1.06E-02	2.31E-03	4.13E-03	5.46E-03	1.60E-03	1.93E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.81E-02	7.98E-03	3.41E-02	3.85E-03	1.51E-02	1.80E-02	2.39E-03	7.80E-03	100%
M9-M7-M3	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.31E-02	8.65E-03	1.63E-03	3.51E-03	7.79E-03	2.01E-03	2.89E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.96E-02	1.01E-02	2.59E-02	2.72E-03	1.16E-02	2.34E-02	3.01E-03	1.02E-02	100%
M9-M8-M3	0.36	0.36	0.405	0.315	2.21E-02	3.42E-01	1.40E-01	1.18E-02	5.59E-03	3.12E-03	5.07E-02	3.01E-02	1.03E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.64E-01	1.56E-02	2.82E-02	5.59E-03	1.13E-02	1.05E-01	3.01E-02	3.74E-02	100%
M9-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.45E-02	3.54E-02	1.33E-02	1.11E-02	3.23E-03	1.33E-03	9.50E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	2.67E-03	9.75E-02	2.22E-02	3.77E-02	1.05E-02	1.99E-03	4.27E-03	100%
M9-M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.07E-02	1.48E-02	3.93E-03	5.43E-03	4.72E-03	1.60E-03	1.56E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.66E-02	5.67E-03	4.91E-02	6.56E-03	2.13E-02	1.62E-02	2.39E-03	6.91E-03	100%
M9-M7-M4	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.25E-02	1.08E-02	2.31E-03	4.26E-03	7.10E-03	2.01E-03	2.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.30E-02	8.56E-03	3.37E-02	3.85E-03	1.49E-02	2.22E-02	3.01E-03	9.60E-03	100%
M9-M8-M4	0.36	0.36	0.405	0.315	2.21E-02	3.43E-01	1.39E-01	1.43E-02	6.96E-03	3.68E-03	5.02E-02	3.01E-02	1.01E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.67E-01	1.44E-02	3.42E-02	6.96E-03	1.36E-02	1.04E-01	3.01E-02	3.70E-02	100%
M9-M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.44E-02	3.52E-02	1.33E-02	1.10E-02	3.85E-03	1.60E-03	1.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.14E-01	2.62E-03	9.67E-02	2.22E-02	3.72E-02	1.25E-02	2.39E-03	5.04E-03	100%
M9-M7-M5	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.12E-02	1.53E-02	3.93E-03	5.67E-03	6.21E-03	2.01E-03	2.10E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	8.15E-02	6.27E-03	4.88E-02	6.56E-03	2.11E-02	2.02E-02	3.01E-03	8.59E-03	100%
M9-M8-M5	0.36	0.36	0.405	0.315	2.21E-02	3.44E-01	1.38E-01	1.83E-02	9.23E-03	4.56E-03	4.97E-02	3.01E-02	9.83E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.72E-01	1.27E-02	4.35E-02	9.23E-03	1.71E-02	1.03E-01	3.01E-02	3.65E-02	100%
M9-M7-M6	0.09	0.09	0.09	0.09	1.67E-01	2.11E-01	8.47E-02	3.62E-02	1.33E-02	1.14E-02	5.10E-03	2.01E-03	1.54E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.19E-01	3.10E-03	9.72E-02	2.22E-02	3.75E-02	1.58E-02	3.01E-03	6.39E-03	100%
M9-M8-M6	0.36	0.36	0.405	0.315	2.21E-02	3.47E-01	1.36E-01	2.62E-02	1.37E-02	6.23E-03	4.92E-02	3.01E-02	9.58E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.82E-01	1.03E-02	5.99E-02	1.37E-02	2.31E-02	1.01E-01	3.01E-02	3.56E-02	100%
M9-M8-M7	0.36	0.36	0.405	0.315	2.21E-02	3.57E-01	1.30E-01	4.83E-02	2.66E-02	1.09E-02	4.89E-02	3.01E-02	9.40E-03	100%
	0.36	2	0.405	1.955	2.20E-02	2.09E-01	6.65E-03	9.76E-02	2.66E-02	3.55E-02	9.79E-02	3.01E-02	3.39E-02	100%
M10-PO1-FOX	0.05	0.11	0.054	0.108	1.47E+01	2.05E-01	8.84E-02	2.65E-02	5.83E-03	1.03E-02	1.47E-03	2.92E-04	5.90E-04	100%
	0.05	2.16	0.054	2.16	1.47E+01	8.80E-02	1.55E-03	8.04E-02	5.83E-03	3.73E-02	4.51E-03	2.92E-04	2.11E-03	100%
M10-M1-FOX	0.08	0.08	0.0875	0.0745	1.89E-01	2.31E-01	1.06E-01	1.77E-02	4.54E-03	6.57E-03	1.85E-03	5.72E-04	6.37E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	8.08E-02	6.80E-03	6.08E-02	7.93E-03	2.64E-02	6.45E-03	9.22E-04	2.77E-03	100%
M10-M1-OD	0.08	0.08	0.0875	0.0745	1.89E-01	2.34E-01	1.02E-01	2.79E-02	9.62E-03	9.16E-03	1.48E-03	5.72E-04	4.56E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.05E-01	3.69E-03	9.20E-02	1.68E-02	3.76E-02	5.17E-03	9.22E-04	2.12E-03	100%
M10-M2-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.21E-02	1.34E-02	2.70E-03	5.34E-03	2.50E-03	6.51E-04	9.23E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.78E-02	8.91E-03	4.19E-02	4.51E-03	1.87E-02	8.02E-03	9.73E-04	3.52E-03	100%
M10-M2-OD	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.64E-02	3.95E-03	6.22E-03	2.18E-03	6.51E-04	7.62E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.42E-02	6.89E-03	5.31E-02	6.58E-03	2.33E-02	7.31E-03	9.73E-04	3.17E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M10-M3-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.30E-02	1.06E-02	1.82E-03	4.37E-03	3.09E-03	7.10E-04	1.19E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.24E-02	1.06E-02	3.18E-02	3.04E-03	1.44E-02	9.45E-03	1.06E-03	4.20E-03	100%
M10-M3-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	1.20E-02	2.31E-03	4.83E-03	2.81E-03	7.10E-04	1.05E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.50E-02	9.33E-03	3.74E-02	3.85E-03	1.68E-02	8.96E-03	1.06E-03	3.95E-03	100%
M10-M4-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.34E-02	8.90E-03	1.37E-03	3.76E-03	3.72E-03	7.81E-04	1.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.02E-02	1.18E-02	2.57E-02	2.29E-03	1.17E-02	1.09E-02	1.17E-03	4.88E-03	100%
M10-M4-OD	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	9.79E-03	1.64E-03	4.08E-03	3.47E-03	7.81E-04	1.35E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.15E-02	1.09E-02	2.91E-02	2.73E-03	1.32E-02	1.05E-02	1.17E-03	4.68E-03	100%
M10-M5-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.36E-02	7.73E-03	1.10E-03	3.31E-03	4.41E-03	8.67E-04	1.77E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.93E-02	1.25E-02	2.17E-02	1.84E-03	9.92E-03	1.26E-02	1.30E-03	5.63E-03	100%
M10-M5-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.34E-02	8.36E-03	1.27E-03	3.55E-03	4.19E-03	8.67E-04	1.66E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.01E-02	1.20E-02	2.40E-02	2.11E-03	1.09E-02	1.22E-02	1.30E-03	5.45E-03	100%
M10-M6-FOX	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.36E-02	6.86E-03	9.21E-04	2.97E-03	5.22E-03	9.75E-04	2.12E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	5.96E-02	1.32E-02	1.88E-02	1.53E-03	8.62E-03	1.45E-02	1.46E-03	6.50E-03	100%
M10-M6-OD	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.35E-02	7.35E-03	1.03E-03	3.16E-03	5.02E-03	9.75E-04	2.02E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.01E-02	1.28E-02	2.04E-02	1.72E-03	9.36E-03	1.41E-02	1.46E-03	6.33E-03	100%
M10-M7-FOX	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.45E-02	6.48E-03	7.91E-04	2.85E-03	6.57E-03	1.11E-03	2.73E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.32E-02	1.49E-02	1.66E-02	1.32E-03	7.63E-03	1.69E-02	1.67E-03	7.60E-03	100%
M10-M7-OD	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.44E-02	6.90E-03	8.71E-04	3.01E-03	6.38E-03	1.11E-03	2.63E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.36E-02	1.46E-02	1.79E-02	1.45E-03	8.20E-03	1.66E-02	1.67E-03	7.44E-03	100%
M10-M8-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	8.49E-03	3.25E-03	2.62E-03	1.69E-02	7.63E-03	4.66E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.15E-01	2.92E-02	1.92E-02	3.25E-03	7.98E-03	3.78E-02	7.63E-03	1.51E-02	100%
M10-M8-OD	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	9.04E-03	3.51E-03	2.76E-03	1.68E-02	7.63E-03	4.57E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.16E-01	2.88E-02	2.05E-02	3.51E-03	8.51E-03	3.76E-02	7.63E-03	1.50E-02	100%
M10-M9-FOX	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.52E-01	6.15E-03	2.45E-03	1.85E-03	4.33E-02	2.32E-02	1.00E-02	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.25E-02	1.41E-02	2.45E-03	5.82E-03	9.39E-02	2.32E-02	3.53E-02	100%
M10-M9-OD	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.52E-01	6.46E-03	2.60E-03	1.93E-03	4.31E-02	2.32E-02	9.96E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.23E-02	1.48E-02	2.60E-03	6.12E-03	9.36E-02	2.32E-02	3.52E-02	100%
M10-M1-PO1(OD)	0.08	0.08	0.0875	0.0745	1.89E-01	2.38E-01	9.91E-02	3.79E-02	1.47E-02	1.16E-02	1.38E-03	5.72E-04	4.03E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.24E-01	2.73E-03	1.14E-01	2.56E-02	4.42E-02	4.60E-03	9.22E-04	1.84E-03	100%
M10-M1-PO1(FOX)	0.08	0.08	0.0875	0.0745	1.89E-01	2.39E-01	9.82E-02	4.13E-02	1.64E-02	1.24E-02	1.36E-03	5.72E-04	3.93E-04	100%
	0.08	1.5	0.1461	1.4349	9.26E-02	1.30E-01	2.54E-03	1.21E-01	2.87E-02	4.60E-02	4.47E-03	9.22E-04	1.77E-03	100%
M10-M2-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.06E-02	1.79E-02	4.60E-03	6.63E-03	2.07E-03	6.51E-04	7.11E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.74E-02	6.18E-03	5.80E-02	7.66E-03	2.52E-02	7.03E-03	9.73E-04	3.03E-03	100%
M10-M2-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.05E-02	1.82E-02	4.75E-03	6.73E-03	2.05E-03	6.51E-04	7.00E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.82E-02	6.04E-03	5.92E-02	7.92E-03	2.56E-02	6.97E-03	9.73E-04	3.00E-03	100%
M10-M3-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.25E-02	2.52E-03	5.01E-03	2.72E-03	7.10E-04	1.00E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.62E-02	8.87E-03	3.97E-02	4.20E-03	1.77E-02	8.79E-03	1.06E-03	3.86E-03	100%
M10-M3-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.27E-02	2.57E-03	5.05E-03	2.70E-03	7.10E-04	9.95E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.64E-02	8.77E-03	4.02E-02	4.28E-03	1.79E-02	8.75E-03	1.06E-03	3.85E-03	100%
M10-M4-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.30E-02	1.01E-02	1.74E-03	4.19E-03	3.39E-03	7.81E-04	1.31E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.21E-02	1.06E-02	3.04E-02	2.90E-03	1.38E-02	1.04E-02	1.17E-03	4.61E-03	100%
M10-M4-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.30E-02	1.02E-02	1.76E-03	4.22E-03	3.38E-03	7.81E-04	1.30E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.22E-02	1.06E-02	3.07E-02	2.93E-03	1.39E-02	1.04E-02	1.17E-03	4.59E-03	100%
M10-M5-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.34E-02	8.59E-03	1.33E-03	3.63E-03	4.11E-03	8.67E-04	1.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.04E-02	1.18E-02	2.48E-02	2.21E-03	1.13E-02	1.21E-02	1.30E-03	5.39E-03	100%
M10-M5-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	8.63E-03	1.34E-03	3.65E-03	4.10E-03	8.67E-04	1.62E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.05E-02	1.17E-02	2.50E-02	2.23E-03	1.14E-02	1.20E-02	1.30E-03	5.38E-03	100%
M10-M6-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.35E-02	7.52E-03	1.07E-03	3.22E-03	4.95E-03	9.75E-04	1.99E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.03E-02	1.26E-02	2.10E-02	1.79E-03	9.61E-03	1.40E-02	1.46E-03	6.28E-03	100%
M10-M6-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.35E-02	7.55E-03	1.08E-03	3.24E-03	4.94E-03	9.75E-04	1.98E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.04E-02	1.26E-02	2.11E-02	1.80E-03	9.67E-03	1.40E-02	1.46E-03	6.27E-03	100%
M10-M7-PO1(OD)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.44E-02	7.04E-03	8.99E-04	3.07E-03	6.31E-03	1.11E-03	2.60E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.37E-02	1.45E-02	1.83E-02	1.50E-03	8.40E-03	1.64E-02	1.67E-03	7.39E-03	100%
M10-M7-PO1(FOX)	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.44E-02	7.07E-03	9.05E-04	3.08E-03	6.30E-03	1.11E-03	2.59E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.37E-02	1.44E-02	1.84E-02	1.51E-03	8.44E-03	1.64E-02	1.67E-03	7.38E-03	100%
M10-M8-	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	9.22E-03	3.60E-03	2.81E-03	1.67E-02	7.63E-03	4.54E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
PO1(OD)														
	0.36	2	0.405	1.955	2.20E-02	1.16E-01	2.87E-02	2.10E-02	3.60E-03	8.70E-03	3.75E-02	7.63E-03	1.49E-02	100%
M10-M8-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	9.26E-03	3.62E-03	2.82E-03	1.67E-02	7.63E-03	4.54E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.16E-01	2.87E-02	2.11E-02	3.62E-03	8.73E-03	3.75E-02	7.63E-03	1.49E-02	100%
M10-M9-PO1(OD)	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.52E-01	6.57E-03	2.65E-03	1.96E-03	4.31E-02	2.32E-02	9.93E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.22E-02	1.51E-02	2.65E-03	6.22E-03	9.35E-02	2.32E-02	3.52E-02	100%
M10-M9-PO1(FOX)	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.52E-01	6.59E-03	2.66E-03	1.96E-03	4.31E-02	2.32E-02	9.92E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.22E-02	1.51E-02	2.66E-03	6.24E-03	9.35E-02	2.32E-02	3.52E-02	100%
M10-M2-M1	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.65E-02	1.33E-02	1.16E-02	1.68E-03	6.51E-04	5.14E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.12E-01	3.19E-03	1.01E-01	2.22E-02	3.92E-02	5.44E-03	9.73E-04	2.23E-03	100%
M10-M3-M1	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.61E-02	3.93E-03	6.08E-03	2.34E-03	7.10E-04	8.13E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.39E-02	6.70E-03	5.26E-02	6.56E-03	2.30E-02	7.92E-03	1.06E-03	3.43E-03	100%
M10-M4-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.25E-02	1.18E-02	2.31E-03	4.76E-03	3.05E-03	7.81E-04	1.13E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.52E-02	9.17E-03	3.71E-02	3.85E-03	1.66E-02	9.77E-03	1.17E-03	4.30E-03	100%
M10-M5-M1	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.31E-02	9.66E-03	1.63E-03	4.01E-03	3.80E-03	8.67E-04	1.47E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.20E-02	1.08E-02	2.89E-02	2.72E-03	1.31E-02	1.16E-02	1.30E-03	5.13E-03	100%
M10-M6-M1	0.09	0.09	0.09	0.09	1.67E-01	1.99E-01	9.33E-02	8.29E-03	1.26E-03	3.51E-03	4.66E-03	9.75E-04	1.84E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.13E-02	1.20E-02	2.38E-02	2.11E-03	1.08E-02	1.36E-02	1.46E-03	6.05E-03	100%
M10-M7-M1	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.42E-02	7.67E-03	1.03E-03	3.32E-03	6.04E-03	1.11E-03	2.46E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.43E-02	1.40E-02	2.03E-02	1.72E-03	9.29E-03	1.60E-02	1.67E-03	7.18E-03	100%
M10-M8-M1	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.51E-01	1.00E-02	4.01E-03	3.02E-03	1.65E-02	7.63E-03	4.43E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.17E-01	2.82E-02	2.30E-02	4.01E-03	9.51E-03	3.72E-02	7.63E-03	1.48E-02	100%
M10-M9-M1	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	7.02E-03	2.86E-03	2.08E-03	4.28E-02	2.32E-02	9.82E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.53E-01	2.20E-02	1.62E-02	2.86E-03	6.65E-03	9.32E-02	2.32E-02	3.50E-02	100%
M10-M3-M2	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.47E-02	3.64E-02	1.33E-02	1.16E-02	1.82E-03	7.10E-04	5.55E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.14E-03	1.00E-01	2.22E-02	3.91E-02	5.91E-03	1.06E-03	2.42E-03	100%
M10-M4-M2	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.11E-02	1.60E-02	3.93E-03	6.02E-03	2.55E-03	7.81E-04	8.82E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.41E-02	6.59E-03	5.23E-02	6.56E-03	2.29E-02	8.64E-03	1.17E-03	3.74E-03	100%
M10-M5-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.24E-02	1.17E-02	2.31E-03	4.70E-03	3.35E-03	8.67E-04	1.24E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.57E-02	9.05E-03	3.69E-02	3.85E-03	1.65E-02	1.08E-02	1.30E-03	4.73E-03	100%
M10-M6-M2	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.29E-02	9.61E-03	1.63E-03	3.99E-03	4.25E-03	9.75E-04	1.64E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.31E-02	1.08E-02	2.87E-02	2.72E-03	1.30E-02	1.29E-02	1.46E-03	5.71E-03	100%
M10-M7-M2	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.40E-02	8.68E-03	1.26E-03	3.71E-03	5.64E-03	1.11E-03	2.26E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.54E-02	1.32E-02	2.37E-02	2.11E-03	1.08E-02	1.54E-02	1.67E-03	6.87E-03	100%
M10-M8-M2	0.36	0.36	0.405	0.315	2.21E-02	3.28E-01	1.50E-01	1.13E-02	4.67E-03	3.34E-03	1.62E-02	7.63E-03	4.27E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.18E-01	2.74E-02	2.63E-02	4.67E-03	1.08E-02	3.69E-02	7.63E-03	1.46E-02	100%
M10-M9-M2	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	7.68E-03	3.19E-03	2.25E-03	4.25E-02	2.32E-02	9.66E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.54E-01	2.17E-02	1.78E-02	3.19E-03	7.29E-03	9.27E-02	2.32E-02	3.48E-02	100%
M10-M4-M3	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.63E-02	1.33E-02	1.15E-02	1.99E-03	7.81E-04	6.05E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.08E-03	1.00E-01	2.22E-02	3.89E-02	6.47E-03	1.17E-03	2.65E-03	100%
M10-M5-M3	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.10E-02	1.59E-02	3.93E-03	5.97E-03	2.80E-03	8.67E-04	9.68E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.46E-02	6.50E-03	5.21E-02	6.56E-03	2.27E-02	9.53E-03	1.30E-03	4.11E-03	100%
M10-M6-M3	0.09	0.09	0.09	0.09	1.67E-01	2.00E-01	9.23E-02	1.17E-02	2.31E-03	4.69E-03	3.75E-03	9.75E-04	1.39E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.68E-02	9.10E-03	3.66E-02	3.85E-03	1.64E-02	1.20E-02	1.46E-03	5.26E-03	100%
M10-M7-M3	0.09	0.09	0.09	0.09	1.67E-01	2.02E-01	9.36E-02	1.01E-02	1.63E-03	4.24E-03	5.16E-03	1.11E-03	2.02E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	6.73E-02	1.20E-02	2.86E-02	2.72E-03	1.30E-02	1.47E-02	1.67E-03	6.51E-03	100%
M10-M8-M3	0.36	0.36	0.405	0.315	2.21E-02	3.29E-01	1.50E-01	1.31E-02	5.59E-03	3.76E-03	1.58E-02	7.63E-03	4.10E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.20E-01	2.63E-02	3.07E-02	5.59E-03	1.26E-02	3.65E-02	7.63E-03	1.44E-02	100%
M10-M9-M3	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	8.50E-03	3.59E-03	2.46E-03	4.22E-02	2.32E-02	9.48E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.54E-01	2.12E-02	1.98E-02	3.59E-03	8.08E-03	9.22E-02	2.32E-02	3.45E-02	100%
M10-M5-M4	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.46E-02	3.62E-02	1.33E-02	1.15E-02	2.20E-03	8.67E-04	6.67E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.13E-01	3.04E-03	9.98E-02	2.22E-02	3.88E-02	7.14E-03	1.30E-03	2.92E-03	100%
M10-M6-M4	0.09	0.09	0.09	0.09	1.67E-01	2.01E-01	9.09E-02	1.59E-02	3.93E-03	5.98E-03	3.16E-03	9.75E-04	1.09E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.56E-02	6.57E-03	5.18E-02	6.56E-03	2.26E-02	1.06E-02	1.46E-03	4.59E-03	100%
M10-M7-M4	0.09	0.09	0.09	0.09	1.67E-01	2.03E-01	9.29E-02	1.23E-02	2.31E-03	5.01E-03	4.59E-03	1.11E-03	1.74E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.10E-02	1.02E-02	3.67E-02	3.85E-03	1.64E-02	1.37E-02	1.67E-03	6.03E-03	100%
M10-M8-M4	0.36	0.36	0.405	0.315	2.21E-02	3.29E-01	1.49E-01	1.57E-02	6.96E-03	4.36E-03	1.55E-02	7.63E-03	3.92E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.23E-01	2.48E-02	3.71E-02	6.96E-03	1.51E-02	3.61E-02	7.63E-03	1.42E-02	100%
M10-M9-M4	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	9.52E-03	4.11E-03	2.71E-03	4.18E-02	2.32E-02	9.27E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.55E-01	2.06E-02	2.22E-02	4.11E-03	9.07E-03	9.16E-02	2.32E-02	3.42E-02	100%
M10-M6-M5	0.09	0.09	0.09	0.09	1.67E-01	2.08E-01	8.45E-02	3.63E-02	1.33E-02	1.15E-02	2.48E-03	9.75E-04	7.53E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.14E-01	3.14E-03	9.95E-02	2.22E-02	3.86E-02	7.99E-03	1.46E-03	3.27E-03	100%
M10-M7-M5	0.09	0.09	0.09	0.09	1.67E-01	2.04E-01	9.15E-02	1.68E-02	3.93E-03	6.43E-03	3.89E-03	1.11E-03	1.39E-03	100%
	0.09	1.5	0.141	1.449	8.46E-02	7.97E-02	7.65E-03	5.22E-02	6.56E-03	2.28E-02	1.23E-02	1.67E-03	5.30E-03	100%
M10-M8-M5	0.36	0.36	0.405	0.315	2.21E-02	3.30E-01	1.48E-01	1.98E-02	9.23E-03	5.29E-03	1.51E-02	7.63E-03	3.73E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.28E-01	2.28E-02	4.70E-02	9.23E-03	1.89E-02	3.56E-02	7.63E-03	1.40E-02	100%
M10-M9-M5	0.36	0.36	0.405	0.315	2.21E-02	3.53E-01	1.51E-01	1.09E-02	4.81E-03	3.02E-03	4.13E-02	2.32E-02	9.03E-03	100%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.36	2	0.405	1.955	2.20E-02	1.56E-01	1.99E-02	2.55E-02	4.81E-03	1.04E-02	9.09E-02	2.32E-02	3.39E-02	100%
M10-M7-M6	0.09	0.09	0.09	0.09	1.67E-01	2.11E-01	8.50E-02	3.77E-02	1.33E-02	1.22E-02	3.05E-03	1.11E-03	9.67E-04	100%
	0.09	1.5	0.141	1.449	8.46E-02	1.18E-01	3.93E-03	1.01E-01	2.22E-02	3.93E-02	9.33E-03	1.67E-03	3.83E-03	100%
M10-M8-M6	0.36	0.36	0.405	0.315	2.21E-02	3.33E-01	1.45E-01	2.78E-02	1.37E-02	7.06E-03	1.47E-02	7.63E-03	3.55E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.39E-01	1.98E-02	6.45E-02	1.37E-02	2.54E-02	3.49E-02	7.63E-03	1.36E-02	100%
M10-M9-M6	0.36	0.36	0.405	0.315	2.21E-02	3.54E-01	1.50E-01	1.27E-02	5.79E-03	3.44E-03	4.07E-02	2.32E-02	8.76E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.58E-01	1.88E-02	3.00E-02	5.79E-03	1.21E-02	9.02E-02	2.32E-02	3.35E-02	100%
M10-M8-M7	0.36	0.36	0.405	0.315	2.21E-02	3.43E-01	1.39E-01	5.03E-02	2.66E-02	1.19E-02	1.44E-02	7.63E-03	3.38E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.68E-01	1.52E-02	1.04E-01	2.66E-02	3.88E-02	3.35E-02	7.63E-03	1.29E-02	100%
M10-M9-M7	0.36	0.36	0.405	0.315	2.21E-02	3.54E-01	1.49E-01	1.53E-02	7.28E-03	4.01E-03	4.01E-02	2.32E-02	8.45E-03	100%
	0.36	2	0.405	1.955	2.20E-02	1.61E-01	1.74E-02	3.65E-02	7.28E-03	1.46E-02	8.93E-02	2.32E-02	3.30E-02	100%
M10-M9-M8	0.36	0.36	0.405	0.315	2.21E-02	3.67E-01	1.40E-01	4.84E-02	2.66E-02	1.09E-02	3.85E-02	2.32E-02	7.66E-03	100%
	0.36	2	0.405	1.955	2.20E-02	2.01E-01	8.81E-03	9.95E-02	2.66E-02	3.65E-02	8.41E-02	2.32E-02	3.04E-02	100%

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12.15 MIM Capacitor Model

Please refer to T-N65-CM-SP-007.

12.15.1 Model Usage Guide

Two types of metal-insulator-metal (MIM) capacitor, with and without underlying metal, are modeled based on the two-port S-parameter measurement and Y-parameter fitting. Capacitance density of 1.0fF/μm^2, 1.5fF/μm^2 and 2.0fF/μm^2 are supported for both MIM types, which can be fabricated with processes 1PM4 to 1PM9. We use mimflag to select capacitance density, whose selection are minflag=1 for 1.0fF/μm^2, minflag=2 for 1.5fF/μm^2, and minflag=3 for 2.0fF/μm^2. Moreover, process for MiM capacitor with UTM direct contact (UDC) is allowed to use the metal scheme from M4 to M8.

Measurement data come from seven MIM capacitor testers of areas (width (WT) x length (LT)), 4x4, 10x10, 20x20, 30x30, 4x100, 30x100, and 100x100, all in μm^2. In addition, there are another seven MiM capacitors with UTM direct contact (UDC) of areas 4x4, 10x10, 20x20, 30x30, 4x25, 4x100, and 100x100 (all in μm^2) are characterized. The convention in area specification is to have the length larger than or equal to width. Scalable models are generated for capacitors of areas with both the width and length in the range from 4μm to 100μm.

EXAMPLE

To use a MIM capacitor of area 10x10 μm^2 and density 2.0fF/μm^2 with underneath metal (node “um”):

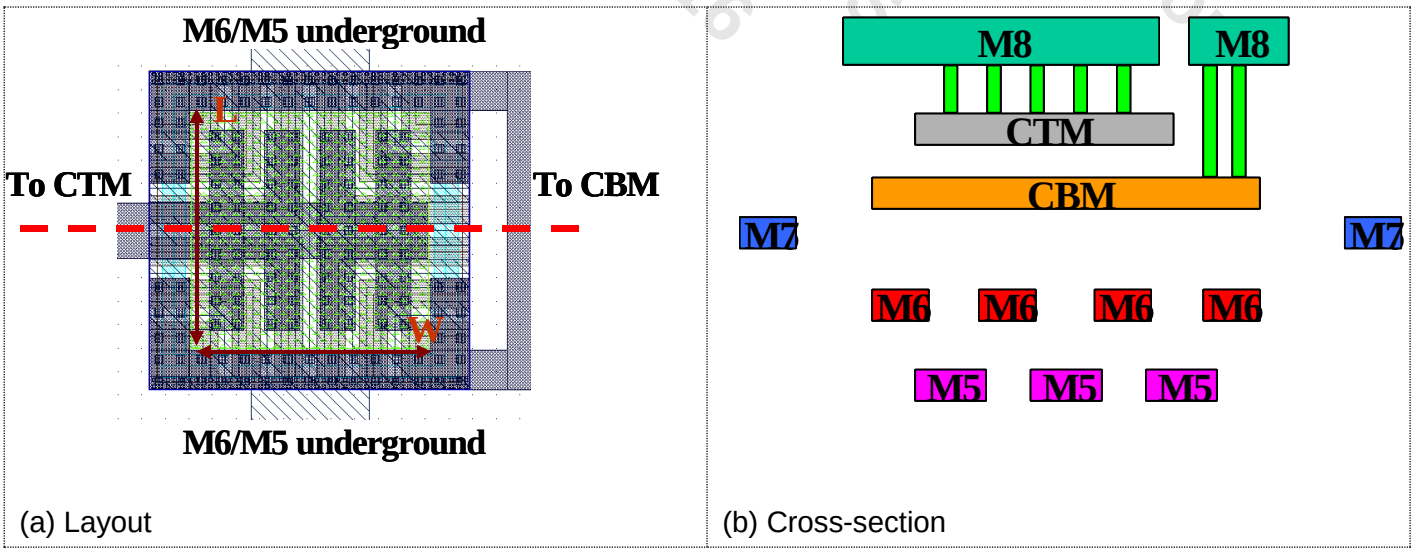
X1_mimcap1 top bottom um mimcap_um_sin_rf lt=10u wt=10u mimflag=3

To use a MIM capacitor of area 10x10 μm^2 and density 2.0fF/μm^2 without underneath metal:

X2_mimcap2 top bottom mimcap_woum_sin_rf lt=10u wt=10u mimflag=3

12.15.2 Test Structure and Measurement Procedures

The layout in Fig. 12.15.1 (a) and the cross-section view in Fig. 12.15.1 (b) show the structure of a MIM capacitor, using top metal layer M8 and underlying metals M5 and M6, which are normally tied to the ground node. The same MIM capacitor less the underlying metals are shown in Fig. 12.15.2. To characterize the MIM capacitors, two-port S-parameter measurements have been performed with a frequency of from 200 MHz to 30.0 GHz. Open and short test structure measurements are used as RF de-embedding for each MIM.



(a) Layout (b) Cross-section

Fig. 12.15.1: (a) Layout and (b) Cross-section of a MIM capacitor with M5 and M4 as the underlying metal.

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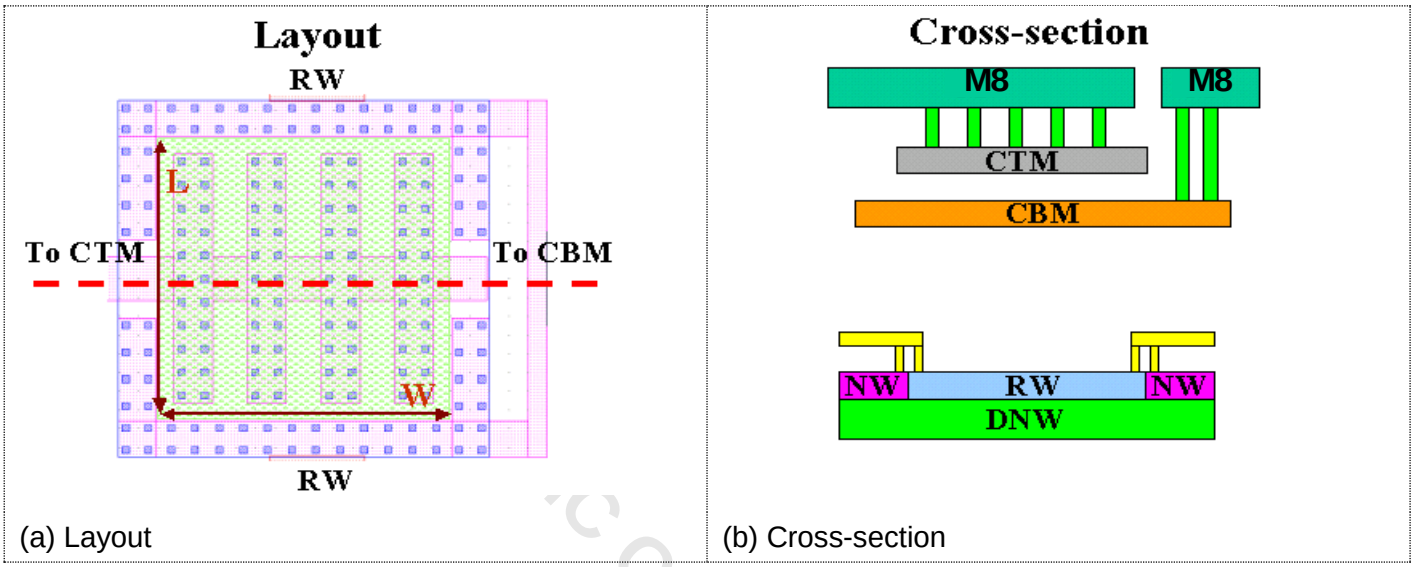

Fig. 12.15.2: (a) Layout and (b) Cross-section of a MIM capacitor without underlying metal.

12.15.3 Equivalent Circuit Model

The equivalent circuit model for the MIM capacitor with underlying metal is shown in Fig. 12.15.3. Circuit elements are described in the following:

- Cmim models the main element of the capacitor due to the inter-metal dielectric material
- Rtop and Ltop are the parasitic resistance and inductance of the top plate (port 1)
- Rbot and Lbot are the parasitic resistance and inductance of the bottom plate (port 2)
- Cox represents the capacitance between the bottom-plate to the underlying metal

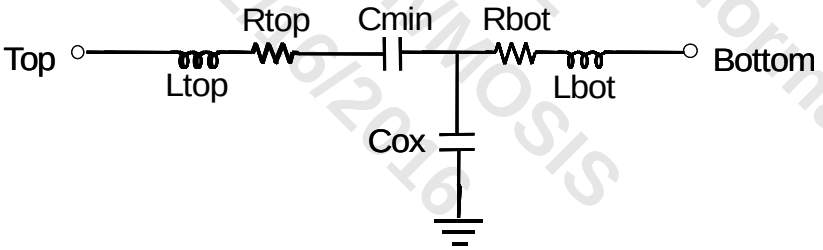

Fig. 12.15.3: Equivalent circuit of the MIM capacitor with underlying metal.

The equivalent circuit model for the MIM capacitor without the underlying metal is shown in Fig. 12.15.4. Circuit elements are same as those in Fig. 12.15.3, with two additional elements:

- Rsub and Csub are parasitic resistance and capacitance from the substrate

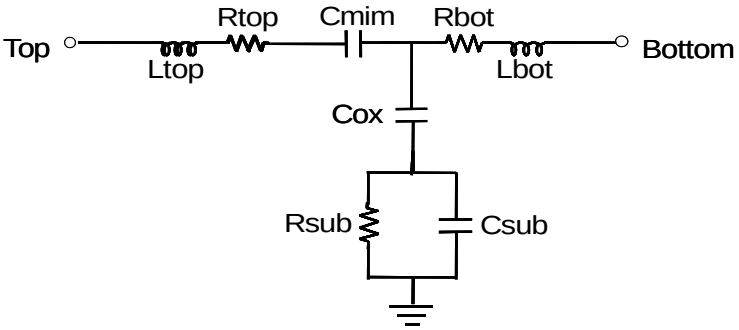

Fig. 12.15.4: Equivalent circuit of the MIM capacitor without underlying metal.

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12.15.4 Model Details

12.15.4.1 Scaling Rule

The scaling equations for the equivalent circuit elements just described, which are empirically determined, are shown for the MIMCAP and UDC MIMCAP in Table 12.15.1, and Table 12.15.2, respectively.

The scaling equations for the equivalent circuit elements just described, which are empirically determined, are shown for the MIMCAP in Table 12.15.1.

Table 12.15.1 Scaling equations for the equivalent circuit elements of MIMCAP with and without underlying metal.

L_{top} (H)	ltop_para
R_{top} (Ω)	rtop_para·(0.003·(temper-25)+1)
C_{mim} (F)	cmim_para·(1+v(n2,n3)·vcc1+(abs(v(n2,n3))^2)·vcc2)·cmim_corner
R_{bot} (Ω)	rbot_para·(0.003·(temper-25)+1)
L_{bot} (H)	lbot_para
C_{ox} (F)	cox_para·((1/(4.35717+(1.42106)·(lay-2)))/0.0872414)
C_{sub} (F)	csub_para
R_{sub} (Ω)	rsub_para
where,	
mis	((mismatchflag-1)·(mismatchflag-2)·(mismatchflag-3)/(0-1)/(0-2)/(0-3)·(0)+(mismatchflag-0) ·(mismatchflag-2)·(mismatchflag-3)/(1-0)/(1-2)/(1-3)·(0.007083)+(mismatchflag-0)·(mismatchflag-1)·(mismatchflag-3)/(2-0)/(2-1)/(2-3)·(0.006203)+(mismatchflag-0)·(mismatchflag-1)*(mismatchflag-2)/(3-0)/(3-1)/(3-2)*(0.006082))
geo_fac	1/sqrt((lt·scale)·(wt·scale)·1e12)
factmis	mis·geo_fac
ltop_para	((0.24·((wt·scale)·1e6)·(log(((wt·scale)·1e6)/((lt·scale)·1e6+0.08))+1.19+0.022·((lt·scale)·1e6+0.08)/((wt·scale)·1e6))/1+1.5)/3+3.6)·1e-12
lbot_cbm	((0.24·((wt·scale)·1e6+3.52)·(log(((wt·scale)·1e6+3.52)/(((lt·scale)·1e6+3.52)+0.2))+1.19+0.022 ·(((lt·scale)·1e6+3.52)+0.2)/((wt·scale)·1e6+3.52))/1+1.5)/3+3.6)·1e-12
lbot_lead	((0.606+0.24·(((lt·scale)·1e6+3.52)/2)·(log((((lt·scale)·1e6+3.52)/2)/(1+0.9))+1.19+0.022 ·(1+0.9)/(((lt·scale)·1e6+3.52)/2))/1+1.5)/2+3.6)·1e-12
lbot_para	(lbot_cbm+lbot_lead)
via_v	int(((lt·scale)·1e6/2-1.196)/(0.91)+1)
res_v	(via_v-1)·(2·via_v-1)/(6·via_v)·0.007902299+23.975/via_v
via_h	int(((wt·scale)·1e6-3.24)/(2.69)+1)
rtop_para	(0.067902542+(via_h-1)·(2·via_h-1)/(6·via_h)·0.010063559+res_v/2/via_h+0.25)
r1	((lt·scale)·1e6+0.2)/2/((wt·scale)·1e6+0.2)·0.3/3
r3	((wt·scale)·1e6+0.2)/2/((lt·scale)·1e6+0.2)·0.3/3
rcbm	(1/(2/r1+2/r3))
via_left	int(((((wt·scale)·1e6+3.52)-0.83+(((lt·scale)·1e6+3.52)/2-2.85))-0.76)/(0.91)+1)
res_left	0.003012048+(via_left-1)·(2·via_left-1)/(6·via_left)·0.008283133+0.615/via_left
via_vert	int(((((lt·scale)·1e6+3.52)/2-2.85)-0.76)/(0.91)+1)
res_vert	0.003012048+(via_vert-1)·(2·via_vert-1)/(6·via_vert)·0.008283133+0.615/via_vert
res_cbm	1/(1/res_left+1/res_vert)
res_lead	(2/1.66+((lt·scale)·1e6+3.52)/2/1.66)·0.025
res_upper	res_cbm+res_lead
rbot_para	(res_upper/2+rcbm+0.25)
mim_a	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(-0.029u)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3) ·(-0.049u)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-0.037u))
mim_b	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(1.03)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3) ·(1.485)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(2.014))
mim_c	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(0.207)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3) ·(0.21)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(0.218))

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mim_d	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(0.193)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(0.193)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(0.193))
tcc1	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(-5.11e-5)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(-5.365e-5)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-1.573e-5))
tcc2	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(-0.03e-6)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(-0.052e-6)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-0.018e-6))
vcc1	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(3.66e-5)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(4.335e-5)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-2.9e-5))
vcc2	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(-1.84e-5)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(-4.23e-5)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-2.97e-5))
cmim_corner	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(cmim_mimfac)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(cmim_mimfac)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(cmim2p0_mimfac))
cmim_para	(1+factmis)·((((wt·scale)+mim_a)·((lt·scale)+mim_a)·1e12·mim_b)+2·(((wt·scale)+mim_a)+((lt·scale)+mim_a))·1e6·mim_c+mim_d)·1e-15·(1+(temper-25)·tcc1+(temper-25)·(temper-25)·tcc2)
cox_para	(((lt·scale)·1e6+3.52)·((wt·scale)·1e6+3.52)·0.0105357+0.04382+((lt·scale)·1e6+3.52)·0.0066)·1e-15
rsub_para	(1/(2/(((lt·scale)·1e6+3.52)/2/((wt·scale)·1e6+3.52)·1100/3)+2/(((wt·scale)·1e6+3.52)/2/((lt·scale)·1e6+3.52)·1100/3)))·(-0.0000114365·(temper-25)·(temper-25)+0.0045985091·(temper-25)+1)
csub_para	(312/rsub_para)·1e-15 For MIMcap without underlying metal

Table 12.15.2 Scaling equations for the equivalent circuit elements of MIMCAP with and without underlying metal.

L_{top} (H)	ltop_para
R_{top} (Ω)	rtop_para·(0.003·(temper-25)+1)
C_{mim} (F)	cmim_para·(1+v(n2,n3)·vcc1+(abs(v(n2,n3))^2)·vcc2)·cmim_corner
R_{bot} (Ω)	rbot_para·(0.003·(temper-25)+1)
L_{bot} (H)	lbot_para
C_{ox} (F)	cox_para·((1/(4.35717+(1.42106)·(lay-2)))/0.0872414)
C_{sub} (F)	csub_para
R_{sub} (Ω)	rsub_para
where,	
mis	((mismatchflag-1)·(mismatchflag-2)·(mismatchflag-3)/(0-1)/(0-2)/(0-3)·(0)+(mismatchflag-0)·(mismatchflag-2)·(mismatchflag-3)/(1-0)/(1-2)/(1-3)·(0.007083)+(mismatchflag-0)·(mismatchflag-1)·(mismatchflag-3)/(2-0)/(2-1)/(2-3)·(0.006203)+(mismatchflag-0)·(mismatchflag-1)*(mismatchflag-2)/(3-0)/(3-1)/(3-2)*(0.006082))
geo_fac	1/sqrt((lt·scale)·(wt·scale)·1e12)
factmis	mis·geo_fac
ltop_para	((0.24·((wt·scale)·1e6)·(log(((wt·scale)·1e6)/((lt·scale)·1e6+0.08))+1.19+0.022·((lt·scale)·1e6+0.08)/((wt·scale)·1e6))/1+1.5)/3+3.6)·1e-12
lbot_cbm	((0.24·((wt·scale)·1e6+7.84)·(log(((wt·scale)·1e6+7.84)/(((lt·scale)·1e6+7.84)+0.2))+1.19+0.022·(((lt·scale)·1e6+7.84)+0.2)/((wt·scale)·1e6+7.84))/1)/3)·1e-12
lbot_lead	((0.606+0.24·(((lt·scale)·1e6+7.84)/2)·(log((((lt·scale)·1e6+7.84)/2)/(2+3.4))+1.19+0.022·(2+3.4)/(((lt·scale)·1e6+7.84)/2))/1)/2)·1e-12
lbot	(lbot_cbm+lbot_lead)·1e12
lbot_para	9.05445538528849·lbot$^{0.590075891297729}$·1e-12-(1.18350020828306·((lt·scale)/(wt·scale))-1)·1e-12
via_v	int(((lt·scale)·1e6/2-0.7)/(0.9)+1)
res_v	(via_v-1)·(2·via_v-1)/(6·via_v)·0.0009712230216+23.975/via_v
via_h	int(((wt·scale)·1e6-3.075)/(5.385)+1)
rtop	(0.0170868644+(via_h-1)·(2·via_h-1)/(6·via_h)·0.0055190678+res_v/2/via_h)
rtop_para	1.06872158·rtop$^{0.697186362}$
r1	((lt·scale)·1e6+3.72)/2/((wt·scale)·1e6+3.72)·0.26/3
r3	((wt·scale)·1e6+3.72)/2/((lt·scale)·1e6+3.72)·0.26/3
rcbm	(1/(2/r1+2/r3))
via_left	int(((((wt·scale)·1e6+7.84)-1.03+(((lt·scale)·1e6+7.84)/2-4.21))-1.16)/(0.9)+1)
res_left	0.0009708737864/2+(via_left-1)·(2·via_left-1)/(6·via_left)·0.0013106796+0.615/via_left
via_vert	int(((((lt·scale)·1e6+7.84)/2-4.21)-1.16)/(0.9)+1)
res_vert	0.0009708737864/2+(via_vert-1)·(2·via_vert-1)/(6·via_vert)·0.0013106796+0.615/via_vert
res_cbm	1/(1/res_left+1/res_vert)

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res_lead	(2/2.06+((lt·scale)·1e6+7.84)/2/2)·0.005
res_upper	res_cbm+res_lead
rbot_para	(res_upper/2+rcbm+0.25)
mim_a	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(-0.029u)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(-0.049u)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-0.037u))
mim_b	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(1.03)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(1.485)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(2.014))
mim_c	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(0.207)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(0.21)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(0.218))
mim_d	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(0.199)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(0.199)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(0.199))
tcc1	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(-5.11e-5)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(-5.365e-5)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-1.573e-5))
tcc2	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(-0.03e-6)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(-0.052e-6)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-0.018e-6))
vcc1	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(3.66e-5)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(4.335e-5)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-2.9e-5))
vcc2	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(-1.84e-5)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(-4.23e-5)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(-2.97e-5))
cmim_corner	((mimflag-2)·(mimflag-3)/(1-2)/(1-3)·(cmim_mimfac)+(mimflag-1)·(mimflag-3)/(2-1)/(2-3)·(cmim_mimfac)+(mimflag-1)·(mimflag-2)/(3-1)/(3-2)·(cmim2p0_mimfac))
cmim_para	(1+factmis)·((((wt·scale)+mim_a)·((lt·scale)+mim_a)·1e12·mim_b)+2·(((wt·scale)+mim_a)+((lt·scale)+mim_a))·1e6·mim_c+mim_d)·1e-15·(1+(temper-25)·tcc1+(temper-25)·(temper-25)·tcc2)
cox_para	(((lt·scale)·1e6+7.84)·((wt·scale)·1e6+7.84)·0.0105357+0.04382+((lt·scale)·1e6+7.84)·0.0066)·1e-15
rsub_para	(1/(2/(((lt·scale)·1e6+7.84)/2/((wt·scale)·1e6+7.84)·1100/3)+2/(((wt·scale)·1e6+7.84)/2/((lt·scale)·1e6+7.84)·1100/3)))·(-0.0000114365·(temper-25)·(temper-25)+0.0045985091·(temper-25)+1)
csub_para	(312/rsub_para)·1e-15

12.15.4.2Model Parameter

Values of the equivalent circuit elements for the seven MIMCAP and UDC MIMCAP testers with underlying metal are shown in Table 12.15.3, and Table 12.15.4, respectively. These are used as the bases to derive the models for the MIMCAP without underlying metal. For instance, models for the 1.5fF/μm^2 MIMCAP without underlying metal are generated based on those of the same MIMCAP with underlying metal, but replacing the ground node with the substrate of the 1.5 fF/μm^2 MIMCAP without underlying metal.

Lt(μm)	4	10	20	30	100	100	100
Wt(μm)	4	10	20	30	100	4	30
L_{top}(pH)	4.48	5.06	6.03	7.00	13.79	3.63	4.24
R_{top}(Ω)	12.31	1.12	0.51	0.42	0.44	0.61	0.38
R_{bot}(mΩ)	348.17	355.98	391.29	430.25	725.83	697.49	710.03
L_{bot}(pH)	10.32	12.05	15.28	18.77	46.70	36.00	37.02
C_{ox}(fF)	0.69	2.06	6.03	12.10	113.63	8.93	37.29
C_{sub}(fF)	6.81	6.81	6.81	6.81	6.81	47.10	11.61
R_{sub}(Ω)	45.83	45.83	45.83	45.83	45.83	6.62	26.87

Table 12.15.3: Equivalent circuit parameters for MIMCAP with underlying metal.

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Lt(µm)	4	10	20	30	100	4	4
Wt(µm)	4	10	20	30	100	25	100
L_{top}(pH)	4.482	5.063	6.033	7.003	13.79	10.113	39.22
R_{top}(Ω)	3.732	1.226	0.456	0.286	0.15	1.229	0.545
R_{bot}(mΩ)	294.989	289.231	291.575	296.825	342.742	280.76	287.676
L_{bot}(pH)	14.846	19.853	27.315	34.039	71.526	29.384	68.892
C_{ox}(fF)	1.599	3.515	8.393	15.379	123.28	4.219	13.574
C_{sub}(fF)	6.807	6.807	6.807	6.807	6.807	10.668	31.374
R_{sub}(Ω)	45.833	45.833	45.833	45.833	45.833	29.247	9.944

Table 12.15.4: Equivalent circuit parameters for UDC MIMCAP with underlying metal.

12.15.4.3 Model Error Table

Fitting errors are obtained by fitting the real and imaginary parts of the four Y-parameters according to the equations given in Chapter 13 of T-N65-CM-SP-007. Fitting errors for MIMCAPs and UDC MIMCAPs with underlying metal are shown in Tables 12.15.5,12.15.6 and Tables 12.15.9 . Fitting errors for MIMCAPs and UDC MIMCAPs without underlying metal are shown in Tables 12.15.7, 12.15.8 and Tables 12.15.10 .

W(µm)	4	10	20	30	100	4	30
L(µm)	4	10	20	30	100	100	100
Real(Y11)(%)	16.07	10.70	12.37	17.13	10.43	6.20	4.85
Real(Y21)(%)	12.42	8.99	12.41	18.40	9.34	6.43	4.48
Real(Y12)(%)	13.49	9.84	12.25	18.47	9.41	6.30	4.52
Real(Y22)(%)	12.39	10.73	12.77	19.73	8.36	6.15	4.28
Imag(Y11)(%)	4.71	1.18	2.71	3.97	3.31	3.75	7.35
Imag(Y21)(%)	5.47	1.20	2.73	4.09	3.50	4.79	6.70
Imag(Y12)(%)	5.46	1.20	2.72	4.11	3.49	4.79	6.75
Imag(Y22)(%)	9.77	2.70	3.85	4.14	3.37	4.60	6.45

Table 12.15.5: Fitting errors (Real and Imaginary) for 1.0fF/µm² MIMCAP with underlying metal.

W(µm)	4	10	20	30	100	4	30
L(µm)	4	10	20	30	100	100	100
Real(Y11)(%)	26.57	19.74	16.92	9.71	13.45	28.40	16.92
Real(Y21)(%)	19.22	20.15	16.80	8.96	12.87	29.20	16.15
Real(Y12)(%)	18.36	20.21	16.90	8.96	12.86	29.41	16.17
Real(Y22)(%)	14.50	22.91	16.82	8.25	12.30	30.10	15.43
Imag(Y11)(%)	6.19	8.23	16.24	10.92	10.61	2.65	18.44
Imag(Y21)(%)	6.05	8.25	16.09	10.36	10.82	3.50	16.83
Imag(Y12)(%)	6.07	8.25	16.11	10.36	10.78	3.47	16.86
Imag(Y22)(%)	8.14	9.01	15.85	10.01	10.41	3.75	16.03

Table 12.15.6: Fitting errors (Real and Imaginary) for 2.0fF/µm² MIMCAP with underlying metal.

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W(μm)	4	10	20	30	100	4	30
L(μm)	4	10	20	30	100	100	100
Real(Y11)(%)	8.89	12.34	4.90	9.00	11.75	3.09	15.77
Real(Y21)(%)	15.86	13.62	4.78	9.06	11.58	3.16	15.61
Real(Y12)(%)	15.19	13.05	4.84	9.06	11.57	3.13	15.64
Real(Y22)(%)	31.48	17.68	4.78	9.11	11.32	3.38	15.47
Imag(Y11)(%)	3.58	1.21	4.36	16.39	7.50	1.89	9.61
Imag(Y21)(%)	5.97	1.28	4.33	16.47	7.56	1.92	9.53
Imag(Y12)(%)	5.96	1.28	4.33	16.44	7.55	1.90	9.55
Imag(Y22)(%)	6.41	1.89	3.85	16.26	7.42	2.16	9.63

Table 12.15.7: Fitting errors (Real and Imaginary) for 1.0fF/μm² MIMCAP without underlying metal.

W(μm)	4	10	20	30	100	4	30
L(μm)	4	10	20	30	100	100	100
Real(Y11)(%)	34.76	9.71	31.76	10.37	10.99	6.24	10.99
Real(Y21)(%)	36.87	10.81	31.61	10.33	10.86	6.35	10.86
Real(Y12)(%)	36.33	10.06	31.35	10.34	10.92	6.41	10.92
Real(Y22)(%)	11.31	9.94	31.12	10.30	10.76	6.55	10.76
Imag(Y11)(%)	5.86	3.44	9.47	14.74	11.26	7.29	11.26
Imag(Y21)(%)	6.15	3.65	9.38	14.71	11.29	7.27	11.29
Imag(Y12)(%)	6.16	3.66	9.37	14.70	11.28	7.30	11.28
Imag(Y22)(%)	7.70	4.29	9.11	14.70	11.17	7.04	11.17

Table 12.15.8: Fitting errors (Real and Imaginary) for 2.0fF/μm² MIMCAP without underlying metal.

W(μm)	4	10	20	30	100	4	4
L(μm)	4	10	20	30	100	25	100
Real(Y11)(%)	29.94	29.20	14.31	20.75	37.20	7.75	8.33
Real(Y21)(%)	37.23	28.36	14.62	21.72	37.20	12.19	8.01
Real(Y12)(%)	35.18	31.22	14.90	22.17	37.21	11.53	8.09
Real(Y22)(%)	39.36	28.24	15.17	23.13	37.16	4.63	6.00
Imag(Y11)(%)	11.05	5.08	11.42	10.37	14.28	4.74	5.30
Imag(Y21)(%)	11.74	4.11	10.84	9.86	15.03	4.74	5.31
Imag(Y12)(%)	11.77	4.15	10.87	9.91	15.01	8.16	6.07
Imag(Y22)(%)	18.71	7.11	10.77	9.64	14.78	3.75	16.03

Table 12.15.9: Fitting errors (Real and Imaginary) for 2.0fF/μm² UDC MIMCAP with underlying metal.

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W(μm)	4	10	20	30	100	4	4
L(μm)	4	10	20	30	100	25	100
Real(Y11)(%)	26.31	7.81	13.99	15.36	31.21	8.59	8.25
Real(Y21)(%)	34.67	10.52	14.68	15.44	31.20	12.04	9.01
Real(Y12)(%)	33.17	9.82	14.57	15.37	31.23	11.24	8.91
Real(Y22)(%)	33.25	13.47	15.25	15.45	31.21	15.67	9.72
Imag(Y11)(%)	8.34	3.46	7.40	4.17	6.99	3.64	8.43
Imag(Y21)(%)	9.12	3.56	7.46	4.30	6.98	3.85	8.65
Imag(Y12)(%)	9.13	3.58	7.41	4.27	6.99	3.86	8.60
Imag(Y22)(%)	12.57	4.74	7.34	4.37	6.97	5.42	8.38

Table 12.15.10: Fitting errors (Real and Imaginary) for 2.0fF/μm² UDC MIMCAP without underlying metal.

12.15.5 Corner Model Table

Table 12.15.11 lists the skew parameters for the slow-corner (SS), typical (TT) and fast-corner (FF) cases, corresponding to libraries SS_RFMIM, TT_RFMIM and FF_RFMIM.

Skew Parameter	SS	TT	FF
cm7_mimfac	1.08	1.0	0.926
cm5_mimfac	1.074	1.0	0.931
rctm_mimfac	1.1	1.0	0.9
rsub_mimfac	1.2	1.0	0.8
csub_mimfac	0.833	1.0	1.25
cmim_mimfac	1.1	1.0	0.9
cmim2p0_mimfac	1.15	1.0	0.85
l_mimfac	1.0235	1.0	0.9762

Table 12.15.11: Skew parameters for MIMCAP with and without underlying metal.

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12.15.6 Temperature Effect Model

A MIMCAP tester with area of 4x100 μm^2 is used to study the temperature characteristics. As for MiM capacitor with UTM direct contact (UDC), a UDC MIMCAP tester with area of 30x30 μm^2 is used. The parasitic resistance elements, Rtop and Rbot, show linear dependences on temperature as modeled by the following functions,

Rtop(T)=Rtop*(0.003*(temper-25)+1)

Rbot(T)=Rbot*(0.003*(temper-25)+1)

Values of the quality factor (Q) as function of frequency at temperatures -40℃, 25℃, 125℃ are shown in Fig. 12.15.5 (a), 12.15.6 (a) and 12.15.7 (a). The Q is measured up to 30 GHz, and its variations with temperature are evident, which may be due to the sensitivity of the parasitic resistances to temperature. On the other hand, the capacitance, as plotted in Fig. 12.15.5 (b), Fig. 12.15.6 (b) and Fig. 12.15.7 (b), changes little with temperature.

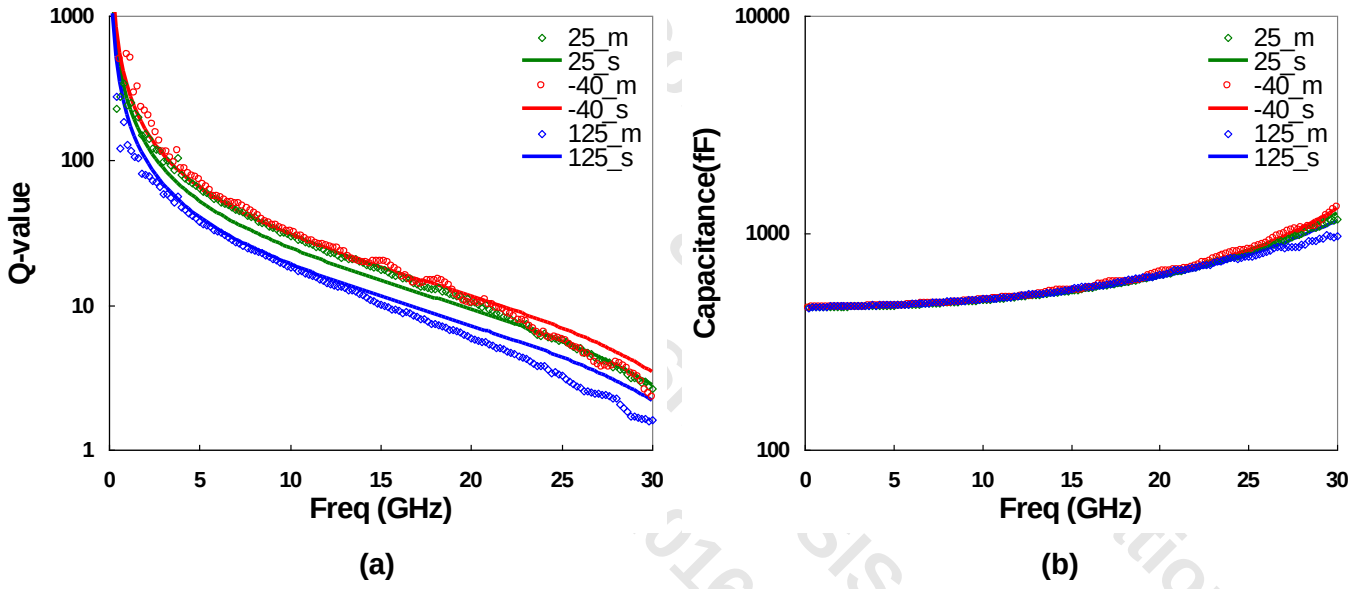

Fig. 12.15.5: Quality factor (a) and capacitance (b) versus frequency for the 1.0fF/μm^2 MIMCAP tester at 125℃, 25℃ and -40℃.

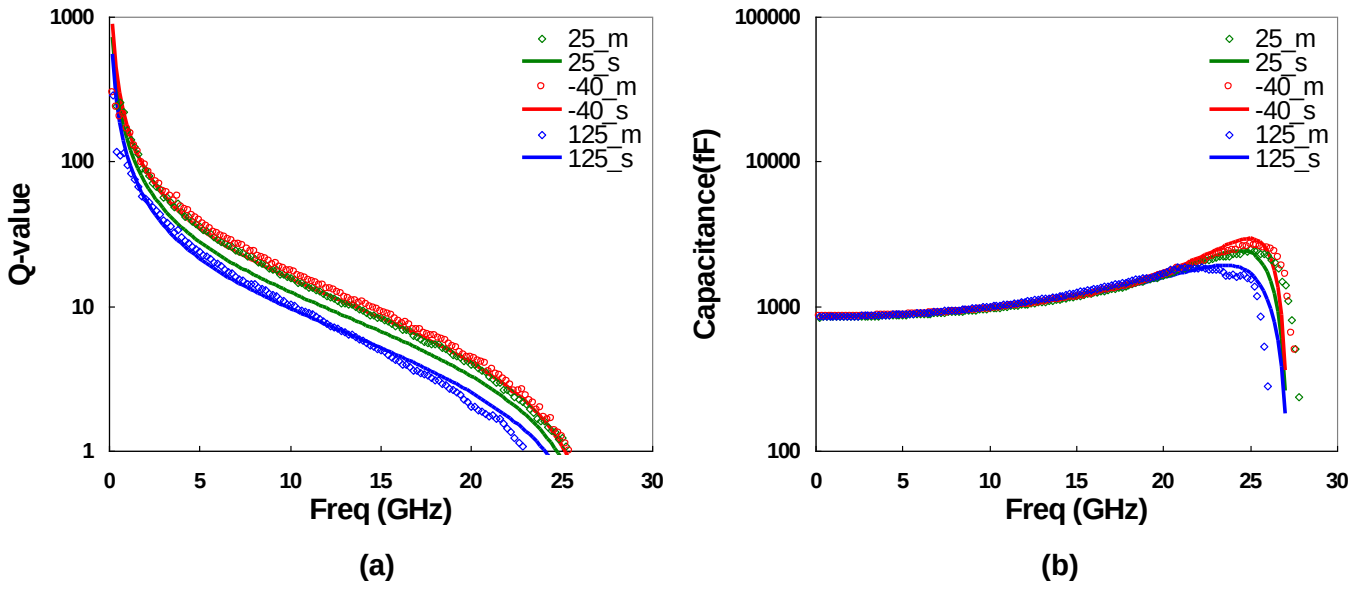

Fig. 12.15.6: Quality factor (a) and capacitance (b) versus frequency for the 2.0fF/μm^2 MIMCAP tester at 125℃, 25℃ and -40℃.

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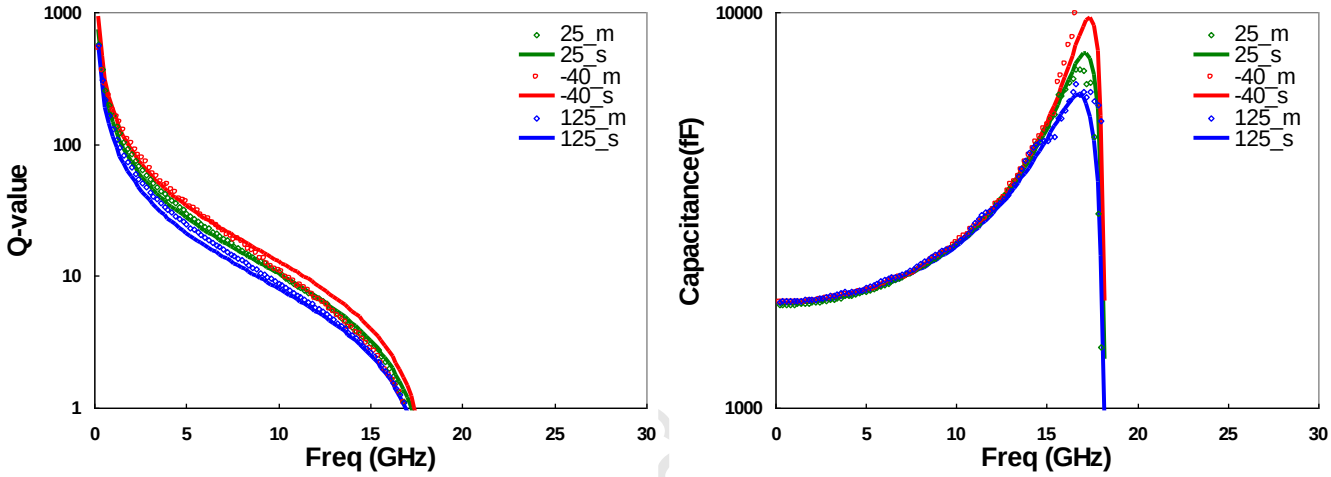

Fig. 12.15.7: Quality factor (a) and capacitance (b) versus frequency for the 2.0fF/μm² UDC MIMCAP tester at 125℃, 25℃ and -40℃.

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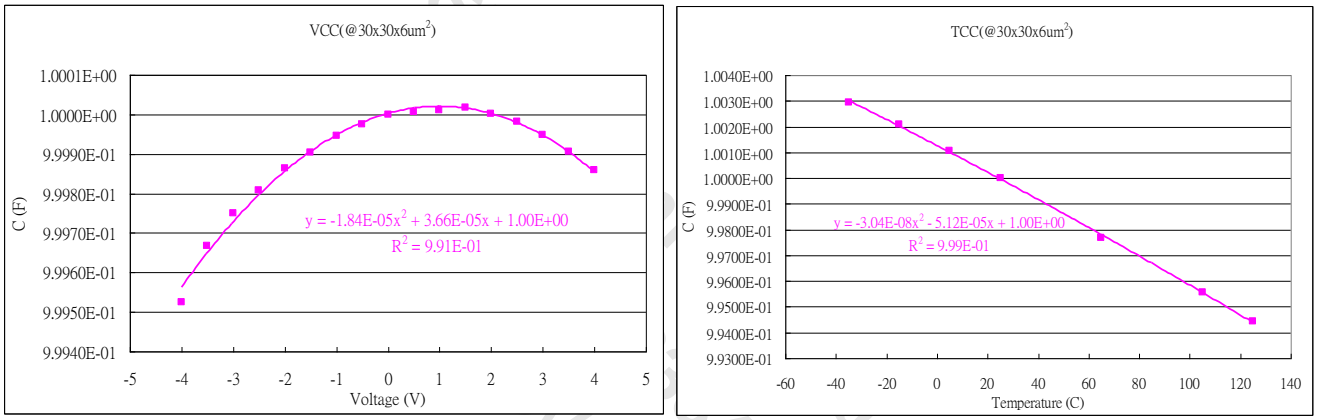
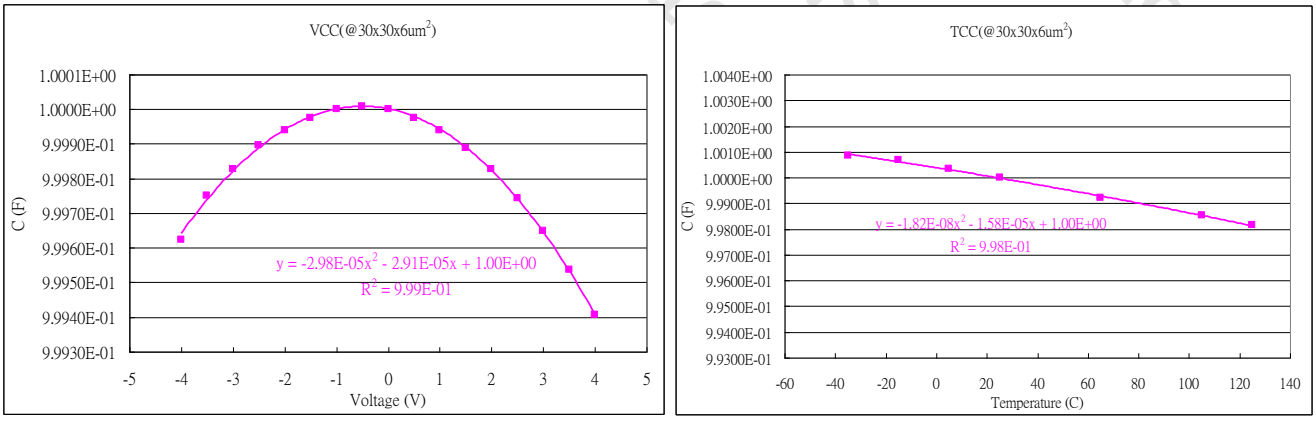
12.15.7 TCC and VCC

The sensitivity of the capacitances to the DC bias voltage (VCC) and temperature (TCC) variations are characterized using a MIMCAP tester with area of 30x30 μm^2. The data for the capacitance measured at 25 °C while stepping the DC bias voltage from –4V to 4V (in 0.5V steps, see Fig. 12.15.8 (a) and Fig. 12.15.9 (a)) can be fit to a quadratic function with voltage coefficients Vcc2 = -18.36 ppm/V^2 and Vcc1 = 36.6 ppm/V for 1.0fF/μm^2 MIMCAP, and Vcc2 = -29.658 ppm/V^2 and Vcc1 = -28.97 ppm/V for 2.0fF/μm^2 MIMCAP. Likewise, at zero bias voltage, and temperature varying from -40°C to 125°C, the temperature coefficients Tcc2 = -0.03 ppm/°C^2 and Tcc1 = -51.1 ppm/°C have been obtained for 1.0fF/μm^2 MIMCAP (see Fig. 12.15.8 (b)), and Tcc2 = -0.018 ppm/°C^2 and Tcc1 = -15.73 ppm/°C for 2.0fF/μm^2 MIMCAP (Fig. 12.15.9 (b)).



(a) **(b)**

Fig. 12.15.8: Curve-fitting capacitance data of 1.0fF/μm^2 MIMCAP to (a) DC bias voltage variations, (b) temperature variations



(a) **(b)**

Fig. 12.15.9: Curve-fitting capacitance data of 2.0fF/μm^2 MIMCAP to (a) DC bias voltage variations, (b) temperature variations.

Notes for Fig. 12.15.7 and 12.15.8:

1 Curve fitting of the measured C for VCC uses C(V)=Co[1+Vcc1(V)+Vcc2(V)2], where Co is capacitance at 0V bias.

2 Curve fitting of the measured C for TCC uses C(T)=C(Tnom)[1+Tcc1(T-Tnom)+Tcc2(T-Tnom)2], where Tnom is at 25℃ and C(Tnom) is capacitance at 25℃.

3 Measurements have been carried out using the HP 4284 LCR meter @100KHz.

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12.15.8 Mismatch Model

The model for this technology has added the capability for mismatch analysis of pairs of identical MIMCAPs in proximity. Random variations in the Gaussian distribution of the total capacitance are included in the model to account for the mismatch effects. Fig.12.15.10 shows the simulation results and the measured data in terms of the sigma of the percentage difference of the capacitances versus 1/(Area) $^{0.5}$.

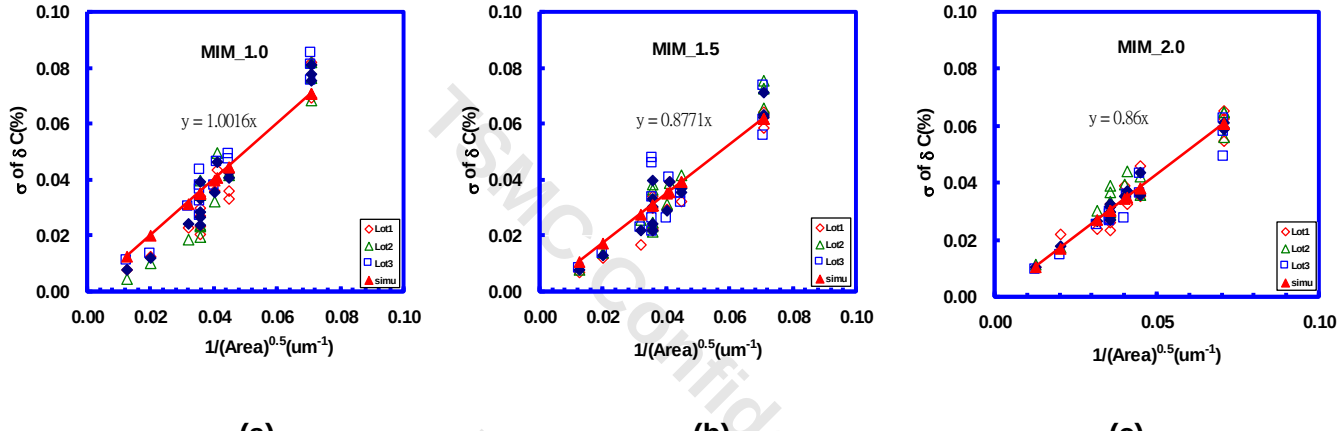

Fig. 12.15.10: Measurement and simulation results of 1000 Monte Carlo random tests of sigma 2*(C1-C2)/(C1+C2) for (a) 1.0fF/μm² , (b) 1.5fF/μm² MIMCAP, and (c) 2.0fF/μm² MIMCAP pair.

12.15.9 Statistical Model

In addition to the corner models described in Section 12.15.5, a statistical library like MC_MIM and MC_RFMIM are also available for Monte-Carlo simulation. The statistical model is derived from the corner cases based on the PCA (Principal Component Analysis) result. Fig. 12.15.11 shows results of the Monte-Carlo simulations with various corner cases.

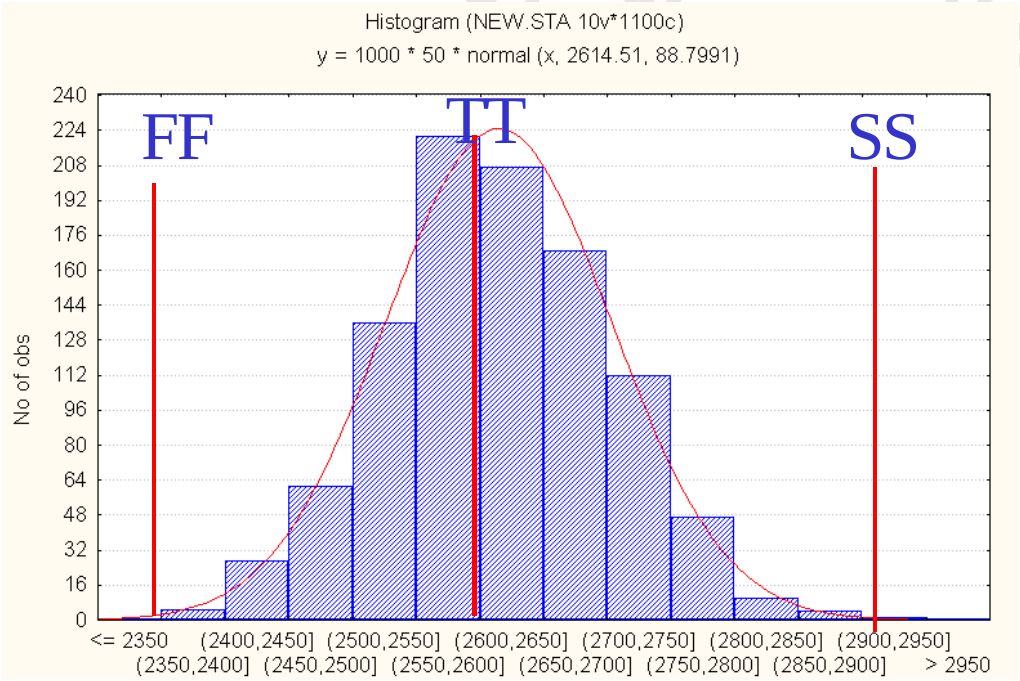

Fig. 12.15.11: The MC distribution of MIMCAP.

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12.16 MOM Capacitor Model

12.16.1 RF Model Usage Guide

The rotative metal capacitor (RTMOM) with poly shield is modeled for RF design based on the two-port S-parameter measurement and Y-parameter fitting. Top-level metal up to M7 is supported. The design parameters include the number of metal fingers in X and Y directions (NH and NV, see Fig. 12.16.1), the width and space of the metal fingers (W and S), and the start-metal and stop-metal layer (STM and SPM). STM is the lower level metal on which at least two more layers are stacked (i.e. SPM – STM ≥ 2). Even numbers in the range from 6 to 288 are allowed for NH and NV, and widths and spaces are between 0.1μm and 0.16μm. Model parameters are summarized in Table 12.16.1. Regrding the BB RTMOM model, designer can refer to DOC T-N65-CM-SP-002 for the mismatch and TCC&VCC characteristic of RTMOM.

Model Parameter	Range
Valid NV number	6 ~ 288 (even fingers)
Valid NH number	6 ~ 288 (even fingers)
Valid spacing	0.1μm ~ 0.16μm
Valid width	0.1μm ~ 0.16μm
Start metal layer (STM)	M1, M2, M3, M4, M5
Stop metal layer (SPM)	M3, M4, M5, M6, M7
Bus metal width	0.18um
Ftip	0.2um
TCC	-40℃ to 125℃
VCC	-5V to 5V

Table 12.16.1: Parameters and values for the RTMOM capacitor

EXAMPLE

To use an RF RTMOM with W=L=0.1μm, NH=NV=32 and start/stop metal=M1/M7:

```
X1_rf_rtmom a b p crtmom_rf nv=32 nh=32 w=0.1u s=0.1u stm=1 spm=7
```

12.16.2 RF Test Structure and Measurement Procedures

The structure of the RTMOM capacitor is illustrated in Fig. 12.16.1. The capacitor has two ports with a poly shield connected to the ground node. Width and space of metal fingers are same in both the X and Y directions, which along with NH and NV determine the area of the capacitor. Fingers for both electrodes in each metal layer are connected with L-shape strips. The strips in different layers are then shunted together with vias. Two-port S-parameters have been measured in a frequency range of 200 MHz to 30 GHz, with RF de-embedding using open and short test structures.

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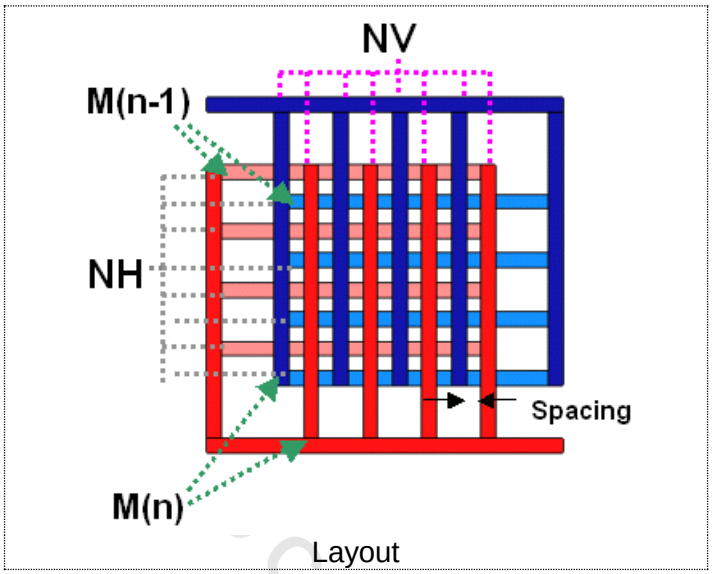

Fig. 12.16.1: The top layout view of structure of an RTMOM capacitor with NV x NH = 8 x 8, showing only the top two metal layers

12.16.3 RF Equivalent Circuit Model

The equivalent circuit model for the RF RTMOM capacitor with poly shield is shown in Fig. 12.16.2. The circuit elements are described below:

- **Cmom is the main capacitor element due to the inter-metal dielectric material**
- **Ra and La are the resistive and inductive parasitic at electrode 'a' (port 1)**
- **Rb and Lb are the resistive and inductive parasitic at electrode 'b' (port 2)**
- **Cpa and Cpb represent the capacitances between metal and poly shield.**

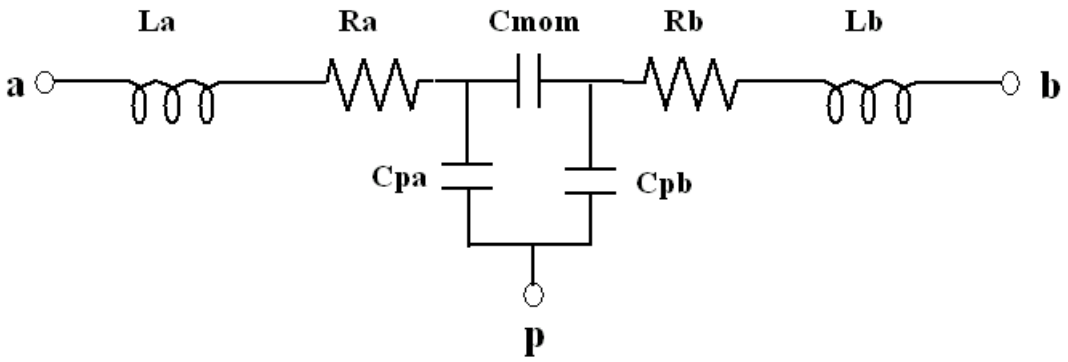

Fig. 12.16.2: Equivalent circuit of the RF RTMOM capacitor with poly shield.

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12.16.4 RF Model Details

12.16.4.1 Scaling Rule

The scaling equations for the various elements R, L and C are empirically determined and shown in Table 12.16.2.

Component	Equation
L_a (H)	total_l
R_a (Ω)	total_res·(0.0036·(temper-25)+1)
C_{ab} (F)	(1+factmis)·(Cc1·Edg+Cf·FRI1+Ca·AREA+Cc2·FRI2)·1e-9·(1+(temper-25)·tcc1+(temper-25) ·(temper-25)·tcc2)·(1+vcc1·v(a1,b1)+vcc2·v(a1,b1)·v(a1,b1))
C_{pa} (F)	(Ca_p·(Abm+Afm)+Cf_p·Pf+Cc_p·Pfb)·1e-9·(1+(temper-25)·tcc1+(temper-25)·(temper-25) ·tcc2)·(1+vcc1·v(a1,p)+vcc2·v(a1,p)·v(a1,p))
C_{pb} (F)	(Ca_p·(Abm+Afm)+Cf_p·Pf+Cc_p·Pfb)·1e-9·(1+(temper-25)·tcc1+(temper-25)·(temper-25) ·tcc2)·(1+vcc1·v(b1,p)+vcc2·v(b1,p)·v(b1,p))
R_b (Ω)	total_res·(0.0036·(temper-25)+1)
L_b (H)	total_l
where,	
layno	spm-stm+1
laym1	INT(layno/spm)
layodd	INT((layno+j1+j3+j5)/2)-laym1
layeven	INT((layno+j2+j4)/2)
r	0.92
dw	((0.228495016028492)·(w·scale·1e6)+(0.864862940554024)·(s·scale·1e6)+(-4.46733713068237)·(s·scale·1e6)·(w·scale·1e6)+(-6.35923905319406E-02))·(1e-6)
ww	w·scale +dw
ss	s·scale -dw
wb	0.18u+dw
sb	0.2u-dw
lnv	nh·(ww+ss)-ss
lnh	nv·(ww+ss)-ss
tcc1	-12.4·1e-6
tcc2	0.0133·1e-6
vcc1	-0.1·1e-6
vcc2	0.8·1e-6
j1	(stm-2)·(stm-3)·(stm-4)·(stm-5)/(1-2)/(1-3)/(1-4)/(1-5)
j2	(stm-1)·(stm-3)·(stm-4)·(stm-5)/(2-1)/(2-3)/(2-4)/(2-5)
j3	(stm-1)·(stm-2)·(stm-4)·(stm-5)/(3-1)/(3-2)/(3-4)/(3-5)
j4	(stm-1)·(stm-2)·(stm-3)·(stm-5)/(4-1)/(4-2)/(4-3)/(4-5)
j5	(stm-1)·(stm-2)·(stm-3)·(stm-4)/(5-1)/(5-2)/(5-3)/(5-4)
Edg	((layodd+r·laym1)·(nv-1)·lnv+layeven·(nh-1)·lnh)
AREA	nv·nh/2·ww·(layno-1)
FRI1	(2·nh·nv·ww)·(layno-1)
FRI2	(layodd+r·laym1)·lnv·2+layeven·(lnh+sb)·2+((layodd+r·laym1)·nv·ww+layeven·nh·ww) +layno·wb·2
Abm	((lnh+(wb+sb)·2)+(lnv+sb))·wb/ww·(1.7·j1+8·j2+8·(j3+j4+j5))
Afm	(j1+j3+j5)·(nv·(lnv+sb))/2+(j2+j4)·(nh·(lnh+sb))/2
Pf	(j1+j3+j5)·nv·(lnv+sb)+(j2+j4)·nh·(lnh+sb)+2·(lnv+lnh)+6·wb+6·sb
Pfb	j1·(lnv+2·wb+sb)·1
Cc1	((3.31778571428518E-03)/(w·scale·1e6)+(4.58367293233029E-03)/(s·scale·1e6) +(3.33151365255902E-05)/(s·scale·1e6)/(w·scale·1e6)+(3.18642857143291E-03))·1.0005

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Cc2	(0.0471)·1.49
Cf	((0.217378960485214)·(w·scale·1e6)+(0.152520469919126)·(s·scale·1e6)+(-0.787958348173258)·(s·scale·1e6) ·(w·scale·1e6)+(-1.11529681382862E-02))·0.7
Ca	(((-7.4178977970751E-03)·(w·scale·1e6)+(1.64193663145724E-02)·(s·scale·1e6)+(0.22479975089191)·(s·scale·1e6)·(w·scale·1e6)+(5.00430980214061E-03))·0.5)
ca_p_a	(j1·(0.228499695208201)·0.6308+j2·(9.21578947359392E-02)·0.4976+j3·(4.63684210684769E-02)·0.4055+j4·(2.64537201083299E-02)·0.4055+j5·(2.00000889208476E-02)·0.4055)
ca_p_b	(j1·(9.07506717796861E-02)·0.6308+j2·(5.95789473675215E-02)·0.4976+j3·(3.06315789633253E-02)·0.4055+j4·(2.07273050345198E-02)·0.4055+j5·(1.56699002205504E-02)·0.4055)
ca_p_c	(j1·(-0.377728701830403)·0.6308+j2·(-0.354986149577421)·0.4976+j3·(-0.176869806250642)·0.4055+j4·(-0.105731576687923)·0.4055+j5·(-7.99127797182435E-02)·0.4055)
ca_p_d	(j1·(-8.09567284527284E-03)·0.6308+j2·(-6.66999999988505E-03)·0.4976+j3·(-3.22000000149291E-03)·0.4055+j4·(-1.82074224563325E-03)·0.4055+j5·(-1.36635723238263E-03)·0.4055)
cf_p_a	(j1·(3.92322184993517E-03)·0.6308+j2·(9.73684223713357E-04)·0.4976+j3·(0.008631579009041)·0.4055+j4·(-1.35697747026833E-03)·0.4055+j5·(-1.38305409476152E-04)·0.4055)
cf_p_b	(j1·(5.26195109392581E-02)·0.6308+j2·(6.47368422147126E-03)·0.4976+j3·(8.02631583671123E-03)·0.4055+j4·(2.91660738192766E-03)·0.4055+j5·(3.3899964647692E-03)·0.4055)
cf_p_c	(j1·(0.095762967753077)·0.6308+j2·(0.121952908482245)·0.4976+j3·(4.46675895930827E-02)·0.4055+j4·(0.055633676966577)·0.4055+j5·(4.34229260807518E-02)·0.4055)
cf_p_d	(j1·(8.54632956062667E-03)·0.6308+j2·(5.82999999863725E-03)·0.4976+j3·(4.2199999931874E-03)·0.4055+j4·(5.05353060446388E-03)·0.4055+j5·(4.65741277617021E-03)·0.4055)
Ca_p	(ca_p_a·(w·scale·1e6)+ca_p_b·(s·scale·1e6)+ca_p_c·(s·scale·1e6)·(w·scale·1e6)+ca_p_d)·1
Cf_p	(cf_p_a·(w·scale·1e6)+cf_p_b·(s·scale·1e6)+cf_p_c·(s·scale·1e6)·(w·scale·1e6)+cf_p_d)·1
Cc_p	(0.017)·4
geo_fac	1/sqrt((Cc1·Edg·1e-9+Cf·1e-9·FRI1+Ca·1e-9·AREA+Cc2·1e-9·FRI2)·1e15)
mis	$0.32\cdot(((geo_fac-0.027)^2+0.000000000000000001)^{0.5}+geo_fac)+2.4\cdot(((geo_fac-0.027)^2+0.000000000000000001)^{0.5}-geo_fac)+0.084$
factmis	mis/1.414/100·mismatchflag
length_nv	nh·((w·scale)+(s·scale))-(s·scale)
res_nv	length_nv/(w·scale)·0.14+0.2·1e-6/(w·scale)·0.14
latres_nv	((w·scale)+2·(s·scale))/(0.18·1e-6)·0.14
fin_nv	nv/2
totres_nv	(latres_nv/2+(fin_nv/2-1)·(fin_nv-1)/(6·fin_nv/2)·latres_nv+res_nv/(fin_nv/2))/2
allres_nv	totres_nv/(layodd+laym1)
length_nh	nv·((w·scale)+(s·scale))-(s·scale)
res_nh	length_nh/(w·scale)·0.14+0.2·1e-6/(w·scale)·0.14
latres_nh	((w·scale)+2·(s·scale))/(0.18·1e-6)·0.14
fin_nh	nh/2
rend_nh	(0.2·1e-6+(w·scale)+(s·scale)+length_nh/2+0.2·1e-6)/(0.18·1e-6)·0.14
totres_nh	rend_nh+(fin_nh-1)·(2·fin_nh-1)/(6·fin_nh)·latres_nh+res_nh/fin_nh
allres_nh	totres_nh/layeven
total_res	1/(1/allres_nv+1/allres_nh)·(((-0.00712873084974587·nh/nv+3.35551710606971/nh)+(-0.0089591025471292 6·nv/nh+2.01477796505834/nv)+6.5884069072713E-07·nv·nh)·(-35.140406193376·((w·scale)·1e6)-68.3803850278667·((s·scale)·1e6)+0.108753331486981/((w·scale)·1e6)/((s·scale)·1e6)+1023.2423085004
l_nvnh	((0.2·(length_nv·1e6)·(log((length_nv·1e6)/(length_nh·1e6+0.22))+1.19+0.022·(length_nh·1e6+0.22)/(length_nv·1e6))+1.5))
total_nvnh	(0.1+(layno-1)·(2·layno-1)/(6·layno)·0.1+l_nvnh/layno)
total_l	((0.229289757299351·total_nvnh2+0.365863332205633·total_nvnh-0.242677462368036)·(0.205246455834331·(((w·scale)·1e6)+((s·scale)·1e6))(-0.30997693758166))·((0.139488733019201·nv·nh+0.268982725644102·nv/nh-4.97906032421557·nh/nv)(0.0850436841380641))·(0.138127474751232·(lay

Table 12.16.2: Subcircuit elements for a RTMOM.

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12.16.4.2 Model Parameter

Values for the equivalent circuit elements are shown in Table 12.16.3. The testers have metal finger widths and spaces of (0.1μm, 0.1μm) and (0.16μm, 0.1μm) start metal layers (stm) from M1 to M5 and stop metal layer (spm) from M3 to M7, with NV values ranging from 6 to 288 and NH values from 6 to 288.

nv	6	6	48	48	6	48	72	288	6	48	48	288	6	48	288
nh	48	288	48	288	288	48	72	6	288	48	48	6	288	48	6
w (μm)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.16	0.16	0.16
s (μm)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
stm	1	1	1	1	1	1	1	1	1	1	2	2	1	1	1
spm	5	5	5	5	7	7	7	7	3	3	4	4	5	5	5
L_a, L_b(pH)	4.82	26.63	4.56	20.39	24.89	4.59	4.83	4.20	30.55	4.56	4.56	4.26	37.89	4.64	4.22
R_a, R_b(Ω)	3.14	2.06	0.58	0.85	1.47	0.46	0.43	1.42	3.56	0.83	1.30	5.04	2.08	0.58	2.20

Table 12.16.3: Equivalent circuit parameters for RF RTMOM.

12.16.4.3 Model Error Table

Fitting errors are summarized in Table 12.16.4; the root mean square of capacitance fitting error C_{RMS} is calculated from 1GHz to 20GHz according to the equation given in Chapter 13. The Q fitting is higher priority fitting in the range of 2GHz~15GHz to get trade-off best fitting accuracy for each size. Due to the RF measurement limitation, the parasitic elements of RTMOM with small dimension are evaluated by physical extrapolation based on larger devices.

nv	6	6	48	48	6	48	72	288	6	48	48	288	6	48	288
nh	48	288	48	288	288	48	72	6	288	48	48	6	288	48	6
w (um)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.16	0.16	0.16
w (um)	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1	0.1
stm	1	1	1	1	1	1	1	1	1	1	2	2	1	1	1
spm	5	5	5	5	7	7	7	7	3	3	4	4	5	5	5
C_{RMS}(%) *	0.7	1.8	1.1	3.8	8.2	5.5	5.4	2.6	3.2	4.7	2.6	2.9	2.3	0.3	1.2
$C_{f=10GHz}$ (%)	-0.6	-1.5	-0.8	-4.7	4.6	5.4	5.3	2.5	-3.1	-4.7	2.6	2.9	2.3	-0.1	-1.0
$Q_{f=10GHz}$ (%)	-3.4	-4.8	16.9	-1.1	-9.3	-13.1	-12.6	2.7	-13.7	-3.8	-12.6	-6.4	-7.9	0.6	-5.9

Table 12.16.4: Capacitance and Q value fitting errors for RF RTMOM.

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12.16.5 RF Corner Model Table

Table 12.16.5 lists the skew parameters for the slow-corner (SS), typical (TT) and fast-corner (FF) cases, which correspond to libraries SS_RFRTMOM, TT_RFRTMOM and FF_RFRTMOM. There is also a statistical model library, MC_RFRTMOM, for Monte Carlo simulation

Skew Parameter	SS	TT	FF
RTMOM_momfac1	1.15	1	0.85
RTMOM_momfac2	1.4	1	0.6
l_momfac	1.0235	1	0.9762
r_momfac	1.3	1	0.7

Table 12.16.5: Skew parameters for RF RTMOM.

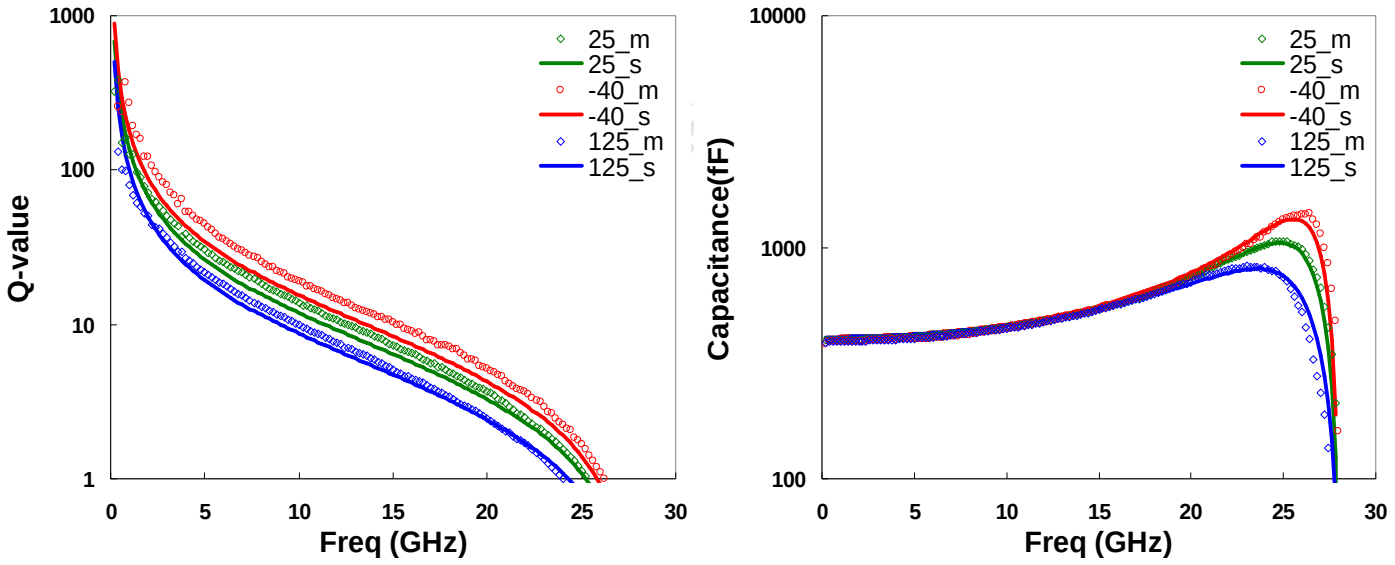
12.16.6 RF Temperature Effect Model

A capacitor tester with W/S=0.16μm /0.16μm, NV/NH=8/288 and metal stack M1 to M7 is used to study the temperature characteristics. The parasitic resistance elements, Ra and Rb, show linear dependences on temperature as modeled by the following functions,

Ra(T)=Ra*(0.0036*(temper-25)+1)

Rb(T)=Rb*(0.0036*(temper-25)+1)

Values of the quality factor (Q) as function of frequency at temperatures -40℃, 25℃, 125℃ are shown in Fig. 12.16.3 (a); variations of Q with temperature in the whole frequency range (~DC to 30 GHz) are evident. Note that lower Q at higher temperature is most likely due to the larger parasitic resistances. On the other hand, the capacitance, as plotted in Fig. 12.16.3 (b), changes little with temperature up to about 22 GHz.



(a) (b)

Fig. 12.16.3: Quality factor (a) and capacitance (b) versus frequency for the RF RTMOM tester at 125℃, 25℃ and -40℃.

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12.17 Inductor Model

12.17.1 Model Usage Guide

Testers for the standard and symmetric octagonal spiral inductors using thick Cu metal (physical thickness: 3.4 mm) on P-substrate have been fabricated and modeled based on two-port Y-parameter fitting. The symmetric inductors can be used in both single-ended and differential mode operations, with the latter having an extra node ("tap") as the center tap. Two metallization technologies for fabricating the core inductor are supported: One uses UTM in processes 1P5M to 1P9M (i.e., *mu_z*), and the other uses Mz+AL_RDL and Mu+AL_RDL in processes 1P5M to 1P8M (i.e., *mza_a, mu_a, respectively*). Scalable models for the three types of inductors, the standard (*spiral_std_mu_z*; *spiral_std_mza_a; spiral_std_mu_a*), symmetric (*spiral_sym_mu_z; spiral_sym_mza_a; spiral_sym_mu_a*) and symmetric with center tap *(spiral_sym_ct_mu_z; spiral_sym_ct_mza_a; spiral_sym_ct_mu_a*), are included in this release. The guard-ring effect is included in these models. The valid parameter values are listed in Table 12.17.1.

Table 12.17.1: Parameters and valid values of the inductor models

Type	Mz+Mu inductor			Mz+ALRDL inductor			Mu+ALRDL inductor		
Specification	STD	SYM	CT	STD	SYM	CT	STD	SYM	CT
Inductance(nH)	0.06~12.17	0.086~15.26	0.086~15.26	0.06~12.38	0.086~15.26	0.086~15.26	0.06~12.17	0.086~15.26	0.086~15.26
Valid width(um)	3~30	3~30	3~30	7.5~30	7.5~30	7.5~30	6.2~30	6.2~30	6.2~30
Valid Turns(N)	0.5 ~ 5.5 (1/4 per step)	1 ~ 6 (1 per step)	1 ~ 6 (1 per step)	0.5 ~ 5.5 (1/4 per step)	1 ~ 6 (1 per step)	1 ~ 6 (1 per step)	0.5 ~ 5.5 (1/4 per step)	1 ~ 6 (1 per step)	1 ~ 6 (1 per step)
Valid Radius(R:um)	15 ~ 90(when width <20), 20 ~ 90(when width >=20)								
Spacing(um)	2 ~ 4								
Guard-ring distance	10 ~ 50 um								
Variable Metal Layer	1P5M ~ 1P9M			1P5M ~ 1P8M			1P5M ~ 1P8M		
Valid Temperature	- 40 ~ 125 (degree)								
Valid Frequency	min(30GHz, Fsr)								

No devices should be placed under the inductor, as the performance will be affected by the magnetic field penetrating into the silicon substrate. Designers can change the number of turns (NR), the spacing (SPACING), the inner radius (RAD) and track width (W) to adjust the inductance (L) value. Parameter *gdis* (10μm to 50μm) sets the distance between core inductor and the guard-ring. Minimum value of *gdis* should be avoided because couplings with other devices are not included in the models. For more information regarding the inductor design, please refer to the thick metal rule, T-N65-CM-DR-001, at the TSMC website.

EXAMPLE

To use standard inductor processed with UTM metal (i.e., *mu_z*; maximum *lay* = 9):

```
Xl_spiral_1 top bottom gnode spiral_std_mu_z nr=3.5 rad=60u spacing=3u w=15u lay=9 gdis=50u
```

To use symmetric inductor with center tap processed with AL_RDL metal (i.e., *mza_a*; maximum *lay* = 8):

```
Xl_spiral_2 top bottom gnode tap spiral_sym_ct_mza_a nr=3 rad=60u spacing=3u w=15u lay=8 gdis=50u
```

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12.17.2 Test Structure and Measurement Procedures

Top layout views of the three types of inductors are shown in Fig. 12.17.1 with the key design parameters:

- N: number of turns
- W: inductor track width
- S: spacing between tracks
- R: inner radius of inductor
- **Gdis: guard-ring distance**

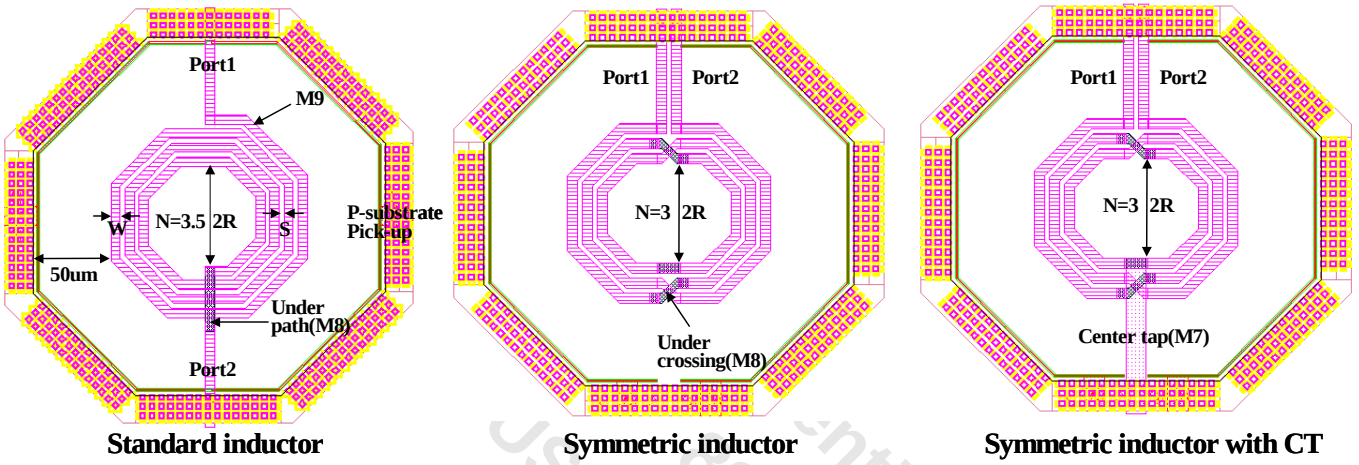

Fig. 12.17.1: Top views of inductor layouts.

12.17.3 Equivalent Circuit Model

Lumped RLC equivalent 2-π circuit representation of the standard, symmetric and π circuit for center-tapped inductor is shown in Fig. 12.17.2. These models are fitted with empirical equations. The component values are extracted by fitting the two-port Y-parameters, simulated from calibrated EM tools. The calibrated EM tools have good agreements with measurement data, which are de-embedded with equivalent open and thru.

The equivalent circuit are as follows, where K is the mutual inductance:

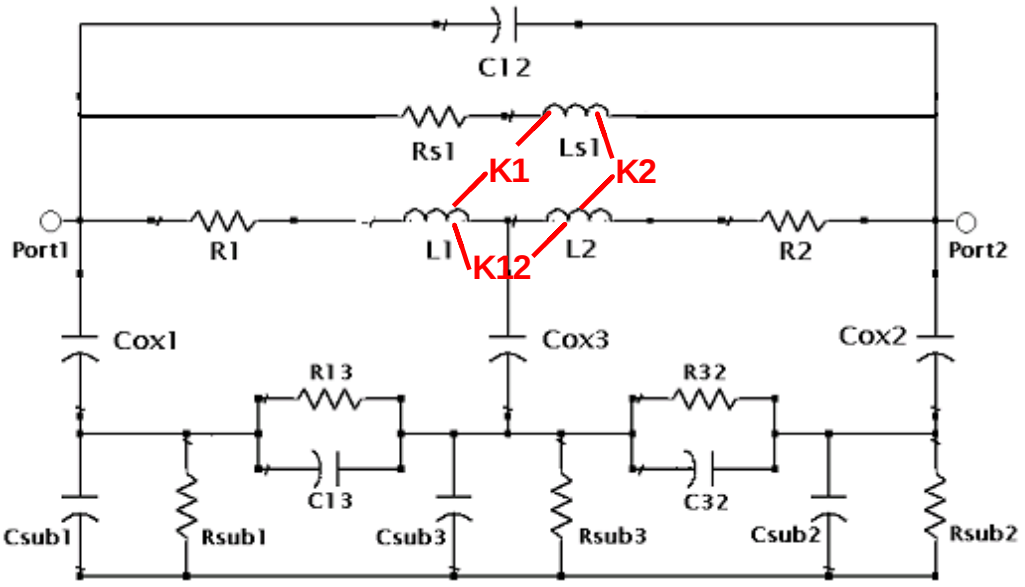

Fig. 12.17.2: Equivalent circuit of a standard inductor.

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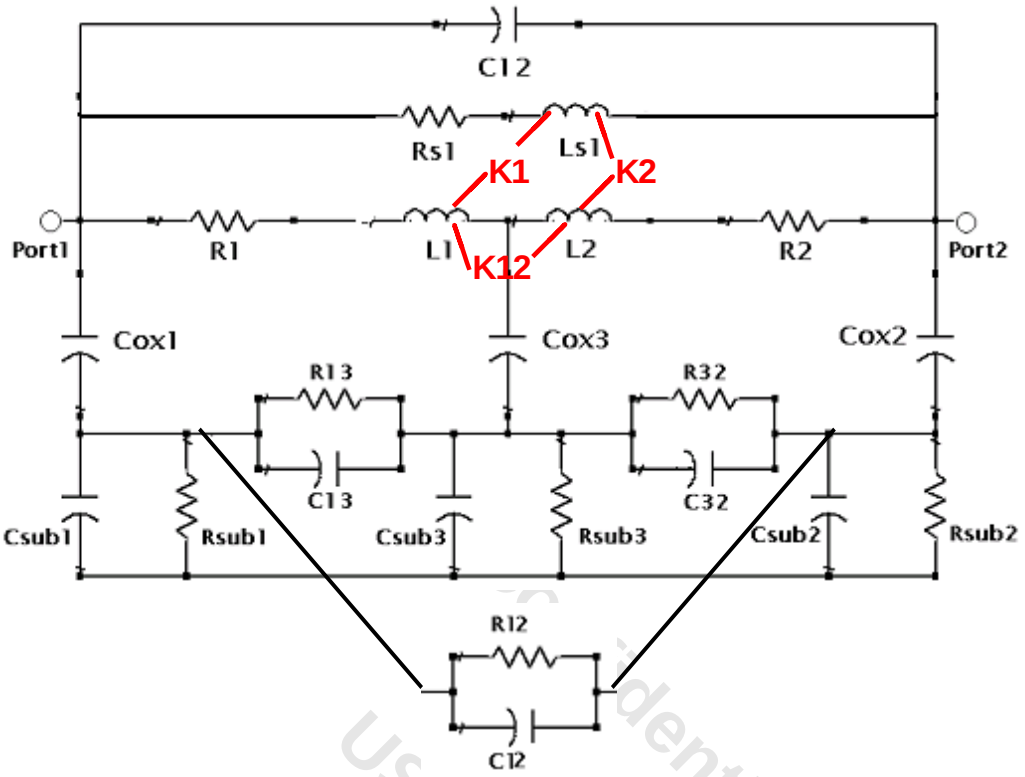

Fig. 12.17.3: Equivalent circuit of a symmetric inductor.

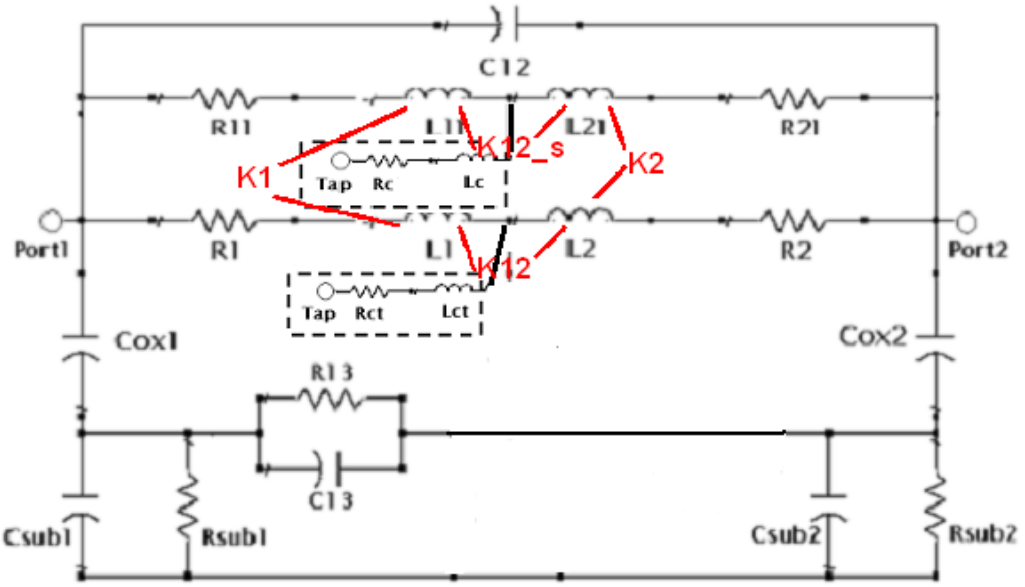

Fig. 12.17.4: Equivalent circuit of a symmetric center-tapped inductor.

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12.17.4 Model Details

12.17.4.1 Standard Inductor Model Error Table

Modeling errors are obtained by fitting the real and imaginary parts of the four Y-parameters according to the equations given in Chapter 13 of T-N65-CM-SP-007. Fitting errors for the mu_z (mza_a) [mu_a] standard inductors with track widths of 3μm, 6μm, 9μm, 15μm and 30μm (7.5μm, 15μm and 30μm) [6.2μm, 9μm, 15μm and 30μm] and different guard-ring distance are summarized in Tables 12.17.2 to 12.17.12.

N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	15	15	30	30	60	60	60	90	90	90
Real(Y11)(%)	14.82	6.22	7.20	3.43	14.13	2.86	0.31	10.03	0.59	0.32
Real(Y21)(%)	14.84	6.25	7.21	3.43	14.13	2.87	0.26	10.04	0.59	0.31
Real(Y12)(%)	14.84	6.25	7.21	3.43	14.13	2.87	0.26	10.04	0.59	0.31
Real(Y22)(%)	14.83	6.22	7.20	3.40	14.13	2.86	0.26	10.04	0.58	0.28
Imag(Y11)(%)	0.33	0.89	0.36	0.11	2.61	0.25	0.42	0.61	0.21	0.24
Imag(Y21)(%)	0.34	0.89	0.36	0.08	2.60	0.27	0.41	0.62	0.21	0.24
Imag(Y12)(%)	0.34	0.89	0.36	0.08	2.60	0.27	0.41	0.62	0.21	0.24
Imag(Y22)(%)	0.34	0.90	0.35	0.08	2.61	0.24	0.41	0.62	0.21	0.23

Table 12.17.2: Fitting errors (Real and Imaginary) for a mu_z standard inductor with W=15μm , gdis=50μm, spacing=3μm

N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	15	15	30	30	60	60	60	90	90	90
Real(Y11)(%)	1.92	1.37	4.93	1.15	7.22	1.01	1.92	4.60	0.42	1.00
Real(Y21)(%)	1.92	1.37	4.93	1.15	7.22	1.01	1.92	4.60	0.41	0.99
Real(Y12)(%)	1.92	1.37	4.93	1.15	7.22	1.01	1.92	4.60	0.41	0.99
Real(Y22)(%)	1.92	1.36	4.92	1.15	7.22	1.02	1.55	4.60	0.42	1.00
Imag(Y11)(%)	4.17	5.33	14.64	8.56	12.52	8.37	6.18	8.30	6.79	4.55
Imag(Y21)(%)	4.15	5.30	14.56	8.51	12.46	8.32	6.13	8.25	6.74	4.51
Imag(Y12)(%)	4.15	5.30	14.56	8.51	12.46	8.32	6.13	8.25	6.74	4.51
Imag(Y22)(%)	4.16	5.32	14.62	8.55	12.52	8.36	6.18	8.30	6.79	4.55

Table 12.17.3: Fitting errors (Real and Imaginary) for a mu_z standard inductor with W=3μm , gdis=50μm, spacing=3μm.

N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	15	15	30	30	60	60	60	90	90	90
Real(Y11)(%)	2.44	1.65	2.51	0.96	1.10	0.85	1.63	0.23	1.69	2.55
Real(Y21)(%)	2.44	1.65	2.51	0.97	1.11	0.85	1.63	0.22	1.69	2.57
Real(Y12)(%)	2.44	1.65	2.51	0.97	1.11	0.85	1.63	0.22	1.69	2.57
Real(Y22)(%)	2.44	1.65	2.51	0.97	1.10	0.85	1.62	0.22	1.68	2.55
Imag(Y11)(%)	5.32	1.40	0.48	0.24	1.04	0.56	0.29	1.22	0.29	0.58
Imag(Y21)(%)	5.30	1.38	0.49	0.24	1.04	0.55	0.24	1.22	0.22	0.52
Imag(Y12)(%)	5.30	1.38	0.49	0.24	1.04	0.55	0.24	1.22	0.22	0.52
Imag(Y22)(%)	5.31	1.39	0.49	0.23	1.04	0.55	0.25	1.22	0.22	0.51

Table 12.17.4: Fitting errors (Real and Imaginary) for a mu_z standard inductor with W=6μm , gdis=50μm, spacing=3μm.

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N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	15	15	30	30	60	60	60	90	90	90
Real(Y11)(%)	7.75	0.69	8.16	3.79	3.69	5.87	1.95	1.75	2.32	0.34
Real(Y21)(%)	7.75	0.63	8.16	3.80	3.69	5.88	1.97	1.75	2.32	0.34
Real(Y12)(%)	7.75	0.63	8.16	3.80	3.69	5.88	1.97	1.75	2.32	0.34
Real(Y22)(%)	7.75	0.68	8.16	3.80	3.69	5.87	1.97	1.75	2.08	0.34
Imag(Y11)(%)	2.63	1.10	3.00	1.45	2.88	1.81	1.27	0.86	1.29	1.41
Imag(Y21)(%)	2.62	1.11	2.99	1.43	2.88	1.81	1.26	0.86	1.28	1.41
Imag(Y12)(%)	2.62	1.11	2.99	1.43	2.88	1.81	1.26	0.86	1.28	1.41
Imag(Y22)(%)	2.63	1.11	2.99	1.43	2.88	1.81	1.25	0.85	1.28	1.38

Table 12.17.5: Fitting errors (Real and Imaginary) for a mu_z standard inductor with W=9μm , gdis=50μm, spacing=3μm.

N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	20	20	55	55	90	90	90
Real(Y11)(%)	12.63	0.36	1.72	0.02	23.85	1.01	0.42
Real(Y21)(%)	12.70	0.31	1.75	0.12	23.89	1.04	0.55
Real(Y12)(%)	12.70	0.31	1.75	0.12	23.89	1.04	0.55
Real(Y22)(%)	12.64	0.34	1.74	0.17	23.86	1.05	0.49
Imag(Y11)(%)	3.54	1.07	1.31	0.29	1.47	0.46	0.08
Imag(Y21)(%)	3.52	1.05	1.30	0.29	1.47	0.45	0.13
Imag(Y12)(%)	3.52	1.05	1.30	0.29	1.47	0.45	0.13
Imag(Y22)(%)	3.54	1.08	1.31	0.30	1.47	0.46	0.03

Table 12.17.6: Fitting errors (Real and Imaginary) for a mu_z standard inductor with W=30μm , gdis=50μm, spacing=3μm.

N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	15	15	30	30	60	60	60	90	90	90
Real(Y11)(%)	2.28	1.08	2.21	1.11	3.40	0.46	1.39	1.55	0.75	0.91
Real(Y21)(%)	2.28	1.03	2.20	1.01	3.40	0.15	1.30	1.55	0.49	0.53
Real(Y12)(%)	2.28	1.03	2.20	1.01	3.40	0.15	1.30	1.55	0.49	0.53
Real(Y22)(%)	2.28	1.04	2.21	1.07	3.40	0.36	1.40	1.55	0.69	1.05
Imag(Y11)(%)	0.57	0.62	1.04	0.28	4.09	0.51	0.40	0.34	0.35	0.35
Imag(Y21)(%)	0.54	0.57	1.04	0.29	4.08	0.52	0.36	0.34	0.35	0.28
Imag(Y12)(%)	0.54	0.57	1.04	0.29	4.08	0.52	0.36	0.34	0.35	0.28
Imag(Y22)(%)	0.54	0.59	1.04	0.28	4.09	0.50	0.33	0.34	0.33	0.25

Table 12.17.7: Fitting errors (Real and Imaginary) for a mza_a standard inductor with W=15μm , gdis=50μm, spacing=3μm.

N (turns)	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	20	20	55	55	55	90	90	90
Real(Y11)(%)	3.83	1.83	8.47	2.98	1.44	14.02	1.85	2.82
Real(Y21)(%)	3.83	1.69	8.48	2.94	0.94	14.04	1.54	1.45
Real(Y12)(%)	3.83	1.69	8.48	2.94	0.94	14.04	1.54	1.45
Real(Y22)(%)	3.84	1.86	8.47	2.94	1.44	14.02	1.67	2.42
Imag(Y11)(%)	1.97	0.67	0.39	0.63	0.38	1.03	0.25	0.62
Imag(Y21)(%)	1.94	0.57	0.38	0.55	0.11	1.01	0.13	0.26
Imag(Y12)(%)	1.94	0.57	0.38	0.55	0.11	1.01	0.13	0.26
Imag(Y22)(%)	1.97	0.66	0.39	0.57	0.23	1.03	0.11	0.29

Table 12.17.8: Fitting errors (Real and Imaginary) for a mza_a standard inductor with W=30μm , gdis=50μm, spacing=3μm.

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N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	15	15	30	30	60	60	60	90	90	90
Real(Y11)(%)	0.42	0.25	1.07	0.26	1.91	0.21	0.37	1.60	0.43	0.58
Real(Y21)(%)	0.41	0.12	1.07	0.18	1.91	0.13	0.24	1.60	0.32	0.48
Real(Y12)(%)	0.41	0.12	1.07	0.18	1.91	0.13	0.24	1.60	0.32	0.48
Real(Y22)(%)	0.42	0.19	1.07	0.26	1.91	0.21	0.41	1.60	0.41	0.62
Imag(Y11)(%)	2.81	0.42	2.97	1.94	2.43	2.34	1.16	3.12	1.61	1.02
Imag(Y21)(%)	2.79	0.37	2.93	1.89	2.40	2.30	1.07	3.08	1.56	0.89
Imag(Y12)(%)	2.79	0.37	2.93	1.89	2.40	2.30	1.07	3.08	1.56	0.89
Imag(Y22)(%)	2.80	0.39	2.97	1.93	2.43	2.33	1.14	3.12	1.61	1.01

Table 12.17.9: Fitting errors (Real and Imaginary) for a mza_a standard inductor with W=7.5μm , gdis=50μm, spacing=3μm.

N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	15	15	30	30	60	60	60	90	90	90
Real(Y11)(%)	16.62	6.09	6.60	4.95	17.47	3.38	7.23	8.84	6.43	11.10
Real(Y21)(%)	16.65	5.52	6.53	2.60	17.48	1.42	2.89	8.83	4.88	5.57
Real(Y12)(%)	16.65	5.52	6.53	2.60	17.48	1.42	2.89	8.83	4.88	5.57
Real(Y22)(%)	16.63	5.76	6.56	4.03	17.48	2.66	6.23	8.84	6.04	10.35
Imag(Y11)(%)	1.87	0.42	0.43	0.58	5.73	0.41	0.89	0.48	0.50	1.25
Imag(Y21)(%)	1.88	0.38	0.38	0.43	5.72	0.31	0.50	0.40	0.51	0.75
Imag(Y12)(%)	1.88	0.38	0.38	0.43	5.72	0.31	0.50	0.40	0.51	0.75
Imag(Y22)(%)	1.88	0.28	0.41	0.27	5.73	0.24	0.43	0.47	0.25	0.68

Table 12.17.10: Fitting errors (Real and Imaginary) for a mu_a standard inductor with W=15μm , gdis=50μm, spacing=3μm.

N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	15	15	30	30	60	60	60	90	90	90
Real(Y11)(%)	2.99	2.96	2.30	1.66	2.69	1.63	2.96	1.26	1.92	4.46
Real(Y21)(%)	2.98	2.86	2.26	0.85	2.69	1.28	1.30	1.23	1.06	3.18
Real(Y12)(%)	2.98	2.86	2.26	0.85	2.69	1.28	1.30	1.23	1.06	3.18
Real(Y22)(%)	2.99	2.94	2.30	1.43	2.69	1.54	2.70	1.26	1.80	4.45
Imag(Y11)(%)	5.74	1.97	2.03	2.25	1.03	2.72	1.52	1.81	1.74	1.88
Imag(Y21)(%)	5.73	1.97	1.96	2.10	0.95	2.59	1.12	1.75	1.50	1.19
Imag(Y12)(%)	5.73	1.97	1.96	2.10	0.95	2.59	1.12	1.75	1.50	1.19
Imag(Y22)(%)	5.74	1.95	2.01	2.19	1.03	2.69	1.38	1.81	1.71	1.75

Table 12.17.11: Fitting errors (Real and Imaginary) for a mu_a standard inductor with W=6.2μm , gdis=50μm, spacing=3μm.

N (turns)	3.5	5.5	3.5	5.5	1.5	3.5	5.5	1.5	3.5	5.5
R(radius in μm)	15	15	30	30	60	60	60	90	90	90
Real(Y11)(%)	5.15	2.59	3.81	1.17	4.51	1.97	4.80	2.98	2.99	6.75
Real(Y21)(%)	5.15	2.23	3.75	1.17	4.50	1.00	2.50	2.95	1.32	3.55
Real(Y12)(%)	5.15	2.23	3.75	1.17	4.50	1.00	2.50	2.95	1.32	3.55
Real(Y22)(%)	5.15	2.45	3.80	1.93	4.51	1.66	4.38	2.98	2.69	6.51
Imag(Y11)(%)	2.68	0.34	0.93	0.47	5.38	0.44	0.82	1.76	0.59	1.16
Imag(Y21)(%)	2.68	0.20	0.92	0.30	5.37	0.24	0.66	1.77	0.50	0.64
Imag(Y12)(%)	2.68	0.20	0.92	0.30	5.37	0.24	0.66	1.77	0.50	0.64
Imag(Y22)(%)	2.68	0.18	0.92	0.20	5.38	0.32	0.56	1.76	0.49	0.79

Table 12.17.12: Fitting errors (Real and Imaginary) for a mu_a standard inductor with W=9μm , gdis=50μm, spacing=3μm.

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12.17.4.2Symmetric Inductor Model Error Table

Modeling errors for the mu_z (mza_a) [mu_a] symmetric inductor are obtained as outlined in this section, and summarized in Tables 12.17.13 to 12.17.24 for track widths of 3μm, 6μm, 9μm, 15μm and 30μm (7.5μm, 15μm and 30μm) [6.2μm, 9μm, 15μm and 30μm].

N (turns)	3	5	3	5	3	5	3	5
R(radius in μm)	15	15	30	30	60	60	90	90
Real(Y11)(%)	21.95	6.08	10.81	0.48	2.16	1.88	8.84	0.79
Real(Y21)(%)	21.96	6.09	10.82	0.48	2.17	1.89	8.87	0.79
Real(Y12)(%)	21.96	6.09	10.82	0.48	2.17	1.89	8.87	0.79
Real(Y22)(%)	21.95	6.08	10.82	0.48	2.17	1.88	8.84	0.78
Imag(Y11)(%)	3.91	1.30	0.31	0.74	0.36	0.34	0.23	0.28
Imag(Y21)(%)	3.90	1.30	0.31	0.74	0.38	0.35	0.24	0.25
Imag(Y12)(%)	3.90	1.30	0.31	0.74	0.38	0.35	0.24	0.25
Imag(Y22)(%)	3.91	1.30	0.31	0.74	0.36	0.34	0.22	0.26

Table 12.17.13: Fitting errors (Real and Imaginary) for mu_z symmetric inductor with W=15μm , gdis=50μm, spacing=3μm.

N (turns)	3	5	3	5	3	5
R(radius in μm)	20	20	55	55	90	90
Real(Y11)(%)	16.38	2.25	21.06	0.63	1.93	0.66
Real(Y21)(%)	16.43	2.32	21.22	0.70	1.89	0.21
Real(Y12)(%)	16.43	2.32	21.22	0.70	1.89	0.21
Real(Y22)(%)	16.38	2.26	21.10	0.61	1.91	0.71
Imag(Y11)(%)	3.66	2.36	2.46	1.29	1.42	0.68
Imag(Y21)(%)	3.64	2.33	2.45	1.26	1.40	0.68
Imag(Y12)(%)	3.64	2.33	2.45	1.26	1.40	0.68
Imag(Y22)(%)	3.66	2.36	2.46	1.29	1.42	0.68

Table 12.17.14: Fitting errors (Real and Imaginary) for mu_z symmetric inductor with W=30μm , gdis=50μm, spacing=3μm.

N (turns)	3	5	3	5	3	5	1	3	5
R(radius in μm)	15	15	30	30	60	60	90	90	90
Real(Y11)(%)	4.68	0.42	5.99	1.99	3.31	2.18	6.26	0.85	1.08
Real(Y21)(%)	4.68	0.42	6.00	2.00	3.31	2.18	6.26	0.85	1.08
Real(Y12)(%)	4.68	0.42	6.00	2.00	3.31	2.18	6.26	0.85	1.08
Real(Y22)(%)	4.68	0.42	5.99	1.99	3.29	2.18	6.26	0.85	1.08
Imag(Y11)(%)	7.09	0.94	15.70	10.08	7.33	5.69	9.32	6.32	5.47
Imag(Y21)(%)	7.07	0.95	15.64	10.03	7.28	5.66	9.26	6.28	5.42
Imag(Y12)(%)	7.07	0.95	15.64	10.03	7.28	5.66	9.26	6.28	5.42
Imag(Y22)(%)	7.09	0.94	15.70	10.08	7.33	5.69	9.32	6.32	5.47

Table 12.17.15: Fitting errors (Real and Imaginary) for mu_z symmetric inductor with W=3μm , gdis=50μm,spacing=3μm.

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N (turns)	3	5	3	5	3	5	1	3	5
R(radius in μm)	15	15	30	30	60	60	90	90	90
Real(Y11)(%)	1.44	1.92	0.95	1.30	0.12	1.90	0.12	1.35	3.14
Real(Y21)(%)	1.44	1.92	0.96	1.30	0.14	1.90	0.10	1.35	3.15
Real(Y12)(%)	1.44	1.92	0.96	1.30	0.14	1.90	0.10	1.35	3.15
Real(Y22)(%)	1.44	1.90	0.95	1.30	0.12	1.90	0.12	1.34	3.13
Imag(Y11)(%)	9.26	0.88	4.42	0.77	0.34	0.37	0.94	0.29	0.49
Imag(Y21)(%)	9.24	0.87	4.41	0.78	0.38	0.39	0.94	0.29	0.46
Imag(Y12)(%)	9.24	0.87	4.41	0.78	0.38	0.39	0.94	0.29	0.46
Imag(Y22)(%)	9.26	0.88	4.42	0.77	0.34	0.36	0.94	0.28	0.48

Table 12.17.16: Fitting errors (Real and Imaginary) for mu_z symmetric inductor with W=6μm , gdis=50μm, spacing=3μm.

N (turns)	3	5	3	5	3	5	1	3	5
R(radius in μm)	15	15	30	30	60	60	90	90	90
Real(Y11)(%)	8.99	5.48	1.73	7.14	0.24	3.80	1.82	3.27	1.25
Real(Y21)(%)	8.99	5.48	1.73	7.15	0.23	3.81	1.82	3.28	1.26
Real(Y12)(%)	8.99	5.48	1.73	7.15	0.23	3.81	1.82	3.28	1.26
Real(Y22)(%)	8.99	5.48	1.74	7.14	0.25	3.80	1.82	3.27	1.25
Imag(Y11)(%)	7.12	0.40	0.76	1.58	0.89	0.86	4.08	1.27	0.90
Imag(Y21)(%)	7.11	0.41	0.76	1.59	0.91	0.88	4.07	1.27	0.90
Imag(Y12)(%)	7.11	0.41	0.76	1.59	0.91	0.88	4.07	1.27	0.90
Imag(Y22)(%)	7.12	0.40	0.75	1.58	0.89	0.85	4.08	1.27	0.90

Table 12.17.17: Fitting errors (Real and Imaginary) for mu_z symmetric inductor with W=9μm , gdis=50μm, spacing=3μm.

N (turns)	3	5	3	5	3	5	1	3	5
R(radius in μm)	15	15	30	30	60	60	90	90	90
Real(Y11)(%)	3.55	2.55	0.86	0.99	2.70	2.77	0.78	1.07	3.15
Real(Y21)(%)	3.55	2.57	0.85	1.00	2.70	2.75	0.77	1.06	3.13
Real(Y12)(%)	3.55	2.57	0.85	1.00	2.70	2.75	0.77	1.06	3.13
Real(Y22)(%)	3.55	2.55	0.86	1.00	2.70	2.77	0.77	1.08	3.16
Imag(Y11)(%)	1.57	0.39	0.31	0.43	1.05	0.44	2.30	0.13	0.38
Imag(Y21)(%)	1.57	0.37	0.32	0.40	1.05	0.40	2.29	0.14	0.30
Imag(Y12)(%)	1.57	0.37	0.32	0.40	1.05	0.40	2.29	0.14	0.30
Imag(Y22)(%)	1.57	0.39	0.31	0.43	1.05	0.45	2.30	0.14	0.40

Table 12.17.18: Fitting errors (Real and Imaginary) for mza_a symmetric inductor with W=15μm , gdis=50μm, spacing=3μm.

N (turns)	3	5	3	5	3	5
R(radius in μm)	20	20	55	55	90	90
Real(Y11)(%)	4.57	1.26	6.66	6.71	7.42	1.47
Real(Y21)(%)	4.58	1.36	6.70	6.97	7.50	0.92
Real(Y12)(%)	4.58	1.36	6.70	6.97	7.50	0.92
Real(Y22)(%)	4.57	1.30	6.66	6.73	7.43	1.57
Imag(Y11)(%)	2.66	1.58	1.09	0.83	0.74	0.38
Imag(Y21)(%)	2.64	1.50	1.07	0.77	0.71	0.13
Imag(Y12)(%)	2.64	1.50	1.07	0.77	0.71	0.13
Imag(Y22)(%)	2.66	1.58	1.09	0.84	0.74	0.40

Table 12.17.19: Fitting errors (Real and Imaginary) for mza_a symmetric inductor with W=30μm, gdis=50μm, spacing=3μm.

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N (turns)	3	5	3	5	3	5	1	3	5
R(radius in μm)	15	15	30	30	60	60	90	90	90
Real(Y11)(%)	0.50	0.16	1.90	0.15	0.72	1.55	1.77	0.18	0.29
Real(Y21)(%)	0.50	0.19	1.90	0.15	0.72	1.55	1.77	0.17	0.23
Real(Y12)(%)	0.50	0.19	1.90	0.15	0.72	1.55	1.77	0.17	0.23
Real(Y22)(%)	0.50	0.17	1.90	0.15	0.72	1.56	1.77	0.19	0.30
Imag(Y11)(%)	1.89	1.06	3.51	3.70	1.88	2.86	2.87	2.23	1.87
Imag(Y21)(%)	1.88	1.06	3.49	3.67	1.86	2.81	2.85	2.19	1.82
Imag(Y12)(%)	1.88	1.06	3.49	3.67	1.86	2.81	2.85	2.19	1.82
Imag(Y22)(%)	1.89	1.06	3.51	3.70	1.89	2.86	2.87	2.23	1.87

Table 12.17.20: Fitting errors (Real and Imaginary) for mza_a symmetric inductor with W=7.5μm , gdis=50μm, spacing=3μm.

N (turns)	3	5	3	5	3	5	3	5
R(radius in μm)	15	15	30	30	60	60	90	90
Real(Y11)(%)	14.37	14.18	10.91	14.92	6.07	1.61	1.82	0.45
Real(Y21)(%)	14.36	14.22	10.89	15.01	6.08	1.60	1.86	0.46
Real(Y12)(%)	14.36	14.22	10.89	15.01	6.08	1.60	1.86	0.46
Real(Y22)(%)	14.38	14.18	10.91	14.93	6.07	1.58	1.81	0.43
Imag(Y11)(%)	5.16	0.55	1.63	0.92	0.37	0.21	0.21	0.33
Imag(Y21)(%)	5.15	0.55	1.63	0.92	0.39	0.26	0.25	0.49
Imag(Y12)(%)	5.15	0.55	1.63	0.92	0.39	0.26	0.25	0.49
Imag(Y22)(%)	5.16	0.56	1.63	0.93	0.38	0.23	0.23	0.35

Table 12.17.21: Fitting errors (Real and Imaginary) for mu_a symmetric inductor with W=15μm , gdis=50μm, spacing=3μm.

N (turns)	3	5	3	5	3	5
R(radius in μm)	20	20	55	55	90	90
Real(Y11)(%)	5.95	2.30	17.66	1.77	5.70	1.14
Real(Y21)(%)	5.97	2.38	17.80	1.79	5.80	1.55
Real(Y12)(%)	5.97	2.38	17.80	1.79	5.80	1.55
Real(Y22)(%)	5.96	2.30	17.67	1.70	5.70	0.99
Imag(Y11)(%)	3.32	2.35	2.29	0.45	1.37	0.28
Imag(Y21)(%)	3.30	2.31	2.28	0.40	1.35	0.10
Imag(Y12)(%)	3.30	2.31	2.28	0.40	1.35	0.10
Imag(Y22)(%)	3.32	2.35	2.29	0.46	1.37	0.26

Table 12.17.22: Fitting errors (Real and Imaginary) for mu_a symmetric inductor with W=30μm , gdis=50μm, spacing=3μm.

N (turns)	3	5	3	5	3	5	3	5
R(radius in μm)	30	30	60	60	90	90	90	90
Real(Y11)(%)	1.90	1.56	0.68	0.36	3.18	2.81	2.05	1.46
Real(Y21)(%)	1.89	1.56	0.68	0.35	3.18	2.81	2.06	1.46
Real(Y12)(%)	1.89	1.56	0.68	0.35	3.18	2.81	2.06	1.46
Real(Y22)(%)	1.90	1.56	0.68	0.36	3.19	2.80	2.05	1.46
Imag(Y11)(%)	1.71	2.19	2.24	1.96	0.61	1.73	0.91	1.73
Imag(Y21)(%)	1.71	2.18	2.23	1.95	0.62	1.71	0.93	1.72
Imag(Y12)(%)	1.71	2.18	2.23	1.95	0.62	1.71	0.93	1.72
Imag(Y22)(%)	1.71	2.19	2.24	1.96	0.60	1.72	0.91	1.73

Table 12.17.23: Fitting errors (Real and Imaginary) for mu_a symmetric inductor with W=6.2μm , gdis=50μm, spacing=3μm.

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N (turns)	3	5	3	5	3	5	3	5
R(radius in μm)	15	15	30	30	60	60	90	90
Real(Y11)(%)	2.87	2.99	1.70	2.54	1.28	0.18	4.12	1.83
Real(Y21)(%)	2.86	2.99	1.69	2.55	1.29	0.15	4.12	1.83
Real(Y12)(%)	2.86	2.99	1.69	2.55	1.29	0.15	4.12	1.83
Real(Y22)(%)	2.87	2.99	1.70	2.55	1.29	0.20	4.12	1.82
Imag(Y11)(%)	4.63	0.39	1.02	0.26	0.29	0.16	0.96	0.19
Imag(Y21)(%)	4.61	0.39	1.01	0.27	0.30	0.21	0.99	0.19
Imag(Y12)(%)	4.61	0.39	1.01	0.27	0.30	0.21	0.99	0.19
Imag(Y22)(%)	4.63	0.39	1.02	0.26	0.30	0.18	0.96	0.20

Table 12.17.24: Fitting errors (Real and Imaginary) for mu_a symmetric inductor with W=9μm , gdis=50μm, spacing=3μm.

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12.17.5 Corner Model Table

Table 12.17.25 lists the skew parameters for the slow-corner (SS), typical (TT) and fast-corner (FF) cases. Please refer to Table 1-1 of T-N65-CM-SP-007 for library names.

Skew Parameter	SS	TT	FF
rm9_indfac	1.1	1.0	0.9
cm9_indfac	1.07	1.0	0.913
c12_indfac	1.081	1.0	0.926
rsub_indfac	1.2	1.0	0.8
csub_indfac	0.8333	1.0	1.25
l_indfac	1.0235	1.0	0.9762

Table 12.17.25: Parameters and values for inductor corner cases.

12.17.6 Temperature Effect Model

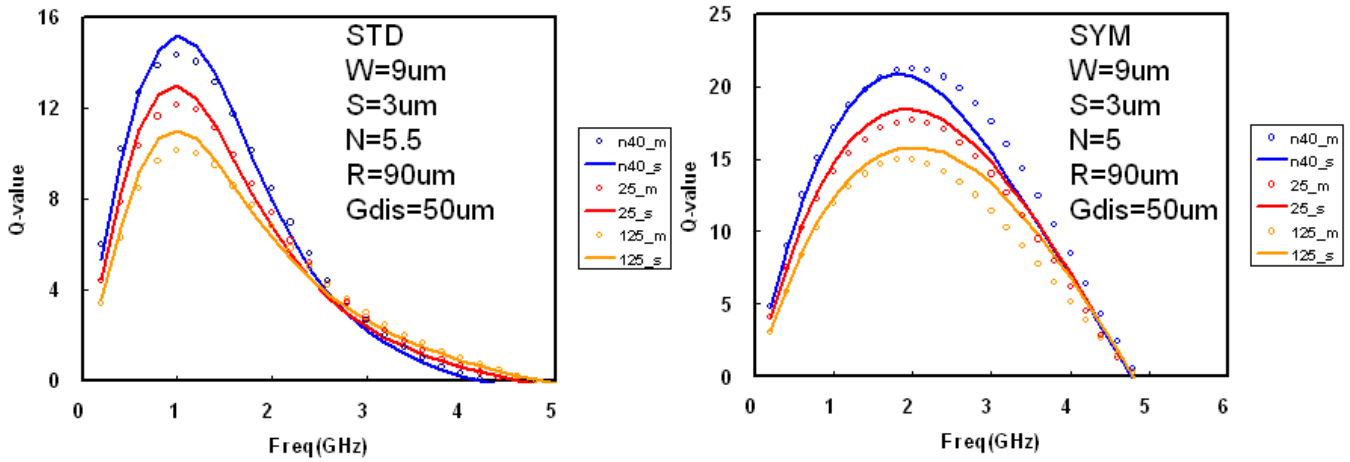
The temperature effects have been analyzed by S-parameter measurements at three temperatures, -40℃, 25℃, and 125℃, for both the standard and symmetric inductors. The following functions have been implemented to model the temperature effects.

$$R(T)=R*(0.0026*(temper-25)+1)$$

$$Rs(T)=Rs*(0.0026*(temper-25)+1)^{0.5}$$

$$Rsub(T)=Rsub*(-0.0000114*(temper-25)*(temper-25)+0.0046*(temper-25)+1)$$

The temperature effects on the quality factor (Q) are determined primarily by the temperature coefficients (TCR) of the spiral metal (e.g., UTM) and substrate resistances. Both materials have positive temperature coefficients, but their effects on the quality factor are different. As temperature increases, the resistance in the spiral metal causes the quality factor to decrease, while the resistance in the substrate improves the quality factor at high frequencies. Fig. 12.17.5 (a) shows the simulated and measured data for a 1P9M standard inductor at temperatures -40℃, 25℃, and 125℃. Fig. 8-5(b) shows the data for a 1P9M symmetric inductor.



Circle: Measured; Line: Simulated

(a) (b)

Fig. 12.17.5: Temperature effect of mu_z standard inductor (a), and symmetric inductor (b).

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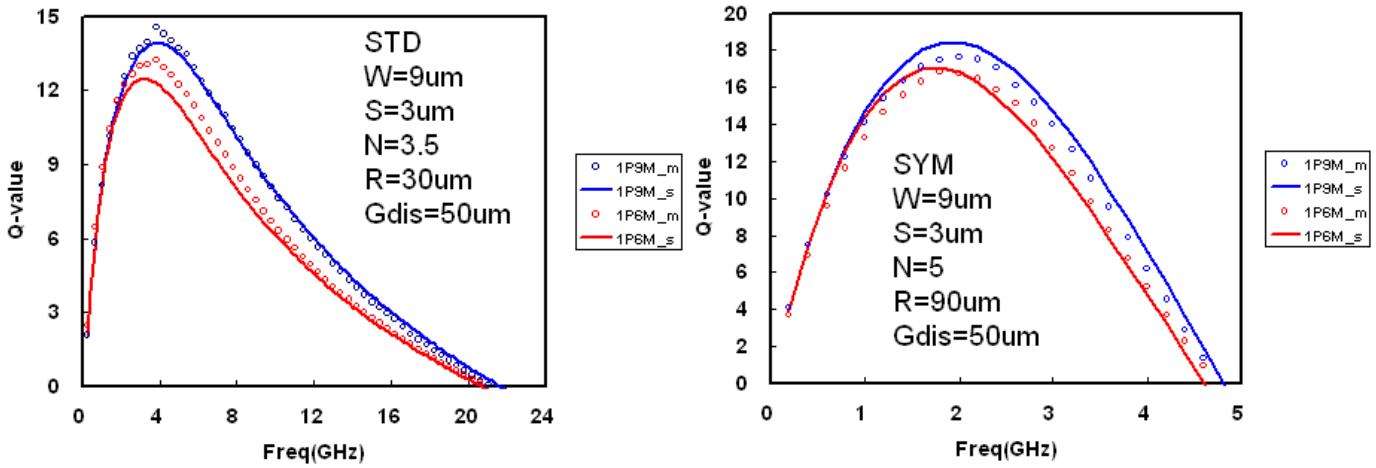
12.17.7 Variable Metal Layer Model

Inductors using different metal layers (1P5M to 1P9M) have different capacitances over the substrate (Cox). The higher the metal layer the lower the Cox, which results in a higher quality factor. Inductors fabricated in three processes, 1P6M and 1P9M for Mu_z or 1P4M and 1P8M for Mza_a and Mu_a, have been characterized to model the effects of the different metal layers. The following function has been implemented in the model.

Cox (layer)=Cox(layer=9)*[(1/(12.5039+(1.7014)*(layer-3)))/(0.0444)]

Fig. 12.17.6 (a) shows the simulated and measured data for mu_z standard inductors processed with 1P6M, and 1P9M. Fig. 12.17.6 (b) shows the results for mu_z symmetric inductors.



Circle: Measured; Line: Simulated

(a) (b)

Fig. 12.17.6: Effects of different metal layer: (a) standard inductors; (b) symmetric inductors.

12.17.8 Statistical Model

In this version inductor provides statistical model and their corresponding corner models. Whenever the corners of inductor were provided, their statistical model was made accordingly based on PCA result. Statistical libraries for Monte-Carlo simulation are denoted by MC. RF models are labeled as “RFIND”. For example, the library “TT_RFIND” is for typical RF model; “MC_RFIND” for statistical RF model. The simulation results with corner of inductor are shown in Fig. 12.17.7.

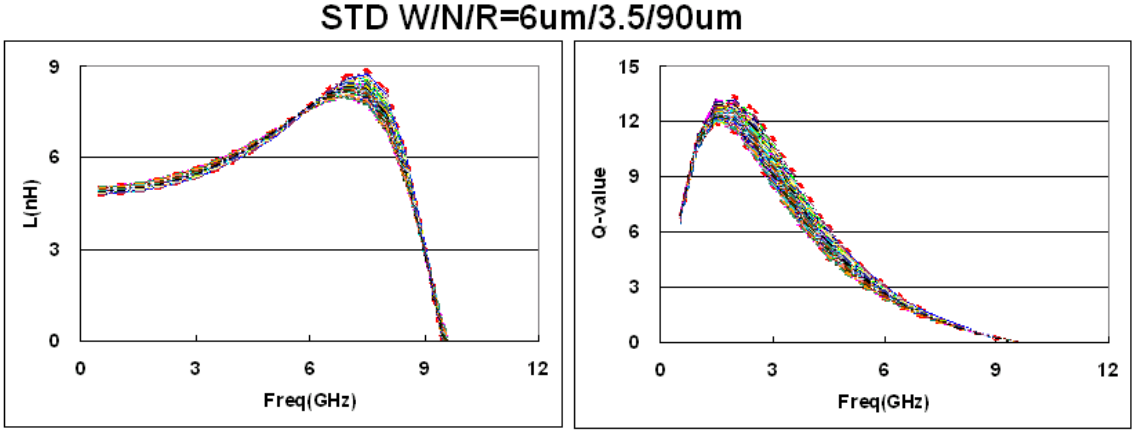


Fig. 12.17.7: Simulation results of 250 Monte-Carlo random tests.

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12.18 RF I/O PAD MODEL

12.18.1 Model Usage Guide

Low-capacitance pads used for input/output (I/O) ESD low-capacitance purpose are modeled for high-frequency application based on the one-port S-parameter measurement and Y-parameter fitting. The pads are scalable both in width (wt = 47~80um) and length (lt = 47~80um). Four different metal schemes (1PXM, X=6,7,8, and 9 for MuMz scheme) are available by using “lay” as parameter. Dummy metal with two different dummy-metal densities (15% and 23%) underneath MuMz metal layers can be utilized for design flexibility (lowcpad_d15 for 15% and lowcpad_d23 for 23%). The usage example of this RF I/O pad is given as follows.

Usage Example:

To use a low-capacitance pad with size 50um by 50um with dummy-metal density 15% in 1P9M metal scheme:

```
X_lowcpad APAD 0 lowcpad_d15 wt=50u lt=50u lay=9
```

12.18.2 Test Structure and Measurement Procedure

The cross section of low-capacitance pads are shown in Fig. 12.18.1. Solid rectangular pads located in M_{top} (Mu) and M_{top-1} (Mz) layers are connected with each other by vias. Dummy metal layers inserted from M_1 to M_{top-2} with two different metal densities (15% and 23%) are available. Poly shielding is adopted just beneath M_1. One-port S-parameter measurements are performed from 200MHz to 20GHz.

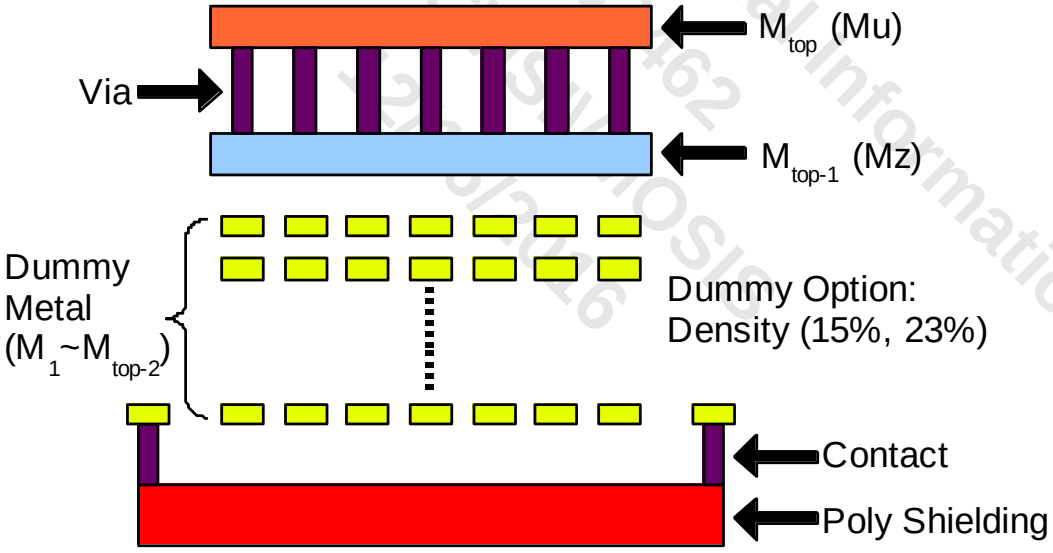

Fig. 12.18.1: Cross-section of the RF I/O low-capacitance pad.

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12.18.3 Equivalent Circuit and Model Scaling Rule

The equivalent circuit model of this RF pad can be simply considered as a lumped capacitor since the extracted capacitance from admittance (Y) matrix varies slightly with frequency. In addition, the parasitic resistance value is of μΩ order thus can almost be neglected. For use convenience, three pad subcircuits are built for three different dummy-metal densities. The scaling equations for the capacitance which can be empirically determined, are shown in Table 12.18.1.

	Density	Element	Scaling Equation
lowcpad_d15	15 %	cpad (F)	(0.0186*lt*scale*wt*scale*1e12+2.4107)*(0.0171*lay**2 - 0.3719*lay + 2.6155)*1e-15
lowcpad_d23	23 %	cpad (F)	(0.0197*lt*scale*wt*scale*1e12+1.4200)*(0.0164*lay**2 - 0.3622*lay + 2.5815)*1e-15

Table 12.18.1: Scaling equations for the equivalent-circuit elements of low-capacitance pad.

12.18.4 Modeled Capacitance and Model Error Table

12.18.4.1 Modeled and Measured Capacitance

Modeled and measured capacitance of the equivalent circuit elements for the ten low-capacitance pad samples in 1P6M and 1P9M metal schemes are shown in Table 12.18.2 for demonstration. Note that pads with 0% dummy density are used for width and length scaling purpose and pad model with this 0% dymmy density is not provided.

		1P6M		1P9M	
Size (wt * lt)	Dummy Metal Density	Capacitance (cpad)		Capacitance (cpad)	
		Modeled	Measured	Modeled	Measured
44um * 44um	0 %	36.64 fF	34.36 fF	24.44 fF	23.73 fF
50um * 50um	0 %	45.4 fF	43.44 fF	30.28 fF	30.10 fF
80um * 80um	0 %	105.9 fF	105.0 fF	70.65 fF	72.41 fF
50um * 50um	15 %	48.9 fF	46.26 fF	31.96 fF	31.83 fF
50um * 50um	23 %	50.6 fF	47.67 fF	32.94 fF	33.50 fF

Table 12.18.2: Modeled and measured capacitaqnce for the ten low-capacitance pad samples.

12.18.4.2 Fitting Error Table

Fitting errors of imaginary part of Y11 between measurement and simulation results for the ten low-capacitance pad samples in 1P6M and 1P9M metal schemes, summarized in Table 12.18.3, are obtained according to the calculation equations given in Chapter 13 of T-N65-CM-SP-007.

		1P6M	1P9M
Size (wt * lt)	Dummy Metal Density	Fitting Error imag(Y11)	Fitting Error imag(Y11)
44um * 44um	0 %	7.29287 %	3.98673 %
50um * 50um	0 %	4.97394 %	1.34188 %
80um * 80um	0 %	1.41830 %	1.77413 %
50um * 50um	15 %	6.00569 %	1.15426 %
50um * 50um	23 %	6.60680 %	1.08686 %

Table 12.18.3: Fitting errors (Imaginary part of Y11).

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Appendix A Revision History

A.1 T-N65-CL-DR-001 (Logic)

A.1.1 From Version 0.1 to Version 0.2

	From Version 0.1 to Version 0.2			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.		3.3	Dummy Pattern CAD Layers	Modifies Table 3.3.1 for metal datatypes.
2.		3.4	Special Recognition CAD Layer Summary	Adds new CAD layers, SRAMDMY;1, CO;11, RRuleRequire, RRuleRecommend, RRuleAnalog, and FILLER. Modifies the CAD layers, SRAMDMY;0 and SRAMDMY;4.
3.	G.5	3.7.1	Design Geometry Rules	Adds the rule.
4.	OPC.R.1®	3.7.2	OPC Recommendations and Guidelines	Adds the recommendation.
5.	OPC.R.2g^{U}	3.7.2	OPC Recommendations and Guidelines	Adds the guideline.
6.	DNW.S.6/ DNW.EN.2	4.5.1	DNW Layout Rules	Adds the rules.
7.	OD.S.3	4.5.2	OD Layout Rules	Changes the entire rule and figure.
8.	OD.S.3.1	4.5.2	OD Layout Rules	Changes the entire rule and figure.
9.	OD.S.6®	4.5.2	OD Layout Rules	Adds the recommendation.
10.	OD.W.1®	4.5.2	OD Layout Rules	Deletes the recommendation of “Recommended minimum interconnect OD width ≥ 0.11”.
11.	NW.S.6.1/ NW.EN.2.1	4.5.3	NW Layout Rules	Adds the rules.
12.	NT_N.EN.1	4.5.6	NT_N Layout Rules	Modifies the rule as a range.
13.	PO.R.6/PO.DN.3/ PO.DN.4	4.5.8	PO Layout Rules	Adds the rules.
14.	PO.DN.1	4.5.8	PO Layout Rules	Changes the rule from “≤ 50%” to “≤ 40%”.
15.	PO.EX.2	4.5.8	PO Layout Rules	Changes the rule from “0.13” to “0.115”.
16.	PO.S.1.1®	4.5.8	PO Layout Rules	Adds the recommendation.
17.	PO.S.11®	4.5.8	PO Layout Rules	Adds the recommendation.
18.	PO.S.12®	4.5.8	PO Layout Rules	Adds the recommendation.
19.	PO.S.13®	4.5.8	PO Layout Rules	Adds the recommendation.
20.	PO.S.14®	4.5.8	PO Layout Rules	Adds the recommendation.
21.	PO.EN.1®	4.5.8	PO Layout Rules	Adds the recommendation.
22.	PO.EN.2®	4.5.8	PO Layout Rules	Adds the recommendation.
23.	PO.EN.3®	4.5.8	PO Layout Rules	Adds the recommendation.
24.	PO.W.1®	4.5.8	PO Layout Rules	Deletes the recommendation.
25.	PO.A.3®	4.5.8	PO Layout Rules	Deletes the recommendation.
26.	VTH_N.W.1	4.5.9	VTH_N Layout Rules	Changes the rule from “0.28” to “0.18”.
27.	VTH_N.S.3	4.5.9	VTH_N Layout Rules	Changes the rule from “0.26” to “0.22”.
28.	VTH_P.W.1	4.5.10	VTH_P Layout Rules	Changes the rule from “0.28” to “0.18”.
29.	VTH_P.S.3	4.5.10	VTH_P Layout Rules	Changes the rule from “0.26” to “0.22”.
30.	VTL_N.W.1	4.5.11	VTL_N Layout Rules	Changes the rule from “0.28” to “0.18”.
31.	VTL_N.S.3	4.5.11	VTL_N Layout Rules	Changes the rule from “0.26” to “0.22”.
32.	VTL_P.W.1	4.5.12	VTL_P Layout Rules	Changes the rule from “0.28” to “0.18”.
33.	VTL_P.S.3	4.5.12	VTL_P Layout Rules	Changes the rule from “0.26” to “0.22”.
34.	PP.EX.2®	4.5.13	PP Layout Rules	Deletes the recommendation.
35.	NP.EX.2®	4.5.13	NP Layout Rules	Deletes the recommendation.
36.	RES.8g	4.5.17	OD and PO Resistor Guidelines	Adds the guideline.
37.	RES.9g	4.5.17	OD and PO Resistor Guidelines	Adds the guideline.
38.		4.5.18	MOS Varactor Layout Rules	Adds the section.
39.	CO.EN.1.1	4.5.19	CO Layout Rules	Adds the rule.
40.	CO.EN.2	4.5.19	CO Layout Rules	Changes the rule from “0.02” to “0.01”.
41.	CO.R.7g^{U}	4.5.19	CO Layout Rules	Adds the guideline.
42.	M1.DN.4	4.5.20	M1 Layout Rules	Adds the rule.
43.	M1.S.2	4.5.20	M1 Layout Rules	Modifies the parallel metal run length from “> 0.42 μm” to “> 0.38 μm”.
44.	M1.DN.1	4.5.20	M1 Layout Rules	Modifies the lower density window from “100x100” to “50x50”.
45.	M1.DN.3	4.5.20	M1 Layout Rules	Modifies the lower density window from “100x100” to “25x25”.
46.	M1.S.1®	4.5.20	M1 Layout Rules	Adds the recommendation.

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	From Version 0.1 to Version 0.2			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
47.	M1.S.7®	4.5.20	M1 Layout Rules	Adds the recommendation.
48.	M1.DN.3®	4.5.20	M1 Layout Rules	Adds the recommendation.
49.	VIAx.EN.1®	4.5.21	VIAx Layout Rules	Adds the recommendation.
50.	VIAx.R.10g^{U}	4.5.21	VIAx Layout Rules	Adds the guideline.
51.	Mx.DN.4/Mx.R.3	4.5.22	Mx Layout Rules	Adds the rules.
52.	Mx.DN.1	4.5.22	Mx Layout Rules	Modifies the lower density window from “100x100” to “50x50”.
53.	Mx.DN.3	4.5.22	Mx Layout Rules	Modifies the lower density window from “100x100” to “25x25”.
54.	Mx.W.4®	4.5.22	Mx Layout Rules	Adds the recommendation.
55.	Mx.S.1®	4.5.22	Mx Layout Rules	Adds the recommendation.
56.	Mx.S.7®	4.5.22	Mx Layout Rules	Adds the recommendation.
57.	Mx.EN.1®	4.5.22	Mx Layout Rules	Adds the recommendation.
58.	Mx.DN.3®	4.5.22	Mx Layout Rules	Adds the recommendation.
59.	Mx.R.2g^{U}	4.5.22	Mx Layout Rules	Adds the guideline.
60.	VIAz.R.6g^{U}	4.5.23	VIAz Layout Rules	Adds the guideline.
61.	Mz.DN.1	4.5.24	Mz Layout Rules	Modifies the lower density window from “100x100” to “50x50”.
62.	Mz.DN.3	4.5.24	Mz Layout Rules	Modifies the lower density window from “100x100” to “25x25”.
63.	Mz.W.3®	4.5.24	Mz Layout Rules	Adds the recommendation.
64.	Mz.R.2g^{U}	4.5.24	Mz Layout Rules	Adds the guideline.
65.	AP.S.1	4.5.26	Al RDL Layout Rules	Changes the rule from “3” to “2”.
66.	AP.DN.1	4.5.26	Al RDL Layout Rules	Changes the higher bound density from “50% to “70%”.
67.	SRAM.EX.1	4.5.29	SRAM Rules	Adds the rule.
68.	SRAM.O.1	4.5.29	SRAM Rules	Adds the rule.
69.	SRAM.R.12	4.5.29	SRAM Rules	Adds the rule.
70.	SRAM.R.13	4.5.29	SRAM Rules	Adds the rule.
71.	SRAM.R.14	4.5.29	SRAM Rules	Adds the rule.
72.	SRAM.R.15	4.5.29	SRAM Rules	Adds the rule.
73.	SRAM.R.16^{U}	4.5.29	SRAM Rules	Adds the rule.
74.	SRAM.R.7^{U}	4.5.29	SRAM Rules	Adds the description “SRAMDMY_4 (186;4) is a must for CO mask tape-out if SRAM decoder is rule pushed.”
75.	SRAM.W.1	4.5.29	SRAM Rules	Changes the rule from “0.47” to “0.28”.
76.	SRAM.S.1	4.5.29	SRAM Rules	Changes the rule from “0.47” to “0.28”.
77.	SRAM.S.2	4.5.29	SRAM Rules	Changes the rule from “0.2” to “0.12”.
78.	SRAM.EN.1	4.5.29	SRAM Rules	Changes the rule from “0.2” to “0.12”.
79.		4.5.31	CSR Layout Rules	Adds the section.
80.		4.5.32	Seal Ring Layout Rules	Adds the section.
81.	DMx.S.3.1	5.3	DM Rules	Adds the rule.
82.	DMx.W.1	5.3	DM Rules	Changes the rule from “0.32” to “0.3” for M1/Mx.
83.	DMx.S.1	5.3	DM Rules	Changes the rule from “0.4” to “0.3” for M1/Mx.
84.	DMx.S.2	5.3	DM Rules	Changes the rule from “0.6” to “0.3” for M1/Mx.
85.	DMx.A.1	5.3	DM Rules	Changes the rule from “0.32” to “0.24” for M1/Mx. Changes the rule from “0.6” to “0.565” for Mz.
86.	DMx.W.1g^{U}	5.3	DM Rules	Modifies the table.
87.		6	Design for Manufacturing	Modifies the entire chapter.
88.	ESD.46g^{U}	7.2.4	ESD Guidelines	Adds the guideline.
89.	ESD.47g^{U}	7.2.4	ESD Guidelines	Adds the guideline.
90.	ESD.2g	7.2.4	ESD Guidelines	Modifies the description by adding “(for gate poly width ≥ 0.13μm)”.
91.	ESD.35g	7.2.4	ESD Guidelines	Changes the guideline number from “20” to “10”.
92.	ESD.14g^{U}	7.2.4	ESD Guidelines	Changes the dimensions of 1.0V or 1.2V I/O NMOS and PMOS from “20/0.15” to “20/0.1”.
93.		8.1	Back-end Process Reliability Rules	Modifies the entire section.

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A.1.2 From Version 0.2 to Version 0.3

	From Version 0.2 to Version 0.3			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.		3.1	Mask Information, Key Process Sequence, & CAD Layer	Modifies Table 3.1.1 & Table 3.1.3.
2.		3.4	Special Recognition CAD Layer Summary	Adds the layer usage of SRAMDMY_5 (186;5).
3.		3.6	Mask Requirement for Device Options	Modifies Table 3.6.1.
4.	G.1	3.7.1	Design Geometry Rules	Modifies the layer 186;4 as 186;5 in the rule description.
5.	NT_N.W.2.1	4.5.6	Native Device Layout Rules	Adds this rule.
6.	PO.S.13®	4.5.8	PO Layout Rules	Changes the rule numbers **from** "0.14~0.19/0.27~0.3/0.39~0.46" **to** "0.14~0.185/0.27~0.295/0.39~0.455".
7.	PO.DN.4	4.5.8	PO Layout Rules	Modifies the rule description of checking window **from** "25 μm x 25 μm" **to** "30 μm x 30 μm".
8.	CO.S.3	4.5.19	CO Layout Rules	Modifies the rule description **from** "[space can be ≥ 0.043 μm inside SRAM word line decoder covered by layer 186;4]" **to** "[space can be ≥ 0.05 μm inside SRAM word line decoder covered by layer 186;4, and space ≥ 0.043 μm covered by 186;5]".
9.		4.5.30	SRAM Periphery Rules	Adds the section for layout rules in word line decoder.
10.		5.3	Dummy Metal Rules	Changes the width/space rules of dummy Mz.
11.		6	Design for Manufacturing	Modifies some wordings.
12.		7	Layout Guidelines for Latch-up and I/O ESD	Modifies the entire chapter to remove 3.3V part.

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A.1.3 From Version 0.3 to Version 1.0

	From Version 0.3 to Version 1.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1		3.1	Mask Information, Key Process Sequence, & CAD Layer	Modifies Table 3.1.1 & Table 3.1.2.
2		3.4	Special Recognition CAD Layer Summary	Adds the layer usage of Ncap_NTN (11;20), BJTDMY(110;0).
3		3.5.2	Device Truth Tables	Modifies Table 3.5.3
4		3.5.3	Device Truth Tables	Deletes the section
5	NW.S.6.1/ NW.EN.2.1	4.5.3	NW Layout Rules	Changes the rule from “0.22” to “0.19”.
6	NWROD.R.1®	4.5.4	N-Well Within OD Layout Rules	Modifies the recommendation.
7	NWRSTI.R.1®	4.5.5	N-Well Within STI Layout Rules	Adds the recommendation.
8	NT_N.W.2.2	4.5.6	Native Device Layout Rules	Adds the rule.
9	OD2.R.2^{U}	4.5.7	OD2 Layout Rules	Adds the rule.
10	PO.S.5®	4.5.8	PO Layout Rules	Modifies the recommendation.
11	PO.S.13®	4.5.8	PO Layout Rules	Modifies the recommendation.
12	PO.EX.4®	4.5.8	PO Layout Rules	Adds the rule.
13	PO.EX.5®	4.5.8	PO Layout Rules	Adds the rule.
14	PO.DN.4	4.5.8	PO Layout Rules	Modifies the rule
15	VTH_N.R.2	4.5.9	VTH_N Layout Rules	Adds the rule.
16	VTH_P.R.2	4.5.10	VTH_P Layout Rules	Adds the rule.
17	VTL_N.R.2	4.5.11	VTL_N Layout Rules	Adds the rule.
18	VTL_P.R.2	4.5.12	VTL_P Layout Rules	Adds the rule.
19		4.5.13	mVTL Layout Rules	Adds the section for layout rules
20	CO.EN.0/ CO.EN.4	4.5.20	CO Layout Rules	Adds the rules.
21	CO.EN.1	4.5.20	CO Layout Rules	Modifies the rule.
20	CO.EN.1.1	4.5.20	CO Layout Rules	Modifies the rule.
21	CO.EN.1.2	4.5.20	CO Layout Rules	Adds the rule.
22	M1.S.5	4.5.21	M1 Layout Rules	Modifies the rule.
23	Mx.S.5	4.5.23	Mx Layout Rules	Modifies the rule.
24	SRAM.R.4^{U}	4.5.30	SRAM Layout Rules	Modifies the rule
25	SRAM.R.17	4.5.30	SRAM Layout Rules	Adds the rule.
26	WLD.R.5	4.5.31	SRAM Periphery Rules	Deletes the rule.
27	WLD.R.7	4.5.31	SRAM Periphery Rules	Adds the rule.
28		5	Layout Rules and Recommendations for Analog Circuits	Adds the chapter
29		6.3	Dummy Metal Rules	Modifies some wordings.
30	DMx.S.10	6.3	Dummy Metal Rules	Adds the rule.
31		6.4	Dummy Pattern Fill Usage Summary	Modifies some wordings.
32		7	Design for Manufacturing	Modifies some wordings.

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A.1.4 From Version 1.0 to Version 1.1

	From Version 1.0 to Version 1.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.		1.1	Overview	Adds CLN65G+ technology
2.		1.2	Reference Documentation	Modifies Table 1.2.1
3.		1.3	Guidelines for Half Node Technologies (CLN65 only)	Adds the section
4.		2.1.1	Front-End Features	Modifies GateOX, SRAM, Varactor informations
5.		2.1.2	Back-End Features	Adds My selections for inter-layer and top-layer.
6.		2.2	Devices	Modifies Table 2.2.1
7.		2.3	Power Supply and Operation Temperature Ranges	Modifies Table 2.3.1
8.		2.4	Cross–section	Modifies Fig. 2.41, Fig. 2.4.2, Fig.2.4.3
9.		2.5	Metallization Options	Modifies Table 2.5.1 to Table 2.5.5
10.		3.1	Mask Information, Key Process Sequence, and CAD Layers	Modifies Table 3.1.1 to Table 3.1.8
11.		3.2	Metal/Via CAD Layer Information for Metallization Options	Adds data type 20 for VIAy/My
12.		3.3	Dummy Pattern Fill CAD Layers	Adds data type 21 for DMy
13.		3.4	Special Recognition CAD Layer Summary	Adds special layers, POFUSE, OD25_33, OD25_18
14.		3.5	Device Truth Tables	Modifies Table 3.5.1 to Table 3.5.4
15.		3.6	Mask Requirement for Device options (High/STD/Low VT)	Modifies Table 3.6.1
16.	G.5	3.7.1	Design Geometry Rules	Modifies reserved layers (adding 40, removing 168)
17.		4.2.1	Derived Geometries	Modifies OD2 definition (including OD_33)
18.		4.3	Definition of Layout Geometrical Terminology	Adds Definition of cut, channel width, and channel length
19.		4.4	Minimum Pitches	Adds VIAy/My minimum pitches.
20.	DNW.S.3	4.5.1	DNW Layout Rules	Changes the rule from “1.32” to “1.65”.
21.	DNW.S.4	4.5.1	DNW Layout Rules	Modifies the rule (PW is considered)
22.	DNW.S.5	4.5.1	DNW Layout Rules	Modifies the rule (PW is considered)
23.	DNW.S.6	4.5.1	DNW Layout Rules	Modifies the rule (DNW cut PMOS gate is not allowed)
24.	DNW.S.7	4.5.1	DNW Layout Rules	Adds the rule
25.	DNW.EN.1®	4.5.1	DNW Layout Rules	DNW.EN.1 is changed to DNW.EN.1®
26.	DNW.R.1	4.5.1	DNW Layout Rules	Deletes the rule.
27.	DNW.R.5	4.5.1	DNW Layout Rules	Adds the rule.
28.	OD.W.3	4.5.2	OD Layout Rules	Modifies the rule (3.3V is considered)
29.	OD.S.3	4.5.2	OD Layout Rules	Modifies the rule
30.	OD.S.3.1	4.5.2	OD Layout Rules	Modifies the rule
31.	OD.DN.3	4.5.2	OD Layout Rules	Modifies the rule
32.	OD.R.1	4.5.2	OD Layout Rules	Changes the description from “DOD” to “{DOD OR NWDMY}”.
33.	NW.S.6.1	4.5.3	NW Layout Rules	Deletes the rule
34.	NW.EN.2.1	4.5.3	NW Layout Rules	Deletes the rule
35.	NWROD.S.3®	4.5.4	NWROD Layout Rules	Adds the recommendation.
36.	NWROD.R.2g	4.5.4	NWROD Layout Rules	Adds the guideline.
37.	NWROD.R.3g	4.5.4	NWROD Layout Rules	Adds the guideline.
38.	NWRSTI.EN.2®	4.5.5	NWRSTI Layout Rules	Adds the recommendation.
39.	NWRSTI.R.2g	4.5.5	NWRSTI Layout Rules	Adds the guideline.
40.	NWRSTI.R.3g	4.5.5	NWRSTI Layout Rules	Adds the guideline.
41.	NT_N.W.2	4.5.6	NT_N Layout Rules	Modifies the rule (1.05V is removed)
42.	NT_N.W.3	4.5.6	NT_N Layout Rules	Modifies the rule (3.3V is added)
43.	NT_N.S.2	4.5.6	NT_N Layout Rules	Modifies the rule (OD is changed to Active)
44.	NT_N.R.2	4.5.6	NT_N Layout Rules	Deletes the rule.
45.	OD2.S.3	4.5.7	OD2 Layout Rules	Modifies the rule (in S/D direction is added)
46.	OD2.EN.1	4.5.7	OD2 Layout Rules	Modifies the rule (3.3V is added)
47.	OD2.R.1	4.5.7	OD2 Layout Rules	Modifies the rule (OD_33 is added)
48.	OD25_33.W.1	4.5.8	OD25_33 Layout Rules	Adds the rule.
49.	OD25_33.W.2	4.5.8	OD25_33 Layout Rules	Adds the rule.
50.	OD25_33.R.1	4.5.8	OD25_33 Layout Rules	Adds the rule.

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	From Version 1.0 to Version 1.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
51.	OD25_18.W.1	4.5.9	OD25_18 Layout Rules	Adds the rule.
52.	OD25_18.R.1	4.5.9	OD25_18 Layout Rules	Adds the rule.
53.	PO.W.3	4.5.10	PO Layout Rules	Adds the rule.
54.	PO.S.2®	4.5.10	PO Layout Rules	Modifies the recommendation (only LP is considered)
55.	PO.S.4.1	4.5.10	PO Layout Rules	Adds the rule.
56.	PO.S.4.1®	4.5.10	PO Layout Rules	Adds the recommendation.
57.	PO.S.10	4.5.10	PO Layout Rules	Modifies the rule
58.	PO.S.12®	4.5.10	PO Layout Rules	Deletes the recommendation.
59.	PO.S.15	4.5.10	PO Layout Rules	Changes the rule from PO.DN.4
60.	PO.EN.2®	4.5.10	PO Layout Rules	Modifies the recommendation (3.3V is added)
61.	PO.EN.3®	4.5.10	PO Layout Rules	Modifies the recommendation (3.3V is added)
62.	PO.A.1.1	4.5.10	PO Layout Rules	Adds the rule.
63.	PO.A.2	4.5.10	PO Layout Rules	Changes the rule from “0.077” to “0.094”.
64.	PO.R.1	4.5.10	PO Layout Rules	Modifies the rule (including Gate to have jog)
65.	PO.R.5	4.5.10	PO Layout Rules	Modifies the rule
66.	VTH_N.R.2	4.5.11	VTH_N Layout Rules	Change the description from “edge length” to “width”
67.	VTH_P.R.2	4.5.12	VTH_P Layout Rules	Change the description from “edge length” to “width”
68.	VTL_N.R.2	4.5.13	VTL_N Layout Rules	Change the description from “edge length” to “width”
69.	VTL_P.R.2	4.5.14	VTL_P Layout Rules	Change the description from “edge length” to “width”
70.	LDN.EX.3	4.5.18	Layout Rules for LDD Mask Logical Operations	Change the description from “RH” to “{RH OR BJTDMY}”
71.	LDP.EX.2	4.5.18	Layout Rules for LDD Mask Logical Operations	Change the description from “RH” to “{RH OR BJTDMY}”
72.	RES.2®	4.5.20	OD and Poly Resistor Guidelines	RES.2g is changed to RES.2® (Change the length from “0.4” to “0.8”).
73.	RES.5®	4.5.20	OD and Poly Resistor Guidelines	RES.5g is changed to RES.5®.
74.	RES.8®	4.5.20	OD and Poly Resistor Guidelines	RES.8g is changed to RES.8® (Change the space from “0.32” to “0.185”).
75.	RES.9®	4.5.20	OD and Poly Resistor Guidelines	RES.9g is changed to RES.9®. (RH enclosure of unsilicided OD/PO resistor ≥ 0.13)
76.	RES.3g	4.5.20	OD and Poly Resistor Guidelines	Adds the table, Performance and variation of unsilicided OD/PO resistance
77.	RES.4g	4.5.20	OD and Poly Resistor Guidelines	Modifies the guideline (Maximum current density for unsilicided PO: 0.25 mA/μm)
78.	RES.10g	4.5.20	OD and Poly Resistor Guidelines	Adds the guideline
79.	RES.11g	4.5.20	OD and Poly Resistor Guidelines	Adds the guideline
80.	RES.12g	4.5.20	OD and Poly Resistor Guidelines	Adds the guideline
81.	RES.13g	4.5.20	OD and Poly Resistor Guidelines	Adds the guideline
82.	RES.14g	4.5.20	OD and Poly Resistor Guidelines	Adds the guideline
83.	RES.15g	4.5.20	OD and Poly Resistor Guidelines	Adds the guideline
84.	VAR.R.2	4.5.21	MOS Varactor Layout Rules	Change the description from “PSPO” to “mVTL”
85.	CO.W.2	4.5.22	CO Layout Rules	Adds the rule
86.	CO.S.5	4.5.22	CO Layout Rules	Change the rule from “0.11” to “0.09”. 3.3V is included.
87.	CO.EN.1.1	4.5.22	CO Layout Rules	Change the description from “three sides” to “two opposite sides”
88.	CO.EN.1.2	4.5.22	CO Layout Rules	Deletes the rule
89.	CO.R.7g	4.5.22	CO Layout Rules	Deletes the guideline
90.	M1.S.5	4.5.23	M1 Layout Rules	Modifies the rule
91.	M1.EN.0®	4.5.23	M1 Layout Rules	Adds the recommendation
92.	M1.DN.3	4.5.23	M1 Layout Rules	Modifies the rule (with 3 μm x 3 μm open area)
93.	M1.DN.4	4.5.23	M1 Layout Rules	Change checking window from “100 μm x 100 μm” to “200 μm x 200 μm”.
94.	VIAx.W.2	4.5.24	VIAx Layout Rules	Adds the rule
95.	VIAx.EN.0®	4.5.24	VIAx Layout Rules	Adds the recommendation
96.	VIAx.EN.1	4.5.24	VIAx Layout Rules	Modifies the rule (including M1)
97.	VIAx.EN.1®	4.5.24	VIAx Layout Rules	Modifies the recommendation (including M1)
98.	VIAx.EN.2	4.5.24	VIAx Layout Rules	Modifies the rule (including M1)
99.	VIAx.EN.2®	4.5.24	VIAx Layout Rules	Modifies the recommendation (including M1)
100.	VIAx.R.8®	4.5.24	VIAx Layout Rules	VIAx.R.8 is changed to VIAx.R.8®
101.	VIAx.R.10g	4.5.24	VIAx Layout Rules	Deletes the guideline
102.	Mx.S.2.1	4.5.25	Mx Layout Rules	Change W2/L2 from “0.38/0.38” to “0.4/0.4”.
103.	Mx.S.5	4.5.25	Mx Layout Rules	Modifies the rule

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	From Version 1.0 to Version 1.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
104.	Mx.EN.0®	4.5.25	Mx Layout Rules	Adds the recommendation
105.	Mx.DN.3	4.5.25	Mx Layout Rules	Modifies the rule (with 3 µm x 3 µm open area)
106.	Mx.DN.4	4.5.25	Mx Layout Rules	Change checking window from “100 µm x 100 µm” to “200 µm x 200 µm”.
107.	Mx.DN.5	4.5.25	Mx Layout Rules	Modifies the rule (excluding top2 metals at CUP area)
108.		4.5.26	VIAy Layout Rules	Adds the section for layout rules in VIAy Layout Rules
109.		4.5.27	My Layout Rules	Adds the section for layout rules in My Layout Rules
110.	VIAz.W.2	4.5.28	VIAz Layout Rules	Adds the rule
111.	VIAz.EN.1	4.5.28	VIAz Layout Rules	Modifies the rule (including Mx or My)
112.	VIAz.EN.2	4.5.28	VIAz Layout Rules	Modifies the rule (including Mx or My)
113.	VIAz.R.6g	4.5.28	VIAz Layout Rules	Deletes the guideline
114.	Mz.DN.3	4.5.29	Mz Layout Rules	Modifies the rule (with 3 µm x 3 µm open area)
115.	Mz.DN.4	4.5.29	Mz Layout Rules	Change checking window from “100 µm x 100 µm” to “200 µm x 200 µm”.
116.	RV.S.2	4.5.30	RV Layout Rules	Deletes the rule
117.	AP.W.1	4.5.31	Al RDL Layout Rules	Modifies the rule (excluding UBM)
118.	AP.W.2®	4.5.31	Al RDL Layout Rules	Deletes the recommendation
119.		4.5.32	Via Layout Recommendations	Modifies some wordings
120.	SRAM.R.4	4.5.34	SRAM Rules	Modifies the rule
121.	SRAM.R.15	4.5.34	SRAM Rules	Modifies the rule
122.	WLD.R.3.1	4.5.35	SRAM Periphery Rules	Deletes the rule
123.	WLD.R.4	4.5.35	SRAM Periphery Rules	Deletes the rule
124.	WLD.R.7	4.5.35	SRAM Periphery Rules	Modifies the rule (including 186;4)
125.		4.5.37	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Adds the section
126.		4.5.38	CSR Layout Rules	Modifies some wordings
127.		4.5.39	Seal Ring Layout Rules	Modifies some wordings
128.		4.5.40	CDU Layout Rules	Adds the section for layout rules in CDU Layout Rules
129.	A.R.6	4.5.41	Antenna Layout Rules	Change OD2 rule (except 1.8V IO) from “1000” to “5000”.
130.	A.R.9	4.5.41	Antenna Layout Rules	Adds the rule
131.	PO,S.14m	5.4.1	Layout Rules for the WPE	Modifies the rule (including NT_N)
132.	PO.EN.1m	5.4.1	Layout Rules for the WPE	Modifies the rule (including NT_N)
133.	PO.EN.2m	5.4.1	Layout Rules for the WPE	Modifies the rule (including NT_N)
134.	PO.EN.3m	5.4.1	Layout Rules for the WPE	Modifies the rule (including NT_N)
135.	PO.S.5m®	5.4.2	MOS Recommendations	Adds the recommendation
136.	PO.S.6m®	5.4.2	MOS Recommendations	Adds the recommendation
137.	PO.EX.2m®	5.4.2	MOS Recommendations	Adds the recommendation
138.	BJT.R.1	5.4.3	BJT Rules and Recommendations	Modifies the rule (adding F=0.6µm)
139.	BJT.R.7®	5.4.3	BJT Rules and Recommendations	Modifies the recommendation (excluding RH)
140.	BJT.R.8	5.4.3	BJT Rules and Recommendations	Adds the rule
141.	RES.2m	5.4.4	Resistor Rules	Changes the length rule from “0.8” to “0.4”.
142.	A.N.R.19mg	5.5.3	Electrical Performance Rules and Guidelines	Deletes the guideline
143.	A.N.R.25mg	5.5.4	Noise Rules	Modifies the guideline (adding NT_N width>1 µm)
144.	DOD.S.2	6.1	DOD Rules	Changes the rule from “0.6” to “0.34”.
145.	DOD.S.3	6.1	DOD Rules	Changes the rule from “0.6” to “0.3”.
146.	DOD.S.5	6.1	DOD Rules	Changes the rule from “0.6” to “0.3”.
147.	DOD.S.7.0	6.1	DOD Rules	Adds the rule
148.	DOD.S.7.1		DOD Rules	Adds the rule
149.	DOD.EN.1	6.1	DOD Rules	Changes the rule from “0.6” to “0.3”.
150.	OD.DN.3	6.1	DOD Rules	Modifies the rule
151.	DPO.S.6.0	6.2	DPO Rules	Adds the rule
152.	DPO.S.6.1	6.2	DPO Rules	Adds the rule
153.	DMx.S.5.0	6.3	DMx Rules	Adds the rule
154.	DMx.S.5.1	6.3	DMx Rules	Adds the rule
155.	Mx.DN.3	6.3	DMx Rules	Modifies the rule
156.	DMx.R.3	6.3	DMx Rules	Modifies the rule (45 degree shape is allowed)
157.		7	Design for Manufacturing	Modifies some wordings.
158.		8.2	ESD Protection Circuit Design and Layout Guidelines	Adds the 3.3V ESD Protection Circuit Design and Layout Guidelines

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	From Version 1.0 to Version 1.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
159.	ESD.38g	8.2	ESD Protection Circuit Design and Layout Guidelines	Deletes the guideline
160.	ESD.45g	8.2	ESD Protection Circuit Design and Layout Guidelines	Modifies the guideline
161.		8.2.6	Tips for the Power Bus	Modifies the approach
162.		9.2	Front-End Process Reliability Rules and Models	Adds the section for layout rules in Front-End Process Reliability Rules and Models
163.		9.3	Back-End Process Reliability Rules	Modifies the section for layout rules in Back-End Process Reliability Rules
164.		10	Electrical Parameters Summary	Adds the chapter

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12/16/2016
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A.1.5 From Version 1.1 to Version 1.2

	From Version 1.1 to Version 1.2			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1	VIAz.W.2	4.5.28	VIAz Layout Rules	Corrects the rule from “0.34” to “0.36”
2	Mz.DN.4	4.5.29	Mz Layout Rules	Corrects the stepping from “100µm” to “200µm”.
3	SRAM.R.15	4.5.34	SRAM Rules	Corrects the description from “SRAM cell or SRAM decoder ” to “SRAM cell”.
4	CSR.W.3	4.5.38	CSR Layout Rules	Corrects the description from “L-mark” to “L-slot”.
5	CSR.EN.7	4.5.38	CSR Layout Rules	Corrects the description from “L-mark” to “L-slot”.
6	CSR.EN.8	4.5.38	CSR Layout Rules	Corrects the description from “L-mark” to “L-slot”.
7	BJT.R.7®	5.4.3	BJT Rules and Recommendations	Corrects the description from “VTLN” to “VTL_N”.
8	DOD.S.8	6.1	Dummy OD Rules	Corrects the rule from “0.3” to “0.6”.
9	DOD.EN.1	6.1	Dummy OD Rules	Corrects the rule from “0.6” to “0.3”.
10	Mx.DN.3	6.3	Dummy Metal Rules	Corrects the Mz/UTM rule from “20% in 50x50” to “20% in 25x25 (with 3 µm x 3 µm open area)”.

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A.1.6 From Version 1.2 to Version 1.3

	From Version 1.2 to Version 1.3			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.		Title		Add (G/G+/LP/LPG) in the title
2.		1.1	Overview	Adds CLN65LPG technology
3.		1.2	Reference Documentation	Modifies Table 1.2.1
4.		1.3	Guidelines for Half Node Technologies (CLN55 only)	Adds the description, “CLN65G+ can be shrunk to CLN55”
5.		2.1.1	Front-End Features	1. Add LPG information 2. Modifies SRAM informations
6.		2.1.2	Back-End Features	Adds Mr for top-layer metal.
7.		2.2	Devices	Add LPG information in Table 2.2.1
8.		2.3	Power Supply and Operation Temperature Ranges	Add LPG information in Table 2.3.1
9.		2.4	Cross–section	Add Fig. 2.4.4,
10.		2.5	Metallization Options	Add Mr/VIAr information
11.		3.1	Mask Information, Key Process Sequence, and CAD Layers	1. Modifies Table 3.1.1 to Table 3.1.7, and Table 3.1.9. 2. Add Table 3.1.8 for the LPG.
12.		3.2	Metal/Via CAD Layer Information for Metallization Options	Adds Mr/VIAr information
13.		3.3	Dummy Pattern Fill CAD Layers	Adds data type 81 for DMr
14.		3.4	Special Recognition CAD Layer Summary	1. Adds special layers, MOMDMY_1, MOMDMY_2, MOMDMY_3, MOMDMY_4, MOMDMY_5, MOMDMY_6, MOMDMY_7, MOMDMY_8, MOMDMY_9, MOMDMY_AP, RTMOMDMY, FUSELINK, 2. Modify special layers, SRM, SRMDMY_0, SRAMDMY_4, SRMDMY_0, CO_11,
15.		3.5.4	LP-based Triple Gate Oxide (LPG) Design	Add the section
16.		3.6	Mask Requirements for Device options (High/STD/Low VT)	Modify the G+/LP information and add LPG infromation
17.		3.7	Design Geometry Rules	Nodify the G.4 for OPC layer
18.	G.6g^{U}	3.7	Design Geometry Rules	Add G.6g^{U}
19.		3.7.2	OPC Recommendations and Guidelines	Add the description, ”Using the commercial LPC tools or tsmc DFM LPC service, to identify the potential patterening marginalities (such as pinch or bridge) with process window, and then modify the layout.”
20.		4.3	Definition of Layout Geometrical Terminology	Add the vertex
21.		4.4	Minimum Pitches	Add Mr/VIAr information
22.	DNW.S.6	4.5.1	DNW Rules	Remove the rule
23.	DNW.EN.2	4.5.1	DNW Rules	Remove the rule
24.	DNW.EN.3	4.5.1	DNW Rules	Change the rule number from DNW.S.7 to DNW.EN.3
25.	DNW.R.6g^{U}	4.5.1	DNW Rules	Add the guideline
26.	OD.W.1®	4.5.2	OD Rules	Remove the rule
27.	OD.W.4	4.5.2	OD Rules	1. Change the rule vaule from 0.4 to 0.18 2. Add the description, “Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.6g^{U}, in section 3.7)”
28.	OD.S.4	4.5.2	OD Rules	Change the rule vaule from 0.4 to 0.18
29.	OD.L.2	4.5.2	OD Rules	Change the wording from “[OD width is ≤ 0.15 μm]” “[OD width is < 0.15 μm]”
30.	OD.L.3	4.5.2	OD Rules	Remove the rule
31.	NW.A.1	4.5.3	NW Rules	Change the rule vaule from 1.2 to 0.64
32.	NW.A.2	4.5.3	NW Rules	Change the rule vaule from 1.2 to 0.64
33.	NW.A.3	4.5.3	NW Rules	Add the rule
34.	NW.A.4	4.5.3	NW Rules	Add the rule
35.	NW.R.1g^{U}	4.5.3	NW Rules	Modify the the description from “unintentional floating well” to “floating well unless necessary”
36.	NT_N.EN.1	4.5.6	NT_N Rules	Remove the wording, “If the layout will be shrunk 10%, it should be plotted = 0.285.”
37.	NT_N.A.1	4.5.6	NT_N Rules	Change the rule vaule from 1.2 to 0.64

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	From Version 1.2 to Version 1.3			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
38.	NT_N.A.2	4.5.6	NT_N Rules	Change the rule vaule from 1.2 to 0.64
39.	NT_N.A.3	4.5.6	NT_N Rules	Add the rule
40.	NT_N.A.4	4.5.6	NT_N Rules	Add the rule
41.	NT_N.R.2	4.5.6	NT_N Rules	Change the rule wording from “P+OD” to “P+ Gate”
42.	OD2.W.2	4.5.7	OD2 Rules	Add the rule
43.	OD2.S.2	4.5.7	OD2 Rules	Add the “Gate” in the rule
44.	OD2.S.5	4.5.7	OD2 Rules	Add the rule
45.	OD2.S.6	4.5.7	OD2 Rules	Add the rule
46.	OD2.S.7	4.5.7	OD2 Rules	Add the rule
47.		4.5.8	DCO Rules	Add the section
48.		4.5.9	OD25_33 Rules	Add G/G+
49.	PO.W.3	4.5.11	PO Rules	Add the description, “(for 2.5V overdrive to 3.3V, please refer to section 4.5.9)”
50.	PO.W.4	4.5.11	PO Rules	Add the description, “(for 2.5V underdrive to 1.8V, please refer to section 4.5.10)”
51.	PO.W.5	4.5.11	PO Rules	Add the rule
52.	PO.S.1.1®	4.5.11	PO Rules	Remove the recommendation
53.	PO.S.5®	4.5.11	PO Rules	Change from J<0.2 to J<0.1
54.	PO.S.6®	4.5.11	PO Rules	Remove the recommendation
55.	PO.S.10	4.5.11	PO Rules	Add the wording” (except for small jog with edge length < 0.06 (R))”
56.	PO.S.11®	4.5.11	PO Rules	Add the condition, [channel length ≤ 0.08um]
57.	PO.S.16	4.5.11	PO Rules	Add the rule
58.	PO.S.14®	4.5.11	PO Rules	Add the description, “, to reduce the impact by well proximity effect.”
59.	PO.EN.1®	4.5.11	PO Rules	Add the description, “, to reduce the impact by well proximity effect.”
60.	PO.EN.2®	4.5.11	PO Rules	Add the description, “, to reduce the impact by well proximity effect.”
61.	PO.EN.3®	4.5.11	PO Rules	Add the description, “, to reduce the impact by well proximity effect.”
62.	PO.EX.2®	4.5.11	PO Rules	Add the description, “especially for channel width>1μm.”
63.	PO.EX.4®	4.5.11	PO Rules	Remove the recommendation
64.	PO.EX.5®	4.5.11	PO Rules	Remove the recommendation
65.	PO.L.1			Modify the decription from “Maximum PO length between two contacts, as well as between one contact and PO line end, when the PO width is < 0.13 μm.” to “Maximum PO length between two contacts without gate, as well as the length from any point inside PO gate to nearest CO, when the PO width is < 0.13 μm.”
66.	PO.R.4	4.5.11	PO Rules	Add the description, “except RTMOM region (RTMOMDMY, CAD, 155;21).”
67.	PO.R.5	4.5.11	PO Rules	Remove the rule
68.	PO.R.7g^{U}	4.5.11	PO Rules	Add the guideline
69.	mVTL.R.1	4.5.16	mVTL Rules	Add VTL_N, VTL_P in the rule description
70.	LDN.EX.2	4.5.19	LDD Rules	Add DCO in the rule description
71.	LDN.O.1	4.5.19	LDD Rules	Add DCO in the rule description
72.	LDP.EX.1	4.5.19	LDD Rules	Add DCO in the rule description
73.	LDP.O.2	4.5.19	LDD Rules	Add DCO in the rule description
74.	VT.S.1	4.5.19	LDD Rules	Add DCO in the rule description
75.	VT.EX.2	4.5.19	LDD Rules	Add DCO in the rule description
76.		4.5.21	OD and Poly Resistor Recommendations and Guidelines	Update the resistance examples in T-N65-CL-SP-009 from V1.0 to V1.2.
77.	VAR.W.1	4.5.22	VAR Rules	Add the description, “for the baseband circuit, according to the SPICE model”
78.	VAR.W.2	4.5.22	VAR Rules	Add the rule
79.	VAR.W.3	4.5.22	VAR Rules	Add the rule
80.	VAR.W.4	4.5.22	VAR Rules	Add the rule
81.	VAR.S.2®	4.5.22	VAR Rules	Remove the recommendation
82.	VAR.S.3®	4.5.22	VAR Rules	Remove the recommendation
83.	VAR.A.1®	4.5.22	VAR Rules	Add the decription, “for baseband circuit”
84.	CO.S.3®	4.5.23	CO Rules	Add the recommendation
85.	CO.EN.1®	4.5.23	CO Rules	Change the recommendation vaule from 0.06 to 0.04
86.	CO.R.5g^{U}	4.5.23	CO Rules	Add the description, “ 1. Recommended to use double CO or more on the resistor connection. 2. Double CO on Poly gate to reduce the probability of high Rc 3.Recommend putting multiple and symmetrical source/drain CO for SPICE simulation accuracy. 4.For large transistor, limit the number of source/drain CO: have the number of CO necessary for the current, and then spread them all over the Source/Drain area. If possible, also increase the CO to gate spacing (to reduce the short possibility by particle)”
87.	CO.R.6g^{U}	4.5.23	CO Rules	Merge the guideline to CO.R.5g^{U}
88.	M1.W.2	4.5.24	M1 Rules	1. Change the rule vaule from 0.4 to 0.19 2. Add the description, “Please make sure the vertex of 45 degree

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	From Version 1.2 to Version 1.3			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
				pattern is on 5nm grid (refer to the guideline, G.6g^{U}, in section 3.7)"
89.	M1.S.4	4.5.24	M1 Rules	Add the decription. "Note: When M1 width > 9um is used, please take care of the M1.DN.2 rule by using larger space.For example, if two M1 with width 12um and space 1.5um, it will get 92.5% density violation on M1.DN.2; either enlarger the M1 space (like 2um) or reduce the M1 width (like 9um) to meet M1.DN.2."
90.	M1.S.5	4.5.24	M1 Rules	Add the wording "(except for small jog with edge length < 0.09um (R))"
91.	M1.S.6	4.5.24	M1 Rules	Change the rule vaule from 0.4 to 0.19
92.	M1.S.7®	4.5.24	M1 Rules	Add the decription. "e.g. enlarge the metal width ≥ 0.35 for the guard ring design."
93.	M1.L.1	4.5.24	M1 Rules	Remove the rule
94.	M1.DN.4	4.5.24	M1 Rules	Add the decription. "Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient)"
95.	VIAx.EN.0	4.5.25	VIAx Rules	Add the rule.
96.	VIAx.EN.1®	4.5.25	VIAx Rules	Add the decription. "Please refer to the "Via Layout Recommendations" section in Chapter 4.5.34"
97.	VIAx.EN.2®	4.5.25	VIAx Rules	Add the decription. "Please refer to the "Via Layout Recommendations" section in Chapter 4.5.34"
98.	VIAx.EN.3	4.5.25	VIAx Rules	Add the rule
99.	VIAx.R.11	4.5.25	VIAx Rules	Add the rule
100.	Mx.W.2	4.5.26	Mx Rules	1. Change the rule vaule from 0.4 to 0.19 2. Add the description, "Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.6g^{U}, in section 3.7)"
101.	Mx.S.4	4.5.26	Mx Rules	Add the decription. "Note: When Mx width > 9um is used, please take care of the Mx.DN.2 rule by using larger space. For example, if two Mx with width 12um and space 1.5um, it will get 92.5% density violation on Mx.DN.2; either enlarger the Mx space (like 2um) or reduce the Mx width (like 9um) to meet Mx.DN.2."
102.	Mx.S.5	4.5.26	Mx Rules	Add the wording "(except for small jog with edge length < 0.1um (R))"
103.	Mx.S.6	4.5.26	Mx Rules	Change the rule vaule from 0.4 to 0.19
104.	Mx.S.7®	4.5.26	Mx Rules	Add the decription. "e.g. enlarge the metal width ≥ 0.35 for the guard ring design."
105.	Mx.EN.0	4.5.26	Mx Rules	Add the rule
106.	Mx.EN.1®	4.5.26	Mx Rules	Add the decription. "Please refer to the "Via Layout Recommendations" section in Chapter 4.5.34"
107.	Mx.EN.2®	4.5.26	Mx Rules	Add the decription. "Please refer to the "Via Layout Recommendations" section in Chapter 4.5.34"
108.	Mx.EN.3	4.5.26	Mx Rules	Add the rule
109.	Mx.L.1	4.5.26	Mx Rules	Remove the rule
110.	Mx.DN.4	4.5.26	Mx Rules	Add the decription. "Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient)"
111.	Mx.R.2g^{U}	4.5.26	Mx Rules	Change the description, from "Recommended to enlarge the metal space" to "For the small metal space, recommended to enlarge the metal space"
112.	VIAy.EN.1®	4.5.27	VIAy Rules	Add the decription. "Please refer to the "Via Layout Recommendations" section in Chapter 4.5.34"
113.	VIAy.EN.2®	4.5.27	VIAy Rules	Add the decription. "Please refer to the "Via Layout Recommendations" section in Chapter 4.5.34"
114.	My.W.2	4.5.28	My Rules	1. Change the rule vaule from 0.4 to 0.39 2. Add the description, "Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.6g^{U}, in section 3.7)"
115.	My.S.2	4.5.28	My Rules	Change "≥0.39" and "≥1.0" to ">0.39" and ">1.0"
116.	My.S.4	4.5.28	My Rules	Add the decription. "Note: When My width > 9um is used, please take care of the My.DN.2 rule by using larger space. For example, if two My with width 12um and space 1.5um, it will get 92.5% density violation on My.DN.2; either enlarger the My space (like 2um) or reduce the My width (like 9um) to meet My.DN.2."
117.	My.S.5	4.5.28	My Rules	Change the rule vaule from 0.4 to 0.39
118.	My.S.6®	4.5.28	My Rules	Add the decription. "e.g. enlarge the metal width ≥ 0.35 for the guard ring design."
119.	My.EN.1®	4.5.28	My Rules	Add the decription. "Please refer to the "Via Layout Recommendations" section in Chapter 4.5.34"
120.	My.EN.2®	4.5.28	My Rules	Add the decription. "Please refer to the "Via Layout Recommendations" section in Chapter 4.5.34"
121.	My.L.1	4.5.28	My Rules	Remove the rule

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	From Version 1.2 to Version 1.3			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
122.	My.DN.4	4.5.28	My Rules	Add the decription. “Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient)”
123.	My.R.2g^{U}	4.5.28	My Rules	Change “Recommended to enlarge the metal space, by using Wire Spreading function of EDA tool, to reduce the wire capacitance and the possibility of metal short” to “For the small space, recommended to enlarge the metal space, by using Wire Spreading function of EDA tool, to reduce the wire capacitance”
124.	My.R.8®	4.5.28	My Rules	Remove the recommendation
125.	Mz.S.3	4.5.30	Mz Rules	Add the decription. “Note: When Mz width > 9um is used, please take care of the Mz.DN.2 rule by using larger space. For example, if two Mz with width 12um and space 1.5um, it will get 92.5% density violation on Mz.DN.2; either enlarger the Mz space (like 2um) or reduce the Mz width (like 9um) to meet Mz.DN.2.”
126.	Mz.DN.4	4.5.30	Mz Rules	Add the decription. “Anticipate metal density gradient from layout of small cell by targeting density ~40% (this way, it will limit the risk of low density and of high gradient)”
127.		4.5.31	VIAr Rules	Add the section
128.		4.5.32	Mr Rules	Add the section
129.			RV Rules	Move it to T-000-CL-DR-002
130.			AP Rules	Move it to T-000-CL-DR-002
131.		4.5.33	MOM Rules	Add the section
132.	LOGO.O.1	4.5.35	LOGO Rules	Remove the AP in the rule
133.	LOGO.R.2	4.5.35	LOGO Rules	Remove PO.EX.1® in the rule
134.	SRAM.R.4^{U}	4.5.36	SRAM Rules	1. Add 0.525 mm²/ 0.62 mm²/ 0.974 mm²/8T 1.158 mm²/10T 1.158 mm² for G/G+. 2. Add 0.974 mm²/8T 1.158 mm²/10T 1.158 mm² for LP. 1. Add LPG SRAM cell
135.	SRAM.R.7^{U}	4.5.36	SRAM Rules	Remove the description, “(0.499 µm² and 0.525 µm²)”
136.	SRAM.R.15	4.5.36	SRAM Rules	Add item 4. CO_11 must be fully covered by SRM (50;0) and SRAMDMY_0 (186;0)
137.	SRAM.R.16^{U}	4.5.36	SRAM Rules	Remove the rule
138.		4.5.37	SRAM Periphery (Word Line Decoder) Rules	Modify the description, “186;4 is used for LP process and 186;5 is used for G process.“ to “186;4 is used for 0.499µm² cell and 186;5 is used for 0.525 µm², 0.62 µm², 0.974µm², 1.158µm² cell”
139.		4.5.39	Fuse Rules	Add the section
140.		4.5.40	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Add Mr information
141.		4.5.40.1	Metallization Options	Add Mr information
142.		4.5.40.1.3	Metallization Options Using Mr as the Top Metal	Add the section
143.	CSR.S.5	4.5.41	Chip Corner Stress Relief Pattern (CSR)	Add the rule
144.	CSR.EN.9	4.5.41	Chip Corner Stress Relief Pattern (CSR)	Add the rule
145.	CSR.R.3	4.5.41	Chip Corner Stress Relief Pattern (CSR)	Add VIAr in the rule and change the “≥” to “=”
146.	CSR.W.1	4.5.41	Chip Corner Stress Relief Pattern (CSR)	Remove the “minimum”
147.	CSR.W.3	4.5.41	Chip Corner Stress Relief Pattern (CSR)	Add VIAr in the rule
148.	CSR.EN.7	4.5.41	Chip Corner Stress Relief Pattern (CSR)	Add VIAr in the rule
149.	VIAr.W.2	4.5.42	Seal Ring Rules	Add the rule
150.		4.5.44	Antenna Rules	Add item 12:Failure Criterion
151.		5.2	Layout Rules for the WPE (Well Proximity Effect)	Add item 4, “If the distance between gate and well is the same, the WPE impact from the poly end cap direction is smaller than that from the source/drain direction.”
152.	AN.R.34mg^{U}	5.4.1	General Guidelines	Add the guideline
153.	AN.R.35mg^{U}	5.4.1	General Guidelines	Add the guideline
154.	AN.R.36mg^{U}	5.4.1	General Guidelines	Add the guideline
155.	PO.EX.2mg^{U}	5.4.2	5.4.2 MOS Recommendations	Change PO.EX.2m® to PO.EX.2mg^{U}
156.	AN.R.37mg^{U}	5.4.5	Capacitor Guidelines	Add the guideline
157.	AN.R.38mg^{U}	5.4.5	Capacitor Guidelines	Add the guideline
158.	AN.R.39m^{U}	5.5.2	Matching Rules and Guidelines	Add the rule
159.	AN.R.10mg^{U}	5.5.2	Matching Rules and	Change the decription, “Pay attention on the associated routing

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	From Version 1.2 to Version 1.3			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
			Guidelines	layout, of the matching pair. " to “Pay attention on the associated routing layout, as well as the associated pattern density, of the matching pair, to minimize the Rs difference.”
160.	AN.R.12mg^{U}	5.5.2	Matching Rules and Guidelines	Add “current mirror” in the decription.
161.	AN.R.40.mg^{U}	5.5.2	Matching Rules and Guidelines	Add the guideline
162.	AN.R.15mg^{U}	5.5.3	Electrical Performance Rules and Guidelines	Change the decription, from “Maximum” to “optimize”
163.	AN.R.16mg^{U}	5.5.3	Electrical Performance Rules and Guidelines	Add “unsilicided” in the descrition.
164.	AN.R.41.mg^{U}	5.5.3	Electrical Performance Rules and Guidelines	Add the guideline
165.		5.6	Burn-in Guidelines for Analog Circuits	Add the section
166.	DOD.EN.1	6.1	DOD Rules	Add the description, “(fully outside is allowed)”
167.		6.3	DMx Rules	Add dummy Mr related rules
168.	DMx.S.8	6.3	DMx Rules	Change the rule value from 18 to 2.5
169.	Mx.DN.3	6.3	DMx Rules	Add the description, “if there is 3 μm x 3 μm open area inside the region <15%/20%.”
170.		7.1.1	Layout Tips for Minimizing Critical Areas	Add the item 1: Enlarge the width of the wire
171.		7.2.4	Grouping Table of DFM Action-Required Rules, Recommendations and Guidelines	Add the section
172.		7.4	DFM Service	Add the section
173.		7.5	MFU Optimization kit	Add the section
174.		8.1	Layout Guidelines for Latch-Up Prevention	Change the rule vaule from 15 to 10.
175.	ESD.35g^{U}	8.2.4	ESD Guidelines	1. Change the guidleine vaule from 10 to 15 2. Add the description, “(wire bond and flip chip)”
176.		9.2.2.3	Test Methodology	Add LPG information
177.		9.2.3.3.3	Dimension Ranges of Stress Devices	0.18 μm ~ 0.315 μm for 1.8V I/O N/PMOS devices in channel length
178.		9.2.3.3.5	DC Lifetime and Vmax	Add G/G+ information
179.		9.2.4.4.4	DC Lifetime and Vmax	Add G/G+ information
180.		9.3.3	Cu Metal Current Density (EM) Specifications	Add Mr/VIAr information
181.		9.3.5	Cu Metal AC Operation	Add Mr information
182.		9.3.6	AlCu RDL AC Operation	Add the description, “The I_{peak} rule for AP RDL is 58 mA/um”
183.		9.3.6	Poly Current Density Guidelines	Add the description, “For silicided poly, the maximum DC current density should be less than 6mA/um to avoid silicided poly melting or burn out.”
184.		9.3.7		1. Change the EM spec for unsilicide PO from 0.25 mA/μm to 0.5 mA/μm. 2. Add the wording for the EM of silicided poly, “For silicided poly, the maximum DC current density is 6mA/um at a junction temperature of 110°C. This density is calculated using 0.1% point of measurement data at a 5% resistance increase after 100K hours of continuous operation.”
185.		9.4	Product Early Failure Rate Screening Guidelines	Add the section
186.		9.5	e-Reliability Model System Introduction	Add the section
187.		10	Electrical Parameters Summary	1. Update the electrical parameters summary based on T-000-CL-SP-009 from V1.2. 2. Update the electrical parameters summary based on T-000-CL-SP-031 to V1.1. 3. Update the electrical parameters summary based on T-000-CL-SP-040 to V1.1. 4. Update the electrical parameters summary based on T-000-CL-SP-041 to V1.1.

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A.1.7 From Version 1.3 to Version 1.4

	From Version 1.3 to Version 1.4			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.				Merge T-N65-CM-DR-001(MS_RF rule, V1.0), T-000-CL-DR-001(PAD rule, V1.4), and T-N55-CL-DR-001(N55 rule, V1.0) into T-N65-CL-DR-001(Logic rule, V1.4)
2.		Title		Add ULP in CLN65, CLN55: GP, CMN65: GP/LP, in the title
3.		1.1	Overview	Add ULP in CLN65, CLN55: GP, CMN65: GP/LP
4.		1.2	Reference Documentation	Modifies Table 1.2.1
5.		1.3	Guidelines for Half Node Technologies (CLN55 only)	removed
6.		2.1.1	Front-End Features	1. Add the description “subtrate resistivity of 8-12 Ω-cm)” 2. Add ULP in CLN65, CLN55: GP, CMN65: GP/LP 3. Remove 1.2/1.8 in CLN65LP 4. Update SRAM information 5. Add NW resistor information
7.		2.1.2	Back-End Features	1. Add infromnation of CLN55, CMN65 metal 2. Add infromnation of MOM, MiM, Industor 3. Add the descripton, “TSMC N55 generation does not support MIM capacitor and inductor devices.”
8.		2.2	Devices	1. Add information of MOM, MiM, Industor 2. Add CLN55, CMN65
9.		2.3	Power Supply and Operation Temperature Ranges	1. Add CLN55, CMN65 2. Remove 1.2/1.8 in CLN65LP 3. Add 2.5V overdrive to 3.3V 4. Add 2.5V underdrive to 1.8V
10.		2.4	Cross section	Add Cross section for CMN65
11.		2.5	Metallization Options	1. Add infromnation of CLN55, CMN65 metal/ Via 2. Add table 2.5.5-7 3. Add Mr in table 2.5.8
12.		3.1	Mask Information, Key Process Sequence, and CAD Layers	1. Add item 6, “In the tabe of section 3.1, “ * “ means optional mask. “ # “ means non-design level mask which is no need to draw (or design) this layer. This non-design level mask is generated by logical operation from other drawn layers.” 2. Remove table for CLN65LP 1.8V 3. Add the table 3.1.8-12 4. Add thecolumn, Non-design level mask, in table 3.1.13
13.		3.2	Metal/Via CAD Layer Information for Metallization Options	Add thecolumn, u, in table 3.2.1
14.		3.3	Dummy Pattern Fill CAD Layers	Add thecolumn, u, in table 3.3.1
15.		3.4	Special Recognition CAD Layer Summary	1. Modify Ncap_NTN, SEALRING, SRAMDMY_0 2. Add SRAMDMY_1, LUPWDMY, TCDDMY, RruleGuildeline, excludeRRuleRequire, excludeRRuleRecommended, excludeRRuleAnalog, excludeRRuleGuideline. 3. Copy Ms_RF related layers from T-N65-CM-DR-001 4. Copy WBDMY from T-000-CL-DR-002. 5. Remove ESD1DMY and ESD2DMY.
16.		3.5	Device Truth Tables	1. Add more diode information in table 3.5.2-5 2. Add CLN65LPG 3. Add CLN65ULP 4. Add CLN55GP 5. Add CMN65 MiM/Inductor
17.		3.6	Mask Requirements for Device Options (High/STD/Low VT)	1. Add CLN55, CMN65 2. Remove 1.2/1.8 in CLN65LP
18.	OPC.R.1®	3.7.2	OPC Recommendations and Guidelines	Modify it from 0.5 to 0.27.
19.	OPC.R.2g	3.7.2	OPC Recommendations and Guidelines	Change it to DRC checkable
20.		4.2.2	Special Definition	Add information of CUP
21.		4.4	Minimum Pitches	Add pitch information of Mu/ CBM/ CTM/ VIAr/ VIAu ≥ 3 neighboring
22.		4.5	CLN65(Logic) Layout Rules and Guidelines	Modify the title to add CLN65(Logic)

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	From Version 1.3 to Version 1.4			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
23.	DNW.R.6g	4.5.1.	DNW Rules	1. change it to DRC checkable 2. Add the description, DRC can flag RW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.
24.	NW.R.1g	4.5.3	NW Rules	1. Change it to DRC checkable 2. Add the description, DRC can flag both NW is not with CO in NPOD and PW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.
25.	NWROD.R.2g^{U}	4.5.4	NWROD Rules	Removed
26.	NWROD.R.3g	4.5.4	NWROD Rules	1. Change it to DRC checkable 2. Add the description, DRC can flag {NWDMY AND NW} is not a rectangle.
27.	NWRSTI.R.2g^{U}	4.5.5	NWRSTI Rules	Removed
28.	NWRSTI.R.3g	4.5.5	NWRSTI Rules	1. Change it to DRC checkable 2. Add the description, DRC can flag {NWDMY AND NW} is not a rectangle.
29.	NT_N.W.2	4.5.6	NT_N Rules	Change it from “1.0 native device” to “core native device [G/GP/G in LPG process]”
30.	NT_N.W.2.1	4.5.6	NT_N Rules	Change it from “1.2 native device [LP process] ” to “core native device [LP/ULP/LP in LPG process]”
31.	NT_N.W.2.2	4.5.6	NT_N Rules	Change it from “1.2 native device [LP process with limited E and M (E<=1um, M<=0.5um)]” to “core native device [LP/ULP/LP in LPG process with limited E and M (E<=1um, M<=0.5um)]”
32.	NT_N.R.3	4.5.6	NT_N Rules	Add the description” You have to draw a NCap_NTN layer to cover the NMOS capacitors. The NCap_NTN enclosure of OD have to be ≥ 0um. DRC also flags NCap_NTN and OD outside of the NCap_NTN in the same NT_N.”
33.		4.5.9	OD25_33 Rules	Add N65 LPG/ ULP process, and N55 GP process.
34.	OD25_33.W.1	4.5.9	OD25_33 Rules	Add the description, “except gate without PO CO in RFDMY”
35.	OD25_33.W.2	4.5.9	OD25_33 Rules	Add the description, “except gate without PO CO in RFDMY”
36.		4.5.10	OD25_18 Rules	N65G/ GP/ LPG/ ULP process, not in N55 GP process.
37.	PO.W.3	4.5.11	PO Rules	Add the description, “except gate without PO CO in RFDMY”
38.	PO.EN.1®	4.5.11	PO Rules	Separate it to {(NW NOT OD2) NOT NT_N} for 3.3V IO process and (NW NOT NT_N) for1.8V or 2.5V IO process
39.	PO.EN.3®	4.5.11	PO Rules	Separate it to 3.3V PMOS gate enclosure by {(NW AND OD2) NOT NT_N} and 1.8V or 2.5V PMOS gate enclosure by (NW NOT NT_N)
40.	PO.DN.3	4.5.11	PO Rules	Add “except TCDDMY”
41.	PO.R.8	4.5.11	PO Rules	Add this rule
42.	PO.FU.R.8	4.5.11	PO Rules	Add this rule
43.		4.5.16	MVTL Rules	mVTL is only used for core LP/ULP devices (LP, ULP). It is not allowed in core G/GP/LPG devices or I/O devices (1.8V, 2.5V, and 3.3V).
44.	RES.1® RES.3® RES.4® RES.6® RES.7® RES.14®	4.5.21	OD and Poly Resistor Recommendations and Guidelines	Removed
45.	RES.5®	4.5.21	OD and Poly Resistor Recommendations and Guidelines	Move it to RES.5m®
46.	CO.S.6g	4.5.23	CO Rules	1. Change it to DRC checkable 2. Add the description, DRC can flag if the STRAP is butted on source, one of STRAP and source is without CO.
47.	CO.R.5g	4.5.23	CO Rules	1. Modify item 4 to, If it is hard to increase the CO to gate spacing (CO.S.3®) for the large transitor, limit the number of source/drain CO: to have the necessary CO number for the current, and then distribute the CO evenly on the Source/Drain area. If possible, also increase the CO to gate spacing (to reduce the short possibility by particle) 2. Change it to DRC checkable 3. Add the description, DRC can flag single CO.
48.	M1.DN.1	4.5.24	M1 Rules	Modify it from 15% in 50x50, 70% in100x100 to 10% in 75x75, 80% in100x100
49.	M1.DN.3	4.5.24	M1 Rules	Removed
50.	M1.DN.3®	4.5.24	M1 Rules	Removed
51.	M1.DN.4	4.5.24	M1 Rules	Modify it from 200umx200um to 250umx250um.
52.	VIAx.R.9g	4.5.25	VIAx Rules	1. Change it to DRC checkable 2. Add the description, DRC can flag single via.
53.	Mx.W.4®	4.5.26	Mx Rules	Removed

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	From Version 1.3 to Version 1.4			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
54.	Mx.DN.1	4.5.26	Mx Rules	Modify it from 15% in 50x50, 70% in100x100 to 10% in 75x75, 80% in100x100
55.	Mx.DN.3	4.5.26	Mx Rules	Removed
56.	Mx.DN.3®	4.5.26	Mx Rules	Removed
57.	Mx.DN.4	4.5.26	Mx Rules	Modify it from 200umx200um to 250umx250um.
58.	Mx.DN.5	4.5.26	Mx Rules	Modify it from 70% to 80%
59.	VIAy.R.8®	4.5.27	VIAy Rules	Removed
60.	VIAy.R.9g	4.5.27	VIAy Rules	1. Change it to DRC checkable 2. Add the description, DRC can flag single via.
61.	My.W.4®	4.5.28	My Rules	Removed
62.	My.DN.1	4.5.28	My Rules	Modify it from 15% in 50x50, 70% in100x100 to 10% in 75x75, 80% in100x100
63.	My.DN.3	4.5.28	My Rules	Removed
64.	My.DN.4	4.5.28	My Rules	Modify it from 200umx200um to 250umx250um.
65.	VIAz.R.5g	4.5.29	VIAz Rules	1. Change it to DRC checkable 2. Add the description, DRC can flag single via.
66.	Mz.W.3®	4.5.30	Mz Rules	Removed
67.	Mz.DN.1	4.5.30	Mz Rules	Modify it from 20% in 50x50 to 10% in 75x75,
68.	Mz.DN.3	4.5.30	Mz Rules	Removed
69.	Mz.DN.4	4.5.30	Mz Rules	Modify it from 200umx200um to 250umx250um.
70.	VIAr.R.5g	4.5.31	VIAr Rules	1. Change it to DRC checkable 2. Add the description, DRC can flag single via.
71.	Mr.W.3®	4.5.32	Mr Rules	Removed
72.	Mr.DN.1	4.5.32	Mr Rules	Modify it from 20% in 50x50 to 10% in 75x75,
73.	Mr.DN.3	4.5.32	Mr Rules	Removed
74.	Mr.DN.4	4.5.32	Mr Rules	Modify it from 200umx200um to 250umx250um.
75.		4.5.33	MOM Rules	MOM can be used for N55.
76.		4.5.33.1	RTMOM (Rotated Metal Oxide Metal) Capacitor Guidelines	TSMC RTMOM PDK cell meets all required OD/Poly density rules. If your design your own RTMOM cell, you have to take care the OD/Poly density rules carefully.
77.	LOGO.S.1	4.5.35	LOGO Rules	Add the description, “and non-dummy TCD”.
78.	SRAM.A.1	4.5.36	SRAM Rules	Add this rule
79.	SRAM.R.4^{U}	4.5.36	SRAM Rules	Move the table to Table 4.5.36.1
80.	SRAM.R.20g^{U}	4.5.36	SRAM Rules	Add this guideline
81.		4.5.43	Antenna Rules	Change diode to protection OD.
82.		4.6	CMN65 (Mixed Singnal, RF) Layout Rules and Guidelines	Add this section(merged from T-N65-CM-DR-001)
83.		5	Wire Bond, Flip Chip and Interconnection Design Rules	Add this chapter (merged from T-000-CL-DR-002)
84.		6	N55 Design Information	Add this chapter (merged from T-N55-CL-DR-001)
85.	PO.EN.1m	7.2	Layout Rules for the WPE (Well Proximity Effect)	Separate it to {(NW NOT OD2) NOT NT_N} for 3.3V IO process and (NW NOT NT_N) for1.8V or 2.5V IO process
86.	PO.EN.3m	7.2	Layout Rules for the WPE (Well Proximity Effect)	Separate it to 3.3V PMOS gate enclosure by {(NW AND OD2) NOT NT_N} and 1.8V or 2.5V PMOS gate enclosure by (NW NOT NT_N)
87.	AN.R.45mg^{U}	7.4.2	MOS Recommendations and Guidelines	Add this guideline
88.	BJT.R.6®	7.4.3	Bipolar Transist or (BJT) Rules and Recommendations	Change it from 5.5 to 3
89.	RES.5m®	7.4.4	Resistor Rules and Recommendations	Add this recommendation
90.	AN.R.37mg^{U}	7.4.5	Capacitor Guidelines	Change it to “It is recommended not to use a very long channel device in the design. In order to ensure the channel relaxation time of the MOS capacitor (excluding varactor) is enough to build up charge to the steady state, it is recommended to use proper channel length at the high operation frequency range. The operating frequency shall be below 0.2 * gm / Cgate, where gm is the transconductance of the transistor and Cgate is the gate-oxide capacitance.”
91.	AN.R.26mg^{U}	7.5.4.1	Power and Ground	Add the description, nd also for the analog and digital circuits. (Figure 7.5.15).
92.		8.3	Dummy TCD Rules and Filling Guidelines	Add this section
93.	Mx.DN.1	8.4	DMx Rules	Modify it from 15% in 50x50, 70% in100x100 to 10% in 75x75, 80% in100x100
94.	Mx.DN.3	8.4	DMx Rules	Removed

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	From Version 1.3 to Version 1.4			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
95.	Mx.DN.3®	8.4	DMx Rules	Removed
96.	Mx.DN.4	8.4	DMx Rules	Modify it from 200umx200um to 250umx250um.
97.	Mx.DN.5	8.4	DMx Rules	Modify it from 70% to 80%
98.	CB.W.4®^{u}	9.2.2	Recommendations	Add thie recommendation (merged from T-000-CL-DR-002)
99.	AP.W.2®^{U}	9.2.2	Recommendations	Add thie recommendation (merged from T-000-CL-DR-002)
100.	UBM.S.4®	9.2.2	Recommendations	Add thie recommendation (merged from T-000-CL-DR-002)
101.	UBM.EN.1®	9.2.2	Recommendations	Add thie recommendation (merged from T-000-CL-DR-002)
102.	UBM.DN.1®	9.2.2	Recommendations	Add thie recommendation (merged from T-000-CL-DR-002)
103.	UBM.DN.3®	9.2.2	Recommendations	Add thie recommendation (merged from T-000-CL-DR-002)
104.	UBM.R.6®^{u}	9.2.2	Recommendations	Add thie recommendation (merged from T-000-CL-DR-002)
105.	CBM.R.2g^{U}	9.2.3	Guidelines	Add thie guidelines (merged from T-N65-CM-DR-001)
106.	VIAz.R.6g^{U}	9.2.3	Guidelines	Add thie guidelines (merged from T-N65-CM-DR-001)
107.	UBM.R.4g^{u}	9.2.3	Guidelines	Add thie guidelines (merged from T-000-CL-DR-002)
108.	UBM.R.5g^{u}	9.2.3	Guidelines	Add thie guidelines (merged from T-000-CL-DR-002)
109.		9.3	Mechanical and Thermal Guidelines for FCBGA	Move this section to chapter 5
110.		9.4	GDA die size optimization kit	Modify this section from “MFU Optimization kit”
111.		10.1.1	Latch-up Introduction	Add this section
112.		10.1.2.1	Special Definition in Latch-up Prevention	Add this section
113.		10.1.2.2	Latch-up Dummy Layers Summary	Add this section
114.		10.1.2.3	Layout Rules and Guidelines for Latch-up Prevention	1. Modify this section from Guidelines for Latch-up Prevention 2. Modify it from LUP.3 to LUP.6 3. Modify it from LUP.1/2/4/5/6/8/9 to LUP.1/2/3/4/5/7/8/9
115.		10.1.3	Test Specification and Requirements	Add this section
116.		10.2.1	ESD introduction	Add this section
117.		10.2.2	TSMC IO ESD layout style introduction	Add this section
118.		10.2.3	ESD Dummy Layers Summary	Add this section
119.		10.2.4	ESD circuits Definition	Add this section
120.		10.2.5	Requirements for ESD Implant Masks	Add this section
121.		10.2.6	ESD Guidelines	1. Modify this section from ESD Guidelines 2. Add ESD.WARN.1, ESD.WARN.2 3. Modify it from ESD.1-47 to ESD.1-57
122.		10.2.7	Tips for the Power Bus	Add this section
123.		10.2.8	ESD test methodology	Add this section
124.		11.3.3.4	Rating factor for Maximum DC Current	Add rating factor from 85C to 100C in table 11.3.1.
125.		11.3.3.5	Maximum DC Current for Metal Lines, Contacts and Vias (T_j = 110°C)	Add the information of Mu/Vu.
126.		11.3.3.5.4	Dependence of Via array/Contact array on DC current (T_j = 110°C)	Add the information of metal/contact/Vu
127.		11.3.4	N55 DC Current Density (EM) Specifications	Add this section (merged from T-N55-CL-DR-001)
128.		11.3.4.1	Rating factor for Maximum DC Current	Add rating factor from 85C to 100C in table 11.3.6.
129.		11.3.5	N65/N55 Cu Metal AC Operation	The AC operations of N55 can be directly shrunk from N65.
130.		11.3.5.3.9	Maximum Root-Mean-Square Current for LK Dielectrics (1P9M M1MxMzMu process)	Add table 11.3.28-35
131.		11.3.6.1	Maximum DC current Current	Add rating factor from 85C to 100C in table 11.3.37.
132.		12	Electrical Parameters Summary	1. Add ULP in CLN65, CLN55: GP, CMN65: GP/LP 2. Remove 1.2V/1.8V in CLN65LP 3. Update other electrical parameter based on the following SPICE document version: ● T-N65-CL-SP-023 from V1.2 to V1.3 ● T-N65-CL-SP-020 from V1.2 to V1.3 ● T-N65-CL-SP-031 from V1.1 to V1.2 ● T-N65-CL-SP-041 from V1.1 to V1.2

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A.1.8 From Version 1.4 to Version 1.4_1

	From Version 1.4 to Version 1.41			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.	Mx.S.1	4.5.26	Mx Rules	Mx.S.1 was described in DRM V1.3 but lost in DRM V1.4 due to typo. So, Mx.S.1 is put back in DRM V1.4_1.
2.	Mx.S.1®	4.5.26	Mx Rules	Mx.S.1® was described in DRM V1.3 but lost in DRM V1.4 due to typo. So, Mx.S.1® is put back in DRM V1.4_1.

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A.1.9 From Version 1.4_1 to Version 2.0

	From Version 1.4_1 to Version 2.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.				Merge T-N65-CL-DR-029(5V HVMOS rule, V1.0), T-N55-CL-DR-005(N55 rule, V1.0)
2.		Title		Add CLN55: LP, CMN55: LP, in tilte
3.		1.1	Overview	Add CLN65LP/ CMN65LP 5V HVMOS, CLN55: LP, CMN55: LP
4.		1.2	Reference Documentation	Modify Table 1.2.1
5.		2.1.1	Front-End Features	1. Add CLN55: LP, CMN55: LP 2. Update SRAM cells' information 3. Add eDRAM information
6.		2.1.2	Back-End Features	1. Add AP-MD infromnation 2. Revise Cu RDL description 3. Revise MS and RF process for CMN65GP/ LP and CMN55LP 4. Remove inductor devices for N55 generation
7.		2.2	Devices	1. Modify table 2.2.1 2. Add CLN55LP, CMN55LP
8.		2.3	Power Supply and Operation Temperature Ranges	1. Modify table 2.3.1 2. Add CLN55LP, CMN55LP, 5V HVMOS only for LP 2.5V IO 3. Add maximum power supply voltage 4. Add table 2.3.2 (merge from T-N65-CL-DR-029)
9.		2.5	Metallization Options	1. Add CMN55, AP-MD, RV 2. Add CMN55LP metallization options
10.		3.1	Mask Information, Key Process Sequence, and CAD Layers	1. Add HVD_P, HVD_N for CLN65LP2.5V 2. Update FW_AP Mask ID for CLN65G1.8V 3. Add CLN55P2.5V 4. Add CMN55 in table 3.1.12 5. Add the wording for CMN55 6. Add LDC_N information in table 3.1.13
11.		3.4	Special Recognition CAD Layer Summary	1. Modify Ncap_NTN, RTMOMDMY, DMxEXCL 2. Add CDUDMY, BJTDMY (drawing 1), HVD_N, HVD_P, CTMDMY (drawing 1), RFDMY (drawing 1), VDDDMY, VSSDMY, HIA_DUMMY, M1(pin) ~ M9(pin)
12.		3.5	Device Truth Tables	1. Add HV MOS 2. Add sections for CLN55 LP, CLN65/ CMN65/ CLN55/ CMN55 MOM, CMN65LP high current diode 3. Remove Mx+Mz+Mz+AP-RDL in CMN65 inductor
13.		3.6	Mask Requirements for Device Options (High/STD/Low VT)	Add CLN55LP/ CMN55LP
14.	G.1	3.7.1	Design Geometry Rules	Add the description, DRC will not flag UBM/ CBD/PM/CB2/PM2/PPI layers when vertexes of polygon are larger than 100.
15.		3.7.1.1	DBU guideline	Add
16.		4.1	CMN65 (MIXED SINGNAL, RF) Layout Rules and guidelines Layout Rule Conventions	Modify title
17.		4.2.2	Special Definition	Add HV NMOS, HV PMOS, Guard ring (merge from T-N65-CL-DR-029)
18.	DNW.S.2	4.5.1	Deep N-Well (DNW) Layout Rules (Mask ID: 119) [Optional]	Add the description " with different potential"
19.	DNW,S,3	4.5.1	Deep N-Well (DNW) Layout Rules (Mask ID: 119) [Optional]	Add the description "except dummy TCD region (TCDDMY)"
20.	NW,S,3	4.5.3	N-Well (NW) Layout Rules	Add the description " with different potential (*)"
21.	NW.S.6	4.5.3	N-Well (NW) Layout Rules	Add the description "except dummy TCD region (TCDDMY)"
22.	NWROD.R.4 NWROD.R.5 NWROD.R.6 NWROD.R.7	4.5.4	N-Well Resistor Within OD (NWROD) Layout Rules	Add
23.		4.5.6	Native Device (NT_N) Layout Rules	Remove the description "A Native NMOS device is based on a standard Vt process. It cannot be applied to pure low Vt designs."

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	From Version 1.4_1 to Version 2.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
24.	NT_N.W.2.3	4.5.6	Native Device (NT_N) Layout Rules	Add
25.	NT_N.R.3	4.5.6	Native Device (NT_N) Layout Rules	Modify the descriptoion
26.		4.5.9	OD25_33 Layout Rules	1. Add N55LP into the description 2. Remove “2.5V overdrive to 3.3V is not offered in 2.5V native device”.
27.		4.5.10	OD25_18 Layout Rules	Add N55LP into the description
28.	PO.S.2®	4.5.11	Poly (PO) Layout Rules (Mask ID: 130)	Add the wording “GP/LPG/ULP”
29.	PO.L.1	4.5.11	Poly (PO) Layout Rules (Mask ID: 130)	Add the description “except RTMOM region (RTMOMDMY, CAD layer: 155;21)”.
30.	PO.FU.R.8	4.5.11	Poly (PO) Layout Rules (Mask ID: 130)	Add the description “only for N65GP/ N55GP/ N55LP”
31.	PO.R.7g^{U}	4.5.11	Poly (PO) Layout Rules (Mask ID: 130)	Remove
32.	VTH_N.S.3	4.5.12	High Vt NMOS (VTH_N) Layout Rules (Mask ID: 128)	Remove unsilicided PO
33.	VTH_P.S.3	4.5.13	High Vt PMOS (VTH_P) Layout Rules (Mask ID: 127)	Remove unsilicided PO
34.	VTL_N.S.3	4.5.14	Low Vt NMOS (VTL_N) Layout Rules (Mask ID: 118)	Remove unsilicided PO
35.	VTL_P.S.3	4.5.15	Low Vt PMOS (VTL_P) Layout Rules (Mask ID: 117)	Remove unsilicided PO
36.		4.5.17	HVD_N Layout Rules	Add the section (merge from T-N65-CL-DR-029)
37.		4.5.18	HVD_N Layout Rules	Add the section (merge from T-N65-CL-DR-029)
38.		4.5.19	5V HVMOS Layout Rules and Guidelines	Add the section (merge from T-N65-CL-DR-029)
39.		4.5.22	Layout Rules for LDD Mask Logical Operations	Remove the warning description “ recommendations”
40.	RES.8	4.5.24	OD and Poly Resistor Recommendations and Guidelines	Add
41.	RES.10 RES.11	4.5.24	OD and Poly Resistor Recommendations and Guidelines	Change the guidelines to rules
42.		4.5.25	MOS Varactor Layout Rules (VAR)	1. Modify the section to meet SPICE model 2. Modify VAR.W.1, VAR.W.4 3. Remove VAR.W.2, VAR.W.3, VAR.A.1® 4. Add the table 4.5.25.1 minumum W/L of baseband and RF model for SPICE valid range
43.		4.5.36	MOM Layout Rules	1. Add the description “TSMC RTMOM PDK cell is without Via” 2. Remove MOM.S.2® 3. Remove MOM.R.g^{U}
44.		4.5.36.1	RTMOM (Rotated Metal Oxide Metal) Capacitor Guidelines	1. Remove figure 4.5.33.1.1 2. Add description for item 1 2. Add the item 7 and 8
45.	SRAM.R.3^{U}	4.5.39	SRAM Rules	Modifies the description
46.	SRAM.R.15	4.5.39	SRAM Rules	Add the description “except SRAM 0.62 μm² cell size of N55GP”.
47.		4.5.39	SRAM Rules	1. Revise the mm^2 to um^2 2. Add VTC_N for N65ULP high VT 3. Remove VTC_P for N55GP 4. Add N55LP
48.		4.5.42	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Add WLCSP information
49.	CSR.EN.5 CSR.EN.5.1 CSR.EN.6 CSR.EN.6.1	4.5.43	Chip Corner Stress Relief Pattern (CSR)	1. Add the description “Except WLCSP sealring region” 2. Add the rule for WLCSP sealring 3. Add the description “Except WLCSP sealring region” 4. Add the rule for WLCSP sealring 5. Add the figure of chip corner stress relief pattern for WLCSP
50.	SR.R.1	4.5.44	Seal Ring Layout Rules	Modify the description for non-WLCSP seal ring and for WLCSP seal ring

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	From Version 1.4_1 to Version 2.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
51.	SR.EN.1	4.5.44	Seal Ring Layout Rules	Add
52.		4.5.44	Seal Ring Layout Rules	1. Add cross-sectional view of WLCSP sealring 2. Add the mask information for WLCSP layers
53.	A.R.10~13	4.5.46	Antenna Effect Prevention (A) Layout Rules	Merge from 5.1.2.6.3 Antenna Effect Prevention (A) Layout Rules for RV and AP-MD.
54.	CTM.R.3	4.6.1	Capacitor Top Metal (CTM) Layout Rules (Mask ID: 182)	Add the rule (merge from T-N55-CL-DR-005)
55.	Mx.DN.6 Mx.R.3g^{U}	4.6.2	Capacitor Bottom Metal (CBM) Layout Rules (Mask ID: 183)	Add
56.	VIAz(u).R.6g^{U}	4.6.4.1	VIAz(u) Layout Rule (Mask ID: 373, 374, 375, 376, 377, 372) for CTM/CBM	Modify the RF application to MIM application.
57.		4.6.6.1.2	MIM Structure Recognition Methodology	Add this section
58.		4.6.6.1.3	Check Methods	Change the figures of (k), (p), (q) from balanced to unbalanced
59.	A.R.MIM.2 A.R.MIM.3	4.6.6.2	Antenna Effect Prevention Layout Rules	1. Add the wording “and AP-MD sidewall area” 2. Add the connect “to OD” for balance structure
60.	A.R.MIM.4 A.R.MIM.5	4.6.6.2	Antenna Effect Prevention Layout Rules	1. Modify the description from single layer to cumulative 2. Add the connect “to OD” for balance structure
61.	Mu.DN.3	4.6.7	Ultra Thick Metal (Mu) Layout Rules (Mask ID: 384, 385, 386, 387, 388, 389)	Change Mz to Mu
62.		4.6.8	Layout Rules for Inductors with INDDMY Layer	Remove the description “ For customized inductors…”
63.	IND.DN.1	4.6.8	Layout Rules for Inductors with INDDMY Layer	Modify the descrption
64.	IND.R.15^{U} IND.R.16^{U}	4.6.8	Layout Rules for Inductors with INDDMY Layer	Add
65.		4.6.9.1	Introduction to PDK Inductor	Remove Mx+Mz+Mz+Al-RLD in table 4.6.9.1
66.	CSR.EN.6 CSR.EN.6.1	4.6.10	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	1. Add the description for “N65_Mu_SR_09282009_WLCSP.gds” 2. Add the description “except WLCSP sealring region” 3. Add this rule for WLCSP sealring
67.		4.6.11	Seal-Ring Rule	1. Add the description for “N65_Mu_SR_09282009_WLCSP.gds” 2. Add the cross-sectional view of seal ring for WLCSP
68.	SR.EN.1	4.6.11	Seal-Ring Rule	Add
69.		5	Wire Bond, Flip Chip and interconnection Design rules	1. Add the warning information 2. Add the description for 14.5K and 28K of AP-MD thickness 3. Add the description for lead-free bump design rule, please consult with tsmc.
70.		5.1.2.2	Passivation Layer Open Rules	1. Modfiy the table 5.1.2.2.1 and add 40um/50um/60um single in-line and 45um/50um staggered 2. Add the description “40um pitch single in-line and 45um pitch staggered are not supported in N55.”
71.		5.1.2.5	Wire Bond Non-shrinkable Rules for the N55	1. Add the description “40um pitch single in-line and 45um pitch staggered are not supported in N55.” 2. Modfiy the table and add 45um single in-line and 50um stagger
72.		5.1.2.6	RV and AP-MD Layout Rules for Wire Bond	Update the figures
73.	RV.R.1	5.1.2.6.1	RV Layout Rules (CB VIA hole)	Add the description “Except WLCSP seal ring region”
74.	AP.S.1.1	5.1.2.6.2	AP-MD Layout Rules	Add the description “Except spacing in the same polygon”
75.	AP.R.1^{U}	5.1.2.6.2	AP-MD Layout Rules	Add the wording “Need to add polyimide layer for wirebond using AP-MD routing for die size >= 100mm^2”
76.		5.1.2.6.3	Antenna Effect Prevention (A) Layout Rules for RV and AP-MD.	Remove (merge into 4.5.46 Antenna Effect Prevention (A) Layout Rules)
77.		5.2	Layout Rules for EU/HL Flip Chip	1. Modify the title to add “EU/HL” 2. Remove the wording of LF: lead free 3. Add the description " “ For lead free application, please refer to LF design rule”
78.		5.2.1	Recommendations for	Add the description of item 14 “If you are going to design a

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	From Version 1.4_1 to Version 2.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
			EU/HL Flip Chip	new produt……."
79.		5..2.1.2	Recommendations for Redistribution Metal	Remove " Recommended minimum counts of VIAD conncting to bump pad:300 each".
80.		5.2.2	Under Bump Metallurgy (UBM) Rules	Add the description "For lead-free bump design rule, please consult with tsmc"
81.	UBM.DN.1	5.2.2	Under Bump Metallurgy (UBM) Rules	Modify the rule value to 10% from 2.5%
82.	UBM.DN.1®	5.2.2	Under Bump Metallurgy (UBM) Rules	Remove (merge into UBM.DN.1)
83.	UBM.DN.2	5.2.2	Under Bump Metallurgy (UBM) Rules	Remove (merge into UBM.DN.1)
84.	UBM.DN.3	5.2.2	Under Bump Metallurgy (UBM) Rules	Remove the description " for the die sizing > = 169mm^2"
85.	UBM.DN.3®	5.2.2	Under Bump Metallurgy (UBM) Rules	Remove (merge into UBM.DN.3)
86.	UBM.R.5	5.2.2	Under Bump Metallurgy (UBM) Rules	1. Change the "^{U}" to the rule and modify the description 2. Add the Note for LF application 3. Add the schematic diagram
87.		5.2.3.1	Mask Information	Remove the wording "Cu RDL (Cu MD) is prohibited".
88.	BP.EN.5	5.2.3.2	Bump Pad Structure Rules	Add the description " without AP RDL/ with AP RDL…"
89.		5.2.3.2	Bump Pad Structure Rules	Add the description " For lead free application, please refer to LF design rule"
90.		5.2.3.3	Polyimide (PM) Rules for EU/HL Flip Chip	1. Modify the title to add "EU/HL" 2. Add the description " Polyimide is must for LF application……..."
91.	BP.EN.5	5.2.3.4	Flip Chip Non-shrinkable Rules for the N55	Add the description " without AP RDL/ with AP RDL…"
92.	RV.R.1	5.2.3.5.1	RV Layout Rules (Passivation-1 VIA Hole)	1. Add the description "Except WLCSP seal ring region" 2. Remove the wording of LF: lead free
93.		5.2.3.5.3	Seal Ring Structure Using AP-MD layer	Modify the title to add "S"
94.		6.1	Overview	1. Add the information for CLN55LP/ CMN55LP 2. Modify the description for metal scheme of N55
95.		6.1.2	SRAM Design Specifications	Remove the wording "GP"
96.	SRAM.R.15	6.2.3	SRAM Rules	Add the description "except SRAM 0.62 μm² cell size of N55GP".
97.		6.2.4.1	Non-shrinkable Rules	Modify table
98.	#BP.EN.5	6.2.5.1	Non-shrinkable Rules	Add the description " without AP RDL/ with AP RDL…"
99.	PO.EN.3m	7.2	Layout Rules for the WPE (Well Proximity Effect)	Modify the "Core" to "IO" PMOS
100.		7.4.3	Parasitic Bipolar Transist or (BJT) Rules and Recommendations	1. Modify the section due to tsmc off two set of BJT models 2. Remove BJT.R.3®, BJT.R.4®, BJT.R.5®, BJT.R.6®, BJT.R.7®
101.	Mx.DN.1	8.4	Dummy Metal (DM) Rules	Modify the wording "10%" for LMARK
102.	Mx.DN.2	8.4	Dummy Metal (DM) Rules	Add the description of Mx.DN.2 would exclude the following regions.
103.	DMx_O.R.1	8.4	Dummy Metal (DM) Rules	Add
104.		9.1.2.1	Transistors	Remove the wording "pay attention to the unexpected leakage current from floating gate".
105.	PO.S.14® PO.EN.1® PO.EN.2® PO.EN.3®	9.2.1	Action-Required Rules	Change to section 9.2.2 recommendations
106.	MOM.S.2®	9.2.2	Recommendations	Remove
107.	PO.R.7g^U MOM.R.1g^U	9.2.3	Guidelines	Remove
108.	VIAz.R.6g^U	9.2.3	Guidelines	Modfiy the RF application to MIM application.
109.		9.2.4	Grouping Table of DFM Action-Required Rules, Recommendations and Guidelines	Remove MOM.S.2®, PO.R.7g, MOM.R.1g^U
110.		10.1.1	Latch-up Introduction	Update figures 10.1.3~10.1.6
111.		10.1.2.3	DRC methodology for Latch-up Rules	Add this section
112.	LUP.3.5.1g LUP.3.5.2g LUP.5.5.1g LUP.3.5.2g	10.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Add these guidelines (merge from T-N65-CL-DR-029)

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	From Version 1.4_1 to Version 2.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
113.		10.2.3.2	ESD3 Dummy Layer Description	Add the description for ESD3 should enclosure of ACTIVE.
114.		10.2.6.5	5V HVMOS protection (Field Device)	Add this section
115.		10.2.7	CDM Protection for Cross Domain Interface	Add this section
116.		10.2.8	High Current Diode (HIA_DIO)	Add this section
117.		10.2.9	Tips for the Power Bus	Modify the description
118.		10.2.9.1	Approach	Modify the description
119.		11.2	Front-End Process Reliability Rules and Models	1. Add N55 reliability informations 2. Add the description for guidelines for negative bias temperature instability (NBTI) 3. Add the description for failure mechanism of NBTI
120.		11.3	Back-End Process Reliability Rules	Merge N65/N55 currnet density specifications Add the Imax for 28KÅ AP RDL
121.		11.3.7	Poly Current Density Specifications	Update title from Guidelines to Specifications
122.		11.3.8	OD Current Density Specifications	Update title from Guidelines to Specifications
123.		12	Electrical parameters Summary	Modify this section and add the key parameters of MOS transistors in CLN55LP, CLN65LPHV, add MOM capacitor model, RF I/O PAD model

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A.1.10 From Version 2.0 to Version 2.1

	From Version 2.0 to Version 2.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.				Merge T-N65-CM-DR-016 V1.0 (TSMC 65 NM / 55 NM CMOS MS_RF LOGIC INDUCTOR DESIGN RULE)
2.				Merge T-N65-CL-DR-043 V1.0 (5V GUARD-RING DESIGN RULE)
3.				Merge T-N65-CL-DR-040 V1.0 (TSMC 65 NM ESD IMPLANT (ESDIMP) DESIGN RULE)
4.		1.2	Reference Document	(1)Add lead free flip chip doc. T-000-CL-DR-017 (2)Add schottky barrier diode doc. T-N65-CM-DR-015 (3)Add P+/PW Varactor design rule T-N65-CM-DR-012 (4)Add N55 5V HVMOS design rule T-N55-CL-DR-006
5.		2.2	Device	Add Table Note for Table 2.2.1
6.		2.2	Device	Remove N55LP mLVT device
7.		3.1	Mask information, key process sequence, and CAD layer	Add warning message
8.		3.1	Mask information, key process sequence, and CAD layer	(1)Add NW2V information into Table3.1.14 (2)Modify mask name from LDC_N to VTC_N at Table3.1.14
9.		3.3	Dummy Pattern Fill CAD Layer	Update Table Note from section 6 to section 8
10.		3.4	Special Recognition CAD Layer Summary	Add RPDMY information into Table3.4.1
11.		3.4	Special Recognition CAD Layer Summary	Modify SEALRING information (For N55, SEALRING is tape out required layer)
12.		3.4	Special Recognition CAD Layer Summary	Modify HVD_N and HVD_P as tape out required layers
13.		3.4	Special Recognition CAD Layer Summary	Add AP (pin) into table 3.4.1 Add ESDIMP (merge T-N65-CL-DR-040)
14.		3.5.4	CLN65 LP-based Triple Gate Oxide (LPG) Design	Put OD25_18 and OD25_33 into special layer
15.		3.5.5	CLN65 Ultar Low Power (ULP) Design	Add LVT information
16.		3.5.7	CLN55 Low Power (LP)	Add LVT and 5V HVMOS information
17.	G.1	3.7.1	Design Geometry Rules	Add “DRC will not flag PM1”, and align DRC to remove “when vertexes of polygon are larger than 100”.
18.		3.9	Chip Implementation and Tape Out Checklist	Add this section
19.		4.1	Layout Rule Conventions	Modify the title from “CMN65 (MIXED SINGAL, RF) Layout Rules and guidelines” to “Layout Rule Conventions”
20.	DNW.R.3	4.5.1	Deep N-Well (DNW) Layout Rules	Align DRC to modify to “uncheckable “
21.	NWROD.S.3®	4.5.4	N-Well Resistor Within OD (NWROD) Layout Rules	Refine description, no DRC change
22.	NWRSTI.EN.2®	4.5.5	N-Well Resistor Under STI (NWRSTI) Layout Rules	Refine description, no DRC change
23.	PO.DN.3	4.5.11	Poly (PO) Layout Rules	Add “except RFDMY”
24.	VTH_N.R.2	4.5.12	High Vt NMOS (VTH_N) Layout Rules	Refine wording, no DRC change
25.	VTH_P.R.2	4.5.13	High Vt PMOS (VTH_P) Layout Rules	Refine wording, no DRC change
26.	VTL_N.R.2	4.5.14	Low Vt NMOS (VTL_N) Layout Rules	Refine wording, no DRC change
27.	VTL_P.R.2	4.5.15	Low Vt PMOS (VTL_P) Layout Rules	Refine wording, no DRC change
28.	GR.R.2[U] GR.R.3[U] GR.R.4®[U] GR.R.5[U] GR.R.6[U] GR.R.7 GR.R.8 GR.R.9[U] GR.R.10 GR.R.11	4.5.19.1	Guard Ring Rules and Guidelines	Merge from T-N65-CL-DR-043

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	From Version 2.0 to Version 2.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
	GR.R.12 [U] GR.R.13 GR.R.14 GR.R.15® [U]			
29.		4.5.25	MOS Varactor Layout Rules (VAR)	Update N55LP dimension for Table 4.5.25.1
30.		4.5.27	Metal-1 (M1) Layout Rules (Mask ID:360)	Refine wording for “Table Note”
31.	M1.DN.1	4.5.27	Metal-1 (M1) Layout Rules (Mask ID:360)	Separate min. and max. rules to add M1.DN.1.1
32.	M1.DN.1.1	4.5.27	Metal-1 (M1) Layout Rules (Mask ID:360)	Separate min. and max. rules to add M1.DN.1.1
33.	M1.DN.2	4.5.27	Metal-1 (M1) Layout Rules (Mask ID:360)	Refine wording, no DRC change
34.	Mx.DN.1	4.5.29	Mx Layout Rules	Separate min. and max. rules to add Mx.DN.1.1
35.	Mx.DN.1.1	4.5.29	Mx Layout Rules	Separate min. and max. rules to add Mx.DN.1.1
36.	Mx.DN.2	4.5.29	Mx Layout Rules	Refine wording, no DRC change
37.		4.5.29	Mx Layout Rules	Refine wording for “Table Note”
38.	My.DN.1	4.5.31	My Layout Rules	Separate min. and max. rules to add My.DN.1.1
39.	My.DN.1.1	4.5.31	My Layout Rules	Separate min. and max. rules to add My.DN.1.1
40.		4.5.31	My Layout Rules	Refine wording for “Table Note”
41.	Mz.DN.1	4.5.33	Top Mz Layout Rules	Separate min. and max. rules to add Mz.DN.1.1
42.	Mz.DN.1.1	4.5.33	Top Mz Layout Rules	Separate min. and max. rules to add Mz.DN.1.1
43.		4.5.33	Top Mz Layout Rules	Refine wording for “Table Note”
44.	Mr.R.1 [U]	4.5.35	Top Mr Layout Rules	Remove the duplicate rule
45.	Mr.DN.1	4.5.35	Top Mr Layout Rules	Separate min. and max. rules to add Mr.DN.1.1
46.	Mr.DN.1.1	4.5.35	Top Mr Layout Rules	Separate min. and max. rules to add Mr.DN.1.1
47.		4.5.35	Top Mr Layout Rules	Refine wording for “Table Note”
48.	SRAM.R.15	4.5.39	SRAM Rules	Remove “except SRAM 0.62um^2 cell size of N55GP”
49.		4.5.42	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Add wording “WLCSP sealring can be used for WB/FC process”
50.		4.6.8	INDDMY Rule Overview	Add inductor information (merge T-N65-CM-DR-016
51.	IND.R.15	4.6.8	INDDMY Rule Overview	Change to ceckable
52.	IND.R.16	4.6.8	INDDMY Rule Overview	Change to ceckable
53.	IND.R.17g [U]	4.6.8.1	Layout Rules for Inductors with INDDMY Layer	Add recommendation to achieve the high quality factor
54.	IND.R.15	4.6.8.1	Layout Rules for Inductors with INDDMY Layer	Change to checkable
55.	IND.R.16	4.6.8.1	Layout Rules for Inductors with INDDMY Layer	Change to checkable
56.	Waive items	4.6.8.1	Layout Rules for Inductors with INDDMY Layer	Add inductor information (merge T-N65-CM-DR-016
57.		4.6.8.2	Layout Rules for Inductor with INDDMY_MD Layer	Add INDDMY_MD information (merge T-N65-CM-DR-016
58.		4.6.8.3	Layout Rules for Inductor with INDDMY_HD Layer	Add INDDMY_HD information (merge T-N65-CM-DR-016
59.	CSR.EN.10	4.6.9	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	1.Rename from CSR.EN.6 to CSR.EN.10 2.Refine description, no DRC change
60.	SR.EN.2	4.6.10	Seal-Ring Rules	Rename from SR.EN.1 to SR.EN.2
61.		4.7	RV Layout Rules (CB VIA hole)	Move this section from s5.1.2.6.1 to s4.7
62.	RV.W.1.WB	4.7.1	RV Layout Rules (CB VIA hole) for Wire Bond	Rename from RV.W.1 toRV.W.1.WB
63.	RV.S.1.WB	4.7.1	RV Layout Rules (CB VIA hole) for Wire Bond	Rename from RV.S.1 to RV.S.1.WB
64.	RV.S.3.WB	4.7.1	RV Layout Rules (CB VIA hole) for Wire Bond	Rename from RV.S.3 to RV.S.3.WB
65.	RV.EN.1.WB	4.7.1	RV Layout Rules (CB VIA hole) for Wire Bond	Rename from RV.EN.1 to RV.EN.1.WB
66.	RV.R.1.WB	4.7.1	RV Layout Rules (CB VIA hole) for Wire Bond	Rename from RV.R.1 to RV.R.1.WB
67.	RV.R.2.WB	4.7.1	RV Layout Rules (CB VIA hole) for Wire Bond	Rename from RV.R.2 to RV.R.2.WB
68.	RV.W.1.FC	4.7.2	RV Layout Rules (Passivation-1 VIA hole) for Flip Chip	Rename from RV.W.1 to RV.W.1.FC
69.	RV.S.1.FC	4.7.2	RV Layout Rules	Rename from RV.S.1 to RV.S.1.FC

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	From Version 2.0 to Version 2.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
			(Passivation-1 VIA hole) for Flip Chip	
70.	RV.S.2.FC	4.7.2	RV Layout Rules (Passivation-1 VIA hole) for Flip Chip	Rename from RV.S.2 to RV.S.2.FC
71.	RV.EN.1.FC	4.7.2	RV Layout Rules (Passivation-1 VIA hole) for Flip Chip	Rename from RV.EN.1 to RV.EN.1.FC
72.	RV.R.1.FC	4.7.2	RV Layout Rules (Passivation-1 VIA hole) for Flip Chip	Rename from RV.R.1 to RV.R.1.FC
73.	RV.R.3.FC	4.7.2	RV Layout Rules (Passivation-1 VIA hole) for Flip Chip	Rename from RV.R.3 to RV.R.3.FC
74.		4.8	AP-MD Layout Rules	Move this section from 5.1.2.6.2 to s4.8
75.	AP.W.1.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.W.1 to AP.W.1.WB
76.	AP.W.2.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.W.2 to AP.W.2.WB
77.	AP.W.2.WB®^{U}	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.W.2®^{U} to AP.W.2.WB®^{U}
78.	AP.W.3.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.W.3 to AP.W.3.WB
79.	AP.S.1.WB	4.8.1	AP-MD Layout Rules for Wire Bond	1.Add “except space in the same polygon and in {CB2 SIZING 5um} region” 2.Rename from AP.S.1 to AP.S.1.WB
80.	AP.S.1.1.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.S.1.1 to AP.S.1.1.WB
81.	AP.S.2.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.S.2 to AP.S.2.WB
82.	AP.S.3.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.S.3 to AP.S.3.WB
83.	AP.S.4.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.S.4 to AP.S.4.WB
84.	AP.EN.1.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.EN.1 to AP.EN.1.WB
85.	AP.EN.2.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.EN.2 to AP.EN.2.WB
86.	AP.DN.1.WB	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.DN.1 to AP.DN.1.WB
87.	AP.R.1.WB^{U}	4.8.1	AP-MD Layout Rules for Wire Bond	Rename from AP.R.1^{U} to AP.R.1.WB^{U}
88.	AP.W.1.FC	4.8.2	AP-MD Layout Rules for Flip Chip	Rename from AP.W.1 to AP.W.1.FC
89.	AP.W.2.FC	4.8.2	AP-MD Layout Rules for Flip Chip	1.Modify from “Not inside CB or CB2” to “NOT INSIDE UBM, CBD OR CB2” 2. Rename from AP.W.2 to AP.W.2.FC
90.	AP.W.2.FC®^{U}	4.8.2	AP-MD Layout Rules for Flip Chip	Rename from AP.W.2®^{U} to AP.W.2.FC®^{U}
91.	AP.W.3.FC	4.8.2	AP-MD Layout Rules for Flip Chip	Rename from AP.W.3 to AP.W.3.FC
92.	AP.S.1	4.8.2	AP-MD Layout Rules for Flip Chip	Add “except space in the same polygon and in {UBM SIZING 5um} region”
93.	AP.S.1.FC	4.8.2	AP-MD Layout Rules for Flip Chip	Rename from AP.S.1.1 to AP.S.1.1.FC
94.	AP.S.2.FC	4.8.2	AP-MD Layout Rules for Flip Chip	Rename from AP.S.2 to AP.S.2.FC
95.	AP.S.3.FC	4.8.2	AP-MD Layout Rules for Flip Chip	Rename from AP.S.3 to AP.S.3.FC
96.	AP.S.4.FC	4.8.2	AP-MD Layout Rules for Flip Chip	Rename from AP.S.4 to AP.S.4.FC
97.	AP.EN.1.FC	4.8.2	AP-MD Layout Rules for Flip Chip	Rename from AP.EN.1 to AP.EN.1.FC
98.	AP.DN.1.FC	4.8.2	AP-MD Layout Rules for Flip Chip	Rename from AP.DN.1 to AP.DN.1.FC
99.		4.6.11	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Modify Table note from VIA4(x)(54;0), (35:0), (55:0) and (36:0) to VIA5(z)(54;40), (35:40), (55:40) and (36:60)
100.		5	Wire Bump, Flip Chip and Interconnection Design	Move the content to T-000-CL-DR-017

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	From Version 2.0 to Version 2.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
			Rules	
101.	M1.S.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from M1.S.2 to M1.S.2.S
102.	M1.S.2.1.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from M1.S.2.1 to M1.S.2.1.S
103.	M1.S.2.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from M1.S.2.2 to M1.S.2.2.S
104.	M1.S.2.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from M1.S.2.3 to M1.S.2.3.S
105.	M1.S.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from M1.S.3 to M1.S.3.S
106.	M1.S.4.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from M1.S.4 to M1.S.4.S
107.	VIAx.R.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAx.R.2 to VIAx.R.2.S
108.	VIAx.R.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAx.R.3 to VIAx.R.3.S
109.	VIAx.R.4.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAx.R.4 to VIAx.R.4.S
110.	VIAx.R.5.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAx.R.5 to VIAx.R.5.S
111.	VIAx.R.6.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAx.R.6 to VIAx.R.6.S
112.	Mx.S.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mx.S.2 to Mx.S.2.S
113.	Mx.S.2.1.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mx.S.2.1 to Mx.S.2.1.S
114.	Mx.S.2.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mx.S.2.2 to Mx.S.2.2.S
115.	Mx.S.2.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mx.S.2.3 to Mx.S.2.3.S
116.	Mx.S.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mx.S.3 to Mx.S.3.S
117.	Mx.S.4.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mx.S.4 to Mx.S.4.S
118.	VIAy.R.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAy.R.2 to VIAy.R.2.S
119.	VIAy.R.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAy.R.3 to VIAy.R.3.S
120.	VIAy.R.4.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAy.R.4 to VIAy.R.4.S
121.	VIAy.R.5.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAy.R.5 to VIAy.R.5.S
122.	VIAy.R.6.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAy.R.6 to VIAy.R.6.S
123.	My.S.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from My.S.2 to My.S.2.S

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	From Version 2.0 to Version 2.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
124.	My.S.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from My.S.3 to My.S.3.S
125.	My.S.4.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from My.S.4 to My.S.4.S
126.	VIAz.R.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAz.R.2 to VIAz.R.2.S
127.	VIAz.R.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAz.R.3 to VIAz.R.3.S
128.	Mz.S.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mz.S.2 to Mz.S.2.S
129.	Mz.S.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mz.S.3 to Mz.S.3.S
130.	VIAr.R.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAr.R.2 to VIAr.R.2.S
131.	VIAr.R.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from VIAr.R.3 to VIAr.R.3.S
132.	Mr.S.2.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mr.S.2.S to Mr.S.2.S
133.	Mr.S.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from Mr.S.3.S to Mr.S.3.S
134.	DMx.S.3.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from DMx.S.3 to DMx.S.3.S
135.	DMx.S.3.1.S	6.2.2	Stress Migration and Wide Metal Spacing Rules Adjustment	Rename from DMx.S.3.1 to DMx.S.3.1.S
136.	SRAM.R.15	6.2.3	SRAM Rules	Remove “except SRAM 0.62um^2 cell size of N55GP”
137.		6.2.4.1	Non-shrinkable Rules	Move the related pad rules to T-000-CL-DR-017
138.		6.2.5.1	Non-shrinkable Rules	Move the related pad rules to T-000-CL-DR-017
139.	AN.R.2mg^U	7.4.1	General Guideline	Remove the unnecessary description
140.	Mx.DN.1	8.4	Dummy Metal (DM) Rules	Separate min. and max. rules to add M1.DN.1.1
141.	Mx.DN.1.1	8.4	Dummy Metal (DM) Rules	Separate min. and max. rules to add M1.DN.1.1
142.	Mx.DN.1	8.4	Dummy Metal (DM) Rules	Remove “(M1/Mx/My/Mz/Mr)”; align whit format
143.	Mx.DN.4	8.4	Dummy Metal (DM) Rules	Align with the description of sec. 4.
144.	Mx.DN.5	8.4	Dummy Metal (DM) Rules	Align with the description of sec. 4.
145.	PO.S.2®	9.2.1	Action-Required Rules	Add “GP/LPG/ULP” (v2.0 had agreed)
146.	VAR.A.1®	9.2.1	Action-Required Rules	Remove (v2.0 had agreed)
147.	RES.2®	9.2.2	Recommendation	Align with the description of sec. 4.
148.	RES.5m®	9.2.2	Recommendation	Align with the description of sec. 4.
149.	RES.8®	9.2.2	Recommendation	Align with the description of sec. 4.
150.	RES.9®	9.2.2	Recommendation	Align with the description of sec. 4.
151.	Mx.S.7®	9.2.2	Recommendation	Align with the description of sec. 4.
152.	VAR.A.1®	9.2.2	Recommendation	Remove VAR.A.1®
153.		9.2.2	Recommendation	Move CB.W.4®^{U}/UBM.S.4®/UBM.A.EN.1®/UBM.A.1®^{U} /UBM.DN.1®/UBM.DN.3®/UBM.R.6®^{U}/BP.R.2®/UBM.R.7® to T-000-CL-DR-017
154.	OPC.R.2g	9.2.3	Guidelines	Align with the description of sec. 4.
155.	CO.R.5g	9.2.3	Guidelines	Align with the description of sec. 4.
156.	VIAx.R.9g	9.2.3	Guidelines	Align with the description of sec. 4.
157.	VIAy.R.9g	9.2.3	Guidelines	Align with the description of sec. 4.
158.	VIAz.R.5g	9.2.3	Guidelines	Align with the description of sec. 4.
159.	VIAr.R.5g	9.2.3	Guidelines	Align with the description of sec. 4.
160.		9.2.4	Grouping Table of DFM Action-Required Rules, Recommendations and Guideline	Align with the recommendations of sec. 4
161.				
162.		9.3	DFM Service	Remove “DFM Service” section

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	From Version 2.0 to Version 2.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
163.		9.3	GDA die size optimization kit	Update TSMC On-line directory Align on-line to 80%
164.		9.3.1	What is MFU?	Add this section
165.		9.3.2	Recommended GDA criteria MFU>80%	Align on-line to 80%
166.		10.1.2.3.2	DRC methodology for LUP.2	Delete the exception of “NMOS inside NW 5um away from PMOS ”
167.	LUP.2g	10.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify description; no DRC change
168.	LUP.3g	10.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify description; no DRC change
169.	LUP.3.1.0 LUP.3.2.0 LUP.3.3.0 LUP.3.4.0 LUP.3.5.0 LUP.5.2.0 LUP.5.3.0 LUP.5.4.0	10.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Add rule no; no change description
170.		10.2.1	ESD introduction	Modify typo
171.		10.2.3	ESD Implant (ESDIMP) Layout Rules (MASK ID:111)	Add this section (merge from T-N65-CL-DR-040)
172.		10.2.6	Requirements for ESD Implant Masks	Add ESD IMP into table 10.2.1
173.		10.2.7	DRC methodology for ESD quidelines	Add new section to explain DRC methodology
174.	ESD.1g	10.2.8.1	General Guideline for ESD Protection	Relax rule to delete condition2
175.		10.2.8.2	Regular IO (3.3V/2.5V/1.8V/1.2V/1.0V RPO Device)	Align DRC to refine the wording
176.	ESD.34g	10.2.8.3	HV Tolerant I/O	Add ESDIMP
177.	ESD.40g	10.2.8.4	Power Clamp Device	Modify wording; no DRC change
178.		10.2.8.5	5V HVMOS protection (Field Device)	Relax rule to add “NOT RPDMY”
179.	HIA.3g^{U}	10.2.10.1.3.1	HIA_DUMMY Layer (CAD layer: 168;0)	Add new guideline
180.	HIA.4g^{U}	10.2.10.1.3.1	HIA_DUMMY Layer (CAD layer: 168;0)	Change rule no. from HIA.3g^{U} to HIA.4g^{U}
181.	HIA.5g^{U}	10.2.10.1.3.1	HIA_DUMMY Layer (CAD layer: 168;0)	Change rule no. from HIA.4g^{U} to HIA.5g^{U}
182.	HIA.6g^{U}	10.2.10.1.3.1	HIA_DUMMY Layer (CAD layer: 168;0)	Change rule no. from HIA.5g^{U} to HIA.6g^{U}
183.	HIA.7g^{U}	10.2.10.1.3.1	HIA_DUMMY Layer (CAD layer: 168;0)	Relax the guideline from 16 to 15
184.		10.2.11	Tips for the ESD/LU Design	Add new section
185.		10.2.12	Tips for the ESD Protection	Modify the description
186.		10.2.9.1	Approach	Delete this section
187.		11.3.4.4	Peak Current	Add Note “the above equation is only applicable for frequency larger than 1 MHz and *r* larger than 0.05.”
188.		11.3.4.4	Peak Current	Add Mu information into Table 11.3.31
189.		11.3.6	N65/N55 AP RDL AC Operation	Add RDL 28K information
190.		11.3.8	N65 Poly EM Joule heating Guidelines	Add this section
191.		12.1.8	CLN55LP (1.2V)	Remove N55LP mLVT device
192.		12	Electrical Parameters Summary	Udate doc. Version (1) T-N65-CL-SP-009: change from V1.3 to V1.4 (2) T-N65-CL-SP-070: change from V1.0 to V1.1 (3) T-N65-CL-SP-031: change from V1.2 to V1.3 (4) T-N65-CL-SP-041: change from V1.2 to V1.3 (5) T-N55-CL-SP-007: change from V1.1 to V1.2 (6) T-N55-CL-SP-010: change from V1.1 to V1.2 (7) T-N55-CL-SP-021: change from V1.0 to V1.1 (8) T-N65-CM-SP-002: change from V1.3 to V1.4 (9) T-N65-CM-SP-007: change from V1.5 to V1.6 (10) T-N65-CM-SP-012: change from V1.3 to V1.4 (11) T-N65-CM-SP-006: change from V1.2 to V1.3
193.		12.1.1	CLN65LP(1.2V)	Add “2.5V over-drive 3.3V MOS and 2.5V under-drive 1.8v MOS” into table

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	From Version 2.0 to Version 2.1			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
194.		12.1.4	CLN65GP(1.0V-2.5V)	Revise table
195.		12.1.7	CLN55GP(1.0V-2.5V)	Revise table
196.		12.2.1	1.2V Standard Vt MOS	Revise table
197.		12.2.2	1.2V High Vt MOS	Revise table
198.		12.2.3	1.2V mLow MOS	Revise table
199.		12.2.3	1.2V Low Vt MOS	Revise table
200.		12.2.5	1.8V IO MOS (2.5V underdrive to 1.8V	Refine the title to “2.5V underdrive to 1.8V” and revise table
201.		12.2.6	2.5V IO MOS	Revise table
202.		12.2.7	3.3V IO MOS (2.5V overdrive to 3.3V)	Refine the title to “2.5V overdrive to 3.3V” and revise table
203.		12.2.8	3.3V IO MOS	Add this section (copy from T-N65-CL-SP-040)
204.		12.2.12	2.5/5.5V High Voltage MOS	Revise table
205.		12.4.1	1.0V Standard Vt MOS	Revise table
206.		12.4.2	1.0V High Vt MOS	Revise table
207.		12.4.3	1.0V Low Vt MOS	Revise table
208.		12.4.4	1.8V I/O MOS	Revise table
209.		12.4.5	2.5V I/O MOS	Revise table
210.		12.4.6	1.8V I/O MOS(2.5V underdrive to 1.8V)	Revise table
211.		12.4.7	3.3V I/O MOS(2.5V overdrive to 3.3V)	Revise table
212.		12.4.8	1.0V Native MOS	Revise table
213.		12.4.11	3.3V Native I/O MOS	Add this section (copy from T-N55-CL-SP-041
214.		12.7.4	1.0V Ultra High Vt MOS	Add this section (copy from T-N55-CL-SP-007
215.		12.7.11	3.3V Native MOS	Add this section (copy from T-N55-CL-SP-010
216.		12.7.12	2.5V over drive 3.3V Native MOS	Revise table
217.		12.8.3	1.2V mLow MOS	Remove this section due to no N55LP mLVT offering
218.		12.8.3	1.2V Low Vt MOS	Revise table
219.		12.8.4	1.8V I/O MOS	Revise table
220.		12.8.5	2.5V I/O MOS	Revise table
221.		12.8.6	3.3V I/O MOS	Revise table
222.		12.8.7	2.5V under drive 1.8V I/O MOS	Revise table
223.		12.8.8	2.5V over drive 3.3V I/O MOS	Revise table
224.		12.9.7	CLN55LP	Revise table
225.		12.10.1	CLN65LP	Revise table
226.		12.10.3	CLN65GP	Revise table
227.		12.11.1	CLN65LP	Refine the title
228.		12.11.5	CLN65ULP	Refine the title

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A.1.11 From Version 2.1 to Version 2.2

	From Version 2.1 to Version 2.2			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1		3.1	Mask information, key process sequence, and CAD layer	Refine OD description in table 3.1.1 ~ table 3.1.12
2		3.1	Mask information, key process sequence, and CAD layer	Upadte the mask grade of RPO2 that align with MB
3		3.1	Mask information, key process sequence, and CAD layer	Add new CAD layer LUPWDMY_2 for AAIO latch-up rules check
4		4.2.1	Derived Geometries	1.Refine the definition NW1V and NW2V 2.Turn ON "NW_SUGGESTED" for correct I/O NW space to core or I/O
5	DNW.R.7	4.5.1	Deep N-Well (DNW) Layout Rules (Mask ID: 119) [Optional]	New rule to prevent DNW charge effect
6	NW.R.2^{U}	4.5.3	N-Well (NW) Layout Rules	Add new rule to prevent misuse
7	NT_N.W.2	4.5.6	Native Device (NT_N) Layout Rules	Clarify the description
8	NT_N.W.2.1	4.5.6	Native Device (NT_N) Layout Rules	Clarify the description
9	NT_N.W.2.2	4.5.6	Native Device (NT_N) Layout Rules	Clarify the description
1		4.5.17	N65 HVD_N Layout Rules	Add information. For N55 5V HVMOS, please refer to T-N55-CL-DR-006.
1		4.5.18	N65 HVD_P Layout Rules	Add information. For N55 5V HVMOS, please refer to T-N55-CL-DR-006.
1	Mx.W.3	4.5.29	Mx Layout Rules (Mask ID:380, 381, 384, 385, 386, 387)	Relax rule to add "[except bond pad, if Mx is Mtop-1 layer]"
1	IND.W.4	4.6.8.1	Layout Rules for Inductors with INDDMY Layer	Relax rule
1	IND_MD.W.4	4.6.8.2	Layout Rules for Inductors with INDDMY_MD Layer	Relax rule
1		4.6.9	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Update Mu S/R gds from *N65_Mu_SR_00132007.gds to N65_Mu_SR_03152013.gds.* That only revised the PM pattern. Since PM needs to cover S/R and assembly isolation.
1		4.6.10	Seal-Ring Rule	Update Mu S/R gds from *N65_Mu_SR_00132007.gds to N65_Mu_SR_03152013.gds.* That only revised the PM pattern. Since PM needs to cover S/R and assembly isolation.
1		10.1.2.1	Special Definition in Latch-up Prevention	Add the definition of OD injector, include diode and resistor
1		10.1.2.2.1	SDI Dummy Layer (CAD layer: 122)	Remove the SDI for DRC recognize MOS/ACTIVE which connect to I/O pad
1		10.1.2.3.1	DRC methodology for LUP.1	Refine the description
2		10.1.2.3.2	DRC methodology for LUP.2	Modify Active/MOS to OD injector
2		10.1.2.3.3	DRC methodology for LUP.3	Modify Active/MOS to OD injector
2		10.1.2.3.4	DRC methodology for LUP.4	Modify Active/MOS to OD injector
2		10.1.2.3.5	DRC methodology for LUP.5	Modify Active/MOS to OD injector
2	LUP.1g	10.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify Active to OD injector
2	LUP.2g	10.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify "MOS connectd to an I/O pad" to OD injector
2	LUP.4g	10.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify "MOS connectd to an I/O pad" and "ACTIVE connectd to an I/O pad" to OD injector
2	LUP.5.1.0 LUP.5.2.0 LUP.5.3.0 LUP.5.4.0 LUP.5.5.0	10.1.2.4	Layout Rules and Guidelines for Latch-up Prevention	Modify "MOS connectd to an I/O pad" and "ACTIVE connectd to an I/O pad" to OD injector

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	From Version 2.1 to Version 2.2			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
2		10.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	Add section for area I/O latch-up prevention
2	LUP.10.g	10.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	New rule for AAIO
3	LUP.11.g^{U}	10.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	New rule for AAIO
3	LUP.12.g^{U}	10.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	New rule for AAIO
3	LUP.13.g	10.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	New rule for AAIO
3	LUP.14.g	10.1.2.5	Layout Rules and Guidelines for Area I/O Latch-up Prevention	New rule for AAIO
3		11.3.3	DC Cu Metal Current Density (EM) Speifications	Refine the description for N65/N55.
3		12.1.1	CLN65LP (1.2V)	Align with spice table for 3.3V MOS and 3.3V Native MOS
3		12.1.8	CLN55LP (1.2V)	Align with spice table for 1.8V MOS and 2.50V_under-drive 1.8V MOS (revise min. length from 0.252 to 0.234)

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A.1.12 From Version 2.2 to Version 2.3

	From Version 2.2 to Version 2.3			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.		4.5.36.1	RTMOM (Rotated Metal Oxide Metal) Capacitor Guidelines	Modify CAD layer number and description
2.	CSR.EN.6.1	4.5.43	Chip Corner Stress Relief Pattern (CSR)	Modify description
3.	CSR.EN.6.2	4.5.43	Chip Corner Stress Relief Pattern (CSR)	Add new rule
4.		4.5.44.1	WLCSP Seal Ring Layout Rules	Add new chapter
5.	CSR.EN.10.1	4.6.9	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Modify description
6.	CSR.EN.10.2	4.6.9	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Add new rule

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A.2 Revision History of T-N65-CM-DR-001 (MS_RF)

A.2.1 New (Version 0.1): only for Mu and MIM

A.2.2 From Version 0.1 to Version 0.2

	From Version 0.1 to Version 0.2			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.		1.1	Overview	Modifies wording
2.		1.2	Related Documentation	Adds new documents
3.		1.3.1	Design Recommendations for Yield and reliability	Modifies wording
4.		2.1	Semiconductor Process Features for MS/RF Devices	Renames UTM as Mu and Inductor Via as Vu.
5.		2.2	Metallization Options	Modifies terminology.
6.		2.2.1	Metallization Option Tables	Renames UTM as Mu and Inductor Via as Vu. Modifies Note 1~5 to note 1~3.
7.		3.2	Special Layer Summary	Corrects typing error and adds new special layers for MiM.
8.		3.3	Device Truth Table	Deletes truth table and add comment to refer to corresponding section of both MiM and Inductor offering.
9.		4.2	Derived Geometries Used in Physical Design Rules	Unifies Table 4.2.1 terminology.
10.		4.3	Minimum Pitches	Renames UTM9 to Mu
11.		4.4	Layout Rules and Guidelines	Re-organizes the contents
12.		4.4.1	MiM Capacitor Scheme Recommendations	New adds section
13.		4.4.2	MiM Capacitor PDK Guideline	New adds Section of “MIM capacitor PDK Guideline”
14.		4.4.3	Capacitor Top Metal (CTM) Layout Rules (182)	Modifies the description.
15.	CTM.R.2^{U}®	4.4.3		Adds un-checkable mark and refines the wording.
16.	CTM.R.3^{U}	4.4.3		Refines the wording.
17.	CTM.R.4	4.4.3		New adds rule
18.		4.4.4	Capacitor Bottom Metal (CBM) Layout Rules (183)	Modifies the description.
19.	CBM.W.3	4.4.4		Includes dummy pattern for check
20.	CBM.W.5	4.4.4		Renames UTM to Mu
21.	CBM.S.3	4.4.4		Includes dummy pattern for check
22.	CBM.S.7	4.4.4		Renames UTM to Mu
23.	CBM.R.3^{U}	4.4.4		Refines the wording
24.	Note1~4	4.4.4		Modifies and resorts note1~4
25.		4.4.5	Antenna Effect Prevention Design Rules for MIM Capacitor	Adds section of “Antenna Effect Prevention Design Rules For MIM capacitor”.
26.		4.4.6	Inductor Guidelines	Adds section of “Inductor Guideline”.
27.		4.4.7	Ultra Thick Metal (Mu) Layout Rules (389)	Renames UTM to Mu for all rules. And separates inductor related rule to section 4.4.8.
28.		4.4.7	Ultra Thick Metal (Mu) Layout Rules (389)	Renames UTM to Mu for all rules. And separates inductor related rule to section 4.4.8.
29.		4.4.8		Adds section of “Inductor Layout Rules”
30.		4.4.9		Adds section of “Chip Corner Stress Relief Pattern (CSR)”.
31.		4.4.10		Adds section of “Seal-Ring Rule” is added.

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A.2.3 From Version 0.2 to Version 1.0

	Version 0.2 to Version 1.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.		1	Introduction	Adds the description and modifies some wordings
2.		1.1	Overview	Adds the description and modifies some wordings
3.		1.2	Related Documentation	Adds the description
4.		1.2	Related Documentation	Updates the reference documents information in Table 1.2.1
5.		1.3	User Guidelines	Adds the description and modifies some wordings
6.		1.3.1	Design Recommendations for Yield, Performance and Reliability	1. Modifies the section title 2. Adds the description and modifies some wordings
7.		2	Technology Overview	Modifies some wordings
8.		2.1	Additional Semiconductor Process Features for MS/RF Devices	Adds the description and modifies some wordings
9.		2.2	Available Metallization Options for MS/RF Design	1. Modifies the section title 2. Adds the description and modifies some wordings
10.		2.2.1	Metallization Option Tables	1. Modifies the section title 2. Delete a table with information similar to Table 2.2.1
11.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Correct the Digitized Area type from “Dark” to “Clear” for Mask ID “118” in Table 3.1.1
12.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Correct the Mask ID of OD2 layer as “152” in Table 3.1.1
13.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Modifies the description for optional CTM and CBM layers in Table 3.1.1
14.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Modifies the layer “395” (FW-Cu) description in Table 3.1.1
15.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Adds the layer “30A” (FW-Al) into Table 3.1.1
16.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Adds the optional cell implantation layer “199” into Table 3.1.1
17.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Correct the Mask Name of OD2 layer as “152” in Table 3.1.2
18.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Correct the Mask Grade of PO layer as “L” in Table 3.1.2
19.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Modifies the Mask Grade, Mask Type, OPC and PSM of layers as ‘TBD” in Table 3.1.2. The modified layers include Mask ID of 379, 381, 373, 384, 374, 385, 375, 386, 376, 387, 377, 388, 372 and 389.
20.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Modifies the Mask Name for layer “395” as “FW-Cu” in Table 3.1.2
21.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Adds the layer “30A” (FW-Al) into Table 3.1.2
22.		3.1	Reserved Mask Names and IDs, Key Process Sequence, and CAD Layers	Adds the optional cell implantation layer “199” into Table 3.1.2
23.		3.2	Special Layer Summary	Modifies some wordings
24.		3.2	Special Layer Summary	Modifies the Table 3.3.1 as Table 3.2.1
25.		3.2	Special Layer Summary	Modifies the description of INDDMY layer in Table 3.2.1
26.		3.3	Device Truth Table	Modifies some wordings
27.		4.2	Derived Geometrical Definitions Used in Physical Design Rules	1. Modifies the section title 2. Modifies the description of Vcap in Table 4.2.1 3. Modifies some wordings
28.		4.4	Layout Rules and Guidelines	Adds the section of “RTMOM (Rotate Metal Oxide Metal) Capacitor Guidelines” into section 4.4.6
29.		4.4	Layout Rules and Guidelines	Modifies the title of section 4.4.9
30.		4.4.1	MIM Capacitor Scheme	Modifies the description

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	Version 0.2 to Version 1.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
			Recommendations	
31.		4.4.2	MIM Capacitor PDK Guideline	Modifies the description
32.		4.4.2	MIM Capacitor PDK Guideline	Modifies the Table 4.4.2.2 and the table title
33.		4.4.2	MIM Capacitor PDK Guideline	Modifies the Table 4.4.2.3
34.		4.4.2	MIM Capacitor PDK Guideline	Modifies metal layer and via naming for MIM structures in Figure 4.4.2.1
35.		4.4.2	MIM Capacitor PDK Guideline	Modifies the Table 4.4.2.4 title
36.	Table 4.4.2.4	4.4.2	MIM Capacitor PDK Guideline	Correct the Spice and PDK offering status of MIM directly under Mu in Table 4.4.2.4
37.	CTM.EN.1 CTM.S.2 CTM.R.1 CTM.S.3 CTM.R.2^{U} CTM.R.3^{U}	4.4.3 and 4.4.3.1	Capacitor Top Metal (CTM) Layout Rules (182) Vcap(Vz or Vu) and Mcap(Mz or Mu) Layout Rules Associated to CTM(182)	Renames to Vcap.EN.1 Renames to Vcap.S.1 Deletes. Renames to Vcap.S.2 Renames to Vcap.R.1^{U} Renames to Mcap.R.1^{U}
38.	Title CBM.EN.1 CBM.DN.1 CBM.DN.2 CBM.S.2 CBM.W.3 CBM.W.5 CBM.S.3 CBM.S.7 CBM.S.4 CBM.EN.3 CBM.R.1	4.4.4 and 4.4.4.1	Capacitor Bottom Metal (CBM) Layout Rules (183) Vcap(Vz or Vu) and Mcap(Mz or Mu) Layout Rules Associated to CBM(183)	Modifies the description Renames to Vcap.EN.2 Renames to Mcap.DN.1 Renames to Mcap.DN.2 Renames to Vcap.S.3 Renames to Mcap.W.1 Renames to Mcap.W.2 Renames to Mcap.S.1 Renames to Mcap.S.2 Renames to Mcap.S.3 Renames to Vcap.EN.3 Renames to Vcap.R.2
39.	Note 2 & 4	4.4.4	Capacitor Bottom Metal (CBM) Layout Rules (183)	Modifies some wordings in Note 2 & 4
40.		4.4.5	Antenna Effect Prevention Design Rules for MIM Capacitor	Modifies the description and some wordings
41.		4.4.5	Antenna Effect Prevention Design Rules for MIM Capacitor	Modifies the Table 4.4.5.1
42.		4.4.5	Antenna Effect Prevention Design Rules for MIM Capacitor	Modifies the definition of “Floating” and “Connected” in Terminology table
43.		4.4.5	Antenna Effect Prevention Design Rules for MIM Capacitor	Modifies the Figure 4.4.5.1 and 4.4.5.2 for “Balanced” and “Unbalanced” structure illustrations
44.	A.R.MIM.3 & A.R.MIM.5	4.4.5	Antenna Effect Prevention Design Rules for MIM Capacitor	Modifies the defined diode area
45.		4.4.6	RTMOM (Rotate Metal Oxide Metal) Capacitor Guidelines	Adds the section of “RTMOM (Rotate Metal Oxide Metal) Capacitor Guidelines”
46.		4.4.7	Inductor Guidelines	Modifies some wordings
47.		4.4.7.1	Introduction to PDK Inductor	Modifies the description in item 5
48.		4.4.7.1	Introduction to PDK Inductor	Modifies the description of Note3 in Table 4.4.7.2
49.		4.4.7.1	Introduction to PDK Inductor	Modifies the description of “GDIS” in Table 4.4.7.3
50.	Mu.W.2	4.4.8	Ultra Thick Metal (Mu) Layout Rules (389)	Modifies the description of rule “Mu.W.2”
51.		4.4.8	Ultra Thick Metal (Mu) Layout Rules (389)	Modifies the wordings in Guideline 2
52.		4.4.9	Layout Rules for Inductors with INDDMY Layer	Modifies some wordings
53.	IND.W.4	4.4.9	Layout Rules for Inductors with INDDMY Layer	Modifies the description
54.	IND.W.5	4.4.9	Layout Rules for Inductors with INDDMY Layer	Modifies the description
55.	IND.R.9^{U}	4.4.9	Layout Rules for Inductors with INDDMY Layer	Deletes the rule “IND.R.9^{U}”
56.	IND.R.10	4.4.9	Layout Rules for Inductors with INDDMY Layer	Deletes the rule “IND.R.10”
57.	IND.DN.2	4.4.9	Layout Rules for Inductors with INDDMY Layer	Deletes the rule “IND.DN.2”
58.	IND.DN.3	4.4.9	Layout Rules for Inductors with INDDMY Layer	Deletes the rule “IND.DN.3”
59.	IND.R.11^{U}	4.4.9	Layout Rules for Inductors with INDDMY Layer	Deletes the rule “IND.R.11^{U}”

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	Version 0.2 to Version 1.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
60.	IND.R.12	4.4.9	Layout Rules for Inductors with INDDMY Layer	Deletes the rule “IND.R.12”
61.	IND.DN.4	4.4.9	Layout Rules for Inductors with INDDMY Layer	Deletes the rule “IND.DN.4”
62.	IND.DN.5	4.4.9	Layout Rules for Inductors with INDDMY Layer	Deletes the rule “IND.DN.5”
63.	IND.DN.7	4.4.9	Layout Rules for Inductors with INDDMY Layer	Adds the exclusive checking condition by adding “except Mz which is used as top metal layer”
64.	IND.DN.8	4.4.9	Layout Rules for Inductors with INDDMY Layer	Adds the exclusive checking condition by adding “except Mz which is used as top metal layer”
65.	Note 10	4.4.9	Layout Rules for Inductors with INDDMY Layer	Modifies the description in Note 10
66.		4.4.9	Layout Rules for Inductors with INDDMY Layer	Modifies the INDDMY location, width of region “b” & ”d” and “IND.R.8” illustration in lower plot of Figure 4.4.9
67.	CSR.EN.6	4.4.10	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Modifies the wordings
68.		4.4.10.1	Metallization Options Using Mu as the Top Metal	Corrects the “Mz” as “Mu” in the section title and table
69.		4.4.10.1	Metallization Options Using Mu as the Top Metal	Modifies the description
70.		4.4.11	Seal-Ring Rule	Modifies the description

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12/16/2016

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A.2.4 Rule Mapping from MS_RF Rule to Logic Rule

This following rule mapping table lists the change from N65 MS_RF design rule(T-N65-CM-DR-001, V1.0) and N65 Logic design rule(T-N65-CL-DR-001, V1.4)

MS_RF Ver.1.0	Logic Ver.1.4
CTM Rules	
CTM.W.1	CTM.W.1
CTM.W.2	CTM.W.2
CTM.S.1	CTM.S.1
CTM.EN.1	CTM.EN.1
CTM.R.1	CTM.R.1
-	CTM.R.2
CBM Rules	
CBM.W.1	CBM.W.1
CBM.W.2	CBM.W.2
CBM.EN.2	CBM.EN.2
CBM.S.1	CBM.S.1
CBM.S.2	CBM.S.2
CBM.R.1	CBM.R.1
CBM.R.2g^{U}	CBM.R.2g^{U}
CBM.S.3	CBM.S.3
VIAz/VIAu Rules	
Vcap.EN.1	VIAz(u).EN.3
Vcap.EN.2	VIAz(u).EN.4
Vcap.S.1	VIAz(u).S.3
Vcap.S.2	VIAz(u).S.4
Vcap.S.3	VIAz(u).S.5
Vcap.R.1^{U}	VIAz(u).R.6g^{U}
Mcap.R.1^{U}	remove
Vcap.R.2	VIAz(u).R.7
Mu.EN.3	VIAu.EN.5
Mu.R.1	VIAu.R.8
Mz Rules	
Vcap.EN.3	Mz.EN.3
Mcap.DN.1	Mz.DN.5
Mcap.DN.2	Mu.DN.3
Mcap.W.1	Mz.W.4
Mcap.W.2	remove
Mcap.S.1	Mz.S.4

MS_RF Ver.1.0	Logic Ver.1.4
Mz Rules	
Mcap.S.2	remove
Mcap.S.3	remove
Mu Rules	
Mu.W.1	Mu.W.1
Mu.W.2	Mu.W.2
Mu.W.3	Mu.W.3
Mu.S.1	Mu.S.1
Mu.EN.1	Mu.EN.1
Mu.A.1	Mu.A.1
Mu.A.2	Mu.A.2
Mu.R.2 ^{U}	Mu.R.2 ^{U}
Mu.R.3	remove
Mu.DN.1	Mu.DN.1
Mu.DN.2	Mu.DN.2
INDDMY Rules	
IND.W.1	IND.W.1
IND.W.2	IND.W.2
IND.W.3	IND.W.3
IND.W.4	IND.W.4
IND.W.5	IND.W.5
IND.W.6	IND.W.6
IND.W.7	IND.W.7
IND.S.1	IND.S.1
IND.S.2	IND.S.2
IND.S.3	IND.S.3
IND.S.4	IND.S.4
IND.S.5	IND.S.5
IND.R.1	IND.R.1
IND.R.2	IND.R.2
IND.R.3	IND.R.3
IND.R.4	IND.R.4
IND.R.5^{U}	IND.R.5^{U}

MS_RF Ver.1.0	Logic Ver.1.4
INDDMY Rules	
IND.R.6	IND.R.6
IND.R.7^{U}	IND.R.7^{U}
IND.R.8	IND.R.8
IND.DN.1	IND.DN.1
IND.R.13	IND.R.13
-	IND.R.14
IND.DN.6	IND.DN.6
IND.DN.7	IND.DN.7
IND.DN.8	IND.DN.8
IND.DN.9	IND.DN.9
IND.DN.10	remove
CSR Rules	
CSR.EN.6	CSR.EN.6
Seal ring Rules	
VIAu.W.2	VIAu.W.2

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A.3 Revision History of T-N55-CL-DR-001 (N55 Logic)

A.3.1 From Version 0.1 to Version 0.2

	Version 0.1 to Version 0.2			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.		2.2	Power Supply and Operation Temperature Ranges	Modifies Table 2.2.1
2.		2.4	Reserved mask name and ID, Key process sequence, and CAD layer	Modifies Table2.4.1, Table2.4.2, Table2.4.3
3.		2.4	Reserved mask name and ID, Key process sequence, and CAD layer	Modifies Table 2.4.4, Mask Name/ID/Grade/Type, OPC, and PSM Information
4.		2.5	Special Layer Summary	Adds SRAMDMY_1 for tape-out if N55 SRAM Cell is used.
5.	DNW.S.1	3.2.2.1	Non-shrinkable Rules	Deletes the rule.
6.	DNW.S.2	3.2.2.1	Non-shrinkable Rules	Deletes the rule.
7.	NW.A.1	3.2.2.1	Non-shrinkable Rules	Deletes the rule.
8.	NW.A.2	3.2.2.1	Non-shrinkable Rules	Deletes the rule
9.	NT_N.S.2	3.2.2.1	Non-shrinkable Rules	Deletes the rule.
10.	NT_N.S.3	3.2.2.1	Non-shrinkable Rules	Deletes the rule.
11.	NT_N.A.1	3.2.2.1	Non-shrinkable Rules	Deletes the rule.
12.	NT_N.A.2	3.2.2.1	Non-shrinkable Rules	Deletes the rule
13.	OD25_33.W.1	3.2.2.1	Non-shrinkable Rules	Adds the rule
14.	OD25_33.W.1	3.2.2.1	Non-shrinkable Rules	Adds the rule
15.	SRAM.R.15			Modifies DRC
16.	SRAM.R.18	3.2.2.4	SRAM Rules	Adds the rule
17.		4	Design Flow For Tape-Out	Modifies some wordings.

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A.3.2 From Version 0.2 to Version 1.0

	Version 0.2 to Version 1.0			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.		1.1	Overview	Modifies some wordings.
2.		1.2	Related Design Rule Manuals And Documents	Adds metal fuse rule
3.		1.3.2	SRAM Design Specifications	Deletes LP selection
4.		2.1	Devices	Modifies Table 2.1.1
5.		2.2	Power Supply and Operation Temperature Ranges	Modifies Table 2.2.1
6.		2.3	Metallization Options	Modifies Table 2.3.1
7.		2.3	Metallization Options	Modifies Table 2.3.2
8.		2.3	Metallization Options	Adds Table 2.3.5
9.		2.3	Metallization Options	Modifies Table 2.3.6
10.		2.4	Reserved mask name and ID, Key process sequence, and CAD layer	Modifies Table 2.4.2, CLN55G+2.5V
11.		2.4	Reserved mask name and ID, Key process sequence, and CAD layer	Deletes Table 2.4.3, CLN55LP2.5V
12.		2.4	Reserved mask name and ID, Key process sequence, and CAD layer	Modifies Table 2.4.4, Mask Name/ID/Grade/Type, OPC, and PSM Information
13.		2.5.1	Special Layer Summary	Adds OD25_33 special layer
14.		2.6.2	Low Power (LP): 1.2V Core Design	Deletes Table 2.6.3
15.	NT_N.W.2	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
16.	NT_N.W.2.1	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
17.	NT_N.W.2.2	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
18.	NT_N.W.3	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
19.	NT_N.W.4	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
20.	NT_N.W.5	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
21.	NT_N.EN.1	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
22.	PO.W.2	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
23.	PO.W.4	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
24.	OD25_33.W.1	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
25.	OD25_33.W.2	3.2.2.1	Non-shrinkable Rules of General Logic Rules	Deletes this rule
26.		3.2.2.2	Recommended Non-shrinkable Rules of General Logic Rules	Deletes this section
27.	SRAM.R.15	3.2.2.2	SRAM Rules of General Logic Rules	Adds this rule
28.	# UBM.EN.1	3.2.4	Non-shrinkable Rules of Flip Chip Bump Rules	Deletes this rule
29.	#UBM.EN.2	3.2.4	Non-shrinkable Rules of Flip Chip Bump Rules	Changes the rule from “2.3” to “2.2”.
30.	#BP.W.4	3.2.4	Non-shrinkable Rules of Flip Chip Bump Rules	Deletes this rule
31.	#BP.EN.5	3.2.4	Non-shrinkable Rules of Flip Chip Bump Rules	Changes the rule from “11.2” to “11.0”.
32.		3.2.5	AP Metal Fuse Rules	Adds this section
33.		4.1	How to shrink the existing CLN65 design	Deletes LP selection

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A.4 Revision History of T-000-CL-DR-002 (Pad)

A.4.1 Change from Each Document to Version 1.0

A.4.1.1 Merged from Design Rule Documents

Version 2.0 includes rules that were merged from the following Design Rule documents:

- *T-000-LO-DR-001: TSMC AL BOND PAD DESIGN RULE FOR WIRE BOND (Ver.2.3)*
- *T-000-LO-DR-004: TSMC CU BOND PAD DESIGN RULE FOR WIRE BOND (Ver.0.3)*
- *T-000-FC-DR-001: TSMC FLIP CHIP BOND PAD DESIGN RULE FOR AL PAD (Ver.2.1)*
- *T-000-FC-DR-002: TSMC FLIP CHIP BOND PAD DESIGN RULE FOR CU PAD (Ver.1.2)*
- *T-000-LO-DR-002: REDISTRIBUTION FOR SOLDER BUMP DESIGN RULE (Ver.0.4)*
- *T-000-FC-DR-003: TSMC POST PASSIVATION INTERCONNECTION (PPI) FOR SOLDER BUMP DESIGN RULE (Ver.0.2)*
- *T-000-LO-DR-005: TSMC CMOS LOGIC GENERAL PURPOSE COPPER INTERCONNECTION DESIGN RULE FOR FLIP CHIP (Ver.0.1)*

T-000-FC-DR-004: TSMC AL INTERCONNECT DESIGN RULE FOR FLIP CHIP (0.15/0.18/0.22/0.25UM) (Ver.0.1)

A.4.1.2 Rule Changes from Pre-merged Document to this Version 1.0 Merged Document

T-000-LO-DR-001 (Ver.2.3)

Rule	Revision
CB	Added CB structure rules of CL022 (via and metal rules)
CB.EN.1	Revised CB.EN.1 from M1/M2 to M1~Mtop-3.
CB.R.1:	Changed the pattern of notch (50 µm pitch) and the length of probing area from 60 µm to 50 µm.
CB.W.1	Changed 48 µm to 43 µm for BGA and from 53 µm to 48 µm for non-BGA.
CB.W.3	• Changed M1/M2 to M1~Mtop-3 and 50. • Added 50 µm for 80 µm pitch staggered.
Double bonds	Added wording that double bonds are for QFP only.
Pitch (50 µm)	Merged 50 µm pitch rules (43 µm* 80 µm) with the CB rule for BGA.
PM.R.3	Revised PM.R.3 and removed the PM logical operation.
Staggered	Changed inner/out tier of staggered to inner/outer pad.
Tri-Tier	Changed first/second/third tier of Tri-Tier to inner/middle/outer pad.

T-000-LO-DR-004 (Ver.0.3)

Rule	Revision
CB.EN.1	Revised CB.EN.1 from M1/M2 to M2~Mtop-3.
CB.R.1/CB.W.3	Added rules.
CB.S.1	Add CB.S.1= 9 µm.for 50µm and 55µm pitch
CB.W.1	Add CB.W.1= 46 µm of 55µm pitch for all packages and = 41 µm of 50µm pitch for BGA only.
CBVIAT.EN.2	Revised CBVIAT.EN.2 from Mtop-1 to Mtop-1/Mtop (for CL013) and Mtop-2/Mtop-1/Mtop for (CN90).
Staggered	Revised from inner/outer tier of staggered to inner/outer pad. Added rules for pitch staggered (70 µm).
Tri-Tier	Added rules for pitch tri-tier (80 µm.

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T-000-FC-DR-001 (Ver2.0)

Rule	Revision
BP.EN.3	Revised BP.EN.3 from 2 μm to 12 μm.
UBM.R.2	Revised the wording for UBM.R.2.
UBM.DN.1	Added rule.
UBM.EN.3	Revised UBM.EN.3 from 160 μm (from the center of the scribe lane) to 100 μm (from the chip edge).

T-000-FC-DR-002 (Ver.1.2)

Rule	Revision
BP.S.3/BP.S.4	Removed space between two AP (BP.S.3 and BP.S.4).
UBM.DN.1	Added rule.
UBM.EN.3	Revised UBM.EN.3 from 160 μm (from the center of the scribe lane) to 100 μm (from the chip edge).
UBM.R.2	Revised the wording for UBM.R.2.

T-000-LO-DR-002 (Ver.0.4)

Rule	Revision
Rule writing style	Revised the rule writing style to refer to the top VIA and the top metal rule of each generation's design rule.
VIAD.R.2 (Al)	Revised VIAD.R.2 (A1) from 400 to 200.

T-000-FC-DR-003 (Ver0.2)

Rule	Revision
Application process	Revised the application process from both Cu and Al processes to the Al process only.
CB.S.4	Added rule.

T-000-LO-DR-005 (Ver.1.0)

Rule	Revision
BP.R.7	Removed rule BP.R.7.
UBM.EN.1	Revised UBM.EN.1 from 120 μm (space to center of scribe lane) to 100 μm (enclosure by chip edge).

T-000-FC-DR-004 (Ver.0.1)

Rule	Revision
BP.R.7	Removed rule BP.R.7.
BP.R.9	Revised BP.R.9 from 170 μm (space to center of scribe lane) to 110 μm (space to chip edge).
UBM.EN.1	Revised UBM.EN.1 from 120 μm (space to center of scribe lane) to 100 μm (enclosure by chip edge).

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A.4.2 Change from Version 1.0 to 1.1

New

	New rules (Version 1.0 to 1.1)	Description
1	New bump pad pitch rules (150~175μm) for Al and Cu process	Add new rules of UBM, CBD, PM, bump diameter, and bump height for 150 ~ 175μm pitch
2	BP.EN.4 for Al process	Add this rule of “PM enclosure by CBD region”
3	Mechanical and Thermal guidelines for FCBGA	Add new packaging guideline for CL013 and beyond technologies.
4	1.1 OVERVIEW	Add the wordings of ” The pad pitch and packaging technology ...”
5	2.2 Flip Chip Guideline	Add “ 3. For bump pad pitch selection:…”
6	2.5 Non-shrinkable Guidelines for Shrinkage Technologies	For easier use by the designer who wants to use the TSMC shrinkage technologies
7	PM.W.2	Add this rule for the polyimide window opening on non-CB region
8	4.7 Non-shrinkable Rule For Shrinkable Technologies	For easier use by the designer who wants to use the TSMC shrinkage technologies
9	Add the seal ring cross section on section 4.6.1 and section 4.6.2	Insert the MD/PPI layer into the seal ring cross-section

Modified

	Modified rules (Version 1.0 to 1.1)	Description
1	UBM.P.1	Modify from 175μm to 150μm
2	CB.W.2	Modify from “width” to “length”
3	BP.W.4	Add “… under UBM area”
4	The bump height and diameter in Table1 & Table2	Simplify the bump height and diameter information
5	BP.EN.2 for Al process	Add the description “without polyimide process only”
6	CB.EN.1	Remark this rule at section 4.4.2.
7	2.3 Redistribution Interconnection Guidelines 4. I/O ESD protection recommendations:	Modify “The minimum bus line width is 20μm.” to The minimum total bus line width is 20μm.
8	1.1 OVERVIEW	Modify the wordings of “is only applied…” to “is verified by…”
9	Modify the description using “Mil” unit	Add “μm” in front of “Mil”
10	PM.W.1	Specify this rule using on PM opening on CB region.
11	PPI.S.3	Relax from 30μm to 5μm
12	Modify CB.EN.1 for Cu process	Relax this rule from 2μm to 1.5μm
13	BP.EN.2	Add”…. (Without Polyimide process only”
14	Modify “*” mark for DRC can’t check	Change from “#” to “u”

Deleted

	Deleted rule (Version 1.0 to 1.1)	Description
1	60 μm pitch for single in-line Cu pad	Delete the rules of this pitch due to no impact on TSMC IO library.

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A.4.3 Change from Version 1.1 to 1.2

New

	New rules (Version 1.1 to 1.2)	Description
1.	Add CLN65 relative wire bond and flip chip design rules	1. Wire bond pad structure need have new rules. 2. Flip chip rules are same with CLN90 low-K
2	#CB.S.3 [t]	Space of the different pad geometries [(Single to Stagger), (Single to Tri-tier) or (Stagger to Tri-tier)]
3	CB.W.1/CB.S.1 for dual passivation	Relax CB.W.1/CB.S.1 to 44/6um(50um pitch) and 49/6um (60um pitch) for dual passivation only
4	60um pitch staggered rule	CB.W.1/CB.W.2/CB.S.1=50/66/10um .CB.W.1/CB.S.1 will be set as non-shrinkable.
5	UBM.S.4®	Recommended maximum space between two UBM
6	UBM.R.5	At least one bump has to be placed near, and as close as possible, to the chip corner.
7	UBM.R.5®	It's recommended not to place the IO bump pads on 2nd and 3rd row on bump array corners, but instead to put Vss, Vdd or dummy bump pads.
8	UBM.EN.1g	Recommended enclosure by chip edge (Maximum)
9	UBM.R.4g	• It is recommended not to put any bump on the top of SRAM area and the matching pairs. The circuits should be located at a minimum distance of 60 µm from the bump pad's PM or CBD edge. It's also recommended to consider UBM.S.4® at the same time. If bump over SRAM area is needed, it's recommended to use the ultra-low alpha particle materials during the bump and assembly processes (solder bump, under-fill, pre-solder bump…) to avoid high Soft Error Rate (SER). TSMC uses ultra-low alpha particle materials in the solder bump process. If a customer couldn't meet UBM.S.4® and UBM.R.4g at the same time, you can consult TSMC for layout suggestion.
10	#BP.S.1 [t]	PM space to AP-MD [PM on AP is prohibited, except UBM region and seal ring] (CL013 FSG with Al PPI)
11	BP.EN.8 [t]	PM enclosure by UBM (CL013 FSG with Al PPI)
12	BP.R.1 [t]	CB2 on AP-MD for interconnection is prohibited [except UBM and sealring]
13	CB-VD and AP-MD rules for Al PPI for CL013/CLN90 Cu process flip chip design	
	CB.W.1	Width (maximum =minimum) {Not inside seal ring}
	CB.S.1	Space
	CB.EN.1	Enclosure by MT {Not inside seal ring}
	CB.R.1	A 45-degree rotated CB-VD is prohibited
	AP.W.1	Width {Interconnection only} {Not inside UBM or seal ring}
	AP.S.1	Space
	AP.S.2	Space to FW
	AP.S.3	Space to LMARK
	AP.S.4	Space to CB2/PM
	AP.EN.1	Enclosure of CB-VD {Not inside seal ring}
	AP.DN.1	AP density across full chip
	AP.W.2®[U]	Recommended total width of BUS line [Connect with bump pad]
14	Add Sec. 2.1 wire bond guideline item 2	Pad Geometries selection
15	Add Sec. 2.1 wire bond guideline item 3	Pad pitch and size.
16	Add Sec. 2.2 Flip chip guideline item 6	Add new Polyimide guideline

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Modified

	Modified rules (Version 1.1 to 1.2)	Description
1	#UBM.S.1 [t]	Space to metal fuse protection ring (change from 60 to 50um)
2	UBM.S.3 [t]	Space to L target (for Cu process only) (change from 90 to 80um)
3	Non-shrinkable rule of CB.W.2 of 55um pitch single	Change from 72u.6um to 66um.
4	Non-shrinkable of UBM.S.1	Change from 66 to 55um
5	Non-shrinkable of UBM.S.3	Change form 99 to 88um
6	Sec. 2.2 Flip chip guideline item 7	Modify this process sequence table and add Al PPI(AP-MD)
7	Sec. 2.2 Flip chip guideline item 9	Modify the alpha particle sensitive area and forbidden SRAM area ,except use ultra-low alpha particle material

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A.4.4 Change from Version 1.2 to 1.3

	From Version 1.2 to Version 1.3			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
1.	Consolidate C015/C018 (T-000-CL-DR-001) and C013 CUP design rule (T-013-CL-DR-005)	2.1.2	Circuit Under Pad (CUP) Recommendations	Recommendations for CUP
		3.2	Special Recognition CAD Layers	Add WBDMY to cover CUP pad
		4.4	Pad Pitch Rules for Wire Bond	Add CUP relative descriptions in the current rules (CB.W.3/CB.S.2/CB.EN.1)
		4.6.2	Circuit Under Pad (CUP) Pad structure rules (for C015/C018 only)	Merge all rules from T-000-CL-DR-001
		4.7.2	Circuit Under Pad (CUP) Pad structure rules (for C013 only)	Merge all rules from T-013-CL-DR-005
2.	Add RV and AP-MD rule for C013/N90/N65 wire bond application	3.1	Mask Information, Process Sequence and CAD layers	Add the process sequence of AP-MD with dual passivation scheme on C013 and below technologies
		3.2	Special Recognition CAD Layers	Add RV, AP-MD and CB2 for AP RDL application
		4.4	Pad Pitch Rules for Wire Bond	Add AP-MD and CB2 relative descriptions in the current rules (CB.W.1/CB.W.2/CB.W.3/CB.S.1 /CB.S.2/CB.EN.1/CB.R.1)
		4.7	Wire Bond Pad Structure Rules for Cu Process	Add AP-MD and CB2 relative descriptions in the current rules (CB.R.5/CB.R.6/CBVIAx.R.3/ CBVIAx.R.3.1)
		4.8	RV And AP-MD Layout Rules for Wire Bond	Add RV and AP-MD rules for wire bond
		5.2	Polyimide Window (PM) Rules for Flip Chip	Add AP-MD and CB2 relative descriptions in PM.W.2
3.	Item 5: Required bumping testing flow	2.2	Recommendations for Flip Chip Application	Change “Suggested bumping and testing flow… to “Required bumping and testing flow…”
4.	Mask layer, Process Sequence Table	3.1	Mask Information, Process Sequence and CAD layers	Modify the table and separate the tables of “Al process,” “C013 single passivation,” C013/CN90 dual passivation,” and “CN65 dual passivation”
5.	60um pitch staggered pad rules	4.4	Pad Pitch Rules for Wire Bond	CN90/CN65 dual passivation and Al process single passsivation share the same rules and separated with C013.
6.	70um and 80um pitch staggered pad rules	4.4	Pad Pitch Rules for Wire Bond	Change to become the recommended rules
7.	PM.R.1/PM.R.2	4.5	Polyimide Window (PM) Rules for Wire Bond	Add “ (Al process only)”
8.	CBVIAx.R.1	4.6.1	Wire Bond Pad Structures Rules For Al Process	Modify the description to except the regions of CBVIAx.R.1.1
9.	CBVIAx.R.1.1	4.6.1	Wire Bond Pad Structures Rules For Al Process	Add this new rule for “Ratio of total exposure area of {VIA1~VIAtop-2 INSIDE CB} to CB area (In the inter row pad of staggered and the inter/middle row pad of Tri-tier)”
10.	CBVIAx.R.3	4.7.1	Wire Bond Pad Structures Rules For Al Process	Modify the description to except the regions of CBVIAx.R.3.1
11.	CBVIAx.R.3.1	4.7.1	Wire Bond Pad Structures Rules For Al Process	Add this new rule for “Ratio of total exposure area of {VIA1~VIAtop-2 INSIDE CB} to CB area (In the inter row pad of staggered and the inter/middle row pad of Tri-tier)”
12.	CN90(2XTM)/CN65(2XTM)/CN65(VIAy) rules	4.7.1	Wire Bond Pad Structures Rules For Al Process	Add new rules for CN90(2XTM)/CN65(2XTM)/ CN65 (VIAy) processes
13.	UBM.R.3	5.1	Under Bump Metallurgy (UBM) Rules	Add the required layers for the bump ball structure of different processes
14.	UBM.R.5®	5.1	Under Bump Metallurgy (UBM) Rules	Rename to UBM.R.5g
15.	UBM.R.6®	5.1	Under Bump Metallurgy (UBM) Rules	New guideline for the size ratio of UBM/Pre-Solder Bump SRO (=C/S) and BGA SRO/Board Pad (=T/O) = 1.0~1.1
16.	UBM.EN.1g	5.1	Under Bump Metallurgy (UBM) Rules	Rename to UBM.EN.1®
17.	BP.S.1	5.4	Bump Pad Structure Rules For Cu Process	Deleted this rule and replaced by AP.S.4
18.	BP.EN.7	5.4	Bump Pad Structure Rules For Cu Process	Relax the number from 15um to 2um.
19.	BP.EN.8	5.4	Bump Pad Structure Rules For Cu Process	Deleted this rule due to Single pass+PM scheme is prohibited for AP RDL process
20.	Rename all rules	5.5.2.1	RV Layout Rules (Passivation-1 VIA hole)	Rename CB.W.5/CB.S.3/CB.S.4/CB.EN.3 to RV.W.2/RV.S.1/RV.S.2/RV.EN.2
21.	RV.W.2	5.5.2.1	RV Layout Rules (Passivation-1 VIA hole)	Relax from >=25um to =5um
22.	RV.S.1	5.5.2.1	RV Layout Rules (Passivation-1	Relax from >=15um to >=3um

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	From Version 1.2 to Version 1.3			
	Rule	**Sec. No.**	**Section Title**	**Revision Description**
			VIA hole)	
23.	RV.S.2	5.5.2.1	RV Layout Rules (Passivation-1 VIA hole)	Relax from >=9um to >=0um
24.	Rename all rules	5.5.3.1	RV Layout Rules (Passivation-1 VIA hole)	Rename CB.W.1/CB.S.1/CB.EN.1/CB.R.1 to RV.W.1/RV.S.1/RV.EN.1/RV.R.1
25.	RV.S.2	5.5.3.1	RV Layout Rules (Passivation-1 VIA hole)	New rule
26.	RV.R.3	5.5.3.1	RV Layout Rules (Passivation-1 VIA hole)	New rule
27.	AP.W.1	5.5.3.2	AP-MD Layout Rules	Add CBD, CB2, and FW(AP) in the rule description
28.	AP.S.2/AP.S.3/AP.S.4	5.5.3.2	AP-MD Layout Rules	Add " overlapping is prohibited in the rule description
29.	AP.EN.1	5.5.3.2	AP-MD Layout Rules	Modify CB-VD to RV
30.	AP.DN.1	5.5.3.2	AP-MD Layout Rules	Relax the maximum density from 60% to 70%
31.	A.R.10/A.R.11/A.R.12/ A.R.13	4.8.3 5.5.3	Layout Rules for RV and AP-MD	Add new rules Cu process.

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A.4.4.1 Rule Number Mapping Table (from Version 1.2 to 1.3):

Consolidate from T-000-CL-DR-001 Ver1.2		
T-000-CL-DR-001	**Version1.3**	**Note**
CB.EN.1	CUPCB.EN.1	No rule change
CB.R.3	CUPCB.R.1	No rule change
CBVIAT.EN.2	CUPVIAT.EN.1	No rule change
CBVIAT.W.2	CUPVIAT.W.1	No rule change
CBVIAT.W.3	CUPVIAT.W.2	No rule change
CBVIAT.S.3	CUPVIAT.S.1	No rule change
CBVIAT.S.4	CUPVIAT.S.2	No rule change
CBVIAT.DN.1	CUPVIAT.DN.1	No rule change
CBVIAT.R.2	CUPVIAT.R.1	No rule change
Consolidate from T-013-CL-DR-005 Ver.1.2		
T-013-CL-DR-005	**Version1.3**	**Note**
CB.EN.3	CUPCB.EN.2	No rule change
CB.EN.4	CUPCB.EN.3	No rule change
CB.EN.5	CUPCB.EN.4	No rule change
CB.EN.6	CUPCB.EN.5	No rule change
CB.W.5	CUPCB.W.1	Change from =5um to >=5um
CB.R.3[u]	CUPCB.R.2 [u]	No rule change
CB.R.4	CUPCB.R.3	No rule change
CB.R.5	CUPCB.R.4	No rule change
CB.R.6[u]	CUPCB.R.5 [u]	Remove the constraint of “It’s prohibited to place CUP chip and non-CUP pad in the same chip”
CB.R.7	CUPCB.R.6	No rule change
CBVIAT.W.1	CUPVIAT.W.3	No rule change
CBVIAT.S.1	CUPVIAT.S.3	No rule change
CBVIAT.S.2	CUPVIAT.S.4	No rule change
CBVIAT.S.3	CUPVIAT.S.5	No rule change
CBVIAT.EN.1	CUPVIAT.EN.2	No rule change
CBVIAT.R.1	CUPVIAT.R.2	No rule change
CBVIAT.R.2	-	Remove
Rename the RV rules in section 5.5.2		
Version1.2	**Version1.3**	**Note**
CB.W.5**	RV.W.2	Change from 25um to 5um
CB.S.3**	RV.S.1	Change from15um to 3um
CB.S.4	RV.S.2	Change from 9um to 0um
CB.EN.3	RV.EN.2	
Rename the RV rules in section 5.5.3		
Version1.2	**Version1.3**	**Note**
CB.W.1	RV.W.1	No rule change
CB.S.1	RV.S.1	No rule change
-	RV.S.2	New rule
CB.EN.1	RV.EN.1	No rule change
CB.R.1	RV.R.1	No rule change
-	RV.R.3	New rule

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A.4.5 Change from Version 1.3 to 1.4

From Version 1.3 to Version 1.4			
Rule	**Sec. No.**	**Section Title**	**Revision Description**
Consolidate N90/N65 CUP design rule (T-N90-CL-DR-009)	2.4	Special Recognition CAD Layers	Add WBDMY to cover CUP pad
	3.3.3	Pad Pitch Rules for Wire Bond	Add CUP relative descriptions in the current rules (CB.W.3/CB.S.2/CB.EN.1)
	3.3.4.2.2	Circuit Under Pad (CUP) Pad structure rules (for N65/N90)	Merge all rules from T-N90-CL-DR-009
A.R.10/A.R.11/A.R.12	3.3.7.3	Antenna Effect Prevention (A) Layout Rules for RV and AP-MD	Add antenna rules with core and I/O devices Modify the A.R.12 parameter numbers
UBM.EN.1	4.2	Under Bump Metallurgy (UBM) Rules	Change rule number from 100um to 80um.
UBM.EN.1®	4.2	Under Bump Metallurgy (UBM) Rules	New rule for placing UBM uniform.
UBM.EN.2	4.2	Under Bump Metallurgy (UBM) Rules	New rule for placing UBM uniform.
UBM.EN.3	4.2	Under Bump Metallurgy (UBM) Rules	New rule for preventing iso bump.
UBM.EN.3®	4.2	Under Bump Metallurgy (UBM) Rules	New rule for preventing iso bump.
UBM.R.6®^{u}	4.2	Under Bump Metallurgy (UBM) Rules	Change rule number from 1.0~1.1 to 0.95~1.05
UBM.EN.2	4.3.5	Flip Chip non-shrinkable Rules for the Half Node Technologies	Change rule number from 2.3 to 2.2
BP.EN.5	4.3.5	Flip Chip non-shrinkable Rules for the Half Node Technologies	Change rule number from 11.2 to 11

A.4.5.1 Rule Number Mapping Table (from Version 1.3 to 1.4):

Consolidate from T-N90-CL-DR-009 Ver.1.2		
T-N90-CL-DR-009	**Version1.4**	**Note**
CB.EN.3	CUPCB.EN.6	No rule change
CB.EN.4	CUPCB.EN.7	No rule change
CB.R.3^{u}	CUPCB.EN.7^{u}	No rule change
CB.R.6^{u}	CUPCB.EN.8^{u}	No rule change
CB.R.7	CUPCB.R.7	No rule change
CBVIAT.W.1	CUPVIAT.W.1	No rule change
CBVIAT.S.1	CUPVIAT.S.1	No rule change
CBVIAT.EN.1	CUPVIAT.EN.1	No rule change
CBVIAT.DN.1	CUPVIAT.DN.1	No rule change
CBVIAT.DN.2	CUPVIAT.DN.2	No rule change

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A.5 Revision History of T-N65-CL-DR-029 (5V HV CMOS)

A.5.1 Change from Version 0.1 to 1.0

	Rule	Sec. No.	Section Title	Revision Description
1	HVD_N.W.2	3.2	HVD_N Layout Rules	Add this rule
2	HVD_N.R.6	3.2	HVD_N Layout Rules	Add this rule
3	HVD_P.W.2	3.3	HVD_P Layout Rules	Add this rule
4	HVD_P.EN.1	3.3	HVD_P Layout Rules	Change the rule from 0.6 to 1.6
5	HVD_P.R.1	3.3	HVD_P Layout Rules	Change NW to {NW not interact with DNW}
6	HVD_P.R.6	3.3	HVD_P Layout Rules	Add this rule
7		4.1	Latch-up Dummy Layers Summary	Add this section
8	LUP.3.5.1g	4.2	Layout Guidelines for Latch-Up Prevention	Add this guideline
9	LUP.3.5.2g	4.2	Layout Guidelines for Latch-Up Prevention	Add this guideline.
10	LUP.5.5.1g	4.2	Layout Guidelines for Latch-Up Prevention	Add this guideline.
11	LUP.5.5.2g	4.2	Layout Guidelines for Latch-Up Prevention	Add this guideline.
12		4.3	Layout Guidelines for ESD	Add this section
13	GR.R.1	5.1	Guard Ring Rules	Add this rule
14	GR.R.2^{U}	5.1	Guard Ring Rules	Add this rule
15	GR.R.3^{U}	5.1	Guard Ring Rules	Add this rule
16	GR.R.4^{U}	5.1	Guard Ring Rules	Add this rule
17	GR.R.5^{U}	5.1	Guard Ring Rules	Add this rule
18	BV.W.1g	5.2	Breakdown Characterization Guidelines	Add this guideline.
19	BV.W.2g	5.2	Breakdown Characterization Guidelines	Add this guideline.
20	BV.R.1g	5.2	Breakdown Characterization Guidelines	Add this guideline.

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