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OP AMPS FOR EVERYONE

Third Edition

- Overflowing with "how-to" design material
- Includes a comprehensive view of op amp design tools
- Details working solutions that keep your schedule in mind

Bruce Carter and Ron Mancini
Editors in Chief

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Dedication

I dedicate this edition to Erin Sanders, whose television portrayal of teenage scientist Quinn Pensky encourages young women not to abandon scientific study but to embrace it instead.

Foreword

Everyone interested in analog electronics should find some value in this book, and an effort has been made to make the material understandable to the relative novice while not too boring for the practicing engineer. Special effort has been taken to ensure that each chapter can stand alone for the reader with the proper background. Of course, this causes redundancy that some people might find boring, but it's worth the price to enable the satisfaction of a diversified audience.

Chapter 1 is a history and story chapter. It is not required reading for anyone, but it defines the op amp's place in the world of analog electronics. Start at Chapter 1 if you are a novice, and read through until completion of Chapter 11. After Chapter 11 is completed, the reader can jump to any chapter and be confident that they are prepared for the material. More experienced people such as electronic technicians, digital engineers, and non-electronic engineers can start at Chapter 3 and read through Chapter 11. Senior electronic technicians, electronic engineers, and fledgling analog engineers can start anywhere they feel comfortable and read through Chapter 13. Experienced analog engineers should jump to the subject that interests them.

First Edition Credits

- Thanks to editor James Karki for his contribution.
- Thanks to Ted Thomas, a marketing manager with courage enough to support this book.
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Ron Mancini, Chief Editor, First Edition

Preface to the Third Edition

In the intervening years since the first edition was published, there have been many developments in the field of op amps and related design aids. This edition augments the original material in light of these developments, and highlights the new exciting design tools and techniques.

Op amps have increased dramatically in speed, enabling design into the RF domain. New generations of op amps have included fully differential models, which not only return to the op amp's roots, but open up new applications in the interfacing of differential signal chains. Op amp design tools now include not only new generations of filter design and simulation software, but gain and offset design software as well—making the task of the signal chain designer almost trivial. Focus can now be on the selection of the best amplifier for the job, instead of being mired in transfer equations and confusing topologies to interface one signal level and offset to another. It is hoped that a theoretically minded engineer will find this book a useful design reference, but the focus is more on the signal chain designer on a tight schedule, who needs good working solutions to a project with a minimum of calculation. This book includes extensive "how-to" design sections, which will produce very good design solutions rapidly, using readily available components.

I wish to thank John Bishop and Thomas Kugelstadt, who contributed to this edition. A very special thanks to my friend and mentor Ron Mancini, whose material still makes up a very significant portion of this volume. Without his inspiration, there never would have been a first edition of *Op Amps for Everyone*, let alone a second and third.

Bruce Carter, Chief Editor, Third Edition

CHAPTER 1

The Op Amp's Place in the World

Ron Mancini

1.1 The Problem

In 1934, Harry Black [1] commuted from his home in New York City to work at Bell Labs in New Jersey by way of a railroad and a ferry. The ferry ride relaxed Harry, enabling him to do some conceptual thinking. Harry had a tough problem to solve; when phone lines were extended long distances, they needed amplifiers, and undependable amplifiers limited phone service. First, initial tolerances on the gain were poor, but that problem was quickly solved with an adjustment. Second, even when an amplifier was adjusted correctly at the factory, the gain drifted so much during field operation that the volume was too low or the incoming speech was distorted.

Many attempts had been made to make a stable amplifier, but temperature changes and power supply voltage extremes experienced on phone lines caused uncontrollable gain drift. Passive components had much better drift characteristics than active components; therefore, if an amplifier's gain could be made dependent on passive components, the problem would be solved. During one of his ferry trips, Harry's fertile brain conceived a novel solution for the amplifier problem, and he documented the solution while riding on the ferry.

1.2 The Solution

The solution was to first build an amplifier that had more gain than the application required. Then, some of the amplifier output signal was fed back to the input in a manner that makes the circuit gain (the circuit includes the amplifier and feedback components) dependent on the feedback circuit rather than the amplifier gain. Now,

the circuit gain is dependent on the passive feedback components rather than the active amplifier. This, called *negative feedback*, is the underlying operating principle for all modern day op amps. Harry documented the first intentional feedback circuit during a ferry ride. I am sure unintentional feedback circuits had been built prior to that time, but the designers ignored the effect!

I can hear the squeals of anguish coming from the managers and amplifier designers of the era. I imagine that they said something like this, "It is hard enough to achieve 30 kHz gain-bandwidth (GBW), and now this fool wants me to design an amplifier with 3 MHz GBW. But, he is still going to get a circuit gain GBW of 30 kHz." Well, time has proven Harry right, but there is a minor problem that Harry didn't discuss in detail, the oscillation problem. It seems that circuits designed with large open loop gains sometimes oscillate when the loop is closed. A lot of people investigated the instability effect, and it was pretty well understood in the 1940s, but solving stability problems involved long, tedious, and intricate calculations. Years passed with nobody making the problem solution simpler or more understandable.

In 1945, H. W. Bode presented a system for analyzing the stability of feedback systems by using graphical methods. Until this time, feedback analysis was done by multiplication and division, so calculation of transfer functions was a time consuming, laborious task. Remember, engineers did not have electronic calculators or computers until the 1970s. Bode presented a logarithmic technique that transformed the intensely mathematical process of calculating a feedback system's stability into graphical analysis that was simple and perceptive. Feedback system design was still complicated, but it no longer was an art dominated by a few electrical engineers kept in a small dark room. Any electrical engineer could use Bode's methods to find the stability of a feedback circuit, so the application of feedback to machines began to grow. There really wasn't much call for electronic feedback design until computers and transducers became of age, however.

1.3 The Birth of the Op Amp

The first real-time computer was the analog computer! This computer used preprogrammed equations and input data to calculate control actions. The programming was hardwired, with a series of circuits that performed math operations on the data; and the hardwiring limitation eventually caused the declining popularity of the analog computer. The heart of the analog computer was a device called an *operational amplifier*, because it could be configured to perform many mathematical operations,

such as multiplication, addition, subtraction, division, integration, and differentiation, on the input signals. The name was shortened to the familiar *op amp*, as we have come to know and love them. The op amp used an amplifier with a large open loop gain, and when the loop was closed, the amplifier performed the mathematical operations dictated by the external passive components. This amplifier was very large because it was built with vacuum tubes and required a high voltage power supply, but it was the heart of the analog computer, so its large size and huge power requirements were accepted as the price of doing business. Early op amps were designed for analog computers, and it was soon found out that op amps had other uses and were very handy to have around the physics lab.

At this time, general purpose analog computers were found in universities and large company laboratories because they were critical to the research work done there. There was a parallel requirement for transducer signal conditioning in lab experiments, and op amps found their way into signal conditioning applications. As the signal conditioning applications expanded, the demand for op amps grew beyond the analog computer requirements. Even when the analog computers lost favor to digital computers, the op amp survived because of its importance in universal analog applications. Eventually digital computers replaced the analog computers (a sad day for real time measurements), but the demand for op amps increased as measurement applications increased.

1.4 The Vacuum Tube Era

The first signal conditioning op amps were constructed with vacuum tubes prior to the introduction of transistors, so they were large and bulky. During the 1950s, miniature vacuum tubes that worked from lower voltage power supplies enabled the manufacture of op amps that shrank to the size of a brick used in house construction, so the op amp modules were nicknamed *bricks*. Vacuum tube size and component size decreased until an op amp was shrunk to the size of a single octal vacuum tube.

One of the first commercially available op amps was the model K2-W, sold by George A. Philbrick Research. It consisted of two vacuum tubes, and operated from a ± 300 V power supply! If that is not enough to make a modern analog designer cringe, then it's fully differential nature would be sure to. A fully differential op amp, as opposed to the more familiar single ended op amp, has two outputs—a noninverting output and an inverting output. It requires the designer to close two feedback paths, not just one. Before panic sets in—the two feedback pathways require only duplication

of components, not an entirely new design methodology. Fully differential op amps are currently enjoying resurgence, because they are ideal components for driving the inputs of fully differential analog to digital converters (ADCs). They also find use in driving differential signal pairs, such as DSL and balanced 600 Ω audio. Suffice it to say, op amps have come full circle since their original days.

1.5 The Transistor Era

Transistors were commercially developed in the 1960s, and they further reduced op amp size to several cubic inches, but the nickname *brick* still held on. Now the nickname *brick* is attached to any electronic module that uses potting compound or non-integrated circuit (non-IC) packaging methods. Most of these early op amps were made for specific applications, so they were not necessarily general purpose. The early op amps served a specific purpose, but each manufacturer had different specifications and packages; hence, there was little second sourcing among the early op amps.

1.6 The IC Era

ICs were developed during the late 1950s and early 1960s, but it wasn't until the middle 1960s that Fairchild released the μA709. This was the first commercially successful IC op amp, and Robert J. Widler designed it. The μA709 had its share of problems, but any competent analog engineer could use it, and it served in many analog applications. The major drawback of the μA709 was stability—it required external compensation and a competent analog engineer to apply it. Also, the μA709 was quite sensitive because it had a habit of self-destructing under any adverse condition. The self-destruction habit was so prevalent that one major military equipment manufacturer published a paper titled something like, "The 12 Pearl Harbor Conditions of the μA709."

The legacy of the μA709 continues today, but it is a negative legacy. The μA709 would not work if applied incorrectly, primarily due to its external compensation. The engineers of today may not even know the part, but memory of its instability remains—few uncompensated amplifiers are sold today due to the problem of misapplication. Stability remains one of the least understood aspects of op amp design, and one of the easiest ways to misapply an op amp. Even engineers with years of analog design experience have differing opinions on the topic. The wise engineer, however, will look

carefully at the op amp data sheet and not attempt a gain less than its specification. It may be counterintuitive, but the op amp is least stable at its lowest specified gain. Future chapters delve deeply into this phenomenon.

The μA741 followed the μA709, and it is an internally compensated op amp that requires no external compensation if operated under data sheet conditions. Also, it is much more forgiving than the μA709.

The legacy of the μA741 is much more positive than that of its predecessor. In fact, the part number, 741, is etched into the memory of practically every engineer in the world, much like the 2N2222 transistor and the 1N4148 diode. It is usually the first part number that comes to mind whenever an engineer thinks of an op amp. Unlike the μA709, the μA741 will work unless grossly misapplied, a fact that has endeared it to generations of engineers. Its power supply requirement of ±15 V has given rise to hundreds of power supply components that generate these levels, much as +5 V has been driven by TTL logic and ±12 V has been driven by RS232 serial interfaces. For many years, every op amp introduced used the same ±15 V power supplies as the μA741. Even today, the μA741 is an excellent choice where wide dynamic range and ruggedness are required.

A never-ending series of new op amps has been released each year since the introduction of the μA741, and the performance and reliability have improved to the point where present day op amps can be used for analog applications by anybody.

The IC op amp is here to stay; the latest generation op amps cover the frequency spectrum from 5 kHz GBW for extremely low power devices to beyond 3 GHz GBW. The supply voltage ranges from guaranteed operation at 0.9 V to absolute maximum voltage ratings of 1000 V. The input current and input offset voltage has fallen so low that customers have problems verifying the specifications during incoming inspection. The op amp has truly become the universal analog IC because it performs all analog tasks. It can function as a line driver, amplifier, level shifter, oscillator, filter, signal conditioner, actuator driver, current source, voltage source, and in many other applications. The designer's problems are how to rapidly select the correct circuit/op amp combination and, then, how to calculate the passive component values that yield the desired transfer function in the circuit.

It should be noted that no op amp is universally applicable. An op amp that is ideal for transducer interfaces will not work at all for RF applications. An op amp with good RF performance may have miserable DC specifications. All the hundreds of op amp

models offered by manufacturers are optimized in slightly different ways, so the designer's task is to weed through those hundreds of devices and find the handful that are appropriate for the specific application. This edition includes a design methodology for doing so—at least in the case of signal chains.

This book deals with op amp circuits, not with the innards of op amps. It treats the calculations from the circuit level, and it doesn't get bogged down in a myriad of detailed calculations. Rather, the reader can start at the appropriate level and quickly move on to advanced topics. If you are looking for material about the innards of op amps you are looking in the wrong place. The op amp is treated as a completed component in this book.

The op amp will continue to be a vital component of analog design because it is such a fundamental component. Each generation of electronics equipment integrates more functions on silicon and takes more of the analog circuitry inside the IC. Don't fear, as digital applications increase, analog applications also increase because the predominant supply of data and interface applications are in the real world, and the real world is an analog world. Therefore, each new generation of electronics equipment creates requirements for new analog circuits; hence, new generations of op amps are required to fulfill these requirements. Analog design, and op amp design, is a fundamental skill that will be required far into the future.

Reference

1. Black, H. S. (1934). "Stabilized Feedback Amplifiers," *BST Journal* 13 (January).

CHAPTER 2

Review of Circuit Theory

Ron Mancini

2.1 Introduction

Although this book minimizes math, some algebra is germane to the understanding of analog electronics. Math and physics are presented here in the manner in which they are used later, so no practice exercises are given. For example, after the voltage divider rule is explained, it is used several times in the development of other concepts, and this usage constitutes practice.

Circuits are a mix of passive and active components. The components are arranged in a manner that enables them to perform some desired function. The resulting arrangement of components is called a *circuit* or sometimes a *circuit configuration.* The art portion of analog design is developing the circuit configuration. Many published circuit configurations are available for almost any circuit task; therefore, circuit designers need not be artists.

When the design has progressed to the point that a circuit exists, equations must be written to predict and analyze circuit performance. Textbooks are filled with rigorous methods for equation writing, and this review of circuit theory does not supplant those textbooks. But, a few equations are used so often that they should be memorized, and these equations are considered here.

A circuit can be analyzed in almost as many ways as there are electronic engineers, and if the equations are written correctly, all methods yield the same answer. There are some simple ways to analyze the circuit without completing unnecessary calculations, and these methods are illustrated here.

2.2 Laws of Physics

Ohm's law is stated as $V = IR$, and it is fundamental to all electronics. Ohm's law can be applied to a single component, to any group of components, or to a complete circuit. When the current flowing through any portion of a circuit is known, the voltage dropped across that portion of the circuit is obtained by multiplying the current times the resistance (Equation 2.1):

$$V = IR \tag{2.1}$$

In Figure 2.1, Ohm's law is applied to the total circuit. The current (I) flows through the total resistance (R), and the voltage (V) is dropped across R.

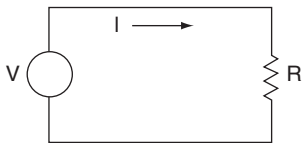


Figure 2.1: Ohm's law applied to the total circuit.

In Figure 2.2, Ohm's law is applied to a single component. The current (I_R) flows through the resistor (R) and the voltage (V_R) is dropped across R. Note: The same formula is used to calculate the voltage drop across R even though it is only a part of the circuit.

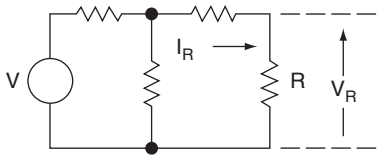


Figure 2.2: Ohm's law applied to a component.

Kirchhoff's voltage law states that the sum of the voltage drops in a series circuit equals the sum of the voltage sources. Otherwise, the source (or sources) voltage must be dropped across the passive components. When taking sums keep in mind that the sum is an algebraic quantity. Kirchhoff's voltage law is illustrated in Figure 2.3 and Equations (2.2) and (2.3):

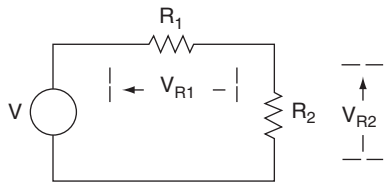


Figure 2.3: Kirchhoff's voltage law.

$$\sum V_{\text{SOURCES}} = \sum V_{\text{DROPS}} \tag{2.2}$$

$$V = V_{R1} + V_{R2} \tag{2.3}$$

Kirchhoff's current law states that the sum of the currents entering a junction equals the sum of the currents leaving a junction. It makes no difference if a current flows from a current source, through a component, or through a wire, because all currents are treated identically. Kirchhoff's current law is illustrated in Figure 2.4 and Equations (2.4) and (2.5):

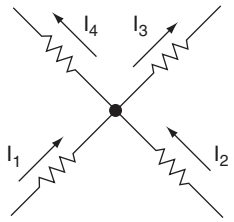


Figure 2.4: Kirchhoff's current law.

$$\sum I_{\text{IN}} = \sum I_{\text{OUT}} \tag{2.4}$$

$$I_1 + I_2 = I_3 + I_4 \tag{2.5}$$

2.3 Voltage Divider Rule

When the output of a circuit is not loaded, the voltage divider rule can be used to calculate the circuit's output voltage. Assume that the same current flows through all circuit elements (Figure 2.5). Equation (2.6) is written using Ohm's law as $V = I\ (R_1 + R_2)$. Equation (2.7) is written as Ohm's law across the output resistor.

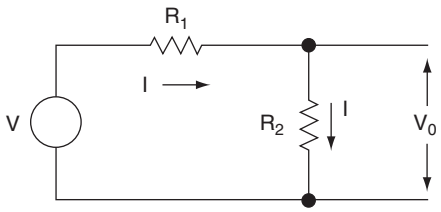


Figure 2.5: Voltage divider rule.

$$I = \frac{V}{R_1 + R_2} \tag{2.6}$$

$$V_{\text{OUT}} = I_{R2} \tag{2.7}$$

Substituting Equation (2.6) into Equation (2.7) and using algebraic manipulation yields Equation (2.8):

$$V_{\text{OUT}} = V\frac{R_2}{R_1 + R_2} \tag{2.8}$$

A simple way to remember the voltage divider rule is that the output resistor is divided by the total circuit resistance. This fraction is multiplied by the input voltage to obtain the output voltage. Remember that the voltage divider rule always assumes that the output resistor is not loaded; the equation is not valid when the output resistor is loaded by a parallel component. Fortunately, most circuits following a voltage divider are input circuits, and input circuits are usually high resistance circuits. When a fixed load is in parallel with the output resistor, the equivalent parallel value comprising the output resistor and loading resistor can be used in the voltage divider calculations with no error. Many people ignore the load resistor if it is 10 times greater than the output resistor value, but this will lead to a 10% error.

2.4 Current Divider Rule

When the output of a circuit is not loaded, the current divider rule can be used to calculate the current flow in the output branch circuit (R_2). The currents I_1 and I_2 in Figure 2.6 are assumed to be flowing in the branch circuits. Equation (2.9) is

written with the aid of Kirchhoff's current law. The circuit voltage is written in Equation (2.10) with the aid of Ohm's law. Combining Equations (2.9) and (2.10) yields Equation (2.11).

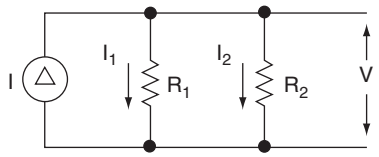


Figure 2.6: Current divider rule.

$$I = I_1 + I_2 \tag{2.9}$$

$$V = I_1 R_1 = I_2 R_2 \tag{2.10}$$

$$I = I_1 + I_2 = I_2 \frac{R_2}{R_1} + I_2 = I_2 \left(\frac{R_1 + R_2}{R_1} \right) \tag{2.11}$$

Rearranging the terms in Equation (2.11) yields Equation (2.12):

$$I_2 = I \left(\frac{R_1}{R_1 + R_2} \right) \tag{2.12}$$

The total circuit current divides into two parts, and the resistance (R_1) divided by the total resistance determines how much current flows through R_2. An easy method of remembering the current divider rule is to remember the voltage divider rule. Then, modify the voltage divider rule such that the opposite resistor is divided by the total resistance and the fraction is multiplied by the input current to get the branch current.

2.5 Thevenin's Theorem

At times, it is advantageous to isolate a part of the circuit to simplify the analysis of the isolated part of the circuit rather than write loop or node equations for the complete circuit and solve them simultaneously. Thevenin's theorem enables us to isolate the part of the circuit we are interested in. We then replace the remaining circuit with a simple series equivalent circuit, thus Thevenin's theorem simplifies the analysis.

Two theorems do similar functions. The Thevenin theorem, just described, is the first, and the second is called *Norton's theorem*. Thevenin's theorem is used when the input source is a voltage source, and Norton's theorem is used when the input source is a current source. Norton's theorem is rarely used, so its explanation is left for the reader to dig out of a textbook if it is ever required.

The rules for Thevenin's theorem start with the component or part of the circuit being replaced. Referring to Figure 2.7 look back into the terminals (left from C and R_3 toward point X–X in the figure) of the circuit being replaced. Calculate the no load voltage (V_{TH}) as seen from these terminals (use the voltage divider rule).

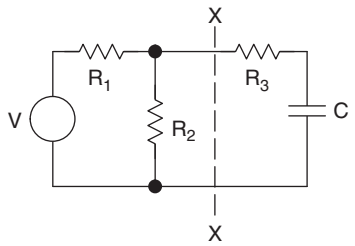


Figure 2.7: Original circuit.

Look into the terminals of the circuit being replaced, short independent voltage sources, and calculate the impedance between these terminals. The final step is to substitute the Thevenin equivalent circuit for the part you wanted to replace, as shown in Figure 2.8.

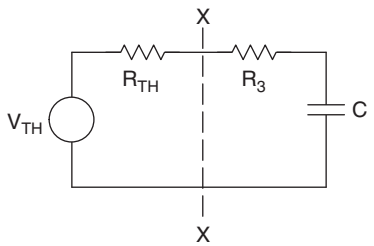
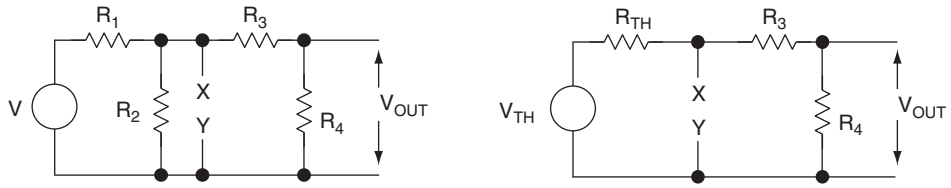


Figure 2.8: Thevenin's equivalent circuit for Figure 2.7.

The Thevenin equivalent circuit is a simple series circuit, thus further calculations are simplified. The simplification of circuit calculations is often sufficient reason to use Thevenin's theorem, because it eliminates the need for solving several simultaneous

equations. The detailed information about what happens in the circuit that was replaced is not available when using Thevenin's theorem, but that is no consequence because you had no interest in it.

As an example of Thevenin's theorem, let's calculate the output voltage (V_{OUT}) shown in Figure 2.9(a). The first step is to stand on the terminals *X*–*Y* with your back to the output circuit and calculate the open circuit voltage seen (V_{TH}). This is a perfect opportunity to use the voltage divider rule to obtain Equation (2.13):



(a) The Original Circuit (b) The Thevenin Equivalent Circuit

Figure 2.9: Example of Thevenin's equivalent circuit.

$$V_{TH} = V\frac{R_2}{R_1 + R_2} \tag{2.13}$$

Still standing on the terminals *X*–*Y*, step 2 is to calculate the impedance seen looking into these terminals (short the voltage sources). The Thevenin impedance is the parallel impedance of R_1 and R_2, as calculated in Equation (2.14). Now, get off the terminals *X*–*Y* before you damage them with your big feet. Step 3 replaces the circuit to the left of *X*–*Y* with the Thevenin equivalent circuit V_{TH} and R_{TH}.

$$R_{TH} = \frac{R_1R_2}{R_1 + R_2} = R_1 \| R_2 \tag{2.14}$$

(Note: Two parallel vertical bars (||) are used to indicate parallel components.)

The final step is to calculate the output voltage. Note that the voltage divider rule is used again. Equation (2.15) describes the output voltage, and it comes out naturally in the form of a series of voltage dividers, which makes sense. That's another advantage of the voltage divider rule: The answers normally come out in a recognizable form rather than a jumble of coefficients and parameters.

$$V_{\text{OUT}} = V_{\text{TH}} \frac{R_4}{R_{TH} + R_3 + R_4} = V\left(\frac{R_2}{R_1 + R_2}\right) \frac{R_4}{\frac{R_1 R_2}{R_1 + R_2} + R_3 + R_4} \tag{2.15}$$

The circuit analysis is done the hard way in Figure 2.10, so you can see the advantage of using Thevenin's theorem. Two loop currents, I_1 and I_2, are assigned to the circuit. Then, the loop Equations (2.16) and (2.17) are written:

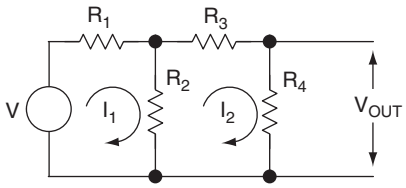


Figure 2.10: Analysis done the hard way.

$$V = I_1(R_1 + R_2) - I_2 R_2 \tag{2.16}$$

$$I_2(R_2 + R_3 + R_4) = I_1 R_2 \tag{2.17}$$

Equation (2.17) is rewritten as Equation (2.18) and substituted into Equation (2.16) to obtain Equation (2.19):

$$I_1 = I_2 \frac{R_2 + R_3 + R_4}{R_2} \tag{2.18}$$

$$V = I_2\left(\frac{R_2 + R_3 + R_4}{R_2}\right)(R_1 + R_2) - I_2 R_2 \tag{2.19}$$

The terms are rearranged in Equation (2.20). Ohm's law is used to write Equation (2.21), and the final substitutions are made in Equation (2.22).

$$I_2 = \frac{V}{\frac{R_2 + R_3 + R_4}{R_2}(R_1 + R_2) - R_2} \tag{2.20}$$

$$V_{OUT} = I_2 R_4 \tag{2.21}$$

$$V_{OUT} = V \frac{R_4}{\frac{(R_2 + R_3 + R_4)(R_1 + R_2)}{R_2} - R_2} \tag{2.22}$$

This is a lot of extra work for no gain. Also, the answer is not in a usable form because the voltage dividers are not recognizable. Therefore, more algebra is required to get the answer into usable form.

2.6 Superposition

Superposition is a theorem that can be applied to any linear circuit. Essentially, when there are independent sources, the voltages and currents resulting from each source can be calculated separately, and the results are added algebraically. This simplifies the calculations, because it eliminates the need to write a series of loop or node equations. An example is shown in Figure 2.11.

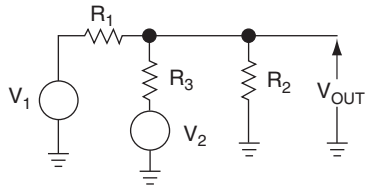


Figure 2.11: Superposition example.

When V_1 is grounded, V_2 forms a voltage divider with R_3 and the parallel combination of R_2 and R_1. The output voltage for this circuit (V_{OUT2}) is calculated with the aid of the voltage divider Equation (2.23). The circuit is shown in Figure 2.12. The voltage divider rule yields the answer quickly.

$$V_{OUT2} = V_2 \frac{R_1 \| R_2}{R_3 + R_1 \| R_2} \tag{2.23}$$

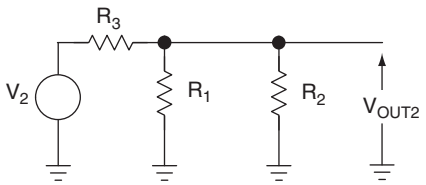


Figure 2.12: When V_1 is grounded.

Likewise, when V_2 is grounded (Figure 2.13), V_1 forms a voltage divider with R_1 and the parallel combination of R_3 and R_2, and the voltage divider theorem is applied again to calculate V_{OUT}, Equation (2.24):

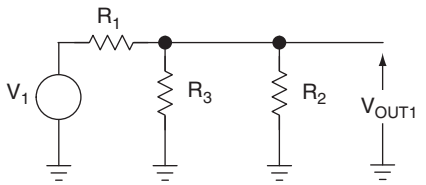


Figure 2.13: When V_2 is grounded.

$$V_{OUT1} = V_1 \frac{R_2 \| R_3}{R_1 + R_2 \| R_3} \tag{2.24}$$

After the calculations for each source are made, the components are added to obtain the final solution, Equation (2.25):

$$V_{OUT} = V_1 \frac{R_2 \| R_3}{R_1 + R_2 \| R_3} + V_2 \frac{R_1 \| R_2}{R_3 + R_1 \| R_2} \tag{2.25}$$

The reader should analyze this circuit with loop or node equations to gain an appreciation for superposition. Again, the superposition results come out as a simple arrangement that is easy to understand. One looks at the final equation and it is obvious that, if the sources are equal and opposite polarity and $R_1 = R_3$, then the output voltage is zero. Conclusions such as this are hard to make after the results of a loop or node analysis unless considerable effort is made to manipulate the final equation into symmetrical form.

2.7 Calculation of a Saturated Transistor Circuit

The circuit specifications are these: When $V_{IN} = 12$ V, $V_{OUT} < 0.4$ V at $I_{SINK} < 10$ mA, and $V_{IN} < 0.05$ V, $V_{OUT} > 10$ V at $I_{OUT} = 1$ mA. The circuit diagram is as shown in Figure 2.14.

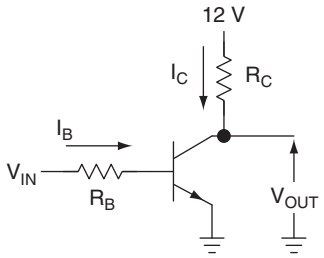


Figure 2.14: Saturated transistor circuit.

The collector resistor must be sized, Equation (2.26), when the transistor is off, because it has to be small enough to allow the output current to flow through it without dropping more than 2 V to meet the specification for a 10 V output:

$$R_C \leq \frac{V_{+12} - V_{OUT}}{I_{OUT}} = \frac{12 - 10}{1} = 2 \text{ k} \tag{2.26}$$

When the transistor is off, 1 mA can be drawn out of the collector resistor without pulling the collector or output voltage to less than 10 V, Equation (2.27). When the transistor is on, the base resistor must be sized, Equation (2.28), to enable the input signal to drive enough base current into the transistor to saturate it. The transistor beta is 50.

$$I_C = \beta I_B = \frac{V_{+12} - V_{CE}}{R_C} + I_L \approx \frac{V_{+12}}{R_C} + I_L \tag{2.27}$$

$$R_B \leq \frac{V_{IN} - V_{BE}}{I_B} \tag{2.28}$$

Substituting Equation (2.27) into Equation (2.28) yields Equation (2.29):

$$R_B \leq \frac{(V_{IN} - V_{BE})\beta}{I_C} = \frac{(12 - 0.6)50 \text{ V}}{\left[\frac{12}{2} + (10)\right]\text{mA}} = 35.6 \text{ k} \tag{2.29}$$

When the transistor goes on, it sinks the load current, and it still goes into saturation. These calculations neglect some minor details, but they are in the 98% accuracy range.

2.8 Transistor Amplifier

The amplifier is an analog circuit (Figure 2.15), and the calculations, plus the points that must be considered during the design, are more complicated than for a saturated circuit. This extra complication leads people to say that analog design is harder than digital design (the saturated transistor is digital, i.e., on or off). Analog design is harder than digital design because the designer must account for all states in analog, whereas only two states must be accounted for in digital. The specifications for the amplifier are an AC voltage gain of 4 and a peak to peak signal swing of 4 V.

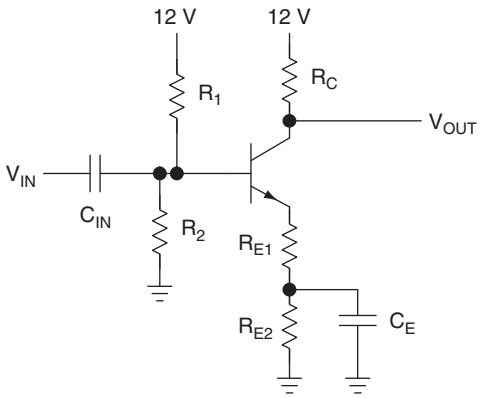


Figure 2.15: Transistor amplifier.

IC is selected as 10 mA because the transistor has a current gain (β) of 100 at that point. The collector voltage is arbitrarily set at 8 V; when the collector voltage swings positive 2 V (from 8 V to 10 V), enough voltage still is dropped across R_C to keep the transistor on. Set the collector/emitter voltage at 4 V; when the collector voltage swings negative 2 V (from 8 V to 6 V), the transistor still has 2 V across it, so it stays linear. This sets the emitter voltage (V_E) at 4 V.

$$R_C \leq \frac{V_{+12} - V_C}{I_C} = \frac{12\text{ V} - 8\text{ V}}{10\text{ mA}} = 400\ \Omega \tag{2.30}$$

$$R_E = R_{E1} + R_{E2} = \frac{V_E}{I_E} = \frac{V_E}{I_B + I_C} \cong \frac{V_E}{I_C} = \frac{4\text{ V}}{10\text{ mA}} = 400\ \Omega \tag{2.31}$$

Use Thevenin's equivalent circuit to calculate R_1 and R_2, as shown in Figure 2.16:

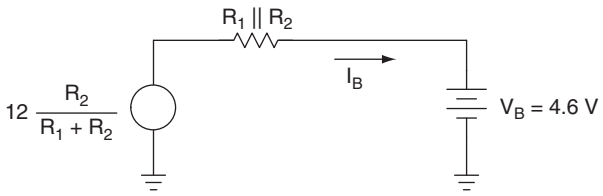


Figure 2.16: Thevenin equivalent of the base circuit.

$$I_B = \frac{I_C}{\beta} = \frac{10\text{ mA}}{100} = 0.1\text{ mA} \tag{2.32}$$

$$V_{\text{TH}} = \frac{12R_2}{R_1 + R_2} \tag{2.33}$$

$$R_{\text{TH}} = \frac{R_1R_2}{R_1 + R_2} \tag{2.34}$$

We want the base voltage to be 4.6 V because the emitter voltage is then 4 V. Assume a voltage drop of 0.4 V across R_{TH}, so Equation (2.35) can be written. The drop across R_{TH} may not be exactly 0.4 V because of beta variations, but a few hundred millivolts does not matter in this design. Now, calculate the ratio of R_1 and R_2 using the voltage divider rule (the load current has been accounted for).

$$R_{\text{TH}} = \frac{0.4}{0.1}\text{k} = 4\text{ k} \tag{2.35}$$

$$V_{\text{TH}} = I_BR_{\text{TH}} + V_B = 0.4 + 4.6 = 5 = 12\frac{R_2}{R_1 + R_2} \tag{2.36}$$

$$R_2 = \frac{7}{5}R_1 \tag{2.37}$$

R_1 is almost equal to R_2, thus selecting R_1 as twice the Thevenin resistance yields approximately 4 k, as shown in Equation (2.35). Hence, $R_1 = 11.2$ k and $R_2 = 8$ k. The AC gain is approximately R_C/R_{E1} because C_E shorts out R_{E2} at high frequencies, so we can write Equation (2.38):

$$R_{E1} = \frac{R_C}{G} = \frac{400}{4} = 100\ \Omega \tag{2.38}$$

$$R_{E2} = R_E - R_{E1} = 400 - 100 = 300\ \Omega \tag{2.39}$$

The capacitor selection depends on the frequency response required for the amplifier, but 10 μF for C_{IN} and 1000 μF for C_E suffice for a starting point.

CHAPTER 3

Development of the Ideal Op Amp Equations

Ron Mancini

3.1 Ideal Op Amp Assumptions

The name *ideal op amp* is applied to this and similar analyses because the salient parameters of the op amp are assumed to be perfect. An engineer may wish that an ideal op amp existed at times, but if such a component actually did exist, it would destroy the known universe! See the end of this chapter for an explanation. We are all thankful that there is no such thing as an ideal op amp, but present day op amps come so close to ideal that *ideal op amp* analysis approaches actual analysis. Op amps depart from the ideal in two ways. First, DC parameters, such as input offset voltage, are large enough to cause departure from the ideal. The ideal assumes that input offset voltage is zero. Second, AC parameters, such as gain, are a function of frequency, so they go from large values at DC to small values at high frequencies.

This assumption simplifies the analysis, thus it clears the path for insight. It is so much easier to see the forest when the brush and huge trees are cleared away. Although the ideal op amp analysis makes use of perfect parameters, the analysis is often valid because some op amps approach perfection. In addition, when working at low frequencies, several kilohertz, the ideal op amp analysis produces accurate answers. Voltage feedback op amps are covered in this chapter, and current feedback op amps are covered in Chapter 9.

Several assumptions have to be made before the ideal op amp analysis can proceed. First, assume that the current flow into the input leads of the op amp is zero. This

assumption is almost true in FET op amps where input currents can be less than a picoamp, but this is not always true in bipolar high speed op amps, where tens of microamp input currents are found.

Second, the op amp gain is assumed to be infinite, hence it drives the output voltage to any value to satisfy the input conditions. This assumes that the op amp output voltage can achieve any value. In reality, saturation occurs when the output voltage comes close to a power supply rail; but reality does not negate the assumption, it only bounds it.

Also, implicit in the infinite gain assumption is the need for zero input signal. The gain drives the output voltage until the voltage between the input leads (the error voltage) is zero. This leads to the third assumption, that the voltage between the input leads is zero. The implication of zero voltage between the input leads means that, if one input is tied to a hard voltage source such as ground, then the other input is at the same potential. The current flow into the input leads is zero, so the input impedance of the op amp is infinite.

Fourth, the output impedance of the ideal op amp is zero. The ideal op amp can drive any load without an output impedance dropping voltage across it. The output impedance of most op amps is a fraction of an ohm for low current flows, so this assumption is valid in most cases. Fifth, the frequency response of the ideal op amp is flat: This means that the gain does not vary as frequency increases. By constraining the use of the op amp to the low frequencies, we make the frequency response assumption true.

Table 3.1 lists the basic ideal op amp assumptions and Figure 3.1 shows the ideal op amp.

Table 3.1: Basic Ideal Op Amp Assumptions

Parameter name	Parameters symbol	Value
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	a	∞

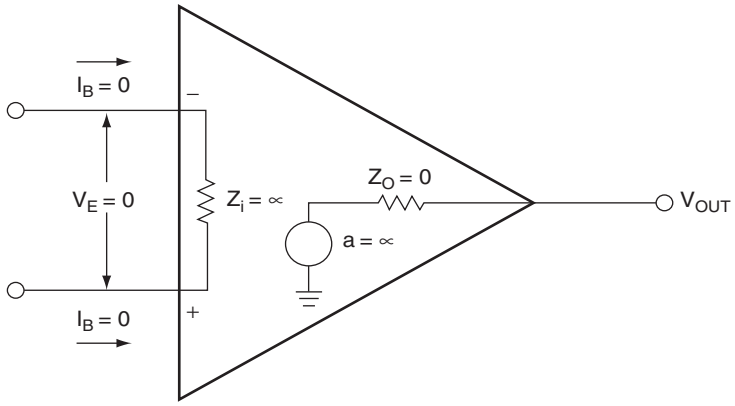


Figure 3.1: The ideal op amp.

3.2 The Noninverting Op Amp

The noninverting op amp has the input signal connected to its noninverting input (Figure 3.2), thus its input source sees an infinite impedance. There is no input offset voltage, because $V_{OS} = V_E = 0$, hence the negative input must be at the same voltage as the positive input. The op amp output drives current into R_F until the negative input is at the voltage, V_{IN}. This action causes V_{IN} to appear across R_G.

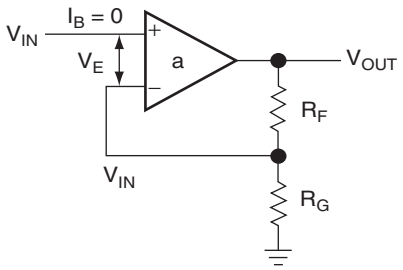


Figure 3.2: The noninverting op amp.

The voltage divider rule is used to calculate V_{IN}: V_{OUT} is the input to the voltage divider, and V_{IN} is the output of the voltage divider. Since no current can flow into either op amp lead, use of the voltage divider rule is allowed. Equation (3.1)

is written with the aid of the voltage divider rule, and algebraic manipulation yields Equation (3.2) in the form of a gain parameter:

$$V_{\text{IN}} = V_{\text{OUT}} \frac{R_G}{R_G + R_F} \tag{3.1}$$

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{R_G + R_F}{R_G} = 1 + \frac{R_F}{R_G} \tag{3.2}$$

when R_G becomes very large with respect to R_F, $(R_F/R_G) \Rightarrow 0$ and Equation (3.2) reduces to Equation (3.3):

$$V_{\text{OUT}} = 1 \tag{3.3}$$

Under these conditions $V_{\text{OUT}} = 1$ and the circuit becomes a unity gain buffer. R_G is usually deleted to achieve the same results, and when R_G is deleted, R_F can also be deleted (R_F must be shorted when it is deleted). When R_F and R_G are deleted, the op amp output is connected to its inverting input with a wire. Some op amps are self-destructive when R_F is left out of the circuit, so R_F is used in many buffer designs. When R_F is included in a buffer circuit, its function is to protect the inverting input from an overvoltage to limit the current through the input ESD (electrostatic discharge) structure (typically <1 mA), and it can have almost any value (20 k is often used). R_F can never be left out of the circuit in a current feedback amplifier design because R_F determines stability in current feedback amplifiers.

3.3 The Inverting Op Amp

The noninverting input of the inverting op amp circuit is grounded (Figure 3.3). One assumption made is that the input error voltage is zero, so the feedback keeps inverting the input of the op amp at a virtual ground (not actual ground but acting like ground). The current flow in the input leads is assumed to be zero, hence the current flowing through R_G equals the current flowing through R_F. Using Kirchhoff's law, we write Equation (3.4); and the minus sign is inserted because this is the inverting input. Algebraic manipulation gives Equation (3.5).

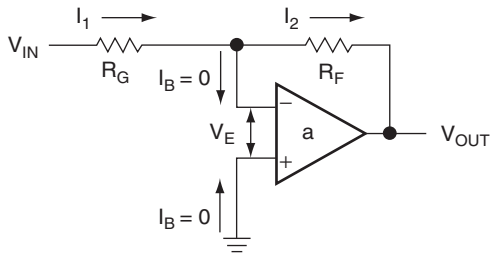


Figure 3.3: The inverting op amp.

$$I_1 = \frac{V_{\text{IN}}}{R_G} = -I_2 = -\frac{V_{\text{OUT}}}{R_F} \tag{3.4}$$

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = -\frac{R_F}{R_G} \tag{3.5}$$

Note that the gain is a function of only the feedback and gain resistors, so the feedback has accomplished its function of making the gain independent of the op amp parameters. The actual resistor values are determined by the impedance levels that the designer wants to establish. If $R_F = 10$ k and $R_G = 10$ k, the gain is –1, as shown in Equation (3.5); and if $R_F = 100$ k and $R_G = 100$ k, the gain is still –1. The impedance levels of 10 k or 100 k determine the current drain, the effect of stray capacitance, and a few other points. The impedance level does not set the gain; the ratio of R_F/R_G does.

One final note: The output signal is the input signal amplified and inverted. The circuit input impedance is set by R_G, because the inverting input is held at a virtual ground.

3.4 The Adder

An adder circuit can be made by connecting more inputs to the inverting op amp (Figure 3.4). The opposite end of the resistor connected to the inverting input is held at virtual ground by the feedback; therefore, adding new inputs does not affect the response of the existing inputs.

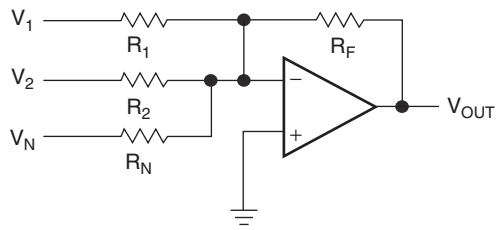


Figure 3.4: The adder circuit.

Superposition is used to calculate the output voltages resulting from each input, and the output voltages are added algebraically to obtain the total output voltage. Equation (3.6) is the output equation when V_1 and V_2 are grounded. Equations (3.7) and (3.8) are the other superposition equations, and the final result is given in Equation (3.9).

$$V_{OUTN} = -\frac{R_F}{R_N}V_N \tag{3.6}$$

$$V_{OUT1} = -\frac{R_F}{R_1}V_1 \tag{3.7}$$

$$V_{OUT2} = -\frac{R_F}{R_2}V_2 \tag{3.8}$$

$$V_{OUT} = -\left(\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_N}V_N\right) \tag{3.9}$$

3.5 The Differential Amplifier

The differential amplifier circuit amplifies the difference between signals applied to the inputs (Figure 3.5). Superposition is used to calculate the output voltage resulting from each input voltage, then the two output voltages are added to arrive at the final output voltage.

The op amp input voltage resulting from the input source, V_1, is calculated in Equations (3.10) and (3.11). The voltage divider rule is used to calculate the voltage,

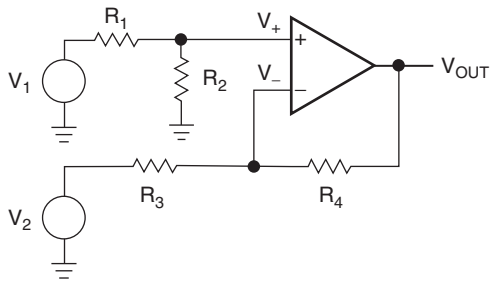


Figure 3.5: The differential amplifier.

V_+, and the noninverting gain equation, Equation (3.2), is used to calculate the noninverting output voltage, V_{OUT1}:

$$V_+ = V_1 \frac{R_2}{R_1 + R_2} \tag{3.10}$$

$$V_{OUT1} = V_+(G_+) = V_1 \frac{R_2}{R_1 + R_2}\left(\frac{R_3 + R_4}{R_3}\right) \tag{3.11}$$

The inverting gain equation, Equation (3.5), is used to calculate the stage gain for V_{OUT2} in Equation (3.12). These inverting and noninverting gains are added in Equation (3.13).

$$V_{OUT2} = V_2\left(\frac{-R_4}{R_3}\right) \tag{3.12}$$

$$V_{OUT} = V_1 \frac{R_2}{R_1 + R_2}\left(\frac{R_3 + R_4}{R_3}\right) - V_2\frac{R_4}{R_3} \tag{3.13}$$

$$V_{OUT} = (V_1 - V_2)\frac{R_4}{R_3} \tag{3.14}$$

It is now obvious that the differential signal, $(V_1 - V_2)$, is multiplied by the stage gain, so the name *differential amplifier* suits the circuit. Because it amplifies only the differential portion of the input signal, it rejects the common mode portion of

the input signal. A common mode signal is illustrated in Figure 3.6. Because the differential amplifier strips off or rejects the common mode signal, this circuit configuration is often employed to strip DC or injected common mode noise off a signal.

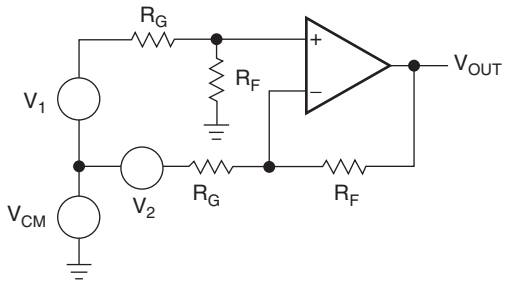


Figure 3.6: Differential amplifier with common mode input signal.

The disadvantage of this circuit is that the two input impedances cannot be matched when it functions as a differential amplifier, thus the two or three op amp versions of this circuit specially designed for high performance applications require matched input impedances.

3.6 Complex Feedback Networks

When complex networks are put into the feedback loop, the circuits get harder to analyze, because the simple gain equations cannot be used. The usual technique is to write and solve node or loop equations. There is only one input voltage, so superposition is not of use, but Thevenin's theorem can be used, as is shown in the example problem that follows.

Sometimes, it is desirable to have a low resistance path to ground in the feedback loop. Standard inverting op amps cannot do this when the driving circuit sets the input resistor value and the gain specification sets the feedback resistor value. Inserting a T network in the feedback loop (Figure 3.7) yields a degree of freedom that enables both specifications to be met with a low DC resistance path in the feedback loop.

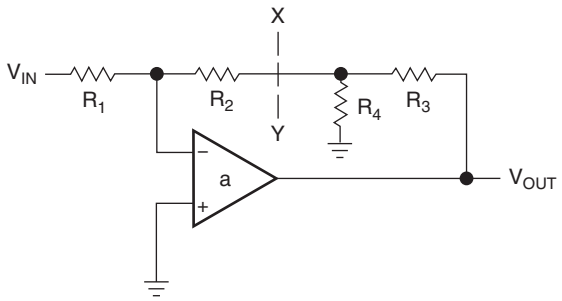


Figure 3.7: T network in feedback loop.

Break the circuit at point *X*–*Y*, stand on the terminals looking into R_4, and calculate the Thevenin equivalent voltage as shown in Equation (3.15). The Thevenin equivalent impedance is calculated in Equation (3.16).

$$V_{TH} = V_{OUT}\frac{R_4}{R_3 + R_4} \tag{3.15}$$

$$R_{TH} = R_3 \| R_4 \tag{3.16}$$

Replace the output circuit with the Thevenin equivalent circuit, as shown in Figure 3.8, and calculate the gain with the aid of the inverting gain equation as shown in Equation (3.17):

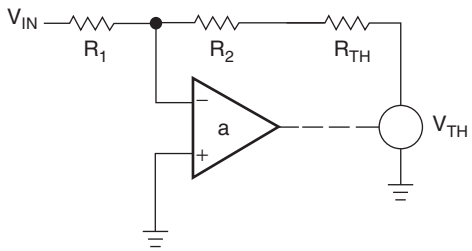


Figure 3.8: Thevenin's theorem applied to a T network.

$$-\frac{V_{TH}}{V_{IN}} = \frac{R_2 + R_{TH}}{R_1} \tag{3.17}$$

Substituting the Thevenin equivalents into Equation (3.17) yields Equation (3.18):

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_{TH}}{R_1}\left(\frac{R_3 + R_4}{R_4}\right) = \frac{R_2 + (R_3 \| R_4)}{R_1}\left(\frac{R_3 + R_4}{R_4}\right) \tag{3.18}$$

Algebraic manipulation yields Equation (3.19):

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_3 + \dfrac{R_2 R_3}{R_4}}{R_1} \tag{3.19}$$

Specifications for the circuit you are required to build are an inverting amplifier with an input resistance of 10 k ($R_G = 10$ k), a gain of 100, and a feedback resistance of 20 k or less. The inverting op amp circuit cannot meet these specifications, because R_F must equal 1000 k. Inserting a T network with $R_2 = R_4 = 10$ k and $R_3 = 485$ k approximately meets the specifications.

3.7 Video Amplifiers

Video signals contain high frequencies, and they use coaxial cable to transmit and receive signals. The cable connecting these circuits has a characteristic impedance of 75 Ω. To prevent reflections, which cause distortion and ghosting, the input and output circuit impedances must match the 75 Ω cable.

Matching the input impedance is simple for a noninverting amplifier, because its input impedance is very high; just make $R_{IN} = 75$ Ω. R_F and R_G can be selected as high values, in the hundreds of ohms range, so that they have minimal effect on the impedance of the input or output circuit. A matching resistor, R_M, is placed in series with the op amp output to raise its output impedance to 75 Ω; a terminating resistor, R_T, is placed at the input of the next stage to match the cable (Figure 3.9).

The matching and terminating resistors are equal in value, and they form a voltage divider of 1/2 because R_T is not loaded. Very often, R_F is selected equal to R_G so that the op amp gain equals 2. Then the system gain, which is the op amp gain multiplied by the divider gain, is equal to 1 ($2 \times 1/2 = 1$).

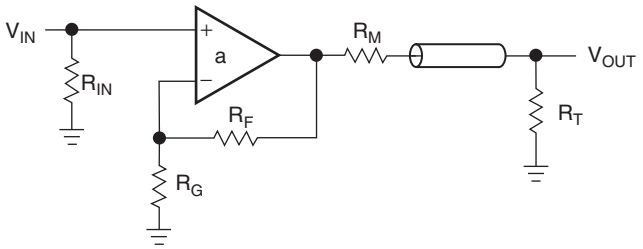


Figure 3.9: Video amplifier.

3.8 Capacitors

Capacitors are a key component in a circuit designer's tool kit; therefore, a short discussion on evaluating their affect on circuit performance is in order. Capacitors have an impedance of $X_C = 1/2\pi fC$. Note that, when the frequency is zero, the capacitive impedance (also known as *reactance*) is infinite; and when the frequency is infinite, the capacitive impedance is zero. These end points are derived from the final value theorem, and they are used to get a rough idea of the effect of a capacitor. When a capacitor is used with a resistor, they form what is called a *break point*. Without going into complicated math, just accept that the break frequency occurs at $f = 1/(2\pi R_C)$ and the gain is –3 dB at the break frequency.

The low pass filter circuit shown in Figure 3.10 has a capacitor in parallel with the feedback resistor. The gain for the low pass filter is given in Equation (3.20):

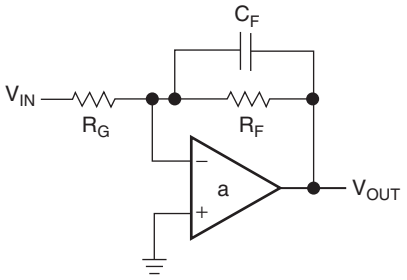


Figure 3.10: Low pass filter.

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = -\frac{X_C \| R_F}{R_G} \tag{3.20}$$

At very low frequencies $X_C \Rightarrow \infty$, so R_F dominates the parallel combination in Equation (3.20), and the capacitor has no effect. The gain at low frequencies is $-R_F/R_G$. At very high frequencies $X_C \Rightarrow 0$, so the feedback resistor is shorted out, thus reducing the circuit gain to zero. At the frequency where $X_C = R_F$, the gain is reduced by $\sqrt{2}$ because complex impedances in parallel equal half the vector sum of both impedances.

Connecting the capacitor in parallel with R_G, where it has the opposite effect, makes a high pass filter (Figure 3.11). Equation (3.21) gives the equation for the high pass filter.

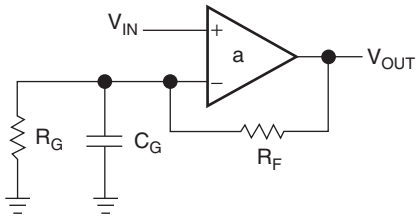


Figure 3.11: High pass filter.

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = 1 + \frac{R_F}{X_C \| R_G} \tag{3.21}$$

At very low frequencies $X_C \Rightarrow \infty$, so R_G dominates the parallel combination in Equation (3.21), and the capacitor has no effect. The gain at low frequencies is $1 + R_F/R_G$. At very high frequencies, $X_C \Rightarrow 0$, so the gain setting resistor is shorted out, thus increasing the circuit gain to maximum.

This simple technique is used to predict the form of a circuit transfer function rapidly. Better analysis techniques are presented in later chapters for those applications requiring more precision.

3.9 Why an Ideal Op Amp Would Destroy the Known Universe

An understanding of op amp parameters, as explained in Chapter 13, is not required but would be helpful at this point. An ideal op amp has the following specifications:

- It draws no supply current and therefore has no power supplies. Hence, it doesn't even have to be turned on to be dangerous!

- It has no V_{OH} and V_{OL} limitations because it has no power supplies. Therefore, its output voltage swings from $\pm\infty$ V.
- It has zero output resistance, and therefore it is capable of supplying infinite current at each voltage extreme.
- It has infinite gain, and therefore the slightest input signal would allow it to swing to positive and negative infinite voltage (without feedback components, that is).
- It has infinite slew rate and therefore would swing to either rail—both equally destructive—instantly.

Therefore, an ideal op amp, just lying on the table with no power applied, would instantly take a quantum difference between its positive and negative terminals and amplify that difference to an infinite voltage output at infinite current. The resulting surge of power would be a sphere of destruction radiating out from the op amp at the speed of light!

This somewhat humorous analysis is included to drive home a few points:

1. If the ideal op amp model is employed, the engineer must also know how real world op amp parameters degrade and alter the ideal op amp model. An ideal op amp model is a useful tool for initial phases of simulation and analysis but does not adequately explain real world op amp behavior.
2. All of this mathematical analysis can be boiled down to a simple concept: *The op amp will do whatever it has to do at its output to equalize the voltages at its inputs*. This is the entire content of this book, distilled to its simplest form. This fundamental concept can be used to derive all of the behavior of all op amp circuits in all applications. Of course, it must be filtered through statement 1 for real world op amps.
3. A very astute analog design engineer might see one fallacy in this "death star" scenario: "Where is the return path?" When a single ended op amp is employed, the return path is to ground. But when no power supplies are utilized, there is no ground! So, to be technically correct, the only type of ideal op amp that would destroy the known universe is a fully differential type, where the return for one output is the other output. This book explains in detail the subject of proper return to ground for single ended op amps and single ended op amps configured in single supply operation.

3.10 Summary

When the proper assumptions are made, the analysis of op amp circuits is straightforward. These assumptions, which include zero input current, zero input offset voltage, and infinite gain, are realistic assumptions because the new op amps make them essentially true in most real world applications.

When the signal comprises low frequencies, the gain assumption is valid because op amps have very high gain at low frequencies. When CMOS op amps are used, the input current is in the femtoamp range; close enough to zero for most applications. Laser trimmed input circuits reduce the input offset voltage to a few microvolts; close enough to zero for most applications. The ideal op amp is becoming real, especially for undemanding applications.

CHAPTER 4

Single Supply Op Amp Design Techniques

Ron Mancini

4.1 Single Supply versus Dual Supply

The previous chapter assumed that all op amps were powered from dual or split supplies, and this is not the case in today's world of portable, battery powered equipment. When op amps are powered from dual supplies (see Figure 4.1), the supplies are normally equal in magnitude, opposing in polarity, and the center tap of the supplies is connected to ground. Any input sources connected to ground are automatically referenced to the center of the supply voltage, so the output voltage is automatically referenced to ground.

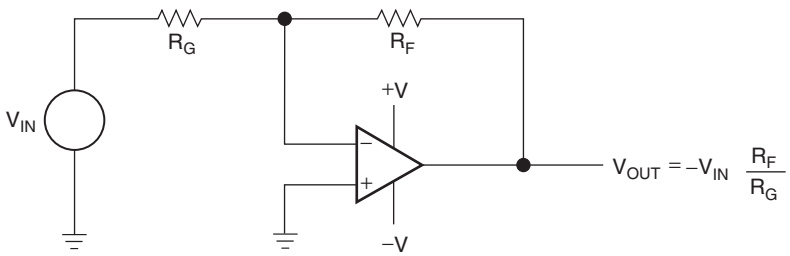


Figure 4.1: Split supply op amp circuit.

Single supply systems do not have the convenient ground reference of dual supply systems, therefore biasing must be employed to ensure that the output voltage swings between the correct voltages. Input sources connected to ground are actually connected

to a supply rail in single supply systems. This is analogous to connecting a dual supply input to the minus power rail. This requirement for biasing the op amp inputs to achieve the desired output voltage swing complicates single supply designs.

When the signal source is not referenced to ground (see Figure 4.2), the voltage difference between ground and the reference voltage is amplified along with the signal. Unless the reference voltage was inserted as a bias voltage, and such is not the case when the input signal is connected to ground, the reference voltage must be stripped from the signal so that the op amp can provide maximum dynamic range.

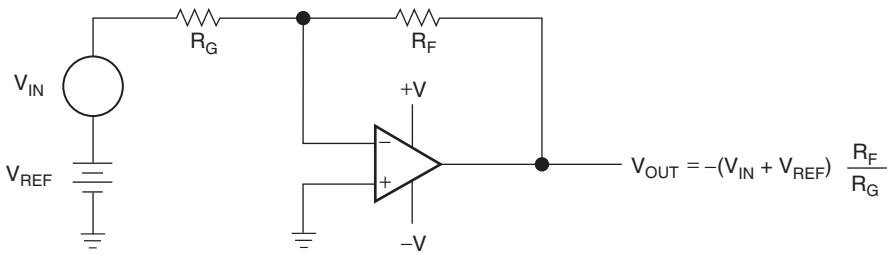


Figure 4.2: Split supply op amp circuit with reference voltage input.

An input bias voltage is used to eliminate the reference voltage when it must not appear in the output voltage (see Figure 4.3). The voltage, V_{REF}, is in both input circuits; hence it is named a *common mode voltage*. Voltage feedback op amps reject common mode voltages because their input circuit is constructed with a differential amplifier (chosen because it has natural common mode voltage rejection capabilities).

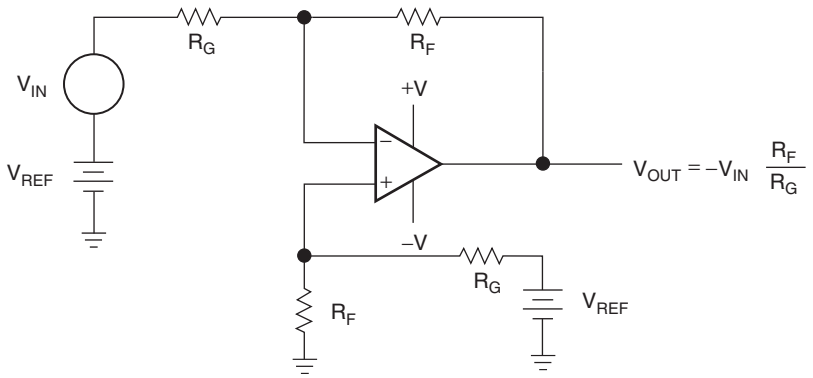


Figure 4.3: Split supply op amp circuit with common mode voltage.

When signal sources are referenced to ground, single supply op amp circuits exhibit a large input common mode voltage. Figure 4.4 shows a single supply op amp circuit that has its input voltage referenced to ground. The input voltage is not referenced to the midpoint of the supplies, as in a split supply application, rather it is referenced to the lower power supply rail. This circuit does not operate when the input voltage is positive, because the output voltage would have to go to a negative voltage, hard to do with a positive supply. It operates marginally with small negative input voltages, because most op amps do not function well when the inputs are connected to the supply rails.

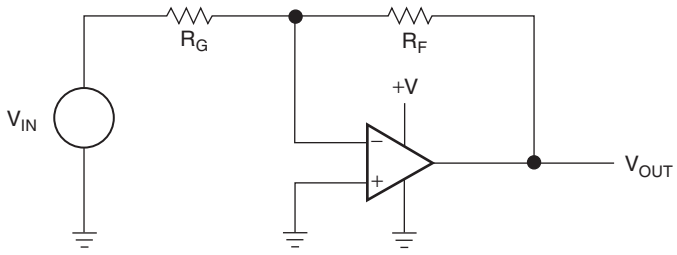


Figure 4.4: Single supply op amp circuit.

The constant requirement to account for inputs connected to ground or different reference voltages makes it difficult to design single supply op amp circuits. Unless otherwise specified, all op amp circuits discussed in this chapter are single supply circuits. The single supply may be wired with the negative or positive lead connected to ground, but as long as the supply polarity is correct, the wiring does not affect circuit operation.

Use of a single supply limits the polarity of the output voltage. When the supply voltage $V_{CC} = 10$ V, the output voltage is limited to the range $0 \leq V_{OUT} \leq 10$. This limitation precludes negative output voltages when the circuit has a positive supply voltage, but it does not preclude negative input voltages when the circuit has a positive supply voltage. As long as the voltage on the op amp input leads does not become negative, the circuit can handle negative input voltages.

Beware of working with negative (positive) input voltages when the op amp is powered from a positive (negative) supply because op amp inputs are highly susceptible to reverse voltage breakdown. Also, ensure that all possible startup conditions do not reverse bias the op amp inputs when the input and supply voltage are of opposite polarity.

4.2 Circuit Analysis

The complexities of single supply op amp design are illustrated with the following example. Note that the biasing requirement complicates the analysis by presenting several nonrealizable conditions. It is best to wade through this material to gain an understanding of the problem, especially since a cookbook solution is given later in this chapter. The previous chapter assumed that the op amps were ideal, and this chapter starts to deal with op amp deficiencies. The input and output voltage swings of many op amps are limited, as shown in Figure 4.7, but if one designs with the selected rail to rail op amps, the input/output swing problems are minimized. The inverting circuit shown in Figure 4.5 is analyzed first.

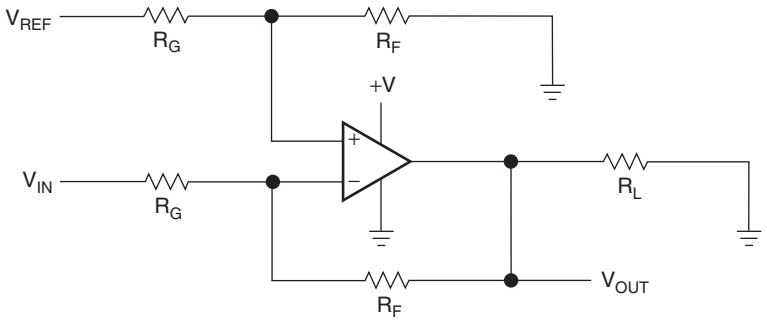


Figure 4.5: Inverting op amp.

Equation (4.1) is written with the aid of superposition and simplified algebraically to acquire Equation (4.2):

$$V_{\text{OUT}} = V_{\text{REF}}\left(\frac{R_F}{R_G + R_F}\right)\left(\frac{R_F + R_G}{R_G}\right) - V_{\text{IN}}\frac{R_F}{R_G} \tag{4.1}$$

$$V_{\text{OUT}} = (V_{\text{REF}} - V_{\text{IN}})\frac{R_F}{R_G} \tag{4.2}$$

As long as the load resistor, R_L, has a large value, it does not enter into the circuit calculations, but it can introduce some second order effects, such as limiting the output voltage swings. Equation (4.3) is obtained by setting V_{REF} equal to V_{IN}, and there is no output voltage from the circuit regardless of the input voltage. The author unintentionally designed a few of these circuits before he created an orderly method of op amp circuit design. Actually, a real circuit has a small output voltage equal to the lower transistor saturation voltage, which is about 150 mV for a TLC07X.

$$V_{OUT} = (V_{REF} - V_{IN})\frac{R_F}{R_G} = (V_{IN} - V_{IN})\frac{R_F}{R_G} = 0 \tag{4.3}$$

When $V_{REF} = 0$, $V_{OUT} = -V_{IN}(R_F/R_G)$, there are two possible solutions to Equation (4.2). First, when V_{IN} is any positive voltage, V_{OUT} should be negative voltage. The circuit cannot achieve a negative voltage with a positive supply, so the output saturates at the lower power supply rail. Second, when V_{IN} is any negative voltage, the output spans the normal range according to Equation (4.5):

$$V_{IN} \geq 0, \quad V_{OUT} = 0 \tag{4.4}$$

$$V_{IN} \leq 0, \quad V_{OUT} = |V_{IN}|\frac{R_F}{R_G} \tag{4.5}$$

When V_{REF} equals the supply voltage, V_{CC}, we obtain Equation (4.6). In Equation (4.6), when V_{IN} is negative, V_{OUT} should exceed V_{CC}; that is impossible, so the output saturates. When V_{IN} is positive, the circuit acts as an inverting amplifier.

$$V_{OUT} = (V_{CC} - V_{IN})\frac{R_F}{R_G} \tag{4.6}$$

The transfer curve for the circuit shown in Figure 4.6 ($V_{CC} = 5$ V, $R_G = R_F = 100$ kΩ, $R_L = 10$ kΩ) is shown in Figure 4.7.

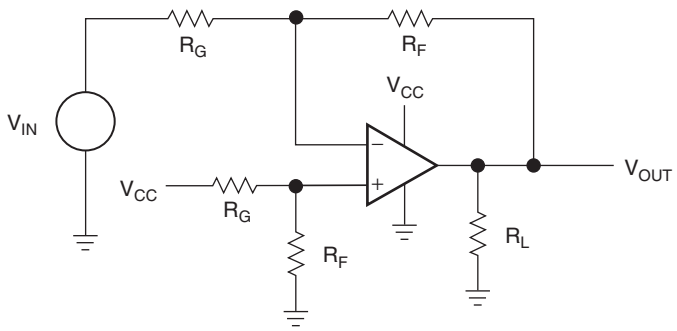


Figure 4.6: Inverting op amp with V_{CC} bias.

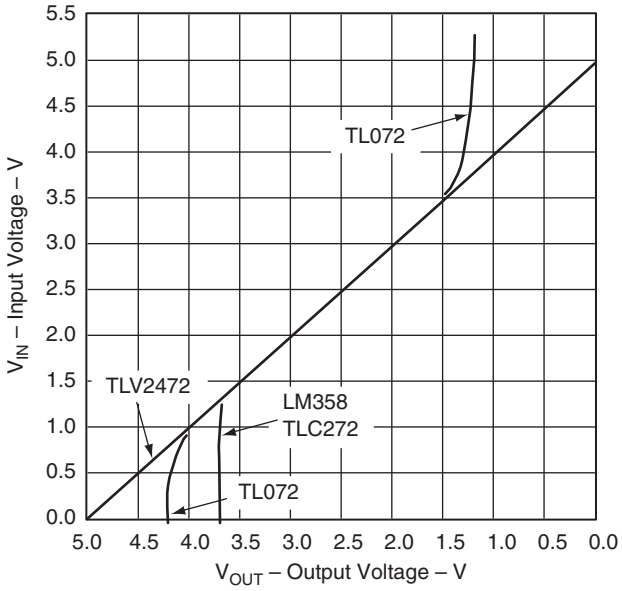


Figure 4.7: Transfer curve for an inverting op amp with V_{CC} bias.

Four op amps were tested in the circuit configuration shown in Figure 4.6. Three of the old generation op amps (LM358, TL07X, and TLC272) had output voltage spans of 2.3 V to 3.75 V. This performance does not justify the ideal op amp assumption made in the previous chapter unless the output voltage swing is severely limited. Limited output or input voltage swing is one of the worst deficiencies a single supply op amp can have, because the limited voltage swing limits the circuit's dynamic range. Also, the limited voltage swing frequently results in distortion of large signals. The fourth op amp tested was the newer TLV247X, which was designed for rail to rail operation in single supply circuits. The TLV247X plotted a perfect curve (results limited by the instrumentation), and it amazed the author with a textbook performance that justifies the use of ideal assumptions. Some of the older op amps must limit their transfer equation as shown in Equation (4.7):

$$V_{\text{OUT}} = (V_{\text{CC}} - V_{\text{IN}})\frac{R_F}{R_G} \text{ for } V_{\text{OH}} \geq V_{\text{OUT}} \geq V_{\text{OL}} \tag{4.7}$$

The noninverting op amp circuit is shown in Figure 4.8. Equation (4.8) is written with the aid of superposition and simplified algebraically to acquire Equation (4.9):

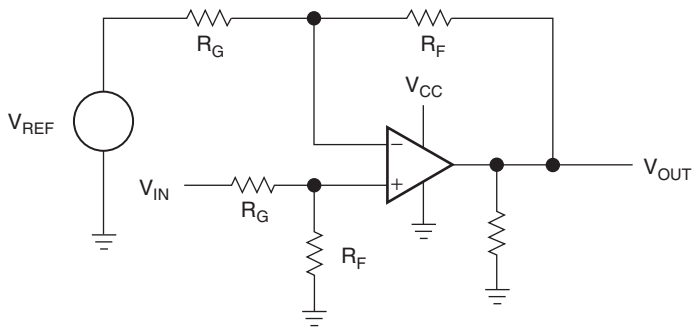


Figure 4.8: Noninverting op amp.

$$V_{\text{OUT}} = V_{\text{IN}}\left(\frac{R_F}{R_G + R_F}\right)\left(\frac{R_F + R_G}{R_G}\right) - V_{\text{REF}}\frac{R_F}{R_G} \tag{4.8}$$

$$V_{\text{OUT}} = (V_{\text{IN}} - V_{\text{REF}})\frac{R_F}{R_G} \tag{4.9}$$

When $V_{\text{REF}} = 0$, $V_{\text{OUT}} = V_{\text{IN}}\frac{R_F}{R_G}$, two circuit solutions are possible. First, when V_{IN} is a negative voltage, V_{OUT} must be a negative voltage. The circuit cannot achieve a negative output voltage with a positive supply, so the output saturates at the lower power supply rail. Second, when V_{IN} is a positive voltage, the output spans the normal range, as shown by Equation (4.11):

$$V_{\text{IN}} \leq 0, \quad V_{\text{OUT}} = 0 \tag{4.10}$$

$$V_{\text{IN}} \geq 0, \quad V_{\text{OUT}} = V_{\text{IN}} \tag{4.11}$$

The noninverting op amp circuit is shown in Figure 4.8 with $V_{\text{CC}} = 5$ V, $R_G = R_F = 100$ kΩ, and $R_L = 10$ kΩ. The transfer curve for this circuit is shown in Figure 4.9; a TLV247X serves as the op amp.

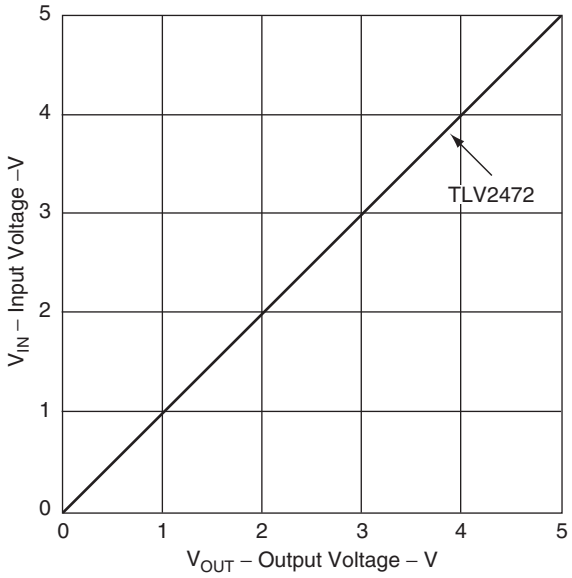


Figure 4.9: Transfer curve for a noninverting op amp.

There are many possible variations of inverting and noninverting circuits. At this point, many designers analyze these variations, hoping to stumble on the one that solves the circuit problem. Rather than analyze each circuit, it is better to learn how to employ simultaneous equations to render specified data into equation form. When the form of the desired equation is known, a circuit that fits the equation is chosen to solve the problem. The resulting equation must be a straight line, therefore only four solutions are possible.

4.3 Simultaneous Equations

Taking an orderly path to developing a circuit that works the first time starts here: Follow these steps until the equation of the op amp is determined. Use the specifications given for the circuit coupled with simultaneous equations to determine what form the op amp equation must have. Go to the section that illustrates that equation form (called a *case*), solve the equation to determine the resistor values, and you have a working solution.

A linear op amp transfer function is limited to the equation of a straight line:

$$y = \pm mx \pm b \tag{4.12}$$

The equation of a straight line has four possible solutions, depending on the sign of m, the slope, and b, the intercept; therefore simultaneous equations yield solutions in four forms. Four circuits must be developed, one for each form of the equation of a straight line. The four equations, cases, or forms of a straight line are given in Equations (4.13) through (4.16), where electronic terminology has been substituted for math terminology:

$$V_{OUT} = +mV_{IN} + b \tag{4.13}$$

$$V_{OUT} = +mV_{IN} - b \tag{4.14}$$

$$V_{OUT} = -mV_{IN} + b \tag{4.15}$$

$$V_{OUT} = -mV_{IN} - b \tag{4.16}$$

Given a set of two data points for V_{OUT} and V_{IN}, simultaneous equations are solved to determine m and b for the equation that satisfies the given data. The signs of m and b determine the type of circuit required to implement the solution. The given data are derived from the specifications; that is, a sensor output signal ranging from 0.1 V to 0.2 V must be interfaced into an analog to digital converter that has an input voltage range of 1 V to 4 V. These data points ($V_{OUT} = 1$ V at $V_{IN} = 0.1$ V, $V_{OUT} = 4$ V at $V_{IN} = 0.2$ V) are inserted into Equation (4.13), as shown in Equations (4.17) and (4.18), to obtain m and b for the specifications:

$$1 = m(0.1) + b \tag{4.17}$$

$$4 = m(0.2) + b \tag{4.18}$$

Multiply Equation (4.17) by 2 and subtract it from Equation (4.18):

$$2 = m(0.2) + 2b \tag{4.19}$$

$$b = -2 \tag{4.20}$$

After algebraic manipulation of Equation (4.17), substitute Equation (4.20) into Equation (4.17) to obtain (Equation 4.21):

$$m = \frac{2 + 1}{0.1} = 30 \tag{4.21}$$

Now m and b are substituted back into Equation (4.13), yielding Equation (4.22):

$$V_{OUT} = 30\ V_{IN} - 2 \tag{4.22}$$

Note: Although Equation (4.13) was the starting point, the form of Equation (4.22) is identical to the format of Equation (4.14). The specifications or given data determine the signs of m and b; and starting with Equation (4.13), the final equation form is discovered after m and b are calculated. The next step required to complete the problem solution is to develop a circuit that has $m = 30$ and $b = -2$. Circuits were developed for Equations (4.13) through (4.16), and they are given under the headings Case 1 through Case 4, respectively. Different circuits yield the same equations, but these circuits were selected because they require no negative references.

4.3.1 Case 1. $V_{OUT} = mV_{IN} + b$

The circuit configuration that yields a solution for Case 1 is shown in Figure 4.10. The figure includes two 0.01 µF capacitors. These capacitors, called *decoupling capacitors*, are included to reduce noise and provide increased noise immunity. Sometimes two 0.01 µF capacitors serve this purpose, sometimes more extensive filtering is needed, and sometimes one capacitor serves this purpose. Special attention must be paid to the regulation and noise content of V_{CC} when V_{CC} is used as a reference, because some portion of the noise content of V_{CC} is multiplied by the circuit gain.

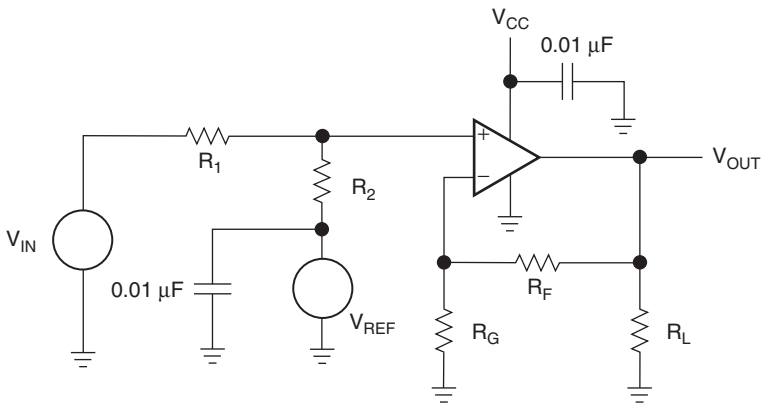


Figure 4.10: Schematic for Case 1, $V_{OUT} = +mV_{IN} + b$.

The circuit equation is written using the voltage divider rule and superposition:

$$V_{OUT} = V_{IN}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{4.23}$$

The equation of a straight line (Case 1) is repeated in Equation (4.24) so comparisons can be made between it and Equation (4.23):

$$V_{OUT} = mV_{IN} + b \tag{4.24}$$

Equating coefficients yields Equations (4.25) and (4.26):

$$m = \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{4.25}$$

$$b = V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{4.26}$$

For example, the circuit specifications are $V_{OUT} = 1$ V at $V_{IN} = 0.01$ V, $V_{OUT} = 4.5$ V at $V_{IN} = 1$ V, $R_L = 10$ k, 5% resistor tolerances, and $V_{CC} = 5$ V. No reference voltage is available, so V_{CC} is used for the reference input, and $V_{REF} = 5$ V. A reference voltage source is left out of the design as a space and cost saving measure, and it sacrifices noise performance, accuracy, and stability performance. Cost is an important specification, but the V_{CC} supply must be specified well enough to do the job. Each step in the subsequent design procedure is included in this analysis to ease learning and increase boredom. Many steps are skipped when subsequent cases are analyzed.

The data are substituted into simultaneous equations:

$$1 = m(0.01) + b \tag{4.27}$$

$$4.5 = m(1.0) + b \tag{4.28}$$

Equation (4.27) is multiplied by 100, Equation (4.29), and Equation (4.28) is subtracted from Equation (4.29) to obtain Equation (4.30):

$$100 = m(1.0) + 100b \tag{4.29}$$

$$b = \frac{95.5}{99} = 0.9646 \tag{4.30}$$

The slope of the transfer function, m, is obtained by substituting b into Equation (4.27):

$$m = \frac{1 - b}{0.01} = \frac{1 - 0.9646}{0.01} = 3.535 \tag{4.31}$$

Now that b and m are calculated, the resistor values can be calculated. Equations (4.25) and (4.26) are solved for the quantity $(R_F + R_G)/R_G$, then they are set equal in Equation (4.32), yielding Equation (4.33):

$$\frac{R_F + R_G}{R_G} = m\left(\frac{R_1 + R_2}{R_2}\right) = \frac{b}{V_{CC}}\left(\frac{R_1 + R_2}{R_1}\right) \tag{4.32}$$

$$R_2 = \frac{3.535}{\frac{0.9646}{5}} R_1 = 18.316 R_1 \tag{4.33}$$

Resistors of 5% tolerance are specified for this design, so we choose $R_1 = 10$ kΩ, and that sets the value of $R_2 = 183.16$ kΩ. The closest 5% resistor value to 183.16 kΩ is 180 kΩ; therefore select $R_1 = 10$ kΩ and $R_2 = 180$ kΩ. Being forced to yield to reality by choosing standard resistor values means that there is an error in the circuit transfer function, because m and b are not exactly the same as calculated. The real world constantly forces compromises into circuit design, but the good circuit designer accepts the challenge and throws money or brains at the challenge. Resistor values closer to the calculated values could be selected by using 1% or 0.5% resistors, but that selection increases cost and violates the design specification. The cost increase is hard to justify except in precision circuits. Using 10 cent resistors with a 10 cent op amp usually is false economy.

The left half of Equation (4.32) is used to calculate R_F and R_G:

$$\frac{R_F + R_G}{R_G} = m\left(\frac{R_1 + R_2}{R_2}\right) = 3.535\left(\frac{180 + 10}{180}\right) = 3.73 \tag{4.34}$$

$$R_F = 2.73R_G \tag{4.35}$$

The resulting circuit equation is

$$V_{OUT} = 3.5V_{IN} + 0.97 \tag{4.36}$$

The gain setting resistor, R_G, is selected as 10 kΩ, and 27 kΩ, the closest 5% standard value is selected for the feedback resistor, R_F. Again, a slight error is involved with standard resistor values. This circuit must have an output voltage swing from 1 V to 4.5 V. The older op amps cannot be used in this circuit, because they lack dynamic range, so the TLV247X family of op amps is selected. The data shown in Figure 4.7 confirm the op amp selection because there is little error. The circuit with the selected component values is shown in Figure 4.11. The circuit was built with the specified components, and the transfer curve is shown in Figure 4.12.

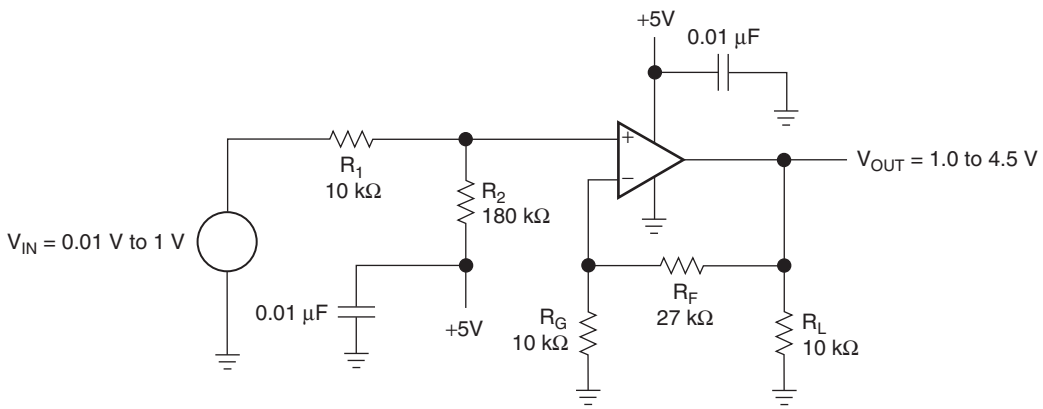


Figure 4.11: Case 1 example circuit.

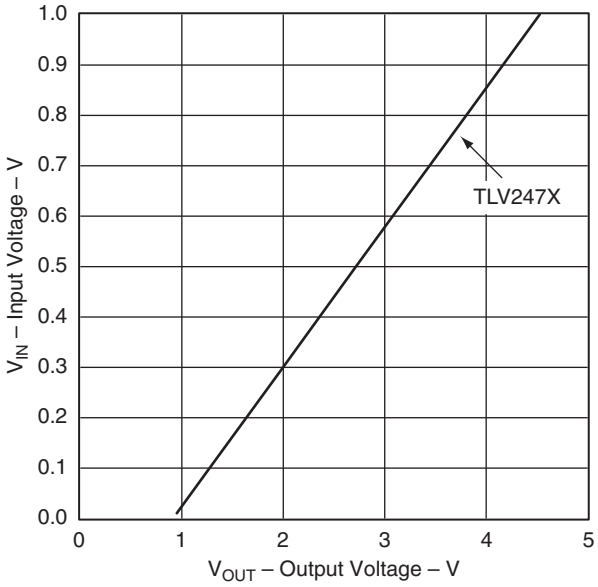


Figure 4.12: Case 1 example circuit measured transfer curve.

The transfer curve shown is a straight line, which means that the circuit is linear. The V_{OUT} intercept is about 0.98 V rather than 1 V as specified, and this is excellent performance, considering that the components were selected randomly from bins of resistors. Different sets of components would have slightly different slopes because of the resistor tolerances. The TLV247X has input bias currents and input offset voltages, but the effect of these errors is hard to measure on the scale of the output voltage. The output voltage measured 4.53 V when the input voltage was 1 V. Considering the low and high input voltage errors, it is safe to conclude that the resistor tolerances have skewed the gain slightly, but this is still excellent performance for 5% components. Often lab data similar to that shown here is more accurate than the 5% resistor tolerance, but do not fall into the trap of expecting this performance, because you will be disappointed if you do.

The resistors were selected in the kilo-ohm range arbitrarily. The gain and offset specifications determine the resistor ratios, but supply current, frequency response, and op amp drive capability determine their absolute values. The resistor value selection in this design is high because modern op amps do not have input current offset problems and they yield reasonable frequency response. If higher frequency response is

demanded, the resistor values must decrease, and resistor value decreases reduce input current errors, while supply current increases. When the resistor values get low enough, it becomes hard for another circuit, or possibly the op amp, to drive the resistors.

4.3.2 Case 2. $V_{OUT} = +mV_{IN} - b$

The circuit shown in Figure 4.13 yields a solution for Case 2. The circuit equation is obtained by taking the Thevenin equivalent circuit looking into the junction of R_1 and R_2. After the R_1, R_2 circuit is replaced with the Thevenin equivalent circuit, the gain is calculated with the ideal gain equation, Equation (4.37):

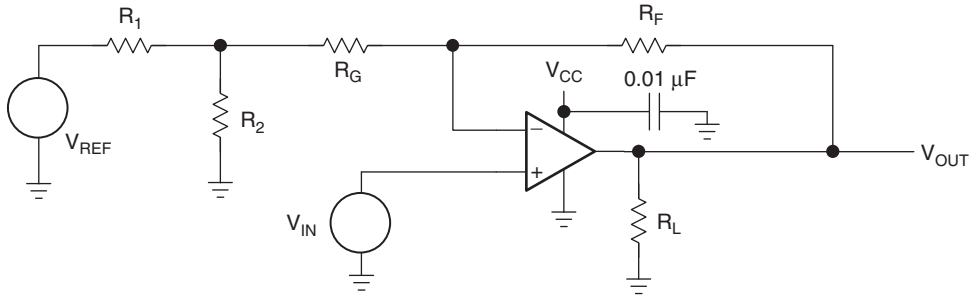


Figure 4.13: Schematic for Case 2, $V_{OUT} = +mV_{IN} - b$.

$$V_{OUT} = V_{IN}\left(\frac{R_F + R_G + R_1||R_2}{R_G + R_1||R_2}\right) - V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1||R_2}\right) \tag{4.37}$$

Comparing the terms in Equations (4.37) and (4.14) enables the extraction of m and b:

$$m = \frac{R_F + R_G + R_1||R_2}{R_G + R_1||R_2} \tag{4.38}$$

$$|b| = V_{REF}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1||R_2}\right) \tag{4.39}$$

The specifications for an example design are $V_{OUT} = 1.5$ V at $V_{IN} = 0.2$ V, $V_{OUT} = 4.5$ V at $V_{IN} = 0.5$ V, $V_{REF} = V_{CC} = 5$ V, $R_L = 10$ kΩ, and 5% resistor tolerances. The simultaneous equations follow:

$$1.5 = 0.2m + b \tag{4.40}$$

$$4.5 = 0.5m + b \tag{4.41}$$

From these equations, we find that $b = –0.5$ and $m = 10$. Making the assumption that $R_1 \| R_2 \ll RG$ simplifies the calculations of the resistor values:

$$m = 10 = \frac{R_F + R_G}{R_G} \tag{4.42}$$

$$R_F = 9R_G \tag{4.43}$$

Let $R_G = 20$ kΩ and $R_F = 180$ kΩ:

$$b = V_{CC}\left(\frac{R_F}{R_G}\right)\left(\frac{R_2}{R_1 + R_2}\right) = 5\left(\frac{180}{20}\right)\left(\frac{R_2}{R_1 + R_2}\right) \tag{4.44}$$

$$R_1 = \frac{1 - 0.01111}{0.01111}R_2 = 89\ R_2 \tag{4.45}$$

Select $R_2 = 0.82$ kΩ and $R_1 = 72.98$ kΩ. Since 72.98 kΩ is not a standard 5% resistor value, R_1 is selected as 75 kΩ. The difference between the selected and calculated value of R_1 has about a 3% effect on b, and this error shows up in the transfer function as an intercept rather than a slope error. The parallel resistance of R_1 and R_2 is approximately 0.82 kΩ, and this is much less than R_G, which is 20 kΩ, thus the earlier assumption that $R_G \gg R_1 \| R_2$ is justified. R_2 could have been selected as a smaller value, but the smaller values yielded poor standard 5% values for R_1. The final circuit is shown in Figure 4.14 and the measured transfer curve for this circuit is shown in Figure 4.15.

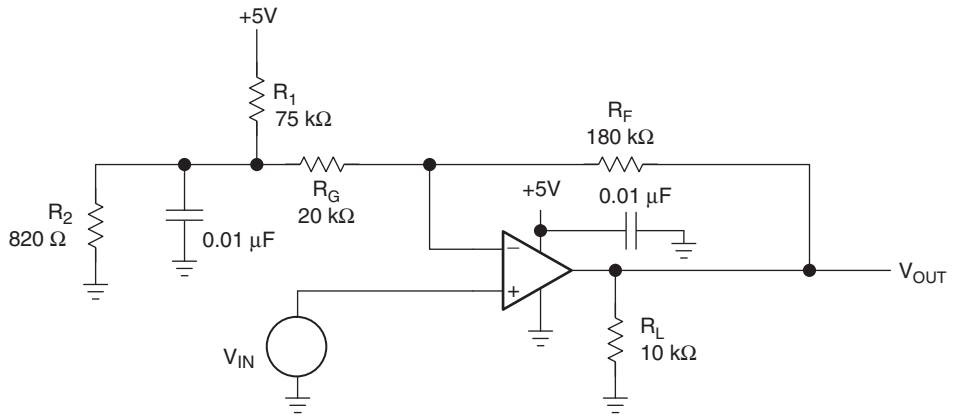


Figure 4.14: Case 2 example circuit.

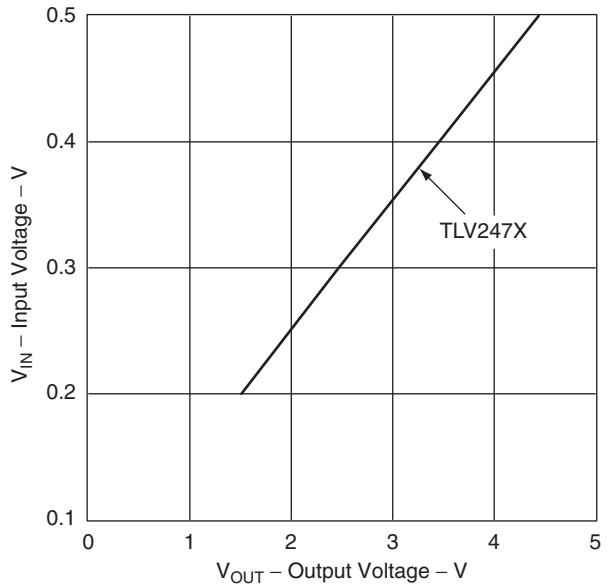


Figure 4.15: Case 2 example circuit measured transfer curve.

The TLV247X was used to build the test circuit because of its wide dynamic range. The transfer curve plots very close to the theoretical curve; the direct result of using a high performance op amp.

4.3.3 Case 3. $V_{OUT} = -mV_{IN} + b$

The circuit shown in Figure 4.16 yields the transfer function desired for Case 3.

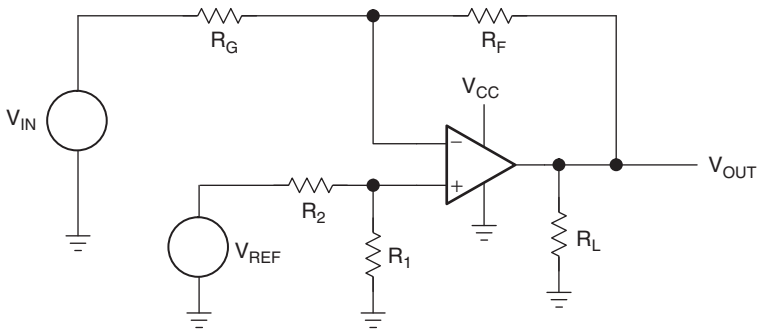


Figure 4.16: Schematic for Case 3, $V_{OUT} = -mV_{IN} + b$.

The circuit equation is obtained with superposition:

$$V_{\text{OUT}} = -V_{\text{IN}}\left(\frac{R_F}{R_G}\right) + V_{\text{REF}}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{4.46}$$

Comparing terms between Equations (4.45) and (4.15) enables the extraction of m and b:

$$|m| = \frac{R_F}{R_G} \tag{4.47}$$

$$b = V_{\text{REF}}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{4.48}$$

The design specifications for an example circuit are $V_{\text{OUT}} = 1$ V at $V_{\text{IN}} = -0.1$ V, $V_{\text{OUT}} = 6$ V at $V_{\text{IN}} = -1$ V, $V_{\text{REF}} = V_{\text{CC}} = 10$ V, $R_L = 100\ \Omega$, and 5% resistor tolerances. The supply voltage available for this circuit is 10 V, and this exceeds the maximum allowable supply voltage for the TLV247X. Also, this circuit must drive a

back terminated cable that looks like two 50 Ω resistors connected in series, so the op amp must be able to drive 6/100 = 60 mA. The stringent op amp selection criteria limits the choice to relatively new op amps if ideal op amp equations are going to be used. The TLC07X has excellent single supply input performance coupled with high output current drive capability, so it is selected for this circuit. The simultaneous equations, Equations (4.49) and (4.50), follow:

$$1 = (-0.1)m + b \tag{4.49}$$

$$6 = (-1)m + b \tag{4.50}$$

From these equations, we find that $b = 0.444$ and $m = -5.6$:

$$|m| = 5.56 = \frac{R_F}{R_G} \tag{4.51}$$

$$R_F = 5.56R_G \tag{4.52}$$

Let $R_G = 10$ kΩ and $R_F = 56.6$ kΩ, which is not a standard 5% value, hence R_F is selected as 56 kΩ:

$$b = V_{CC}\left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_1}{R_1 + R_2}\right) = 10\left(\frac{56 + 10}{10}\right)\left(\frac{R_1}{R_1 + R_2}\right) \tag{4.53}$$

$$R_2 = \frac{66 - 0.4444}{0.4444}R_1 = 147.64R_1 \tag{4.54}$$

The final equation for the example follows:

$$V_{OUT} = -5.56\ V_{IN} + 0.444 \tag{4.55}$$

Select $R_1 = 2$ kΩ and $R_2 = 295.28$ kΩ. Since 295.28 kΩ is not a standard 5% resistor value, R_1 is selected as 300 kΩ. The difference between the selected and calculated values of R_1 has a nearly insignificant effect on b. The final circuit is shown in Figure 4.17, and the measured transfer curve for this circuit is shown in Figure 4.18.

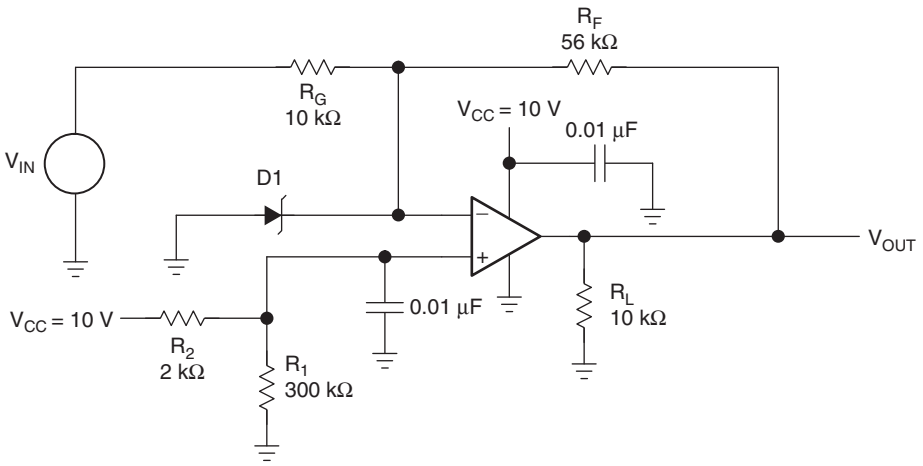


Figure 4.17: Case 3 example circuit.

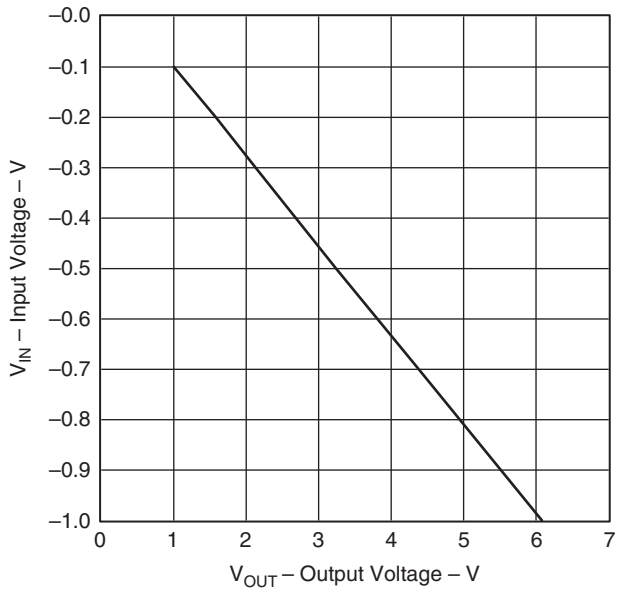


Figure 4.18: Case 3 example circuit measured transfer curve.

As long as the circuit works normally, there are no problems handling the negative voltage input to the circuit, because the inverting lead of the TLC07X is at a positive voltage. The positive op amp input lead is at a voltage of approximately 65 mV, and normal op amp operation keeps the inverting op amp input lead at the same voltage because of the assumption that the error voltage is zero. When V_{CC} is powered down while there is a negative voltage on the input circuit, most of the negative voltage appears on the inverting op amp input lead.

The most prudent solution is to connect the diode, $D1$, with its cathode on the inverting op amp input lead and its anode at ground. If a negative voltage gets on the inverting op amp input lead, it is clamped to ground by the diode. Select the diode type as germanium or Schottky so the voltage drop across the diode is about 200 mV; this small voltage does not harm most op amp inputs. As a further precaution, R_G can be split into two resistors with the diode inserted at the junction of the two resistors. This places a current limiting resistor between the diode and the inverting op amp input lead.

4.3.4 Case 4. $V_{OUT} = -mV_{IN} - b$

The circuit shown in Figure 4.19 yields a solution for Case 4. The circuit equation is obtained by using superposition to calculate the response to each input. The individual responses to V_{IN} and V_{REF} are added to obtain Equation (4.56):

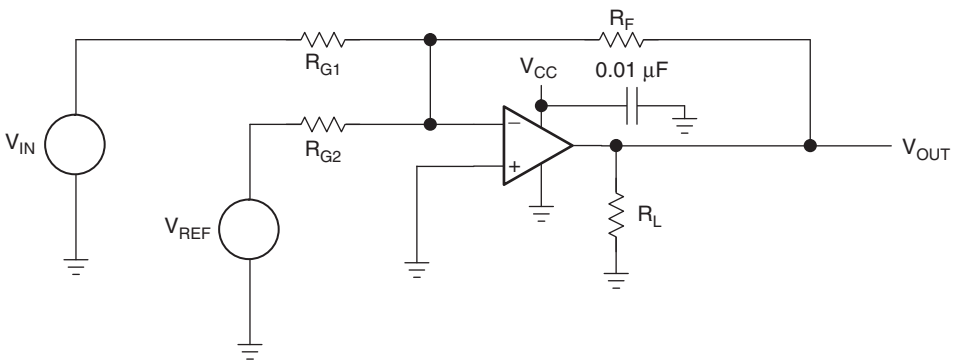


Figure 4.19: Schematic for Case 4, $V_{OUT} = -mV_{IN} - b$.

$$V_{OUT} = -V_{IN}\frac{R_F}{R_{G1}} - V_{REF}\frac{R_F}{R_{G2}} \tag{4.56}$$

Comparing terms in Equations (4.56) and (4.16) enables the extraction of m and b:

$$|m| = \frac{R_F}{R_{G1}} \tag{4.57}$$

$$|b| = V_{\text{REF}} \frac{R_F}{R_{G2}} \tag{4.58}$$

The design specifications for an example circuit are $V_{\text{OUT}} = 1$ V at $V_{\text{IN}} = -0.1$ V, $V_{\text{OUT}} = 5$ V at $V_{\text{IN}} = -0.3$ V, $V_{\text{REF}} = V_{\text{CC}} = 5$ V, $R_L = 10$ kΩ, and 5% resistor tolerances. The simultaneous Equations (4.59) and (4.60) follow:

$$1 = (-0.1)m + b \tag{4.59}$$

$$5 = (-0.3)m + b \tag{4.60}$$

From these equations, we find that $b = -1$ and $m = -20$. Setting the magnitude of m equal to Equation (4.57) yields Equation (4.61):

$$|m| = 20 = \frac{R_F}{R_{G1}} \tag{4.61}$$

$$R_F = 20R_{G1} \tag{4.62}$$

Let $R_{G1} = 1$ kΩ and $R_F = 20$ kΩ:

$$|b| = V_{\text{CC}} \left(\frac{R_F}{R_{G1}} \right) = 5 \left(\frac{R_F}{R_{G2}} \right) = 1 \tag{4.63}$$

$$R_{G2} = \frac{R_F}{0.2} = \frac{20}{0.2} = 100 \text{ kΩ} \tag{4.64}$$

The final equation for this example is

$$V_{\text{OUT}} = -20\, V_{\text{IN}} - 1 \tag{4.65}$$

The final circuit is shown in Figure 4.20 and the measured transfer curve for this circuit is shown in Figure 4.21.

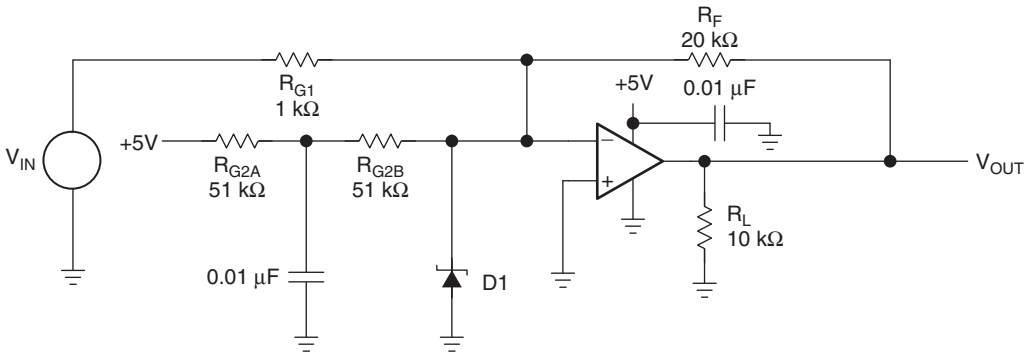


Figure 4.20: Case 4 example circuit.

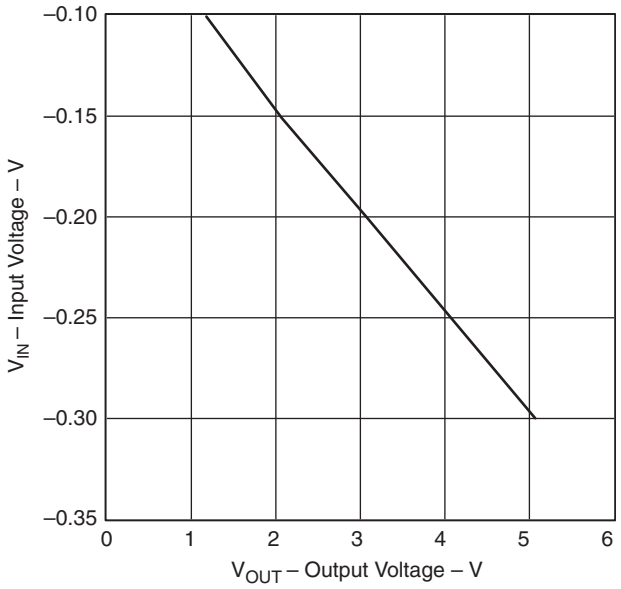


Figure 4.21: Case 4 example circuit measured transfer curve.

The TLV247X was used to build the test circuit because of its wide dynamic range. The transfer curve plots very close to the theoretical curve, and this results from using a high performance op amp.

As long as the circuit works normally, there are no problems handling the negative voltage input to the circuit because the inverting lead of the TLV247X is at a positive voltage. The positive op amp input lead is grounded, and normal op amp operation keeps the inverting op amp input lead at ground because of the assumption that the error voltage is zero when V_{CC} is powered down while there is a negative voltage on the inverting op amp input lead.

The most prudent solution is to connect the diode $D1$ with its cathode on the inverting op amp input lead and its anode at ground. If a negative voltage gets on the inverting op amp input lead, it is clamped to ground by the diode. Select the diode type as germanium or Schottky, so the voltage drop across the diode is about 200 mV; this small voltage does not harm most op amp inputs. R_{G2} is split into two resistors ($R_{G2A} = R_{G2B} = 51$ kΩ) with a capacitor inserted at the junction of the two resistors. This places a power supply filter in series with V_{CC}.

4.4 Summary

Single supply op amp design is more complicated than split supply op amp design, but with a logical design approach, excellent results are achieved. Single supply design used to be considered technically limiting, because older op amps had limited capability. The new op amps, such as the TLC247X, TLC07X, and TLC08X, have excellent single supply parameters; therefore when used in the correct applications, these op amps yield rail to rail performance equal to their split supply counterparts.

Single supply op amp design usually involves some form of biasing, and this requires more thought, so single supply op amp design needs discipline and a procedure. The recommended procedure for single supply op amp design is

- Substitute the specification data into simultaneous equations to obtain m and b (the slope and intercept of a straight line).
- Let m and b determine the form of the circuit.
- Choose the circuit configuration that fits the form.

- Using the circuit equations for the circuit configuration selected, calculate the resistor values.
- Build the circuit, take data, and verify performance.
- Test the circuit for nonstandard operating conditions (circuit power off while interface power is on, over- or underrange inputs, etc.).
- Add protection components as required.
- Retest.

When this procedure is followed, good results follow. As single supply circuit designers expand their horizon, new challenges require new solutions. Remember, the only equation a linear op amp can produce is the equation of a straight line. That equation has only four forms. The new challenges may consist of multiple inputs, common mode voltage rejection, or something different, but this method can be expanded to meet these challenges.

CHAPTER 5

Beyond Case 4

5.1 A Continuum of Applications

The previous chapter presented four cases. Other configurations, like inverting and noninverting gain with no offset, also are covered in previous chapters. While these constitute the vast majority of applications, some additional applications must be addressed. This is best shown in Table 5.1, which lists what has been covered thus far and gives section numbers, not in parentheses, for cases addressed in this chapter. For the sake of brevity, cases with a negative reference are not covered; very few negative voltage references are manufactured or utilized. Also, for the sake of brevity, the equations are not derived, as they were in Chapter 4. They all were developed, however, using the same voltage divider, superposition, and other laws covered in previous chapters.

Table 5.1: The Gain and Offset Matrix

		Offset < 0	**Offset = 0**	**Offset > 0**
Noninverting	Gain > 1	Case 2 (4.3.2)	Noninverting gain (3.2)	Case 1 (4.3.1)
	Gain = 1	5.4	Noninverting buffer	
	Gain < 1		5.2	5.3
	Gain = 0	Voltage references		
Inverting	Gain < –1	5.7	5.5	5.6
	Gain ≥ –1	Case 4 (4.3.4)	Inverting gain (3.3)	Case 3 (4.3.3)

Clearly, some work is yet to be done, particularly in the cases of attenuation. For designers to have a complete set of tools to understand every combination of gain and offset that can come across their path, they need to know more than the applications with which they are most familiar (inverting and noninverting gain and noninverting buffers). The four cases presented in Chapter 4 supplemented the familiar basic circuits, and this chapter presents the rest of the cases. Voltage references, however, are not the subject of this volume.

5.2 Noninverting Attenuator with Zero Offset

The simplest of all the new cases is that of noninverting attenuation (Figure 5.1). It is done by building on the voltage divider principle (Section 2.3) and adding a unity gain op amp buffer.

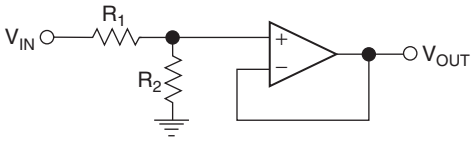


Figure 5.1: Noninverting attenuator: $V_{OUT} = mV_{IN}$, $m = R_2/(R_1 + R_2)$.

5.3 Noninverting Attenuation with Positive Offset

The case of noninverting attenuation with positive offset (Figure 5.2) is a minor variation of the noninverting attenuator, in this case, adding a second input for the reference, which is also attenuated by the voltage divider law.

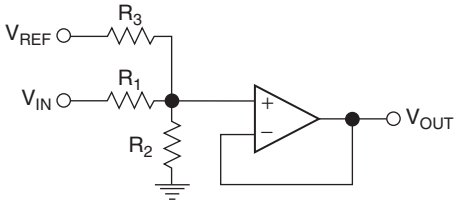


Figure 5.2: Noninverting attenuation with positive offset: $V_{OUT} = mV_{IN} + b$, $m = (1/R_1)/(1/R_1 + 1/R_2 + 1/R_3)$, $b = V_{REF} \times (1/R_3)/(1/R_1 + 1/R_2 + 1/R_3)$.

5.4 Noninverting Attenuation with Negative Offset

The case of noninverting attenuation with negative offset (Figure 5.3) is another slight variation of the noninverting buffer. In this case, instead of applying the reference by superposition to the noninverting input, the reference is applied to the inverting input through an inverting gain stage. The only limitation is that the gain on the reference must be equal to or greater than the stable bandwidth of the op amp.

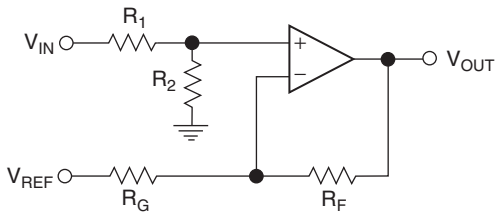


Figure 5.3: Noninverting attenuation with negative offset: $V_{OUT} = mV_{IN} - b$, $m = [R_2/(R_1 + R_2)] \times [1/(R_F/R_G)]$, $b = V_{REF} \times (R_F/R_G)$.

5.5 Inverting Attenuation with Zero Offset

This is the most often misdesigned circuit of all the cases. Many inexperienced designers create an unstable stage by attempting to extrapolate an inverting gain stage to the attenuation case by making R_G greater than R_F. The easiest fix for this problem is to use a voltage divider followed by a unity gain buffer, as described in Section 5.2. If inverting gain is absolutely required, then a similar solution can be implemented by adding a voltage divider to the input of an inverting gain stage.

The balance here is simple enough to understand, see Figure 5.4. R_{IN} is split into R_{INA} and R_{INB}, the sum of which cannot be greater than R_F. By the addition of R_{ATTEN}, the effective attenuation of the stage can be any value desired, while the gain of the stage from R_{INB} and R_F is always between a gain of 1 and 2.

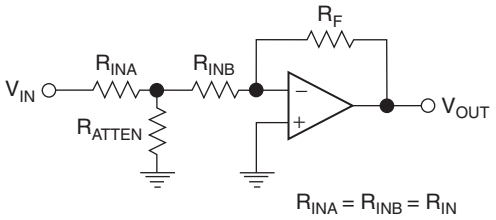


Figure 5.4: Inverting attenuation with zero offset: $V_{OUT} = mV_{IN}$, $m = (R_F \times R_{ATTEN})/[R_{IN} \times (R_{IN} + R_{ATTEN})]$.

5.6 Inverting Attenuation with Positive Offset

If positive offset is needed along with inverting attenuation, a combination of the previous section and Section 5.2 can be employed (Figure 5.5). Just remember that the offset is also attenuated by the same factor as V_{IN}.

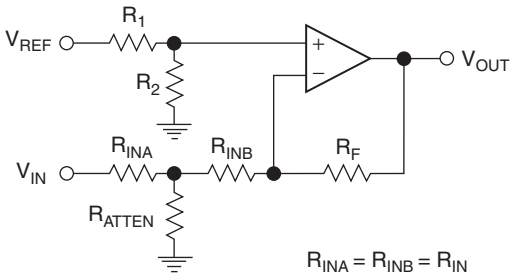


Figure 5.5: Inverting attenuation with positive offset: $V_{OUT} = mV_{IN} + b$, $m = (R_F \times R_{ATTEN})/[R_{IN} \times (R_{IN} + 2R_{ATTEN})]$, $b = V_{REF} \times [R_2/(R_1 + R_2)] \times [1 + R_F/(R_{IN} + R_{IN} \| R_{ATTEN})]$.

5.7 Inverting Attenuation with Negative Offset

If negative offset is needed along with inverting attenuation, the reference can be added to the inverting input using a voltage summation method at the inverting input (Figure 5.6). Again, it is important to have a gain of more than 1 on the V_{REF} gain channel or instability may result.

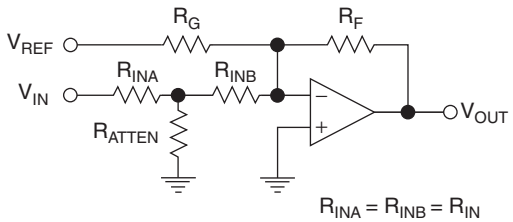


Figure 5.6: Inverting unity gain with negative offset: $V_{OUT} = mV_{IN} - b$, $m = (R_F \times R_{ATTEN})/[R_{IN} \times (R_{IN} + 2R_{ATTEN})]$, $b = V_{REF} \times R_F/R_G$.

5.8 Conclusion

The preceding circuits should provide a way to design just about any interface circuit the designer needs. The primary use of these gain and offset circuits, of course, is the interface between an input voltage and a data converter. The designer may also need to include filtering in their interface circuit, which is covered in later chapters.

CHAPTER 6

Feedback and Stability Theory

Ron Mancini

6.1 Why Study Feedback Theory?

The gain of all op amps decreases as frequency increases, and the decreasing gain results in decreasing accuracy, as the ideal op amp assumption ($a \Rightarrow \infty$) breaks down. In most real op amps, the open loop gain starts to decrease before 10 Hz, so an understanding of feedback is required to predict the closed loop performance of the op amp. The real world application of op amps is feedback controlled and depends on op amp open loop gain at a given frequency. A designer must know theory to be able to predict the circuit response regardless of frequency or open loop gain.

Analysis tools have something in common with medicine, because both can be distasteful but necessary. Medicine often tastes bad or has undesirable side effects, and analysis tools involve lots of hard learning work before they can be applied to yield results. Medicine assists the body in fighting an illness; analysis tools assist the brain in learning and designing feedback circuits.

The descriptions of analysis tools given here are a synopsis of salient points, so they are detailed enough to get you where you are going without any extras. The references, along with thousands of their counterparts, must be consulted when making an in-depth study of the field. Aspirin, home remedies, and good health practice handle the majority of health problems, and these analysis tools solve the majority of circuit problems.

Ideal op amp circuits can be designed without knowledge of feedback analysis tools, but these circuits are limited to low frequencies. Also, an understanding of feedback analysis tools is required to understand AC effects, like ringing and oscillations.

6.2 Block Diagram Math and Manipulations

Electronic systems and circuits are often represented by block diagrams, and block diagrams have a unique algebra and set of transformations [1]. Block diagrams are used because they are a shorthand pictorial representation of the cause and effect relationship between the input and output in a real system. They are a convenient method for characterizing the functional relationships between components. It is not necessary to understand the functional details of a block to manipulate a block diagram.

The input impedance of each block is assumed to be infinite to preclude loading. Also, the output impedance of each block is assumed to be zero to enable high fan out. The systems designer sets the actual impedance levels, but the fan out assumption is valid because the block designers adhere to the system designer's specifications. All blocks multiply the input times the block quantity (see Figure 6.1) unless otherwise

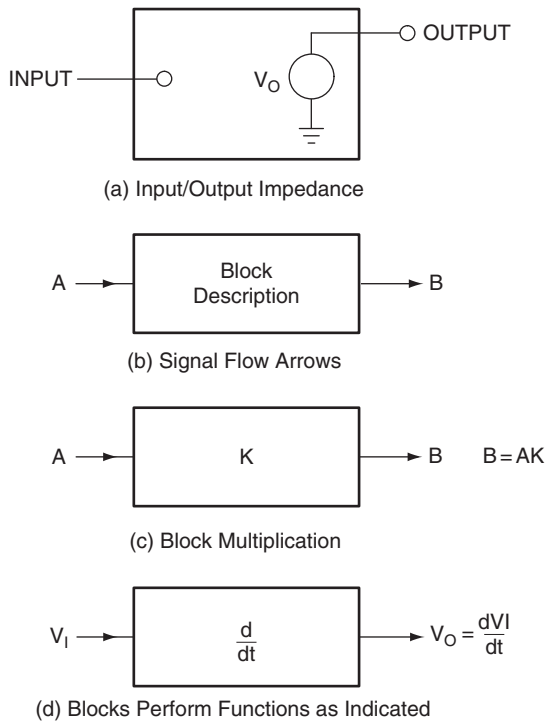


Figure 6.1: Definition of blocks.

specified within the block. The quantity within the block can be a constant, as shown in Figure 6.1(c), or a complex math function involving Laplace transforms. The blocks can perform time based operations such as differentiation and integration.

Adding and subtracting are done in special blocks called *summing points*. Figure 6.2 gives several examples of summing points. Summing points can have unlimited inputs, add or subtract, and have mixed signs, yielding addition and subtraction within a single summing point. Figure 6.3 defines the terms in a typical control system, and Figure 6.4

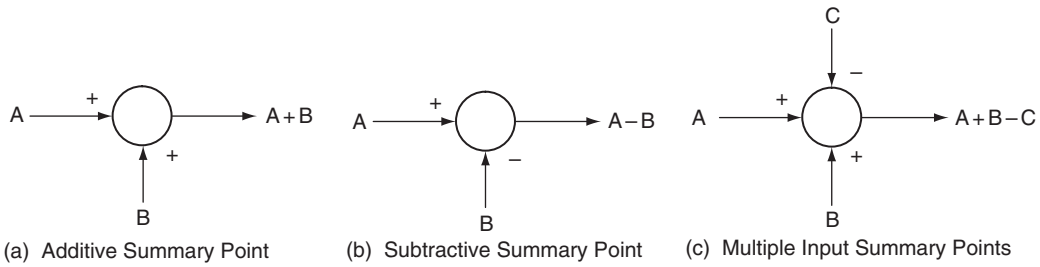


Figure 6.2: Summary points.

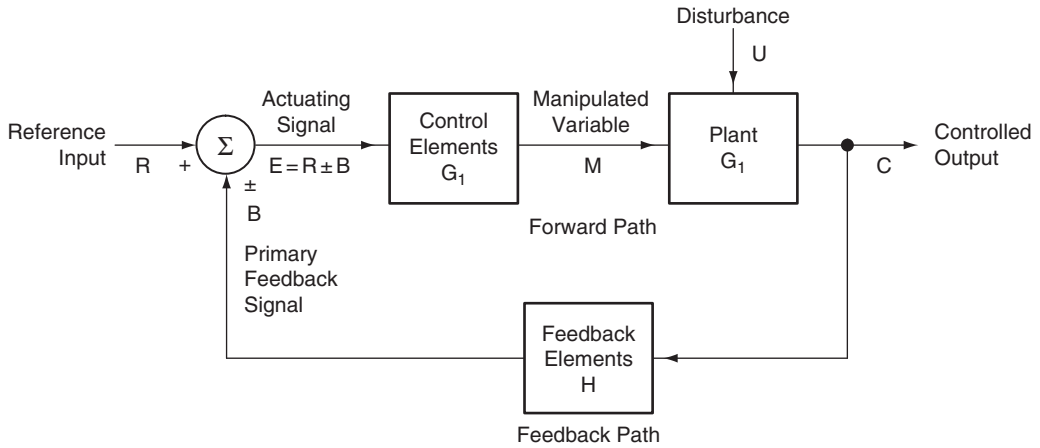


Figure 6.3: Definition of control system terms.

defines the terms in a typical electronic feedback system. Multiloop feedback systems (Figure 6.5) are intimidating, but they can be reduced to a single loop feedback system, as shown in the figure, by writing equations and solving for V_{OUT}/V_{IN}. An easier method for reducing multiloop feedback systems to single loop feedback systems is to follow the rules and use the transforms given in Figure 6.6.

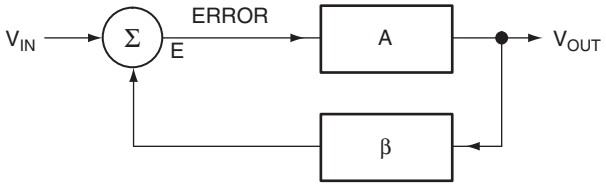


Figure 6.4: Definition of an electronic feedback circuit.

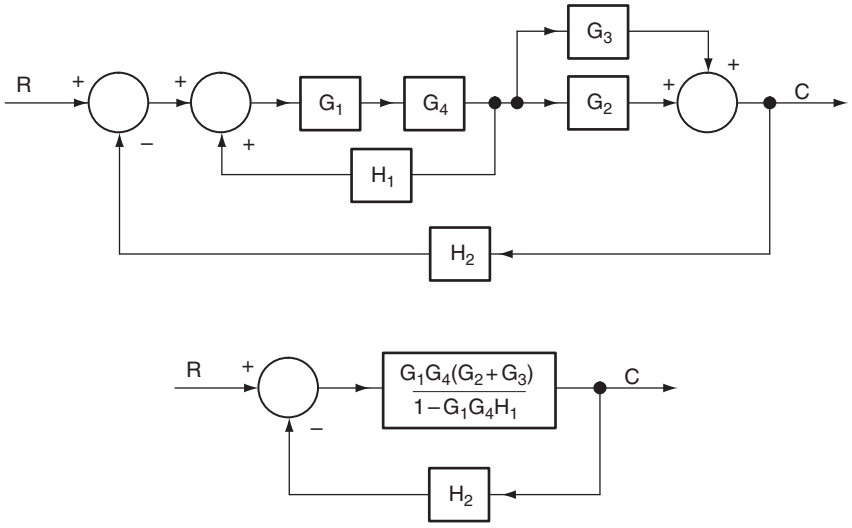


Figure 6.5: Multiloop feedback system.

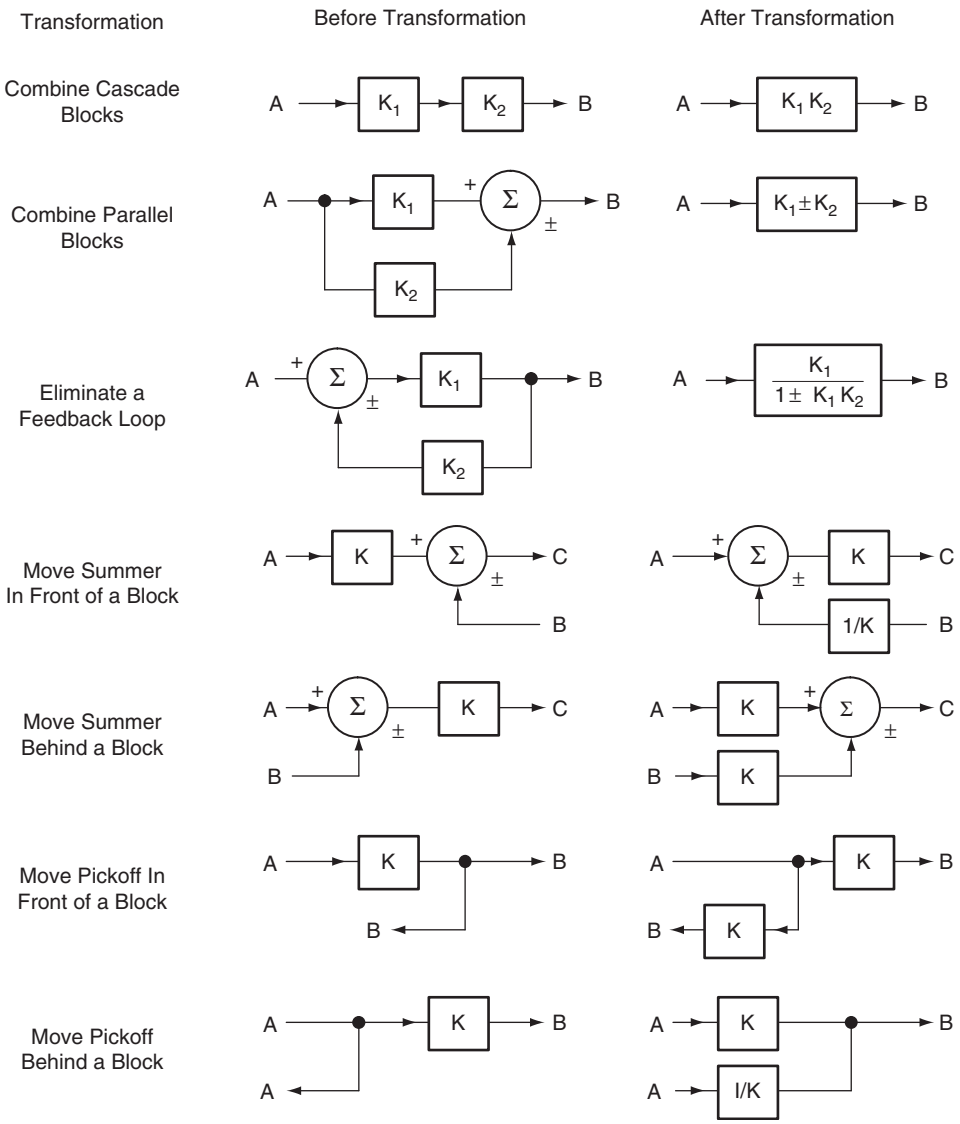


Figure 6.6: Block diagram transforms.

The block diagram reduction rules are these:

- Combine cascade blocks.
- Combine parallel blocks.
- Eliminate interior feedback loops.
- Shift summing points to the left.
- Shift takeoff points to the right.
- Repeat until canonical form is obtained.

Figure 6.6 gives the block diagram transforms. The idea is to reduce the diagram to its canonical form because the canonical feedback loop is the simplest form of a feedback loop, and its analysis is well documented. All feedback systems can be reduced to the canonical form, so all feedback systems can be analyzed with the same math. A canonical loop exists for each input to a feedback system; although the stability dynamics are independent of the input, the output results are input dependent. The response of each input of a multiple input feedback system can be analyzed separately and added through superposition.

6.3 Feedback Equation and Stability

Figure 6.7 shows the canonical form of a feedback loop with control system and electronic system terms. The terms make no difference except that they have meaning to the system engineers, but the math does have meaning, and it is identical for both types of terms. The electronic terms and negative feedback sign are used in this analysis, because subsequent chapters deal with electronic applications. The output

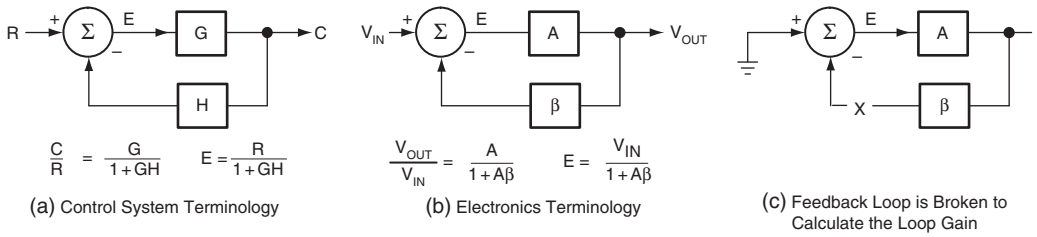


Figure 6.7: Comparison of control and electronic canonical feedback systems.

equation is written in Equation (6.1):

$$V_{OUT} = EA \tag{6.1}$$

The error equation is written in Equation (6.2):

$$E = V_{IN} - \beta V_{OUT} \tag{6.2}$$

Combining Equations (6.1) and (6.2) yields Equation (6.3):

$$\frac{V_{OUT}}{A} = V_{IN} - \beta V_{OUT} \tag{6.3}$$

Collecting terms yields Equation (6.4):

$$V_{OUT}\left(\frac{1}{A} + \beta\right) = V_{IN} \tag{6.4}$$

Rearranging terms yields the classic form of the feedback, Equation (6.5):

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{6.5}$$

When the quantity $A\beta$ in Equation (6.5) becomes very large with respect to 1, the 1 can be neglected and Equation (6.5) reduces to Equation (6.6), which is the ideal feedback equation. Under the conditions that $A\beta \gg 1$, the system gain is determined by the feedback factor, β. Stable passive circuit components are used to implement the feedback factor; thus in the ideal situation, the closed loop gain is predictable and stable because β is predictable and stable.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{\beta} \tag{6.6}$$

The quantity $A\beta$ is so important that it has been given a special name, *loop gain*. In Figure 6.7, when the voltage inputs are grounded (current inputs are opened) and the

loop is broken, the calculated gain is the loop gain, $A\beta$. Now, keep in mind that we are using complex numbers, which have magnitude and direction. When the loop gain approaches –1, or to express it mathematically, $1\angle -180°$, Equation (6.5) approaches $1/0 \Rightarrow \propto$. The circuit output heads for infinity as fast as it can using the equation of a straight line. If the output were not energy limited, the circuit would explode the world, but happily it is energy limited, so somewhere it comes up against the limit.

Active devices in electronic circuits exhibit nonlinear phenomena when their output approaches a power supply rail, and the nonlinearity reduces the gain to the point where the loop gain no longer equals $1\angle -180°$. Now, the circuit can do two things: First, it can become stable at the power supply limit; second, it can reverse direction (because stored charge keeps the output voltage changing) and head for the negative power supply rail.

The first state, where the circuit becomes stable at a power supply limit, is named *lockup*: The circuit will remain in a locked up state until power is removed and reapplied. The second state, where the circuit bounces between power supply limits, is named *oscillatory*. Remember, the loop gain, $A\beta$, is the sole factor determining stability of the circuit or system. Inputs are grounded or disconnected, so they have no bearing on stability.

Equations (6.1) and (6.2) are combined and rearranged to yield Equation (6.7), which is the system or circuit error equation:

$$E = \frac{V_{IN}}{1 + A\beta} \tag{6.7}$$

First, note that the error is proportional to the input signal. This is the expected result, because a bigger input signal results in a bigger output signal, and bigger output signals require more drive voltage. As the loop gain increases, the error decreases, thus large loop gains are attractive for minimizing errors.

6.4 Bode Analysis of Feedback Circuits

H. W. Bode developed a quick, accurate, and easy method of analyzing feedback amplifiers, and he wrote a book about his techniques, published in 1945 [2]. Operational amplifiers had not been developed when Bode's book was published, but they fall under the general classification of feedback amplifiers, so they are easily

analyzed with Bode techniques. The mathematical manipulations required to analyze a feedback circuit are complicated because they involve multiplication and division. Bode developed the Bode plot, which simplifies the analysis through the use of graphical techniques.

The Bode equations are log equations that take the form $20 \log[F(t)] = 20 \log[|F(t)|] +$ phase angle. Terms that are normally multiplied and divided can now be added and subtracted because they are log equations. The addition and subtraction is done graphically, easing the calculations and giving the designer a pictorial representation of circuit performance. Equation (6.8) is written for the low pass filter shown in Figure 6.8:

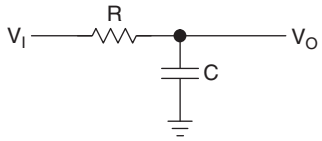


Figure 6.8: Low pass filter.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}} = \frac{1}{1 + RCs} = \frac{1}{1 + \tau s} \tag{6.8}$$

where $s = j\omega$, $j = \sqrt{(-1)}$, and $RC = \tau$.

The magnitude of this transfer function is $|V_{OUT}/V_{IN}| = 1/\sqrt{1^2 + (\tau\omega)^2}$. This magnitude, $|V_{OUT}/V_{IN}| \cong 1$ when $\tau = 0.1/\tau$; it equals 0.707 when $\tau = 1/\tau$; and it is approximately = 0.1 when $\tau = 10/\tau$. These points are plotted in Figure 6.9 using straight line approximations. The negative slope is –20 dB/decade or –6 dB/octave. The magnitude curve is plotted as a horizontal line until it intersects the break point, where $\tau = 1/\tau$. The negative slope begins at the break point, because the magnitude starts decreasing at that point. The gain is equal to 1 or 0 dB at very low frequencies, equal to 0.707 or –3 dB at the break frequency, and it keeps falling with a –20 dB/decade slope for higher frequencies.

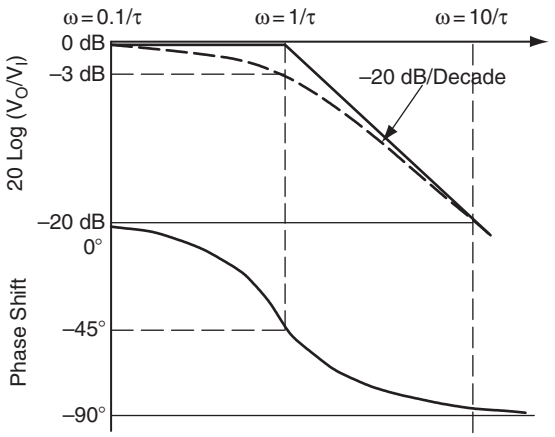


Figure 6.9: Bode plot of low pass filter transfer function.

The phase shift for the low pass filter or any other transfer function is calculated with the aid of Equation (6.9):

$$\phi = \text{tangent}^{-1}\left(\frac{\text{Real}}{\text{Imaginary}}\right) = -\text{tangent}^{-1}\left(\frac{\omega\tau}{1}\right) \tag{6.9}$$

The phase shift is much harder to approximate because the tangent function is nonlinear. Normally, the phase information is required only around the 0 dB intercept point for an active circuit, so the calculations are minimized. The phase is shown in Figure 6.9, and it is approximated by remembering that the tangent of 90° is 1, the tangent of 60° is $\sqrt{3}$, and the tangent of 30° is $\sqrt{3}/3$.

A break point occurring in the denominator is called a *pole*, and it slopes down. Conversely, a break point occurring in the numerator is called a *zero*, and it slopes up. When the transfer function has multiple poles and zeros, each pole or zero is plotted independently, and the individual poles and zeros are added graphically. If multiple poles, zeros, or a pole/zero combination have the same break point, they are plotted on top of each other. Multiple poles or zeros cause the slope to change by multiples of 20 dB/decade.

An example of a transfer function with multiple poles and zeros is a band reject filter (see Figure 6.10). The transfer function of the band reject filter is given in Equation (6.10):

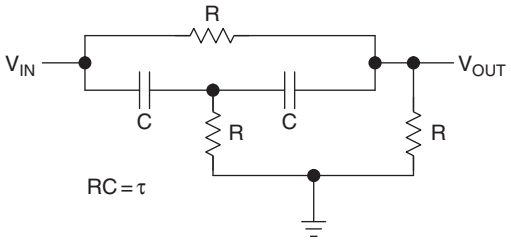


Figure 6.10: Band reject filter.

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{(1 + \tau s)(1 + \tau s)}{2\left(1 + \frac{\tau s}{0.44}\right)\left(1 + \frac{\tau s}{4.56}\right)} \tag{6.10}$$

The pole zero plot for each individual pole and zero is shown in Figure 6.11, and the combined pole zero plot is shown in Figure 6.12.

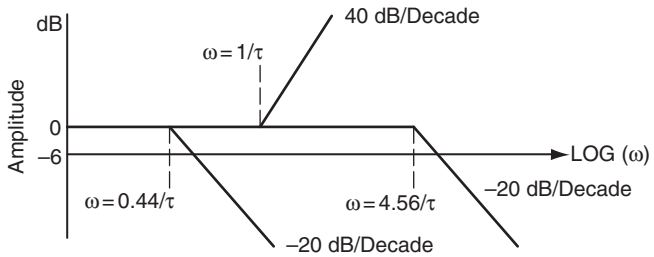


Figure 6.11: Individual pole zero plot of a band reject filter.

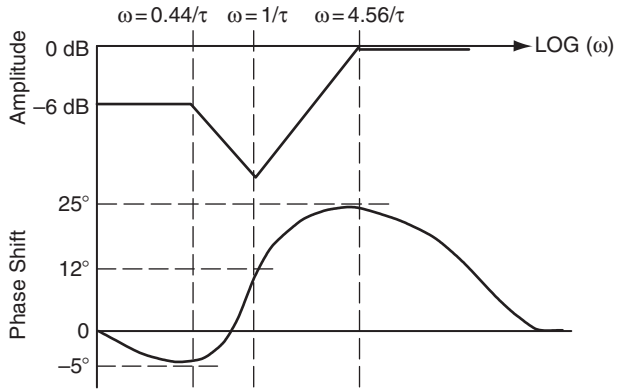


Figure 6.12: Combined pole zero plot of a band reject filter.

The individual pole zero plots show the DC gain of 1/2 plotting as a straight line from the –6 dB intercept. The two zeros occur at the same break frequency, thus they add to a 40 dB/decade slope. The two poles are plotted at their break points of $\tau = 0.44/\tau$ and $\tau = 4.56/\tau$. The combined amplitude plot intercepts the amplitude axis at –6 dB because of the DC gain, then breaks down at the first pole. When the amplitude function gets to the double zero, the first zero cancels out the first pole and the second zero breaks up. The upward slope continues until the second pole cancels out the second zero, and the amplitude is flat from that point out in frequency.

When the separation between all the poles and zeros is great, a decade or more in frequency, it is easy to draw the Bode plot. As the poles and zeros get closer together, the plot gets harder to make. The phase is especially hard to plot because of the tangent function, but picking a few salient points and sketching them in first gets a pretty good approximation [3]. The Bode plot enables the designer to get a good idea of pole zero placement, and it is valuable for fast evaluation of possible compensation techniques. When the situation gets critical, accurate calculations must be made and plotted to get an accurate result.

Consider Equation (6.11):

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{6.11}$$

Taking the log of Equation (6.11) yields Equation (6.12):

$$20\log\left(\frac{V_{OUT}}{V_{IN}}\right) = 20\log(A) - 20\log(1 + A\beta) \tag{6.12}$$

If A and β contain no poles or zeros, there are no break points. Then, the Bode plot of Equation (6.12) looks like that shown in Figure 6.13; and because there are no poles to contribute negative phase shift, the circuit cannot oscillate.

All real amplifiers have many poles, but they are normally internally compensated so that they appear to have a single pole. Such an amplifier would have an equation similar to that given in Equation (6.13):

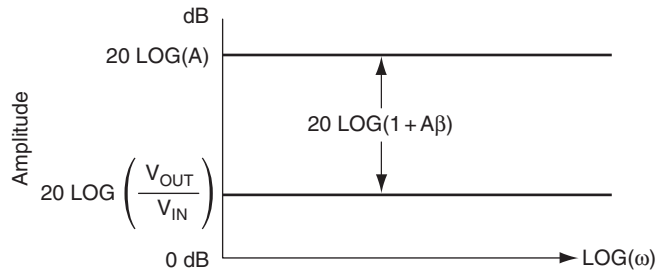


Figure 6.13: When no pole exists in Equation (6.12).

$$A = \frac{a}{1 + j\dfrac{\omega}{\omega_a}} \tag{6.13}$$

The plot for the single pole amplifier is shown in Figure 6.14.

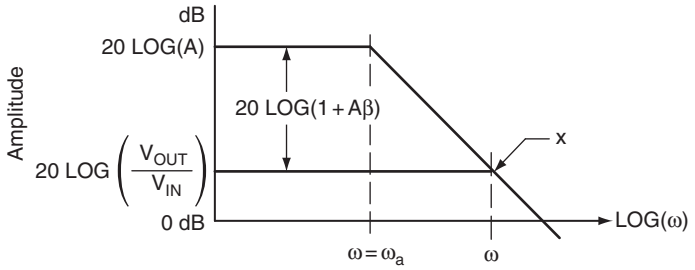


Figure 6.14: When Equation (6.12) has a single pole.

The amplifier gain, A, intercepts the amplitude axis at 20 log(A), and it breaks down at a slope of –20 dB/decade at $\omega = \omega_a$. The negative slope continues for all frequencies greater than the break point, $\omega = \omega_a$. The closed loop circuit gain intercepts the amplitude axis at 20 log(V_{OUT}/V_{IN}), and because ω has no poles or zeros, it is constant until its projection intersects the amplifier gain at point X. After intersection with the amplifier gain curve, the closed loop gain follows the amplifier gain, because the amplifier is the controlling factor.

Actually, the closed loop gain starts to roll off earlier, and it is down 3 dB at point *X*. At point *X*, the difference between the closed loop gain and the amplifier gain is –3 dB, so according to Equation (6.12), the term $-20 \log(1 + A\beta) = -3$ dB. The magnitude of 3 dB is $\sqrt{2}$, hence $\sqrt{1 + (A\beta)^2} = \sqrt{-2}$, and elimination of the radicals shows that $A\beta = 1$. There is a method [4] of relating phase shift and stability to the slope of the closed loop gain curves, but only the Bode method is covered here. An excellent discussion of poles, zeros, and their interaction is given by M. E. Van Valkenberg [5], who also includes some excellent prose to liven the discussion.

6.5 Loop Gain Plots Are the Key to Understanding Stability

Stability is determined by the loop gain; and when $A\beta = -1 = |1|\angle -180°$, instability or oscillation occurs. If the magnitude of the gain exceeds 1, it is usually reduced to 1 by circuit nonlinearities, so oscillation generally results for situations where the gain magnitude exceeds 1.

Consider oscillator design, which depends on nonlinearities to decrease the gain magnitude; if the engineer designed for a gain magnitude of 1 at nominal circuit conditions, the gain magnitude would fall below 1 under worst case circuit conditions, causing oscillation to cease. Therefore, the prudent engineer designs for a gain magnitude of 1 under worst case conditions, knowing that the gain magnitude is much more than 1 under optimistic conditions. The prudent engineer depends on circuit nonlinearities to reduce the gain magnitude to the appropriate value, but this same engineer pays the price of poorer distortion performance. Sometimes, a design compromise is reached by putting a nonlinear component, such as a lamp, in the feedback loop to control the gain without introducing distortion.

Some high gain control systems always have a gain magnitude greater than 1, but they avoid oscillation by manipulating the phase shift. The amplifier designer who pushes the amplifier for superior frequency performance has to be careful not to let the loop gain phase shift accumulate to 180°. Problems with overshoot and ringing pop up before the loop gain reaches the 180° phase shift, so the amplifier designer must keep a close eye on loop dynamics. Ringing and overshoot are handled in the next section, so preventing oscillation is emphasized in this section.

Equation (6.14) has the form of many loop gain transfer functions or circuits, so it is analyzed in detail:

$$(A)\beta = \frac{(K)}{[1 + \tau_1(s)][1 + \tau_2(s)]} \tag{6.14}$$

The quantity K is the DC gain, and it plots as a straight line with an intercept of 20 log (K). The Bode plot of Equation (6.14) is shown in Figure 6.15. The two break points, $\tau = \tau_1 = 1/\tau_1$ and $\tau = \tau_2 = 1/\tau_2$, are plotted in the Bode plot. Each break point adds –20 dB/decade slope to the plot, and a 45° phase shift accumulates at each break point. This transfer function is referred to as a *two slope* because of the two break points. The slope of the curve when it crosses the 0 dB intercept indicates phase shift and the ability to oscillate. Note that a one slope can accumulate only a 90° phase shift; so when a transfer function passes through 0 dB with a one slope, it cannot oscillate. Furthermore, a two slope system can accumulate a 180° phase shift, therefore a transfer function with a two or greater slope is capable of oscillation.

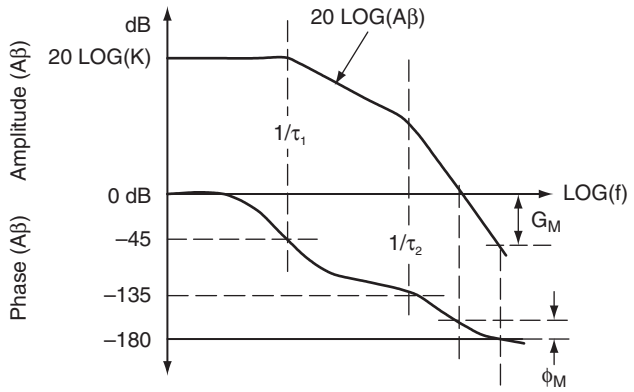


Figure 6.15: Magnitude and phase plot of Equation (6.14).

A one slope crossing the 0 dB intercept is stable, whereas a two or greater slope crossing the 0 dB intercept may be stable or unstable depending on the accumulated phase shift. Figure 6.15 defines two stability terms; the phase margin, ϕ_M, and the gain margin, G_M. Of these two terms, the phase margin is much more important because phase shift is critical for stability. The phase margin is a measure of the difference in the

actual phase shift and the theoretical 180° required for oscillation, and the phase margin measurement or calculation is made at the 0 dB crossover point. The gain margin is measured or calculated at the 180° phase crossover point. The phase margin is expressed mathematically in Equation (6.15):

$$\phi M = 180 - \text{tangent}^{-1}(A\beta) \tag{6.15}$$

The phase margin in Figure 6.15 is very small, 20°, so it is hard to measure or predict from the Bode plot. A designer probably doesn't want a 20° phase margin, because the system overshoots and rings badly, but this case points out the need to calculate small phase margins carefully. The circuit is stable, and it does not oscillate, because the phase margin is positive. Also, the circuit with the smallest phase margin has the highest frequency response and bandwidth.

Increasing the loop gain to ($K + C$), as shown in Figure 6.16, shifts the magnitude plot up. If the pole locations are kept constant, the phase margin reduces to zero as shown, and the circuit will oscillate. The circuit is not good for much in this condition because production tolerances and worst case conditions ensure that the circuit will oscillate when you want it to amplify, and vice versa.

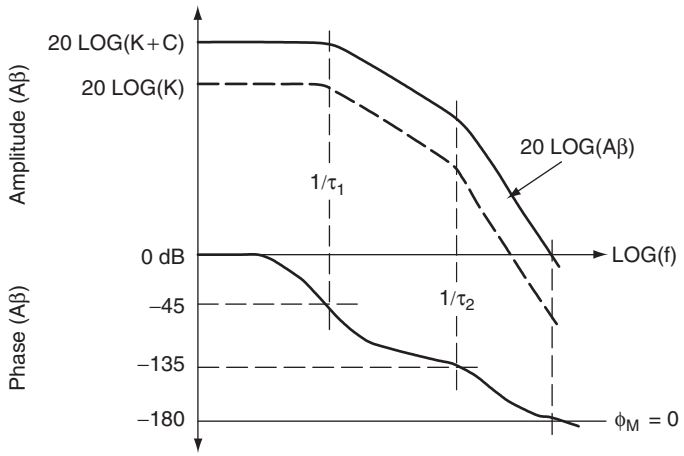


Figure 6.16: Magnitude and phase plot of the loop gain increased to ($K + C$).

The circuit poles are spaced closer in Figure 6.17, and this results in a faster accumulation of phase shift. The phase margin is zero because the loop gain phase shift reaches 180° before the magnitude passes through 0 dB. This circuit oscillates, but it is not a very stable oscillator, because the transition to 180° phase shift is very slow. Stable oscillators have a very sharp transition through 180°.

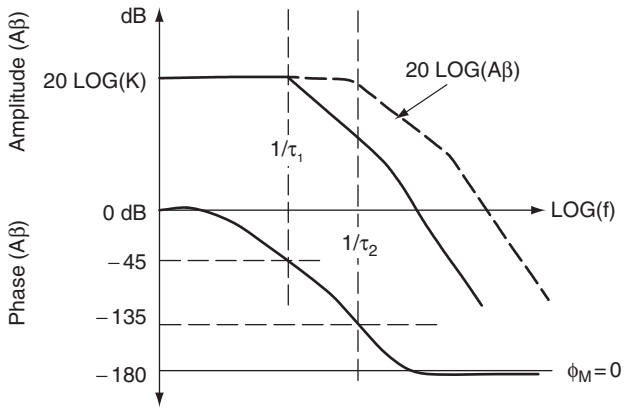


Figure 6.17: Magnitude and phase plot of the loop gain with the pole spacing reduced.

When the closed loop gain is increased, the feedback factor, β, is decreased because $V_{OUT}/V_{IN} = 1/\beta$ for the ideal case. This in turn decreases the loop gain, $A\beta$, so the stability increases. In other words, increasing the closed loop gain makes the circuit more stable. Stability is not important except to oscillator designers, because overshoot and ringing become intolerable to linear amplifiers long before oscillation occurs. The overshoot and ringing situation is investigated next.

6.6 The Second Order Equation and Ringing/ Overshoot Predictions

The second order equation is a common approximation used for feedback system analysis because it describes a two pole circuit, which is the most common approximation used. All real circuits are more complex than two poles, but except

for a small fraction, they can be represented by a two pole equivalent. The second order equation is extensively described in electronic and control literature [6].

$$(1 + A\beta) = 1 + \frac{K}{(1 + \tau_1 s)(1 + \tau_2 s)} \tag{6.16}$$

After algebraic manipulation, Equation (6.16) is presented in the form of Equation (6.17):

$$s^2 + S\frac{\tau_1 + \tau_2}{\tau_1 \tau_2} + \frac{1 + K}{\tau_1 \tau_2} = 0 \tag{6.17}$$

Equation (6.17) is compared to the second order control Equation (6.18), and the damping ratio, ζ, and natural frequency, w_N are obtained through like term comparisons:

$$s^2 + 2\zeta\omega_N s + \omega_N^2 \tag{6.18}$$

Comparing these equations yields formulas for the phase margin and percent overshoot as a function of damping ratio:

$$\omega_N = \sqrt{\frac{1 + K}{\tau_1 \tau_2}} \tag{6.19}$$

$$\xi = \frac{\tau_1 + \tau_2}{2\omega_N \tau_1 \tau_2} \tag{6.20}$$

When the two poles are well separated, Equation (6.21) is valid:

$$\phi_M - M = \text{tangent}^{-1}(2\xi) \tag{6.21}$$

The salient equations are plotted in Figure 6.18, which enables a designer to determine the phase margin and overshoot when the gain and pole locations are known.

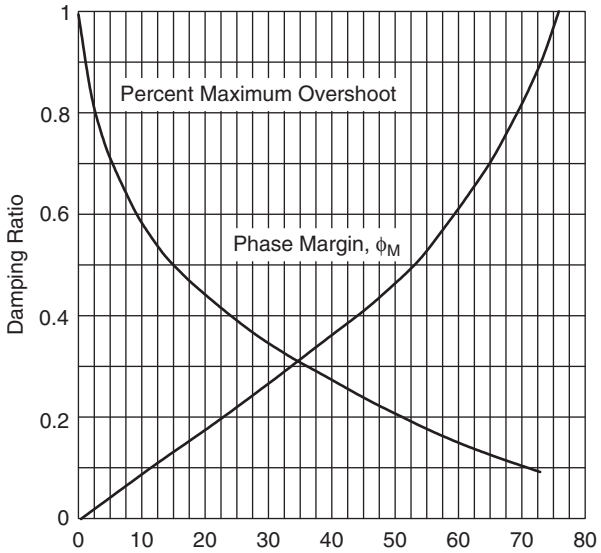


Figure 6.18: Phase margin and overshoot versus damping ratio.

Enter Figure 6.18 at the calculated damping ratio, say 0.4, and read the overshoot at 25% and the phase margin at 42°. If a designer had a circuit specification of 5% maximum overshoot, then the damping ratio must be 0.78 with a phase margin of 62°.

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CHAPTER 7

Development of the Nonideal Op Amp Equations

Ron Mancini

7.1 Introduction

Error sources in op amps are of two types, and they fall under the general classification of DC and AC errors. Examples of DC errors are input offset voltage and input bias current. The DC errors stay constant over the usable op amp frequency range; therefore the input bias current is 10 pA at 1 kHz and 10 pA at 10 kHz. Because of their constant and controlled behavior, DC errors are not considered until later chapters.

AC errors are flighty, so we address them here by developing a set of nonideal equations that account for AC errors. The AC errors may show up under DC conditions, but they get worse as the operating frequency increases. A good example of an AC error is common mode rejection ratio (CMRR). Most op amps have a guaranteed CMRR specification, but this specification is valid only at DC or very low frequencies. Further inspection of the data sheet reveals that CMRR decreases as operating frequency increases. Several other specifications that fall into the category of AC specifications are output impedance, power supply rejection ratio, peak to peak output voltage, differential gain, differential phase, and phase margin.

Differential gain is the most important AC specification, because the other AC specifications are derived from the differential gain. Until now, differential gain has been called *op amp gain* or *op amp open loop gain*, and we continue with that terminology. Let the data sheet call it *differential gain.*

As shown in prior chapters, when frequency increases, the op amp gain decreases and errors increase. This chapter develops the equations that illustrate the effects of the gain changes. We start with a review of the basic canonical feedback system stability because the op amp equations are developed using the same techniques.

Amplifiers are built with active components, such as transistors. Pertinent transistor parameters, like transistor gain, are subject to drift and initial inaccuracies from many sources, so amplifiers being built from these components are subject to drift and inaccuracies. The drift and inaccuracy are minimized or eliminated by using negative feedback. The op amp circuit configuration employs feedback to make the transfer equation of the circuit independent of the amplifier parameters (well almost), and while doing this, the circuit transfer function is made dependent on external passive components. External passive components can be purchased to meet almost any drift or accuracy specification; only the cost and size of the passive components limit their use.

Once feedback is applied to the op amp it is possible for the op amp circuit to become unstable. Certain amplifiers belong to a family called *internally compensated op amps*; they contain internal capacitors that are sometimes advertised as precluding instability. Although internally compensated op amps should not oscillate when operated under specified conditions, many have relative stability problems that manifest themselves as poor phase response, ringing, and overshoot. The only absolutely stable internally compensated op amp is the one lying on the workbench with no power applied! All other internally compensated op amps oscillate under some external circuit conditions.

Noninternally compensated or *externally* compensated op amps are unstable without the addition of external stabilizing components. This situation is a disadvantage in many cases because they require additional components, but the lack of internal compensation enables the top drawer circuit designer to squeeze the last drop of performance from the op amp. The designer has two options: op amps internally compensated by the IC manufacturer or op amps externally compensated by the designer. Compensation, except that done by the op amp manufacturer, must be done external to the IC. Surprisingly enough, internally compensated op amps require external compensation for demanding applications.

Compensation is achieved by adding external components that modify the circuit transfer function so that it becomes unconditionally stable. There are several different methods of compensating an op amp, and as you might suspect, pros and cons are associated with each method of compensation. After the op amp circuit is compensated, it must be analyzed to determine the effects of compensation. The modifications that

compensation has on the closed loop transfer function often determine which compensation scheme is most profitably employed.

7.2 Review of the Canonical Equations

A block diagram for a generalized feedback system is repeated in Figure 7.1. This simple block diagram is sufficient to determine the stability of any system.

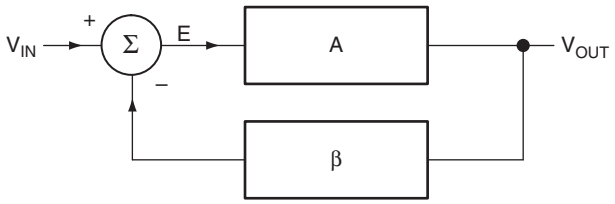


Figure 7.1: Feedback system block diagram.

The output and error equation development also is repeated here:

$$V_{\text{OUT}} = EA \tag{7.1}$$

$$E = V_{\text{IN}} = \beta V_{\text{OUT}} \tag{7.2}$$

Combining Equations (7.1) and (7.2) yields Equation (7.3):

$$\frac{V_{\text{OUT}}}{A} = V_{\text{IN}} - \beta V_{\text{OUT}} \tag{7.3}$$

Collecting terms yields Equation (7.4):

$$V_{\text{OUT}}\left(\frac{1}{A} + \beta\right) = V_{\text{IN}} \tag{7.4}$$

Rearranging terms yields the classic form of the feedback equation:

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{A}{1 + A\beta} \tag{7.5}$$

Note that Equation (7.5) reduces to Equation (7.6) when the quantity $A\beta$ in Equation (7.5) becomes very large with respect to 1. Equation (7.6) is called the *ideal feedback equation*, because it depends on the assumption that $A\beta \gg 1$; and it finds extensive use when amplifiers are assumed to have ideal qualities. Under the conditions that $A\beta \gg 1$, the system gain is determined by the feedback factor, β. Stable passive circuit components are used to implement the feedback factor, thus the ideal closed loop gain is predictable and stable because β is predictable and stable.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{\beta} \tag{7.6}$$

The quantity $A\beta$ is so important that it has been given a special name, *loop gain*. Consider Figure 7.2; when the voltage inputs are grounded (current inputs are opened) and the loop is broken, the calculated gain is the loop gain, $A\beta$. Now, keep in mind that this is a mathematics of complex numbers, which have magnitude and direction. When the loop gain approaches –1, or to express it mathematically, $1\angle -180°$, Equation (7.5) approaches infinity because $1/0 \Rightarrow \infty$. The circuit output heads for infinity as fast as it can using the equation of a straight line. If the output were not energy limited, the circuit would explode the world, but it is energy limited by the power supplies, so the world stays intact.

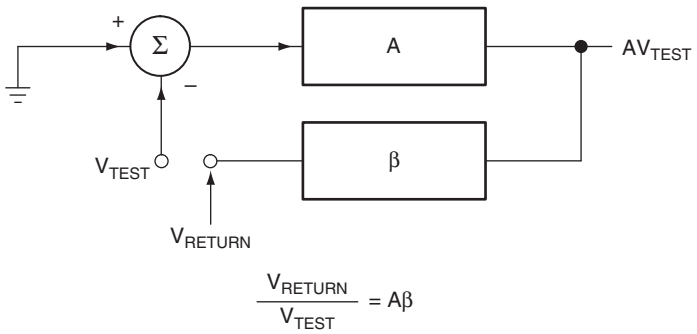


Figure 7.2: Feedback loop broken to calculate the loop gain.

Active devices in electronic circuits exhibit nonlinear behavior when their output approaches a power supply rail, and the nonlinearity reduces the amplifier gain until the loop gain no longer equals $1\angle -180°$. Now the circuit can do two things: First, it could

become stable at the power supply limit; second, it can reverse direction (because stored charge keeps the output voltage changing) and head for the negative power supply rail.

The first state, where the circuit becomes stable at a power supply limit, is named *lockup*; the circuit remains in the locked up state until power is removed. The second state, where the circuit bounces between power supply limits, is named *oscillatory*. Remember, the loop gain, $A\beta$, is the sole factor that determines stability for a circuit or system. Inputs are grounded or disconnected when the loop gain is calculated, so they have no effect on stability. The loop gain criteria is analyzed in depth later.

Equations (7.1) and (7.2) are combined and rearranged to yield Equation (7.7), which gives an indication of system or circuit error:

$$E = \frac{V_{\text{IN}}}{1 + A\beta} \tag{7.7}$$

First, note that the error is proportional to the input signal. This is the expected result because a bigger input signal results in a bigger output signal, and bigger output signals require more drive voltage. Second, the loop gain is inversely proportional to the error. As the loop gain increases, the error decreases; thus large loop gains are attractive for minimizing errors. Large loop gains also decrease stability, so there is always a trade-off between error and stability.

7.3 Noninverting Op Amps

A noninverting op amp is shown in Figure 7.3. The dummy variable V_B is inserted to make the calculations easier, and a is the op amp gain.

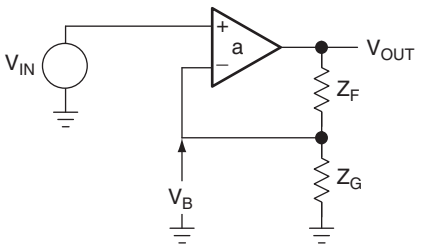


Figure 7.3: Noninverting op amp.

Equation (7.8) is the amplifier transfer equation:

$$V_{\text{OUT}} = a(V_{\text{IN}} \pm V_B) \tag{7.8}$$

The output equation is developed with the aid of the voltage divider rule. Using the voltage divider rule assumes that the op amp impedance is low.

$$V_B = \frac{V_{\text{OUT}} Z_G}{Z_F + Z_G} \text{ for } I_B = 0 \tag{7.9}$$

Combining Equations (7.8) and (7.9) yields Equation (7.10):

$$V_{\text{OUT}} = aV_{\text{IN}} - \frac{aZ_G V_{\text{OUT}}}{Z_G + Z_F} \tag{7.10}$$

Rearranging terms in Equation (7.10) yields Equation (7.11), which describes the transfer function of the circuit:

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{a}{1 + \dfrac{aZ_G}{Z_G + Z_F}} \tag{7.11}$$

Equation (7.5) is repeated as Equation (7.12) to make a term by term comparison of the equations easy:

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{A}{1 + A\beta} \tag{7.12}$$

By virtue of the comparison, we get Equation (7.13), which is the loop gain equation for the noninverting op amp. The loop gain equation determines the stability of the circuit. The comparison also shows that the open loop gain, A, is equal to the op amp open loop gain, a, for the noninverting circuit:

$$A\beta = \frac{aZ_G}{Z_G + Z_F} \tag{7.13}$$

Equation (7.13) is also derived with the aid of Figure 7.4, which shows the open loop noninverting op amp.

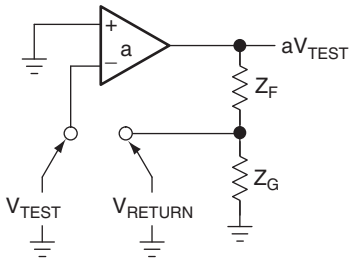


Figure 7.4: Open loop noninverting op amp.

The test voltage, V_{TEST}, is multiplied by the op amp open loop gain to obtain the op amp output voltage, aV_{TEST}. The voltage divider rule is used to calculate Equation (7.15), which is identical to Equation (7.14) after some algebraic manipulation:

$$V_{\text{RETURN}} = \frac{aV_{\text{TEST}}Z_G}{Z_F + Z_G} \tag{7.14}$$

$$\frac{V_{\text{RETURN}}}{V_{\text{TEST}}} = A\beta = \frac{aZ_G}{Z_F + Z_G} \tag{7.15}$$

7.4 Inverting Op Amps

The inverting op amp circuit is shown in Figure 7.5. The dummy variable V_A is inserted to make the calculations easier, and a is the op amp open loop gain.

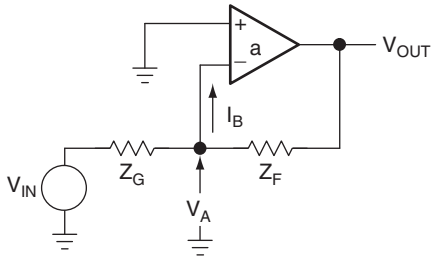


Figure 7.5: Inverting op amp.

The transfer equation is given in Equation (7.16):

$$V_{\text{OUT}} = -aV_A \tag{7.16}$$

The node voltage, Equation (7.17), is obtained with the aid of superposition and the voltage divider rule. Equation (7.18) is obtained by combining Equations (7.16) and (7.17).

$$V_A = \frac{V_{\text{IN}}Z_F}{Z_G + Z_F} + \frac{V_{\text{OUT}}Z_G}{Z_G + Z_F} \text{ for } I_B = 0 \tag{7.17}$$

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{\dfrac{-aZ_F}{Z_G + Z_F}}{1 + \dfrac{aZ_G}{Z_G + Z_F}} \tag{7.18}$$

Equation (7.16) is the transfer function of the inverting op amp. By virtue of the comparison between Equations (7.18) and (7.14), we get Equation (7.15) again, which is also the loop gain equation for the inverting op amp circuit. The comparison also shows that the open loop gain (A) is different from the op amp open loop gain (a) for the noninverting circuit.

The inverting op amp with the feedback loop broken is shown in Figure 7.6, and this circuit is used to calculate the loop gain given in Equation (7.19):

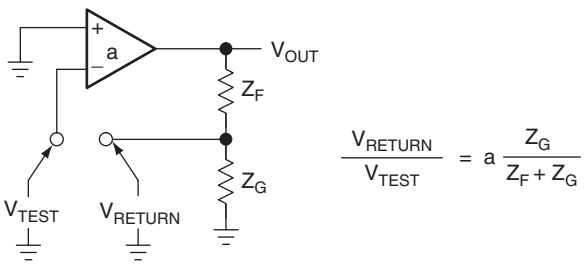


Figure 7.6: Inverting op amp: Feedback loop broken for loop gain calculation.

$$\frac{V_{\text{RETURN}}}{V_{\text{TEST}}} = \frac{aZ_G}{Z_G + Z_F} = A\beta \tag{7.19}$$

Several things must be mentioned at this point in the analysis. First, the transfer functions for the noninverting and inverting equations, (7.13) and (7.18), are different.

For a common set of Z_G and Z_F values, the magnitude and polarity of the gains are different. Second, the loop gain of both circuits, as given by Equations (7.15) and (7.19), is identical. Therefore the stability performance of both circuits is identical although their transfer equations are different. This makes the important point that *stability is not dependent on the circuit inputs*. Third, the A gain block shown in Figure 7.1 is different for each op amp circuit. By comparison of Equations (7.5), (7.11), and (7.18), we see that $A_{\text{NONINV}} = a$ and $A_{\text{INV}} = aZ_F/(Z_G + Z_F)$.

7.5 Differential Op Amps

The differential amplifier circuit is shown in Figure 7.7. The dummy variable V_E is inserted to make the calculations easier, and a is the open loop gain.

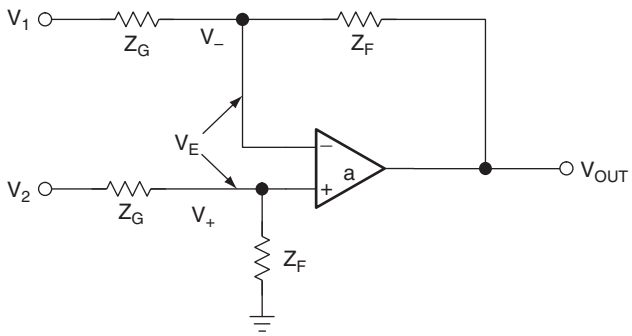


Figure 7.7: Differential amplifier circuit.

Equation (7.20) is the circuit transfer equation:

$$V_{\text{OUT}} = aV_E = V_+ \pm V_- \tag{7.20}$$

The positive input voltage, V_+, is written in Equation (7.21) with the aid of superposition and the voltage divider rule:

$$V_+ = V_2 \frac{Z_F}{Z_F + Z_G} \tag{7.21}$$

The negative input voltage, V_-, is written in Equation (7.22) with the aid of superposition and the voltage divider rule:

$$V_- = V_1 \frac{Z_F}{Z_F + Z_G} - V_{OUT} \frac{Z_G}{Z_F + Z_G} \tag{7.22}$$

Combining Equations (7.20), (7.21), and (7.22) yields Equation (7.23):

$$V_{OUT} = a\left[\frac{V_2 Z_F}{Z_F + Z_G} - \frac{V_1 Z_F}{Z_F + Z_G} - \frac{V_{OUT} Z_G}{Z_F + Z_G}\right] \tag{7.23}$$

After algebraic manipulation, Equation (7.23) reduces to Equation (7.24):

$$\frac{V_{OUT}}{V_2 - V_1} = \frac{\dfrac{aZ_F}{Z_F + Z_G}}{1 + \dfrac{aZ_G}{Z_F + Z_G}} \tag{7.24}$$

The comparison method reveals that the loop gain, as shown in Equation (7.25), is identical to that shown in Equations (7.13) and (7.19):

$$A\beta = \frac{aZ_G}{Z_G + Z_F} \tag{7.25}$$

Again, the loop gain, which determines stability, is a function of only the closed loop and independent of the inputs.

CHAPTER 8

Voltage Feedback Op Amp Compensation

Ron Mancini

8.1 Introduction

Voltage feedback amplifiers (VFA) have been with us for about 60 years, and they have been problems for circuit designers since the first day. You see, the feedback that makes them versatile and accurate also has a tendency to make them unstable. The operational amplifier (op amp) circuit configuration uses a high gain amplifier whose parameters are determined by external feedback components. The amplifier gain is so high that, without these external feedback components, the slightest input signal would saturate the amplifier output. The op amp is in common usage, so this configuration is examined in detail, but the results are applicable to many other voltage feedback circuits. Current feedback amplifiers (CFA) are similar to VFAs, but the differences are important enough to warrant handling CFAs separately.

Stability, as used in electronic circuit terminology, is often defined as achieving a nonoscillatory state. This is a poor, inaccurate definition of the word. *Stability* is a relative term, and this situation makes people uneasy, because relative judgments are exhaustive. It is easy to draw the line between a circuit that oscillates and one that does not oscillate, so we can understand why some people believe that oscillation is a natural boundary between stability and instability.

Feedback circuits exhibit poor phase response, overshooting, and ringing long before oscillation occurs; and these effects are considered undesirable by circuit designers. This chapter is not concerned with oscillators; therefore *relative stability* is defined in terms of

performance. By definition, when designers decide what trade-offs are acceptable, they determine what the relative stability of the circuit is. A relative stability measurement is the damping ratio (ζ). The damping ratio is related to the phase margin, hence the phase margin is another measure of relative stability. The most stable circuits have the longest response times, lowest bandwidth, highest accuracy, and least overshoot. The least stable circuits have the fastest response times, highest bandwidth, lowest accuracy, and some overshoot.

Op amps left in their native state oscillate without some form of compensation. The first IC op amps were very hard to stabilize, but there were a lot of good analog designers around in the 1960s, so we used them. Internally compensated op amps were introduced in the late 1960s in an attempt to make op amps easy for everyone to use. Unfortunately, internally compensated op amps sacrifice a lot of bandwidth and still oscillate under some conditions, so an understanding of compensation is required to apply op amps.

Internal compensation provides a worst case trade-off between stability and performance. Uncompensated op amps require more attention, but they can do more work. Both are covered here.

Compensation is a process of applying a judicious patch in the form of an *RC* network to make up for a less than perfect op amp or circuit. Many problems can introduce instability, hence there are many compensation schemes.

8.2 Internal Compensation

Op amps are internally compensated to save external components and enable their use by less knowledgeable people. It takes some measure of analog knowledge to compensate an analog circuit. Internally compensated op amps normally are stable when they are used in accordance with the application's instructions. Internally compensated op amps are not unconditionally stable. They are multiple pole systems, but they are internally compensated such that they appear as a single pole system over much of the frequency range. Internal compensation severely decreases the possible closed loop bandwidth of the op amp.

Internal compensation is accomplished in several ways, but the most common method is to connect a capacitor across the collector base junction of a voltage gain transistor (see Figure 8.1). The Miller effect multiplies the capacitor value by an amount approximately equal to the stage gain, thus the Miller effect uses small value capacitors for compensation.

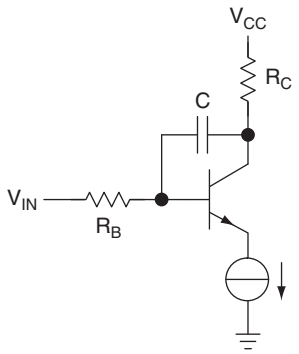


Figure 8.1: Miller effect compensation.

Figure 8.2 shows the gain/phase diagram for an older op amp (TL03X). When the gain crosses the 0 dB axis (gain = 1), the phase shift is approximately 108°, therefore the op amp must be modeled as a second order system because the phase shift is more than 90°.

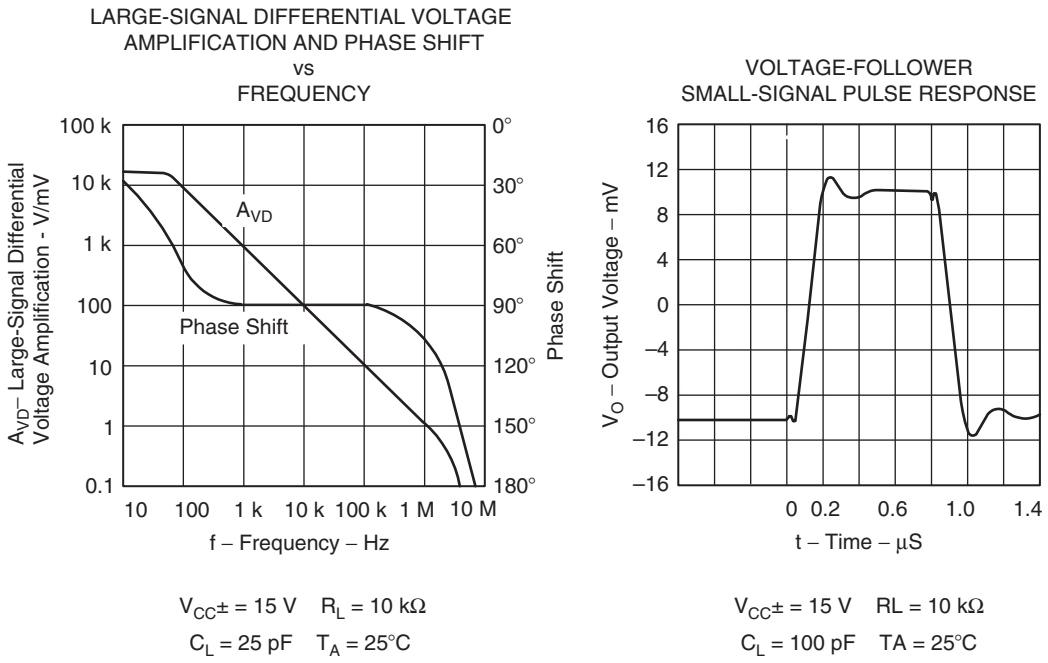


Figure 8.2: TL03X frequency and time response plots.

This yields a phase margin of $\varphi = 180° - 108° = 72°$, so the circuit should be very stable. Referring to Figure 8.3, the damping ratio is 1 and the expected overshoot is 0. Figure 8.2 shows approximately 10% overshoot, which is unexpected, but inspecting Figure 8.2 further reveals that the loading capacitance for the two plots is different. The pulse response is loaded with 100 pF rather than the 25 pF shown for the gain/phase plot, and this extra loading capacitance accounts for the loss of phase margin.

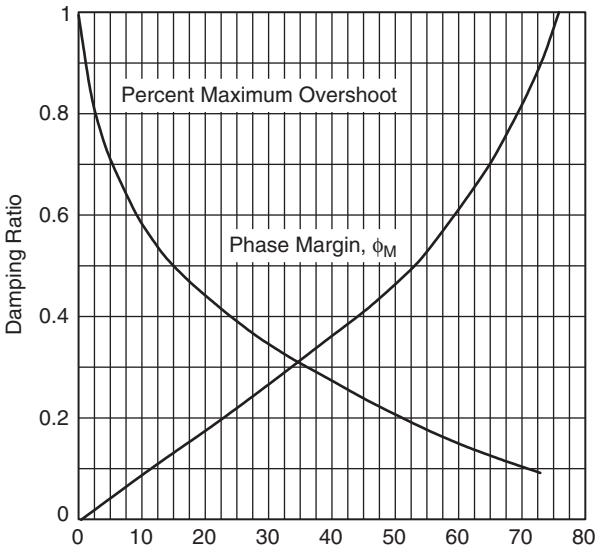


Figure 8.3: Phase margin and percent overshoot versus damping ratio.

Why does the loading capacitance make the op amp unstable? Look closely at the gain/phase response between 1 MHz and 9 MHz, and observe that the gain curve changes slope drastically while the rate of phase change approaches 120°/decade. The radical gain/phase slope change proves that several poles are located in this area. The loading capacitance works with the op amp output impedance to form another pole, and the new pole reacts with the internal op amp poles. As the loading capacitor value is increased, its pole migrates down in frequency, causing more phase shift at the 0 dB crossover frequency. The proof of this is given in the TL03X data sheet, where plots of ringing and oscillation versus loading capacitance are shown.

Figure 8.4 shows similar plots for the TL07X, which is the newer family of op amps. Note that the phase shift is approximately 100° when the gain crosses the 0 dB axis.

This yields a phase margin of 80°, which is close to unconditionally stable. The slope of the phase curve changes to 180°/decade about one decade from the 0 dB crossover point. The radical slope change causes suspicion about the 90° phase margin; furthermore the gain curve must be changing radically when the phase is changing radically. The gain/phase plot may not be totally false, but it sure is overly optimistic.

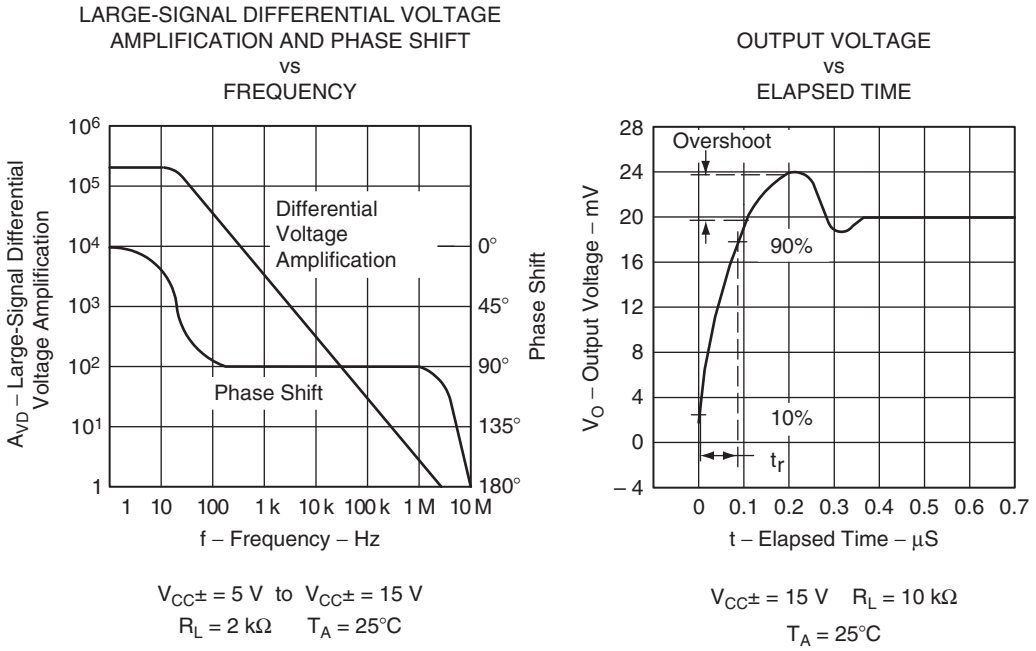


Figure 8.4: TL07X frequency and time response plots.

The TL07X pulse response plot shows approximately 20% overshoot. No loading capacitance is indicated on the plot to account for a seemingly unconditionally stable op amp exhibiting this large an overshoot. Something is wrong here: The analysis is wrong, the plots are wrong, or the parameters are wrong. Figure 8.5 shows the plots for the TL08X family of op amps, which are sisters to the TL07X family. The gain/phase curve and pulse response is virtually identical, but the pulse response lists a 100 pF loading capacitor. This little exercise illustrates three valuable points: First, if the data seem wrong, they probably are wrong; second, even the factory people make mistakes; and third, the loading capacitor makes op amps ring, overshoot, or oscillate.

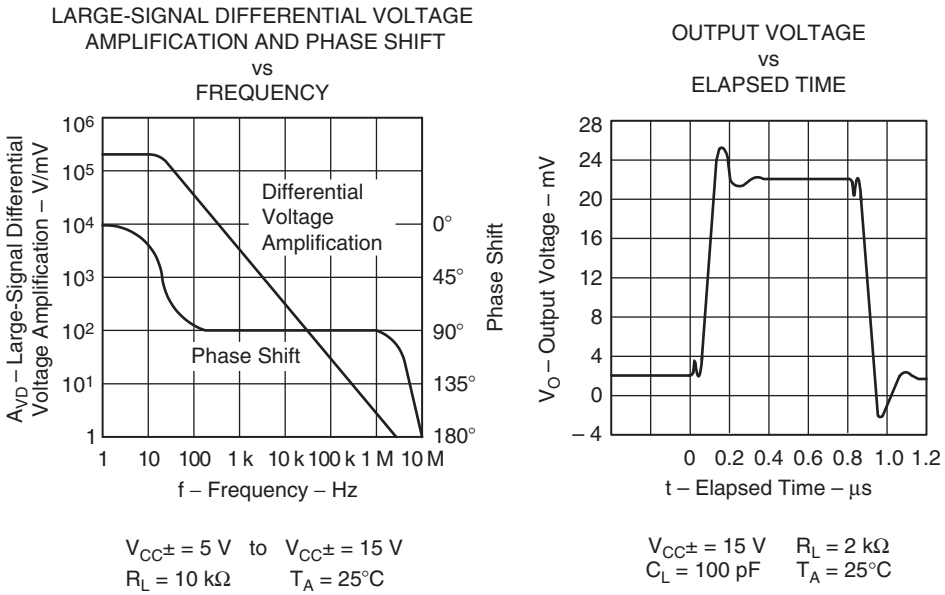


Figure 8.5: TL08X frequency and time response plots.

The frequency and time response plots for the TLV277X family of op amps is shown in Figures 8.6 and 8.7. First, note that the information is more sophisticated because the phase response is given in degrees of phase margin; second, both gain/phase plots are done with substantial loading capacitors (600 pF), so they have some practical value; and third, the phase margin is a function of power supply voltage.

At $V_{CC} = 5$ V, the phase margin at the 0 dB crossover point is 60°, while it is 30° at $V_{CC} = 2.7$ V. This translates into an expected overshoot of 18% at $V_{CC} = 5$ V and 28% at $V_{CC} = 2.7$ V. Unfortunately the time response plots are done with 100 pF loading capacitance, hence we cannot check our figures very well. The $V_{CC} = 2.7$ V overshoot is approximately 2%, and it is almost impossible to figure out what the overshoot would have been with a 600 pF loading capacitor. The small signal pulse response is done with millivolt signals, and that is a more realistic measurement than using the full signal swing.

Internally compensated op amps are very desirable because they are easy to use and do not require external compensation components. Their drawback is that the bandwidth is limited by the internal compensation scheme. The op amp open loop gain eventually

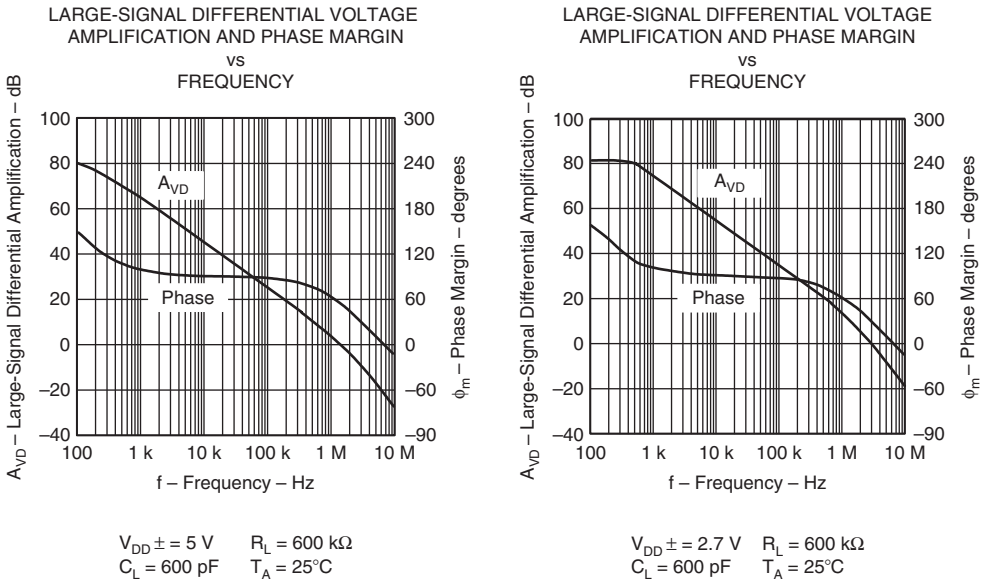


Figure 8.6: TLV277X frequency response plots.

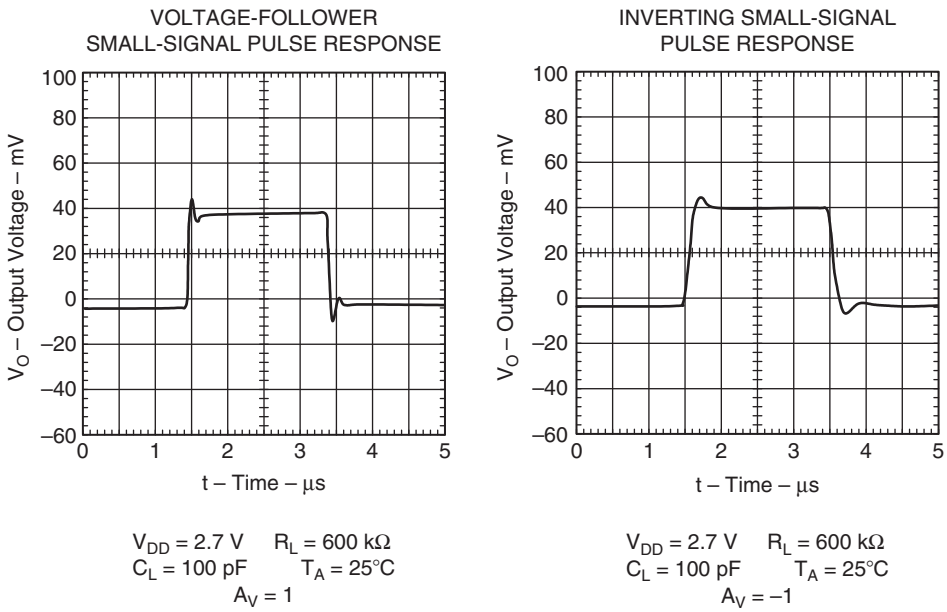


Figure 8.7: TLV277X time response plots.

(when it shows up in the loop gain) determines the error in an op amp circuit. In a noninverting buffer configuration, the TLV277X is limited to 1% error at 50 kHz ($V_{CC} = 2.7$ V) because the op amp gain is 40 dB at that point. Circuit designers can play tricks, such as bypassing the op amp with a capacitor to emphasize the high frequency gain, but the error is still 1%. Keep Equation (8.1) in mind, because it defines the error. If the TLV277X were not internally compensated, it could be externally compensated for a lower error at 50 kHz, because the gain would be much higher.

$$E = \frac{V_{IN}}{1 + A\beta} \tag{8.1}$$

8.3 External Compensation, Stability, and Performance

Nobody compensates an op amp just because it is there; designers have a reason to compensate the op amp, and that reason is usually stability. They want the op amp to perform a function in a circuit where it is potentially unstable. Internally and noninternally compensated op amps are compensated externally because certain circuit configurations do cause oscillations. Several potentially unstable circuit configurations are analyzed in this section, and the reader can extend the external compensation techniques as required.

Other reasons for externally compensating op amps are noise reduction, flat amplitude response, and obtaining the highest bandwidth possible from an op amp. An op amp generates noise, and noise is generated by the system. The noise contains many frequency components; and when a high pass filter is incorporated in the signal path, it reduces high frequency noise. Compensation can be employed to roll off the op amp's high frequency, closed loop response, thus causing the op amp to act as a noise filter. Internally compensated op amps are modeled with a second order equation, and this means that the output voltage can overshoot in response to a step input. When this overshooting (or peaking) is undesirable, external compensation can increase the phase margin to 90°, where there is no peaking. An uncompensated op amp has the highest bandwidth possible. External compensation is required to stabilize uncompensated op amps, but the compensation can be tailored to the specific circuit, thus yielding the highest possible bandwidth consistent with the pulse response requirements.

8.4 Dominant Pole Compensation

We saw that capacitive loading caused potential instabilities, therefore an op amp loaded with an output capacitor is a circuit configuration that must be analyzed. This circuit is called *dominant pole compensation*, because if the pole formed by the op amp output impedance and the loading capacitor is located close to the zero frequency axis, it becomes dominant. The op amp circuit is shown in Figure 8.8, and the open loop circuit used to calculate the loop gain ($A\beta$) is shown in Figure 8.9.

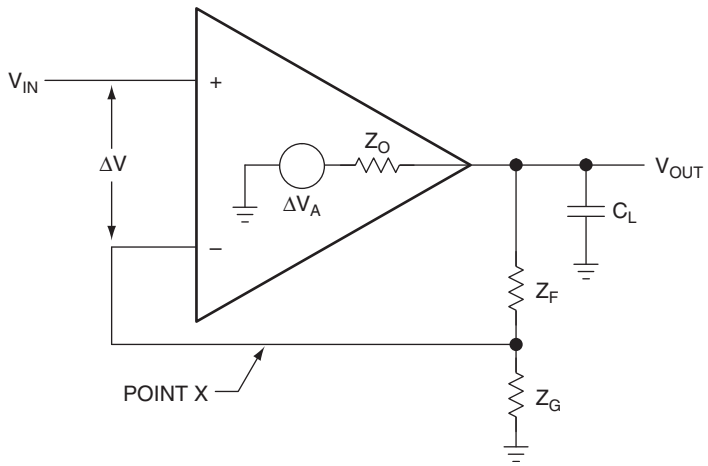


Figure 8.8: Capacitively loaded op amp.

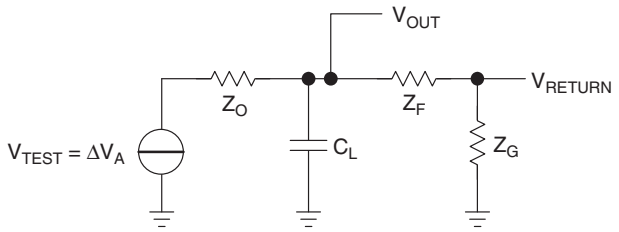


Figure 8.9: Capacitively loaded op amp with loop broken for loop gain ($A\beta$) calculation.

The analysis starts by looking into the capacitor and taking the Thevenin equivalent circuit:

$$V_{\mathrm{TH}} = \frac{\Delta V a}{Z_O C_L s + 1} \tag{8.2}$$

$$Z_{\mathrm{TH}} = \frac{Z_O}{Z_O C_L s + 1} \tag{8.3}$$

Then, the output equation is written:

$$V_{\mathrm{RETURN}} = \frac{V_{\mathrm{TH}} z_G}{Z_G + Z_F + Z_{\mathrm{TH}}} = \frac{\Delta V a}{Z_O C_L s + 1}\left(\frac{z_G}{Z_F + Z_G + \dfrac{Z_O}{Z_O C_L s + 1}}\right) \tag{8.4}$$

Rearranging terms yields Equation (8.5):

$$\frac{V_{\mathrm{RETURN}}}{V_{\mathrm{TEST}}} = A\beta = \frac{\dfrac{aZ_G}{Z_F + Z_G + Z_O}}{\dfrac{(Z_F + Z_G) Z_O C_L s}{Z_F + Z_G + Z_O} + 1} \tag{8.5}$$

When the assumption is made that $(Z_F + Z_G) \gg Z_O$, Equation (8.5) reduces to Equation (8.6):

$$A\beta = \frac{aZ_G}{Z_F + Z_G}\left(\frac{1}{Z_O C_L s + 1}\right) \tag{8.6}$$

Equation (8.7) models the op amp as a second order system. Hence, substituting the second order model for a in Equation (8.6) yields Equation (8.8), which is the stability equation for the dominant pole compensation circuit:

$$a = \frac{K}{(s + \tau_1)(s + \tau_2)} \tag{8.7}$$

$$A\beta = \frac{K}{(s + \tau_1)(s + \tau_2)} \frac{Z_G}{Z_F + Z_G} \frac{1}{Z_O C_L s + 1} \tag{8.8}$$

Several conclusions can be drawn from Equation (8.8), depending on the location of the poles. If the Bode plot of Equation (8.7), the op amp transfer function, looks like that shown in Figure 8.10, it has only a 25° phase margin and there is approximately a 48% overshoot. When the pole introduced by Z_O and C_L moves toward the zero frequency axis, it comes close to the τ_2 pole, and it adds phase shift to the system. Increased phase shift increases peaking and decreases stability. In the real world, many loads, especially cables, are capacitive; and an op amp like the one pictured in Figure 8.10 would ring while driving a capacitive load. The load capacitance causes peaking and instability in internally compensated op amps when the op amps do not have enough phase margin to allow for the phase shift introduced by the load.

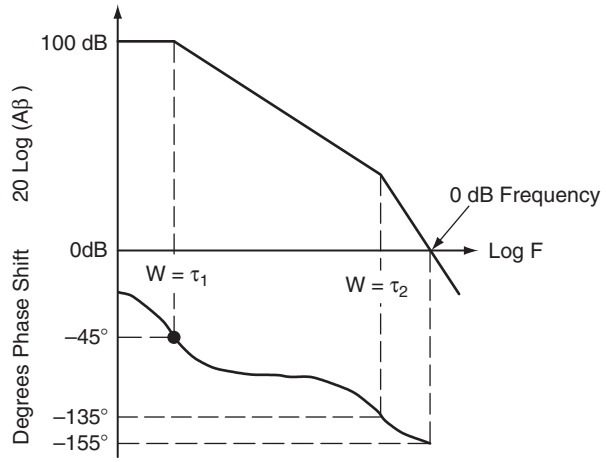


Figure 8.10: Possible Bode plot of the op amp described in Equation (8.7).

Prior to compensation, the Bode plot of an uncompensated op amp looks like that shown in Figure 8.11. Note that the break points are located close together, accumulating about 180° of phase shift before the 0 dB crossover point; the op amp is not usable and probably unstable. Dominant pole compensation is often used to stabilize these op amps. If a dominant pole, in this case ω_D, is properly placed, it rolls off the gain so that τ_1 introduces 45° phase at the 0 dB crossover point. After the dominant pole is introduced, the op amp is stable with 45° phase margin, but the op amp gain is drastically reduced for frequencies higher than ω_D. This procedure works well for internally compensated op amps but is seldom used for externally compensated op amps, because inexpensive discrete capacitors are readily available.

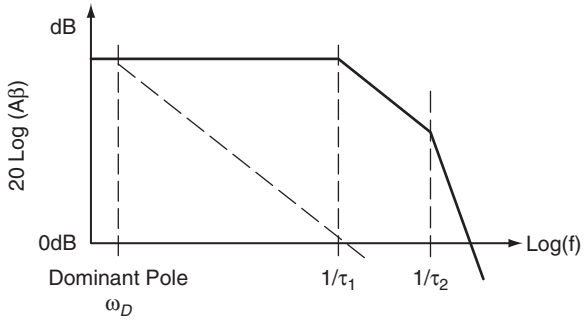


Figure 8.11: Dominant pole compensation plot.

Assuming that $Z_O \ll Z_F$, the closed loop transfer function is easy to calculate, because C_L is enclosed in the feedback loop. The ideal closed loop transfer equation is the same as Equation (7.11) for the noninverting op amp and is repeated here as Equation (8.9):

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{a}{1 + \dfrac{aZ_G}{Z_G + Z_F}} \tag{8.9}$$

When $a \Rightarrow \infty$, Equation (8.9) reduces to Equation (8.10):

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{Z_F + Z_G}{Z_G} \tag{8.10}$$

As long as the op amp has enough compliance and current to drive the capacitive load and Z_O is small, the circuit functions as though the capacitor were not there. When the capacitor becomes large enough, its pole interacts with the op amp pole, causing instability. When the capacitor is huge, it completely kills the op amp's bandwidth, thus lowering the noise while retaining a large low frequency gain.

8.5 Gain Compensation

When the closed loop gain of an op amp circuit is related to the loop gain, as it is in voltage feedback op amps, the closed loop gain can be used to stabilize the circuit. This type of compensation cannot be used in current feedback op amps because a

mathematical relationship between the loop gain and ideal closed loop gain does not exist. The loop gain equation is repeated as Equation (8.11). Note that the closed loop gain parameters Z_G and Z_F are contained in Equation (8.11); hence the stability can be controlled by manipulating the closed loop gain parameters:

$$A\beta = \frac{aZ_G}{Z_G + Z_F} \tag{8.11}$$

The original loop gain curve for a closed loop gain of 1 is shown in Figure 8.12, and it is or comes very close to being unstable. If the closed loop noninverting gain is changed to 9, then K changes from $K/2$ to $K/10$. The loop gain intercept on the Bode plot (Figure 8.12) moves down 14 dB and the circuit is stabilized.

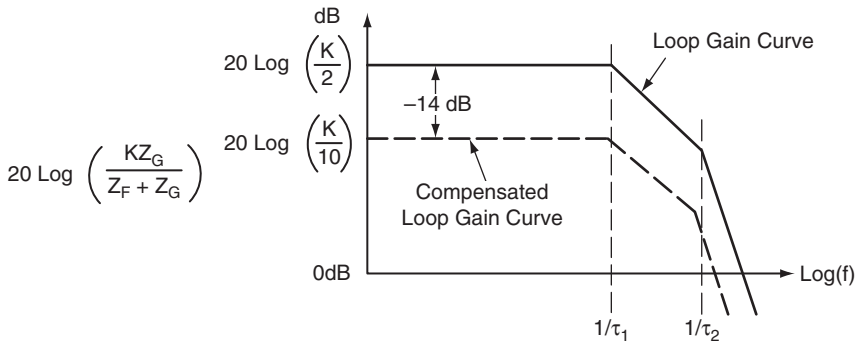


Figure 8.12: Gain compensation.

Gain compensation works for inverting or noninverting op amp circuits, because the loop gain equation contains the closed loop gain parameters in both cases. When the closed loop gain is increased, the accuracy and bandwidth decrease. As long as the application can stand the higher gain, gain compensation is the best type of compensation to use. Uncompensated versions of normally internally compensated op amps are offered for sale as stable op amps with minimum gain restrictions. As long as gain in the circuit designed exceeds the gain specified on the data sheet, this is economical and a safe mode of operation.

8.6 Lead Compensation

Sometimes lead compensation is forced on the circuit designer because of the parasitic capacitance associated with packaging and wiring op amps. Figure 8.13 shows the circuit for lead compensation; note the capacitor in parallel with R_F. That capacitor is often made by parasitic wiring and the ground plane, and high frequency circuit designers go to great lengths to minimize or eliminate it. What is good in one sense is bad in another, because adding the parallel capacitor is a good way to stabilize the op amp and reduce noise. Let's analyze the stability first, then we analyze the closed loop performance.

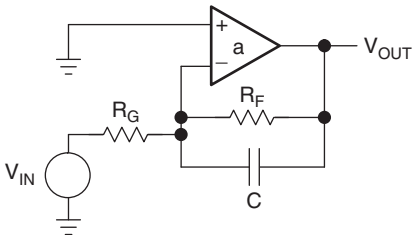


Figure 8.13: Lead compensation circuit.

The loop equation for the lead compensation circuit is given by Equation (8.12):

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{R_F C s + 1}{R_G \| R_F C s + 1}\right)\left(\frac{K}{(s + \tau_1)(s + \tau_2)}\right) \tag{8.12}$$

The compensation capacitor introduces a pole and zero into the loop equation. The zero always occurs before the pole because $R_F > R_F \| R_G$. When the zero is properly placed, it cancels out the τ_2 pole along with its associated phase shift. The original transfer function is shown in Figure 8.14, drawn in solid lines. When the $R_F C$ zero is placed at $\omega = 1/\tau_2$, it cancels out the τ_2 pole, causing the Bode plot to continue on a slope of -20 dB/decade. When the frequency gets to $\omega = 1/(R_F \| R_G)C$, this pole changes the slope to -40 dB/decade. Properly placed, the capacitor aids stability, but what does it do to the closed loop transfer function? The equation for the inverting op amp closed-loop gain is repeated here:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{-aZ_F}{Z_G + Z_F}}{1 + \dfrac{aZ_G}{Z_G + Z_F}} \tag{8.13}$$

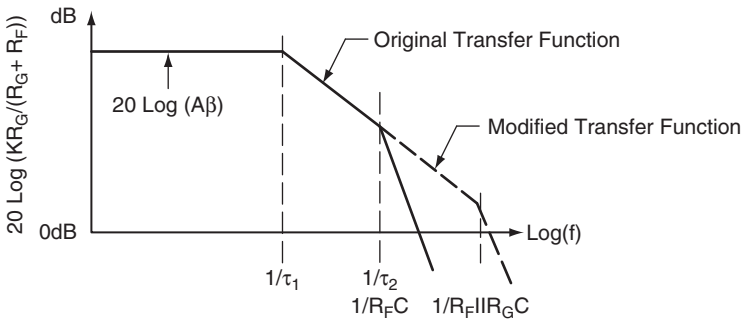


Figure 8.14: Lead compensation Bode plot.

When a approaches infinity, Equation (8.13) reduces to Equation (8.14):

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = -\frac{Z_F}{Z_{\text{IN}}} \tag{8.14}$$

Substituting $R_F \| C$ for Z_F and R_G for Z_G in Equation (8.14) yields Equation (8.15), which is the ideal closed loop gain equation for the lead compensation circuit:

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = -\frac{R_F}{R_G}\left(\frac{1}{R_F C s + 1}\right) \tag{8.15}$$

The forward gain for the inverting amplifier is given by Equation (8.16). Compare Equation (8.13) with Equation (6.5) to determine A:

$$A = \frac{aZ_F}{Z_G + A_F} = \left(\frac{aR_F}{R_G + R_F}\right)\left(\frac{1}{R_F \| R_G C s + 1}\right) \tag{8.16}$$

The op amp gain (a), the forward gain (A), and the ideal closed loop gain are plotted in Figure 8.15. The op amp gain is plotted for reference only. The forward gain for the inverting op amp is not the op amp gain. Note that the forward gain is reduced by the factor $R_F/(R_G + R_F)$, and it contains a high frequency pole. The ideal closed loop gain follows the ideal curve until the $1/R_F C$ break point (same location as $1/\tau_2$ break point), then it slopes down at -20 dB/decade. Lead compensation sacrifices the bandwidth between the $1/R_F C$ break point and the forward gain curve. The location

of the $1/R_FC$ pole determines the bandwidth sacrifice, and it can be much greater than shown here. The pole caused by R_F, R_G, and C does not appear until the op amp's gain has crossed the 0 dB axis, thus it does not affect the ideal closed loop transfer function.

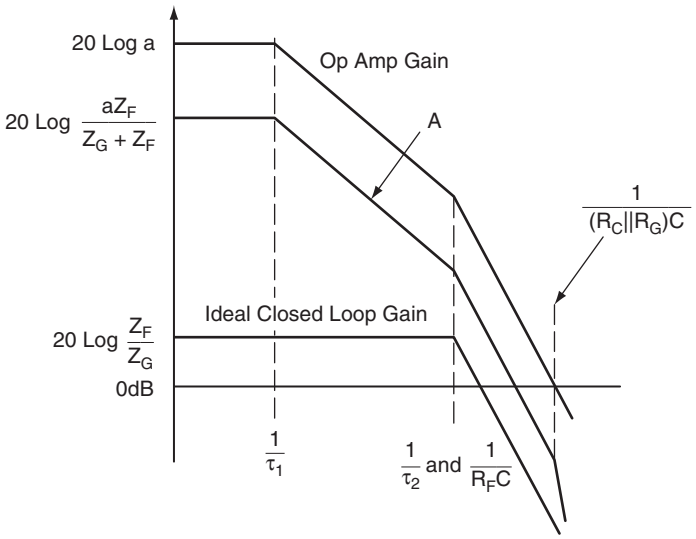


Figure 8.15: Inverting op amp with lead compensation.

The forward gain for the noninverting op amp is a; compare Equation (7.11) to Equation (7.5). The ideal closed loop gain is given by Equation (8.17):

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_F + Z_G}{Z_G} = \left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_F \| R_G Cs + 1}{R_F Cs + 1}\right) \tag{8.17}$$

The plot of the noninverting op amp with lead compensation is shown in Figure 8.16. There is only one plot for both the op amp gain (a) and the forward gain (A), because they are identical in the noninverting circuit configuration. The ideal starts out as a flat line, but it slopes down because its closed loop gain contains a pole and a zero. The pole always occurs closer to the low frequency axis, because $R_F > R_F \| R_G$. The zero flattens the ideal closed loop gain curve, but it never does any good because it cannot fall on the pole. The pole causes a loss in the closed loop bandwidth by the amount separating the closed loop and forward gain curves.

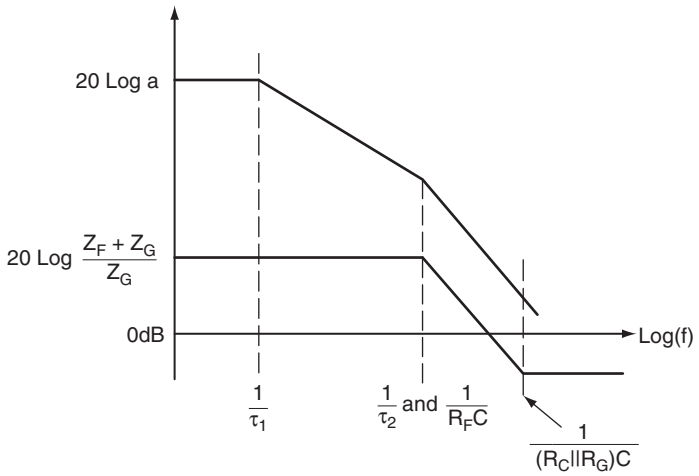


Figure 8.16: Noninverting op amp with lead compensation.

Although the forward gain is different in the inverting and noninverting circuits, the closed loop transfer functions take very similar shapes. This becomes truer as the closed loop gain increases because the noninverting forward gain approaches the op amp gain. This relationship cannot be relied on in every situation, and each circuit must be checked to determine the closed loop effects of the compensation scheme.

8.7 Compensated Attenuator Applied to Op Amp

Stray capacitance on op amp inputs is a problem that circuit designers are always trying to avoid, because it decreases stability and causes peaking. The circuit shown in Figure 8.17 has some stray capacitance (C_G) connected from the inverting input

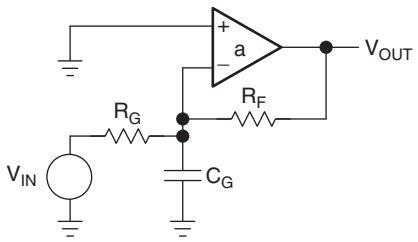


Figure 8.17: Op amp with stray capacitance on the inverting input.

to ground. Equation (8.18) is the loop gain equation for the circuit with input capacitance:

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{1}{R_G \| R_F C s + 1}\right)\left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right) \tag{8.18}$$

Op amps having high input and feedback resistors are subject to instability caused by stray capacitance on the inverting input. Referring to Equation (8.18), when the $1/(R_F \| R_G C_G)$ pole moves close to τ_2, the stage is set for instability. Reasonable component values for a CMOS op amp are $R_F = 1$ MΩ, $R_G = 1$ MΩ, and $C_G = 10$ pF. The resulting pole occurs at 318 kHz, and this frequency is lower than the break point of τ_2 for many op amps. A 90° of phase shift results from τ_1, the $1/(R_F \| R_G C)$ pole adds 45° phase shift at 318 kHz, and τ_2 starts to add another 45° phase shift at about 600 kHz. This circuit is unstable because of the stray input capacitance. The circuit is compensated by adding a feedback capacitor, as shown in Figure 8.18.

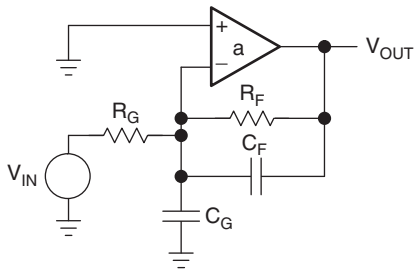


Figure 8.18: Compensated attenuator circuit.

The loop gain with C_F added is given by Equation (8.19):

$$A\beta = \left[\frac{\dfrac{R_G}{R_G C_G s + 1}}{\dfrac{R_G}{R_G C_G s + 1} + \dfrac{R_F}{R_F C_F s + 1}}\right]\left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right) \tag{8.19}$$

If $R_G C_G = R_F C_F$, Equation (8.19) reduces to Equation (8.20):

$$A\beta = \left[\frac{R_G}{R_G + R_F}\right]\left(\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right) \tag{8.20}$$

The compensated attenuator Bode plot is shown in Figure 8.19. Adding the correct $1/R_F C_F$ break point cancels out the $1/R_G C_G$ break point; the loop gain is independent of the capacitors. Now is the time to take advantage of the stray capacitance. C_F can be formed by running a wide copper strip from the output of the op amp over the ground plane under R_F; do not connect the other end of this copper strip. The circuit is tuned by removing some copper (a razor works well) until all peaking is eliminated. Then, measure the copper and have an identical trace put on the printed circuit board.

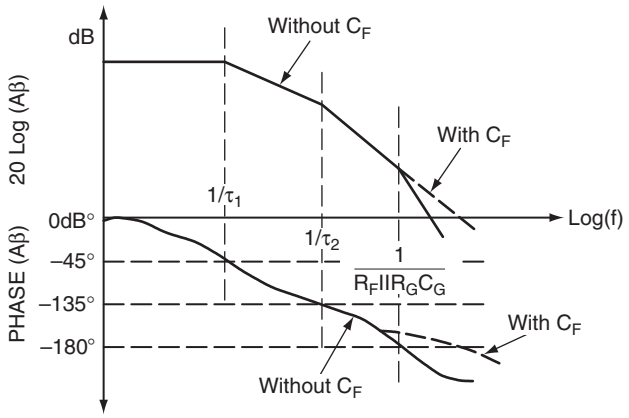


Figure 8.19: Compensated attenuator Bode plot.

The inverting and noninverting closed loop gain equations are a function of frequency. Equation (8.21) is the closed loop gain equation for the inverting op amp. When $R_F C_F = R_G C_G$, Equation (8.21) reduces to Equation (8.22), which is independent of the break point. This also happens to the noninverting op amp circuit. This is one of the few occasions when the compensation does not affect the closed loop gain frequency response.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{R_F}{R_F C_F s + 1}}{\dfrac{R_G}{R_G C_G s + 1}} \tag{8.21}$$

When $R_F C_F = R_G C_G$,

$$\frac{V_{OUT}}{V_{IN}} = -\left(\frac{R_F}{R_G}\right) \tag{8.22}$$

8.8 Lead/Lag Compensation

Lead/lag compensation stabilizes the circuit without sacrificing the closed loop gain performance. It is often used with uncompensated op amps. This type of compensation provides excellent high frequency performance. The circuit schematic is shown in Figure 8.20, and the loop gain is given by Equation (8.23):

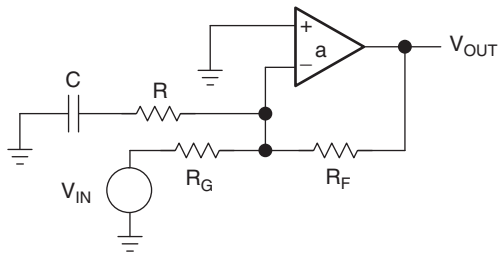


Figure 8.20: Lead/lag compensated op amp.

$$A\beta = \frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)} \frac{R_G}{R_G + R_F} \frac{RCs + 1}{\frac{(RR_G + RR_F + R_G R_F)}{(R_G + R_F)} Cs + 1} \tag{8.23}$$

Referring to Figure 8.21, a pole is introduced at $\omega = 1/RC$, and this pole reduces the gain 3 dB at the break point. When the zero occurs prior to the first op amp pole, it cancels out the phase shift caused by the $\omega = 1/RC$ pole. The phase shift is completely canceled before the second op amp pole occurs, and the circuit reacts as if the pole were never introduced. Nevertheless, $A\beta$ is reduced by 3 dB or more, so the loop gain crosses the 0 dB axis at a lower frequency. The beauty of lead/lag compensation is that the closed loop ideal gain is not affected, as is shown next. The Thevenin equivalent of the input circuit is calculated in Equation (8.24), the circuit gain in terms of Thevenin equivalents is calculated in Equation (8.25), and the ideal closed loop gain is calculated in Equation (8.26):

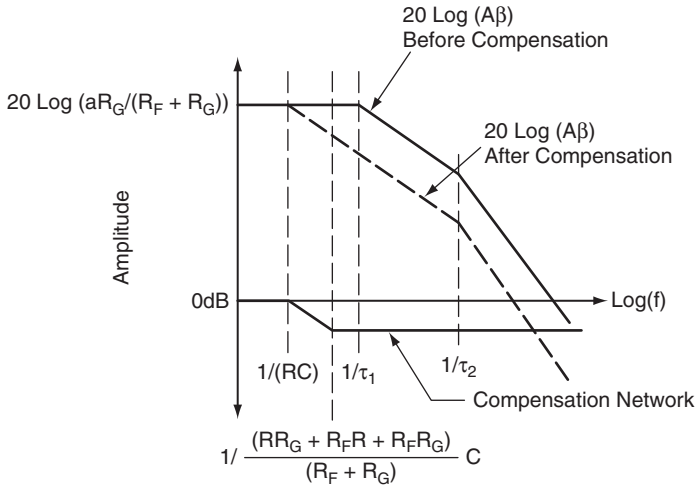


Figure 8.21: Bode plot of lead/lag compensated op amp.

$$V_{TH} = V_{IN}\frac{R + \frac{1}{Cs}}{R + R_G + \frac{1}{Cs}}, \quad R_{TH}\frac{R_G\left(R + \frac{1}{Cs}\right)}{R + R_G + \frac{1}{Cs}} \tag{8.24}$$

$$V_{OUT} = -V_{TH}\frac{R_F}{R_{TH}} \tag{8.25}$$

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R + \frac{1}{Cs}}{R + R_G + \frac{1}{Cs}}\frac{R_F}{\frac{R_G\left(R + \frac{1}{Cs}\right)}{R + R_G + \frac{1}{Cs}}} = \frac{R_F}{R_G} \tag{8.26}$$

Equation (8.26) is intuitively obvious, because the *RC* network is placed across a virtual ground. As long as the loop gain, $A\beta$, is large, the feedback nulls out the closed loop effect of *RC* and the circuit will function as if it were not there. The closed loop log plot of the lead/lag compensated op amp is given in Figure 8.22. Note that the pole and zero resulting from the compensation occur and are gone before the first amplifier poles come on the scene. This prevents interaction, but it is not required for stability.

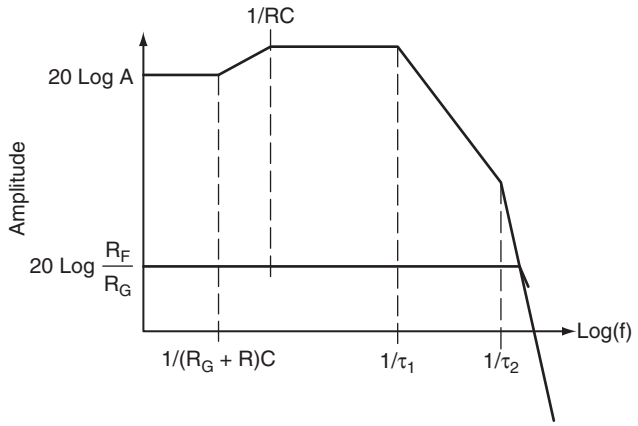


Figure 8.22: Closed loop plot of lead/lag compensated op amp.

8.9 Comparison of Compensation Schemes

Internally compensated op amps can, and often do, oscillate under some circuit conditions. Internally compensated op amps need an external pole to get the oscillation or ringing started, and circuit stray capacitances often supply the phase shift required for instability. Loads, such as cables, often cause internally compensated op amps to ring severely.

Dominant pole compensation is often used in IC design because it is easy to implement. It rolls off the closed loop gain early; therefore it is seldom used as an external form of compensation unless filtering is required. Load capacitance, depending on its pole location, usually causes the op amp to ring. Large load capacitance can stabilize the op amp because it acts as dominant pole compensation.

The simplest form of compensation is gain compensation. High closed loop gains are reflected in lower loop gains, and, in turn, lower loop gains increase stability. If an op amp circuit can be stabilized by increasing the closed loop gain, do it.

Stray capacitance across the feedback resistor tends to stabilize the op amp because it is a form of lead compensation. This compensation scheme is useful for limiting the circuit bandwidth, but it decreases the closed loop gain.

Stray capacitance on the inverting input works with the parallel combination of the feedback and gain setting resistors to form a pole in the Bode plot, and this pole

decreases the circuit's stability. This effect is normally observed in high impedance circuits built with CMOS op amps. Adding a feedback capacitor forms a compensated attenuator scheme that cancels out the input pole. The cancellation occurs when the input and feedback *RC* time constants are equal. Under the conditions of equal time constants, the op amp functions as though the stray input capacitance were not there. An excellent method of implementing a compensated attenuator is to build a stray feedback capacitor using the ground plane and a trace off the output node.

Lead/lag compensation stabilizes the op amp, and it yields the best closed loop frequency performance. Contrary to some published opinions, no compensation scheme increases the bandwidth beyond that of the op amp. Lead/lag compensation just gives the best bandwidth for the compensation.

8.10 Conclusions

The stability criteria often is not oscillation, rather it is circuit performance as exhibited by peaking and ringing.

The circuit bandwidth can often be increased by connecting an external capacitor in parallel with the op amp. Some op amps have hooks that enable a parallel capacitor to be connected in parallel with a portion of the input stages. This increases bandwidth because it shunts high frequencies past the low bandwidth g_m stages, but this method of compensation depends on the op amp type and manufacturer.

The compensation techniques given here are adequate for the majority of applications. When the new and challenging application presents itself, use the procedure outlined here to invent your own compensation technique.

CHAPTER 9

Current Feedback Op Amp Analysis

Ron Mancini

9.1 Introduction

Current feedback amplifiers (CFA) do not have the traditional differential amplifier input structure, therefore they sacrifice the parameter matching inherent to that structure. The CFA circuit configuration prevents them from obtaining the precision of voltage feedback amplifiers (VFA), but the circuit configuration that sacrifices precision results in increased bandwidth and slew rate. The higher bandwidth is relatively independent of closed loop gain, so the constant gain/bandwidth restriction applied to VFAs is removed for CFAs. The slew rate of CFAs is much improved from their counterpart VFAs, because their structure enables the output stage to supply slewing current until the output reaches its final value. In general, VFAs are used for precision and general purpose applications, while CFAs are restricted to high frequency applications, above 100 MHz.

Although CFAs lack the precision of their VFA counterparts, they are precise enough to be DC coupled in video applications, where dynamic range requirements are not severe. CFAs, unlike previous generation high frequency amplifiers, have eliminated the AC coupling requirement; they are usually DC coupled while they operate in the gigahertz range. CFAs have much faster slew rates than VFAs, so they have faster rise and fall times and less intermodulation distortion.

9.2 CFA Model

The CFA model is shown in Figure 9.1. The noninverting input of a CFA connects to the input of the input buffer, so it has very high impedance, similar to that of a bipolar

transistor noninverting VFA input. The inverting input connects to the input buffer's output, so the inverting input impedance is equivalent to a buffer's output impedance, which is very low. Z_B models the input buffer's output impedance, and it is usually less than 50 Ω. The input buffer gain, G_B, is as close to 1 as IC design methods can achieve, and it is small enough to neglect in the calculations.

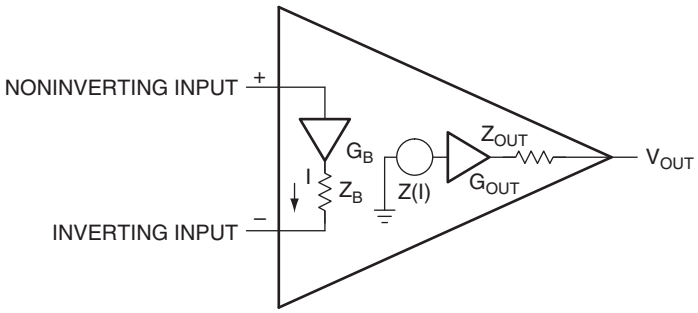


Figure 9.1: Current feedback amplifier model.

The output buffer provides low output impedance for the amplifier. Again, the output buffer gain, G_{OUT}, is very close to 1, so it is neglected in the analysis. The output impedance of the output buffer is ignored during the calculations. This parameter may influence the circuit performance when driving very low impedance or capacitive loads, but this is usually not the case. The input buffer's output impedance can't be ignored because it affects stability at high frequencies.

The current controlled current source, Z, is a transimpedance. The transimpedance in a CFA serves the same function as gain in a VFA: It is the parameter that makes the performance of the op amp dependent only on the passive parameter values. Usually the transimpedance is very high, in the megaohm range, so the CFA gains accuracy by closing a feedback loop in the same manner as the VFA.

9.3 Development of the Stability Equation

The stability equation is developed with the aid of Figure 9.2 Remember, stability is independent of the input and depends solely on the loop gain, $A\beta$. Breaking the loop at point X, inserting a test signal, V_{TI}, and calculating the return signal, V_{TO}, develops the stability equation.

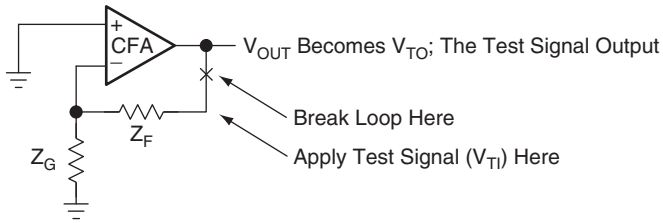


Figure 9.2: Stability analysis circuit.

The circuit used for stability calculations is shown in Figure 9.3, where the model of Figure 9.1 is substituted for the CFA symbol. The input and output buffer gain and the output buffer output impedance have been deleted from the circuit to simplify calculations. This approximation is valid for almost all applications.

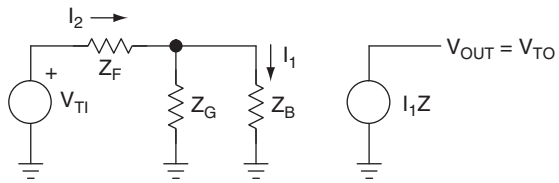


Figure 9.3: Stability analysis circuit.

The transfer equation is given in Equation (9.1), and Kirchhoff's law is used to write Equations (9.2) and (9.3):

$$V_{\mathrm{TO}} = I_1 Z \tag{9.1}$$

$$V_{\mathrm{TI}} = I_2(Z_F + Z_G \| Z_B) \tag{9.2}$$

$$I_2(Z_G \| Z_B) = I_1 Z_B \tag{9.3}$$

Equations (9.2) and (9.3) are combined to yield Equation (9.4):

$$V_{\mathrm{TI}} = I_1(Z_F + Z_G \| Z_B)\left(1 + \frac{Z_B}{Z_G}\right) = I_1 Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right) \tag{9.4}$$

Dividing Equation (9.1) by Equation (9.4) yields Equation (9.5), and this is the open loop transfer equation. This equation is commonly known as the *loop gain*.

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left[Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)\right]} \tag{9.5}$$

9.4 The Noninverting CFA

The closed loop gain equation for the noninverting CFA is developed with the aid of Figure 9.4, where external gain setting resistors have been added to the circuit. The buffers are shown in Figure 9.4, but because their gains equal 1 and they are included within the feedback loop, the buffer gain does not enter into the calculations.

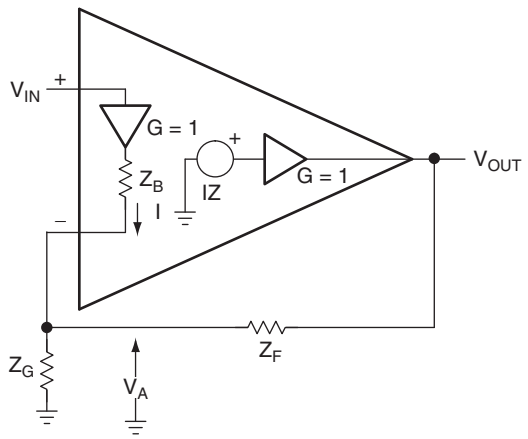


Figure 9.4: Noninverting CFA.

Equation (9.6) is the transfer equation, Equation (9.7) is the current equation at the inverting node, and Equation (9.8) is the input loop equation. These equations are combined to yield the closed loop gain equation, Equation (9.9).

$$V_{OUT} = I_Z \tag{9.6}$$

$$I = \left(\frac{V_A}{Z_G}\right) - \left(\frac{V_{OUT} - V_A}{Z_F}\right) \tag{9.7}$$

$$V_A = V_{IN} - IZ_B \tag{9.8}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{Z\left(1 + \dfrac{Z_F}{Z_G}\right)}{Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}}{1 + \dfrac{Z}{Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}} \tag{9.9}$$

When the input buffer output impedance, Z_B, approaches zero, Equation (9.9) reduces to Equation (9.10):

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{Z\left(1 + \dfrac{Z_F}{Z_G}\right)}{Z_F}}{1 + \dfrac{Z}{Z_F}} = \frac{1 + \dfrac{Z_F}{Z_G}}{1 + \dfrac{Z_F}{Z}} \tag{9.10}$$

When the transimpedance, Z, is very high, the term Z_F/Z in Equation (9.10) approaches zero, and Equation (9.10) reduces to Equation (9.11), the ideal closed loop gain equation for the CFA. The ideal closed loop gain equations for the CFA and VFA are identical, and the degree to which they depart from ideal depends on the validity of the assumptions. The VFA has one assumption, that the direct gain is very high, while the CFA has two assumptions, that the transimpedance is very high and the input buffer output impedance is very low. As would be expected, two assumptions are much harder to meet than one, so the CFA departs from the ideal more than the VFA.

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{Z_F}{Z_G} \tag{9.11}$$

9.5 The Inverting CFA

The inverting CFA configuration (Figure 9.5) is seldom used, because the inverting input impedance is very low ($Z_B \| Z_F + Z_G$). When Z_G is made dominant by selecting it as a high resistance value, it overrides the effect of Z_B. Z_F must also be selected as a high value to achieve at least unity gain, and high values for Z_F result in poor bandwidth performance, as we see in the next section. If Z_G is selected as a low value, the frequency sensitive Z_B causes the gain to increase as frequency increases. These limitations restrict inverting applications of the inverting CFA.

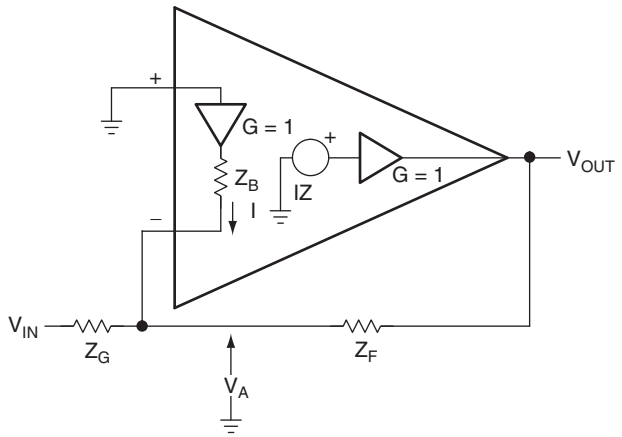


Figure 9.5: Inverting CFA.

The current equation for the input node is written as Equation (9.12). Equation (9.13) defines the dummy variable V_A, and Equation (9.14) is the transfer equation for the CFA. These equations are combined and simplified, leading to Equation (9.15), which is the closed loop gain equation for the inverting CFA.

$$1 + \frac{V_{\text{IN}} - V_A}{Z_G} = \frac{V_A - V_{\text{OUT}}}{Z_F} \tag{9.12}$$

$$IZ_B = -V_A \tag{9.13}$$

$$IZ = V_{\text{OUT}} \tag{9.14}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\dfrac{Z}{Z_G\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}}{1 + \dfrac{Z}{Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)}} \tag{9.15}$$

When Z_B approaches zero, Equation (9.15) reduces to Equation (9.16):

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\dfrac{1}{Z_G}}{\dfrac{1}{Z} + \dfrac{1}{Z_F}} \tag{9.16}$$

When Z is very large, Equation (9.16) becomes Equation (9.17), which is the ideal closed loop gain equation for the inverting CFA:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{Z_G} \tag{9.17}$$

The ideal closed loop gain equation for the inverting VFA and CFA op amps are identical. Both configurations have lower input impedance than the noninverting configuration, but the VFA has one assumption while the CFA has two assumptions. Again, as was the case with the noninverting counterparts, the CFA is less ideal than the VFA because of the two assumptions. The zero Z_B assumption always breaks down in bipolar junction transistors, as is shown later. The CFA is almost never used in the differential amplifier configuration because of the CFA's gross input impedance mismatch.

9.6 Stability Analysis

The stability equation is repeated as (Equation 9.18):

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left[Z_F\left(1 + \dfrac{Z_B}{Z_F \| Z_G}\right)\right]} \tag{9.18}$$

Comparing Equations (9.9) and (9.15) to Equation (9.18) reveals that the inverting and noninverting CFA op amps have identical stability equations. This is the expected result because stability of any feedback circuit is a function of the loop gain, and the input signals have no effect on stability. The two op amp parameters affecting stability are the transimpedance, Z, and the input buffer's output impedance, Z_B. The external components affecting stability are Z_G and Z_F. The designer controls the external impedance, although stray capacitance that is a part of the external impedance sometimes seems to be uncontrollable. Stray capacitance is the primary cause of ringing and overshooting in CFAs. Z and Z_B are CFA op amp parameters that can't be controlled by the circuit designer, who has to live with them.

Prior to determining stability with a Bode plot, we take the log of Equation (9.18) and plot the logs, Equations (9.19) and (9.20), in Figure 9.6:

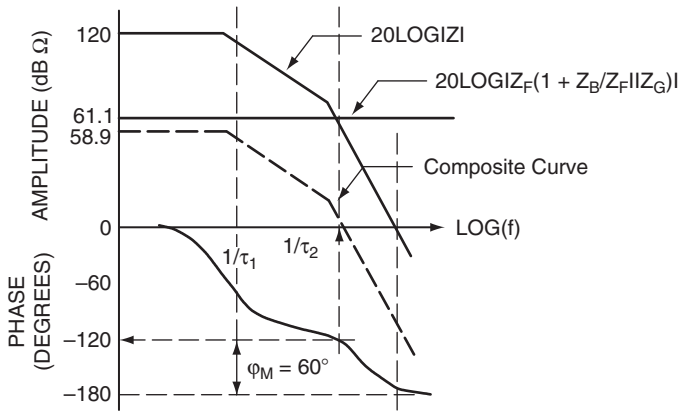


Figure 9.6: Bode plot of stability equation.

$$20\ \log|A\beta| = 20\ \log|Z| - 20\ \log\left|Z_F\left(1 + \frac{Z_B}{Z_F \| Z_B}\right)\right| \tag{9.19}$$

$$\varphi = \text{tangent}^{-1}(A\beta) \tag{9.20}$$

This enables the designer to add and subtract components of the stability equation graphically.

The plot in Figure 9.6 assumes typical values for the parameters

$$Z = \frac{1\text{M}\Omega}{(1 + \tau_1 S)(1 + \tau_2 S)} \tag{9.21}$$

$$Z_B = 70\ \Omega \tag{9.22}$$

$$Z_G = Z_F = 1\text{k}\ \Omega \tag{9.23}$$

The transimpedance has two poles, and the plot shows that the op amp is unstable without the addition of external components, because 20 log|Z| crosses the 0 dB axis after the phase shift is 180°. Z_F, Z_B, and Z_G reduce the loop gain 61.1 dB, so the circuit is stable because it has a 60° phase margin. Z_F is the component that stabilizes the circuit. The parallel combination of Z_F and Z_G contribute little to the phase margin, because Z_B is very small, so Z_B and Z_G have little effect on stability.

The manufacturer determines the optimum value of R_F during the characterization of the IC. Referring to Figure 9.6, we see that, when R_F exceeds the optimum value recommended by the IC manufacturer, stability increases. The increased stability has a price, called *decreased bandwidth*. Conversely, when R_F is less than the optimum value recommended by the IC manufacturer, stability decreases, and the circuit response to step inputs is overshooting or possibly ringing. Sometimes the overshoot associated with less than optimum R_F is tolerated because the bandwidth increases as R_F decreases. The peaked response associated with less than optimum values of R_F can be used to compensate for cable droop caused by cable capacitance.

When $Z_B = 0\ \Omega$ and $Z_F = R_F$, the loop gain equation is $A\beta = Z/R_F$. Under these conditions, Z and R_F determine stability, and a value of R_F can always be found to stabilize the circuit. The transimpedance and feedback resistor have a major impact on stability, and the input buffer's output impedance has a minor effect on stability. Since Z_B increases with an increase in frequency, it tends to increase stability at higher frequencies. Equation (9.18) is rewritten as Equation (9.24), but it has been manipulated so that the ideal closed loop gain is readily apparent:

$$A\beta = \frac{Z}{Z_F + Z_B\left(1 + \dfrac{R_F}{R_G}\right)} \tag{9.24}$$

The closed loop ideal gain equation (inverting and noninverting) shows up in the denominator of Equation (9.24), so the closed loop gain influences the stability of the op amp. When Z_B approaches zero, the closed loop gain term also approaches zero, and the op amp becomes independent of the ideal closed loop gain. Under these conditions R_F determines stability, and the bandwidth is independent of the closed loop gain. Many people claim that the CFA bandwidth is independent of the gain, and that claim's validity depends on the ratio Z_B/Z_F being very low.

Z_B is important enough to warrant further investigation, so the equation for Z_B follows:

$$Z_B \cong h_{\text{ib}} + \frac{R_B}{\beta_0 + 1}\left[\frac{1 + \dfrac{s\beta_0}{\omega_T}}{1 + \dfrac{s\beta_0}{(\beta_0 + 1)\omega_T}}\right] \tag{9.25}$$

At low frequencies $h_{\text{ib}} = 50\ \Omega$ and $R_B/(\beta_0 + 1) = 25$, so $Z_B = 75\ \Omega$. Z_B varies in accordance with Equation (9.25) at high frequencies. Also, the transistor parameters in Equation (9.25) vary with transistor type; they are different for NPN and PNP transistors. Because Z_B depends on the output transistors used, and this is a function of the quadrant the output signal is in, Z_B has an extremely wide variation. Z_B is a small factor in the equation, but it adds a lot of variability to the current feedback op amp.

9.7 Selection of the Feedback Resistor

The feedback resistor determines stability, and it affects closed loop bandwidth, so it must be selected very carefully. Most CFA IC manufacturers employ applications and product engineers who spend a great deal of time and effort selecting R_F. They measure each noninverting gain with several feedback resistors to gather data. Then they pick a compromise value of R_F that yields stable operation with acceptable peaking, and that value of R_F is recommended on the data sheet for that specific gain. This procedure is repeated for several gains in

anticipation of the various gains customer applications require (often $G = 1$, 2, or 5). When the value of R_F or the gain is changed from the values recommended on the data sheet, bandwidth and/or stability is affected.

A circuit designer who must select a different R_F value from that recommended on the data sheet gets into stability or low bandwidth problems. Lowering R_F decreases stability, and increasing R_F decreases bandwidth. What happens when the designer needs to operate at a gain not specified on the data sheet? The designer must select a new value of R_F for the new gain, but there is no guarantee that new value of R_F is an optimum value. One solution to the R_F selection problem is to assume that the loop gain, $A\beta$, is a linear function. Then, the assumption can be made that $(A\beta)_1$ for a gain of 1 equals $(A\beta)_N$ for a gain of N, and that this is a linear relationship between stability and gain. Equations (9.26) and (9.27) are based on the linearity assumption:

$$\frac{Z}{Z_{F1} + Z_B\left(1 + \dfrac{Z_{F1}}{Z_{G1}}\right)} = \frac{Z}{Z_{FN} + Z_B\left(1 + \dfrac{Z_{FN}}{Z_{GN}}\right)} \tag{9.26}$$

$$Z_{FN} = Z_{F1} + Z_B\left[\left(1 + \frac{Z_{F1}}{Z_{G1}}\right) - \left(1 + \frac{Z_{FN}}{Z_{GN}}\right)\right] \tag{9.27}$$

Equation (9.27) leads one to believe that a new value Z_F can easily be chosen for each new gain. This is not the case in the real world; the assumptions don't hold up well enough to rely on them. When changing to a new gain not specified on the data sheet, Equation (9.27), at best, supplies a starting point for R_F, but it must be tested to determine the final value of R_F.

When the R_F value recommended on the data sheet can't be used, an alternate method of selecting a starting value for R_F is to use graphical techniques. The graph shown in Figure 9.7 is a plot of the typical 300 MHz CFA data given in Table 9.1.

Enter the graph at the new gain, say $A_{CL} = 6$, and move horizontally until you reach the intersection of the gain versus feedback resistance curve. Then, drop vertically to the

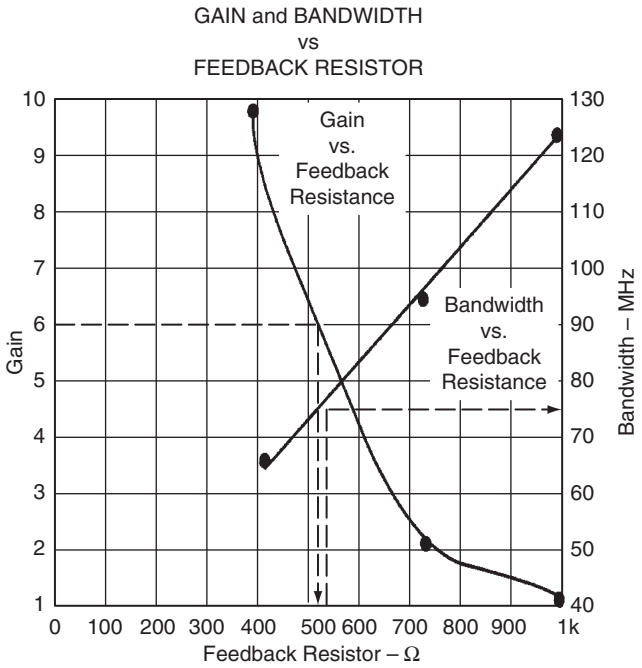


Figure 9.7: Plot of CFA R_F, gain, and bandwidth.

Table 9.1: Data Set for Curves in Figure 9.7

Gain (A_{CL})	R_F (Ω)	Bandwidth (MH_Z)
+1	1000	125
+2	681	95
+10	383	65

resistance axis and read the new value of R_F (500 Ω in this example). Enter the graph at the new value of R_F and travel vertically until you intersect the bandwidth versus feedback resistance curve. Now, move to the bandwidth axis to read the new bandwidth (75 MHz in this example). As a starting point, you should expect to get approximately 75 MHz bandwidth with a gain of 6 and $R_F = 500$ Ω. Although this technique yields more reliable solutions than Equation (9.27), op amp peculiarities,

circuit board stray capacitances, and wiring make extensive testing mandatory. The circuit must be tested for performance and stability at each new operating point.

9.8 Stability and Input Capacitance

When the designer lets the circuit board introduce stray capacitance on the inverting input node to ground, it causes the impedance Z_G to become reactive. The new impedance, Z_G, is given in Equation (9.28), and Equation (9.29) is the stability equation that describes the situation:

$$Z_G = \frac{R_G}{1 + R_G C_G s} \tag{9.28}$$

$$A\beta = \frac{Z}{Z_B + \dfrac{Z_F}{Z_G^2 + Z_B Z_G}} \tag{9.29}$$

$$A\beta = \frac{2}{R_F\left(1 + \dfrac{R_B}{R_F \| R_G}\right)(1 + R_B \| R_F \| R_G C_G s)} \tag{9.30}$$

Equation (9.29) is the stability equation when Z_G consists of a resistor in parallel with stray capacitance between the inverting input node and ground. The stray capacitance, C_G, is a fixed value because it depends on the circuit layout. The pole created by the stray capacitance depends on R_B because it dominates R_F and R_G. R_B fluctuates with manufacturing tolerances, so the $R_B C_G$ pole placement is subject to IC manufacturing tolerances. As the $R_B C_G$ combination becomes larger, the pole moves toward the zero frequency axis, lowering the circuit stability. Eventually it interacts with the pole contained in Z, $1/T_2$, and instability results.

The effects of stray capacitance on CFA closed loop performance are shown in Figure 9.8.

Note that the introduction of C_G causes more than 3 dB peaking in the CFA frequency response plot, and it increases the bandwidth about 18 MHz. Two picofarads are not a lot of capacitance, because a sloppy layout can easily add 4 pF or more to the circuit.

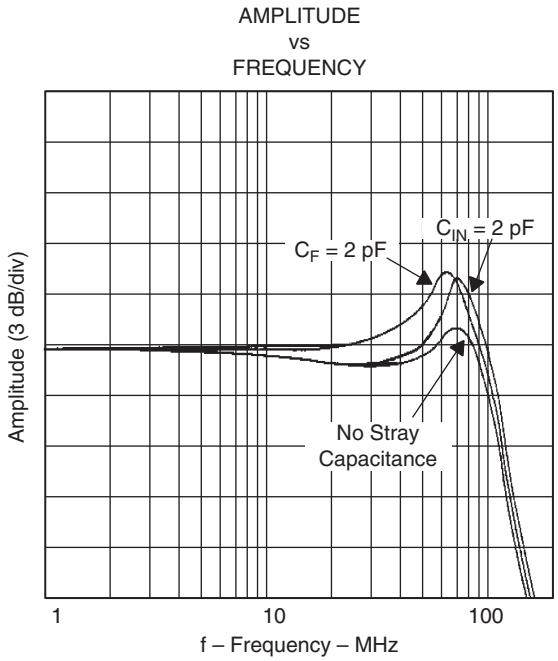


Figure 9.8: Effects of stray capacitance on CFAs.

9.9 Stability and Feedback Capacitance

When a stray capacitor is formed across the feedback resistor, the feedback impedance is given by Equation (9.31). Equation (9.32) gives the loop gain when a feedback capacitor has been added to the circuit.

$$Z_F = \frac{R_F}{1 + R_F C_F s} \tag{9.31}$$

$$A\beta = \frac{Z(1 + R_F C_F s)}{R_F\left(1 + \dfrac{R_B}{R_F \| R_G}\right)(1 + R_B \| R_F \| R_G C_F s)} \tag{9.32}$$

This loop gain transfer function contains a pole and zero, therefore, depending on the pole/zero placement, oscillation can result. The Bode plot for this case is shown in Figure 9.9. The original and composite curves cross the 0 dB axis with a slope of

–40 dB/decade, so either curve can indicate instability. The composite curve crosses the 0 dB axis at a higher frequency than the original curve, hence the stray capacitance has added more phase shift to the system. The composite curve is surely less stable than the original curve. Adding capacitance to the inverting input node or across the feedback resistor usually results in instability. R_B largely influences the location of the pole introduced by C_F, so here is another case where stray capacitance leads to instability.

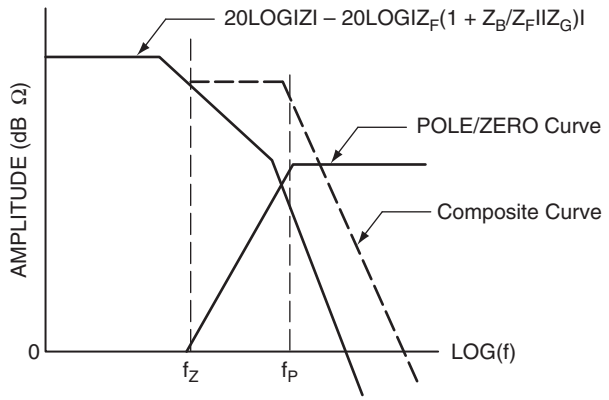


Figure 9.9: Bode plot with C_F.

Figure 9.8 shows that $C_F = 2$ pF adds about 4 dB of peaking to the frequency response plot. The bandwidth increases about 10 MHz because of the peaking. C_F and C_G are the major causes of overshooting, ringing, and oscillation in CFAs; and the circuit board layout must be carefully done to eliminate these stray capacitances.

9.10 Compensation of C_F and C_G

When both C_F and C_G are present in the circuit, they may be adjusted to cancel out each other. The stability equation for a circuit with C_F and C_G is Equation (9.33):

$$A\beta = \frac{Z(1 + R_F C_F s)}{R_F\left(1 + \dfrac{R_B}{R_F \| R_G}\right)[R_B \| R_F \| R_G (C_F + C_G)s + 1]} \tag{9.33}$$

If the zero and pole in Equation (9.33) are made to cancel each other, the only poles remaining are in Z. Setting the pole and zero in Equation (9.33) equal yields Equation (9.34) after some algebraic manipulation:

$$R_F C_F = C_G(R_G \| R_B) \tag{9.34}$$

R_B dominates the parallel combination of R_B and R_G, so Equation (9.34) is reduced to Equation (9.35):

$$R_F C_F = R_B C_G \tag{9.35}$$

R_B is an IC parameter, so it depends on the IC process. R_B it is an important IC parameter, but it is not important enough to be monitored as a control variable during the manufacturing process. R_B has widely spread, unspecified parameters; so depending on R_B for compensation is risky. Rather, the prudent design engineer assures that the circuit will be stable for any reasonable value of R_B and the resulting frequency response peaking is acceptable.

9.11 Summary

Constant gain/bandwidth is not a limiting criterion for the CFA, so the feedback resistor is adjusted for maximum performance. Stability depends on the feedback resistor: As R_F is decreased, stability is decreased; and when R_F goes to zero, the circuit becomes unstable. As R_F is increased stability increases, but the bandwidth decreases.

The inverting input impedance is very high, but the noninverting input impedance is very low. This situation precludes CFAs from operation in the differential amplifier configuration. Stray capacitance on the inverting input node or across the feedback resistor always leads to peaking, usually to ringing, and sometimes to oscillations. A prudent circuit designer scans the PC board layout for stray capacitances and eliminates them. Breadboarding and lab testing are a must with CFAs. The CFA performance can be improved immeasurably with a good layout, good decoupling capacitors, and low inductance components.

CHAPTER 10

Voltage and Current Feedback Op Amp Comparison

Ron Mancini and James Karki

10.1 Introduction

The name *operational amplifier* was given to voltage feedback amplifiers (VFA) when they were the only op amps in existence. These new (they were new in the late 1940s) amplifiers could be programmed with external components to perform various math operations on a signal, so they were nicknamed *op amps*. Current feedback amplifiers (CFA) have been around approximately 20 years, but their popularity increased in only the last several years. Two factors limit the popularity of CFAs, their application difficulty and lack of precision.

The VFA is a familiar component, and several variations of internally compensated VFAs can be used with little application work. Because of its long history, the VFA comes in many varieties and packages, so there are VFAs applicable to almost any job. VFA bandwidth is limited, so it can't function as well at high signal frequencies as the CFA. For now, the signal frequency and precision separates the applications of the two op amp configurations.

The VFA has other redeeming virtues, such as excellent precision, that makes it the desirable amplifier in low frequency applications. Many functions other than signal amplification are accomplished at low frequencies, and functions like level shifting a signal require precision. Fortunately, precision is not required in most high frequency applications, where amplification or filtering of a signal is predominant, so CFAs

are suitable to high frequency applications. The lack of precision coupled with the application difficulties prevents the CFA from replacing the VFA.

10.2 Precision

The long tailed pair input structure, which gives the VFA its precision, is shown in Figure 10.1.

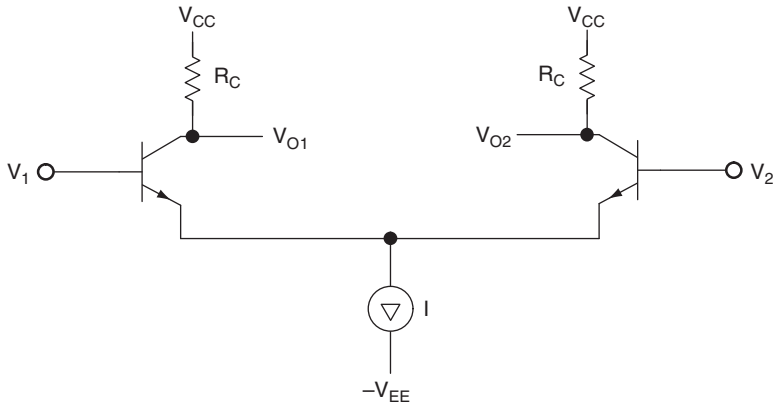


Figure 10.1: Long tailed pair.

The transistors, Q_1 and Q_2, are very carefully matched for initial and drift tolerances. Careful attention is paid to detail in the transistor design to ensure that parameters like current gain, β, and base emitter voltage, V_{BE}, are matched between the input transistors, Q_1 and Q_2. When $V_{B1} = V_{B2}$, the current, I, splits equally between the transistors, and $V_{O1} = V_{O2}$. As long as the transistor parameters are matched, the collector currents stay equal. The slightest change of V_{B1} with respect to V_{B2} causes a mismatch in the collector currents and a differential output voltage $|V_{B1} - V_{B2}|$.

When temperature or other outside influences change transistor parameters like current gain or base emitter voltage, as long as the change is equal, it causes no change in the differential output voltage. IC designers go to great lengths to ensure that transistor parameter changes due to external influences do not cause a differential output voltage change. Now, the slightest change in either base voltage causes a differential output voltage change, and gross changes in external conditions do not cause a differential

output voltage change. This is the formula for a precision amplifier because it can amplify small input changes while ignoring changes in the parameters or ambient conditions.

This is a simplified explanation, and many techniques are used to ensure transistor matching. Some of the techniques used to match input transistors are parameter trimming, special layout techniques, thermal balancing, and symmetrical layouts. The long tailed pair is an excellent circuit configuration for obtaining precision in the input circuit, but the output circuit has one fault. The output circuit collector impedance has to be high to achieve high gain in the first stage. High impedance coupled with the Miller capacitance, discussed in Chapter 8, forms a quasidominant pole compensation circuit that has poor high frequency response.

The noninverting input of the CFA (see Figure 10.2) connects to a buffer input inside the op amp. The inverting input of the CFA connects to a buffer output inside the CFA. Buffer inputs and outputs have dramatically different impedance levels, so any matching becomes a moot point. The buffer can't reject common mode voltages introduced by parameter drifts because it has no common mode rejection capability. The input current causes a voltage drop across the input buffer's output impedance, R_B, and there is no way that this voltage drop can be distinguished from an input signal.

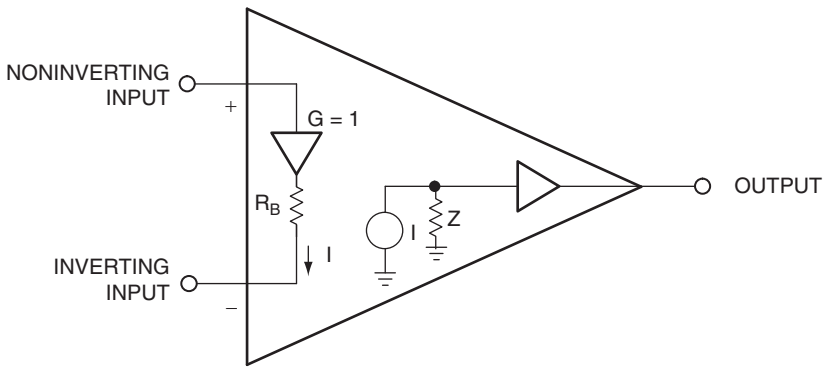


Figure 10.2: Ideal CFA.

The CFA circuit configuration was selected for high frequency amplification because it has current controlled gain and a current dominant input. Being a current device, the CFA does not have the Miller effect problem of the VFA. The input structure of the CFA sacrifices precision for bandwidth, but CFAs achieve usable bandwidths 10 times the usable VFA bandwidth.

10.3 Bandwidth

The bandwidth of a circuit is defined by high frequency errors. When the gain falls off at high frequencies, unequal frequency amplification causes the signal to become distorted. The signal loses its high frequency components; an example of high frequency signal degradation is a square wave with sharp corners that is amplified and turned into a slump cornered semi sine wave. The error equation for any feedback circuit is repeated in Equation (10.1):

$$E = \frac{V_{IN}}{1 + A\beta} \tag{10.1}$$

This equation is valid for any feedback circuit, so it applies equally to a VFA or a CFA. The loop gain equation for any VFA is repeated as Equation (10.2):

$$A\beta = \frac{aR_G}{R_F + R_G} \tag{10.2}$$

Equation (10.2) is rewritten as Equations (10.3) and (10.4) for the noninverting and inverting circuits, respectively. In each case, the symbols G_{CLNI} and G_{CLI} represent the closed loop gain for the noninverting and inverting circuits, respectively.

$$A\beta = \frac{a}{\frac{R_F + R_G}{R_G}} = \frac{a}{G_{CLNI}} \tag{10.3}$$

$$A\beta = \frac{a}{\frac{R_F + R_G}{R_G}} = \frac{a}{G_{CLI} + 1} \tag{10.4}$$

In both cases, the loop gain decreases as the closed loop gain increases, thus all VFA errors increase as the closed loop gain increases. The error increase is mathematically coupled to the closed loop gain equation, so there is no working around this fact. For the VFA, the effective bandwidth decreases as the closed loop gain increases, because the loop gain decreases as the closed loop gain increases.

A plot of the VFA loop gain, closed loop gain, and error is given in Figure 10.3. Referring to Figure 10.3, the direct gain, A, is the op amp open loop gain, a, for a noninverting op amp. The direct gain for an inverting op amp is $\{a[Z_F/(Z_G + Z_F)]\}$. The Miller effect causes the direct gain to fall off at high frequencies, so the error increases as frequency increases, because the effective loop gain decreases. At a given frequency, the error also increases when the closed loop gain is increased.

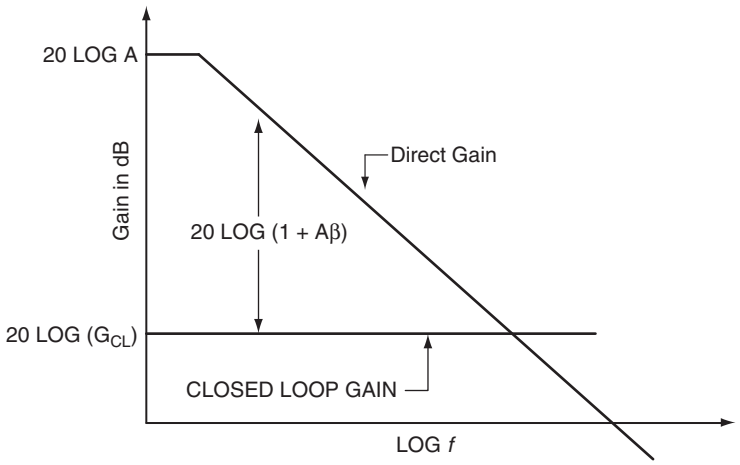


Figure 10.3: VFA gain versus frequency.

The CFA is a current operated device; hence it not nearly as subject to the Miller effect resulting from stray capacitance as the VFA. The absence of the Miller effect enables the CFA's frequency response to hold up far better than the VFA's. A plot of the CFA loop gain, transimpedance, and error is given in Figure 10.4. Note that the transimpedance stays at the large low frequency intercept value until much higher frequencies than in the VFA.

The loop gain equation for the CFA is repeated here as Equation (10.5):

$$A\beta = \frac{Z}{R_F\left(1 + \dfrac{R_B}{R_F \| R_G}\right)} \tag{10.5}$$

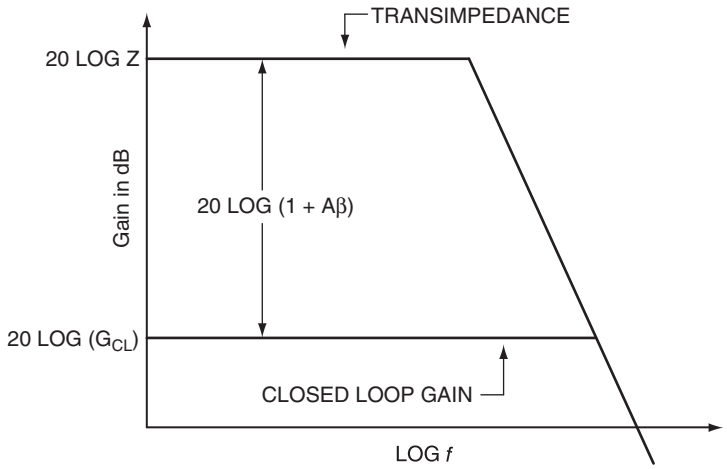


Figure 10.4: CFA gain versus frequency.

When the input buffer output resistance approaches zero, Equation (10.5) reduces to Equation (10.6):

$$A\beta = \frac{Z}{R_F} \tag{10.6}$$

Equation (10.6) shows that the closed loop gain has no effect on the loop gain when $R_B = 0$, so under ideal conditions, one would expect the transimpedance to fall off with a zero slope. Figure 10.4 shows that there is a finite slope, but much less than that of a VFA, and the slope is caused by $R_B \neq 0$. For example, R_B is usually 50 Ω when $R_F = 1000$ Ω at $A_{CL} = 1$. If we let $R_F = R_G$, then $R_F \| R_G = 500$ Ω and $R_B/R_F \| R_G = 50/500 = 0.1$.

Substituting this value into Equation (10.6) yields Equation (10.7), and Equation (10.7) is almost identical to Equation (10.6). R_B does cause some interaction between the loop gain and the transimpedance, but because the interaction is secondary, the CFA gain falls off with a faster slope.

$$A\beta = \frac{Z}{1.1R_F} \tag{10.7}$$

The direct gain of a VFA starts falling off early, often at 10 Hz or 100 Hz, but the transimpedance of a CFA does not start falling off until much higher frequencies. The VFA is constrained by the gain/bandwidth limitation imposed by the closed loop gain being incorporated within the loop gain. The CFA, with the exception of the effects of R_B, does not have this constraint. This adds up to the CFA being the superior high frequency amplifier.

10.4 Stability

Stability in a feedback system is defined by the loop gain, and no other factor, including the inputs or type of inputs, affects stability. The loop gain for a VFA is given in Equation (10.2). Examining Equation (10.2), we see that the stability of a VFA depends on two items, the op amp transfer function, a, and the gain setting components, Z_F/Z_G.

The op amp contains many poles, and if it is not internally compensated, it requires external compensation. The op amp always has at least one dominant pole, and the most phase margin that an op amp has is 45°. Phase margins beyond 60° are a waste of op amp bandwidth. When poles and zeros are contained in Z_F and Z_G, they can compensate for the op amp phase shift or add to its instability. In any case, the gain setting components always affect stability. When the closed loop gain is high, the loop gain is low; and low loop gain circuits are more stable than high loop gain circuits.

Wiring the op amp to a printed circuit board always introduces components formed from stray capacitance and inductance. Stray inductance becomes dominant at very high frequencies; hence in VFAs, it does not interfere with stability as much as it does with signal handling properties. Stray capacitance causes stability to increase or decrease, depending on its location. Stray capacitance from the input or output lead to ground induces instability, while the same stray capacitance in parallel with the feedback resistor increases stability.

The loop gain for a CFA with no input buffer output impedance, R_B, is given in Equation (10.6). Examining Equation (10.6), we see that the stability of a CFA depends on two items, the op amp transfer function, Z, and the gain setting component, Z_F. The op amp contains many poles, therefore they require external compensation. Fortunately, the external compensation for a CFA is done with Z_F. The factory applications engineer does extensive testing to determine the optimum value of R_F for a given gain. This value should be used in all applications at that gain,

but increased stability and less peaking can be obtained by increasing R_F. Essentially this sacrifices bandwidth for lower frequency performance, but in applications not requiring the full bandwidth, it is a wise trade-off.

The CFA stability is not constrained by the closed loop gain, so a stable operating point can be found for any gain, and the CFA is not limited by the gain/bandwidth constraint. If the optimum feedback resistor value is not given for a specific gain, one must test to find the optimum feedback resistor value.

Stray capacitance from any node to ground adversely affects the CFA performance. Stray capacitance of just a couple of picofarads from any node to ground causes 3 dB or more of peaking in the frequency response. Stray capacitance across the CFA feedback resistor, quite unlike that across the VFA feedback resistor, always causes some form of instability. CFAs are applied at very high frequencies, so the printed circuit board inductance associated with the trace length and pins adds another variable to the stability equation. Inductance cancels out capacitance at some frequency, but this usually seems to happen in an adverse manner. The wiring of VFAs is critical, but the wiring of CFAs is a science. Stay with the layout recommended by the manufacturer whenever possible.

10.5 Impedance

The input impedance of a VFA and CFA differ dramatically, because their circuit configurations are very different. The VFA input circuit is a long tailed pair, and this configuration gives the advantage that both input impedances match. Also, the input signal looks into an emitter/follower circuit that has high input impedance. The emitter/follower input impedance is $\beta(r_e + R_E)$, where R_E is a discrete emitter resistor. At low input currents, R_E is very high and the input impedance is very high. If a higher input impedance is required, the op amp uses a Darlington circuit that has an input impedance of $\beta^2(r_e + R_E)$.

So far, the implicit assumption is that the VFA is made with a bipolar semiconductor process. Applications requiring very high input impedances often use an FET process. Both BIFET and CMOS processes offer very high input impedance in any long tailed pair configuration. It is easy to get matched and high input impedances at the amplifier inputs. Do not confuse the matched input impedance at the op amp leads with the overall circuit input impedance. The input impedance looking into the inverting input

is R_G, and the impedance looking into the noninverting input is the input impedance of the op amp. While these are two different impedances, they are mismatched because of the circuit, not the op amp.

The CFA has a radically different input structure, which causes it to have mismatched input impedances. The noninverting input lead of the CFA is the input of a buffer that has very high input impedance. The inverting input lead is the output of a buffer that has very low impedance. There is no possibility that these two input impedances can be matched.

Again, because of the circuit, the inverting circuit input impedance is R_G. Once the circuit gain is fixed, the only way to increase R_G is to increase R_F. But, R_F is determined by a trade-off between stability and bandwidth. The circuit gain and bandwidth requirements fix R_F, hence there is no room to further adjust R_F to raise the resistance of R_G. If the manufacturer's data sheet says that $R_F = 100\ \Omega$ when the closed loop gain is 2, then $R_G = 100\ \Omega$ or $50\ \Omega$, depending on the circuit configuration. This sets the circuit input impedance at $100\ \Omega$. This analysis is not entirely accurate because R_B adds to the input impedance, but this addition is very small and depends on IC parameters. CFA op amp circuits are usually limited to noninverting voltage applications, but they serve very well in inverting applications that are current driven.

The CFA is limited to the bipolar process, because that process offers the highest speed. The option of changing process to BIFET or CMOS to gain increased input impedance is not attractive today. Although this seems like a limiting factor, it is not, because CFAs are often used in low impedance, where the inputs are terminated in 50 or $75\ \Omega$. Also, most very high speed applications require low impedances.

10.6 Equation Comparison

The pertinent VFA and CFA equations are repeated in Table 10.1. Note that the ideal closed loop gain equations for the inverting and noninverting circuits are identical. The ideal equations for the VFA depend on the op amp gain, a, being very large thus making $A\beta$ large compared to 1. The CFA needs two assumptions to be valid to obtain the ideal equations. First, the ideal equations for the CFA depend on the op amp transimpedance, Z, being very large, thus making $A\beta$ large compared to 1. Second, R_B must be very small compared to $Z_F \| Z_G$.

Table 10.1: Tabulation of Pertinent VFA and CFA Equations

Circuit configuration	Current feedback amplifier	Voltage feedback amplifier
Noninverting		
Forward or direct gain	$\dfrac{Z(1 + Z_F/Z_G)}{Z_F(1 + Z_B/Z_F\|\|Z_G)}$	a
Actual closed loop gain	$\dfrac{Z_F\left(1 + \dfrac{Z_B}{Z_G}\right)}{\dfrac{Z_F\left(1 + \dfrac{Z_B}{Z_F\|\|Z_G}\right)}{1 + \dfrac{Z}{Z_F\left[1 + \dfrac{\dfrac{Z_B}{1 + Z_B}}{Z_F\|Z_G}\right]}}}$	$\dfrac{a}{1 + \dfrac{aZ_G}{Z_F\|Z_G}}$
Closed loop gain	$1 + Z_F/Z_G$	$1 + Z_F/Z_G$
Inverting		
Forward or direct gain	$\dfrac{Z}{Z_G(1 + Z_B/Z_F\|\|Z_G)}$	$aZ_F/(Z_F + Z_G)$
Ideal loop gain	$Z/Z_F(1 + Z_B/Z_F\|\|Z_G)$	$aZ_F/(Z_F + Z_G)$
Actual closed loop gain	$\dfrac{-Z_G\left(1 + \dfrac{Z_B}{Z_F\|\|Z_G}\right)}{1 + \dfrac{Z}{Z_F\left(1 + \dfrac{Z_B}{Z_F\|\|Z_G}\right)}}$	$\dfrac{\dfrac{-aZ_F}{Z_F + Z_G}}{1 + \dfrac{aZ_G}{Z_F\|Z_G}}$
Closed loop gain	$-Z_F/Z_G$	$-Z_F/Z_G$

The ideal gain equations are identical, but the applications are very different, because the VFA is best applied to lower frequency, high precision jobs while the CFA applications are in the very high frequency realm. The transimpedance in a CFA acts much like the gain in a VFA. In each case, transimpedance or gain, it is the parameter that enables the use of feedback.

CHAPTER 11

Fully Differential Op Amps

11.1 Introduction

The term *fully differential op amp* probably brings chills to the spine of designers, with such thoughts as, "Oh no—now I have to learn something new." What most designers don't realize is that, over 50 years ago, op amps began as fully differential components. Techniques about how to use the fully differential versions have been almost lost over the decades. Today's fully differential op amps offer performance advantages unheard of in those first units.

This chapter presents just the facts a designer needs to get started and some resources for further design assistance. We hope, after reading this chapter, a designer can approach a fully differential op amp design with confidence and excitement.

11.2 What Does *Fully Differential* Mean?

Designers should already be familiar with single ended op amps after reading the other chapters of this book. Briefly, single ended op amps (Figure 11.1) have two inputs, a positive input and negative input, which are understood to be fully differential. They have a single output, which is referenced to system ground.

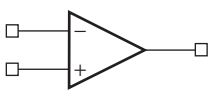


Figure 11.1: Single ended op amp schematic symbol.

The op amp also has two power supply inputs, which are connected to bipolar power supplies (equal and opposite positive and negative potentials), or a single potential, with a positive supply and a ground connected to the power supply pins. These power supply pins are often omitted from the schematic symbol, when power supply connections are implied elsewhere on the schematic. Fully differential op amps add a second output, see Figure 11.2.

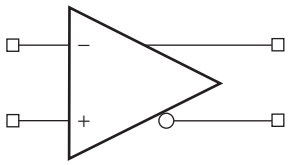


Figure 11.2: Fully differential op amp schematic symbol.

The second output is fully differential, the two outputs are called *positive output* and *negative output*, similar terminology to the two inputs. Like the inputs, they are differential. The output voltages are equal but opposite in polarity (referenced to the common mode operating point of the circuit).

11.3 How Is the Second Output Used?

An op amp is used as a closed loop device. Most designers know how to close the loop on a single ended op amp (see Figure 11.3).

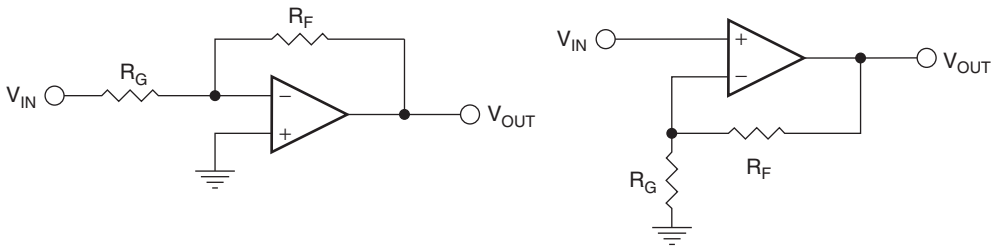


Figure 11.3: Closing the loop on a single ended op amp.

Whether the single ended op amp is used in an inverting or a noninverting mode, the loop is closed from the output to the inverting input.

11.4 Differential Gain Stages

So, how is the loop closed on a fully differential op amp? It stands to reason, if there are two outputs, both have to be operated in closed loop form. Therefore, the equivalent way of closing the loop on a fully differential op amp is as shown in Figure 11.4.

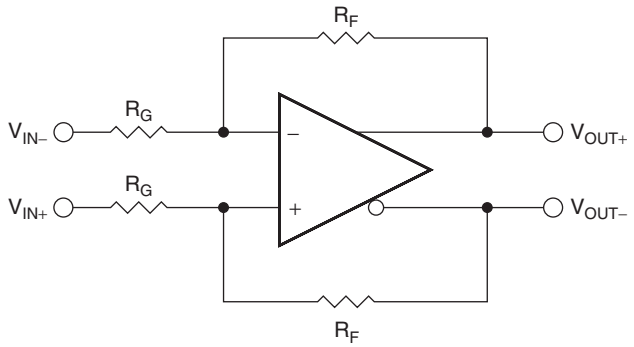


Figure 11.4: Closing the loop on a fully differential op amp.

Two identical feedback loops are required to close the loops for a fully differential op amp. If the loops are not matched, there can be significant second order harmonic distortion, but in some special cases, the output pathways can be different, and one such case is discussed later in this chapter.

Note that, for a fully differential op amp, each feedback loop is an inverting feedback loop. Both polarities of output are available, so terms like *inverting* and *noninverting* are meaningless. Instead, think of the single ended schematics in Figure 11.3. In both cases, the loop goes from the (noninverting) output to the inverting input, introducing a 180° phase shift. For the fully differential op amp, the top feedback loop has a 180° phase shift from the noninverting output to the inverting input, and the bottom feedback loop has a 180° phase shift from the inverting output to the noninverting input. Both feedback paths are therefore inverting. There is no "noninverting" fully differential op amp gain circuit.

The gain of the differential stage is

$$\frac{V_O}{V_I} = \frac{R_F}{R_G} \tag{11.1}$$

11.5 Single Ended to Differential Conversion

The schematic shown in Figure 11.4 is a fully differential gain circuit. Fully differential applications, however, are somewhat limited. Very often, the fully differential op amp is used to convert a single ended signal to a differential signal (Figure 11.5), perhaps to connect to the differential input of an analog to digital converter.

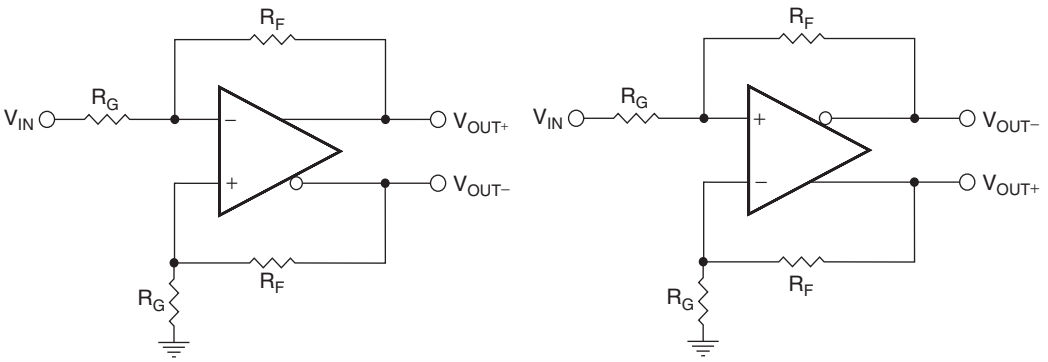


Figure 11.5: Single ended to differential conversion.

The two configurations shown in Figure 11.5 are equivalent. At first glance, they look identical, but they are not. The difference is that, in the left configuration, the inverting input is used for signal and the noninverting input for reference. In the right configuration, the noninverting input is used for signal and the inverting input for reference. They are functionally equivalent—either one will work.

The gain of the single ended to differential stage is

$$\frac{V_O}{V_I} = \frac{R_F}{R_G} \tag{11.2}$$

The only difference between this configuration and the previous is that one side of the input voltage is referenced to ground.

The dynamics of the gain are sometimes best described pictorially. Figure 11.6 shows the relationship among V_{IN}, V_{OUT+}, and V_{OUT-} when $R_F = R_G$.

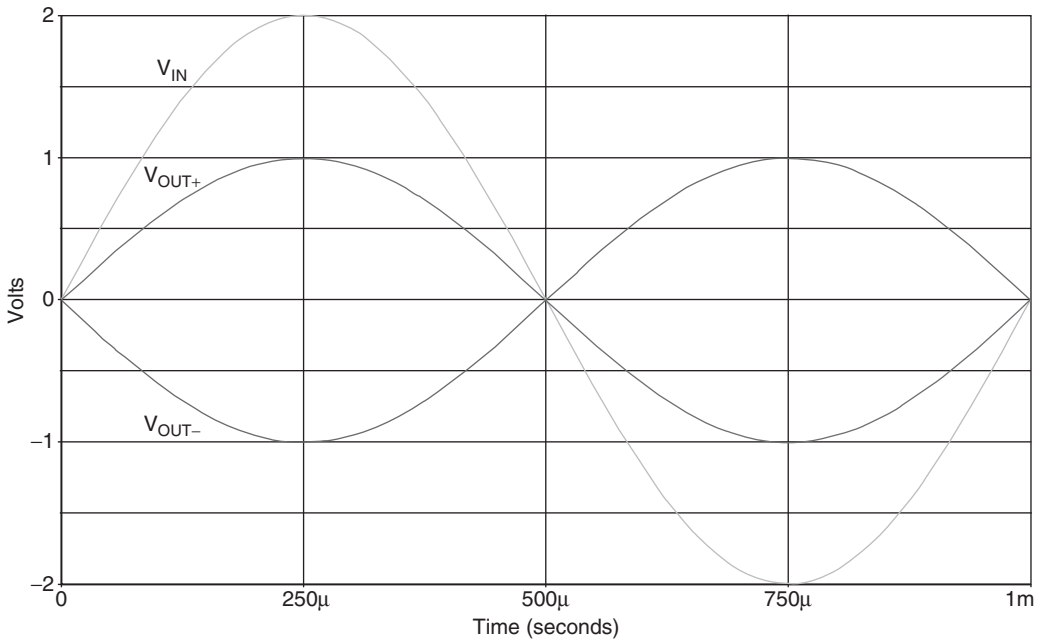


Figure 11.6: Relationship among V_{IN}, V_{OUT+}, and V_{OUT-}.

What is going on here? The amplitude of the input, V_{IN}, is twice that of the output? The gain is correct, however, because the value of the differential gain, $(V_{OUT+}) - (V_{OUT-})$, at any point in Figure 11.6 is equal to the amplitude of V_{IN}.

11.6 Working with Terminated Inputs

The design becomes more complicated if a single ended input signal must be terminated. This upsets the balance of the loop and changes the impedance. The design technique is anything but simple. Two equations in two variables interact, making design an interactive process. To simplify this difficult task for designers, Texas Instruments provides an online calculator on its Web site. This tool can be accessed

through the Analog and Mixed-Signal Knowledgebase, by typing "fully differential component calculator" in the search text box.

The fully differential component calculator has six panes. Data entry is made primarily in the upper left pane, although the bottom middle pane contains some secondary entry fields.

The top middle pane contains the schematic for a terminated single ended to fully differential conversion. Design equations are shown in the upper right pane. The astute designer will see that the equations for $R_{R3,R4}$ and R_t are interrelated through the A parameter. The tool makes a preliminary calculation to get close to the correct values, then it refines the calculation and "goal seeks" to the final value. The execution time depends on the step size used in the goal seeking calculation, and therefore selecting E96 resistor values execute much faster than Exact values. The designer should be patient, because execution times of several seconds or longer are possible, especially if gain is changed radically when Exact values is selected. The designer selects the desired gain and the impedance of the signal source (default value of 50 Ω). The designer then has the option of selecting a seed value for either R3 or R4 (but not both). If the designer attempts to select both, only the last value entered is used for calculation.

Almost without exception, the designer should initially try to select the value of R4, because it is often specified on the data sheet. The designer should experiment with R3 only if the recommended value of R4 does not yield an acceptable design (the tool has internal limits set to resistor values that make sense for real designs).

When the designer selects Calculate Values, the tool calculates resistor values in the bottom left pane and circuits simulation results in the bottom right pane. If the designer wishes, the power and input voltages can be changed in the bottom middle pane, and these affect the simulation results in the bottom right.

Note that this tool provides DC operating point only, it does not give AC simulation. Nevertheless, it saves the designer a lot of grief trying to do it using the "brute force" method.

11.7 A New Function

Texas Instruments' fully differential op amps have an additional pin, V_{OCM}, which stands for "voltage output common mode (level)." The function of this pin can be either an input or an output, because its source is just a voltage divider off of the power supply—but it is seldom used as an output. When it is used as an output, it corresponds to the common mode voltage about which the V_{OUT+} and V_{OUT-} outputs swing.

11.8 Conceptualizing the V_{OCM} Input

Figures 11.7 and 11.8 show electrical and mechanical models of V_{OCM}, respectively.

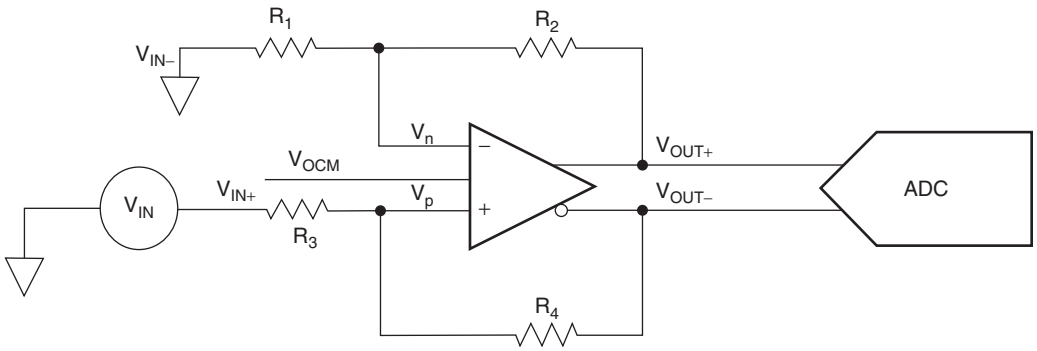


Figure 11.7: Electrical model of V_{OCM}.

In the mechanical model, which is a more complex version of a child's teeter-totter, physically raising the V_{IN-} arm (with a length of R_1), causes the arm to pivot on fulcrum V_n, and the other side of the arm, V_{OUT+}, to rise proportionally to the length of the arm (R_2). A second fulcrum (V_{OCM}), between the two arms, forces the end of the other arm (V_{OUT-}) to go down by the same amount. The second arm also has a fulcrum at V_p, which causes its other side (V_{IN+}) to move the same amount as V_{IN-} but in the other direction (assuming lengths $R_1 = R_3$, and $R_2 = R_4$). V_{OCM} can be used to raise and

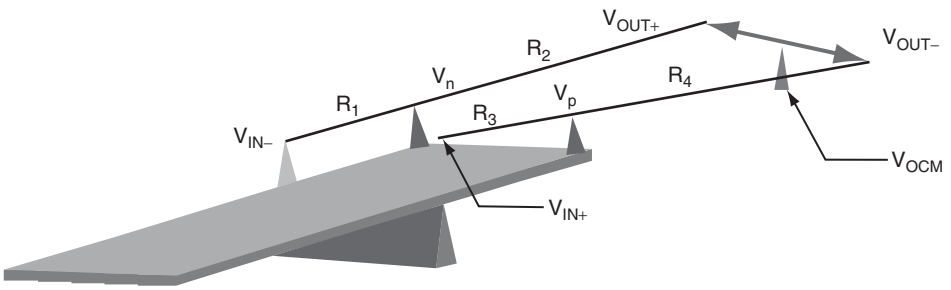


Figure 11.8: Mechanical model of V_{OCM}.

lower the average height (offset) of both V_{OUT+} and V_{OUT-} equally. But, be careful! It can also exceed the mechanical limits of the model. Too low and the V_{OUT+} and V_{OUT-} ends of the arms hit "ground." Too high and the V_{IN-} and V_{IN+} ends of the arms both hit "ground." The base of the teeter-totter and its fulcrum represent the "potential" for movement or power supply.

We actually implemented this teeter-totter model with a well known set of child's building blocks, complete with a motor for excitation (Figure 11.9). The reader who has a set of these toys might consider building the model for some enjoyment,

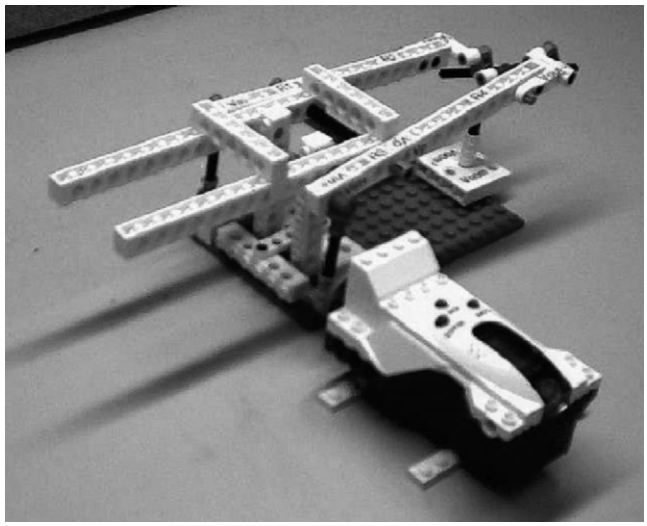


Figure 11.9: A mechanical fully differential amplifier.

education, and a way to introduce children to the concepts of differential transmission.

The most common use of the V_{OCM} pin is to set the output common mode level of the fully differential op amp (Figure 11.10). This is a very useful function, because it can be used to match the common mode point of a data converter to which the fully differential amplifier is connected. High precision, high speed data converters often employ differential inputs and provide a reference output.

The schematic of Figure 11.10 is simplified and does not show compensation, termination, or decoupling components for clarity. Nevertheless, it shows the basic concept. This is an important type of interface and is elaborated on further in a later chapter.

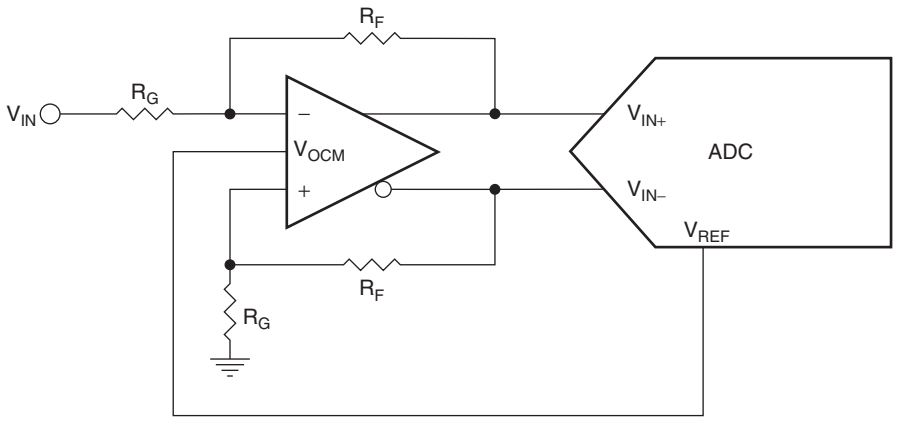


Figure 11.10: Using a fully differential op amp to drive an ADC.

The remainder of this chapter presents the designer with a basic set of applications based on fully differential applications.

11.9 Instrumentation

An instrumentation amplifier can be constructed from two single ended amplifiers and a fully differential amplifier, as shown in Figure 11.11. Both polarities of the output signal are available, of course, and there is no ground dependence.

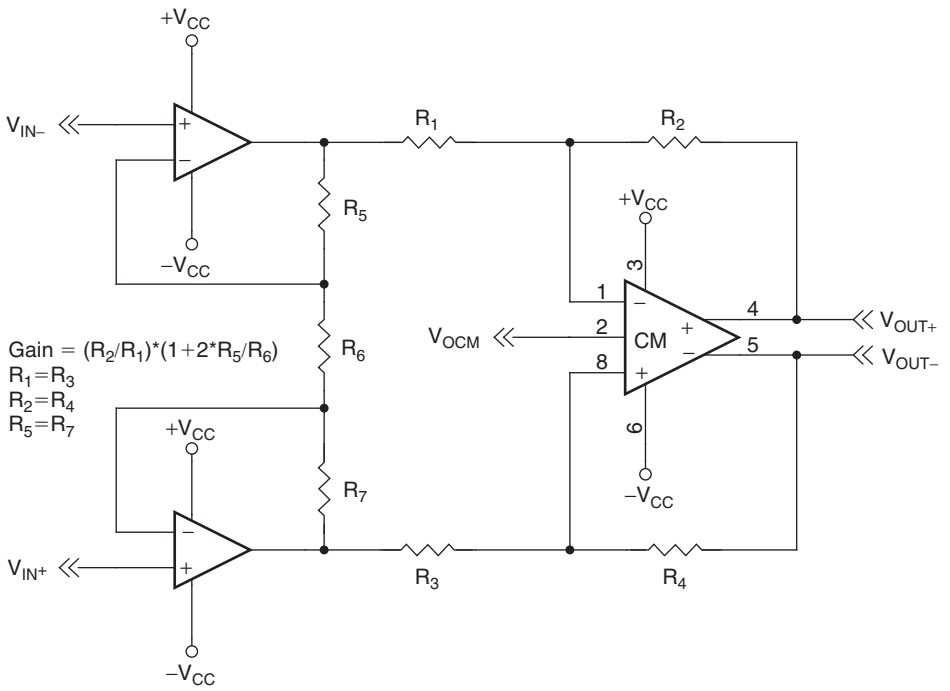


Figure 11.11: Instrumentation amplifier.

11.10 Filter Circuits

Filtering is done to eliminate unwanted content in audio, among other things. Differential filters that do the same job to differential signals as their single ended cousins do to single ended signals can be applied.

For differential filter implementations, the components are simply mirror imaged for each feedback loop. The components in the top feedback loop are designated *A*, and those in the bottom feedback loop are designated *B*.

For clarity, decoupling components are not shown in the following schematics. Proper operation of high speed op amps requires proper decoupling techniques. That does not mean the shotgun approach of using inexpensive 0.1 μF capacitors. Decoupling component selection should be based on the frequencies that need to be rejected and the characteristics of the capacitors used at those frequencies.

11.10.1 Single Pole Filters

Single pole filters are the simplest filters to implement with single ended op amps, and the same holds true with fully differential amplifiers.

A low pass filter can be formed by placing a capacitor in the feedback loop of a gain stage, in a manner similar to single ended op amps (see Figure 11.12).

A high pass filter can be formed by placing a capacitor in series with an inverting gain stage as shown in Figure 11.13.

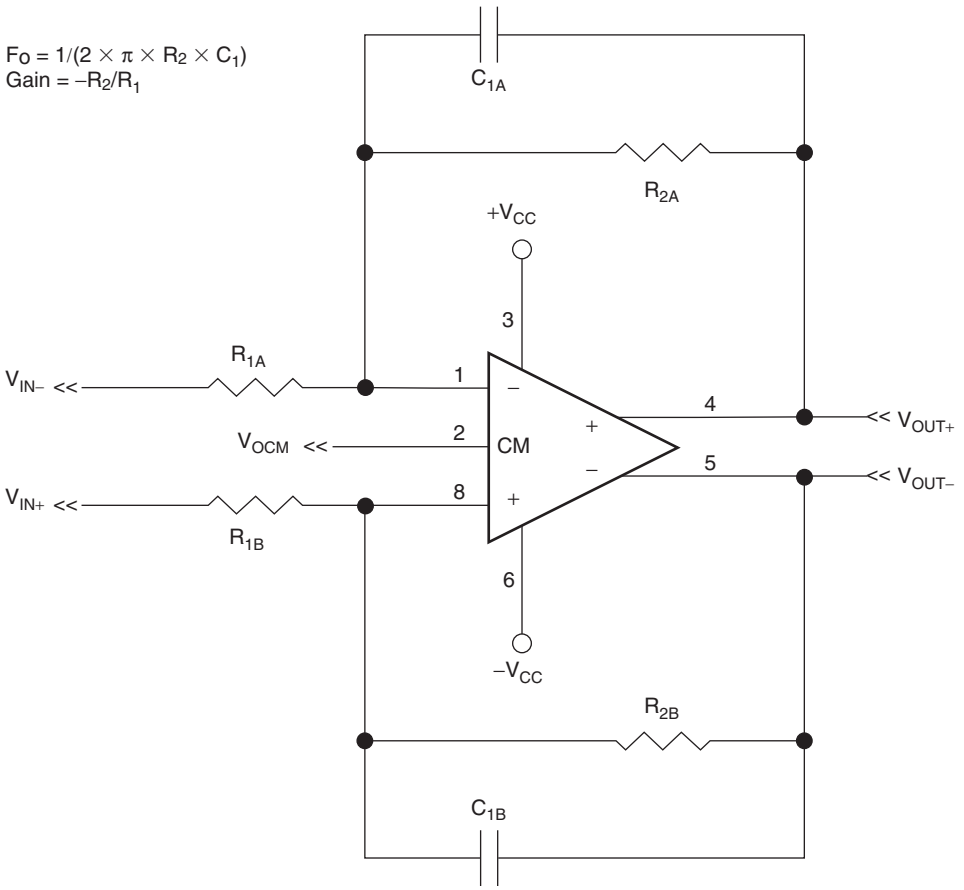


Figure 11.12: Single pole differential low pass filter.

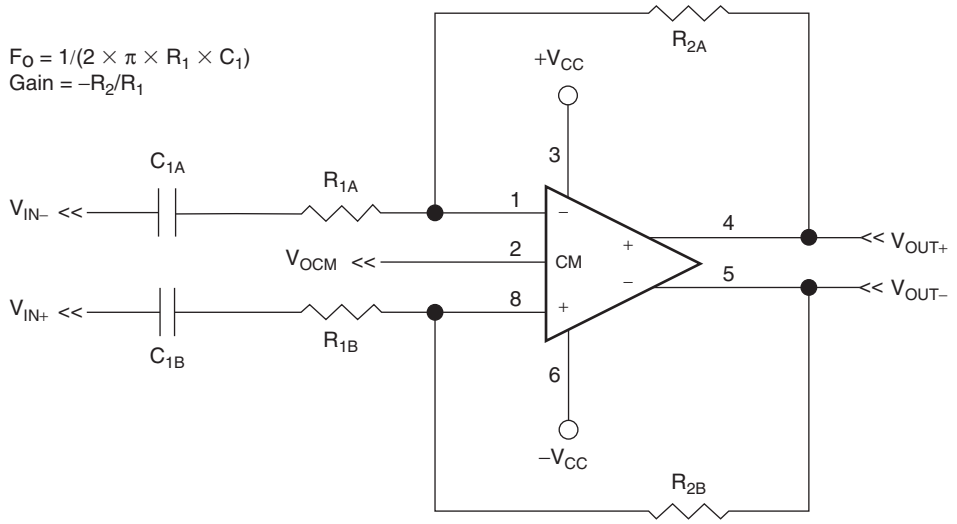


Figure 11.13: Single pole differential high pass filter.

11.10.2 Double Pole Filters

Many double pole filter topologies incorporate positive and negative feedback and therefore have no differential implementation. Others employ only negative feedback but use the noninverting input for signal input and also have no differential implementation. This limits the number of options for designers, because both feedback paths must return to an input.

The good news, however, is that topologies are available to form differential low pass, high pass, bandpass, and notch filters. However, the designer might have to use an unfamiliar topology or more op amps than would have been required for a single ended circuit.

11.10.3 Multiple Feedback Filters

Multiple feedback (MFB) filter topology is the simplest topology that supports fully differential filters (Figures 11.14 and 11.15). Unfortunately, the MFB topology is a bit hard to work with, but component ratios are shown for common unity gain filters.

There is no reason why the feedback paths have to be identical. A bandpass filter can be formed by using nonsymmetrical feedback pathways (one low pass and one high pass). Figure 11.16 shows a bandpass filter that passes the range of human speech (300 Hz to 3 kHz). Figure 11.17 shows the response.

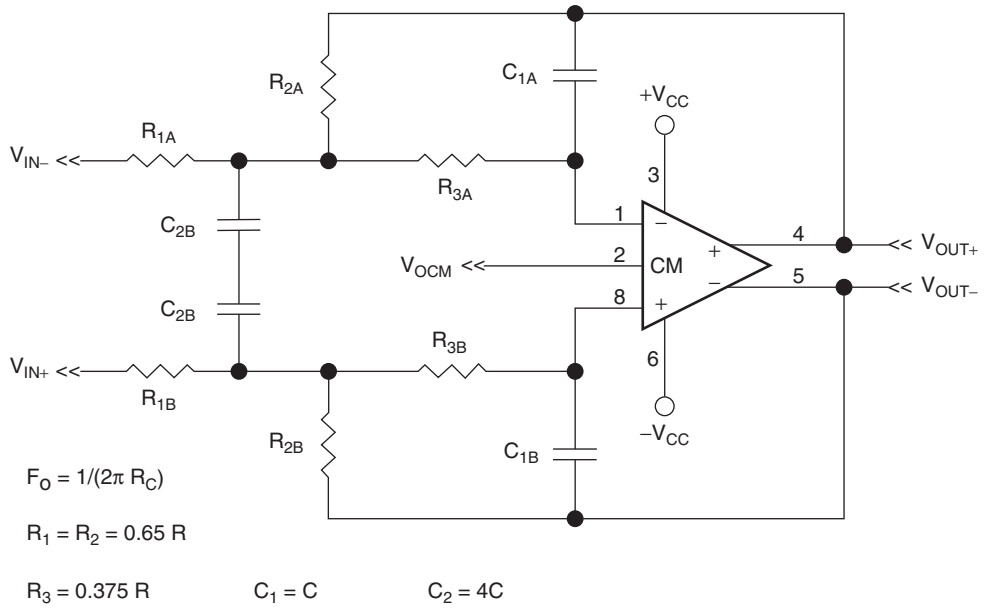


Figure 11.14: Differential low pass filter.

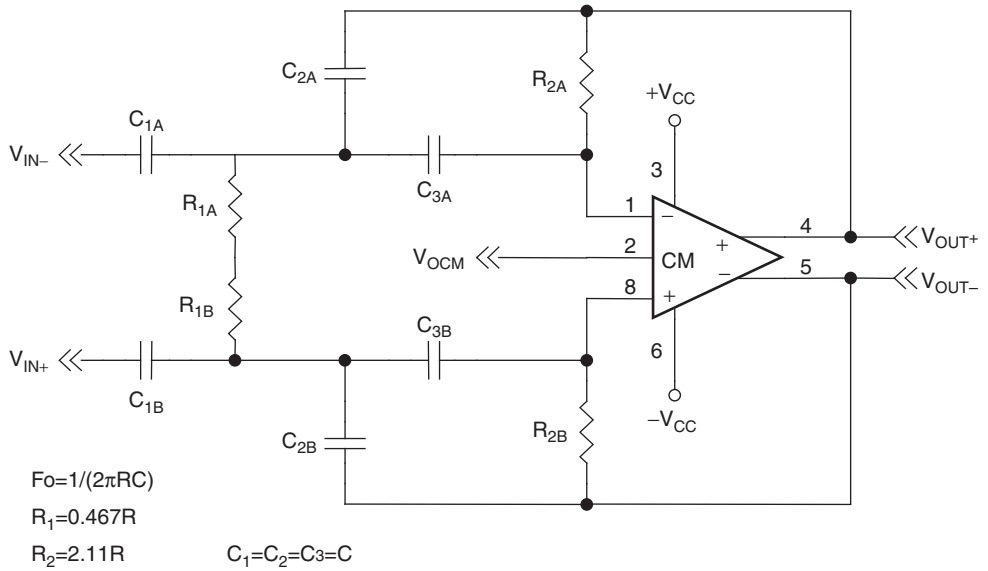


Figure 11.15: Differential high pass filter.

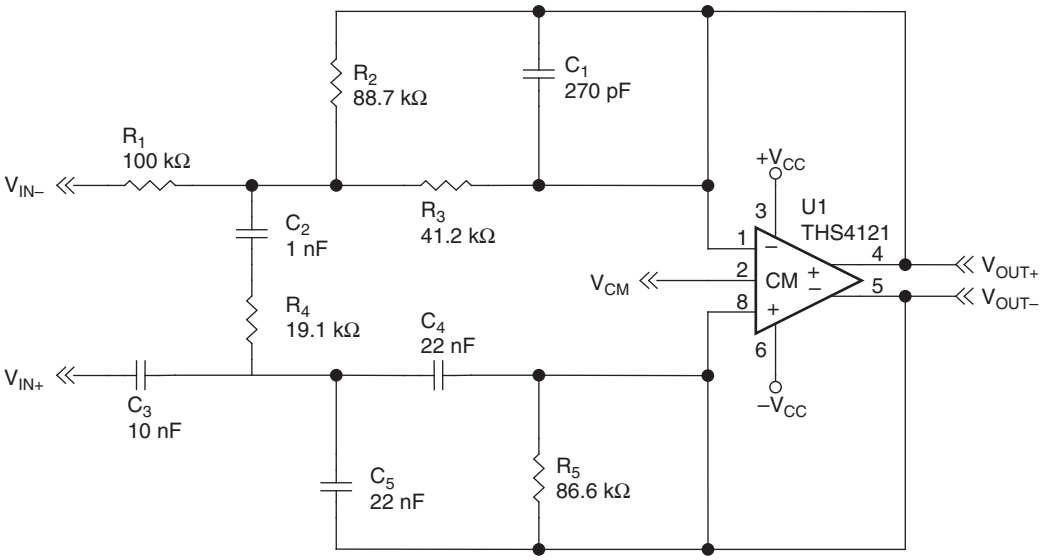


Figure 11.16: Differential speech filter.

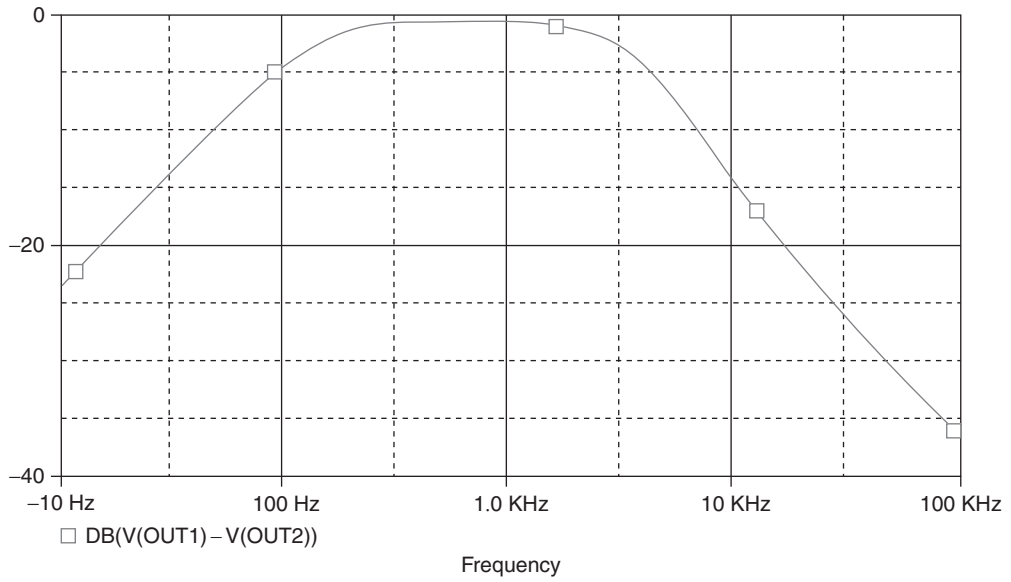


Figure 11.17: Differential speech filter response.

11.10.4 Biquad Filter

Biquad filter topology (Figure 11.18) is a double pole topology available in low pass, high pass, bandpass, and notch. The single ended implementation of this filter topology has three op amps, with the third op amp included only to invert the output of the previous op amp. That inversion is inherent in the fully differential op amp and therefore eliminates the third op amp, reducing the total number of op amps required to two.

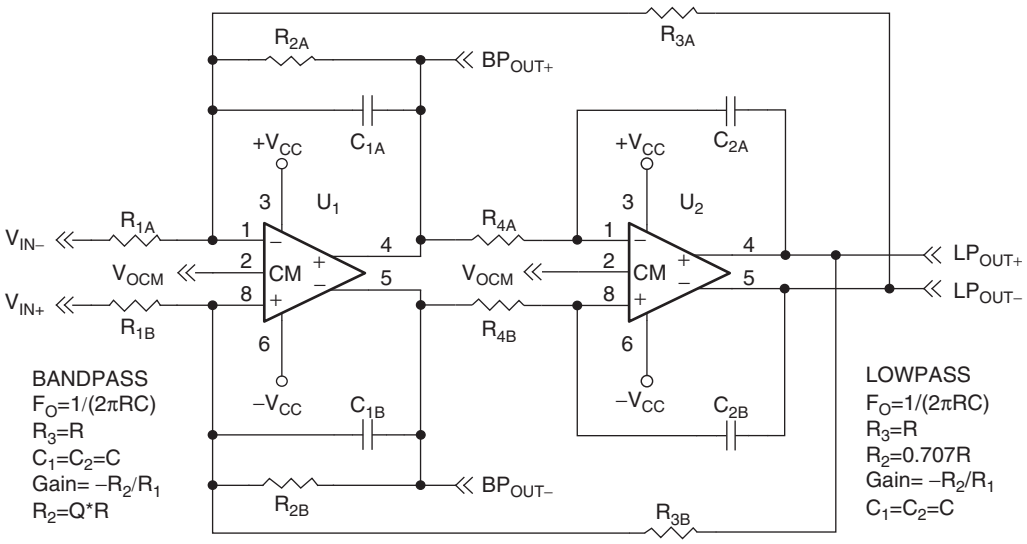


Figure 11.18: Differential biquad filter.

The high pass and notch versions of this particular biquad configuration require additional op amps, and therefore this topology is not optimum for them. Other topologies, however, can generate all four functions and can also be implemented with only two fully differential op amps.

CHAPTER 12

Op Amp Noise Theory and Applications

Bruce Carter

12.1 Introduction

The purpose of op amp circuitry is the manipulation of the input signal in some fashion. Unfortunately, in the real world, the input signal has unwanted noise superimposed on it.

Noise is not something most designers get excited about. In fact, they probably wish the whole topic would go away. It can, however, be a fascinating study by itself. A good understanding of the underlying principles can, in some cases, be used to reduce noise in the design.

12.2 Characterization

Noise is a purely random signal, the instantaneous value or phase of the waveform cannot be predicted at any time. Noise can either be generated internally in the op amp or from its associated passive components or superimposed on the circuit by external sources. External noise is covered in another chapter and is usually the dominant effect.

12.2.1 rms versus P-P Noise

Instantaneous noise voltage amplitudes are as likely to be positive as negative. When plotted, they form a random pattern centered on zero. Since noise sources have

amplitudes that vary randomly with time, they can be specified only by a probability density function. The most common probability density function is Gaussian. In a Gaussian probability function, there is a mean value of amplitude, which is most likely to occur. The probability that a noise amplitude will be higher or lower than the mean falls off in a bell shaped curve, which is symmetrical around the center (Figure 12.1).

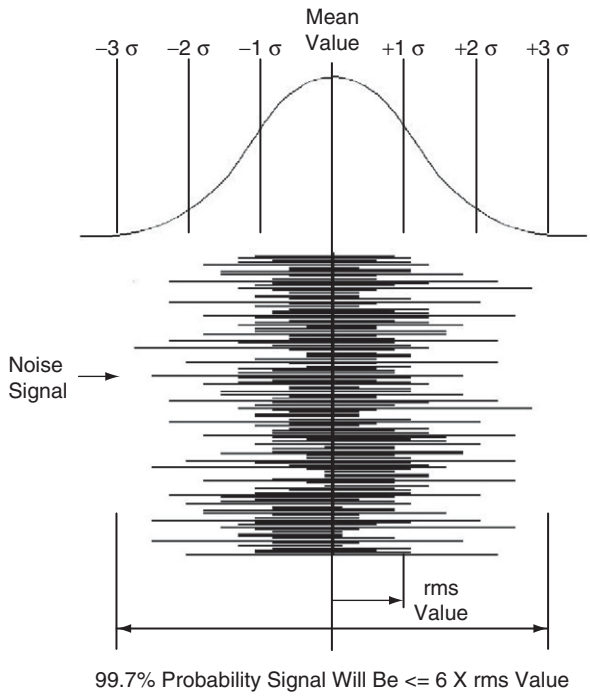


Figure 12.1: Gaussian distribution of noise energy.

The term σ is the standard deviation of the Gaussian distribution and the rms (root mean square) value of the noise voltage and current. The instantaneous noise amplitude is within ±1σ 68% of the time. Theoretically, the instantaneous noise amplitude can have values approaching infinity. However, the probability falls off rapidly as amplitude increases. The instantaneous noise amplitude is within ±3σ of the mean 99.7% of the time. If more or less assurance is desired, it is between ±2σ 95.4% of the time and ±3.4σ 99.94% of the time.

The term σ^2 is the average mean square variation about the average value. This also means that the average mean square variation about the average value, $\overline{i^2}$ or $\overline{e^2}$, is the same as the variance σ^2.

Thermal noise and shot noise (see later) have Gaussian probability density functions. The other forms of noise do not.

12.2.2 Noise Floor

When all input sources are turned off and the output is properly terminated, a level of noise, called the *noise floor*, determines the smallest signal for which the circuit is useful. The objective for the designer is to place the signals that the circuit processes above the noise floor but below the level where the signals clip.

12.2.3 Signal to Noise Ratio

The noisiness of a signal is defined as

$$\frac{S_{(f)}}{N_{(f)}} = \frac{\text{rms signal voltage}}{\text{rms noise voltage}} \tag{12.1}$$

In other words, it is a ratio of signal voltage to noise voltage (hence the name *signal to noise ratio*).

12.2.4 Multiple Noise Sources

When there are multiple noise sources in a circuit, the total rms noise signal that results is the square root of the sum of the average mean square values of the individual sources:

$$E_{\text{TOTALrms}} = \sqrt{e_{1\text{rms}}^2 + e_{2\text{rms}}^2 + \ldots + e_{n\text{rms}}^2} \tag{12.2}$$

Put another way, this is the only "break" the designer gets when dealing with noise. If the circuit contains two noise sources of equal amplitude, the total noise is not doubled (increased by 6 dB). It increases by only 3 dB. Consider a very simple case, two noise sources with amplitudes of 2 V_{rms}:

$$E_{\text{TOTALrms}} = \sqrt{2^2 + 2^2} = \sqrt{8} = 2.83\ V_{\text{rms}} \tag{12.3}$$

Therefore, with two equal sources of noise in a circuit, the noise is $20 \times \log(2.83/2) = 3.01$ dB higher than if there were only one source of noise—instead of double (6 dB) as would be intuitively expected.

This relationship means that the worst noise source in the system tends to dominate the total noise. Consider a system in which one noise source is 10 V_{rms} and another is 1 V_{rms}:

$$E_{\text{TOTALrms}} = \sqrt{10^2 + 1^2} = \sqrt{108} = 10.05\ V_{\text{rms}} \tag{12.4}$$

There is hardly any effect from the 1 V noise source!

12.2.5 Noise Units

Noise is normally specified as a spectral density in rms volts or amps per root hertz, $\text{V}/\sqrt{\text{Hz}}$ or $\text{A}/\sqrt{\text{Hz}}$. These are not very "user friendly" units. A frequency range is needed to relate these units to the actual noise levels that will be observed.

For example,

- A TLE2027 op amp with a noise specification of 2.5 $\text{nV}/\sqrt{\text{Hz}}$ is used over an audio frequency range of 20 Hz to 20 kHz, with a gain of 40 dB. The output voltage is 0 dBV (1 V).
- To begin with, calculate the *root hertz* part: $\sqrt{20,000 - 20} = 141.35$.
- Multiply this by the noise spec, $2.5 \times 141.35 = 353.38$ nV, which is the equivalent input noise (EIN). The output noise equals the input noise multiplied by the gain, which is 100 (40 dB).

The signal to noise ratio can be now be calculated:

$$353.38\ \text{nV} \times 100 = 35.3\ \mu\text{V} \tag{12.5}$$

$$\text{Signal to noise (dB)} = 20 \times \log(1\ \text{V} \div 35.3\ \mu\text{V}) = 20 \times \log(28329) = 89\ \text{dB}$$

The TLE2027 op amp is an excellent choice for this application. Remember, though, that passive components and external noise sources can degrade performance.

There is also a slight increase in noise at low frequencies, due to the 1/*f* effect (see later).

12.3 Types of Noise

Five types of noise are in op amps and their associated circuitry:

1. Shot noise
2. Thermal noise
3. Flicker noise
4. Burst noise
5. Avalanche noise

Some or all of these noises may be present in a design, presenting a noise spectrum unique to the system. It is not possible in most cases to separate the effects, but knowing general causes may help the designer optimize the design, minimizing noise in a particular bandwidth of interest. Proper design for low noise may involve a "balancing act" between these sources of noise and external noise sources.

12.3.1 Shot Noise

The name *shot noise* is short for Schottky noise, sometimes referred to as *quantum noise*. It is caused by random fluctuations in the motion of charge carriers in a conductor. Put another way, current flow is not a continuous effect. Current flow is electrons, charged particles that move in accordance with an applied potential. When the electrons encounter a barrier, potential energy builds until they have enough energy to cross that barrier. When they have enough potential energy, it is abruptly transformed into kinetic energy as they cross the barrier. A good analogy is stress in an earthquake fault that is suddenly released as an earthquake.

As each electron randomly crosses a potential barrier, such as a pn junction in a semiconductor, energy is stored and released as the electron encounters and then shoots across the barrier. Each electron contributes a little *pop* as its stored energy is released when it crosses the barrier (Figure 12.2).

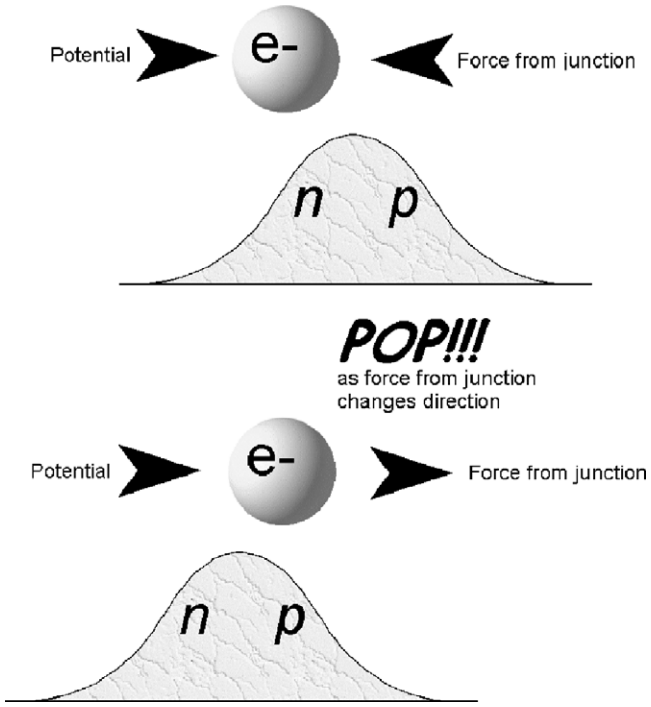


Figure 12.2: Shot noise generation.

The aggregate effect of all of the electrons shooting across the barrier is the shot noise. Amplified shot noise has been described as sounding like lead shot hitting a concrete wall.

Some characteristics of shot noise are these:

- Shot noise is always associated with current flow. It stops when the current flow stops.
- Shot noise is independent of temperature.
- Shot noise is spectrally flat or has a uniform power density, meaning that when plotted versus frequency it has a constant value.
- Shot noise is present in any conductor—not just a semiconductor. Barriers in conductors can be as simple as imperfections or impurities in the metal. The

level of shot noise, however, is very small due to the enormous numbers of electrons moving in the conductor and the relative size of the potential barriers. Shot noise in semiconductors is much more pronounced.

The rms shot noise current is equal to

$$I_{SH} = \sqrt{(2qI_{DC} + 4qI_O)B} \tag{12.6}$$

where

q = Electron charge (1.6×12^{-19} coulombs).

I_{DC} = Average forward DC current in amps.

I_Q = Reverse saturation current in amps.

B = Bandwidth in hertz.

If the pn junction is forward biased, I_O is zero, and the second term disappears. Using Ohm's law and the dynamic resistance of a junction,

$$r_d = \frac{kT}{qI_{DC}} \tag{12.7}$$

The rms shot noise voltage is equal to

$$E_{SH} = kT\sqrt{\frac{2B}{qI_{DC}}} \tag{12.8}$$

where

k = Boltzmann's constant (1.38×10^{-23} joules/K).

q = Electron charge (1.6×12^{-19} coulombs).

T = Temperature in Kelvins.

I_{DC} = Average DC current in amps.

B = Bandwidth in hertz.

For example, a junction carries a current of 1 mA at room temperature. Its noise over the audio bandwidth is

$$E_{SH} = 1.38 \times 10^{-23} \times 298 \sqrt{\frac{2(20{,}000 - 20)}{\left(1.6 \times 10^{-19}\right) \times \left(1 \times 10^{-3}\right)}} = 65 \text{ nV} = -144 \text{ dBV} \tag{12.9}$$

Obviously, it is not much of a problem in this example.

Look closely at the formula for shot noise voltage. Note that the shot noise voltage is inversely proportional to the current. Stated another way, shot noise voltage decreases as average DC current increases and increases as average DC current decreases. This can be an elegant way of determining if shot noise is a dominant effect in the op amp circuit being designed. If possible, decrease the average DC current by a factor of 100 and see if the overall noise increases by a factor of 10. In the preceding example,

$$E_{SH} = 1.38 \times 10^{-23} \times 298 \sqrt{\frac{2(20{,}000 - 20)}{\left(1.6 \times 10^{-19}\right) \times \left(1 \times 10^{-5}\right)}} = 650 \text{ nV} = -124 \text{ dBV} \tag{12.10}$$

The shot noise voltage does increase by a factor of 10, or 20 dB.

12.3.2 Thermal Noise

Thermal noise is sometimes referred to as *Johnson noise*, after its discoverer. It is generated by thermal agitation of electrons in a conductor. Simply put, as a conductor is heated, it becomes noisy. Electrons are never at rest; they are always in motion. Heat disrupts the electrons' response to an applied potential. It adds a random component to their motion (Figure 12.3). Thermal noise stops only at absolute zero.

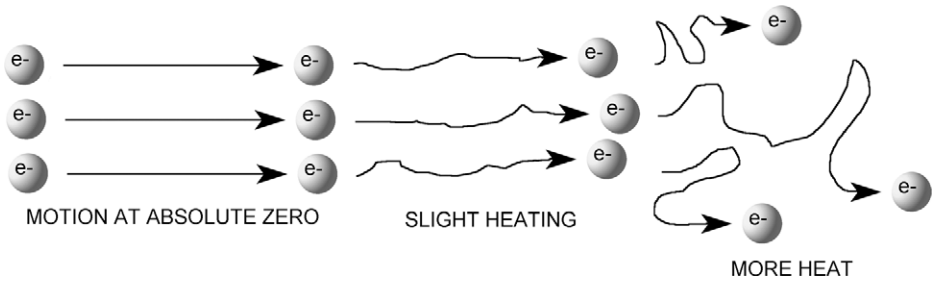


Figure 12.3: Thermal noise.

Like shot noise, thermal noise is spectrally flat or has a uniform power density (it is *white*), but thermal noise is independent of current flow.

At frequencies below 100 MHz, thermal noise can be calculated using Nyquist's relation:

$$E_{TH} = \sqrt{4kTRB} \tag{12.11}$$

or

$$I_{TH} = \sqrt{\frac{4kTB}{R}} \tag{12.12}$$

where

E_{TH} = Thermal noise voltage in volts rms.

I_{TH} = Thermal noise current in amps rms.

k = Boltzmann's constant (1.38×10^{-23}).

T = Absolute temperature (in Kelvins).

R = Resistance in ohms.

B = Noise bandwidth in hertz ($f_{MAX} - f_{MIN}$).

The noise from a resistor is proportional to its resistance and temperature. It is important not to operate resistors at elevated temperatures in high gain input stages. Lowering resistance values also reduces thermal noise.

For example, the noise in a 100 kΩ resistor at 25°C (298 K) over the audio frequency range of 20 Hz to 20 kHz is

$$\begin{aligned} E_{\mathrm{TH}} &= \sqrt{4kTRB} \\ &= \sqrt{4 \times \left(1.38 \times 10^{-23}\right) \times 298 \times 100{,}000 \times (20{,}000 - 20)} \\ &= 5.73\ \mu\mathrm{V} \\ &= -104.8\ \mathrm{dBV} \end{aligned} \tag{12.13}$$

Decreasing the temperature would reduce the noise slightly, but scaling the resistor down to 1 kΩ (a factor of 100) would reduce the thermal noise by 20 dB. Similarly, increasing the resistor to 10 MΩ would increase the thermal noise to –84.8 dBV, a level that would affect a 16 bit audio circuit. The noise from multiple resistors adds according to the root mean square law in Section 12.2.4. Beware of large resistors used as the input resistor of an op amp gain circuit, their thermal noise is amplified by the gain in the circuit (Section 12.4). Thermal noise in resistors is often a problem in portable equipment, where resistors have been scaled up to get power consumption down.

12.3.3 Flicker Noise

Flicker noise is also called *1/f noise*. Its origin is one of the oldest unsolved problems in physics. It is pervasive in nature and in many human endeavors. It is present in all active and many passive devices. It may be related to imperfections in crystalline structure of semiconductors, as better processing can reduce it.

Some characteristics of flicker noise are these:

- It increases as the frequency decreases, hence the name *1/f*.
- It is associated with a DC current in electronic devices.
- It has the same power content in each octave (or decade).

$$E_n = K_v \sqrt{\left(\ln \frac{f_{\mathrm{MAX}}}{f_{\mathrm{MIN}}}\right)}, \quad I_n = K_i \sqrt{\left(\ln \frac{f_{\mathrm{MAX}}}{f_{\mathrm{MIN}}}\right)} \tag{12.14}$$

where

K_e and K_i are proportionality constants (volts or amps) representing E_n and I_n at 1 Hz.

f_{MAX} and f_{MIN} are the minimum and maximum frequencies in hertz.

Flicker noise is found in carbon composition resistors, where it is often referred to as *excess noise*, because it appears in addition to the thermal noise that is there. Other types of resistors also exhibit flicker noise to varying degrees, with wire wound showing the least. Since flicker noise is proportional to the DC current in the device, if the current is kept low enough, thermal noise will predominate and the type of resistor used will not change the noise in the circuit.

Reducing power consumption in an op amp circuit by scaling up resistors may reduce the $1/f$ noise, at the expense of increased thermal noise.

12.3.4 Burst Noise

Burst noise, also called *popcorn noise*, is related to imperfections in semiconductor material and heavy ion implants. It is characterized by discrete high frequency pulses. The pulse rates may vary, but the amplitudes remain constant at several times the thermal noise amplitude. Burst noise makes a popping sound at rates below 100 Hz when played through a speaker—it sounds like popcorn popping, hence the name. Low burst noise is achieved by using clean device processing and therefore is beyond the control of the designer. Modern processing techniques at Texas Instruments have all but eliminated its occurrence.

12.3.5 Avalanche Noise

Avalanche noise is created when a pn junction is operated in the reverse breakdown mode. Under the influence of a strong reverse electric field within the junction's depletion region, electrons have enough kinetic energy that, when they collide with the atoms of the crystal lattice, additional electron/hole pairs are formed (Figure 12.4). These collisions are purely random and produce random current pulses similar to shot noise but much more intense.

When electrons and holes in the depletion region of a reversed biased junction acquire enough energy to cause the avalanche effect, a random series of large noise spikes is generated. The magnitude of the noise is difficult to predict due to its dependence on the materials.

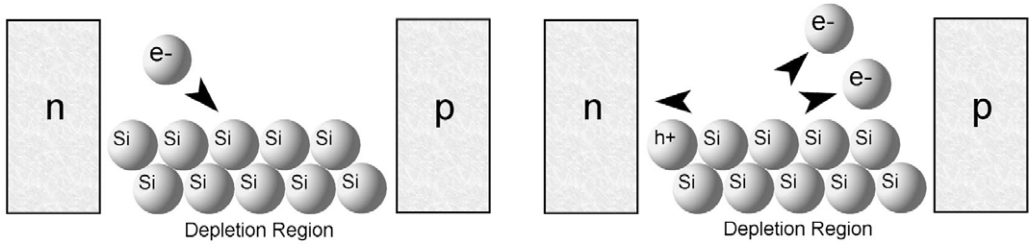


Figure 12.4: Avalanche noise.

Because the zener breakdown in a pn junction causes avalanche noise, it is an issue with op amp designs that include zener diodes. The best way of eliminating avalanche noise is to redesign a circuit to use no zener diodes.

12.4 Noise Colors

While the noise types are interesting, real op amp noise appears as the summation of some or all of them. The various noise types themselves are difficult to separate. Fortunately, there is an alternative way to describe noise, called *color*. The colors of noise come from rough analogies to light and refer to the frequency content. Many colors are used to describe noise, some of them having a relationship to the real world and some of them more attuned to the field of psychoacoustics.

White noise is in the middle of a *spectrum* that runs from purple to blue to white to pink and red/brown. These colors correspond to powers of the frequency to which their spectrum is proportional, as shown in Table 12.1.

Table 12.1: Noise Colors

Color	Frequency content
Purple	f^2
Blue	f
White	1
Pink	$1/f$
Red/brown	$1/f^2$

An infinite number of variations lie between the colors. All inverse powers of frequency are possible, as are noises that are narrowband or appear only at one discrete frequency. Those, however, are primarily external sources of noise, so their presence is an important clue that the noise is external, not internal. There are no pure colors; at high frequencies, all of them begin to roll off and become pinkish. The op amp noise sources just described appear in the region between white noise and red/brown noise (Figure 12.5).

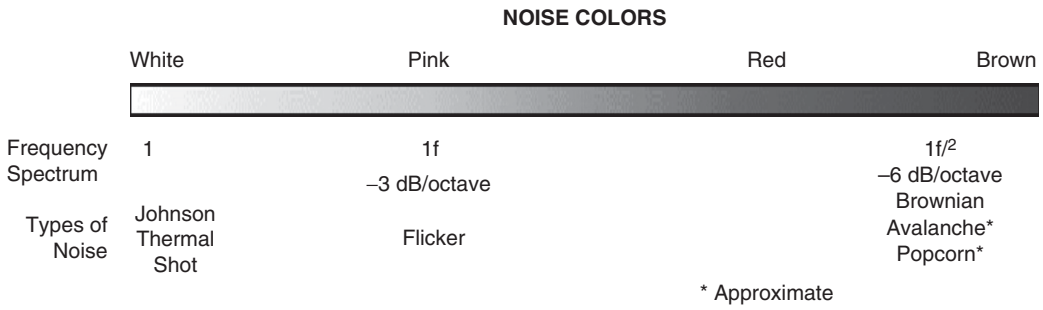


Figure 12.5: Noise colors.

12.4.1 White Noise

White noise is noise in which the frequency and power spectrum is constant and independent of frequency. The signal power for a constant bandwidth (centered at frequency f_O) does not change if f_O is varied. Its name comes from a similarity to white light, which has equal quantities of all colors.

When plotted versus frequency, white noise is a horizontal line of constant value.

Shot and thermal (Johnson) noise sources are approximately white, although there is no such thing as pure white noise. By definition, white noise would have infinite energy at infinite frequencies. White noise always becomes pinkish at high frequencies.

Steady rainfall or radio static on an unused channel approximate a white noise characteristic.

12.4.2 Pink Noise

Pink noise is noise with a $1/f$ frequency and power spectrum excluding DC. It has equal energy per octave (or decade for that matter). This means that the amplitude

decreases logarithmically with frequency. Pink noise is pervasive in nature—many supposedly random events show a $1/f$ characteristic.

Flicker noise displays a $1/f$ characteristic, which also means that it rolls off at 3 dB/octave.

12.4.3 Red/Brown Noise

Red noise is not universally accepted as a noise type. Many sources omit it and go straight to brown, attributing red characteristics to brown. This has more to do with aesthetics than anything else (if brown noise is the low end of the spectrum, then pink noise should be named *tan*). So if pink noise is pink, then the low end of the spectrum should be red. Red noise is named for a connection with red light, which is on the low end of the visible light spectrum. But then, this noise simulates Brownian motion, so perhaps it should be called *Brown*. Red/brown noise has a –6 dB/octave frequency response and a frequency spectrum of $1/f^2$ excluding DC.

Red/brown noise is found in nature. The acoustic characteristics of large bodies of water approximate red/brown noise frequency response.

Popcorn and avalanche noise approximate a red/brown characteristic, but they are more correctly defined as pink noise, where the frequency characteristic has been shifted down as far as possible in frequency.

12.5 Op Amp Noise

This section describes the noise in op amps and associated circuits.

12.5.1 The Noise Corner Frequency and Total Noise

Op amp noise is never specified as shot, thermal, or flicker, or even white or pink. Noise for audio op amps is specified with a graph of equivalent input noise versus frequency.

These graphs usually show two distinct regions:

- Lower frequencies where pink noise is the dominant effect.
- Higher frequencies where white noise is the dominant effect.

Actual measurements for the TLV2772 show that the noise has both white and pink characteristics (Figure 12.6). Therefore, the noise equations for each type of noise cannot approximate the total noise out of the TLV2772 over the entire range shown on the graph. It is necessary to break the noise into two parts—the pink part and the white part—then add those parts together to get the total op amp noise using the root mean square law of Section 12.2.4.

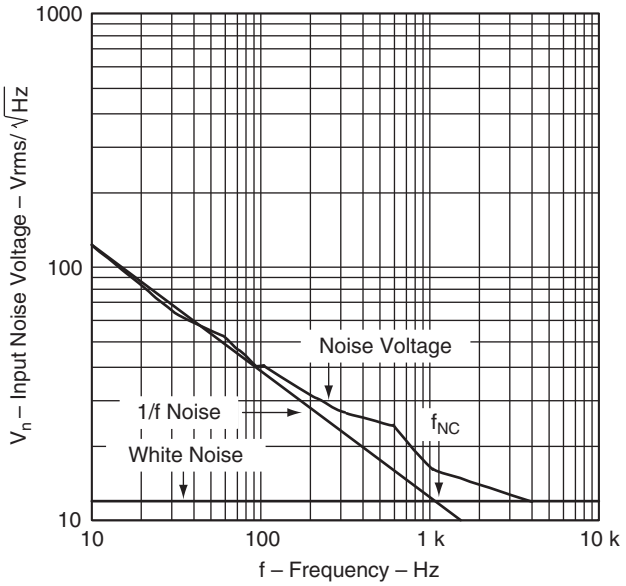


Figure 12.6: TLV2772 op amp noise characteristics.

12.5.2 The Corner Frequency

The point in the frequency spectrum where 1/*f* noise and white noise are equal is referred to as the *noise corner frequency*, f_{NC}. Note on the graph in Figure 12.6 that the actual noise voltage is higher at f_{NC} due to the root mean square addition of noise sources, as defined in Section 12.2.4.

The value of f_{NC} can be determined visually from the graph in Figure 12.6. It appears a little above 1 kHz. This was done by

- Taking the white noise portion of the curve and extrapolating it down to 10 Hz as a horizontal line.

- Taking the portion of the pink noise from 10 Hz to 100 Hz and extrapolating it as a straight line.
- The point where the two intercept is f_{NC}, the point where the white noise and pink noise are equal in amplitude. The total noise is then $\sqrt{2} \times$ white noise specification (from Section 10.2.4). This would be about 17 nV/$\sqrt{\text{Hz}}$ for the TLV2772.

This is good enough for most applications. As can be seen from the actual noise plot in Figure 12.6, small fluctuations make precise calculation impossible. There is a precise method, however:

- Determine the 1/*f* noise at the lowest possible frequency.
- Square it.
- Subtract the white noise voltage squared (subtracting noise with root mean squares is just as valid as adding).
- Multiply by the frequency. This will give the noise contribution from the 1/*f* noise.
- Then, divide by the white noise specification squared. The answer is f_{NC}.

For example, the TLV2772 has a typical noise voltage of 130 nV/$\sqrt{\text{Hz}}$ at 10 Hz (from a 5 V plot on a data sheet).

The typical white noise specification for the TLV2772 is 12 nV/$\sqrt{\text{Hz}}$ (from the data sheet) is

$$1/f \text{ noise}^2 \text{ at } 10 \text{ Hz} = \left[\left(\frac{130 \text{ nV}}{\sqrt{\text{Hz}}}\right)^2 - \left(\frac{12 \text{ nV}}{\sqrt{\text{Hz}}}\right)^2\right] \times 10 \text{ Hz} = 167,560(\text{nV})^2 \tag{12.15}$$

$$f_{NC} = \frac{1/f \text{ noise}^2 \text{ at } 10 \text{ Hz}}{\text{White noise}^2} = \frac{167,560(\text{nV})^2}{\left(\frac{12 \text{ nV}}{\sqrt{\text{Hz}}}\right)^2} = 1164 \text{ Hz} \tag{12.16}$$

Once the corner frequency is known, the individual noise components can be added together as shown in Section 12.2.2. Continuing the preceding example for a frequency range of 10 Hz to 10 kHz,

$$E_n = E_{\text{WHITENOISE}}\sqrt{f_{\text{NC}} \times 1\text{n}\frac{f_{\text{MAX}}}{f_{\text{MIN}}} + (f_{\text{MAX}} - f_{\text{MIN}})} \tag{12.17}$$

$$E_n = \frac{12\text{ nV}}{\sqrt{\text{Hz}}}\sqrt{1164\text{ Hz} \times 1\text{n}\frac{10_4}{10} + \left(10^4\text{ Hz} - 10\text{ Hz}\right)} = 1.611\ \mu\text{V} = -116\text{ dBV} \tag{12.18}$$

This example presupposed that the bandwidth includes f_{NC}. If it does not, all of the contribution is from either the $1/f$ noise or the white noise. Similarly, if the bandwidth is very large and extends to three decades or so above f_{NC}, the contribution of the $1/f$ noise can be ignored.

12.5.3 The Op Amp Circuit Noise Model

Texas Instruments measures the noise characteristics of a large sampling of devices. This information is compiled and used to determine the typical noise performance of the device. These noise specifications refer the input noise of the op amp. Some noise portions can be represented better by a voltage source and some by a current source. Input voltage noise is always represented by a voltage source in series with the noninverting input. Input current noise is always represented by current sources from both inputs to ground (Figure 12.7).

In practice, op amp circuits are designed with low source impedance on the inverting and noninverting inputs. For low source impedances and CMOS JFET inputs, only the noise voltage is important; the current sources are insignificant in the calculations because they are swamped in the input impedances.

The equivalent circuit, therefore, reduces to that shown in Figure 12.8.

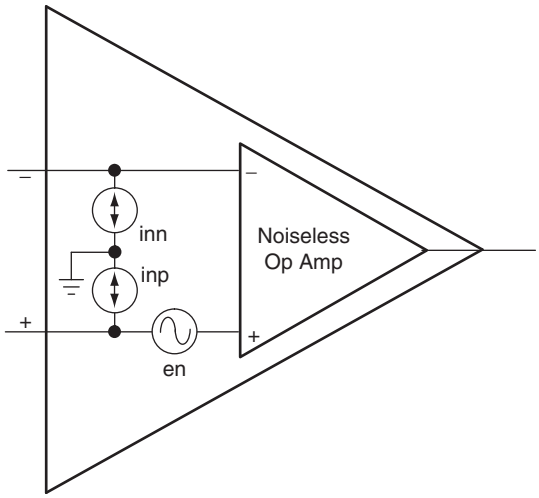


Figure 12.7: Op amp circuit noise model.

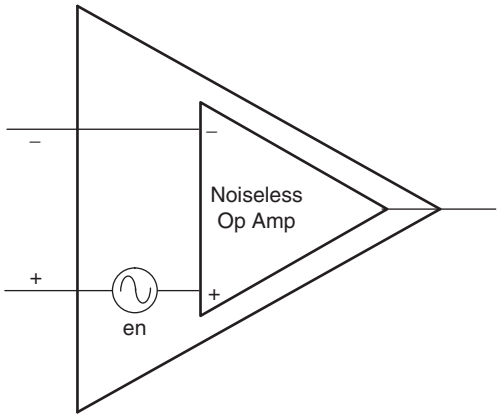


Figure 12.8: Equivalent op amp circuit noise model.

12.5.4 Inverting Op Amp Circuit Noise

If the previous circuit is operated in an inverting gain stage, the equivalent circuit becomes that shown in Figure 12.9.

The additional voltage sources e1 through e3 represent the thermal noise contribution from the resistors. As stated in Section 12.3.2, the resistor noise can also be

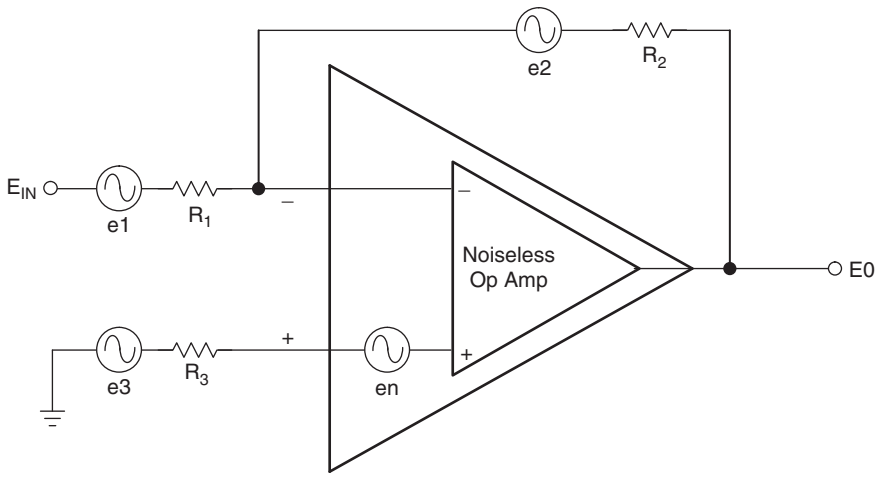


Figure 12.9: Inverting op amp circuit noise model.

discounted if the values are low. Resistor noise is omitted in the examples that follow. R_3 is also not usually present, unless low common mode performance is important. Deleting it and connecting the noninverting input directly to (virtual) ground makes the common mode response of the circuit worse but may improve the noise performance of some circuits. This means one less noise source to worry about. Therefore, the equivalent circuit becomes that shown in Figure 12.10.

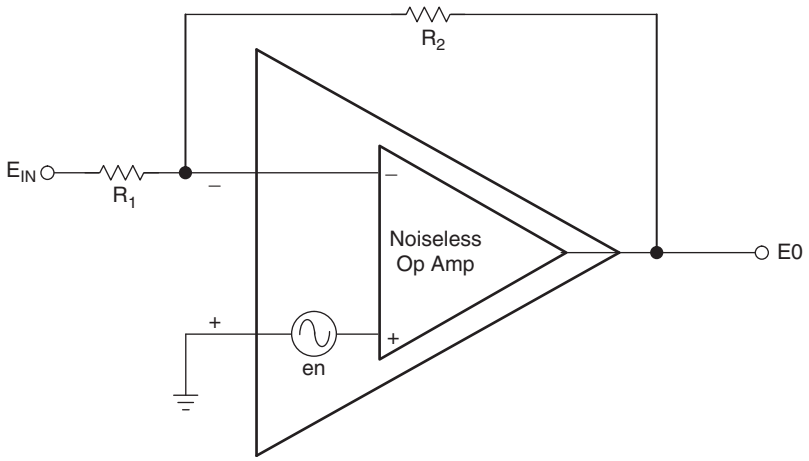


Figure 12.10: Inverting equivalent op amp circuit noise model.

This simplifies the gain calculation:

$$E_0 = \sqrt{\left(E_{IN}\frac{R_2}{R_1}\right)^2 + \left[e_n\left(1 + \frac{R_2}{R_1}\right)\right]^2} \tag{12.19}$$

where e_n = the total noise over the bandwidth of interest.

12.5.5 Noninverting Op Amp Circuit Noise

Taking the simplified equivalent op amp circuit from Section 12.5.2 as the base, the noise equivalent of a noninverting op amp circuit is shown in Figure 12.11.

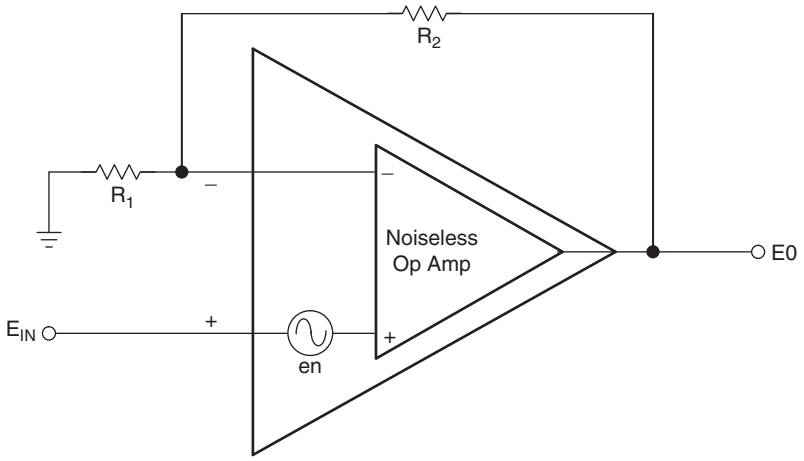


Figure 12.11: Noninverting equivalent op amp circuit noise model.

The gain of this circuit is

$$E_0 = \sqrt{\left(E_{IN}\left(1 + \frac{R_2}{R_1}\right)\right)^2 + \left[e_n\left(1 + \frac{R_2}{R_1}\right)\right]^2} \tag{12.20}$$

12.5.6 Differential Op Amp Circuit Noise Model

Taking the simplified equivalent op amp circuit from Section 12.5.2 as the base, the noise equivalent of a differential op amp circuit is shown in Figure 12.12.

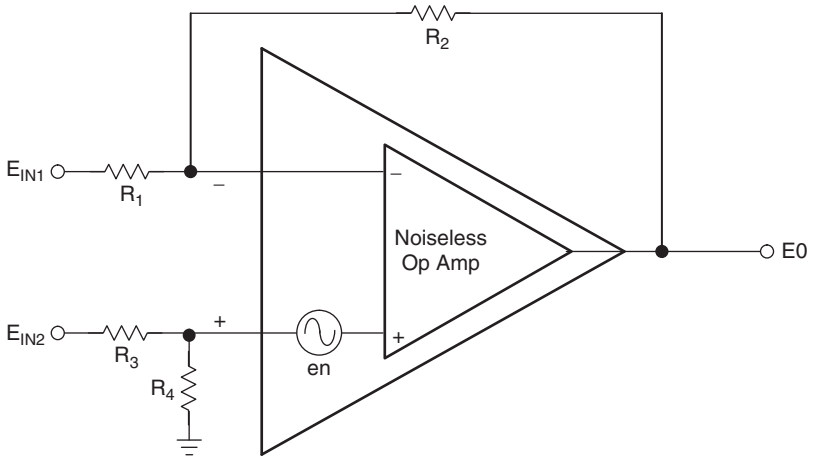


Figure 12.12: Differential equivalent op amp circuit noise model.

Assuming that $R_1 = R_3$ and $R_2 = R_4$, the gain of this circuit is

$$E_0 = \sqrt{\left((E_{IN2} - IN_{IN1})\frac{R_2}{R_1}\right)^2 + \left[e_n\left(1 + \frac{R_2}{R_1}\right)\right]^2} \tag{12.21}$$

12.5.7 Summary

The previous examples, though trivial, illustrate that noise always adds to the overall output of the op amp circuit. Reference [1] provides a much more in-depth derivation of op amp noise in circuits, including resistive effects.

12.6 Putting It All Together

This example is provided for analysis only—actual results depend on a number of other factors. Expanding on the techniques of Section 12.2.5, a low noise op amp is needed over an audio frequency range of 20 Hz to 20 kHz, with a gain of 40 dB. The output voltage is 0 dBV (1 V). The schematic is shown in Figure 12.13.

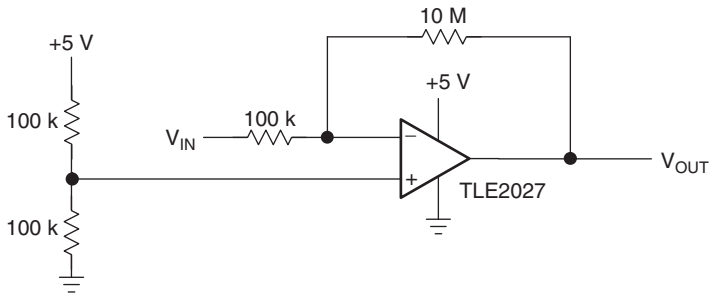


Figure 12.13: Split supply op amp circuit.

It would be nice to use a TLE2027, with a noise figure of 2.5 $\text{nV}/\sqrt{\text{Hz}}$. The data sheet, however, reveals that this is a ± 15 V part and that noise figure is specified at only ± 15 V. Furthermore, the specification for $V_{\text{OM}+}$ and $V_{\text{OM}-}$ (see Chapter 13) shows that it can swing to only within approximately 2 V of its voltage rails. If they are +5 V and ground, the op amp is close to clipping with a 1 V output signal. This illustrates a common fallacy: The designer chooses an op amp based on one parameter only, without checking others that affect the circuit. An expert analog designer must develop an attention to details or be prepared to spend a lot of time in the lab with false starts and unexpected problems.

So, the only choice is to select a different op amp. The TLC2201 is an excellent choice. It is a low noise op amp optimized for single supply operation.

The first circuit change in this example is to change the TLE2027 to a TLC2201. Visually, the corner frequency, f_{NC}, appears to be somewhere around 20 Hz (from Section 12.5.2), the lower frequency limit of the band we are interested in. This is good: It means, for all practical purposes, the $1/f$ noise can be discounted. It has 8 $\text{nV}/\sqrt{\text{Hz}}$ noise instead of 2.5 $\text{nV}/\sqrt{\text{Hz}}$, and from Section 12.2.5,

- To begin with, calculate the root hertz part: $\sqrt{20,000 - 20} = 141.35$.
- Multiply this by the noise spec, $8 \times 141.35 = 1.131$ μV, which is the equivalent input noise. The output noise equals the input noise multiplied by the gain, which is 100 (40 dB).

The signal to noise ratio can be now be calculated:

$$1.131\ \mu V \times 100 = 113.1\ \mu V$$

$$\text{Signal to noise(dB)} = 20 \times \log(1\ V \div 113.1\ \mu V) = 20 \times \log(8842) = 78.9\ dB \tag{12.22}$$

Pretty good, but it is 10 dB less than would have been possible with a TLE2027. If this is not acceptable (let's say for 16 bit accuracy), you are forced to generate a ±15 V supply. Suppose for now that 78.9 dB signal to noise is acceptable, and build the circuit.

When it is assembled, it oscillates. What went wrong?

To begin with, it is important to look for potential sources of external noise. The culprit is a long connection from the half supply voltage reference to the high impedance noninverting input. Added to that is a source impedance that does not effectively swamp external noise sources from entering the noninverting input. There is a big difference between simply providing a correct DC operating point and providing one that has low impedances where they are needed. Most designers know the "fix," which is to decouple the noninverting input, as shown in Figure 12.14.

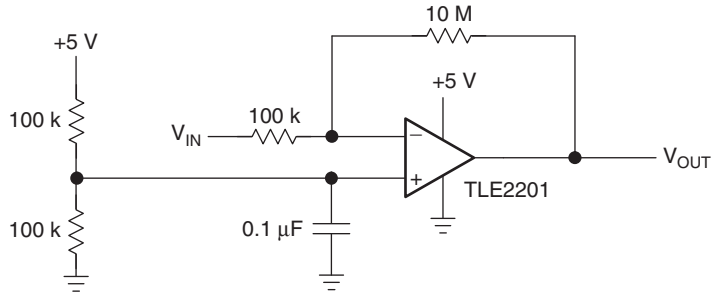


Figure 12.14: TLC2201 op amp circuit.

Better—it stopped oscillating. Probably a nearby noise source radiating into the noninverting input was providing enough noise to put the circuit into oscillation. The capacitor lowers the input impedance of the noninverting input and stops the oscillation. Much more information on this topic is found in Chapter 23, including layout effects and component selection. For now, it is assumed that all of these have been taken into account.

The circuit is still slightly noisier than the 78.9 dB signal to noise ratio given previously, especially at lower frequencies. This is where the real work of this example begins, that of eliminating component noise.

The circuit in Figure 12.15 has four resistors. Assuming that the capacitor is noiseless (not always a good assumption), that means four noise sources. For now, only the two resistors in the voltage divider that forms the voltage reference are considered. The capacitor, however, has transformed the white noise from the resistors into pink ($1/f$) noise. From Sections 12.3.2 and 12.2.5, the noise from the resistors and the amplifier itself is

$$E_{\text{TOTALrms}} = \sqrt{5.73\ \mu\text{V}^2 + 5.73\ \mu\text{V}^2 + 113.1\ \mu\text{V}^2} = 113.1\ \mu\text{V}_{\text{rms}} \tag{12.23}$$

$$\text{Signal to noise(dB)} = 20 \times \log(1\ \text{V} \div 113.1\ \mu\text{V}) = 20 \times \log(8842) = 78.9\ \text{dB} \tag{12.24}$$

So far, so good. The amplifier noise is swamping the resistor noise, which only adds a very slight pinkish component at low frequencies. Remember, however, that this noise voltage is multiplied by 101 through the circuit, but that was previously taken into account for the preceding 78.9 dB signal to noise calculation.

Reducing the value of the resistors to decrease their noise is an option. Changing the voltage divider resistors from 100 kΩ to 1 kΩ while leaving the 0.1 μV capacitor the same changes the corner frequency from 32 Hz to 796 Hz, right in the middle of the audio band.

Note: Resist the temptation to make the capacitor larger to move the pinkish effect below the lower limits of human hearing. The resulting circuit must charge the large capacitor up during power up and down during power down. This may cause unexpected results.

If the noise from the half supply generator is critical, the best possible solution is to use a low noise, low impedance half supply source. Remember, however, that its noise is multiplied by 101 in this application.

The effect of the 100 kΩ resistor on the inverting input is whitish and appears across the entire bandwidth of the circuit. Compared to the amplifier noise, it is still small, just like the noise from the noninverting resistors on the input. The noise contribution of resistors is discounted.

Of much more concern, however, is the 10 MΩ resistor used as the feedback resistor. The noise associated with it appears as a voltage source at the inverting input of the op amp and, therefore, is multiplied by a factor of 100 through the circuit. From Section 12.3.2, the noise of a 10 MΩ resistor is –84.8 dBV, or 57.3 μV. Adding this and the 100 kΩ resistor noise to the amplifier noise,

$$E_{\text{TOTALrms}} = \sqrt{5.73\ \mu\text{V}^2 + 113.1\ \mu\text{V}^2} = 126.8\ \mu\text{V}_{\text{rms}} = -77.9\ \text{dBV} \tag{12.25}$$

$$\text{Signal to noise(dB)} = 20 \times \log(1\ \text{V} \div 126.8\ \mu\text{V}) = 20 \times \log(7887) = 77.9\ \text{dB} \tag{12.26}$$

The noise contribution from the 10 MΩ resistor subtracts 1 dB from the signal to noise ratio. Changing the 10 MΩ resistor to 100 kΩ and the input resistor from 100 kΩ to 1 kΩ preserves the overall gain of the circuit. The redesigned circuit is shown in Figure 12.15.

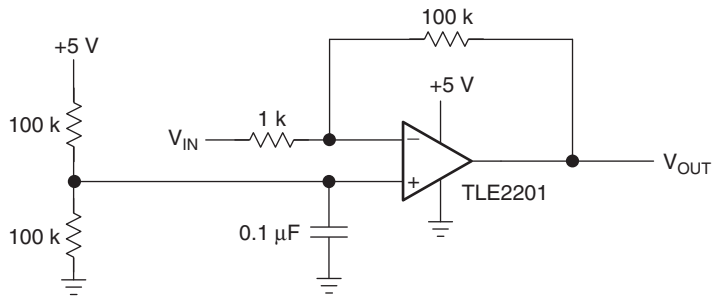


Figure 12.15: Improved TLC2201 op amp circuit.

For frequencies above 100 Hz, where the 1/*f* noise from the op amp and the reference resistors is negligible, the total noise of the circuit is

$$E_{\text{TOTALrms}} = \sqrt{0.57\ \mu\text{V}^2 + 5.73\ \mu\text{V}^2 + 113.1\ \mu\text{V}^2} = 113.2\ \mu\text{V}_{\text{rms}} = -78.9\ \text{dBV} \tag{12.27}$$

$$\text{Signal to noise(dB)} = 20 \times \log(1\ \text{V} \div 113.2\ \mu\text{V}) = 20 \times \log(8830) = 78.9\ \text{dB} \quad (12.28)$$

Proper selection of resistors, therefore, has yielded a signal to noise ratio close to the theoretical limit for the op amp itself. The power consumption of the circuit, however, has increased slightly, which may be unacceptable in a portable application. Remember, too, that this signal to noise ratio is only at an output level of 0 dBV, an input level of –40 dBV. If the input signal is reduced, the signal to noise ratio is reduced proportionally.

Music, in particular, almost never sustains peak levels. The average amplitude may be down 20 dB to 40 dB from the peak values. This erodes a 79 dB signal to noise ratio to 39 dB in quiet passages. If someone "cranks up the volume" during the quiet passages, the noise becomes audible. This is done automatically with automatic volume controls. The only way a designer can combat this is to increase the voltage levels through the individual stages. If the preceding audio stages connecting to this example, for instance, could be scaled to provide 10 dB more gain, the TLC2201 would be handling an output level of 3.16 V instead of 1 V, which is well within its rail to rail limit of 0 V to 4.7 V. This would increase the signal to noise gain of this circuit to 88.9 dB, almost the same as would have been possible with a TLE2027 operated off of ± 15 V! But noise in the preceding stages would also increase. Combatting noise is a difficult problem, and trade-offs are always involved.

Reference

1. Texas Instruments Application Report. (1999). *Noise Analysis in Operational Amplifier Circuits*, SLVA043A.

CHAPTER 13

Understanding Op Amp Parameters

Bruce Carter

13.1 Introduction

This chapter is about op amp data sheet parameters. There are usually three main sections of electrical tables in op amp data sheets.

Absolute maximum ratings are those limits beyond which the life of individual devices may be impaired and are never to be exceeded in service or testing. Limits, by definition, are maximum ratings, so if double ended limits are specified, the term is defined as a range (e.g., operating temperature range).

Recommended operating conditions have a similarity to maximum ratings, in that operation outside the stated limits could cause unsatisfactory performance. Recommended operating conditions, however, do not carry the implication of device damage if they are exceeded.

Electrical characteristics are measurable electrical properties of a device inherent in its design. They are used to predict the performance of the device as an element of an electrical circuit. The measurements that appear in the electrical characteristics tables are based on the device being operated within the recommended operating conditions.

Table 13.1 lists op amp condition and parameter abbreviations plus their corresponding description and units. Select active links to obtain additional information. As the name of the table implies, some of it is composed of parameters and some test conditions. Test conditions are conditions placed on the op amp when the parameters are measured. Some abbreviations are used for both a condition and a parameter. Units listed in the

Table 13.1: Op Amp Conditions and Parameters

Abbreviation	Parameter	Units	Abbreviation	Parameter	Units
αI_{IO}	Temperature coefficient of input offset current	A/°C	SR	Slew rate	V/S
αV_{IO} or α_{VIO}	Temperature coefficient of input offset voltage	V/°C	T_A	Operating temperature	°C
A_D	Differential gain error	%	t_{DIS} or $t_{(off)}$	Turn off time (shutdown)	s
A_m	Gain margin	dB	t_{EN} or $t_{(on)}$	Turn on time (shutdown)	s
A_{OL}	Open loop voltage gain	dB	t_f	Fall time	s
A_V	Large signal voltage amplification (gain)	dB	THD	Total harmonic distortion	%
A_{VD}	Differential large signal voltage amplification	dB	THD + N	Total harmonic distortion plus noise	%
B_1	Unity gain bandwidth	Hz	T_J	Maximum junction temperature	°C
B_{OM}	Maximum output swing bandwidth	Hz	t_r	Rise time	s
BW	Bandwidth	Hz	t_s	Settling time	s
C_I	Input capacitance	F	T_S or T_{stg}	Storage temperature	°C
C_{ic} or $C_{i(c)}$	Common mode input capacitance	F	V_{CC}, V_{DD}	Supply voltage	V
C_{id}	Differential input capacitance	F	V_I	Input voltage range	V
C_L	Load capacitance	F	V_{IC}	Common mode input voltage	V
$\Delta V_{DD\pm}$ (or CC±)/ ΔV_{IO}, or k_{SVS}	Supply voltage sensitivity	dB	V_{ICR}	Input common mode voltage range	V

Table 13.1: Op Amp Conditions and Parameters (Cont'd)

Abbreviation	Parameter	Units	Abbreviation	Parameter	Units
CMRR or k_{CMR}	Common mode rejection ratio	dB	V_{ID}	Differential input voltage	V
f	Frequency	Hz	V_{DIR}	Differential Input voltage range	V
GBW	Gain bandwidth product	Hz	$V_{IH\text{-}SHDN}$ or $V_{(ON)}$	Turn on voltage (shutdown)	V
$I_{CC\text{-}(SHDN)}$, $I_{DD\text{-}(SHDN)}$	Supply current (shutdown)	A	$V_{IL\text{-}SHDN}$ or $V_{(OFF)}$	Turn off voltage (shutdown)	V
I_{CC}, I_{DD}	Supply current	A	V_{IN}	Input voltage (DC)	V
I_I	Input current range	A	V_{IO}, V_{OS}	Input offset voltage	V
I_{IB}	Input bias current	A	V_n	Equivalent input noise voltage	$V/\sqrt{Hz}$
I_{IO}	Input offset current	A	$V_{N(PP)}$	Broadband noise	V P–P
I_n	Input noise current	$A/\sqrt{Hz}$	V_{OH}	High level output voltage	V
I_O	Output current	A	V_{OL}	Low level output voltage	V
I_{OL}	Low level output current	A	$V_{OM\pm}$	Maximum peak to peak output voltage swing	V
I_{OS} or I_{SC}	Short circuit output current	A	$V_{O(PP)}$	Peak to peak output voltage swing	V
CMRR or k_{CMR}	Common mode rejection ratio	dB	$V_{(STEP)PP}$	Step voltage peak to peak	V
k_{SVR}	Supply rejection ratio	dB	X_T	Crosstalk	dB
k_{SVS}	Supply voltage sensitivity	dB	Z_o	Output impedance	Ω
P_D	Power dissipation	W	Z_t	Open loop transimpedance	Ω

(*Continued*)

Table 13.1: Op Amp Conditions and Parameters (Cont'd)

Abbreviation	Parameter	Units	Abbreviation	Parameter	Units
PSRR	Power supply rejection ratio	dB	Φ_D	Differential phase error	°
θ_{JA}	Junction to ambient thermal resistance	°C/W	Φ_m	Phase margin	°
θ_{JC}	Junction to case thermal resistance	°C/W		Bandwidth for 0.1 dB flatness	Hz
r_i	Input resistance	Ω		Case temperature for 60 s	°C
r_{id}, $r_{i(d)}$	Differential input resistance	Ω		Continuous total dissipation	W
R_L	Load resistance	Ω		Differential gain error	%
R_{null}	Null resistance	Ω		Differential phase error	°
r_o	Output resistance	Ω		Duration of short circuit current	s
R_S	Signal source resistance	Ω		Input offset voltage long term drift	V month
				Lead temperature for 10 or 60 s	°C

units column of Table 13.1 are part of the standard SI units of measure. Multiplier prefixes such as p (pico) and M (mega) are often used in data sheets.

13.2 Temperature Coefficient of the Input Offset Current, αI_{IO}

The temperature coefficient of the input offset current, αI_{IO}, is defined as the ratio of the change in input offset current to the change in the die temperature. This is an average value for the specified temperature range.

The term αI_{IO} specifies the expected input offset current drift over temperature. Its units are microamperes per degree Centigrade. I_{IO} is measured at the temperature extremes of the part, and αI_{IO} is computed as $\Delta I_{IO}/\Delta^{\circ}C$.

Normal aging in semiconductors causes changes in the characteristics of devices. The input offset voltage long term drift specifies how I_{IO} is expected to change with time. Its units are amps per month.

13.3 Temperature Coefficient of Input Offset Voltage, αV_{IO} or α_{VIO}

The temperature coefficient of input offset voltage, αV_{IO} or α_{VIO}, is defined as the ratio of the change in input offset voltage to the change in the die temperature. This is an average value for the specified temperature range.

The term αV_{IO} specifies the expected input offset drift over temperature. Its units are volts per degree Centigrade. V_{IO} is measured at the temperature extremes of the part, and αV_{IO} is computed as $\Delta V_{IO}/\Delta^{\circ}C$.

Normal aging in semiconductors causes changes in the characteristics of devices. The input offset voltage long term drift specifies how V_{IO} is expected to change with time. Its units are microvolts per month.

13.4 Differential Gain Error, A_D

The differential gain error parameter, A_D, is defined as the change in AC gain with a change in DC level. The AC signal is 40 IRE (0.28 V PK), and the DC level change is $\pm$100 IRE ($\pm$0.7 V). Typically tested at 3.58 MHz (NTSC) or 4.43 MHz (PAL) carrier frequencies. It is represented in units of percent.

13.5 Gain Margin Parameter, A_m

Gain margin, A_m, is defined as the absolute value of the difference in gain between the unity gain point and the gain at the -180° phase shift point. It is measured for an open loop and expressed in units of decibels.

Gain margin (A_m) and phase margin (Φ_m) are different ways of specifying the stability of the circuit. Since rail to rail output op amps have higher output impedance, a significant phase shift is seen when driving capacitive loads. This extra phase shift

erodes the phase margin; and for this reason, most CMOS op amps with rail to rail outputs have limited ability to drive capacitive loads.

Figure 13.1 shows the gain margin graphically.

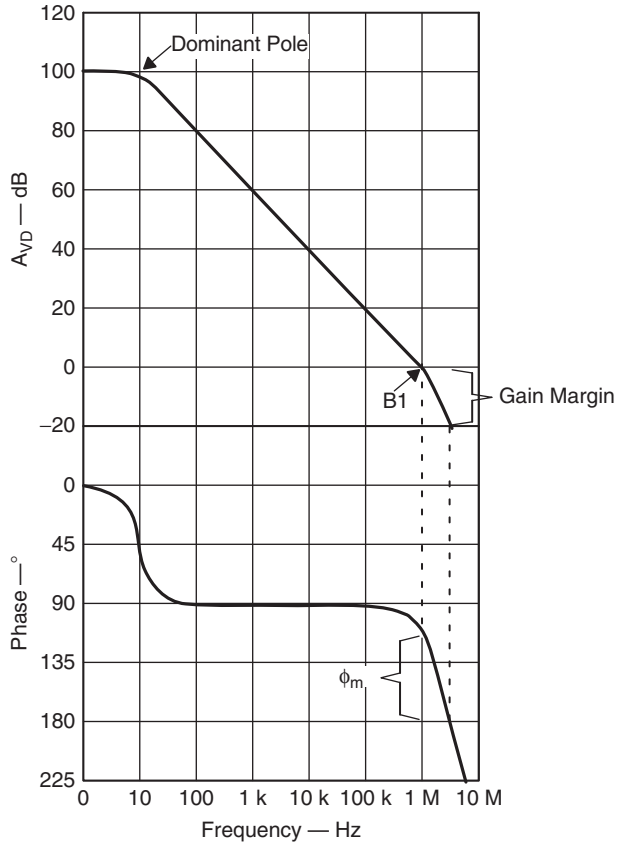


Figure 13.1: Gain and phase margin: Voltage amplification and phase shift versus frequency.

13.6 Open Loop Voltage Gain Parameter, A_{OL}

The open loop voltage gain parameter, A_{OL}, is defined as the ratio of change in output voltage to the change in voltage across the input terminals. Usually, the DC value and a graph showing the frequency dependence are shown in the data sheet. It is expressed either unitless or in decibels.

A_{OL} is similar to the open loop gain, A_{VD}, of the amplifier except that A_{VD} is usually measured with an output load. A_{OL} is usually measured with no load. Both parameters are measured as an open loop. Figure 13.2 indicates that the A_{OL} from 1 kHz to over 40 kHz is over 90 dB for this specific op amp.

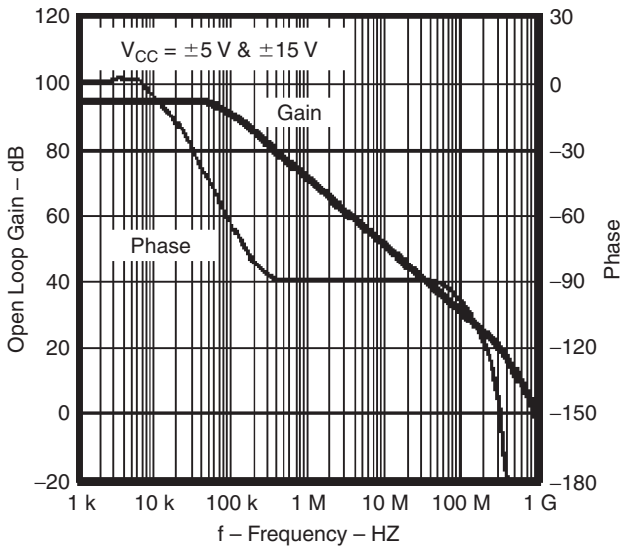


Figure 13.2: Gain and phase margin: Open loop gain and phase response versus frequency.

13.7 Large Signal Voltage Amplification Gain Condition, A_V

The large signal voltage amplification or gain condition, A_V, is defined as the ratio of change in output voltage to the change in voltage across the input terminals that is set up for a test of parameters such as Z_O or THD + N. It is expressed either unitless or in decibels.

13.8 Differential Large Signal Voltage Amplification Parameter, A_{VD}

The differential large signal voltage amplification parameter, A_{VD}, is defined as the ratio of change in output voltage to the change in voltage across the input terminals. It is expressed either unitless or in decibels. A_{VD} is sometimes referred to as *differential voltage gain.*

A_{VD} is similar to the open loop gain, A_{OL}, of the amplifier except that A_{OL} is usually measured with no load and A_{VD} is usually measured with a load. Both parameters are measured as an open loop. Figure 13.1 shows a typical graph of A_{VD} versus frequency.

A_{VD} is a design issue when precise gain is required. This is because the higher the open loop gain for the frequency bandwidth being used, the more precise is the gain. The ratio of resistors in the op amp circuit more closely defines the gain.

13.9 Unity Gain Bandwidth Parameter, B_1

The unity gain bandwidth, B_1, is defined as the range of frequencies within which the open loop voltage amplification is greater than or equal to unity (0 dB). B_1 is expressed in units of hertz.

13.10 Maximum Output Swing Bandwidth Parameter, B_{OM}

The maximum output swing bandwidth parameter, B_{OM}, is defined as the maximum frequency that the output swing is above a specified value or at the extent of its linear range. B_{OM} is also called *full power bandwidth*. B_{OM} is expressed in units of hertz.

The limiting factor for B_{OM} is the slew rate (SR). As the frequency gets higher and higher, the output becomes slew rate limited and cannot respond quickly enough to maintain the specified output voltage swing.

A simple test that relies on visual acuity for this parameter is to connect a sine wave generator to the input of an op amp circuit with a gain of 1. An oscilloscope or spectrum analyzer can be used to view the output. The generator is adjusted at low frequency and the amplitude increased until distortion (clipping) is visible on the output. The amplitude is then reduced until no distortion is visible. If a specific output amplitude is desired instead of the distortion free amplitude, then the generator should be adjusted to this amplitude. The frequency is increased until distortion is visible, then reduced until again there is no distortion visible. This is the B_{OM}. If the frequency is increased further, the resulting waveform would look more and more like a sawtooth wave. When a sawtooth wave is achieved, increasing the frequency decreases the amplitude.

The following equation expresses the relationship between B_{OM} and SR:

$$B_{OM} = SR/2\pi V_{(PP)}$$

13.11 Bandwidth Parameter, BW

Bandwidth, BW, is defined as the maximum frequency that an op amp circuit can deliver the specified output. The specified output varies and includes conditions such as small signal (−3 dB), 0.1 dB flatness, and full power. BW is expressed in units of hertz.

13.12 Input Capacitance Parameter, C_I

The input capacitance parameter, C_I, is defined as the capacitance between the input terminals of an op amp with either input grounded. It is expressed in units of farads.

C_I is one of a group of parasitic elements affecting input impedance. Figure 13.3 shows a model of the resistance and capacitance between each input terminal and ground and between the two terminals. There is also parasitic inductance, but the effects are negligible at low frequency. Input impedance is a design issue when the source impedance is high. The input loads the source.

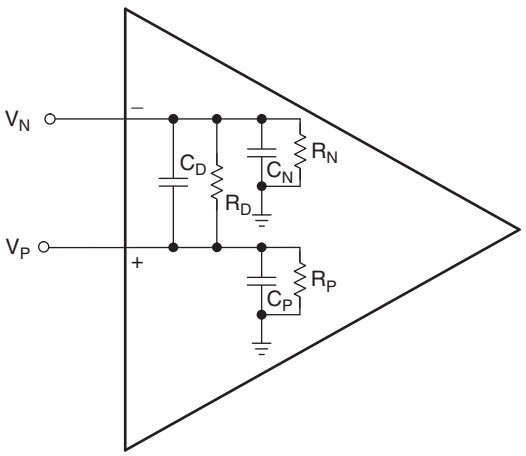


Figure 13.3: Input parasitic elements.

Input capacitance, C_I, is measured between the input terminals with either input grounded. C_I is usually a few picofarads. In Figure 13.3, if V_P is grounded, then $C_I = C_D \| C_N$.

Sometimes common mode input capacitance, C_{ic} is specified. In Figure 13.3, if V_P is shorted to V_N, then $C_{ic} = C_P \| C_N$. C_{ic} is the input capacitance a common mode source would see when referenced to ground.

13.13 Common Mode Input Capacitance Parameter, C_{ic} or $C_{i(c)}$

The common mode input capacitance parameter, C_{ic} or $C_{i(c)}$, is defined as the input capacitance a common mode source would see to ground. It is expressed in units of farads.

C_{ic} is one of a group of parasitic elements affecting input impedance. Figure 13.3 shows a model of the resistance and capacitance between each input terminal and ground and between the two terminals. There is also parasitic inductance, but the effects are negligible at low frequency. Input impedance is a design issue when the source impedance is high. The input loads the source.

Input capacitance, C_I, is measured between the input terminals with either input grounded. C_I is usually a few picofarads. In Figure 13.3, if V_P is grounded, then $C_I = C_D \| C_N$.

Sometimes, common mode input capacitance, C_{ic} is specified. In Figure 13.3, if V_P is shorted to V_N, then $C_{ic} = C_P \| C_N$. C_{ic} is the input capacitance a common mode source would see when referenced to ground.

13.14 Differential Input Capacitance Parameter, C_{id}

The differential input capacitance parameter, C_{id}, is the same as the common mode input capacitance, C_{ic}. It is the input capacitance a common mode source would see to ground. It is expressed in units of farads.

13.15 Load Capacitance Condition, C_L

The load capacitance condition, C_L, is defined as the capacitance between the output terminal of an op amp and ground. It is expressed in units of farads.

C_L is a capacitive load that is sometimes connected to an op amp when parameters such as SR, t_s, Φ_m, or A_m are being tested.

13.16 Supply Voltage Sensitivity, $\Delta V_{DD\pm(\text{or } CC\pm)}/\Delta V_{IO}$ or k_{SVS}

The power supply rejection ratio, $\Delta V_{DD\pm(\text{or } CC\pm)}/\Delta V_{IO}$, is the same as the supply rejection ratio, k_{SVR}. It is defined as the absolute value of the ratio of the change in supply voltages to the resulting change in input offset voltage. Typically, both supply voltages are varied symmetrically. It is expressed in decibels.

The power voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which in turn changes the output voltage.

For a dual supply op amp, $k_{SVR} = \Delta V_{CC\pm}/\Delta V_{OS}$ or $\Delta V_{DD\pm}/\Delta V_{OS}$. The plus and minus sign in the term $\Delta V_{CC\pm}$ means that the plus and minus power supplies are changed symmetrically. For a single supply op amp, $k_{SVR} = \Delta V_{CC}/\Delta V_{OS}$ or $\Delta V_{DD}/\Delta V_{OS}$. Also note that the mechanism that produces k_{SVR} is the same as for the common mode rejection ratio (CMRR). Therefore, k_{SVR} as published in the data sheet is a DC parameter, like CMRR. When k_{SVR} is graphed versus frequency, it falls off as the frequency increases.

Switching power supplies produce noise frequencies from 50 kHz to 500 kHz and higher. The value of k_{SVR} is almost zero at these frequencies, so noise on the power supply results in noise on the output of the op amp. Proper bypassing techniques must be used.

13.17 Common Mode Rejection Ratio Parameter, CMRR or k_{CMR}

The common mode rejection ratio parameter, CMRR or k_{CMR}, is defined as the ratio of differential voltage amplification to common mode voltage amplification. This is measured by determining the ratio of a change in input common mode voltage to the resulting change in input offset voltage. It is expressed in decibels.

Ideally, CMRR or k_{CMR} would be infinite with common mode voltages being totally rejected.

The common mode input voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which in turn changes the output voltage. The real mechanism at work is $\Delta V_{OS}/\Delta V_{COM}$.

In a Texas Instruments data sheet, CMRR $= \Delta V_{COM}/\Delta V_{OS}$, which gives a positive number in decibels. CMRR, as published in the data sheet, is a DC parameter. CMRR, when graphed versus frequency, falls off as the frequency increases.

A common source of common mode interference voltage is 50 Hz or 60 Hz AC noise. Care must be used to ensure that the CMRR of the op amp is not degraded by other circuit components. High values of resistance make the circuit vulnerable to common mode (and other) noise pick up. It is usually possible to scale resistors down and capacitors up to preserve circuit response.

13.18 Frequency Condition, *f*

Frequency condition, *f*, is the frequency available to a circuit for a specific parameter test. It is expressed in hertz.

13.19 Op Amp Gain Bandwidth Product Parameter, GBW

The gain bandwidth product, GBW, is defined as the product of the open loop voltage gain and the frequency at which it is measured. GBW is expressed in units of hertz. Figure 13.1 shows the open loop bandwidth graphically.

The GBW is similar to the unity gain bandwidth (B_1). While B_1 specifies the frequency at which the gain of the op amp is 1, GBW specifies the gain bandwidth product of the op amp at a frequency that may be different than the B_1.

The GBW is constant for voltage feedback amplifiers. It does not have much meaning for current feedback amplifiers, because there is no linear relationship between gain and bandwidth.

When an op amp is selected for a specific application, both the bandwidth and the slew rate should be taken into account (along with other factors, including power consumption, distortion, and price).

13.20 Supply Current (Shutdown) Parameter, $I_{CC(SHDN)}$ or $I_{DD(SHDN)}$

The supply current (shutdown) parameter, $I_{CC(SHDN)}$ or $I_{DD(SHDN)}$, is defined as the current into the V_{CC+} (V_{DD+}) or V_{CC-} (V_{DD-}) terminal of the amplifier while it is turned off. It is expressed in units of amps.

13.21 Supply Current Parameter, I_{CC} or I_{DD}

The supply current parameter, I_{CC} or I_{DD}, is defined as the current into the V_{CC+} (V_{DD+}) or V_{CC-} (V_{DD-}) terminal of the op amp while it is operating with no load and the input or output is at virtual ground. It is expressed in units of amps.

In a Texas Instruments data sheet, this parameter is usually the total quiescent current draw for the whole package. There are exceptions, however, such as data sheets that cover single and multiple packaged op amps of the same type. In these cases, I_{DD} is the quiescent current draw for each amplifier.

13.22 Input Current Range Parameter, I_I

The input current range parameter, I_I, is defined as the amount of current that can be sourced or sinked by the op amp input. It is usually specified as an absolute maximum rating expressed in units of amperes.

13.23 Input Bias Current Parameter, I_{IB}

The input bias current parameter, I_{IB}, is defined as the average of the currents into the two input terminals with the output at a specified level. It is expressed in units of amperes.

The input circuitry of all op amps requires a certain amount of bias current for proper operation. The input bias current, I_{IB}, is computed as the average of the two inputs:

$$I_{IB} = \frac{I_N + I_P}{2}$$

CMOS and JFET inputs offer much lower input current than standard bipolar inputs. Figure 13.4 shows a typical test circuit for measuring input bias currents.

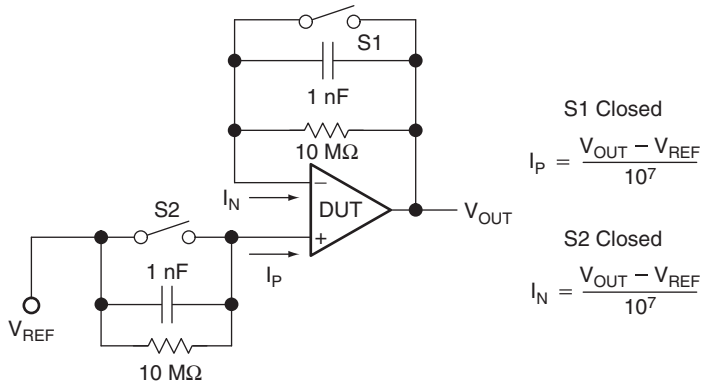


Figure 13.4: Test circuit, I_{IB}.

Input bias current is of concern when the source impedance is high. If the op amp has high input bias current, it loads the source and a lower than expected voltage is seen. If the source impedance is high, the best solution is to use an op amp with either CMOS or JFET input. The source impedance can also be lowered by using a buffer stage to drive the op amp that has high input bias current.

In the case of bipolar inputs, offset current can be nullified by matching the impedance seen at the inputs. In the case of CMOS or JFET inputs, the offset current is usually not an issue and matching the impedance is not necessary.

13.24 Input Offset Current Parameter, I_{IO}

The input offset current parameter, I_{IO}, is defined as the difference between the currents into the two input terminals of an op amp with the output at the specified level. It is expressed in units of amperes.

13.25 Input Noise Current Parameter, I_n

The input noise current parameter, I_n, is defined as the internal noise current reflected back to an ideal current source in parallel with the input pins. It is expressed in units of amperes divided by the square root of hertz.

It is important for a designer to calculate the noise that the device will deliver in an application. The simplest way to calculate this noise is to use the following equation:

$$e_{\text{nt}} = \sqrt{V_n^2 + (I_n \times R_s)^2}$$

where

e_{nt} = Total noise voltage.

V_n = Voltage noise $(\text{nV}/\sqrt{\text{Hz}})$.

I_n = Current noise $(\text{pA}/\sqrt{\text{Hz}})$.

R_s = Source resistance (Ω).

13.26 Output Current Parameter, I_O

The output current parameter, I_O, is defined as the amount of current that may be drawn from the op amp output. Usually, I_O is expressed in units of amperes.

Sometimes (for micropower op amps), I_O is specified as an absolute maximum rating, but for most op amps, it is part of the electrical characteristics tables and graphs.

13.27 Low Level Output Current Condition, I_{OL}

The low level output current condition, I_{OL}, is defined as the current into an output that is supplied during the test for V_{OL}. It is usually expressed in units of amperes.

13.28 Short Circuit Output Current Parameter, I_{OS} or I_{SC}

The short circuit output current parameter, I_{OS} or I_{SC}, is defined as the maximum output current available from the amplifier with the output shorted to ground, either supply, or a specified point. Sometimes, a low value series resistor is specified. It is usually expressed in units of amperes.

It is important to observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of the part's data sheet for more information.

13.29 Supply Rejection Ratio Parameter, k_{SVR}

The supply rejection ratio, k_{SVR}, is the same as the power supply rejection ratio, PSRR. It is defined as the absolute value of the ratio of the change in supply voltages to the resulting change in input offset voltage. Typically both supply voltages are varied symmetrically. It is expressed in decibels.

The power voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which in turn changes the output voltage.

For a dual supply op amp, $k_{SVR} = \Delta V_{CC\pm}/\Delta V_{OS}$ or $\Delta V_{DD\pm}/\Delta V_{OS}$. The plus and minus sign in the term $\Delta V_{CC\pm}$ means that the plus and minus power supplies are changed symmetrically. For a single supply op amp, $k_{SVR} = \Delta V_{CC}/\Delta V_{OS}$ or $\Delta V_{DD}/\Delta V_{OS}$. Also note that the mechanism that produces k_{SVR} is the same as for CMRR. Therefore, k_{SVR} as published in the data sheet is a DC parameter, like CMRR. When k_{SVR} is graphed versus frequency, it falls off as the frequency increases.

Switching power supplies produce noise frequencies from 50 kHz to 500 kHz and higher. The value of k_{SVR} is almost zero at these frequencies, so noise on the power supply results in noise on the output of the op amp. Proper bypassing techniques must be used.

13.30 Power Dissipation Parameter, P_D

The power dissipation, P_D, is defined as the power supplied to the device less any power delivered from the device to a load. Note: At no load, $P_D = V_{CC+} \times I_{CC}$ or $P_D = V_{DD+} \times I_{DD}$. It is expressed in units of watts.

13.31 Power Supply Rejection Ratio Parameter, PSRR

The power supply rejection ratio, PSRR, is the same as the supply rejection ratio, k_{SVR}. It is defined as the absolute value of the ratio of the change in supply voltages to the resulting change in input offset voltage. Typically, both supply voltages are varied symmetrically. It is expressed in units of decibels.

The power voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which in turn changes the output voltage.

For a dual supply op amp, $k_{SVR} = \Delta V_{CC\pm}/\Delta V_{OS}$ or $\Delta V_{DD\pm}/\Delta V_{OS}$. The plus and minus sign in the term $\Delta V_{CC\pm}$ means that the plus and minus power supplies are changed symmetrically. For a single supply op amp, $k_{SVR} = \Delta V_{CC}/\Delta V_{OS}$ or $\Delta V_{DD}/\Delta V_{OS}$. Also note that the mechanism that produces k_{SVR} is the same as for CMRR. Therefore, k_{SVR} as published in the data sheet is a DC parameter, like CMRR. When k_{SVR} is graphed versus frequency, it falls off as the frequency increases.

Switching power supplies produce noise frequencies from 50 kHz to 500 kHz and higher. The value of k_{SVR} is almost zero at these frequencies, so noise on the power supply results in noise on the output of the op amp. Proper bypassing techniques must be used.

13.32 Junction to Ambient Thermal Resistance Parameter, θ_{JA}

The junction to the ambient thermal resistance parameter, θ_{JA}, is defined as the ratio of the difference in temperature from the die junction to the ambient air and the power dissipated by the die. The value of θ_{JA} is expressed in units of degrees Centigrade per watt.

The term θ_{JA} is dependent on the case to the ambient thermal resistance as well as the θ_{JC} parameter.

The θ_{JA} is a better indicator of thermal resistance when the package is not well thermally sinked to other components in the assembly.

The θ_{JA} is listed in the data sheet for different packages. It is useful for evaluating which package is least likely to overheat and determine what the die temperature is when the ambient temperature and power dissipation are known.

The following equation more fully defines the math of heat dissipation:

$$T_J = T_A + \text{PD} \times \theta_{JA}$$

where

$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$

T_A (C°) = Temperature of ambient air.

T_J (C°) = Temperature of semiconductor junction.

PD (W) = Power dissipated in semiconductor.

θ_{JC} (°C/W) = Thermal resistance (junction to case).

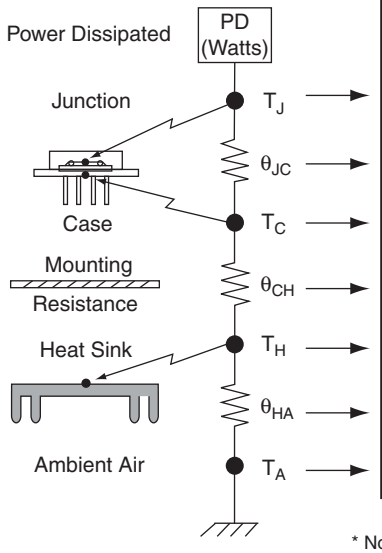
θ_{CH} (°C/W) = Thermal resistance (case to heat sink).

θ_{HA} (°C/W) = Thermal resistance (heat sink to ambient air).

θ_{JA} (°C/W) = Thermal resistance (junction to ambient air).

The design of a heat sink is based on empirical measurements made by the heat sink manufacturer and made within the enclosure of the final system. The actual math is straightforward. It looks like a simple electrical circuit. Take temperature to be the equivalent of voltage; thermal resistance is now just a simple resistor and the power is considered the same as current. Now, this looks like a linear circuit, and in fact, the resistances add linearly.

Figure 13.5 compares the performance of two heat sinks, each at two power levels. A place to start is at ground or the ambient temperature. Since the temperature within an enclosure or in some environmental areas can range widely, the expected maximum temperature should be used for T_A.



Units	High Power Application		Low Power Application	
Watts	100W	10W	10W	1W
°C	145	37*	158*	39
°C/Watt	0.8	0.8	0.8	0.8
°C	65	29	150	38
°C/Watt	0.1	0.1	0.5	0.5
°C	55	28	145	37
°C/Watt	0.3	0.3	12	12
°C	25	25	25	25

* Note the difference in junction temperature that thermal resistance can make even when operating at the same power level.

Figure 13.5: Thermal resistances.

The power is multiplied by the heat sink thermal resistance and added to the ambient temperature to find the temperature at the interface between the heat sink and the case. Each step is the same as this one, finding the temperature at the next point.

Now, the power has to pass through the mounting resistance of either 0.1 or 0.5°C/W. The 10 W dissipation can result in a junction temperature of either 37°C or 158°C. This points out the advantage of using a highly efficient heat sink to get the heat out of the device and into the air.

Installing a fan on the heat sink significantly increases its effectiveness. For example, nearly all PCs use a fan attached to the processor's heat sink for this reason.

13.33 Junction to Case Thermal Resistance Parameter, θ_{JC}

The junction to the case thermal resistance parameter, θ_{JC}, is defined as the ratio of the difference in temperature from the die junction to the case and the power dissipated by the die. The value of θ_{JC} is expressed in units of degrees Centigrade per watt.

The term θ_{JC} is not dependent on the case to the ambient thermal resistance, as is the θ_{JA} parameter. The θ_{JC} is a better indicator of thermal resistance when the package is to be thermally sinked to other components in the assembly.

The θ_{JC} is listed in the data sheet for different packages. It is useful for evaluating which package is least likely to overheat and determine what the die temperature is when the case temperature and power dissipation are known.

The following equation more fully defines the math of heat dissipation:

$$T_J = T_A + \text{PD} \times \theta_{JA}$$

where

$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$

T_A (C°) = Temperature of ambient air.

T_J (C°) = Temperature of semiconductor junction.

PD (W) = Power dissipated in semiconductor.

θ_{JC} (°C/W) = Thermal resistance (junction to case).

θ_{CH} (°C/W) = Thermal resistance (case to heat sink).

θ_{HA} (°C/W) = Thermal resistance (heat sink to ambient air).

θ_{JA} (°C/W) = Thermal resistance (junction to ambient air).

The design of a heat sink is based on empirical measurements made by the heat sink manufacturer and made within the enclosure of the final system. The actual math is straightforward. It looks like a simple electrical circuit. Take temperature to be the equivalent of voltage; thermal resistance is now just a simple resistor and the power is considered the same as current. Now, this looks like a linear circuit, and in fact, the resistances add linearly.

Figure 13.5 compares the performance of two heat sinks, each at two power levels. A place to start is at ground or at the ambient temperature. Since the temperature within an enclosure or in some environmental areas can range widely, the expected maximum temperature should be used for T_A.

The power is multiplied by the heat sink thermal resistance and added to the ambient temperature to find the temperature at the interface between the heat sink and the case. Each step is the same as this one, finding the temperature at the next point.

Now, the power has to pass through the mounting resistance of either 0.1 or 0.5°C/W. The 10 W dissipation can result in a junction temperature of either 37°C or 158°C. This points out the advantage of using a highly efficient heat sink to get the heat out of the device and into the air.

Installing a fan on the heat sink significantly increases its effectiveness. For example, nearly all PCs use a fan attached to the processor's heat sink for this reason.

13.34 Input Resistance Parameter, r_i

The input resistance parameter, r_i, is defined as the DC resistance between the input terminals with either input grounded. It is expressed in units of ohms.

The r_i is one of a group of parasitic elements affecting input impedance. Figure 13.3 shows a model of the resistance and capacitance between each input terminal and

ground and between the two terminals. There is also parasitic inductance, but the effects are negligible at low frequency. Input impedance is a design issue when the source impedance is high. The input loads the source.

Input resistance, r_i, is the resistance between the input terminals with either input grounded. In Figure 13.3, if V_P is grounded, then $r_i = R_D \| R_N$. The value of r_i ranges from 10^7 Ω to 10^{12} Ω, depending on the type of input.

Sometimes common mode input resistance, r_{ic}, is specified. In Figure 13.3, if V_P is shorted to V_N, then $r_{ic} = R_P \| R_N$. The r_{ic} is the input resistance a common mode source would see when referenced to ground.

13.35 Differential Input Resistance Parameter (r_{id} or $r_{i(d)}$)

The differential input resistance, r_{id} or $r_{i(d)}$, is defined as the small signal resistance between two ungrounded input terminals. It is expressed in units of ohms.

The r_{id} is one of a group of parasitic elements affecting input impedance. Figure 13.3 shows a model of the resistance and capacitance between each input terminal and ground and between the two terminals. There is also parasitic inductance, but the effects are negligible at low frequency. Input impedance is a design issue when the source impedance is high. The input loads the source.

Input resistance, r_i, is the resistance between the input terminals with either input grounded. In Figure 13.3, if V_P is grounded, then $r_i = R_D \| R_N$. The value of r_i ranges from 10^7 Ω to 10^{12} Ω, depending on the type of input.

Sometimes, common mode input resistance, r_{ic}, is specified. In Figure 13.3, if V_P is shorted to V_N, then $r_{ic} = R_P \| R_N$. The r_{ic} is the input resistance a common mode source would see when referenced to ground. In Figure 13.3, $r_{id} = R_D$.

13.36 Load Resistance Condition, R_L

The load resistance condition, R_L, is defined as the DC resistance that is attached from the output of an op amp to ground during a test for a parameter such as A_{VD}, SR, THD + D, $t_{(on)}$, $t_{(off)}$, GBW, t_s, φ_m, or A_m. It is expressed in units of ohms.

13.37 Null Resistance Condition, R_{null}

The null resistance condition, R_{null}, is defined as the DC resistance attached in series with C_L when testing for parameters such as phase margin or gain margin. It is expressed in units of ohms.

13.38 Output Resistance Parameters, r_o

The output resistance parameter, r_o, is defined as the DC resistance placed in series with the output of an ideal amplifier and the output terminal for simulation of the real device. It is expressed in units of ohms.

This parameter is difficult to measure, because when an amplifier is configured as an open loop, it is hard to balance the inputs to cause the output to become zero (or $V_{CC}/2$ if single supply) because of the extremely high open loop gain. When this is accomplished, a load current can be drawn from the output and the change in voltage measured. Ohm's law is then used to calculate r_o.

13.39 Signal Source Condition, R_S

The signal source condition, R_S, is defined as the output resistance of a signal source. It is expressed in units of ohms.

R_S is used as a test condition when measuring parameters such as V_{IO}, α_{VIO}, I_{IO}, I_{IB}, or CMMR. A typical value for R_S used in these parameter tests is 50 Ω.

13.40 Open Loop Transresistance Parameters, R_t

In a transimpedance or current feedback amplifier, the open loop transresistance parameter, R_t, is defined as the ratio of change in DC output voltage to the change in DC current at the inverting input. It is expressed in units of ohms.

13.41 Op Amp Slew Rate Parameter, SR

The slew rate parameter, SR, is defined as the rate of change in the output voltage caused by a step change at the input. It is expressed in volts per second. The SR parameter of an op amp is the maximum SR it will pass and is generally specified with a gain of 1. Figure 13.6 shows SR graphically.

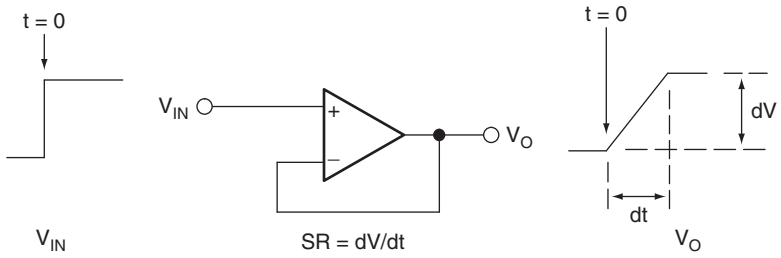


Figure 13.6: Slew rate.

For an amplifier to pass a signal without distortion due to insufficient SR, the amplifier must have at least the maximum SR of the signal. The maximum SR of a sine wave occurs as it crosses zero. The following equation defines this slew rate:

$$\text{SR} = 2\pi f V$$

f = Frequency of the signal.

V = Peak voltage of the signal.

The SR is sometimes represented as SR+ and SR−. SR+ is the abbreviation for the slew rate for a positive transition, and SR− is the abbreviation for the slew rate for a negative transition. Many applications are best served when SR+ and SR− are the same magnitude.

The primary factor controlling SR in most op amps is an internal compensation capacitor, which is added to make the op amp unity gain stable. Remember, however, that not all op amps have compensation capacitors. In op amps without internal compensation capacitors, the SR is determined by internal op amp parasitic capacitances. Noncompensated op amps generally exhibit faster SR than decompensated op amps, and decompensated op amps exhibit faster slew rates than fully compensated op amps. When noncompensated or decompensated op amps are used, the designer must ensure the stability of the circuit by other means.

The type of op amp that offers the fastest SR is the current feedback op amp. It is optimized for fast SR. Figure 13.7 shows a table of the bandwidth and SR of two high speed op amps. The graph shows the step response of a current feedback (CFB) versus a voltage feedback (VFB) op amp.

CHARACTERISTIC Part number	VOLTAGE FEEDBACK OPA2652	CURRENT FEEDBACK THS3001
Bandwidth (MHz)	700	420
Slew rate (V/μs)	335	6500

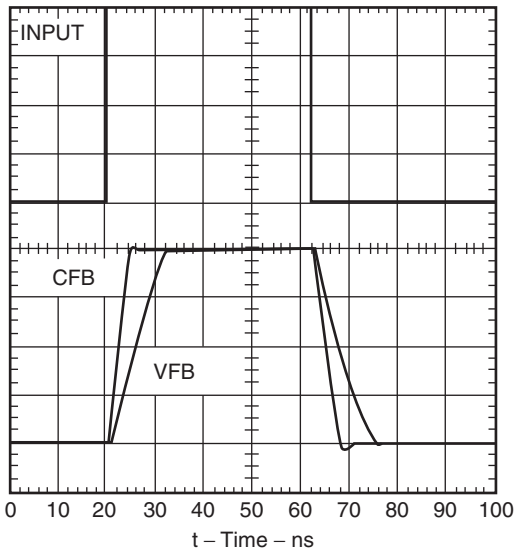


Figure 13.7: Bandwidth versus slew rate.

When an op amp is selected for a specific application both the bandwidth and the SR should be taken into account (along with other factors, including power consumption, distortion, and price).

13.42 Operating Free Air Temperature Condition, T_A

The operating free air temperature condition, T_A, is defined as the free air temperature over which the op amp is being operated. Some of the other parameters may change with temperature, leading to degraded operation at temperature extremes. The value of T_A is expressed in units of degrees Centigrade.

A range of T_A is listed in a data sheet's absolute maximum ratings table, because stress beyond those listed may cause permanent damage to the device. Functional operation

to this limit is not implied and may affect reliability. Another range of T_A is listed in a data sheet's recommended operating conditions. The term T_A is also used in a data sheet to define a condition during parameter tests and typical characteristic graphs. In addition, it may be one of the axis variables on a chart.

13.43 Turn off Time (Shutdown) Parameter, t_{DIS} or $t_{(off)}$

The turn off time (shutdown) parameter, t_{DIS} or $t_{(off)}$, is defined as the time from when the turn off voltage is applied to the shutdown pin to when the supply current has reached half of its final value. It is expressed in units of seconds.

13.44 Turn on Time (Shutdown) Parameter, t_{EN}

The turn on time (shutdown) parameter, t_{EN}, is defined as the time from when the turn on voltage is applied to the shutdown pin to when the supply current has reached half of its final value. It is expressed in units of seconds.

13.45 Fall Time Parameter, t_f

The fall time parameter, t_f, is defined as the time required for an output voltage step to change from 90% to 10% of its final value. It is expressed in units of seconds.

13.46 Total Harmonic Distortion Parameter, THD

The total harmonic distortion parameter, THD, is defined as the ratio of the rms voltage of the harmonics of the fundamental signal to the total rms voltage at the output. THD is expressed in "dBc" (decibel relative to the carrier) or percent.

THD does not account for the noise as does the total harmonic distortion plus noise parameter.

13.47 Total Harmonic Distortion Plus Noise Parameter, THD + N

The total harmonic distortion plus noise parameter, THD + N, is defined as the ratio of the rms noise voltage plus the rms harmonic voltage of the fundamental signal to the fundamental rms voltage signal at the output. It is expressed in dBc or percent.

THD + N compares the frequency content of the output signal to the frequency content of the input. Ideally, if the input signal is a pure sine wave, the output signal is a pure sine wave. Due to nonlinearity and noise sources within the op amp, the output is never pure.

To simplify further, THD + N is the ratio of all other frequency components to the fundamental:

$$\text{THD} + \text{N} = \left[\frac{(\sum \text{Harmonic voltages} + \text{Noise voltages})}{\text{Fundamental}}\right] \times 100\%$$

Figure 13.8 shows a hypothetical graph where THD + N = 1%. The fundamental is the same frequency as the input signal. The nonlinear behavior of the op amp results in harmonics of the fundamental being produced in the output. The noise in the output is due to the input noise of the op amp and other noise sources. All the harmonics and noise added together are 1% of the fundamental.

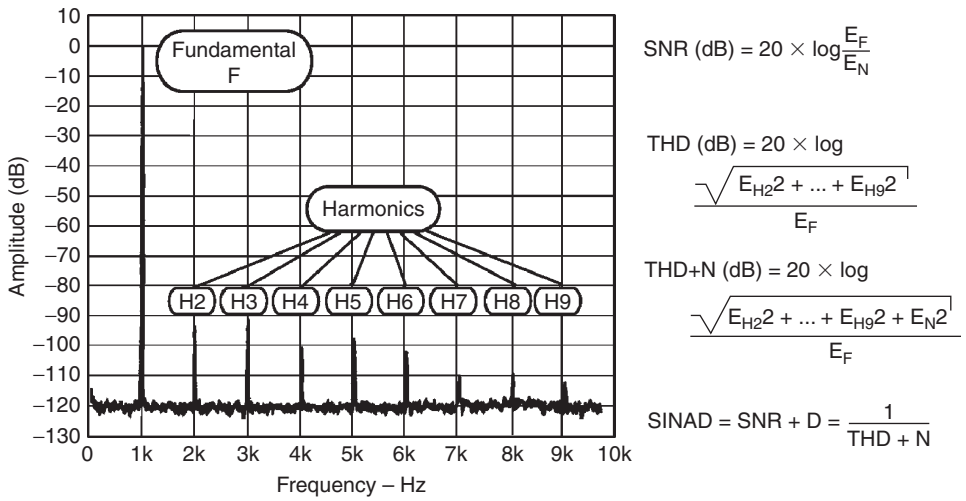


Figure 13.8: Graph of THD + N = 1%.

The three greatest causes of distortion in an op amp are the limit on output voltage swing, Class A–B crossover nonlinearity, and slew rate. Typically an op amp must be

operated at or below its recommended operating conditions to realize low THD. Figure 13.9 shows two signals. The lower frequency signal is a low distortion sine wave while the higher frequency signal is distorted because of slew rate limitation. Figure 13.10 shows a signal with clipping caused by a limited output voltage swing. Finally, Figure 13.11 shows a signal with crossover distortion caused by Class A–B crossover nonlinearity.

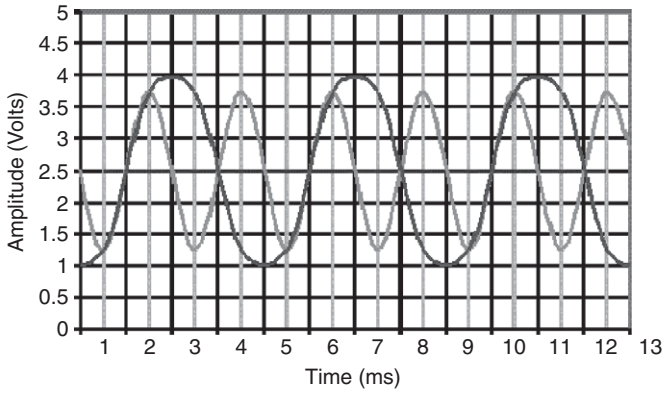


Figure 13.9: Effect of slew rate limits on signals.

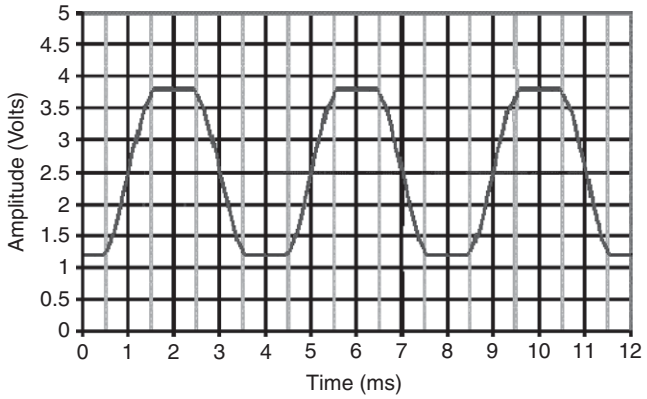


Figure 13.10: Signal with distortion due to clipping.

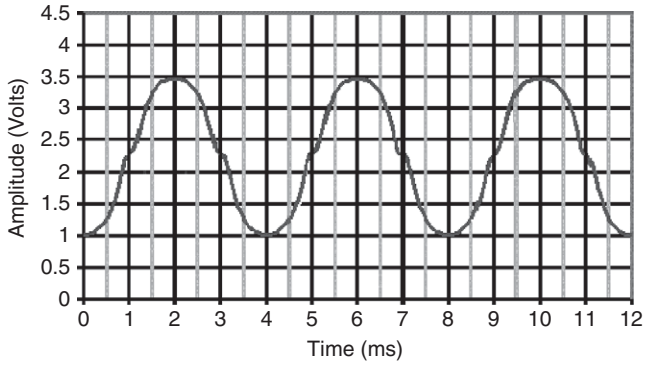


Figure 13.11: Signal with crossover distortion.

13.48 Maximum Junction Temperature Parameter, T_J

The maximum junction temperature parameter, T_J, is defined as the temperature over which the die may be operated. Some of the other parameters may change with temperature, leading to degraded operation at temperature extremes. The value of T_J is expressed in units of degrees Centigrade.

The term T_J is listed in the absolute maximum ratings table, because stress beyond those listed may cause permanent damage to the device. Functional operation to this limit is not implied and may affect reliability.

13.49 Rise Time Parameter, t_r

The rise time parameter, t_r, is defined as the time required for an output voltage step to change from 10% to 90% of its final value. It is expressed in units of seconds.

13.50 Settling Time Parameter, t_s

The settling time parameter, t_s, is defined as the time required for the output voltage to settle within the specified error band of the final value with a step change at the input. It is also known as *total response time*, t_{tot}. It is expressed in units of seconds.

It takes a finite time for a signal to propagate through the internal circuitry of an op amp. Therefore, it takes a period of time for the output to react to a step change in the input. In addition, the output normally overshoots the target value, experiences damped oscillation, and settles to a final value. Figure 13.12 shows t_s graphically.

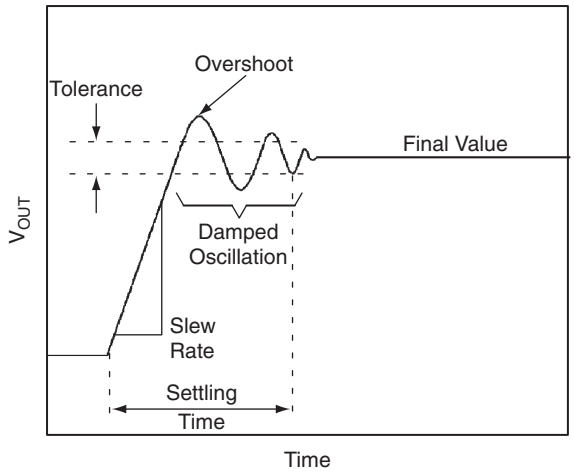


Figure 13.12: Settling time.

Settling time is a design issue in data acquisition circuits when signals are changing rapidly. An example is when using an op amp following a multiplexer to buffer the input to an A to D converter. Step changes can occur at the input to the op amp when the multiplexer changes channels. The output of the op amp must settle to within a certain tolerance before the A to D converter samples the signal.

13.51 Storage Temperature Parameter, T_S or T_{stg}

The storage temperature parameter, T_S or T_{stg}, is defined as the temperature over which the op amp may be stored (unpowered) for long periods of time without damage. It is expressed in units of degrees Centigrade.

13.52 Supply Voltage Condition, V_{CC} or V_{DD}

The supply voltage condition, V_{CC} or V_{DD}, is defined as the bias voltage applied to the op amp power supply pin(s). For single supply applications, it is specified as a positive value; and for split supply applications, it is specified as a plus or minus value, referenced to analog ground. It is expressed in units of volts.

The term V_{CC} or V_{DD} is often defined in the maximum ratings, recommended operating conditions, and as a test condition in parameter tables and graphs, because the voltage

supplied has an important impact on the way a circuit operates. It is also used as one of the axis variables in some of the characteristic graphs.

13.53 Input Voltage Range Condition or Parameter, V_I

The input voltage range parameter, V_I, is defined as the range of input voltages that may be applied to either the IN+ or IN− inputs.

The input voltage range condition, V_I, is defined as the voltage delivered to a circuit input when testing for V_O on a graph, such as Large Signal Inverting Pulse Response versus Time.

The value of V_I is expressed in units of volts for either a condition or parameter.

13.54 Common Mode Input Voltage Condition, V_{IC}

The common mode input voltage condition, V_{IC}, is defined as the voltage that is common to both input pins. The value of V_{IC} as expressed in units of volts.

The term V_{IO} set at $V_{DD}/2$ (for single supply op amps) is often used as a condition when testing for various parameters including V_{IO}, I_{IO}, I_{IB}, V_{OH}, or V_{OL}.

When a two wire signal is subject to noise and this noise is being received equally on both signal lines, it can be rejected by a differential amplifier with good common mode rejection.

13.55 Common Mode Input Voltage Range Parameter, V_{ICR}

The common mode input voltage range parameter, V_{ICR}, is defined as the range of common mode input voltage that, if exceeded, may cause the operational amplifier to cease functioning properly. This sometimes is taken as the voltage range over which the input offset voltage remains within a set limit. The value of V_{ICR} is expressed in units of volts.

The input common voltage, V_{IC}, is defined as the average voltage at the inverting and noninverting input pins. If the common mode voltage gets too high or too low, the inputs shut down and proper operation ceases. The common mode input voltage range, V_{ICR}, specifies the range over which normal operation is guaranteed.

Different input structures allow for different input common mode voltage ranges:

- The LM324 and LM358 use bipolar pnp inputs that have their collectors connected to the negative power rail. This allows the common mode input voltage range to include the negative power rail.
- The TL07X and TLE207X type BiFET op amps use p-channel JFET inputs with the sources tied to the positive power rail via a bipolar current source. This allows the common mode input voltage range to include the positive power rail.
- TI LinCMOS op amps use p channel CMOS inputs with the substrate tied to the positive power rail. This allows the common mode input voltage range to include the negative power rail.
- Rail to rail input op amps use complementary n- and p-type devices in the differential inputs. When the common mode input voltage nears either rail, at least one of the differential inputs is still active, and the common mode input voltage range includes both power rails.

The trends toward lower, single supply voltages make V_{ICR} of increasing concern.

Rail to rail input is required when a noninverting unity gain amplifier is used and the input signal ranges between both power rails. An example of this is the input of an analog to digital converter in a low voltage, single supply system.

High side sensing circuits require operation at the positive input rail.

13.56 Differential Input Voltage Parameter, V_{ID}

The differential input voltage parameter, V_{ID}, is defined as the voltage at the noninverting input with respect to the inverting input. The value of V_{ID} is expressed in units of volts.

The limit V_{ID} is usually defined in the absolute maximum ratings table, because stress beyond this limit may cause permanent damage to the device.

13.57 Differential Input Voltage Range Parameter, V_{DIR}

The input common mode voltage range parameter, V_{DIR}, is defined as the range of differential input voltage that, if exceeded, may cause the operational amplifier to cease functioning properly. The value of V_{DIR} is expressed in units of volts.

Some devices have protection built into them, and the current into the input needs to be limited. Normally, differential input mode voltage limit is not a design issue.

13.58 Turn on Voltage (Shutdown) Parameter, $V_{IH\text{-}SHDN}$ or $V_{(ON)}$

The turn on voltage (shutdown) parameter, $V_{IH\text{-}SHDN}$ or $V_{(ON)}$, is defined as the voltage required on the shutdown pin to turn the device on. It is expressed in units of volts.

13.59 Turn off Voltage (Shutdown) Parameter, $V_{IL\text{-}SHDN}$ or $V_{(OFF)}$

The turn off voltage (shutdown) parameter, $V_{IL\text{-}SHDN}$ or $V_{(OFF)}$, is defined as the voltage required on the shutdown pin to turn the device off. It is expressed in units of volts.

13.60 Input Voltage Condition, V_{IN}

The input voltage condition, V_{IN}, is defined as the DC voltage delivered to a circuit input when testing for V_n. The value of V_{IN} is expressed in units of volts.

13.61 Input Offset Voltage Parameter, V_{IO} or V_{OS}

The input offset voltage parameter, V_{IO} or V_{OS}, is defined as the DC voltage that must be applied between the input terminals to cancel DC offsets within the op amp. It is expressed in units of volts.

All op amps require a small voltage between their inverting and noninverting inputs to balance mismatches due to unavoidable process variations. The required voltage, known as the *input offset voltage*, is abbreviated V_{IO}. V_{IO} is normally modeled as a voltage source driving the noninverting input.

Figure 13.13 shows two typical methods for measuring input offset voltage. DUT stands for device under test. Test circuit (a) is simple, but since V_{OUT} is not at zero volts, it does not really meet the definition of the parameter. Test circuit (b) is referred to as a servo loop. The action of the loop is to maintain the output of the DUT at zero volts.

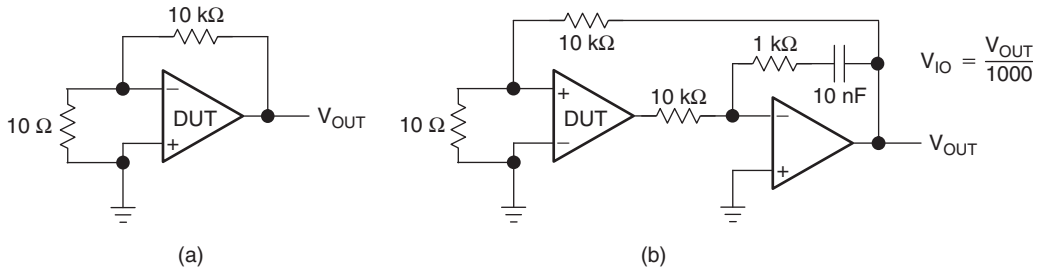


Figure 13.13: Test circuits for input offset voltage.

V_{IO} is an input referred parameter. This means that it is amplified by the positive closed loop gain of the circuit. For this reason, the figure indicates that V_{IO} is V_{OUT} divided by 1000. This constant is used because the gain of the DUT is 1000.

V_{IO} is normally attributed to the characteristics of the input differential pair in a voltage feedback amplifier. Different processes provide certain advantages. Bipolar input stages tend to have lower offset voltages than CMOS or JFET input stages.

Input offset voltage is of concern anytime that DC accuracy is required of the circuit. One way to null the offset is to use external null inputs on a single op amp package (see Figure 13.14). A potentiometer is connected between the null inputs with the adjustable terminal connected to the negative supply through a series resistor. The input offset voltage is nulled by shorting the inputs and adjusting the potentiometer until the output is zero.

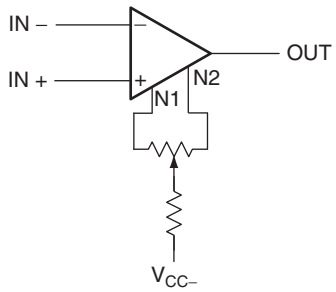


Figure 13.14: Offset voltage adjust.

13.62 Equivalent Input Noise Voltage Parameter, V_n

The equivalent input noise voltage parameter, V_n, is defined as the internal noise voltage reflected back to an ideal voltage source in parallel with the input pins at a specific frequency. The value of V_n is expressed in units of volts per the square root of hertz.

When this parameter is measured, the noise measured at the output (with the input connected to virtual ground) is divided by the gain of the amplifier circuit. This is the amplitude of noise at the input that would be amplified by an ideal amplifier to cause an equivalent signal at the output.

The limit of V_n is sometimes defined at several frequencies in the operating characteristics table or as a graph.

Given the same structure within an op amp, increasing bias currents lowers noise (and increases SR, GBW, and power dissipation).

Also the resistance seen at the input to an op amp adds noise. Balancing the input resistance on the noninverting input to that seen at the inverting input, while helping with offsets due to input bias current, adds noise to the circuit.

It is important for a designer to calculate noise that the device will deliver in an application. The simplest way is to calculate this noise is to use the following equation:

$$e_{\text{nt}} = \sqrt{V_n^2 + (I_n \times R_s)^2}$$

where

e_{nt} = Total noise voltage.

V_n = Voltage noise $(\text{nV}/\sqrt{\text{Hz}})$.

I_n = Current noise $(\text{pA}/\sqrt{\text{Hz}})$.

R_s = Source resistance (Ω).

13.63 Broadband Noise Parameter ($V_{\text{N(PP)}}$)

The broadband noise parameter, $V_{\text{N(PP)}}$, is defined as the peak to peak voltage over a specific frequency band, typically 0.1 Hz to 1 Hz or 0.1 Hz to 10 Hz. The units of measurement are typically volts peak to peak.

Given the same structure within an op amp, increasing bias currents lowers noise (and increases SR, GBW, and power dissipation).

Also the resistance seen at the input to an op amp adds noise. Balancing the input resistance on the noninverting input to that seen at the inverting input, while helping with offsets due to input bias current, adds noise to the circuit.

13.64 High Level Output Voltage Condition or Parameter, V_{OH}

The high level output voltage parameter, V_{OH}, is defined as the positive rail of the op amp output for the load current conditions applied to the power pins. When the V_{OH} parameter is tested, it may be defined with an I_{OH} of -1 mA, -20 mA, -35 mA, or -50 mA load.

When V_{OH} is listed on a data sheet as a test condition, it is used for testing another parameter. Whether V_{OH} is a condition or a parameter it is expressed in units of volts.

13.65 Low Level Output Voltage Condition or Parameter, V_{OL}

The low level output voltage parameter, V_{OL}, is defined as the negative rail of the op amp output for the load current conditions applied to the power pins. When the V_{OL} parameter is tested it may be defined with an I_{OL} of -1 mA, -20 mA, -35 mA, or -50 mA load.

When V_{OL} is listed on a data sheet as a test condition, it is used for testing another parameter.

Whether V_{OL} is a condition or parameter it is expressed in units of volts.

13.66 Maximum Peak to Peak Output Voltage Swing Parameter, $V_{OM\pm}$

The maximum peak to peak output voltage swing parameter, $V_{OM\pm}$, is defined as the maximum peak to peak output voltage that can be obtained without clipping when the op amp is operated from a bipolar supply. The value of $V_{OM\pm}$ is expressed in units of volts.

Another way to describe $V_{OM\pm}$ is the maximum positive or negative peak output voltage that can be obtained without waveform clipping, when quiescent DC output voltage is zero. $V_{OM\pm}$ is limited by the output impedance of the amplifier, the saturation voltage of the output transistors, and the power supply voltages. This is shown pictorially in Figure 13.15.

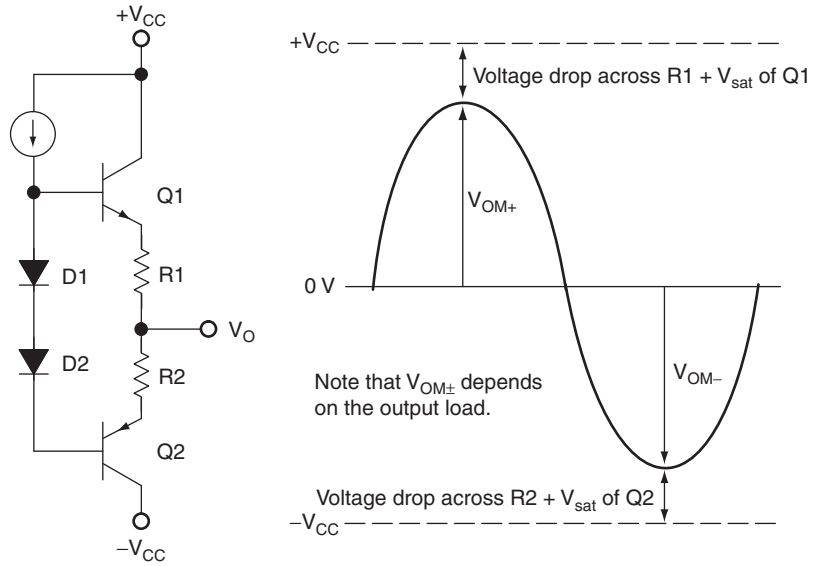


Figure 13.15: $V_{OM\pm}$.

This emitter/follower structure cannot drive the output voltage to either rail. Rail to rail output op amps use a common emitter (bipolar) or common source (CMOS) output stage. With these structures, the output voltage swing is limited by only the saturation voltage (bipolar) or the on resistance (CMOS) of the output transistors and the load being driven.

Because newer products are focused on single supply operation, more recent data sheets from Texas Instruments use the terminology V_{OH} and V_{OL} to specify the maximum and minimum output voltages.

Maximum and minimum output voltage is usually a design issue when dynamic range is lost if the op amp cannot drive to the rails. This is the case in single supply systems where the op amp is used to drive the input of an A to D converter, which is configured for full scale input voltage between ground and the positive rail.

13.67 Peak to Peak Output Voltage Swing Condition or Parameter, $V_{O(PP)}$

The peak to peak output voltage swing condition, $V_{O(PP)}$, is defined as the peak to peak voltage set up on the output waveform to test for parameters such as A_{VD} or SR.

The peak to peak output voltage swing parameter, $V_{O(PP)}$, is the maximum peak to peak output voltage that an op amp can deliver. When it is measured, V_{DD}, THD + N, R_L, and T_A are the typical test conditions.

The value of $V_{O(PP)}$ is also expressed in units of volts for either a condition or parameter.

13.68 Step Voltage Peak to Peak Condition, $V_{(STEP)PP}$

The step voltage peak to peak condition, $V_{(STEP)PP}$, is defined as the peak to peak voltage step that is used as a test condition for parameters such as t_s. The value of $V_{(STEP)PP}$ is expressed in units of volts.

13.69 Crosstalk Parameter, X_T

The crosstalk parameter, X_T, is defined as the ratio of the change in output voltage of a driven channel to the resulting change in output voltage from another channel that is not driven. The value of X_T is expressed in units of decibels.

X_T is a function of how good the separation is between channels in an IC package or system. It is caused by the signal from one channel being coupled to the other channel inductively, capacitively, through the power supply, and so forth.

13.70 Output Impedance Parameter, Z_o

The output impedance parameter, Z_o, is defined as the frequency dependent small signal impedance that is placed in series with an ideal amplifier and the output terminal in a closed loop configuration. The value of Z_o is expressed in units of ohms. Figure 13.16 is an example of defining Z_o and is shown with gains of 1, 10, and 100.

Common emitter (bipolar) and common source (CMOS) output stages used in rail to rail output op amps have higher output impedance than emitter/follower output stages.

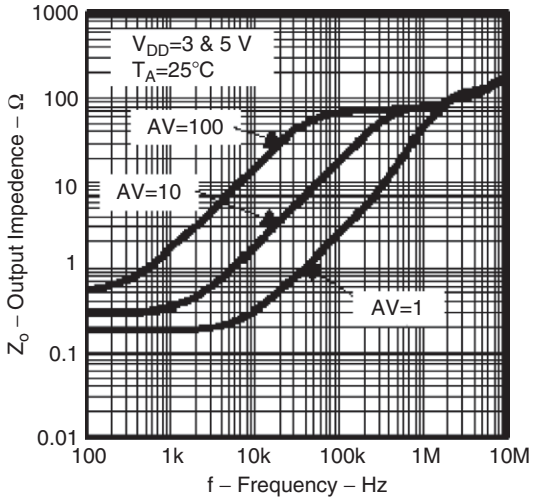


Figure 13.16: Output impedance versus frequency.

Output impedance is a design issue when using rail to rail output op amps to drive heavy loads. If the load is mainly resistive, the output impedance limits how close to the rails the output can go. If the load is capacitive, the extra phase shift erodes the phase margin.

Figure 13.17 shows how output impedance affects the output signal, assuming Z_o is mostly resistive.

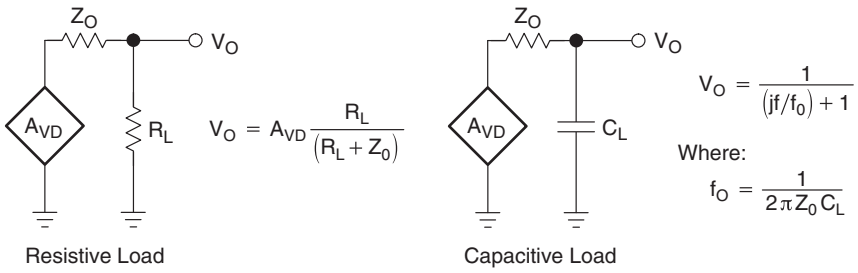


Figure 13.17: Effect of output impedance.

Some new audio op amps are designed to drive the load of a speaker or headphone directly. They can be an economical method of obtaining very low output impedance.

13.71 Open Loop Transimpedance Parameter, Z_t

The open loop transimpedance parameter, Z_t, is defined as the frequency dependent ratio of change in output voltage to the frequency dependent change in current at the inverting input in a transimpedance or current feedback amplifier. The value of Z_t is expressed in units of ohms.

13.72 Differential Phase Error Parameter, Φ_D

The differential phase error parameter, Φ_D, is defined as the change in AC phase with a change in DC level. The AC signal is 40 IRE (0.28 V PK) and the DC level change is ±100 IRE (±0.7 V). It is typically tested at 3.58 MHz (NTSC) or 4.43 MHz (PAL) carrier frequencies. The value of Φ_D is expressed in units of degrees.

13.73 Phase Margin Parameter, Φ_m

The phase margin parameter, Φ_m, is defined as the absolute value of the difference in the phase shift of 180° and the phase shift at unity gain. The Φ_m is measured as an open loop and is expressed in units of degrees:

$$\Phi_m = 180^\circ - \Phi \text{ at } B_1$$

Gain margin (A_m) and phase margin (Φ_m) are different ways of specifying the stability of the circuit. Since rail to rail output op amps have higher output impedance, a significant phase shift is seen when driving capacitive loads. This extra phase shift erodes the phase margin, and for this reason, most CMOS op amps with rail to rail outputs have limited ability to drive capacitive loads.

Figure 13.1 shows Φ_m graphically.

13.74 Bandwidth for 0.1 dB Flatness

The bandwidth for 0.1 dB flatness is defined as the range of frequencies within which the gain is ±0.1 dB of the nominal value with full output power. It is expressed in units of hertz. Figure 13.18 describes a device with the bandwidth for 0.1 dB flatness to 100 MHz.

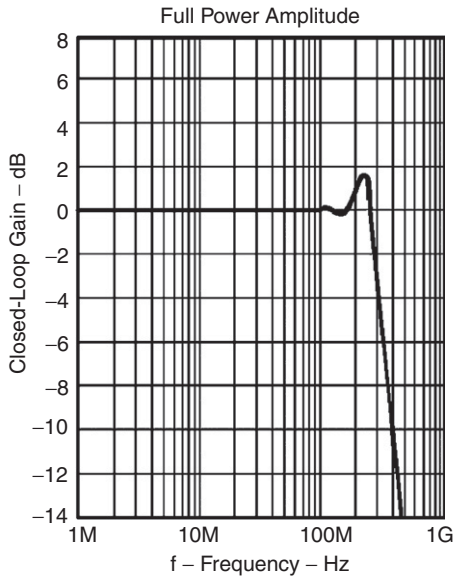


Figure 13.18: 0.1 dB flatness.

13.75 Case Temperature for 60 Seconds

The case temperature for 60 s is defined as the temperature to which the case may safely be exposed for 60 s. It is usually specified as an absolute maximum and is meant as a guide for automated soldering processes. It is expressed in degrees Centigrade.

13.76 Continuous Total Dissipation Parameter

The continuous total dissipation parameter is defined as the power that can be dissipated by an op amp package, including loads. It is usually specified as an absolute maximum. This parameter may be broken down by ambient temperature and package style in a table.

Continuous total dissipation is expressed in units of watts.

13.77 Duration of Short Circuit Current

The duration of the short circuit current parameter is defined as the amount of time that the output can be shorted to network ground. It is usually specified as an absolute maximum. The duration of short circuit current is usually expressed in seconds.

13.78 Input Offset Voltage Long Term Drift Parameter

The input offset voltage long term drift parameter is defined as the ratio of the change in input offset voltage to the change in time. It is the average value for the month and is expressed in units of volts per month.

13.79 Lead Temperature for 10 or 60 Seconds

The lead temperature for 10 or 60 s is defined as the temperature to which the leads may safely be exposed for 10 or 60 s. It is usually specified as an absolute maximum and is meant as a guide for automated soldering processes. This parameter is expressed in units of degrees Centigrade.

CHAPTER 14

Instrumentation: Sensors to A/D Converters

Ron Mancini

14.1 Introduction

The typical transducer measurement system block diagram is shown in Figure 14.1. The transducer is the electronic system's interface with the real world, and it issues data about a variable. The transducer converts the data into an electrical signal adequate for processing by the circuitry that follows the transducer. Bias and excitation circuitry does the care and feeding of the transducer, providing the offset voltages, bias currents, excitation signals, external components, and protection required for the transducer to operate properly. The output of the transducer is an electrical signal representing the measured variable.

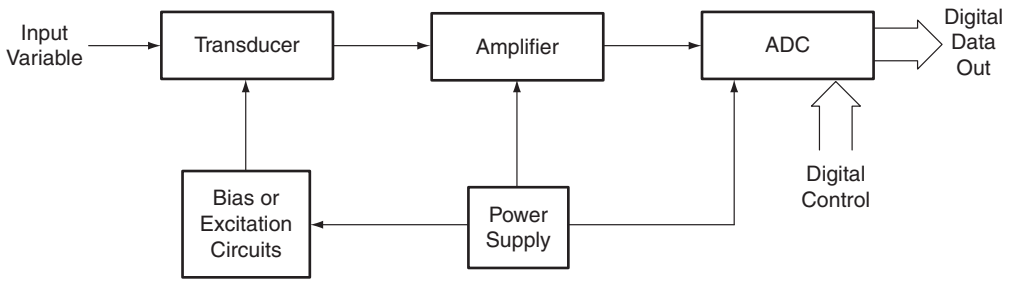


Figure 14.1: Block diagram of a transducer measurement system.

The variables that must be measured are determined by the customer's application, and the *measured variable* normally dictates the transducer selection. If the measured

variable is temperature, then some sort of temperature sensing transducer must be employed and the range of temperatures to be measured or the accuracy of the measurement is the primary factor influencing temperature transducer selection. Note that the electrical output of the transducer is not a major concern at this point in the transducer selection. The transducer's electrical output is always a consideration, although picking the right transducer for the job is the primary goal. The correct transducer for the job can have an ohm per degree Centigrade change, microvolt per degree Centigrade change, or millivolt per degree Centigrade change. All transducers have offset voltages or currents, and they can be referenced to ground, either power supply rail, or some other voltage. The selection of the transducer is out of circuit designer's hands; therefore the circuit designer must accept what the application demands.

The A/D converter (ADC) selection is based on several system criteria, such as resolution, conversion speed, power requirements, physical size, processor compatibility, and interface structure. The ADC must have enough bits to obtain the resolution required by the accuracy specification. The formula for calculating the resolution of an ADC is given in Equation (14.1), where n is the number of significant bits contained in the ADC:

$$\text{Resolution} = 2^n \tag{14.1}$$

Some confusion exists about the word *bits*, because the same word is used for binary bits and significant bits. Binary bits are ones and zeros used to calculate binary numbers; for example, a converter with eight digital states has significant bits and $2^n = 256$ binary bits (see Figure 14.2). The voltage value of a single bit, called a *least significant bit* (LSB), is calculated in Equation (14.2):

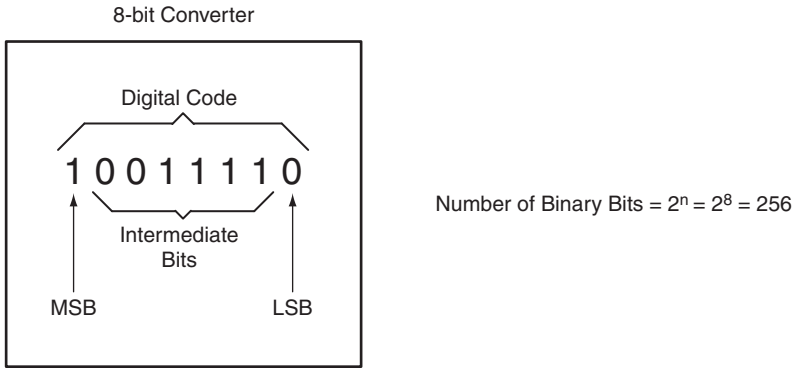


Figure 14.2: Significant bits versus binary bits.

$$\text{LSB} = \frac{\text{FSV}}{2^n} \tag{14.2}$$

FSV is the full scale voltage of the converter in volts; hence, a 14 bit converter FSV = 10 V has an LSB equal to $10/2^{12} = 2.441406$ mV/bit. In an ADC, an LSB is the maximum voltage change required to for a 1 bit output change; and in an ADC, an LSB is defined as LSB = FSV/$(2^n - 1)$.

Conversion speed is not critical in temperature measurement applications, because temperature changes occur at slow rates. Directional control in a rocket traveling at Mach 2 happens much faster than temperature changes, so conversion speed is an important factor in rocket applications. The speed of an ADC is generally thought of as the conversion time plus the time required between conversions, and conversion speed dictates the converter structure. When conversion speed is a primary specification, a flash converter is used, and flash converters require low impedance driving circuits. This is an example of a converter imposing a specification requirement, low output impedance, on the driving amplifier.

The system definition specifies the voltages available for design and the maximum available current drain. Some systems have multiple voltages available, and others are limited to a single voltage. The available voltage affects the converter selection. Size, processor compatibility, and interface structure are three more factors that must be considered when selecting the ADC. The available package that the converter comes in determines what footprint or size the converter takes on the printed circuit board. Some applications preclude large, power hungry ADCs, so these applications are limited to recursive or $\sum\Delta$ type ADCs. The converter must be compatible with the processor to preclude the addition of glue logic; so the processor dictates the ADC's structure. This defines the interface structure, sometimes the ADC structure, and the ADC timing.

Note that the amplifier designer has not been consulted during this decision process, but, in actuality, the systems engineers do talk to the amplifier designers, if only to pacify them. The selection of the ADC is out of the circuit designer's hands; so the circuit designer must accept what the application demands.

Many different transducer/ADC combinations are possible, and each combination has a different requirement. Although they may be natural enemies, any transducer may be coupled with any ADC, therefore the amplifier must make the coupling appear to be seamless. There is no reason to expect that the selected transducer's output voltage span

matches the selected ADC's input voltage span, so an amplifier stage must match the transducer output voltage span to the ADC input voltage span. The amplifier stage amplifies the transducer output voltage span and shifts its DC level until the transducer output voltage span matches the ADC input voltage span. When the spans are matched, the transducer/ADC combination achieves the ultimate accuracy; any other condition sacrifices accuracy or dynamic range.

The transducer output voltage span seldom equals the ADC input voltage span. Transducer data are lost or the ADC dynamic range is not fully utilized when the spans are unequal, start at different DC voltages, or both. In Figure 14.3(A), the spans are equal (3 V), but they are offset by 1 V. This situation requires level shifting to move the sensor output voltage up by 1 V so the spans match. In Figure 14.3(B), the spans are unequal (2 V and 4 V), but no offset voltage exists. This situation requires amplification of the sensor output to match the spans. When the spans are unequal (2 V versus 3 V) and offset (1 V), as is the case in Figure 14.3(C), level shifting and amplification are required to match the spans.

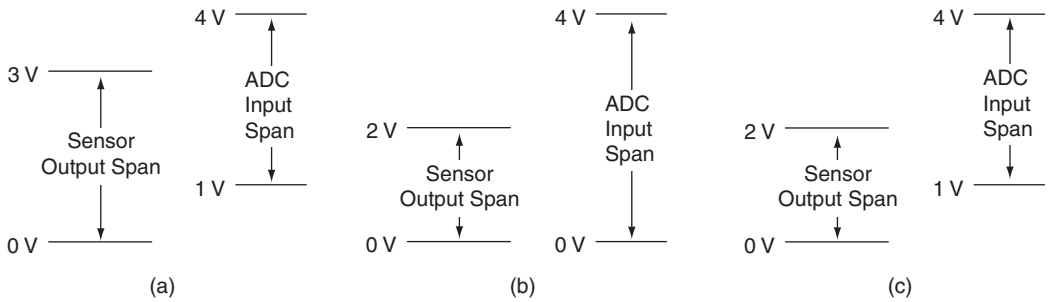


Figure 14.3: Example of spans that require correction.

The output span of the transducer must be matched to the input span of the ADC to achieve optimum performance. When the spans are mismatched, either the transducer output voltage does not fit into the ADC input span, hence losing sensor data, or the transducer output voltage does not fill the ADC input span, losing ADC accuracy. The latter situation requires an increase in ADC dynamic range (increased cost), because a higher bit converter must be used to achieve the same resolution. The best analog circuit

available for matching the spans is the op amp because it level shifts and amplifies the input voltage to make the spans equal. The op amp is so versatile that it shifts the signal's DC level and amplifies the input signal simultaneously.

A similar but different problem exists in the digital to analog converter (DAC) to actuator interface. The DAC output voltage or current span must match the actuator input voltage span to achieve maximum performance. The procedure for matching the DAC output span to the actuator input span can be quite different from the procedure for matching the transducer output span to the ADC input span. Transducer outputs are usually low level signals, so care must be taken to preserve their signal to noise ratio. Actuator input signals may require significant power, so robust op amps are required to drive some actuators.

The system specifications eventually determine the transducer, ADC, and analog circuit specifications. System specifications are seen as absolute specifications; they must be met for the design to function in a satisfactory manner. Component specifications are divided into several categories; absolute maximum ratings (AMRs), guaranteed minimum/maximum specifications (V_{MAX} or V_{MIN}), typical specifications (V), and guaranteed but not tested (GNT) specifications.

If any of the device parameters is taken beyond the AMR, the device can be destroyed (expect destruction). The manufacturer guard bands the AMR to guarantee safety and quality, and you should guard band the AMRs, too. Typical specifications are the most appealing, but throw them out because they are meaningless in most cases. In the vast majority of cases, the typical specifications are not related to meaningful data; rather, they are marketing dreams. Never design with typical specifications unless you are in the habit of designing with meaningless data or have a good reason for believing that the typical specification is close to reality. A violation of this rule is a specification, like output voltage swing, that depends heavily on test conditions, such as the value of the load resistor. When the load resistance is much higher than that specified for the test condition, the output voltage swing is closer to the typical specification rather than the guaranteed specification. The laws of physics guarantee this truth, but the amount of extra voltage swing achieved is hard to calculate.

Guaranteed minimum/maximum specifications define the limits of a parameter. The parameter always exceeds the minimum value and it never exceeds the maximum value. The guaranteed min/max specifications are your design specifications.

Guaranteed but not tested specifications are usually applied to parameters that are very expensive to test. The manufacturer either tests some other parameter related to the specification or it sample tests each lot to ensure compliance. GNT specifications are design specifications. There is a fifth specification, called *guaranteed by design* (GBD); and if they are not critical specifications, GBD is a useful design specification.

All specifications have conditions associated with testing. They specify ambient temperature, supply voltage, test signals, test loads, and other conditions; and they define how the measurements are made. Inspect the test conditions carefully; an op amp that specifies a 5 V output swing with a 50 Ω load is much more capable of driving a load than an op amp that specifies a 5 V output swing with a 10 kΩ load. Beware, you assume the risk of a parameter being out of specification when you use devices at conditions other than the test conditions.

An error budget is a logical and orderly method of tabulating errors, and it helps the designer keep track of the errors by error sources. Meeting the system specifications translates into minimizing errors, choosing components with acceptable errors and canceling or eliminating errors when possible. The error budget is first applied to the ADC and transducer because they are the components over which the designer has the least control. When these two error budgets are combined and subtracted from the system error allowance, the result is the error allowance for the amplifier and peripheral circuits. The designer must choose components and design wisely to stay within the error allowance, or the system specifications are not met.

Sometimes the systems specifications can't be met, and this fact is greeted with moans, name calling, and finger pointing. The error budgets are the design engineer's only defense against subjective accusations. The error budgets document the design trail, and they show where changes need to be made to do the best job possible. It is very hard to maintain an error budget, because errors must be converted to equivalent units (volts, bits, or amps) and the impact of the error term may not be calculable at that point in the design. When this situation occurs, tabulate the error terms in a table and calculate their effect later in the design process.

This chapter teaches the designer how to characterize the transducer and ADC, how to determine amplifier and design specifications through the use of error budgets, and how to complete circuit design. The equations developed in this chapter are not nearly as important as the design philosophy.

14.2 Transducer Types

This is not a treatise on transducers, but an appreciation for the many types of transducers gives a feel for the extent and complexity of the transducer characterization problem (following section). The variety of electrical output that they offer loosely groups transducers. Various types of transducer outputs are resistive, optical, AC excited, junction voltage, and magnetic; and each of these outputs must be converted to an electrical signal that can be amplified to fit the input span of an ADC. There are excellent references (such as [1]) that deal with transducer characterization, but the transducer manufacturer should be your first source of reference material.

Transducer manufacturers publish data similar to that contained in an IC data sheet, and they take the same liberties with typical specifications as the IC manufacturers. Sort through the data to determine the meaning of the various specifications, then pay special attention to the test conditions that prevailed when the data were gathered. Look for application notes that show transducer excitation, bias, or interface circuits. Search several manufacturers for similar information because nobody manages to cover every aspect of a design.

Some transducers, such as strain gauges, thermistors, RTDs, and potentiometers, sense a change in resistance (ΔR). The ΔR sensing devices are used in at least three circuit configurations: the voltage divider, current excited, and Wheatstone bridge circuits shown in Figures 14.4, 14.5, and 14.6. The transducer resistance is R_T, and the change in transducer resistance caused by a change in the measured variable is ΔR.

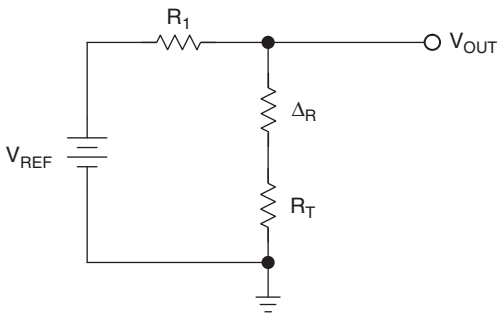


Figure 14.4: Voltage divider circuit for a resistive transducer.

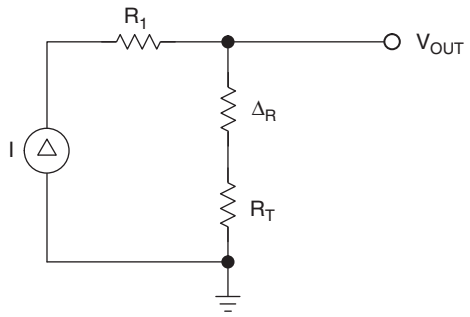


Figure 14.5: Current source excitation for a resistive transducer.

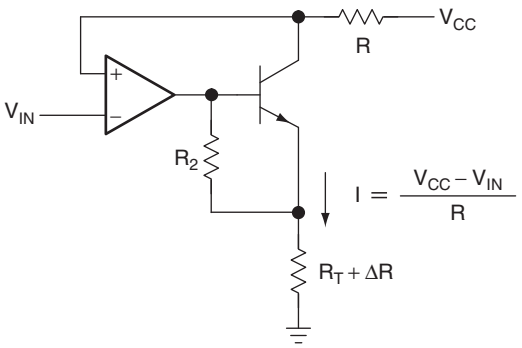


Figure 14.6: Precision current source.

The voltage divider circuit uses a stable reference voltage to convert the transducer resistance into voltage, and its output voltage is given in Equation (14.3):

$$V_{\text{OUT}} = V_{\text{REF}} \frac{\Delta R + R_T}{\Delta R + R_T + R_1} \tag{14.3}$$

If R_1 is comparable in value to R_T, the circuit has very low sensitivity because the circuit must measure a small change in resistance in the presence of a large resistance. When the bias resistor, R_1, is selected as a large value, V_{REF} and R_1 act as a current source and the transducer resistance can be neglected in the calculations,

yielding Equation (14.4). When $R_1 \gg (R_T + \Delta R)$ Equation (14.3) reduces to Equation (14.4):

$$V_{\text{OUT}} = \frac{V_{\text{REF}}}{R_1}(\Delta R + R_T) \tag{14.4}$$

Equation (14.5) is the equivalent of Equation (14.4), and it is obtained by exciting the transducer with a bias current as shown in Figure 14.5. The bias current can be made very accurate by employing op amps in a current source configuration, as shown in Figure 14.6; therefore the approximation $R1 \gg (R_T + \Delta R)$ need not enter the calculations:

$$V_{\text{OUT}} = I(\Delta R + R_T) \tag{14.5}$$

The Wheatstone bridge shown in Figure 14.7 is a precision device used to measure small changes in resistance. One leg of the bridge is made up of a voltage divider consisting of equal stable resistors (R_1 and R_2) and the reference voltage. When R_X and ΔR equal zero, R_{TX} is selected equal to R_T. As the transducer resistance changes, ΔR assumes some value, and R_X is switched until the bridge output voltage nulls to zero. At this point, the value of ΔR is read from the R_X dial. Bridge circuits are used to convert resistive transducer values to dial readings, but some methods of using transducers in bridge circuits yield a voltage change proportional to the resistance change. The bridge circuit has a high output impedance, so op amps configured in an instrumentation configuration (both inputs are equal, high resistances) must be used to amplify the output voltage from bridge circuits.

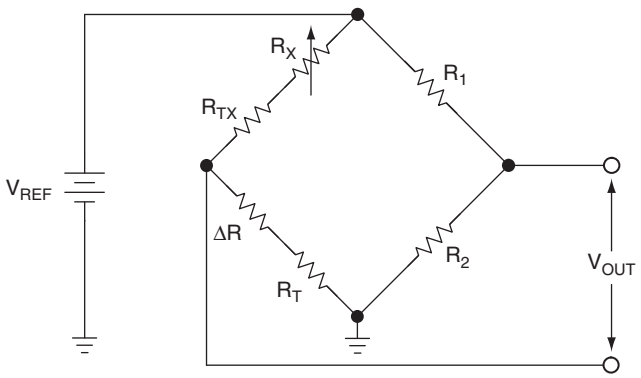


Figure 14.7: Wheatstone bridge circuit.

The three most popular optical transducers are the photoconductive cell, the photodiode, and the photovoltaic cell. The photoconductive cell acts like a light sensitive resistor, so one of the circuits shown in Figure 14.4, 14.5, or 14.7 that converts resistance changes to voltage is used in photoconductive cell applications. The photodiode is a very fast diode with a small output current, and the circuit shown in Figure 14.8 is used to convert current to voltage. The photodiode is reversed biased with a constant voltage, so the photodiode terminating voltage stays constant, thus maintaining linearity. The photodiode amplifier output voltage equation is Equation (14.6):

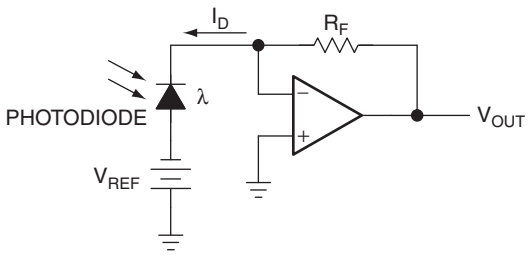


Figure 14.8: Photodiode amplifier.

$$V_{\text{OUT}} = I_D R_F \tag{14.6}$$

The phototransistor has a junction that is light sensitive, and the junction has a transparent cover so that it can sense ambient light. The collector base junction of the transistor is reverse biased, and normal transistor action takes place with the ambient light induced base current taking the place of the normal base current (see Figure 14.9).

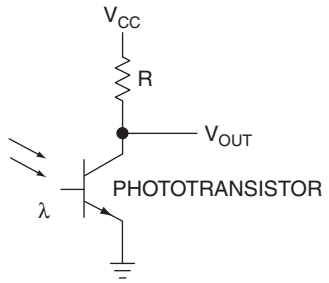


Figure 14.9: Phototransistor amplifier.

The photovoltaic or solar cell circuit is shown in Figure 14.10. The circuit zero biases the cell for minimum leakage current, and the cell's output current is a linear function of the area exposed to light. When the photovoltaic cell is properly masked and evenly flooded with light, it operates as a linear distance transducer, see Figure 14.10 and Equation (14.6).

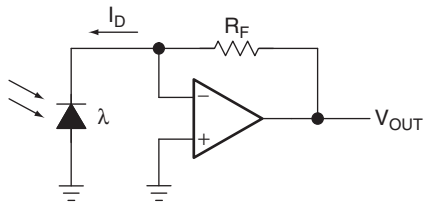


Figure 14.10: Photovoltaic cell amplifier.

AC excited transducers are usually used to make motion or distance sensors. In one type of AC excited transducer, a stationary winding is excited with an AC current and another winding is moved past the stationary winding, inducing a voltage in the second winding. In a well designed transducer, the induced voltage is proportional to distance, hence the output voltage is proportional to distance. Another AC excited transducer uses two plates: One plate is excited with an AC current, and the other plate is ground. An object coming near the excited plate changes the capacitance between the plates, and the result is an output voltage change.

Resolvers and synchros are position transducers that indicate position as a function of the phase angle between the exciting signal and the output signal. Resolvers and synchros normally are multiple winding devices excited from two or more sources. They indicate position very accurately, but their special circuitry requirements, cost, and weight limit them to a few applications such as airfoil control surfaces and gyros.

AC excited transducers require a rectifier circuit to make the output voltage unipolar prior to integration. Coarse transducers use a diode or diode bridge to rectify the output voltage, but diodes are not adequate for precision applications, because their forward voltage drop is temperature sensitive and poorly regulated. The diode problems are overcome through the use of feedback in the active full wave rectifier circuit shown in Figure 14.11. An integrating capacitor, *C*, is added to the circuit so the output voltage is a DC voltage proportional to the average voltage value of the input voltage.

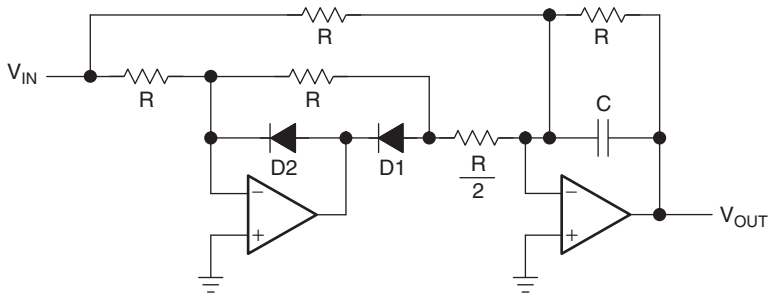


Figure 14.11: Active full wave rectifier and filter.

Semiconductor or wire junctions (thermocouples) are often used as temperature transducers because there is a linear relationship between temperature and output voltage over a restricted temperature range. Thermocouples have small voltages, varying from microvolt per degree Centigrade to millivolt per degree Centigrade, and they normally are configured with thermistors and zeroing resistors in the output circuit. Thermocouples have small output voltages and high output resistance, so a special op amp, called an *instrumentation amplifier*, is required for thermocouple amplification. An instrumentation amplifier has very high and equal input impedances, thus they don't load the input signal source.

Semiconductor junctions have a nominal temperature coefficient (TC) of -2 mV/°C. The TC is linear, but it varies from diode to diode because of manufacturing techniques, semiconductor materials, and bias currents. In a well controlled application, where thermal mass is insignificant, semiconductor junctions make excellent temperature transducers. The junction effect is so stable and linear that commercial temperature transducers have become available in a single IC.

Magnetic fields can be sensed by the Hall effect and special semiconductors called *Hall effect sensors* have been developed to sense magnetic fields. Current is passed through the semiconductor in a direction perpendicular to the magnetic field. A pair of voltage pick off leads is placed perpendicular to the direction of current flow, and the output voltage is proportional to the magnetic field strength. The manufacturing process for Hall effect transducers is a standard semiconductor manufacturing process, so Hall effect transducers are offered for sale as transistors or ICs.

14.3 Design Procedure

A step by step design procedure that results in the proper op amp selection and circuit design follows. This design procedure works best when the op amp has almost ideal performance, so the ideal op amp equations are applicable. When nonideal op amps are used, parameters like input current affect the design, and they must be accounted for in the design process. The latest generation of rail to rail op amps makes the ideal op amp assumption more valid than it ever was.

No design procedure can anticipate all possible situations; and depending on the op amp selected, procedure modifications may have to be made to account for op amp bias current, input offset voltage, or other parameters. This design procedure assumes that system requirements have determined the transducer and ADC selection and changing these selections adversely affects the project.

1. Review the system specifications to obtain specifications for noise, power, current drain, frequency response, accuracy, and other variables that might affect the design.
2. Characterize the reference voltage including initial tolerances and drift.
3. Characterize the transducer to determine its salient parameters, including output voltage swing, output impedance, DC offset voltage, output voltage drift, and power requirements. These parameters determine the op amp's required input voltage range (V_{IN1} to V_{IN2}) and input impedance requirements. The offset voltage and voltage drift are tabulated as errors. At this point, it is assumed that the selected op amp's input voltage span is greater than the transducer's output voltage excursion. Design peripheral circuits if required.
4. Scrutinize the ADC's specification sheet to determine its required input voltage range, because this range eventually sets the op amp's output voltage swing requirement (V_{OUT1} to V_{OUT2}). Determine the ADC's input resistance, input capacitance, resolution, accuracy, full scale range, and allowable input circuit charge time. Calculate the LSB value.
5. Create an error budget (in bits) for the transducer and ADC. Use the transducer/ADC error budget to determine the value and range of the critical op amp parameters. Select an op amp, and justify the selection by creating an error budget for the op amp circuit.

6. Scan the transducer and ADC specifications, and make a set of analog interface amplifier specifications
7. Complete the AIA circuit design.
8. Build the circuit, and test it.

14.4 Review of the System Specifications

The power supply has only one voltage available, and that voltage is 5 V ± 5% = 5 V ± 250 mV. The power supply is connected with the negative terminal at ground and the positive terminal at V_{CC}. This is not a portable application, therefore the allowed current drain, 50 mA, is adequate for the job. No noise specifications are given, but the proposed power, ground, and signal traces are being done on high quality circuit board material with planes and good size copper. A system of this quality should experience no more than 50 mV of noise on the logic power lines and 10 mV of noise on the analog power lines.

This is a temperature measuring system that requires updates every 10 s. Clearly, ADC conversion speed or input charging rate is not cause for consideration. The low conversion speed translates into lower logic speed, and slow logic means less noise generated. The temperature transducer is located at the end of a 3 ft long cable, so expect some noise picked up by the cable to be introduced into the circuit. Fortunately, the long time between ADC conversions enable extensive filtering to reduce the cable noise.

The system accuracy required is 11 bits. The application measures several parameters, so it is multiplexed, and a TLV2544 12 bit resolution ADC has been selected. The temperature transducer is a diode, and the temperature span to be measured is −25°C to 100°C. The ambient temperature of the electronics package is held between 15°C to 35°C.

14.5 Reference Voltage Characterization

A reference voltage is required to bias the transducer and act as a reference voltage for the analog interface amplifier (AIA). Selecting a reference with a total accuracy better than the accuracy specification (11 bits) does not guarantee meeting the system accuracy specification, because other error sources exist in the design. Resistor tolerances, amplifier tolerances, and transducer tolerances all contribute to the

inaccuracy, and the reference can't diminish these errors. The quandary here is a choice between an expensive reference and expensive accurate components or an adjustment to null out initial errors. This quandary boils down to which is the lesser of two evils: expensive components or the expense of an adjustment.

System engineering has decided that it wants the adjustment, so the reference need not have 11 bit accuracy. A TL431A voltage reference is chosen for the design. The output voltage specification at 25°C and 10 mA bias current is 2495 mV ± 25 mV. This reference has a temperature drift of 25 mV over 70°C, and this translates to 7.14 mV drift over a 20°C temperature range. Another drift is caused by the cathode voltage change, and this drift is 2.7 mV/V. The supply voltage regulation is 0.5 V, but much of this tolerance is consumed by the initial tolerance and wiring scheme, so the less than 0.1 V is due to regulator drift. The total drift is 7.14 mV + 0.27 mV = 7.41 mV. This yields a total drift of 0.3% maximum. The amplifier usually uses a fraction of the reference voltage, so the final AIA does not drift the full 0.3%.

14.6 Transducer Characterization

The temperature transducer is a special silicon diode characterized for temperature measurement work. When this diode is forward biased at 2.0 mA ± 0.1 mA, its forward voltage drop is 0.55 V ± 50 mV and its temperature coefficient is −2 mV/°C. The wide acceptable variation in bias current makes this an easy device to work with. The circuit for the bias calculations is shown in Figure 14.12.

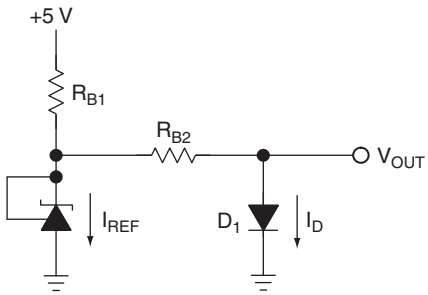


Figure 14.12: Reference and transducer bias circuit.

The current through R_{B1} is calculated in Equation (14.7). Remember, the reference must be biased at 10 mA and the transducer must be biased at 2 mA.

$$I = I_{\text{REF}} + I_D = 10 + 2 = 12 \text{ mA} \tag{14.7}$$

The value of R_{B1} is calculated in Equation (14.8), and the value of R_{B2} is calculated in Equation (14.9):

$$R_{B1} = \frac{V_{+5} - V_{\text{REF}}}{I} = \frac{5 - 2.495}{12} = 208\ \Omega \tag{14.8}$$

$$R_{B2} = \frac{V_{\text{REF}}}{I_D} = \frac{2.495}{2} = 1247\ \Omega \tag{14.9}$$

Both resistors are selected from the list of 1% decade values, therefore $R_{B1} = 210\ \Omega$, 1%, and $R_{B2} = 1240\ \Omega$, 1%. The resistor values have been established, so it is time to calculate the worst case excursions of I_D, Equations (14.10) and (14.11). The resistors are assumed to have a 2% tolerance in these calculations. The extra 1% allows for temperature changes, vibration, and life. Three percent tolerances would have been used if the electronics' ambient temperature range were larger.

$$I_{D(\text{MIN})} = \frac{V_{\text{REF(MIN)}}}{\text{R}_{B2(\text{MAX})}} = \frac{2.47 - 0.025 - 0.007}{1.02\ (1.24)} = 1.93 \text{ mA} \tag{14.10}$$

$$I_{D(\text{MAX})} = \frac{V_{\text{REF(MAX)}}}{R_{B2(\text{MIN})}} = \frac{2.52 - 0.025 - 0.007}{0.98\ (1.24)} = 2.10 \text{ mA} \tag{14.11}$$

The bias current extremes do not exceed the transducer bias current requirements, so the transducer meets the specifications advertised. The converter is 12 bits and the full scale voltage is assumed to be 5 V, so the value of an LSB is calculated in Equation (14.12). The nominal transducer output voltage is 550 mV at an ambient temperature of 25°C. At −25°C, the transducer output voltage is 550 mV + (−2 mV/°C)(−50°C) = 650 mV. At 125°C, the transducer output voltage is 550 mV + (−2 mV°C)(75°C) = 400 mV. These data are tabulated in Table 14.1.

Table 14.1: Transducer Output Voltage

Transducer temperature	Transducer output voltage	Analog interface amplifier input voltage
−25°C	650 mV	$V_{IN1} = 650$ mV
25°C	550 mV	550 mV
100°C	400 mV	$V_{IN2} = 400$ mV

$$\text{LSB} = \frac{\text{FSV}}{2^N} = \frac{5}{2^{12}} = 1.22 \text{ mV} \tag{14.12}$$

The steady state (V_{TOS}) offset voltage is ±50 mV, so transducer output voltage (V_{TOV}) ranges from 350 mV to 700 mV. The offset voltage is stripped out by the adjustments in the AIA, so it is not of any concern here. V_{TOS} spans 100 mV, so it is a 100 mV/1.22 mV/bit = 82 bit error unless it is adjusted out.

The output impedance of the transducer is equivalent to the resistance of a forward biased diode, Equation (14.13):

$$R_D = \frac{26}{I} = \frac{26}{2} = 13\ \Omega \tag{14.13}$$

At this stage of the design, two parameters influence the accuracy of the measurement: the temperature coefficient of the transducer and the output impedance of the transducer. The temperature transducer has been biased correctly, so its temperature coefficient should be the advertised value of −2 mV/°C. The output impedance of the transducer forms a voltage divider with the input resistance of the AIA, but this error can't be calculated until the AIA is selected. The final transducer error contribution is that portion of the V_{TOS} that can't be adjusted out, and this error is determined during the AIA design.

14.7 ADC Characterization

This particular ADC was selected because it has a multiplexer and it enables modes of operation. The temperature measurement is done in the single shot mode because this mode allows the user to set the charge time at the input to the converter. During charging, the ADC's input resistance is low, but after the ADC input is charged, the

input resistance rises to 20 kΩ. This high input resistance does not load the AIA output circuit, so the AIA achieves full rail to rail output voltage swing.

The internal reference is used in this application, and the reference sets the input voltage span required to obtain full accuracy for the ADC. Using the internal reference, the input voltage span is 0 V to 4 V. The offset voltage (V_{ADCOS}) is ±150 mV, and the voltage drift is 40 PPM/°C. The voltage drift over the full temperature range is 40 PPM/°C(20°C) = 800 PPM. A 14 bit converter has 244 PPM/LSB, so the drift voltage error is 800/244 ≈ 4 bits error.

The ADC output is full scale (all bits 1) when the input voltage is 4 V, and it is zero (all bits 0) when the input voltage is 0 V. These data are tabulated in Table 14.2. Because the full scale output voltage has changed to 4 V, the LSB is calculated to be $4/(2^{12}) = 976.6$ μV/bit.

Table 14.2: ADC Input Voltage

ADC input voltage	Digital output	Analog interface amplifier output voltage
0 V	000000000000	$V_{OUT1} = 0$ V
4 V	111111111111	$V_{OUT2} = 4$ V

14.8 Op Amp Selection

It is time to select the op amp, and the easiest way to do this is to list the known specifications or requirements, list a candidate op amp's specifications, and calculate the projected error that the candidate op amp yields (Table 14.3).

There should be almost no error from R_{IN}, because the transducer output impedance is very low. The high side of the op amp's output voltage swing (4.85 V) is much higher than the ADC input voltage (4 V). The low side of the op amp's output voltage swing (0.185 V) is less than the ADC input voltage swing (0 V). The ADC input circuit is 20 kΩ, and that doesn't load the op amp output stage, so the op amp output voltage swing is very close to the ADC input voltage range. R_{OUT} should present no problems acting as a voltage divider with the ADC input resistance. V_{OS} and I_{IB} create offset voltages that add to the reference offset voltage, and they have to be adjusted out as a group. The system noise overshadows the op amp noise, so the op amp noise is accepted unless later calculations prove otherwise.

Table 14.3: Op Amp Selection

Design specification	Estimated value	Candidate op amp: TLV247X
R_{IN}	10^6 (13) Ω	1012 Ω
V_{TOV}	350 mV to 700 mV	–0.2 V to 5.2 V
R_{OUT}		1.8 Ω
V_{INADC}	0 V to 4 V	0.15 V to 4.85 V
V_{OS}	–	2.2 mV
I_B	–	100 pA
V_N	–	28 nV/$\sqrt{\text{Hz}}$
I_N	–	0.39 pA/$\sqrt{\text{Hz}}$
Analog noise	–	10 mV
k_{SVR}	–	63 dB

14.9 Amplifier Circuit Design

Enough information exists for the AIA to be designed. The TLV247X op amp is selected because it meets all the system requirements. The first step in the design is to determine the AIA input and output voltages, and this has already been done. These voltages are taken from Tables 14.1 and 14.2 and repeated here as Table 14.4.

Table 14.4: AIA Input and Output Voltages

Input voltage	Output voltages	
$V_{IN1} = 650$ mV	$V_{OUT1} = 0$ V	First pair of data points
$V_{IN2} = 400$ mV	$V_{OUT2} = 4$ V	Second pair of data points

The equation of an op amp is the equation of a straight line, as given in Equation (14.14):

$$Y = mX + b \tag{14.14}$$

The two pairs of data points shown in Table 14.4 are substituted in Equation (14.14), making Equations (14.15) and (14.16):

$$4 = 0.4m + b \tag{14.15}$$

$$0 = 0.65m + b \tag{14.16}$$

Equation (14.15) is solved and substituted into Equation (14.16) to obtain Equation (14.17):

$$4 = 0.4\left(\frac{-b}{0.65}\right) + b \tag{14.17}$$

Solving Equation (14.17) yields $b = 10.4$, and solving Equation (14.15) yields $m = -16$. Substituting these values back into Equation (14.14) yields Equation (14.18), and Equation (14.18) (the final equation for the AIA) is put in electronic terminology:

$$V_{OUT} = -16\,V_{IN} + 10.4 \tag{14.18}$$

The circuit that yields the transfer function developed in Equation (14.18) is shown in Figure 14.13.

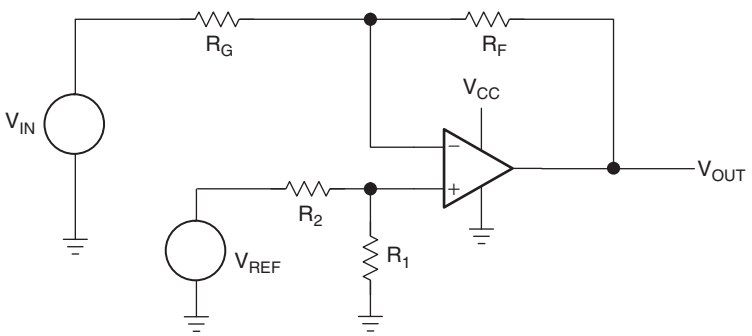


Figure 14.13: AIA circuit.

The equations for the AIA circuit follow:

$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_G}\right) + V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{14.19}$$

$$|m|\frac{R_F}{R_G} \tag{14.20}$$

$$b = V_{REF}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{14.21}$$

Equation (14.18) gives the value for m as 16, and using Equation (14.20) yields $R_F = 16R_G$. Select $R_F = 383$ kΩ and $R_G = 23.7$ kΩ, because they are standard 1% resistor values, and this yields $m = 16.16$. The resistors R_1 and R_2 are calculated with the aid of Equations (14.22) and (14.23):

$$\frac{R_1}{R_1 + R_2} = \frac{b}{V_{REF}}\left(\frac{R_G}{R_F + R_G}\right) = \frac{10.4}{2.495}\left(\frac{23.7}{23.7 + 383}\right) = 0.2424 \tag{14.22}$$

$$R_1 = \frac{0.2424}{0.7576}R_2 = 0.32R_2 \tag{14.23}$$

The parallel combination of R_1 and R_2 should equal the parallel combination of R_F and R_G, so that the input voltage offset caused by the op amp input current is canceled. Select $R_2 = 105$ kΩ and $R_1 = 33.2$ kΩ, because they are standard 1% values, then $b = 10.3$. The value of the parallel combination of R_1, R_2 ($R_1 \| R_2 = 25.22$ kΩ) almost matches the value of the parallel combination of R_F, R_G ($R_F \| R_G = 22.3$ kΩ), and this is an adequate match for input current cancelation. The downsides of selecting large resistor values for RF are current noise amplification, increased resistor noise, smaller bandwidth because of stray capacitance, and increased offset voltage due to input current. Bandwidth clearly is not a factor in this design. The op amp input current is 100 pA, so it won't cause much offset with a 383 kΩ feedback resistor (38.3 μV). The noise current and voltage are calculated later when the error budget is made.

The gain, m, and the intercept, b, are not accurate, because the exact resistor values were not available in the 1% resistor selection chart. This is a normal situation; and in less demanding designs, the small error either does not matter or is corrected someplace

else in the signal chain. That error is critical in this design, so it must eliminated. Several nondrift type errors have accumulated up to this point, and now is the time to correct all the nondrift errors with the addition of adjustments. Two adjustments are used: one adjustment controls the gain, m, and the other controls the intercept, b. The value of the adjustable resistor must be large enough to deliver an adequate adjustment range, but any value larger than that decreases the adjustment resolution.

The data that determine the adjustment range required are tabulated in Table 14.5. Drift and gain errors are calculated in volts, but drift errors are calculated in bits because they are not eliminated by adjustments. Remember, an LSB for this system is 4/4096 = 976.6 μV/bit.

Table 14.5: Offset and Gain Error Budget

Error parameter	Intercept	Gain	Drift
V_{REF}	±25 mV		
V_{REF} drift			7.41 mV ≈ 8 LSB
Transducer offset		±50 mV	
Transducer R_{OUT}			13 Ω ≈ 0 LSB
ADC reference		±150 mV	1 LSB
Total unadjusted ADC error			2 LSB
Gain error		1.6 LSB	
ADC drift			4 LSB
V_{OS} op amp	2.2 mV		
I_B op amp	100 pA		
V_N op amp			28nV/$\sqrt{\text{Hz}}$ ≈ 1 LSB
I_N op amp			139pA/$\sqrt{\text{Hz}}$ ≈ 0 LSB
V_{NPS} PS noise			10 mV ≈ 2 LSB
R_{OUT} op amp			1.8 Ω ≈ 0 LSB
$V_{OUT\ LOW}$ op amp			70 mV ≈ 72 LSB
Total error			18 LSB

The adjustment for the intercept, b, depends on R_1, R_2, and V_{REF}. This adjustment has to account for the reference offset, the op amp input voltage offset, the op amp input current, and the resistor tolerances. The offset voltage inherent in the reference is given as ±25 mV. The op amp input offset voltage is 2.2 mV; usually op amp offset voltage calculations include multiplying this offset by the closed loop gain, but this isn't done because the offset voltage is adjusted out in the input circuit. The op amp input current is converted to a common mode voltage by the parallel combination of the reference resistors, so it is neglected in this calculation.

The worst case reference input voltage for the op amp, $V_{REF(MIN)}$, is calculated in Equation (14.24), where the resistor tolerances are assumed to be 3% and the reference voltage error is 50 mV:

$$\begin{aligned} V_{REF(MIN)} &= (V_{REF} - 50\text{ mV})\frac{0.97R_1}{0.97R_1 + 1.03R_2} \\ &= (2.495 - 0.05)\frac{0.97(33.2)}{0.97(33.2) + 1.03(105)} = 0.566\text{ V} \end{aligned} \tag{14.24}$$

The nominal reference voltage at the op amp input is 0.6 V, so the reference voltage has to have about 40 mV adjustment around the nominal, or a total adjustment range of 80 mV. The nominal current through the voltage divider is $I_{DIVIDER} = [2.495/(105 + 33.2)]\ \text{k}\Omega = 0.018$ mA. A 4444 kΩ resistor drops 80 mV, so the adjustable resistor (a potentiometer) must be greater than 4444 kΩ. Select the adjustable resistor, R_{1A}, equal to 5 kΩ because this is an available potentiometer value, and the offset adjustment is ±45 mV. Half of the potentiometer value is subtracted from R_1 to yield R_{1B}, and this subtraction centers the adjustment about the nominal value of 0.6 V. $R_{1B} = 33.2\ \text{k}\Omega - 2.5\ \text{k}\Omega = 30.7\ \text{k}\Omega$. Select R_{1B} as 30.9 kΩ.

The adjustment for the gain employs R_F and R_G to ensure that the gain can always be set at the value required to ensure that the transducer output swing fills the ADC input range. The gain equation, Equation (14.18), is algebraically manipulated, worst case values are substituted for m and b, and it is presented as Equation (14.25):

$$G = \frac{V_{OUT} - 10.4}{-V_{IN}} = \frac{3.85 - 10.4}{-0.35} = 18.71 \tag{14.25}$$

Equation (14.26) is Equation (14.20) with 3% resistor tolerances:

$$0.97R_F = 18.71(1.03R_G) \tag{14.26}$$

Doing the arithmetic in Equation (14.26) yields $R_F = 19.86R_G$. Therefore, on the high side, the gain must go from 16 to 19.86, or it must increase by 3.86. Assuming that the low side gain variation is equal and rounding off to 4 sets the gain variation from 12 to 20. When $R_G = 23.7$ kΩ, R_F varies from 284.4 kΩ to 474 kΩ. R_F is divided into a potentiometer $R_{FA} = 200$ kΩ and $R_{FB} = 280$ kΩ, thus the nominal gain can be varied from 11.8 to 20.2 (see Figure 14.14).

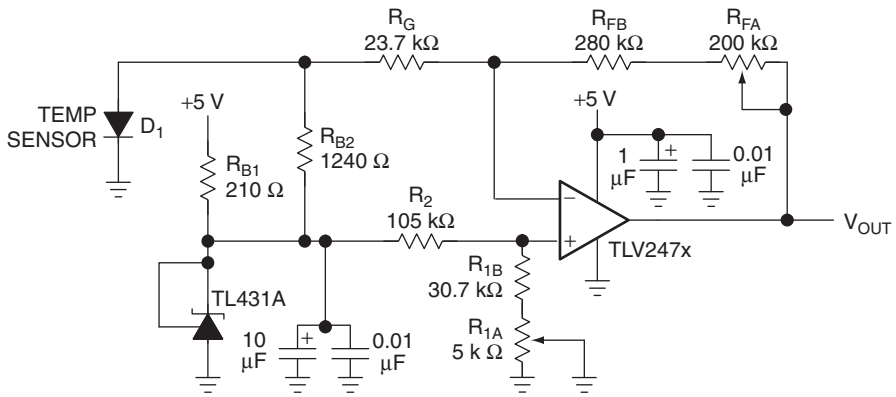


Figure 14.14: Final analog interface circuit.

There is no easy method of setting two interacting adjustments, because when the gain is changed, the offset voltage changes. They quickest method of adjustment is to connect the transducer to the circuit, adjust the offset, then adjust the gain. It takes several series of adjustments to get to the point where the both parameters are set correctly.

The impedance and noise errors are calculated prior to completing the error budget. The op amp input impedance works against the transducer output impedance to act like a voltage divider. The value of the voltage divider is calculated in Equation (14.27); and

as Equation (14.27) indicates, the output resistance of the transducer is negligible compared to the input resistance of the op amp. This is not always the case!

$$V_D = V_T \frac{R_{\text{IN}}}{r_C + R_{\text{IN}}} = V_T \frac{10^6}{13 + 10^6} \approx V_T \tag{14.27}$$

The ADC input impedance works against the op amp output impedance to act like a voltage divider. The value of the voltage divider is calculated in Equation (14.28). The voltage divider action introduces about a 0.009% error into the system, and this is within 13 bit accuracy, so it can be neglected.

$$V_{\text{IN}} = V_{\text{OUT}} \frac{20(10^3)}{1.8 + 20(10^3)} = \frac{20}{20.0018} = 0.99991\ V_{\text{OUT}} \tag{14.28}$$

The noise specification is given in nV/(Hz$^{0.5}$), and this must be converted to volts. Involved formulas are used for the conversion, but the simplest thing to do is assume the noise is wideband. If the numbers add up to a significant error, detailed calculations have to be made. The voltage noise is multiplied by the closed loop gain, therefore $V_{\text{NWB}} = V_N(G_{\text{MAX}}) = 28$ nV(20) = 560 nV = 0.56 μV. The current noise is multiplied by the parallel combination of R_F and R_G, so $I_{\text{NWB}} I_N(R_F \| R_G) = 139$ pA(22.5 kΩ) = 3.137 nV. The system noise is 10 mV, and this noise comes in through the inputs and the power supply. The power supply contribution is reduced by the power supply rejection ratio, and it is 10 mV/63 dB = 10 mV/1412 = 7.08 nV. This calculation assumes that high frequency noise is not a problem; but if this is not true, CMRR must be reduced per the data sheet CMRR versus frequency curves.

Some of the system noise propagates through the inputs and is rejected by the common mode rejection of the op amp. The op amp is not configured as a differential amplifier, so a portion of the closed loop gain multiplies some of the system noise.

The AC gain of the AIA is given in Equation (14.29):

$$\begin{aligned} V_{\text{OUT}} &= \alpha V_{\text{SN}} \left(\frac{R_1}{R_1 + R_2} \right) \left(\frac{R_F}{R_F + R_G} \right) - \alpha V_{\text{SN}} \frac{R_F}{R_G} \\ &= \alpha V_{\text{SN}} (4.12 - 16) = 11.8\ \alpha V_{SN} \end{aligned} \tag{14.29}$$

All of the system noise does not get in on the inputs, rather most of the system noise is found on the power supply. The fraction of the system noise that gets into the ground system and onto the op amp inputs is very small. This fraction, α, is normally about 0.01 because the power supplies are heavily decoupled to localize the noise. Considering this, the system noise is 1.18 mV, or less than 2 LSBs.

The op amp output voltage range does not include 0 V, and the ADC output voltage low value is 0 V, so this introduces another error. The guaranteed op amp low voltage is 185 mV at a load current of 2.5 mA. The output current in this design is 185 mV/20 kΩ = 9.25 μA. This output current approximates a no load condition, hence the nominal low voltage typical specification of 70 mV is used. This leads to a 72 LSB error, by far the biggest error.

Referring to Table 14.5, note that the total error is 90 LSB. Losing 90 LSBs out of 4096 total LSBs is approximately 11.97 bits accurate, so the 11 bit specification is met. The final circuit is shown in Figure 14.14.

Note that large decoupling capacitors have been added to the power supply and reference voltage. The decoupling capacitors localize IC noise, prevent interaction between circuits, and help keep noise from propagating. Two decoupling capacitors are used, a large electrolytic for medium and low frequencies and a ceramic for high frequencies. Although this portion of the design is low frequency, the op amp has a good frequency response, and the decoupling capacitors prevent local oscillations through the power lines. If cable noise is a problem, an integrating capacitor can be put in parallel with R_F to form a low pass filter.

14.10 Test

The final circuit is ready to build and test. The testing must include every possible combination of transducer input and ADC output to determine that the AIA functions in all manufacturing situations. The span of the adjustments, op amp output voltage range, and ADC input range must be checked for conformance to the design criteria. After the design has been tested for the specification limits, it should be tested for user abuse. What happens when the power supply is ramped up, turned on instantly, or something between these two limits? What happens when the inputs are subjected to overvoltage or the polarity is reversed? These are a few ideas to guide your testing.

14.11 Summary

The systems engineers select the transducer and ADC, and their selection criterion is foreordained by the application requirements. The AIA design engineer must accept the selected transducer and ADC, and it is the AIA designer's job to make these parts play together with adequate accuracy. The AIA design often includes the design of peripheral circuits, like transducer excitation circuits, and references.

The design procedure starts with an analysis of the transducer and ADC. The analysis is followed by a characterization of the transducer and reference. At this point, enough information is available to make an error budget and select candidate op amps. The op amp is selected in the next step in the procedure, and the circuit design follows.

The output voltage span of the transducer and corresponding input voltage span of the ADC are coupled as two pairs of data points that form the equation of a straight line. The data point pairs are substituted into simultaneous equations, and the equations are solved to determine the slope and intercept of a straight line (an op amp solution). The op amp circuit configuration is selected based on the sign of the slope and the intercept. Finally, the passive components used in the op amp circuit are calculated with the aid of the op amp circuit design equations.

The final circuit must be tested for conformance to the system specifications, but the prudent engineer tests beyond these specifications to determine the AIA's true limits.

Reference

1. Wobschall, Darold. (1979). *Circuit Design for Electronic Instrumentation*. New York: McGraw-Hill.

CHAPTER 15

Interfacing an Op Amp to an Analog to Digital Converter

15.1 Introduction

One of the most common questions asked by customers is, "Which op amp should I use with a given data converter?" The answer is enough to make a marketing engineer cringe, because it depends on the answers to many questions—way too many to be in the customer's comfort zone. Yet, the answers to these questions are not only necessary for the customer's design to be a success, they are questions that a customer must eventually answer.

It would be handy to have a table with A/D converters on one side and recommended op amps on the other. But this table will never exist—too many variables in system design affect the choice of op amp. The questions in this chapter help organize the designer's thoughts into the correct direction and define the issues. These questions are the ones that a designer should be prepared to answer, before committing to a design.

The list of questions may look daunting at the beginning, but they are divided into sections. This breaks up the system into component parts that surround the op amp and define exactly what that component needs to do. The completion of each section is a piece of the puzzle, and by the end of the process, the designer should have weeded out op amps that are unsuitable for the job.

Once the op amp has been selected, the job is not done. Some architectural considerations for the signal chain and trade-offs are associated with each one. A few of the most useful options are explored.

15.2 System Information

The overall characteristics of the system oftentimes yield valuable information. A clear understanding of the product and its function is imperative to design success:

- Exactly what is the end equipment and its application? Different systems have different requirements. For example, key concerns in a video system are completely different than those in a wireless communication system.
- In general terms, what is the function of this signal acquisition chain in the system? Where does the input signal come from and what happens to it once it is digitized?
- How many signal acquisition chains are used in the product? Channel density can influence system design in numerous ways, including space constraints, thermal requirements, and amplifier channel density per package.
- Will this signal chain be duplicated in other products? Is flexibility an advantage or can the design be narrowly focused on the task at hand?
- Is the design forced to adhere to a particular standard?
- Under what temperature conditions will the system operate; for example, –40°C to +85°C, 0°C to +70°C, +45°C to +55°C?
- Does the system have forced airflow from a fan to help with thermal dissipation?
- Is automatic gain control (AGC) functionality required? If so, is it digital or analog control? What is the gain range and so forth?
- Is a current solution unsatisfactory in some way? Why is the current solution unsatisfactory?

15.3 Power Supply Information

Power supply rails can quickly rule out amplifier solutions (Figure 15.1). This is similar to clothing shopping—the style may be desirable, but if the size doesn't fit, the style is useless. So a wise shopper finds the options in the size first, before becoming attached to a style. Similarly, an op amp with fantastic specifications at ±15 V may not

operate at all from a +3.3 V power supply. Power supply information is collected first, because it simply and unequivocally narrows the choices:

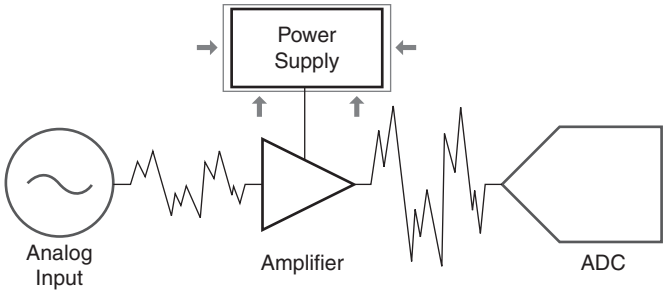


Figure 15.1: Focusing on the power supply characteristics.

- What is the power budget for the overall system? Is power a concern or is performance the ultimate goal?
- What power supply voltages are available in the design?
- Is there a preferred power supply voltage for the amplifier circuitry?
- Can an additional supply voltage be added if performance could be improved? Often, the best amplifier performance can be obtained with split supplies.
- Is a precision reference available in the system? In single supply systems, it is important to supply a virtual ground to the op amp circuitry. If the system already contains a reference, it may be possible to utilize it.
- Are there any special characteristics of the power supply? For example, is the power supply a switching power supply? Although op amps usually have excellent power supply rejection, it could be a concern in high resolution system. Any widely varying loads could also affect the op amp supply voltage.

15.4 Input Signal Characteristics

Understanding the input source (Figure 15.2) is key to properly designing the interface circuitry between the source and the analog to digital converter:

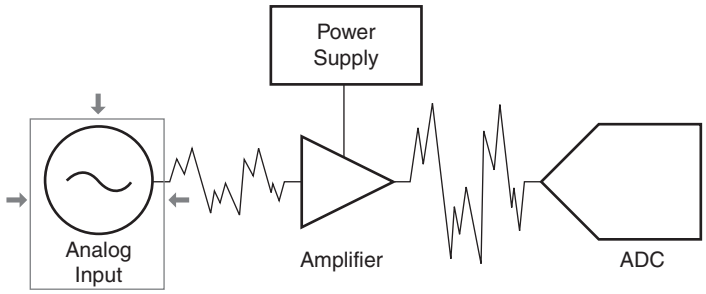


Figure 15.2: Focusing on the input signal.

- What is used for the signal source to the amplifier block in front of the ADC? Is it another amplifier, a sensor, or what?
- Describe the input signal. For example, is it continuous or discontinuous (i.e., pulsed)? The signal might be a QAM signal, an NTSC signal, a nonstandard continuous wave signal, a random analog signal, or some other signal.
- Are there any unusual characteristics of the signal source? Some sources have characteristics that affect the performance of the amplifier circuit. For example, photodiodes have an associated capacitance, and the value of this capacitance plays an important role in designing the associated amplifier circuit.
- What is the output amplitude range of the source?
- Does the source produce a voltage or a current output?
- Is the signal source output single ended or differential?
- What is the output impedance of the signal source?
- Is the input signal DC referenced? If so, to what DC voltage is it referenced?
- What are the frequency characteristics of the input signal? For example, the signal might have a 10 MHz bandwidth centered around 25 MHz or it might be a signal with frequency content from DC up to 20 MHz. If low frequency isn't important, this opens the possibility of AC coupling the input signal.
- What level of rejection is required out of band? Some applications have very strict requirements for out of band rejection, while others are less strict. The

filter interface between the amplifier network and the ADC is dictated by this sort of information.

- Must a known interfering frequency (such as a system clock or sample clock) be filtered out? Are other large signals expected outside of the band of interest? Oftentimes, a simple low pass filter may not have sufficient rejection of a particular interfering signal, forcing additional circuitry to produce a high Q notch filter.
- Is there a requirement for gain or phase flatness or error? This is a concern in video systems.
- Is there a matching requirement on the input impedance of the amplifier circuit? Some circuits require that the load seen is matched to a particular value for optimum performance (e.g., 50 Ω).

15.5 Analog to Digital Converter Characteristics

Now that the power supply and input signal have been defined, it is time to focus on the device that the op amp will drive, the analog to digital converter (Figure 15.3):

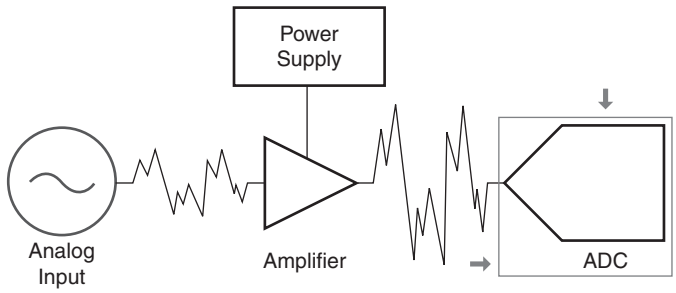


Figure 15.3: Focusing on the analog to digital converter.

- Has the analog to digital converter been selected or is it possible to change the converter if performance can be enhanced?
- What is the desired sampling rate? Often, people assume that a data converter is going to be used at its maximum level of performance, but this typically isn't the case. For example, an 80 MSps (megasample per second) converter might be given a sampling frequency of 60 MSps.

- What is the desired resolution and effective number of bits? A 14 bit converter won't effectively yield 14 bits. The true resolution probably is closer to 12 or 13.
- What is the full scale input range of the data converter? Some data converters have the option of configuring the input for different ranges.
- Will the data converter be used with single ended or differential inputs? Typically, most high performance data converters have differential inputs and require their use for optimum performance.
- Could any other options on the data converter be an advantage? Data converters have lots of options that vary from part to part. The most important feature of some ADCs is the availability of a precision reference that can be used for the op amp interface circuitry.
- Are there any compensation requirements for the input of the data converter? Normally, a small RC filter is required at the input of the data converter to compensate for its capacitive input. These components are usually specified in the converter data sheet and should be included as part of the interface. Otherwise, the op amp interface circuit may exhibit instability.

15.6 Operational Amplifier Characteristics

Although this chapter is intended to aid in the selection of the correct operational amplifier (Figure 15.4), it is possible that the nature of the system already defines some op amp characteristics:

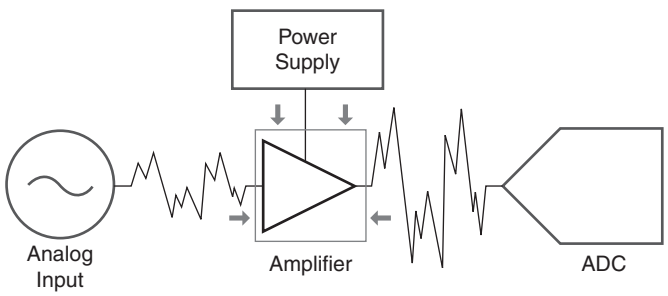


Figure 15.4: Focusing on the operational amplifier.

- Has the selection of operational amplifier already been made or can it be changed if performance of the system could be improved?
- Are there specific requirements for the package of the amplifiers? For example, must it be an 8 pin SOIC or as small as possible?
- Does the cost of the operational amplifier interface or the physical size of the interface circuitry dictate that as few operational amplifiers as possible be used or would it be an advantage for the circuitry to be easily modified in the future, using more operational amplifiers for the flexibility?

15.7 Architectural Decisions

The job is still not done. A decision must be made at this point: How will the signal chain (and interface) be implemented. The guidelines in this chapter are not meant to be device specific for every data converter or op amp, rather they are general cases that can be used as a basis for design. Let's get started.

In some cases, such as IF baseband, the best interface may well be no op amp at all but a simple transformer over a narrow frequency band, which has been employed successfully in many designs. As the title of this publication is *Op Amps for Everyone*, purely transformer interfaces are not explored at length, however a transformer may be employed in combination with op amps when gain is required.

Besides the transformer, the other decisions are

- To use single ended or fully differential op amps.
- Whether to power the interface from a single supply or split supplies (if possible).
- Whether to reference the input to ground (single ended) or make it fully differential.
- Whether the interface circuit can be AC coupled or must the operational range include DC.
- Whether the data converter can or should be referenced to ground or should it be operated in fully differential mode.

Some of the decisions may be premade, such as the selection of data converter or the power supplies (split versus single supply).

Figure 15.5 shows one of the simplest interface circuits. The CM pin of the data converter is used to set the common mode input of the fully differential op amp. The data converter compensation inputs are shown (R_5/C_1 and R_6/C_2). An input termination resistor, usually 50 Ω, is shown but may or may not be utilized. Gain of the op amp interface is set by R_1 through R_4, the common mode input range of the data converter includes ground, and the frequency response extends from DC to the bandwidth limit of the op amp circuit.

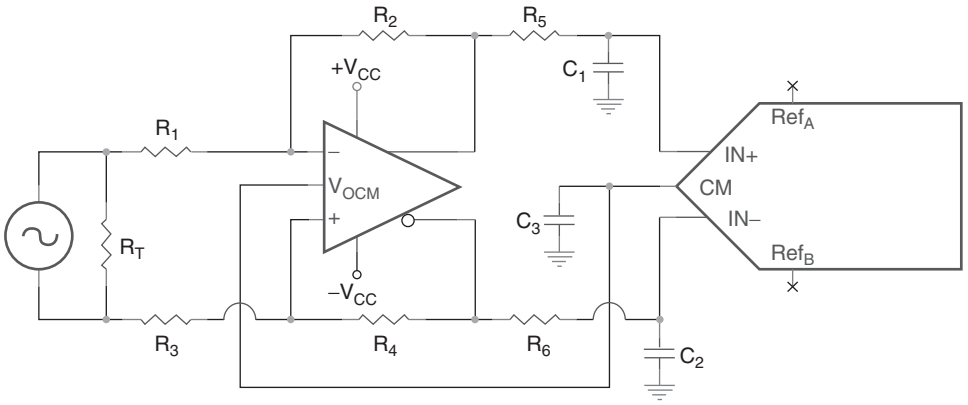


Figure 15.5: Fully differential DC coupled interface.

While this circuit is very nice, it is also not very typical of real world applications. To begin with, the op amp interface operates from split supplies, which may not be available in the system. Also, most input signals are referenced to ground, which presents its own set of challenges.

Figure 15.6 shows a more typical interface circuit. The input signal is referenced to ground, while the common mode operating point of the op amp interface is set by the data converter. The op amp interface can be run off of a single supply.

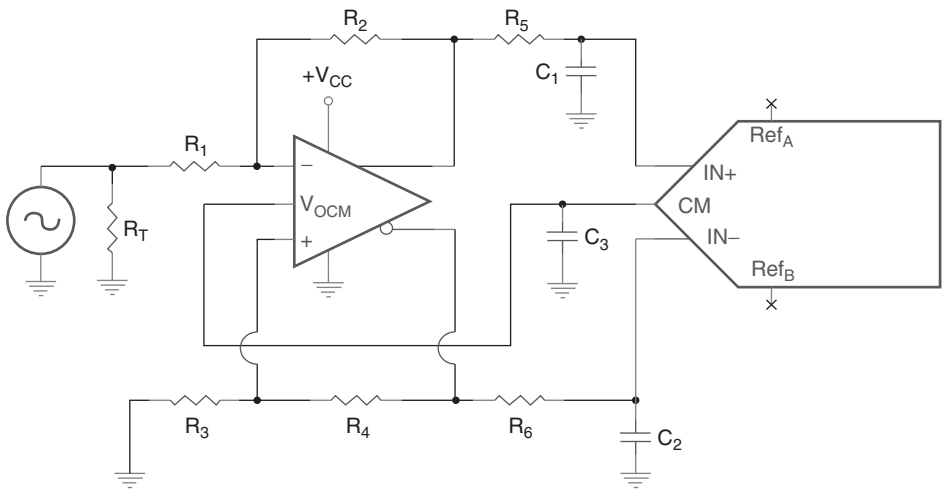


Figure 15.6: Single ended to fully differential DC coupled interface.

This configuration is covered in more detail in a later chapter, one devoted to application errors. Suffice it to say, a circuit such as this must be applied carefully.

There are several keys to the successful application of this circuit:

- The first is to be aware of the DC gain and DC operating point of the circuit. This will probably limit the AC gain severely.
- It is important to utilize an op amp that includes ground in its common mode range. Texas Instruments manufactures an op amp specifically for this configuration, the THS4500.
- If the input has to be terminated, as shown in Figure 15.6, the value of the termination resistor affects the values of the other resistors. This is covered in Section 11.6.

It is not absolutely necessary to utilize a fully differential op amp to drive a differential data converter. Figure 15.7 shows the preferred method to drive a fully differential op amp using single ended op amps. The input signal is referenced to ground, and

decoupling from the op amp interface is accomplished by using a transformer. Each phase of the output signal is handled in a conventional inverting op amp stage, and the common mode point for both amplifiers is set by the data converter. Remember that, if termination is employed, it must be reflected through the transformer. For a 1:1 transformer, R_{T1} equals R_{T2}.

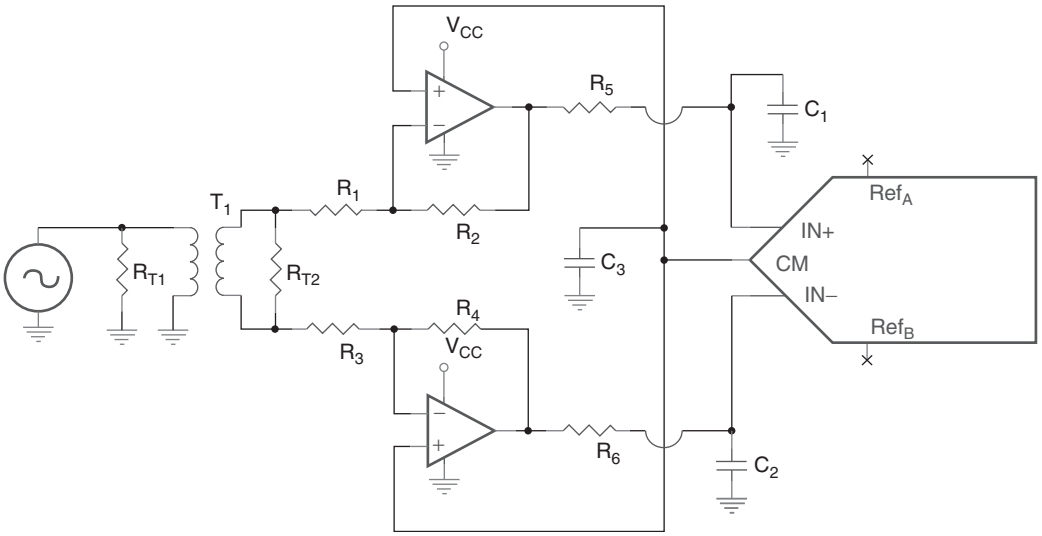


Figure 15.7: Single ended to fully differential AC coupled interface.

Figure 15.8 shows the preferred way to convert single ended signals to differential without a transformer. While this circuit looks a bit unusual, the strategy is to equalize the delay for IN+ and IN– by forcing each phase of the signal to go through both op amps before being applied to the inputs. This may not be intuitive at first glance! Each amplifier, though, is in the feedback loop for the other. Think of this as an inverting op amp circuit—gain is adjusted by changing R_1 (corresponding to R_G), R_2 through R_6 are equal values (corresponding to R_F). If DC gains are taken into account, this circuit also works for DC coupled applications.

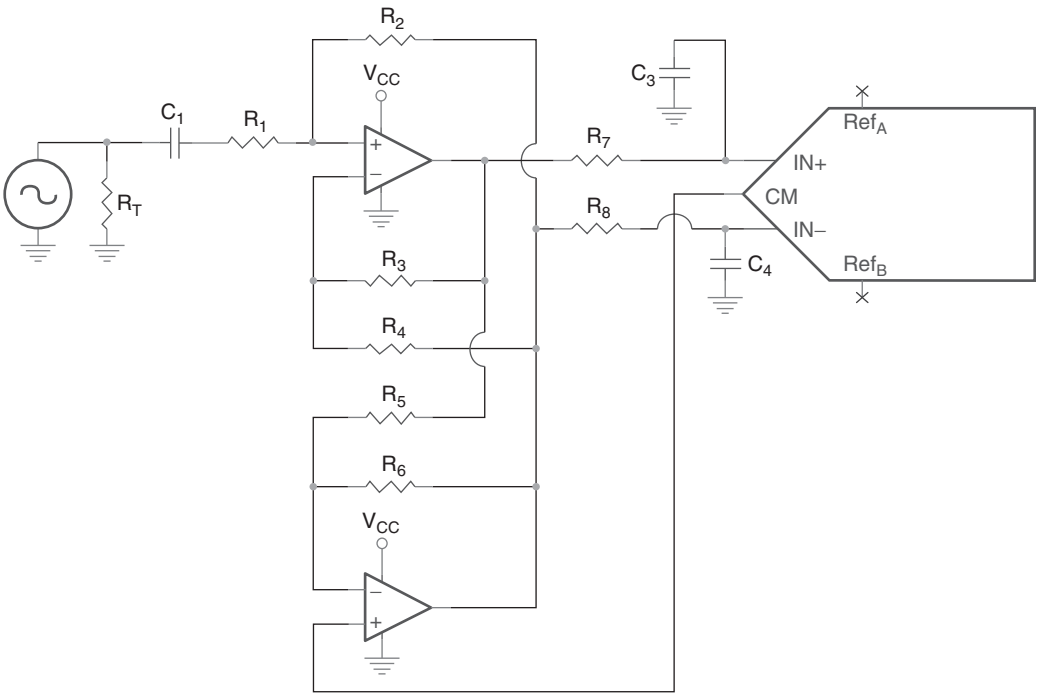


Figure 15.8: Preferred single ended to fully differential AC coupled interface.

CHAPTER 16

Wireless Communication: Signal Conditioning for IF Sampling

Perry Miller and Richard Cesari

16.1 Introduction

High speed operational amplifiers (op amps) are used extensively in wireless communication systems. These amplifiers typically operate at intermediate frequencies (IF) $\leq$500 MHz and most frequently operate below 25 MHz. Applications for high speed op amps include filtering circuits in radio receivers, IF amplifiers, mixer circuits, and bandpass amplifiers.

16.2 Wireless Systems

This chapter focuses on the requirements for the op amp and a number of techniques used in wireless communication systems to interface high speed op amps to analog to digital converters (ADCs) and digital to analog converters (DACs). This section provides several examples of op amp usage.

Figure 16.1 shows an example of a dual IF receiver. In this application, several stages with different IF frequencies are used to get the desired performance. The receiver converts the received radio frequency (RF) input from the antenna to a baseband signal. This type of system requires the ability to receive and operate over a wide range of signal strength. The inherent system noise level determines the lower operating limit and is a critical factor in the overall performance of the receiver. The receiver performance is measured in terms of receiver sensitivity, which is defined as the ratio between the power of the wanted baseband signal at the output of the ADC and the

total power of all unwanted signals (including random noise, aliasing, distortion, and phase noise contributed by the local oscillator) introduced by the different circuit elements in the receiver. A low sensitivity receiver can cause signal saturation in the ADC input.

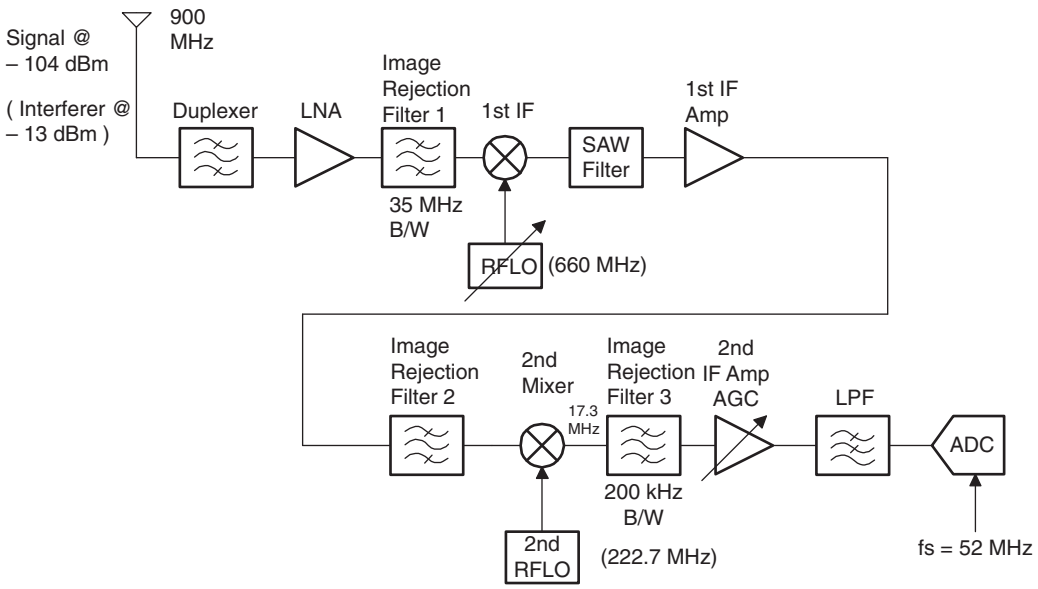


Figure 16.1: A typical GSM cellular base station receiver block diagram.

The receiver contains two mixer stages, reminiscent of a classic superheterodyne receiver with good selectivity. The process of heterodyning involves the translation of one frequency to another by the use of a mixer and local oscillator (LO) offset at the proper frequency to convert the RF signal to the desired IF. The LO signal is at a much higher level than the RF signal. In Figure 16.1, the 900 MHz RF signal is picked up by the antenna and amplified by a low noise amplifier (LNA). After being sufficiently amplified by the LNA to overcome the noise level, the RF signal passes through a bandpass filter (BPF) used to provide image rejection and sufficient selectivity prior to the first stage mixing.

High selectivity prevents adjacent channel energy from getting into the input of the ADC and decreasing the receiver dynamic range. A strong signal in an adjacent channel causes intermodulation products in the receiver that can result in loss of the received

signal. The bandpass filter is implemented with a surface acoustic wave (SAW) filter. The SAW filter provides very sharp edges to the passband, with minimum ripple and phase distortion.

The first stage mixer down converts the band limited RF signal with the LO signal, producing a number of new frequencies in the spectrum, including the sum frequency component, the difference frequency component, and spurious responses. The first stage IF filter provides sufficient filtering after the mixing circuit. It selects the difference frequency component while rejecting the sum frequency component and undesirable spurious responses. Passing on the difference frequency component to the next stage of the receiver makes it much easier to provide the gain and filtering needed for proper receiver functionality. Image rejection also places a constraint on the choice of the IF (10 MHz to 20 MHz). The spurious responses are the result of power supply harmonics and intermodulation products created during the mixing of the RF signal and the LO signal. If not substantially suppressed, spurious responses often corrupt the IF signal and cause it to be accepted as a valid IF signal by the IF amplifier.

The first stage IF amplifier minimizes the effects of the first stage filter loss on the noise figure and amplifies the signal to a suitable level for the second stage mixer. The output from the second stage mixer is applied to the second stage IF amplifier, automatic gain control (AGC) amplifier, and the subsequent low pass filter, producing a 1 V full scale input to the ADC. The ADC samples and digitizes this baseband analog input. The AGC amplifier ensures that, if the received signal amplitude goes up rapidly, the ADC is not saturated. At the other extreme, if there is a fast power ramp down, the AGC prevents the signal quality from passing below an acceptable level. High speed current feedback operational amplifiers (CFA) are typically used to filter and amplify the IF signals because this type of operational amplifier has good slew rate, wide bandwidth, large dynamic range, and a low noise figure.

In this type of receiver, the ADC is a key component requiring sampling rates of $\geq$40 MSps with 12 bits to 14 bits of resolution and is usually a pipeline architecture device. The output of the ADC is highly dependent on the ADC's sampling frequency, nonlinearities in the ADC and the analog input signal, and the converter maximum frequency.

Table 16.1 tabulates the contribution of each stage depicted in Figure 16.1 to the system level budget for a typical GSM receiver. GSM is the global system for mobile communications. It is one of the most popular digital cellular formats in the world.

Table 16.1: GSM Receiver Block System Budget

Element	Noise figure (dB)	Gain (dB)	ANF[†]
Duplexer	1	−1	1
LNA	1.6	+18	0.51616
Image rejection filter #1		−2	0.00517
First stage mixer	9.87	−7	0.21853
Noise filter		−2	0.07363
First stage amplifier	7.92	+49	1.7957
Image rejection filter #2		−2	4.31E-06
Second stage mixer	10.8	−7	5.68E-05
Second stage image filter		−2	0.0009
AGC	11	+50	2.16E-09
Antialias filter		−2	3.83E-10
ADC	7.63	−2	3.83E-10
Total			3.61 (5.7 dB)

[†]ANF = Adjusted noise figure (linear).

Figure 16.2 shows a more flexible implementation for the receiver, using a digital signal processor (DSP). Using a DSP allows a single receiver to access several wireless systems through changes in software configuration.

Figure 16.3 shows a basic W-CDMA transmit chain. A voiceband CODEC (coder/decoder), op amps, and a DSP are used to digitize and band limit the audio signal. The digitized signal is then compressed to the appropriate data rate, either in hardware or by a software program implemented on the DSP. Redundancy (error correction), encryption, and the appropriate form of modulation (QPSK for W–CDMA or GMSK for GSM) are added to the compressed digitized signal. This signal goes via an interpolating filter to the communication DAC, as shown in Figure 16.4. Eight times interpolation [1,2] is shown in Figure 16.4, but other multiples of 2 interpolations are possible and quite often used. Assuming that the modulated bit stream is a 3.84 MSPS W–CDMA signal, for 8× interpolation, the sampling clock frequency would need to be 30.72 MHz. The DAC converts the modulated bit stream to analog,

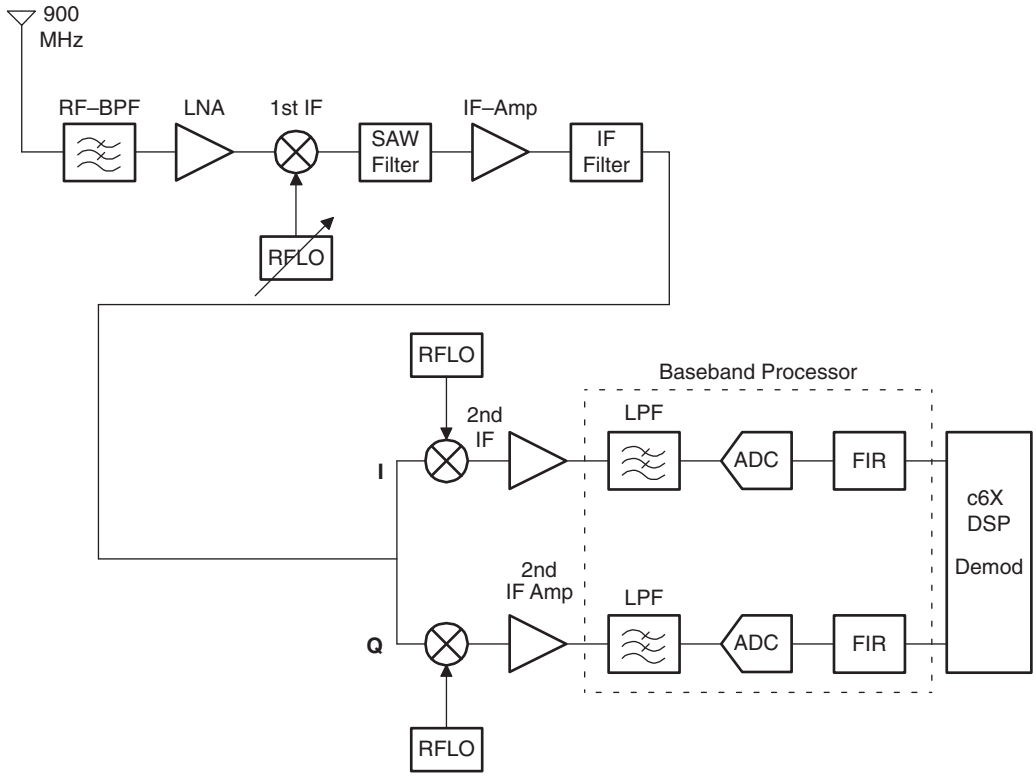


Figure 16.2: An implementation of a software configurable dual IF receiver.

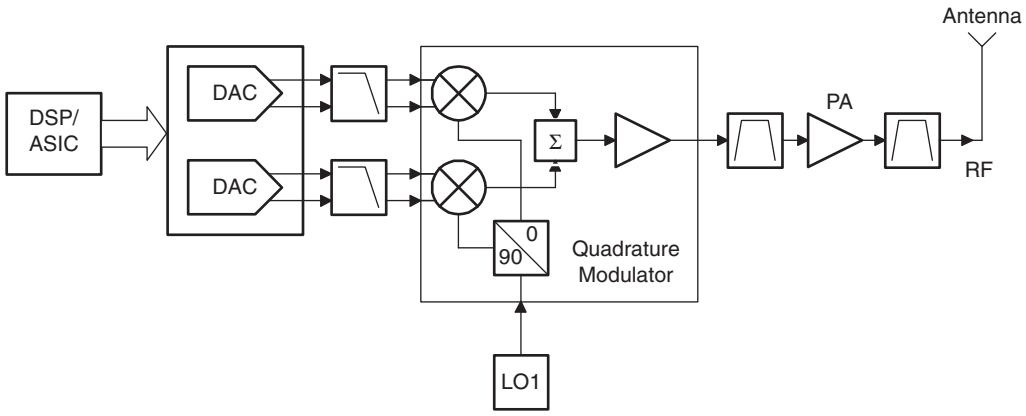


Figure 16.3: Basic W-CDMA cellular base station transmitter block.

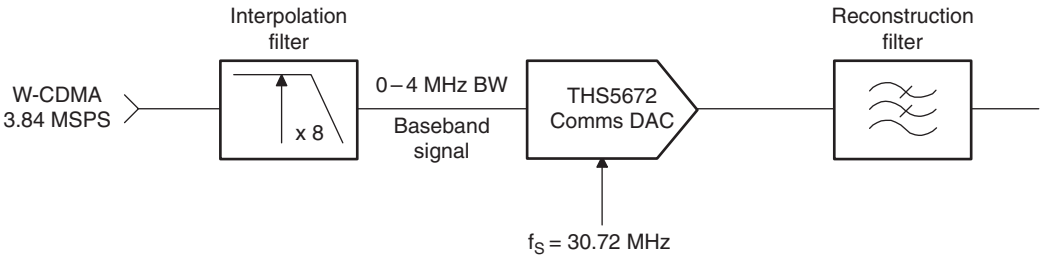


Figure 16.4: Communication DAC with interpolation and reconstruction filters.

and the conversion is usually performed by a pair of DACs: one for *I* channel and one for *Q* channel (see Figure 16.3). The reconstruction filter, at the output of the DAC, is usually a high order Bessel or elliptic filter used to low pass filter the analog output from the DAC.

The modulator block converts the baseband *I* and *Q* signals to the appropriate carrier frequency, typically 864 MHz. The up converted 864 MHz signal is amplified to a suitable level by the power amplifier (PA) and sent out via the antenna over the air or to a nearby wireless base station.

The RF power amplifier is a large signal device with power gain and efficiency on the order of 50% for GSM and about 30% for code division multiple access (CDMA), an access method in which multiple users are permitted simultaneously on the same frequency.

16.3 Selection of ADCs/DACs

In communication applications, the DC nonlinearity specifications that describe the converter's static performance are less important than the dynamic performance of the ADC. The receiver (overall system) specifications depend very much on the ADC dynamic performance parameters: ENOB (effective number of bits), SFDR (spurious free dynamic range), THD (total harmonic distortion), and SNR (signal to noise ratio). Good dynamic performance and fast sampling rate are required for accurate conversion of the baseband analog signal at RF or IF frequencies. The SFDR specification describes the converter's in band harmonic characterization and it represents the converter's dynamic range. SFDR is slew rate and converter input frequency dependent.

The output from an ADC is highly dependent on the converter sampling frequency and the maximum frequency of the analog input signal. A low pass or bandpass

antialiasing filter placed immediately before the ADC band limits the analog input. Band limiting ensures that the original input signal can be reconstructed exactly from the ADC's output samples when a sampling frequency (f_s) of twice the information bandwidth of the analog input signal is used (Nyquist sampling). Undesirable signals, above $f_s/2$, of a sufficient level can create spectrum overlap and add distortion to the desired baseband signal. This must not be allowed to dominate the distortion caused by ADC nonlinearities. Sampling at the Nyquist rate places stringent requirements on the antialiasing filter, usually a steep transition 10th or higher order filter is needed.

Oversampling techniques (sampling rate greater than the Nyquist rate) can be employed to drastically reduce the steepness of the antialiasing filter roll-off and simplify the filter design. However, whenever oversampling is used, a faster ADC is required to digitize the input signal. Very fast ADCs can be costly, and they consume a fair amount of power ($\geq$1000 mW). In a system application, such as a wireless base station, where large numbers of ADCs are used, the individual device power consumption must be kept to the bare minimum ($\leq$400 mW). High resolution ADCs, with slower sampling rates, offer potential cost savings, lower power consumption, and good performance and are often used in some applications. In this case, undersampling or bandpass sampling techniques (the analog signal digitization by the ADC exceeds half the sampling frequency, f_s, of the ADC, but the signal information bandwidth is $\leq f_s/2$) are employed.

Operating the ADC in a bandpass sampling application requires knowledge of the converter's dynamic performance for frequencies above $f_s/2$. In general, as the input signal frequency to the converter increases, ENOB, SNR, SFDR, and harmonic performance degrade.

The fact that the analog input to the ADC cannot be represented exactly with a limited number of discrete amplitude levels introduces quantization error into the output digital samples. This error is given by the rms quantization error voltage: $e_{\text{qns}}^2 = \frac{1}{12} q_s^2$, where q_s is the quantization step size.

The mean squared quantization noise power is $P_{\text{qn}} = q_s^2/12R$, where R is the ADC input resistance, typically 600 Ω to 1000 Ω.

Communication ADCs similar to the THS1052 and THS1265 typically have a full scale range (FSR) of 1 V P–P to 2 V P–P. Generally, wireless systems are based on a 50 Ω input/output termination, therefore the ADC input is made to look like 50 Ω.

Based on this assumption, the quantization noise power for a 12 bit, 65 MSps ADC (THS1265) is –73.04 dBm.

For a noise limited receiver, the receiver noise power can be computed as the thermal noise power in the given receiver bandwidth plus the receiver noise figure (NF) [3].

For a 200 kHz BW (GSM channel), temperature 25°C, and 4 dB to 6 dB NF, the receiver noise power is –115 dBm. Therefore, to boost the receiver noise to the quantization noise power level requires a gain of 42 dB.

In Figure 16.1, the GSM 900 signal is at –104 dBm (GSM 900 spec for smallest possible signal at which the raw bit error rate must meet or exceed 1%) and therefore the signal to noise ratio at baseband or at the converter and due to the thermal noise component is given by $\mathrm{SNR}_{\mathrm{thermal}} = \dfrac{E_b}{N_0} = -104\ \mathrm{dBm} + 115\ \mathrm{dBm} = 9\ \mathrm{dB}$.

For the raw bit error rate (BER) to be 1% in a GSM system, testing and standard curves [4] indicate, that a baseband SNR (derived from the sum of both thermal noise and ADC noise) of 9 dB is needed for this performance node.

The process gain (G_P) is defined as

$$G_P = \frac{f_s}{\mathrm{BW}} = \frac{52 \times 10^6}{200 \times 10^3} = 2.6 \times 10^2 = 24.15\ \mathrm{dB} \tag{16.1}$$

where GSM channel BW = 200 kHz and f_s = 52 MHz (the ADC sampling frequency).

The converter noise at the baseband should be much better than the radio noise (= thermal noise + process gain). Furthermore, the thermal noise alone brings the system only to the reference bit error rate. Therefore the converter noise (at baseband) = $\mathrm{SNR}_{\mathrm{adc}}$ + process gain G_p.

The ADC $\mathrm{SNR}_{\mathrm{adc}}$ should be 20 dB to 40 dB above the $\mathrm{SNR}_{\mathrm{thermal}}$ of the thermal noise component (+9 dBm). In this example, ADC $\mathrm{SNR}_{\mathrm{adc}}$ is selected to be 37 dB better than the $\mathrm{SNR}_{\mathrm{thermal}}$ of the thermal noise component (9 dB).

In other words, if the converter $\mathrm{SNR}_{\mathrm{adc}}$ is desired to be 37 dB better than the thermal noise component ($\mathrm{SNR}_{\mathrm{thermal}}$), the baseband converter is chosen to be 9 + 37 dB = 46 dB.

The total noise (N_{sum}) = thermal noise (N_t) + converter noise (N_{conv}). Therefore, the noise to signal ratio is

$$\frac{N_{sum}}{S_{GSM}} = \frac{N_t}{S_{GSM}} + \frac{N_{conv}}{S_{GSM}} = \frac{1}{10^{0.9}} + \frac{1}{10^{4.6}} \tag{16.2}$$

The signal to noise ratio is $S_{GSM}/N_{sum} = 7.942$ (linear), which is 8.999 dB.

This shows that the converter noise degenerates the baseband SNR due to thermal noise alone, by only 0.0001 dB (9.000 dBm – 8.999 dB) when the signal is at reference sensitivity level.

At $f_s = 52$ MSps, the converter SNR_{adc} required to fit the GSM 900 signal is (46 – 24.15) dB = 22 dB.

The effective number of bits required for fitting the GSM 900 signal is

$$\text{ENOB} = \frac{\text{SNR} - 1.76}{6.02} \tag{16.3}$$

hence 4 bits are needed for the GSM 900 signal.

Assuming that filter 3 attenuates the interferer by 50 dB, the interferer drops from –13 dBm to –53 dBm, or 40 dB above the GSM signal. The requirements for the number of bits needed to accommodate the interferer is (40 dB)/(6 dB/bit) = 63 bits.

Approximately 6 bits are needed to accommodate the interferer, plus 2 bits of headroom for constructive interference, for a total of 8 bits. The ADC requirements are 4 bits for the GSM signal plus 8 bits for the interferer for a total of 12 bits (Figure 16.5).

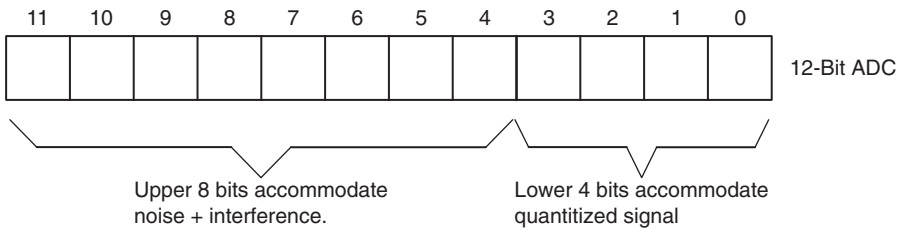


Figure 16.5: ADC requirements for the GSM signal.

It follows from the preceding analysis that the GSM signal is 8 bits down, or 8 bits × 6 dB/bit = 48 dB down from the 1 V FSR of the ADC. The full scale input power to an ADC having a 50 Ω termination can be calculated as

$$\frac{V_2}{R} = \frac{(1)^2}{50} = 2 \times 10^{-2} = 13 \text{ dBm (full scale or FSR)} \quad (16.4)$$

Therefore, the 4 bits for the GSM signal gives 13 dBm – (8 bits × 6 dB/bit) = –35 dBm, the smallest possible ADC input signal power with the interferer that meets the GSM specification. Without the interferer present, the signal level is chosen to be about 20 dB below the ADC full scale, or –8 dBm, to accommodate constructive interference and any large ADC input signal that may arise from short term errant gain due to gain settling in the AGC. Thus, with the smallest possible signal specified by the GSM 900 spec, the signal is amplified from –104 dBm to –8 dBm without the interferer and to –35 dBm with the interferer.

For a practical receiver, as shown in Figure 16.1, an AGC is necessary to assure that the LSB represents a uniform noise input while the peak power does not exceed the ADC's FSR.

The receiver block shown in Figure 16.1 uses a high speed, fairly wide bandwidth (100 MHz to 550 MHz) communication ADC to convert the baseband signal to a high speed parallel bit stream for processing in a DSP. For an ADC to accurately produce a digital version of the baseband analog input, the device must have very good resolution and dynamic performance.

The signal path shown in Figure 16.1 needs 95 dB of gain to bring the –104 dBm GSM signal up to –9 dBm (equivalent to about 0.112 V P–P across 50 Ω), with allowances for losses in the filters, and mixers. Usually this gain is split evenly between the RF and baseband, but baseband gain is less expensive and consumes less power. The LNA provides 18 dB, which after filtering and cable losses, yields about 16 dB, while the mixer provides –7 dB of conversion gain/loss.

Modern communication DACs are, effectively, an array of matched current sources optimized for frequency domain performance. To handle both strong and weak signals, communication DACs require a large dynamic range. The dynamic specifications of most interest are SFDR, SNR, THD, IMD (two tone intermodulation distortion), ACPR (adjacent channel power rejection), and settling time.

Besides these, a number of DC parameters, such as integral nonlinearity (INL) and differential nonlinearity (DNL), are considered important because of their influence on

the SFDR parameter. DNL errors occur only at certain points in the converter's transfer function. INL and DNL errors appear as spurious components in the output spectrum and can degrade the signal to noise ratio of the DAC.

Typical SFDR figures for 12 bit and 14 bit DACs, with a 5 MHz single tone input at 50 MSps, range from 75 dB to 80 dB. To prevent adjacent communication channels from interfering with each other, the DAC must exhibit a good SFDR specification. Communication DACs normally have differential outputs, and the current mode architecture is used to give the DAC a higher update rate.

16.4 Factors Influencing the Choice of Op Amps

IF amplifiers and filters can be built from discrete components, although most modern applications use integrated circuits. High speed wideband op amps are employed as buffer amplifiers in the LO circuit, at the front end of ADCs, at the output of the DAC, in the external voltage reference circuits for ADCs and DACs, and in the AGC amplifier and antialiasing stage. Op amps operating at IF frequencies, such as the AGC amplifier in Figure 16.1, must attain a large gain control range. How well the amplifier handles large and small signals is a measure of its dynamic range. The current feedback op amp can be used everywhere except for the antialiasing filter and in the reconstruction filter stage. The op amp must have a level gain response from almost DC to at least 500 MHz, after which a gentle roll-off is acceptable. Also, the phase response is important to avoid dispersing the signal—this requires a linear phase response.

Several factors influence the choice of the current feedback op amp (CFA) and voltage feedback amplifier (VFA) for use in wireless communication systems:

- The ADC/DAC resolution.
- ADC/DAC dynamic specification.
- Operating frequencies.
- Type of signal.
- Supply voltages.
- Cost.

In both the receiver and transmitter circuits, shown in Figures 16.1 and 16.3, the SFDR and IMD are the key ADC/DAC parameters that have the most influence on op amp selection. A minimum requirement is that the op amp's SFDR or THD parameter,

measured at the frequency of operation, should be 5 dB to 10 dB better than the converter's SFDR. For a perfect 12 bit ADC, the SFDR is 72 dB, therefore the op amp in front of the ADC should exhibit an SFDR (or THD) of 77 dB to 82 dB.

When an op amp is used as a buffer amplifier, it must faithfully reproduce the input to a very high degree of accuracy. This requires that the amplifier be designed and optimized for settling time. Fast settling time is mandatory when driving the analog input of an ADC, because the op amp output must settle to within 1 LSB of its final value (within a time period set by the sampling rate) before the ADC can accurately digitize the analog input. The amplifier settling time determines the maximum data transfer rate for a given accuracy. For example, to settle within 1 LSB of full scale range implies that the settling accuracy of the ADC is ±½ LSB. Hence, a 12 bit ADC requires the op amp to settle to $1/(2 \times 2^{12}) = 1.22 \times 10^{-4}$ of final value, or 0.0122% of final value. An LSB = 244 μV for a 12 bit ADC with 1 V full scale range. Values for the settling time and other important op amp parameters as they relate to the receiver and transmit blocks are listed in Table 16.2. The op amp dynamic

Table 16.2: High Speed Op Amp Requirements

Parameter	Value
Noise voltage	2.7nV/$\sqrt{\text{Hz}}$ to 8 nV/$\sqrt{\text{Hz}}$
Noise current	1pA/$\sqrt{\text{Hz}}$ to 30 pA/$\sqrt{\text{Hz}}$
THD	70 dBc to 95 dBc
Slew rate	260 V/μV to 3500 V/μV
Small signal bandwidth	200 MHz to 600 MHz
Large signal bandwidth	≥100 MHz
Common mode input voltage	3 V
Supply voltage	±5 V
Settling time	8 ns to 20 ns
Output current	40 mA to 100 mA
Output impedance	≤20 Ω
PSRR	−60 dB
CMRR	−70 dB
Input offset voltage	10 mV (typical)

parameters in Table 16.2 represent the range of values to achieve low noise, good SFDR, high slew rate, good bandwidth, and the like.

Op amps operating from ±5 V supplies typically have 6 V to 8 V of common mode range. Single supply op amps often handle much smaller voltage ranges and, in some communication applications, could exhibit limited linear operation over a wide signal swing. With the exception of rail to rail op amps, most op amps can swing to within 1 V to 1.5 V of the positive rail. Typically, signal to noise ratio, slew rate, and bandwidth suffer for devices operating from low supply voltages.

When selecting current feedback op amps, the gain/bandwidth plots are essential. They are needed because, with current feedback, ordinary loop gain/proportional bandwidth relationships do not hold.

16.5 Antialiasing Filters

Spurious effects in the receiver channel (Figure 16.1) appear as high frequency noise in the baseband signal present at the ADC. The spurious signals ($>f_s/2$) must be blocked from getting to the ADC (sampling at Nyquist rate, f_s), where they cause aliasing errors in the ADC output.

A suitable antialiasing low pass analog filter placed immediately before the ADC can block all frequency components capable of causing aliasing from reaching the ADC. The antialiasing filter cutoff frequency (f_c) is set to the highest baseband signal frequency of interest ($f_{\max}$) so that $f_c = f_{\max}$. The sampling theorem requires that the ADC minimum Nyquist rate sampling frequency $f_s = 2f_{\max}$. This ensures that the original baseband or IF signal can be reconstructed exactly from the ADC's digital outputs. It is important to know that only an antialiasing filter having a *brickwall* type response could fully satisfy the exacting requirements imposed by the sampling theorem. The roll-off of real filters increases more gradually from cutoff to the stop band, and therefore in practice, the ADC sampling frequency is usually slightly higher than $2f_{\max}$.

The antialiasing filter must reduce the out of band aliasing producing signals to less than 1 LSB of the ADC resolution, without introducing additional distortion of the baseband or IF signal in band components and without predominating distortion due to the ADC nonlinearities. The spectrum overlap (aliasing) requirements are determined by

- Highest frequency of interest.
- Sampling rate.
- ADC resolution.

The highest signal frequency of interest sets the filter cutoff frequency. For example, suppose the input signal is to be sampled to 12 bit accuracy with a sampling frequency of 52 MHz. If the IF signal is 17 MHz, an 18 MHz filter –3 dB cutoff frequency could be chosen. All frequencies above the Nyquist frequency should be attenuated to $\leq$½ LSB, but generally only frequencies above the ADC's limit of resolution are a problem; that is, $f_{alias} = (52 - 17)$ MHz $= 35$ MHz. The frequency roll-off is 18 MHz to 35 MHz (about one octave) and the required attenuation is 72 dB (12 bit ADC). A very high order filter is required to accomplish this task. Practical antialiasing filters are limited to a fifth order or sixth order type because of amplifier bandwidth, phase margin, layout parasitics, supply voltage, and component tolerances. Keep in mind that, as the roll-off sharpens, the passband ripple and phase distortion increase.

For communication applications, linear phase characteristic and gain accuracy (low passband ripple) are important. And normally, Tschebyscheff or elliptic (Cauer) filter types are used for the antialiasing filter.

For good transient response or to preserve a high degree of phase coherence in complex signals, the filter must be of linear phase type (Bessel type filter).

The THS4011 or THS4021 voltage feedback op amp is a good choice for implementing the antialiasing filter in this example.

The quality of the capacitors and resistors used to implement the design is critical for performance of the antialiasing filter.

16.6 Communication D/A Converter Reconstruction Filter

Modern communication DACs are, effectively, an array of matched current sources optimized for frequency domain performance. The most important dynamic specifications are SFDR, SNR, THD, IMD, ACPR, and settling time. The DC parameters INL and DNL are considered important because of their influence on the SFDR parameter. Typical SFDR figures for 12 bit to 14 bit DACs, with a 5 MHz single tone input at 50 MSps, range from 75 dB to 80 dB. To prevent adjacent communication channels from interfering with each other, the DAC must exhibit a good SFDR specification.

Communication DACs normally have differential outputs, and current mode architecture is used to give the DAC a higher update rate.

Figure 16.4 shows an interpolating filter block before the DAC and the reconstruction analog filter at the output of the DAC. The interpolating filter is a digital filter whose system clock frequency is an integer multiple of the filter input data stream and is employed to reduce the DACs in band aliased images. This eases the job of the reconstruction filter at the output of the DAC. The filter is used to smooth the input data—the output waveform frequency is the same as the input to the interpolating filter. Figure 16.6 shows the interpolation filter output. The system clock frequency of the DAC and the interpolating filter run at the same rate; therefore the frequency spectrum of the DAC output signal, repeated at integer multiples of the sampling rate, becomes increasingly separated as the sampling rate is increased. The further apart the repeated DAC output spectrum, then the less steep the attenuation characteristic of the antialiasing needs to be. Consequently, a simpler antialiasing filter with a less steep roll-off from passband to stop band can be used without any increase in distortion due to aliasing. In Figure 16.4, the system clock is 30.772 MHz (3.84 MSps $\times$ 8). Figure 16.7 shows the attenuation characteristics needed for the reconstruction antialiasing filter.

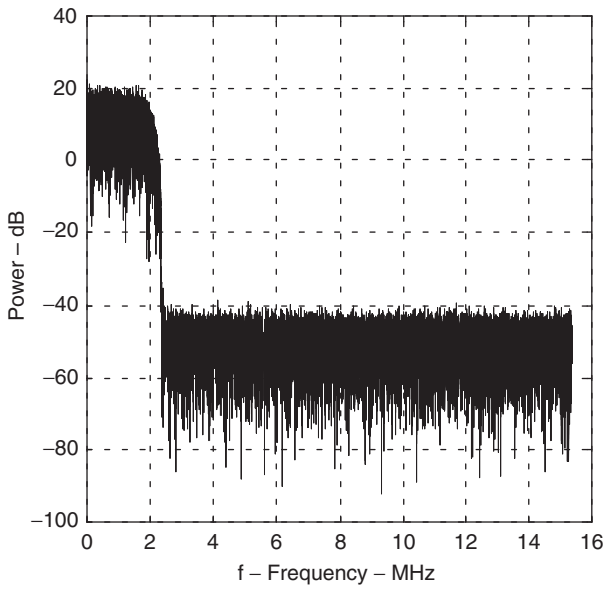


Figure 16.6: QPSK power spectral density without raised cosine filter, W-CDMA.

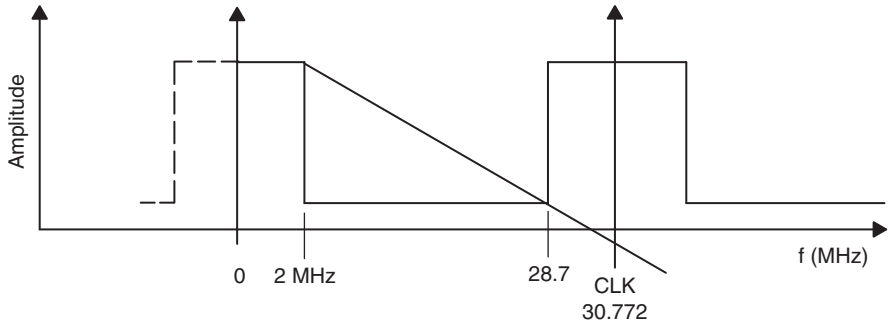


Figure 16.7: Reconstruction filter characteristics.

The aliasing frequency is $f_{alias} = (28.7 - 2) = 26.7$ MHz, and the required attenuation is 84 dB (14 bit DAC). A third order antialiasing low pass elliptic or Bessel filter could be used to meet the attenuation requirements. Either type of high order filter gives a relatively flat response up to just below one half the sampling frequency, followed by a sharp cutoff. But this arrangement provides no correction for the sinc function $(\sin x)/x$ falloff in amplitude naturally produced by the sample and hold function in the DAC.

The trade-off in building a simpler reconstruction filter is that a faster DAC is required to convert the input digital data stream to analog signal.

Figure 16.8 shows a first order reconstruction (low pass) filter consisting of a high speed differential amplifier configured for unity gain. The DAC outputs are terminated into 50 Ω. In Figure 16.8, the value for the filter capacitor is given by the expression

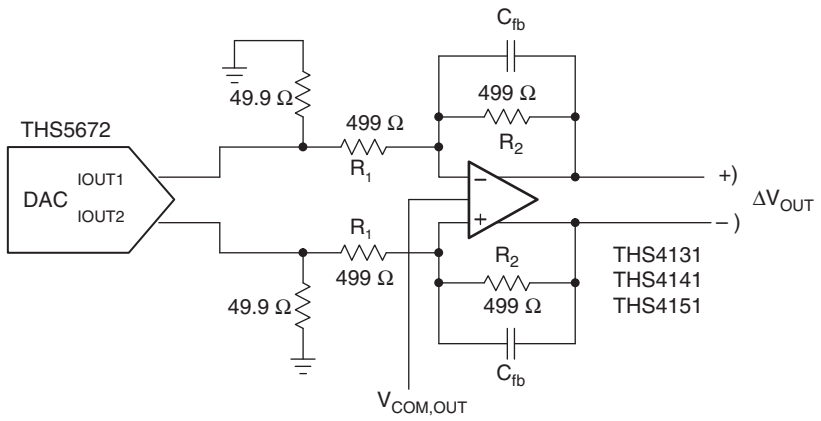


Figure 16.8: A single-pole reconstruction filter.

$$C_{\text{fb}} = \frac{3.1827 \times 10^{-4}}{\frac{f_{\text{clk}}}{2}} \tag{16.5}$$

16.7 External V_{REF} Circuits for ADCs/DACs

Figure 16.9 shows an op amp voltage follower circuit often used to interface the external precision voltage reference supplying the ADC/DAC external reference voltage (see, for example, Miller and Moore [5, 6] for a more detailed discussion on voltage reference circuits used in ADC and DAC systems). V_{IN} is the output from a precision voltage reference, such as the Thaler Corporation's VRE3050. The low pass filter (formed by C_1R_1) filters noise from the reference and op amp buffer. The –3 dB corner frequency of the filter is $1/2\pi C_1R_1$ and the transfer function for this circuit can be written as

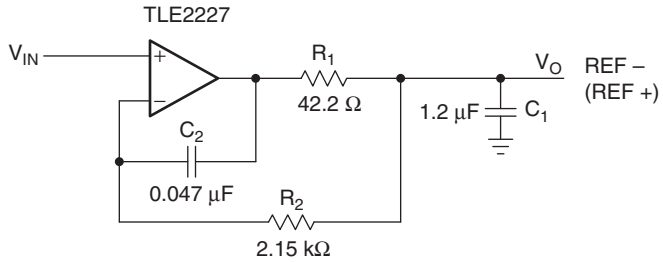


Figure 16.9: Voltage reference filter circuit.

$$\frac{V_o}{V_{\text{IN}}} = \frac{(1 + sC_2R_2)}{\left(s^2 + \frac{sC_2R_2}{C_1C_2R_1R_2} + \frac{1}{C_1C_2R_1R_2}\right)C_1C_2R_1R_2} \tag{16.6}$$

which has a zero at $s = C_2R_2$.

With the approximation $C_2R_2 = 2C_1R_1$, the denominator polynomial is solved for complex poles P_1 and P_2 of the response, which results in

$$P_1 = -\frac{1}{2C_1R_1} + j\frac{1}{2C_1R_1} \tag{16.7}$$

$$P_2 = -\frac{1}{2C_1R_1} + j\frac{1}{2C_1R_1} \tag{16.8}$$

The zero in the numerator of the transfer function improves the relative stability of the circuit. Resistor R_2 should be kept fairly low, since a small amount of bias current flows through it and causes DC error and noise. The value of resistor R_1 ranges from 10 Ω to 50 Ω. Resistor R_1 is in the feedback loop, so any small leakage current due to capacitor C_1 flows through R_1 and the voltage dropped across R_1 is divided by the loop gain. For all practical purposes, the voltage across C_2 is 0 V and hence gives rise to negligible leakage current.

A design example for a 3 kHz bandwidth filter is illustrated:

Choose $C_1 = 1.2$ μF and $R1 = 42.2$ Ω.

Having determined the value for C_1 and R_1, the capacitor C_2 value is estimated to be approximately 4 to 5% of the C_1 value ($C_2 = 0.047$ μF), and resistor R_2 is calculated using the approximation $C_2R_2 = 2C_1R_1$ ($R_2 = 2.15$ kΩ).

The calculated –3 dB bandwidth for the circuit is 3.1 kH, and this value agrees with the circuit's frequency response plot shown in Figure 16.10. This circuit topology is good for driving large capacitive loads.

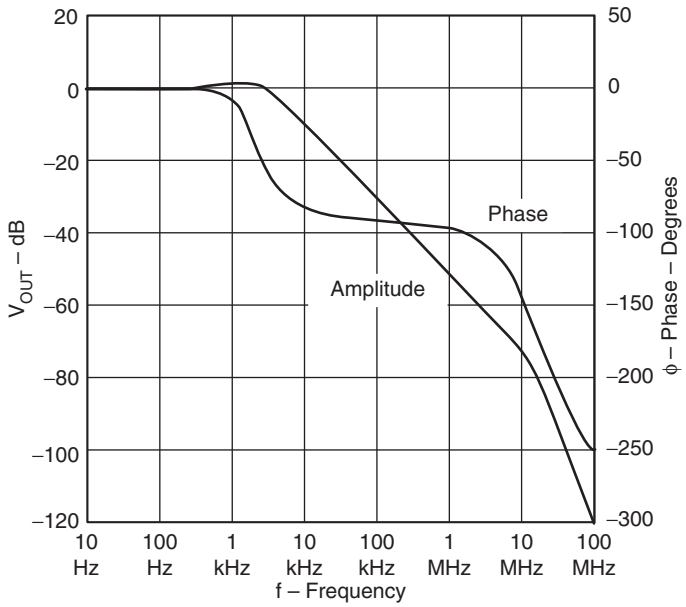


Figure 16.10: Voltage follower frequency response plot.

Figure 16.11 shows an external reference circuit that provides a wide adjustment range of the ADC full scale range. Resistors R_{281} and R_{282} play two roles in this circuit:

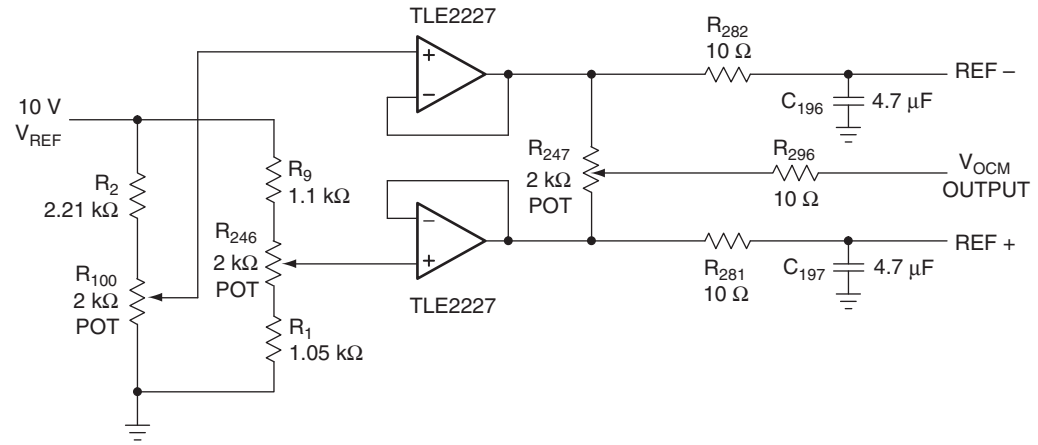


Figure 16.11: External voltage reference circuit for ADC/DAC.

- Form part of the low pass filter used to roll off noise.
- Isolate the ADC's reference input load capacitance from the buffer op amp output.

Potentiometer R_{247} sets the external common mode voltage (V_{OCM}) for the differential amplifier in Figure 16.12.

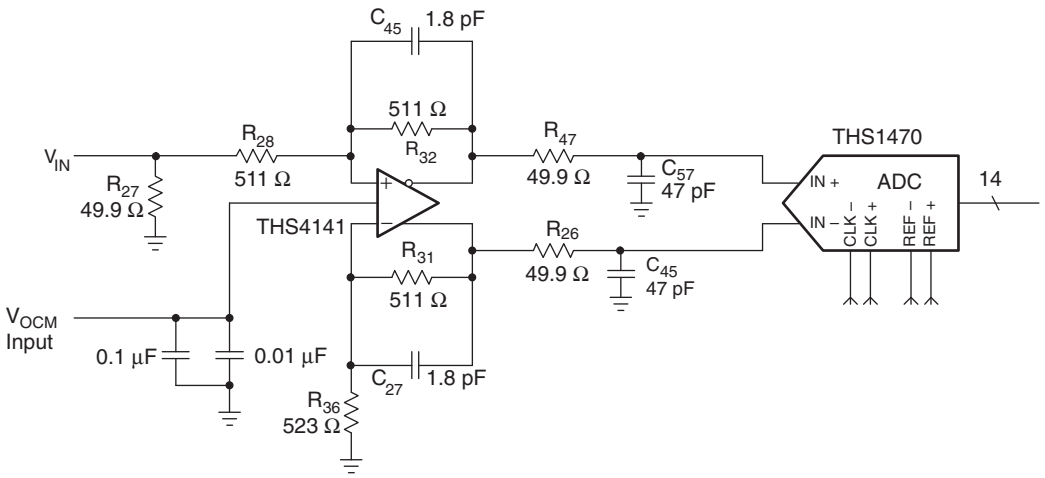


Figure 16.12: Single ended to differential output drive circuit.

16.8 High Speed Analog Input Drive Circuits

Communication ADCs, for the most part, have differential inputs and require differential input signals to properly drive the device. Drive circuits are implemented with either RF transformers or high speed differential amplifiers with large bandwidth, fast settling time, low output impedance, good output drive capabilities, and a slew rate on the order of 1500 V/μs. The differential amplifier is usually configured for a gain of 1 or 2 and is used primarily for buffering and converting the single ended incoming analog signal to differential outputs. Unwanted common mode signals, such as hum, noise, DC, and harmonic voltages are generally attenuated or canceled out. Gain is restricted to wanted differential signals, which is often 1 V to 2 V.

The analog input drive circuit, as shown in Figure 16.12, employs a complementary bipolar (BiCom) THS4141 device. The BiCom offers fast speed, linear operation over a wide frequency range, and a wide power supply voltage range but draws slightly more current than a BiCMOS device. The circuit closed loop response is shown in Figure 16.13, where the –3 dB bandwidth is 120 MHz, measured at the output of the amplifier. The analog input V_{IN} is AC coupled to the THS4141 and the DC voltage V_{OCM} is the applied input common mode voltage. The combination R47–C57 and R26–C34 are selected to meet the desired frequency roll-off. If the input signal frequency is above 5 MHz, higher order low pass filtering techniques (third order or greater) are employed to reduce the op amp's inherent second harmonic distortion component.

Figure 16.14 shows a design example of an AC coupled, single ended analog input drive circuit. This circuit uses a THS3201 current feedback op amp and operates up to 975 MHz. The amplifier is configured as a noninverting amplifier with a gain of 2, where gain is $1 + R_4/R_3$. In a current feedback amplifier, the feedback resistor sets the amplifier bandwidth and the frequency response shape as well as defining the gain of the circuit. R_4 and R_3 cannot be arbitrary values.

The frequency response plots for a gain of 2, with $R_3 = R_4 = 619\ \Omega$, are shown in Figures 16.14 and 16.15. R_4 affects the amplifier bandwidth and frequency response peaking. R_3 has no effect on bandwidth and frequency peaking; it affects only the gain. The –3 dB bandwidth is 520 MHz. Increasing the resistance of R_4 decreases the bandwidth. Conversely, lowering R_4 resistance increases the bandwidth at the expense of increased peaking in the AC response.

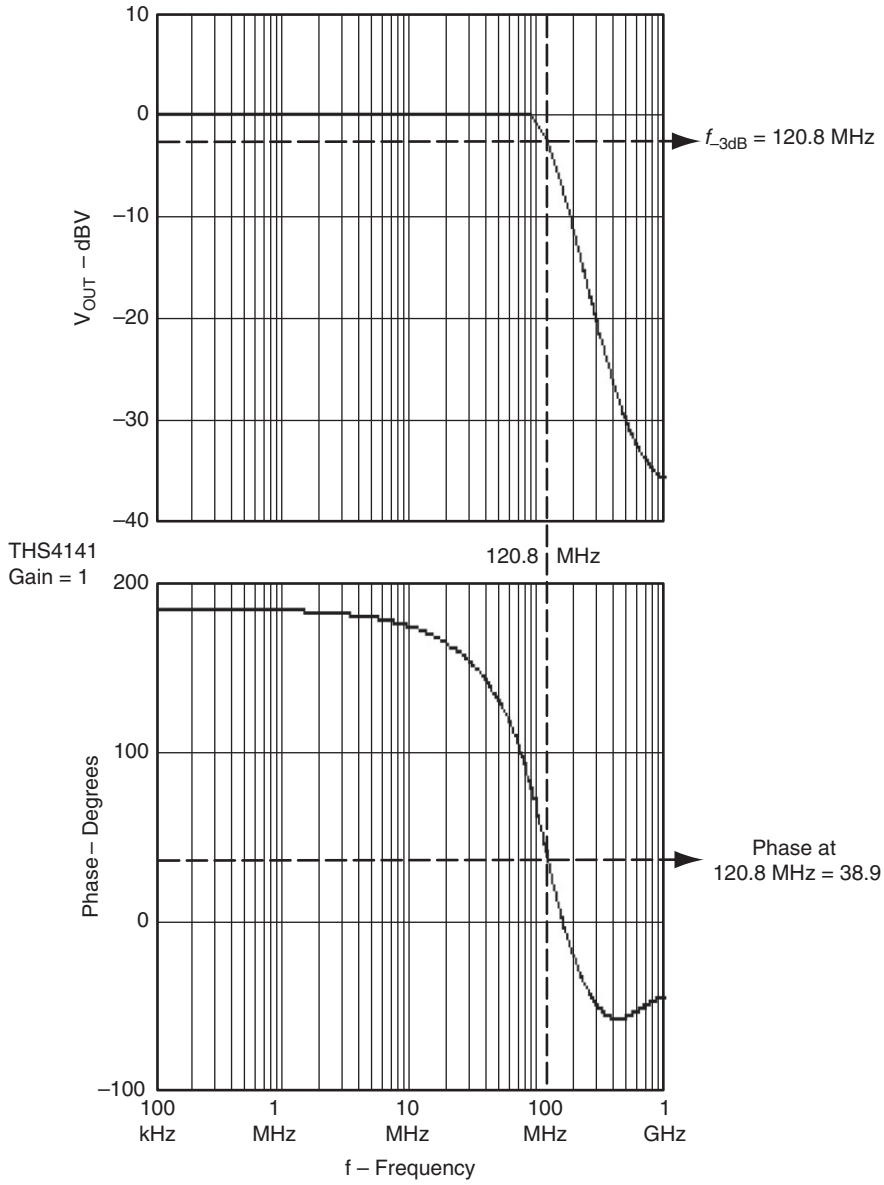


Figure 16.13: Differential amplifier closed loop response.

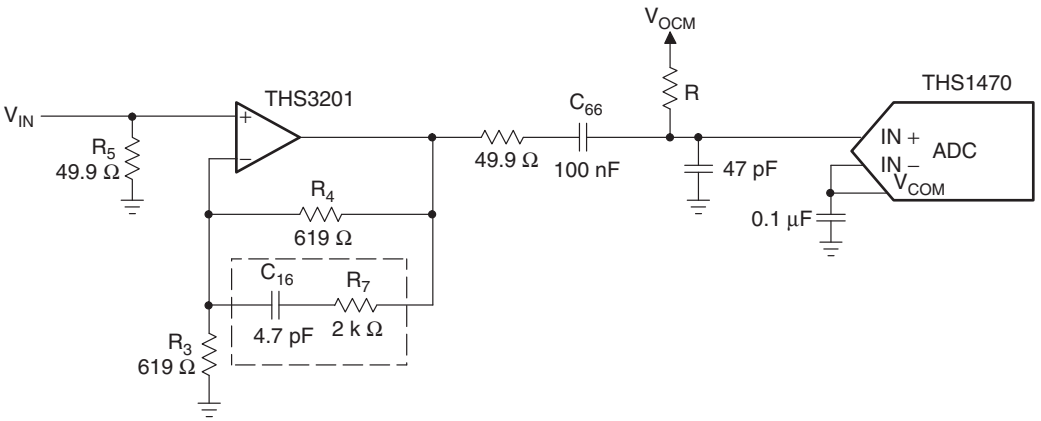


Figure 16.14: ADC single ended input drive circuit.

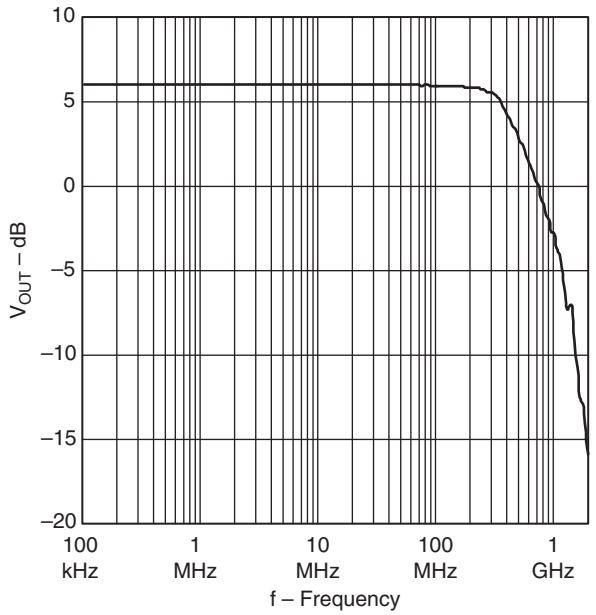


Figure 16.15: Gain versus frequency plot for THS3201.

The phase plot in Figure 16.16 exhibits a fairly linear phase shift (a flat group delay response) and hence the amplifier output should show excellent signal reproduction.

Unlike a voltage feedback amplifier, the power supply voltage affects the bandwidth of a current feedback amplifier. For example, lowering the supply voltage of the THS3201 from ±5 V to ±2.5 V reduces the bandwidth from 925 MHz to 350 MHz.

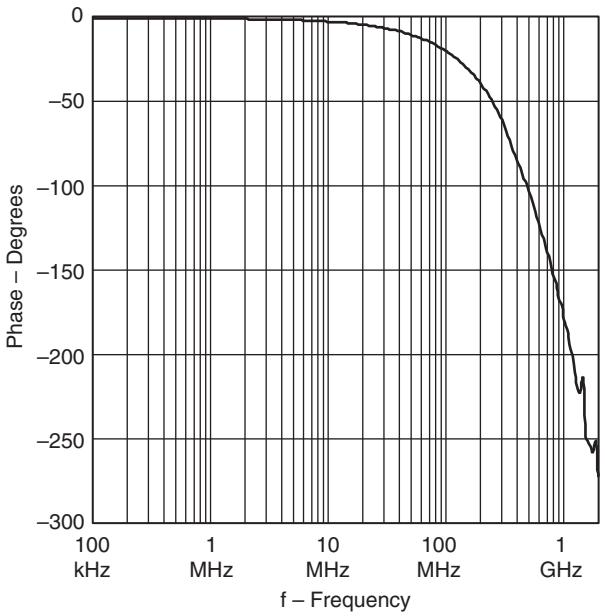


Figure 16.16: Phase versus frequency plot for THS3201.

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CHAPTER 17

Using Op Amps for RF Design

17.1 Introduction

RF design used to be the exclusive domain of discrete devices. The advent of new generations of high speed voltage and current feedback op amps made it possible to use op amps for RF design. Op amp based RF circuitry is easier to design and has less associated risk. "Tweaking" in the lab can be almost eliminated. Despite the many advantages, traditional RF designers are reluctant to utilize op amps. They are confronted with a bewildering array of op amp parameters, many of which do not relate directly to the set of design parameters with which they are familiar. This chapter bridges the gap between RF designers and op amp designers, giving RF designers common ground with which to begin their design.

When talking about using op amps for RF design, the question that has to be answered is, Why? Traditional RF design techniques, using discrete transistors, have been practiced successfully for decades. RF designers who are comfortable with things "as is" scrutinize introduction of a new design technique, using op amps. The cost of high speed op amps, in particular, raises eyebrows. Why replace a transistor, which costs a few cents, with a component that may cost several dollars?

This is a valid question to ask for high volume consumer goods, and in almost every case, the answer is to stay with traditional techniques. For high performance RF equipment, however, high speed op amps have some distinct advantages. History has shown than many other applications have migrated to op amps in the past to take advantage of the superior performance they provide. It is reasonable to assume that high speed applications such as RF will also make the move.

17.2 Advantages

The first major advantage is flexibility. High speed op amps offer a high degree of flexibility over discrete transistor implementations. When discrete transistors are used, the bias and operating point of the transistor interacts with the gain and tuning of the stage.

In contrast, when op amps are used, the bias of the stage is accomplished simply by applying the appropriate power supplies to the op amp power pins. Gain of the stage is completely independent of the bias. Gain does not affect the tuning of the stage, which is accomplished through passive components.

Transistor parameter drift must also be taken into account over the system operating temperature range. When op amps are used, the drift is reduced.

17.3 Disadvantages

As attractive as op amps are for RF design, some barriers hinder their use. The first barrier, of course, is cost.

The RF designer must learn how to set the op amp's operating point, but the process is considerably easier than biasing a transistor stage.

The RF designer is used to describing RF performance in certain ways. Analog designers think in terms of AC performance. The two ways of thinking are not compatible. The RF designer must learn how to translate op amp AC performance parameters into an RF context. That is one of the main purposes of this chapter.

17.4 Voltage Feedback or Current Feedback?

The RF designer considering op amps is presented with a dilemma: Are voltage feedback amplifiers or current feedback amplifiers better for the design? Frequency of operation is usually the most demanding aspect of RF design, and this makes the op amp bandwidth a critical parameter. The bandwidth specification given in op amp data sheets refers only to the point where the unity gain bandwidth of the device has been reduced by 3 dB by internal compensation or parasitics, which is not very useful for determining the actual operating frequency range of the device in an RF application.

Internally compensated voltage feedback amplifier bandwidth is dominated by an internal "dominant pole" compensation capacitor. This gives them a constant gain/bandwidth limitation. Current feedback amplifiers, in contrast, have no dominant

pole capacitor and therefore can operate much closer to their maximum frequency at higher gain. Stated another way, the gain/bandwidth dependence has been broken.

To illustrate this, a voltage feedback and current feedback op amp are compared:

- THS4001, a voltage feedback amplifier with a 270 MHz (−3 dB) open loop bandwidth, is usable to only about 10 MHz at a gain of 10 (20 dB).
- THS3001, a current feedback amplifier with a 420 MHz (−3 dB) open loop bandwidth, is usable to about 150 MHz at a gain of 10 (20 dB).

It is still the call of the designer to determine what he or she wants to do. At unity and low gains, there may not be much advantage to using a current feedback amplifier, but at higher gains, the choice is clearly a current feedback amplifier. Many RF designers would be extremely happy if they could obtain a gain of 10 (20 dB) in a single stage with a transistor—it is difficult to do. With an op amp, it is almost trivial.

17.5 A Review of Traditional RF Amplifiers

A traditional RF amplifier (Figure 17.1) uses a transistor (or, in the early days, a tube) as the gain element. DC bias ($+V_{BB}$) is injected into the gain element at the load

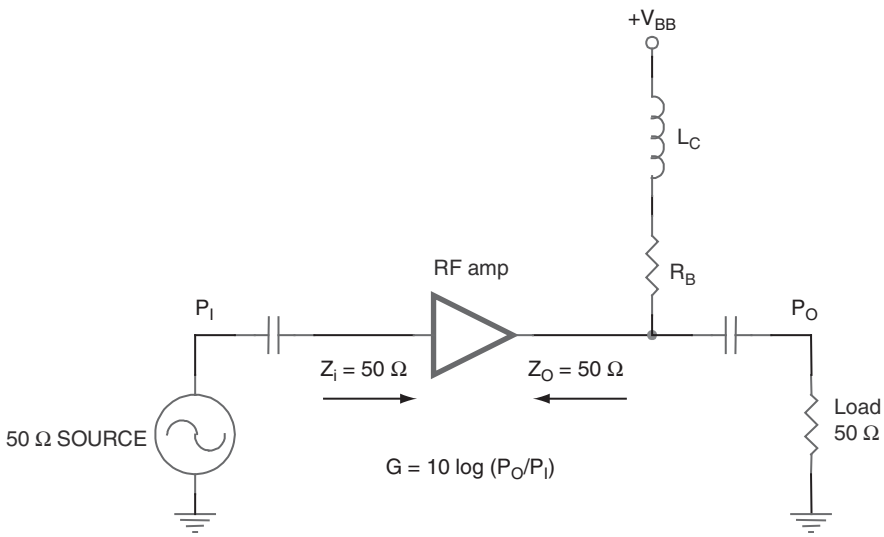


Figure 17.1: A traditional RF stage.

through a bias resistor R_B. RF is blocked from being shorted to the supply by an inductor L_C, and DC is blocked from the load by a coupling capacitor.

Both the input impedance and the load are 50 Ω, which ensures matching between stages.

When an op amp is substituted as the active circuit element, several changes are made to accommodate it.

By themselves, op amps are differential input, open loop devices. They are intended to be operated in a closed loop topology (different from a receiver's AGC loop). The feedback loop for each op amp must be closed locally, within the individual RF stage.

There are two ways of accomplishing this. The op amp designer refers to them as *inverting* and *noninverting*. These terms refer to whether the output of the op amp circuit is inverted from the input or not. From the standpoint of RF design, this is seldom of any concern. For all practical purposes, either configuration works and gives equivalent results.

Figure 17.2 shows a noninverting RF amplifier. The input impedance of the noninverting input is high, so the input is terminated with a 50 Ω resistor. Gain is set by the ratio of R_F and R_G:

$$G = 20 \log \frac{1}{2}\left(1 + \frac{R_F}{R_G}\right) \text{dB, log gain}$$

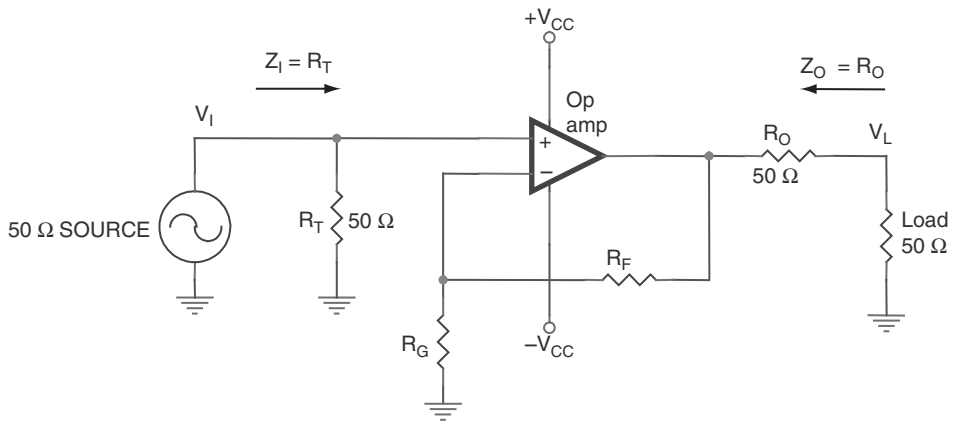


Figure 17.2: Noninverting RF op amp gain stage.

For a desired gain,

$$1 + \frac{R_F}{R_G} = 2(10^{G/20})$$

The gain of this stage as shown should never be below one half (−6 dB), because most op amps are unity gain stable.

The output of the stage is converted to 50 Ω by placing a 50 Ω resistor in series with the output. This, combined with a 50 Ω load, means that the gain is divided by 2 (−6 dB) in a voltage divider. So, a unity gain (0 dB) gain stage would become a gain of one half, or −6 dB.

The RF designer may note that the power supply requirements have been complicated by the addition of a second negative supply. The stage can be modified easily for single supply operation, as shown in Figure 17.3.

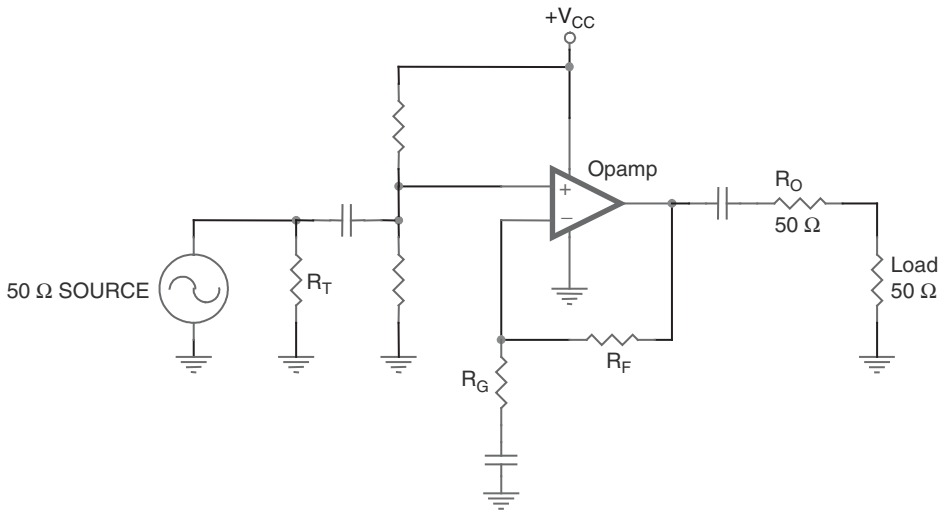


Figure 17.3: Single supply noninverting RF amplifier.

A virtual ground is generated on the noninverting input after the coupling capacitor, to raise the operating point of the op amp to a virtual ground halfway between the supply voltage and ground.

Coupling capacitors are needed to isolate preceding and succeeding stages and the gain resistor R_G from the virtual ground DC potential. These capacitors should be selected to have low impedance at the operating frequency, but not so small that they affect the gain of the stage directly or cause unacceptable variations in gain over the operating range of the stage.

If the amplifier selected is a voltage feedback type, it is also possible to make an inverting RF stage. Inverting stages made from current feedback amplifiers are not generally practical because of the low input impedance of the inverting input, which is connected to the output of an internal voltage buffer.

Figure 17.4 shows an inverting RF amplifier. The input impedance of this configuration is still relatively high and is again terminated with a 50 Ω resistor. Gain is set by the ratio of R_F and R_G.

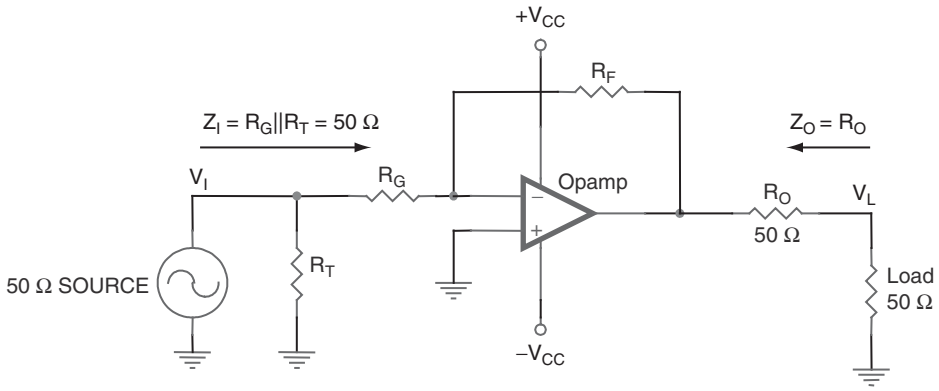


Figure 17.4: Inverting RF stage.

The output of the stage is converted to 50 Ω by placing a 50 Ω resistor in series with the output. This is combined with a 50 Ω load, which means that the gain is divided in 2 (6 dB) in a voltage divider. An inverting stage must be used for gains less than one half, or −6 dB, again because most op amps are unity gain stable.

$$G = 20 \log\left(\frac{1}{2}\frac{R_F}{R_G}\right)\text{dB, log gain}$$

For a desired gain,

$$\frac{R_F}{R_G} = 2(10^{G/20})$$

As before, the RF designer may notice that the power supply requirements have been complicated by the addition of a second negative supply. As before, it can be modified easily for single supply operation, as shown in Figure 17.5.

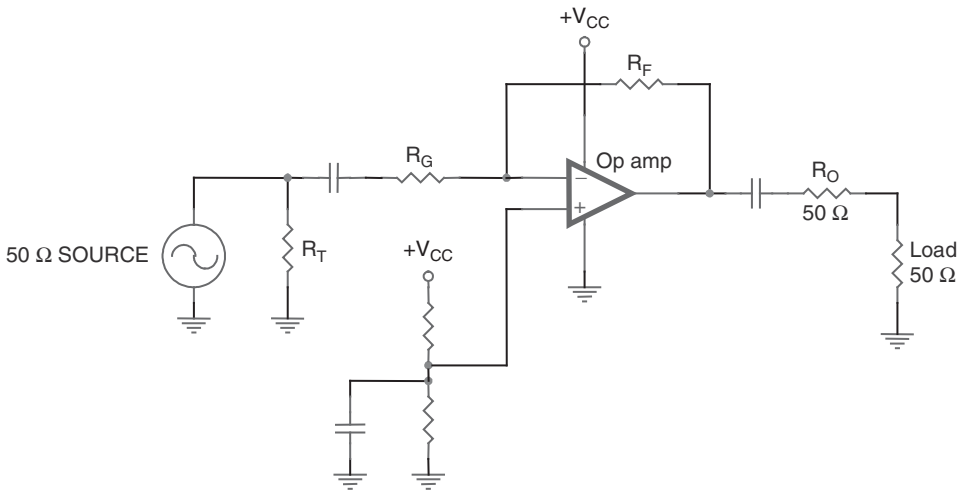


Figure 17.5: Single supply inverting RF amplifier.

A virtual ground is generated on the noninverting input to raise the operating point of the op amp to a virtual ground halfway between the supply voltage and ground. This virtual ground should be local to the stage and decoupled locally to prevent RF emission or conduction out of the stage. It is unwise to produce a virtual ground to use in more than one stage because of the possibility of crosstalk.

Coupling capacitors are needed to isolate preceding and succeeding stages from the virtual ground DC potential. These capacitors should be selected to have low impedance at the operating frequency, as before.

17.6 Amplifier Gain Revisited

Op amp designers think of the gain of an op amp stage in terms of voltage gain. RF designers, in contrast, are used to thinking of RF stage gain in terms of power:

$$\text{Absolute power (W)} = \frac{V_{\text{rms}}^2}{50\ \Omega}$$

$$P_0(\text{dBm}) = 10 \log \frac{\text{Absolute power}}{0.001\text{W}}$$

$$\text{dBm} = \text{dBV} + 13 \text{ in a } 50\ \Omega \text{ system}$$

17.7 Scattering Parameters

RF stage performance is often characterized by four "scattering" parameters, which are defined in Table 17.1.

Table 17.1: Scattering Parameters

	Scattering parameter	RF amplifier specification
S_{11}	Input reflection	Input VSWR
S_{22}	Output reflection	Output VSWR
S_{21}	Forward transmission	Amplifier gain and bandwidth
S_{12}	Reverse transmission	Reverse isolation

The term *scattering* has a certain implication of loss, and that is indeed the case in three cases. Reflections, as in the VSWR (voltage standing wave ratio) scattering parameters S_{11} and S_{22}, can cancel useful signals. Reverse transmission, S_{12}, steals output power from the load. The only desirable scattering parameter is S_{21}, the forward transmission. Design of an RF stage involves maximizing S_{21} and minimizing S_{11}, S_{22}, and S_{12}.

Small signal AC parameters specified for RF amplifiers are derived from S parameters. These specifications are frequency dependent. They are measured using a network analyzer and an S parameter test set. The test circuit is shown in Figure 17.6.

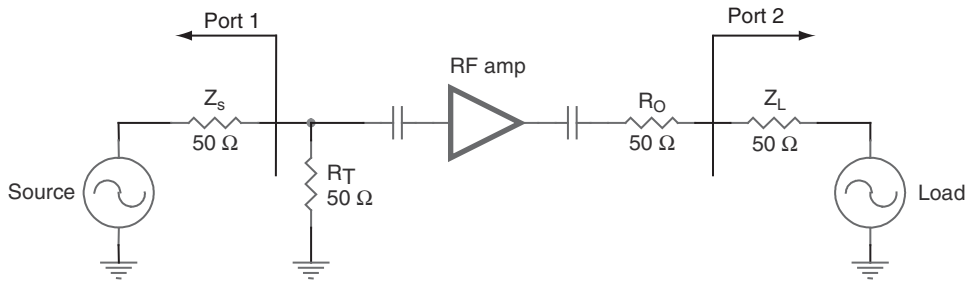


Figure 17.6: Scattering parameter test circuit.

17.7.1 Input and Output VSWR S_{11} and S_{22}

The voltage standing wave ratio is just another term for input or output reflection. It is a ratio, and therefore a unitless quantity. VSWR is a measure of how well the input and output impedances are matched to the source and load impedances. They should be as closely matched as possible to avoid reflections.

VSWR is defined as

$$\text{VSWR} = \frac{Z_I}{Z_S} \text{ or } \frac{Z_S}{Z_I}, \text{whichever is} > 1$$

where

Z_I = amplifier input or output impedance.

Z_S = test system source impedance.

The ideal VSWR is equal to 1:1, but typical VSWR's are no better than 1.5:1 for RF amps over their operating frequency range.

Measuring the input VSWR is a matter of measuring the ratio of the reflected power versus incident power on Port 1 of the previous figure (S_{11}). A perfect match reflects no power. Output VSWR is measured the same way at Port 2 (S_{22}).

An op amp's input and output impedances are determined by external components selected by the designer. For this reason, VSWR cannot be specified on an op amp's data sheet.

17.7.2 Return Loss

Return loss is related to VSWR in the following way:

$$\text{Return loss} = 20 \log \frac{\text{VSWR} + 1}{\text{VSWR} - 1}$$

$$= 10 \log(S_{11})^2 \text{ input}$$

$$= 10 \log(S_{22})^2 \text{ output}$$

R_O is not a perfect match for Z_L at high frequencies. The output impedance of the amplifier increases as the loop gain falls off. This changes the output VSWR. A peaking capacitor, C_O, added in parallel with R_O can compensate for this effect. Because op amp output impedance is well defined, a fixed value can usually be substituted after experimentation determines the correct value (Figure 17.7).

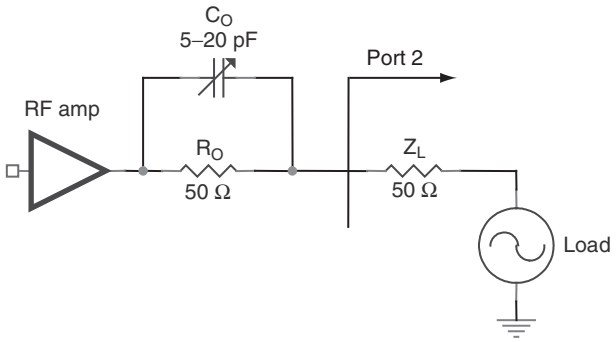


Figure 17.7: Output peaking capacitor.

The termination resistor sets the input impedance, but as the frequency increases, nonresistive effects come into play. Not only do the effects of the termination resistor come into effect, but those of R_G and R_F as well. Figure 17.8 illustrates the high frequency model of a stage.

Obviously, analysis of a high frequency stage can become a nightmare. Using microwave components reduces these parasitic effects and extends the maximum usable frequency of the circuit. Reducing the input impedance of the amplifier also extends the maximum usable frequency by swamping the effects of high frequency parasitic components.

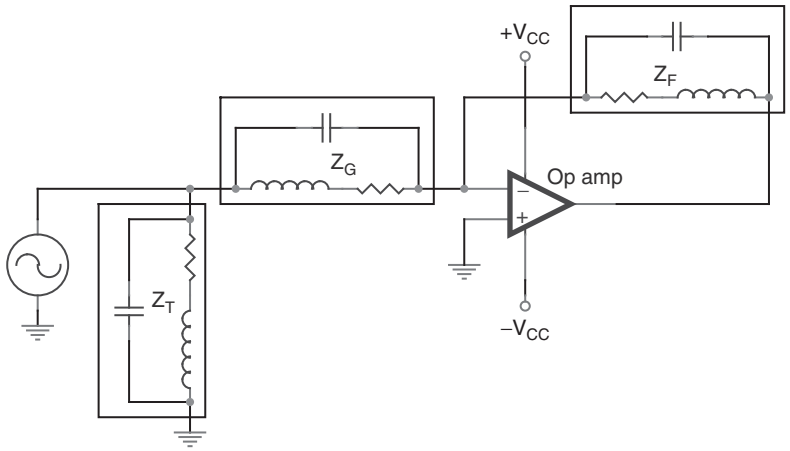


Figure 17.8: Simplified high frequency inverting stage.

There are three ways of reducing the input impedance:

- Use the inverting configuration with a voltage feedback amplifier.
- Use the noninverting configuration with a current feedback amplifier.
- Limit the gain of the stage.

17.7.3 Forward Transmission S_{21}

The forward transmission, S_{21}, is specified over the operating frequency range of interest. S_{21} is never specified on an op amp data sheet, because it is a function of the gain, which is set by the input and feedback resistors, R_F and R_G. The forward transmission of a noninverting op amp stage is

$$S_{21} = A_L = \frac{V_L}{V_I} = \frac{1}{2}\left(1 + \frac{R_F}{R_G}\right)$$

The forward transmission of an inverting op amp stage is

$$S_{21} = A_L = \frac{V_L}{V_I} = -\frac{1}{2}\frac{R_F}{R_G}$$

Op amp data sheets show open loop gain and phase. It is the responsibility of the designer to know the closed loop gain and phase. Fortunately, this is not hard to do. The data sheets many times include excellent graphs of open loop bandwidth and sometimes include phase. Closing the loop produces a straight line across the graph at the desired gain, curving to meet the limit. The open loop bandwidth plot should be used as an absolute maximum. The designer that approaches the limit does so at the expense of extensive compensation and complex PCB layout techniques.

To illustrate this point, two hypothetical 1 GHz op amps are shown in Figure 17.9, one voltage feedback and the other current feedback. If a gain of 20 dB is required, the voltage feedback amplifier is limited to just over 10.7 MHz, barely adequate for an FM IF amplifier. If a gain of 40 dB is required, the voltage feedback amplifier is limited to just over 1 MHz, barely adequate for medium wave/AM amplification.

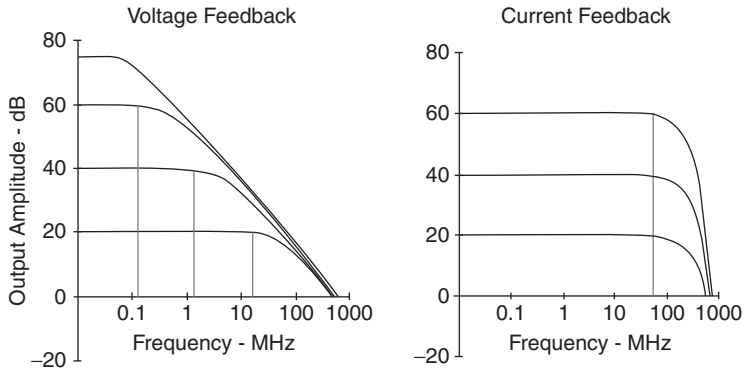


Figure 17.9: Gain bandwidth comparison of voltage and current feedback op amps.

The current feedback amplifier, on the other hand, is usable to about 50 MHz in both cases. The designer is cautioned to take extra care to avoid oscillations at high gains. Remember the RF designer's rule: All oscillators begin as amplifiers, and all amplifiers begin as oscillators.

17.7.4 Reverse Transmission S_{12}

Op amp topologies, in particular current feedback amplifiers, assume both inputs are connected to low impedances. Therefore, the reverse isolation of op amp RF circuits is excellent (Figure 17.10).

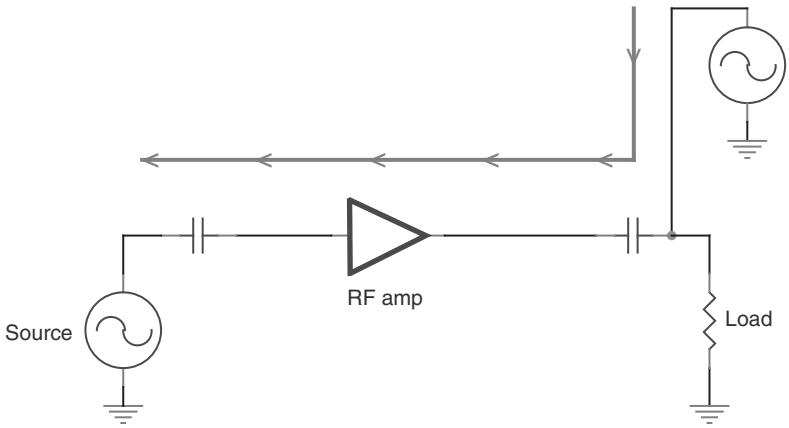


Figure 17.10: Reverse transmission.

The reason why op amps have such good reverse isolation is that, instead of the gain element being a single transistor with its associated leakage, the reverse signal has to go through the leakage of dozens or hundreds of transistors fabricated on the silicon of the op amp (Figure 17.11).

Reverse isolation is somewhat better in noninverting current feedback amplifier configurations, because the output signal must also leak through the circuitry connecting the noninverting and inverting inputs to get to the source.

17.8 Phase Linearity

Oftentimes, a designer is concerned with the phase response of an RF circuit. This is particularly the case with video design, which is a specialized type of RF design.

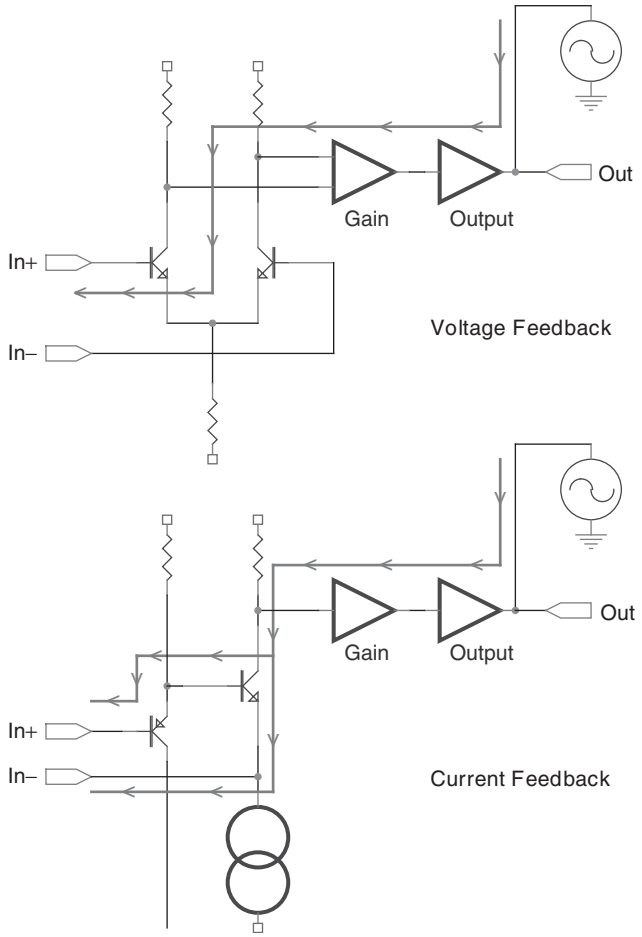


Figure 17.11: Reverse transmission path through op amps.

Current feedback amplifiers tend to have better phase linearity than voltage feedback amplifiers:

- Voltage feedback THS 4001: Differential phase = 0.15°.
- Current feedback THS 3001: Differential phase = 0.02°.

17.9 Frequency Response Peaking

Current feedback amplifiers allow an easy resistive trim for frequency peaking that has no impact on the forward gain. This frequency response flatness trim has the same effect in noninverting and inverting configurations.

Figure 17.12 shows this adjustment added to an inverting circuit. This resistive trim inside the feedback loop has the effect of adjusting the loop gain, hence the frequency response, without adjusting the signal gain, which is still set by R_F and R_G.

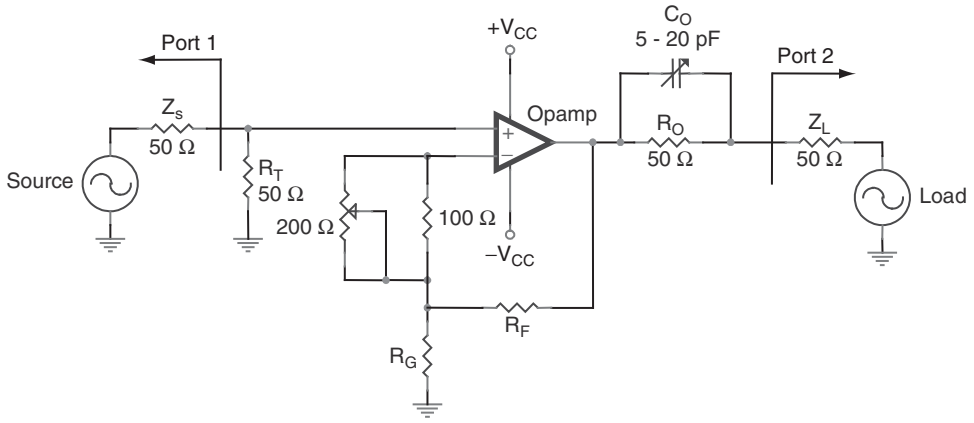


Figure 17.12: Frequency response peaking.

Values for R_F and R_G must be reduced to compensate for the addition of the trim potentiometer, although their ratio and hence the gain should remain the same. The adjustment range of the potentiometer, combined with the lower R_F value, ensures that the frequency response can be peaked for slight current feedback amplifier parameter variations.

17.10 −1 dB Compression Point

The −1 dB compression point is defined as the output power, at a fixed input frequency, where the amplifier's actual output power is 1 dBm less than expected. Stated another way, it is the output power at which the actual amplifier gain has been reduced by

1 dB from its value at lower output powers. The −1 dB compression point is the way RF designers talk about voltage rails.

Op amp designers and RF designers have very different ways of thinking about voltage rails, which are related to the requirements of the systems that they design:

- An op amp designer interfacing op amps to data converters, for example, takes great pain not to hit the voltage rail of the op amp, thus losing precious codes.
- An RF designer, on the other hand, is often concerned with squeezing the last half decibel out of an RF circuit. In broadcasting, for example, a very slight increase in decibels means a lot more coverage. More coverage means more audience and more advertising dollars. Therefore, slight clipping is acceptable, as long as the resulting spurs are within FCC regulations.

Standard AC coupled RF amplifiers show a relatively constant −1 dB compression power over their operating frequency range. For an operational amplifier, the maximum output power depends strongly on the input frequency. The two op amp specifications that serve a similar purpose to −1 dB compression are V_{OM} and slew rate.

At low frequencies, increasing the power of a fixed frequency input eventually drives the output "into the rails," the V_{OM} specification. At high frequencies, op amps reach a limit on how fast the output can transition (respond to a step input). This is the slew rate limitation of the amplifier. The op amp slew rate specification is divided by 2, because of the matching resistor used at the output.

As is the case for op amps used in any other application, it is probably best to avoid operation near the rails, as the inevitable distortion produces harmonics in the RF signal—harmonics that are probably undesirable for FCC testing. That said, if harmonics are still at an acceptable level at the −1 dB compression point, it can be a very useful way to boost power to a maximum level out of the circuit.

17.11 Two Tone, Third Order Intermodulation Intercept

When two closely spaced signals are present in the RF bandwidth being amplified, sum and difference frequencies are created. These sum and difference frequencies are intermodulation harmonics. They are undesirable and may lead to problems with FCC testing of the system.

The problem with these harmonics is that they increase in amplitude three times as fast as the fundamentals. Figure 17.13 shows a theoretical system with a beginning fundamental signal level of 0 dBM, with intermodulation harmonics at −60 dBm. As the amplitude of the fundamentals is increased, the harmonics are seen increasing at three times the rate of the fundamentals, leading to an eventual intercept of the two lines at +30 dBm.

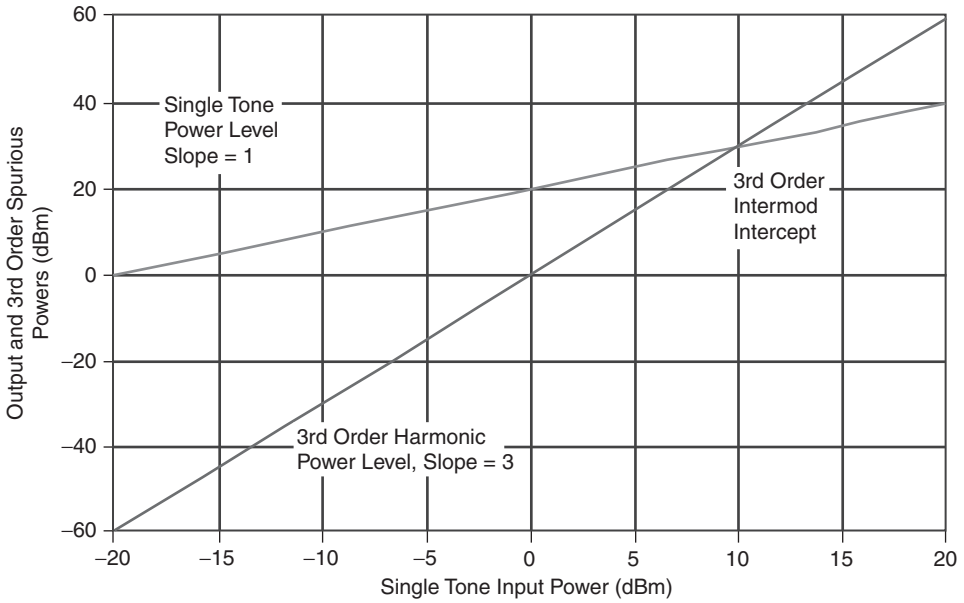


Figure 17.13: Two tone, third order intermodulation intercept.

The typical RF circuit can not be adjusted to +30 dBm, so the third order intermodulation intercept is theoretical. The third order intermodulation intercept should be as high as possible, because that means that the intermodulation harmonics are proportionally lower at any real world fundamental level.

Figure 17.14 demonstrates the two tone intermodulation intercept in a different way. The fundamental frequencies at $f_O - \Delta f$ and $f_O + \Delta f$ are shown, so are the third order harmonics at $f_O - 3\Delta f$ and $f_O + 3\Delta f$. While the fundamentals are raised a total of 30 dBm, the harmonics increase 90 dBm, eventually attaining the same amplitude as the fundamentals! Clearly, this must be avoided in a working RF system if spurs are to be rejected at all.

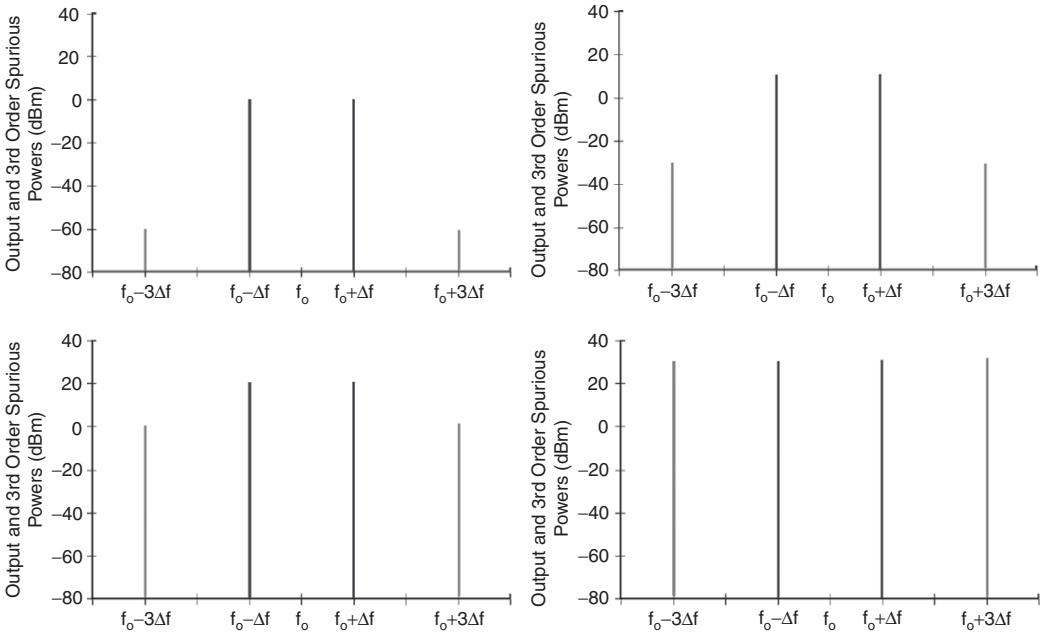


Figure 17.14: Two tone, third order intermodulation intercept amplitudes.

17.12 Noise Figure

The RF noise figure is the same thing as op amp noise, when an op amp is the active element. There is some effect from thermal noise in resistors used in RF systems, but the resistor values in RF systems are usually so small that their noise can be ignored.

Noise for an op amp RF circuit is dependent on the bandwidth being amplified and gain.

This example assumes the 11.5 $nV/\sqrt{Hz}$ op amp. The application is a 10.7 MHz IF amplifier. The signal level is 0 dBV. The gain is unity.

Figure 17.15 is extrapolated from real data. The 1/*f* corner frequency, in this case, is much lower than the bandwidth of interest. Therefore, the 1/*f* noise can be completely discounted (assuming that filtering removes any noise that would cause the amplifier or data converter to saturate). For narrow bandwidths, noise may be quite low! Various bandwidths are shown in Table 17.2.

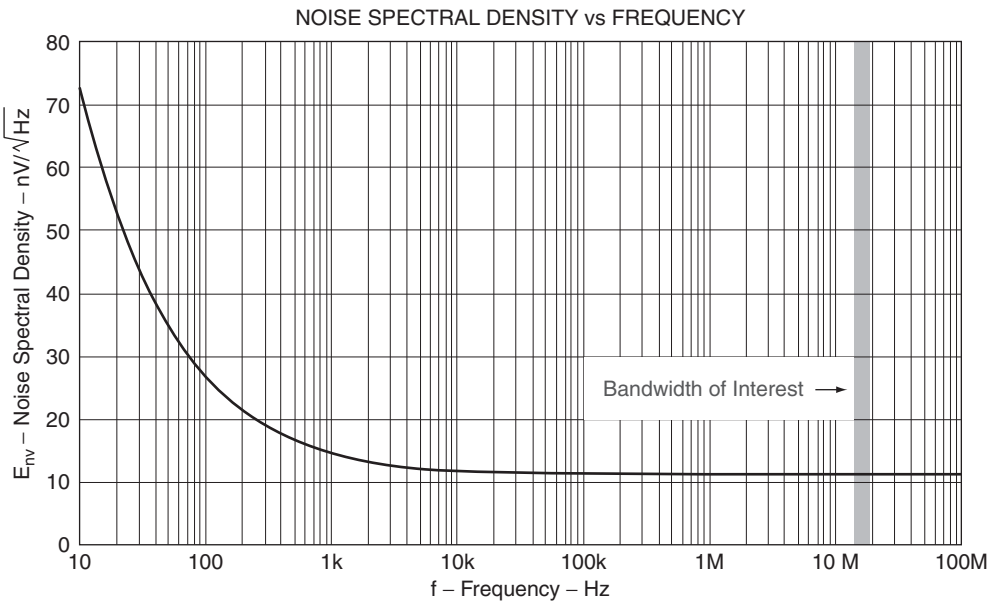


Figure 17.15: Noise bandwidth.

Table 17.2: Noise for Various Bandwidths

Bandwidth	EIN	SNR
280 kHz	6.09 μV	−104.3 dB
230 kHz	5.52 μV	−105.2 dB
180 kHz	4.88 μV	−106.2 dB
150 kHz	4.45 μV	−107.0 dB
110 kHz	3.81 μV	−108.4 dB
90 kHz	3.45 μV	−109.4 dB

Obviously, a slight advantage is to be had from reducing the bandwidth. A lower noise op amp, however, provides greater benefit.

Noise is amplified by the gain of the stage. Therefore, if a stage has high gain, care must be taken to find a low noise op amp. If the gain of a stage is lower, then the noise is not amplified as much, and a less expensive op amp may be suitable.

17.13 Conclusions

Op amps are suitable for RF design, provided that the cost can be justified. They are more flexible to use than discrete transistors, because the biasing of the op amp is independent of the gain and termination. Current feedback amplifiers are more suitable for high frequency, high gain RF design, because they do not have the gain/bandwidth limitation of voltage feedback op amps.

Scattering parameters for RF amplifiers constructed with op amps are very good. Input and output VSWR are good because the effects of termination and matching resistors can be made independent of stage biasing. Reverse isolation is very good, because the RF stage is made of an op amp consisting of dozens or hundreds of transistors, instead of a single transistor. Forward gain is very good with a current feedback amplifier.

Special considerations apply to RF designs that do not normally apply to op amp designs: the phase linearity; the −1 dB compression point (as opposed to voltage rails); the two tone, third order intermodulation intercept; peaking; and noise bandwidth. In just about every case, the performance of an RF stage implemented with op amps is better than one implemented with a single transistor.

CHAPTER 18

Interfacing DACs to Loads

Bruce Carter

18.1 Introduction

A digital to analog converter, DAC, is a component that takes a digital word and converts it to a corresponding analog voltage. It has the opposite function of an analog to digital converter. The DAC is capable of producing only a quantized representation of an analog voltage, not an infinite range of output voltages.

The application almost always dictates the selection of the DAC, leaving the designer the task of interfacing that converter with the output load.

A DAC interfaces with a buffer op amp. Most DACs are manufactured with a process that is incompatible with op amps. Therefore, the op amp cannot be manufactured on the same IC. It must be external, and its characteristics are an integral part of the conversion process. In most cases, the data sheet makes a recommendation for the selection of a buffer op amp. Follow the recommendation, unless there is a compelling reason not to do so. Performance can be improved only if you know exactly what op amp specifications need to be optimized.

All signal conditioning—low pass filtering, DC offsets, and power stages—should be placed after the recommended op amp buffer. Do not attempt to combine these functions with the buffer unless you are an experienced designer with a good grasp of all of the implications.

18.2 Load Characteristics

There are two main types of loads that a DAC may have to drive, AC and DC. Each has different characteristics and requires different interface circuitry.

18.2.1 DC Loads

DC loads include linear actuators such as those used on positioning tables, motors, programmable power supplies, outdoor displays, and lighting systems. Large load currents or high voltages characterize some of these loads. DC accuracy is important, because it is related to a series of desired mechanical positions or intensities in the load device.

18.2.2 AC Loads

AC loads include things like audio chains, frequency generators, IF outputs—any load that does not have a DC component.

18.3 Understanding the DAC and Its Specifications

It is important to understand the DAC and its specifications before discussing interfaces.

18.3.1 Types of DACs—Understanding the Trade-Offs

DACs are available in several types, the most common of which is the resistor ladder type. There are several variations on the resistor ladder technique, with the *R*/2*R* configuration being the most common.

18.3.2 The Resistor Ladder DAC

In the resistor ladder DAC, a precision voltage reference is divided into 2^{N-1} parts in an internal voltage divider, where N is the number of bits specified for the converter. One switch at a time turns on, corresponding to the correct DC level (Figure 18.1).

Unfortunately, the number of resistors and switches doubles for each additional bit of resolution. This means that an 8 bit DAC has 255 resistors and 256 switches, and a 16 bit DAC has 65,535 resistors and 65,536 switches. For this reason, this architecture is almost never used for higher resolution DACs.

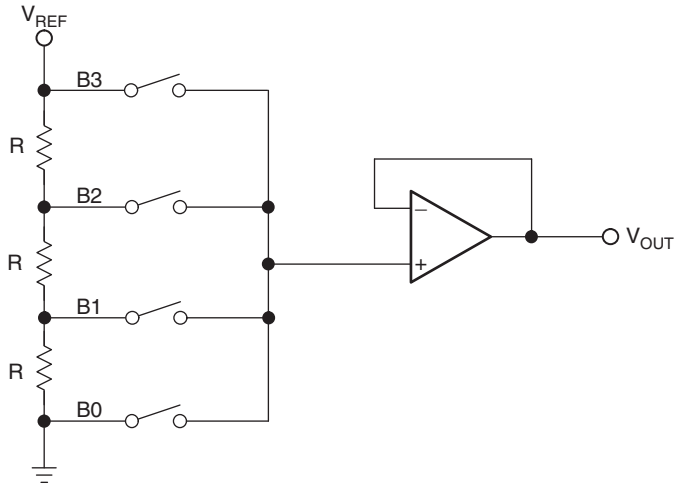


Figure 18.1: Resistor ladder DAC.

18.3.3 The Weighted Resistor DAC

The weighted resistor DAC is very similar to the resistor ladder DAC. In this case, however, each resistor in the string is given a value proportional to the binary value of the bit it represents. Currents are then summed from each active bit to achieve the output (Figure 18.2).

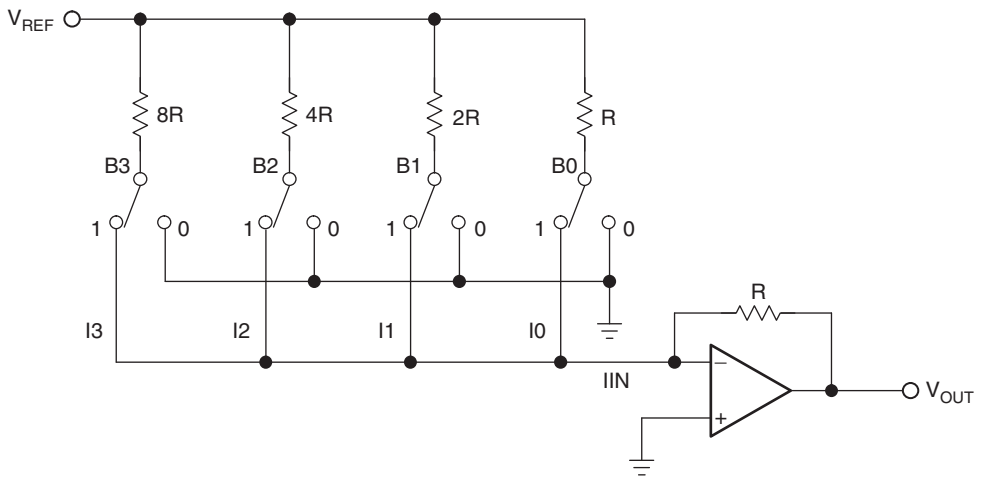


Figure 18.2: Binary weighted DAC.

The number of resistors and switches are reduced to one per bit, but the range of the resistors is extremely wide for high resolution converters, making it hard to fabricate all of them on the IC. The resistor used for B0 in Figure 18.2 is the limiting factor for power dissipation from V_{REF} to ground.

This converter architecture is often used to make logarithmic converters. In this case, the R, $2R$, $4R$, $8R$, ... resistors are replaced with logarithmically weighted resistors.

This type of converter and the $R/2R$ converter described in the next subsection use a feedback resistor fabricated on the DAC IC itself. This feedback resistor is not an optional convenience for the designer—it is crucial to the accuracy of the DAC. It is fabricated on the same silicon as the resistor ladder. Therefore, it experiences the same thermal drift as the resistor ladder. The gain of the buffer amplifier is fixed, with a full scale output voltage limited to V_{REF}. If a different full scale DAC output voltage is needed, change V_{REF}. If the full scale V_{OUT} must exceed the maximum rating of the DAC reference voltage, use a gain stage after the buffer op amp (see Section 18.7.2).

The op amp must be selected carefully, because it is operated in much less than unity gain mode for some combinations of bits. This is probably one of the main reasons why this architecture is not popular, as well as the requirement for a wide range of resistor values for high precision converters.

18.3.4 The $R/2R$ DAC

An $R/2R$ network can be used to make a DAC that has none of the disadvantages of the types mentioned previously (Figure 18.3).

For a given reference voltage, V_{REF}, a current I flows through resistor R. If two resistors, each the same value ($2R$) are connected from V_{REF} to ground, a current $I/2$ flows through each leg of the circuit. But the same current flows if one leg is made up of two resistors, each with the value of R. If two resistors in parallel whose value is $2R$ replace the bottom resistor, the parallel combination is still R. $I/4$ flows through both legs, adding to $I/2$. Extending the network for 4 bits as shown on the right, the total current on the bottom leg is $I/4$ plus $I/8$ plus $I/16$ plus $I/16$ in the resistor to ground. Kirchhoff's current law is satisfied and convenient tap points have been established to construct a DAC (Figure 18.4).

This converter architecture has advantages over the types previously mentioned. The number of resistors has doubled from the number required for the current summing

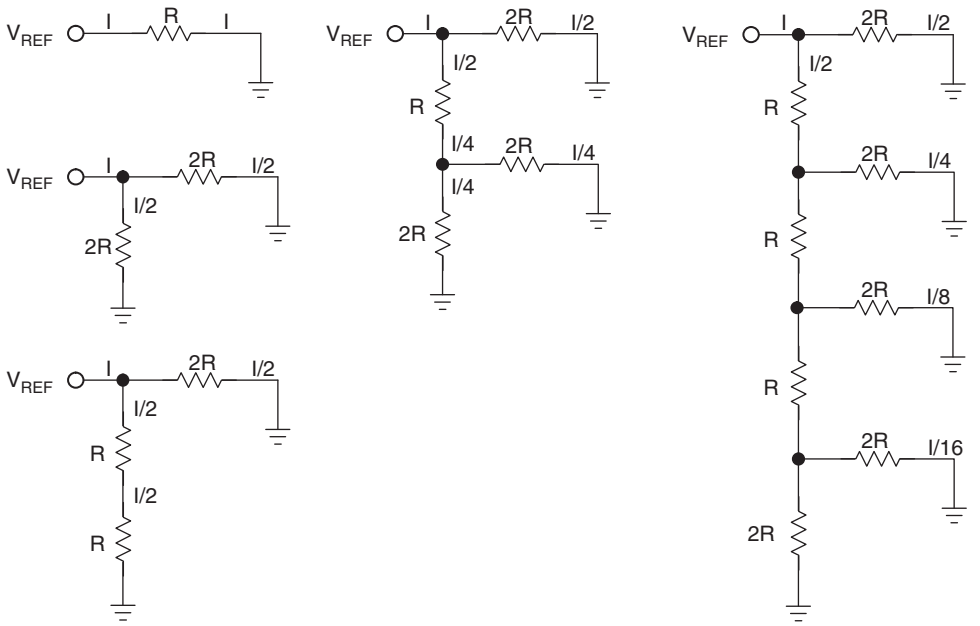


Figure 18.3: R/2R resistor array.

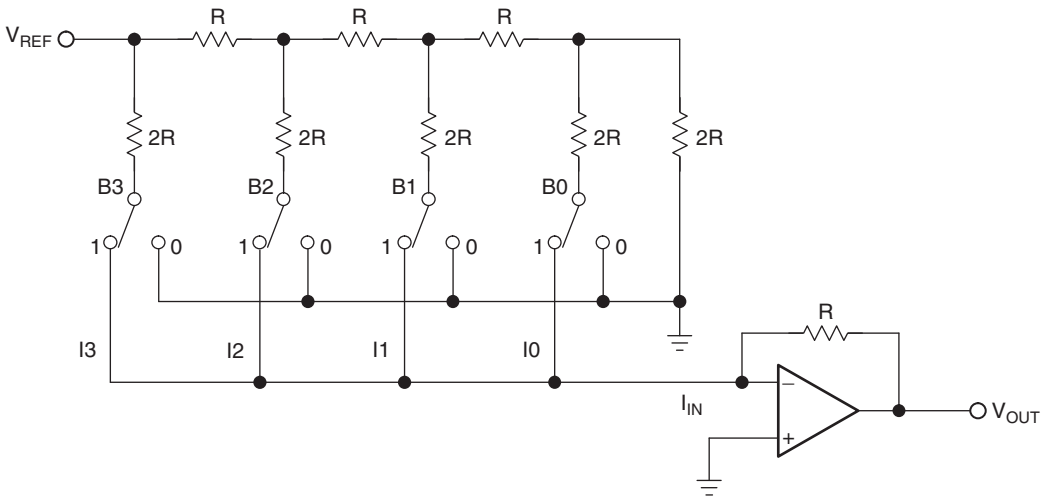


Figure 18.4: R/2R DAC.

type, but there are only two values. Usually, the 2*R* resistors are composed of two resistors in series, each with a value of *R*. The feedback resistor for the buffer amplifier is again fabricated on the converter itself for maximum accuracy. Although the op amp is still not operated in unity gain mode for all combinations of bits, it is much closer to unity gain with this architecture.

The important op amp parameters for all resistor ladder DACs are

- Input offset voltage—the lower the better. It adds to the converter offset error.
- Input bias current—the lower the better. The product of the bias current and the feedback resistance creates an output offset error.
- Output voltage swing—it must meet or, preferably, exceed the zero to full scale swing from the DAC.
- Settling time and slew rate—it must be fast enough to allow the op amp to settle before the next digital bit combination is presented to the DAC input register.

18.3.5 The Sigma Delta DAC

The sigma delta DAC takes advantage of the speed of advanced IC processes to do a conversion as a series of approximations summed together. A phase locked loop (PLL) derived sample clock operates at many times the overall conversion frequency; in the case shown in Figure 18.5, it is 128×. The PLL is used to drive an interpolation filter, a digital modulator, and a 1 bit DAC. The conversion is done by using the density ratio of the voltage out of the 1 bit DAC as the analog signal. As the pattern of ones and zeros is presented to the 1 bit converter, their time average at the sample frequency recreates the analog waveform.

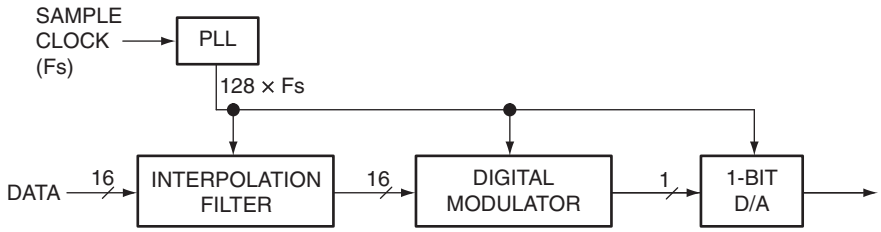


Figure 18.5: Sigma delta DAC.

Sigma delta converters are popular for audio frequencies, particularly CD players. The primary limiting factor is the sample clock. CD players operate at a sample rate of 44.1 kHz, which means that, according to Nyquist sampling theory, the maximum audio frequency that can be reproduced is 22.05 kHz. If an audio frequency of 23.05 kHz is present in the recorded material, it will alias back into the audio output at 1 kHz, producing an annoying whistle. This places a tremendous constraint on the low pass filter following the DAC in a CD player. It must reject all audio frequencies above 22.05 kHz while passing those up to 20 kHz, the commonly accepted upper limit of human hearing. While this can be done in conventional filter topologies, they are extremely complex (nine or more poles). Inevitably, phase shift and amplitude roll-off or ripple starts far below 20 kHz. The original CD players often sounded a bit "harsh" or "dull" because of this.

The solution was to overclock the sample clock. To keep things simple, designers made it a binary multiple of the original sampling frequency. Today, eight times or even higher oversampling is standard in CD players. Little do the audio enthusiasts know that the primary reason why this was done was to substantially reduce the cost of the CD player. A faster sample clock is very cheap. Nine pole audio filters are not. At eight times oversampling, the CD player needs to achieve maximum roll-off at only 352.8 kHz, a very easy requirement. Instead of the filter having to roll off in a mere 2 kHz of bandwidth, now it has 332 kHz of bandwidth to accomplish the roll-off. The sound of an oversampled CD player really is better, but it comes at the cost of increased radiated RFI, coming from the sample clock.

Sigma delta converters introduce a great deal of noise onto the power rails, because the internal digital circuitry is continually switching to the power supply rails at the sample clock frequency f_S.

18.4 DAC Error Budget

The system designer must do an error budget to know how many bits are actually needed to meet the system requirements—how much "graininess" or what step size is acceptable in the output signal.

18.4.1 Accuracy versus Resolution

It is important for the designer to understand the difference between converter accuracy and converter resolution. The number of bits determines resolution of a converter.

Insufficient resolution is not an error—it is a design characteristic of the DAC. If a given converter's resolution is insufficient, use a converter with better resolution (more bits).

Accuracy is the error in the analog output from the theoretical value for a given digital input. Errors are described in the next section. A very common method of compensating for DAC error is to use a converter that has 1 or 2 bits more resolution than the application requires. With the cost of converters coming down and more advanced models being introduced every day, this may be cost effective.

18.4.2 DC Application Error Budget

DC applications depend on the value of DC voltage coming out of the converter. THD and signal to noise ratio are not important, because the frequency coming out of the converter is almost DC.

The resolution of a converter is ±½ LSB, where an LSB is defined as

$$1\ \text{LSB} = \frac{V_{FS}}{2^N - 1} \tag{18.1}$$

where

V_{FS} = Full scale output voltage.

N = Number of converter bits.

The number of bits in a DC system determines the DC step size that corresponds to a bit. Table 18.1 shows the number of bits and the corresponding voltage step size for three popular voltages.

The bit step size can get critical, especially for portable equipment. There is a requirement to operate off of low voltage to minimize the number of batteries. The buffer amplifier, if it includes gain, uses large resistor values, lowering its noise immunity. Fortunately, the vast majority of DC applications are not portable; they are in an industrial environment.

For example, a converter is used to position a drill on a table used to drill PCB holes. The positions of the holes are specified as 0.001 in., ±0.0003 in. The actuators are

Table 18.1: DC Step Size for DACs

Bits	States	3 V	5 V	10 V
4	16	0.1875	0.3125	0.625
8	256	0.011719	0.019531	0.039063
10	1024	0.00293	0.004883	0.009766
12	4096	0.000732	0.001221	0.002441
14	16384	0.000183	0.000305	0.00061
16	65536	4.58 E–05	7.63 E–05	0.000153
18	262144	1.14 E–05	1.91 E–05	3.81 E–05
20	1048576	2.86 E–06	4.77 E–06	9.54 E–06
22	4194304	7.15 E–07	1.19 E–06	2.38 E–06
24	16777216	1.79 E–07	2.98 E–07	5.96 E–07

centered on the table at 0 V, with full negative position of −12 in. occurring at −5 V, and full positive position of +12 in. occurring at +5 V. There are two actuators, one for vertical, and one for horizontal.

This example has several aspects. The first is that the positioning voltage has to swing both positive and negative. In the real world, it may be necessary to add (or subtract in this case) a fixed offset to the DAC output. The output voltage has to swing over a 10 V range, which may mean that the output of the DAC has to be amplified. The actuators themselves probably operate off of higher current than the DAC is designed to provide. Section 18.7 covers some methods for meeting these requirements.

Assume, for now, that the DAC has the necessary offset and gain. A ±12 in. position is 24 in. total, which corresponds to ±5 V from the DAC circuitry. The 24 in. range must be divided into equal 0.0003 in. steps to meet the resolution requirement, which is 80,000 steps. From Table 18.1, an 18 bit DAC is required. The actual system is able to position with a step size of 0.0000916 in. Two independent conversion systems are needed, one for horizontal and one for vertical.

18.4.3 AC Application Error Budget

The error budget for an AC application most likely is specified as total harmonic distortion, dynamic range, or signal to noise ratio. Assuming no internal noise and no noise in the buffer op amp circuitry, the inverse of the dynamic range is the SNR of the DAC. Of course, noise is always present and is measured with all input data set to zero. Noise makes the SNR decrease.

The number of converter bits, however, is the overwhelming factor determining these parameters. Technically, they are not "errors," because the design of the converter sets them. If the designer cannot live with these design limits, the only choice is to specify a converter with better resolution (more bits).

Total Harmonic Distortion

The total harmonic distortion of an ideal DAC is the quantization noise due to the converter resolution. The number of bits of the converter determines the lowest possible total harmonic distortion. The greater is the number of bits, the lower the amplitude of the harmonics, as shown in Figure 18.6.

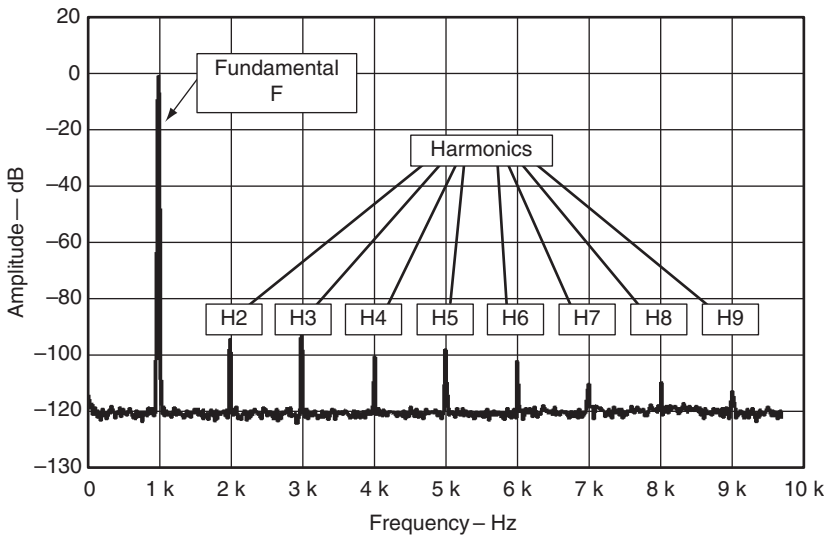


Figure 18.6: Total harmonic distortion.

Assuming ideal digital to analog conversion, there is a direct relationship between the number of bits and the THD caused by the resolution:

$$\text{THD}(\%) = \frac{1}{2^N} \times 100 \tag{18.2}$$

where N is the number of converter bits. Of course, this is the limit for ideal conversion.

Dynamic Range

There is also a direct relationship between the number of bits (N) and the maximum dynamic range of the DAC, Equation (18.2) and Table 18.2:

Table 18.2: Converter Bits, THD, and Dynamic Range

Bits	States	THD	Dynamic range
4	16	6.25%	25.8
8	256	0.390625%	49.9
10	1024	0.097656%	62.0
12	4096	0.024414%	74.0
14	16,384	0.006104%	86.0
16	65,536	0.001526%	98.1
18	262,144	0.000381%	110.1
20	1,048,576	0.000095%	122.2
22	4,194,304	0.000024%	134.2
24	16,777,216	0.000006%	146.2

$$\text{Dynamic range} = 6.02 \times N + 1.76 \tag{18.3}$$

Note that there is approximately a 6 dB improvement in dynamic range per bit. This is an easy way to figure out what improvement can be realized by increasing the number of bits from one value to another.

For example, if the designers of a CD player want to have a 90 dB SNR, they would pick a 16 bit converter from Table 18.2. The THD is 0.0015% minimum.

18.4.4 RF Application Error Budget

RF applications are a high frequency subset of AC applications. RF applications may be concerned with the position and relative amplitude of various harmonics. Minimizing one harmonic at the expense of another may be acceptable if the overall RF spectrum is within specified limits.

18.5 DAC Errors and Parameters

The DAC errors described in this section add to the errors caused by the resolution of the converter.

The section is divided into DC and AC sections, but many of the DC errors masquerade as AC errors. A given DAC may or may not include either DC or AC error specifications. This should give the designer a clue that the device is optimized for DC or AC applications. Like any component, DACs are designed with trade-offs. It is possible to misapply a converter meant for high frequency AC operation in a DC application and so forth.

18.5.1 DC Errors and Parameters

The following are some DAC DC errors and parameters.

Offset Error

The analog output voltage range for the complete range of input bits may be shifted linearly from the ideal 0 to the full scale value (Figure 18.7). The offset error is the $\pm\Delta V$ from 0 V that results when a digital code is entered that is supposed to produce 0.

Related to the offset error is the offset error temperature coefficient, which is the change in offset over temperature. This is usually specified in pulse position modulation per degree Centigrade.

The offset error is critical in DC applications. For this reason, a buffer op amp must be selected that does not contribute to the problem—its own offset voltages should be

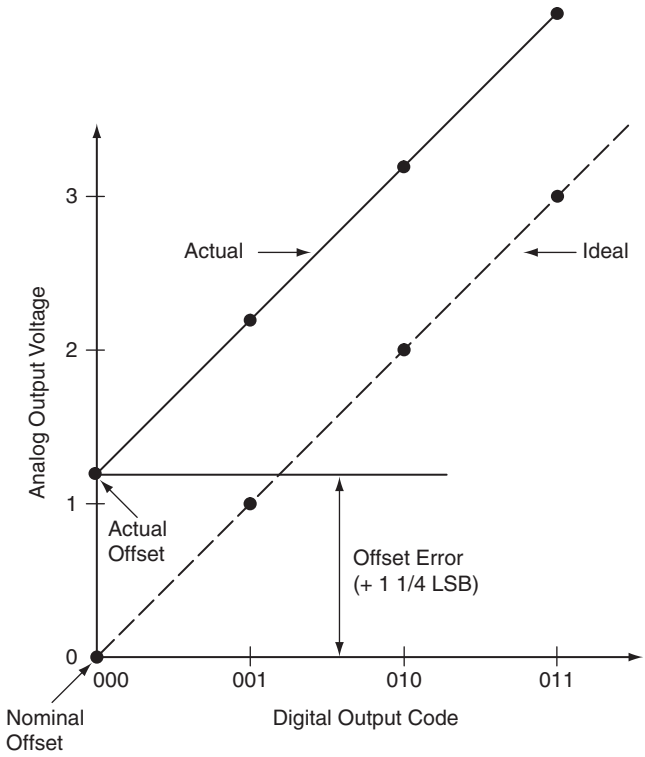


Figure 18.7: DAC offset error.

much less than that of the converter. In AC applications, the offset error is not important and can be ignored. The buffer op amp can be selected for low THD, high slew rate, or whatever other parameters are important for the application.

Gain Error

The gain of the DAC may greater than or less than the gain needed to produce the desired full scale analog voltage (Figure 18.8). The gain error is the difference in slope between the ideal DAC output gain and the actual gain.

Related to the gain error is the gain error temperature coefficient, which is the change in gain over temperature.

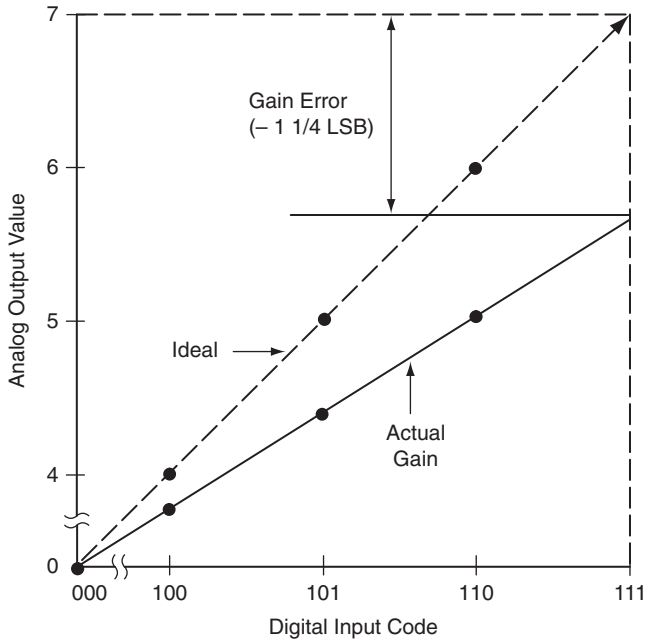


Figure 18.8: DAC gain error.

The gain error can be critical in both AC and DC applications. For example,

- An RF predriver must not cause the output stage to exceed FCC license requirements.
- A mechanical positioner must not stop short of or go past its intended position.

The op amp buffer should be operated with the internal feedback resistor. If possible, full scale amplitude adjustments should be made to V_{REF}. This way, tolerances and thermal drift in external resistors do not contribute to the gain error.

Differential Nonlinearity Error

When the increase in output voltage (ΔV) is not the same for every combination of bits, the converter has a differential nonlinearity error (DNL). If the DNL exceeds 1 LSB, the converter is nonmonotonic. This can cause a problem for some servo control loops. A nonmonotonic DAC would appear in Figure 18.9 as a momentary dip in the analog output characteristic.

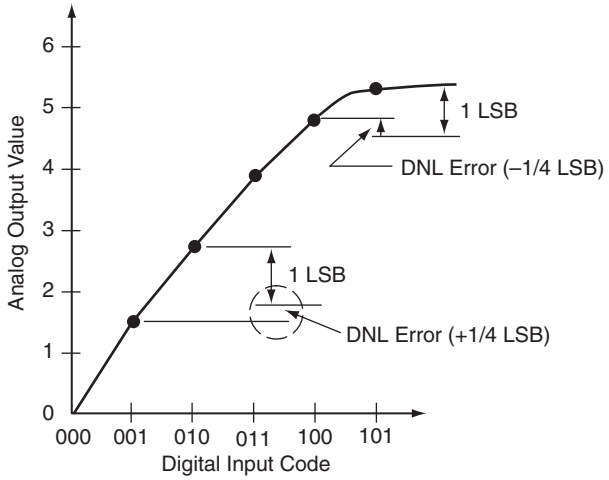


Figure 18.9: Differential nonlinearity error.

Integral Nonlinearity Error

The integral nonlinearity error is similar to the differential nonlinearity error, except it is a first order effect that stretches across the entire range from 0 to full scale output voltage (Figure 18.10).

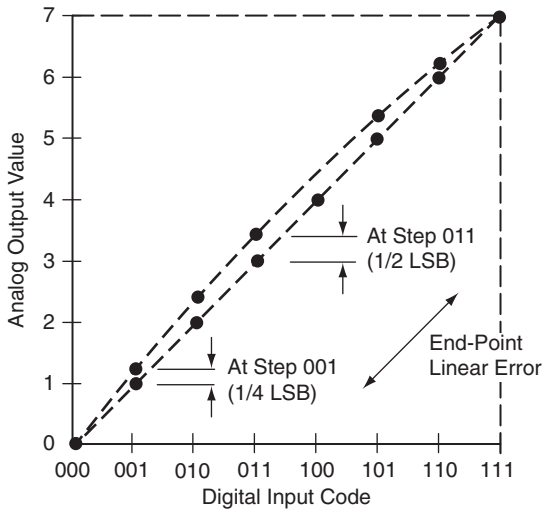


Figure 18.10: Integral nonlinearity error.

Both the INL and DNL errors affect AC applications as distortion and spectral harmonics (spurs). In DC applications, they result in an error in the DC output voltage. The mechanical steps of a positioning table, for instance, may not be in exact increments.

Power Supply Rejection Ratio

The power supply rejection ratio is sometimes called the *power supply sensitivity*. It is the ability of the converter to reject ripple and noise on its power inputs. DC applications may not be adversely affected. Poor power supply rejection can cause spurs and harmonic distortion in AC applications, as external frequency components leak into the output and modulate with it. The designer must decouple the DAC and buffer op amp carefully to combat these problems.

18.5.2 AC Errors and Parameters

The following are DAC AC errors and parameters.

THD + N

Some noise is always generated internally in the converter and buffer amp. A useful specification for audio and communication system designers is the THD + N (total harmonic distortion plus noise). The distortion plus noise (THD + N) is the ratio of the sum of the harmonic distortion and noise to the rms power of the input signal. As is the case with op amp parameters (Chapter 13), the noise sources add according to the root mean square law. The distortion and noise are measured separately then added together to form the ratio. The noise voltage relates to the measured bandwidth.

SINAD

The signal to noise and distortion (SINAD) ratio is the ratio of the input signal to the sum of the harmonic distortion and noise. The distortion and noise are measured separately then added together to form the ratio. The SINAD is the reciprocal to the THD + N. The SINAD and THD + N are a good indication of the overall dynamic performance of the ADC, because all components of noise and distortion are included.

ENOB

The SINAD is used to determine the *effective number of bits* (ENOB) of accuracy the converter displays at that frequency. For example, a nominal 8 bit resolution DAC may be specified as having 45 dB SNR at a particular input frequency. The number of effective bits is defined as

$$\text{ENOB} = \frac{\text{SNR}_{\text{REAL}} - 1.76}{6.02} = 7.2 \text{ bits} \tag{18.4}$$

The actual performance of the device is therefore less than its nominal resolution at this frequency.

Spurious Free Dynamic Range

Spurious free dynamic range is the difference in decibels between the maximum signal component and the largest distortion component (Figure 18.11). It is an important specification in RF applications, where FCC regulations specify the magnitude of spurs.

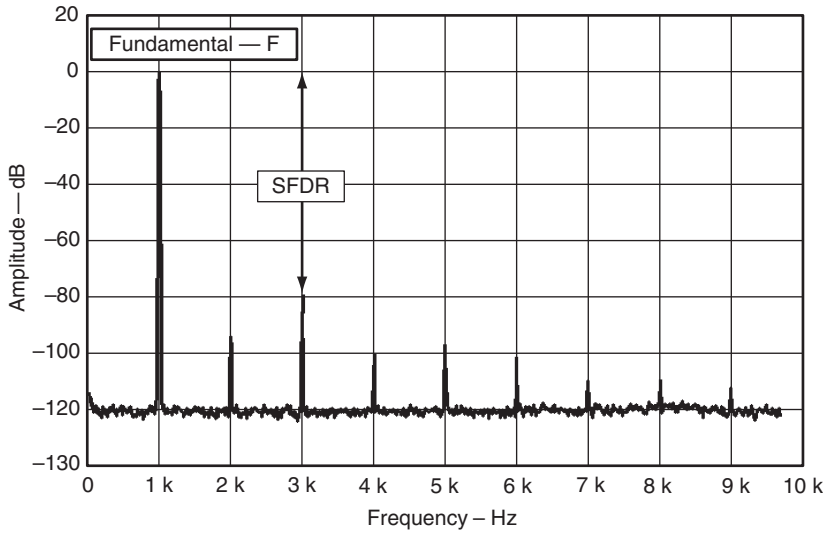


Figure 18.11: Spurious free dynamic range.

Improper decoupling may cause spurs. A notch filter can be used to eliminate a spur, but many RF applications are RF agile—changing the frequency of the spur as well. The notch must catch all spur frequencies or it is useless.

Intermodulation Distortion

The differential and integral nonlinearity errors described previously appear in a high frequency AC application as intermodulation distortion (Figure 18.12).

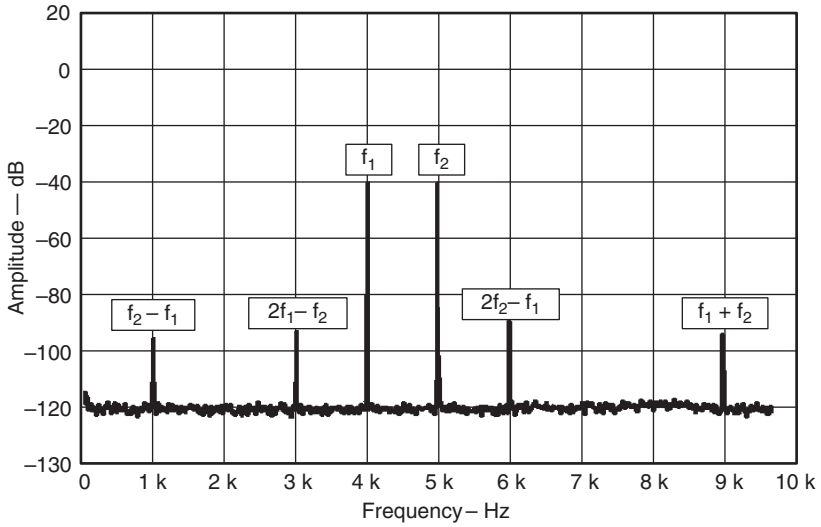


Figure 18.12: Intermodulation distortion.

The best method of combating intermodulation distortion is to make the buffer amplifier system as linear as possible (beware of rail to rail op amps that may not be linear near the voltage rails). Try to limit current through the internal feedback resistor in the DAC. See Section 18.7.1 on increasing the voltage rail for suggestions about reducing internal feedback resistor power dissipation.

Settling Time

The settling time of a DAC is the time between the switching of the digital inputs of the converter and when the output reaches its final value and remains within a specified error band (Figure 18.13). Settling time is the reciprocal of the maximum DAC conversion rate.

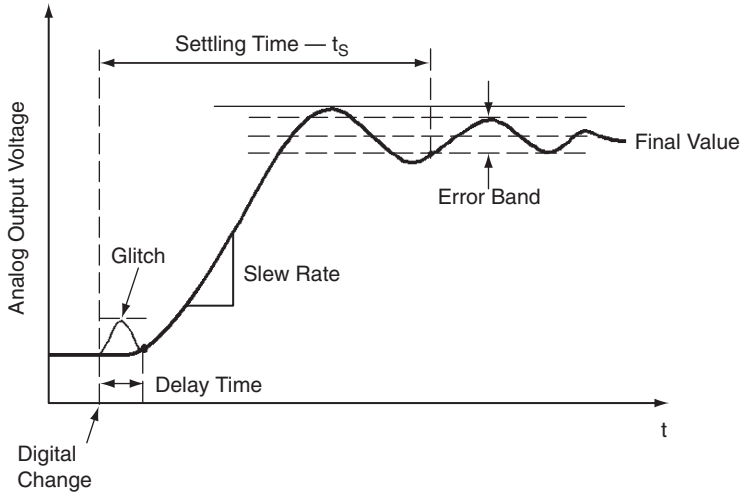


Figure 18.13: DAC settling time.

When an output buffer op amp is used with a DAC, it becomes a part of the settling time/conversion rate calculations.

Related to the settling time is a glitch response that occurs when the digital code changes state. Even though this effect is transitory in nature, it can result in noise or harmonics when used in fast AC applications. The best way of reducing the glitch is to properly decouple the DAC and op amp buffer (see Chapter 23). In extreme cases, a deglitching circuit may be needed (Figure 18.14).

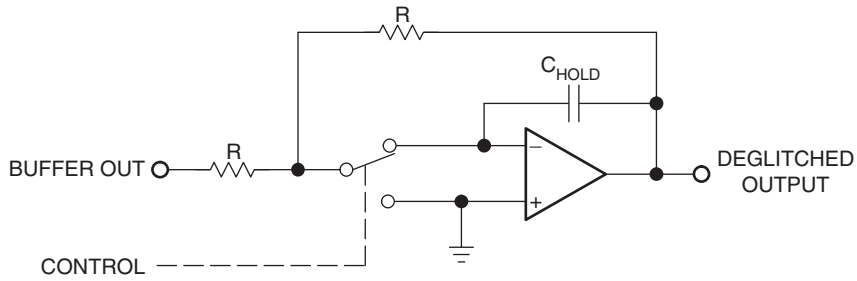


Figure 18.14: DAC deglitch circuit.

This technique relies on the software designer to balance the timing of the control signal so it activates the hold function right before the DAC input code changes then releases the hold right after the code has changed. The selection of C_{HOLD} is critical—it must hold the buffer output without droop and without compromising system bandwidth.

18.6 Compensating for DAC Capacitance

DACs are constructed of either bipolar or CMOS technology, with CMOS being the more common. CMOS transistors, however, have a lot of capacitance. This capacitance adds in DACs, depending on the number of resistors switched on or off. Capacitance at an inverting op amp input is a good way to cause it to oscillate, especially since some buffer amplifiers are operated at less than unity gain. The converter capacitance, C_O, must be compensated for externally (Figure 18.15).

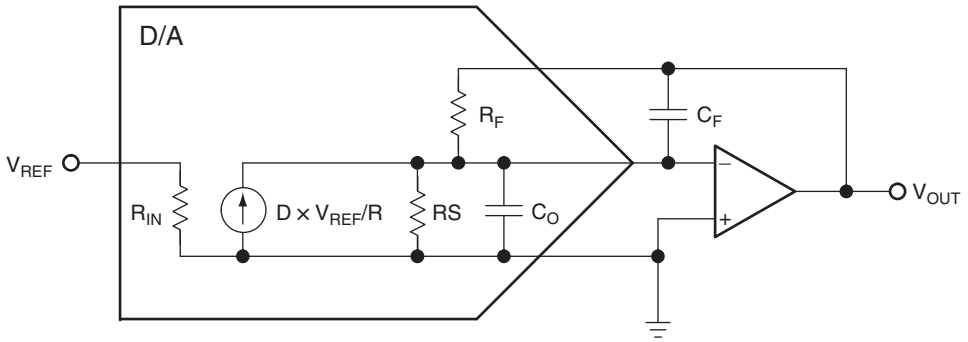


Figure 18.15: Compensating for CMOS DAC output capacitance.

The normal technique for compensating the buffer amplifier for output capacitance is to add a feedback capacitor, C_F. C_F is calculated by the following:

$$C_F = 2 \times \sqrt{\frac{C_O}{2\pi R_F} \times \frac{1}{G_{BW}}} \tag{18.5}$$

where

C_O = the output capacitance from the DAC data sheet.

R_F = the feedback resistance from the DAC data sheet.

G_{BW} = the small signal unity gain bandwidth product of the output amplifier.

Unfortunately, both the feedback capacitors, C_F, and the internal DAC capacitance, C_O, limit the conversion speed of the DAC. If faster conversion is needed, a DAC with a lower output capacitance, and therefore a lower feedback compensation capacitor, is needed. The overall settling time with the external capacitance is

$$T_S \approx \sqrt{\frac{R_F(C_O + C_F)}{2G_{\mathrm{BW}}}} \tag{8.6}$$

where

C_O = the DAC internal capacitance.

R_F = the feedback resistor.

C_F = the compensation capacitance.

G_{BW} = the small signal unity gain bandwidth product of the output amplifier.

18.7 Increasing Op Amp Buffer Amplifier Current and Voltage

Process limitations of op amps limit the power that can be dissipated at the output. Unfortunately, some applications require the DAC to interface to loads that dissipate considerable power. These include actuators, position solenoids, stepper motors, loudspeakers, vibration tables, positioning tables—the possibilities are endless.

While several "power op amps" are available that can drive heavy loads, they usually compromise several other specifications to achieve the high power operation. Input voltage offset, input current, and input capacitance can be decades higher than the designer is accustomed to and make these power op amps unsuitable for direct interface with a DAC as a replacement for the buffer op amp.

The power booster stage can be designed discretely or a prepackaged amplifier of some sort, depending on what is needed for the application. Sometimes, high current is required for driving loads such as actuators and stepper motors. Audio applications can require a lot of wattage to drive loudspeakers. This implies a higher voltage rail than op amps commonly operate at. This and other high voltage applications can operate off of and generate lethal voltages. The designer needs to be extremely careful not to create an unsafe product or be electrocuted while developing it.

The power stage is most often included in the feedback loop of the op amp circuit, so that the closed loop can compensate for power stage errors. This is not always possible if the voltage swing of the output exceeds that of the op amp voltage rails. In these cases, a voltage divided version of the output should be used.

The three broad categories of booster are current boosters, voltage boosters, and boosters that do both. All of them work on the same principle: Anything put inside the feedback loop of the op amp is compensated for—the output voltage swings to whatever voltage it needs to make the voltage at the buffer op amp inputs equal.

18.7.1 Current Boosters

Current boosters usually use some variation of the class-B push/pull amplifier topology (Figure 18.16).

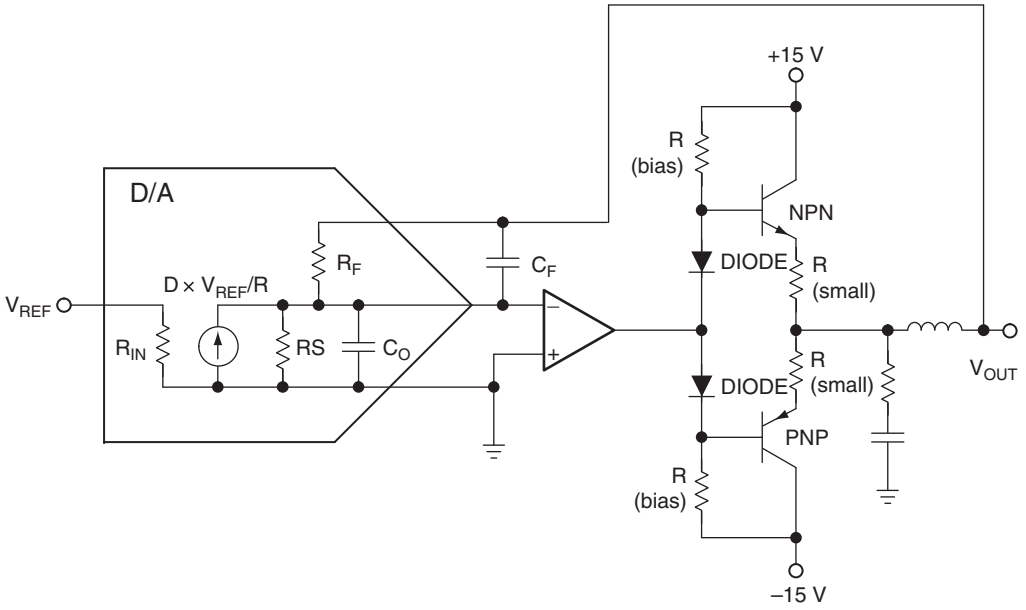


Figure 18.16: DAC output current booster.

The circuit in Figure 18.16 has been employed for decades—many resources are available to design exact component values. It boosts current because the output impedance of the op amp has been bypassed and used as the driver for the base of

the npn and pnp power transistors. The two diodes compensate for the VBE drop in the transistors, whose bases are biased by two resistors off of the supplies. The output of the booster stage is fed back to the feedback resistor in the DAC to complete the feedback loop. The output impedance of the stage is limited by only the characteristics of the output transistors and small emitter resistors. Modern power transistors have such high frequency response that this circuit may oscillate. The RC snubber network and a small inductor in series with the load can be used to damp the oscillation—or be omitted if oscillation is not a problem. Beware of varying transistor betas, however.

18.7.2 Voltage Boosters

If even more current is needed or the output voltage swing must be more than ±15 V, the booster stage can be operated at voltages higher than the buffer amplifier potentials. A designer might be tempted to try the circuit of Figure 18.17.

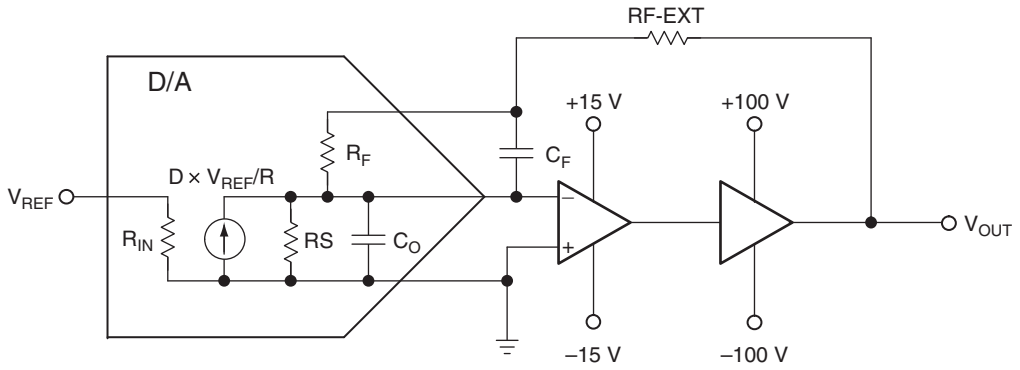


Figure 18.17: Incorrect method of increasing voltage swing of DACs.

Any time there are higher voltage rails on the output section, there are potential hazards. This circuit illustrates a common misapplication:

- The whole reason for using the booster amp is to allow the V_{OUT} to swing to a ±100 V rail. If this circuit is operated in the unity gain mode (external $R_F = 0$), the V_{OUT} swings only ±15 V maximum. There is no need for the ±100 V rail. That voltage rail is there to allow voltage gain.

- If the circuit is operated with a gain (external R larger than 0), the external R_F adds to the internal R_F to create the gain:

$$\text{Gain} = \frac{R_{\text{F,EXT}} + R_{F,\text{INT}}}{R_{\text{S}}} \tag{18.7}$$

The problem with this is that the wattage of the resistors increases as the external voltage rail increases. The designer has control over the wattage of the external R_F but no control whatsoever over internal R_F or R_S. Because these resistors are fabricated on the IC, their wattage is limited. Even if the wattage rating of the internal resistors is meticulously observed, they may have undesirable thermal coefficients if allowed to dissipate that wattage. Resistor self-heating changes the resistance according to its rated temperature coefficient (maximum). The external resistor is sure to have a different thermal coefficient from the internal resistors, causing a gain error. The designer may never have encountered the effects of resistor self-heating before, because through hole and surface mount devices have enough bulk to minimize the effect of self-heating. At the geometries present on IC DACs, resistor self-heating is a much more pronounced effect. It produces a nonlinearity error in the DAC output.

This effect is most pronounced in high resolution converters, where the geometry is the smallest. The designer, therefore, must limit the current in the feedback resistor if at all possible. Figure 18.18 shows a method of achieving gain control while keeping the high current path out of the internal feedback resistor.

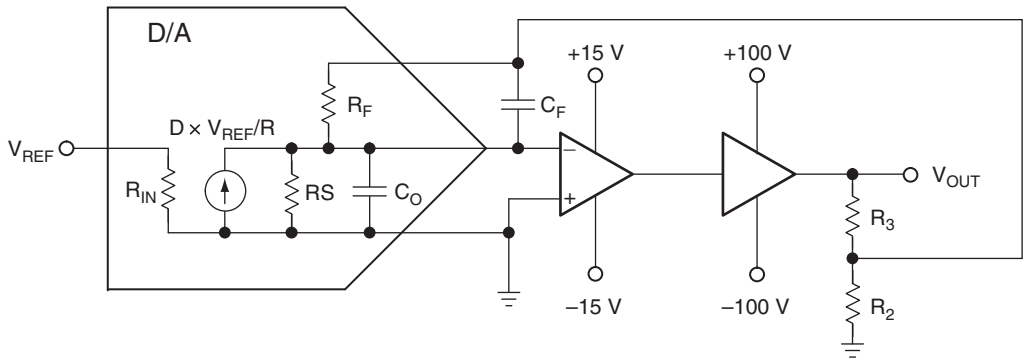


Figure 18.18: Correct method of increasing voltage range.

In Figure 18.18,

- R_3 and R_2 are selected to ensure that the feedback voltage to the DAC internal R_F can never exceed the DAC rated limits.
- R_3 and R_2, of course, have to be the correct power rating. R_2, in particular, has to be carefully selected. If it burns out, the feedback loop presents hazardous voltages to the DAC. R_3, which drops the bulk of the voltage, has to dissipate considerable wattage.

If the combination of voltage swing and power ratings cannot be balanced to achieve a working design, the only choice left to the designer is to break the feedback loop and live with the loss of accuracy. For AC applications, this may be acceptable.

18.7.3 Power Boosters

The preceding two types of boosters can, of course, be combined to produce more power. In audio applications, for example, a ± 15 V power supply limits the output power to 112.5 W, absolute maximum, into an 8 Ω load. To increase the power, the voltage rails must also be increased, with all of the cautions of the previous subsection observed.

18.7.4 Single Supply Operation and DC Offsets

A DAC power circuit is not the right place to try to apply single supply design techniques. In audio applications, a single supply design forces a large coupling capacitor, which distorts and limits low frequency response. In DC applications, a DC offset continually drives the load, which has to dissipate the excess voltage through its internal resistance as heat.

Nevertheless, some applications may require a DC offset. The designer is fortunate in that a precision reference is already available in the circuit. The reference drives the resistor network in the DAC and may be external or internal to it. In most cases, an internal reference is brought out to a pin on the device. It is important for the designer not to load the reference excessively, as that directly affects DAC accuracy (Figure 18.19).

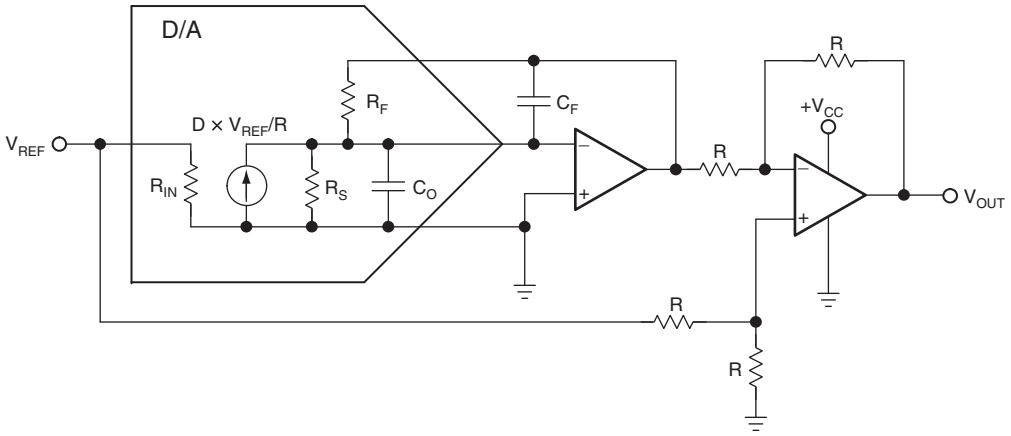


Figure 18.19: Single supply DAC operation.

In the circuit in Figure 18.19, the output of the buffer amplifier is shifted up in DC level by 1/2 V_{REF} (not 1/2 V_{CC}). V_{REF} is selected because it is much more stable and accurate than V_{CC}. The four resistors in the level shifter circuit must be highly accurate and matched, or this circuit will contribute to gain and offset errors. Thermal errors, however, cannot be compensated for, because the external resistors are probably going to have a different thermal drift than those on the IC. This technique is limited to applications that will see only a small change in ambient temperature.

CHAPTER 19

Sine Wave Oscillators

Ron Mancini and Richard Palmer

19.1 What Is a Sine Wave Oscillator?

Op amp oscillators are circuits that are unstable—not the type that are sometimes unintentionally designed or created in the lab, but circuits intentionally designed to remain in an unstable state. Oscillators are useful for creating uniform signals that are used as a reference in applications such as audio, function generators, digital systems, and communication systems.

Two general classes of oscillators exist: sinusoidal and relaxation. Sinusoidal oscillators consist of amplifiers with RC (resistance/capitance) or LC (inductance/capitance) circuits that have adjustable oscillation frequencies or crystals that have a fixed oscillation frequency. Relaxation oscillators generate triangular, sawtooth, square, pulse, or exponential waveforms; and they are not discussed here.

Op amp sine wave oscillators operate without an externally applied input signal. Some combination of positive and negative feedback is used to drive the op amp into an unstable state, causing the output to transition back and forth at a continuous rate. The amplitude and the oscillation frequency are set by the arrangement of passive and active components around a central op amp.

Op amp oscillators are restricted to the lower end of the frequency spectrum because op amps do not have the required bandwidth to achieve low phase shift at high frequencies. Voltage feedback op amps are limited to the low kilohertz range, since their dominant, open loop pole may be as low as 10 Hz. The new current feedback op amps have a much wider bandwidth, but they are very hard to use in oscillator circuits, because they are sensitive to feedback capacitance and are beyond the scope of this chapter.

Crystal oscillators are used in high frequency applications up to the hundreds of megahertz range.

19.2 Requirements for Oscillation

The canonical, or simplest form, of a negative feedback system is used to demonstrate the requirements for oscillation to occur. The block diagram of this system is shown in Figure 19.1, and the corresponding classic expression for a feedback system is shown in Equation (19.1). The derivation and explanation of the block diagram and equation can be found in Chapter 6.

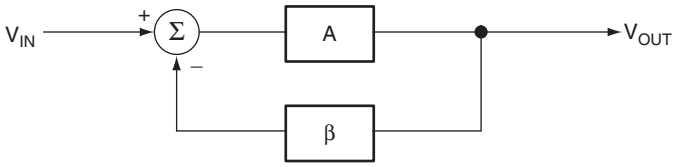


Figure 19.1: Canonical form of a feedback system with positive or negative feedback.

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{19.1}$$

Oscillators do not require an externally applied input signal but instead use some fraction of the output signal created by the feedback network as the input signal. It is the noise voltage that provides the initial boost signal to the circuit when positive feedback is employed. Over a period of time, the output builds up, oscillating at the frequency set by the circuit components [1].

Oscillation results when the feedback system is not able to find a stable state because its transfer function cannot be satisfied. The system becomes unstable when the denominator in Equation (19.1) is 0. When $(1 + A\beta) = 0$, $A\beta = -1$. The key to designing an oscillator, then, is to ensure that $A\beta = -1$. This is called the *Barkhausen criterion*. This constraint requires the magnitude of the loop gain be 1 with a corresponding phase shift of 180°, as indicated by the minus sign. An equivalent expression using complex math is $A\beta = 1\angle{-180}°$ for a negative feedback system. For a positive feedback system, the expression becomes $A\beta = 1\angle 0°$ and the sign is negative in Equation (19.1).

Once the phase shift is 180° and $A\beta = |1|$, the output voltage of the unstable system heads for infinite voltage in an attempt to destroy the world and is prevented from succeeding only by an energy limited power supply. When the output voltage approaches either power rail, the active devices in the amplifiers change gain, causing the value of A to change so the value of $A\beta \neq 1$; therefore the charge to infinite voltage slows down and eventually halts. At this point, one of three things can occur. First, nonlinearity in saturation or cutoff can cause the system to become stable and lock up at the power rail. Second, the initial charge can cause the system to saturate (or cut off) and stay that way for a long time before it becomes linear and heads for the opposite power rail. Third, the system stays linear and reverses direction, heading for the opposite power rail. Alternative 2 produces highly distorted oscillations (usually quasi square waves), and the resulting oscillators are called *relaxation oscillators*. Alternative 3 produces sine wave oscillators.

19.3 Phase Shift in the Oscillator

The 180° phase shift in the equation $A\beta = 1\angle{-180°}$ is introduced by active and passive components. Like any well designed feedback circuit, oscillators are made dependent on passive component phase shift, because it is accurate and almost drift free. The phase shift contributed by active components is minimized because it varies with temperature, has a wide initial tolerance, and is device dependent. Amplifiers are selected such that they contribute little or no phase shift at the oscillation frequency. These constraints limit the op amp oscillator to relatively low frequencies.

A single pole RL or RC circuit contributes up to 90° phase shift per pole, and because 180° of phase shift is required for oscillation, at least two poles must be used in the oscillator design. An LC circuit has two poles, thus it contributes up to 180° phase shift per pole pair. But LC and LR oscillators are not considered here because low frequency inductors are expensive, heavy, bulky, and very nonideal. LC oscillators are designed in high frequency applications, beyond the frequency range of voltage feedback op amps, where the inductor size, weight, and cost are less significant. Multiple RC sections are used in low frequency oscillator design in lieu of inductors.

Phase shift determines the oscillation frequency because the circuit oscillates at the frequency that accumulates 180° phase shift. The rate of change of phase with frequency, $d\varphi/d\omega$, determines frequency stability. When buffered RC sections (an op amp buffer provides high input and low output impedance) are cascaded, the phase shift multiplies by the number of sections, n (see Figure 19.2).

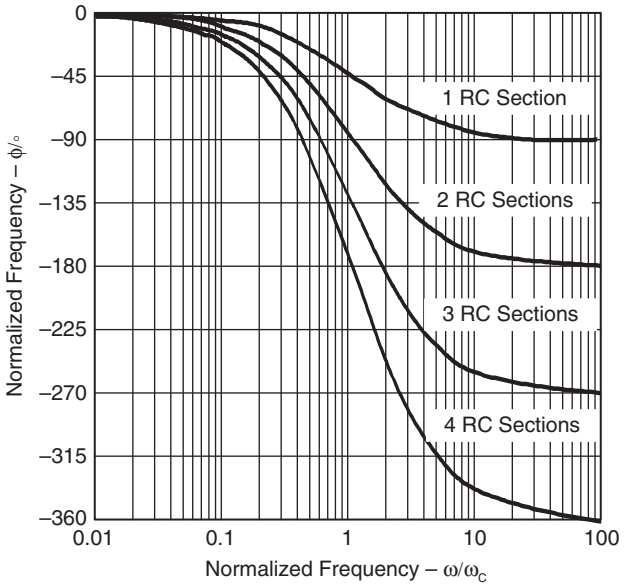


Figure 19.2: Phase plot of RC sections.

The frequency of oscillation is very dependent on the change in phase at the point where the phase shift is 180°. A tight frequency specification requires a large change in phase shift, $d\varphi$, for a small change in frequency, $d\omega$, at 180°. Figure 19.2 demonstrates that, although two cascaded RC sections eventually provide 180° phase shift, $d\varphi/d\omega$ at the oscillator frequency is unacceptably low. Thus, oscillators made with two cascaded RC sections have poor frequency stability. Three equal cascaded RC filter sections have a much higher $d\varphi/d\omega$ (see Figure 19.2), and the resulting oscillator has improved frequency stability. Adding a fourth RC section produces an oscillator with an excellent $d\varphi/d\omega$ (see Figure 19.2); so this is the most stable RC oscillator configuration. Four sections are the maximum number used because op amps come in quad packages, and the four section oscillator section yields four sine waves 45° phase shifted relative to each other. This oscillator can be used to obtain sine/cosine or quadrature sine waves.

Crystal or ceramic resonators make the most stable oscillators, because resonators have an extremely high $d\varphi/d\omega$ resulting from their nonlinear properties. Resonators are used for high frequency oscillators, but low frequency oscillators do not use resonators because of size, weight, and cost restrictions. Op amps are not generally used with crystal or ceramic resonator oscillators because op amps have low bandwidth.

Experience shows that it is more cost effective to build a high frequency crystal oscillator, count the output down, and filter the output to obtain a low frequency than it is to use a low frequency resonator.

19.4 Gain in the Oscillator

The oscillator gain must equal 1 ($A\beta = 1\angle{-180}^\circ$) at the oscillation frequency. Under normal conditions, the circuit becomes stable when the gain exceeds 1 and oscillations cease. However, when the gain exceeds 1 with a phase shift of –180°, the active device nonlinearity reduces the gain to 1 and the circuit oscillates. The nonlinearity happens when the amplifier swings close to either power rail because cutoff or saturation reduces the active device (transistor) gain. The paradox is that worst case design practice requires nominal gains exceeding 1 for manufacturability, but excess gain causes more distortion of the output sine wave.

When the gain is too low, oscillations cease under worst case conditions; and when the gain is too high, the output waveform looks more like a square wave than a sine wave. Distortion is a direct result of excess gain overdriving the amplifier; hence gain must be carefully controlled in low distortion oscillators. Phase shift oscillators have distortion, but they achieve low distortion output voltages because cascaded RC sections act as distortion filters. Also, buffered phase shift oscillators have low distortion because the gain is controlled and distributed among the buffers.

Most circuit configurations require an auxiliary circuit for gain adjustment when low distortion outputs are desired. Auxiliary circuits range from inserting a nonlinear component in the feedback loop, to automatic gain control (AGC) loops, to limiting by external components such as resistors and diodes. Consideration must also be given to the change in gain due to temperature variations and component tolerances, and the level of circuit complexity is determined based on the required stability of the gain. The more stable the gain, the better the purity of the sine wave output.

19.5 Active Element (Op Amp) Impact on the Oscillator

Up to this point it has been assumed that the op amp has an infinite bandwidth and the output is not frequency dependent. In reality, the loop gain, Aβ, of the circuit is frequency dependent. Figure 19.3 shows the typical gain versus frequency response of op amps. Dividing the numerator and denominator of Equation 19.1 by Aβ yields Equation 19.2, the closed loop gain (A_{CL}), where 1/β represents the ideal closed

loop gain ($A_{CLideal}$). Normally, the bandwidth of the system is specified where $A_{CLideal}$ intersects the open loop gain (A_{OL}) rolloff. This is the point, f_0, where $A_{CLideal}$ is attenuated by 3 dB and is normally drooping at a rate of 20 dB per decade. Even worse, the phase shift contributed by the op amp is 45° at this point. This is true at whatever point the gain of the circuit intercepts the open loop gain rolloff of the op amp. Clearly this region of operation must either be avoided or be compensated for by the circuit.

$$A_{CL} = \frac{A}{1 + A\beta} = \frac{\frac{1}{\beta}}{1 + \frac{1}{A\beta}} = \frac{A_{CLideal}}{1 + \frac{A_{CLideal}}{A_{OL}}} \tag{19.2}$$

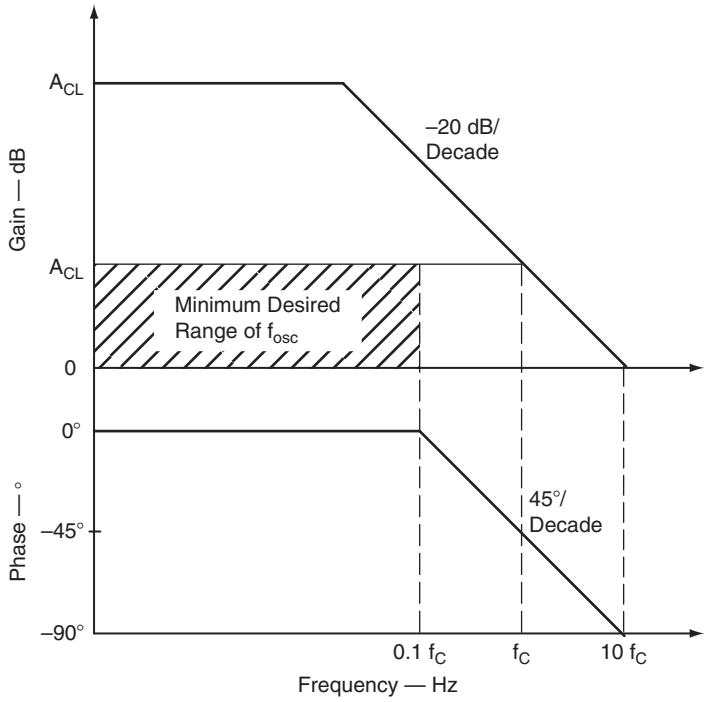


Figure 19.3: Op amp frequency response.

Most op amps are compensated and may have more than the 45° of phase shift at ω_{3dB}. The op amp should therefore be chosen with a gain bandwidth that is at least one decade above the oscillation frequency, as shown by the shaded area of Figure 19.3. The Wien bridge requires a gain bandwidth greater than $43\omega_{OSC}$ to maintain the gain and frequency within 10% of the ideal values [2]. Figure 19.4 compares the output distortion versus frequency of an LM328, a TLV247X, and a TLC071 op amp, which have bandwidths of 0.4 MHz, 2.8 MHz, and 10 MHz, respectively. In a Wien bridge oscillator with nonlinear feedback (see Section 19.7.1 for the circuit and transfer function), the oscillation frequency ranges from 16 Hz to 160 kHz. The graph illustrates the importance of choosing the correct op amp for the application. The LM328 achieves a maximum oscillation of 72 kHz and is attenuated more than 75%, while the TLV247X achieves 125 kHz with 18% attenuation. The wide bandwidth of the TLC071 provides a 138 kHz oscillation frequency with a mere 2% attenuation. The op amp must be chosen with the proper bandwidth or the output may oscillate at a frequency well below the design specification.

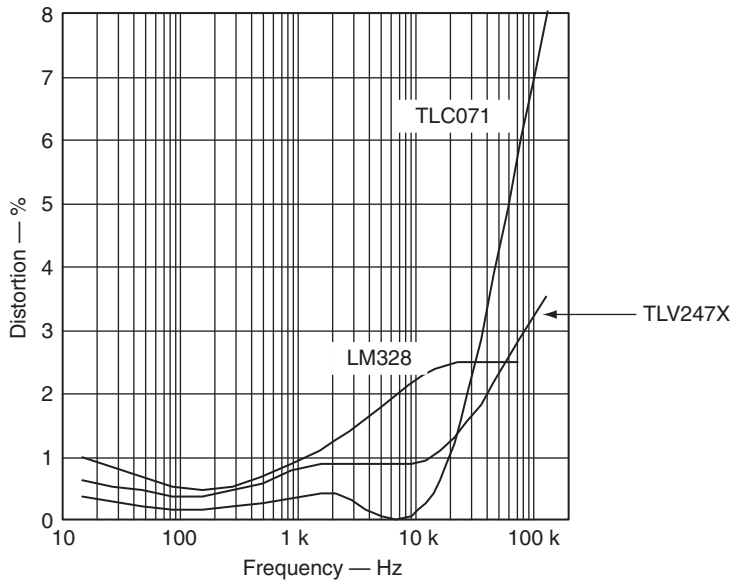


Figure 19.4: Op amp bandwidth and oscillator output.

Care must be taken when using large feedback resistors, since they interact with the input capacitance of the op amp to create poles with negative feedback and both poles and zeros with positive feedback. Large resistor values can move these poles and zeros into the proximity of the oscillation frequency and affect the phase shift [3].

A final consideration is given to the slew rate limitation of the op amp. The slew rate must be greater than $2\pi V_P f_0$, where V_P is the peak output voltage and f_0 is the oscillation frequency, or distortion of the output signal will result.

19.6 Analysis of the Oscillator Operation (Circuit)

Oscillators are created using various combinations of positive and negative feedback. Figure 19.5 shows the basic negative feedback amplifier block diagram with a positive feedback loop added. When positive and negative feedback are used, the gain of the negative feedback path is combined into one gain term (representing the closed loop gain) and Figure 19.5 reduces to Figure 19.1. The positive feedback network is then represented by $\beta = \beta_2$, and subsequent analysis is simplified. When negative feedback is used, the positive feedback loop can be ignored, since β_2 is 0. The case of positive and negative feedback combined is covered here, since the negative feedback case was reviewed in Chapters 6 and 7.

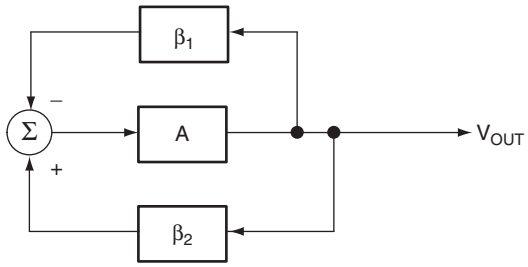
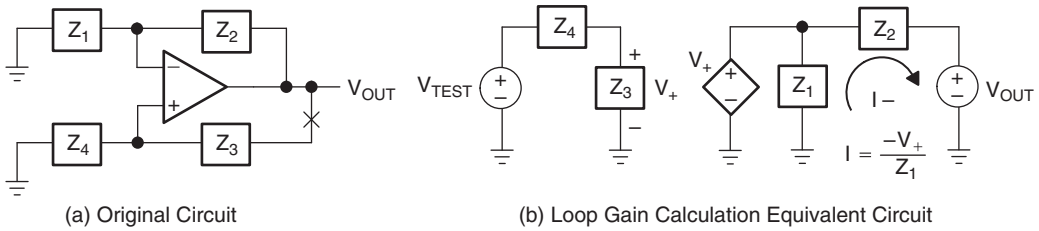


Figure 19.5: Block diagram of an oscillator.

A general form of an op amp with positive and negative feedback is shown in Figure 19.6(a). The first step is to break the loop at some point without altering the gain of the circuit. The positive feedback loop is broken at the point marked with an *X*. A test signal (V_{TEST}) is applied to the broken loop and the resulting output voltage (V_{OUT}) is measured with the equivalent circuit shown in Figure 19.6(b).



(a) Original Circuit

(b) Loop Gain Calculation Equivalent Circuit

Figure 19.6: Amplifier with positive and negative feedback.

V_+ is calculated first in Equation (19.3), then is treated as an input signal to a noninverting amplifier, resulting in Equation (19.4). Equation (19.3) is substituted for V_+ in Equation (19.4) to get the transfer function in Equation (19.5). The actual circuit elements are then substituted for each impedance and the equation is simplified. These equations are valid when the op amp open loop gain is large and the oscillation frequency is $<0.1\ \omega_{3dB}$.

$$V_+ = V_{TEST}\left(\frac{Z_4}{Z_3 + Z_4}\right) \tag{19.3}$$

$$V_{OUT} = V_+\left(\frac{Z_1 + Z_2}{Z_1}\right) \tag{19.4}$$

$$\frac{V_{OUT}}{V_{TEST}} = \left(\frac{Z_3}{Z_3 + Z_4}\right)\left(\frac{Z_1 + Z_2}{Z_1}\right) \tag{19.5}$$

Phase shift oscillators generally use negative feedback, so the positive feedback factor (β_2) becomes zero. Oscillator circuits such as the Wien bridge use both negative (β_1) and positive (β_2) feedback to achieve a constant state of oscillation. This circuit is analyzed in detail in Section 19.7.1 using Equation (19.5).

19.7 Sine Wave Oscillator Circuits

There are many types of sine wave oscillator circuits and variations of these circuits—the choice depends on the frequency and the desired purity of the output waveform. The focus of this section is on the more prominent oscillator circuits: Wien bridge, phase shift, and quadrature. The transfer function is derived for each case using the techniques described in Section 19.6 of this chapter and in Chapters 3, 6, and 7.

19.7.1 Wien Bridge Oscillator

The Wien bridge is one of the simplest and best known oscillators and is used extensively in circuits for audio applications. Figure 19.7 shows the basic Wien bridge circuit configuration. This circuit has only a few components and good frequency stability. The major drawback of the circuit is that the output amplitude is at the rails, saturating the op amp output transistors and causing high output distortion. Taming this distortion is more of a challenge than getting the circuit to oscillate. A couple of ways may be used to minimize this effect, which is covered later. It is now time to analyze this circuit and come up with the transfer function.

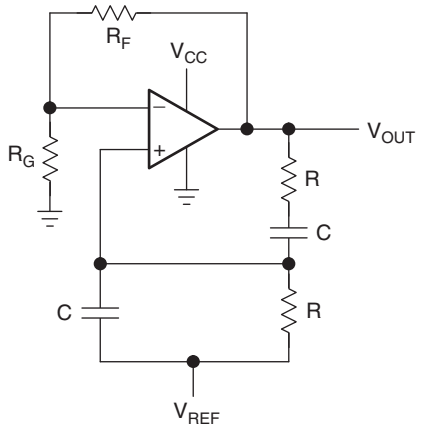


Figure 19.7: Wien bridge circuit schematic.

The Wien bridge circuit is of the form detailed in Section 19.6. The transfer function for the circuit is created using the technique described in that section. It is readily apparent that $Z_1 = R_G$, $Z_2 = R_F$, $Z_3 = (R_1 + 1/sC_1)$, and $Z_4 = (R_2 \| 1/sC_2)$. The loop is broken between the output and Z_1, V_{TEST} is applied to Z_1, and V_{OUT} is calculated. The positive feedback voltage, V_+, is calculated first in Equations (19.6) through (19.8). Equation (19.6) shows the simple voltage divider at the noninverting input. Each term is then multiplied by $(R_2C_2s + 1)$ and divided by R_2 to get Equation (19.7).

$$V_+ = V_{TEST}\left(\frac{Z_4}{Z_3 + Z_4}\right) = V_{TEST}\left[\frac{\left(\frac{R_2}{R_2C_2s + 1}\right)}{\left(\frac{R_2}{R_2C_2s + 1}\right) + \left(R_1 + \frac{1}{C_1s}\right)}\right] \tag{19.6}$$

$$\frac{V_+}{V_{\text{TEST}}} = \frac{1}{1 + R_1C_2s + \frac{R_1}{R_2} + \frac{1}{R_2C_1s} + \frac{C_2}{C_1}} \tag{19.7}$$

Substitute $s = j\omega_0$, where ω_0 is the oscillation frequency, $\omega_1 = 1/R_1C_2$, and $\omega_2 = 1/R_2C_1$ to get Equation (19.8):

$$\frac{V_+}{V_{\text{TEST}}} = \frac{1}{1 + \frac{R_1}{R_2} + \frac{C_2}{C_1} + j\left(\frac{\omega_0}{\omega_1} - \frac{\omega_2}{\omega_0}\right)} \tag{19.8}$$

Some interesting relationships now become apparent. The capacitor in the zero, represented by ω_1, and the capacitor in the pole, represented by ω_2, must each contribute 90° of phase shift toward the 180° required for oscillation at ω_0. This requires that $C_1 = C_2$ and $R_1 = R_2$. Setting ω_1 and ω_2 equal to ω_0 cancels the frequency terms, ideally removing any change in amplitude with frequency, since the pole and zero negate one another. An overall feedback factor of $\beta = 1/3$ is the result, Equation (19.9):

$$\frac{V_+}{V_{\text{TEST}}} = \frac{1}{1 + \frac{R}{R} + \frac{C}{C} + j\left(\frac{\omega_0}{\omega} - \frac{\omega}{\omega_0}\right)} = \frac{1}{3 + j\left(\frac{\omega_0}{\omega_0} - \frac{\omega_0}{\omega_0}\right)} = \frac{1}{3} \tag{19.9}$$

The gain of the negative feedback portion, A, of the circuit must then be set such that $|A\beta| = 1$, requiring $A = 3$. R_F must be set to twice the value of R_G to satisfy the condition. The op amp in Figure 19.7 is single supply, so a DC reference voltage, V_{REF}, must be applied to bias the output for full scale swing and minimal distortion. Applying V_{REF} to the positive input through R_2 restricts DC current flow to the negative feedback leg of the circuit. V_{REF} is set at 0.833V to bias the output at the midrail of the single supply, rail to rail input, and output amplifier, or 2.5 V. See Chapter 4 for details on DC biasing single supply op amps. V_{REF} is shorted to ground for split supply applications.

The final circuit is shown in Figure 19.8, with component values selected to provide an oscillation frequency of $\omega_0 = 2\pi f_0$, where $f_0 = 1/(2\pi RC) = 19.9$ kHz. The circuit oscillated at 1.57 kHz due to slightly varying component values with 2% distortion. This high value is due to the extensive clipping of the output signal at both supply rails, producing several large odd and even harmonics. The feedback resistor was then adjusted ±1%. Figure 19.9 shows the output voltage waveforms. The distortion grows as the saturation increases with increasing R_F, and oscillations cease when R_F is decreased by more than 0.8%.

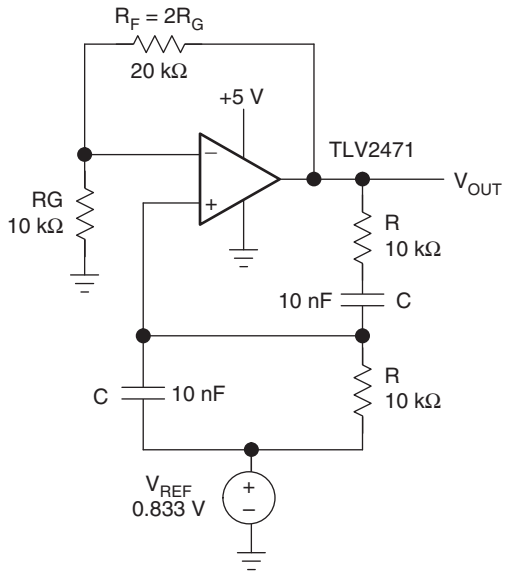


Figure 19.8: Final Wien bridge oscillator circuit.

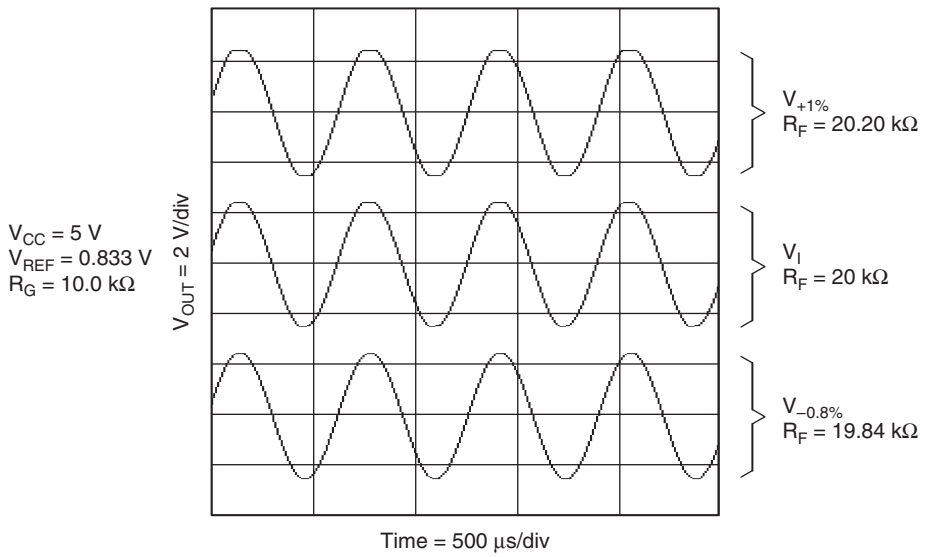


Figure 19.9: Wien bridge output waveforms.

Applying nonlinear feedback can minimize the distortion inherent in the basic Wien bridge circuit. A nonlinear component, such as an incandescent lamp, can be substituted into the circuit for R_G, as shown in Figure 19.10. The lamp resistance, R_{LAMP}, is nominally selected as half the feedback resistance, R_F, at the lamp current established by R_F and R_{LAMP}. When the power is first applied, the lamp is cool and its resistance is small, so the gain is large (>3). The current heats the filament and the resistance increases, lowering the gain. The nonlinear relationship between the lamp current and resistance keeps output voltage changes small. Figure 19.11 shows the output of this amplifier with a distortion of 1% for $f_{\text{OSC}} = 1.57$ kHz. The distortion for this variation is reduced over the basic circuit by avoiding hard saturation of the op amp transistors.

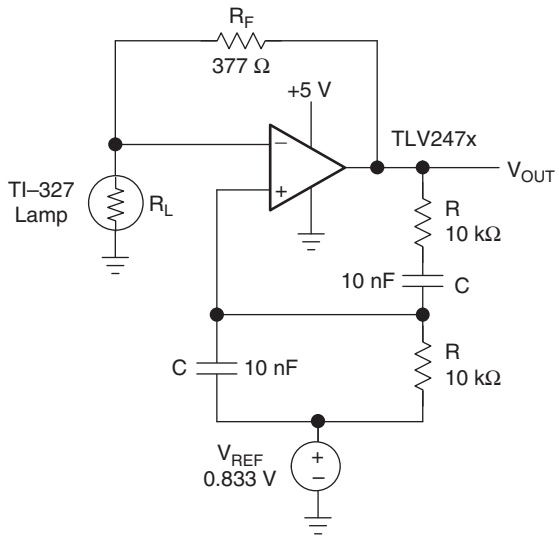


Figure 19.10: Wien bridge oscillator with nonlinear feedback.

The impedance of the lamp is due mostly to thermal effects. The output amplitude is then very temperature sensitive and tends to drift. The gain must be set higher than 3 to compensate for any temperature variations, which increases the distortion in the circuit [4]. This type of circuit is useful when the temperature does not fluctuate over a wide range or when used in conjunction with an amplitude limiting circuit.

The lamp has an effective low frequency thermal time constant, t_{thermal} [5]. As f_{OSC} approaches t_{thermal}, distortion is greatly increased. Several lamps can be placed in series

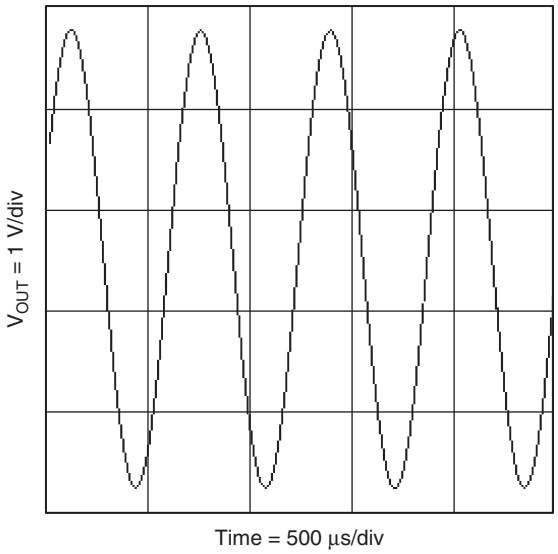


Figure 19.11: Output of the circuit in Figure 19.10.

to increase $t_{thermal}$ and reduce distortion. The drawbacks are that the time required for oscillations to stabilize is increased and the output amplitude is reduced.

An automatic gain control circuit must be used when neither of the two previous circuits yield low distortion. A typical Wien bridge oscillator with an AGC circuit is shown in Figure 19.12, with the output waveform of the circuit shown in Figure 19.13. The AGC is used to stabilize the magnitude of the sinusoidal output to an optimum gain level. The JFET serves as the AGC element, providing excellent control because of the wide range of the drain to source resistance (R_{DS}), which is controlled by the gate voltage. The JFET gate voltage is 0 V when the power is applied, and the JFET turns on with low R_{DS}. This places $R_{G2} + R_S + R_{DS}$ in parallel with R_{G1}, raising the gain to 3.05, and oscillations begin and gradually build up. As the output voltage gets large, the negative swing turns the diode on and the sample is stored on C_1, which provides a DC potential to the gate of Q_1. Resistor R_1 limits the current and establishes the time constant for charging C_1, which should be much greater than f_{OSC}. When the output voltage drifts high, R_{DS} increases, lowering the gain to a minimum of 2.87 $(1 + R_F/R_{G1})$. The output stabilizes when the gain reaches 3. The distortion of the AGC is 0.8%, which is due to slight clipping at the positive rail.

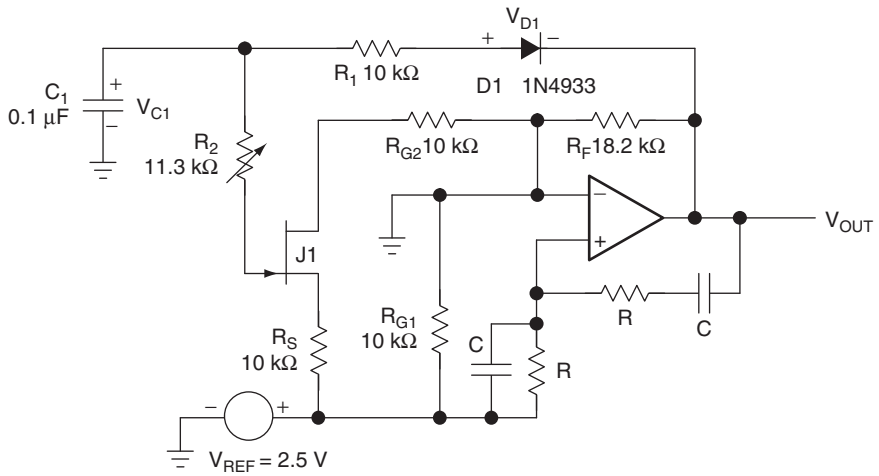


Figure 19.12: Wien bridge oscillator with AGC.

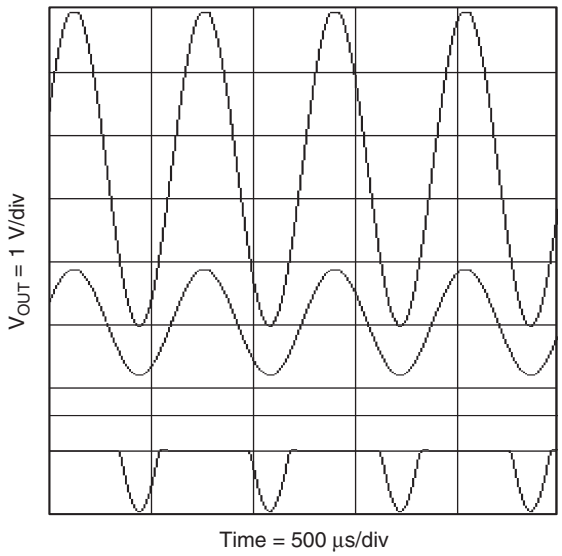


Figure 19.13: Output of the circuit in Figure 19.12.

The circuit of Figure 19.12 is biased with V_{REF} for a single supply amplifier. A zener diode can be placed in series with D_1 to limit the positive swing of the output and reduce distortion. A split supply can be easily implemented by grounding all points connected to V_{REF}. A wide variety of Wien bridge variations exist to more precisely control the amplitude and allow selectable or even variable oscillation frequencies. Some circuits use diode limiting in place of a nonlinear feedback component. The diodes reduce the distortion by providing a soft limit for the output voltage.

19.7.2 Phase Shift Oscillator, Single Amplifier

Phase shift oscillators have less distortion than the Wien bridge oscillator, coupled with good frequency stability. A phase shift oscillator can be built with one op amp as shown in Figure 19.14; the resulting output waveform is in Figure 19.15. Three RC sections are cascaded to get the steep $d\varphi/d\omega$ slope, as described in Section 19.3, to get a stable oscillation frequency. Any less and the oscillation frequency is high and interferes with the op amp BW limitations.

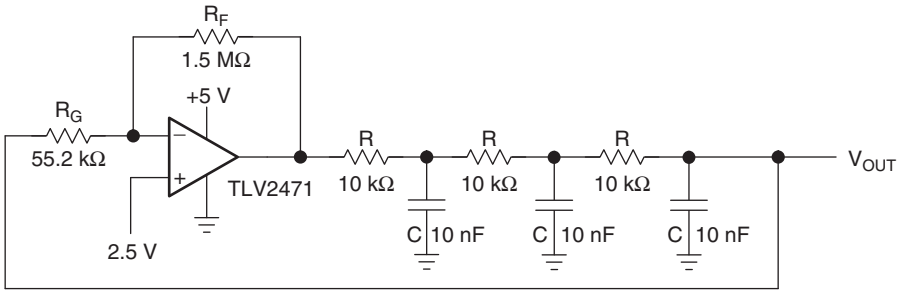


Figure 19.14: Phase shift oscillator (single op amp).

The normal assumption is that the phase shift sections are independent of each other. Then Equatiotn (19.10) is written:

$$A\beta = A\left(\frac{1}{RCs + 1}\right)^3 \tag{19.10}$$

The loop phase shift is –180° when the phase shift of each section is –60°, and this occurs when $\omega = 2\pi f = 1.732/RC$ because the tangent of 60° = 1.732. The magnitude

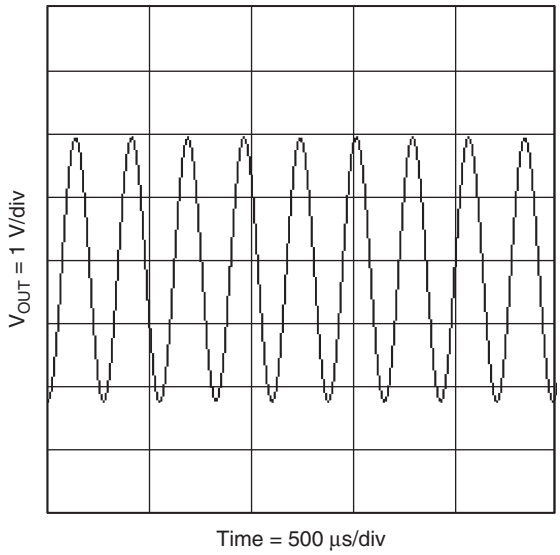


Figure 19.15: Output of the circuit in Figure 19.14.

of β at this point is $(1/2)^3$, so the gain, *A*, must be equal to 8 for the system gain to be equal to 1.

The oscillation frequency with the component values shown in Figure 19.14 is 3.76 kHz rather than the calculated oscillation frequency of 2.76 kHz. Also, the gain required to start oscillation is 27 rather than the calculated gain of 8. These discrepancies are partially due to component variations, but the biggest contributing factor is the incorrect assumption that the RC sections do not load each other. This circuit configuration was very popular when active components were large and expensive. But now op amps are inexpensive, small, and come four in a package, so the single op amp phase shift oscillator is losing popularity. The output distortion is a low 0.46%, considerably less than the Wein bridge circuit without amplitude stabilization.

19.7.3 Phase Shift Oscillator, Buffered

The buffered phase shift oscillator is much improved over the unbuffered version, the cost being a higher component count. The buffered phase shift oscillator is shown in Figure 19.16 and the resulting output waveform in Figure 19.17. The buffers prevent the RC sections from loading each other, hence the buffered phase shift oscillator

performs closer to the calculated frequency and gain. The gain setting resistor, R_G, loads the third RC section. If the fourth buffer in a quad op amp buffers this RC section, the performance becomes ideal. Low distortion sine waves can be obtained from either phase shift oscillator design, but the purest sine wave is taken from the output of the last RC section. This is a high impedance node, so a high impedance input is mandated to prevent loading and frequency shifting with load variations.

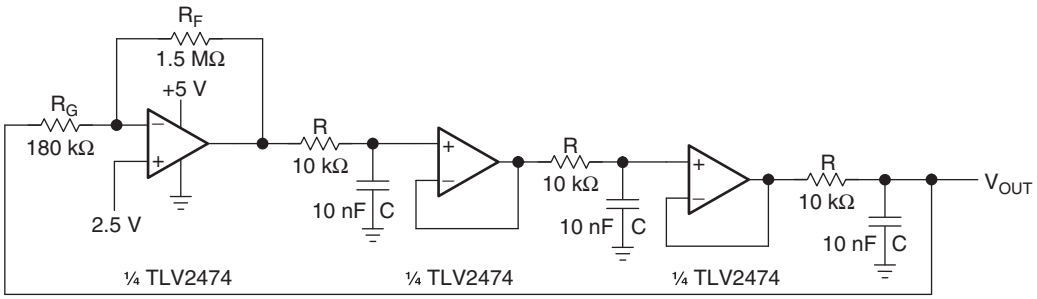


Figure 19.16: Phase shift oscillator, buffered.

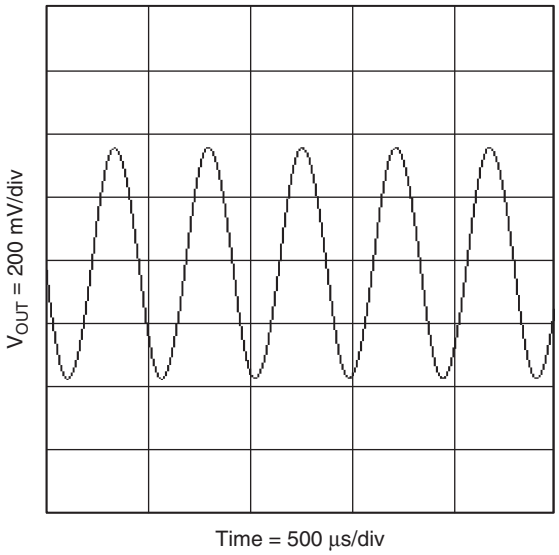


Figure 19.17: Output of the circuit in Figure 19.16.

19.7.4 Bubba Oscillator

The bubba oscillator in Figure 19.18 is another phase shift oscillator, but it takes advantage of the quad op amp package to yield some unique advantages. Four RC sections require 45° phase shift per section, so this oscillator has an excellent $d\varphi/dt$, resulting in minimized frequency drift. The RC sections each contribute 45° phase shift, so taking outputs from alternate sections yields low impedance quadrature outputs. When an output is taken from each op amp, the circuit delivers four 45° phase shifted sine waves. The loop equation is given in Equation (19.11). When $\omega = 1/RCs$, Equation (19.11) reduces to Equations (19.12) and (19.13):

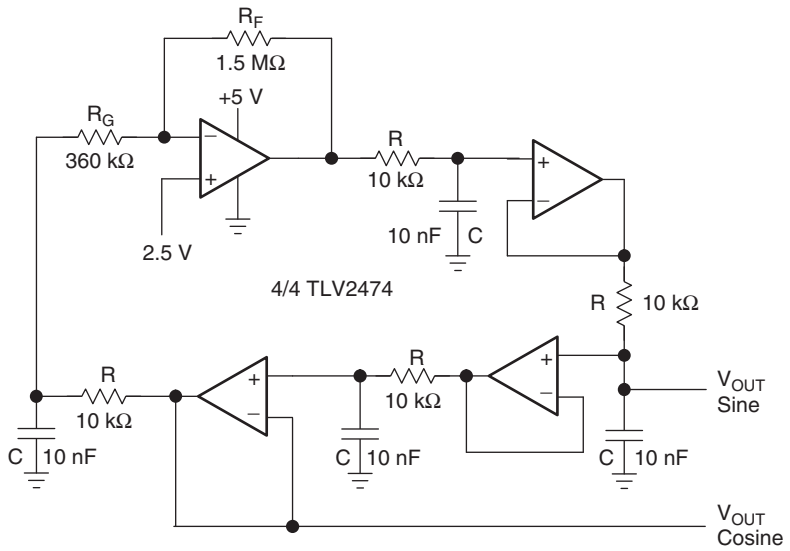


Figure 19.18: Bubba oscillator.

$$A\beta = A\left(\frac{1}{RCs + 1}\right)^4 \tag{19.11}$$

$$|\beta| = \left|\left(\frac{1}{j + 4}\right)^4 = \frac{1}{\sqrt{2}^4} = \frac{1}{4}\right| \tag{19.12}$$

$$\varphi = \tan^{-1}(1) = 45° \tag{19.13}$$

The gain, A, must equal 4 for oscillation to occur. The test circuit oscillated at 1.76 kHz rather than the ideal frequency of 1.72 kHz when the gain was 4.17 rather than the ideal gain 4. The output waveform is shown in Figure 19.19. Distortion is 1% for $V_{OUTSINE}$ and 0.1% for $V_{OUTCOSINE}$. With low gain A and low bias current op amps, the gain setting resistor, R_G, does not load the last RC section, thus ensuring oscillator frequency accuracy. Very low distortion sine waves can be obtained from the junction of R and R_G. When low distortion sine waves are required at all outputs, the gain should be distributed among all the op amps. The noninverting input of the gain op amp is biased at 0.5 V to set the quiescent output voltage at 2.5 V for single supply operation and should be ground for split supply op amps. Gain distribution requires biasing of the other op amps, but it has no effect on the oscillator frequency.

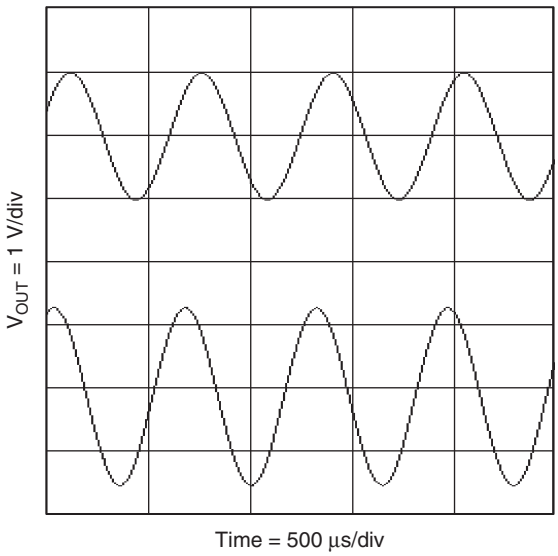


Figure 19.19: Output of the circuit in Figure 19.18.

19.7.5 Quadrature Oscillator

The quadrature oscillator shown in Figure 19.20 is another type of phase shift oscillator, but the three RC sections are configured so each section contributes 90° of phase shift. This provides both sine and cosine waveform outputs (the outputs are quadrature, or 90° apart), which is a distinct advantage over other phase shift

oscillators. The idea of the quadrature oscillator is to use the fact that the double integral of a sine wave is a negative sine wave of the same frequency and phase. The phase of the second integrator is then inverted and applied as positive feedback to induce oscillation [6].

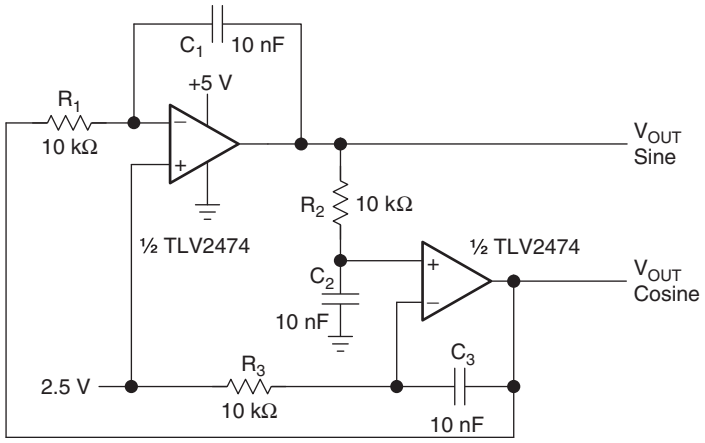


Figure 19.20: Quadrature oscillator.

The loop gain is calculated in Equation (19.14). When $R_1C_1 = R_2C_2 = R_3C_3$, Equation (19.14) reduces to Equation (19.15). When $\omega = 1/RC$, Equation (19.14) reduces to $1\angle -180$, so oscillation occurs at $\omega = 2\pi f = 1/RC$. The test circuit oscillated at 1.65 kHz rather than the calculated 1.59 kHz, as shown in Figure 19.21. This discrepancy is attributed to component variations. Both outputs have relatively high distortion that can be reduced with a gain stabilizing circuit. The sine output had 0.846% distortion and the cosine output had 0.46% distortion. Adjusting the gain can increase the amplitudes. The cost is bandwidth.

$$A\beta = A\left(\frac{1}{R_1C_1s}\right)\left(\frac{R_3C_3s + 1}{R_3C_3s(R_2C_2s + 1)}\right) \tag{19.14}$$

$$A\beta = A\left(\frac{1}{RCs}\right)^2 \tag{19.15}$$

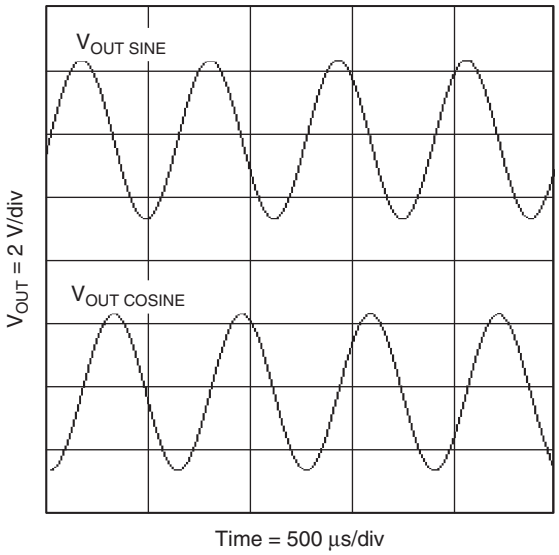


Figure 19.21: Output of the circuit in Figure 19.20.

19.8 Conclusion

Op amp oscillators are restricted to the lower end of the frequency spectrum because they do not have the required bandwidth to achieve low phase shift at high frequencies. The new current feedback op amps have a much greater bandwidth than the voltage feedback op amps but are very difficult to use in oscillator circuits because of their sensitivity to feedback capacitance. Voltage feedback op amps are limited to tens of hertz (at the most!) because of their low frequency roll-off. The bandwidth is reduced when op amps are cascaded due to the multiple contribution of phase shift.

The Wien bridge oscillator has few parts and good frequency stability, but the basic circuit has a high output distortion. AGC improves the distortion considerably, particularly at the lower frequency range. Nonlinear feedback offers the best performance over the middle and upper frequency ranges. The phase shift oscillator has lower output distortion and, without buffering, requires a high gain, which limits the use to very low frequencies. Decreasing cost of op amps and components has reduced the popularity of the phase shift oscillators. The quadrature oscillator requires only two op amps, has reasonable distortion, and offers both sine and cosine waveforms.

The drawback is the low amplitude, which may require a higher gain and a reduction in bandwidth, or an additional gain stage.

May your oscillators always oscillate, and your amplifiers always amplify.

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CHAPTER 20

Active Filter Design Techniques

Thomas Kugelstadt

20.1 Introduction

What is a filter?

A filter is a device that passes electric signals at certain frequencies or frequency ranges while preventing the passage of others.—Webster.

Filter circuits are used in a wide variety of applications. In the field of telecommunication, bandpass filters are used in the audio frequency range (0 kHz to 20 kHz) for modems and speech processing. High frequency bandpass filters (several hundred megahertz) are used for channel selection in telephone central offices. Data acquisition systems usually require antialiasing low pass filters as well as low pass noise filters in their preceding signal conditioning stages. System power supplies often use band rejection filters to suppress the 60 Hz line frequency and high frequency transients.

In addition, there are filters that do not filter frequencies of a complex input signal but just add a linear phase shift to each frequency component, thus contributing to a constant time delay. These are called *all pass filters*.

At high frequencies (>1 MHz), all these filters usually consist of passive components such as inductors (L), resistors (R), and capacitors (C). They are then called *LRC filters*.

In the lower frequency range (1 Hz to 1 MHz), however, the inductor value becomes very large and the inductor itself gets quite bulky, making economical production difficult.

In these cases, active filters become important. Active filters are circuits that use an operational amplifier (op amp) as the active device in combination with some resistors and capacitors to provide an LRC-like filter performance at low frequencies (Figure 20.1).

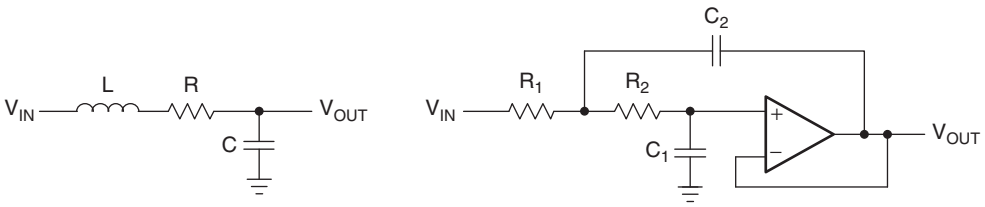

Figure 20.1: Second order passive low pass and second order active low pass filters.

This chapter covers active filters. It introduces the three main filter optimizations (Butterworth, Tschebyscheff, and Bessel), followed by five sections describing the most common active filter applications: low pass, high pass, bandpass, band rejection, and all pass filters. Rather than resembling just another filter book, the individual filter sections are written in a cookbook style, thus avoiding tedious mathematical derivations. Each section starts with the general transfer function of a filter, followed by the design equations to calculate the individual circuit components. The chapter closes with a section on practical design hints for single supply filter designs.

20.2 Fundamentals of Low Pass Filters

The most simple low pass filter is the passive RC low pass network shown in Figure 20.2.

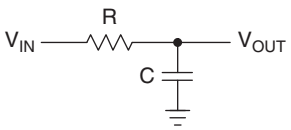

Figure 20.2: First order passive RC low pass filter.

Its transfer function is

$$A(S) = \frac{\frac{1}{RC}}{S + \frac{1}{RC}} = \frac{1}{1 + SRC}$$

where the complex frequency variable, $S = j\omega + \sigma$, allows for any time variable signals. For pure sine waves, the damping constant, σ, becomes zero and $S = j\omega$.

For a normalized presentation of the transfer function, S is referred to the *filter's corner frequency* or *–3 dB frequency*, ω_C, and has these relationships:

$$S = \frac{S}{\omega_C} = \frac{j\omega}{\omega_C} = j\frac{f}{f_C} = j\Omega$$

With the corner frequency of the low pass in Figure 20.2 being $f_C = 1/2\pi RC$, S becomes $S = sRC$ and the transfer function $A(s)$ results in

$$A(S) = \frac{1}{1 + S}$$

The magnitude of the gain response is

$$|A| = \frac{1}{\sqrt{1 + \Omega^2}}$$

For frequencies $\Omega \gg 1$, the roll-off is 20 dB/decade. For a steeper roll-off, n filter stages can be connected in series, as shown in Figure 20.3. To avoid loading effects, op amps, operating as impedance converters, separate the individual filter stages.

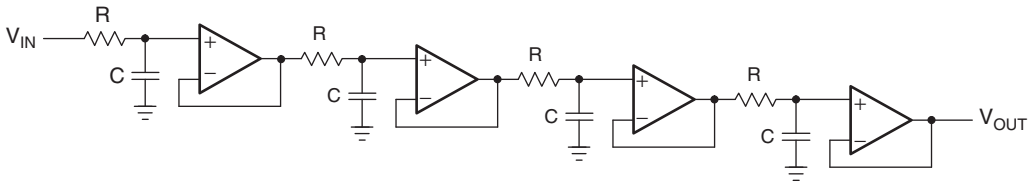

Figure 20.3: Fourth order passive RC low pass filter with decoupling amplifiers.

The resulting transfer function is

$$A(S) = \frac{1}{(1 + \alpha_1 S)(1 + \alpha_2 S) \ldots (1 + \alpha_N S)}$$

In the case that all filters have the same cutoff frequency, f_C, the coefficients become $\alpha_1 = \alpha_2 = \ldots = \alpha_n = \alpha\sqrt{\sqrt[n]{2} - 1}$, and f_C of each partial filter is $1/\alpha$ times higher than f_C of the overall filter.

Figure 20.4 shows the results of a fourth order RC low pass filter. The roll-off of each partial filter (Curve 1) is –20 dB/decade, increasing the roll-off of the overall filter (Curve 2) to 80 dB/decade.

Note: Filter response graphs plot gain versus the normalized frequency axis $\Omega(\Omega = f/f_C)$.

The corner frequency of the overall filter is reduced by a factor of $\alpha \approx 2.3$ times versus the –3 dB frequency of partial filter stages.

In addition, Figure 20.4 shows the transfer function of an ideal fourth order low pass function (Curve 3).

In comparison to the ideal low pass filter, the RC low pass filter lacks the following characteristics:

- The passband gain varies long before the corner frequency, f_C, thus amplifying the upper passband frequencies less than the lower passband.
- The transition from the passband into the stop band is not sharp but happens gradually, moving the actual 80 dB roll-off by 1.5 octaves above f_C.
- The phase response is not linear, thus increasing the amount of signal distortion significantly.

The gain and phase response of a low pass filter can be optimized to satisfy *one* of the following three criteria:

1. A maximum passband flatness.
2. An immediate passband to stop band transition.
3. A linear phase response.

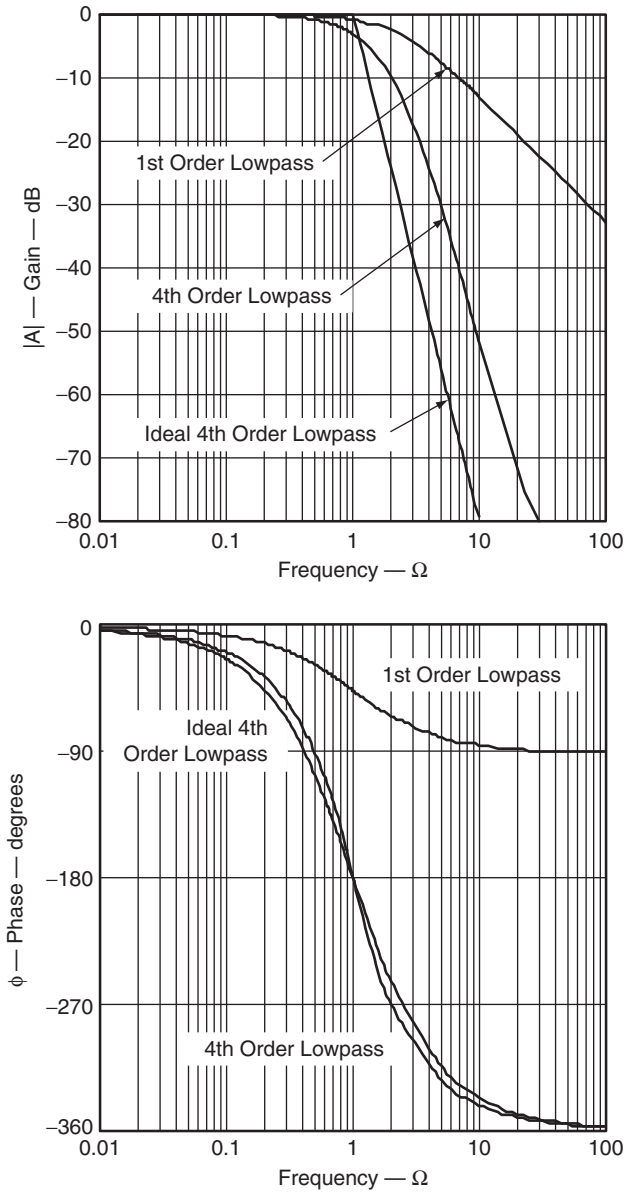

Figure 20.4: Frequency and phase responses of a fourth order passive RC low pass filter. Curve 1, first order partial low pass filter; Curve 2, fourth order overall low pass filter; Curve 3, ideal fourth order low pass filter.

For that purpose, the transfer function must allow for complex poles and needs to be of the following type:

$$A(S) = \frac{A_0}{(1 + a_1S + b_1S^2)(1 + a_2S + b_2S^2)\ldots(1 + a_nS + b_nS^2)} = \frac{A_0}{\prod_i (1 + a_iS + b_iS^2)}$$

where A_0 is the passband gain at DC and a_i and b_i are the filter coefficients.

Since the denominator is a product of quadratic terms, the transfer function represents a series of cascaded second order low pass stages, with a_i and b_i being positive real coefficients. These coefficients define the complex pole locations for each second order filter stage, thus determining the behavior of its transfer function.

The following three types of predetermined filter coefficients are available listed in table format in Section 20.9:

- The Butterworth coefficients, optimizing the passband for maximum flatness.
- The Tschebyscheff coefficients, sharpening the transition from passband into the stop band.
- The Bessel coefficients, linearizing the phase response up to f_C.

The transfer function of a passive RC filter does not allow further optimization, due to the lack of complex poles. The only possibility to produce conjugate complex poles using passive components is the application of LRC filters. However, these filters are mainly used at high frequencies. In the lower frequency range (<10 MHz), the inductor values become very large and the filter becomes uneconomical to manufacture. In these cases, active filters are used. Active filters are RC networks that include an active device, such as an operational amplifier (op amp).

Section 20.3 shows that the products of the *RC* values and the corner frequency must yield the predetermined filter coefficients a_i and b_i to generate the desired transfer function.

The following subsections introduce the most commonly used filter optimizations.

20.2.1 Butterworth Low Pass Filters

The Butterworth low pass filter provides maximum passband flatness. Therefore, a Butterworth low pass is often used as antialiasing filter in data converter applications where precise signal levels are required across the entire passband.

Figure 20.5 plots the gain response of different orders of Butterworth low pass filters versus the normalized frequency axis, $\Omega(\Omega = f/f_C)$; the higher the filter order, the longer the passband flatness.

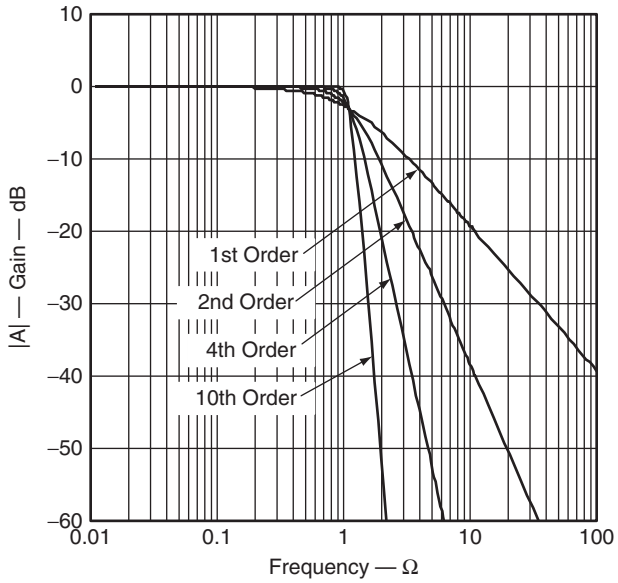

Figure 20.5: Amplitude responses of Butterworth low pass filters.

20.2.2 Tschebyscheff Low Pass Filters

The Tschebyscheff low pass filters provide an even higher gain roll-off above f_C. However, as Figure 20.6 shows, the passband gain is not monotone but contains ripples of constant magnitude instead. For a given filter order, the higher the passband ripples, the higher the filter's roll-off.

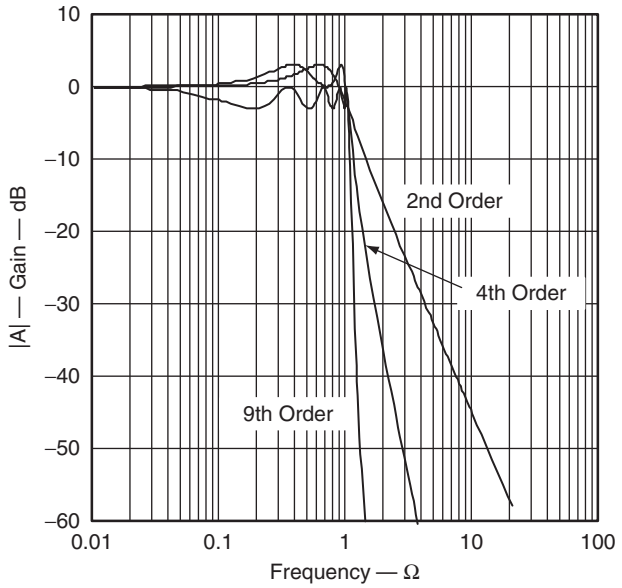

Figure 20.6: Gain responses of Tschebyscheff low pass filters.

With increasing filter order, the influence of the ripple magnitude on the filter roll-off diminishes.

Each ripple accounts for one second order filter stage. Filters with even order numbers generate ripples above the 0 dB line, while filters with odd order numbers create ripples below 0 dB.

Tschebyscheff filters are often used in filter banks, where the frequency content of a signal is of more importance than a constant amplification.

20.2.3 Bessel Low Pass Filters

The Bessel low pass filters have a linear phase response (Figure 20.7) over a wide frequency range, which results in a constant group delay (Figure 20.8) in that frequency range. Bessel low pass filters, therefore, provide an optimum square wave transmission behavior. However, the passband gain of a Bessel low pass filter is not as flat as that of the Butterworth low pass, and the transition from passband to stop band is by far not as sharp as that of a Tschebyscheff low pass filter (Figure 20.9).

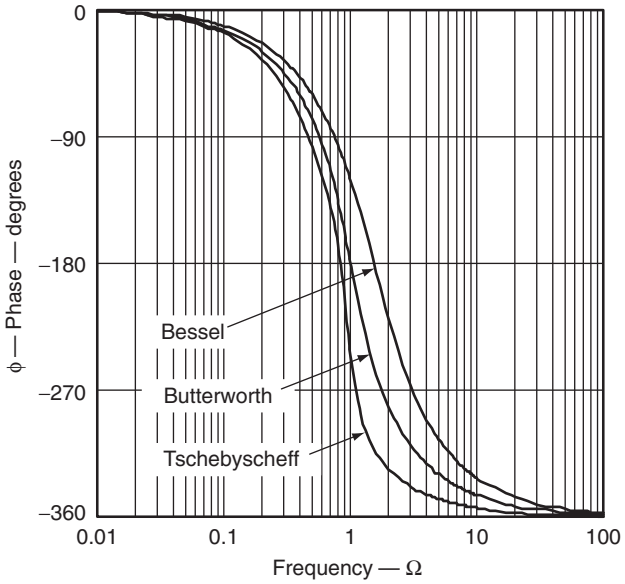

Figure 20.7: Comparison of phase responses of fourth order low pass filters.

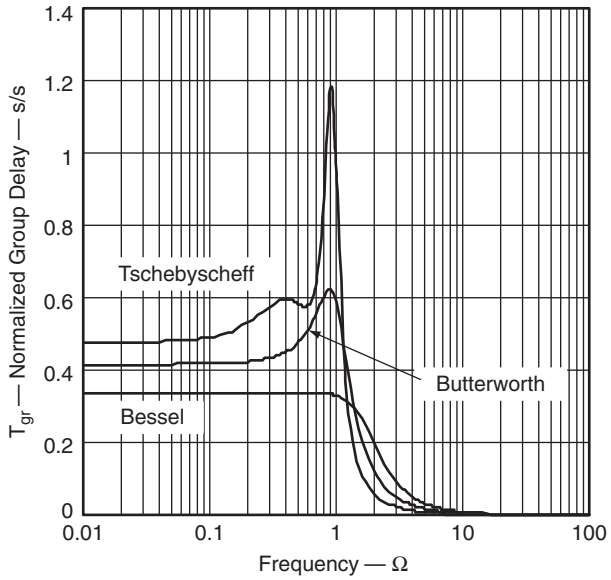

Figure 20.8: Comparison of normalized group delay (T_{gr}) of fourth order low pass filters.

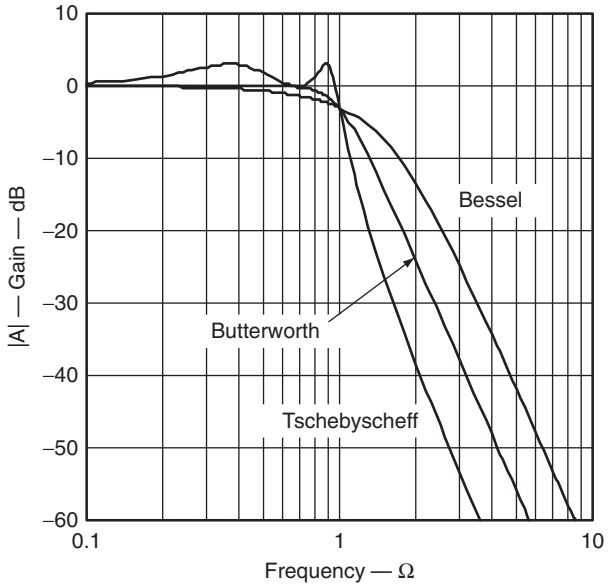

Figure 20.9: Comparison of gain responses of fourth order low pass filters.

20.2.4 Quality Factor Q

The quality factor Q is an equivalent design parameter to the filter order n. Instead of designing an nth order Tschebyscheff low pass filter, the problem can be expressed as designing a Tschebyscheff low pass filter with a certain Q.

For bandpass filters, Q is defined as the ratio of the mid frequency, f_m, to the bandwidth at the two –3 dB points:

$$Q = \frac{f_m}{(f_2 - f_1)}$$

For low pass and high pass filters, Q represents the pole quality and is defined as

$$Q = \frac{\sqrt{b_i}}{a_i}$$

High values of Q can be graphically presented as the distance between the 0 dB line and the peak point of the filter's gain response. An example is given in Figure 20.10, which shows a 10th order Tschebyscheff low pass filter and its five partial filters with their individual Q values.

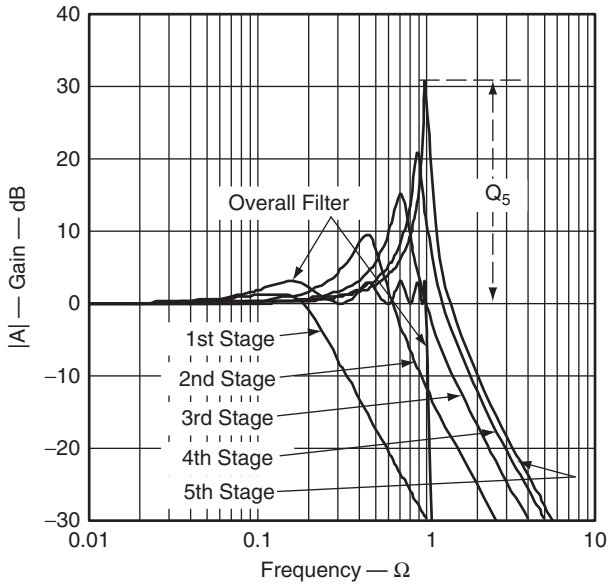

Figure 20.10: Quality factor Q on a 10th order Tschebyscheff low pass filter.

The gain response of the fifth filter stage peaks at 31 dB, which is the logarithmic value of Q_5:

$$Q_5(\text{dB}) = 20 \log Q_5$$

Solving for the numerical value of Q_5 yields

$$Q_5 = 10\frac{31}{20} = 35.48$$

which is within 1% of the theoretical value of $Q = 35.85$ given in Section 20.9, Table 20.12, last row.

The graphical approximation is good for $Q > 3$. For lower Q values, the graphical values differ from the theoretical value significantly. However, only higher Q values are of concern, since the higher the Q is, the more a filter inclines to instability.

20.2.5 Summary

The general transfer function of a low pass filter is

$$A(S) = \frac{A_0}{\prod_i (1 + a_i S + b_i S)} \tag{20.1}$$

The filter coefficients a_i and b_i distinguish between Butterworth, Tschebyscheff, and Bessel filters. The coefficients for all three types of filters are tabulated down to the 10th order in Section 20.9, Tables 20.7 through 20.13.

The multiplication of the denominator terms with each other yields an nth order polynomial of S, with n being the filter order.

While n determines the gain roll-off above f_C with $-n \times 20$ dB/decade, a_i and b_i determine the gain behavior in the passband.

In addition, the ratio $\sqrt{b_i}/a_i = Q$ is defined as the pole quality. The higher the Q value, the more a filter inclines to instability.

20.3 Low Pass Filter Design

Equation (20.1) represents a cascade of second order low pass filters. The transfer function of a single stage is

$$A_i(S) = \frac{A_0}{(1 + a_i S + b_i S^2)} \tag{20.2}$$

For a first order filter, the coefficient b is always zero ($b_1 = 0$), yielding

$$A(S) = \frac{A_0}{1 + a_1 S} \tag{20.3}$$

The first order and second order filter stages are the building blocks for higher order filters.

Often, the filters operate at unity gain ($A_0 = 1$) to lessen the stringent demands on the op amp's open loop gain.

Figure 20.11 shows the cascading of filter stages up to the sixth order. A filter with an even order number consists of second order stages only, while filters with an odd order number include an additional first order stage at the beginning.

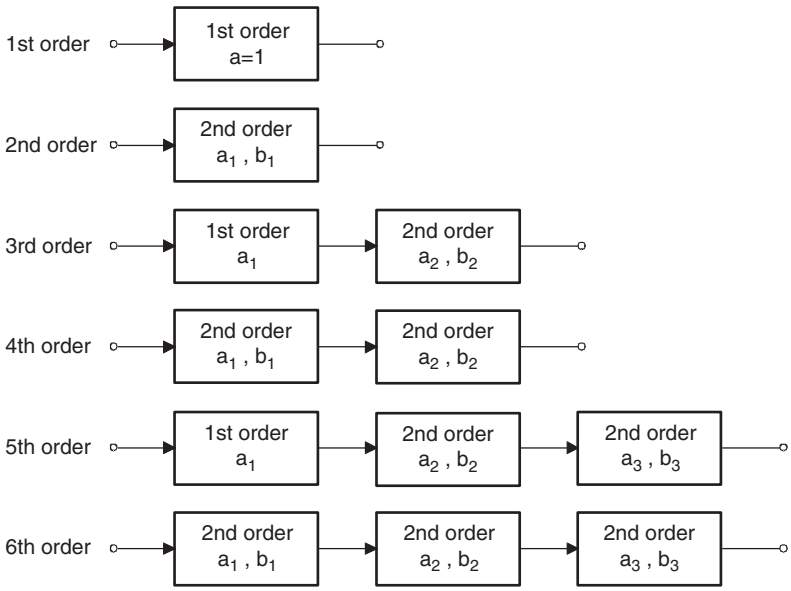

Figure 20.11: Cascading filter stages for higher order filters.

Figure 20.10 demonstrates that the higher the corner frequency of a partial filter, the higher is its Q. Therefore, to avoid the saturation of the individual stages, the filters need to be placed in the order of rising Q values. The Q values for each filter order are listed (in rising order) in Section 20.9, Tables 20.7 through 20.13.

20.3.1 First Order Low Pass Filter

Figures 20.12 and 20.13 show a first order low pass filter in the inverting and noninverting configurations.

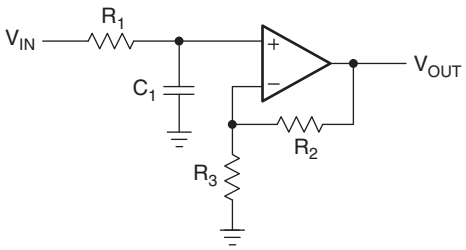

Figure 20.12: First order noninverting low pass filter.

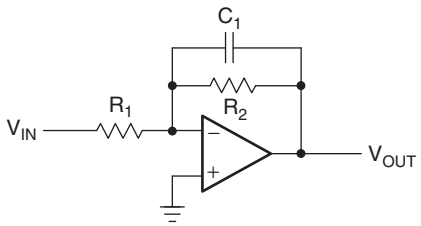

Figure 20.13: First order inverting low pass filter.

The transfer functions of the circuits are

$$A(S) = \frac{1 + \dfrac{R_2}{R_3}}{1 + \omega_c R_1 C_1 S}$$

and

$$A(S) = \frac{-\dfrac{R_2}{R_1}}{1 + \omega_c R_2 C_1 S}$$

The negative sign indicates that the inverting amplifier generates a 180° phase shift from the filter input to the output.

The coefficient comparison between the two transfer functions and Equation (20.3) yields

$$A_0 = 1 + \frac{R_2}{R_3} \text{ and } A_0 = -\frac{R_2}{R_1}$$

$$a_1 = \omega_c R_1 C_1 \text{ and } a_1 = \omega_c R_2 C_1$$

To dimension the circuit, specify the corner frequency (f_C), the DC gain (A_0), and capacitor C_1, then solve for resistors R_1 and R_2:

$$R_1 = \frac{a_1}{2\pi f_c C_1} \text{ and } R_2 = \frac{a_1}{2\pi f_c C_1}$$

$$R_2 = R_3(A_0 - 1) \text{ and } R_1 = -\frac{R_2}{A_0}$$

The coefficient a_1 is taken from one of the coefficient tables (Tables 20.7 through 20.13 in Section 20.9).

Note that all filter types are identical in their first order and $a_1 = 1$. For higher filter orders, however, $a_1 \neq 1$, because the corner frequency of the first order stage is different from the corner frequency of the overall filter.

Example 20.1. First Order Unity Gain Low Pass Filter For a first order unity gain low pass filter with $f_C = 1$ kHz and $C_1 = 47$ nF, R_1 calculates to

$$R_1 = \frac{a_1}{2\pi f_c C_1} = \frac{1}{2\pi \times 10^3\,\text{Hz} \times 47 \times 10^{-9}\text{F}} = 3.38\ \text{k}\Omega$$

However, to design the first stage of a third order unity gain Bessel low pass filter, assuming the same values for f_C and C_1, requires a different value for R_1. In this case, obtain a_1 for a third order Bessel filter from Table 20.7 in Section 20.9 (Bessel coefficients) to calculate R_1:

$$R_1 = \frac{a_1}{2\pi f_c C_1} = \frac{0.756}{2\pi \times 10^3\,\text{Hz} \times 47 \times 10^{-9}\text{F}} = 2.56\ \text{k}\Omega$$

When operating at unity gain, the noninverting amplifier reduces to a voltage follower (Figure 20.14), thus inherently providing a superior gain accuracy. In the case of the inverting amplifier, the accuracy of the unity gain depends on the tolerance of the two resistors, R_1 and R_2.

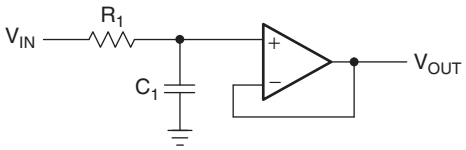

Figure 20.14: First order noninverting low pass filter with unity gain.

20.3.2 Second Order Low Pass Filter

There are two topologies for a second order low pass filter: the Sallen-Key and the multiple feedback (MFB).

Sallen-Key Topology

The general Sallen-Key topology in Figure 20.15 allows for separate gain setting via $A_0 = 1 + R_4/R_3$. However, the unity gain topology in Figure 20.16 is usually applied in filter designs with high gain accuracy, unity gain, and low Q values ($Q < 3$).

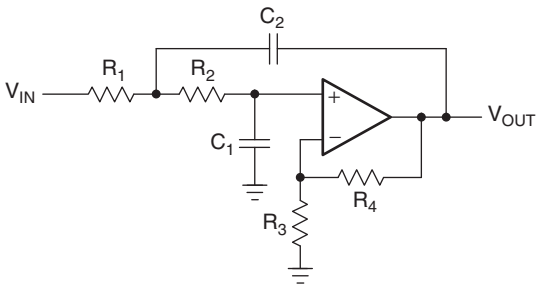

Figure 20.15: General Sallen-Key low pass filter.

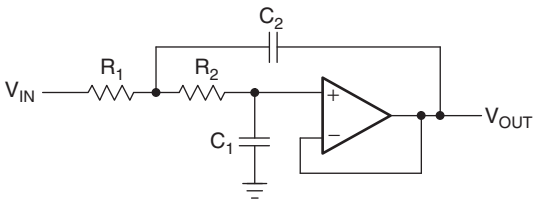

Figure 20.16: Unity gain Sallen-Key low pass filter.

The transfer function of the circuit in Figure 20.15 is

$$A(S) = \frac{A_0}{1 + \omega_c[C_1(R_1 + R_2) + (1 - A_0)R_1C_2]S + \omega_c^2 R_1R_2C_1C_2S^2}$$

For the unity gain circuit in Figure 20.16 ($A_0 = 1$), the transfer function simplifies to

$$A(S) = \frac{1}{1 + \omega_c C_1(R_1 + R_2)S + \omega_c^2 R_1R_2C_1C_2S^2}$$

The coefficient comparison between this transfer function and Equation (20.2) yields

$$A_0 = 1$$

$$a_1 = \omega_c C_1(R_1 + R_2)$$

$$b_1 = \omega_c^2 R_1R_2C_1C_2$$

Given C_1 and C_2, the resistor values for R_1 and R_2 are calculated through

$$R_{1,2} = \frac{a_1C_2 \pm \sqrt{a_1^3C_2^2 - 4b_1C_1C_2}}{4\pi f_c C_1C_2}$$

To obtain real values under the square root, C_2 must satisfy the following condition:

$$C_2 \geq C_1\frac{4b_1}{a_1^2}$$

Example 20.2. Second Order Unity Gain Tschebyscheff Low Pass Filter The task is to design a second order unity gain Tschebyscheff low pass filter with a corner frequency of $f_C = 3$ kHz and a 3 dB passband ripple.

From Table 20.12 (the Tschebyscheff coefficients for 3 dB ripple), obtain the coefficients a_1 and b_1 for a second order filter with $a_1 = 1.0650$ and $b_1 = 1.9305$.

Specifying C_1 as 22 nF yields a C_2 value of

$$C_2 \geq C_1 \frac{4b_1}{a_1^2} = 22.10^{-9}\,\text{nF} \times \frac{4 \times 1.9305}{1.065^2} \cong 150\,\text{nF}$$

Inserting a_1 and b_1 into the resistor equation for $R_{1,2}$ results in

$$R_1 = \frac{1.065 \times 150 \times 10^{-9} - \sqrt{(1.065 \times 150 \times 10^{-9})^2 - 4 \times 1.9305 \times 22 \times 10^{-9} \times 150 \times 10^{-9}}}{4\pi \times 3 \times 10^3 \times 22 \times 10^{-9} \times 150 \times 10^{-9}} = 1.26\,\text{k}\Omega$$

and

$$R_2 = \frac{1.065 \times 150 \times 10^{-9} - \sqrt{(1.065 \times 150 \times 10^{-9})^2 - 4 \times 1.9305 \times 22 \times 10^{-9} \times 150 \times 10^{-9}}}{4\pi \times 3 \times 10^3 \times 22 \times 10^{-9} \times 150 \times 10^{-9}} = 1.30\,\text{k}\Omega$$

with the final circuit shown in Figure 20.17.

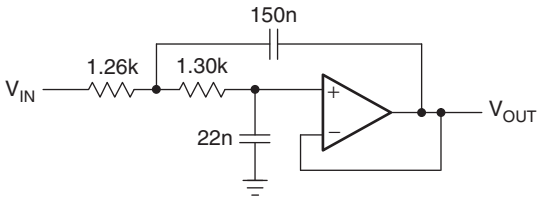

Figure 20.17: Second order unity gain Tschebyscheff low pass with 3 dB ripple.

A special case of the general Sallen-Key topology is the application of equal resistor values and equal capacitor values: $R_1 = R_2 = R$ and $C_1 = C_2 = C$.

The general transfer function changes to

$$A(S) = \frac{A_0}{1 + \omega_c RC(3 - A_0)S + (\omega_c RC)^2 S^2} \text{ with } A_0 = 1 + \frac{R_4}{R_3}$$

The coefficient comparison with Equation (20.2) yields

$$a_1 = \omega RC(3 - A_0)$$

$$b_1 = (\omega RC)^2$$

Given C and solving for R and A_0 results in

$$R = \frac{\sqrt{b_1}}{2\pi f_c C}$$

and

$$A_0 = 3 - \frac{a_1}{\sqrt{b_1}} = 3 - \frac{1}{Q}$$

Therefore, A_0 depends solely on the pole quality Q and vice versa; Q, and with it the filter type, is determined by the gain setting of A_0:

$$Q = \frac{1}{3 - A_0}$$

The circuit in Figure 20.18 allows the filter type to be changed through the various resistor ratios R_4/R_3.

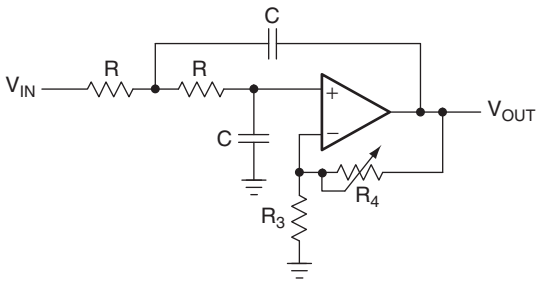

Figure 20.18: Adjustable second order low pass filter.

Table 20.1 lists the coefficients of a second order filter for each filter type and gives the resistor ratios that adjust the Q value.

Table 20.1: Second Order Filter Coefficients

Second order	Bessel	Butterworth	3 dB Tschebyscheff
a_1	1.3617	1.4142	1.065
b_1	0.618	1	1.9305
Q	0.58	0.71	1.3
R_4/R_3	0.268	0.568	0.234

Multiple Feedback Topology

The MFB topology is commonly used in filters that have high Q values and require a high gain. The transfer function of the circuit in Figure 20.19 is

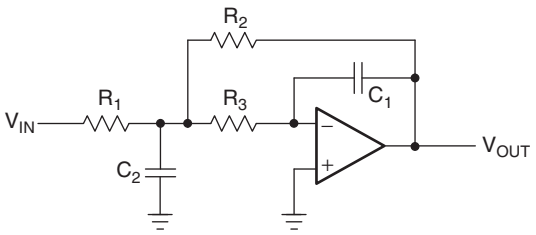

Figure 20.19: Second order MFB low pass filter.

$$A(S) = -\frac{\frac{R_2}{R_1}}{1 + \omega_c C_1\left(R_2 + R_3 + \frac{R_2R_3}{R_1}\right)S + \omega_c^2 C_1C_2R_2R_3S^2}$$

Through coefficient comparison with Equation (20.2), one obtains the relations

$$A_0 = -\frac{R_2}{R_1}$$

$$a_1 = \omega_c C_1 \left(R_2 + R_3 + \frac{R_2 R_3}{R_1} \right)$$

$$b_1 = \omega_c^2 C_1 C_2 R_2 R_3$$

Given C_1 and C_2 and solving for the resistors $R_1 - R_3$,

$$R_2 = \frac{a_1 C_2 - \sqrt{a_1^2 C_2^2 - 4 b_1 C_1 C_2 (1 - A_0)}}{4\pi f_c C_1 C_2}$$

$$R_1 = \frac{R_2}{-A_0}$$

$$R_3 = \frac{b_1}{4\pi^2 f_c C_1 C_2 R_2}$$

To obtain real values for R_2, C_2 must satisfy the following condition:

$$C_2 \geq C_1 \frac{4 b_1 (1 - A_0)}{a_1^2}$$

20.3.3 Higher Order Low Pass Filter

Higher order low pass filters are required to sharpen a desired filter characteristic. For that purpose, first order and second order filter stages are connected in series, so that the product of the individual frequency responses results in the optimized frequency response of the overall filter.

To simplify the design of the partial filters, the coefficients a_i and b_i for each filter type are listed in the coefficient tables (Tables 20.7 through 20.13 in Section 20.9), with each table providing sets of coefficients for the first 10 filter orders.

Example 20.3. Fifth Order Filter The task is to design a fifth order unity gain Butterworth low pass filter with the corner frequency $f_C = 50$ kHz.

First the coefficients for a fifth order Butterworth filter are obtained from Table 20.8, Section 20.9, and shown here in Table 20.2.

Table 20.2: Example 20.3 Filters

	a_i	b_i
Filter 1	$a_1 = 1$	$b_1 = 0$
Filter 2	$a_2 = 1.6180$	$b_2 = 1$
Filter 3	$a_3 = 0.6180$	$b_3 = 1$

Then, dimension each partial filter by specifying the capacitor values and calculating the required resistor values. The first filter is shown in Figure 20.20.

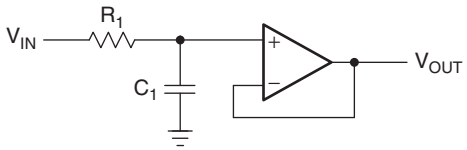

Figure 20.20: First order unity gain low pass filter.

With $C_1 = 1$ nF,

$$R_1 = \frac{a_1}{2\pi f_c C_1} = \frac{1}{2\pi \times 50 \times 10^3 \text{ Hz} \times 1 \times 10^{-9} \text{ F}} = 3.18 \text{ k}\Omega$$

The closest 1% value is 3.16 kΩ.

The second filter is shown in Figure 20.21.

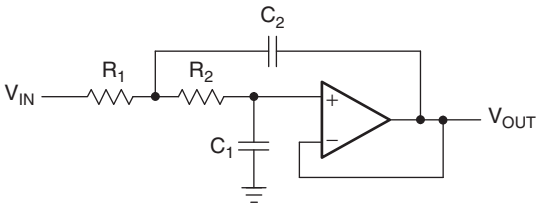

Figure 20.21: Second order unity gain Sallen-Key low pass filter.

With $C_1 = 820$ pF,

$$C_2 \geq C_1 \frac{4b_2}{a_2^2} = 820 \times 10^{-12} \text{ F} \times \frac{4 \times 1}{1.618^2} = 1.26 \text{ nF}$$

The closest 5% value is 1.5 nF.

With $C_1 = 820$ pF and $C_2 = 1.5$ nF, calculate the values for R_1 and R_2 through

$$R_1 = \frac{a_2 C_2 - \sqrt{a_2^2 C_2^2 - 4b_2 C_1 C_2}}{4\pi f_c C_1 C_2}$$

and

$$R_2 = \frac{a_2 C_2 + \sqrt{a_2^2 C_2^2 - 4b_2 C_1 C_2}}{4\pi f_c C_1 C_2}$$

and obtain

$$R_1 = \frac{1.618 \times 1.5 \times 10^{-9} - \sqrt{\left(1.618 \times 1.5 \times 10^{-9}\right)^2 - 4 \times 1 \times 820 \times 10^{-12} \times 1.5 \times 10^{-9}}}{4\pi \times 50 \times 10^3 \times 820 \times 10^{-12} \times 1.5 \times 10^{-9}} = 1.87 \text{ k}\Omega$$

$$R_2 = \frac{1.618 \times 1.5 \times 10^{-9} - \sqrt{\left(1.618 \times 1.5 \times 10^{-9}\right)^2 - 4 \times 1 \times 820 \times 10^{-12} \times 1.5 \times 10^{-9}}}{4\pi \times 50 \times 10^3 \times 820 \times 10^{-12} \times 1.5 \times 10^{-9}} = 4.42 \text{ k}\Omega$$

R_1 and R_2 are available 1% resistors.

The calculation of the third filter is identical to the calculation of the second filter, except that a_2 and b_2 are replaced by a_3 and b_3, thus resulting in different capacitor and resistor values.

Specify C_1 as 330 pF, and obtain C_2 with

$$C_2 \geq C_1 \frac{4b_3}{a_3^2} = 330 \times 10^{-12} \text{ F} \times \frac{4.1}{0.618^2} = 3.46 \text{ nF}$$

The closest 10% value is 4.7 nF.

With $C_1 = 330$ pF and $C_2 = 4.7$ nF, the values for R_1 and R_2 are

- $R_1 = 1.45$ kΩ, with the closest 1% value being 1.47 kΩ.
- $R_2 = 4.51$ kΩ, with the closest 1% value being 4.53 kΩ.

Figure 20.22 shows the final filter circuit with its partial filter stages.

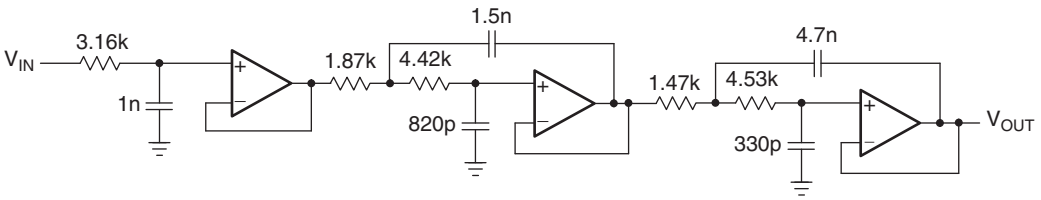

Figure 20.22: Fifth order unity gain Butterworth low pass filter.

20.4 High Pass Filter Design

By replacing the resistors of a low pass filter with capacitors and its capacitors with resistors, a high pass filter is created (Figure 20.23).

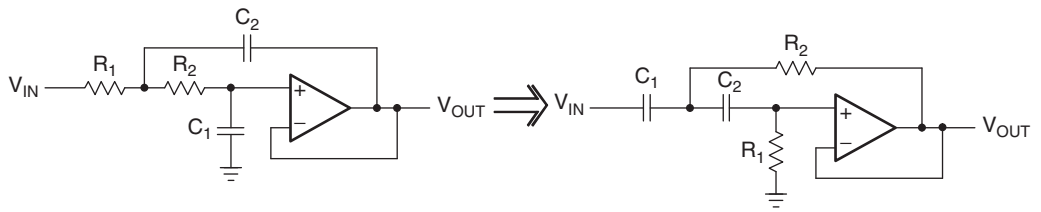

Figure 20.23: Low pass to high pass transition through components exchange.

To plot the gain response of a high pass filter (Figure 20.24), mirror the gain response of a low pass filter at the corner frequency, $\Omega = 1$, thus replacing Ω with $1/\Omega$ and S with $1/S$ in Equation (20.1).

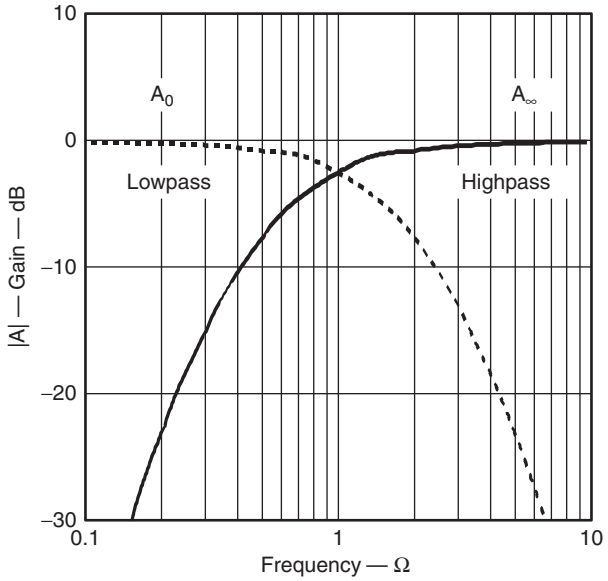

Figure 20.24: Developing the gain response of a high pass filter.

The general transfer function of a high pass filter is then

$$A(S) = \frac{A_\infty}{\prod_i \left(1 + \frac{a_i}{S} + \frac{b_i}{S^2}\right)} \tag{20.4}$$

with A_∞ being the passband gain.

Since Equation (20.4) represents a cascade of second order high pass filters, the transfer function of a single stage is

$$A_i(S) = \frac{A_\infty}{\left(1 + \frac{a_i}{S} + \frac{b_i}{S^2}\right)} \tag{20.5}$$

With $b = 0$ for all first order filters, the transfer function of a first order filter simplifies to

$$A(S) = \frac{A_0}{1 + \frac{a_i}{S}} \tag{20.6}$$

20.4.1 First Order High Pass Filter

Figures 20.25 and 20.26 show a first order high pass filter in the noninverting and inverting configurations.

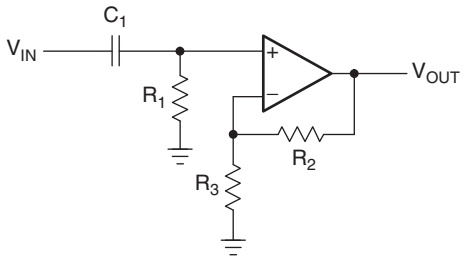

Figure 20.25: First order noninverting high pass filter.

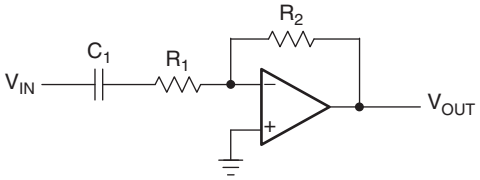

Figure 20.26: First order inverting high pass filter.

The transfer functions of the circuits are

$$A(S) = \frac{1 + \dfrac{R_2}{R_3}}{1 + \dfrac{1}{\omega_c R_1 C_1} \times \dfrac{1}{S}}$$

and

$$A(S) = -\frac{\dfrac{R_2}{R_1}}{1 + \dfrac{1}{\omega_c R_1 C_1} \times \dfrac{1}{S}}$$

The negative sign indicates that the inverting amplifier generates a 180° phase shift from the filter input to the output.

The coefficient comparison between the two transfer functions and Equation (20.6) provides two passband gain factors:

$$A_\infty = 1 + \frac{R_2}{R_3}$$

and

$$A_\infty = -\frac{R_2}{R_1}$$

while the term for the coefficient a_1 is the same for both circuits:

$$a_1 = \frac{1}{\omega_c R_1 C_1}$$

To dimension the circuit, specify the corner frequency (f_C), the DC gain (A_∞), and capacitor (C_1), then solve for R_1 and R_2:

$$R_1 = \frac{1}{2\pi f_c a_1 C_1}$$

$$R_2 = R_3(A_\infty - 1) \text{ and } R_2 = -R_1 A_\infty$$

20.4.2 Second Order High Pass Filter

High pass filters use the same two topologies as the low pass filters: Sallen-Key and multiple feedback. The only difference is that the positions of the resistors and the capacitors have changed.

Sallen-Key Topology

The general Sallen-Key topology in Figure 20.27 allows for separate gain setting via $A_0 = 1 + R_4/R_3$.

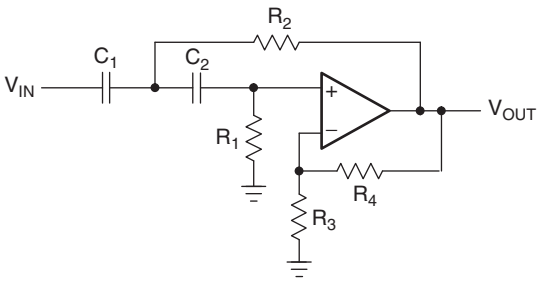

Figure 20.27: General Sallen-Key high pass filter.

The transfer function of the circuit in Figure 20.27 is

$$A(S) = \frac{\alpha}{1 + \dfrac{R_2(C_1 + C_2) + R_1C_2(1 - \alpha)}{\omega_c R_1 R_2 C_1 C_2} \times \dfrac{1}{S} + \dfrac{1}{\omega_c R_1 R_2 C_1 C_2} \times \dfrac{1}{S^2}}$$

with

$$\alpha = 1 + \frac{R_4}{R_3}$$

The unity gain topology in Figure 20.28 is usually applied in low Q filters with high gain accuracy.

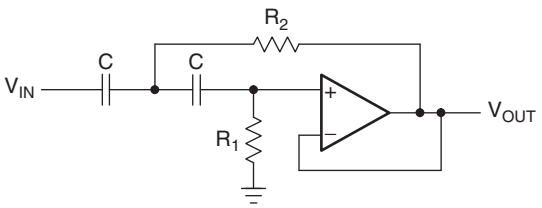

Figure 20.28: Unity gain Sallen-Key high pass filter.

To simplify the circuit design, it is common to choose unity gain ($\alpha = 1$) and $C_1 = C_2 = C$. The transfer function of the circuit in Figure 20.28 then simplifies to

$$A(S) = \frac{1}{1 + \frac{2}{\omega_c R_1 C} \times \frac{1}{S} + \frac{2}{\omega_c^2 R_1 R_2 C^2} \times \frac{1}{S^2}}$$

The coefficient comparison between this transfer function and Equation (20.5) yields

$$A_\infty = 1$$

$$a_1 = \frac{2}{\omega_c R_1 C}$$

$$b_1 = \frac{1}{\omega_c^2 R_1 R_2 C^2}$$

Given C, the resistor values for R_1 and R_2 are calculated through

$$R_1 = \frac{1}{\pi f_c C a_1}$$

$$R_2 = \frac{a_1}{4\pi f_c C b_1}$$

Multiple Feedback Topology

The MFB topology is commonly used in filters that have high Q values and require a high gain.

To simplify the computation of the circuit, capacitors C_1 and C_3 assume the same value ($C_1 = C_3 = C$), as shown in Figure 20.29.

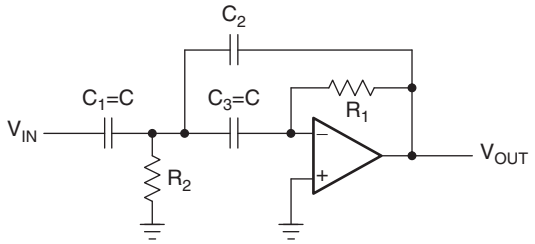

Figure 20.29: Second order MFB high pass filter.

The transfer function of the circuit in Figure 20.29 is

$$A(S) = \frac{-\frac{C}{C_2}}{1 + \frac{2C_2 + C}{\omega_c R_1 C_2 C} \times \frac{1}{S} + \frac{2C_2 + C}{\omega_c^2 R_2 R_1 C_2 C} \times \frac{1}{S^2}}$$

Through coefficient comparison with Equation (20.5), obtain the following relations:

$$A_\infty = \frac{C}{C_2}$$

$$a_1 = \frac{2C + C_2}{\omega_c R_1 C C_2}$$

$$b_1 = \frac{2C + C_2}{\omega_c R_1 C C_2}$$

Given capacitors C and C_2 and solving for resistors R_1 and R_2,

$$R_1 = \frac{1 - 2A_\infty}{2\pi f_c \times C \times a_1}$$

$$R_2 = \frac{a_1}{2\pi f_c \times b_1 C_2 (1 - 2A_\infty)}$$

The passband gain (A_∞) of an MFB high pass filter can vary significantly due to the wide tolerances of the two capacitors, C and C_2. To keep the gain variation at a minimum, it is necessary to use capacitors with tight tolerance values.

20.4.3 Higher Order High Pass Filter

As with the low pass filters, higher order high pass filters are designed by cascading first order and second order filter stages. The filter coefficients are the same ones used for the low pass filter design and are listed in the coefficient tables (Tables 20.7 through 20.13 in Section 20.9).

Example 20.4. Third Order High Pass Filter with $f_C = 1$ kHz The task is to design a third order unity gain Bessel high pass filter with the corner frequency $f_C = 1$ kHz.

Obtain the coefficients for a third order Bessel filter from Table 20.7, Section 20.9, shown here in Table 20.3, and compute each partial filter by specifying the capacitor values and calculating the required resistor values.

Table 20.3: Example 20.4 Filters

	a_i	b_i
Filter 1	$a_1 = 0.756$	$b_1 = 0$
Filter 2	$a_2 = 0.9996$	$b_2 = 0.4772$

For the first filter, with $C_1 = 100$ nF,

$$R_1 = \frac{1}{2\pi f_c a_1 C_1} = \frac{1}{2\pi \times 10^3\,\text{Hz} \times 0.756 \times 100 \times 10^{-9}\,\text{F}} = 2.105\ \text{k}\Omega$$

The closest 1% value is 2.1 kΩ.

For the second filter, with C = 100 nF,

$$R_1 = \frac{1}{\pi f_c C a_1} = \frac{1}{\pi \times 10^3 \times 100 \times 10^{-9} \times 0.756} = 3.18\ \text{k}\Omega$$

The closest 1% value is 3.16 kΩ.

$$R_2 = \frac{a_1}{4\pi f_c C b_1} = \frac{0.9996}{4\pi \times 10^3 \times 100 \times 10^{-9} \times 0.4772} = 1.67\ \text{k}\Omega$$

The closest 1% value is 1.65 kΩ.

Figure 20.30 shows the final filter circuit.

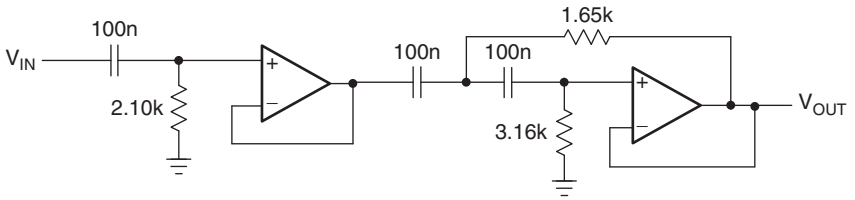

Figure 20.30: Third order unity gain Bessel high pass filter.

20.5 Bandpass Filter Design

In Section 20.4, a high pass response was generated by replacing the term S in the low pass transfer function with the transformation $1/S$. Likewise, a bandpass characteristic is generated by replacing the S term with the transformation

$$\frac{1}{\Delta\Omega}\left(S + \frac{1}{S}\right) \tag{20.7}$$

In this case, the passband characteristic of a low pass filter is transformed into the upper passband half of a bandpass filter. The upper passband is then mirrored at the mid frequency, f_m ($\Omega = 1$), into the lower passband half (Figure 20.31).

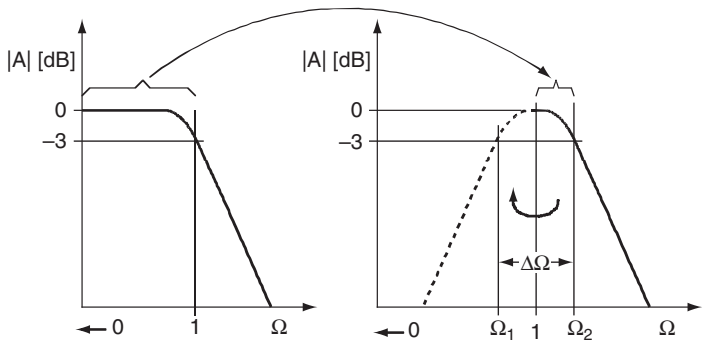

Figure 20.31: Low pass to bandpass transition.

The corner frequency of the low pass filter transforms to the lower and upper –3 dB frequencies of the bandpass, Ω_1 and Ω_2. The difference between both frequencies is defined as the normalized bandwidth $\Delta\Omega$:

$$\Delta\Omega = \Omega_2 - \Omega_1$$

The normalized mid frequency, where $Q = 1$, is

$$\Omega_m = 1 = \Omega_2 \times \Omega_1$$

In analogy to the resonant circuits, the quality factor Q is defined as the ratio of the mid frequency (f_m) to the bandwidth (B):

$$Q = \frac{f_m}{B} = \frac{f_m}{f_2 - f_1} = \frac{1}{\Omega_2 - \Omega_1} = \frac{1}{\Delta\Omega} \tag{20.8}$$

The simplest design of a bandpass filter is the connection of a high pass filter and a low pass filter in series, which is commonly done in wideband filter applications. Thus, a first order high pass filter and a first order low pass provide a second order bandpass, while a second order high pass filter and a second order low pass result in a fourth order bandpass response.

In comparison to wideband filters, narrowband filters of higher order consist of cascaded second order bandpass filters that use the Sallen-Key or the multiple feedback topology.

20.5.1 Second Order Bandpass Filter

To develop the frequency response of a second order bandpass filter, apply the transformation in Equation (20.7) to a first order low pass transfer function:

$$A(S) = \frac{A_0}{1 + S}$$

Replacing S with

$$\frac{1}{\Delta\Omega}\left(S + \frac{1}{S}\right)$$

yields the general transfer function for a second order bandpass filter:

$$A(S) = \frac{A_0 \times \Delta\Omega \times S}{1 + \Delta\Omega + S^2} \tag{20.9}$$

When designing bandpass filters, the parameters of interest are the gain at the mid frequency (A_m) and the quality factor (Q), which represents the selectivity of a bandpass filter.

Therefore, replace A_0 with A_m and $\Delta\Omega$ with $1/Q$, Equation (20.7), and obtain

$$A(S) = \frac{\frac{A_m}{Q} \times S}{1 + \frac{1}{Q} \times S + S^2} \tag{20.10}$$

Figure 20.32 shows the normalized gain response of a second order bandpass filter for different Q values.

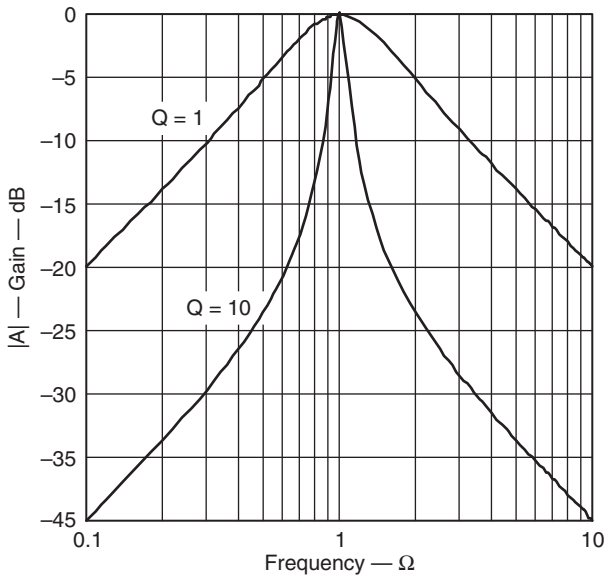

Figure 20.32: Gain response of a second order bandpass filter.

The graph shows that the frequency response of second order bandpass filters gets steeper with rising Q, making the filter more selective.

Sallen-Key Topology

The Sallen-Key bandpass circuit in Figure 20.33 has the following transfer function:

$$A(S) = \frac{G \times RC\omega_m \times S}{1 + RC\omega_M(3 - G) \times S + R^2C^2\omega_m^2 \times S^2}$$

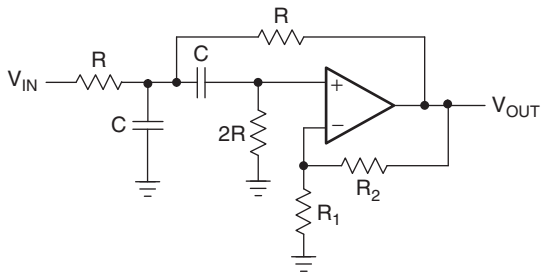

Figure 20.33: Sallen-Key bandpass filter.

Through coefficient comparison with Equation (20.10), obtain the following equations:

$$\text{Mid frequency}: f_m = \frac{1}{2\pi RC}$$

$$\text{Inner gain}: G = 1 + \frac{R_2}{R_1}$$

$$\text{Gain at } f_m: A_m = \frac{G}{3 - G}$$

$$\text{Filter quality}: Q = \frac{1}{3 - G}$$

The Sallen-Key circuit has the advantage that the quality factor (Q) can be varied via the inner gain (G) without modifying the mid frequency (f_m). A drawback is, however, that Q and A_m cannot be adjusted independently.

Care must be taken when G approaches the value of 3, because then A_m becomes infinite and causes the circuit to oscillate.

To set the mid frequency of the bandpass, specify f_m and C then solve for R:

$$R = \frac{1}{2\pi f_m C}$$

Because of the dependency between Q and A_m, there are two options to solve for R_2, either set the gain at mid frequency,

$$R_2 = \frac{2A_m - 1}{1 + A_m}$$

or design for a specified Q,

$$R_2 = \frac{2Q - 1}{Q}$$

Multiple Feedback Topology

The MFB bandpass circuit in Figure 20.34 has the following transfer function:

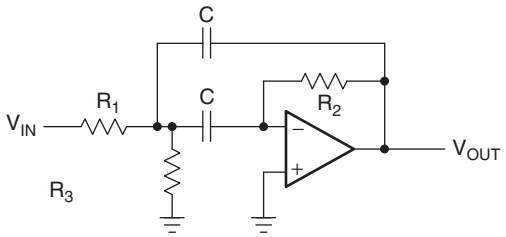

Figure 20.34: MFB bandpass filter.

$$A(S) = \frac{-\frac{R_2R_3}{R_1 + R_3}C\omega_m \times S}{1 + \frac{2R_1R_3}{R_1 + R_3}C\omega \times S + \frac{R_1R_2R_3}{R_1 + R_3}C^2 \times \omega_m^2 \times S^2}$$

The coefficient comparison with Equation (20.9) yields the following equations:

$$\text{Mid frequency}: f_m = \frac{1}{1\pi C}\sqrt{\frac{R_1 + R_3}{R_1R_2R_3}}$$

$$\text{Gain at } f_m: -A_m = \frac{R_2}{2R_1}$$

$$\text{Filter quality}: Q = \pi f_m R_2 C$$

$$\text{Bandwidth}: B = \frac{1}{\pi R_2 C}$$

The MFB bandpass allows adjusting Q, A_m, and f_m independently. The bandwidth and gain factor do not depend on R_3. Therefore, R_3 can be used to modify the mid frequency without affecting bandwidth, B, or gain, A_m. For low values of Q, the filter can work without R_3, however, Q then depends on A_m via

$$-A_m = 2Q^2$$

Example 20.5. Second Order MFB Bandpass Filter with $f_m = 1$ kHz To design a second order MFB bandpass filter with a mid frequency of $f_m = 1$ kHz, a quality factor of $Q = 10$, and a gain of $A_m = -2$, assume a capacitor value of $C = 100$ nF and solve the previous equations for R_1 through R_3 in the following sequence:

$$R_2 = \frac{Q}{\pi f_m C} = \frac{10}{\pi \times 1\ \text{kHz} \times 100\ \text{nF}} = 31.8\,\text{k}\Omega$$

$$R_1 = \frac{R_2}{-2A_m} = \frac{31.8\ \text{k}\Omega}{4} = 7.96\ \text{k}\Omega$$

$$R_3 = \frac{-A_m R_1}{2Q^2 + A_m} = \frac{2 \times 7.96\ \text{k}\Omega}{200 - 2} = 80.4\ \Omega$$

20.5.2 Fourth Order Bandpass Filter (Staggered Tuning)

Figure 20.32 shows that the frequency response of second order bandpass filters gets steeper with rising Q. However, some bandpass applications require a flat gain response close to the mid frequency as well as a sharp passband to stop band transition. These tasks can be accomplished by higher order bandpass filters.

Of particular interest is the application of the low pass to bandpass transformation onto a second order low pass filter, since it leads to a fourth order bandpass filter.

Replacing the S term in Equation (20.2) with Equation (20.7) gives the general transfer function of a fourth order bandpass:

$$A(S) = \frac{\dfrac{S^2 \times A_0(\Delta\Omega)^2}{b_1}}{1 + \dfrac{a_1}{b_1}\Delta\Omega \times S + \left[2 + \dfrac{(\Delta\Omega)^2}{b_1}\right] \times S_2 + \dfrac{a_1}{b_1}\Delta\Omega \times S^3 + S^4} \tag{20.11}$$

Similar to the low pass filters, the fourth order transfer function is split into two second order bandpass terms. Further mathematical modifications yield

$$A(S) = \frac{\dfrac{A_{mi}}{Q_i} \times \alpha S}{\left[1 + \dfrac{\alpha S}{Q_1} + (\alpha S)^2\right]} \times \frac{\dfrac{A_{mi}}{Q_i} \times \dfrac{S}{\alpha}}{\left[1 + \dfrac{1}{Q_i}\left(\dfrac{S}{\alpha}\right) + \left(\dfrac{S}{\alpha}\right)^2\right]} \tag{20.12}$$

Equation (20.12) represents the connection of two second order bandpass filters in series, where

- A_{mi} is the gain at the mid frequency, f_{mi}, of each partial filter.
- Q_i is the pole quality of each filter.
- α and $1/\alpha$ are the factors by which the mid frequencies of the individual filters, f_{m1} and f_{m2}, derive from the mid frequency, f_m, of the overall bandpass.

In a fourth order bandpass filter with high Q, the mid frequencies of the two partial filters differ only slightly from the overall mid frequency. This method is called *staggered tuning*.

Factor α needs to be determined through successive approximation using Equation (20.13):

$$\alpha^2 = \left[\frac{\alpha \times \Delta\Omega \times a_1}{b_1(1 + \alpha)^2}\right]^2 + \frac{1}{\alpha^2} - 2 - \frac{(\Delta\Omega)^2}{b_1} = 0 \tag{20.13}$$

with a_1 and b_1 being the second order low pass coefficients of the desired filter type.

To simplify the filter design, Table 20.4 lists those coefficients and provides the α values for three quality factors, $Q = 1$, $Q = 10$, and $Q = 100$.

Table 20.4: Values of α for Different Filter Types

Bessel				**Butterworth**				**Tschebyscheff**			
a_1	1.3617			a_1	1.4142			a_1	1.0650		
b_1	0.6180			b_1	1.0000			b_1	1.9305		
Q	100	10	1	Q	100	10	1	Q	100	10	1
$\Delta\Omega$	0.01	0.1	1	$\Delta\Omega$	0.01	0.1	1	$\Delta\Omega$	0.01	0.1	1
α	1.0032	1.0324	1.438	α	1.0035	1.036	1.4426	α	1.0033	1.0338	1.39

After α has been determined, all quantities of the partial filters can be calculated using the following equations.

The mid frequency of filter 1 is

$$f_{m1} = \frac{f_m}{\alpha} \tag{20.14}$$

and the mid frequency of filter 2 is

$$f_{m2} = f_m \times \alpha \tag{20.15}$$

with f_m being the mid frequency of the overall forth order bandpass filter.

The individual pole quality, Q_i, is the same for both filters:

$$Q_i = Q \times \frac{(1 + \alpha^2)b_1}{\alpha \times a_1} \tag{20.16}$$

with Q being the quality factor of the overall filter.

The individual gain (A_{mi}) at the partial mid frequencies, f_{m1} and f_{m2}, is the same for both filters:

$$A_{mi} = \frac{Q_i}{Q} \times \sqrt{\frac{A_m}{B_1}} \tag{20.17}$$

with A_m being the gain at mid frequency, f_m, of the overall filter.

Example 20.6. Fourth Order Butterworth Bandpass Filter The task is to design a fourth order Butterworth bandpass filter with the following parameters:

- Mid frequency, $f_m = 10$ kHz.
- Bandwidth, $B = 1000$ Hz.
- Gain, $A_m = 1$.

From Table 20.4, the following values are obtained:

- $a_1 = 1.4142$.
- $b_1 = 1$.
- $\alpha = 1.036$.

In accordance with Equations (20.14) and (20.15), the mid frequencies for the partial filters are

$$f_{mi} = \frac{10\ \text{kHz}}{1.036} = 9.653\ \text{kHz}$$

and

$$f_{m2} = 10\ \text{kHz} \times 1.036 = 10.36\ \text{kHz}$$

The overall Q is defined as $Q = f_m/B$, and for this example results in $Q = 10$.

Using Equation (20.16), the Q_i of both filters is

$$Q_i = 10 \times \frac{\left(1 + 1.036^2\right) \times 1}{1.036 \times 1.4142} = 14.15$$

With Equation (20.17), the passband gain of the partial filters at f_{m1} and f_{m2} calculates to

$$A_{mi} = \frac{14.15}{10} \times \sqrt{\frac{1}{1}} = 1.415$$

Equations (20.16) and (20.17) show that Q_i and A_{mi} of the partial filters need to be independently adjusted. The only circuit that accomplishes this task is the MFB bandpass filter in Section 20.5.1.

To design the individual second order bandpass filters, specify $C = 10$ nF, and insert the previously determined quantities for the partial filters into the resistor equations of the MFB bandpass filter. The resistor values for both partial filters are calculated in Table 20.5.

Table 20.5: Resistor Values for Both Partial Filters

Filter 1	Filter 2
$R_{21} = \frac{Q_i}{\pi f_{m1} C} = \frac{14.15}{\pi \times 9.653\ \text{kHz} \times 10\ \text{nF}} = 46.7\ \text{k}\Omega$	$R_{22} = \frac{Q_i}{\pi f_{m2} C} = \frac{14.15}{\pi \times 10.36\ \text{kHz} \times 10\ \text{nF}} = 43.5\ \text{k}\Omega$
$R_{11} = \frac{R_{21}}{-2A_{mi}} = \frac{46.7\ \text{k}\Omega}{-2 \times -1.415} = 16.5\ \text{k}\Omega$	$R_{12} = \frac{R_{22}}{-2A_{mi}} = \frac{43.5}{-2 \times -1.415} = 15.4\ \text{k}\Omega$
$R_{31} = 2\frac{-A_{mi}R_{11}}{2Q_i^2 + A_{mi}} = \frac{1.415 \times 16.5\ \text{k}\Omega}{2 \times 14.15^2 + 1.415} = 58.1\ \Omega$	$R_{32} = \frac{A_{mi}R_{12}}{2Q_i^2 + A_{mi}} = \frac{1.415 \times 15.4\ \text{k}\Omega}{2 \times 14.15^2 + 1.415} = 54.2\ \Omega$

Figure 20.35 compares the gain response of a fourth order Butterworth bandpass filter with $Q = 1$ and its partial filters to the fourth order gain of Example 20.4 with $Q = 10$.

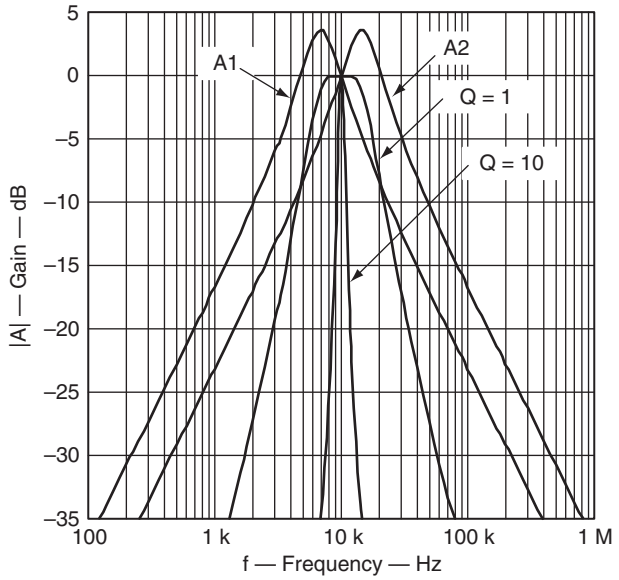

Figure 20.35: Gain responses of a fourth order Butterworth bandpass and its partial filters.

20.6 Band Rejection Filter Design

A band rejection filter is used to suppress a certain frequency rather than a range of frequencies.

Two of the most popular band rejection filters are the active twin T and the active Wien-Robinson circuits, both of which are second order filters.

To generate the transfer function of a second order band rejection filter, replace the S term of a first order low pass response with the transformation in Equation (20.18):

$$\frac{\Delta\Omega}{S + \frac{1}{S}} \tag{20.18}$$

which gives

$$A(S) = \frac{A_0(1 + S^2)}{1 + \Delta\Omega \times S + S_2} \tag{20.19}$$

Thus, the passband characteristic of the low pass filter is transformed into the lower passband of the band rejection filter. The lower passband is then mirrored at the mid frequency, f_m ($\Omega = 1$), into the upper passband half (Figure 20.36).

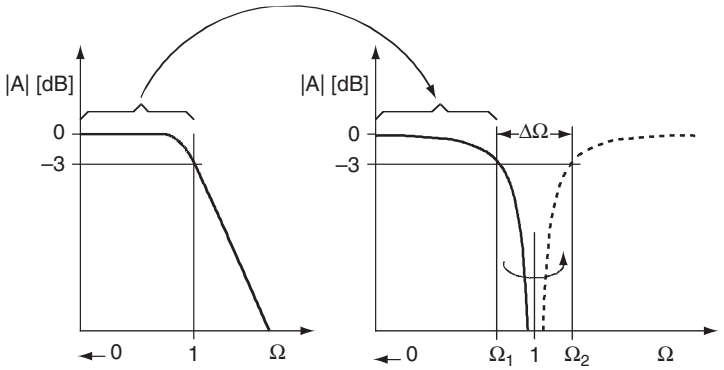

Figure 20.36: Low pass to band rejection transition.

The corner frequency of the low pass filter transforms to the lower and upper –3 dB frequencies of the band rejection filter, Ω_1 and Ω_2. The difference between both frequencies is the normalized bandwidth $\Delta\Omega$:

$$\Delta\Omega = \Omega_{\max} - \Omega_{\min}$$

Identical to the selectivity of a bandpass filter, the quality of the filter rejection is defined as

$$Q = \frac{f_m}{B} = \frac{1}{\Delta\Omega}$$

Therefore, replacing $\Delta\Omega$ in Equation (20.19) with $1/Q$ yields

$$A(S) = \frac{A_0(1 + S^2)}{1 + \frac{1}{Q} \times S + S^2} \tag{20.20}$$

20.6.1 Active Twin T Filter

The original twin T filter, shown in Figure 20.37, is a passive RC network with a quality factor of $Q = 0.25$. To increase Q, the passive filter is implemented into the feedback loop of an amplifier, turning into an active band rejection filter, shown in Figure 20.38.

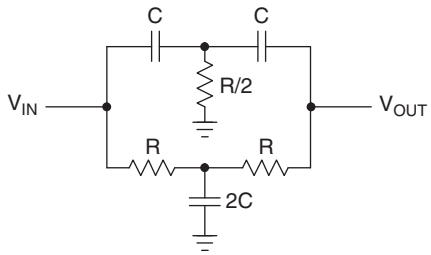

Figure 20.37: Passive twin T filter.

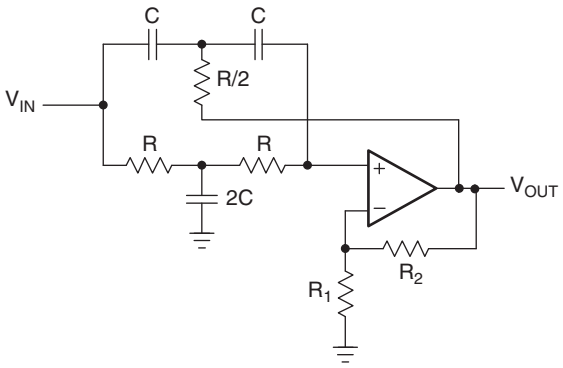

Figure 20.38: Active twin T filter.

The transfer function of the active twin T filter is

$$A(S) = \frac{k(1 + S^2)}{1 + 2(2 - k) \times S + S^2} \tag{20.21}$$

Comparing the variables of Equation (20.21) with Equation (20.20) provides the equations that determine the filter parameters:

$$\text{Mid frequency}: f_m = \frac{1}{2\pi RC}$$

$$\text{Inner gain}: G = 1 + \frac{R_2}{R_1}$$

$$\text{Passband gain}: A_0 = G$$

$$\text{Rejection quality}: Q = \frac{1}{2(2 - G)}$$

The twin T circuit has the advantage that the quality factor (Q) can be varied via the inner gain (G) without modifying the mid frequency (f_m). However, Q and A_m cannot be adjusted independently.

To set the mid frequency of the bandpass, specify f_m and C, then solve for R:

$$R = \frac{1}{2\pi f_m C}$$

Because of the dependency between Q and A_m, there are two options to solve for R_2, either set the gain at mid frequency,

$$R_2 = (A_0 - 1)R_1$$

or design for a specific Q,

$$R_2 = R_1\left(1 - \frac{1}{2Q}\right)$$

20.6.2 Active Wien-Robinson Filter

The Wien-Robinson bridge in Figure 20.39 is a passive band rejection filter with differential output. The output voltage is the difference between the potential of a constant voltage divider and the output of a bandpass filter. Its Q factor is close to that of the twin T circuit. To achieve higher values of Q, the filter is connected into the feedback loop of an amplifier.

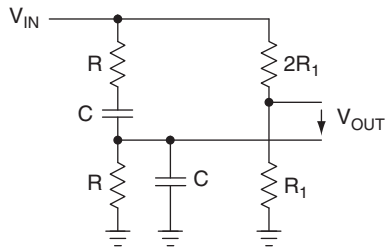

Figure 20.39: Passive Wien-Robinson bridge.

The active Wien-Robinson filter in Figure 20.40 has the transfer function

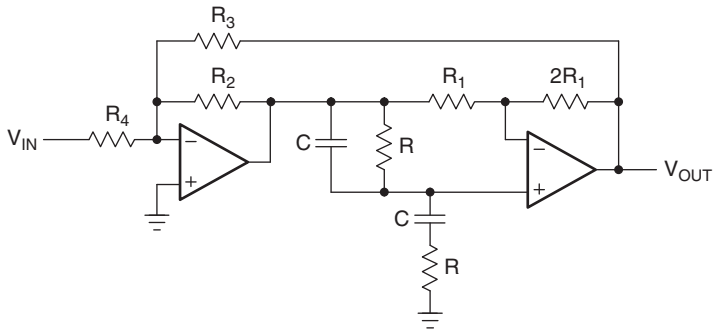

Figure 20.40: Active Wien-Robinson filter.

$$A(S) = -\frac{\dfrac{\beta}{1+\alpha}\left(1+S^2\right)}{1+\dfrac{3}{1+\alpha}\times S+S^2} \tag{20.22}$$

with $\alpha = R_2/R_3$ and $\beta = R_2/R_4$.

Comparing the variables of Equation (20.22) with Equation (20.20) provides the equations that determine the filter parameters:

$$\text{Mid frequency}: f_m = \frac{1}{2\pi RC}$$

$$\text{Passband gain}: A_0 = -\frac{\beta}{1+\alpha}$$

$$\text{Rejection quality}: Q = \frac{1+\alpha}{3}$$

To calculate the individual component values, establish the following design procedure:

1. Define f_m and C and calculate R with

$$R = \frac{1}{2\pi f_m C}$$

2. Specify Q and determine α via $\alpha = 3q - 1$.
3. Specify A_0 and determine β via $\beta = -A_0 \times 3Q$.
4. Define R_2 and calculate R_3 and R_4 with $R_3 = R_2/\alpha$ and $R_4 = R_2/\beta$.

In comparison to the twin T circuit, the Wien-Robinson filter allows modification of the passband gain, A_0, without affecting the quality factor, Q.

If f_m is not completely suppressed due to component tolerances of R and C, a fine-tuning of the resistor $2R_2$ is required.

Figure 20.41 shows a comparison between the filter response of a passive band rejection filter with $Q = 0.25$ and an active second order filter with $Q = 1$ and $Q = 10$.

20.7 All Pass Filter Design

In comparison to the previously discussed filters, an all pass filter has a constant gain across the entire frequency range and a phase response that changes linearly with frequency. Because of these properties, all pass filters are used in phase compensation and signal delay circuits.

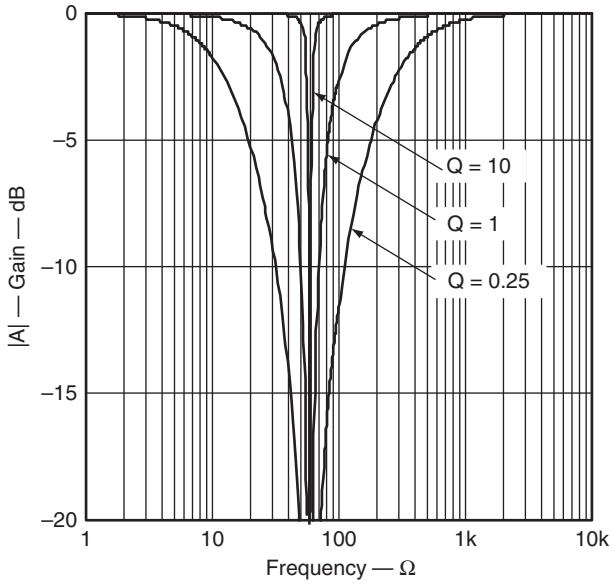

Figure 20.41: Comparison of Q between passive and active band rejection filters.

Similar to the low pass filters, all pass circuits of higher order consist of cascaded first order and second order all pass stages. To develop the all pass transfer function from a low pass response, replace A_0 with the conjugate complex denominator.

The general transfer function of an all pass filter is then

$$A(S) = \frac{\prod_i \left(1 - a_i S + b_i S^2\right)}{\prod_i \left(1 + a_i S + b_i S^2\right)} \tag{20.23}$$

with a_i and b_i being the coefficients of a partial filter. The all pass coefficients are listed in Table 20.13 of Section 20.9.

Expressing Equation (20.23) in magnitude and phase yields

$$A(s) = \frac{\prod_i \sqrt{\left(1 - b_i\Omega^2\right)^2 + a_i^2\Omega^2} \times e^{-ja}}{\prod_i \sqrt{\left(1 - b_i\Omega^2\right)^2 + a_i^2\Omega^2} \times e^{+ja}} \tag{20.24}$$

This gives a constant gain of 1 and a phase shift, φ, of

$$\varphi = -2\alpha = -2\sum_i \arctan\frac{a_i\Omega}{1 - b_i\Omega^2} \tag{20.25}$$

To transmit a signal with minimum phase distortion, the all pass filter must have a constant group delay across the specified frequency band. The group delay is the time by which the all pass filter delays each frequency within that band.

The frequency at which the group delay drops to $1/\sqrt{2}$ times its initial value is the corner frequency, f_C.

The group delay is defined through

$$t_{\text{gr}} = -\frac{d\varphi}{d\omega} \tag{20.26}$$

To present the group delay in normalized form, refer t_{gr} to the period of the corner frequency, T_C, of the all pass circuit:

$$T_{\text{gr}} = \frac{t_{\text{gr}}}{T_c} = t_{\text{gr}} \times f_c = t_{\text{gr}} \times \frac{\omega_c}{2\pi} \tag{20.27}$$

Substituting t_{gr} through Equation (20.26) gives

$$T_{\text{gr}} = -\frac{1}{2\pi} \times \frac{d\varphi}{d\Omega} \tag{20.28}$$

Inserting the φ term in Equation (20.25) into Equation (20.28) and completing the derivation results in

$$T_{\text{gr}} = \frac{1}{\pi}\sum_i \frac{a_i\left(1 + b_i\Omega^2\right)}{1 + \left(a_1^2 - 2b_1\right) \times \Omega^2 + b_1^2\Omega^4} \tag{20.29}$$

Setting $\Omega = 0$ in Equation (20.29) gives the group delay for the low frequencies, $0 < \Omega < 1$, which is

$$T_{gr0} = \frac{1}{\pi}\sum_i a_i \tag{20.30}$$

The values for T_{gr0} are listed in Table 20.13, Section 20.9, from the first to the tenth order.

In addition, Figure 20.42 shows the group delay response versus the frequency for the first 10 orders of all pass filters.

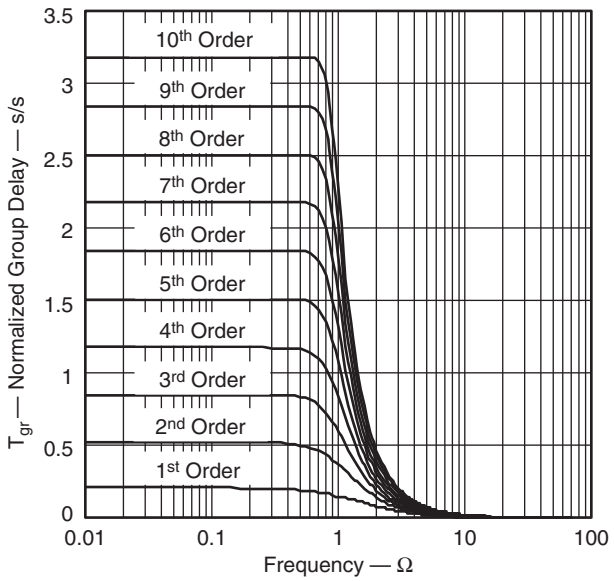

Figure 20.42: Frequency response of the group delay for the first 10 filter orders.

20.7.1 First Order All Pass Filter

Figure 20.43 shows a first order all pass filter with a gain of +1 at low frequencies and a gain of –1 at high frequencies. Therefore, the magnitude of the gain is 1, while the phase changes from 0° to –180°.

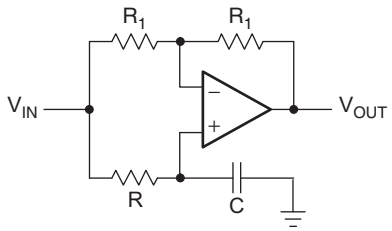

Figure 20.43: First order all pass filter.

The transfer function of this circuit is

$$A(s) = \frac{1 - RC\omega_c \times s}{1 + RC\omega_c \times s}$$

The coefficient comparison with Equation (20.23) ($b_1 = 1$) results in

$$a_i = RC \times 2\pi f_c \tag{20.31}$$

To design a first order all pass, specify f_C and C and then solve for R:

$$R = \frac{a_i}{2\pi f_c \times C} \tag{20.32}$$

Inserting Equation (20.31) into (20.30) and substituting ω_C with Equation (20.27) provides the maximum group delay of a first order all pass filter:

$$t_{gr0} = 2RC \tag{20.33}$$

20.7.2 Second Order All Pass Filter

Figure 20.44 shows that one possible design for a second order all pass filter is to subtract the output voltage of a second order bandpass filter from its input voltage.

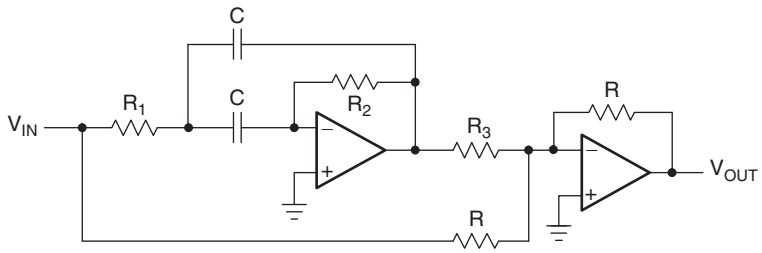

Figure 20.44: Second order all pass filter.

The transfer function of the circuit in Figure 20.44 is

$$A(S) = \frac{1 + (2R_1 - \alpha R_2)C\omega_c \times S + R_1R_2C^2\omega_c^2 \times S^2}{1 + 2R_1C\omega_c \times S + R_1R_2C^2\omega_c^2 \times S^2}$$

The coefficient comparison with Equation (20.23) yields

$$a_1 = 4\pi f_c R_1 C \tag{20.34}$$

$$b_1 = a_1 \pi f_c R_2 C \tag{20.35}$$

$$\alpha = \frac{a_1^2}{b_1} = \frac{R}{R_3} \tag{20.36}$$

To design the circuit, specify f_C, C, and R, then solve for the resistor values:

$$R_1 = \frac{a_1}{4\pi f_c C} \tag{20.37}$$

$$R_2 = \frac{b_1}{a_1 \pi f_c C} \tag{20.38}$$

$$R_3 = \frac{R}{\alpha} \tag{20.39}$$

Inserting Equation (20.34) into Equation (20.30) and substituting ω_C with Equation (20.27) gives the maximum group delay of a second order all pass filter:

$$t_{gr0} = 4R_1C \tag{20.40}$$

20.7.3 Higher Order All Pass Filter

Higher order all pass filters consist of cascaded first order and second order filter stages.

Example 20.7. All Pass Filter with a 2 ms Delay A signal with the frequency spectrum $0 < f < 1$ kHz needs to be delayed by 2 ms. To keep the phase distortions at a minimum, the corner frequency of the all pass filter must be $f_C \geq 1$ kHz.

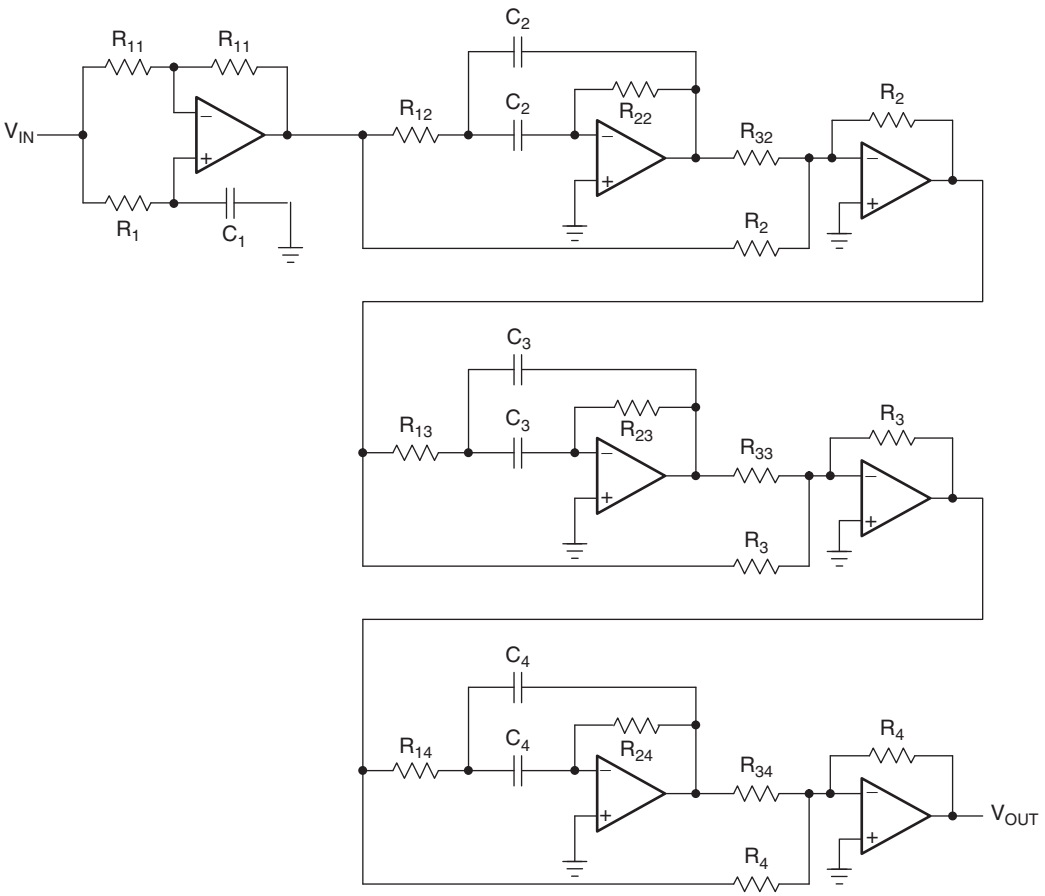

Figure 20.45: Seventh order all pass filter.

Equation (20.27) determines the normalized group delay for frequencies below 1 kHz:

$$T_{gr0} = \frac{t_{gr0}}{T_c} = 2 \text{ ms} \times 1 \text{ kHz} = 2.0$$

Figure 20.42 confirms that a seventh order all pass is needed to accomplish the desired delay. The exact value, however, is $T_{gr0} = 2.1737$. To set the group delay to precisely 2 ms, solve Equation (20.27) for f_C and obtain the corner frequency:

$$f_C = \frac{T_{gr0}}{t_{gr0}} = 1.087 \text{ kHz}$$

To complete the design, look up the filter coefficients for a seventh order all pass filter, specify C, and calculate the resistor values for each partial filter.

Cascading the first order all pass with the three second order stages results in the desired seventh order all pass filter.

20.8 Practical Design Hints

This section introduces DC biasing techniques for filter designs in single supply applications, which are usually not required when operating with dual supplies. It also provides recommendations on selecting the type and value range of capacitors and resistors as well as the decision criteria for choosing the correct op amp.

20.8.1 Filter Circuit Biasing

The filter diagrams in this chapter are drawn for dual supply applications. The op amp operates from a positive and a negative supply, while the input and the output voltage are referenced to ground (Figure 20.46).

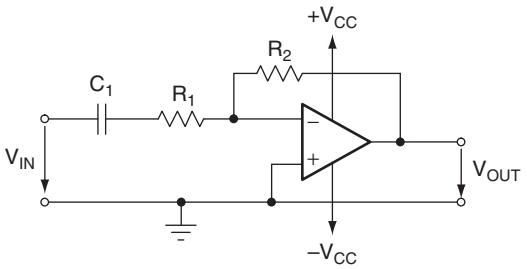

Figure 20.46: Dual supply filter circuit.

For the single supply circuit in Figure 20.47, the lowest supply voltage is ground. For a symmetrical output signal, the potential of the noninverting input is level shifted to midrail.

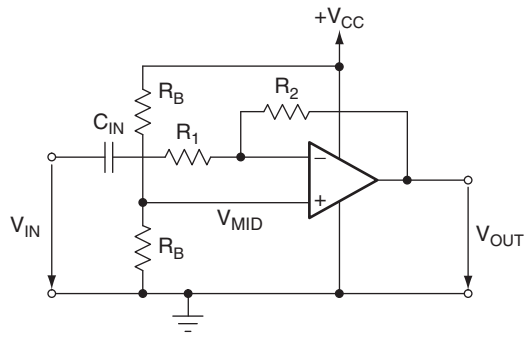

Figure 20.47: Single supply filter circuit.

The coupling capacitor, C_{IN} in Figure 20.47, AC couples the filter, blocking any unknown DC level in the signal source. The voltage divider, consisting of the two equal bias resistors R_B, divides the supply voltage to V_{MID} and applies it to the inverting op amp input.

For simple filter input structures, passive RC networks often provide a low cost biasing solution. In the case of more complex input structures, such as the input of a second order low pass filter, the RC network can affect the filter characteristic. Then, it is necessary to either include the biasing network into the filter calculations or insert an input buffer between biasing network and the actual filter circuit, as shown in Figure 20.48.

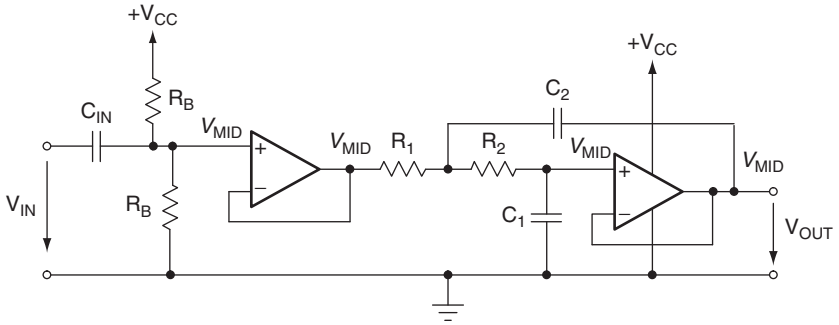

Figure 20.48: Biasing a Sallen-Key low pass filter.

C_{IN} AC-couples the filter, blocking any DC level in the signal source. V_{MID} is derived from V_{CC} via the voltage divider. The op amp operates as a voltage follower and as an impedance converter. V_{MID} is applied via the DC path, R_1 and R_2, to the noninverting input of the filter amplifier.

Note that the parallel circuit of the resistors, R_B, together with C_{IN} create a high pass filter. To avoid any effect on the low pass characteristic, the corner frequency of the input high pass filter must be low versus the corner frequency of the actual low pass filter.

The use of an input buffer causes no loading effects on the low pass filter, thus keeping the filter calculation simple.

In the case of a higher order filter, all following filter stages receive their bias level from the preceding filter amplifier.

Figure 20.49 shows the biasing of a multiple feedback low pass filter.

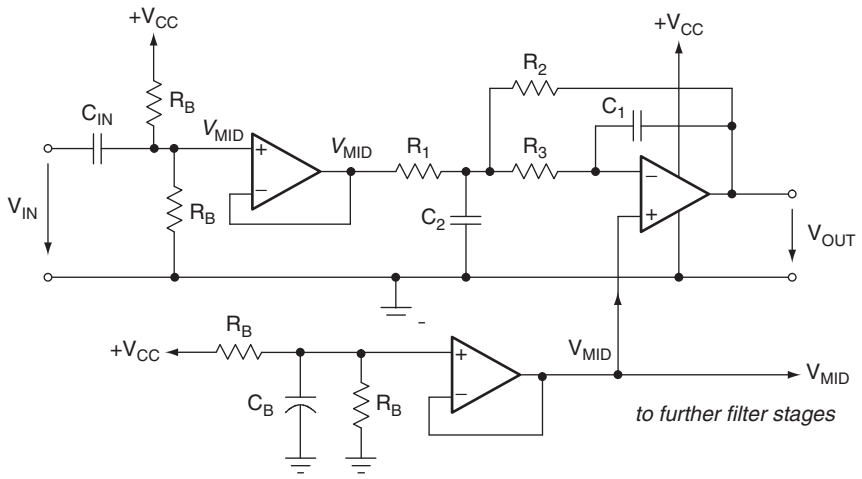

Figure 20.49: Biasing a second order MFB low pass filter.

The input buffer decouples the filter from the signal source. The filter itself is biased via the noninverting amplifier input. For that purpose, the bias voltage is taken from the output of a V_{MID} generator with low output impedance. The op amp operates as a difference amplifier and subtracts the bias voltage of the input buffer from the bias voltage of the V_{MID} generator, thus yielding a DC potential of V_{MID} at zero input signal.

A low cost alternative is to remove the op amp and use a passive biasing network instead. However, to keep loading effects at a minimum, the values for R_B must be significantly higher than without the op amp.

The biasing of a Sallen-Key and an MFB high pass filter is shown in Figure 20.50.

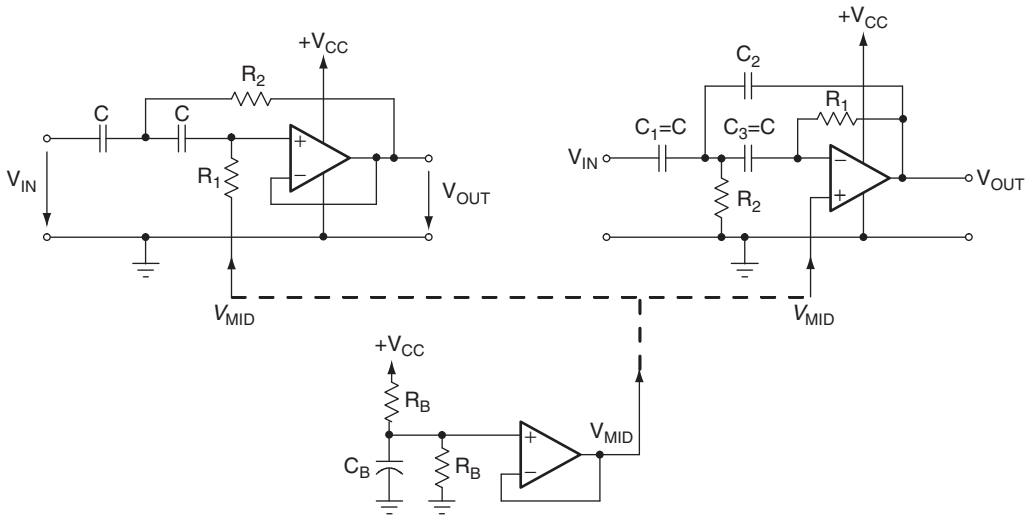

Figure 20.50: Biasing a Sallen-Key and an MFB high pass filter.

The input capacitors of high pass filters already provide the AC coupling between filter and signal source. Both circuits use the V_{MID} generator from Figure 20.50 for biasing. While the MFB circuit is biased at the noninverting amplifier input, the Sallen-Key high pass filter is biased via the only DC path available, which is R_1. In the AC circuit, the input signals travel via the low output impedance of the op amp to ground.

20.8.2 Capacitor Selection

The tolerance of the selected capacitors and resistors depends on the filter sensitivity and performance. Sensitivity is the measure of the vulnerability of a filter's performance to changes in component values. The important filter parameters to consider are the corner frequency, f_C, and Q.

For example, when Q changes by $\pm 2\%$ due to a $\pm 5\%$ change in the capacitance value, the sensitivity of Q to capacity changes is expressed as $s(Q/C) = 2\%/5\% = 0.4(\%/\%)$. The following sensitivity approximations apply to second order Sallen-Key and MFB filters:

$$s\frac{Q}{C} \approx s\frac{Q}{C} \approx s\frac{f_c}{C} \approx \pm 0.5\frac{\%}{\%}$$

Although 0.5%/% is a small difference from the ideal parameter, in the case of higher order filters, the combination of small Q and f_C differences in each partial filter can significantly modify the overall filter response from its intended characteristic.

Figures 20.51 and 20.52 show how an intended eighth order Butterworth low pass can turn into a low pass filter with a Tschebyscheff characteristic, mainly due to capacitance changes from the partial filters.

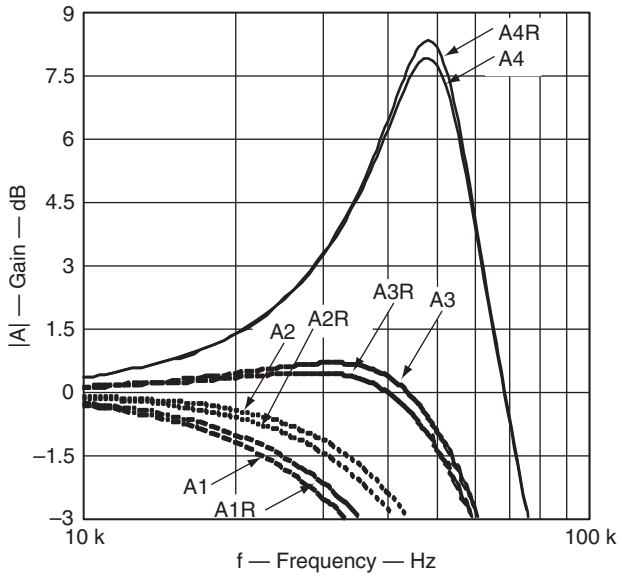

Figure 20.51: Differences in Q and f_C in the partial filters of an eighth order Butterworth low pass filter.

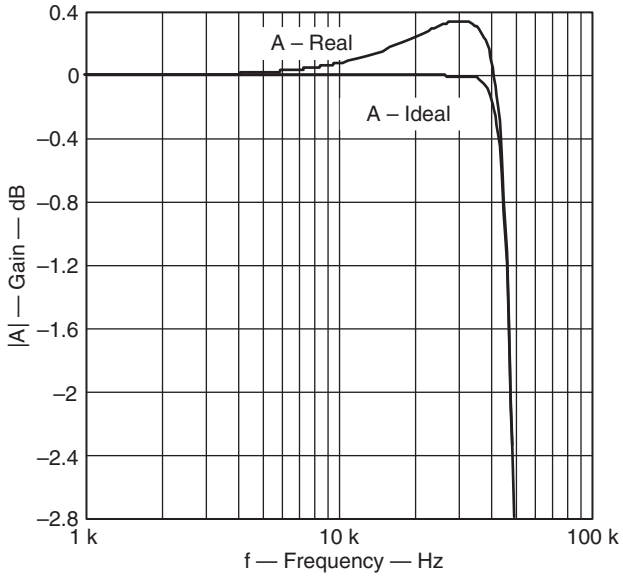

Figure 20.52: Modification of the intended Butterworth response to a Tschebyscheff type characteristic.

Figure 20.51 shows the differences between the ideal and the actual frequency responses of the four partial filters. The overall filter responses are shown in Figure 20.52. The difference between ideal and real response peaks with 0.35 dB at approximately 30 kHz, which is equivalent to an enormous 4.1% gain error, can be seen.

If this filter is intended for a data acquisition application, it could be used at best in a 4 bit system. In comparison, if the maximum full scale error of a 12 bit system is given with ½ LSB, then maximum passband deviation would be –0.001 dB, or 0.012%.

To minimize the variations of f_C and Q, NPO (COG) ceramic capacitors are recommended for high performance filters. These capacitors hold their nominal value over a wide temperature and voltage range. The various temperature characteristics of ceramic capacitors are identified by a three symbol code, such as COG, X7R, Z5U, and Y5V.

COG type ceramic capacitors are the most precise. Their nominal values range from 0.5 pF to approximately 47 nF with initial tolerances from ±0.25 pF for smaller values and up to ±1% for higher values. Their capacitance drift over temperature is typically 30 PPM/°C.

X7R type ceramic capacitors range from 100 pF to 2.2 μF with an initial tolerance of +1% and a capacitance drift over temperature of ±15%.

For higher values, tantalum electrolytic capacitors should be used.

Other precision capacitors are silver mica, metallized polycarbonate, and for high temperatures, polypropylene or polystyrene.

Since capacitor values are not as finely subdivided as resistor values, the capacitor values should be defined prior to selecting resistors. If precision capacitors are not available to provide an accurate filter response, then it is necessary to measure the individual capacitor values and calculate the resistors accordingly.

For high performance filters, 0.1% resistors are recommended.

20.8.3 Component Values

Resistor values should stay within the range of 1 kΩ to 100 kΩ. The lower limit avoids excessive current draw from the op amp output, which is particularly important for single supply op amps in power sensitive applications. Those amplifiers have typical output currents of between 1 mA and 5 mA. At a supply voltage of 5 V, this current translates to a minimum of 1 kΩ. The upper limit of 100 kΩ is to avoid excessive resistor noise.

Capacitor values can range from 1 nF to several microfarads. The lower limit avoids coming too close to parasitic capacitances. If the common mode input capacitance of the op amp, used in a Sallen-Key filter section, is close to 0.25% of C_1, (C_1/400), it must be considered for accurate filter response. The MFB topology, in comparison, does not require input capacitance compensation.

20.8.4 Op Amp Selection

The most important op amp parameter for proper filter functionality is the unity gain bandwidth. In general, the open loop gain (A_{OL}) should be 100 times (40 dB above) the peak gain (Q) of a filter section to allow a maximum gain error of 1% (Figure 20.53).

The following equations are good rules of thumb to determine the necessary unity gain bandwidth of an op amp for an individual filter section.

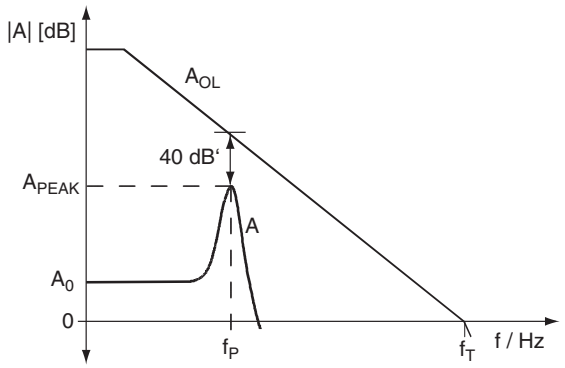

Figure 20.53: Open loop gain (A_{OL}) and filter response (A).

1. First order filter:

$$f_T = 100 \times \text{Gain} \times f_c$$

2. Second order filter ($Q < 1$):

$$f_T = 100 \times \text{Gain} \times f_c \times k_i \text{ with } k_i = f_{ci}/f_c$$

3. Second order filter ($Q > 1$):

$$f_T = 100 \times \text{Gain} \times \frac{f_C}{a_i}\sqrt{\frac{Q_i^2 - 0.5}{Q_i^2 - 0.25}}$$

For example, a fifth order, 10 kHz, Tschebyscheff low pass filter with 3 dB passband ripple and a DC gain of $A_0 = 2$ has its worst case Q in the third filter section. With $Q_3 = 8.82$ and $a_3 = 0.1172$, the op amp needs to have a unity gain bandwidth of

$$f_T = 100 \times 2 \times \frac{10 \text{ kHz}}{0.1172}\sqrt{\frac{8.82^2 - 0.5}{8.82^2 - 0.25}} = 17 \text{ MHz}$$

In comparison, a fifth order unity gain, 10 kHz, Butterworth low pass filter has a worst case Q of $Q_3 = 1.62$; $a_3 = 0.618$. Due to the lower Q value, f_T is also lower and calculates to only

$$f_T = 100 \times \frac{10 \text{ kHz}}{0.618} \sqrt{\frac{1.62^2 - 0.5}{1.62^2 - 0.25}} = 1.5 \text{ MHz}$$

Besides good DC performance, low noise, and low signal distortion, another important parameter that determines the speed of an op amp is the slew rate (SR). For adequate full power response, the slew rate must be greater than

$$\text{SR} = \pi \times V_{\text{PP}} \times fC$$

For example, a single supply, 100 kHz filter with 5 V_{PP} output requires a slew rate of at least

$$\text{SR} = \Pi \times 5\text{V} \times \ 100 \text{ kHz} = 1.57 \text{ V}/\mu\text{s}$$

Texas Instruments offers a wide range of op amps for high performance filters in single supply applications. Table 20.6 provides a selection of single supply amplifiers sorted in order of rising slew rate.

Table 20.6: Single Supply Op Amp Selection Guide ($T_A = 25°C$, $V_{CC} = 5$ V)

Op amp	BW (MHz)	FPR (kHz)	SR (V/μs)	V_{IO} (mV)	Noise (nV/Hz)
TLV2721	0.51	11	0.18	0.6	20
TLC2201A	1.8	159	2.5	0.6	8
TLV2771A	4.8	572	9	1.9	21
TLC071	10	1000	16	1.5	7
TLE2141	5.9	2800	45	0.5	10.5
THS4001	270	127 MHz (1 V_{PP})	400	6	7.5

20.9 Filter Coefficient Tables

The following tables contain the coefficients for the three filter types: Bessel and Butterworth (Tables 20.7 and 20.8) and Tschebyscheff. The Tschebyscheff tables (Tables 20.9 through 20.12) are split into categories for the following passband ripples: 0.5 dB, 1 dB, 2 dB, and 3 dB.

The table headers consist of the following quantities:

n = the filter order.

i = the number of the partial filter.

a_i, b_i = are the filter coefficients.

k_i = the ratio of the corner frequency of a partial filter, f_{Ci}, to the corner frequency of the overall filter, f_C. This ratio is used to determine the unity gain bandwidth of the op amp as well as to simplify the test of a filter design by measuring f_{Ci} and comparing it to f_C.

Q_i = the quality factor of the partial filter.

f_i/f_C = the ratio is used for test purposes of the all pass filters, where f_i is the frequency, at which the phase is 180° for a second order filter, respectively, 90° for a first order all pass filter.

T_{gr0} = the normalized group delay of the overall all pass filter.

Table 20.7: Bessel Coefficients

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
1	1	1.0000	0.0000	1.000	–
2	1	1.3617	0.6180	1.000	0.58
3	1	0.7560	0.0000	1.323	–
	2	0.9996	0.4772	1.414	0.69
4	1	1.3397	0.4889	0.978	0.52
	2	0.7743	0.3890	1.797	0.81

Table 20.7: Bessel Coefficients (Cont'd)

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
5	1	0.6656	0.0000	1.502	–
	2	1.1402	0.4128	1.184	0.56
	3	0.6216	0.3245	2.138	0.92
6	1	1.2217	0.3887	1.063	0.51
	2	0.9686	0.3505	1.431	0.61
	3	0.5131	0.2756	2.447	1.02
7	1	0.5937	0.0000	1.648	–
	2	1.0944	0.3395	1.207	0.53
	3	0.8304	0.3011	1.695	0.66
	4	0.4332	0.2381	2.731	1.13
8	1	1.1112	0.3162	1.164	0.51
	2	0.9754	0.2979	1.381	0.56
	3	0.7202	0.2621	1.963	0.71
	4	0.3728	0.2087	2.992	1.23
9	1	0.5386	0.0000	1.857	–
	2	1.0244	0.2834	1.277	0.52
	3	0.8710	0.2636	1.574	0.59
	4	0.6320	0.2311	2.226	0.76
	5	0.3257	0.1854	3.237	1.32
10	1	1.0215	0.2650	1.264	0.50
	2	0.9393	0.2549	1.412	0.54
	3	0.7815	0.2351	1.780	0.62
	4	0.5604	0.2059	2.479	0.81
	5	0.2883	0.1665	3.466	1.42

Table 20.8: Butterworth Coefficients

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
1	1	1.0000	0.0000	1.000	—
2	1	1.4142	1.0000	1.000	0.71
3	1	1.0000	0.0000	1.000	—
	2	1.0000	1.0000	1.272	1.00
4	1	1.8478	1.0000	0.719	0.54
	2	0.7654	1.0000	1.390	1.31
5	1	1.0000	0.0000	1.000	—
	2	1.6180	1.0000	0.859	0.62
	3	0.6180	1.0000	1.448	1.62
6	1	1.9319	1.0000	0.676	0.52
	2	1.4142	1.0000	1.000	0.71
	3	0.5176	1.0000	1.479	1.93
7	1	1.0000	0.0000	1.000	—
	2	1.8019	1.0000	0.745	0.55
	3	1.2470	1.0000	1.117	0.80
	4	0.4450	1.0000	1.499	2.25
8	1	1.9616	1.0000	0.661	0.51
	2	1.6629	1.0000	0.829	0.60
	3	1.1111	1.0000	1.206	0.90
	4	0.3902	1.0000	1.512	2.56
9	1	1.0000	0.0000	1.000	—
	2	1.8794	1.0000	0.703	0.53
	3	1.5321	1.0000	0.917	0.65
	4	1.0000	1.0000	1.272	1.00
	5	0.3473	1.0000	1.521	2.88

Table 20.8: Butterworth Coefficients (Cont'd)

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
10	1	1.9754	1.0000	0.655	0.51
	2	1.7820	1.0000	0.756	0.56
	3	1.4142	1.0000	1.000	0.71
	4	0.9080	1.0000	1.322	1.10
	5	0.3129	1.0000	1.527	3.20

Table 20.9: Tschebyscheff Coefficients for 0.5 dB Passband Ripple

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
1	1	1.0000	0.0000	1.000	—
2	1	1.3614	1.3827	1.000	0.86
3	1	1.8636	0.0000	0.537	—
	2	0.0640	1.1931	1.335	1.71
4	1	2.6282	3.4341	0.538	0.71
	2	0.3648	1.1509	1.419	2.94
5	1	2.9235	0.0000	0.342	—
	2	1.3025	2.3534	0.881	1.18
	3	0.2290	1.0833	1.480	4.54
6	1	3.8645	6.9797	0.366	0.68
	2	0.7528	1.8573	1.078	1.81
	3	0.1589	1.0711	1.495	6.51
7	1	4.0211	0.0000	0.249	—
	2	1.8729	4.1795	0.645	1.09
	3	0.4861	1.5676	1.208	2.58
	4	0.1156	1.0443	1.517	8.84

(*Continued*)

Table 20.9: Tschebyscheff Coefficients for 0.5 dB Passband Ripple (Cont'd)

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
8	1	5.1117	11.9607	0.276	0.68
	2	1.0639	2.9365	0.844	1.61
	3	0.3439	1.4206	1.284	3.47
	4	0.0885	1.0407	1.521	11.53
9	1	5.1318	0.0000	0.195	—
	2	2.4283	6.6307	0.506	1.06
	3	0.6839	2.2908	0.989	2.21
	4	0.2559	1.3133	1.344	4.48
	5	0.0695	1.0272	1.532	14.58
10	1	6.3648	18.3695	0.222	0.67
	2	1.3582	4.3453	0.689	1.53
	3	0.4822	1.9440	1.091	2.89
	4	0.1994	1.2520	1.381	5.61
	5	0.0563	1.0263	1.533	17.99

Table 20.10: Tschebyscheff Coefficients for 1 dB Passband Ripple

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
1	1	1.0000	0.0000	1.000	—
2	1	1.3022	1.5515	1.000	0.96
3	1	2.2156	0.0000	0.451	—
	2	0.5442	1.2057	1.353	2.02
4	1	2.5904	4.1301	0.540	0.78
	2	0.3039	1.1697	1.417	3.56

Table 20.10: Tschebyscheff Coefficients for 1 dB Passband Ripple (Cont'd)

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
5	1	3.5711	0.0000	0.280	—
	2	1.1280	2.4896	0.894	1.40
	3	0.1872	1.0814	1.486	5.56
6	1	3.8437	8.5529	0.366	0.76
	2	0.6292	1.9124	1.082	2.20
	3	0.1296	1.0766	1.493	8.00
7	1	4.9520	0.0000	0.202	—
	2	1.6338	4.4899	0.655	1.30
	3	0.3987	1.5834	1.213	3.16
	4	0.0937	1.0432	1.520	10.90
8	1	5.1019	14.7608	0.276	0.75
	2	0.8916	3.0426	0.849	1.96
	3	0.2806	1.4334	1.285	4.27
	4	0.0717	1.0432	1.520	14.24
9	1	6.3415	0.0000	0.158	—
	2	2.1252	7.1711	0.514	1.26
	3	0.5624	2.3278	0.994	2.71
	4	0.2076	1.3166	1.346	5.53
	5	0.0562	1.0258	1.533	18.03
10	1	6.3634	22.7468	0.221	0.75
	2	1.1399	4.5167	0.694	1.86
	3	0.3939	1.9665	1.093	3.56
	4	0.1616	1.2569	1.381	6.94
	5	0.0455	1.0277	1.532	22.26

Table 20.11: Tschebyscheff Coefficients for 2 dB Passband Ripple

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
1	1	1.0000	0.0000	1.000	—
2	1	1.1813	1.7775	1.000	1.13
3	1	2.7994	0.0000	0.357	—
	2	0.4300	1.2036	1.378	2.55
4	1	2.4025	4.9862	0.550	0.93
	2	0.2374	1.1896	1.413	4.59
5	1	4.6345	0.0000	0.216	—
	2	0.9090	2.6036	0.908	1.78
	3	0.1434	1.0750	1.493	7.23
6	1	3.5880	10.4648	0.373	0.90
	2	0.4925	1.9622	1.085	2.84
	3	0.0995	1.0826	1.491	10.46
7	1	6.4760	0.0000	0.154	—
	2	1.3258	4.7649	0.665	1.65
	3	0.3067	1.5927	1.218	4.12
8	1	4.7743	18.1510	0.282	0.89
	2	0.6991	3.1353	0.853	2.53
	3	0.2153	1.4449	1.285	5.58
	4	0.0547	1.0461	1.518	18.39
9	1	8.3198	0.0000	0.120	—
	2	1.7299	7.6580	0.522	1.60
	3	0.4337	2.3549	0.998	3.54
	4	0.1583	1.3174	1.349	7.25
	5	0.0427	1.0232	1.536	23.68

Table 20.11: Tschebyscheff Coefficients for 2 dB Passband Ripple (Cont'd)

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
10	1	5.9618	28.0376	0.226	0.89
	2	0.8947	4.6644	0.697	2.41
	3	0.3023	1.9858	1.094	4.66
	4	0.1233	1.2614	1.380	9.11
	5	0.0347	1.0294	1.531	29.27

Table 20.12: Tschebyscheff Coefficients for 3 dB Passband Ripple

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
1	1	1.0000	0.0000	1.000	—
2	1	1.0650	1.9305	1.000	1.30
3	1	3.3496	0.0000	0.299	—
	2	0.3559	1.1923	1.396	3.07
4	1	2.1853	5.5339	0.557	1.08
	2	0.1964	1.2009	1.410	5.58
5	1	5.6334	0.0000	0.178	—
	2	0.7620	2.6530	0.917	2.14
	3	0.1172	1.0686	1.500	8.82
6	1	3.2721	11.6773	0.379	1.04
	2	0.4077	1.9873	1.086	3.46
	3	0.0815	1.0861	1.489	12.78
7	1	7.9064	0.0000	0.126	—
	2	1.1159	4.8963	0.670	1.98
	3	0.2515	1.5944	1.222	5.02
	4	0.0582	1.0348	1.527	17.46

(*Continued*)

Table 20.12: Tschebyscheff Coefficients for 3 dB Passband Ripple (Cont'd)

n	i	a_i	b_i	$k_i = f_{Ci}/f_C$	Q_i
8	1	4.3583	20.2948	0.286	1.03
	2	0.5791	3.1808	0.855	3.08
	3	0.1765	1.4507	1.285	6.83
	4	0.0448	1.0478	1.517	22.87
9	1	10.1759	0.0000	0.098	—
	2	1.4585	7.8971	0.526	1.93
	3	0.3561	2.3651	1.001	4.32
	4	0.1294	1.3165	1.351	8.87
	5	0.0348	1.0210	1.537	29.00
10	1	5.4449	31.3788	0.230	1.03
	2	0.7414	4.7363	0.699	2.94
	3	0.2479	1.9952	1.094	5.70
	4	0.1008	1.2638	1.380	11.15
	5	0.0283	1.0304	1.530	35.85

Table 20.13: All Pass Coefficients

n	i	a_i	b_i	f_i/f_C	Q_i	T_{gr0}
1	1	0.6436	0.0000	1.554	—	0.2049
2	1	1.6278	0.8832	1.064	0.58	0.5181
3	1	1.1415	0.0000	0.876	—	0.8437
	2	1.5092	1.0877	0.959	0.69	
4	1	2.3370	1.4878	0.820	0.52	1.1738
	2	1.3506	1.1837	0.919	0.81	

Table 20.13: All Pass Coefficients (Cont'd)

n	i	a_i	b_i	f_i/f_C	Q_i	T_{gr0}
5	1	1.2974	0.0000	0.771	—	1.5060
	2	2.2224	1.5685	0.798	0.56	
	3	1.2116	1.2330	0.901	0.92	
6	1	2.6117	1.7763	0.750	0.51	1.8395
	2	2.0706	1.6015	0.790	0.61	
	3	1.0967	1.2596	0.891	1.02	
7	1	1.3735	0.0000	0.728	—	2.1737
	2	2.5320	1.8169	0.742	0.53	
	3	1.9211	1.6116	0.788	0.66	
	4	1.0023	1.2743	0.886	1.13	
8	1	2.7541	1.9420	0.718	0.51	2.5084
	2	2.4174	1.8300	0.739	0.56	
	3	1.7850	1.6101	0.788	0.71	
	4	0.9239	1.2822	0.883	1.23	
9	1	1.4186	0.0000	0.705	—	2.8434
	2	2.6979	1.9659	0.713	0.52	
	3	2.2940	1.8282	0.740	0.59	
	4	1.6644	1.6027	0.790	0.76	
	5	0.8579	1.2862	0.882	1.32	
10	1	2.8406	2.0490	0.699	0.50	3.1786
	2	2.6120	1.9714	0.712	0.54	
	3	2.1733	1.8184	0.742	0.62	
	4	1.5583	1.5923	0.792	0.81	
	5	0.8018	1.2877	0.881	1.42	

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CHAPTER 21

Fast, Practical Filter Design for Beginners

21.1 Introduction

The previous chapter presented a rigorous theoretical approach to filter design. Many designers prefer this method because it gives the most flexibility in filter design. Years of customer support, however, have revealed that the vast majority of designers want a working filter with the minimum effort and development time. This chapter presents a pragmatic, simple design methodology that allows a designer to implement all but the most complex filters rapidly and have a reasonable expectation that they will be producible.

To design a filter, these things must be known in advance:

- The frequencies that need to be passed and those that need to be rejected.
- A transition frequency, the point at which the filter starts to work or a center frequency around which the filter is symmetrical.
- An initial capacitor value—pick one somewhere from 100 pF for high frequencies to 0.1 μF for low frequencies. If the resulting resistor values are too large or too small, pick another capacitor value.

21.2 Picking the Response

For the beginner, the filter responses are presented pictorially in Figures 21.1 through 21.6. The shaded area represents the frequencies that will be passed, and the area in white the frequencies that will be rejected. Don't be concerned with the exact frequency yet, that will be taken care of in the following sections.

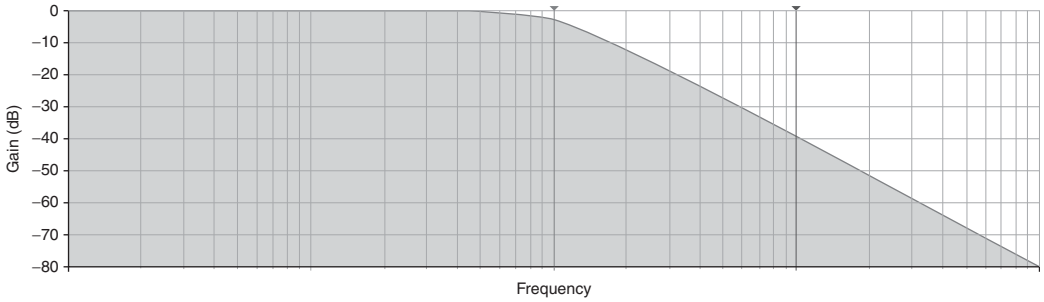


Figure 21.1: Low pass response, go to Section 21.3.

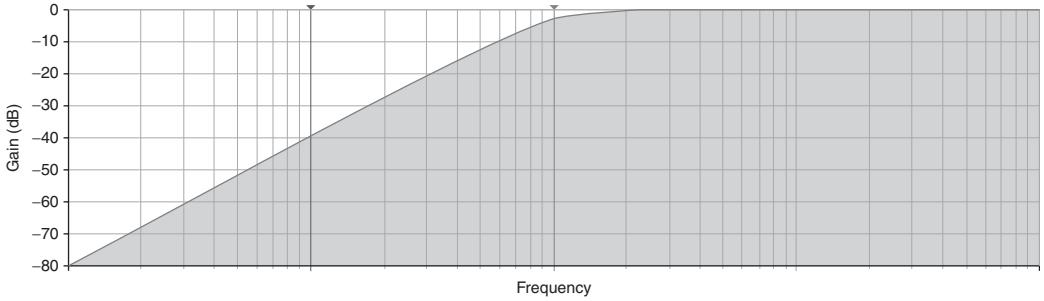


Figure 21.2: High pass response, go to Section 21.4.

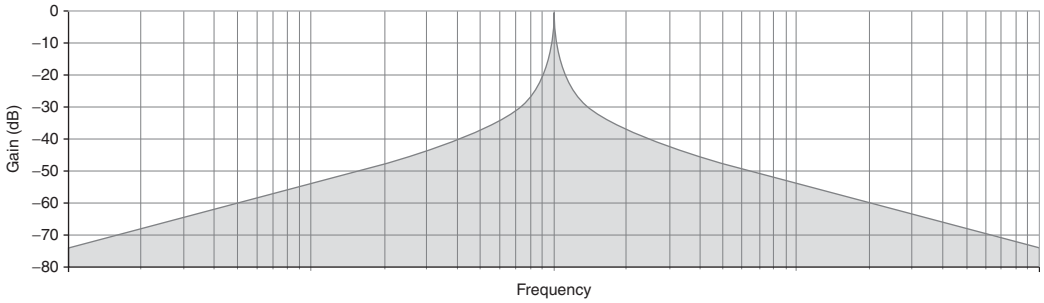


Figure 21.3: Narrow (single frequency) bandpass, go to Section 21.5.

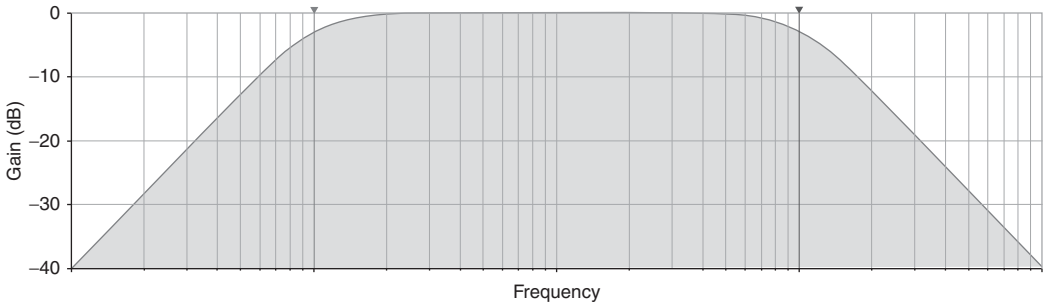


Figure 21.4: Wide bandpass, go to Section 21.6.

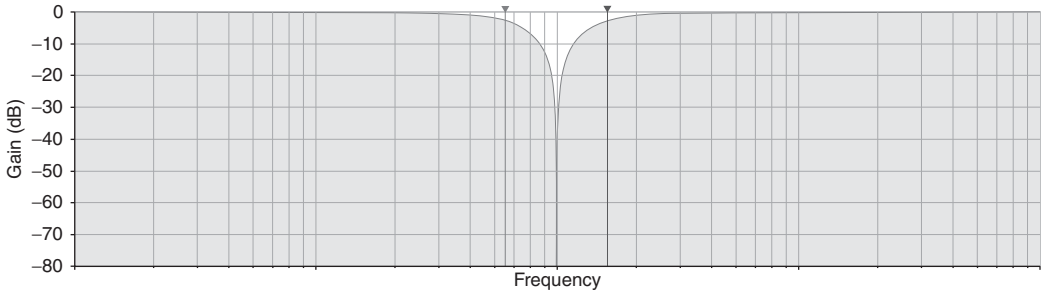


Figure 21.5: Notch (single frequency rejection) filter, go to Section 21.7.

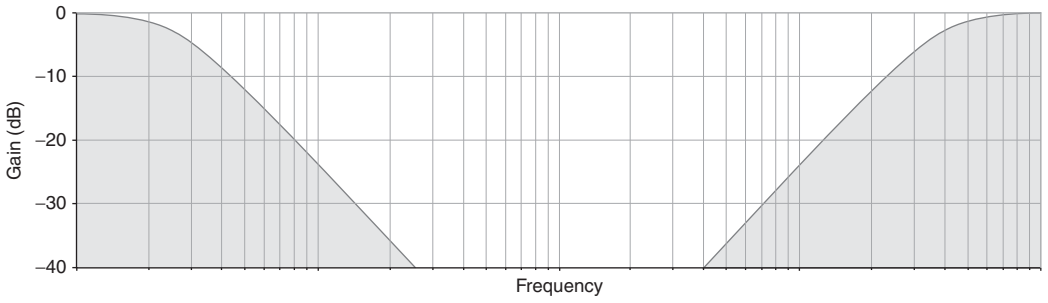


Figure 21.6: Wide band rejection, go to Section 21.8.

21.3 Low Pass Filter

Figure 21.7 shows a low pass filter.

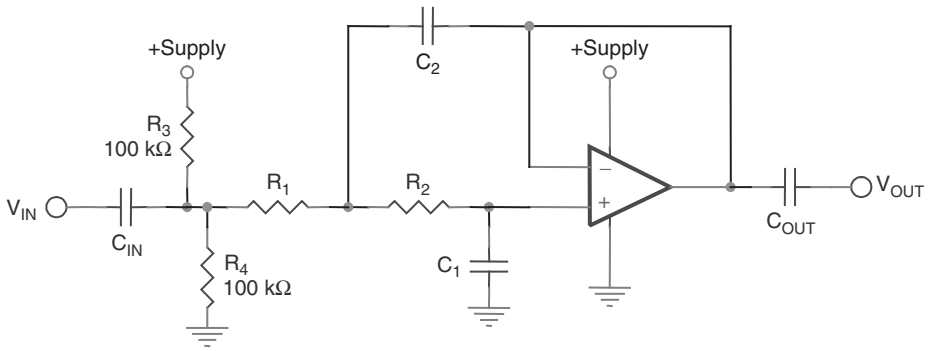


Figure 21.7: Low pass filter.

The design procedure is as follows:

- Pick C_1: _____
- Calculate $C_2 = C_1 \times 2$: _____
- Calculate R_1 and $R_2 = \dfrac{1}{2\sqrt{2} \times \pi \times C_1 \times \text{Frequency}}$: _____
- Calculate $C_{IN} = C_{OUT} =$ 100 to 1000 times C_1 (not critical): _____

Done!

Digging deeper, the filter selected is a unity gain Sallen-Key filter, with a Butterworth response characteristic. Note that, with the addition of C_{IN} and C_{OUT}, the filter is no longer purely a low pass filter. It is a wide bandpass filter, but the high pass response characteristic can be placed well below the frequencies of interest. If DC response is required, the circuit should be modified to operate off of split supplies.

21.4 High Pass Filter

Figure 21.8 shows a high pass filter.

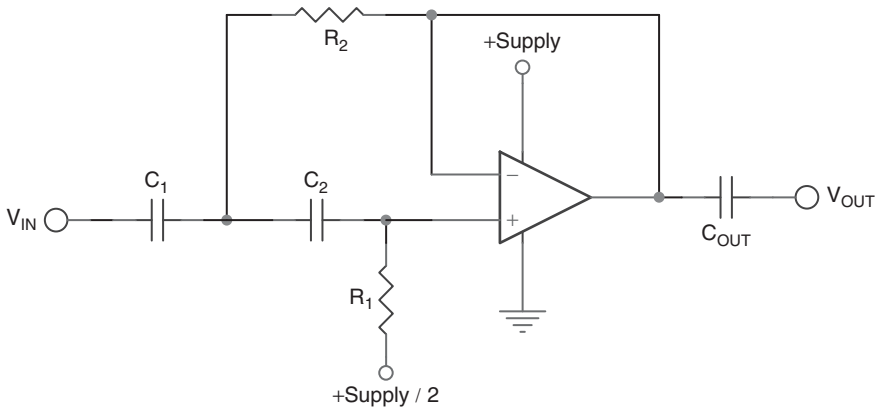


Figure 21.8: High pass filter.

The design procedure is as follows:

- Pick $C_1 = C_2 =$ _____
- Calculate $R_1 = \dfrac{1}{\sqrt{2} \times \pi \times C_1 \times \text{Frequency}} =$ _____
- Calculate $R_2 = \dfrac{1}{2\sqrt{2} \times \pi \times C_1 \times \text{Frequency}} =$ _____
- Calculate $C_{\text{OUT}} = 100$ to 1000 times C_1 (not critical) = _____

Done!

Digging deeper, the filter selected is a unity gain Sallen-Key filter, with a Butterworth response characteristic. Just as was the case with the low pass filter, there is no such thing as an active high pass filter—but for a different reason. The gain and bandwidth product of the op amp used ultimately produces a low pass response characteristic, making this a wide bandpass filter. It is the responsibility of the designer to choose an op amp with a frequency limit well above the bandwidth of interest.

21.5 Narrow (Single Frequency) Bandpass Filter

Figure 21.9 shows a narrow bandpass filter.

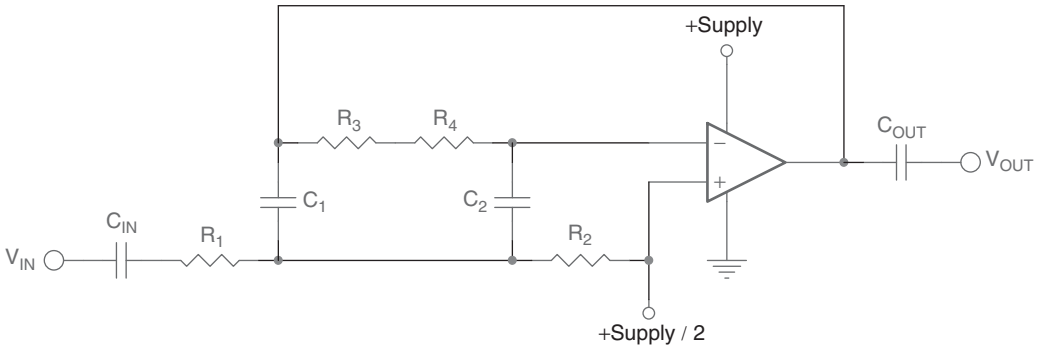


Figure 21.9: Narrow bandpass filter.

The design procedure is as follows:

- Pick $C_1 = C_2 =$ _____
- Calculate $R_1 = R_4 = \dfrac{1}{2 \times \pi \times C_1 \times \text{Frequency}} =$ _____
- Calculate $R_3 = 19 \times R_1$
- Calculate $R_2 = R_1/19$
- Calculate $C_{IN} = C_{OUT} = 100$ to 1000 times C_1 (not critical) = _____

Done!

Digging deeper, the filter selected is a modified Deliyannis filter. A Deliyannis filter is a special case of the MFB bandpass configuration, one that is very stable and relatively insensitive to component variation. The Q is set at 10, which also locks the gain at 10, as the two are related by the expression

$$\frac{R_3 + R_4}{2 \times R_1} = Q = \text{Gain}$$

A higher Q was not selected, because the op amp gain bandwidth product can be easily reached, even with a gain of 20 dB. At least 40 dB of headroom should be allowed above the center frequency peak. The op amp slew rate should also be sufficient to allow the waveform at the center frequency to swing to the amplitude required.

Digging even deeper, we look at the narrow versus wide bandpass filter (Figure 21.10). At what point is it better to implement a bandpass filter as a narrow or single frequency

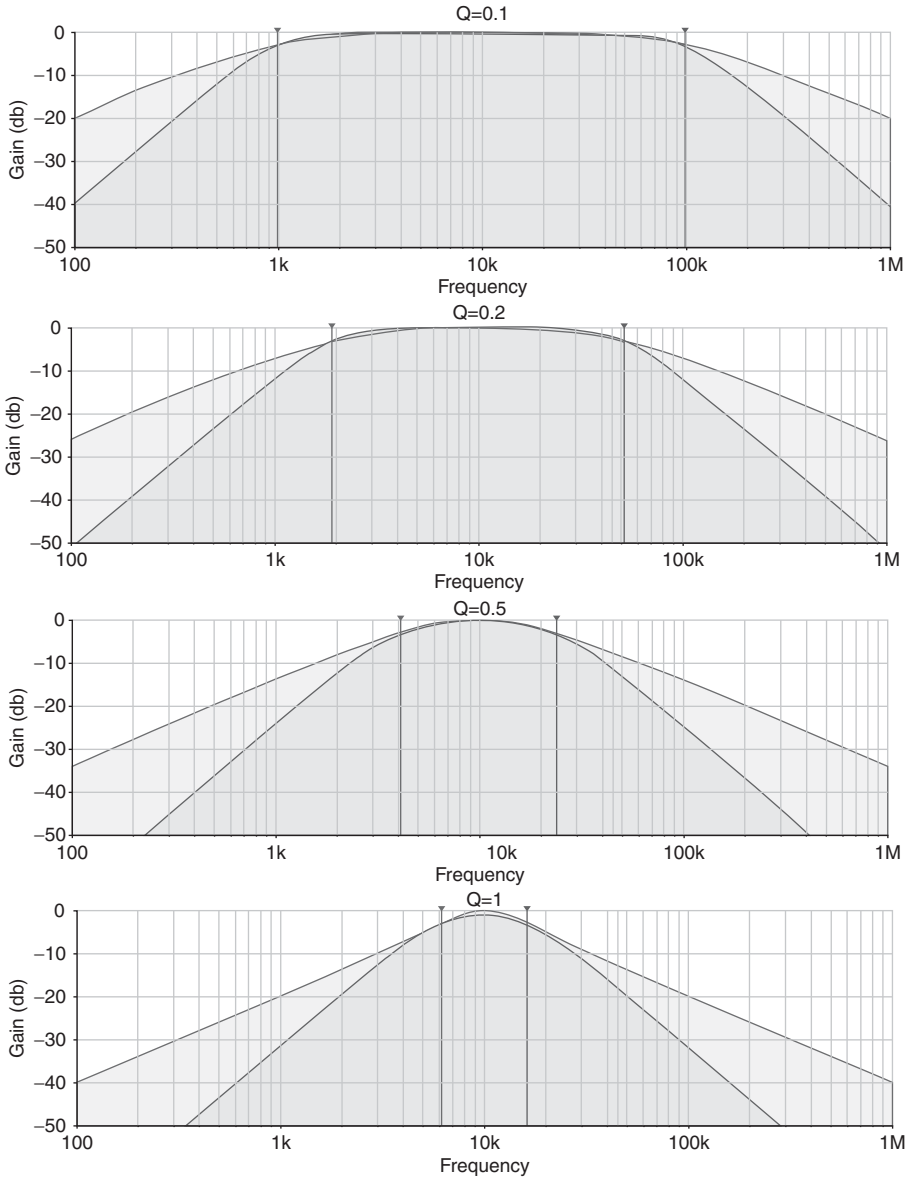


Figure 21.10: Narrow versus wide bandpass filter.

filter versus a wide bandpass? At high Q values, the single frequency bandpass is clearly the better choice. However, as Q values decrease, the difference begins to blur. What can be a very sharp peak at resonance erodes to a single pole roll-off on the low end and single pole roll-off on the high end. This results in a lot of unwanted energy in the stop bands.

Clearly, for Q values of 0.1 (and below) and 0.2, the best implementation is high pass cascaded with low pass. The lighter shaded regions correspond to a large amount of energy in the stop bands not rejected with a bandpass filter. In the wide passband, the cascaded approach is also clearly superior, because there is a wider region in the passband where response is flat.

The two implementations have almost an identical pass band response for a Q of 0.5. The designer is presented with a choice—use a bandpass filter (which can be implemented with a single op amp) to save money or use a cascaded approach that has better rejection in the stop bands.

As the Q becomes higher and higher, however, the responses of two separate stages begin to interact, destroying the amplitude of the signal. The designer at this point can still opt for the cascaded approach if stop band rejection is the primary concern and amplitude response is secondary. Amplitude response begins to degrade badly for even higher values of Q, however, ending the usefulness of the cascaded approach.

A good rule of thumb is that the starting and ending frequencies of the band should be at least five times different.

21.6 Wide Bandpass Filter

Figure 21.11 shows a wide bandpass filter.

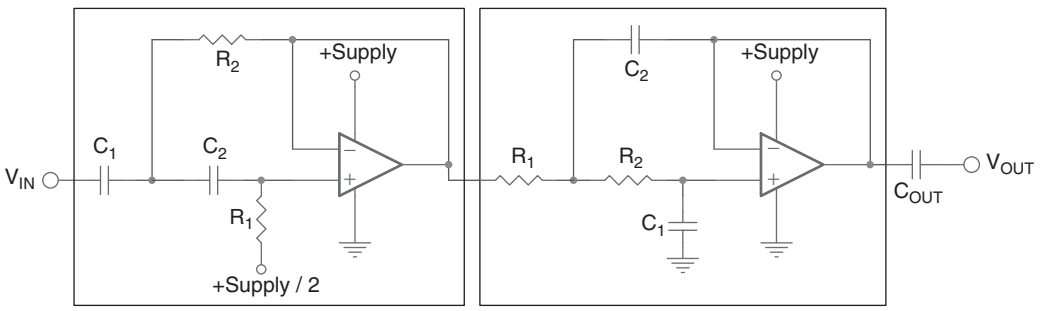


Figure 21.11: Wide bandpass filter.

The design procedure is as follows:

- Go to Section 21.3, and design a high pass filter for the low end of the band.
- Go to Section 21.2, and design a low pass filter for the high end of the band.
- Calculate $C_{IN} = C_{OUT} =$ 100 to 1000 times C_1 in the low pass filter section (not critical) = _____.

Done!

Digging deeper, we find this is nothing more than cascaded Sallen-Key high pass and low pass filters. The high pass comes first, so noise from it will be low passed.

21.7 Notch (Single Frequency Rejection) Filter

Figure 21.12 shows a notch (single frequency rejection) filter.

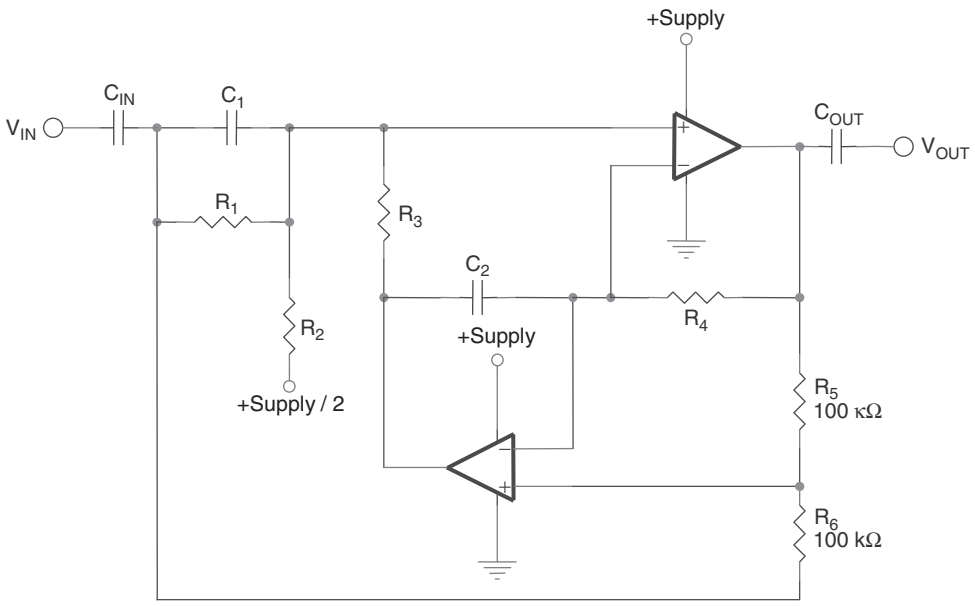


Figure 21.12: Notch filter.

The design procedure is as follows:

- Pick $C_1 = C_2 =$ _____
- Calculate $R_3 = R_4 = \dfrac{1}{2 \times \pi \times C_1 \times \text{Frequency}} =$ _____
- Calculate $R_1 = R_2 = 20 \times R_3$.
- Calculate $C_{IN} = C_{OUT} = 100$ to 1000 times C_1 (not critical): _____

Done!

Digging deeper, we find this is the Fliege filter topology, set to a Q value of 10. The Q can be adjusted independently from the center frequency by changing R_1 and R_2. Q is related to the center frequency set resistor by the following:

$$R_1 = R_2 = 2 \times Q \times R_3$$

The Fliege filter topology has a fixed gain of 1.

Many designers use the "twin T" notch topology for notches. While it is a popular topology, it has many problems. The biggest is that it is not producible. Many runs of simulation with component tolerances of 1% have shown tremendous variation in notch center frequency and notch depth. The only real advantage is that it can be implemented with a single op amp. Some additional stability can be obtained from the two op amp configuration, but if two op amps are used, then why not use a different topology, such as the Fliege? To successfully use the twin T topology, six precision components are required. The Fliege produces a deep null at some frequency, and it is easy to tune that frequency by adjusting one of the resonance resistors—the null will remain as deep over a fairly wide range. R_5 and R_6 are the only critical elements, they don't have to be 100 k, they can be scaled together, but they should be matched.

We dig even deeper. Just as was the case with the narrow bandpass filter versus the wide bandpass filter, a decision must be made about whether it is better to implement a notch filter or a band reject filter. Figure 21.13 shows the transition between the two types of filter.

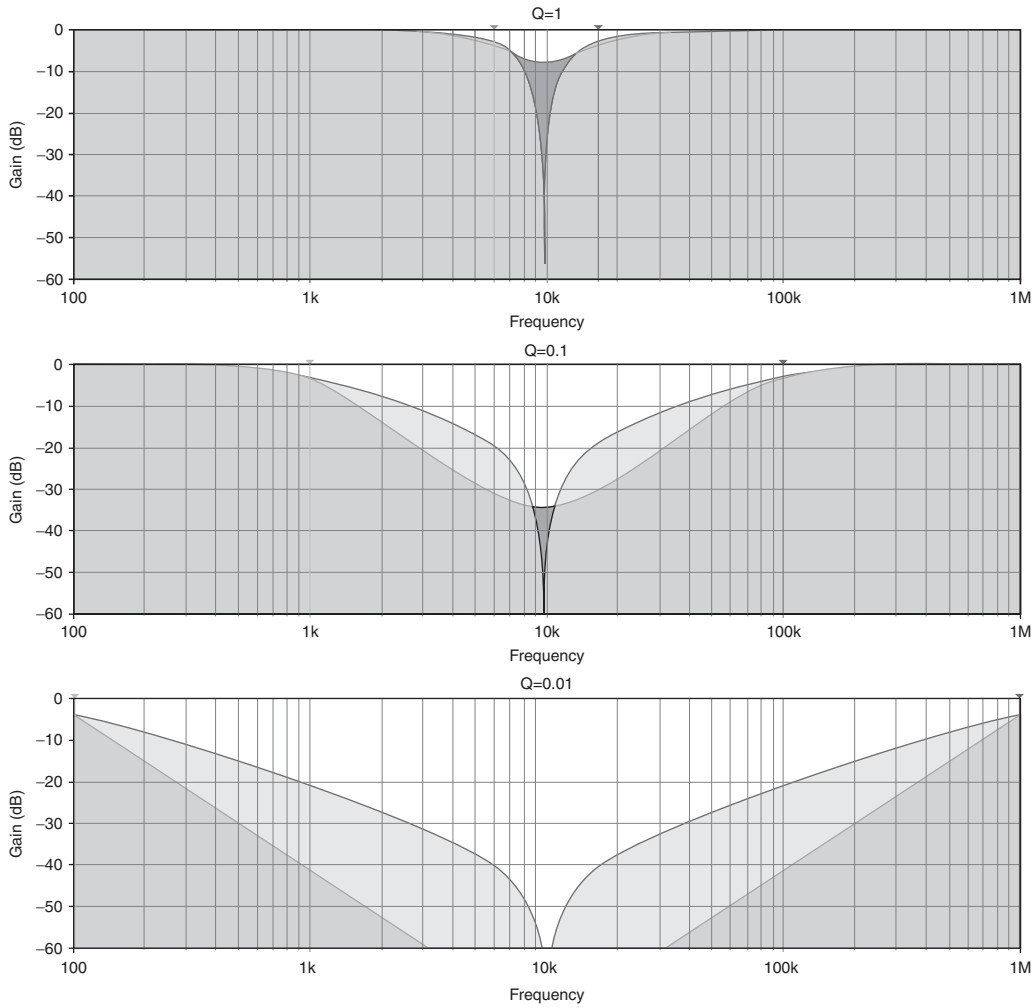


Figure 21.13: Notch filter versus wide band reject filter.

Even with Q as low as 1, it is clearly better to use a notch filter for a single frequency. But for lower Q values, more and more unwanted energy is passed by a notch filter than a band reject filter. A good rule of thumb for using a band reject filter is that the starting and ending frequencies of the band to be rejected should be at least 50 times different.

21.8 Band Reject Filter

Figure 21.14 shows a band reject filter.

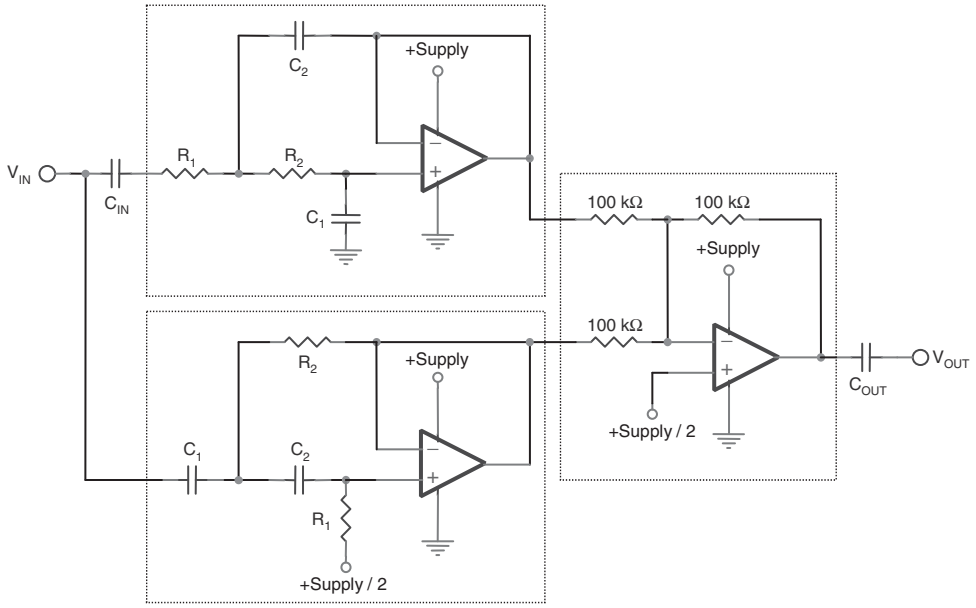


Figure 21.14: Band reject filter.

The design procedure is as follows:

- Go to Section 21.3, and design a high pass filter for the low end of the upper band.
- Go to Section 21.2, and design a low pass filter for the high end of the lower band.
- For the single supply case only, calculate $C_{IN} = C_{OUT} = 100$ to 1000 times C_1 in the low pass filter section (not critical): _____.

Done!

Digging deeper, we find this is nothing more than summed Sallen-Key high pass and low pass filters. They cannot be cascaded, because their responses do not overlap as in the wide bandpass filter case.

21.9 Summary of Filter Characteristics

Table 21.1 gives a summary of the various filter types and the cost of implementing them.

Table 21.1: Filter Characteristics

Desired function	Topology	Op amp	*C*	*R*	*Q*	Limitations
Low pass	Sallen-Key	1	2	2		Unity gain
	MFB	1	2	3		
High pass	Sallen-Key	1	2	2		Unity gain
	MFB	1	3	2		
Narrow bandpass	Deliyannis	1	2	3 to 6	0.5 to ∞	Gain and Q interact
Wide bandpass	Cascaded HP LP SK	2	4	4	<0.5	Unity gain
	Cascaded HP LP MFB	2	5	5	<0.5	
Notch	Fliege	2	2	4	0.05 to ∞	Unity gain
Band reject	Summed HP LP SK	3	4	6	<0.5	Unity gain
	Summed HP LP MFB	3	5	8	<0.5	

CHAPTER 22

High Speed Filter Design

22.1 Introduction

Designing of high speed filters, as opposed to designing filters fast (as presented in the last chapter), represents the final frontier of active filter design. As filter operating frequencies approach higher and higher frequencies, their response begins to change in unpredictable ways, presenting the designer with an increasingly difficult design problem. Many of these effects are related to the slew rate limitation of the amplifier and begin to manifest themselves decades in frequency below the unity gain bandwidth. A 1 GHz amplifier may be limited to a few hundred kilohertz when used in a filter design. This chapter presents these limitations and shows actual examples of how successful high speed filter designs can be implemented.

22.2 High Speed, Low Pass Filters

Believe it or not, achieving low pass filter response at high speeds is very easy. All the designer has to do is to find an op amp with the correct unity gain bandwidth (or bandwidth at the gain desired). Then, the designer has to close the loop—the compensation internal to the op amp does the rest! In fact, multiple poles inside the op amp may make multiple pole, low pass filters unnecessary. A single op amp may suffice for two or more poles of low pass response.

22.3 High Speed, High Pass Filters

At high speeds, all potential high pass filter topologies are ultimately limited by the bandwidth of the op amp. Therefore, the very best scenario for a high pass filter is that

it will become some kind of high pass, followed by a low pass, in other words, a wide bandpass filter. This is not to say there will be no applications where a –3 dB point for a high pass filter won't reject unwanted low frequency components, but the designer must be cognizant that, as the cutoff frequency of a high pass filter increases, it also approaches the bandwidth limitation of the op amp. Therefore, this chapter does not cover high speed, high pass filters in any great detail.

22.4 High Speed Bandpass Filters

At high speeds, all potential high pass filter topologies are ultimately limited by the bandwidth of the op amp. Obviously, limiting the number of op amps yields the highest frequency bandpass, as only one op amp limits the bandwidth. There are several single op amp bandpass filter topologies, but the most producible is a modified version of the MFB topology, also a variation of the Deliyannis. When one looks at the Deliyannis and MFB schematics side by side, in Figure 22.1, it is evident that they differ by only one resistor R_3.

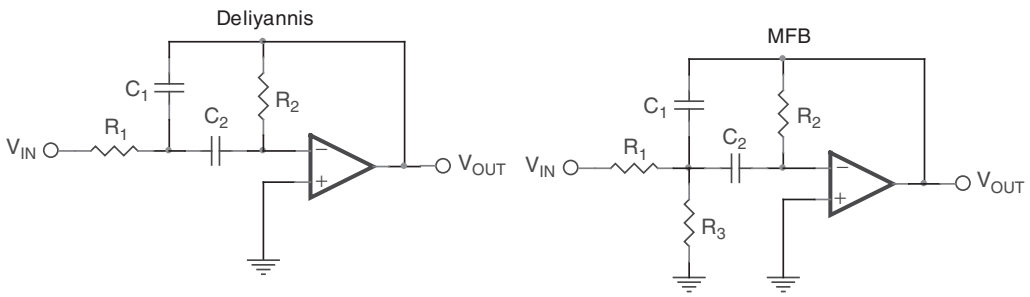


Figure 22.1: Deliyannis and MFB topologies.

As is often the case in filter design, an increase in the number of components increases design flexibility. For the Deliyannis bandpass filter, if $R_1 = R_2 = R_O$ and $C_1 = C_2 = C_O$, the center frequency is given by

$$f_O = \frac{1}{2\pi \times R_O \times C_O}$$

Gain is –6.02 dB and Q is 0.5

However, this is only one case. As the Q of the Deliyannis filter is increased, the gain increases in an almost unbounded fashion. The designer using the Deliyannis filter has the correct value of Q but excessive gain, which also limits the usable bandwidth of the op amp. For relatively low values of Q, the Deliyannis is acceptable, but it is possible to do better.

22.4.1 Modifying the Deliyannis Topology

Consider again the special case of the Deliyannis where $R_1 = R_2 = R_O$ and $C_1 = C_2 = C_O$. Modifying the Deliyannis filter by the addition of R_3 has a curious effect. Designers used to voltage dividers are drawn visually to a voltage divider formed by R_1 and R_3, and assume that the gain is reduced by a factor of 2. Curiously, this is not the case. If $R_1 = R_2 = R_3 = R_O$, and $C_1 = C_2 = C_O$, the gain is unchanged: It is still –6.02 dB. The center frequency, however, has become

$$f_O = \frac{1}{\sqrt{2}\pi \times R_O \times C_O}$$

The bandwidth of the filter also remains unchanged; however the change in f_O has affected the Q:

$$Q = \frac{1}{\sqrt{2}}$$

Clearly, jumping to conclusions is not advisable. Doubling the value of R_2 in the circuit, however, makes both the gain and Q equal to 1 and the center frequency again becomes

$$f_O = \frac{1}{2\pi \times R_O \times C_O}$$

Redrawing the MFB portion of Figure 22.1 to resemble a modified Deliyannis filter gives us Figure 22.2.

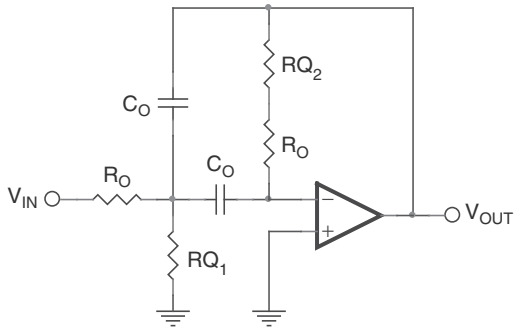


Figure 22.2: MFB topology redrawn as modified Deliyannis filter.

If all four resistors are made equal, center frequency, Q, and gain are unchanged from the previous example. The nice thing about this particular implementation is that center frequency f_O can be adjusted independently of gain and Q by controlling the values of R_O and C_O. Gain and Q, however, are linked by the relationship

$$\frac{R_O + RQ_2}{2 \times R_O} = \text{Gain} = Q$$

where

$$n \times RQ_1 = R_O = \frac{1}{n} \times RQ_2$$

If RQ_2 is doubled, RQ_1 must be halved and vice versa. If one is tripled, the other must be one third, and so on. RQ_2 and RQ_1 must always be related in this way. Otherwise, the center frequency is changed—and analysis of this circuit must be done with traditional MFB transfer equations.

The linking of gain and Q is not a huge disadvantage for narrow bandpass filters, as the objective is usually to detect a tone, and gain is usually desirable or at least not a tight requirement. The designer must be careful only to not drive the op amp outputs beyond the voltage rails for the maximum expected input signal level. If the tone being detected has a large dynamic range and high sensitivity is needed, that would also lead to voltage levels beyond the rails of the op amp in close proximity to the source of the tone—output limiting op amps such as the OPA688 and OPA689 should be used.

Simulating this circuit yields the family of curves for increasing gain and Q in Figure 22.3. A couple of things are apparent in the figure.

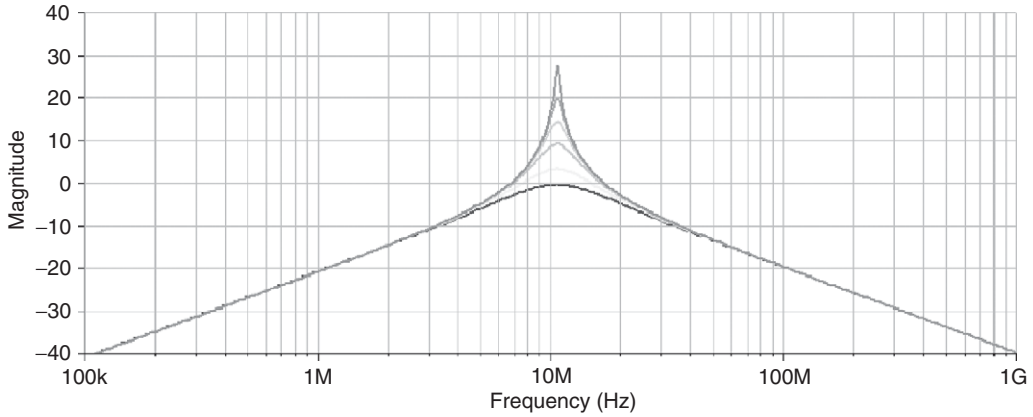


Figure 22.3: Effect of varying RQ_1 and RQ_2.

- As in all single stage bandpass filters, the ultimate roll-off slope in the stop bands is –20 dB/decade. The best way for the designer to think of this is that single stage (two pole) bandpass filters provide one pole low pass and one pole high pass filtering. Where the bandpass filter response reduces to this slope is entirely dependent on the Q value.
- The response of this filter at 100 kHz, 1 MHz, 100 MHz, and 1 GHz is (almost) unchanged for values of Q between 1 and infinity. The filter response at 10 MHz, however, goes to whatever amplitude it takes to achieve the Q value required of the circuit.

These are the response characteristics inherent in the circuit of Figure 22.2. If more control is required over gain, it can be adjusted down by the addition of a voltage divider on the input. This voltage divider, of course, modifies one of the R_O resistors, so the design process can get tedious. But it does give some measure of independent control over the center frequency, Q, and gain of the bandpass circuit.

22.4.2 Modified Deliyannis versus MFB

A designer might be asking at this point, "Why not just use the MFB bandpass topology as a more general solution!" This is a very reasonable question and is not trivialized

here. The answer again lies in component sensitivities and past experience with MFB bandpass filters. When a general solution for an MFB filter was used to design a bandpass filter, the resulting Monte Carlo analysis again shows tremendous variation in gain, as shown in Figure 22.4.

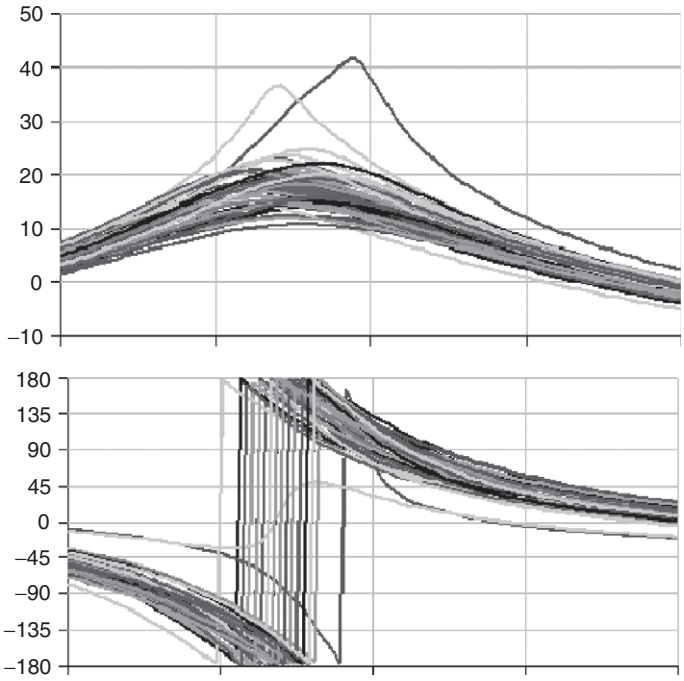


Figure 22.4: Monte Carlo analysis of an MFB filter.

This filter was supposed to have 17 dB of gain, yet the result of 50 runs, using 1% resistors and 2% capacitors, showed a gain variation of more than 30 dB (from 12 dB to 42 dB). Further, hidden somewhere in the amplitude response is a case where the filter does not even have a bandpass characteristic. The evidence of this is on the phase plot, where the phase of one run went exactly opposite in phase to the rest.

It is evident that, in high production volumes, the MFB approach is simply not manufacturable. Even with 2% capacitors—two amplitude plots and one phase plot showed unacceptable variation—3 runs out of 50 is a 6% failure rate.

The modified Deliyannis approach described previously gave the Monte Carlo analysis shown in Figure 22.5.

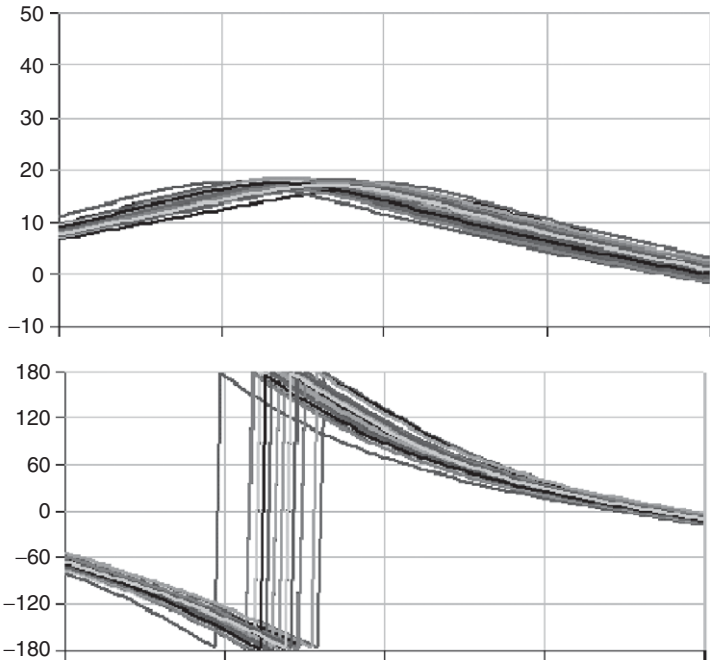


Figure 22.5: Monte Carlo analysis of a modified Deliyannis filter.

When the two analyses are compared, the modified Deliyannis approach is far superior. It produces component values that are not as sensitive to variation as those that can be obtained from the general MFB approach.

22.4.3 Lab Results

A modified THS4271 EVM was tested at a standard bandpass frequency of 10.7 MHz to see what levels of Q could realistically be implemented. The schematic is shown in Figure 22.6.

The values of RQ were varied in to change the Q without affecting the center frequency. A 1% resistor sequence made it very easy to change resistors in a 1–2–5 sequence (rather than aiming for specific values of Q).

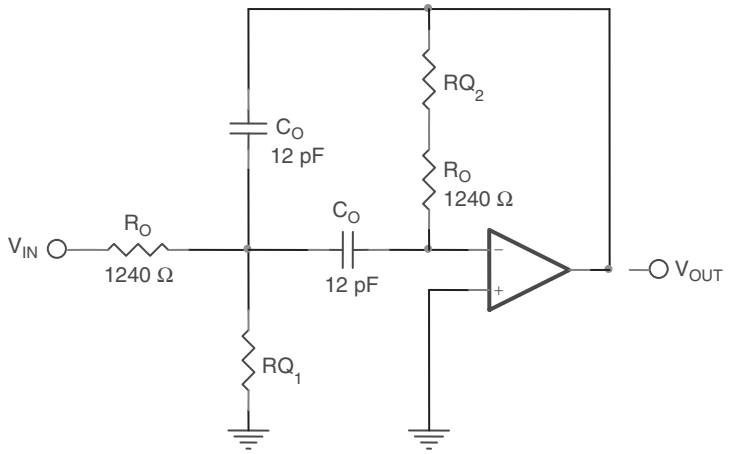


Figure 22.6: 10.7 MHz bandpass filter.

The values of RQ_1 and RQ_2 in Table 22.1 were used in the bandpass filter of Figure 22.6. The resulting responses are shown on the right hand set of curves in Figure 22.7.

Table 22.1: RQ_1 and RQ_2 Values

RQ_1	RQ_2	Resulting Q	Resulting gain (dB)
1240 Ω	1240 Ω	1	0
619 Ω	2490 Ω	1.5	5.28
249 Ω	6190 Ω	3	9.54
124 Ω	12.4 kΩ	5.5	14.8
61.9 Ω	24.9 kΩ	10.5	20.4
24.9 Ω	61.9 kΩ	25.5	28.1
12.4 Ω	124 kΩ	50.5	34.1

Clearly, the results show some type of problem with higher Q bandpass filters at 10.7 MHz. The center frequency shifts to the left, while the amplitude decreases. No attempt was even made to do a plot at a Q of 50.5—the plot at a Q of 25.5 was degraded so badly that the trend was clear.

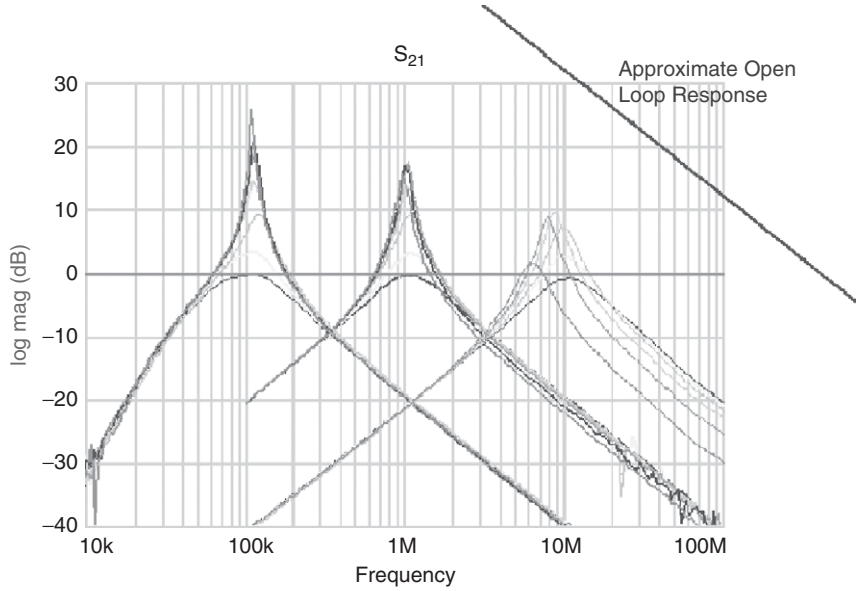


Figure 22.7: Bandpass filter lab results.

The open loop response of the op amp, when superimposed on the preceding data, shows that the 10.7 MHz bandpass filters come within 30 dB of the open loop plot. There is a "truism" when working with op amps that one should have at least 40 dB of headroom above the center frequency before encountering the open loop characteristic. Nowhere is that demonstrated more dramatically than here. At a gain and Q of 1, a bandpass filter at 10.7 MHz is about 33 dB away from the open loop characteristic of the THS4271. The bandpass filter works almost correctly; the slightly low amplitude probably has more to do with real world resistor values than any sort of bandwidth limitation. But, at higher values of Q and gain, the amplitude could never rise to 10 dB. In fact, the center frequency is shifted lower as the circuit tries to compensate for the open loop response limitation.

It is very easy to scale the center frequency of the filter down by a factor of 10 and 100 to change the two C_O capacitors to 120 pF and 1.2 nF, respectively. This created filters centered at 1.07 MHz and 107 kHz. The results are also shown on Figure 22.7:

- Clearly, the filters centered at 1.07 MHz suffer far less from degradation at higher Q values than those at 10.7 MHz. Very little frequency shift was observed. There is, however, a limit on the amplitude to just below 20 dB, which is about 30 dB from where the open loop curve crosses 1 MHz.

- The filters centered at 107 kHz create a set of curves reminiscent of Figure 22.3, yet there is a slight degradation of amplitude at higher values of Q. Amplitude on the highest peaks is limited to about 28 dB, which is 42 dB below the open loop response at 1 MHz.

Clearly, the 40 dB headroom rule is well advised. Operating a bandpass circuit too close to the open loop response degrades first the gain and Q and finally affects the center frequency.

22.5 High Speed Notch Filter

Ordinarily, the lowest possible number of op amps would be the best for a high speed filter, and that would lead a designer to a twin T notch. This chapter does not cover the twin T notch filter topology, because it is too hard to control center frequency and Q with real world components. Instead, the more producible Fliege notch topology is used and shown in Figure 22.8.

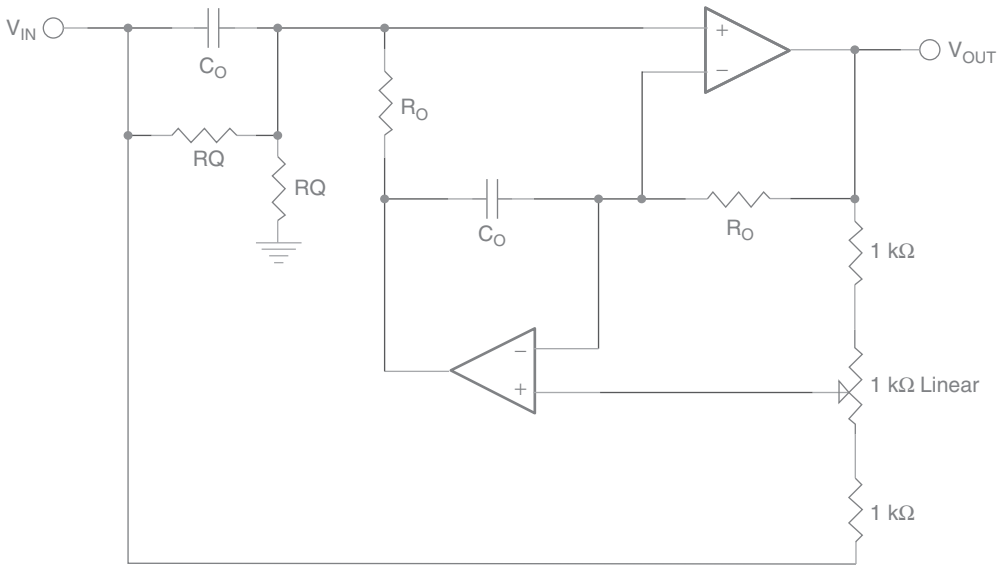


Figure 22.8: Fliege notch filter topology.

The advantages of this circuit over the twin T are

- Only four precision components (two R and two C) are required for tuning the center frequency. One nice feature of this circuit is that slight mismatches of components are OK—the center frequency is affected but not the notch depth.
- The Q value of the filter can be adjusted independently from the center frequency by using two noncritical resistors of the same value.
- The center frequency of the filter can be adjusted over a narrow range without seriously eroding the depth of the notch.

22.5.1 Simulations

Simulations were first performed with ideal op amp models. Real op amp models were used later, which produced results similar to those observed in the lab. Table 22.2 shows the component values that were used for the schematic of Figure 22.8. There was no point in performing simulations at or above 10 MHz, because lab tests were actually done first and 1 MHz was the top frequency at which a notch filter worked.

Table 22.2: Component Values for the Notch Filter

	1 MHz			100 kHz			10 kHz		
Q	R_O	C_O	RQ	R_O	C_O	RQ	R_O	C_O	RQ
100	1.58 kΩ	100 pF	316 kΩ	1.58 kΩ	1 nF	316 kΩ	1.58 kΩ	10 nF	316 kΩ
10			31.6 kΩ			31.6 kΩ	15.8 kΩ	1 nF	316 kΩ
1			3.16 kΩ			3.16 kΩ			31.6 kΩ

A word about capacitors: although the capacitance is just a value for simulations, actual capacitors are constructed of different dielectric materials. For 10 kHz, resistor value spread constrained the capacitor to a value of 10 nF. While this worked perfectly well in simulation, it forced the author to change from an NPO dielectric to an X7R dielectric in the lab, with the result that the notch filter lost its characteristic completely. The 10 nF capacitors used measured close in value, so the loss of notch response was most likely due to poor dielectric. The circuit had to revert to the values for a Q of 10, and a 3 MΩ RQ was used. For real world circuits, it is best to stay with NPO capacitors.

These component values were used in both simulations and lab testing. Initially, the simulations were done without the 1 kΩ potentiometer (the two 1 kΩ fixed resistors were connected directly together and to the noninverting input of the bottom op amp). Simulation results are shown in Figure 22.9.

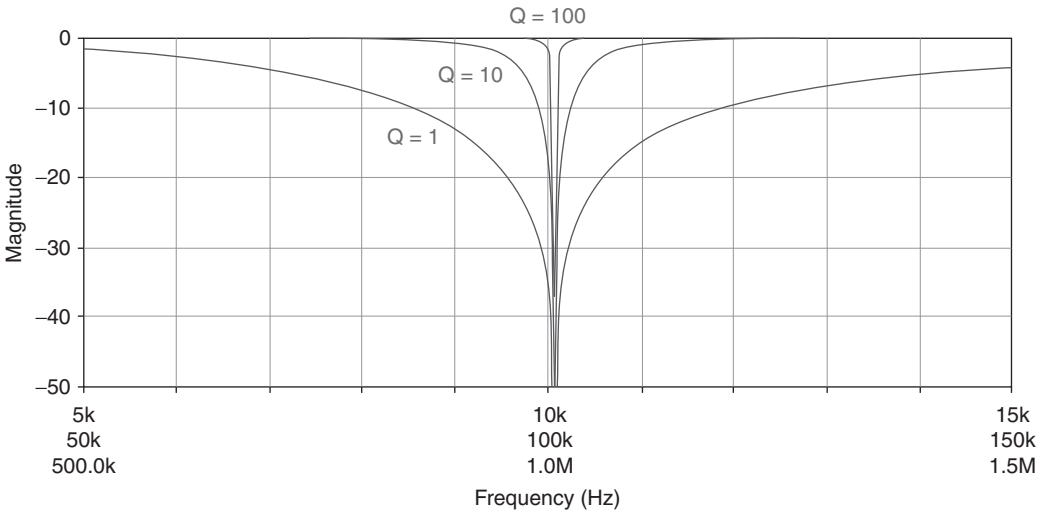


Figure 22.9: Simulation results before tuning.

There are actually nine sets of results in Figure 22.9, but the curves for each Q value overlay those at the other frequencies. The center frequency in each case is slightly above a design goal that would be right on 10 kHz, 100 kHz, or 1 MHz. This is as close as a designer can get with a standard E96 resistor and E12 capacitor. Consider the 100 kHz case:

$$f_O = \frac{1}{2\pi R_O C_O} = \frac{1}{2\pi \times 1.58\ \text{k}\Omega \times 1\ \text{nF}} = 100{,}731\ \text{Hz}$$

A closer combination exists if E24 sequence capacitors are available:

$$f_O = \frac{1}{2\pi R_O C_O} = \frac{1}{2\pi \times 4.42\ \text{k}\Omega \times 360\ \text{pF}} = 100{,}022\ \text{Hz}$$

The inclusion of E24 sequence capacitors can lead to more accurate center frequencies in many cases, but procuring the E24 sequence values is considered an expensive (and unwarranted) expenditure in many labs. While it may be easy to specify

E24 capacitor values in theory, in practice many of them are seldom used and have long lead times associated with them.

There are easier alternatives to selecting E24 capacitor values. Close examination of Figure 22.9 shows that the notch "misses" the center frequency by only a small amount. At lower Q values, there is still substantial rejection of the desired frequency. If the rejection is not sufficient, then it becomes necessary to tune the notch filter.

Again considering the 100 kHz case, the response near 100 kHz is spread out on Figure 22.10. The 1 kΩ potentiometer is inserted and adjusted up and down in 1% steps.

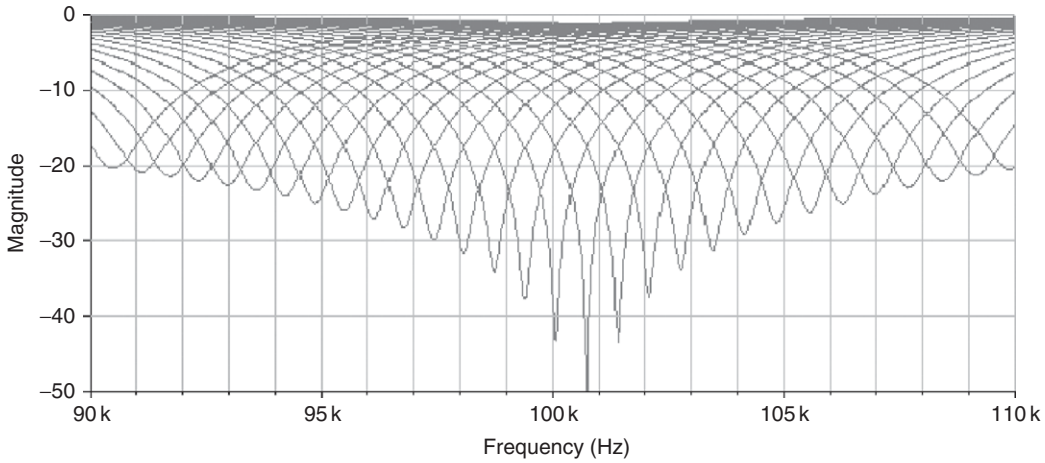


Figure 22.10: Tuning for center frequency.

The family of curves to the left and right of the center frequency (100,731 Hz) represents the filter response when the potentiometer is adjusted in 1% increments. When the potentiometer is exactly in the middle, the notch filter rejects frequencies at the exact center frequency. The depth of the simulated notch is actually on the order of 95 dB, but that is not going to happen in the real world. A 1% adjustment of the potentiometer puts a notch that is greater than 40 dB right on the desired frequency. Again, this is best case with ideal components, but lab results are close at low frequencies (10 kHz and 100 kHz).

Figure 22.10 shows that it is important to get close to the correct frequency, starting with R_O and C_O. While the potentiometer can correct for frequency over a broad range, the depth of the notch degrades. Over a small range (±1%), it is possible to get a 100:1 rejection of the undesirable frequency. But over a larger range (±10%), it is possible to get only a 10:1 rejection.

22.5.2 Lab Results

A THS4032 evaluation board was used to construct the circuit of Figure 22.8. Its general purpose layout required only three jumpers and one trace cut to complete the circuit. The components of Table 22.2 were used, starting with the components that would produce 1 MHz. It was the intention to look for bandwidth and slew rate restrictions at 1 MHz and test at lower or higher frequencies as necessary.

22.5.3 1 MHz Results

Figure 22.11 shows that there are some very definite bandwidth or slew rate effects at 1 MHz. The response at a Q of 100 shows barely a ripple on the response curve where the notch should be. At a Q of 10, there is only a 10 dB notch, and a 30 dB notch at a Q of 1. Apparently, notch filters cannot achieve as high a frequency as hoped. But the THS4032 is only a 100 MHz device; it is reasonable to expect better performance from parts with a greater unity gain bandwidth. Unity gain stability is important, because the Fliege topology has fixed unity gain.

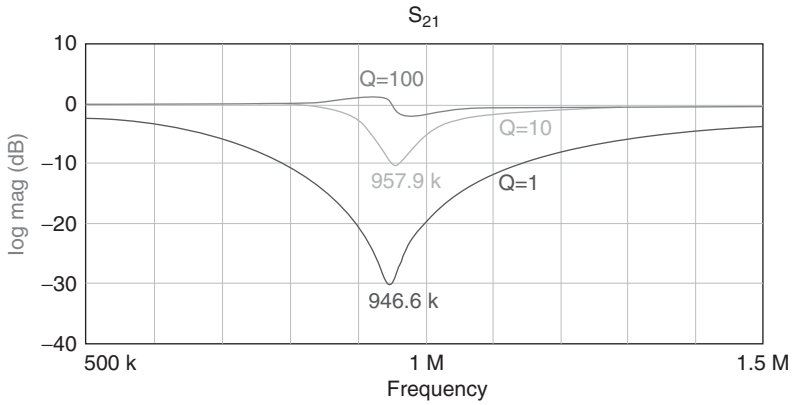


Figure 22.11: 1 MHz lab results.

If the designer wishes to estimate what bandwidth is required for a notch at a given frequency, a good place to start is the published gain and bandwidth product, which should be 100 times the center frequency of the notch. Additional bandwidth is required for higher Q values. There is a slight frequency shift of the notch center frequency as Q is changed. This is similar to the frequency shift seen for bandpass filters. The frequency shift is less for notch filters centered at 100 kHz (Figure 22.12) and 10 kHz (Figure 22.13).

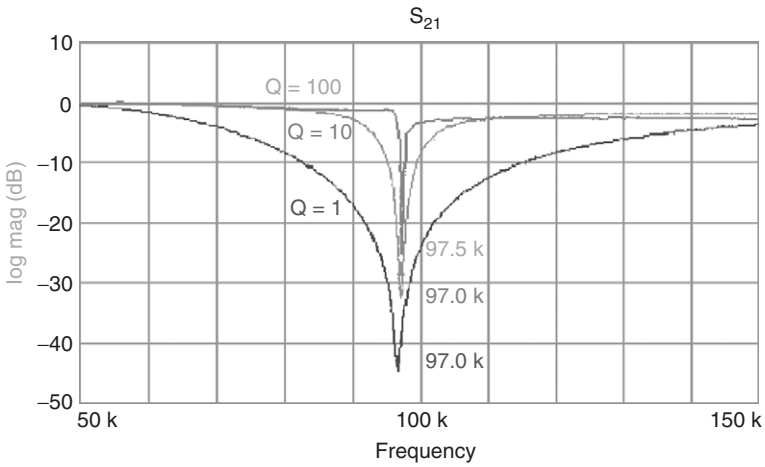


Figure 22.12: 100 kHz lab results.

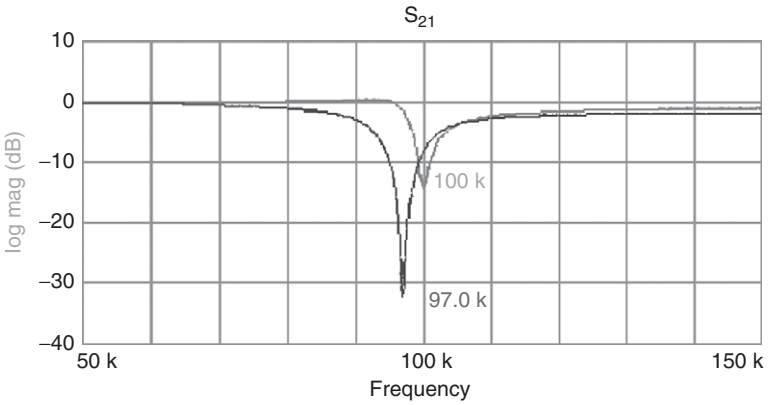


Figure 22.13: Tuning for exact center frequency.

22.5.4 100 kHz Results

Component values from Table 22.2 were then used to create 100 kHz notch filters with different Q values. The results are shown in Figure 22.12. It is immediately obvious that viable notch filters can be constructed with center frequency of 100 kHz, although the notch depth appears to be less at higher values of Q.

Remember, though, that the design goal in this section is a 100 kHz notch, not a 97 kHz notch. The component values selected are the same as the simulation, so the notch center frequency should theoretically be at 100,731 Hz, but the difference is explained by the parts in the lab. The mean value of the 1000 pF capacitor stock was 1030 pF and that of the 1.58 kΩ resistor stock was 1.583 kΩ. When the center frequency is calculated with these values, it comes out to 97.14 kHz. The actual components, however, could not be measured (the board was too fragile).

As long as the capacitors are matched, it would be possible to go up a couple of standard E96 resistor values to get closer to 100 kHz. Of course, this is probably not an option in high volume manufacturing, where 10% capacitors could come from any batch and potentially from different manufacturers. The range of center frequencies is determined by the tolerances of R_O and C_O, which is not good news if a high Q notch is required. There are three ways of handling this:

- Purchase higher precision resistors and capacitors.
- Lower the Q requirement and live with less rejection of the unwanted frequency.
- Tune the circuit (which is explored next).

At this point, the circuit was modified to have a Q of 10, and a 1 kΩ potentiometer was added for tuning the center frequency (as shown in Figure 22.8). In real world design, the value of the potentiometer should be selected to slightly more than cover the range of center frequencies possible with worst case R_O and C_O tolerances. That was not done here, as this was an exercise in determining possibilities; and 1 kΩ was the lowest potentiometer value available in the lab.

When the circuit was tuned for a center frequency of 100 kHz, as shown in Figure 22.13, the notch depth degraded from 32 dB to 14 dB. Remember that this notch depth could be greatly improved by making the initial f_O closer to ideal. The potentiometer is meant to tune over only a small range of center frequencies. Still, a 5:1 rejection of an unwanted frequency is respectable and may be sufficient for some applications. More critical applications will obviously need higher precision components.

It may also be true that bandwidth limitations from the op amp are keeping the notch depth from being as low as possible, which also degrades the tuned notch depth. With this in mind, the circuit was retuned for a center frequency of 10 kHz.

22.5.5 10 kHz Results

Figure 22.14 shows that the notch depth for a Q of 10 increased to 32 dB, which is about what one would expect from a center frequency 4% off from simulation (Figure 22.9). The op amp was indeed limiting the notch depth at a center frequency of 100 kHz! The 32 dB is a rejection of 40:1, which is quite good.

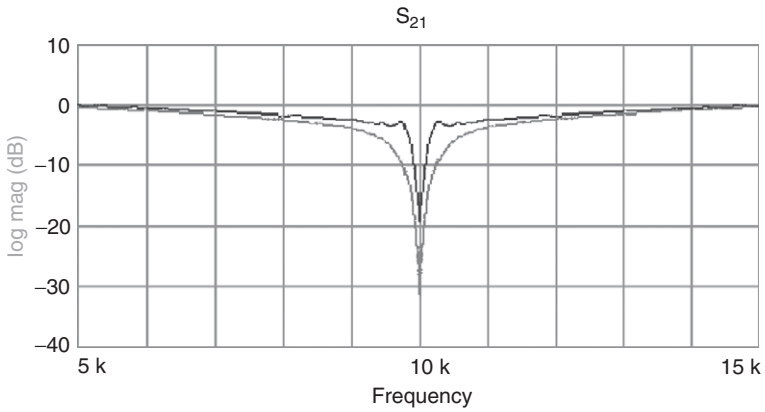


Figure 22.14: 10 kHz lab results.

So, even with components that produced an initial 4% error, it is possible to produce a 32 dB notch at the desired center frequency. The bad news is that, to escape op amp bandwidth limitations, the highest notch frequency possible with a 100 MHz op amp is somewhere between 10 kHz and 100 kHz. So in the case of notch filters, *high speed* is defined as being somewhere in the tens or hundreds of kilohertz.

Note: Some artistic liberties were taken on this plot. The laboratory instrument displays only down to 10 kHz, so the left hand portion of the plot is a mirror image of the right hand portion. Also, the laboratory instrument has some roll-off at frequencies below 100 kHz, which were artistically eliminated from this plot.

A good application for 10 kHz notch filters is AM (medium wave) receivers, where the carrier from adjacent stations produces a loud 10 kHz whine in the audio, particularly at night. This is a real earful and can really grate on one's nerves when listening for a prolonged time. Figure 22.15 shows the received audio spectrum of a station before and after the 10 kHz notch was applied. In this case, the 10 kHz carrier interference is

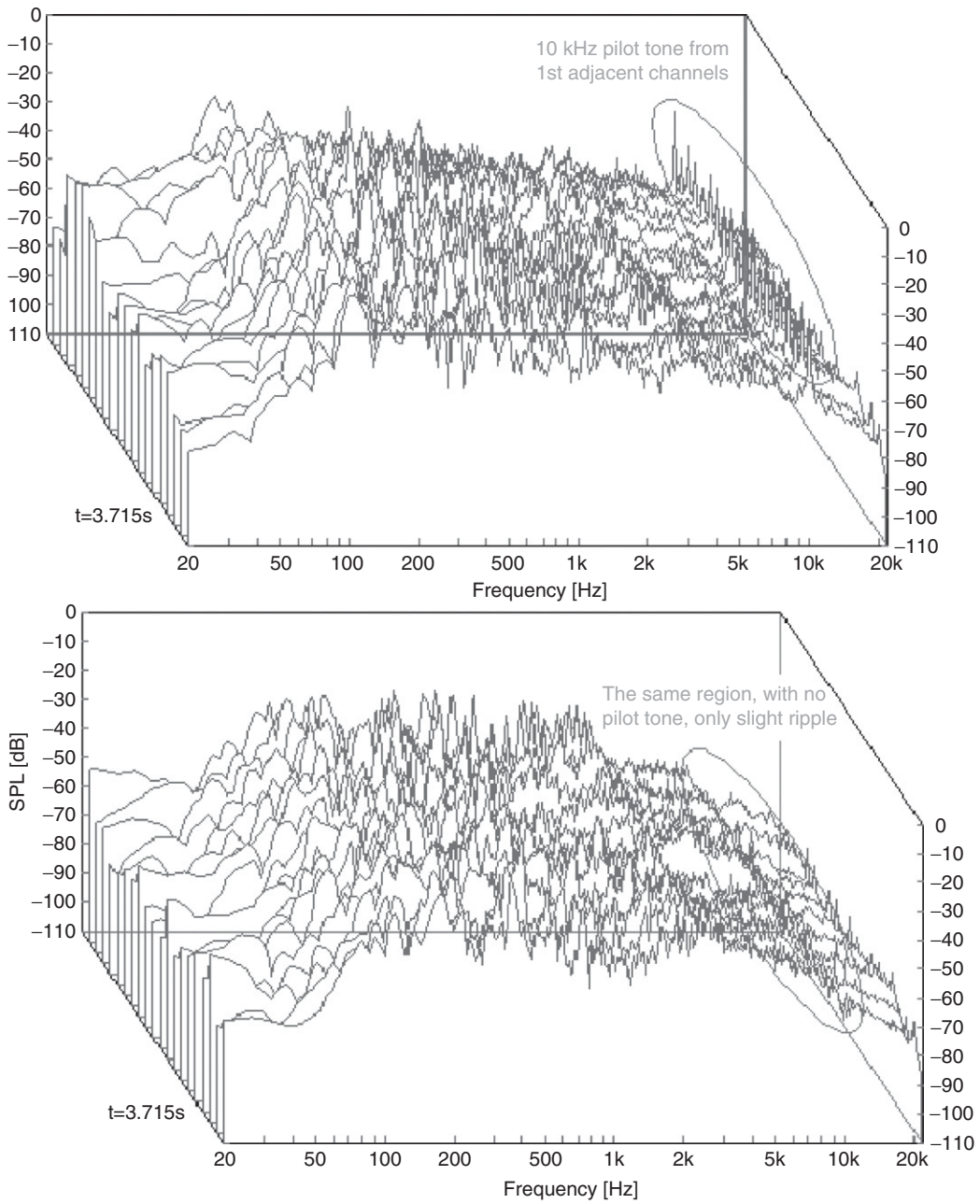


Figure 22.15: Effect of heterodyning and the notch filter.

shown as a string of peaks that vary in amplitude. When the notch is applied, the 10 kHz peaks are eliminated, and there is only a slight ripple in the received audio where 10 kHz has been notched out.

For European readers who want to have a more pleasing medium wave listening experience, the component values are these:

$$C_O = 330 \text{ pF}, \; R_O = 53.6 \text{ k}\Omega, \text{ and } RQ = 1 \text{ M}\Omega$$

Shortwave listeners benefit from a two stage notch filter, one section being the 10 kHz described previously and the other stage being a 5 kHz notch filter with these component values:

$$C_O = 270 \text{ pF}, \; R_O = 118 \text{ k}\Omega, \text{ and } RQ = 2 \text{ M}\Omega$$

22.6 Conclusions

High speed op amps have been used to produce low pass and high pass filters up to the tens of megahertz with fairly good success. Narrow bandpass filters and notch filters are much less understood and much more critical applications. While the tolerance of a capacitor might change the cutoff frequency of a low pass filter or produce ripple in the passband, that same tolerance can produce dramatic changes in center frequency and Q of bandpass and notch filters.

CHAPTER 23

Circuit Board Layout Techniques

Bruce Carter

23.1 General Considerations

Prior discussions focused on how to design op amp circuitry, how to use ICs, and the use of associated passive components. One additional circuit component must be considered for the design to be a success—the printed circuit board (PCB) on which the circuit is to be located.

23.1.1 The PCB Is a Component of the Op Amp Design

Op amp circuitry is analog circuitry and very different from digital circuitry. It must be partitioned in its own section of the board, using special layout techniques.

Printed circuit board effects become most apparent in high speed analog circuits, but common mistakes described in this chapter can even affect the performance of audio circuits. The purpose of this chapter is to discuss some of the more common mistakes made by designers and how they degrade performance and to provide simple fixes to avoid the problems.

In all but very rare cases, the PCB layout for analog circuitry must be designed such that the effect of the PCB is transparent to the circuit. Any effect caused by the PCB itself should be minimized so that the operation of the analog circuitry in production is the same as the performance of the design and prototype.

23.1.2 Prototype, Prototype, Prototype!

Normal design cycles, particularly of large digital boards, dictate laying out of the PCB as soon as possible. The digital circuitry has been simulated, but in most cases, the production PCB itself is the prototype and may even be sold to a customer. Digital designers can correct small mistakes by implementing *cuts and jumpers*, reprogramming gate arrays or flash memories, and going on to the next project. This is not the case with analog circuitry. Some of the common design mistakes discussed in this chapter cannot be corrected by the cut and jumper method. They render the entire PCB unusable. It is very important for the digital designer, who is used to cuts and jumpers, to read and understand this chapter prior to releasing a board to a layout service.

A little care, taken up front, can save a board worth thousands of dollars from becoming scrap because of blunders in a tiny section of analog circuitry. This author has been the unfortunate recipient of a simple analog circuit designed by another engineer, who was accustomed to the cut and jumper method of correcting his mistakes. This resulted in a design that was full of mistakes. Not only was the op amp hooked up with inverting and noninverting inputs reversed, but an RC time constant had to be added to prevent a race condition. Repercussions from these mistakes and associated rework problems actually caused hundreds of hours to be lost from a tight production schedule. Prototyping this circuit would have taken less than a day. *Prototype all analog circuitry!*

23.1.3 Noise Sources

Noise is the primary limitation on analog circuitry performance. Internal op amp noise is covered in Chapter 12. Other types of noise include

- Conducted emissions, noise that the analog circuitry generates through its connections to other circuits. This is usually negligible in analog circuitry, unless it is high power, such as an audio amplifier that draws heavy currents from its power supply.
- Radiated emissions, noise that the analog circuitry generates or transmits through the air. This is also usually negligible in analog circuitry, unless it is high frequency, such as video.
- Conducted susceptibility, noise from external circuitry that is conducted into the analog circuit through its connections to other circuits. Analog circuitry must

be connected to the "outside world" by at least a ground connection, a power connection, an input, and an output. Noise can be conducted into the circuit through all of these paths, as well as any others present.

- Radiated susceptibility, noise that is received through the air (or transmitted into the analog circuitry) from external sources. Analog circuitry, in many cases, resides on a PCB that may have high speed digital logic, including DSP chips. High speed clocks and switching digital signals create considerable radio frequency interference (RFI). Other sources of radiated noise are endless: the switching power supply in a digital system, cellular telephones, broadcast radio and TV, fluorescent lighting, nearby PCs, lightning in thunderstorms, and so on. Even if the analog circuitry is primarily audio in frequency, RFI may produce noticeable noise in the output.

23.2 PCB Mechanical Construction

It is important to choose a PCB with the right mechanical characteristics for the application.

23.2.1 Materials: Choosing the Right One for the Application

Printed circuit board materials are available in various grades, as defined by the National Electrical Manufacturers Association (NEMA). It would be very convenient for designers if this organization were closely allied with the electronics industry, controlling parameters such as the resistivity and dielectric constant of the material. Unfortunately, that is not the case. NEMA is an electrical safety organization, and the different PCB grades primarily describe the flammability, high temperature stability, and moisture absorption of the board. Therefore, specifying a given NEMA grade does not guarantee electrical parameters of the material. If this becomes critical for an application, consult the manufacturer of the raw board stock.

Laminated materials are designated with FR (flame resistant) and G grades. FR–1 is the least flame resistant, and FR–5 is the most. G10 and G11 have special characteristics, as described in Table 23.1.

Do not use FR–1. There are many examples of boards with burned spots, where high wattage components heated a section of the board for a period of time. This grade of PCB material has more in common with cardboard than anything else.

Table 23.1: PCB Materials

Grade designation	Material/comments
FR–1	Paper/phenolic: room temperature punchable, poor moisture resistance
FR–2	Paper/phenolic: suitable for single sided PCB consumer equipment, good moisture resistance
FR–3	Paper/epoxy: designed for balance of good mechanical and electrical characteristics
FR–4	Glass cloth/epoxy: excellent mechanical and electrical properties
FR–5	Glass cloth/epoxy: high strength at elevated temperatures, self-extinguishing
G10	Glass cloth/epoxy: high insulation resistance, highest bond strength of glass laminates, high humidity resistance
G11	Glass cloth/epoxy: high flexural strength retention at high temperature, extreme resistance to solvents

FR–4 is commonly used in industrial quality equipment, while FR–2 is used in high volume consumer applications. These two board materials appear to be industry standards. Deviating from these standards can limit the number of raw board material suppliers and PCB houses that can fabricate the board because their tooling is already set up for these materials. Nevertheless, in some applications, one of the other grades may make sense. For very high frequency applications, it may be necessary to consider Teflon or even ceramic board substrate. One thing can be counted on, however: The more exotic the board substrate, the more expensive it is.

In selecting a board material, pay careful attention to the moisture absorption. Just about every desirable performance characteristic of the board is negatively affected by moisture. This includes surface resistance of the board, dielectric leakage, high voltage breakdown and arcing, and mechanical stability. Also, pay attention to the operating temperature. High operating temperatures can occur in unexpected places, such as in proximity to large digital ICs that switch at high speeds. Be aware that heat rises, so if one of those 500 pin monster ICs is located directly under a sensitive analog circuit, both the PCB and circuit characteristics may vary with the temperature.

After the board substrate material has been selected, the next decision is how thick to make the copper foil laminate. For most applications, 1 oz copper is sufficient. If the

circuit consumes a lot of power, 2 oz may be better. Avoid ½ oz copper, because it tends to break between the trace and the pad.

23.2.2 How Many Layers Are Best?

Depending on the complexity of the overall circuitry being designed, a designer must decide how many layers to make the PCB.

Single Sided

Very simple consumer electronics are sometimes fabricated on single sided PCBs, keeping the raw board material inexpensive (FR–1 or FR–2) with thin copper cladding. These designs frequently include many jumper wires, simulating the circuit routing on a double sided board. This technique is recommended only for low frequency circuitry. For reasons described later, this type of design is extremely susceptible to radiated noise. It is harder to design a board of this type because of the many things that can go wrong. Many complex designs have been successfully implemented with this technique, but they require a lot of forethought. An example is a television set that puts all the analog circuitry on a single sided board at the bottom of the case and uses the metallized CRT itself to shield the board from a separate digital tuning board near the top of the set. Be prepared to get creative if the design demands high volume, low cost PCBs.

If a single sided PCB is a requirement, remember the trace resistance! The op amp is not a three terminal device (inverting input, noninverting input, and output). It is a seven terminal device, as shown in Figure 23.1.

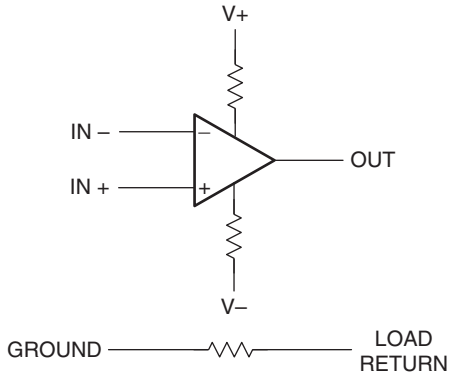


Figure 23.1: Op amp terminal model.

Resistance in the power leads of the device must be taken into account, as well as resistance between the return for the inputs and the load. Both the input and load must return somewhere. If these are at different potentials due to trace resistance, there can be problems.

Double Sided

The next level of complexity is double sided. Although there are some double sided FR–2 boards, they are more commonly fabricated with FR–4 material. The increased strength of FR–4 material supports vias better. Doubled sided boards are easier to route, because there are two layers of foil; and it is possible to route signals by crossing traces on different layers. Crossing traces, however, is not recommended for analog circuitry. Wherever possible, the bottom layer should be devoted to a ground plane and all other signals routed on the top layer. A ground plane provides several benefits:

- Ground is frequently the most common connection in the circuit. Having it continuous on the bottom layer usually makes the most sense for circuit routing.
- It increases mechanical strength of the board.
- It lowers the impedance of all ground connections in the circuit, which reduces undesirable conducted noise.
- It adds a distributed capacitance to every net in the circuit, helping to suppress radiated noise.
- It acts as a shield to radiated noise coming from underneath the board.

Multilayer

Double sided boards, in spite of their benefits, are not the best method of construction, especially for sensitive or high speed designs. The most common board thickness is 1.5 mm. This separation is too great for full realization of some of the benefits listed previously. Distributed capacitance, for example, is very low due to the separation.

Critical designs call for multilayer boards. Some of the reasons are obvious:

- Better routing for power as well as ground connections. If the power is also on a plane, it is available to all points in the circuit simply by adding vias.

- Other layers are available for signal routing, making routing easier.
- Capacitance is distributed between the power and ground planes, reducing high frequency noise.

Other reasons for multilayer boards, however, may not be obvious or intuitive:

- Better EMI/RFI rejection due to the *image plane effect*, which has been known since the time of Marconi. When a conductor is placed close to a parallel conductive surface, most of the high frequency currents return directly under the conductor, flowing in the opposite direction. This mirror image of the conductor within the plane creates a transmission line. Since currents are equal and opposite in the transmission line, it is relatively immune to radiated noise. It also couples the signal very efficiently. The image plane effect works equally well with ground and power planes, but they must be continuous. Any gap or discontinuity causes the beneficial effects to quickly vanish. More discussion on this follows.
- Reduced overall project cost for small production runs. Although multilayer boards are more expensive to manufacture, EMI/RFI requirements from the FCC or other agencies may require expensive testing of the design. Any problems can force a complete redesign of the PCB, leading to additional rounds of testing. A multilayer PCB can have as much as 20 dB better EMI/RFI performance over a two layer PCB. If production volumes are going to be small, it makes sense to make a better PCB to begin with than try to cut costs and take the risk of failing $25,000 to $50,000 tests.

23.2.3 Board Stack-Up: The Order of Layers

There has been a lot of confusion in the past over the optimum order for PCB layers. Take, for example, a four layer board consisting of two signal layers, a power plane, and a ground plane. Is it better to route the signal traces between the layers, thus providing shielding for the signal traces, or to make the ground and power planes the two inner planes?

In considering this question, it is important to remember that, no matter what is decided, signals will still be exposed on one or both of the top and bottom planes. The leads of the op amp PCB package and the traces on the board leading to nearby passive

components and feed throughs will be exposed. Therefore, all shielding effects are compromised. It is far better to take advantage of the distributed capacitance between the power and ground plane by making them internal.

Another advantage of placing the planes internally is that the signal traces are available for probing and modification on the top and bottom layers. Anyone who has had to change connections on buried traces appreciates this feature.

For more than four layers, it is a general rule to shield higher speed signals between the ground and power planes and route slower signals on the outer layers.

23.3 Grounding

Good grounding is a system level design consideration. It should be planned into the product from the first conceptual design reviews.

23.3.1 The Most Important Rule: Keep Grounds Separate

Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. If the designer is not careful, the analog circuitry will be connected directly to these ground planes. The analog circuitry return, after all, is the same net in the netlist as digital return. Autorouters respond accordingly and connect all the grounds, creating a disaster.

After the fact separation of grounds on a mixed digital and analog board is almost impossible. Every ground connection in the analog circuitry must be lifted from the board and connected together. For surface mount boards, this results in a colossal mess of "tombstoned" passive components and floating IC leads.

23.3.2 Other Ground Rules

- Ground and power planes are at the same AC potential, due to decoupling capacitors and distributed capacitance. Therefore, it is important to isolate the power planes as well.
- Do not overlap digital and analog planes (Figure 23.2). Place analog power coincident with analog ground and digital power coincident with digital ground.

If any portion of analog and digital planes overlap, the distributed capacitance between the overlapping portions couples high speed digital noise with the analog circuitry. This defeats the purpose of isolated planes.

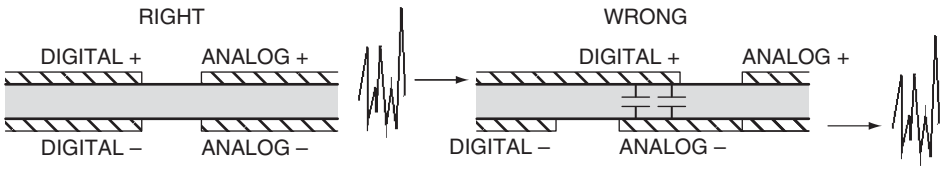


Figure 23.2: Digital and analog plane placement.

- *Separate grounds* (Figure 23.3) does not mean that the grounds are electrically separate in the system. They have to be common at some point, preferably a single, low impedance point. Systemwise, there is only one ground, and it is the electrical safety ground in an AC powered system or battery ground in a DC powered system. Everything else "returns" to that ground. It would be a good idea to develop the discipline to refer to everything that is not a *ground* as a *return*. All returns should be connected together at a single point, which is the system ground. At some point, this will be the chassis. It is important to avoid ground loops by multiple connections to the chassis. Ensuring only one chassis ground point is one of the most difficult aspects of system design.

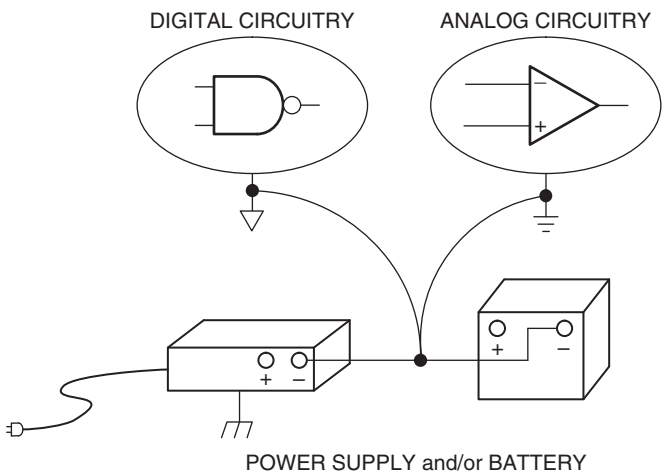


Figure 23.3: Separate grounds.

- If at all possible, dedicate separate connector pins to separate returns and combine the returns only at the system ground. Aging and repeated mating cause connector pins to increase in contact resistance, so several pins are needed. Many digital boards consist of many layers and hundreds or thousands of nets. The addition of one more net is seldom an issue, but the addition of several connector pins almost always is. If this cannot be done, then it will be necessary to make the two returns a single net on the PCB—with very special routing precautions.
- It is important to keep digital signals away from analog portions of the circuit. It makes little sense to isolate planes, keep analog traces short, and place passive components carefully if high speed digital traces are running right next to the sensitive analog traces. Digital signals must be routed around analog circuitry and not overlap analog ground and power planes. If not, the design will include a new schematic symbol shown in Figure 23.4, the broadcasting antenna! Most digital clocks are high enough in frequency that even small capacitances between traces and planes can couple significant noise. Remember that it is not only the fundamental frequency of the clock that can cause a potential problem but also the higher frequency harmonics.

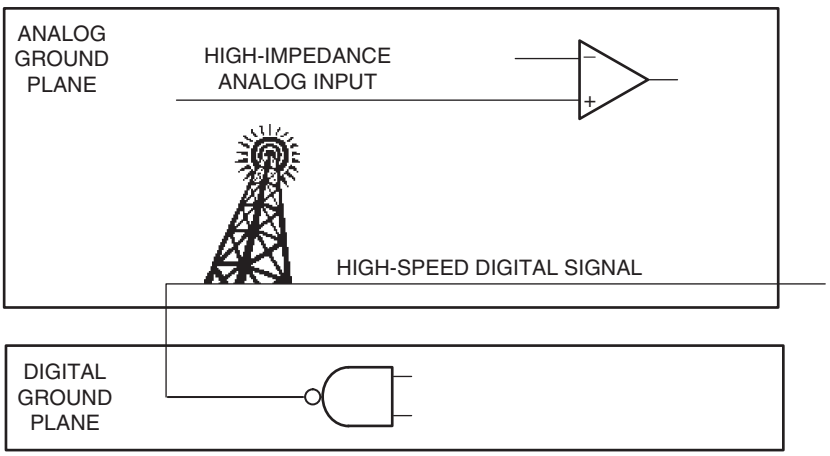


Figure 23.4: Broadcasting from PCB traces.

- It is a good idea to locate analog circuitry as close as possible to the input/output connections of the board. Digital designers, used to high current ICs, will be tempted to make a 50 mil trace run several inches to the analog circuitry, thinking that reducing the resistance in the trace will help get rid of noise. What they actually do is create a long, skinny capacitor that couples noise from digital ground and power planes into the op amp, making the problem worse!

23.3.3 A Good Example

Figure 23.5 shows a possible board layout. In this system, all electronics, including the power supply, reside on one PCB. Three isolated ground/power planes are employed: one for power, one for digital, and one for analog. Power and ground connections from digital and analog sections of the board are combined only in the supply section and are combined in close proximity. High frequency conducted noise on the power lines is limited by inductors (chokes). In this case, the designer has even located low frequency analog circuitry close to low speed digital, keeping high frequency digital and analog physically apart on the board. This is a good, careful design that has a high likelihood of success—providing good layout and decoupling rules are also followed.

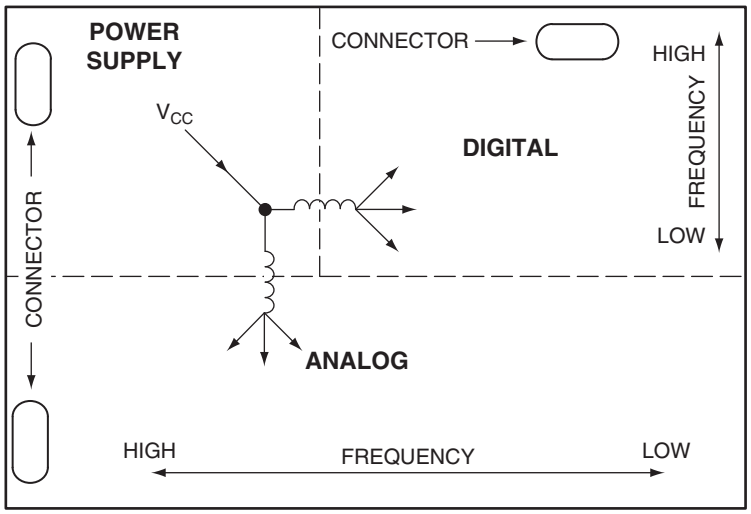


Figure 23.5: A careful board layout.

23.3.4 A Notable Exception

In one case, it is necessary to combine analog and digital signals on the analog ground plane. Analog to digital and digital to analog converters (ADCs and DACs) are packaged as ICs with analog and digital ground pins coming out of the package. One might assume, based on the previous discussion, that the digital ground pin should be connected to digital ground and the analog ground pin to analog ground. That, however, is not correct.

The pin names *analog ground* and *digital ground* refer to internal connections in the IC, not the plane to which they should be connected. Both should connect to the analog ground plane. The connection would have been made inside the IC, but it is impossible to get low enough impedance at the typical geometries inside ICs. The IC designer actually counts on the end user to supply a low impedance connection outside the IC. Otherwise, the performance of the converter is worse than specified.

One might suspect that the digital portions of the converter would make circuit performance worse by coupling digital switching noise onto the analog ground and power plane. Converter designers realize this and design digital portions without a lot of output power to minimize switching transients. If the converter does not drive large fanouts, this should be no problem. Be sure to properly decouple the logic supply for the converter to analog ground (see the following section).

23.4 The Frequency Characteristics of Passive Components

Choosing the right passive components for an analog design is important. In most cases, a *right* passive component fits on the same pads as a *wrong* passive component but not always. Start the design process by carefully considering the high frequency characteristics of passive components and putting the correct part outline on the board from the start.

Most designers are totally ignorant of the frequency limitations of the passive components they use in analog circuitry. Passive components have limited frequency ranges, and operation of the part outside that range can have some very unexpected results. One might think that this discussion applies only to high speed analog circuits. But high frequencies that are radiated or conducted into a low speed circuit also affect passive components. For example, a simple op amp low pass filter may well turn into a high pass filter at RF frequencies.

23.4.1 Resistors

High frequency performance of resistors is approximated by the schematic shown in Figure 23.6.

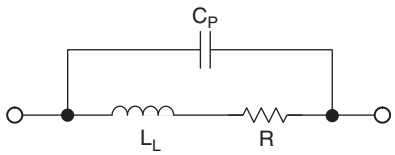


Figure 23.6: Resistor high frequency performance.

Resistors are typically one of three types: wire wound, carbon composition, or film. It does not take a lot of imagination to understand how wire wound resistors can become inductive, because they are coils of resistive wire. Most designers are not aware of the internal construction of film resistors, which are also coils of thin metallic film. Therefore, film resistors are also inductive at high frequencies. The inductance of film resistors is lower, however, and values under 2 kΩ are usually suitable for high frequency work.

The end caps of resistors are parallel, and there will be an associated capacitance. Usually, the resistance will make the parasitic capacitor so "leaky" that the capacitance does not matter. For very high resistances, the capacitance appears in parallel with the resistance, lowering its impedance at high frequencies.

23.4.2 Capacitors

High frequency performance of capacitors is approximated by the schematic shown in Figure 23.7. Capacitors are used in analog circuitry for power supply decoupling and as filter components. For an ideal capacitor, reactance decreases by the formula

$$X_C = \frac{1}{(2\pi fC)} \tag{23.1}$$

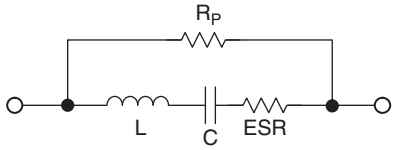


Figure 23.7: Capacitor high frequency performance.

where

X_C = capacitive reactance in ohms.

f = frequency in hertz.

C = capacitance in microfarads.

Therefore, a 10 μF electrolytic capacitor has a reactance of 1.6 Ω at 10 kHz and 160 μΩ at 100 MHz. Right?

In reality, one never sees the 160 μΩ with the electrolytic capacitor. Film and electrolytic capacitors have layers of material wound around each other, which creates a parasitic inductance. The self-inductance effects of ceramic capacitors are much smaller, giving them a higher operating frequency. There is also some leakage current from plate to plate, which appears as a resistance in parallel with the capacitor, as well as resistance within the plates themselves, which add a parasitic series resistance. The electrolyte itself in electrolytic capacitors is not perfectly conductive (to reduce leakage current). These resistances combine to create the equivalent series resistance (ESR). The capacitors used for decoupling should be low ESR types, as any series resistance limits the effectiveness of the capacitor for ripple and noise rejection. Elevated temperatures also severely increase the ESR and can be permanently destructive to capacitors. Therefore, if an aluminum electrolytic will be subjected to high temperatures, use the high temperature grade (105°C) not the low temperature grade (85°C).

For leaded parts, the leads themselves also add a parasitic inductance. For small values of capacitance, it is important to keep the lead lengths short. The combination of parasitic inductance and capacitance can produce resonant circuits! Assuming a lead self-inductance of 8 nH/cm (see the following sections), a 0.01 μF capacitor with two 1 cm leads resonates at 12.5 MHz. This effect was well known to engineers many decades ago, who designed vacuum tube based products with leaded components. Woe be to any hobbyist restoring antique radios that is unaware of this effect!

If electrolytic capacitors are used in a design, make sure that the polarity is correctly observed. The positive terminal of the capacitor must be connected to the more positive of two DC potentials. If there is any doubt whatsoever which polarity is correct, design calculations must continue until it is known, or a prototype must be built. Incorrect polarity of electrolytic capacitors causes them to conduct DC current, in most cases, destroying the part—and probably the rest of the circuit as well. If there is a rare case in

which both polarities are present, use a nonpolarized electrolytic capacitor (which is constructed by connecting two polarized electrolytic capacitors in series). Of course, one can always connect two capacitors in series on the PCB, keeping in mind that the effective capacitance is cut in half for equal values of capacitor.

23.4.3 Inductors

High frequency performance of inductors is approximated by the schematic shown in Figure 23.8. Inductive reactance is described by the formula

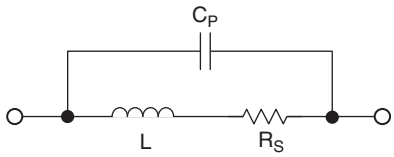


Figure 23.8: Inductor high frequency performance.

$$X_L = 2\pi fL \tag{23.2}$$

where

X_L = inductive reactance in ohms.

f = frequency in hertz.

L = inductance in Henrys.

Therefore, a 10 mH inductor has a reactance of 628 Ω at 10 kHz, which increases to 6.28 MΩ at 100 MHz. Right?

In reality, one never sees the 6.28 MΩ with this inductor. Parasitic resistances are easy to understand: The inductor is constructed of wire, which has a given resistance per unit length. Parasitic capacitance is harder to visualize, unless one considers that each turn of wire in the inductor is located next to adjacent turns, forming a capacitor. This parasitic capacitance limits the upper frequency of this inductor to under 1 MHz. Even small wire wound inductors start to become ineffective in the 10 MHz to 100 MHz range.

23.4.4 Unexpected PCB Passive Components

In addition to the obvious passive components just discussed, the PCB itself has characteristics that form components every bit as real as those discussed previously—just not as obvious.

PCB Trace Characteristics

The layout pattern on a PCB can make it susceptible to radiated noise. A good layout minimizes the susceptibility of analog circuitry to as many radiated noise sources as possible. Unfortunately, some level of RF energy always is able to upset the normal operation of the circuit. If good design techniques are followed, this level is one that the circuit never encounters in normal operation.

Trace Antennas A board is susceptible because the pattern of traces and component leads form antennas. Antenna theory is a complex subject, well beyond the scope of this book. Nevertheless, a few basics are presented here.

One basic type of antenna is the whip, or straight conductor. This antenna works because a straight conductor has parasitic inductance and therefore can concentrate flux from external sources. The impedance of any straight conductor has a resistive component and an inductive component:

$$Z = R + j\omega L \tag{23.3}$$

For DC and low frequencies, resistance is the major factor. As the frequency increases, however, the inductance becomes more important. Somewhere in the range of 1 kHz to 10 kHz, the inductive reactance exceeds the resistance, so the conductor is no longer a low resistance connection but rather an inductor.

The formula for the inductance of a PCB trace is

$$L(\mu H) = 0.0002X \times \left[\ln\left(\frac{2X}{W + H}\right) + 0.2235\left(\frac{W + H}{X}\right) + 0.5\right] \tag{23.4}$$

where

X = length of the trace.

W = width of the trace.

H = thickness of the trace.

The inductance is relatively unaffected by the diameter, since it varies as the logarithm of the circumference. Common wires and PCB traces vary between 6 nH and 12 nH per centimeter.

For example, a 10 cm PCB trace has a resistance of 57 mΩ and an inductance of 8 nH per centimeter. At 100 kHz, the inductive reactance reaches 50 mΩ. At frequencies above 100 kHz, the trace is inductive—not resistive.

A rule of thumb for whip antennas is that they begin to couple significant energy at about one 20th of the wavelength of the received signal, peaking at one quarter the wavelength. Therefore, the 10 cm conductor of the previous paragraph begins to be a fairly good antenna at frequencies above 150 MHz. Remember that, although the clock generator on a digital PCB may not operate at a frequency as high as 150 MHz, it approximates a square wave. Square waves have harmonics throughout the frequency range where PCB conductors become efficient antennas. If through hole components are mounted in a way that leaves significant lead length, those component leads also become antennas, particularly if they are bent.

Another major type of antenna is the loop. The inductance of a straight conductor is dramatically increased by bending it into partial or complete loops. Increased inductance lowers the frequency at which the conductor couples radiated signals into the circuit.

Without realizing it, most digital designers are well versed in loop antenna theory. They know not to make loops in critical signal pathways. Some designers that would never think of making a loop with a high speed clock or reset signal, however, turn right around and create a loop by the technique they use for layout of the analog section of the board. Loop antennas constructed as loops of wire are easy to visualize. What is not as obvious is that slot antennas are just as efficient. Consider the three cases shown in Figure 23.9.

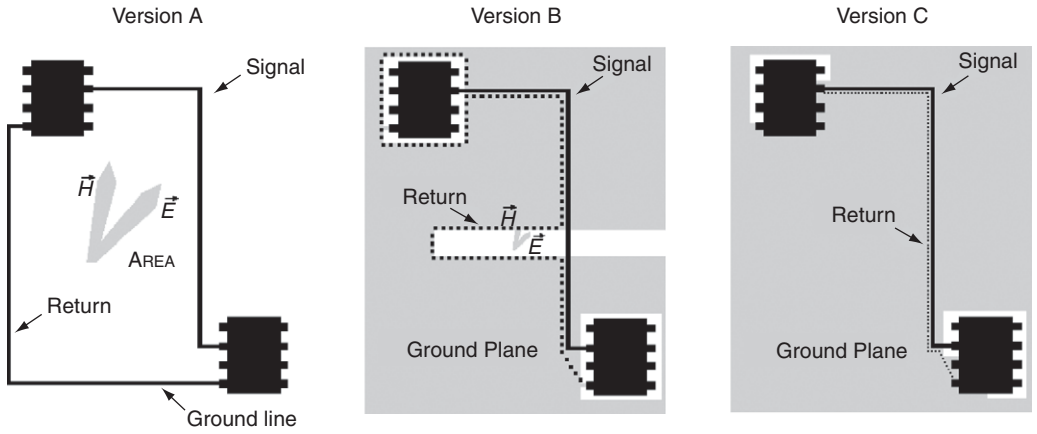


Figure 23.9: Loop and slot antenna board trace layouts.

Version A is a poor design. It does not use an analog ground plane at all. A loop is formed by the ground and signal traces. An electric field, *E*, and perpendicular magnetic field, *H*, are created and form the basis of a loop antenna. A rule of thumb for loop antennas is that the length of each leg is equal to half the most efficiently received wavelength. Remember, however, that, even at one 20th of the wavelength, the loop still is a fairly efficient antenna.

Version B is a better design, but there is intrusion into the ground plane, presumably to make room for a signal trace. A much smaller slot antenna is formed by the difference in pathways between signal and return. A second loop is created by the cutout for the IC.

Version C is the best design. Signal and return are coincident with each other, eliminating loop antenna effects completely. Note that there is still a cutout for the IC, but it is located away from the return path for the signal.

Trace Reflections Reflections and matching are closely related to loop antenna theory but different enough to warrant their own discussion.

When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change in width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self-inductance of the trace, resulting in the reflection. It is a given that not all PCB traces can be straight, so they have to turn

corners. Most CAD systems give some rounding effect on the trace. Sharp 90° corners in traces are a relic of the *tape up* days of PCB layout. The rounding effects of CAD programs, however, still do not necessarily maintain constant width as the trace rounds the corner. Figure 23.10 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections. Most CAD programs now support these methods, but they can entail a little more work to master.

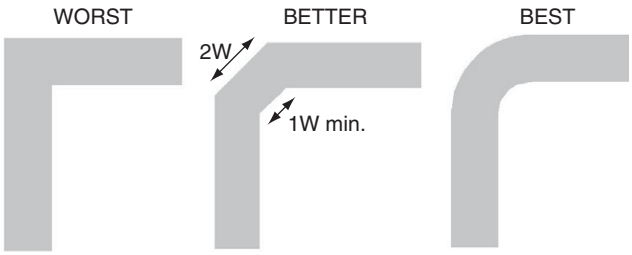
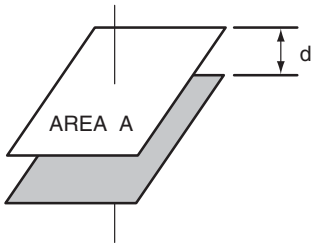


Figure 23.10: PCB trace corners.

A suggestion for the advanced PCB layout engineer is to leave rounding to the last step before tear dropping and flood filling. Otherwise, the CAD program slows down doing numerical calculations as the traces are moved around during routing.

Trace to Plane Capacitors

PCB traces, being composed of foil, form capacitance with other traces that they cross on other layers. For two traces crossing each other on adjacent planes, this is seldom a problem. Coincident traces (those that occupy the same routing on different layers), form a long, skinny capacitor. The formula for capacitance is shown in Figure 23.11.



$$C = 0.0085 \times \epsilon_R \times \frac{A}{d}$$

where:

C = capacitance (pF)

ϵ_R = dielectric constant

A = area of plate (mm^2)

d = separation of plates (mm)

Figure 23.11: PCB trace to plane capacitance formula.

For example, if the capacitance formula is applied to the following trace:

- Four layer board, signal routing next to the ground plane.
- Board layer thickness, 0.188 mm.
- Trace width, 0.75 mm.
- Trace length, 7.5 mm.

A typical value for E_R of FR–4 PCB material is 4.5. Due to the variations of material from which an FR–4 board can be fabricated, this value is not guaranteed but should be in the range of 4 to 5.

The capacitance between these traces would be 1.1 pF. Of course, the antenna effect on a 7.5 mm trace would be devastating, so this example is a bit extreme. Ignoring the antenna effects for now, in some cases, even a very small parasitic capacitance, like 1 pF, is unacceptable. Figure 23.12 dramatically illustrates the effect of 1 pF capacitance occurring at the inverting input of the op amp. It causes doubling of the output amplitude near the bandwidth limit of the op amp. This is an invitation to oscillation, especially since the trace is an efficient antenna above 180 MHz.

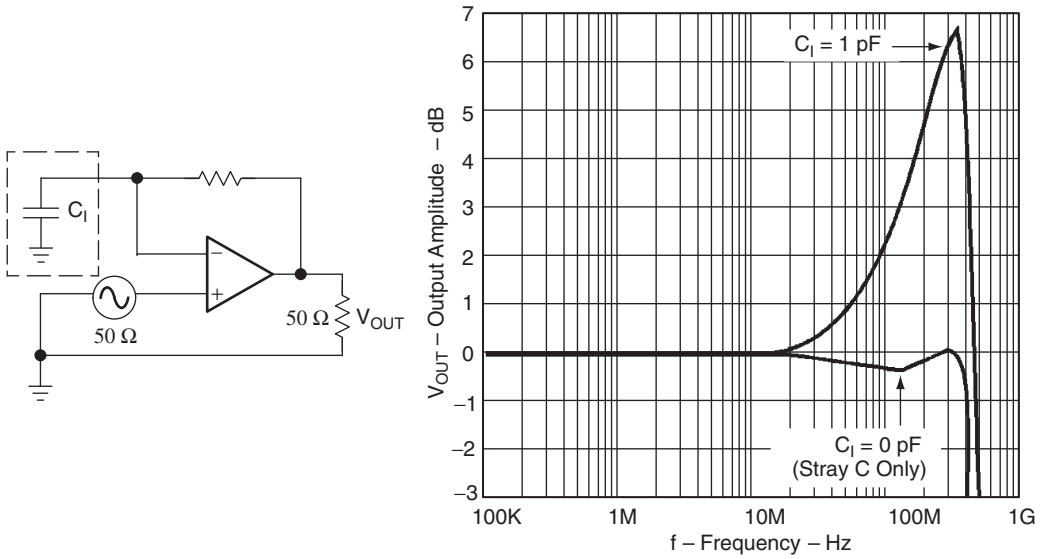


Figure 23.12: Effect of a 1 pF capacitance on op amp inverting input.

There are numerous fixes to this problem. The most obvious would be to shorten the length of the traces. Another, not so obvious fix would be to use a different trace width. There is no reason why an inverting op amp trace has to be 0.75 mm wide—it carries almost no current. If the trace length is reduced to 2.5 mm (one third as long) and the trace width is changed to 0.188 mm (one quarter as wide), the capacitance becomes 0.1 pF, much less significant in the preceding example. Another fix is to remove the ground plane under the inverting input and the traces leading to it.

The inverting input of op amps, particularly high speed op amps, is especially prone to oscillation in high gain circuits. This is due to unwanted capacitance on the input stage. It is important to minimize capacitance on this input by reducing trace width and placing components as close as possible to this input. If this input still oscillates, it may be necessary to scale the input and feedback resistors lower by a decade or two to change the resonance of the circuit. Scaling up the resistors seldom helps, as the problem is also related to the impedance of the circuit. If filter components are involved, they also must be scaled to avoid changing the filter characteristics of the circuit. The power consumption of the circuit also increases if resistors are lowered.

Trace to Trace Capacitors and Inductors

PCB traces are not infinitely thin. They have some finite thickness, as defined by the *ounce* parameter of the copper clad foil. The higher the number of ounces, the thicker the copper. If two traces run side by side, then there is capacitive and inductive coupling between them (Figure 23.13). The formulas for these parasitic effects can be found in transmission line or microstrip references but are too complex for inclusion here.

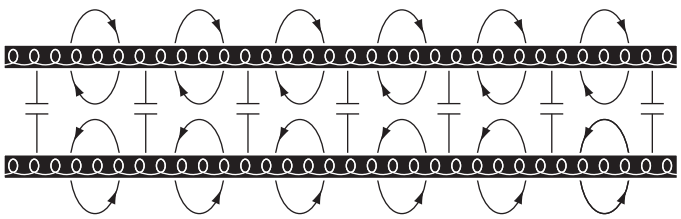


Figure 23.13: Coupling between parallel signal traces.

Signal lines should not be routed parallel to each other, unless transmission line or microstrip effects are desired. Otherwise, a gap of at least three times the signal trace width should be maintained.

Capacitance between traces in an analog design can become a problem if fixed resistors in the design are large (several megaohms). Capacitance between the inverting and noninverting inputs of an op amp could easily cause oscillation.

Inductive Vias

Whenever routing constraints force a *via* (connection between layers of a PCB, Figure 23.14), a parasitic inductor is also formed. At a given diameter (d), the approximate inductance (L) of an via at a height of (h) may be calculated as follows:

$$L = \approx \frac{h}{5} \times \left[1 + \ln\left(\frac{4h}{d}\right)\right] \text{nH} \tag{23.5}$$

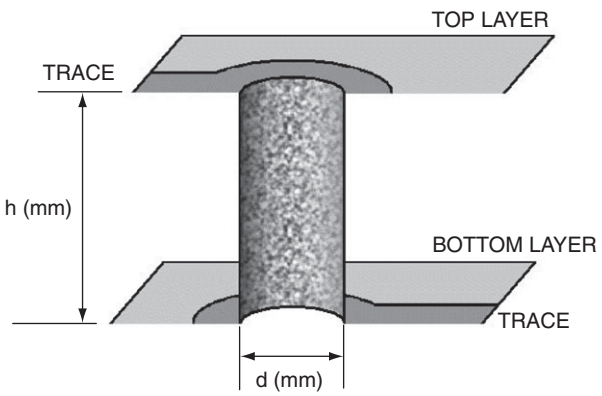


Figure 23.14: Via inductance measurements.

For example, a 0.4 mm diameter via through a 1.5 mm thick PCB has an inductance of 1.1 nH.

Keep in mind that inductive vias combined with parasitic capacitance can form resonant circuits. The self-inductance of a via is small enough that these resonances are in the gigahertz range, but inductors add in series, lowering the resonant frequency. Do not put several vias on a critical trace of a high speed analog circuit! Another

concern is that the vias put holes in ground planes, potentially creating ground loops. They should be avoided: The best analog layout is one that routes all signal traces on the top layer of the PCB.

Flux Residue Resistance

Yes, even an unclean board can affect analog circuit performance.

Be aware that if the circuit has very high resistances, even in the low megaohms, special attention may need to be paid to cleaning. A finished assembly may be adversely affected by flux or cleansing residue. The electronics industry in the past few years has joined the rest of the world in becoming environmentally responsible. Hazardous chemicals are being removed from the manufacturing process, including flux that has to be cleaned with organic solvents. Water soluble fluxes are becoming more common, but water itself can easily become contaminated with impurities. These impurities lower the insulation characteristics of the PCB substrate. It is vitally important to clean with fresh distilled water every time a high impedance circuit is cleaned. Some applications that may call for the older organic fluxes and solvents, such as very low power battery powered equipment with resistors in the tens of megaohm range. Nothing can beat a good vapor defluxing machine for ensuring that the board is clean.

23.5 Decoupling

Noise, of course, can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.

23.5.1 Digital Circuitry: A Major Problem for Analog Circuitry

If analog circuitry is located on the same board with digital circuitry, it is important to understand a little about the electrical characteristics of digital gates.

A typical digital output consists of two transistors connected in series between power and ground (Figure 23.15). One transistor is turned on and the other turned off to produce logic high and vice versa for logic low. Because one transistor is turned off for either logic state, the power consumption for either logic state is low, while the gate is static at that level.

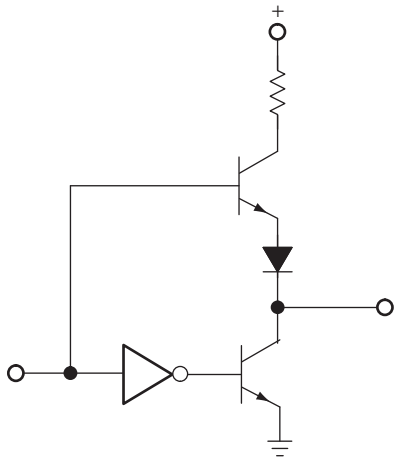


Figure 23.15: Logic gate output structure.

The situation changes dramatically whenever the output switches from one logic state to the other. For a brief period of time, both transistors conduct simultaneously. During this period of time, current drawn from the power supply increases dramatically, since there is now a low impedance path through the two transistors from power to ground. Power consumption rises dramatically then falls, creating a droop on the power supply voltage and a corresponding current spike. The current spike radiates radio frequency (RF) energy. There may be dozens or even hundreds of such outputs on a digital IC, so the aggregate effect may be quite dramatic.

It is impossible to predict the frequencies of these spikes, because the frequencies are affected by the propagation delays of the transistors in the gate. Propagation delay is affected by random factors that occur during manufacture. Digital switching noise is broadband, with harmonics throughout the spectrum. A general rejection technique is required, rather than one that rejects a specific frequency.

23.5.2 Choosing the Right Capacitor

Table 23.2 is a rough guideline describing the maximum useful frequencies of common capacitor types.

Table 23.2: Recommended Maximum Frequencies for Capacitors

Type	Maximum frequency
Aluminum electrolytic	100 kHz
Tantalum electrolytic	1 MHz
Mica	500 MHz
Ceramic	1 GHz

Obviously, from the table, tantalum electrolytic capacitors are useless for frequencies above 1 MHz. Effective high frequency decoupling at higher frequencies demands a ceramic capacitor. Self-resonances of the capacitor must be known and avoided, or the capacitor may not help or even make the problem worse. Figure 23.16 illustrates the typical self-resonance of two capacitors commonly used for bypassing: 10 µF tantalum electrolytic and 0.01 µF ceramic.

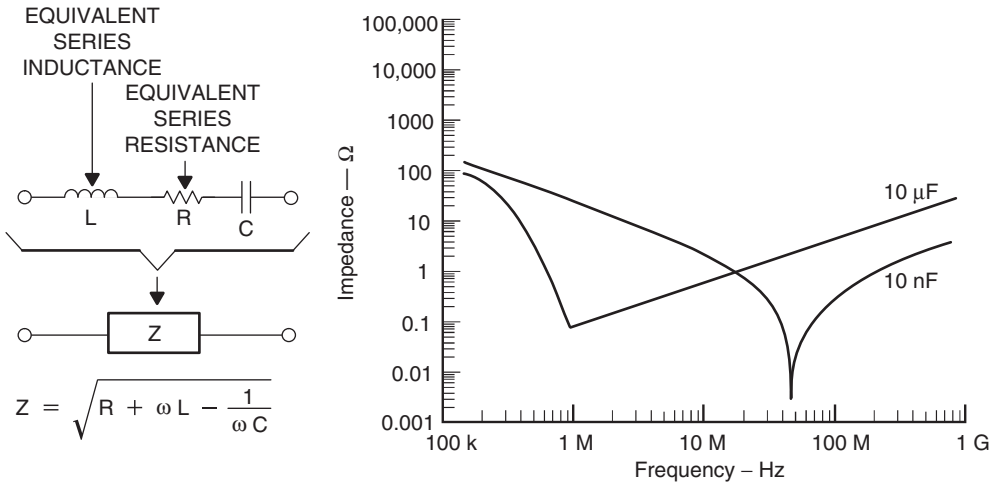


Figure 23.16: Capacitor self-resonance.

Consider these resonances to be typical values, the characteristics of actual capacitors can vary from manufacturer to manufacturer and grade of part to grade of part. The important thing is to make sure that the self-resonance of the capacitor occurs at a frequency above the range of the noise that must be rejected. Otherwise, the capacitor enters a region where it is inductive.

Do not assume that a single 0.1 μF capacitor will decouple all frequencies. Smaller capacitors may work better at higher frequencies than larger ones. When poor decoupling at higher frequencies is suspected, try a smaller capacitor rather than a larger one.

23.5.3 Decoupling at the IC Level

The method most often used to decouple the high frequency noise is to include a capacitor or multiple capacitors connected from the op amp power pin to the op amp ground pin. It is important to keep the traces on this decoupling capacitor short. If not, the traces on the PCB have significant self-inductance, defeating the purpose of the capacitor.

A decoupling capacitor must be included on every op amp package, whether it contains one, two, or four devices per package. The value of capacitor must be picked carefully to reject the type of noise present in the circuit.

In particularly troublesome cases, it may be necessary to add a series inductor into the power supply line connecting to the op amp. This inductor is in addition to the decoupling capacitors, which are the first line of defense. The inductor should be located before, not after, the capacitors.

Another technique that is lower in cost is to replace the series inductor with a small resistor in the 10 Ω to 100 Ω range. The resistor forms a low pass filter with the decoupling capacitors. There is a penalty to pay for this technique: Depending on the power consumption of the op amp, it will reduce the rail to rail voltage range. The resistor forms a voltage divider with the op amp as a resistive active component in the lower leg of the divider. Depending on the application, this may or may not be acceptable.

23.5.4 Decoupling at the Board Level

Usually, enough low frequency ripple is on the power supply at the board input to warrant a bulk decoupling capacitor at the power input. This capacitor is used primarily to reject low frequency signals, so an aluminum or tantalum capacitor is acceptable. An additional ceramic cap at the power input decouples any stray high frequency switching noise that may be coupled off of the other boards.

23.6 Input and Output Isolation

Many noise problems are the result of noise being conducted into the circuit through its input and output pins. Due to the high frequency limitations of passive components, the response of the circuit to high frequency noise may be quite unpredictable.

In situations in which conducted noise is substantially different in frequency from the normal operating range of the circuit, the solution may be as simple as a passive RC low pass filter that rejects RF frequencies while having negligible effect at audio frequencies. A good example is RF noise being conducted into an audio op amp circuit. Be careful, though. A low pass filter loses its characteristics at 100 to 1000 times f_{3dB}. More stages may be required to cover different frequency ranges. If this is the case, make the highest frequency filter the one nearest the source of noise. Inductors or ferrite beads can also be used in a noise rejection filter network to eliminate conducted noise. Ferrite beads are inductive up to a specified frequency then become resistive.

The effect of radiated energy coupling into an analog circuit can be so bad that the only solution to the problem may be to completely shield the circuit from radiated energy. This shield, called a *Faraday cage*, must be carefully designed so that the frequencies causing the problem are not allowed to enter the circuit. This means that the shield must have no holes or slots larger than one 20th the wavelength of the offending frequency. This can be a demanding requirement. It is a good idea to design a PCB from the beginning to have enough room to add a metal shield if it becomes necessary. If a shield is used, frequently the problem is severe enough that ferrite beads also are required on all connections to the circuit.

23.7 Packages

Op amps are commonly supplied one, two, or four per package (Figure 23.17). Single op amps often contain additional inputs for features such as offset nulling. Op amps supplied two and four per package offer only inverting and noninverting inputs and the output. If additional features are important, the only package choice is single. Be aware, though, that the offset nulling pins on a single op amp package can act as secondary inputs and must be treated carefully. Consult the data sheet on the particular device being used.

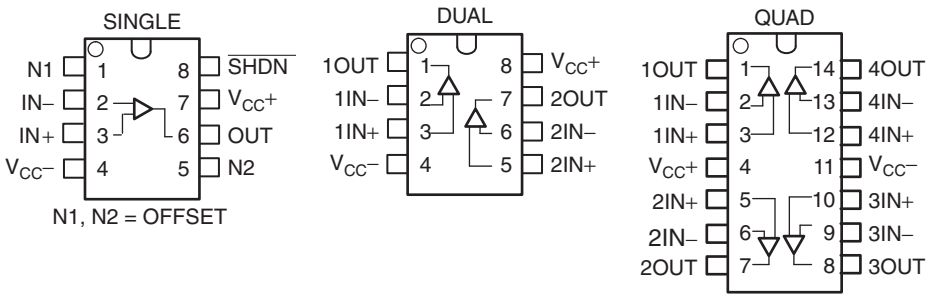


Figure 23.17: Common op amp pinouts.

The single op amp package places the output on the opposite side from the inputs. This can be a disadvantage at high speeds, because it forces longer PCB traces. One way to overcome this difficulty is to use a surface mount package and mount the feedback components on the rear of the board. This, however, adds at least two vias to the design and places a hole in the ground plane for a two layer design. It may make more sense to use a dual op amp package, even if the second op amp is unused (remember to terminate it properly, see Section 23.7.3). Figure 23.18 illustrates a trace length for an inverting op amp stage.

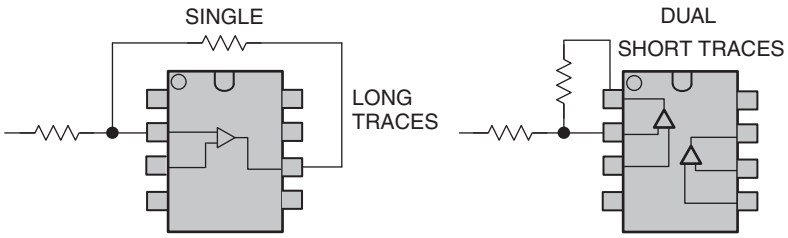


Figure 23.18: Trace length for an inverting op amp stage.

It is popular to use dual op amps for stereophonic circuits and quad op amps for filter stages with many sections. There is a penalty for doing so, however. Although modern processing techniques provide high levels of isolation between amplifiers on the same piece of silicon, there is some crosstalk. If isolation between amplifiers is important, then single packages should be considered. Crosstalk problems are not limited to the IC—the dual and quad packages place a high density of passive components in close proximity to each other. This proximity leads to some crosstalk.

Dual and quad op amp packages offer additional benefits beyond density. The amplifier stages tend to be mirror images of each other. If similar stages are to be laid out on the PCB, the layout needs to be done only once, then it can be mirror imaged to form the other stage. Figure 23.19 illustrates this effect for four inverting op amp stages implemented in a quad package.

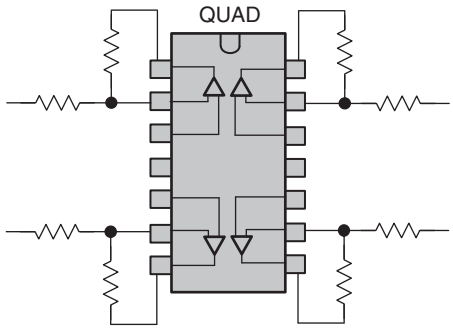


Figure 23.19: Mirror image layout for quad op amp package.

These illustrations, however, do not show all connections required for operation, in particular, the half supply generator for single supply operation. Modifying the diagram of Figure 23.19 to use the fourth op amp as a half supply generator is shown in Figure 23.20.

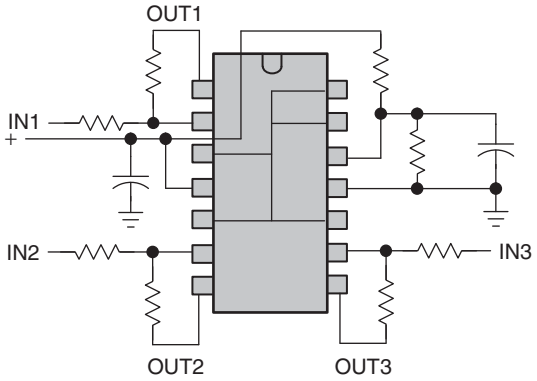


Figure 23.20: Quad op amp package layout with half supply generator.

This example shows all the connections actually required to produce three independent inverting stages. Note that the half supply connection can be made entirely under the IC, keeping the trace length short. This example is not meant to be used as a suggested PCB layout, it merely illustrates what can be done. The half supply op amp, for example, could be any one of the four. The passive components can be selected so that they span the lead pitch. Surface mount 0402 packages, for example, span a width equal to or less than a standard small outline package. This can keep trace lengths extremely short for high frequency applications.

Package styles for op amps include the dual inline and small outline. Lead pitches for op amps have been continually decreasing, as has been the case for all ICs in general. Decreasing lead pitches are accompanied by a decrease in the size of passive components as well. Decreasing the overall circuit dimensions reduces parasitic inductance, which should allow higher frequency circuits, but it also increases the potential for crosstalk by placing conductors closer to each other where capacitive effects increase.

23.7.1 Through Hole Considerations

The older technology for op amps and other components is through hole. Components are constructed with leads that insert through holes in the board, hence the name.

Through hole components, due to their size, are better suited to applications where space is not an issue. The components themselves are frequently lower in cost but the PCB is more expensive, because the PCB fabrication house has to drill holes for component leads. PCBs are primarily a mechanical fabrication; the number of holes and number of different drills have a big impact on the price.

The leads on a through hole op amp are arranged on a 0.1 in. grid. Many PCB layout people like to maintain the 0.1 in. grid for the rest of the components as well. Resistors and other passive components can even be purchased with leads prebent to land on a 0.1 in. grid. Some electrolytic capacitors have leads that are on a 0.025 in. grid.

These component sizes may force a lot of wasted area on the PCB. Components that ideally should be placed close to the op amp itself may be forced several tenths of an inch away, due to intervening components. Therefore, through hole circuitry is not recommended for high speed analog circuitry or for analog circuitry in proximity to high speed digital.

Some designers attempt to overcome the long trace length caused by resistors by placing the resistors on the board vertically, one lead of the resistor bent close to the body of the part. This is common in older consumer electronics. This allows for denser placement of parts and may help some with trace length, but each resistor exposes almost 1 cm of one component lead to radiated signals and lead self-inductance.

An advantage of the through hole approach of PCB layout is that the through holes themselves can serve as feed throughs, reducing the number of vias in complex circuits.

23.7.2 Surface Mounting

Surface mount circuitry does not require a hole for each component lead. Automated testing, however, may require vias on every node. The holes were never an issue with through hole circuitry, because every component lead made a hole in the board. The PCB layout designer who is used to designing a board with a minimum number of vias now has to put a via on *every* node of the circuit. This can make Swiss cheese out of a nice continuous ground plane, negating many of the advantages it provides.

Fortunately, there is a close variation of the "via on every node" requirement. This requirement can often be met by putting a test pad on every node. The automated test station can then access the analog circuitry from the top of the board. A *clamshell test* fixture is significantly more expensive than one that accesses only one side of the board. The extra cost can be justified if there is documentation that circuit performance will be unacceptable with vias.

Signal connections to ground or the power supply may have to be made through a small fixed resistor instead, so the automated equipment can access that pin of the IC and test its function.

23.7.3 Unused Sections

In many op amp designs, one or more op amps may be unused. If this is the case, the unused section must be terminated properly. Improper termination can result in greater power consumption, more heat, and more noise in op amps on the same physical IC. If the unused section of the op amp is connected as shown in the *better* side of Figure 23.21, it will be easier to use it for design changes.

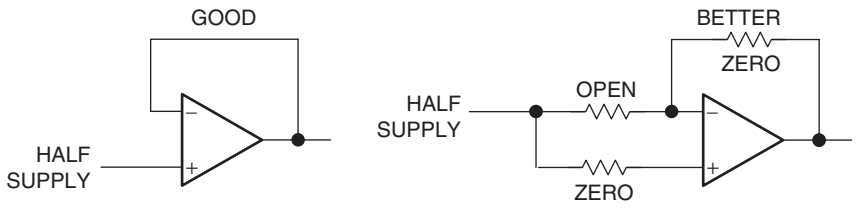


Figure 23.21: Proper termination of unused op amp sections.

23.8 Summary

Keep the following points in mind when designing a PCB for analog circuitry.

23.8.1 General

- Think of the PCB as a component of the design.
- Know and understand the types of noise to which the circuit will be subjected.
- Prototype the circuit.

23.8.2 Board Structure

- Use a high quality board material, such as FR–4.
- Multilayer boards are as much as 20 dB better than double sided boards.
- Use separate, nonoverlapping ground and power planes.
- Place power and ground planes to the interior of the board instead of the exterior.

23.8.3 Components

- Be aware of frequency limitations of traces and other passive components.
- Avoid vertical mounting of through hole passive components in high speed circuits.

- Use surface mount for high speed analog circuitry.
- Keep traces as short as possible.
- Use narrow traces if long traces are required.
- Terminate unused op amp sections properly.

23.8.4 Routing

- Keep analog circuitry close to the power connector of the board.
- Never route digital traces through analog sections of the board or vice versa.
- Make sure that traces to the inverting input of the op amp are short.
- Make sure that traces to the inverting and noninverting inputs of the op amp do not parallel each other for any significant length.
- It is better to avoid vias, but the self-inductance of vias is small enough that a few should cause few problems.
- Do not use right angle traces, use curves if at all possible.

23.8.5 Bypassing

- Use the correct type of capacitor to reject the conducted frequency range.
- Use tantalum capacitors at power input connectors for filtering power supply ripple.
- Use ceramic capacitors at power input connectors for high frequency conducted noise.
- Use ceramic capacitors at the power connections of every op amp IC package. More than one capacitor may be necessary to cover different frequency ranges.
- Change the capacitor to a smaller—not larger—value if oscillation occurs.
- Add series inductors or resistors for stubborn cases.
- Bypass analog power only to analog return, never to digital return.

References

1. Bryant, James. (2002). "Ask the Applications Engineer –10." *Analog Devices*, Analog Dialog 30th Anniversary Issue.
2. Hahn, Andy. (2000). *High-Speed Operational Amplifier Layout Made Easy*, SLOA046. Dallas: Texas Instruments.

CHAPTER 24

Designing Low Voltage Op Amp Circuits

Ron Mancini

24.1 Introduction

In one respect, voltage is like water: you don't appreciate its value until your supply runs low. Low voltage systems, defined here as a single power supply less than 5 V, teach us to appreciate voltage. We aren't the first electronic types to learn how valuable voltage is; over 20 years ago, the audio console design engineers appreciated the relationship between voltage and dynamic range. They needed more dynamic range to satisfy their customers; therefore, they ran op amps at the full rated voltage not the recommended operating voltage, so they could squeeze a few more decibels of dynamic range from the op amp. These engineers were willing to take a considerable risk running op amps at the full rated voltage, but their customers demanded more dynamic range. The moral of this story is that dynamic range is an important parameter, and supply voltage is tied directly to dynamic range.

Knowing how to obtain and use the maximum dynamic range and input/output voltage range is critical to achieving success in low voltage design. We investigate these subjects in detail later, but for now it is useful to review the history of op amps. Knowing how op amps evolved into the today's marvels is interesting, and it gives designers an insight into system problems that they encounter as they design in the low voltage world.

When power supplies were ± 15 V, the output voltage swing of an op amp didn't seem important. When the power supply was 30 V, the typical circuit designer could afford to sacrifice 3 V from each end of the output voltage swing (this was because of transistor

saturation or cutoff). The transistors in the op amp need enough voltage across them to operate correctly, so why worry about 6 V out of 30 V? Also, the input transistors required base bias, so an op amp with 30 V supplies often offered a common mode input voltage range of 24 V or less. These numbers come from the μA741 data sheet; the μA741 (about 1969) is the first internally compensated op amp to achieve wide popularity.

A later generation op amp, the LM324, had better dynamic range characteristics than the μA741. The LM324's output voltage swing is 26 V when operated from a 30 V power supply, and the common mode input voltage range is 28.5 V. The LM324 was big news because it was specified to operate with a 5 V power supply. The LM324's output voltage swing at $V_{CC} = 5$ V is 3.48 V, and this presented problems for the early low voltage circuit designers because the output voltage swing was smaller than most analog to digital converter (ADC) input voltage ranges. The ADC input voltage range must be filled to obtain its full dynamic range. The LM324 had an input voltage common mode range of ($V_{CC} - 1.5$ V) to 0 V; at least this op amp could work with transducers connected to the lower power supply rail if the transducer did not have an AC output voltage swing.

The next incremental improvement in op amps was the LM10, because it operated on 1.1 V power supplies. It was introduced almost as an afterthought, because there was no pressing demand for it. Its brilliant designer, Robert J. Widlar, wrote "IC op amps have reached a certain maturity in that there no longer seems to be a pressing demand for better performance." There were no pressing demands for a low voltage op amp in 1978 because portable (portable means battery applications, which are almost always single supply) did not become popular until the late 1980s or early 1990s.

Cell phones, calculators, and portable instruments—not new battery technology—opened the market for low voltage op amps; and when the portable concept caught on, the demand for low voltage op amps increased. The increasing demand did not breed new companies committed to low voltage IC design; rather, the established IC manufacturers threw a few low voltage op amps into their portfolio. These op amps, like the LM324, could operate on a low voltage, but they were severely lacking in input common mode voltage range and output voltage swing. Circuit designers had to be satisfied with this generation of op amps until something better came along. Well, something better is here now!

The next generation of low voltage op amps has much better specifications. The TLV278X operates off a power supply ranging from 1.8 V to 3.6 V and has an output voltage swing of 1.63 V (when the power supply is 1.8 V) coupled with an input

common mode voltage range of −0.2 V to 2 V. The TLV240X operates off a power supply ranging from 2.5 V to 16 V and has an output voltage swing of 2.53 V when the power supply voltage is 2.7 V. Also, when it is operated off a 2.7 V power supply, it has an input common mode voltage range of −0.1 V to 7.7 V. These new op amps are far superior to their predecessors when evaluated on their merits, which are extended output voltage swing and input common voltage range.

The latest op amps make it possible to design more accurate and cost effective electronic equipment, but there is one problem that they don't solve. Low voltage applications are defined here as single supply applications; and in single supply design, the op amp input voltage and output voltage are referenced to the midpoint of the power supply ($V_{CC}/2$). Unfortunately, most transducers are not connected to the midpoint of the power supply, because in the majority of cases, this requires a third wire beyond V_{CC} and ground. It doesn't help to create $V_{CC}/2$ at the transducer location (to save a wire) because it is not identical to the midpoint of the power supply (unresolved errors enter because of the reference voltage difference). When the transducer in a single supply design is referenced to any voltage other than the midpoint of the power supply, the reference voltage is amplified with the transducer voltage.

The trick to designing single supply op amp circuits is using external biasing to strip off or null out the reference voltage. Designing op amp circuits with biasing normally involves an iterative cut and try approach, where the designer assumes a circuit configuration, solves equations, changes the configuration, and repeats the process until a solution is found. A technique that solves the problem the first time is presented later.

24.2 Dynamic Range

It is extremely hard to define dynamic range (DR) for an op amp, so let's start with a digital to analog converter, where DR is defined as the ratio of the maximum output voltage to the smallest output voltage the DAC can produce (least significant bit, or LSB). Dynamic range is usually expressed in decibels using the formula given in Equation (24.1):

$$\mathrm{DR} = 20 \log_{10}\left(\frac{V_{\mathrm{OUT(MAX)}}}{V_{\mathrm{OUT(MIN)}}}\right) \tag{24.1}$$

The same definition of DR can be used for an op amp, and the maximum output voltage swing equals V_{OUTMAX}. This output voltage swing is defined as the maximum output voltage the op amp can achieve (V_{OH}) minus the minimum output voltage the op amp can achieve (V_{OL}). V_{OH} and V_{OL} are easily obtainable from an op amp IC data sheet. Normally, V_{OH} and V_{OL} are guaranteed minimum and maximum parameters respectively. This yields Equation (24.2):

$$V_{OUT(MAX)} = V_{OH(MIN)} - V_{OL(MAX)} \tag{24.2}$$

Equation (24.2) can be used to illustrate the role that power supply voltage plays in limiting the DR. $V_{OH(MIN)}$ is the most positive power supply voltage minus the voltage drop across the upper output transistor, therefore $V_{OH(MIN)}$ is directly proportional to the most positive power supply voltage. For any op amp, the output voltage swing is directly proportional to the power supply voltage, therefore, in the same op amp, the DR is directly proportional to the power supply voltage.

At first thought, one might think that the smallest output voltage that an op amp can have is zero, and the natural conclusion based on this assumption is that the DR is equal to infinity. This is never the case, because op amp and external circuit imperfections ensure that the smallest op amp output voltage is greater than zero. $V_{OUT(MIN)}$ is actually determined by a series of error terms. These error terms are the op amp's internal noise (V_n and I_n), external resistor noise (V_{nR}), power supply rejection ratio (k_{SVR}), voltage offset (V_{IO}), current offset (I_{IO}), common mode rejection ratio (CMRR), and closed loop gain (G). Each of these error terms is referred to the input of the op amp, so they must be multiplied by the closed loop gain to be referred to the output (see Figure 24.1).

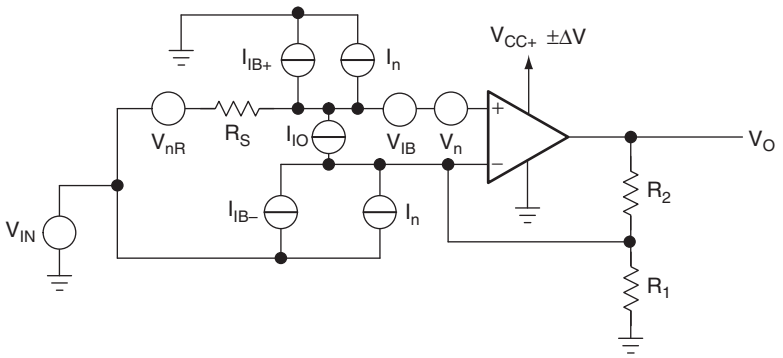


Figure 24.1: Op amp error sources.

The error sources are taken into account in Equation (24.3), and this equation refers them to the op amp output by multiplying them by the op amp's closed loop gain:

$$V_{OUT(MIN)} = G_{CL}\left(V_{IO} + I_{IO}R_S + \alpha V_{IO}\Delta + \frac{V_{IN} + I_{IB}R_P}{CMRR} + \frac{\Delta V}{k_{SVR}} + V_n + I_nR_{EQ} + I_{nR}R\right) \quad (24.3)$$

The maximum DR that can be achieved by an op amp is given in Equation (24.4):

$$DR = 20\log_{10}\left(\frac{V_{OH(MIN)} - V_{OH(MIN)}}{V_{OUT(MIN)}}\right) = 20\log_{10}\frac{V_{OUT(MAX)}}{V_{OUT(MIN)}} \quad (24.4)$$

The DR is reduced by the sum of the error terms, so it is proper to conclude that the maximum power supply voltage and the op amp choice (this defines the error magnitude) both establish the DR of an op amp. The first two terms in Equation (24.3) are DC error terms; therefore, they can be adjusted to zero by one of several methods, not mentioned here. The input offset current and input bias current error terms were big factors with older generation ICs, but today's technology render them much less significant (see Table 24.1).

Table 24.1: Comparison of Op Amp Error Terms

Parameter	LM324	TLV278X	TLV240X	Units
V_{IO}	9	1.5	4.5	mV
αV_{IO}	No spec	8	3	μV
I_{IB}	500,000	100	350	pA
I_{IO}	50,000	100	300	pA
CMMR	50	50	65	dB
k_{SVR}	65	70	100	dB
V_n	No spec	18 (1 kHz)	500 (100 Hz)	$nV/(Hz)^{1/2}$
I_n	No spec	0.9 (1 kHz)	8 (100 Hz)	$fA/(Hz)^{1/2}$

The data in Table 24.1 indicate that older low voltage op amps are not capable of yielding the DR of later technology op amps.

24.3 Signal to Noise Ratio

Noise sets a limit on the information and signals that can be handled by a system. The ability of an amplifier, receiver, or other device to discern a signal is degraded by noise. Noise mixed with the incoming signal, noise generated by the op amp, resistor noise, and power supply noise ultimately determine the size of the signal that can be recovered and measured.

Noise fluctuates randomly over a period of time, so instantaneous signal or noise levels don't describe the situation adequately. Averages over a long period of time (root mean squared, or rms) are used to describe both the signal and the noise. The signal to noise ratio (SNR) was initially established as a measure of the quality of the signal that exists in the presence of noise. This SNR was a power ratio, and it was established at the output of a circuit. The SNR we are interested in is a voltage ratio because the impedance is constant, and it is established at the input to the op amp. This means that all noise voltages, including resistor noise voltage, must be calculated in rms volts at the op amp input. The SNR is given in Equation (24.5):

$$\text{SNR} = 20 \log_{10}\left(\frac{V_{\text{SIGNAL}}}{V_{\text{NOISE}}}\right) \tag{24.5}$$

The signal is established by a transducer, a device that senses a change in a variable and converts that change into a voltage change. Transducers also convert some of their physical surroundings into a noise voltage that is combined with the signal. Noise from the physical surroundings of the transducer, unless its nature is well known, is almost impossible to separate from the transducer signal. When transducers are connected to the electronics, cabling picks up noise; and some transducers, like thermocouples, can pick up noise from the connecting junctions. Therefore, the signal is never clean as it enters the electronics. The noise generated by the op amp was defined in the previous section as V_n, I_nR_{EQ}, $I_{\text{nR}}R$, and $\Delta V/k_{\text{SVR}}$; and this noise is added to the signal.

The transducer often has a very small output voltage swing, so when the transducer output voltage swing is converted to least significant bits, the noise voltage should be very small compared to an LSB. Consider a temperature transducer that has a 10 mV swing over its range. When the transducer output voltage swing is considered to be

the full scale voltage (FSV) of an ADC, the LSB is very small, as is shown in Equation (24.6) for a 12 bit (N) ADC:

$$\text{LSB} = \frac{\text{FSV}}{2^N} = \frac{10\text{ mV}}{2^{12}} = \frac{10\text{ mV}}{4096} = 2.44\ \mu\text{V} \tag{24.6}$$

The op amp for this application must be a very low noise op amp, because an op amp with a 20 nV/(Hz)$^{1/2}$ equivalent input noise voltage and a bandwidth of 4 MHz contributes 40 μV of noise. This high noise contribution is why extensive filtering and "optimally" low bandwidth is found desirable in the input stages of some electronic systems. If there is power supply noise, some of that noise passes through the op amp to its input. The power supply noise is divided by the power supply rejection ratio, but there is always a residual noise component of the power supply on the op amp input, as shown in Equation (24.7), where k_{SVR} is 60 dB:

$$V_{\text{PS(INPUT)}} = \frac{V_{\text{PS}}}{\text{k}_{\text{SVR}}} = \frac{10\text{ mV}}{1000} = 10\ \mu\text{V} \tag{24.7}$$

24.4 Input Common Mode Range

Years ago the op amp's input common mode voltage range (V_{ICR}) did not include the power supply rails. The best V_{ICR} available was ($V_{\text{CC}} + |V_{\text{EE}}| - 6$ V); and when the input voltage approached V_{ICR}, distortion occurred. If the input voltage exceeded the power supply rails, the output stage might invert phase (it sometimes latched in the inverted position causing control problems) or the IC might self-destruct. The vast majority of transducers were connected to ground (0 V) because it was easy to make a ground connection and a split supply op amp has inputs referenced to ground. In a split supply application with the transducer connected to ground, latch-up or self-destruction is unlikely.

In special cases, transducers are connected to a power supply rail (usually V_{CC} when power supply current sensing) or some other voltage; and in this special case, additional bias circuitry is added to split power supply designs to keep the input voltage swing within V_{ICR}. Bias circuitry in conjunction with external components remove the effects of the power supply rail connection.

Many low voltage op amp input signals come from transducers connected to a power supply rail like the circuit shown in Figure 24.2.

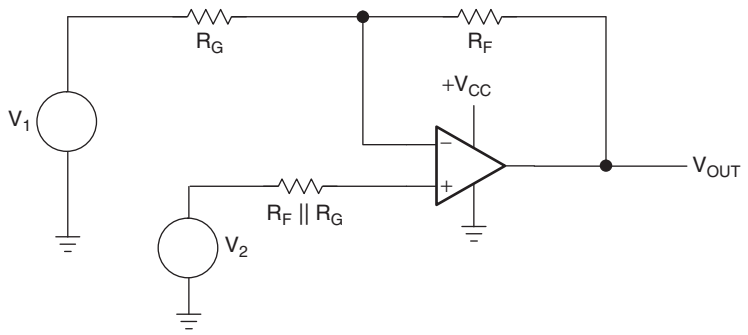


Figure 24.2: Noninverting op amp.

When $V_1 = 0$ and V_2 is the transducer input, the op amp must be capable of handling input voltages that go to 0 V. Furthermore, the transducer voltage may be AC, so it swings above and below ground, thus the transducer voltage drops below the low power supply rail. This situation requires that the op amp's V_{ICR} exceed the power supply voltage. Rail to rail input (RRI) voltage capability is a necessary requirement for a low voltage op amp that handles transducers connected to a power supply rail.

When the input voltage is connected to ground and the input voltage swing is very small, a standard op amp like the LM324 suffices. Referring to Figure 24.3, it can be seen that the pnp input transistors are biased by the emitter current source. If the

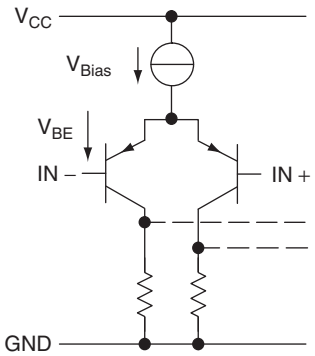


Figure 24.3: Input circuit of a non-RRI op amp.

positive input is connected to ground, bias current still flows and the transistor stays active. If the input transistors are selected very carefully for operation with low collector base junction reverse bias, the input voltage can go slightly below ground (−200 mV for the TLV278X) and the op amp still operates correctly. The circuit operation is one sided though, because when the input voltage approaches the positive supply rail, the emitter current source and input transistors turn off. This type of circuit does not offer rail to rail operation, but it does offer rail to (V_{CC} − 1.5 V) operation.

An op amp with an npn input stage works in a similar way around the positive supply rail. It can sense voltages close to V_{CC} and maybe slightly above V_{CC}, but it won't work when it is within 1.5 V of ground. The solution for this problem is to include parallel input circuits, as shown in Figure 24.4.

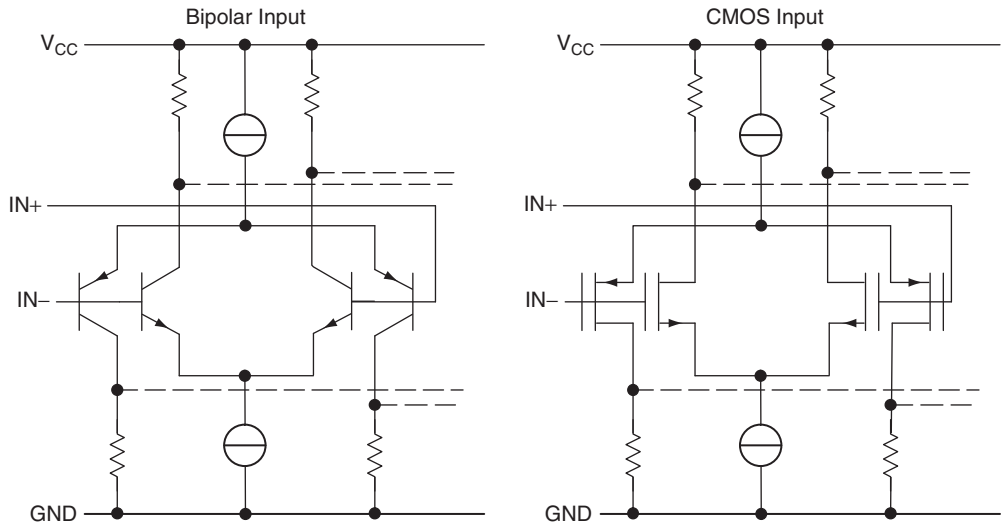


Figure 24.4: Input circuit of an RRI op amp.

The RRI op amps have parallel input stages. Both pnp and npn differential amplifiers are used in the input stages of the RRI op amp, so the RRI op amp can operate above and below the power supply voltage. As Figure 24.4 shows, the parallel input stages can be made in bipolar or MOS technology.

The input stages operate in three ranges. When the input voltage ranges from about −0.2 V to 1 V, the pnp differential amplifier is active and the npn differential amplifier is cut off. When the input voltage ranges from about 1 V to (V_{CC} − 1 V), both the npn and pnp differential amplifiers are active. When the input voltage ranges from about (V_{CC} − 1 V) to (V_{CC} + 0.2 V), the npn differential amplifier is active and the pnp differential amplifier is cut off. Inclusion of complementary differential input amplifiers achieves V_{ICR} exceeding the power supply limits, but there is a penalty to pay in input bias current, input offset voltage, and distortion. Figures 24.5 and 24.6 show the input bias current and input offset voltage as a function of the input common mode voltage.

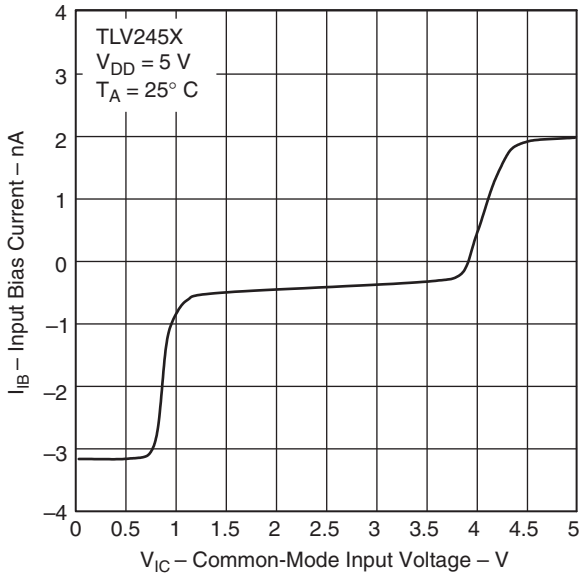


Figure 24.5: Input bias current changes with input common mode voltage.

When both transistors are conducting current, the input bias currents have a tendency to cancel; so in the range of ±1 V, the bias current is extremely low even when bipolar transistors are used to make the op amp. Above this range, the pnp differential amplifier cuts off, so the full bias current requirement of the npn transistor becomes

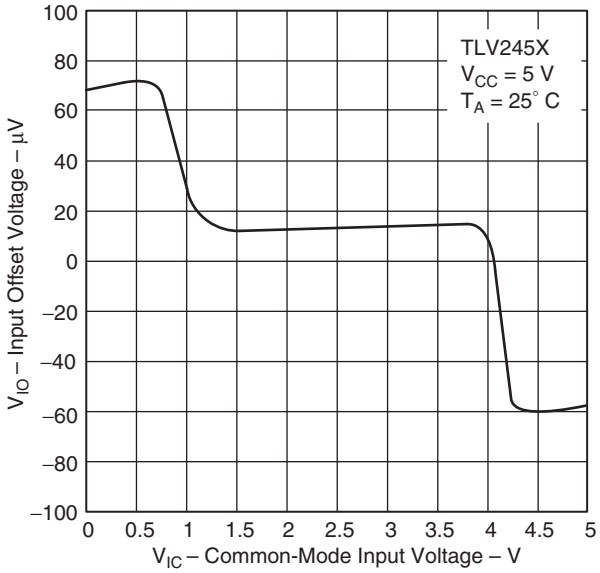


Figure 24.6: Input offset voltage changes with input common mode voltage.

apparent. The same action happens below this range when the npn differential amplifier cuts off. Note that the pnp bias current is significantly larger than the npn bias current; this is expected because npn transistors have better gain characteristics than pnp transistors. The base/emitter voltage of the npn and pnp transistors is well matched because the magnitude of the input offset voltage at the extremes is almost equal.

The bias current and offset voltage variation with input signal amplitude cause errors and distortion of the input signal. Inserting a resistance equal to the parallel combination of R_F and R_G into the positive op amp lead minimizes the effect of input bias current. The resistor R_P has the same voltage drop across as the parallel combination of R_F and R_G, hence the bias current is converted to a common mode voltage. The common mode voltage is normally in the microvolt range because I_{IB} is in the fractional nanoamp range and R_P is in the tens of kilo-ohms. The CMMR is approximately 60 dB, so the input bias current effect is reduced to the nanovolt range, where it is insignificant compared to the offset voltage. The input offset current is multiplied by R_P, and it shows up as an input error. If the design can't tolerate these errors, it is wise to switch to a CMOS op amp because its input currents are in the picoamp range.

Another type of error creeps in when complementary differential amplifiers are used to obtain DR, and this error results from the different gain of the pnp and npn transistors.

Op amps always suffer to a limited extent from distortion introduced by different gains when operating in different quadrants The positive quadrant is above $V_{CC}/2$ where npn transistors operate, and the negative quadrant is below $V_{CC}/2$ where the pnp transistors operate. Normally, this is a very minor effect because only the gain of the output stage changes with quadrant, but with complementary input stages, the input and output gains change with quadrant. These errors are small, and they are accepted as the sacrifice required for obtaining RRI operation.

24.5 Output Voltage Swing

The rail to rail output (RRO) voltage swing is desirable for at least two reasons. First, the DR can achieve the maximum obtainable value if the op amp is RRO. Second, RRO op amps can drive any converter connected to the same power supply if the impedance is compatible. The schematic of a RRO op amp output stage, part of the TLC227X, is shown in Figure 24.7.

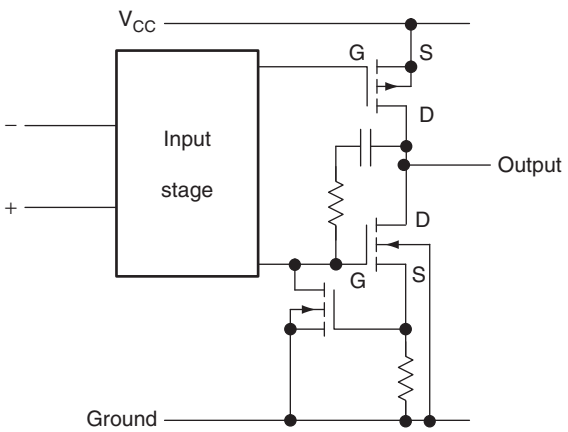


Figure 24.7: RRO output stage.

The RRO characteristic is achieved in the construction of the op amp output stage. A totem pole design that has upper and lower output transistors is used, and the output

transistors are a complementary pair. Each transistor in the pair is a "self-locking" type of transistor operating in the common source mode. Consider the p channel output transistor: As long as this transistor has a drain source resistance, it forms a voltage divider with the load resistance. When the load is a very large resistor or the output current flow is very small, the voltage drop across the output transistor can be neglected. Output current flows through the output transistor, and because current drops a voltage (V_{DS}) across the drain source resistor, the output voltage swing is reduced. The voltage drop subtracts from the power supply voltage, reducing the output voltage to less than RRO.

RRO op amps can't drive heavy loads and maintain their RRO capability because of the voltage dropped across the output transistors. Load resistance or output current is a test condition when the measurement of an op amp's output voltage swing is made. The size of the load resistor or output current is a measure of the op amp's ability to retain its RRO capability while sourcing or sinking an output current. When selecting a RRO op amp, the designer must consider the load resistance or output current required, because these conditions control the output voltage swing.

When an op amp is made that has RRI and RRO capability, it is called a *rail to rail input/output op amp*. This long name is shortened to *RRIO amp*.

24.6 Shutdown and Low Current Drain

Low voltage design often is accompanied by a requirement that the power supply current drain be low. The power supply current drain is kept low to decrease battery size and prolong battery charge, so recharging can be put off as long as possible. Many methods are employed to keep the current drain low, including using high value resistors, low bias current regulators/references, slow speed logic, keeping logic transitions to a minimum, low voltage power supplies, selecting op amps for low current drain, and shutting off unused capacitors.

High value resistors have less current flowing through them than low value resistors, and they can be used effectively in ratio applications, but there are some downsides to using high value resistors. When resistor values exceed 2 MΩ to 10 MΩ, depending on the type of resistor, the temperature drift, vibration, and time induced drift increase rapidly compared to that of lower value resistors. The input resistor to an op amp, R_G, works with the stray capacitance from the input node to ground to form a pole in the loop gain. As the resistance increases, the pole moves toward the zero frequency

intercept and the circuit overshoots, rings, or becomes unstable. The feedback resistor, R_F, works with stray capacitance in parallel with R_F to form a low pass filter. Sometimes this filter action is desirable, but the filter often distorts the signal.

Very often, low bias current regulators and references are just standard ICs specified at a lower current. These devices generally do not have the same small tolerances at low bias currents that they had at high bias currents. Although they are more often costly, redesigned low bias current regulators and references are becoming available. Ensure that the reference or regulator bias current used in the application is the same as that used to specify the device, because sometimes the error curves for references are nonlinear. Also, investigate the reference noise voltage to ensure that low bias current has not moved the device to a noisy portion of its operating curve.

Saturated logic is the choice for low current drain applications, because nonsaturated logic stays in the active region and has a higher current drain. Always pick the slowest logic gates that you can get away with. Speed in saturated logic requires enough current to drive low impedance loads, which means high power supply currents coupled with logic generated noise. High speed logic has a low impedance totem pole output stage; and every time the output is switched, both totem pole transistors are on, causing a current spike through the power supply. Large decoupling capacitors are required to localize the current spike at the logic IC, thus preventing noise propagation. CMOS logic draws the least quiescent current, and if the logic transitions are kept at a minimum, the current drain stays small. One method of minimizing logic transitions is to use asynchronous logic.

The op amp should be selected with current drain in mind. Three rail to rail op amps have widely differing current drains, because they are designed for different applications. The TLV240X is designed for micropower applications, and its current drain is 1.29 μA. The TLV411X is designed high output drive, and its current drain is 800 μA. The TLV278X is designed for high speed, and its current drain is 820 μA. All three are low voltage op amps, but each serves a different application.

The best method of conserving current is to shut down the op amp if you are not using it. Most op amps designed for low voltage applications have shutdown pins. A typical op amp that draws 820 μA when operating draws 1.7 μA when it is shut down. The problem with shutdown is the time that it takes to wake the op amp and knowing when to wake the op amp. A typical low voltage op amp turns on in less

than 1 μs, but the system designer usually has to choose the variable that eventually wakes the op amp.

24.7 Single Supply Circuit Design

The op amp is a linear device, so it follows the equation of a straight line. The equation of a straight line has four forms, as shown in Equation (24.8):

$$Y = \pm mx \pm b \tag{24.8}$$

These four forms can be implemented with four single supply circuits. When the designer discovers the form of Equation (24.8) that yields the transform function required, it is a small task to find the corresponding circuit. Once the circuit and transfer function are established, the task reduces to matching coefficients between the transfer function and the circuit equation then calculating the resistor values. The key required to unlock the puzzle is to determine the form of Equation (24.8) that yields the required transfer function. This key is found in simultaneous equations, because they define the equation of a straight line. Several examples of using simultaneous equations to determine the required form of the op amp transfer function are given in the next two sections.

24.8 Transducer to ADC Analog Interface

An example is a transducer that needs to be interfaced to an ADC. The transducer specifications are $V_{MIN} = 0.2$ V, $V_{MAX} = 0.5$ V, and $R_{OUT} = 600\ \Omega$. The ADC specifications are $V_{IN(LOW)} = 1.5$ V, $V_{IN(HIGH)} = 4.5$ V, and $R_{IN} = 20\ k\Omega$. The system specifies a 5 V power supply and 5% tolerance resistors. The transducer is connected to input of the amplifier (see Figure 24.8), so its output voltage swing is renamed V_{IN}; and the ADC is connected to the output of the amplifier, so its input voltage range is renamed V_{OUT}. Now, two data points are constructed as $V_{IN1} = 0.2$ V at $V_{OUT1} = 1.5$ V and $V_{IN2} = 0.5$ V at $V_{OUT2} = 4.5$ V. The data points are substituted into the equation $Y = mX + b$, where m is named the slope and b is named the X axis intercept or just the intercept for short. Don't worry about the sign of m or b because it is determined by the math, and it is substituted into the equation that determines the transfer equation. The simultaneous equations follow:

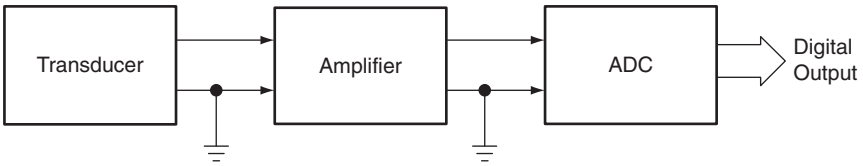


Figure 24.8: Data acquisition system.

$$1.5 = 0.2m + b \tag{24.9}$$

$$4.5 = 0.5m + b \tag{24.10}$$

From these equations we find that $b = -0.5$ and $m = 10$. The slope and intercept values are substituted into Equation (24.8) to get Equation (24.11):

$$Y = 10X - 0.5 \tag{24.11}$$

The mathematical terminology in Equation (24.11) is replaced by electronics terminology in Equation (24.12), and this is the transfer function required for the amplifier. The next step is to select the op amp, and this isn't a hard task, because many candidates could do the job with these undemanding specifications, so let us not dwell on the selection process. Assume that the selected op amp operates on a 5 V power supply, can drive the ADC input resistance of 20 kΩ with no voltage divider action, and its input impedance is so big that it doesn't load the transducer.

$$V_{OUT} = 10\ V_{IN} - 0.5 \tag{24.12}$$

The circuit that produces the desired transfer function is given in Figure 24.9.

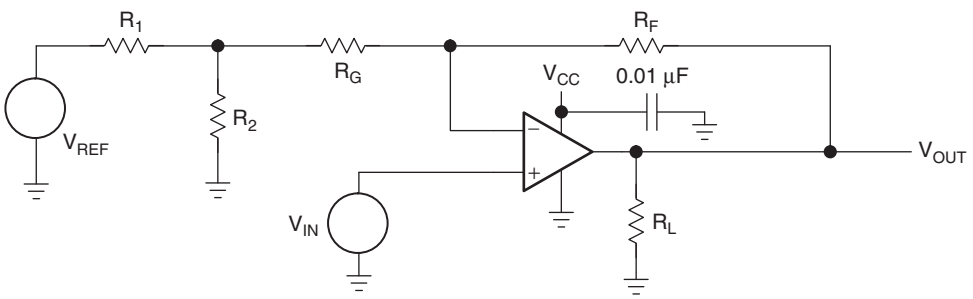


Figure 24.9: Schematic for the transducer to ADC interface circuit.

The circuit equation is obtained with the aid of superposition:

$$V_{\text{OUT}} = V_{\text{IN}}\left(\frac{R_F + R_G + R_1\|R_2}{R_G + R_1\|R_2}\right) - V_{\text{REF}}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1\|R_2}\right) \tag{24.13}$$

Comparing terms between Equations (24.12) and (24.13) enables the extraction of m and b:

$$m = \left(\frac{R_F + R_G + R_1\|R_2}{R_G + R_1\|R_2}\right) \tag{24.14}$$

$$|b| = V_{\text{REF}}\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_F}{R_G + R_1\|R_2}\right) \tag{24.15}$$

Making the assumption that $R_1\|R_2 \ll R_G$ simplifies the calculations:

$$m = 10 = \frac{R_F + R_G}{R_F} \tag{24.16}$$

$$R_F = 9R_G \tag{24.17}$$

Let $R_G = 20\ \text{k}\Omega$, then $R_F = 180\ \text{k}\Omega$, add, and let $V_{\text{REF}} = V_{\text{CC}}$:

$$|b| = V_{\text{CC}}\left(\frac{R_F}{R_G}\right)\left(\frac{R_2}{R_1 + R_2}\right) \tag{24.18}$$

$$R_1 = \frac{1 - 0.01111}{0.01111}R_2 = 89\ R_2 \tag{24.19}$$

Select $R_2 = 0.82\ \text{k}\Omega$ and $R_1 = 72.98\ \text{k}\Omega$. Since $72.98\ \text{k}\Omega$ is not a standard 5% resistor value, R_1 is selected as $75\ \text{k}\Omega$. The difference between the selected and calculated values of R_1 introduces about 3% error in the b coefficient, and this error shows up in the transfer function as an intercept rather than a slope error. The parallel resistance of R_1 and R_2 is approximately $0.82\ \text{k}\Omega$ and this is much less than R_G, which is $20\ \text{k}\Omega$; hence the earlier assumption that $R_1\|R_2 \ll R_G$ is justified. R_2 could have been selected as a smaller value, but the smaller values yielded poor standard 5% values for R_1. The final circuit is shown in Figure 24.10.

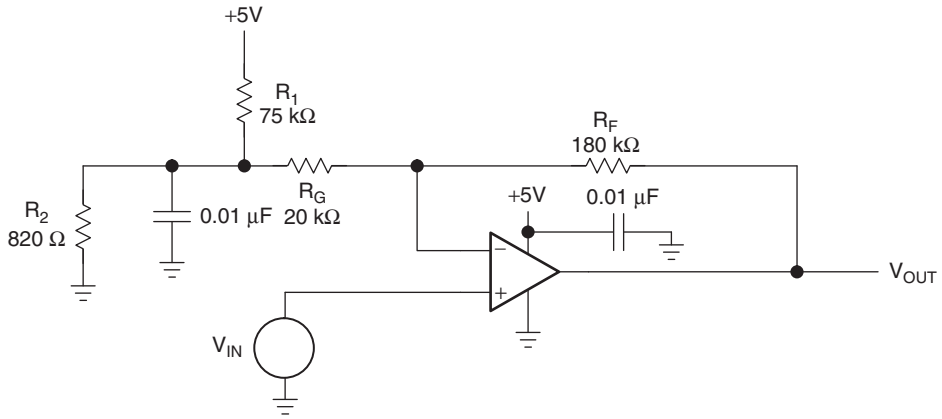


Figure 24.10: Final schematic for the transducer to ADC interface circuit.

24.9 DAC to Actuator Analog Interface

An amplifier is also used to interface a DAC with an actuator (see Figure 24.11).

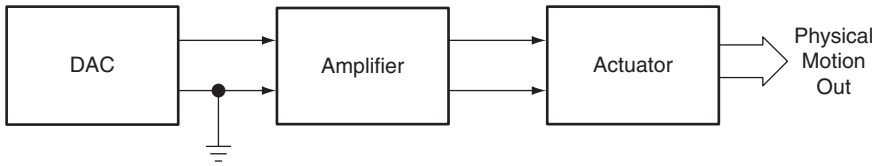


Figure 24.11: Digital control system.

The interface is different from the ADC interface because the DAC output signal is usually current rather than voltage. The first inclination is to stuff the DAC output into a current to voltage converter like we always did with split power supplies. This doesn't always work because the DAC current can be sinked or sourced from ground or the power supply. If a current sourced from the positive power supply is put into a standard current to voltage circuit, it wants to drive the op amp output negative, and a negative resistor is needed to counter this. The alternate solution for a sourced current from the positive power supply is to terminate the DAC output in a resistor that converts current into voltage, then level shift and amplify the terminated voltage. The circuit that performs this function is shown in Figure 24.12.

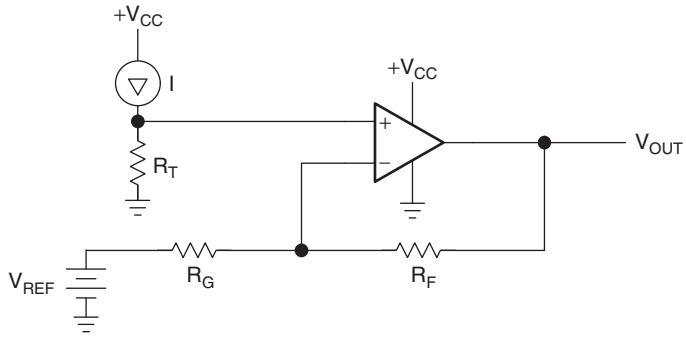


Figure 24.12: DAC current source to actuator interface circuit.

The DAC output current sources from $I_{OUT(ZEROS)} = 1$ mA to $I_{OUT(ONES)} = 2$ mA at an output compliance of 4.33 V. The actuator requires an input voltage swing of $V_{IN1} = 1$ V to $V_{IN2} = 4$ V to drive it, and its input resistance is 100 kΩ. The system specifications include one 5 V power supply and 5% resistors. The DAC is connected to the input of the amplifier (see Figure 24.11), so its output current swing is renamed I_{IN}; and the actuator is connected to the output of the amplifier, so its input voltage range is renamed V_{OUT}. Now, two data points are constructed as $I_{IN1} = 1$ mA at $V_{OUT1} = 1$ V and $I_{IN2} = 2$ mA at $V_{OUT2} = 4$ V. The data points are substituted into the Equation (24.20). Don't worry about the sign of m or b, because it is determined by the math; and it is substituted into the equation that determines the transfer equation. The simultaneous equations follow:

$$V_{OUT} = mI_{IN} + b \tag{24.20}$$

$$1 = m + b \tag{24.21}$$

$$4 = 2m + b \tag{24.22}$$

From these equations, we find that $b = -2$ and $m = 3$. The slope and intercept values are substituted into Equation (24.20) to get Equation (24.23):

$$V_{OUT} = 3I_{IN} - 2 \tag{24.23}$$

The equation for the circuit shown in Figure 24.12 is derived with the aid of superposition, and it is given in Equation (24.24):

$$V_{\text{OUT}} = I_{\text{IN}} R_T \left(1 + \frac{R_F}{R_G}\right) - V_{\text{REF}} \frac{R_F}{R_G} \tag{24.24}$$

Comparing terms between Equations (24.20) and (24.24) enables the extraction of m and b:

$$|b| = V_{\text{REF}} \frac{R_F}{R_G} \tag{24.25}$$

$$m = R_T \left(1 + \frac{R_F}{R_G}\right) \tag{24.26}$$

$$\frac{R_F}{R_G} = \frac{2}{5} \tag{24.27}$$

$$R_T = \frac{5\dfrac{R_F}{R_G} + 1}{\dfrac{R_F}{R_G} + 1} = 2.14 \tag{24.28}$$

These equations are written in terms of milliamps and kilo-ohms, so $R_T = 2.14\ \text{k}\Omega$. There is no $2.14\ \text{k}\Omega$ resistor in the 5% standard values; so, R_T is split into $1.8\ \text{k}\Omega$ and $0.33\ \text{k}\Omega$ resistors. R_G is selected as $51\ \text{k}\Omega$, so $R_F = 20\ \text{k}\Omega$. When $I_{\text{IN}} = 2\ \text{mA}$, $V_{\text{RT}} = 4.28\ \text{V}$, so the compliance of the DAC is not violated. You might find that standard DACs are not so generous with their compliance specifications.

When the current is sinked from the power supply by the DAC, its sign reverses and the previous circuit is not usable. Consider these specifications: The DAC output sinks current from the power supply $I_{\text{OUT(ZEROS)}} = -1\ \text{mA}$ to $I_{\text{OUT(ONES)}} = -2\ \text{mA}$ at an output compliance of 4.33 V. The actuator requires an input voltage swing of $V_{\text{IN1}} = 1\ \text{V}$ to $V_{\text{IN2}} = 4\ \text{V}$ to drive it, and its input resistance is $100\ \text{k}\Omega$. The system specifications include one 5 V power supply and 5% resistors. The DAC is connected to input of the amplifier (see Figure 24.11), so its output current swing is renamed I_{IN}; and the actuator is connected to the output of the amplifier, so its input voltage range is renamed V_{OUT}. Now, two data points are constructed as $I_{\text{IN1}} = -1\ \text{mA}$ at $V_{\text{OUT1}} = 1\ \text{V}$

and $I_{IN2} = -2$ mA at $V_{OUT2} = 4$ V. The data points are substituted into the Equation (24.20). Don't worry about the sign of m or b, because it is determined by the math; and it is substituted into the equation that determines the transfer equation. The transfer function for the current sink DAC is given in Equation (24.29):

$$V_{OUT} = I_{IN}m + b \tag{24.29}$$

The simultaneous equations follow:

$$1 = -m + b \tag{24.30}$$

$$4 = -2 + b \tag{24.31}$$

From these equations we find that $b = -2$ and $m = -3$. The slope and intercept values are substituted into Equation (24.28) to get Equation (24.32):

$$V_{OUT} = -I_{IN}(-m) - b = mI_{IN} - b \tag{24.32}$$

The current equation for the circuit shown in Figure 24.13 is given as Equation (24.33), and after algebraic manipulation it becomes Equation (24.34):

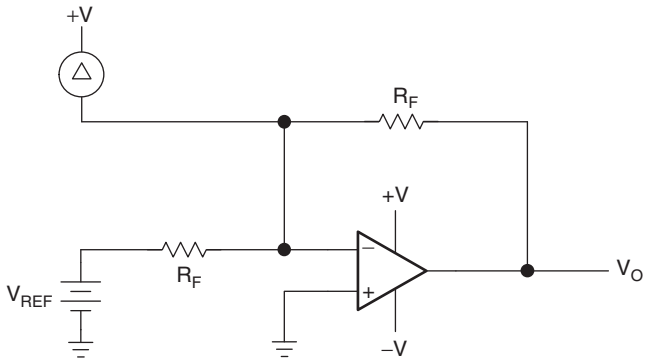


Figure 24.13: DAC current sink to actuator interface circuit.

$$\frac{V_{OUT}}{R_F} = I_{IN} - \frac{V_{REF}}{R_G} \tag{24.33}$$

$$V_{OUT} = I_{IN}R_F - V_{REF}\frac{R_F}{R_G} \tag{24.34}$$

Comparing terms between Equations (24.29) and (24.34) enables the extraction of m and b:

$$R_F = |m| = 3 \tag{24.35}$$

$$|b| = V_{REF}\frac{R_F}{R_G} \tag{24.36}$$

$$\frac{R_F}{R_G} = \frac{2}{5} \tag{24.37}$$

These equations are written in terms of milliamps and kilo-ohms. R_G is selected as 51 kΩ, so $R_F = 20$ kΩ. When $I_{IN} = 2$ mA, the compliance of the DAC is 0.0 V.

When DAC interface circuits are designed, two parameters that have not been considered in detail can control the design. The DAC has a compliance voltage requirement, and that requirement must be met regardless of the circuit demands. If the DAC compliance requirements are not met, the DAC saturates or is starved for current, and either of these situations introduces considerable error. The actuators driven in these examples are quite benign, because most actuators require considerably more current or voltage than is available from an op amp. This fact does not negate the analysis given here. Regardless of the actuator current or voltage requirements, the design procedure is similar. Very often, the low voltage device is plugged into a booster that supplies power to the actuator.

One last item to consider is the output capacitance of DACs. The DAC output can have large amounts of stray capacitance that show up as a capacitor across the op amp inverting input node when the DAC is interfaced into circuits, as shown in Figure 24.13. The DAC capacitance from the inverting node to ground acts with R_G to form a pole in the op amp loop gain. Adding a pole to the op amp loop gain leads to overshoot, then ringing, and finally oscillation. The effect that the DAC capacitance has on stability must be investigated. Also, the DAC output capacitance is a function of the digital number addressing the DAC. This capacitance can range from near zero to hundreds of picofarads, thus the op amp must be compensated for the worst case which is the largest capacitance.

Compensation schemes include connecting a capacitor across the feedback resistor. This compensation scheme is called a *compensated attenuator*; and if the RC time constants are equal, there will be excellent performance at that DAC output capacitance. Alas, the circuit can be ideally compensated at only one point, and this point is normally chosen as the highest DAC output capacitance. The remainder of the DAC range suffers from poor bandwidth because of overcompensation.

24.10 Comparison of Op Amps

Since the author is familiar with only Texas Instruments op amps, a comparison involving actual op amp parameters would be unfair to other op amp manufacturers. Also, any comparison using today's production op amps becomes invalid in a short period of time. I write about Texas Instruments op amps, so I get plenty of samples, and the new product introductions come so fast that I have a hard time keeping up with them. The other point to consider is that teaching how to make the op amp comparison is a much more powerful tool, therefore Table 24.2 containing the op amp parameters is established, and each of the parameters is discussed only in terms of low voltage design.

Table 24.2: Op Amp Parameters

Parameter	Range of values	Units	Discussion
V_{IO}	25 to 8000	mV	DC parameter that can be adjusted out
αV_{IO}	3 to 1000	µV/°C	Drift parameter that ends up as an error
I_{IB}	0.1 to 9999	pA	Input bias current that can be canceled out
I_{IO}	0.1 to 9999	pA	Input offset current that can be adjusted out
R_{IN}	0.0002 to 1	GΩ	Acts as a voltage divider with driving circuit
CMRR	0 to 90	dB	Common mode voltage is a nonlinear error.
A_{VD}	20 to 140	dB	Determines high frequency errors
V_{ICR}	V_{CC} −1.5 V to V_{CC} + 0.5 V	V	Input voltage range over which op amp works correctly with specified error
V_{OH}	V_{CC} −1.5 V to V_{CC} + 0.5 V	V	Maximum high output voltage swing. Load resistance or current is important. Limits dynamic range

(*Continued*)

Table 24.2: Op Amp Parameters (Cont'd)

Parameter	Range of values	Units	Discussion
V_{OL}	0 + 1.5 V to 0 − 1.5 V	V	Minimum low output voltage swing. Load resistance or current is important. Limits dynamic range
$_{IO}$	1 to 100	mA	Current available to drive loads
I_{CC}	0.1 to 10000	μA	Power supply current
k_{SVR}	20 to 120	dB	Power supply noise rejection
$I_{CC(SHDN)}$	0.01 to 100	μA	Power supply current in shutdown mode
V_n	1 to 1000	nV/(Hz)$^{1/2}$	Noise voltage limits dynamic range
I_n	0.01 to 100	fA/(Hz)$^{1/2}$	Noise current limits dynamic range
$t_{(ON)}$	0.5 to 10	μs	Op amp wakeup time
$t_{(OFF)}$	0.1 to 5	μs	Time until power supply current reaches $I_{CC(SHDN)}$

As the table shows, a lot of parameters must be considered in the selection of a low voltage op amp. The application weeds out some of these parameters, thus easing the selection process. If the application is measuring the output from a low bandwidth transducer, such as a thermocouple, bandwidth is not a parameter of interest, so speed can immediately be sacrificed for power supply current.

When the maximum supply voltage available is 3 V, rafts of op amps requiring more than 3 V operating voltage are eliminated. Taking this concept further, if dynamic range is an important specification in the 3 V design, those op amps that operate on 3 V without RRIO specifications can be eliminated. Because dynamic range is important, the noise voltage and current that detract from dynamic range are important parameters. If this 3 V application requires very low power supply current, the choice is narrowed down to a few candidates. The application selects the op amp, and if this application puts a few more requirements on the 3 V op amp, we may have to design a new IC.

Always start the selection process with the parameter that absolutely can't be wavered. The next parameter considered in the selection process should be the next most important parameter, and this process is continued parameter by parameter until all requirements are exhausted. Sometimes the supply of op amp candidates runs out before

the parameter requirements do. When you reach this point, it is time to renegotiate the design specifications, find a new op amp, negotiate with op amp manufacturers, or announce that you won't meet specifications. These designs are hard to work because the low power supply voltage requirement and the specifications usually leave very little room to work. As time marches on, more low power supply voltage op amps will come on the market, and these designs get easier to work.

24.11 Summary

It is extremely hard to achieve large dynamic range when the application is limited to a low power supply voltage. In an attempt to approach the dynamic range obtained by ± 30 V power supply designs, the new op amp designs put increased emphasis on the output voltage swing. The ratio of output voltage swing to power supply voltage was 0.8 for ± 30 V powered op amps, 0.7 for the first 5 V powered op amps, and has risen to 0.9 for the newest family of 1.8 V powered op amps. The ratio output voltage swing to power supply voltage has increased with each new generation of low power supply voltage op amps, but this improvement has reached the point of diminishing returns.

The op amp's DC offset diminishes the output voltage swing, but in most cases, the offsets are adjusted out, so they have less importance in the design. New op amp technology is not being pushed hard to improve in this area, because the passive components continue to require the adjustments. Drift and noise continue to decrease the dynamic range. Op amp noise has decreased in new generation op amps, and another decrease should put noise in the category of "don't care" parameters.

The signal to noise ratio has several components that have to be analyzed. The signal comes to the op amp with a noise burden caused by the transducer, cabling, and connections. Making the op amp a filter/amplifier combination eliminates some of this noise. The biggest drawback to making the op amp a filter is the time required to charge the ADC input capacitance. ADC charging has not been investigated here because of scope limitations, but suffice it to say that filters slow down op amps. The internally generated op amp noise is multiplied by the closed loop gain; and the SNR should be established in the front end, so the closed loop gain hurts one way and helps the other way. There is always system noise, and a portion of this noise propagates through the op amp into the signal. The system noise is minimized by extensive use of decoupling capacitors and a high power supply rejection ratio. In higher voltage systems, a resistor is placed in series with the power supply, making the decoupling capacitors more effective; low power supply voltage designs usually can't afford that trick.

RRI op amps are able to work with transducers connected to the power supply rails. As long as the AC component of the transducer output voltage does not exceed the input common mode range of the op amp, the design is reliable. RRI op amps are troubled by distortion introduced by the change in bias current, input offset voltage, and gain, but their contribution to the system's signal handling capability is invaluable. RRO op amps yield the highest output voltage swing of any series of op amps. Beware: RRO op amps are specified at a load resistance or current, and the output voltage swing decreases dramatically when the load resistance or current is increased. RRIO op amps contain the input and output features of RRI and RRO op amps. They also contain the drawbacks of both features.

Shutdown is a current saving feature that is becoming standard on RRIO op amps. When working off a battery, there is no reason to waste power when the electronics is not busy; and the shutdown feature accomplishes the power savings by turning the op amp off when it is not needed. The shutdown feature has a disadvantage in that it has a finite wakeup time for which the designer must allow. Don't just depend on shutdown to reduce current drain because there are other ways to reduce current drain, and some of these ways use high value resistors, low speed logic, fewer logic transitions, and low bias current regulators or references.

The final thing to be considered is that low power supply voltage invariably means single supply design, and single supply design is tougher than split supply design. Remember to get the two sets of data points, put them in simultaneous equations, solve for the slope and intercept, select the circuit configuration, and calculate the component values. DACs are a little different because you have to account for the polarity of the current, but their design generally follows the same procedure. A good reference for single supply design is the Texas Instruments application report *Single Supply Op Amp Design Techniques* (TI literature number SLOA030).

CHAPTER 25

Common Application Mistakes

25.1 Introduction

When one works as an analog applications engineer for many years supporting customer inquiries, some patterns begin to emerge. Inquires run the gamut from newcomers who have no business attempting analog design to those from analog design experts who encountered something new and unusual that challenges even the best support engineer. Unfortunately, there is also a class of inquiries that are bound to elicit a groan, mistakes the author has seen many times before and unfortunately will see many times again. It is hoped that this chapter will educate people to some of the most common mistakes and save designers from continuing to make them.

25.2 Op Amp Operated at Less than Unity (or Specified) Gain

Does the phrase *unity gain stable* ring a bell? In early chapters of this book, the statement was made that an op amp is least stable at its lowest specified gain. Ideally, the engineer has read the material and understands the true nature of stability, and yet, during the book tour for the first edition of this book, a customer approached me with a problem: This person had a programmable gain op amp circuit where resistors were switched to program a gain of 1, 1/10, and 1/100 (see Figure 25.1). The unity gain case worked as expected, but ringing occurred with a gain of 1/10 and sustained oscillation at a gain of 1/100. In no way do I demean the individual who made this mistake; I have been known to grab an amplifier out of a bin to construct a quick circuit, only to have it oscillate uncontrollably. Invariably, a quick glance at the data sheet reveals it is a "gain of ten" stable op amp not unity gain stable. There is no other option at that point but to use a different op amp.

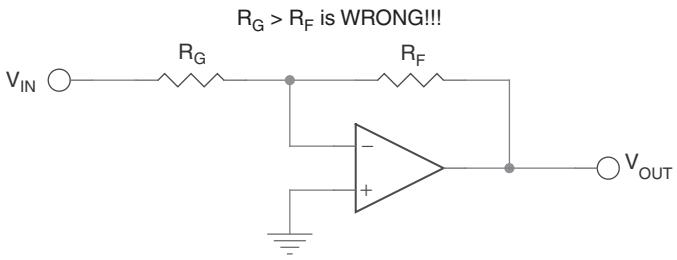


Figure 25.1: Op amp attenuator done wrong.

Fortunately, the solution to the problem is exceptionally easy. A voltage divider can be applied to the input of a noninverting op amp buffer, as shown in Figure 25.2.

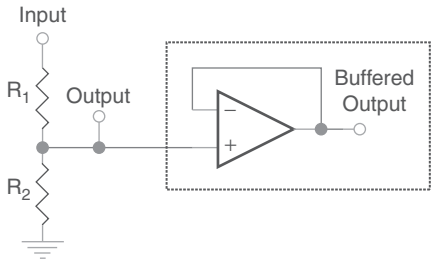


Figure 25.2: Op amp attenuator done correctly.

As far as the op amp is concerned, it is operating at unity gain and is stable. The voltage divider rule is employed to calculate the correct degree of attenuation. The high input impedance of the noninverting op amp input does not affect the voltage divider to any degree unless extremely large value resistors are used.

If the signal must be inverted, then the inverting attenuator of Figure 25.3 can be used. It is a variation on the approach used in Figure 25.2 but takes into account the resistors used for the op amp feedback and input resistance.

Texas Instruments has a calculator available on its Web site to assist in the calculation.

A common objection to the solution of Figure 25.2 is that it introduces resistor noise to the attenuator. This is a fallacy for two reasons—first of all, the incorrect inverting attenuator also contains resistors that are going to be almost the same value. The second reason is that the carbon composition resistors that caused the problem are

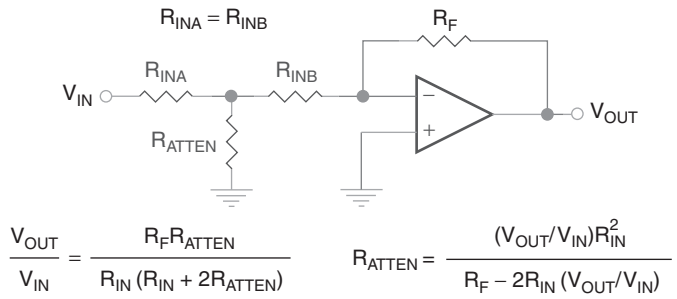


Figure 25.3: Inverting op amp attenuator.

a fast fading memory. Most resistors now are metal film or thick film types that have much better noise specifications.

25.3 Op Amp Used as a Comparator

This misapplication usually occurs in cost sensitive pieces of equipment when a comparator is needed and a quad op amp has an unused section. I first encountered it when I discovered that the expensive telephone answering machine I had purchased quit working. "Why?" I asked myself, "is there an open loop op amp circuit on one quarter of an LM324, and why is it interfaced to a digital logic gate?" The answer was that somebody looked at the schematic symbol of an op amp and the schematic symbol of a comparator (Figure 25.4), saw that they look alike, and decided that they both work the same way!

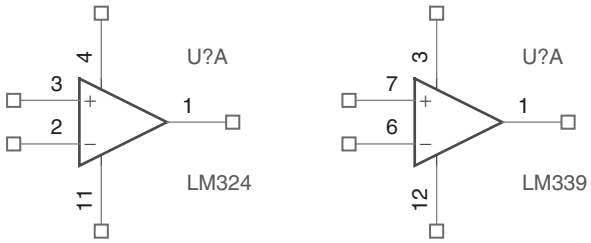


Figure 25.4: Similar schematic symbols, very different parts!

Unfortunately, not even the internal schematic of the parts give much indication of what is going on (see Figures 25.5 and 25.6).

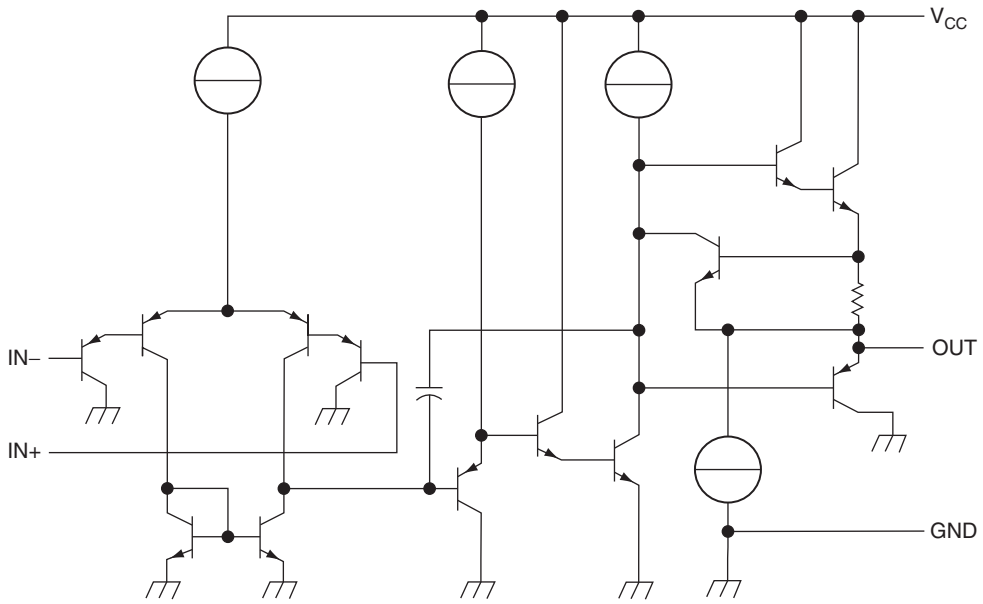


Figure 25.5: Example op amp schematic.

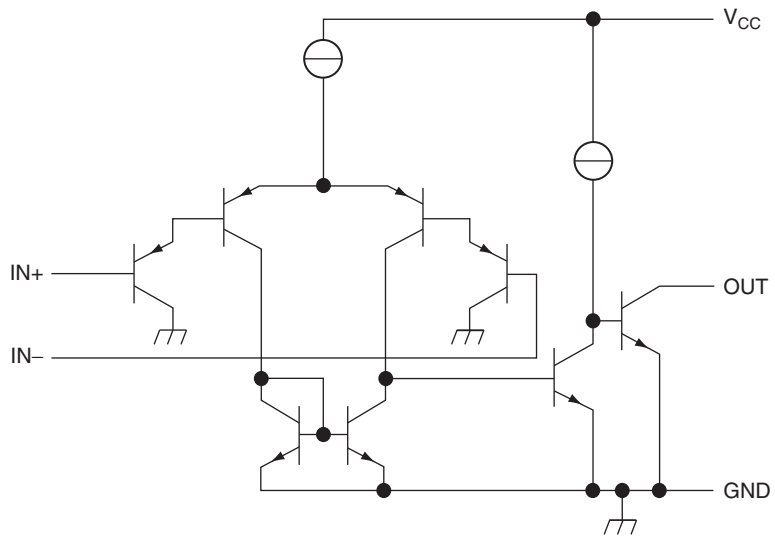


Figure 25.6: Example comparator schematic.

The input stages look almost identical, except the inputs have opposite labels (a fine point discussed later). The output stage of the op amp is a bit more complex, which should be a clue that something is different. The output stage of the comparator is obviously different, in that it is a single open collector. But be careful—many newer comparators have bipolar stages that are very similar in appearance to op amp output stages.

So, if very little appears to be different in the schematic symbol or the internal workings, what is the difference? The difference is in the output stage. An op amp has an output stage optimized for linear operation, while the output stage of a comparator is optimized for saturated operation.

25.3.1 The Comparator

A comparator is a 1 bit analog to digital converter. It has a differential analog input and a digital output. Very few designers make the mistake of using a comparator as an op amp, because most comparators have open collector output. The output transistor of open collector comparators is characterized by low V_{CE} for switching heavy loads. The open collector structure depends on external circuitry to make the connection to power and complete the circuit. Some comparators also bring out the emitter pin as well, relying on the designer to complete the circuit by making both collector and emitter connections. Other comparators substitute an FET, having open drain outputs instead of open collector. The emphasis is on driving heavy loads.

The comparator is an open loop device, utilizing no feedback resistors. When applying a comparator, the designer compares the voltage level at two inputs. The comparator produces a digital output that corresponds to the inputs:

- If the voltage on the noninverting (+) input is greater than the voltage on the inverting (–) input, the output of the comparator goes to low impedance "on" for open collector/drain outputs and "high" for totem pole outputs.
- If the voltage on the noninverting (+) input is less than the voltage on the inverting (–) input, the output of the comparator goes to high impedance "off" for open collector/drain outputs and "low" for totem pole outputs.

25.3.2 The Op Amp

An op amp is an analog component with a differential analog input and an analog output. If an op amp is operated open loop, the output seems to act like a comparator output, but is this a good thing to do?

An op amp, being intended for closed loop operation, is optimized for closed loop applications. The results are unpredictable when an op amp is used open loop. No semiconductor manufacturer can or will guarantee the operation of an op amp used in an open loop application. The analog output transistors used in op amps are designed for the output of analog waveforms and therefore have large linear regions. The transistors spend an inordinate amount of time in the linear region before saturation, making the rise and fall times lengthy.

In some cases, the designer may get away with using an op amp as a comparator. When an LM324 is operated in this fashion, it hits a rail and stays there, but nothing "bad" happens. The situation can change dramatically, however, when another device is substituted.

The design of an op amp output stage is bad news for the designer who needs a comparator with fast response time. The transistors used for op amp output stages are not switching transistors. They are linear devices, designed to output accurate representation of analog waveforms. When saturated, they not only may consume more power than expected, they may also latch up. Recovery time may be very unpredictable. One batch of devices may recover in microseconds, another batch in tens of milliseconds. Recovery time is not specified, because it cannot be tested. Depending on the device, it may not recover at all! Runaway destruction of the output transistors is a distinct possibility in some rail to rail devices. Even the best designer might produce a saturated or even open loop op amp circuit without realizing it.

Oh, why did my answering machine fail? The Vol rail of the open loop op amp circuit created was above the logic threshold of the digital gate to which it was interfaced. The two levels were very close—and the slightest drift upward of the op amp output stage caused the low logic threshold to never be reached. Vol is yet another op amp specification that will never be specified under open loop conditions.

25.4 Improper Termination of Unused Sections

One of the easiest ways to unintentionally misapply an op amp is to misapply unused sections of a multiple section IC. Figure 25.7 shows the most common ways designers connect unused sections.

Many designers know how to properly terminate unused digital inputs, hooking them to the supply or ground. These designers may not have a clue how to terminate unused op amps. Figure 25.7 demonstrates techniques of Texas Instruments applications actually seen. I gave them titles:

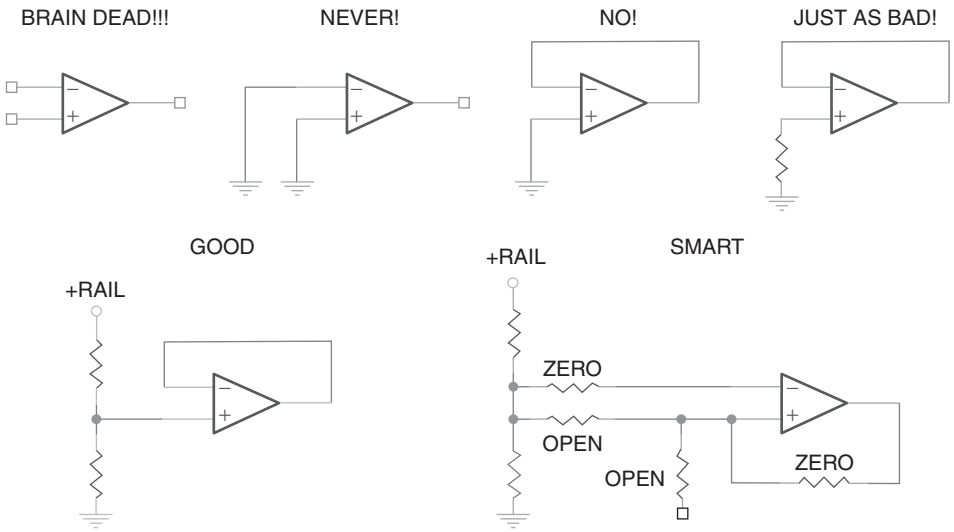


Figure 25.7: Different ways of dealing with unused op amp sections.

- **Brain dead.** This is a common mistake. Designers will assume an op amp is like an audio amp at home and just leave unused inputs unconnected. This is the absolute *worst* thing that can be done to an op amp. An open loop op amp saturates to one voltage rail or the other. Because the inputs are floating—and picking up noise—the output of the op amp switches from rail to rail, sometimes at unpredictable high frequencies.
- **Never.** This is another really bad thing that designers occasionally do. Usually, one op amp input is slightly higher than the other due to ground plane gradients, and the best possible scenario is that the op amp will saturate at one rail or the other. There is no guarantee it will stay there, as a slight change on one pin could cause it to switch to the other rail.
- **No.** This is a little better than the previous case but not that much. All the designer has accomplished is to ensure that the op amp will hit a rail—and stay there. This can wreak havoc—self-heating, increased power consumption.
- **Just as bad.** Designers who are designing a board for in circuit test commonly do this. It still makes the op amp hit a rail.
- **Good.** This is the minimum recommended circuit configuration. The noninverting input is tied to a potential between the positive and negative rail

or to ground in a split supply system. Virtual ground may already exist in the system, making the resistors unnecessary. The op amp output also is at virtual ground (or ground in a split supply system).

- **Smart.** The smart designer anticipates the possibility of system changes in the future and lays out the board so that the unused op amp section could be used by changing resistors and jumpering. The schematic shows how the unused section could be used for either an inverting or noninverting stage, as required.

25.5 DC Gain

Another way designers create problems is when they forget about DC components on AC signals. Figure 25.8 illustrates this problem. When an AC signal source has a DC offset, a coupling capacitor isolates the potential in the top circuit. The DC component is rejected, and output voltage is 1 VAC. If the coupling capacitor is omitted, the circuit attempts a gain of –10 on both the AC and DC components, which would be 1 VAC, –50 VDC. Because the power supply of the circuit limits the DC output to ±15 VDC, the output will be saturated at –15 VDC (minus the voltage rail limitation of the op amp).

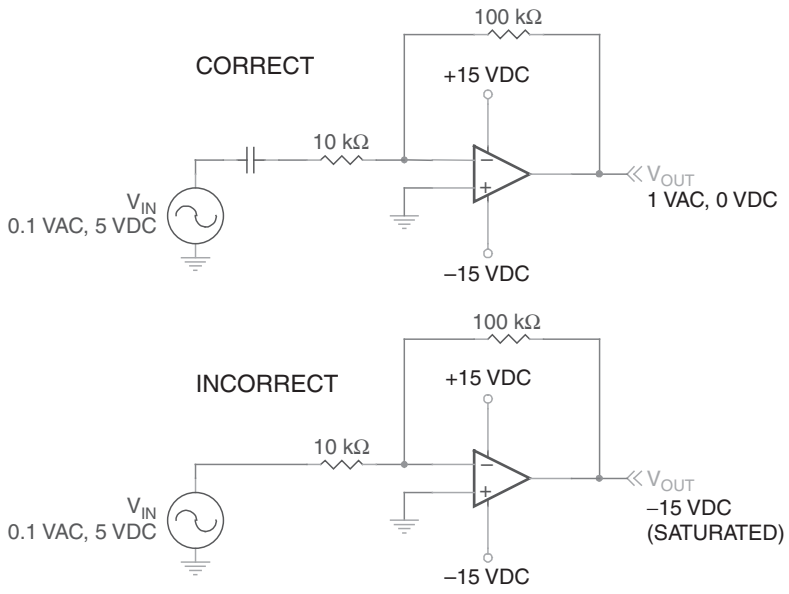


Figure 25.8: Unexpected DC gain.

25.6 Current Source

The op amp current source circuit shown in Figure 25.9 *must* always contain the load. Many applications put the load at the end of a cable, and the cable is on a connector. When the cable is unplugged, the op amp has positive feedback! It will hit the negative voltage rail.

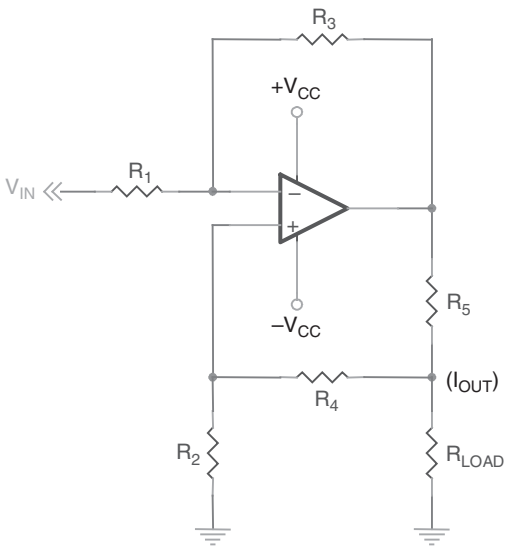


Figure 25.9: Current source.

The output of the current source is

$$I_{\text{OUT}} = \frac{R_3 \times V_{\text{IN}}}{R_1 \times R_5}$$

$$R_3 = R_4 + R_5$$

$$R_1 = R_2$$

It should be understood that R_1 through R_4 are much greater than R_5, and $R_5 \gg R_{\text{LOAD}}$.

25.7 Current Feedback Amplifier: Shorted Feedback Resistor

By far the most common mistake with current feedback amplifiers occurs when a designer shorts the output directly to the inverting input, as in Figure 25.10.

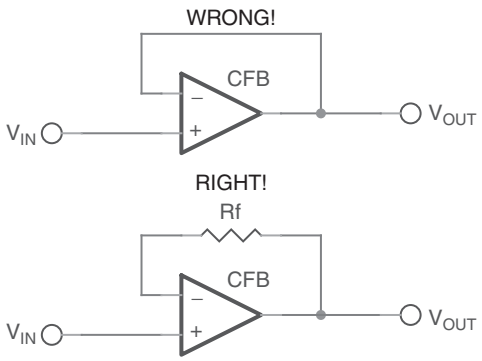


Figure 25.10: Current source with shorted output.

The designer is invariably trying to take advantage of the speed and bandwidth of the CFB to create a buffer. Shorting the output pin to the inverting input is always a bad idea, because it makes the CFB unstable. Stability criteria for the current feedback amplifier are different from that of the voltage feedback amplifier. The voltage feedback amplifier stability criterion is

$$A\beta = \frac{aR_G}{R_F + R_G}$$

The current feedback amplifier stability criterion is

$$A\beta = \frac{Z}{R_F\left(1 + \frac{Z_B}{R_F \| R_G}\right)}$$

As you can see, VFB stability depends equally on both R_F and R_G. But CFB stability is much more dependent on R_F. In fact, if R_F is zero, the denominator goes to zero

and the stability criterion fails! This is seen graphically in actual data sheet plots (Figure 25.11).

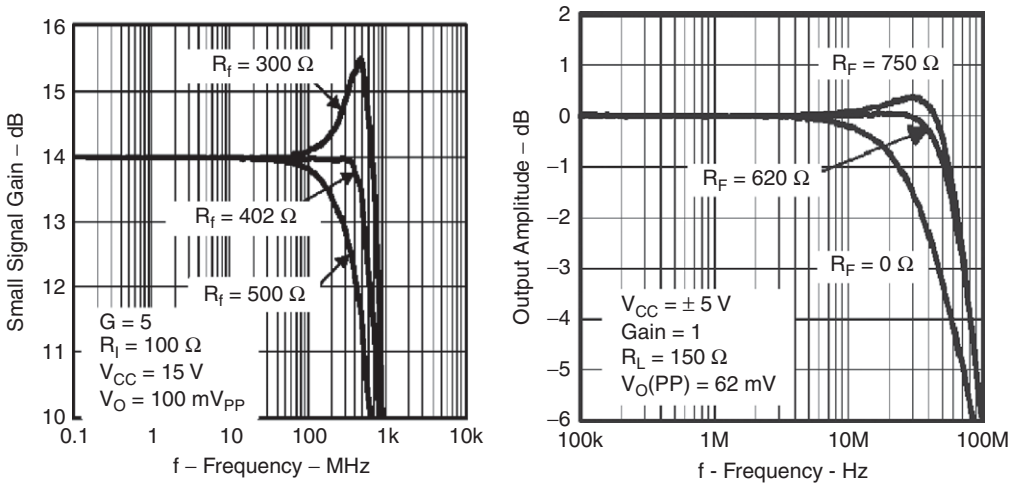


Figure 25.11: VFB versus CFB stability versus load resistor.

The effect of changing R_F only slightly has an enormous effect on the CFB response on the left, with an alarming trend as the resistor is lowered. The effect is much smaller and opposite with the VFB plot on the right. The bottom line is this: Stick with the recommended value of feedback resistor for CFB op amps. That also makes a very easy solution when a noninverting buffer is desired. Just put the recommended value of feedback resistor between the output and inverting input, and the stage will work perfectly!

25.8 Current Feedback Amplifier: Capacitor in the Feedback Loop

A capacitor often ends up in the feedback loop when the designer is attempting to do active filter design with CFAs (Figure 25.12).

Very few filter topologies work with CFAs. The Sallen-Key is one—if the proper value of feedback resistor is employed. The bottom line is that CFAs are not the best choice for active filter designs. Choose something else wherever possible.

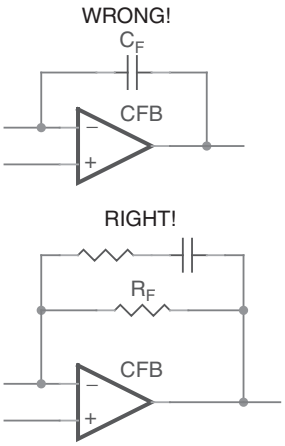


Figure 25.12: Capacitor in the feedback loop.

25.9 Fully Differential Amplifier: Incorrect Single Ended Termination

One of the most common applications for a fully differential op amp is single ended to fully differential conversion. However, when the input signal must be terminated, the situation gets very complicated!

Looking at the circuit in Figure 25.13 and the equations that govern it, R_1 and R_t are cross defined. Solving this equation for the correct values requires a goal seeking algorithm. If the values are calculated incorrectly, the results can be

- Wrong gain.
- Differential offset.
- Unmatched differential gain.
- Incorrect matching impedance.

Fortunately for the designer, Texas Instruments provides a calculator on its Web site to do this task automatically.

The designer might want to consider the simpler design alternative in Figure 25.14.

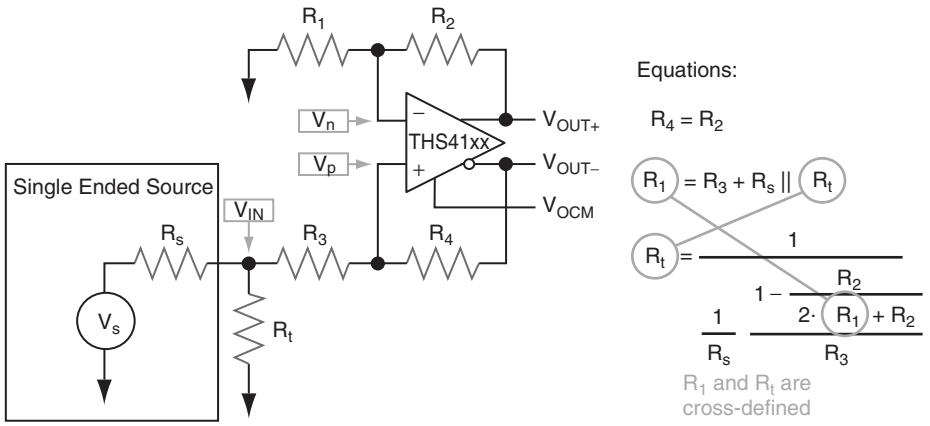


Figure 25.13: Terminating a fully differential amplifier.

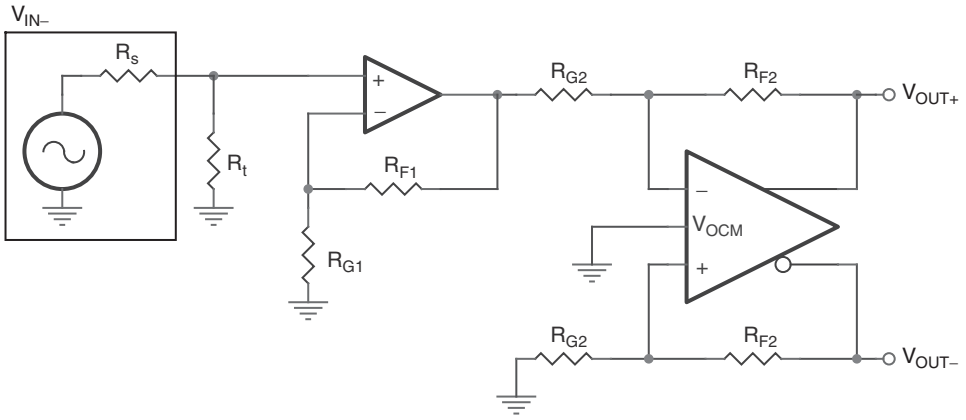


Figure 25.14: Using an input stage.

25.10 Fully Differential Amplifier: Incorrect DC Operating Point

Single supply operation of a fully differential amplifier is very easy to mess up (just see Figure 25.15).

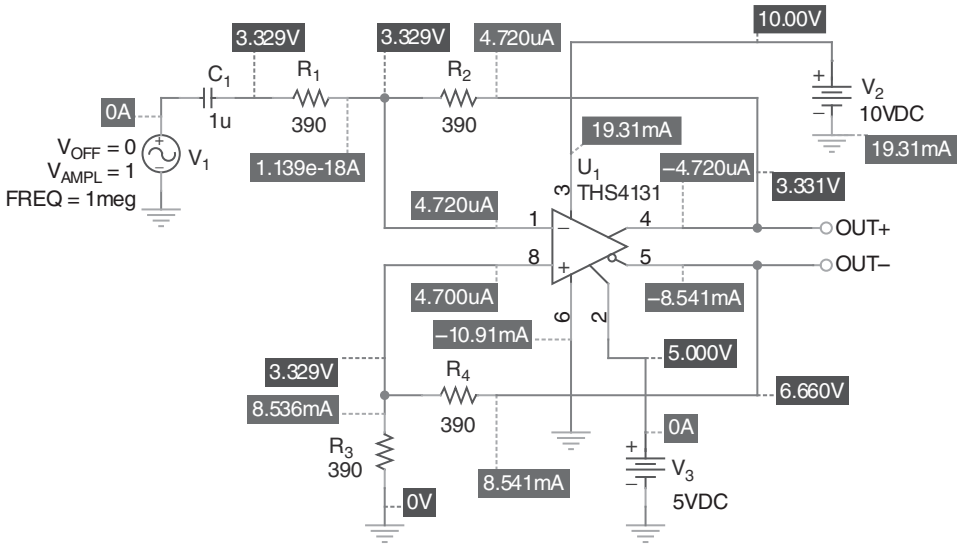


Figure 25.15: Incorrect DC operating point.

What happened? The two outputs have a 3.3 VDC difference between their operating points! Remember that differential input circuits have two potential sources of DC. In this case, the designer correctly put an AC coupling capacitor between V_1 and R_1 but forgot to put one between R_3 and ground. Figure 25.16 shows what happens when the second AC coupling capacitor is installed.

When the second AC coupling capacitor is inserted, the correct DC operating point is established.

25.11 Fully Differential Amplifier: Incorrect Common Mode Range

A very subtle but equally destructive problem often arises from incorrect application of the V_{OCM} input of the fully differential amplifier when the amplifier frequency response has to include DC, making AC coupling capacitors impossible. Consider the circuit in Figure 25.17.

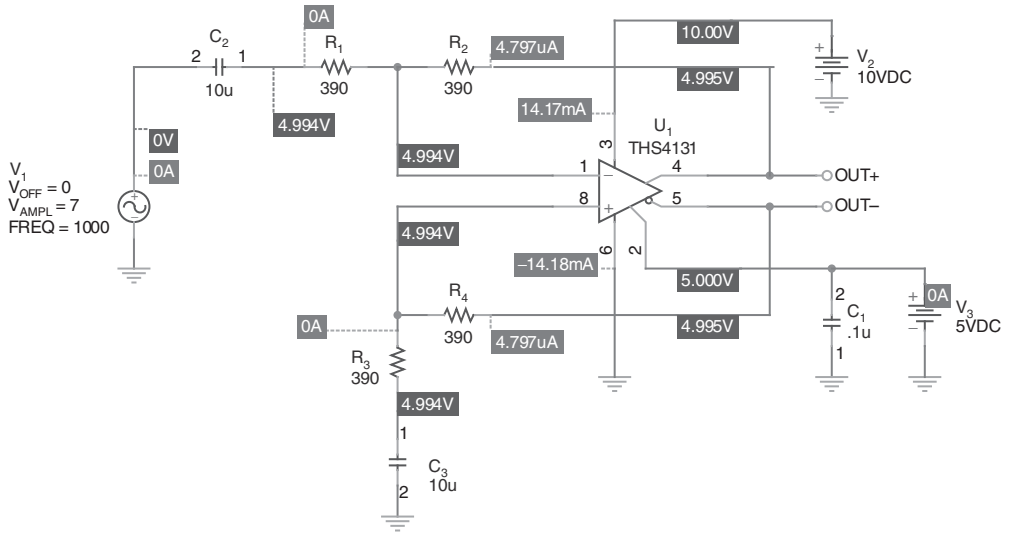


Figure 25.16: Correct DC operating point.

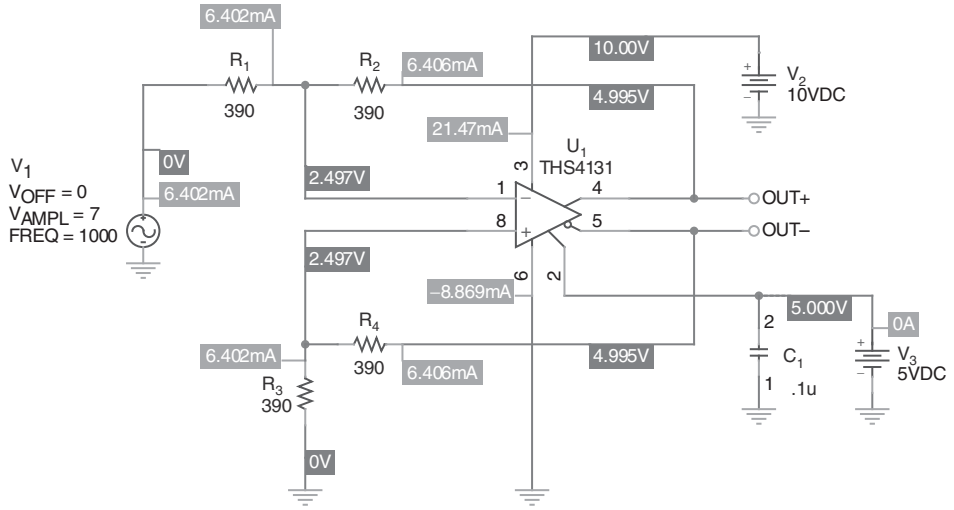


Figure 25.17: Common mode error.

The DC operating point appears to be correctly established, the outputs will swing around the V_{OCM} common mode point, which is established at 5 V by V_3. But, when an AC simulation is done, the results are terrible. What happened?

The problem comes when the input voltage range does not include the negative rail, in this case, ground. There are two solutions for the problem. One is to offset the inputs to the same DC level as V_{OCM}. The other is to choose a fully differential amplifier that includes the negative rail in its common mode range. Figure 25.18 illustrates the effect of V_{OCM} on the output signals.

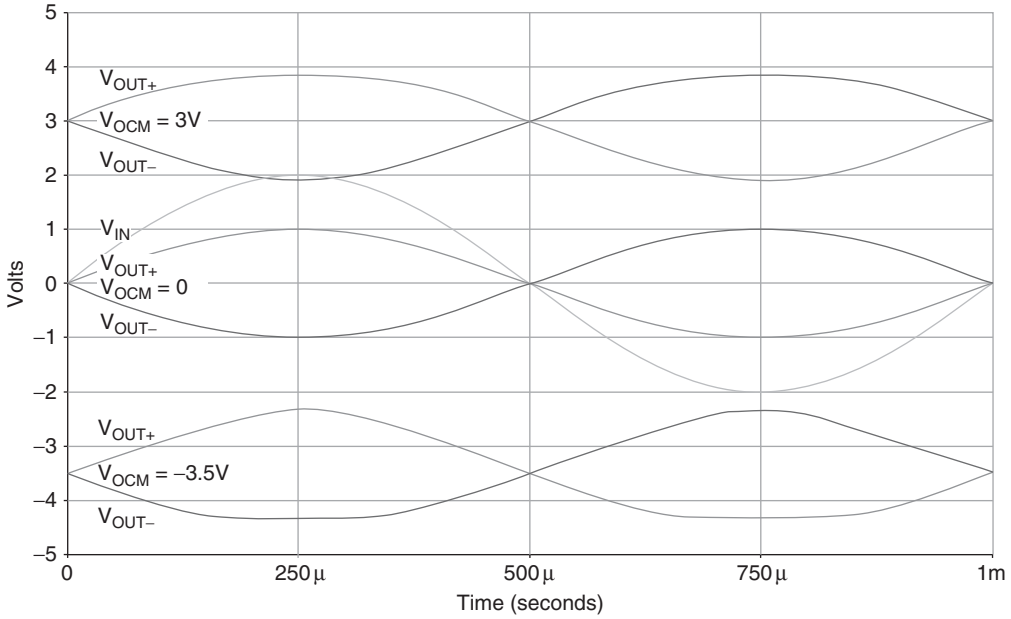


Figure 25.18: The effects of V_{OCM} on outputs.

V_{OCM} causes problems when it forces the outputs of the amplifier too close to the power supply rails. It is best to operate both inputs and V_{OCM} as close as possible to the same DC potential.

25.12 The Number 1 Design Mistake

I saved the very best and most common mistake for last. And it doesn't even involve an op amp. It involves support components: the decoupling capacitors!

In Chapter 1, I mentioned some part numbers that are etched in the memory of every design engineer, at least those involved in analog design. There is one other: 0.1 μF.

Need to decouple? OK, everybody knows you put a 0.1 μF capacitor on every power supply input and the job is done, right? I can disprove that truism very easily with two words: cell phone.

Put your cell phone near your prototype circuit, which is bypassed with 0.1 μF, and make a call while monitoring the output on a high bandwidth oscilloscope. You will see horrendous 2.4 GHz leakage!

An alternative version of this problem came from some cellular telephone base station installers who called in a panic, "We have 90 MHz noise running all over our system—and can't figure out where it is coming from." A suspicion on my part asked them to tell me the exact coordinates where they were installing the system, and they provided the exact latitude and longitude. A quick check of the FCC database revealed the problem. I asked them, "Are you anywhere near the tower for W____ 90.5 FM, a 100,000 W NPR station listed at those coordinates?" They told me on the phone that they could see the transmitter 5 ft away—they were colocating with the station!

The point of this is that their board was bypassed with 0.1 μF capacitors. While that worked fine for the digital portions of the board, the analog portions were being clobbered by radiation of the powerful 90.5 MHz FM station. Conventional thinking is that the lower the value of capacitance, the lower the frequencies it will filter. So, 0.1uF should get rid of just about everything because it is a very large value (relatively speaking). This conventional wisdom is wrong! The actual case is the exact opposite.

Where did the value 0.1 μF come from, anyway? A high technology store near me used to have antiquated computer boards as a wall decoration. Backlit with white light, the translucent green boards made a pretty sight. But, they were also populated with 0.1 μF decoupling capacitors. A quick survey of the circuitry revealed that the clock rate of the old computer had been 1 MHz.

So, the 0.1 μF capacitor value seems to have come from bypassing TTL logic in the 1960s! Isn't it time to rethink the issue a bit, in light of op amps and other analog components that can operate to frequencies of 3 GHz, especially when almost every engineer carries a 2 W, 2.4 GHz transmitter into the lab (cell phone)?

The reality of the situation is that a good 0.1 μF capacitor with an X7R dielectric exhibits a resonance in the 10 MHz region. This is due to parasitic inductance creating an LC circuit. Below 10 MHz, its impedance is capacitive, decreasing almost linearly on a logarithmic plot until it reaches the resonant frequency. Above the resonant frequency, the impedance is inductive. Since inductor resists the flow of high frequencies and passes only low frequencies, the decoupling capacitor is useless above its resonant frequency.

Looking at representative plots from capacitor manufacturers, at 100 MHz, the venerable 0.1 μF bypass capacitor has become an inductor with an XL of at least 1 Ω. By 2.4 GHz, XL has risen to above 10 Ω.

A good rule of thumb for effective bypassing is to put several capacitors in parallel. The standard 0.1 μF capacitor does quite nicely for frequencies up to 10 MHz, a 1000 pF NPO dielectric does nicely up to 100 MHz, and 33 pF NPO eliminates frequencies in the 2.4 GHz region. Bulk decoupling of the power supply as it enters the board eliminates low frequency ripple.

Here is a truism to replace the older one: When poor decoupling is suspected, decrease (do not increase) the value of the capacitance.

APPENDIX A

Single Supply Circuit Collection

Bruce Carter

A.1 Introduction

This chapter is devoted to a collection of single supply op amp circuits. These are presented here because they are somewhat unusual and do not fit well into the material presented in the main portion of the book.

A.2 Instrumentation Amplifier

In the circuit configuration in Figure A.1, both sources connect to the noninverting input of two op amps. This impedance is very high, and if the op amps are identical, both impedances are very nearly equal. This is ideal for interfacing to very high impedance input signals. The propagation delay is equal to two op amp propagation delays, but the propagation delay is very nearly equal, so any distortion resulting from unequal propagation delays is minimized.

When $R_7 = R_6$, $R_5 = R_2$, $R_1 = R_4$, and $V_{REF1} = V_{REF2}$, Equation (A.1) reduces to Equation (A.2):

$$V_{OUT} = (V_{IN2} + V_{REF2})\left(\frac{2R_4 + R_3}{R_3}\right)\left(\frac{R_7}{R_5 + R_7}\right)\left(\frac{R_6 + R_2}{R_2}\right) - (V_{IN1} + V_{REF1})\left(\frac{2R_1 + R_3}{R_3}\right)\frac{R_6}{R_2} + V_{REF3}\left(\frac{R_5}{R_5 + R_7}\right)\left(\frac{R_6 + R_2}{R_2}\right) \tag{A.1}$$

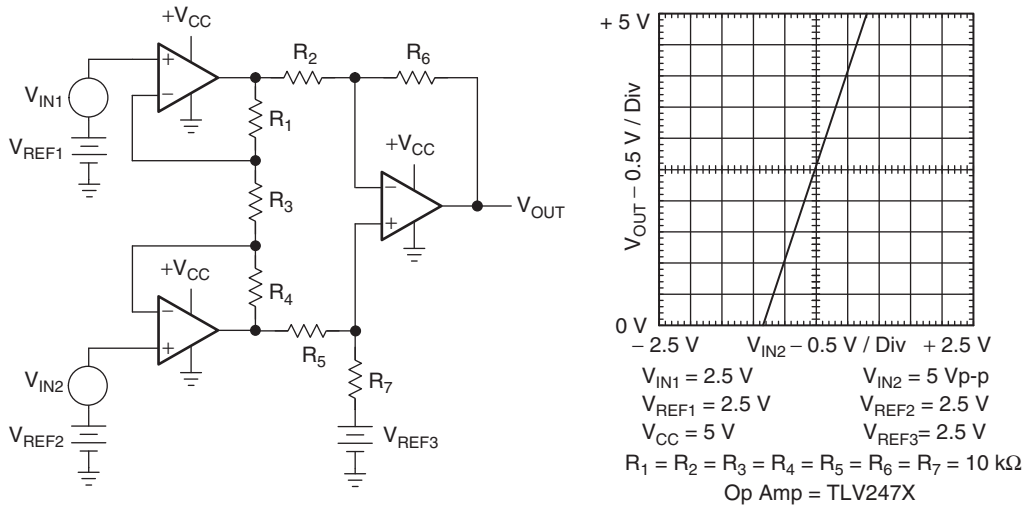


Figure A.1: High precision differential amplifier.

$$V_{OUT} = (V_{IN2} - V_{IN1})\left(\frac{2R_1}{R_3} + 1\right)\left(\frac{R_6}{R_2}\right) + V_{REF3} \qquad (A.2)$$

The equal resistors should be matched with more precision than is expected from the circuit. Resistor matching eliminates distortion due to unequal gains, and it reduces the common mode voltage feed through. Resistors equal to $(R_1 \| R_3)/2$ may be placed in series with the sources to reduce errors resulting from bias currents. This differential amplifier has the unique feature that the gain can be changed with only one resistor, and if the gain setting resistor is R_3, no resistor matching is required to change gain.

A.3 Simplified Instrumentation Amplifier

As shown in Figure A.2, both input sources are loaded equally with very high impedances in the simplified instrumentation amplifier. This configuration eliminates three resistors, two of which are matched, but it sacrifices flexibility in gain setting capability because the gain must be set with a matched pair of resistors.

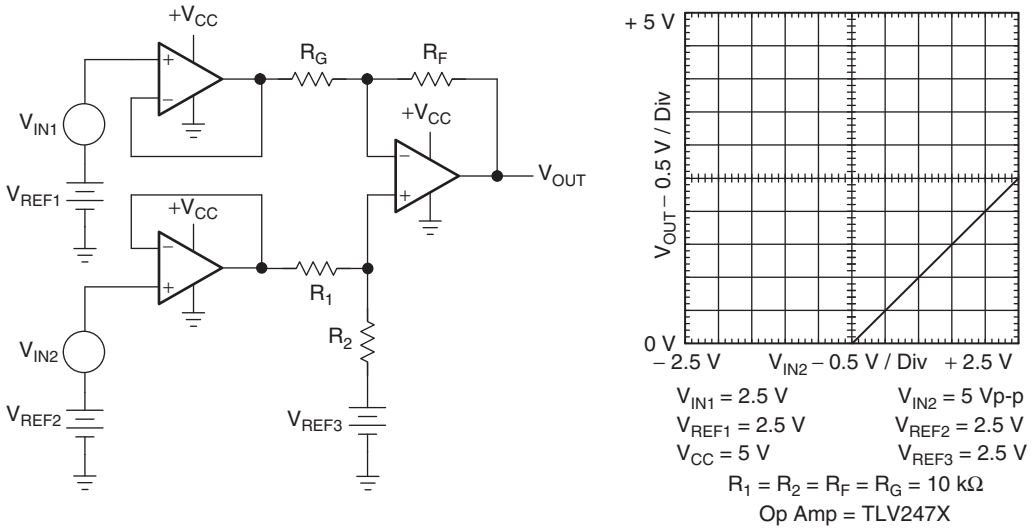


Figure A.2: Simplified high precision differential amplifier.

When R_F is set equal to R_2, R_G is set equal to R_1, and $V_{REF1} = V_{REF2}$, Equation (A.3) reduces to Equation (A.4):

$$V_{OUT} = (V_{IN2} + V_{REF2})\left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_2}{R_1 + R_2}\right) - (V_{IN1} + V_{REF1})\left(\frac{R_F}{R_G}\right) + V_{REF3}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{R_F + R_G}{R_G}\right) \tag{A.3}$$

$$V_{OUT} = (V_{IN2} - V_{IN1})\left(\frac{R_F}{R_G}\right) + V_{REF3} \tag{A.4}$$

A.4 T Network in the Feedback Loop

Sometimes, it is desirable to have a low resistance path to ground in the feedback loop. Standard inverting op amps cannot do this when the driving circuit sets the input resistor value and the gain specification sets the feedback resistor value. Inserting a

T network in the feedback loop (Figure A.3) yields a degree of freedom that enables both specifications to be met with a low DC resistance path to ground in the feedback loop:

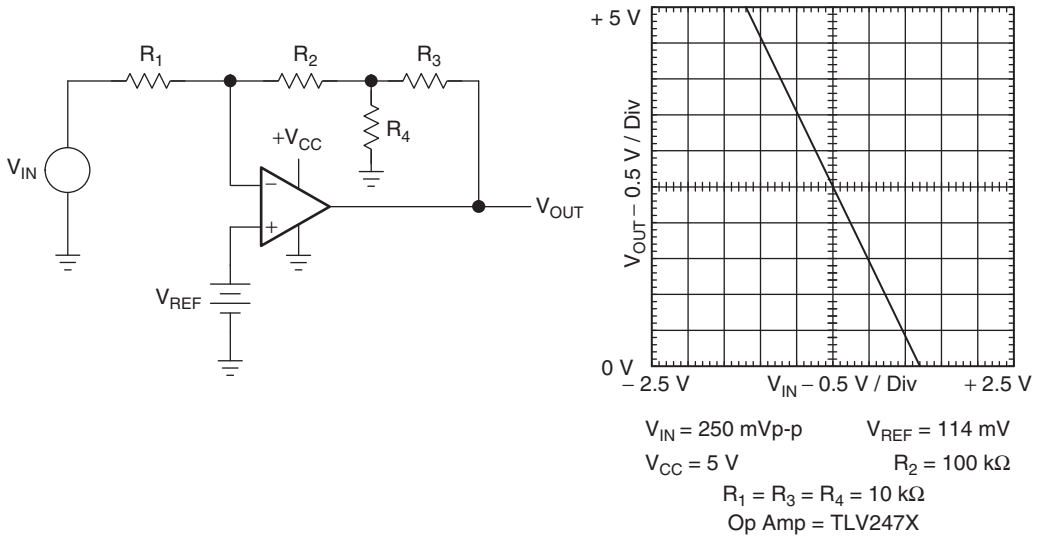


Figure A.3: T network in the feedback loop.

$$V_{OUT} = -V_{IN}\left[\frac{R_2 + R_3 + \frac{R_2R_3}{R_4}}{R_1}\right] + V_{REF}\left[1 + \frac{R_2 + R_3 + \frac{R_2R_3}{R_4}}{R_1}\right] \quad \text{(A.5)}$$

A.5 Inverting Integrator

The Laplace operator, $s = j\omega$, is used in Equation (A.6), and the mathematical operation $1/s$ constitutes an integration. Differentiation circuits are shown later, and the mathematical operation, s, constitutes a differentiation. The integration time constant is RC, thus the magnitude crosses 0 dB on a log plot when $RC = 1$. Also the phase is –45° when $RC = 1$:

$$V_{OUT} = -V_{IN}\frac{1}{RCs} \quad \text{(A.6)}$$

This integrator, shown in Figure A.4, is not very practical because there is no method of discharging the capacitor; hence any current leakage eventually charges the capacitor until the circuit becomes saturated. The positive input of the integrator is biased at $V_{CC}/2$ to center the output voltage at $V_{CC}/2$, thus allowing for positive and negative voltage swings. The bias resistors are selected as $2R$ so that the parallel combination equals R. This offsets the input current drawn through R.

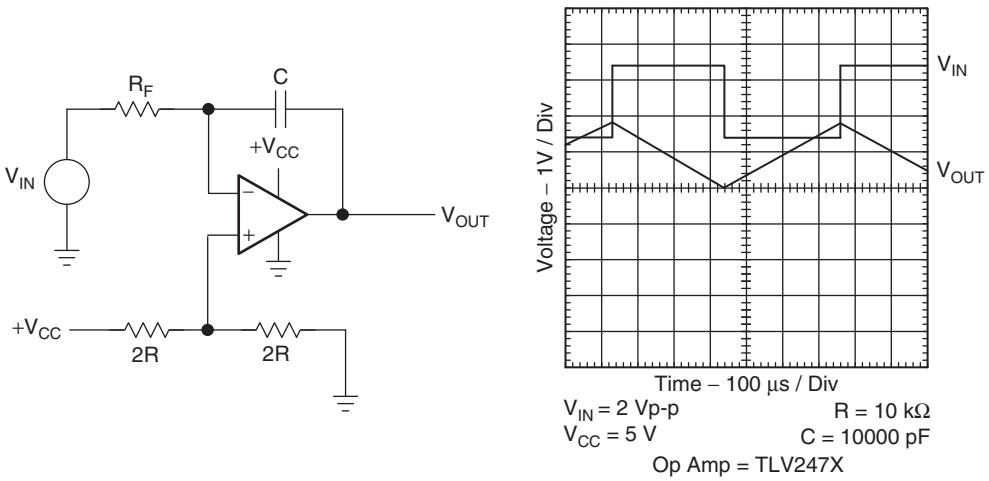


Figure A.4: Inverting integrator.

A.6 Inverting Integrator with Input Current Compensation

Functionally, the circuit in Figure A.5 is the same as that shown in Figure A.4, but a current compensation network has been added to offset the input current. V_{CC}, R_1, and R_2 bias the positive input at $V_{CC}/2$ to center the output voltage at $V_{CC}/2$, thus allowing for positive and negative voltage swings.

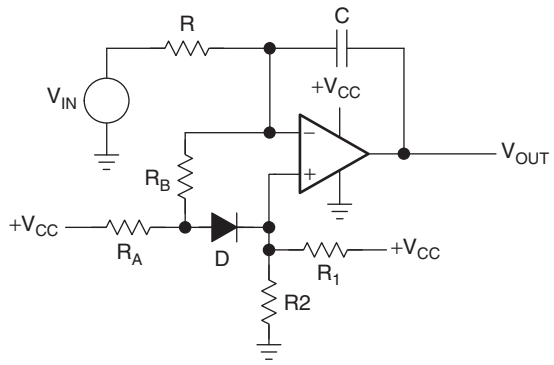


Figure A.5: Inverting integrator with input current compensation.

R_1 and R_2 are selected as relatively small values, because the current flowing through R_A also flows through the parallel combination of R_1 and R_2. R_A forward biases the diode with a constant current, so the diode acts like a small voltage regulator. The diode voltage drop is temperature sensitive, and this factor works in our favor because the input transistors are temperature sensitive. The two temperature sensitivities cancel out if the diode current is selected correctly. R_B is a large value resistor that acts like a current source, so it is selected such that it supplies the input bias current. Selecting R_B correctly ensures that no input current flows through the integration resistor, R.

This integrator is not very practical, because there is no method of discharging the capacitor. Hence, any input current eventually charges the capacitor until the circuit becomes saturated. The bias circuit drastically reduces the input current flowing through R, thus it extends the integration time. A reset circuit is needed to make the integrator more practical.

This bias compensation scheme is set up for an op amp that has npn input transistors. The diode must be reversed and connected to ground for op amps with pnp input circuits.

$$V_{\text{OUT}} = -V_{\text{IN1}} \frac{1}{RCs} \tag{A.7}$$

A.7 Inverting Integrator with Drift Compensation

Functionally, the circuit in Figure A.6 is the same as that shown in Figure A.5, but it uses an *RC* circuit in the positive lead to obtain drift compensation. The voltage divider is made from a series string of resistors (R_A), and V_{CC} biases the input in the center of the power supply.

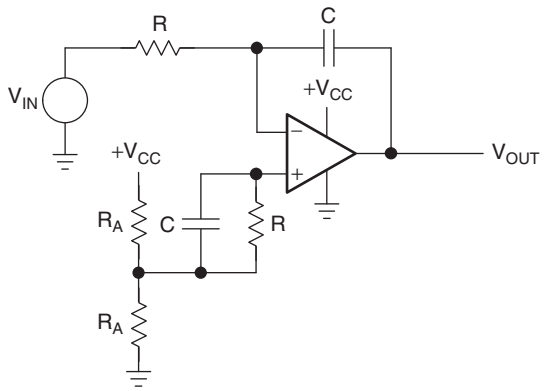


Figure A.6: Inverting integrator with drift compensation.

Positive input current flows through *R* and *C* in parallel, so the positive input current drops the same voltage across the parallel *RC* combination as the negative input current drops across its series *RC* combination. The common mode rejection capability of the op amp rejects the voltages caused by the input currents. Much longer integration times can be achieved with this circuit, but when the input signal does not center around $V_{CC}/2$, the compensation is poor.

$$V_{OUT} = -V_{IN1}\frac{1}{RCs} \tag{A.8}$$

A.8 Inverting Integrator with Mechanical Reset

Functionally, the circuit in Figure A.7 is the same as that shown in Figure A.5, but a method has been provided to discharge (reset) the capacitor. S_1 is a mechanical switch or relay; and when the contacts close, they short the integrating capacitor, forcing

it to discharge. Some capacitors are sensitive to fast discharge cycles, so R_S is put in the discharge path to limit the initial discharge current. When R_S is absent from the circuit, the impulse of current that occurs at the first instant of discharge causes considerable noise, so the selection of R_S is also based on noise considerations. For all practical purposes, the time constant formed by R_S and C determines the discharge rate.

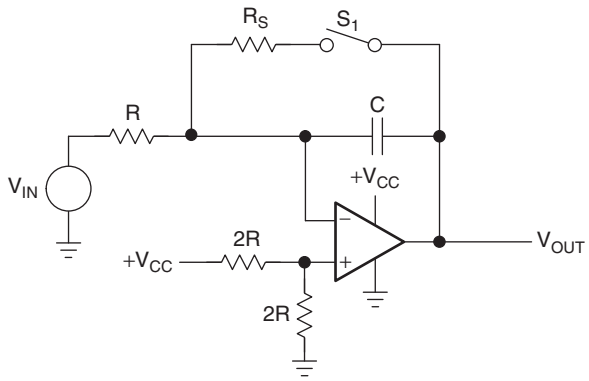


Figure A.7: Inverting integrator with mechanical reset.

One advantage of mechanical discharge methods is that they are isolated from the remainder of the circuit. Their size, weight, time delay, and uncertain actuating time offset this advantage. When the disadvantages of mechanical reset outweigh the advantages, circuit designers go to electronic reset circuits.

$$V_{\text{OUT}} = -V_{\text{IN1}} \frac{1}{RCs} \tag{A.9}$$

A.9 Inverting Integrator with Electronic Reset

Functionally, the circuit in Figure A.8 is the same as that shown in Figure A.5, but an electronic method has been provided to discharge (reset) the capacitor. Q_1 is controlled by a gate drive signal that changes its state from on to off. When Q_1 is on,

the gate source resistance is low, less than 100 Ω. And when Q_1 is off, the gate source resistance is high, about several hundred megaohms.

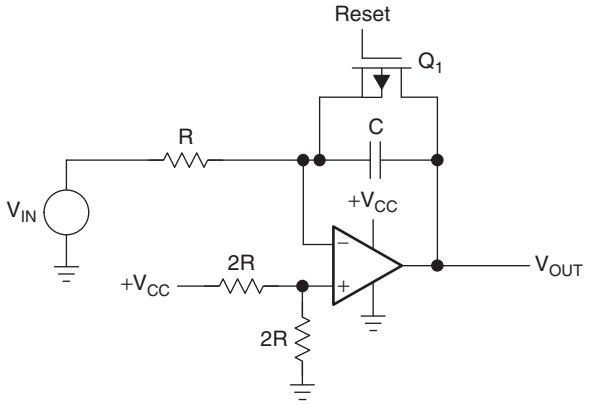


Figure A.8: Inverting integrator with electronic reset.

The source of the FET is at the inverting lead that is at ground, so the Q_1 gate source bias is not affected by the input signal. Sometimes, the output signal can get large enough to cause leakage currents in Q_1, so the designer must take care to bias Q_1 correctly. Consult a transistor book for more detailed information on transistor reset circuits. A major problem with electronic reset is the charge injected through the transistor's stray capacitance. This charge can be large enough to cause integration errors.

$$V_{OUT} = -V_{IN1}\frac{1}{RCs} \tag{A.10}$$

A.10 Inverting Integrator with Resistive Reset

The circuit in Figure A.9 differs from that shown in Figure A.5, because it yields a break point rather than a pure integration. On a log plot, the integrator slope is –6 dB per octave at the 0 frequency intercept, and the 0 dB intercept occurs when $f = 1/2\pi RC$.

A break point plots flat on a log plot until the break point, where it breaks down at –6 dB per octave. It is –3 dB when $f = 1/2\pi RC$.

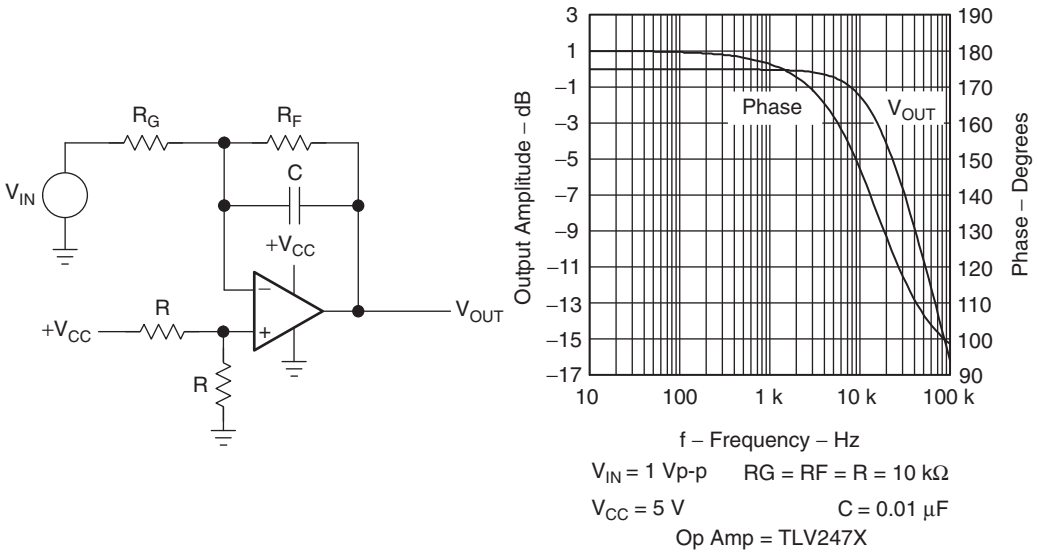


Figure A.9: Inverting integrator with resistive reset.

R_F is in parallel with the integrating capacitor, C, so it is continually discharging C. The low frequency attenuation that is the best attribute of the pure integrator is sacrificed for the reset circuit complexity.

$$V_{OUT} = -V_{IN1}\left(\frac{R_F}{R_G}\right)\frac{1}{R_F C + 1} \tag{A.11}$$

A.11 Noninverting Integrator with Inverting Buffer

The circuit in Figure A.10 is an inverting integrator preceded by an inverting buffer. Eliminating the signal inversion costs an op amp and four resistors, but this is the easiest way to get true noninverting integrator performance.

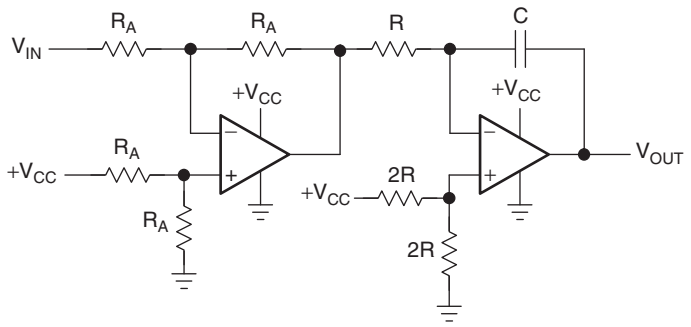


Figure A.10: Noninverting integrator with inverting buffer.

$$V_{OUT} = \frac{R_A}{R_A}\left(-V_{IN}\frac{1}{RCs}\right) = V_{IN}\frac{1}{RCs} \tag{A.12}$$

A.12 Noninverting Integrator Approximation

The circuit in Figure A.11 has fewer parts than the noninverting integrator with inverting buffer (Figure A.10), but it is not a true integrator because there is a zero in the transfer equation. The log plot starts rolling off at a –6 dB per octave rate at low frequencies, but when $f = 1/2\pi RC$, the zero cuts in. The zero causes the log plot to flatten out because the slope decreases to 0 dB per decade.

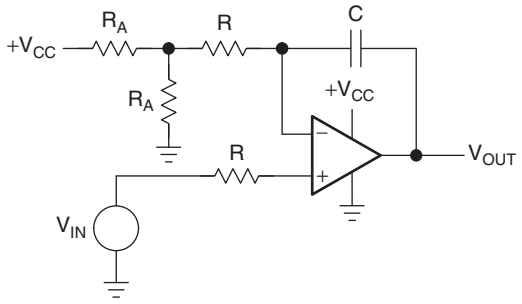


Figure A.11: Noninverting integrator approximation.

This circuit functions as an integrator at very low frequencies, but at frequencies higher than $f = 1/2\pi RC$, it functions as a buffer.

$$V_{\text{OUT}} = \frac{RCs + 1}{RCs} \tag{A.13}$$

A.13 Double Integrator

The circuit in Figure A.12 shows a double integrator.

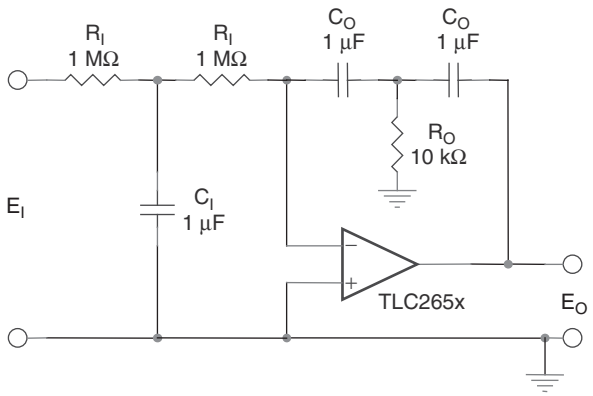


Figure A.12: Double integrator.

$$E_O = \frac{-4}{(R_I C_I)^2} \iint E_I dt = -4 \iint E_I dt \tag{A.14}$$

where

$$C_O = \frac{C_I}{2}, \; R_O = \frac{R_I}{2}$$

The double integrator integrates twice with one amplifier.

A.14 Differential Integrator

The circuit in Figure A.13 shows a differential integrator.

$$E_O = \frac{-1}{R_I C_O} \int (E_I - E_2) dt = 10 \int (E_2 - E_1) dt \tag{A.15}$$

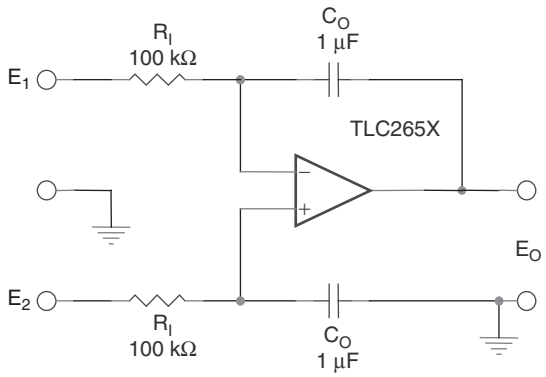


Figure A.13: Differential integrator.

The differential integrator integrates the difference between two signals.

A.15 AC Integrator

The circuit in Figure A.14 shows an AC integrator, which Integrates only the AC component.

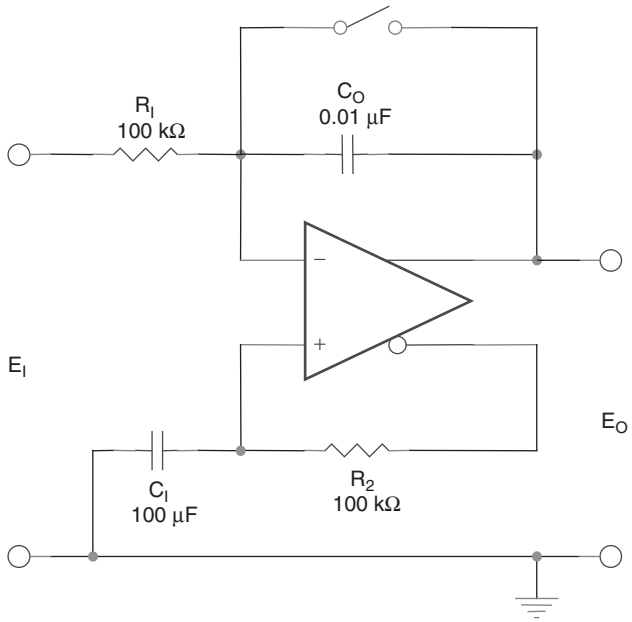


Figure A.14: AC integrator.

A.16 Augmenting Integrator

The circuit in Figure A.15 sums the input signal and its time integral:

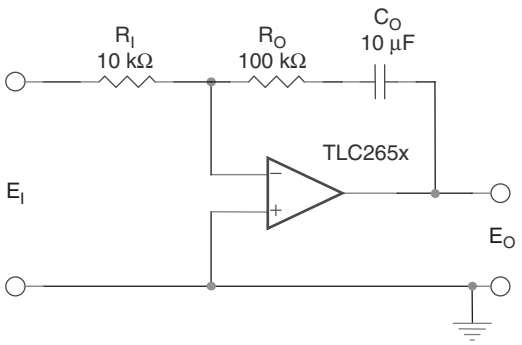


Figure A.15: Augmenting integrator.

$$E_O = \frac{-R_O E_I}{R_I} - \frac{1}{C_O R_I}\int E_I dt = -10E_I - \int E_I dt \tag{A.16}$$

A.17 Inverting Differentiator

In Figure A.16, the log plot of the differentiator is a positive slope of 6 dB per octave passing through 0 dB at $f = 1/2\pi RC$. At extremely high frequencies, the capacitive reactance goes to very low values, thus the circuit gain approaches the op amp open loop gain. This performance emphasizes any system noise or noise generated by the op amp. The poor noise performance of this circuit limits its application to a very few specialized situations.

This configuration has a pole in the feedback loop. If the op amp has more than one pole, and most op amps have several poles, this configuration can become oscillatory. The V_{CC} and R_A circuit bias the output in the center of the power supplies. $R_A/2$ should be selected equal to $R_G \| R_F$ so that input currents are canceled out.

$$V_{OUT} = -V_{IN} RCs \tag{A.17}$$

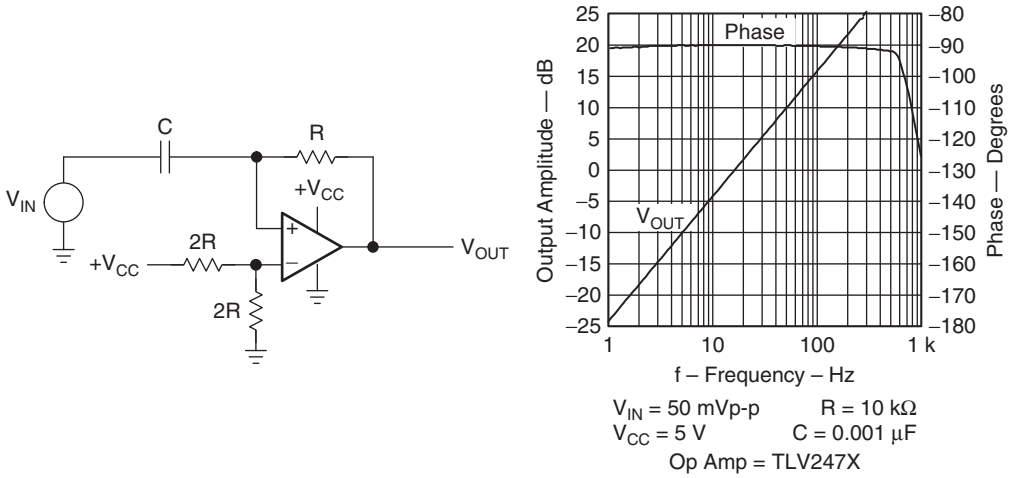


Figure A.16: Inverting differentiator.

A.18 Inverting Differentiator with Noise Filter

The circuit in Figure A.17 has a pure differentiator that rises at a 6 dB per octave slope from zero frequency. At $f = 1/2\pi R_F C_F$, the pole kicks in and the slope is reduced to zero.

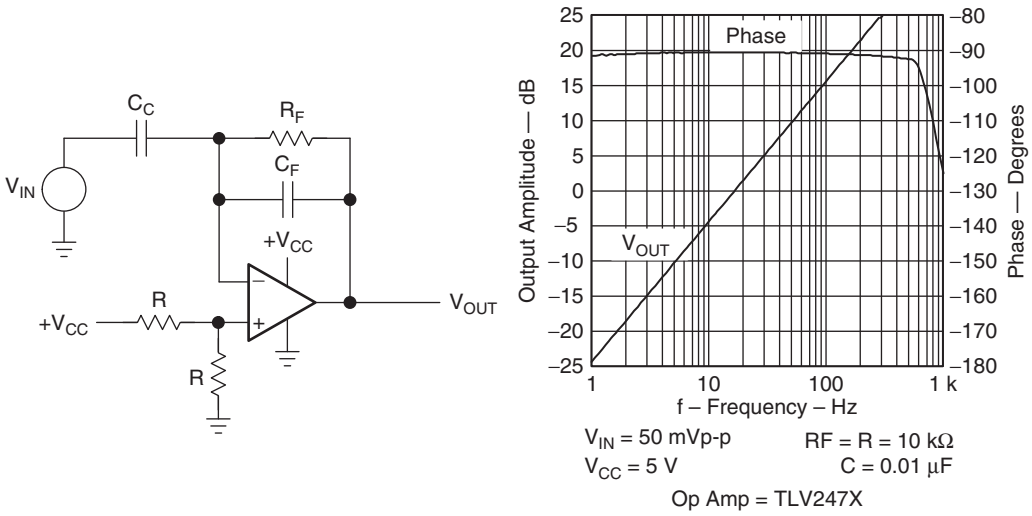


Figure A.17: Inverting differentiator with noise filter.

The pole has two effects. First, it stabilizes the circuit by canceling zero's phase shift. Second, it limits the circuit gain to 1 at high frequencies, so it acts like a noise filter.

$R/2$ should equal R_F for good input current cancellation, and V_{CC} coupled with R centers the output voltage.

$$V_{OUT} = -V_{IN}\frac{R_F C s}{R_F C_F s + 1} \tag{A.18}$$

A.19 Augmented Differentiator

The circuit in Figure A.18 shows an augmented differentiator, which sums the input and its derivative.

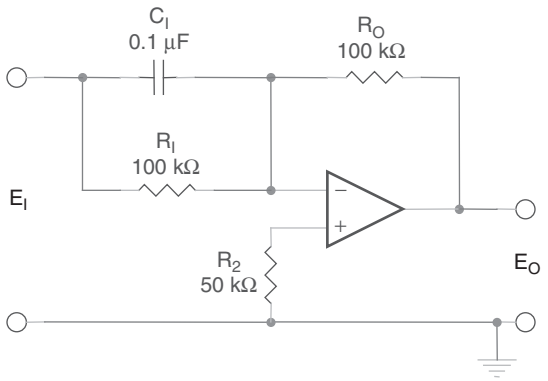


Figure A.18: Augmented differentiator.

$$E_O = \frac{-R_O E_I}{R_I} - R_O C_I \frac{dE_I}{dt} \tag{A.19}$$

A.20 Basic Wien Bridge Oscillator

The circuit in Figure A.19 shows a basic Wien bridge oscillator. When $\omega = 2\pi f = 1/RC$, the feedback is in phase (this is positive feedback) and the gain is 1/3, so oscillation requires an amplifier with a gain of 3. When $R_F = 2R_G$, the amplifier gain is 3 and

oscillation occurs at $f = 1/2\pi RC$. Normally, the gain is larger than 3 to ensure oscillation under worst case conditions.

V_{REF} sets the output DC voltage in the center of the span.

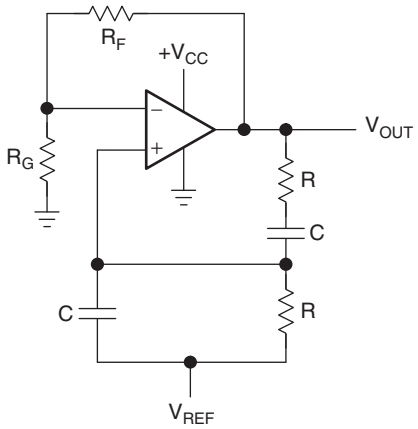


Figure A.19: Basic Wien bridge oscillator.

The output sine wave is highly distorted because limiting by saturation and cutoff controls the output voltage excursion. The distortion decreases when the gain is decreased, but the circuit may not oscillate under worst case low gain conditions.

$$V_{REF} = \frac{\frac{V_{CC}}{2}}{1 + \frac{R_F}{R_G}} \tag{A.20}$$

A.21 Wien Bridge Oscillator with Nonlinear Feedback

The circuit in Figure A.20 shows a Wien bridge oscillator with nonlinear feedback. When the circuit gain is 3, $R_L = R_F/2$.

Substituting a lamp (R_L) for the gain setting resistor reduces distortion, because the nonlinear lamp resistance adjusts the gain to keep the output voltage smaller than the

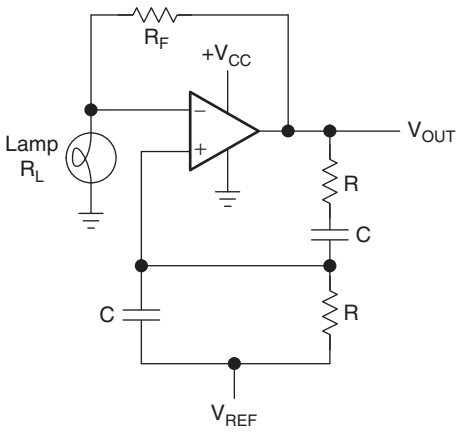


Figure A.20: Wien bridge oscillator with nonlinear feedback.

power supply voltage. The output voltage never approaches the power supply rail, so distortion doesn't occur. R_F and R_L determine the lamp current, see Equations (A.21) and (A.22):

$$I_{\text{LAMP}} = \frac{V_{\text{OUT(rms)}}}{R_F + R_L} \tag{A.21}$$

$$R_F = \frac{2\left(V_{\text{OUT(rms)}}\right)}{3\left(I_{\text{OUT(rms)}}\right)} \tag{A.22}$$

The lamp is selected by examining lamp resistance curves until a lamp with a resistance approximately equal to $R_F/2$ at $I_{\text{OUT(rms)}}$ is found. The output voltage swing should be less than 75% of the maximum guaranteed voltage swing, and $3R_L$ must be greater than the load resistance specified for the voltage swing specification. V_{REF} should be $V_{\text{CC}}/5$.

A.22 Wien Bridge Oscillator with AGC

In Figure A.21, the op amp is configured as an AC amplifier to ease biasing problems. The gain equation for the op amp follows. R_{G1} or R_{G2}, but not both resistors, is required depending on the selection of the Q_1.

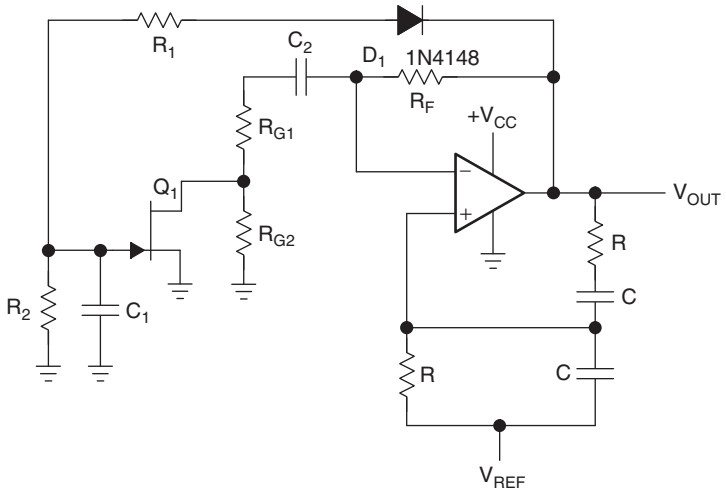


Figure A.21: Wien bridge oscillator with AGC.

$$G = \frac{R_F}{R_{G1} + R_{G2} \| R_{\text{FET}}} \tag{A.23}$$

The diode, D_1, half wave rectifies the output voltage and applies it to the voltage divider formed by R_1 and R_2. The voltage divider biases Q_1 in its linear region, and they eventually set the output voltage. C_1 filters the rectified sine wave with a long time constant, so that the output voltage stays constant. C_2 must be selected large enough to act as a short at the oscillation frequency.

As the output voltage increases, the negative voltage across the gate of Q_1 increases. The increased negative gate voltage causes Q_1 to increase its drain to source resistance. This results in increased op amp gain and an output voltage decrease. When the voltage divider and FET are selected properly, the output voltage swing is less than the guaranteed maximum swing, so distortion doesn't occur.

A.23 Quadrature Oscillator

Quadrature oscillators (Figure A.22) produce sine waves 90° out of phase, so they output sine/cosine, or quadrature waves.

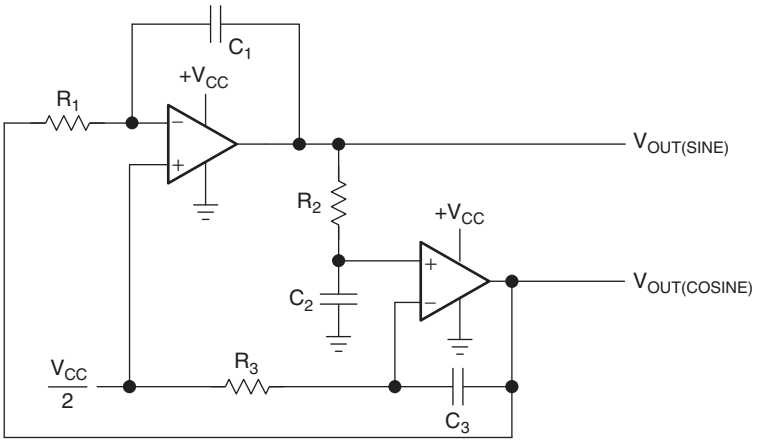


Figure A.22: Quadrature oscillator.

When $R_1C_1 = R_2C_2 = R_3C_3$, the circuit oscillates at $\omega = 2\pi f = 1/RC$. Both op amps act as integrators, causing two poles at $1/RC$, therefore the circuit oscillates when the loop gain crosses the 0 dB axis. The integrators ensure that gain is always sufficient for oscillation. There is a slight bit of distortion at the sine output, and it is very hard to eliminate this distortion.

A.24 Classical Phase Shift Oscillator

Theoretically, the three *RC* sections in Figure A.23 do not load each other, therefore the loop gain has three identical poles multiplied by the op amp gain.

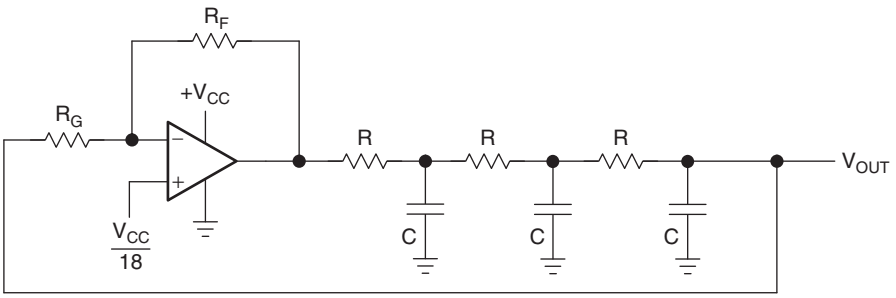


Figure A.23: Classical phase shift oscillator.

The loop phase shift is –180° when the phase shift of each section is –60°, and this occurs when $\omega = 2\pi f = 1.732/RC$, because the tangent of 60° = 1.73. The magnitude is (1/2)3, so the gain, $A = R_F/R_G$, must be greater than or equal to 8 for the system gain to be equal to 1.

The assumption that the *RC* sections do not load each other is not entirely valid, therefore the circuit does not oscillate at the specified frequency and the gain required for oscillation is more than 8. This circuit configuration was very popular when an active component was large and expensive; but now that op amps are inexpensive, small, and come in quad packages, the classical phase shift oscillator is losing popularity.

The classical phase shift oscillator has an undistorted sine wave available at the output of the third *RC* section. This is not a low impedance output, and the signal amplitude is smallest here, but these sacrifices have to be made to get away from distortion. An undistorted output can be obtained from the op amp by employing an AGC circuit similar to the one shown in Figure A.21. The reference voltage is set according to the equation $V_{\text{REF}} = V_{\text{CC}}/(1 + R_F/R_G)$ to center the output voltage at $V_{\text{CC}}/2$.

$$A\beta = \left(\frac{1}{RCs + 1}\right)^3 \tag{A.24}$$

A.25 Buffered Phase Shift Oscillator

A noninverting op amp buffers each RC section in the oscillator in a buffered phase shift oscillator. Equation (A.25) represents the transfer function of this circuit if $R_G \gg R$:

$$A\beta = \left(\frac{1}{RCs + 1}\right)^3 \tag{A.25}$$

The loop phase shift is –180° when the phase shift of each section is –60°, and this occurs when $\omega = 2\pi f = 1.732/RC$, because the tangent 60° = 1.73. The magnitude of β at this point is (1/2)3, so the gain, $A = R_F/R_G$, must be greater than or equal to 8 for the system gain to be equal to 1.

The buffered phase shift oscillator has an undistorted sine wave available at the output of the third *RC* section. This is not a low impedance output, and the signal amplitude is smallest here, but these sacrifices have to be made to get away from distortion. An undistorted output can be obtained from the op amp if an AGC circuit similar to the one shown in Figure A.24 is employed.

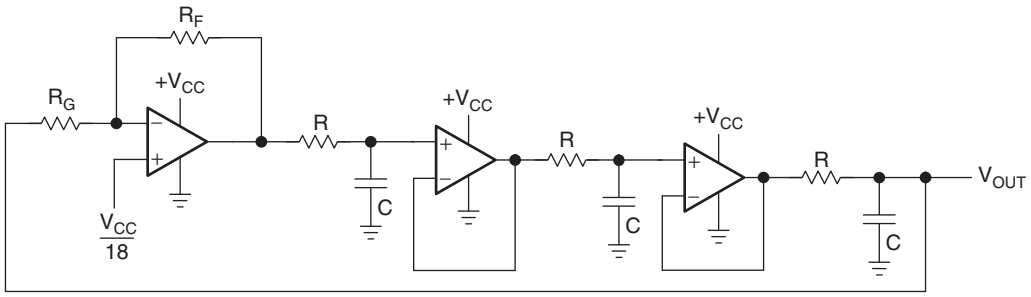


Figure A.24: Buffered phase shift oscillator.

There are three op amps, so the gain can be distributed among the op amps at the expense of a few resistors and the distortion is reduced. Another method of reducing distortion is to limit the output voltage swing softly with external components. The limiting technique does not yield as good results as the AGC technique, but it is less expensive. The reference voltage is set according to the equation $V_{REF} = V_{CC}/2(1 + R_F/R_G)$ to center the output voltage at $V_{CC}/2$.

A.26 Bubba Oscillator

The bubba oscillator (Figure A.25) is another phase shift oscillator, but it takes advantage of the quad op amp package to yield some unique advantages. Each *RC* section is buffered by an op amp to prevent loading. When $R_G \gg R$, there is no loading in the circuit and the circuit yields theoretical performance.

Four RC sections require –45° phase shift per section to accumulate –180° phase shift. Each *RC* section contributes –45° phase shift when $\omega = 1/RC$. The gain required for oscillation is $G \geq (1/0.707)4 = 4$. Taking outputs from alternate sections yields low impedance quadrature outputs. When an output is taken from each op amp, the circuit delivers four 45° phase shifted sine waves.

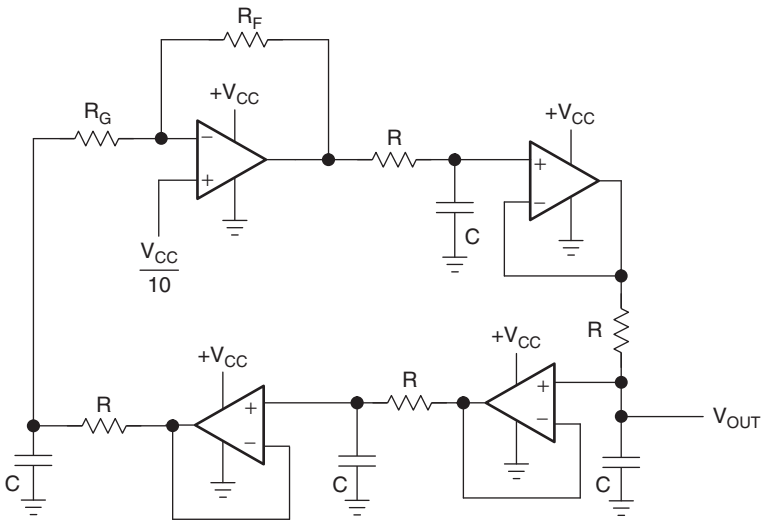


Figure A.25: Bubba oscillator.

The gain, A, must equal 4 for oscillation to occur. Very low distortion sine waves can be obtained from the junction of R and R_G. When low distortion sine waves are required at all outputs, the gain should be distributed among the op amps. Gain distribution requires biasing of the other op amps, but it has no effect on the oscillator frequency. This oscillator has the best $d\varphi/df$ of the phase shift oscillators, so it has minimum frequency drift. The reference voltage is set according to the equation $V_{REF} = V_{CC}/2(1 + R_F/R_G)$ to center the output voltage at $V_{CC}/2$.

$$A\beta = \left(\frac{1}{RCs + 1}\right)^4 \tag{A.26}$$

A.27 Triangle Oscillator

The triangle oscillator (Figure A.26) produces triangle waves and square waves. The op amp functions as an integrator. When the output voltage of the comparator is low, the output of the op amp charges C until the output voltage exceeds the hysteresis voltage set by R_1 and R_F and the reference voltage ($V_{CC}/2$). At this point, the comparator output switches to a high state and the op amp integrates the voltage in a negative direction. The triangle wave (op amp output voltage swing) is given in Equation (A.27) and the frequency of oscillation is given in Equation (A.28):

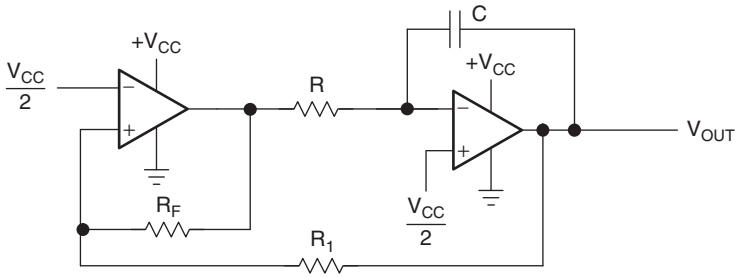


Figure A.26: Triangle oscillator.

$$V_{\text{OUT}} = \frac{V_{\text{CC}}}{2} \pm \frac{V_{\text{CC}} R_1}{2R_F} \tag{A.27}$$

$$f = \frac{R_F}{4CRR_1} \tag{A.28}$$

The op amp reference voltage can be adjusted to equalize the triangle rise and fall times.

A.28 Attenuation

An inverting attenuation circuit (this circuit is taken from the design notes of William Ezell) can be thought of as a T network in the R_G resistor. It is shown in Figure A.27.

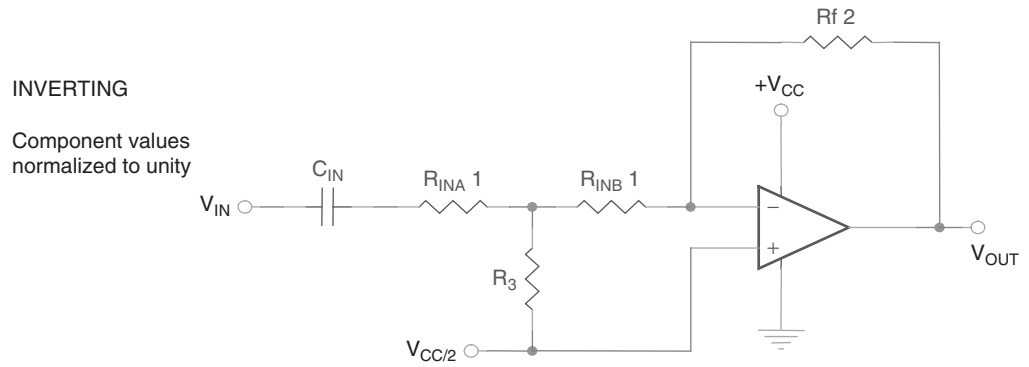


Figure A.27: Inverting attenuator circuit.

R_G is replaced by a T network consisting of R_{INA}, R_{INB}, and R_3. A set of normalized values of the resistor R_3 for various levels of attenuation is shown in Table A.1. For nontablated attenuation values, the resistance is

Table A.1: Normalization Factors

DB pad	V_{OUT}/V_{IN}	R_3
0	1.0000	∞
0.5	0.9441	8.4383
1	0.8913	4.0977
2	0.7943	0.9311
2	0.7079	1.2120
3.01	0.7071	1.2071
3.52	0.6667	1.000
4	0.6310	0.8549
5	0.5623	0.6424
6	0.5012	0.5024
6.02	0.5000	0.5000
7	0.4467	0.4036
8	0.3981	0.3307
9	0.3548	0.2750
9.54	0.3333	0.2500
10	0.3162	0.2312
12	0.2512	0.1677
12.04	0.2500	0.1667
13.98	0.2000	0.1250
15	0.1778	0.1081
15.56	0.1667	0.1000
16.90	0.1429	0.08333

(*Continued*)

Table A.1: Normalization Factors (Cont'd)

DB pad	V_{OUT}/V_{IN}	R_3
18	0.1259	0.07201
18.06	0.1250	0.07143
A1.08	0.1111	0.06250
20	0.1000	0.05556
25	0.0562	0.02979
30	0.0316	0.01633
40	0.0100	0.005051
50	0.0032	0.001586
60	0.0010	0.0005005

$$R_3 = \frac{V_O/V_{IN}}{2 - 2(V_O/V_{IN})} \tag{A.29}$$

To work with normalized values, do the following:

- Select a base value of resistance, usually between 1 kΩ and 100 kΩ for R_f and R_{IN}.
- Divide R_{IN} in two for R_{INA} and R_{INB}.
- Multiply the base value for R_f and R_{IN} by 1 or 2, as shown in Figure A.27.
- Look up the normalization factor for R_3 in Table A.1, and multiply it by the base value of resistance.

For example, if R_f is 20 kΩ, R_{INA} and R_{INB} are each 10 kΩ, and a 3 dB attenuator would use a 12.1 kΩ resistor.

A.29 Simulated Inductor

The circuit in Figure A.28 reverses the operation of a capacitor, making a simulated inductor. An inductor resists any change in its current, so when a DC voltage is applied

to an inductance, the current rises *slowly* and the voltage falls as the external resistance becomes more significant.

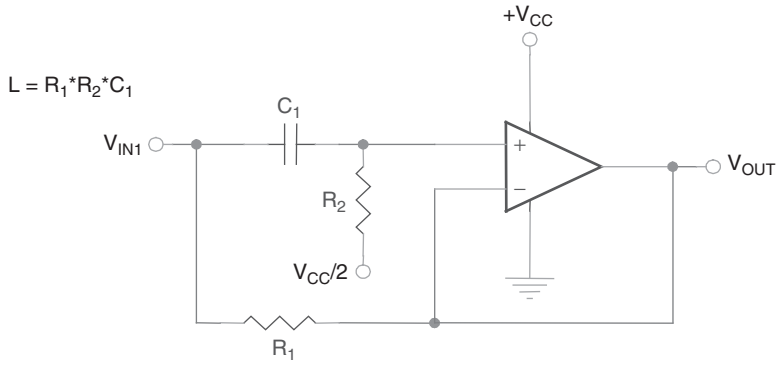


Figure A.28: Simulated inductor.

An inductor passes low frequencies more readily than high frequencies, the opposite of a capacitor. An ideal inductor has zero resistance. It passes DC without limitation, but it has infinite impedance at infinite frequency.

If a DC voltage is suddenly applied to the inverting input through resistor R_1, the op amp ignores the sudden load because the change is also coupled directly to the noninverting input via C_1. The op amp represents high impedance, just like an inductor.

As C_1 charges through R_2, the voltage across R_2 falls, so the op amp draws current from the input through R_1. This continues as the capacitor charges, and eventually the op amp has an input and output close to virtual ground ($V_{CC}/2$).

When C_1 is fully charged, resistor R_1 limits the current flow; and this appears as a series resistance within the simulated inductor. This series resistance limits the Q of the inductor. Real inductors generally have much less resistance than the simulated variety.

A simulated inductor has some limitations:

- One end of the inductor is connected to virtual ground.
- The simulated inductor cannot be made with high Q, due to the series resistor R_1.

- It does not have the same energy storage as a real inductor. The collapse of the magnetic field in a real inductor causes large voltage spikes of opposite polarity. The simulated inductor is limited to the voltage swing of the op amp, so the flyback pulse is limited to the voltage swing.

These factors limit the use of simulated inductors, but one application is perfect for simulated inductors: graphic equalizers.

To make a graphic equalizer, start with the basic op amp circuit shown in Figure A.29. The inductor L is shown with a parasitic resistance R_S. It resonates with C_2; and depending on the setting of potentiometer R_2, the stage either produces a gain or a loss at the resonant frequency. The parasitic resistance of the inductor R_S also sets the Q of the resonant circuit. Therefore, it determines the number of stages of equalization required to cover the audio band. In the right hand side of Figure A.29, the inductor L has been replaced by a simulated inductor circuit. To form the graphic equalizer, multiple stages of equalization are added in parallel by placing more potentiometers in parallel with R_2.

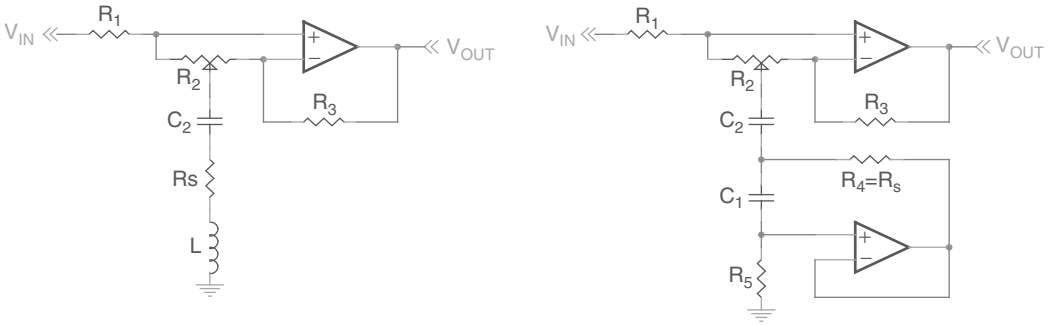


Figure A.29: Graphic equalizer.

A.30 Twin T Single Op Amp Bandpass and Notch Filters

The filter design sections of this book presented some good topologies for bandpass and notch filters. However, some designers still believe superior performance can be achieved using the twin T topology. In the case of the notch filter, the only single op amp topology for a notch filter is the twin T configuration.

Twin T filters are based on a passive (*RC*) topology that uses three resistors and three capacitors. Matching these six passive components is critical; fortunately, it is also easy. The entire network can be constructed from a single value of resistance and a single value of capacitance, running them in parallel to create R_3 and C_3 in the twin T schematics shown in Figure A.30. Components from the same batch are likely to have very similar characteristics.

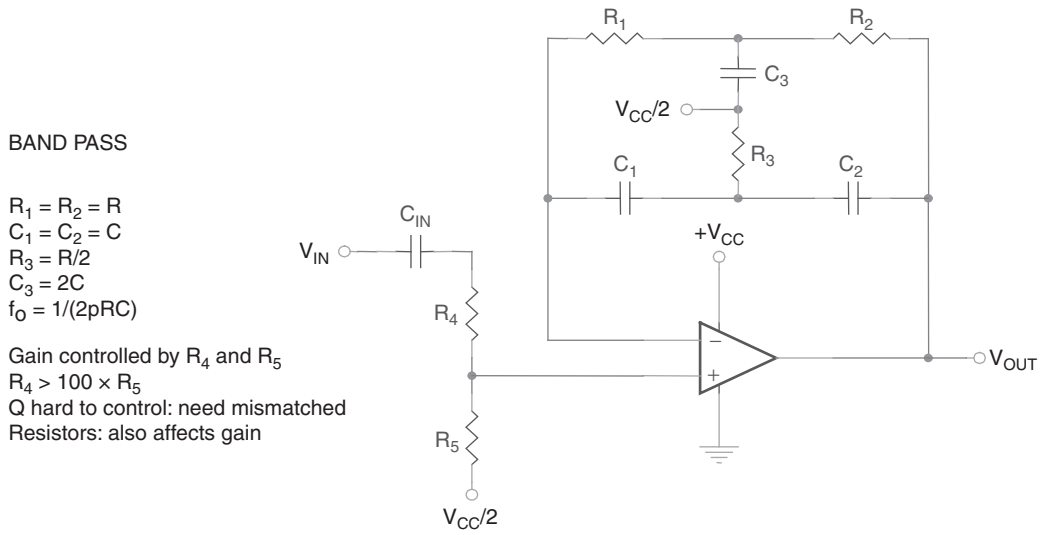


Figure A.30: Single op amp bandpass filter.

The bandpass circuit oscillates if the components are matched too closely. It is best to detune it slightly, by selecting the resistor to virtual ground to be one E-96 1% resistor value off, for instance.

The notch configuration of the twin T filter is shown in Figure A.31.

Figure A.32 shows a very nice way to lay out a twin T circuit. Considering all values of *R* and all values of *C* to be of equal value, for surface mount components, lay a pattern vertically with *C*, *R*, *R*, *C* on the top row and *R*, *C*, *C*, *R* on the bottom row. Input to the twin T connects to the *C* and *R* on the left, output from the *C* and *R* on the right connect all the top pads together, all of the bottom pads together, and connect the middle four components to $V_{CC}/2$. The author has employed this strategy successfully in a high volume production product.

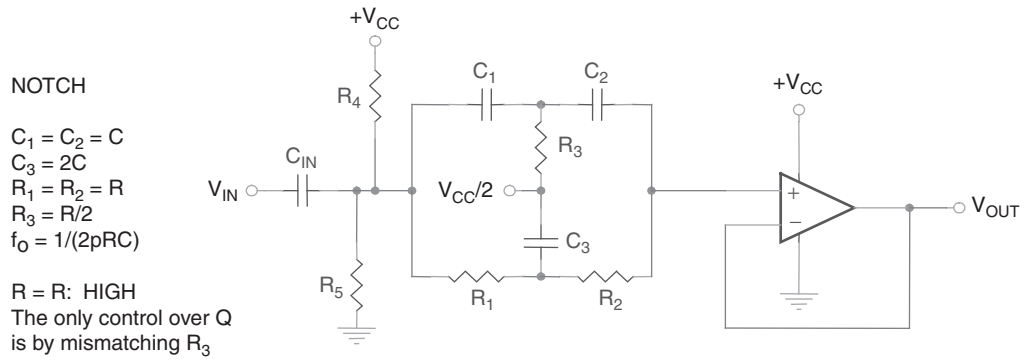


Figure A.31: Single op amp notch filter.

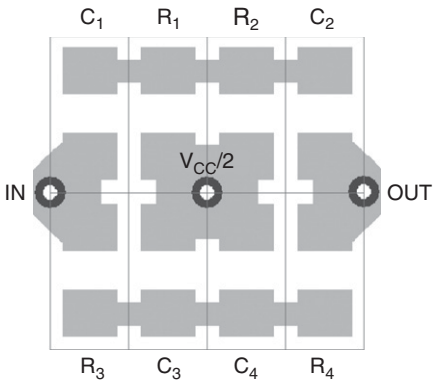


Figure A.32: Twin T network layout.

A.31 Constant Current Generator

Figure A.33 shows a constant current generator. Equations (A.30) are a convenient current reference up to 20 mA:

$$I = \frac{V_Z}{R_2} = \frac{6}{300} = 20 \text{ mA}$$

$$R_1 = \frac{15 - V_Z}{I_Z} = \frac{9}{25} = 360\ \Omega \tag{A.30}$$

$$R_{L\,\min} = \frac{\text{Saturation voltage}}{I} = \frac{13.5 \text{ V}}{20 \text{ mA}} = 675\ \Omega$$

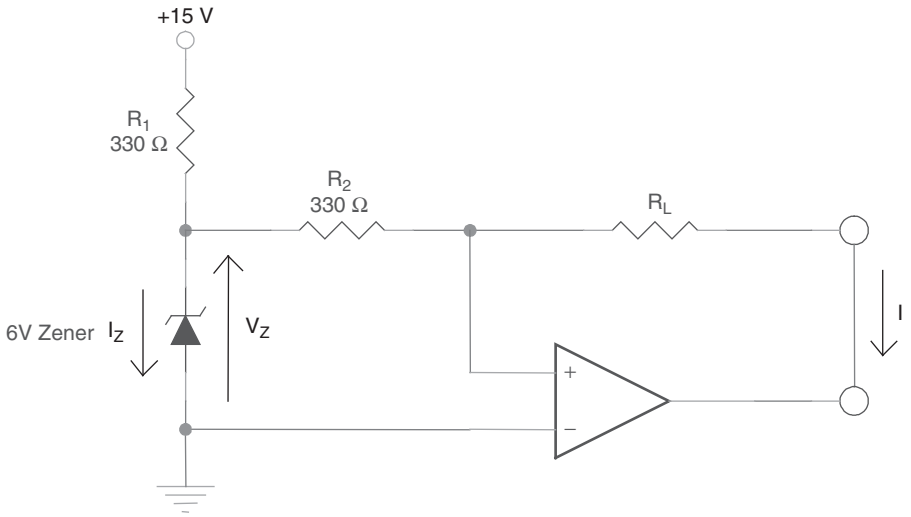


Figure A.33: Constant current generator.

A.32 Inverted Voltage Reference

The circuit of Figure A.34 can be used to generate a negative voltage reference equal to a positive reference voltage. This circuit requires split supplies, however.

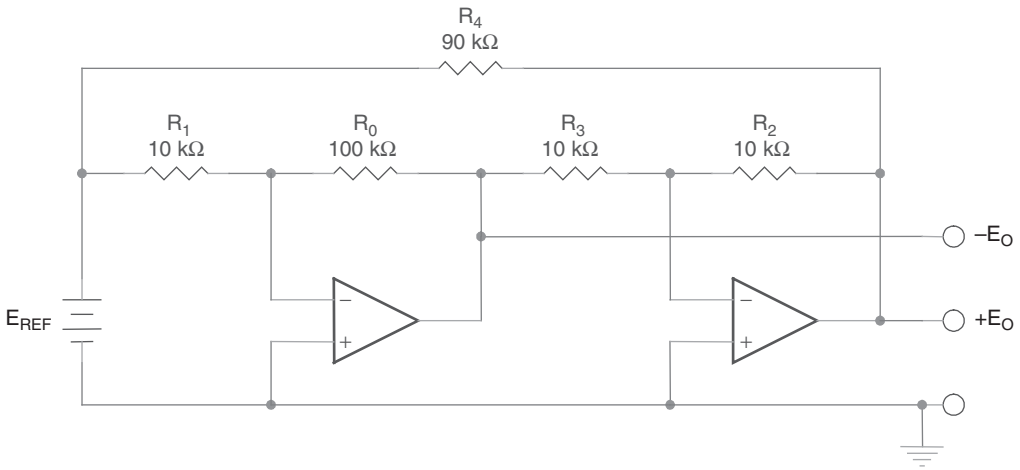


Figure A.34: Reference voltage supply.

A.33 Power Booster

If a designer is careful, it is possible to create a composite amplifier whose important characteristics are better than either individual op amp.

The circuit in Figure A.35 shows a composite amplifier constructed from an OPA277 and an OPA512. The OPA512 is used as a power output buffer in the feedback loop of the OPA277. Its characteristics are tabulated in Table A.2.

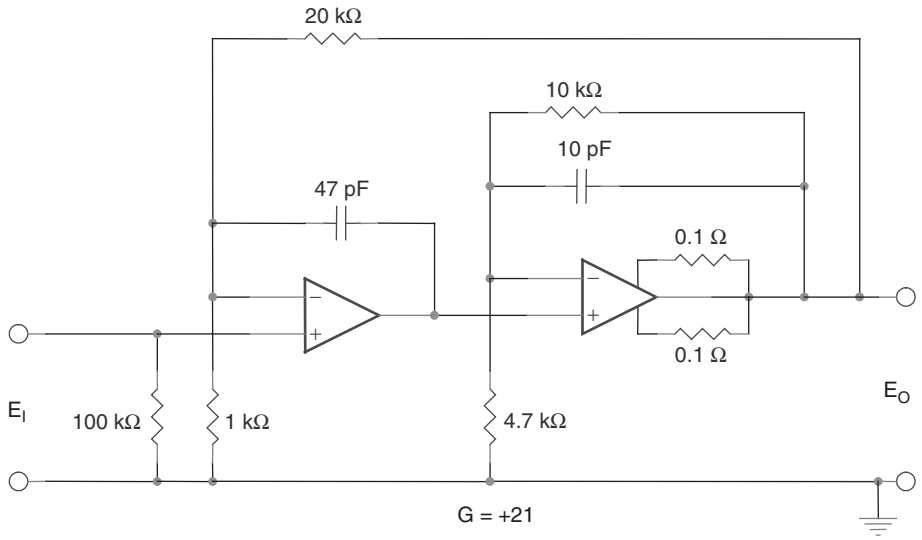


Figure A.35: Composite op amp.

Table A.2: Composite Amplifier

Parameter	OPA277	OPA512	Compound
V_{OS}	20 μV	6 mV	20 μV
Drift	0.15 μV/°C	65 μV/°C	0.15 μV/°C
I_B	1 nA	30 nA	1 nA
CMRR	130 dB	100 dB	130 dB
V_{OUT}	±13 V	±35 V	±35 V
I_{OUT}	5 mA	10 A	10 A
SR	0.8 V/μs	2.5 V/μs	2.4 V/μs

The OPA512 has the highest slew rate and therefore is operated within a local closed loop. The slower OPA277 is operated within the outer loop. The 47 pF capacitor provides a small amount of phase shift to help stabilize the system. The resulting performance of the compound amplifier shows that the front end characteristics of the OPA277 are joined with the ±35 V at 10 A drive current capabilities out of the OPA512. The slew rate of the OPA277 is 0.8 V/μs. That slew rate is gained up times three in the OPA512 so that there is an effective slew rate for the compound amplifier of 2.4 V/μs.

A.34 Absolute Value

Figure A.36 shows an absolute value circuit, where $+E_I$ is the follower circuit, $-E_I$ is the inverter circuit, and $E_O = |E_I|$. There is full wave rectification. Reverse the diodes to give $E_O = -|E_I|$.

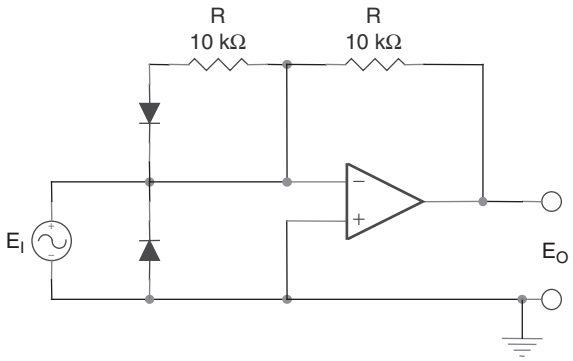


Figure A.36: Absolute value circuit.

A.35 Peak Follower

Figure A.37 shows a peak follower circuit with peak value memory. Use a low leakage capacitor. $E_O = E_I$ maximum. Common mode input voltage must be observed.

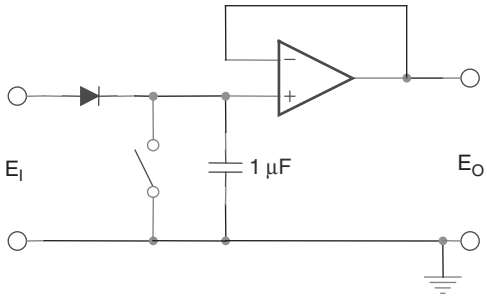


Figure A.37: Peak follower circuit.

A.36 Precision Rectifier

Figure A.38 shows a precision rectifier circuit.

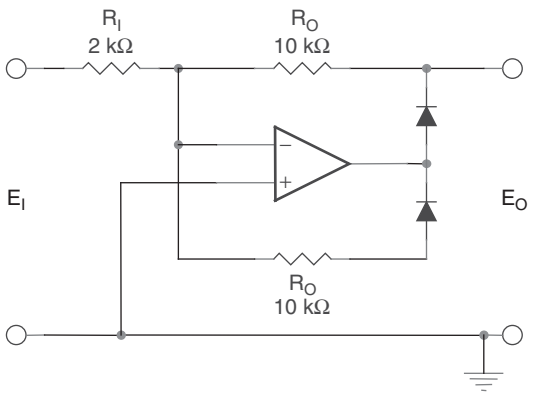


Figure A.38: Precision rectifier.

$$E_O \text{ peak} = \frac{-R_O}{R_I} E_I \text{ peak} = -5E_I \text{ peak} \tag{A.31}$$

Placing rectifiers in feedback loop decreases nonlinearity to a very small value.

A.37 AC to DC Converter

Figure A.39 shows an AC to DC converter.

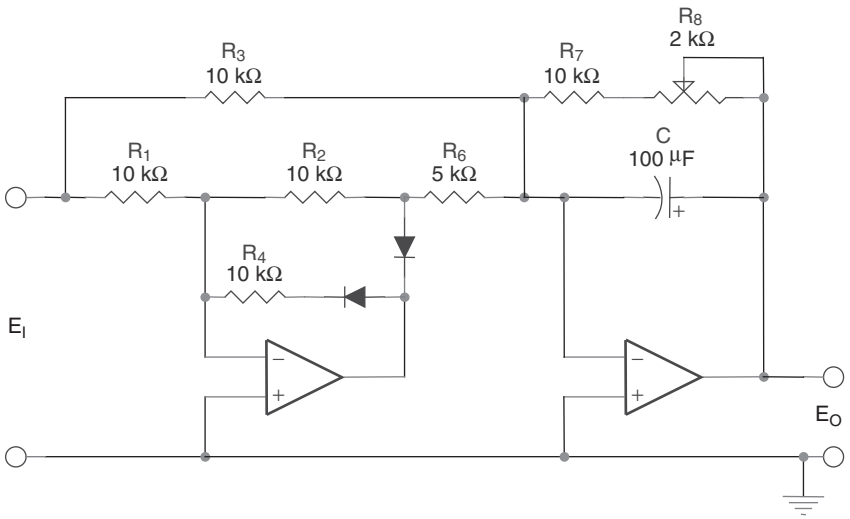


Figure A.39: AC to DC converter.

$$E_{O(\text{AVERAGE})} = 0.9E_{I(\text{rms})}$$

$$E_I = 6 \text{ mV to } 6 \text{ mV rms at } 10 \text{ to } 1000 \text{ Hz}$$

This is used for precision conversion for measurement or control. It features full wave rectifier with a smoothing filter.

A.38 Full Wave Rectifier

Figure A.40 shows a full wave rectifier. This is a precision absolute value circuit.

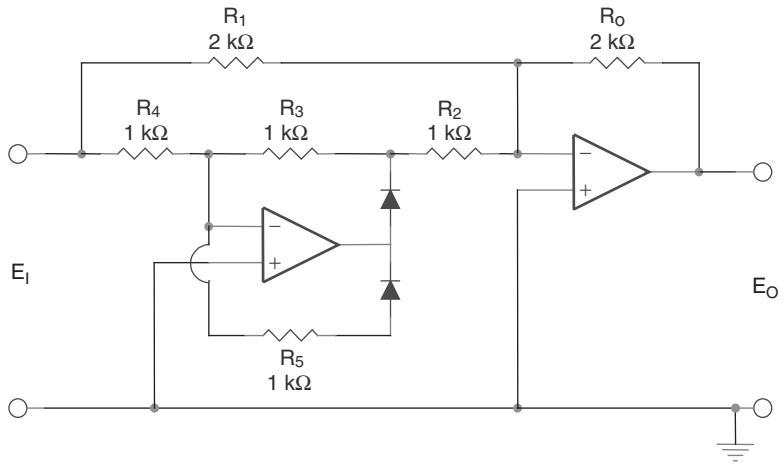


Figure A.40: Full wave rectifier.

A.39 Tone Control

One rather unusual op amp circuit is the tone control circuit (Figure A.41). It bears some superficial resemblance to the twin T circuit configuration, but it does not have a twin T topology. It is actually a hybrid of one pole low pass and high pass circuits with gain and attenuation.

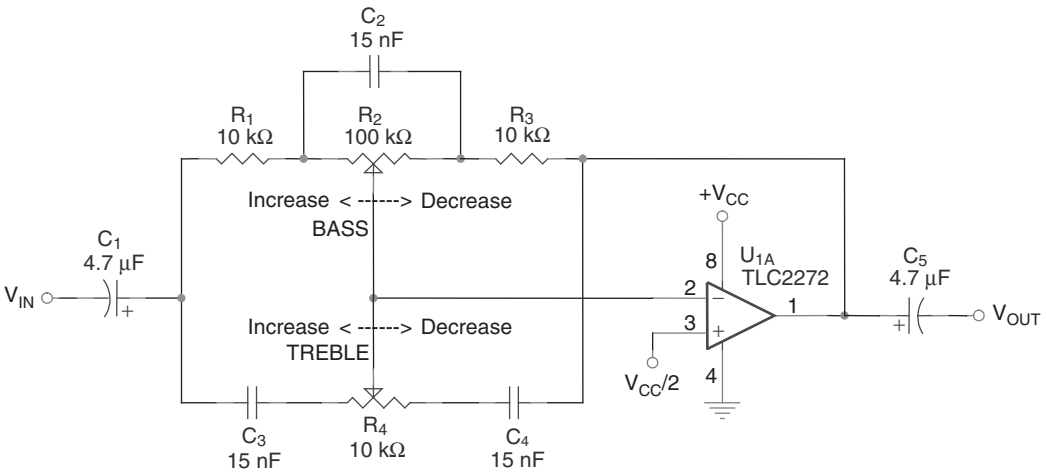


Figure A.41: Tone control.

The midrange for the tone adjustments is 1 kHz. It gives about ±20 dB of boost and cut for bass and treble. The circuit is a minimum component solution, seeking to limit cost. This circuit, unlike similar circuits, uses linear potentiometers instead of logarithmic. Two different potentiometer values are unavoidable, but the capacitors are the same value except for the coupling capacitor. The ideal value of capacitor is 0.016 µF, which is an E-24 value, so the more common E-12 value of 0.015 µF is used instead. Even that value is a bit odd, but it is easier to find an oddball capacitor value than it is an oddball potentiometer value.

The plots in Figure A.42 show the response of the circuit with the potentiometers at the extremes and at one quarter and three quarter positions. The mid position, although not shown, is flat to within a few millidecibels. The compromises involved in reducing the circuit cost and using linear potentiometers lead to some slight nonlinearities. The one quarter and three quarter positions are not exactly 10 and –10dB, meaning that the potentiometers are most sensitive toward the end of their travel. This may be preferable to the listener, giving a fine adjustment near the middle of the potentiometers and more rapid adjustment near the extreme positions. The center frequency shifts slightly, but this should be inaudible. The frequencies nearer the midrange are adjusted more rapidly than the frequency extremes, which also may be more desirable to the listener. A tone control is not a precision audio circuit, and therefore the listener may prefer these compromises.

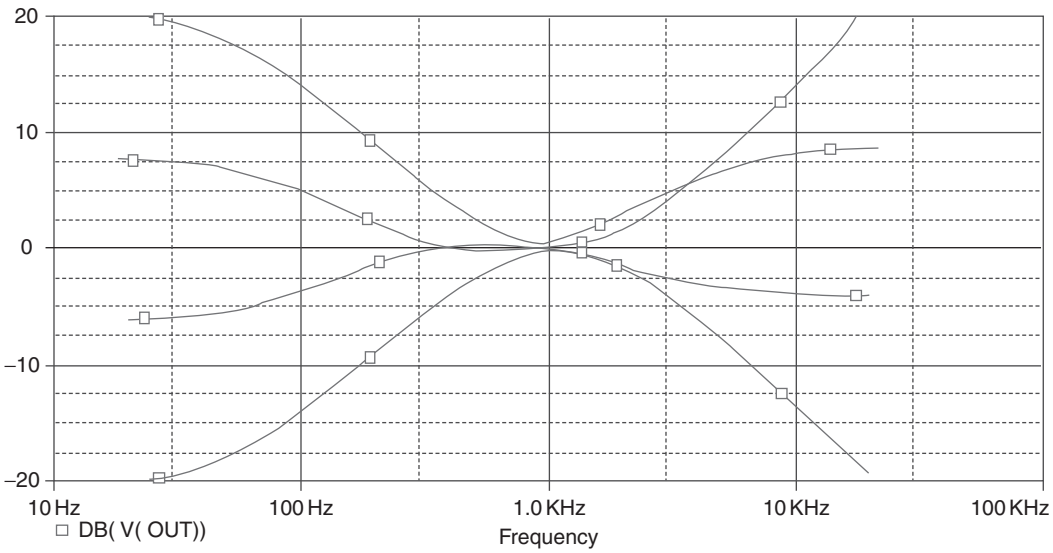


Figure A.42: Tone control response.

A.40 Curve Fitting Filters

Analog designers are often asked to design low pass and high pass filter stages for maximum rejection of frequencies that are out of band. This is not always the case, however. Sometimes the designer is asked to design a circuit that conforms to a specified frequency response curve. This can be a challenging task, particularly if all the designer knows is that a single pole filter rolls off 20 dB per decade and double pole 40 dB per decade. How does the designer implement a different roll-off?

To begin with, it is not possible to get more out of a filter than it is designed to produce. A single pole will give no more than 20 dB per decade—and cannot be increased or decreased. More roll-off demands a double pole filter with 40 dB per decade. Obtaining different roll-off characteristics is done by allowing filters at closely spaced frequencies to overlap.

One popular curve fitting application is the RIAA equalization (Figure A.43), which compensates for equalization applied to vinyl record albums during manufacture. Many newer pieces of audio gear have omitted the RIAA equalization circuit completely, assuming that the majority of users do not desire the function. In spite of the enormous popularity of audio CDs, there is still a dedicated group of audiophiles that have a large library of record albums, titles that are not available on CD or are out of print.

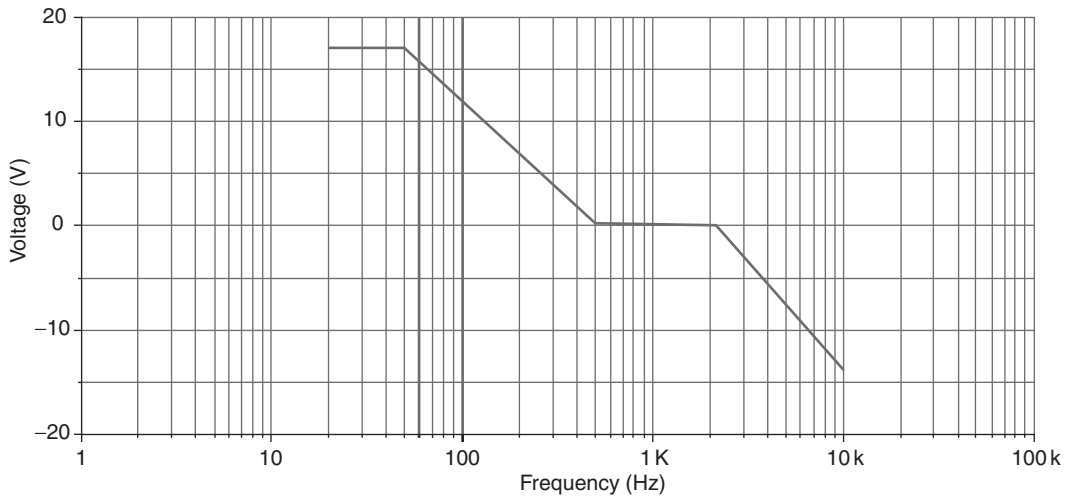


Figure A.43: RIAA equalization curve.

RIAA has three break points:

- 17 dB from 20 to 50 Hz.
- 0 dB from 500 to 2120 Hz.
- –13.7 dB at 10 kHz.

RIAA equalization curves often include another break point at 10 Hz to limit low frequency "rumble" effects that could resonate with the turntable's tonearm. The standard input impedance in the circuits shown here is 47 kΩ. This impedance makes a convenient place to inject DC offset into single supply circuits, so it is isolated from the phono cartridge by an input capacitance. The phono cartridge output is assumed to be 12 mV.

Application circuits were evaluated from many sources in print and on the Web. Many of these either did not work at all, did not easily translate to single supply operation, or deviated markedly from the RIAA specification. Many circuits have been proposed for this function; in fact, competitions have been held to propose the best. To this fray, this volume respectfully submits Figure A.44.

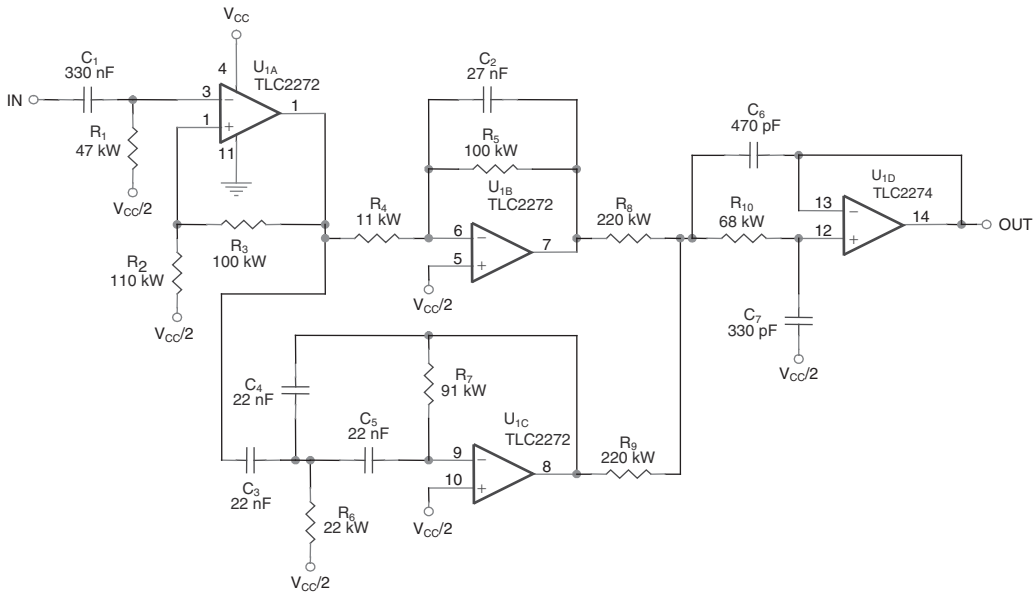


Figure A.44: RIAA equalization preamplifier.

This circuit topology is very flexible—most of the RIAA break points are independently adjustable:

- R_1 and C_1 set the low frequency response.
- U_{1A}, R_2, and R_3 control the overall gain of the circuit.
- R_4 and R_5 control the low frequency gain.
- R_5 and C_2 control the 50 Hz low frequency break point.
- C_3, C_4, C_5, R_6, R_7, and U_{1C} form a 500 Hz high pass filter that reverses the effect of the 50 Hz low pass filter and flattens the response through 1 kHz until the 2120 Hz low pass filter begins to affect the response.
- R_8, R_9, R_{10}, C_6, C_7, U_{1D} form the 2120 Hz low pass filter, the input resistor has been split into a summing resistor.

The overall response of the filter is shown in Figure A.45.

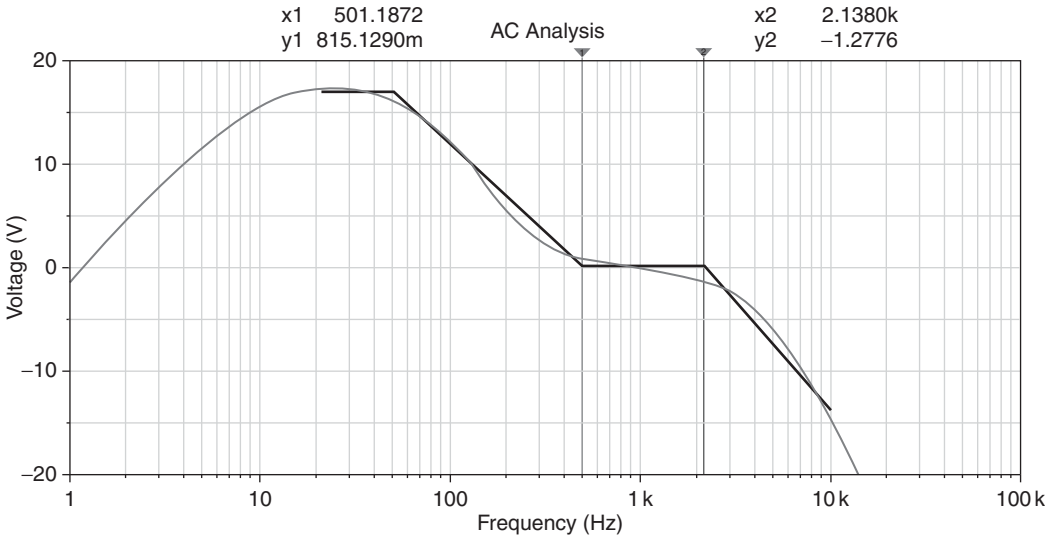


Figure A.45: RIAA response.

The 500 Hz response is above the ideal curve by 0.8 dB, and the 2120 Hz response is below the ideal curve by –1.3 dB. This circuit is about the best that can be done without many more op amps and complex design techniques. It should produce very aesthetically pleasing sound reproduction.

References

1. Brown, Thomas R. (1963). *Handbook of Operational Amplifier Applications*. Application Report SBOA092A. Texas Instruments.
2. Carter, Bruce. (2000) *An Audio Circuit Collection*, parts 1–3. Dallas: Texas Instruments.

APPENDIX B

Terminating Differential Amplifiers

Bruce Carter

B.1 Introduction

Termination of differential amplifiers is a complex and little understood technique. It has been moved to an appendix because it is a rarely used design problem and so it doesn't slow the flow of material in Chapter 3. It should also be understood that the term *differential amplifier* refers to a single ended op amp configured as a differential amplifier, as opposed to a fully differential op amp configured as a differential amplifier, which is covered separately.

Op amp instrumentation amplifiers have been the mainstay of high accuracy DC instrumentation for decades. The familiar three op amp topology of Figure B.1 has the advantage of high input impedance on both inputs, allowing the designer to interface to sources such as Wheatstone bridges that have relatively high source impedance. The instrumentation amplifier has high gain and is inherently balanced, which also contributes to its popularity.

An instrumentation amplifier is a type of differential amplifier using two input op amps to isolate the source from the input impedance of the differential output stage.

There is a new use for differential amplifiers. They are gaining popularity due to differential data and analog transmission down balanced lines. The traditional instrumentation amplifier and difference amplifier products are too slow to handle these high speed requirements, so new design techniques are required. High speed data can be handled by line receiver products, this appendix focuses on high speed analog.

Balanced line transmission requires termination. This negates the need for high input impedance afforded by the instrumentation amplifier topology of Figure B.1. It allows

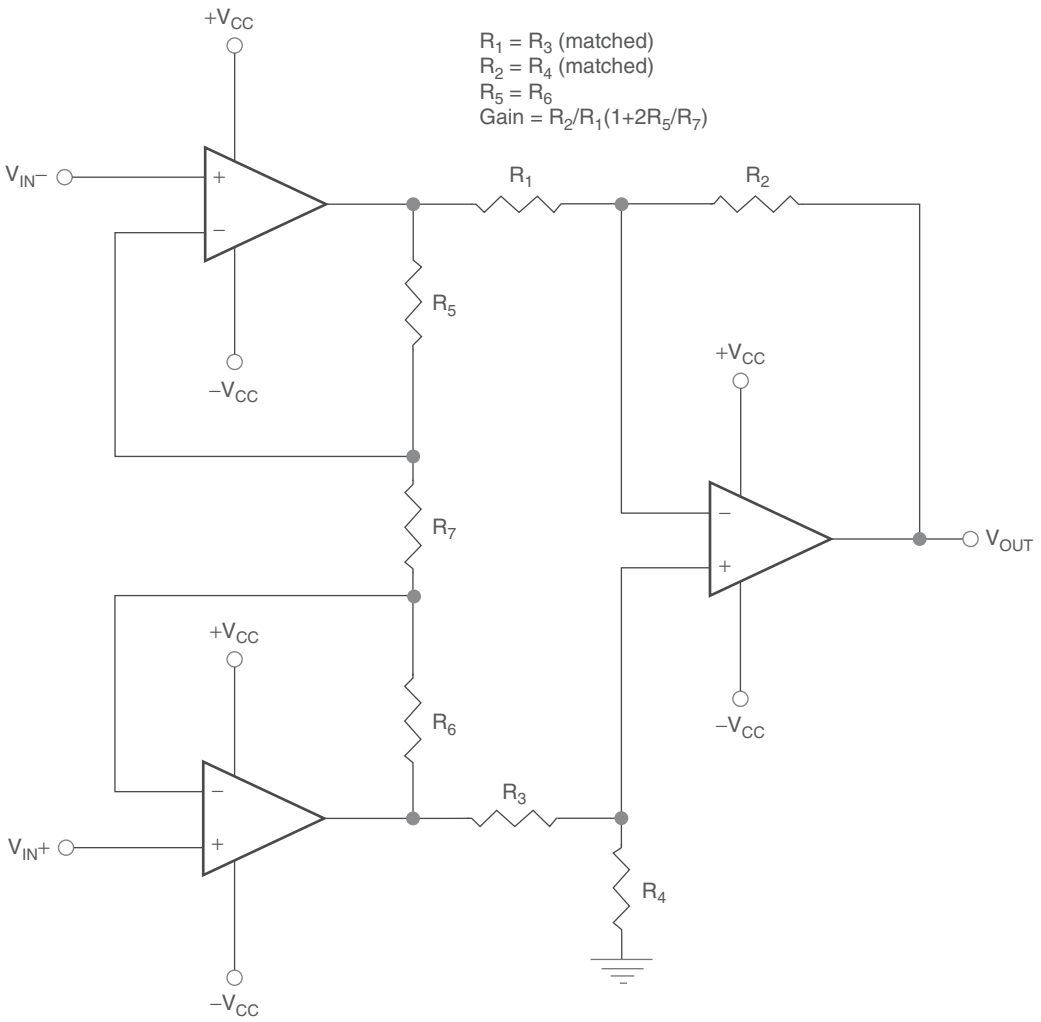


Figure B.1: Instrumentation amplifier.

the designer to delete the two input op amps and implement a differential amplifier consisting of only the third (output) amplifier. There is an additional benefit: The elimination of the two input amplifiers and their associated slew rate limitations allows the one remaining amplifier to receive faster analog signals. The drawback with this system comes with its termination: How does the designer assure proper termination for the balanced line?

B.2 Terminating a Differential Amplifier

To begin with, consider the terminated system shown in Figure B.2.

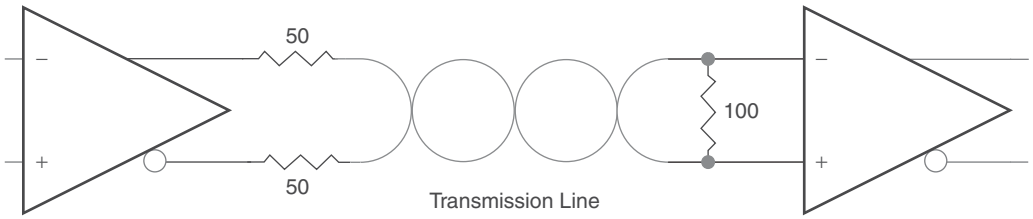


Figure B.2: Data transmission system.

In this system, differential analog data are driven into two 50 Ω resistors to match a transmission line impedance of 100 Ω. At the far end of the transmission line, a 100 Ω termination resistor completes the termination, and the terminated input is applied to a receiver.

Next, assume that the balanced line termination can be grounded at its center point; that is, a single fixed resistor that is normally placed from one signal polarity to the other can be tapped in the middle and connected to ground as shown in Figure B.3.

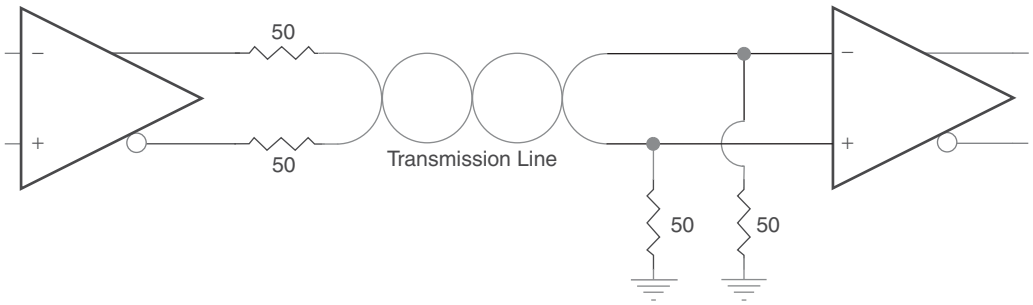


Figure B.3: Modified data transmission system.

Admittedly, this cannot be done in some applications, in particular when the ground at the receiver contains a lot of noise. In practice, however, the line should be

balanced, with equal and opposite voltage swings in each conductor. This means that the midpoint of the signal is at 0 V by definition, no matter what the signal level is. Also, a perfect receiver has infinite common mode rejection. No matter what common mode voltage appears on the inputs (due to the midpoint connection to ground), it is rejected by the receiver. Modern op amps can be chosen that have very good common mode rejection, so this is a good assumption.

Figure B.4 shows the schematic of the proposed high speed receiver. A 100 Ω line impedance is assumed, because it is a common value of line impedance for cables such as Category 5, 5A, and 6. The input signal is represented by two identical and opposite ideal voltage sources V_1 and V_2, each in series with a 50 Ω resistor (for a total of 100 Ω source impedance).

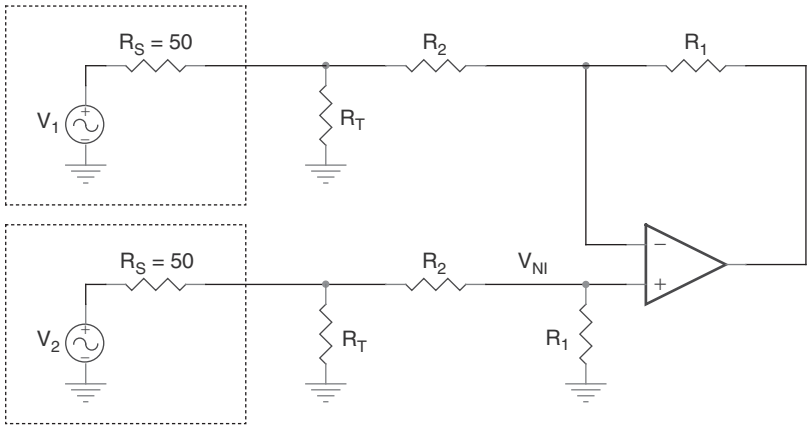


Figure B.4: Differential receiver.

For the receiver to be balanced,

- R_1 top $= R_1$ bottom.
- R_2 top $= R_2$ bottom.
- R_T top $= R_T$ bottom.

From superposition, the gains on V_1 and V_2 can be calculated separately, then summed. Therefore, each polarity of the signal is analyzed separately and the results summed.

B.3 Inverting Side

Make $V_2 = 0$.

Gain is the product of a voltage divider and the normal inverting gain equation. The voltage divider is composed of R_S and R_T in parallel with R_2:

$$-\frac{V_{\text{OUT}}}{V_1} = \frac{R_2 \| R_T}{R_S + R_2 \| R_T} \times \frac{R_1}{R_2}$$

$$= \frac{\dfrac{R_2 \times R_T}{R_2 + R_T}}{R_S + \dfrac{R_2 \times R_T}{R_2 + R_T}} \times \frac{R_1}{R_2}$$

$$= \frac{\dfrac{R_1 \times R_T}{R_2 + R_T}}{R_S + \dfrac{R_2 \times R_T}{R_2 + R_T}}$$

$$= \frac{\dfrac{R_1 \times R_T}{R_2 + R_T}}{R_S \times \dfrac{R_2 + R_T}{R_2 + R_T} + \dfrac{R_2 \times R_T}{R_2 + R_T}}$$

$$= \frac{R_1 \times R_T}{R_S(R_2 + R_T) + R_2 \times R_T}$$

$$\frac{V_{\text{OUT}}}{V_1} = \frac{-R_1 \times R_T}{R_S \times R_2 + R_S \times R_T + R_2 \times R_T}$$

Therefore,

$$V_{\text{OUT}} = \frac{-V_1 \times R_1 \times R_T}{R_S \times R_2 + R_S \times R_T + R_2 \times R_T}$$

B.4 Noninverting Side

Make $V_1 = 0$.

The noninverting side also has a voltage divider on the input. To simplify matters, first calculate the gain on the voltage at the noninverting input V_{NI}. The gain on this voltage is the normal noninverting gain:

$$
\begin{aligned}
V_{OUT} &= V_{NI} \times \left(1 + \frac{R_1}{R_2 + R_S \| R_T}\right) \\
&= V_{NI} \times \left(1 + \frac{R_1}{R_2 + \dfrac{R_S \times R_T}{R_S + R_T}}\right) \\
&= V_{NI} \times \left(1 + \frac{R_1}{R_2 \times \dfrac{R_S + R_T}{R_S + R_T} + \dfrac{R_S \times R_T}{R_S + R_T}}\right) \\
&= V_{NI} \times \left(1 + \frac{R_1 \times (R_S + R_T)}{R_2 \times R_S + R_2 \times R_T + R_S \times R_T}\right) \\
&= V_{NI} + \frac{V_{NI} \times R_1 \times (R_S + R_T)}{R_2 \times R_S + R_2 \times R_T + R_S \times R_T} \\
&= \frac{V_{NI} \times (R_2 \times R_S + R_2 \times R_T + R_S \times R_T) + V_{NI} \times R_1 \times (R_S + R_T)}{R_2 \times R_S + R_2 \times R_T + R_S \times R_T} \\
&= \frac{\begin{array}{c} V_{NI} \times R_2 \times R_S + V_{NI} \times R_2 \times R_T + V_{NI} \times R_S \times R_T \\ + V_{NI} \times R_1 \times R_S + V_{NI} \times R_1 \times R_T \end{array}}{R_2 \times R_S + R_2 \times R_T + R_S \times R_T}
\end{aligned}
$$

Therefore,

$$
V_{OUT} = V_{NI} \times \frac{R_2 \times R_S + R_2 \times R_T + R_S \times R_T + R_1 \times R_S + R_1 \times R_T}{R_2 \times R_S + R_2 \times R_T + R_S \times R_T}
$$

Next, calculate V_{NI} from the voltage divider rule. There are two voltage dividers on V_2: one composed of R_S and the parallel combination of $R_T\Pi(R_1 + R_2)$, and the second composed of R_1 and R_2.

First, define $R_P = R_T\Pi(R_1 + R_2)$:

$$V_{\mathrm{NI}} = V_2 \times \left(\frac{R_P}{R_S + R_P}\right) \times \left(\frac{R_1}{R_1 + R_2}\right)$$

Substituting for R_P,

$$V_{\mathrm{NI}} = V_2 \times \left(\frac{\dfrac{R_T \times (R_1 + R_2)}{R_T + R_1 + R_2}}{R_s + \left(\dfrac{R_T \times (R_1 + R_2)}{R_T + R_1 + R_2}\right)}\right) \times \frac{R_1}{R_1 + R_2}$$

$$= V_2 \times \left[\frac{R_T \times R_1}{R_s \times (R_T + R_1 + R_2) + R_T \times (R_1 + R_2)}\right]$$

Therefore,

$$V_{\mathrm{NI}} = \frac{V_2 \times R_1 \times R_T}{R_s \times R_T + R_s \times R_1 + R_s \times R_2 + R_T \times R_1 + R_T \times R_2}$$

Now, substitute the expression for V_{NI} into the expression for the noninverting gain:

$$V_{\mathrm{OUT}} = \frac{V_2 \times R_1 \times R_T}{R_S \times R_T + R_S \times R_1 + R_S \times R_2 + R_T \times R_1 + R_T \times R_2} \times \frac{R_2 \times R_S + R_2 \times R_T + R_S \times R_T + R_1 \times R_S + R_1 \times R_T}{R_2 \times R_S + R_2 \times R_T + R_S \times R_T}$$

and the large numerator and denominator cancel out; therefore,

$$V_{\mathrm{OUT}} = \frac{V_2 \times R_1 \times R_T}{R_2 \times R_S + R_2 \times R_T + R_S \times R_T}$$

B.5 Differential Output

To get the differential output voltage, just add together the inverting and noninverting gains using the superposition rule:

$$V_{\text{OUT}} = \frac{V_2 \times R_1 \times R_T}{R_2 \times R_S + R_2 \times R_T + R_S \times R_T} - \frac{V_1 \times R_1 \times R_T}{R_S \times R_2 + R_S \times R_T + R_2 \times R_T}$$

$$= \frac{(V_2 - V_1) \times R_1 \times R_T}{R_2 \times R_S + R_2 \times R_T + R_S \times R_T}$$

Therefore,

$$\frac{V_{\text{OUT}}}{V_2 - V_1} = \frac{R_1 \times R_T}{R_S \times R_2 + R_S \times R_T + R_2 \times R_T}$$

This equation is a bit formidable looking. Fortunately, three out of the five variables are known:

- R_S is the source resistance of the line (usually half of the line impedance, since it is tapped in the middle; so for a 100 Ω line, R_S is 50 Ω on each side, for a total of 100 Ω).
- The gain is known: $V_{\text{OUT}}/(V_2 - V_1)$.
- The value of R_1 is known, because the data sheet usually specifies a value of feedback resistance for maximum stability.
- This leaves only two unknowns: the input resistance R_2 and proper termination resistance R_T. The calculation, therefore, becomes a goal seeking problem in two variables. A Javascript design utility has been located on the Texas Instruments Web site (ti.com) for the convenience of the designer.

B.6 Testing the Result

The preceding expressions were tested at a gain of 0.5 and 1.

B.6.1 Gain of 0.5

$$\frac{V_{OUT}}{V_2 - V_1} = \frac{R_1 \times R_T}{R_S \times R_2 + R_S \times R_T + R_2 \times R_T}$$

$$= \frac{249 \times 61.9}{50 \times 249 + 50 \times 61.9 + 249 \times 61.9}$$

$$= \frac{15{,}413.1}{12{,}450 + 3{,}095 + 15{,}413.1} = \frac{15{,}413.1}{30{,}958.1} = 0.498 = -6.058 \text{ dB}$$

For inverting input with noninverting input grounded, simulation and lab results are shown in Figure B.5.

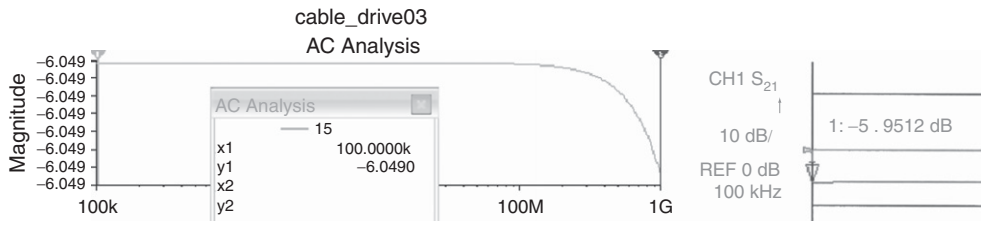


Figure B.5: Simulation and lab results for inverting input, gain of 0.5.

For noninverting input with inverting input grounded, simulation and lab results are shown in Figure B.6.

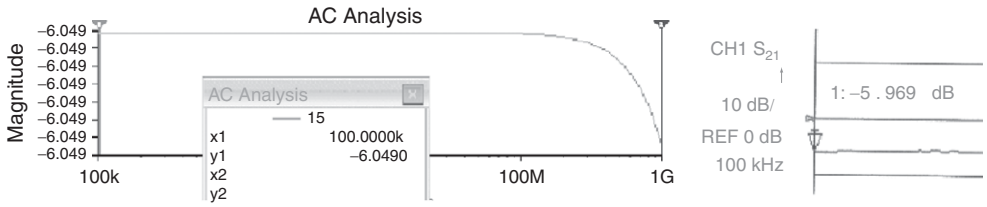


Figure B.6: Simulation and lab results for noninverting input, gain of 0.5.

B.6.2 Gain of 1

Next, at a stage gain of 1,

$$\frac{V_{OUT}}{V_2 - V_1} = \frac{R_1 \times R_T}{R_S \times R_2 + R_S \times R_T + R_2 \times R_T}$$

$$= \frac{499 \times 61.9}{50 \times 249 + 50 \times 61.9 + 249 \times 61.9}$$

$$= \frac{30{,}888.1}{12{,}450 + 3{,}095 + 15{,}413.1} = \frac{30{,}888.1}{30{,}958.1} = 0.998 = -0.02 \text{ dB}$$

For inverting input with noninverting input grounded, simulation and lab results are shown in Figure B.7.

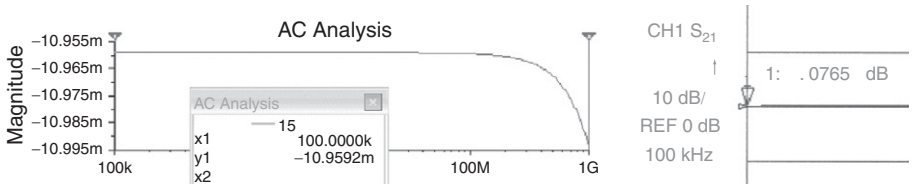


Figure B.7: Simulation and lab results for inverting input, gain of 1.

For noninverting input with inverting input grounded, simulation and lab results are shown in Figure B.8.

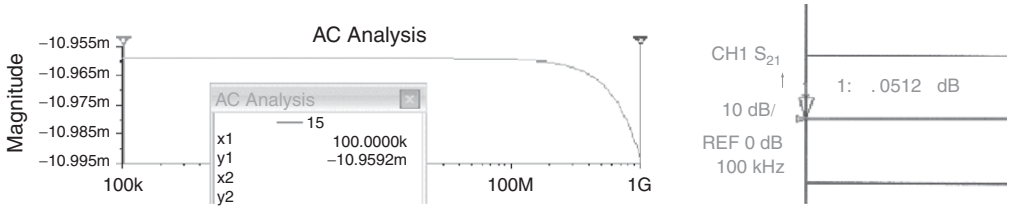


Figure B.8: Simulation and lab results for noninverting input, gain of 1.

Again, pretty close. At this point, it is important to point out that, when the inputs are equal in magnitude and opposite in polarity, the stage gain is double the results seen here. In other words, stage gain on a differential input is double the stage gain when only one input is used.

Index

In this index individual filters, converters, etc. are entered by their initialism, i.e., BPF (bandpass filter).

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