Analog IC−Design

Lab 3

In the third lab we will simulate the properties of an operational amplifier (opamp). The simulation setups are explained in the included text: "Simulation and Measurement of Op Amps"

Objectives:

1. Create and simulate the differential amplifier section of Figure 1.
2. Expand the schematic to create the entire opamp of Figure 1 and simulate the following properties:
   - Offset voltage
   - Open and closed loop frequency response and finite gain
   - Input Common Mode Range (CMR)
   - Common Mode Rejection Ration (CMRR)
   - Slew rate and settling time
   - Power Supply Rejection Ratio (PSRR)

1. Differential amplifier

Figure 1 shows a differential amplifier which is used as the first gain stage in the operational amplifier. Create it with Cadence Schematic Editor and create the netlist with analog artist. Remember to include the model file **mtcn0u35.mod** and add the power supply voltages to the netlist. Use V_{DD} = 1.5 V and V_{SS} = −1.5 V. See the earlier labs for details.

Find out the output resistance and the gain of the differential amplifier by connecting the other input to the ground and the other to an AC voltage source **Vin** (use an AC value of 1 V). Then run the small signal transfer function analysis:

.TF V(output_node) Vin

Output resistance =

Amplifier gain =

2. Opamp

Expand the differential amplifier circuit to create the entire opamp schematic of Figure 1 and create a component symbol for the opamp:

Design −> Create Cellview −> From Cellview...

Save the component and create a new cellview to use as a testbench for the opamp. Add the opamp to the cellview as **symbol**. Create input and output **pins** for the opamp symbol:

Add −> Pin...

Add the V_{DD} and V_{SS} voltage sources by creating two DC voltage sources (valued 1.5 V and −1.5 V). Connect the negative nodes to gnd! and connect short wires to the positive nodes and name them vdd! and vss! Save the cellview. You should have a cellview that looks something like Figure 2. How can you make the opamp symbol triangular? (Hint! symbol generation options) You can now use this cellview to set up the simulations.

You now have **different levels of hierarchy** in your design. You have a testbench schematic with a symbol level view of the opamp. You can descend in the hierarchy of your cellview to view or edit your opamp schematic by selecting the opamp symbol and the selecting

Design −> Hierarchy −> Descend Edit...

This way you can edit the schematic or the symbol of the opamp without leaving your testbench cellview. To return to an upper level in the hierarchy select:

Design −> Hierarchy −>Return

3. Opamp offset voltage

Take a look at Figure 8.5−4 of the material included with this lab. Edit your testbench schematic otherwise according to this figure, except add a dummy voltage source (V (DC) = 0) to the feedback loop. This voltage source doesn't do anything but without it Analog Artist will not let you generate the netlist! This is called a **voltage follower** configuration. Create the netlist.

First sweep the input voltage from −100 mV to 100 mV with 0.1 mV steps and plot the output. Zoom in to find out the offset voltage.

Now set the input voltage to 0 V and run the simulation again and take a look at the hspice output. Find the operating point information and find out the output voltage. This is the **offset voltage** value. Compare it to the previous plot.

Offset voltage =

Do you think that this simulated offset voltage accurately represents the true offset of an opamp manufactured on silicon?

3.1 Offset compensation

Because the offset voltage V_{os} is the output voltage that is created with an input of 0 V, you can compensate for it by connecting a voltage source with a value of $-V_{os}$ to the positive input of the opamp. **Use this compensation in all the following circuits and simulations**, if not told otherwise.

4. Transfer function analysis

After compensating for the offset voltage, remove the feedback loop and connect the negative input node to the ground. Again you have to do this is by using the same zero valued voltage source (Vtest), only this time between the negative input and ground. Add a .TF simulation to the netlist, and remember to apply an AC voltage to the positive input node. Find out the **gain**, **output resistance** and **total power dissipation** from the hspice output.

Gain=

R_{out} =

Power dissipation =

Examine the hspice output further. Are the transistors in saturation?

5. Frequency Response

5.1 Open loop frequency response

The open loop gain of an ideal opamp is infinite. In reality the gain is never infinite, just very large. To simulate the frequency response of the opamp in an open loop configuration, connect the positive input node to the ground through a voltage source (remember the offset compensation!) and use a voltage source in the negative feedback loop (Vtest) as an AC signal source. The AC source in the feedback loop works as an open circuit at DC, thus opening the loop. Add a 5 pF load capacitance between the output and ground.

Now do an AC frequency sweep from 1 Hz to 10 GHz and plot the DC−gain and phase difference between the output and the negative input of the opamp:

.PRINT VDB(out_node, neg_in_node) VP(out_node, neg_in_node)

Plot the VdB and phase curves in their own panels. Find out the **phase margin** from the plotted curves. Is it large enough to guarantee the stability of the opamp over a frequency range of up to 10 MHz ?

Gain (DC) =

Phase margin =

Now remove the compensation capacitance C_0 (3p) from the opamp and run the same AC−sweep again. How are the gain and phase margin affected?

5.2 Closed loop frequency response

To plot the closed loop frequency response, set the feedback voltage source to a DC value of 0 V (closing the loop at DC). This is the same voltage follower configuration that was used when the offset voltage of the amplifier was determined. Use the same 5 pF load capacitance. Add an AC signal to the positive input of the opamp:

VIN pos_in_node 0 DC V_{offset} *AC 1*

Plot the output magnitude and phase:

.PRINT VDB(out_node) VP(out_node)

6. Input Common Mode Range (CMR)

The input common mode range (CMR) is the input voltage range which results in a linear transfer curve at the output, i.e. the output slope is 1. To simulate the input common mode range of the opamp, use again the voltage follower configuration (Figure 8.5−10). Do a DC sweep of the input from −2 V to 2 V with a step of 0.1 mV.

Plot the output voltage. Create the derivative of the output voltage by using the *Expression* tool in Awanwaves. Plot the derivative in a new panel and determine the approximately linear range.

CMR =

7. Common Mode Rejection Ratio (CMRR)

Common mode rejection ratio is the amount with which the amplifier attenuates a common mode signal, i.e. An identical signal applied simultaneously to both inputs. Because of the differential amplifier stage at the input, an ideal opamp would have infinite common mode attenuation.

Create the circuit of Figure 8.5−7. Voltages V_{cm} are AC sources with a magnitude of 1 V. Sweep the frequency from 10 Hz to 10 GHz. Plot the output magnitude and phase in dB. Use a 5 pF load capacitance.

CMRR (DC) =

8. Slew Rate

Connect the opamp again in the voltage follower configuration (Figure 8.5−14.) and use the same 5 pF load capacitance as before. To measure the slew rate and settling time of the opamp, you need a pulse input voltage. Create it with a **PWL** (PieceWise Linear) voltage source:

Vname node1 node2 PWL time1 value1 time2 value2 time3 value3 ... R repeat TD delay

Create an input pulse with rise and fall times of 2 ns, a width of 10 μs and minimum and maximum values of −500 mV and +500 mV. The delay and repeat times are not compulsory. Run a transient simulation and plot the output voltage. To find the slew rate, use:

Measure −> Point

in Avanwaves and determine the slope of the output as V/ μs during the rise and fall of the output voltage. The settling time is the time measured from the point when the output starts to rise (or fall) to the point when the output has settled within approximately ± 1 % of the final value.

Slew Rate (rise) =

Slew Rate (fall) =

Settling Time =

9. Power Supply Rejection Ratio (PSRR)

Power supply rejection ratio characterizes the amplifiers tendency to resist undesired error signals carried by the power supplies. Use again the circuit setup of Figure 8.5−4 but this time with the positive input grounded the whole time, i.e. with no AC−input to the positive input node, just offset compensation.

To measure the power supply rejection ratio we will introduce AC fluctuation into the power supplies V_{DD} and V_{SS} . First simulate $PSRR^+$ by keeping V_{SS} constant and applying an AC voltage to V_{DD} :

Vdd VDD! 0 DC 1.5 AC 1

Now use the *.PRINT* function to plot the output voltage magnitude in dB. The Y−axis values of the plot will be negative, this is a case of attenuation.

Repeat the simulation with an error signal in the V_{SS} while keeping V_{DD} constant.

$PSRR^+$ (DC) =

$PSRR^-$ (DC) =

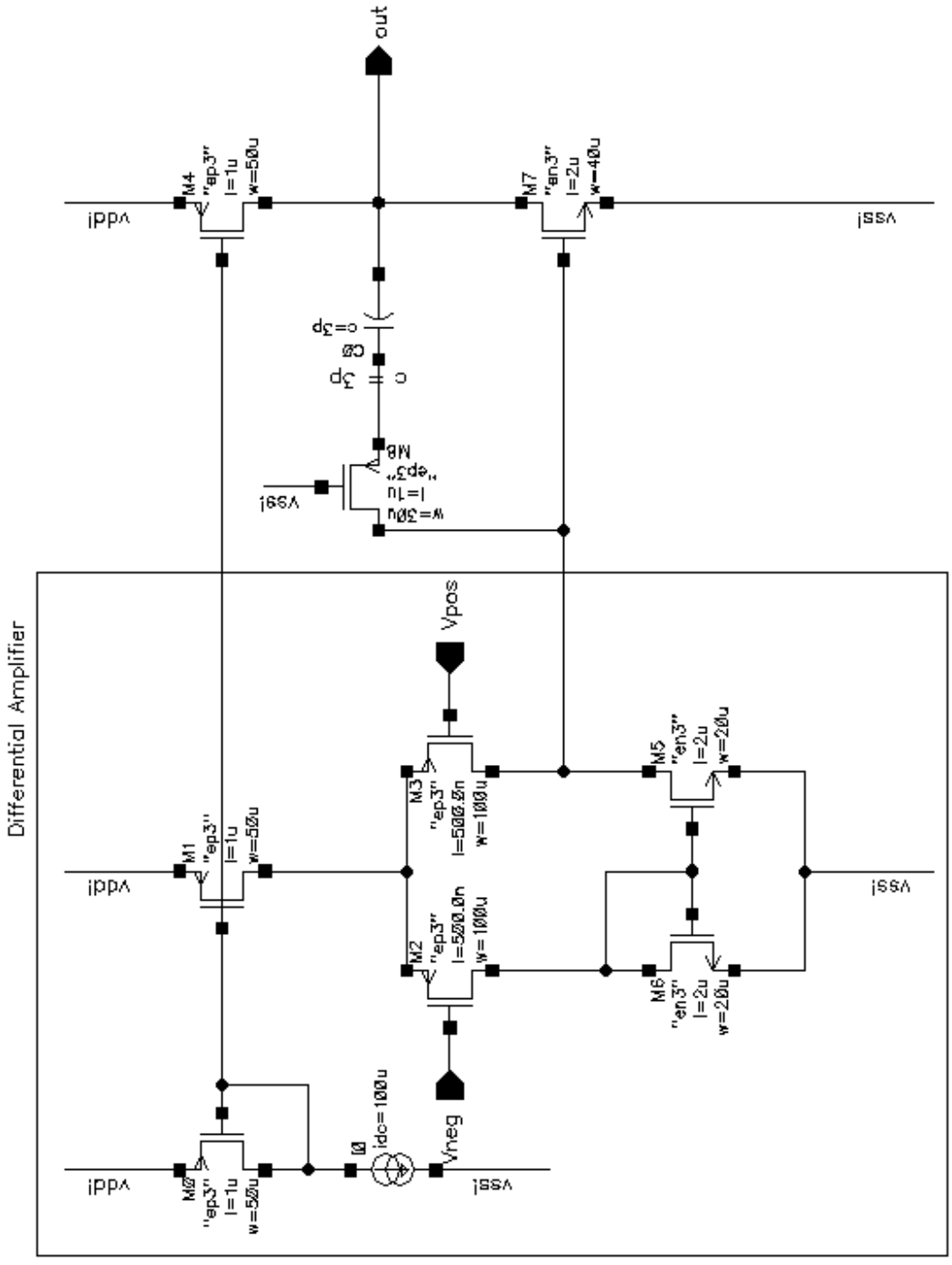
out
M4
"ep3"
l=1u
w=50u
M7
"en3"
l=2u
w=40u
vddi
vssi
c = 3p
C0
c=3p
M8
"ep3"
l=1u
w=30u
vssi
Differential Amplifier
Vpos
M3
"ep3"
l=500.0n
w=100u
M5
"en3"
l=2u
w=20u
M1
"ep3"
l=1u
w=50u
vddi
vssi
M2
"ep3"
l=500.0n
w=100u
M6
"en3"
l=2u
w=20u
idc=100u
I0
Vneg
M0
"ep3"
l=1u
w=50u
vddi
vssi

figure 1

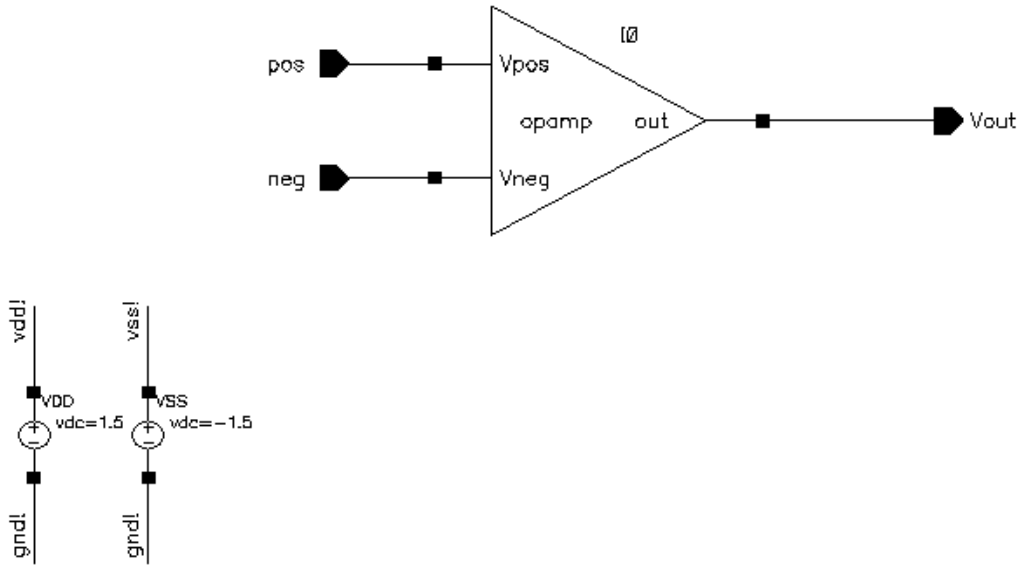
pos
neg
Vpos
Vneg
opamp
out
Vout
vdd!
vss!
VDD
VSS
vdc=1.5
vdc=-1.5
gnd!
gnd!

figure 2