Chapter 5 Midband Analysis of CMOS Operational Amplifiers (OP AMPs)

§5-1 General Considerations

§5-1.1 General Procedures to analyze an OP AMP IC

1. Identify all the biasing circuits (current & voltage).
2. Identify all the protection circuits and then take them away.
3. Calculate all the operating currents and voltages.
4. Trace the signal path and identify the amplifier, buffer, level shifter, and output driver configurations.
5. Calculate the midfrequency gain.
6. Identify the compensation circuits.
7. Calculate the high-frequency response.
8. Perform the SPICE simulations to obtain the performance parameters.

§5-1.2 Some important OP AMP Specifications

1. Open-loop differential gain $A_d(\omega)$.
2. Open-loop common-mode gain $A_c(\omega)$.
3. Common-mode rejection ratio (CMRR)

$$CMRR(\omega) \equiv \left|\frac{A_d(\omega)}{A_c(\omega)}\right| = \left[\left.\frac{\partial V_{io}}{\partial V_{ic}}\right|_{V_o=0}\right]^{-1}$$

where V_{io} is the input offset voltage

V_{ic} is the input common-mode voltage

4. Output swing.

5. Unity-gain frequency f_u.

6. Upper 3-dB frequency $f_{3\text{-}dB}$.

7. Power-supply rejection ratio (PSRR).

$$PSRR^{+}(\omega) \equiv \left| \frac{A_d(\omega)}{\frac{\partial V_o}{\partial V_{DD}}(\omega)} \right| = \left[\frac{\partial V_{io}}{\partial V_{DD}}(\omega)\Big|_{V_o=0} \right]^{-1}$$

$$PSRR^{-}(\omega) \equiv \left| \frac{A_d(\omega)}{\frac{\partial V_o}{\partial V_{SS}}(\omega)} \right| = \left[\frac{\partial V_{io}}{\partial V_{SS}}(\omega)\Big|_{V_o=0} \right]^{-1}$$

8. Slew rate and settling time

Slew rate: Maximun $\frac{d}{dt}v_o$ in an unity-gain close-loop OP Amp with a fixed step input under maximum load.

Settling time: The time required for the OP AMP in an unity-gain closed loop to reach ~% of its final value with a fixed step input under maximum load.

9. Linearity and harmonic distortion

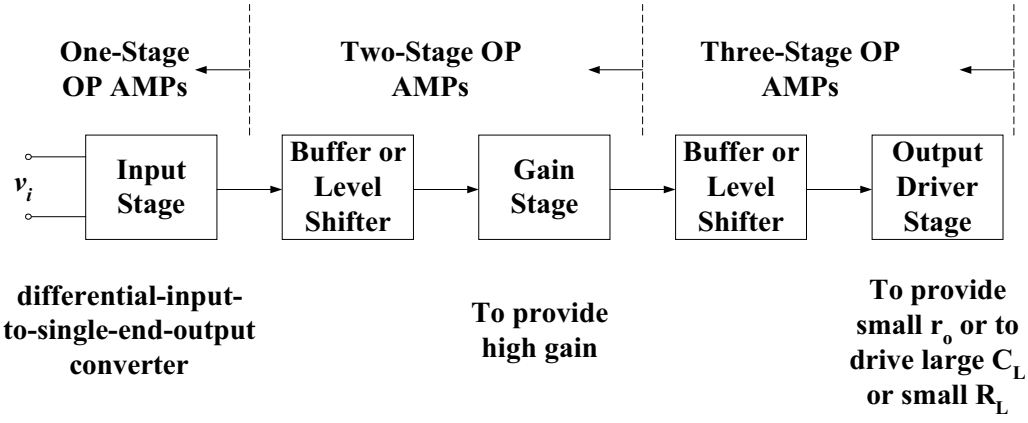
Usually dominated by the output stage.

Closed-loop characteristics.

10. Equivalent input noise and input offset

Usually dominated by the input stage.

§5-1.3 General Block Diagram of an OP AMP



§5-2 One-Stage (Single-Stage) CMOS OP AMPs

§5-2.1 Single-ended-output OP AMPs

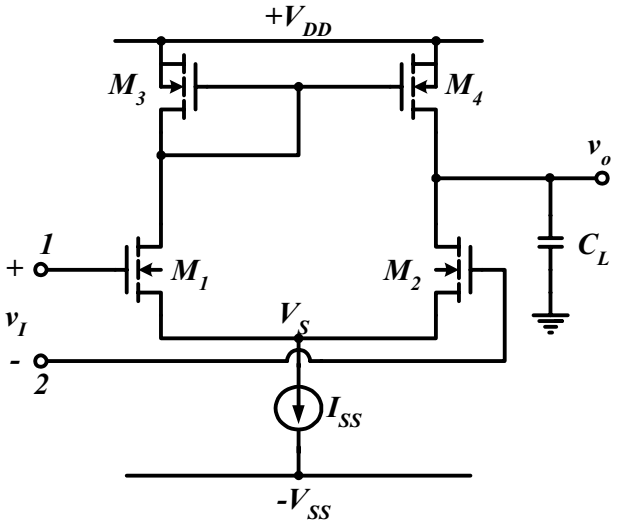
1. Simple OP AMP

* Inverting input: 2

Noninverting input: 1

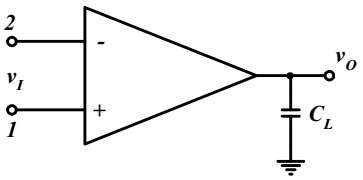
* Open-loop voltage gain

$$\equiv \frac{v_o}{v_i} = A_d \quad = -g_{mN}(r_{dsP} \,//\, r_{dsN})$$



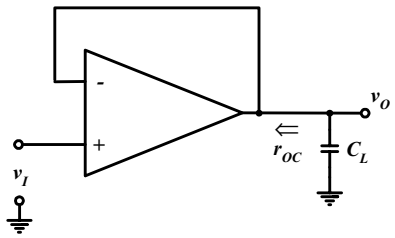
* Open-loop output resistance

$$r_o = r_{dsP} \;//\; r_{dsN}$$



Close-loop output resistance

$$r_{oc} \cong \frac{r_{dsP} \,//\, r_{dsN}}{1 + g_{mN}(r_{dsP} \,//\, r_{dsN})} \cong \frac{1}{g_{mN}}$$



The closed-loop output resistance is independent of the open-loop output resistance.

* The dominate pole is located at the output with the RC time constant r_oC_L.

* $A_d \sim 100$, Power dissipation ~ μW, $f_u \sim$ MHz.

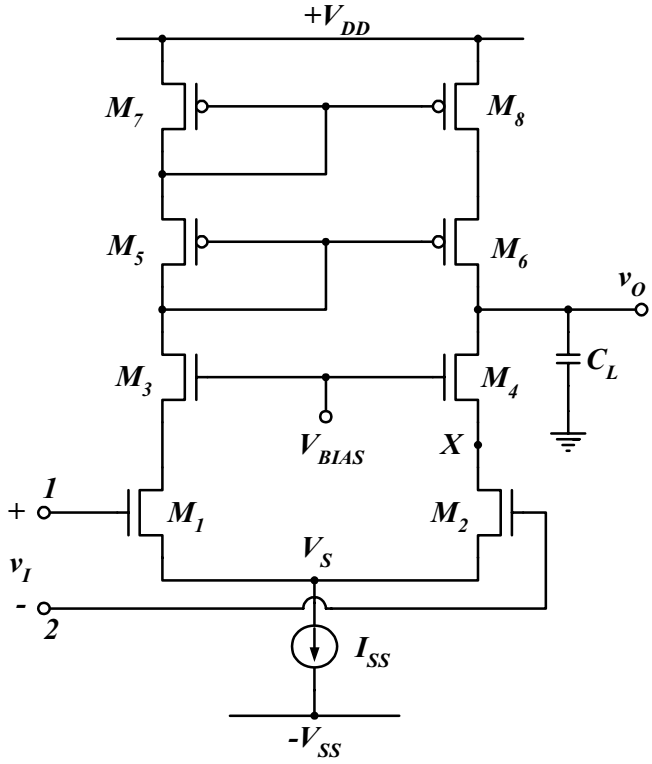
Suitable for small-load internal-use applications.

* Cannot drive heavy load.
* Output swing: $V_{DD} - |V_{DSATP}| \rightarrow -V_{SS} + V_S + V_{DSATN}$

2. Telescopic cascode OP AMP with cascode-current-source load

* Open-loop voltage gain

$$A_d = -g_{mN}(g_{mN} r^2_{dsN} \,//\, g_{mP} r^2_{dsP})$$



* Open-loop

$$r_o = g_{mN} r^2_{dsN} \,//\, g_{mP} r^2_{dsP}$$

Close-loop

$$r_{oc} \cong \frac{1}{g_{mN}}$$

* In the unity-gain feedback, the node 2 is connected to the output node.

$\Rightarrow M_2$ and M_4 sat.

$\Rightarrow V_{o\,min} = V_{BIAS} - V_{TH4}$,

$$V_{o\,max} = V_x + V_{TH2} = V_{BIAS} - V_{GS4} + V_{TH2}$$

$\Rightarrow$ Output swing $= V_{TH2} - (V_{GS4} - V_{TH4}) \le V_{TH2}$

Too small output swing

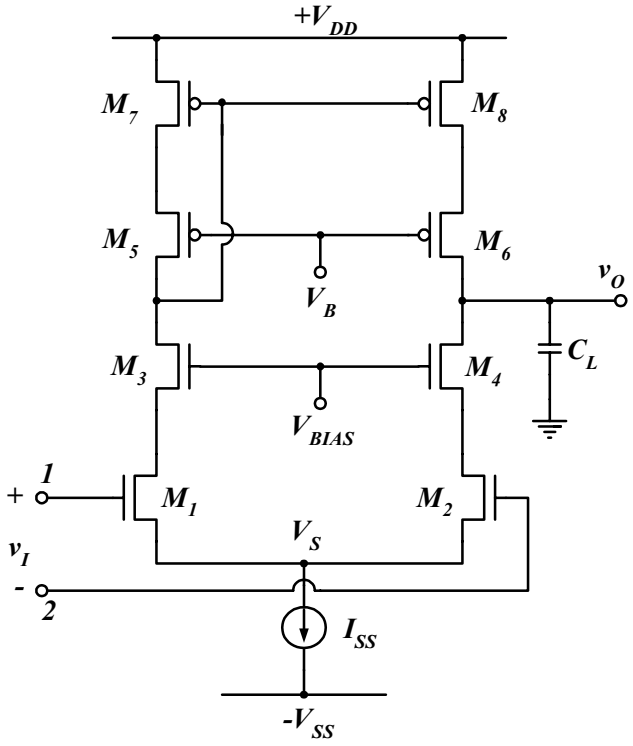
Not suitable for unity gain buffer.

* Limit output swing:

$$V_{DD} - |V_{DSAT8}| - |V_{DSAT6}| \rightarrow -V_{SS} + V_S + V_{DSAT2} + V_{DSAT4}$$

3. Telescopic cascode OP AMP with high-swing cascode-current-source load

* Higher output swing
* Not suitable for unity-gain buffer



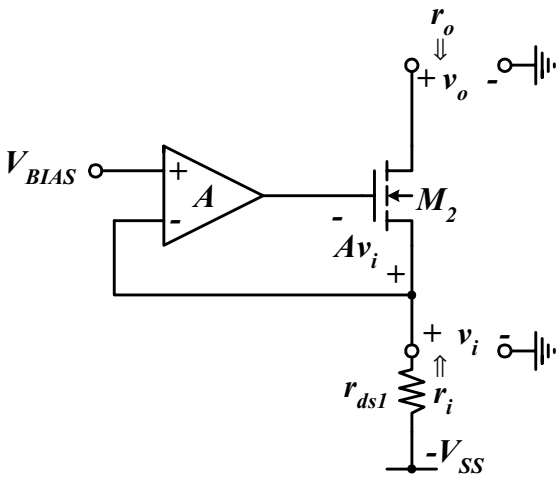
4. Telescopic cascode OP AMP with gain-boosting (or enhanced-output -impedance) circuit

1) Basic concept

* $v_i \rightarrow Av_i \rightarrow i_o = Ag_m v_i$

$$\frac{i_o}{v_i} = Ag_m$$

The transconductance is boosted by A times, $A \sim 100$.



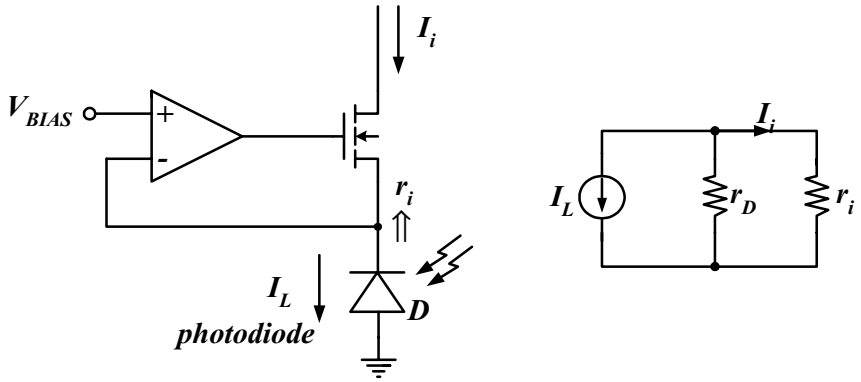
* $r_i \cong \frac{1}{g_m}\frac{1}{A} \sim 100\Omega - 10\Omega$

The input resistance is lowered by A times.

Suitable for current input because of small r_i.

$\Rightarrow$ High injection efficiency

Example:



If the output resistance of D is not large, e.g. r_D=10KΩ,

We need $r_i \le 100\Omega$ to obtain $I_i = I_L \dfrac{10K\Omega}{10K\Omega + r_i} \cong 99\ \%$ of I_L

⇒ 99 % injection efficiency and stable photodiode reverse bias V_{BIAS}

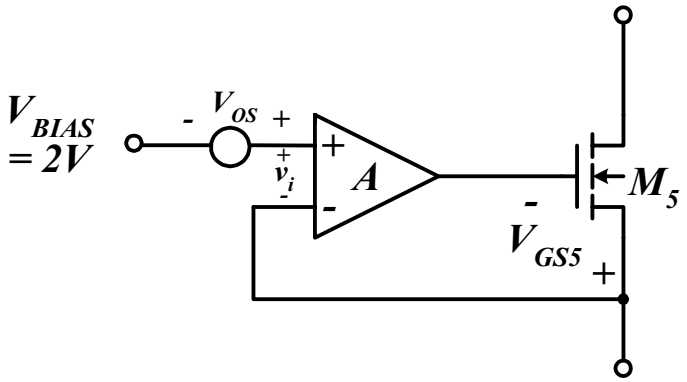
* $r_o \cong (G_{m2} r_{ds1}) r_{ds2} = A g_{m2} r_{ds1} r_{ds2}$

The output resistance is boosted by A times as compared to the cascode structure without A.

No extra cascode device is required

⇒ The swing is not further degraded.

* Offset voltage problem



A = 100, V_{OS} = 0V, V_{GS5} = 1.4V > V_{TH5} = 1.1V,

⇒ v_i = 14mV and M_5 is turned on to provide negative feedback.

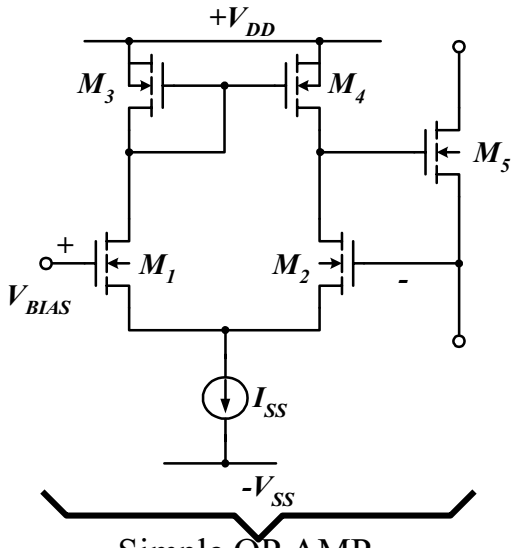
But if V_{OS} = -5mV

$\Rightarrow V_{GS5}$ = 0.9V smaller than V_{TH5}

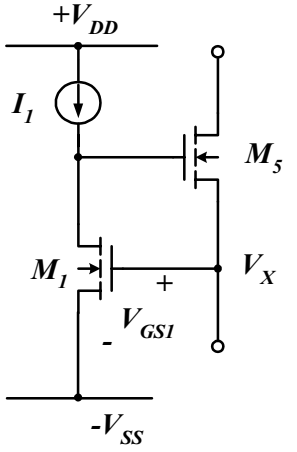
$\Rightarrow M_5$ is off and the circuit fails.

So suitable systematic offset should be introduced to make sure that $V_{OS} > 0$

* Realization



Simple OP AMP

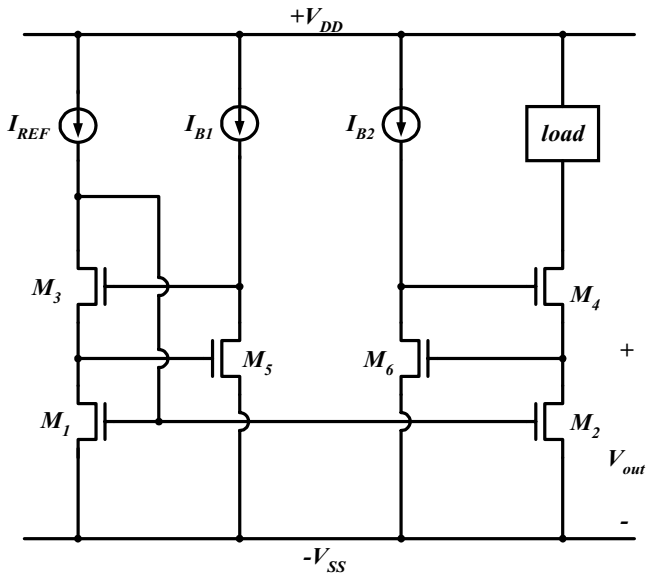


$V_x = V_{GS1} - V_{SS}$ fixed

$A = -g_{m1}(r_{ds1} // r_{o1})$

2) Current mirror with enhanced-output-impedance circuit

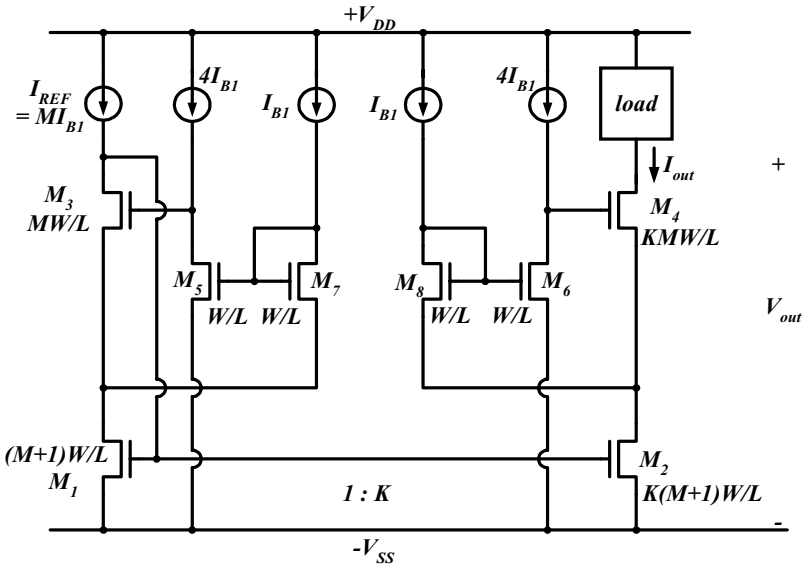
A: The Sackinger implementation



* Low swing
* $r_o = (g_{m4} r_{ds2} r_{ds1})[g_{m6}(r_{ds6} // r_{OB2})]$
* Minimum required V_{out}

  $V_{out} = V_{GS6} + V_{GS4} - V_{TH4}$
* $V_{GS6} = V_{GS5} \Rightarrow V_{DS1} = V_{DS2}$ precise current ratio

B: High-swing implementation



* Add extra devices M_7 and M_8 to decrease V_{DS1} and V_{DS2}.
* $V_{DS1} = V_{GS5} - V_{GS7}$

  $V_{DS2} = V_{GS6} - V_{GS8}$
* High swing

  Min $V_{out} = V_{GS6} - V_{GS8} + V_{GS4} - V_{TH4}$
* $I_{out} = KI_{REF}$

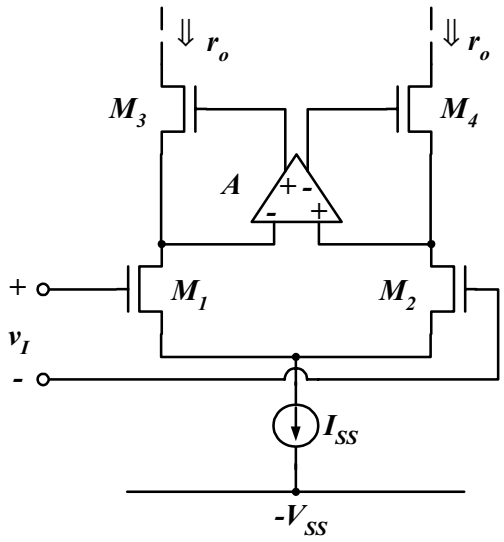
  $V_{DS1} = V_{DS2} \Rightarrow$ precise ratio

3) OP AMPs

A: Using the gain-boosting circuit in cascode amplifier

* $g_{m3} = g_{m4}$ is increased by A times.
* The effective resistance seen by M_1 and M_2 is lowered by A times

  $\Rightarrow$ The gain is lowered by A



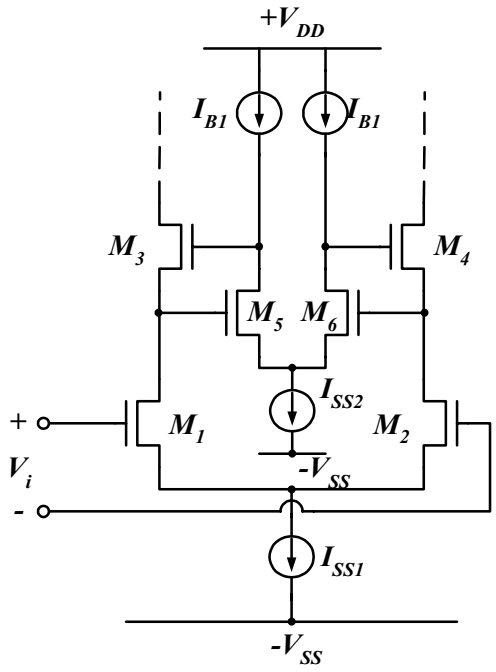
times.

⇒ Has much less Miller capacitance at the input while keeping M_1 and M_2 saturated.

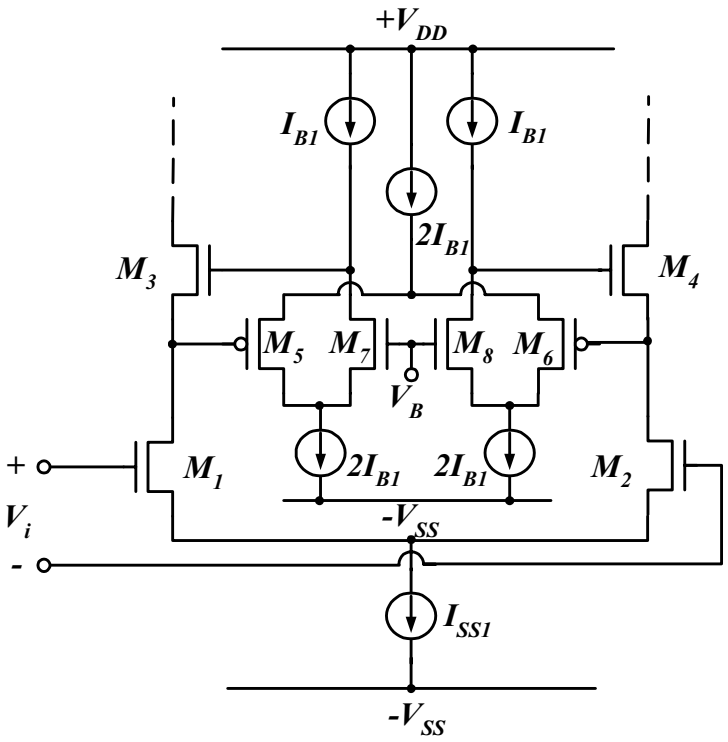
* r_o seen by M_3 and M_4 is increased by A times ⇒ Gain boosting

* Realization

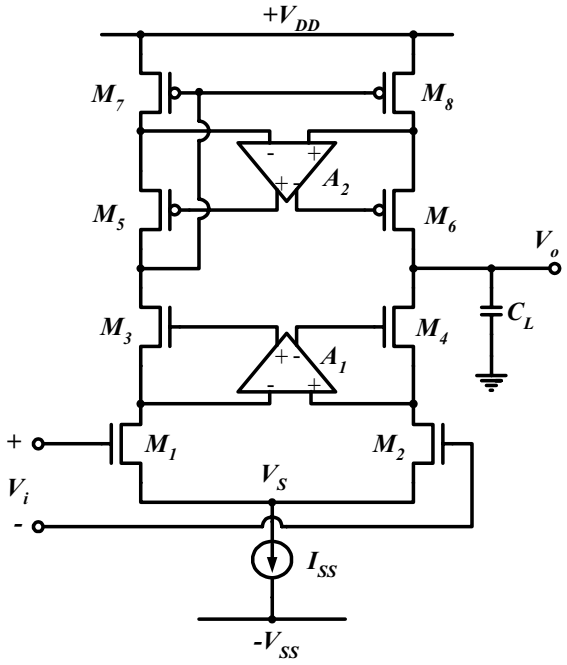
Why I_{SS2} ?



The amplifier A is realized by fully differential folded cascode amplifier

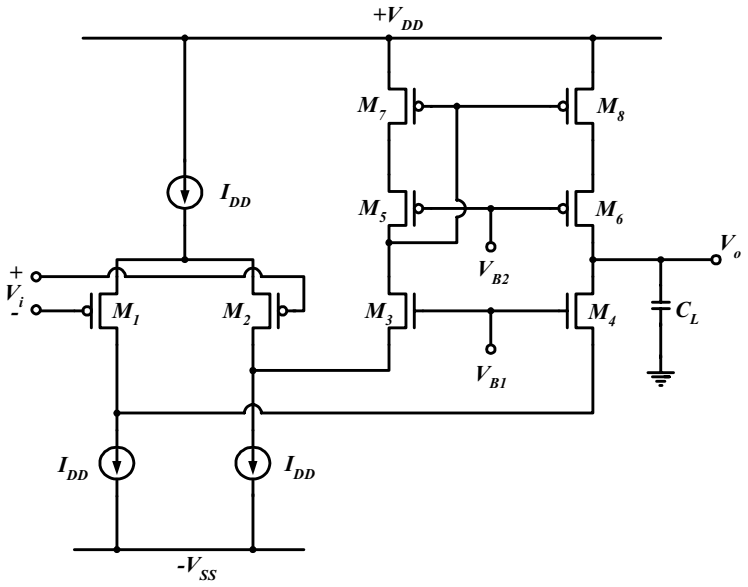


B: Using the gain-boosting circuits in both cascode amplifier and current-mirror load



5. Folded cascode OP AMP

1) PMOS input



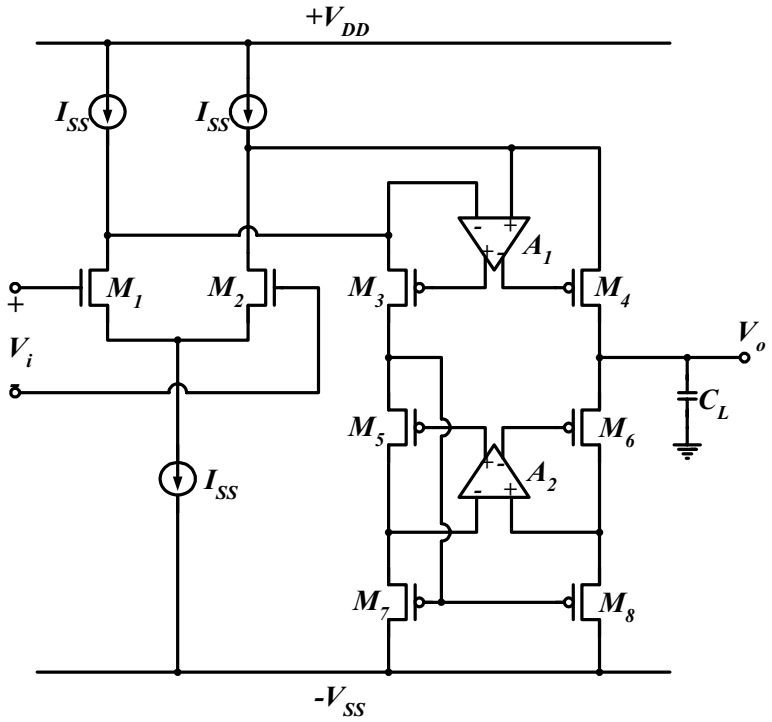
* Higher power dissipation than the telescopic cascode OP AMP.

* Higher input equivalent noise and input offset voltage

∵ More devices are involved.

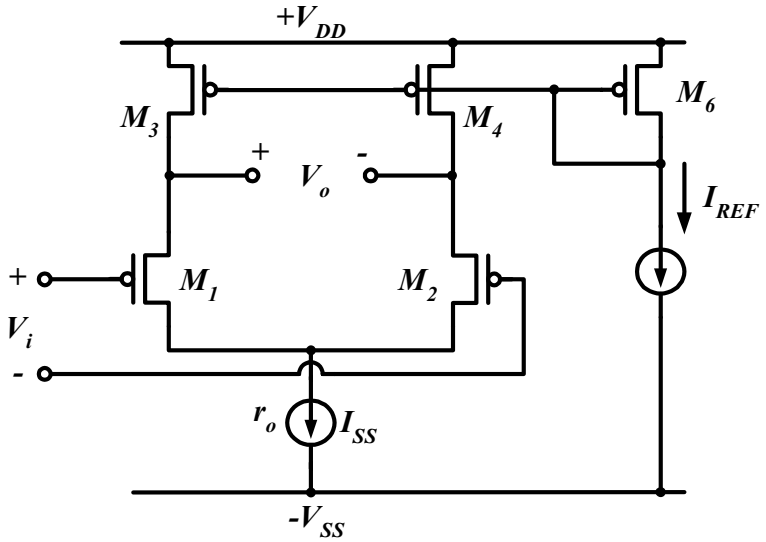
* Higher V_{ICM} range and higher output swing.
* Lower voltage gain as compared with the PMOS-input telescopic cascode OP AMP. Why ?
* Lower r_o

2) With the gain-boosting circuit



§5-2.2 Fully differential OP AMPs

1. Simple OP AMPs

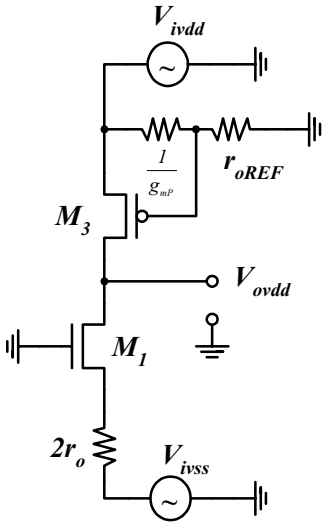


* $A_{dm} \cong -g_{mN}(r_{dsN} \,//\, r_{dsP})$

$$A_{cm\cong} = -\frac{\alpha_1 r_{dsP}}{2r_o}$$

$$CMRR = \frac{\alpha_1 g_{mN}(r_{dsN} // r_{dsP})r_{dsP}}{2r_o}$$

* Power supply noise gain



$$A_{cvddm} \cong +g_{mP}[r_{dsP} //(g_{mN} 2r_o)r_{dsN}][\frac{1}{g_{mP} r_{oREF} + 1}] \cong \frac{r_{dsP}}{r_{oREF}} \cong 1$$

$$A_{cvssm} \cong +(\frac{\frac{1}{g_{mN}}}{2r_o + \frac{1}{g_{mN}}})[g_{mN}(r_{dsN} // r_{dsP})] = \frac{r_{dsN} // r_{dsP}}{2r_o + \frac{1}{g_{mN}}}$$

$$PSRR+ \equiv \frac{|A_{dm}|}{|A_{cvddm}|} = \frac{g_{mN}(r_{dsN} // r_{dsP})}{g_{mP} r_{dsP}}$$

$$g_{mP} > g_{mN} \quad \text{for large } PSRR+$$

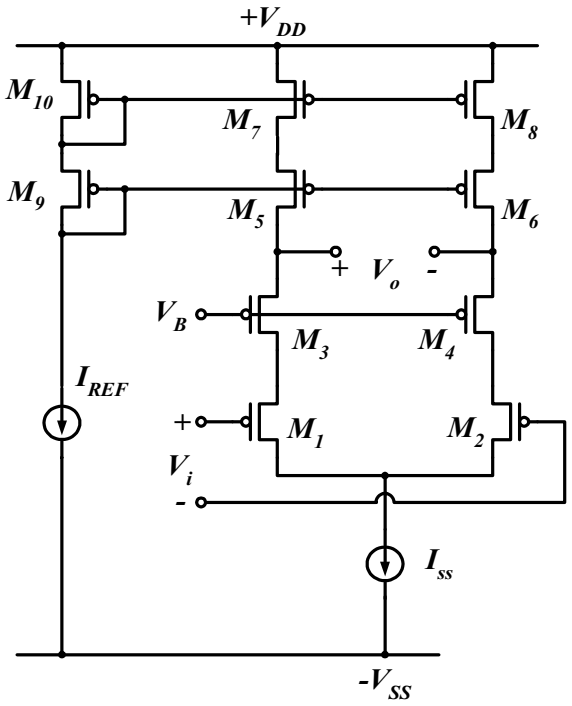
$$PSRR- \equiv \frac{|A_{dm}|}{|A_{cvssm}|} = \frac{g_{mN}(r_{dsN} // r_{dsP})(2r_o + \frac{1}{g_{mN}})}{(r_{dsN} // r_{dsP})} \cong 2g_{mN} r_o$$

$$PSRR- > PSRR+$$

$PSRR+$ for V_{DD} is not high enough.

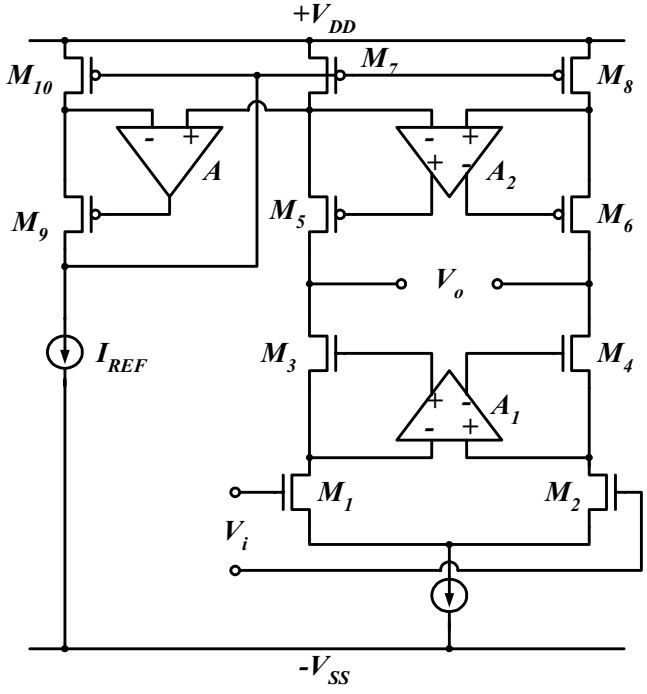
* Commond-Mode Feedback (*CMFB*) is required to decrease A_{cm} and increase *CMRR*. With *CMFB* circuit, *PSRR* ↑.

2. Telescopic cascode OP AMPs with cascode or high-swing cascode current-source load

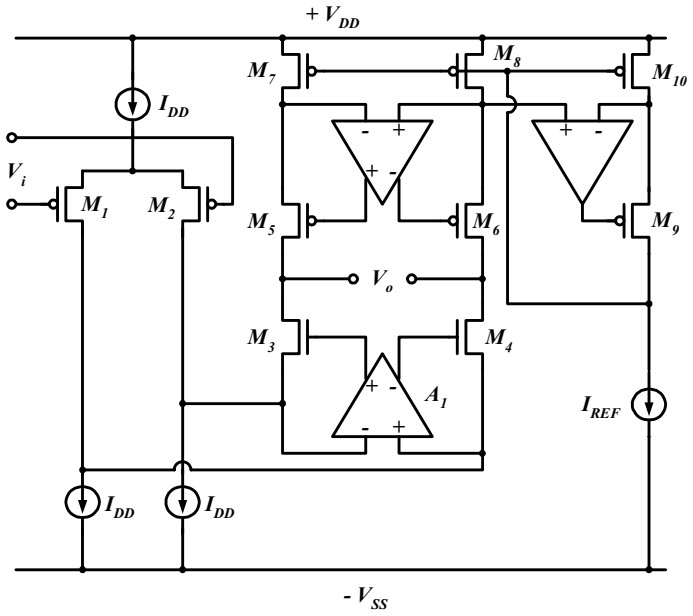


	cascode	high-swing cascode
Output swing	Low	High
PSRR+	?	?
PSRR-	High	High

3. Telescopic cascode OP AMPs with gain-boosting cascode amplifier or current-source load
   * To obtain maximum swings at the output, A_2 must employ an NMOS-input differential pair (high output dc voltage) whereas A_1 an PMOS-input one (Low output dc voltage)
   * Very high voltage gain



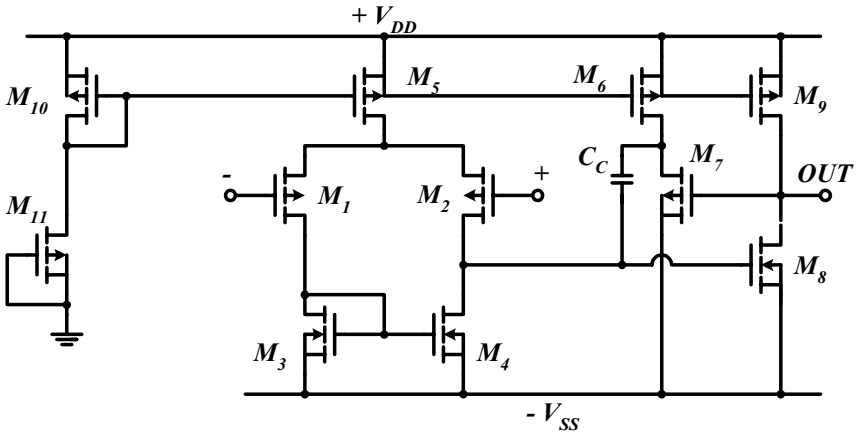
4. Folded cascode OP AMPs with cascode, high-swing cascode, or gain-boosting current-source load



§5-3 General-Purpose Two-Stage CMOS OP AMPs

§5-3.1 Single-ended-output OP AMPs

1. PMOS-input design I



M_{10}, M_1 : Master stage of PMOS current mirror.

M_5, M_6, M_9 : Slave stages

M_1, M_2, M_3, M_4, M_5: Differential-input-to-single-ended - output converter (input stage)

M_8, M_9 : CS amplifier with current-source load (gain stage)

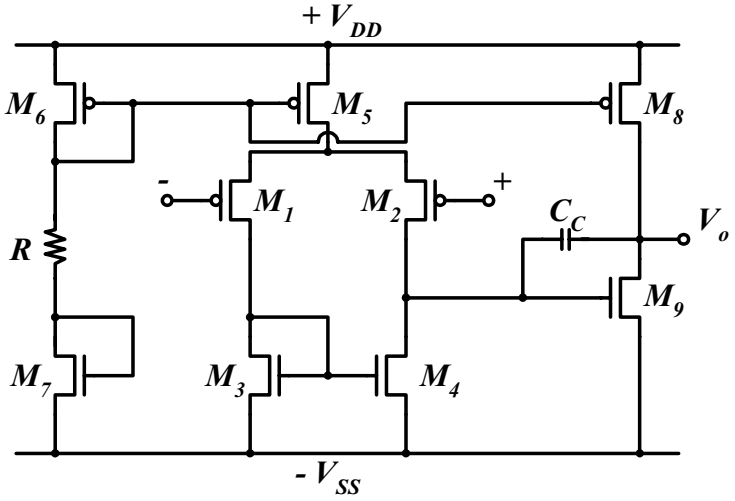
M_6, M_7, C_C : Compensation circuit with source follower.

OP AMP Characteristics :

Open-loop dc gain: 60 ~ 66 dB

CMRR : 60 dB

2. PMOS-input design II



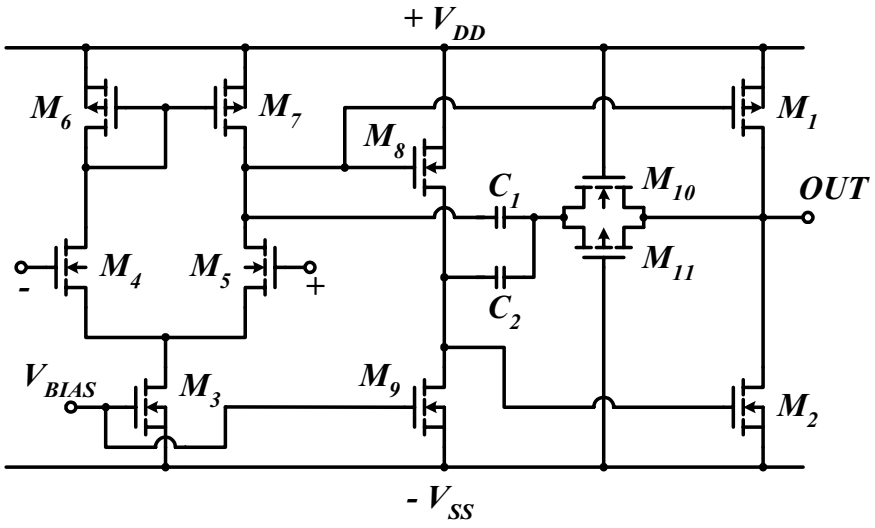
C_C : Compensation capacitor

R : n+ diffusion resistor

* First commercial CMOS OP AMP

* Designed by Motorola in 12-bit ADC.

3. NMOS-input design with level-shifted CMOS amplifier



C_2 : for PSRR (V_{DD}) consideration.

C_1 : normal compensation capacitor

Reference : IEEE JSSC, vol. sc-14, pp. 961-969, Dec. 1979

* Designed by AMI in PCM voice CODEC.

OP AMP characteristics:

Open-loop gain : 90 dB

CMRR : 73 dB

PSRR+ : 68 dB

PSRR- : 70 dB

Input offset : 10 mV (standard deviation)

0.4 mV (mean)

4. Typical characteristics of CMOS 2-stage OP AMPs

Reference : IEEE JSSC, vol. sc-17, pp. 969-982, Dec. 1982

Open-loop dc gain (C_L only) : $10^3 \sim 10^4$ (60 dB ~ 80 dB)

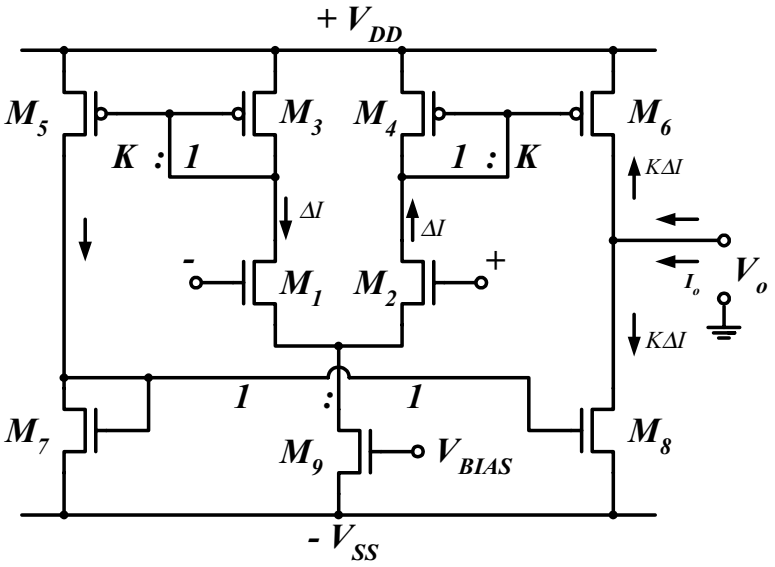
PSRR : 60 dB ~ 70 dB

Input offset : 2 mV (standard deviation)

Input common-mode range : within 1V of supply voltage.

5. Output Transconductance Amplifier (OTA) or current-mirror OP AMP

Reference : IEEE JSSC, vol. sc-19, pp. 349-359, June 1984



M_3, M_5 / M_4, M_6 : PMOS current mirrors

M_7, M_8 : NMOS current mirror

$M_1 \sim M_4$, M_9 : Input stage

$M_5 \sim M_8$: Gain stage

ΔV_{in} (input differential voltage) $\Rightarrow \Delta I \Rightarrow K\Delta I \Rightarrow \Delta I_{out} = 2K\Delta I = I_o$

$$G_m \equiv \frac{\Delta I_{out}}{\Delta V_{in}} = g_m K \qquad A_v = G_m(r_{ds6} \,//\, r_{ds8})$$

Characteristics :

Open-loop gain : 58 dB

Total dc current；4μA

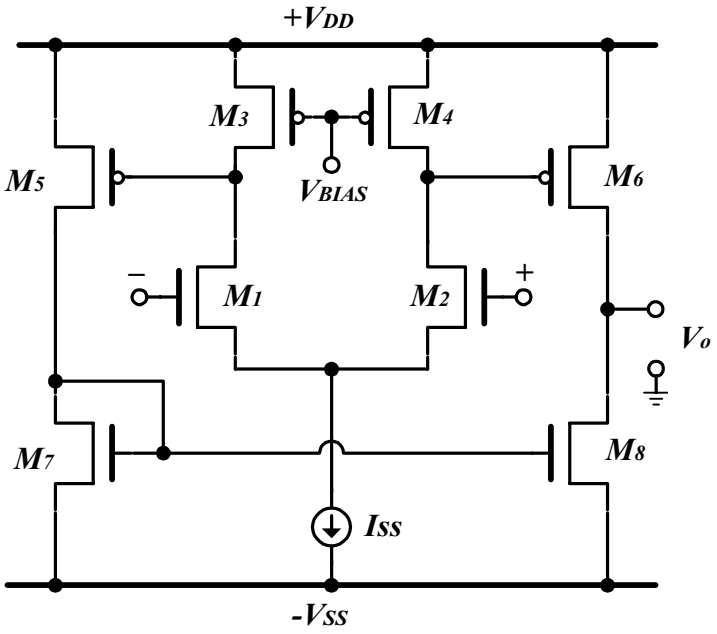
Output load capacitance；~10pF

* DC power dissipation can be decreased.

Micropower ICs for low-power applications.

* Frequency response, slew rate, and output load C_L are limited.

6. Modified OTA



* Higher G_m and higher open-loop voltage gain.

  $Gm \cong 2g_{m12}(r_{ds34} \,||\, r_{ds12})\, g_{m56}$

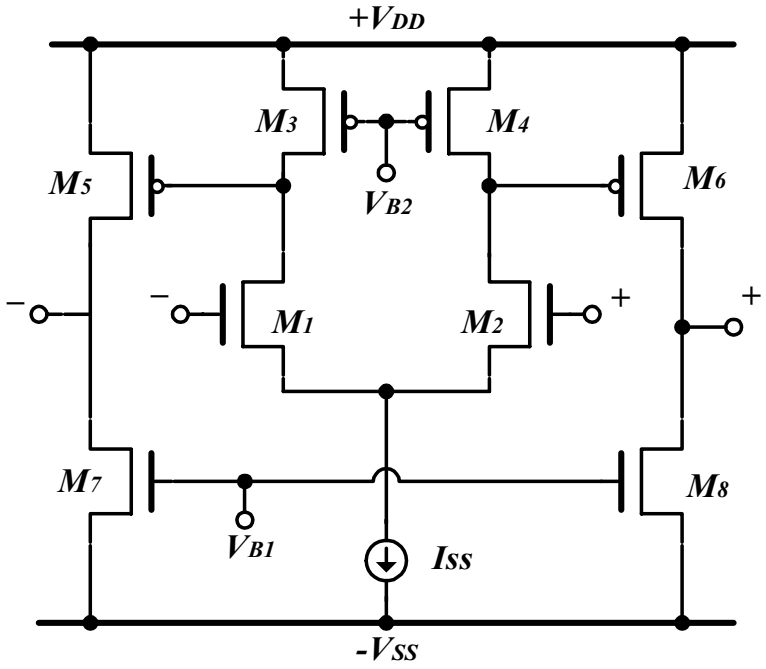
* Frequency compensation is required.
* Designed by Toshiba in C^2MOS ADC.

  Reference ; IEEE JSSC, vol.sc-13, pp.779-785, Dec. 1978

* M_5 (M_7) is matched to M_6 (M_8) => The effect of V_{TH} variations on M_6 and M_8 can be reduced.

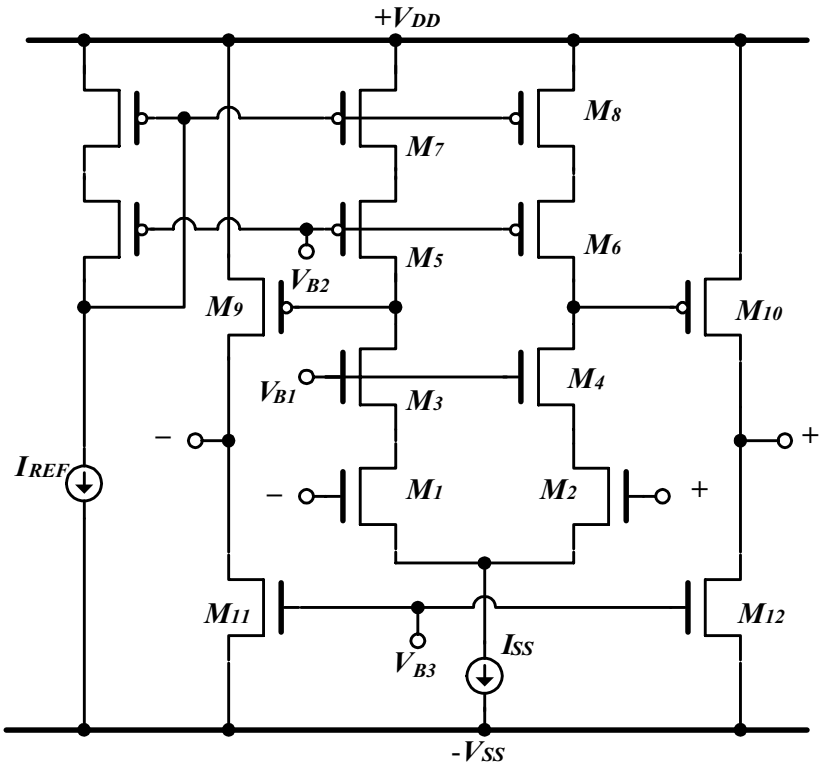
§ 5-3.2 Fully differential OP AMPs

1. Simple OP AMP



* Open-loop gain $A_v \cong g_{m12}(r_{ds12} \,||\, r_{ds34})\, g_{m56}(r_{ds56} \,||\, r_{ds78})$
* Frequency compensation is required.
* CMFB is required.

2. High-gain OP AMP



* Higher gain because of high-swing cascode current-source load.
* If high-swing cascode current source is not used, the design of M_9 and M_{10} is difficult.

  $\because \; V_{GS910} = V_{DS78} + V_{DS56}$

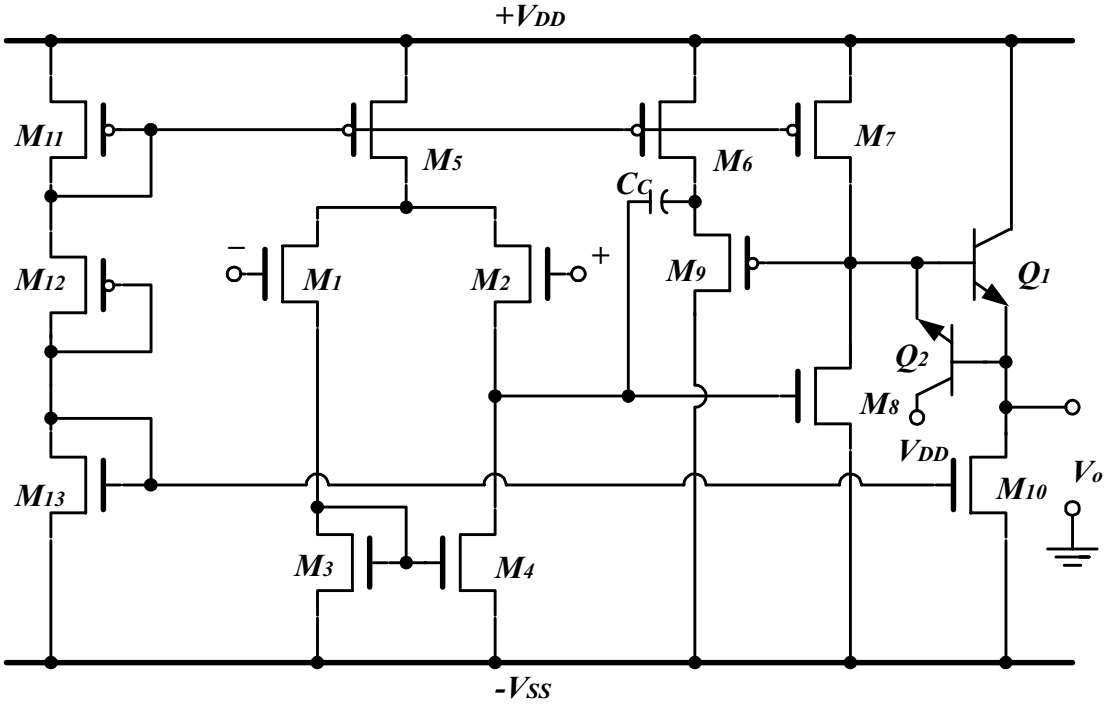
3. General comparion

	Gain	Output Swing	Power Dissipation	Speed	Noise
Telescopic	Medium	Medium	Low	Highest	Low
Folded Cascode	Medium	Medium	Medium	High	Medium
Two-stage	High	Highest	Medium	Low	Lowest
Gain-boosted	High	Medium	High	Medium	Medium

§ 5-4 General-Purpose Three-Stage CMOS OP AMPs

1. Using the emitter follower as output stage

I ;



M_6, M_9, C_C ; Frequency compensation circuit

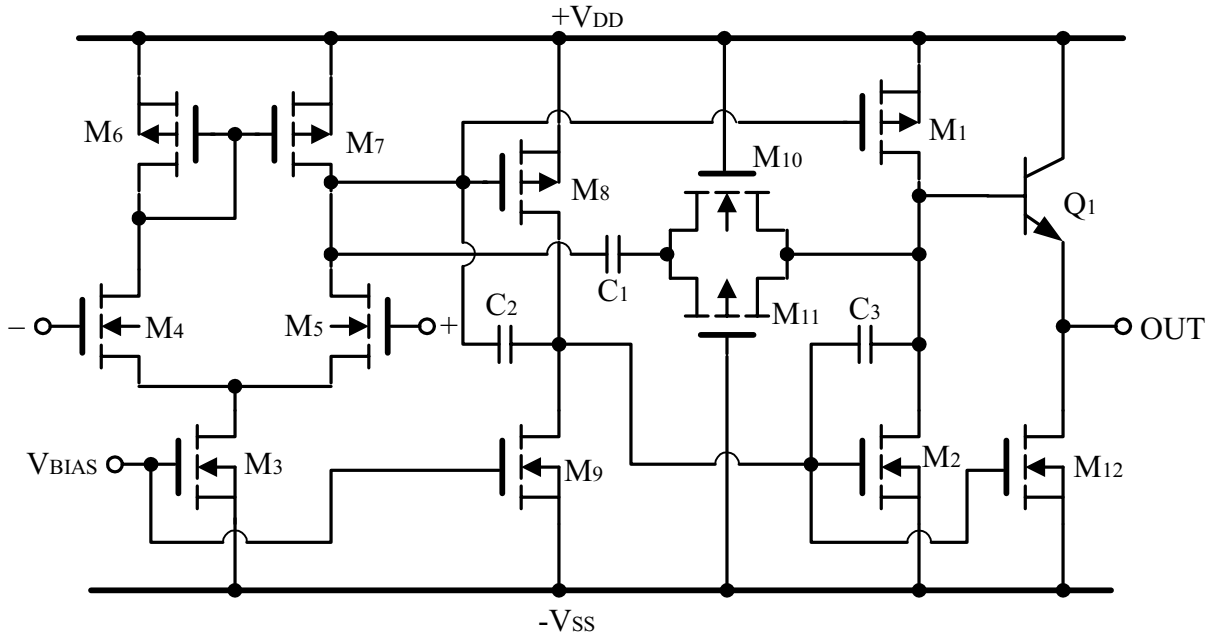
Q_2 ; Protection circuit for Q_1 to avoid the reverse breakdown of B-E junction diode of Q_1.

Q_1, M_{10} ; Emitter follower as output stage.

* Designed by Westinghouse for analog signal processing.

* Open-loop gain = 60db, power dissipation = 16mW.

II.



M10, M11, C1：Frequency compensation circuit.
C2, C3　　：Improving frequency response of Av and PSRR.

§5-5 Common-Mode Feedback (CMFB) Circuits

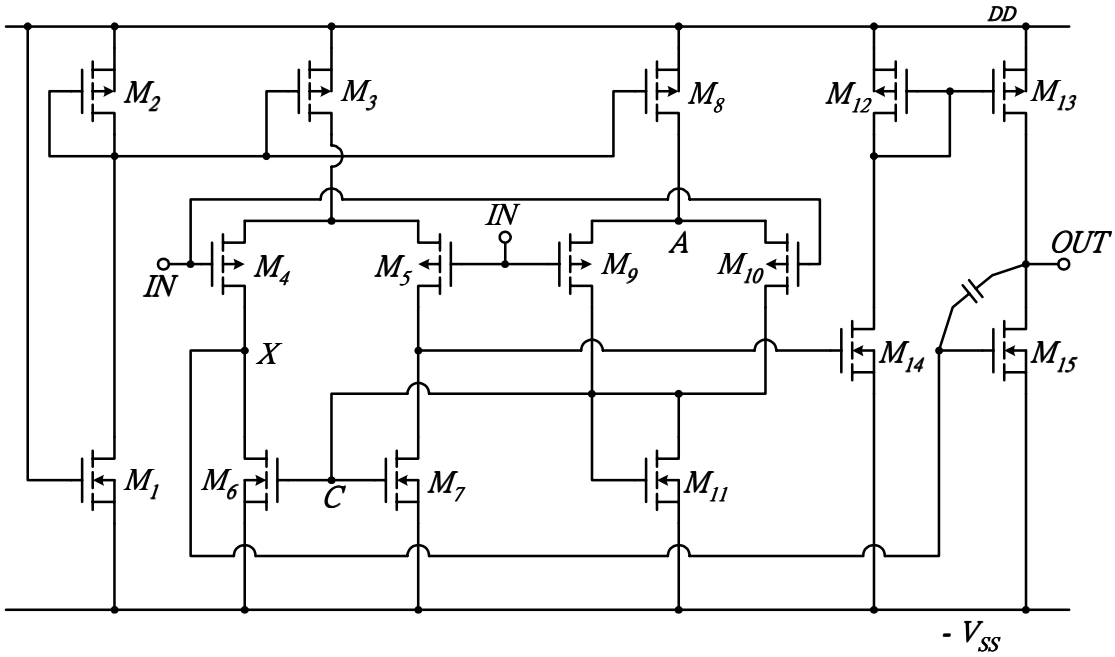
Purposes：1.To provide a stable common-mode level to the nodes.
2.To decrease the common-mode gain.

Design Considerations：

1.To create a negative feedback path only for common-mode signals. For differential signals, CMFB has no effect on circuit performance.
2.To keep power dissipation and chip area of CMFB circuit as low as possible.
3.CMFB is not required in single-ended-output OP AMPs. But it can be used to boost CMRR.
4.CMFB is required in differential-output OP AMPs.

§5-1.1 CMFB circuits for single-ended-output CMOS OP AMPs

1. Reference : IEEE JSSC, vol. sc-13, pp. 779-785, Dec. 1978



M_8, M_9, M_{10}, M_{11} : CMFB circuit

$$M_9 \equiv M_{10} \equiv M_4 \equiv M_5$$

* IN+, IN- ↑ ⇒ X, Y ↑ ⇒ common-mode voltage ↑

IN+, IN- ↑ ⇒ B ↑ ⇒ C ↑ ⇒ X, Y ↓ ⇒ compensation

* For differential signals, A and B are ac grounded

⇒ CMFB circuit has no effect on differential signals.

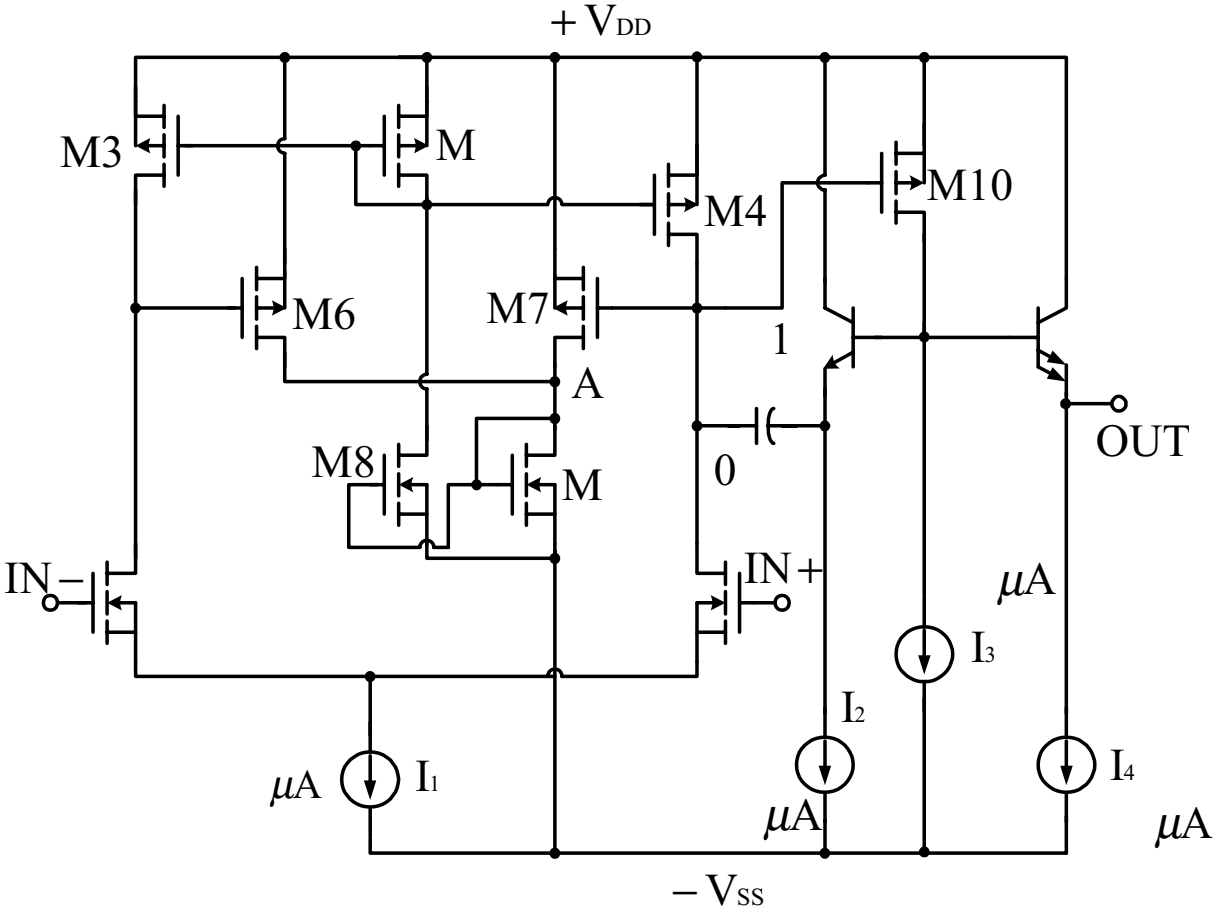
* What is the purpose of M_8 ?

* Designed by Toshiba in C^2MOS ADC

* OP AMP characteristics :

Supply voltage : 5V
Supply current : 150μA
Input common-mode range : +1V ~ +4.5V
Input offset voltage : ± 1mV
CMRR : 75dB
Open-loop gain : 90dB
Output swing : 0 ~ 5V

2.Reference: IEEE JSSC , vol. sc-14, pp. 38-46 , Feb. 1979



Q_1, I_2, C_c : Frequency compensation circuit
M_6, M_7, M_9, M_8, M_5 : CMFB circuit.

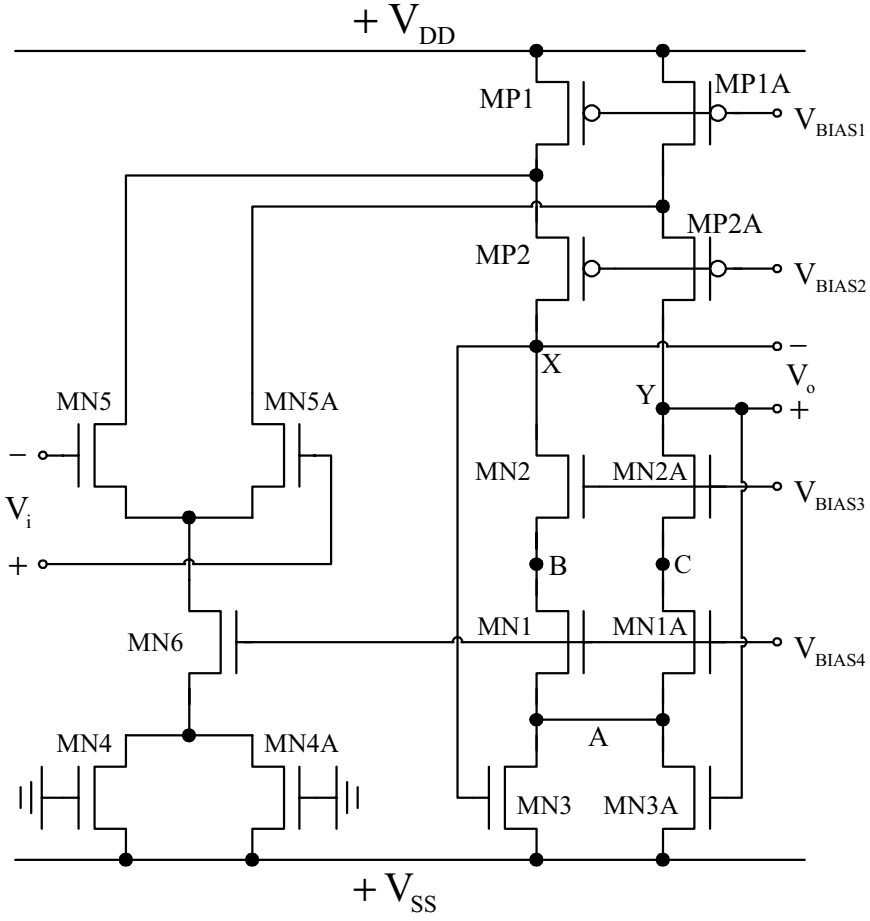
* IN+ , IN- ↑ ➔ X, Y ↓ ➔ common – mode voltage ↓

  ➔ A ↑ ➔ B ↓ ➔ X, Y ↑ ➔compensation.

* For differential signals, A is ac grounded.
  ➔No effect on differential signals.
* Keep $I_{DS6}=I_{DS7}=25$ $_{DS9}=I_{DS8}=I_{DS5}=50$
  and $I_{DS3}=I_{DS4}=25$
* Designed by MOSTEK in PCM Codec.

5-5.2 CMFB circuit for differential-output CMOS OP MP

1. Reference；IEEE JSSC , vol.sc-18 , pp.652-664 , Dec.1983



MN3 , MN3A : CMFB circuit

*Common-mode signals at $X,Y \uparrow \Rightarrow A \downarrow \Rightarrow B,C \downarrow \Rightarrow X,Y \downarrow$

*For differential signals , A is ac grounded.

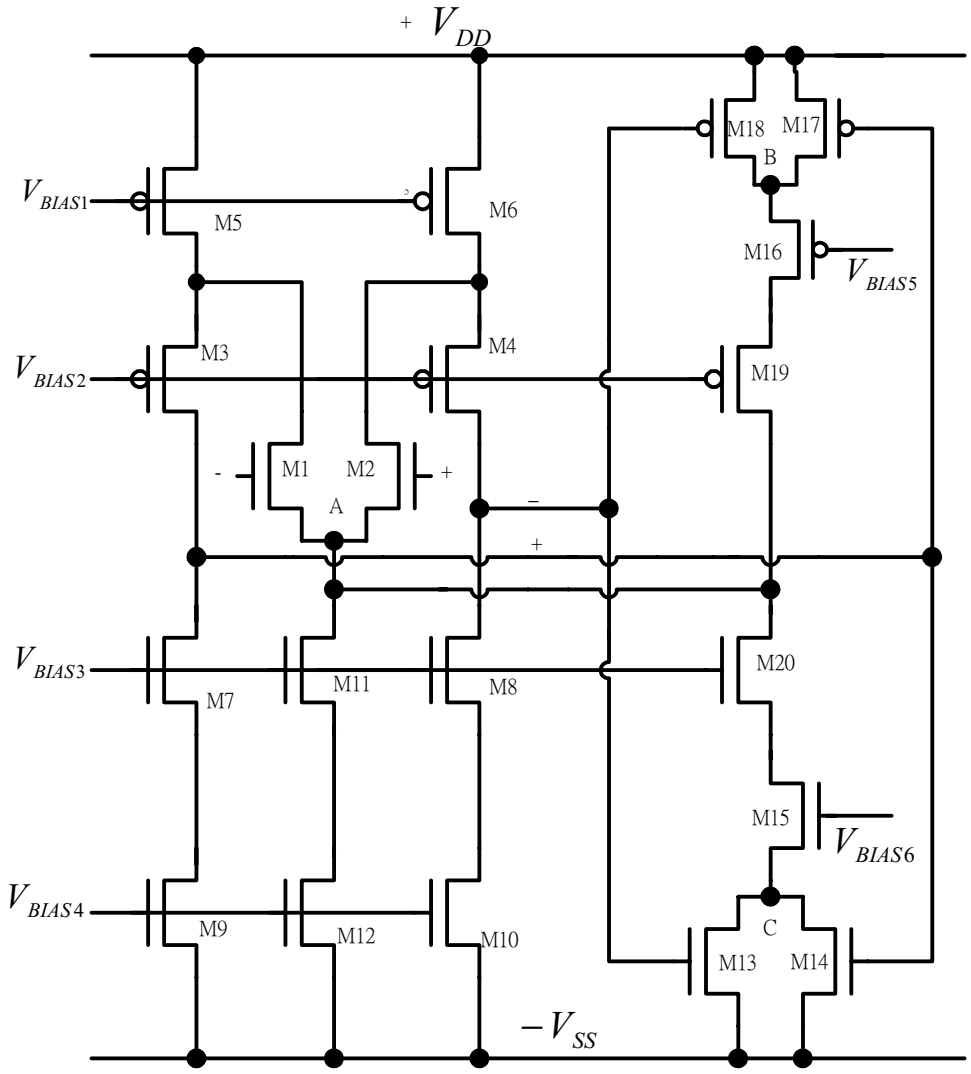
*Why MN4 and MN4A?

*Output swing is decreased by MN3 and MN3A.
To reduce the effect , MN3 and MN3A can be operated in the linear region.

*Output CM level is still a function of device parameters.

*Under differential signals , due to I_{DS} nonlinearity , A is not exactly ac ground $\Rightarrow$ differential characteristics are changed.

2.Reference: IEEE JSSC ,vol.SC-19, pp.912-918, Dec.1984



M13~M20: CMFB circuit

Cascoded common-mode amplifier

*For differential signals,nodes A,B,and C are ac grounded.

3. Resistive CMFB circuit

*For differential signals,

A is ac grounded.

$A_{dm} = g_{m12}(r_{ds12} // r_{ds34} // R_F)$

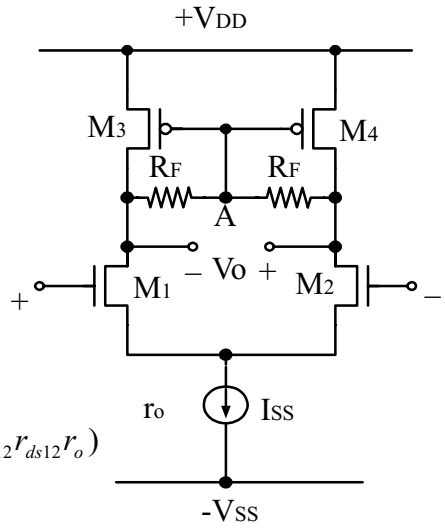
A_{dm} is decreased by R_F

*For CM signals,

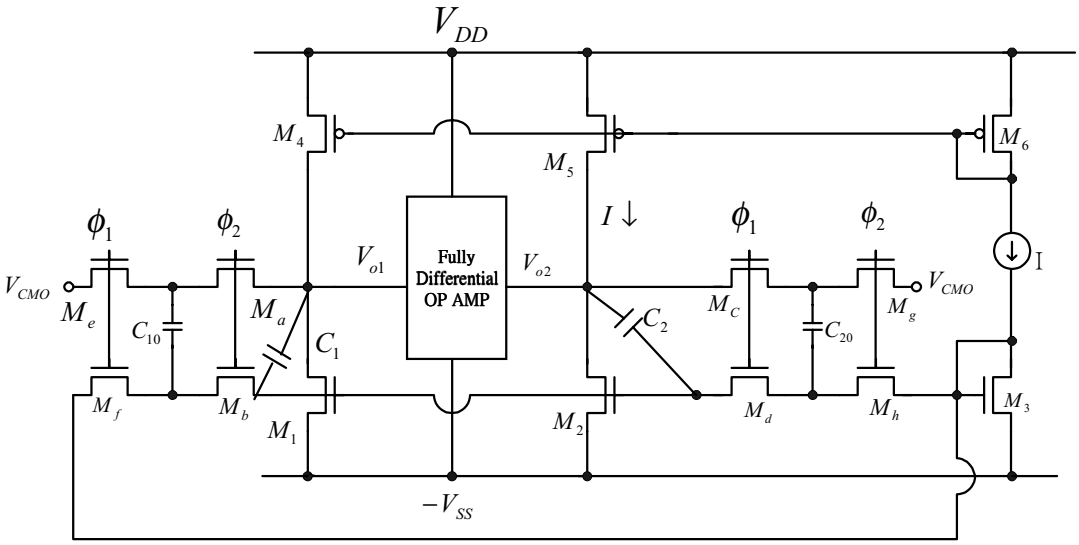
$$A_{cm} \approx -\alpha_{12}\frac{1}{2g_{m34}r_o}$$

smaller than $-\frac{\alpha_{12}}{2r_o}(r_{ds34} // g_{m12}r_{ds12}r_o)$

⇨ CMRR ↑



4. Dynamic CMFB (DCMFB) circuit



Reference: IEEE JSSC, vol. SC-20, pp.1122-1132, Dec.1985

V_{CMO}, ϕ_1, ϕ_2, $M_a \sim M_h$: CMFB circuit

$M_1 \sim M_6$: current sources associated with CMFB circuit

* DCMFB versus static CMFB

1.Less power dissipation.

2.Has no effect on output swing, noise, and speed of the OP AMP.

3.ϕ_1, ϕ_2 nonoverlapping clocks are required.