Experiment 13 - Differential Amplifiers

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UC Berkeley EE 105

1.0 Objective

In this experiment, we will examine some of the properties of both bipolar and MOS differential gain stages. The lab begins with a procedure for setting the DC bias required to obtain the correct operating point for a differential pair. With the bias conditions set, you will then measure the small signal gain for both a MOS and bipolar “diff. pair” while varying the load resistance. Two-stage differential pairs will also be examined along with other configurations which include an emitter degenerated gain stage and diff. pair commonly used to combat the effect of input offset voltage.

To show your understanding of the lab, your write-up should contain:

- 2-Port representations of the differential pair
- A discussion on the output offset voltage.
- A comparison between single-stage amplifiers and differential amplifiers
- A discussion on DC biasing issues
- A discussion on trade-offs between MOS and BJT differential pairs

2.0 Prelab

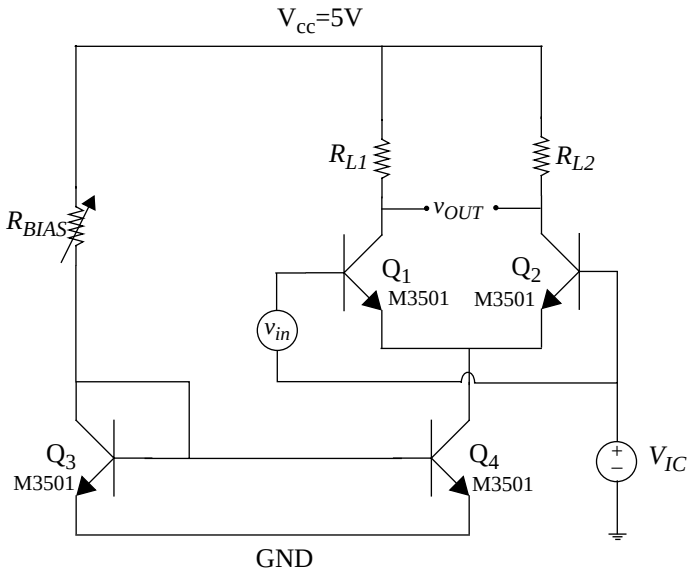
H & S: Chapters 11.1 - 11.2

M3501 $\beta_F = 104.3$ $V_{An} = 43.3V$
N3515 $V_{TOn} = 0.88\ V$ $\mu_n C_{ox} = 79.47\ \mu A/V^2$ $\lambda_n = 0.06\ V^{-1}$

2.1 1. BJT Differential Pair

A single BJT differential pair is shown below. For R_{L1} and R_{L2}=1 kΩ, calculate I_{BIAS} to set V_{O1} and V_{O2} at a level that will give the maximum output swing. Assume V_{CEsat} =0.2 V and V_{BE} = 0.7 V. With your value of I_{BIAS} calculate the differential mode gain $A_{dm}=v_{out}/v_{in}$ and the common mode gain $A_{cm}=v_{out}/v_{in}$. What is the CMRR?

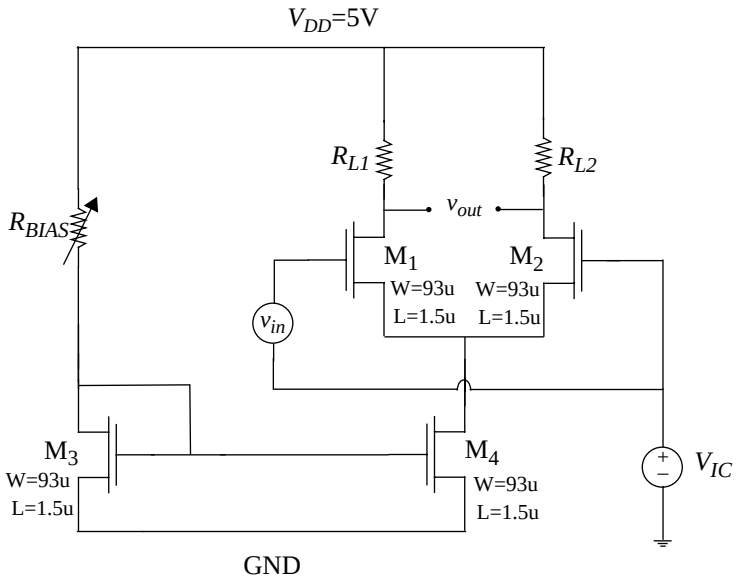
FIGURE 1. Bipolar Differential Pair



2.2 MOS Differential Pair

A single MOS differential pair is shown below. For R_{L1} and R_{L2}=1kΩ, calculate I_{BIAS} to set V_{O1} and V_{O2} at 2.75V. Calculate the differential mode gain $A_{dm}=v_{out}/v_{in}$ and the common mode gain $A_{cm}=v_{out}/v_{in}$. What is the CMRR?

FIGURE 2. MOS Differential Pair



3.0 Procedure

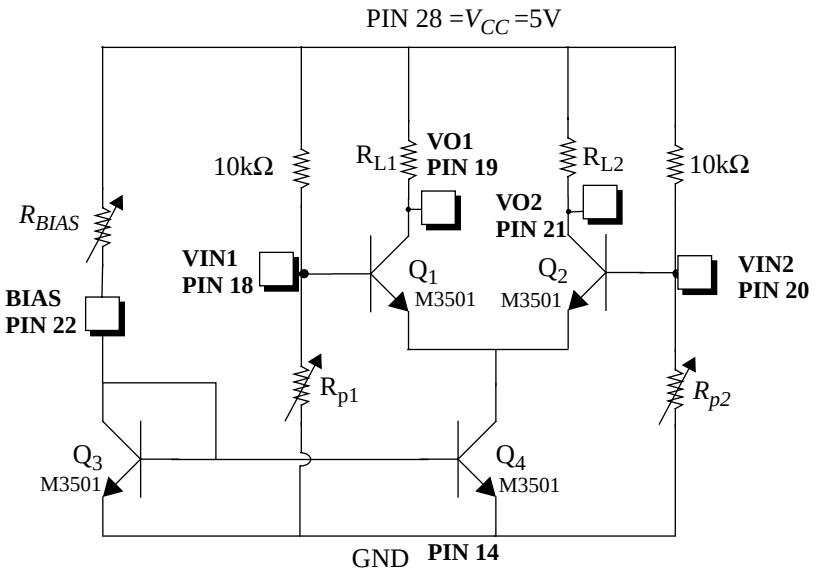
3.1 BJT Differential Pair

3.1.1 DC Measurement

1. Connect up the bjt diff. pair circuit shown in figure 3. Use $R_{L1,2}$=2.5kΩ and R_{BIAS} =2 kΩ. Note the collector currents and collector voltages. Also note I_{BIAS}.
2. Adjust R_{p1} and R_{p2} until V_{BQ1} and V_{BQ2} is ≅1.2V.
3. Make sure that all the transistors are in the forward active region of operation.
4. Connect a voltmeter at $V_{O1.}$ Adjust R_{p2} and observe what happens at V_{O1}. In particular, note the *difference* in the base voltages when $V_{O1} \cong 0$ and V_{O1} = 5V.
5. Readjust R_{p1} and R_{p2} until V_{O1}-V_{O2} is at a minimum (< 100mV) while making sure that the DC values of V_{O1} and V_{O2} are approximately at 1.2V.
6. The DC voltage required at the base of Q_1 and Q_2 to make the differential output voltage equal zero is referred to as the input offset voltage. By adjusting R_{p1} and R_{p2}, you have removed the offset voltage at the output of the circuit shown in Figure 3. When designing any type of differential amplifier it is extremely important to minimize this offset which will be amplified if we cascade (pass the signal through a series of gain stages) the signal through more than one amplifying stage. Now measure the input offset voltage of the circuit you have just built, V_{os}=V_{BE1}-V_{BE2}=V_{BQ1}-

V_{BQ2} using the digital multi-meter. Later in this lab we will discuss how this offset arises and a technique to minimize the input offset voltage of a differential pair

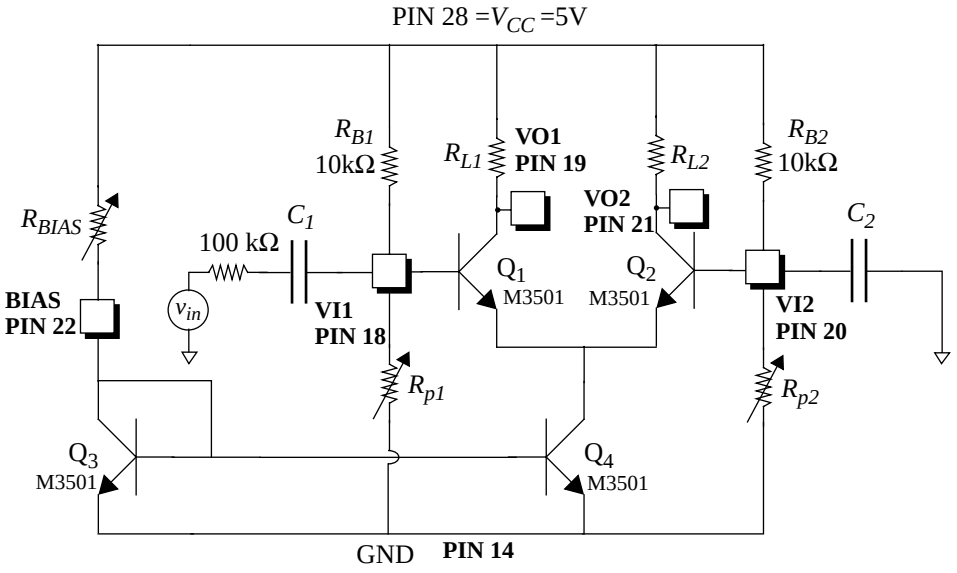
FIGURE 3. Bipolar Differential Pair for DC Measurements (Lab Chip 6)



3.1.2 AC Measurement

1. To perform an AC analysis, modify the circuit in figure 3 to the circuit in figure 4. Use the signal generator to apply a small sinusoidal input at v_{in} at 10kHz. Let C_1 and C_2 be large capacitors (10μF). Observe the output waveform using the oscilloscope by connecting v_{o1} to Channel 1 and v_{o2} to Channel 2. Invert Channel 2 and add both Channels together. What can you say about the phase of the signals at v_{o1} and v_{o2}? Why do we need the 100kΩ resistor in series with the signal source? Also, how much is the signal attenuated between the signal source and the base of Q_1? What is A_{dm}? What is the relationship between the differential gain and the single-ended gain.
2. Increase the amplitude of v_{in} until the output begins to “rail out” (clip)-record this range of the input voltage and output voltage.
3. To measure the input resistance, measure the voltage gain v_{b1}/v_{in} (The gain at the base of the resistor). Using a resistive divider relationship, find the input resistance of the differential pair (The biasing resistors are part of the input resistance).
4. For A_{cm}, remove R_{B2}, R_{P2} and C_2.and short the bases of Q_1 and Q_2 together. Apply a small sinusoidal input at v_{in} and use the oscilloscope to measure A_{cm} by observing the output waveform at v_{o1}. What is CMRR for this diff. pair?

FIGURE 4. Bipolar Differential Pair for AC Measurements



4. Use SPICE to confirm your experiment. Use transistor data from previous experiments.

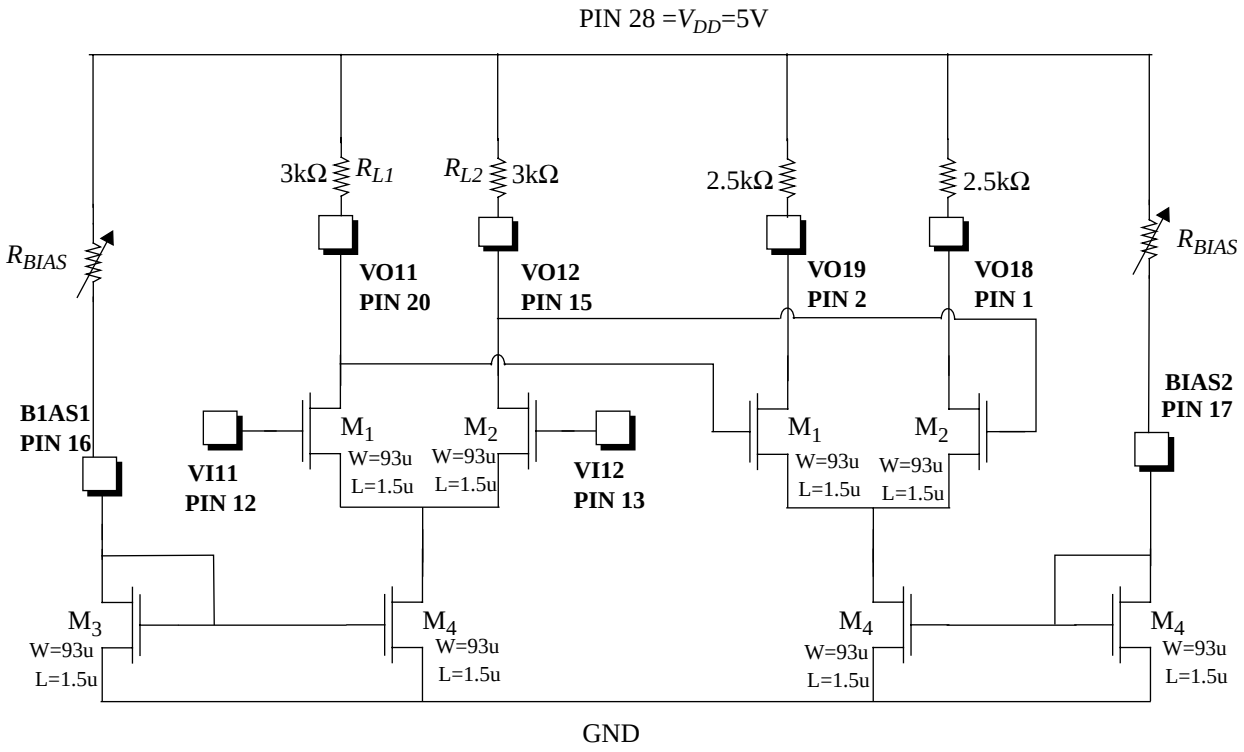
Note: $R_{p1,2}$ should both be about 3 kΩ.

3.2 Two Stage MOS Differential Pair

3.2.1 DC Measurements

1. A two stage diff. pair is shown in Fig. 5. Let R_{BIAS} be 2 kΩ. Bias the gates of the first stage (pins 5 and 6) to be 2.5V DC using a resistive divider as you did with the bipolar diff pair.
2. As before, minimize the output offset of the first stage by adjusting the variable resistors. What is the effect of a large offset voltage on the second stage? You can play with the variable resistors and see for yourself.
3. Again, note all the drain and bias currents. Verify that all the devices are in its saturation region.

FIGURE 5. Two Stage MOS Differential Pair (MOSDP, Lab Chip 5)



Note: The second stage doesn't need to be biased. It is biased by the first stage.

3.2.2 AC Measurements

1. Repeat the procedures for the ac measurements of the bipolar diff pair. This time, find the gain of the first stage as well as the two-stage composite amplifier.
2. As always use SPICE to verify.

4.0 Optional Experiments

4.1 Emitter Degenerated BJT Differential Pair

When trying to amplify a voltage signal, we always want to have a high input resistance. One way of increasing the input and output impedance of a bipolar differential pair is to degenerate the emitter of Q_1 and Q_2. On Lab Chip 6 there is a differential pair provided (BJTDPDE) which will allow you to investigate some of the properties of emitter degenerated differential pairs.

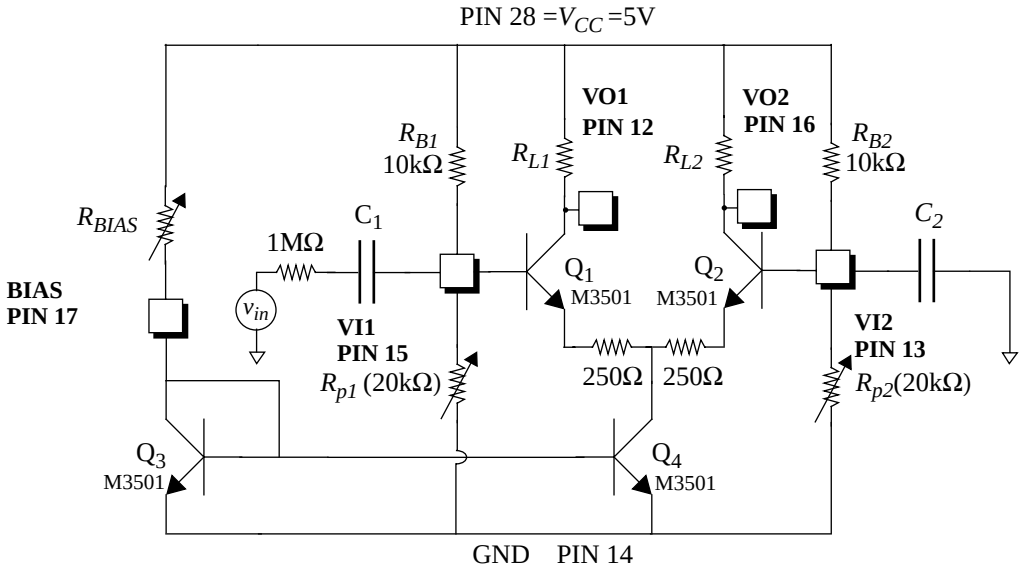
4.1.1 DC Measurements

1. Connect up the emitter degenerated diff. pair circuit shown in Figure 6. Bias the diff. pair using the same procedure in part 3.1 of the lab. Use $R_{L1,2}$=50kΩ. Adjust R_{p1} and R_{p2} until V_{BQ1} and V_{BQ2} is ≅1.6V. Why is 1.6V a good bias voltage for the base of Q_1 & Q_2?
2. Calculate the bias current needed for V_{O1} and V_{O2} to be equal to 2.75V. Adjust R_{BIAS} until the current through Q_3 equals I_{bias} and V_{o1} and V_{o2} equal 2.75V.
3. Connect a voltmeter between V_{O1} and V_{O2} and adjust R_{p2} until V_{O1} - V_{O2} is a minimum while making sure that V_{O1} and V_{O2} are about 2.75V.
4. Now measure the offset voltage V_{os}=V_{BE1} - V_{BE2}= V_{BQ1} - V_{BQ2}. Notice that the offset voltage is larger than that of the non-degenerate diff. pair with the same load resistance. (why?-explain).

4.1.2 AC Measurement

1. Apply a small sinusoidal input at v_{in} at 10 kHz. Observe the output waveform using the oscilloscope by connecting v_{o1} to Channel 1 and v_{o2} to Channel 2. Invert Channel 2 and add both Channels together. Measure A_{vd}, and compare with A_{vd} of non-degenerate case.
2. For A_{vc} remove R_{B2} and R_{P2} and short the bases of Q_1 and Q_2 together. Apply a small sinusoidal input at v_{in} and use the oscilloscope to measure A_{cm} by observing the output waveform at v_{o1}. What is CMRR for this diff. pair? Compare this with that of the non-degenerate case. Use SPICE to calculate A_{vd}, A_{vc} and R_{in}.

FIGURE 6. Bipolar Differential Pair with Emitter Degeneration (BJTDPDE, Lab Chip 6)



5.0 Appendix

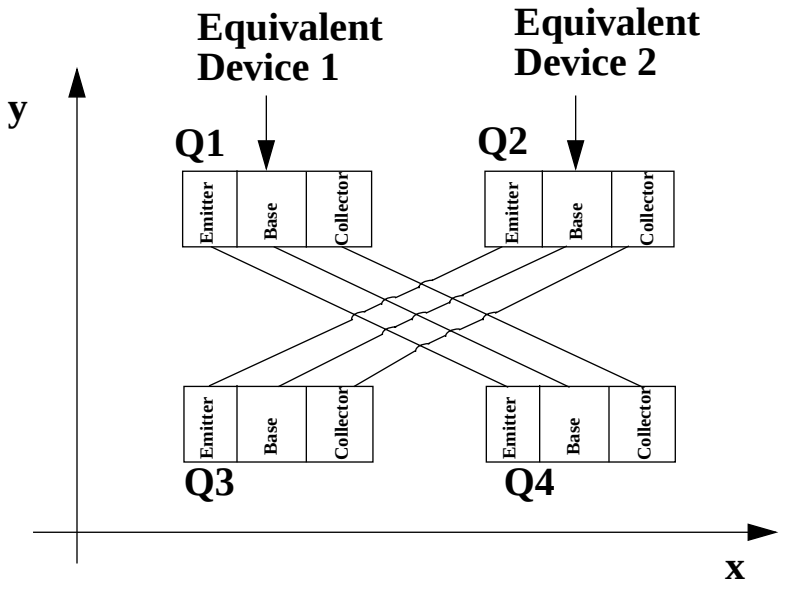
5.1 Offset Voltage and Device Mismatches

5.1.1 V_{OS} of Unmatched Differential Pair

Due to a mismatch in the input transistors and in the collector load resistors, there will be always be a slight offset in the output DC level. As explained before, this offset will degrade the maximum output voltage swing and can potentially be amplified by cascaded gain stages. For our differential pair there isn't much we can due to alleviate the problem of the mismatch between load resistors. However, there is a very popular technique for lowering the mismatch between the two input transistors.

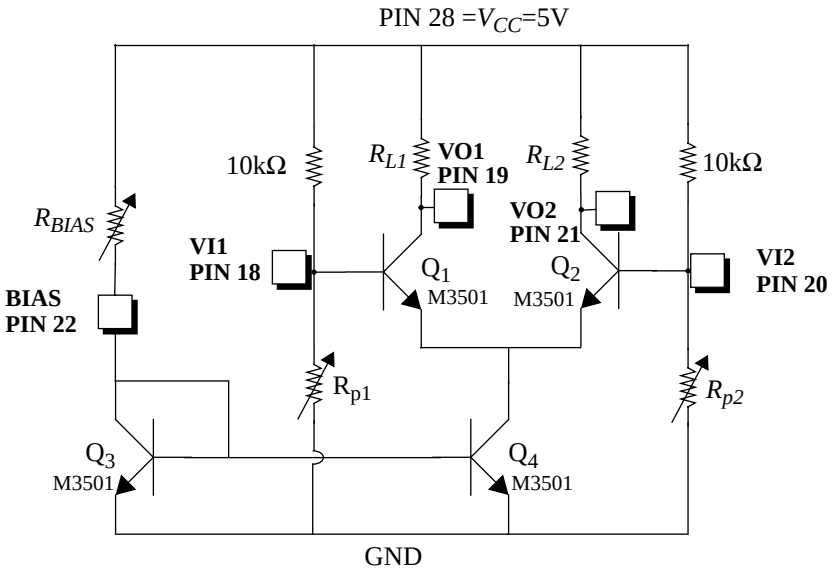
During the fabrication of integrated circuits, mismatches between identical transistors, resistors and capacitors are created by process variations across the entire wafer. For example, variations in the value of on-chip capacitors can be attributed to a change in the thickness of the dielectric from one end of the wafer to the other. Process variations can also be the result of a non-uniform implant doping or gas diffusion. The change in process parameters across the wafer usually occur in one direction. Two adjacent devices can still experience a significant mismatch in device parameters even though they are physically close to each other. Fortunately, a technique know as "common-centroid layout" exists to minimize the effect of process variations. When trying to critically match devices as in the input stage of an Operational Amplifier two devices at adjacent angles can be combined to make one device. Figure 7 shows the basic idea of a common-centroid, here we see two devices combined to make one large device. Any process variation in the x or y direction will automatically be cancelled by the two devices.

FIGURE 7. Common Centroid Layout



To exacerbate the effect of mismatch between input devices, we have deliberately laid out a differential pair with input devices on opposite corners of Lab Chip 6 (See Figure 8). Measure the input offset voltage using the procedure in part 3.1 of this lab. Now measure the value of the load resistors. How much of the input referred offset is attributed to the mismatch in the load resistors? How much input referred offset is due to Q_1 and Q_2?

FIGURE 8. Unmatched BJT Differential Pair (BJTDPUM, Lab Chip 6)



5.1.2 V_{OS} of Matched Differential Pair

Shown below (Figure 9) is a schematic of an on-chip differential pair with matched input devices using a common-centroid layout. Also shown below in Figure 10, we see the actual layout of the circuit shown in Figure 9. Try to identify and understand this layout, as much as feasible given the black-and-white rendering. Then using the same resistor values as you did for the unmatched diff. pair, again measure the input offset voltage. Is there been a significant improvement in the input referred offset?

FIGURE 9. Circuit Diagram of Diff Pair using Common Centroid Layout (BJTDPM, Lab Chip 6)

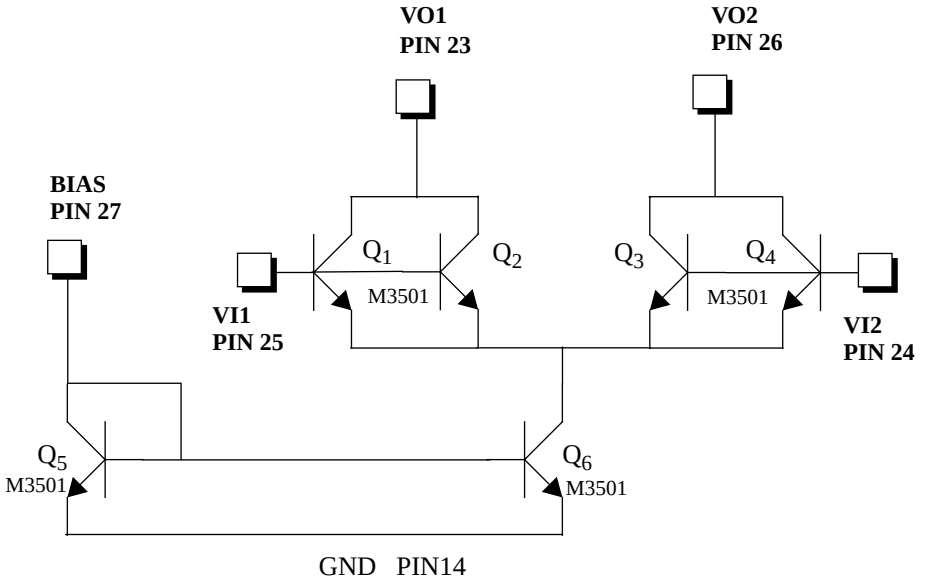


FIGURE 10. Layout of Matched Input Devices