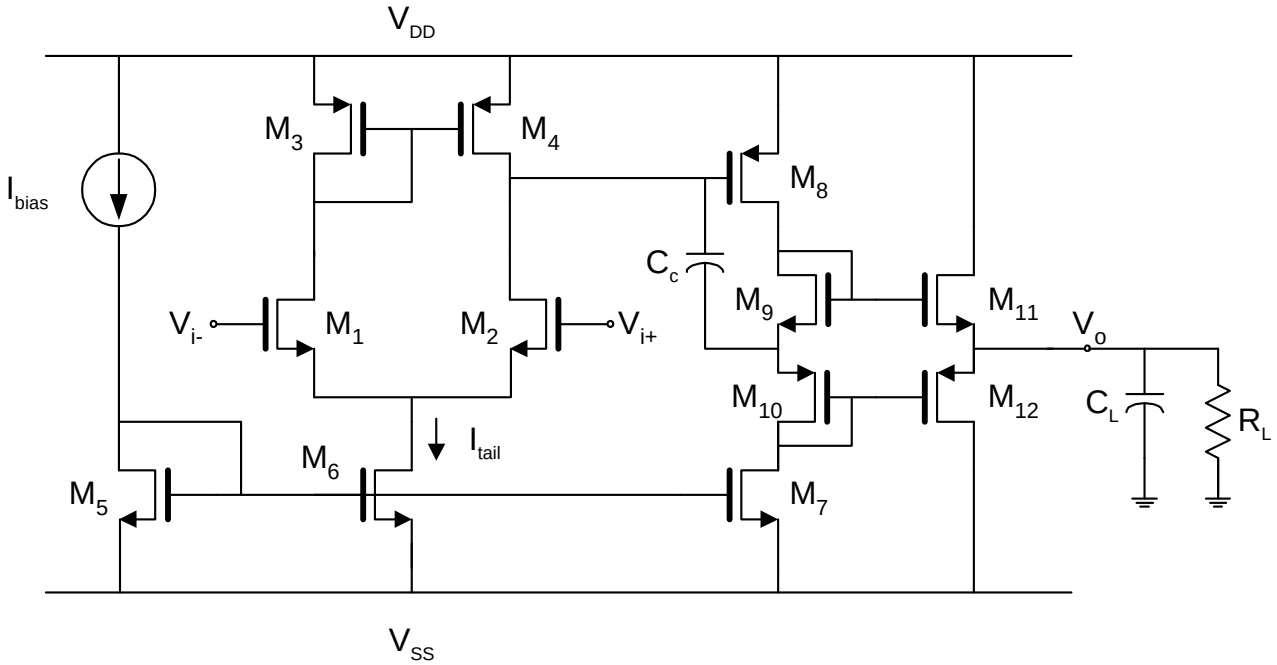
The following is an example design procedure for a three stage operational amplifier.



Transistor Parameters;

```
STUDENT > KPN:=5.1169e-5;KPP:=1.6528e-5;VTN:=0.7339;VTP:=0.7776;LAMB
          DAN:=3.1220E-02;LAMBDAP:=4.3490E-02;GAMMAN:=0.4823;GAMMAP:
          =0.6727;PHI:=0.7;
```

$$KPN := .000051169$$

$$KPP := .000016528$$

$$VTN := .7339$$

$$VTP := .7776$$

$$LAMBDAN := .031220$$

$$LAMBDAP := .043490$$

$$GAMMAN := .4823$$

$$GAMMAP := .6727$$

$$PHI := .7$$

Opamp Specifications

```
STUDENT > Avo:=1000;GBW:=1e6;SR:=2/1e-6;PM:=45;PD:=1e-3;
```

$$Avo := 1000$$

$$GBW := .1\ 10^{7}$$

$$SR := .2000000000\ 10^{7}$$

$$PM := 45$$

$$PD := .001$$

```
STUDENT > RL:=1e3;CL:=30e-12;Vomax:=0.9;VDD:=2.5;VSS:=-2.5;
```

$$RL := 1000.$$

$$CL := .30\ 10^{-10}$$

$$Vomax := .9$$

$$VDD := 2.5$$

$$VSS := -2.5$$

Design varibles

```
STUDENT > alpha:=2;
```

$$\alpha := 2$$

1) Choose Compensation Capacitor. First aproximation CC=CL.

```
STUDENT > CC:=CL;
```

$$CC := .30\ 10^{-10}$$

2) Choose the tail current to satisfy the slew rate requirement.

```
STUDENT > Itail:=SR*CC;
```

$$Itail := .00006000000000$$

3) Determine the transconductance of the input stage.

```
STUDENT > GmA:=6.2832*GBW*CC;
```

$$GmA := .0001884960$$

4) Determine the transconductance of the input transistors.

```
STUDENT > WL1:=GmA^2/(KPN*Itail);
```

$$WL1 := 11.57300384$$

5) Determine the transconductance of the gain stage

```
STUDENT > GmB:=(6.2832*GBW*CC)/tan( (1.57-(PM*6.2832)/360)/2 );
```

$$GmB := .0004555837655$$

6) Determine the size of the inverter amplifier transistor.

```
STUDENT > WL8:=(GmB^2)/(2*KPP*alpha*Itail);
```

$$WL8 := 52.32448155$$

```
STUDENT > alpha*Itail;
```

$$.0001200000000$$

7) Determine the size of M5 and M6 depending the Itail and the Ibias of the tail current mirror. Assume that the virtual ground node of the differential amplifier is at the same voltage as the diode connected transistor of the current mirror.

```
STUDENT > Vgs6:=1.2;
STUDENT > WL6:=(2*Itail)/(KPN*(Vgs6-VTN)^2);
```

$$Vgs6 := 1.2$$

$$WL6 := 10.79483754$$

8) Design the current mirror load for the gain stage

```
STUDENT > WL7:=alpha*WL6;
```

$$WL7 := 21.58967508$$

9) Design the current mirror active load for the input stage.

This design gives zero output voltage for zero input voltage.

```
STUDENT > WL3:=(1/(2*alpha))*WL8;
```

$$WL3 := 13.08112039$$

10) M11 and M12 are calculated as follows

```
STUDENT > Iomax:=Vomax/RL;Iomin:=-Vomax/RL;
```

$$Iomax := .0009000000000$$

$$Iomin := -.0009000000000$$

```
STUDENT > VBS11:=VSS-Vomax;VSB12:=-Vomax-VDD;
```

$$VBS11 := -3.4$$

$$VSB12 := -3.4$$

```
STUDENT > VTN11:=VTN+GAMMAN*(sqrt(PHI-VBS11)-sqrt(PHI));
          VTP12:=VTP+GAMMAP*(sqrt(PHI-VSB12)-sqrt(PHI));
```

$$VTN11 := 1.306961938$$

$$VTP12 := 1.576892485$$

```
STUDENT > Vdssat8:=0;Vsdsat7:=0;
```

$$Vdssat8 := 0$$

$$Vsdsat7 := 0$$

```
STUDENT > Vg11max:=VDD-Vdssat8;Vg12min:=Vsdsat7+VSS;
```

$$Vg11max := 2.5$$

$$Vg12min := -2.5$$

```
STUDENT > Vgs11max:=Vg11max-Vomax;Vsg12min:=Vomax+Vg12min;
```

$$Vgs11max := 1.6$$

$$Vsg12min := -1.6$$

Verify that under the maximum transfer both transistors operate in saturation

```
STUDENT > Vgs11max-VTN11;abs(Vsg12min)-VTP12;
STUDENT >
```

$$.293038062$$

$$.023107515$$

```
STUDENT > WL11:=(2*Iomax)/(KPN*(Vgs11max-VTN11)^2*(1+LAMBDAN*(VDD-Vo
          max)));
STUDENT > WL12:=(2*Iomax)/(KPP*(abs(Vsg12min)-VTP12)^2*(1+LAMBDAP*(V
          DD-Vomax)));
          WL12:=(KPN/KPP)*WL11;
```

$$WL11 := 390.1647802$$

$$WL12 := 190691.2721$$

$$WL12 := 1207.910312$$

Find the DC operating Bulk to source voltage to determine the VT's

```
STUDENT > VBS11Q:=VSS;VSB12Q:=-VDD;
          VTN11Q:=VTN+GAMMAN*(sqrt(PHI-VBS11Q)-sqrt(PHI));
          VTP12Q:=VTP+GAMMAP*(sqrt(PHI-VSB12Q)-sqrt(PHI));
```

$$VBS11Q := -2.5$$

$$VSB12Q := -2.5$$

$$VTN11Q := 1.193143338$$

$$VTP12Q := 1.418141143$$

Assign a voltage which will barely turn both transistors

```
STUDENT > VON:=1.42;(VON-VTN11Q);(VON-VTP12Q);
STUDENT >
```

$$VON := 1.42$$

$$.226856662$$

$$.001858857$$

```
STUDENT > IDQ:=(KPN/2)*(WL11)*(VON-VTN11Q)^2;
STUDENT > Vg11Q:=sqrt((IDQ*2)/(KPN*WL11))+VTN11Q;
          Vg12Q:=sqrt((IDQ*2)/(KPP*WL12))+VTP12Q;
```

$$IDQ := .0005137218910$$

$$Vg11Q := 1.420000000$$

$$Vg12Q := 1.644997805$$

```
STUDENT > IbiasInv:=alpha*Itail;
```

$$IbiasInv := .0001200000000$$

```
STUDENT > WL9:=(IbiasInv/IDQ)*WL11;
          WL10:=(IbiasInv/IDQ)*WL12;
```

$$WL9 := 91.13836580$$

$$WL10 := 282.1550726$$

```
STUDENT > round(WL1*2);
          round(WL8*2);
          round(WL6*2);
          round(WL7*2);
          round(WL3*2);
          round(WL11*2);
          round(WL12*2);
          round(WL9*2);
          round(WL10*2);
```

$$23$$

$$105$$

$$22$$

$$43$$

$$26$$

$$780$$

$$2416$$

182

564

STUDENT >