Chapter 10 CMOS Bandgap References

§10-1 Basic Principles of Bandgap References (BGR)

$V_{BE(on)} = mV_{therm}\ln(I_1 / I_S)$

$I_S = qAn_i^{\,2}\overline{D_n}/Q_B$ $\quad I_S$: Reverse saturation current of a BJT

$= Bn_i^{\,2}\overline{D}$ $\quad A$: Area of a BJT

$= B'n_i^{\,2}T\overline{m}$ $\quad Q_B$: Base minority carrier charges

where B and B' are constants, indep. of T. $\quad \overline{D}$: Average diffusivity of carriers

$\overline{m} = CT^{-n}$ $\quad$ C:Constant, indep. of T.

n:Temp. exponent.

$n_i^{\,2} = ET^3\exp(-V_{GO}/V_{therm})$ $\quad E$: Constant, indep. of T.

V_{GO} : Energy gap.

$\Rightarrow V_{BE(on)} = mV_{therm}\ln[I_1T^{-g}F\exp(V_{GO}/V_{therm})]$

F : Constant , indep. of T.

$g = 4 - n$

$I_1 = GT^a$ where I_1 is the collector current and G is a temp.-indep. constant.

$\Rightarrow V_{BE(on)} = V_{GO} - V_{therm}[(g-a)\ln T - \ln(FG)]$

In general, the output voltage V_{out} is a sum of $V_{BE(on)}$, and KV_{therm} with a weighting factor K such that V_{out} is nearly indep. of T.

$$V_{BE(on)} + KV_{therm} = V_{out} = V_{GO} - mV_{therm}(g-a)\ln T + mV_{therm}[K + \ln(FG)] \text{ .....(1)}$$

$$\left.\frac{dV_{out}}{dT}\right|_{T=T_O} = 0 = \frac{mV_{thermo}}{T_O}[K + \ln(FG)] - \frac{mV_{thermo}}{T_O}(g-a)\ln T_O - \frac{mV_{thermo}}{T_O}(g-a) + \frac{d}{dT}V_{GO}$$

$$\Rightarrow K + \ln(FG) = (g-a)\ln T_O + (g-a) - \left(\frac{d}{dT}V_{GO}\right)\cdot\frac{T_O}{mV_{thermo}} \text{ ....(2)}$$

Substituting (2) into (1) , we have

$$V_{out} = V_{GO} + mV_{therm}(g-a)(1+\ln\frac{T_O}{T}) - T\frac{d}{dT}V_{GO}$$

$$V_{GO} = 1.16 - \frac{7.02\times10^{-4}\cdot T^2}{T+1108}$$

$$\left.\frac{d}{dT}V_{GO}\right|_{T=T_O} = -\frac{14.04\times10^{-4}T_O(T_O+1108) - 7.02\times10^{-4}\cdot T_O{}^2}{(T_O+1108)^2}$$

$$= -\frac{14.04\times10^{-4}\cdot T_O}{T_O+1108} + \frac{7.02\times10^{-4}\cdot T_O{}^2}{(T_O+1108)^2}$$

$$\Rightarrow V_{out} = mV_{therm}(g-a)(1+\ln\frac{T_O}{T}) + 1.16 - \frac{7.02\times10^{-4}\cdot T^2}{T+1108} - \frac{14.04\times10^{-4}\cdot T_O T}{T_O+1108} + \frac{7.02\times10^{-4}\cdot T_O^2\cdot T}{(T_O+1108)^2}$$

If $g = 3.2, m = 1, a = 1, T_O = 25^O C$

$$\Rightarrow V_{out}(T)\big|_{T=25^O C} = 1.16 + 2.2(0.0259) - \frac{21.06\times10^{-4}(298)^2}{298+1108} + \frac{7.02\times10^{-4}(298)^2}{(298+1108)^2}$$

$$= 1.093V$$

§10-2 Bipolar Bandgap Reference

Widlar bandgap reference

*Feedback element Q_4 is used to force Q_3 on.

*Q_4 also serves as a start-up circuit.

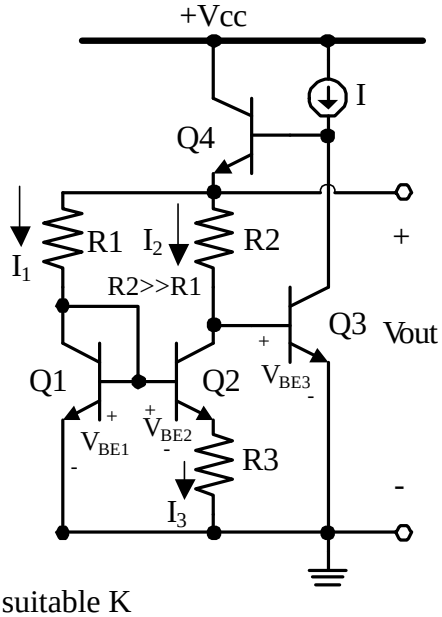
*$V_{out} = I_2R_2 + V_{BE3}$

$I_2 = I_3$ if $I_{B2} = I_{B3}$

$$I_3 = \frac{V_{BE1} - V_{BE2}}{R_3} = \frac{1}{R_3}mV_{therm}\left[\ln(\frac{I_1}{I_2}) + \ln(\frac{I_{S2}}{I_{S1}})\right]$$

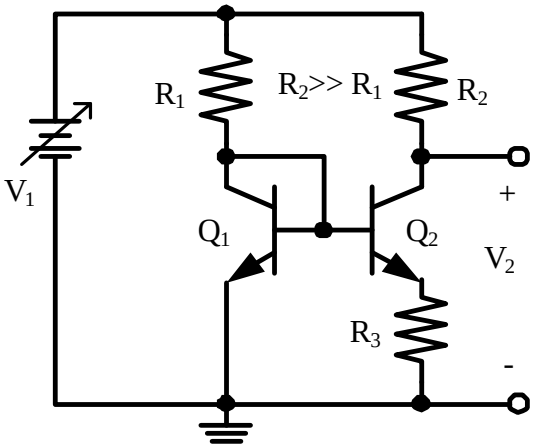
$$V_{out} = V_{BE3} + \left\{\frac{R_2}{R_3}m\left[\ln\left(\frac{R_2}{R_1}\right) + \ln\left(\frac{I_{S2}}{I_{S1}}\right)\right]\right\}\cdot V_{therm}$$

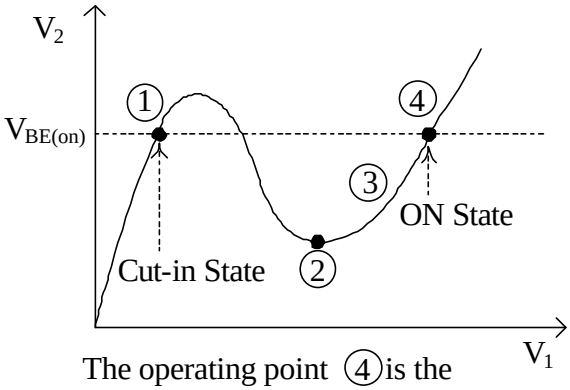
$I_1/I_2 = R_2/R_1$ If $V_{BE1} = V_{BE3}$



Adjust R_2/R_3 , R_2/R_1 and I_{S2}/I_{S1} to give a suitable K

And Keep $I \cong I_2$ to obtain $I_{B2} \cong I_{B3}$ and $\frac{I_{S3}}{I_{S1}} = \frac{I_3}{I_1}$ to obtain $V_{BE1} = V_{BE3}$.





The operating point ④ is the desired operating point

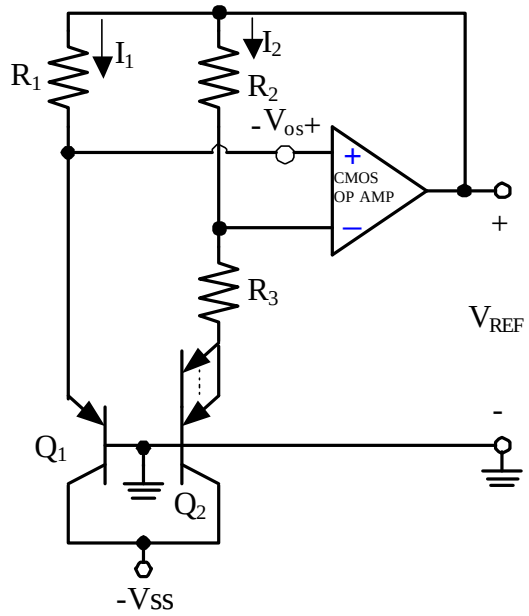
=>Need a start-up circuit.

§10-3 CMOS Real Bandgap Reference (BGR)

§10-3.1 CMOS BGR via BJTs and Resistors

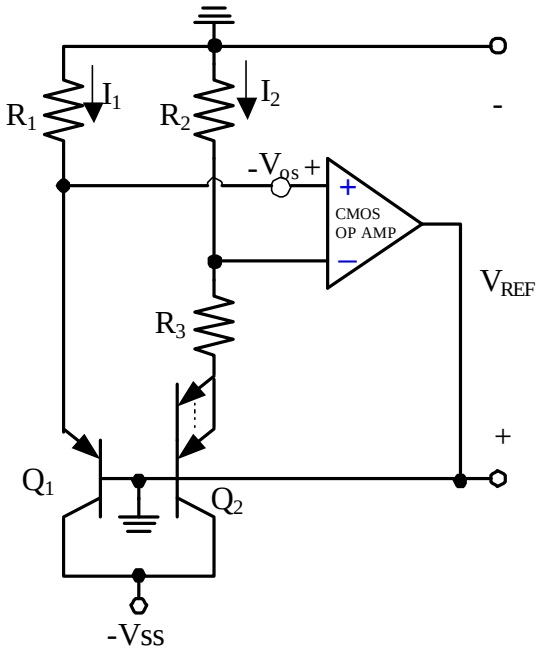
Version 1:

N-well CMOS, positive V_{REF}



Version 2:

N-well CMOS, Negative V_{REF}



Q_1,Q_2:Substrage-well-source/drain parasitic vertical BJTs

$$V_{BE} = mV_{therm} \ln \frac{I_E}{I_S}$$

$$V_{REF} = \pm\{V_{BE1} + \frac{R_2}{R_3} V_{therm} (\ln \frac{R_2}{R_1} + \ln \frac{I_{s2}}{I_{s1}}) + V_{OS}[\frac{R_3 + R_2}{R_3}]\}$$

Typical design values:

I_1=80 μ A I_2=8 μ A

$$R_2 \approx \frac{0.6V}{8\mu A} = 75K\Omega,\ R_1 = \frac{R_2}{10} = 7.5K\Omega,\ R_3 = \frac{60mV}{8\mu A} = 7.5K\Omega$$

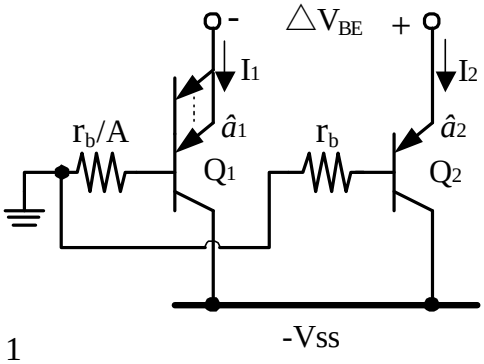
Large resistance➔use well resistors

R1,R2,R3: n+/p+ diffusion resistors

n+ - poly resistors

well resistors

Both transistors are in the active region



Error analysis:

1. Error due to base resistances

$$V_{BE1} = V_{therm} \ln \frac{I_1}{I_S} + V_{therm} \ln \frac{1}{1+\frac{1}{\beta_1}} + \frac{r_b I_1}{A\beta_1}$$

$$\Delta V_{BE} = V_{therm} \ln A + V_{therm} \ln \frac{I_2}{I_1} + V_{therm} \ln \frac{1+\frac{1}{\beta_1}}{1+\frac{1}{\beta_2}} + r_b\left(\frac{I_2}{\beta_2} - \frac{I_1}{A\beta_1}\right)$$

If $\hat{a}_1$, $\hat{a}_2$ are not large enough or r_b is too large,

➔ ΔV_{BE} due to r_b and β is large.

$$V_{REF} = \pm\{V_{BE1} + V_{OS}\left(\frac{R_3+R_2}{R_3}\right) + \frac{R_2}{R_3} V_{therm}\left(\ln\frac{R_2}{R_1} + \ln\frac{I_{s2}}{I_{s1}} + \ln\frac{1+\frac{1}{\beta_1}}{1+\frac{1}{\beta_2}}\right) + \frac{R_2}{R_3} r_b\left(\frac{I_2}{\beta_2} - \frac{I_1}{A\beta_1}\right)\}$$

2.Error due to input offset voltage V_{os}

V_{os}=10mV, $V_{OS}(1+\frac{R_2}{R_3}) \approx 10V_{OS} = 100mV$

TC error due to

$$V_{OS} : \frac{1}{V_{REF}} \frac{d}{dT} V_{REF} = \frac{(1+\frac{R_2}{R_1})V_{OS}}{V_{REF} T_0} = \frac{10 \times 10mV}{1.26V \times 300^o K} = 264\, ppm/^o C$$

3.Error due to Bias current variation

$$V_{BE1} = V_{therm} \ln \frac{I_1}{I_{S1}} = V_{Threm} \ln \frac{V_{therm} \ln A}{R\ I_{S1}}$$ (R_3=R_1)

$$= V_{therm} \ln \frac{V_{therm} \ln A}{R_1(T_O) I_{S1}} + V_{therm} \ln \frac{R_1(T_O)}{R_1(T)} \qquad I_1 = I_2$$

If R_1 is indep. of T $\Rightarrow V_{BE} = V_{therm} \ln \frac{V_{therm} \ln A}{R_1(T_O) I_{S1}}$

If R_1 depends on T $\Rightarrow V_{BE} = V_{therm} \ln \frac{V_{therm} \ln A}{R_1(T_O) I_{S1}} + V_{therm} \ln \frac{R_1(T_O)}{R_1(T)}$

$$V_{BE} = V_{BE}\big|_{ideal} - V_{therm} \cdot \left(\frac{1}{R} \frac{dR}{dT}\bigg|_{T_O} \right)(T - T_O) - V_{therm} \left(\frac{1}{2R} \frac{d^2R}{dT^2}\bigg|_{T_O} \right)(T - T_O)^2$$

$PTAT^2$ $PTAT$ $PTAT^3$ $PTAT$

$$+ V_{therm} \left(\frac{1}{2R^2} \frac{dR}{dT}\bigg|_{T_O} \right)(T - T_O)^2 - .....$$

$PTAT^3$ $PTAT$

If R is only linearly dependent on T, we still have $PTAT^2$ term
The $PTAT^2$ term can be cancelled via curvature compensations.

4.TC Error due to Base Resistance

$$\Delta V_{BE} = r_b \frac{I_2}{\beta_2}$$

$$\text{TC error} = (1 + \frac{R_2}{R_1}) \frac{r_b I_2}{V_{ref} \beta_2} \left(\frac{1}{r_b} \frac{dr_b}{dT} + \frac{1}{I_2} \frac{dI_2}{dT} - \frac{1}{\beta_2} \frac{d\beta_2}{dT} \right)$$

Example : $r_b = 2K\Omega$, TC of $r_b = 1000 ppm/^O C$, $I_2 = 30mA$, $\beta = 150$,

TC of $\beta = 7000 ppm/^O C$

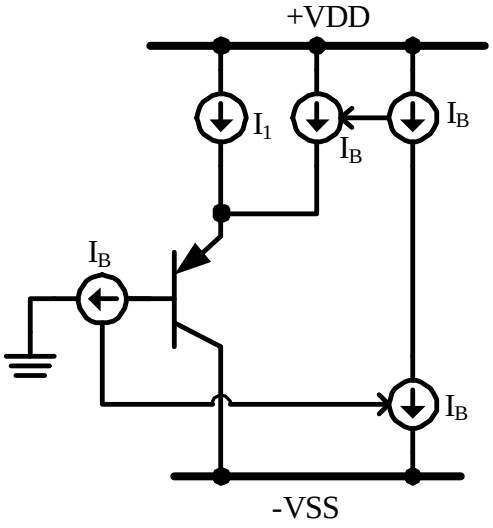
$\Rightarrow$ TC = –8.6 $ppm/^O C$

5.Error due to base current

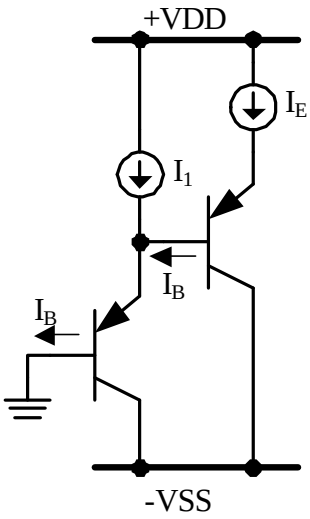
Base current cancellation technique

*To compensate for the different between the collector, emitter, or base current

Version 1:



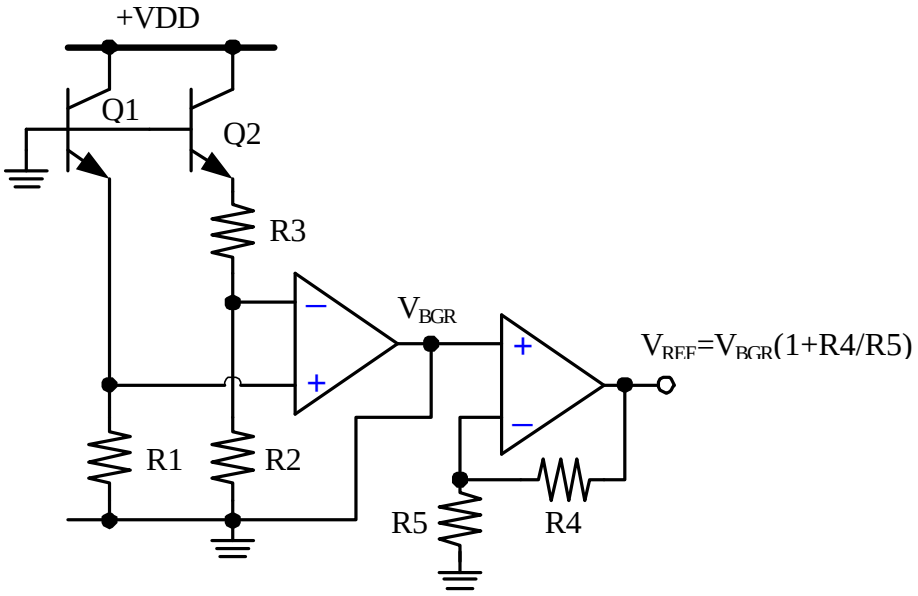
Version2:



Ref:1.IEEE J .Solid-State Circuits, vol.SC-18, pp634-640, DEC. 1983

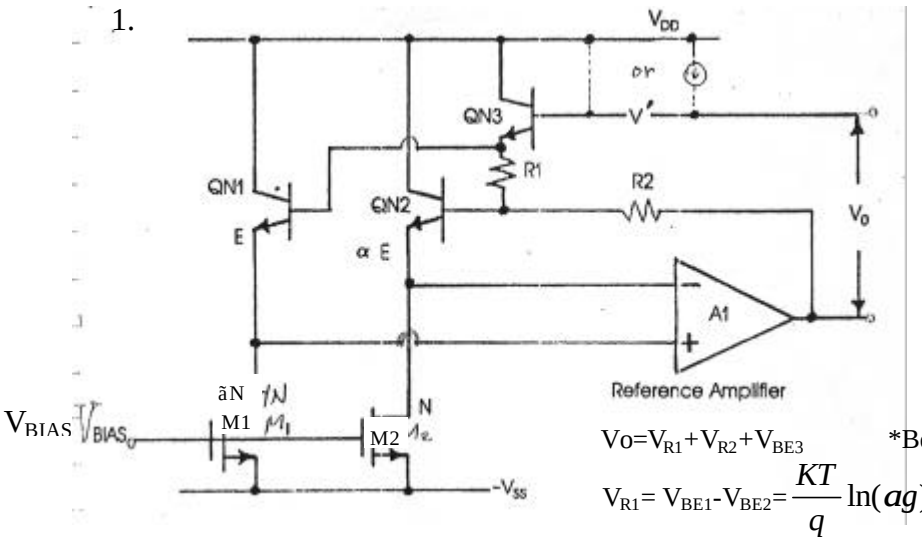
2. IEEE J .Solid-State Circuits, vol.SC-19, pp1014-1021, DEC. 1984

The circuit to obtain V_{REF} from a BGR



§ 10-3.2 Improved structure

1.

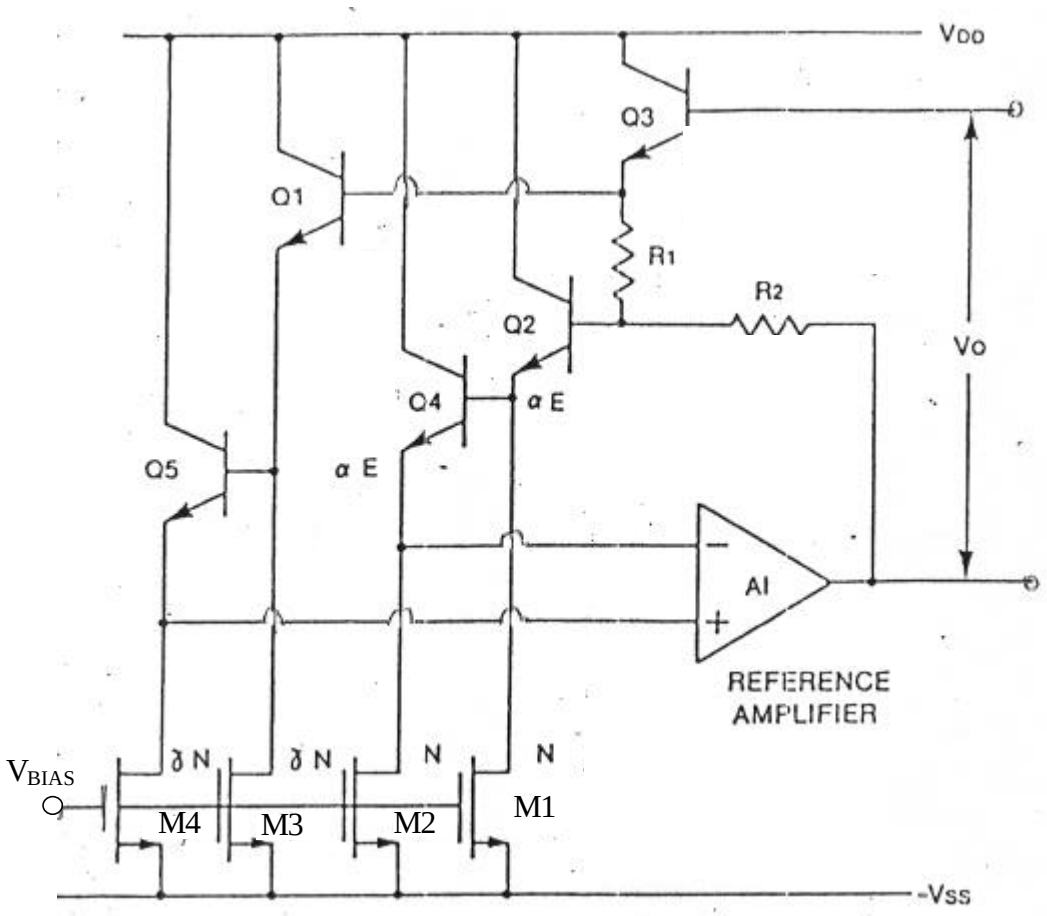


Vo=V_{R1}+V_{R2}+V_{BE3} *Better matching

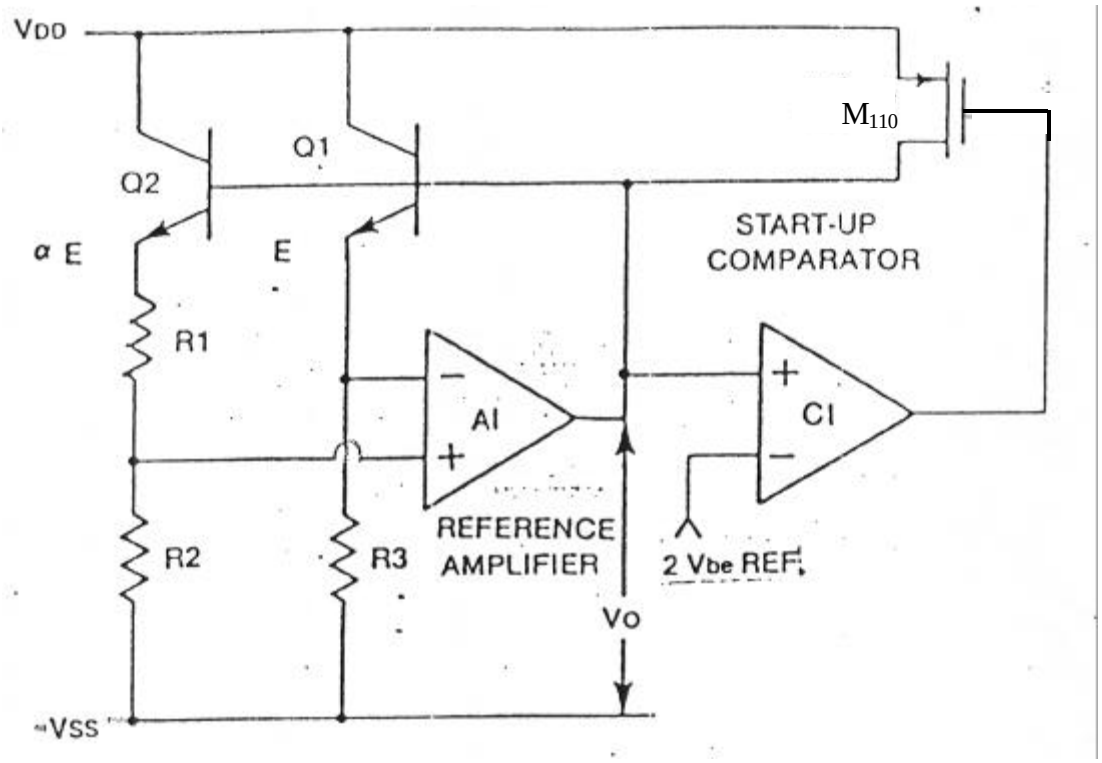
V_{R1}= V_{BE1}-V_{BE2}= $\frac{KT}{q}\ln(ag)$

Vo=VBE3+ $\frac{KT}{q}[\ln(ag)]$(1+R/R) =>Bandgap Reference

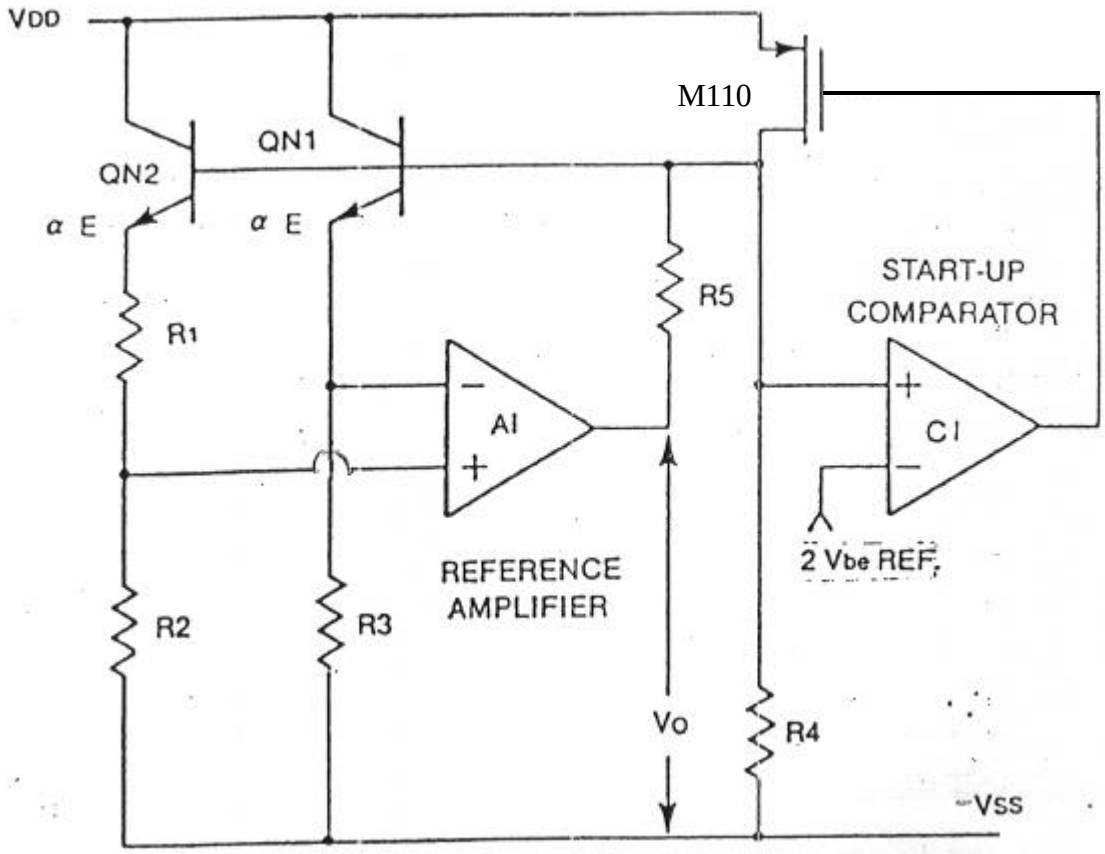
2.

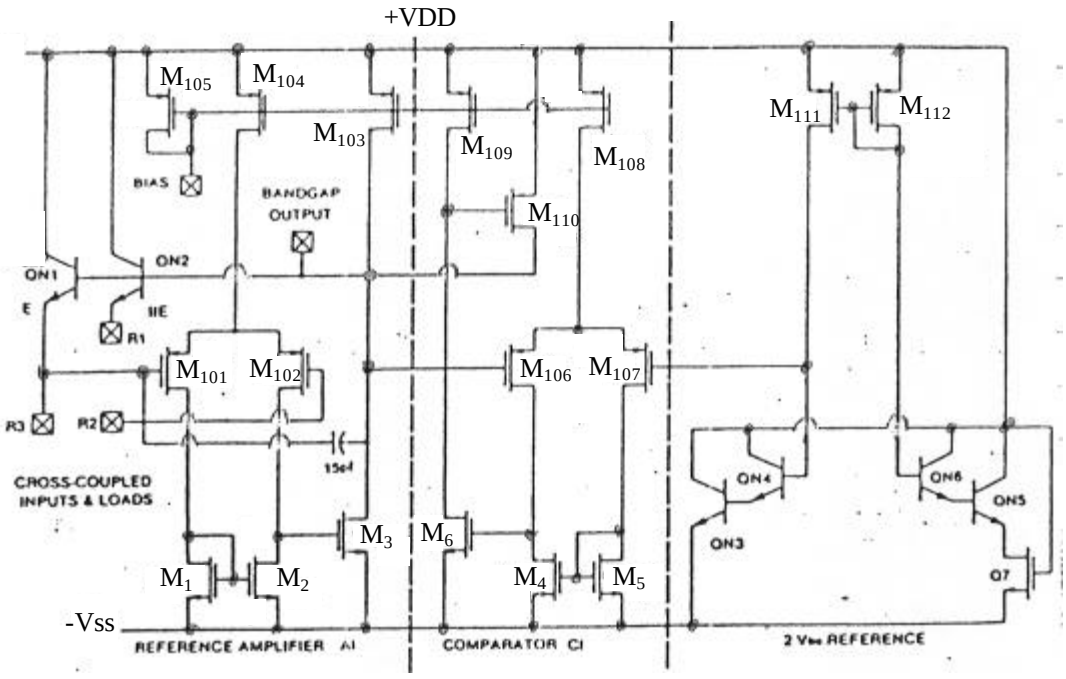

VDD
Q3
Q1
R1
R2
Q2
Vo
Q4
α E
Q5
α E
AI
REFERENCE
AMPLIFIER
VBIAS
∂ N
∂ N
N
N
M4
M3
M2
M1
-Vss

3.

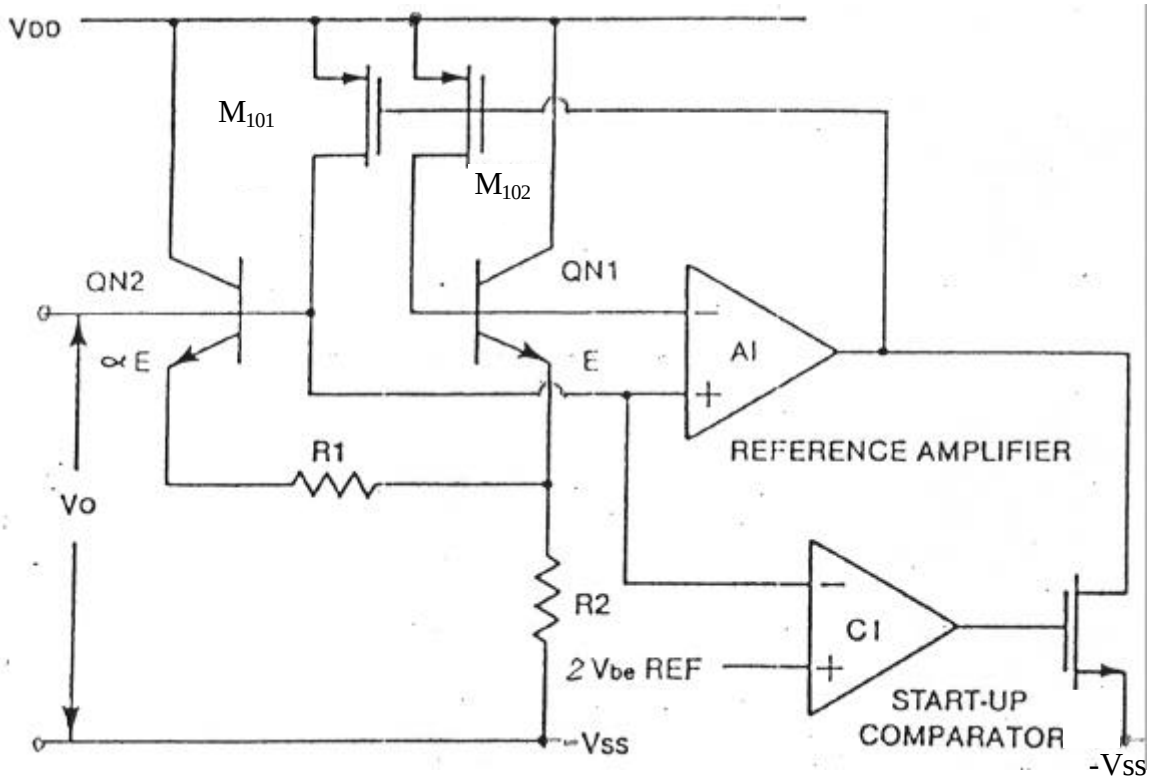

VDD
M110
Q1
Q2
START-UP
COMPARATOR
α E
E
R1
AI
CI
REFERENCE
AMPLIFIER
2 Vbe REF.
R2
R3
Vo
-VSS

4.


VDD
M110
QN1
QN2
α E
α E
R1
R5
START-UP
COMPARATOR
A1
C1
REFERENCE
AMPLIFIER
2 Vbe REF
R2
R3
Vo
R4
-Vss


+VDD
M105
M104
M103
M109
M108
M111
M112
BIAS
BANDGAP
OUTPUT
M110
QN1
QN2
E
IIE
R1
M101
M102
M106
M107
R3
R2
CROSS-COUPLED
INPUTS & LOADS
QN4
QN6
QN5
QN3
Q7
M3
M6
M1
M2
M4
M5
-Vss
REFERENCE AMPLIFIER A1
COMPARATOR C1
2 Vbe REFERENCE

5.Low Power Supply Circuit:



*Low driving capability

Power supply limits:

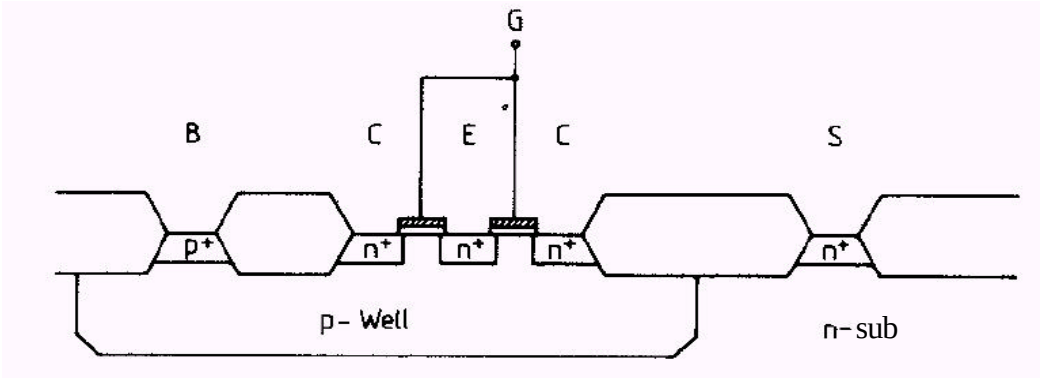
	Low Possible	Voltage T=25°C
Bandgap reference Topology	PMOS Inputs	NMOS Inputs
	$V_{TP} \leq 1.0V$	$V_{TN} \leq 1.0V$
1	1.5v	2.2v
2	1.95v	2.95v
3	1.90v	-
5	2.5v	1.5v

§ 10-3.3 CMOS BGR via lateral Transistor

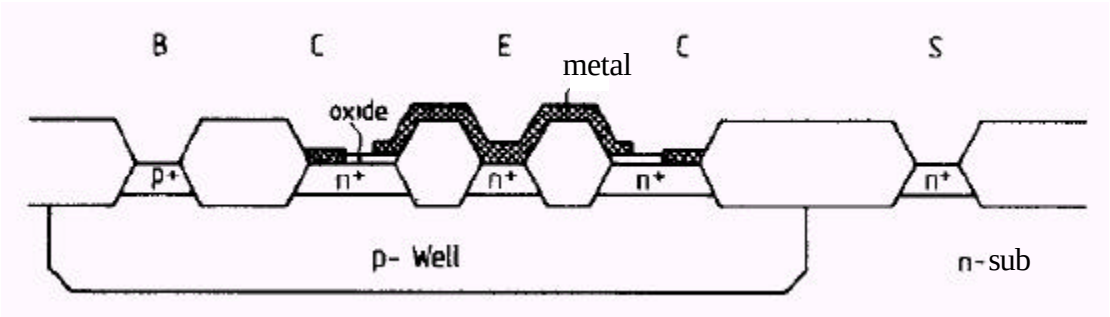
Ref:IEEE J .Solid-State Circuits, vol. SC-20, pp.1151-1157, DEC. 1985

Structure of a lateral BJT in CMOS:

A.

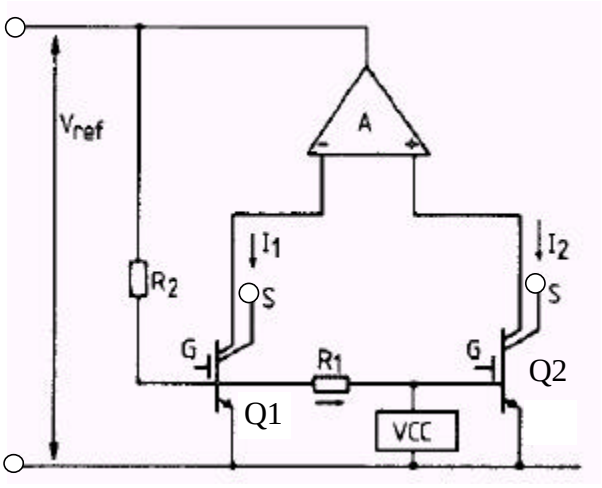


B.

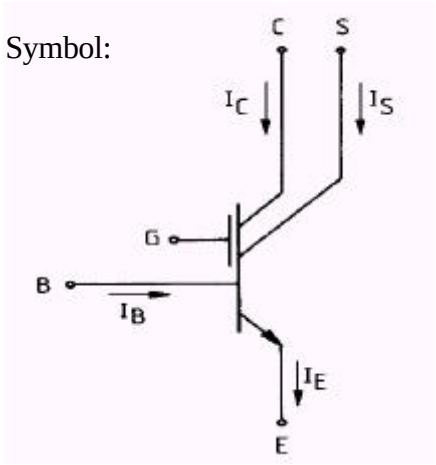


Voltage reference via LBJT:

Conceptual circuit：



Symbol:



A:Current comparator

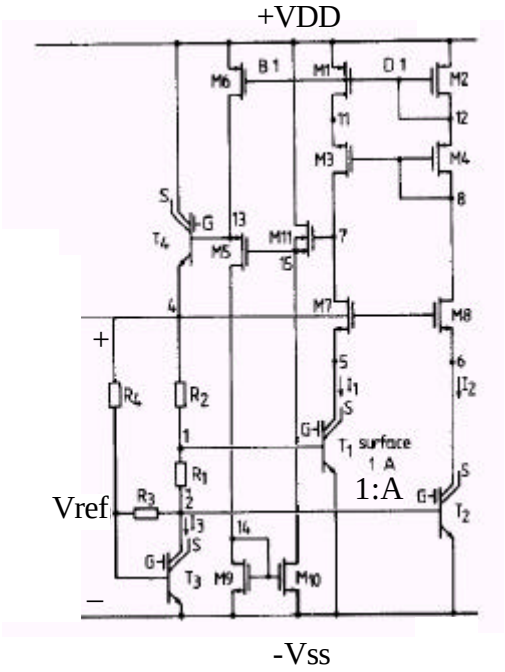
VCC:Voltage-controlled current source

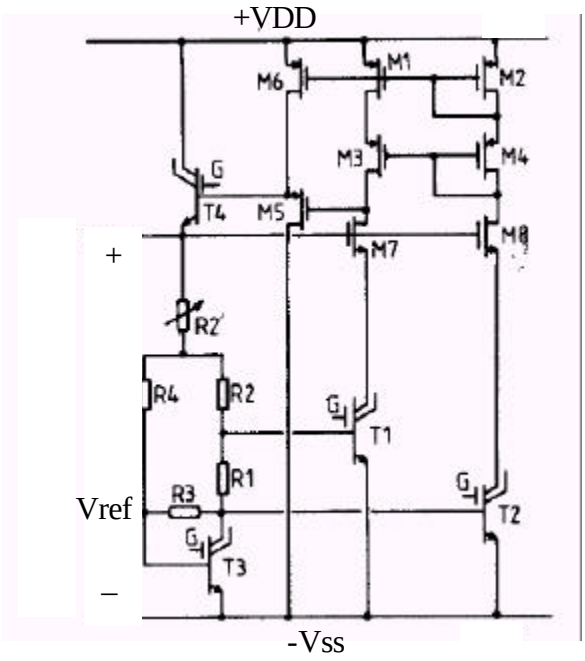
G:A negative voltage is applied to cause accumulation.

Advantages:(1)The offset of the amplifier A has a negligible effect on V_{REF}

(2)Simple structure.

Purpose of VCC : To provide a current path for $I_{R1} >> I_{B1}, I_{B2}$





* High supply voltage.
* Two source follwers+one emitter follower in(A) current amp.=>higher current gain

* Low supply voltage
* Low current gain in A
* R2 is trimmable

R4,R3,T3:VCC

R3: To keep T3 from quasi-saturation

R4:To sense the output voltage and transform it into the collector current of T3.

* All resistor are polyresistors
* Low output impedance.

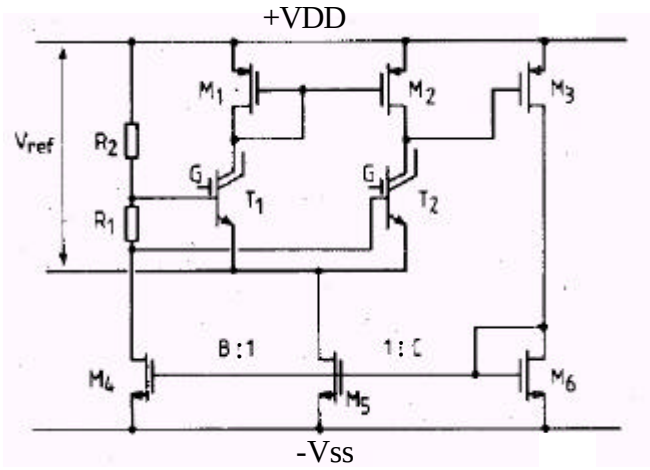
Measured results:

V_{REF} mean :1.2285V ;	standard deviation :150ì V
Minimal supply voltage	2.2V
Supply current	79ì A
Noise spectra	$316nV/\sqrt{Hz}(white)$; $560nV/\sqrt{Hz}(\frac{1}{f},1KHz)$
PSRR(100Hz)	60dB
Load regulation (ÄVout/Iout)	3.6ì V/ì A
Chip area	0.42 mm^2

High PSRR BGR:

* R_1,R_2 may be p-well resistors and PSRR still high.

Experimental results:



V_{REF}	1.2281V (mean)
	350ì V (ó)
Minimal Supply	1.7V
Supply Current	20ì A
Noise Spectra	$500nV/\sqrt{Hz}(white)$
	$1mV/\sqrt{Hz}(\frac{1}{f},1KHz)$
PSRR(100Hz)	77dB
Load Regulation ($ÄV_{out}/I_{out}$)	4.1mv/ì A
Chip area	0.18 mm^2

Curvature-Compensated BGR:

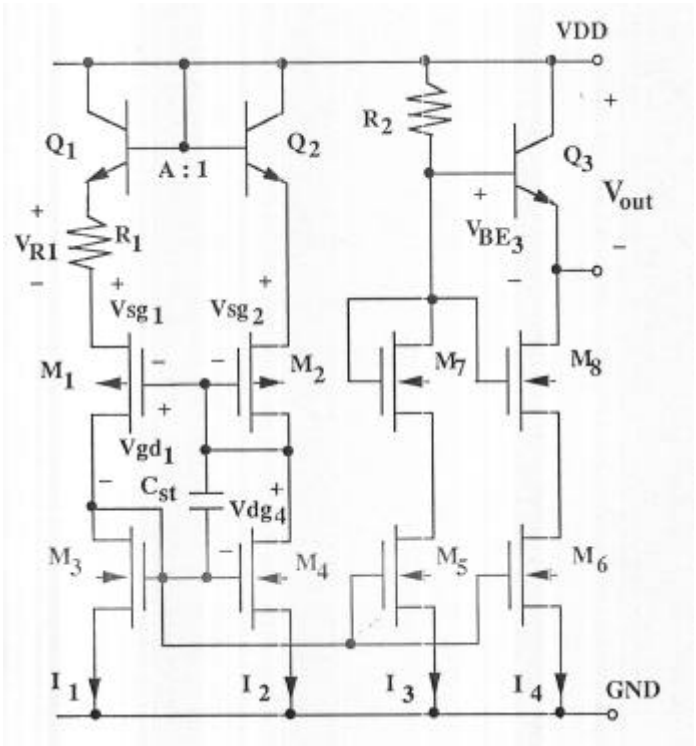
Ref: IEEE J. Solid-State Circuits, vol. sc-20, pp.1283-1285, Dec. 1985

§10-4 High-Precision Curvature-Compensated CMOS Bandgap Voltage References (BVR)

Ref: Int. J. of Analog ICs and Signal Processing, Kluwer, pp. 207-215, 1992

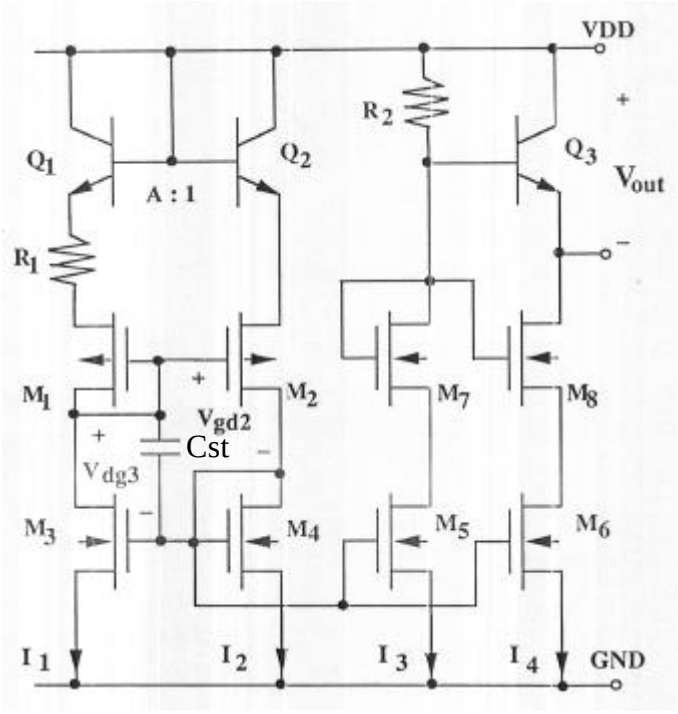
1. Type A structure

The circuit stricture of the proposed BVR (Type A)

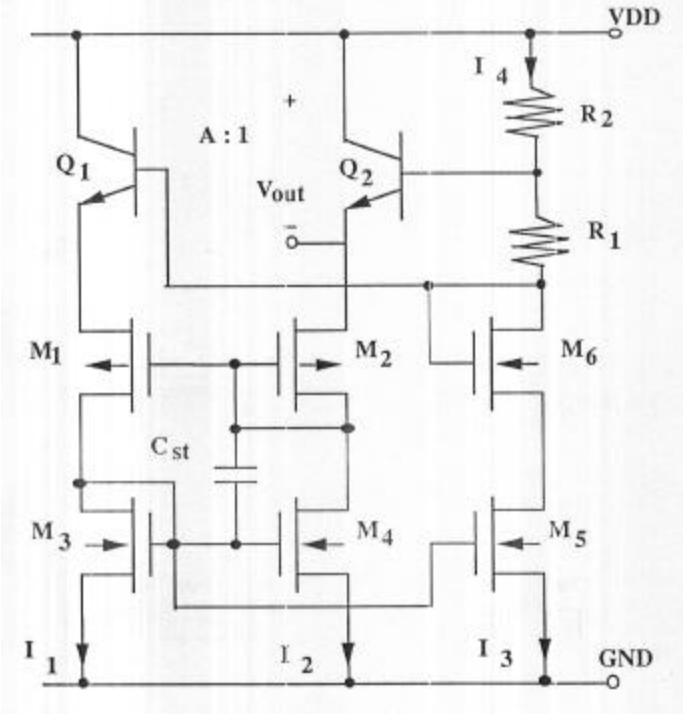


$$V_{out} = V_{BE3} + I_3 R_2 = V_{BE3} + r_3 \frac{R_2}{R_1}\left(\frac{kT}{q}\ln A^* + \Delta V_{sg}\right)$$

2. Type $\bar{A}$ structure

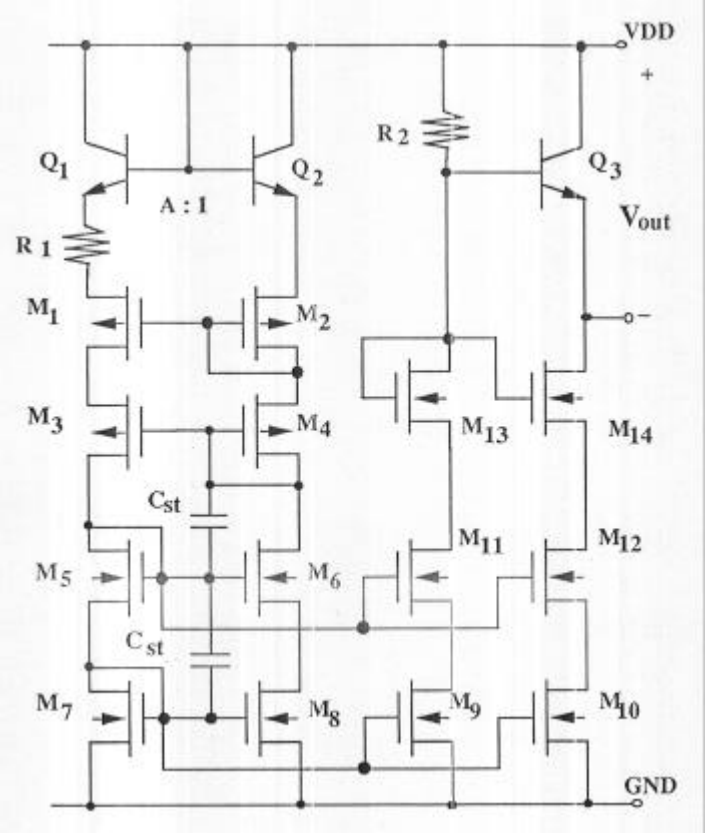


3. Type B structure

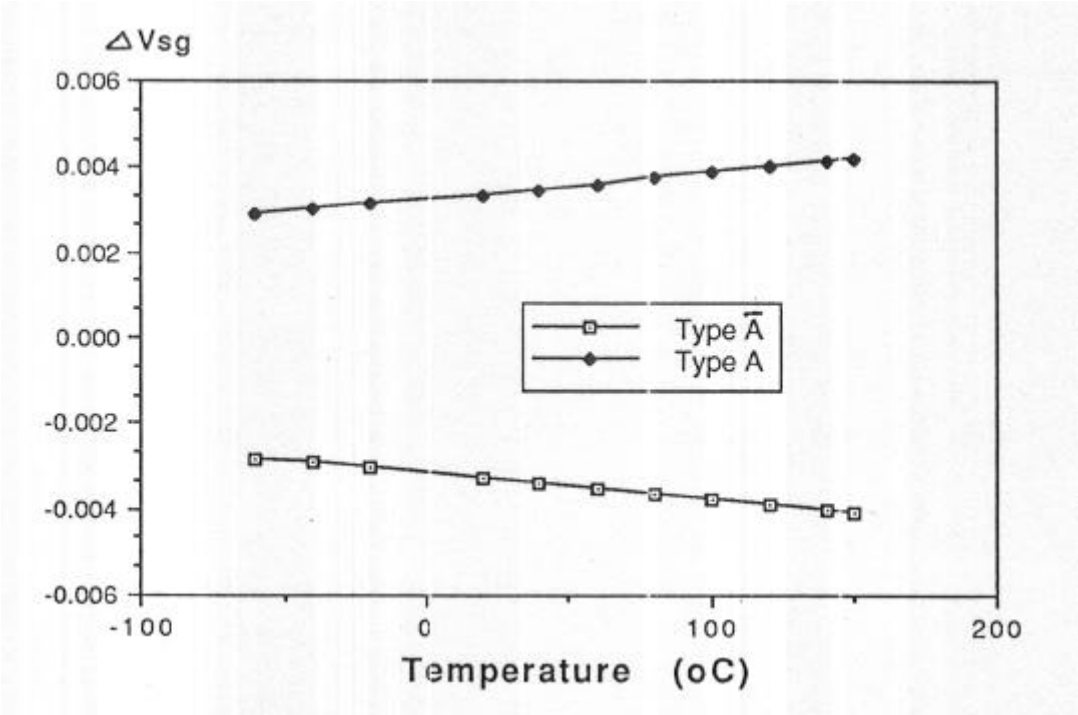


4. Type C structure

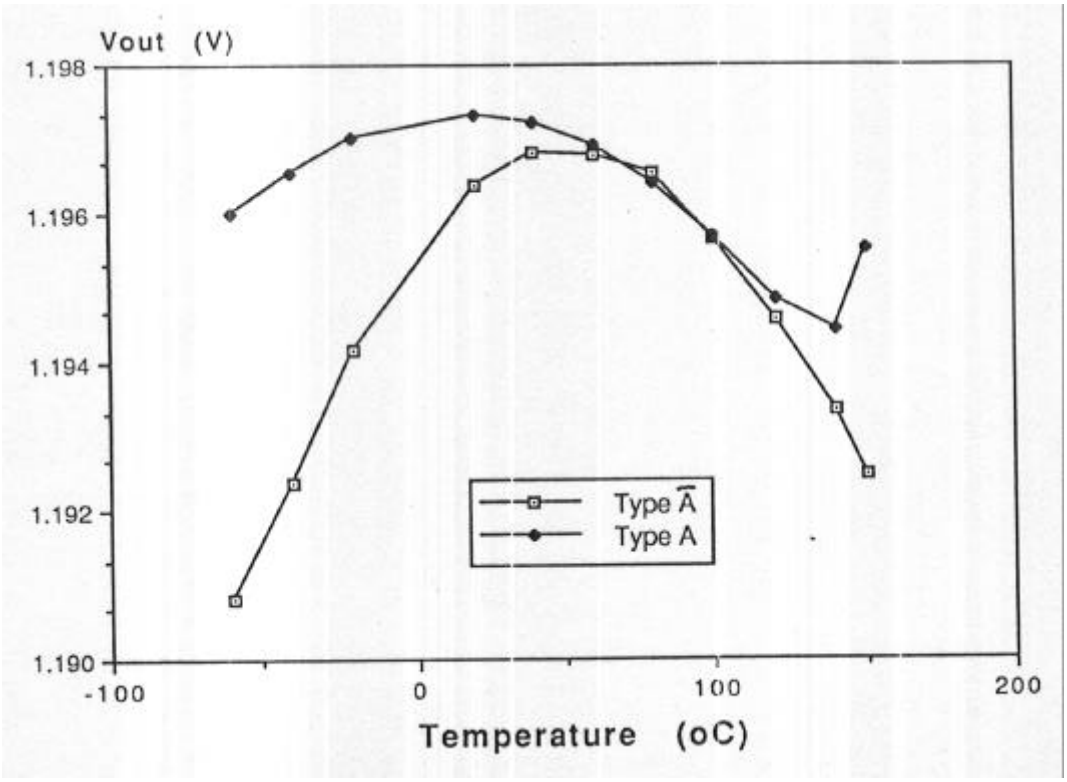
The cascode structure of BVR (Type C):



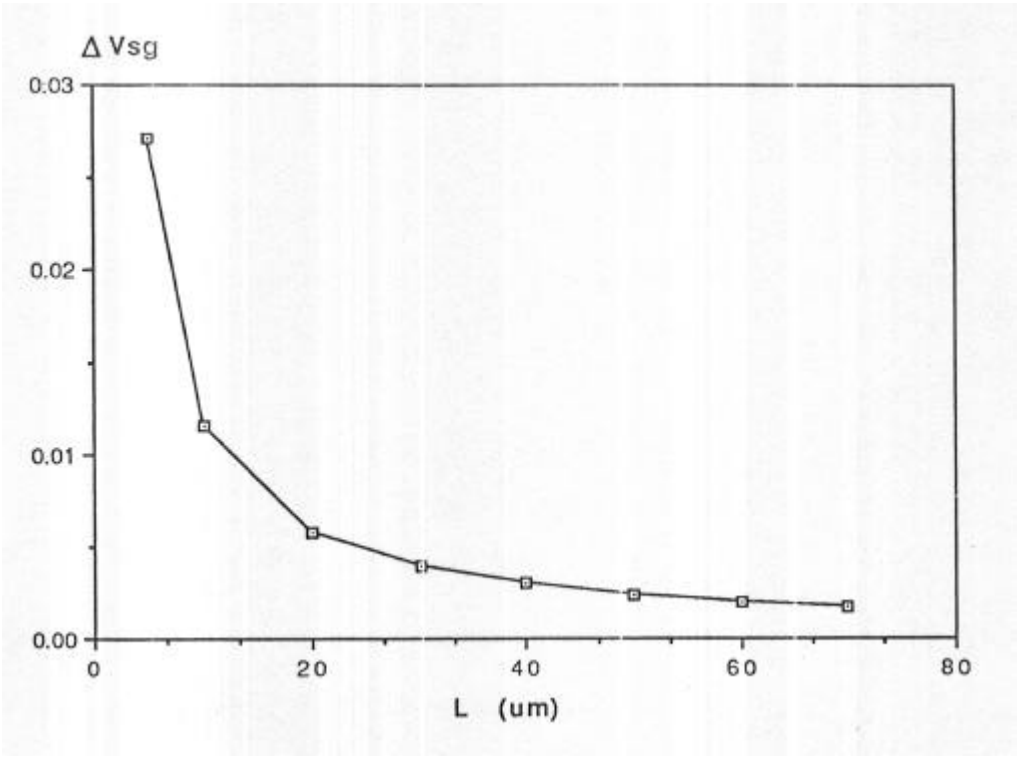
The variation of △Vsg versus temperature



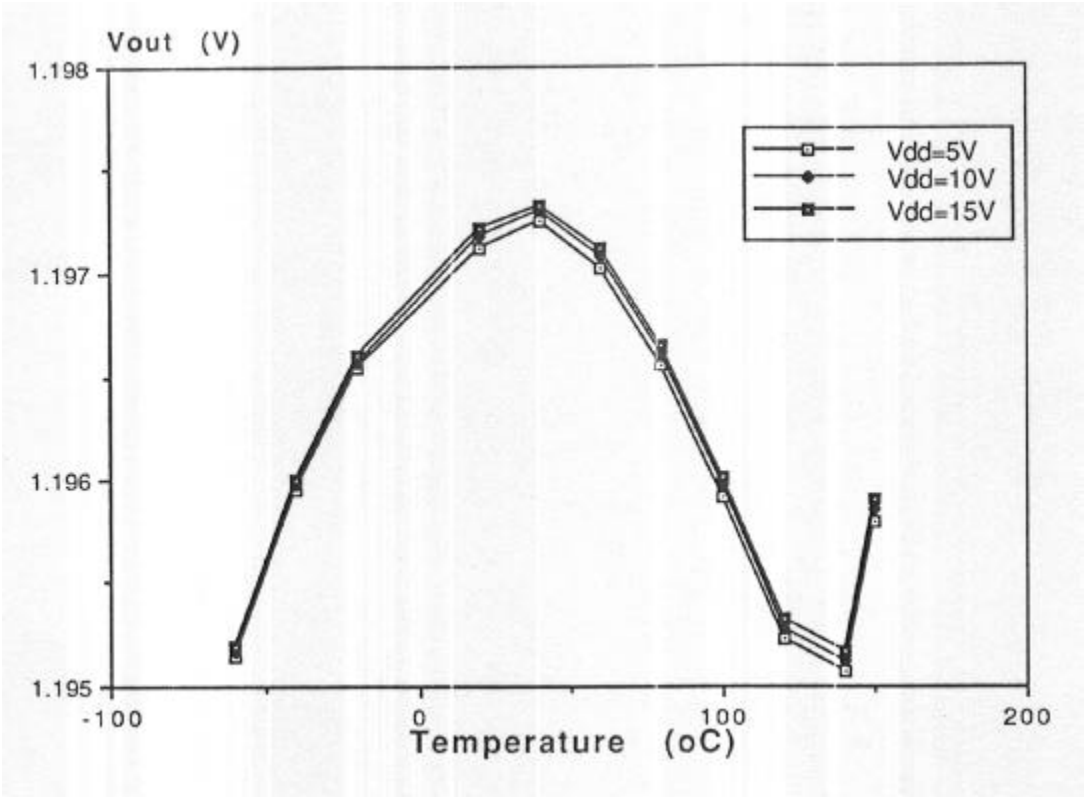
The simulated output voltages versus temperature in Type A and Type A $\bar{B}$VR



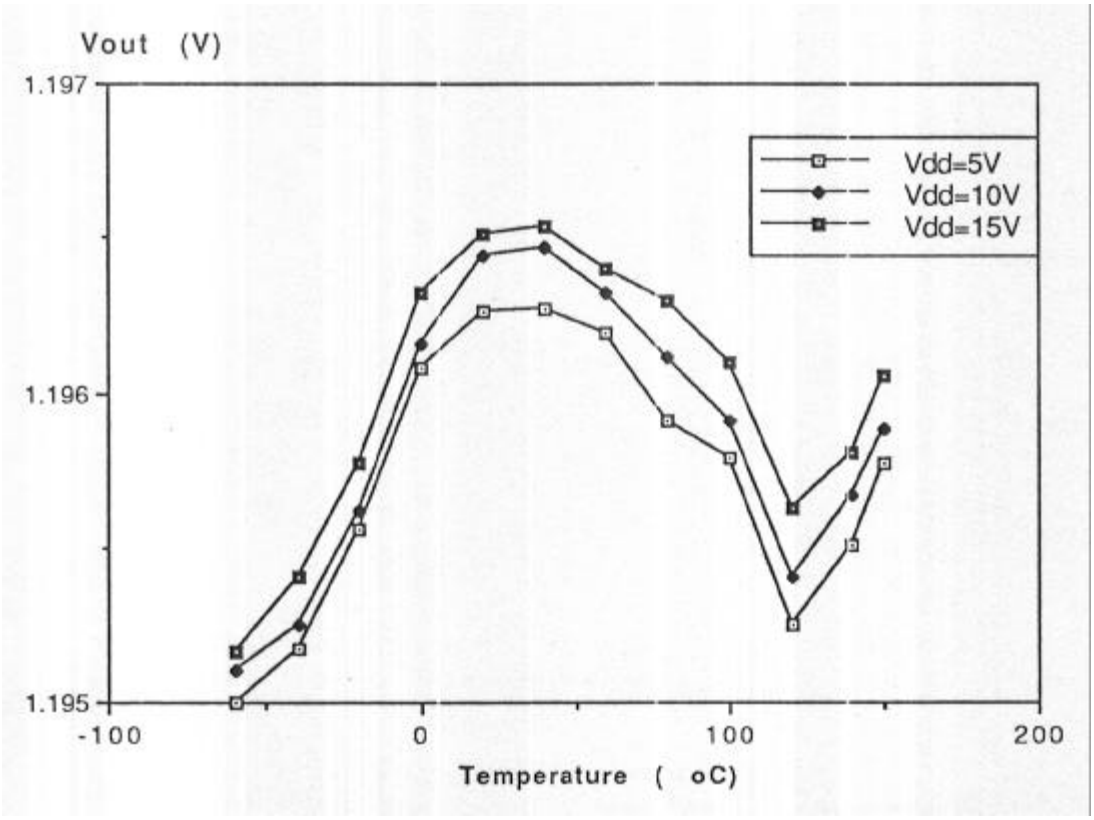
The variation of △Vsg versus MOS channel length in Type A BVR



The Spice simulated output voltages versus temperature in Type C BVR



The measured output voltages versus temperature in the fabricared cascaded-structure BVR(Type C)[3.5 ì m CMOS technology , R_1=1KÙ(external),R_2=25.9KÙ(external)]



* Average temperature drift

  5.5 ppm/^{o}C -60 ^{o}C ~ +150 ^{o}C

  5V~15V

* At 25 ^{o}C, average voltage drift 25ì V/V

  Vout=1.1963V ~ 1.1965V

  5V ~ 15V

* 2 mil^2 , 0.8 mW at 5V

§10-5 CMOS Bandgap Reference with Sub-1-V Operation

Ref.: IEEE JSSC, vol.34, pp.670~674, May 1999

Concept: * Convertional BGR $V_{ref} = 1.25V$

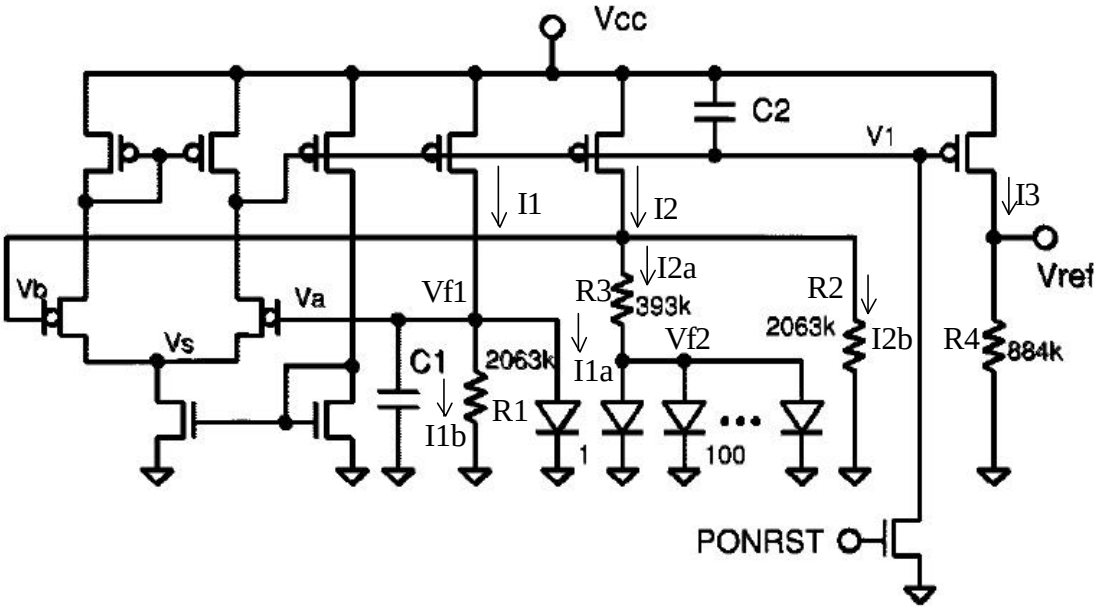
Can' t be operated below 1V supply.

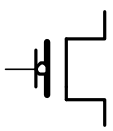
* The built-in voltage V_f of the diode $\rightarrow$ the current I_{2b}

The thermal voltage V_{therm} $\rightarrow$ the current I_{2a}

$(I_{2a} + I_{2b})R \rightarrow V_{ref} < 1V$

1.Schematic of the proposed BGR



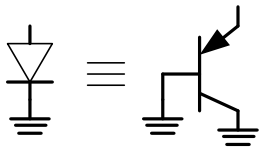


Native NMOS $V_{THI} = -0.2V$

NMOS $V_{THN} = +0.7V$

PMOS $V_{THP} = -1.0V$

*The diode is realized by the parasitic $P^+ / n-well / P-substract$ BJT as



*C_1 and C_2 are used to stabilized the circuit.

*The control signal PONRST is used to initialize the BGR circuit when the power is turned on.

* $R_1 = R_2$

$V_a = V_b$

$I_1 = I_2 = I_3$ and $I_{1a} = I_{2a}$, $I_{1b} = I_{2b}$

$dV_f = V_{f1} - V_{f2} = V_{therm} \ln(N)$, $N = 100$

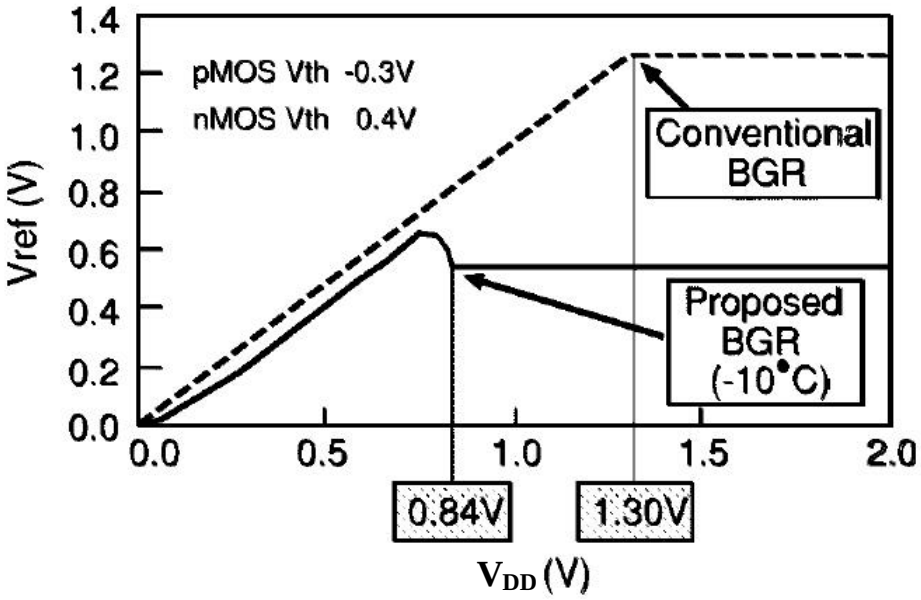
$$I_{2a} = \frac{dV_f}{R_3} \propto V_{therm}$$

$$I_{2b} = \frac{V_{f1}}{R_2} \propto V_f$$

$$I_3 = I_2 = I_{2a} + I_{2b}$$

$$V_{ref} = R_4 I_3 = \frac{R_4}{R_2} V_{f1} + \frac{R_4}{R_3} dV_f$$

2. Simulated V_{ref} characteristics



*$V_{ref} = 1.25V$ conventional BGR

*$V_{ref} = 0.84V$ proposed BGR

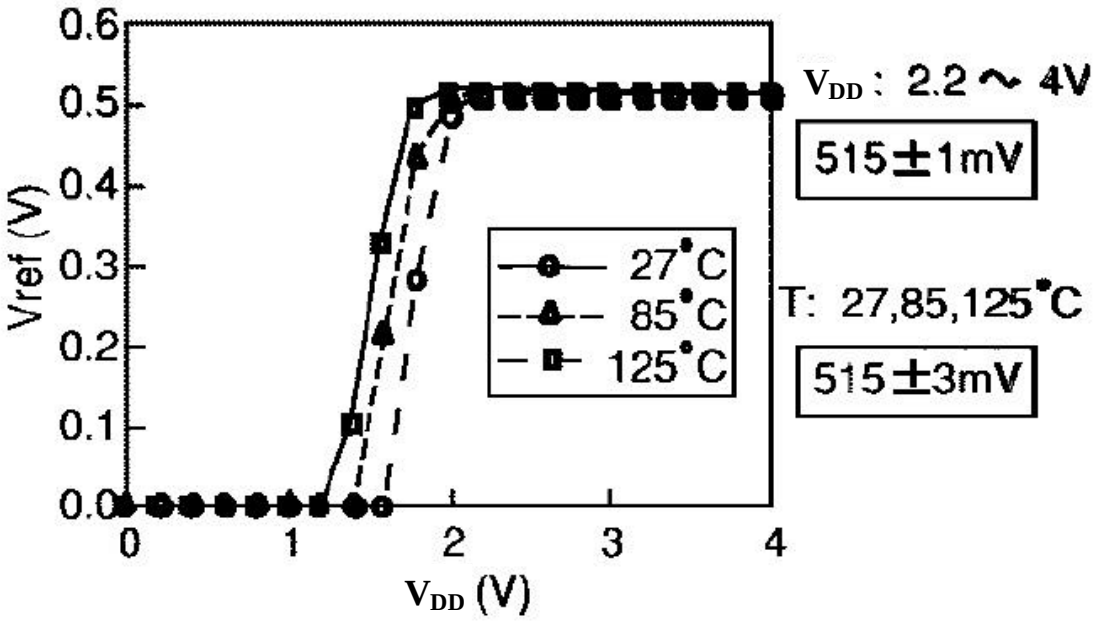
3.Minimum V_{DD}

$$\min\ V_1 \cong V_s \cong V_b - V_{THI} \cong V_f + |V_{THI}| \cong V_{DD} + V_{THP} = \min V_{DD} - |V_{THP}|$$

$$\Rightarrow \min V_{DD} = V_f + |V_{THI}| + |V_{THP}| \cong 0.8 \sim 1.0V$$

0.54 -0.2 -0.3

4.Measured results:



*$TC \cong 60\,ppm/^{O}C$ $27^{O} \sim 125^{O}C$

Voltage drift (average) $\cong 600mV/V$ 2.2V~4V