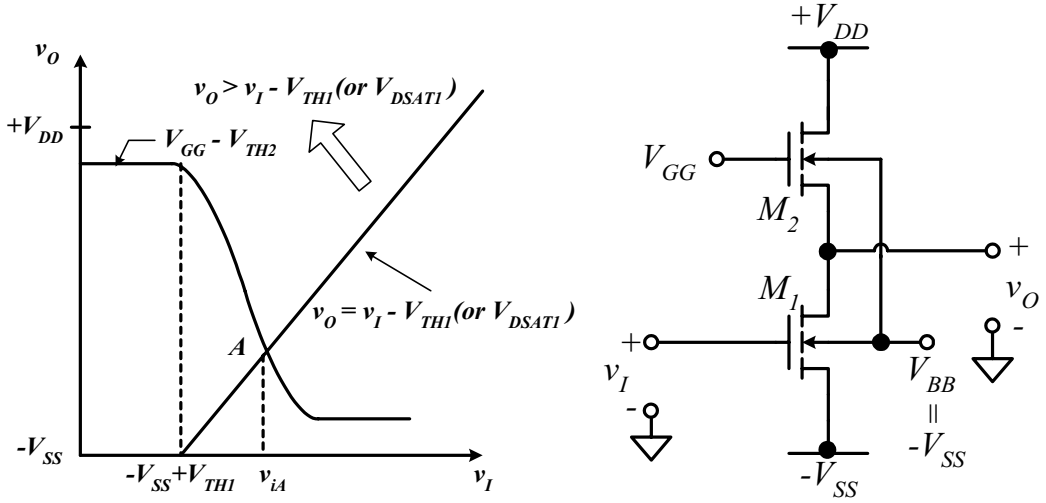
Chapter 4 CMOS Amplifiers, Level Shifting Circuits, and Output stages

4-1 Active-Load MOS Amplifiers

4-1.1 NMOS Amplifiers

1. Simple NMOS common-source amplifier



* M_1 and M_2 must be always biased in the saturation region.

* M_1 sat $\Rightarrow \; v_O \geq V_{DSAT1} \leq v_I - V_{TH1}$

  M_2 sat $\Rightarrow \; V_{DD} - v_O \geq V_{DSAT2} \leq V_{GG} - V_{TH2} - v_O$

* $V_{GG} < V_{DD} + V_{TH2} \Rightarrow V_{GG} < V_{DD}$

Transfer characteristic:

Assume $\lambda \to 0$, $GAMMA \to 0$, and the same $\mu_n C_{ox}$

$$\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (v_I + V_{SS} - V_{TH2})^m = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GG} - v_O - V_{TH2})^m, 1 \leq m \leq 2$$

$$\Rightarrow v_O = V_{GG} - \left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}} (v_I + V_{SS} - V_{TH1}) - V_{TH2}$$

$V_{ODC} \propto V_{IDC}$

At point A , $v_{IA} = v_{OA} + V_{TH1}$

$$\Rightarrow v_{OA} = \frac{\left(V_{GG} - V_{TH2} - \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}} V_{SS} \right)}{1 + \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}}}$$

The range of v_O in which both MOS are in the saturation region is

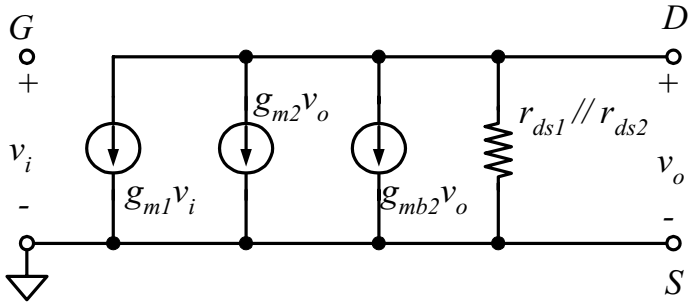
$$V_{GG} - V_{TH2} > v_O \geq \frac{\left(V_{GG} - V_{TH2} - \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}} V_{SS} \right)}{1 + \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}}} \text{ or } V_{DSAT1}$$

$$A_v \equiv \frac{\partial v_O}{\partial v_I} = -\left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}} \quad , \quad (W/L)_2 < 1 \text{ for high } A_v$$

The range for v_I is

$$-V_{SS} + V_{TH1} \leq v_I \leq \frac{\left(V_{GG} - V_{TH2} - \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}} V_{SS} \right)}{1 + \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}}} + V_{TH1} \text{ (or } v_{IA})$$

Small-signal model:



$$A_v \equiv \frac{v_o}{v_I} = -\frac{g_{m1}}{g_{m2} + g_{mb2} + \frac{1}{r_{ds1} || r_{ds2}}} \approx -\frac{g_{m1}}{g_{m2} + g_{mb2}}$$

if $(g_{m2} + g_{mb2}) >> \frac{1}{r_{ds1} || r_{ds2}}$

$$A_v = -\frac{g_{m1}}{g_{m2}} \cdot \frac{1}{1 + \eta_2} = -\alpha_2 \frac{g_{m1}}{g_{m2}}$$

where $\eta_2 = \dfrac{GAMMA_2}{2\sqrt{V_{BB} + v_O + \phi_S}}$ $\qquad \alpha_2 \equiv \dfrac{1}{1+\eta_2}$

$g_m = 2\sqrt{\dfrac{\mu_n C_{ox}}{2}\left(\dfrac{W}{L}\right)\cdot I_{DS}}$ or $m\left(\dfrac{\mu_n C_{ox}}{2}\cdot\dfrac{W}{L}\cdot {I_{DS}}^{m-1}\right)^{\frac{1}{m}}$

$\Rightarrow A_v = -\alpha_2\sqrt{(W/L)_1 \big/ (W/L)_2}$ or $-\alpha_2[(W/L)_1 \big/ (W/L)_2]^{\frac{1}{m}}, \quad 1 < m < 2$

If $\eta_2 << 0$, $\alpha_2 = 1$. ($GAMMA_2 \downarrow$, $V_{BB} + v_O \uparrow \Rightarrow \eta_2 \downarrow$)

$\Rightarrow A_v = -\sqrt{(W/L)_1 \big/ (W/L)_2}$ or $\left[-(W/L)_1 \big/ (W/L)_2\right]^{\frac{1}{m}}$

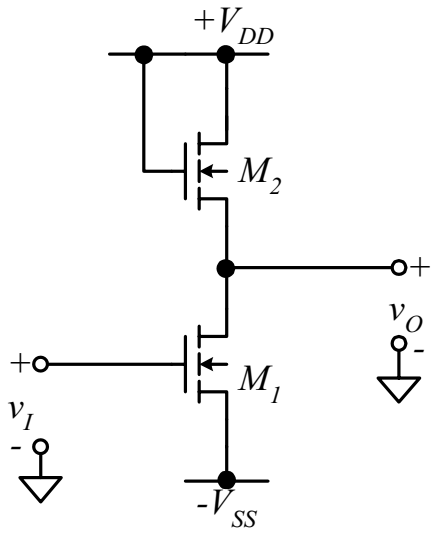
* The voltage gain is determined by the geometeric ratio.

  Example: $(W/L)_1 = 10 \quad (W/L)_2 = 0.1 \quad \alpha_2 = 1$

  $\Rightarrow A_v = -\sqrt{100} = -10$

* The body effect of M_2 degrades the voltage gain.
* The dc output voltage is dependent on the input dc bias voltage or equivalently the dc operating current.

2. NMOS inverter without V_{GG}



Amplifier range:

$$V_{DD} - V_{TH2} > v_O \geq \frac{\left(V_{DD} - V_{TH2} - \left(\dfrac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}} V_{SS}\right)}{1 + \left(\dfrac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}} \quad \text{or } V_{DSAT1}$$

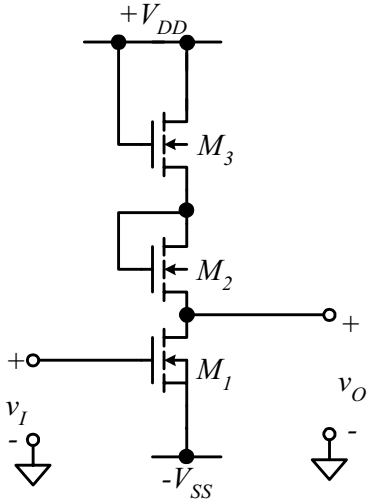
$$-V_{SS}+V_{TH1}\le v_I\le \frac{\left(V_{DD}-V_{TH2}-\left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}V_{SS}\right)}{1+\left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}}+V_{TH1}$$ or v_{IA}

$$V_{ODC}=V_{DD}-\left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}(V_{IDC}+V_{SS}-V_{TH1})-V_{TH2}$$

* No extra power supply V_{GG} is required.

* $A_v=-\alpha_2\left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}\Rightarrow (W/L)_2<1$ for high A_v

3. Split-Load inverter



Single M_2 $\Rightarrow (W/L)_2<<1$ very long channel device

$$C_{gs2}=\frac{2}{3}C_{ox}(L\cdot W)_2=\frac{2}{3}C_{ox}\frac{W^2}{(W/L)_2}$$

$$(W/L)_2<<1\Rightarrow C_{gs2}\uparrow$$

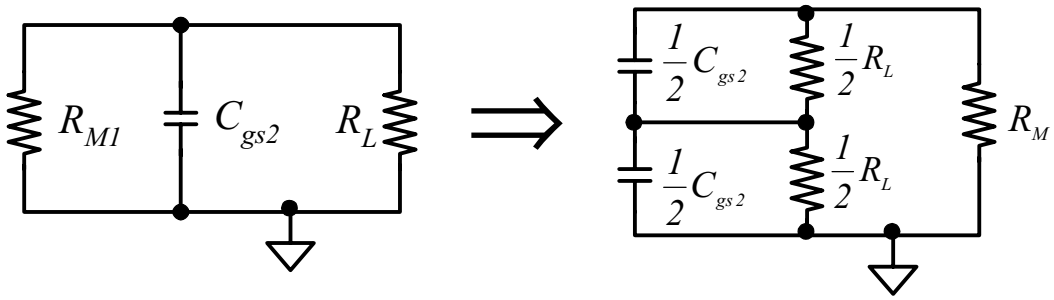
$$f_{-3dB}\approx\frac{1}{2\pi\frac{1}{g_{m2}}C_{gs2}}=\frac{3I_{DS}{}^2}{2\pi\frac{\mu_nC_{ox}}{2}W^2C_{ox}(V_{GS2}-V_{TH2})^3}$$

$$I_{DS}\uparrow\Rightarrow f_{-3dB}\uparrow\ ;\ C_{gs2}\uparrow\Rightarrow f_{-3dB}\downarrow$$

$\Rightarrow$ Split load

(1) RC time constant $\downarrow$ $\quad f_{-3dB} \uparrow$

(2) Gain is nearly unchanged



$$C_{gs2}(R_L \,//\, R_{M1}) \cong R_L C_{gs2}$$

$$\frac{1}{2}C_{gs2}[\frac{1}{2}R_L \,//(\frac{1}{2}R_L + R_{M1})] + \frac{1}{2}C_{gs2}[\frac{1}{2}R_L \,//(\frac{1}{2}R_L + R_{M1})] \cong \frac{1}{2}R_L C_{gs2}$$

4. NMOS Cascode amplifier

If $I_{DS1} = I_{DS2}$

$$A_{v1} \equiv \frac{v_{D1}}{v_I} = -\alpha_2 \frac{g_{m1}}{g_{m2}} = -\alpha_2 \left[\frac{(W/L)_1}{(W/L)_2}\right]^{1/m}$$

If $I_{DS1} = I_{DS3}$

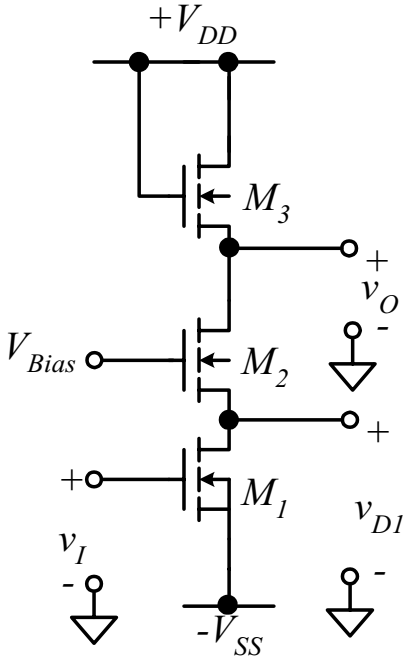
$$A_v \equiv \frac{v_O}{v_I} = -\alpha_3 \frac{g_{m1}}{g_{m3}} = -\alpha_3 \left[\frac{(W/L)_1}{(W/L)_3}\right]^{1/m}$$

$$C_{in} = C_{gs1} + C_{gd1}\left(1 + \frac{g_{m1}}{g_{m2}}\right)$$

If $g_{m1} = g_{m2}$

$\Rightarrow C_{in} = C_{gs1} + 2C_{gd1}$

$C_{in} \propto g_{m1}/g_{m2}$



* Design considerations:

(1) $\left(W/L\right)_1 = \left(W/L\right)_2 \Rightarrow g_{m1} = g_{m2}$ (Neglecting the body effect of M_2)

Keep C_{in} Small , Miller Effect $\downarrow$

(2) $\left(W/L\right)_3 << \left(W/L\right)_1 \Rightarrow g_{m3} << g_{m1}$, Voltage gain $A_v \uparrow$

(3) $V_{DS2}(V_{DS1})$ must be large enough to keep $M_2(M_1)$ sat.

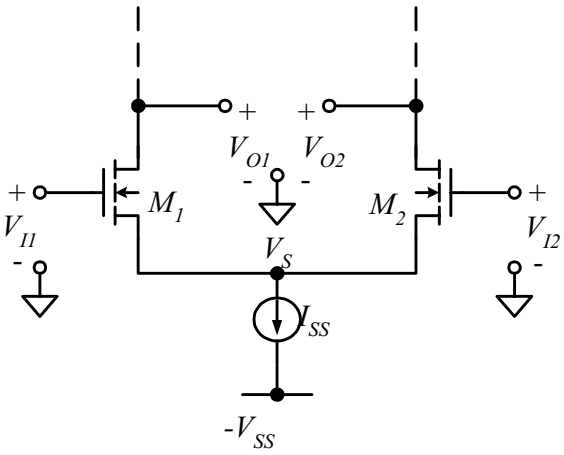
* $g_{m1} < g_{m2} \Rightarrow A_{v1} < 1 \Rightarrow$ Smaller Miller effect

But $\left(W/L\right)_1 < \left(W/L\right)_2$ is not recommended.

$\because$ V_{DS1} will become smaller $\Rightarrow M_1$ may not be in the sat. region.

* $\left(W/L\right)_2 > \left(W/L\right)_1$ slightly to compensate the body effect of M_2 .

5. MOS source-couple pair



$$I_{DS1} = \left(\frac{\mu_n C_{ox}}{2}\right)_1 \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2$$

$$I_{DS2} = \left(\frac{\mu_n C_{ox}}{2}\right)_2 \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2$$

$$I_{DS1} + I_{DS2} = I_{SS}$$

$$V_{GS1} = V_{I1} - V_S$$

$$V_{GS2} = V_{I2} - V_S$$

Assume identical devices

i.e. $V_{TH1} = V_{TH2}, \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$ and $\left(\frac{\mu_n C_{ox}}{2}\right)_1 = \left(\frac{\mu_n C_{ox}}{2}\right)_2 = \frac{\mu_n C_{ox}}{2}$

$$\Rightarrow \Delta I_{DS} \equiv I_{Ds1} - I_{DS2} = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(\Delta V_I)\sqrt{\frac{2I_{SS}}{\frac{\mu_n C_{OX}}{2}\frac{W}{L}} - (\Delta V_I)^2}$$

where $\Delta V_I \equiv V_{I1} - V_{I2}$ (input differential voltage)

If $\Delta V_I \le \sqrt{\frac{I_{SS}}{\frac{\mu_n C_{OX}}{2}\frac{W}{L}}}$

$\Rightarrow \Delta I_D \propto \Delta V_I$, linear range

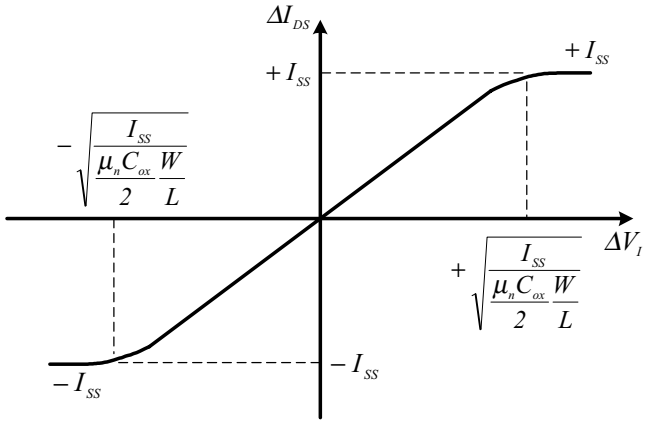
$\Rightarrow$ between $+\frac{I_{SS}}{2}$ and $-\frac{I_{SS}}{2}$.

Linear range $\propto \sqrt{I_{SS}}, \frac{L}{W}$

Typically, $\Delta V_I \approx \pm 300mv$ to

$\pm V$ in the linear range,

Larger than that of the emitter-couple pair.



$$G_m \equiv \left.\frac{\partial \Delta I_{DS}}{\partial \Delta V_I}\right|_{\Delta V_I=0} = \left(\frac{\mu_n C_{OX}}{2}\frac{W}{L}\right)\sqrt{\frac{2I_{SS}}{\frac{\mu_n C_{OX}}{2}\frac{W}{L}} - (\Delta V_I)^2} - \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)\Delta V_I$$

$$\left.\frac{\Delta V_I}{\sqrt{\frac{2I_{SS}}{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)} - (\Delta V_I)^2}}\right|_{\Delta V_I=0}$$

$$= 2\sqrt{\frac{I_{SS}}{2}\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)} = g_{m1} \text{ or } g_{m2}$$

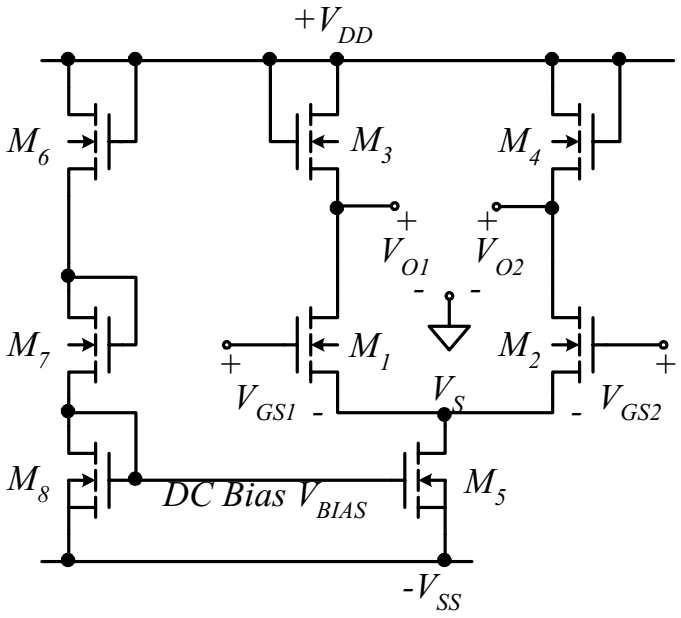
$$= \sqrt{I_{SS}(\mu_n C_{ox})\left(\frac{W}{L}\right)}$$

* Gm is the differential output transconductance

Gm at $\Delta V_I=0$ is the maximum.

* If operated in the subthreshold region, Gm max = g_{m1} or $g_{m2}=\frac{I_{DS}}{nv_t}$

6. NMOS differential stage



DC considerations :

(1) Transfer characteristic :

$(W/L)_1=(W/L)_2$ $(W/L)_3=(W/L)_4$

Source-coupled pair M_1 and M_2

$$\Rightarrow \Delta I_{DS} \equiv I_{DS1} - I_{DS2} = (\frac{\mu_n C_{ox}}{2}\frac{W}{L})_1(\Delta V_I)\sqrt{\frac{2I_{SS}}{(\frac{\mu_n C_{ox}}{2}\frac{W}{L})_1} - (\Delta V_I)^2}$$

where $\Delta V_I \equiv V_{I1} - V_{I2}$

$$I_{DS3} = I_{DS1} = \frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3(V_{DD} - V_{O1} - V_{TH3})^2$$

$$I_{DS4} = I_{DS2} = \frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3(V_{DD} - V_{O2} - V_{TH4})^2$$

$$V_{O1} = V_{DD} - V_{TH3} - \sqrt{\frac{I_{DS1}}{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}} \qquad V_{O2} = V_{DD} - V_{TH4} - \sqrt{\frac{I_{DS2}}{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}}$$

$$\Delta V_O \equiv V_{O1} - V_{O2} = V_{TH4} + \sqrt{\frac{I_{DS2}}{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}} - V_{TH3} - \sqrt{\frac{I_{DS1}}{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}}$$

$$= (V_{TH4} - V_{TH3}) + \frac{1}{\sqrt{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}}(\sqrt{\frac{I_{SS}}{2} - \frac{\Delta I_{DS}}{2}} - \sqrt{\frac{I_{SS}}{2} + \frac{\Delta I_{DS}}{2}})$$

$$= f(I_{SS}, \Delta V_I)$$

$\Rightarrow \Delta V_O$ *vs* ΔV_I is the voltage transfer characteristic.

(2) Input voltage limits :

Positive maximum common-mode voltage V_{ICM}^+

$$V_{ICM}^+ = V_{O1} + V_{TH1} = V_{DD} - V_{TH3} - \sqrt{\frac{I_{SS}/2}{(\mu_n C_{ox}/2)(W/L)_3}} + V_{TH1}$$

(long-channel device)

V_{ICM}^+ such that V_{O1}-V_S=V_{DSAT1} (short-channel device)
(M1 and M2 sat.)

Negative maximum common-mode voltage V_{ICM}^-

M5 must be sat.

$$V_{ICM}^{-} = V_{BIAS} + V_{TH5} + \sqrt{\frac{I_{SS}/2}{(\mu_n C_{ox}/2)(W/L)_1}} + V_{TH1}$$

(long-channel device)

V_{ICM}^{-} such that $V_S+V_{SS}=V_{DSAT5}$ (short-channel device)

Positive maximum differential voltage V_{ID}^{+}

$$V_{ID}^{+} = V_{DD} - V_{TH3} + \sqrt{\frac{I_{SS}}{(\mu_n C_{ox}/2)(W/L)_3}} + V_{TH1}$$ (long-channel device)

V_{ID}^{+} such that $V_{O1}-V_S=V_{DSAT1}$ (short –channel device)

(Keep M1 or M2 sat.)

Negative maximum differential voltage V_{ID}^{-}

$V_{ID}=-V_{ID}^{+}$

(3) Input offset voltage

$$V_{OS} \equiv V_{GS1} - V_{GS2}\Big|_{V = V_2}$$

$$= \sqrt{\frac{I_{DS1}}{(\mu_n C_{ox}/2)_1(W/L)_1}} + V_{TH1} - \sqrt{\frac{I_{DS2}}{(\mu_n C_{ox}/2)_2(W/L)_2}} - V_{TH2}$$

$$V_{O1} = V_{O2} = V_O = V_{DD} - V_{TH3} - \sqrt{\frac{I_{DS1}}{(\mu_n C_{ox}/2)_3(W/L)_3}}$$

$$= V_{DD} - V_{TH4} - \sqrt{\frac{I_{DS1}}{(\mu_n C_{ox}/2)_4(W/L)_4}}$$

$$\Rightarrow \sqrt{I_{DS1}} = \sqrt{(\mu_n C_{ox}/2)_3(W/L)_3}(V_{DD} - V_{TH3} - V_O)$$

$$\sqrt{I_{DS2}} = \sqrt{(\mu_n C_{ox}/2)_4(W/L)_4}(V_{DD} - V_{TH4} - V_O)$$

$$\Rightarrow V_{OS}=\sqrt{\frac{\left(\frac{\mu_n C_{OX}}{2}\right)_3\left(\frac{W}{L}\right)_3}{\left(\frac{\mu_n C_{OX}}{2}\right)_1\left(\frac{W}{L}\right)_1}}(V_{DD}-V_O-V_{TH3})$$

$$-\sqrt{\frac{\left(\frac{\mu_n C_{OX}}{2}\right)_4\left(\frac{W}{L}\right)_4}{\left(\frac{\mu_n C_{OX}}{2}\right)_2\left(\frac{W}{L}\right)_2}}(V_{DD}-V_O-V_{TH4})+(V_{TH1}-V_{TH2})$$

Define $\Delta X_2 = X - X_2 \qquad X_2 = -X + X_2)$

$$\Rightarrow X_1 = X_{12}+\frac{\Delta X_{12}}{2} \qquad X_2 = X_{12}-\frac{\Delta X_{12}}{2}$$

$$\Rightarrow V_{OS}=\sqrt{\frac{\left(\frac{\mu_n C_{OX}}{2}\right)_{34}\left(\frac{W}{L}\right)_{34}}{\left(\frac{\mu_n C_{OX}}{2}\right)_{12}\left(\frac{W}{L}\right)_{12}}}(V_{DD}-V_O-V_{TH34})[\frac{\Delta\left(\frac{\mu_n C_{OX}}{2}\right)_{34}}{2\left(\frac{\mu_n C_{OX}}{2}\right)_{34}}+\frac{\Delta\left(\frac{W}{L}\right)_{34}}{2\left(\frac{W}{L}\right)_{34}}$$

$$-\frac{\Delta\left(\frac{\mu_n C_{OX}}{2}\right)_{12}}{2\left(\frac{\mu_n C_{OX}}{2}\right)_{12}}-\frac{\Delta\left(\frac{W}{L}\right)_{12}}{2\left(\frac{W}{L}\right)_{12}}-\frac{\Delta V_{TH34}}{V_{DD}-V_O-V_{TH34}}]+\Delta V_{TH12}$$

$$=\sqrt{\frac{I_{DS34}}{(\frac{\mu_n C_{ox}}{2})_{12}(\frac{W}{L})_{12}}}\left[\frac{\Delta(\frac{\mu_n C_{ox}}{2})_{34}}{2(\frac{\mu_n C_{ox}}{2})_{34}}-\frac{\Delta L_{34}}{2L_{34}}+\frac{\Delta W_{34}}{2W_{34}}-\frac{\Delta(\frac{\mu_n C_{ox}}{2})_{12}}{2(\frac{\mu_n C_{ox}}{2})_{12}}-\frac{\Delta W_{12}}{2W_{12}}+\frac{\Delta L_{12}}{2L_{12}}\right]$$

$$-\sqrt{\frac{\left(\frac{\mu_n C_{OX}}{2}\right)_{34}\left(\frac{W}{L}\right)_{34}}{\left(\frac{\mu_n C_{OX}}{2}\right)_{12}\left(\frac{W}{L}\right)_{12}}}\Delta V_{TH34}+\Delta V_{TH12}$$

$$\cong\sqrt{\frac{I_{DS34}}{(\frac{\mu_n C_{ox}}{2})_{12}(\frac{W}{L})_{12}}}\left[\frac{\Delta W_{34}}{2W_{34}}+\frac{\Delta L_{12}}{2L_{12}}\right]+\Delta V_{TH12}-\sqrt{\frac{(\frac{\mu_n C_{ox}}{2})_{34}(\frac{W}{L})_{34}}{(\frac{\mu_n C_{ox}}{2})_{12}(\frac{W}{L})_{12}}}\Delta V_{TH34}$$

$$=\Delta V_{TH12}+(V_{GS12}-V_{TH12})\left[\frac{\Delta W_{34}}{2W_{34}}+\frac{\Delta L_{12}}{2L_{12}}\right]-\sqrt{\frac{(\frac{W}{L})_{34}}{(\frac{W}{L})_{12}}}\Delta V_{TH34}$$

* If ΔV_{TH} is large and the differential gain is high,

$V_{OS} \cong \Delta V_{TH12}$

* If $\frac{\Delta W}{2W}$ and $\frac{\Delta L}{2L}$ is large , keep $V_{GS12} - V_{TH12}$ small.

$$\Rightarrow V_{OS} \cong (V_{GS} - V_{TH12})(\frac{\Delta W_{34}}{2W_{34}} + \frac{\Delta L_{12}}{2L_{12}})$$

$V_{OS} \propto$ input overdrive voltage

* If operated in the subthreshold region,

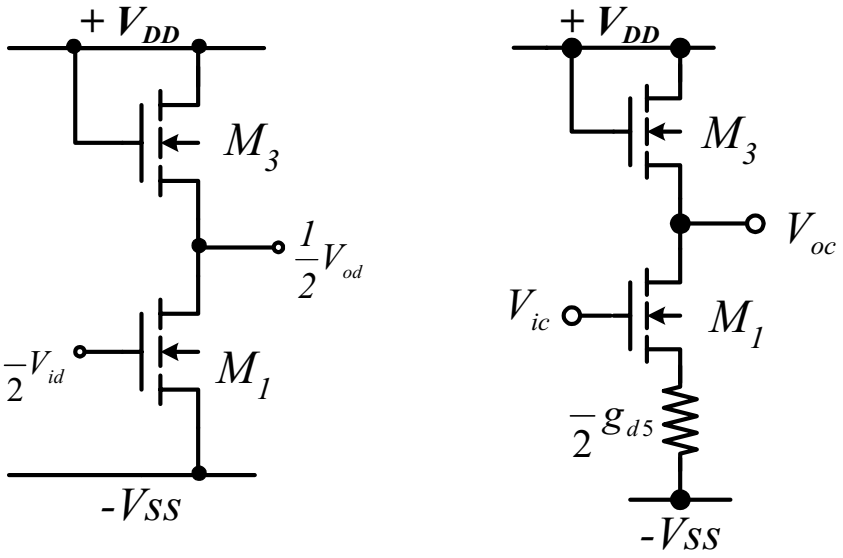
$$I_{DS} \propto exp(\frac{V_{GS}}{nv_t})$$

V_{OS} is smaller than that operated in the saturation region.

This case is similar to the BJT case. $\because V_{OS} \propto \Delta I_{DS}$)

(3) AC Gain

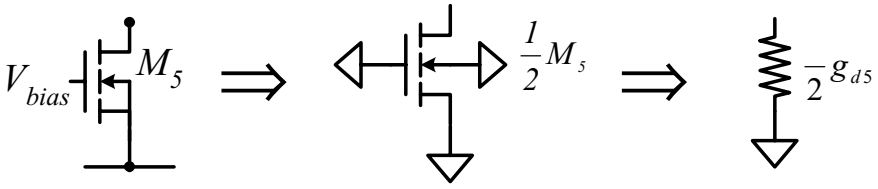
Differential signal *Common-mode signal*



Half-Circuit concept:

$$A_{dm} \equiv \frac{v_{od}}{v_{id}} = -\alpha_3 \frac{g_{m1}}{g_{m3}}$$

Common-mode half-circuit:



$$A_{cm} \equiv \frac{v_{oc}}{v_{ic}} = -\alpha_1\alpha_3 \frac{g_{d5}}{2g_{m3}}$$

$$CMRR \equiv \frac{A_{dm}}{A_{cm}} = \frac{2g_{m1}}{g_d\ \alpha_1}$$

* $L_5 \uparrow \Rightarrow g_{d5} \downarrow \Rightarrow CMRR \uparrow$

* When cascoded current source is used for Iss, $_{d5} \downarrow \Rightarrow CMRR \uparrow$

But $Vs \uparrow \Rightarrow$ common-mode range $\downarrow$

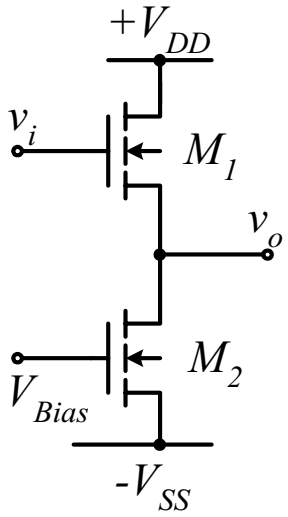
7. NMOS source follower

The voltage gain (midband) is

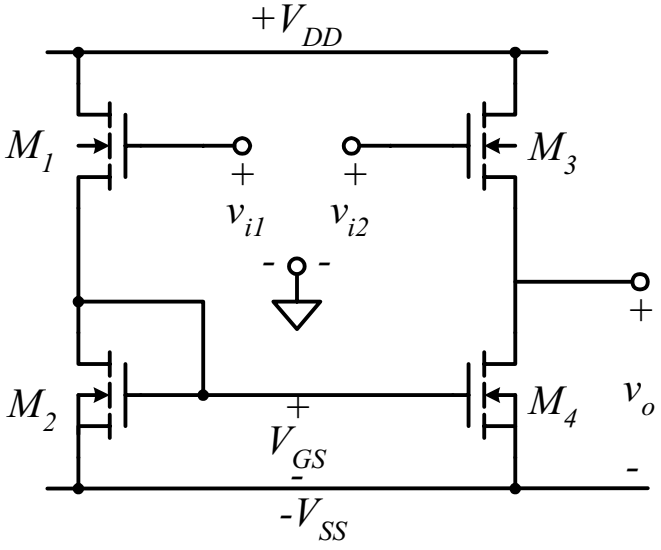
$$A_v = \frac{g_{m1}}{\frac{g_{m1}}{\alpha_1} + \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}}} < 1$$

If $r_{ds1}\ , r_{ds1} >> \frac{\alpha_1}{g_{m1}}$

$\Rightarrow A_v \cong \alpha_1 < 1$, smaller than that of the emitter follower.



8. NMOS differential-input to single-ended converter



$$A_v = \frac{N+1}{2} = \frac{\alpha_3}{1+\frac{\alpha_3}{g_{m3}}(\frac{1}{r_{ds3}}+\frac{1}{r_{ds4}})} (= \frac{v_o}{(v_{i1}-v_{i2})})$$

where $N = \dfrac{g_{m1}g_{m4}}{g_{m3}(\frac{g_{m1}}{\alpha_1}+g_{m2}+\frac{1}{r_{ds1}}+\frac{1}{r_{ds2}})}$

If $M_2 \equiv M_4$, $M_3 \equiv M_1$, $\dfrac{1}{r_{ds}} << g_m$

$\Rightarrow$ $g_{m2} = g_{m4}$, $g_{m3} = g_{m1}$

$$N \cong \frac{g_{m4}}{g_{m4}+g_{m3}/\alpha_3}$$

$$A_v \cong \alpha_3 \frac{2g_{m4}+g_{m3}/\alpha_3}{2g_{m4}+2g_{m3}/\alpha_3} < 1$$

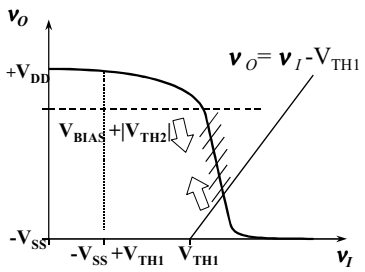
$$CMRR = \frac{1+N}{2(1-N)} = \frac{1}{2}+\frac{g_{m4}}{g_{m3}/\alpha_3}$$

To obtain a large CMRR , $g_{m4} >> g_{m3}/\alpha_3$

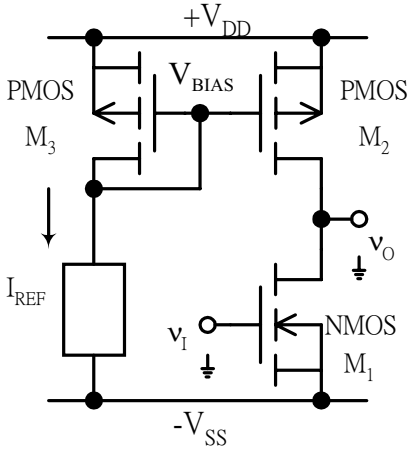
$$\Rightarrow A_v \cong \alpha_3 < 1$$

§ 4-1.2 CMOS Amplifier

1. Simple common-source amplifier



M_2 : PMOS current source



$$M_1 \text{ and } M_2 \text{ sat.} \Rightarrow V_{BIAS}+|V_{TH2}| > v_o > v_I - V_{TH1} \text{ or } V_{DD}-|V_{DSAT2}| \geq V_o \geq V_{DSAT1}-V_{SS}$$

$A_v = -g_{m1}(r_{ds1} // r_{ds2})$

$g_{m1} = \sqrt{2I_{DS1}\mu_n C_{ox}\left(\frac{W}{L}\right)_1}$, $r_{ds1} = \frac{1}{\lambda_1 I_{S1}}$ $r_2 = \frac{1}{\lambda_2 I_{S2}}$

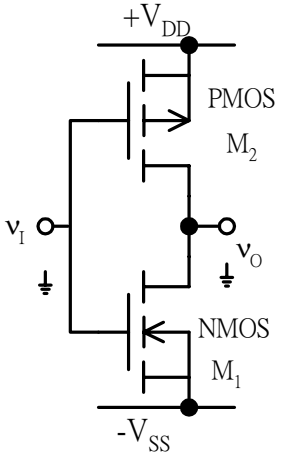
$\Rightarrow A = \frac{1}{\sqrt{I_{S1}}}\left(\frac{1}{\lambda_1 + \lambda_2}\right)\sqrt{2\mu C\left(\frac{W}{L}\right)_1}$

$|A_v| \propto \frac{1}{\sqrt{I_{DS1}}}$ (long-channel devices)

$|A_v| \propto (I_{DS1})^{-\frac{1}{m}}$ (short-channel devices)

Output resistance r_o $r_o = r_{ds1} // r_{ds2}$

2. Complementary CMOS common-source amplifier



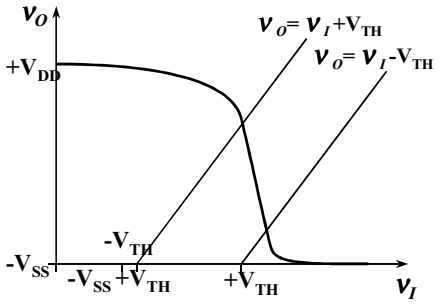
Assume $V_{TH1} = |V_{TH2}| = V_{TH}$

If $v_I - V_{TH} < v_o < v_I + V_{TH}$ or $V_{DD} - |V_{DSAT2}| \geq v_o \geq V_{DSAT1} - V_{SS}$

$\Rightarrow M_1$ and M_2 are saturated

$A_v = -(g_{m1} + g_{m2})(r_{ds1} // r_{ds2})$

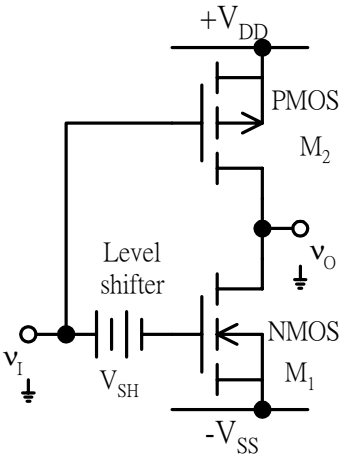
$r_o = r_{ds1} // r_{ds2}$



*Higher gain than the circuit in 1.

*Narrow operating range.

3. Complementary inverter with level shifter.



M_2 sat. $\Rightarrow V_{DD} - v_I - V_{TH} < V_{DD} - v_o$

M_1 sat. $\Rightarrow v_I - V_{SH} + V_{ss} - V_{TH} < v_o + V_{SS}$

$\Rightarrow v_I - V_{TH} - V_{SH} < v_o < v_I + V_{TH}$

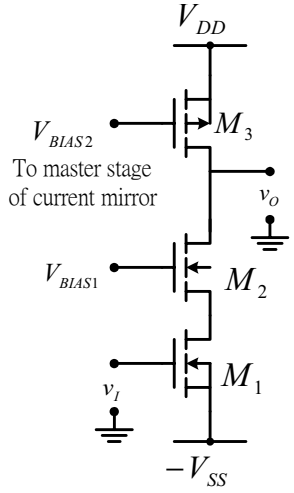
* $r_o = r_{ds1} // r_{ds2}$

* The range of v_o is increased by V_{SH}.

* In the short-channel case, $V_{GS1} \downarrow$ *by* V_{SH},

$V_{DSAT1} \downarrow \Rightarrow$ The range is also increased.

4. Cascode amplifier with PMOS current-source load



$$A_v = -g_{m1}[r_{ds3} \| (\frac{1}{\alpha_2} g_{m2} r_{ds1} r_{ds2})]$$

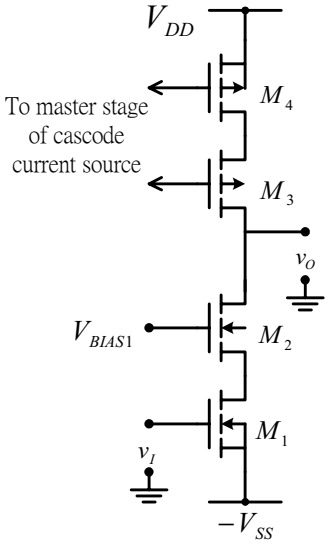
$$\cong -g_{m1} r_{ds3}$$

$$r_o = r_{ds3} \| (\frac{1}{\alpha_2} g_{m2} r_{ds1} r_{ds2})$$

$$\cong r_{ds3}$$

* PMOS devices can be used as cascode amplifier whereas NMOS device as current source.

5. Cascode amplifier with PMOS cascode current-source load



$$A_v = -g_{m1}[(\frac{1}{\alpha_3} g_{m3} r_{ds4} r_{ds3}) \| (\frac{1}{\alpha_2} g_{m2} r_{ds1} r_{ds2})]$$

$$\cong -\frac{1}{2\alpha} g_{m1} g_m r_{ds}^2$$

if $\alpha_3 = \alpha_2 = \alpha$

$g_{m3} = g_{m2} = g_m$

$r_{ds4} = r_{ds3} = r_{ds2} = r_{ds1} = r_{ds}$

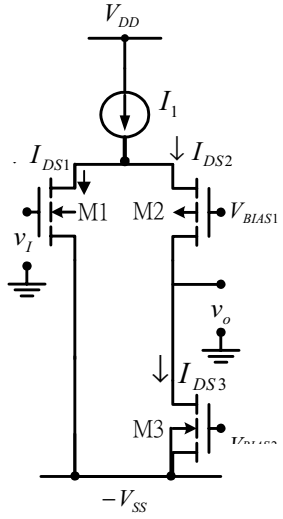
$$r_o \cong \frac{1}{2\alpha} g_m r_{ds}^2$$

* Larger r_o and A_v

* Limited output voltage swing

➔High-swing cascode current source is preferred

6. Folded cascode amplifier



M1: CS amplifier

M2: CG amplifier

Optimal operating point:

$$I_{DS1} = I_{DS2} = \frac{I_1}{2} = I_{DS3}$$

$g_{m1} = g_{m2}$

(to avoid large Miller capacitance at input)

$$A_v = -g_{m1}\{r_{ds3} \| [g_{m2}(r_{ds1} \| r_{dsI1}) r_{ds2}]\}$$

$$\cong -g_{m1} r_{ds3}$$

$r_o = r_{ds3} \| [g_{m2}(r_{ds1} \| r_{dsI1})r_{ds2}]$

* Nearly the same A_v and r_o can be achieved as the cascode amplifier
* Less devices in cascode at the input CS amplifier

➔M1 can be easily operated in the saturation region

7. Improved cascode amplifier with current injection circuitry

conventional cascode amplifier

$$A_v \cong -g_{m1}r_{ds3} \propto \frac{1}{\sqrt{I_{DS}}}$$

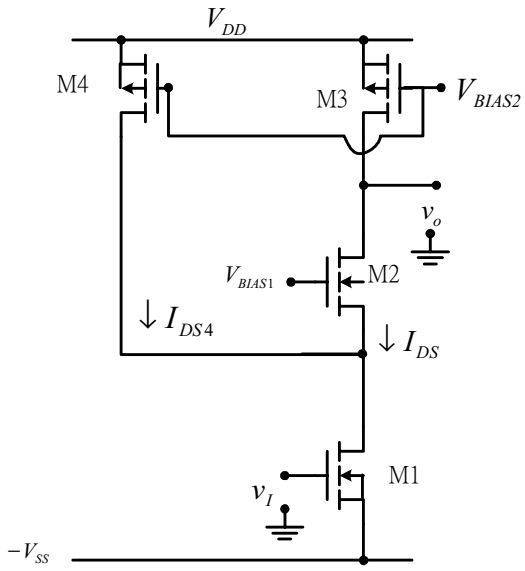
$I_{DS} \downarrow \Rightarrow A_v \uparrow$ until subthreshold

M3: current source as load

M4: current-injection current source

$$A_v \cong -g_{m1}r_{ds3} \propto \frac{\sqrt{I_{DS4}}}{\sqrt{I_{DS}}}$$

To increase A_v ➔ $I_{DS4} \uparrow$ and $I_{DS} \downarrow$



* Higher voltage gain and the same r_o
* Extra device M4 and extra power dissipation
* Firstly, design the circuit of M1, M2, and M3. Then add M4. Readjust the channel dimensions to keep the dc bias so that all devices are in saturation.

8. Differential amplifier with PMOS load

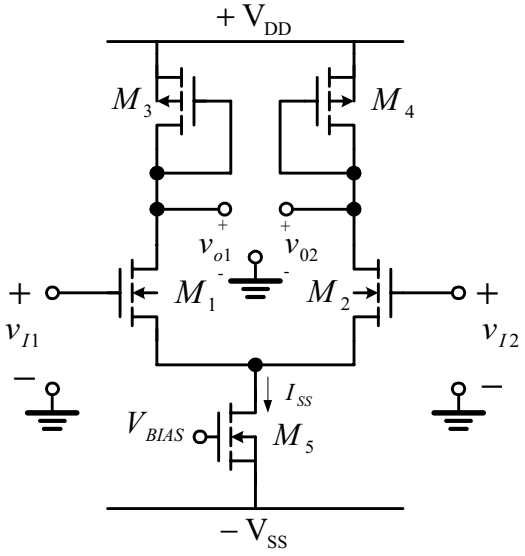
Half-circuit method can be used

$$v_{id} \equiv v_{I1} - v_{I2}\ ,\quad v_{ic} \equiv \frac{v_{I1} + v_{I2}}{2}$$

$$v_{od} \equiv v_{O1} - v_{O2}\ ,\quad v_{oc} \equiv \frac{v_{O1} + v_{O2}}{2}$$

$$A_{dm} \equiv \frac{v_{od}}{v_{id}} \cong -g_{m1}\frac{1}{g_{m3}}$$

$$A_{cm} \equiv \frac{v_{oc}}{v_{ic}} \cong -\alpha_1 \frac{g_{d5}}{2g_{m3}}$$



$$CMRR \equiv \left|\frac{A_{dm}}{A_{cm}}\right| \cong \frac{2g_{m1}}{g_{d5}\cdot\alpha_1}$$

$$r_{od} \cong \frac{1}{gm3}$$

$$r_{oc} \cong \frac{1}{gm3}$$

*Matched devices for M_1/M_2 and M_3/M_4

* $A_{cm} < 1$ can be achieved

9. Different amplifier with PMOS current-source load

M_3, M_4 :Two slave stages of the current mirror

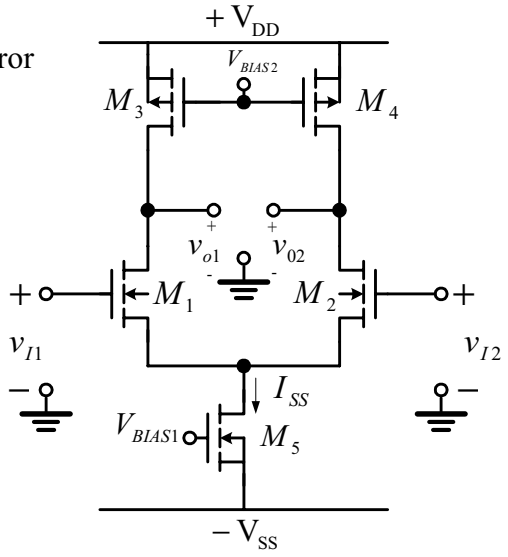
=> current-source load

$$A_{dm} \cong -g_{m1}\left(r_{ds1} \parallel r_{ds3}\right)$$

$$A_{cm} \cong -\frac{\alpha_1}{2r_{ds5}}\left(r_{ds3} \parallel g_{m1}r_{ds5}r_{ds1}\right)$$

$$CMRR \cong -\frac{2g_{m1}\left(r_{ds1} \parallel r_{ds3}\right)r_{ds5}}{\alpha_1 r_{ds3}}$$

* $g_{m1} \uparrow$, $r_{ds5} \uparrow$ => CMRR $\uparrow$



* $A_{cm} < 1$ is preferred => $r_{ds5} > r_{ds3}$

* I_{SS} can be realized by cascode or high-swing cascode current source to increase

$$r_{ds5}\left(=\frac{1}{g_{d5}}\right)$$

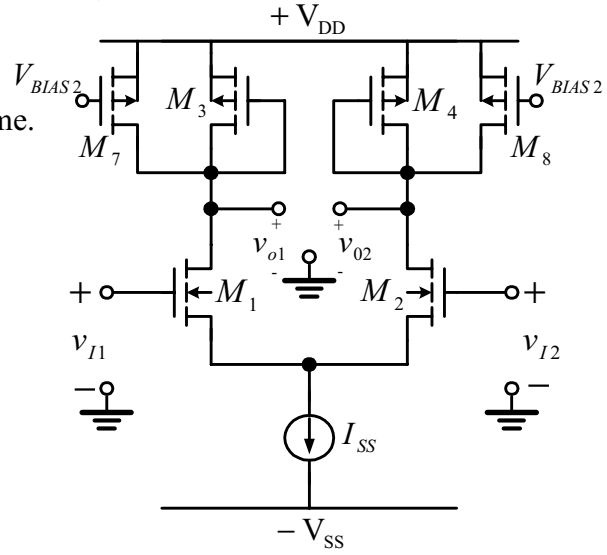
10. Differential amplifier with PMOS current injection circuit

If I_{SS} remains unchanged, gm1=gm2 the same.

But gm3=gm4 is reduced by $\frac{1}{\sqrt{2}}$ if

$I_{DS3} = I_{DS4}$ is reduced by half.

$\Rightarrow A_{dm} \uparrow$ by $\sqrt{2}$



$r_{ds7} = r_{ds8} >> \frac{1}{gm3} = \frac{1}{gm4}$

CMRR is the same.

* If M_3 and M_4 are current-source loads , could A_{dm} be increased? Why?

11. Differnetial cascode amplifier

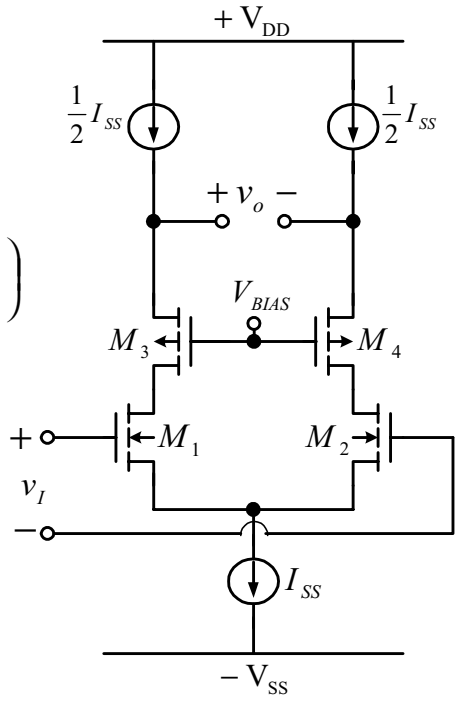
$v_O \equiv v_{O1} - v_{O2}$

$v_I \equiv v_{I1} - v_{I2}$

*Higher A_{dm}

*4 MOS devices stacked $\left(M_1, M_3, I_{SS}, \frac{1}{2} I_{SS}\right)$

$\Rightarrow V_{DD} + V_{SS}$ might not be enough to maintain all the devices in saturation when low supply voltage is used.



12. Differential Folded cascode amplifier

*To retain the characteristics of cascode amplifier, the optimal design is

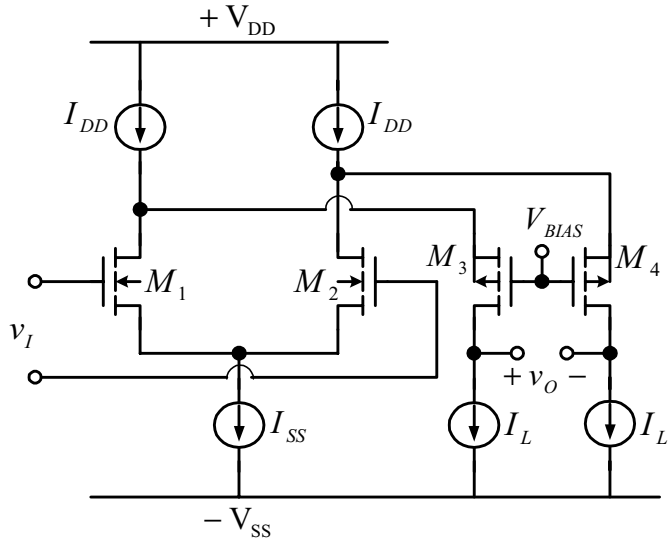
$I_{DD} = I_{SS}$

$I_L = \frac{1}{2} I_{SS}$

* Only 3 MOS devices stacked

=>low voltage operation is possible

* $V_{ICM} \uparrow$ why?



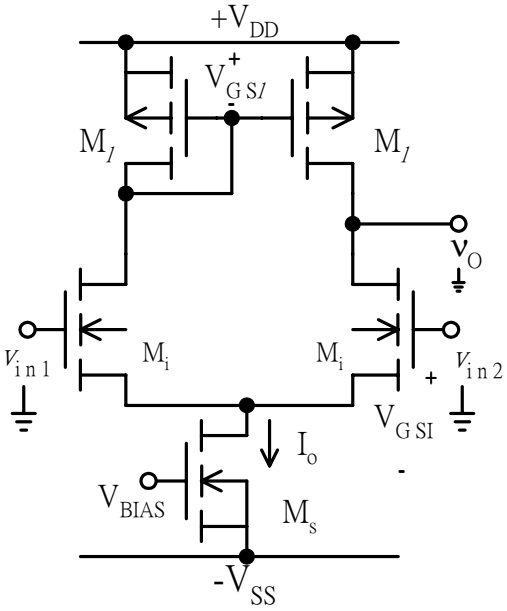
13. CMOS differential-input to single-ended-output converter.

Version I : NMOS input

DC operating point :

It is better to keep $V_{ODC} \cong V_{DD} - V_{GSI}$

for better current-mirror balance.



Common-mode range :

$$V_{ICM}+ = V_{DD} + V_{THN} - V_{GSI}$$

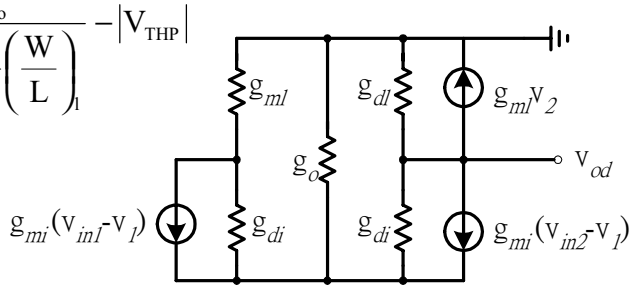
$$= V_{DD} + V_{THN} - \sqrt{\frac{I_o/2}{\frac{\mu_p C_{oxp}}{2}\left(\frac{W}{L}\right)_l}} - |V_{THP}|$$

$$V_{ICM}- = V_{GSI} + V_{BIAS} - V_{THN}$$

$$= \sqrt{\frac{I_o/2}{\frac{\mu_p C_{oxn}}{2}\left(\frac{W}{L}\right)_i}} + V_{BIAS}$$

Differential-mode range :

$$V_{Id}^{+} = -V_{Id}^{-} = V_{DD} + V_{THN} - \sqrt{\frac{I_o}{\frac{\mu_p C_{oxp}}{2}\left(\frac{W}{L}\right)_l}} - |V_{THP}|$$



$$v_{in1} = \frac{v_{id}}{2} + v_{ic}$$

$$v_{in2} = \frac{-v_{id}}{2} + v_{ic}$$

$\Rightarrow$ Exact A_{cm} and A_{dm} can be solved.

$$A_{dm} \approx \frac{g_{mi}}{g_{dl} + g_{di}} \qquad A_{cm} \approx -\frac{g_o g_{di}}{2g_{ml}(g_{dl} + g_{di})}$$

$$\text{CMRR} \equiv \left|\frac{A_{dm}}{A_{cm}}\right| \approx 2\frac{g_{mi} g_{ml}}{g_o g_{di}} \qquad \text{output resistance } r_o \approx \frac{1}{g_{dl} + g_{di}}$$

* Longer channel in Ms leads to smaller g_o and higher CMRR.

* $A_{dm} \propto \frac{1}{\sqrt{I_o}}$ or $(I_o)^{-1/m}$ => higher bias current, lower gain.

* In the weak inversion region, $g_{mi} \propto$ Io => $A_{dm} \approx$ constant.

* Cascode current source can be used for Io to increase CMRR,but Vicm $\downarrow$

* This circuit is not a pure symmetric differential circuit. But it can be approximated by a differential circuit and half -circuit analysis method can be used.

* Signal paths:

v_{in1} :

$v_{in1} \rightarrow v_{gsl}$: $A_v' = -g_{mi}\dfrac{1}{g_{ml}}$

$v_{gsl} \rightarrow v_o$: $A_v'' = -g_{ml}(r_{dsl} // r_{dsi})$

⇨ $A_v\big|_{v_1} = A_v' A_v'' = g_{mi}(r_{dsl} // r_{dsi}) = A_{dm}$

How about $v_{in1} \rightarrow v_1 \rightarrow v_o$?

v_{in2} :

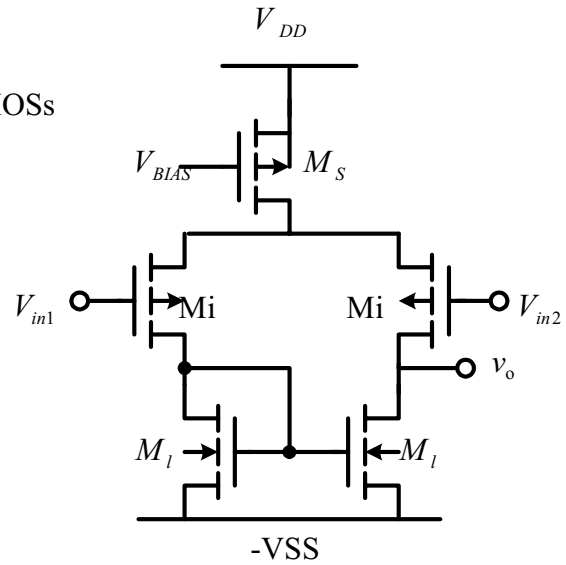
$v_{in2} \rightarrow v_o$: $A_v\big|_{vin2} = -g_{mi}(r_{dsl} // r_{dsi}) = |A_{dm}|$

How about $v_{in2} \rightarrow v_1 \rightarrow v_{gsl} \rightarrow v_o$?

The voltage gain of the four signal paths have nearly the same amplitudes. But different signal paths affect the high frequency response.

Version II: PMOS input

* Lower noise(1/f noise) due to input PMOSs
* Lower output dc voltage



14. The available amplifier circuits in CMOS trechnology

1). NMOS amplifier in 4-1.1
2). PMOS amplifier with the same configurations as in 4-1.1
3). CMOS amplifiers (NMOS version) in 4-1.2
4). PMOS version with the same configurations as in 4-1.2

Comparisons:

1) NMOS(PMOS) amplifiers versus CMOS amplifiers

	single-type MOS amplifier	CMOS amplifier
Voltage gain	Low	High
Output resistance	Low	High
Immunity to process variations	High	Low
Power dissipation	High	Low

2) NMOS amplifier (CMOS amplifier with NMOS version) versus PMOS amplifier (CMOS amplifier with PMOS version)

1.Better frequency response

2.Smaller chip area

3) Differential amplifier versus single-ended-output amplifier

1.Excellent common-mode signal rejection capability

Common-mode signals: external noise, dc voltage due to variations, power-supply noise, substrate noise.

2.Good for weak signal amplification in noisy environment.

3.Wide applications especially in high-frequency ICs.

4.More component used ➔ Higher power dissipation and larger chip area.

5.Matched devices are required ➔ Special care is need in layout and process.

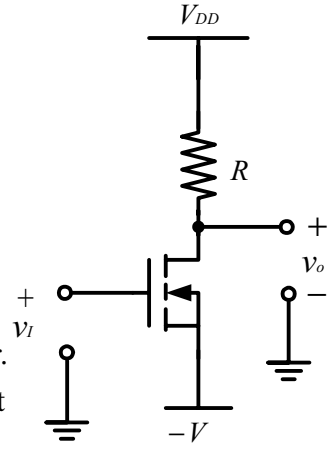
6.I/O testing requires special I/O external circuits or equipment.

§4.2 Passive-Load MOS Amplifiers

§4-2.1 Resistive-load MOS amplifiers

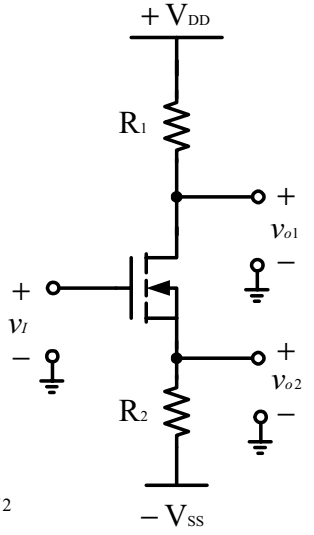
1. Resistive-Load MOS amplifier

$Av = -g_{m1}R$, $r_o \approx R$



* Low voltage gain and low r_o
* If R ↑, M1 might be in the linear region.
* Only used for low-gain high-frequency amplifier.
  ∵ Parasitic capacitance of R is smaller than that of the current-source active load.
* Process variations of R might be ±20%.

2. Resistive-load MOS phase splitter



$$A_{V1} \equiv \frac{V_{O1}}{V_i} \cong -\alpha_1 \frac{R_1}{R_2}$$

$$A_{V2} \equiv \frac{V_{O2}}{V_i} \cong \frac{\alpha_1 g_{m1} R_2}{g_{m1} R_2 + \alpha_1}$$

$$r_{o1} \cong R_1$$

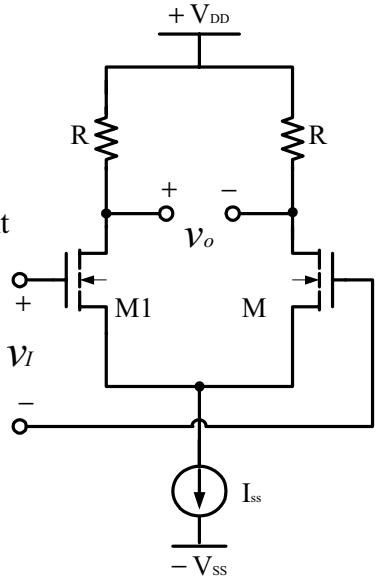
$$r_{o2} \cong R_2 \left\| \frac{1}{g_m} \right.$$

* R1 and R2 can be chosen so that $A_{V1} = A_{V2}$

➔ Phase splitter

* Process variation effect of R1 and R2 on A_{V1} and A_{V2} is reduced.

3. Resistive-load differential amplifier



* Suitable for low-gain low-r_o high-frequency amplifiers.

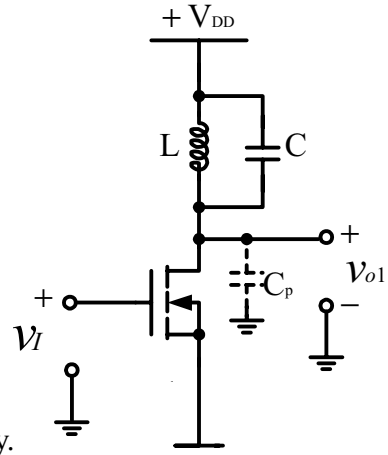
* I_{SS} can be generated by the constant-gm current source with R_{cogm}

➔ I_{SS} or $g_{m1}, g_{m2} \propto \frac{1}{R_{cogm}}$

➔ $A_{dm} = -g_{m1} R \propto \frac{R}{R_{cogm}}$

➔ Process variation of R and temperature coefficient of R can be compensated.

§ 4-2.2 Inductive load MOS amplifier



1. LC-tank MOS amplifier

* If L is implemented by on-chip inductor, only ~GHz RF operation is allowed.

* L combined with the parasitic capacitance Cp and the capacitor C to form a LC tank.

➔ Narrow-band amplifier or tuned amplifier.

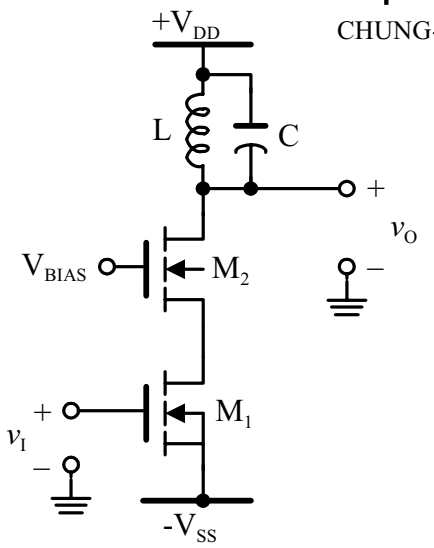
➔Bandpass amplifier with frequency selectivity.

2. LC-tank MOS cascode amplifier

*The output LC-tank impedance has a much smaller effect on the input impedance at high frequency due to the isolation effect of M2.

* $V_{ODC} = V_{DD}$

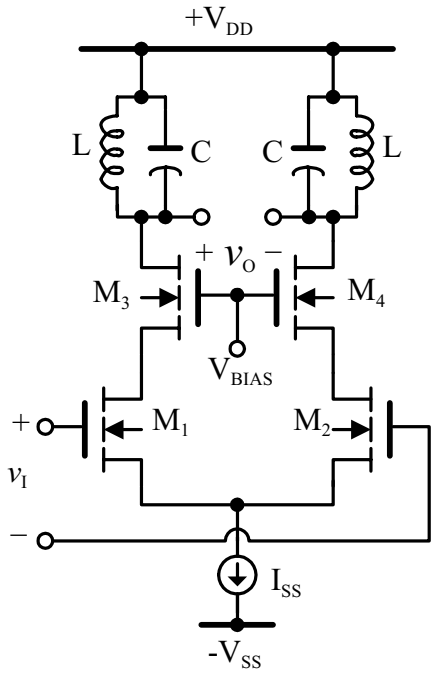
$v_O > V_{DD}$



3. MOS differential cascodee amplifier with series LC-tank

* $V_{O1DC} = V_{O2DC} = V_{DD}$

*Two LC-tanks are required.



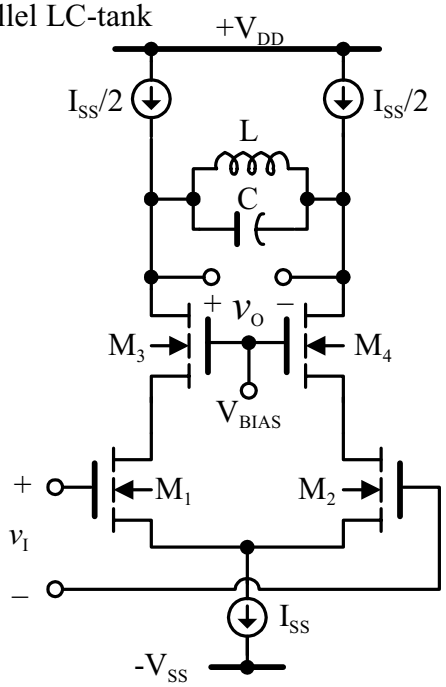
4. MOS differential cascode amplifier with parallel LC-tank

* Only one LC-tank is used

=>chip area↓

* $V_{O1DC} = V_{O2DC} < V_{DD}$

*Bandpass amplifier with the maximum differential gain the same as that of the cascode amplifier.

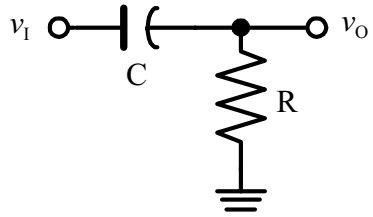


§ 4-3 Level shifting circuits

Purpose: to provide a dc voltage difference between input and output signals so that the dc level of the output signal is acceptable for the next amplifier stage.

∵ At low frequency operation below several tens MHz, dc blocking capacitors are not effective in blocking the dc voltage and passing the ac signal.

DC blocking capacitor:



ac gain: $\left|\frac{Vo}{Vi}\right| = \left|\frac{R}{R - j\frac{1}{wc}}\right| = \frac{R}{\sqrt{R^2 + \left(\frac{1}{wc}\right)^2}} \cong \frac{1}{1 + \frac{1}{2}\frac{\left(\frac{1}{wc}\right)}{R^2}}$

At 10MHz, $w \cong 6.3\times10^7$ rad/sec

CASE1: If C=10PF, $\frac{1}{wc} = \frac{1}{6.3}\times10^4\,\Omega \cong 1.6k\Omega$

To obtain 1% signal attenuation, we have

$$\left|\frac{v_o}{v_i}\right| = 0.99 \quad => \frac{1}{2}\frac{\left(\frac{1}{wc}\right)^2}{R^2} \cong 0.1$$

$$=>R=\left(\frac{1}{wc}\right)\frac{1}{\sqrt{0.02}} \cong 11.2k\Omega$$

The values of R and C are too large and area-consuming.

CASE 2: At 1GHz, $w=6.3\times10^9$ rad/sec

If C=1PF, $\frac{1}{wc} = \frac{100}{6.3} \cong 160\Omega$

The required R for 1% attenuation is

$$R=7(\frac{1}{wc})=1.12k\Omega$$

The values of R and C are reasonable.

1. Simple level shifting circuit

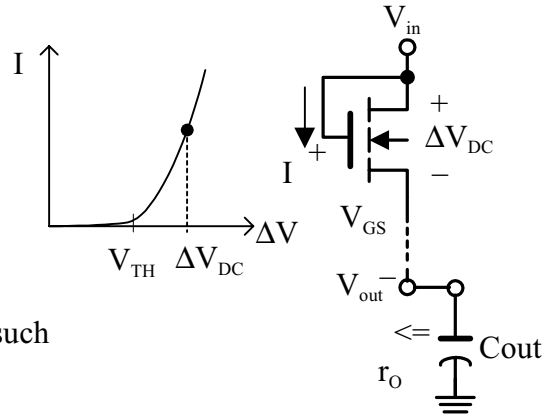
$\triangle V_{DC}=V_{GS}$

* W/L $<<1$ to obtain a large $\triangle V_{DC}$
* Output resistance looking into Vout is very large

$r_O \cong \frac{1}{g_m}$ $\because W/L<<1,\ g_m \downarrow \Rightarrow r_O \uparrow$

* Frequency response could be degraded by such a large r_O.

$\because$ r_OCout $\uparrow$



2. High-Z level shifting circuit

$\triangle V_{DC}(NMOS)=+V_{GS}$

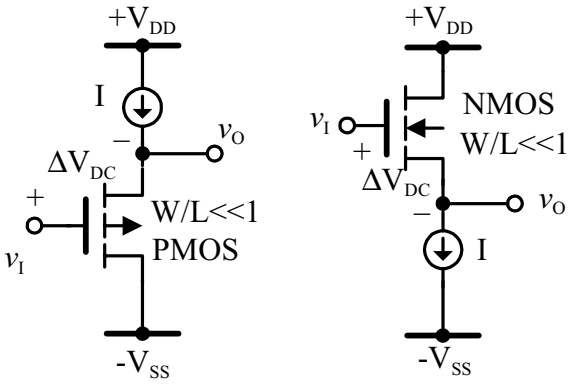
$\triangle V_{DC}(PMOS)=-V_{GS}$

* $r_O \cong \frac{1}{g_m}$

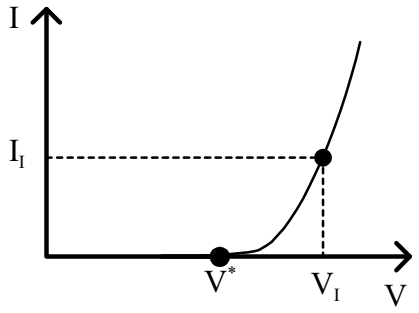
$\because W/L<<1$

$\Rightarrow r_O \uparrow (\triangle V_{DC} \uparrow)$

Frequency response could be degraded.

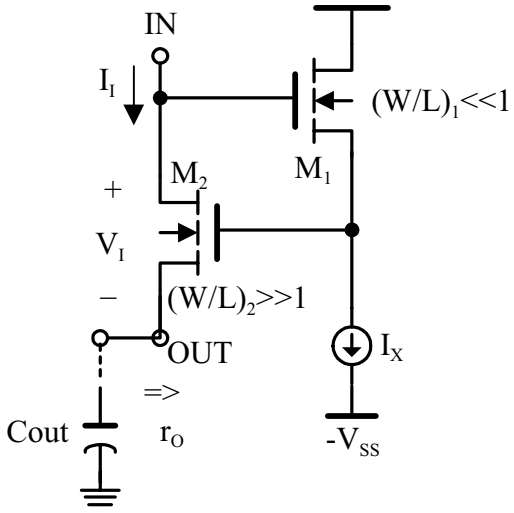


3. Low-Z level shifting circuit



$V^*=V_{TH2}+V_{GS1}$

$=V_{TH2}+V_{TH1}+\sqrt{\frac{Ix}{\left(\frac{\mu C_{ox}}{2}\right)_1 (W/L)_1}}$



$$V_I = V^* + \sqrt{\frac{I_I}{\left(\frac{\mu C_{ox}}{2}\right)_2 (W/L)_2}}$$

$\because (W/L)_1 << 1$ and $(W/L)_2 >> 1$ =>large enough V^*

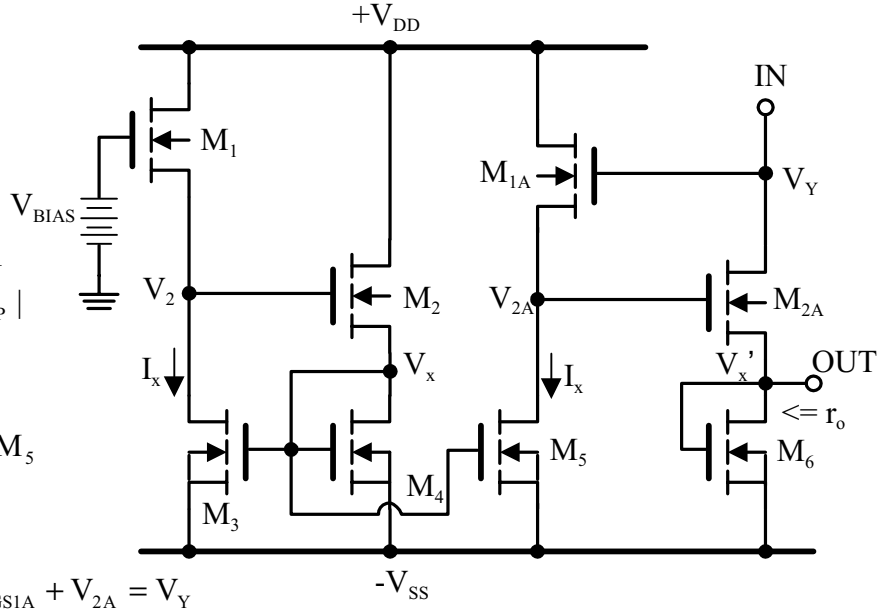
$V_I \cong V^*$ independent of I_I

* V_I (dc voltage shift) can be stabilized by choosing a large $(W/L)_2$ and a stable I_x.

* $r_0 \cong \frac{1}{g_{m2}}$ is not large since $(W/L)_2 >> 1$.

=> Better frequency response.

4. Replica bias circuit



$(W/L)_6, (W/L)_4 >> 1$

$\Rightarrow V_{GS4} \cong V_{GS6} \cong V_{THN}$

$\Rightarrow V_X \cong V_X'$

$(W/L)_2, (W/L)_{2A} >> 1$

$\Rightarrow V_{GS2} \cong V_{GS2A} \cong |V_{THP}|$

$\Rightarrow V_2 \cong V_{2A}$

$M_1 \cong M_{1A}$ and $M_3 \cong M_5$

$I_{DS3} = I_{DS5} = I_X$

$V_{GS1} = V_{GS1A}$

$V_{BIAS} = V_{GS1} + V_2 = V_{GS1A} + V_{2A} = V_Y$

* Provide a fixed bias voltage $V_Y = V_{BIAS}$ at the input node to stablize the preceding stage.

* Provide a DC voltage shift of $V_Y - V_X'$

* The output resistance looking into the OUT node is very small

$(r_o \cong \frac{1}{g_{m2A}} \| \frac{1}{g_{m6}}, (W/L)_{2A}, (W/L)_6 >> 1 \Rightarrow r_o \downarrow)$

* The matching between $M_1(M_3)$ and $M_{1A}(M_5)$ is very important to stablize V_Y.

§ 4-4 MOS Output stages

§ 4-4.1 Requirements

(1) Suitable power and voltage swing to drive an adequate external load equally in both positive and negative directions.

(2) Acceptably low levels of signal distortion.

(3) Minimum output impedance.

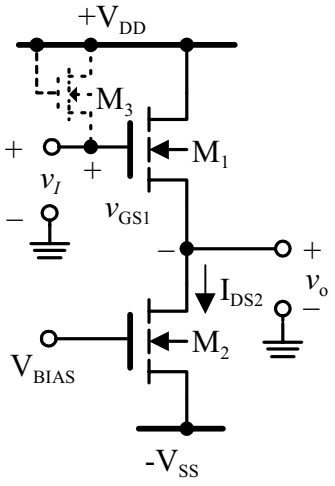
(4) Low quiescent power dissipation and maximum efficiency.

(5) High frequency response.

(6) Buffering the previous gain stage from C_L or R_L

§ 4-4.2 NMOS (PMOS) Output Stages

1.Source followers (Enhancement device)



* Voltage swing:

$$v^{+}_{o\max} = v_I - v_{GS1}$$

$$= V_{DD} - V_{TH3} - v_{GS1} \text{ (or } V_{TH1}\text{)}$$

(not full level to V_{DD})

$$v^{-}_{o\max} = V_{BIAS} - V_{TH2} \text{ (M_2 sat)}$$

$$= -V_{SS} \text{ (M_1 off)}$$

* $r_0 \cong \dfrac{1}{g_{m1}}$

Small r_0 Need large $(W/L)_1$ and I_{DS1}

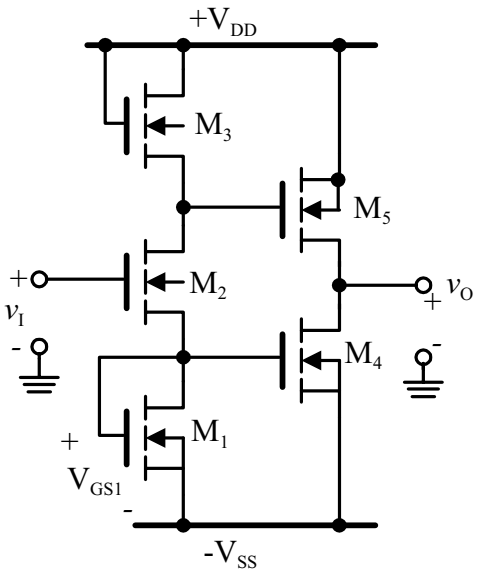
* The rise time is decreased by the larger $(W/L)_1$

But the fall time is fixed by I_{DS2}

=>Unsymmetric driving capability.

* Provide a dc voltage shift and a voltage gain smaller than 1

2. Phase-splitting output driver



* voltage swing: (low)

$$v_{o\max}{}^{+} = V_{DD} - V_{TH3} - V_{TH5}$$

(M2 and M4 are off)

$$v_{o\max}{}^{-} = -V_{SS} - V_{GS1} + V_{TH4} \text{ (M4 sat.)}$$

$$= -V_{ss} + V_{DS4} > -V_{SS}$$

(maximum)

* Fall time is not limited by the current source.

* $r_o \approx \left(1/g_{m5}\right) \| \left(r_{ds4}\right) \approx 1/g_{m5}$

3. NMOS output stage with feedback

M3, M4 : output common-source amplifier.

M1, M2 : First common-source amplifier

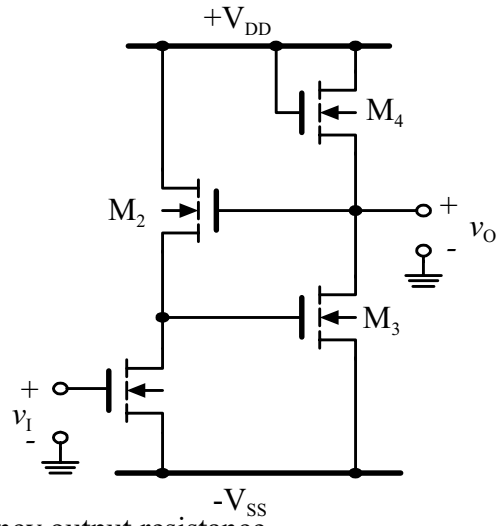
M2 : series-shunt negative feedback

Series-shunt negative feedback

=> voltage gain ↓

frequency bandwidth ↑

output resistance ↓



$$r_o = \frac{\alpha_4 / g_{m4}}{1 + \left(\alpha_2 \alpha_4 g_{m3} / g_{m4} \right)}$$ midfrequency output resistance

$$A_v = \frac{g_{m1}}{g_{m2}} \frac{\alpha_2 \alpha_4 g_{m3} / g_{m4}}{1 + \left(\alpha_2 \alpha_4 g_{m3} / g_{m4} \right)}$$ midfrequency voltage gain

If $\alpha \to 1$ $$A_V \equiv \sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{\sqrt{(W/L)_3 / (W/L)_4}}{1 + \sqrt{(W/L)_3 / (W/L)_4}}$$

* Larger $g_{m3} / g_{m4} \Rightarrow r_0 \downarrow,\ A_o \uparrow$

* The W/L ratio of M1,M2,M3 and M4 can be suitably designed to satisfy the specifications on (1) voltage gain ; (2) output swing ; (3) power dissipation ; (4) chip area ; (5) fast transient ; (6) good frequency response.
((5) and (6) involve non-linear analysis)

§ 4-4.3 CMOS Output Stages

1.Simple source follower.(NMOS and PMOS)
Too larger r_o

2.Class AB puah-pull CMOS output buffer

*Capable of low standby power.

e.g. $I_{bias} \cong$ nA

$I_{out} \cong <$ 1mA

* $V_{ODC} = \frac{V_{DD} + V_{SS}}{2}$ is desired

*Small output voltage swing.

If R_L exists at the output node, the voltage swing is further degraded.

3.Emitter-follower output stage.

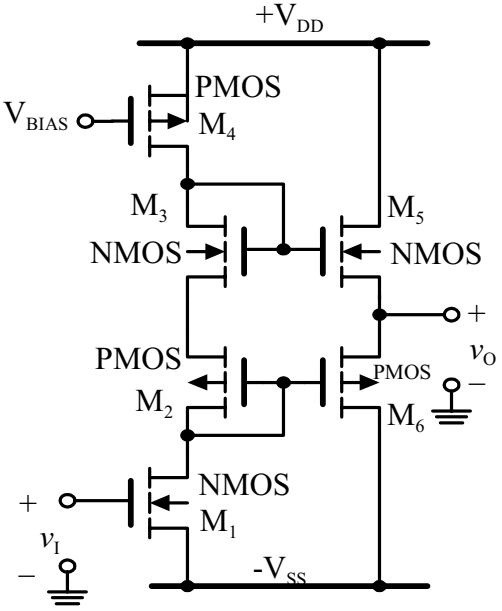
* $r_o \downarrow$

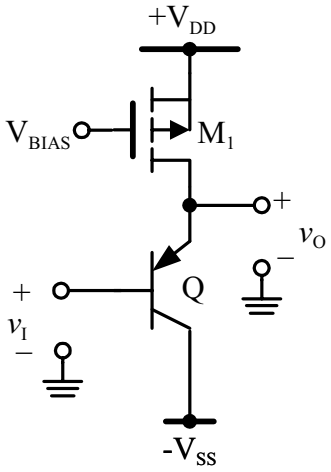
* Q_1 : free BJT in CMOS n-well technology.
Voltage swing:

$v_{O\max}^{-} = v_I + |V_{BE}|$

$= V_{SS} + |V_{BE}|$ (if $v_{I\max}^{-} = -V_{SS}$)

$v_{O\max}^{+} = +V_{DD}$ (If Q_1 is off)





* The collector series resistance r_C of Q_1 may degrade the output swing and saturate the transistor.