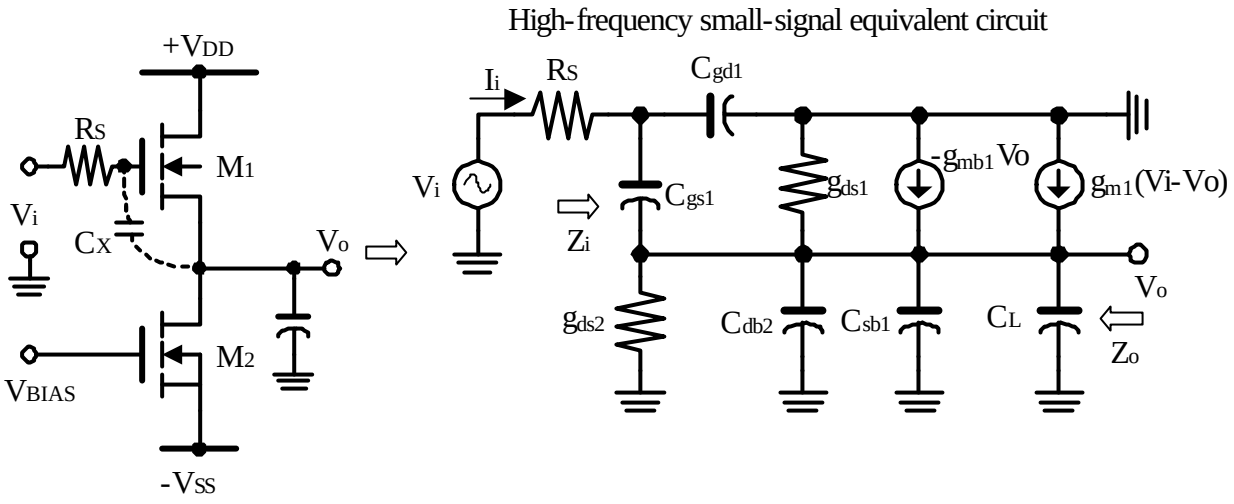
Chapter 6 Frequency Response of MOS Amplifiers

§6-1 Single-Stage Amplifier

§6-1.1 Source follower



$$A_V(s) \equiv \frac{Vo(s)}{Vi(s)} = \frac{sC_{gs1} + g_{m1}}{Rs(C_{gs1}C_{Leq} + C_{gs1}C_{gd1} + C_{gd1}C_{Leq})s^2 + (\frac{g_{m1}}{\alpha_1}RsC_{gd1} + C_{Leq} + C_{gs1})s + g_{m1}/\alpha_1 + G_{Leq}}$$

where $G_{Leq}=g_{ds1}+g_{ds2}$, $C_{Leq}=C_L+C_{sb1}+C_{db2}$

* Left-Half-Plane (LHP) pole: $fp = \frac{G_{Leq} + g_{m1}/\alpha_1}{2\pi(C_{gs1} + C_{Leq})}$

$$\text{LHP zero: } fz = \frac{g_{m1}}{2\pi C_{gs1}}$$

In general, $fp < fz$ $\because C_{Leq} > C_{gs1}$

* If $\frac{C_{Leq}}{C_{gs1}} = (\frac{1}{\alpha_1} - 1) + \frac{G_{Leq}}{g_{m1}}$, we have

fp = fz and $Av(s) \cong \frac{C_{gs1}}{C_{gs1} + C_{Leq}} \cong 1$ indep. of s.

=>Better high frequency response.

How to achieve this?

Adding an extra capacitor Cx such that

$$Cx+C_{gs1}=C_{Leq}\left[\frac{1}{(\frac{1}{\alpha_1}-1)+\frac{G_{Leq}}{g_{m1}}}\right]$$

$$Zi(s)\equiv\frac{Vi(s)}{Ii(s)}=\left[\frac{1}{C_{gs1}s}+\frac{C_{gs1}s+g_{m1}}{C_{gs1}s(G_{Leq}+g_{mb1}+sC_{Leq})}\right]\Big\|(C_{gd1}s)$$

* If $g_{mb1}+G_{Leq}<< C_{Leq}S$ and C_{gd1} is neglected,

$$Zi(s)\cong\frac{1}{C_{gs1}S}+\frac{1}{C_{Leq}S}+\frac{g_{m1}}{C_{gs1}C_{Leq}S^2}$$

The input impedance consists of the series connected

C_{gs1}, C_{Leq}, and the negative resistance

$$-\frac{g_{m1}}{C_{gs1}C_{Leq}\omega^2}$$

Thus oscillation is possible.

* If $g_{mb1}+G_{Leq}$ is neglected, the equivalent input capacitances

$$Cin=Cgd1\Big\|Cin'$$

$$Cin'\cong C_{Leq}\left(\frac{1}{\frac{C_{Leq}}{C_{gs1}}+1+\frac{g_{m1}}{C_{gs1}s}}\right)$$

For large g_{m1}, $C_{in}'<<C_{Leq}$

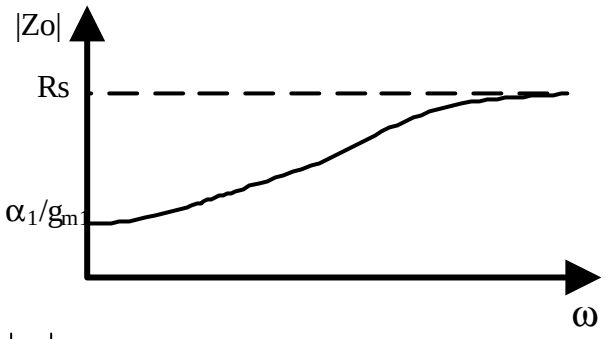
The large load capacitance C_L is well blocked or buffered from the preceding stage.

$$Zo(s)\equiv\frac{Vo(s)}{Io(s)}\Big|_{Vi=0}=\frac{1}{G_{Leq}+g_{mb1}+sC_{Leq}+(sC_{gs1}+g_{m1})\frac{R_sC_{gd1}s+1}{R_s(C_{gd1}s+C_{gs1}s)+1}}$$

* If s = 0, $Zo = Ro = \frac{1}{g_{m1}+g_{mb1}}$

If $s\rightarrow\infty$, Zo'(without C_{Leq})$\cong$ Rs for $Rs<\frac{1}{G_{Leq}+g_{m1}}$ and $C_{gs1}>>C_{gd1}$

Since usually $Rs>\frac{1}{g_{m1}+g_{mb1}}$, we have



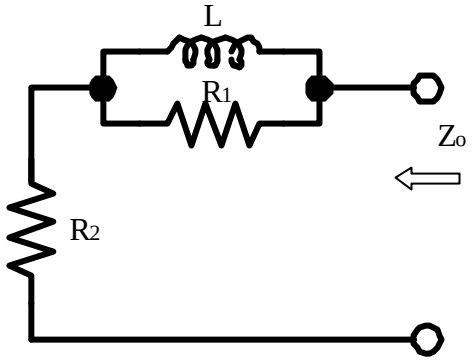
=> |Zo| α ω => Inductive load

$$Zo(s) \cong \frac{R_s C_{gs1} s + 1}{g_{m1}/\alpha_1 + C_{gs1} s}$$

$$R_1 = R_s - \frac{\alpha_1}{g_{m1}}$$

$$R_2 = \frac{\alpha_1}{g_{m1}}$$

$$L = \frac{C_{gs1}\alpha_1}{g_{m1}}\left(R_s - \frac{\alpha_1}{g_{m1}}\right)$$



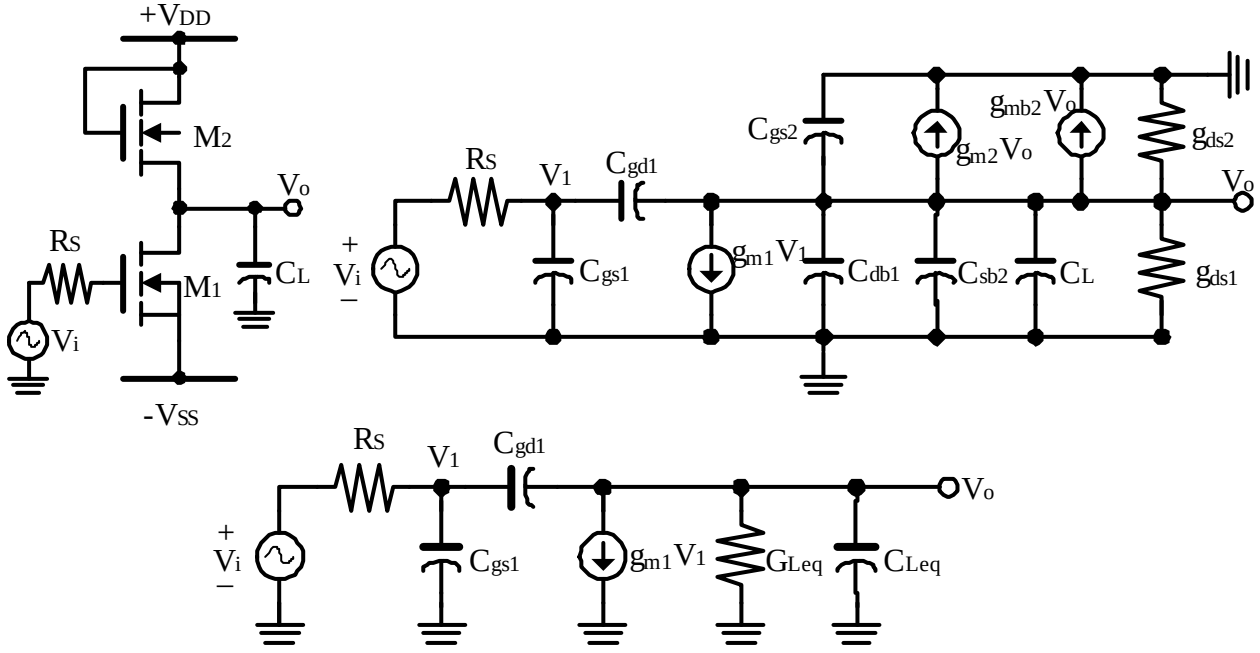
L and C_L causes output signal ringing.

* Two source followers in cascade might cause oscillation because

First SF ： L in Zo 1

Second SF ：-R and Cin Z_{i2}

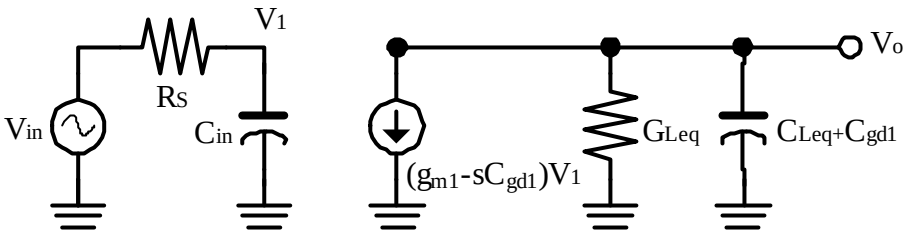
§6-1.2 Enhancement－load NMOS common-source gain stage



$G_{Leq}=g_{ds1}+g_{ds2}+g_{m2}+g_{mb2}$

$C_{Leq}=C_{db1}+C_{gs2}+C_{sb2}+C_L$

Applying the Miller's theorem, we have



$C_{in}=C_{gs1}+C_{gd1}(1+g_{m1}/G_{Leq})$

$$=>Av(s)\cong\frac{G_s(sC_{gd1}-g_{m1})}{(sC_{in}+G_s)\left[s(C_{Leq}+C_{gd1})+C_{Leq}\right]}$$

* Right-Half-Plane Zero：$Sz = g_{m1}/C_{gd1}$
* Left-Half-Plane Poles ：$S_{p1}=-G_s/C_{in}$ (input pole)

$S_{p2}=-G_{Leq}/(C_{Leq}+C_{gd1})$ (output pole).

If C_{gd1} and C_{Leq} are small $=>S_{p1}$ is the dominant pole.

* If C_L is large, the dominate pole is $S_{p2}\cong(g_{m2}+g_{mb2})/C_L$
* The input impedance can be approximated by

$$Zin\cong\frac{1}{\left[C_{gs1}+(1+g_{m1}\frac{1}{G_{Leq}})C_{gd1}\right]s}$$ near the upper 3dB frequency.

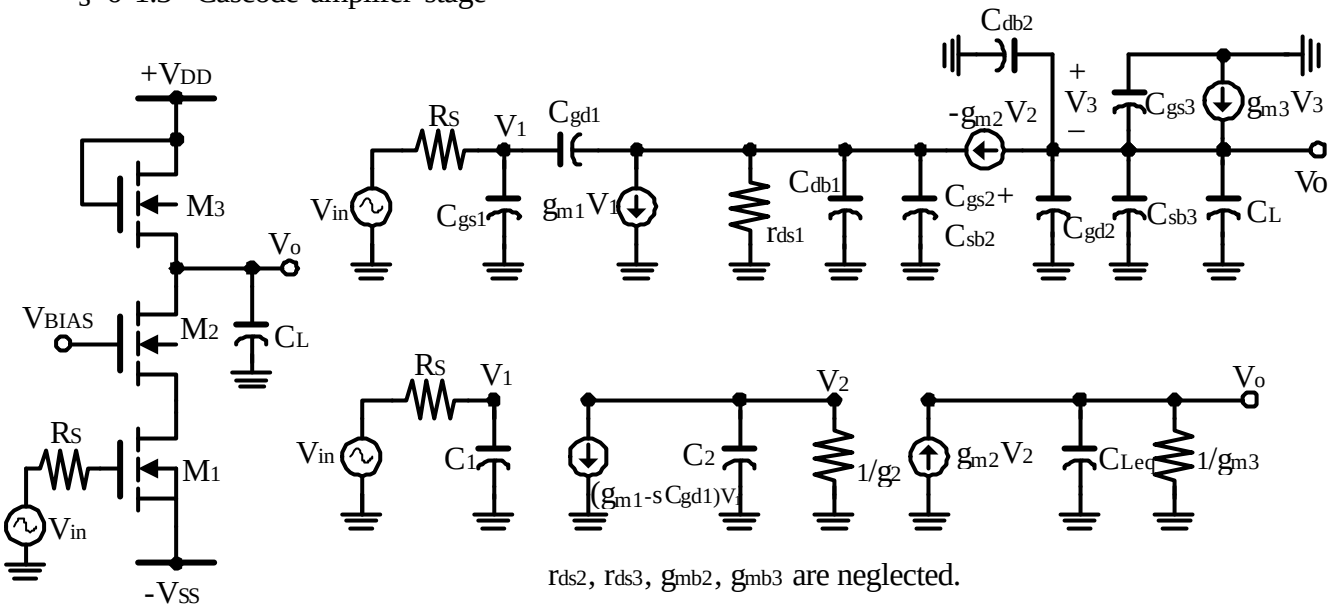
* The exact Zin is

$$Zin\cong C_{gs1}s\left\|\left[\frac{1+\frac{1}{G_{Leq}}(C_{gd1}+C_{Leq})s}{C_{gd1s}(1+g_m\frac{1}{G_{Leq}}+\frac{1}{G_{Leq}}C_{Leq}s)}\right]\right.$$

If $\left|\frac{1}{G_{Leq}}(C_{gd1}+C_{Leq})s\right|$ <<1 and $\left|\frac{1}{G_{Leq}}C_{gds1}s\right|<<(1+gm\frac{1}{G_{Leq}})$,

Zin can be approximated by the previous formula.

§ 6-1.3 Cascode amplifer stage



r_{ds2}, r_{ds3}, g_{mb2}, g_{mb3} are neglected.

$$g_2 = g_{m2} + \frac{1}{r_{ds1}}$$

$$C_2 = C_{gs1} + (1 + \frac{g_{m1}}{g_{m2}})C_{gd1}$$

$$C_2 = C_{gd1} + C_{db1} + C_{gs2} + C_{sb2}$$

$$C_{Leq} = C_L + C_{gd2} + C_{db2} + C_{sb3} + C_{gs3}$$

$$A_v(s) = \frac{-G_s g_{m2}(sC_{gd1} - g_{m1})}{(sC_1 + G_s)(sC_2 + g_2)(sC_{Leq} + g_{m3})}$$

RHP Zero: $S_z = \frac{g_{m1}}{C_{gd1}}$

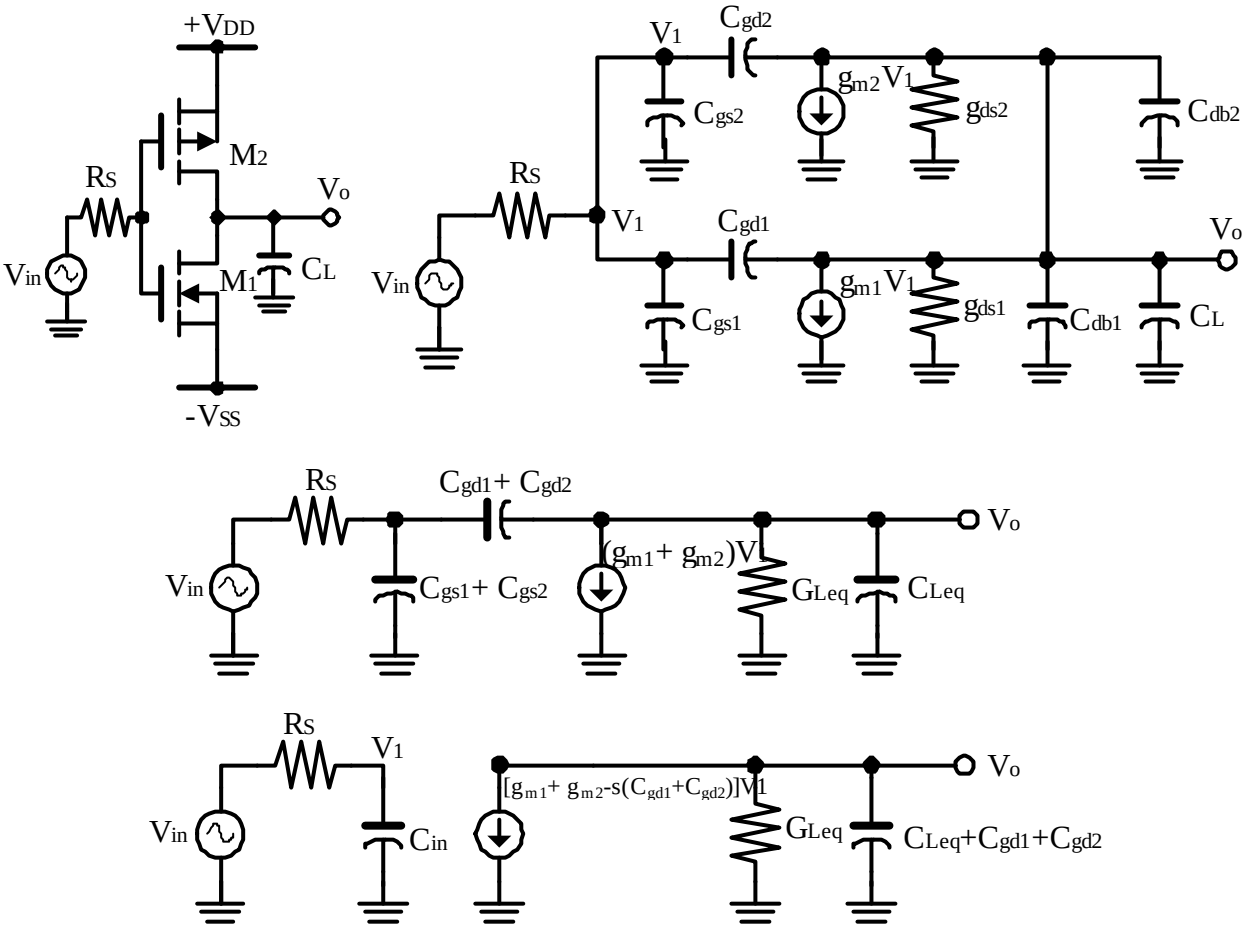
LHP Pole : $S_{p1} = -\frac{G_s}{C_1}$; $S_{p2} = -\frac{g_2}{C_2}$; $S_{p3} = \frac{-g_{m3}}{C_{Leq}}$

S_{p1} usually is the dominant pole.

$$\Rightarrow f_{3dB} \cong \frac{|S_{p1}|}{2\pi} = \frac{G_s}{2\pi C_1}$$

* Typically, $g_{m1} = g_{m2}$, then $C_1 = C_{gs1} + 2C_{gd1}$

§ 6-1.4 CMOS gain stage



$$G_{Leq} = g_{ds1} + g_{ds2} \qquad C_{Leq} = C_{db1} + C_{db2} + C_L$$

$$C_{in} = C_{gs1} + C_{gs2} + (1 + \frac{g_{m1} + g_{m2}}{G_{Leq}})(C_{gd1} + C_{gd2})$$

$$A_v(s) \cong \frac{G_s[s(C_{gd1} + C_{gd2}) - (g_{m2} + g_{m2})]}{[s(C_{gd1} + C_{gd2} + C_{Leq}) + G_{Leq}](sC_{in} + G_s)}$$

RHP Zero: $S_z = \dfrac{g_{m1} + g_{m2}}{C_{gd1} + C_{gd2}}$

LHP Poleo: $S_{p1} = -\dfrac{G_s}{C_{in}}$

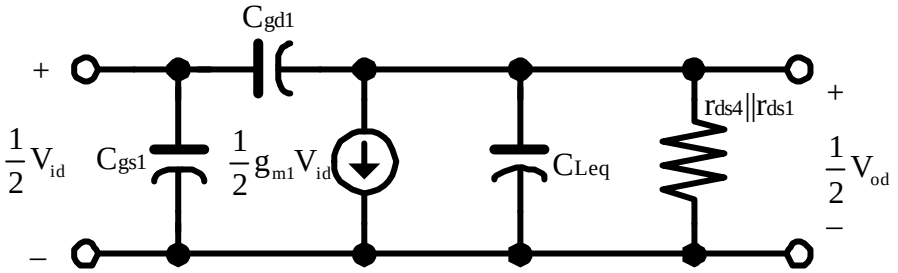
$$S_{p2} = -\frac{G_{Leq}}{C_{gd1} + C_{gd2} + C_{Leq}}$$

If R_s is large enough (R_s is the output resistance of the preceding stage),
$|S_{p1}| << |S_{p2}|$

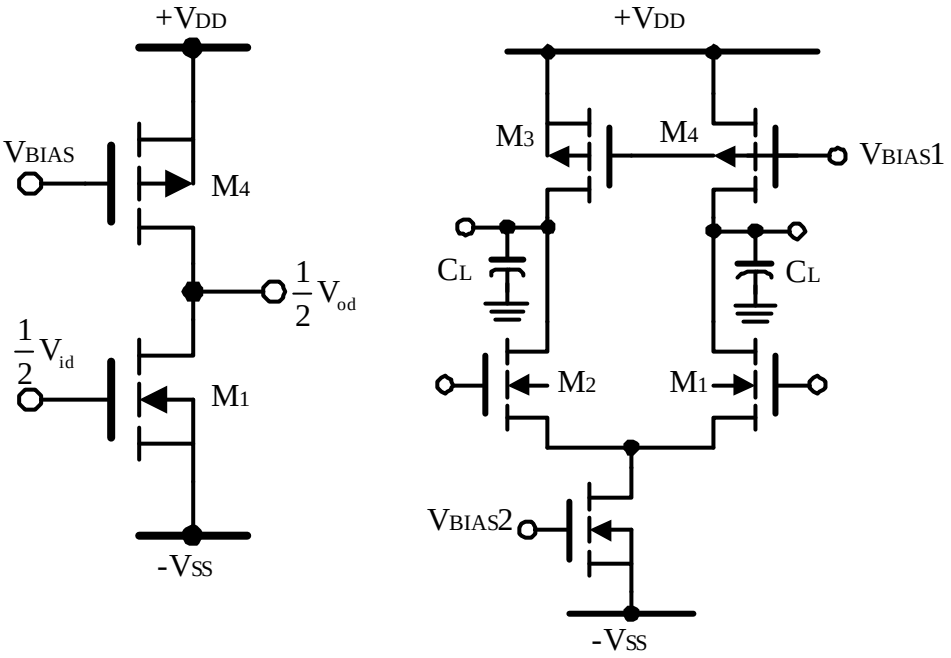
S_{p1} is the dominant pole.

§ 6-1.5 CMOS differential amplifier

1.Differential-mode half circuit



$$C_{Leq} \equiv C_L + C_{db4} + C_{db1}$$

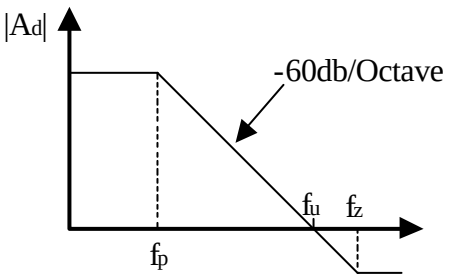


$$A_d = \frac{V_{od}}{V_{id}} = H(s) = -\frac{g_{m1}}{g_{ds4}+g_{ds1}}\left[\frac{1-s\frac{C_{gd1}}{g_{m1}}}{1+(\frac{C_{Leq}+C_{gd1}}{g_{ds4}+g_{ds1}})s}\right]$$

RHP Zero: $f_z = \frac{g_{m1}}{2\pi C_{gd1}}$ $\quad f_z > f_p$

LHP Pole: $f_p = \frac{g_{ds4}+g_{ds1}}{2\pi(C_{db4}+C_{db1}+C_L+C_{gd1})}$

$f_u \quad A_0 f_p = \frac{g_{m1}}{2\pi(C_{db4}+C_{db1}+C_L+C_{gd1})}$



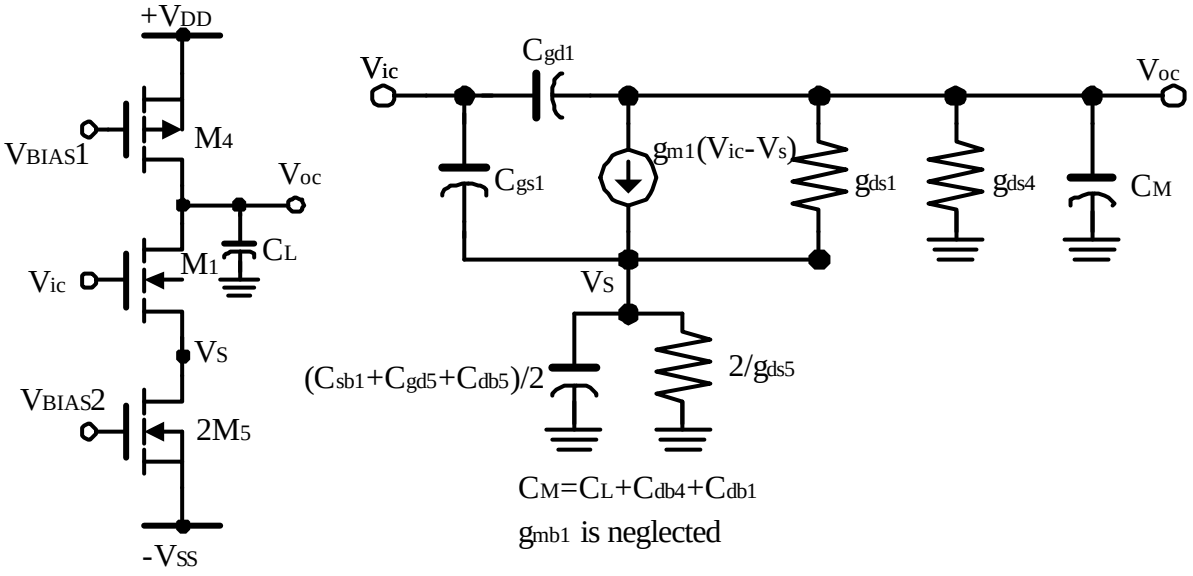
2.Common-mode half circuit:

$$(g_{ds4}+sC_M)V_{oc} + g_{ds1}(V_{oc}-V_s) + g_{m1}(V_{ic}-V_s) + C_{gd1}s(V_{oc}-V_{ic}) = 0$$

$$g_{ds1}(V_s - V_{oc}) + V_s(\frac{1}{2r_{ds5}} + \frac{C_{gd5} + C_{db5} + C_{sb1}}{2}s) - g_{m1}(V_{ic} - V_s) - C_{gs1}s(V_{ic} - V_s) = 0$$

$$V_s[\frac{1}{2r_{ds5}} + \frac{1}{2}(C_{gd5} + C_{db5} + C_{sb1})s + C_{gs1}s] = -[g_{ds4} + sC_M + sC_{gd1}]V_{oc} + (C_{gs1}s + C_{gd1}s)V_{ic}$$

$$V_s = -\frac{[g_{ds4} + sC_M + sC_{gd1}]V_{oc} - (C_{gs1}s + C_{gd1}s)V_{ic}}{\left[\frac{1}{2r_{ds5}} + \frac{C_{gd5} + C_{db5} + C_{sb1}}{2}s + C_{gs1}s\right]}$$



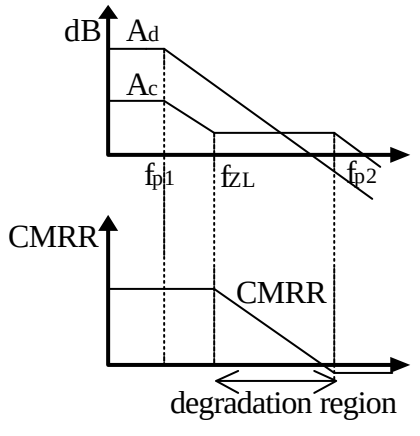
$C_M = C_L + C_{db4} + C_{db1}$

g_{mb1} is neglected

$$\Rightarrow A_c(s) = \frac{V_{oc}}{V_{ic}} = -\frac{-C_{gd1}(\frac{C_{gd5} + C_{db5} + C_{sb1}}{2} + C_{gs1})s^2 + [(\frac{C_{gd5} + C_{db5} + C_{sb1}}{2} + C_{gs1})g_{m1}}{(\frac{C_{gd5} + C_{db5} + C_{sb1}}{2} + C_{gs1})(C_M + C_{gd1})s^2 + [(\frac{C_{gd5} + C_{db5} + C_{sb1}}{2} + C_{gs1})}$$

$$\frac{-\frac{1}{2r_{ds5}}C_{gd1} - (g_{ds1} + g_{m1})(C_{gs1} + C_{gd1})]s + \frac{1}{2r_{ds5}}g_{m1}}{(g_{ds4} + g_{ds1}) + \frac{C_M + C_{gd1}}{2r_{ds5}} + (C_M + C_{gd1})(g_{ds1} + g_{m1})]s + \frac{g_{ds4} + g_{ds1}}{2r_{ds5}} + (g_{ds1} + g_{m1})g_{ds4}}$$

Solve the pole-zero position : $\Rightarrow$ 1 RHP zero, 1 LHP zero,2 LHP poles



f_{ZR} f_{ZL} f_{p1} f_{p2}

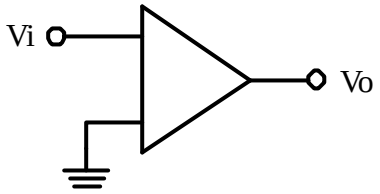
$f_{ZR} >> f_{ZL}$

f_{p1}: C_M f_{p2}: $(C_{gd5}+C_{db5}+C_{sb1})/2$

$f_{p1} < f_{p2}$

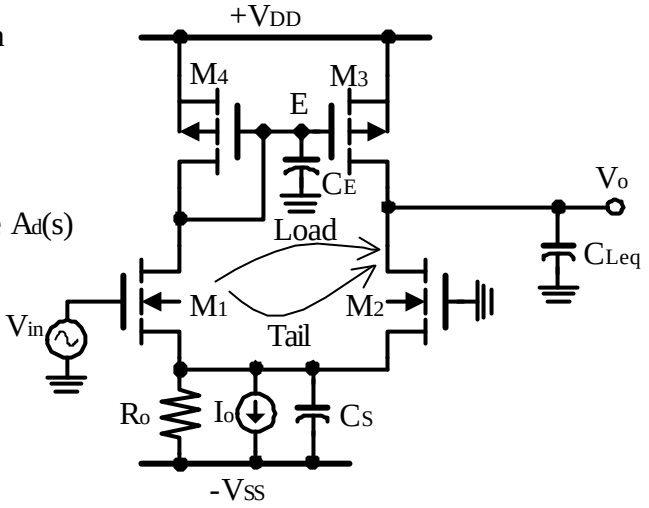
Load pole tail pole

§ 6-1.6 CMOS differential-input-to-single-ended output converter



$$V_i = V_{id} + V_{ic} \quad V_o = V_{od} + V_{oc}$$

* The hail-circuit method cannot be used in the high frequency analysis.
* Two unequal signal paths to the output
  - $\Rightarrow$ Load path and tail path
  - $\Rightarrow$ Both C_s and C_E appears in the $A_d(s)$ expression.
* There are two dominate poleo in A_d.



Output pole $W_{p1} \cong \dfrac{g_{ds1} + g_{ds4}}{C_{Leq}}$

Mirror pole $W_{p2} \cong \dfrac{g_{m34}}{C_E}$

Tail path: $A_1(s) = \dfrac{A_0}{1 + \dfrac{s}{W_{p1}}}$

Load path: $A_2(s) = \dfrac{A_0}{(1 + \dfrac{s}{W_{p1}})(1 + \dfrac{s}{W_{p2}})}$

$$A_d(s) = A_1(s)A_s(s) = \frac{A_0(2 + \dfrac{s}{W_{p2}})}{(1 + \dfrac{s}{W_{p1}})(1 + \dfrac{s}{W_{p2}})}$$

LHP zero: $W_{z1} \cong \dfrac{2g_{m34}}{C_E} = 2W_{p2}$

* Approximate analysis:

The dominant pole of $A_d(s)$ is $S_{p1} = -\dfrac{g_{ds1} + g_{ds4}}{C_{Leq}}$ (output pole)

$$A_d(s) \cong \frac{g_{m1}}{sC_{Leq} + (g_{ds1} + g_{ds4})}$$

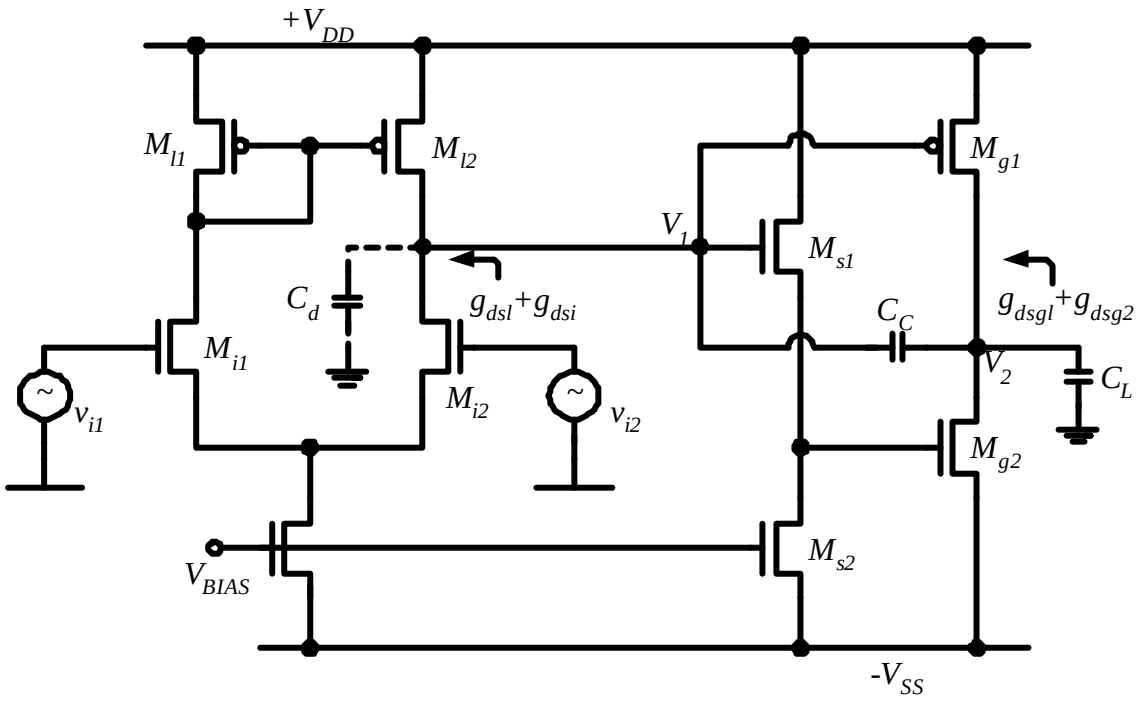
The $A_c(s)$ can be written as $A_c(s) \cong -\frac{g_{ds1}}{2g_{m4}} \frac{(\frac{1}{R_0}) + sC_s}{sC_{Leq} + (g_{ds1} + g_{ds4})}$

The dominant pole of $A_c(s)$ is $S_{p1} = -\frac{g_{ds1} + g_{ds4}}{C_{Leq}}$

But the left-half-plane zero is $S_{zL} = -\frac{1}{R_0}(\frac{1}{C_s})$

The CMRR$(\equiv \frac{A_d}{A_c})$ is degradated by 20dB/decade at high frequency.

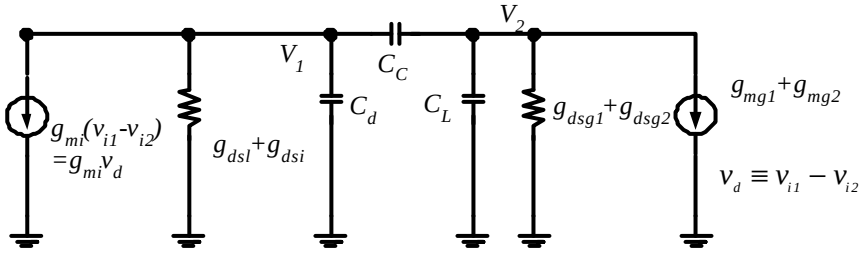
§6-2 Frequency Compensations



Without C_C

$$S_{P1} = -\frac{1}{C_d}(g_{dsl} + g_{dsi}) \ , \quad S_{P2} = -\frac{1}{C_L}(g_{dsg1} + g_{dsg2})$$

equivalent circuit



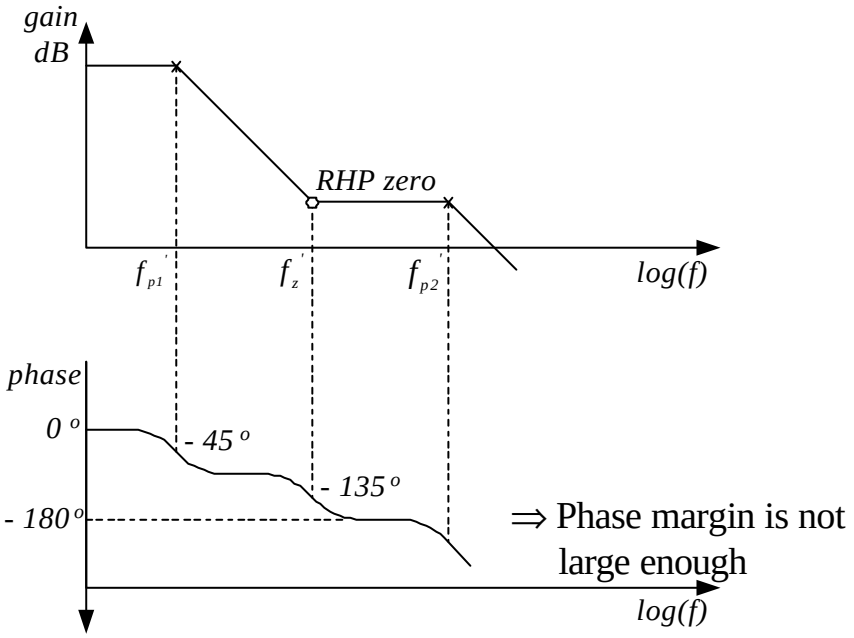
$$H(s)=\frac{v_2}{v_{i1}-v_{i2}}$$

$$=\frac{+g_{mi}(g_{mg1}+g_{mg2})R_dR_o(1-\dfrac{sC_C}{g_{mg1}+g_{mg2}})}{1+s[(C_L+C_C)R_O+(C_C+C_d)R_d+C_C(g_{mg1}+g_{mg2})R_OR_d]+(C_CC_L+C_CC_d+C_dC_L)R_OR_ds^2}$$

where $R_o \equiv -\dfrac{1}{g_{dsg1}+g_{dsg2}}$ $\qquad$ $R_d \equiv -\dfrac{1}{g_{dsl}+g_{dsi}}$

$$\Rightarrow \quad S_{p1}' \approx -\frac{1}{(g_{mg1}+g_{mg2})R_OR_dC_C} \qquad S_{p2}' \approx -\frac{C_C(g_{mg1}+g_{mg2})}{C_OC_L+C_dC_L+C_dC_C}$$

$$S_z' \approx \frac{g_{mg1}+g_{mg2}}{C_C} \quad \rightarrow \text{RHP Zero}$$



$\Rightarrow$ Phase margin is not large enough

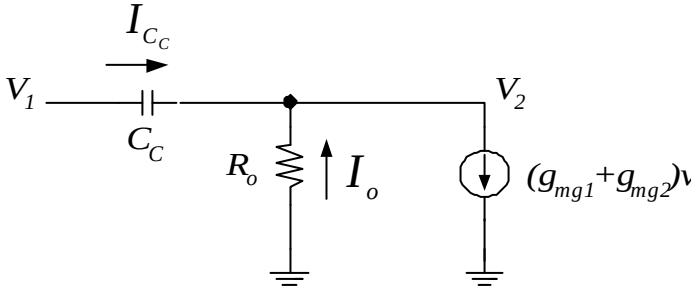
* Feedforward effect on C_C

How to solve this problem ?

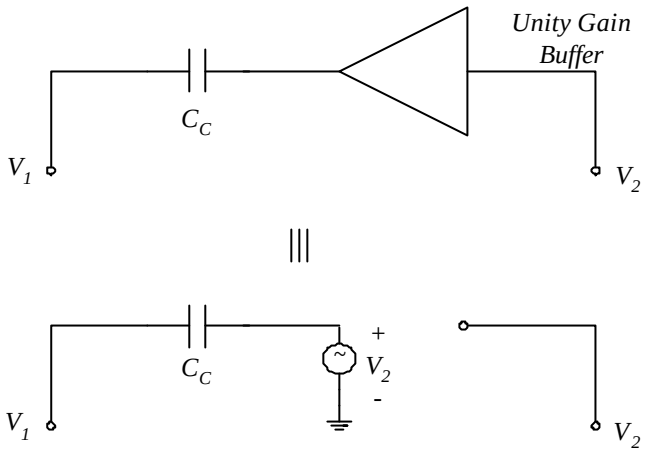
If $I_{C_C}=(g_{mg1}+g_{mg2})V_d$,

$I_o=0$ and $V_2=0$

$\Rightarrow$ A zero is formed.



§6-2.1 Using a unity-gain buffer in the feedback path



* Isolate node 1 from node 2 to prevent feedforward.
* Keep the Miller effect unchanged.
* Source follower can act as a unity gain buffer.

$$g_{mi}V_d + \frac{V_1}{R_d} + C_d sV_1 + (V_1 - V_2)C_c s = 0 \qquad \text{--------- (1)}$$

$$(g_{mg1} + g_{mg2})V_1 + \frac{1}{R_o}V_2 + C_L sV_2 = 0 \qquad \text{--------- (2)}$$

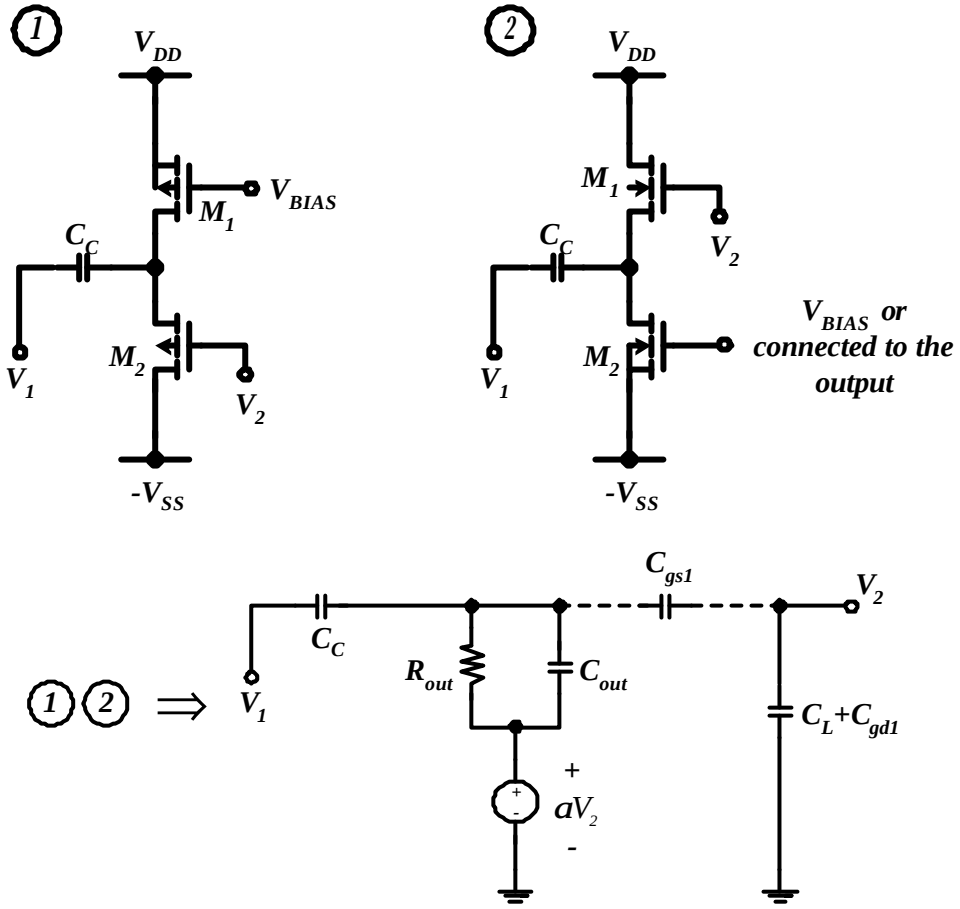
$$H(s) = \frac{V_2}{V_d}$$

$$= \frac{g_{mi}(g_{mg1} + g_{mg2})}{1 + s\left[R_o C_c + R_d(C_d + C_c) + C_c(g_{mg1} + g_{mg2})R_o R_d\right] + (C_c C_L + C_d C_L)R_o R_d s}$$

$$S_{p1}' \approx -\frac{1}{(g_{mg1} + g_{mg2})R_o R_d C_c} \quad \text{(unchanged)}$$

$$S_{p2}' \approx -\frac{C_c(g_{mg1} + g_{mg2})}{C_c C_L + C_d C_L} \qquad \text{RHP Zero has be eliminated.}$$

Actual Circuits :



* C_{gs1} may introduce a RHP zero. But usually this RHP zero is large.

∵ C_{gs1} is very small.

* $R_{out} \approx (\frac{1}{g_{m1}} \| \frac{1}{g_{m2}})$

$$g_{mi}V_d + \frac{V_1}{R_d} + C_d s V_1 + (V_1 - aV_2)(\frac{1}{C_c s} + \frac{1}{\frac{1}{R_{out}} + C_{out}s})^{-1} = 0$$

If $\frac{1}{R_{out}} \geq C_{out}s$

$$\Rightarrow \left(\frac{1}{C_c s} + \frac{1}{\frac{1}{R_{out}} + C_{out}s} \right)^{-1} \approx \frac{C_c s}{C_c R_{out} s + 1}$$

The numerator of $H(s)=\frac{V_2(s)}{V_d(s)}$ is $g_{mi}(g_{mg1}+g_{mg2})(C_cR_{out}s+1)$

$\Rightarrow$ LHP Zero : $-\frac{1}{C_cR_{out}}$

If R_{out} is large , LHP Zero may form a pole-zero doublet with S_{p1}' or S_{p2}'

$\Rightarrow$ very slow slew rate !!

If R_{out} is small , too large g_{m1} or g_{m2} is required.

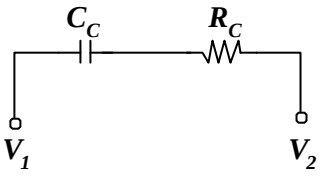
$\Rightarrow$ (large area ,large power)

$\Rightarrow$ large C_{out}. Freq. Resp. $\downarrow$

* Somehow difficult to design.

* Also the power dissipation of the buffer is large. (additional power dissipation)

§6-2.2 Adding Rc in series with Cc.



$H(s)=\frac{v_2}{v_d}$ can be solved.

Low frequency gain : $A_{dm}=g_{mi}(g_{mg1}+g_{mg2})R_oR_d$

LHP Poles : $S_{P1}\cong\frac{-1}{(g_{mg1}+g_{mg2})R_oR_dC_c}$ (unchanged)

$$S_{P2}\cong-\frac{(g_{mg1}+g_{mg2})C_c}{C_dC_L+C_cC_L+C_dC_c}$$ (unchanged)

$$S_{P3}\cong-\frac{C_dC_c+C_dC_L+C_cC_L}{R_CC_dC_LC_c}$$

$$\begin{pmatrix}LHP\\RHP\end{pmatrix}Zero: S_Z=-\frac{g_{mg1}+g_{mg2}}{C_c[R_c(g_{mg1}+g_{mg2})-1]}$$

1. If $R_C = \dfrac{1}{g_{mg1} + g_{mg2}}$ or $R_C = \dfrac{1}{g_{m2}}$ g_{m2} : second-stage transconductance

$S_Z \to \pm\infty$ No effect on the frequency response of the OP.

S_{P1} dominant pole $\Rightarrow$ $A_d(s) \cong \dfrac{A_{dm}}{\dfrac{s}{S_{P1}} + 1} = \dfrac{A_{do} S_{P1}}{s + S_{P1}}$

For $w >> S_{P1}$ $A_d(jw) = \dfrac{A_{dm} S_{P1}}{jw}, |A_d(jw)| = \dfrac{A_{dm} S_{P1}}{w}$

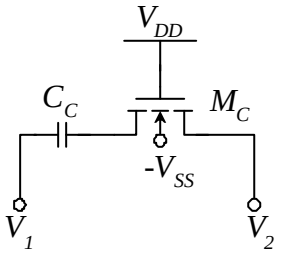
At w_u , $|A_d(jw_u)| = 1$ $\Rightarrow$ $w_u = A_{dm} S_{P1} = \dfrac{g_{mi}}{C_c}$

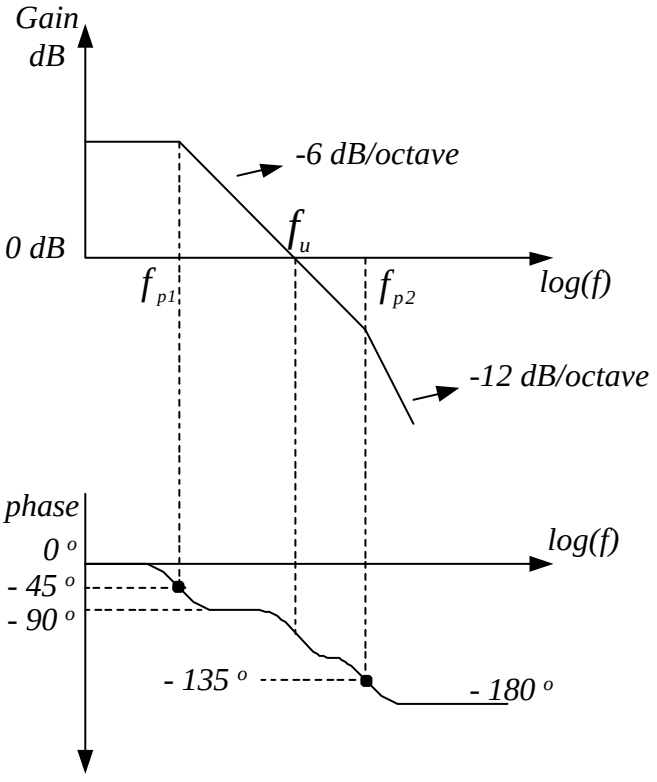
Large $C_L \Rightarrow S_{P2} \approx -\dfrac{g_{mg1} + g_{mg2}}{C_L}$

For phase margin $45^0 \sim 60^0$ $\Rightarrow$ $\dfrac{S_{P2}}{w_u} \cong 2 \sim 4, \dfrac{C_c}{C_L} \dfrac{g_{mg1} + g_{mg2}}{g_{mi}} = 2 \sim 4$

If $\dfrac{g_{mi}}{g_{mg1} + g_{mg2}} \cong 2 \sim 4$, $C_L \cong C_c$ stable

1) NMOS Realization :

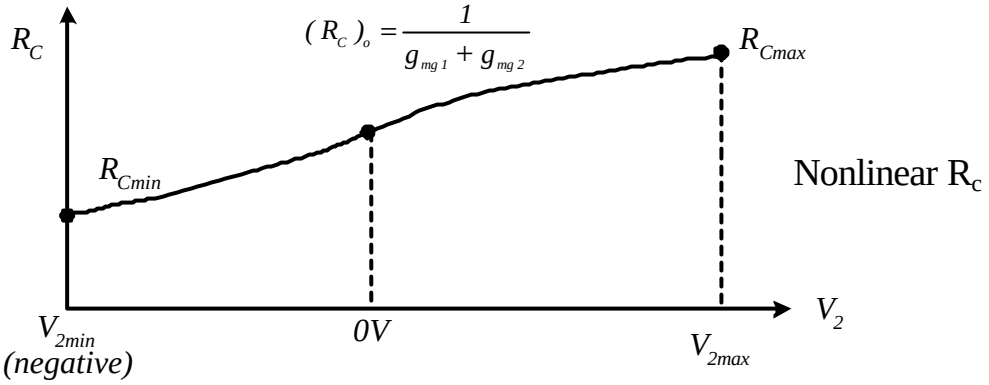




$$I_{DS} = \frac{m_n C_{ox}}{2}\frac{W}{L}\left[2(V_{DD} - V_2 - V_{TH})V_{DS} - V_{DS}^{\ 2}\right] ,$$

$$R_C = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)^{-1}\Bigg|_{V_{DS}=0} = \frac{1}{\frac{m_n C_{ox}}{2}\frac{W}{L}\left[2(V_{DD} - V_2 - V_{TH})\right]}$$

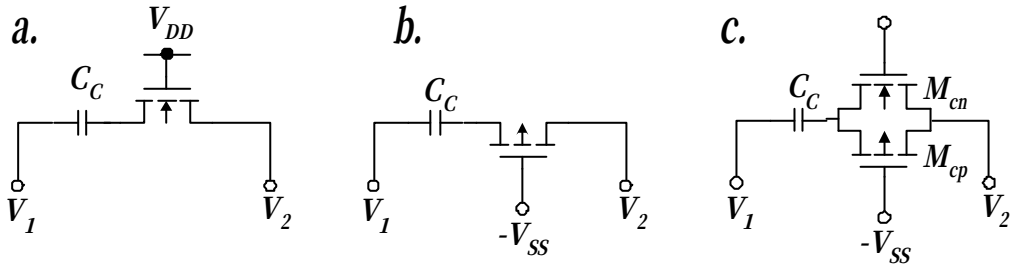
$V_2 \uparrow$ $V_{TH} \uparrow$ body effect



Design R_c : (1) Design R_c, s.t. $(R_c)_{V_2=0V} = \frac{1}{g_{m2}}\left(\frac{1}{g_{mg1} + g_{mg2}}\right)$

(2) At $R_c = R_{cmax}$ or R_{cmin} ,
S_z must be large enough ! Otherwise, frequency performance will be degradated.

1) CMOS Realizations :



Consider the case in *c.*:

$$I_{DSn} = \frac{m_n C_{ox}}{2}\frac{W_n}{L_n}\left[2(V_{DD} - V_2 - V_{THn})V_{DS} - V_{DS}^{\ 2}\right]$$

$$R_{cn} = \frac{1}{\frac{m_n C_{ox}}{2}\frac{W_n}{L_n}\left[2(V_{DD} - V_2 - V_{THn})\right]}$$

$$I_{DSp} = \frac{m_p C_{ox}}{2}\frac{W_p}{L_p}[2(V_2 + V_{SS} - V_{THp})V_{DS} - V_{DS}^{\ 2}]$$

$$R_{cp} = \frac{1}{\frac{m_p C_{ox}}{2}\frac{W_p}{L_p}[2(V_2 + V_{SS} - V_{THp})]}$$

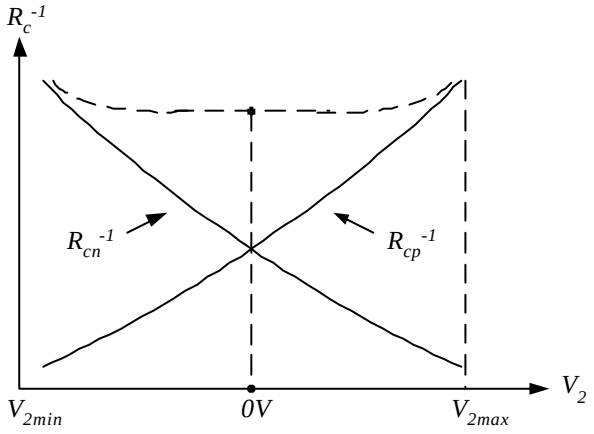
$$R_c^{-1} = (R_{cn} // R_{cp})^{-1} = R_{cn}^{-1} + R_{cp}^{-1}$$

$$= \frac{m_n C_{ox}}{2}\frac{W_n}{L_n}[2(V_{DD} - V_2 - V_{THn})] + \frac{m_p C_{ox}}{2}\frac{W_p}{L_p}[2(V_2 + V_{SS} - V_{THp})]$$

If $\frac{m_n C_{ox}}{2}\frac{W_n}{L_n} = \frac{m_p C_{ox}}{2}\frac{W_p}{L_p} = b$

$$R_c^{-1} = b[2V_{DD} - 2V_{THn} + 2V_{SS} - 2V_{THp}]$$ nearly indep. Of V_2

$$R_c^{-1}\Big|_{V_2=0V} = g_{mg1} + g_{mg2}$$



2. If $R_c = \frac{1 + (C_d + C_L)/C_C}{g_{mg1} + g_{mg2}}$

$S_z = S_{p2}$ and pole-zero cancellation occurs.

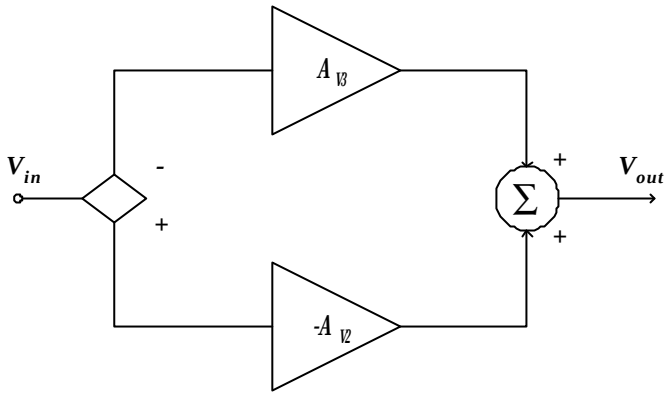
$\Rightarrow S_{p3} >> S_{p1} \Rightarrow A_{dm}S_{p1} < S_{p3} \Rightarrow$ stable

However, if the cancellation is not complete

$\Rightarrow$ pole-zero doublet occurs ! $\Rightarrow$ slow slew rate.

§6-2.2 Feedforward compensation

A_{v3} is the gain of the source follower



$$A_{v3}=\frac{A_{v3}(0)(1+\frac{s}{z_3})}{(1+\frac{s}{P_3})}$$

1 LHP zero
1 LHP pole

$$A_{v2}=\frac{A_{v2}(0)(1-\frac{s}{z_1})(1+\frac{s}{z_2})}{(1+\frac{s}{P_1})(1+\frac{s}{P_2})}$$

2 LHP poles
1 RHP zero (C_C)
1 LHP zero

z_3 & z_2 are generated from the C_{gs} of the source follower.

$$\frac{V_{out}}{V_{in}}=A_{VTOT}(s)=A_{V2}(s)+A_{V3}(s)$$

$$=[A_{V2}(0)+A_{V3}(0)]\frac{(1+\frac{s}{z_1'})(1+\frac{s}{z_2'})(1+\frac{s}{z_3'})}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})(1+\frac{s}{p_3})}$$

p_1' : dominant pole

z_1', z_2', z_3' : LHP Zeros

Design consideration : Any zeros below the unity-gain frequency must be placed as close as possible to their matching poles. This prevents the formation of any doublet !

$z_1' = p_2$ by adding CB1 and CB2(3.8pF) to control $C_{gs9}+C_{gs11}$

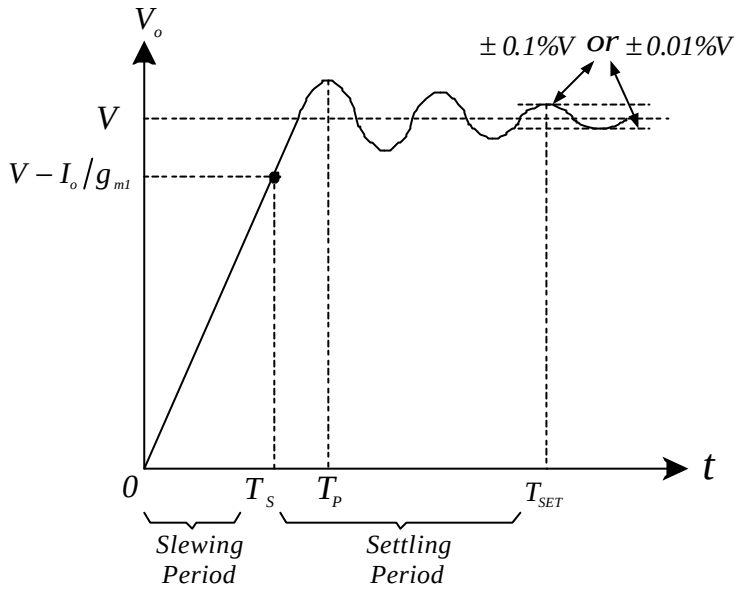
Ref:IEEE JSSC , col SC-14, no.6 pp.1070-1077 , DEC.1979

Feedfoward +Miller(direct)

Ref:IEEE JSSC , col SC-15, no.6 pp.921-928 , DEC.1980

Feedfoward +Unity gain buffer + Miller

§ 6-3 Settling Behavior



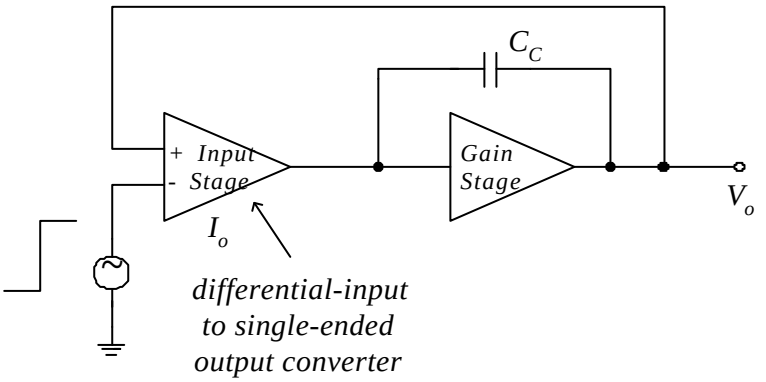
Slewing Period (*Ts*): V_o from 0V to $V\text{-}I_o/g_{m1}$ under voltage follower connection and worse case loading.(nonlinear operation)

Settling Period ($T_{SET}\text{-}T_s$):

V_o from ($V\text{-}I_o/g_{m1}$) to $\pm 0.1\%$ V or $\pm 0.01\%$ V (quasi-linear operation)

Settling Time (T_{SET}): T_s +($T_{SET}\text{-}T_s$) = slewing period + settling period.

§ 6-3.1 Single-pole case



Slew rate:

$$SR \equiv \frac{dVo}{dt}\Big|_{max} = \frac{I_o}{C_c}$$

$$w_u = \frac{g_{mi}}{C_c} \leftarrow \text{single-pole case}$$

$$SR = \frac{I_o w_u}{g_{mi}} = w_u \sqrt{\frac{I_o}{2\frac{uC_{ox}}{2}(\frac{W}{L})_i}}$$

§ 6-3.1 Two-pole case

Ref；IEEE JSSC vol.SC-17, no.1 pp.74-80, Feb. 1982

$$Ts = -\frac{1}{w_1} ln[1 - \frac{g_{m1}}{I_o a_o}(V - \frac{I_o}{g_{m1}})$$ Fig.2

approximation： $e^{-w_1 T_S} \cong 1 - w_1 T_S$ => eq.(19) conventional expression

After Ts： $V_o = V - I_o/g_{m1}$ Input voltage = $V-(V-I_o/g_{m1}) = I_o/g_{m1}$

=> enter the linear (or quasi-linear) region

Feedback Function for unity-gain voltage-follower connection

=> $A(s) = \frac{a(s)}{1 + a(s)}$ eq.(20)-(23)

two poles： $S = -xw_n \pm \sqrt{x^2 - 1} w_n$ eq.(24) $\boxed{\xi = \frac{\omega_1 + \omega_2}{2\omega_n}}$

(double negative real poles) damping ratio

x = 1 critically damped

x < 1 underdamped x > 1 overdamped

(complex conjugate poles) (real and negative pole)

$$x = \frac{w_1 + w_2}{2w_n} \cong \frac{\sqrt{w_2}}{2\sqrt{a_o w_1}} = \frac{\sqrt{w_2}}{2\sqrt{w_u}} = \frac{\sqrt{g_{m2}/c_2}}{2\sqrt{g_{m1}/c_c}}$$ (C_C, C_2 >> C_1)

$x \gtrless 1 \quad \Rightarrow C_C \gtrless 4(\frac{g_{m1}}{g_{m2}})C_2 \quad (C_C, C_2 >> C_1)$

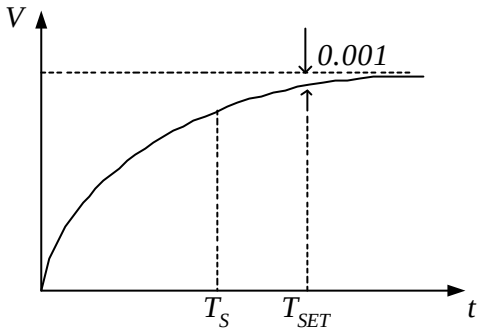
$\Rightarrow \quad w_2 \gtrless 4w_u \Leftrightarrow \frac{w_2}{w_u} = 2 \sim 4$ $\quad \omega_2 < 4\omega_u$ underdamped; $\omega_2 > 4\omega_u$ overdamped

(1) Underdamped: T_S eq. (14) or (19) max.overshoot: eq.(36)

T_P eq. (35), (33) settling time: eq.(40),(39)

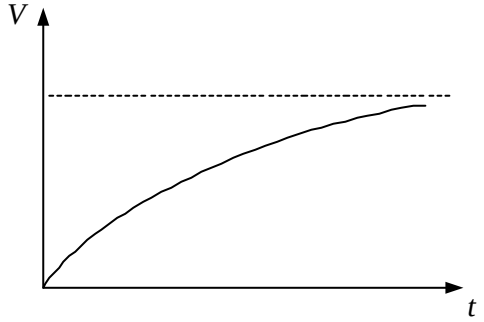
(2) Critically Damped $V_o(t)$: eq.(41)

T_{SET} : eq.(43)



(3) Overdamped T_{SET}: eq.(47)

Simulation & Calculation : Fig.7, Fig.8



Further references:

(1) IEEE JSSC, vol. SC-18, pp.389-394, Aug. 1983

(2) IEEE JSSC, vol. SC-21, pp.478-483, June. 1986

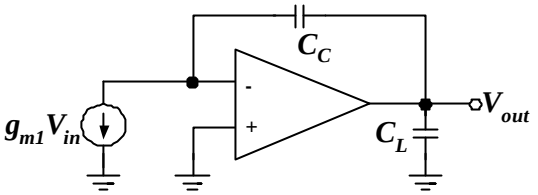
§ 6-4 Slew rate of CMOS OP AMPs

§ 6-4.1 Two-stage OP AMPs

Two poles: $S_{p1}, S_{p2}, |S_{p1}| << |S_{p2}|$

If $|S_{p1}| << w_u << |S_{p2}|, V_{out}(s) = g_{mi} V_{in}(s) / sCc$

$$\frac{V_{out}(jw)}{V_{in}(jw)} = \frac{g_m}{jwCc}$$



At $w = w_u$, $\frac{V_{out}}{V_{in}} = 1$

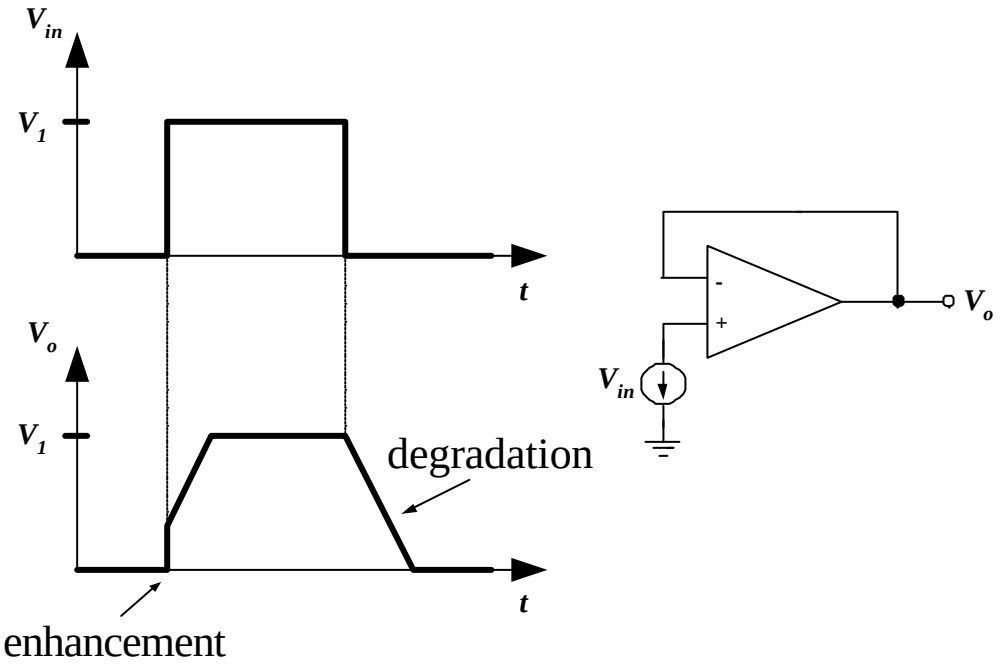
$$\Rightarrow w_u = \frac{g_{mi}}{C_C} \quad or \quad C_C = g_{mi} / w_u$$

The slew rate $SR = \frac{dV_{out}}{dt}\Big|_{max} = I_o / C_C = \frac{I_C w_u}{g_{mi}} = w_u \sqrt{\frac{I_o}{2uC_{ox}(W/L)i}}$

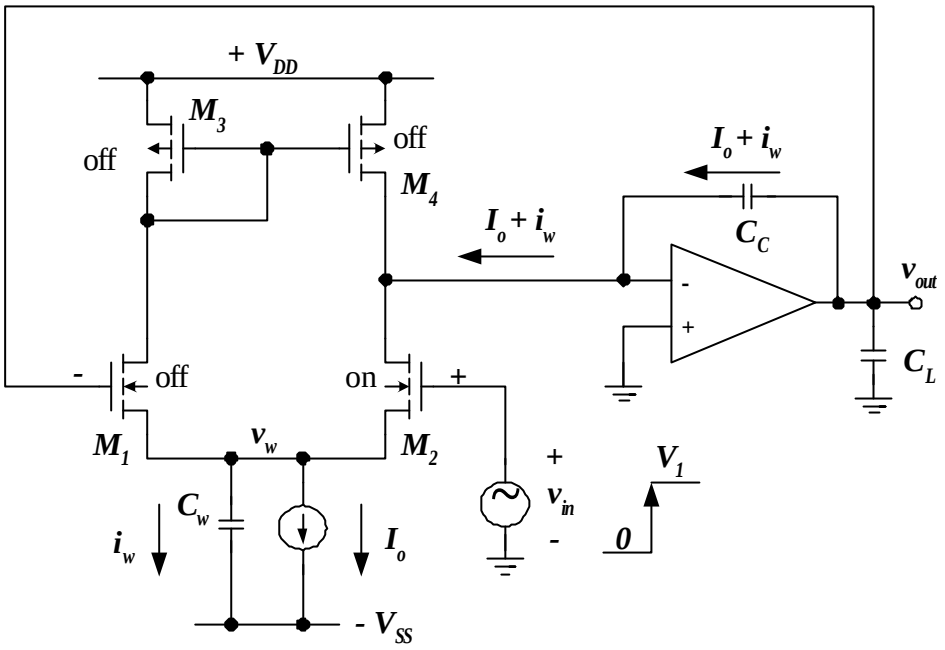
$$w_u \uparrow, I_o \uparrow, (W/L)_i \downarrow \Rightarrow \text{SR} \uparrow$$

* $I_o / C_L \geq I_o / C_C$ or $C_L \frac{dV_{out}}{dt} \leq C_C \frac{dV_{out}}{dt} (= I_o)$

Slew rate enhancement and degradation



(1) Positive step

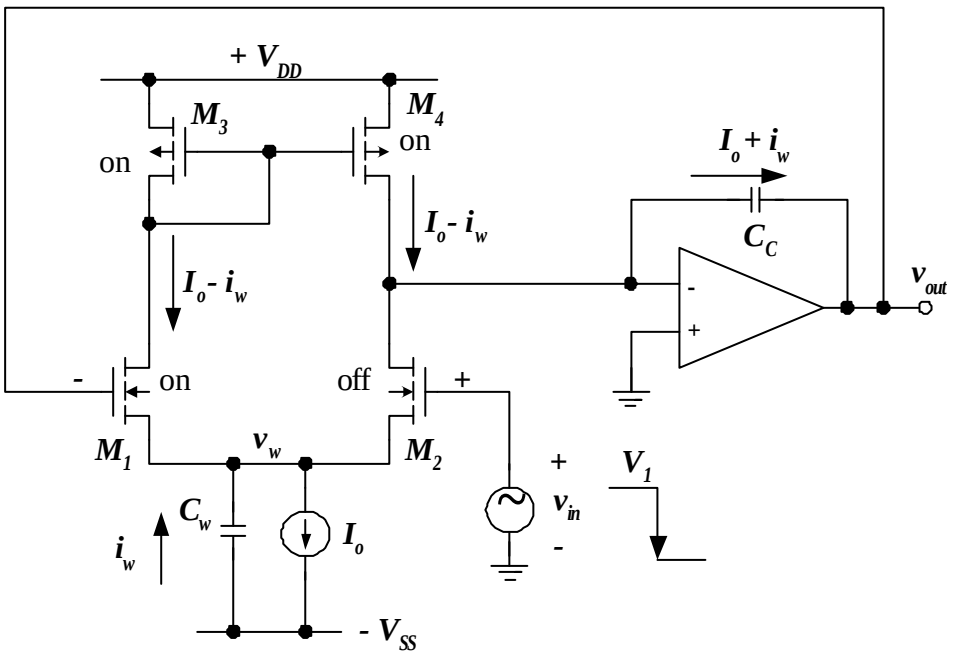


$$i_w(t) = C_w \frac{dv_w(t)}{dt} \cong C_w \frac{dv_{in}(t)}{dt}$$

$$v_{out}(t) = \frac{1}{C_C}\int_0^t (I_o + i_w)dt = \frac{I_o}{C_C}t + \frac{C_w}{C_C}\int_0^t \frac{dv_{in}}{dt}dt$$

$$= \frac{I_o}{C_C}t + \frac{C_w}{C_C}V_1 u(t)$$

(2) Negative step



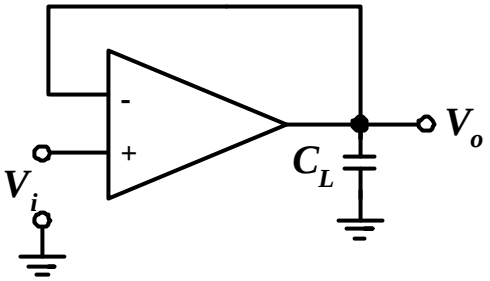
$$v_{out} \cong v_w$$

$$\frac{d}{dt}v_{out} = -\frac{I_o - i_w}{C_C} = \frac{dv_w}{dt} = -\frac{i_w}{C_w} \quad \Rightarrow i_w = \frac{I_o C_w}{(C_C + C_w)}$$

$$\frac{dv_{out}}{dt} = -\frac{I_o}{C_C + C_w}$$ slew degradation

§ 6-4.2 Single-stage OP AMPs

$$SR = \frac{I_o}{C_L}$$

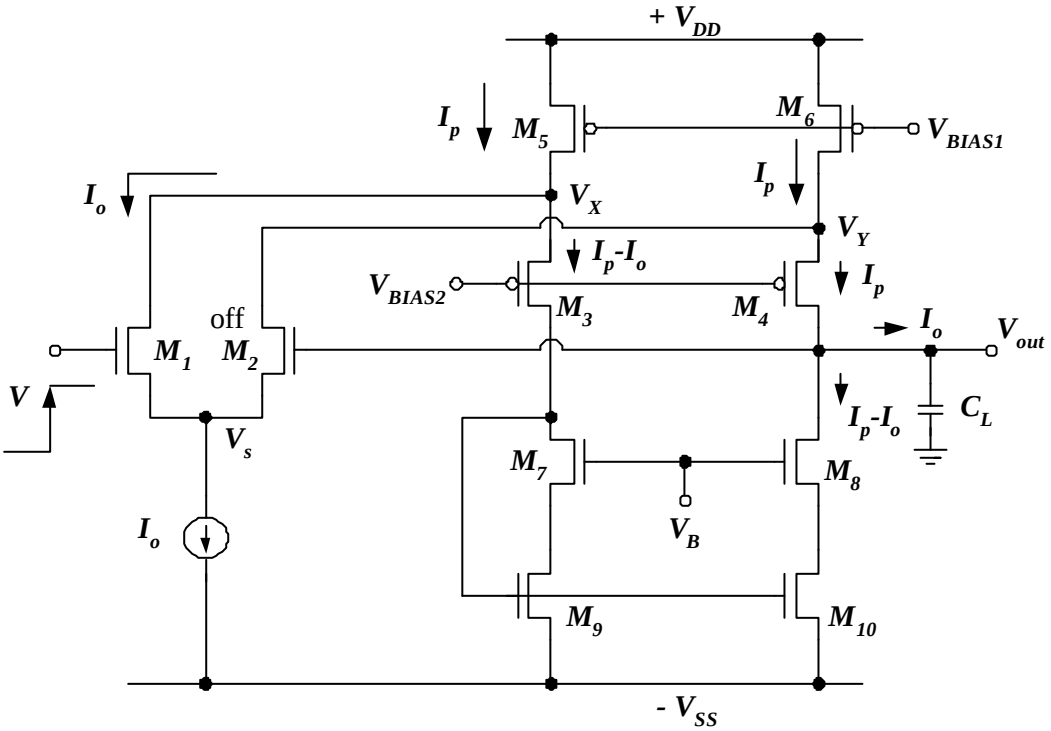


Different phase margins

$\Rightarrow$ different settling behavior.

I_o : First-stage bias current

SR of the folded cascode OP AMPs



$$SR = \frac{I_o}{C_L}$$

* If I_p=I_o, we can keep M_5, M_1 and I_o current source in saturation.

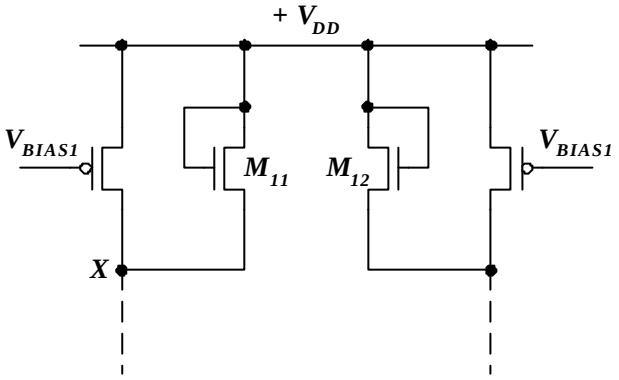
The change of V_x is not significant because the gain of the common-source amplifier M_1 is nearly equal to –1. When M_2 is turned on, the recovery time of V_x is very short.

* If $I_p < I_o$, the current source I_o is forced to linear region and $V_s\downarrow$ $V_x\downarrow$. The decrease of V_x is large. Thus the recovery time of V_x when M_2 is turned on is very long, $\Rightarrow$ The settling is slow down.

How to solve this problem?

(1) Keep $I_p = I_o$ as the optimal design.

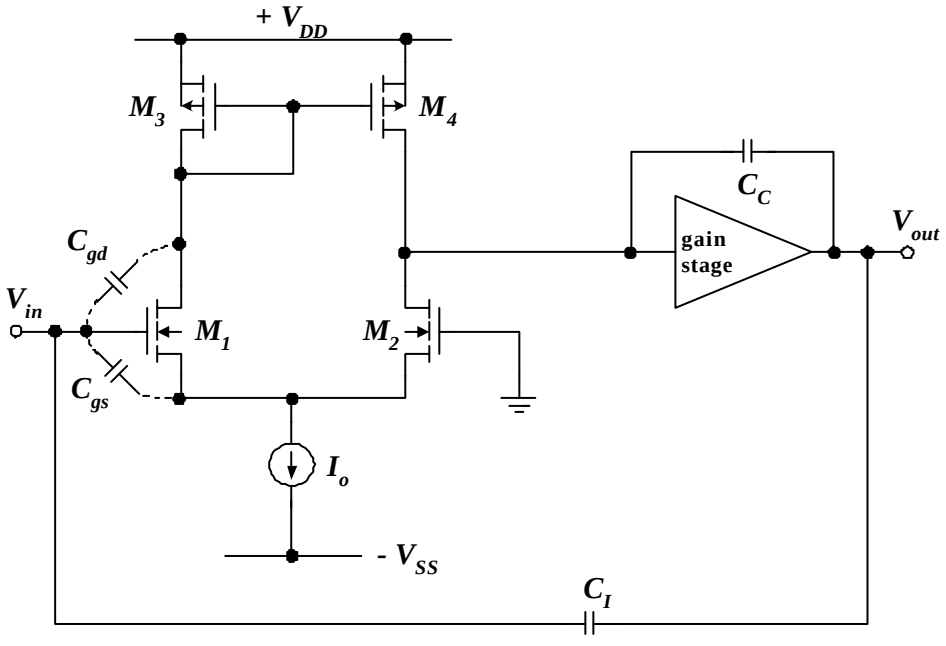
(2) Add clamping devices between V_{DD} and $V_x(V_Y)$



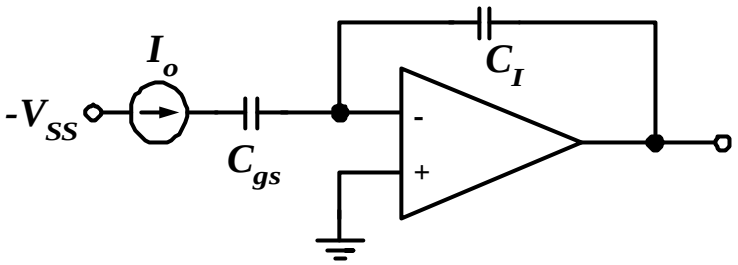
In normal operation, M_{11} and M_{12} are turned off by setting V_{DD}-$V_x < V_{TH11}, V_{TH12}$.

§ 6-5 Power supply rejection ratio (*PSRR*)

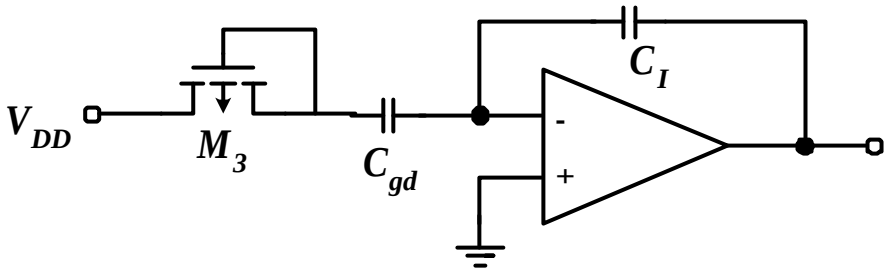
§ 6-5.1 Low frequency analysis for integrators



$$\frac{\partial V_{out}}{\partial V_{SS}} \cong \frac{C_{gs}}{C_I}\left[\frac{\partial I_o}{\partial V_{SS}}\frac{1}{2g_{m1}} + \frac{\partial V_{GS1}}{\partial V_{SS}}\right] + \frac{C_{gd}}{C_I}\frac{1}{2g_{m3}}\frac{\partial I_o}{\partial V_{SS}}$$



$$\frac{\partial V_{out}}{\partial V_{DD}} \cong -\frac{C_{gd}}{C_I}\left[1 - \frac{\partial I_o}{\partial V_{DD}}\frac{1}{2g_{m3}}\right] + \frac{C_{gs}}{C_I}\frac{1}{2g_{m1}}\frac{\partial I_o}{\partial V_{DD}}$$



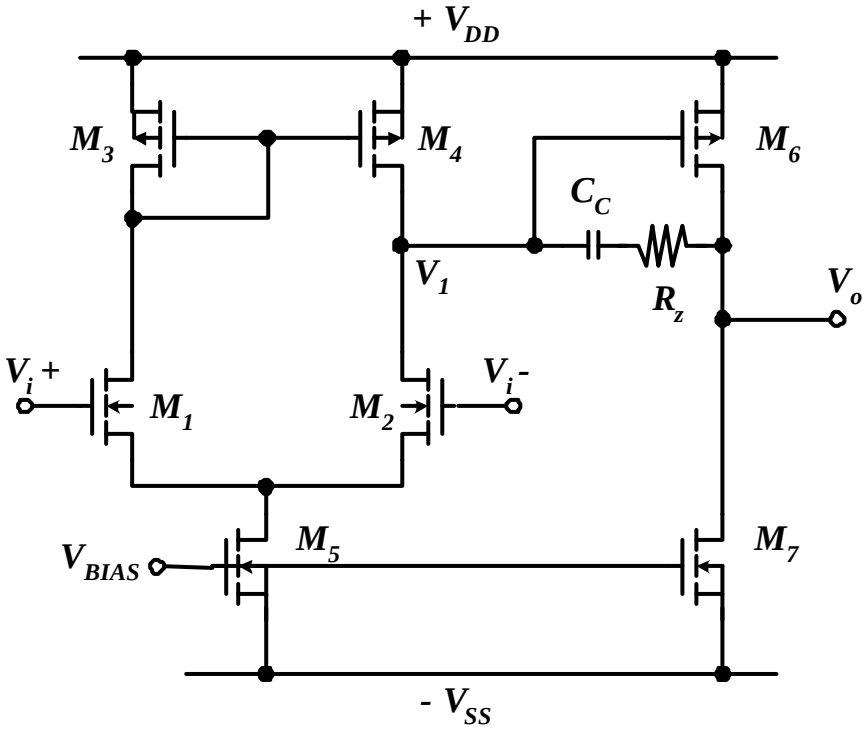
Ref. : IEEE , JSSC , vol.SC-15 , pp.929-938 , Dec. 1980.

* C_{gs}/C_I and C_{gd}/C_I have a strong effect on $PSRR^+$ and $PSRR^-$.

* Small $C_I \Rightarrow$ chip area $\downarrow$ but $PSRR \downarrow$.

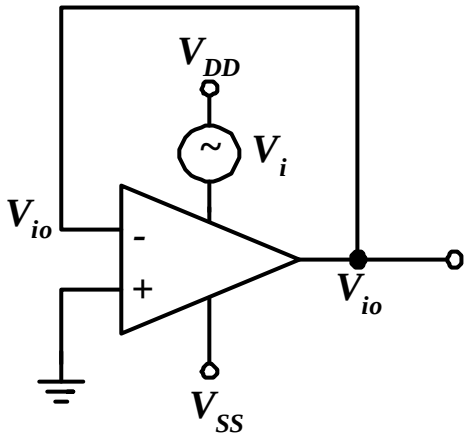
§ 6-5.2 High frequency analysis for OP AMP's

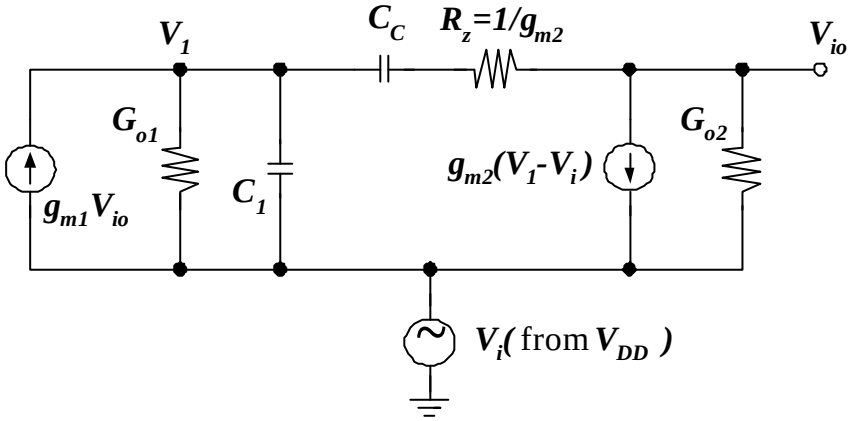
Ref. : IEEE JSSC , vol. sc-19 , pp. 919-925 , Dec. 1984.



$$* \quad PSRR^{+} \equiv \frac{\left|\frac{\partial V_o}{\partial V_i}\right|}{\left|\frac{\partial V_o}{\partial V_{DD}}\right|} = \frac{\left|\frac{\partial V_o}{\partial V_i}\right|_{V_o=0}}{\left|\frac{\partial V_o}{\partial V_{DD}}\right|_{V_o=0}} = \left[\left.\frac{\partial V_{io}}{\partial V_{DD}}\right|_{V_o=0}\right]^{-1}$$

How to calculate $\frac{\partial V_{io}}{\partial V_{DD}}$?





$$PSRR^{+}(s) \cong \frac{s + G_{o1}G_{o2}/(g_{m2}C_c)}{s + g_{m1}/C_c}$$

where $G_{o1}=g_{o4}$ (g_{o2} is connected to the drain of M_5 which is open-circuited, i.e. $r_{ds5} \to \infty$)

$G_{o2}=g_{o6}$ $(r_{ds7} \to \infty)$

$G_{o1}G_{o2}/(g_{m2}C_c) < g_{m1}/C_c$

$\Rightarrow$ Low-frequency LHP zero degrades the *PSRR* .

* To improve *PSRR*, C_c must be decoupled from the gate of M_6 to eliminate the LHP zero .