Chapter 8 Advanced Design Techniques and Recent Design Examples of CMOS OP AMPs

§8-1 Advanced Design Techniques of CMOS OP AMPs

§8-1.1 Improved PSRR and frequency compensation

P.6-26

$$\frac{\partial V_{out}}{\partial V_{ss}} \approx \frac{C_{gs}}{C_I}\left[\frac{\partial I_o}{\partial V_{ss}}\frac{1}{2g_{m1}}+\frac{\partial V_{GS1}}{V_{ss}}\right]+\frac{C_{gd}}{C_I}\frac{1}{2g_{m3}}\frac{\partial I_o}{\partial V_{ss}}$$

$$\frac{\partial V_{out}}{\partial V_{DD}} \approx \frac{C_{gd}}{C_I}\left[1-\frac{\partial I_o}{\partial V_{DD}}\frac{1}{2g_{m3}}\right]+\frac{C_{gs}}{C_I}\frac{1}{2g_{m1}}\frac{\partial I_o}{\partial V_{DD}}$$

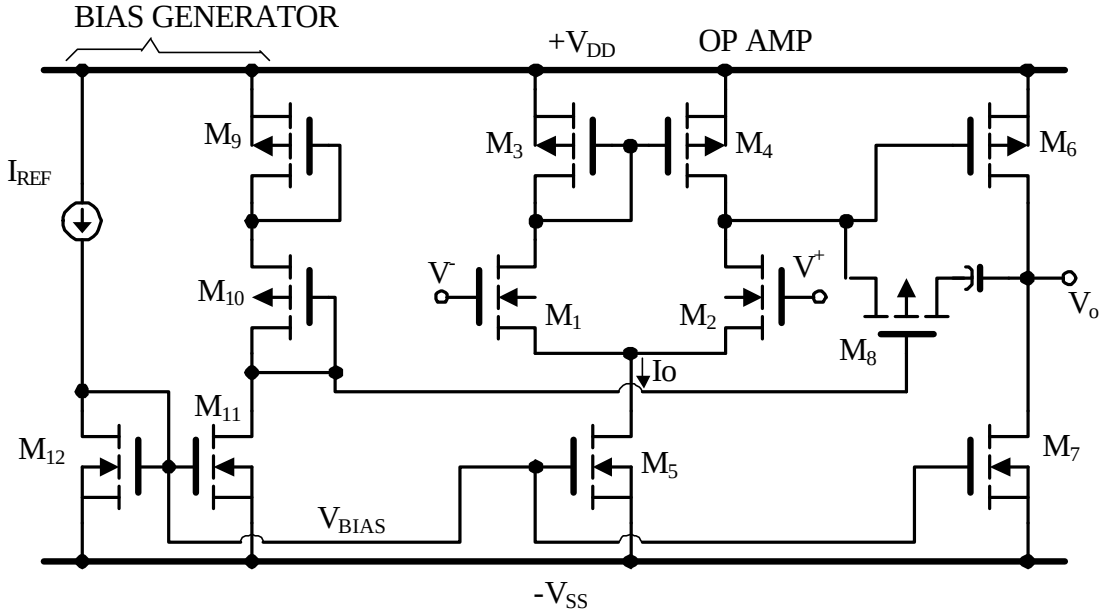
Where I_o represents the input stage bias current.

If I_o is independent of V_{ss} and V_{DD}

and the input devices have no body effect.

==> $\frac{\partial V_{out}}{\partial V_{ss}} \to 0$ $\frac{\partial V_{out}}{\partial V_{DD}} \to -\frac{C_{gd}}{C_I}$

Ref.: IEEE JSSC, vol. SC-15, pp.929-938, Dec. 1980



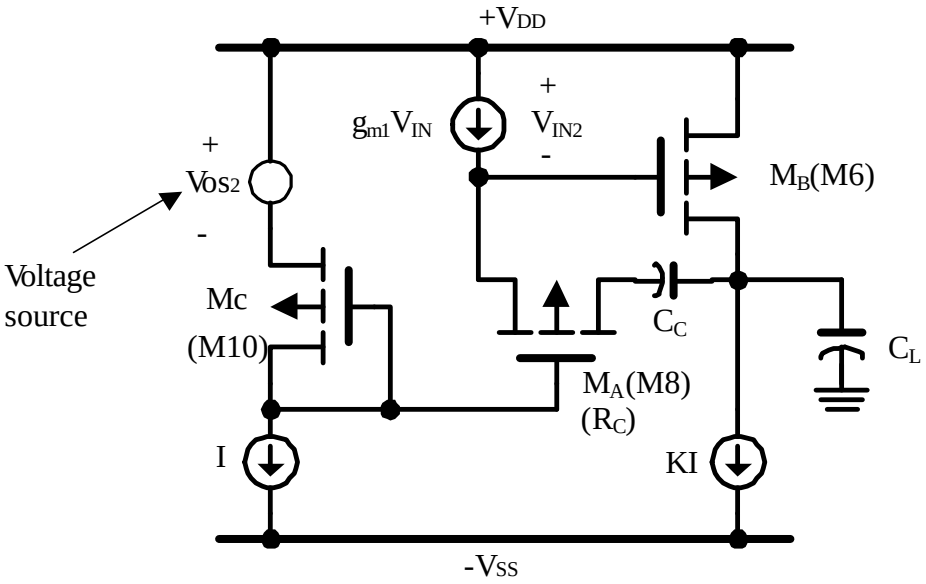
* I_{REF} is generated by using the power supply independent current source.

* V_{BIAS} is nearly independent of V_{DD} and V_{ss}.

*It is better to use separate p-wells for M_1 and M_2 to avoid the body effect.

*Tracking RC compensation

Conceptual circuits :



In the quiescent case ,$Vin_2=V_{OS2}$

$$\text{If } (W/L)_A \approx [(W/L)_B \bullet (W/L)_C \bullet K]^{1/2} \frac{Cc}{Cc+C_L}$$

$$\Rightarrow R_{dsA} \approx \frac{Cc+C_L}{g_{m2}Cc} \approx Rc$$

The requires Rc is $Rc = 1/g_{m2}[1+(C_d+C_L)/Cc] \approx 1/g_{m2}[(Cc+C_L)/C_C]$

Thus LHP zero=LHP pole P2

and P3 becomes the second pole.

The stability considerations,

$$P_3 \geq A_{do}P_1$$

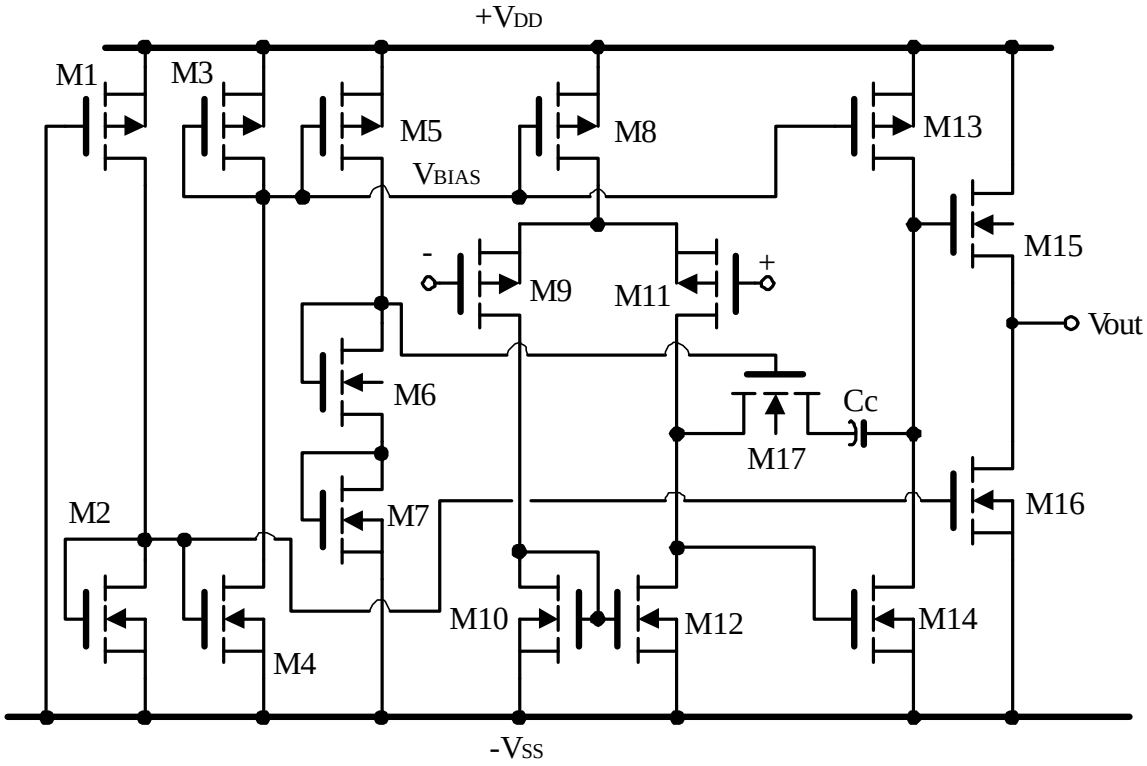
or $$Cc \geq \sqrt{\frac{g_{m1}}{g_{m2}}c_1c_L}$$

allows a smaller gm2 and larger C_L

* $R_{dsA} \approx Rc$ indep of temperature, process , and supply variations.

=>Tracking design to make sure that z=P_2

=>No pole-zero doublet problem!

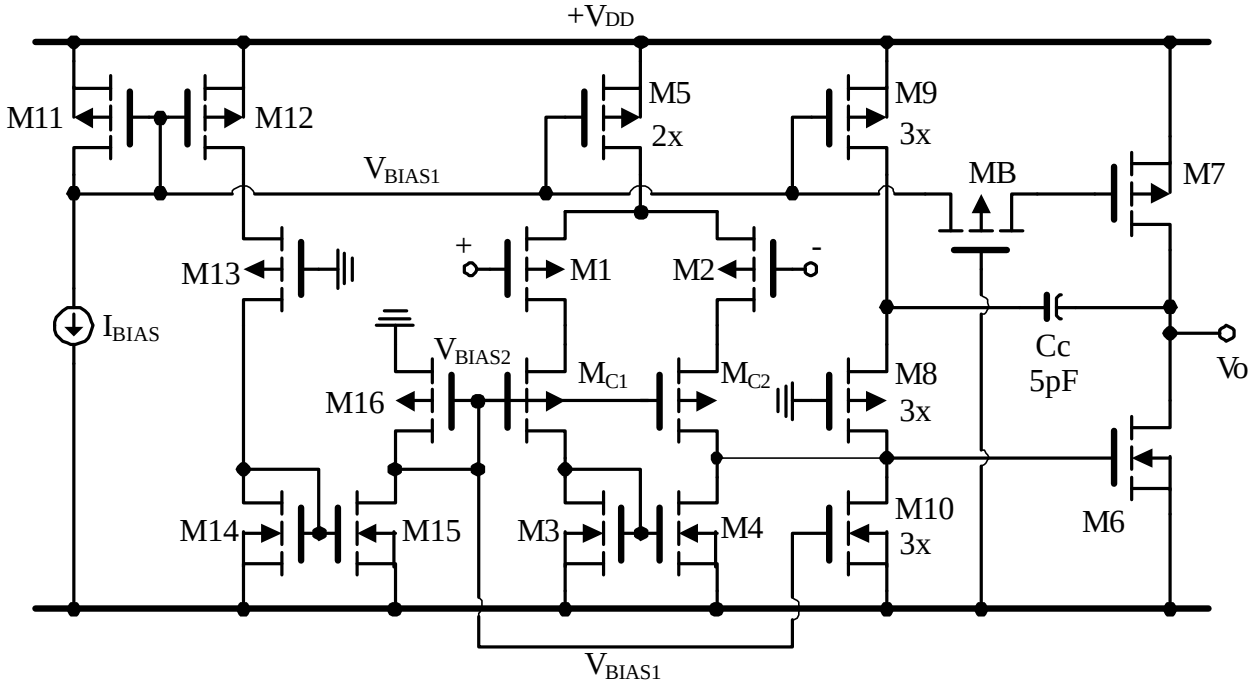


* M17,Cc : Tracking RC compensation.
* M9,M11:Sharing the separate n-well.
* V_{BIAS} is not strictly independent of V_{DD} and V_{SS}.

§8-1.2 Improved frequency compensation technique.

Ref.: IEEE JSSC ,vol.sc-18, pp 629-633, Dec.1983

Grounded gate cascode compensation

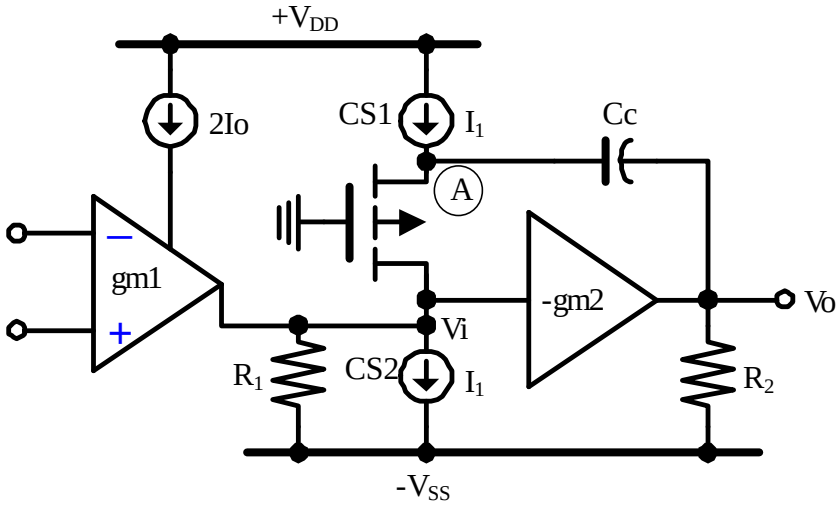


MB,Cgs_7:low pass filter for high frequency noises.

M8,M9,M10:new compensation circuit.

M11~M16:Bias generator.

Conceptual circuits:



Net current in C_C $(C_c \frac{d}{dt} V_o)$ enters the second stage.

The input voltage Vi can' t reach the node Ⓐ

➔ * Better PSRR (∵ no low-freq. zero) , especially PSRR

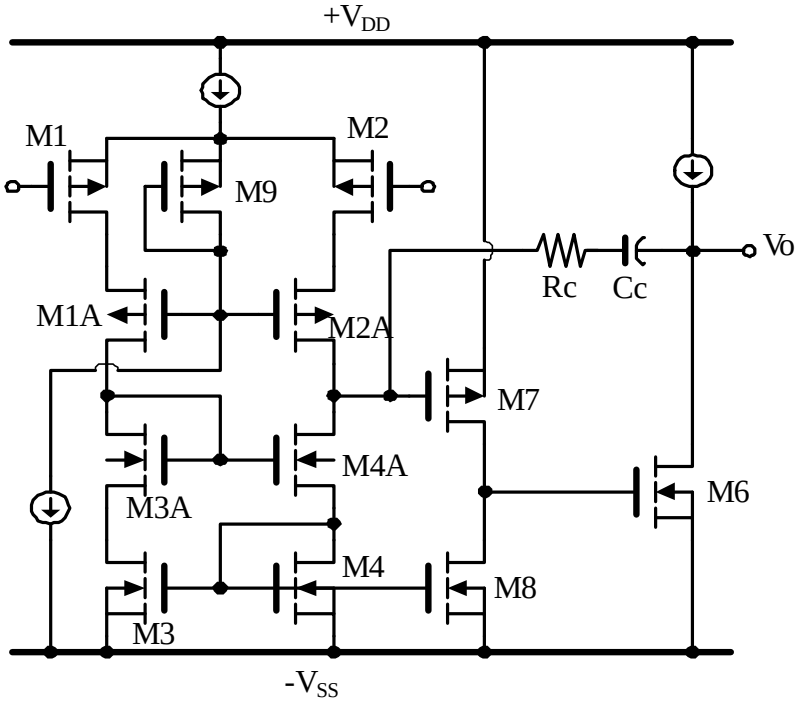
* Allow larger capacitive loads.

* Slight increase in complexity , random offset and noise.

§ 8-1.3 Improved cascode structure

1. To improve gain:

Ref: IEEE JSSC , vol. SC-17, pp. 969-982, Dec. 1982 ☆☆

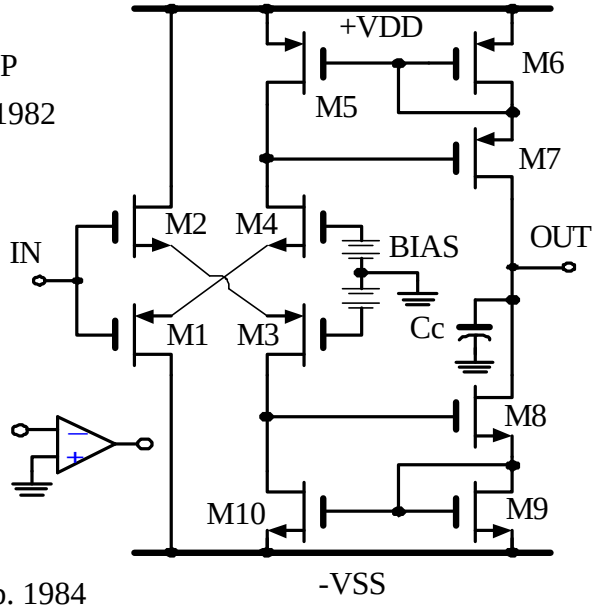


* Substantial reduction in input-stage common-mode range.
* Improved wilson current source is used as the load to improve the balance of the first stage.

2. Single-stage push-pull class AB CMOS OP AMP

Ref: IEEE JSSC , vol.sc-17, pp.969-982, Dec. 1982

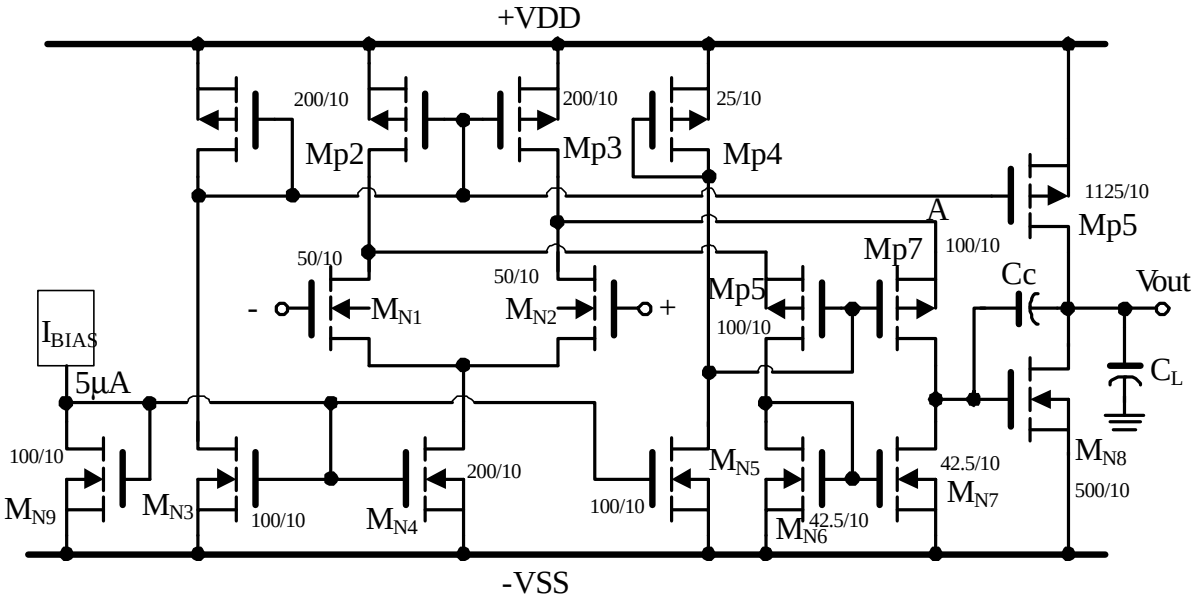
* Inverting mode only. (+ grounded)
* Capable of high current driving and high voltage gain.
* Not a differential-amplifier-based OP AMP.



3. Cascoded CMOS OP AMP with high ac PSRR

Ref: (1) IEEE JSSC , vol. SC-19, pp.55-61, Feb. 1984
(2) IEEE JSSC , vol SC-19, pp. 919-925, Dec. 1984

1) Original version

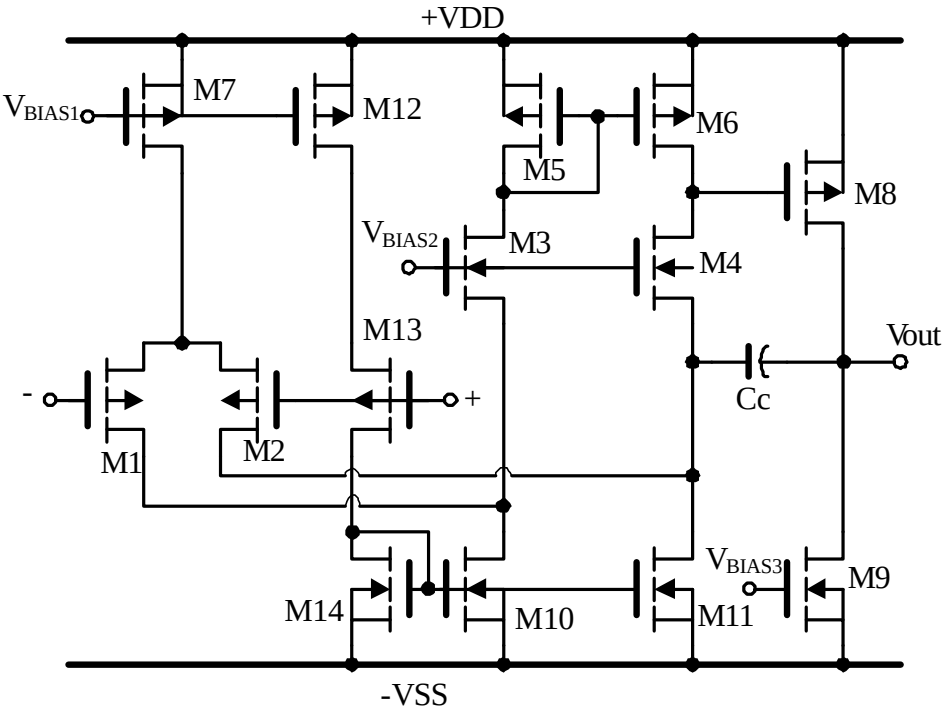


Chrarcteristics:

V_{DD}=V_{SS}=2.5V	
Input offset voltage	5mV
Supply current	100ì A
Output voltage range	-V_{SS}~V_{DD}
Input common mode range	-V_{SS}+1.47V ~ V_{DD}
CMRR @ 1KHz	99dB
Unity-gain frequency	1.0MHz
Slew rate	1.8 V/ì sec

* Better input common-mode range.
* Vic↓ ➔ V_{DSN4}↓ ➔ I_{DSN4}↓ ➔ V_A↑ ➔ M_{N8} is turned on ➔ V_{out}→-V_{SS} voltage spike at V_{out}.
* The possible spike in the settling period.

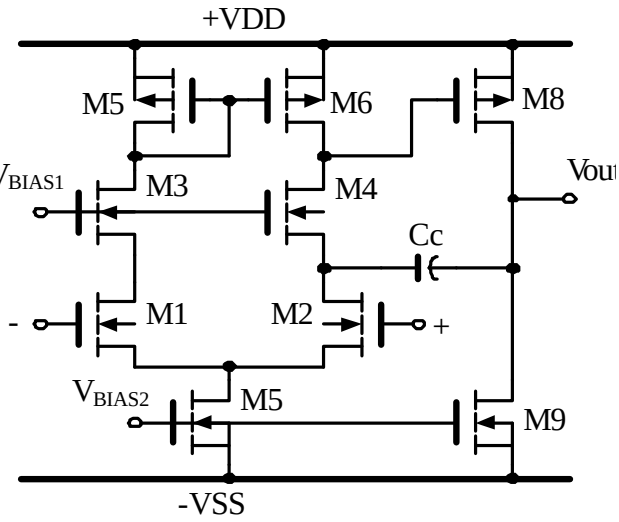
2) Improved version



* M_{12}, M_{13} and M_{14} : Let the drain bias currents of M_{10} and M_{11} follow the change of I_{D7} under positive input common mode voltage.
  ⇒ No voltage spike at V_{out}
  Also serves as CMFB
* Better PSRR and input common-mode range.
* C_c is decoupled from the gate of the driver M_8.

4.Simple cascoded CMOS OP AMP

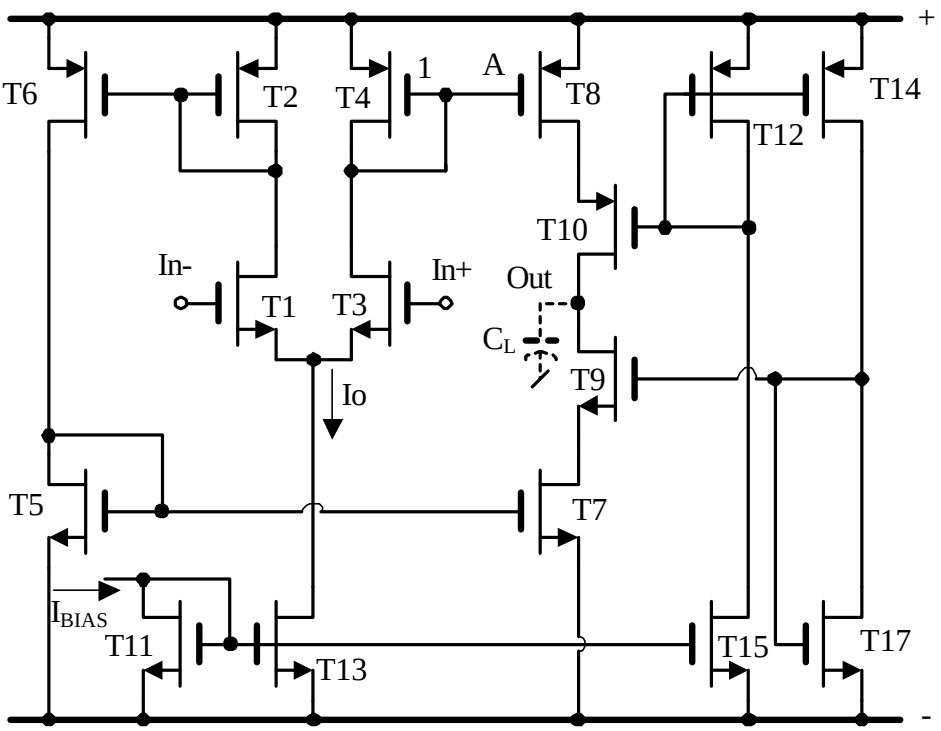
Ref.:IEEE JSSC , vol.SC-19 , pp.919~925 , Dec. 1984



* Good PSRR
* Reduced input common range.
  ⇒ restrict its applications to those which use a virtual ground.

5.Single-stage cascode OTA

Ref.: IEEE JSSC , vol. SC-20 , pp.657~665 , June 1985 ☆☆



T_9, T_{10} : Cascode structure

* Output conductance ↓ without any noise penalty and with only a very small reduction of phase margin.

  ⇒ Gain↑ no any compensation is necessary.

* Maximum output swing↓

§ 8-2 Advanced Design Techniques on High-frequency Non-differential-type CMOS OP AMPs

1. Single-ended push-pull CMOS OP AMP

*Current-gain-based design

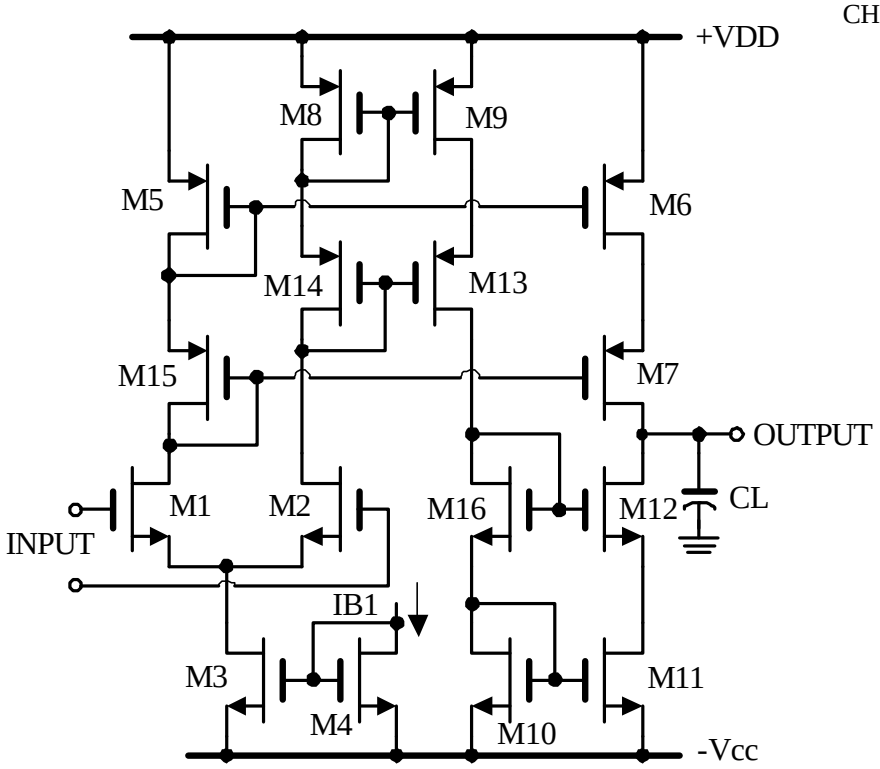


TABLE I

Parameter	Measured Value
DC-Open Circuit Gain	69dB
Unity0Gain Bandwidth	70MHz
Phase Margin	40^o
Slew Rate	$200V / m\text{sec}$
PSRR (DC^+)	68dB
PSRR (DC^-)	66dB
Input Offset Voltage	10mV
CMRR (DC)	62dB
Output Voltage Swing	$1.5V_P$
Output Resistance	$3M\Omega$
Input Referred Noise (@1KHz)	$0.54mV/\sqrt{Hz}$
DC-Power Dissipation	1.1mWatt

$V_{DD} = +3V$; $V_{CC} = -3V$; $I_{B1} = 50mA$; CL=1pF

TABLE II

Bias Current	Unity-Gain Bandwidth	DC-Open Circuit Voltage Gain	DC-Power Dissipation
$25mA$	50MHz	70dB	0.55mW
$50mA$	70MHz	69dB	1.1mW
$100mA$	100MHz	66dB	2.2mW

$V_{DD} = +3V$; $V_{CC} = -3V$; CL=1pF

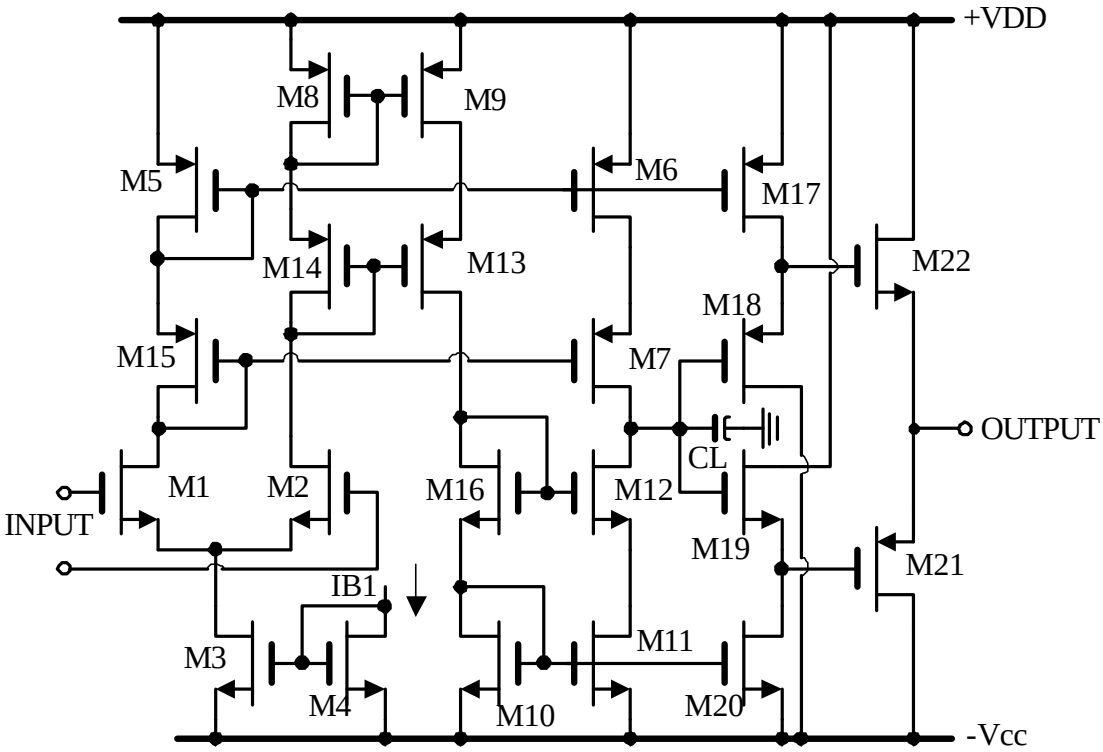
2.Low output resistance CMOS OP AMP

*C_L is a compensation capacitor

*For low-resistance load

*Smaller maximum output voltage swing.

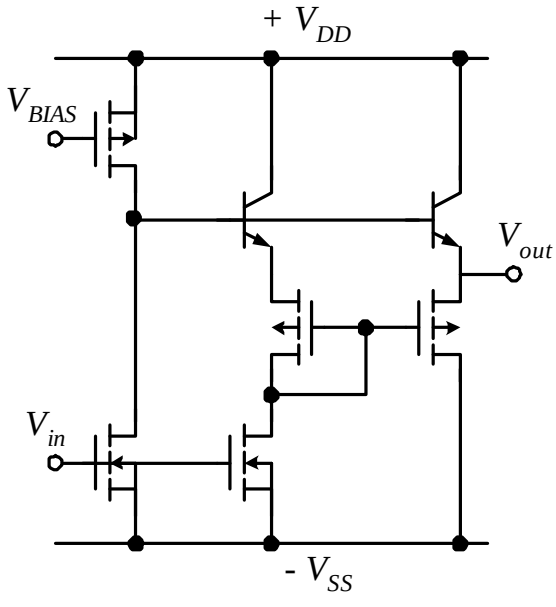
* $I_{B1} = 50mA, C_L = 1pF$, $f_u = 60MHz$



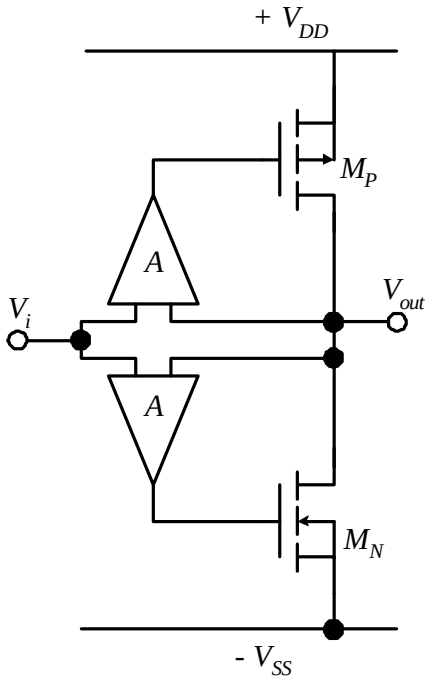
§ 8-3 Advanced Design Techniques on High-drive MOS Power or Buffer OP AMPs

§ 8-3.1 Efficient Output Stages.

A. CMOS output stage using a biplar emitter follower and a low-threshold PMOS source follower.

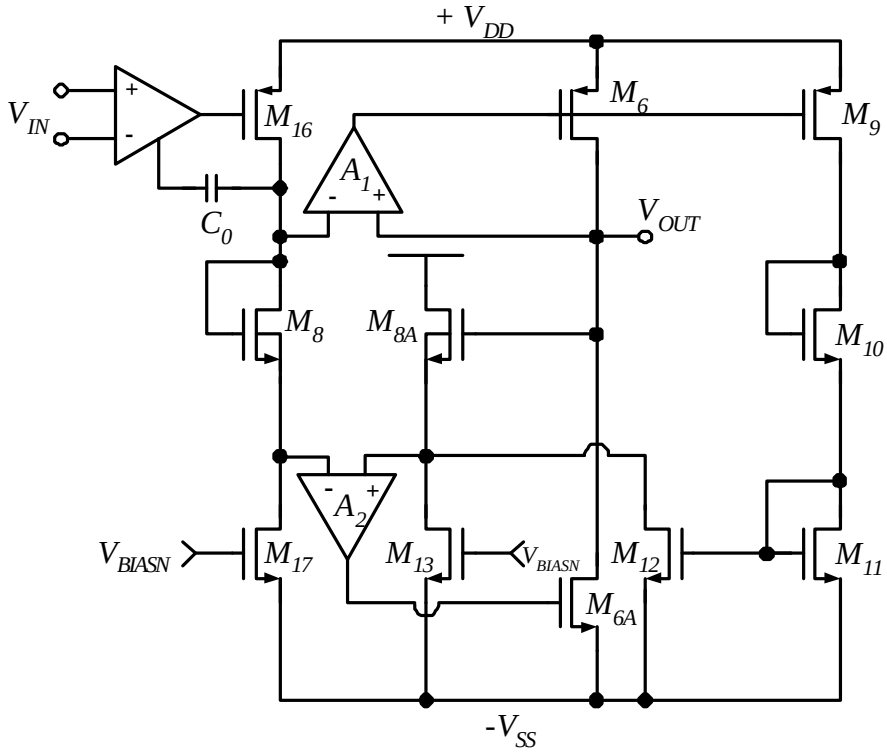


B. Complementary class B output stage using compound devices with common-source output MOS.

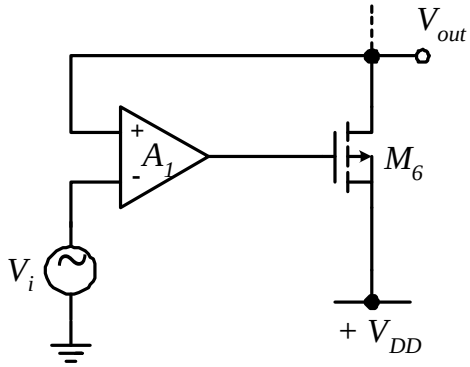


§ 8-3.2 High-drive power or buffer CMOS OP AMPs

1. Large swing CMOS power amplifier (National Semiconductor)



* Noninverting unity gain amplifier



$V_{in} \cong V_{out}$

M_6 provides the negative feedback

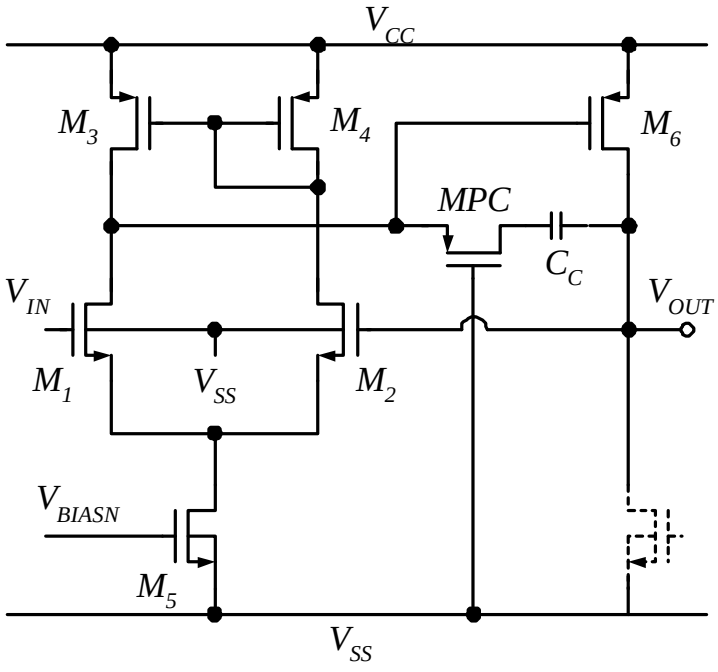
* A_1, M_6 and A_2, M_{6A} form a class AB push-pull output stage.

* Full swing from $+V_{DD}$ to $-V_{SS}$

* $M_9, M_{10}, M_{11},$ and M_{12} form a current feedback to stablize the bias current of M_6 and M_{6A}.

Offset in A_1 ,e.g. $V_{inA1}^- \uparrow \Rightarrow V_{outA1} \downarrow \Rightarrow I_{DM6} \uparrow$ and $I_{DM9} \uparrow \Rightarrow I_{DM11} \uparrow$ and $I_{DM12} \uparrow \Rightarrow V_{GSM8A} \uparrow$ and $V_{inA2}^+ \downarrow \Rightarrow V_{out} \uparrow$, i.e. $V_{inA1}^+ \uparrow \Rightarrow V_{out} \downarrow \Rightarrow V_{inA1}^- \downarrow$ (virtual short between + and -) $\Rightarrow V_{inA2}^- \downarrow$ througt $M_8 \Rightarrow$ All the bias voltage and current are restored to the normal values and the offset is absorbed by M_{8A}.

Since the current feedback is not unity gain ,some current variation in transistors M_6 and M_{6A} still exists.



Large positive common mode range allows M_6 to source large amount of current to the load. (because $V_{in} \cong V_{out}$)

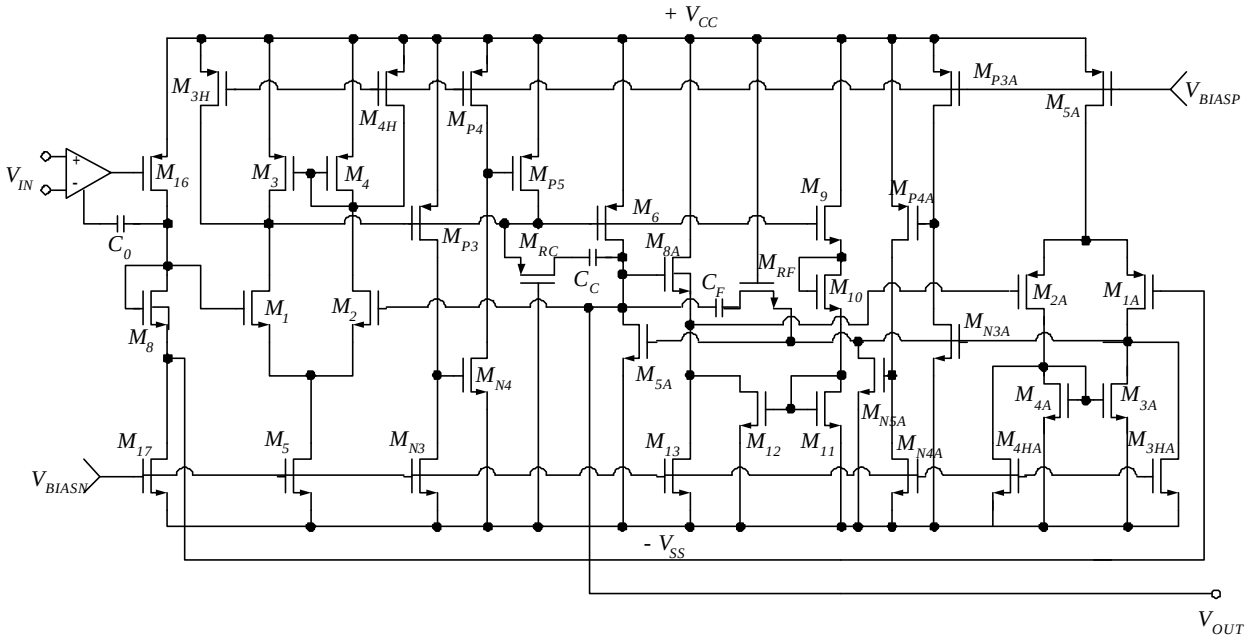
The maximum V_{GS6} which M_1 and M_2 still in the saturation region is

$$V_{GS6\,max} = -(V_{DD} - (V_{IN} - V_{GS1} + V_{DSAT1})) = -(V_{CC} - V_{IN} + V_{TH1})$$

$$\Rightarrow V_{TH1} \uparrow \Rightarrow V_{GS6\,max} \uparrow \Rightarrow I_{DM6} \uparrow$$

(1). Threshold implant to increase V_{THO1}

(2). Negative substrate bias $-V_{SS}$ to increase V_{TH1}



* The input stage is not shown in the diagram.

* M_{16}, M_8, M_{17} form the second stage with C_D the Miller compensation capacitor.

* If $V_{out} \to -V_{SS}, V_{DSM5} \to 0$ and $I_{DSM5} \to 0$.

$\Rightarrow M_1, M_2, M_3$ and M_4 are off

$\Rightarrow M_{3H}$ and M_{4H} are still on to keep $V_{GS6} \cong 0V$.

Otherwise, M_6 will be turned on.

Similarly, M_{3HA} and M_{4HA} turn off M_{6A} in the positive voltage swing

* $M_{P3}, M_{N3}, M_{N4}, M_{P4}$ and M_{P5} are output short-circuit protection circuitry.

Normally, M_{P5} is off.

When $I_{DM6} \cong 60mA$, $I_{DMP3} \uparrow \Rightarrow I_{DMN4} \uparrow \Rightarrow V_{GSMP5} \uparrow$.

$\Rightarrow I_{DM6}$ is limited to approximately 60 mA.

Table I

POWER AMPLIFIER PREFORMANCE

Parameter	Simulation	Measured Results
Power dissipation($\pm 5V$)	7.0mW	5.0mW
A_{vol}	82dB	83dB
F_u	500KHz	420KHz
V_{offset}	0.4mV	1mV
PSRR+(dc)	85dB	86dB
(1KHz)	81dB	80dB
PSRR-(dc)	104dB	106dB
(1KHz)	98dB	98dB
THD V_{IN}=3.3V_p R_L=300Ω	0.03%	0.13%(1KHz)
C_L=1000 pF	0.08%	0.32%(4KHz)
V_{IN}=4.0V_p R_L=15 kΩ	0.05%	0.13%(1KHz)
C_L=200 pF	0.16%	0.20%(4KHz)
$T_{settling}$ (0.1%)	3.0us	<5.0us
Slew rate	0.8V/us	0.6V/us
1/f noise at 1KHz	N/A	130nV/Hz
Broad-band noise	N/A	49nV/Hz
Die area		1500$mils^2$

TABLE II

COMPONENT SIZES (μm, pF)

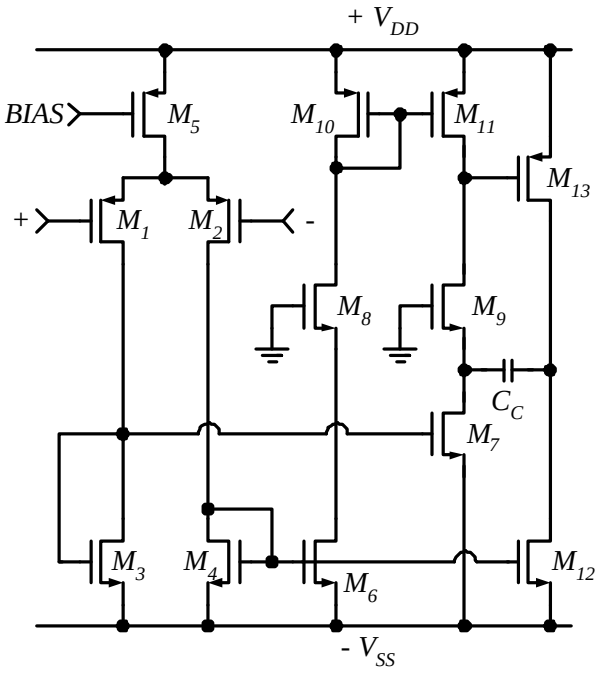
MI6	184/9	M8A	481/6
MI7	66/12	M13	66/12
M8	184/6	M9	27/6
M1,M2	36/10	M10	6/22
M3,M4	194/6	M11	14/6
M3H,M4H	16/12	M12	140/6
M5	145/12	MP3	8/6
M6	2647/6	MN3	244/6
MRC	48/10	MP4	43/12
CC	11.0	MN4	12/6
M1A,M2A	88/12	MP5	6/6
M3A,M4A	196/6	MN3A	6/6
M3HA,M4HA	10/12	MP3A	337/6
M5A	229/12	MN4A	24/12
M6A	2420/6	MP4A	20/12
MRF	25/12	MN5A	6/6
CF	10.0		

Maximum loads : 300Ω and 1000pF to ground.

Ref.:IEEE JSSC , vol.SC-18 , pp.624-629 , Dec.1983

2. High-performance CMOS power amplifier (Siemens AG)

(1). New input stage : 3 gain stages.



* Cc is connected to the source of M_9 to improve PSRR

* Three poles and one zero :

$$Z = \frac{-2g_{m6}g_{m8}g_{m13}}{C_c g_{m6} g_{m13} + C_1 g_{m8} g_{m12}} \qquad \text{LHP.}$$

$$P_1 \cong \frac{-g_{ds10}g_o}{g_{m13}C_c}$$

$$P_2, P_3 \cong \frac{-g_{m8}(C_c + C_O)}{2C_O C_c} \pm j\left[\frac{g_{m8}g_{m13}}{C_O C_1} - \left(\frac{g_{m8}(C_O + C_C)}{2C_O C_c}\right)^2\right]^{1/2}$$

where $g_o \equiv g_{ds12} + g_{ds13}$

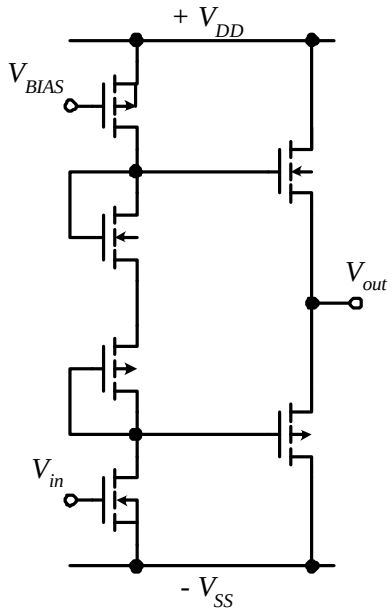
$$C_O = C_L + C_{db12} + C_{db13}$$

$$C_1 = C_{gs13} + C_{db11} + C_{db9} + C_{gd9}$$

Design guidelines for stability :

g_{m8} large , $g_{m13} >> g_{m6}$

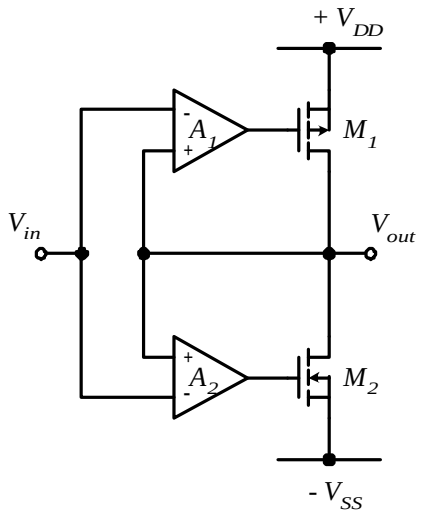
(2). Output stage



Class AB source follower

* One pole and one zero at high frequencies.

* Not full swing

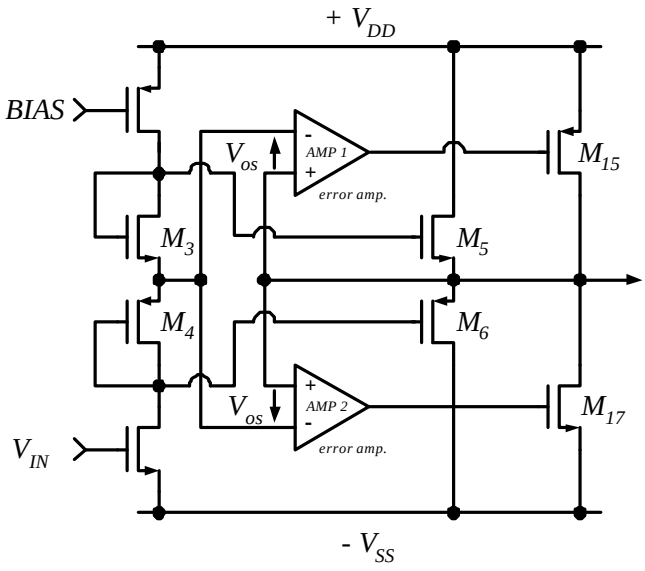


Pseudo source follower

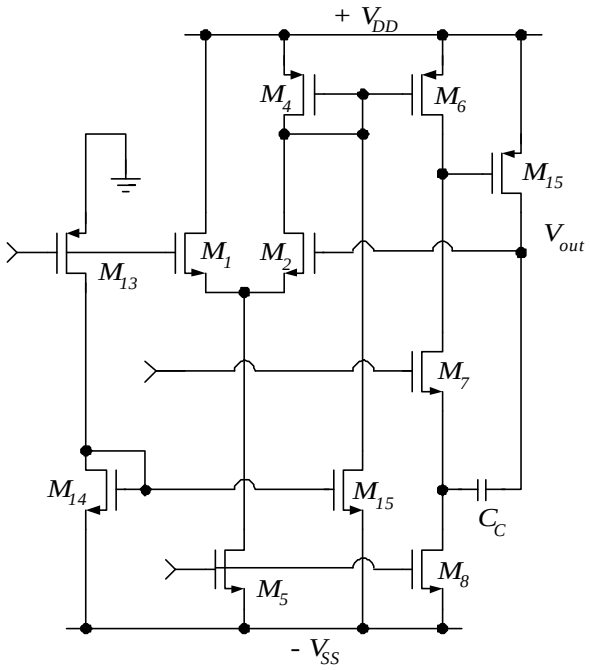
* The quiescent current in M_1 and M_2 will vary widely with variations in Vos1 and Vos2.
* Suitable common-mode range of the two amplifiers A_1 and A_2 are required.
* Large phase shift at high frequencies due to A_1 and A_2 $\Rightarrow$ stability problem.

Combined output stage:

* M_1 and M_2 are turned off in the quiescent state by building a small offset voltage into A_1 and $A_2 \Rightarrow M_3$-M_6 control the output quiescent currents.
* M_2 (M_1) sinks (sources) approximately 95% of the required currents.
* M_1 and M_2 provide a high-frequency feed-forward path.



Still has a smaller swing limited by M_5, M_6 .



* M_{13}, M_{14} and M_{15} form a circuit to turn off M_{15} when $V_{out} < V_{TP13}$ (negative)
* C_c : compensation.
* Three poles and one zeros.

$$Z_1 \approx -\frac{g_{m7} + g_{mbs7}}{C_c + C_{gs7}}$$

$$P_1 \approx \frac{-g_L}{C_L + C_C \dfrac{g_{m15}}{g_{ds6}}}$$

$$P_2, P_3 \approx -\frac{g_{m7}(C_c + C_L)}{2C_cC_L} \pm j\left[\frac{g_{m7}g_{ds6}(C_L + C_c\dfrac{g_{m15}}{g_{ds6}})}{C_cC_LC_1} - \left(\frac{g_{m7}(C_c + C_L)}{2C_cC_L}\right)^2\right]^{\frac{1}{2}}$$ where

$$C_1 = C_{gs9} + C_{db6} + C_{db7} + C_{gd7}$$

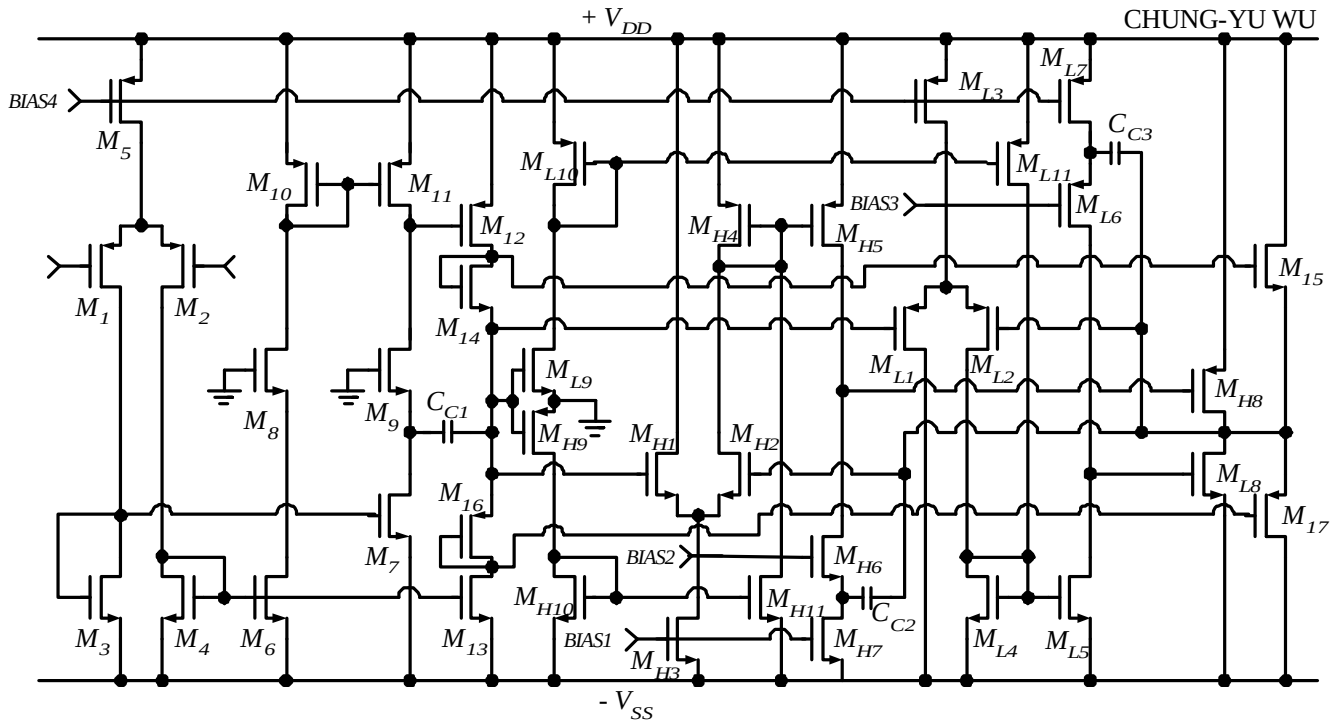


TABLE I Component Sizes

M1	400/15	MH1	48/10	ML1	48/6
M2	400/15	MH2	50/10	ML2	50/6
M3	150/10	MH3	500/15	ML3	300/15
M4	150/10	MH4	300/6	ML4	150/5
M5	100/15	MH5	300/6	ML5	100/5
M6	150/10	MH6	200/5	ML6	300/6
M7	150/10	MH7	250/15	ML7	100/15
M8	300/5	MH8	700/6	ML8	400/5
M9	300/5	MH9	15/6	ML9	5/5
M10	300/10	MH10	10/15	ML10	5/15
M11	300/10	MH11	20/15	ML11	15/15
M12	1200/10	Cc1	20pf		
M13	600/10	Cc2	4pf		
M14	200/5	Cc3	4pf		
M15	200/5				
M16	600/6				
M17	600/6				

TABLE II

POWER AMPLIFIER PERFORMANCE SUMMARY

(First Revision)

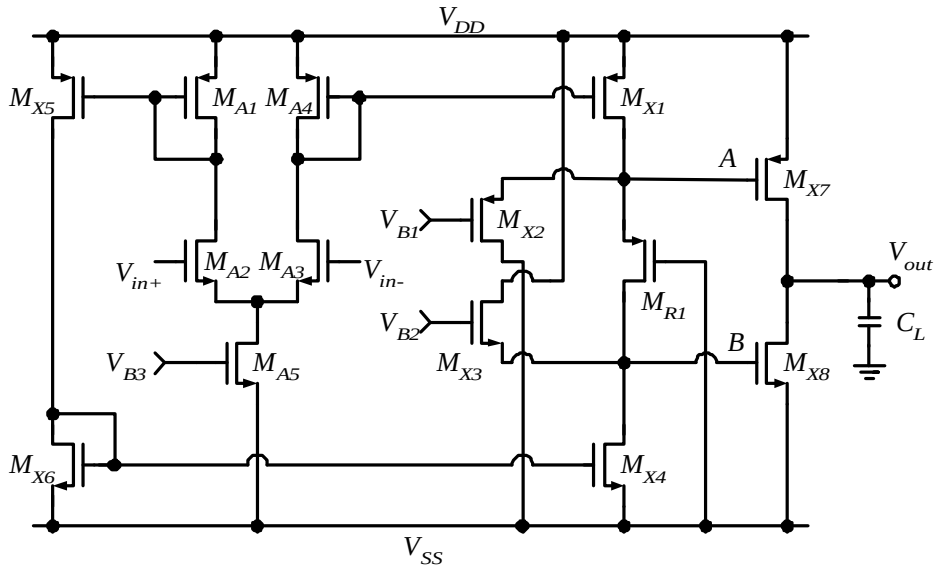
parameter	**Measured Results**
Supplies	±5V
Open-Loop Gain	93dB
Bandwidth	1.2MHz
Power Dissipation $\bar{x}$	12.7 mW
ó	1.76mW
Output Swing (R_L=200Ù)	±3.1V
PSRR+ at DC	93dB
1 kHz	91dB
10 kHz	76dB
100 kHz	60dB
PSRR- at DC	102dB
1 kHz	89dB
10 kHz	75dB
100 kHz	53dB
Slew Rate	1.5V/î s
Input Common Mode Range	+3.3V
	-5.5V
Die Area (5î m CMOS)	1000 $mils^2$
Harmonic Distortion (3 kHz) V_{in}=3 V_p R_L=200Ù	
HD2	-73dB
HD3	-78dB

Maximum Loads : 1000pF and 200Ùto ground.

Ref.: IEEE JSSC , vol. sc-20, pp.1200-1205, Dec. 1985.

3. Efficient Unity-gain CMOS buffer for driving large C_L.

High-drive OTA buffer



Bias stage

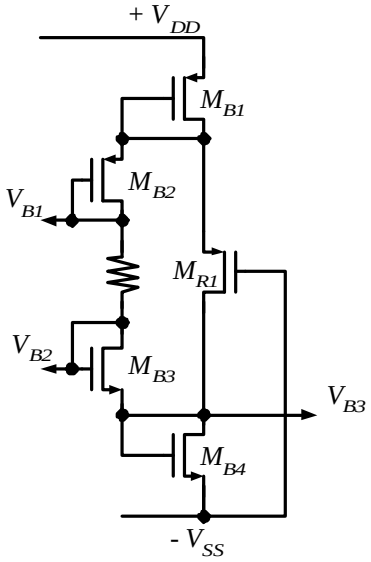


TABLE I

TRANSISTORS' DIMENSIONS

TRANSISTOR	W (μm)	L (μm)
MX1, MX5	225	3
MX2	75	3
MX3	30	3
MX4, MX6	90	3
MR1	6	21
MA1, MA4	45	3
MA2, MA3	450	3
MA5	36	3
MX7	600	3
MX8	240	3

* M_{R1} has a low W/L and is operated in the linear region

$\Rightarrow$ like a linear resistor.

* M_{X2} and M_{X3}

Quiescent operation:

✧ M_{X2} and M_{X3} are on.

$\Rightarrow$ Keep V_{GSMX7} and V_{GSMX8} low to reduce dc power.

$\Rightarrow$ Provide a low-impedance level at node A and B.

The low-order poles created by the Miller cap. of M_{X7} and M_{X8} can be avoid

* If $V_{in} << 0$

  M_{X3}-M_{X6} are turned off and M_{X1} and M_{X2} are on

  $\Rightarrow$ Node A has a high voltage $\Rightarrow$ M_{X7} off.

  $V_B = V_A$ because of $M_{R1} \Rightarrow M_{X8}$ on.

* In the bias circuit, $M_{R2} \leftrightarrow M_{R1}$, $M_{B1} \leftrightarrow M_{X1}$, $M_{B2} \leftrightarrow M_{X2}$, $M_{B3} \leftrightarrow M_{X3}$, $M_{B4} \leftrightarrow M_{X4}$.

  In the quiescent case, $V_{GSMX1} \approx V_{GSMX7}$ and $V_{GSMX4} \approx V_{GSMX8}$

  $\Rightarrow$ The current in M_{B1} and M_{B4} controls that in M_{X1} and M_{X4} and M_{X7} and M_{X8}.

* R_{BIAS} controls the current through M_{B2} and M_{B3}.

  $\Rightarrow$ i.e. the current through M_{X2} and M_{X3}.

Characteristics:

3 μm CMOS area: 100mils^2.

$C_L \geq 100$pF and $R_L \geq 10$ kΩ : stable.

C_L=5000pF $\Rightarrow$ f ≈ 100kHz.

TABLE II
BUFFER' S PERFORMANCE

PARAMETER	MEASURED VALUE	SPICE
Supply Voltage	± 2.5 V	± 2.5 V
Supply Current	285 μA	270 μA
Voffset	< 10 mV	5 mV
Voltage Gain	+ 1.00 V/V	+ 1.00 V/V
F_{3dB} (C_L=100pF)	6 MHz	8 MHz
Gain Peaking	0.4 dB	0
R_{oCL}	330 Ω	270 Ω
CMRR	80 dB	84 dB
Input CM Range	± 1.8 V	± 1.7 V
SR (CL=5nF)	± 0.9 V/μs	± 1.0 V/μs
$T_{settling}$ (to 1%)	3.9 μs	4 μs

Input Noise Density F = 1 kHz	270 $V/\sqrt{H_Z}$	NA
F = 50 kHz	70 $V/\sqrt{H_Z}$	NA

Ref.: IEEE JSSC, vol. sc-21, pp.464-469, June 1986.

§ 8-4 Advanced Design Techniques on Fully differential type CMOS OP AMPs

1. Low-noise chopper-stabilized OP AMP

Techniques for the reduction of 1/f noise:

1) Use large device geometries.

Possibly too large chip area.

2) Use buried channel devices

Not a standard technology.

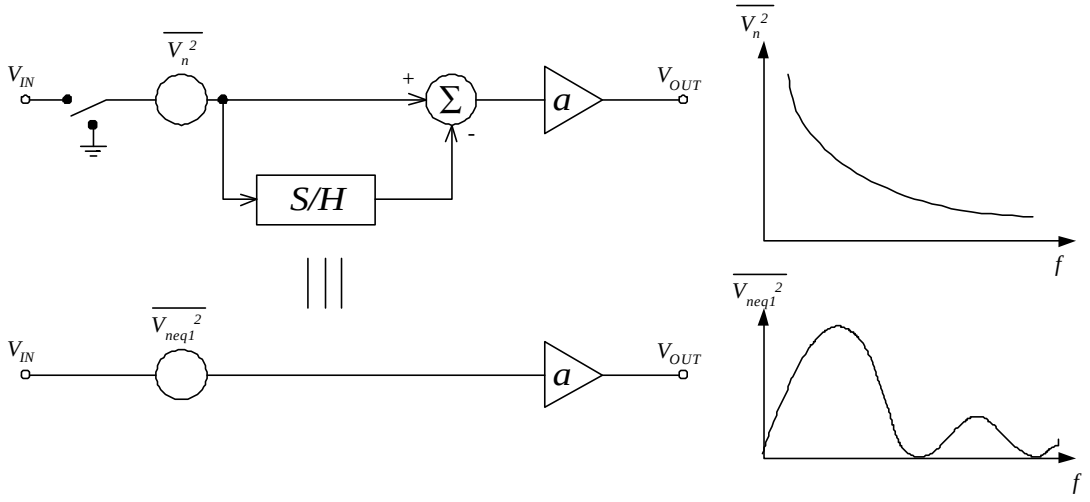
3) Transform the noise to a higher frequency range

So that it does not contarninate the signal.

a. The correlated double sampling (CDS) method

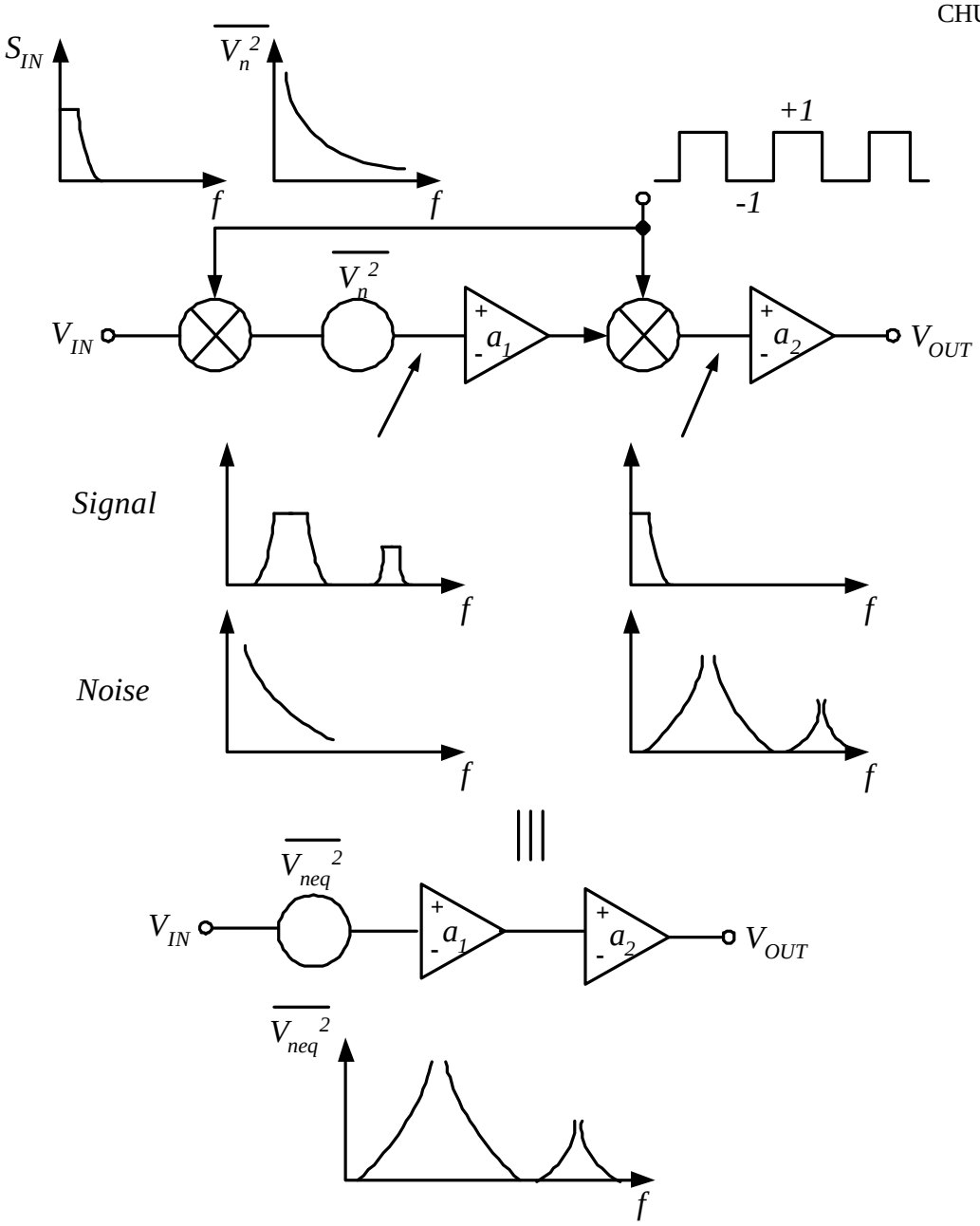
b. The chopper stabilization method

a. CDS method



⇒ Noise reduction

b. Chopper stabilization method



* If the chopper frequency is much higher than the signal bandwidth, the 1/f noise in the signal band will be greatly reduced.

Example: Fully differential class AB chopper stabilized OP AMP with DCMFB circuit.

Major advantage of fully differential OP AMPs:

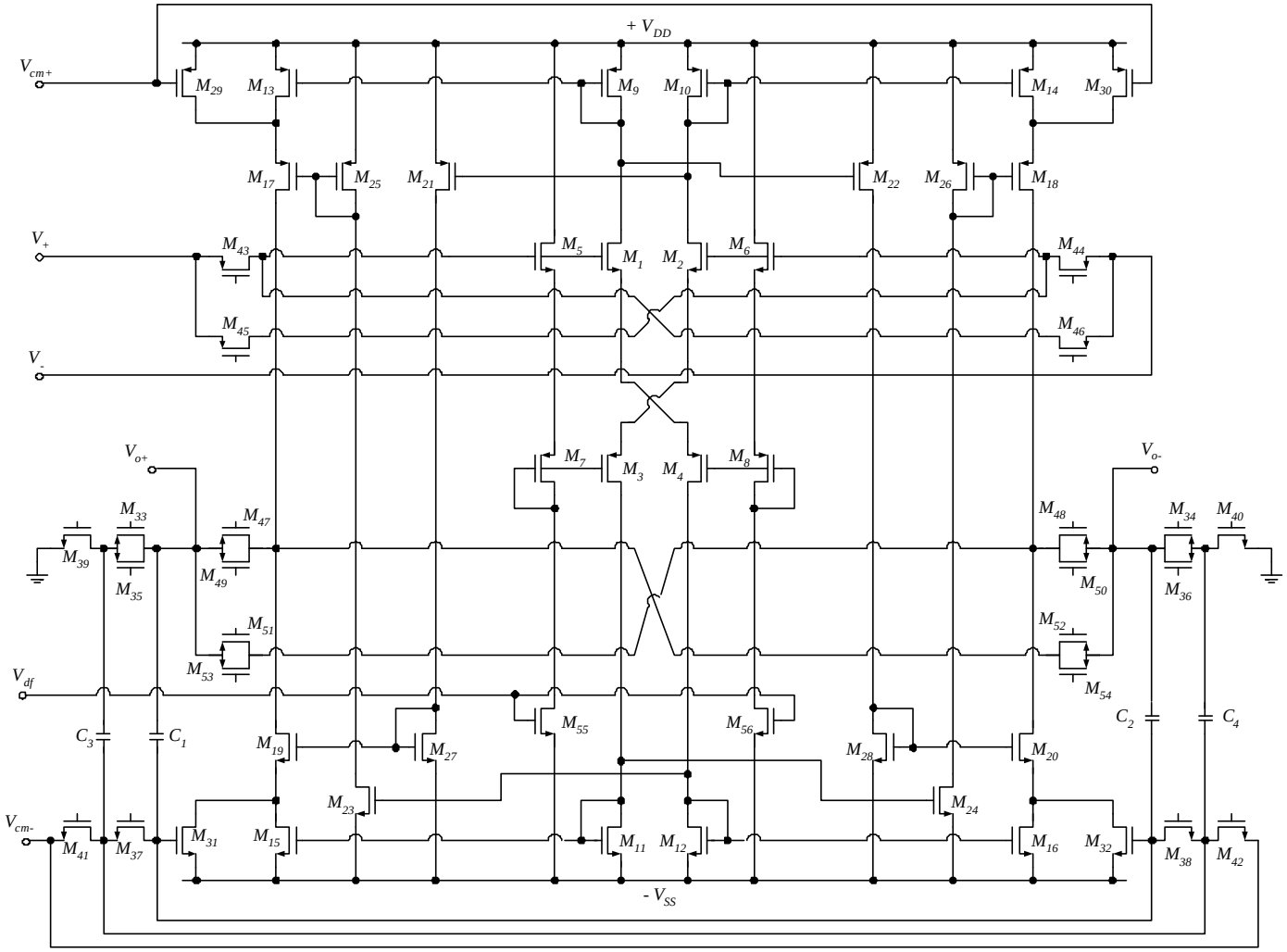
1. Improvement of PSRR
2. Improvement of dynamic range
3. double the output swing
4. Reduction on the sensitivity to clock and supply noise.

Disadvantage:

1. Larger area, mainly due to interconnection

2. Additional design complexity

3. Increase power dissipation.



M43-M46, M47-M54: the input chopper and the output chopper.

M29-M42, C1-C4 : DCMFB circuit

Device	W(um)	L(um)	Device	W(um)	L(um)
M1	25	3	M19	7	3.5
M2	25	3	M20	7	3.5
M3	25	3	M21	17.5	3.5
M4	25	3	M22	17.5	3.5
M5	25	3	M23	7	3.5
M6	25	3	M24	7	3.5

M7	25	3	M25	3.5	3.5
M8	25	3	M26	3.5	3.5

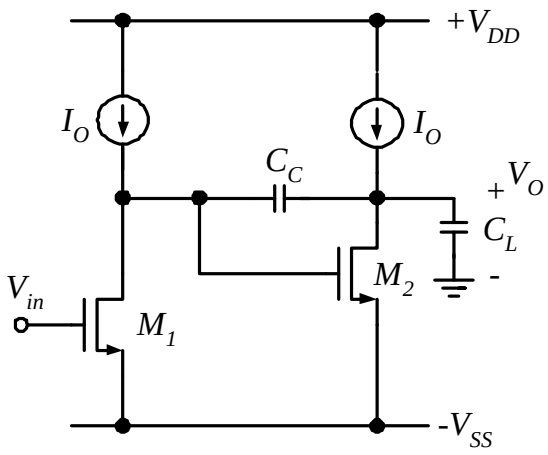
M9	10	3.5	M27	3	7
M10	10	3.5	M28	3	7
M11	4	3.5	M29	12	3.5
M12	4	3.5	M30	12	3.5
M13	17.5	3.5	M31	16	3.5
M14	17.5	3.5	M32	18	3.5
M15	7	3.5	M33-M34	7	3
M16	7	3.5	M55	7	3
M17	17.5	3.5	M56	7	3
M18	17.5	3.5			

Ref: IEEE JSSC vol.sc-21, pp.57-64 Feb.1986

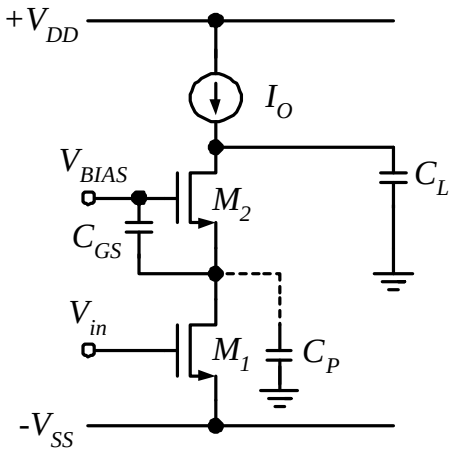
2. Fully differential folded cascode amplifier(National Semiconductor)

For internal OP AMPs, high output impedance is O.K.

$\Rightarrow$ simple 2-stage or single-stage OP AMP.



TWO-STAGE



SINGLE-STAGE

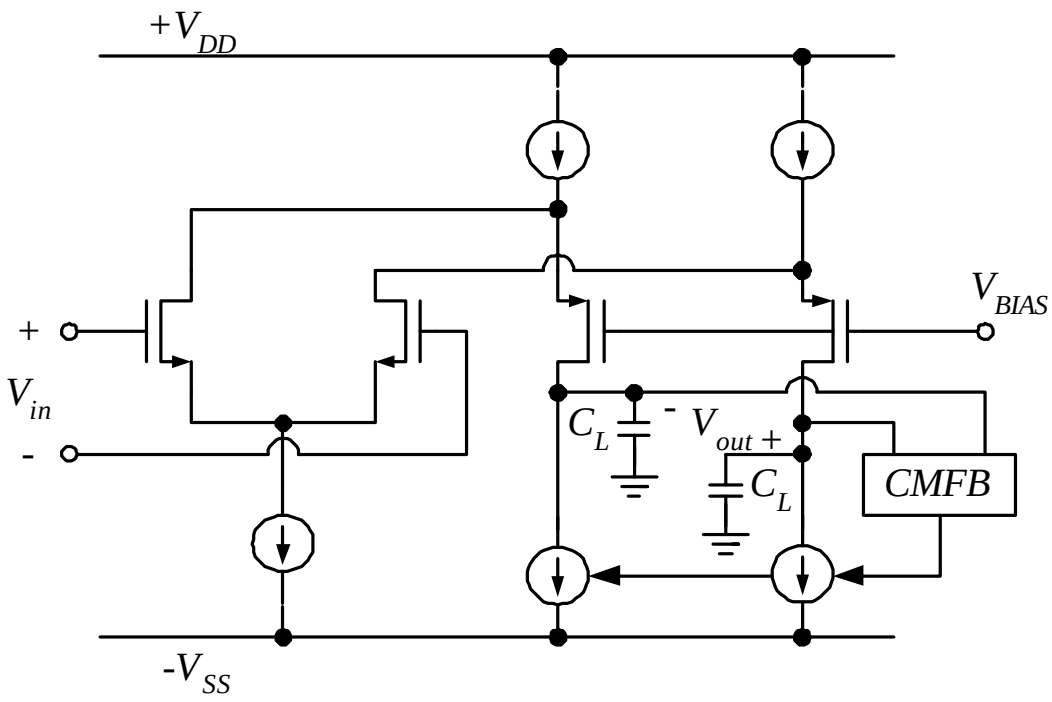
CASCODE

DOMINANT AND NONDOMINANT POLE LOCATIONS
FOR THE TWO-AND SINGLE-STAGE AMPLIFIERS

	Dominant pole location	Nondominant pole location
Two-stage amplifier	$\frac{1}{r_o C_c g_m r_o}$	$\frac{g_m}{C_L}$
One-stage amplifier	$\frac{1}{r_o C_L g_m r_o}$	$\frac{g_m}{C_p}$

In general, the higher the 2nd pole frequency, the faster the settling response.

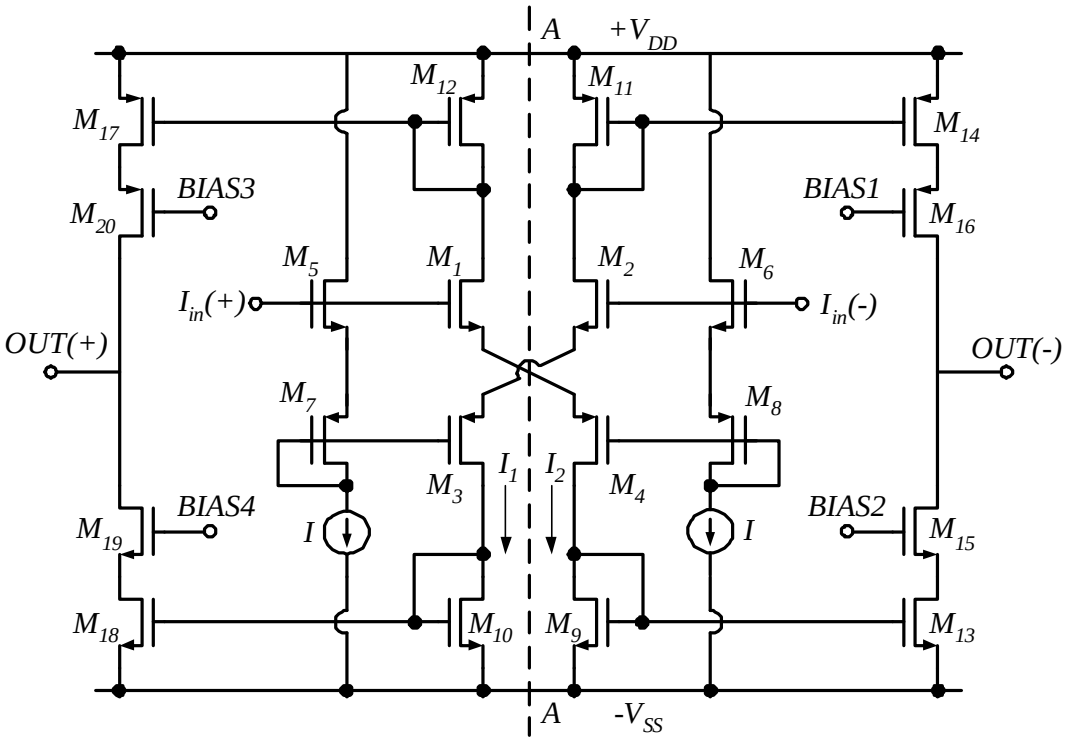
$\Rightarrow$ Single-stage cascode amp. has a faster settling behavior.

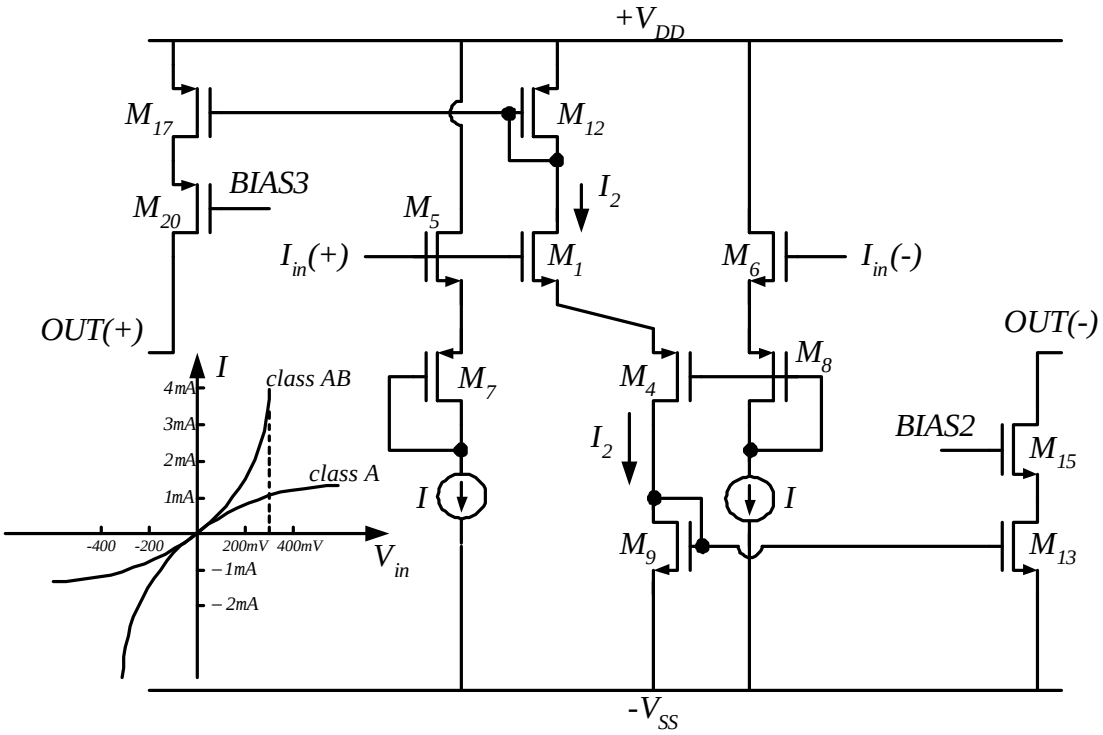


CMFB: Common-mode feedback circuitry

3. High-performance micropower fully differential OP AMP.

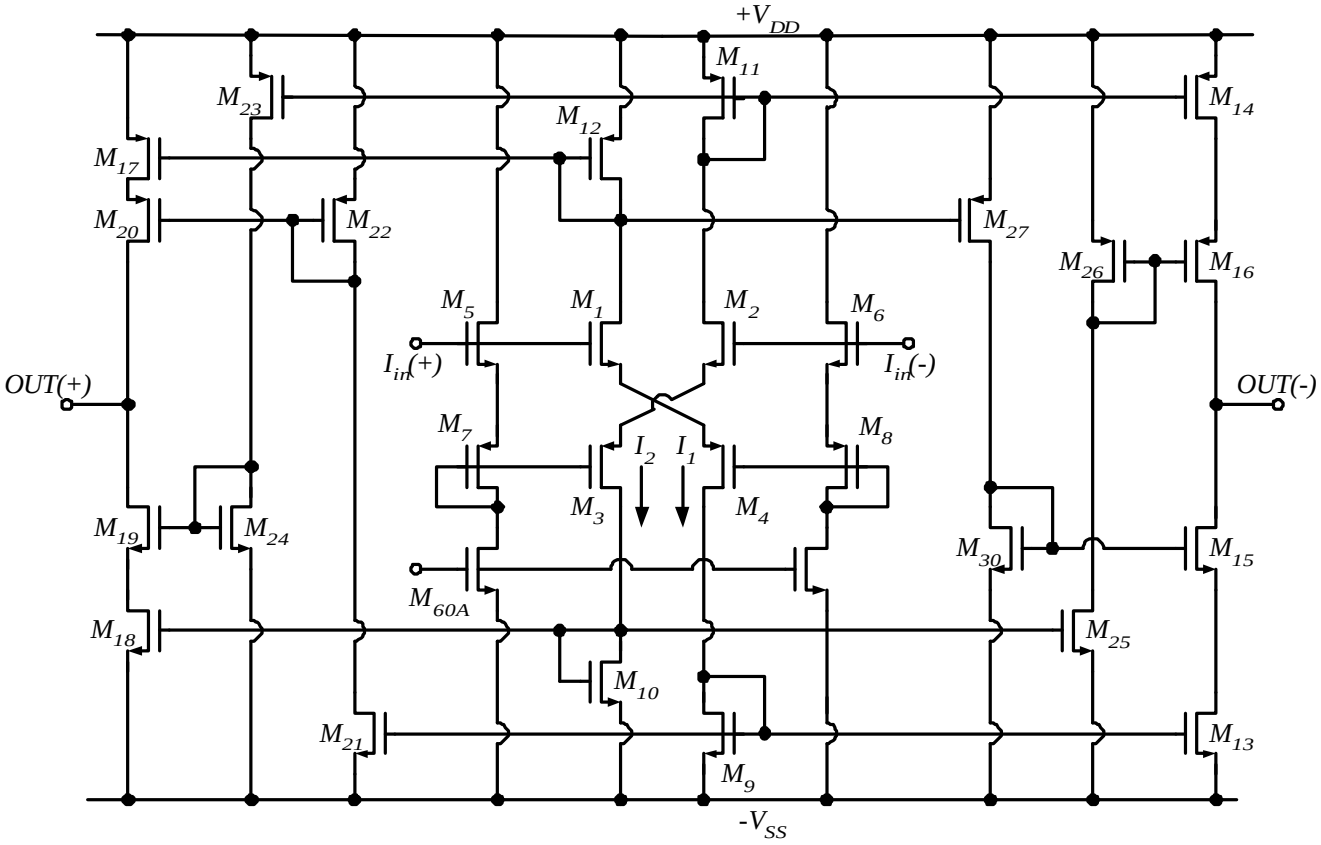
Simplified schematic of the class AB amplifier:



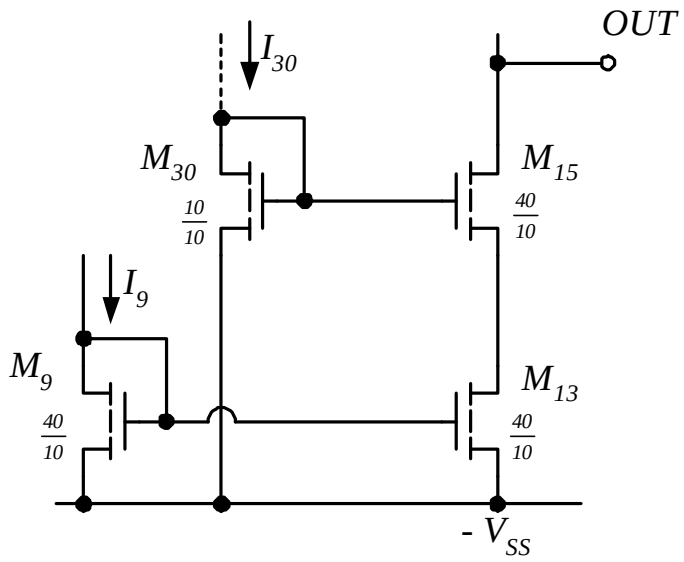


Active portion of the amplifier for a positive input signal.

Detailed schematic of the entire amplifier without CMFB:



* NMOS dynamically biased current mirror:



If $I_9 = I_{30}$, $V_{GS9} = V_{GS13} = V_{GS15}$

$$V_{DS13} = V_{GS30} - V_{GS9}$$

Set $V_{DG13} = -V_{TH} \Rightarrow V_{GS30} = 2V_{GS9} - V_{TH}$

Design $(\frac{W}{L})_{30}$, such that $V_{GS30} = 2V_{GS9} - V_{TH}$

$\Rightarrow$ M_{13} is always sat. at the edge of the linear region.

$\Rightarrow$ Output swing$\uparrow$

* Dynamic CMFB is used.

AMPLIFIER DEVICE SIZES

DEVICE	Z(μ m)	L(μ m)
M1	180	6
M2	180	6
M3	140	6
M4	140	6
M5	150	6
M6	150	6
M7	200	6
M8	200	6
M9	22	10
M10	22	10

M11	29	7
M12	29	7
M13	22	10
M14	29	7
M15	22	6
M16	29	6
M17	29	7
M18	22	10
M19	22	6
M20	29	6
M21	20	9
M22	6	12
M23	28	6
M24	6	14
M25	20	9
M26	6	12
M27	28	6
M30	6	14

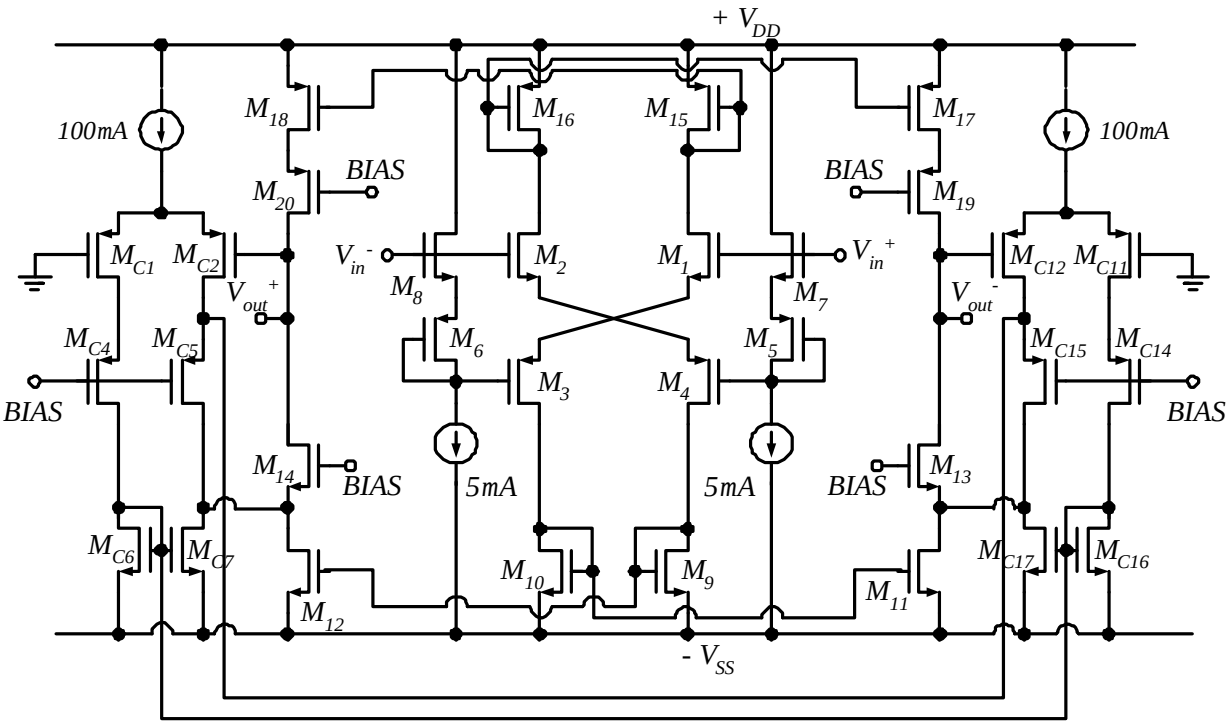
AMPLIFIER SPECIFICATIONS

CORE AMPLIFIER SPECIFICATIONS (0-5 Volts Supply) 100 μW Quiescent Power Dissipation	
DIFFERENTIAL GAIN	>10.000★
UNITY GAIN FREQUENCY	2 MHz★
NOISE	140 nV/$\sqrt{Hz}$ 1KHz 50 nV/$\sqrt{Hz}$ white
OUTPUT SWING	0.5 Volts from Supply★
AREA	300 $mils^2$

★inferred from filter measurement

Ref: IEEE JSSC, vol. SC-20, pp.1122-1132, Dec. 1985

4. Fully differential class AB OP AMP with CMFB circuit



Characteristics:

Technology	: 5um, P-well CMOS, double-poly cap.		
Open loop gian	: 1180	unity-gain freq	: 10Mhez
CMRR	: 61db	power consumption	: 2.3mw
Area	: 290 mils^2	power supply	: ± 5*V*

Ref: IEEE JSSC ,vol.sc-20 , pp.1103-1112 , Ddec,1985

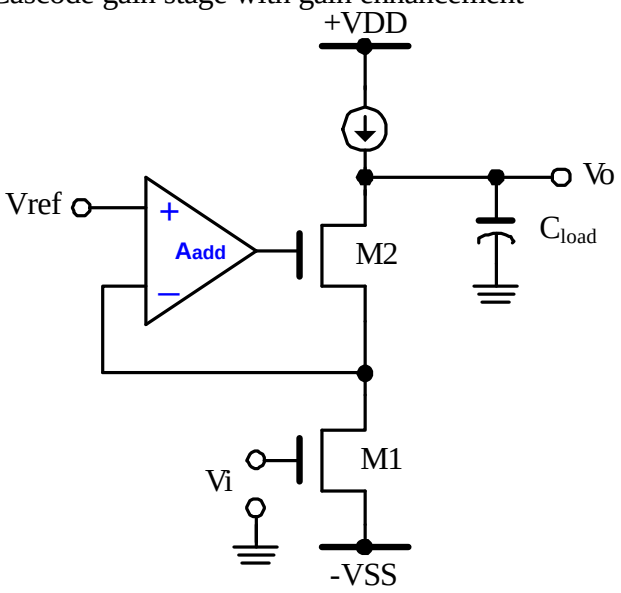
§ 8-5 Recent Design Examples of CMOS OP AMPs

§ 8-5.1 Fast-settling CMOS OP AMP for SC Circuit with 90-dB DC Gain

Reference : IEEE JSSC, vol.25, no.6, pp.1379-1384, Dec 1990.

1.Gain boosting

1) Cascode gain stage with gain enhancement

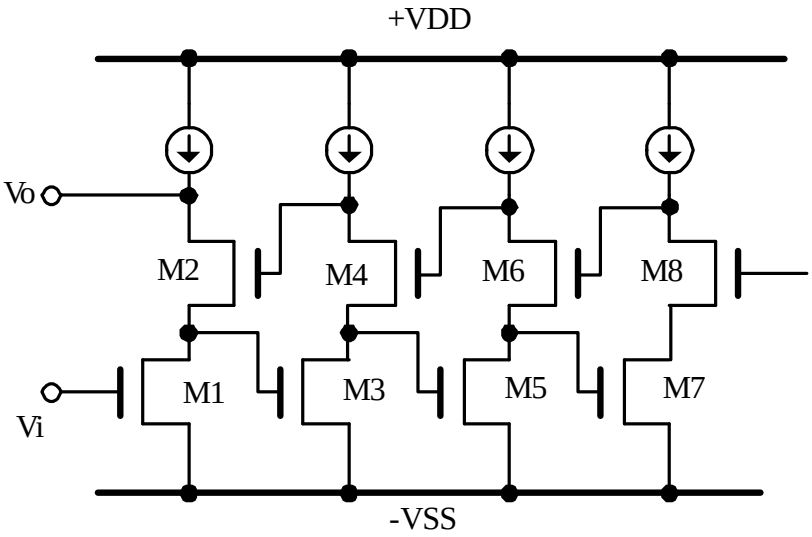


$$R_{out} = [g_{m2} r_{o2} (A_{add} + 1) + 1] r_{o1} + r_{o2}$$

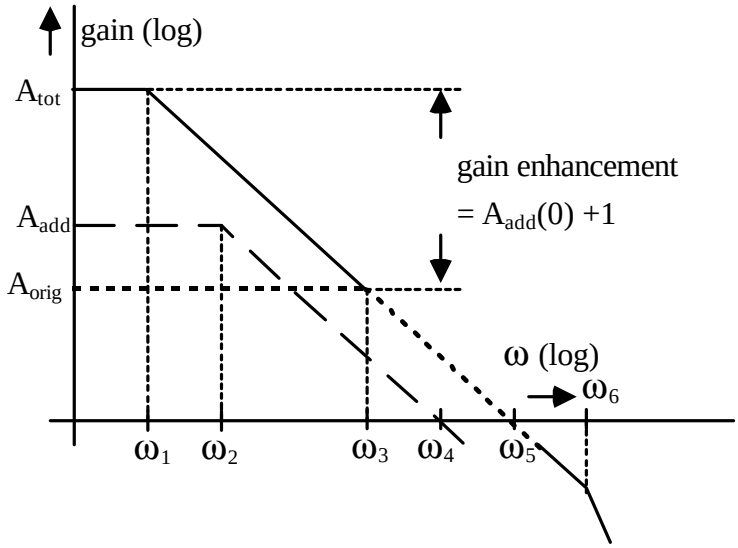
$$A_{tot} = g_{m1} r_{o1} [g_{m2} r_{o2} (A_{add} + 1) + 1]$$

$$A_{orig} = g_{m1} g_{m2} r_{o1} r_{o2}$$

2) Repetitive implementation of gain enhancement



2.High-frequency behavior



w_3 : Upper 3-dB frequency of A_{orig}

w_5 : Unity-gain frequency of A_{tot}

w_2 : Upper 3-dB frequency of A_{add}

w_4 : Unity-gain frequency of A_{add}

w_1 : Upper 3-dB frequency of A_{tot}

w_5 : Unity-gain frequency of A_{orig}

We want $\omega_5\big|_{Aorig} = \omega_5\big|_{Atot}$

$\omega_2 > \omega_1$ => The bandwidth is determined by ω_1, i.e. R_{out} and C_{load}.

=> $\omega_4 > \omega_3$

But $\omega_4 < \omega_5$ for easy design of A_{add}.

A_{add} and M2 forms a close loop with the dominant pole of ω_2 and the second pole at the source of M2, i.e. ω_6

The stability consideration requires $\omega_4 < \omega_6$

=>The safe range of ω_4 is

$$\omega_3 < \omega_4 < \omega_6$$

* The repetitive usage of the gain-enhancement techniques yields a decoupling of the op-amp gain and unity-gain frequency fu. That is:gain↑ without fu↓.

3.Settling behavior

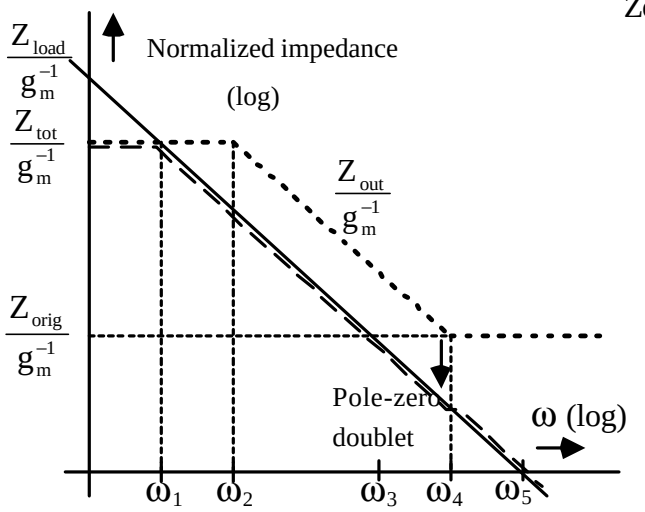
1. Total output impedance Ztot

Ztot= $Z_{load} // Z_{out}$

Z_{load}: impedance of C_{load}

Zout: output impedance of the amplifier

Zout ≅ Zorig (Add+1)



ω_2 : Upper-3dB freq. Of A_{add}

➔the same for Z_{out}

ω_4 : Unity-gain freq. Of A_{add}

For $\omega > \omega_4$, $A_{add} < 1$➔ $Z_{out} \rightarrow Z_{orig}$

➔A zero is formed at ω_4 for Z_{out}

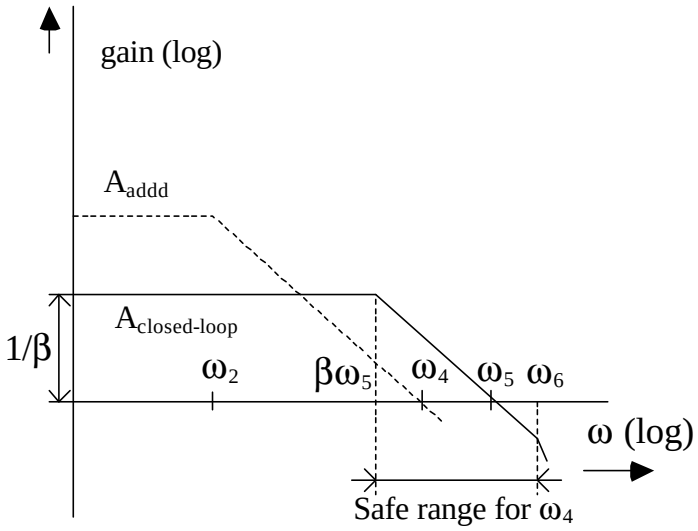
$Z_{total} = Z_{load} \parallel Z_{out}$ ➔A pole-zero doublet is formed around ω_4

➔The same doublet of A_{total}

3. Design technique for fast settling

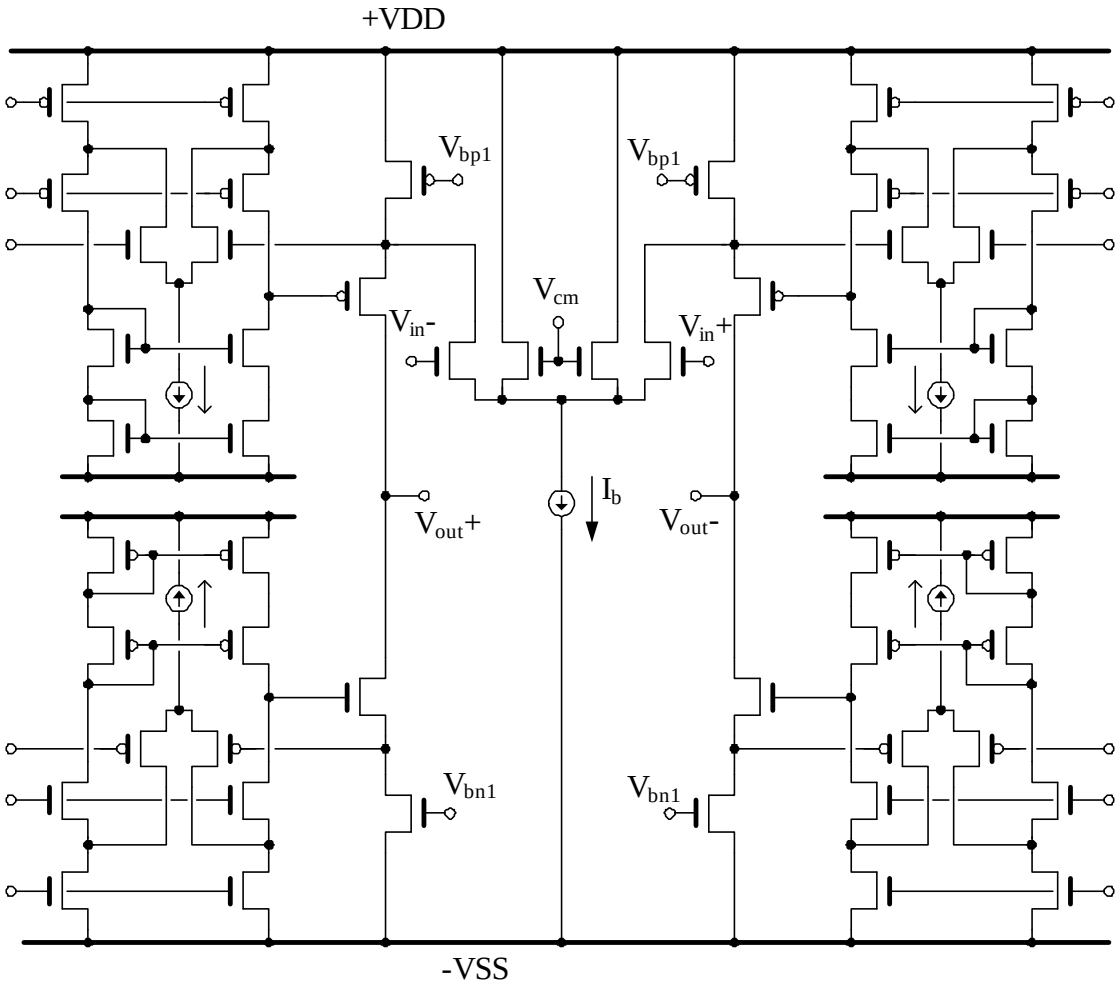
The time constant of the doublet, $\frac{1}{\omega_{PZ}}$, must be smaller than the main close-loop time constant, $\frac{1}{\beta\omega_{unity}}$. where β is the feedback factor.

The safe range for the ω_4.



$$\beta\omega_5 < \underset{\text{doublet}}{\omega_4} < \omega_6$$

4. CMOS OP AMP circuit



MAIN CHARACTERISTICS OF THE OP AMP

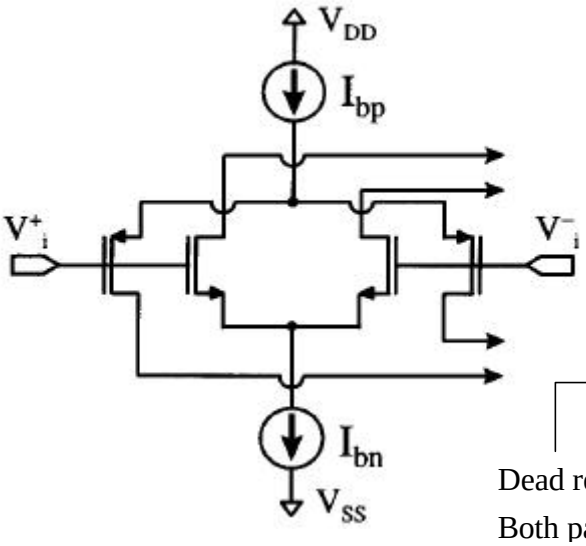
Gain enh.	on	Off
DC-gain	90dB	46dB
Unity-gain freq.	116MHz	120MHz
Load cap.	16pF	16pF
Phase margin	64deg.	63deg
Power cons.	52mW	45mW
Output-swing	4.2V	4.2V
Supply voltage	5.0V	5.0V
Settling time 0.1% , $\Delta V_o = 1V$	61.5ns	-

§ 8-5.2 1V Rail-to-Rail CMOS OP AMPs

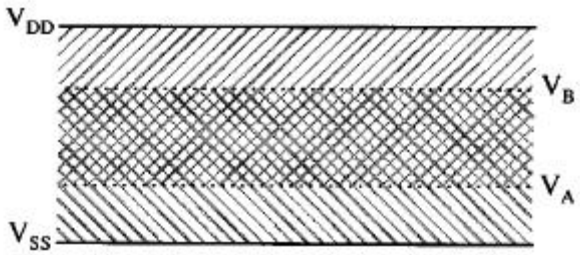
Ref.: IEEE JSSC vol.35, no.1, pp.33-44 Jan. 2000

1. Typical input stage for rail-to-rail amplifiers

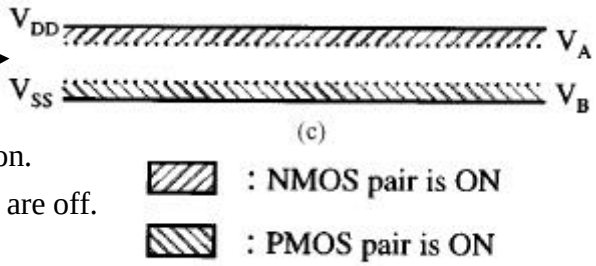
* Parallel-connected complementary differential pairs.



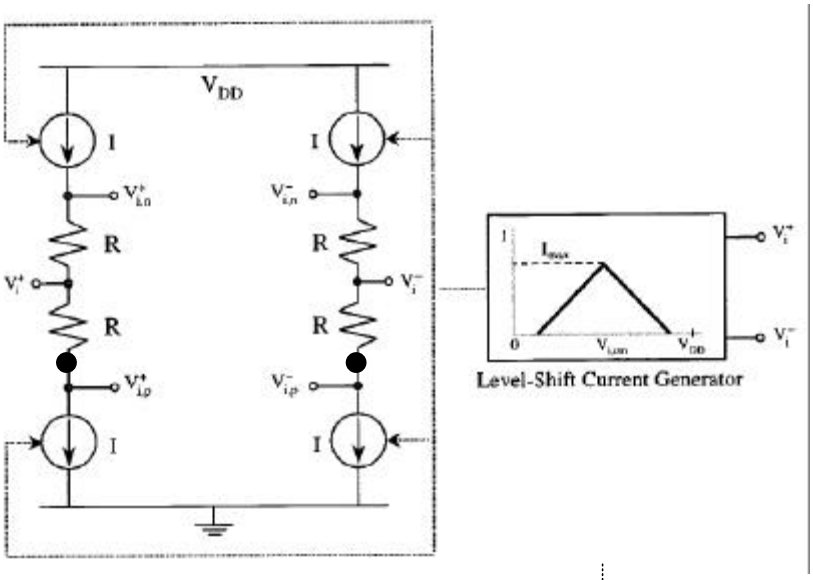
* Operating zones for low VDD/VSS



* Operating zones for extremely low VDD/VSS



2. Dynamic level-shifting current generator



Vi,n,cm=Vi,cm+IR

Vi,p,cm=Vi,cmi-IR

* The input resistance over the entire voltage range is infinite and no loading effect or input current over the previous stage.

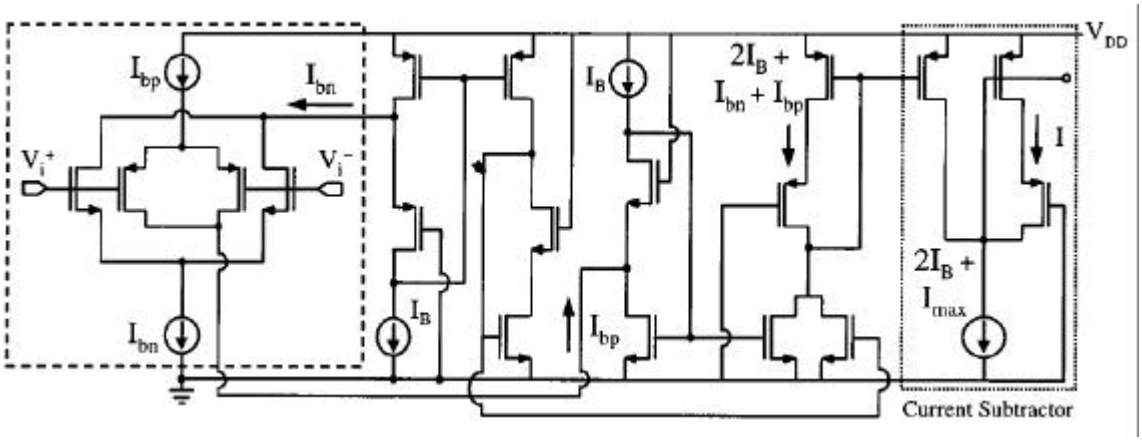
Usually mismatches cause negligible input current.

* The symmetrical topology ensures very high CMRR

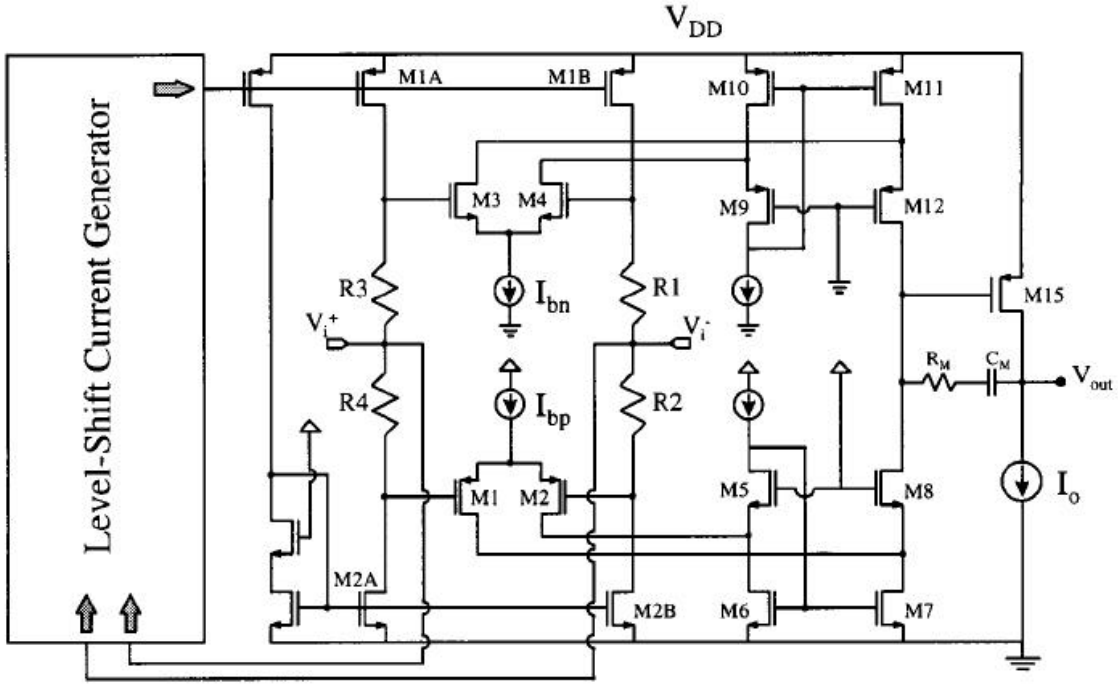
$$CMRR = \frac{1}{RG_m}\left(\frac{\Delta R}{R} + \frac{\Delta G_m}{G_m}\right)^{-1}$$

where $G_m = \Delta I / \Delta V_{i,cm}$

Circuit implementation



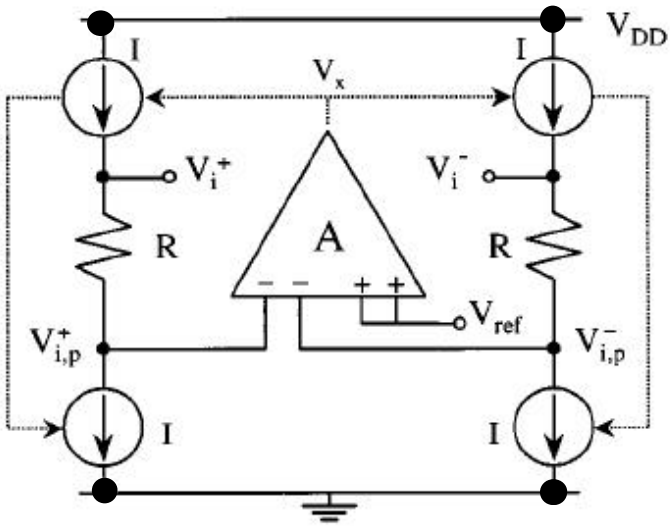
3. Rail-to-rail very LV CMOS OP AMP with input dynamic level-shifting circuit



MAIN TRANSISTOR ASPECT RATIOS (IN μm) AND ELEMENT VALUES OF THE AMPLIFIER BASED ON COMPLEMENTARY PAIRS

M1A,M1B	400/5	M15	700/2
M2A,M2B	200/5	R1-R4	30 *K*Ω
M1,M2	400/2	R_M	5 *K*Ω
M3,M4	200/2	C_M	10pF
M5-M8	400/5	$I_{bn} = I_{bp}$	10μA
M9-M12	500/5	I_o	40μA

4. Input CM adapter



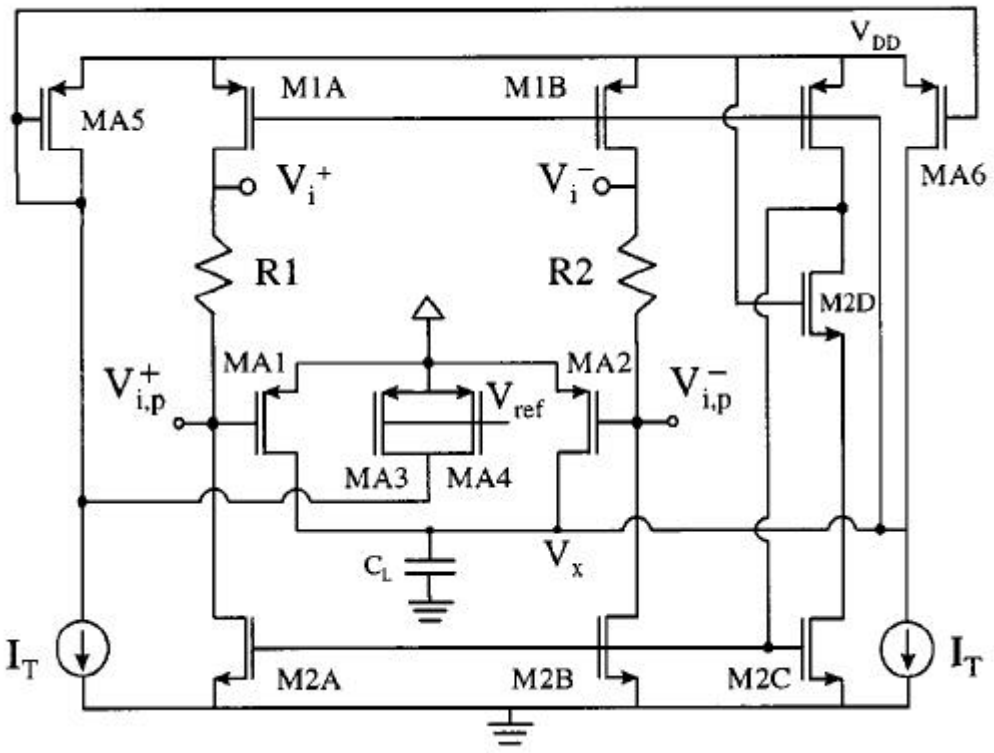
$$Vx = A[2V_{ref} - (V_{i,p}^{+} + V_{i,p}^{-})]$$
$$= 2A(V_{ref} - V_{i,p,cm})$$

$$I = G_m V_x$$
$$\Rightarrow V_{i,p,cm} \cong V_{ref} + \frac{V_{i,cm}}{2RG_mA}$$

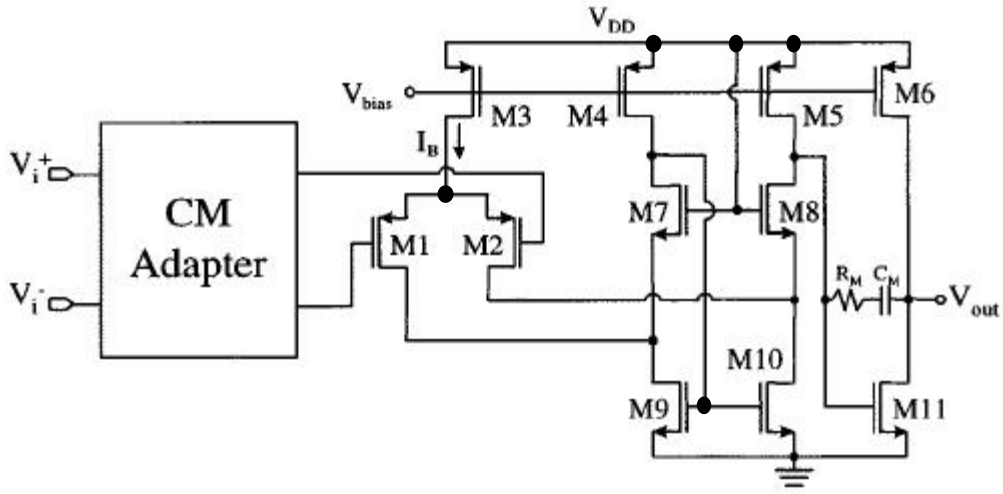
$$V_{i,p,dm} = V_{i,dm}$$

*$V_{i,cm}$ is degraded by A and $V_{i,p,cm} \cong V_{ref}$

Circuit implementation:



5. Very LV CMOS OP AMP with a single differential pair and the input CM adapter.



Main transistor ratios(in μm) and element values of the amplifier based on a single input pair

M1A M1B	1000/6	M6	1600/2
M2A M2B	600/4	M7-M10	300/4
MA1-MA4	50/2	M11	700/2
MA5-MA6	300/4	R1-R2	15KΩ
M2D	150/2	R_M	5KΩ
M1,M2	200/2	C_M	5pF
M3-M5	400/2	Is=Ir/2	10μA

6.Measured results

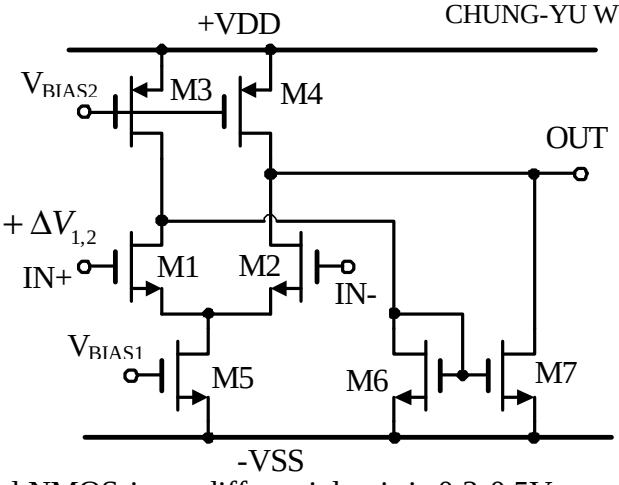
Experimental performance of amplifiers(Vsupply=1V,technology:1.2μm CMOS, C_L=15pF)

Parameter	Dynamic-shifting amp	CM adapater amp
Active die area	0.81mm^2	0.26 mm^2
Ido(supply current)	410uA	208uA
DC gain	87dB	70.5dB
unity-gain frequency	1.9Mhz	2.1Mhz
Phase margin	61°	73°
SR+ SR-	0.8V/us 1V/us	0.9V/us 1.7V/us
THD(0.5Vpp@1kHz) THD(0.5Vpp@40kHz	-54dB -32dB	-77dB -57dB
Vni(@1KHz) Vni(@10KHz) Vni(@1MHz)	267nV/$\sqrt{Hz}$ 91nV/$\sqrt{Hz}$ 74nV/$\sqrt{Hz}$	359nV/$\sqrt{Hz}$ 171nV/$\sqrt{Hz}$ 82nV/$\sqrt{Hz}$
CMRR	62dB	58dB
PSRR+ PSRR-	-54.4dB -52.1dB	-56.7dB -51.5dB

§8-5.3 1.5V High Drive Capability CMOS OP AMP

Ref.: IEEE JSSC vol.34, no.2, pp. 248-252, Feb. 1999

1. Folded-mirror differential input stage



$$V_{CM} \le V_{GS\,6,7} + V_{THn} = 2V_{THn} + \Delta V_{6,7}$$

$$V_{CM} \ge V_{DSsat\,5} + V_{GS\,1,2} = 2V_{THn} + \Delta V_5 + \Delta V_{1,2}$$

$$CMR = V_{THn} - \Delta V_5$$

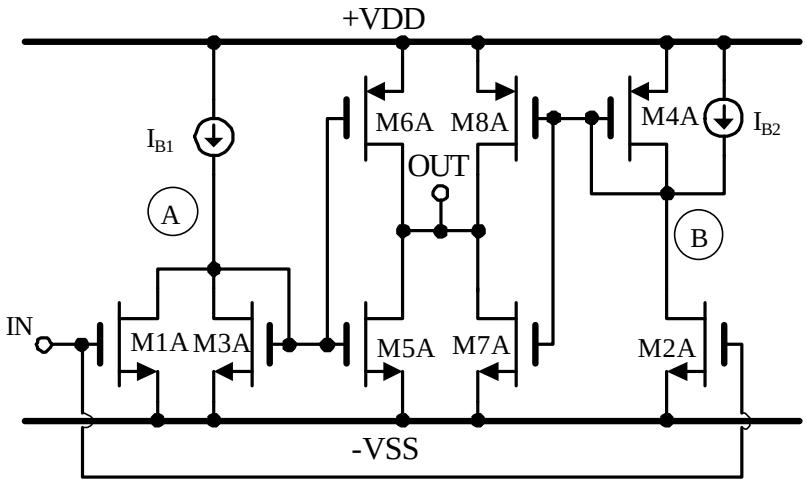
ΔV : overdrive voltage.

CMR is independent of supply voltage.

For V_{DD}=1.5V , CMR=0.6 ~ 0.7V

CMR of the conventional NMOS-input differential pair is 0.3-0.5V

2. Output Stage



Input section : M1A-M4A , I_{B1} , I_{B2}

Output section: M5A-M6A and M7A-M8A

M5A, M8A sat

M6A, M7A off.

For low input levels , M6A and M7A off ➔ Class A operation.

For large positive input signals,

$I_{D1A}=I_{B1}$ ➔ M3A and M5A OFF

➔ $V_A \rightarrow -V_{SS}$

➔ M_{6A} is turned on to supply most of the output current.

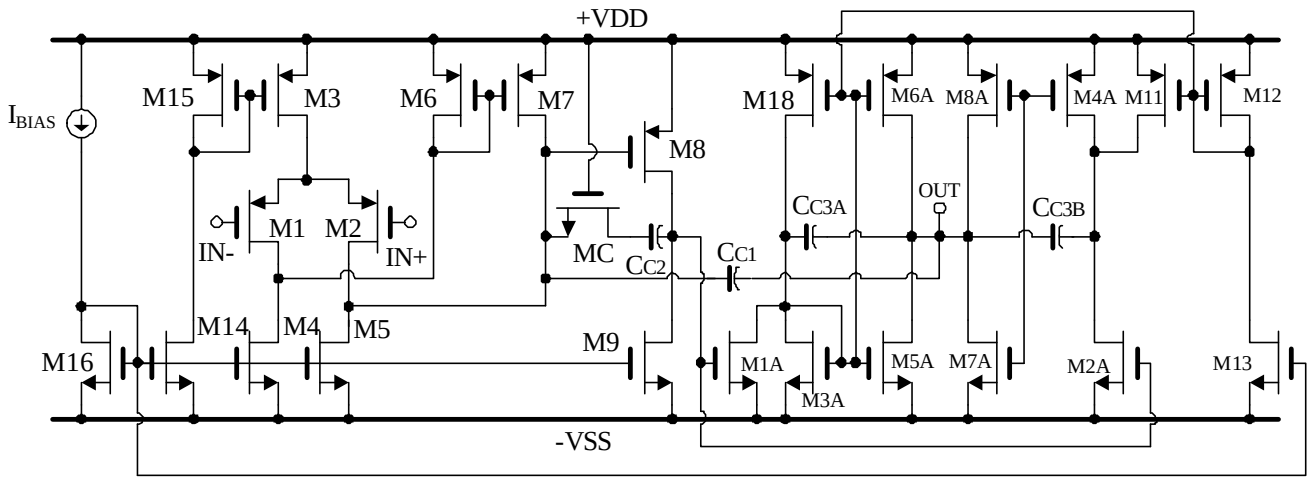
But M7A remains cutoff.

The current of M8A is increased.

For large negative input signals, M_{7A} supplies most of the output current.

$(W/L)_{5A,8A} << (W/L)_{6A,7A}$ for low dc power dissipation and high drive.

3. Overall LV CMOS OP AMP.



Dominant pole : $Wp1 \approx \frac{1}{r_{o5,7}\{(g_{m8}r_{o8,9})2[g_{m5A,8A}(r_{o5A} \| r_{o8A})]\}Cc}$

Gain-bandwidth product: $W_{GBW} \approx \frac{g_{m1,2}}{C_{c1}}$

Hybrid nested Miller compensation: C_{C1}, C_{C2}, $C_{C3A,B}$

The inner amplifier M_8,M_9,M_{1A}~M_{8A} contributes the nondominant poles.

* The two-stage OP AMP M_1~M_9 has a gain-bandwidth product of $\frac{g_{m1,2}}{C_{c2}}$

and the gain of $\frac{g_{m1,2}}{sC_{c2}}$ at high frequency. The gain of M_1-M_7 at high frequency is

$\frac{g_{m1,2}}{sC_{c1}}$. Thus the gain of the gain stage M8 and M9 is approximately equal to $\frac{C_{C1}}{C_{C2}}$.

* The open-loop gain of the inner amplifier is

$$A_{in} \cong -\left(\frac{C_{C1}}{C_{C2}}\right)\left(\frac{g_{m1A,2A}}{g_{m3A,4A}}\right)2g_{m5A,8A}\left(r_{o5A} \| r_{o8A}\right)$$

Dominant pole : $w_{P1in} \cong \frac{g_{m3A,4A}}{g_{m5A,8A}(r_{o5A} \| r_{o8A})C_{C3A,B}}$

Second pole : $w_{P2in} \cong \frac{2g_{m5A,8A}}{C_L}$

Gain-bandwidth product : $\omega_{GBWin} \cong 2\frac{C_{C1}}{C_{C2}}\frac{g_{m1A,2A}}{C_{C3A,B}}$
or the second pole of the
whole amplifier

Design consideration :

To obtain a maximally flat Butterworth response without gain peaking, we have the unity-gain frequency equal to one half of the second-pole frequency.

$$\omega_{GBWin} = \omega_{uin} = \frac{1}{2}\omega_{P2in}$$

$$\omega_{GBW} = \omega_{u} = \frac{1}{2}\omega_{uin} = \frac{1}{2}\omega_{GBWin}$$

Reference : IEEE JSSC, vol.27, pp.1709-1716, Dec. 1992.

Setting $2C_{C3A,B} = C_{C2}$, we have

$$C_{C1} = 2\frac{g_{m1,2}}{g_{m5A,8A}}C_L$$

$$C_{C2} = 2C_{C3A,B} = \sqrt{2g_{m1,2}g_{m1A,2A}} \cdot \frac{C_L}{g_{m5A,8A}}$$

Component values :

M1,M2,M3,M9,M1A,M2A,M10	60/2
M4,M5,M11,M12,M13	20/2
M6,M7	15/2
M8	90/2
M3A	5/1.2
M4A	15/1.2
M5A	30/1.2
M7A	120/1.2
M6A	360/1.2
M8A	90/1.2
M14,M16	10/1.2
M15,MC	30/2
C_{C1}	4pF
C_{C2}	6pF
C_{C3A},C_{C3B}	2pF
I_{BIAS}	5uA
V_{TH}	0.8V

Experimental results:

MEASURED MAIN PERFORMANCE

Open-Loop Gain	68dB
GBW	1MHz
Phase Margin	65^o
Gain Margin	16dB
Settling Time(0.1%), $\Delta V = 200mV$	400ns
Slew Rate	1 V/ μs
THD@1kHz $V_{out} = 0.5V$ RL=500Ω Closed-Loop Gain=20dB	-57dB
PSRR+@1kHz	75dB
PSRR- @1kHz	75dB
CMRR @1kHz	95dB
Offset	< 8mv
Power Dissipation	280 μW
Die Size	$0.08\,mm^2$
Technology	1.2 μm CMOS
Loading	50pF ‖ 500Ω