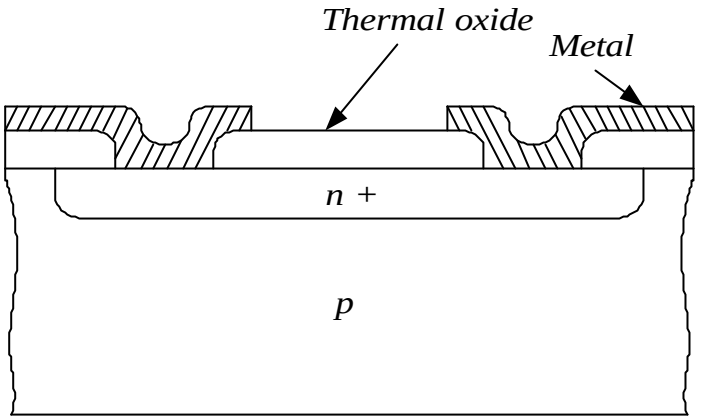
Chapter 9 Passive Components and Switches

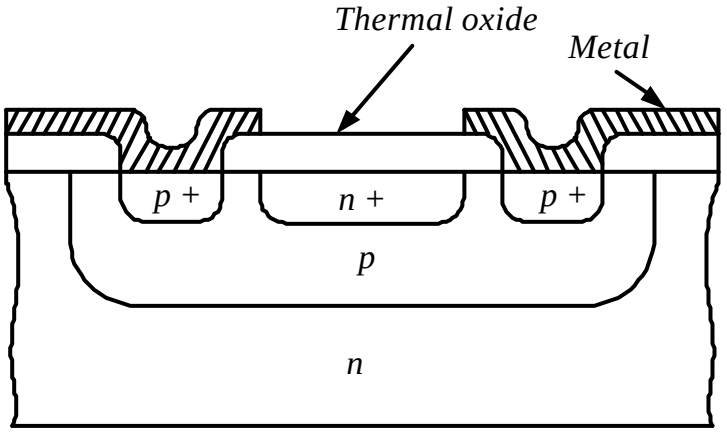
§ 9-1 Resistors

1. Source/Drain diffused resistor



* Compatible with NMOS and CMOS. metal-gate and Si-gate techniologies.
* $R_{\square}$ = *20 ~ 100W /□* (*100KW* max)
* Temperature Coefficient of Resistance (TCR) = 500~1500 ppm/^{o}C.
  Voltage Coefficient of Resistance (VCR)=100~500ppm/ ^{o}C
  Tolerance= ± 20% (Absolute)
* High parasitic capacitance (n^{+}-p junction cap.)
  Piezoresistance error. (Because of shallow junction)

2. P-well (N-well) diffused resistor (Well or tub resistor)

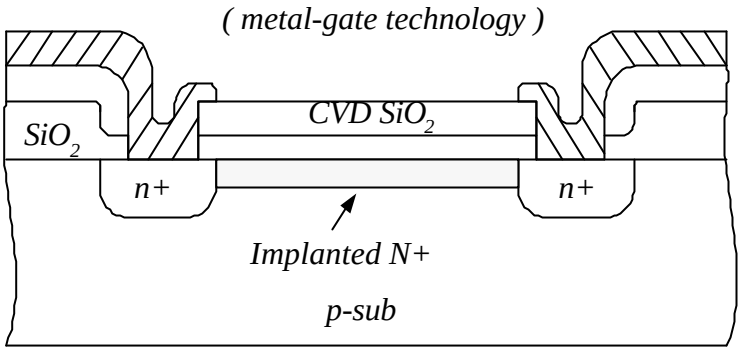


* Compatible with CMOS metal-gate or Si-gate technology.
* $R_{\square}$= *1KW ~ 5KW /□*
  Large VCR

Tolarance= ± 40% (absolute)

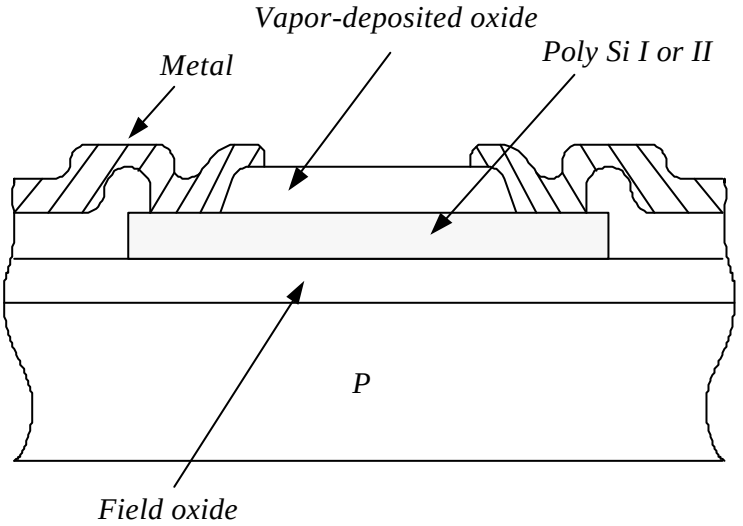
* Large depth and lateral spreading ⇒ narrow resistors are impossible.

3. Implanted resistor



* Compatible with NMOS and CMOS, metal-gate and Si-gate technologies.
* Need an additional masking step.
* $R_{\square} > 500\Omega \sim 1000\Omega / \square$; can be accurately controlled.
* Higher VCR ; smaller tolerance.
* Difficult to eliminate the piezoresistance effect.
* The resistor implant can be combined with the depletion implant.

4. Poly-Si resistor



* Realizable by NMOS and CMOS Si-gate technologies.
* $R_{\square} = 30\Omega \sim 200\Omega / \square$ (doped with the source/drain diffusion)
* TCR ≅ 500~1500 ppm/^{o}C ; Tolerance= ± 40%

* Can be trimmed by laser or poly fuse.
* Fully isolated with smaller parasitic capacitance.

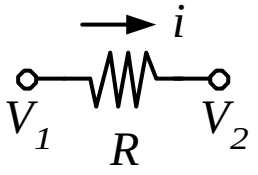
✧ Version I :Poly-I resistor

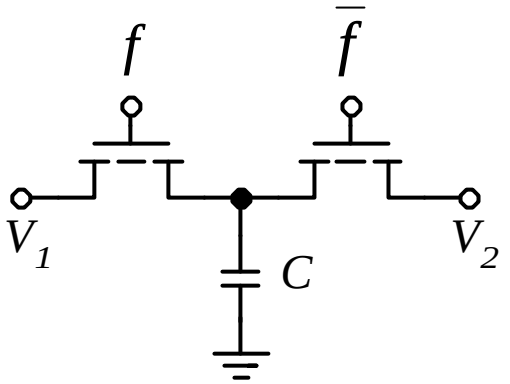
✧ Version II:Poly-II resistor

✧✧ Version III :Poly-I and Poly-II distributed RC structure (please see the structure shown in poly to poly capacitor)

5. Switched-capacitor simulated resistor

* Realizable by NMOS and CMOS , metal-gate and Sigate technologies.
* High frequency operation?





$i = \frac{V_1 - V_2}{R}$

f_C is the clock frequency of f or $\bar{f}$

$i = \frac{C(V_1 - V_2)}{T}$, $R = \frac{T}{C} = \frac{1}{f_C \cdot C}$

6. Thin-film resistor

* Realizable by NMOS and CMOS, metal-gate and Si-gate technologies.
* Need additional process steps.
* Si-Chromium resistor or Mo resistor.
* Laser trimming is possible.
* Non-conventional material may be involved.

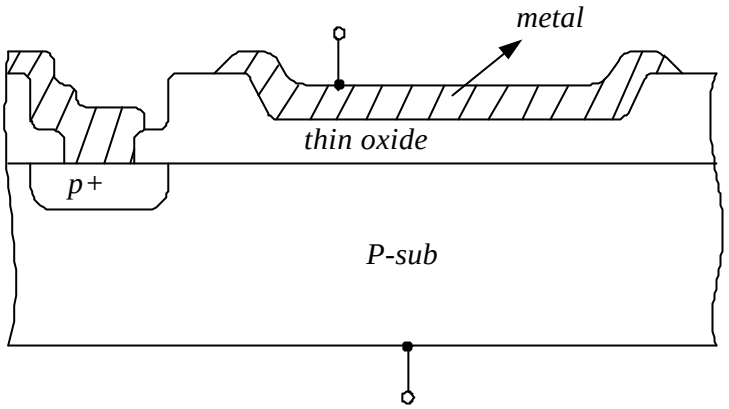
§ 9-2 Capacitors

1. PN junction capacitor

* Well known and understood.
* Nonlinear capacitance with a large VCR.

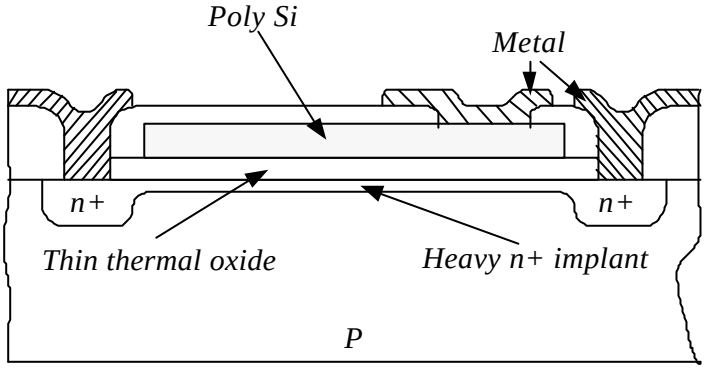
* Compatible with all MOS technologies.

2. MOS capacitor



* Realizable only by NMOS and CMOS metal-gate technology.
* TC=25 ppm/^{o}C
  Tolerance=±15%
  VC=25ppm/V
* Voltage-dependent capacitance
  accumulation depletion
  Co $(Co^{-1}\ Cd^{-1})^{-1}$

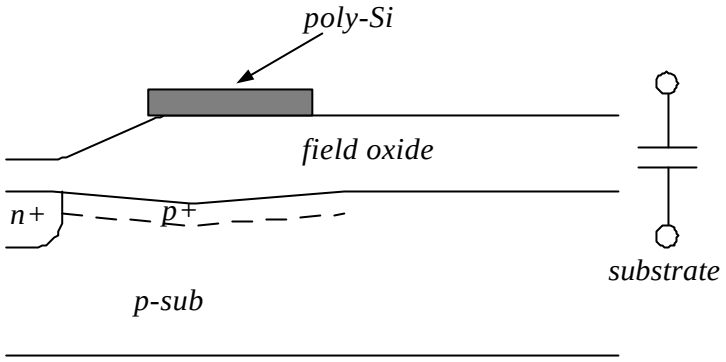
3. Poly (or metal) to bulk silicon capacitor



* Realizable by NMOS and CMOS poly-Si-gate (metal-gate) technologies.
* Need an extra mask to define the heavy n^{+} implant as the bottom plate.
* Can be trimmed by laser on poly-fuse.
  (Poly-fuse : blown with 10-20mA)
* Bottom plate pn junction parasitic capacitance ($\approx 15\% - 30\%$)
* VC of the capacitor$\approx$ -10ppm/V

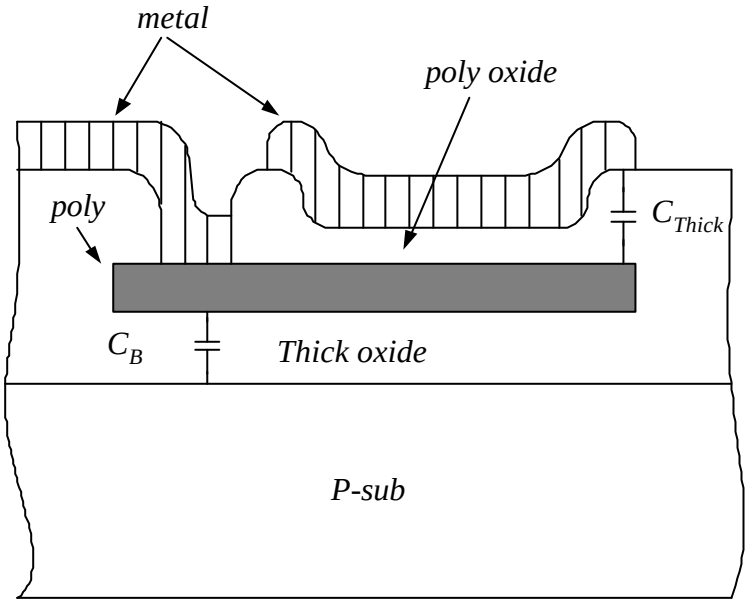
* TC ≈ 20-50 ppm/^{o}C
* Tolerance ≈ ±15%

4. Poly to field implant region capacitor



* Realizable only by NMOS and CMOS Si-gate technologies with the field implant.
* Smaller oxide capacitance per unit area
  ∵ Thick field oxide
* The capacitor's bottom plate must be always connected to the substrate.
* Low quality dielectric oxide.

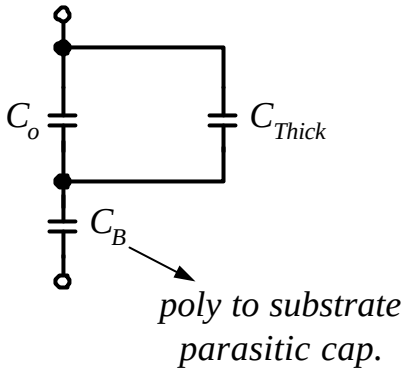
5. Metal to poly capacitor



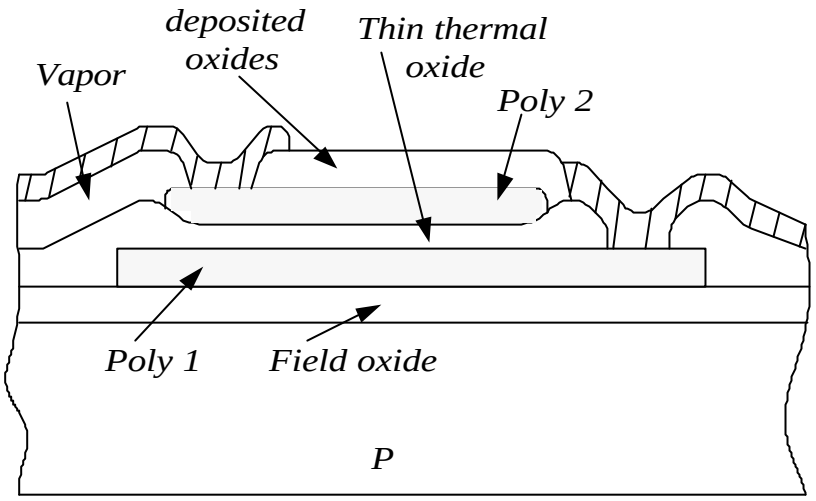
* Realizable by NMOS and CMOS Si-gate technologies.
* Interdielectric is poly-oxide.
* Extra mask to define the ploy-oxide pattern.
* Poly fuse trimming is possible.
* CVD oxide is not good as capacitor dielectric

∵ hysteresis in Q-V due to dielectric changing and relaxation.

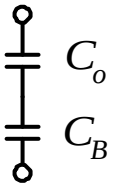
* For reliability consideration, the top metal layer must be larger than the poly oxide layer.
  ⇒ C_{Thick} exists
  ⇒ parasitic capacitance
* VC=100ppm/v, TC=100ppm/^{o}C



6. poly to poly capacitor



* Realizable by NMOS and CMOS double-poly technologies.
* VC=100ppm/v
  TC=100ppm/^{o}C
* Double-poly
  ⇒ EPROM or E^2PROM are available
  ⇒ may be applied in trimming
* The poly2 area may be smaller than the poly-oxide area
  ⇒ small C_{Thick}



General Reference: D. J. Allstot and W. C Black, Jr., IEEE Proc. vol-71, pp967-986, 1983.

§ 9-3 Tolerance Considerations.

Resistors : Absolute tolerance ≈ ±20% ~ ±40%
Matching or ratio tolerance ≈ ±0.1% ~ ±10%
Capacitors: Absolute tolerance ≈ ±15%

Matching or ratio tolerance $\approx \pm 0.01\% \sim \pm 1\%$

Resistors :

$$R = Rs\frac{L}{W} \quad , \quad \frac{DR}{R} = \frac{DL}{L} - \frac{DRs}{Rs} \approx \frac{DL}{L} - \frac{DW}{W}$$

If L is large $\Rightarrow \ \frac{DL}{L} \approx 0 \Rightarrow \frac{DR}{R} \approx \frac{DW}{W}$

$$R = \frac{\overline{r}}{Xt}\frac{L}{W} \quad , \quad s_R = \left[\left(\frac{d\overline{r}}{\overline{r}}\right)^2 + \left(\frac{dL}{L}\right)^2 + \left(\frac{dW}{W}\right)^2 + \left(\frac{dXt}{Xt}\right)^2\right]^{1/2}$$

$$= \frac{dW}{W} \qquad for \quad long \quad resistor$$

* Long resistor pattern is recommended in precise resistors.

Capacitors:

$$C = \frac{e_{sio2}}{t_{ox}}WL \qquad \frac{DC}{C} = \underbrace{\frac{DW}{W} + \frac{DL}{L}} + \underbrace{\frac{De_{si02}}{e_{sio2}} - \frac{Dt_{ox}}{t_{ox}}}$$

edge effect Oxide effect

CASE I : Absolute tolerance

$\frac{DC}{C} = \frac{DW}{W} + \frac{DL}{L}$ (if W and L are small or De_{sio2} and *Dtox* are neglible)

If ΔW and ΔL are independent with $s_{Dl} = s_{Dw} = s_l$

$s_{\frac{DC}{C}} = s_l\sqrt{\frac{1}{W^2} + \frac{1}{L^2}}$ (random variation)

Assume L=W=d , $s_{\frac{DC}{C}} = \frac{\sqrt{2}\sqrt{l}}{d}$ is minimum

$$\Rightarrow \ s_{\frac{DC}{C}}\Big|_{square(L=W)} < s_{\frac{DC}{C}}\Big|_{non-square(W\neq L)}$$

For the same WL ,minimum perimeter leads to minimum telerance.

Circular shape?

CASEII : Ratio or Matching tolerance under geometry random variation

$$a \equiv \frac{C_1}{C_2} = \frac{W_1 L_1}{W_2 L_2} \quad , \quad \frac{da}{a} = \frac{dC_1}{C_1} - \frac{dC_2}{C_2}$$

$$s_{\frac{da}{a}} = \sqrt{s_{\frac{dc_1}{c_1}}^{\,2} + s_{\frac{dc_2}{c_2}}^{\,2}} = s_l \sqrt{\frac{1}{L_1^{\,2}} + \frac{1}{W_1^{\,2}} + \frac{1}{L_2^{\,2}} + \frac{1}{W_2^{\,2}}}$$

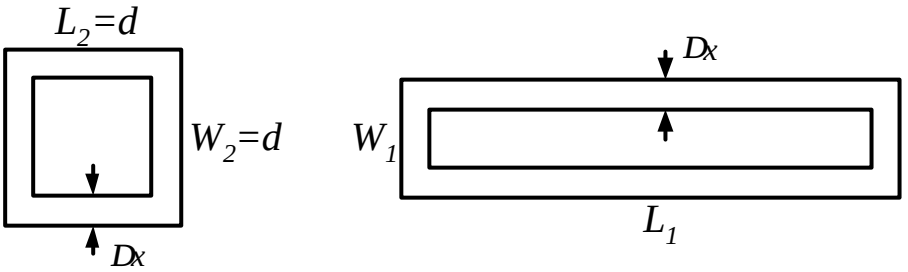
For W_2=L_2=d, $s_{\frac{da}{a}} = \frac{s_l}{d}\sqrt{2 + \frac{L_1^{\,2} + W_1^{\,2}}{(ad)^2}}$

$$\Rightarrow \left. s_{\frac{da}{a}} \right|_{min} = 2\frac{s_l}{d} \quad \text{if} \quad L_1 = W_1 = \sqrt{a}\,d \qquad (1)$$

square versus square

CASE III : Ratio tolerance under the uniform undercut effect

Uniform undercut is not a random variation.



$$a \equiv \frac{C_1}{C_2} = \frac{W_1 L_1}{d^2}$$

$$a_{actual} = \frac{W_1 L_1 - P_1 Dx + 4Dx^2}{d^2 - P_2 Dx + 4Dx^2} \cong \frac{W_1 L_1 - P_1 Dx}{d^2 - P_2 Dx}$$

$$\frac{Da}{a} \cong \frac{Dx}{d^2}\left(P_2 - \frac{P_1}{a}\right)$$

IF $P_2 = \frac{P_1}{a} \Rightarrow Da \cong 0$ i.e. $4d = \frac{2(W_1 + L_1)}{a}$

So $\left.\begin{array}{l} W_1 L_1 = ad^2 \\ 2(W_1 + L_1) = 4da \end{array}\right\}$

$$\Rightarrow W_1 = d\left(a - \sqrt{a^2 - a}\right) \quad ; \quad L_1 = d\left(a + \sqrt{a^2 - a}\right) \qquad (2)$$

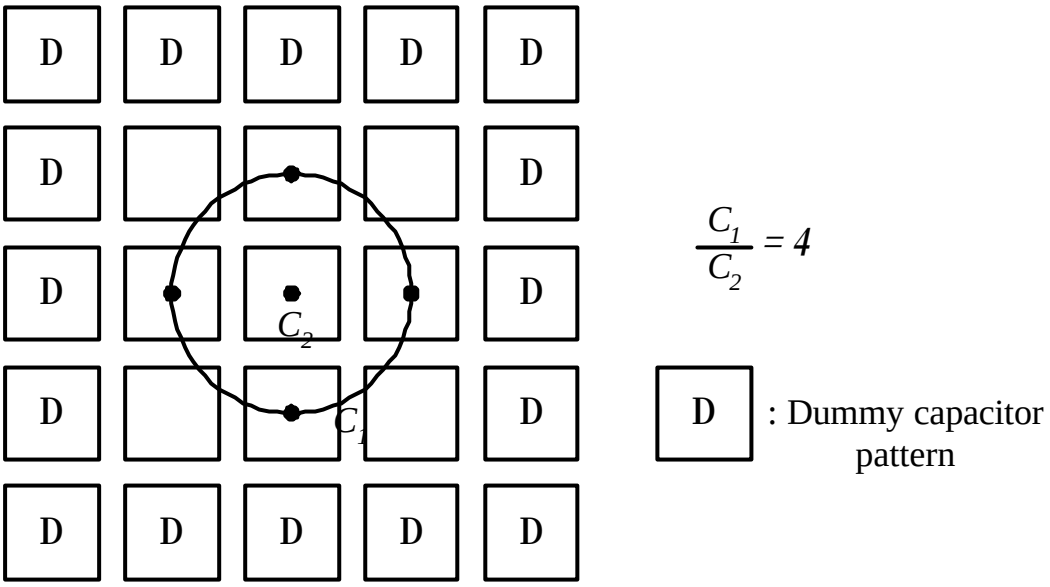
$$s_{\frac{da}{a}} = \frac{s_l}{d}\sqrt{6 - \frac{2}{a}} \overset{a>>1}{\cong} \frac{s_l}{d}\sqrt{6}$$

If $a = 1$, both conditions(1) and (2) can be satisfied

$\Rightarrow$ Ratio tolerance $\downarrow$

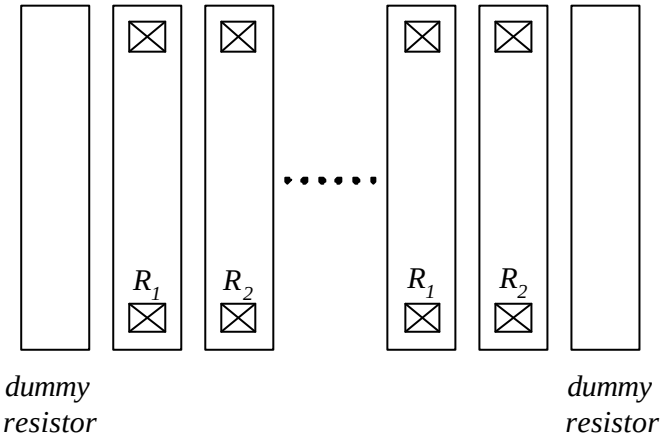
CASE IV : Ratio tolerance under edge and oxide effects

Take $a = 1 \Rightarrow$ unit capacitor array



* Centralized structure to avoid the oxide effect.
* Dummy capacitor may be omitted to save area.
* Ratio tolerance can be ±0.06 %

Similarly, for resistors, we have

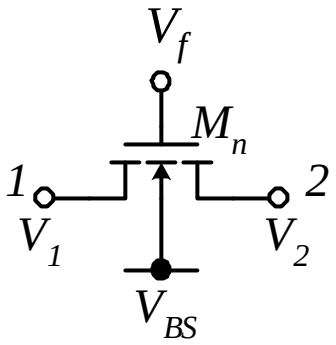


* Ratio tolerance can be ±0.25 %

§ 9-4 The MOS Switch

1. The NMOS switch

1) If $V_\phi \geq V_1 + V_{THN}$, M_N on $\Rightarrow V_2 = V_1$ full transimission



Example:

V_1= 0V, V_ϕ= 3V $\Rightarrow$ V_2= 0

V_1= 5V, V_ϕ= 8V, V_{TN} =1.5V $\Rightarrow$ V_2= 5V

2) If $V_1 + V_{THN} > V_f > V_{THN}$, M_N on

$V_2 = V_f - V_{THN}$

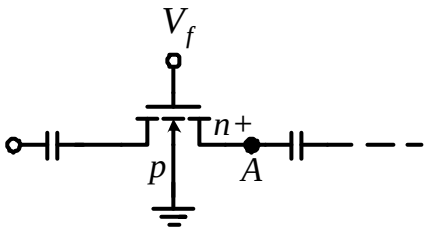
Example: $V_\phi = 5V$, $V_1 = 5V$, $V_{THN} = 1.5V$ (under substrate bias), $V_{BS} = 0V$

$\Rightarrow V_2 = 3.5V$

3) If $V_f < V_{THN}$, M_N off

Node 1 or 2 may be floating

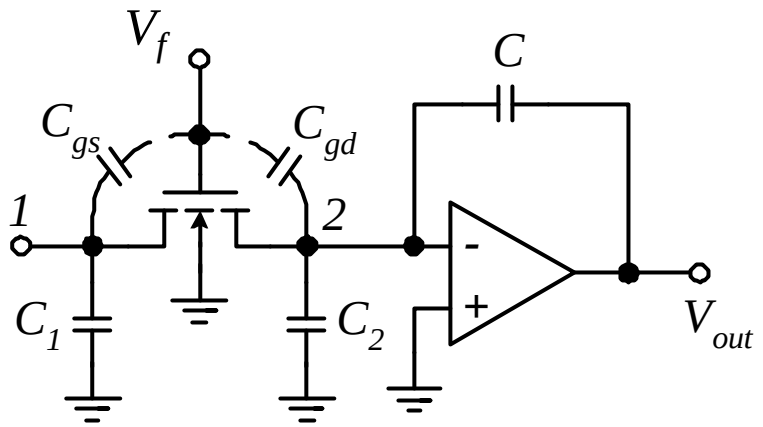
$\Rightarrow$ V_1 or V_2 will be gradually charged or discharged by the leakage current in MOS or PN junctions.



If $V_f = 0V$ for a very long time, $V_A \rightarrow 0V$ by the n^+p junction leakage current $\Rightarrow$ Not allowable in circuit design

* When the switch is turned on or off, the charging or discharging current is nonlinear $\Rightarrow$ Nonlinear resistor

Capacitance feedthrough effect:



$V_f : V_{DD} \rightarrow 0$

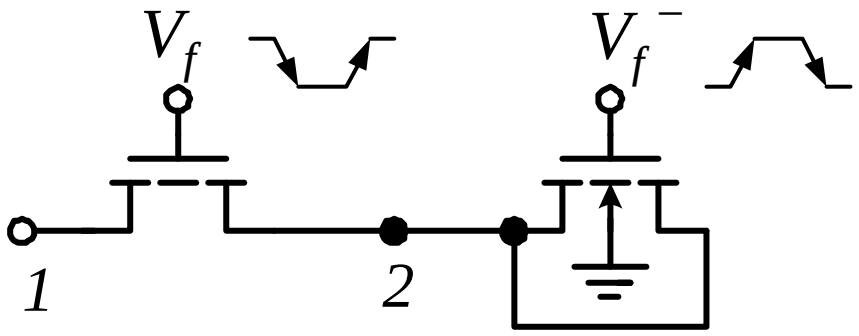
$$V_{1f} \approx V_{1i} - V_{DD}\frac{C_{gs}}{C_{gs}+C_1}$$

$$V_{2f} \approx V_{2i} - V_{DD}\frac{C_{gd}}{C_{gd}+C_1}$$

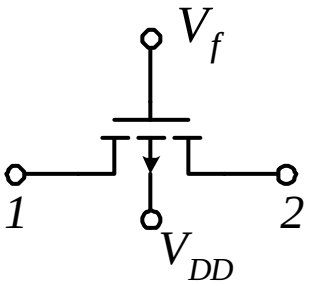
error voltage

Example: $C_{gd} \approx 0.02PF, C_2 = 2PF, V_{DD} = 10V$, error voltage $\approx 0.1V$

Compensation circuit:



2. The PMOS switch



* Can pass high voltage without offset.

Example: $V_\phi = 0V$, $V_{DD} = 5V = V_1$

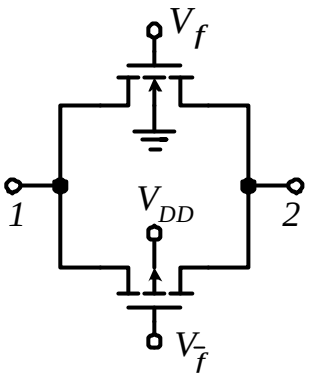
$\Rightarrow V_2 = 5V \quad \because 1 = source$ and $|V_{GS}| = 5V$

* Can' t pass low voltage completely.

  Example: $V_\phi = 0V$, $V_{2i} = 5V$, $V_1 = 0V$, $|V_{TP}| = 1.5V$

  $\Rightarrow V_{2f} \approx 1.5V \neq 0V$

3. The CMOS switch



* Full transmission
* The clock feedthrough effect can be greatly compensated, if the delay between V_f and $V_{\bar{f}}$ is zero.
* Nonlinear C_{gs} and C_{gd} and the delay between V_f and $V_{\bar{f}}$ make the compensation of the feedthrough effect quite complicated.
* If $V_1 = 5V = V_f, V_{\bar{f}} = 0V, V_{DD} = 5V, V_{TN} = |V_{TP}| = 1.5V$

  $V_2 = 0V \rightarrow V_2 = 5V - 1.5V = 3.5V$: NMOS and PMOS

  $V_2 = 3.5V \rightarrow V_2 = 5V$: Only PMOS

  If V_1=0V, V_{2i}=5V

  $V_2 = 5V \rightarrow V_2 = 1.5V$: NMOS and PMOS

  $V_2 = 1.5V \rightarrow V_2 = 0V$: Only NMOS