**EECS 140, Spring 2002**
**Problem Set 5 Solutions**

Reference:\\coeus\home\mdscott\240\project\defaults240.mcd

**Problem 1:**

Part A:

From HW4 solutions: $I_D := 2.5 \cdot mA \quad V_{dsatn} := 300 \cdot mV \quad \lambda := 0.02 \cdot \frac{1}{V} \quad A_{dm} := 333.333 \cdot \frac{V}{V}$

thus $g_{mn} := \frac{2 \cdot I_D}{V_{dsatn}} \qquad r_{otail} := \frac{1}{\lambda \cdot (2 \cdot I_D)}$

implies $A_{cm} := \frac{-1}{1 + 2g_{mn} \cdot r_{otail}} \qquad A_{cm} = -2.991 \frac{mV}{V}$

$CMRR := \frac{|A_{dm}|}{|A_{cm}|} \qquad CMRR = 1.114 \times 10^5 \frac{V}{V} \qquad dB(CMRR) = 100.941$

When the CM input is less than Vcm,min then the diff pair devices go into triode. This does not affect the CM gain that much (see equation above, it is not dependent on the diff pair devices).

When the CM input is greater than Vcm,max then the tail current source goes into triode. This decreases rotail quite a bit, and gmn goes down as well due to decreased current in the current mirror. So CM gain should grow in magnitude since gmn*rotail is decreasing. This continues until the tail current source is completely off (at Vcm=1V) at which point the CM gain is exactly 0.

Part B: See SPICE plots. The results are as expected (see above for explanations of curves).

Part C:

From HW4 solutions: $R_o := 10 \cdot k\Omega$ calculated $R_{ospice} := 10.18 \cdot k\Omega$

We must find the TOTAL output capacitance: $C_L := 10 \cdot pF$

$C_{draindiff} := 1.11 \cdot pF \qquad C_{drainn} := 138.9 \cdot fF$ from SPICE output

$C_{total} := C_L + C_{draindiff} + C_{drainn} \qquad C_{total} = 11.249\, pF$

$\omega_p := \frac{1}{R_{ospice} \cdot C_{total}} \qquad \omega_p = 8.733 \times 10^6 \frac{rad}{s} \qquad f_p := \frac{\omega_p}{2 \cdot \pi} \qquad f_p = 1.39\, MHz$

thus $\omega_u := A_{dm} \cdot \omega_p \qquad \omega_u = 2.911 \times 10^9 \frac{rad}{s} \qquad f_u := \frac{\omega_u}{2 \cdot \pi} \qquad f_u = 0.463\, GHz$

Part D:

The current mirror pole and zero are set by gm of the mirror and the total capacitance at that node.

$W_n := 277.8 \cdot \mu m$ $\quad L_n := 1 \cdot \mu m$ $\quad C_{ox} := 5 \cdot \frac{fF}{\mu m^2}$ $\quad C_{gs0} := 0.5 \cdot \frac{fF}{\mu m}$

$C_{gsn} := \frac{2}{3} \cdot C_{ox} \cdot W_n \cdot L_n + C_{gs0} \cdot W_n$ $\quad C_{gsn} = 1.065\,pF$

$C_{total} := 2 \cdot C_{gsn} + C_{draindiff} + C_{drainn}$ $\quad C_{total} = 3.379\,pF$

$\omega_{pm} := \frac{g_{mn}}{C_{total}}$ $\quad \omega_{pm} = 4.933 \times 10^9 \frac{rad}{s}$ $\quad f_{pm} := \frac{\omega_{pm}}{2 \cdot \pi}$ $\quad f_{pm} = 785.09\,MHz$

$\omega_{zm} := 2 \cdot \omega_{pm}$ $\quad \omega_{zm} = 9.866 \times 10^9 \frac{rad}{s}$ $\quad f_{zm} := \frac{\omega_{zm}}{2 \cdot \pi}$ $\quad f_{zm} = 1.57\,GHz$

Part E:

In addition to the output pole and the current mirror pole/zero doublet, there is an additional RHP zero in this circuit, due to Cgd of the diff pair (this is very similar to the zero we got for the amplifier circuit analyzed in HW3 and on the midterm):

$C_{gddiff} := 1.11 \cdot pF$ $\quad g_{mdiff} := 33.85 \cdot mS$ $\quad$ from SPICE

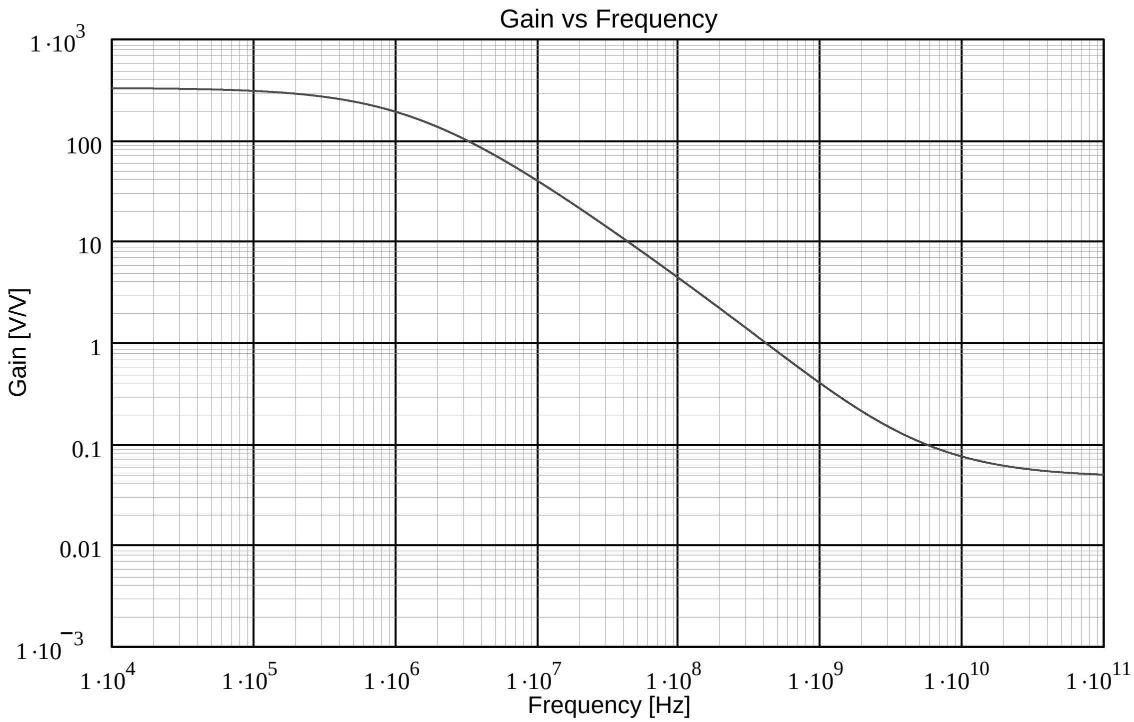
$\omega_{zdiff} := \frac{g_{mdiff}}{C_{gddiff}}$ $\quad \omega_{zdiff} = 3.05 \times 10^{10} \frac{rad}{s}$ $\quad f_{zdiff} := \frac{\omega_{zdiff}}{2 \cdot \pi}$ $\quad f_{zdiff} = 4.854\,GHz$

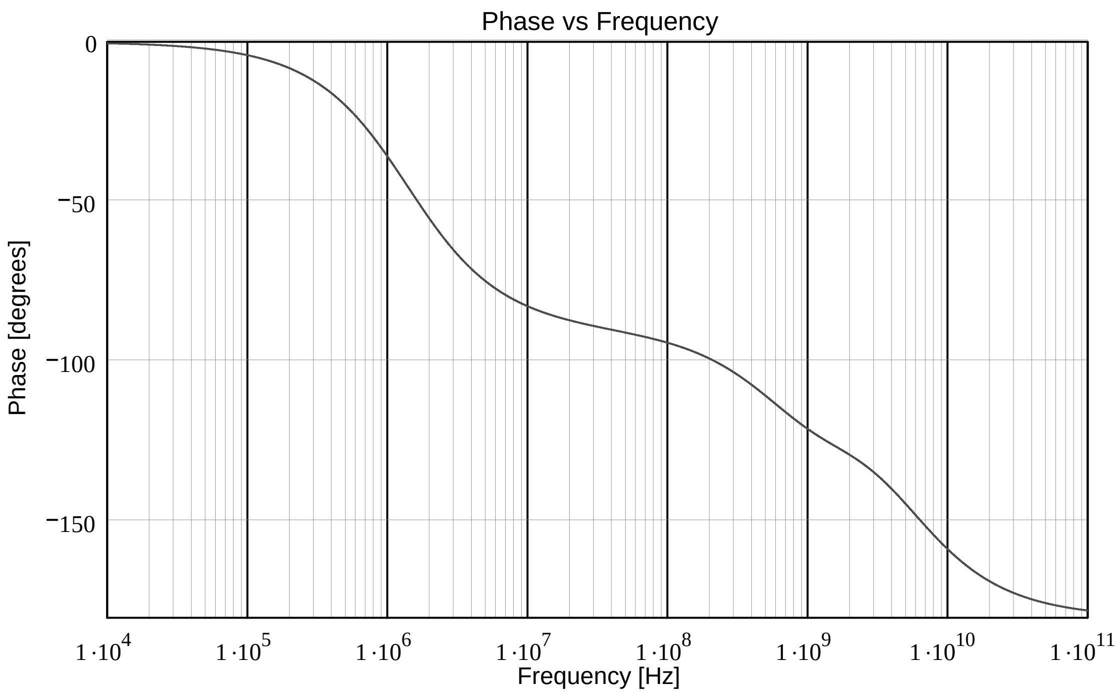
This high frequency zero contributes phase lag (RHP zero) which tends to cancel the phase effects of the LHP zero from the current mirror. Thus, the final phase should be -180 degrees instead of -90 degrees.

$$mag\_A_v(f) := \left[ \frac{A_{dm}^2 \cdot \left(1 + \frac{f}{f_{zm}}\right)^2 \cdot \left(1 + \frac{f}{f_{zdiff}}\right)^2}{\left(1 + \frac{f}{f_p}\right)^2 \cdot \left(1 + \frac{f}{f_{pm}}\right)^2} \right]^{0.5}$$

$$phase\_A_v(f) := \frac{180}{\pi} \cdot \left( atan\left(\frac{f}{f_{zm}}\right) + atan\left(\frac{-f}{f_{zdiff}}\right) - atan\left(\frac{f}{f_p}\right) - atan\left(\frac{f}{f_{pm}}\right) \right)$$

$n := 10000$ $\quad i := 1 .. n$ $\quad fr := logrange(10 \cdot Hz, 100 \cdot GHz, n)$




Part F: See SPICE plot. There is good agreement between the Bode plot above and SPICE.

Part G: See SPICE plots, which show the peak-to-peak output and the time delay (which can be used to determine output phase).

One fifth the pole freq: $f := \frac{f_p}{5}$ $f = 277.966\,\text{kHz}$

$V_{pp} := 0.674 \cdot V$ $A_{dm} := \frac{V_{pp}}{2 \cdot mV}$ $A_{dm} = 337\,\frac{V}{V}$

$t_d := 116 \cdot ns$ $phase := -360 \cdot t_d \cdot f$ $phase = -11.608$

From Bode plot above: $A_{dm} := 300$ $phase := -15$ decent agreement

Equal to the pole freq: $f := f_p$ $f = 1.39\,\text{MHz}$

$V_{pp} := 0.483 \cdot V$ $A_{dm} := \frac{V_{pp}}{2 \cdot mV}$ $A_{dm} = 241.5\,\frac{V}{V}$

$t_d := 90.4 \cdot ns$ $phase := -360 \cdot t_d \cdot f$ $phase = -45.231$

From Bode plot above: $A_{dm} := 243$ $phase := -45$ very good agreement

Five times the pole freq: $f := 5f_p$ $f = 6.949\,\text{MHz}$

$V_{pp} := 0.133 \cdot V$ $A_{dm} := \frac{V_{pp}}{2 \cdot mV}$ $A_{dm} = 66.5\,\frac{V}{V}$

$t_d := 33.5 \cdot ns$ $phase := -360 \cdot t_d \cdot f$ $phase = -83.807$

From Bode plot above: $A_{dm} := 60$ $phase := -80$ good agreement

Part H: See SPICE plots. We see that for low frequencies, the amplifier eventually settles to the correct output value and looks reasonably like a square wave. But for high frequencies, the amplifier cannot settle quickly enough and the output ends up looking like a triangle wave instead of square.

**Problem 2:**

Design

PMOS current source is the same size as the tail current source for the diff pair.

NMOS common source device must be twice the W/L as the current mirror devices because it runs twice the current for the same gate source bias. See circuit diagram.

Thus

Diff pair: $I_{tail} := 5 \cdot mA$ $\quad A_{diff} := 333.33 \cdot \frac{V}{V}$

CS amp: $g_{mcs} := \frac{2 \cdot I_{tail}}{V_{dsatn}}$ $\quad R_{ocs} := \frac{1}{2 \cdot \lambda \cdot I_{tail}}$ $\quad A_{cs} := g_{mcs} \cdot R_{ocs}$ $\quad A_{cs} = 166.667 \frac{V}{V}$

Part A:

Overall Diff Mode gain:

$A_{dm} := A_{diff} \cdot A_{cs}$ $\quad A_{dm} = 5.555 \times 10^4 \frac{V}{V}$ $\quad dB(A_{dm}) = 94.894$

Overall Common Mode gain: $\quad A_{cmdiff} := -2.991 \cdot \frac{mV}{V}$

$A_{cm} := -A_{cmdiff} \cdot A_{cs}$ $\quad A_{cm} = 0.499 \frac{V}{V}$ $\quad dB(A_{cm}) = -6.047$

$CMRR := \frac{|A_{dm}|}{|A_{cm}|}$ $\quad CMRR = 1.114 \times 10^5$ $\quad dB(CMRR) = 100.941$

Part B: See SPICE plot. The common mode gain agrees very well with the calculation above.

Part C:

$V_{dd} := 1.5 \cdot V$ $\quad V_{ss} := -1.5 \cdot V$ $\quad V_{tn} := 0.5 \cdot V$ $\quad V_{tp} := -0.5 \cdot V$ $\quad V_{dsatp} := 150 \cdot mV$

Common mode input range is unchanged from HW4:

| | | Reason: |
|---|---|---|
| $V_{cm\_min} := V_{ss} + V_{tn} + V_{dsatn} - \lvert V_{tp} \rvert$ | $V_{cm\_min} = -1.2\,V$ | keep diff pair devices in saturation |
| $V_{cm\_max} := V_{dd} - 2 \cdot V_{dsatp} - \lvert V_{tp} \rvert$ | $V_{cm\_max} = 0.7\,V$ | keep tail current source in saturation |

Output range is improved with common source output stage:

$V_{o\_min} := V_{ss} + V_{dsatn}$ $\quad V_{o\_min} = -1.2\,V$ keep current source in saturation

$V_{o\_max} := V_{dd} - V_{dsatp}$ $\quad V_{o\_max} = 1.35\,V$ keep diff pair in saturation

Part D: See SPICE plots. We see that the amplifier gain is essentially unchanged over this range of CM input. This is to be expected since Vcm= -1, 0, and 0.5V is within the CM input range above.

Part E:

Actual gain calculation:

$$A_v := \frac{A_{vo}}{1 + A_{vo} \cdot f}$$ classical feedback result

For unity gain: $A_{vo} := 5.555 \cdot 10^4$ $\quad f := 1$

$$A_v := \frac{A_{vo}}{1 + A_{vo} \cdot f} \qquad A_v = 1$$

For gain of 5 (40kohm and 10kohm): $f := \frac{1}{5}$ $\quad A_{cs} := g_{mcs} \cdot R_{ototal}$

$$R_{ototal} := \frac{1}{\frac{1}{R_{ocs}} + \frac{1}{50 \cdot k\Omega}} \qquad R_{ototal} = 4.545\,k\Omega$$

$$A_{vo} := A_{diff} \cdot \left(g_{mcs} \cdot R_{ototal}\right) \qquad A_{vo} = 5.05 \times 10^4$$

$$A_v := \frac{A_{vo}}{1 + A_{vo} \cdot f} \qquad A_v = 5$$

For gain of 5 (800ohm and 200ohm): $f := \frac{1}{5}$ $\quad A_{cs} := g_{mcs} \cdot R_{ototal}$

$$R_{ototal} := \frac{1}{\frac{1}{R_{ocs}} + \frac{1}{1 \cdot k\Omega}} \qquad R_{ototal} = 0.833\,k\Omega$$

$$A_{vo} := A_{diff} \cdot \left(g_{mcs} \cdot R_{ototal}\right) \qquad A_{vo} = 9.259 \times 10^3$$

$$A_v := \frac{A_{vo}}{1 + A_{vo} \cdot f} \qquad A_v = 4.997$$

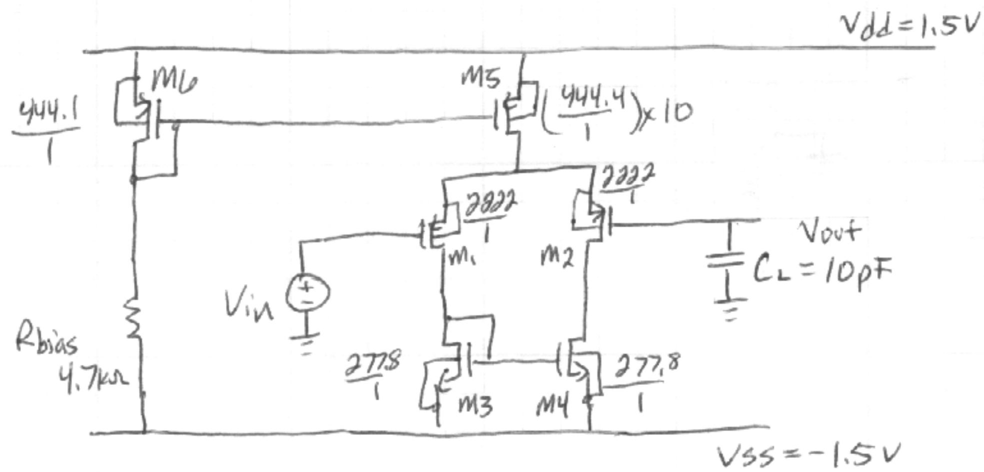
For all cases now we see that the gains are extremely close to the desired value. This is due to the fact that Avo is so large (and hence Avo*f is large). Thus the gain is very nearly equal to 1/f, which is the whole point of designing an opamp to have such a large DC gain.

SPICE verifies these caculations, along with the CM input range and output ranges found above. Specifically, we hit Vcm,max for the unity gain case, and we always see that the gain degrades for all cases once the output is below Vo,min and above Vo,max.

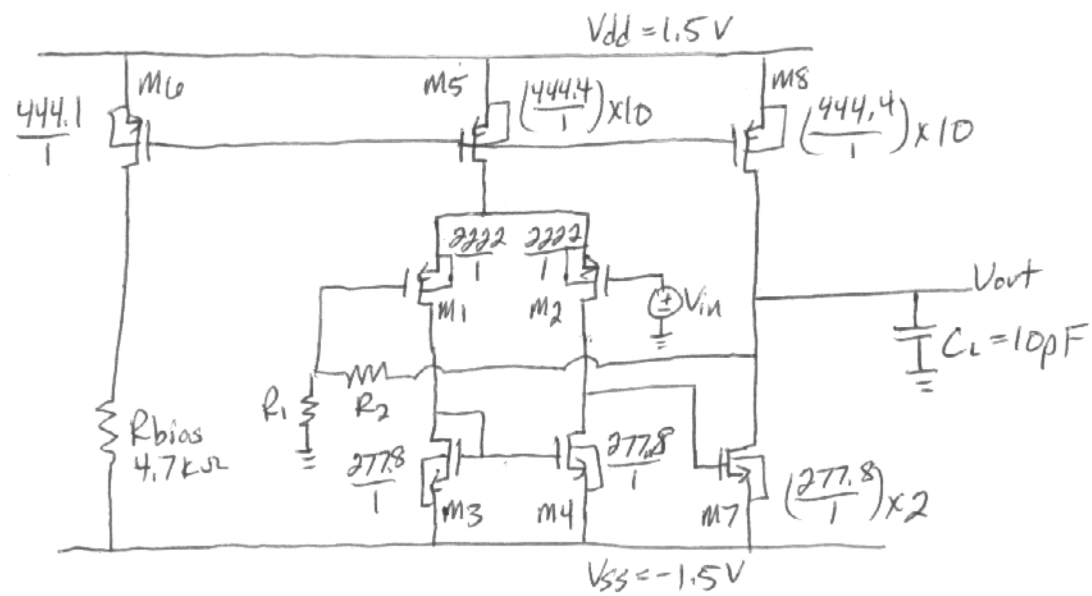
Note that this new opamp (2-stage) is capable of swinging within 100mV of each rail, as we can set the Vdsat's for both devices in the second stage equal to 100mV if we choose.

## Circuits used:

Problem 1:




Problem 2:



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* EECS 140, Spring 2002
* HW 5 Solutions
* Simple opamp
*

* opamp subcircuit *
.subckt opamp inp inm out vdd vss
M1 vo1 inp vtail vtail PMOS1 W=2222u L=1u
M2 out inm vtail vtail PMOS1 W=2222u L=1u
M3 vo1 vo1 vss vss NMOS1 W=277.8u L=1u
M4  out vo1 vss vss NMOS1 W=277.8u L=1u
M5 vtail vbias vdd vdd PMOS1 W=444.4u L=1u M=10
M6 vbias vbias vdd vdd PMOS1 W=444.4u L=1u
Rbias vbias vss 4.7k
.ends opamp

************************************************************************
**
* balun
*     converts diff/cm <---> balanced signals
*     (works both ways)
* terminals:
*     vdm         differential voltage
*     vcm         common-mode voltage
*     vp          positive terminal of balanced port
*     vm          negative terminal of balanced port
*
************************************************************************
**
*
.subckt balun vdm vcm vp vm
e1 vp vcm transformer vdm 0 2
e2 vcm vm transformer vdm 0 2
.ends

* opamp *
x1 vinp vinm vout vdd vss opamp
x2 vdm vcm vinp vinm balun

* Supply voltages *
Vdd vdd 0 DC 1.5V
Vss vss 0 DC -1.5V

* Input voltages *
*Vdm vdm 0 DC 0V AC 1V
*Vdm vdm 0 DC 0V AC SIN(0 1e-3 1.39e6Hz 0 0 0)
Vdm vdm 0 DC 0V PULSE(-1e-3 1e-3 0 1n 1n 360n 720n)
Vcm vcm 0 DC 0V

* Load *
Cl vout 0 10p

* Analyses *
.include '../lib/model2'
*.OP
*.dc Vcm -1.5 1.5 10m
*.tf V(vout) Vcm
*.tf V(vout) Vdm
*.pz V(vout) Vdm
*.ac dec 100 10 100G
```

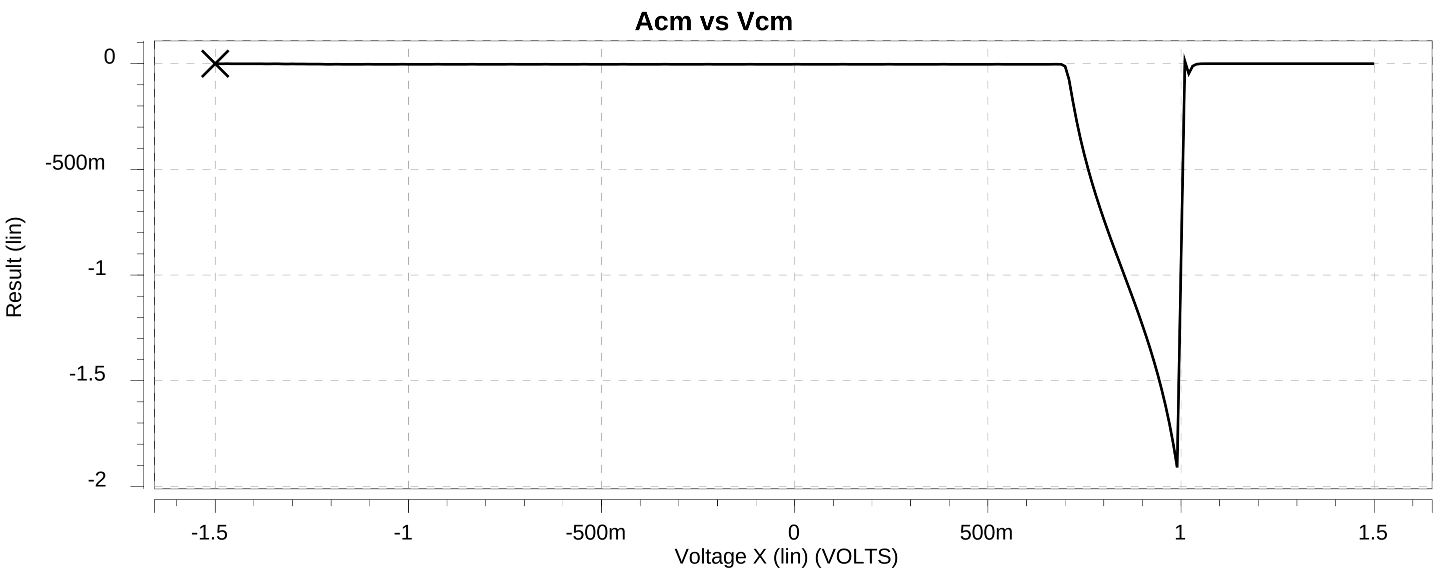
```
.tran 1n 5u
.options dccap post=2 nomod brief accurate

* Hand calculation for Acm
VAcm Acm 0 DC -2.99mV

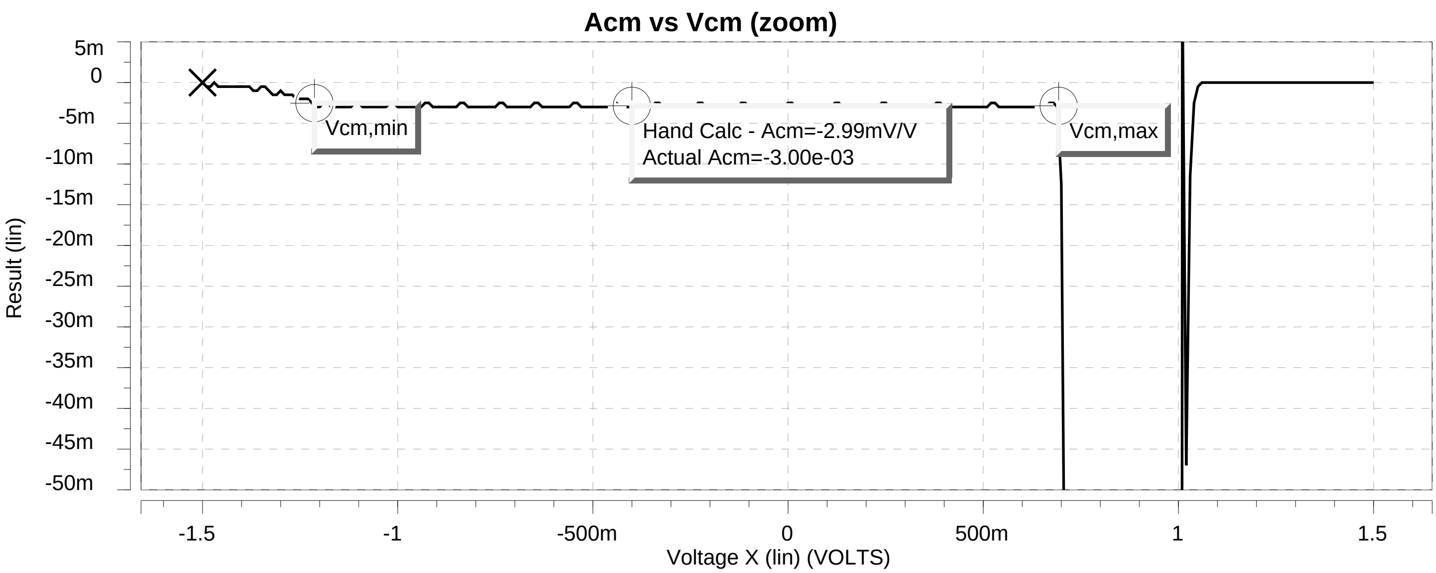
* Also probe equations for the hand calculations
* so that it can all be plotted in Awaves
.probe V(vcm) V(vout) gain_dB=PAR('20*log10(V(vout)/V(vdm))') V(Acm)

.alter 5xpole
Vdm vdm 0 DC 0V PULSE(-1e-3 1e-3 0 1n 1n 72n 144n)
*Vdm vdm 0 DC 0V AC sin(0 1e-3 6.95e6Hz 0 0 0)
.alter 0.2xpole
Vdm vdm 0 DC 0V PULSE(-1e-3 1e-3 0 1n 1n 1.8u 3.6u)
*Vdm vdm 0 DC 0V AC sin(0 1e-3 0.278e6Hz 0 0 0)

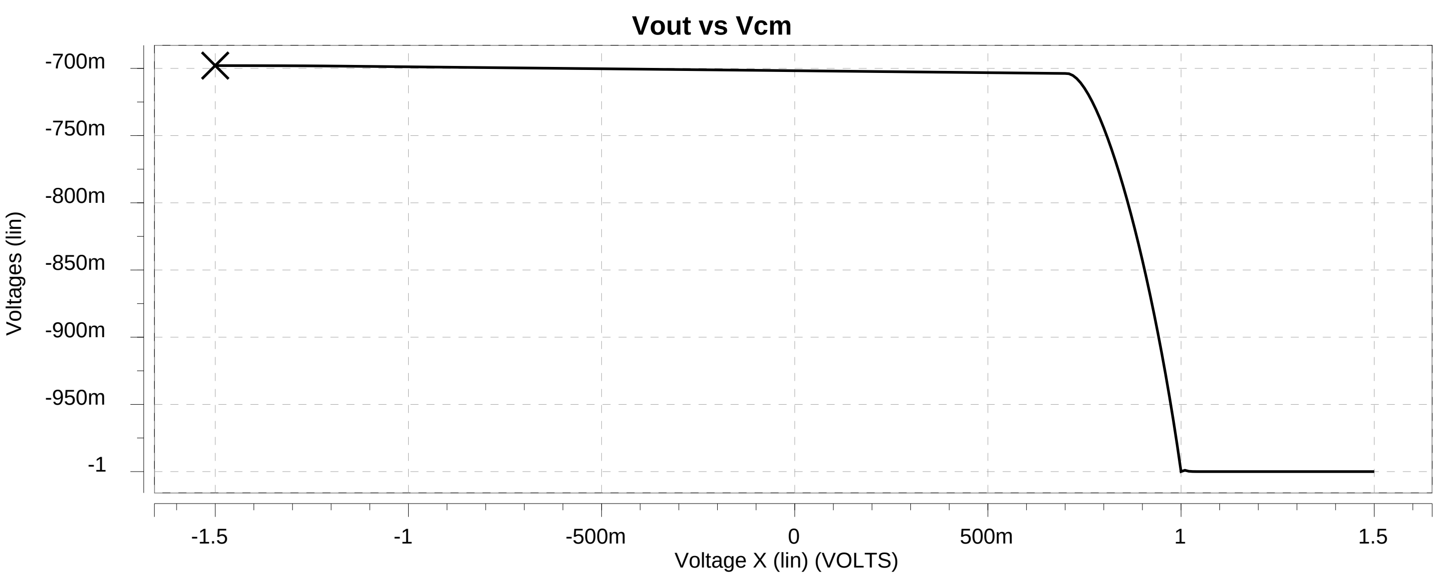
.end
```



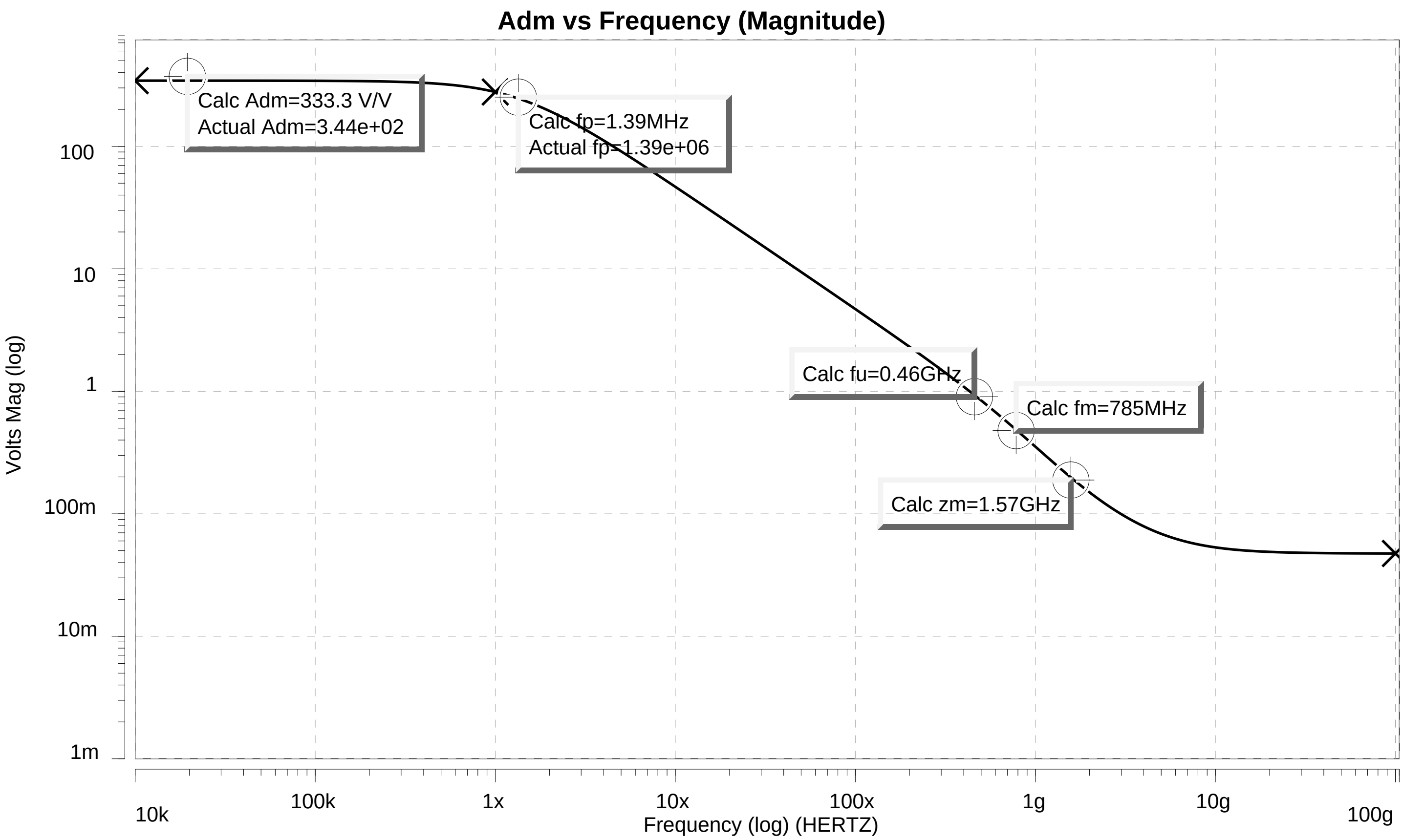
Acm vs Vcm
Result (lin)
0
-500m
-1
-1.5
-2
-1.5
-1
-500m
0
500m
1
1.5
Voltage X (lin) (VOLTS)

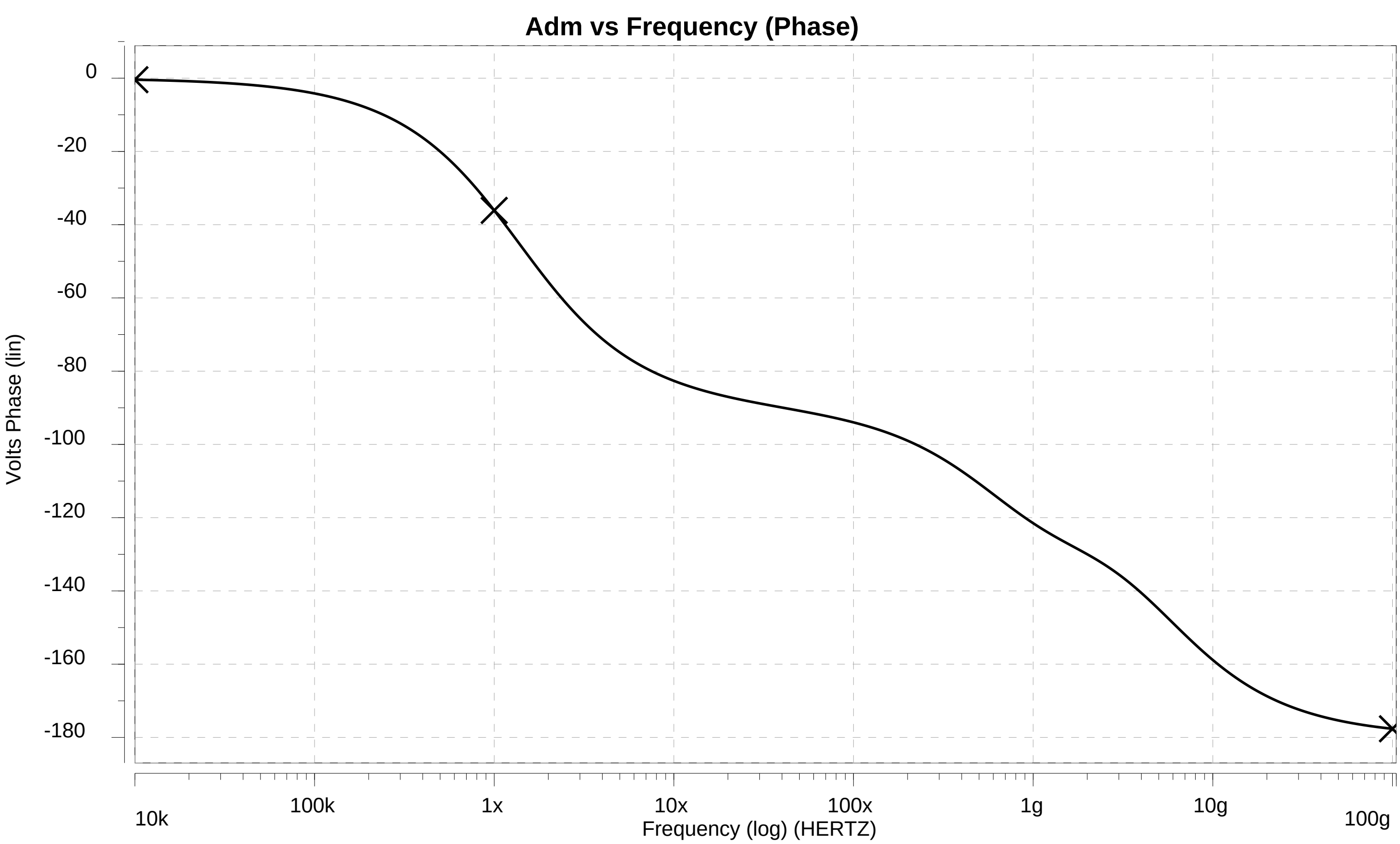
Acm vs Vcm (zoom)
Result (lin)
5m
0
-5m
-10m
-15m
-20m
-25m
-30m
-35m
-40m
-45m
-50m
Vcm,min
Hand Calc - Acm=-2.99mV/V
Actual Acm=-3.00e-03
Vcm,max
-1.5
-1
-500m
0
500m
1
1.5
Voltage X (lin) (VOLTS)

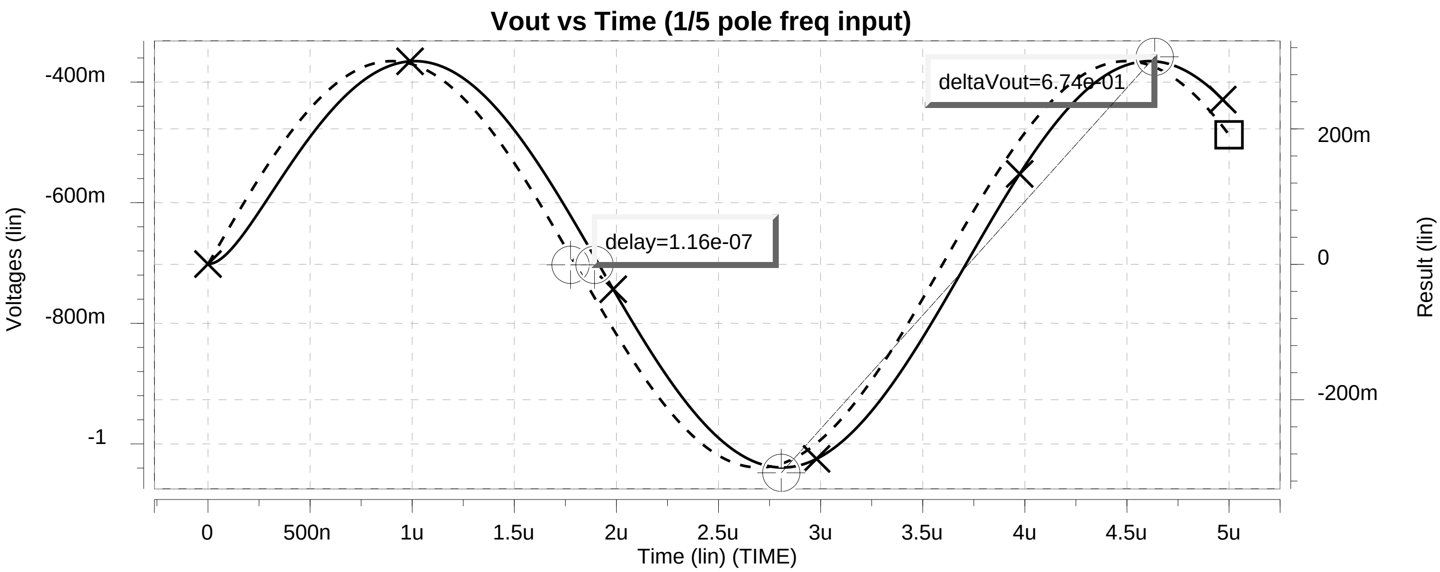
Vout vs Vcm
Voltages (lin)
-700m
-750m
-800m
-850m
-900m
-950m
-1
-1.5
-1
-500m
0
500m
1
1.5
Voltage X (lin) (VOLTS)

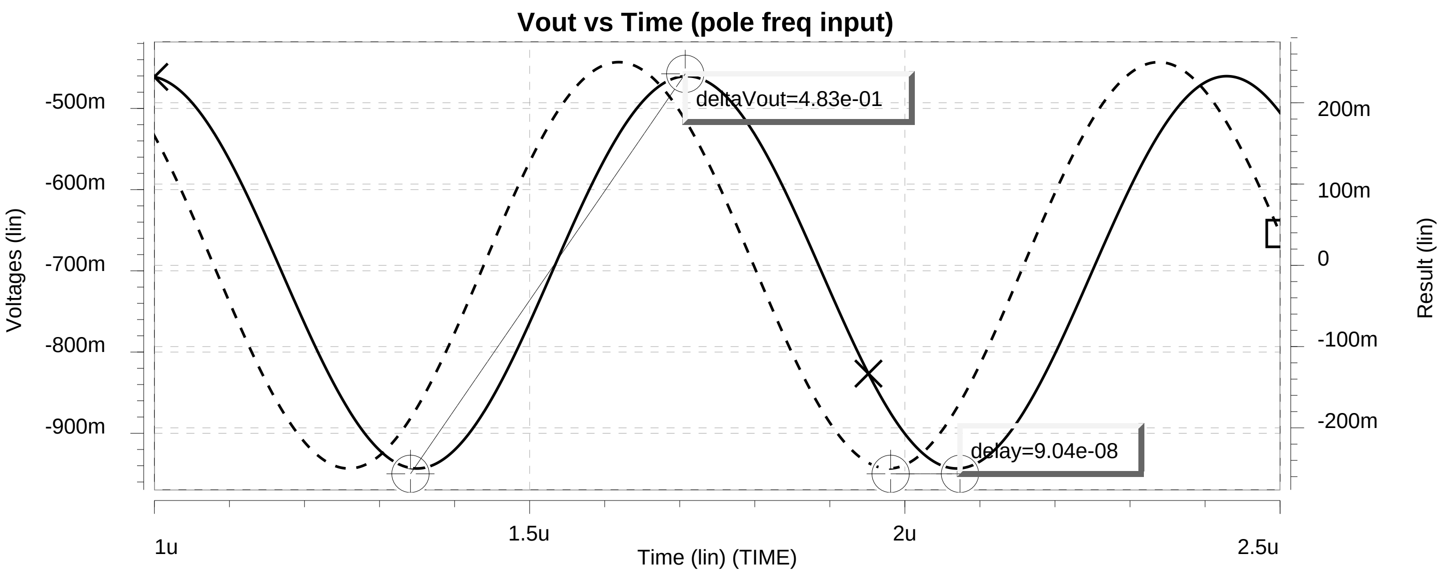


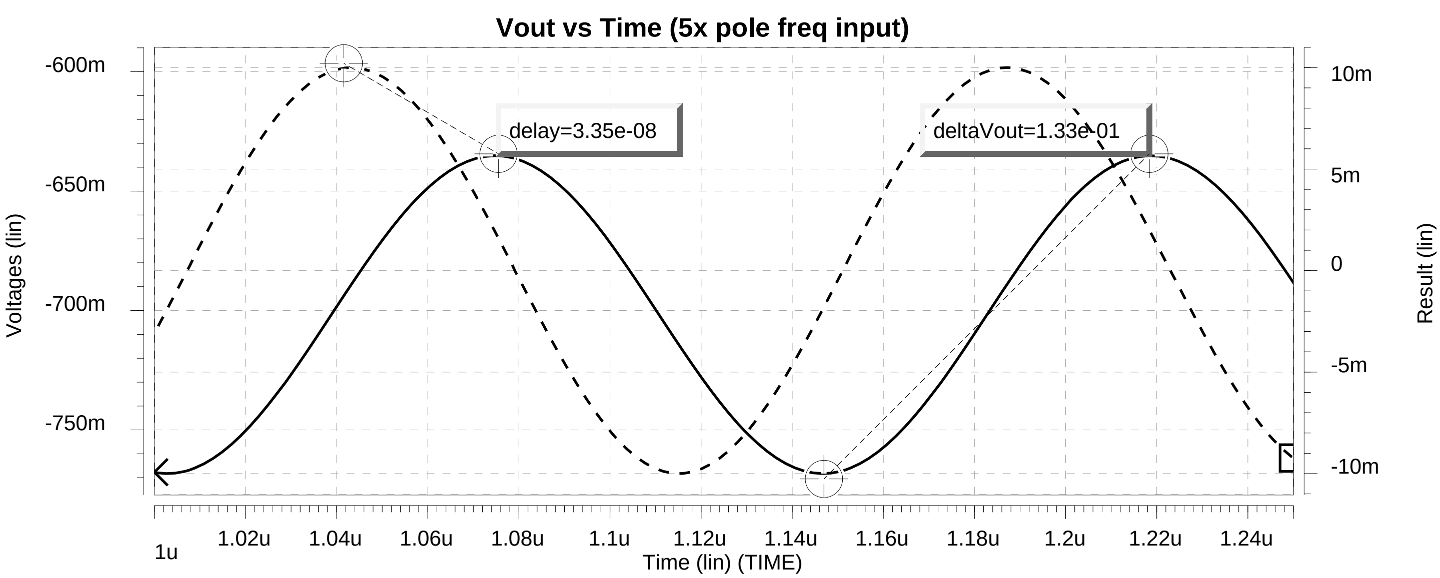
Adm vs Frequency (Magnitude)
Volts Mag (log)
100
10
1
100m
10m
1m
Calc Adm=333.3 V/V
Actual Adm=3.44e+02
Calc fp=1.39MHz
Actual fp=1.39e+06
Calc fu=0.46GHz
Calc fm=785MHz
Calc zm=1.57GHz
10k
100k
1x
10x
100x
1g
10g
100g
Frequency (log) (HERTZ)

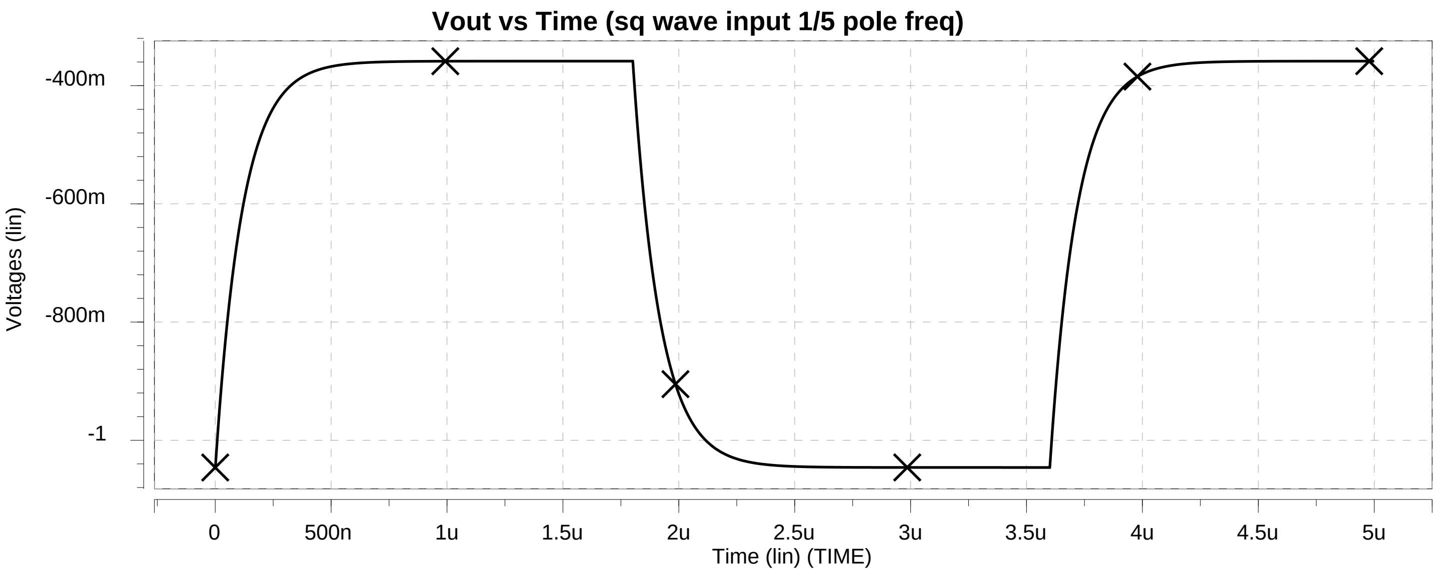



Adm vs Frequency (Phase)
Volts Phase (lin)
0
-20
-40
-60
-80
-100
-120
-140
-160
-180
10k
100k
1x
10x
100x
1g
10g
100g
Frequency (log) (HERTZ)

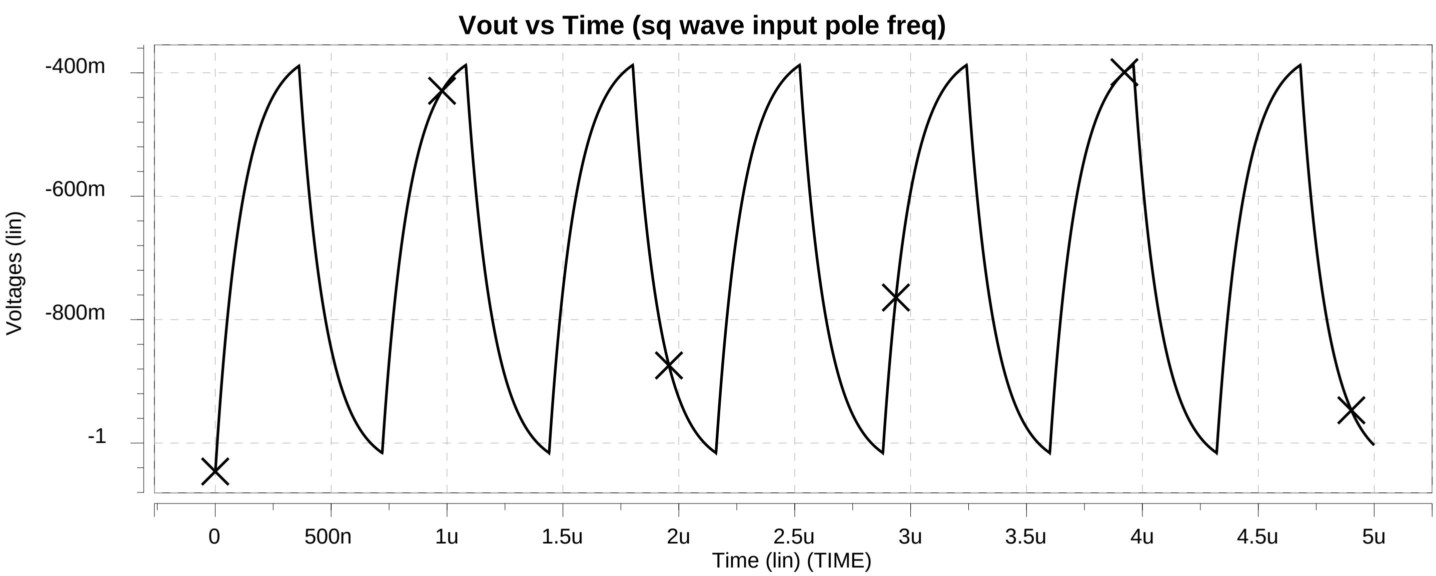

Vout vs Time (1/5 pole freq input)
deltaVout=6.74e-01
delay=1.16e-07
Voltages (lin)
-400m
-600m
-800m
-1
Result (lin)
200m
0
-200m
0
500n
1u
1.5u
2u
2.5u
3u
3.5u
4u
4.5u
5u
Time (lin) (TIME)


Vout vs Time (pole freq input)
deltaVout=4.83e-01
delay=9.04e-08
Voltages (lin)
-500m
-600m
-700m
-800m
-900m
Result (lin)
200m
100m
0
-100m
-200m
1u
1.5u
2u
2.5u
Time (lin) (TIME)

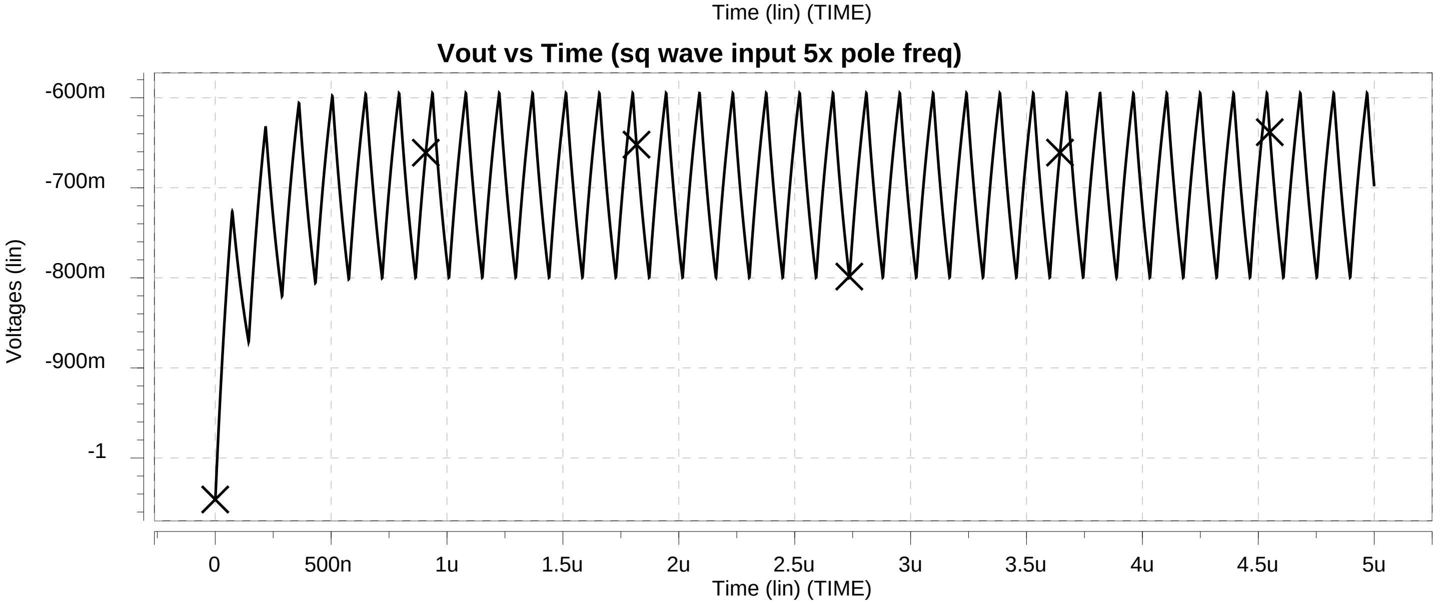

Vout vs Time (5x pole freq input)
delay=3.35e-08
deltaVout=1.33e-01
Voltages (lin)
-600m
-650m
-700m
-750m
Result (lin)
10m
5m
0
-5m
-10m
1u
1.02u
1.04u
1.06u
1.08u
1.1u
1.12u
1.14u
1.16u
1.18u
1.2u
1.22u
1.24u
Time (lin) (TIME)



Vout vs Time (sq wave input 1/5 pole freq)
Voltages (lin)
-400m
-600m
-800m
-1
0
500n
1u
1.5u
2u
2.5u
3u
3.5u
4u
4.5u
5u
Time (lin) (TIME)

Vout vs Time (sq wave input pole freq)
Voltages (lin)
-400m
-600m
-800m
-1
0
500n
1u
1.5u
2u
2.5u
3u
3.5u
4u
4.5u
5u
Time (lin) (TIME)

Vout vs Time (sq wave input 5x pole freq)
Voltages (lin)
-600m
-700m
-800m
-900m
-1
0
500n
1u
1.5u
2u
2.5u
3u
3.5u
4u
4.5u
5u
Time (lin) (TIME)

```
* EECS 140, Spring 2002
* HW 5 Solutions
* Simple opamp
*

* opamp subcircuit *
.subckt opamp inp inm out vdd vss
M1 vo1 inm vtail vtail PMOS1 W=2222u L=1u
M2 vo2 inp vtail vtail PMOS1 W=2222u L=1u
M3 vo1 vo1 vss vss NMOS1 W=277.8u L=1u
M4 vo2 vo1 vss vss NMOS1 W=277.8u L=1u
M7 out vo2 vss vss NMOS1 W=277.8u L=1u M=2
M8 out vbias vdd vdd PMOS1 W=444.4u L=1u M=10
M5 vtail vbias vdd vdd PMOS1 W=444.4u L=1u M=10
M6 vbias vbias vdd vdd PMOS1 W=444.4u L=1u
Rbias vbias vss 4.7k
.ends opamp

************************************************************************
**
* balun
*     converts diff/cm <---> balanced signals
*     (works both ways)
* terminals:
*     vdm         differential voltage
*     vcm         common-mode voltage
*     vp          positive terminal of balanced port
*     vm          negative terminal of balanced port
*
************************************************************************
**
*
.subckt balun vdm vcm vp vm
e1 vp vcm transformer vdm 0 2
e2 vcm vm transformer vdm 0 2
.ends

* opamp *
x1 vinp vinm vout vdd vss opamp
*x2 vdm vcm vinp vinm balun

* Supply voltages *
Vdd vdd 0 DC 1.5V
Vss vss 0 DC -1.5V

* Input voltages *
*.param vcm=0V
*Vdm vdm 0 DC 0V AC 1V
*Vcm vcm 0 DC vcm
Vin vinp 0 DC 1V

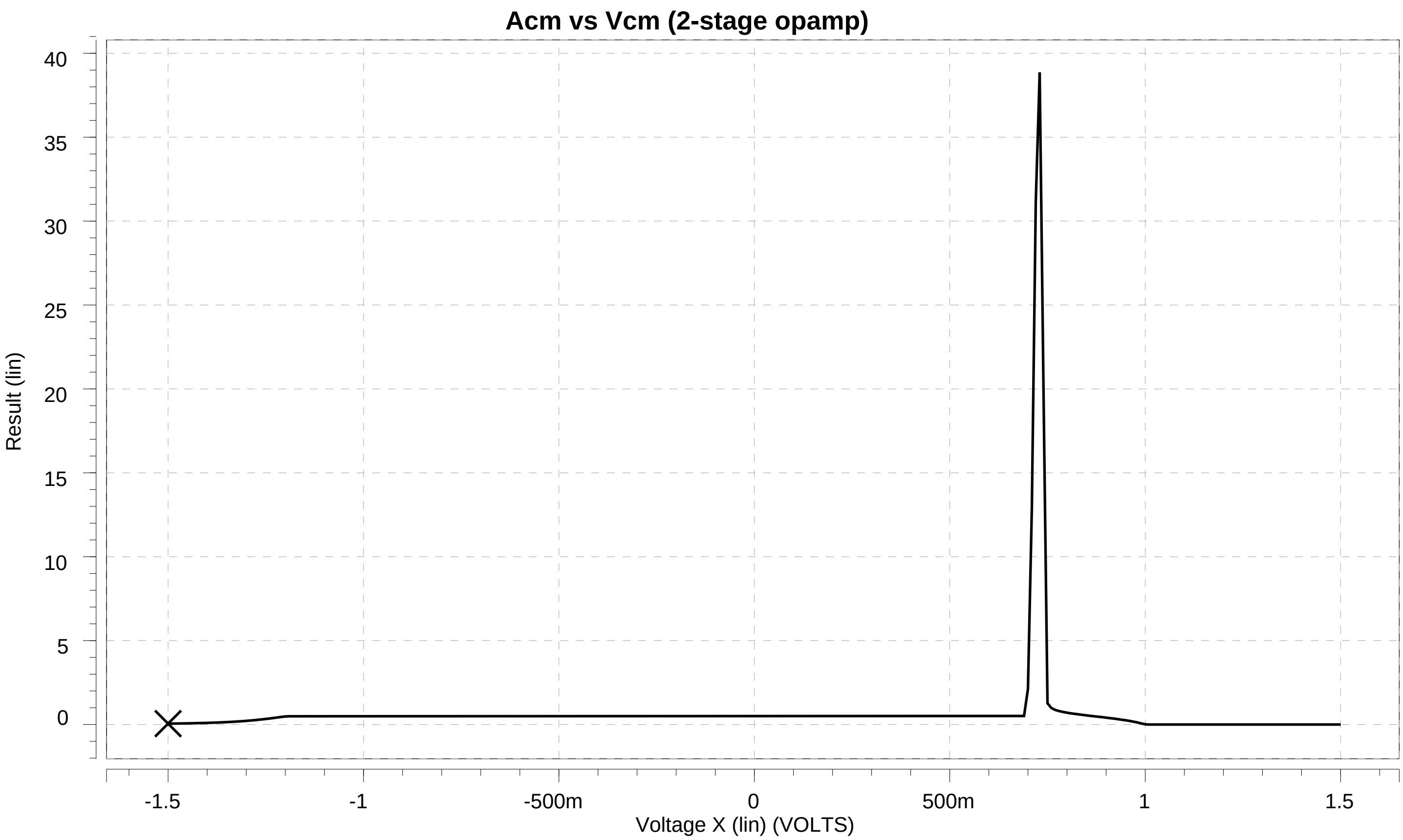
* Feedback and loads *
R2 vout vinm 1m
*R1 vinm 0 200
Cl vout 0 10p

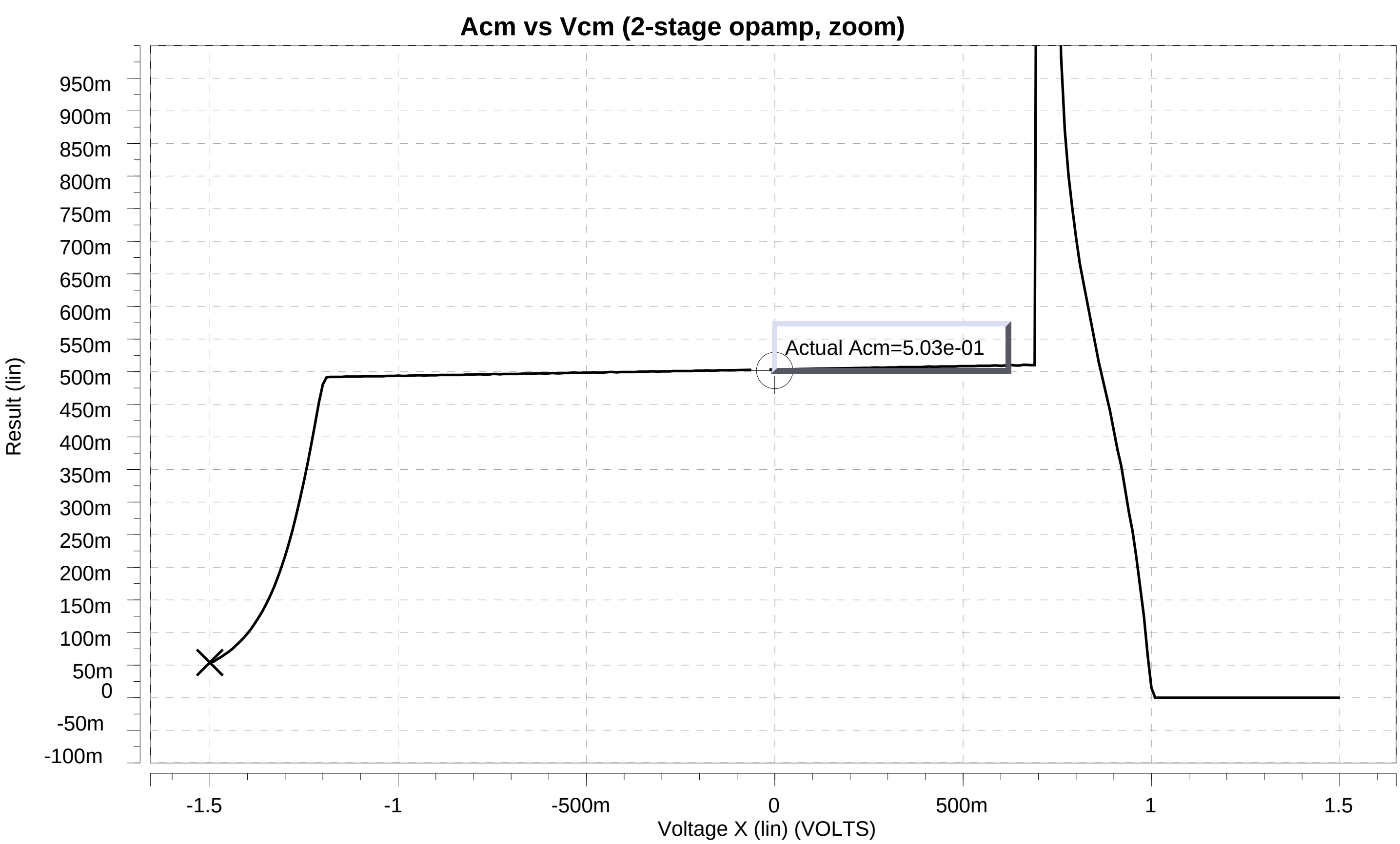
* Analyses *
.include '../lib/model2'
.OP
*.dc Vcm -1.5 1.5 10m
```

```
.dc Vin -1.5 1.5 1m
*.tf V(vout) Vcm
*.tf V(vout) Vdm
*.ac dec 100 10 100G
*.tran 0 5u 1n
.options dccap post=2 nomod brief accurate

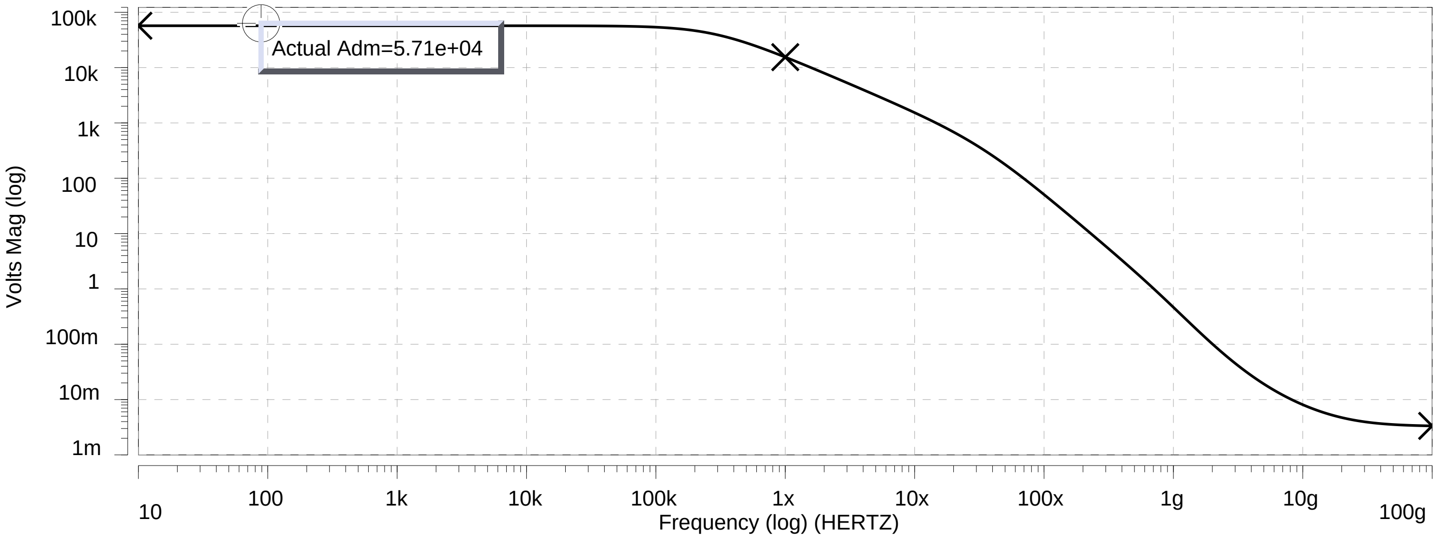
.probe V(vcm) V(vdm) V(vout) gain_dB=PAR('20*log10(V(vout)/V(vdm))')

*.alter vcm=-1V
*.param vcm=-1V
*.alter vcm=0.5V
*.param vcm=-0.5V
.end
```

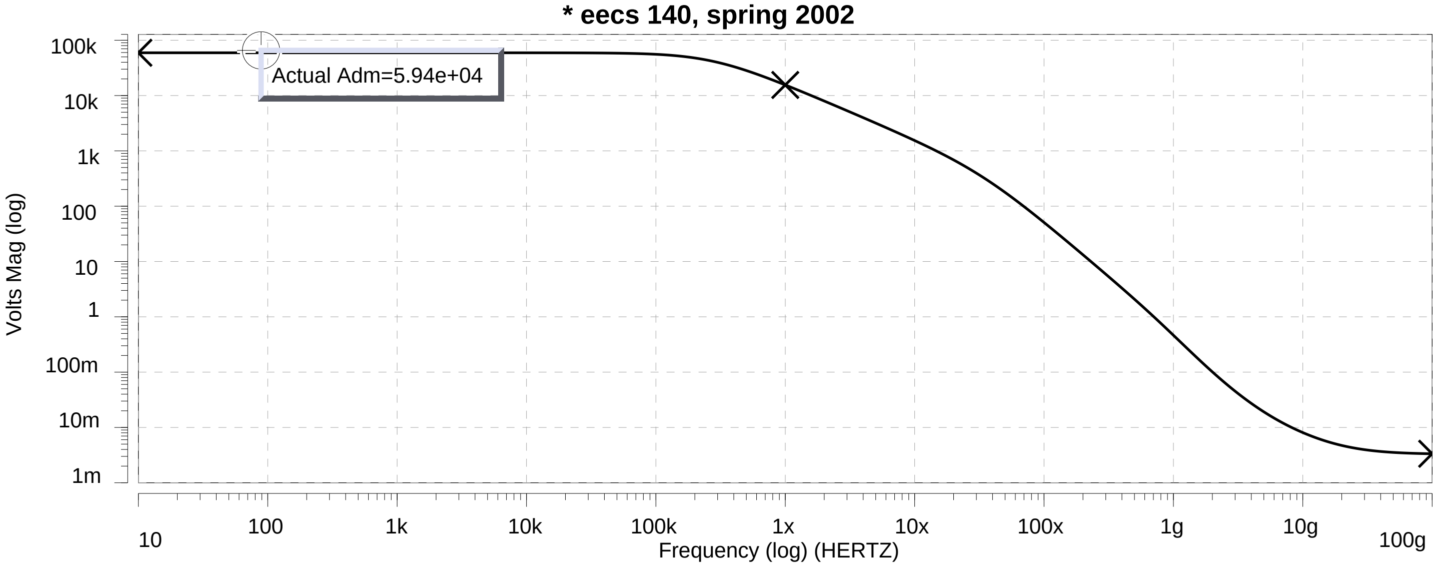

Acm vs Vcm (2-stage opamp)
Result (lin)
40
35
30
25
20
15
10
5
0
-1.5
-1
-500m
0
500m
1
1.5
Voltage X (lin) (VOLTS)


Acm vs Vcm (2-stage opamp, zoom)
Result (lin)
950m
900m
850m
800m
750m
700m
650m
600m
550m
500m
450m
400m
350m
300m
250m
200m
150m
100m
50m
0
-50m
-100m
Actual Acm=5.03e-01
-1.5
-1
-500m
0
500m
1
1.5
Voltage X (lin) (VOLTS)

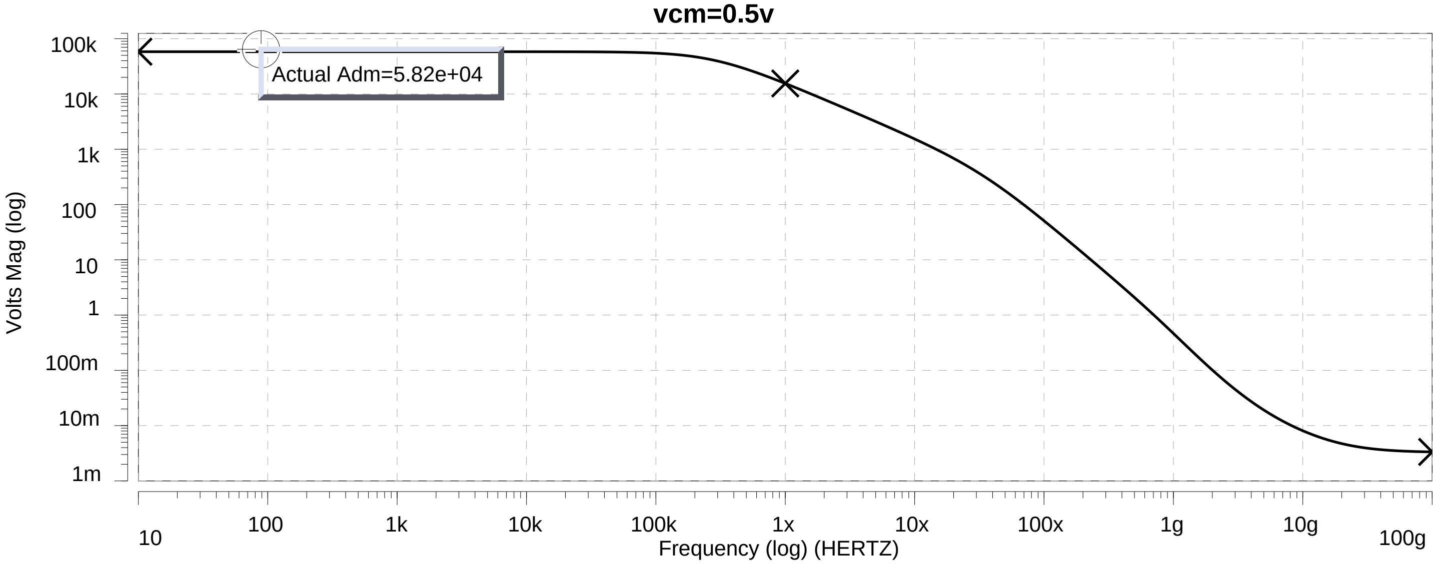
**vcm=-1v**

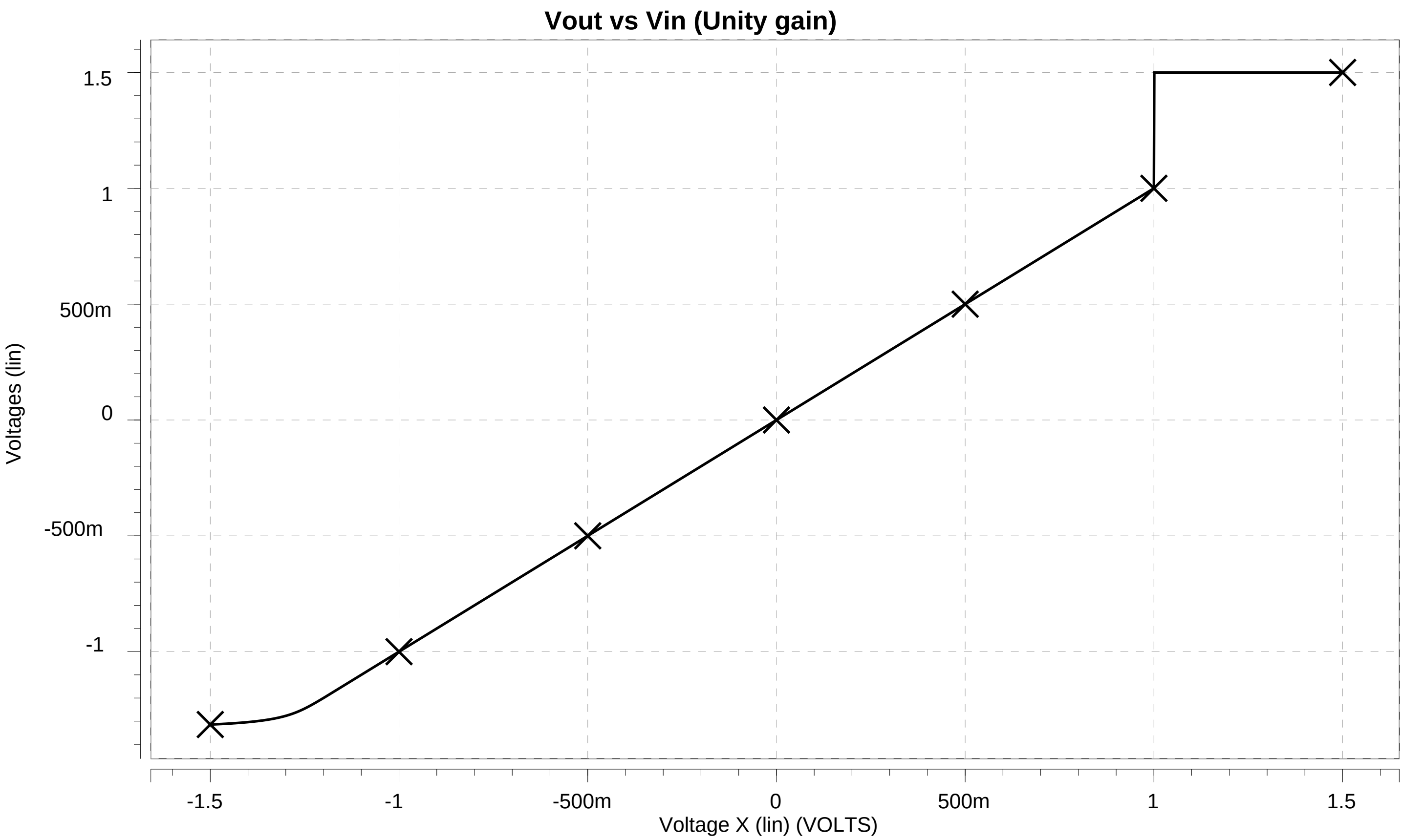



*** eecs 140, spring 2002**

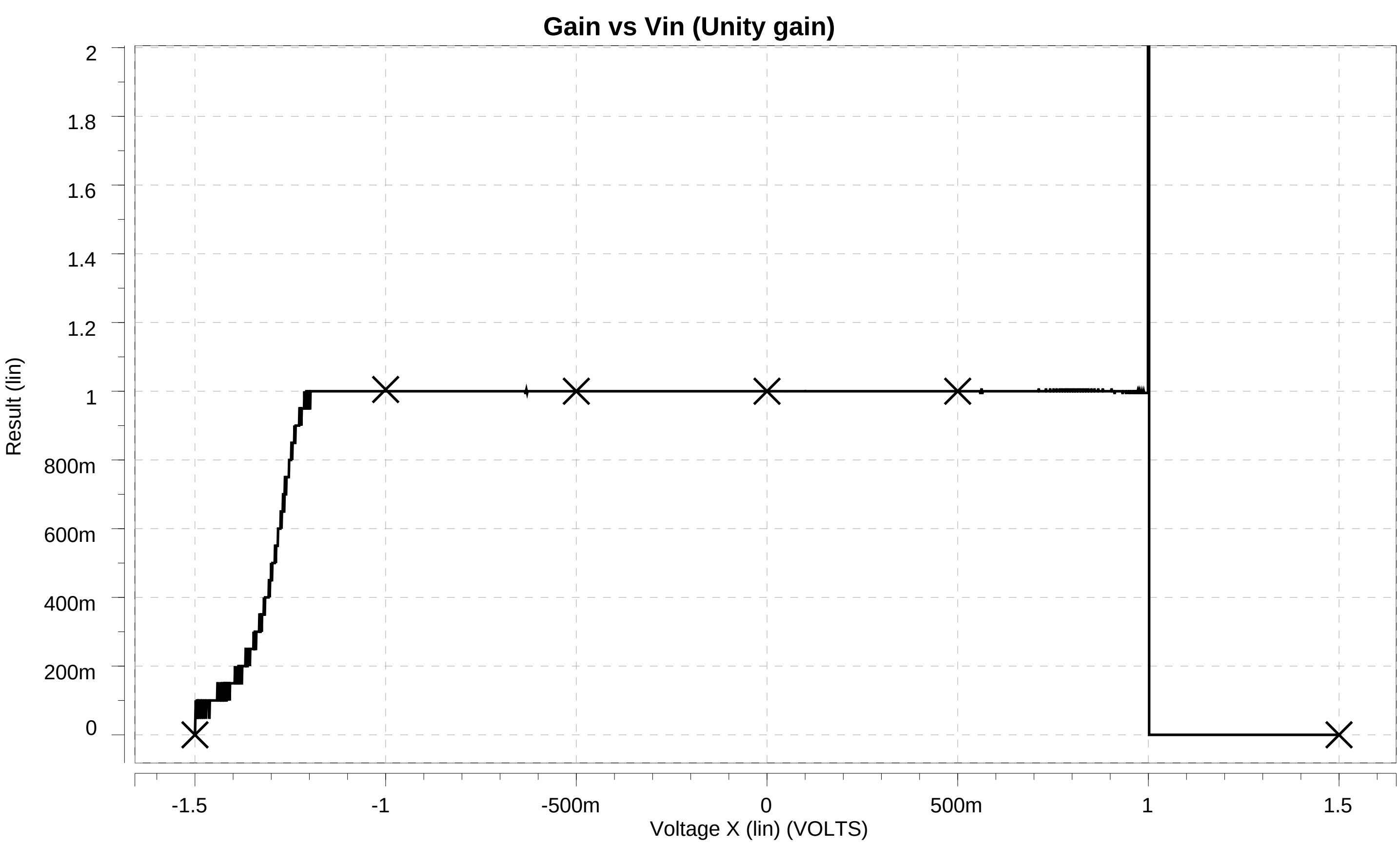



**vcm=0.5v**

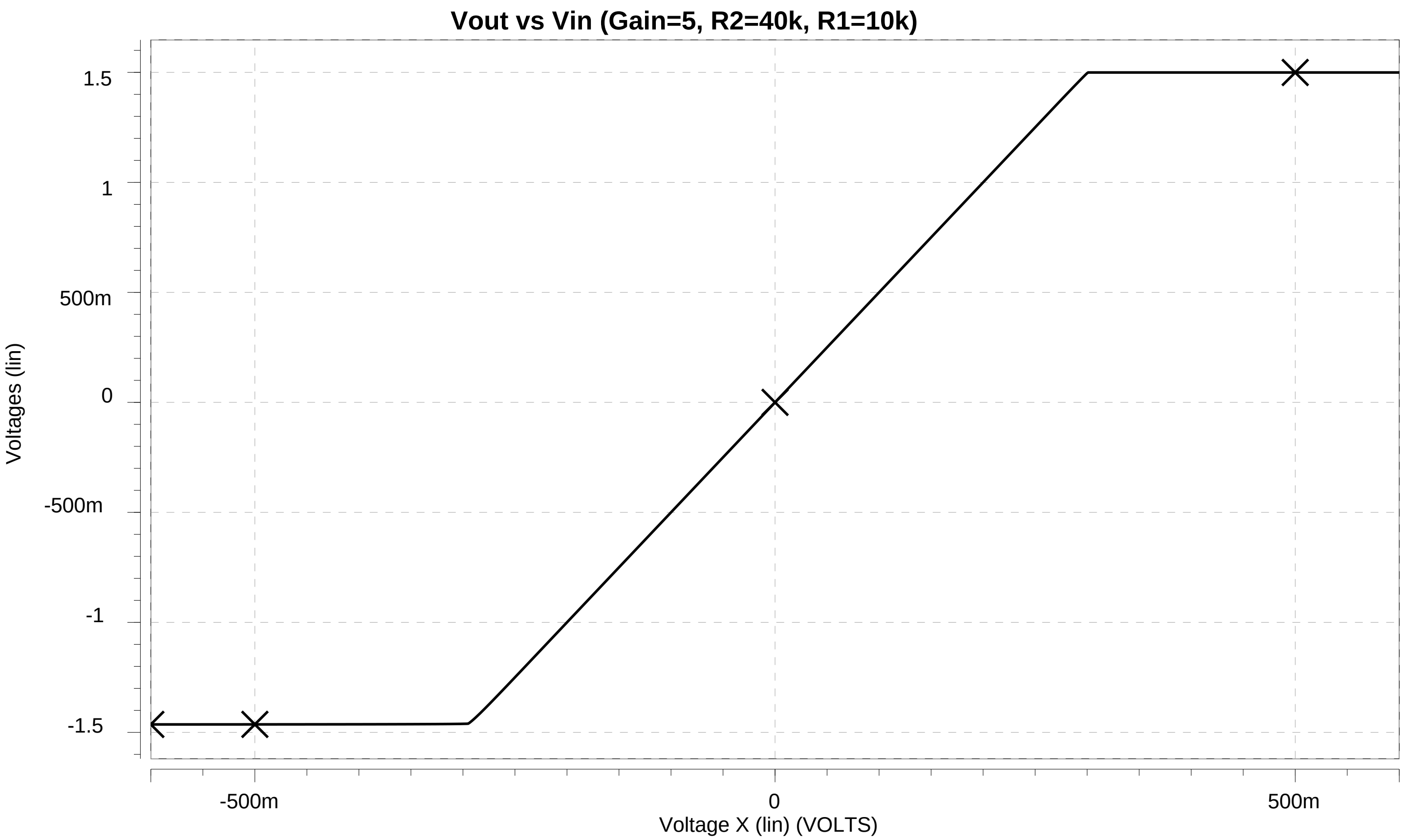




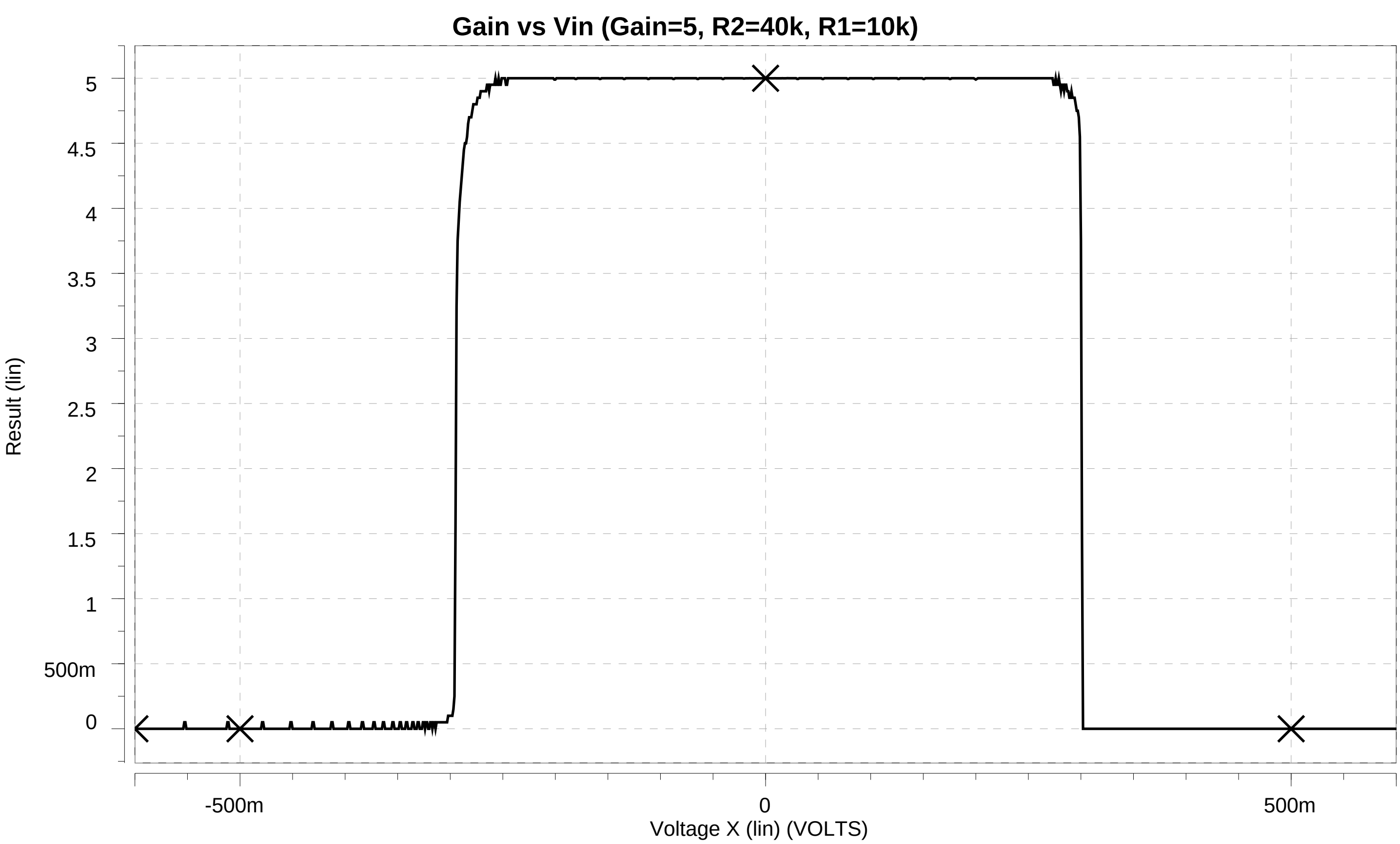
Vout vs Vin (Unity gain)
Voltages (lin)
1.5
1
500m
0
-500m
-1
-1.5
-1
-500m
0
500m
1
1.5
Voltage X (lin) (VOLTS)

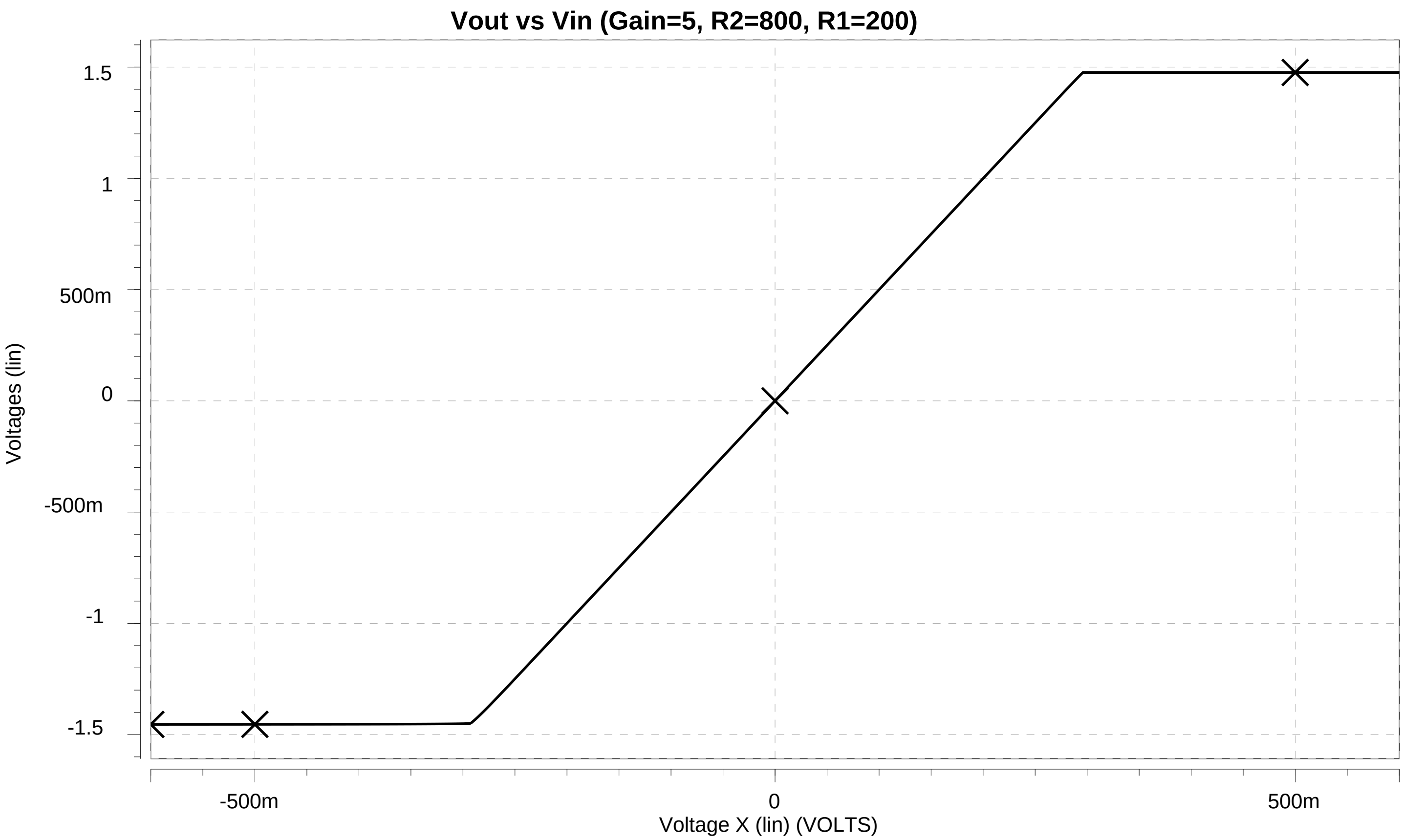
Gain vs Vin (Unity gain)
Result (lin)
2
1.8
1.6
1.4
1.2
1
800m
600m
400m
200m
0
-1.5
-1
-500m
0
500m
1
1.5
Voltage X (lin) (VOLTS)

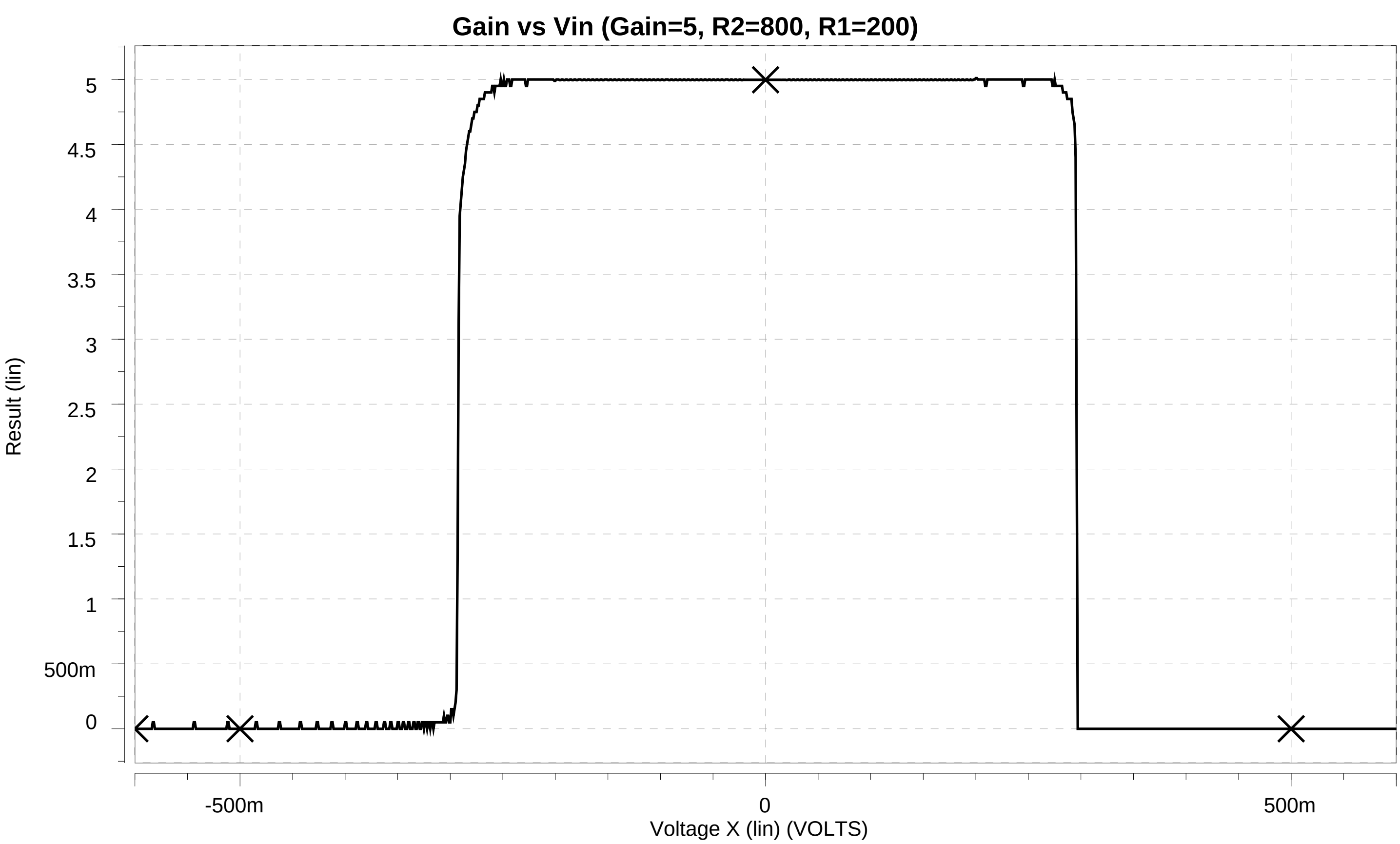


Vout vs Vin (Gain=5, R2=40k, R1=10k)
Voltages (lin)
1.5
1
500m
0
-500m
-1
-1.5
-500m
0
500m
Voltage X (lin) (VOLTS)

Gain vs Vin (Gain=5, R2=40k, R1=10k)
Result (lin)
5
4.5
4
3.5
3
2.5
2
1.5
1
500m
0
-500m
0
500m
Voltage X (lin) (VOLTS)


Vout vs Vin (Gain=5, R2=800, R1=200)
Voltages (lin)
1.5
1
500m
0
-500m
-1
-1.5
-500m
0
500m
Voltage X (lin) (VOLTS)


Gain vs Vin (Gain=5, R2=800, R1=200)
Result (lin)
5
4.5
4
3.5
3
2.5
2
1.5
1
500m
0
-500m
0
500m
Voltage X (lin) (VOLTS)