IDDQ TUTORIAL

Goals:

To show how a quiescent current supply test, Iddq, contributes to IC defect isolation.

To understand the challenges of the Iddq measurement.

To select from the available Iddq test methods, the ones which most practically reduce test time.

To Identify and validate circuit defect using failures analysis techniques and relate Iddq anomalies to the circuit flaw cause.

Objectives:

List the circuit requirements and test conditions for Iddq and describe how Iddq limit is derived.

Write the advantages and disadvantages of the three main categories of electrical tests DC, Function Iddq and AC in isolating defects.

List the order of defect types and their related symptoms and the characteristics of a valid Iddq failure.

Topics:

- Iddq Concepts
- Defects and Faults
- Iddq Test Pattern Generation
- Testing Methods
- Failure Analysis
- Review Questions

Iddq Concepts

13.0Introduction

CMOS IC makers were frustrated, because, oddly, some parts which were successfully tested failed to function in the field, while some other parts suffered performance degradation.

Two peculiarities were common to these escape (bad) parts:

(1) Iddq is several order of magnitude higher than the normal expected residual value of less than 1uA.

(2) Iddq value varies with the applied pattern between normal to abnormal.

A circuit defect, such as a short or partial transistor saturation, was suspected since CMOS is a nanowatt logic. See the example below for explanation of such case where a defective device eludes screening.

13.1 Example

An embedded inverter is shown in Figure 13.1 in which the source and drain of the p-FET are shorted.

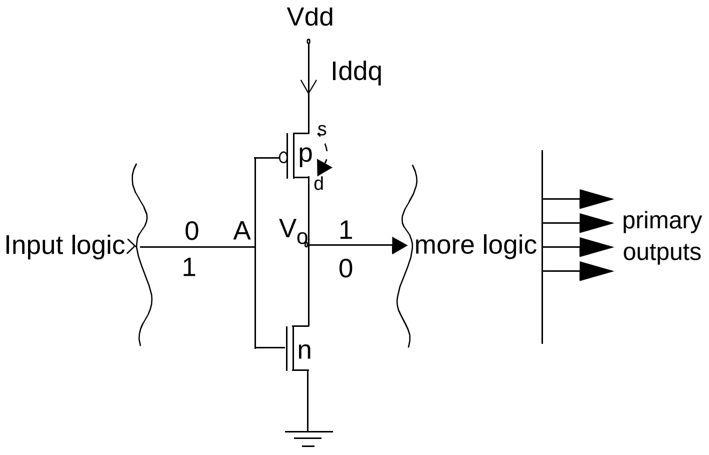

Figure 13.1 Embedded Inverter with source to drain defect

Ans (1): When an input logic 0 pattern is applied at A, the n-FET is turned off and the voltage appearing at the output correspond to logic 1. The value of Iddq is residual despite the existence of the short.

However, when an input logic 1 pattern is applied, the n-FET is turned on elevating Iddq.

Ans (2): Assume that the short is resistive. The equivalent circuit of the elevated Iddq is the voltage divider shown in Figure 13.2.

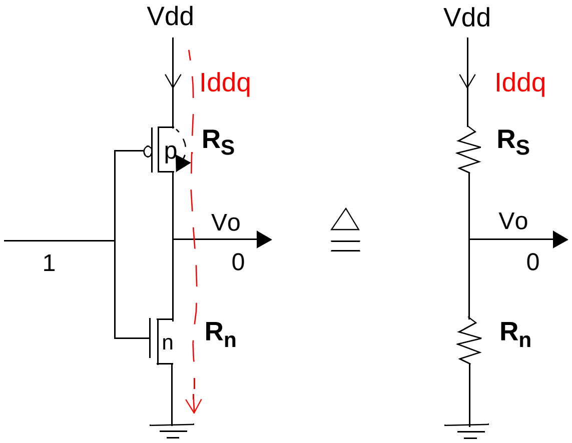

Figure 13.2 Equivalent Circuit at input logic 1

Rs is the short resistance and Rn is the output ON resistance of the n-FET.

By assuming that Rs/Rn is greater than 3, Vo turns to be logically correct for the subsequent gate. Although weak, this logic level allows function test to pass. Flaws due to one type of defects called bridging have impedances that could easily meet the previous assumption of Rs/Rn > 3.

If Iddq was monitored during logic 1 application, that defect would have been found. There would be no need to propagate and validate, as in conventional function, any signal at the primary outputs.

13.2 What is Iddq Testable?

To be able to use this powerful, and at first glance simple, detection method some requisites are needed namely:

- The device circuitry must be CMOS.
- The magnitude of background current from voltage dividers, embedded RAMs, pull-up or pull-down resistors, etc., must not be high enough to swamp the minuscule Iddq measurement.

- The voltage applied to any part of the circuit must not partially turn on the p or the n-FETs. Refer to the CMOS Transfer Characteristics.
- The part is rested from all external as well as internal transients at time of measurement.

13.3 The Advantages of Iddq

Diagnosing defects using Iddq offers several advantages because:

- Iddq is a cost-effective test method indispensable to identify some defects which are indiscernible by the conventional functional tests.
- The applied pattern needs only sensitize the node. This offers an immense computational reduction (1:7) over the conventional function test in pattern generation.
- It has been proven that the number of Iddq measurements required to reach a fault coverage greater than 90% is relatively small (2 digits).
- Iddq performs, to some extent, the job of burn-in by isolating those devices which will not survive in the field; the walking-wounded ones.
- Iddq enhances quality, shortens time-to-market and provides an efficient SPMC (Statistical Process Monitor and Control) for yield enhancement.

The types of potential problems detected by Iddq include:

- Process flaws: bridging, deformed traces, mask problems, incomplete etching, logically redundant defects.
- Design flaws: Floating gates, logic contention, mask generation errors.

13.4 Why doesn’t Iddq replace Function?

Iddq is intended to complement and not replace function for several reasons:

- Neither conventional function nor Iddq alone detects 100% of the defects.

- The Iddq timing is not set to run at the max specified frequency all the times due to test method constrains.
- The voltages and currents requirements Vil/Vih, Iol/Ioh, Vdd are different in conventional function than those in Iddq.

13.5 What Iddq does not detect

Iddq does not detect any defect which does not lead to an appreciable increase in the supply current such as:

- Highly resistive interconnects and open defects which do not elevate Iddq.
- Defects which inhibit the transistor from being conductive.
- Transmission gate defects which lead to weak logic.
- Dynamic interconnects such as capacitive and inductive coupling.

Defects and Faults

This section familiarizes the reader with some defects types in order to afterwards review Iddq pattern generation to then see how function and Iddq differ in the testing approaches.

Defects can occur anywhere on the wafer and at anytime during the making of the IC. They can occur as a result of an error in design, layout, mask, process, test overstress, packaging, handling etc. But the defect does not always manifest itself as a fault.

13.6 The Difference between Defects and Faults

Table 1: Defects and Faults

DEFECTS	FAULTS
Physical flaws	Logical errors
Not all defects cause faults	Not all faults cause malfunction at the time of test
Iddq finds defects directly (analog)	Function finds defects indirectly through logical faults (digital)

- If all defects cause faults then there would be no need for Iddq testing.

13.7 Short Defects on a Transistor Level

As shown in Figure 13.3, one could identify six possible short defects per FET namely:

Three shorts between transistor terminals.

Three shorts between each terminal and the bulk.

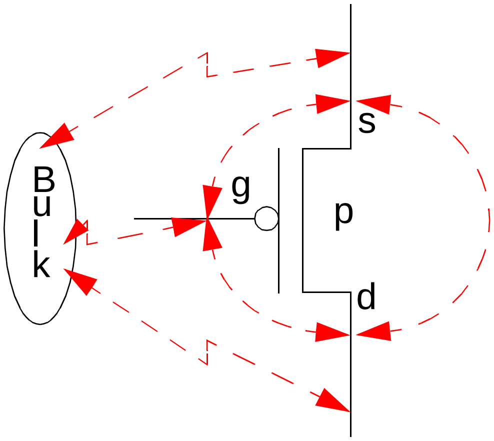

Figure 13.3 Six possible short defects per FET

A gate which contains 2 transistors has 6 X 2 or 12 possible shorts, a two-input NAND gate (2 P’s and 2 N’s) has 24 and so on. The defects that are within a gate are called **intra-gate** defects.

13.8 Short Defects on a Node level

Unintended connections between gates or signal lines are called **inter-gate** or **Bridging** defects.

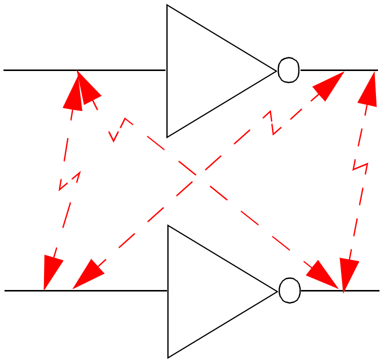

Figure 13.4 Bridging increases Iddq and could transform a combinatorial circuit to sequential

Bridging is caused by the unwanted presence of metal, polysilicone or other contaminants. This type of defect is proximity dependent, vertical or horizontal. Therefore expect bridging defects to be prevalent in submicron technology.

One common way to check for bridging is to let the node assume the complement state of its surrounding nodes. See Figure 13.5.

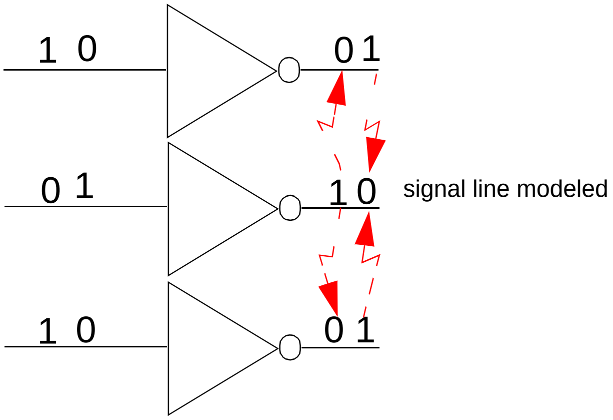

Figure 13.5 The signal line being modeled is driven to the complement of the others

The other forms of unwanted connections between signals are due to coupling and cross talk. These are discussed in the Noise Reduction chapter.

Not all defects in a circuit are due to shorts. There are defects which are due to opens and still lead to a high Iddq. E.G. in Figure 13.6, when the gate of P1 is open it is probably charged up due to the ratio of input impedances (mainly capacitive) causing P1 to be stuck. Refer to the Review Questions at the end of this chapter.

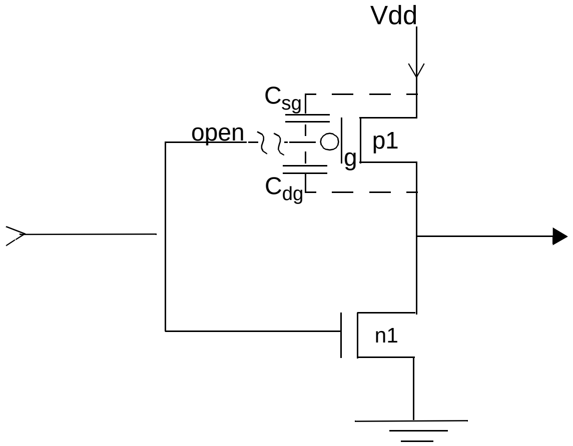

Figure 13.6 Open Defect

Open defects are more complex to model.

13.9 Types of Faults

By definition all malfunctions are due to faults.

A short between the source and drain of the p-FET is called “**stuck-at-one**” due to the type of logic to which it is stuck.

Conversely, a short between the drain and the source of the n-FET is called a “**stuck-at-0**” fault.

The generic name is Stuck-At-Fault **_SAF** or just **stuck-at**.

Stuck means that the FET is always conducting.

The “**stuck-at-Z**” or “**stuck-at-open”** is a fault caused by mainly an open gate. In some cases this fault increases Iddq by only a few uA.

13.10 Undetectable faults and Possible faults

The simulator for SAF pattern does not model all faults. There are some probabilistic measures taken in the generation of the pattern. In addition, some faults remain undetected for the following reasons:

- It is impossible to model the fault even after exhausting all input logic combination, such as for the logically redundant nodes.
- Some faults are known to be **undetectable** and are specifically excluded from the model, like the degraded signal level type.

- Some fault modeling requires a long CPU time (weeks).
- When the result of the simulation produces an immense amount of vectors, which is impractical for the tester to handle, such as in large sequential circuits.
- If the simulator times out before collapsing, it assigns unknown states to some nodes logic **_possible** defects. (Notice the difference between unknown states and don’t care).

Iddq Test Pattern Generation

There are three methods to generate the test patterns for Iddq testing.

- Generate using the existing, or a subset of, the SAF pattern.
- Generate using a dedicated Iddq pattern tool.
- Hand write the pattern.

13.11 Generate Using the Existing SAF Pattern

One method, FaultSim, uses the full SAF pattern and annotates the target vectors with labels. The pattern execution either halts at the label to do a static measurement or the timing is modified by extending the period, then strobing an Iddq representative voltage at the end of the period. The later is a high speed measurement and is discussed in the Functional Iddq section.

Another method, TestGen, generates vectors from a SAF pattern. The vectors that are classified by the simulator as possible detects or return unknown states are targeted.

QUIETEST is another efficient Iddq pattern tool. QUIETTEST first selects a subset from the SAF pattern, typically less that 1%, then recursively select the effective vectors as targets.

While the above methods imply generating SAF patterns first then work the Iddq patterns, it could be found more efficient to generate a customized Iddq pattern first to exclude the covered models from SAF and drastically unburden the model.

13.12 Generate Using a Customized Iddq Pattern

This method requires a specialized pattern generator and do not require a SAF pattern as a prerequisite.

Each target vector sensitizes as many nodes as possible and thus tremendously reduces the number of target vectors.

Statistically, one vector could initialize 50% of the node to logic 0 or 1.

13.13 Hand write the Pattern

As seen above, since few vectors could sensitize the majority of the nodes, a hand written pattern is not impractical to consider implementing.

Device knowledge, process and layout information is a must to perform such task. Analog conditioning, timing and formatting are to be considered as per the guidelines below.

Using this manual method, however, could be time consuming when some nodes require special handling to sensitize.

13.14 Iddq Test Pattern Generation Guidelines

In general, a pattern is composed of interleaving sets of conditioning vectors and test point vectors. The test point vectors are called the target vectors and must yield in a low current draw for a fault-free device. The following is a check list to assist the engineer during pattern debug or when hand writing patterns:

- Pull-up or a pull-down circuits must be deactivated at the targeted Iddq vector unless the target vector state is 1 for pull-up and 0 for pull-down. It is of good practice to select in the design, if one has to, only pull-up or only pull-down.
- In the DC static method, the final states of the DUT must not be conditioned to change. E.G. Internal busses should not Tri-State, outputs or inputs may not disturb the nodes to a different logic etc. This is handled in timing and formatting.

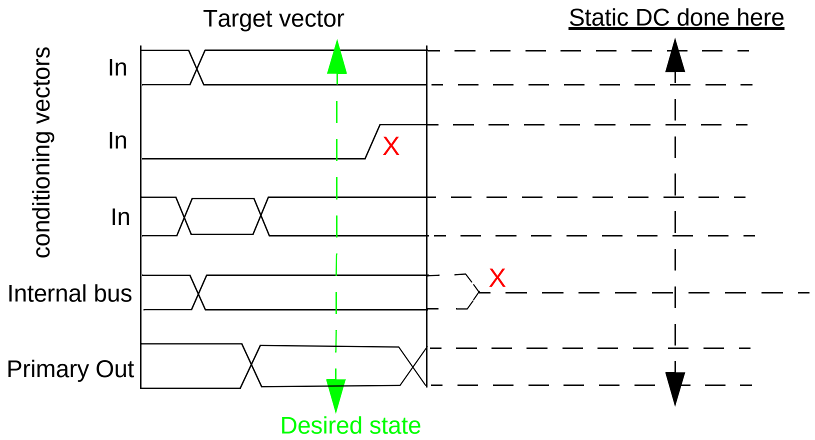

Figure 13.7 Inputs and Outputs switch (X) from desired state may invalidate Iddq

- When applicable, the pattern must bring the current drawing partitions of the circuit to a low power mode. In, say, embedded memories, the test or the standby mode is used to turn off the background current.
- The topological layout of the circuits must be considered for realistic checks on defects. This means that the patterns that are applied to the inputs are selected to account for grouping.
- Critical patterns, responsible for unveiling the modeled defect, must be included.

13.15 Fault coverage

When the pattern succeeds to sentitize all the nodes with logic 0 and logic 1, 100% fault coverage is realized. This measure is known as raw fault coverage. Coverage is calculated by the Simulator’s Fault-grading tools.

When the pattern sensitizes a node to one logic state and not the other, the node is classified as “Untestable”. For SAF model, untestable nodes include not only those node that could not be sensitized but also those which cannot be observed.

Test Methods for Fault Detection

13.16 Defect Detection Methods

In total there are four production, ATE-assisted, test methods used to find defects.

- Conventional SAF Function:Logic comparison
- AC Fault Test: Time Delays
- DC Iddq Test: Current measurement
- Functional Iddq Test: Voltage measurement

Additional methods are: optical liquid crystal, thermal, Ion Beam, acoustical and electromagnetic.

The combined goal of all four methods is to attain Zero Defects at the lowest cost and of course as soon as possible.

13.17 Conventional Function and Iddq Test methods

Below is the difference between conventional function and Iddq tests.

Table 2: Conventional Function Test versus Iddq test

	Conventional Function Test	Iddq Test
Node	Sensitize, Propagate then observe	Sensitize and observe
Flaw detection	Logic (Voltage)	Analog (Current)
Measured Pins	Primary Outputs	Vdd or Vss
Speed	DUT’s max. data rate	Slow for settling or interpolation

13.18 AC Fault Tests

This method, also known as Delay Fault test, is not an Iddq type of measurement per say. It is used to detect flaws which conventional Function and Iddq left behind like: the highly resistive interconnects, the weak logic and the open defects that do not appreciably increase Iddq. See details in the AC chapter.

13.19 DC Iddq Test

DC Iddq Test is a classic static measurement. The tester instrumentation PMU measures the supply current after the nodes are preconditioned to the target state.

13.19.1DC Iddq Testing Methodology

The following is a summary of the test procedure from the DC chapter summarized here for convenience:

- The tester is programmed to condition the device per the specifications for the test. Outputs are not loaded through any one of; the programmable loads, the tester drivers or external components. Input voltage levels Vil or Vih are equal to Vss or Vdd.
- A Timing and conditioning pattern is executed and halted at the target vector.
- The DPS provides the substantial Idd switching currents during the preconditioning stage. See Figure 13.8. After the pattern halts, the tester switches in the PMU, disconnects the DPS, waits for the programmed delay then performs the measurement.

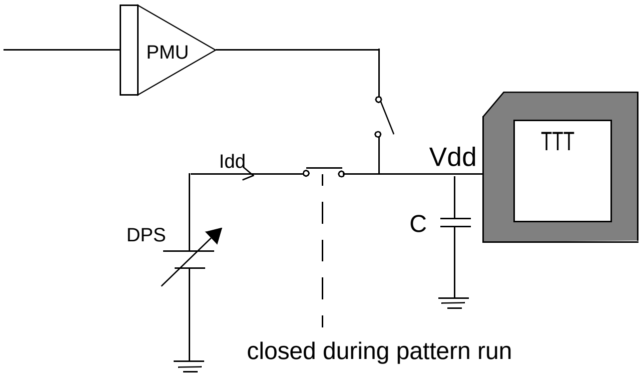

Figure 13.8 Tester DPS provides Idd during preconditioning

- In the cases where the PMU can handle the switching current (often in amps), the PMU is also Device Power Supply. The PMU measuring range is selected to provide the best resolution.
- The programmed delay is estimated for a stable Iddq reading. The measurement is compared with the threshold limit, Iddq(max).

13.19.2Calculating Iddq(max) limit

Iddq(max) limit is not a value normally usable from design, therefore it must be carefully estimated. If Iddq(max) is too loose, bad parts remain uncaptured and if too tight, some good parts are wasted.

A good way to obtain Iddq(max) limit is by plotting the reading of a large number of units (>100) then examining the relative scatter of data in the histogram. Some deltas are then added to the Iddq value associated with the highest percentile. Fortunately, the plot is not expected to look like the normal Gaussian distribution. See a typical plot below:

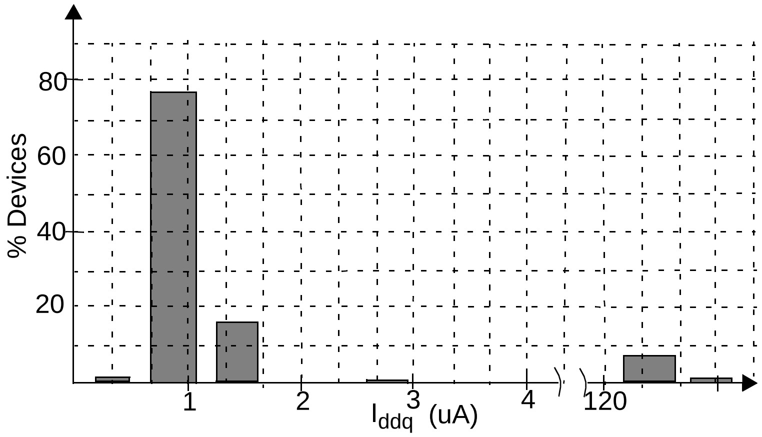

Figure 13.9 Iddq (max) Limit estimation

All values above this agreed upon limit falls in rejected region.

Most methods to predict Iddq (max) limit are predominantly “experienced guesses”

13.19.3The Advantages of the DC Method

The DC static test provides the most accurate Iddq measurement.

Talking failure analysis language, this measurement is robust by virtue of being a current versus being a voltage measurement.

The PMU is a standard instrument in ATE systems, therefore is readily available.

The measured value could be easily stored for analysis.

13.19.4The Disadvantages of the DC Method

The biggest disadvantage is Low throughput. Even after optimizing and reducing the Iddq measurements set, each test takes at least 10ms.

Because of the Vdd decoupling caps, instrument swapping (DPS-PMU) and the potentially huge switching pre-Iddq supply current, a fast and stable tiny current measurement is unlikely.

Some dynamic devices may not maintain the desired logic state until the measurement is captured. The result is logic switching which invalidates the node sensitization.

13.19.5The Challenges facing the DC Method

There are two principal challenges to address:

- Design a DPS with PMU accuracy inside a dedicated PE.
- Work around the laws of physics (Time constant) to reach a faster steady state in the presence of a large decoupling capacitance

A different approach, was therefore considered, namely, performing a Functional Iddq test.

13.20 Functional Iddq Tests

This method is not to be confused with the conventional function SAF test. It is basically an Iddq current to voltage conversion technique to speed up test times. It requires either an off or on Chip Current Sensor.

An off-chip current sensor is used here to illustrate the concept. Figure 13.10 shows and elemental sensor circuit that uses two components; a resistor and a comparator.

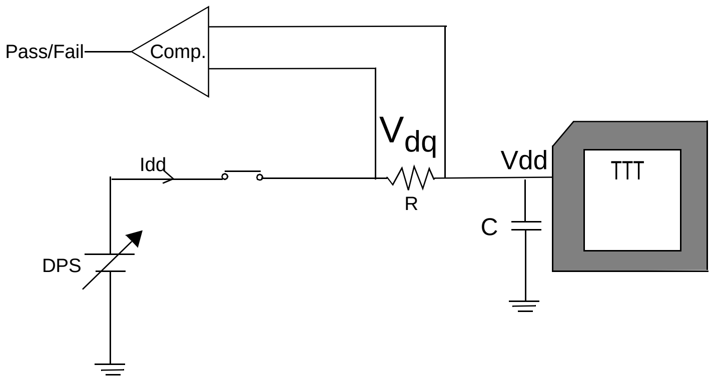

Figure 13.10 Elemental off-chip Current Sensor

The comparator sets a pass/fail flag to the ATE strobe subject to a voltage limit V_{dq} = Iddq(max) X R.

The resistor, being in series with the DPS, must be small enough to not degrade VDD at high currents and yet large enough to create an appreciable voltage V_{dq} at low currents.

Since these are non linear characteristics, an active voltage dropping circuit is more appropriate to use. The Quality Test Association Group, QTAG, has designed a standard off-chip tester-independent circuit for that purpose.

Nevertheless when a serial voltage dropping device is present together with wide current ranges, signal degradation occur.

Several circuits have been designed to settle with Iddq measurement challenges and a novel method was implemented in a circuit named the Keating-Meyer sensor, described below.

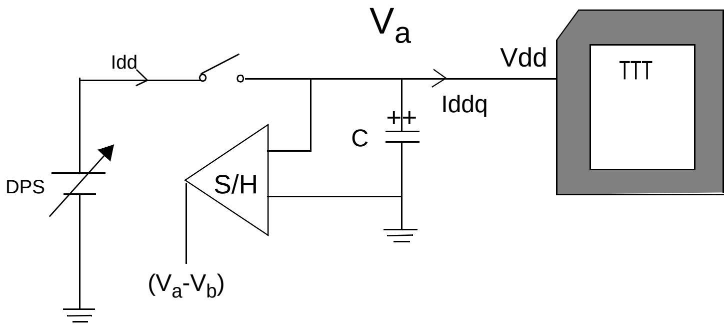

Figure 13.11 Keating-Meyers circuit

The DPS provides the high current during switching then it is isolated at the target vector leaving the large decoupling capacitor C the responsible of providing Iddq.

The voltage across C decays exponentially as in Figure 13.12. The sample and hold circuit acquires two voltage measurements Va and Vb within a short time interval ΔT determined by the resolution. The voltages are sampled during the Vdd voltage decay of the decoupling capacitor.

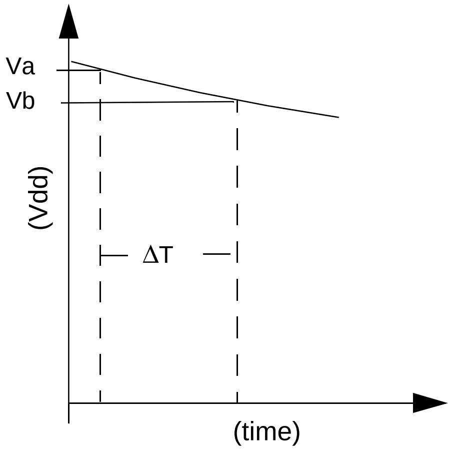

Figure 13.12 Exponential Vdd Decay

Iddq is then calculated using the equation:

I = C (Va-Vb)/ΔT. All elements in the RHS are known.

The other class of sensors are built on-chip and called BICS for **B**uilt **I**n **C**urrent **S**ensors.

BICS are active circuits designed on the chip and could be made to monitor Iddq at all times even in field operation. The DUT logic is advantageously partitioned with a dedicated sensor at each section and should any malfunction arise, the system is prompted for corrective action. Of special usefulness are BICS working with scan circuitry under DFT guide.

One circuit by Rius-Figueras uses proportional BICS which in its simplified form requires only three elements as shown in Figure 13.13: a Diode (VBJT) biasing a common base configuration (LBJT) and a sense resistor R_m.

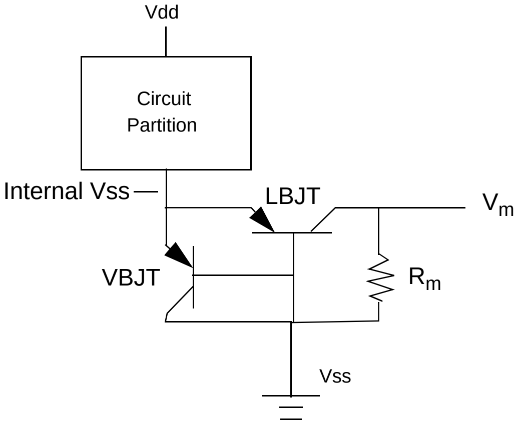

Figure 13.13 Elemental (on-chip) proportional Current Sensor

The monitored voltage V_m developed at the sense resistor R_m is proportional to Idd. However the internal Vss is offset by some 200mV to 600mV above the external signal ground depending on the size of Idd. There are now more complex circuits that guarantee an offset of 100mv.

BICS have clear advantages and they are slowly adapted due to high design cost, the required overhead for processing bipolar over CMOS technology, the amount of silicon real estate consumed and the impact on circuit performance.

13.20.1Testing Methodology

The testing methodology depends on the current sensor mechanism:

- The tester is programmed to condition the device per the specifications. Outputs are not loaded by any one of: the programmable loads, the tester drivers or by external components. Input voltages levels Vil or Vih are equal to Vss or Vdd
- A timing and conditioning pattern is executed and the strobe is enabled on the care pins at each target vector.
- At the target vector the sensors have their pass/fail flag set and transmitted through signal lines connected to the tester channels.
- The tester high speed comparator treats these flag channels as care pins. Any failed flag interrupts the tester CPU and stops further pattern execution.
- The failure results are displayed by the datalogger and indicate the failed logic, the failed channel, the vector count and the relative vector location in the pattern.

13.20.2Advantages of Functional Iddq

- Reduced test time mainly due to the digitization (voltage) of an analog quantity (current)
- The Keating-Meyer circuit calculates Iddq by sampling (digitize and interpolate) prior to Idd settling time to increase the throughput.
- BICS failures point directly to the defective circuit partition.
- BICS are embedded in the chip and could continuously monitor defects in the field and alert for corrective action
- QTAG packages could be commercially ready
- Some testers make available dedicated Iddq PE(s)

13.20.3Disadvantages of Functional Iddq

- All added sensor circuits are limited by the testing environment’s noise and resolution.
- Any methods that uses a voltage reference Vref as a compare limit require correlation and calibration not only on lot to lot but also tester to tester basis
- Any voltage dropping device, like in BICS, creates noise margin and speed degradations even after all design, layout and process difficulties are dealt with
- All methods that attempt to speed up test time by reducing or relocating the bypass capacitor(s) are production unoriented. The bypass capacitor is here to stay. Its value is always increasing. Its location is at closer proximity of the DUT.

Failure Analysis

Failure analysis is carried on at different phases of the IC life namely: During design verification, process evaluation, wafer tests, final tests and field rejects verification. The sooner a defect is identified the more effective is the corrective action to fix the problem.

The test engineer is principally involved at the wafer test where an escaped defect costs a bundle.

The second important phase is during final test to evaluate speed performances and analyse the handling and packaging induced defects prior to shipping.

The third phase is the field reject verification.

If the engineer’s task is only to verify failure, then it is preferable to deal with Iddq as a strong failure indicator over conventional function failures. A look at how many potential factors are eliminated in Iddq diagnostics can tell why?; relaxed timing, fixed input and output voltage levels, zero output loading and less noise.

On the other hand, if the goal is to isolate and identify in the hierarchical groupings of nodes the faulty one(s), further analysis are required. This is evident due to the small number of target Iddq vectors relative to the number of nodes.

The following is the electrical aspect of failure analysis which is greatly facilitated if:

- The circuit is designed with partial or full scan and follows the DFT rules.
- The target vector is mapped into the conventional pattern for validation
- The flaw detection is not erratic
- The measured quantity is not marginal

For erratic flaws and marginal measurements, it is advised to aggravate the condition through burn-in, maximum Vdd (or very low Vdd in the case of AC) or higher temperature.

In the mist of this analysis, one must also assess the realistic defects of the fabrication process. In CMOS the dominant failures are due to:

1) **Gate oxide shorts**

2) **Bridging**

3) **Open gates**

4) **Parasitic and Diode Leakages**

13.21 Gate Oxide Shorts Symptoms

Gate shorts are often resistive (>1KΩ) and non-linear. The location of the short determines the fault model.

13.22 Bridging Symptoms

Bridgings are resistive and vary between several hundred Ohms to several thousand Ohms. Bridging defects symptoms are:

- **Reduced noise immunity**. This is due to weakening of the logic. Vary Vdd or characterize Vil/Vih to reveal the vector that causes the worst reading.
- **Changing States**. Some bridging may feedback and create sequential logic causing the node to change state. Subsequent application of the test yields different Iddq results.
- **Oscillation and temperature rise**. The feedback may also create oscillation, heat-up the circuit or propagate signals in reverse.
- **Propagation delay deviations**. Deviations could be as low as one gate delay when compared to typical reading of good devices of the same lot. This could be impossible to discern without the use of serial scan.

13.23 Open Gates and Open Signals Symptoms

Depending on where the open is located, the results rely mostly on the floating conditions.

13.24 False Failure indicators

The test engineer must, at one point prevent diagnosis to get entangled in an endless search for a phantom defect. False or invalid readings surely lead that way.

The following are some pointers to check the validity of a measurement. The reader must be already familiar with many.

- **Repeatability of the measurement:** Is the measurement repeatable within the tester resolution? Examine if the variances are multiples of resolution.
- **Full Scale reached:** Is the measurement maxed out at the full scale of the measure range, therefore, invalid?
- **Reference value:** What does a golden circuit measure? Is the programmed limit adequate. Where does the reading fit in the Iddq distribution?
- **Data collection Method:** Is there a difference in the measured value between debug, test or datalog modes. Could the measurement be repeated on the bench?
- **Test induced errors:** What is the measurement at the target vector without a device? without a load board? Caution! ESD and EOS may be hunting.
- **Device conditioning:** Are the outputs isolated from the tester? What are the measurements of the input voltages.
- **Device response:** Is the device in quiescent state? The devices that contain internal keep alive circuitry provoke a sudden increase in Iddq reading even with the deliberate absence of the external clock.
- **Debug tools:** Was the scope used on power, outputs and also input pins to verify the quietness at the target vector. A feedback may create oscillation, heat-up the circuit or even propagate signals in reverse.
- **Alternate validation:** After a failure mechanism is presumed validate it through alternate methods? Does gross function or other tests pass?
- **Aggravation:** Examine the effect of applying the minimum and maximum voltages and temperature. Be careful not to destroy an already weak device and burry the early evidence of a failure mode.

- **Eye-witness:** To confirm the existence of a defect Optical liquid crystal, acoustic and electron beam diagnostics are used. The subject is beyond the scope of this discussion.

Review Questions

Ten selected questions are used in group classroom exercise. The remaining ones are assigned as homework with answers handled on the next day following the lecture.

1) List the type of devices and the test requirements necessary for Iddq

2) Is the Iddq(max) limit linearly proportional to the number of circuit nodes? Explain your answer. (Hint: Leakage equation and process integration.)

3) In an Iddq plot, the x axis contains the value of Iddq and the Y axis the percentile. Is a Gaussian distribution expected? Sketch your expectation and explain why.

4) A good way to determine the Iddq(max) limit is to test a large number of units and add some deltas to the value of the maximum percentile. One can argue that if the circuit has a design flaw, which is unknown to engineering, then the derived Iddq(max) limit is a misleading limit to use. Show the invalidity of such argument.

5) Consider the logically redundant circuit in Figure 13.14, where Q is true when I_{1-3} are true and false otherwise. SAF method will not detect if G_2 is stuck at one. Give two reasons why Iddq is necessary for this design eventhough the circuit works despite the defect?

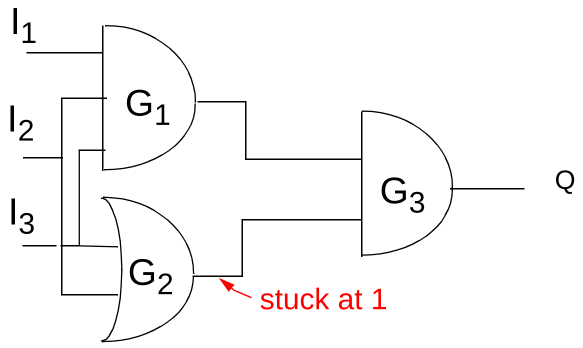

Figure 13.14 Iddq detects this defect and SAF does not.

6) What is the difference between a defect and a fault? Do all defects cause faults? Do all faults cause malfunction?

7) What is the difference between SAF (Stuck-At-Fault) and Stuck open and which defect causes which fault? Hint: Choose: shorts, open Gates

8) Explain the main reason why there are very few Iddq vectors and list three DFT guidelines which facilitate Iddq defect diagnosis. (see the DFT chapter for reference)

9) What are the two ATE major impediment in implementing a production oriented Iddq test?

10) Why are open defects more difficult to analyse than short defects. In Figure 13.6, if Cdg = 100*Csg, will p1 conduct?

11) What is the value of Iddq in Figure 13.15 with a Gate to Source bridging defect of 1kΩ. If the drive node can supply a max of 2mA, does Iddq increase or decrease?

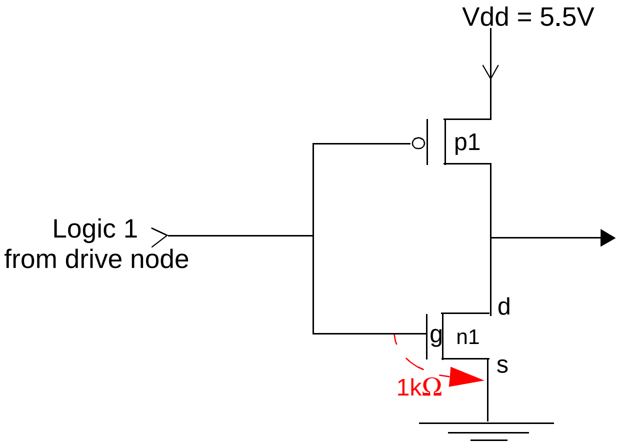

Figure 13.15 Gate to Source bridging

12) Write the advantages of the Keating-Meyer current sensor.

13) List three reasons on why BICS are preferred over the external (off-chip) current sensors? Where are BICS added in an n-well design, on the Vdd or the Vss line?

14) Write the advantages and the drawbacks of sensing the quiescent supply current from Vss (Issq) instead of from Vdd (Iddq) terminal in digital circuits.

15) What could cause the Iddq to have a positive but much less than expected value, a slightly negative or a considerably negative value? Note that the conventional current is positive when current flows from Tester to DUT.

16) List two effective ways to reduce test time when using the PMU.

17) List three different techniques used to obtain a stable Iddq measurement while maintaining throughput.

18) Write a descending order of the predominant defects in CMOS?

19) What are the characteristics of valid and invalid Iddq measurements?