



## Cadence Design Systems

### GPDK 45 nm Mixed Signal GPDK Spec

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## Revision History

### DRC Revision History

#### RELEASE NOTES FOR THE 45nm GPDK

##### VERSION 4.0 (17 JUNE 2014)

- gpdk045 IC615 library built natively with IC6.1.5 ISR17 release code
- Following CCRs has been fixed (27 ccrs)  
1287271,1283169,1256253,1254045,1254038,1245309,1237646,1183733,  
1170331,1126098,1113873,1101516,1094783,1090381,1079752,1037745,  
1035602,1027840,1027316,997831,990813,987559,981093,980054,980053,  
980051,959147
- Major changes:-  
MOS gates are now weak connect instead of must connect.  
Modified pvLVS deck, few new features has been added.  
pvfILL deck by Ray/Nalayini has been included.  
Model (resistor) file modified according to CCR 1245309

##### VERSION pre-release (15 DEC 2011)

- gpdk045 IC615 library built natively with IC6.1.5 ISR8 release code
- Following CCRs has been fixed,  
914090, 916997, 919813, 919964, 933415, 934958, 940090,  
940191, 962137

##### VERSION 3.5

- gpdk045 IC615 library built natively with IC6.1.5 ISR4 release code
- Added Fluid Guardring support to technology file (CCR884149)
- Modified liblnit files to set various tool defaults (CCR910688)
- Added techDerivedLayers to techfile to support substrate extraction and poly cutting diffusion. Added new layers to virtuosoDefaultExtractor Setup Constraint Group (CCR875571/911171))
- Modified MOS pcell to add additional gate pin when GateConnection != None (CCR911205)
- Added ASCII techfile named tech\_gpdk045.tf in the gpdk045 library (CCR869154)
- Modified PDK to have/use hspiceD views instead of hspiced (CCR887688) (only mimcap)
- Added 'soce' directory and data to support digital place and route (CCR869153)
- Corrected Assura DRC rule deck for end-of-line space (CCR868717)
- Corrected PVS LVS rules for the symmetric inductor (CCR890569)
- Moved rcx data from assura to qrc directory. It can be used for PVS/assura.

##### VERSION 3.0

- gpdk045 IC615 library built natively with IC6.1.5 release code
- Added WPE parameter in assura, pvs LVS decks.
- Added new antenna rules in tech file (815543)
- Added taperHalo constraint in virtuosoDefaultTaper in techfile (820934)
- Added minWidth and minSpacing rule for all 4 VT layers.  
Modified techfile and DRC deck to adopt this addition.
- Modified the assura\_tech.lib file and also added pvtech.lib for PVS.  
(847441)...

# Introduction

This document defines the Design Rules and Electrical Parameters for a generic, foundary independent 45nm CMOS Mixed-Signal process.

This document is divided into three sections:

- \* CMOS Digital Core Design Rules

describes the widths, spacings, enclosures, overlaps, etc. needed to create the physical layout of the core section of a digital CMOS design.

- \* CMOS I/O Design Rules

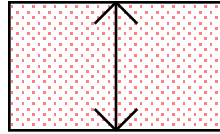
describes the widths, spacings, enclosures, overlaps, etc. needed to create the physical layout of the I/O section of a CMOS design.

- \* CMOS Digital Electrical Parameters

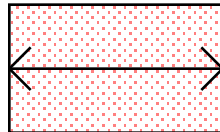
describes the electrical parameters of a digital CMOS design.

# Terminology Definitions

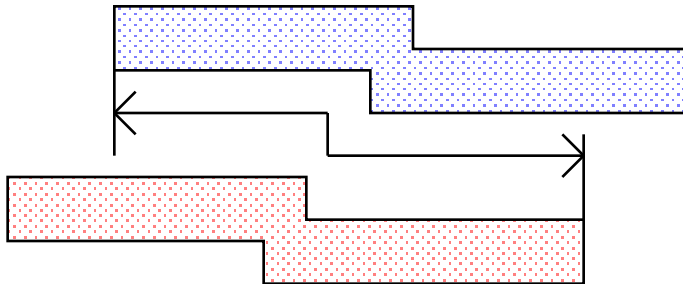
Width - shortest distance from the inside of the edge of a shape to the inside of the edge of the same shape.



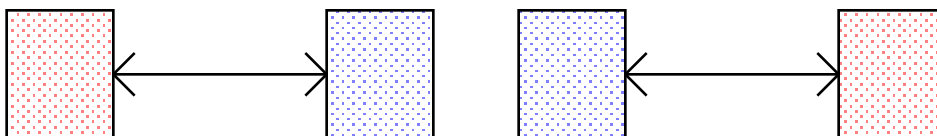
Length - opposite of Width - the measurement of the longest edge of a shape.



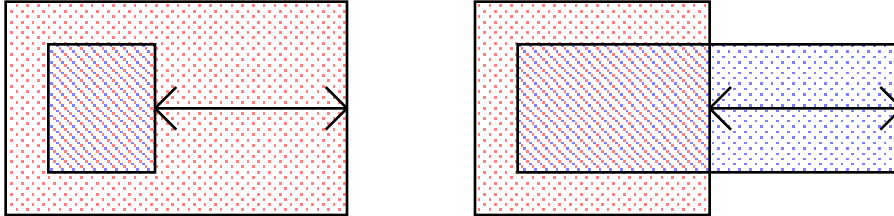
Parallel Run Length - the distance two shapes maintain a spacing less than the check value.



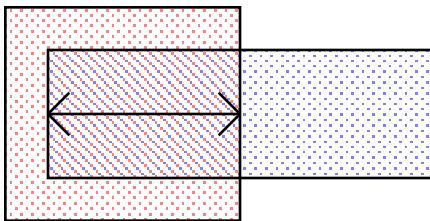
Spacing - distance from the outside of the edge of a shape to the outside of the edge of another shape.



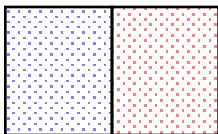
Enclosure - distance from the inside of the edge of a shape to the outside of the edge of another shape.



Overlap - distance from the inside of the edge of a shape to the inside of the edge of another shape.



Butting - outside of the edge of a shape touching the outside of the edge of another shape.



# Layer Descriptions

This table describes the layers used to create devices.

Comment Table

Layer Name	GDSII Stream Number	GDSII Data Type	DFII LSW Name	DFII Layer Name	DFII Layer Purpose	DFII Layer Number	DFII Purpose Number	Description
Bondpad	36	0	Bondpad	Bondpad	drawing	95	252	Bonding Pad
CapMetal	14	0	CapMetal	CapMetal	drawing	97	252	MiM capacitor metal
Nburied	19	0	Nburied	Nburied	drawing	18	252	N+ Buried Layer
Nhvt	18	0	Nhvt	Nhvt	drawing	11	252	NMOS High Vt
Nlvt	26	0	Nlvt	Nlvt	drawing	26	252	NMOS Low Vt
Nimp	4	0	Nimp	Nimp	drawing	12	252	N+ Implant
Nwell	2	0	Nwell	Nwell	drawing	6	252	Nwell
Nzvt	52	0	Nzvt	Nzvt	drawing	15	252	NMOS Zero Vt
Oxide	1	0	Oxide	Oxide	drawing	2	252	Active Area
Oxide_thk	24	0	Oxide_thk	Oxide_thk	drawing	4	252	1.8V Active Area
Phvt	23	0	Phvt	Phvt	drawing	13	252	PMOS High Vt
Plvt	27	0	Plvt	Plvt	drawing	27	252	PMOS Low Vt
Pimp	5	0	Pimp	Pimp	drawing	14	252	P+ Implant
Poly	3	0	Poly	Poly	drawing	10	252	Poly
SiProt	72	0	SiProt	SiProt	drawing	16	252	Salicide Block

**Table 1: Device Layers**

This table describes the layers used to interconnect devices.

Comment Table

Layer Name	GDSII Stream Number	GDSII Data Type	DFII LSW Name	DFII Layer Name	DFII Layer Purpose	DFII Layer Number	DFII Purpose Number	Description
Cont	6	0	Cont	Cont	drawing	20	252	Metal Contact to Oxide/Poly
Metal1	7	0	Metal1	Metal1	drawing	30	252	1st Metal for interconnect
Metal2	9	0	Metal2	Metal2	drawing	34	252	2nd Metal for interconnect
Metal3	11	0	Metal3	Metal3	drawing	38	252	3rd Metal for interconnect
Metal4	31	0	Metal4	Metal4	drawing	42	252	4th Metal for interconnect
Metal5	33	0	Metal5	Metal5d	drawing	46	252	5th Metal for interconnect
Metal6	35	0	Metal6	Metal6	drawing	50	252	6th Metal for interconnect
Metal7	38	0	Metal7	Metal7	drawing	54	252	7th Metal for interconnect
Metal8	40	0	Metal8	Metal8d	drawing	58	252	8th Metal for interconnect
Metal9	42	0	Metal9	Metal9	drawing	62	252	9th Metal for interconnect
Metal10	152	0	Metal10	Metal10	drawing	66	252	10th Metal for interconnect
Metal11	162	0	Metal11	Metal11	drawing	70	252	11th metal for interconnect
Via1	8	0	Via1	Via1	drawing	32	252	Via between 1st and 2nd Metal
Via2	10	0	Via2	Via2	drawing	36	252	Via between 2nd and 3rd Metal
Via3	30	0	Via3	Via3	drawing	38	252	Via between 3rd and 4th Metal
Via4	32	0	Via4	Via4	drawing	44	252	Via between 4th and 5th Metal
Via5	34	0	Via5	Via5	drawing	48	252	Via between 5th and 6th Metal
Via6	37	0	Via6	Via6	drawing	52	252	Via between 6th and 7th Metal
Via7	39	0	Via7	Via7	drawing	54	252	Via between 7th and 8th Metal
Via8	41	0	Via8	Via8	drawing	60	252	Via between 8th and 9th Metal
Via9	151	0	Via9	Via9	drawing	64	252	Via between 9th and 10th Metal
Via10	161	0	Via10	Via10	drawing	68	252	Via between 10th and 11th Metal

**Table 2: Interconnect Layers**

This table describes the layers used to mark/label shapes for DRC and/or LVS..  
 Comment Table

Layer Name	GDSII Stream Number	GDSII Data Type	DFII LSW Name	DFII Layer Name	DFII Layer Purpose	DFII Layer Number	DFII Purpose Number	Description
BJTdum	15	0	BJTdum	BJTdum	drawing	92	252	Marks BJT emitters
Capdum	12	0	Capdum	Capdum	drawing	96	252	Marks capacitors
Cap3dum	84	0	Cap3dum	Cap3dum	drawing	93	252	Marks capacitors 3 term
DIOdummy	22	0	DIOdum	DIOdummy	drawing	82	252	Marks diodes
INDdummy	90	0	INDdum	INDdummy	drawing	90	252	Marks inductor terminal
IND2dummy	88	0	IND2dum	IND2dummy	drawing	88	252	Marks inductor terminal
IND3dummy	114	0	IND3dum	IND3dummy	drawing	114	252	Marks inductor terminal
ESDdummy	74	0	ESDdum	ESDdummy	drawing	115	252	Marks ESD and I/O devices
Metal1_text	7	3	Metal1	Metal1	drawing	30	252	Labels Metal1 nodes
Metal2_text	9	3	Metal2	Metal2	drawing	34	252	Labels Metal2 nodes
Metal3_text	11	3	Metal3	Metal3	drawing	38	252	Labels Metal3nodes
Metal4_text	31	3	Metal4	Metal4	drawing	42	252	Labels Metal4 nodes
Metal5_text	33	3	Metal5	Metal5	drawing	46	252	Labels Metal5 nodes
Metal6_text	35	3	Metal6	Metal6	drawing	50	252	Labels Metal6 nodes
Metal7_text	38	3	Metal7	Metal7	drawing	54	252	Labels Metal7 nodes
Metal8_text	40	3	Metal8	Metal8	drawing	58	252	Labels Metal8 nodes
Metal9_text	42	3	Metal9	Metal9	drawing	62	252	Labels Metal9 nodes
Metal10_text	52	3	Metal10	Metal10	drawing	72	252	Labels Metal10 nodes
Metal11_text	62	3	Metal11	Metal11	drawing	82	252	Labels Metal11 nodes
NPNdummy	20	0	NPNdum	NPNdummy	drawing	86	252	Marks NPN devices
PNPdummy	21	0	PNPdum	PNPdummy	drawing	84	252	Marks PNP devices
Psub	25	0	Psub	Psub	drawing	80	252	Marks separate substrate areas
Resdum	13	0	Resdum	Resdum	drawing	94	252	Marks Poly/Oxide resistor area
ResWdum	71	0	ResWdum	ResWdum	drawing	98	252	Marks Nwell resistor area
text	63	0	text	text	drawing	230	252	Text for information
SRAM	64	0	SRAM	SRAM	drawing	71	252	Memory marker layer
PO_text	65	0	PO_text	PO_text	drawing	72	252	Poly text marker layer
SEALRING	66	0	SEALRING	SEALRING	drawing	73	252	Die Sealing marker layer
LOGO	67	0	LOGO	LOGO	drawing	74	252	Chip Logo marker layer
ANALOG	68	0	ANALOG	ANALOG	drawing	75	252	Special Analog marker layer
FUSE	69	0	FUSE	FUSE	drawing	76	252	Fuse marker layer
FILLER	86	0	FILLER	FILLER	drawing	77	252	Fill cell marker layer
VIAEXCL	87	0	VIAEXCL	VIAEXCL	drawing	78	252	Via exclude marker layer

**Table 3: DRC/LVS Marker/Label Layers**



# Device Layer Table

This table describes the layers used in each device.

0: the layer must not touch the device structure

1: the layer must enclose or straddle the device structure

-: the layer may either enclose or avoid the device structure

Comment Table

	NMOS (1.2V)	PMOS (1.2V)	LP NMOS (1.2V)	LP PMOS (1.2V)	NMOS (1.8V)	PMOS (1.8V)	Native NMOS (1.2V)	Native NMOS (1.8V)
Nburied	0	0	0	0	0	0	0	0
Nwell	0	1	0	1	0	1	0	0
Oxide	1	1	1	1	1	1	1	1
Oxide_thk	0	0	0	0	1	1	0	1
Poly	1	1	1	1	1	1	1	1
Nimp	1	0	1	0	1	0	1	1
Pimp	0	1	0	1	0	1	0	0
Nzvt	0	0	0	0	0	0	1	1
Nhvt	0	0	1	0	0	0	0	0
Phvt	0	0	0	1	0	0	0	0
SiProt	0	0	0	0	0	0	0	0

**Table 4: MOS Device Layers**

Comment Table

	N+/PW Diode	P+/NW Diode
Nburied	0	0
Nwell	0	1
Oxide	1	1
Oxide_thk	0	0
Poly	0	0
Nimp	1	0
Pimp	0	1
Nzvt	0	0
Nhvt	0	0
Phvt	0	0
SiProt	0	0

**Table 5: Diode Device Layers**

Comment Table

	Salicided N+ Poly Resistor	Salicided P+ Poly Resistor	Salicided N+ Oxide Resistor	Salicided P+ Oxide Resistor	Non- Salicided N+ Poly Resistor	Non- Salicided P+ Poly Resistor	Non- Salicided N+ Oxide Resistor	Non- Salicided P+ Oxide Resistor
Nburied	0	0	0	0	0	0	0	0
Nwell	-	-	0	1	-	-	0	1
Oxide	0	0	1	1	0	0	1	1
Oxide_thk	0	0	0	0	0	0	0	0
Poly	1	1	0	0	1	1	0	0
Nimp	1	0	1	0	1	0	1	0
Pimp	0	1	0	1	0	1	0	1
Nzvt	0	0	0	0	0	0	0	0
Nhvt	0	0	0	0	0	0	0	0
Phvt	0	0	0	0	0	0	0	0
SiProt	0	0	0	0	1	1	1	1

Comment Table

	Nwell in Oxide Resistor	Nwell in STI Resistor
Nburied	0	0
Nwell	1	1
Oxide	1	1
Oxide_thk	0	0
Poly	0	0
Nimp	1	1
Pimp	0	0
Nzvt	0	0
Nhvt	0	0
Phvt	0	0
SiProt	1	0

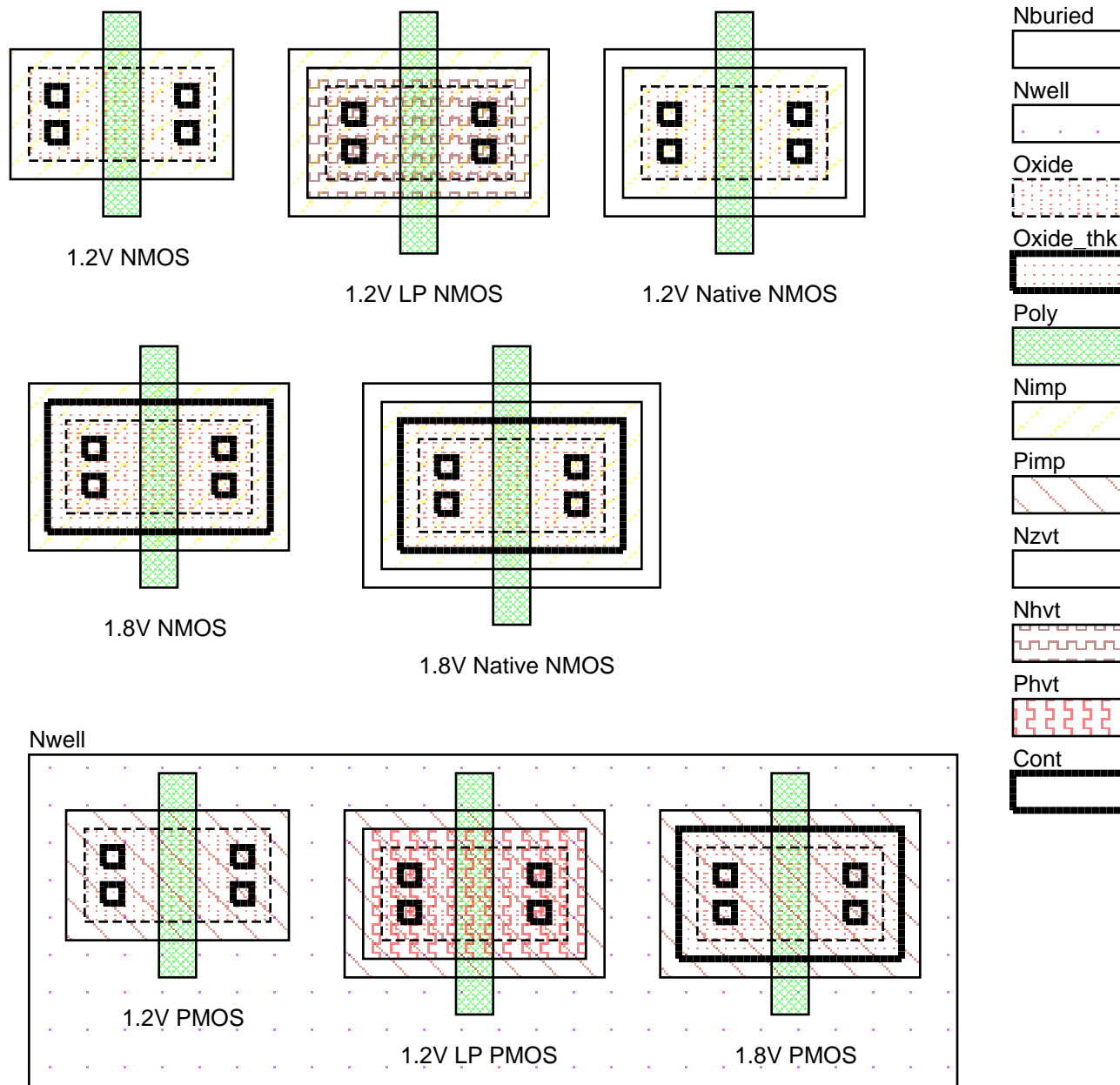
Table 6: Resistor Device Layers

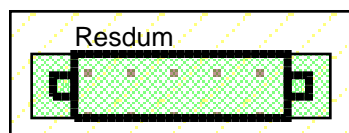
Comment Table

	SPNP	VNPN	Varactor (NMOSCAP)
Nburied	0	1	0
Nwell	1	1	1
Oxide	1	1	1
Oxide_thk	0	0	0
Poly	0	0	1
Nimp	1	1	1
Pimp	1	1	0
Nzvt	0	0	0
Nhvt	0	0	0
Phvt	0	0	0
SiProt	0	0	0

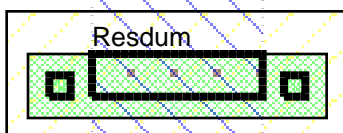
**Table 7: Bipolar and Varactor Device Layers**

# Device Layout Examples

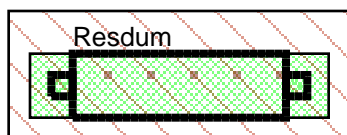




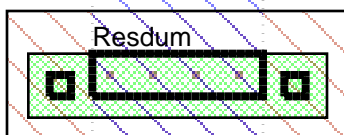
Salicided N+ Poly Resistor



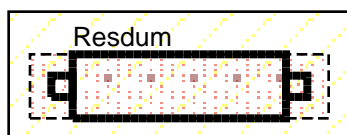
Non-Salicided N+ Poly Resistor



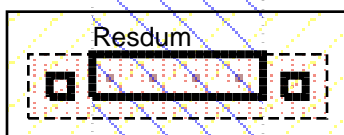
Salicided P+ Poly Resistor



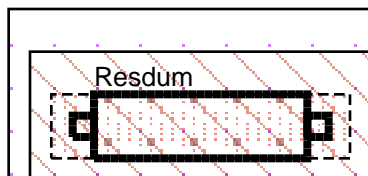
Non-Salicided P+ Poly Resistor



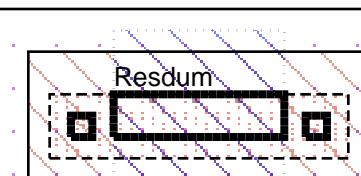
Salicided N+ Oxide Resistor



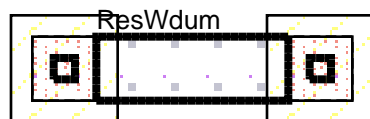
Non-Salicided N+ Oxide Resistor



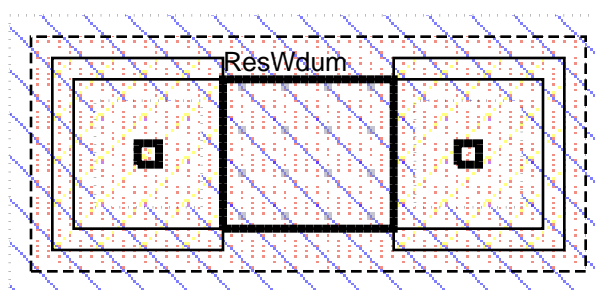
Salicided P+ Oxide Resistor



Non-Salicided P+ Oxide Resistor

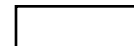


Nwell in STI Resistor



Nwell in OD Resistor

Nburied



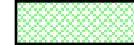
Nwell



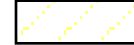
Oxide



Poly



Nimp



Pimp



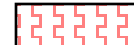
Nzvt



Nhvt



Phvt



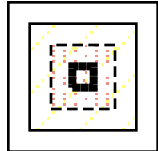
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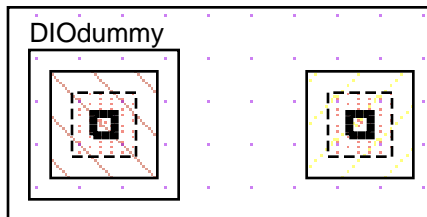
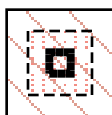
SiProt



DIOdummy

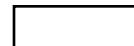


N+/PW Diode



P+/NW Diode

Nburied



Nwell



Oxide



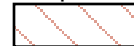
Poly



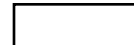
Nimp



Pimp



Nzvt



Nhvt



Phvt



Cont



SiProt

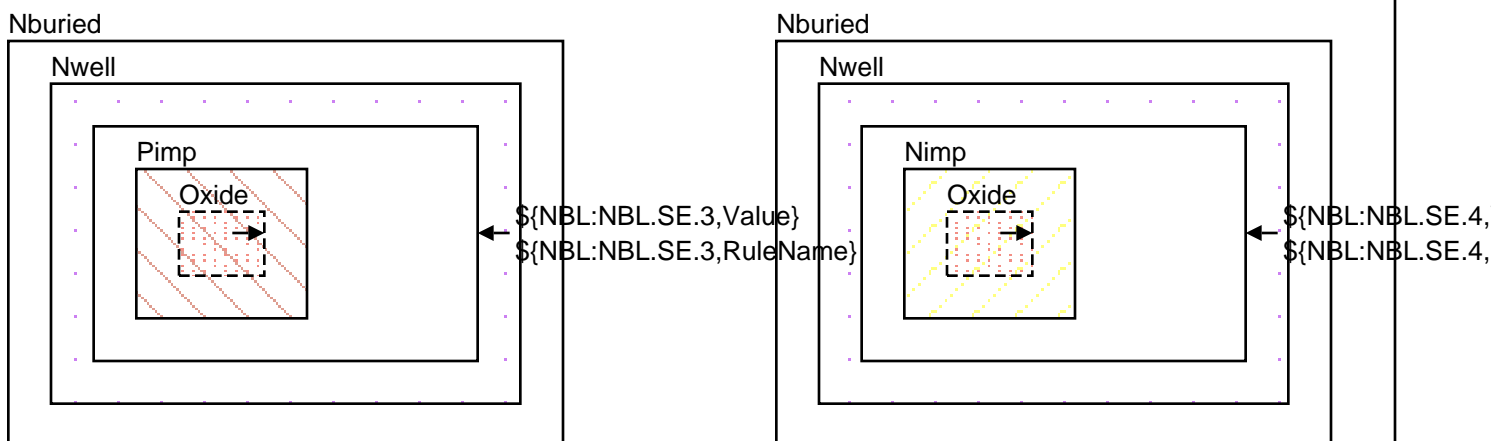
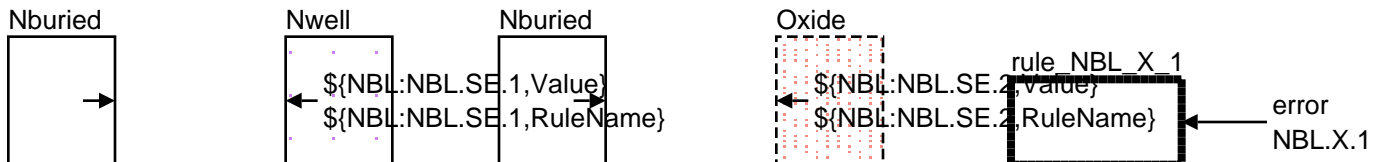
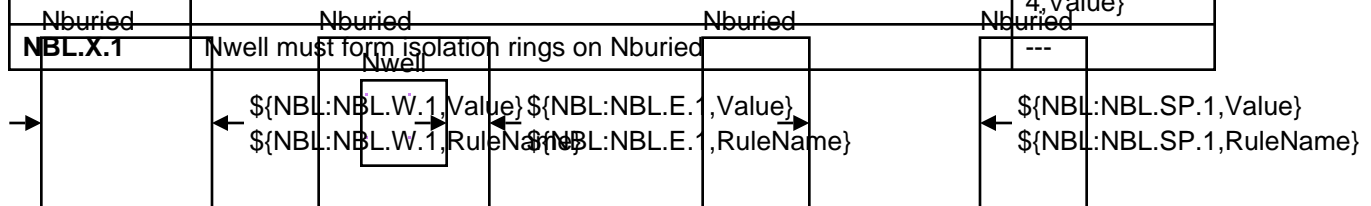


# CMOS Digital Core Design Rules

## N BURIED LAYER RULES

Data Table: NBL\_DRC

RuleName	Description	Value
NBL.W.1	\${NBL:NBL.W.1,Description}	\${NBL:NBL.W.1,Value}
NBL.E.1	\${NBL:NBL.E.1,Description}	\${NBL:NBL.E.1,Value}
NBL.SP.1	\${NBL:NBL.SP.1,Description}	\${NBL:NBL.SP.1,Value}
NBL.SE.1	\${NBL:NBL.SE.1,Description}	\${NBL:NBL.SE.1,Value}
NBL.SE.2	\${NBL:NBL.SE.2,Description}	\${NBL:NBL.SE.2,Value}
NBL.SE.3	\${NBL:NBL.SE.3,Description}	\${NBL:NBL.SE.3,Value}
NBL.SE.4	\${NBL:NBL.SE.4,Description}	\${NBL:NBL.SE.4,Value}
NBL.X.1	Nwell must form isolation rings on Nburied	---



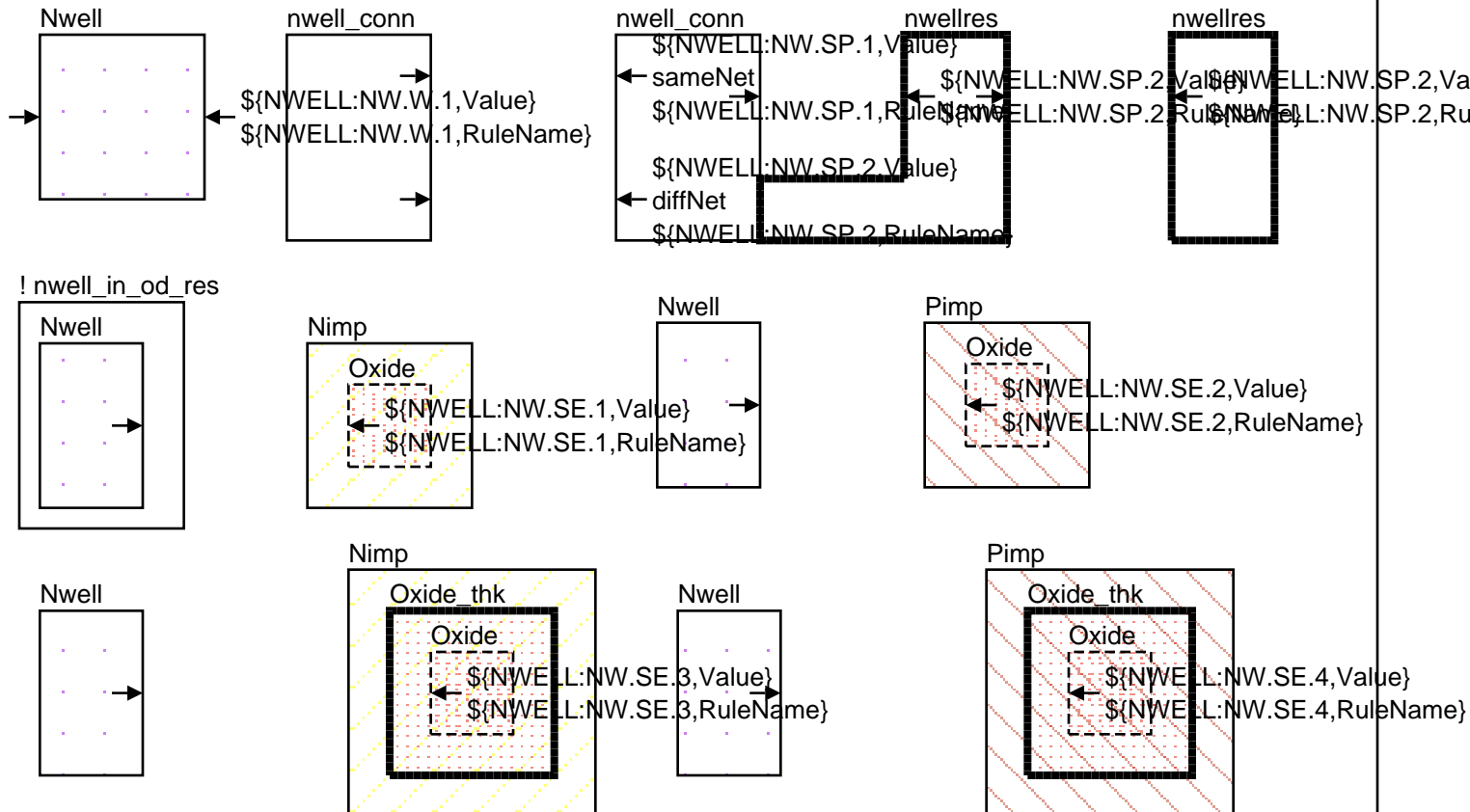
## NWELL AND NWELL RESISTOR (under STI) RULES

Data Table: NWELL\_DRC

RuleName	Description	Value
NW.W.1	\${NWELL:NW.W.1,Description}	\${NWELL:NW.W.1,Value}
NW.SP.1	\${NWELL:NW.SP.1,Description}	\${NWELL:NW.SP.1,Value}
NW.SP.2	\${NWELL:NW.SP.2,Description}	\${NWELL:NW.SP.2,Value}
NW.SE.1	\${NWELL:NW.SE.1,Description}	\${NWELL:NW.SE.1,Value}
NW.SE.2	\${NWELL:NW.SE.2,Description}	\${NWELL:NW.SE.2,Value}
NW.SE.3	\${NWELL:NW.SE.3,Description}	\${NWELL:NW.SE.3,Value}
NW.SE.4	\${NWELL:NW.SE.4,Description}	\${NWELL:NW.SE.4,Value}
NW.E.1	\${NWELL:NW.E.1,Description}	\${NWELL:NW.E.1,Value}
NW.E.2	\${NWELL:NW.E.2,Description}	\${NWELL:NW.E.2,Value}
NW.E.3	\${NWELL:NW.E.3,Description}	\${NWELL:NW.E.3,Value}
NW.E.4	\${NWELL:NW.E.4,Description}	\${NWELL:NW.E.4,Value}
NW.A.1	\${NWELL:NW.A.1,Description}	\${NWELL:NW.A.1,Value}
NW.EA.1	\${NWELL:NW.EA.1,Description}	\${NWELL:NW.EA.1,Value}

Nwell resistor is defined by the intersection of Nwell and ResWdum for DRC and LVS.

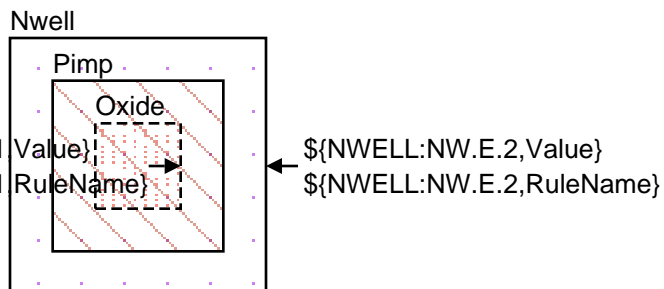
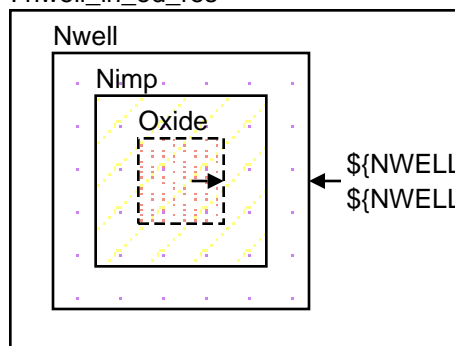
For STI Nwell resistors, the ResWdum shape must butt the N+ Oxide on both ends of Nwell the resistor and the ResWdum shape must be coincident or extend beyond the Nwell edges along the...





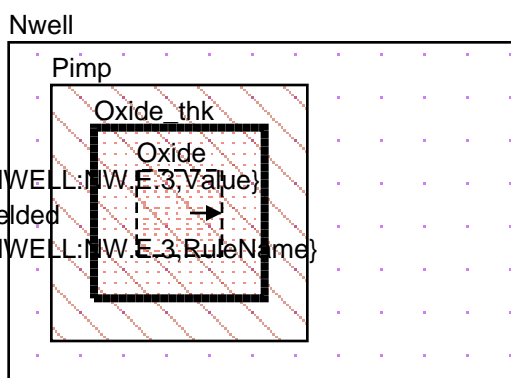
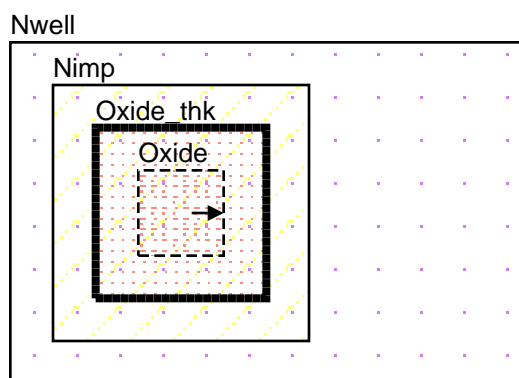
## NWELL AND NWELL RESISTOR (under STI) RULES (continued)

! nwell\_in\_od\_res



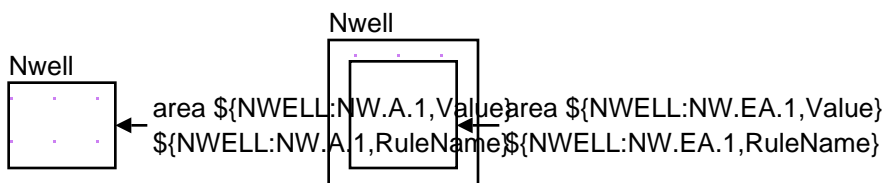
←  $\{\text{NWELL:NW.E.1,Value}\}$   
 $\{\text{NWELL:NW.E.1,RuleName}\}$

←  $\{\text{NWELL:NW.E.2,Value}\}$   
 $\{\text{NWELL:NW.E.2,RuleName}\}$



←  $\{\text{NWELL:NW.E.3,Value}\}$   
 shielded  
 $\{\text{NWELL:NW.E.3,RuleName}\}$

←  $\{\text{NWELL:NW.E.4,Value}\}$   
 shielded  
 $\{\text{NWELL:NW.E.4,RuleName}\}$



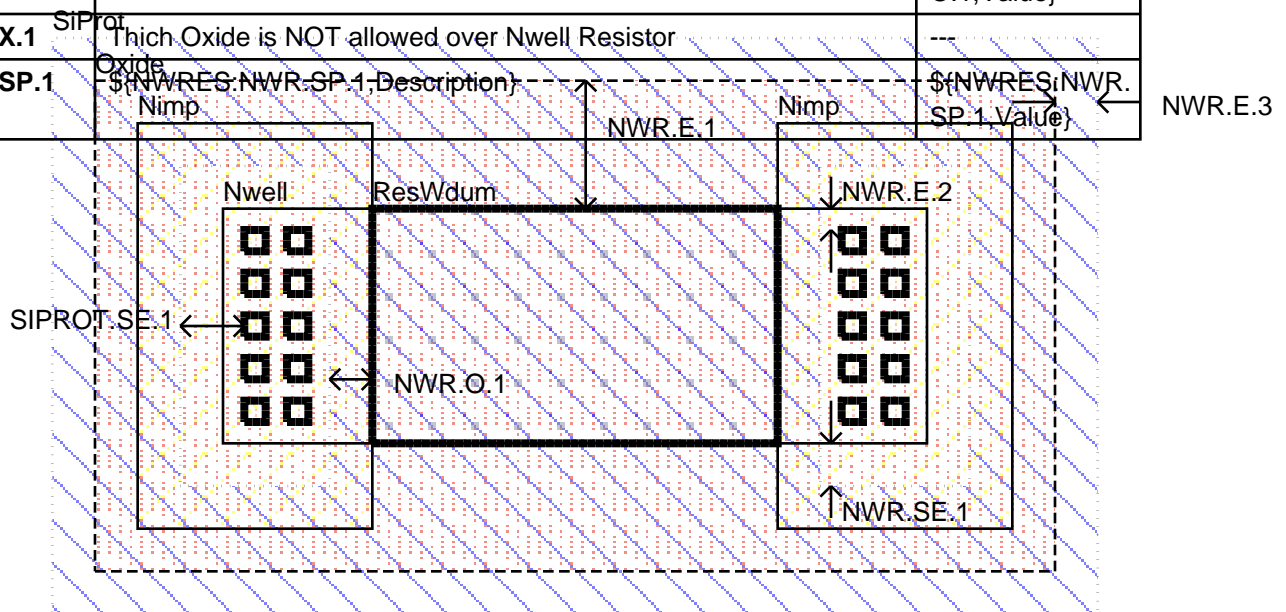
←  $\text{area } \{\text{NWELL:NW.A.1,Value}\}$   
 $\{\text{NWELL:NW.A.1,RuleName}\}$

←  $\text{area } \{\text{NWELL:NW.EA.1,Value}\}$   
 $\{\text{NWELL:NW.EA.1,RuleName}\}$

## NWELL RESISTOR WITHIN OXIDE RULES

Data Table: NWRES\_DRC

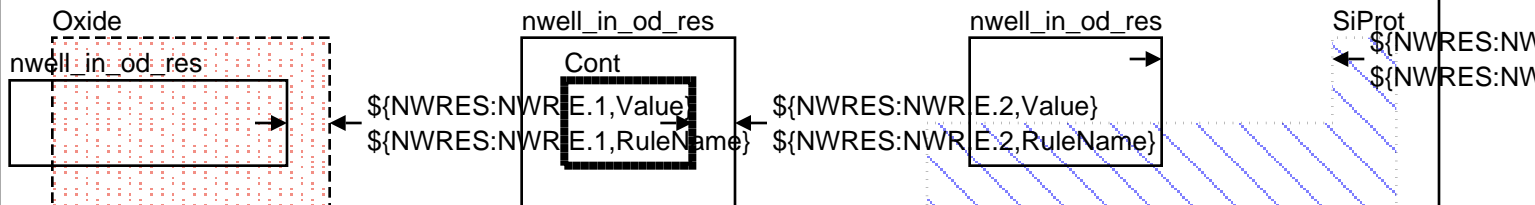
RuleName	Description	Value
NWR.E.1	\${NWRES:NWR.E.1,Description}	\${NWRES:NWR.E.1,Value}
NWR.E.2	\${NWRES:NWR.E.2,Description}	\${NWRES:NWR.E.2,Value}
NWR.SE.1	\${NWRES:NWR.SE.1,Description}	\${NWRES:NWR.SE.1,Value}
NWR.E.3	\${NWRES:NWR.E.3,Description}	\${NWRES:NWR.E.3,Value}
NWR.O.1	\${NWRES:NWR.O.1,Description}	\${NWRES:NWR.O.1,Value}
NWR.X.1	Thick Oxide is NOT allowed over Nwell Resistor	---
NWR.SP.1	\${NWRES:NWR.SP.1,Description}	\${NWRES:NWR.SP.1,Value}



**Figure 1: NWELL RESISTOR WITHIN OXIDE RULES**

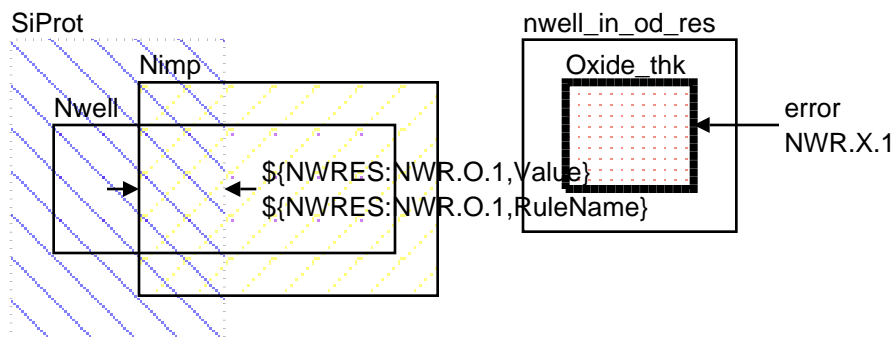
Nwell resistor in Oxide is defined by the intersection of Nwell and Resdum for DRC and LVS.

For Nwell resistor within Oxide, the ResWdum shape must butt the Nimp on both ends of the Nwell resistor and the ResWdum shape must be coincident or extend beyond the Nwell edges along the length of the Nwell resistor.



**NWELL RESISTOR WITHIN OXIDE RULES (continued)**

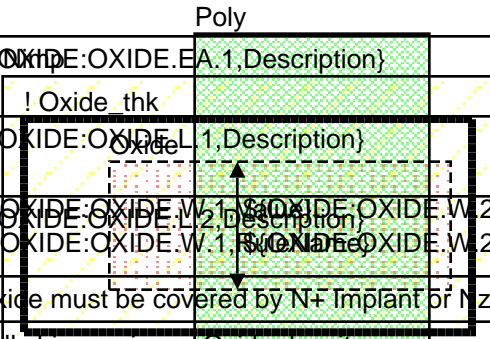
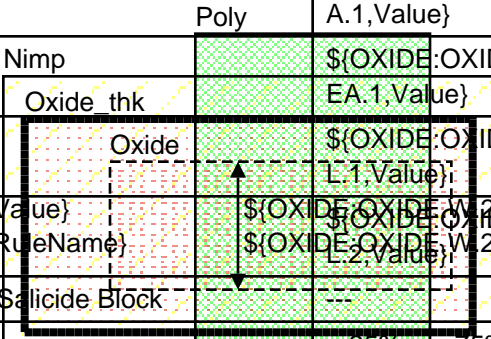
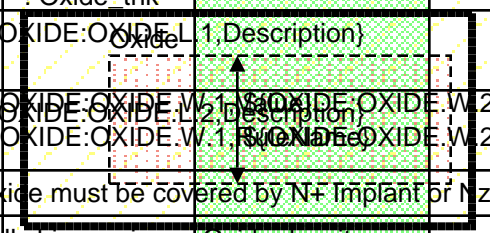
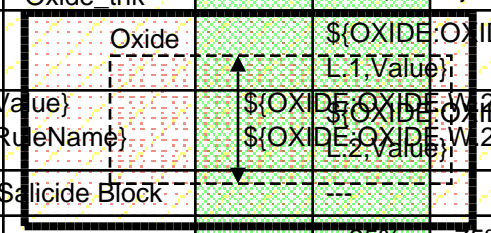
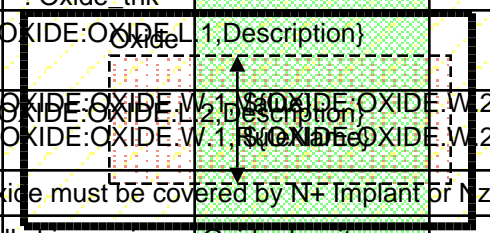
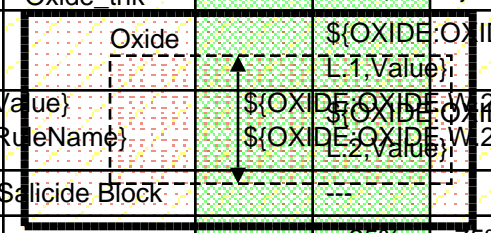
NWR.E.3 - Covered by  
SIPROT.E.1.

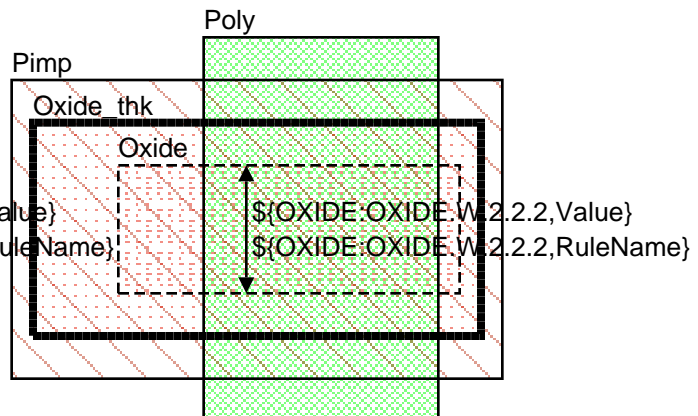
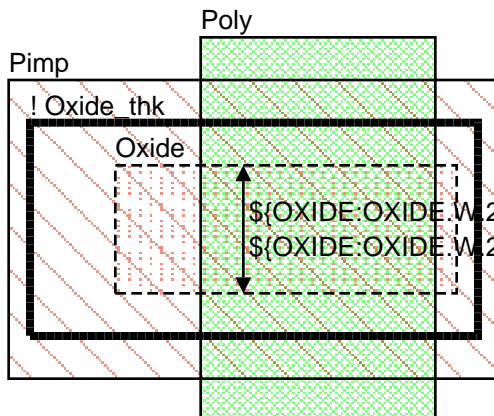


NWR.SP.1 - Covered by NW.SP.2.

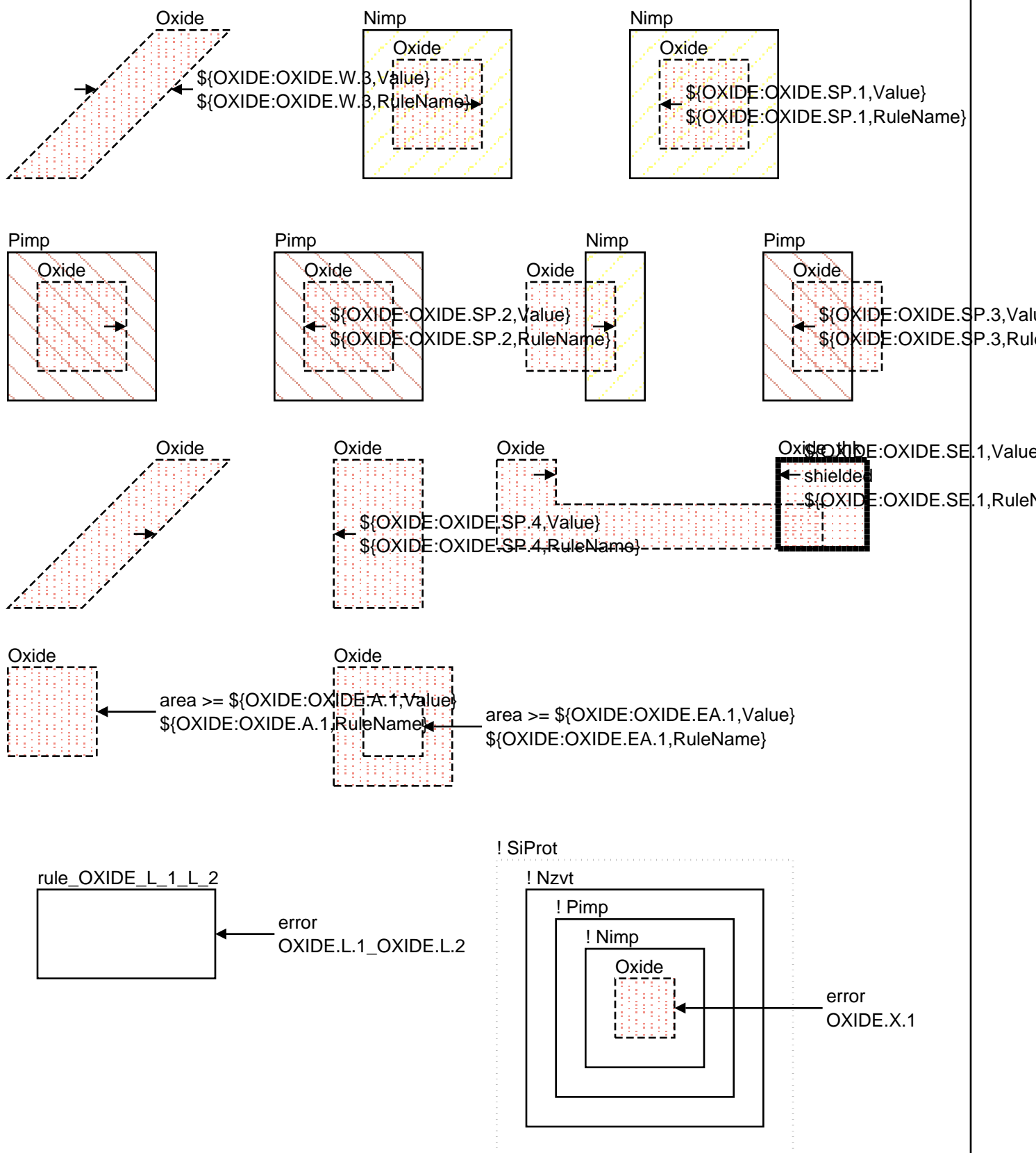
## ACTIVE RULES

Data Table: OXIDE\_DRC

RuleName	Description	Value
OXIDE.W.1	\${OXIDE:OXIDE.W.1,Description}	\${OXIDE:OXIDE.W.1,Value}
OXIDE.W.2.1.1	\${OXIDE:OXIDE.W.2.1.1,Description}	\${OXIDE:OXIDE.W.2.1.1,Value}
OXIDE.W.2.1.2	\${OXIDE:OXIDE.W.2.1.2,Description}	\${OXIDE:OXIDE.W.2.1.2,Value}
OXIDE.W.2.2.1	\${OXIDE:OXIDE.W.2.2.1,Description}	\${OXIDE:OXIDE.W.2.2.1,Value}
OXIDE.W.2.2.2	\${OXIDE:OXIDE.W.2.2.2,Description}	\${OXIDE:OXIDE.W.2.2.2,Value}
OXIDE.W.3	\${OXIDE:OXIDE.W.3,Description}	\${OXIDE:OXIDE.W.3,Value}
OXIDE.SP.1	\${OXIDE:OXIDE.SP.1,Description}	\${OXIDE:OXIDE.SP.1,Value}
OXIDE.SP.2	\${OXIDE:OXIDE.SP.2,Description}	\${OXIDE:OXIDE.SP.2,Value}
OXIDE.SP.3	\${OXIDE:OXIDE.SP.3,Description}	\${OXIDE:OXIDE.SP.3,Value}
OXIDE.SP.4	\${OXIDE:OXIDE.SP.4,Description}	\${OXIDE:OXIDE.SP.4,Value}
OXIDE.SE.1	\${OXIDE:OXIDE.SE.1,Description}	\${OXIDE:OXIDE.SE.1,Value}
OXIDE.A.1	\${OXIDE:OXIDE.A.1,Description}	\${OXIDE:OXIDE.A.1,Value}
OXIDE.EA.1	 \${OXIDE:OXIDE.EA.1,Description}	 \${OXIDE:OXIDE.EA.1,Value}
OXIDE.L.1	 \${OXIDE:OXIDE.L.1,Description}	 \${OXIDE:OXIDE.L.1,Value}
OXIDE.L.2	 \${OXIDE:OXIDE.W.1,Value} \${OXIDE:OXIDE.L.2,Description} \${OXIDE:OXIDE.W.1,RuleName} \${OXIDE:OXIDE.W.2.1.1,Value} \${OXIDE:OXIDE.W.2.1.1,RuleName} \${OXIDE:OXIDE.W.2.1.2,Value} \${OXIDE:OXIDE.W.2.1.2,RuleName}	 \${OXIDE:OXIDE.W.1,Value} \${OXIDE:OXIDE.L.2,Value} \${OXIDE:OXIDE.W.2.1.1,Value} \${OXIDE:OXIDE.W.2.1.1,RuleName} \${OXIDE:OXIDE.W.2.1.2,Value} \${OXIDE:OXIDE.W.2.1.2,RuleName}
OXIDE.X.1	Oxide must be covered by N+ Implant or Nzvt or Salicide Block	---
OXIDE.D.1	Full chip maximum Oxide density	> 25% <75%
OXIDE.D.2	Local Oxide density 300x300 window stepped at 150	> 25% <75%



## ACTIVE RULES (continued)



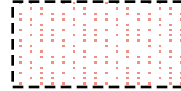
switch CHECK\_DENSITY

Density

ratio > 0.30 < 0.80

id: OXIDE.D.1

Oxide



message: Oxide full chip density must be > 30% < 80%

Density

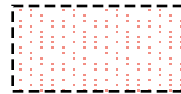
ratio > 0.25 < .75

windowSize: 300.0

stepSize: 150.0

id: OXIDE.D.2

Oxide



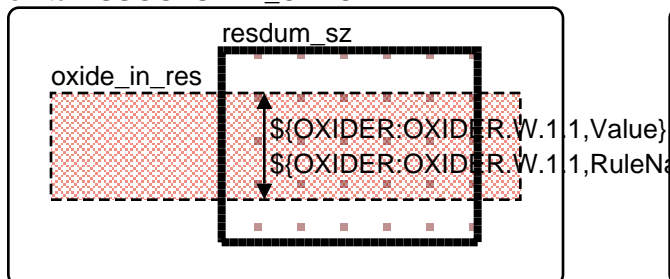
message: Oxide local (300x300) density must be > 25% < 75%

## ACTIVE RESISTOR RULES (salicided/non-salicided)

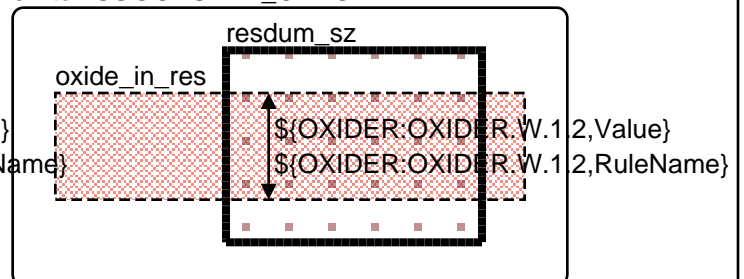
Data Table: OXIDER\_DRC

RuleName	Description	Value
<b>OXIDER.W.1.1</b>	\${OXIDER:OXIDER.W.1.1,Description}	\${OXIDER:OXIDER.W.1.1,Value}
<b>OXIDER.W.1.2</b>	\${OXIDER:OXIDER.W.1.2,Description}	\${OXIDER:OXIDER.W.1.2,Value}
<b>OXIDER.L.1</b>	\${OXIDER:OXIDER.L.1,Description}	\${OXIDER:OXIDER.L.1,Value}
<b>OXIDER.SE.1</b>	\${OXIDER:OXIDER.SE.1,Description} Active resistor is defined by the intersection of Oxide and Resdum for DRC and LVS.	\${OXIDER:OXIDER.SE.1,Value}
<b>OXIDER.E.1</b>	For salicided Oxide resistors, the Resdum shape must butt the contacts on both ends of Oxide the resistor and the Resdum shape must be coincident or extend beyond the Oxide edges along the length of the Oxide resistor.	\${OXIDER:OXIDER.E.1,Value}
<b>OXIDER.SE.2</b>	For non-salicided Oxide resistors, the Resdum shape must be coincident with the edges of the Signal that crosses the width of the Oxide resistor and the Resdum shape must be coincident or extend beyond the Oxide edges along the length of the Oxide resistor.	\${OXIDER:OXIDER.SE.2,Value}
<b>OXIDER.X.1</b>	Active resistors must have N+ or P+ Implant	---

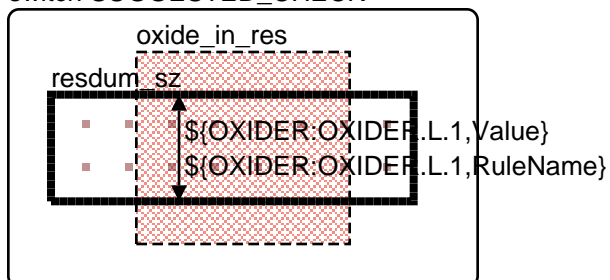
switch !SUGGESTED\_CHECK



switch SUGGESTED\_CHECK



switch SUGGESTED\_CHECK



**OXIDER.SE.1 is checked by  
SIPROT.SE.1**

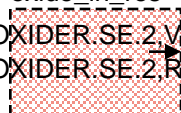
oxide\_in\_res



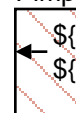
Nimp



oxide\_in\_res

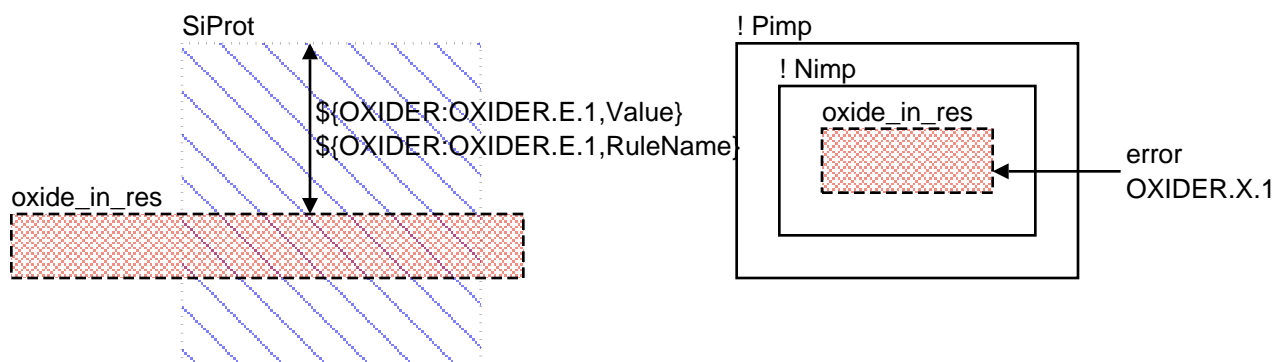


Pimp



\${OXIDER:OXIDER.SE.2,Value}  
 \${OXIDER:OXIDER.SE.2,RuleName}

\${OXIDER:OXIDER.SE.2,Value}  
 \${OXIDER:OXIDER.SE.2,RuleName}

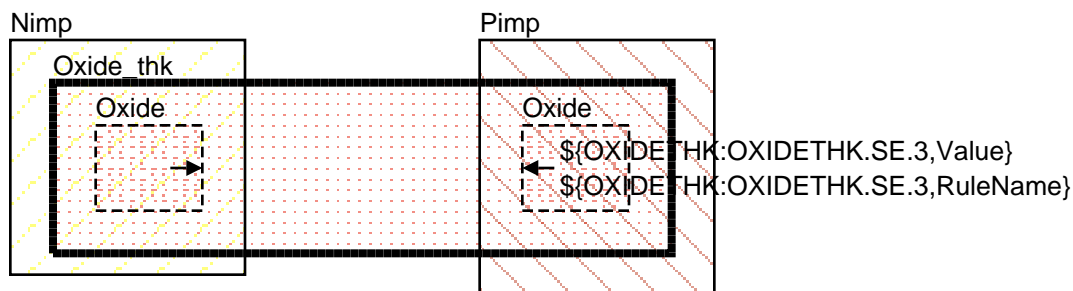
**ACTIVE RESISTOR RULES (continued)**



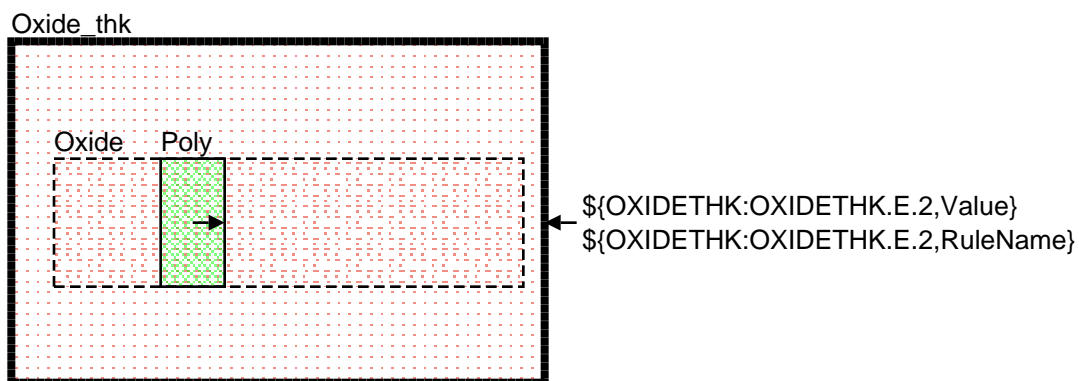
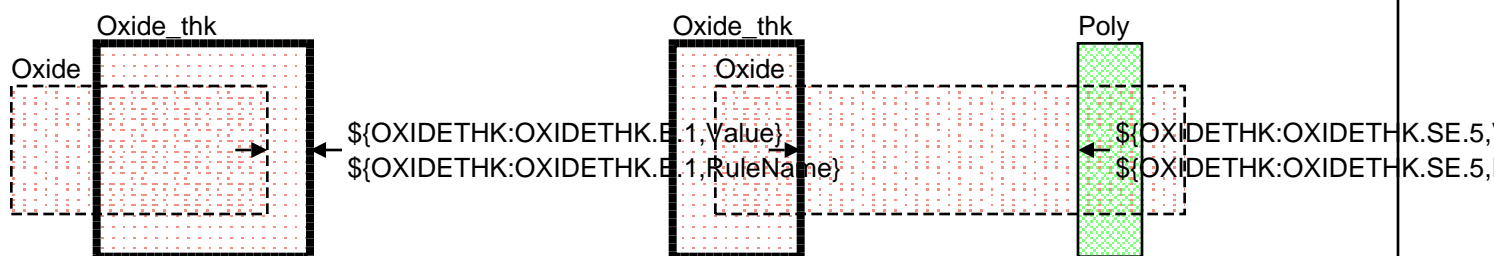
## THICK ACTIVE (1.8V) RULES

Data Table: OXIDETHK\_DRC

RuleName	Description	Value
<b>OXIDETHK.W.1</b>	\${OXIDETHK:OXIDETHK.W.1,Description}	\${OXIDETHK:OXIDETHK.W.1,Value}
<b>OXIDETHK.SP.1</b>	\${OXIDETHK:OXIDETHK.SP.1,Description}	\${OXIDETHK:OXIDETHK.SP.1,Value}
<b>OXIDETHK.SP.2</b>	\${OXIDETHK:OXIDETHK.SP.2,Description}	\${OXIDETHK:OXIDETHK.SP.2,Value}
<b>OXIDETHK.SE.1</b>	\${OXIDETHK:OXIDETHK.SE.1,Description}	\${OXIDETHK:OXIDETHK.SE.1,Value}
<b>OXIDETHK.SE.2</b>	\${OXIDETHK:OXIDETHK.SE.2,Description} Note 1: 1.8V MOS must be defined by Active which is fully enclosed by Thick Active (with 0.0 overlap). Note 2: 1.2V MOS is only defined by Active without any Thick Active.	\${OXIDETHK:OXIDETHK.SE.2,Value}
<b>OXIDETHK.SE.3</b>	\${OXIDETHK:OXIDETHK.SE.3,Description}	\${OXIDETHK:OXIDETHK.SE.3,Value}
<b>OXIDETHK.SE.4</b>	\${OXIDETHK:OXIDETHK.SE.4,Description} \${OXIDETHK:OXIDETHK.W.1,Value} \${OXIDETHK:OXIDETHK.W.1,RuleName} \${OXIDETHK:OXIDETHK.SP.1,Value} \${OXIDETHK:OXIDETHK.SP.1,RuleName}	\${OXIDETHK:OXIDETHK.SE.4,Value} \${OXIDETHK:OXIDETHK.W.1,Value} \${OXIDETHK:OXIDETHK.W.1,RuleName} \${OXIDETHK:OXIDETHK.SP.1,Value} \${OXIDETHK:OXIDETHK.SP.1,RuleName}
<b>OXIDETHK.E.1</b>	\${OXIDETHK:OXIDETHK.E.1,Description}	\${OXIDETHK:OXIDETHK.E.1,Value} Nimp Pimp
<b>OXIDETHK.SE.5</b>	\${OXIDETHK:OXIDETHK.SE.5,Description} \${OXIDETHK:OXIDETHK.SE.1,Value} \${OXIDETHK:OXIDETHK.SE.1,RuleName}	\${OXIDETHK:OXIDETHK.SE.5,Value} \${OXIDETHK:OXIDETHK.SE.1,Value} \${OXIDETHK:OXIDETHK.SE.1,RuleName}
<b>OXIDETHK.E.2</b>	\${OXIDETHK:OXIDETHK.E.2,Description} \${OXIDETHK:OXIDETHK.SE.1,Value} \${OXIDETHK:OXIDETHK.SE.1,RuleName}	\${OXIDETHK:OXIDETHK.E.2,Value} \${OXIDETHK:OXIDETHK.SE.1,Value} \${OXIDETHK:OXIDETHK.SE.1,RuleName}



OXIDETHK.SE.4 - Covered by OXIDE.SE.1.

**Thick ACTIVE RULES (continued)**

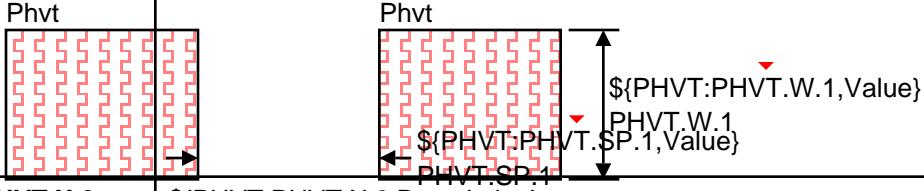
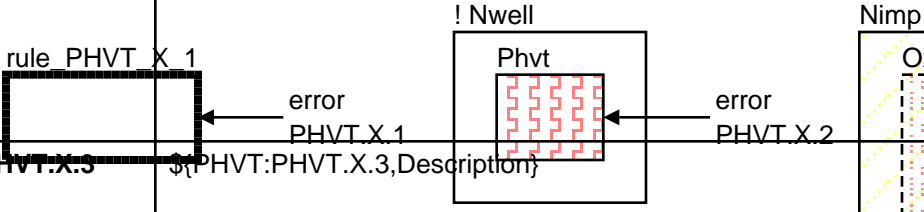
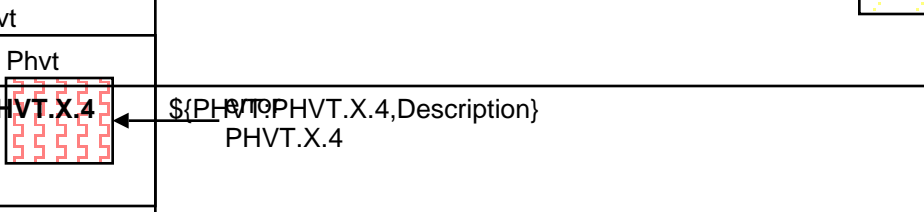
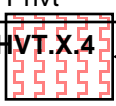
## N+ HIGH VT RULES

Data Table: NHVT

RuleName	Description	Value
<b>NHVT.W.1</b>	\${NHVT:NHVT.W.1,Description}	\${NHVT:NHVT.W.1,Value}
<b>NHVT.SP.1</b>	\${NHVT:NHVT.SP.1,Description}	\${NHVT:NHVT.SP.1,Value}
Note 1: Nhvt defines the 1.2V LP NMOS device.		
<b>NHVT.X.1</b> Nhvt	<div> <div> </div> </div>	\${NHVT:NHVT.X.1,Value}
<b>NHVT.X.2</b>	\${NHVT:NHVT.X.2,Description}	\${NHVT:NHVT.X.2,Value}
<b>NHVT.X.3</b>	<div> <div>rule_NHVT_X_1</div> <div> </div> </div>	<div> <div>error NHVT.X.1</div> <div>error NHVT.X.2</div> <div>error NHVT.X.3</div> </div>
<b>NHVT.X.4</b> Nhvt	<div> <div> </div> </div>	<div> <div>error NHVT.X.4</div> </div>

## P+ HIGH VT RULES

Data Table: PHVT

RuleName	Description	Value
PHVT.W.1	\${PHVT:PHVT.W.1,Description}	\$(PHVT:PHVT.W.1,Value)
PHVT.SP.1	\${PHVT:PHVT.SP.1,Description}  Note 1: Phvt defines the 1.2V LP PMOS device.	\$(PHVT:PHVT.SP.1,Value)
PHVT.X.1	\${PHVT:PHVT.X.1,Description} 	\$(PHVT:PHVT.X.1,Value)
PHVT.X.2	\${PHVT:PHVT.X.2,Description} 	\$(PHVT:PHVT.X.2,Value)
PHVT.X.3	\${PHVT:PHVT.X.3,Description} 	\$(PHVT:PHVT.X.3,Value)
PHVT.X.4	\${PHVT:PHVT.X.4,Description} 	\$(PHVT:PHVT.X.4,Value)

## N+ LOW VT RULES

Data Table: NLVT

RuleName	Description	Value
NLVT.W.1	\${NLVT:NLVT.W.1,Description}	\${NLVT:NLVT.W.1,Value}
NLVT.SP.1	\${NLVT:NLVT.SP.1,Description}	\${NLVT:NLVT.SP.1,Value}
Note 1: Nlvt defines the 1.2V LP NMOS device.		
NLVT.X.1	<div> </div>	\${NLVT:NLVT.X.1,Value}
NLVT.X.2	<div> </div>	\${NLVT:NLVT.X.2,Value}
NLVT.X.3	<div> </div>	\${NLVT:NLVT.X.3,Value}
NLVT.X.4	<div> </div>	\${NLVT:NLVT.X.4,Value}

## P+ LOW VT RULES

Data Table: PLVT

RuleName	Description	Value
PLVT.W.1	\$(PLVT:PLVT.W.1,Description)	\$(PLVT:PLVT.W.1,Value)
PLVT.SP.1	\$(PLVT:PLVT.SP.1,Description)	\$(PLVT:PLVT.SP.1,Value)
Note 1: Plvt defines the 1.2V LP PMOS device.		
PLVT.X.1	\$(PLVT:PLVT.X.1,Description)	\$(PLVT:PLVT.X.1,Value)
PLVT.X.2	\$(PLVT:PLVT.X.2,Description)	\$(PLVT:PLVT.X.2,Value)
PLVT.X.3	\$(PLVT:PLVT.X.3,Description)	\$(PLVT:PLVT.X.3,Value)
PLVT.X.4	\$(PLVT:PLVT.X.4,Description)	\$(PLVT:PLVT.X.4,Value)

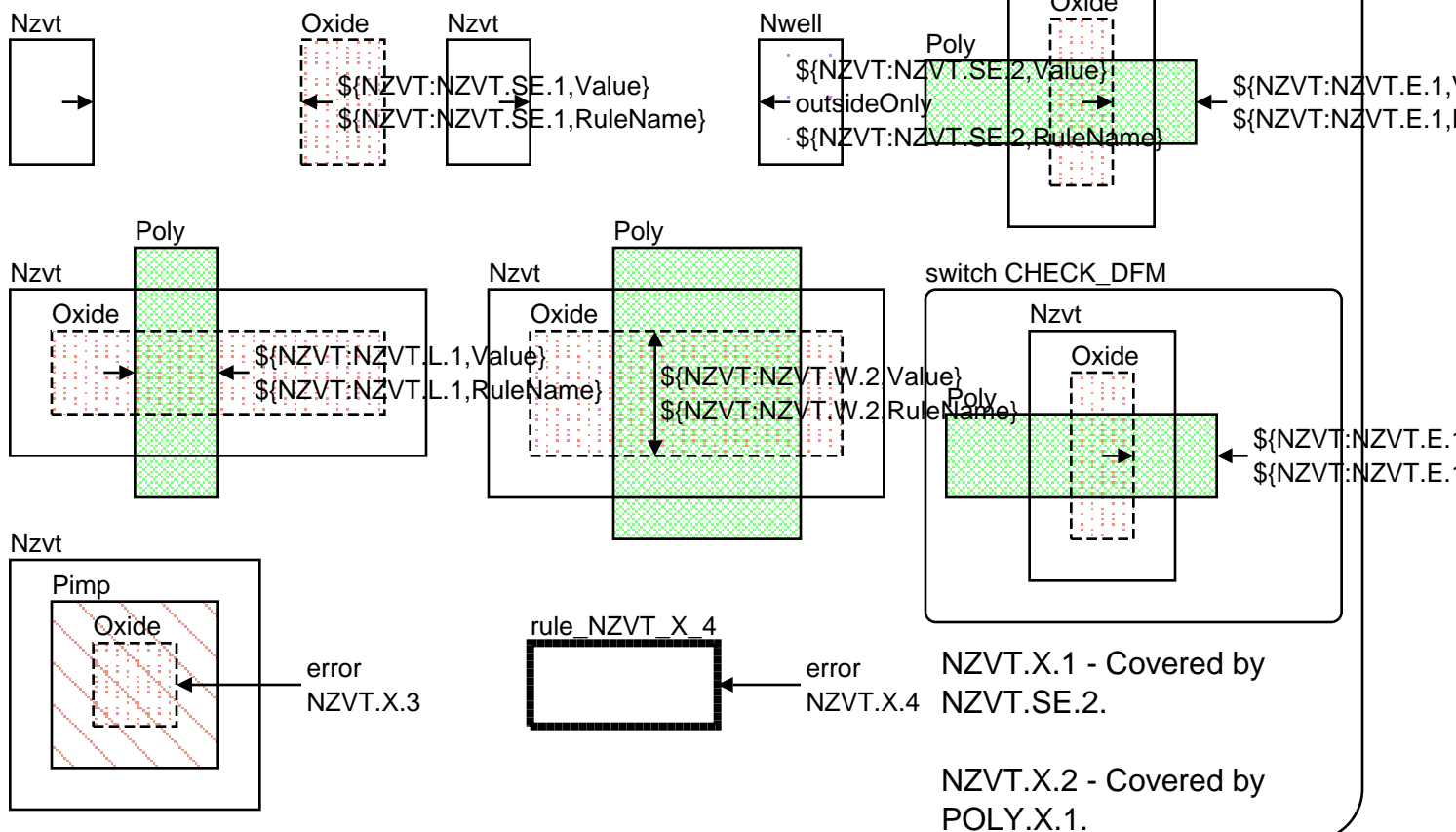
Diagram illustrating the layout rules for PLVT (P+ LOW VT) rules:

- PLVT.W.1**: Width rule. Diagram shows a rectangle with width dimensioned as  $\$(PLVT:PLVT.W.1,Value)$ .
- PLVT.SP.1**: Spacing rule. Diagram shows two rectangles with spacing dimensioned as  $\$(PLVT:PLVT.SP.1,Value)$ .
- PLVT.X.1**: Layout rule. Diagram shows a rectangle labeled "Plvt" with dimensions  $\$(PLVT:PLVT.W.1,Value)$  and  $\$(PLVT:PLVT.SP.1,Value)$ .
- PLVT.X.2**: Layout rule. Diagram shows a rectangle labeled "Plvt" with dimensions  $\$(PLVT:PLVT.W.1,Value)$  and  $\$(PLVT:PLVT.SP.1,Value)$ .
- PLVT.X.3**: Layout rule. Diagram shows a rectangle labeled "Plvt" with dimensions  $\$(PLVT:PLVT.W.1,Value)$  and  $\$(PLVT:PLVT.SP.1,Value)$ . It includes labels for "rule PLVT.X.1", "Nwell", "Nimp", and "Oxide".
- PLVT.X.4**: Layout rule. Diagram shows a rectangle labeled "Plvt" with dimensions  $\$(PLVT:PLVT.W.1,Value)$  and  $\$(PLVT:PLVT.SP.1,Value)$ . It includes labels for "Nzvt" and "error PLVT.X.4".

# NATIVE NMOS ACTIVE RULES

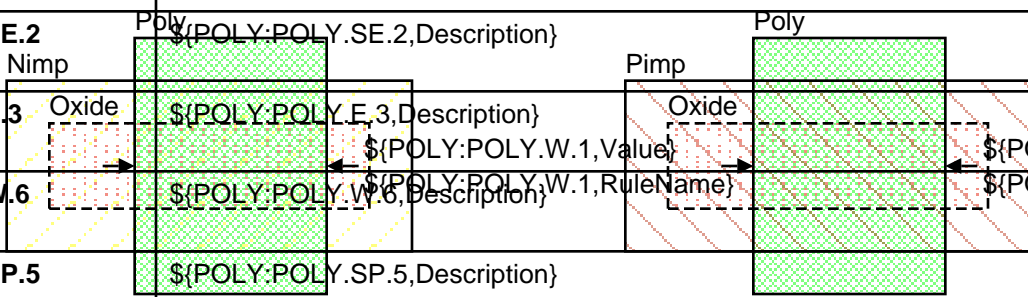
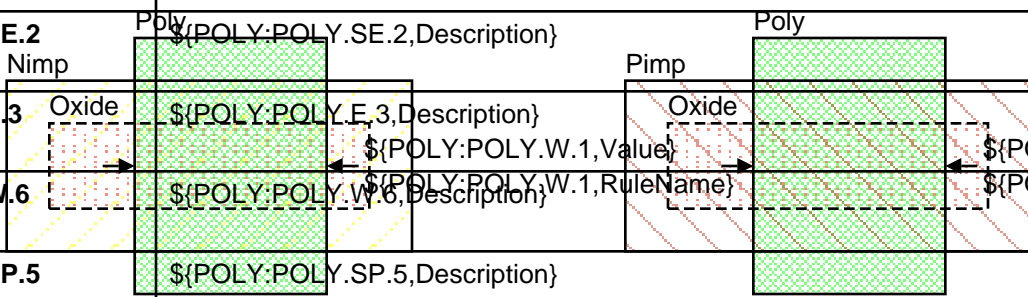
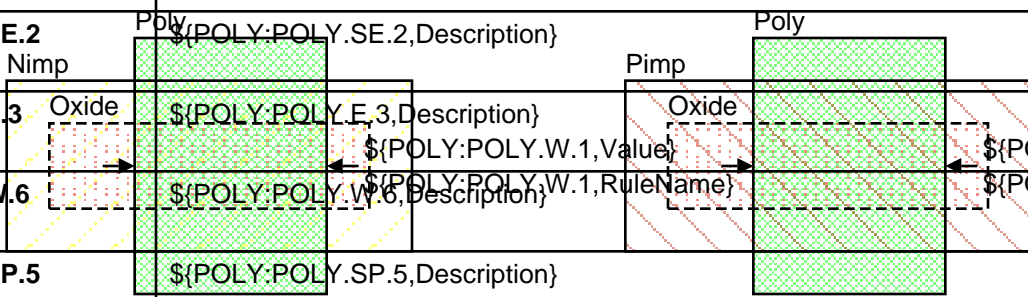
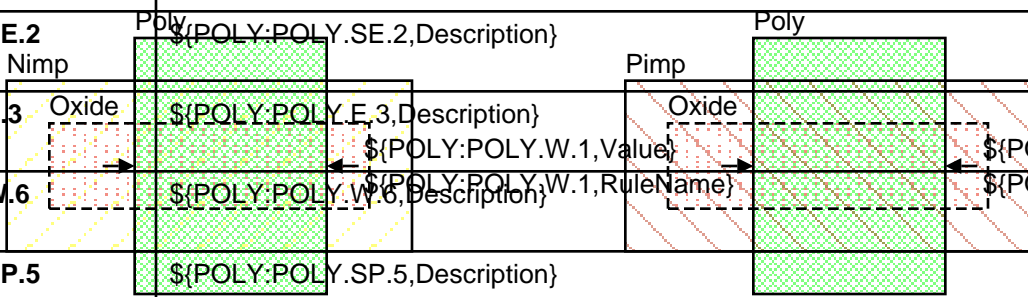
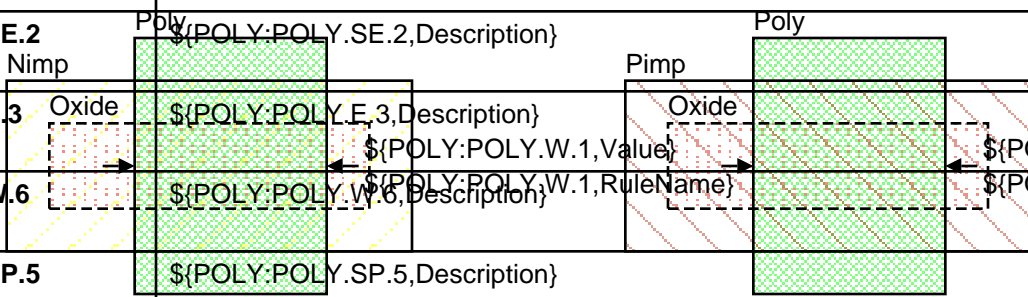
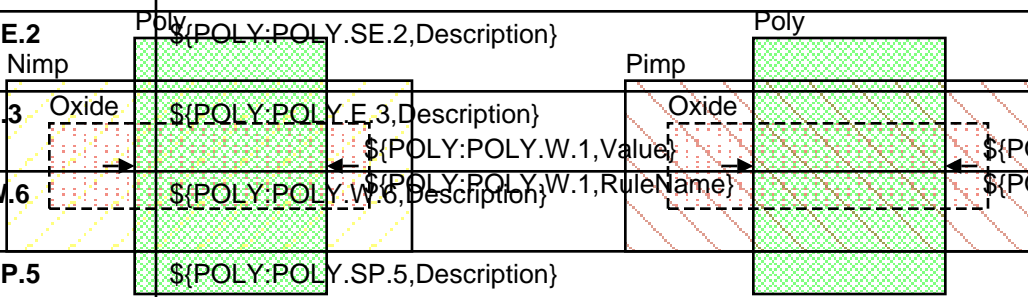
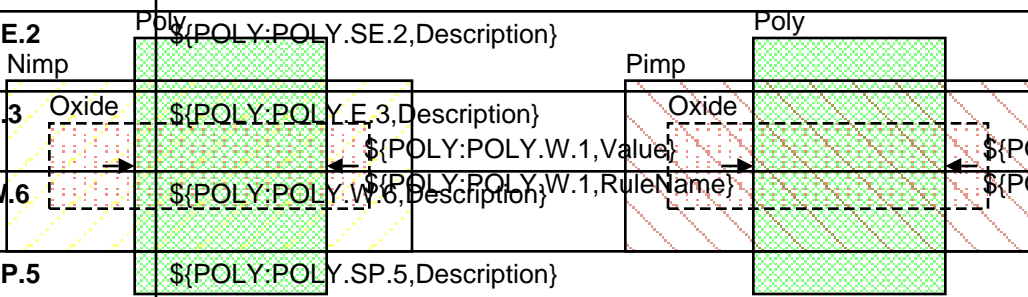
Data Table: NZVT\_DRC

RuleName	Description	Value
NZVT.W.1	\${NZVT:NZVT.W.1,Description}	\${NZVT:NZVT.W.1,Value}
NZVT.SP.1	\${NZVT:NZVT.SP.1,Description}	\${NZVT:NZVT.SP.1,Value}
NZVT.O.1	\${NZVT:NZVT.O.1,Description}	\${NZVT:NZVT.O.1,Value}
NZVT.SE.1	\${NZVT:NZVT.SE.1,Description}	\${NZVT:NZVT.SE.1,Value}
NZVT.SE.2	\${NZVT:NZVT.SE.2,Description}	\${NZVT:NZVT.SE.2,Value}
NZVT.E.1	\${NZVT:NZVT.E.1,Description}	\${NZVT:NZVT.E.1,Value}
NZVT.E.1.DFM	\${NZVT:NZVT.E.1.DFM,Description}	\${NZVT:NZVT.E.1.DFM,Value}
NZVT.L.1	\${NZVT:NZVT.L.1,Description}	\${NZVT:NZVT.L.1,Value}
NZVT.W.2	Note 1: Native NMOS is defined by Active which is full enclosed by Nzvt with 0.3um enclosure. \${NZVT:NZVT.W.2,Description}	\${NZVT:NZVT.W.2,Value}
NZVT.X.1	Nzvt is NOT allowed on Nwell	---
NZVT.X.2	Benf Poly Gates are NOT allowed on Nzvt	---
NZVT.X.3	P+ Active Area is NOT allowed on Nzvt	---
NZVT.X.4	Only one Active Area is allowed in an Nzvt region	---

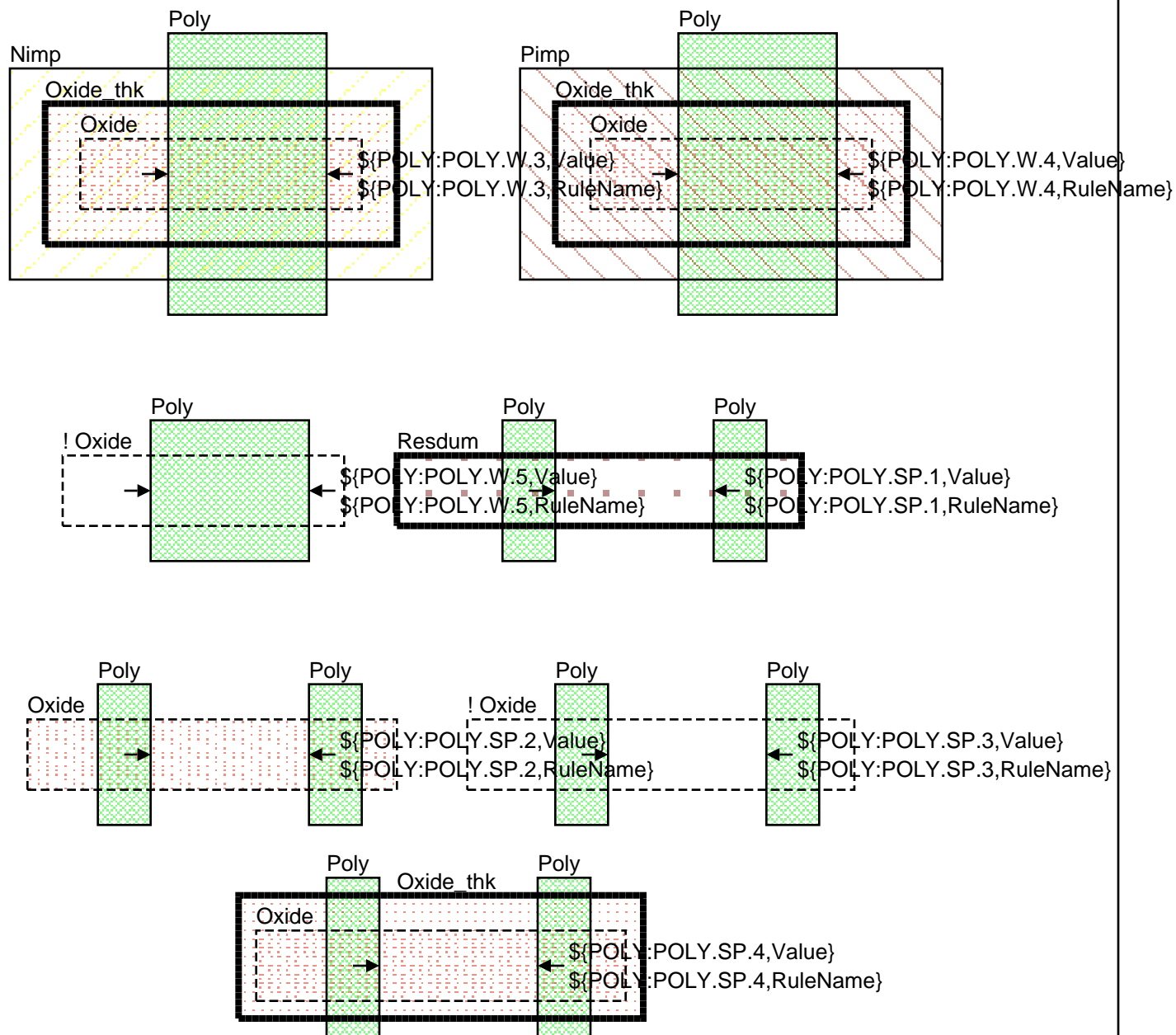


## POLY RULES

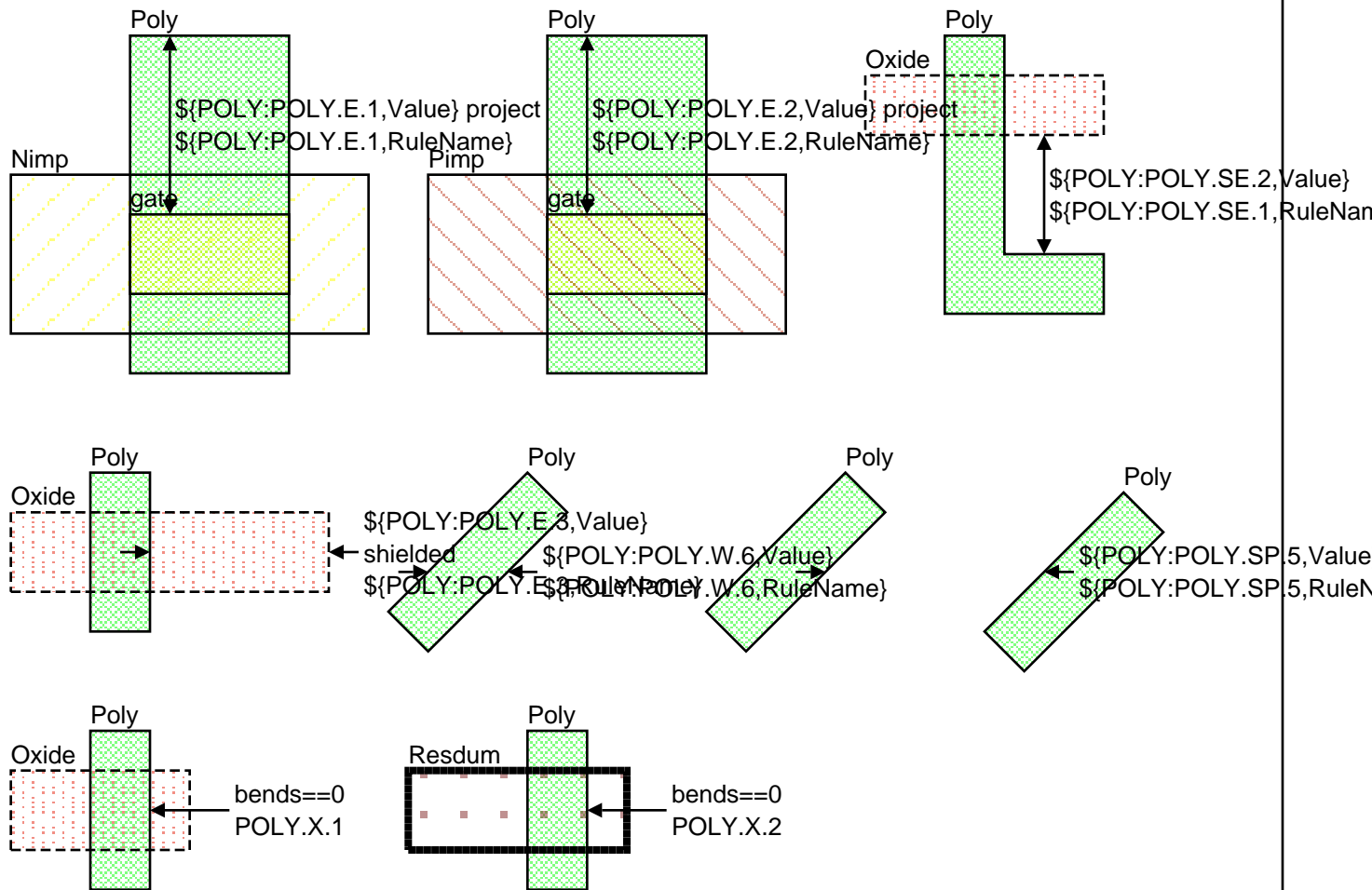
Data Table: POLY\_DRC

RuleName	Description	Value
POLY.W.1	\${POLY:POLY.W.1,Description}	\${POLY:POLY.W.1,Value}
POLY.W.2	\${POLY:POLY.W.2,Description}	\${POLY:POLY.W.2,Value}
POLY.W.3	\${POLY:POLY.W.3,Description}	\${POLY:POLY.W.3,Value}
POLY.W.4	\${POLY:POLY.W.4,Description}	\${POLY:POLY.W.4,Value}
POLY.W.5	\${POLY:POLY.W.5,Description}	\${POLY:POLY.W.5,Value}
POLY.SP.1	\${POLY:POLY.SP.1,Description}	\${POLY:POLY.SP.1,Value}
POLY.SP.2	\${POLY:POLY.SP.2,Description}	\${POLY:POLY.SP.2,Value}
POLY.SP.2.DFM	\${POLY:POLY.SP.2.DFM,Description}	\${POLY:POLY.SP.2.DFM,Value}
POLY.SP.3	\${POLY:POLY.SP.3,Description}	\${POLY:POLY.SP.3,Value}
POLY.SP.4	\${POLY:POLY.SP.4,Description}	\${POLY:POLY.SP.4,Value}
POLY.LN.1	\${POLY:POLY.LN.1,Description}	\${POLY:POLY.LN.1,Value}
POLY.E.1	\${POLY:POLY.E.1,Description}	\${POLY:POLY.E.1,Value}
POLY.E.2	\${POLY:POLY.E.2,Description}	\${POLY:POLY.E.2,Value}
POLY.E.1.DFM	\${POLY:POLY.E.1.DFM,Description}	\${POLY:POLY.E.1.DFM,Value}
POLY.E.2.DFM	\${POLY:POLY.E.2.DFM,Description}	\${POLY:POLY.E.2.DFM,Value}
POLY.SE.1	\${POLY:POLY.SE.1,Description}	\${POLY:POLY.SE.1,Value}
POLY.SE.2	 \${POLY:POLY.SE.2,Description}	\${POLY:POLY.SE.2,Value}
POLY.E.3	 \${POLY:POLY.E.3,Description}	 \${POLY:POLY.E.3,Value}
POLY.W.6	 \${POLY:POLY.W.6,Description}	 \${POLY:POLY.W.6,Value}
POLY.SP.5	 \${POLY:POLY.SP.5,Description}	 \${POLY:POLY.SP.5,Value}
POLY.X.1	Bent gate in not allowed	---
.. ..	.. ..	.. ..





## POLY RULES (continued)



### assuraDRC Native Code

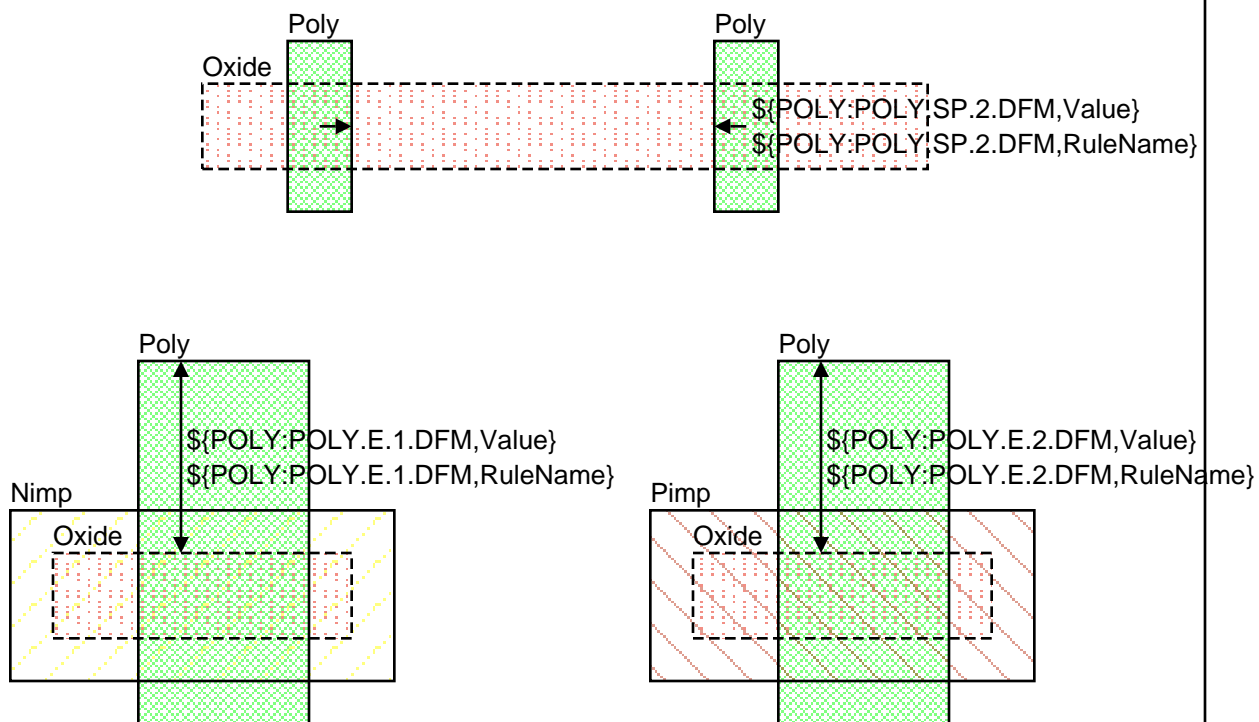
```

inpo2 = geomAndNot(Poly Oxide)
pol2_longp1 = drc( inpo2 area > 0.08* 20.0 )
pol2_longp = geomOr(pol2_longp1 gate)
copo = geomAnd(Cont Poly)
pol21_x = geomButtOrOver( pol2_longp copo )
pol22_check_copo = geomButtOrOver( copo pol21_x )
pol23_a = geomSizeAnd( pol22_check_copo pol21_x 0.11* 0.8 20.0/2 )
pol24_linen = geomButtOrOver( pol21_x pol23_a keep == 1 )
pol25_p2p = geomButtOrOver( pol21_x pol23_a keep > 1 )
pol26_b = geomButtOrOver( pol23_a pol24_linen )
pol27_c = geomSizeAnd( pol26_b pol24_linen 0.11* 0.8 20.0/2 )
linen_not1 = geomAndNot(pol24_linen pol27_c)
p2p_not1 = geomAndNot(pol25_p2p pol23_a)
pol28_bad = geomOr(linen_not1 p2p_not1)
pol29_bad_edge = geomGetEdge(pol28_bad coincident Poly)
pol210_err = drc( pol29_bad_edge width <= 0.16 )
errorLayer( geomButtOrOver( pol21_x pol210_err )
  "POLY.LN.1 Maximum Poly length [Poly width is <= 0.16 um] between two contacts as well..."

```

## POLY RULES (continued)

switch CHECK\_DFM



switch CHECK\_DENSITY

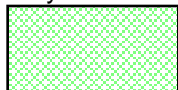
Density

ratio  $\leq 0.5$

id: POLY.D.1

message: Poly density must be  $\leq 50\%$

Poly

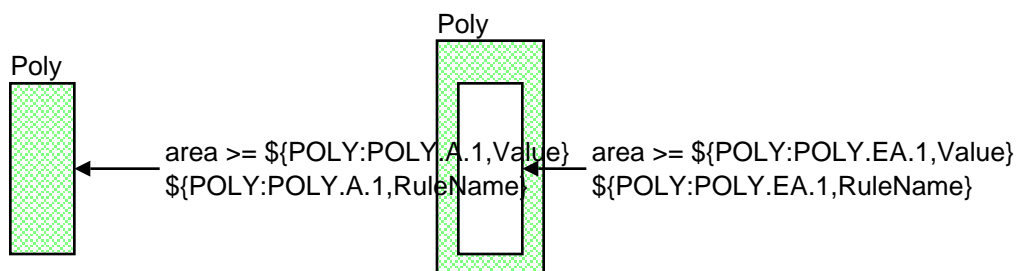


rule POLY\_SE\_3



error

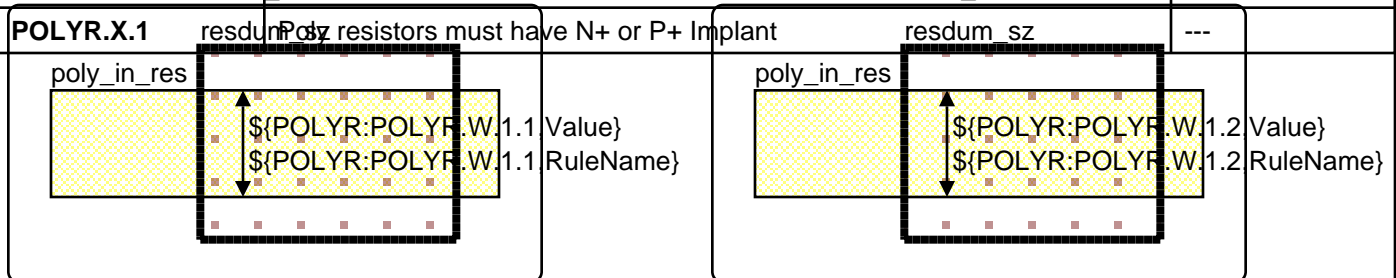
$\{\text{POLY:POLY.SE.3,RuleName}\}$



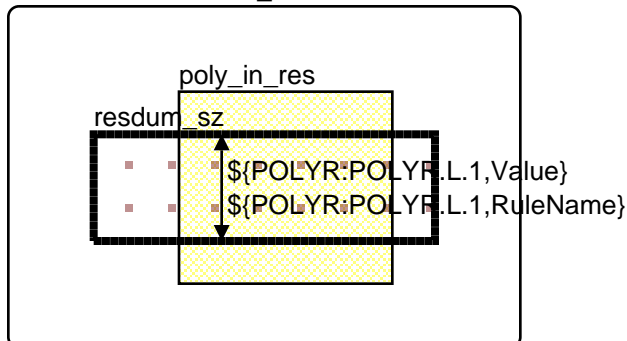
## POLY RESISTOR RULES (salicided/non-salicided)

Data Table: POLYR\_DRC

RuleName	Description	Value
<b>POLYR.W.1.1</b>	\${POLYR:POLYR.W.1.1,Description}	\${POLYR:POLYR.W.1.1,Value}
<b>POLYR.W.1.2</b>	\${POLYR:POLYR.W.1.2,Description}	\${POLYR:POLYR.W.1.2,Value}
<b>POLYR.L.1</b>	\${POLYR:POLYR.L.1,Description}	\${POLYR:POLYR.L.1,Value}
<b>POLYR.SE.1</b>	\${POLYR:POLYR.SE.1,Description}	\${POLYR:POLYR.SE.1,Value}
<b>POLYR.E.1</b>	<p>Poly resistor is defined by the intersection of Poly and Resdum for DRC and LVS.</p> <p>For salicided Poly resistors, the Resdum shape must butt the contacts on both ends of Poly the</p>	\${POLYR:POLYR.E.1,Value}
<b>POLYR.E.2</b>	<p>resistor and the Resdum shape must be coincident or extend beyond the Poly edges along the length of the Poly resistor.</p> <p>For non-salicided Poly resistors, the Resdum shape must be coincident with the edges of the Siprot</p>	\${POLYR:POLYR.E.2,Value}
<b>POLYR.E.3</b>	<p>that crosses the width of the Poly resistor and the Resdum shape must be coincident or extend beyond the Poly edges along the length of the Poly resistor.</p>	\${POLYR:POLYR.E.3,Value}
<b>POLYR.SE.2</b>	<p>switch !SUGGESTED_CHECK</p> <p>switch SUGGESTED_CHECK</p>	\${POLYR:POLYR.SE.2,Value}

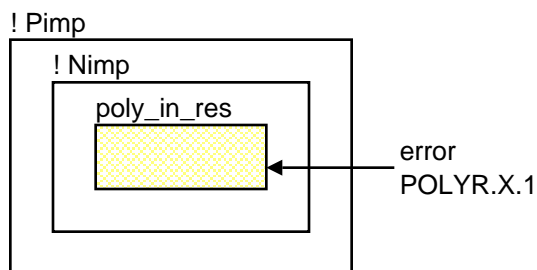
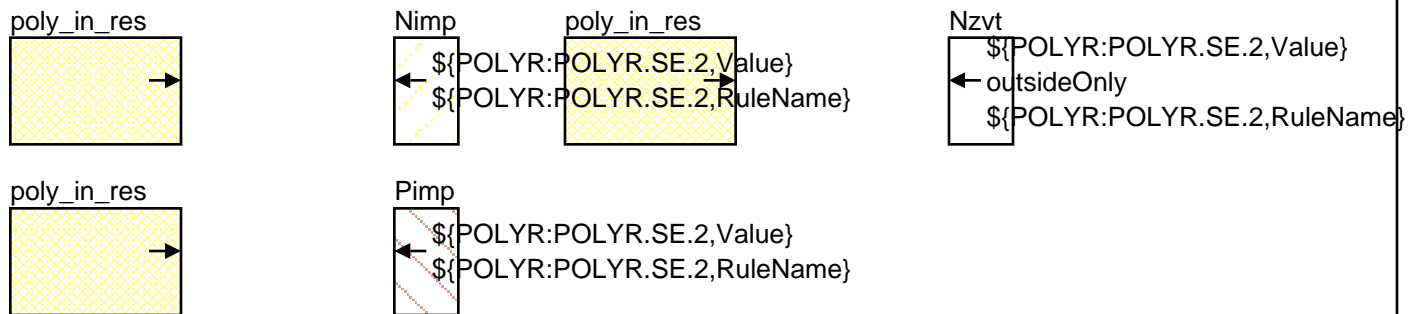
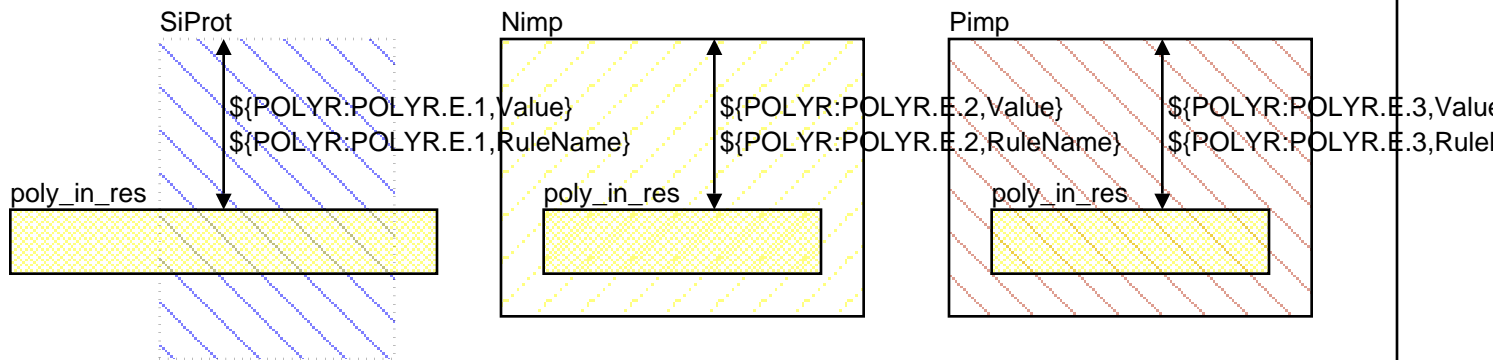


switch SUGGESTED\_CHECK



**POLYR.SE.1 is checked by  
SIPROT.SE.1**

## POLY RESISTOR RULES (continued)



## Data Table: NIMP DRC

<b>NIMP.E.4</b>	$\{NIMP:NIMP.E.4, Description\}$	Nimp	$\{NIMP:NIMP.E.4, Value\}$
<b>NIMP.SE.3</b>	$\{NIMP:NIMP.W.1, Value\}$ $\{NIMP:NIMP.W.1, RuleName\}$	Nimp $\{NIMP:NIMP.SP.1, Value\}$ $\{NIMP:NIMP.SP.1, RuleName\}$	$\{NIMP:NIMP.E.1, Value\}$ $\{NIMP:NIMP.E.1, RuleName\}$
<b>NIMP.A.1</b>	$\{NIMP:NIMP.A.1, Description\}$		$\{NIMP:NIMP.A.1, Value\}$
<b>NIMP.EA.1</b>	$\{NIMP:NIMP.EA.1, Description\}$		$\{NIMP:NIMP.EA.1, Value\}$
<b>NIMP.X.1</b>	N+ Implant is NOT allowed over P+ Implant	Nwell	---

Diagram illustrating the relationship between NIMP and NIMP.X.1. NIMP is a yellow hatched rectangle. NIMP.X.1 is a white rectangle. NIMP is divided into Nimp (yellow hatched) and Nwell (white) regions. NIMP.X.1 is divided into N+ Implant (white) and P+ Implant (yellow hatched) regions. The diagram shows that NIMP.X.1 is not allowed over P+ Implant.

<b>NIMP.O.1</b>	$\{NIMP:NIMP.O.1, Value\}$ $\{NIMP:NIMP.O.1, RuleName\}$	! Oxide	
<b>NIMP.SE.1</b>	$\{NIMP:NIMP.SE.1, Value\}$ $\{NIMP:NIMP.SE.1, RuleName\}$	Pimp	

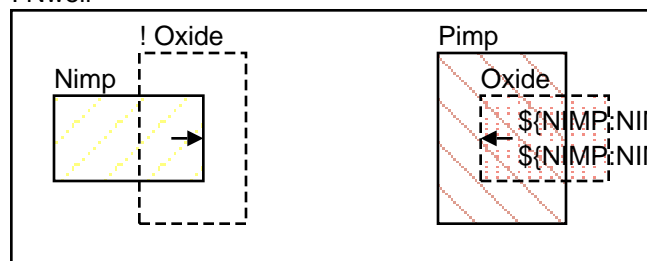
Diagram illustrating the relationship between NIMP.O.1 and NIMP.SE.1. NIMP.O.1 is a yellow hatched rectangle. NIMP.SE.1 is a white rectangle. NIMP.O.1 is divided into Nimp (yellow hatched) and Nwell (white) regions. NIMP.SE.1 is divided into Pimp (white) and Oxide (yellow hatched) regions. The diagram shows that NIMP.O.1 is not allowed over Pimp.

<b>NIMP.E.2</b>	$\{NIMP:NIMP.E.2, Value\}$ $\{NIMP:NIMP.E.2, RuleName\}$	Nimp	
<b>NIMP.E.3</b>	$\{NIMP:NIMP.E.3, Value\}$ $\{NIMP:NIMP.E.3, RuleName\}$	Poly	

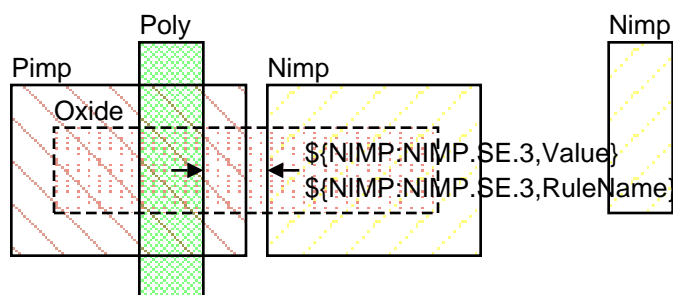
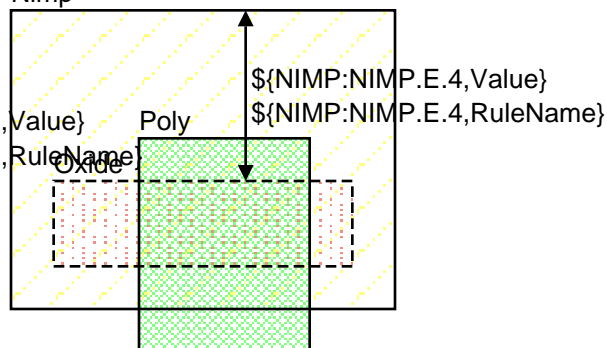
Diagram illustrating the relationship between NIMP.E.2 and NIMP.E.3. NIMP.E.2 is a yellow hatched rectangle. NIMP.E.3 is a white rectangle. NIMP.E.2 is divided into Nimp (yellow hatched) and Nwell (white) regions. NIMP.E.3 is divided into Nimp (yellow hatched) and Poly (green hatched) regions. The diagram shows that NIMP.E.2 is not allowed over Poly.

**N+ IMPLANT RULES (continued)**

! Nwell



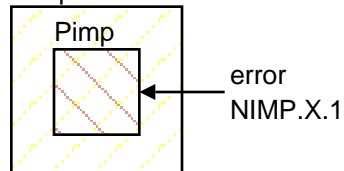
Nimp



area >=  $\$(NIMP:NIMP.A.1,Value)$   
 $\$(NIMP:NIMP.A.1,RuleName)$

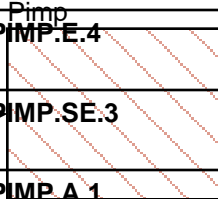
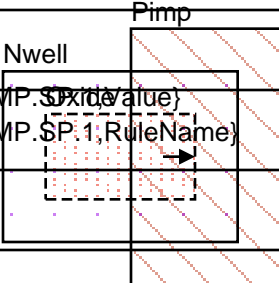
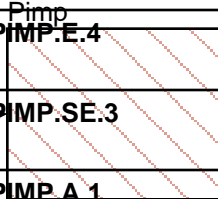
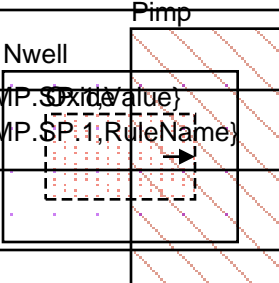
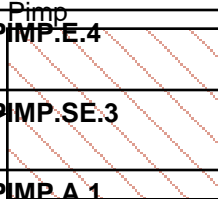
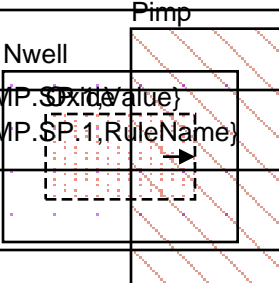
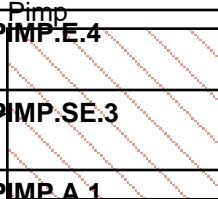
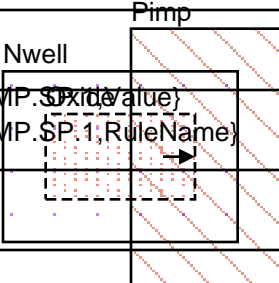
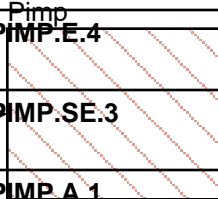
area >=  $\$(NIMP:NIMP.EA.1,Value)$   
 $\$(NIMP:NIMP.EA.1,RuleName)$

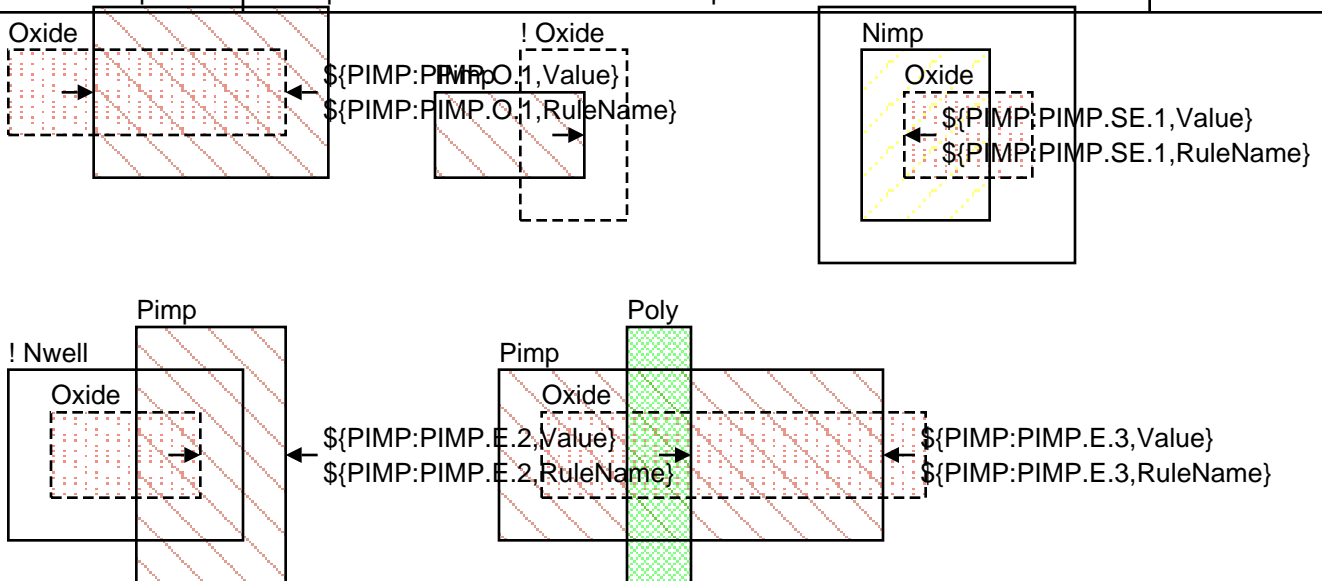
Nimp



## P+ IMPLANT RULES

Data Table: PIMP\_DRC

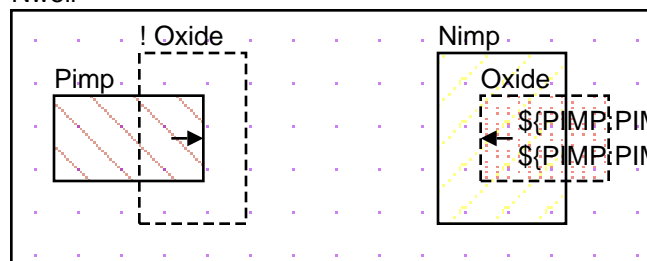
RuleName	Description	Value
PIMP.W.1	\${PIMP:PIMP.W.1,Description}	\${PIMP:PIMP.W.1,Value}
PIMP.SP.1	\${PIMP:PIMP.SP.1,Description}	\${PIMP:PIMP.SP.1,Value}
PIMP.E.1	\${PIMP:PIMP.E.1,Description}	\${PIMP:PIMP.E.1,Value}
PIMP.O.1	\${PIMP:PIMP.O.1,Description}	\${PIMP:PIMP.O.1,Value}
PIMP.SE.1	\${PIMP:PIMP.SE.1,Description}	\${PIMP:PIMP.SE.1,Value}
PIMP.E.2	\${PIMP:PIMP.E.2,Description}	\${PIMP:PIMP.E.2,Value}
PIMP.E.3	\${PIMP:PIMP.E.3,Description}	\${PIMP:PIMP.E.3,Value}
PIMP.SE.2	\${PIMP:PIMP.SE.2,Description}	\${PIMP:PIMP.SE.2,Value}
PIMP.E.4	 \${PIMP:PIMP.E.4,Description}	 \${PIMP:PIMP.E.4,Value}
PIMP.SE.3	 \${PIMP:PIMP.W.1,Value} \${PIMP:PIMP.W.1,RuleName}	 \${PIMP:PIMP.SP.1,RuleName}
PIMP.A.1	 \${PIMP:PIMP.A.1,Description}	 \${PIMP:PIMP.E.1,Value} \${PIMP:PIMP.E.1,RuleName}
PIMP.EA.1	 \${PIMP:PIMP.EA.1,Description}	 \${PIMP:PIMP.EA.1,Value}
PIMP.X.1	 P+ Implant is NOT allowed over N+ Implant ! Nwell	---



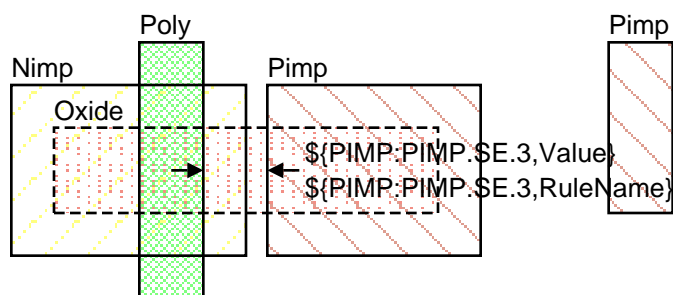
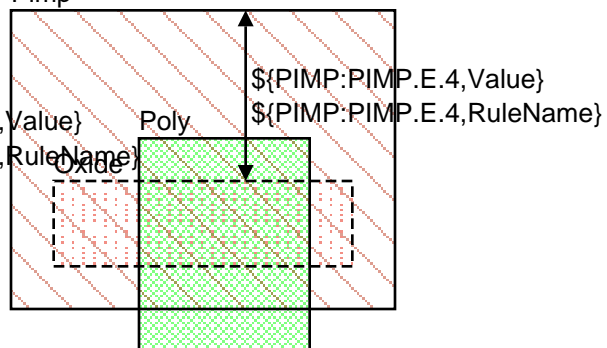


## P+ IMPLANT RULES (continued)

Nwell



Pimp



area >= \$(PIMP:PIMP.A.1,Value)  
\$(PIMP:PIMP.A.1,RuleName)

area >= \$(PIMP:PIMP.EA.1,Value)  
\$(PIMP:PIMP.EA.1,RuleName)

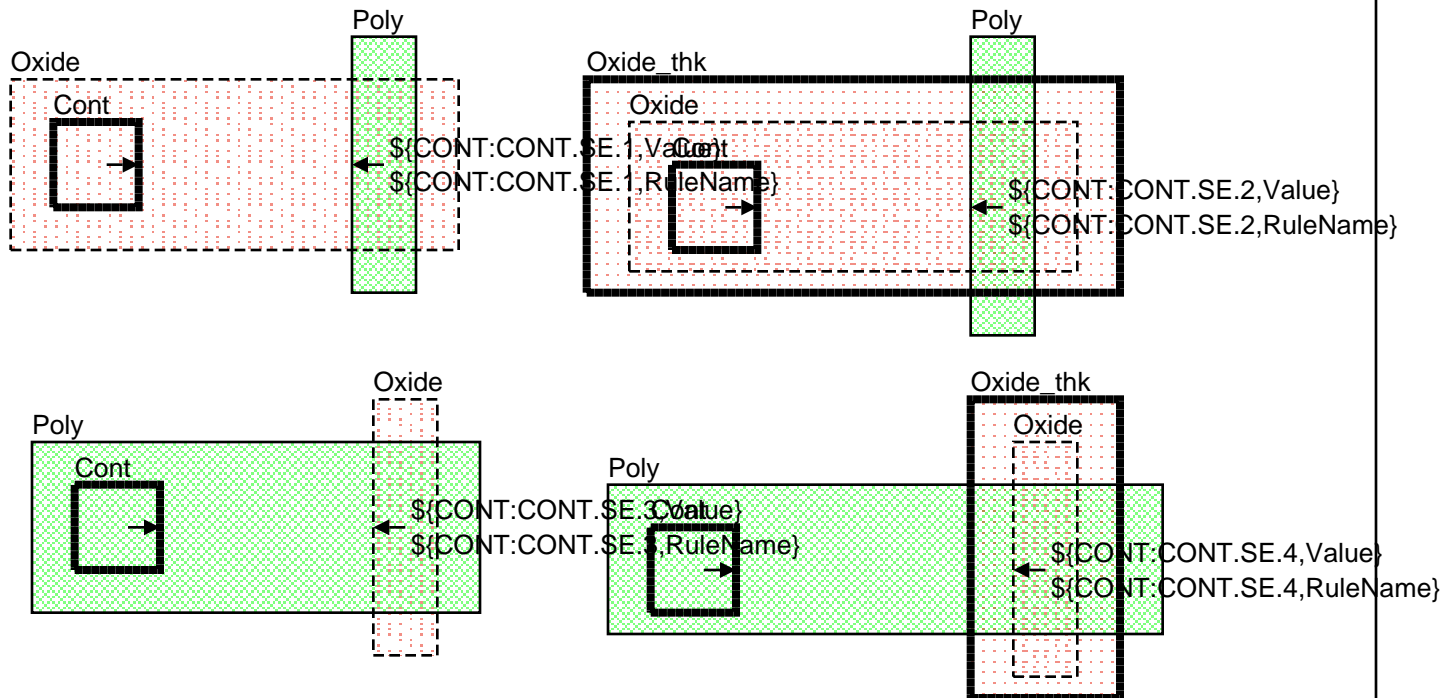
PIMP.X.1 - Covered by NIMP.X.1.

## CONTACT RULES

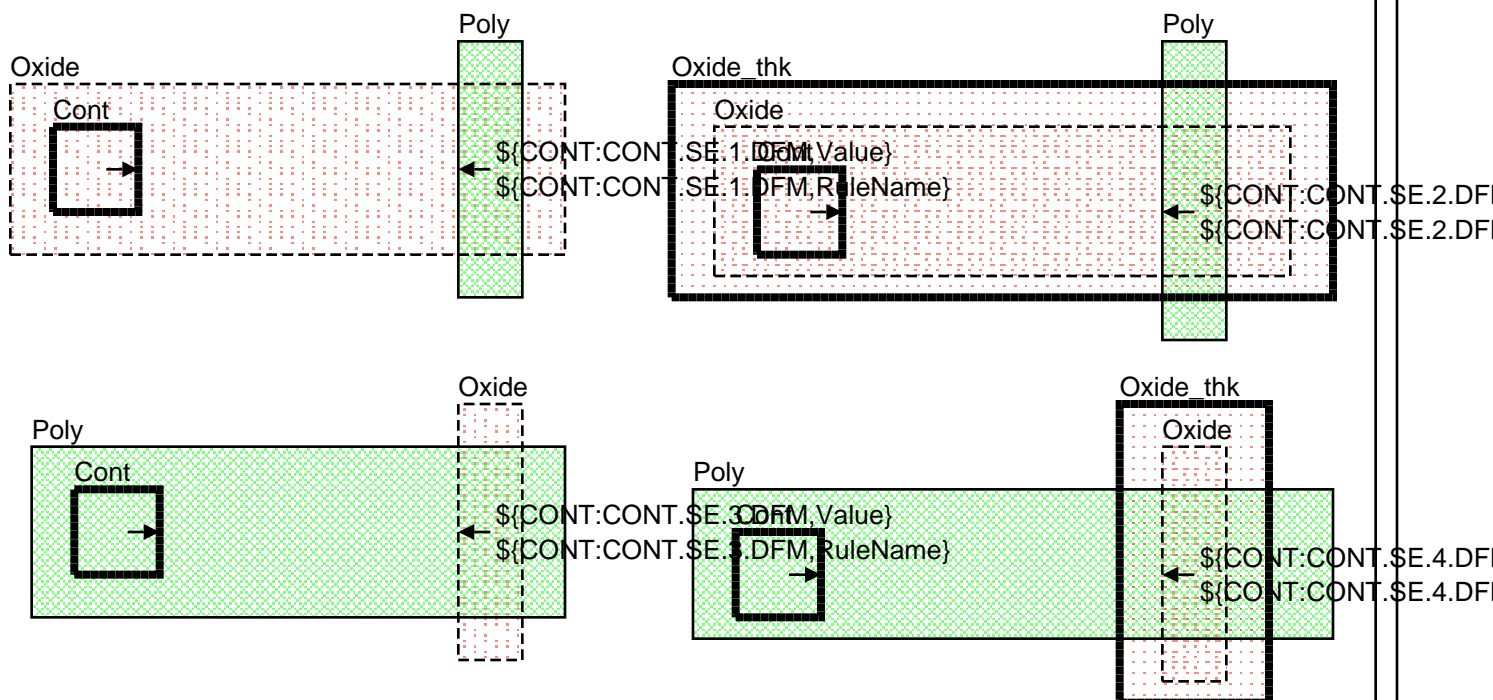
Data Table: CONT\_DRC

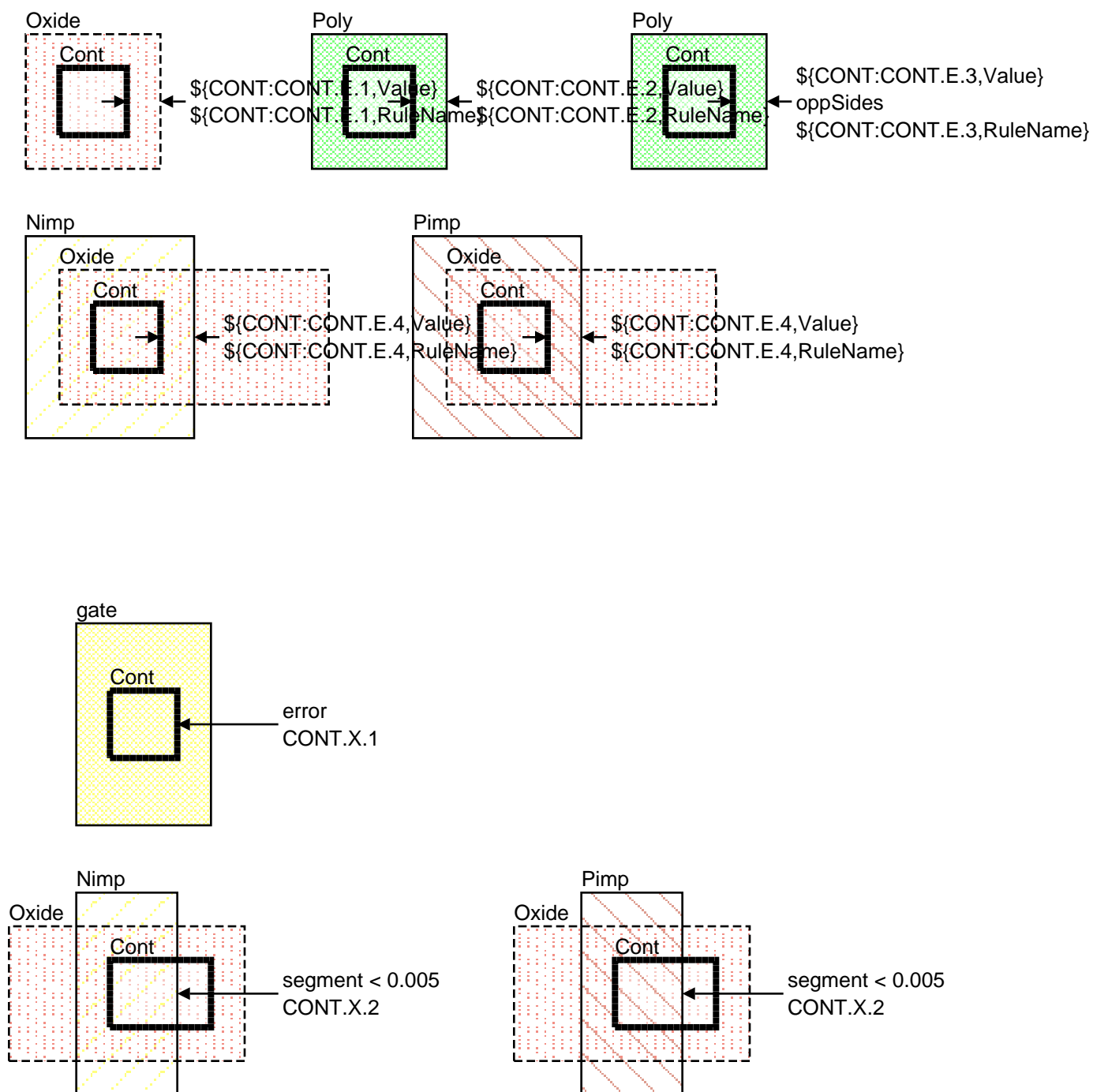
RuleName	Description	Value
CONT.W.1	\${CONT:CONT.W.1,Description}	\${CONT:CONT.W.1,Value}
CONT.SP.1	\${CONT:CONT.SP.1,Description}	\${CONT:CONT.SP.1,Value}
CONT.SP.2	\${CONT:CONT.SP.2,Description}	\${CONT:CONT.SP.2,Value}
CONT.SE.1	\${CONT:CONT.SE.1,Description}	\${CONT:CONT.SE.1,Value}
CONT.SE.2	\${CONT:CONT.SE.2,Description}	\${CONT:CONT.SE.2,Value}
CONT.SE.3	\${CONT:CONT.SE.3,Description}	\${CONT:CONT.SE.3,Value}
CONT.SE.4	\${CONT:CONT.SE.4,Description}	\${CONT:CONT.SE.4,Value}
CONT.SE.1.DFM	\${CONT:CONT.SE.1.DFM,Description}	\${CONT:CONT.SE.1.DFM,Value}
CONT.SE.2.DFM	\${CONT:CONT.SE.2.DFM,Description}	\${CONT:CONT.SE.2.DFM,Value}
CONT.SE.3.DFM	\${CONT:CONT.SE.3.DFM,Description}	\${CONT:CONT.SE.3.DFM,Value}
CONT.SE.4.DFM	$\frac{\$ \{ \text{CONT:CONT.W.1,Value} \} \times \$ \{ \text{CONT:CONT.SP.1,Value} \}}{\$ \{ \text{CONT:CONT.W.1,RuleName} \} \times \$ \{ \text{CONT:CONT.SP.1,RuleName} \}}$	$\frac{\$ \{ \text{CONT:CONT.W.1,Value} \} \times \$ \{ \text{CONT:CONT.SP.1,Value} \}}{\$ \{ \text{CONT:CONT.W.1,RuleName} \} \times \$ \{ \text{CONT:CONT.SP.1,RuleName} \}}$
CONT.E.1	$\frac{\$ \{ \text{CONT:CONT.E.1,Description} \}}{\text{cont\_cluster\_lt\_pt1} \times \text{cont\_cluster\_lt\_pt1}}$	\${CONT:CONT.E.1,Value}
CONT.E.2	$\frac{\$ \{ \text{CONT:CONT.E.2,Description} \}}{\$ \{ \text{CONT:CONT.SP.2,Value} \} \times \$ \{ \text{CONT:CONT.SP.2,RuleName} \}}$	\${CONT:CONT.E.2,Value}
CONT.E.3	\${CONT:CONT.E.3,Description}	\${CONT:CONT.E.3,Value}
CONT.E.4	\${CONT:CONT.E.4,Description}	\${CONT:CONT.E.4,Value}
CONT.X.1	Contact on gate is NOT allowed	---
CONT.X.2	Active Area Contact on N+/P+ Implant edge is NOT allowed	---
CONT.X.3	Contact must be covered by Metal1 and Active Area or Poly	---

## CONTACT RULES (continued)



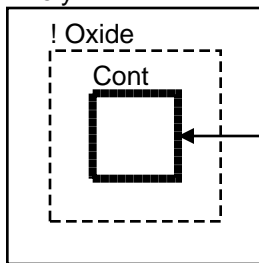
switch CHECK\_DFM



**CONTACT RULES (continued)**

**CONTACT RULES (continued)**

! Poly



error  
CONT.X.3



## METAL 1 RULES

Data Table: METAL1\_DRC

RuleName	Description	Value
<b>METAL1.W.1</b>	\${METAL1:METAL1.W.1,Description}	\${METAL1: METAL1.W.1, Value}
<b>METAL1.W.2</b>	\${METAL1:METAL1.W.2,Description}	\${METAL1: METAL1.W.2, Value}
<b>METAL1.SP.1.1</b>	\${METAL1:METAL1.SP.1.1,Description}	\${METAL1: METAL1.SP.1.1, Value}
<b>METAL1.SP.1.2</b>	\${METAL1:METAL1.SP.1.2,Description}	\${METAL1: METAL1.SP.1.2, Value}
<b>METAL1.SP.1.3</b>	\${METAL1:METAL1.SP.1.3,Description}	\${METAL1: METAL1.SP.1.3, Value}
<b>METAL1.SP.1.4</b>	\${METAL1:METAL1.SP.1.4,Description}	\${METAL1: METAL1.SP.1.4, Value}
<b>METAL1.SP.1.5</b>	\${METAL1:METAL1.SP.1.5,Description}	\${METAL1: METAL1.SP.1.5, Value}
<b>METAL1.SP.1.6</b>	\${METAL1:METAL1.SP.1.6,Description}	\${METAL1: METAL1.SP.1.6, Value}
<b>METAL1.E.1</b>	\${METAL1:METAL1.E.1,Description}	\${METAL1: METAL1.E.1, Value}
<b>METAL1.E.2</b>	\${METAL1:METAL1.E.2,Description}	\${METAL1: METAL1.E.2, Value}
<b>METAL1.L.1</b>	\${METAL1:METAL1.L.1,Description}	\${METAL1: METAL1.L.1, Value}
<b>METAL1.SP.2</b>	\${METAL1:METAL1.SP.2,Description}	\${METAL1: METAL1.SP.2, Value}
<b>METAL1.SP.3</b>	\${METAL1:METAL1.SP.3,Description}	\${METAL1: METAL1.SP.3, Value}
<b>METAL1.W.3</b>	\${METAL1:METAL1.W.3,Description}	\${METAL1: METAL1.W.3, Value}
.. ..	.. .. .. ..	.. ..

**METAL k (k = 2, 3, 4, 5, 6, 7, 8, 9) RULES**

Comment Table METAL k ( k = 2, 3, 4, 5, 6, 7, 8, 9) RULES

Rule Name	Value (um)	Description
METALk.W.1	0.08	Minimum Metal k width.
METALk.W.2	6.0	Maximum Metal k width.
METALk.SP.1.1	0.07	Minimum Metal k to Metal k spacing.
		Minimum Metal k to Metal k spacing if:
METALk.SP.1.2	0.15	one Metal k width > 0.10 and parallel length > 0.32
METALk.SP.1.3	0.25	one Metal k width > 0.75 and parallel length > 0.75
METALk.SP.1.4	0.45	one Metal k width > 1.5 and parallel length > 1.5
METALk.SP.1.5	0.75	one Metal k width > 2.5 and parallel length > 2.5.
METALk.SP.1.6	1.25	one Metal k width > 3.5 and parallel length > 3.5.
METALk.E.1	0.005	Minimum Metal k enclosure of Via k-1.
METALk.E.2	0.03	Minimum Metal k enclosure of Via k-1on at least two opposite sides.
METALk.L.1	0.1	Minimum bent Metal k (45 degree angle) length.
METALk.SP.2	0.1	Minimum bent Metal k (45 degree angle) space.
METALk.SP.3	0.08	Space at Metalk line-end ( $W < 0.1$ , $Q = 0.1$ ) (dense-line-end) If Metalk has parallel run length with opposite Metalk (measured with $T=0.035$ extension) along 2 adjacent edges of Metalk [any one edge $< Q$ distance from the corner of the two edges], then one of the space (S1 or S2) must be (k=2-9) (check does not include jog with edge $< 0.07u$ )
METALk.W.3	0.09	Minimum bent Metal k (45 degree angle) width.
METALk.A.1	0.02	Minimum Metal k area.
METALk.EA.1	0.055	Minimum Metal k enclosed area.
METALk.D.1	> 20% < 65%	Metal k Density range over any 120um x 120um area (checked by stepping in 60um increments).
METALk.D.2	< 60%	Maximum Metal k density over any 600um x 600um area (checked by stepping in 300um increments).

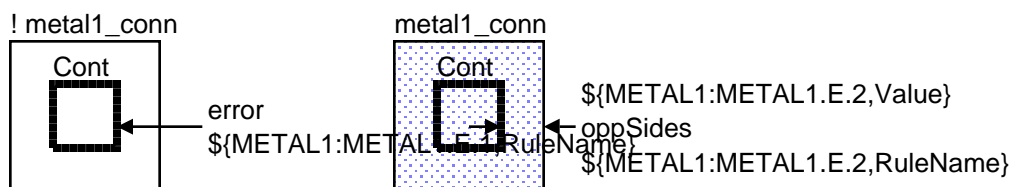


## METAL k (k = 10, 11) RULES

Comment Table METAL k (k = 10, 11) RULES

Rule Name	Value (um)	Description
METALk.W.1	0.22	Minimum Metal k width.
METALk.W.2	6.0	Maximum Metal k width.
METALk.SP.1.1	0.20	Minimum Metal k to Metal k spacing.
		Minimum Metal k to Metal k spacing if:
METALk.SP.1.2	0.35	one Metal k width > 0.75 and parallel length > 0.75
METALk.SP.1.3	0.45	one Metal k width > 1.50 and parallel length > 1.50
METALk.SP.1.4	0.75	one Metal k width > 2.50 and parallel length > 2.50.
METALk.SP.1.5	1.25	one Metal k width > 3.5 and parallel length > 3.5.
METALk.E.1	0.03	Minimum Metal k overlap of Via k-1.
METALk.E.2	0.05	Minimum Metal k overlap of Via k-1 on at least two opposite sides.
METALk.A.1	0.10	Minimum Metal k area.
METALk.EA.1	0.11	Minimum Metal k enclosed area.
METALk.D.1	> 20% < 65%	Metal k Density range over any 120um x 120um area (checked by stepping in 60um increments).
METALk.D.2	< 60%	Maximum Metal k density over any 600um x 600um area (checked by stepping in 300um increments).

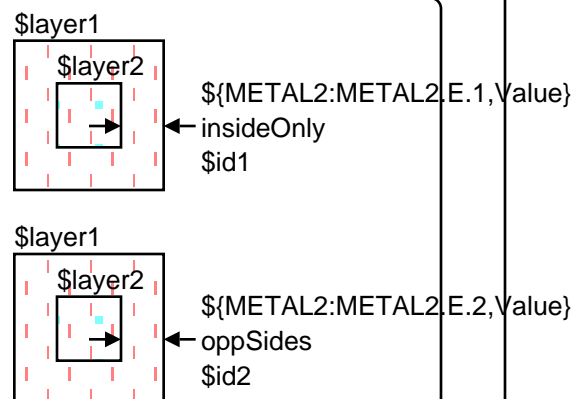
## METAL RULES (continued)



macro

Macro Table

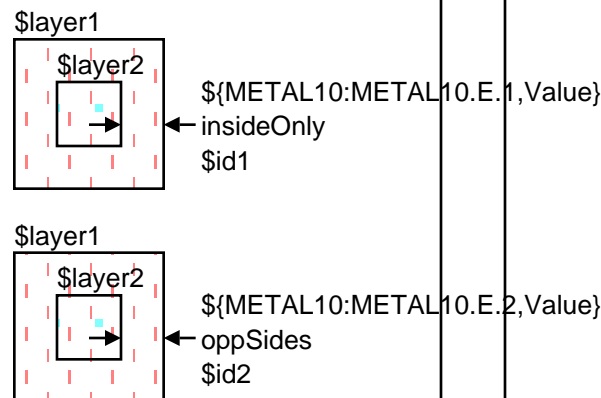
\$name1	\$layer1	\$layer2	\$id1	\$id2
Metal2	metal2_conn	Via1	METAL2.E.1	METAL2.E.2
Metal3	metal3_conn	Via2	METAL3.E.1	METAL3.E.2
Metal4	metal4_conn	Via3	METAL4.E.1	METAL4.E.2
Metal5	metal5_conn	Via4	METAL5.E.1	METAL5.E.2
Metal6	metal6_conn	Via5	METAL6.E.1	METAL6.E.2
Metal7	metal7_conn	Via6	METAL7.E.1	METAL7.E.2
Metal8	metal8_conn	Via7	METAL8.E.1	METAL8.E.2
Metal9	metal9_conn	Via8	METAL9.E.1	METAL9.E.2



macro

Macro Table

\$name1	\$layer1	\$layer2	\$id1	\$id2
Metal10	Metal10	Via9	METAL10.E.1	METAL10.E.2
Metal11	Metal11	Via10	METAL11.E.1	METAL11.E.2



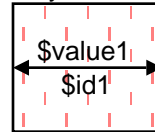
## METAL RULES (continued)

macro

Macro Table

\$layer1	\$name1	\$id1	\$value1
metal1_conn	Metal1	METAL1.W.1	0.06
metal2_conn	Metal2	METAL2.W.1	0.08
metal3_conn	Metal3	METAL3.W.1	0.08
metal4_conn	Metal4	METAL4.W.1	0.08
metal5_conn	Metal5	METAL5.W.1	0.08
metal6_conn	Metal6	METAL6.W.1	0.08
metal7_conn	Metal7	METAL7.W.1	0.08
metal8_conn	Metal8	METAL8.W.1	0.08
metal9_conn	Metal9	METAL9.W.1	0.08
Metal10	Metal10	METAL10.W.1	0.22
Metal11	Metal11	METAL11.W.1	0.22

\$layer1



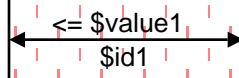
macro

! Bondpad

! \$layer3

! \$layer2

\$layer1



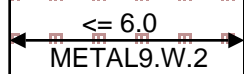
Macro Table

\$layer1	\$layer2	\$layer3	\$name1	\$id1	\$value1
metal1_conn	cont_array_zone	via1_array_zone	Metal1	METAL1.W.2	6.0
metal2_conn	via1_array_zone	via2_array_zone	Metal2	METAL2.W.2	6.0
metal3_conn	via2_array_zone	via3_array_zone	Metal3	METAL3.W.2	6.0
metal4_conn	via3_array_zone	via4_array_zone	Metal4	METAL4.W.2	6.0
metal5_conn	via4_array_zone	via5_array_zone	Metal5	METAL5.W.2	6.0
metal6_conn	via5_array_zone	via6_array_zone	Metal6	METAL6.W.2	6.0
metal7_conn	via6_array_zone	via7_array_zone	Metal7	METAL7.W.2	6.0
metal8_conn	via7_array_zone	via8_array_zone	Metal8	METAL8.W.2	6.0

! Bondpad

! via6\_array\_zone

Metal9



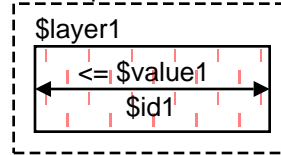
## METAL RULES (continued)

macro

Macro Table

\$layer1	\$name1	\$id1	\$value1
Metal10	Metal10	METAL10.W.2	6.0
Metal11	Metal11	METAL11.W.2	6.0

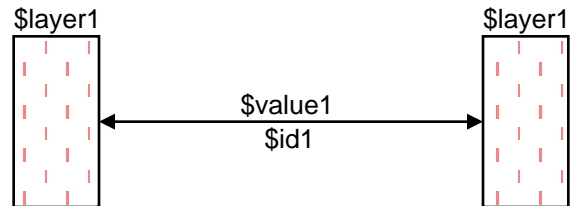
! Bondpad



macro

Macro Table

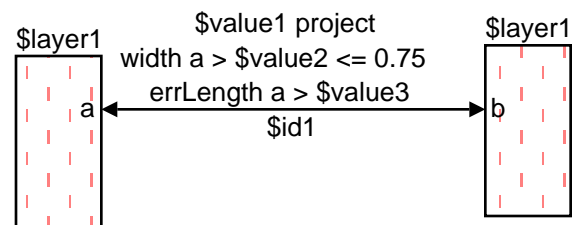
\$layer1	\$id1	\$value1
Metal1	METAL1.SP.1.1	0.06
Metal2	METAL2.SP.1.1	0.07
Metal3	METAL3.SP.1.1	0.07
Metal4	METAL4.SP.1.1	0.07
Metal5	METAL5.SP.1.1	0.07
Metal6	METAL6.SP.1.1	0.07
Metal7	METAL7.SP.1.1	0.07
Metal8	METAL8.SP.1.1	0.07
Metal9	METAL9.SP.1.1	0.07
Metal10	METAL10.SP.1.1	0.20
Metal11	METAL11.SP.1.1	0.20



macro

Macro Table

\$layer1	\$id1	\$value1	\$value2	\$value3
Metal1	METAL1.SP.1.2	0.1	0.1	0.32
Metal2	METAL2.SP.1.2	0.15	0.1	0.32
Metal3	METAL3.SP.1.2	0.15	0.1	0.32
Metal4	METAL4.SP.1.2	0.15	0.1	0.32
Metal5	METAL5.SP.1.2	0.15	0.1	0.32
Metal6	METAL6.SP.1.2	0.15	0.1	0.32
Metal7	METAL7.SP.1.2	0.15	0.1	0.32
Metal8	METAL8.SP.1.2	0.15	0.1	0.32
Metal9	METAL9.SP.1.2	0.15	0.1	0.32

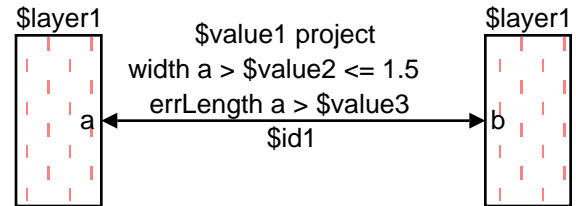


## METAL RULES (continued)

macro

Macro Table

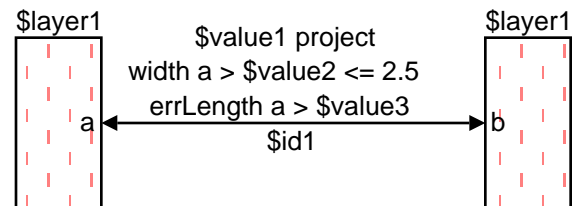
\$layer1	\$id1	\$value1	\$value2	\$value3
Metal1	METAL1.SP.1.3	0.25	0.75	0.75
Metal2	METAL2.SP.1.3	0.25	0.75	0.75
Metal3	METAL3.SP.1.3	0.25	0.75	0.75
Metal4	METAL4.SP.1.3	0.25	0.75	0.75
Metal5	METAL5.SP.1.3	0.25	0.75	0.75
Metal6	METAL6.SP.1.3	0.25	0.75	0.75
Metal7	METAL7.SP.1.3	0.25	0.75	0.75
Metal8	METAL8.SP.1.3	0.25	0.75	0.75
Metal9	METAL9.SP.1.3	0.25	0.75	0.75
Metal10	METAL10.SP.1.2	0.35	0.75	0.75
Metal11	METAL11.SP.1.2	0.35	0.75	0.75



macro

Macro Table

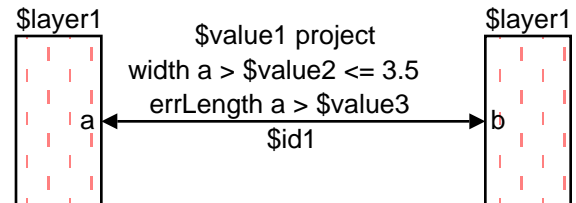
\$layer1	\$id1	\$value1	\$value2	\$value3
Metal1	METAL1.SP.1.4	0.45	1.5	1.5
Metal2	METAL2.SP.1.4	0.45	1.5	1.5
Metal3	METAL3.SP.1.4	0.45	1.5	1.5
Metal4	METAL4.SP.1.4	0.45	1.5	1.5
Metal5	METAL5.SP.1.4	0.45	1.5	1.5
Metal6	METAL6.SP.1.4	0.45	1.5	1.5
Metal7	METAL7.SP.1.4	0.45	1.5	1.5
Metal8	METAL8.SP.1.4	0.45	1.5	1.5
Metal9	METAL9.SP.1.4	0.45	1.5	1.5
Metal10	METAL10.SP.1.3	0.45	1.5	1.5
Metal11	METAL11.SP.1.3	0.45	1.5	1.5



macro

Macro Table

\$layer1	\$id1	\$value1	\$value2	\$value3
Metal1	METAL1.SP.1.5	0.75	2.5	2.5
Metal2	METAL2.SP.1.5	0.75	2.5	2.5
Metal3	METAL3.SP.1.5	0.75	2.5	2.5
Metal4	METAL4.SP.1.5	0.75	2.5	2.5
Metal5	METAL5.SP.1.5	0.75	2.5	2.5
Metal6	METAL6.SP.1.5	0.75	2.5	2.5
Metal7	METAL7.SP.1.5	0.75	2.5	2.5
Metal8	METAL8.SP.1.5	0.75	2.5	2.5
Metal9	METAL9.SP.1.5	0.75	2.5	2.5
Metal10	METAL10.SP.1.4	0.75	2.5	2.5
Metal11	METAL11.SP.1.4	0.75	2.5	2.5

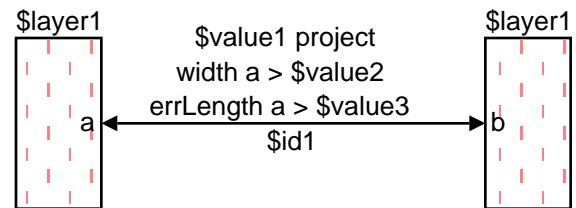


## METAL RULES (continued)

macro

Macro Table

\$layer1	\$id1	\$value1	\$value2	\$value3
Metal1	METAL1.SP.1.6	1.25	3.5	3.5
Metal2	METAL2.SP.1.6	1.25	3.5	3.5
Metal3	METAL3.SP.1.6	1.25	3.5	3.5
Metal4	METAL4.SP.1.6	1.25	3.5	3.5
Metal5	METAL5.SP.1.6	1.25	3.5	3.5
Metal6	METAL6.SP.1.6	1.25	3.5	3.5
Metal7	METAL7.SP.1.6	1.25	3.5	3.5
Metal8	METAL8.SP.1.6	1.25	3.5	3.5
Metal9	METAL9.SP.1.6	1.25	3.5	3.5
Metal10	METAL10.SP.1.5	1.25	3.5	3.5
Metal11	METAL11.SP.1.5	1.25	3.5	3.5

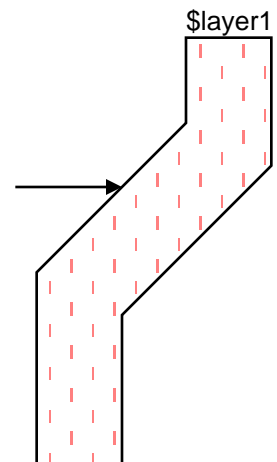


macro

Macro Table

\$layer1	\$id1	\$value1
Metal1	METAL1.L.1	0.1
Metal2	METAL2.L.1	0.1
Metal3	METAL3.L.1	0.1
Metal4	METAL4.L.1	0.1
Metal5	METAL5.L.1	0.1
Metal6	METAL6.L.1	0.1
Metal7	METAL7.L.1	0.1
Metal8	METAL8.L.1	0.1
Metal9	METAL9.L.1	0.1

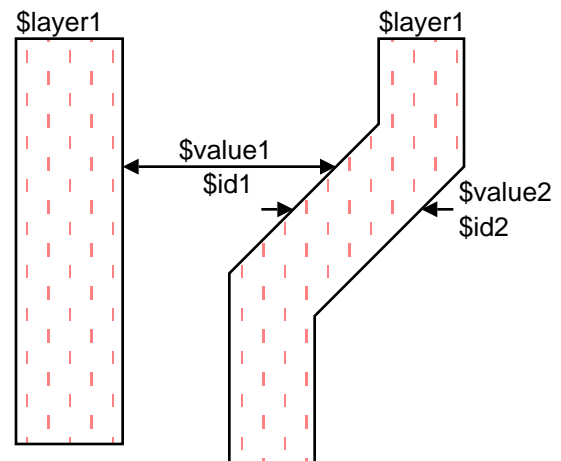
segment >= \$value1  
\$id1



macro

Macro Table

\$layer1	\$id1	\$value1	\$id2	\$value2
Metal1	METAL1.SP.2	0.1	METAL1.W.3	0.07
Metal2	METAL2.SP.2	0.1	METAL2.W.3	0.09
Metal3	METAL3.SP.2	0.1	METAL3.W.3	0.09
Metal4	METAL4.SP.2	0.1	METAL4.W.3	0.09
Metal5	METAL5.SP.2	0.1	METAL5.W.3	0.09
Metal6	METAL6.SP.2	0.1	METAL6.W.3	0.09
Metal7	METAL7.SP.2	0.1	METAL7.W.3	0.09
Metal8	METAL8.SP.2	0.1	METAL8.W.3	0.09
Metal9	METAL9.SP.2	0.1	METAL9.W.3	0.09



## METAL1.SP.3

assuraDRC Native Code

```
metx1_a=drcDenseLineEnd(Metal1 sep < 0.08 endLength(0.06 0.09) legLength(.10) endExt(.025)
legExt(0.025))
errorLayer(metx1_a "METAL1.SP.3: Min End of Line Spacing >= 0.08")
```

## METALk.SP.3 k=2-9

assuraDRC Native Code

```
metx2_a=drcDenseLineEnd(Metal2 sep < 0.08 endLength(0.07 0.1) legLength(0.1) endExt(0.035)
legExt(0.035))
errorLayer(metx2_a "METAL2.SP.3: Min End of Line Spacing >= 0.08")
```

```
metx3_a=drcDenseLineEnd(Metal3 sep < 0.08 endLength(0.07 0.1) legLength(0.1) endExt(0.035)
legExt(0.035))
errorLayer(metx3_a "METAL3.SP.3: Min End of Line Spacing >= 0.08")
```

```
metx4_a=drcDenseLineEnd(Metal4 sep < 0.08 endLength(0.07 0.1) legLength(0.1) endExt(0.035)
legExt(0.035))
errorLayer(metx4_a "METAL4.SP.3: Min End of Line Spacing >= 0.08")
```

```
metx5_a=drcDenseLineEnd(Metal5 sep < 0.08 endLength(0.07 0.1) legLength(0.1) endExt(0.035)
legExt(0.035))
errorLayer(metx5_a "METAL5.SP.3: Min End of Line Spacing >= 0.08")
```

```
metx6_a=drcDenseLineEnd(Metal6 sep < 0.08 endLength(0.07 0.1) legLength(0.1) endExt(0.035)
legExt(0.035))
errorLayer(metx6_a "METAL6.SP.3: Min End of Line Spacing >= 0.08")
```

```
metx7_a=drcDenseLineEnd(Metal7 sep < 0.08 endLength(0.07 0.1) legLength(0.1) endExt(0.035)
legExt(0.035))
errorLayer(metx7_a "METAL7.SP.3: Min End of Line Spacing >= 0.08")
```

```
metx8_a=drcDenseLineEnd(Metal8 sep < 0.08 endLength(0.07 0.1) legLength(0.1) endExt(0.035)
legExt(0.035))
errorLayer(metx8_a "METAL8.SP.3: Min End of Line Spacing >= 0.08")
```

```
metx9_a=drcDenseLineEnd(Metal9 sep < 0.08 endLength(0.07 0.1) legLength(0.1) endExt(0.035)
legExt(0.035))
errorLayer(metx9_a "METAL9.SP.3: Min End of Line Spacing >= 0.08")
```

## METAL1.SP.3

pvsDRC Native Code

```
rule METAL1.SP.3 {
caption METAL1.SP.3: Min End Of Line Spacing >= 0.08;
convex_edge Metal1 -angle1 -eq 90 -angle2 -eq 90 -with_length -lt 0.09 met1_lw;
exte met1_lw Metal1 -lt 0.08 -abut -lt 90 -metric opposite_extended 0.025 met1_sp;
edge_select -inside met1_lw met1_sp met1Edge1;
inte met1Edge1 Metal1 -lt 0.1 -abut -eq 90 -intersecting only met1_q1;
edge_length met1_q1 -ge 0.06 met1_q2;
edge_expand met1_q2 -inside_by 0.001 -extend_by 0.025 met1exp1;
edge_expand met1_q2 -inside_by 0.001 met1exp2;
not met1exp1 met1exp2 met1Exp;
select -with_edge met1Exp met1_lw met1_lwEdg;
or met1_lwEdg met1exp2 met1_allEdg;
edge_select met1_allEdg met1_q2 met1_extEdg;
edge_select -not met1_extEdg met1_sp met1_last
exte met1_last Metal1 -lt 0.08 -abut -lt 90 -metric opposite -output region ;
}
```

## METALK.SP.3 k=2-9

pvsDRC Native Code

```
rule METAL2.SP.3 {
caption METAL2.SP.3: Min End Of Line Spacing >= 0.08;
convex_edge Metal2 -angle1 -eq 90 -angle2 -eq 90 -with_length -lt 0.1 met2_lw;
exte met2_lw Metal2 -lt 0.08 -abut -lt 90 -metric opposite_extended 0.035 met2_sp;
edge_select -inside met2_lw met2_sp met2Edge1;
inte met2Edge1 Metal2 -lt 0.1 -abut -eq 90 -intersecting only met2_q1;
edge_length met2_q1 -ge 0.07 met2_q2;
edge_expand met2_q2 -inside_by 0.001 -extend_by 0.035 met2exp1;
edge_expand met2_q2 -inside_by 0.001 met2exp2;
not met2exp1 met2exp2 met2Exp;
select -with_edge met2Exp met2_lw met2_lwEdg;
or met2_lwEdg met2exp2 met2_allEdg;
edge_select met2_allEdg met2_q2 met2_extEdg;
edge_select -not met2_extEdg met2_sp met2_last
exte met2_last Metal2 -lt 0.08 -abut -lt 90 -metric opposite -output region ;
}

rule METAL3.SP.3 {
caption METAL3.SP.3: Min End Of Line Spacing >= 0.08;
convex_edge Metal3 -angle1 -eq 90 -angle2 -eq 90 -with_length -lt 0.1 met3_lw;
exte met3_lw Metal3 -lt 0.08 -abut -lt 90 -metric opposite_extended 0.035 met3_sp;
edge_select -inside met3_lw met3_sp met3Edge1;
inte met3Edge1 Metal3 -lt 0.1 -abut -eq 90 -intersecting only met3_q1;
edge_length met3_q1 -ge 0.07 met3_q2;
edge_expand met3_q2 -inside_by 0.001 -extend_by 0.035 met3exp1;
edge_expand met3_q2 -inside_by 0.001 met3exp2;
not met3exp1 met3exp2 met3Exp;
select -with_edge met3Exp met3_lw met3_lwEdg;
or met3_lwEdg met3exp2 met3_allEdg;
edge_select met3_allEdg met3_q2 met3_extEdg;
edge_select -not met3_extEdg met3_sp met3_last
exte met3_last Metal3 -lt 0.08 -abut -lt 90 -metric opposite -output region ;...
```



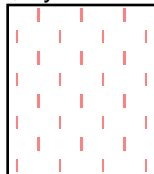
## METAL RULES (continued)

macro

Macro Table

\$layer1	\$id1	\$value1
Metal1	METAL1.A.1	0.02
Metal2	METAL2.A.1	0.02
Metal3	METAL3.A.1	0.02
Metal4	METAL4.A.1	0.02
Metal5	METAL5.A.1	0.02
Metal6	METAL6.A.1	0.02
Metal7	METAL7.A.1	0.02
Metal8	METAL8.A.1	0.02
Metal9	METAL9.A.1	0.02
Metal10	METAL10.A.1	0.10
Metal11	METAL11.A.1	0.10

\$layer1



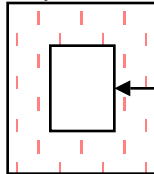
area >= \$value1  
\$id1

macro

Macro Table

\$layer1	\$id1	\$value1
Metal1	METAL1.EA.1	0.045
Metal2	METAL2.EA.1	0.055
Metal3	METAL3.EA.1	0.055
Metal4	METAL4.EA.1	0.055
Metal5	METAL5.EA.1	0.055
Metal6	METAL6.EA.1	0.055
Metal7	METAL7.EA.1	0.055
Metal8	METAL8.EA.1	0.055
Metal9	METAL9.EA.1	0.055
Metal10	METAL10.EA.1	0.11
Metal11	METAL11.EA.1	0.11

\$layer1



area >= \$value1  
\$id1

## METAL RULES (continued)

switch CHECK\_DENSITY

macro

Macro Table

\$name1	\$layer1	\$id1
Metal1	metal1_conn	METAL1.D.1
Metal2	metal2_conn	METAL2.D.1
Metal3	metal3_conn	METAL3.D.1
Metal4	metal4_conn	METAL4.D.1
Metal5	metal5_conn	METAL5.D.1
Metal6	metal6_conn	METAL6.D.1
Metal7	metal7_conn	METAL7.D.1
Metal8	metal8_conn	METAL8.D.1
Metal9	metal9_conn	METAL9.D.1
Metal10	metal10_conn	METAL10.D.1
Metal11	metal11_conn	METAL11.D.1

Density

ratio  $\geq 0.20 \leq 0.65$

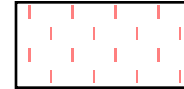
windowSize: 120.0

stepSize: 60.0

id: \$id1

message: \$name1 density must be  $\geq 20\% \leq 65\%$

\$layer1



macro

Macro Table

\$name1	\$layer1	\$id1
Metal1	metal1_conn	METAL1.D.2
Metal2	metal2_conn	METAL2.D.2
Metal3	metal3_conn	METAL3.D.2
Metal4	metal4_conn	METAL4.D.2
Metal5	metal5_conn	METAL5.D.2
Metal6	metal6_conn	METAL6.D.2
Metal7	metal7_conn	METAL7.D.2
Metal8	metal8_conn	METAL8.D.2
Metal9	metal9_conn	METAL9.D.2
Metal10	metal10_conn	METAL10.D.2
Metal11	metal11_conn	METAL11.D.2

Density

ratio  $\leq 0.60$

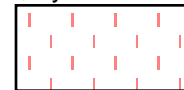
windowSize: 600.0

stepSize: 300.0

id: \$id1

message: \$name1 density must be  $\leq 60\%$

\$layer1





## VIA k (k = 1, 2, 3, 4, 5, 6, 7, 8) RULES

Comment Table VIA k (k = 1, 2, 3, 4, 5, 6, 7, 8) RULES

Rule Name	Value (um)	Description
VIAk.W.1	0.07	Minimum and maximum Via k width.
VIAk.SP.1	0.07	Minimum Via k to Via k spacing.
VIAk.SP.2	0.10	Space to three adjacent Via k (< 0.11 um apart)
VIAk.E.1	0.005	Minimum Metal k to Via k enclosure.
VIAk.E.2	0.03	Minimum Metal k to Via k enclosure on at least two opposite sides of Via k.
VIAk.E.3		At least 2 Via k must be used to join two Metal k when they are within 3.0um of a metal plate (Metal k or Metal k+1) when the metal plate size is has width > 1.5 and length > 1.5
VIAk.X.1	---	Minimum of two Via k with spacing <= 0.30um or four Via k with spacing <= 0.60um are required when connecting Metal k and Metal k+1 when one of the Metals has a width > 0.40um at the connection point.
VIAk.X.2	---	Minimum of four Via k with spacing <= 0.30um or nine Via k with spacing <= 0.60um are required when connecting Metal k and Metal k+1 when one of the Metals has a width > 1.0um at the connection point.
VIAk.X.3	---	Vias 1 through 8 may be consecutively stacked up to four high when only one Via is connecting two Metal layers for any level of the stack.
VIAk.X.4	---	Vias 1 through 8 may be consecutively stacked up more than four high when at least two Vias are connecting two Metal layers for all levels of the stack.

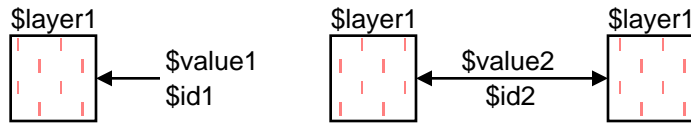
## VIA 9, 10 RULES

Comment Table VIA k (k = 9, 10) RULES

Rule Name	Value (um)	Description
VIAk.W.1	0.18	Minimum and maximum Via k width.
VIAk.SP.1	0.18	Minimum Via k space.
VIAk.SP.2	0.20	Space to three adjacent Via k (< 0.25 um apart)
VIAk.E.1	0.015	Minimum Metal k to of Via k enclosure.
VIAk.E.2	0.04	Minimum Metal k to Via k enclosure on at least two opposite sides of Via k.

## VIA RULES (continued)

macro



Macro Table

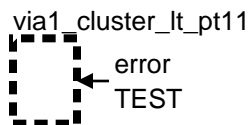
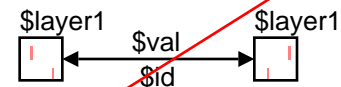
\$layer1	\$id1	\$value1	\$id2	\$value2
Via1	VIA1.W.1	0.07x0.07	VIA1.SP.1	0.07
Via2	VIA2.W.1	0.07x0.07	VIA2.SP.1	0.07
Via3	VIA3.W.1	0.07x0.07	VIA3.SP.1	0.07
Via4	VIA4.W.1	0.07x0.07	VIA4.SP.1	0.07
Via5	VIA5.W.1	0.07x0.07	VIA5.SP.1	0.07
Via6	VIA6.W.1	0.07x0.07	VIA6.SP.1	0.07
Via7	VIA7.W.1	0.07x0.07	VIA7.SP.1	0.07
Via8	VIA8.W.1	0.07x0.07	VIA8.SP.1	0.07
Via9	VIA9.W.1	0.18x0.18	VIA9.SP.1	0.18
Via10	VIA10.W.1	0.18x0.18	VIA10.SP.1	0.18

switch FALSE

macro

Macro Table

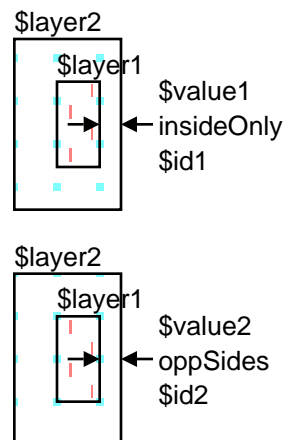
\$layer1	\$name	\$val	\$val2	\$id
via1_cluster_lt_pt11	Via1	.10	0.11	VIA1.SP.2
via2_cluster_lt_pt11	Via2	.10	0.11	VIA2.SP.2
via3_cluster_lt_pt11	Via3	.10	0.11	VIA3.SP.2
via4_cluster_lt_pt11	Via4	.10	0.11	VIA4.SP.2
via5_cluster_lt_pt11	Via5	.10	0.11	VIA5.SP.2
via6_cluster_lt_pt11	Via6	.10	0.11	VIA6.SP.2
via7_cluster_lt_pt11	Via7	.10	0.11	VIA7.SP.2
via8_cluster_lt_pt11	Via8	.10	0.11	VIA8.SP.2
via9_cluster_lt_pt25	Via9	.20	0.25	VIA9.SP.2
via10_cluster_lt_pt25	Via10	.20	0.25	VIA10.SP.2



macro

Macro Table

\$name1	\$layer1	\$layer2	\$id1	\$value1	\$id2	\$value2
Metal1	Via1	metal1_conn	VIA1.E.1	0.005	VIA1.E.2	0.03
Metal2	Via2	metal2_conn	VIA2.E.1	0.005	VIA2.E.2	0.03
Metal3	Via3	metal3_conn	VIA3.E.1	0.005	VIA3.E.2	0.03
Metal4	Via4	metal4_conn	VIA4.E.1	0.005	VIA4.E.2	0.03
Metal5	Via5	metal5_conn	VIA5.E.1	0.005	VIA5.E.2	0.03
Metal6	Via6	metal6_conn	VIA6.E.1	0.005	VIA6.E.2	0.03
Metal7	Via7	metal7_conn	VIA7.E.1	0.005	VIA7.E.2	0.03
Metal8	Via8	metal8_conn	VIA8.E.1	0.005	VIA8.E.2	0.03
Metal9	Via9	metal9_conn	VIA9.E.1	0.015	VIA9.E.2	0.04
Metal10	Via10	Metal10	VIA10.E.1	0.015	VIA10.E.2	0.04

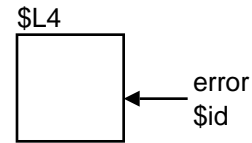


## VIA RULES (continued)

macro

Macro Table

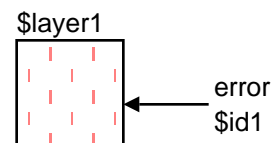
\$L1	\$L2	\$L3	\$L4	\$id
Via1	Metal1	Metal2	rule_VIA1_E_3	VIA1.E.3
Via2	Metal2	Metal3	rule_VIA2_E_3	VIA2.E.3
Via3	Metal3	Metal4	rule_VIA3_E_3	VIA3.E.3
Via4	Metal4	Metal5	rule_VIA4_E_3	VIA4.E.3
Via5	Metal5	Metal6	rule_VIA5_E_3	VIA5.E.3
Via6	Metal6	Metal7	rule_VIA6_E_3	VIA6.E.3
Via7	Metal7	Metal8	rule_VIA7_E_3	VIA7.E.3
Via8	Metal8	Metal9	rule_VIA8_E_3	VIA8.E.3



macro

Macro Table

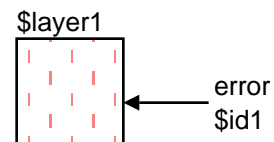
\$name1	\$name2	\$name3	\$layer1	\$id1
Via1	Metal1	Metal2	rule_VIA1_X_1	VIA1.X.1
Via2	Metal2	Metal3	rule_VIA2_X_1	VIA2.X.1
Via3	Metal3	Metal4	rule_VIA3_X_1	VIA3.X.1
Via4	Metal4	Metal5	rule_VIA4_X_1	VIA4.X.1
Via5	Metal5	Metal6	rule_VIA5_X_1	VIA5.X.1
Via6	Metal6	Metal7	rule_VIA6_X_1	VIA6.X.1
Via7	Metal7	Metal8	rule_VIA7_X_1	VIA7.X.1
Via8	Metal8	Metal9	rule_VIA8_X_1	VIA8.X.1



macro

Macro Table

\$name1	\$name2	\$name3	\$layer1	\$id1
Via1	Metal1	Metal2	rule_VIA1_X_2	VIA1.X.2
Via2	Metal2	Metal3	rule_VIA2_X_2	VIA2.X.2
Via3	Metal3	Metal4	rule_VIA3_X_2	VIA3.X.2
Via4	Metal4	Metal5	rule_VIA4_X_2	VIA4.X.2
Via5	Metal5	Metal6	rule_VIA5_X_2	VIA5.X.2
Via6	Metal6	Metal7	rule_VIA6_X_2	VIA6.X.2
Via7	Metal7	Metal8	rule_VIA7_X_2	VIA7.X.2
Via8	Metal8	Metal9	rule_VIA8_X_2	VIA8.X.2

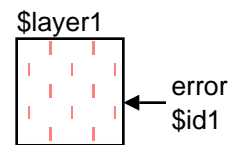


**VIA RULES (continued)**

macro

Macro Table

\$name1	\$name2	\$layer1	\$id1
Metal1	Metal6	rule_VIAk_X_3_X_4a	VIAk.X.3_VIAk.X.4
Metal2	Metal7	rule_VIAk_X_3_X_4b	VIAk.X.3_VIAk.X.4
Metal3	Metal8	rule_VIAk_X_3_X_4c	VIAk.X.3_VIAk.X.4
Metal4	Metal9	rule_VIAk_X_3_X_4d	VIAk.X.3_VIAk.X.4

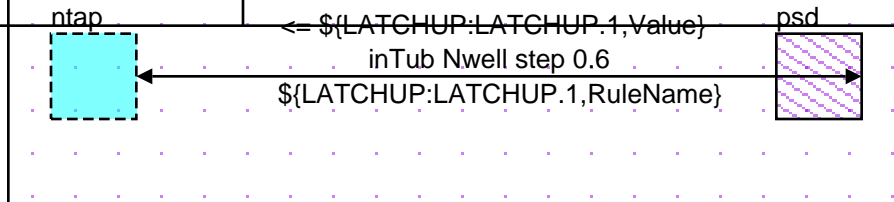




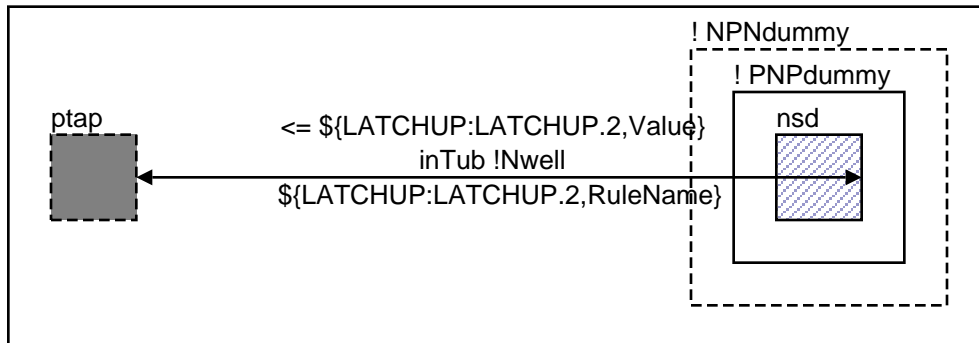
## LATCH-UP RULES

Data Table: LATCHUP\_DRC

RuleName	Description	Value
LATCHUP.1	\${LATCHUP:LATCHUP.1,Description}	\${LATCHUP:LATCHUP.1,Value}
LATCHUP.2	\${LATCHUP:LATCHUP.2,Description}	\${LATCHUP:LATCHUP.2,Value}
LATCHUP.3	\${LATCHUP:LATCHUP.3,Description}	\${LATCHUP:LATCHUP.3,Value}
Nwell LATCHUP.4	\${LATCHUP:LATCHUP.4,Description}	\${LATCHUP:LATCHUP.4,Value}



! Nwell



nmos\_io\_esd

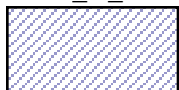


pmos\_io\_esd



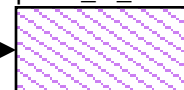
$\text{\${LATCHUP:LATCHUP.3,Value}}$   
 $\text{\${LATCHUP:LATCHUP.3,RuleName}}$

nmos\_io\_esd



$\text{\${LATCHUP:LATCHUP.4,Value}}$   
 notBlockedBy ntap  
 notBlockedBy ptap  
 $\text{\${LATCHUP:LATCHUP.4,RuleName}}$

pmos\_io\_esd



## ANTENNA RULES

Comment Table ANTENNA RULES

Rule Name	Value (um)	Description
ANT.1	275.0	Maximum ratio of Poly area to the gate area the Poly is connected to.
ANT.2	550.0	Maximum ratio of Poly sidewall area to the gate area the Poly is connected to.
ANT.3	15.0	Maximum ratio of Poly Contact area to the gate area the Contact is connected with.
ANT.4.Mx	475.0	Maximum ratio of Metal x (x = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11) area to the gate area the Metal x is connected to (without diode protection).
ANT.5.Vx	25.0	Maximum ratio of Via x (x = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10) area to the gate area the Via x is connected with (without diode protection).
ANT.6.M1_x (x = 3, 4, 5, 6, 7, 8, 9)	1200.0	Maximum ratio of cumulative Metal areas to the gate area the Metals are connected to (without diode protection).
DIODE PROTECTION		
ANT.7.M1_x (x = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11)		<p>When a protection diode with an area greater than or equal to <math>0.1\mu\text{m}^2</math> is connected to the gate area, the maximum ratio of cumulative Metal areas (Metal 1 - Metal 8) is calculated as follows:</p> <ul style="list-style-type: none"> <li>Ratio = (diode area X 500) + 45000</li> </ul> <p>For Metal 11 only, the ratio is calculated as follows:</p> <ul style="list-style-type: none"> <li>Ratio = (diode area X 7500) + 55000</li> </ul>
ANT.8.V1_x (x = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10)		<p>When a protection diode with an area greater than or equal to <math>0.1\mu\text{m}^2</math> is connected to the gate area, the maximum ratio of cumulative Via areas (Via 1 - Via 10) is calculated as follows:</p> <ul style="list-style-type: none"> <li>Ratio = (diode area X 250) + 1000</li> </ul>

Note 1: Source/drain diffusion areas of MOS devices are counted as part of the diode area.

Note 2: It is recommended to use one large diode with multiple Contacts rather than several smaller diodes.

Note 3: When the sum of the areas of all diodes on a net equals or exceeds  $0.1\mu\text{m}^2$ , then those diodes can be treated as a protection diode for ANT.7 and ANT.8.

## ANTENNA RULES (continued)

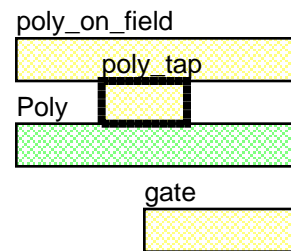
switch CHECK\_POLY\_ANT\_1

Antenna

$\text{ratio}(\text{poly\_on\_field.area} / \text{gate.area}) \leq 275.0$

id: ANT.1

message: Field Poly area to gate area ratio must be  $\leq 275.0$



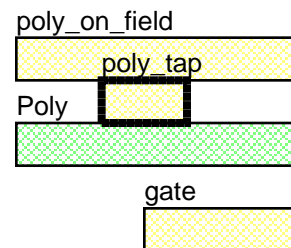
switch CHECK\_POLY\_ANT\_2

Antenna

$\text{ratio}(\text{poly\_on\_field.perimeter} / \text{gate.area}) \leq 550.0$

id: ANT.2

message: Field Poly perimeter to gate area ratio must be  $\leq 550.0$



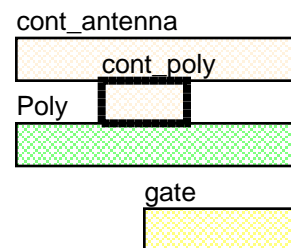
switch CHECK\_CONT\_ANT\_3

Antenna

$\text{ratio}(\text{cont\_antenna.area} / \text{gate.area}) \leq 15.0$

id: ANT.3

message: Poly Contact area to gate area ratio must be  $\leq 15.0$



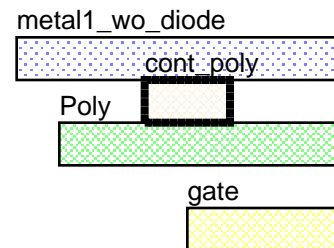
switch CHECK\_METAL1\_ANT\_4

Antenna

$\text{ratio}(\text{metal1\_wo\_diode.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M1

message: Metal1 area to gate area ratio must be  $\leq 475.0$



## ANTENNA RULES (continued)

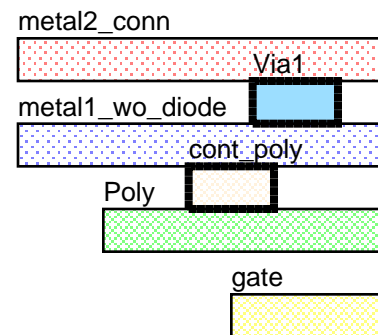
switch CHECK\_METAL2\_ANT\_4

Antenna

$\text{ratio}(\text{metal2\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M2

message: Metal2 area to gate area ratio must be  $\leq 475.0$



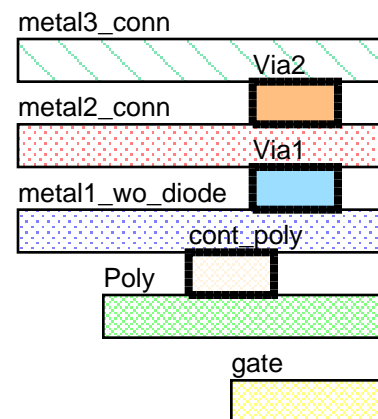
switch CHECK\_METAL3\_ANT\_4

Antenna

$\text{ratio}(\text{metal3\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M3

message: Metal3 area to gate area ratio must be  $\leq 475.0$



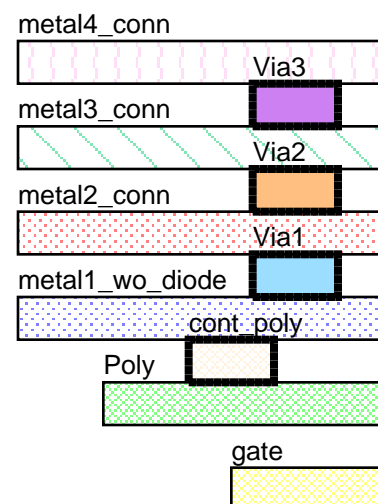
switch CHECK\_METAL4\_ANT\_4

Antenna

$\text{ratio}(\text{metal4\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M4

message: Metal4 area to gate area ratio must be  $\leq 475.0$



## ANTENNA RULES (continued)

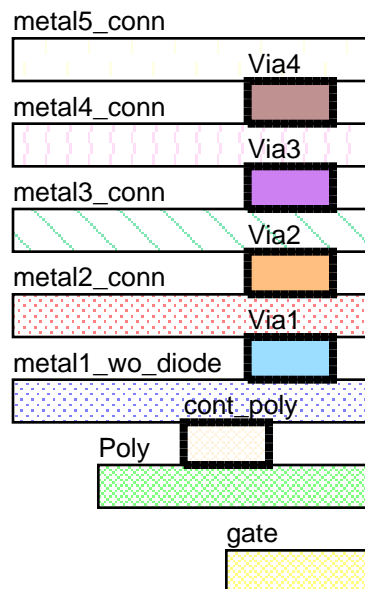
switch CHECK\_METAL5\_ANT\_4

Antenna

$\text{ratio}(\text{metal5\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M5

message: Metal5 area to gate area ratio must be  $\leq 475.0$



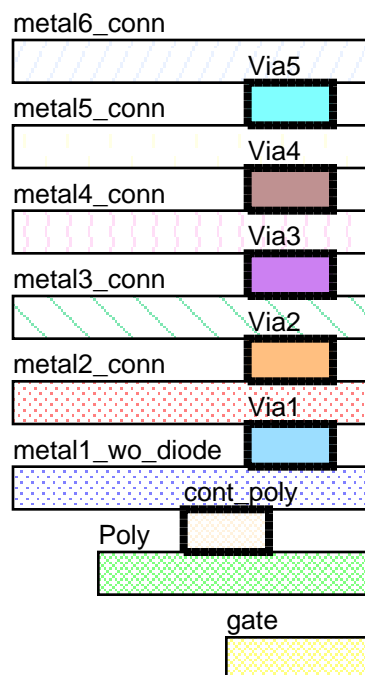
switch CHECK\_METAL6\_ANT\_4

Antenna

$\text{ratio}(\text{metal6\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M6

message: Metal6 area to gate area ratio must be  $\leq 475.0$



## ANTENNA RULES (continued)

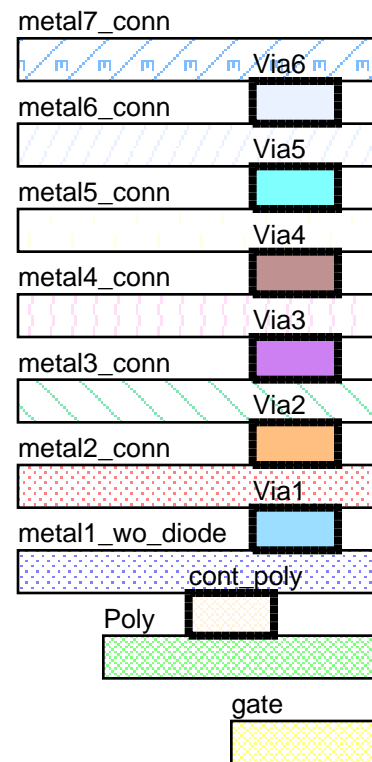
switch CHECK\_METAL7\_ANT\_4

Antenna

$\text{ratio} (\text{metal7\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M7

message: Metal7 area to gate area ratio must be  $\leq 475.0$



## ANTENNA RULES (continued)

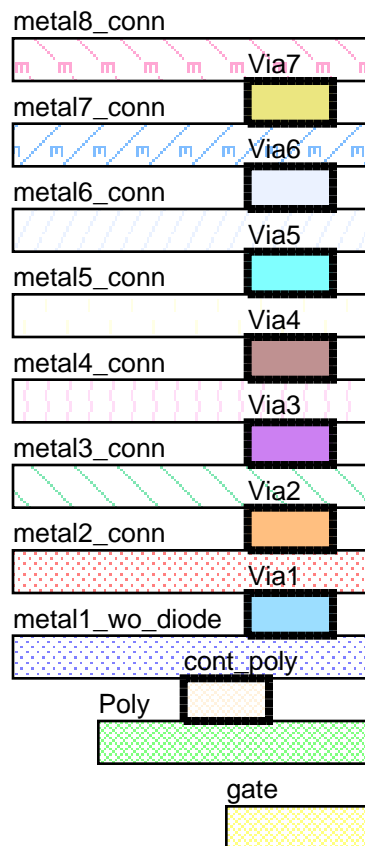
switch CHECK\_METAL8\_ANT\_4

Antenna

$\text{ratio}(\text{metal8\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M8

message: Metal8 area to gate area ratio must be  $\leq 475.0$



## ANTENNA RULES (continued)

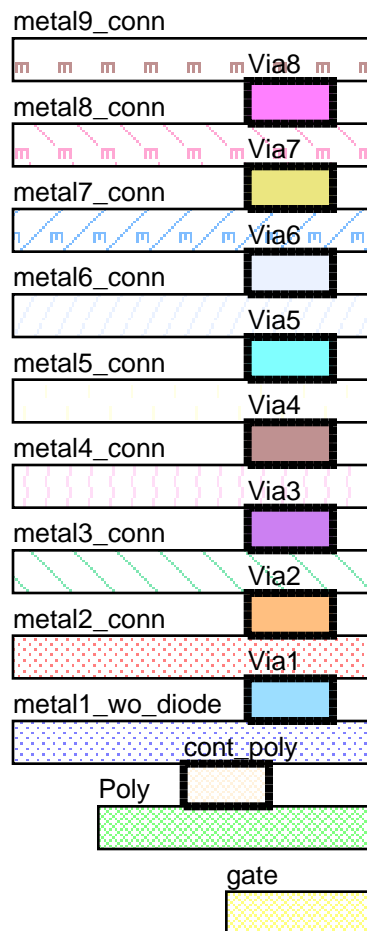
switch CHECK\_METAL9\_ANT\_4

Antenna

$\text{ratio}(\text{metal9\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M9

message: Metal9 area to gate area ratio must be  $\leq 475.0$





## ANTENNA RULES (continued)

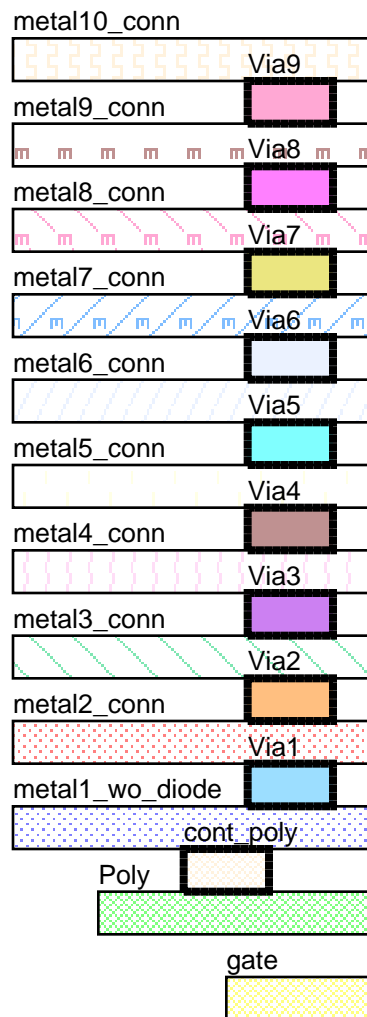
switch CHECK\_METAL10\_ANT\_4

Antenna

$\text{ratio} (\text{metal10\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M10

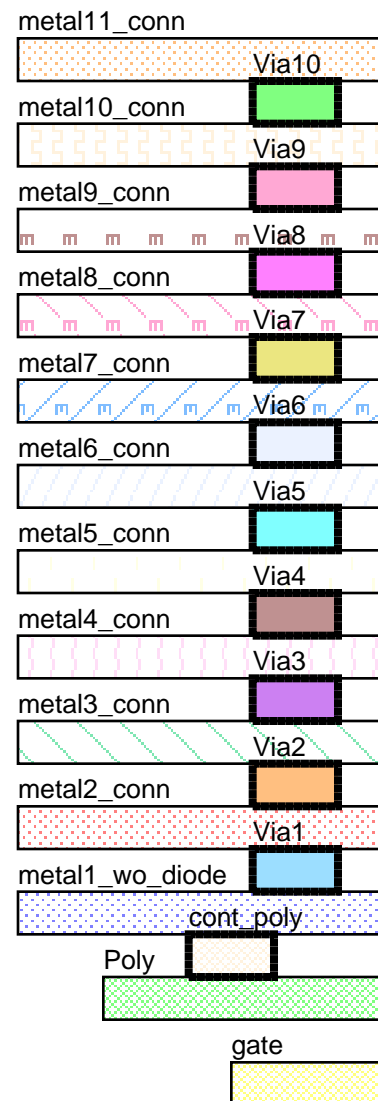
message: Metal10 area to gate area ratio must be  $\leq 475.0$



## ANTENNA RULES (continued)

switch CHECK\_METAL11\_ANT\_4

Antenna



$\text{ratio}(\text{metal11\_conn.area} / \text{gate.area}) \leq 475.0$

id: ANT.4.M11

message: Metal11 area to gate area ratio must be  $\leq 475.0$

## ANTENNA RULES (continued)

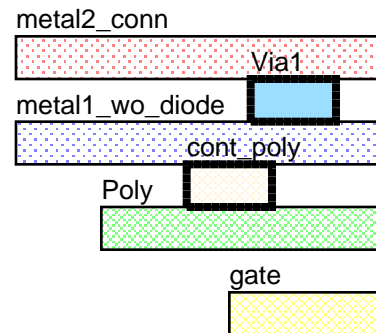
switch CHECK\_VIA1\_ANT\_5

Antenna

$\text{ratio (Via1.area / gate.area)} \leq 25.0$

id: ANT.5.V1

message: Via1 area to gate area ratio must be  $\leq 25.0$



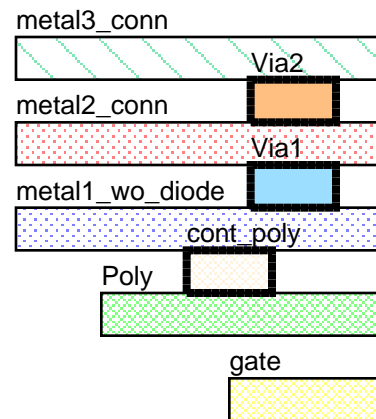
switch CHECK\_VIA2\_ANT\_5

Antenna

$\text{ratio (Via2.area / gate.area)} \leq 25.0$

id: ANT.5.V2

message: Via2 area to gate area ratio must be  $\leq 25.0$



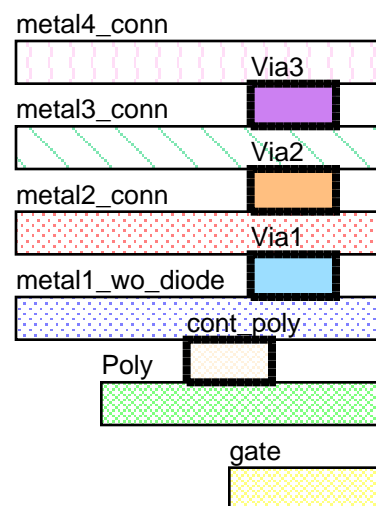
switch CHECK\_VIA3\_ANT\_5

Antenna

$\text{ratio (Via3.area / gate.area)} \leq 25.0$

id: ANT.5.V3

message: Via3 area to gate area ratio must be  $\leq 25.0$



## ANTENNA RULES (continued)

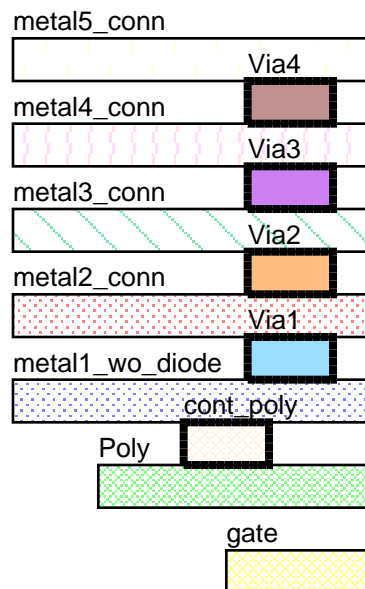
switch CHECK\_VIA4\_ANT\_5

Antenna

ratio (Via4.area / gate.area) <= 25.0

id: ANT.5.V4

message: Via4 area to gate area ratio must be <= 25.0



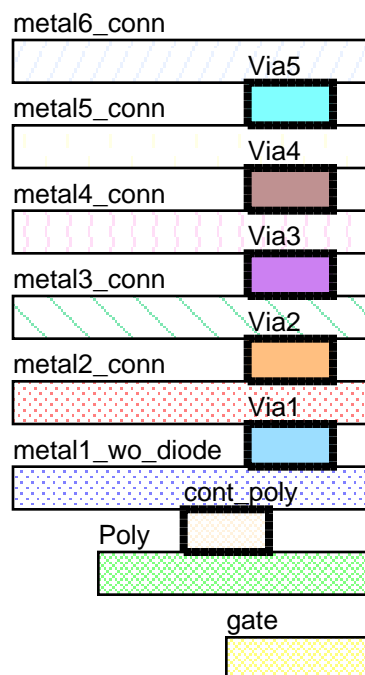
switch CHECK\_VIA5\_ANT\_5

Antenna

ratio (Via5.area / gate.area) <= 25.0

id: ANT.5.V5

message: Via5 area to gate area ratio must be <= 25.0



## ANTENNA RULES (continued)

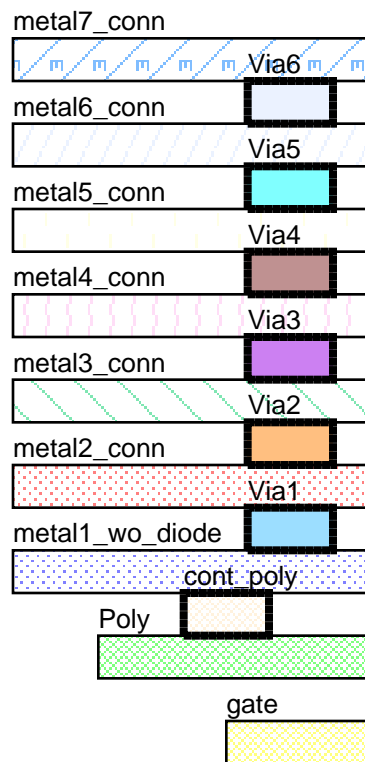
switch CHECK\_VIA6\_ANT\_5

Antenna

ratio (Via6.area / gate.area) <= 25.0

id: ANT.5.V6

message: Via6 area to gate area ratio must be <= 25.0



## ANTENNA RULES (continued)

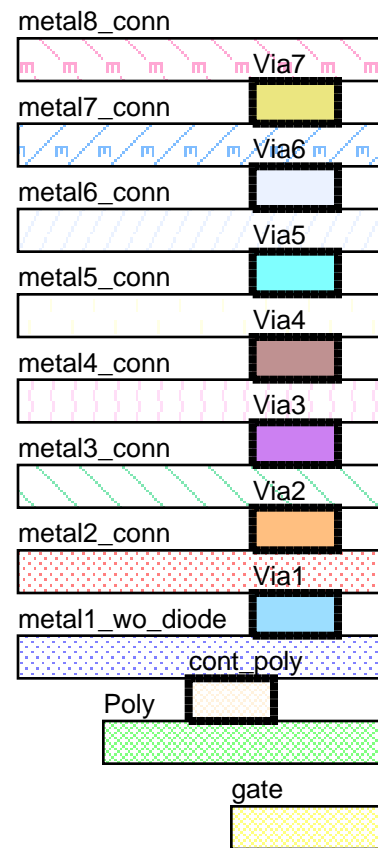
switch CHECK\_VIA7\_ANT\_5

Antenna

ratio (Via7.area / gate.area) <= 25.0

id: ANT.5.V7

message: Via7 area to gate area ratio must be <= 25.0



## ANTENNA RULES (continued)

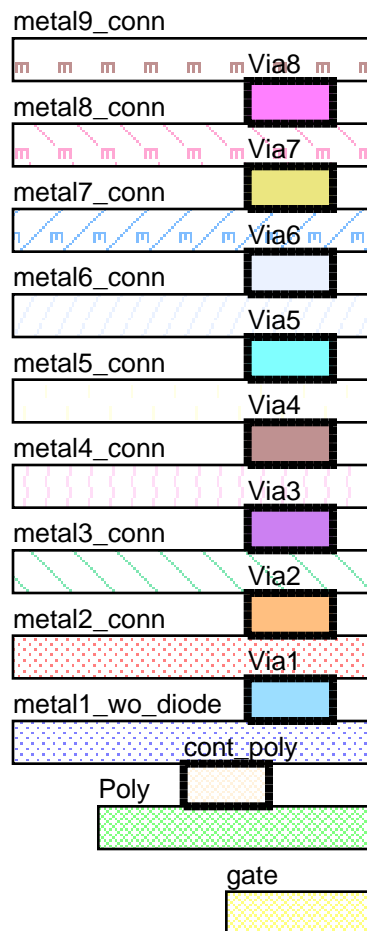
switch CHECK\_VIA8\_ANT\_5

Antenna

ratio (Via8.area / gate.area) <= 25.0

id: ANT.5.V8

message: Via8 area to gate area ratio must be <= 25.0



## ANTENNA RULES (continued)

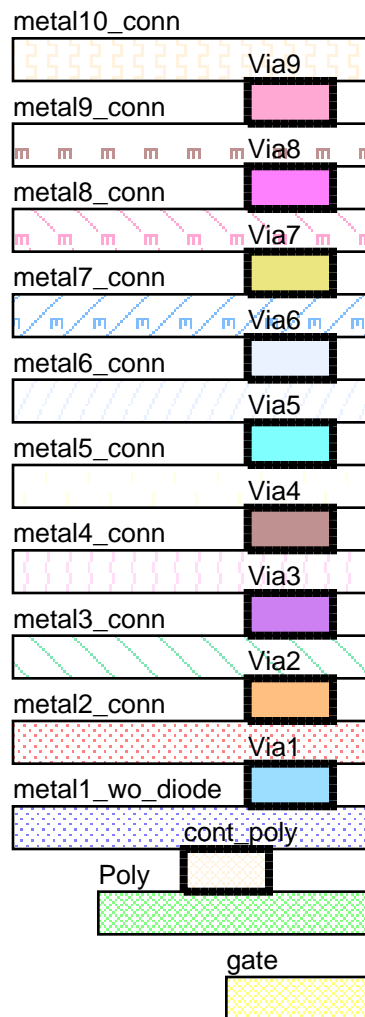
switch CHECK\_VIA9\_ANT\_5

Antenna

ratio (Via9.area / gate.area) <= 25.0

id: ANT.5.V9

message: Via9 area to gate area ratio must be <= 25.0





## ANTENNA RULES (continued)

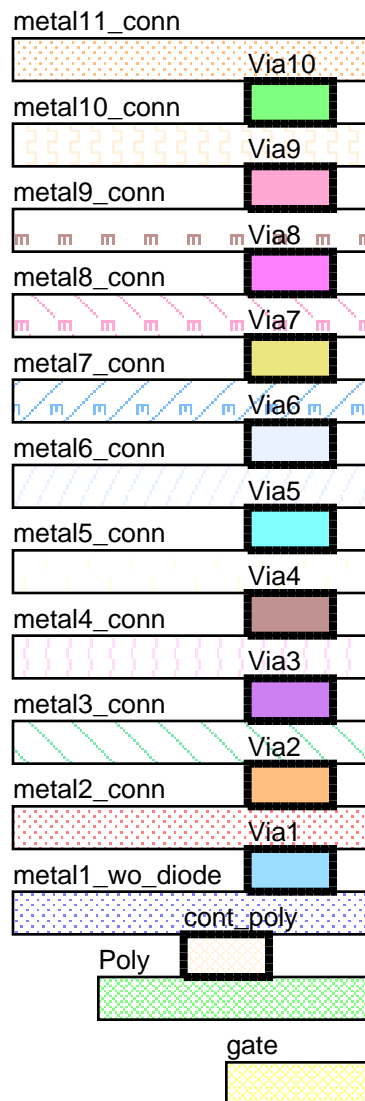
switch CHECK\_VIA10\_ANT\_5

Antenna

ratio (Via10.area / gate.area) <= 25.0

id: ANT.5.V10

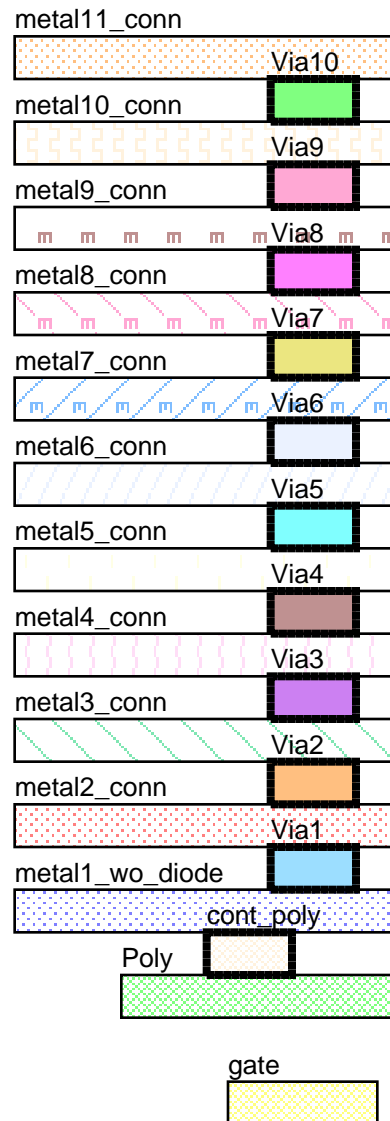
message: Via10 area to gate area ratio must be <= 25.0



## ANTENNA RULES (continued)

switch CHECK\_METAL11\_ANT\_6

Antenna



$$\text{ratio} ((\text{metal11\_conn.area} + \text{metal10\_conn.area} + \text{metal9\_conn.area} + \text{metal8\_conn.area} + \text{metal7\_conn.area} + \text{metal6\_conn.area} + \text{metal5\_conn.area} + \text{metal4\_conn.area} + \text{metal3\_conn.area} + \text{metal2\_conn.area} + \text{metal1\_wo\_diode.area}) / \text{gate.area}) \leq 1200.0$$

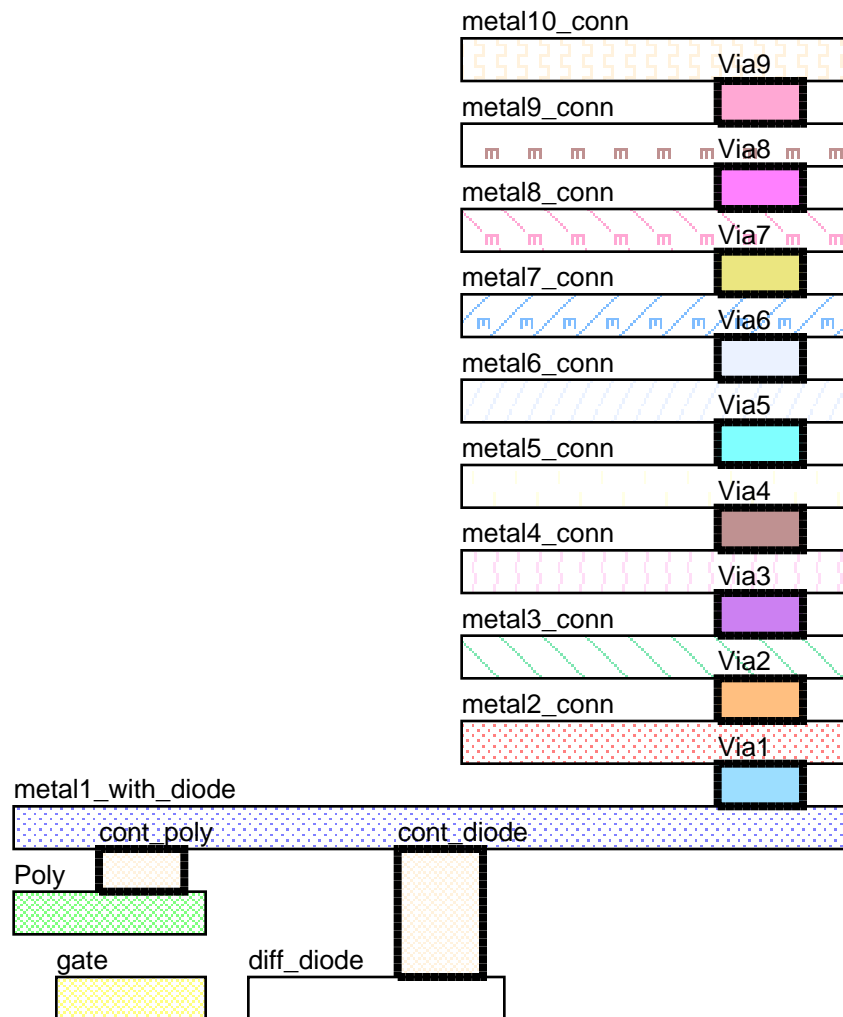
id: ANT.6.M1\_11

message: Cumulative Metal1 through Metal11 area to gate area ratio must be  $\leq 1200.0$

## ANTENNA RULES (continued)

switch CHECK\_METAL10\_ANT\_7

Antenna



ratio (((metal1\_with\_diode.area + metal2\_conn.area + metal3\_conn.area +  
metal4\_conn.area + metal5\_conn.area + metal6\_conn.area +  
metal7\_conn.area + metal8\_conn.area + metal9\_conn.area +  
metal10\_conn.area) / gate.area) - ((diff\_diode.area \* 500.0) + 45000.0)) <= 0.0

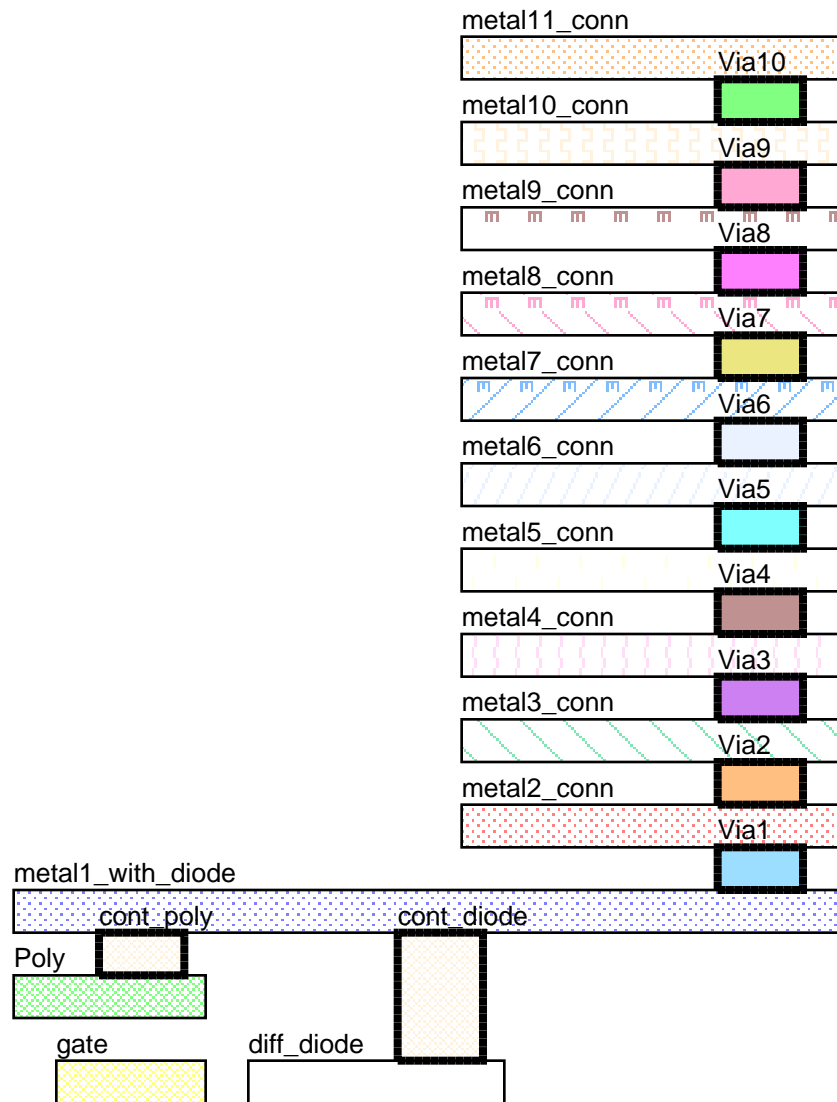
id: ANT.7.M1\_10

message: Cumulative Metal1 through Metal10 area to gate area ratio must be  
<= 45000 + (diode area \* 500)

## ANTENNA RULES (continued)

switch CHECK\_METAL11\_ANT\_7

Antenna



id: ANT.7.M1\_11

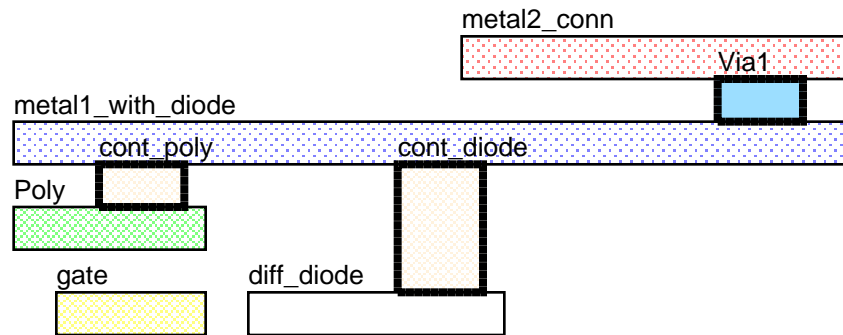
ratio ((metal1\_with\_diode.area + metal2\_conn.area + metal3\_conn.area +  
metal4\_conn.area + metal5\_conn.area + metal6\_conn.area +  
metal7\_conn.area + metal8\_conn.area + metal9\_conn.area +  
metal10\_conn.area + metal11\_conn.area / gate.area) -  
((diff\_diode.area \* 7500.0) + 55000.0)) <= 0.0

message: Cumulative Metal1 through Metal11 area to gate area ratio must be  
<= 55000 + (diode area \* 7500)

## ANTENNA RULES (continued)

switch CHECK\_VIA1\_ANT\_8

Antenna



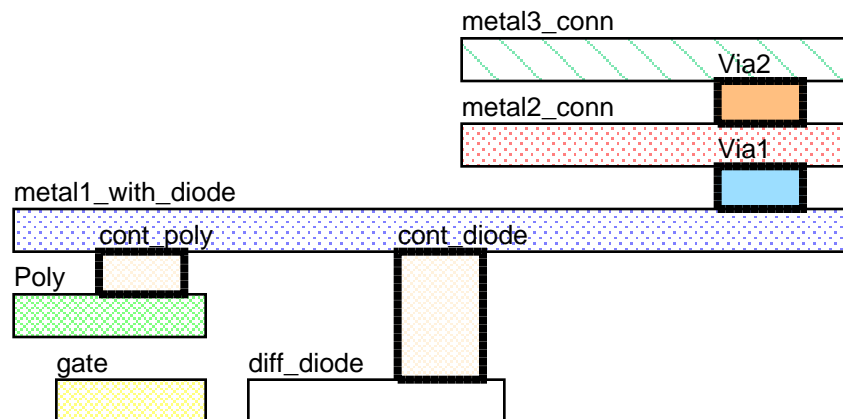
$$\text{ratio} ((\text{Via1.area} / \text{gate.area}) - ((\text{diff\_diode.area} * 250.0) + 1000.0)) \leq 0.0$$

id: ANT.8.V1\_1

message: Via1 area to gate area ratio must be  $\leq 1000 + (\text{diode area} * 250)$

switch CHECK\_VIA2\_ANT\_8

Antenna



$$\text{ratio} (((\text{Via1.area} + \text{Via2.area}) / \text{gate.area}) - ((\text{diff\_diode.area} * 250.0) + 1000.0)) \leq 0.0$$

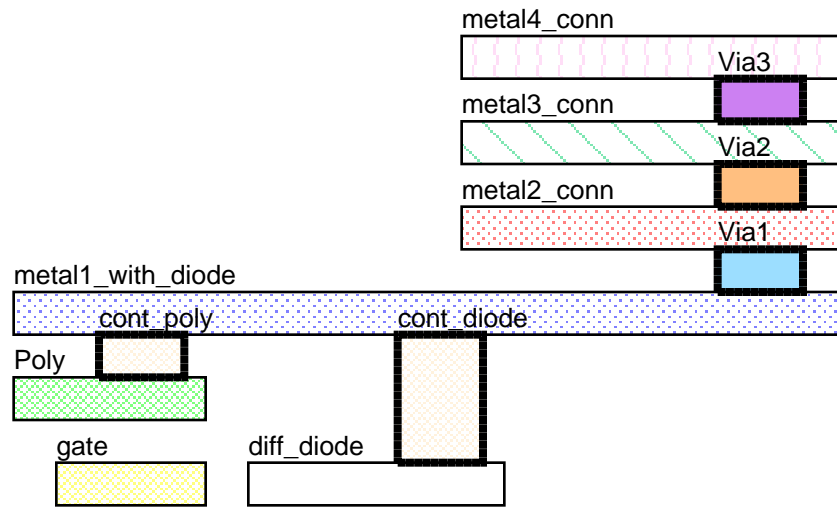
id: ANT.8.V1\_2

message: Cumulative Via1 through Via2 area to gate area  
ratio must be  $\leq 1000 + (\text{diode area} * 250)$

## ANTENNA RULES (continued)

switch CHECK\_VIA3\_ANT\_8

Antenna



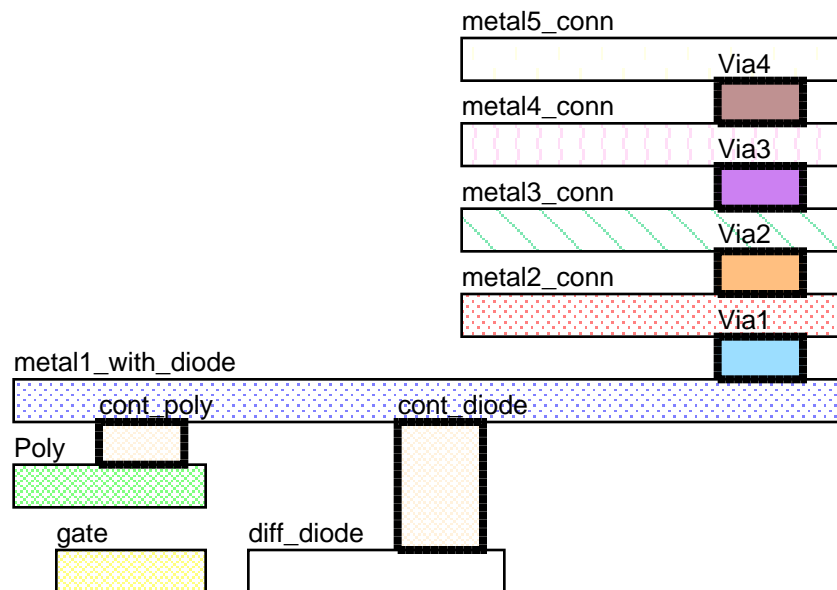
ratio (((Via1.area + Via2.area + Via3.area) / gate.area) -  
((diff\_diode.area \* 250.0) + 1000.0)) <= 0.0

id: ANT.8.V1\_3

message: Cumulative Via1 through Via3 area to gate area  
ratio must be <= 1000 + (diode area \* 250)

switch CHECK\_VIA4\_ANT\_8

Antenna



ratio (((Via1.area + Via2.area + Via3.area + Via4.area) /  
gate.area) - ((diff\_diode.area \* 250.0) + 1000.0)) <= 0.0

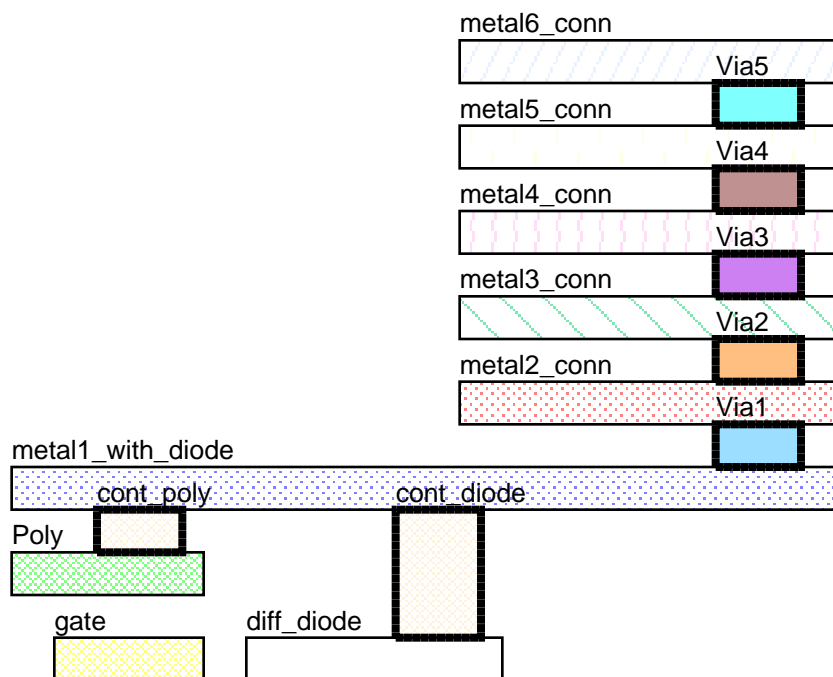
id: ANT.8.V1\_4

message: Cumulative Via1 through Via4 area to gate area  
ratio must be <= 1000 + (diode area \* 250)

## ANTENNA RULES (continued)

switch CHECK\_VIA5\_ANT\_8

Antenna



$$\text{ratio}(((\text{Via1.area} + \text{Via2.area} + \text{Via3.area} + \text{Via4.area} + \text{Via5.area}) / \text{gate.area}) - ((\text{diff\_diode.area} * 250.0) + 1000.0)) \leq 0.0$$

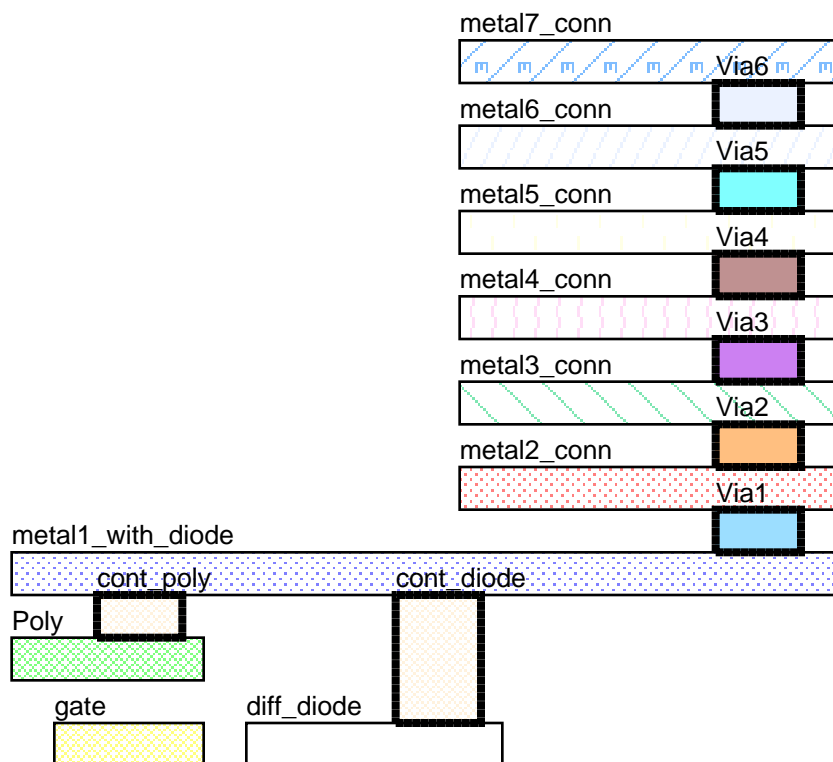
id: ANT.8.V1\_5

message: Cumulative Via1 through Via5 area to gate area  
ratio must be  $\leq 1000 + (\text{diode area} * 250)$

## ANTENNA RULES (continued)

switch CHECK\_VIA6\_ANT\_8

Antenna



ratio (((Via1.area + Via2.area + Via3.area + Via4.area + Via5.area + Via6.area) / gate.area) - ((diff\_diode.area \* 250.0) + 1000.0)) <= 0.0

id: ANT.8.V1\_6

message: Cumulative Via1 through Via6 area to gate area

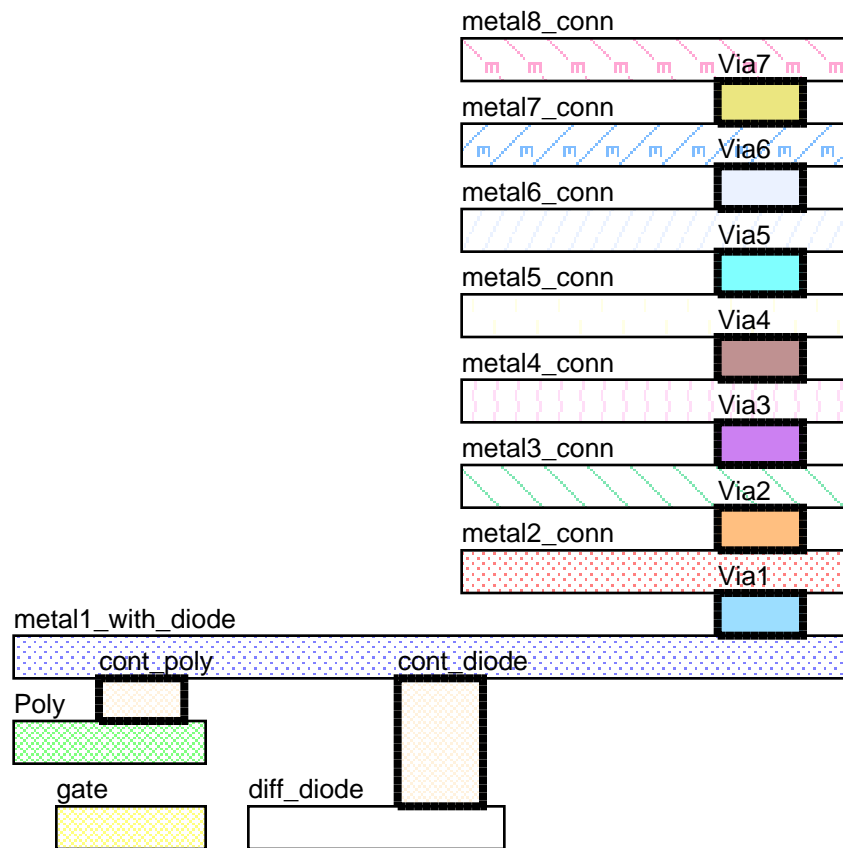
ratio must be <= 1000 + (diode area \* 250)



## ANTENNA RULES (continued)

switch CHECK\_VIA7\_ANT\_8

Antenna



ratio (((Via1.area + Via2.area + Via3.area + Via4.area +  
Via5.area + Via6.area + Via7.area) / gate.area) - ((diff\_diode.area \* 250.0) + 1000.0))  
<= 0.0

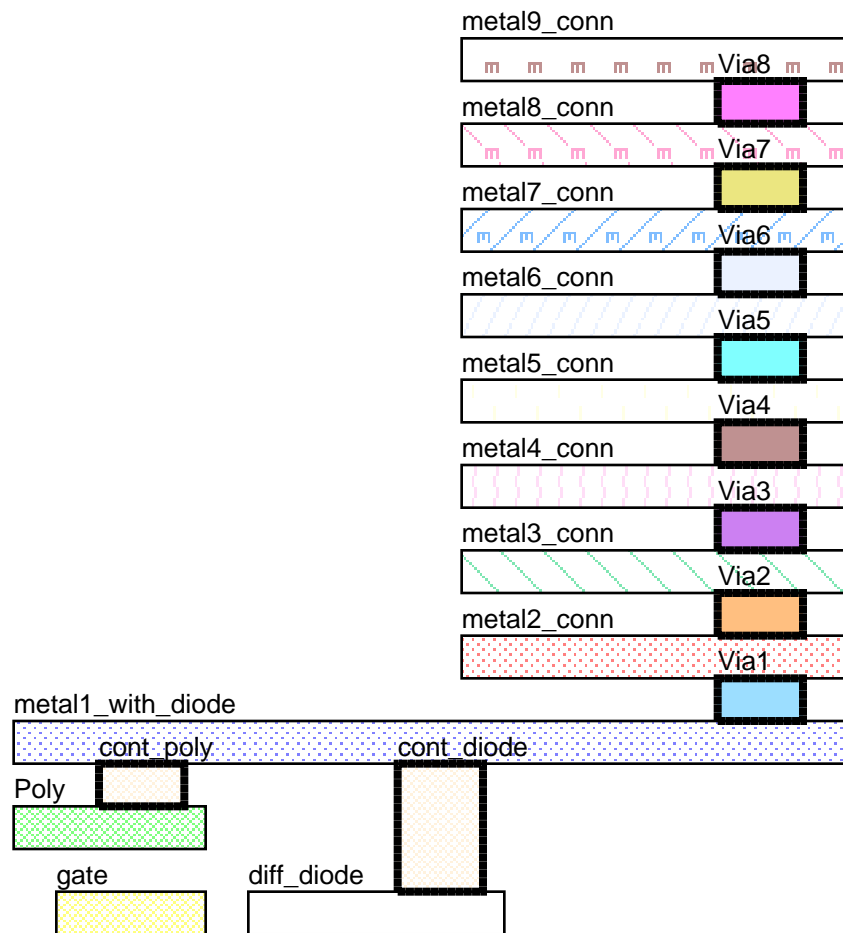
id: ANT.8.V1\_7

message: Cumulative Via1 through Via7 area to gate area  
ratio must be <= 1000 + (diode area \* 250)

## ANTENNA RULES (continued)

switch CHECK\_VIA8\_ANT\_8

Antenna



ratio (((Via1.area + Via2.area + Via3.area + Via4.area + Via5.area +  
Via6.area + Via7.area + Via8.area) / gate.area) - ((diff\_diode.area  
\* 250.0) + 1000.0)) <= 0.0

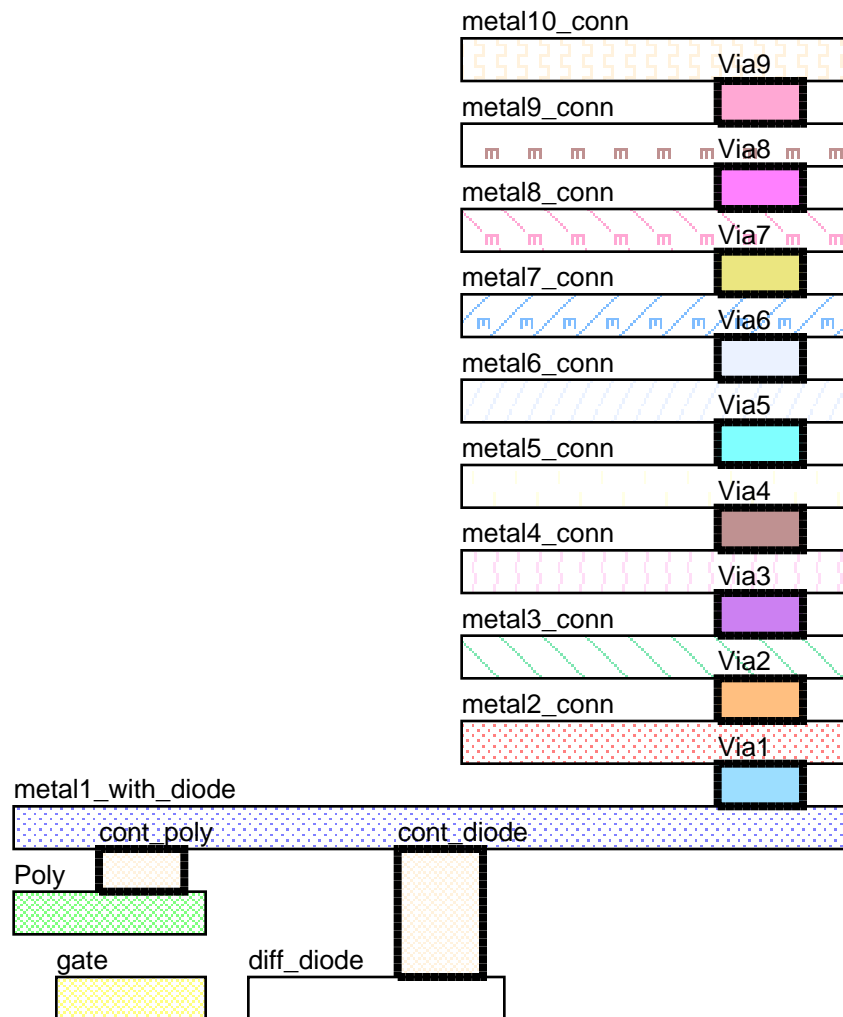
id: ANT.8.V1\_8

message: Cumulative Via1 through Via8 area to gate area  
ratio must be <= 1000 + (diode area \* 250)

## ANTENNA RULES (continued)

switch CHECK\_VIA9\_ANT\_8

Antenna



ratio (((Via1.area + Via2.area + Via3.area + Via4.area + Via5.area +  
Via6.area + Via7.area + Via8.area + Via9.area) / gate.area) - ((diff\_diode.area  
\* 250.0) + 1000.0)) <= 0.0

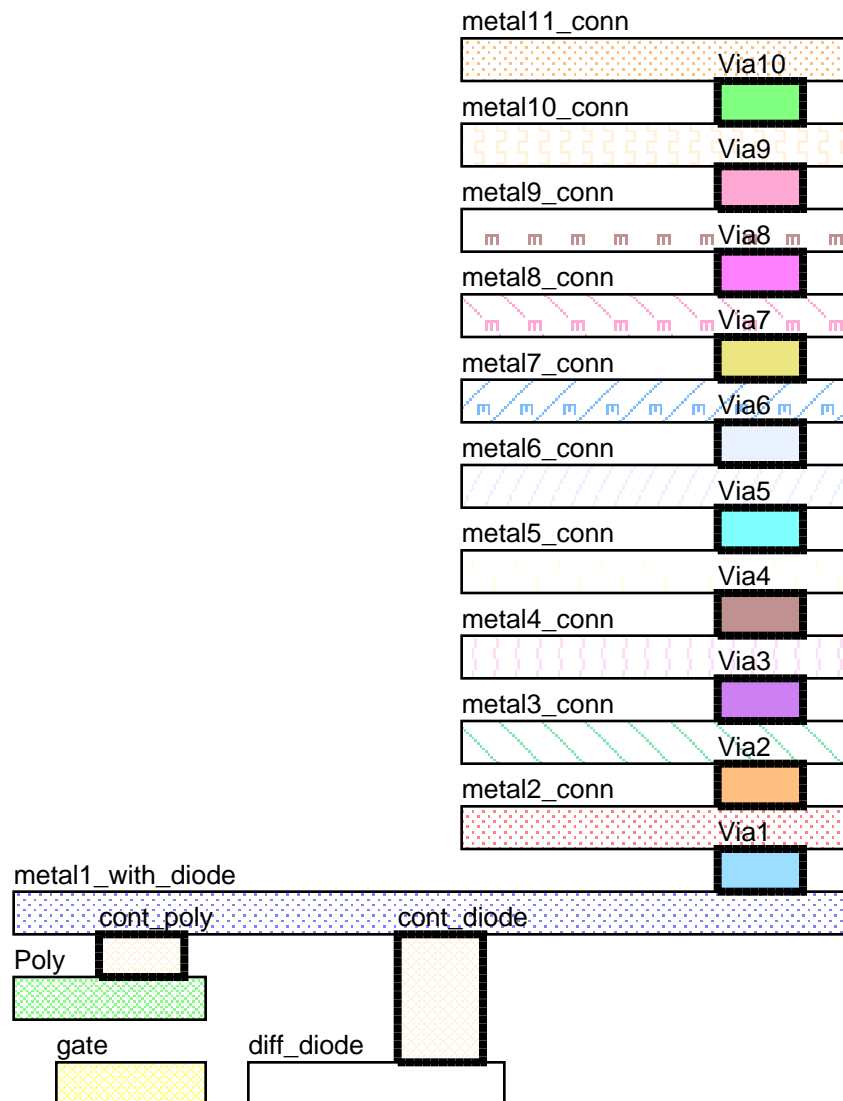
id: ANT.8.V1\_9

message: Cumulative Via1 through Via9 area to gate area  
ratio must be <= 1000 + (diode area \* 250)

## ANTENNA RULES (continued)

switch CHECK\_VIA10\_ANT\_8

Antenna



ratio (((Via1.area + Via2.area + Via3.area + Via4.area + Via5.area +  
Via6.area + Via7.area + Via8.area + Via9.area + Via10.area)  
/ gate.area) - ((diff\_diode.area \* 250.0) + 1000.0)) <= 0.0

id: ANT.8.V1\_10

message: Cumulative Via1 through Via10 area to gate area  
ratio must be <= 1000 + (diode area \* 250)

# CMOS I/O Design Rules

## ESD Design Rules

The "ESDdummy" marker layer must be used to mark I/O ESD circuitry. If the "ESDdummy" layer is not used, the correct DRC checks of I/O ESD circuitry will not take place.

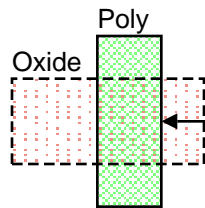
NMOS and PMOS devices used for ESD protection follow a strict finger structure using specific finger dimensions and layout.

Comment Table ESD Design Rules

Rule Name	Value (um)	Description
ESD.1	10 - 30	Width of each finger of NMOS and PMOS in I/O buffers and in Vdd to Vss ESD protection.
ESD.2	210	Minimum NMOS combined finger width for I/O buffers and for Vdd to Vss ESD protection.
ESD.3	210	Minimum PMOS combined finger width for I/O buffers.
ESD.4		Outer Oxide area of NMOS and PMOS in I/O buffers and in Vdd to Vss ESD protection must be Source or connected to Bulk to prevent parasitic bipolars and unwanted discharge paths during ESD zapping.
ESD.5		NMOS ESD protection devices must be surrounded by a P+ Guard Ring.
ESD.6		PMOS ESD protection devices must be surrounded by an N+ Guard Ring.
ESD.7		NMOS and PMOS in ESD protection can NOT have butted taps.
ESD.8		NMOS and PMOS in an I/O buffer must have non-salicided Drains. The Contacts still must be salicided.
ESD.9		A P+ Oxide strap should be placed between N+ Oxides of different I/O and ESD devices when both connect to different pads.
ESD.10		An N+ Oxide strap should be placed between P+ Oxides of different I/O and ESD devices when both connect to different pads.
ESD.11	0.05	Minimum SiProt to Poly gate overlap in NMOS and PMOS drains.
ESD.12	0.9	Minimum enclosure of SiProt edge to Poly gate edge in NMOS and PMOS I/O drains.
ESD.13	0.9	Minimum SiProt to Oxide overlap in NMOS and PMOS I/O drains.
ESD.14	0.2	Exact gate length of NMOS and PMOS in I/O buffers and in Vdd to Vss ESD protection.
ESD.15	0.12	Minimum Poly gate to Contact spacing in NMOS and PMOS in I/O buffers and in Vdd to Vss ESD protection.

## ESD Design Rules (continued)

ESDdummy



segment  $\geq$   $\{ESD:ESD.1.MIN, Value\}$   $\leq$   $\{ESD:ESD.1.MAX, Value\}$   
ESD.1

ESD.2 - Checked during LVS.

ESD.3 - Checked during LVS.

rule ESD 4 nmos



error  
ESD.4

rule ESD 4 pmos



error  
ESD.4

rule ESD 5



error  
ESD.5

rule ESD 6



error  
ESD.6

rule ESD 7 nmos



error  
ESD.7

rule ESD 7 pmos



error  
ESD.7

rule ESD 8 nmos

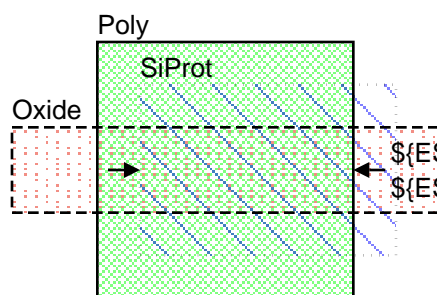


error  
ESD.8

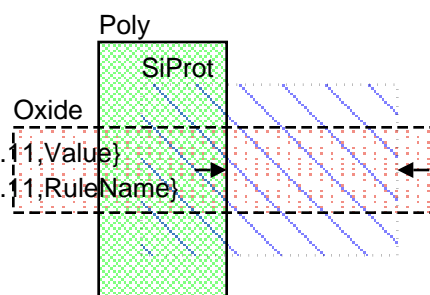
rule ESD 8 pmos



error  
ESD.8



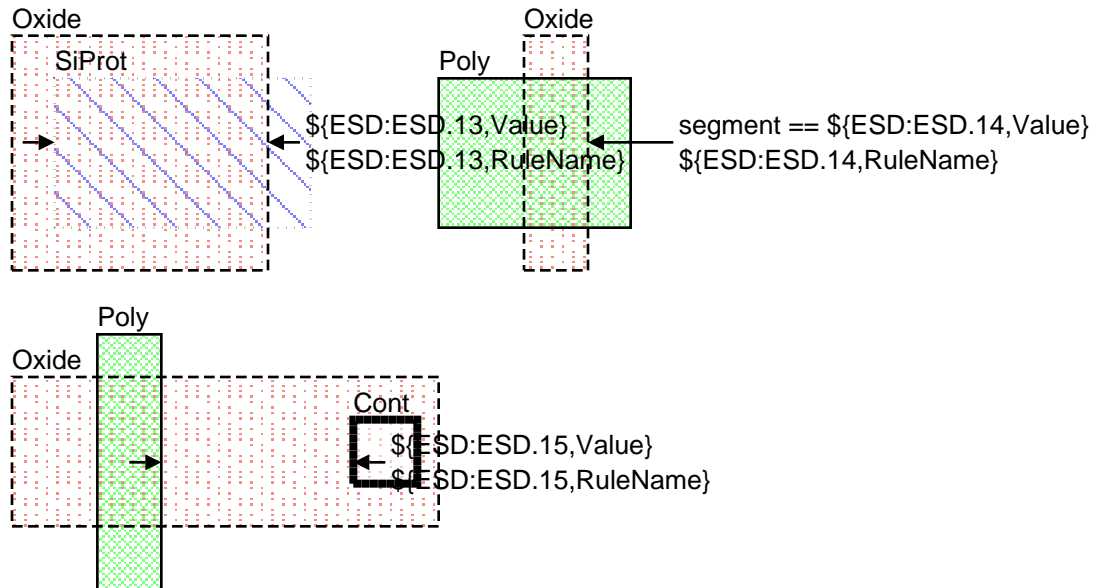
$\{ESD:ESD.11, Value\}$   
 $\{ESD:ESD.11, RuleName\}$



$\{ESD:ESD.12, Value\}$   
 $\{ESD:ESD.12, RuleName\}$

## ESD Design Rules (continued)

ESDdummy



## Bond Pad Design Rules

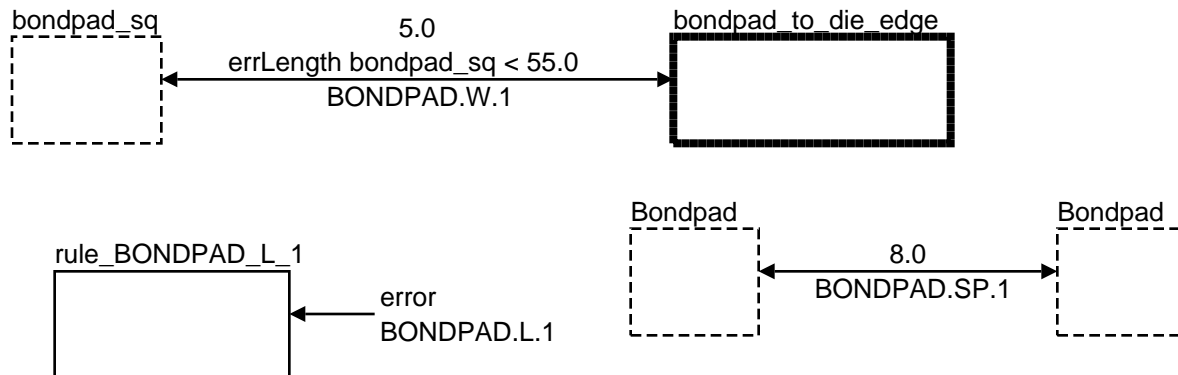
- 1) The bond pad structure must contain all Metal levels and all Via levels.
- 2) Metals over the Bonpad area must NOT have stress relief slots.
- 3) Vias on odd levels should be on top of each other. Vias on even levels should be on top of each other.

Comment Table In-Line Bond Pad Design Rules

Rule Name	Value (um)	Description
BONDPAD.W.1	55.0	Minimum Bondpad width of edges parallel to the die edge.
BONDPAD.L.1	68.0	Minimum Bondpad length of edges perpendicular to the die edge.
BONDPAD.SP.1	8.0	Minimum Bondpad to Bondpad spacing.
BONDPAD.E.1	2.0	Minimum Metal (all levels) enclosure of Bondpad.
BONDPAD.SP.2	3.0	Minimum Bondpad Metal to Metal (including Bondpad Metal) spacing.
BONDPAD.B.1	1.8~3.2	Minimum length of Bonpad Metal beveled corner. All Bondpad Metal corners must be beveled at 45 degrees.
BONDPAD.W.2	0.14	Minimum and maximum Bondpad Via k width (k = 1, 2, 3, 4, 5, 6).
BONDPAD.W.3	0.36	Minimum and maximum Bondpad Via k width (k = 7, 8).
BONDPAD.SP.3	0.22	Minimum Bondpad Viak to Bondpad Viak spacing (k = 1, 2, 3, 4, 5, 6).
BONDPAD.SP.4	0.54	Minimum Bondpad Viak to Bondpad Viak spacing (k = 7, 8).
BONDPAD.E.2	0.05	Minimum Bondpad Metalk to Bondpad Viak enclosure (k = 1, 2, 3, 4, 5, 6, 7, 8). Minimum Bondpad Metalk+1 to Bondpad Viak enclosure (k = 1, 2, 3, 4, 5, 6, 7, 8).
BONDPAD.E.3	0.09	Maximum Bondpad Metalk to Bondpad Viak enclosure (k = 7, 8). Maximum Bondpad Metalk+1 to Bondpad Viak enclosure (k = 7, 8).
BONDPAD.R.1	16.0	Minimum Bondpad Viak inside Metalk to Metalk+1 crossing (k = 1, 2, 3, 4, 5, 6).
BONDPAD.R.2	4.0	Minimum Bondpad Viak inside Metalk to Metalk+1 crossing (k = 7, 8).
BONDPAD.SP.5	1.5	Minimum and Maximum Pad Metal slot to Pad Metal slot spacing.
BONDPAD.W.4	1.0	Minimum and Maximum Pad Metal slot width (expect first slot on each edge of Pad).
BONDPAD.W.5	5.0	Minimum and Maximum Pad Metalk width in outer ring of Pad Metalk (expect for the bevelled corners) (k = 1, 2, 3, 4, 5, 6, 7, 8).
BONDPAD.SP.6	1.0~3.5	Minimum and Maximum Pad Metalk ring to nearest Pad Metalk across first slot (k = 1, 2, 3, 4, 5, 6, 7, 8).
BONDPAD.SP.7	1.1	Minimum Pad Viak array to Pad Viak array spacing (k = 1, 2, 3, 4, 5, 6, 7, 8).



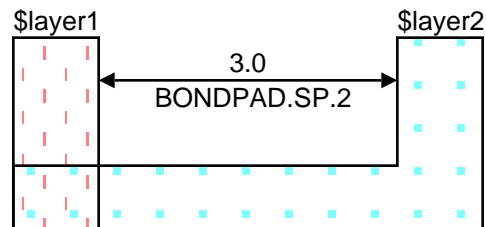
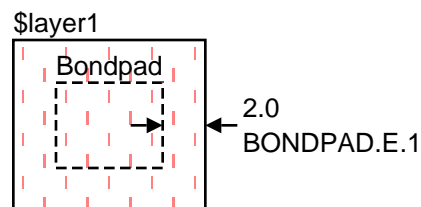
## Bond Pad Design Rules (continued)



macro

Macro Table

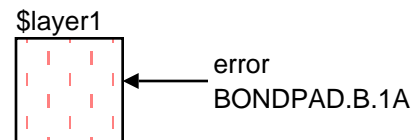
\$layer1	\$layer2
bondpad_metal1_filled	Metal1
bondpad_metal2_filled	Metal2
bondpad_metal3_filled	Metal3
bondpad_metal4_filled	Metal4
bondpad_metal5_filled	Metal5
bondpad_metal6_filled	Metal6
bondpad_metal7_filled	Metal7
bondpad_metal8_filled	Metal8
bondpad_metal9_filled	Metal9
bondpad_metal10_filled	Metal10
bondpad_metal11_filled	Metal11



macro

Macro Table

\$layer1	\$name1
rule_BONDPAD_B_1_m1	Metal1
rule_BONDPAD_B_1_m2	Metal2
rule_BONDPAD_B_1_m3	Metal3
rule_BONDPAD_B_1_m4	Metal4
rule_BONDPAD_B_1_m5	Metal5
rule_BONDPAD_B_1_m6	Metal6
rule_BONDPAD_B_1_m7	Metal7
rule_BONDPAD_B_1_m8	Metal8
rule_BONDPAD_B_1_m9	Metal9
rule_BONDPAD_B_1_m10	Metal10
rule_BONDPAD_B_1_m11	Metal11

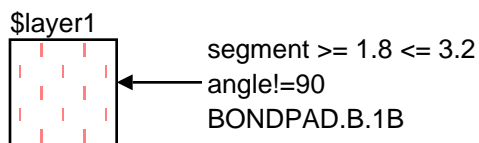


## Bond Pad Design Rules (continued)

macro

Macro Table

\$layer1	\$name1
bondpad_metal1	Metal1
bondpad_metal2	Metal2
bondpad_metal3	Metal3
bondpad_metal4	Metal4
bondpad_metal5	Metal5
bondpad_metal6	Metal6
bondpad_metal7	Metal7
bondpad_metal8	Metal8
bondpad_metal9	Metal9
bondpad_metal10	Metal10
bondpad_metal11	Metal11



## Bond Pad Design Rules (continued)

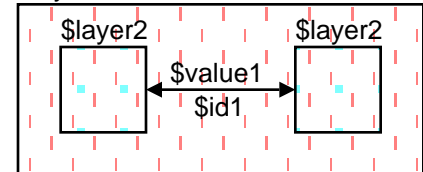
BONDPAD.W.2 and BONDPAD.W.3 - covered by VIAk.W.1.

macro

Macro Table

\$layer1	\$layer2	\$value1	\$id1
bondpad_metal1	Via1	0.22	BONDPAD.SP.3
bondpad_metal2	Via2	0.22	BONDPAD.SP.3
bondpad_metal3	Via3	0.22	BONDPAD.SP.3
bondpad_metal4	Via4	0.22	BONDPAD.SP.3
bondpad_metal5	Via5	0.22	BONDPAD.SP.3
bondpad_metal6	Via6	0.22	BONDPAD.SP.3
bondpad_metal7	Via7	0.22	BONDPAD.SP.4
bondpad_metal8	Via8	0.22	BONDPAD.SP.4
bondpad_metal9	Via9	0.54	BONDPAD.SP.4
bondpad_metal10	Via10	0.54	BONDPAD.SP.4

\$layer1

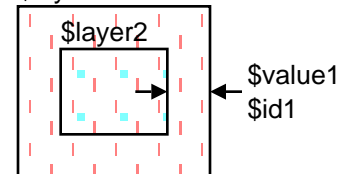


macro

Macro Table

\$layer1	\$layer2	\$name1	\$value1	\$id1
bondpad_metal1	Via1	Metal1	0.05	BONDPAD.E.2
bondpad_metal2	Via2	Metal2	0.05	BONDPAD.E.2
bondpad_metal3	Via3	Metal3	0.05	BONDPAD.E.2
bondpad_metal4	Via4	Metal4	0.05	BONDPAD.E.2
bondpad_metal5	Via5	Metal5	0.05	BONDPAD.E.2
bondpad_metal6	Via6	Metal6	0.05	BONDPAD.E.2
bondpad_metal7	Via7	Metal7	0.05	BONDPAD.E.3
bondpad_metal8	Via8	Metal8	0.05	BONDPAD.E.3
bondpad_metal9	Via9	Metal9	0.09	BONDPAD.E.3
bondpad_metal10	Via10	Metal9	0.09	BONDPAD.E.3

\$layer1

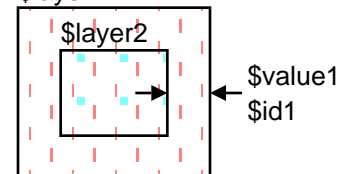


macro

Macro Table

\$layer1	\$layer2	\$name1	\$value1	\$id1
bondpad_metal2	Via1	Metal2	0.05	BONDPAD.E.2
bondpad_metal3	Via2	Metal3	0.05	BONDPAD.E.2
bondpad_metal4	Via3	Metal4	0.05	BONDPAD.E.2
bondpad_metal5	Via4	Metal5	0.05	BONDPAD.E.2
bondpad_metal6	Via5	Metal6	0.05	BONDPAD.E.2
bondpad_metal7	Via6	Metal7	0.05	BONDPAD.E.2
bondpad_metal8	Via7	Metal8	0.05	BONDPAD.E.3
bondpad_metal9	Via8	Metal9	0.05	BONDPAD.E.3
bondpad_metal10	Via9	Metal10	0.09	BONDPAD.E.3
bondpad_metal11	Via10	Metal11	0.09	BONDPAD.E.3

\$layer1



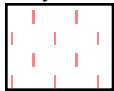
## Bond Pad Design Rules (continued)

macro

Macro Table

\$layer1	\$name1	\$name2	\$name3	\$value	\$id1
rule_BONDPAD_R_1_via1	Via1	Metal1	Metal2	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via2	Via2	Metal2	Metal3	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via3	Via3	Metal3	Metal4	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via4	Via4	Metal4	Metal5	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via5	Via5	Metal5	Metal6	16.0	BONDPAD.R.1
rule_BONDPAD_R_1_via6	Via6	Metal6	Metal7	16.0	BONDPAD.R.1
rule_BONDPAD_R_2_via7	Via7	Metal7	Metal8	16.0	BONDPAD.R.1
rule_BONDPAD_R_2_via8	Via8	Metal8	Metal9	16.0	BONDPAD.R.1
rule_BONDPAD_R_2_via9	Via9	Metal9	Metal10	4.0	BONDPAD.R.2
rule_BONDPAD_R_2_via10	Via10	Metal10	Metal11	4.0	BONDPAD.R.2

\$layer1



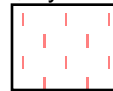
error  
\$id1

macro

Macro Table

\$layer1	\$name1
rule_BONDPAD_SP_5_metal1	Metal1
rule_BONDPAD_SP_5_metal2	Metal2
rule_BONDPAD_SP_5_metal3	Metal3
rule_BONDPAD_SP_5_metal4	Metal4
rule_BONDPAD_SP_5_metal5	Metal5
rule_BONDPAD_SP_5_metal6	Metal6
rule_BONDPAD_SP_5_metal7	Metal7
rule_BONDPAD_SP_5_metal8	Metal8
rule_BONDPAD_SP_5_metal9	Metal9
rule_BONDPAD_SP_5_metal10	Metal10

\$layer1



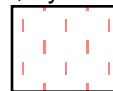
error  
BONDPAD.SP.5

macro

Macro Table

\$layer1	\$name1
rule_BONDPAD_W_4_metal1	Metal1
rule_BONDPAD_W_4_metal2	Metal2
rule_BONDPAD_W_4_metal3	Metal3
rule_BONDPAD_W_4_metal4	Metal4
rule_BONDPAD_W_4_metal5	Metal5
rule_BONDPAD_W_4_metal6	Metal6
rule_BONDPAD_W_4_metal7	Metal7
rule_BONDPAD_W_4_metal8	Metal8
rule_BONDPAD_W_4_metal9	Metal9
rule_BONDPAD_W_4_metal10	Metal10

\$layer1



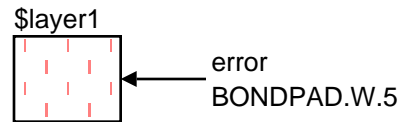
error  
BONDPAD.W.4

## Bond Pad Design Rules (continued)

macro

Macro Table

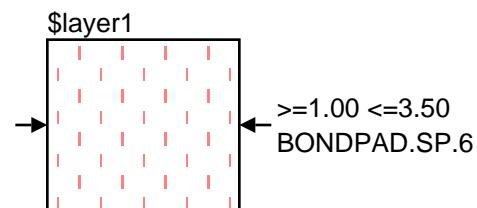
\$layer1	\$name1
rule_BONDPAD_W_5_metal1	Metal1
rule_BONDPAD_W_5_metal2	Metal2
rule_BONDPAD_W_5_metal3	Metal3
rule_BONDPAD_W_5_metal4	Metal4
rule_BONDPAD_W_5_metal5	Metal5
rule_BONDPAD_W_5_metal6	Metal6
rule_BONDPAD_W_5_metal7	Metal7
rule_BONDPAD_W_5_metal8	Metal8
rule_BONDPAD_W_5_metal9	Metal9
rule_BONDPAD_W_5_metal10	Metal10



macro

Macro Table

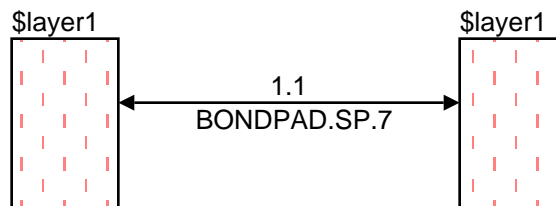
\$layer1	\$name1
bondpad_metal1_slot_on_edge	Metal1
bondpad_metal2_slot_on_edge	Metal2
bondpad_metal3_slot_on_edge	Metal3
bondpad_metal4_slot_on_edge	Metal4
bondpad_metal5_slot_on_edge	Metal5
bondpad_metal6_slot_on_edge	Metal6
bondpad_metal7_slot_on_edge	Metal7
bondpad_metal8_slot_on_edge	Metal8
bondpad_metal9_slot_on_edge	Metal9
bondpad_metal10_slot_on_edge	Metal10



macro

Macro Table

\$layer1	\$name1
bondpad_via1_array	Via1
bondpad_via2_array	Via2
bondpad_via3_array	Via3
bondpad_via4_array	Via4
bondpad_via5_array	Via5
bondpad_via6_array	Via6
bondpad_via7_array	Via7
bondpad_via8_array	Via8
bondpad_via9_array	Via9
bondpad_via10_array	Via10



# CMOS Digital Electrical Parameters

## Sheet Resistances The units are ohms/square

Global Parameters

R_metal1	0.0736	Metal 1 sheet resistance	
R_metal2_7	0.0604	Metal 2,3,4,5,6,7 sheet resistance	
R_metal8_10	0.0214	Metal 8,9,10 sheet resistance	
R_metal11	0.021	Metal 11 sheet resistance	
R_snpoly	15	Salicide N+ Poly sheet resistance	
R_sppoly	15	Salicide P+ Poly sheet resistance	
R_nsnpoly	200	Non-salicide N+ Poly sheet resistance	
R_nsppoly	650	Non-salicide P+ Poly sheet resistance	
R_snactive	18	Salicide N+ Oxide sheet resistance	
R_spactive	15	Salicide P+ Oxide sheet resistance	
R_nsnactive	100	Non-salicide N+ Oxide sheet resistance	
R_nspactive	200	Non-salicide P+ Oxide sheet resistance	
R_nwell	450	Nwell sheet resistance	
R_pwell	1000	Pwell sheet resistance	

## Contact/Via Resistances The units are ohms/contact or ohms/via

Global Parameters

R_via10	0.4	Via 10 resistance	
R_via8_9	0.28	Via 8,9 resistance	
R_via1_7	0.5	Via 1,2,3,4,5,6,7 resistance	
R_metal1-contact	1	Metal 1 to Contact resistance	
R_poly-contact	45	Poly to Contact resistance	
R_pplus-contact	62	P+ Oxide to Contact resistance	
R_nplus-contact	75	N+ Oxide to Contact resistance	

## Current Densities The units are ma/um

Global Parameters

L_metal10_11	8	Metal 10,11 current density	
L_metal1_9	2	Metal 1,2,3,4,5,6,7, 8, 9 current density	

## Contact/Via Current Densities The units are ohm/contact or ma/via

Global Parameters

I_via1_8	0.1	Via 1,2,3,4,5,6 current density	
I_Via9_10	0.8	Via 7,8 current density	
I_metal-contact-poly	0.1	Metal 1 Contact to Poly current density	
I_metal-contact-oxide	0.1	Metal 1 Contact to Oxide current density	

## Layer and Dielectric Thickness

Comment Table

Layer	Thickness (A)	Description
Pass2	7500	k= 8.0
Pass1	6500	k = 4.2
IMD11a	14000	K = 4.2
Metal11	14000	Cu
IMD10b	6000	K = 4.2
IMD10a	10000	K = 4.2
Metal10	10000	Cu
IMD9b	6000	K = 4.2
IMD9a	10000	K = 4.2
Metal9	10000	Cu
IMD8b	3000	K = 2.6
IMD8a	1500	K = 4.2
Metal8	1500	Cu
IMD7b	3000	K = 2.6
IMD7a	1500	K = 4.2
Metal7	1500	Cu
IMD6b	3000	K = 2.6
IMD6a	1500	K = 4.2
Metal6	1500	Cu
IMD5b	3000	K = 2.6
IMD5a	1500	K = 4.2
Metal5	1500	Cu
IMD4b	3000	K = 2.6
IMD4a	1500	K = 4.2
Metal4	1500	Cu
IMD3b	3000	K = 2.6
IMD3a	1500	K = 4.2
Metal3	1500	Cu
IMD2b	3000	K = 2.6
IMD2a	1500	K = 4.2
Metal2	1500	Cu
IMD1b	3000	K = 2.6
IMD1a	1500	K = 4.2
Metal1	1500	Cu
ILD	3000	k = 4.2
LINER	1200	k = 7
Poly	1200	
STI (FOX)	3500	k=3.9

**For further information on electrical parameters and Model parameters, Please look into the following document.  
gpdk045\_PDK\_Model\_Report.pdf**



# Connectivity Definition

## Connectivity

