



# **Process Design Kit Reference Manual**

for

## **Generic**

# **Process Design Kit**

## **180um**

## **Revision 3.3**

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# Overview

The purpose of this Reference Manual is to describe the technical details of the Generic Process Design Kit (“GPDK”) provided by Cadence Design Systems, Inc. (“Cadence”).

**THIS PDK IS INTENDED TO BE USED FOR DEMONSTRATION PURPOSES ONLY.**

## 1.1 Software Environment

The GPDK has been designed for use within a Cadence software environment that consists of the following tools -

- Virtuoso Analog Design Environment
- Virtuoso Schematic Composer
- Spectre Circuit Simulator
- Virtuoso Layout Editor
- Virtuoso-XL
- Virtuoso Custom Router (VCR)
- Diva
- Assura

This PDK requires the following UNIX environmental variables

“CDS\_Netlisting\_Mode” to be set to “Analog”

“CDSHOME” to be set to the Cadence DFII installation path

## 1.2 Software Releases

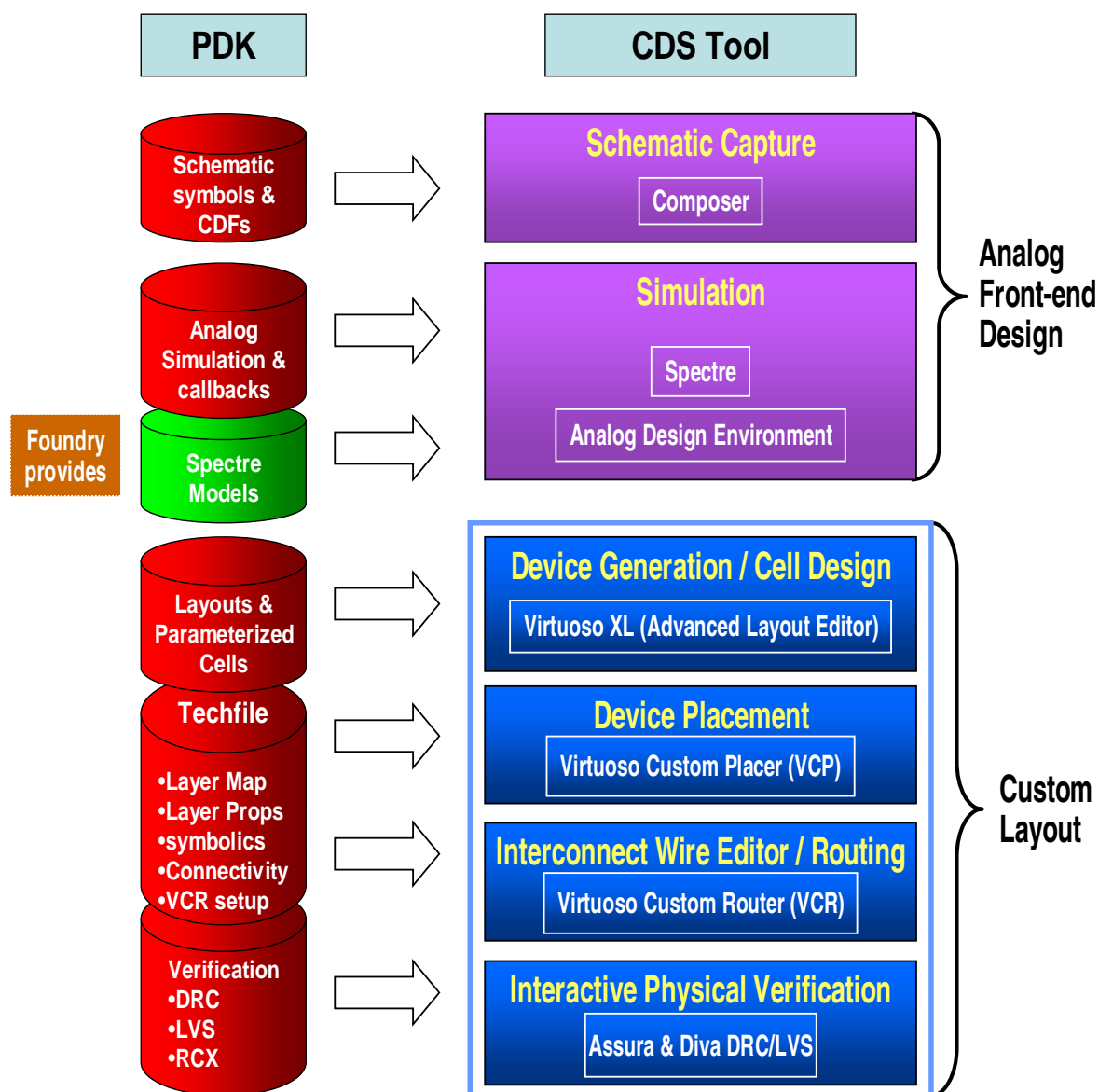
This PDK was tested for use with Cadence IC 5.1.41 and IC6.1.3 Release.

## 1.3 Training

Cadence DFII software training is not provided as part of this PDK. Please consult Cadence Education Service for a list of available training courses and location schedules.

## 2 What makes up a PDK?

PDK stands for Process Design Kit. A PDK contains the process technology and needed information to do device-level design in the Cadence DFII environment.



## 3 Installation of the PDK

The user who will own and maintain the PDK should logon to the computer.

Choose a disk and directory under which the PDK will be installed. This disk should be exported to all client machines and must be mounted consistently across all client machines.

Connect to the directory where the PDK will be installed:

```
cd <pdk_install_directory>
```

Extract the PDK from the archive using the following commands:

```
zcat <path_to_pdk_tar_file>/pdk.tar.Z | tar xf -
```

The default permissions on the PDK have already been set to allow only the owner to have write, read and execute access. Other users will have only read and execute access.

## 4 PDK Install Directory Structure/Contents

Within the <**pdk\_install\_directory**> directory there are several directories to organize the information associated with the PDK.

assura\_tech.lib - file containing the Cadence Assura initialization path

cds.lib - file containing pointer to the Cadence CDB initialization file.

cds.lib.cdb - file containing the Cadence CDB initialization file.

cds.lib.oa22 - file containing the Cadence OA 2.2 initialization file.

docs - directory containing the Cadence PDK documentation

libs.cdba - CDB GPDK Process PDK Cadence Library directory

libs.oa22 - OA 2.2 GPDK Process PDK Cadence Library directory

models - directory that contains the PDK models

neocell - directory containing the Neocell technology files

neockt - directory containing the Neocircuit technology files

pv - directory containing the Assura and Diva verification files

techfiles - directory containing ASCII versions of the CDB and OA 2.2 techfiles

## 5 Creation of a Design Project

A unique directory should be created for each circuit design project. The following command can be executed in UNIX:

```
mkdir ~/circuit_design
```

```
cd ~/circuit_design
```

All work by the user should be performed in this circuit design directory. The following file should be copied from the PDK install directory to begin the circuit design process. The following command can be used:

```
cp <pdk_install_directory>/display.drf .
```

Next the user should create a "cds.lib" file. Using any text editor the following entry should be put in the cds.lib file:

```
INCLUDE <pdk_install_directory>/cds.lib
```

Where "pdk\_install\_directory" is the path to where the GPDK PDK was installed.

The following UNIX links are optional but may aid the user in entering certain forms with the Cadence environment. In UNIX the following command can be used:

```
ln -s <pdk_install_directory>/models
```

```
ln -s <pdk_install_directory>/stream
```

Where, again, "pdk\_install\_directory" is the path to where the GPDK PDK was installed.

## 6 Technology File Methodology

The GPDK Library techfile will be designated as the **master** techfile. This techfile will contain all required techfile information. There is an ASCII version of this techfile shipped with the PDK. This ASCII version represents the techfile currently compiled into the gpdk library

The **attach** method should be used for any design library that is created. This allows the design database techfile to be kept in sync with the techfile in the process PDK. To create a new library that uses an attached techfile, use the command *File->New->Library* from either the CIW or library manager and select the *Attach to an existing techfile* option. Select the GPDK library when asked for the name of the *Attach To Technology Library*.

## 7 Customizing Layer Display Properties

The display.drf can be autoloaded at Cadence start-up time or manually loaded during the Cadence session. For the file to be autoloaded, the display.drf file must be located in the Cadence start-up directory. To manually load the display.drf file (or load a new version), choose *Tools->Display Resources->Merge Files...* from the CIW and enter the location of the display.drf file that you want to use. If the display.drf file is not autoloaded and you do not manually load it, you will get error messages about missing packets when you try to open a schematic or layout view and you will not be able to see any process specific layers.

The GPDK process display.drf file can be found in the PDK install directory.

Listed below are the packet, color, lineStyle, and stipplePattern definitions for a metal3 drawing layer. The packet info references predefined color, lineStyle, and stipplePattern definitions. Any of these can be changed to suit an individual user's preferences in the project copy of the display.drf file.

drDefinePacket(

```
;( DisplayName      PacketName      Stipple      LineStyle
  Fill      Outline )
( display      m3      dots      solid      green green )
)
```

drDefineColor(

```
;( DisplayName      ColorName      Red      Green      Blue      Blink )
( display      green      0      204      102      nil )
)
```

drDefineLineStyle(

```
;( DisplayName      LineStyle      Size      Pattern )
( display      solid      1      (1 1 1) )
)
```

drDefineStipple(

```
;( DisplayName      StippleName      Bitmap )
( display      dots      (
                                (0 1 0 0 0 1 0 0 0 1 0 0 0 1 0 0)
                                )
)
```

(000000000000000000)  
(0001000100010001)  
(000000000000000000)  
(0100010001000100)  
(000000000000000000)  
(0001000100010001)  
(000000000000000000)  
(0100010001000100)  
(000000000000000000)  
(0001000100010001)  
(000000000000000000)  
(0100010001000100)  
(000000000000000000)  
(0001000100010001)  
(000000000000000000)  
(0001000100010001)  
(000000000000000000)

)

## 8 Schematic Design

The user should follow the guidelines listed below while building schematics using Composer:

Project libraries should list the primitive PDK library as a reference library in the library properties form.

Users can add instances from the PDK library to designs stored in the project libraries.

When performing hierarchical copy of schematic designs care should be taken to preserve the references to the PDK libraries. These references should not be copied locally to the project directories and the references set to the local copy of PDK cells. This would prevent your designs from inheriting any fixes done to the PDK library from an upgrade.

Users should exercise caution when querying an instance and changing the name of the cell and replacing it with a reference to another cell. While like parameters will inherit values, callbacks are not necessarily executed. This would cause dependent parameters to have incorrect values.

Schematics should be designed with schematic driven layout methodology in mind. Partitioning of schematics, hierarchical design, input and output ports, should be done in a clean and consistent fashion.

Usage of pPar and iPar in a schematic design context is discouraged. While this works fine in schematic design, this could lead to problems while performing schematic driven layout.

## 9 Library Device Setup

### 9.1 Resistors

The resistors in the library consist of two types; diffused and insulated. The diffused types include n+ and are 2 terminal resistors with diode backplates. The insulated resistors are those that are isolated from silicon by an insulator (oxide) such as poly resistors. These resistors are 2 terminal devices. Only one of the series or parallel parameters can be equal to an integer other than 1 at a time. When series is set to a number other than 1, that number of segments are connected in series with metal. The segments are placed side by side for both series and parallel combinations. There is no change in the segment placement. Serpentine resistor layouts are not allowed.

**Units:**

The width is specified in meters for schematic simulation. All parameters entered into the resistor form must be integers or floating-point numbers. No design variables are supported due to the calculations that must be performed on the entries.

**Calculation:**

The width and length are snapped to grid, and the resistances are recalculated and updated on the component form based on actual dimensions.

**Simulation:**

These resistors are netlisted as Spectre resistor devices for simulation purposes.

### 9.2 Capacitors

All capacitors in the PDK library are 2 terminal devices. The capacitors for this process are Mimcaps. Mimcaps are metal on metal capacitors.

**Units:**

The length and width are specified in meters for schematic simulation. All parameters entered into the capacitor form must be integers or floating-point numbers. Design variables are supported here.

**Calculation:**

The width and length are snapped to grid, and the capacitance is recalculated and updated on the component form based on actual dimensions.

**Simulation:**

These mimcaps are netlisted as Spectre capacitor devices for simulation purposes.

## 9.3 MOSFETS

All mosfets in the PDK library are 4 terminal devices, with the body terminal explicitly connected.

**Units:**

Length and width are in meters, with areas and perimeters in meters squared and meters, respectively. Design variables are allowed for Length and Width entries.

**Calculation:**

The area and perimeter parameters for the sources and drains are calculated from the width and the number of fingers used. This calculation assumes that the drain will always have the lesser capacitance (area) when there is an even number of fingers (odd number of diffusion areas). The Width per finger is calculated by dividing the width by the number of fingers. This parameter is for viewing by the designer.

**Simulation:**

These mosfets are netlisted as their predefined device names for simulation purposes. The provided model definitions are used for these devices.

## 9.4 Bipolar Transistors

This PDK contains a vertical PNP transistor that has a substrate collector. The device has fixed dimensions for its emitter size. This device is typical of a Cmos process.

A bipolar npn and pnp also exist.

**Units:**

The emitter width is specified in meters for schematic entry. All parameters entered into the npn and pnp form must be integers or floating point numbers. Design variables are supported here.

**Simulation:**

The bipolar npn and pnp are netlisted as BJT devices with fixed emitter area for simulation purposes. Default spectre model definitions are used for these devices.

## 9.5 Inductor

The inductor in the PDK library is a 2 terminal device. The inductor for this process is created using the top layer of Metal Interconnect.

**Units:**

The number of turns, width, space, and inner radius are specified in meters for schematic entry. All parameters entered into the inductor form must be integers or floating-point numbers. Design variables are supported here.

**Calculation:**

The width space and inner radius are snapped to grid, and the inductance is calculated and updated on the component form based on actual dimensions.

**Simulation:**

The inductor is netlisted as a Spectre inductor device for simulation purposes.

# 10 Supported Devices

## 10.1 MOSFETS

- nmos - NMOS transistor
- nmos3 - 3 terminal NMOS transistor with an inherited connection for the Body
- pmos - PMOS transistor
- pmos3 - 3 terminal PMOS transistor with an inherited connection for the Body

## 10.2 RESISTORS

- nplusres - N+ Diffused Resistor
  - ◆  $Rho = 300 \text{ ohms/sq}$
- polyres - Poly Resistor
  - ◆  $Rho = 7.5 \text{ ohms/sq}$

## 10.3 CAPACITORS

- mimcap - metal-to-metal capacitor
  - ◆  $CapA = 1.0fF/\mu m^2$
- nmoscap - NMOS transistor configured as a capacitor
  - ◆  $CapA = 8.0fF/\mu m^2$

## 10.4 INDUCTOR

- inductor - Metal 3 Inductor

## 10.5 BIPOLARS

- vnpn - CMOS vertical PNP with substrate collector
  - Fixed emitter area
- npn - Bipolar NPN
  - Variable emitter area for layout, Fixed emitter area for simulation
- pnp - Bipolar vertical PNP
  - Variable emitter area, Fixed emitter area for simulation

## 10.6 DIODES

- ndio - N type diode
  - Variable diode length and width
- pdio - P type diode
  - Variable diode length and width

# 11 Views provided

The following table explains the use of the cellviews provided as part of this PDK:

symbol	Used in Composer schematics
spectre	Simulation / netlisting view for the Spectre simulator
auLvs	Netlisting view for DIVA and Assura
auCdl	Circuit Descriptive Language netlisting view typically used to generate a netlist for Dracula or third party simulators.
ivpcell	Device recognition symbol used in the extracted layout for netlisting purposes with DIVA and Assura
layout	Fixed cell or pcell used in Virtuoso Layout Editor.

## 11.1 MOSFETS

- Four terminals (D, G, S, B)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

## 11.2 RESISTORS

- Three terminals (PLUS, MINUS, B) for diffused resistor
- Two terminals (PLUS, MINUS) for poly resistor
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

## 11.3 CAPACITORS

- Two terminals (PLUS, MINUS) for mimcap
- Three terminals (TOP, BOT, B) for nmoscapp
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

## 11.4 INDUCTOR

- Two terminals (PLUS, MINUS)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

## 11.5 BIPOLARS

- Three terminals (C, B, E)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Fixed for vnpn, Pcells for npn/pnp)

## 11.6 DIODES

- Two terminals (PLUS, MINUS)
- symbol, spectre, auLvs, auCdl, ivpcell, layout (Pcells)

## 12 CDF parameters

### 12.1 MOSFETS

<b>Model Name</b>	Spectre model name (non-editable)
<b>l (M)</b>	Gate length in meters
<b>Calculate Width Method</b>	Cyclic which controls user entry of total Width value or individual finger Width value
<b>w (M)</b>	Gate width in meters (non-editable using fingerWidth)
<b>Number of Fingers</b>	Number of poly gate stripes used in layout (w/nf width)
<b>Width Per Finger</b>	Width of each gate stripe (non-editable using totalWidth)
<b>Multiplier</b>	Number of Parallel MOS devices
<b>Calc Diff Params</b>	Cyclic which controls the calculation of area and periphery of the source/drain regions for simulation. Default is true which auto calculates the values. If nil, the user can enter the values.
<b>Source diffusion area</b>	Calculated source diffusion area in square meters
<b>Drain diffusion area</b>	Calculated drain diffusion area in square meters
<b>Source diffusion periphery</b>	Calculated source diffusion periphery in meters
<b>Drain diffusion periphery</b>	Calculated drain diffusion periphery in meters

## MOSFET ADD INSTANCE FORM

**Edit Object Properties**

OK Cancel Apply Defaults Previous Next Help

Apply To ☐ only current ☐ instance

Show ☐ system ☒ user ☒ CDF

Property	Value	Display
Library Name	gpdk	off
Cell Name	rmos3	off
View Name	symbol	off
Instance Name	MN	off

CDF Parameter	Value	Display
Model name	rmos1	off
I (M)	180.0n M	off
Calculate Width Method	totalWidth	off
w (M)	2u M	off
Number of Fingers	1	off
Width Per Finger	2u M	off
Multiplier	1	off
Calc Diff Params	<input checked="" type="checkbox"/>	off
Source diffusion area	1.2e-12	off
Drain diffusion area	1.2e-12	off
Source diffusion periphery	3.2u M	off
Drain diffusion periphery	3.2u M	off
Substrate Node	gnd	off

## 12.2 RESISTORS

Resistance (ohms)	Resistance value used for simulation
Contact Resistance (ohms)	Resistor contact resistance in ohms
Width (M)	Resistor width in meters
Length (M)	Resistor length in meters (non-editable)
Entry Mode	Allows user to specify either “r and w” or “l and w”
Multiplier	Number of Parallel Resistor devices

### RESISTOR ADD INSTANCE FORM

**Edit Object Properties**

OK Cancel Apply Defaults Previous Next Help

Apply To: ☐ only current ☐ instance

Show: ☐ system ☒ user ☒ CDF

Property	Value	Display
Library Name	gpdk	off <input type="checkbox"/>
Cell Name	nplusres	off <input type="checkbox"/>
View Name	symbol	off <input type="checkbox"/>
Instance Name	R0	off <input type="checkbox"/>

CDF Parameter	Value	Display
Resistance (Ohms)	4.6K Ohms	off <input type="checkbox"/>
Contact Resistance (Ohms)	0 Ohms	off <input type="checkbox"/>
Width (m)	600n M	off <input type="checkbox"/>
Length (m)	9.2u M	off <input type="checkbox"/>
Entry Mode	r & w <input type="radio"/>	off <input type="checkbox"/>
Multiplier	1	off <input type="checkbox"/>

## 12.3 CAPACITORS

<b>Capacitance</b>	Capacitance value used in simulation
<b>total Capacitance</b>	Capacitance multiplied times Multiplier (non-editable)
<b>l (M)</b>	Capacitor length in meters (non-editable for mimcap)
<b>w (M)</b>	Capacitor width in meters (non-editable for mimcap)

### 12.3.1 MIMCAP

The following parameters are for the mimcap only

<b>Spec</b>	Cyclic used to choose capacitor entry method (Capacitance, Cap & w, l & w)
<b>CapA (F/M<sup>2</sup>)</b>	Plate Capacitance (non-editable, units are Farads per Meter Squared)
<b>CapP (F/M)</b>	Fringe Capacitance (non-editable, units are Farads per Meter)

### 12.3.2 NMOSCAP

The following parameters are for the nmoscap only

<b>Spec</b>	cyclic used to choose capacitor entry method (Capacitance, Cap & l, Cap & w, l & w)
<b>Width Per Finger</b>	Width of each gate stripe (non-editable using totalWidth)
<b>Number of Fingers</b>	Number of poly gate stripes used in layout (w/nf width)
<b>Multiplier</b>	Number of Parallel MOS devices

## CAPACITOR ADD INSTANCE FORM

**Edit Object Properties**

OK Cancel Apply Defaults Previous Next Help

Apply To ☐ only current ☐ instance

Show ☐ system ☒ user ☒ CDF

Property	Value	Display
Library Name	gpdk	<input type="button" value="off"/>
Cell Name	mimcap	<input type="button" value="off"/>
View Name	symbol	<input type="button" value="off"/>
Instance Name	C1	<input type="button" value="off"/>

CDF Parameter	Value	Display
Capacitance	17.6f F	<input type="button" value="off"/>
total Capacitance	17.6f F	<input type="button" value="off"/>
Spec	<input type="button" value="Capacitance"/>	<input type="button" value="off"/>
I (M)	4u M	<input type="button" value="off"/>
w (M)	4u M	<input type="button" value="off"/>
CapA	0.001	<input type="button" value="off"/>
CapP	1e-10	<input type="button" value="off"/>

## 12.4 INDUCTOR

Inductance (H)	Inductance in Henry's based on calculation (non-editable)
Number of Turns	Fixed number of coil turns (1.5, 2.5, 3.5, 4.5, 5.5, 6.5, 7.5, 8.5, or 9.5)
Inner Radius	Radius of inner coil (non-editable)
Inductor Space	Space of top metal (non-editable)
Inductor Width	Width of top metal (non-editable)

### INDUCTOR ADD INSTANCE FORM

The screenshot shows the 'Edit Object Properties' dialog box for an inductor instance. The dialog has a title bar 'Edit Object Properties' and buttons for 'OK', 'Cancel', 'Apply', 'Defaults', 'Previous', 'Next', and 'Help'. Below the buttons, there are sections for 'Apply To' (with 'only current' and 'instance' radio buttons), 'Show' (with 'system', 'user', and 'CDF' checkboxes), and a 'Browse' button. The main area contains a table with columns 'Property', 'Value', and 'Display'. The properties listed are 'Library Name' (gpdk), 'Cell Name' (inductor), 'View Name' (symbol), and 'Instance Name' (I0). Below this table are 'Add', 'Delete', and 'Modify' buttons. At the bottom, there is another table for 'CDF Parameter' with columns 'Value' and 'Display'. The CDF parameters are 'Inductance (H)' (5.95156e-10), 'Number Of Turns' (2.5), 'Inner Radius' (20u M), 'Inductor Space' (2u M), and 'Inductor Width' (5u M). All 'Display' checkboxes are currently 'off'.

Property	Value	Display
Library Name	gpdk	off
Cell Name	inductor	off
View Name	symbol	off
Instance Name	I0	off

CDF Parameter	Value	Display
Inductance (H)	5.95156e-10	off
Number Of Turns	2.5	off
Inner Radius	20u M	off
Inductor Space	2u M	off
Inductor Width	5u M	off

## 12.5 BIPOLARS

<b>Model name</b>	Spectre model name (non-editable)
<b>Area</b>	Emitter Area (non-editable)
<b>Emitter width</b>	The width of the emitter, in meters (For npn and pnp only)
<b>Emitter Size</b>	The length and width of the emitter, in meters (For vnp only)
<b>Multiplier</b>	Number of Parallel Bipolar devices

### BIPOLAR ADD INSTANCE FORM

**Edit Object Properties**

OK Cancel Apply Defaults Previous Next Help

Apply To: ☐ only current ☐ instance

Show: ☐ system ☒ user ☒ CDF

Browse Reset Instance Labels Display

Property	Value	Display
Library Name	gpdk	<input type="checkbox"/> off
Cell Name	npr	<input type="checkbox"/> off
View Name	symbol	<input type="checkbox"/> off
Instance Name	q	<input type="checkbox"/> off

Add Delete Modify

CDF Parameter	Value	Display
Model name	npr	<input type="checkbox"/> off
Area	0.36	<input type="checkbox"/> off
Emitter width	0.6	<input type="checkbox"/> off
Multiplier	1	<input type="checkbox"/> off

## 12.6 DIODES

<b>Model name</b>	Spectre model name (non-editable)
<b>Device Area</b>	Calculated junction area in meters squared (non-editable)
<b>Multiplier</b>	Number of Parallel Diode devices
<b>Length (M)</b>	Diode length in meters
<b>Width (M)</b>	Diode width in meters

### DIODE ADD INSTANCE FORM

**Edit Object Properties**

OK Cancel Apply Defaults Previous Next Help

Apply To: ☐ only current ☐ instance

Show: ☐ system ☒ user ☒ CDF

Property	Value	Display
Library Name	gpdk	<input type="checkbox"/> off
Cell Name	ndio	<input type="checkbox"/> off
View Name	symbol	<input type="checkbox"/> off
Instance Name	D0	<input type="checkbox"/> off

CDF Parameter	Value	Display
Model name	dion	<input type="checkbox"/> off
Device area	1e-12	<input type="checkbox"/> off
Multiplier	1	<input type="checkbox"/> off
Length (M)	1u	<input type="checkbox"/> off
Width (M)	1u	<input type="checkbox"/> off

## 13 Component Label Defaults

### 13.1 MOSFETS

- component parameters: l, w, fingers, m
- operating point: ids, vgs, vds, vth, vdsat
- model: vto, kp, gamma
- instance name prefix: MN, MP

### 13.2 RESISTORS

- component parameters: r, w, l
- operating point: v i pwr
- model: -
- instance name prefix: R

### 13.3 CAPACITORS

- component parameters: c, l, w, m
- operating point: -
- model: -
- instance name prefix: C

### 13.4 INDUCTORS

- component parameters: model, nr, rad
- operating point: -
- model: -
- instance name prefix: L

### 13.5 BIPOLARS

- component parameters: model, area, m
- operating point: betadc, ic, Vce
- model: bf, is, va
- instance name prefix: Q

## 13.6 DIODES

- component parameters: model, area, m
- operating point: id, vd, reg
- model: is, rs, n
- instance name prefix: D

## 14 Spectre Models

This PDK supports the Cadence Spectre circuit simulator, including corner modeling of the MOSFETs.

The following model library setup should be entered into the Setup Model Libraries form in the Analog Artist Environment.

Model Library File	Section
<pdk_install_directory>/models/gpdk.scs	NN

In Analog Artist, you may select the appropriate corner parameters by choosing the appropriate 'section' of the gpdk.scs file:

NN - Typical N, Typical P

FF - Fast N, Fast P

SF - Slow N, Fast P

FS - Fast N, Slow P

SS - Slow N, Slow P

The Bipolar models are included in the gpdk.scs file. They use the intrinsic bjt model supplied with Spectre. No corner modeling data is supplied for these devices.

## 15 Techfile Layers

Cadence will provide a standard display setup, and will not support desired changes to the display. The customer is free to modify the display.drf file used on-site to achieve any desired display.

CDS #	GDS #	CDS name	Drawn	Description
1	1	Oxide	yes	Oxide
2	2	Nwell	yes	N-well
3	3	Poly	yes	Poly Si
4	4	Nimp	yes	N+ SD Implant
5	5	Pimp	yes	P+ SD Implant
6	6	Cont	yes	Contact
7	7	Metal1	yes	Metal 1
8	8	Via1	yes	Via 1
9	9	Metal2	yes	Metal 2
10	10	Via2	yes	Via 2
11	11	Metal3	yes	Metal 3
12	12	Capdum	no	Capacitor Recognition Layer
13	13	Resdum	no	Resistor Recognition Layer
14	14	CapMetal	yes	Capacitor Metal
15	15	BJTdum	yes	BJT Recognition Layer
16	16	INDdummy	no	Inductor Recognition Layer #1
17	17	IND2dummy	no	Inductor Recognition Layer #2
18	18	Pwell	yes	BJT pwell layer
19	19	Nburied	yes	BJT buried layer / MOS isolation
20	20	NPNdummy	no	NPN Recognition Layer

21	21	PNPdummy	no	PNP Recognition Layer
22	22	DIOdummy	no	Diode Recognition Layer
30	30	Via3	yes	Via 3
31	31	Metal4	yes	Metal 4
32	32	Via4	yes	Via4
33	33	Metal5	yes	Metal 5
34	34	Via5	yes	Via 5
35	35	Metal6	yes	Metal 6
36	36	Bondpad	yes	Silox Opening
50	50	WellBody	no	Dummy Substrate Recognition Layer
66	66	scaPort	no	SCA interconnect layer
67	67	scaNwell	no	SCA Nwell Layer
68	68	scaNburied	no	SCA Nburied Layer
69	69	scaSelect	yes	SCA Selection Layer
100	100	allGeoShare	no	Neocell Recognition Layer
101	101	OVERLAP	no	P&R Floorplanning Layers

## 16 Virtuoso XL

The standard Cadence Virtuoso XL design flow will be implemented. This includes basic connectivity of connection layers, wells, and substrate, and symbolic contacts. The M factor will be used for device instance multiplier - there will be no conflict with the parameter used in cell operation. Names will be displayed on the layout views to aid in schematic-layout instance correlation. Auto-abutment of MOSFET devices is supported. Pin permuting of MOSFET and Resistor device is also supported. The skill pcell layouts are compiled into the PDK.

The users should follow the guidelines listed below for layout design:

The VirtuosoXL tool requires a separate license for operation.

Users obtain maximum leverage from the PDK by doing schematic driven layout in the Virtuoso XL environment. This flow will produce a correct by design layout. The Virtuoso Custom Router (VCR) can be used to finish the unconnected interconnect in the layout.

The VCR rules file for the target process is provided with the PDK.

Abutment is currently supported only for MOS transistors.

Note, abutment will work only on schematic driven layouts.

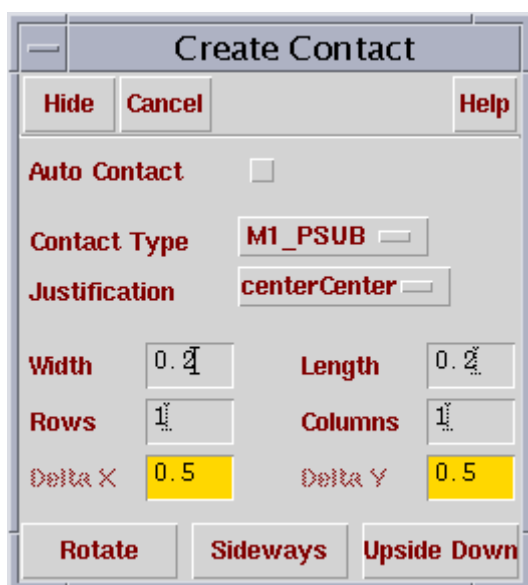
Schematic Driven Layout is recommended over Netlist Driven Layout.

NOTE: Skill pcell source code is not included in the PDK kit.

### 16.1 SYMBOLIC CONTACTS

- M1\_NIMP - Metal 1 to Nimp, Oxide contact
- M1\_NWELL - Metal 1 to Nwell contact
- M1\_PIMP - Metal 1 to Pimp, Oxide contact
- M1\_POLY1 - Metal 1 to Poly contact
- M1\_PSUB - Metal1 to Substrate contact
- M1\_NBL - Metal1 to Nburied contact
- M2\_M1 - Metal 2 to Metal 1 via contact
- M3\_M2 - Metal 3 to Metal 2 via contact
- M4\_M3 - Metal 4 to Metal 3 via contact
- M5\_M4 - Metal 5 to Metal 4 via contact
- M6\_M5 - Metal 6 to Metal 5 via contact

## ADD CONTACT FORM



The "Create Contact" dialog box is used to define the properties of a new contact. It features a title bar with a minus button and the text "Create Contact". Below the title bar are three buttons: "Hide", "Cancel", and "Help". The main area contains several settings:

- Auto Contact:** A checkbox that is currently unchecked.
- Contact Type:** A dropdown menu showing "M1\_PSUB".
- Justification:** A dropdown menu showing "centerCenter".
- Width:** A text input field containing "0.2".
- Length:** A text input field containing "0.2".
- Rows:** A text input field containing "1".
- Columns:** A text input field containing "1".
- Delta X:** A text input field containing "0.5", highlighted in yellow.
- Delta Y:** A text input field containing "0.5", highlighted in yellow.

At the bottom of the dialog are three buttons: "Rotate", "Sideways", and "Upside Down".

## 17 Dracula Support

Dracula support will be limited to providing the capability of creating an auCdl netlist. Listed below is an example of the CDL netlist for each device.

### CDL OUT FORM

**Virtuoso® CDL Out**

OK Cancel Defaults Apply Help

**Template File**   
Load Save

**Run In Background** ☒

**Library Browser**

**Top Cell Name**

**View Name**

**Library Name**

**Output File**

**Run Directory**

**Resistor Threshold Value**

**Resistor Model Name**

**Equivalents**

**Include File**

**Check Resistors** ☒ value ☐ size ☐ none

**Check Capacitors** ☒ value ☐ area ☐ perimeter ☐ both ☐ none

**Check Diodes** ☒ area ☐ perimeter

**Scale** ☒ meter ☐ micron ☐ none

## 18 Diva Decks

Cadence has developed the DIVA DRC, Antenna, LVS, and LPE decks from the documentation provided.

These decks can be found in the extracted PDK directory tree. The user needs the licenses for these tools to perform verification. When performing verification you have to provide the library name to the verification deck. Select the desired switches before starting the verification run. Refrain from working on the target layout being verified while the run is in progress.

### 18.1 DIVA DRC

Three separate DIVA DRC rules files have been provided with this PDK and are based on the design rules outlined in the Design Rule Section of this document.

The three files are:

1. **divaDRC.rul** - This rule file is for checking the design rules outlined in the Design Rule Section of this document.

The following switches are available in the divaDRC.rul file:

- **Skip\_Soft-Connect\_Checks** - Do not DRC flag well regions that are connected only through the well. This is valid for both nmos and pmos devices.

2. **divaANT.rul** - This rule file is for checking Antenna rules only (see the Antenna Rules Section of this document).

The following switches are available in the divaAntenna.rul file:

- **Check\_CO\_Antenna** - Perform Contact Antenna checks
- **Check\_M1\_Antenna** - Perform Metal 1 Antenna checks
- **Check\_M2\_Antenna** - Perform Metal 2 Antenna checks
- **Check\_M3\_Antenna** - Perform Metal 3 Antenna checks
- **Check\_M4\_Antenna** - Perform Metal 4 Antenna checks
- **Check\_M5\_Antenna** - Perform Metal 5 Antenna checks
- **Check\_M6\_Antenna** - Perform Metal 6 Antenna checks
- **Check\_Poly\_Antenna** - Perform Poly Antenna checks
- **Check\_V1\_Antenna** - Perform Via 1 Antenna checks

- Check\_V2\_Antenna - Perform Via 2 Antenna checks
- Check\_V3\_Antenna - Perform Via 3 Antenna checks
- Check\_V4\_Antenna - Perform Via 4 Antenna checks
- Check\_V5\_Antenna - Perform Via 5 Antenna checks
- Check\_V6\_Antenna - Perform Via 6 Antenna checks

**Note: One and only one switch must be chosen for Antenna Rule Checking**

- **divaDEN.rul** - This rule file is for checking Density rules only (see the Density Rules Section of this document).

No switches are available in the divaDEN.rul file.

## DIVA DRC RUN FORM

The screenshot shows the 'DRC' dialog box with the following settings:

- Checking Method:** ☒ flat, ☐ hierarchical, ☐ hier w/o optimization
- Checking Limit:** ☒ full, ☐ incremental, ☐ by area
- Coordinate:** [Yellow field] **Sel by Cursor**
- Switch Names:** [Text field] **Set Switches**
- Run-Specific Command File:** ☐ [Yellow field]
- Inclusion Limit:** [1000]
- Join Nets With Same Name:** ☐
- Echo Commands:** ☐
- Rules File:** [divaDRC.rul]
- Rules Library:** ☒ [gpdk]
- Machine:** ☒ local, ☐ remote **Machine:** [Text field]

## 18.2 DIVA EXTRACT

The DIVA EXTRACT rule decks contains the following switches:

**Skip\_Soft-Connect\_Checks** - Do not DRC flag well regions that are connected only through the well. This is valid for both nmos and pmos devices.

**PARASITIC\_C** - When switch is set parasitic capacitors will be generated in the extracted view. The standard Cadence flow is used to perform post-layout simulations.

**PARASITIC\_RC** - When switch is set parasitic resistors and capacitors will be generated in the extracted view. The standard Cadence flow is used to perform post-layout simulations.

**SKIP\_MERGE\_Cont\_VIA\_ARRAYS** - When switch is set all via arrays will NOT be merged into a single object. The default is to merge vias as it leads to smaller device counts.

**SCA** - When switch is set the substrate coupling analysis extraction will be performed. The SCA tool should be used for analysis of the results.

### DIVA EXTRACT FORM

**Extractor**

OK Cancel Defaults Apply Help

**Extract Method** ☒ flat ☐ macro cell ☐ full hier ☐ incremental hier

**Join Nets With Same Name** ☐ **Echo Commands** ☒

**Switch Names**  **Set Switches**

**Run-Specific Command File** ☐

**Inclusion Limit**

**View Names** **Extracted**  **Excell**

**Rules File**

**Rules Library** ☒

**Machine** ☒ local ☐ remote **Machine**

## 18.3 DIVA LVS

The parameters checked in LVS include:

- MOS Devices - type, length and combination of width, “m” factor
- Resistors - type, width, and value
- Capacitors - type, area and capacitance
- Bipolars - type and area
- Diodes - type and area
- Inductor - Number of turns, width, space, and inner radius

### DIVA LVS FORM

**LVS**

**Commands** Help 5

**Run Directory** LVS Browse

**Create Netlist** ☒ schematic ☒ extracted

**Library** circuitLib circuitLib

**Cell** circuit circuit

**View** schematic extracted

Browse Sel by Cursor Browse Sel by Cursor

**Rules File** divaLVS.rul Browse

**Rules Library** ☒ gpdk

**LVS Options** ☒ Rewiring ☐ Device Fixing  
☐ Create Cross Reference ☒ Terminals

**Correspondence File** ☐ lvs\_corr\_file Create

**Priority** 0 **Run** local

Run Output Error Display Monitor Info

Backannotate Parasitic Probe Build Analog Build Mixed

## 18.4 DIVA LPE/PRE

The PDK utilizes the interconnect coefficients listed in this document.

For Capacitance:

- Section - Interconnect Capacitance Table.
- Section - Coupling Capacitance Table.

For Resistance:

- Section - Sheet Resistance Table.

Note: The resistance extraction is written with a 10 square distribution setting.

## 19 Assura Decks

Cadence has developed the Assura DRC, LVS, and RCX rule files from the documentation provided.

These decks can be found in the extracted PDK directory tree in the directory:

- `assura_gpdk_tech`

The user needs the licenses for these tools to perform verification. When performing verification you have to provide the library name to the verification deck. Select the desired switches before starting the verification run. Refrain from working on the target layout being verified while the run is in progress.

### 19.1 Assura DRC

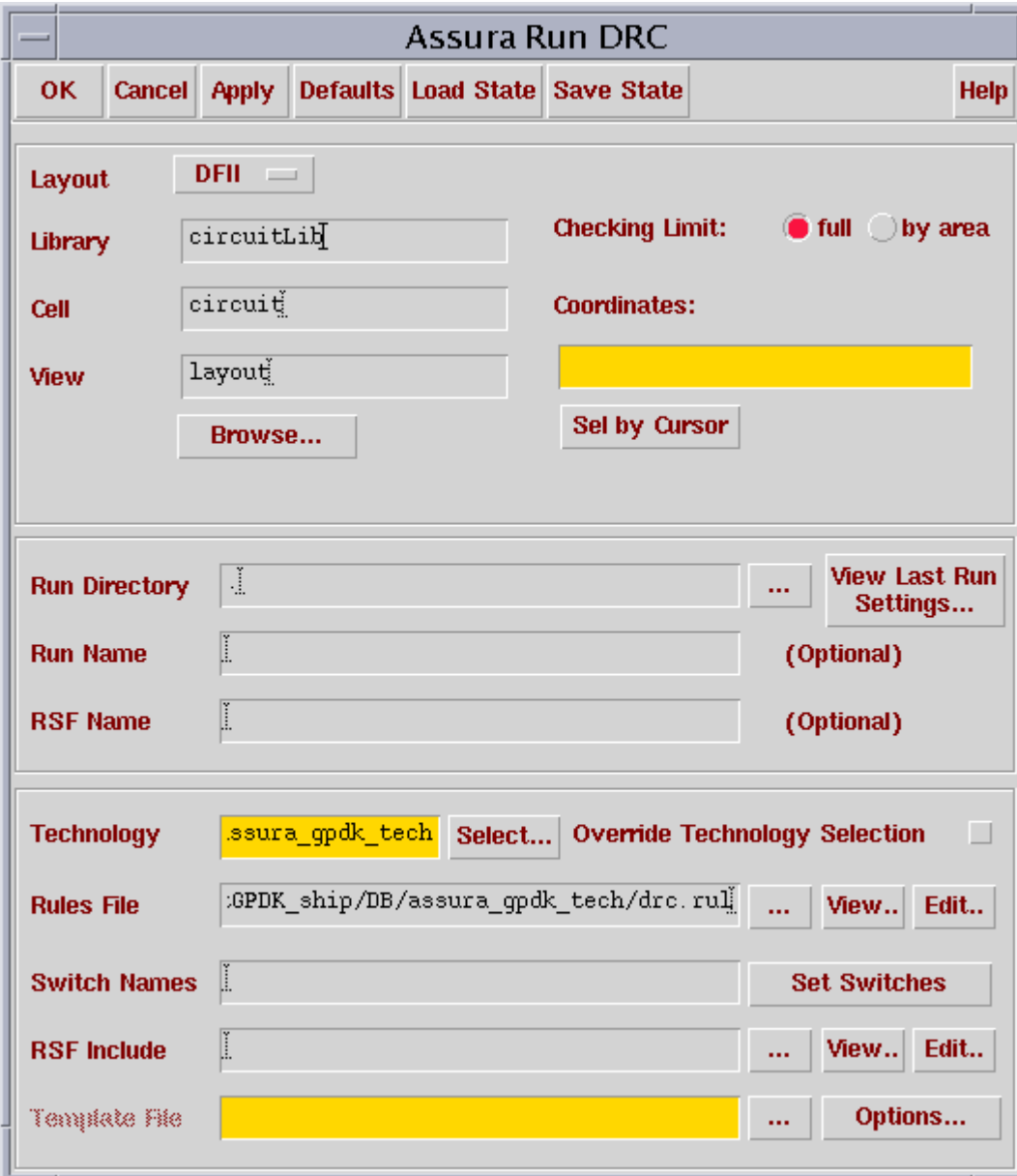
The Assura DRC file provided is named

- `drc.rul`

The following switches are available in the Assura DRC file:

- `Skip_Latch-Up_Checks` - Switch to turn off DRC checks for body tie distance to MOS devices.

## ASSURA DRC FORM



The image shows the 'Assura Run DRC' dialog box. It has a title bar with a minus sign. Below the title bar is a row of buttons: OK, Cancel, Apply, Defaults, Load State, Save State, and Help. The main area is divided into several sections. The top section has 'Layout' set to 'DFII'. Below it are 'Library' (circuitLib), 'Cell' (circuit), and 'View' (layout). To the right of these are 'Checking Limit' (radio buttons for 'full' and 'by area', with 'full' selected) and 'Coordinates' (a yellow rectangular area). Below 'View' is a 'Browse...' button. To the right of 'Coordinates' is a 'Sel by Cursor' button. The middle section has 'Run Directory' (a text box with a browse button), 'Run Name' (a text box with '(Optional)' next to it), and 'RSF Name' (a text box with '(Optional)' next to it). There is a 'View Last Run Settings...' button to the right of the 'Run Directory' field. The bottom section has 'Technology' (a text box with '.ssura\_gpd\_k\_tech' and a 'Select...' button), 'Rules File' (a text box with ':GPDK\_ship/DB/assura\_gpd\_k\_tech/drc.rules' and 'View..' and 'Edit..' buttons), 'Switch Names' (a text box with a 'Set Switches' button), 'RSF Include' (a text box with 'View..' and 'Edit..' buttons), and 'Template File' (a yellow rectangular area with an 'Options...' button). There is also an 'Override Technology Selection' checkbox.

**Assura Run DRC**

OK Cancel Apply Defaults Load State Save State Help

Layout: DFII

Library: circuitLib

Cell: circuit

View: layout

Checking Limit: ☒ full ☐ by area

Coordinates: [Yellow Area]

Browse... Sel by Cursor

Run Directory: [Text Box] ... View Last Run Settings...

Run Name: [Text Box] (Optional)

RSF Name: [Text Box] (Optional)

Technology: .ssura\_gpd\_k\_tech Select... Override Technology Selection ☐

Rules File: :GPDK\_ship/DB/assura\_gpd\_k\_tech/drc.rules ... View.. Edit..

Switch Names: [Text Box] Set Switches

RSF Include: [Text Box] ... View.. Edit..

Template File: [Yellow Area] ... Options...

## 19.2 Assura LVS

The Assura LVS files provided are located in the `gpdtech` directory and named

- `extract.rul`
- `compare.rul`

The following switches are available in the Assura extract file:

- `Skip_Soft-Connect_Checks` - Select the switch to turn on the creation of markers for connections that are made through nwell or substrate

## ASSURA LVS FORM

Assura Run LVS			
<input type="button" value="OK"/> <input type="button" value="Cancel"/> <input type="button" value="Apply"/> <input type="button" value="Defaults"/> <input type="button" value="Load State"/> <input type="button" value="Save State"/> <input type="button" value="Help"/>			
<b>Layout</b> <input type="button" value="DFII"/>		<b>Schematic</b> <input type="button" value="DFII"/>	
<input type="checkbox"/> Use Existing Extracted Netlist		<input type="checkbox"/> Use Existing Netlist	
<b>Library</b> <input type="text" value="circuitLib"/>	<b>Library</b> <input type="text" value="circuitLib"/>		
<b>Cell</b> <input type="text" value="circuit"/>	<b>Cell</b> <input type="text" value="circuit"/>		
<b>View</b> <input type="text" value="layout"/>	<b>View Name</b> <input type="text" value="schematic"/>		
<input type="button" value="Browse..."/>		<input type="button" value="Browse..."/>	
<hr/>			
<b>Run Directory</b> <input type="text"/> ...		<input type="button" value="View Last Run Settings..."/>	
<b>Run Name</b> <input type="text"/> (Optional)			
<b>RSF Name</b> <input type="text"/> (Optional)			
<hr/>			
<b>Technology</b> <input type="text" value=".ssura_gpd_k_tech"/> <input type="button" value="Select..."/>		<b>Override Technology Selection</b> <input type="checkbox"/>	
<b>Extract Rules</b> <input type="text" value="stGPDK_ship/DB/assura_gpd_k_tech/extract.rul"/> ...		<input type="button" value="View.."/> <input type="button" value="Edit..."/>	
<b>Switch Names</b> <input type="text"/>		<input type="button" value="Set Switches"/>	
<b>Compare Rules</b> <input type="text" value="stGPDK_ship/DB/assura_gpd_k_tech/compare.rul"/> ...		<input type="button" value="View.."/> <input type="button" value="Edit..."/>	
<b>Binding File(s)</b> <input type="text"/> ...		<input type="button" value="View.."/> <input type="button" value="Edit..."/>	
<b>RSF Include</b> <input type="text"/> ...		<input type="button" value="View.."/> <input type="button" value="Edit.."/>	
<b>Template File</b> <input type="text"/> ...		<input type="button" value="Options..."/>	
<hr/>			
<b>View list</b> <input type="text" value="uLvs schematic symbol"/>		<b>Stop list</b> <input type="text" value="auLvs"/>	
<input type="checkbox"/> Device Information File <input type="text"/> ...		<input type="button" value="View.."/> <input type="button" value="Edit..."/>	
<input type="checkbox"/> Ignore namePrefix from CDF		<b>avSimName</b> <input type="text"/>	

## 19.3 Assura RCX

The Assura RCX files provided are located in the following directory

- `assura_gpdtech` - Directory where Assura RCX files are provided

Please consult the Assura RCX User's manual for available RCX options.

### ASSURA RCX FORM

**Assura Parasitic Extraction**

OK Cancel Defaults Load State Save State Help

Environment	Value
Design (dfII)	circuitLib circuit layout
Technology	assura_gpdtech
Run Directory	/home/johnag/projects/testGPDK_ship/DB

Run Name:

Nets: ☐ From File ☒ Layout Names ☐ Schematic Names

Type:  Edit...

Extract: ☒ Capacitance ☒ Resistance  
☒ Decoupled ☐ Coupled

Ref Node:

Mult Factor:

Output: ☐ Spice File ☐ DSPF File ☒ Extracted View

Library:  Cell:  View:

Option	Value
Extract Src/Drn Res	no
Max Fracture Length	infinite

Options...

## 20 DEVICE SPECIFICATIONS

### 20.1 Data Source Table

Foundry Documents			Version	Date
Layout Design	GPDK Reference Manual		1.8	30-Sep-02
Simulation Models	GPDK Generic Process Models		1.8	30-Sep-02
Electrical Parameters	GPDK Reference Manual		1.8	30-Sep-02
Device Formation	GPDK Reference Manual		1.8	30-Sep-02
Layer Definition	GPDK Reference Manual			30-Sep-02
Foundry	None			

## 20.2 Model and Layout Source

Device	Description	Spectre Model	GDS or DFII Sample Layout	Fixed Layout or Variable Layout (Pcell)
<b>As of Sep 29, 2002</b>				
<b>Mos</b>				
nmos	4 terminal nMOS	Y	Y	Pcell
pmos	4 terminal pMOS	Y	Y	Pcell
nmos3	3 terminal nMOS (with bn property)	Y	Y	Pcell
pmos3	3 terminal pMOS (with bn property)	Y	Y	Pcell
<b>Resistor</b>				
nplusres	n+ diffusion resistor	Y	Y	Pcell
polyres	poly resistor	Y	Y	Pcell
<b>Capacitor</b>				
nmoscap	nMOS cap ( nMOS with w/ cap symbol)	Y	Y	Pcell
mimcap	Square Metal-Insulator-Metal Capacitor	Y	Y	Pcell
<b>Diode</b>				
ndio	N+/PW diode	Y	Y	Pcell
pdio	P+/NW diode	Y	Y	Pcell
<b>Inductor</b>				
ind	spiral turn inductor	Y	Y	Pcell
<b>Bjt</b>				
vpnp	Vertical PNP	Y	Y	Fixed
pnp	BIPOLAR PNP	Y	Y	Pcell
nnp	Bipolar NPN	Y	Y	Pcell

## 20.3 MOS FORMAL PARAMETERS

DEVICE		l (gate length in microns)			
		min	Value got from	max	Value got from
nmos		0.18	GPDK PDK	20	PDK Standard
pmos		0.18	GPDK PDK	20	PDK Standard
nmos3		0.18	GPDK PDK	20	PDK Standard
pmos3		0.18	GPDK PDK	20	PDK Standard
DEVICE		w (gate width in microns)			
		min	Value got from	max	Value got from
nmos		0.42	GPDK PDK	100	PDK Standard
pmos		0.42	GPDK PDK	100	PDK Standard
nmos3		0.42	GPDK PDK	100	PDK Standard
pmos3		0.42	GPDK PDK	100	PDK Standard
DEVICE		Nf (Number of Fingers)			
		min	Value got from	max	Value got from
nmos		1	GPDK PDK	100	PDK Standard
pmos		1	GPDK PDK	100	PDK Standard
nmos3		1	GPDK PDK	100	PDK Standard
pmos3		1	GPDK PDK	100	PDK Standard

## 20.4 RESISTOR FORMAL PARAMETERS

DEVICE		r (resistance in ohms)			
		min	Value got from	max	Value got from
nplusres		1.5	GPDK PDK		PDK Standard
polyres		0.135	GPDK PDK		PDK Standard
DEVICE		w (resistor width in microns)			
		min	Value got from	max	Value got from
nplusres		0.6	GPDK PDK	100	PDK Standard
polyres		0.6	GPDK PDK	50	PDK Standard

## 20.5 CAPACITOR FORMAL PARAMETERS

DEVICE		c (capacitance in farads)			
		min	Value got from	max	Value got from
mimcap		17.6f	GPDK PDK	912f	GPDK PDK
nmoscap		.12f	GPDK PDK	444f	PDK Standard
DEVICE		w (capacitor width in microns)			
		min	Value got from	max	Value got from
mimcap		4	GPDK PDK	30	GPDK PDK
nmoscap		0.6	GPDK PDK	100	PDK Standard
DEVICE		l (capacitor width in microns)			
		min	Value got from	max	Value got from
mimcap		4	GPDK PDK	30	GPDK PDK
nmoscap		0.6	GPDK PDK	20	PDK Standard
DEVICE		fingers (number of capacitor fingers)			
		min	Value got from	max	Value got from
nmoscap		1	GPDK PDK	50	PDK Standard

## 20.6 INDUCTOR FORMAL PARAMETERS

DEVICE		ind (Inductance in Henrys)			
		min	Value got from	max	Value got from
inductor		2.09E-10	GPDK PDK	4.43E-08	GPDK PDK
DEVICE		nr (inductor turns)			
		min	Value got from	max	Value got from
inductor		1.5	GPDK PDK	9.5	GPDK PDK
DEVICE		rad (inductor inner radius in microns)			
		min	Value got from	max	Value got from
inductor		20	GPDK PDK	100	GPDK PDK
DEVICE		space (inductor metal space in microns)			
		min	Value got from	max	Value got from
inductor		2	GPDK PDK	10	GPDK PDK
DEVICE		width (inductor metal width in microns)			
		min	Value got from	max	Value got from
inductor		5	GPDK PDK	20	GPDK PDK

## 20.7 BIPOLAR FORMAL PARAMETERS

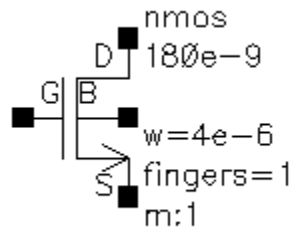
DEVICE		emitter size ( fixed emitter size in microns)			
		min	Value got from	max	Value got from
vpnp		1.3x.13	GPDK PDK	1.3x1.3	GPDK PDK
nnp					
npn					
DEVICE		w (variable emitter width in microns)			
		min	Value got from	max	Value got from
vpnp					
nnp		0.6	GPDK PDK	10	GPDK PDK
npn		0.6	GPDK PDK	10	GPDK PDK

## 20.8 DIODES FORMAL PARAMETERS

DEVICE		l (diode length in microns)			
		min	Value got from	max	Value got from
ndio		0.6	GPDK PDK	20u	GPDK PDK
pdio		0.6	GPDK PDK	20u	GPDK PDK
DEVICE		w (diode width in microns)			
		min	Value got from	max	Value got from
ndio		0.6	GPDK PDK	20u	GPDK PDK
pdio		0.6	GPDK PDK	20u	GPDK PDK

## 21 DEVICE DATASHEETS

### 21.1 nmos - Nmos Transistor



#### Spectre Netlist

**Spectre Model Name = "nmos1"**

```
MN1 (D G S B) nmos1 w=4u l=180.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \
      pd=5.2u m=(1)*(1)
```

#### DIVA LVS Netlist

**DIVA Device Name = "nmos"**

```
; nmos Instance /MN1 = auLvs device M1
d nmos D G S B (p D S)
i 1 nmos D G S B " m 1.0 l 180e-9 w 4e-6 "
```

#### CDL Netlist

**CDL Device Name = "NR"**

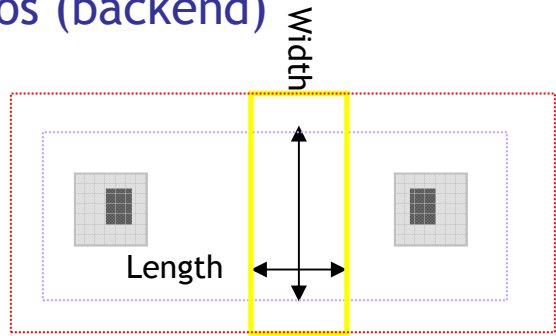
```
MMN1 D G S B N W=4u L=180.0n M=1.0
```






#### Assura Netlist

**Assura auLvs Device Name = "nmos"**

```
c nmos MOS DRAIN B GATE B SOURCE B SUBSTRATE B ;;
* 4 pins
* 4 nets
* 0 instances
i MN1 nmos D G S B ; m 1 l 1.8e-07 w 4e-06 ;
```

21.2 nmos (backend)



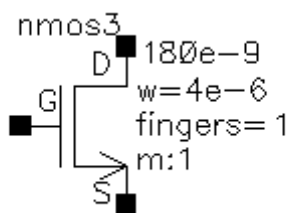
Device Layers	
Layer	Color and Fill
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	Oxide AND Nimp CONTAINS Poly
G	Poly
D	Oxide AND Nimp NOT Poly
S	Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	Calculation
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

\* S and D are PERMUTABLE

## 21.3 nmos3 - Nmos Transistor



\* Term B is an inherited property

### Spectre Netlist

**Spectre Model Name = "nmos1"**

```
MN1 (D G S B) nmos1 w=4u l=180.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \
      pd=5.2u m=(1)*(1)
```

### DIVA LVS Netlist

**DIVA Device Name = "nmos"**

```
; nmos Instance /MN1 = auLvs device M1
d nmos D G S B (p D S)
i 1 nmos D G S B " m 1.0 l 180e-9 w 4e-6 "
```

### CDL Netlist

**CDL Device Name = "N"**

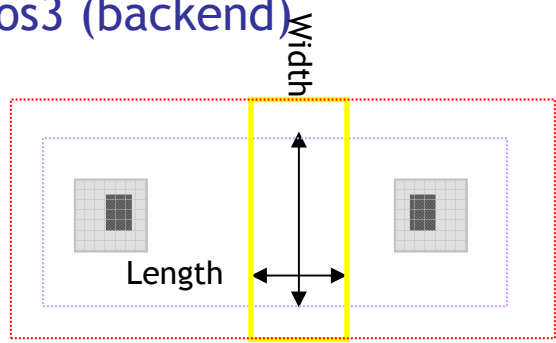
```
MMN1 D G S B N W=4u L=180.0n M=1.0
```

### Assura Netlist

**Assura auLvs Device Name = "nmos"**

```
c nmos MOS DRAIN B GATE B SOURCE B SUBSTRATE B ;;
* 4 pins
* 4 nets
* 0 instances
i MN1 nmos D G S B ; m 1 l 1.8e-07 w 4e-06 ;
```

21.4 nmos3 (backend)



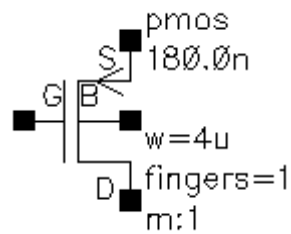
Device Layers	
Layer	Color and Fill
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	Oxide AND Nimp CONTAINS Poly
G	Poly
D	Oxide AND Nimp NOT Poly
S	Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	Calculation
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

\* S and D are PERMUTABLE

## 21.5 pmos - Pmos Transistor



### Spectre Netlist

**Spectre Model Name = "pmos1"**

```
MP1 (D G S B) pmos1 w=4u l=180.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \
      pd=5.2u m=(1)*(1)
```

### DIVA LVS Netlist

**DIVA Device Name = "pmos"**

```
; pmos Instance /MP1 = auLvs device M1
d pmos D G S B (p D S)
i 1 pmos D G S B " m 1.0 l 180e-9 w 4e-6 "
```

### CDL Netlist

**CDL Device Name = "P"**

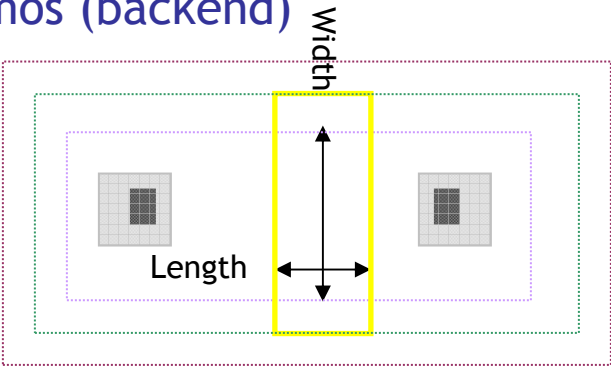
```
MMP1 D G S B P W=4u L=180.0n M=1.0
```

### Assura Netlist

**Assura auLvs Device Name = "pmos"**

```
c pmos MOS DRAIN B GATE B SOURCE B SUBSTRATE B ;;
* 4 pins
* 4 nets
* 0 instances
i MP1 pmos D G S B ; m 1 l 1.8e-07 w 4e-06 ;
```

21.6 pmos (backend)



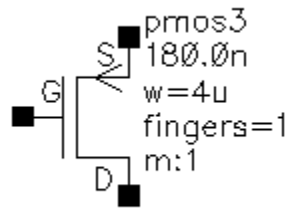
Device Layers	
Layer	Color and Fill
Nwell	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	Nwell AND Oxide AND Pimp CONTAINS Poly
G	Poly
D	Nwell AND Oxide AND Pimp NOT Poly
S	Nwell AND Oxide AND Pimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	Calculation
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

\* S and D are PERMUTABLE

## 21.7 pmos3 - Pmos Transistor



\* Term B is an inherited property

### Spectre Netlist

**Spectre Model Name = "pmos1"**

```
MP1 (D G S B) pmos1 w=4u l=180.0n as=2.4e-12 ad=2.4e-12 ps=5.2u \
      pd=5.2u m=(1)*(1)
```

### DIVA LVS Netlist

**DIVA Device Name = "pmos"**

```
; pmos Instance /MP1 = auLvs device M1
d pmos D G S B (p D S)
i 1 pmos D G S B " m 1.0 l 180e-9 w 4e-6 "
```

### CDL Netlist

**CDL Device Name = "P"**

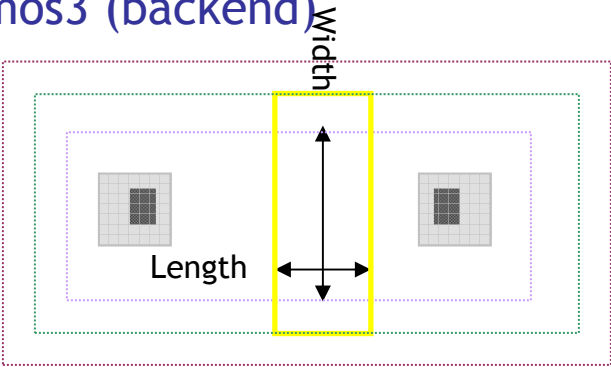
```
MMP1 D G S B P W=4u L=180.0n M=1.0
```







### Assura Netlist

**Assura auLvs Device Name = "pmos"**

```
c pmos MOS DRAIN B GATE B SOURCE B SUBSTRATE B ;;
* 4 pins
* 4 nets
* 0 instances
i MP1 pmos D G S B ; m 1 l 1.8e-07 w 4e-06 ;
```

21.8 pmos3 (backend)



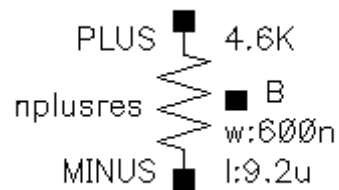
Device Layers	
Layer	Color and Fill
Nwell	
Oxide	
Pimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	Nwell AND Oxide AND Pimp CONTAINS Poly
G	Poly
D	Nwell AND Oxide AND Pimp NOT Poly
S	Nwell AND Oxide AND Pimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	Calculation
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

\* S and D are PERMUTABLE

## 21.9 nplusres - Nplus Resistor



### Spectre Netlist

**Spectre Model Name = "nplusres"**

R1 (PLUS MINUS B) nplusres r=4.6K Area=6e-12 Perim=2.12e-05

### DIVA LVS Netlist

**DIVA Device Name = "nplusres"**

; nplusres Instance /R1 = auLvs device R1

d nplusres PLUS MINUS B (p PLUS MINUS)

i 1 nplusres PLUS MINUS B " r 4.6e3 w 600e-9 "

### CDL Netlist

**CDL Device Name = "NR"**

RR1 PLUS MINUS 4.6K \$[NR]

### Assura Netlist

**Assura auLvs Device Name = "nplusres"**

c nplusres RES IN B OUT B SUBSTRATE B ;;

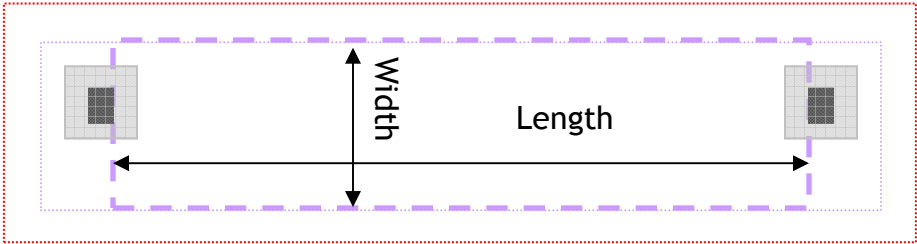
\* 3 pins





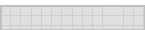
\* 3 nets

\* 0 instances

i R1 nplusres PLUS MINUS ; r 4600 w 6e-07 ;

## 21.10 nplusres (backend)



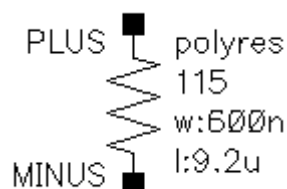
Device Layers	
Layer	Color and Fill
Oxide	
Nimp	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	Oxide AND Nimp AND Resdum
PLUS	Oxide NOT Resdum
MINUS	Oxide NOT Resdum
B	Substrate

LVS Comparison	
Parameter	Calculation
Length	Contact to Contact (illustrated above)
Width	Oxide Width (illustrated above)
Resistance	sheet resistance * Length / Width

\* PLUS and MINUS are PERMUTABLE

## 21.11 polyres - Poly Resistor



### Spectre Netlist

**Spectre Model Name = “resistor”**

R1 (PLUS MINUS) resistor r=115

### DIVA LVS Netlist

**DIVA Device Name = “polyres”**

; polyres Instance /R1 = auLvs device R1

d polyres PLUS MINUS (p PLUS MINUS)

i 1 polyres PLUS MINUS " r 115 w 600e-9 "

### CDL Netlist

**CDL Device Name = “PR”**

RR1 PLUS MINUS 115 \$[PR]

### Assura Netlist

**Assura auLvs Device Name = “polyres”**

c polyres RES IN B OUT B ;;

\* 2 pins




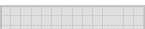
\* 2 nets

\* 0 instances

i R1 polyres PLUS MINUS ; r 115 w 6e-07 ;

## 21.12 polyres (backend)



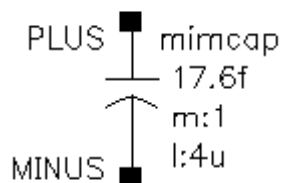
Device Layers	
Layer	Color and Fill
Poly	
Resdum (Marker Layer)	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	Poly AND Resdum
PLUS	Poly NOT Resdum
MINUS	Poly NOT Resdum

LVS Comparison	
Parameter	Calculation
Length	Contact to Contact (illustrated above)
Width	Poly Width (illustrated above)
Resistance	sheet resistance * Length / Width

\* PLUS and MINUS are PERMUTABLE

## 21.13 mimcap - Metal to Metal Capacitor



### Spectre Netlist

**Spectre Model Name = “capacitor”**

C1 (PLUS MINUS) capacitor c=17.6f m=1

### DIVA LVS Netlist

**DIVA Device Name = “mimcap”**

; mimcap Instance /C1 = auLvs device C1

d mimcap PLUS MINUS

i 1 mimcap PLUS MINUS " c 1.76e-14 m 1.0 "

### CDL Netlist

**CDL Device Name = “MC”**

CC1 PLUS MINUS 17.6f \${MC}

### Assura Netlist

**Assura auLvs Device Name = “mimcap”**

c mimcap CAP IN B OUT B ;;

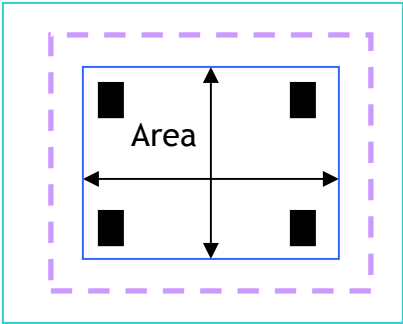
\* 2 pins





\* 2 nets

\* 0 instances

i C1 mimcap PLUS MINUS ; c 1.76e-14 m 1 ;

## 21.14 mimcap (backend)

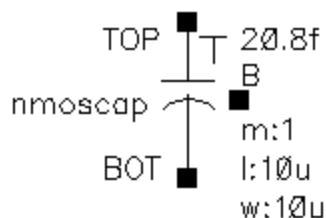


Device Layers	
Layer	Color and Fill
Metal 2	
CapMetal	
Via2	
Metal3	

Device Derivation	
Device	Layer Derivation
Recognition	CapMetal AND Metal2
PLUS	CapMetal
MINUS	Metal2 UNDER CapMetal

LVS Comparison	
Parameter	Calculation
Area	Area of CapMetal (illustrated above)
Capacitance	$C_{perA} * Area$

## 21.15 nmoscap - Nmos Transistor Configured as Cap



### Spectre Netlist

**Spectre Model Name = "nmos1"**

```
C1 (TOP BOT TOP B) nmos1 w=10u l=10u as=6e-12 ad=6e-12 ps=11.2u \
    pd=11.2u m=(1)*(1)
```

### DIVA LVS Netlist

**DIVA Device Name = "nmoscap"**

```
; nmoscap Instance /C1 = auLvs device C1
d nmoscap TOP BOT B
i 1 nmoscap TOP BOT B " m 1.0 l 10e-6 w 10e-6 "
```

### CDL Netlist

**CDL Device Name = "N"**

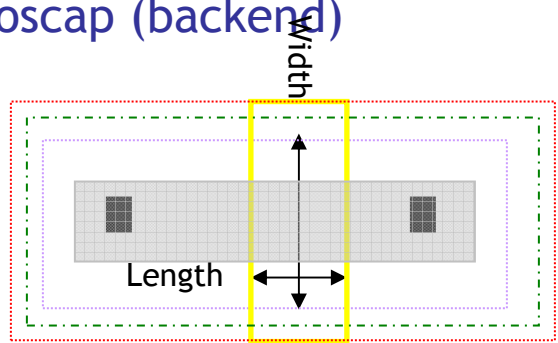
```
MC1 TOP BOT TOP B N W=10u L=10u M=1
```







### Assura Netlist

**Assura auLvs Device Name = "nmoscap"**

```
c nmoscap CAP POS B MINUS B SUBSTRATE I ;;
* 3 pins
* 3 nets
* 0 instances
i C1 nmoscap TOP BOT B ; m 1 l 1e-05 w 1e-05 ;
```

21.16 nmoscap (backend)



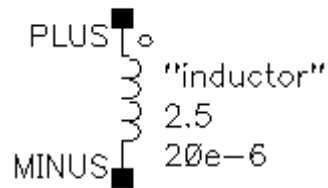
Device Layers	
Layer	Color and Fill
Capdum	
Oxide	
Nimp	
Poly	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	Capdum AND Oxide AND Nimp CONTAINS Poly
TOP	Poly
BOT	CAPDUM AND Oxide AND Nimp NOT Poly
B	Substrate

LVS Comparison	
Parameter	Calculation
Length	Poly intersecting Oxide (illustrated above)
Width	Poly inside Oxide (illustrated above)

\* Nmos Source and Drain are Shorted Together

## 21.17 inductor - Metal 3 Inductor



### Spectre Netlist

**Spectre Model Name = "inductor"**

L1 (PLUS MINUS) inductor l=5.95156e-10

### DIVA LVS Netlist

**DIVA Device Name = ind"**

; inductor Instance /L1 = auLvs device L1

d inductor PLUS MINUS

i 1 inductor PLUS MINUS " ind 5,95156e-10 "

### CDL Netlist

**CDL Black Box Name = "inductor"**

QL1 PLUS MINUS inductor

### Assura Netlist

**Assura auLvs Device Name = "inductor"**

c inductor Generic PLUS B MINUS B ;;

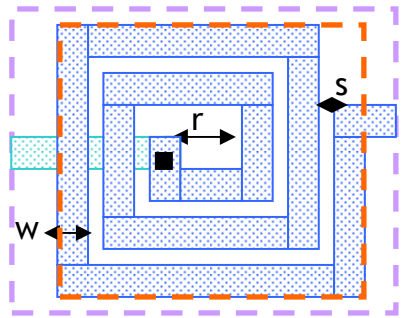
\* 2 pins

\* 2 nets

\* 0 instances

i L1 inductor PLUS MINUS ; ind 5.95156e-10;

21.18 inductor (backend)

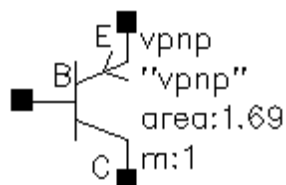


Device Layers	
Layer	Color and Fill
INDdummy	
IND2dummy	
Metal 2	
Via2	
Metal3	

Device Derivation	
Device	Layer Derivation
Recognition	INDdummy AND IND2dummy AND Metal3
PLUS	Metal3 BUTTING IND2dummy
MINUS	Metal2 BUTTING IND2dummy

LVS Comparison	
Parameter	Calculation
r	Inner radius (illustrated above)
s	Metal3 space (illustrated above)
w	Metal3 width (illustrated above)
nr	Number of Metal3 turns
Inductance	$(k1 = 2.34 \quad k2 = 2.75 \quad u0 = 4e-7 * 3.14)$ $Ind = (k1 * u0 * nr * nr * (.5 * ((2 * r + (nr + .5) * w + (nr - .5) * s) + (2 * r)))) / (1 + k2 * (((2 * r + (nr + .5) * w + (nr - .5) * s) - (2 * r)) / ((2 * r + (nr + .5) * w + (nr - .5) * s) + (2 * r))))$

## 21.19 vpnp - Vertical Bipolar PNP



### Spectre Netlist

**Spectre Model Name = "vpnp"**

Q0 ( C B E ) vpnp area=1 m=1

### DIVA LVS Netlist

**DIVA Device Name = "vpnp"**

; vpnp Instance /Q0 = auLvs device Q0

d vpnp C B E

i 0 vpnp C B E " area 1.69 m 1.0 "

### CDL Netlist

**CDL Device Name = "PV"**

QQ0 C B E PV M=1 \$EA=1.69

### Assura Netlist

**Assura auLvs Device Name = "vpnp"**

c vpnp BJT COLLECTOR B BASE B EMITTER B ;;

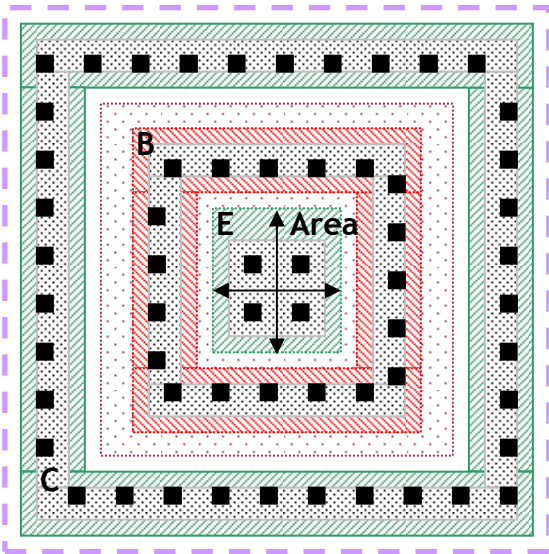
\* 3 pins







\* 3 nets

\* 0 instances

i Q0 vpnp C B E; area 1.69 m 1 ;

21.20 vnpn (backend)

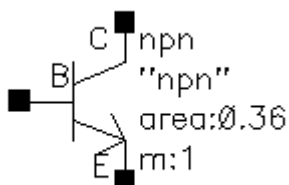


Device Layers	
Layer	Color and Fill
BJTdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal3	

Device Derivation	
Device	Layer Derivation
Recognition	BJTdummy contains Nimp AND Pimp
E	BJTDummy AND Pimp And Oxide AND Nwell
B	BJTDummy AND Nimp And Oxide AND Nwell
C	BJTDummy AND Pimp And Oxide ANDNOT Nwell

LVS Comparison	
Parameter	Calculation
Area	Area of Emitter (illustrated above)

## 21.21 npn - Bipolar npn



### Spectre Netlist

**Spectre Model Name = "npn"**

Q1 ( C B E ) npn area=1 m=1

### DIVA LVS Netlist

**DIVA Device Name = "npn"**

; npn Instance /Q1 = auLvs device Q1

d npn C B E

i 1 npn C B E " area 360e-3 m 1.0 "

### CDL Netlist

**CDL Device Name = "NP"**

QQ1 C B E NP \$EA=0.36

### Assura Netlist

**Assura auLvs Device Name = "npn"**

c npn BJT COLLECTOR B BASE B EMITTER B ;;

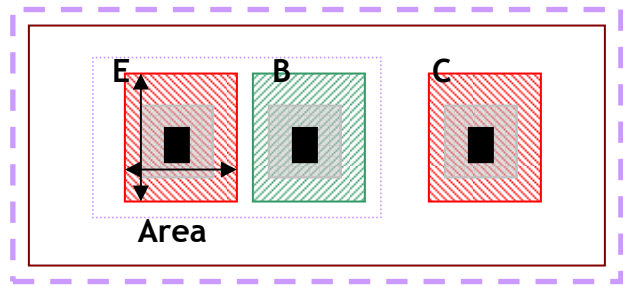
\* 3 pins



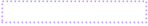



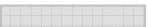
\* 3 nets

\* 0 instances

i Q1 npn C B E ; area 0.36 m 1 ;

21.22 npn (backend)

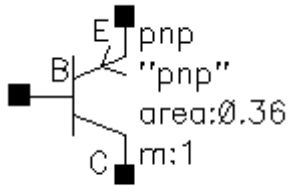


Device Layers	
Layer	Color and Fill
NPNdummy	
Nburied	
Pwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	NPNdummy AND Nimp AND Pwell
E	NPNdummy AND Nburied AND Nimp AND Pwell
B	NPNdummy AND Nburied AND Pimp AND Pwell
C	NPNdummy AND Nburied AND Nimp ANDNOT Pwell

LVS Comparison	
Parameter	Calculation
area	Area of Emitter (illustrated above)

## 21.23 pnp - Bipolar pnp



### Spectre Netlist

**Spectre Model Name = "pnp"**

Q1 ( C B E ) pnp area=1 m=1

### DIVA LVS Netlist

**DIVA Device Name = "pnp"**

; pnp Instance /Q1 = auLvs device Q1

d pnp C B E

i 1 pnp C B E " area 360e-3 m 1.0 "

### CDL Netlist

**CDL Device Name = "PN"**

QQ1 C B E PN \$EA=0.36

### Assura Netlist

**Assura auLvs Device Name = "pnp"**

c pnp BJT COLLECTOR B BASE B EMITTER B ;;

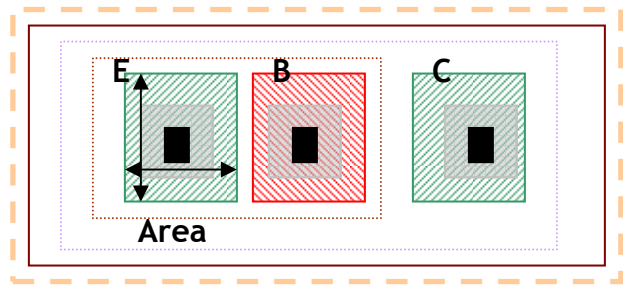
\* 3 pins









\* 3 nets

\* 0 instances

i Q1 pnp C B E ; area 0.36 m 1 ;

21.24 pnp (backend)

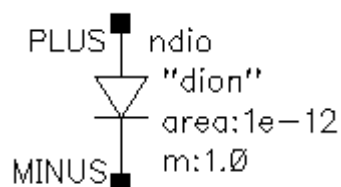


Device Layers	
Layer	Color and Fill
PNPdummy	
Nburied	
Nwell	
Pwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	PNPdummy AND Pimp AND Pwell
E	PNPdummy AND Nburied AND Pimp AND Nwell
B	PNPdummy AND Nburied AND Nimp AND Nwell
C	PNPdummy AND Nburied AND Pimp ANDNOT Nwell

LVS Comparison	
Parameter	Calculation
area	Area of Emitter (illustrated above)

## 21.25 ndio - N type Diode



### Spectre Netlist

**Spectre Model Name = "dion"**

D0 ( PLUS MINUS ) dion area=1e-12 m=1

### DIVA LVS Netlist

**DIVA Device Name = "ndio"**

; ndio Instance /D0 = auLvs device D0

d ndio PLUS MINUS

i 0 ndio PLUS MINUS " area 1e-12 m 1.0 "

### CDL Netlist

**CDL Device Name = "DN"**

DD0 PLUS MINUS DN 1e-12

### Assura Netlist

**Assura auLvs Device Name = "ndio"**

c ndio DIO POS B MINUS B ;;

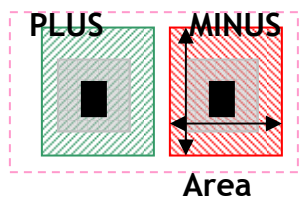
\* 2 pins




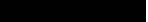
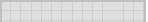
\* 2 nets

\* 0 instances

i D0 ndio PLUS MINUS ; area 1e-12 m 1 ;

21.26 ndio (backend)



Device Layers	
Layer	Color and Fill
DIOdummy	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

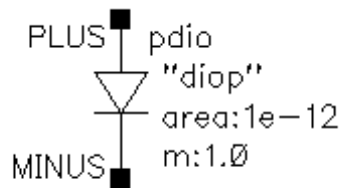
  

Device Derivation	
Device	Layer Derivation
Recognition	DIOdummy AND Nimp
PLUS	DIOdummy AND Pimp
MINUS	DIOdummy AND Nimp

LVS Comparison	
Parameter	Calculation
area	Area of MINUS (illustrated above)

## 21.27 pdio - N type Diode



### Spectre Netlist

**Spectre Model Name = "diop"**

D0 ( PLUS MINUS ) diop area=1e-12 m=1

### DIVA LVS Netlist

**DIVA Device Name = "pdio"**

; pdio Instance /D0 = auLvs device D0

d pdio PLUS MINUS

i 0 pdio PLUS MINUS " area 1e-12 m 1.0 "

### CDL Netlist

**CDL Device Name = "DP"**

DD0 PLUS MINUS DP 1e-12

### Assura Netlist

**Assura auLvs Device Name = "pdio"**

c pdio DIO POS B MINUS B ;;

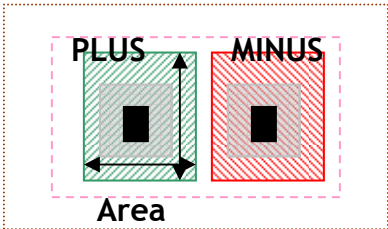
\* 2 pins





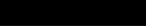

\* 2 nets

\* 0 instances

i D0 pdio PLUS MINUS ; area 1e-12 m 1 ;

21.28 pdio (backend)



Device Layers	
Layer	Color and Fill
DIOdummy	
Nwell	
Nimp / Oxide	
Pimp / Oxide	
Cont	
Metal1	

Device Derivation	
Device	Layer Derivation
Recognition	DIOdummy AND Pimp AND Nwell
PLUS	DIOdummy AND Pimp AND Nwell
MINUS	DIOdummy AND Nimp AND Nwell

LVS Comparison	
Parameter	Calculation
area	Area of PLUS (illustrated above)

## 22 DESIGN RULES

### 22.1 Layout Guidelines

- 0A Minimum NBURIED width 1.0um
- 0B Minimum NBURIED space 1.0um
- 1A Minimum NWELL width 1.0um
- 1B Minimum NWELL space 1.0um
- 1C Minimum NBURIED enclosure of NWELL 0.3um
- 1D Minimum PWELL width 1.0um
- 1E Minimum PWELL space 1.0um
- 1F Minimum NBURIED enclosure of PWELL 0.3um
- 2A Minimum OXIDE width 0.4um
- 2B Minimum OXIDE space 0.3um
- 2C Minimum NWELL enclosure of OXIDE 0.5um
- 2D Minimum NWELL to OXIDE space 0.5um
- 3A Minimum NIMP width 0.4um
- 3B Minimum NIMP space 0.4um
- 3C Minimum NIMP enclosure of OXIDE 0.2um
- 3D Minimum NBURIED enclosure of NIMP 0.6um
- 4A Minimum PIMP width 0.4um
- 4B Minimum PIMP space 0.4um
- 4C Minimum PIMP enclosure of OXIDE 0.2um
- 4D Minimum NBURIED enclosure of PIMP 0.6um
- 4E PIMP and NIMP cannot overlap
- 5A Minimum POLY width 0.18um
- 5B Minimum POLY space 0.3um
- 5C Minimum POLY extension beyond OXIDE (poly endcap) 0.2um
- 5D Minimum OXIDE extension beyond gate POLY 0.4um
- 5E Minimum Poly to OXIDE spacing 0.2um
- 6A Minimum and maximum width of CONT 0.2um
- 6B Minimum CONT space 0.2um
- 6C Minimum OXIDE enclosure of CONT 0.2um

- 6D Minimum POLY enclosure of CONT 0.2um
- 6E Minimum POLY to CONT space 0.2um
- 6F Minimum NIMP enclosure of CONT 0.2um
- 6G Minimum PIMP enclosure of CONT 0.2um
- 6H Minimum CONT to Oxide space 0.2um
- 7A Minimum METAL1 width 0.3um
- 7B Minimum METAL1 space 0.3um
- 7C Minimum METAL1 enclosure of CONT 0.1um
- 8A Minimum and maximum width of VIA1 0.2um
- 8B Minimum VIA1 space 0.3um
- 8C Minimum METAL1 enclosure of VIA1 0.1um
- 9A Minimum METAL2 width 0.3um
- 9B Minimum METAL2 space 0.3um
- 9C Minimum METAL2 enclosure of VIA1 0.1um
- 10A Minimum and maximum width of VIA2 0.2um
- 10B Minimum VIA2 space 0.3um
- 10C Minimum METAL2 enclosure of VIA2 0.1um
- 11A Minimum METAL3 width 0.3um
- 11B Minimum METAL3 space 0.3um
- 11C Minimum METAL3 enclosure of VIA2 0.1um
- 11D Minimum METAL3 enclosure of VIA2 for metal capacitor 0.1um
- 12A Minimum CAPMETAL width 0.5um
- 12B Minimum METAL2 enclosure of CAPMETAL 0.4um
- 12C Minimum CAPMETAL enclosure of VIA2 0.2um
- 12D Minimum CAPMETAL enclosure of METAL3 0.3um
- 13A Maximum distance from a source/drain OXIDE  
region to the nearest well tie 10um
- 14A Minimum and maximum width of VIA3 0.2um
- 14B Minimum VIA3 space 0.3um
- 14C Minimum METAL3 enclosure of VIA3 0.1um
- 15A Minimum METAL4 width 0.3um
- 15B Minimum METAL4 space 0.3um

- 15C Minimum METAL4 enclosure of VIA3 0.1um
- 16A Minimum and maximum width of VIA4 0.2um
- 16B Minimum VIA4 space 0.3um
- 16C Minimum METAL4 enclosure of VIA4 0.1um
- 17A Minimum METAL5 width 0.3um
- 17B Minimum METAL5 space 0.3um
- 17C Minimum METAL5 enclosure of VIA4 0.1um
- 18A Minimum and maximum width of VIA5 0.2um
- 18B Minimum VIA5 space 0.3um
- 18C Minimum METAL5 enclosure of VIA5 0.1um
- 19A Minimum METAL6 width 0.3um
- 19B Minimum METAL6 space 0.3um
- 19C Minimum METAL6 enclosure of VIA5 0.1um
- 20A Minimum BONDPAD width 45.0um
- 20B Minimum BONDPAD space 10.0um
- 20C Minimum and Maximum METAL1 enclosure BONDPAD 3.0um
- 20D Minimum and Maximum METAL2 enclosure BONDPAD 3.0um
- 20E Minimum and Maximum METAL3 enclosure BONDPAD 3.0um
- 20F Minimum and Maximum METAL4 enclosure BONDPAD 3.0um
- 20G Minimum and Maximum METAL5 enclosure BONDPAD 3.0um
- 20H Minimum and Maximum METAL6 enclosure BONDPAD 3.0um

## 22.2 Antenna Rules

ANT1 Maximum ratio of field poly area to poly gate area 100

ANT2 Maximum ratio of metal area (METAL1 to METAL6) to  
poly gate area 200

ANT3 Maximum ratio of contact area to the poly gate area 10

ANT4 Maximum ratio of VIA area (VIA1 to VIA5) to poly  
gate area 20

## 22.3 Density Rules

DEN1 Minimum POLY density\* 15%

DEN2 Minimum METAL1 density\* 25%

DEN3 Minimum METAL2 density\* 25%

DEN4 Minimum METAL3 density\* 25%

DEN5 Minimum METAL4 density\* 25%

DEN6 Minimum METAL5 density\* 25%

DEN7 Minimum METAL6 density\* 25%

\*Density is calculated as Total POLY/METAL area/Chip area

## 23 Interconnect Capacitance Table

Top Layer	Bottom Layer	Area Capacitance aF/um <sup>2</sup>	Fringe Capacitance aF/um	Dielectric Thickness
Poly	Field	100	50	4000A
Poly	Nwell	100	50	4000A
Metal 1	Field	30	35	12000A
Metal 1	Nwell	30	35	12000A
Metal 1	Active	40	45	10000A
Metal 1	Poly	65	60	6000A
Metal 2	Field	15	25	27000A
Metal 2	Nwell	15	25	27000A
Metal 2	Active	18	27	24000A
Metal 2	Poly	17.5	30	22000A
Metal 2	Metal 1	35	45	10000A
Metal 3	Field	10	20	40000A
Metal 3	Nwell	10	20	40000A
Metal 3	Active	7.5	17.5	38000A
Metal 3	Poly	12.5	22.5	36000A
Metal 3	Metal 1	15.5	25.5	25000A
Metal 3	Metal 2	35.5	45.5	9000A
Metal 4	Field	5	20	60000A
Metal 4	Nwell	5	20	60000A
Metal 4	Active	6.5	32.5	55000A
Metal 4	Poly	7	18.5	55000A
Metal 4	Metal 1	9	46	40000A

Metal 4	Metal 2	15	47.5	30000A
Metal 4	Metal 3	40	60	10000A
Metal 5	Field	5	18.5	72000A
Metal 5	Nwell	5	18.5	67000A
Metal 5	Active	5.5	28	67000A
Metal 5	Poly	5.5	17	66000A
Metal 5	Metal 1	8	47.5	54000A
Metal 5	Metal 2	9.5	49	38000A
Metal 5	Metal 3	15	52	24000A
Metal 5	Metal 4	40.5	63.5	9000A
Metal 6	Field	4.5	17	84000A
Metal 6	Nwell	4.5	17	83000A
Metal 6	Active	6.0	21.5	81000A
Metal 6	Poly	6.5	16.5	63000A
Metal 6	Metal 1	8	48	58000A
Metal 6	Metal 2	10	50	46000A
Metal 6	Metal 3	17	50.5	31000A
Metal 6	Metal 4	18	52	22000A
Metal 6	Metal 5	50	67.5	10000A

## 24 Coupling Capacitance Table

Structure	Coupling Capacitance fF/um
Poly-Field	0.0555
Metal1-Field	0.1220
Metal1-Active	0.1110
Metal1-Poly	0.1000
Metal2-Field	0.0955
Metal2-Active	0.0888
Metal2-Poly	0.0800
Metal2-Metal1	0.0900
Metal3-Field	0.0966
Metal3-Active	0.0966
Metal3-Poly	0.0977
Metal3-Metal1	0.0933
Metal3-Metal2	0.0888
Metal4-Field	0.0889
Metal4-Active	0.0931
Metal4-Poly	0.0931
Metal4-Metal1	0.0991
Metal4-Metal2	0.0914
Metal4-Metal3	0.0889
Metal5-Field	0.0922
Metal5-Active	0.0920
Metal5-Poly	0.0922

Metal5-Metal1	0.0977
Metal5-Metal2	0.0966
Metal5-Metal3	0.0933
Metal5-Metal4	0.0899
Metal6-Field	0.1111
Metal6-Active	0.1122
Metal6-Poly	0.1221
Metal6-Metal1	0.1222
Metal6-Metal2	0.1233
Metal6-Metal3	0.1322
Metal6-Metal4	0.1112
Metal6-Metal5	0.1002

## 25 Sheet Resistance Table

Layer	Sheet Rho (in ohm/square)
Poly	7.5
N+ Diffusion	300
Metal 1	.1
Metal 2	.1
Metal 3	.1
Metal 4	.1
Metal 5	.1
Metal 6	.1
Poly Contact	5
Diffusion Contact	7.5