Control Design of PWM Converters: The User Friendly Approach

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Seminar material download: PET06

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Motivation

- Most switch mode systems need to operated in closed loop
- Performance largely dependent on the Compensator (feedback) design
- Loop control design is conceived as “black magic” OR requiring tedious analytical derivations
- Digital control is becoming relevant

Objective

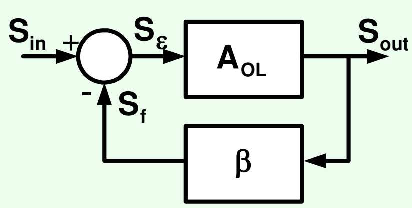
- To present a user friendly version of control loop design including both analog and digital control
- Based on:
  - ✓Intuition
  - ✓Simulation
  - ✓Simple calculations

Outline

1. Basics of feedback theory and graphical representation
2. Relationship between LoopGain and dynamic response
3. PWM converters as feedback systems
4. Voltage Mode (VM) control
5. Current Mode (dual loop) control
6. Simulation tools
7. Average models
8. Analog compensator networks
9. Digital control
10. Q&A

1. Basics of feedback theory and graphical representation

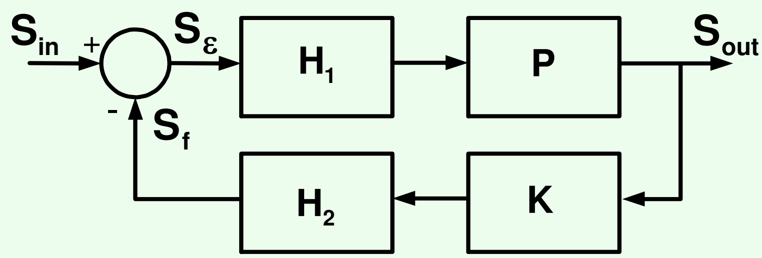
Block diagram of a feedback systems (one loop)



$$\boxed{A_{CL} = \frac{S_o}{S_{in}} = \frac{A_{OL}}{1+\beta \cdot A_{OL}}} \qquad \boxed{LG \equiv \beta A_{OL}}$$

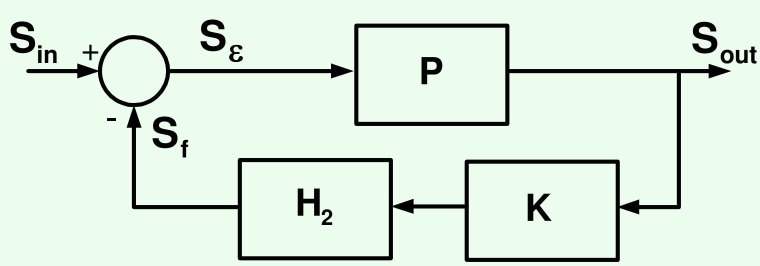
$$\left.\frac{S_o}{S_{in}}\right|_{\beta \cdot A_{OL} >> 1} = \frac{1}{\beta} \qquad \left.\frac{S_o}{S_{in}}\right|_{\beta \cdot A_{OL} << 1} = A_{OL}$$

Block Diagram



$$A_{CL} = \frac{S_o}{S_{in}} = \frac{1}{1 + \underbrace{H_1 H_2 K P}_{LG(f)}}$$

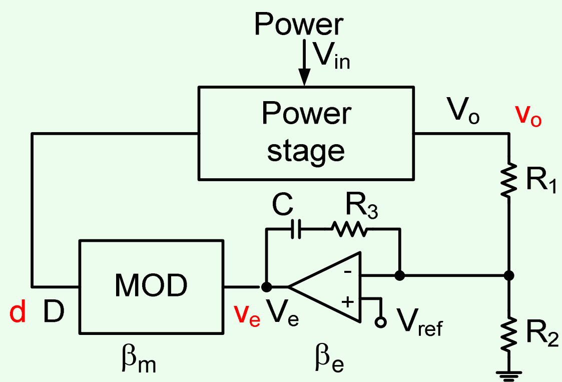
Effect of Feedback



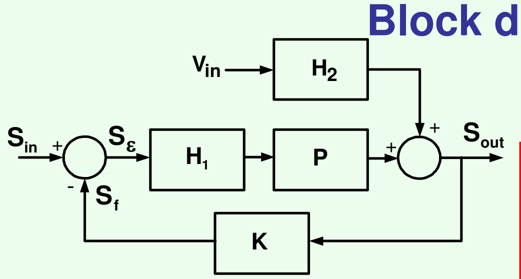
$$A_{CL} = \frac{S_o}{S_{in}} = \frac{P}{1 + \underbrace{H_2 P K}_{LG(f)}}$$

$$A_{CL}\Big|_{LG(f)>>1} = \frac{1}{H_2 K}$$

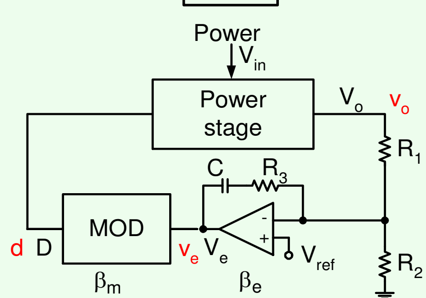
PWM Converter



Block diagram concepts

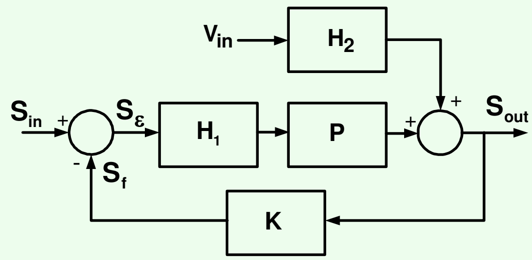


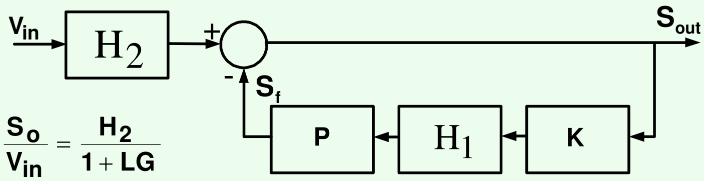
$$A_{CL} = \frac{S_o}{S_{in}} = \frac{H_1 P}{1 + \underbrace{H_1 P K}_{LG(f)}}$$



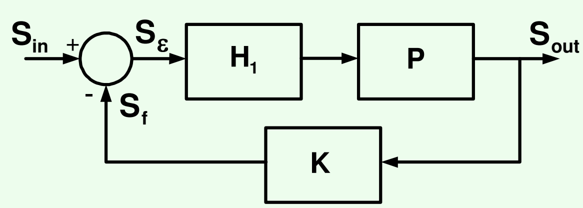
$$A_{CL}\Big|_{LG(f)>>1} = \frac{1}{K}$$

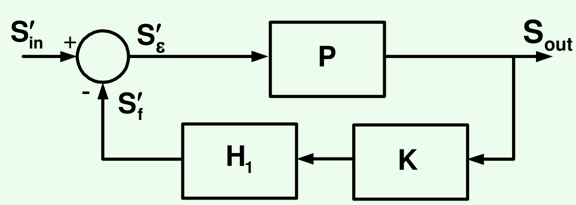
Audio susceptibility





$$\frac{S_o}{V_{in}} = \frac{H_2}{1+LG}$$

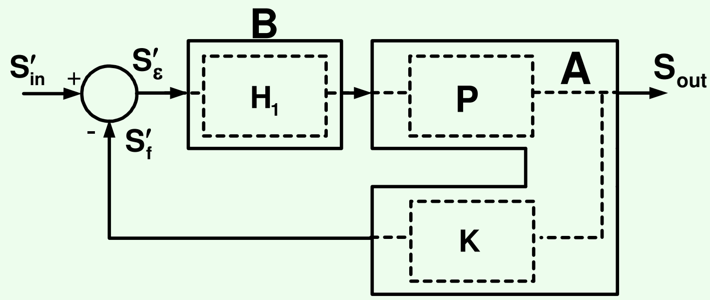




$$A_{CL} = \frac{S_{out}}{S_{in}} = \frac{H_1 P}{1+kH_1P} \rightarrow \frac{1}{k} \neq A'_{CL} = \frac{S_{out}}{S'_{in}} = \frac{P}{1+H_1P} \rightarrow \frac{1}{H_1 k}$$

But loop gains are equal: $LG(f) = H_1 K P$

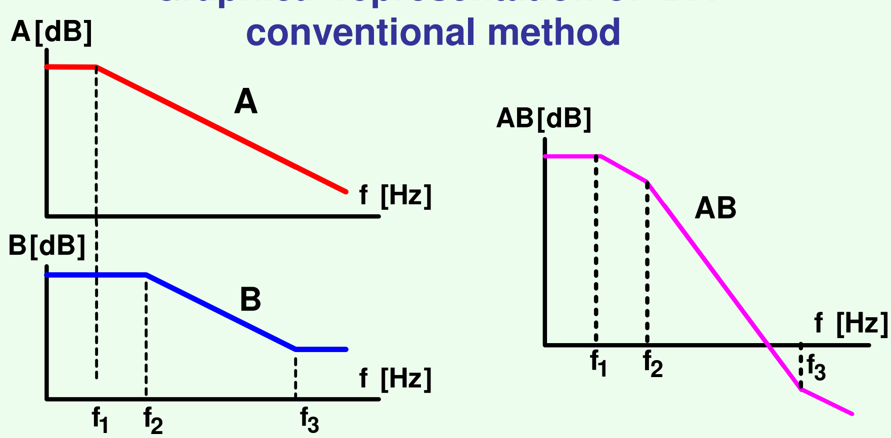
Block diagram division



$$LG(f) = AB$$

A – known (power stage + divider)
B – unknown (have to be designed)

Graphical representation of BA conventional method

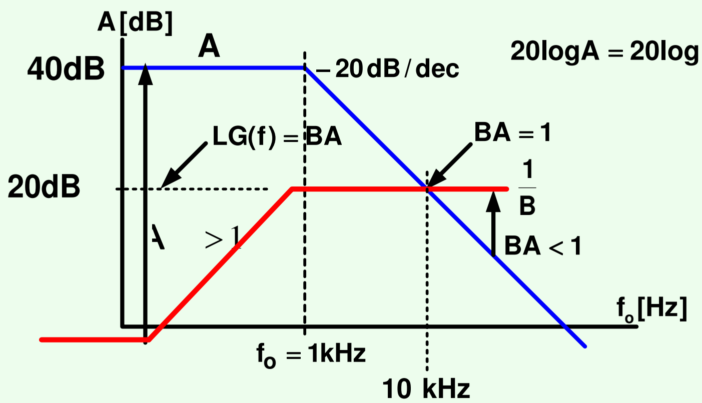


- Tedious – need to re-plot BA
- Analysis (not design) oriented
- Requires iterations

Graphical Representation of BA

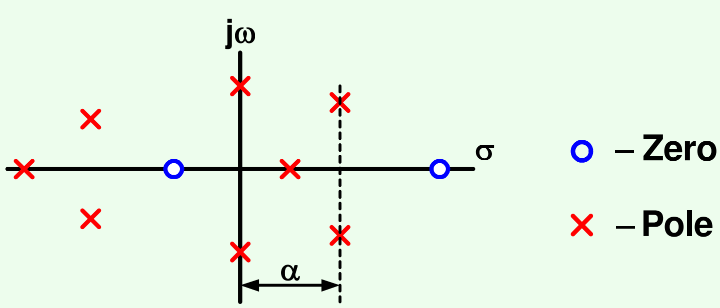
$$20\log A - 20\log\frac{1}{B} = 20\log(BA)$$

$$20\log A = 20\log\frac{1}{B} \Rightarrow B\cdot A = 1$$



Stability of Feedback System

$$H(s) = \frac{b_m s^m + b_{m-1}s^{m-1} + \ldots + 1}{a_n s^n + a_{n-1}s^{n-1} + \ldots + 1}$$



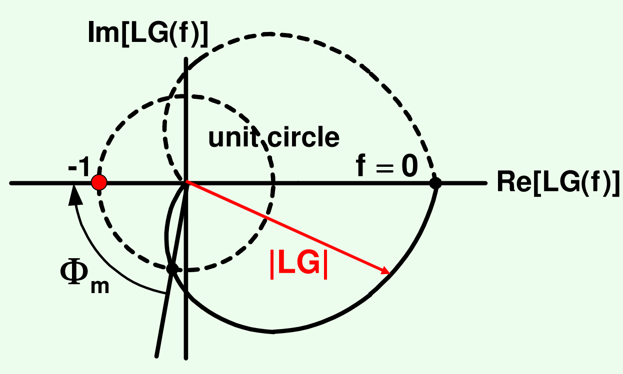
- RHP solutions include the term $\sin(\omega t)e^{\alpha t}$

Stability Criterion

$$A_{CL} = \frac{H_1 K}{1 + LG(f)}$$

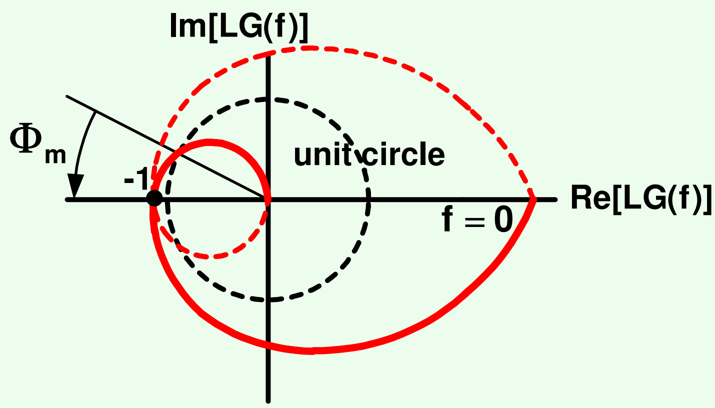
- The system is unstable if {1+LG(f)} has roots in the right half of the complex plane.
- Nyquist criterion is a test for location of {1+LG(f)} roots.
- Nyquist criterion is normally translated into the Bode plane (frequency domain)

Nyquist



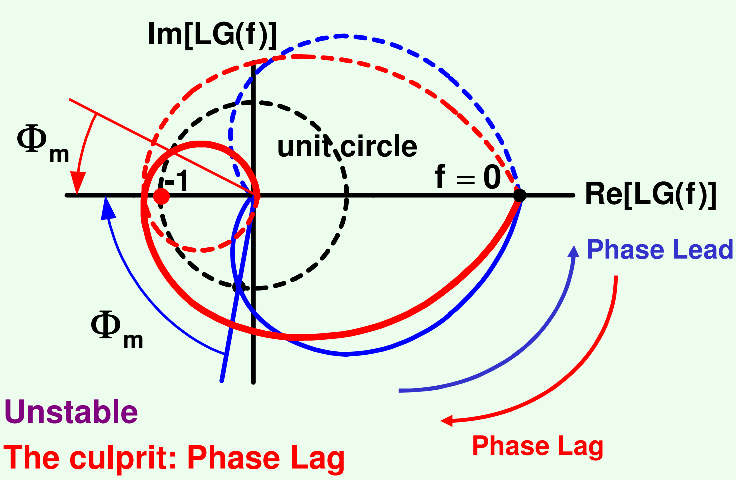
- **Stable**

Nyquist



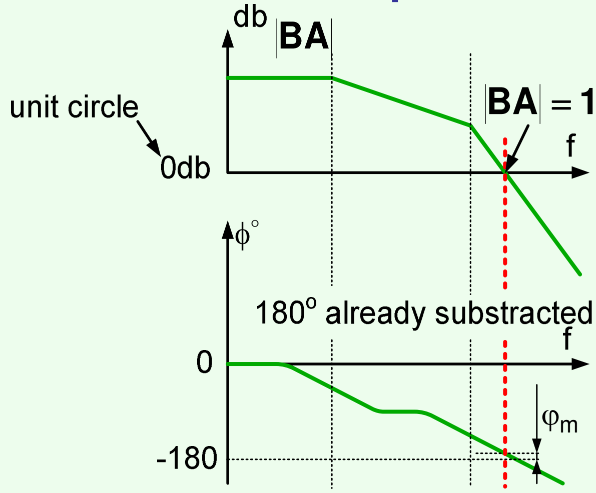
- Oscillatory

Nyquist



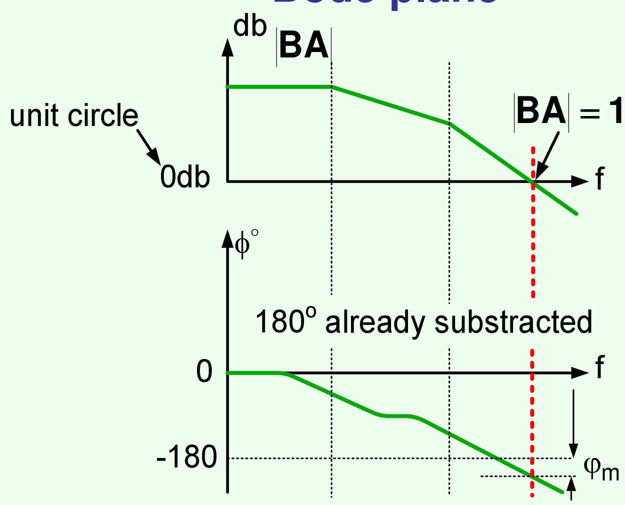
- Unstable
- The culprit: Phase Lag
- Phase Lead in LG can help stabilize a system

Bode plane



$$\varphi_m = \varphi_{|BA|=1} - (-180^{o}) = \varphi_{|BA|=1} + 180^{o}$$

Bode plane



$$\varphi_m = \varphi_{|BA|=1} - (-180^{o}) = \varphi_{|BA|=1} + 180^{o}$$

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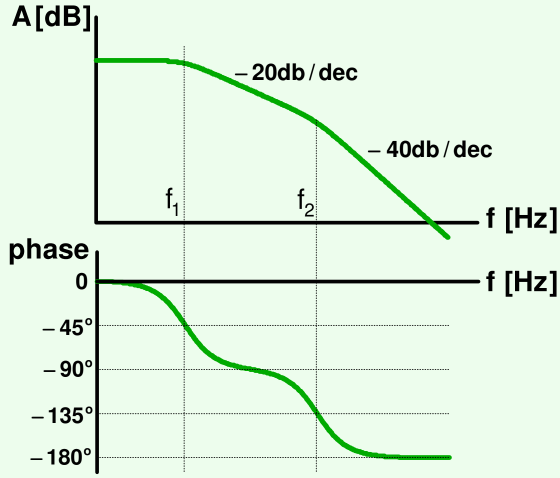
Minimum Phase Systems
no Right Half Plane Zero (RHPZ)



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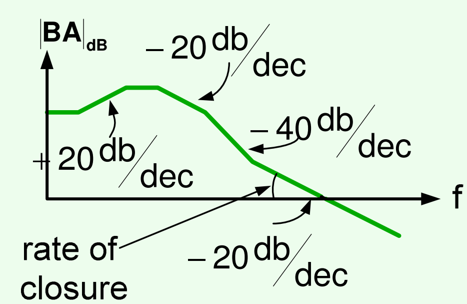
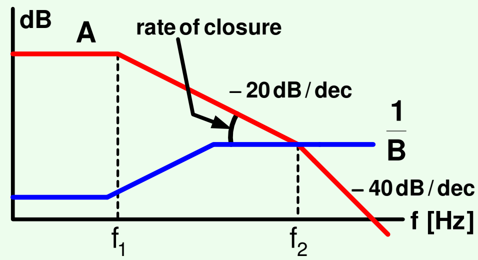
Rate of closure (ROC)
(minimum phase systems)



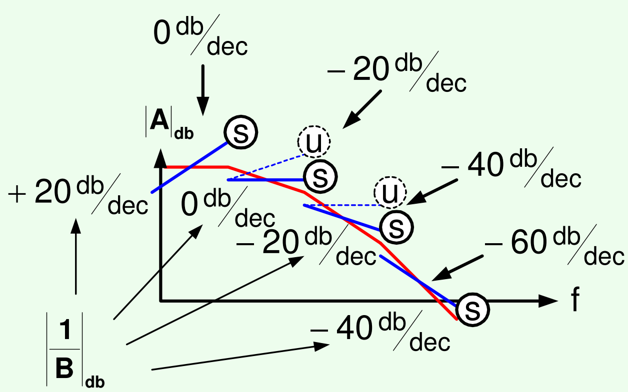
$$BA = \frac{\left(1+j\frac{f}{f_1}\right)\cdot\left(1+j\frac{f}{f_2}\right)\cdot\left(1+j\frac{f}{f_3}\right)\cdots\cdots}{\left(1+j\frac{f}{f_1}\right)\cdot\left(1+j\frac{f}{f_2}\right)\cdot\left(1+j\frac{f}{f_3}\right)\cdots\cdots}\cdots = \frac{k}{\left(1+j\frac{f}{f_p}\right)}$$

Application of the 1/B curve
Rate of closure



- Rate of closure of BA is the difference between the A and B slopes
- No need to re-plot BA
- Design oriented approach

Stability Criterion



If rate of closure $-20\,{}^{db}/_{dec}$ system is stable

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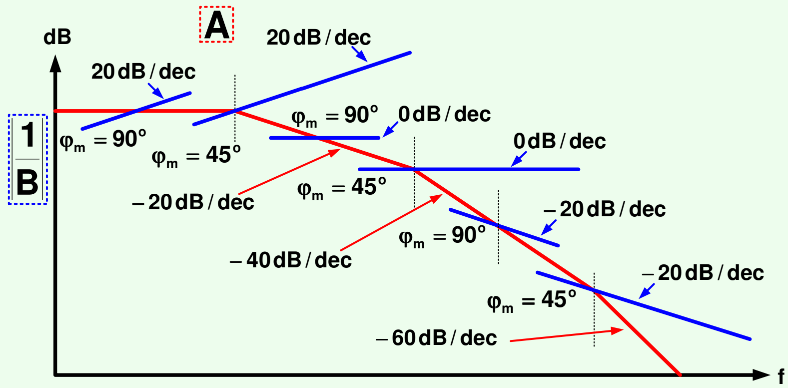
Phase Margin Examples



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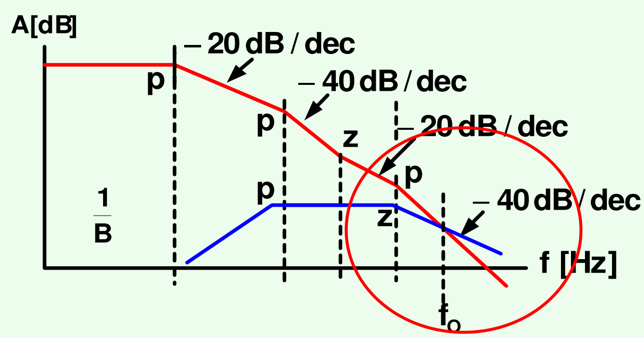
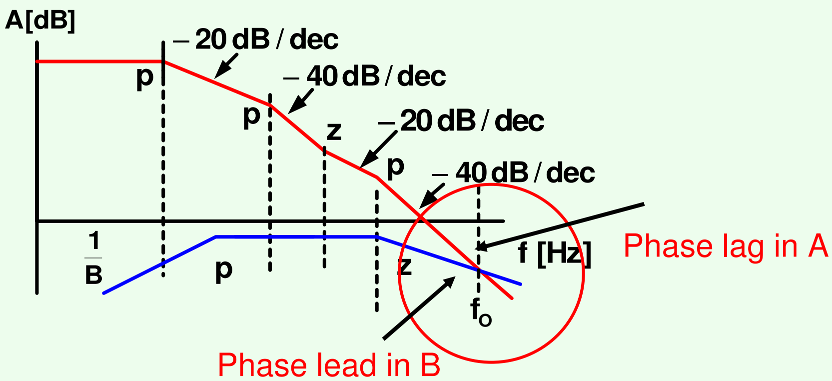
Phase Margin Calculation



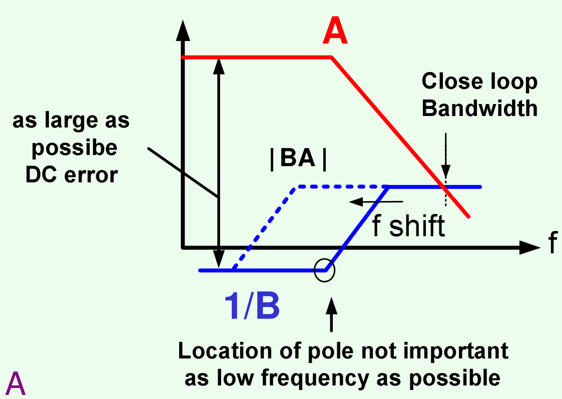
- For minimum phase systems history is not important

Approximate Phase Margin Calculation



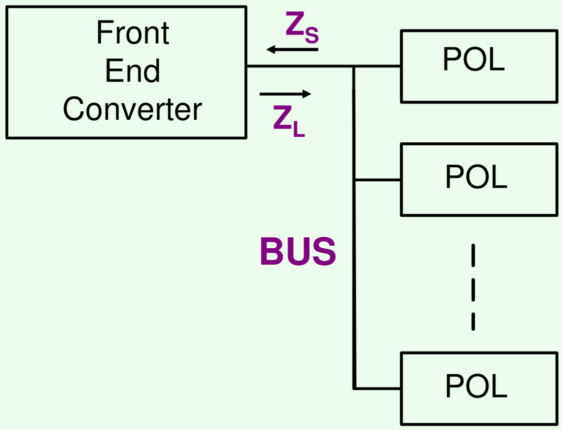
- Get the accurate phase at intersection by **simulation**

Design Steps



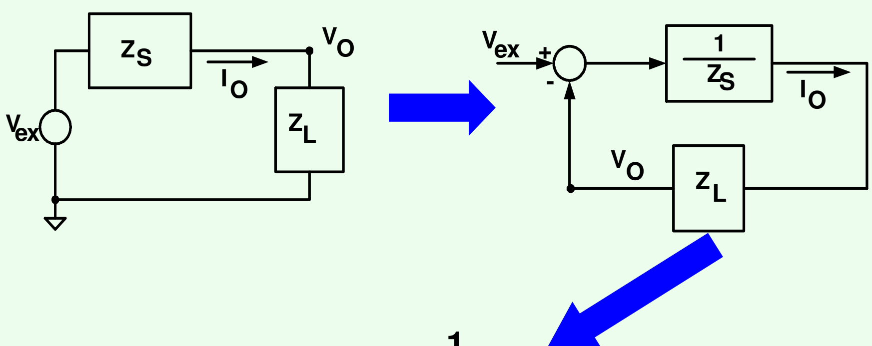
- Draw A
- Select cross point of BA (<< than $f_s/2$, for PWM)
- Select B shape

Stability of a Source-Load System



- $Z_L \rightarrow$ **negative resistance**

System stability

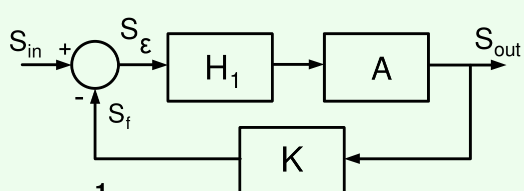


$$\text{LoopGain} = \frac{1}{Z_S} Z_L$$

Convenient way to examine the LG stability is the Nyquist stability test

2. Relationship between Loop Gain and dynamic response

Response in Closed Loop



$$\text{Desired: } A_{CL} = \frac{1}{K}$$

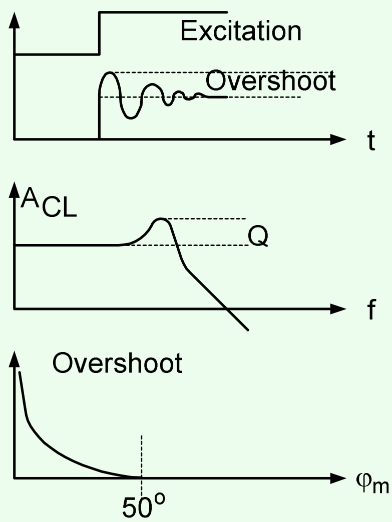
$$\text{What we get: } A_{CL} = \frac{1}{K} \cdot \frac{1}{\frac{s^2}{\omega_0{}^2} + \frac{s}{\omega_0 Q} + 1} \quad \text{for } \varphi_m \le 50^o$$

$$A_{CL} = \frac{1}{K} \cdot \frac{1}{\frac{s}{\omega_0} + 1} \quad \text{for } \varphi_m \ge 50^o$$

$$A_{CL}(0) = \frac{1}{K}$$

- **For small φ_m, A_{CL} behaves as a second order system**

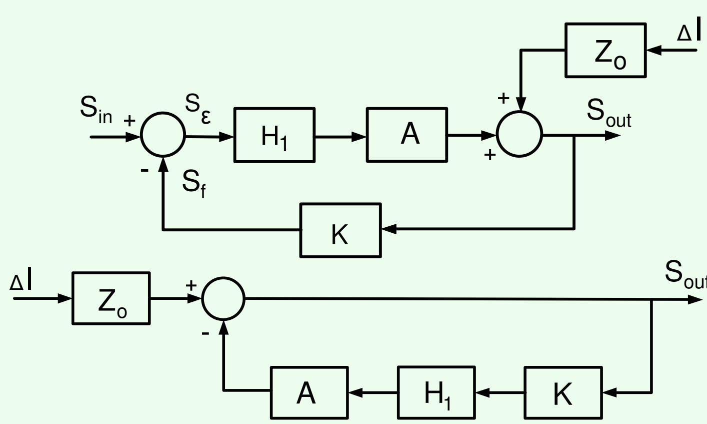
Overshoot and Q in Closed Loop in Response to step in S_{in}



$$Q \cong \frac{\sqrt{\cos\varphi_m}}{\sin\varphi_m} \quad \text{for} \quad \varphi_m < 50^o$$

$$\boxed{\text{Design target } \varphi_m \geq 45^o}$$

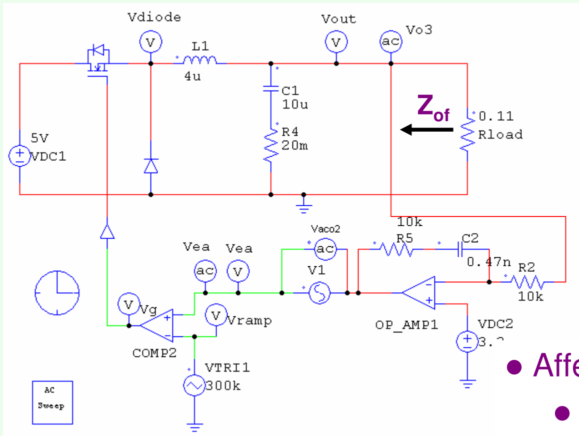
Load-Step Response



$$\frac{S_{out}}{\Delta I} = \frac{Z_o}{1 + \underbrace{A \cdot H_1 \cdot K}_{LG}}$$

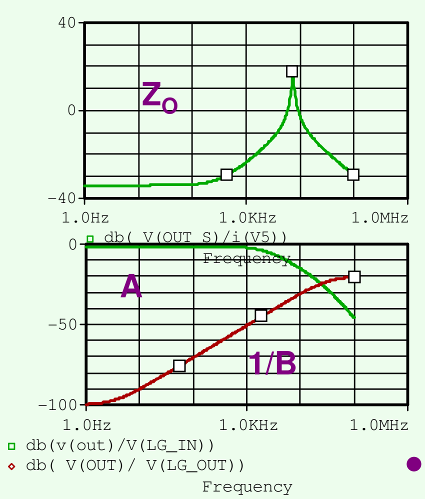
- Small-signal output impedance

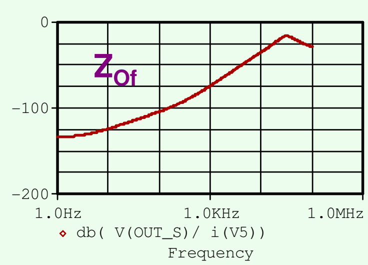
Load-Step Response



- Affected by:
  - Output impedance
  - ESR of output capacitor
  - Slew rate of inductor

Output Impedance (Immunity to load changes)

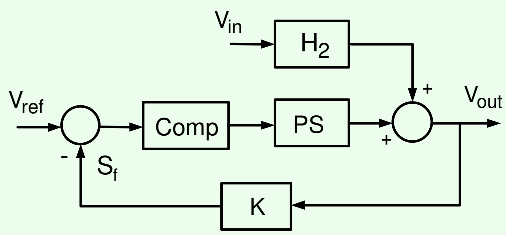




$$Z_{of} = \frac{v_{out}}{\Delta i_o} = \frac{Z_o}{1+\underbrace{AB}_{LG}}$$

- **Buck converter – small signal**

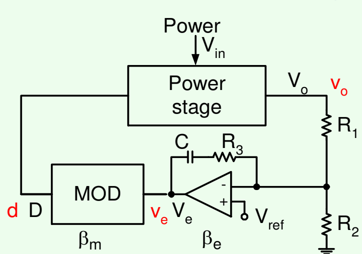
Audio-Susceptibility (Line Regulation) (Immunity to input voltage changes)

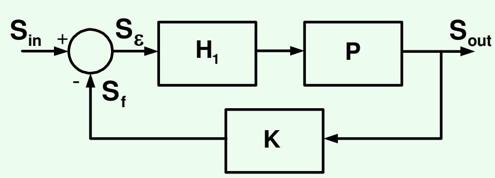


$$\frac{V_{out}}{V_{in}} = \frac{H_2}{1+LG(f)}$$

- **Large LG reduces susceptibility**

Steady-state (DC) Error





$$S_\varepsilon = \frac{S_{in}}{1+LG}$$

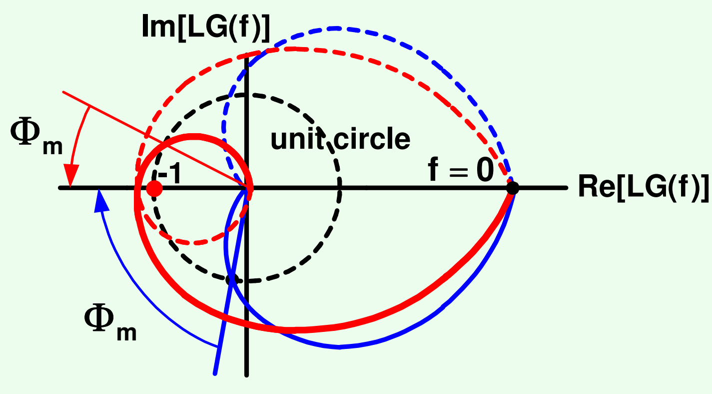
- S_ε is the offset between the sampled output and reference
- Small DC error for large LG(0)

Dynamic Response Summary

- Systems that have a slope of –20 db/dec are easy to control
- Response is largely determined by LG(f)
- Desired LG:
  - LG as large as possible at low frequencies
    (small DC errors)
  - LG of large BW - intersection point of A and 1/B
    (quick response, fast recovery, rejection of Vin changes)
  - Phase margin > 45^0
    (reasonable overshoot)

The culprit: Phase delay in LG

Nyquist



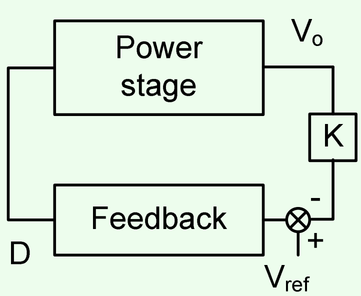
Design target $\varphi_m \geq 45^o$

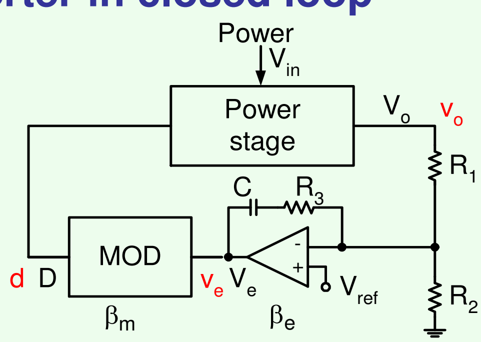
3. PWM converters as feedback systems

Issues:

- Stability
- Rejection of input voltage variations (audio susceptibility)
- Immunity to load changes
- Quick response to reference change - good tracking.

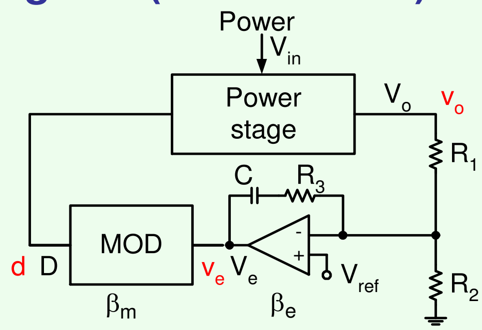
PWM converter in closed loop





- **Small signal responses**
- **Linearization around operating point**

Type of Blocks
Small Signals (Perturbation) Responses



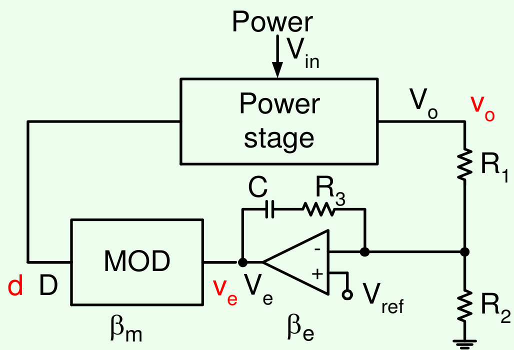
- Power stage is a Switching System (may be non linear)
- Feedback is an analog or digital controller
- Modulator: mixed mode
- Linear control theory based design → small signal response

Small-Signals (Perturbation) Responses

- Analytical solutions
- Simulation
  - Injection of sinusoidal perturbation
  - AC analysis of behavioral average model

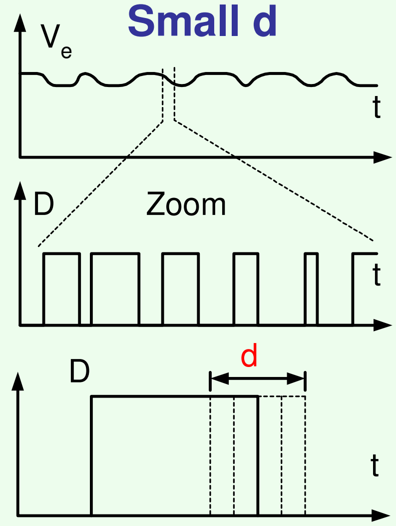
- **This seminar promotes the simulation approach**

Small signal response of the modular



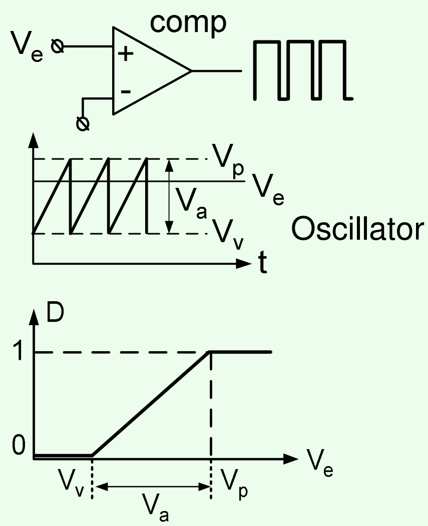
- **Relationship between v_e and d ($K_m = d/v_e$)**

Small d



d is the AC component of D

Modulator



$$V_t = \frac{(V_p - V_v)t}{T_s} + V_v$$

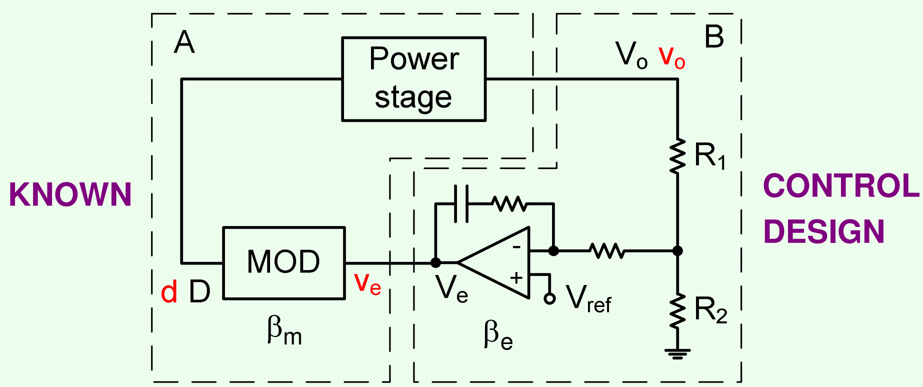
$$V_t = V_e = \frac{(V_p - V_v)t_{on}}{T_s} + V_v$$

$$\frac{t_{on}}{T_s} = D_{on} = \frac{(V_e - V_v)}{V_p - V_v}$$

$$\mathbf{d} = \frac{\mathbf{v_e}}{\mathbf{V_p} - \mathbf{V_v}} = \frac{\mathbf{v_e}}{\mathbf{V_a}}$$

$$\mathbf{K_m} = \frac{\mathbf{d}}{\mathbf{ve}} = \frac{\mathbf{1}}{\mathbf{V_a}}$$

THE CONTROL DESIGN PROBLEM

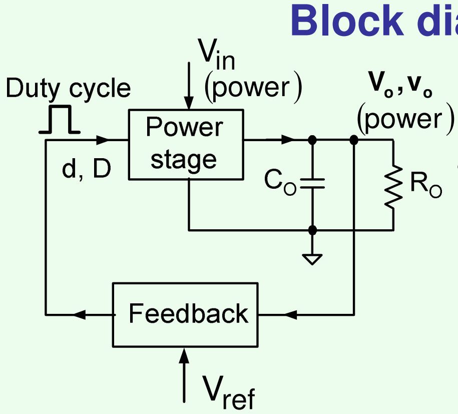


$$\frac{v_o}{v_e}(f) - \text{Analog Function} \qquad \beta_m = \frac{d}{v_e}$$

- **A → Power Stage ; B → compensator**

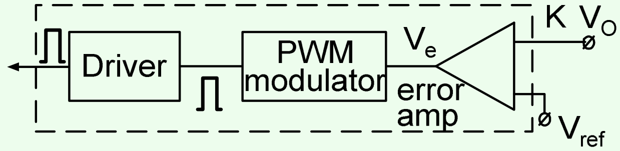
4. Voltage mode (one loop) control

Block diagram

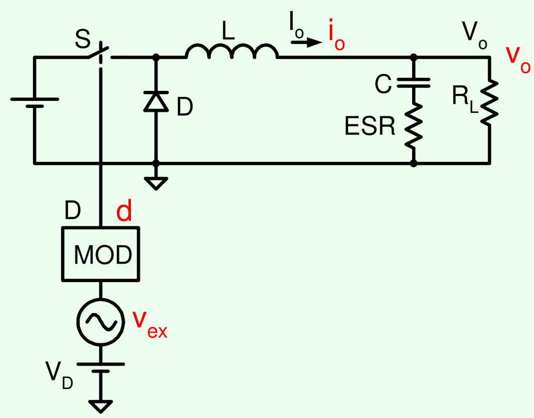


The power conversion system

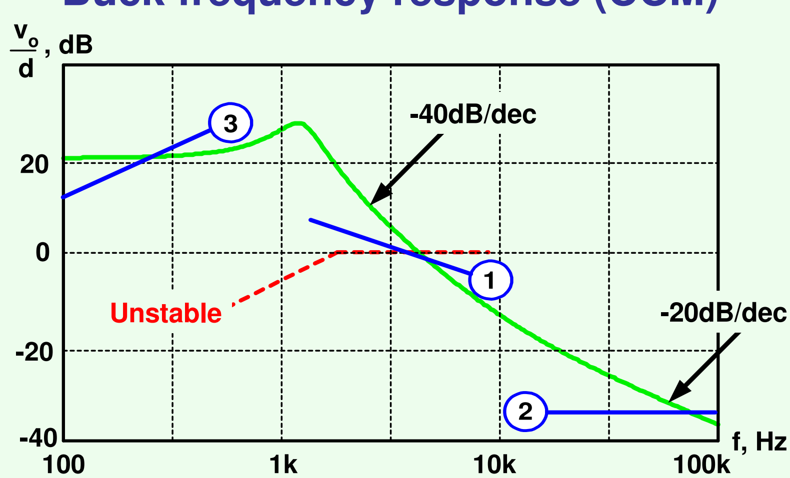
Controller



Buck small-signal frequency response (CCM)



Buck frequency response (CCM)



- Second order plus zero due to ESR of C_O

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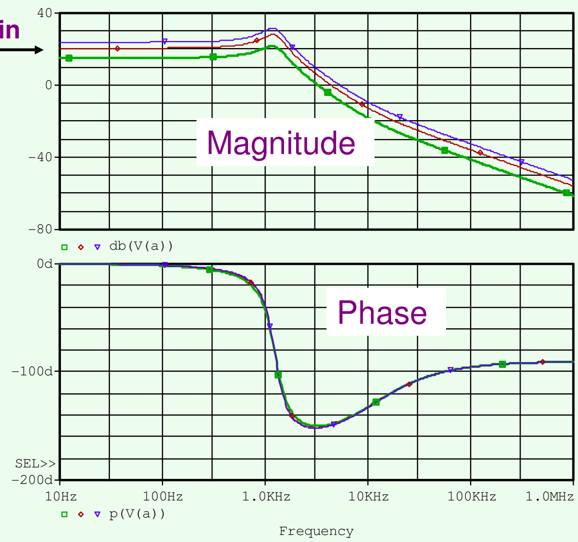
Dependence on V_{in}

$\frac{d}{v_e}$

V_{in}

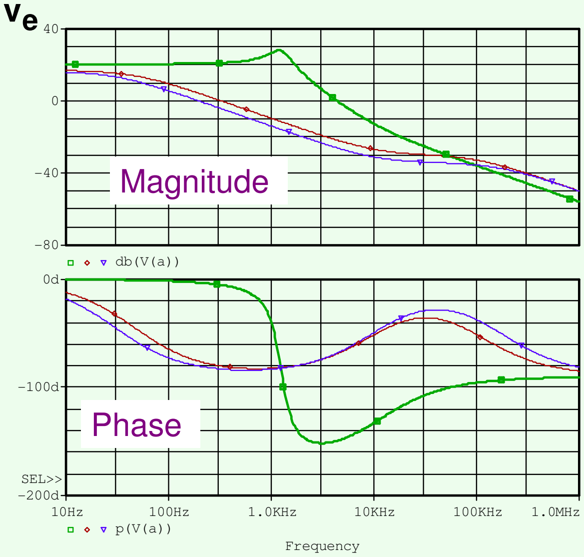


V_{in}:
5V
10V
15V

Prof. S. Ben-Yaakov , Control Design of PWM Converters [56]

Effect of Load

$\frac{d}{v_e}$



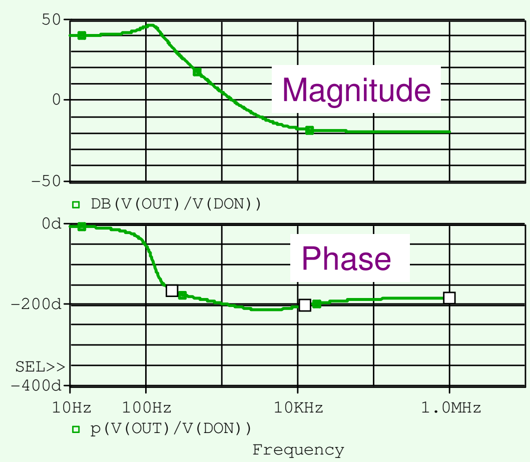
R_L=
10Ω - CCM
50 Ω - DCM
100 Ω - DCM

Buck Derived Converters

- Forward
- Half bridge (HB)
- Full Bridge (FB)

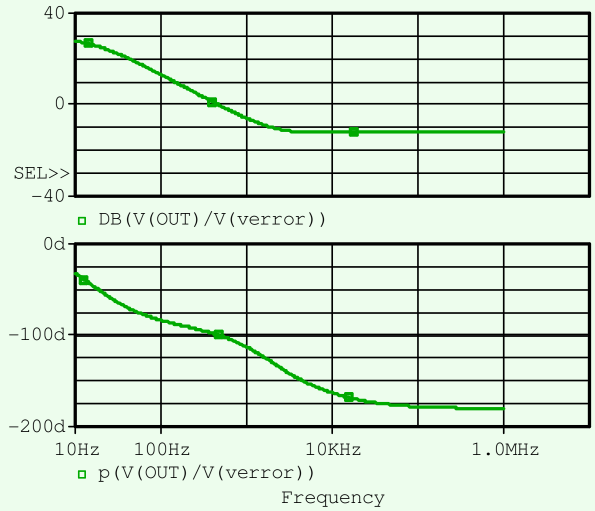
- **Simulation is the simplest way to obtain the transfer functions**

Boost Power Stage
Small signal response

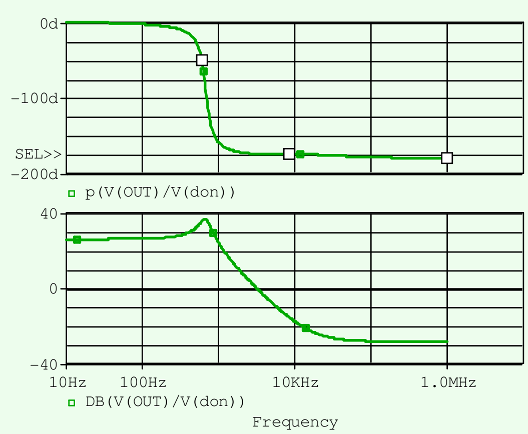


- **RHPZ – non minimum-phase system**

CM Boost



Buck-Boost (Flyback) Power Stage



- RHPZ – non minimum-phase system

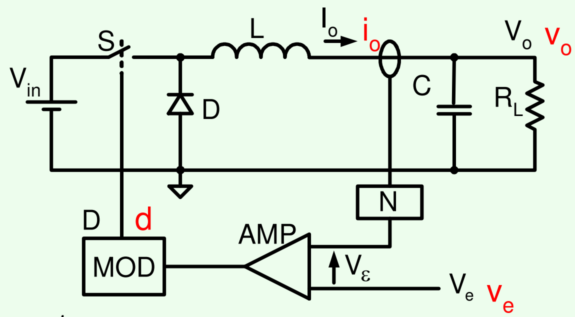
5. Current Mode (dual loop) control

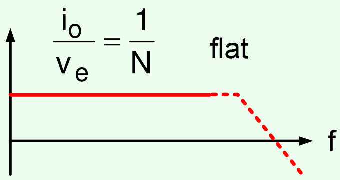
Current Feedback

- The problem of voltage mode control:
  Transfer function is second order
- Solution: Add current Feedback

- **System order is reduced for each state variable (inner loop) feedback**

The effect of current feedback



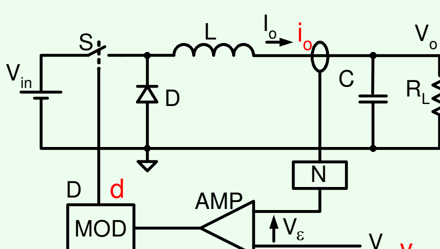


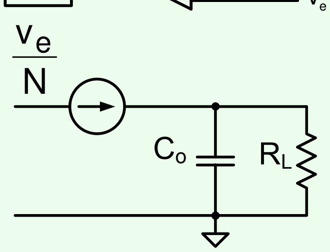
For ‘strong’ feedback

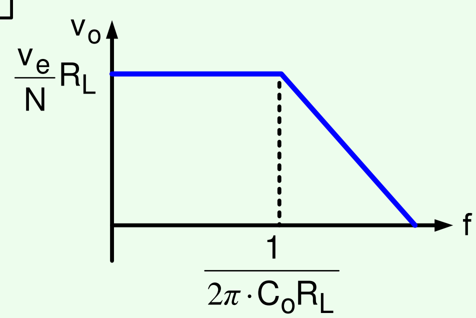
$$LG >> 1 \quad v_\varepsilon \to 0$$

$$i_o = \frac{1}{N} v_e$$

Transfer function with closed Current Loop

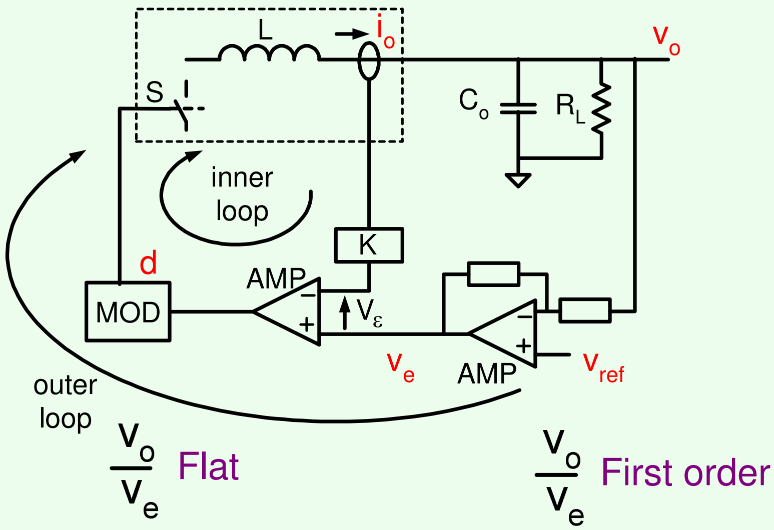




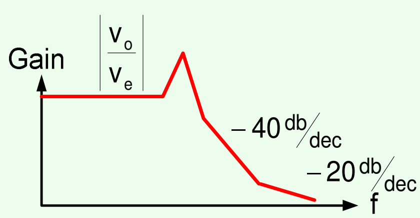


- First order system !

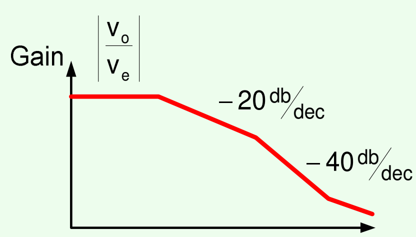
Current Mode



The advantages of current feedback



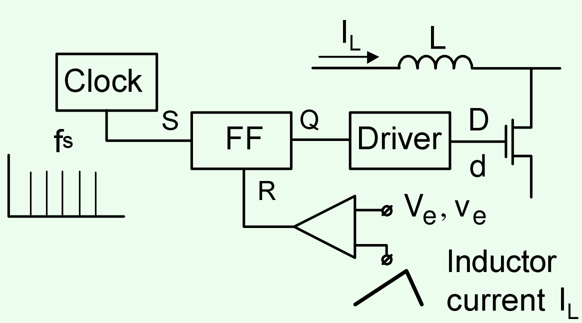
Typical power stage VM



Same power stage (outer loop) with CM

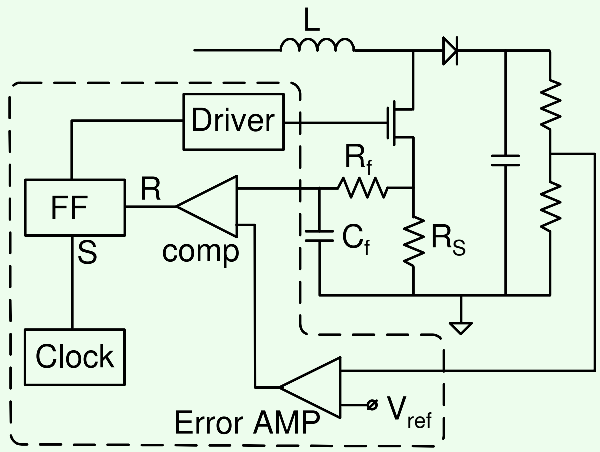
7. Peak Current Mode (PCM) control

PCM Modulator



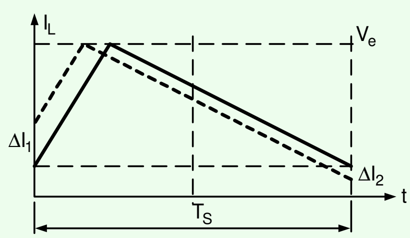
$$\frac{V_o}{V_{in}} = f(D_{on}) \text{ is the same !}$$

Implementation CM Boost



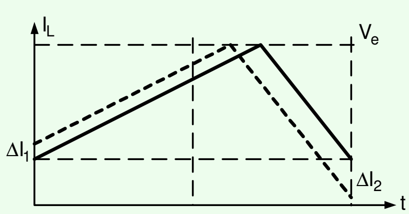
Some controllers have amplifiers for sensed current

The nature of Subharmonic Oscillations



The geometric explanation

D<0.5 $\Delta I_2 < \Delta I_1$



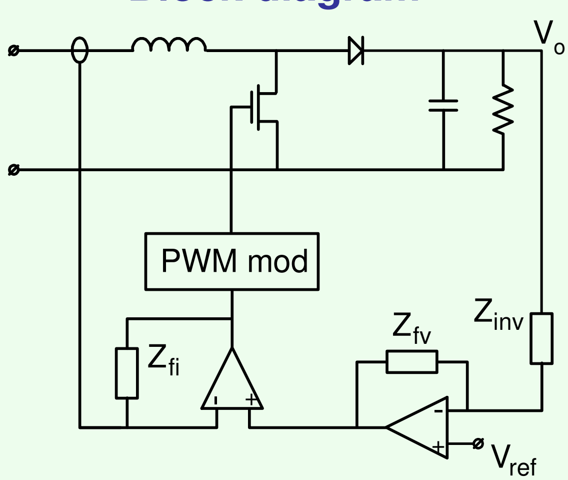
D>0.5 $\Delta I_2 > \Delta I_1$

- **For D>0.5 need slope compensation**

Extra delay in PCM (Ridley)

- PCM is a current sampling process
- Subject to sampling delay
- Delay was derived by Ray Ridley
- Important for frequencies above $f_s/10$
- Mostly of theoretical importance

Average Current Mode (ACM) Block diagram



- Current sample is filtered first attenuate high frequency (f_S)

PCM and ACM

- Both are current feedbacks
- Both reduce the order of system
- The difference is in BW of the current feedback loop
- Both increase the output impedance

Advantages of peak CM (PCM)

- Cycle by cycle protection
- Better dynamics

Disadvantages

- Leading edge spike
- Subharmonic oscillations

6. Simulation tools

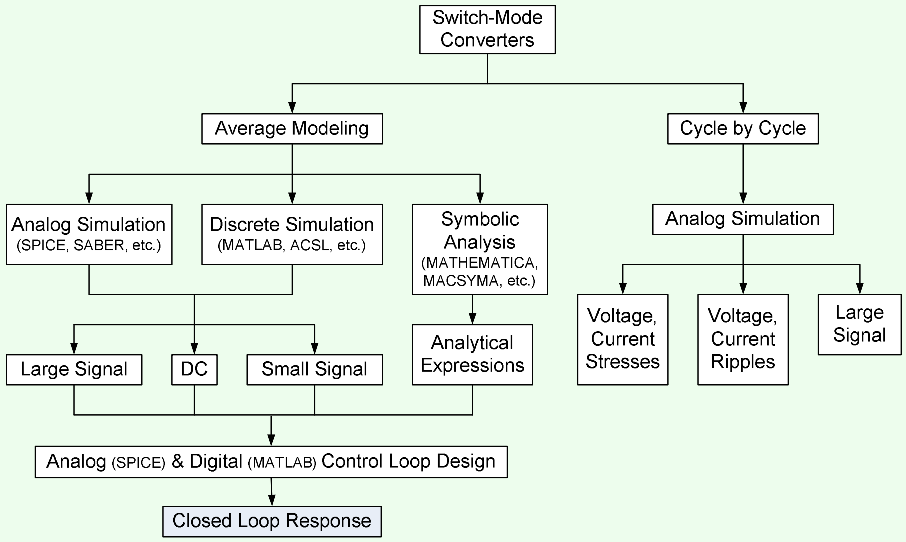
- General purpose simulators
- Dedicated simulators
- PC and web based simulators

- **This seminar promotes PC based general purpose simulators**

Why Simulation

- Most control design methods apply graphical representations of transfer functions
- One can get the plots from analytical expressions or by simulation
- Simulation is the easiest way to get “A” (the **small signal** response of the power stage)

Computer Simulation of Power Conversion Systems



Desired Simulator's Features for Power Electronics Systems

- Convergence
- Physical models
- Small signal analysis
- Interfaces
- Run time
- Behavioral models
- Statistical and optimization analysis
- Discrete domain simulation capabilities

Some Popular Modern Simulators

SPICE Based (Berkeley)

- PSPICE – MicroSim - Orcad - Cadence
- ICAP/4 – Intusoft
- MICROCAP - Spectrum

Others

- PSIM - Powersim
- Simplorer -Ansoft
- PLECS -Plexim

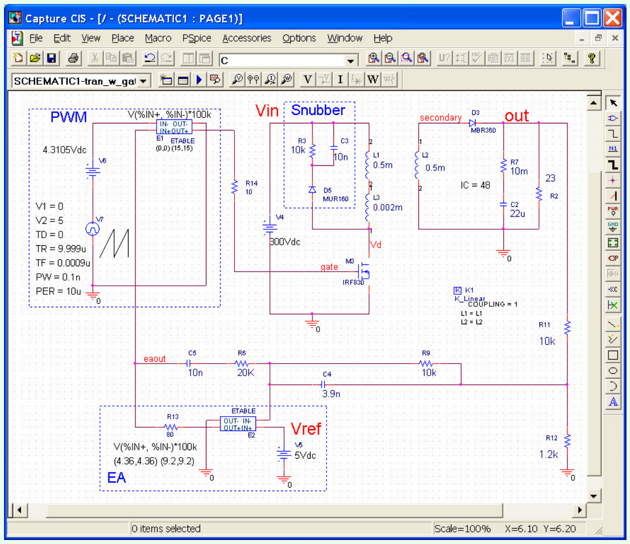
Power IC Models Library

- AEi – Design Automation

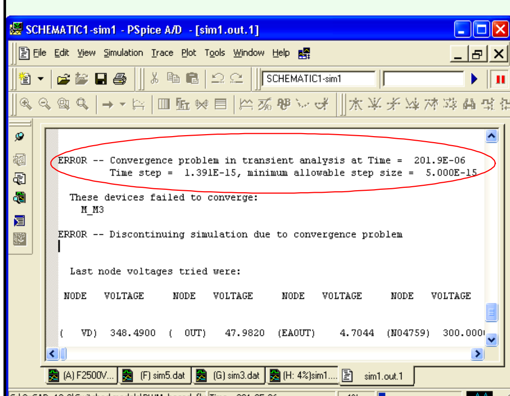
PSPICE – The Physical Simulator

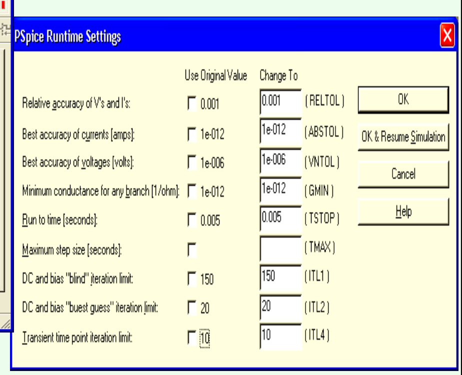
- Most popular
- SPICE based simulator (Berkley)
- Used extensively for circuit simulation
- Extensive physical models libraries
- Behavioral models (ABM)
- AC analysis
- Statistical analysis
- Optimization tool
- Some PWM models
- MATLAB/Simulink interface

Working with PSPICE



PSPICE Convergence Problems





- Very common in switched circuits simulation

AEi Power IC Library

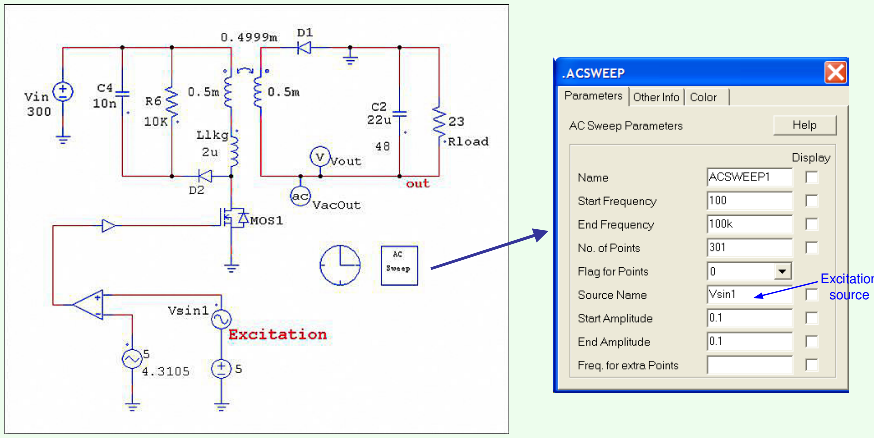
- PWM controllers are not included in PSPICE libraries
- AEi's library supports Power Electronics
  - *150 SPICE Models for Popular Power ICs*
    - ✓ *Regulators, Controllers, Switchers*
    - ✓ *FET Drivers*
  - *Support for Capture and Schematics*
    - ✓ *Symbols*
    - ✓ *Example Applications schematics/simulations*
    - ✓ *Documentation*

PSIM -The Switching Circuit Simulator

- Disregards switching instances
- Fast and effective time domain algorithm
- Constant time step approach
- Transient (time domain) based AC analysis
- User friendly intuitive interface
- Generic models: passive, switchers, motors
- Analog Behavior Models library
- Simulink interface
- Interface to magnetics program

- Prone to errors in simulation results
- Simple output graphics utility

PSIM AC Model



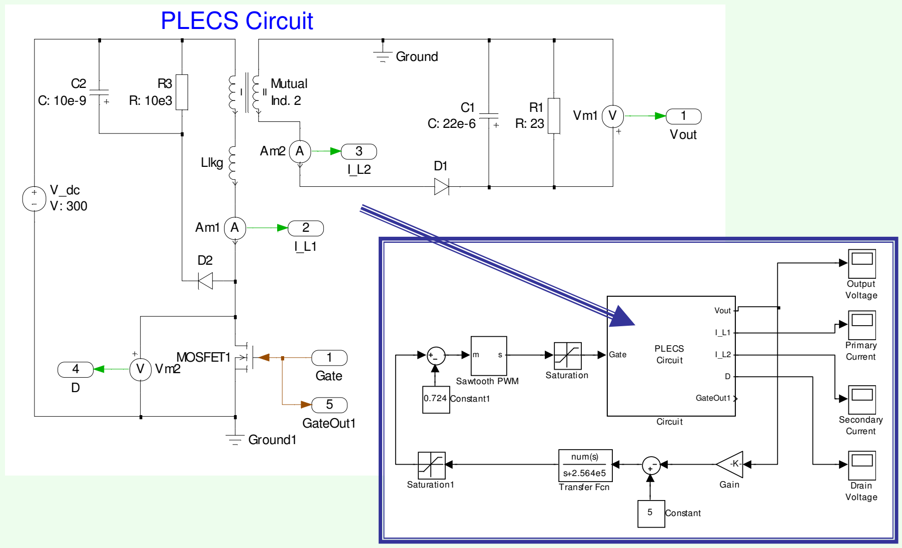
- Multiple time-domain runs are used to obtain AC response

PLECS – The MATLAB Plug-In

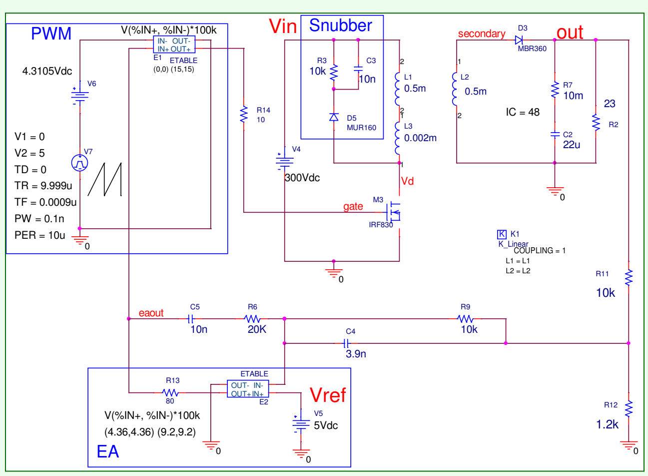
- Power tool-kit for SIMULINK
- Allows the simulation of power stage as integrated part of MATLAB (SIMULINK) simulation without introducing extra delays
- Ideal for investigating digital control loops in power systems

- Only generic models
- Simulink interface for both schematic and graphics

PLECS Circuit as a Simulink Block



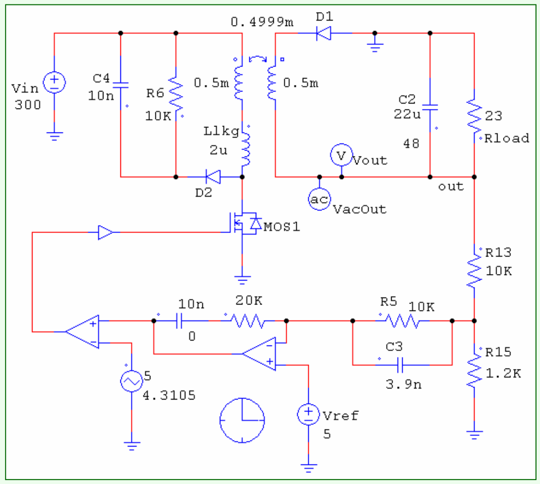
PSPICE cycle-by-cycle model



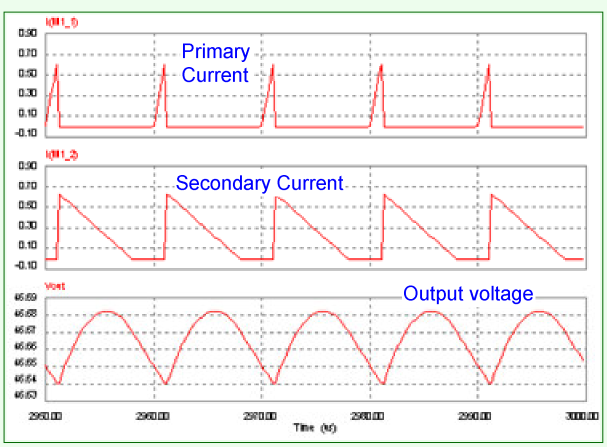
- Uses physical level models of “real” devices

PSIM Flyback cycle-by-cycle model (Time Domain)

Demo
Real time: 3 ms



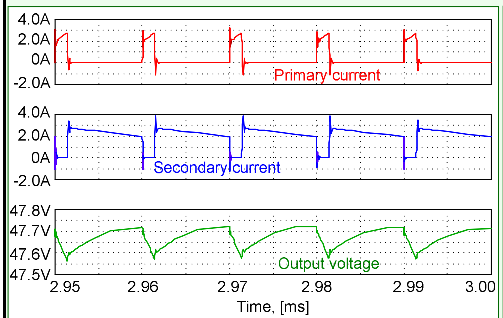
PSIM DCM cycle-by-cycle simulation results

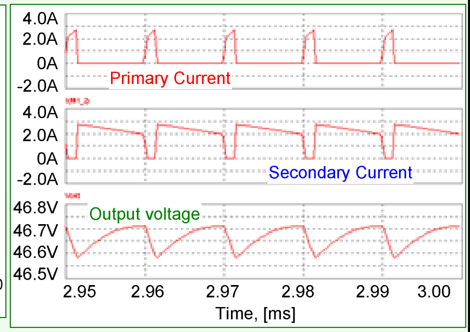


Rload=220Ω

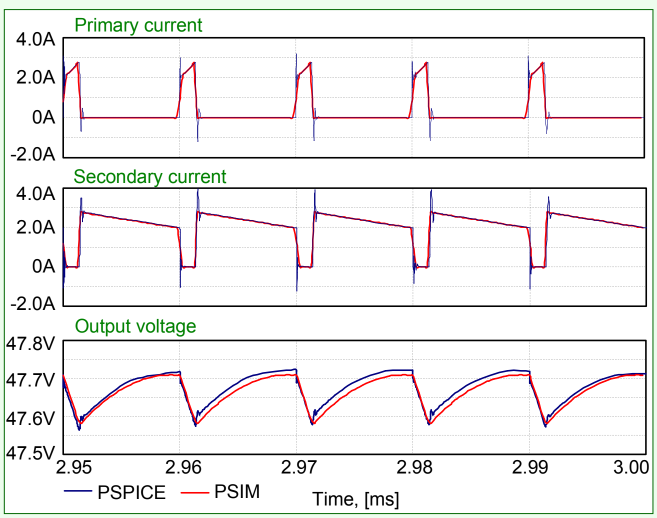
- Textbook waveforms

PSPICE vs. PSIM Flyback cycle-by-cycle simulation results





PSPICE vs. PSIM Flyback cycle-by-cycle simulation results



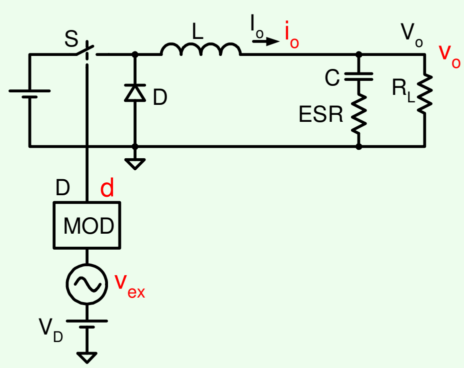
Small Signal (AC) Analysis
(Needed for Control Design)

Two Alternatives:

1. Full switched circuit:
   Injection of a sinusoidal perturbations
   PSPICE → manually
   PSIM → automatic

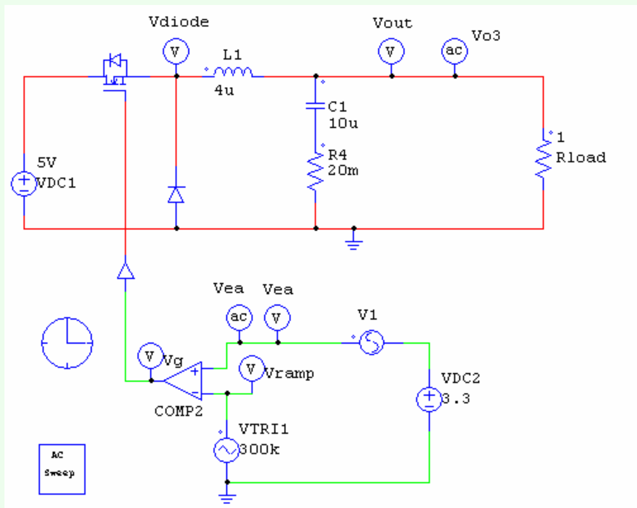
2. Average Model
   PSPICE → AC analysis
   (linearization by simulator)
   PSIM → automatic transient injection

Small signal response by injection of sinusoidal perturbations (time domain)

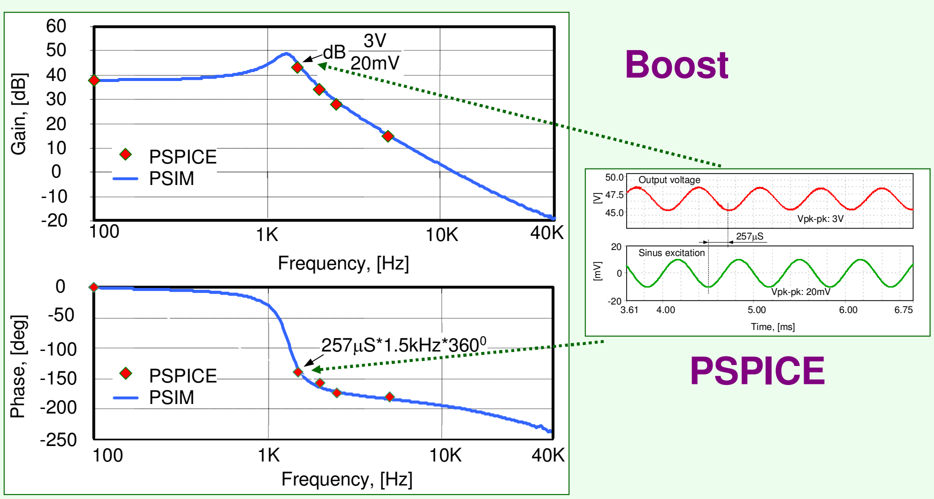


- **Transient simulation – any simulator**

PSIM Realization (Buck)

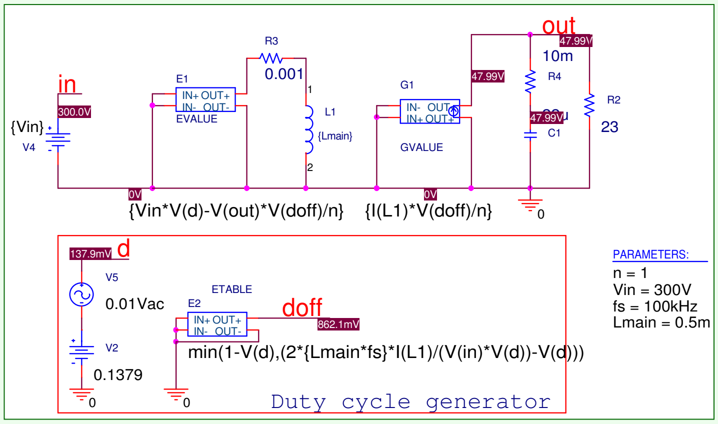


Power-Stage small signal transfer function By injection of sinusoidal perturbation - PSIM & PSPICE



The Behavioral Approach

Average Model of Flyback - PSPICE



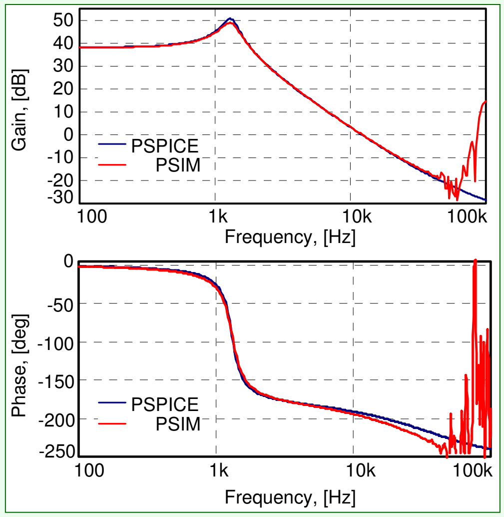
- Average models can be applied to obtain frequency response – AC analysis (to be discussed later)

Signal injection versus Average model

- Signal injection
  - Applies the switching schematics as is
  - Takes a long time to run
  - Noisy at high frequency
- Average model
  - Runs very fast
  - Need to built a behavioral equivalent
  - Some topologies/controllers are not easy to convert to average circuits

PSIM vs. PSPICE AC Comparison

$$\frac{v_{out}}{d}$$



Behavioral average modeling of switch mode systems

Applications:

- DC transfer functions
- Transient (large signal, time domain) phenomena
- Small signal (AC, time domain) transfer functions

Not applicable to:

- Switching details, rise and fall times, spikes
- Device characteristics and losses
- Subharmonic oscillations

- Conduction losses can be accounted for
- HF ripple can be estimated

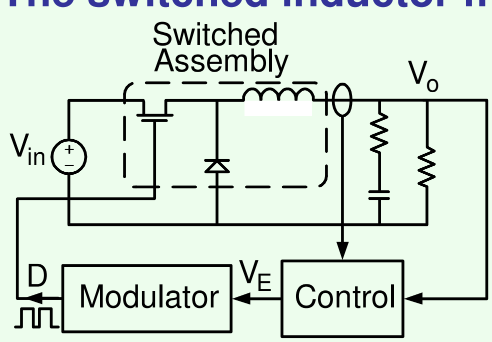
7. Average Models
The Switched Inductor Model (SIM) Strategy

- Identify the switched assembly
- Replace the switching part by a continuous behavioral (analog) equivalent circuit
- Leave the analog part as-is
- Run the combined circuit on a general purpose simulator

The modeling methodology presented in this seminar is highly 'portable', independent of simulator

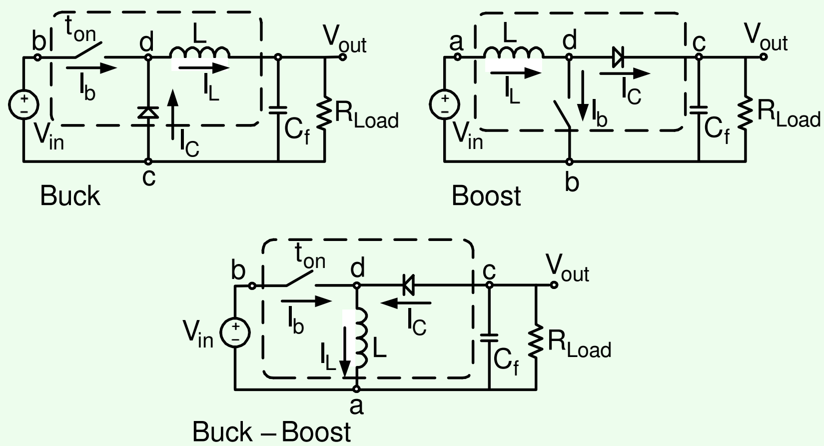
Demonstration by PSPICE Ver. 10.5 (Demo Edition)

The switched inductor model

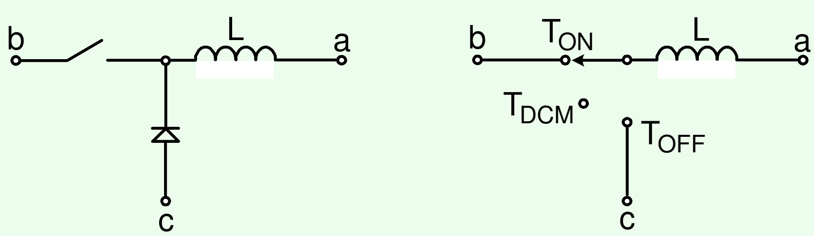


- The problematic part : Switched Assembly
- Rest of the circuit continuous - SPICE compatible
- The objective : translate the Switched Assembly into an equivalent circuit which is SPICE compatible

Average Simulation of PWM Converters



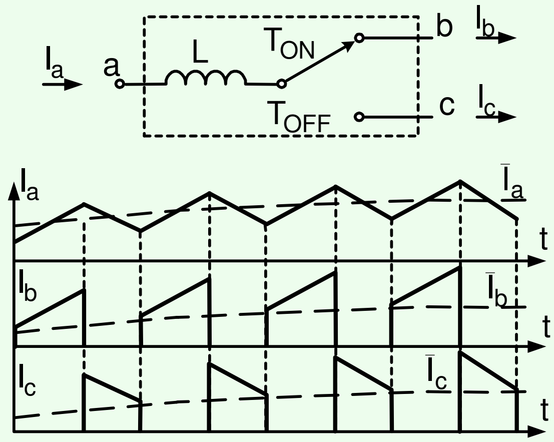
Possible switch modes



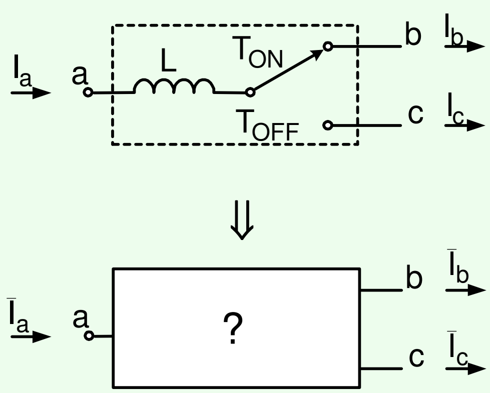
T_{ON} - switch conduction time
T_{OFF} - diode conduction time
T_{DCM} - no current time (in DCM)

The Switched Inductor Model (SIM) (CCM)

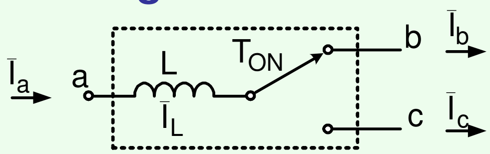
The concept of average signals



Objective : To replace the switched part by a continuous network



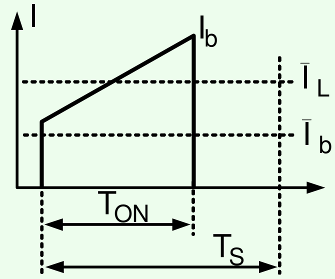
Average current



$$\bar{I}_b = \frac{\bar{I}_L T_{ON}}{T_S} = \bar{I}_L D_{on}$$

$$D_{on} = \frac{T_{ON}}{T_S}$$

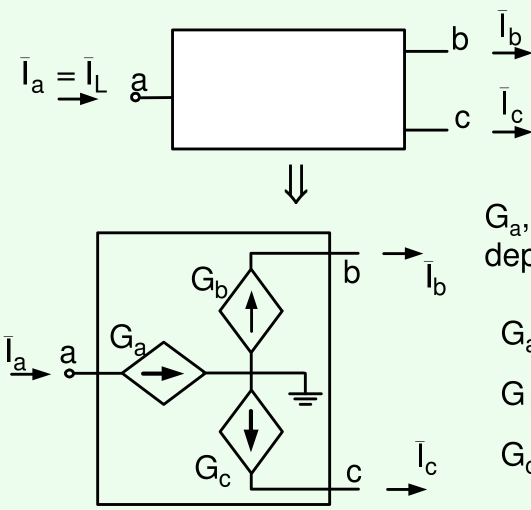
$$\bar{I}_a = \bar{I}_L$$



Similarly :

$$\bar{I}_c = \frac{\bar{I}_L T_{OFF}}{T_S} = \bar{I}_L D_{off}$$

Toward a continuous model



G_a, G_b,C_c - current dependent sources

$$G_a \equiv \bar{I}_L$$

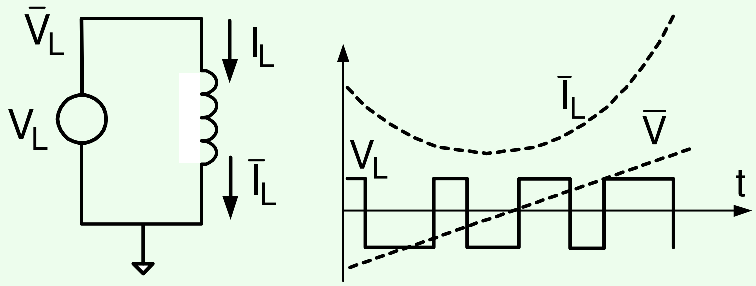
$$G_b \equiv \bar{I}_L \cdot D_{on}$$

$$G_c \equiv \bar{I}_L \cdot D_{off}$$

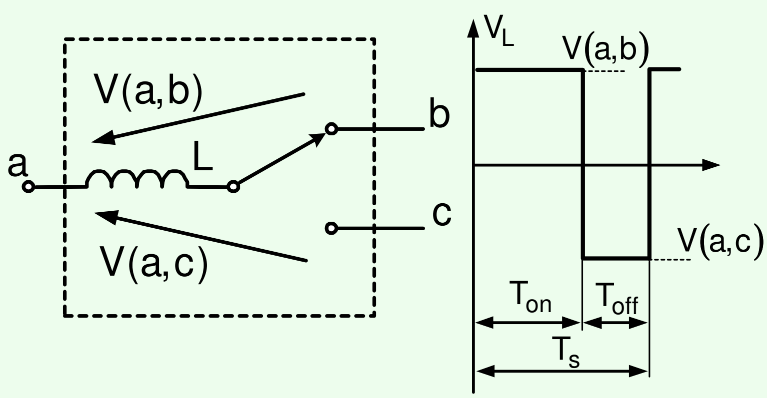
I_L derivation

$$\frac{dI_L}{dt} = \frac{V}{L} \quad \Rightarrow \quad \frac{d\langle I_L \rangle}{dt} = \frac{\langle V \rangle}{L}$$

$$\langle X \rangle = \bar{X} = \text{Average value}$$



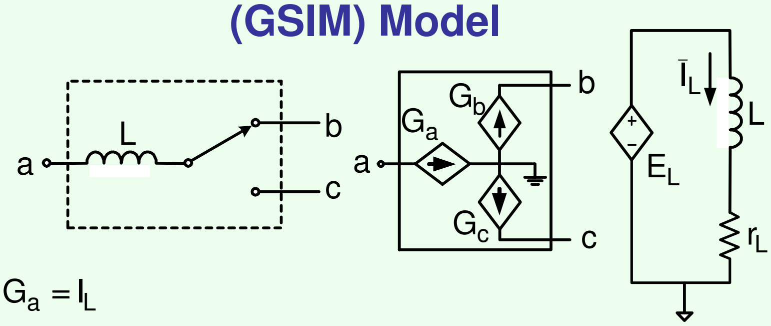
Average inductor voltage



$$\bar{V}_L = \frac{V(a,b) \cdot T_{on} + V(a,c) \cdot T_{off}}{T_S} =$$

$$= V(a,b) \cdot D_{on} + V(a,c) \cdot D_{off}$$

The Generalized Switched Inductor Model (GSIM) Model



$G_a = I_L$

$G_b = I_L \cdot D_{on}$

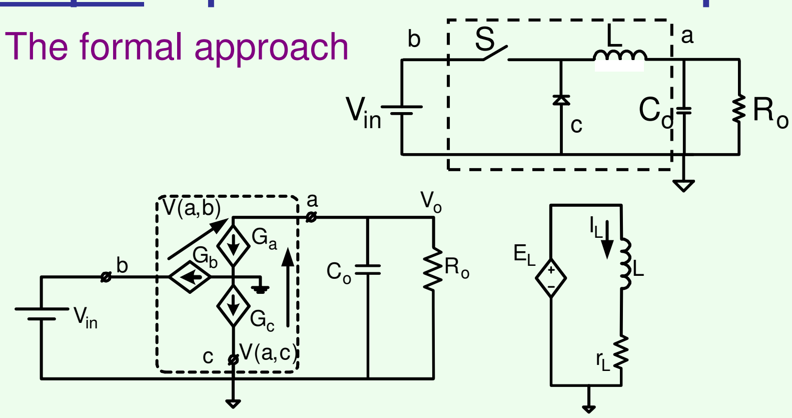
$G_c = I_L \cdot D_{off}$

$\bar{V}_L = V(a,b) \cdot D_{on} + V(a,c) \cdot D_{off}$

Topology independent !

Example: Implementation in Buck Topology

1. The formal approach

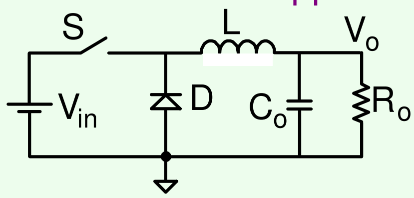


$\mathbf{G_a = I(L) \quad G_b = I(L) \cdot D_{on} \quad G_c = I(L) \cdot D_{off}}$

$\mathbf{E_L = [V_0 - V_{in}] \cdot D_{on} + [V_0 - 0] \cdot D_{off}}$

Implementation in Buck Topology

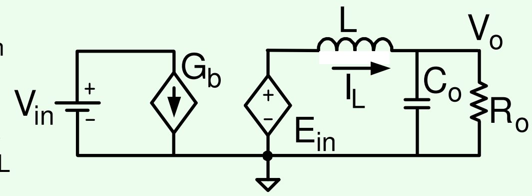
2. The intuitive approach - by inspection



$E_{in} = V_{in} \cdot D_{on}$

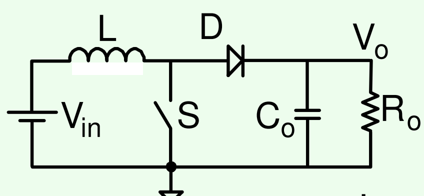
$G_b = \bar{I}_L \cdot D_{on}$

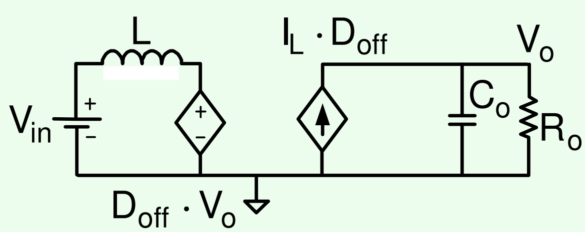
$E_{in} + V_o \rightarrow \overline{V}_L$



Polarity: (voltage and current sources) selected by inspection

Boost



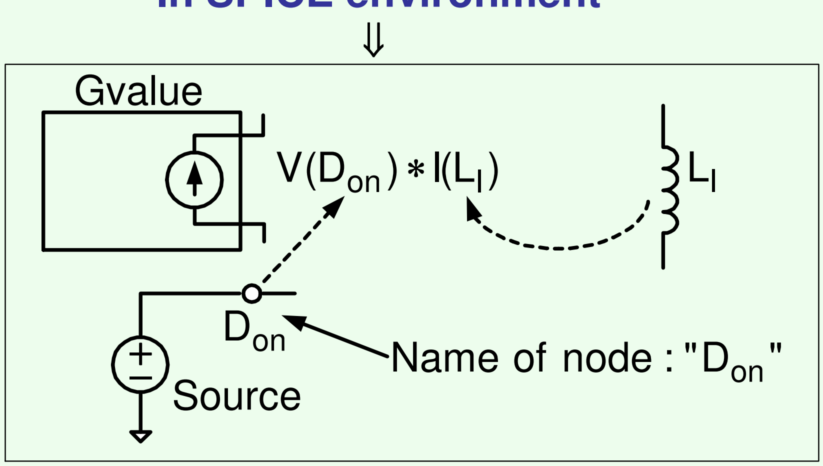


- Emulate average voltage on inductor
- Create I_L dependent current sources

Making the model SPICE compatible

I_L and D_{ON} are time dependent Variables $\{I_L(t), D_{ON}(t)\}$
D_{ON} is not an electrical variable

In SPICE environment



D_{on} is coded into voltage

Running SPICE simulation

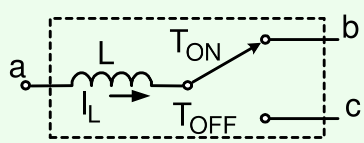
DC (steady state points) - as is

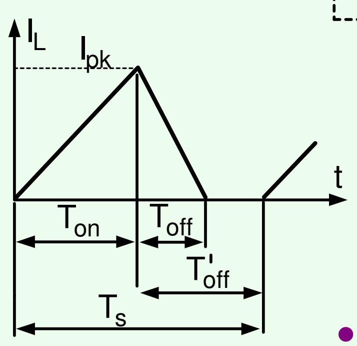
TRAN (time domain) - as is

AC (small signal) - as is

- Linearization is carried out by simulator !

Discontinuous Model (DCM)



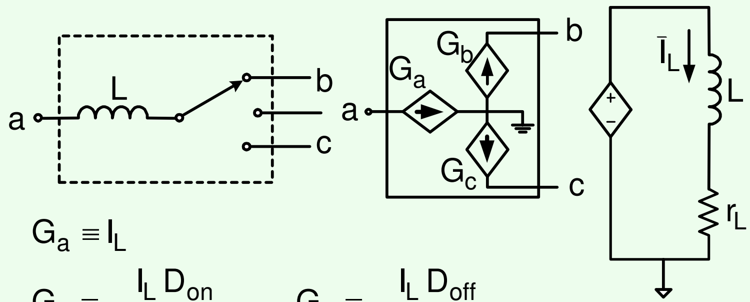


$$T'_{off} = T_s - T_{on}$$

$$D'_{off} = \frac{T_s - T_N}{T_s} = 1 - D_{on}$$

- **$D_{off} \neq 1 - D_{on}$**

The combined DCM / CCM model



$$G_a \equiv I_L$$

$$G_b \equiv \frac{I_L D_{on}}{D_{on} + D_{off}} \qquad G_c \equiv \frac{I_L D_{off}}{D_{on} + D_{off}}$$

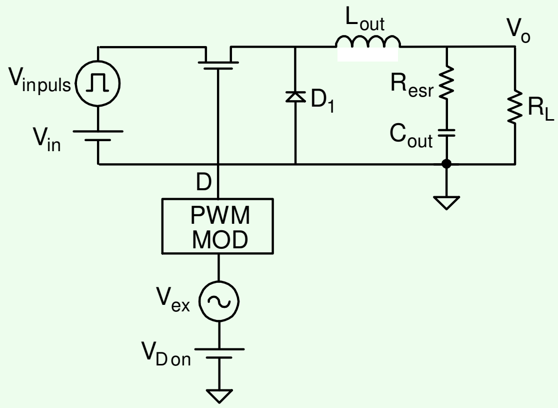
$$V_L = V(a,b) D_{on} + V(a,c) D_{off}$$

$$D_{off} = \min\left\{(1 - D_{on}),\ \left(\frac{2 I_L L f_s}{V(a,b) D_{on}} - D_{on}\right)\right\}$$

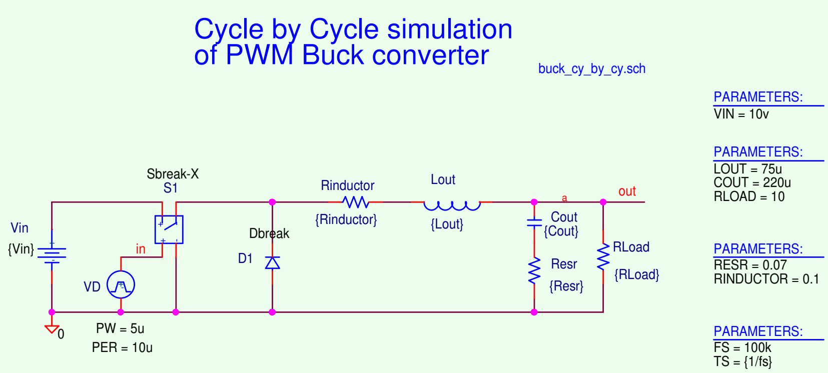
Synchronous Power Stages (diode replaced by switch)

- Only two stated for switched inductor: open and closed
- No third state as in DCM
- Use CCM model

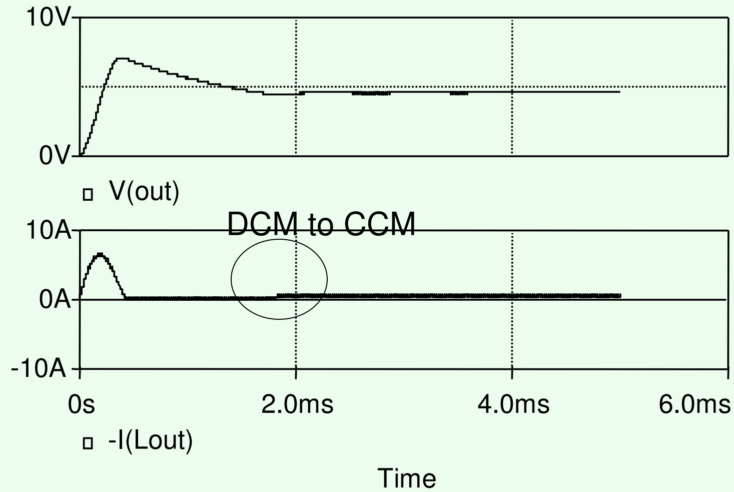
Example: Buck Converter



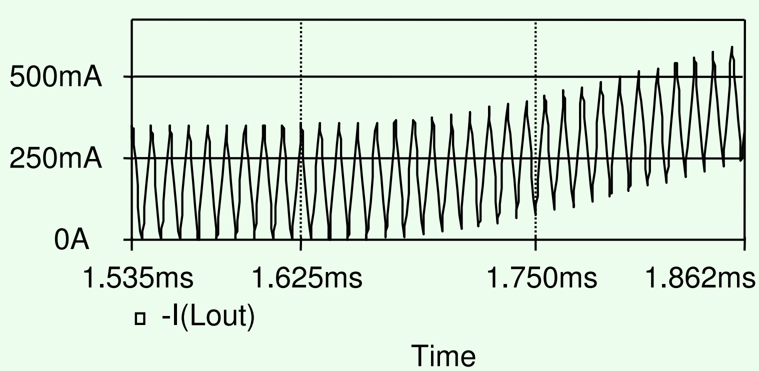
File: Buck_cy_by_cy.OPJ



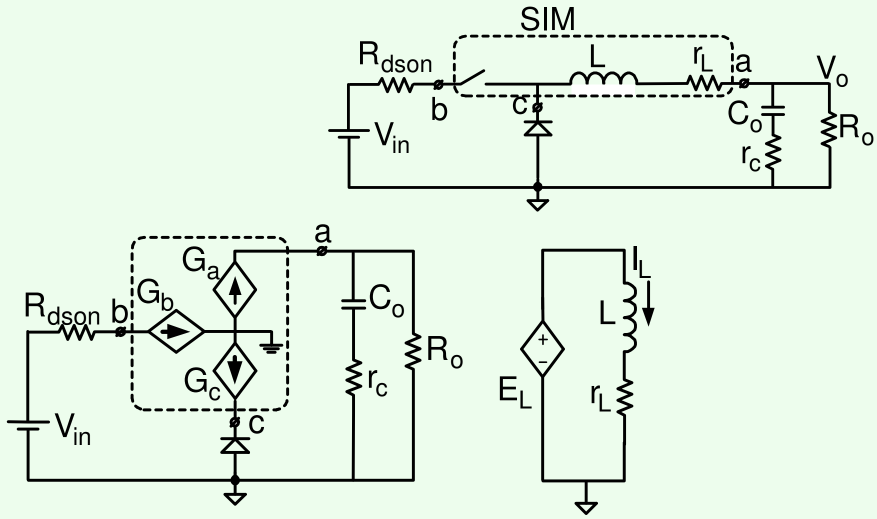
Power Start-Up at Constant D_{on}



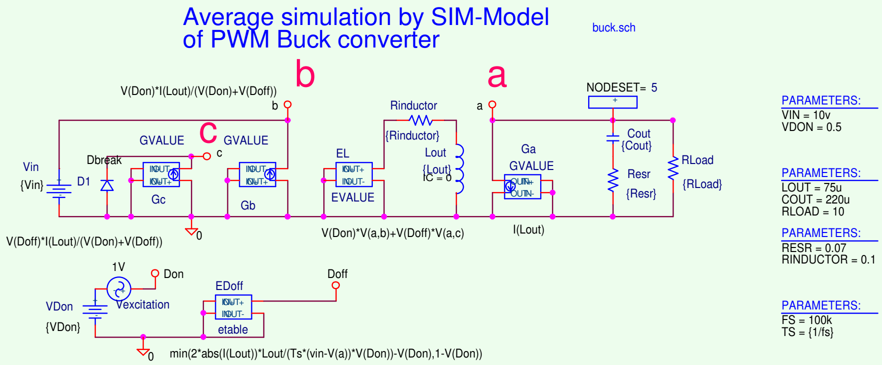
Zooming up



Average model

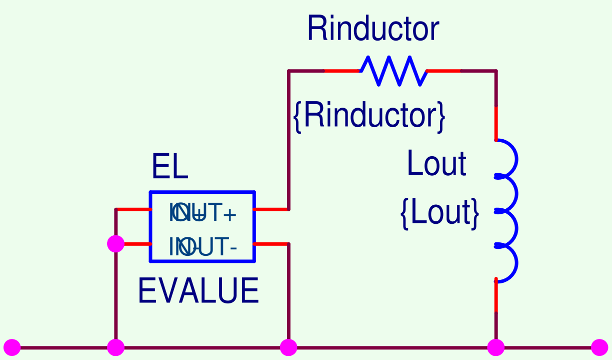


File: Buck.OPJ



- D_{on} coded into voltage
- D_{off} for CCM/DCM

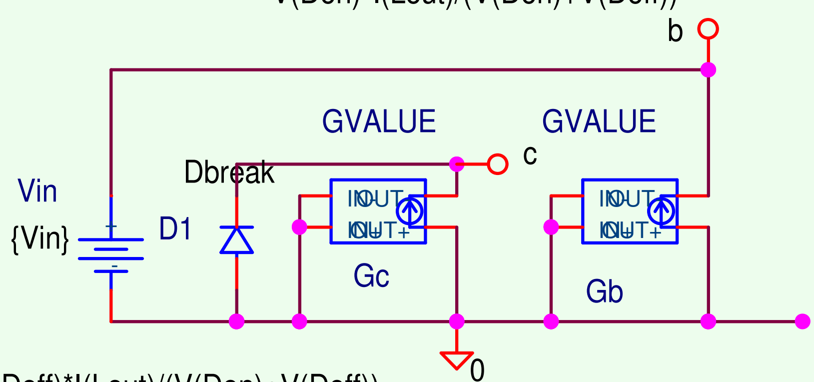
Inductor



V(Don)*V(a,b)+V(Doff)*V(a,c)

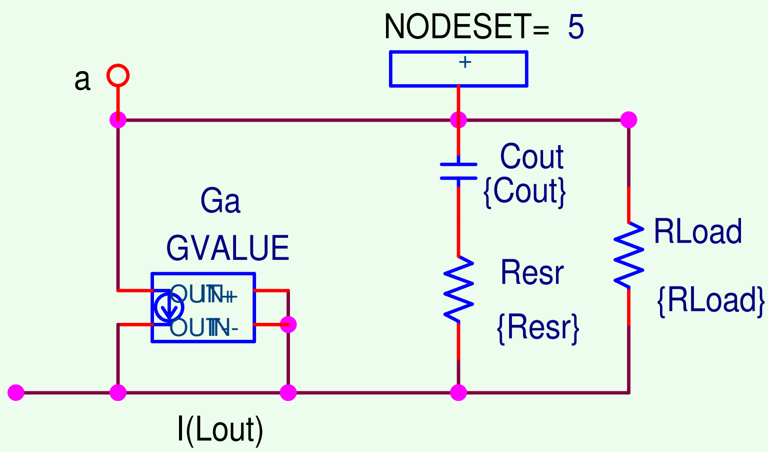
Input side

V(Don)*I(Lout)/(V(Don)+V(Doff))

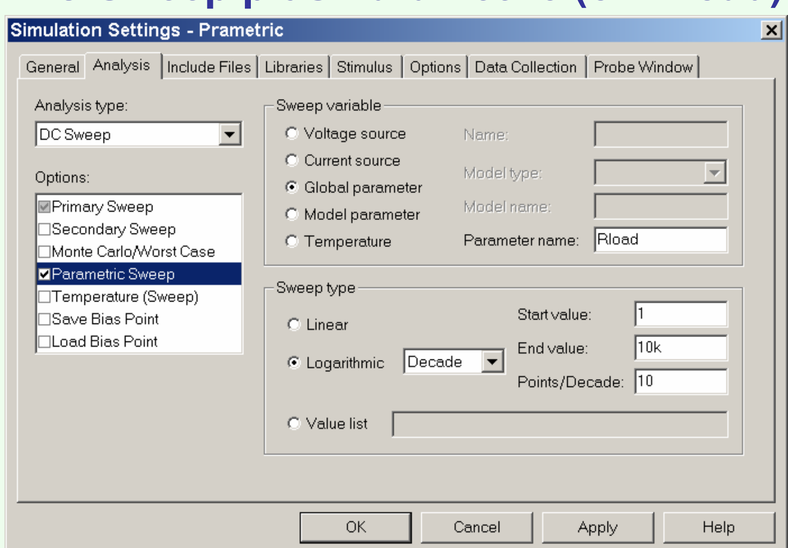


V(Doff)*I(Lout)/(V(Don)+V(Doff))

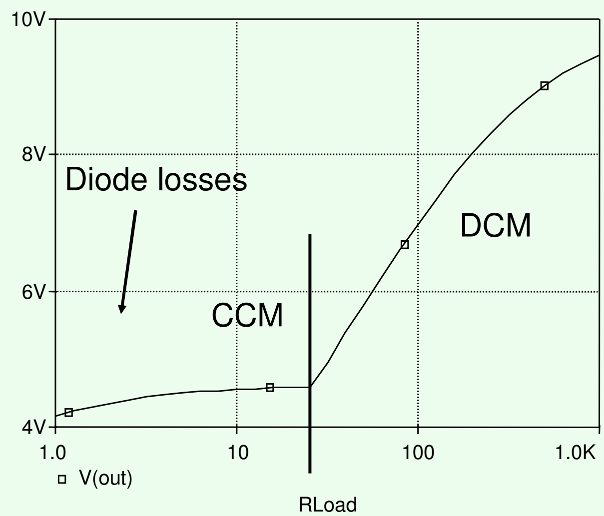
Output side



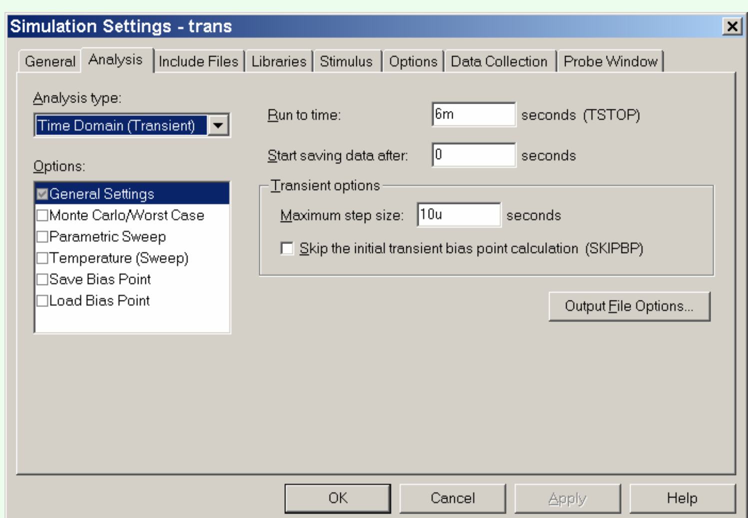
DC Sweep plus Parametric (on Rload)



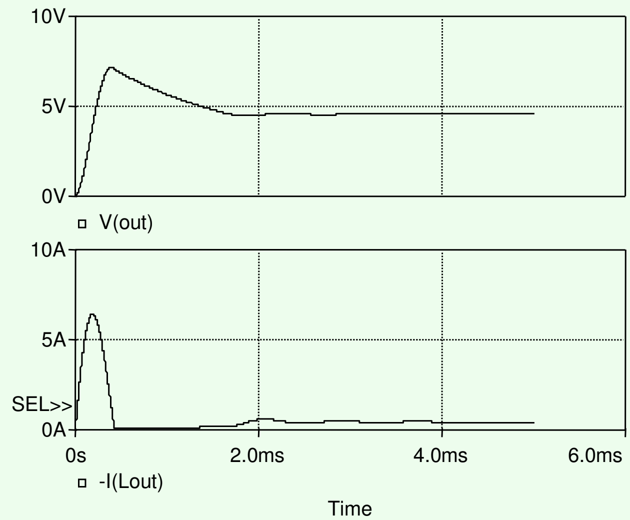
Sweeping R_{load} Constant D_{on}



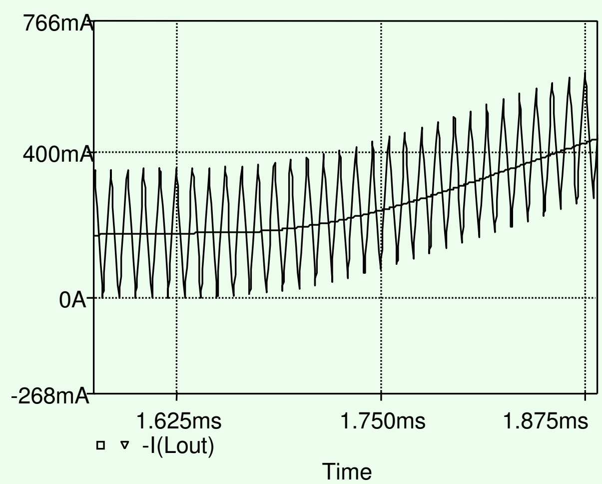
Transient Analysis –Power Turn-On



Power Start-Up at Constant D_{on}

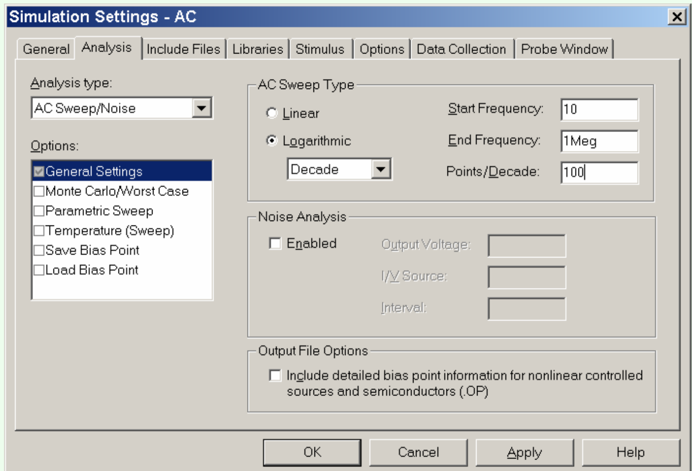


Comparing Cycle-by-Cycle to Average Simulation



AC Analysis

The Real Strength of Average Simulation



Linearization

- The circuit is linearized by simulator (elements, devices and expressions)
- Numerical linearization !
  e.g. a source f(x,y,z) is replaced by:

$$\frac{f(X+\Delta X,Y,Z)-f(X,Y,Z)}{\Delta X}x$$
$$+\frac{f(X,Y+\Delta Y,Z)-f(X,Y,Z)}{\Delta Y}y$$
$$+\frac{f(X,Y,Z+\Delta Z)-f(X,Y,Z)}{\Delta Z}z$$

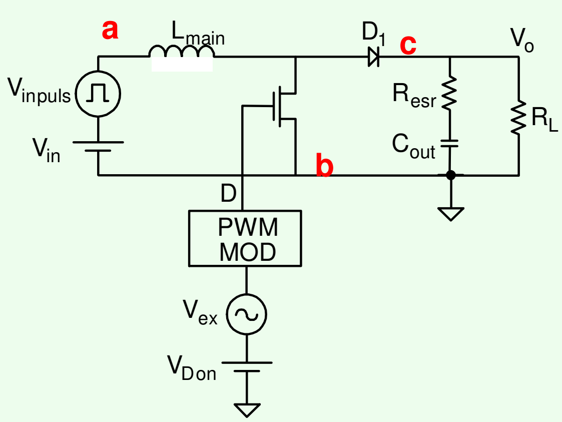
- Transparent to user

PSpice simulations examples

Buck Average

Buck Cy by Cy

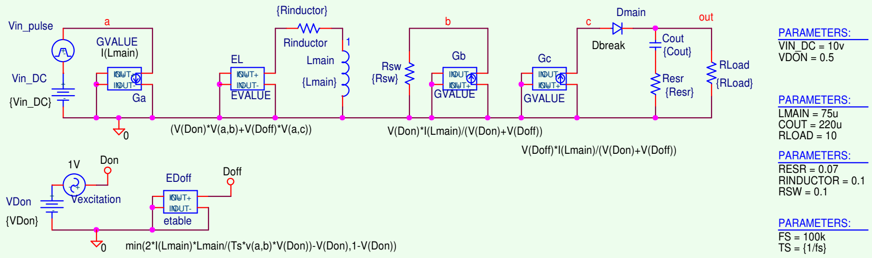
Boost

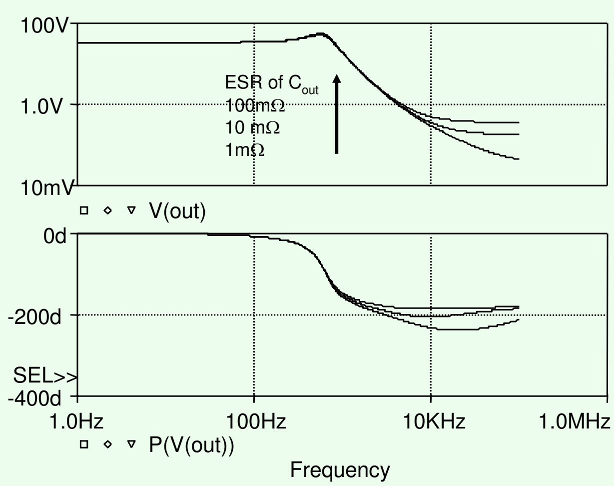


Boost Simulation

SIM-Model under CCM & DCM
for PWM Boost converter

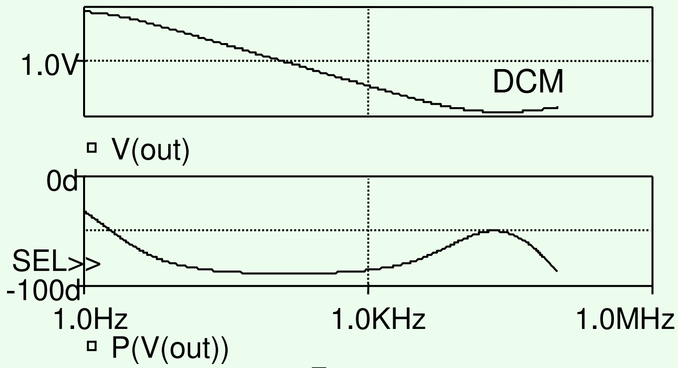
Boost.sch





$R_{Load} = 10\Omega$

DCM

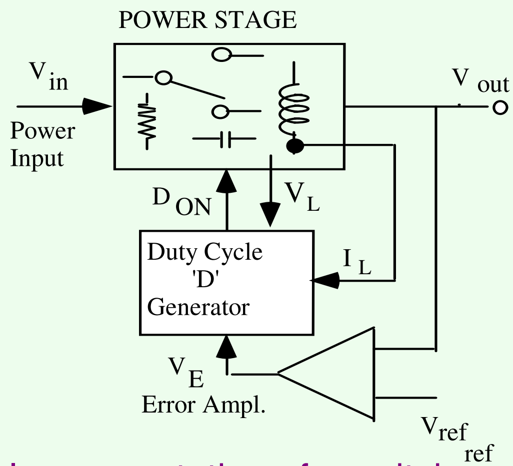


R_{Load} = 1000Ohm

PSpice simulation example

Boost simulation

Modulators – The Duty Cycle Generators

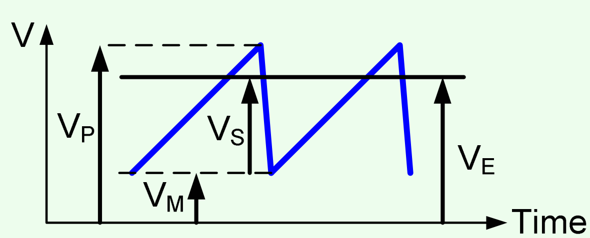


- General representation of a switch mode DC-DC converter

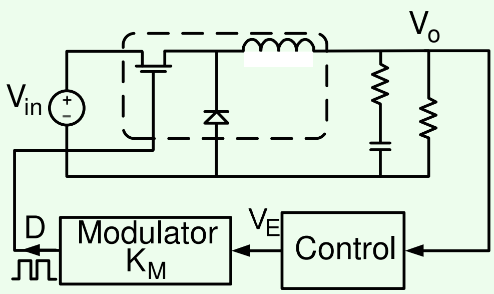
PWM MODULATOR - Voltage Mode

$$\frac{D}{V_e} = K_M\,(\text{voltage mode}) = \frac{V_E - V_M}{V_P - V_M}$$

$$\frac{d}{V_e} = \frac{v_e}{V_P \cdot V_M}$$



Coding



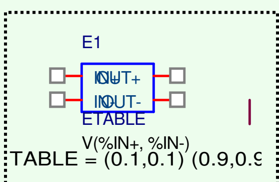
$$K_M\,(\text{voltage mode}) = \frac{V_E - V_M}{V_p - V_M}$$

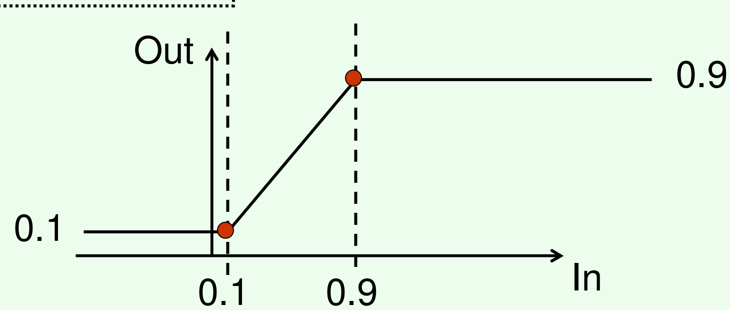
D coded into voltage

$0 \le V_D \le 1$

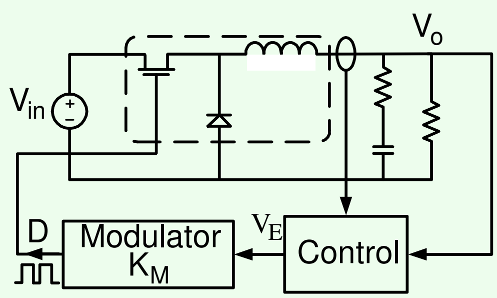
Duty Cycle Limiter

- Behavioral dependent source ETABLE



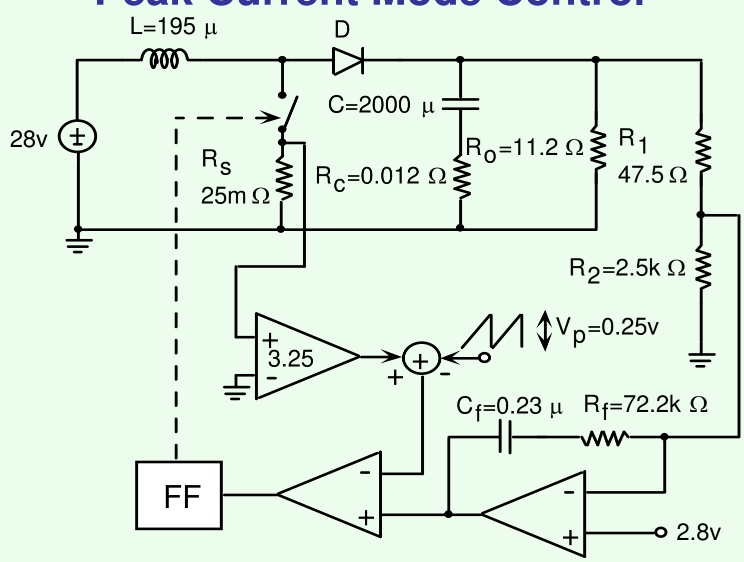


Average Current Mode



- V_E is a function of V_o and I_L
- ‘Control’ is the original analog circuit
- Same modulator as in voltage mode

Peak Current Mode Control



Current Mode CCM

$$EDon = \frac{V(Ve) - KS\dfrac{|I(L)|}{V(Don)+V(Doff)}}{TS\left(MC + KS\dfrac{V(a,b)}{2L}\right)}$$

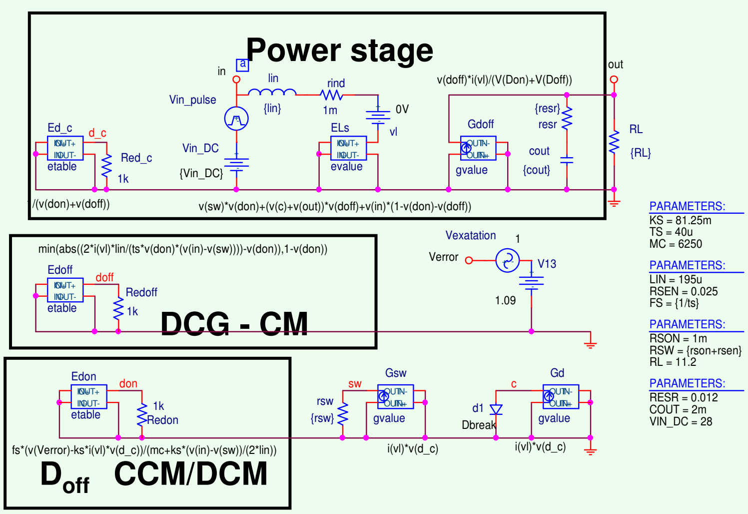
V(V)
KS = Current Loop Gain
MC = Slope Compensation
TS = Switching Period
L = Inductance of main inductor
|I(L)| = Average inductor current

If your can write an expression, it can be modeled !

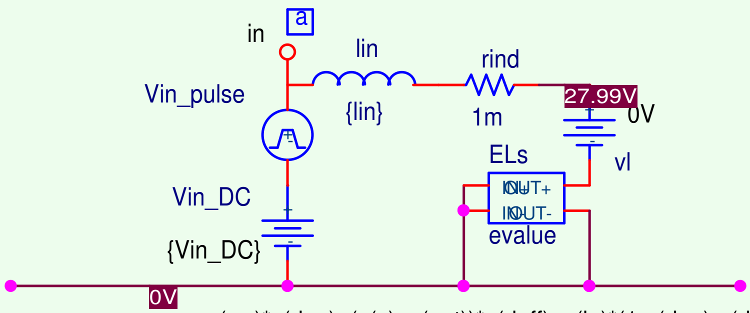
SIM-Model under CCM & DCM
for Current-Mode PWM Boost converter

File: CM-Boost.opj

Schematic file name: CM-Boost\CM-Boost.sch



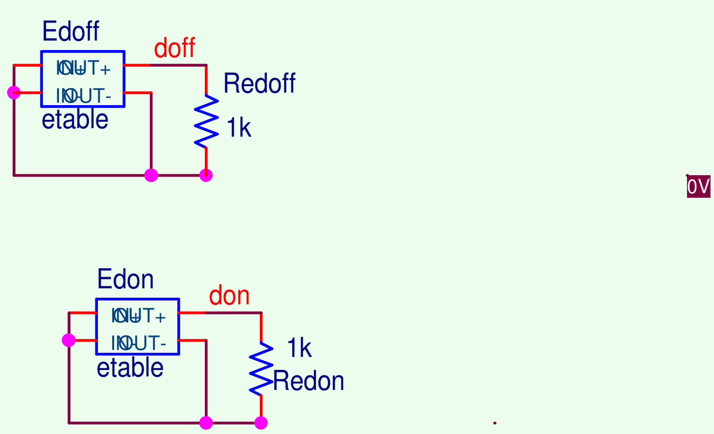
Inductor



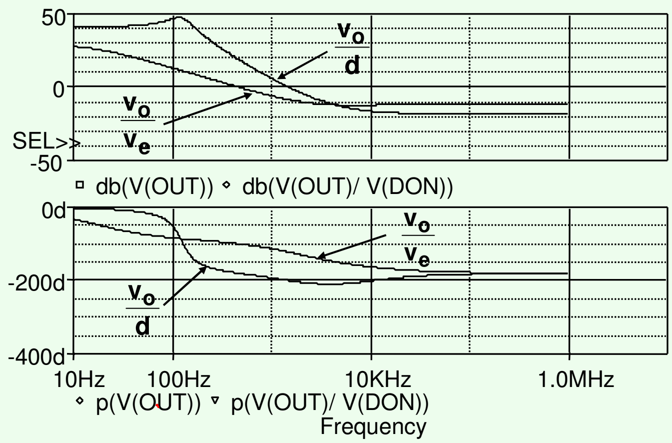
v(sw)*v(don)+(v(c)+v(out))*v(doff)+v(in)*(1-v(don)-v(doff))

Duty Cycle Generator

min(abs((2*i(vl)*lin/(ts*v(don)*(v(in)-v(sw))))-v(don)),1-v(don))



fs*(v(Verror)-ks*i(vl)*v(d_c))/(mc+ks*(v(in)-v(sw))/(2*lin))



V(out)/V(Don) as normal
V(out)/V(Verror) lower order

PSpice simulation example

CM-Boost

Models of IC Controllers

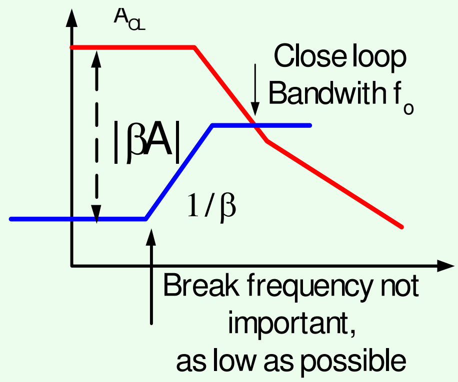
- Vendors do not supply simulation models of IC controllers
- Large signal controllers' models are supplied with some simulators (e.g. PSIM)
- Average models (applicable for small signal analysis) are available from AEi
- It is easy to build your own behavioral average models (for control)

The Power Stage small-signal response

- A prerequisite for control design
- Can be obtained by analytical derivations/expressions
- By Simulation
  - On switched model (cycle by Cycle)
  - Average models

Feedback Loop Design of PWM Converters

1. Find A(f) of Power stage
2. Decide on f_0
3. Choose type of compensating network
4. Calculate feedback network



Make $|\beta A|$ as large as possible

The Relationship to PID

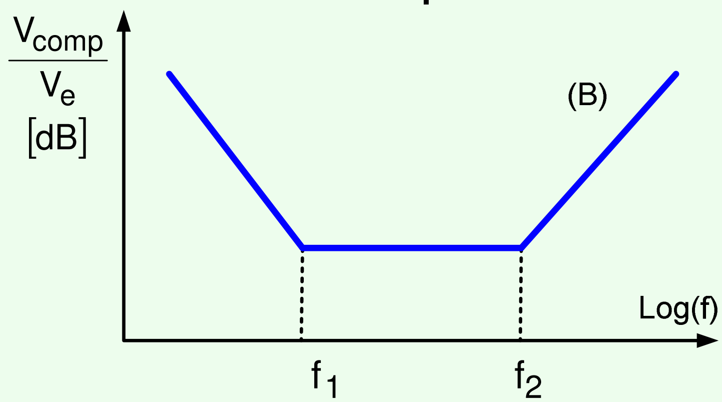
$$H(s) = \frac{v_{comp}}{v_e} = K_p + \frac{K_I}{s} + s \cdot K_d =$$

$$= \frac{K_d \cdot s^2 + K_p \cdot s + K_I}{s} = \frac{K_d}{K_I} \frac{(s+\omega_{z1}) \cdot (s+\omega_{z2})}{s}$$

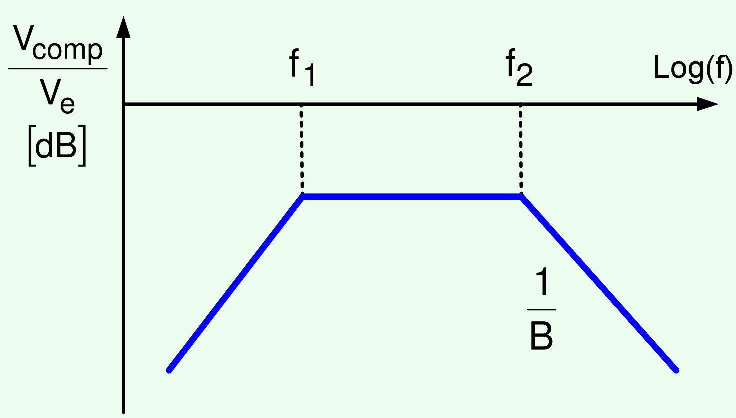
$$\omega_{z1,2} = \frac{-K_p \pm \sqrt{(K_p)^2 - 4K_d K_I}}{2K_d}$$

The Relationship to PID

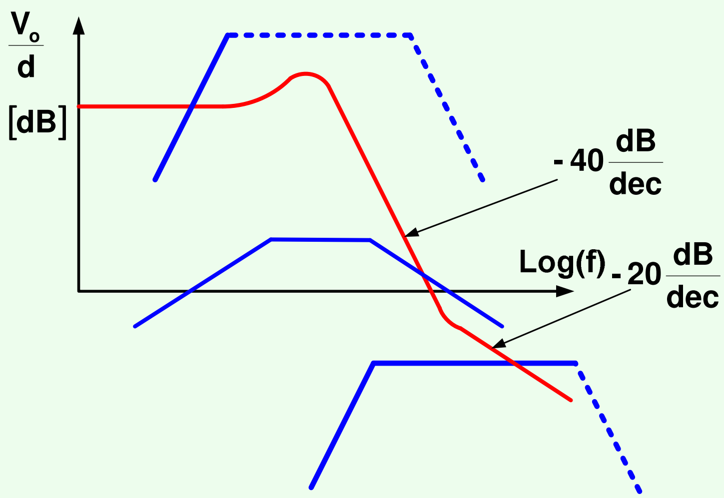
$$= \frac{K_d \cdot s^2 + K_p \cdot s + K_I}{s} = \frac{K_d}{K_I} \frac{(s+\omega_{z1}) \cdot (s+\omega_{z2})}{s}$$



The Relationship to PID



The Relationship to PID

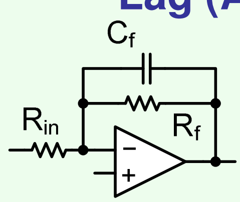


BW Limitations
(of LG, crossing of A and B)

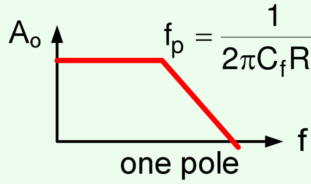
- PWM is a smapled data sysyem .
- Nyquist sampling theorem applies
- Cross over frequency f_o (A, B, LG) < $f_s/2$
- In practice f_o < 10 $f_s/2$

8. Analog compensator networks

Possible phase compensation schemes
Lag (A)

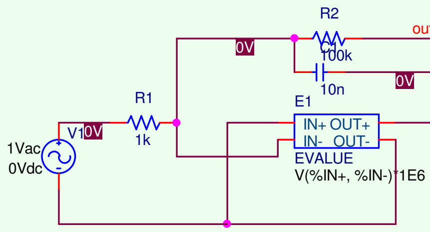


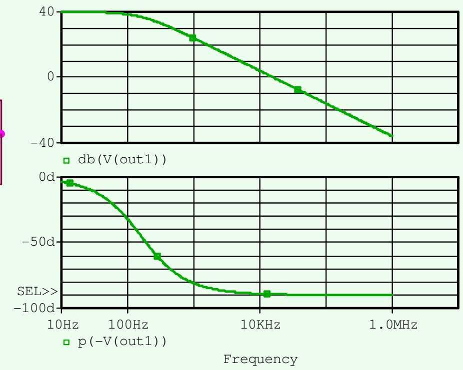
$$A_o = \frac{R_f}{R_{in}}$$



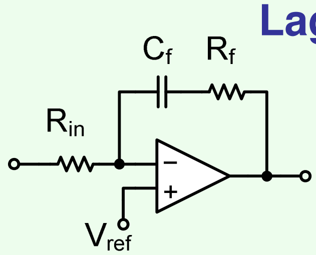
$$f_p = \frac{1}{2\pi C_f R_f}$$

Lag (B)





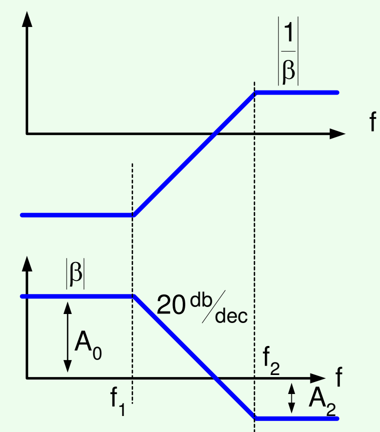
Lag – Lead (B)



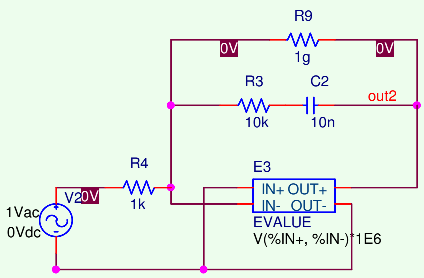
$$A_o = A_{OL}(\text{ampl.})$$

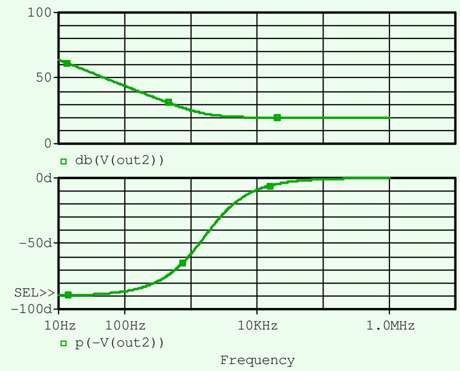
$$f_L = \frac{1}{2\pi C_f R_f}$$

$$A_2 = \frac{R_f}{R_{in}}$$



Lag-Lead (B)

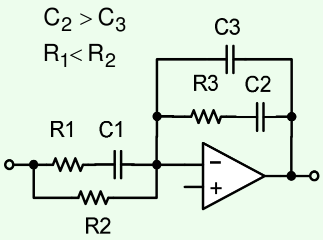


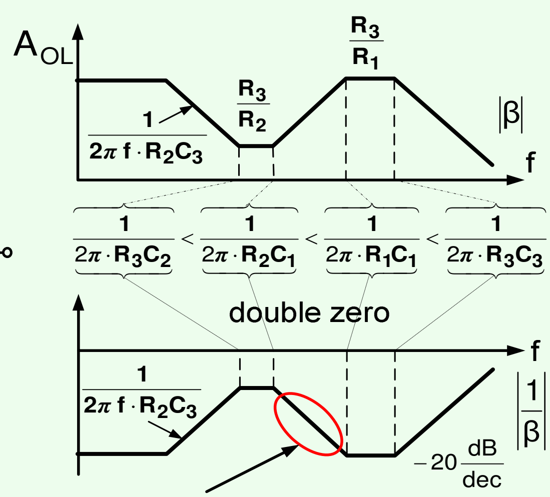


Double zero compensation scheme

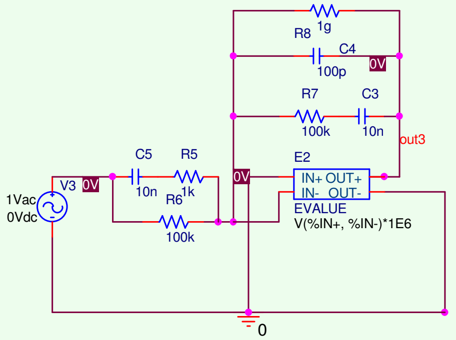
$C_2 > C_3$

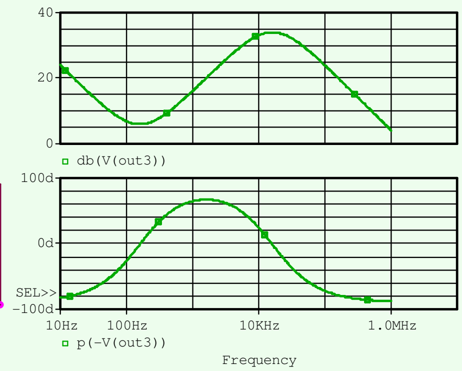
$R_1 < R_2$



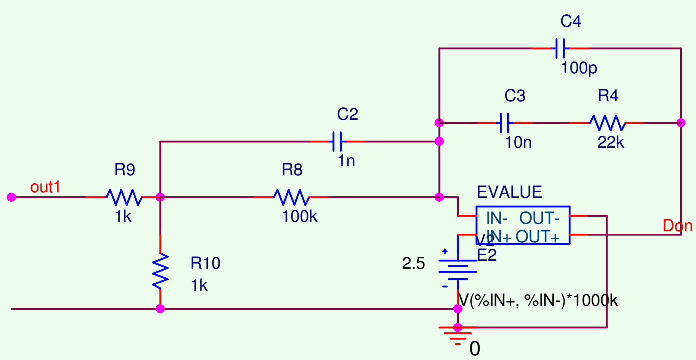


Double Zero (B)

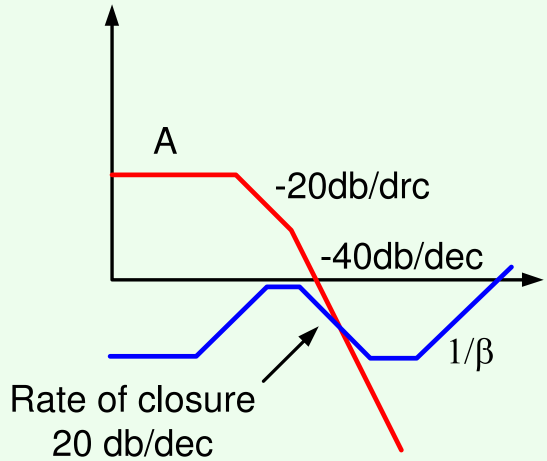




Double Zero- Alternative



Application of Double Zero Compensator

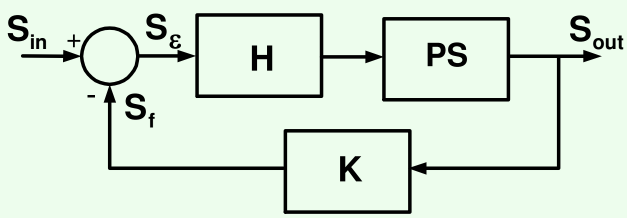


Phase advance by compensator

Voltage Mode Control Compensator Design Example

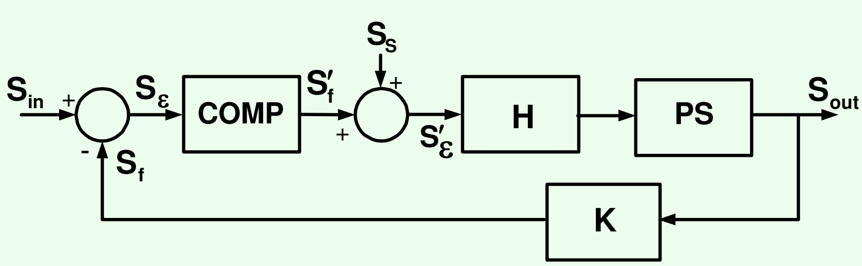
VM Regulator

Obtaining the Loop Gain by Simulation



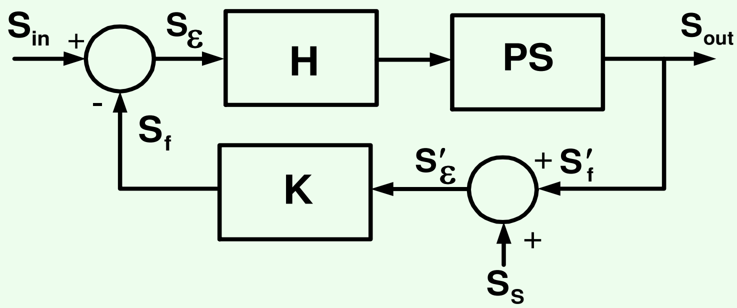
$$LG = \frac{S_f}{S_\varepsilon}$$

Loop Gain by Simulation



$$LG = \frac{S'_f}{S'_\varepsilon}$$

Loop Gain by Simulation

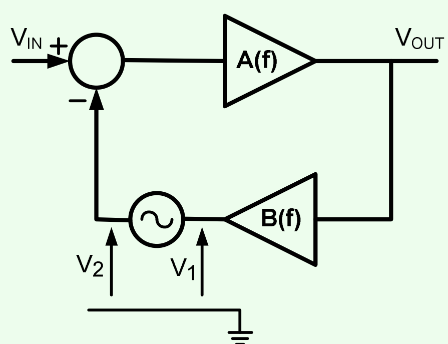


$$LG = \frac{S'_f}{S'_\varepsilon}$$

Loop-Gain

Getting Loop-Gain under closed loop response {A(f)*B(f)}

$V_{in}=0$



LG(f) = V1/V2

Rules for Getting Loop-Gain by Simulation

The relevant analysis is .AC

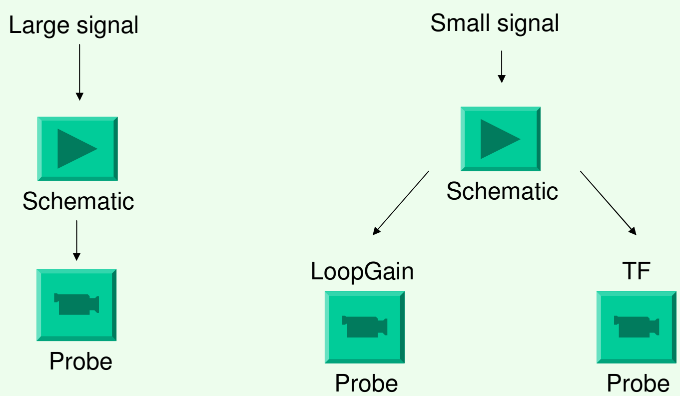
- Locate the AC source at the output of a low impedance device (could be real or behavioral)
- Set the AC value to any value (1 V is fine)
- Make sure that there are no other AC sources in the system
- Check bias point (.OUT file)
- Remember that the classical stability criteria take into account the phase reversal (180^0)

PSpice Simulation

VM Regulator

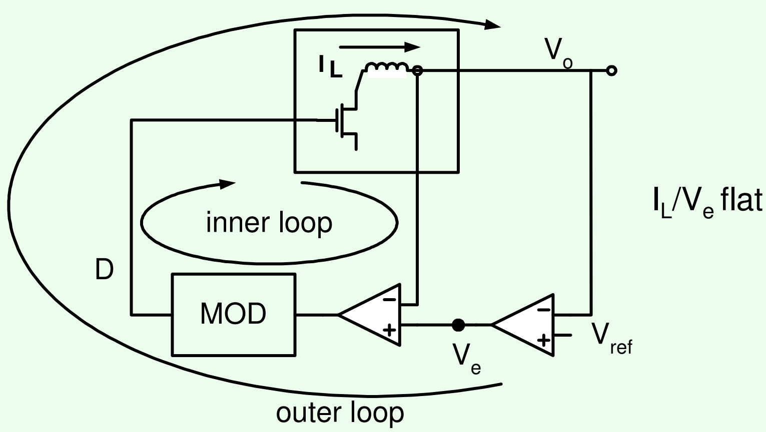
Prof. S. Ben-Yaakov , Control Design of PWM Converters [179]

PSIM Demonstration



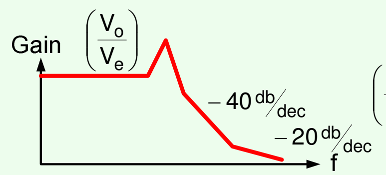
Prof. S. Ben-Yaakov , Control Design of PWM Converters [180]

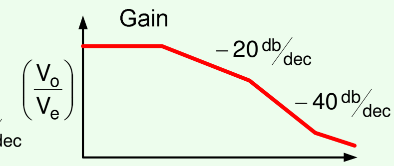
Peak and Average Current Mode



- **Two step design: inner loop and outer loop**

The advantages of current feedback (PCM or ACM)



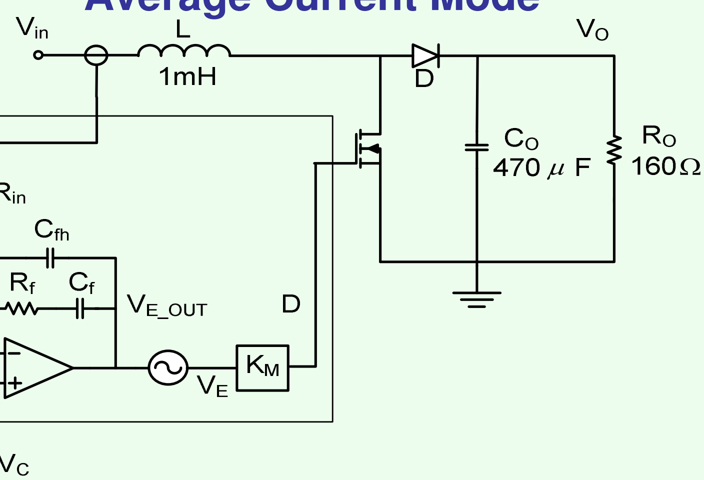


Typical power stage VM

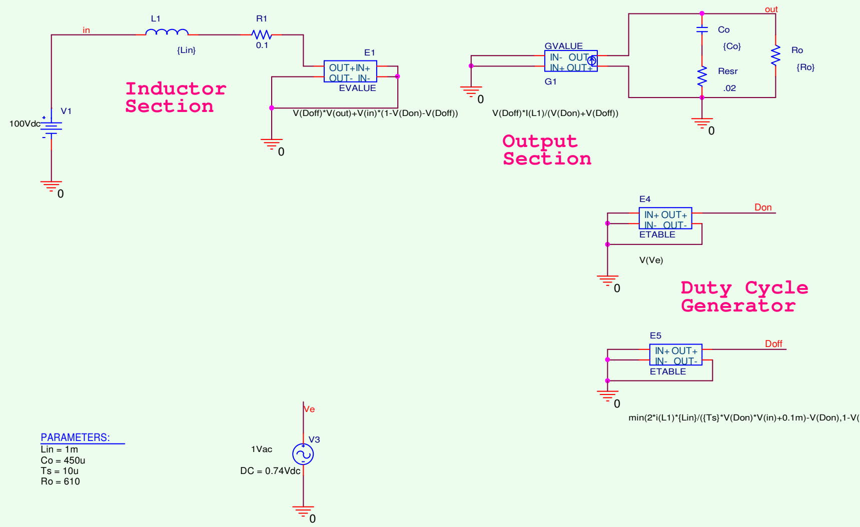
Same power stage (outer loop) with CM

- **With closed inner-loop**

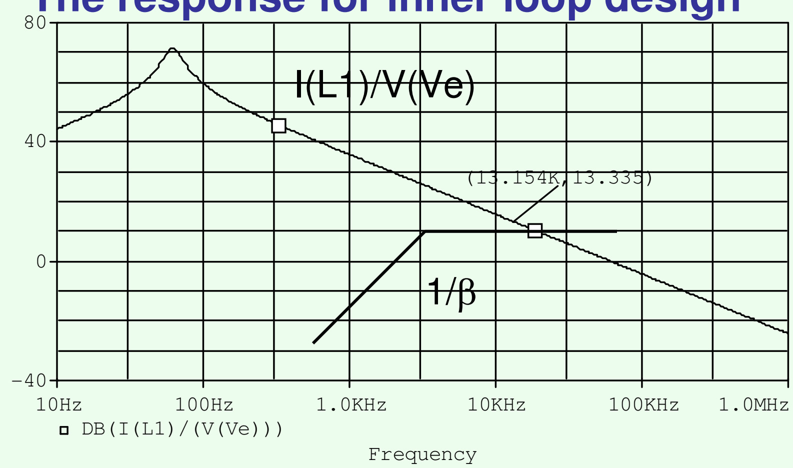
Inner Loop design
Average Current Mode



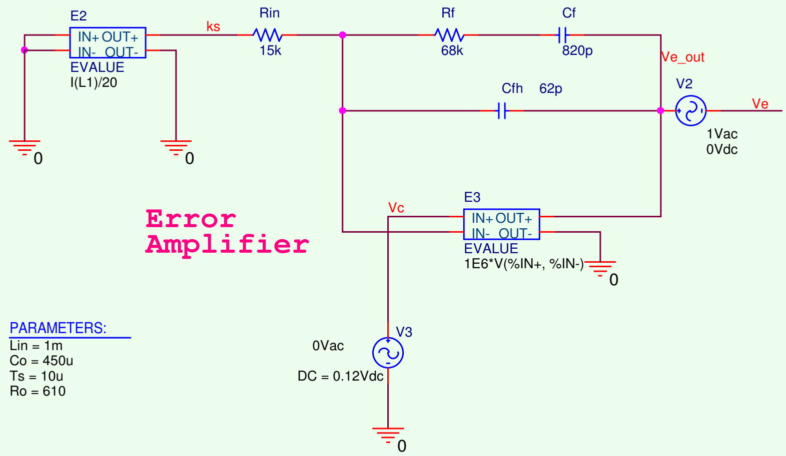
Vac = 1V ; Vc =Constant (operating point) ; KS= 1/20



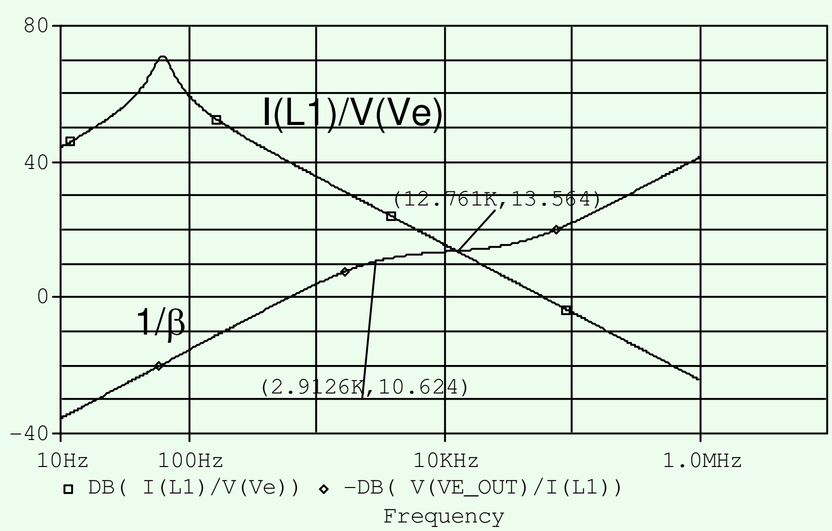
The response for inner loop design

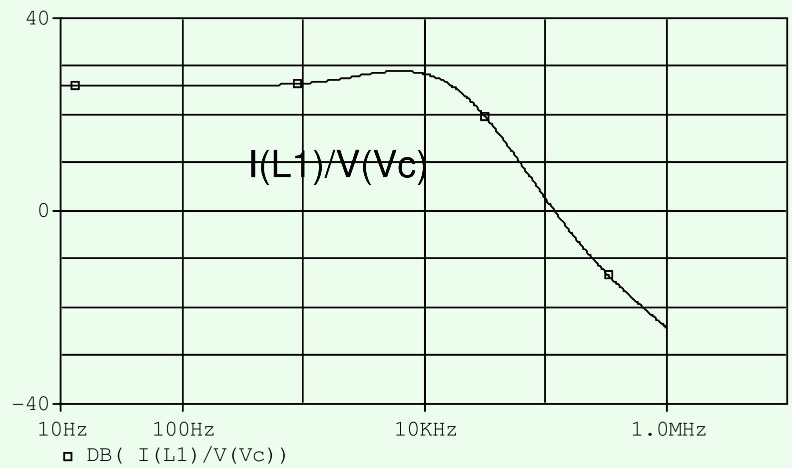


F=13kHz; Gain= -13.3db=0.22

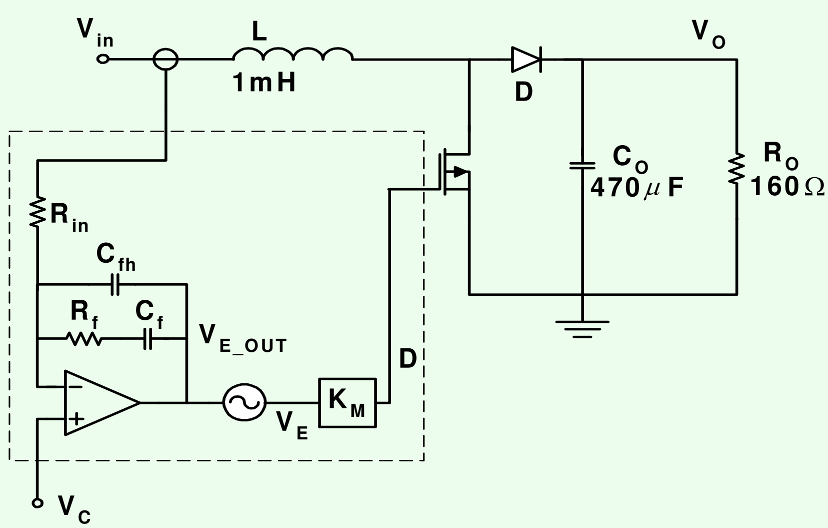


- The error amplifier (For KS =1/20)



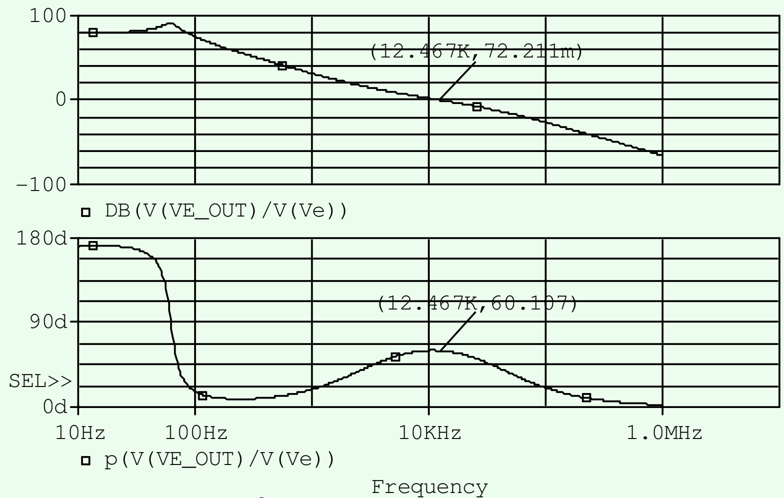


Closed inner Loop



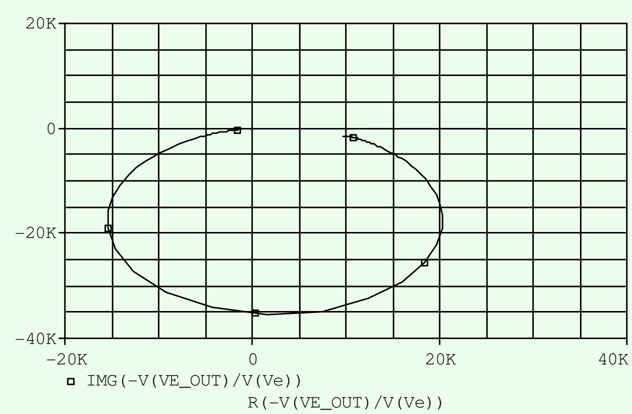
Vac = 1V ; Vc =Constant (operating point) ; KS= 1/20

LoopGain



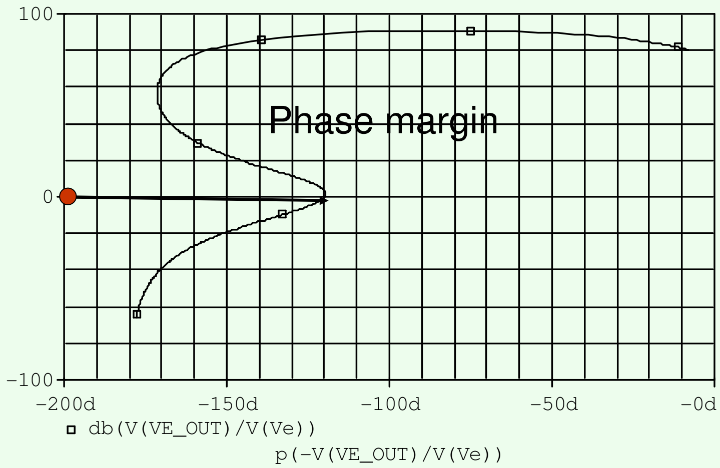
Phase margin 60^0

Nyquist Plot



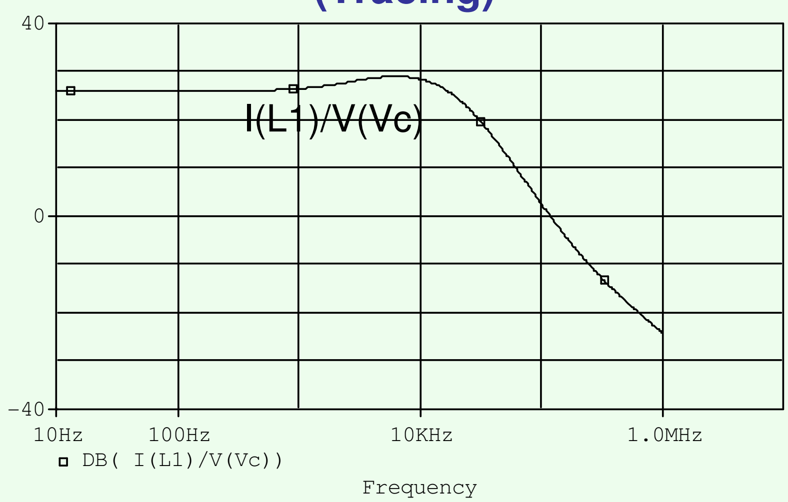
- Imaginary(LG) versus Real(LG)

Nichols Plot

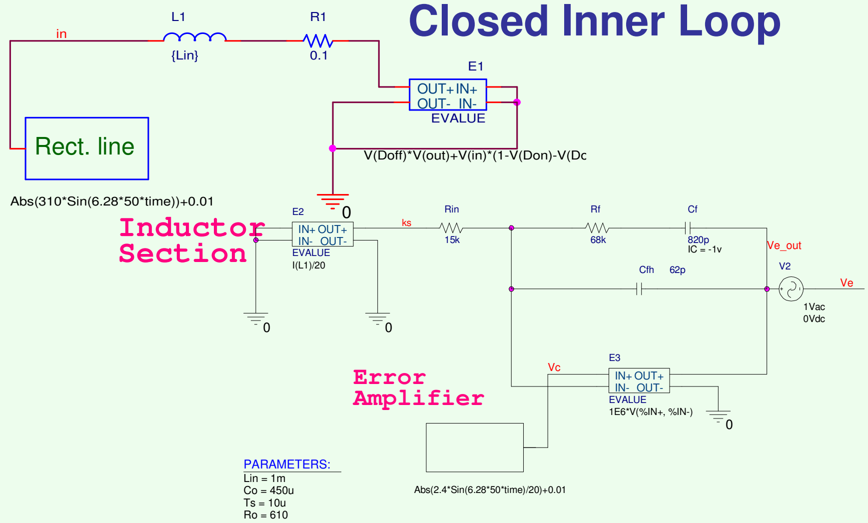


- |LG| versus Phase(LG)

Closed Inner Loop (Tracing)

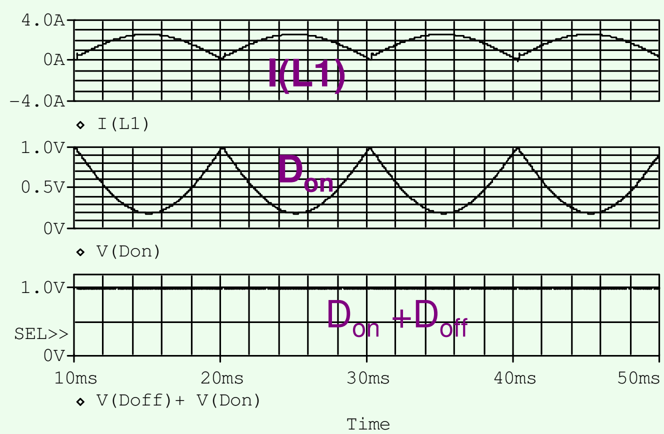


Closed Inner Loop



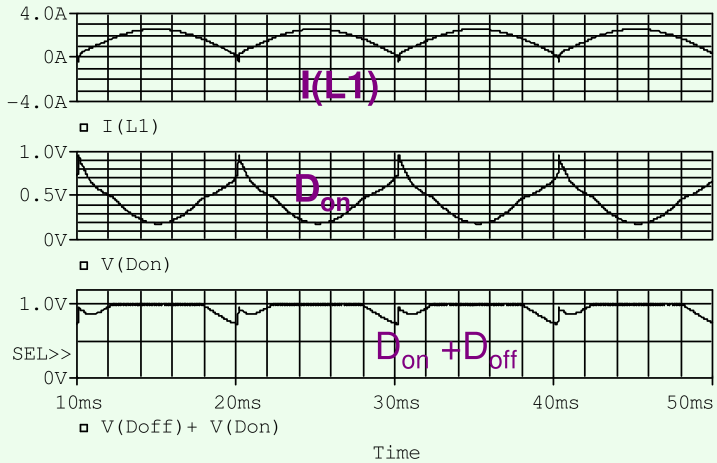
- Toward Power factor Correction (open loop)

Transient Simulation -CCM



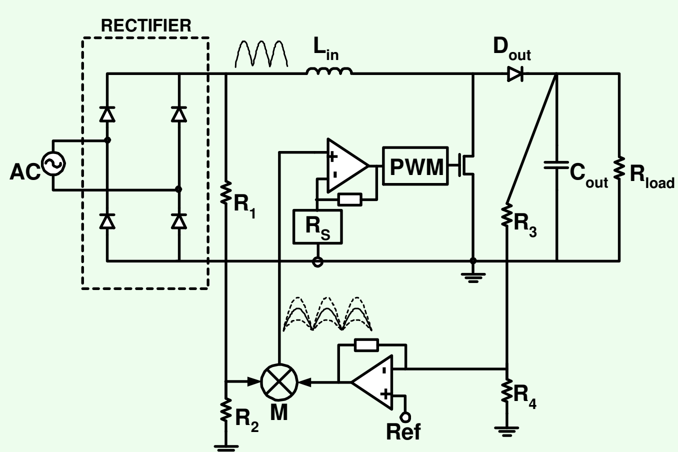
In CCM: Don+Doff = 1

Transient Simulation - CCM/DCM

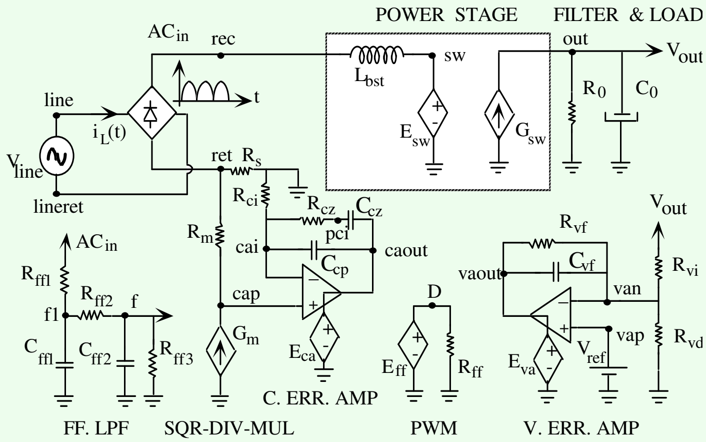


After changing L_m to 300μH

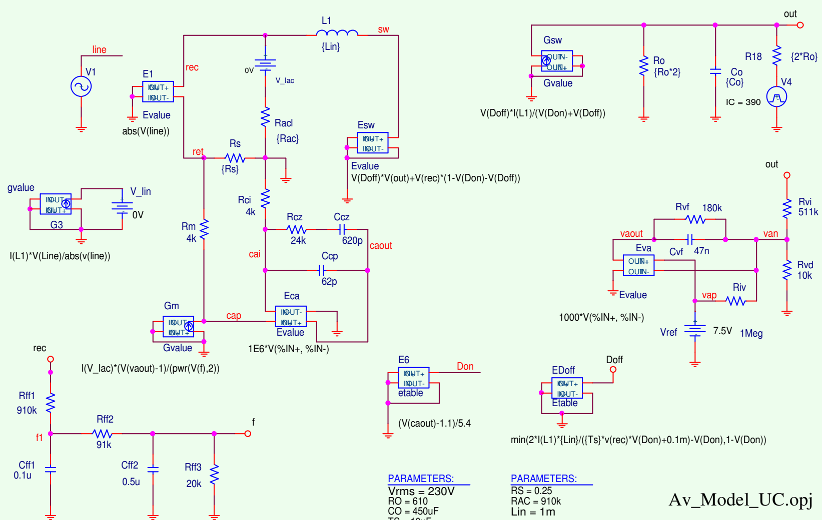
Three Loops Feedback PFC System (Conventional CCM)



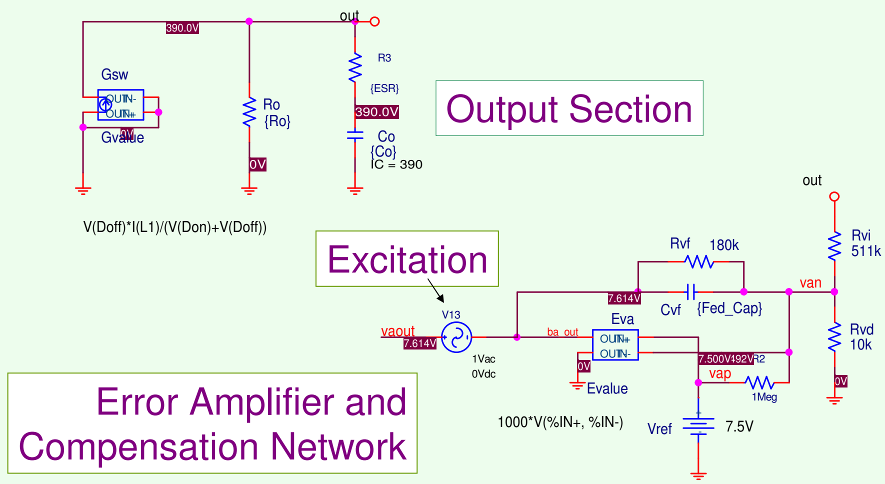
UC3854 Based Average Model



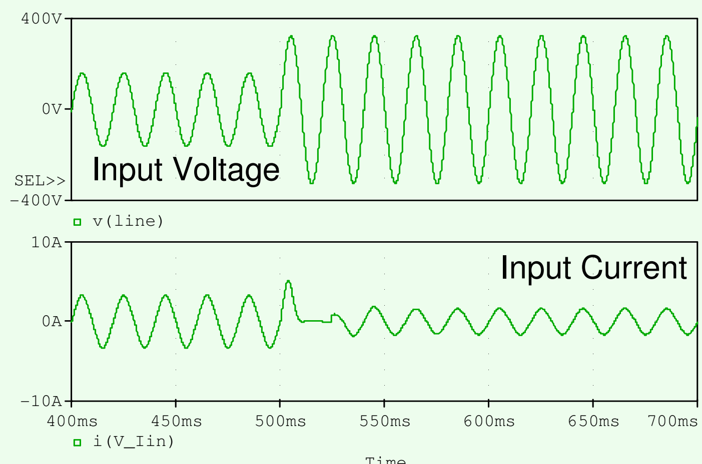
CCM - Based on UC3854



Voltage Control Loop

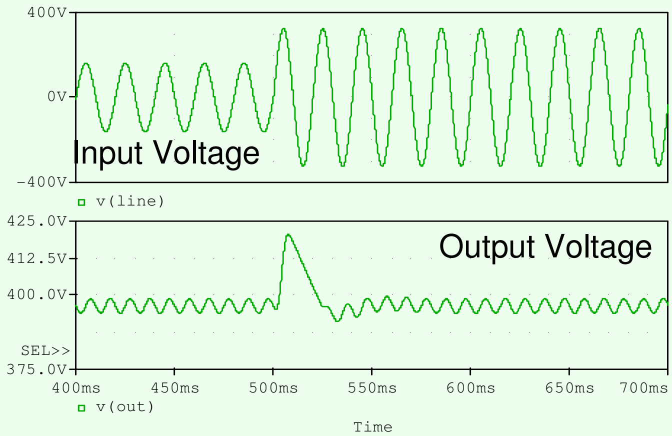


Input Voltage Step Response: 115Vrms to 230Vrms



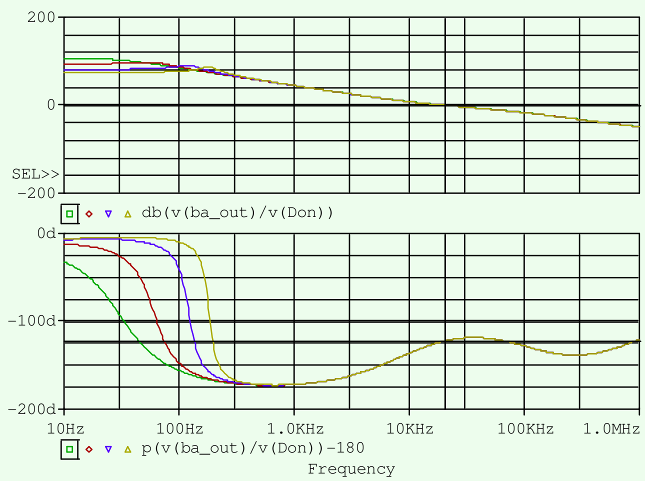
Pout=250W, Slew Rate=160V/mS

Input Voltage Step Response: 115Vrms to 230Vrms



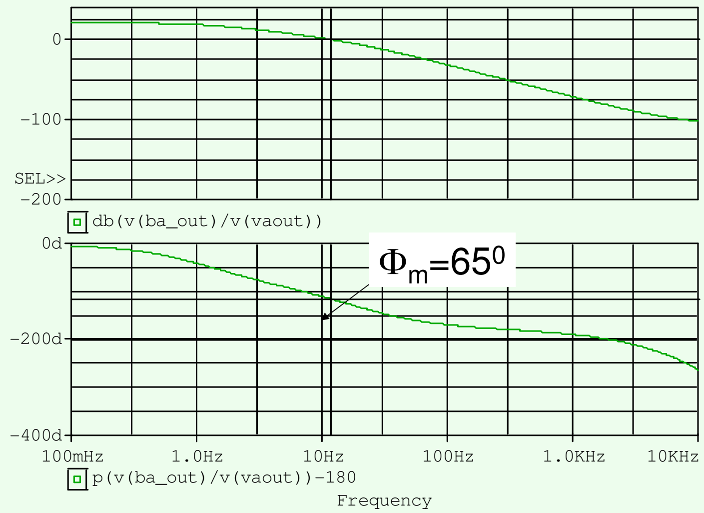
Pout=250W, Slew Rate=160V/mS

Current Loop Gain at Different Input Voltages



Vin=50V, 100V, 200V, 300V

Loop Gain of Voltage Control Loop



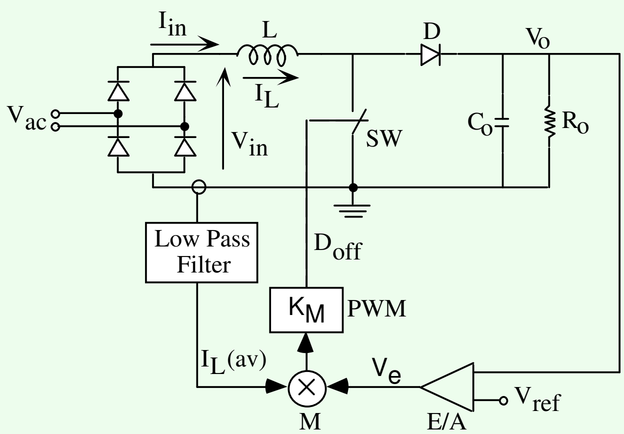
PSpice simulation

PFC-AC

PFC-TRAN

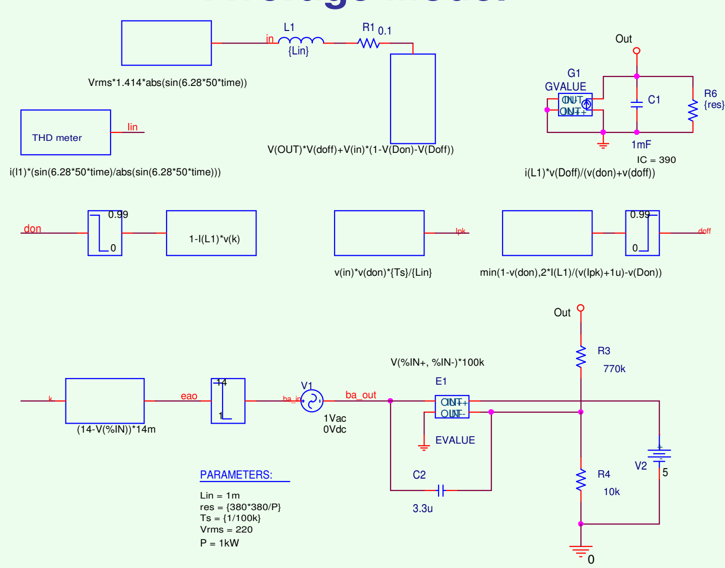
Prof. S. Ben-Yaakov , Control Design of PWM Converters **[205]**

CCM Control Concept with no Sensing of Input Voltage

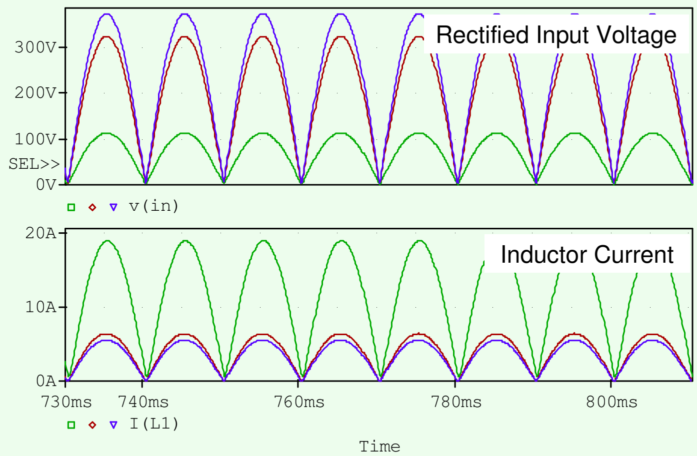


Prof. S. Ben-Yaakov , Control Design of PWM Converters **[206]**

Average Model

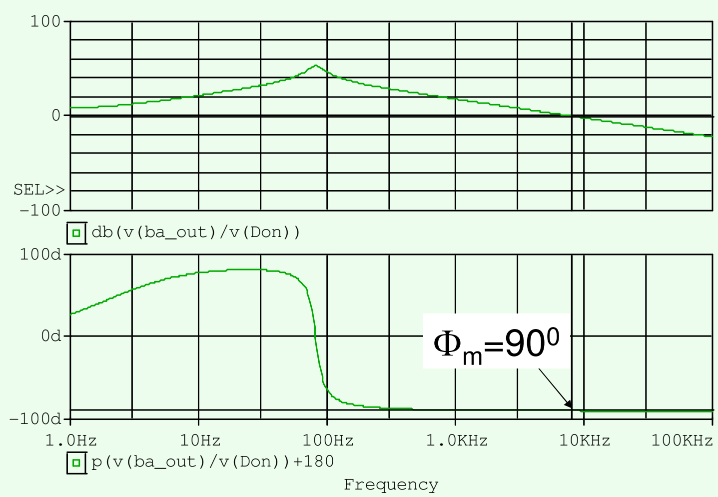


Input Behavior at Different Line Voltages

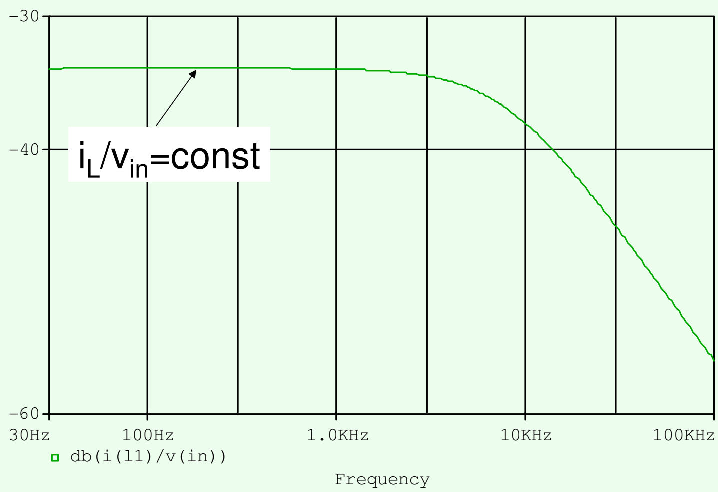


Pout=1kW, Vin=80Vrms, 230Vrms, 265Vrms

Loop Gain of Current Control Loop



Current Loop Transfer Function

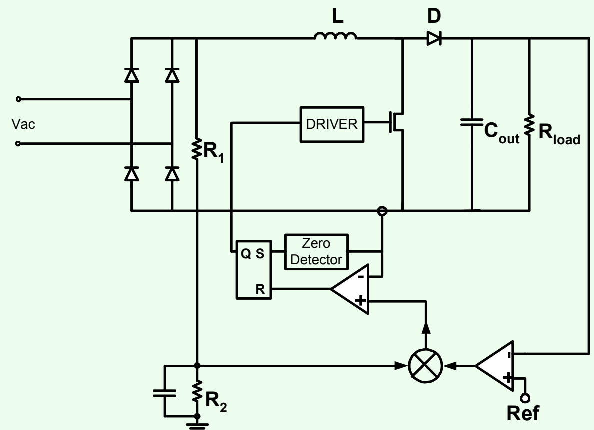


PSpice simulation

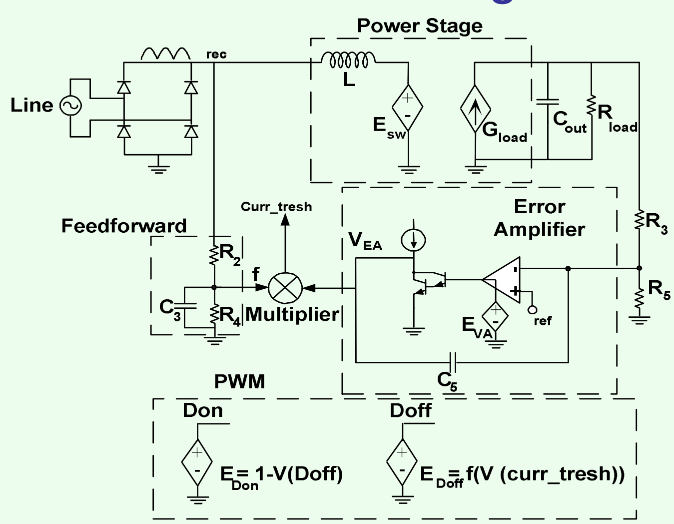
PFC_no_sens-AC

PFC_no_sens-TRAN

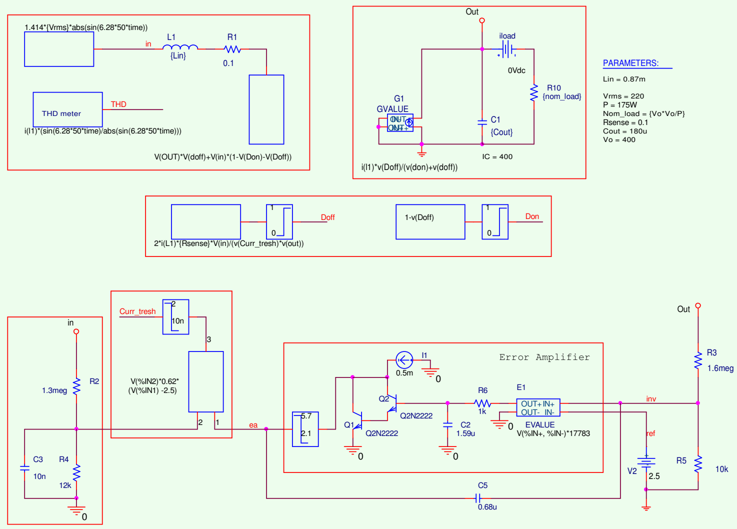
Conventional Border Line Control Method



MC33261 Based Average Model



MC33261 Based Average Model

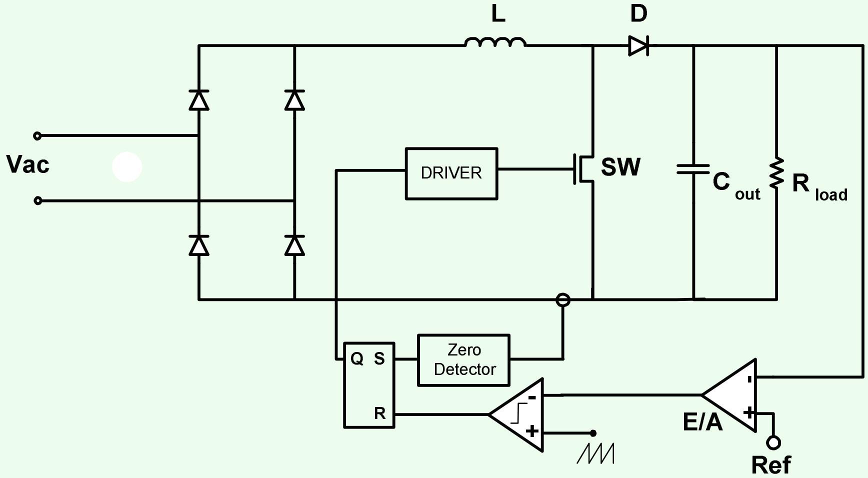


PSpice simulation

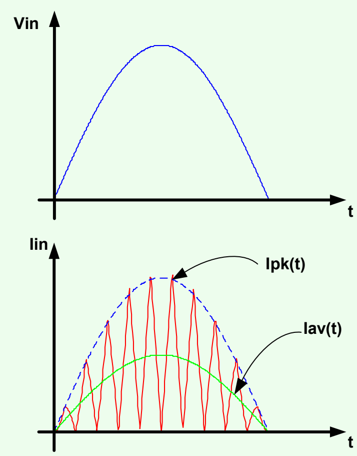
PFC_bord-AC

PFC_bord-TRAN

Border Line Control Concept with no Sensing of Input Voltage

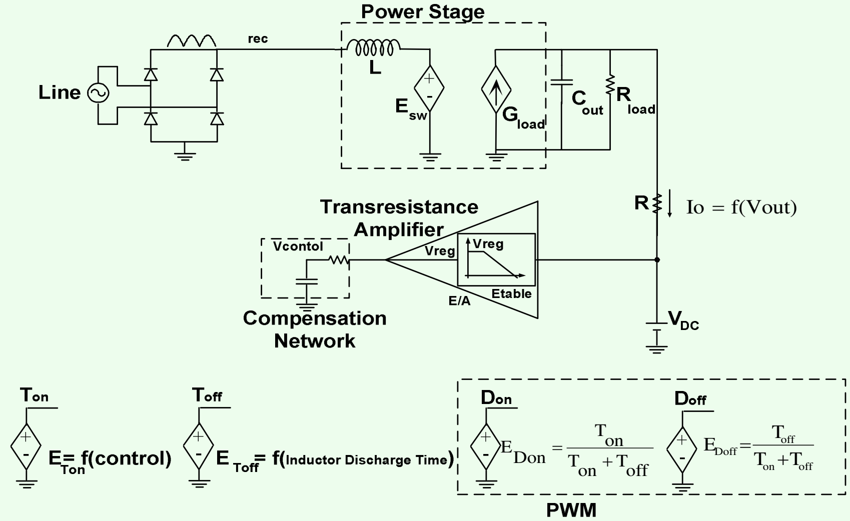


Principle of Operation

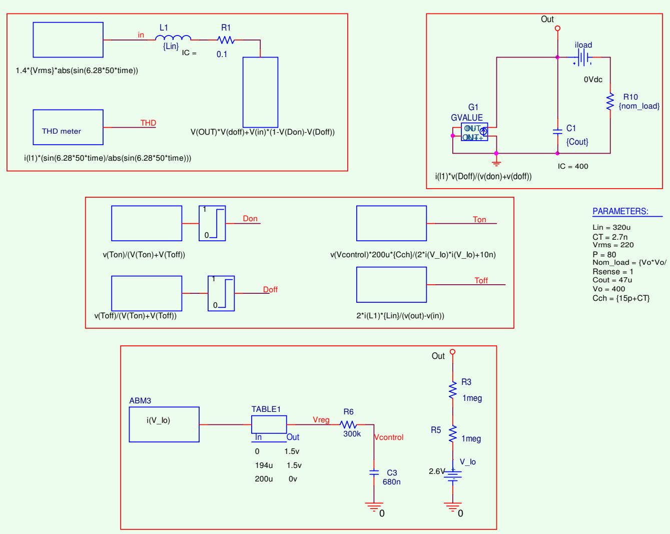


$$I_{pk}(t) = 2I_{av}(t) = \frac{V_{in}}{L} T_{on} \qquad \frac{V_{in}(t)}{I_{av}(t)} = \text{const. if } T_{on} = \text{const.}$$

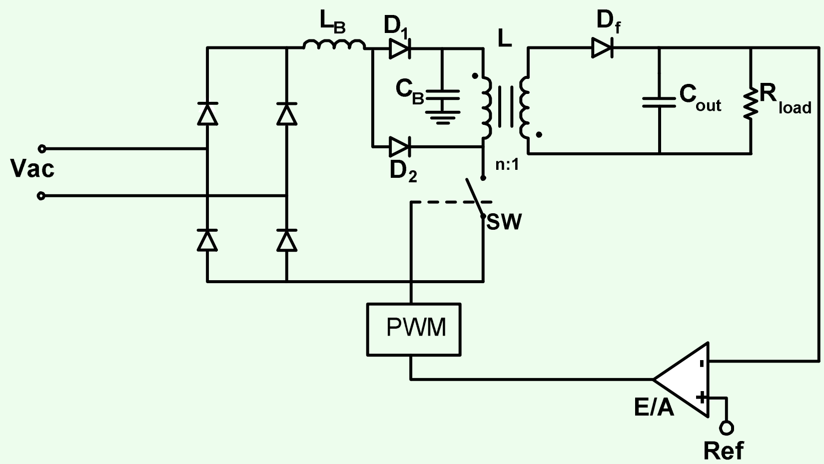
MC33260 Based Average Model



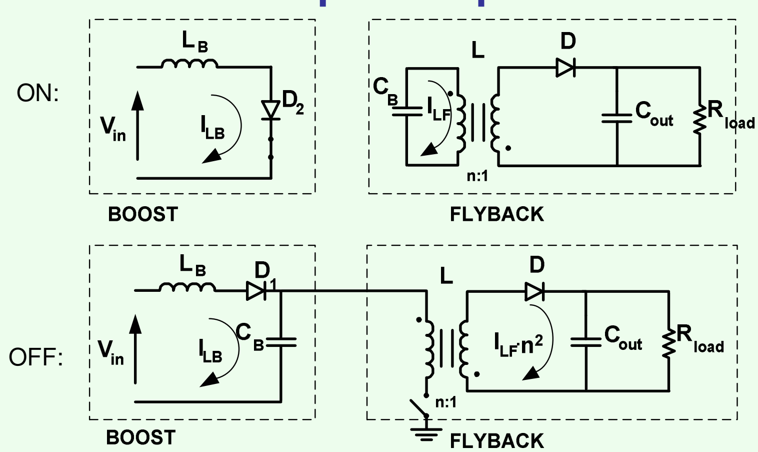
MC33260 Based Average Model



Combined Stage (Boost-Flyback)

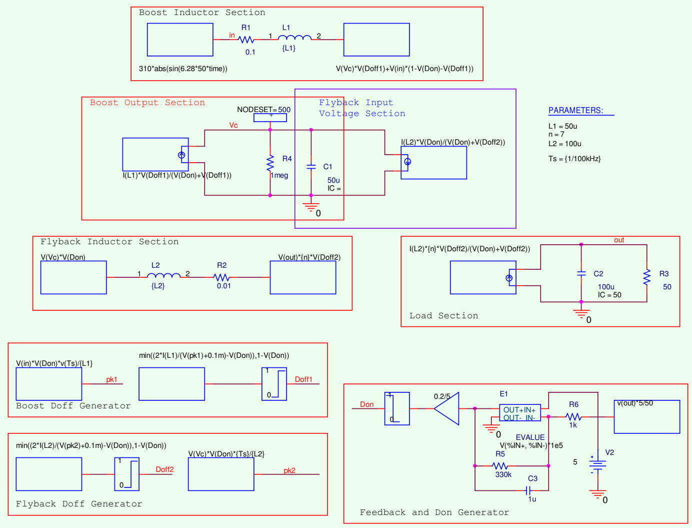


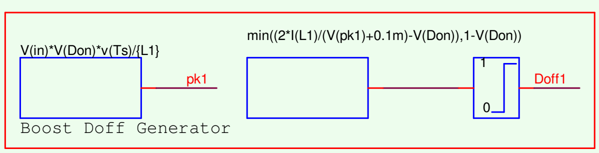
Principle of Operation



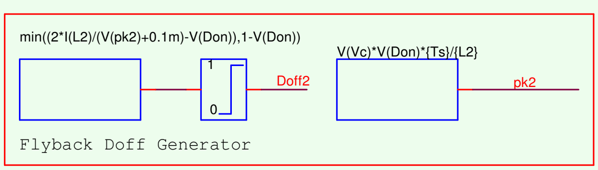
- C_B serves as output capacitor for Boost Section and as input voltage source for Flyback section.

Average Model



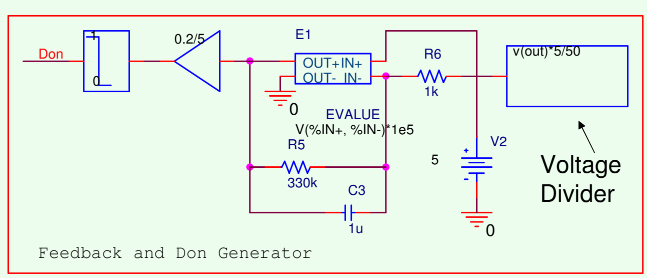


Doff Generator for Boost Section

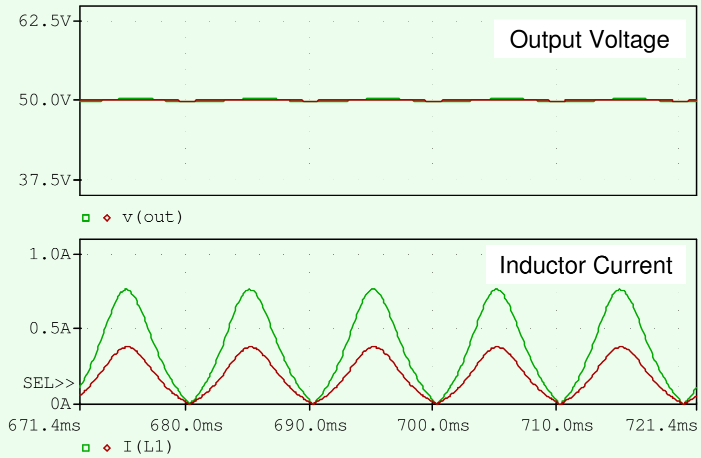


Doff Generator for Flyback Section

Error Amplifier and Don generator

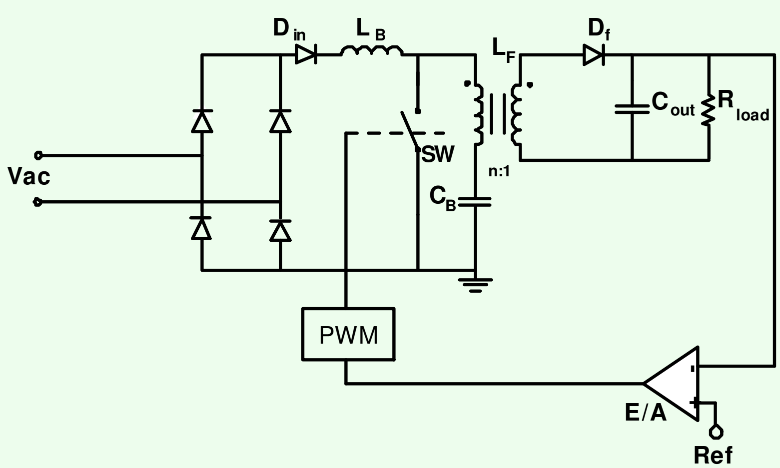


Behavior at Different Power Levels

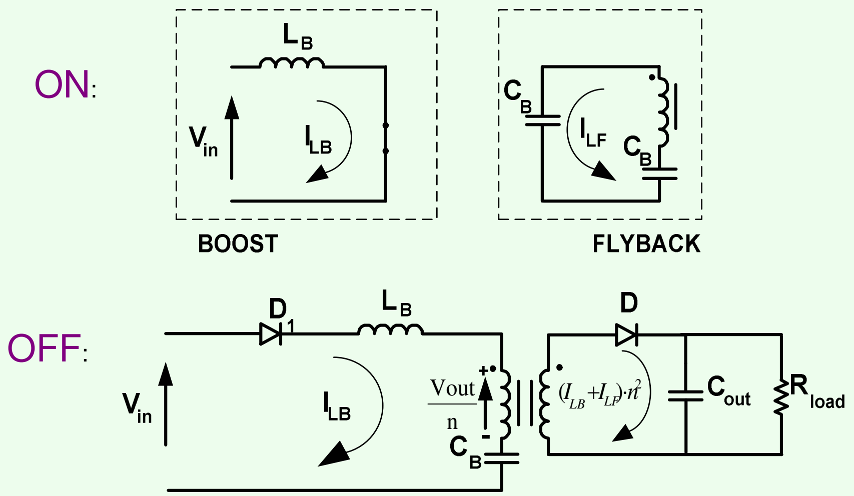


Vin=230V, Pout=100W, 50W

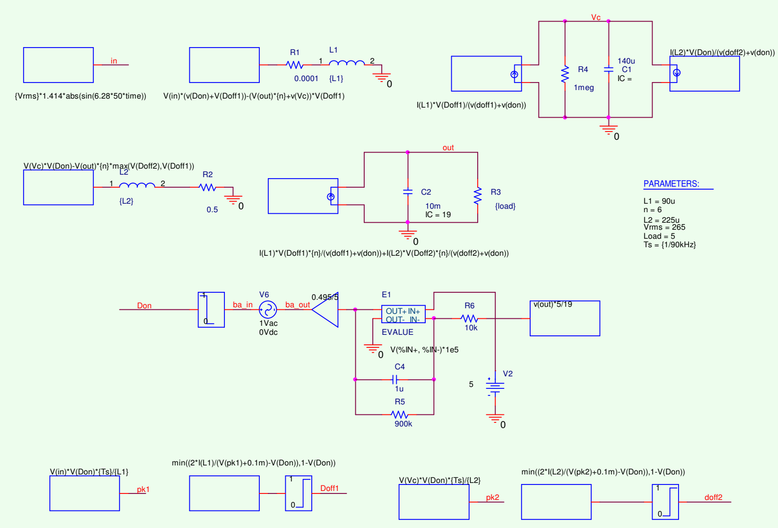
Combined Stage (SEPIC with Transformer)



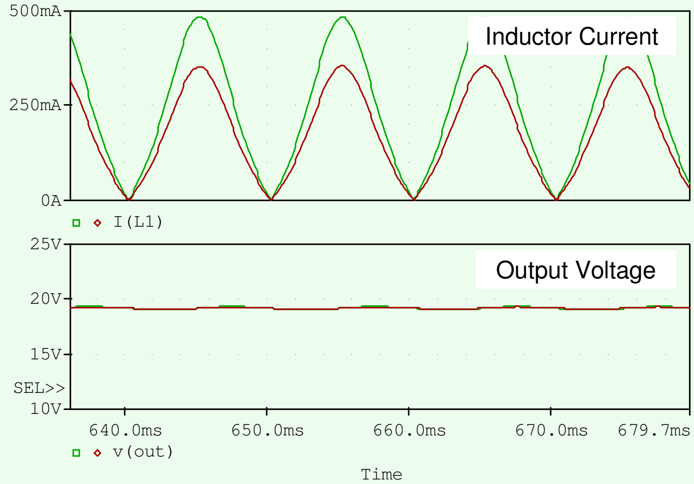
Principle of Operation



Average Model



Behavior at Different Power Levels



Vin=230V, Pout=70W, 50W

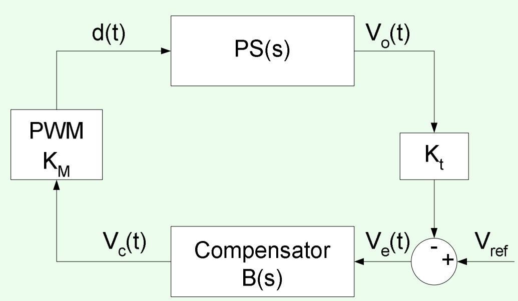
PSpice simulation

PFC_DCM - avg

PFC_DCM - CBC

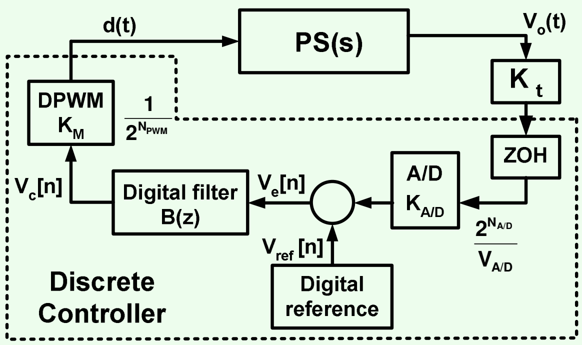
9. Digital Control

Analog/continuous control



$$LG(s) = K_t K_M PS(s) B(s)$$

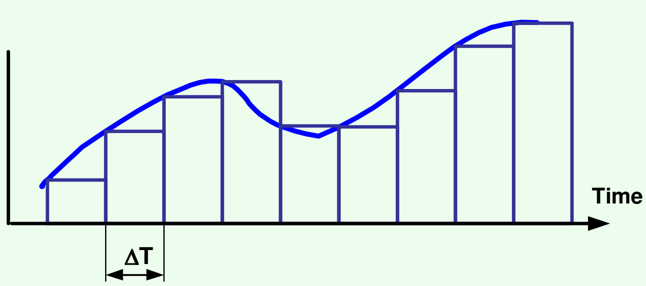
Digital/discrete control



$$LG = K_t K_M K_{A/D}\, e^{-s\Delta T} PS(s) B(z) \qquad e^{-s\Delta T} \Leftrightarrow \frac{1}{z}$$

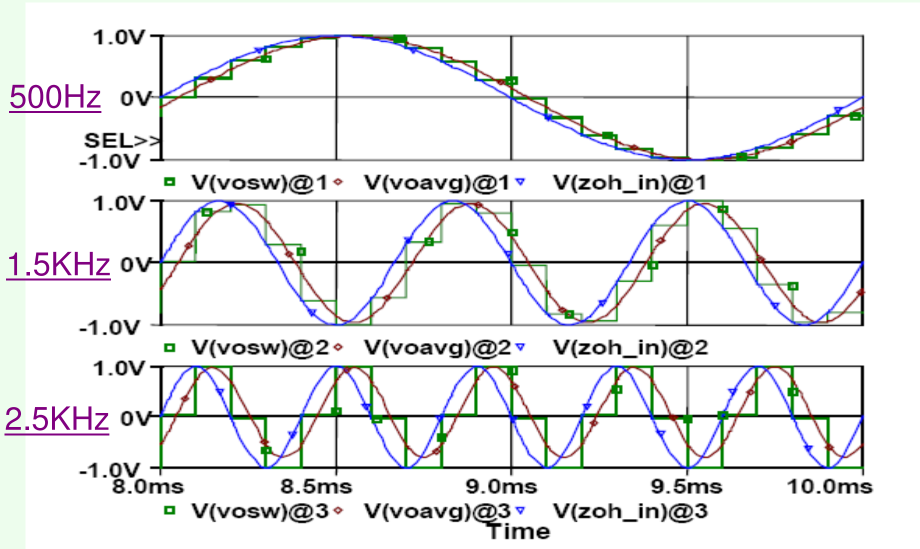
- Sampling and computation delay
- Additional gain – $K_{A/D}$

Sampling Issues
ZOH

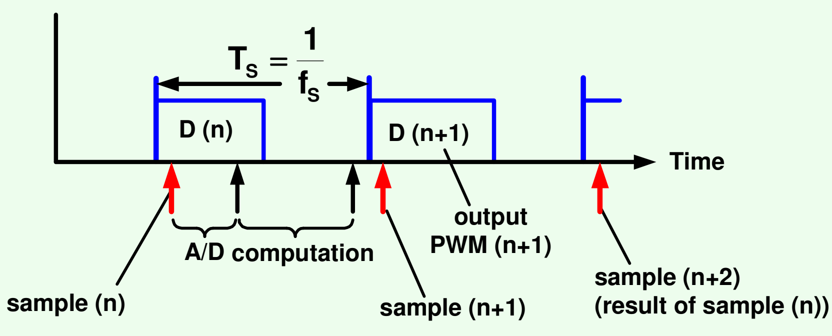


ZOH

fs=10KHz

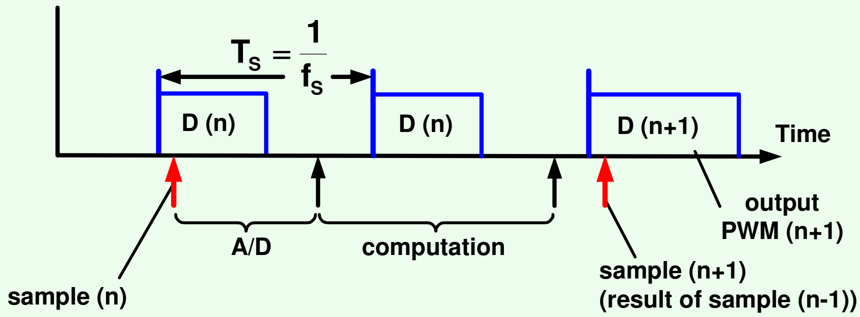


Sampling Delays



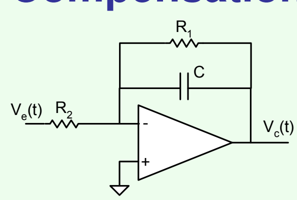
Sampling rate = f_s

Slow Sampling Rate



Sampling rate = $\frac{f_S}{2}$

Compensation network, continuous



$$K = \frac{R_1}{R_2}$$

$$\tau = R_1 C$$

$$\frac{V_e(t)}{R_2} = -C\frac{dV_c(t)}{dt} - \frac{V_c(t)}{R_1}$$

Differential equation: $$-KV_e(t) = \tau\frac{dV_c(t)}{dt} + V_c(t)$$

Integral equation: $$-K\int V_e(t)dt = \tau\int dV_c(t) + \int V_c(t)dt$$

Laplace transform: $$-\frac{K}{s}V_e(s) = \tau V_c(s) + \frac{1}{s}V_c(s)$$

Transfer function: $$\frac{V_c(s)}{V_e(s)} = -\frac{K}{s\tau + 1}$$

Discretization rules

Differential equations transforms to difference equations

$$\frac{dV(t)}{dt} \Rightarrow \frac{V[n]-V[n-1]}{\Delta T}$$

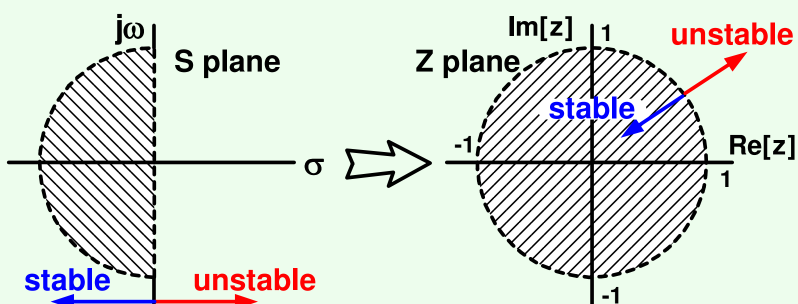
Integral equations transforms to summations

$$\int V(t)dt \Rightarrow \Delta T \sum_{k=-\infty}^{n-1} V[k]$$

Z-transform is the discrete time dual of the Laplace transform

$$V(s)=\int_{-\infty}^{\infty} V(t)e^{-st}dt \Leftrightarrow V(z)=\sum_{k=-\infty}^{\infty} V[k]z^{-k}$$

Transfer functions are represented in Z



$$\frac{v_o}{v_e} = \frac{1}{z+a} = \frac{z^{-1}}{1+az^{-1}}$$

$$v_o(1+az^{-1}) = v_e z^{-1}$$

$$v_o = v_o(n-1)\cdot a + v_e(n-1)$$

Unstable if a>1

The intuitive meaning of the z operator

s ⇒ derivative operator; z ⇒ Delay operator

$$\frac{v_o}{v_{in}}(z) = \frac{z}{z^2 - 1}$$

$$\frac{v_o}{v_{in}}(z) = \frac{z^{-1}}{1 - z^{-2}}$$

$$v_o(1 - z^{-2}) = v_{in}\,z^{-1}$$

$$v_o = v_o\,z^{-2} + v_{in}\,z^{-1}$$

$$v_o = v_o\,(n-2) + v_{in}\,(n-1)$$

Continuous to discrete transformation

- Pole-Zero matching
- Zero Order Hold (ZOH)
- Trapezoid (bilinear) transformation

Pole-Zero matching

- Map discrete poles/zeros by $z_i = e^{s_i \Delta T}$
- For complex s-domain roots $s_i = a_i + jb_i \rightarrow z_i = e^{a_i \Delta T} e^{jb_i \Delta T}$
- Maintain same DC gain $G(s)_{|s=0} = G(z)_{|z=1}$

$$\frac{V_c(s)}{V_e(s)} = \frac{K}{s\tau + 1} \xrightarrow{Z} \frac{KP}{z - e^{-\Delta T/\tau}}$$

$$\boxed{\left(a_i = \frac{1}{\tau}; b_i = 0\right)}$$

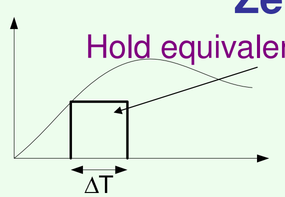
$$\frac{V_c(s)}{V_e(s)}_{|s=0} = \frac{V_c(z)}{V_e(z)}_{|z=1} \rightarrow P = 1 - e^{-\Delta T/\tau}$$

$$\frac{V_c(z)}{V_e(z)} = \frac{K\left(1 - e^{-\Delta T/\tau}\right)}{z - e^{-\Delta T/\tau}} = \frac{m}{z - n}$$

m, n - constants

Zero Order Hold (ZOH)

Hold equivalent = sampled area



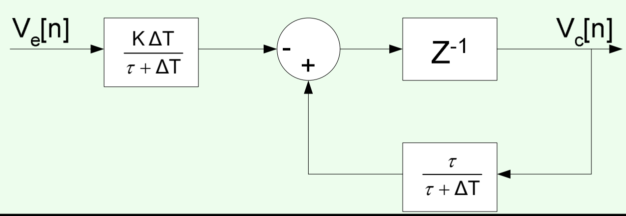
$$s \Leftrightarrow \frac{z-1}{\Delta T}$$

$$\frac{V_c(s)}{V_e(s)} = \frac{K}{s\tau + 1}$$

$$\frac{V_c(z)}{V_e(z)} = \frac{K}{\frac{z-1}{\Delta T}\tau + 1}$$

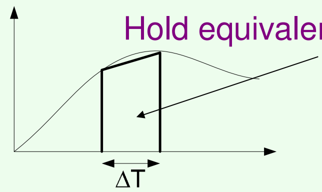
Transfer function:

$$\frac{V_c(z)}{V_e(z)} = \frac{K\Delta T}{\Delta T + \tau}\left(\frac{1}{z - \frac{\tau}{\Delta T + \tau}}\right) = \frac{m}{z - n}$$



Trapezoid (bilinear) transformation

Hold equivalent = sampled area

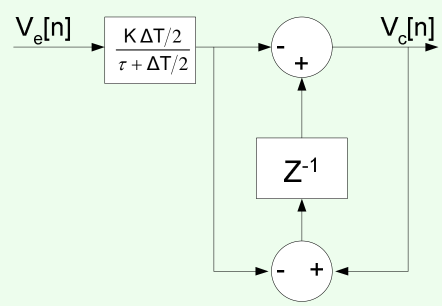


$$\frac{V_c(s)}{V_e(s)} = \frac{K}{s\tau + 1} \qquad s \Leftrightarrow \frac{2}{\Delta T}\frac{z-1}{z+1}$$

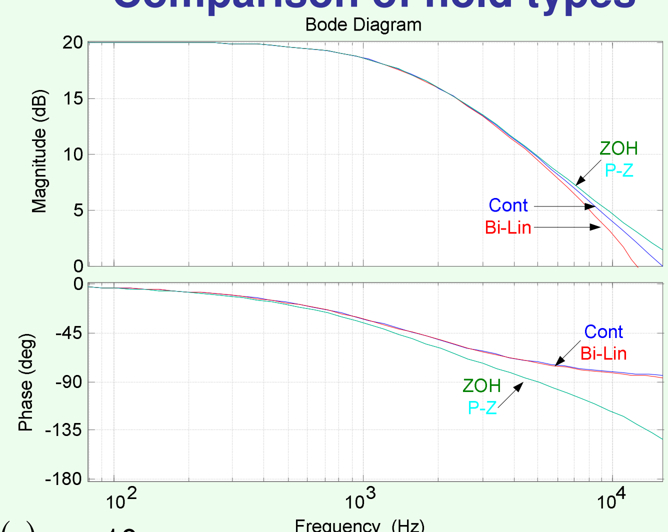
Transfer function:

$$\frac{V_c(z)}{V_e(z)} = \frac{K}{\frac{2\tau}{\Delta T}\frac{z-1}{z+1} + 1}$$

$$\frac{V_c(z)}{V_e(z)} = \frac{K\,\Delta T/2}{\tau + \Delta T/2}\left(\frac{z+1}{z-1}\right)$$



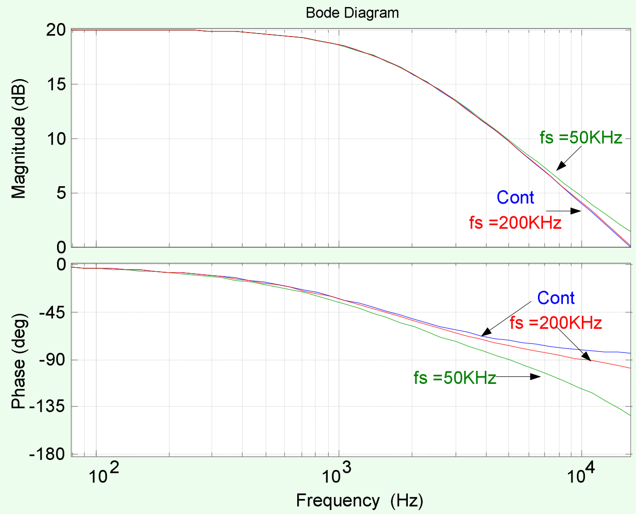
Comparison of hold types



fs=50KHz

$$\frac{V_c(s)}{V_e(s)} = \frac{10}{0.1s + 1}$$

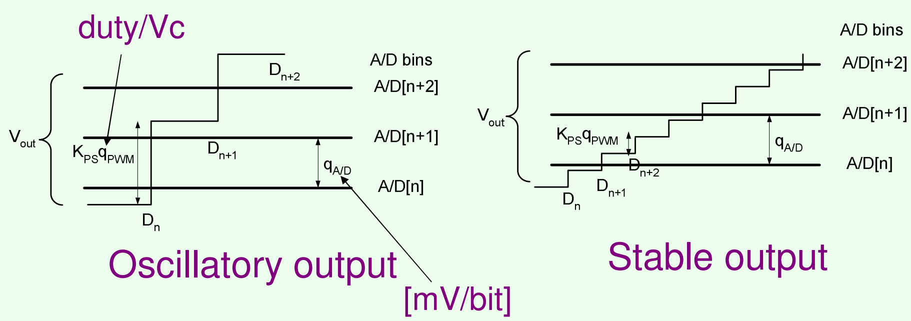
Effects of sampling rate



Hold Type: ZOH

Discretization: Inherent Phase-lag

A/D and PWM Resolution The Limit Cycle Problem



No Limit cycle rules

One bit of the DPWM should change V_o by less than 1 bit of the A/D

Taking into account the system gains

$$K_{PS} K_t q_{DPWM} < q_{A/D}$$

Compensator must include integral action (included in PID)

System must satisfy Nyquist criterion

$$1 + A(s)B(s) > 0 \qquad\qquad 1 + A(s)B(s) \neq 0$$

Stability | Oscillations

Digital Compensator Design Methods

- Frequency domain based
- Pole location in z plane
- Time domain design

Frequency domain design

1. Design a frequency domain controller (Bode, Nichols, etc.)
2. Refinement: take into account the sampling and computational delays
3. Translate the analog controller into a Z equivalent
4. Simulate by numerical simulator (e. g. MATLAB)

Frequency domain design
References

[1] V. Yousefzadeh, W. Narisi, Z. Popovic, and D. Maksimovic, "A digitally controlled DC/DC converter for an RF power amplifier", IEEE Trans. on PE, Vol. 21, 1, 164-172, 2006.

[2] G. F. Franklin, J. D. Powell, M. L. Workman, Digital control of dynamic systems, 3rd edition, Prentice Hall, 1998.

[3] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters", *IEEE Trans. on PE*, Vol. 18, 1, 2, 438-446, 2003.

Z Plane Design
Using the MATLAB SISO tool

1. Define the system structure
2. Define the Plant response
3. Define the compensator template
4. Select the analysis view (Root Locus, Bode, Nichols)
5. Insert design constraints (gain, BW, PM, settling time, Natural frequency, etc.)
6. You can use the GUI to change pole/zero locations (either in S or Z and observe the resulting closed loop response

- Trial and error procedure

MATLAB SISO tool
References

[1] O. Garcia, A. de Castro, A. Soto, J. A. Oliver, J. A. Cobos, J Cezon, “Digital control for power supply of a transmitter with variable reference”, *IEEE Applied Power Electronics conference APEC-2006*, 1411-1416, Dallas, 2006.

[2] The Mathworks, Matlab control toolbox user guide, available at www.mathworks.com.

Time domain Discrete Controller Design

- Digital compensator operates in the sampled-data domain
- Direct controller design - does not involve errors related to approximations (s to z)
- When working in the time domain, system attributes such as bandwidth and phase margin seem artificial
- Relevant parameters are: rise time, overshoot etc.
- Improved performance of the closed loop system compared to other discrete design approaches
- Does not involve trial and error procedure

Time domain Discrete Controller Design
References

[1] G. F. Franklin, J. D. Powell, M. L. Workman, Digital control of dynamic systems, 3rd edition, Prentice Hall, 1998.

[2] J. R. Ragazzini and G. F. Franklin, Sampled-data control systems, McGraw-Hill, 1958.

[3] J. G. Truxal, Automatic feedback control systems synthesis, McGraw-Hill, 1955.

[4] B. Miao, R. Zane, and D. Maksimovic, "Automated Digital Controller

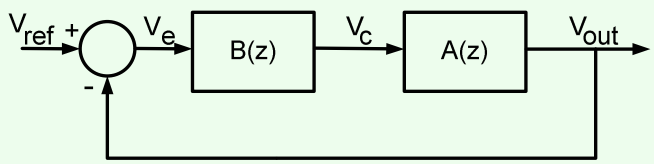
[5] Design for Switching Converters", ***IEEE Power Electronics Specialists Conference, PESC-2005*****, 2729-2735, Recife, 2005.**

NEW **[6] M. M. Peretz and S. Ben-Yaakov, Time domain design of digital compensators for PWM DC-DC converters,** ***IEEE Applied Power Electronics conference APEC-2007, In Press.***

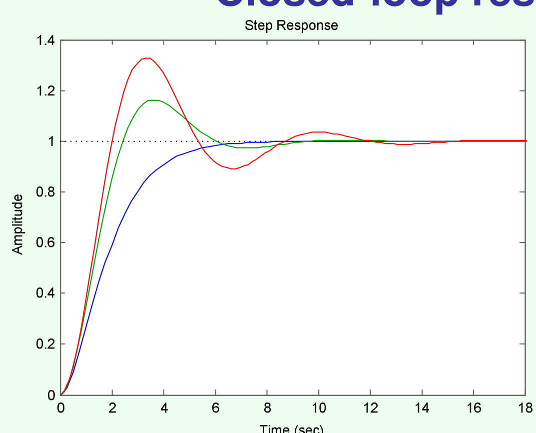
Time domain Discrete Controller Design

- Plant transfer function (continuous): A(s)
- S to Z transformation: A(s) -> A(z)
- Defining the desired closed loop response: $A_{CL}(s)$
- S to Z transformation: $A_{CL}(s)$ -> $A_{CL}(z)$
- Ideal controller:

$$A_{CL}(z) = \frac{A(z)B(z)}{1 + A(z)B(z)} \rightarrow B(z) = \frac{A_{CL}(z)}{1 - A_{CL}(z)} \frac{1}{A(z)}$$



Closed-loop response



$$45^\circ < \varphi_m < 90^\circ$$

2nd order system

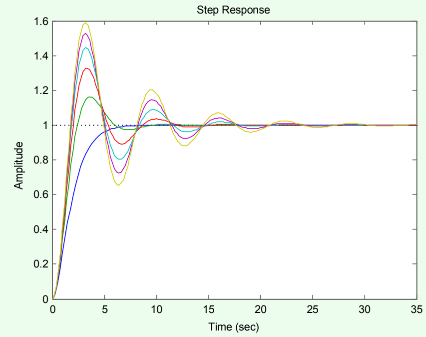
$$\frac{1}{\frac{s^2}{\omega_n^2} + \frac{s}{\omega_n Q} + 1}$$

Design constraint:
System will have the characteristic equation

Describing the closed-loop response by time domain characteristics

2nd order system

$$\frac{V_o(s)}{d(s)} = \frac{1}{\frac{s^2}{\omega_n^2} + \frac{s}{\omega_n Q} + 1}$$



Rise time: $t_r \approx \frac{1.8}{\omega_n} \Rightarrow \omega_n \approx \frac{1.8}{t_r}$

Overshoot $M_p = e^{-\frac{\pi}{2Q} / \sqrt{1 - \frac{1}{4Q^2}}} \Rightarrow Q = -\frac{\sqrt{1 + \left(\frac{\ln(M_p)}{\pi}\right)^2}}{2\frac{\ln(M_p)}{\pi}}$

Describing the desired A_{CL} in Z

- Second order characteristic equation sets the $A_{CL}(z)$ denominator (a_0, a_1, a_2)

$$\frac{}{\frac{s^2}{\omega_n^2} + \frac{s}{\omega_n Q} + 1} \xrightarrow{Z} \frac{b_0 z^2 + b_1 z + b_2}{a_0 z^2 + a_1 z + a_2}$$

- To derive the complete A_{CL} equation (i. e. numerator) additional constraints are to be satisfied:
- Stability at infinity (bounded system) $A_{CL}(z)_{|z=\infty} = 0$
- Steady state error to step $A_{CL}(z)_{|z=1} = 1$
- Response to ramp (velocity constant) $\frac{dA_{CL}(z)}{dz}_{|z=1} = \frac{1}{K_V}$

Template-oriented controller

•Ideal controller to satisfy the design constraints

$$B(z)_{ideal} = \frac{A_{CL}(z)}{1 - A_{CL}(z)} \frac{1}{A(z)}$$

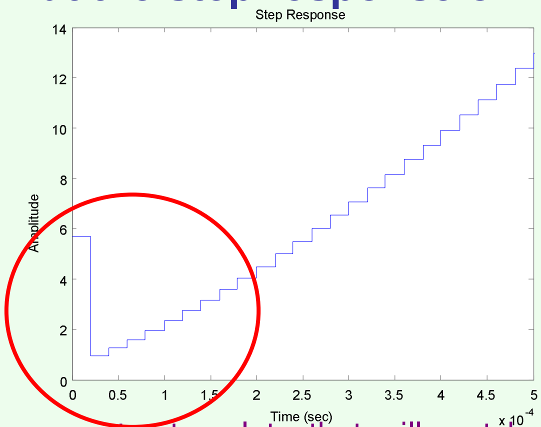
This design method suffers from:

- controller implementation on digital platform vary by design (plant, A_{CL}, etc.)
- High order - too many parameters – long computation time

Template-based controller

- In each computational event, only data points around the sampling instant are considered
- The controller uses only information that is in the vicinity of the sampling instant and is blind to all other information
- The implemented finite difference equation can be based on a short-term time response of the system rather than on the full response

A look at the step response of $B(z)_{ideal}$



Objective:

- Find a compensator template that will match (or will be close to) the the ideal response – at least at the first few samples
- The compensator should have fewer computation cycles

The answer - PID controller

PID template: continuous

$$\frac{V_c(s)}{V_e(s)} = \frac{\frac{s^2}{\omega_c^2} + \frac{s}{\omega_c Q} + 1}{s}$$

PID template: discrete p-z matching

$$\frac{V_c(z)}{V_e(z)} = \frac{a + bz^{-1} + cz^{-2}}{z^{-1} - z^{-2}}$$

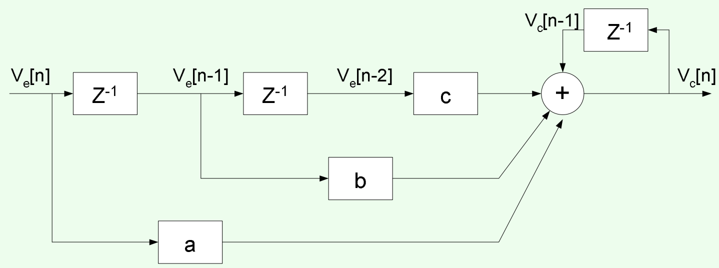
Taking into account the sampling delay (A/D)

$$\frac{V_c(z)}{V_e(z)} = \frac{a + bz^{-1} + cz^{-2}}{1 - z^{-1}}$$

PID controller

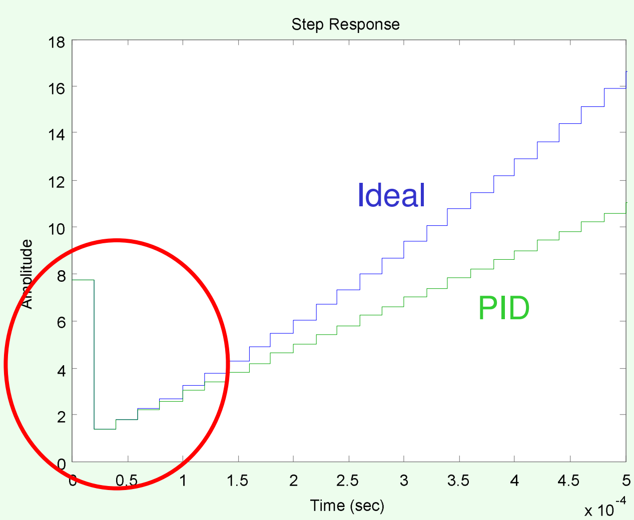
Difference Equation (will be implemented on the digital platform)

$$V_C[n] = V_C[n-1] + aV_e[n] + bV_e[n-1] + cV_e[n-2]$$



Only 3 samples!!!
Only 4 computations!!!

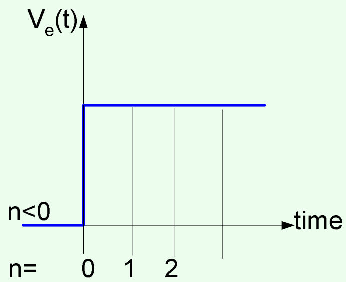
Extracting PID coefficients (a, b, c)

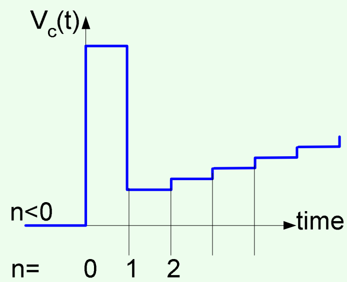


PID coefficients extraction procedure

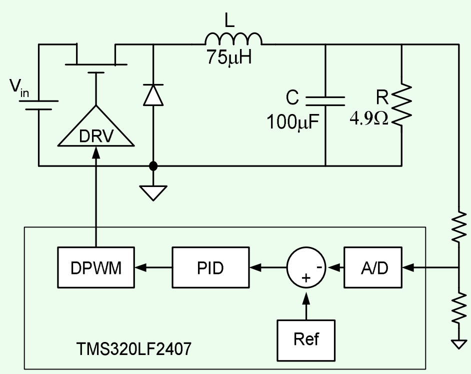
$$V_c[n] = V_c[n-1] + aV_e[n] + bV_e[n-1] + cV_e[n-2]$$

$$\begin{array}{ll} n=0 & \\ n=1 & \\ n=2 & \end{array} \begin{cases} V_c[0] = V_c[-1] + aV_e[0] + bV_e[-1] + cV_e[-2] \\ V_c[1] = V_c[0] + aV_e[1] + bV_e[0] + cV_e[-1] \\ V_c[2] = V_c[0] + aV_e[2] + bV_e[1] + cV_e[0] \end{cases}$$





Design example



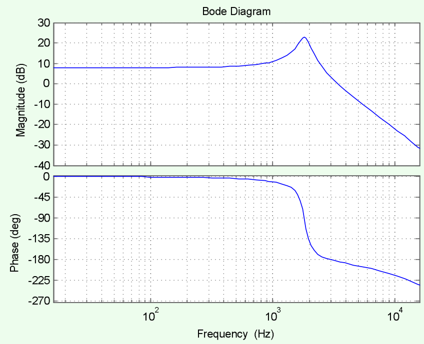
Vo = 5V Switching frequency=sampling rate= 50KHz

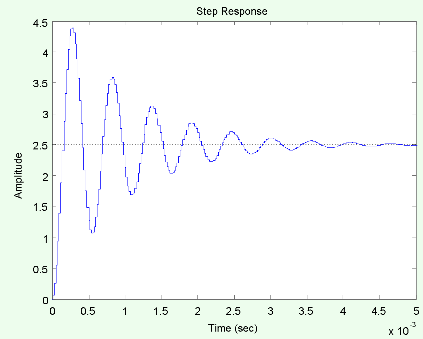
Tr=100u

Mp=10%

$$A_{CL}(z) = \frac{0.5044z + 0.4123}{z^2 - 1.403z + 0.4956}$$

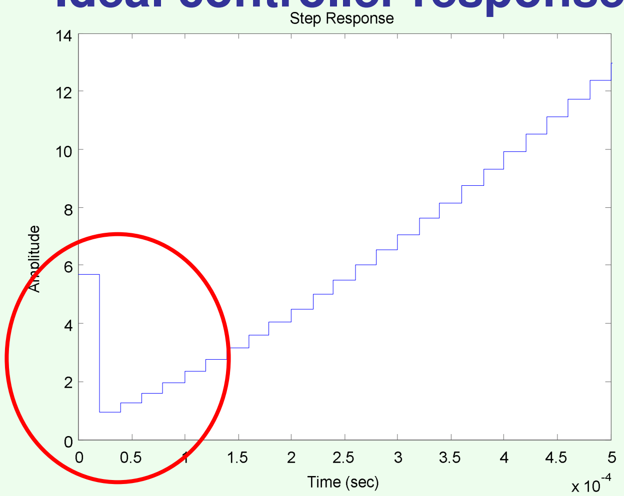
Plant response





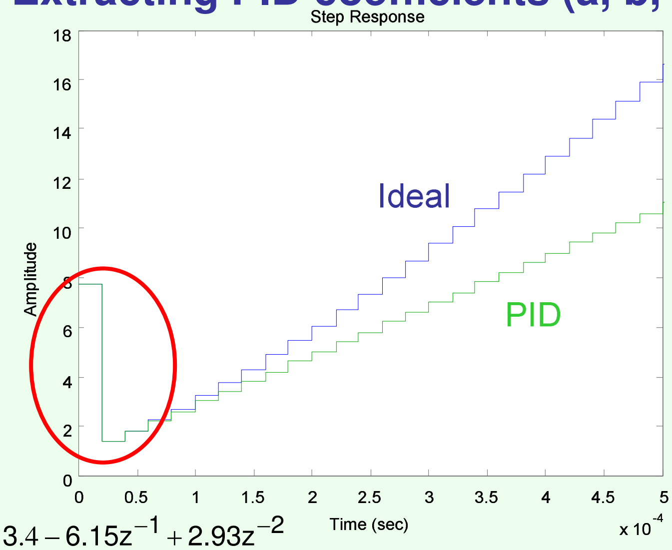
$$PS(s) = \frac{3.333 \cdot 10^8}{s^2 + 2500\,s + 1.333 \cdot 10^8} \xrightarrow{\text{ZOH}} PS(z) = \frac{0.06548\,z + 0.06459}{z^2 + 1.908z + 0.96}$$

Ideal controller response



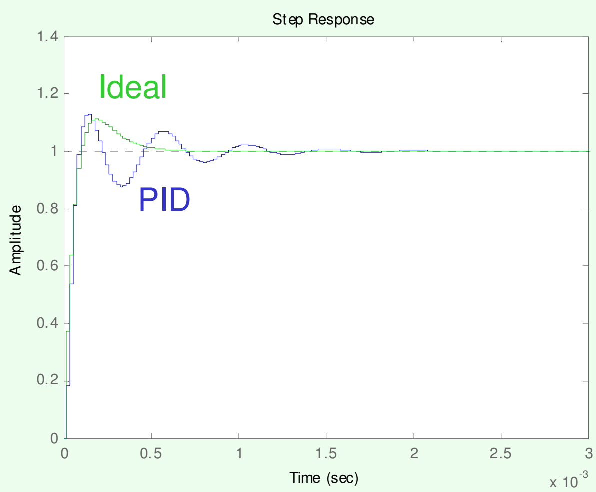
$$B(z) = \frac{0.5044z^3 - 1.375\,z^2 + 1.271z - 0.3958}{0.06548\,z^3 - 0.1249\,z^2 + 0.05945\,z}$$

Extracting PID coefficients (a, b, c)

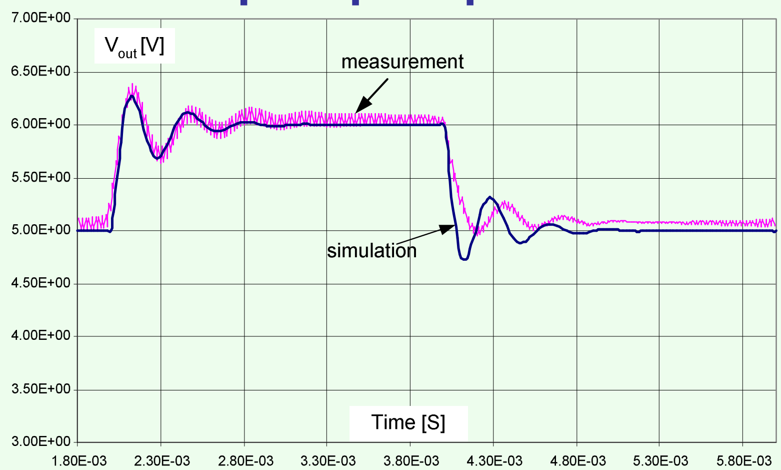


$$B(z)_F = \frac{3.4 - 6.15z^{-1} + 2.93z^{-2}}{1 - z^{-1}}$$

Closed loop response

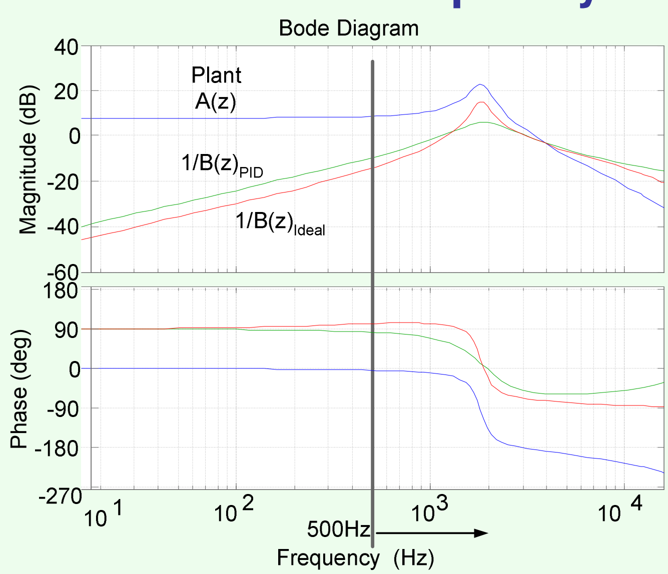


Closed loop step response - results



- Reference is stepped from 5V to 6V

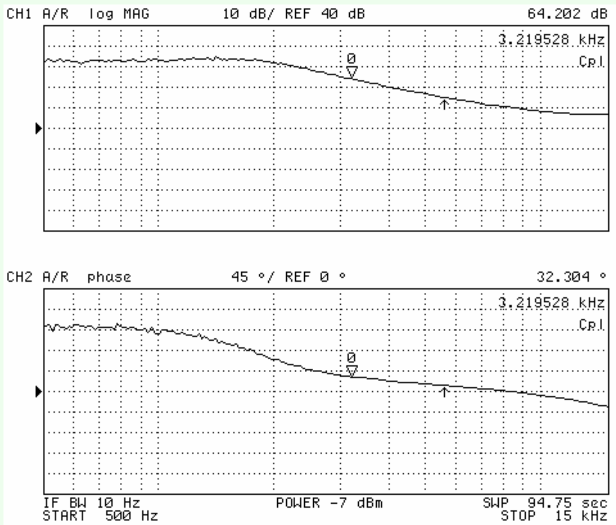
A look at the frequency domain



PM=40

BW=4KHz

Experimental



PM=33

BW=3.2KHz

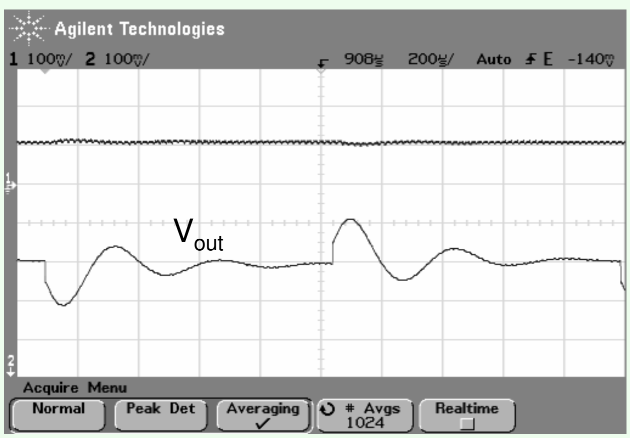
Load step

PID coefficients

a=3.4

b=-6.15

c=2.93



V_{out}

Slower Response

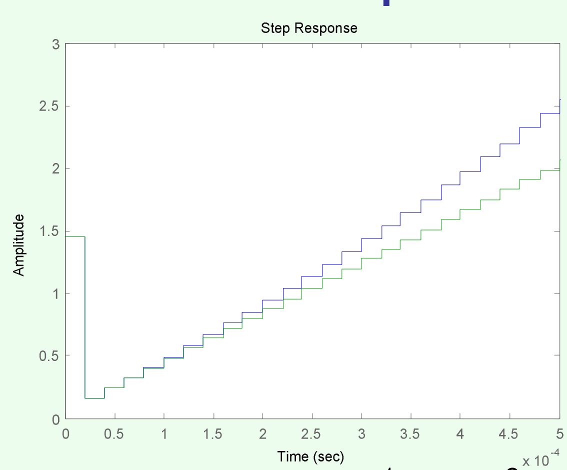
Switching frequency=sampling rate= 50KHz

Vo = 5V

Tr=500u

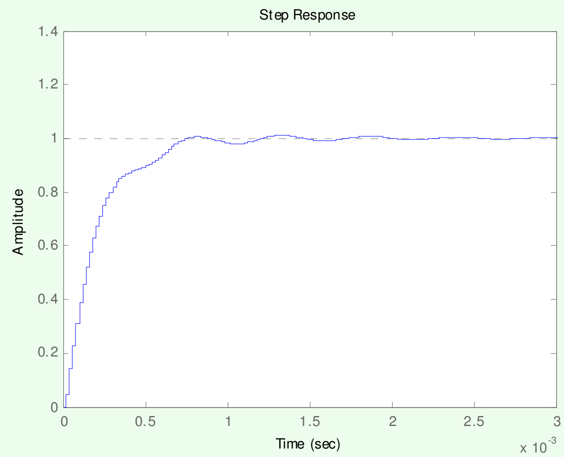
Mp=0% No over shoot

Controller response

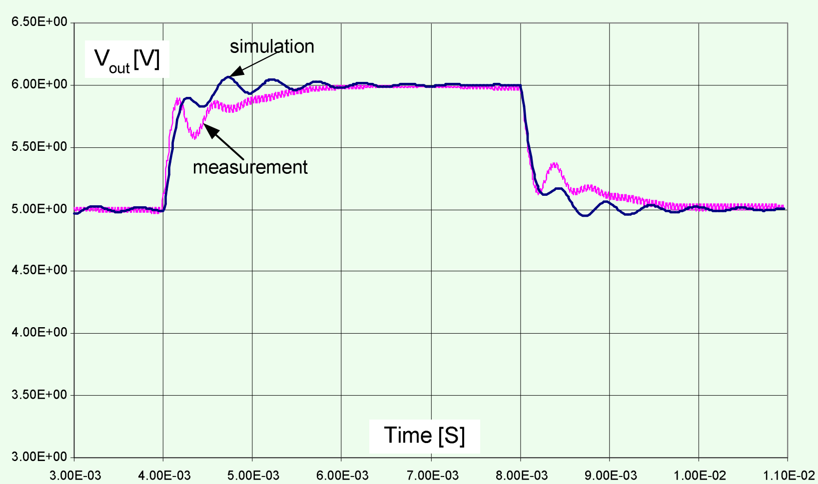


Derived PID: $B(z)_S = \dfrac{1.52 - 2.81z^{-1} + 1.38z^{-2}}{1 - z^{-1}}$

Closed loop

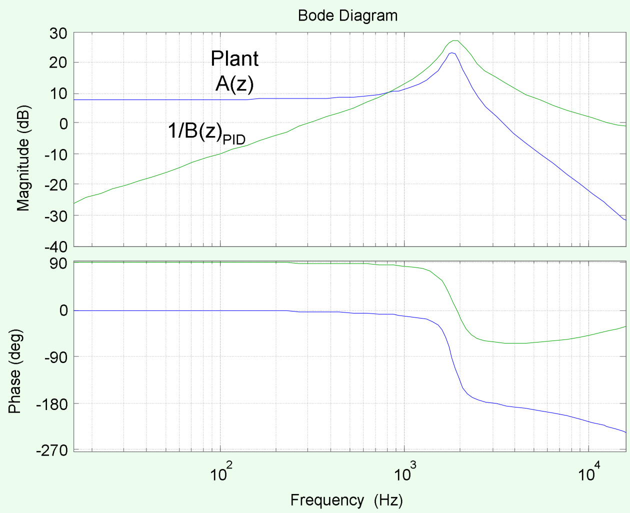


Closed loop step response - results



- Reference is stepped from 5V to 6V

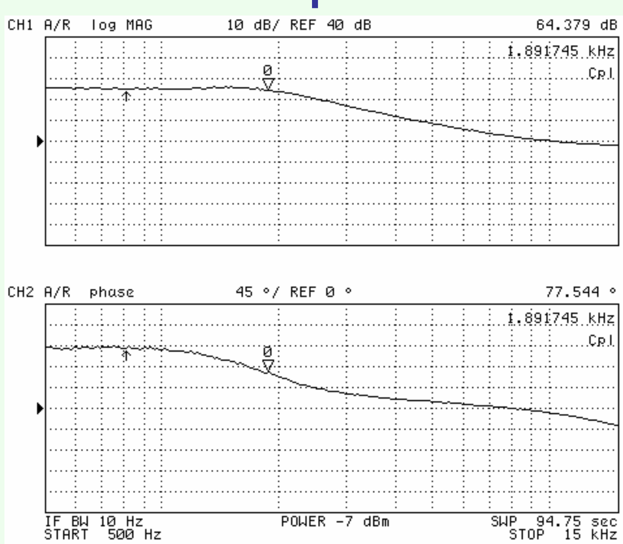
A look at the frequency domain



PM=80

BW=800Hz

Experimental



PM=80

BW=1.5KHz

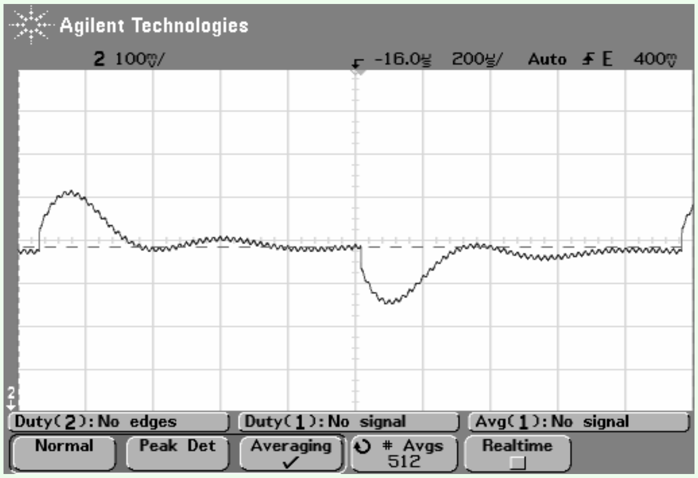
Load step

PID coefficients

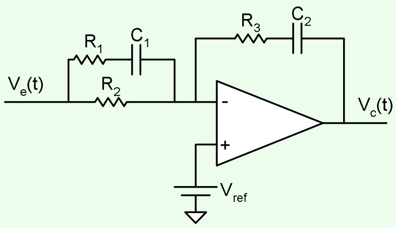
a=1.52

b=-2.81

c=1.38



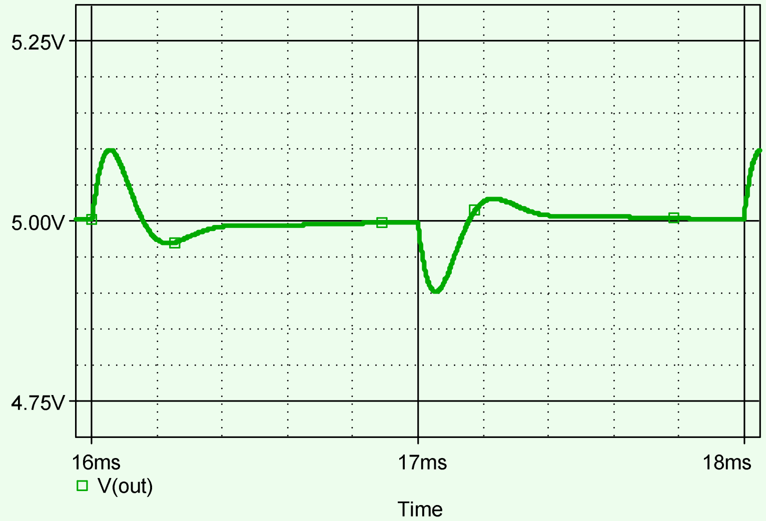
Comparison to analog design



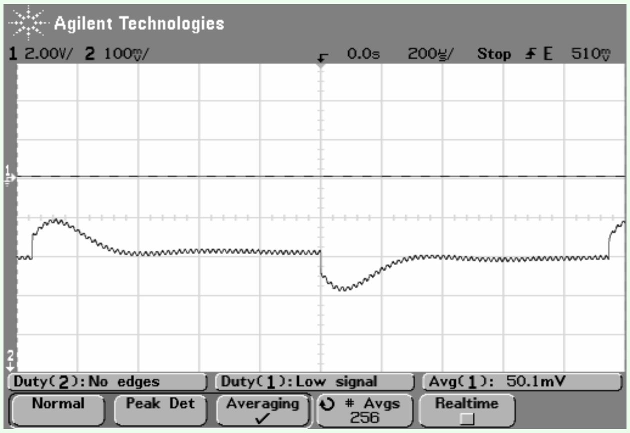
The analog controller was set to have the same bandwidth as the digital design

Load step applied: 1A to 1.5A

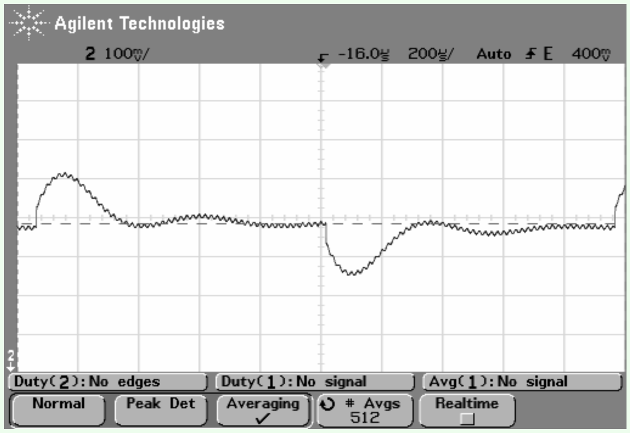
Load step - analog (Spice simulation)



Load step - analog



Load step digital



Thank you for Your Attention

Thanks to the Israeli Science Foundation for supporting our research

10. Q&A

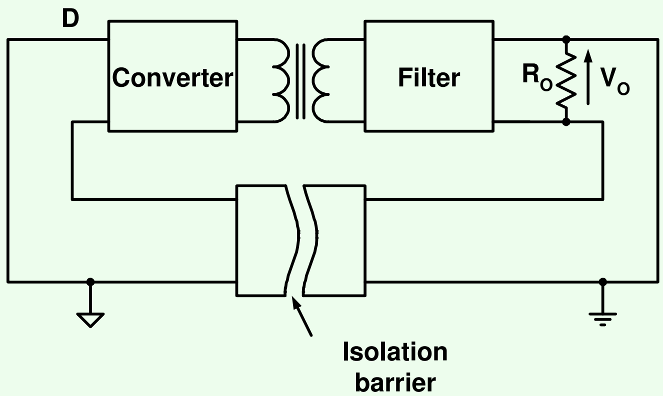
Sort Biography of Presenter

Prof. Shmuel (Sam) Ben-Yaakov

- BSc degree in Electrical Engineering from the Technion, Haifa Israel, in 1961
- MS and PhD degrees in Engineering from the UCLA, in 1967 and 1970 respectively.
- Full Professor at the Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva, Israel,
- Heads the Power Electronics Group of BG University
- Published over 250 scientific and technical papers in leading journals and conferences
- Holds about 20 patents (as an inventor)
- Consultant to companies worldwide on design-oriented theoretical issues in the areas of analog and power electronics as well as on product development.
- Founder and CTO of Green Power Technologies Ltd. (http://www.g-p-t.com)
- Present research interests include: power electronics aspects of piezoelectric elements, analog and digital control, power factor correction, lighting electronics, soft switching and active thermal cooling.

Primary to secondary isolation

The problem :



Alternative